BROOKTREE

PRODUCT DATABOOK

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Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121-2790
(619) 452-7580
(800) VIDEO IC
TLX: 383 596
FAX: (619) 452-1249

Brooktree®

PRODUCT DATABOOK 1991

Thank you for your interest in Brooktree products.

Our commitment is to provide a steady stream of innovative products that offer the highest quality, lowest cost/performance solutions and back them with comprehensive support services. These include timely and accurate technical information and responsive, experienced applications assistance.

At Brooktree, listening to our customer's requirements is what we do first. Solving our customer problems is what we do best.

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SECTION 1

INTRODUCTION

Company Facts

Brooktree began operations in 1983 following the development of an advanced architecture for data conversion. The architecture, invented by company co-founder and chief scientist Henry Katzenstein, permits the combination of high-performance analog and digital circuitry on a single monolithic integrated circuit which can be manufactured using standard bipolar or CMOS processes.

Brooktree Corporation is a privately held company located in San Diego, California. Facilities of 133,000 sq. ft house all design, test, and quality assurance activities as well as marketing, sales, and administration. Brooktree has established a worldwide network of distributors and factory representatives, with offices in the United States, Europe, and the Far East.

The company's products are manufactured under agreements with several domestic and international foundry sources. Second-source agreements are in effect with a number of suppliers.

Since its first volume shipments in 1985, Brooktree has achieved leadership share in the workstation graphics market, and a large share of the emerging markets for PC graphics and electronic imaging.

Products

Our first product, introduced in early 1985, was a 75 MHz 8-bit CMOS video digital-to-analog converter (VIDEODAC). By mid-1985, Brooktree had introduced six CMOS video digital-to-analog converter products (our VIDEODAC line) to the high-performance graphics market. Further system level integration led to our family of RAMDACs, which combine triple VIDEODACs, color palette RAMs, and pixel input multiplexers on a single chip. Recently introduced products include a 360 MHz bipolar RAMDAC and several next-generation CMOS RAMDACs.

In 1988, Brooktree entered the image acquisition market with it's first CMOS flash video A/D converter. Further system level integration led to our family of Image Digitizers, which combine one or more A/D converters and many additional functions required to digitize a video signal. Additional products are under development to enable image acquisition to be a "drop-in" solution.

Products for the automatic test equipment and instrumentation markets include programmable timing verniers, high-speed comparators, and load/driver/comparator circuits.

Strategy

Brooktree will combine the elements of its high-performance mixed signal design capabilities and proprietary test technology to provide a unique family of application-specific products. We will continue to develop highly-integrated products for use in computer graphics and imaging while introducing enabling technologies aimed at solving problems in the automatic test equipment and instrumentation markets.

Data Sheet Designations

Advance Information

This is the first official information released about a potential product. The datasheet contains basic information about the product and contains the target parametric and functional specifications. It usually precedes sample devices by approximately six months. This datasheet has the phrase "Advance Information" in the upper left corner on the front page.

Preliminary Information

This datasheet is released with sample devices. It contains a more extensive discussion of device operation and provides more complete parametric information. The functional operation is fully defined and the parametric information is the result of early testing of the initial devices. Not all of the parametric specifications may be fully tested or characterized. This datasheet has the phrase "Preliminary Information" in the upper left corner on the front page.

Final datasheet

This datasheet evolves from the Preliminary Information datasheet. It is a result of test information collected from fully characterized devices. This datasheet is distinguished by the absence of any designation, except the part number, at the top of the front page.

Device Designations

Engineering Sample

Devices which have exhibited most of the functionality for which it was designed. Engineering samples are used to enable selected customers to evaluate the device as early as possible. While some of the AC and DC parameters may be tested, the accuracy or completeness of the testing is not guaranteed. In addition, the product has not been put through Brooktree's quality and reliability testing. They have standard markings with an additional "ES" marked on top of the package. These devices have a Preliminary datasheet under document control.

Pre-Qual

These devices have production silicon, testing, and burn-in. Most characterization is done, but the device must still pass a QA life-test qual. These devices have standard markings with an additional "PQ" marked on top of the package. These devices have a Preliminary datasheet under document control.

Full Production

These devices have production silicon, testing, burn-in, and have successfully passed a QA life-test qual. These devices have standard markings with no additional designators. These devices have a Final datasheet under document control.

SECTION 2

QUALITY ASSURANCE

Introduction

The value of a product is measured by how well it is designed, manufactured and tested and how well it continues to perform over time. This value can be represented in quantitative terms by stating levels of quality and reliability. Brooktree determines these quality levels by performing industry recognized evaluation and monitoring programs for all products it manufactures.

Quality is a critical aspect of product success, and we have established an aggressive schedule of measuring, testing and monitoring the product to assure our customer that each device will perform to the highest quality and reliability standards. We have made substantial investments in experienced personnel and in state-of-the-art capital equipment for our design, manufacturing, and quality assurance departments.

Product Quality

Quality is a measure of product conformance to the specifications. This is determined by measuring the percentage of defects in a given sample size. The Quality Assurance program includes material inspections which employ industry-standard Lot Tolerance Percent Defective (LTPD) and Acceptable Quality Level (AQL) sampling plans. These sampling procedures assure with a high degree of confidence that a lot will not be approved for shipment if certain levels of quality are not met. For sampling plans, the operating characteristic curve illustrated in Figure 1 shows the relationship of lot quality versus probability of acceptance. Point A on the curve is termed AQL; it signifies the lot quality in percent defective (0.065%) that will give a high probability (95%) of lot acceptance. Point B on the curve is termed LTPD and signifies the unsatisfactory level of quality where the lot will be rejected 90% of the time. Brooktree performs quality conformance testing using an acceptance sampling method based on MIL-STD-105D and MIL-M-38510H.

Manufacturing process control is accomplished through the efforts of the Document Control Department. An effective plan for document sign-off and distribution ensures that updated documents are reviewed and are made available immediately to affected operations.

Brooktree's Quality Assurance program imposes strict requirements on vendors, and monitors their performance through inspection of incoming materials and regular audits of the vendor's facilities and quality methods. Figure 2 is a generalized standard product manufacturing flow which illustrates the manufacturing steps and quality assurance

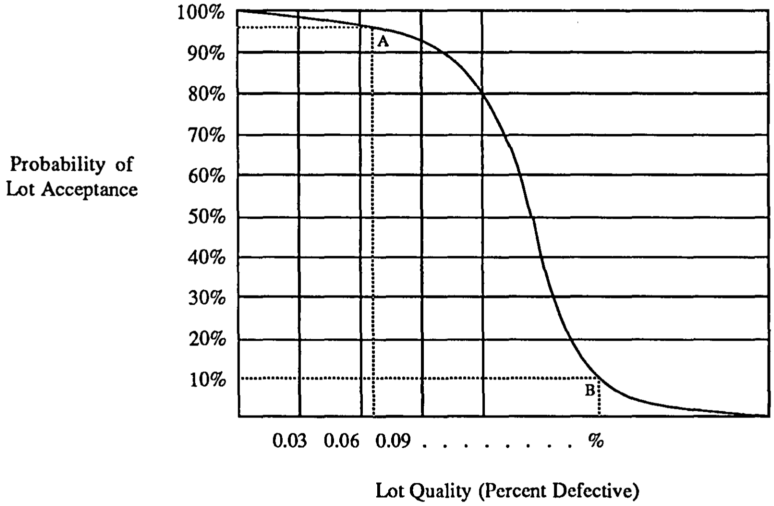

Figure 1. Lot Quality vs. Probability of Acceptance.

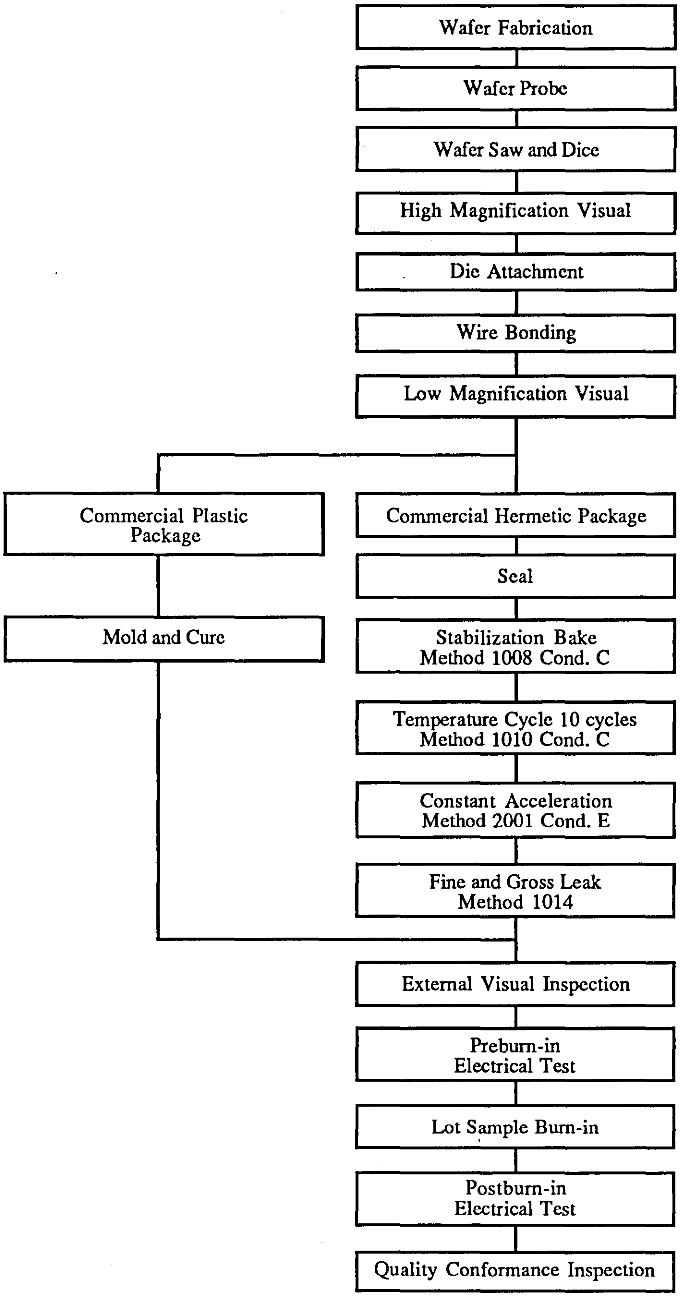
Wafer Fabrication
Wafer Probe
Wafer Saw and Dice
High Magnification Visual
Die Attachment
Wire Bonding
Low Magnification Visual
Commercial Plastic Package
Mold and Cure
Commercial Hermetic Package
Seal
Stabilization Bake Method 1008 Cond. C
Temperature Cycle 10 cycles Method 1010 Cond. C
Constant Acceleration Method 2001 Cond. E
Fine and Gross Leak Method 1014
External Visual Inspection
Preburn-in Electrical Test
Lot Sample Burn-in
Postburn-in Electrical Test
Quality Conformance Inspection

Figure 2. Standard Product Manufacturing Flow.

monitors used for all our products. The Brooktree quality assurance program conforms to the program guidelines as specified in MIL-Q-9858.

Product Reliability

Reliability is quality over time, a measurement of how long the product continues to perform to original specifications. This must be guaranteed by using a worst-case design methodology, precisely controlled wafer-processing, and manufacturing assembly and testing to highest quality standards.

Verification of product reliability is accomplished through accelerated life testing and physical and environmental stress testing. The stress tests performed for product qualification are listed in Tables 1 and 2. These tests are repeated at six-month intervals to verify continuing process and product integrity. Strict engineering change control procedures are used to assure a controlled process.

Screening is performed to eliminate early-failure devices and to conform to military requirements. Military grade products are tested in conformance to MIL-STD-883C. The basic method used to estimate product life is accelerated environmental testing. These tests expose the product to stresses greater than expected in actual use. The number of device failures that occur can be related to the magnitude of the stress applied. The common practice is to express the results in failures in 10^9 hours, or FITs (one FIT is equal to one failure per billion device hours of operation. It can also be expressed in the common notation of 0.0001% failures per 1000 hours).

Figure 3 is an idealized graph of device failure rate vs time, often called the Bathtub Curve. Three distinct regions are of importance. **Region A** is characterized by high failure rates that show up in early usage and then decrease with time. This area of early life failures needs to be eliminated prior to product being shipped to the final consumer. The early life failure rate is minimized by screening procedures, the most common of which is burn-in testing performed at the device and/or system level. **Region B** is characterized by a constant failure rate, and indicates the normal operating region that will assure maximum useful service and reliability. **Region C** indicates the wearout region where device failure rate increases. The wearout region is seldom reached in well-designed semiconductor integrated circuits under normal operating conditions. Results of accelerated life testing are extrapolated to estimates of in-service reliability through use of the Arrhenius model.

Product Development

Quality and reliability planning begins with the product development cycle. It is vital that every possible effort to increase the reliability is made during the development cycle. This is achieved by defining specific design goals, using proven reliable materials and manufacturing methods, and implementing controlled production processes with accurate testing and monitoring.

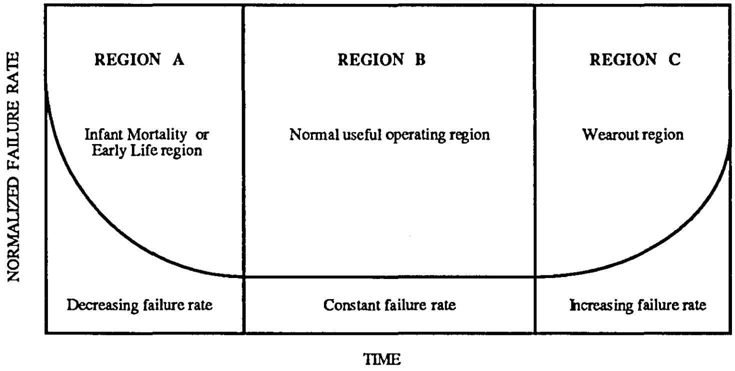

Figure 3. Device Failure Rate vs. Time.

Design

Brooktree's engineering department has established a comprehensive design methodology developed to produce reliable devices. Product definition begins with experienced system designers who can accurately specify the electrical interface and functional boundary requirements. This assures that all new devices will have specifications and worst case operating and environmental conditions identified before design begins.

Design engineers use schematic capture and simulation software to verify the operation of the design over temperature, power supply, and processing variations. Design reviews require designers to demonstrate to the Quality Assurance department that their design will meet or exceed reliability rules, including allowable amount of electrostatic discharge (ESD), latch-up protection (CMOS products), and current density (to prevent metal migration). Computer simulation of each circuit design is done using a worst case methodology.

Conformance to strict layout rules gives products immunity to process variation while maximizing reliability. An extensive set of checks is provided by several state-of-the-art CAD tools that assure the design layout is correct and that wafers can be consistently processed with confidence in yield and reliability.

Wafer Probe

Wafer probe is performed at Brooktree to ensure the tightest quality and reliability controls early in the life of the product. Wafer probe test conditions and limits are guard banded to ensure early removal of defective devices. Correlation between the final test programs and probe programs is an effective gate to prevent a nonfunctional device from entering the assembly operation. Rejected dice are marked with an ink dot to allow easy identification after the individual die is scribed from the wafer.

Device Assembly

The Quality Assurance department monitors the performance of various processing steps by requiring mandatory sampling of each lot moving through critical quality operations. We have instituted eight sampling points or gates in the assembly area: wafer inspection, material inspection, first QA die visual (high magnification), die attach control, second QA die visual (low magnification), QA hermeticity check, QA final inspection, and QA outgoing audit. Daily monitoring and audits of equipment and operators ensure that the final product meets all predefined quality criteria.

Device Packaging

Brooktree packaging uses standard, semi-custom and custom packages. Package outlines and foot prints comply with JEDEC and SEMI standards whenever possible. Since product performance is affected by packaging design, custom packages are constructed when necessary to preserve the reliability and performance of the enclosed device.

Final Testing

Final electrical testing is performed at Brooktree using state-of-the-art test equipment and techniques. Test parameters and test conditions are such that proper performance is guaranteed to data sheet requirements. Test limits are guard banded to compensate for tester inaccuracy, thereby minimizing measurement correlation errors between the factory and customer. To comply with quality conformance requirements, QA verifies proper processing, proper electrical performance over specified operating temperatures and voltage ranges, and visual criteria.

Qualification

All products we manufacture are labeled to show the classification of the products reliability for consumer use. Each product datasheet contains a designation as to the product development and specification parameters status. The product datasheet designations are Advanced, Preliminary, and Final. When the device has been fully characterized to all the specifications and datasheet parameters, and has completed the environmental tests outlined in Tables 1 and 2, it is labeled production-worthy and labeled a Final Data Sheet.

Failure Analysis

Even under the strictest of standards, failures do occur. To control this situation and learn from it, the failure analysis group identifies reliability problems and performs corrective action on failures from in-house stress testing as well as customer field returns. Brooktree provides customers with specific feedback so that the customer can be assured that appropriate action has been taken.

Description	Methods and Conditions*	Sample / Max. Reject	Notes
High Temperature Operating Life Electrical	2000 hours, TA = 125° C *** TA = Tmax	280 (<400 FIT) ****	electrical at 16, 48, 168, 500, 1000, 1500, 2000 hours
High Temperature Storage Electrical	2000 hours, TA = 200° C TA = Tmax	55 / 0	electrical at 500, 1000, 1500, 2000 hours
Temperature Cycle Electrical	Method 1010, condition C, –65° C / +150° C, 500 cycles TA = Tmax	116 / 0	
Thermal Shock Electrical	Method 1011, condition B, –55° C / +125° C, 200 cycles TA = Tmax	116 / 0	electrical every 500 cycles
Pre-conditioning Temperature Cycle Temperature Cycle Electrical	–40° C / +150° C, 20 cycles 0° C / +125° C 3000 cycles TA = Tmax	153 / 0	
Pre-conditioning Temperature Cycle Pre-conditioning Temperature/Humidity Steady-State Temperature/Humidity Electrical	–65° C / +150° C, 10 cycles 85° C / 85% RH, 24 hours, unbiased 85° C / 85% RH, 1500 hours, biased TA = Tmax	195 / 1	plastic package only electrical at 500, 1000, 1500 hours
Pressure Cooker Electrical	125° C, 2.3 atm, 288 hours TA = Tmax	77 / 1	plastic package only
Destructive Physical Analysis	SEM - surface and cross section	3 sets	1 set from each of 3 wafer lots

*Test methods reference MIL-STD-883C.

**Samples to be selected from 3 wafer lots (each lot shall be processed with a minimum of 1 week separating it and the other two wafer lots.

***Power supplies shall be set to 0.5 V less than the absolute maximum specified supply voltage; TA shall be reduced, if necessary, to guarantee TJ to be less than 175° C for ceramic packages, or less than 150° C for plastic packages.

****FIT shall be calculated using the Ahhrenius acceleration model and the following assumptions:
Ea = 0.5 eV if no failures; if failures, Ea to be determined based upon failure mechanism.
Ts = 55° C (derating temperature)
confidence level = 60%

*Table 1. Wafer Foundry Tests**.*

Description	Methods and Conditions*	Sample / Max. Reject	Notes
External Lead Plating Thickness	Method 2003	4 / 0	
Solderability		4 units / all leads	
Resistance to Solvents	Method 2015	4 / 0	
Internal Visual Bond Strength Die Shear	Method 2010 Method 2011 Method 2019	4 / 0	
External Lead Integrity	Method 2004, condition B	34 / 2	
Fine Leak	Method 1014 , condition A or B		for CERDIP only
Gross Leak	Method 1014 , condition C		for CERDIP only
Temperature Cycle	Method 1010, condition C, –65° C / +150° C, 500 cycles	116 / 0	
Electrical	TA = Tmax		
Thermal Shock	Method 1011, condition B, –55° C / +125° C, 200 cycles	116 / 0	
Electrical	TA = Tmax		
Preconditioning Temperature Cycle	–40° C / +150° C, 20 cycles	153 / 0	
Temperature Cycle	0° C / +125° C, 3000 cycles		
Electrical	TA = Tmax		electrical every 500 cycles
Steady-State Temp. and Humidity Visual	85° C / 85% RH, 1500 hours, biased	50 / 0	empty (dummy) packages may be used
Mechanical Shock	Method 2002, condition B	34 / 2	
Vibration	Method 2007, condition A		
Constant Acceleration	Method 2001, condition E, Y1 axis only		
Fine Leak	Method 1014, condition A or B		
Gross Leak	Method 1014, condition C		
Electrical	TA = Tmax		

*Table 2. Monolithic Hermetic Package Assembly Tests**.*

Description	Methods and Conditions*	Sample / Max. Reject	Notes
Salt Atmosphere Fine Leak Gross Leak	Method 1009 Method 1014, condition A or B Method 1014, condition C	34 / 2	
Resistance to Soldering Heat Fine Leak Gross Leak Electrical	15 sec dip to with 1/8" of body in solder at 260° C Method 1014, condition A or B Method 1014, condition C	22 / 0	
Destructive Physical Analysis	SEM - surface and cross-section	3 sets	1 set from each of 3 assembly lots

*Test methods reference MIL-STD-883C.

**Samples to be selected from 3 assembly lots (each lot shall be processed with a minimum of 1 week separating it and the other two assembly lots.

*Table 2. Monolithic Hermetic Package Assembly Tests**.*
(Continued)

Description	Methods and Conditions*	Sample / Max. Reject	Notes
External Lead Plating Thickness Solderability	Method 2003	4 / 0 4 units / 2 leads	
Resistance to Solvents	Method 2015	4 / 0	
X-Ray		4 / 0	
Mechanical Shock Electrical	Method 2002, condition B TA = Tmax	25 / 1	
Temperature Cycle Electrical	Method 1010, condition C, –65° C / +150° C, 500 cycles TA = Tmax	116 / 0	
Thermal Shock Electrical	Method 1011, condition B, –55° C / +125° C, 200 cycles TA = Tmax	116 / 0	
Preconditioning Temperature Cycle Temperature Cycle Electrical	–40° C / +150° C, 20 cycles 0° C / +125° C, 3000 cycles TA = Tmax	153 / 0	electrical every 500 cycles
Preconditioning Temperature cycle Preconditioning Temperature/Humidity Steady-State Temperature/Humidity Electrical	–65° C / +150° C 10 cycles 85° C / 85% RH, 24 hours, unbiased 85° C / 85% RH, 1500 hours, biased TA = Tmax	195 / 1	electrical at 500, 1000, and 1500 hours
Pressure Cooker Electrical	125° C, 2.3 atm, 288 hours TA = Tmax	77 / 1	

*Table 3. Monolithic Plastic Package Assembly Tests**.*

Description	Methods and Conditions*	Sample / Max. Reject	Notes
Salt Atmosphere	Method 1009	34 / 2	
High Temperature Operating Life Electrical	TA = 125° C (TJ < 150° C), 1500 hours TA = Tmax	150 (< 400 FIT) ***	electrical at 500, 1000, 1500 hours
Preconditioning Pressure Cooker Infra-Red Reflow (IR) Pressure Cooker Electrical	125° C, 2.3 atm, 72 hours 3 cycles 125° C, 2.3 atm, 200 hours TA = Tmax	45 / 0	PLCC packages only
Preconditioning Pressure Cooker Infra-Red Reflow (IR) Temperature Cycle Electrical	125° C, 2.3 atm, 72 hours 3 cycles Method 1010, condition C –65° C / +150° C, 500 cycles TA = Tmax	45 / 0	PLCC packages only
Preconditioning Temperature Cycle Preconditioning Temperature/Humidity Vapor Phase Solder Pressure Cooker Electrical / Visual	Method 1010, condition C, –65° C / +150° C, 20 cycles 85° C / 85% RH, 72 hours, unbiased 125° C, 2.3 atm, 200 hours TA = Tmax	45 / 0	PLCC packages only
Resistance to Soldering Heat Electrical	15 sec dip to within 1/8" of body in solder at 260 °C TA = 25 °C	22 / 0	
Destructive Physical Analysis	SEM - surface and cross-section	3 sets	1 set from each of 3 assembly lots

*Test methods reference MIL-STD-883C.

**Samples to be selected from 3 wafer lots (each lot shall be processed with a minimum of 1 week separating it and the other two wafer lots.

***FIT shall be calculated using the Ahhrenius acceleration model and the following assumptions:
Ea = 0.5 eV if no failures; if failures, Ea to be determined based upon failure mechanism.
Ts = 55° C (derating temperature)
confidence level = 60%

*Table 3. Monolithic Plastic Package Assembly Tests**.*
(Continued)

Terms and Definitions

Activation Energy

The excess energy over the ground state which must be acquired by an atomic or molecular system in order for a specific process to occur.

Arrhenius Model (Acceleration Factor)

The Arrhenius Model defines a relationship between the failure rate and time that is commonly used in correlating accelerated life environmental testing to useful lifetime. The equation is used to calculate failure rates based on lower junction temperatures and normal operating environmental conditions.

The acceleration factor is the reaction rate of a process at one temperature compared with the reaction rate of the same process at another temperature. The acceleration factor equation determines the multiplication factor of time that the change in temperature caused on the reaction process.

$$AF = e\,[\,E_a/K\,(1/T_1 - 1/T_2)\,]$$

Where:

AF = Acceleration Factor

e = natural logarithm base of 2.71828

E = the activation energy for semiconductor material

K = Boltzmann's Constant (8.626×10^{-5} eV / Kelvin)

T_1 = Lower temperature in Degrees Kelvin

T_2 = Higher temperature in Degrees Kelvin

Example: The AF for a temperature change from 85° C to 125° C is 25.9 with an assumed activation energy (E_a) of 1.0 eV. This factor is the time multiplication factor: 1 hour at 125° C is equivalent to 25.9 hours (over 1 day) at 85° C.

Bias

The electrical connection to the device pins that allows specified signals, loading, and power supply voltage to be applied. Often referred to as "electrical bias."

Biased Humidity

An environmental test where the subject device is exposed to high humidity and temperature conditions (85% relative humidity and 85° C) while having the device under an electrical bias. This procedure is designed to measure the device's susceptibility to electrolysis or electrolytic corrosion. The acceleration factor for a humidity change from 50% to 85% has been standardized as approximately 10. In analyzing bias humidity and temperature results, the acceleration factors of humidity and temperature are estimated separately.

Burn-In

A thermal and electrical stress test designed to eliminate early failures. The early device failures (infant mortality) are detected and removed, thus enhancing reliability.

Environmental Tests

Several tests that determine the long-term stability and reliability of products. The product is exposed to various conditions and extremes of temperature, humidity, pressure or mechanical stress that stimulates potential faults to appear, and accelerate detection of device failures.

Failure in Time (FIT)

A standard reliability unit that measures the device failure rate as a function of device hours. One FIT is equal to one device failure per billion device hours of operation (1 FIT = 0.0001% failures / 1000 hours).

Infant Mortality

Initial failures of devices that occur in early life operation. This is the region of the device failure rate curve where the device failure rate decreases with time. Product reliability is enhanced when environmental screening eliminates these early failures region.

Terms and Definitions (continued)

Pressure Cooker

A test that subjects the device to an atmosphere of high temperature moisture under a pressure of approximately two atmospheres. This test exposes susceptibility to galvanic corrosion due to chemical instability of the encapsulating materials.

Qualification

The test procedures as defined by the Quality Assurance Department that a product must survive before being considered a reliable manufacturing product.

*Quality**

The extent to which a product successfully serves the purpose of the user, during usage, is called "fitness for use." This concept of fitness for use is popularly called quality. Several parameters can be used to characterize product quality. Quality of design is a technical measure of the level or degree of excellence of the product to meet it's intended needs of the user. Three activities that compose the quality of design are; Quality of market research, Quality of concept, and Quality of specification. Quality of conformance is the extent to which the product conforms to the design, and can be measured by testing to the product specification. Conformance also is termed Quality of manufacturing or Quality of production. The quality of products over time is characterized by the time-oriented factors such as; availability, reliability, and maintainability.

Quality Assurance (QA)

The activity of providing, to all concerned, the evidence needed to establish confidence and assurance that all the activities which affect product quality are being performed adequately.

Reliability

Quality of products over time can be stated by the products ability to perform without failure. The classic definition is "the probability of a product performing without failure a specified function under given conditions for a specified period of time."

Reliability Growth

The continuing efforts to reduce failure rates result in continued improvements (or growth) in reliability. This takes place in the design and manufacturing phases, and when additional product improvements are needed as determined from field performance data.

Sampling

Inspection method to determine lot quality by careful examination of a small number of devices from the lot. A sampling plan is used to set the sample size, based on the desired quality level.

Screening

The process of subjecting all products to non-destructive stresses to accelerate and identify early failures.

Stress

An extreme environmental, electrical or physical condition applied to a device to evaluate the device performance or to accelerate reaction rates.

Temperature Cycling

A test that determines the thermal expansion compatibility of materials used in device packaging. The test exposes the device to temperature extremes, typically a low temperature of -65° C. to a high temperature of +150° C. The device is under no electrical bias.

Thermal Shock

This is a temperature cycling test in which the temperature transitions are very rapid, less than 10 seconds. The device is immersed in suitable liquid baths, each having extreme high and low temperatures to expose failures such as device cracking, and package leaking.

*QUALITY CONTROL HANDBOOK, Third Edition McGraw Hill 1974, JURAN, Joseph M., Frank M. Gryna Jr., and R.S. Bingham Jr.

SECTION 3

IMAGING PRODUCTS

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eliminary Information

s document contains information on a new product. The parametric information, ough not fully characterized, is the result of testing initial devices.

Bt208

18 MSPS
Monolithic CMOS
8-bit Flash
Video A/D Converter

stinguishing Features

- o Video Amplifier Required
- 1/4 LSB Typical DL Error
- 1/2 LSB Typical IL Error
- xternal Zero and Clamp Control
- verflow Output
- n-Chip Reference
- utput Enable Control
- TL Compatible
- 5 V CMOS Monolithic Construction
- 4-pin 0.3" DIP or 28-pin PLCC Package
- ypical Power Dissipation: 500 mW

Applications

- Image Processing
- Image Capture
- Desktop Publishing
- Graphic Art Systems

Related Products

- Bt251, Bt253
- Bt261

Product Description

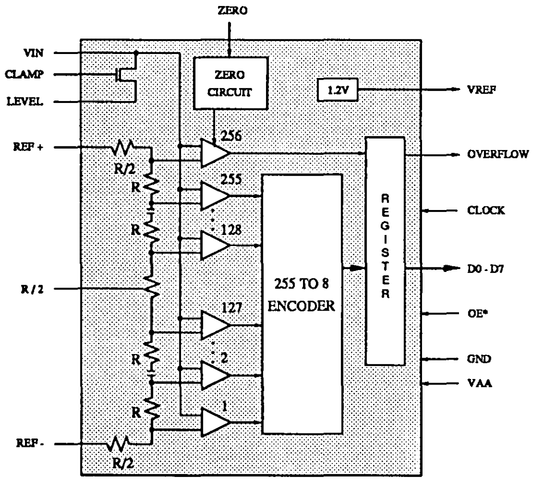
The Bt208 is an 8-bit flash A/D converter designed specifically for video digitizing applications. A flash converter topology is utilized which has 256 high-speed comparators in parallel to digitize the analog input signal.

Flexible input ranges enable NTSC and CCIR video signals to be digitized without requiring a video amplifier.

The TTL-compatible output data and OVERFLOW are registered synchronously with the clock signal. OE* three-states the D0-D7 outputs asynchronously to CLOCK.

The ZERO input is used to zero the comparators, while CLAMP performs DC restoration of the video signal (by forcing the VIN input to the voltage on the LEVEL pin) if AC-coupled to the video signal.

nctional Block Diagram



oktree Corporation
0 Barnes Canyon Rd.
Diego, CA 92121
) 452-7580 • (800) VIDEO IC
: 383 596 • FAX: (619) 452-1249
8001 Rev. J

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt208 contains 256 high-speed comparators, a 255-to-8 encoder, output register, and a resistor divider network. Two hundred fifty-five of the comparators are used to digitize the analog signal; the additional comparator is used to generate the OVERFLOW bit.

General Operation

The Bt208 converts an analog signal in the range of REF– ≤ Vin ≤ REF+, generating a binary number from \$00 to \$FF, and an OVERFLOW output (see Table 1).

The values of REF+ and REF– are flexible to enable various video signals to be digitized without requiring a video amplifier. Refer to the Recommended Operating Conditions and Application Information sections for suggested configurations.

Figure 1 shows the input/output timing of the Bt208. The sample is taken following the falling edge of CLOCK. While CLOCK is low, the 255 to 8 encoding is performed. The binary data and OVERFLOW are registered and output onto the D0–D7 and OVERFLOW pins on the next rising edge of CLOCK.

Comparator Zeroing

The ZERO input is used to periodically zero the comparators. The comparators have an initial threshold mismatch due to manufacturing tolerances. Zeroing charges capacitors in the comparators that offset this threshold mismatch. Due to capacitor discharging, they must be periodically zeroed.

While ZERO is a logical one, the comparators are zeroed. During ZERO cycles, D0–D7 and OVERFLOW are not updated. They retain the data loaded before the ZERO cycle.

Input Signal Clamping

CLAMP and LEVEL are used only in applications where the video signal is AC-coupled to VIN. While CLAMP is a logical one, the VIN input is forced to the voltage level of the LEVEL pin to DC-restore the video signal.

In applications where the video signal is DC-coupled to VIN, the LEVEL pin should float, be connected to VIN, or (only on the 28-pin PLCC package) CLAMP should always be a logical zero.

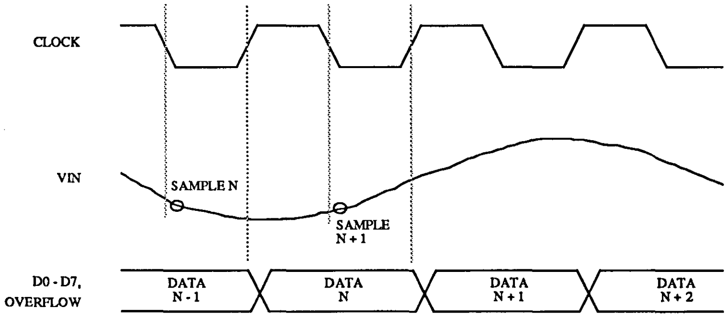
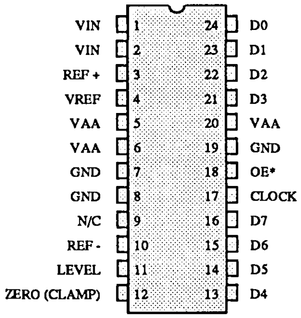


Figure 1. Input/Output Timing.

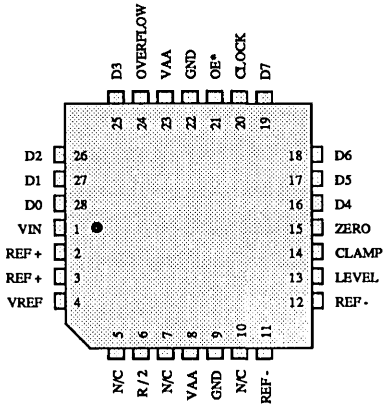
Pin Descriptions

Pin Name	Description
D0–D7	Data outputs (TTL compatible). D0 is the least significant data bit. These outputs are latched and output following the rising edge of CLOCK. Coding is binary. For optimum performance, D0–D7 should have minimal loading. If driving a large capacitive load, an external buffer is recommended.
OE*	Output enable control input (TTL compatible). Negating OE* three-states D0–D7 asynchronously to CLOCK. The OVERFLOW output is not affected by the state of OE*.
OVERFLOW	Overflow output (TTL compatible). OVERFLOW is latched and output following the rising edge of CLOCK. OE* does not affect the OVERFLOW output signal. OVERFLOW is not available on the DIP package.
CLOCK	Clock input (TTL compatible). It is recommended that this pin be driven by a dedicated TTL buffer to minimize sampling jitter.
REF+	Top of ladder voltage reference (voltage input). REF+ sets the VIN voltage level that generates $FF on the D0–D7 outputs. All REF+ pins must be connected together as close to the device as possible. A decoupling capacitor is NOT recommended on REF+.
REF-	Bottom of ladder voltage reference (voltage input). Typically, this input is connected to GND. REF– sets the VIN voltage level that generates $00 on the D0–D7 outputs. All REF– pins must be connected together as close to the device as possible.
R/2	Mid-tap of reference ladder (voltage output). R/2 is not available on the DIP package. If not used, this pin should remain floating. If used, it should be buffered by a voltage follower. A decoupling capacitor is NOT recommended on R/2.
VIN	Analog signal inputs (voltage input). All VIN pins must be connected together as close to the device as possible.
ZERO/CLAMP	Zeroing control input (TTL compatible). While ZERO is a logical one, the comparators are zeroed. ZERO is latched on the rising edge of CLOCK. Note that on the 24-pin DIP package, ZERO and CLAMP share the same pin; hence, zeroing and clamping occur simultaneously. Clamp control input (TTL compatible). While CLAMP is a logical one, the VIN inputs are forced to the voltage level on the LEVEL pin to perform DC restoration of the video signal. CLAMP is asynchronous to clock. Note that on the 24-pin DIP package, ZERO and CLAMP share the same pin; hence, ZERO and CLAMP are asserted simultaneously.
LEVEL	Level control input (voltage input). This input is used to specify what voltage level is to be used for clamping while CLAMP is a logical one. It is typically connected to GND in applications where the video signal is AC-coupled to VIN. In applications where the video signal is DC-coupled to VIN, the LEVEL pin should float or be connected to VIN.
VREF	Voltage reference output pin. This pin provides a 1.2 V (typical) output. A decoupling capacitor is NOT recommended on VREF.
VAA	+5 V power. All VAA pins must be connected together as close to the device as possible. A 0.1 µF ceramic capacitor should be connected between each group of VAA pins and GND, as close to the device as possible.
GND	Ground. All GND pins must be connected together as close to the device as possible.

Pin Descriptions (continued)


VIN 1
VIN 2
REF+ 3
VREF 4
VAA 5
VAA 6
GND 7
GND 8
N/C 9
REF- 10
LEVEL 11
ZERO (CLAMP) 12
24 D0
23 D1
22 D2
21 D3
20 VAA
19 GND
18 OE*
17 CLOCK
16 D7
15 D6
14 D5
13 D4

24-pin 0.3" DIP Package


D3 25
OVERFLOW 24
VAA 23
GND 22
OE* 21
CLOCK 20
D7 19
D2 26
D1 27
D0 28
VIN 1
REF+ 2
REF+ 3
VREF 4
18 D6
17 D5
16 D4
15 ZERO
14 CLAMP
13 LEVEL
12 REF-
5 N/C
6 R/2
7 N/C
8 VAA
9 GND
10 N/C
11 REF-

28-pin Plastic J-Lead (PLCC) Package

Note: N/C pins are reserved and must remain floating.

Vin* (v)	Overflow	D0 - D7	OE*
> 0.998	1	$FF	0
0.996	0	$FF	0
0.992	0	$FE	0
:	:	:	:
0.500	0	$81	0
0.496	0	$80	0
0.492	0	$7F	0
:	:	:	:
0.004	0	$01	0
< 0.002	0	$00	0
		3-state	1

*with REF+ = 1.000 V and REF– = 0.000 V. Ideal center values. 1 LSB = 3.9063 mV.

Table 1. Output Coding.

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS Digitizer layout examples found in the *Bt208, Bt251, or Bt253 Evaluation Module Operation and Measurements,* application notes (AN-13, 14, and 15, respectively). These application notes can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt208 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

Ground Planes

The ground plane area should encompass all Bt208 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt208, the analog input traces, any input amplifiers, and all the digital signal traces leading up to the Bt208.

Power Planes

The Bt208 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 2. This bead should be located within 3 inches of the Bt208.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt208 power pins, any voltage reference circuitry., and any input amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Best performance is obtained using a dedicated linear regulator to provide power to the Bt208.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

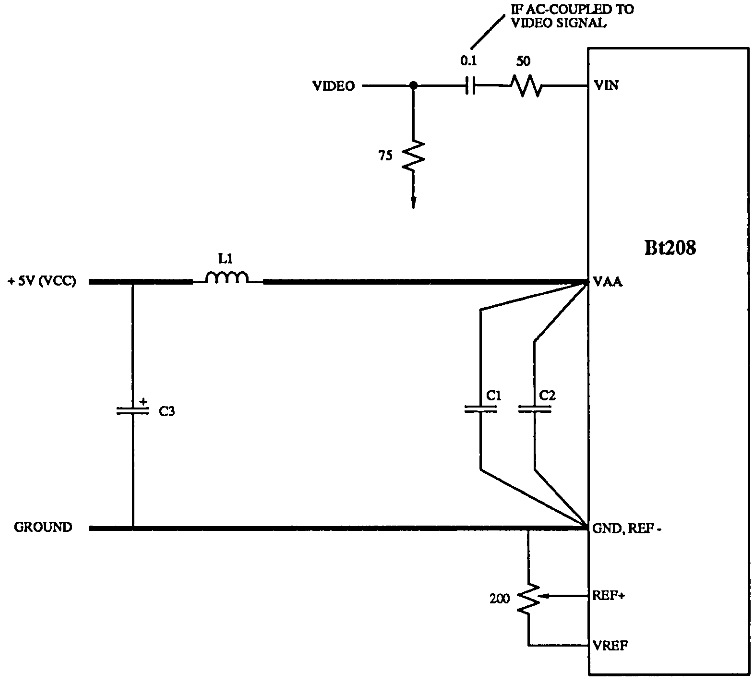
For the best performance, a 0.1 µF ceramic capacitor should be used to decouple each of the two power pin groups to GND. These capacitors should be placed as close as possible to the device.

Signal Interconnect

The digital signals of the Bt208 should be isolated as much as possible from the analog inputs and other analog circuitry. Also, these digital signals should not overlay the analog power plane.

Any termination resistors for the digital signals should be connected to the regular PCB power and ground planes.

PC Board Layout Considerations (continued)


IF AC-COUPLED TO VIDEO SIGNAL
0.1
50
VIDEO
VIN
75
Bt208
L1
+5V (VCC)
VAA
C1
C2
+
C3
GROUND
GND, REF-
200
REF+
VREF

Location	Description	Vendor Part Number
C1, C2	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C3	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt208.

Figure 2. Typical Connection Diagram and Parts List (Internal Reference).

Application Information

Using the Internal Reference

The Bt208 has a 1.2 V on-chip reference available (VREF). VREF may be divided down and used to drive the REF+ input as shown in Figure 2. The 200 Ω potentiometer serves three purposes: to allow adjustment for different video signal levels, to allow for video level tolerances, and to adjust for tolerance of the internal reference.

Note that VREF should supply at least 5 mA of current to maintain voltage stability over temperature. Thus, VREF should drive a resistive load between 90 and 240 Ω.

Using An External Reference

Figure 3 illustrates using a 1.2 V LM385 to generate a 0 V–1.2 V reference for applications requiring a better reference tempco than the internal reference can supply. Supply decoupling of the op-amp is not shown. Any standard op-amp may be used that is capable of operating from a single +5 V supply.

As REF+ should be driven by a high AC impedance source, a 100 Ω resistor should be placed between REF+ and the output of the op-amp, as shown in Figure 3. REF– may be driven in a similar manner if a value other than GND is desired.

AC-Coupled vs. DC-Coupled Input

The Bt208 may be either AC- or DC-coupled to the video signal, as shown in Figure 2. The 75 Ω resistor to ground provides the typical 75 Ω AC and DC termination required by video signals. The 50 Ω resistor provides isolation from any clock kickback noise on VIN and prevents it from being coupled onto the video signal. If DC-coupled to the video signal, the 0.1 µF capacitor is not used and CLAMP should be grounded.

Zeroing

Unlike many CMOS A/D converters requiring the comparators to be zeroed every clock cycle, the comparators in the Bt208 are designed to be only periodically zeroed. It is convenient to assert ZERO during each horizontal retrace interval.

Note that, before using the Bt208 after a power-up condition, ZERO must be a logical one for at least 1000 clock cycles (cumulative) to initialize the comparators to the rated linearity. In normal video applications this will be transparent due to the number of horizontal scan lines that will have occurred before using the Bt208.

As long as the recommended zeroing interval is maintained, the Bt208 will meet linearity specifications. The longer the time between zeroing intervals, the more the linearity error increases.

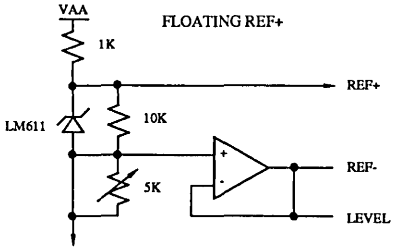


Figure 3. Using an External Reference.

Application Information (continued)

Input Ranges

Table 2 shows some common video signal amplitudes. For signals possibly exceeding 1.2 V, the signal should be attenuated (using a resistor divider network) so as not to exceed the 1.2 V input range.

When digitizing with a full-scale range less than 0.7 V, the Bt208's integral linearity errors are constant in terms of voltage regardless of the value of the reference voltage. Lower reference voltages will therefore produce larger integral linearity errors in terms of LSBs.

For example, with a reference difference of 0.6 V, 0.6 V video signals may be digitized; however, the integral linearity (IL) error will increase to about ± 1.8 LSB; the SNR will be about 40 dB. With a reference difference of 0.5 V, 0.5 V video signals may be digitized with an IL error of about ±2 LSB; the SNR will be about 39 dB.

SNR and Error Rate vs. Clock Timing

Figure 4 illustrates the error rate vs. clock low time, while Figure 5 illustrates the SNR vs. clock high time.

An error is defined as being a sample that is more than 8 LSBs (out of 255) from the expected value, where the previous and following samples are less than (or equal to) 8 LSBs from the expected value.

Output Noise

Although the Bt208 does exhibit some output noise for a DC input, the output noise remains relatively constant for any input bandwidth. Competitive A/D converters have no noise for a DC input; however, the output noise increases greatly as the input bandwidth and clock rate increase.

The output noise of the Bt208 may be reduced by adjusting the duty cycle of the clock—this is especially true above 10 MHz clock operation. Note that uncorrelated noise less than 1% peak-to-peak will be perceived with the same quality as that of a consumer 1/2 inch VCR.

PC Board Sockets

If a socket is required, a low-profile socket is recommended, such as AMP part no. 641746–2 for the PLCC package.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid ADC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Video Standard	Nominal Amplitude	Worst Case Amplitudes
RS-170 w/o sync	1.0 V BLACK - WHITE	0.9–1.1 V
RS-170 w/sync	1.4 V SYNC - WHITE	1.2–1.6 V
RS-170A w/sync	1.2 V SYNC - WHITE	1.0–1.4 V
RS-343A w/o sync	0.7 V BLACK - WHITE	0.6–0.85 V

Table 2. Video Signal Tolerances.

Application Information (continued)

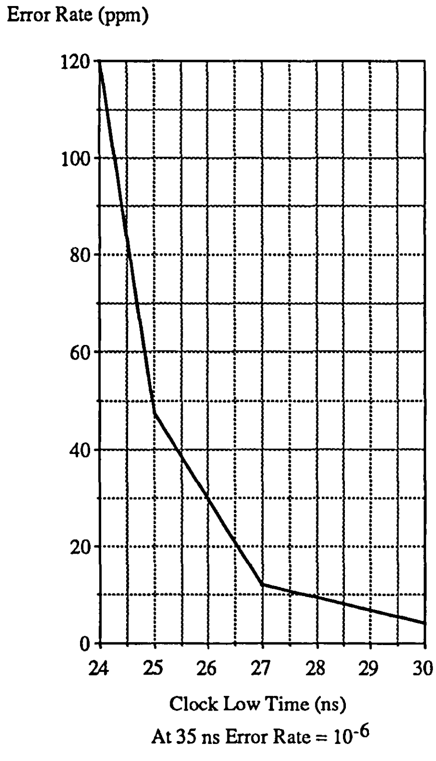


Figure 4. Error Rate vs. Clock Low Time.

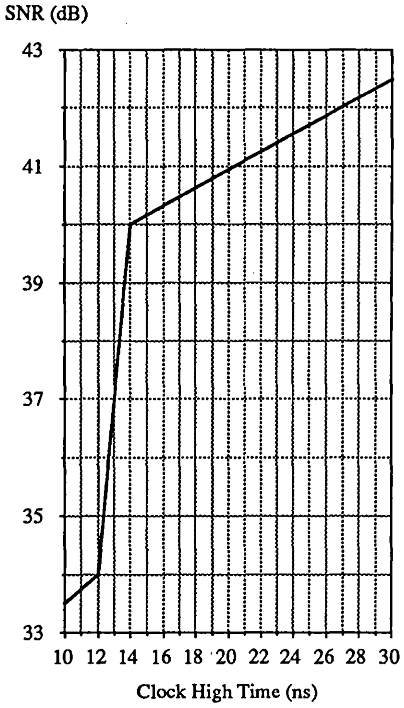


Figure 5. SNR vs. Clock High Time.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.5	5.00	5.5	Volts
Voltage References					
Top	REF+	0.7	1	2.0	Volts
Bottom	REF-	0	0	1.3	Volts
Difference (Top–Bottom)		0.7	1	1.2	Volts
Input Amplitude Range		0.7	1	1.2	Volts
Analog Input Range			REF– to REF+		Volts
LEVEL Input Voltage		GND–0.5	REF–	REF+	Volts
Time between Zeroing Intervals			60	150	µS
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Input Voltage		GND–0.5		VAA + 0.5	Volts
R/2 Output Current				25	µA
Ambient Operating Temperature	TA	–55			
Storage Temperature	TS	–65		+125	°C
Junction Temperature	TJ			+150	°C
				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error (note 1)	IL		±0.5	±1	LSB
Differential Linearity Error	DL		±0.25	±1	LSB
Output Noise (note 2)			±1		LSB
Offset Error					
Top			tbd		mV
Bottom			tbd		mV
Tempco			tbd		mV / °C
Coding					
No Missing Codes			guaranteed		Binary
VIN Analog Inputs (note 3)					
CLAMP = 0					
Input Impedance	RIN	10			M=ohms
Input Current	IB			1	µA
Input Capacitance	CAIN		15		pF
CLAMP = 1					
Input Impedance	RIN		50		Ohms
REF+ Reference Input					
Input Current	IREF+		1		mA
Input Impedance	RREF+		1		kΩ
Digital Inputs					
Input High Voltage	VIH	2.0			Volts
Input Low Voltage	VIL			0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance	CIN		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Clock Kickback (note 4)			160		pV - sec
Digital Outputs					
Output High Voltage (IOH = -50 μA)	VOH	2.4			Volts
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	Volts
Three-State Current	IOZ			10	μA
Output Capacitance	COUT			10	pF
Internal Voltage Reference	VREF	tbd	1.2	tbd	Volts
Regulation (at 6 mA)			5		mV
Output Current	IREF			15	mA
Power Supply Rejection Ratio (not including reference)	PSRR		0.004		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1 V and REF– = GND. REF– ≤ Vin ≤ REF+, LEVEL = float. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note 1: Using best-fit linearity (offset independent). Averaged value evaluated using a closed-loop system.

Note 2: Clock duty cycle adjusted for minimum output noise for a DC input. For a DC input, output noise may increase if clock duty cycle is not adjusted.

Note 3: LEVEL = GND.

Note 4: Measurement of noise coupled onto VIN due to clocking (Rs = 75 Ω). Typically occurs over a 5-ns interval.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate	Fs			18	MHz
Clock Cycle Time	1	55.5			ns
Clock Low Time	2	35*			ns
Clock High Time	3	20**			ns
Data Output Delay	4			25	ns
OE* Asserted to D0–D7 Valid	5			25	ns
OE* Negated to D0–D7 3-Stated	6			25	ns
ZERO Setup Time	7	0			ns
ZERO Hold Time	8	20			ns
ZERO, CLAMP High Time (note 1)		1			Clock
Aperture Delay	9		10		ns
Aperture Jitter			50		ps
Full Power Input Bandwidth	BW	6			MHz
Transient Response (note 2)				1	Clock
Overload Recovery (note 3)				1	Clock
Zero Recovery Time (note 4)				1	Clock
RMS Signal to Noise Ratio	SNR				
Fin = 4.2 MHz, Fs = 10.7 MHz			43		dB
Fin = 4.2 MHz, Fs = 14.32 MHz			42		dB
Fin = 2.75 MHz, Fs = 6.75 MHz			44		dB
Fin = 5.75 MHz, Fs = 13.5 MHz			41		dB
Fin = 4.2 MHz, Fs = 17.72 MHz			41		dB
Differential Gain Error (note 5)	DG		2		%
Differential Phase Error (note 5)	DP		1		Degree
Supply Current (note 6) (Excluding IREF+)	IAA		100	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1 V and REF– = GND. REF– ≤ Vin ≤ REF+, LEVEL = float. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for digital inputs and outputs. D0–D7 and OVERFLOW output load ≤ 75 pF. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

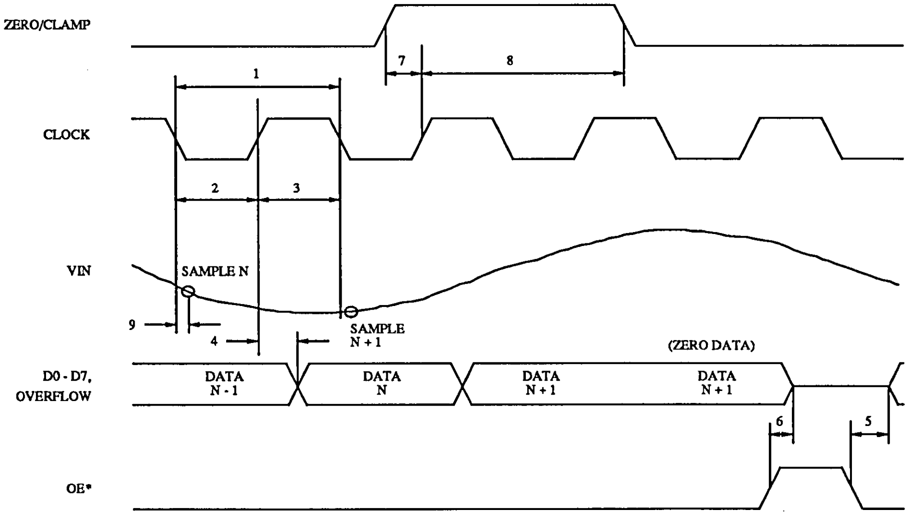
Note 1: Number of clock cycles ZERO is a logical one does not affect linearity. For best performance, ZERO should be a logical one for an odd number of clock cycles.
Note 2: For full-scale step input, full accuracy attained in specified time.
Note 3: Time to recover to full accuracy after a > 1.2 V input signal.
Note 4: Time to recover to full accuracy following a zero cycle.
Note 5: 4x NTSC subcarrier, unlocked.
Note 6: IAA (typ) at VAA = 5.0 V, Fin = 4.2 MHz, Fs = 14.32 MHz.
IAA (max) at VAA = 5.5 V, Fin = 6 MHz, Fs = 18 MHz.

*For 10^{-6} typical error rate (see Figure 4).
**For typical SNR of 41 dB (see Figure 5).

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt208KP	24-pin 0.3" Plastic DIP	0° to +70° C
Bt208KPJ	28-pin Plastic J-Lead	0° to +70° C
Bt208KP EVM	Bt208 Evaluation Board (includes Bt208KP)	

Timing Waveforms


ZERO/CLAMP
CLOCK
VIN
D0 - D7, OVERFLOW
OE*
1
2
3
4
5
6
7
8
9
SAMPLE N
SAMPLE N + 1
(ZERO DATA)
DATA N - 1
DATA N
DATA N + 1
DATA N + 1

Input/Output Timing.

Revision History

Revision	*Change from Previous Revision*
H	Connection diagrams simplified, R/2 tap on PLCC package brought out.
I	Actual numbers for AC/DC parameters replace some "tbds."
J	Revised Application Information.

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt251

18 MSPS
Monolithic CMOS
Single Channel
8-bit Image Digitizer

Distinguishing Features

- 4 Software Selectable Analog Inputs
- DC- or AC-Coupled Video Inputs
- Optional MPU Adjustment of Gain and Offset
- Composite Sync Detection
- 8-bit Flash A/D Converter
- R/2 Reference Ladder Tap
- 256 x 8 Lookup Table
- Genlock Externally Implemented
- Standard MPU Interface
- TTL Compatible
- +5 V CMOS Monolithic Construction
- 44-pin PLCC Package
- Typical Power Dissipation: 750 mW

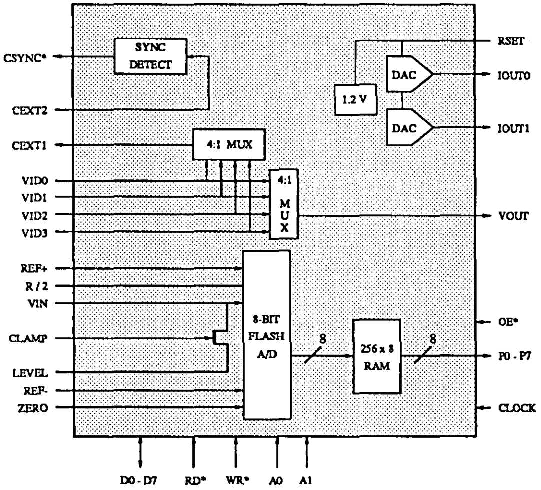
Applications

- Image Processing
- Image Capture
- Desktop Publishing
- Graphic Art Systems

Related Products

- Bt253
- Bt261

Functional Block Diagram



Product Description

The Bt251 Image Digitizer is designed to digitize standard video signals (NTSC or CCIR). The architecture of the Bt251 enables the addition of external circuitry for filtering, gain, etc., along the signal path. A standard MPU interface is provided for accessing various control functions.

Four analog inputs are supported, selectable under MPU control. The MPU may select from which input to detect sync information for external genlocking independently of the video input being digitized. A TTL-compatible composite sync signal is output to interface to the genlock circuitry.

The output of the 8-bit A/D converter addresses a 256 x 8 lookup table RAM, enabling real-time image manipulation prior to data storage, including thresholding, contrast enhancement, reversing video, implementing a nonlinear A/D, etc. The digitized data outputs may be three-stated asynchronously to clock via the OE* control.

Optional MPU-controlled adjustment of gain and offset is supported by the ability to program the levels of the REF+ and REF– inputs to the A/D. Zeroing and clamping signals are available to control the A/D timing for application–specific designs. The clamping level is externally set via the LEVEL pin.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L251001 Rev. H

Brooktree®

Circuit Description

MPU Interface

As shown in the functional block diagram, the Bt251 supports a standard MPU interface (D0–D7, RD*, WR*, A0, and A1). MPU operations are asynchronous to the clock.

An internal 8-bit address register, in conjunction with A0 and A1, is used to specify which control register or RAM location the MPU is accessing, as shown in Table 1. All registers and RAM locations may be written to or read by the MPU at any time; however, while digitizing a video signal, the MPU should not access the RAM as this will corrupt the digitized data.

When the MPU accesses the RAM, the address register increments after each MPU access (read or write cycle). After writing to RAM location $FF, the address register resets to $00.

When accessing the address register or control registers, the address register does not increment after an MPU read or write cycle. Data written to reserved locations is ignored; data read from reserved locations returns invalid data. ADDR0 corresponds to D0 and is the least significant bit.

Flash A/D Converter

The Bt251 uses an 8-bit flash A/D converter to digitize the video signal. The A/D digitizes analog signals in the range of REF- ≤ Vin ≤ REF+. The output will be a binary number from $00 (Vin ≤ REF-) to $FF (Vin ≥ REF+).

VIN may be either DC– or AC-coupled to the video signal. If AC-coupled, the CLAMP and LEVEL controls may be used to DC-restore the video signal.

Analog Input Selection

The Bt251 supports four analog input sources, VID0–VID3. The MPU specifies which one is to be digitized via the command register.

The selected video signal is output onto VOUT. VOUT may be connected directly to VIN if no filtering or gain of the video signal is required.

If digitizing only the luminance information of a video signal containing color subcarrier information, a filter should be used to remove the subcarrier information to avoid possible artifacts on the display screen. A low-pass filter, notch filter, or comb filter may be used to remove the chroma information.

Note that sync information (if present) will still be present on VOUT.

The multiplexers are not a break-before-make design. Therefore, during the multiplexer switching time it is possible for the input video signals to be momentarily connected together through the equivalent of 200 Ω.

The 75 Ω resistors to ground (Figure 1) provide the typical 75 Ω termination required by video signals.

A1	A0	ADDR7 - ADDR0	Addressed by MPU
0	0	xxxx xxxx	address register
0	1	0000 0000	RAM location $00
0	1	0000 0001	RAM location $01
:	:	:	:
0	1	1111 1111	RAM location $FF
1	0	xxxx xx00	command register
1	0	xxxx xx01	IOUT0 data register
1	0	xxxx xx10	IOUT1 data register
1	0	xxxx xx11	reserved
1	1	xxxx xxxx	reserved

Table 1. Address Register Operation.

Circuit Description (continued)

A/D Reference Generation

As shown in Figure 1, the Bt251 may be configured to have either fixed or MPU-adjustable references for the A/D converter.

If jumpers J2 and J4 are selected, REF+ is connected to a 0.7 V to 1.2 V reference (VREF) and REF– is connected to GND. This mode of operation may be used when the only operation is to digitize video signals with an amplitude range of 0.7 V to 1.2 V with no adjustment of gain or offset.

If jumpers J1 and J3 are selected, gain and offset of the video signal may be done via the MPU-adjustable outputs IOUT0 and IOUT1. This mode of operation allows top and bottom reference adjustments so that different video signals may be digitized or operations such as contrast enhancement or level adjustments may be implemented. The TLC272 dual CMOS op-amps can be used for single +5 V operation.

IOUT0 and IOUT1 are current outputs (0 to 2.5 mA) generated by two 6-bit D/A converters. A 511 Ω RSET resistor generates a 2.35 mA full-scale output current. The 511 Ω resistors to GND generate a 0 V to 1.2 V level that drive the REF+ and REF– inputs through voltage followers. The top and bottom references may thus be adjusted with 19 mV resolution.

It is not recommended that the DAC outputs drive the top of the reference ladder directly as the reference ladder resistance changes slightly with temperature.

The DACs are current sources; they do not sink current. Thus, if MPU adjustment of REF– is desired, the DAC output must drive REF– using a voltage follower.

A/D Zeroing

The ZERO input is used to zero the comparators and must be asserted sometime during each horizontal blanking interval. While ZERO is a logical one, the comparators are zeroed. During ZERO cycles, the P0–P7 outputs are not updated. They retain the data loaded before the ZERO cycle.

A/D Input Clamping

If VIN is AC-coupled to the video signal, the CLAMP and LEVEL controls may be used to DC-restore the video signal. While CLAMP is a logical one, the video signal is clamped to the voltage level present on the LEVEL pin. CLAMP should be asserted during static intervals and at least 500 ns before, or after, a video transition.

When DC-restoring RGB or luminance video signals, LEVEL is typically connected to the same potential as REF.

When DC-restoring color difference video signals, LEVEL is typically at the midpoint between REF+ and REF–. The Bt251 provides an R/2 reference ladder tap that may be used to generate the proper DC voltage (jumper J6 in Figure 1). The R/2 tap should drive a high-impedance load while capturing an image to maintain optimum linearity of the A/D converter.

If VIN is DC-coupled to the video signal, LEVEL should float or CLAMP should always be a logical zero.

VIN Input Considerations

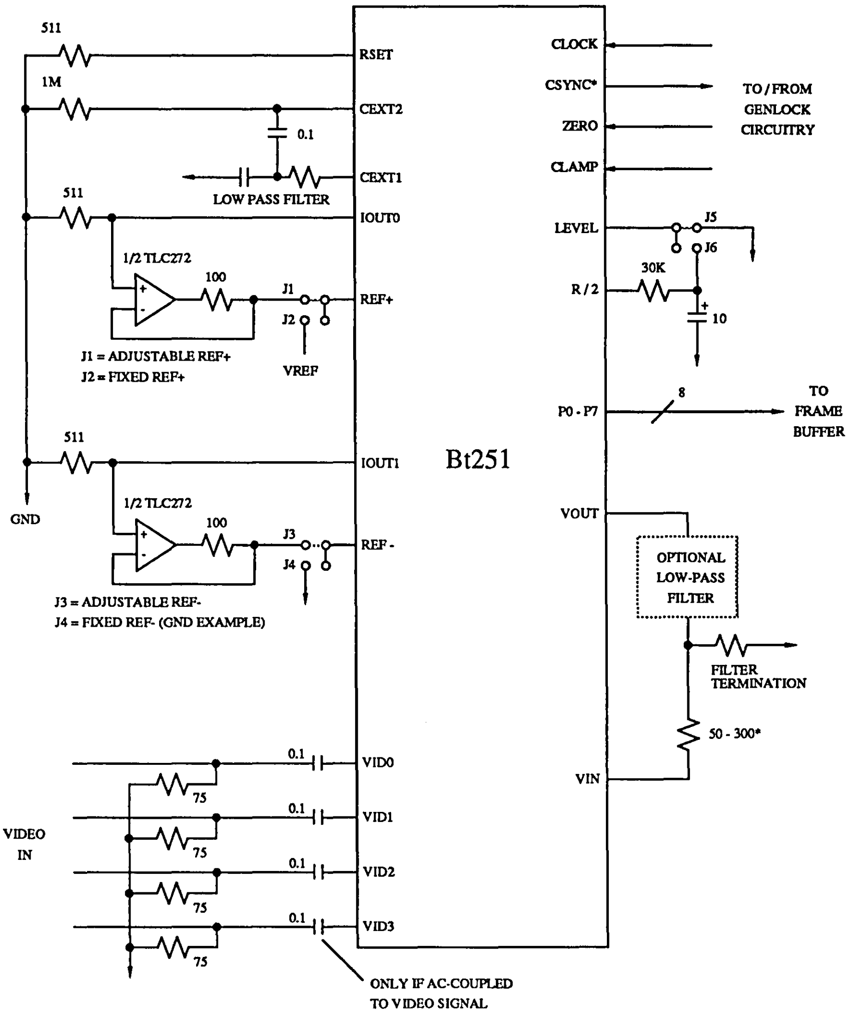
The 50–300 ohm resistor shown in Figure 1 after the low-pass filter is only required if an active low-pass filter is used. It provides isolation from any clock kickback noise on VIN, preventing it from being coupled onto the video signal. The exact value of the resistor should be adjusted for minimum clock kickback noise on VIN. If no filter or a passive low-pass filter is used, the resistor is not required, as the resistance of the multiplexer serves to reduce the clock kickback noise.

The 0.1 µF capacitor shown in Figure 1 after the low-pass filter is only required if an active low-pass filter is used and DC restoration must be performed. If no filter or a passive low-pass filter is used, the capacitor is not required, as the DC restoration can still be implemented using the 0.1 µF capacitors on the VIDx inputs.

Multiplexer Considerations

Maintaining DC levels within the rated compliance range is necessary to obtain the best linearity and crosstalk performance. Clamping through the MUX accomplishes this on the selected channel. Adding clamp diodes on all video inputs to a positive bias will optimize multiplexer fidelity.

Circuit Description (continued)


511
RSET
1M
CEXT2
0.1
CEXT1
LOW PASS FILTER
511
IOUT0
1/2 TLC272
100
J1
REF+
J2
VREF
J1 = ADJUSTABLE REF+
J2 = FIXED REF+
511
IOUT1
GND
1/2 TLC272
100
J3
REF -
J4
J3 = ADJUSTABLE REF-
J4 = FIXED REF- (GND EXAMPLE)
Bt251
CLOCK
CSYNC*
ZERO
CLAMP
TO / FROM GENLOCK CIRCUITRY
LEVEL
J5
J6
30K
R / 2
10
P0 - P7
8
TO FRAME BUFFER
VOUT
OPTIONAL LOW-PASS FILTER
FILTER TERMINATION
50 - 300*
VIN
VIDEO IN
0.1
VID0
75
0.1
VID1
75
0.1
VID2
75
0.1
VID3
75
ONLY IF AC-COUPLED TO VIDEO SIGNAL

J5 = DC RESTORE TO GND
J6 = COLOR DIFFERENCE DC RESTORE

* NEEDED ONLY IF ACTIVE FILTER IS USED. ADJUST FOR MINIMUM CLOCK KICKBACK.

Figure 1. Typical Bt251 External Circuitry.

Circuit Description (continued)

Lookup Table RAM

A 256 x 8 lookup table RAM is provided on-chip to implement simple imaging operations such as gamma manipulation, simple contrast enhancement, inverting of data, or a nonlinear transfer function of the A/D converter. Data from the A/D is used to address the RAM; the addressed data is output onto P0–P7.

The RAM may be effectively bypassed by loading each location with its corresponding address. As the lookup table RAM is not dual-ported, MPU accesses have priority over digitized data passing through the RAM. During MPU accesses to the RAM, P0–P7 are undefined.

Sync Detect Circuitry

The Bt251 performs composite sync detection from the analog input specified by the command register. Thus, sync information may be recovered from one analog input while another input is being digitized. The composite sync signal (CSYNC*) contains any serration and equalization pulses the video signal may contain. Note that CSYNC* is output asynchronously to the clock and there are no pipeline delays (the output delay from VIN to CSYNC* is approximately 25 ns).

The MPU specifies from which analog input to detect sync (negative sync polarity). The selected video signal is output on CEXT1. A 0.1 µF capacitor between CEXT1 and CEXT2 AC-couples the video signal to the sync detection circuit. The MPU selects one of four levels of sync threshold by selecting how many millivolts above the sync tip to use for sync detection. If the sync tip on CEXT2 is below the selected threshold, CSYNC* will be a logical zero. A low-pass filter removes subcarrier burst ringing and extraneous vertical interval signals from false sync detection.

If it is desired to low-pass filter the sync signal prior to sync detection, the low-pass filter should be inserted between CEXT1 and the 0.1 µF capacitor (see Figure 1).

If the sync detection circuit is not used, CEXT2 should be connected to GND or VAA (CEXT1 may float), or an unused (grounded) video input selected for the sync detector.

External Sync Detection

CEXT1 may be connected to an external sync detector circuit. In this case, CEXT2 should be connected directly to GND or VAA and the CSYNC* output left floating.

The sync analog multiplexer may still be used to select from which video source to detect sync information. As the multiplexer switches analog video signals, the selected video source will be output onto CEXT1.

Internal Registers

Command Register

The command register may be written to or read by the MPU at any time and is not initialized. D0 is the least significant bit.

D7, D6	Digitize select (00) VID0 (01) VID1 (10) VID2 (11) VID3	These bits specify which analog input is to be digitized. The selected signal is output onto VOUT.
D5, D4	Sync detect select (00) VID0 (01) VID1 (10) VID2 (11) VID3	These bits specify from which analog input sync information is to be detected. The selected signal is output onto CEXT1.
D3, D2	Sync detect level select (00) 50 mV (01) 75 mV (10) 100 mV (11) 125 mV	These bits specify how much above the sync tip to slice CEXT2 for sync detection.
D1, D0	reserved (logical zero)	The MPU must write a logical zero to these bits to ensure proper operation.

IOUT Data Registers

These two 8-bit registers specify the output current on the IOUT0 and IOUT1 outputs, from 0 mA ($00) to full scale ($FC). The six MSBs of data are used to drive the DACs. D0 and D1 (the two LSBs) must be programmed to be a logical zero.

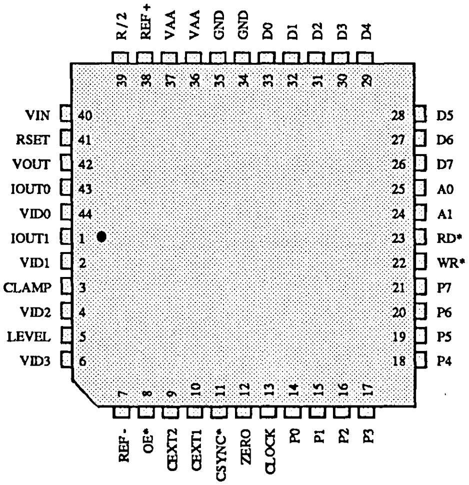
These registers may be written to or read by the MPU at any time and are not initialized. D0 is the least significant bit.

Pin Descriptions

Pin Name	Description
General Reference Functions	
RSET	Full-scale adjust control. An external 511 Ω resistor must be connected between this pin and GND. It is used to provide reference information to the internal D/A converters. See Figure 1.
IOUT0, IOUT1	Current outputs. The amount of output current is specified by the IOUT data registers. External 511 Ω resistors are typically connected between each pin and GND. See Figure 1. The relationship between full-scale IOUT and RSET is: IOUT (mA) = 1,200 / RSET (Ω)
CEXT1, CEXT2	External capacitor pins. A 0.1 µF capacitor must be connected between CEXT1 and CEXT2 to AC-couple the video signal to the sync detect circuitry. A 1M Ω resistor must also be connected between CEXT2 and GND. See Figure 1.
A/D Functions	
REF+	Top of resistor ladder (voltage input). REF+ sets the VIN voltage level that generates $FF from the A/D converter. A decoupling capacitor is NOT recommended on REF+.
REF–	Bottom of resistor ladder (voltage input). REF– sets the VIN voltage level that generates $00 from the A/D converter.
R/2	Reference ladder midpoint tap. If not used, this pin should remain floating. A decoupling capacitor is NOT recommended on R/2. External loading should be < 1 µA to obtain the best linearity.
ZERO	Zeroing control input (TTL compatible). While ZERO is a logical one, the comparators of the A/D are zeroed. ZERO is latched on the rising edge of CLOCK. During zeroing cycles, P0–P7 are not updated; they retain the data loaded before the zeroing cycle.
CLAMP	Clamp control input (TTL compatible). While CLAMP is a logical one, the VIN input is forced to the voltage level on the LEVEL pin to perform DC restoration of the video signal. CLAMP is asynchronous to clock. In applications where VIN is DC-coupled to the video signal, LEVEL should float or be connected to VIN, or CLAMP should always be a logical zero.
LEVEL	Level control input (voltage input). This input is used to specify what voltage level is to be for DC restoration while CLAMP is a logical one. In applications where VIN is DC-coupled to the video signal, LEVEL should float or be connected to VIN, or CLAMP should be a logical zero.
VIN	A/D converter input. The analog signal to be digitized should be connected to this analog input pin. It may be either DC- or AC-coupled to the video signal being digitized.
VID0–VID3, VOUT	Analog inputs and analog output. VID0–VID3 are connected to the video signals to be digitized. The signal selected to be digitized is output onto VOUT. Unused inputs should be connected to GND.
Timing Functions	
CLOCK	Clock input (TTL compatible). CLOCK should be driven by a dedicated TTL buffer to minimize sampling jitter.
CSYNC*	Recovered composite sync output (TTL compatible). Sync information is detected on the VID0–VID3 input specified by the command register, converted to TTL levels, and output onto this pin. It is output asynchronously to the clock and there are no pipeline delays.

Pin Descriptions (continued)

Pin Name	Description
Digital Control Functions	
P0–P7	Digitized video data outputs (TTL compatible). Digitized video data is output onto these pins following the rising edge of CLOCK. P0 is the least significant bit. They are three-stated if OE* is a logical one.
OE*	Output enable control input (TTL compatible). A logical one three-states the P0–P7 outputs asynchronously to CLOCK.
RD*	Read control input (TTL compatible). If RD* is a logical zero, data is output onto D0–D7. RD* and WR* should not be asserted simultaneously.
WR*	Write control input (TTL compatible). If WR* is a logical zero, data is written into the device via D0–D7. Data is latched on the rising edge of WR*. RD* and WR* should not be asserted simultaneously.
D0–D7	Bidirectional data bus (TTL compatible). MPU data is transferred into and out of the device over this 8-bit data bus. D0 is the least significant bit.
A0, A1	Address control inputs (TTL compatible). A0 and A1 are used to specify the operation the MPU is performing as indicated in Table 1. They are latched on the falling edge of either RD* or WR*.
Power and Ground	
VAA	+5 V power. All VAA pins must be connected together as close to the device as possible. A 0.1 μF ceramic capacitor should be connected between each group of VAA pins and GND, as close to the device as possible.
GND	Ground. All GND pins must be connected.


R/2 39
REF+ 38
VAA 37
VAA 36
GND 35
GND 34
D0 33
D1 32
D2 31
D3 30
D4 29
VIN 40
RSET 41
VOUT 42
IOUT0 43
VID0 44
IOUT1 1
VID1 2
CLAMP 3
VID2 4
LEVEL 5
VID3 6
D5 28
D6 27
D7 26
A0 25
A1 24
RD* 23
WR* 22
P7 21
P6 20
P5 19
P4 18
REF- 7
OE* 8
CEXT2 9
CEXT1 10
CSYNC* 11
ZERO 12
CLOCK 13
P0 14
P1 15
P2 16
P3 17

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS Digitizer layout examples found in the Bt208, Bt251, or Bt253 Evaluation Module Operation and Measurements, application notes (AN-13, 14, and 15, respectively). These application notes can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt251 power and ground lines by shielding the digital inputs/outputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

Ground Planes

The ground plane area should encompass all Bt251 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt251, the analog input traces, any input amplifiers, and all the digital signal traces leading up to the Bt251.

Power Planes

The Bt251 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 2. This bead should be located within 3 inches of the Bt251.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt251 power pins, any voltage reference circuitry, and any input amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged so that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Best performance is obtained using a dedicated linear regulator to provide power to the Bt251.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

Each group of VAA pins should have a 0.1 µF ceramic bypass capacitor to GND, located as close as possible to the device.

Digital Signal Interconnect

The digital signals of the Bt251 should be isolated as much as possible from the analog signals and other analog circuitry. Also, the digital signals should not overlay the analog power plane.

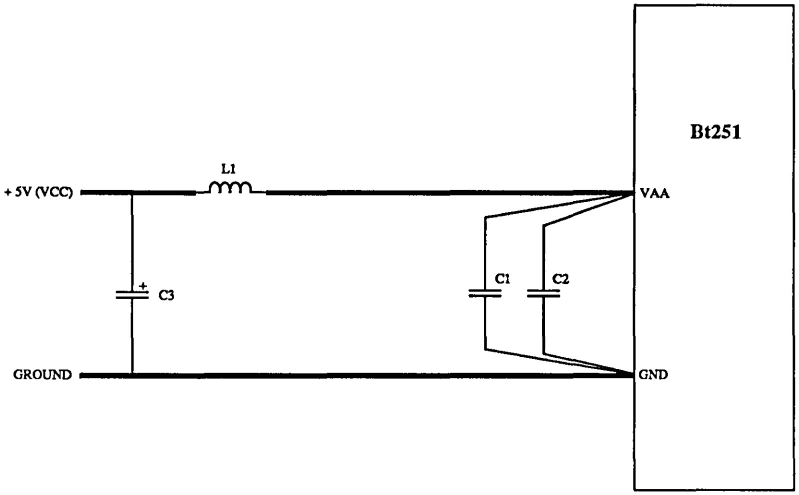
Any termination resistors for the digital signals should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

Long lengths of closely spaced parallel video signals should be avoided to minimize crosstalk. Ideally, there should be a ground line between the video signal traces driving the VIDx inputs.

Also, avoid routing high-speed TTL signals close to the analog signals to minimize noise coupling.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1, C2	0.1 μF ceramic capacitor	Erie RPE112Z5U104M50V
C3	10 μF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt251.

Figure 2. Typical Power Supply Connection Diagram and Parts List.

Application Information

Zeroing

Unlike many CMOS A/D converters requiring the comparators to be zeroed every clock cycle, the comparators in the Bt251 are designed to be only periodically zeroed. It is convenient to assert ZERO during each horizontal retrace interval.

Note that before using the Bt251 after a power-up condition, ZERO must be a logical one for at least 1000 clock cycles (cumulative) to initialize the comparators to the rated linearity. In normal video applications this will be transparent due to the number of horizontal scan lines that will have occurred before using the Bt251.

As long as the recommended zeroing interval is maintained, the Bt251 will meet linearity specifications. The longer the time between zeroing intervals, the more the linearity error increases.

Increasing the Resolution of DACs

With a 511 Ω resistor connected between each DAC output (IOUT0, IOUT1) and GND, the resolution of the ladder adjustment is 19 mV. The resolution of the top of the resistor ladder (REF+) adjustment may be increased by biasing the DAC outputs and using the DAC outputs to adjust the voltage over a smaller range with finer resolution.

Figure 3 shows a circuit that allows adjustment of the REF+ inputs from 0.714 V to 1 V with 4.5 mV resolution. With the DAC data = $00, 0.714 V is output; if the DAC data = $FC, 1 V is output.

As the typical maximum DAC output current is 2.35 mA (RSET = 511 Ω), if a 0.286 V adjustable range is desired, R1 || R2 must equal 121 Ω. The minimum output voltage desired determines the ratio of R1 and R2:

$$V_{min} = VREF * (R2 / (R1 + R2))$$

The bottom of the resistor ladder (REF-) may be adjusted from 0 V to 0.286 V with 4.5 mV resolution by using a 121 Ω resistor to ground rather than a 511 Ω resistor. As long as the minimum range is 0 V, the resistor to ground may be used to adjust the total range, and thus the resolution.

Video Standard	Nominal Amplitude	Worst Case Amplitudes
RS-170 w/o sync	1.0 V BLACK - WHITE	0.9–1.1 V
RS-170 w/sync	1.4 V SYNC - WHITE	1.2–1.6 V
RS-170A w/sync	1.2 V SYNC - WHITE	1.0–1.4 V
RS-343A w/o sync	0.7 V BLACK - WHITE	0.6–0.85 V

Table 2. Video Signal Tolerances.

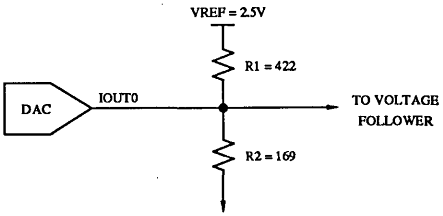


Figure 3. Increasing DAC Output Resolution.

Application Information (continued)

Using an External Reference

Figure 4 illustrates using a 1.2 V LM385 to generate a 0 V to 1.2 V reference for applications requiring a better reference tempco than the internal reference can supply. Supply decoupling of the op-amp is not shown. Any standard op-amp may be used that is capable of operating from a single +5 V supply.

As REF+ should be driven by a high AC impedance source, a 100 Ω resistor should be placed between REF+ and the output of the op-amp, as shown in Figure 4. REF– may be driven in a similar manner if a value other than GND is desired.

Input Ranges

Table 2 shows some common video signal amplitudes. For signals possibly exceeding 1.2 V, the signal should be attenuated (using a resistor divider network) so as not to exceed the 1.2 V input range.

When digitizing with a full-scale range less than 0.7 V, the Bt251's integral linearity errors are constant in terms of voltage regardless of the value of the reference voltage. Lower reference voltages will therefore produce larger integral linearity errors in terms of LSBs.

For example, by setting the reference difference to 0.6 V, 0.6 V video signals may be digitized; however the integral linearity error will increase to about ±1.8 LSB; the SNR will be about 40 dB. With a reference difference of 0.5 V, 0.5 V video signals may be digitized with an IL error of about ± 2LSB; the SNR will be about 39 dB.

SNR and Error Rate vs. Clock Timing

Figure 5 illustrates the A/D error rate vs. clock low time, while Figure 6 illustrates the A/D SNR vs. clock high time.

An A/D error is defined as being a sample that is more than 8 LSBs (out of 255) from the expected value, where the previous and following samples are less than (or equal to) 8 LSBs from the expected value.

Output Noise

Although the A/D does exhibit some output noise for a DC input, the output noise remains relatively constant for any input bandwidth. Competitive A/D converters have no noise for a DC input; however, the output noise increases greatly as the input bandwidth and clock rate increase.

The output noise of the A/D may be reduced by adjusting the duty cycle of the clock—this is especially true above 10 MHz clock operation. Note that uncorrelated noise less than 1% peak-to-peak will be perceived with the same quality as that of a consumer 1/2" VCR.

PC Board Sockets

If a socket is required, a low-profile socket is recommended, such as AMP part no. 641747 - 2.

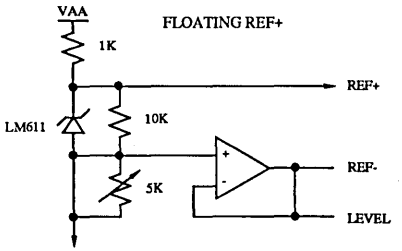


Figure 4. Using an External Reference.

Application Information (continued)

Bt251 with Minimal External Circuitry

Figure 7 shows the Bt251 in an application for digitizing 1 V video signals.

In this instance, the IOUT0 output is driving the top of the reference ladder (REF+) directly, without being buffered by a voltage follower. The 1050 Ω resistor between IOUT0 and GND, in parallel with the reference ladder, develops a 0 V–1.2 V reference voltage for the A/D (based on the contents of the IOUT0 data register). IOUT1 and REF– are connected to GND.

Although this implementation is not as temperature stable as the one shown in Figure 1 (due to some variation in the reference ladder resistance over temperature), it will probably suffice for most applications.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid ADC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

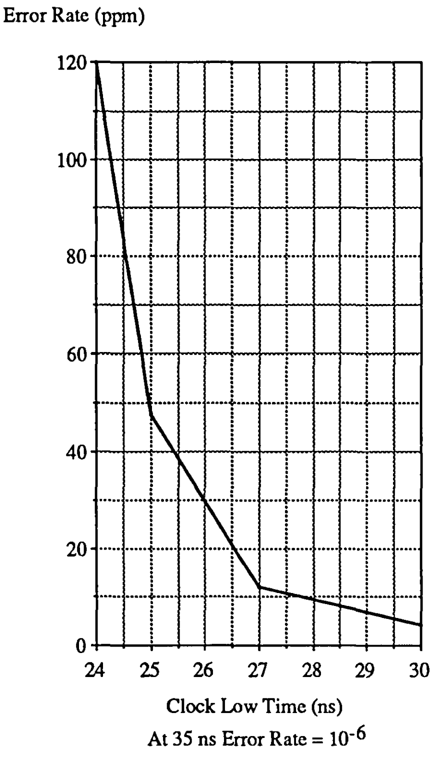


Figure 5. A/D Error Rate vs. Clock Low Time.

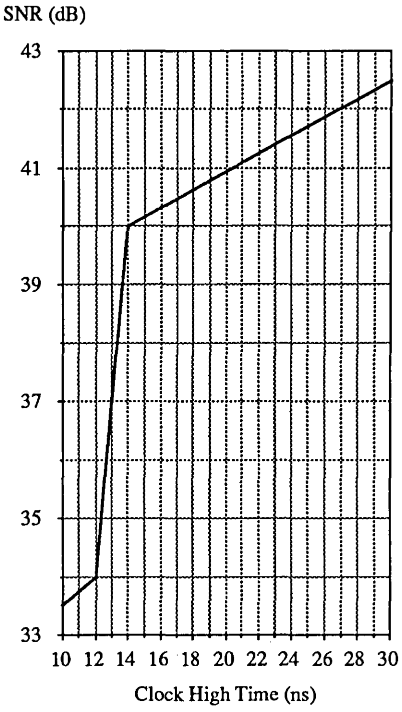


Figure 6. A/D SNR vs. Clock High Time.

Application Information (continued)

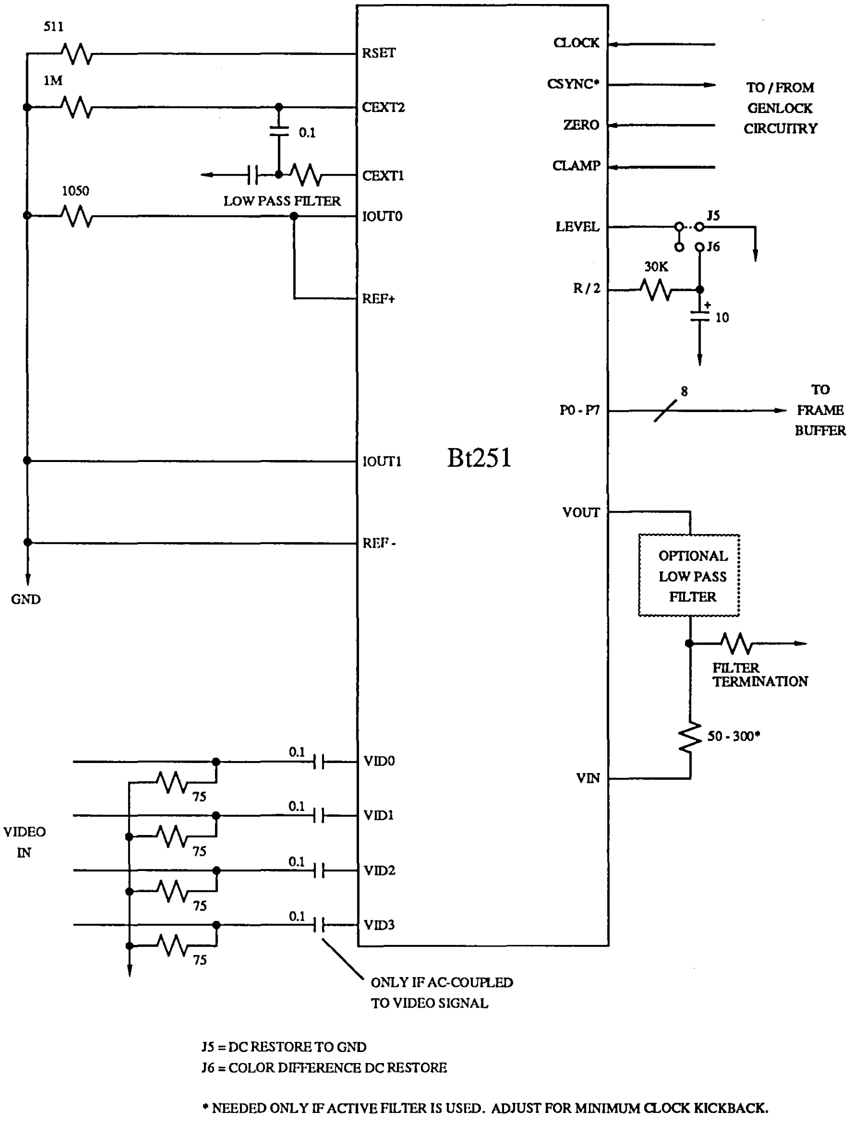

511
1M
0.1
1050
LOW PASS FILTER
RSET
CEXT2
CEXT1
IOUT0
REF+
IOUT1
REF-
GND
Bt251
CLOCK
CSYNC*
ZERO
CLAMP
TO / FROM GENLOCK CIRCUITRY
LEVEL
J5
J6
30K
R/2
10
P0 - P7
8
TO FRAME BUFFER
VOUT
OPTIONAL LOW PASS FILTER
FILTER TERMINATION
50 - 300*
VIN
0.1
VID0
VID1
VID2
VID3
75
VIDEO IN
ONLY IF AC-COUPLED TO VIDEO SIGNAL
J5 = DC RESTORE TO GND
J6 = COLOR DIFFERENCE DC RESTORE
* NEEDED ONLY IF ACTIVE FILTER IS USED. ADJUST FOR MINIMUM CLOCK KICKBACK.

Figure 7. Typical Bt251 External Circuitry.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Voltage References					
Top	REF+	0.7	1	2.0	Volts
Bottom	REF–	0	0	1.3	Volts
Difference (Top–Bottom)		0.7	1	1.2	Volts
VID0–VID3 Amplitude Range		0.5		VAA–0.5	Volts
Multiplexer Compliance (DC)		–0.2		+2.2	Volts
VIN Input Amplitude Range		0.7	1	1.2	Volts
VIN Input Range			REF– to REF+		Volts
CEXT AC Amplitude		0.2 Vp-p		2.0 Vp-p	Volts
LEVEL Input Voltage	TA	GND–0.5	REF–	REF+	Volts
Zeroing Interval			60	150	µS
Ambient Operating Temperature		0		+ 70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Input Voltage	VIN, VIDx	GND–0.5		VAA + 0.5	Volts
R/2 Output Current				25	µA
Ambient Operating Temperature	TA	–55			
Storage Temperature	TS	–65		+125	°C
Junction Temperature	TJ			+150	°C
				+150	°C
Vapor Phase Soldering	TVSOL				
(1 minute)				220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
A/D Resolution		8	8	8	Bits
A/D Accuracy					
Integral Linearity Error (note 1)	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
A/D Offset Error					
Top			tbd		mV
Bottom			tbd		mV
Tempco			tbd		mV / °C
A/D Coding					Binary
No Missing Codes			guaranteed		
VIN Analog Input (note 2)					
CLAMP = 0					
Input Impedance	RIN	10			MΩ
Input Current	IB			1	µA
Input Capacitance	CAIN		15		pF
CLAMP = 1					
Input Impedance	RIN		50		Ω
VID0–VID3 Analog Inputs (note 3)					
Input Impedance to VOUT					
Input Selected			100		Ω
Input Deselected			10		MΩ
Input Capacitance			tbd		pF
REF+ Reference Input					
Input Current			1		mA
Input Impedance			1		kΩ
Clock Kickback (note 4)			tbd		pV - sec
Digital Inputs					
Input High Voltage	VIH	2.0			Volts
Input Low Voltage	VIL			0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance	CIN		10		pF
P0–P7 Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	Volts
Three-State Current	IOZ			1	µA
Output Capacitance	COUT		10		pF
CSYNC* Digital Output					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	Volts
Output Capacitance	COUT		10		

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
D0–D7 Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
Three-State Current	IOZ			1	µA
Output Capacitance	COUT		10		pF
IOUT0 and IOUT1 Outputs					
DAC Output Current		0		2.5	mA
DAC Output Impedance			100		kΩ
DAC Output Capacitance			20		pF
DAC Output Compliance (±100 µA)		–0.2		+1.2	Volts
A/D Power Supply Rejection Ratio (not including reference)	PSRR		tbd		%/% ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1 V and REF– = GND. REF– ≤ Vin ≤ REF+, LEVEL = float. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note 1: Best-fit linearity. Averaged value evaluated using a closed-loop system. Linearity is tested with RAM transparent (data = address).

Note 2: LEVEL = GND.

Note 3: VOUT connected to GND.

Note 4: Measurement of noise coupled onto VIN due to clocking (Rs = 75 Ω). Typically occurs over a 5-ns interval.

Vin* (v)	P0 - P7	OE*
> 0.996	$FF	0
0.992	$FE	0
:	:	:
0.500	$81	0
0.496	$80	0
0.492	$7F	0
:	:	:
0.004	$01	0
< 0.002	$00	0
	3-state	1

*with REF+ = 1.000 V and REF- = 0.000 V. Ideal center values. 1 LSB = 3.9063 mV. RAM transparent (data = address).

A/D Coding.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate	Fs			18	MHz
Multiplexer Switching Time	Tmux		100		ns
ON Resistance			100		Ω
Clock Cycle Time	1	55.5			ns
Clock Low Time	2	35*			ns
Clock High Time	3	20**			ns
P0–P7 Output Delay	4			40	ns
OE* Asserted to P0–P7 Valid	5			50	ns
OE* Negated to P0–P7 3-Stated	6			50	ns
ZERO Setup Time	7	0			ns
ZERO Hold Time	8	20			ns
ZERO, CLAMP High Time (note 1)		1			Clock
Aperture Delay	9		10		ns
Aperture Jitter			50		ps
Full Power Input Bandwidth (note 7)	BW	6			MHz
Transient Response (note 2)				1	Clock
Overload Recovery (note 3)				1	Clock
Zero Recovery Time (note 4)				1	Clock
RMS Signal to Noise Ratio	SNR				
Fin = 4.2 MHz, Fs = 10.7 MHz			43		dB
Fin = 4.2 MHz, Fs = 14.32 MHz			42		dB
Fin = 2.75 MHz, Fs = 6.75 MHz			44		dB
Fin = 5.75 MHz, Fs = 13.5 MHz			41		dB
Fin = 4.2 MHz, Fs = 17.72 MHz			41		dB
Analog Multiplexer Crosstalk					
All Hostile Crosstalk			–50		dB
Single Channel Crosstalk			–50		dB
Adjacent Input Crosstalk			–50		dB
IOUT0, IOUT1 Settling Time to ±1 LSB			100		ns
Differential Gain Error (note 5)	DG		2		%
Differential Phase Error (note 5)	DP		1		Degree
Supply Current (note 6) (Excluding REF+)	IAA		150		mA

See test conditions on next page.

AC Characteristics (continued)

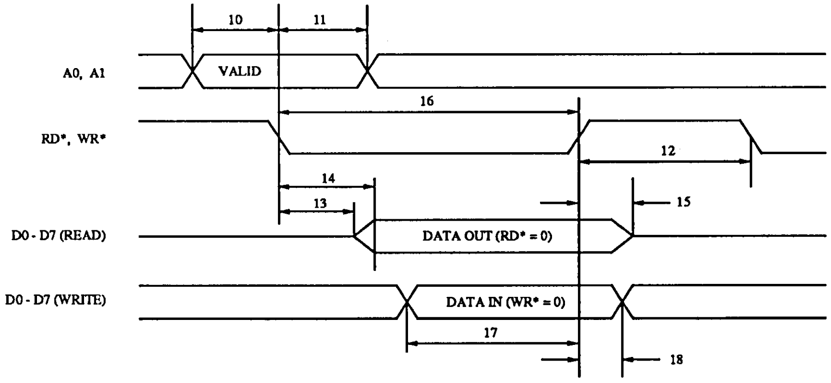
Parameter	Symbol	Min	Typ	Max	Units
A0, A1 Setup Time	10	10			ns
A0, A1 Hold Time	11	10			ns
RD*, WR* High Time	12	50			ns
RD* Asserted to Data Bus Driven	13	5			ns
RD* Asserted to Data Valid	14			40	ns
RD* Negated to Data Bus 3-Stated	15			20	ns
WR* Low Time	16	50			ns
Write Data Setup Time	17	10			ns
Write Data Hold Time	18	10			ns
Pipeline Delay		2	2	2	Clocks

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1 V and REF– = GND. REF– ≤ Vin ≤ REF+, LEVEL = float. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for digital inputs and outputs. D0–D7, P0–P7, CSYNC* output load ≤ 75 pF. VOUT, IOUT0, IOUT1 output load ≤ 75 pF. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

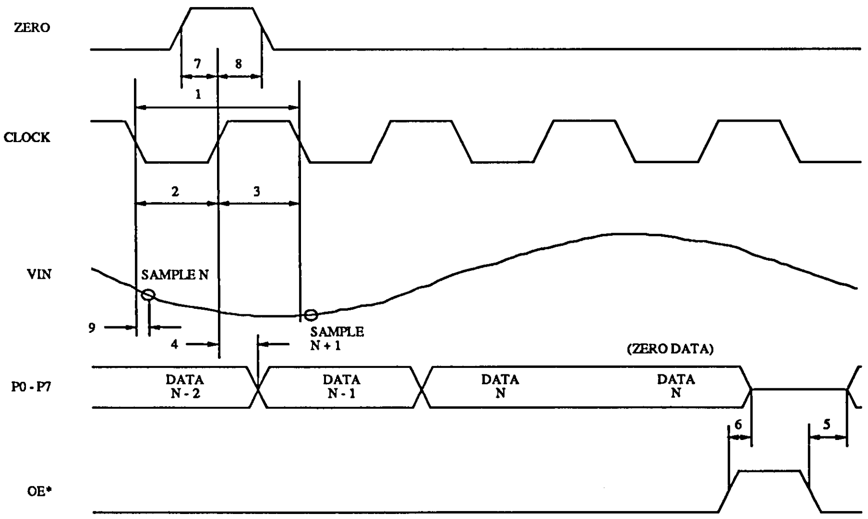
Note 1: Number of clock cycles ZERO is a logical one does not affect linearity. For best performance, ZERO should be a logical one for an odd number of clock cycles.
Note 2: For full-scale step input, full accuracy attained in specified time.
Note 3: Time to recover to full accuracy after a > 1.2 V input signal.
Note 4: Time to recover to full accuracy following a zero cycle.
Note 5: 4x NTSC subcarrier, unlocked.
Note 6: IAA (typ) at VAA = 5.0 V, Fin = 4.2 MHz, Fs = 14.32 MHz.
IAA (max) at VAA = 5.25 V, Fin = 6 MHz, Fs = 18 MHz.
Note 7: Tested.

*For 10^{-6} typical A/D error rate (see Figure 5).
**For typical A/D SNR of 41 dB (see Figure 6).

Timing Waveforms

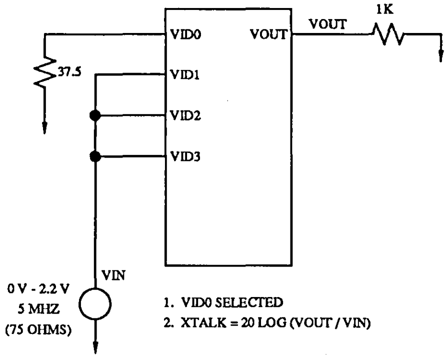

10
11
A0, A1
VALID
16
RD*, WR*
12
14
13
15
D0 - D7 (READ)
DATA OUT (RD* = 0)
D0 - D7 (WRITE)
DATA IN (WR* = 0)
17
18

MPU Read/Write Timing.


ZERO
7
8
1
CLOCK
2
3
VIN
SAMPLE N
9
4
SAMPLE N + 1
(ZERO DATA)
P0 - P7
DATA N - 2
DATA N - 1
DATA N
DATA N
6
5
OE*

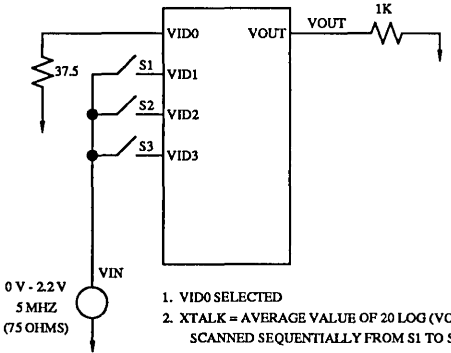
Video Input/Output Timing.

Test Circuits


VID0
VOUT
VOUT
1K
37.5
VID1
VID2
VID3
VIN
0 V - 2.2 V
5 MHZ
(75 OHMS)

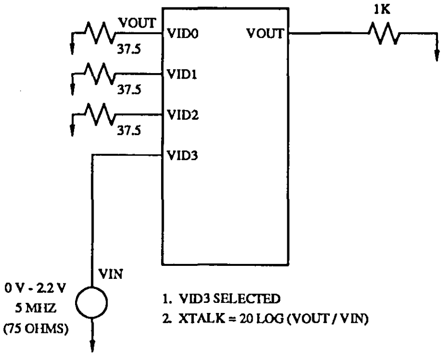
1. VID0 SELECTED
2. XTALK = 20 LOG (VOUT / VIN)

All Hostile Crosstalk Test Circuit.


1K
VOUT
VID0
VOUT
37.5
S1
VID1
S2
VID2
S3
VID3
VIN
0 V - 2.2 V
5 MHZ
(75 OHMS)

1. VID0 SELECTED
2. XTALK = AVERAGE VALUE OF 20 LOG (VOUT / VIN) SCANNED SEQUENTIALLY FROM S1 TO S3
3. OPEN VID INPUTS HAVE 75 OHM TERMINATION TO GND

Single Channel Crosstalk Test Circuit.


VOUT
37.5
VID0
VOUT
1K
37.5
VID1
37.5
VID2
VID3
VIN
0 V - 2.2 V
5 MHZ
(75 OHMS)

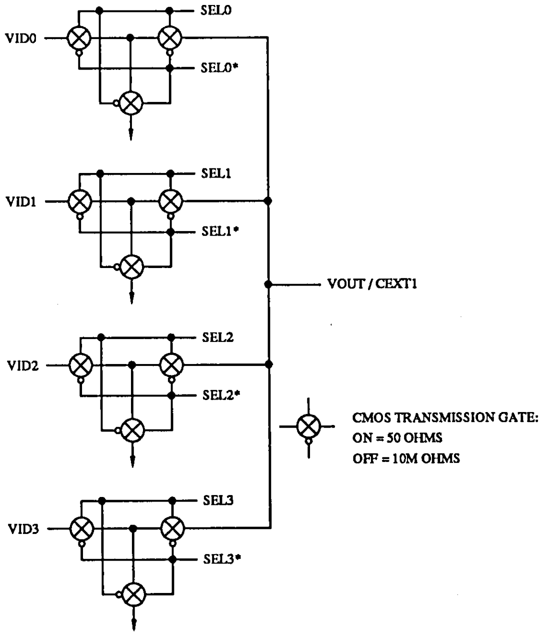
1. VID3 SELECTED
2. XTALK = 20 LOG (VOUT / VIN)

Adjacent Input Crosstalk Test Circuit.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt251KPJ	44-pin Plastic J-Lead	0° to +70° C
Bt251EVM	Bt251 Evaluation Board (includes Bt251KPJ)	

Analog Multiplexer Circuit


SEL0
VID0
SEL0*
SEL1
VID1
SEL1*
VOUT / CEXT1
SEL2
VID2
SEL2*
CMOS TRANSMISSION GATE:
ON = 50 OHMS
OFF = 10M OHMS
SEL3
VID3
SEL3*

Revision History

Datasheet Revision	*Change from Previous Revision*
E	Speed increased to 18 MSPS, production pinout added, AC and DC characteristics have "tbds" replaced with numbers.
F	Maximum DAC output current changed to 2.5 mA; RSET and DAC output resistors changed to 511 Ω. DAC output compliance changed to –0.2 V to +1.2 V. Address register operation corrected.
G	Expanded Applications Section.
H	Revised Figures 1,4, and 7. Updated Table 2. Added parameters.

reliminary Information

his document contains information on a new product. The parametric information, though not fully characterized, is the result of testing initial devices.

Bt253

18 MSPS
Monolithic CMOS Triple-Channel 8-bit Image Digitizer

istinguishing Features

- Three 8-bit Video A/D Converters
- Two Sets Software-Selectable Analog Inputs
- Optional MPU Adjustment of Gain and Offset
- Composite Sync Detection
- Genlock Externally Implemented
- Standard MPU Interface
- TTL Compatible
- +5 V CMOS Monolithic Construction
- 84-pin PLCC Package
- Typical Power Dissipation: 1.5 W

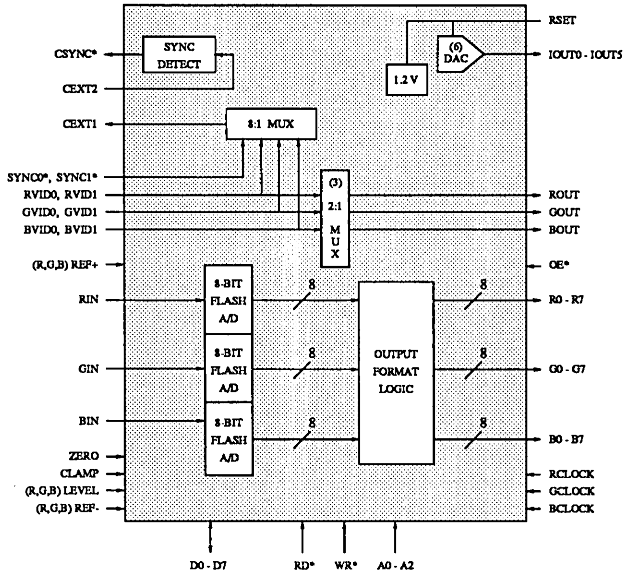
Applications

- Image Processing
- Image Capture
- Desktop Publishing
- Graphic Art Systems

Related Products

- Bt251
- Bt261

unctional Block Diagram


CSYNC*
CEXT2
CEXT1
SYNC0*, SYNC1*
RVID0, RVID1
GVID0, GVID1
BVID0, BVID1
(R,G,B) REF+
RIN
GIN
BIN
ZERO
CLAMP
(R,G,B) LEVEL
(R,G,B) REF-
SYNC DETECT
8:1 MUX
(3) 2:1 MUX
1.2 V
(6) DAC
8-BIT FLASH A/D
8-BIT FLASH A/D
8-BIT FLASH A/D
OUTPUT FORMAT LOGIC
8
RSET
IOUT0 - IOUT5
ROUT
GOUT
BOUT
OE*
R0 - R7
G0 - G7
B0 - B7
RCLOCK
GCLOCK
BCLOCK
D0 - D7
RD*
WR*
A0 - A2

Product Description

The Bt253 Image Digitizer is designed to digitize three channels of video signals, such as RGB, YIQ, YUV, etc., generating up to 24 bits of color pixel information. The architecture also supports single-channel digitization of NTSC and CCIR video signals, generating 8 bits of gray-scale pixel information.

The Bt253 supports 24-bit true color, 15-bit true color, 8-bit true color, and 8-bit pseudo color modes. A standard MPU interface is provided for accessing various control functions.

Six analog inputs (two for each A/D) are supported, selectable under MPU control. The MPU may select from which input to detect sync information for external genlocking. A TTL-compatible composite sync signal is output to interface to genlock circuitry. Two additional sync inputs are also provided to support red, green, blue sync video interfaces.

Optional MPU-controlled adjustment of gain and offset is supported by the ability to program the levels of the REF+ and REF- inputs to the A/D converters. Zeroing and clamping signals are available to control the A/D timing for application-specific timing. The clamping levels are externally set via the red, green, and blue LEVEL pins.

Each A/D converter has its own clock input, top/bottom references, and LEVEL pin.

rooktree Corporation
950 Barnes Canyon Rd.
an Diego, CA 92121
619) 452-7580 • (800) VIDEO IC
LX: 383 596 • FAX: (619) 452-1249
253001 Rev. G

Brooktree®

Circuit Description

MPU Interface

As shown in the functional block diagram, the Bt253 supports a standard MPU interface (D0–D7, RD*, WR*, and A0–A2). MPU operations are asynchronous to the clocks.

A0–A2 address the internal registers, as shown in Table 1.

Flash A/D Converters

The Bt253 uses three 8-bit flash A/D converters to digitize the video signals. Each A/D digitizes analog signals in the range of REF– ≤ Vin ≤ REF+. The output will be a binary number from $00 (Vin ≤ REF–) to $FF (Vin ≥ REF+).

Each A/D converter has its own top and bottom reference: RREF+ and RREF- for the red A/D, GREF+ and GREF- for the green A/D, and BREF+ and BREF– for the blue A/D. Each A/D converter also has its own clock input: RCLOCK for the red A/D, GCLOCK for the green A/D, and BCLOCK for the blue A/D.

RIN, GIN, and BIN may be either DC- or AC-coupled to the video signals. If AC-coupled, the CLAMP and (R,G,B) LEVEL controls may be used to DC-restore the video signals.

Figure 1 shows the internal A/D architecture in detail.

Analog Signal Selection

The Bt253 supports two analog input sources for each A/D converter: RVID0 and RVID1, GVID0 and GVID1, and BVID0 and BVID1. The MPU specifies which ones are to be digitized via the command register.

The selected video signals are output onto ROUT, GOUT, and BOUT. ROUT, GOUT, and BOUT may be connected directly to RIN, GIN, and BIN, respectively, if no filtering or gain of the video signal is required.

If digitizing only the luminance informationa of a video signal containing color subcarrier information, a filter should be used to remove the subcarrier information to avoid possible artifacts on the display screen. A low-pass filter, notch filter, or comb filter may be used to remove the chroma information.

Note that sync information (if present) will still be present on ROUT, GOUT, and BOUT.

The multiplexers are not a break-before-make design. Therefore, during the multiplexer switching time it is possible for the input video signals to be momentarily connected together through the equivalent of 200 Ω.

A2, A1, A0	Addressed by MPU
000	command register
001	IOUT0 data register
010	IOUT1 data register
011	IOUT2 data register
100	IOUT3 data register
101	IOUT4 data register
110	IOUT5 data register
111	reserved

Table 1. Register Addressing.

Circuit Description (continued)

A/D Reference Generation

As shown in Figure 2, the Bt253 may be configured to have either fixed or MPU-adjustable references for the A/D converter.

If jumpers J2 and J4 are selected, RREF+ is connected to a 0.7 V to 1.2 V reference (VREF) and RREF– is connected to GND. This mode of operation may be used when the only operation is to digitize video signals with an amplitude range of 0.7 V to 1.2 V with no adjustment of gain or offset.

If jumpers J1 and J3 are selected, gain and offset of the video signal may be done via the MPU-adjustable outputs IOUT0 and IOUT1. This mode of operation allows top and bottom reference adjustments so that different video signals may be digitized or operations such as contrast enhancement or level adjustments may be implemented. The TLC272 dual CMOS op-amps can be used for single +5 V operation. GREF+, GREF–, BREF+, and BREF– may be similarly configured.

IOUT0–IOUT5 are current outputs (0–2.5 mA) generated by six 6-bit D/A converters. A 511 Ω RSET resistor generates a 2.35 mA full-scale output current. The 511 Ω resistors to GND generate a 0 V to 1.2 V level that drives the (R,G,B)REF+ and (R,G,B)REF– inputs through voltage followers. The top and bottom references may thus be adjusted with 19 mV resolution.

It is not recommended that the DAC outputs drive the top of the reference ladders directly as the reference ladder resistance changes slightly with temperature.

The DACs are current sources; they do not sink current. Thus, if MPU adjustment of (R,G,B)REF– is desired, the DAC outputs must drive (R,G,B)REF– using a voltage follower.

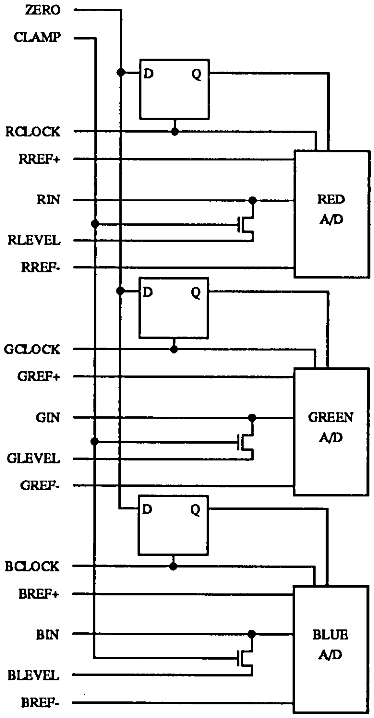


Figure 1. Internal A/D Architecture.

Circuit Description (continued)

A/D Zeroing

The ZERO input is used to zero the comparators, and must be asserted sometime during each horizontal blanking interval. While ZERO is a logical one, the comparators are zeroed. During ZERO cycles, the R0–R7, G0–G7, and B0–B7 outputs are not updated. They retain the data loaded before the ZERO cycle.

Note that each A/D converter uses its own clock to latch the ZERO signal. Thus, ZERO must be asserted for at least one clock cycle of the slowest clock.

A/D Input Clamping

If RIN, GIN, and BIN are AC-coupled to the video signals, the CLAMP and (R,G,B) LEVEL controls may be used to DC restore the video signals. While CLAMP is a logical one, the video signals are clamped to the voltage level present on the (R,G,B) LEVEL pins.

If RIN, GIN, and BIN are DC-coupled to the video signals, all three LEVEL pins should float or CLAMP should always be a logical zero.

VIN Input Considerations

The 50–300 Ω resistor shown in Figure 2 after the low-pass filter is only required if an active low-pass filter is used. It provides isolation from any clock kickback noise on Vin, preventing it from being coupled onto the video signal. The exact value of the resistor should be adjusted for minimum clock kickback noise on Vin. If no filter or a passive low-pass filter is used, the resistor is not required, as the resistance of the multiplexer serves to reduce the clock kickback noise.

The 0.1 µF capacitor shown in Figure 2 after the low-pass filter is only required if an active low-pass filter is used and DC restoration must be performed. If no filter or a passive low-pass filter is used, the capacitor is not required, as the DC restoration can still be implemented using the 0.1 µF capacitors on the (R,G,B)VID inputs.

Multiplexer Considerations

Maintaining DC levels within the rated compliance range is necessary to obtain the best linearity and crosstalk performance. Clamping through the MUX accomplishes this on the selected channel. Adding clamp diodes on all video inputs to a positive bias will optimize multiplexer fidelity.

Sync Detect Circuitry

The Bt253 performs composite sync detection from the analog input specified by the command register. Thus, sync information may be recovered from one analog input while another input is being digitized. The composite sync signal (CSYNC*) contains any serration and equalization pulses the video signal may contain. Note that CSYNC* is output asynchronously to the clock and there are no pipeline delays (the output delay from Vin or SYNC* to CSYNC* is approximately 25 ns).

The MPU specifies from which input to detect sync (negative sync polarity). The selected video signal is output on CEXT1. A 0.1 µF capacitor between CEXT1 and CEXT2 AC-couples the video signal to the sync detection circuit. The MPU selects how many millivolts above the sync tip to use for sync detection. If the sync tip on CEXT2 is below the selected threshold, CSYNC* will be a logical zero.

Two additional sync inputs are provided (SYNC0* and SYNC1*) to support red, green, blue sync systems. SYNC0* and SYNC1* may be either TTL or normal video signal levels.

If it is desired to low-pass filter the sync signal prior to sync detection, the low-pass filter should be inserted between CEXT1 and the 0.1 µF capacitor (see Figure 2).

If the sync detection circuit is not used, CEXT2 should be connected to GND or VAA (CEXT1 may float), or an unused (grounded) video input selected for the sync detector.

External Sync Detection

CEXT1 may be connected to an external sync detector circuit. In this case, CEXT2 should be connected directly to GND or VAA and the CSYNC* output left floating.

The sync analog multiplexer may still be used to select from which video source to detect sync information. As the multiplexer switches analog video signals, the selected video source will be output onto CEXT1.

Color Output Modes

The Bt253 outputs several modes of color information, as shown in Table 2.

R0–R7, G0–G7, and B0–B7 are three-stated while OE* is a logical one.

Circuit Description (continued)

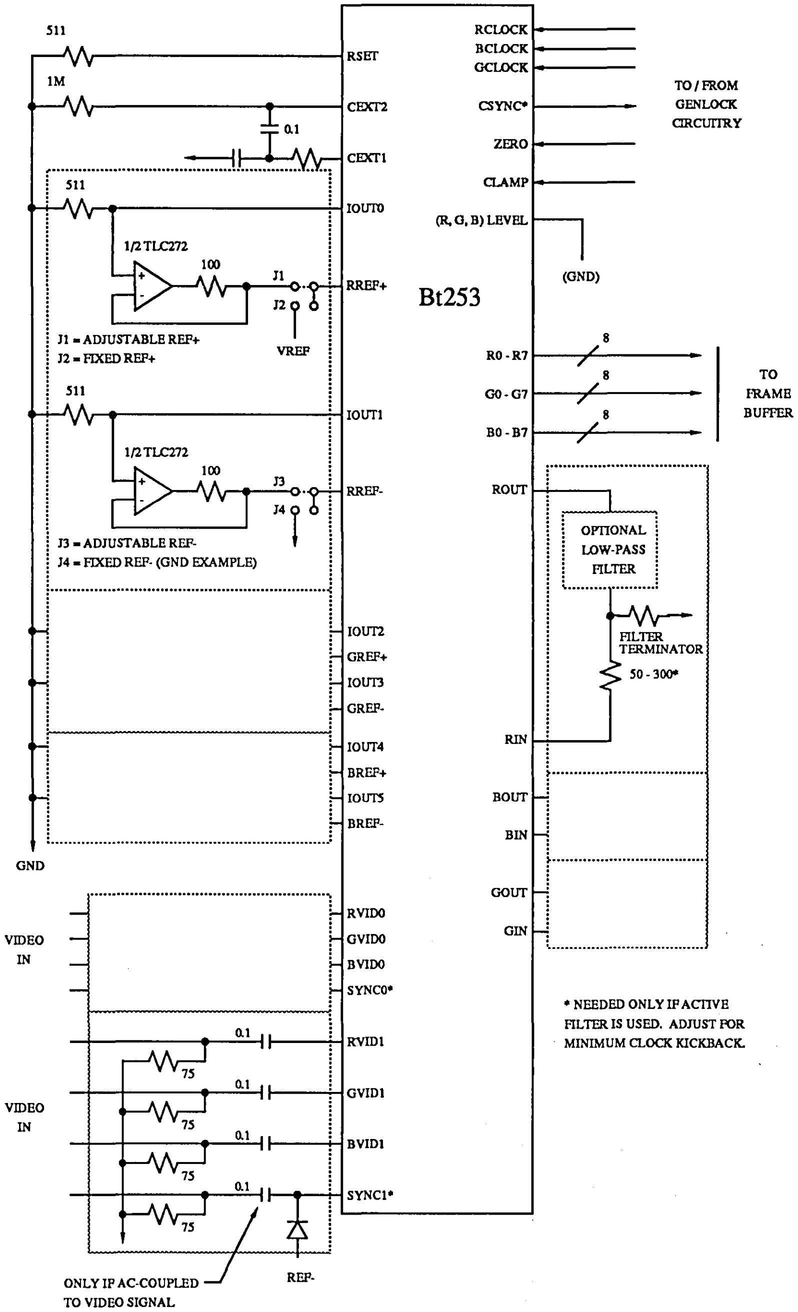

511
RSET
1M
CEXT2
0.1
CEXT1
511
IOUT0
1/2 TLC272
100
J1
J2
RREF+
J1 = ADJUSTABLE REF+
J2 = FIXED REF+
VREF
511
IOUT1
1/2 TLC272
100
J3
J4
RREF-
J3 = ADJUSTABLE REF-
J4 = FIXED REF- (GND EXAMPLE)
IOUT2
GREF+
IOUT3
GREF-
IOUT4
BREF+
IOUT5
BREF-
GND
VIDEO IN
RVID0
GVID0
BVID0
SYNC0*
VIDEO IN
0.1
75
RVID1
GVID1
BVID1
SYNC1*
ONLY IF AC-COUPLED TO VIDEO SIGNAL
REF-
Bt253
RCLOCK
BCLOCK
GCLOCK
CSYNC*
ZERO
CLAMP
(R, G, B) LEVEL
(GND)
TO / FROM GENLOCK CIRCUITRY
R0 - R7
G0 - G7
B0 - B7
8
TO FRAME BUFFER
ROUT
OPTIONAL LOW-PASS FILTER
FILTER TERMINATOR
50 - 300*
RIN
BOUT
BIN
GOUT
GIN
* NEEDED ONLY IF ACTIVE FILTER IS USED. ADJUST FOR MINIMUM CLOCK KICKBACK.

Figure 2. Typical Bt253 External Circuitry.

Internal Registers

Command Register

The command register may be written to or read by the MPU at any time, and is not initialized. D0 is the least significant bit.

D7	Digitize select (0) xVID0 (1) xVID1	This bit specifies which analog input is to be digitized. The selected signals are output onto ROUT, GOUT, and BOUT.
D6–D4	Sync detect select (000) RVID0 (001) RVID1 (010) GVID0 (011) GVID1 (100) BVID0 (101) BVID1 (110) SYNC0* (111) SYNC1*	Composite sync information detected on the selected input is output onto CSYNC*.
D3, D2	Color output select (00) 24-bit true color (01) 15-bit true color (10) 8-bit true color (11) 8-bit pseudo color	Color output mode select. See Table 2. In mode (11), the red and blue A/D converters are ignored.
D1	reserved (logical zero)	A logical zero must be written to this bit when writing to the command register.
D0	Sync detect level select (0) 125 mV (1) 50 mV	This bit specifies how much above the sync tip to slice CEXT2 for sync detection.

Internal Registers (continued)

IOUT Data Registers

These six 8-bit registers specify the output current on the IOUT0–IOUT5 outputs, from 0 mA ($00) to full scale ($FC). The six MSBs of data are used to drive the DACs. D0 and D1 (the two LSBs) must be programmed to be a logical zero.

These registers may be written to or read by the MPU at any time and are not initialized. D0 is the least significant bit.

	24-Bit True Color	15-Bit True Color	8-Bit True Color	8-Bit Pseudo Color
Output Pins	Mode (00)	Mode (01)	Mode (10)	Mode (11)
R7	R7	0	R7	G7
R6	R6	R7	R6	G6
R5	R5	R6	R5	G5
R4	R4	R5	G7	G4
R3	R3	R4	G6	G3
R2	R2	R3	G5	G2
R1	R1	G7	B7	G1
R0	R0	G6	B6	G0
G7	G7	G5	R7	G7
G6	G6	G4	R6	G6
G5	G5	G3	R5	G5
G4	G4	B7	G7	G4
G3	G3	B6	G6	G3
G2	G2	B5	G5	G2
G1	G1	B4	B7	G1
G0	G0	B3	B6	G0
B7	B7	0	R7	G7
B6	B6	0	R6	G6
B5	B5	0	R5	G5
B4	B4	0	G7	G4
B3	B3	0	G6	G3
B2	B2	0	G5	G2
B1	B1	0	B7	G1
B0	B0	0	B6	G0

Table 2. Color Output Configurations.

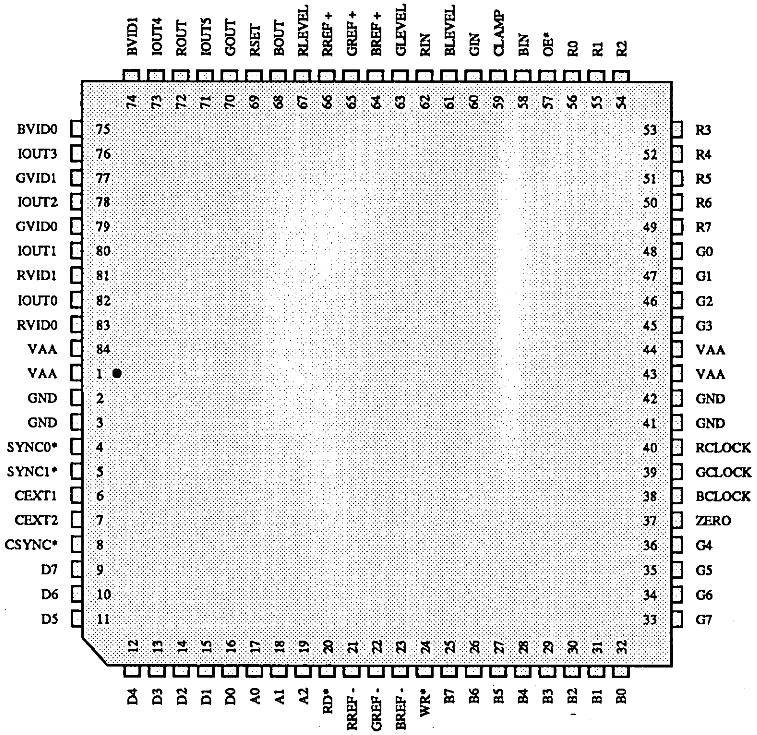
Pin Descriptions

Pin Name	Description
General Reference Functions	
RSET	Full-scale adjust control. An external 511 Ω resistor must be connected between this pin and GND. It is used to provide reference information to the internal D/A converters. See Figure 2.
IOUT0–IOUT5	Current outputs. The amount of output current is specified by the IOUT data registers. External 511 Ω resistors are typically connected between these pins and GND. See Figure 2. The relationship between full scale IOUT and RSET is: IOUT (mA) = 1,200 / RSET (Ω)
CEXT1, CEXT2	External capacitor pins. A 0.1 µF capacitor must be connected between CEXT1 and CEXT2 to AC-couple the video signal to the sync detect circuitry. A 1M Ω resistor must also be connected between CEXT2 and GND. If AC coupled, amplitude is < 2 Vp–p.
A/D Functions	
RREF+, GREF+, BREF+	Red, green, and blue top of resistor ladder (voltage input). These set the Vin voltage level that generates $FF from the appropriate A/D converter. Decoupling capacitors are NOT recommended for the REF+ pins.
RREF–, GREF–, BREF–	Red, green, and blue bottom of resistor ladder (voltage input). These set the Vin voltage level that generates $00 from the appropriate A/D converter.
ZERO	Zeroing control input (TTL compatible). While ZERO is a logical one, the comparators of the A/D converters are zeroed. The red A/D converter latches ZERO on the rising edge of RCLOCK, the green A/D converter latches ZERO on the rising edge of GCLOCK, and the blue A/D converter latches ZERO on the rising edge of BCLOCK. During zeroing cycles, R0–R7, G0–G7, and B0–B7 are not updated; they retain the data loaded before the zeroing cycle.
CLAMP	Clamp control input (TTL compatible). While CLAMP is a logical one, the RIN, GIN, and BIN inputs are forced to the voltage level on the (R, G, B) LEVEL pins to perform DC restoration of the video signals. In applications where RIN, GIN, and BIN are DC-coupled to the video signals, the LEVEL pins should float or CLAMP should always be a logical zero. CLAMP is asynchronous to the clocks.
RLEVEL, GLEVEL, BLEVEL	Red, green, and blue level control inputs (voltage inputs). These inputs are used to specify what voltage level is to be used for DC restoration while CLAMP is a logical one. In applications where RIN, GIN, and BIN are DC-coupled to the signals, the LEVEL pins should float or CLAMP should always be a logical zero.
Input Selection	*Functions*
RIN, GIN, BIN	A/D converter inputs. The analog signals to be digitized should be connected to these analog input pins.
RVID0, RVID1, ROUT	Red channel analog inputs and analog output. RVID0 and RVID1 are connected to the video signals to be digitized. The signal selected to be digitized is output onto ROUT. Unused inputs should be connected to GND.
GVID0, GVID1, GOUT	Green channel analog inputs and analog output. GVID0 and GVID1 are connected to the video signals to be digitized. The signal selected to be digitized is output onto GOUT. Unused inputs should be connected to GND.

Pin Descriptions (continued)

Pin Name	Description
BVID0, BVID1, BOUT	Blue channel analog inputs and analog output. BVID0 and BVID1 are connected to the video signals to be digitized. The signal selected to be digitized is output onto BOUT. Unused inputs should be connected to GND.
Timing Functions	
RCLOCK, GCLOCK, BCLOCK	Clock inputs (TTL compatible). It is recommended that these pins be connected together and driven by a dedicated TTL buffer to minimize sampling jitter.
CSYNC*	Recovered composite sync output (TTL compatible). Sync information is detected from the xVID0 or xVID1 input (as specified by the command register), converted to TTL levels, and output onto this pin. SYNC0* or SYNC1* may also be selected as inputs to the sync detector. CSYNC* is output asynchronously to the clocks and there are no pipeline delays.
SYNC0*, SYNC1*	Sync inputs. Sync information may be input via these pins and output onto CSYNC*. SYNC0* and SYNC1* may be either TTL or normal video signal levels. Unused inputs should be connected to GND.
Digital Control Functions	
R0–R7, G0–G7, B0–B7	Digitized video data outputs (TTL compatible). R0–R7 are output following the rising edge of RCLOCK, G0–G7 are output following the rising edge of GCLOCK, and B0–B7 are output following the rising edge of BCLOCK. They are three-stated if OE* is a logical one. R0, G0, and B0 are the least significant bits.
OE*	Output enable control input (TTL compatible). A logical one three-states R0–R7, G0–G7, and B0–B7 asynchronously to the clocks.
RD*	Read control input (TTL compatible). If RD* is a logical zero, data is output onto D0–D7. RD* and WR* should not be asserted simultaneously.
WR*	Write control input (TTL compatible). If WR* is a logical zero, data is written into the device via D0–D7. Data is latched on the rising edge of WR*. RD* and WR* should not be asserted simultaneously.
D0–D7	Bidirectional data bus (TTL compatible). MPU data is transferred into and out of the device over this 8-bit data bus. D0 is the least significant bit.
A0–A2	Address control inputs (TTL compatible). A0–A2 address the internal registers as shown in Table 1. They are latched on the falling edge of RD* or WR*.
Power and Ground	
VAA	+5 V power. All VAA pins must be connected together as close to the device as possible. A 0.1 µF ceramic capacitor should be connected between each group of VAA pins and GND, as close to the device as possible.
GND	Ground. All GND pins must be connected as close to the device as possible.

Pin Descriptions (continued)


BVID1 74
IOUT4 73
ROUT 72
IOUT5 71
GOUT 70
RSET 69
BOUT 68
RLEVEL 67
RREF+ 66
GREF+ 65
BREF+ 64
GLEVEL 63
RIN 62
BLEVEL 61
GIN 60
CLAMP 59
BIN 58
OE* 57
R0 56
R1 55
R2 54
BVID0 75
IOUT3 76
GVID1 77
IOUT2 78
GVID0 79
IOUT1 80
RVID1 81
IOUT0 82
RVID0 83
VAA 84
VAA 1
GND 2
GND 3
SYNC0* 4
SYNC1* 5
CEXT1 6
CEXT2 7
CSYNC* 8
D7 9
D6 10
D5 11
53 R3
52 R4
51 R5
50 R6
49 R7
48 G0
47 G1
46 G2
45 G3
44 VAA
43 VAA
42 GND
41 GND
40 RCLOCK
39 GCLOCK
38 BCLOCK
37 ZERO
36 G4
35 G5
34 G6
33 G7
12 D4
13 D3
14 D2
15 D1
16 D0
17 A0
18 A1
19 A2
20 RD*
21 RREF-
22 GREF-
23 BREF-
24 WR*
25 B7
26 B6
27 B5
28 B4
29 B3
30 B2
31 B1
32 B0

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS Digitizer layout examples found in the *Bt208, Bt251, or Bt253 Evaluation Module Operation and Measurements*, application notes (AN-13, 14, and 15, respectively). These application notes can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt253 power and ground lines by shielding the digital inputs/outputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

Ground Planes

The ground plane area should encompass all Bt253 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt253, the analog input traces, any input amplifiers, and all the digital signal traces leading up to the Bt253.

Power Planes

The Bt253 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt253.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt253 power pins, any voltage reference circuitry, and any input amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged so that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Best performance is obtained using a dedicated linear regulator to provide power to the Bt253.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. These capacitors should also be placed as close as possible to the device.

Each group of VAA pins should have a 0.1 µF ceramic bypass capacitor to GND, located as close as possible to the device.

Digital Signal Interconnect

The digital signals of the Bt253 should be isolated as much as possible from the analog signals and other analog circuitry. Also, the digital signals should not overlay the analog power plane.

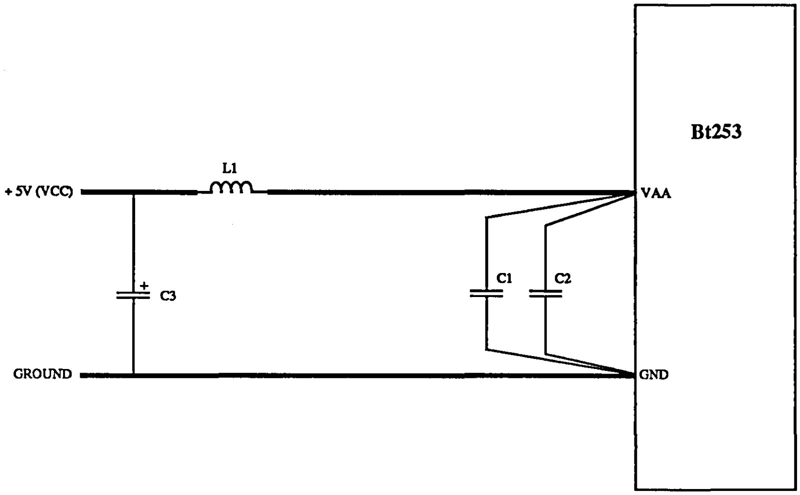
Any termination resistors for the digital signals should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

Long lengths of closely spaced parallel video signals should be avoided to minimize crosstalk. Ideally, there should be a ground line between the video signal traces driving the VIDx inputs.

Also, avoid routing high-speed TTL signals close to the analog signals to minimize noise coupling.

PC Board Layout Considerations (continued)



Location	Description	Vendor Part Number
C1, C2	0.1 μF ceramic capacitor	Erie RPE112Z5U104M50V
C3	10 μF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt253.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

Zeroing

As the comparators on the Bt253 must be periodically zeroed, it is convenient to assert ZERO during each horizontal retrace interval.

Note that before using the Bt253 after a power-up condition, ZERO must be a logical one for at least 1000 clock cycles (cumulative) to initialize the comparators to the rated linearity. In normal video applications this will be transparent due to the number of horizontal scan lines that will have occurred before using the Bt253.

As long as the recommended zeroing interval is maintained, the Bt253 will meet linearity specifications. The longer the time between zeroing intervals, the more the linearity error increases.

Increasing the Resolution of DACs

With a 511 Ω resistor connected between each DAC output (IOUT0–OUT5) and GND, the resolution of the ladder adjustment is 19 mV. The resolution of the top of the resistor ladder (REF+) adjustment may be increased by biasing the DAC outputs and using the DAC outputs to adjust the voltage over a smaller range with finer resolution.

Figure 4 shows a circuit that allows adjustment of the REF+ inputs from 0.714 V to 1 V with 4.5 mV resolution. With the DAC data = $00, 0.714 V is output; if the DAC data = $FC, 1 V is output.

As the typical maximum DAC output current is 2.35 mA (RSET = 511 Ω), if a 0.286 V adjustable range is desired, R1 || R2 must equal 121 Ω. The minimum output voltage desired determines the ratio of R1 and R2:

$$V_{min} = VREF * (R2 / (R1 + R2))$$

The bottom of the resistor ladder (REF–) may be adjusted from 0 V to 0.286 V with 4.5 mV resolution by using a 121 Ω resistor to ground rather than a 511 Ω resistor. As long as the minimum range is 0 V, the resistor to ground may be used to adjust the total range, and thus the resolution.

Video Standard	Nominal Amplitude	Worst Case Amplitudes
RS-170 w/o sync	1.0 V BLACK - WHITE	0.9–1.1 V
RS-170 w/ sync	1.4 V SYNC - WHITE	1.2–1.6 V
RS-170A w/sync	1.2 V SYNC - WHITE	1.0–1.4 V
RS-343A w/o sync	0.7 V BLACK - WHITE	0.6–0.85 V

Table 3. Video Signal Tolerances.

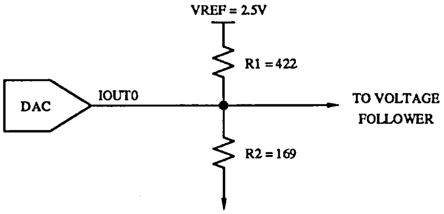


Figure 4. Increasing DAC Output Resolution.

Application Information (continued)

Using an External Reference

Figure 5 illustrates using a 1.2 V LM385 to generate a 0 V to 1.2 V reference for applications requiring a better reference tempco than the internal reference can supply. Supply decoupling of the op-amp is not shown. Any standard op-amp may be used that is capable of operating from a single +5 V supply.

As REF+ should be driven by a high AC impedance source, a 100 Ω resistor should be placed between REF+ and the output of the op-amp, as shown in Figure 5. REF– may be driven in a similar manner if a value other than GND is desired.

Input Ranges

Table 3 shows some common video signal amplitudes. For signals possibly exceeding 1.2 V, the signal should be attenuated (using a resistor divider network) so as not to exceed the 1.2 V input range.

When digitizing with a full scale range less than 0.7 V, the Bt253's integral linearity errors are constant in terms of voltage regardless of the value of the reference voltage. Lower reference voltages will therefore produce larger integral linearity errors in terms of LSBs.

For example, by setting the reference difference to 0.6 V, 0.6 V video signals may be digitized; however the integral linearity error will increase to about ±1.8 LSB; the SNR will be about 40 dB. With a reference difference of 0.5 V, 0.5 V video signals may be digitized with an IL error of about ±2 LSB; the SNR will be about 39 dB.

SNR and Error Rate vs. Clock Timing

Figure 6 illustrates the A/D error rate vs. clock low time, while Figure 7 illustrates the A/D SNR vs. clock high time.

An A/D error is defined as being a sample that is more than 8 LSBs (out of 255) from the expected value, where the previous and following samples are less than (or equal to) 8 LSBs from the expected value.

Output Noise

Although the A/D does exhibit some output noise for a DC input, the output noise remains relatively constant for any input bandwidth. Competitive A/D converters have no noise for a DC input; however, the output noise increases greatly as the input bandwidth and clock rate increase.

The output noise of the A/D may be reduced by adjusting the duty cycle of the clock—this is especially true above 10 MHz clock operation. Note that uncorrelated noise less than 1% peak-to-peak will be perceived with the same quality as that of a consumer 1/2 inch VCR.

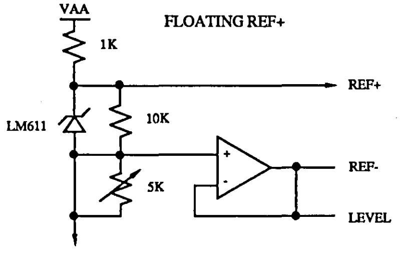


Figure 5. Using an External Reference.

Application Information (continued)

PC Board Sockets

If a socket is required, a low-profile socket is recommended, such as AMP part no. 643066 - 2.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid ADC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

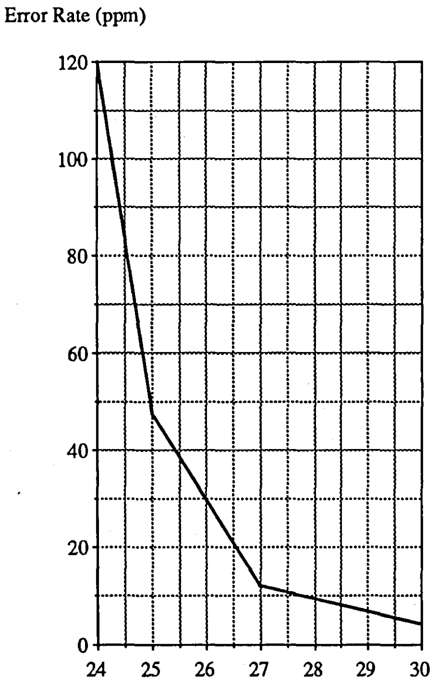


Figure 6. A/D Error Rate vs. Clock Low Time.

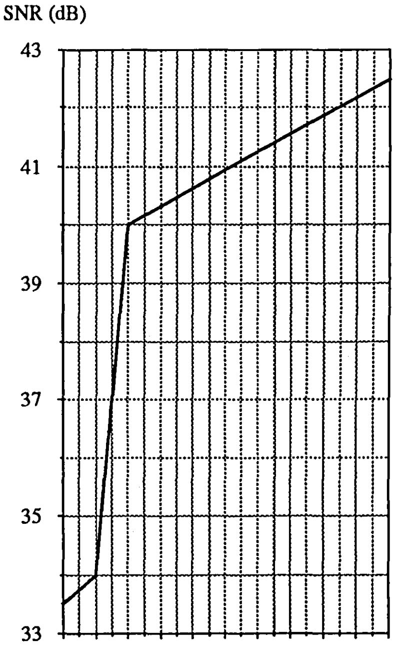


Figure 7. A/D SNR vs. Clock High Time.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Voltage References					
Top	xREF+	0.7	1	2.0	Volts
Bottom	xREF–	0	0	1.3	Volts
Difference (Top–Bottom)		0.7	1	1.2	Volts
VID0–VID1 Amplitude Range		0.5		VAA–0.5	Volts
Multiplexer Compliance (DC)		–0.2		+2.2	Volts
(R,G,B) IN Amplitude Range		0.7	1	1.2	Volts
(R,G,B) IN Input Range			REF– to REF+		Volts
CEXT AC Amplitude		0.2 Vp–p		2.0 Vp–p	Volts
(R,G,B) LEVEL Input Voltage		GND–0.5	REF–	REF+	Volts
Zeroing Interval			60	150	µS
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Input Voltage	VIN, VIDx	GND–0.5		VAA + 0.5	Volts
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
A/D Resolution		8	8	8	Bits
A/D Accuracy					
Integral Linearity Error (note 1)	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
A/D Offset Error					
Top			tbd		mV
Bottom			tbd		mV
Tempco			tbd		mV / °C
A/D to A/D Matching			tbd		%
A/D Coding					Binary
No Missing Codes			guaranteed		
(R,G,B) IN Inputs (note 2)					
CLAMP = 0					
Input Impedance	RIN	10			M-ohms
Input Current	IB			1	µA
Input Capacitance	CAIN		15		pF
CLAMP = 1					
Input Impedance	RIN		50		Ohms
(R,G,B) VID0,1 Inputs (note 3)					
Input Impedance to (R,G,B) OUT					
Input Selected			100		Ohms
Input Deselected			10		M ohms
Input Capacitance			tbd		pF
(R,G,B) REF+ Reference Inputs					
Input Current			1		mA
Input Impedance			1		kΩ
Clock Kickback (note 4)			tbd		pV - sec
Digital Inputs					
Input High Voltage	VIH	2.0			Volts
Input Low Voltage	VIL			0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			−1	µA
Input Capacitance	CIN		10		pF
RGB (0–7) Digital Outputs					
Output High Voltage (IOH = −400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	Volts
Three-State Current	IOZ			1	µA
Output Capacitance	COUT		10		pF
CSYNC* Digital Output					
Output High Voltage (IOH = −400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	Volts
Output Capacitance	COUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
D0 - D7 Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
Three-State Current	IOZ			1	µA
Output Capacitance	COUT		10		pF
IOUT0 - IOUT5 Outputs					
DAC Output Current		0		2.5	mA
DAC Output Impedance			100		kΩ
DAC Output Capacitance			20		pF
DAC Output Compliance		–0.2		+1.2	Volts
A/D Power Supply Rejection Ratio (f = 1 kHz)	PSRR		tbd		%/% ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with (R,G,B)REF+ = 1 V and (R,G,B)REF– = GND. REF– ≤ Vin ≤ REF+, (R,G,B) LEVEL = float. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note 1: Best-fit linearity (offset independent). Averaged value evaluated using a closed loop system.

Note 2: (R,G,B)LEVEL = GND.

Note 3: ROUT, GOUT, BOUT connected to GND.

Note 4: Measurement of noise coupled onto RIN, GIN, and BIN due to clocking (Rs = 75 Ω). Typically occurs over a 5-ns interval.

Vin* (V)	(R,G,B) 0–7	OE*
> 0.996	$FF	0
0.992	$FE	0
:	:	:
0.500	$81	0
0.496	$80	0
0.492	$7F	0
:	:	:
0.004	$01	0
< 0.002	$00	0
	3-state	1

*with (R,G,B)REF+ = 1.000 V and (R,G,B)REF- = 0.000 V. Ideal center values.
1 LSB = 3.9063 mV.

A/D Coding.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate	Fs			18	MHz
Multiplexer Switching Time ON RESISTANCE	Tmux		100 100		ns
Clock Cycle Time Clock Low Time Clock High Time	1 2 3	55.5 35* 20**			ns ns ns
R,G,B(0–7) Output Delay OE* Asserted to Pixel Data Valid OE* Negated to Pixel Data 3-Stated	4 5 6			40 50 50	ns ns ns
ZERO Setup Time ZERO Hold Time ZERO, CLAMP High Time (note 1)	7 8	0 20 1			ns ns Clock
Aperture Delay Aperture Jitter Full Power Input Bandwidth (note 7)	9 BW	 6	10 50		ns ps MHz
Transient Response (note 2) Overload Recovery (note 3) Zero Recovery Time (note 4)				1 1 1	Clock Clock Clock
RMS Signal-to-Noise Ratio Fin = 4.2 MHz, Fs = 10.7 MHz Fin = 4.2 MHz, Fs = 14.32 MHz Fin = 2.75 MHz, Fs = 6.75 MHz Fin = 5.75 MHz, Fs = 13.5 MHz Fin = 4.2 MHz, Fs = 17.72 MHz	SNR		 43 42 44 41 41		 dB dB dB dB dB
Analog Multiplexer Crosstalk All Hostile Crosstalk Single Channel Crosstalk Adjacent Input Crosstalk			 –50 –50 –50		 dB dB dB
IOUT0–IOUT5 Settling Time to ± 1 LSB			100		ns
Differential Gain Error (note 5) Differential Phase Error (note 5)	DG DP		2 1		% Degree
Supply Current (note 6) (Excluding REF+)	IAA		300	tbd	mA

AC Characteristics (continued)

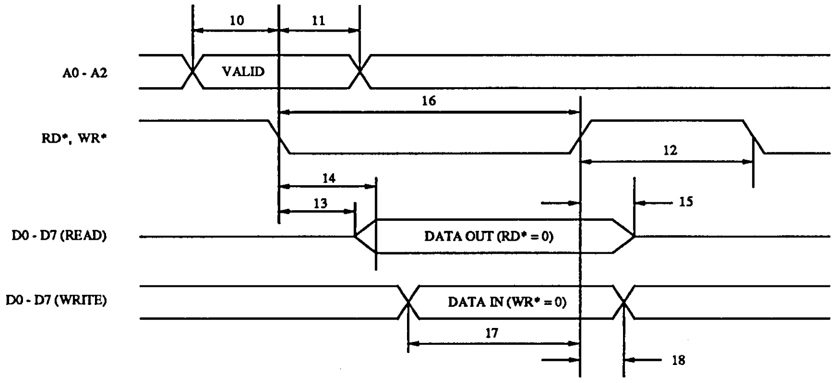
Parameter	Symbol	Min	Typ	Max	Units
A0–A2 Setup Time	10	10			ns
A0–A2 Hold Time	11	10			ns
RD*, WR* High Time	12	50			ns
RD* Asserted to Data Bus Driven	13	5			ns
RD* Asserted to Data Valid	14			40	ns
RD* Negated to Data Bus 3-Stated	15			20	ns
WR* Low Time	16	50			ns
Write Data Setup Time	17	10			ns
Write Data Hold Time	18	10			ns
Pipeline Delay		1	1	1	Clock

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with (R,G,B)REF+ = 1 V and (R,G,B)REF– = GND. REF– ≤ Vin ≤ REF+, (R,G,B) LEVEL = float. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for digital inputs and outputs. D0–D7 output load ≤ 75 pF. CSYNC*, R0–R7, G0–G7, and B0–B7 output load ≤ 75 pF. ROUT, GOUT, BOUT, IOUT0–IOUT5 output load ≤ 75 pF. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

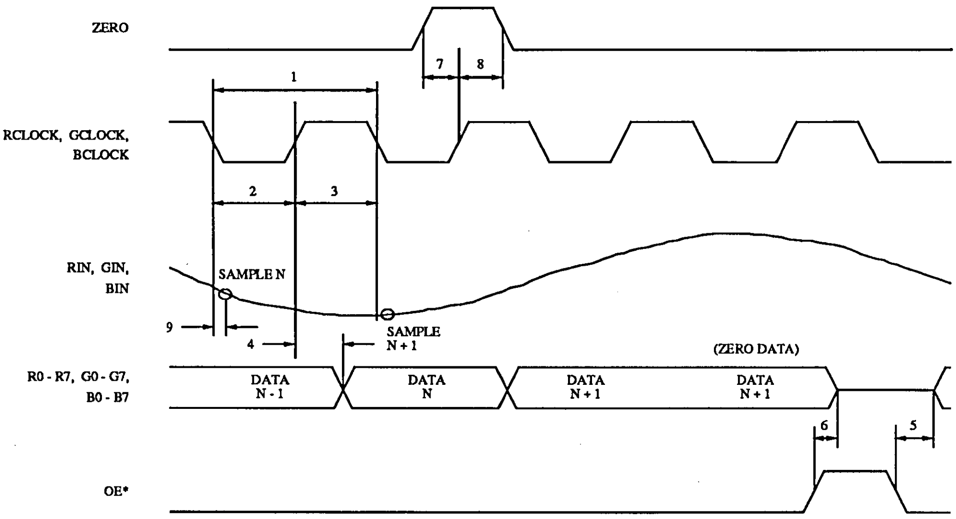
Note 1: Number of clock cycles ZERO is a logical one does not affect linearity. For best performance, ZERO should be a logical one for an odd number of clock cycles.
Note 2: For full-scale step input, full accuracy attained in specified time.
Note 3: Time to recover to full accuracy after a > 1.2 V input signal.
Note 4: Time to recover to full accuracy following a zero cycle.
Note 5: 4x NTSC subcarrier, unlocked.
Note 6: IAA (typ) at VAA = 5.0 V, Fin = 4.2 MHz, Fs = 14.32 MHz.
IAA (max) at VAA = 5.25 V, Fin = 7.5 MHz, Fs = 15 MHz.
Note 7: Tested

*For 10^{-6} typical A/D error rate (see Figure 6).

Timing Waveforms

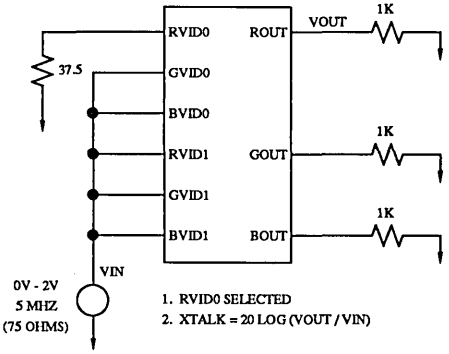

10
11
A0 - A2
VALID
16
RD*, WR*
12
14
13
15
D0 - D7 (READ)
DATA OUT (RD* = 0)
D0 - D7 (WRITE)
DATA IN (WR* = 0)
17
18

MPU Read/Write Timing.


ZERO
7
8
1
RCLOCK, GCLOCK, BCLOCK
2
3
RIN, GIN, BIN
SAMPLE N
9
4
SAMPLE N + 1
(ZERO DATA)
R0 - R7, G0 - G7, B0 - B7
DATA N - 1
DATA N
DATA N + 1
DATA N + 1
6
5
OE*

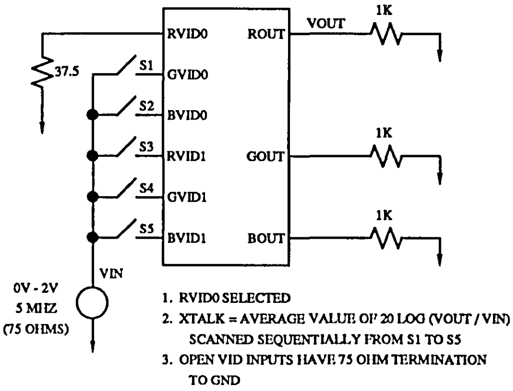
Video Input/Output Timing.

Test Circuits


RVID0
GVID0
BVID0
RVID1
GVID1
BVID1
ROUT
GOUT
BOUT
VOUT
1K
1K
1K
37.5
VIN
0V - 2V
5 MHZ
(75 OHMS)

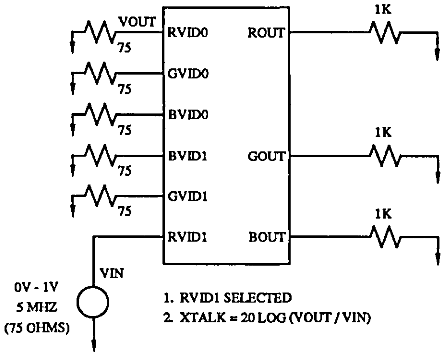
1. RVID0 SELECTED
2. XTALK = 20 LOG (VOUT / VIN)

All Hostile Crosstalk Test Circuit.


RVID0
GVID0
BVID0
RVID1
GVID1
BVID1
ROUT
GOUT
BOUT
VOUT
1K
1K
1K
37.5
S1
S2
S3
S4
S5
VIN
0V - 2V
5 MHZ
(75 OHMS)

1. RVID0 SELECTED
2. XTALK = AVERAGE VALUE OF 20 LOG (VOUT / VIN) SCANNED SEQUENTIALLY FROM S1 TO S5
3. OPEN VID INPUTS HAVE 75 OHM TERMINATION TO GND

Single Channel Crosstalk Test Circuit.


RVID0
GVID0
BVID0
BVID1
GVID1
RVID1
ROUT
GOUT
BOUT
VOUT
75
75
75
75
75
1K
1K
1K
VIN
0V - 1V
5 MHZ
(75 OHMS)

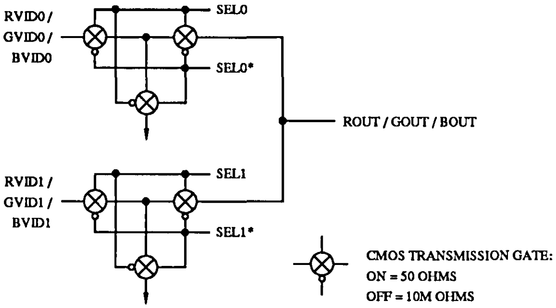
1. RVID1 SELECTED
2. XTALK = 20 LOG (VOUT / VIN)

Adjacent Input Crosstalk Test Circuit.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt253KPJ	84-pin Plastic J-Lead	0° to +70° C
Bt253EVM	Bt253 Evaluation Board (includes Bt253KPJ)	

Analog Multiplexer Circuit


RVID0 /
GVID0 /
BVID0
SEL0
SEL0*
ROUT / GOUT / BOUT
RVID1 /
GVID1 /
BVID1
SEL1
SEL1*
CMOS TRANSMISSION GATE:
ON = 50 OHMS
OFF = 10M OHMS

Revision History

Datasheet Revision	*Change from Previous Revision*
D	Speed increased to 18 MSPS, production pinout added, AC and DC characteristics have "tbds" replaced with numbers.
E	Maximum DAC output current changed to 2.5 mA; RSET and DAC output resistors changed to 511 Ω. DAC output compliance changed to –0.2 V to +1.2v.
F	Command bit D0 function inverted.
G	Added *Multiplexer Considerations* to Circuit Description. Revised figures 2, 5, and table 3. Added Multiplexer Compliance (DC) and CEXT AC Amplitude parameters.

reliminary Information

is document contains information on a new product. The parametric information, hough not fully characterized, is the result of testing initial devices.

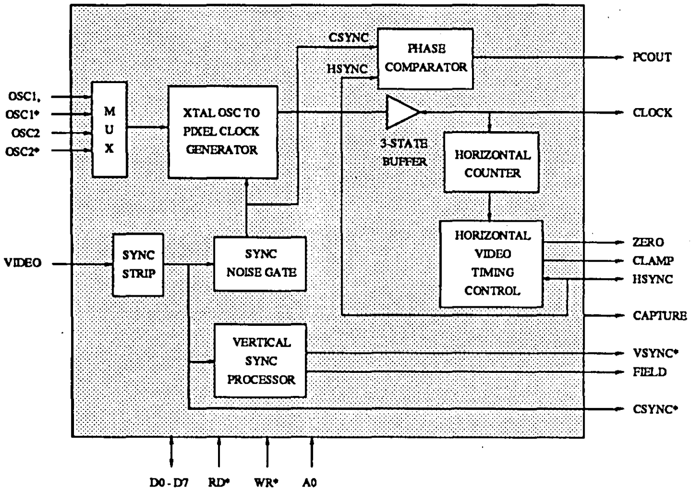
·istinguishing Features

- Programmable 12-Bit Video Timing
- Bidirectional HSYNC and CLOCK Pins
- Horizontal Sync Noise Gating
- External VCO Support
- Standard MPU Interface
- TTL Compatible
- + 5 V Monolithic CMOS
- 28-pin PLCC Package
- Typical Power Dissipation: 300 mW

Applications

- Image Processing
- Video Digitizing
- Desktop Publishing
- Graphic Art Systems

unctional Block Diagram


CSYNC
HSYNC
PHASE COMPARATOR
PCOUT
OSC1
OSC1*
OSC2
OSC2*
M U X
XTAL OSC TO PIXEL CLOCK GENERATOR
3-STATE BUFFER
CLOCK
HORIZONTAL COUNTER
HORIZONTAL VIDEO TIMING CONTROL
ZERO
CLAMP
HSYNC
CAPTURE
VIDEO
SYNC STRIP
SYNC NOISE GATE
VERTICAL SYNC PROCESSOR
VSYNC*
FIELD
CSYNC*
D0 - D7
RD*
WR*
A0

ɔoktree Corporation
50 Barnes Canyon Rd.
ı Diego, CA 92121
9) 452-7580 • (800) VIDEO IC
X: 383 596 • FAX: (619) 452-1249
61001 Rev. E

Bt261

30 MHz Pixel Clock
Monolithic CMOS
HSYNC Line Lock
Controller

Product Description

The Bt261 HSYNC Line Lock Controller is designed specifically for image capture applications.

Either composite video or TTL composite sync information is input via VIDEO. An internal sync separator separates horizontal and vertical sync information. Programmable horizontal and vertical video timing enables recovery of both standard and non-standard timing information.

An external VCO may be used in conjunction with the on-chip phase comparator for implementation of clocks locked to the horizontal frequency.

Alternately, a high speed clock (OSC) may be divided down to generate the pixel clock. The OSC inputs may be configured to be either TTL or ECL compatible. Thus, four TTL clocks, two TTL clocks and one differential ECL clock, or two differential ECL clocks may be used. The ECL clock inputs are designed to be driven by 10KH ECL using a single +5 V supply. The higher the OSC clock rate, the lower the pixel clock jitter.

The CLAMP and ZERO outputs are programmed by the MPU for DC restoration of the video signal and zeroing the Image Digitizer or A/D converter at the appropriate time.

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Circuit Description

MPU Interface

As seen in the functional block diagram, the Bt261 supports a standard MPU interface (D0–D7, RD*, WR*, and A0). MPU operations are asynchronous to the clocks.

A0 is used to select either the internal 5-bit address register (A0 = logical zero) or the control register specified by the address register (A0 = logical one). ADDR5–ADDR7 are ignored during MPU write cycles, and are in an unknown state when read by the MPU. ADDR0 corresponds to D0 and is the least significant bit. ADDR0–ADDR4 increment following any MPU read or write cycle to a control register other than the address register. MPU write cycles to reserved addresses are ignored and MPU read cycles from reserved addresses return invalid data.

Table 1 shows the internal register addressing.

ADDR0 - ADDR4	Addressed by MPU
$00	command register_0
$01	command register_1
$02	command register_2
$03	command register_3
$04	VSYNC sample register
$05	OSC count low register
$06	OSC count high register
$07	status register
$08	HSYNC start low register
$09	HSYNC start high register
$0A	HSYNC stop low register
$0B	HSYNC stop high register
$0C	CLAMP start low register
$0D	CLAMP start high register
$0E	CLAMP stop low register
$0F	CLAMP stop high register
$10	ZERO start low register
$11	ZERO start high register
$12	ZERO stop low register
$13	ZERO stop high register
$14	FIELD gate start low register
$15	FIELD gate start high register
$16	FIELD gate stop low register
$17	FIELD gate stop high register
$18	noise gate start low register
$19	noise gate start high register
$1A	noise gate stop low register
$1B	noise gate stop high register
$1C	HCOUNT start low register
$1D	HCOUNT start high register
$1E	reserved
$1F	reserved

Table 1. Internal Register Addressing.

Video Input / Sync Detector

Either an AC-coupled video signal or a DC-coupled TTL-compatible composite sync signal may be input via the VIDEO input pin (negative going sync polarity).

Command register_0 specifies the threshold above the sync tip to use for sync detection. If the sync tip on VIDEO is below the selected threshold, composite sync information is detected and output onto CSYNC* with no pipeline delay and asynchronous to the pixel clock.

Typically, the VIDEO input will be connected to the TTL-compatible CSYNC* output of the Bt251/253 Image Digitizer, and the highest sync slicing level will be selected.

Horizontal Counter

The rising edge of pixel clock (CLOCK) increments a 12-bit horizontal counter used to generate horizontal video timing information. The value of the counter is compared to various registers to determine when signals are to be asserted and negated. $000 corresponds to the falling edge of CSYNC* with a variable pipeline delay.

Horizontal Sync Separation

The Bt261 separates horizontal sync information from CSYNC* by use of the horizontal noise gate register, which derives gated composite sync by removing equalization and serration pulses at half-line intervals.

Two 12-bit noise gate start and stop registers specify at what horizontal count (with pixel clock resolution) to open and close sync transitions on the VIDEO input to be detected.

Circuit Description (continued)

The sync noise gating is provided to filter incorrect horizontal sync information from noisy video signals. The noise gating also serves a second purpose: to filter serration and equalization pulses at half-line intervals from CSYNC* during the vertical retrace interval. This enables steady synchronization of horizontal sync information during vertical retrace intervals.

HSYNC Input/Output

The HSYNC output may be programmed to be either active high or active low. The beginning of HSYNC (in pixel clock cycles) is determined by the HSYNC start register, and is typically programmed to be coincident with beginning of the noise-gated CSYNC*. The width of the HSYNC output is determined by the HSYNC stop register and is specified in pixel clock cycles.

The HSYNC output may be three-stated via the command register.

HSYNC may also be configured as an input enabling external circuitry to generate HSYNC and drive the phase comparator.

VSYNC Output*

The vertical sync interval is determined by sampling CSYNC* a specified number of pixel clock cycles after the beginning of the recovered composite sync. This interval is specified by the VSYNC sample register.

For each scan line that the sample is a logical zero, the VSYNC* output is a logical zero. Thus, the VSYNC sample register should be programmed so that the sample occurs well after the end of CSYNC*. VSYNC is output on the rising edge of PCLK.

CLAMP and ZERO Outputs

The CLAMP and ZERO outputs are provided to control the clamping and zero timing of the A/D converter or Image Digitizer. The start and stop timing is programmable by the MPU (in pixel clock cycles). ZERO is used to zero the comparators of the A/D converter or Image Digitizer. CLAMP is used to DC-restore the video signal. Both CLAMP and ZERO may be programmed to be either active high or active low.

FIELD Output

The FIELD output is derived from the vertical sync information. By positioning the FIELD gate start/stop values a half-line interval apart, the half-line delay in vertical sync during the second field's vertical interval can provide a signal distinguishing the fields.

The polarity of the FIELD output may be programmed to be either active high (field one = 1, field two = 0) or active low (field one = 0, field two = 1).

When digitizing noninterlaced video signals, the FIELD output will remain a logical one if FIELD is programmed to be active low. FIELD will remain a logical zero if the FIELD output is programmed to be active high.

Figure 1 illustrates the operation of the FIELD gate and FIELD output.

Capture Output

The Bt261 outputs a CAPTURE signal, which is a command register bit (CR05) synchronized to the vertical sync or FIELD signals.

To capture a single frame of video in an interlaced system, the MPU resets the capture bit (CR5) low, then sets it high before the next rising edge of field. At the rising edge of field, the capture output will be set to a logical one until the next rising edge or field (one frame time).

In a non-interlaced system, the MPU resets the capture bit (CR5) low, then sets it high before the falling edge of VSYNC*. When the falling edge of VSYNC* occurs, the capture output will be set high until the next falling edge of VSYNC*.

Circuit Description (continued)

External VCO Pixel Clock Generation

An external VCO or pixel clock may be used to drive the Bt261, as shown in Figure 2. The pixel clock signal (from the VCO if one is used) is connected to the CLOCK pin and any one of the OSC input pins (the one used must be selected by command bits CR00–CR02). Note that the VCO must have positive control voltage (positive voltage forces a higher frequency).

An on-chip phase comparator is available to compare the phase of HSYNC and the falling edge of the noise-gated CSYNC*.

If the falling edge of the noise-gated CSYNC* occurs before the beginning of HSYNC, the phase comparator "dumps" a charge onto an external capacitor, increasing the VCO frequency. If the falling edge of noise-gated CSYNC* occurs after the beginning of HSYNC, the phase comparator "sinks" a charge from the external capacitor, decreasing the VCO frequency.

The output of the phase comparator is PCOUT and it is a TTL-compatible three-statable output. The width of the output pulse on PCOUT is equal to the phase difference with a gain of 4π / VCC.

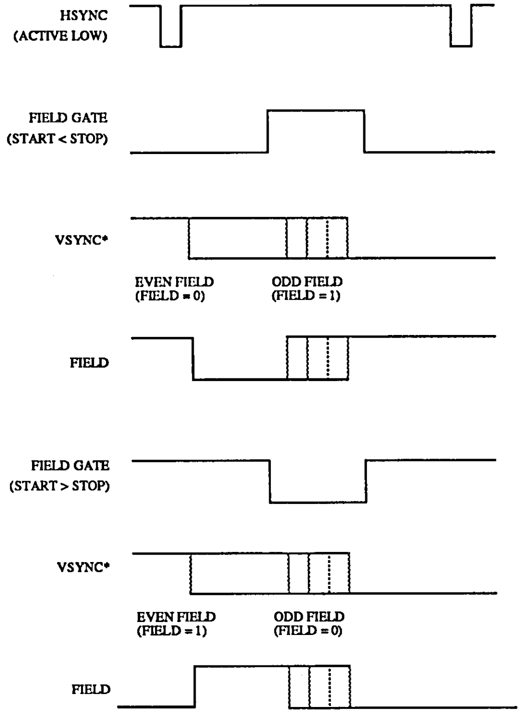

HSYNC
(ACTIVE LOW)
FIELD GATE
(START < STOP)
VSYNC*
EVEN FIELD
(FIELD = 0)
ODD FIELD
(FIELD = 1)
FIELD
FIELD GATE
(START > STOP)
VSYNC*
EVEN FIELD
(FIELD = 1)
ODD FIELD
(FIELD = 0)
FIELD

Figure 1. FIELD Output Operation.

Circuit Description (continued)

The "divide-by-N" for the PLL loop is the 12-bit HCOUNT register. Command register bits CR07 and CR06 must be set to (1,0) for proper operation. This configures the horizontal counter to be reset to zero upon reaching the HCOUNT value.

Phase/Frequency Detector Operation

The phase comparator compares the phase of the falling edge of the noise-gated CSYNC* and generated HSYNC. The HSYNC can be either internally generated (and optionally output onto the HSYNC pin) or an external HSYNC signal can be input via the HSYNC pin.

In the event of a missing horizontal sync (either recovered or generated), the phase comparator can be configured to ignore the missing pulse and to not adjust the frequency of the VCO. This **phase limiting** avoids adjusting the VCO frequency erroneously due to the large phase error that would otherwise occur until the next sync interval. Command bit CR10 enables or disables this capability.

If the falling edge of the noise-gated CSYNC* and generated HSYNC are within the number of pixel clock cycles specified by command bits CR24–CR27 (1 to 16 clock cycles), the Bt261 considers itself locked to the video signal. If the clock cycle condition (as specified by command bits CR24–CR27) is not met, status bit SR00 is set to low to indicate locking to the video signal was lost. If the line count condition (as specified by command bits CR30–CR37) is not met, the phase limiter is disabled.

In the event lock is lost, phase limiting is disabled until lock is re-established. Command bit CR22 may be used to override this feature to tell the phase comparator it is always locked.

Asynchronous (non-line locked) Pixel Clock Generation

Four oscillator clock inputs are provided (OSC), selectable by the MPU, configurable as either TTL or differential ECL inputs (designed to be driven by 10KH ECL using a single +5 V supply).

The selected OSC input is divided down to the desired pixel clock rate and duty cycle. The pixel clock low and high times are programmable by the MPU (as a function of OSC clock cycles) via the OSC count low and high registers. Note that both the rising and falling edge of the OSC inputs are used when specifying the OSC count (for example, values of 2 for the OSC count low and high registers will divide the OSC clock symmetrically by two).

The generated pixel clock is synchronized to the falling edge of the noise-gated CSYNC* each scan line. Each time a horizontal sync is detected on the VIDEO input, the CLOCK output is resynchronized by the OSC clock so that the beginning of a pixel clock cycle and the falling edge of the noise-gated CSYNC*are coincident (see Figure 3) within a period of the OSC input. While there is some sampling jitter on CLOCK associated with the falling edge of CSYNC*, the residual jitter in the remaining line interval is strictly a function of the OSC clock source

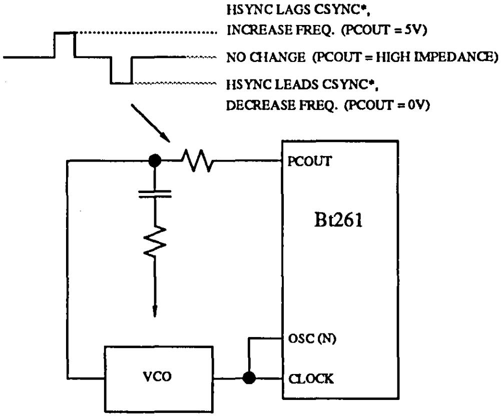

HSYNC LAGS CSYNC*,
INCREASE FREQ. (PCOUT = 5V)
NO CHANGE (PCOUT = HIGH IMPEDANCE)
HSYNC LEADS CSYNC*,
DECREASE FREQ. (PCOUT = 0V)
PCOUT
Bt261
OSC (N)
CLOCK
VCO

Figure 2. External VCO Configuration.

Circuit Description (continued)

jitter, and amplitude/slew rate jitter, at the OSC input. Differential OSC signals of fast edges will minimize the latter contribution.

There are three ways of controlling the horizontal counter, as determined by command bit CR07 and CR06.

CR07 and CR06 are (0,1): if a falling edge of the noise-gated CSYNC* does not occur before the number of pixel clock cycles specified by HCOUNT, the horizontal counter stops at the HCOUNT value and is held there until the next falling edge of the noise-gated CSYNC*, at which time it is reset to zero. CLOCK stops in the high state at the HCOUNT value, until the next falling edge of the noise-gated CSYNC*.

If a falling edge of the noise-gated CSYNC* occurs before the number of pixel clock cycles specified by HCOUNT, the horizontal counter is reset to zero by the falling edge of the noise-gated CSYNC*. CLOCK will be continuous and is resynchronized to each falling edge of the noise-gated CSYNC*. This mode is used if the number of pixel clock cycles per scan line is known and is a fixed number.

CR07 and CR06 are (1,1): if a falling edge of the noise-gated CSYNC* does not occur before the number of pixel clock cycles specified by HCOUNT, the horizontal counter is reset to zero upon reaching HCOUNT, and begins incrementing again, until the next falling edge of the noise-gated CSYNC* or HCOUNT value is reached. CLOCK is continuous and is resynchronized to each falling edge of the noise-gated CSYNC*.

If a falling edge of the noise-gated CSYNC* occurs before the number of pixel clock cycles specified by HCOUNT, the horizontal counter is cleared at the falling edge of the noise-gated CSYNC*, and begins incrementing again, until the next falling edge of the noise-gated CSYNC* or HCOUNT value is reached. CLOCK will be continuous and is resynchronized to the falling edge of the noise-gated CSYNC*. This mode is used if the number of pixel clock cycles per scan line is not known or an arbitrary value is to be used.

CR07 and CR06 are (1,0): Resets H counter at HCOUNT only.

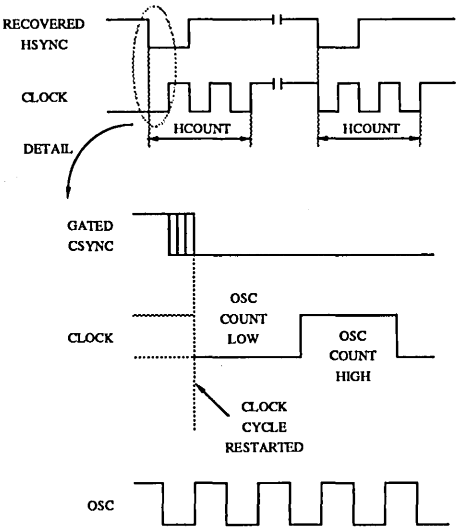


Figure 3. Pixel Clock Output Timing (Crystal-Based Clock).

Internal Registers

Horizontal Counter

The 12-bit horizontal counter is incremented on the rising edge of CLOCK. It is not accessible by the MPU.

Command Register_0

This command register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to D0 and is the least significant bit.

CR07, CR06	Horizontal counter control (00) reserved (01) reset each recovered HSYNC (10) reset to zero upon reaching HCOUNT (11) use both modes (01) and (10)	A value of (01) or (11) forces the horizontal counter to be reset to zero at the beginning of every recovered horizontal sync. These modes (typically mode 01) should be selected when using crystal-based pixel clock generation. A value of (10) specifies that the horizontal counter will be reset to zero upon reaching the HCOUNT value. This mode should be selected when using the horizontal counter as a simple divide-by-N circuit (such as when using an external VCO).
CR05	Capture strobe	This bit is synchronized to VSYNC* and FIELD and output onto the CAPTURE output pin.
CR04, CR03	Sync detect select (00) 25 mV (01) 50 mV (10) 100 mV (11) 125 mV	These bits specify how much above the sync tip to slice VIDEO for sync detection. If inputting TTL sync information, the highest slicing level should be selected.
CR02–CR00	Clock input select (000) TTL compatible OSC1 (001) TTL compatible OSC1* (010) TTL compatible OSC2 (011) TTL compatible OSC2* (100) ECL compatible OSC1, OSC1* (101) ECL compatible OSC2, OSC2* (110) reserved (111) reserved	These bits specify which OSC input is to be used to generate pixel clock information. ECL input selection is compatible with 10KH differential ECL driven by a single +5 V supply.

Internal Registers (continued)

Command Register_1

This command register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to D0 and is the least significant bit.

CR17	Interlaced or noninterlaced select (0) noninterlaced operation (1) interlaced operation	This bit specifies whether an interlaced or noninterlaced video signal is being digitized. The MPU must write a logical zero followed by a logical one to this bit to reset the status bit (SR00) to a logical one.
CR16	CLOCK output disable (0) drive CLOCK output (1) three-state CLOCK output	This bit specifies whether the CLOCK pin is three-stated (logical one) or is actively driven (logical zero). A logical one enables an external pixel clock to drive the internal counters, ignoring the OSC inputs and pixel clock generator.
CR15	CSYNC* output disable (0) drive CSYNC* output (1) three-state CSYNC* output	This bit specifies whether the CSYNC* output is three-stated (logical one) or is actively driven (logical zero).
CR14	VSYNC* output disable (0) drive VSYNC* output (1) three-state VSYNC* output	This bit specifies whether the VSYNC* output is three-stated (logical one) or is actively driven (logical zero).
CR13	HSYNC output disable (0) drive HSYNC output (1) three-state HSYNC output	This bit specifies whether the HSYNC output is three-stated (logical one) or is actively driven with the internally generated HSYNC signal (logical zero). If external circuitry is driving the HSYNC pin, this bit must be set to a logical one.

Internal Registers (continued)

Command Register_1 (continued)

CR12	Reset lock loss status bits (0) reset status bits (1) inactive	This bit resets the status bits indicating loss of lock. The MPU must write a logical zero to this bit to clear the status bits (SR05 and SR00) to a logical zero.
CR11	Phase comparator input select (0) HSYNC pin (1) internally generated HSYNC	One input to the phase comparator is recovered composite sync. The other input to the phase comparator is specified by this bit to be either the internally generated HSYNC or the HSYNC pin. When an external source is driving the HSYNC pin, this bit should be set to a logical zero.
CR10	Phase limit enable (0) inhibit phase limiting (1) enable phase limiting	If this bit is a logical one, both horizontal sync signals (recovered and either internally or externally generated) must be present to adjust the VCO frequency. If one is missing, the VCO frequency is not adjusted. If this bit is a logical zero, a missing horizontal sync signal will adjust the VCO frequency.

Internal Registers (continued)

Command Register_2

This command register may be written to or read by the MPU at any time and is not initialized. CR20 corresponds to D0 and is the least significant bit.

CR27–CR24	Phase lock pixel count (0001) 2 clock cycles : (1111) 16 clock cycles	These bits specify the maximum number of pixel clock cycles between the falling edge of noise-gated CSYNC* and the HSYNC signal (either internally or externally generated) to be considered locked. If the number of pixel clock cycles between the falling edge of noise-gated CSYNC* and the HSYNC signal exceed this value, lock is considered to be lost for that scan line, and the lock loss status bit (SR00) is set to a logical zero.
CR23	Pixel clock mask enable (0) continuous pixel clock (1) stop pixel clock at HCOUNT	If this bit is a logical one, the CLOCK output is stopped in the logical one state when the horizontal counter reaches the HCOUNT value. This ensures a minimum pulse width when the noise-gated CSYNC* signal is asynchronously sampled. If it is a logical zero, the CLOCK output will continuously clock (if command bit CR16 is a logical zero). This bit is ignored if an external pixel clock is driving the CLOCK pin (command bit CR16 is a logical one).
CR22	Lock override (1) normal operation (0) tell phase comparator it's locked	If the Bt261 goes out of lock, the phase limiter is automatically disabled until it is back in lock. If this bit is a logical zero, this function is overridden.
CR21, CR20	Pixel clock select (00) OSC inputs (01) external pixel clock (10) OSC drives CLOCK direct (11) reserved	These bits specify whether to use the OSC-generated pixel clock or an external pixel clock (driving the CLOCK pin) to clock internal counters. In mode (00), the selected OSC input(s) is divided down by the OSC count registers to generate the pixel clock (CLOCK). If mode (01) is selected, an external pixel clock must drive the CLOCK pin and one of the OSC inputs. Command bit CR16 must be a logical one. If mode (10) is selected, the OSC clock is output directly onto the CLOCK pin. The OSC count low and high registers are ignored.

Internal Registers (continued)

Command Register_3

This command register may be written to or read by the MPU at any time and is not initialized. CR30 corresponds to D0 and is the least significant bit.

CR37–CR30	Phase lock line count (0000 0000) 1 scan line (0000 0001) 2 scan lines : (1111 1111) 256 scan lines	These bits specify the number of consecutive scan lines for which lock must be maintained. If lock is not maintained for the specified number of scan lines, the phase limiter is disabled only if command bit CR22 is a logical one.

VSYNC Sample Register

This 8-bit register specifies the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to sample the CSYNC* signal each scan line. This register may be written to or read by the MPU at any time and is not initialized. Values from $00 (1) to $FF (256) may be specified. A value of [1/4 HCOUNT] is recommended (greater than the maximum horizontal sync pulse width of about 5 μS). For a conventional video input with negative-going syncs, this produces a negative-going VSYNC* at the number of clock cycles specified after the falling CSYNC* edge with some pipeline delay.

OSC Count Low and High Registers

These two 4-bit registers specify the number of rising and falling edges of an OSC input the pixel clock output (CLOCK) is to be low and high. Values from $02 (2) to $0E (15) may be specified. These registers may be written to or read by the MPU at any time and are not initialized. A value of $00 results in no pixel clock generation while the OSC inputs are used. Note that the counters clock on both the rising and falling edge of the selected OSC input.

Status Register

This status register may be read by the MPU at any time and is not initialized. MPU write cycles to this register are ignored. SR00 corresponds to D0 and is the least significant bit.

SR00	Lock loss status (pixel count related) (0) lock loss detected (1) reset or no lock loss	This bit is reset if loss of lock occurred for a period defined by CR24–CR27. It is reset by writing to command bit CR12.

Internal Registers (continued)

HSYNC Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to assert or negate the HSYNC output. The [start value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that the HSYNC output is set high. The [stop value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that the HSYNC output is set low. If [start value] = [stop value], HSYNC will remain a constant logical zero. Values from $0000 (1) to $0FFF (4096) may be specified. Note that there is a variable pipeline delay between the CSYNC* and HSYNC outputs.

D4–D7 of HSYNC start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit HSYNC start register is not updated until the write cycle to the HSYNC start high register. Thus, the writing sequence should be [HSYNC start low] [HSYNC start high].

D4–D7 of HSYNC stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit HSYNC stop register is not updated until the write cycle to the HSYNC stop high register. Thus, the writing sequence should be [HSYNC stop low] [HSYNC stop high].

	HSYNC Start/Stop High				HSYNC Start/Stop Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

CLAMP Start and Stop Registers

These two 16-bit registers specify the horizontal count (in pixel clocks) at which to assert and negate the CLAMP output. The [start value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that CLAMP is set high. The [stop value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that CLAMP is set low. If [start value] = [stop value], CLAMP will remain a constant logical zero. Values from $0000 (1) to $0FFF (4096) may be specified. Note that there is a variable pipeline delay between the CSYNC* and CLAMP outputs.

D4–D7 of CLAMP start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit CLAMP start register is not updated until the write cycle to the CLAMP start high register. Thus, the writing sequence should be [clamp start low] [clamp start high].

D4–D7 of CLAMP stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit CLAMP stop register is not updated until the write cycle to the CLAMP stop high register. Thus, the writing sequence should be [clamp stop low] [clamp stop high].

	CLAMP Start/Stop High				CLAMP Start/Stop Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

A value corresponding to 1 µS after the falling edge of CSYNC* is recommended for the [start] value, and a value of 1 µS before the rising edge of CSYNC* is recommended for the [stop] value if DC restoration is to occur during the horizontal sync interval. If DC restoration is to occur during the back porch interval, a value corresponding to 500 ns after the rising edge of CSYNC* is recommended for the [start] value and a value corresponding to 2.5 µS after the rising edge of CSYNC* is recommended for the [stop] value.

Internal Registers (continued)

ZERO Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to assert or negate the ZERO output. The [start value] sets this output high at the specified number of CLOCK cycles following the falling edge of noise-gated CSYNC*. The [stopvalue] sets this output low at the specified number of CLOCK cycles following the falling edge of noise-gated CSYNC*. If [start value] = [stop value], ZERO will remain a constant logical zero. Values from $0000 (1) to $0FFF (4096) may be specified. Note that there is a variable pipeline delay between the CSYNC* and ZERO outputs.

D4–D7 of ZERO start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit ZERO start register is not updated until the write cycle to the ZERO start high register. Thus, the writing sequence should be [zero start low] [zero start high].

D4–D7 of ZERO stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit ZERO stop register is not updated until the write cycle to the ZERO stop high register. Thus, the writing sequence should be [zero stop low] [zero stop high].

	ZERO Start/Stop High				ZERO Start/Stop Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

Since an active high signal is need for the Bt208, Bt251, and Bt253 during non-acquisition intervals, the ZERO output can be programmed to be within the horizontal retrace interval.

Internal Registers (continued)

FIELD Gate Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to start and stop the FIELD gate "window." With the noise gate properly programmed to ignore half-line vertical interval pulses, the VSYNC* transition will occur half a line later during the vertical sync interval between fields one and two (assuming a typical 2:1 interlaced video signal). By programming the FIELD start and stop values to have an interval exceeding half a line (e.g. starting at 1/4 line time and stopping at 3/4 line time) the FIELD output is high during field one if [start value] < [stop value] or low during field one if [start value] > [stop value], with transitions at every falling edge of VSYNC*. If [start value] = [stop value], FIELD will remain a constant logical zero. Values from $0000 (1) to $0FFF (4096) may be specified. Field edge coincides with VSYNC* falling edge.

D4–D7 of FIELD gate start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit FIELD gate start register is not updated until the write cycle to the FIELD gate start high register. Thus, the writing sequence should be [field gate start low] [field gate start high].

D4–D7 of FIELD gate stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit FIELD gate stop register is not updated until the write cycle to the FIELD gate stop high register. Thus, the writing sequence should be [field gate stop low] [field gate stop high].

	FIELD Gate Start/Stop High				FIELD Gate Start/Stop Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

A difference between [start] and [stop] greater than [HCOUNT/2] is recommended, resulting in an active high FIELD output (field one = 1, field two = 0).

Internal Registers (continued)

Noise Gate Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to force the Noise Gate to be closed (start value) or open (stop value). If [start value] = [stop value], the Noise Gate will remain open. Values from $0000 (1) to $0FFF (4096) may be specified.

D4–D7 of Noise Gate start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit Noise Gate start register is not updated until the write cycle to the Noise Gate start high register. Thus, the writing sequence should be [Noise Gate start low] [Noise Gate start high].

D4–D7 of Noise Gate stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit Noise Gate stop register is not updated until the write cycle to the Noise Gate stop high register. Thus, the writing sequence should be [Noise Gate stop low] [Noise Gate stop high].

	Noise Gate Start/Stop High				Noise Gate Start/Stop Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

A value corresponding to [HCOUNT/2 – 2.5 µS] is recommended for the [start] value and a value of [> HCOUNT/2] is recommended for the [stop] value to remove typical equalization and serration pulses. This register should be initialized early to minimize indeterminate outputs during vertical retrace.

HCOUNT Register

This 16-bit register specifies the maximum number of pixel clocks to generate per horizontal line.

The HCOUNT low and high registers are cascaded to form a 16-bit HCOUNT register. D4–D7 of HCOUNT high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit HCOUNT register is not updated until the write cycle to the HCOUNT high register. Thus, the writing sequence should be [HCOUNT low] [HCOUNT high]. Values from $0000 (1) to $0FFF (4096) may be specified. This register should be written first during initialization to minimize indeterminate output activity.

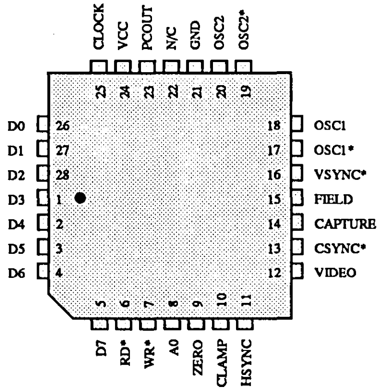
	HCOUNT High				HCOUNT Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

Pin Descriptions

Pin Name	Description
HSYNC	Horizontal sync input/output (TTL compatible). As an output, HSYNC is programmed to be either a logical zero or logical one during the desired horizontal sync interval. It is output following the rising edge of CLOCK. As an input, it is input into the phase comparator asynchronously to the clocks with no pipeline delays.
VSYNC*	Vertical sync output (TTL compatible) with a negative composite sync output. VSYNC* is a logical zero for scan lines during detected vertical sync intervals on the VIDEO input. It is output following the rising edge of CLOCK.
CSYNC*	Composite sync output (TTL compatible). CSYNC* is a logical zero during negative composite sync intervals detected on the VIDEO input. It is output asynchronous to the clocks with no pipeline delays.
ZERO	Zero output (TTL compatible). This output is used to control the ZERO input of the Image Digitizer or A/D converter. It may be programmed to be either active high or active low and is output following the rising edge of CLOCK.
CLAMP	Clamp output (TTL compatible). This output is used to control the CLAMP input of the Image Digitizer or A/D converter. It may be programmed to be either active high or active low and is output following the rising edge of CLOCK.
FIELD	Even/odd field output (TTL compatible). For interlaced operation, this output (with transitions coincident with the VSYNC* output) indicates whether the current field is even or odd; the polarity is programmable. For noninterlaced operation, this output is always either a logical one or a logical zero, depending on whether it is programmed to be active high or low. It is output on the falling edge of VSYNC*.
PCOUT	Phase comparator output (TTL compatible). This three-state output indicates the phase difference in time between the generated horizontal sync signal (either the internally generated HSYNC or the HSYNC pin) and the recovered horizontal sync signal. High = lags, Low = leads.
VIDEO	Video and composite sync input. Either a DC-coupled TTL composite sync information or an AC-coupled analog video signal (less than 2v peak-to-peak) may be input via this pin for detection of sync information. Sync information must be of negative polarity.
CLOCK	Pixel clock input/output (TTL compatible). The device may either drive this pin with a generated clock or an external pixel clock may drive this pin.
OSC1, OSC1*, OSC2, OSC2*	External clock inputs (TTL or ECL compatible). These inputs are programmed to be either TTL or ECL compatible (10KH differential ECL driven by a single +5 V supply).
CAPTURE	Active video output (TTL compatible). This output is active high for a frame duration and is synchronized to the vertical sync interval and FIELD signal. It is output following the rising edge of FIELD for interlaced, or the falling edge of VSYNC* if non-interlaced.
RD*	Read control input (TTL compatible). If RD* is a logical zero, data is output onto D0–D7. RD* and WR* should not be asserted simultaneously.
WR*	Write control input (TTL compatible). If WR* is a logical zero, data is written into the device via D0–D7. Data is latched on the rising edge of WR*. RD* and WR* should not be asserted simultaneously.
D0–D7	Bidirectional data bus (TTL compatible). MPU data is transferred into and out of the device over this 8-bit data bus. If RD* is a logical one, D0–D7 are three-stated.

Pin Descriptions (continued)

Pin Name	Description
A0	Address control inputs (TTL compatible). A0 specifies whether the MPU is accessing the address register (A0 = 0) or the control register specified by the address register (A0 = 1).
VCC	Power.
GND	Ground.


CLOCK
VCC
PCOUT
N/C
GND
OSC2
OSC2*
25
24
23
22
21
20
19
D0 26
D1 27
D2 28
D3 1
D4 2
D5 3
D6 4
18 OSC1
17 OSC1*
16 VSYNC*
15 FIELD
14 CAPTURE
13 CSYNC*
12 VIDEO
5
6
7
8
9
10
11
D7
RD*
WR*
A0
ZERO
CLAMP
HSYNC

Application Information

Interfacing to the Bt208

Figure 4 illustrates interfacing the Bt261 to the Bt208 Flash A/D Converter. The VIDEO input of the Bt261 connects to the VIN input of the Bt208 through a 0.1 µF ceramic capacitor. The sync slicing level of the Bt261 should be selected for optimum performance.

The Bt261 provides the ZERO and CLAMP signals required by the Bt208, in addition to the CLOCK.

The HSYNC, VSYNC*, FIELD, and CAPTURE signals of the Bt261 interface to the video timing controller and video DRAM controller.

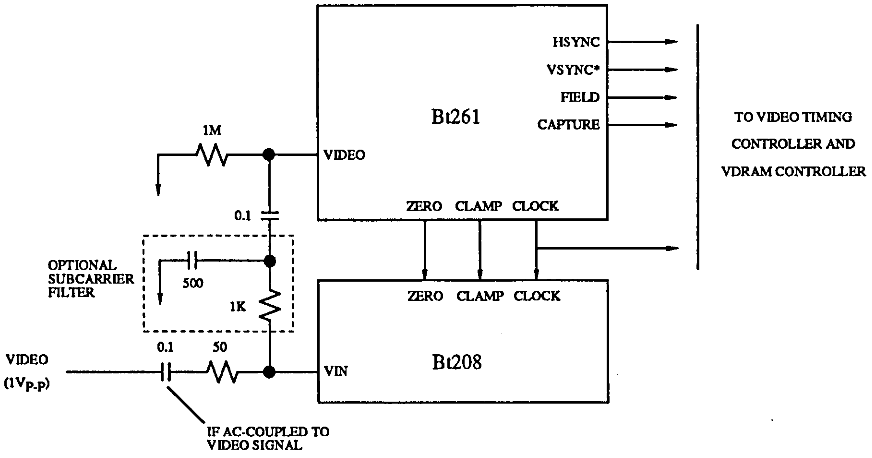

Bt261
HSYNC
VSYNC*
FIELD
CAPTURE
VIDEO
ZERO CLAMP CLOCK
TO VIDEO TIMING
CONTROLLER AND
VDRAM CONTROLLER
1M
0.1
OPTIONAL
SUBCARRIER
FILTER
500
1K
0.1
50
VIDEO
(1VP-P)
ZERO CLAMP CLOCK
Bt208
VIN
IF AC-COUPLED TO
VIDEO SIGNAL

Figure 4. Interfacing to the Bt208.

Application Information (continued)

Interfacing to the Bt251

Figure 5 illustrates interfacing the Bt261 to the Bt251 Image Digitizer. The VIDEO input of the Bt261 connects directly to the CSYNC* output of the Bt251. As CSYNC* is a TTL-compatible output, the highest sync slicing level should be selected on the Bt261.

The Bt261 provides the ZERO and CLAMP signals required by the Bt251, in addition to the CLOCK.

The HSYNC, VSYNC*, FIELD, and CAPTURE signals of the Bt261 interface to the video timing controller and video DRAM controller.

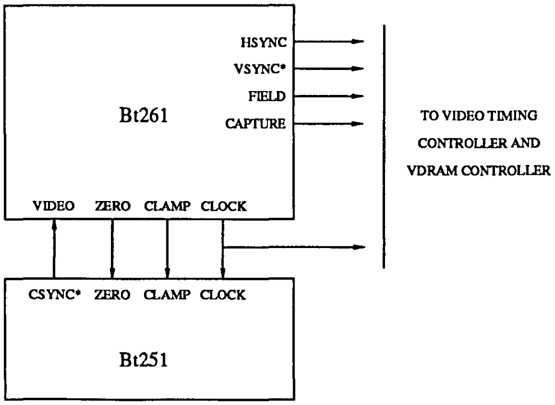

HSYNC
VSYNC*
FIELD
Bt261
CAPTURE
TO VIDEO TIMING CONTROLLER AND VDRAM CONTROLLER
VIDEO
ZERO
CLAMP
CLOCK
CSYNC*
ZERO
CLAMP
CLOCK
Bt251

Figure 5. Interfacing to the Bt251.

Application Information (continued)

Interfacing to the Bt253

Figure 6 illustrates interfacing the Bt261 to the Bt253 Image Digitizer. The VIDEO input of the Bt261 connects directly to the CSYNC* output of the Bt253. As CSYNC* is a TTL-compatible output, the highest sync slicing level should be selected on the Bt261.

The Bt261 provides the ZERO and CLAMP signals required by the Bt253, in addition to the (R,G,B) CLOCK inputs of the Bt253.

The HSYNC, VSYNC*, FIELD, and CAPTURE signals of the Bt261 interface to the video timing controller and video DRAM controller.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

Latchup can be prevented by assuring that all VCC pins are at the same potential and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

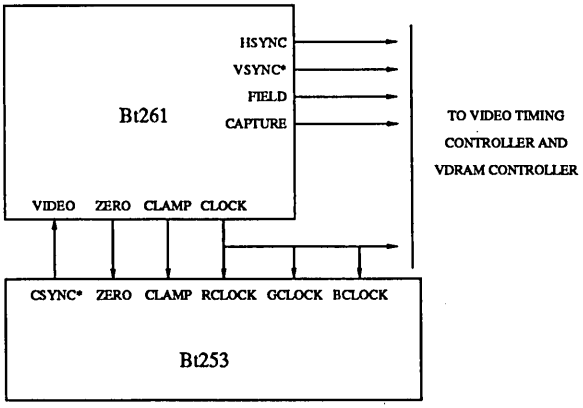

HSYNC
VSYNC*
FIELD
CAPTURE
Bt261
VIDEO
ZERO
CLAMP
CLOCK
TO VIDEO TIMING
CONTROLLER AND
VDRAM CONTROLLER
CSYNC*
ZERO
CLAMP
RCLOCK
GCLOCK
BCLOCK
Bt253

Figure 6. Interfacing to the Bt253.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Video Input					
DC-coupled				5	Volts
AC-coupled*		0.2		2	Volts_{pp}

* Video input DC quiesent about (VCC/2) volts.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	Volts
Voltage on any Signal Pin*		GND–0.5		VCC + 0.5	Volts
Ambient Operating Temperature	TA	–55		+ 125	°C
Storage Temperature	TS	–65		+ 150	°C
Junction Temperature	TJ			+ 150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL Digital Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance	CIN				pF
(f = 1 MHz, Vin = 2.4v)			7		
OSC Digital Inputs					
TTL Mode					
Input High Voltage	VIH	2.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance	CIN		7		pF
(f = 1 MHz, Vin = 2.4 V)					
ECL Mode					
Input High Voltage	VIH	VCC–1.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		VCC–1.6	Volts
Input High Current (Vin = 4.0 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance	CIN		7		pF
(f = 1 MHz, Vin = 2.4v)					
D0 - D7 Digital Outputs					
Output High Voltage	VOH	2.4			Volts
(IOH = –400 µA)					
Output Low Voltage	VOL			0.4	Volts
(IOL = 6.4 mA)					
3-state Current	IOZ			50	µA
Output Capacitance	COUT		20		pF
PCOUT Output					
Output High Voltage	VOH			100	Ω
(IOH = –400 µA)					
Output Low Voltage	VOL			75	Ω
(IOL = 3.2 mA)					
3-state Current	IOZ			50	µA
Output Capacitance	COUT		20		pF
Other Digital Outputs					
Output High Voltage	VOH	2.4			Volts
(IOH = –400 µA)					
Output Low Voltage	VOL			0.4	Volts
(IOL = 3.2 mA)					
3-State Current	IOZ			50	µA
Output Capacitance	COUT		20		pF

Test conditions (unless otherwise specified): "Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

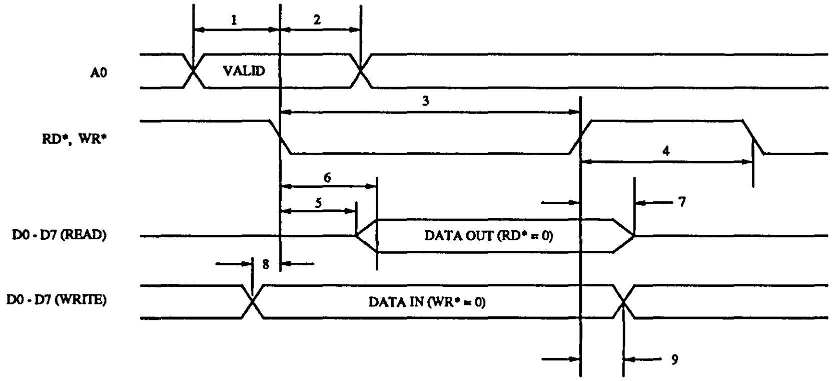
AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
OSC Cycle Time	OSCmax	10			ns
CLOCK Cycle Time*	Fmax	33.33			ns
A0 Setup Time	1	10			ns
A0 Hold Time	2	10			ns
RD*/WR* Low Time	3	50			ns
RD*/WR* High Time	4	50			ns
RD* Asserted to Data Bus Driven	5	5			ns
RD* Asserted to Data Valid	6			40	ns
RD* Negated to Data Bus 3-Stated	7			20	ns
Write Data Setup Time	8	10			ns
Write Data Hold Time	9	10			ns
OSC High Time	10	3.5			ns
OSC Low Time	11	3.5			ns
CLOCK Low Time	12	tbd		tbd	ns
CLOCK High Time	13	tbd		tbd	ns
OSC to CLOCK Output Delay Pipelines	14			tbd	ns
VIDEO to CSYNC* Output Delay	15			tbd	ns
HSYNC, ZERO, CLAMP Output Delay	16			tbd	ns
VSYNC*, FIELD Output Delay Pipelines	17			tbd	ns
PCOUT Output Delay	18			tbd	ns
Minimum Compare Differential	19		5	tbd	ns
VCC Supply Current**	ICC		60	tbd	mA

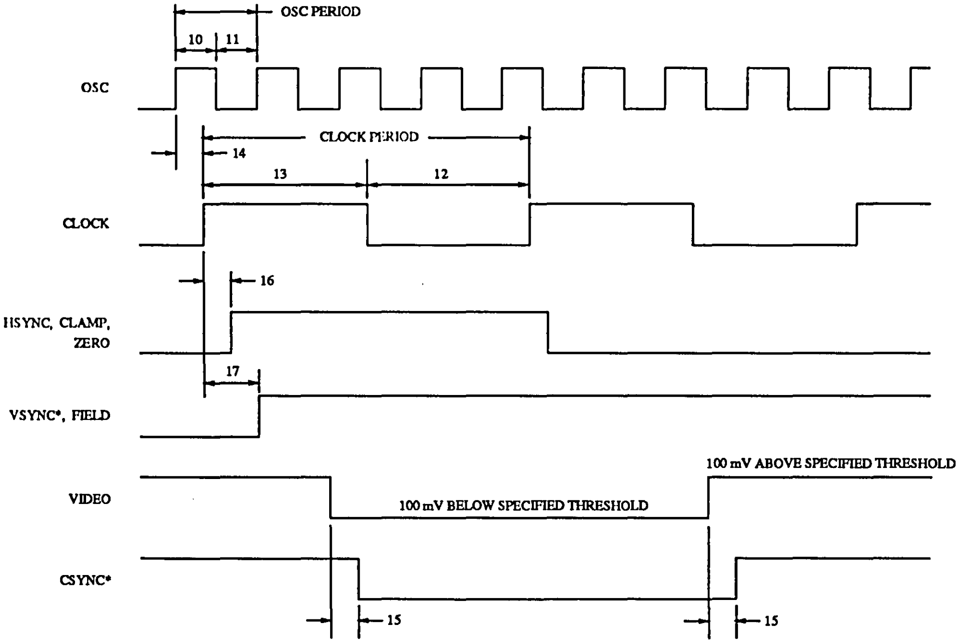
Test conditions (unless otherwise specified): "Recommended Operating Conditions". TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. CLOCK, HSYNC, CLAMP, ZERO, VSYNC*, FIELD, CAPTURE, and CSYNC* output load ≤ 50 pF, D0–D7 output load ≤ 130 pF. Typical values are based on nominal temperature, i.e., and nominal voltage, i.e., 5 V.

*Maximum load of 20 pf.
**At Fmax. ICC (typ) at VCC = 5.0 V. ICC (max) at VCC = 5.25 V. OSC/PCLOCK = 2, CLOCK/HSYNC ≥100.

Timing Waveforms

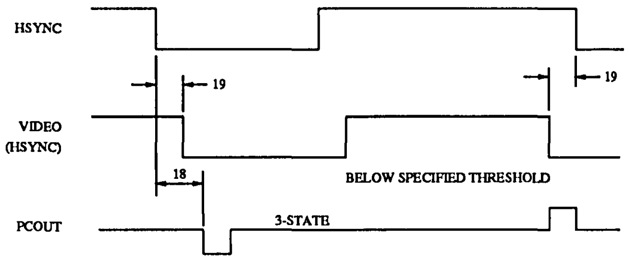

1
2
A0
VALID
3
RD*, WR*
4
6
5
7
D0 - D7 (READ)
DATA OUT (RD* = 0)
8
D0 - D7 (WRITE)
DATA IN (WR* = 0)
9

MPU Read/Write Timing.


OSC PERIOD
10
11
OSC
CLOCK PERIOD
14
13
12
CLOCK
16
HSYNC, CLAMP, ZERO
17
VSYNC*, FIELD
100 mV ABOVE SPECIFIED THRESHOLD
VIDEO
100 mV BELOW SPECIFIED THRESHOLD
CSYNC*
15
15

Video Input/Output Timing.

Timing Waveforms (continued)


HSYNC
19
19
VIDEO
(HSYNC)
18
BELOW SPECIFIED THRESHOLD
PCOUT
3-STATE

Video Input/Output Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt261KPJ	28-pin Plastic J-Lead	0° to +70° C

reliminary Information

is document contains information on a new product. The parametric information, though not fully characterized, is the result of testing initial devices.

Bt281

36 MHz Programmable Color Space Converter and Color Corrector

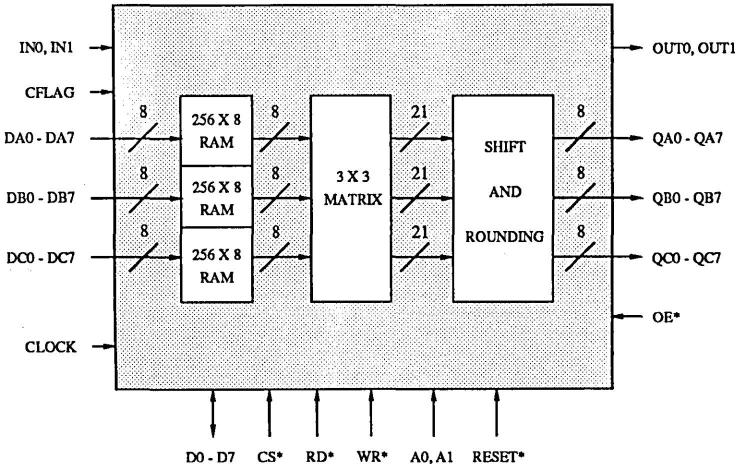
istinguishing Features

- Real-Time Color Space Conversion
- Pseudo-Color Mode
- Programmable Matrix Coefficients
- Three 256 x 8 Input Lookup Table RAMs
- Standard MPU Interface
- TTL Compatible
- +5 V Monolithic CMOS
- 84-pin PLCC Package
- Typical Power Dissipation: 1.1 W

Applications

- Image Processing
- Image Capture
- Color Correction

unctional Block Diagram



Product Description

The Bt281 Color Space Converter is designed specifically for image capture and processing applications. It provides real-time conversion of the color space during the image capture process or during the CRT display process. Thus, the color space of the frame buffer may be optimized for image processing applications regardless of the type of video signal being digitized or the requirement that RGB information be generated to drive the CRT.

Twenty-four bits of color information are input via the DAx, DBx, and DCx inputs, converted to a new color space by the 3 x 3 matrix multiplier, and output onto QAx, QBx, and QCx.

Three independent 256 x 8 input lookup tables enable the addition or removal of gamma correction or gain control prior to converting to another color space.

The QAx, QBx, and QCx outputs may be three-stated asynchronously to CLOCK via the OE* control input.

Two sets of matching delay lines are included to maintain synchronization of control signals.

rooktree Corporation
950 Barnes Canyon Rd.
an Diego, CA 92121
619) 452-7580 • (800) VIDEO IC
LX: 383 596 • FAX: (619) 452-1249
L281001 Rev. F

Brooktree®

Circuit Description

MPU Interface

As seen in the functional block diagram and in Figure 1, the Bt281 supports a standard MPU interface (D0–D7, CS*, RD*, WR*, A0, and A1). MPU operations are asynchronous to clock.

A0 and A1 are used to select address register, RAM location, or control register specified by the address register, as shown in Table 1. The 11-bit address register specifies which control register or RAM location the MPU is accessing, as shown in Table 1. The address register resets to $000 following a read or write cycle to location $7FF. Write cycles to reserved addresses are ignored, and read cycles from reserved addresses return invalid data. ADDR11–ADDR15 are always a logical zero.

The address register increments after each MPU read or write cycle and is not initialized. ADDR0 and ADDR8 correspond to data bus bit D0, with ADDR0 being the least significant bit. The address register is not initialized following a reset or power-up condition.

The lookup table RAMs are not dual-ported, so MPU accesses have priority over pixel accessing. During MPU access to the color palette RAMs, the QAx, QBx, and QCx outputs are undefined and invalid. Thus, lookup table updates should occur only during blanking intervals.

Matrix Multiplier

DA0–DA7, DB0–DB7, and DC0–DC7 are latched on the rising edge of CLOCK and address the three color lookup table RAMs. The outputs of the RAMs are input to the 3 x 3 matrix multiplier.

The 3 x 3 matrix multiplier performs the fundamental color space conversion, as follows:

$$\begin{bmatrix} QA \\ QB \\ QC \end{bmatrix} = \begin{bmatrix} m1 & m2 & m3 \\ m4 & m5 & m6 \\ m7 & m8 & m9 \end{bmatrix} \begin{bmatrix} DA \\ DB \\ DC \end{bmatrix}$$

m1–m9 are loaded by the MPU to perform the color space conversion desired. The values of m1–m9 are programmable over the range of –4.000 to +3.996 using 2's complement notation.

The 3 x 3 matrix multiplier generates three 21-bit (including sign) values (one for each of the three channels). As only 8 bits per channel may be output, command bits CR17–CR15 are used to select which 8 bits (or 7 bits + sign) of these 21 bits are output, as shown in Table 2.

The fractional data indicated in Table 2 is used to round to 8 bits as follows: round up if the fractional data = 0.5 and the rounded result will be an even number (LSB = 0) or if the fractional data is > 0.5. If the fractional data is < 0.5, the number will be rounded down. Circuitry is included to avoid wrapping around on overflow or underflow conditions; rather the data is saturated at the minimum and maximum allowable values.

QA0–QA7, QB0–QB7, and QC0–QC7 are output following the rising edge of CLOCK.

The QAx, QBx, and QCx outputs may be three-stated asynchronously to the output clock via the OE* control input and command bit CR10.

Bypassing

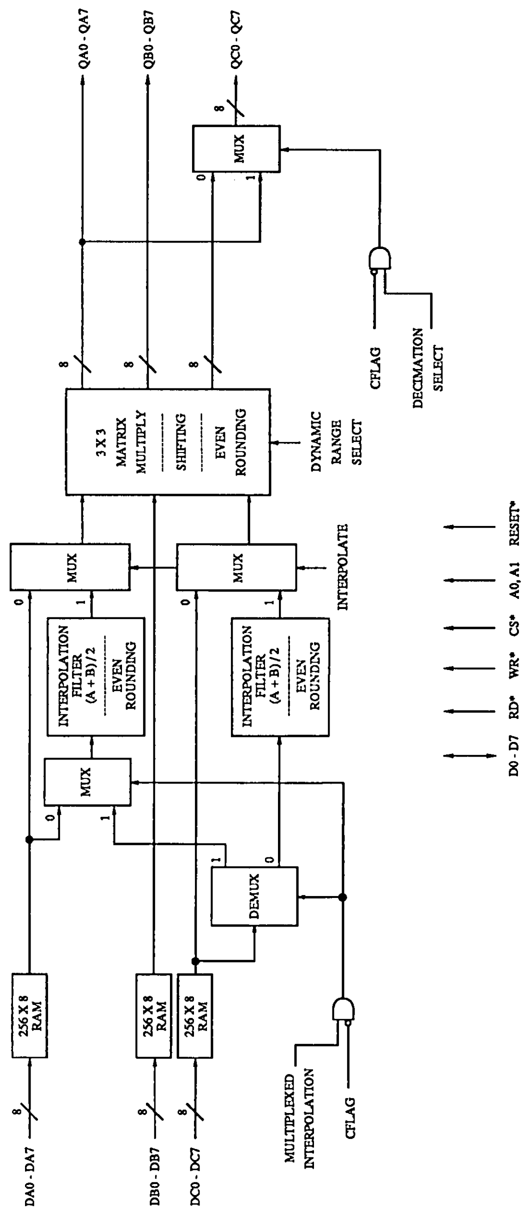
The Bt281 may be entirely bypassed with no change in the pipeline delay via the command register. Following a reset condition, the Bt281 is initialized to be in the bypass mode. (See Figure 8.)

I/O Delay Lines

The IN0 and IN1 inputs are latched on the rising edge of CLOCK, pipelined to maintain synchronization with the color data, and output onto OUT0 and OUT1.

The delay lines may be used for control signals, such as sync, blank, etc., that should have the same pipeline delay as the pixel data.

Circuit Description (continued)



DA0 - DA7
DB0 - DB7
DC0 - DC7
8
256 X 8 RAM
MUX
DEMUX
0
1
INTERPOLATION FILTER (A + B) / 2
EVEN ROUNDING
INTERPOLATE
3 X 3 MATRIX MULTIPLY
SHIFTING
EVEN ROUNDING
DYNAMIC RANGE SELECT
MULTIPLEXED INTERPOLATION
CFLAG
DECIMATION SELECT
QA0 - QA7
QB0 - QB7
QC0 - QC7
D0 - D7
RD*
WR*
CS*
A0, A1
RESET*

Figure 1. Detailed Block Diagram.

Circuit Description (continued)

A1, A0	ADDR0–ADDR10	Accessed by MPU
00	$xxx	address register low (ADDR0–ADDR7)
01	$xxx	address register high (ADDR8–ADDR10)
10	$000	DA RAM location $00
10	$001	DA RAM location $01
:	:	:
10	$0FF	DA RAM location $FF
10	$100	DB RAM location $00
10	$101	DB RAM location $01
:	:	:
10	$1FF	DB RAM location $FF
10	$200	DC RAM location $00
10	$201	DC RAM location $01
:	:	:
10	$2FF	DC RAM location $FF
10	$300	m1 register low
10	$301	m1 register high
10	$302	m2 register low
10	$303	m2 register high
10	$304	m3 register low
10	$305	m3 register high
10	$306	m4 register low
10	$307	m4 register high
10	$308	m5 register low
10	$309	m5 register high
10	$30A	m6 register low
10	$30B	m6 register high
10	$30C	m7 register low
10	$30D	m7 register high
10	$30E	m8 register low
10	$30F	m8 register high
10	$310	m9 register low
10	$311	m9 register high
10	$312	command register_0
10	$313	command register_1
10	$314	reserved
:	:	:
10	$7FF	reserved
11	$xxx	reserved

Table 1. Control Register Addressing.

Circuit Description (continued)

Matrix Multiplication Operation

```
8-bit pixel input:   DA7 DA6 DA5 DA4 DA3 DA2 DA1 DA0
11-bit coefficient:                          C10 C9 C8 . C7 C6 C5 C4 C3 C2 C1 C0
-------------------------------------------------------------------------------
19-bit total:   S T17 T16 T15 T14 T13 T12 T11 T10 T9 T8 . T7 T6 T5 T4 T3 T2 T1 T0
```

Three of these 19-bit totals (since there are three coefficients per channel) must be added together, resulting in a 21-bit result per channel (S = sign bit):

S R19 R18 R17 R16 R15 R14 R13 R12 R11 R10 R9 R8 . R7 R6 R5 R4 R3 R2 R1 R0

CR17–CR15	QA7	QA6	QA5	QA4	QA3	QA2	QA1	QA0	Used for Rounding
unsigned magnitude format									
100	R19	R18	R17	R16	R15	R14	R13	R12	R11–R0
011	R18	R17	R16	R15	R14	R13	R12	R11	R10–R0
010	R17	R16	R15	R14	R13	R12	R11	R10	R9–R0
001	R16	R15	R14	R13	R12	R11	R10	R9	R8–R0
000	R15	R14	R13	R12	R11	R10	R9	R8	R7–R0
other two formats									
100	S	R18	R17	R16	R15	R14	R13	R12	R11–R0
011	S	R17	R16	R15	R14	R13	R12	R11	R10–R0
010	S	R16	R15	R14	R13	R12	R11	R10	R9–R0
001	S	R15	R14	R13	R12	R11	R10	R9	R8–R0
000	S	R14	R13	R12	R11	R10	R9	R8	R7–R0

Table 2. Example Dynamic Output Range Selections (QAx Channel).

Circuit Description (continued)

Number Representations

The Bt281 accommodates analog sign magnitude, unsigned magnitude, and 2's complement formats to ease interfacing to A/D and D/A converters, frame buffers, and processing circuits. (See Table 3.)

Offset Binary Representation

Only the DAx and DCx inputs and the QAx and QCx outputs can be configured for this representation for processing of color difference signals (Cr/Cb, I/Q, U/V, R-Y/B-Y, etc.). The DBx inputs and QBx outputs are always configured for 8-bit unsigned magnitude representation (0–255) for luminance processing.

Offset binary representation should be used if A/D converters drive the DAx and DCx inputs (with the A/D midscale corresponding to zero).

Offset binary representation should be used at the output if the QAx and QCx outputs drive D/A converters (with the D/A midscale corresponding to zero).

2's Complement Representation

Frame buffers and image processors commonly use 2's complement representation to simplify sign bit handling.

Only the DAx and DCx inputs and the QAx and QCx outputs can be configured for this representation for processing of color difference signals (Cr/Cb, I/Q, U/V, R-Y/B-Y, etc.). The DBx inputs and QBx outputs are always configured for 8-bit unsigned magnitude representation (0–255) for luminance processing.

2's complement may be used at the input if a frame buffer is driving the DAx and DCx inputs to ease interfacing to other image processing circuitry. 2's complement may be used at the output if the QAx and QCx outputs are interfaced to a frame buffer to ease interfacing to image processing circuitry.

Unsigned Magnitude Representation

This 0 to 255 range input/output format is used when the Bt281 is inputting or outputting RGB video signals.

	Offset Binary Representation		2's Complement Representation		Unsigned Magnitude Representation	
DAx, DCx, QAx, QCx	DA7–DA0, DC7–DC0	Number Represented	DA7–DA0, DC7–DC0	Number Represented	DA7–DA0, DC7–DC0	Number Represented
$FF	1111 1111	+127	1111 1111	–1	1111 1111	255
$FE	1111 1110	+126	1111 1110	–2	1111 1110	254
:	:	:	:	:	:	:
$81	1000 0001	+1	1000 0001	–127	1000 0001	129
$80	1000 0000	0	1000 0000	–128	1000 0000	128
$7F	0111 1111	–1	0111 1111	+127	0111 1111	127
:	:	:	:	:	:	:
$01	0000 0001	–127	0000 0001	+1	0000 0001	1
$00	0000 0000	–128	0000 0000	0	0000 0000	0

Table 3. Numbering Representations.

Circuit Description (continued)

Input Interpolation Circuitry

The Bt281 may be configured to input 8 bits of luminance on the DBx inputs and 8 bits of multiplexed color difference signals on the DCx inputs. The multiplexed color difference signals are demultiplexed and the missing values interpolated using linear interpolation filters. The resulting 24 bits of luminance and color difference data are input to the 3 x 3 matrix multiplier for processing (see Figure 9). The DAx inputs are ignored. Figure 2 illustrates the input interpolation circuitry.

Assume YCrCb processing with Y input via the DBx inputs and multiplexed Cr/Cb input via the DCx inputs:

The 16-bit input sequence is:

DBx = Y (n) Y (n + 1) Y (n + 2) Y (n + 3)
DCx = Cb (n) Cr (n) Cb (n + 2) Cr (n + 2)

The 24-bit output after the interpolation filters is:

DBx '= Y (n) Y (n + 1) Y (n + 2) Y (n + 3)
DCx '= Cb (n) Cb (n + 1) Cb (n + 2) Cb (n + 3)
DAx '= Cr (n) Cr (n + 1) Cr (n + 2) Cr (n + 3)

The CFLAG input indicates whether the multiplexed DCx inputs contain Cb (CFLAG = 1) or Cr (CFLAG = 0) information. The demultiplexer, controlled by CFLAG, demultiplexes the Cr and Cb information. Alternately, nonmultiplexed color difference signals may be input via the DAx and DCx inputs, with a data rate of 1/2 the DBx inputs (see Figure 11). The interpolation filter generates the missing values by averaging successive data points.

Assume YCrCb processing with Y input via the DBx inputs, Cr input via the DAx inputs, and Cb input via the DCx inputs:

The 24-bit input sequence is:

DAx = Cr (n) Cr (n) Cr (n + 2) Cr (n + 2)
DBx = Y (n) Y (n + 1) Y (n + 2) Y (n + 3)
DCx = Cb (n) Cb (n) Cb (n + 2) Cb (n + 2)

The 24-bit output after the interpolation filters is:

DBx '= Y (n) Y (n + 1) Y (n + 2) Y (n + 3)
DCx' = Cb (n) Cb (n + 1) Cb (n + 2) Cb (n + 3)
DAx' = Cr (n) Cr (n + 1) Cr (n + 2) Cr (n + 3)

In either case, the DBx inputs are configured for an unsigned magnitude representation, while the DAx and DCx inputs are configured for either offset binary or 2's complement numbering representation.

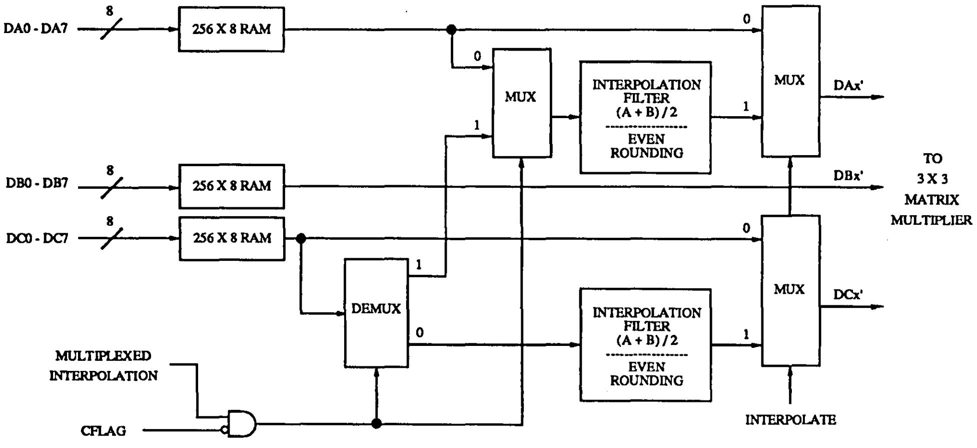

DA0 - DA7
8
256 X 8 RAM
0
1
MUX
INTERPOLATION FILTER (A + B) / 2
EVEN ROUNDING
0
1
MUX
DAx'
DB0 - DB7
8
256 X 8 RAM
DBx'
TO 3 X 3 MATRIX MULTIPLIER
DC0 - DC7
8
256 X 8 RAM
1
DEMUX
0
INTERPOLATION FILTER (A + B) / 2
EVEN ROUNDING
0
1
MUX
DCx'
MULTIPLEXED INTERPOLATION
CFLAG
INTERPOLATE

Figure 2. Input Interpolation Circuitry.

Circuit Description (continued)

The output of the interpolation filters is 9 bits (including sign). Rounding to 8 bits is done as follows: round up if the fractional data = 0.5 and the result will round to an even number (LSB = 0) or if the fractional data is > 0.5. If the fractional data is < 0.5, the number will be rounded down.

Output Decimation Circuitry

The Bt281 may be configured to output 8 bits of luminance on the QBx outputs and 8 bits of multiplexed color difference signals on the QCx outputs. The color difference signals from the matrix multiplier are decimated and multiplexed onto the QCx outputs (see Figure 10).

The QBx outputs are configured for an unsigned magnitude representation, while the QAx and QCx outputs are configured for either offset binary or 2's complement representation.

The CFLAG input is used to specify whether Cr or Cb data is to be output onto the QCx bus. If CFLAG is a logical zero, Cb data is output during the next clock cycle. If CFLAG is a logical one, Cr data is output during the next clock cycle. This timing enables the CFLAG status to match the data present on the QCx outputs.

Decimation is done by the multiplexer, by removing every other sample of color information.

Figure 3 illustrates the output decimation circuitry.

Assume YCrCb processing with Y output via the QBx outputs and multiplexed CrCb output via the QCx outputs:

The 24-bit input to the decimation circuit is:

QAx' = Cr (n) Cr (n + 1) Cr (n + 2) Cr (n + 3)
QBx' = Y (n) Y (n + 1) Y (n + 2) Y (n + 3)
QCx' = Cb (n) Cb (n + 1) Cb (n + 2) Cb (n + 3)

The output sequence is:

QBx = Y (n) Y (n + 1) Y (n + 2) Y (n + 3)
QCx = Cb (n) Cr (n) Cb (n + 2) Cr (n + 2)
QAx = Cr (n) Cr (n + 1) Cr (n + 2) Cr (n + 3)

Note that the QAx outputs contain normal output data.

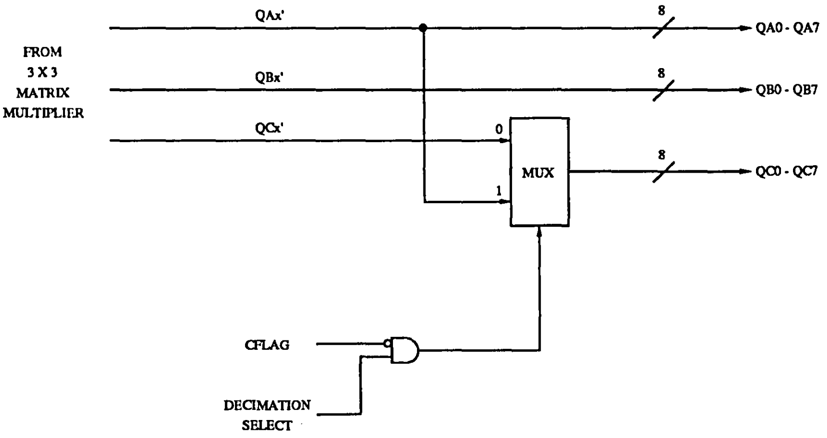


Figure 3. Output Decimation Circuitry.

Circuit Description (continued)

Typical Applications

Figure 4 shows two common applications of the Bt281. Figure 4a shows the Bt281 being used when the color space of the analog video signal to be digitized may be one of several formats. The Bt281 is ensures that the video data is converted into the color space of the frame buffer.

In Figure 4b, the Bt281 is used to convert a frame buffer using a color space other than RGB (i.e., YIQ, YUV, etc.) into the RGB color space to drive the CRT display.

The Bt281 enables these color space transformations to take place in real time, simplifying the system design.

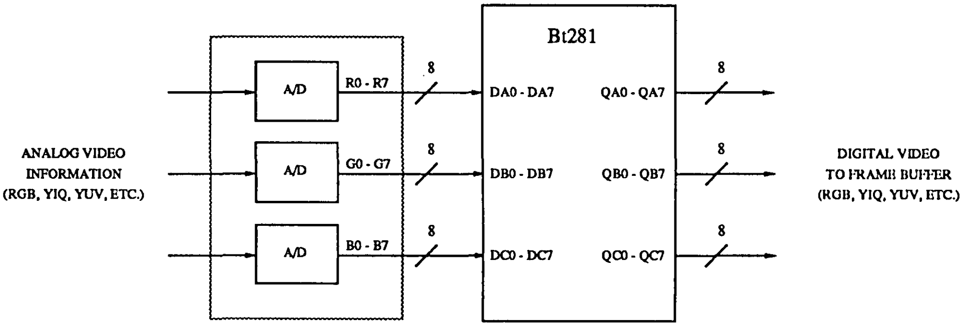

ANALOG VIDEO
INFORMATION
(RGB, YIQ, YUV, ETC.)
A/D
A/D
A/D
R0 - R7
G0 - G7
B0 - B7
8
8
8
Bt281
DA0 - DA7
DB0 - DB7
DC0 - DC7
QA0 - QA7
QB0 - QB7
QC0 - QC7
8
8
8
DIGITAL VIDEO
TO FRAME BUFFER
(RGB, YIQ, YUV, ETC.)

Figure 4a. Typical Application.

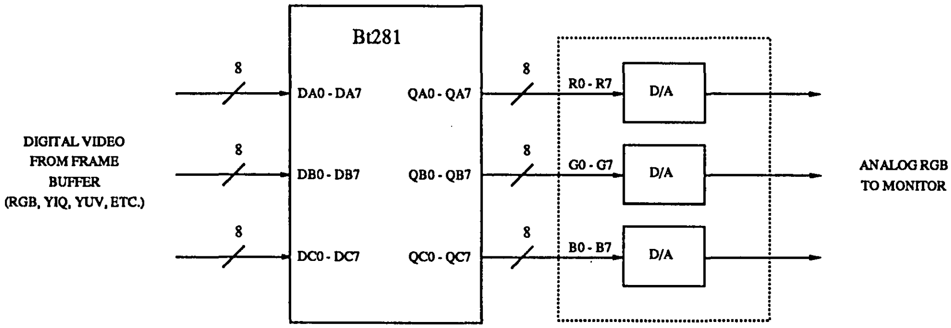

DIGITAL VIDEO
FROM FRAME
BUFFER
(RGB, YIQ, YUV, ETC.)
8
8
8
Bt281
DA0 - DA7
DB0 - DB7
DC0 - DC7
QA0 - QA7
QB0 - QB7
QC0 - QC7
8
8
8
R0 - R7
G0 - G7
B0 - B7
D/A
D/A
D/A
ANALOG RGB
TO MONITOR

Figure 4b. Typical Application.

Internal Registers

Command Register_0

This command register may be written to or read by the MPU at any time and is initialized to $00 following a reset sequence. CR00 is the least significant bit and corresponds to data bus bit D0. Note that the pipeline delay is constant regardless of the input/output configuration.

CR07–CR05 DAx, DCx input format select

(000) unsigned magnitude (nonmultiplexed, no interpolation)
(001) offset binary (nonmultiplexed, no interpolation)
(010) offset binary (nonmultiplexed, interpolated)
(011) offset binary (multiplexed, interpolated)

(100) 2's complement (nonmultiplexed, no interpolation)
(101) 2's complement (nonmultiplexed, interpolated)
(110) 2's complement (multiplexed, interpolated)
(111) pseudo-color mode (unsigned magnitude, nonmultiplexed, no interpolation)

These bits are ignored in bypass mode. They specify the input format and range for the DAx and DCx inputs. The DBx inputs are always configured for unsigned magnitude operation.

If pseudo-color mode is selected, the DBx inputs address all three lookup table RAMs simultaneously, generating 24 bits of color information. The DAx and DCx inputs are ignored.

CR04–CR02 QAx, QCx output format select

(000) unsigned magnitude (nonmultiplexed, no decimation)
(001) offset binary (nonmultiplexed, no decimation)
(010) offset binary (multiplexed, decimated)
(011) reserved

(100) 2's complement (nonmultiplexed, no decimation)
(101) 2's complement (multiplexed, decimated)
(110) reserved
(111) reserved

These bits specify the output format and range for the QAx and QCx outputs. The QBx outputs are always configured for unsigned magnitude operation. These bits are ignored in bypass mode.

CR01 Error flag

(0) reset by MPU
(1) set by device

This bit is set by the device if a negative number is detected on the QAx, QBx, or QCx outputs while outputting an unsigned magnitude number (which should always be positive). To reset the bit to a logical zero, the MPU must write a logical zero to this bit. Note that the error flag may be set if the MPU accesses the lookup table RAMs and while programming the command registers if the operating mode is changed.

Internal Registers (continued)

Command Register_0 (continued)

CR00 Overflow / underflow error flag

(0) reset by MPU
(1) set by device

This bit is set by the device if an overflow or underflow condition is detected on the 3 x 3 matrix multiplier outputs (prior to the saturation circuitry). To reset the bit to a logical zero, the MPU must write a logical zero to this bit. Note that the overflow/underflow flag may be set if the MPU accesses the lookup table RAMs and while programming the command registers if the operating mode is changed.

Command Register_1

This command register may be written to or read by the MPU at any time and is initialized to $E1 following a reset sequence. CR10 is the least significant bit and corresponds to data bus bit D0. Note that the pipeline delay is constant regardless of the input/output configuration.

CR17–CR15 Matrix dynamic output range select

(000) R8–R15 for unsigned magnitude output format; R9–R14 + sign for other formats
(001) R9–R16 for unsigned magnitude output format; R10–R15 + sign for other formats
(010) R10–R17 for unsigned magnitude output format; R11–R16 + sign for other formats
(011) R11–R18 for unsigned magnitude output format; R12–R17 + sign for other formats
(100) R12–R19 for unsigned magnitude output format; R13–R18 + sign for other formats
(101) reserved
(110) reserved
(111) bypass device

Mode (111) specifies to bypass the entire device with no change in pipeline delay. See Table 2.

CR14–CR11 reserved

CR10 QAx, QBx, QCx output disable

(0) enable QAx, QBx, and QCx outputs
(1) disable QAx, QBx, and QCx outputs

This bit is logically gated with the OE* input pin, and the resulting value is used to control three-stating the QAx, QBx, and QCx outputs.

Internal Registers (continued)

m1–m9 Low/High Registers

For the m1–m9 values, the 8-bit low and high registers are cascaded to form a 11-bit register. D0–D7 comprise the low register, while D8–D10 comprise the high register (D8 corresponds to data bus bit D0). D3–D7 of m1–m9 high registers are always a logical zero.

The m1–m9 low/high registers may be written to or read by the MPU at any time and are not initialized following a reset sequence. D0 is the least significant bit.

These registers specify the matrix operators from–4.000 to +3.996 (using 2's complement notation) as follows:

D10 - D0	Value
111 . 1111 1111	–0.004
111 . 1111 1110	–0.008
:	:
100 . 0000 0001	–3.996
100 . 0000 0000	–4.000
011 . 1111 1111	+3.996
:	:
000 . 0000 0001	+0.004
000 . 0000 0000	+0.000

Pin Descriptions

Pin Name	Description
DA0–DA7, DB0–DB7, DC0–DC7	Color inputs (TTL compatible). These inputs are latched on the rising edge of CLOCK. DA0, DB0, and DC0 are the least significant bits.
QA0–QA7, QB0–QB7, QC0–QC7	Color outputs (TTL compatible). These signals are output following the rising edge of CLOCK. QA0, QB0, and QC0 are the least significant bits.
IN0, IN1, OUT0, OUT1	Input/output delay line (TTL compatible). IN0 and IN1 are latched on the rising edge of CLOCK, pipelined to maintain synchronization with the color data, and output onto OUT0 and OUT1 following the rising edge of CLOCK.
CFLAG	Multiplex control input (TTL compatible). If the DAx/DCx inputs are multiplexed, CFLAG indicates when DCx data is present (CFLAG = 1). If the QAx/QCx outputs are multiplexed, CFLAG indicates when QCx data is to be output (CFLAG = 1). CFLAG is latched on the rising edge of CLOCK. This input is ignored when in the bypass mode.
OE*	Output enable control input (TTL compatible). This input is logically gated with command bit CR10, and the result controls three-stating the QAx, QBx, and QCx outputs. OUT0 and OUT1 are not three-statable.

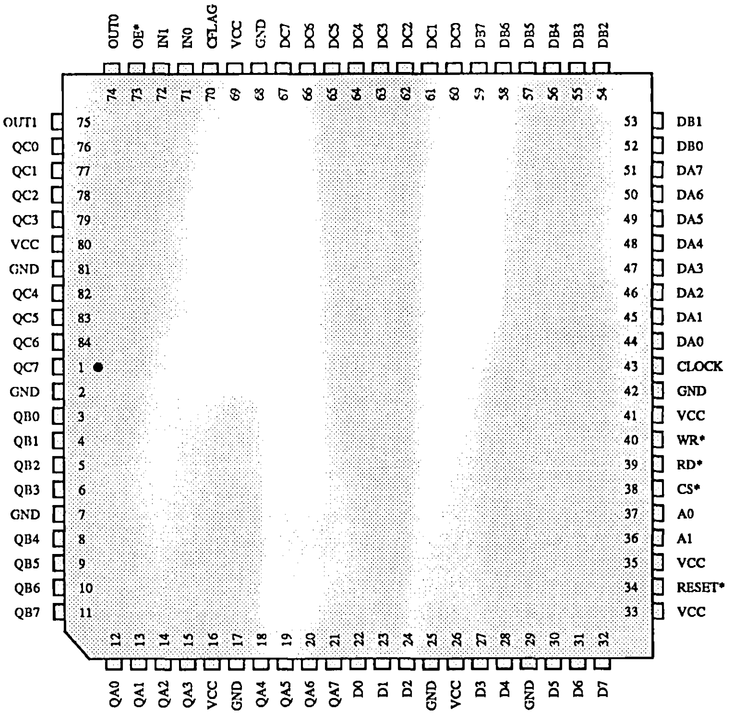
CR10	OE*	QAx, QBx, QCx Outputs
0	0	enabled
0	1	three-stated
1	0	three-stated
1	1	three-stated

Pin Name	Description
CLOCK	Clock input (TTL compatible).
D0–D7	Bidirectional MPU data bus (TTL compatible). MPU data is input to and output from the device via this 8-bit data bus. D0 is the least significant bit.
CS*	Chip select control input (TTL compatible). CS* is latched on the falling edge of either RD* or WR*. An internally latched logical zero enables data to be written to or read from the device by the MPU. CS* should be connected to GND if not used.
RD*	Read control input (TTL compatible). A logical zero enables the MPU to read data from the device. Both RD* and WR* should not be asserted simultaneously. (See Figure 7.)
WR*	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*. Both RD* and WR* should not be asserted simultaneously. (See Figure 7.)

Latched CS*	RD*	WR*	MPU Operation
0	0	0	invalid operation
0	0	1	read data onto D0–D7
0	1	0	write D0–D7 data
0	1	1	D0–D7 three-stated
1	x	x	D0–D7 three-stated

Pin Descriptions (continued)

Pin Name	Description
A0, A1	Register select inputs (TTL compatible). A0 and A1 are latched on the falling edge of either RD* or WR*.
RESET*	Reset control input (TTL compatible). RESET* must be a logical zero for a minimum of three consecutive clock cycles to reset the device. RESET* must be a logical one for normal operation.
VCC	Power. All VCC pins must be connected together.
GND	Ground. All GND pins must be connected together.


74 OUT0
73 OE*
72 IN1
71 IN0
70 CFLAG
69 VCC
68 GND
67 DC7
66 DC6
65 DC5
64 DC4
63 DC3
62 DC2
61 DC1
60 DC0
59 DB7
58 DB6
57 DB5
56 DB4
55 DB3
54 DB2
OUT1 75
QC0 76
QC1 77
QC2 78
QC3 79
VCC 80
GND 81
QC4 82
QC5 83
QC6 84
QC7 1
GND 2
QB0 3
QB1 4
QB2 5
QB3 6
GND 7
QB4 8
QB5 9
QB6 10
QB7 11
53 DB1
52 DB0
51 DA7
50 DA6
49 DA5
48 DA4
47 DA3
46 DA2
45 DA1
44 DA0
43 CLOCK
42 GND
41 VCC
40 WR*
39 RD*
38 CS*
37 A0
36 A1
35 VCC
34 RESET*
33 VCC
12 QA0
13 QA1
14 QA2
15 QA3
16 VCC
17 GND
18 QA4
19 QA5
20 QA6
21 QA7
22 D0
23 D1
24 D2
25 GND
26 VCC
27 D3
28 D4
29 GND
30 D5
31 D6
32 D7

Application Information

RGB-to-Y,R-Y,B-Y Conversion

The matrix for converting analog RGB to Y, R-Y, B-Y is as follows. The RGB inputs are normalized to have a range of 0 to 1 and are gamma-corrected RGB data.

$$\begin{bmatrix} Y \\ R-Y \\ B-Y \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ 0.701 & -0.587 & -0.114 \\ -0.299 & -0.587 & 0.886 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Note that the analog (R – Y) and (B – Y) terms have an output range of ± 0.701 and ± 0.886, respectively, while Y has a range of 0 to 1.

The conversion of digital RGB to normalized digital Y, (R – Y)', (B – Y)' (the ' indicates normalized notation) is slightly different in order to compress the (R – Y)' and (B – Y)' output range to ±0.5. The input and output assignment of the Bt281 video I/O pins is assumed to be as follows:

DA0–DA7 = R_0–R_7
DB0–DB7 = G_0–G_7
DC0–DC7 = B_0–B_7

QA0–QA7 = $(R-Y)'_0$–$(R-Y)'_7$
QB0–QB7 = Y_0–Y_7
QC0–QC7 = $(B-Y)'_0$–$(B-Y)'_7$

The RGB inputs to the matrix can have a range of 0 to 255; the lookup table RAMs on the Bt281 may be used to gamma-correct the RGB data if necessary. The Y output of the matrix can have a range of 0 to 255, while the (R – Y)' and (B – Y)' outputs can have a range of –128 to +127. The ideal matrix (normalized to the dynamic range) is as follows:

$$\begin{bmatrix} Y \\ (R-Y)' \\ (B-Y)' \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ 0.500 & -0.419 & -0.081 \\ -0.169 & -0.331 & 0.500 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Given the resolution of the Bt281 is limited to 0.0039063 (1/256), and the previously specified input/output pin assignments, the following matrix is used (after 2's complement conversion and row-swapping:

$$\begin{bmatrix} (R-Y)' \\ Y \\ (B-Y)' \end{bmatrix} = \begin{bmatrix} \$0.80 & \$7.95 & \$7.EC \\ \$0.4C & \$0.96 & \$0.1D \\ \$7.D5 & \$7.AC & \$0.80 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

The command register should specify unsigned magnitude representation for the DAx and DCx inputs, and either offset binary or 2's complement representation for the QAx and QCx outputs. Command bits CR17–CR15 should be 000.

Application Information (continued)

RGB to YUV Conversion

The matrix for converting analog RGB to YUV is as follows. The RGB inputs are normalized to have a range of 0 to 1 and are gamma-corrected RGB data.

$$\begin{bmatrix} Y \\ U \\ V \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ -0.147 & -0.289 & 0.436 \\ 0.615 & -0.515 & -0.100 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Note that the analog U and V terms have an output range of ± 0.436 and ± 0.615, respectively, while Y has a range of 0 to 1.

Note that U and V may also be defined as:

$$U = (B - Y) / 2.03 = 0.4926(B - Y)$$

$$V = (R - Y) / 1.14 = 0.8772(R - Y)$$

The conversion of digital RGB to normalized digital YU'V' (the ' indicates normalized notation) is slightly different in order to compress the V' output range to ±0.5 and to expand the U' output range to ±0.5. The input and output assignment of the Bt281 video I/O pins is assumed to be as follows:

DA0–DA7 = R_0–R_7
DB0–DB7 = G_0–G_7
DC0–DC7 = B_0–B_7

QA0–QA7 = V'_0–V'_7
QB0–QB7 = Y_0–Y_7
QC0–QC7 = U'_0–U'_7

The RGB inputs to the matrix can have a range of 0 to 255; the lookup table RAMs on the Bt281 may be used to gamma-correct the RGB data if necessary. The Y output of the matrix can have a range of 0 to 255, while the U' and V' outputs can have a range of –128 to +127. The ideal matrix (normalized to the dynamic range) is as follows:

$$\begin{bmatrix} Y \\ U' \\ V' \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ -0.169 & -0.331 & 0.500 \\ 0.500 & -0.419 & -0.081 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Given the resolution of the Bt281 is limited to 0.0039063 (1/256), and the previously specified input/output pin assignments, the following matrix is used (after 2's complement conversion and row swapping:

$$\begin{bmatrix} V' \\ Y \\ U' \end{bmatrix} = \begin{bmatrix} \$0.80 & \$7.95 & \$7.EC \\ \$0.4C & \$0.96 & \$0.1D \\ \$7.D5 & \$7.AC & \$0.80 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

The command register should specify unsigned magnitude representation for the DAx and DCx inputs, and either offset binary or 2's complement representation for the QAx and QCx outputs. Command bits CR17–CR15 should be 000.

Application Information (continued)

RGB to YIQ Conversion

The matrix for converting analog RGB to YIQ is as follows. The RGB inputs are normalized to have a range of 0 to 1 and are gamma-corrected RGB data.

$$\begin{bmatrix} Y \\ I \\ Q \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ 0.596 & -0.275 & -0.321 \\ 0.212 & -0.523 & 0.311 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Note that the analog I and Q terms have an output range of ±0.596 and ±0.525, respectively, while Y has a range of 0 to 1.

I and Q may also be defined as follows:

$$I = V\cos 33^\circ - U\sin 33^\circ$$

$$Q = V\sin 33^\circ + U\cos 33^\circ$$

or

$$I = 0.839V - 0.545U$$

$$Q = 0.545V + 0.839U$$

or

$$I = 0.736(R - Y) - 0.268(B - Y)$$

$$Q = 0.478(R - Y) + 0.413(B - Y)$$

The conversion of digital RGB to normalized digital YI'Q' (the ' indicates normalized notation) is slightly different in order to compress the I' and Q' output range to ±0.5. The input and output assignment of the Bt281 video I/O pins is assumed to be as follows:

DA0–DA7 = R_0–R_7
DB0–DB7 = G_0–G_7
DC0–DC7 = B_0–B_7

QA0–QA7 = I'_0–I'_7
QB0–QB7 = Y_0–Y_7
QC0–QC7 = Q'_0–Q'_7

The RGB inputs to the matrix can have a range of 0 to 255; the lookup table RAMs on the Bt281 may be used to gamma-correct the RGB data if necessary. The Y output of the matrix can have a range of 0 to 255, while the I' and Q' outputs can have a range of –128 to +127. The ideal matrix (normalized to the dynamic range) is as follows:

$$\begin{bmatrix} Y \\ I' \\ Q' \end{bmatrix} = \begin{bmatrix} 0.299 & 0.587 & 0.114 \\ 0.500 & -0.231 & -0.269 \\ 0.203 & -0.500 & 0.297 \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

Given the resolution of the Bt281 is limited to 0.0039063 (1/256), and the previously specified input/output pin assignments, the following matrix is used (after 2's complement conversion and row swapping):

$$\begin{bmatrix} I' \\ Y \\ Q' \end{bmatrix} = \begin{bmatrix} \$0.80 & \$7.C5 & \$7.BC \\ \$0.4C & \$0.96 & \$0.1D \\ \$0.33 & \$7.80 & \$0.4C \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix}$$

The command register should specify unsigned magnitude representation for the DAx and DCx inputs, and either offset binary or 2's complement representation for the QAx and QCx outputs. Command bits CR17–CR15 should be 000.

Application Information (continued)

Y/R-Y/B-Y-to-RGB Conversion

The matrix for converting analog Y/R-Y/B-Y to RGB is as follows. The Y,R-Y,B-Y inputs are not normalized and generate gamma-corrected RGB data.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 \\ 1 & -0.509 & -0.194 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} Y \\ R-Y \\ B-Y \end{bmatrix}$$

Note that the analog (R – Y) and (B – Y) terms have an input range of ±0.701 and ±0.886, respectively, while Y has a range of 0 to 1.

The conversion of normalized digital Y,(R – Y)',(B – Y)' (the ' indicates normalized notation) to digital RGB is slightly different as the (R – Y)' and (B – Y)' input range has probably been compressed to ±0.5. The input and output assignment of the Bt281 video I/O pins is assumed to be as follows:

DA0–DA7 = $(R-Y)'_0$–$(R-Y)'_7$
DB0–DB7 = Y_0–Y_7
DC0–DC7 = $(B-Y)'_0$–$(B-Y)'_7$

QA0–QA7 = R_0–R_7
QB0–QB7 = G_0–G_7
QC0–QC7 = B_0–B_7

The Y input to the matrix can have a range of 0 to 255 for Y, while the (R – Y)' and (B – Y)' inputs can have an input range of –128 to +127. The gamma-corrected RGB outputs of the matrix can have a range of 0 to 255. The ideal matrix (normalized to the dynamic range) is as follows:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 1.402 & 0 \\ 1 & -0.714 & -0.344 \\ 1 & 0 & 1.772 \end{bmatrix} \begin{bmatrix} Y \\ (R-Y)' \\ (B-Y)' \end{bmatrix}$$

Given the resolution of the Bt281 is limited to 0.0039063 (1/256), and the previously specified input/output pin assignments, the following matrix is used (after 2's complement conversion and row swapping):

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} \$1.66 & \$1.00 & \$0.00 \\ \$7.4A & \$1.00 & \$7.A8 \\ \$0.00 & \$1.00 & \$1.C5 \end{bmatrix} \begin{bmatrix} (R-Y)' \\ Y \\ (B-Y)' \end{bmatrix}$$

The command register should specify unsigned magnitude representation for the QAx and QCx outputs, and either offset binary or 2's complement representation for the DAx and DCx inputs. Command bits CR17–CR15 should be 000.

Application Information (continued)

YUV-to-RGB Conversion

The matrix for converting analog YUV to RGB is as follows. The YUV inputs are not normalized and generate gamma-corrected RGB data.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1.140 \\ 1 & -0.395 & -0.581 \\ 1 & 2.032 & 0 \end{bmatrix} \begin{bmatrix} Y \\ U \\ V \end{bmatrix}$$

Note that the analog U and V terms have an input range of ±0.436 and ±0.615, respectively, while Y has a range of 0 to 1.

The conversion of normalized digital YU'V' (the ' indicates normalized notation) to RGB is slightly different as the V' input range has probably been compressed to ±0.5 while the U' input range has probably been expanded to ±0.5. The input and output assignment of the Bt281 video I/O pins is assumed to be as follows:

DA0–DA7 = V'_0–V'_7
DB0–DB7 = Y_0–Y_7
DC0–DC7 = U'_0–U'_7

QA0–QA7 = R_0–R_7
QB0–QB7 = G_0–G_7
QC0–QC7 = B_0–B_7

The Y input to the matrix can have a range of 0 to 255, while the U' and V' inputs can have an input range of –128 to +127. The gamma-corrected RGB outputs of the matrix can have a range of 0 to 255. The ideal matrix (normalized to the dynamic range) is as follows:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1.402 \\ 1 & -0.344 & -0.714 \\ 1 & 1.772 & 0 \end{bmatrix} \begin{bmatrix} Y \\ U' \\ V' \end{bmatrix}$$

Given the resolution of the Bt281 is limited to 0.0039063 (1/256), and the previously specified input/output assignment, the following matrix is used (after 2's complement conversion and row swapping):

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} \$1.66 & \$1.00 & \$0.00 \\ \$7.4A & \$1.00 & \$7.A8 \\ \$0.00 & \$1.00 & \$1.C5 \end{bmatrix} \begin{bmatrix} V' \\ Y \\ U' \end{bmatrix}$$

The command register should specify unsigned magnitude representation for the QAx and QCx outputs, and either offset binary or 2's complement representation for the DAx and DCx inputs. Command bits CR1– CR15 should be 000.

Application Information (continued)

YIQ-to-RGB Conversion

The matrix for converting analog YIQ to RGB is as follows. The YIQ inputs are not normalized and generate gamma-corrected RGB data.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0.956 & 0.620 \\ 1 & -0.272 & -0.647 \\ 1 & -1.108 & 1.705 \end{bmatrix} \begin{bmatrix} Y \\ I \\ Q \end{bmatrix}$$

Note that the analog I and Q terms have an input range of ± 0.596 and ± 0.525, respectively, while Y has a range of 0 to 1.

The conversion of normalized digital YI'Q' (the ' indicates normalized notation) to RGB is slightly different as the I' and Q' input range has probably been compressed to ± 0.5. The input and output assignment of the Bt281 video I/O pins is assumed to be as follows:

DA0–DA7 = I_0–I_7
DB0–DB7 = Y_0–Y_7
DC0–DC7 = Q_0–Q_7

QA0–QA7 = R_0–R_7
QB0–QB7 = G_0–G_7
QC0–QC7 = B_0–B_7

The Y input to the matrix can have a range of 0 to 255, while the I' and Q' inputs can have an input range of –128 to +127. The gamma-corrected RGB outputs of the matrix can have a range of 0 to 255. The ideal matrix (normalized to the dynamic range) is as follows:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 1.139 & 0.648 \\ 1 & -0.324 & -0.677 \\ 1 & -1.321 & 1.783 \end{bmatrix} \begin{bmatrix} Y \\ I' \\ Q' \end{bmatrix}$$

Given the resolution of the Bt281 is limited to 0.0039063 (1/256), and the previously specified input/output assignment, the following matrix is used (after 2's complement conversion and row swapping):

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} \$1.23 & \$1.00 & \$0.A5 \\ \$7.AE & \$1.00 & \$7.53 \\ \$6.AE & \$1.00 & \$1.C8 \end{bmatrix} \begin{bmatrix} I' \\ Y \\ Q' \end{bmatrix}$$

The command register should specify unsigned magnitude representation for the QAx and QCx outputs, and either offset binary or 2's complement representation for the DAx and DCx inputs. Command bits CR17–CR15 should be 000.

Application Information (continued)

YIQ (D2 Format)-to-RGB Conversion

The D2 format digitizes the entire composite color video signal, including sync information. Thus, after digitally separating the Y, I, and Q information, the Y information has a range of 0–130, I has a range of 0–78 and Q has a range of 0–±68.

The matrix for converting digital YIQ (derived from a D2 format) to RGB is as follows.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1.972 & 18.875 & 1.223 \\ 1.972 & -0.538 & -1.267 \\ 1.972 & -2.187 & 3.361 \end{bmatrix} \begin{bmatrix} Y \\ I \\ Q \end{bmatrix}$$

The input and output assignment of the Bt281 video I/O pins is assumed to be as follows:

DA0–DA7 = I_0–I_7
DB0–DB7 = Y_0–Y_7
DC0–DC7 = Q_0–Q_7

QA0–QA7 = R_0–R_7
QB0–QB7 = G_0–G_7
QC0–QC7 = B_0–B_7

The Y input to the matrix can have a range of 0–130, while the I and Q inputs can have a range of 0–±78 and Q can have a range of 0–±68. The gamma-corrected RGB outputs of the matrix have a range of 0–255.

Given the resolution of the Bt281 is limited to 0.0039063 (1/256), and the previously specified input/output assignment, the following matrix is used (after 2's complement conversion and row swapping):

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} \$1.E0 & \$1.F9 & \$1.39 \\ \$7.77 & \$1.F9 & \$6.BC \\ \$5.D1 & \$1.F9 & \$3.5C \end{bmatrix} \begin{bmatrix} I \\ Y \\ Q \end{bmatrix}$$

The command register should specify unsigned magnitude representation for the QAx and QCx outputs, and either offset binary or 2's complement representation for the DAx and DCx inputs. Command bits CR17–CR15 should be 100.

Application Information (continued)

Concatenating Matrices

By concatenating matrices, conversions such as YIQ to YUV may be implemented. The procedure for concatenating matrices is as follows:

$$\begin{bmatrix} aj + bm + cp & ak + bn + cq & al + bo + cr \\ dj + em + fp & dk + en + fq & dl + eo + fr \\ gj + hm + ip & gk + hn + iq & gl + ho + ir \end{bmatrix} = \begin{bmatrix} a & b & c \\ d & e & f \\ g & h & i \end{bmatrix} \begin{bmatrix} j & k & l \\ m & n & o \\ p & q & r \end{bmatrix}$$

Implementing RGB to HSV

RGB to HSV may be performed by configuring the Bt281 to implement RGB-to-Y/R-Y/B-Y conversion.

The V value is equivalent to the Y (luminance) output onto QB0–QB7.

$$\text{Saturation (S)} = \text{SQRT}(R - Y^{2)} + (B - Y)$$

$$\text{Hue (H)} = \tan^{-1} (B - Y) / (R - Y)$$

Using the 16 bits (8 bits each) of (R – Y) and (B – Y) data generated by the Bt281 to address a 64K x 8 ROM (a 16K x 8 ROM may be used addressed by the six MSBs of the (R – Y) and (B – Y) data), the ROM is be programmed to generate 8 bits of saturation data using the equation above. An output register on the ROM data outputs may be needed to meet setup and hold times for any circuitry after the ROM.

The same 16 bits of (R – Y) and (B – Y) data generated by the Bt281 to address another 64K x 8 ROM (a 16K x 8 ROM may be addressed by the six MSBs of the (R – Y) and (B – Y) data), this ROM is programmed to generate 8 bits of hue data using the equation above. An output register on the ROM data outputs may be needed to meet setup and hold times for any circuitry after the ROM.

A single 64K x 16 ROM may be used instead of two 64K x 8 ROMs.

Implementing HSV to RGB

HSV to RGB may be performed by configuring the Bt281 to implement Y/R-Y/B-to-RGB conversion.

The V value is equivalent to the Y (luminance) input via DB0–DB7.

$$R - Y = S * \cos (H)$$

$$B - Y = S * \sin (H)$$

Using the 16 bits (8 bits each) of saturation (S) and hue (H) data to address a 64K x 8 ROM (a 16K x 8 ROM may be used addressed by the six MSBs of the S and H data), the ROM may be programmed to generate 8 bits of (R – Y) data to input to the Bt281 using the equation above. An input register on the ROM data inputs may be needed to meet setup and hold times to the ROM.

The same 16 bits (8 bits each) of saturation (S) and hue (H) data to address a 64K x 8 ROM (a 16K x 8 ROM may be used addressed by the six MSBs of the S and H data), the ROM is programmed to generate 8 bits of (B – Y) data to input to the Bt281 using the equation above. An input register on the ROM data inputs may be needed to meet setup and hold times.

A single 64K x 16 ROM may be used instead of two 64K x 8 ROMs.

Application Information (continued)

Matrix Coefficient Considerations

The example matrices are only typical; adjustment of the matrix coefficients may be required to minimize rounding errors, especially when multiple devices are cascaded.

Also, the matrix coefficients may be multiplied (left shifted) by 2 or 4, and the M1–M8 (2x) or M2–M9 (4x) outputs selected, rather than the M0–M7 outputs. This may reduce rounding errors, especially when multiple devices are used.

Color Correction of Cameras

The color response of a video camera is never exactly that specified by the standards, which require negative responses to certain portions of the light spectrum. In practice, this is achieved by matrixing the three color signals of the form:

$$R_{correct} = aR_{cam} + bG_{cam} + cB_{cam}$$

$$G_{correct} = dR_{cam} + eG_{cam} + fB_{cam}$$

$$B_{correct} = gR_{cam} + gG_{cam} + iB_{cam}$$

where the constants a, e, and i are positive values near unity and the other constants are small in comparison with unity and usually negative.

Since it is usually desired to keep the color balance of the camera constant:

$$a + b + c = 1$$

$$d + e + f = 1$$

$$g + h + i = 1$$

Rather than implementing the color correction using differential amplifiers, the Bt281 makes it feasible to use a digital architecture involving matrix multiplication.

Adjusting Contrast and Saturation

By scaling the matrix or lookup table RAM values, the contrast and saturation of a video signal may be adjusted while simultaneously converting to another color space.

Typical Applications

Figures 5 and 6 show typical applications of the Bt281 in an image capture and display environment.

Note the Bt281 may also be placed between the frame buffer memory and MPU. Thus, the MPU may operate in a single color space, while many color spaces may reside in the frame buffer. The CLOCK of the Bt281 would typically be connected to the video system clock.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance.

Latchup can be prevented by assuring that all VCC pins are at the same potential, and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Application Information (continued)

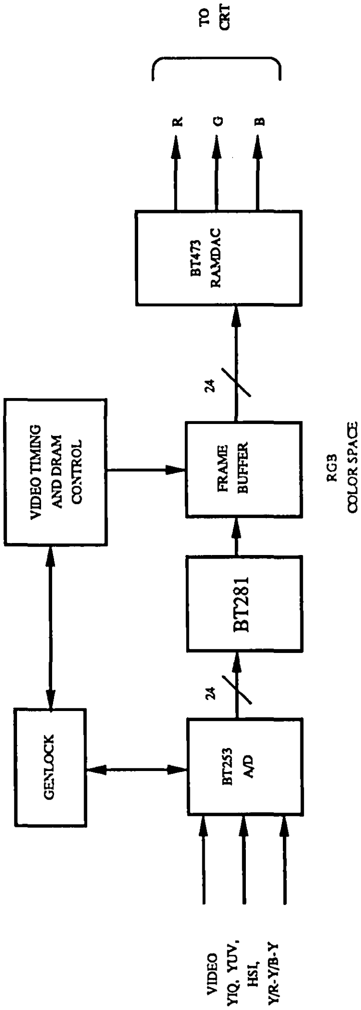

TO
CRT
R
G
B
BT473
RAMDAC
24
VIDEO TIMING
AND DRAM
CONTROL
FRAME
BUFFER
RGB
COLOR SPACE
BT281
24
GENLOCK
BT253
A/D
VIDEO
YIQ, YUV,
HSI,
Y/R-Y/B-Y

Figure 5. Typical Application.

Application Information (continued)

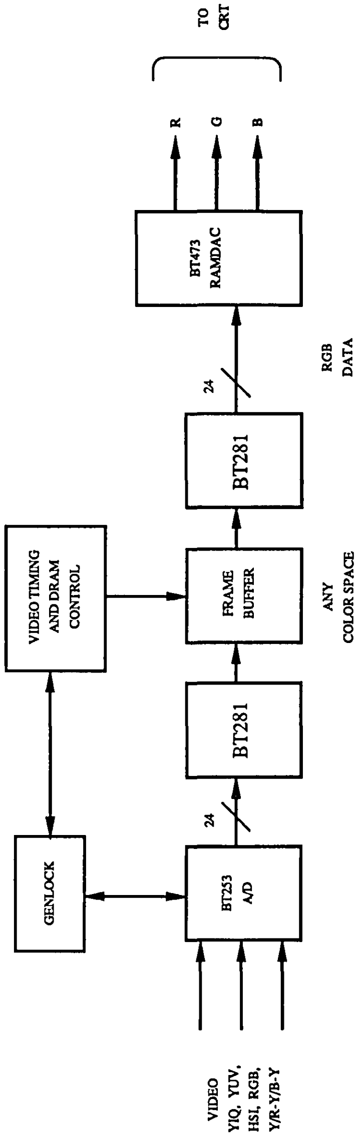

TO CRT
R
G
B
BT473 RAMDAC
24
RGB DATA
BT281
FRAME BUFFER
ANY COLOR SPACE
VIDEO TIMING AND DRAM CONTROL
BT281
24
GENLOCK
BT253 A/D
VIDEO
YIQ, YUV,
HSI, RGB,
Y/R-Y/B-Y

Figure 6. Typical Application.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.5	5.00	5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND– 0.5		VCC + 0.5	Volts
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	Volts
3-state Current	IOZ			10	µA
Output Capacitance	COUT		10		pF
QAx, QBx, QCx Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	Volts
3-state Current	IOZ			10	µA
Output Capacitance	COUT		10		pF
Other Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	Volts
Output Capacitance	COUT		10		pF

Test conditions (unless otherwise specified): "Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			36	MHz
A0, A1, CS* Setup Time	1	10			ns
A0, A1, CS* Hold Time	2	10			ns
RD*, WR* Low Time	3	70			ns
RD*, WR* High Time	4	15			ns
RD* Asserted to Data Bus Driven	5	1			ns
RD* Asserted to Data Valid	6			70	ns
RD* Negated to Data Bus 3-Stated	7			20	ns
Write Data Setup Time	8	10			ns
Write Data Hold Time	9	10			ns
Pixel and Control Setup Time	10				
DAx, DBx, DCx, IN0, IN1, CFLAG		5			ns
Pixel and Control Hold Time	11				
DAx, DBx, DCx, IN0, IN1, CFLAG		4			ns
Clock Cycle Time	12	27.7			ns
Clock Pulse Width High	13	10			ns
Clock Pulse Width Low	14	10			ns
Pipeline Delay		14	14	14	Clocks
Output Delay	15	tbd		16	ns
Three-State Disable Time	16			15	ns
Three-State Enable Time	17			15	ns
VCC Supply Current*	ICC		220	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. QAx, QBx, QCx, OUT0, OUT1 output load ≤ 75 pF, D0–D7 output load ≤ 75 pF. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*At Fmax. ICC (typ) at VCC = 5.0 V. ICC (max) at VCC (max).

Timing Waveforms

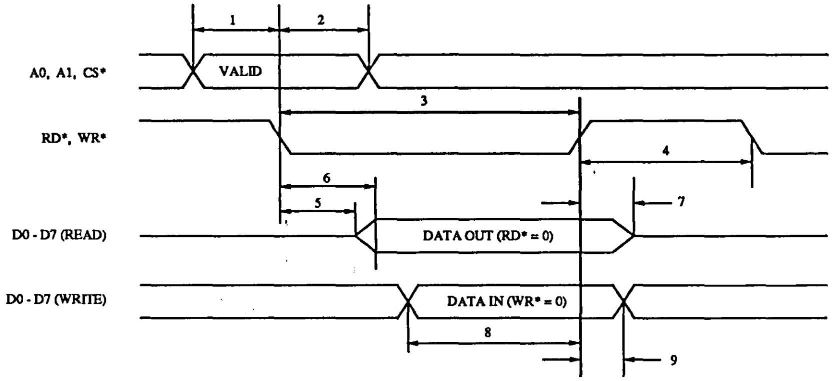

1
2
A0, A1, CS*
VALID
3
RD*, WR*
4
6
5
7
D0 - D7 (READ)
DATA OUT (RD* = 0)
D0 - D7 (WRITE)
DATA IN (WR* = 0)
8
9

Figure 7. MPU Read/Write Timing.

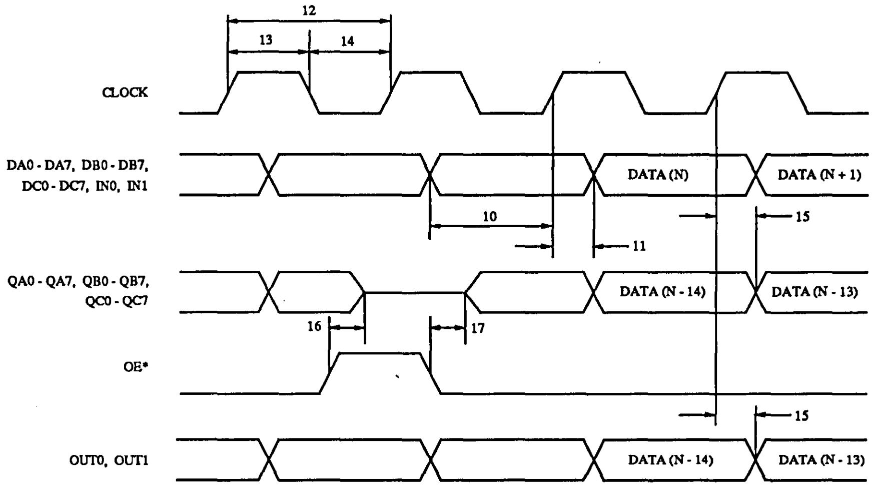

12
13
14
CLOCK
DA0 - DA7, DB0 - DB7,
DC0 - DC7, IN0, IN1
DATA (N)
DATA (N + 1)
10
11
15
QA0 - QA7, QB0 - QB7,
QC0 - QC7
DATA (N - 14)
DATA (N - 13)
16
17
OE*
15
OUT0, OUT1
DATA (N - 14)
DATA (N - 13)

Figure 8. Video Input/Output Timing
(Bypass or Noninterpolated & Nonmultiplexed 24-bit I/O).

Timing Waveforms (continued)

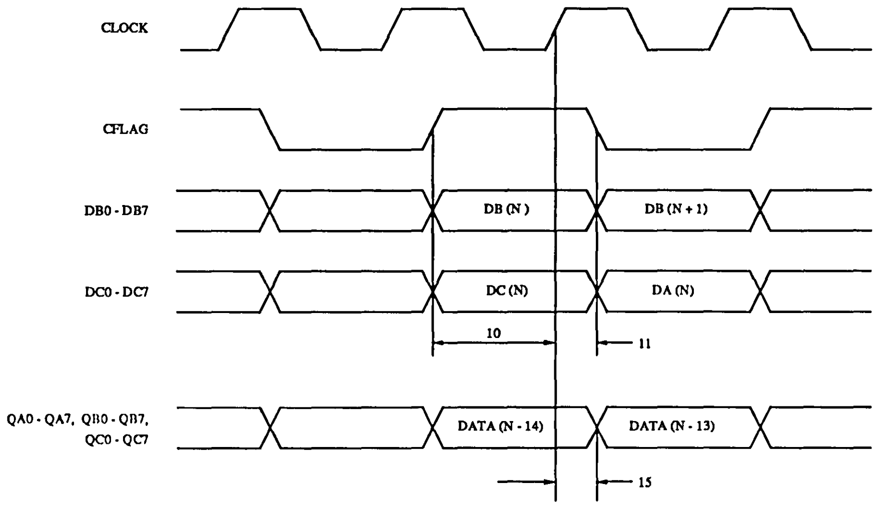

CLOCK
CFLAG
DB0 - DB7
DB (N)
DB (N + 1)
DC0 - DC7
DC (N)
DA (N)
10
11
QA0 - QA7, QB0 - QB7, QC0 - QC7
DATA (N - 14)
DATA (N - 13)
15

Figure 9. Video Input/Output Timing (Multiplexed & Interpolated 16-bit Input, 24-bit Output).

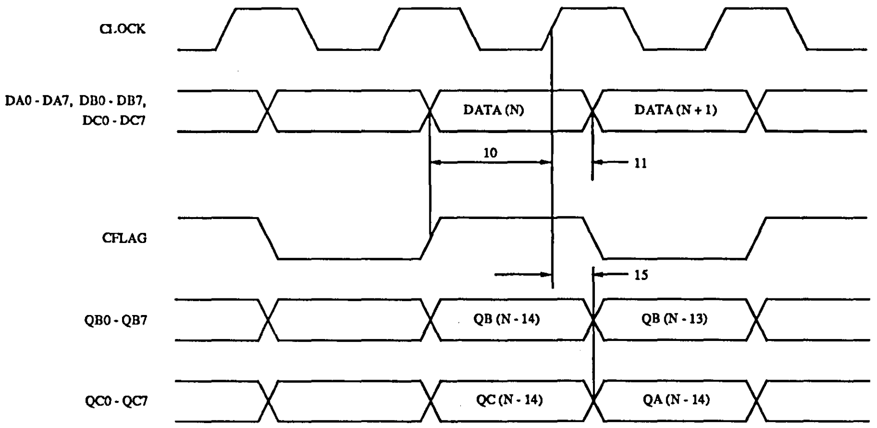

CLOCK
DA0 - DA7, DB0 - DB7, DC0 - DC7
DATA (N)
DATA (N + 1)
10
11
CFLAG
15
QB0 - QB7
QB (N - 14)
QB (N - 13)
QC0 - QC7
QC (N - 14)
QA (N - 14)

Figure 10. Video Input/Output Timing (24-bit Input, Multiplexed & Decimated 16-bit Output).

Timing Waveforms (continued)

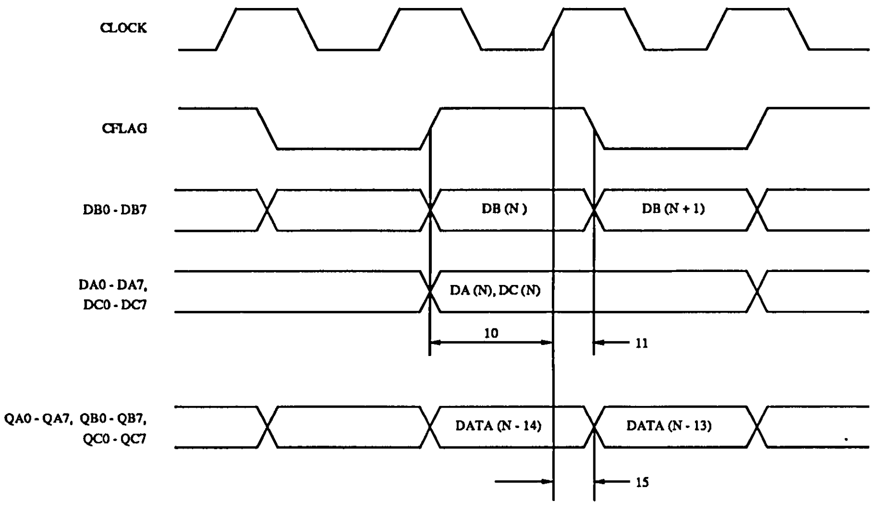

CLOCK
CFLAG
DB0 - DB7
DB (N)
DB (N + 1)
DA0 - DA7,
DC0 - DC7
DA (N), DC (N)
10
11
QA0 - QA7, QB0 - QB7,
QC0 - QC7
DATA (N - 14)
DATA (N - 13)
15

Figure 11. Video Input/Output Timing (Nonmultiplexed & Interpolated 24-bit Input, 24-bit Output).

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt281KPJ	84-pin Plastic J-Lead	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
E	Pipeline delay changed to 14 clock cycles, pixel setup time changed to 5 ns. Even rounding added after interpolation filters. Command bit CR10 modified to optionally three-state outputs. Table 2 added.
F	Replaced analog sign with offset binary notation. Note added to CR01 and CR00 command bits that they may be set while programming the command registers. Note added about 2's complement conversion and row-swapping between some matrices to clarify matrix transformations. YIQ to RGB matrices adjusted. Added note to DC/AC sections regarding typical values.

Preliminary Information

his document contains information on a new product. Parametric information, although ot fully characterized, is the result of testing initial devices.

Bt291

27 MHz VideoNet™ RGB-to-YCrCb 8-bit Encoder for 4:2:2 Video Applications

Distinguishing Features

- NTSC and CCIR Compatible
- Three 256 x 8 RGB Input RAMs
- Selectable RGB to YCrCb Conversion
- 16-Bit Multiplexed YCrCb I/O Bus
- 8-bit Ancillary Data Input Bus
- Selectable Cr/Cb Decimation Filters
- Low-Pass Y Filter (Optional)
- Video Timing Insertion
- Dynamic Range Control
- TTL Compatible Inputs and Outputs
- +5 V Monolithic CMOS
- 100-pin PLCC Package
- Typical Power Dissipation: 1.1 W

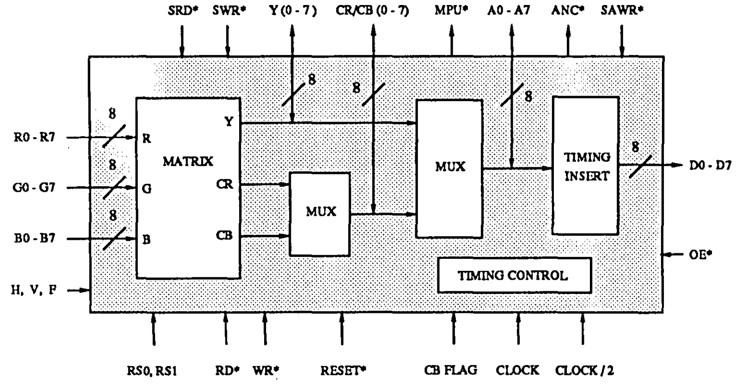
Applications

- CCIR601
- SMPTE RP125
- EBU 3246-E
- Image Processing and Capture
- RGB to YCrCb Conversion

Related Products

- Bt294, Bt296

Functional Block Diagram



Product Description

The Bt291 performs real-time RGB-to-YCrCb conversion. Twenty-four bits of RGB information (8 bits each) are input and converted to YCrCb color information (8 bits each). YCrCb data (4:4:4 format) may also be input via the RGB inputs.

The Y data is optionally low-pass filtered. The Cr and Cb data are decimated to 1/2 the Y data rate and multiplexed together. The Y and Cr/Cb data are further multiplexed, video timing information inserted, and output onto D0–D7.

A 16-bit YCrCb I/O bus is available for active video data I/O. Ancillary data may also be input via A0–A7 for insertion of digital audio, teletext, etc.

Three 256 x 8 lookup RAMs are available on the RGB inputs, to support gamma correction, etc.

The output enable (OE*) three-states the D0–D7 outputs asynchronously to the clocks.

An internal command register (accessible via A0–A7) enables forced blanking levels of Y and Cr/Cb data, and automatic line count transmission. RD* and WR* are used to control accessing the command register.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L291001 Rev. E

Brooktree®

Detailed Block Diagram

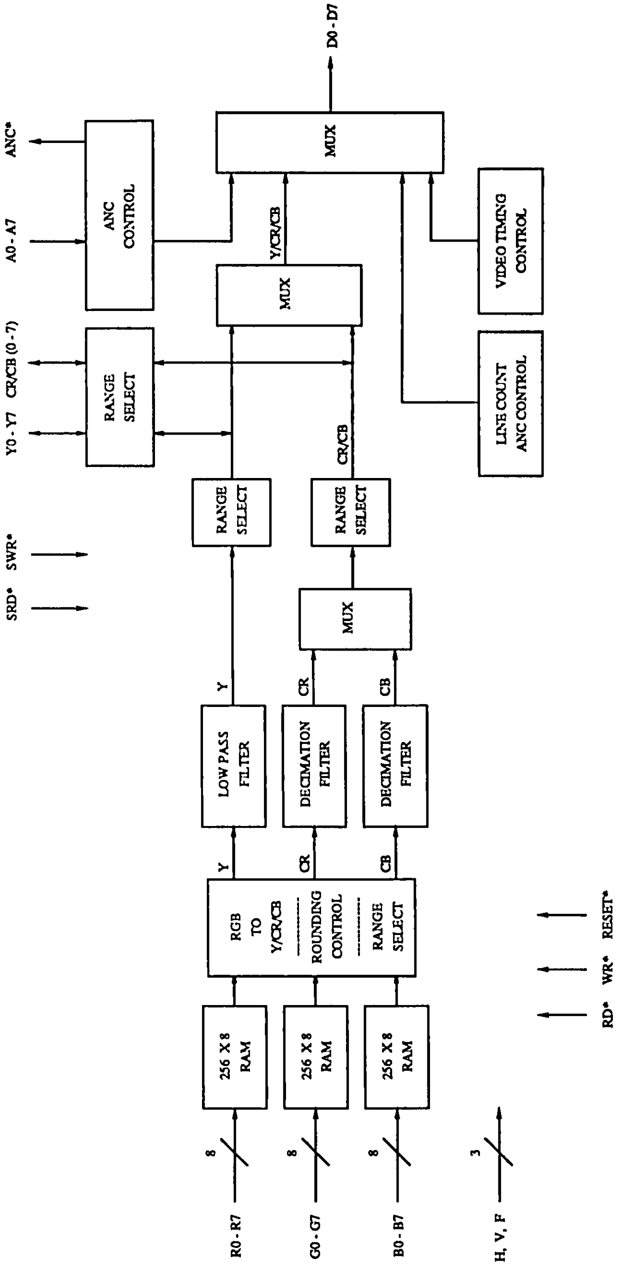

R0 - R7
G0 - G7
B0 - B7
H, V, F
8
8
8
3
256 X 8 RAM
256 X 8 RAM
256 X 8 RAM
RGB TO Y/CR/CB
ROUNDING CONTROL
RANGE SELECT
Y
CR
CB
LOW PASS FILTER
DECIMATION FILTER
DECIMATION FILTER
Y
CR
CB
MUX
RANGE SELECT
RANGE SELECT
CR/CB
RANGE SELECT
ANC CONTROL
MUX
Y/CR/CB
MUX
D0 - D7
LINE COUNT ANC CONTROL
VIDEO TIMING CONTROL
SRD*
SWR*
Y0 - Y7
CR/CB (0 - 7)
A0 - A7
ANC*
RD*
WR*
RESET*

Figure 1. Detailed Block Diagram.

Circuit Description

Input Lookup Table RAMs

R0–R7, G0–G7, and B0–B7 are latched on the rising edge of CLOCK while CLOCK/2 is a logical one. R0–R7 address the red 256 x 8 lookup table RAM, G0–G7 address the green 256 x 8 lookup table RAM, and B0–B7 address the blue 256 x 8 lookup RAM. The outputs of the lookup table RAMs drive the RGB to Y/Cr/Cb color conversion circuitry. (See Figure 1.)

Note that gamma-corrected RGB data must be used for conversion to the YCrCb color space. The three input lookup table RAMs may be used to provide gamma correction on the R0–R7, G0–G7, and B0–B7 inputs in the event that they contain linear (rather than gamma-corrected) RGB data.

The lookup table RAMs are not dual-ported, so MPU accesses have priority over pixel accessing. During MPU access to the color palette RAMs, the lookup table RAM outputs are undefined and invalid.

The lookup table RAMs are not initialized following a reset condition or power-up sequence.

RGB to YCrCb Matrix

The output of the lookup table RAMs drives the RGB to YCrCb matrix. The selected RGB to YCrCb conversion is determined by the command register and is either:

analog coefficient matrix:

$$Y = 0.299R + 0.587G + 0.114B$$

$$Cr = 0.500R - 0.419G - 0.081B + 128$$

$$Cb = -0.169R - 0.331G + 0.500B + 128$$

or digital coefficient matrix:

$$Y = (77/256)R + (150/256)G + (29/256)B$$

$$Cr = (131/256)R - (110/256)G - (21/256)B + 128$$

$$Cb = -(44/256)R - (87/256)G + (131/256)B + 128$$

The analog coefficient matrix can handle RGB data ranges of 1–254 or 16–235. The digital coefficient matrix can only handle RGB data ranges of 16–235. If the RGB data has a range of 0 to 255 (such as data in a graphics frame buffer), the lookup table RAMs may also be used to compress the RGB data range to 16 to 235 (or 1–254), in addition to providing gamma correction.

ROM lookup tables are used to perform the multiplications, and for the analog matrix, 5 bits of fractional data are maintained. The final result is rounded to 8 bits as specified by command register_1. Note the digital matrix maintains full precision (8 bits of fractional data).

The output range of matrix is selected by the CR04 command bit:

(0) Y = 16 to 235; Cr and Cb = 16 to 240

or

(1) Y = 1 to 254; Cr and Cb = 1 to 254

If the CR04 command bit is a logical one, then if the Y, Cr, or Cb output value is zero, it is made 1; if the Y, Cr, or Cb output value is 255, it is made 254.

If the CR04 command bit is a logical zero, then if the Y output value is 0–15, it is made 16; if the Y output value is 236–255, it is made 235. If the Cr or Cb output value is 0–15, it is made 16; if the Cr or Cb output value is 241–255, it is made 240.

This YCrCb range limiting also applies when inputting YCrCb data via the RGB inputs, bypassing the RGB to YCrCb matrix. Note that the lookup table RAMs are still used when inputting YCrCb data via the RGB inputs. The YCrCb range limiting occurs after the lookup table RAMs.

To ease system timing requirements, the RGB, YCrCb, CbFLAG, H, V, and F inputs have the same relative input timing.

Y Low-Pass Filter

The Y channel has a digital low-pass filter after the RGB to YCrCb matrix. Command bit CR00 specifies whether or not to bypass the low-pass filter.

Cr/Cb Filters and Multiplexer

Digital filters low-pass and subsample the Cr and Cb data, reducing the sampling rate of the Cr and Cb data to 1/2 the Y rate, generating 4:2:2 data. The decimated Cr and Cb data is multiplexed together by the Cr/Cb multiplexer. The multiplexer is controlled by the CbFLAG signal.

CbFLAG is latched on the rising edge of CLOCK while CLOCK/2 is a logical one.

Circuit Description (continued)

YCrCb Multiplexer

The YCrCb multiplexer multiplexes the Y and multiplexed Cr/Cb video data into an 8-bit data stream. The timing of the multiplexer is controlled by the internal video timing circuitry.

Timing Insertion

The Bt291 inputs horizontal blanking (H), vertical blanking (V), and even/odd frame (F) timing information. H, V, and F are latched on the rising edge of CLOCK while CLOCK/2 is a logical one and pipelined to maintain synchronization with the RGB data inputs. All changes in state of the V and F inputs must occur with a change of state in H. (Refer to Figures 2–7.)

EAV and SAV Sequences

A zero-to-one transition on the H input triggers an EAV (end of active video) sequence that is output onto D0-D7, overriding YCrCb color data (refer to Figure 9). A one-to-zero transition on the H input triggers a SAV (start of active video) sequence that is output onto D0-D7, overriding any Ancillary data (refer to Figure 10. The pipeline delay of the H input is internally adjusted relative to the RGB inputs so that the SAV and EAV sequences start at the proper location.

The EAV and SAV output sequences are as follows:

$FF $00 $00 $xx

$FF is output with the start of horizontal blanking during the EAV sequence. $xx is output with the end of horizontal blanking during the SAV sequence.

$xx is defined as follows:

D7 = logical one
D6 = F input (F = 1 for field 2; F = 0 for field 1)
D5 = V input (V = 1 during vertical blanking)
D4 = H (H = 0 at SAV, H = 1 at EAV)
D3–D0 = protection bits

The protection bits are derived from V, H, and F as follows:

F = D6	V = D5	H = D4	D3 - D0
0	0	0	0000
0	0	1	1101
0	1	0	1011
0	1	1	0110
1	0	0	0111
1	0	1	1010
1	1	0	1100
1	1	1	0001

D1–D3 are protection bits (Hamming code 6:3) while D0 is an even parity bit for D1–D6.

Line Count Ancillary Sequence

If the line count ANC bit in the command register is set, the Bt291 will generate an Ancillary (ANC) sequence indicating the line number of the scan line about to be sent. This occurs during the six words preceding the SAV sequence. The Line Count ANC output sequence is as follows:

$00 $FF $FF TT MM LL

TT is the automatic Line Count ANC identification code, and is specified by the Line Count register.

Byte TT
D7 = Line Count register bit A7 D6 = Line Count register bit A6 D5 = Line Count register bit A5 D4 = Line Count register bit A4 D3 = Line Count register bit A3 D2 = Line Count register bit A2 D1 = Line Count register bit A1 D0 = odd parity bit

The Bt291 generates an odd parity bit for the Line Count register contents automatically.

Circuit Description (continued)

The MM and LL data words are defined as:

Byte MM	Byte LL
D7 = 0	D7 = 0
D6 = L11	D6 = L5
D5 = L10	D5 = L4
D4 = L9	D4 = L3
D3 = L8	D3 = L2
D2 = L7	D2 = L1
D1 = L6	D1 = L0
D0 = odd parity bit	D0 = odd parity bit

An internal 12-bit vertical counter (L0 is the least significant bit) is used to determine the line number. The H, V, and F inputs are used to control the vertical counter. Command bit CR10 specifies whether line counting is to conform to SMPTE/NTSC or EBU/CCIR standards.

If CR10 is a logical zero (SMPTE/NTSC compatible), the vertical counter is reset to $001 when the V input makes a transition from a logical zero to a logical one while the F input is a logical one. The F input must change state only at the beginning of the vertical sync interval, and have the same timing as the H input. The V input must also have the same timing as the H input (i.e., all changes in state of the V and F inputs must occur with a change of state in H). Field 1 will have 262 lines and field 2 will have 263 lines (assuming a 525-line interlaced system).

If CR10 is a logical one (EBU/CCIR compatible), the vertical counter is reset to $001 when the F input makes a transition from a logical one to a logical zero. The F input must change state only at the beginning of the vertical sync interval, and have the same timing as the H input. The V input must also have the same timing as the H input (i.e. all changes in state of the V and F inputs must occur with a change of state in H). Field 1 will have 312 lines and field 2 will have 313 lines (assuming a 625-line interlaced system).

The vertical counter increments when the H input makes a transition from a logical zero to a logical one.

Note that there are no Ancillary data words associated with the line count ANC sequence. If the automatic line count ANC is enabled, the ANC* output will go high six clock cycles earlier than indicated in Figure 10.

	525-Line 60 Field per Sec.	625-Line 50 Field per Sec.
Effective sampling frequency*		
Luminance (Y)	13.5 MHz	13.5 MHz
Color difference (Cr, Cb)	6.75 MHz	6.75 MHz
Luminance samples (Y) per total line	858	864
Color difference samples per total line (Cr, Cb)	429	432
Number of samples per digital active line		
Y	720	720
Cr, Cb	360	360
Analog to digital horizontal timing relationship		
start of digital blanking to start of analog sync	32 words	24 words
start of analog sync to end of digital blanking	244 words	264 words
digital blanking interval	276 words	288 words

*with CLOCK = 27 MHz. Sampling structure is orthogonal, line, field, and picture repetitive Cr and Cb samples co-sited with odd (1st, 3rd, 5th, etc.) Y samples in each line.

Table 1. Typical Operational Parameters.

Circuit Description (continued)

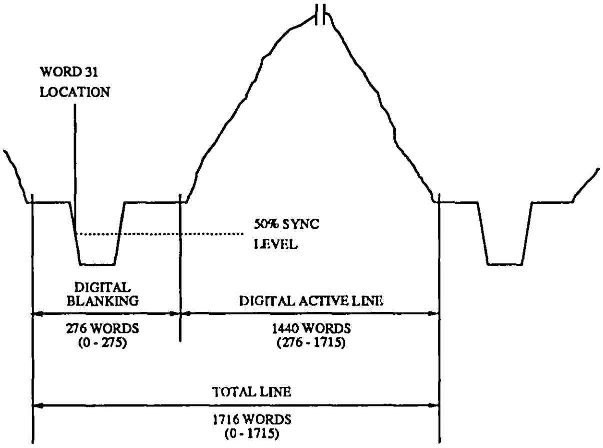

WORD 31
LOCATION
50% SYNC
LEVEL
DIGITAL
BLANKING
276 WORDS
(0 - 275)
DIGITAL ACTIVE LINE
1440 WORDS
(276 - 1715)
TOTAL LINE
1716 WORDS
(0 - 1715)

Figure 2. 525-Line, 60 Field/Sec. Horizontal Sync Relationship.

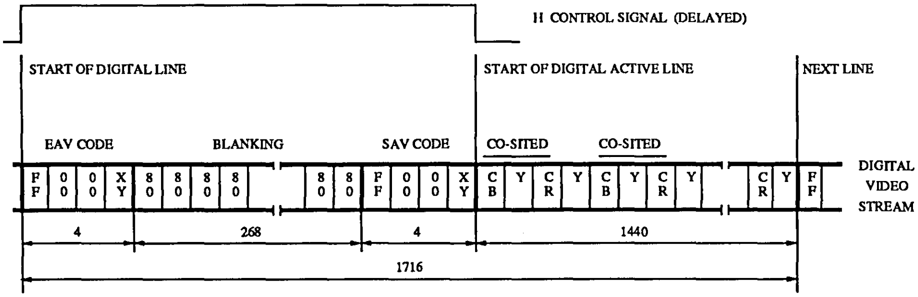

H CONTROL SIGNAL (DELAYED)
START OF DIGITAL LINE
START OF DIGITAL ACTIVE LINE
NEXT LINE
EAV CODE
BLANKING
SAV CODE
CO-SITED
CO-SITED
FF 00 00 XY 80 80 80 80 80 80 FF 00 00 XY CB Y CR Y CB Y CR Y CR Y FF
DIGITAL
VIDEO
STREAM
4
268
4
1440
1716

Figure 3. 525-Line, 60 Field/Sec. Digital Horizontal Blanking.

Circuit Description (continued)

YCrCb I/O Bus

A 16-bit bidirectional multiplexed YCrCb bus is provided for reading and writing active video data. The SRD* and SWR* inputs are used to synchronously read and write YCrCb data. SRD* and SWR* must be synchronous to CLOCK/2. (See Figure 8.)

Reading YCrCb Data

While SRD* is a logical zero, YCrCb information from the RGB to YCrCb matrix is output onto Y (0–7) and Cr/Cb (0–7) following the rising edge of CLOCK while CLOCK/2 is a logical one.

The YCrCb output range is selected by the CR04 command bit:

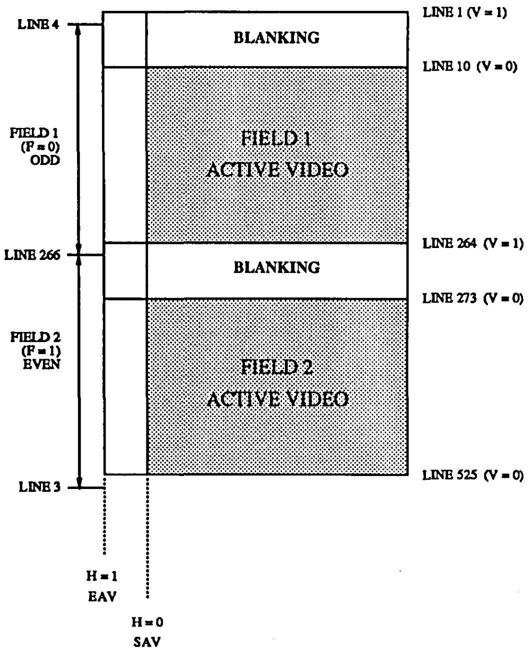
(0) Y = 16 to 235; Cr and Cb = 16 to 240

or

(1) Y = 1 to 254; Cr and Cb = 1 to 254

If the CR04 command bit is a logical one, then if the Y, Cr, or Cb output value is zero, it is made 1; if the Y, Cr, or Cb output value is 255, it is made 254.

If the CR04 command bit is a logical zero, then if the Y output value is 0–15, it is made 16; if the Y output value is 236–255, it is made 235. If the Cr or Cb output value is 0–15, it is made 16; if the Cr or Cb output value is 241–255, it is made 240.


LINE 4
LINE 1 (V = 1)
BLANKING
LINE 10 (V = 0)
FIELD 1 (F = 0) ODD
FIELD 1 ACTIVE VIDEO
LINE 264 (V = 1)
LINE 266
BLANKING
LINE 273 (V = 0)
FIELD 2 (F = 1) EVEN
FIELD 2 ACTIVE VIDEO
LINE 525 (V = 0)
LINE 3
H = 1 EAV
H = 0 SAV

LINE NUMBER	F	V	H (EAV)	H (SAV)
1 - 3	1	1	1	0
4 - 9	0	1	1	0
10 - 263	0	0	1	0
264 - 265	0	1	1	0
266 - 272	1	1	1	0
273 - 525	1	0	1	0

Figure 4. 525-Line, 60 Field/Sec. Vertical Timing.

Circuit Description (continued)

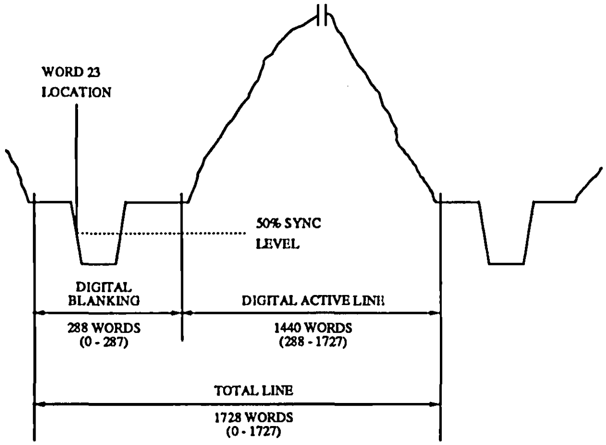

WORD 23
LOCATION
50% SYNC
LEVEL
DIGITAL
BLANKING
DIGITAL ACTIVE LINE
288 WORDS
(0 - 287)
1440 WORDS
(288 - 1727)
TOTAL LINE
1728 WORDS
(0 - 1727)

Figure 5. 625-Line, 50 Field/Sec. Horizontal Sync Relationship.

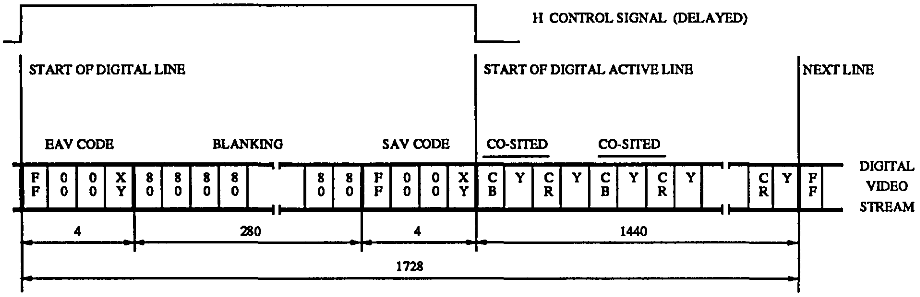

H CONTROL SIGNAL (DELAYED)
START OF DIGITAL LINE
START OF DIGITAL ACTIVE LINE
NEXT LINE
EAV CODE
BLANKING
SAV CODE
CO-SITED
CO-SITED
FF 00 00 XY 80 80 80 80 80 80 FF 00 00 XY CB Y CR Y CB Y CR Y CR Y FF
DIGITAL
VIDEO
STREAM
4
280
4
1440
1728

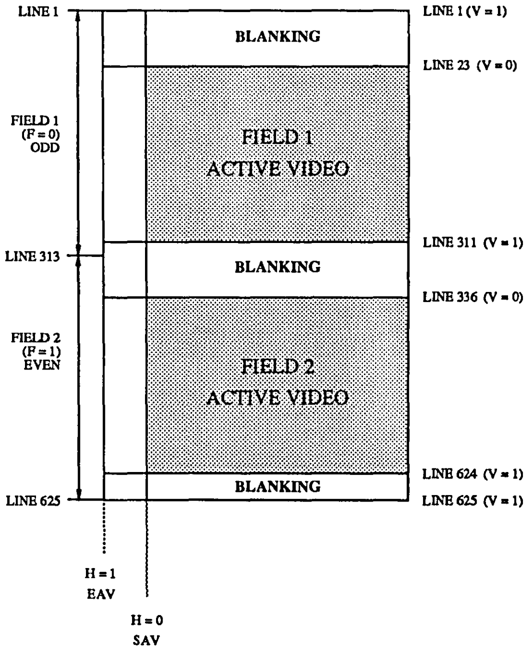
Figure 6. 625-Line, 50 Field/Sec. Digital Horizontal Blanking.

Circuit Description (continued)

525/60 systems	122T	720T	16T	
0H leading edge of line syncs, half-amplitude reference		digital active line period	0H	Next line
625/50 systems	132T	720T	12T	

T = one luminance sampling clock (74 ns nominal).

Table 2. Digital–Analog Timing Relationship.


LINE 1
LINE 1 (V = 1)
BLANKING
LINE 23 (V = 0)
FIELD 1 (F = 0) ODD
FIELD 1 ACTIVE VIDEO
LINE 311 (V = 1)
LINE 313
BLANKING
LINE 336 (V = 0)
FIELD 2 (F = 1) EVEN
FIELD 2 ACTIVE VIDEO
LINE 624 (V = 1)
BLANKING
LINE 625
LINE 625 (V = 1)
H = 1 EAV
H = 0 SAV

LINE NUMBER	F	V	H (EAV)	H (SAV)
1 - 22	0	1	1	0
23 - 310	0	0	1	0
311 - 312	0	1	1	0
313 - 335	1	1	1	0
336 - 623	1	0	1	0
624 - 625	1	1	1	0

Figure 7. 625-Line, 50 Field/Sec. Vertical Timing.

Circuit Description (continued)

If reading YCrCb data during the blanking intervals, Y will be either 1 (CR04 = logical one) or 16 (CR04 = logical zero); CrCb data will be 128.

Note that Y data will be 16 if command register bit CR06 is a logical one (regardless of the value of CR04) and CrCb data will be 128 if command register bit CR07 is a logical one.

If CbFLAG is a logical zero (and CLOCK/2 = 1), Cb data is output onto the CrCb bus during the next read cycle; if CbFLAG is a logical one (and CLOCK/2 = 1), Cr data is output during the next read cycle. This timing enables the CbFLAG status to match the data present on the CrCb (0–7) outputs. CbFLAG is latched on the rising edge of CLOCK while CLOCK/2 is a logical one.

While SRD* is a logical one, the YCrCb bus is three-stated. Note: SRD* must be synchronized to CLOCK externally for proper operation.

Writing YCrCb Data

While SWR* is a logical zero, YCrCb information (and CbFLAG) are latched on the rising edge of CLOCK while CLOCK/2 is a logical one (the RGB inputs are ignored). This YCrCb information is used to generate the D0–D7 output data, rather than the RGB inputs.

The YCrCb input range is selected by the CR04 command bit:

(0) Y = 16 to 235; Cr and Cb = 16 to 240

or

(1) Y = 1 to 254; Cr and Cb = 1 to 254

If the CR04 command bit is a logical one, then if the Y, Cr, or Cb input value is zero, it is made 1; if the Y, Cr, or Cb input value is 255, it is made 254.

If the CR04 command bit is a logical zero, then if the Y input value is 0–15, it is made 16; if the Y input value is 236–255, it is made 235. If the Cr or Cb input value is 0–15, it is made 16; if the Cr or Cb input value is 241–255, it is made 240.

Note that if command register bit CR06 is a logical one, the Y data will be made 16. CrCb data will be made 128 if command register bit CR07 is a logical one.

The CbFLAG input is used to specify whether Cr (CbFLAG = 0) or Cb (CbFLAG = 1) data is being latched via the CrCb bus.

Inputting Ancillary Data—Mode 0

The A1–A7 bus, along with the ANC* output and SAWR* input, are used to input Ancillary data, such as digital audio, teletext, etc. The Bt291 ensures that the ANC and its associated data block will not occupy the intervals reserved for EAV, SAV, or active video.

ANC* is a logical zero for CLOCK cycles that Ancillary data may be input into the Bt291 during horizontal blanking intervals (except when EAV, SAV, or automatic Line Count ANCs are being generated) and active video time during vertical blanking intervals. ANC* is output following the rising edge of CLOCK and its timing is relative to the A1–A7 inputs.

If both SAWR* and ANC* are a logical zero during the rising edge of CLOCK, the A1–A7 input data is accepted as Ancillary data on the rising edge of CLOCK. If ANC* or SAWR* are a logical one, A1–A7 are ignored (except while accessing the command register).

The Ancillary sequence input via A1–A7 and output onto D0–D7 is:

$00 $FF $FF TT MM LL xx xx. . .

where the A1–A7 inputs provide the TT, MM, LL, and $xx data. TT is the data identification code, MM and LL specify the Ancillary data word count, and xx are Ancillary data words.

The Bt291 automatically generates the three word preamble ($00, $FF, $FF). The preamble is generated after a high to low transition of SAWR* while ANC* is a logical zero.

Note that if more than one Ancillary sequence is to be transmitted during a digital blanking interval, the SAWR* input must be a logical one for at least three CLOCK cycles to allow the generation of the three word preamble ($00, $FF, $FF).

Ancillary data identification codes (TT) are represented by a 7-bit word, input via A1–A7. The A0 input is ignored, and the Bt291 internally generates an odd parity bit for the D0 data. This prevents the data identification codes from generating the $00 and $FF values reserved for timing reference purposes.

Circuit Description (continued)

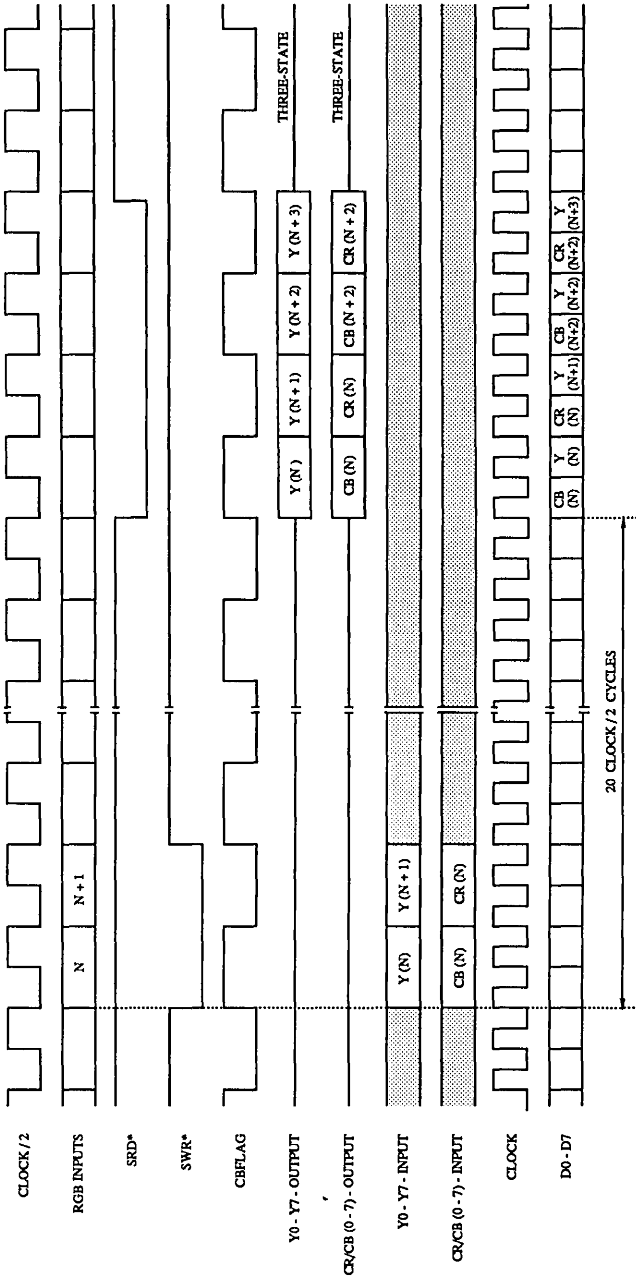

CLOCK / 2
RGB INPUTS
N
N + 1
SRD*
SWR*
CBFLAG
Y0 - Y7 - OUTPUT
Y (N)
Y (N + 1)
Y (N + 2)
Y (N + 3)
THREE-STATE
CR/CB (0 - 7) - OUTPUT
CB (N)
CR (N)
CB (N + 2)
CR (N + 2)
THREE-STATE
Y0 - Y7 - INPUT
Y (N)
Y (N + 1)
CR/CB (0 - 7) - INPUT
CB (N)
CR (N)
CLOCK
D0 - D7
CB (N)
Y (N)
CR (N)
Y (N+1)
CB (N+2)
Y (N+2)
CR (N+2)
Y (N+3)
20 CLOCK / 2 CYCLES

Figure 8. Reading/Writing Active Video Data.

Circuit Description (continued)

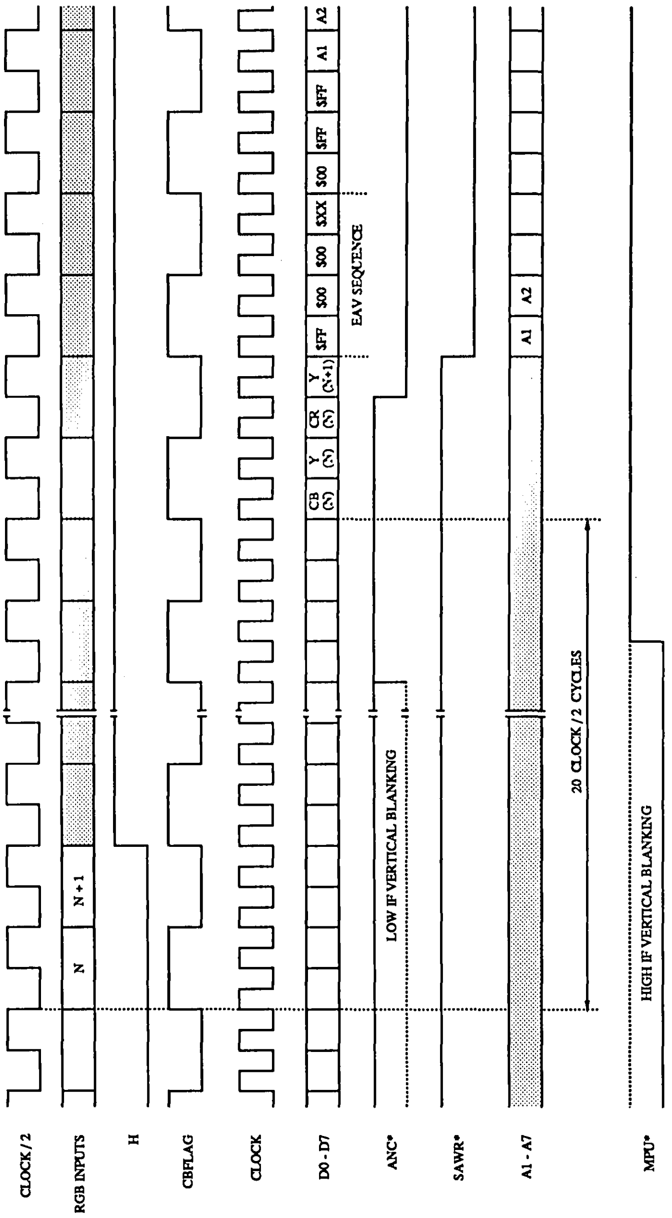

CLOCK/2
RGB INPUTS
H
CBFLAG
CLOCK
D0 - D7
ANC*
SAWR*
A1 - A7
MPU*
N
N+1
CB (N)
Y (N)
CR (N)
Y (N+1)
$FF
$00
$00
$XX
$00
$FF
$FF
A1
A2
A1
A2
EAV SEQUENCE
LOW IF VERTICAL BLANKING
20 CLOCK/2 CYCLES
HIGH IF VERTICAL BLANKING

Figure 9. EAV Sequence and Writing Ancillary Data.

Circuit Description (continued)

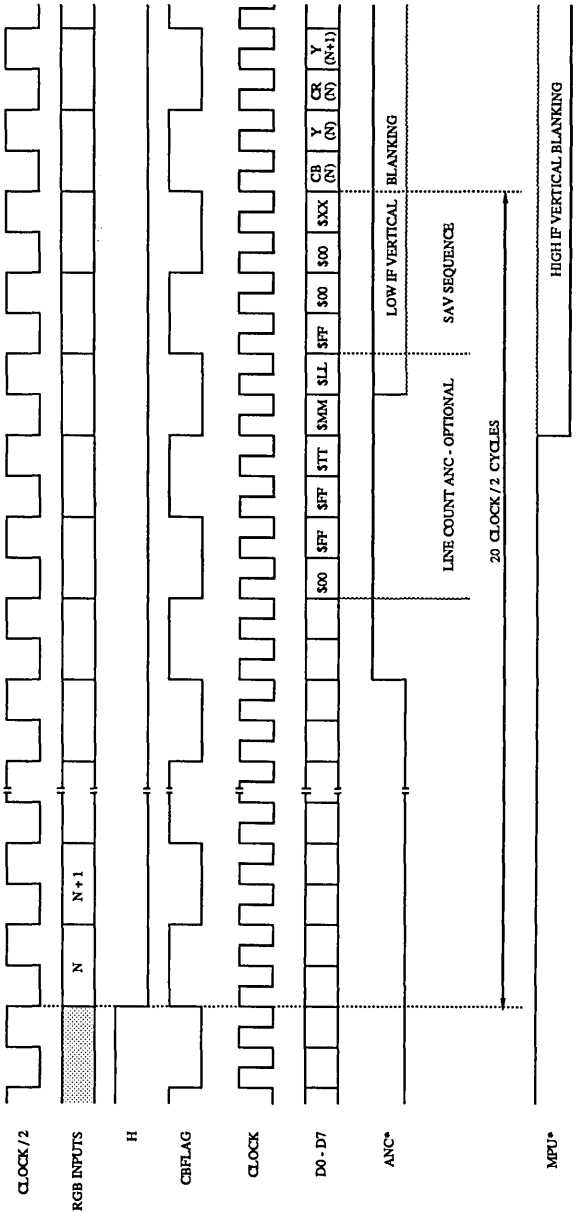

CLOCK/2
RGB INPUTS
H
CBFLAG
CLOCK
D0 - D7
ANC*
MPU*
N
N+1
$00
$FF
$FF
$TT
$MM
$LL
$FF
$00
$00
$XX
CB (N)
Y (N)
CR (N)
Y (N+1)
LOW IF VERTICAL BLANKING
SAV SEQUENCE
LINE COUNT ANC - OPTIONAL
20 CLOCK/2 CYCLES
HIGH IF VERTICAL BLANKING

Figure 10. SAV Sequence.

Circuit Description (continued)

Byte TT
D7 = A7
D6 = A6
D5 = A5
D4 = A4
D3 = A3
D2 = A2
D1 = A1
D0 = odd parity bit (A0 = x)

The Ancillary data word count is specified as a 12-bit binary value, with a range of 1 to 1440. Two 6-bit values (MM) and (LL) are written, the most significant 6 bits (MM) first.

The Ancillary data word count is represented as two 6-bit words, input via A1–A6. The A0 and A7 inputs are ignored. The Bt291 internally generates an odd parity bit for the D0 data and internally sets the D7 bit to a logical zero. This prevents the data from generating the $00 and $FF values reserved for timing reference purposes. The most significant 6 bits are transmitted first.

Byte MM	Byte LL
D7 = 0 (A7 = x)	D7 = 0 (A7 = x)
D6 = M5 (A6)	D6 = L5 (A6)
D5 = M4 (A5)	D5 = L4 (A5)
D4 = M3 (A4)	D4 = L3 (A4)
D3 = M2 (A3)	D3 = L2 (A3)
D2 = M1 (A2)	D2 = L1 (A2)
D1 = M0 (A1)	D1 = L0 (A1)
D0 = odd parity bit (A0 = x)	D0 = odd parity bit (A0 = x)

Ancillary data words are represented as one or more 7-bit words, input via A1–A7. The A0 input is ignored, and the Bt291 internally generates an odd parity bit for the A0 data. This prevents the data from generating the $00 and $FF values reserved for timing reference purposes.

Byte(s) xx
D7 = A7
D6 = A6
D5 = A5
D4 = A4
D3 = A3
D2 = A2
D1 = A1
D0 = odd parity bit (A0 = x)

Ancillary sequences can occur multiple times per scan line if different blocks of data are transmitted.

SAWR* and A1–A7 are latched on the rising edge of CLOCK. When not transmitting Ancillary information (ANC* = logical zero, SAWR* = logical one), a value of 128 is transmitted.

Inputting Ancillary Data—Mode 1

Unlike Mode 0, in this mode the A0–A7 data are output onto D0–D7 directly. No three word ANC preamble is generated, no parity information is generated, and no checking is done to ensure the reserved words $00 and $FF are not transmitted. It is the responsibility of external circuitry to properly generate the Ancillary sequence. There is no change in the pipeline delay from the Mode 0 operation.

Ancillary sequences can occur multiple times per scan line if different blocks of data are transmitted.

SAWR* and A0–A7 are latched on the rising edge of CLOCK. When not transmitting Ancillary information (ANC* = logical zero and SAWR* = logical one), a value of 128 is transmitted.

Ancillary Data Blocks (NTSC)

During horizontal blanking, small blocks of data, up to 268 words in total length (including the ANC preamble(s)), can be transmitted within a horizontal blanking interval. If the Line Count ANC is enabled, 262 words are available (including the ANC preamble (s)).

During vertical blanking, large blocks of data, up to 1440 words in total length (including the ANC preamble(s)), may be transmitted in the interval starting with the end of the SAV and terminating with the beginning of EAV.

Note that in Ancillary mode 1, three less words are available per horizontal or vertical blanking interval.

Ancillary Data Blocks (CCIR)

During horizontal blanking, small blocks of data, up to 280 words in total length (including the ANC preamble(s)), can be transmitted within a horizontal blanking interval. If the Line Count ANC is enabled, 274 words are available (including the ANC preamble (s)).

Circuit Description (continued)

During vertical blanking, large blocks of data, up to 1440 words in total length (including the ANC preamble(s)), may be transmitted in the interval starting with the end of the SAV and terminating with the beginning of EAV.

Note that in Ancillary mode 1, three less words are available per horizontal or vertical blanking interval.

D0–D7 Outputs

Video data is output onto D0–D7 following the rising edge of CLOCK. Command bit CR11 is logically gated with the OE* input, and the resulting value is used to control three-stating the D0–D7 outputs asynchronously to the clocks as described in the Pin Descriptions section.

The output sequence of YCrCb color data is:

Cb Y Cr [Y] ...

where the three words Cb, Y, Cr refer to co-sited samples, the following word [Y] being an isolated luminance sample. Note that Y data will be 16 if command register bit CR06 is a logical one and Cr/Cb data will be 128 if command register bit CR07 is a logical one.

Note that the Bt291 ensures that color data does not generate $00 or $FF to avoid timing errors in the received data.

During horizontal and vertical digital blanking intervals (except for EAV and SAV sequences), the Bt291 outputs 128 if no Ancillary information is being transmitted.

RS1, RS0	CR17, CR16	ADDR0–ADDR7	Accessed by MPU
00	xx	$xx	address register
01	00	$00	red RAM location $00
01	00	$01	red RAM location $01
:	:	:	:
01	00	$FF	red RAM location $FF
01	01	$00	blue RAM location $00
01	01	$01	blue RAM location $01
:	:	:	:
01	01	$FF	blue RAM location $FF
01	10	$00	green RAM location $00
01	10	$01	green RAM location $01
:	:	:	:
01	10	$FF	green RAM location $FF
10	xx	$00	command register_0
10	xx	$01	command register_1
10	xx	$02	line count ANC register
10	xx	$03	reserved
:	:	:	:
10	xx	$FF	reserved
11	xx	$xx	reserved

Table 3. Internal Register Addressing.

Circuit Description (continued)

MPU Interface

The Bt291 supports a standard MPU interface (A0–A7, RD*, WR*, MPU*, RS0, and RS1).

The MPU* output indicates when the MPU may access the Bt291 via the A0–A7 pins. A logical zero indicates MPU accesses may be done without contention with Ancillary data timing.

RS0 and RS1 are used to select address register (logical zero) or RAM location or control register specified by the address register (logical one), as shown in Table 3. The 8-bit address register specifies which control register or RAM location the MPU is accessing, also seen in Table 3. The address register resets to $00 following a read or write cycle to location $FF. Write cycles to reserved addresses are ignored, read cycles from reserved addresses return invalid data.

The address register increments after each MPU read or write cycle (except when reading or writing to the address register), and is not initialized. ADDR0 is the least significant bit and corresponds to bit A0.

As the MPU shares the Ancillary bus with Ancillary information, care must be taken that the MPU does not attempt to access the internal registers and lookup table RAMs during the digital blanking intervals. The MPU* output signal may be used to provide arbitration; while MPU* is a logical zero, the MPU may access the Bt291 without contention with any Ancillary data.

The rising edge of WR* latches A0–A7 into the selected register or lookup table RAM location. While RD* is a logical zero, the contents of the selected register or lookup table RAM location are output onto A0–A7. Only one of the RD*, WR*, and SAWR* inputs should be asserted at a time to avoid bus contention.

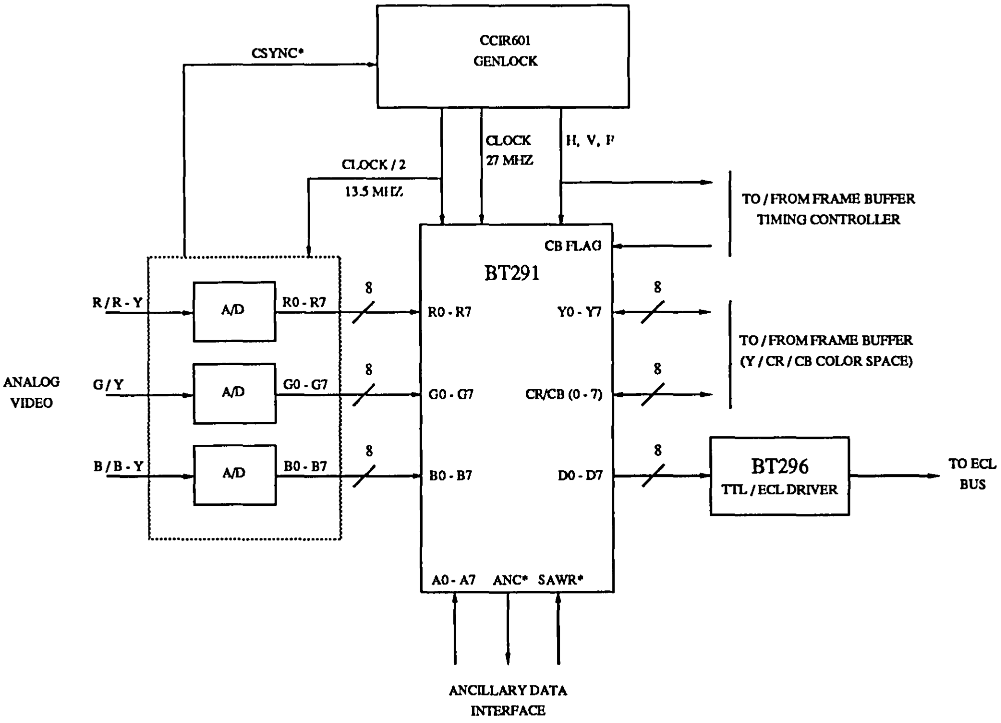

CCIR601
GENLOCK
CSYNC*
CLOCK 27 MHZ
H, V, F
CLOCK / 2
13.5 MHZ
TO / FROM FRAME BUFFER TIMING CONTROLLER
CB FLAG
BT291
ANALOG VIDEO
R/R-Y
G/Y
B/B-Y
A/D
A/D
A/D
R0 - R7
G0 - G7
B0 - B7
8
8
8
R0 - R7
G0 - G7
B0 - B7
Y0 - Y7
CR/CB (0 - 7)
D0 - D7
8
8
8
TO / FROM FRAME BUFFER (Y / CR / CB COLOR SPACE)
BT296
TTL / ECL DRIVER
TO ECL BUS
A0 - A7
ANC*
SAWR*
ANCILLARY DATA INTERFACE

Figure 11. Typical Application.

Circuit Description (continued)

Typical Application

Figure 11 shows the Bt291 in a typical application. Three A/D converters digitize three channels of analog RGB video.

The Bt291 converts this digital video information into 16-bit multiplexed Y and Cr/Cb data for loading into the frame buffer. Data from the frame buffer may also be clocked into the Bt291.

The Bt291 formats the YCrCb data, inserting the necessary timing signals, for driving the Bt296 TTL-to-ECL driver.

A 24-bit frame buffer may also drive the RGB inputs, while the A0–A7 inputs provide Ancillary data. In this instance, the YCrCb I/O bus would not be used, as shown in Figure 12.

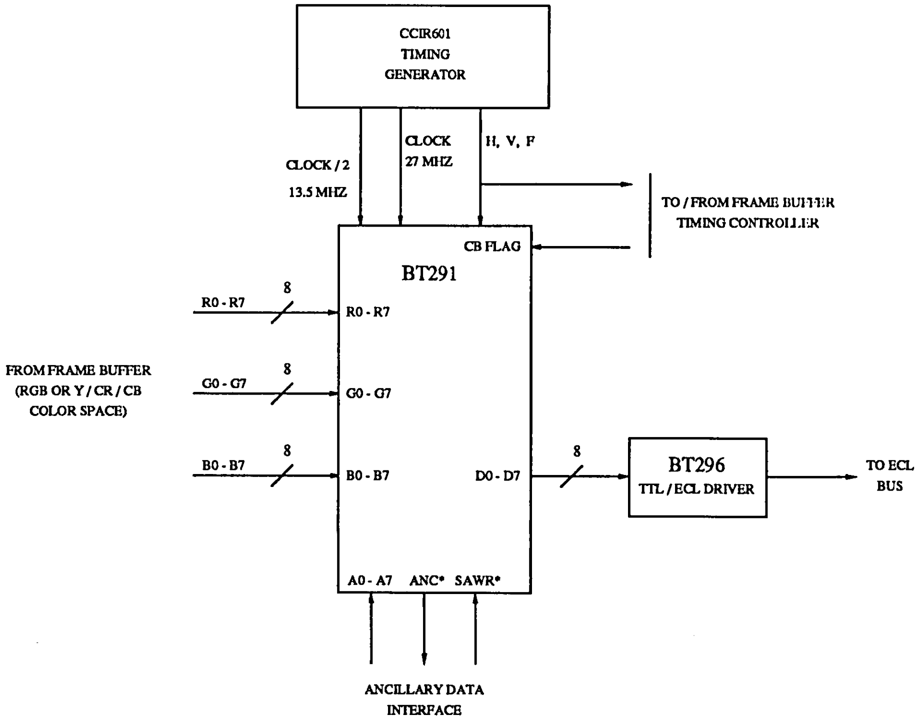

CCIR601
TIMING
GENERATOR
CLOCK / 2
13.5 MHZ
CLOCK
27 MHZ
H, V, F
TO / FROM FRAME BUFFER
TIMING CONTROLLER
CB FLAG
BT291
8
R0 - R7
R0 - R7
FROM FRAME BUFFER
(RGB OR Y / CR / CB
COLOR SPACE)
8
G0 - G7
G0 - G7
8
B0 - B7
B0 - B7
D0 - D7
8
BT296
TTL / ECL DRIVER
TO ECL
BUS
A0 - A7
ANC*
SAWR*
ANCILLARY DATA
INTERFACE

Figure 12. Typical Application.

Internal Registers

Command Register_0

This command register may be written to or read by the MPU at any time and is initialized to $03 following a reset condition. CR00 is the least significant bit and corresponds to bit A0.

CR07	Cr/Cb blanking enable (0) normal operation (1) set Cr/Cb data to 128	A logical one forces the Cr/Cb data from the color matrix to 128, and also forces Cr/Cb data output onto D0–D7 to 128.
CR06	Y blanking enable (0) normal operation (1) set Y data to 16	A logical one forces the Y data from the color matrix to 16, and also forces Y data output onto D0–D7 to 16.
CR05	Line count ANC enable (0) no line count ANC (1) automatic line count ANC	A logical one enables a Line Count ANC to be automatically sent, using the six words prior to the SAV sequence. A logical zero disables transmitting the Line Count ANC.
CR04	YCrCb range (0) Y = 16 to 235, Cr/Cb = 16 to 240 (1) Y, Cr, Cb = 1 to 254	This bit specifies the range of Y, Cr, and Cb for the output of the RGB to YCrCb matrix and the YCrCb I/O bus (when inputting or outputting color data). Typically, mode (0) should be used. Regardless of the selection, there is no change in the pipeline delay.
CR03	RGB or YCrCb input select (0) RGB (1) YCrCb	This bit specifies whether the RGB inputs are inputting RGB or YCrCb color information. Y information is input via the G0–G7 inputs, Cr information is input via the R0–R7 inputs, and Cb information is input via the B0–B7 inputs. If inputting YCrCb information, the RGB-to-YCrCb matrix is bypassed; however, the range specified by command bit CR04 is still used. Regardless of the selection, there is no change in the pipeline delay.
CR02 , CR01	Cr/Cb decimation filters select (00) use 3-tap filters (01) use 13-tap filters (10) reserved (11) bypass filters	These bits specify whether or not to bypass the Cr/Cb decimation filters and which decimation filter to use. If bypassed, the Cr/Cb multiplexer performs the actual decimation of the Cr and Cb data. Regardless of the selection, there is no change in the pipeline delay. Typically, the 13-tap filters should be used.
CR00	Y low pass filter bypass enable (0) use filter (1) bypass filter	This bit specifies whether or not to bypass the Y low pass filter. Regardless of the selection, there is no change in the pipeline delay.

Internal Registers (continued)

Command Register_1

This command register may be written to or read by the MPU at any time and is initialized to $3A following a reset condition. CR10 is the least significant bit and corresponds to bit A0.

CR17, CR16	Lookup table RAM select (00) red lookup table RAM (01) blue lookup table RAM (10) green lookup table RAM (11) reserved	These bits specify which lookup table RAM the MPU is accessing. NOTE: This decode differs from the Bt294 command bits CR03 and CR02.
CR15	Matrix coefficient select (0) analog matrix (1) digital matrix	This bit selects which set of coefficients to use in the RGB-to-YCrCb matrix, as described in the text. Typically, the digital matrix should be used. Regardless of the selection, there is no change in the pipeline delay.
CR14, CR13	Rounding select (00) normal rounding (01) even rounding (10) reserved (11) Dynamic Rounding™	This bit specifies the type of rounding used. Regardless of the selection, there is no change in the pipeline delay. (00) specifies round up if the fractional data is ≥ 0.5. If the fractional data is < 0.5, the number will be rounded down. (01) specifies round up if the fractional data = 0.5 and the rounded result will be an even number (LSB = 0) or if the fractional data is > 0.5. If the fractional data is < 0.5, the number will be rounded down. (11) specifies to use Dynamic Rounding™, where the fractional data is compared to a random number, and the result (1 bit) added to the 8 bits of color data. If the fractional data = 0, no rounding is done. R, G, and B each have their own random number generator. Typically, this mode should be used. Dynamic Rounding™ is used under license from Quantel Limited.
CR12	Ancillary input format (0) mode 0 (1) mode 1	This bit specifies the operation of inputting Ancillary data. Refer to text for details. Typically, mode (0) should be used.
CR11	D0–D7 output disable (0) enable D0–D7 outputs (1) disable D0–D7 outputs	This bit is logically gated with the OE* input pin, and the resulting value is used to control three-stating the D0–D7 outputs.

Internal Registers (continued)

Command Register_1 (continued)

CR10	Vertical counter operation (0) SMPTE/NTSC compatible (1) EBU/CCIR compatible	This bit specifies whether the vertical counter scan line numbering for the Line Count ANC function is to be SMPTE/NTSC (logical zero) or EBU/CCIR (logical one) compatible. During SMPTE/NTSC compatibility, scan line number one is the first scan line during vertical blanking in digital field 2. During EBU/CCIR compatibility, scan line number one is the first scan line during vertical sync in digital field 1.

Line Count ANC Register

The 8-bit Line Count register may be written to or read by the MPU at any time and is initialized to $00 following a reset condition. A0 is the least significant bit.

This register specifies the Ancillary data ID value (TT) of the automatic Line Count ANC.

Bit A0 is always a logical zero. MPU data written to bit A0 is ignored.

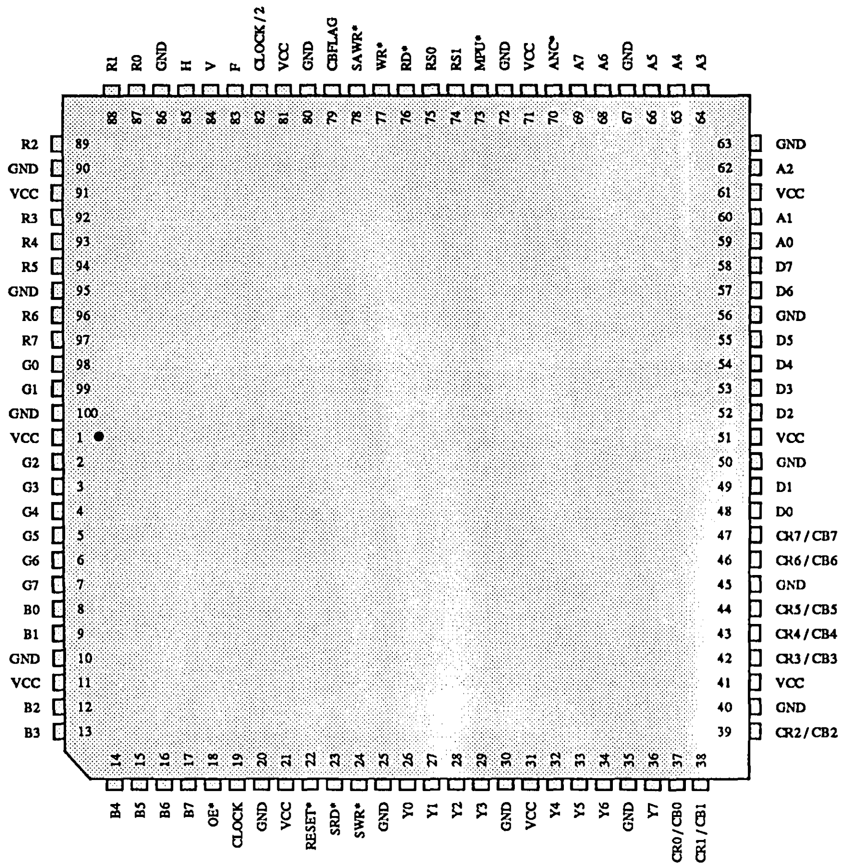
Pin Descriptions

Pin Name	Description
Y0–Y7	Y data inputs/outputs (TTL compatible). Y information is input or output via these pins depending on the value of SWR* and SRD*. Y0 is the least significant bit. If inputting Y data, it is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. If outputting Y data, it is output following the rising edge of CLOCK while CLOCK/2 is a logical one.
CR/Cb (0–7)	Cr/Cb data inputs/outputs (TTL compatible). Multiplexed Cr and Cb information is input or output via these pins depending on the value of SWR* and SRD*. CrCb0 is the least significant bit. If inputting Cr/Cb data, it is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. If outputting Cr/Cb data, it is output following the rising edge of CLOCK while CLOCK/2 is a logical one.
SWR*	Synchronous write control input (TTL compatible). A logical zero enables Y/Cr/Cb data to be input via the Y0–Y7 and Cr/Cb (0–7) pins. Both SRD* and SWR* should not be asserted simultaneously.
SRD*	Synchronous read control input (TTL compatible). A logical zero enables Y/Cr/Cb data to be output onto the Y0–Y7 and Cr/Cb (0–7) pins. Both SRD* and SWR* should not be asserted simultaneously.
A0–A7	Ancillary data inputs (TTL compatible). While both ANC* and SAWR* are a logical zero, A1–A7 are latched on the rising edge of CLOCK and output onto D0–D7. MPU data is also input and output via this bus. A0 is the least significant bit.
SAWR*	Ancillary write control input (TTL compatible). If ANC* is a logical zero, a logical zero on SAWR* will enable A1–A7 data to be latched. SAWR* is latched on the rising edge of CLOCK, and pipelined to maintain synchronization with the A1–A7 data. This pin should be a logical one if the Ancillary data transmission capabilities are not used.
ANC*	Ancillary output (TTL compatible). A logical zero indicates Ancillary data may be input via the A1–A7 pins. ANC* is output following the rising edge of CLOCK.
CbFLAG	CbFLAG control input (TTL compatible). It is latched on the rising edge of CLOCK while CLOCK/2 is a logical one.
R0–R7	Red inputs (TTL compatible). Red color information is input via these pins. Data is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. R0 is the least significant bit.
G0–G7	Green inputs (TTL compatible). Green color information is input via these pins. Data is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. G0 is the least significant bit.
B0–B7	Blue inputs (TTL compatible). Blue color information is input via these pins. Data is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. B0 is the least significant bit.
D0–D7	Data outputs (TTL compatible). Transmitted data is output onto D0–D7 following the rising edge of CLOCK. D0 is the least significant bit.
V, H, F	Video timing control inputs (TTL compatible). They are latched on the rising edge of CLOCK while CLOCK/2 is a logical one.

Pin Descriptions (continued)

<table>
<tr><th>Pin Name</th><th>Description</th></tr>
<tr><td>OE*</td><td>Output enable control input (TTL compatible). This input is logically gated with command bit CR11, and the result controls three-stating the D0–D7 outputs as follows:
<table>
<tr><th>CR11</th><th>OE*</th><th>D0–D7 Outputs</th></tr>
<tr><td>0</td><td>0</td><td>enabled</td></tr>
<tr><td>0</td><td>1</td><td>three-stated</td></tr>
<tr><td>1</td><td>0</td><td>three-stated</td></tr>
<tr><td>1</td><td>1</td><td>three-stated</td></tr>
</table></td></tr>
<tr><td>RESET*</td><td>Reset control input (TTL compatible). RESET* is sampled on the rising edge of CLOCK, and must be a logical zero for a minimum of three consecutive CLOCK cycles to reset the device. RESET* must be a logical one for normal operation.</td></tr>
<tr><td>RD*</td><td>MPU read control input (TTL compatible). While a logical zero, the contents of the control register/RAM location are output onto A0–A7 asynchronously to the clocks. If both RD* and WR* are asserted simultaneously, all signal pins are three-stated (note the device should be reset after three-stating the signal pins).</td></tr>
<tr><td>WR*</td><td>MPU write control input (TTL compatible). The rising edge of WR* latches the A0–A7 inputs into the control register/RAM location asynchronously to the clocks. If both RD* and WR* are a asserted simultaneously, all signal pins are three-stated (note the device should be reset after three-stating the signal pins).</td></tr>
<tr><td>RS0, RS1</td><td>Register select control inputs (TTL compatible). These bits specify whether the MPU is accessing the address register or the control register/RAM location specified by the address register. See Table 3.</td></tr>
<tr><td>MPU*</td><td>MPU access control output (TTL compatible). A logical zero indicates the MPU may access the internal registers without contention with Ancillary data. MPU* is output following the rising edge of CLOCK.</td></tr>
<tr><td>CLOCK</td><td>27 MHz clock input (TTL compatible). The clock must be present for the MPU to access the internal control registers.</td></tr>
<tr><td>CLOCK/2</td><td>13.5 MHz clock input (TTL compatible).</td></tr>
<tr><td>VCC</td><td>Power pins. All VCC pins must be connected together.</td></tr>
<tr><td>GND</td><td>Ground pins. All GND pins must be connected together.</td></tr>
</table>

Pin Descriptions (continued)


R1 88
R0 87
GND 86
H 85
V 84
F 83
CLOCK/2 82
VCC 81
GND 80
CBFLAG 79
SAWR* 78
WR* 77
RD* 76
RS0 75
RS1 74
MPU* 73
GND 72
VCC 71
ANC* 70
A7 69
A6 68
GND 67
A5 66
A4 65
A3 64
R2 89
GND 90
VCC 91
R3 92
R4 93
R5 94
GND 95
R6 96
R7 97
G0 98
G1 99
GND 100
VCC 1
G2 2
G3 3
G4 4
G5 5
G6 6
G7 7
B0 8
B1 9
GND 10
VCC 11
B2 12
B3 13
63 GND
62 A2
61 VCC
60 A1
59 A0
58 D7
57 D6
56 GND
55 D5
54 D4
53 D3
52 D2
51 VCC
50 GND
49 D1
48 D0
47 CR7/CB7
46 CR6/CB6
45 GND
44 CR5/CB5
43 CR4/CB4
42 CR3/CB3
41 VCC
40 GND
39 CR2/CB2
14 B4
15 B5
16 B6
17 B7
18 OE*
19 CLOCK
20 GND
21 VCC
22 RESET*
23 SRD*
24 SWR*
25 GND
26 Y0
27 Y1
28 Y2
29 Y3
30 GND
31 VCC
32 Y4
33 Y5
34 Y6
35 GND
36 Y7
37 CR0/CB0
38 CR1/CB1

Application Information

Cr/Cb Decimation Filters

The Cr/Cb linear phase decimation filters low-pass and subsample the Cr and Cb data to generate 4:2:2 YCrCb data.

If the CR04 command bit is a logical one, then then if the result is zero, it is made 1; if the result is 255, it is made 254. If the CR04 command bit is a logical zero, if the result is 0–15, it is made 16; if the result is 241–255, it is made 240.

The transfer function of the 13-tap filters is:

$$\begin{aligned}H(Z) = {} & 128/256 * Z0 \\ & + (80/25) * (Z^{-1} + Z^{+1}) \\ & + (-24/256)*(Z^{-3} + Z^{+3}) \\ & + (12/256)*(Z^{-5} + Z^{+5}) \\ & + (-6/256)*(Z^{-7} + Z^{+7}) \\ & + (3/256)*(Z^{-9} + Z^{+9}) \\ & + (-1/256)*(Z^{-11} + Z^{+11})\end{aligned}$$

Eighteen-bit precision (including sign and overflow) is maintained until the final output stage, then rounded to 8 bits as specified by command register_1. Figure 13 shows the transfer function of the 13-tap Cr and Cb decimation filters.

The transfer function of the 3-tap filters is:

$$\begin{aligned}H(Z) = {} & 128/256*Z^{0} \\ & + (64/256)*(Z^{-1} + Z^{+1})\end{aligned}$$

Twelve-bit precision (including sign and overflow) is maintained until the final output stage, then rounded to 8 bits as specified by command register_1.

During blanking periods, the input color data is undefined, possibly disturbing the computed color data at the beginning and end of active color data. To avoid this, if the 13-tap is filter selected, the 3-tap filter is automatically used at the beginning and end of the active line unless the 13-tap filter is available (i.e., the filter pipe is full). Regardless of the filter selection, the first active pixel per scan line to be decimated uses only the multiplexer (bypassing the digital filters).

Y Low-Pass Filter

Y may be optionally low-pass filtered using a 19-tap filter whose transfer function is:

$$\begin{aligned}H(Z) = {} & 116/128* Z0 \\ & + (12/128)*(Z^{-1} + Z^{+1}) \\ & + (-11/128)*(Z^{-2} + Z^{+2}) \\ & + (10/128)*(Z^{-3} + Z^{+3}) \\ & + (-8/128)*(Z^{-4} + Z^{+4}) \\ & + (6/128)*(Z^{-5} + Z^{+5}) \\ & + (-5/128)*(Z^{-6} + Z^{+6}) \\ & + (3/128)*(Z^{-7} + Z^{+7}) \\ & + (-2/128)*(Z^{-8} + Z^{+8}) \\ & + (1/128)*(Z^{-9} + Z^{+9})\end{aligned}$$

Seventeen-bit precision (including sign and overflow) is maintained until the final output stage, then rounded to 8 bits as specified by command register_1. If the CR04 command bit is a logical one, then if the result is zero, it is made 1; if the result is 255, it is made 254. If the CR04 command bit is a logical zero, then if the result is 0–15, it is made 16; if the result is 236–255, it is made 235. Figure 14 shows the transfer functions of the 19-tap Y filter.

During blanking periods, the input color data is undefined, possibly disturbing the computed color data at the beginning and end of active color data. To avoid this, the first and last 19 active pixels per scan line are not processed by the digital filter (bypassing the digital filter).

The Y data and control signals are pipelined to maintain synchronization with the Cr/Cb data. There is no change in the pipeline delay regardless of which filter (if any) is used.

Application Information (continued)

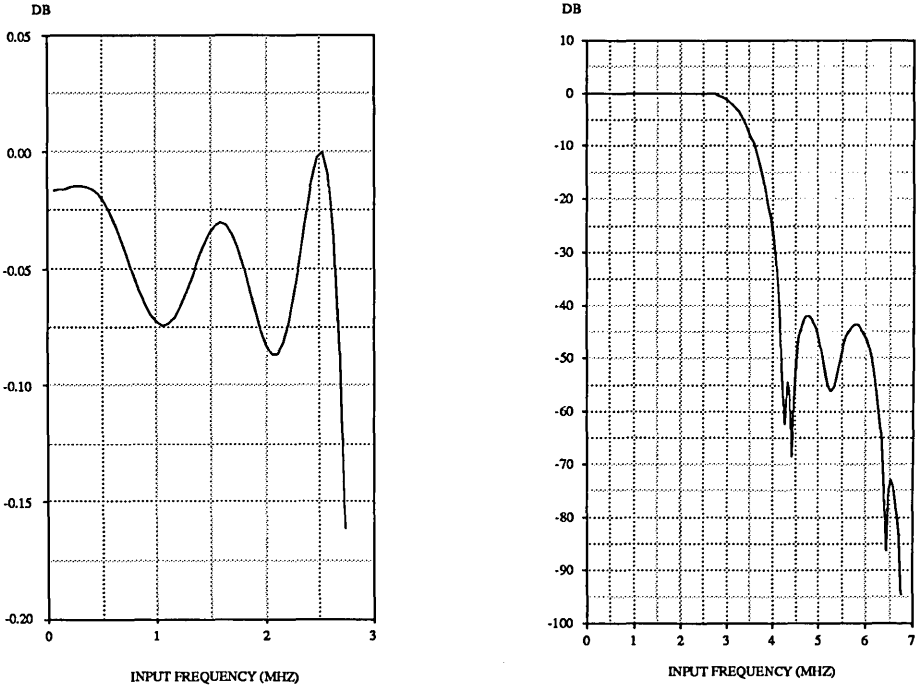


Figure 13. CrCb 13-Tap Pass-Band and Stop-Band Low-Pass / Decimation Filter Characteristics.

Application Information (continued)

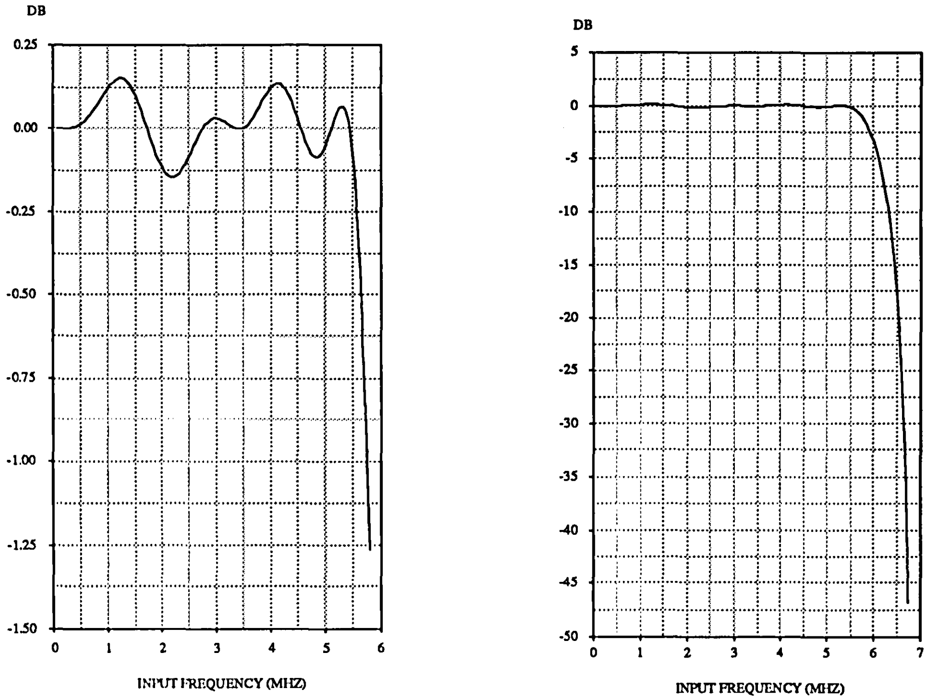


Figure 14. Y 19-Tap Pass-Band and Stop-Band Low-Pass Filter Characteristics.

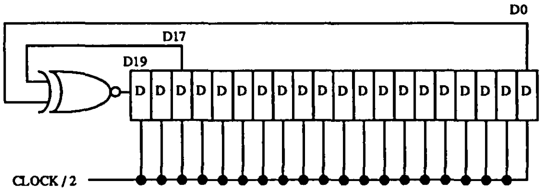


Figure 15. Random Number Generator.

Application Information (continued)

Random Number Generator

Figure 15 illustrates the random number generator used when Dynamic Rounding™ (used under license from Quantel Limited) is selected. Following a reset condition the random number generator is initialized to $00000.

As each YCrCb value in the analog matrix has 5 fractional data bits, 5 bits of random numbering is generated for each Y, Cr, and Cb value (random number bits D0, D4, and D8 correspond to the LSBs of Y, Cr, and Cb digital matrix fractional data).

Usage	Fractional Data Bits (MSB–LSB)
Y matrix (digital)	D7–D0
Y matrix (analog)	D7–D3
Cr matrix (digital)	D11–D4
Cb matrix (digital)	D15–D8
Cr matrix (analog)	D11–D7
Cb matrix (analog)	D15–D11
Y filter	D3–D0, D19–D17
CrCb filter (13-tap)	D19–D12
CrCb filter (3-tap)	D19, D18

As a single CrCb filter is used in a multiplexed fashion, a single CrCb random number generator is used. The 13-tap CrCb filter has 8 bits of fractional data. Random number bit D12 corresponds to the LSB of Cr and Cb fractional data.

Random number bits D19 and D18 are used for the 3-tap CrCb filter, which has 2 bits of fractional data.

The 19-tap Y filter has 7 fractional data bits, with the random number fractional bits shown above.

Typical Applications

Figure 16 shows the Bt291 and Bt294 being used with a 24-bit RGB frame buffer. The Bt291 and Bt294 provide another video I/O port to the imaging/graphics system.

Figure 17 shows the Bt291 and Bt294 being used with a 16-bit YCrCb frame buffer. The Bt291 and Bt294 provide another video I/O port to the imaging/graphics system.

ESD and Latchup Considerations

Correct ESD sensitive handling procedures are required to prevent device damage which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance.

Latchup can be prevented by assuring that all VCC pins are at the same potential, and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

PLCC Sockets

100-pin PLCC sockets for the Bt291 are available from:

McKenzie Technology
44370 Old Warm Springs Blvd.
Fremont, CA 94538
Phone: (415) 651-2700
FAX: (415) 651-1020
TLX: 910-240-6355
Part Number: PLCC-100-P-T

or

Yamaichi Electric Mfg.Co., LTD.
3-28-7 Nakamagome, Ohta-Ku,
Tokyo 143 Japan
Phone: 03-778-6161
FAX: 03-778-6181
U.S. Representative: (408) 452-0797

Application Information (continued)

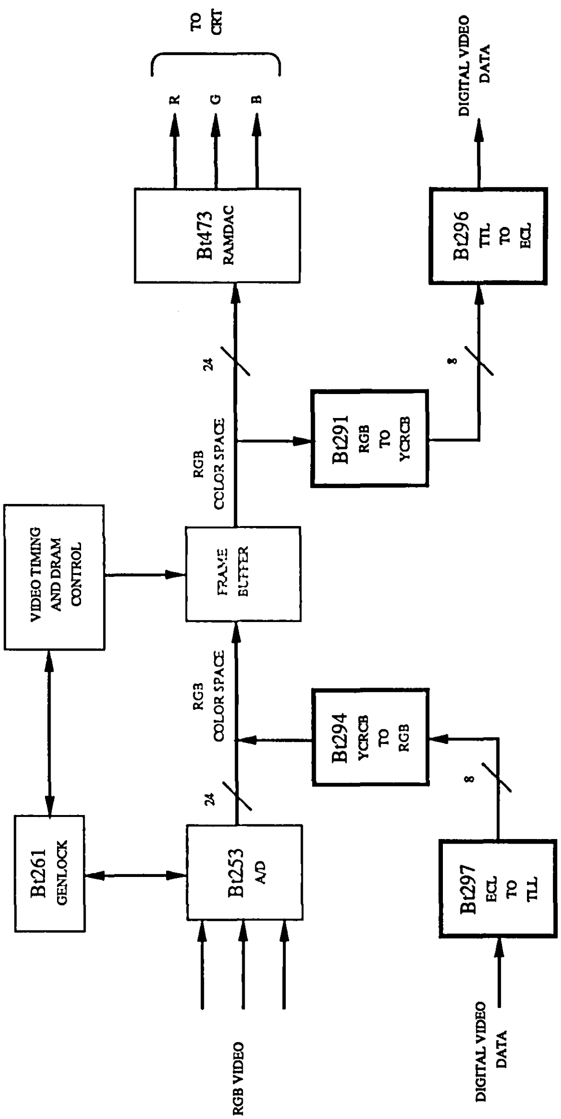

Bt261
GENLOCK
VIDEO TIMING
AND DRAM
CONTROL
RGB VIDEO
Bt253
A/D
24
RGB
COLOR SPACE
FRAME
BUFFER
RGB
COLOR SPACE
24
Bt473
RAMDAC
R
G
B
TO
CRT
Bt294
YCRCB
TO
RGB
Bt291
RGB
TO
YCRCB
DIGITAL VIDEO
DATA
Bt297
ECL
TO
TLL
8
8
Bt296
TTL
TO
ECL
DIGITAL VIDEO
DATA

Figure 16. Typical Application.

Application Information (continued)

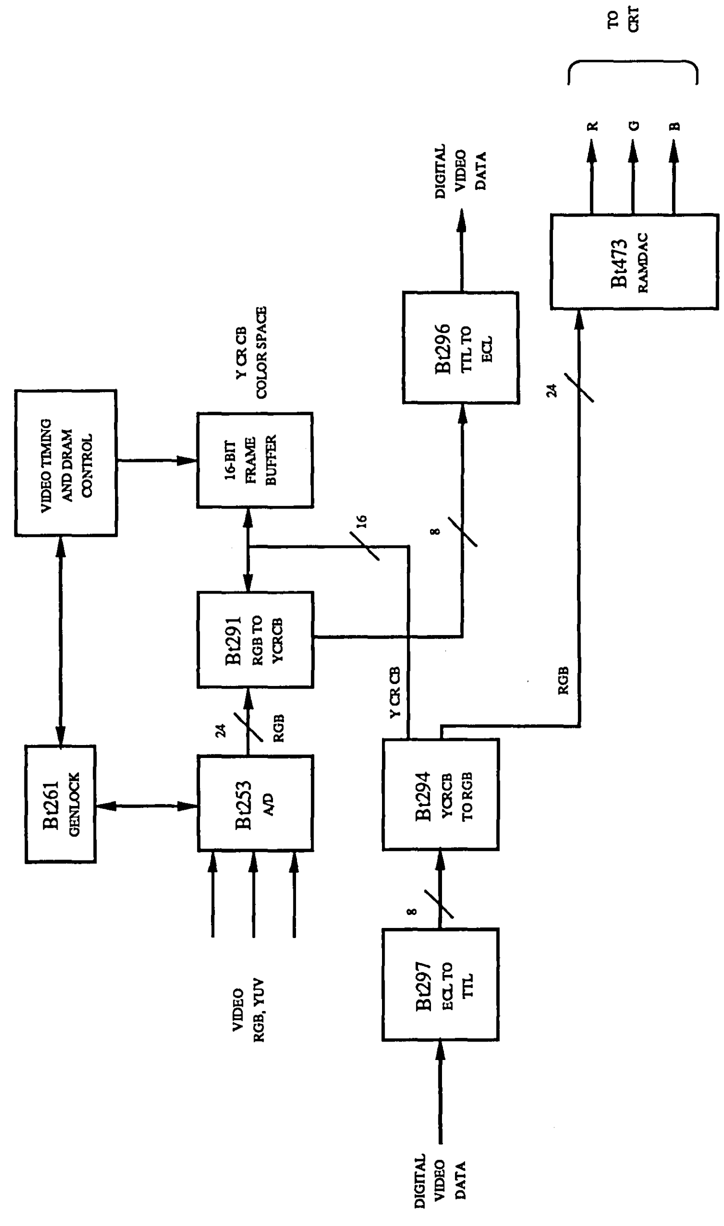

Bt261
GENLOCK
VIDEO TIMING
AND DRAM
CONTROL
VIDEO
RGB, YUV
Bt253
A/D
24
RGB
Bt291
RGB TO
YCRCB
16-BIT
FRAME
BUFFER
Y CR CB
COLOR SPACE
16
DIGITAL
VIDEO
DATA
Bt297
ECL TO
TTL
8
Bt294
YCRCB
TO RGB
Y CR CB
8
Bt296
TTL TO
ECL
DIGITAL
VIDEO
DATA
RGB
24
Bt473
RAMDAC
R
G
B
TO
CRT

Figure 17. Typical Application.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.5	5.00	5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND–0.5		VCC + 0.5	Volts
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	Volts
3-state Current (If Applicable)	IOZ			50	µA
Output Capacitance	COUT		20		pF

Test conditions (unless otherwise specified): "Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

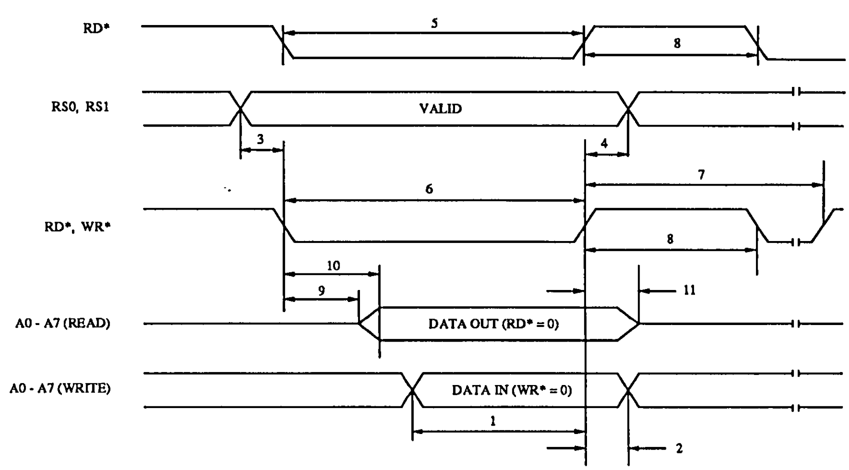
AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			27	MHz
MPU Write Data Setup Time	1	10			ns
MPU Write Data Hold Time	2	10			ns
RS0, RS1 Setup Time	3	10			ns
RS0, RS1 Hold Time	4	10			ns
RD* Low Time	5	1			Clock
WR* Low Time	6	100			ns
WR* Cycle Time	7	3			Clocks
RD*, WR* High Time	8	30			ns
RD* Asserted to Data Bus Driven	9	5			ns
RD* Asserted to Data Valid	10			100	ns
RD* Negated to Data Bus 3-Stated	11			25	ns
Clock/2 Setup Time	12	12			ns
Clock/2 Hold Time	13	5			ns
RGB (0–7), H, V, F, CbFLAG, Y/Cr/Cb (0–7)					
Setup Time	14	10			ns
Hold Time	15	4			ns
Y/Cr/Cb Output Delay	16	5		23	ns
A1–A7 Input Data, SAWR*					
Setup Time	17	10			ns
Hold Time	18	4			ns
SRD* Asserted to YCrCb Bus Driven				25	ns
SRD* Negated to YCrCb Bus 3-Stated				25	ns
MPU*, ANC* Output Delay	19	5		23	ns
D0–D7 Output Delay	20	5		23	ns
D0–D7					
Three-State Disable Time	21			25	ns
Three-State Enable Time	22			25	ns
Clock Cycle Time	23	37.04			ns
Clock Pulse Width High	24	15			ns
Clock Pulse Width Low	25	15			ns
VCC Supply Current*	ICC		220	tbd	mA

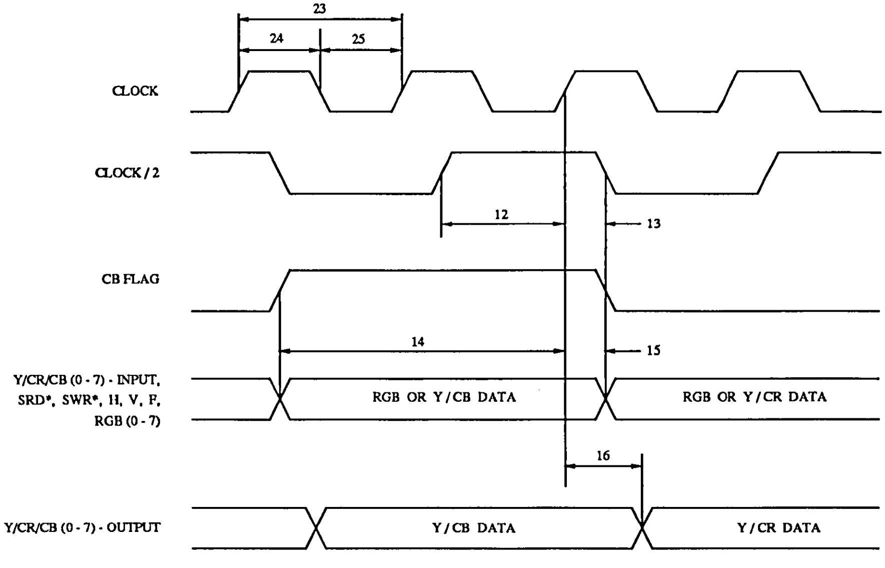
Test conditions (unless otherwise specified): "Recommended Operating Conditions." TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. ANC*, Yx, Crx/Cbx, Dx, MPU* output load ≤ 75 pF. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*At Fmax. ICC (typ) at VCC = 5.0 V. ICC (max) at VCC (max).

Timing Waveforms

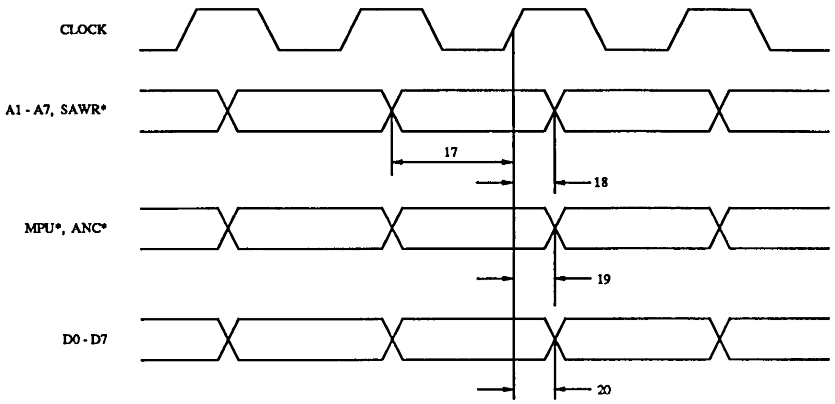

RD*
5
8
RS0, RS1
VALID
3
4
7
6
RD*, WR*
8
10
9
11
A0 - A7 (READ)
DATA OUT (RD* = 0)
A0 - A7 (WRITE)
DATA IN (WR* = 0)
1
2

MPU Read/Write Timing.

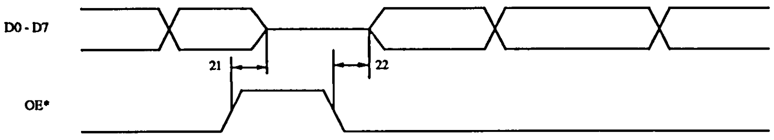

23
24
25
CLOCK
CLOCK / 2
12
13
CB FLAG
14
15
Y/CR/CB (0 - 7) - INPUT, SRD*, SWR*, H, V, F, RGB (0 - 7)
RGB OR Y / CB DATA
RGB OR Y / CR DATA
16
Y/CR/CB (0 - 7) - OUTPUT
Y / CB DATA
Y / CR DATA

RGB, YCrCb Timing.

Timing Waveforms (continued)


CLOCK
A1 - A7, SAWR*
17
18
MPU*, ANC*
19
D0 - D7
20

A1–A7, D0–D7 Timing.


D0 - D7
21
22
OE*

Output Enable Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt291KPJ	100-pin Plastic J-Lead	0° to +70° C

Preliminary Information

This document contains information on a new product. The parametric information, lthough not fully characterized, is the result of testing initial devices.

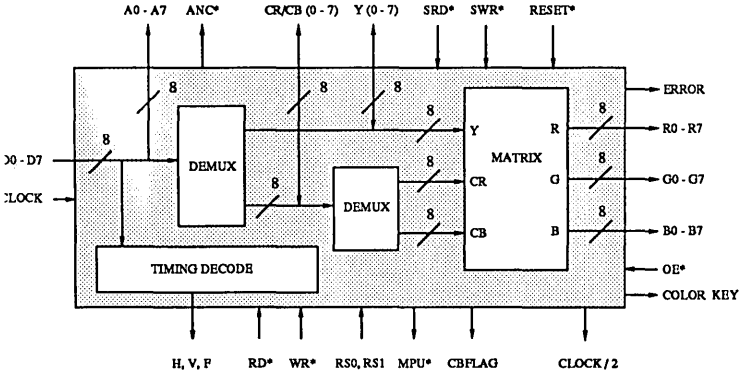
Bt294

27 MHz VideoNet™ YCrCb-to-RGB 8-bit Converter for 4:2:2 Video Applications

Distinguishing Features

- NTSC and CCIR Compatible
- YCrCb to RGB Conversion
- 16-bit Multiplexed YCrCb I/O Bus
- 8-Bit Ancillary Data Output Bus
- Selectable Cr/Cb Interpolation Filters
- Optional Data Rate Doubling to 27 MHz
- Three 256 x 8 RGB Output RAMs
- Video Timing Recovery
- Programmable Color Key Output
- TTL Compatible Inputs and Outputs
- +5 V Monolithic CMOS
- 100-pin PLCC Package
- Typical Power Dissipation: 900 mW

Functional Block Diagram



Applications

- CCIR601
- SMPTE RP125
- EBU 3246-E
- Image Processing and Capture
- YCrCb-to-RGB Conversion

Related Products

- Bt291, Bt297

Product Description

The Bt294 performs real-time YCrCb to RGB conversion. Eight bits of multiplexed YCrCb information are input and converted to RGB color information (8 bits each).

The incoming D0–D7 data has video timing information extracted, generating the horizontal blanking (H), vertical blanking (V), and field (F) outputs. Y and Cr/Cb data are demultiplexed, and available on the 16-bit Y and Cr/Cb I/O bus.

The Cr and Cb data are demultiplexed and interpolated data is generated using one of two interpolation filters, selectable by the MPU.

Ancillary data is detected and output onto the A0–A7 pins. ANC* is a logical zero while outputting Ancillary data.

Three 256 x 8 lookup table RAMs are provided, to support gamma correction, etc.

The output enable (OE*) control three-states the R0–R7, G0–G7, and B0–B7 outputs asynchronously to clock. YCrCb data (4:4:4 format) may also be output onto the RGB outputs.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L294001 Rev. E

Brooktree®

Detailed Block Diagram

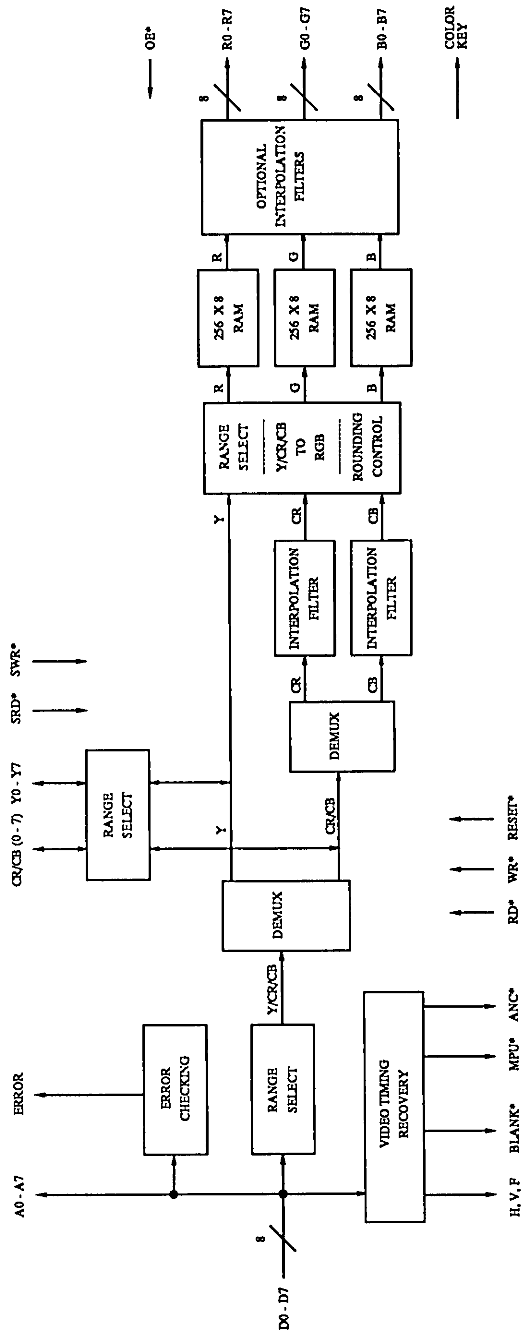

A0 - A7
ERROR
CR/CB (0 - 7)
Y0 - Y7
SRD*
SWR*
OE*
ERROR CHECKING
RANGE SELECT
D0 - D7
8
Y/CR/CB
DEMUX
Y
CR/CB
RANGE SELECT
DEMUX
CR
CB
INTERPOLATION FILTER
INTERPOLATION FILTER
RANGE SELECT
Y/CR/CB TO RGB
ROUNDING CONTROL
R
G
B
256 X 8 RAM
256 X 8 RAM
256 X 8 RAM
OPTIONAL INTERPOLATION FILTERS
R0 - R7
G0 - G7
B0 - B7
COLOR KEY
VIDEO TIMING RECOVERY
H, V, F
BLANK*
MPU*
ANC*
RD*
WR*
RESET*

Figure 1. Detailed Block Diagram.

Circuit Description

Video Timing Recovery

The D0–D7 inputs are monitored for start of active video (SAV) and end of active video (EAV) sequences. (See Figure 1.) The SAV and EAV sequences are as follows:

$FF $00 $00 $xx

where $xx is defined as follows:

D7 = logical one
D6 = F (F = 1 for field 2; = 0 for field 1)
D5 = V (V = 1 during vertical blanking)
D4 = H (H = 0 at SAV, H = 1 at EAV)
D3–D0 = protection bits

After the necessary error-checking and correcting are performed, the H, V, and F signals are output onto their respective pins following the rising edge of CLOCK. The Bt294 corrects single-bit errors in the fourth byte of the SAV and EAV sequences; double-bit errors, and some multiple-bit errors, are detected and flagged (via the ERROR output), but not corrected. If there is an uncorrected error, the ERROR output pin will be a logical one for five CLOCK cycles, three CLOCK cycles after the error has been input via the D0–D7 inputs. Refer to the Application Information section for more details regarding the protection bits and their operation.

To ease system timing requirements, the RGB, YCrCb, CbFLAG, and H, V, and F outputs have the same relative output timing.

Note: a minimum of 36 CLOCK cycles must occur between the end of a SAV sequence and the beginning of an EAV sequence and between the end of a EAV sequence and the beginning of an SAV sequence. (See Figures 3 and 4.)

D0–D7 Color Data Recovery

If the CR07 command bit is a logical one, then, if the Y, Cr, or Cb input value is zero, it is made 1; if the Y, Cr, or Cb input value is 255, it is made 254.

If the CR07 command bit is a logical zero, then, if the Y input value is 0–15, it is made 16; if the Y input value is 236–255, it is made 235. If the Cr or Cb input value is 0–15, it is made 16; if the Cr or Cb input value is 241–255, it is made 240.

Outputting Ancillary Data

The ANC* output is a logical zero during the horizontal and vertical digital blanking intervals, except during the EAV and SAV sequences. All D0–D7 data is output onto A0–A7 unmodified.

Ancillary sequences can occur multiple times per scan line if different blocks of data are received.

The Ancillary input sequence via D0–D7 is:

$00 $FF $FF TT MM LL xx xx...

TT is the Ancillary data identification code, MM and LL specify the Ancillary data word count. xx are information data words.

While receiving the TT Ancillary data identification code, the parity is recalculated and checked against the transmitted parity bit (odd parity). If there is an error in parity, the ERROR output pin will be a logical one for five CLOCK cycles, three CLOCK cycles after the TT data has been input via the D0–D7 inputs. The TT data is output onto the A0–A7 outputs, following the rising edge of CLOCK.

Byte TT

A7 = D7
A6 = D6
A5 = D5
A4 = D4
A3 = D3
A2 = D2
A1 = D1
A0 = D0 (odd parity bit)

While receiving the MM and LL Ancillary data word count, the parity is recalculated and checked against the transmitted parity bit (odd parity). If there is an error in parity, the ERROR output pin will be a logical one for five CLOCK cycles, three CLOCK cycles after the MM or LL data has been input via the D0–D7 inputs. The MM and LL data are output onto the A0–A7 outputs, following the rising edge of CLOCK.

Circuit Description (continued)

Byte MM	Byte LL
A7 = D7 (output as received)	A7 = D7 (output as received)
A6 = M5 (D6)	A6 = L5 (D6)
A5 = M4 (D5)	A5 = L4 (D5)
A4 = M3 (D4)	A4 = L3 (D4)
A3 = M2 (D3)	A3 = L2 (D3)
A2 = M1 (D2)	A2 = L1 (D2)
A1 = M0 (D1)	A1 = L0 (D1)
A0 = D0 (odd parity bit)	A0 = D0 (odd parity bit)

While receiving the Ancillary data (xx), the parity is recalculated and confirmed against the transmitted parity (odd parity). If there is an error in parity, the ERROR output pin will be a logical one for five CLOCK cycles, three CLOCK cycles after the Ancillary data has been input via the D0–D7 inputs. The Ancillary data is output onto the A0–A7 outputs, following the rising edge of CLOCK.

Byte(s) xx
A7 = D7
A6 = D6
A5 = D5
A4 = D4
A3 = D3
A2 = D2
A1 = D1
A0 = D0 (odd parity bit)

Note that the number of Ancillary data words specified by the data word count are parity-checked by the Bt294. After the specified number of data words, parity checking is disabled until the next Ancillary sequence.

Line count ANC sequences (such as implemented on the Bt291) do not follow the standard Ancillary data format. Thus, upon reception of line count ANC sequences, error conditions may occur. No error will occur if the line count ANC sequence occupies the last six words of the digital blanking interval (as implemented on the Bt291).

Note: a minimum of 36 CLOCK cycles must occur between the end of a EAV sequence and the beginning of an SAV sequence.

SAV sequences take precedence over Ancillary data. Therefore, if a SAV sequence is received before the number of Ancillary data words (as specified by the Ancillary data word count) has passed, the Ancillary data sequence is aborted and no ERROR is generated.

Ancillary Data Blocks (NTSC)

During horizontal blanking, small blocks of data, less than 268 words in total length (including the ANC preamble), can be received within a horizontal blanking interval, starting with the end of EAV and terminating with the SAV.

During vertical blanking, large blocks of data, up to 1440 words in total length (including the ANC preamble), may be received with the interval starting with the end of the SAV and terminating with the beginning of EAV.

Ancillary Data Blocks (CCIR)

During horizontal blanking, small blocks of data, less than 280 words in total length (including the ANC preamble), can be received within a horizontal blanking interval, starting with the end of EAV and terminating with the SAV.

During vertical blanking, large blocks of data, up to 1440 words in total length (including the ANC preamble), may be received with the interval starting with the end of the SAV and terminating with the beginning of EAV.

YCrCb Demultiplexer

The YCrCb demultiplexer separates the Y (8 bits) and multiplexed Cr/Cb (8 bits) information using the SAV sequence as a reference.

CbFLAG is also generated using the SAV sequence as a reference. It is output aligned with the YCrCb I/O bus.

YCrCb I/O Bus

A 16-bit bidirectional multiplexed YCrCb bus is provided for reading and writing active video data. The SRD* and SWR* inputs are used to synchronously read and write YCrCb data. SRD* and SWR* must be synchronous to CLOCK. (See Figure 2.)

Circuit Description (continued)

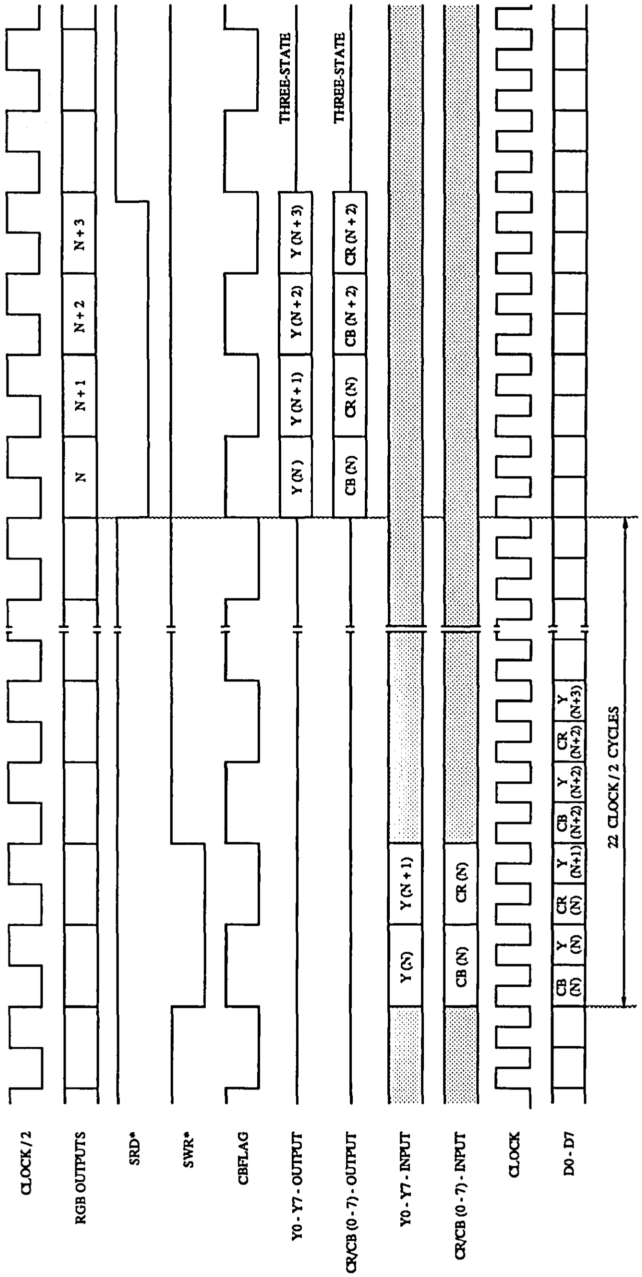

CLOCK / 2
RGB OUTPUTS
SRD*
SWR*
CBFLAG
Y0 - Y7 - OUTPUT
CR/CB (0 - 7) - OUTPUT
Y0 - Y7 - INPUT
CR/CB (0 - 7) - INPUT
CLOCK
D0 - D7
N
N + 1
N + 2
N + 3
THREE-STATE
Y (N)
Y (N + 1)
Y (N + 2)
Y (N + 3)
THREE-STATE
CB (N)
CR (N)
CB (N + 2)
CR (N + 2)
Y (N)
Y (N + 1)
CB (N)
CR (N)
CB (N)
Y (N)
CR (N)
Y (N+1)
CB (N+2)
Y (N+2)
CR (N+2)
Y (N+3)
22 CLOCK / 2 CYCLES

Figure 2. Reading/Writing Active Video Data (13.5 MHz RGB Output Rate).

Circuit Description (continued)

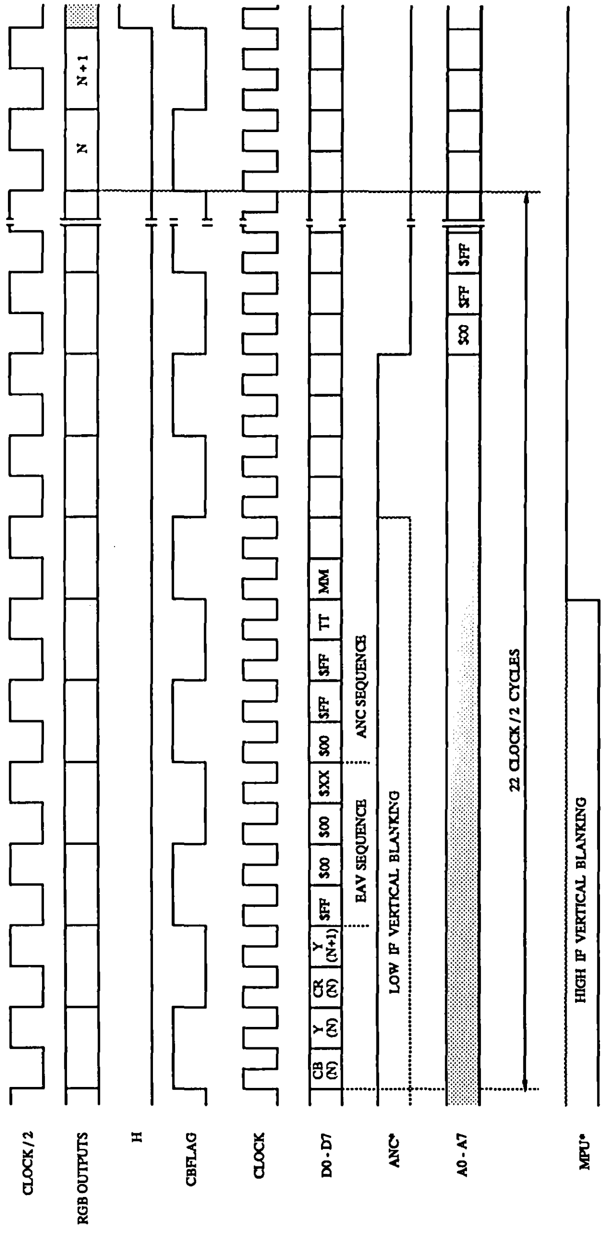

CLOCK/2
RGB OUTPUTS
H
CBFLAG
CLOCK
D0 - D7
ANC*
A0 - A7
MPU*
N
N+1
CB (N)
Y (N)
CR (N)
Y (N+1)
$FF
$00
$00
$XX
$00
$FF
$FF
TT
MM
EAV SEQUENCE
ANC SEQUENCE
LOW IF VERTICAL BLANKING
$00
$FF
$FF
22 CLOCK/2 CYCLES
HIGH IF VERTICAL BLANKING

Figure 3. EAV Sequence and Reading Ancillary Data (13.5 MHz RGB Output Rate).

Circuit Description (continued)

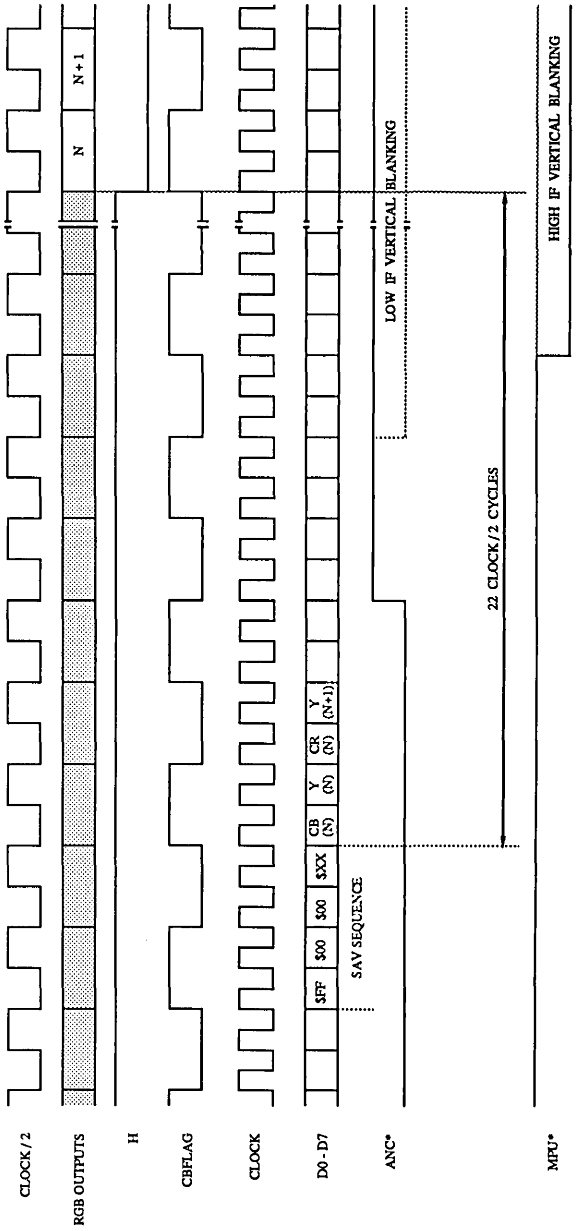

CLOCK/2
RGB OUTPUTS
N
N+1
H
CBFLAG
CLOCK
D0 - D7
$FF
$00
$00
$XX
CB (N)
Y (N)
CR (N)
Y (N+1)
SAV SEQUENCE
ANC*
LOW IF VERTICAL BLANKING
22 CLOCK/2 CYCLES
MPU*
HIGH IF VERTICAL BLANKING

Figure 4. SAV Sequence
(13.5 MHz RGB Output Rate).

Circuit Description (continued)

Reading YCrCb Data

While SRD* is a logical zero, YCrCb information from the RD0–D7 inputs is output onto Y (0–7) and CrCb (0–7) following the rising edge of CLOCK while CLOCK/2 is a logical one. Cb data is being output onto the CrCb bus while CbFLAG is a logical one.

The YCrCb output range is selected by the CR07 command bit:

(0) Y = 16 to 235; Cr and Cb = 16 to 240

or

(1) Y = 1 to 254; Cr and Cb = 1 to 254

If the CR07 command bit is a logical one, then if the Y, Cr, or Cb output value is zero, it is made 1; if the Y, Cr, or Cb output value is 255, it is made 254.

If the CR07 command bit is a logical zero, then if the Y output value is 0–15, it is made 16; if the Y output value is 236–255, it is made 235. If the Cr or Cb output value is 0–15, it is made 16; if the Cr or Cb output value is 241–255, it is made 240.

If CbFLAG is a logical one, Cb data is present on the CrCb bus; if CbFLAG is a logical zero, Cr data is present. CbFLAG is output following the rising edge of CLOCK while CLOCK/2 is a logical one.

While SRD* is a logical one, the YCrCb bus is three-stated. Note: SRD* must be synchronized to CLOCK externally for proper operation.

Writing YCrCb Data

While SWR* is a logical zero, YCrCb information is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. This YCrCb information is used to generate the RGB output data, rather than the D0–D7 inputs.

The YCrCb input range is selected by the CR07 command bit:

(0) Y = 16 to 235; Cr and Cb = 16 to 240

or

(1) Y = 1 to 254; Cr and Cb = 1 to 254

If the CR07 command bit is a logical one, if the Y, Cr, or Cb input value is zero, it is made 1; if the Y, Cr, or Cb input value is 255, it is made 254.

If the CR07 command bit is a logical zero, then if the Y input value is 0–15, it is made 16; if the Y input value is 236–255, it is made 235. If the Cr or Cb input value is 0–15, it is made 16; if the Cr or Cb input value is 241–255, it is made 240.

While CbFLAG is a logical one, Cb data is latched on the CrCb bus; if CbFLAG is a logical zero, Cr data is latched. CbFLAG is output following the rising edge of CLOCK while CLOCK/2 is a logical one.

CrCb Demultiplexer / Filters

The CrCb demultiplexer, using the CbFLAG signal, separates the 8 bits of multiplexed Cr and Cb data.

As Cr and Cb data are to be co-sited with the odd (first, third, fifth, etc.) Y samples, digital interpolation filters provide the even 8 bits of Cr and Cb data, converting the 4:2:2 YCrCb data to 4:4:4 YCrCb data.

YCrCb-to-RGB Matrix

The matrix converts the 24 bits of YCrCb data (8 bits each) to 24 bits of RGB data (8 bits each), and outputs the data onto R0–R7, G0–G7, and B0–B7.

The YCrCb to RGB conversion is selected by the command register and is either:

analog coefficient matrix:

$$R = Y + 1.402(Cr - 128)$$

$$G = Y - 0.714(Cr - 128) - 0.344(Cb - 128)$$

$$B = Y + 1.772(Cb - 128)$$

or digital coefficient matrix:

$$R = Y + 1.370(Cr - 128)$$

$$G = Y - 0.698(Cr - 128) - 0.336(Cb - 128)$$

$$B = Y + 1.730(Cb - 128)$$

Circuit Description (continued)

ROM lookup tables are used to perform the multiplications and 4 bits of fractional data are maintained. The final result is rounded to 8 bits as specified by command register_1. If the resulting R, G, or B value is less than zero, it is set to zero. If the resulting R, G, or B value is greater than 255, it is set to 255.

Note the digital coefficient matrix operates properly only when the YCrCb input range is Y = 16 to 235; Cr and Cb = 16 to 240 (the RGB output range will typically be 16 to 235). The analog coefficient matrix can handle the YCrCb input range of Y = 16 to 235; Cr and Cb = 16 to 240 (the RGB output range will typically be 16 to 235) or YCrCb = 1 to 254 (the RGB output range will typically be 1 to 254).

The YCrCb to RGB matrix may also be bypassed via the command register.

Output Lookup Table RAMs

Note that gamma-corrected RGB data is generated by the YCrCb to RGB matrix. The three output lookup table RAMs may be used to remove gamma correction on the R0–R7, G0–G7, and B0–B7 outputs in the event that they are to contain linear (rather than gamma-corrected) RGB data.

As the RGB data range from the YCrCb to RGB matrix is typically 16 to 235 (or 1 to 254), the lookup table RAMs may also be used to expand the range to 0 to 255.

The lookup table RAMs are not dual-ported, so MPU accesses have priority over pixel accessing. During MPU access to the color palette RAMs, the lookup table RAM outputs are undefined and invalid.

The lookup table RAMs are not initialized following a reset condition or power-up sequence.

RS1, RS0	CR03, CR02	ADDR0–ADDR7	Accessed by MPU
00	xx	$xx	address register
01	00	$00	red RAM location $00
01	00	$01	red RAM location $01
:	:	:	:
01	00	$FF	red RAM location $FF
01	01	$00	green RAM location $00
01	01	$01	green RAM location $01
:	:	:	:
01	01	$FF	green RAM location $FF
01	10	$00	blue RAM location $00
01	10	$01	blue RAM location $01
:	:	:	:
01	10	$FF	blue RAM location $FF
10	xx	$00	command register_0
10	xx	$01	command register_1
10	xx	$02	red color key register
10	xx	$03	green color key register
10	xx	$04	blue color key register
10	xx	$05	red color mask register
10	xx	$06	green color mask register
10	xx	$07	blue color mask register
10	xx	$08	reserved
:	:	:	:
10	xx	$FF	reserved
11	xx	$xx	reserved

Table 1. Internal Register Addressing.

Circuit Description (continued)

The RGB (or YCrCb) output rate may optionally be doubled to 27 MHz via the command register. In this mode of operation, the RGB outputs are updated every CLOCK cycle. The doubling of the data rate occurs after the lookup table RAMs.

Note that RGB data addressing the RAM is $00 during digital blanking intervals (including EAV and SAV sequences). When YCrCb data is selected as the output (CR06 is set to one), the lookup table is bypassed.

Output Enable Control

Command bit CR01 is logically gated with the OE* input, and the resulting value is used to control three-stating the R0–R7, G0–G7, and B0–B7 outputs asynchronously to the clocks as described in the Pin Descriptions section.

Color Key Output

The Bt294 generates a COLOR KEY output, determined by the color key and color mask registers. For a programmed color, or range of colors, the COLOR KEY output will be a logical one coincident with the specified color being output on the RGB outputs. COLOR KEY is output following the rising edge of CLOCK.

MPU Interface

The Bt294 supports a standard MPU interface (A0–A7, RD*, WR*, RS0, and RS1).

The MPU* output indicates when the MPU may access the Bt294 via the A0–A7 pins. A logical zero indicates MPU accesses may be done without contention with Ancillary data timing.

RS0 and RS1 are used to select address register (logical zero) or RAM location or control register specified by the address register (logical one), as shown in Table 1. The 8-bit address register specifies which control register or RAM location the MPU is accessing. The address register resets to $00 following a read or write cycle to location $FF. Write cycles to reserved addresses are ignored, and read cycles from reserved addresses return invalid data.

The address register increments after each MPU read or write cycle (except when reading or writing to the address register), and is not initialized. ADDR0 is the least significant bit and corresponds to bit A0.

As the MPU shares the Ancillary bus with Ancillary information, care must be taken that the MPU does not attempt to access the internal registers and lookup table RAMs during the digital blanking intervals. The MPU* output signal may be used to provide arbitration; while MPU* is a logical zero, the MPU may access the Bt294 without contention with any Ancillary data.

The rising edge of WR* latches A0–A7 into the selected register or lookup table RAM location. While RD* is a logical zero, the contents of the selected register or lookup table RAM location are output onto A0–A7.

Circuit Description (continued)

Typical Application

Figure 5 illustrates a typical application of the Bt294. The Bt294 converts the incoming D0–D7 data stream from the Bt297 ECL to TTL receiver, recovering video timing information, and reformatting the color data into 16 bits of multiplexed Y and Cr/Cb color data for loading into the frame buffer. Data from the frame buffer may also be clocked into the Bt294.

The Bt294 converts the YCrCb data into the RGB format for driving a true-color VIDEODAC and RAMDAC, such as a Bt101 or Bt473.

The RGB outputs may also be used to interface to an RGB frame buffer, rather than driving a VIDEODAC or RAMDAC, as shown in Figure 6.

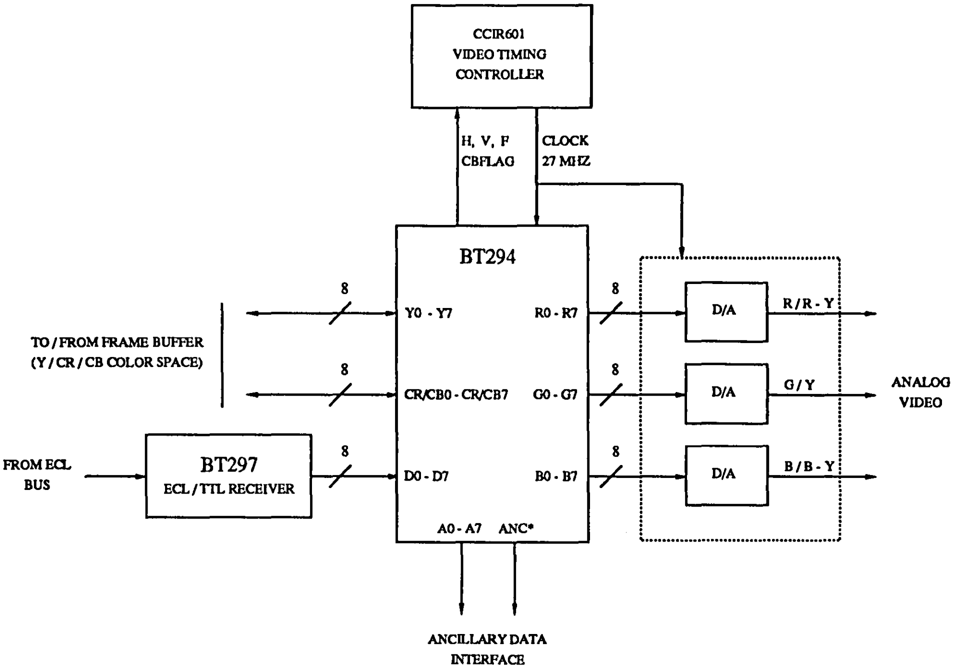

CCIR601
VIDEO TIMING
CONTROLLER
H, V, F
CBFLAG
CLOCK
27 MHZ
BT294
Y0 - Y7
CR/CB0 - CR/CB7
D0 - D7
R0 - R7
G0 - G7
B0 - B7
A0 - A7
ANC*
8
8
8
8
8
8
TO / FROM FRAME BUFFER
(Y / CR / CB COLOR SPACE)
FROM ECL
BUS
BT297
ECL / TTL RECEIVER
D/A
D/A
D/A
R / R - Y
G / Y
B / B - Y
ANALOG
VIDEO
ANCILLARY DATA
INTERFACE

Figure 5. Typical Application.

Circuit Description (continued)

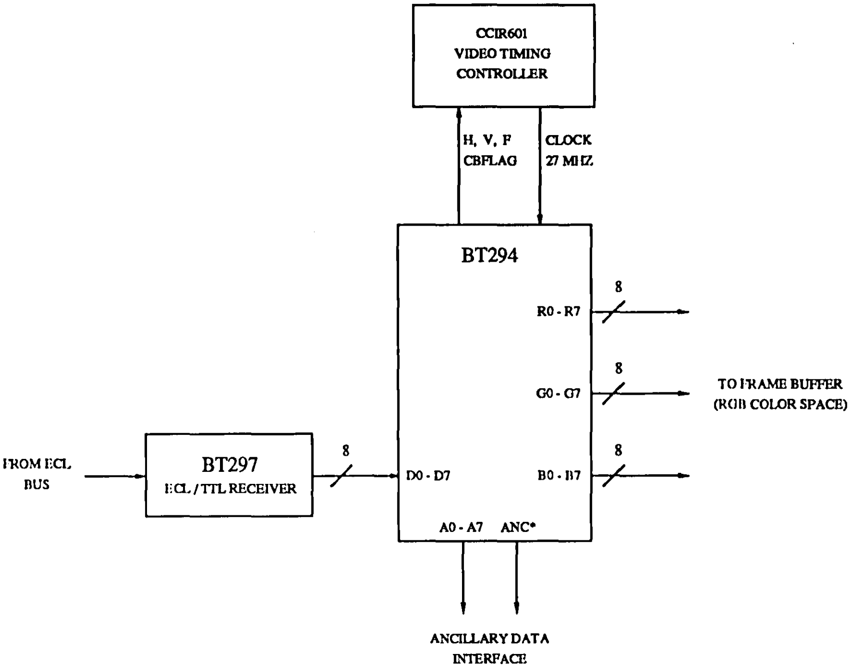

CCIR601
VIDEO TIMING
CONTROLLER
H, V, F
CBFLAG
CLOCK
27 MHZ
BT294
R0 - R7
G0 - G7
B0 - B7
8
8
8
TO FRAME BUFFER
(RGB COLOR SPACE)
FROM ECL
BUS
BT297
ECL / TTL RECEIVER
8
D0 - D7
A0 - A7
ANC*
ANCILLARY DATA
INTERFACE

Figure 6. Typical Application.

Internal Registers

Command Register_0

This command register may be written to or read by the MPU at any time and is initialized to $03 following a reset condition. CR00 is the least significant bit and corresponds to data bit A0.

CR07	YCrCb range (0) Y = 16 to 235, Cr/Cb = 16 to 240 (1) Y, Cr, Cb = 1 to 254	This bit specifies the range of Y, Cr, and Cb on the YCrCb I/O bus (when inputting or outputting color data), and the D0–D7 color data. Typically, mode (0) should be used. Regardless of the selection, there is no change in the pipeline delay.
CR06	RGB or YCrCb output select (0) RGB (1) YCrCb	This bit specifies whether the RGB outputs are outputting RGB or YCrCb color information. Y information is output onto the G0–G7 outputs, Cr information is output onto the R0–R7 outputs, and Cb information is output onto the B0–B7 outputs. Regardless of the selection, there is no change in the pipeline delay.
CR05	13.5 MHz or 27 MHz RGB outputs (0) 13.5 MHz (1) 27 MHz	This bit specifies whether or not to double the data rate of the RGB data.
CR04	Cr/Cb interpolation filters select (0) use 12-tap filters (1) use 2-tap filters	This bit specifies which interpolation filters to use for the Cr and Cb data. Typically, the 12-tap filters should be used. Regardless of the selection, there is no change in the pipeline delay.
CR03, CR02	Lookup table RAM select (00) red lookup table RAM (01) green lookup table RAM (10) blue lookup table RAM (11) reserved	These bits specify which lookup table RAM the MPU is accessing.
CR01	RGB output disable (0) enable RGB outputs (1) disable RGB outputs	This bit is logically gated with the OE* input pin, and the resulting value is used to control three-stating the RGB outputs.
CR00	Matrix coefficient select (0) analog matrix (1) digital matrix	This bit selects which set of coefficients to use in the YCrCb-to-RGB matrix, as described in the text. Typically, the digital matrix should be used. Regardless of the selection, there is no change in the pipeline delay.

Internal Registers (continued)

Command Register_1

This command register may be written to or read by the MPU at any time and is initialized to 11xx xxxx following a reset condition. CR10 is the least significant bit and corresponds to data bit A0.

CR17, CR16	Rounding select (00) normal rounding (01) even rounding (10) reserved (11) Dynamic Rounding™	This bit specifies the type of rounding used. Regardless of the selection, there is no change in the pipeline delay. (00) specifies round up if the fractional data is ≥ 0.5. If the fractional data is < 0.5, the number will be rounded down. (01) specifies round up if the fractional data = 0.5 and the rounded result will be an even number (LSB = 0) or if the fractional data is > 0.5. If the fractional data is < 0.5, the number will be rounded down. (11) specifies to use Dynamic Rounding™, where the fractional data is compared to a random number, and the result (1 bit) added to the 8 bits of color data. If the fractional data = 0, no rounding is done. R, G, and B each have their own random number generator. Typically, this mode should be used. Dynamic Rounding™ is used under license from Quantel Limited.
CR15–CR10	reserved (test bits)	These bits should be ignored when the MPU reads this register. Data written to these bits are ignored.

Color Key Registers

The three 8-bit color key registers may be written to or read by the MPU at any time and are initialized to $00 following a reset condition. Data bit A0 is the least significant bit and corresponds to the R0, G0, and B0 output bits.

The red color key register is compared against the R0–R7 outputs, the green color key register is compared against the G0–G7 outputs, and the blue color key register is compared against the B0–B7 outputs. If all unmasked bits match, the COLOR KEY output is a logical one.

Color Mask Registers

The three 8-bit color mask registers may be written to or read by the MPU at any time and are initialized to $00 following a reset condition. Data bit A0 is the least significant bit and corresponds to the R0, G0, and B0 output bits.

A logical zero specifies that the corresponding RGB output bit is to be compared against the corresponding bit in the color key registers. A logical one specifies that no comparison for the corresponding bit is to take place, and is not used in the generation of the COLOR KEY output signal.

Pin Descriptions

Pin Name	Description
D0–D7	Data inputs (TTL compatible). D0–D7 are latched on the rising edge of CLOCK. D0 is the least significant bit.
Cr/Cb0–Cr/Cb7	Cr/Cb data inputs/outputs (TTL compatible). Multiplexed Cr and Cb information is input or output via these pins depending on the value of SWR* and SRD*. CrCb0 is the least significant bit. If inputting Cr/Cb data, it is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. If outputting Cr/Cb data, it is updated following the rising edge of CLOCK while CLOCK/2 is a logical one.
Y0–Y7	Y data inputs/outputs (TTL compatible). Y information is input or output via these pins depending on the value of SWR* and SRD*. Y0 is the least significant bit. If inputting Y data, it is latched on the rising edge of CLOCK while CLOCK/2 is a logical one. If outputting Y data, it is updated following the rising edge of CLOCK while CLOCK/2 is a logical one.
CbFLAG	CbFLAG control output (TTL compatible). A logical one indicates Cb data may be input or output on the Cr/Cb (0–7) bus. It is output following the rising edge of CLOCK while CLOCK/2 is a logical one.
SWR*	Synchronous write control input (TTL compatible). A logical zero enables Y/Cr/Cb data to be input via the Y0–Y7 and Cr/Cb (0–7) pins. Both SRD* and SWR* should not be asserted simultaneously.
SRD*	Synchronous read control input (TTL compatible). A logical zero enables Y/Cr/Cb data to be output onto the Y0–Y7 and Cr/Cb (0–7) pins. Both SRD* and SWR* should not be asserted simultaneously.
A0–A7	Ancillary data outputs (TTL compatible). D0–D7 data is output onto A0–A7 following the rising edge of CLOCK. MPU data is also input and output via this bus. A0 is the least significant bit.
ANC*	Ancillary output (TTL compatible). A logical zero indicates Ancillary data may be present on the A0–A7 pins. ANC* is output following the rising edge of CLOCK.
R0–R7	Red outputs (TTL compatible). Red color information is output via these pins. Data is output following the rising edge of CLOCK. R0 is the least significant bit.
G0–G7	Green outputs (TTL compatible). Green color information is output via these pins. Data is output following the rising edge of CLOCK. G0 is the least significant bit.
B0–B7	Blue outputs (TTL compatible). Blue color information is output via these pins. Data is output following the rising edge of CLOCK. B0 is the least significant bit.
H, V, F	Video timing control outputs (TTL compatible). They are output following the rising edge of CLOCK.
RESET*	Reset control input (TTL compatible). RESET* is sampled on the rising edge of CLOCK, and must be a logical zero for a minimum of three consecutive CLOCK cycles to reset the device. RESET* must be a logical one for normal operation.
ERROR	Error indicator output (TTL compatible). This output indicates a parity error in the EAV, SAV, Ancillary data identification code, Ancillary data word count, or Ancillary data. If an error is detected, ERROR will be a logical one for five CLOCK cycles, three CLOCK cycles after the error has occurred.

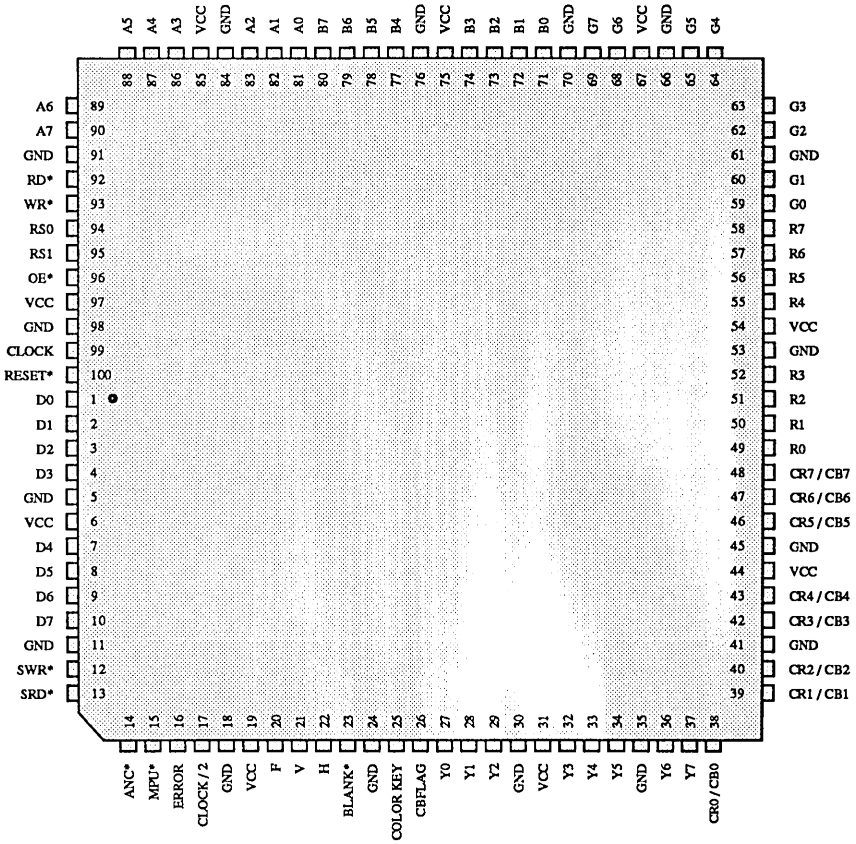
Pin Descriptions (continued)

Pin Name	Description
OE*	Output enable control input (TTL compatible). This input is logically gated with command bit CR01, and the result controls three-stating the RGB outputs as follows:

CR01	OE*	RGB Outputs
0	0	enabled
0	1	three-stated
1	0	three-stated
1	1	three-stated

Pin Name	Description
CLOCK	27 MHz clock input (TTL compatible). The clock must be present for the MPU to access the internal control registers.
CLOCK/2	13.5 MHz clock output (TTL compatible). The clock output is 1/2 the CLOCK rate.
RD*	MPU read control input (TTL compatible). While a logical zero, the contents of the control register/RAM location are output onto A0–A7. If both RD* and WR* are asserted simultaneously, all signal pins are three-stated (note the device should be reset after three-stating the signal pins).
WR*	MPU write control input (TTL compatible). The rising edge of WR* latches A0–A7 into the control register/RAM location. WR* is internally resynchronized to CLOCK, so CLOCK must be a continuous clock. If both RD* and WR* are asserted simultaneously, all signal pins are three-stated (note the device should be reset after three-stating the signal pins).
RS0, RS1	Register select control inputs (TTL compatible). These bits specify whether the MPU is accessing the address register or the control register/RAM location specified by the address register. See Table 3.
MPU*	MPU access control output (TTL compatible). A logical zero indicates the MPU may access the internal registers without contention with Ancillary data. MPU* is output following the rising edge of CLOCK.
BLANK*	Composite blanking output (TTL compatible). BLANK* is the logical NOR of the H and V outputs, and has the same timing.
COLOR KEY	Color key output (TTL compatible). This output is a logical one for clock cycles where the RGB outputs contain color information specified by the color key and color mask registers. It is output following the rising edge of CLOCK.
VCC	Power pins. All VCC pins must be connected together.
GND	Ground pins. All GND pins must be connected together.

Pin Descriptions (continued)


88 A5
87 A4
86 A3
85 VCC
84 GND
83 A2
82 A1
81 A0
80 B7
79 B6
78 B5
77 B4
76 GND
75 VCC
74 B3
73 B2
72 B1
71 B0
70 GND
69 G7
68 G6
67 VCC
66 GND
65 G5
64 G4
63 G3
62 G2
61 GND
60 G1
59 G0
58 R7
57 R6
56 R5
55 R4
54 VCC
53 GND
52 R3
51 R2
50 R1
49 R0
48 CR7/CB7
47 CR6/CB6
46 CR5/CB5
45 GND
44 VCC
43 CR4/CB4
42 CR3/CB3
41 GND
40 CR2/CB2
39 CR1/CB1
89 A6
90 A7
91 GND
92 RD*
93 WR*
94 RS0
95 RS1
96 OE*
97 VCC
98 GND
99 CLOCK
100 RESET*
1 D0
2 D1
3 D2
4 D3
5 GND
6 VCC
7 D4
8 D5
9 D6
10 D7
11 GND
12 SWR*
13 SRD*
14 ANC*
15 MPU*
16 ERROR
17 CLOCK/2
18 GND
19 VCC
20 F
21 V
22 H
23 BLANK*
24 GND
25 COLOR KEY
26 CBFLAG
27 Y0
28 Y1
29 Y2
30 GND
31 VCC
32 Y3
33 Y4
34 Y5
35 GND
36 Y6
37 Y7
38 CR0/CB0

Application Information

Cr and Cb Interpolation Filters

The Cr/Cb linear phase interpolation filters interpolate the missing Cr and Cb data to generate 4:4:4 YCrCb data. Input color data samples are passed unchanged to the output; computed color data (from the filters) are inserted into the output flow.

If the CR07 command bit is a logical one, then if the interpolated result is zero, it is made 1; if the interpolated result is 255, it is made 254. If the CR07 command bit is a logical zero, then if the interpolated result is 0–15, it is made 16; if the interpolated result is 241–255, it is made 240.

The transfer function of the 12-tap filters is:

$$\begin{aligned} H(Z) = {} & (160/256)*(Z^{-1} + Z^{+1}) \\ & + (-48/256)*(Z^{-3} + Z^{+3}) \\ & + (24/256)*(Z^{-5} + Z^{+5}) \\ & + (-12/256)*(Z^{-7} + Z^{+7}) \\ & + (6/256)*(Z^{-9} + Z^{+9}) \\ & + (-2/256)*(Z^{-11} + Z^{+11}) \end{aligned}$$

Seventeen-bit precision (including sign and overflow) is maintained until the final output stage, then rounded to 8 bits as specified by command register_1. Figure 7 shows the transfer function of the 12-tap Cr and Cb interpolation filters.

The transfer function of the 2-tap filters is:

$$H(Z) = (128/256)*(Z^{-1} + Z^{+1})$$

Eleven-bit precision (including sign and overflow) is maintained until the final output stage, then rounded to 8 bits as specified by command register_1.

The Y data and control signals are pipelined to maintain synchronization with the Cr and Cb data. There is no change in the pipeline delay regardless of which filter is used.

During blanking periods, the input color data is undefined, possibly disturbing the computed color data at the beginning and end of active color data. To avoid this, if the 12-tap is filter-selected, the 2-tap filter is automatically used at the beginning and end of the active line unless the 12-tap filter is available (i.e., the filter pipe is full). Regardless of the filter selection, the last active pixel per scan line uses the previous Cr and Cb data for color information.

Doubling the RGB Data Rate

The data rate of RGB output data may be doubled from 13.5 MHz to 27 MHz via the command register. In this instance, new RGB data is output following the rising edge of every CLOCK cycle, rather than every other CLOCK cycle.

To accomplish this, an additional set of 2-tap linear interpolation filters are used to double the RGB data rate from 13.5 MHz to 27 MHz. Input color data samples are passed unchanged to the output; computed color data (from the filters) are inserted into the output flow.

The transfer function of the 2-tap filters is:

$$H(Z) = (128/256)*(Z^{-1} + Z^{+1})$$

Eleven-bit precision (including sign and overflow) is maintained until the final output stage, then rounded to 8 bits using Dynamic Rounding™ (used under license from Quantel Limited).

Outputting RGB data at the 27 MHz rate may simplify the analog filtering if the RGB outputs are driving external D/A converters. Note that any sin x / x correction must be done with the analog filters after the D/A converters.

SAV and EAV Error Correction

Table 2 gives corrected values for F, V, and H where possible. Multiple (uncorrectable) errors are denoted by an asterisk. D1–D3 are Hamming (6:3) protection bits, and D0 is an even parity bit for D1–D6.

In the event of an uncorrectable error, the H, V, and F outputs assume the state specified by the EAV or SAV sequence (as if an error did not occur).

Application Information (continued)

Random Number Generators

The Bt294 contains two random number generators, as shown in Figures 8 and 9, used when Dynamic Rounding™ (used under license from Quantel Limited) is selected.

Figure 8 shows the random number generator used for the YCrCb to RGB matrix and the RGB data rate doubling (it is initialized to $000 following a reset condition). As each RGB value in the matrix has 4 fractional data bits, 4 bits of random numbering is generated for each RGB value. The LSB of each 4-bit random number (D0, D4, D8) corresponds to the LSB of fractional RGB data.

The RGB rate doubling filters have 1 bit of fractional data. Random number bit D12 corresponds to red fractional data, bit D13 corresponds to green, and bit D14 corresponds to blue.

Figure 9 shows the random number generator for the Cr and Cb filters (it is initialized to $00 following a reset condition). As a single CrCb filter is used in a multiplexed fashion, a single CrCb random number generator is used. The 12-tap filter has 7 bits of fractional data. The LSB of the 7-bit random number (D0) corresponds to the LSB of fractional Cr and Cb data. The LSB of this random number generator (D0) is used for the 2-tap filters, which have 1 bit of fractional data.

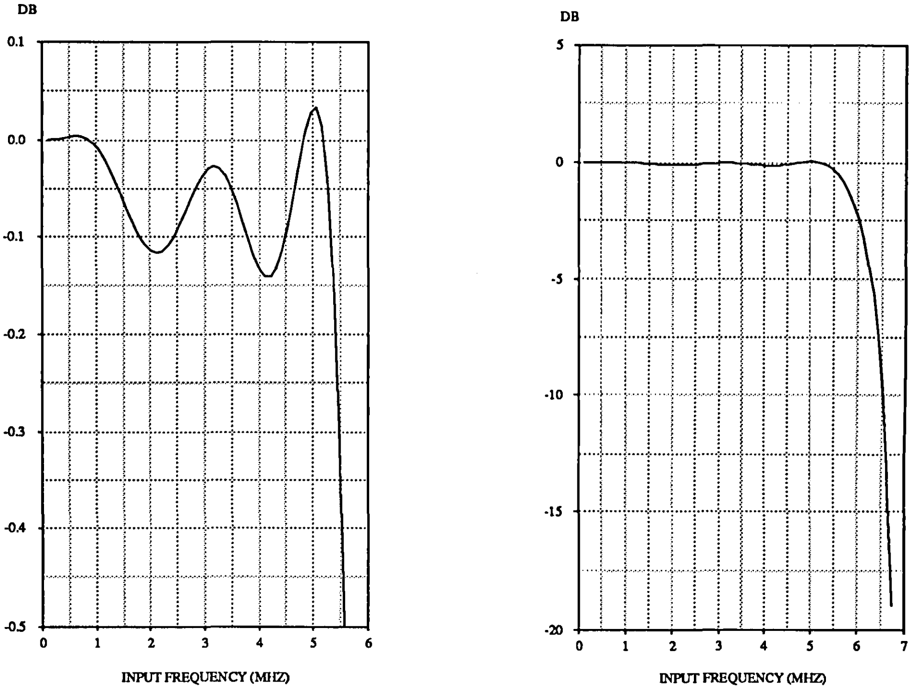


Figure 7. CrCb Pass-Band and Stop-Band Interpolation Filter Characteristics.

Application Information (continued)

Typical Applications

Figure 10 shows the Bt291 and Bt294 being used with a 24-bit RGB frame buffer. The Bt291 and Bt294 provide another video I/O port to the imaging/graphics system.

Figure 11 shows the Bt291 and Bt294 being used with a 16-bit YCrCb frame buffer. The Bt291 and Bt294 provide another video I/O port to the imaging/graphics system.

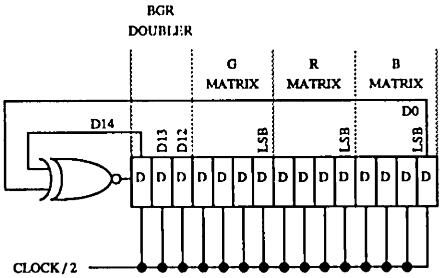

BGR DOUBLER
G MATRIX
R MATRIX
B MATRIX
D0
D14
D13
D12
LSB
LSB
LSB
D D D D D D D D D D D D D D D
CLOCK/2

Figure 8. Random Number Generator.

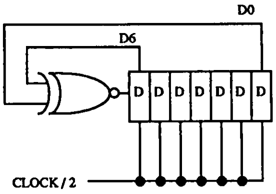

D0
D6
D D D D D D D
CLOCK/2

Figure 9. Random Number Generator for Cr and Cb Filters.

Application Information (continued)

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance.

Latchup can be prevented by assuring that all VCC pins are at the same potential, and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

PLCC Sockets

100-pin PLCC sockets for the Bt294 are available from:

McKenzie Technology
44370 Old Warm Springs Blvd.
Fremont, CA 94538
Phone: (415) 651-2700
FAX: (415) 651-1020
TLX: 910-240-6355
Part Number: PLCC-100-P-T

or

Yamaichi Electric Mfg. Co., LTD.
3-28-7 Nakamagome, Ohta-ku,
Tokyo 143 Japan
Phone: 03-778-6161
FAX: 03-778-6181
US Representative: (408) 452-0797

	Received F, V, H (Bits D6–D4)							
D3 - D0	000	001	010	011	100	101	110	111
0000	000	000	000	*	000	*	*	111
0001	000	*	*	111	*	111	111	111
0010	000	*	*	011	*	101	*	*
0011	*	*	010	*	100	*	*	111
0100	000	*	*	011	*	*	110	*
0101	*	001	*	*	100	*	*	111
0110	*	011	011	011	100	*	*	011
0111	100	*	*	011	100	100	100	*
1000	000	*	*	*	*	101	110	*
1001	*	001	010	*	*	*	*	111
1010	*	101	010	*	101	101	*	101
1011	010	*	010	010	*	101	010	*
1100	*	001	110	*	110	*	110	110
1101	001	001	*	001	*	001	110	*
1110	*	*	*	011	*	101	110	*
1111	*	001	010	*	100	*	*	*

Table 2. SAV and EAV Error Correction Table.

Application Information (continued)

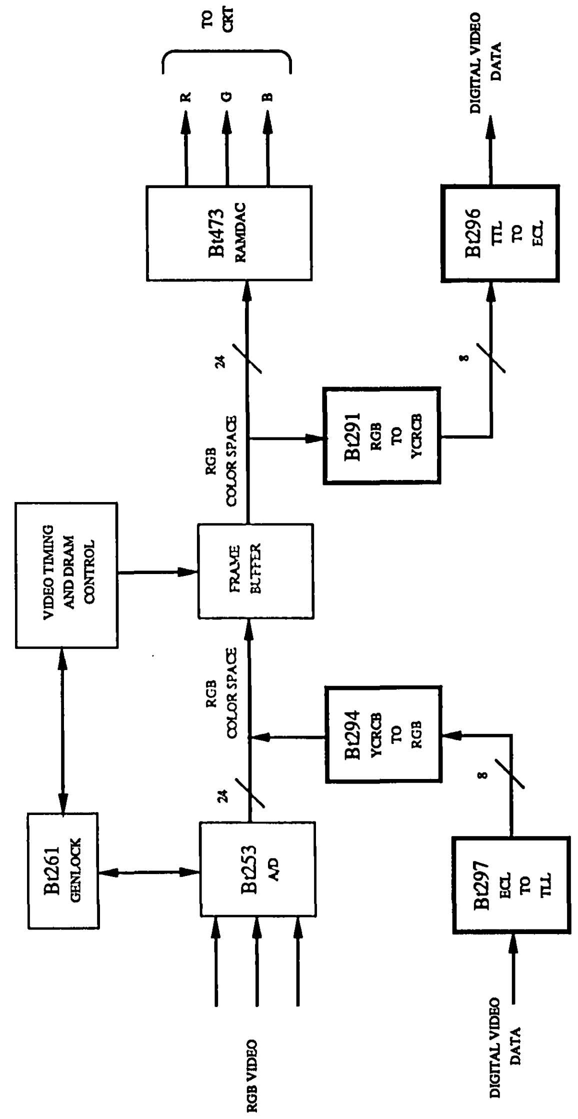

Bt261
GENLOCK
VIDEO TIMING
AND DRAM
CONTROL
RGB VIDEO
Bt253
A/D
24
RGB
COLOR SPACE
FRAME
BUFFER
RGB
COLOR SPACE
24
Bt473
RAMDAC
R
G
B
TO
CRT
Bt294
YCRCB
TO
RGB
Bt291
RGB
TO
YCRCB
DIGITAL VIDEO
DATA
Bt297
ECL
TO
TLL
8
8
Bt296
TTL
TO
ECL
DIGITAL VIDEO
DATA

Figure 10. Typical Application.

Application Information (continued)

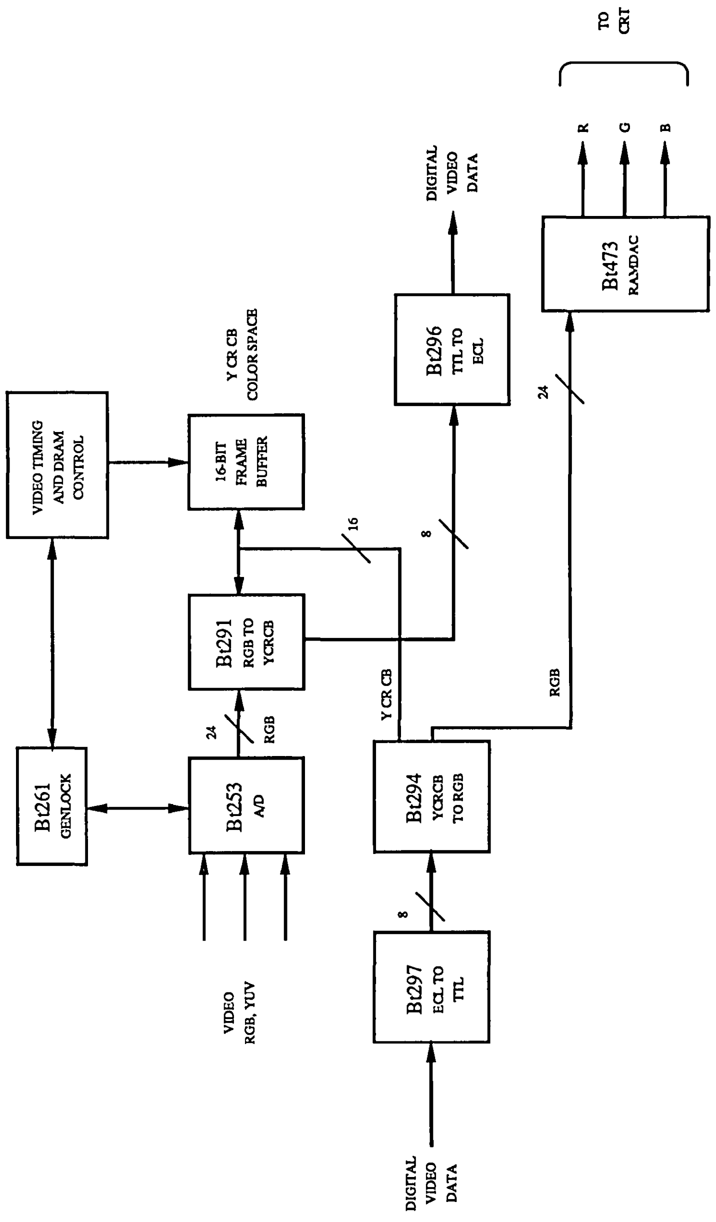

Bt261
GENLOCK
VIDEO TIMING
AND DRAM
CONTROL
VIDEO
RGB, YUV
Bt253
A/D
24
RGB
Bt291
RGB TO
YCRCB
16-BIT
FRAME
BUFFER
Y CR CB
COLOR SPACE
16
DIGITAL
VIDEO
DATA
Bt297
ECL TO
TTL
8
Bt294
YCRCB
TO RGB
Y CR CB
8
Bt296
TTL TO
ECL
DIGITAL
VIDEO
DATA
RGB
24
Bt473
RAMDAC
R
G
B
TO
CRT

Figure 11. Typical Application.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.5	5.00	5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	Volts
Voltage on any Signal Pin*		GND–0.5		VCC + 0.5	Volts
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	Volts
3-state Current (if applicable)	IOZ			50	µA
Output Capacitance	COUT		20		pF

Test conditions (unless otherwise specified): "Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

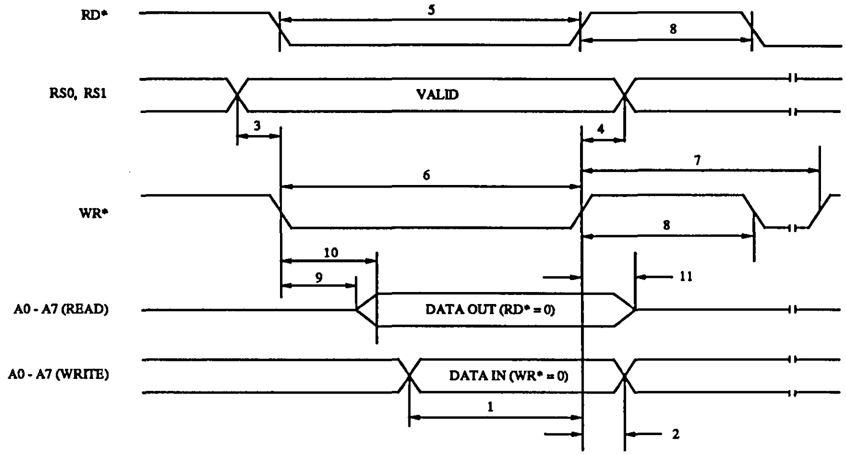
AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			27	MHz
MPU Data Setup Time	1	10			ns
MPU Data Hold Time	2	10			ns
RS0, RS1 Setup Time	3	10			ns
RS0, RS1 Hold Time	4	10			ns
RD* Low Time	5	1			Clock
WR* Low Time	6	100			ns
WR* Cycle Time	7	3			Clocks
RD*, WR* High Time	8	30			ns
RD* Asserted to Data Bus Driven	9	5			ns
RD* Asserted to Data Valid	10			100	ns
RD* Negated to Data Bus 3-Stated	11			25	ns
CLOCK/2 Low Time	12	15		tbd	ns
CLOCK/2 High Time	13	15		tbd	ns
CLOCK/2, H, V, F, Y/Cr/Cb (0–7), RGB (0–7), CbFLAG, BLANK* Output Delay	14	5		23	ns
Y/Cr/Cb Input Data, SRD*, SWR*					
Setup Time	15	10			ns
Hold Time	16	4			ns
D0–D7 Input Data					
Setup Time	17	10			ns
Hold Time	18	4			ns
MPU*, ANC*, ERROR, COLOR KEY Output Delay	19	5		23	ns
A0–A7 Output Delay	20	5		23	ns
SRD* Asserted to YCrCb Bus Driven				25	ns
SRD* Negated to YCrCb Bus 3-Stated				25	ns
RGB Three-State Disable Time	21			25	ns
RGB Three-State Enable Time	22			25	ns
Clock Cycle Time	23	37.04			ns
Clock Pulse Width High	24	15			ns
Clock Pulse Width Low	25	15			ns
VCC Supply Current*	ICC		180	tbd	mA

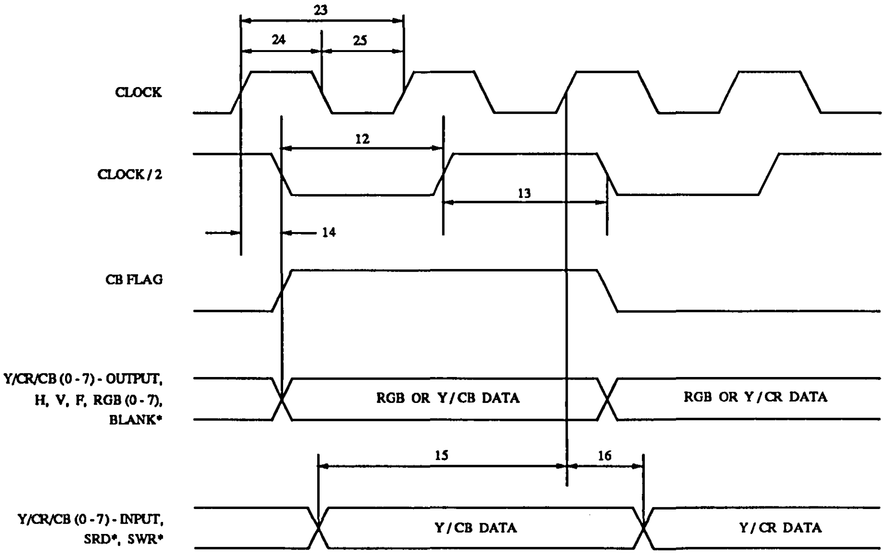
Test conditions (unless otherwise specified): "Recommended Operating Conditions." TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. CbFLAG, CLOCK/2, ANC*, Yx, Crx/Cbx, A0–A7, R0–R7, G0–G7, B0–B7, MPU*, COLOR KEY, and ERROR output load ≤ 75 pF. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*At Fmax. ICC (typ) at VCC = 5.0 V. ICC (max) at VCC (max).

Timing Waveforms

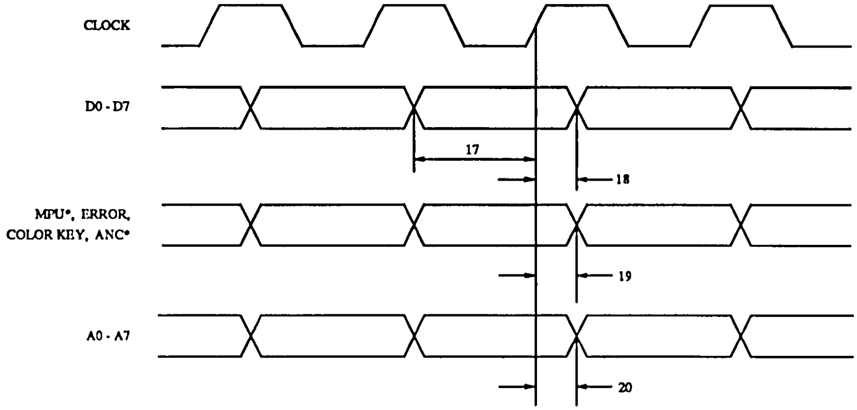

RD*
RS0, RS1
VALID
WR*
A0 - A7 (READ)
DATA OUT (RD* = 0)
A0 - A7 (WRITE)
DATA IN (WR* = 0)
1
2
3
4
5
6
7
8
9
10
11

MPU Read/Write Timing.

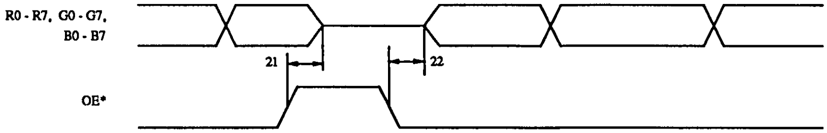

CLOCK
CLOCK / 2
CB FLAG
Y/CR/CB (0 - 7) - OUTPUT, H, V, F, RGB (0 - 7), BLANK*
RGB OR Y/CB DATA
RGB OR Y/CR DATA
Y/CR/CB (0 - 7) - INPUT, SRD*, SWR*
Y/CB DATA
Y/CR DATA
12
13
14
15
16
23
24
25

RGB, YCrCb Timing.

Timing Waveforms (continued)


CLOCK
D0 - D7
17
18
MPU*, ERROR,
COLOR KEY, ANC*
19
A0 - A7
20

A0–A7, D0–D7 Timing.


R0 - R7, G0 - G7,
B0 - B7
21
22
OE*

Output Enable Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt294KPJ	100-pin Plastic J-Lead	0° to +70° C

Advance Information

This document contains information on a product under development. The parametric nformation contains target parameters and is subject to change.

Bt296

27 MHz VideoNet™ TTL-to-10KH ECL 11-Bit Translator

Distinguishing Features

- Latched TTL-Compatible Inputs
- 10KH ECL-Compatible Parallel Outputs
- PLL Operation for Stable Timing
- Separate TTL and ECL Supply Pins
- TTL-Compatible Control Inputs
- 68-pin PLCC Package

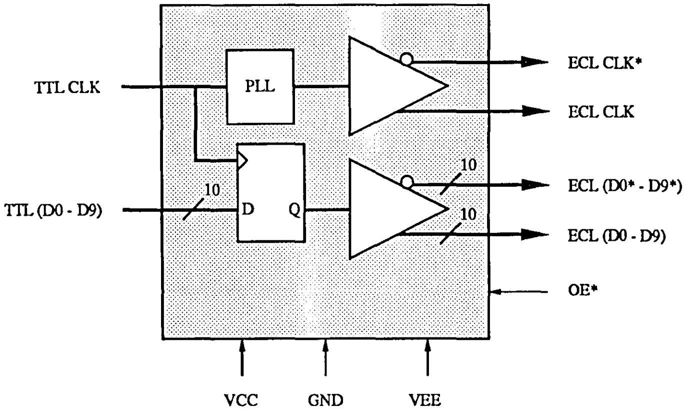
Applications

- CCIR601
- SMPTE RP125
- EBU 3246-E

Related Devices

- Bt297

Functional Block Diagram



Product Description

The Bt296 TTL/ECL Translator converts 11 bits of TTL data to 11 bits of differential 10KH ECL data.

In many cases involving the transmission of digital video signals, differential ECL signals levels are used. In addition, the phase relationship between the clock and data signals (and between data signals) is tightly defined. Thus, the TTL video data must be converted to ECL levels, and the phase relationship between clock and data adjusted to compensate for part-to-part output delay variations of TTL devices.

The Bt296 incorporates all translators in one package to eliminate delay skew that results when using multiple devices. A 10-bit data path is supported for high-end systems and compatibility with future products.

The clock-to-data timing on the ECL outputs is controlled by the on-chip PLL, enabling CCIR601, EBU 3246-E, and SMPTE RP-125 timing requirements to be met without adjustment. In addition, the ECL CLK outputs have a 50% duty cycle regardless of the TTL CLK duty cycle.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L296001 Rev. B

Brooktree®

Pin Descriptions

Pin Name	Description
TTL (D0–D9)	TTL data inputs (TTL compatible). They are latched on the rising edge of TTL CLK, converted to differential ECL levels, and output onto the ECL (D0–D9) and (D0*–D9*) pins. Unused pins should be connected to GND. In 8-bit systems, TTL D0 and TTL D1 should be connected to ground, using the TTL D2 (LSB)–TTL D9 inputs for the 8 bits of data.
TTL CLK	TTL clock input (TTL compatible). The rising edge of TTL CLK latches the TTL D0–D9 data.
ECL (D0–D9), ECL (D0*–D9*)	Differential ECL data outputs (ECL compatible). These are open emitter-follower outputs.
ECL CLK, ECL CLK*	Differential ECL clock outputs (ECL compatible). These are open emitter-follower outputs.
OE*	Output enable control (TTL compatible). A logical one forces the ECL outputs low and the ECL* outputs high (both data and clock) asynchronously to the clocks.
REXT	VCO free-running control. A resistor between this pin and GND sets the free-running frequency of the VCO. For 27 MHz, a value of 4220 ohms is recommended.
LF	Loop filter pin. The loop filter for the PLL is connected between this pin and GND. See Figure 1 (resistor values are in ohms, capacitor values are in µF).
VCC	TTL power supply. All VCC pins must be connected together as close to the device as possible.
GND	Ground. All GND pins must be connected together as close to the device as possible.
VEE	ECL power supply. All VEE pins must be connected together as close to the device as possible.

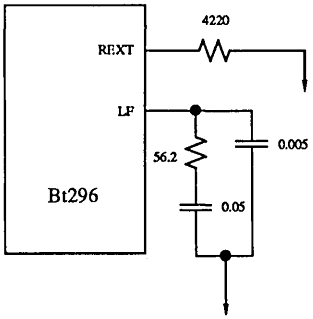


Figure 1. PLL Loop Filter (27 MHz Clock, 100 KHz Loop Bandwidth).

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	GND	0	0	0	Volts
TTL Power Supply	VCC	+4.75	+5.0	+5.25	Volts
ECL Power Supply	VEE	–4.9	–5.2	–5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device, either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (measured to GND)				–8.0	Volts
VCC (measured to GND)				+7.0	Volts
Voltage on Any ECL Pin		–1.8		GND	Volts
Voltage on Any TTL Pin		GND–0.5		VCC + 0.5	Volts
ECL Output Current				–50	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ECL DC Characteristics

Parameter	Symbol	TA (°C)	Min	Typ	Max	Units
Output High Voltage*	VOH	0 +25 +70	–1020 –980 –920		–840 –810 –735	mV mV mV
Output Low Voltage*	VOL	0 +25 +70	–1950 –1950 –1950		–1630 –1630 –1600	mV mV mV
Output Impedance Output Capacitance				7 tbd		Ohms pF
VEE Supply Current**	IEE	0 +25 +70		55 55 55	70 70 70	mA mA mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL output loading of 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Relative to GND.
**For power calculations, it is necessary to add an additional 330 mW due to emitter-follower devices.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device, either mounted in the test socket or on the printed circuit board.

TTL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage*	VIH	2.0		TTL VCC +0.5	Volts
Input Low Voltage*	VIL	TTL GND -0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			70	µA
Input Low Current (Vin = 0.4 V)	IIL			-0.7	mA
Input Capacitance			tbd		pF
VCC Supply Current	ICC		80	110	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Relative to GND.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL D0–D9 Setup Time	1	3			ns
TTL D0–D9 Hold Time	2	3			ns
TTL CLK High Time	3	10			ns
TTL CLK Low Time	4	10			ns
TTL CLK Input Rate	Fin	tbd		27	MHz
ECL D0–D9 Output Delay	5	tbd		10	ns
ECL D0–D9 Delay Skew*				3	ns
ECL CLK Output Delay**	6	(0.5 / Fin)–3	0.5 / Fin	(0.5 / Fin)+3	ns
ECL CLK Output Duty Cycle		42	50	58	%
PLL Acquire Time***					
100 KHz Loop Bandwidth				10,000	Clocks
1 MHz Loop Bandwidth				200	Clocks
Output Rise/Fall Time (20%–80%)		0.5	1	2	ns
Output Disable Time	7			15	ns
Output Enable Time	8			15	ns

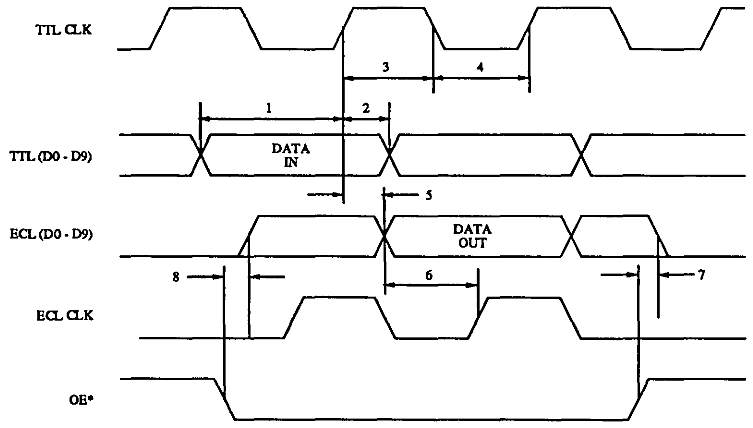
Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL output loading of 50 Ω to –2 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Fastest/slowest (unipolar).

**Rising edge of ECL CLK relative to ECL (D0 - D9).

***At 27 MHz. Initial frequency offset of ± 30%, final residual frequency error of ±1 %.

Timing Waveforms



Input/Output Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt296KPJ	68-pin Plastic J-lead	0° to +70° C

Advance Information

This document contains information on a product under development. The parametric information contains target parametersis are subjcct to change.

Bt297

27 MHz VideoNet™
10KH ECL to TTL
11-Bit Translator

Distinguishing Features

10KH ECL Compatible Inputs
Registered or Transparent Operation
TTL-Compatible Outputs
Separate TTL and ECL Supply Pins
TTL-Compatible Control Inputs
68-pin PLCC Package
Typical Power Dissipation: 550 mW

Applications

- CCIR601
- SMPTE RP125
- EBU 3246-E

Related Devices

- Bt296

Product Description

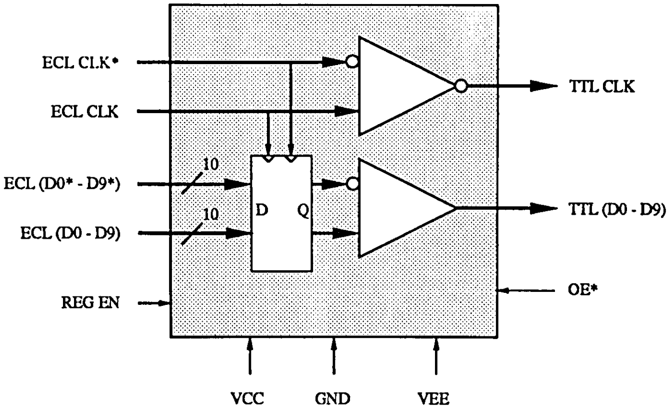
The Bt297 ECL/TTL Translator converts 11 bits of differential 10KH ECL data to 11 bits of TTL data.

The Bt297 incorporates all translators in one package to eliminate delay skew that results when using multiple devices.

The REG EN input controls whether the input data is registered or the data register is bypassed (transparent operation).

The TTL clock and data outputs may be three-stated asynchronously to the clock by the OE* pin.

Functional Block Diagram



Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249

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Pin Descriptions

Pin Name	Description
TTL (D0–D9)	TTL data outputs (TTL compatible).
TTL CLK	TTL clock output (TTL compatible).
ECL (D0–D9) ECL (D0*–D9*)	Differential ECL data inputs (ECL compatible). ECL data is latched by the ECL CLK signals, converted to TTL levels, and output onto the TTL data pins. Single-ended ECL operation may be used by connecting the ECL (D0*–D9*) pins to VBB (–2 V). If a pair of ECL inputs are left floating or are in the same logical state, the corresponding TTL output will be a logical zero.
ECL CLK, ECL CLK*	Differential ECL clock inputs (ECL compatible). Single-ended ECL operation may be used by connecting the ECL CLK pin to VBB (–2 V). If REG EN is a logical one, the ECL CLK is inverted and output onto the TTL CLK output pin. If REG EN is a logical zero, the ECL CLK is not inverted before being output onto the TTL CLK output pin.
REG EN	Register enable control input (TTL compatible). A logical one enables the D0–D9 input data to be registered by the data input register. A logical zero bypasses the data input register, enabling transparent operation.
OE*	Output enable control (TTL compatible). A logical one three-states the TTL (D0–D9) and TTL CLK outputs asynchronously to the clock.
VCC	TTL power supply. All VCC pins must be connected together as close to the device as possible.
GND	Ground. All GND pins must be connected together as close to the device as possible.
VEE	ECL power supply. All VEE pins must be connected together as close to the device as possible.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	GND	0	0	0	Volts
TTL Power Supply	VCC	+4.75	+5.0	+5.25	Volts
ECL Power Supply	VEE	–4.9	–5.2	–5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (measured to GND)				–8.0	Volts
VCC (measured to GND)				+7.0	Volts
Voltage on Any ECL Pin		-1.8 V		GND	Volts
Voltage on Any TTL Pin		GND–0.5		VCC + 0.5	Volts
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ECL DC Characteristics

Parameter	Symbol	TA (°C.)	Min	Typ	Max	Units
Input High Voltage*	VIH	0 +25 +70	−1170 −1130 −1070		−840 −810 −735	mV mV mV
Input Low Voltage*	VIL	0 + 25 + 70	−1950 −1950 −1950		−1480 −1480 −1450	mV mV mV
Input Current (Vin = VIHmax or VIL min)	IIN	0 +25 +70			10 10 10	µA µA µA
Common Mode Voltage Range					−310	mV
Differential Input Voltage			tbd			mV
Input Impedance			- 2450	tbd		Ohms
Input Capacitance			185	tbd		pF
ECL VEE Supply Current	IEE	0 +25 +70		5 5 5	7 7 7	mA mA mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Relative to GND.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device, either mounted in the test socket or on the printed circuit board.

TTL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage*	VIH	2.0		TTL VCC +0.5	Volts
Input Low Voltage*	VIL	TTL GND −0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			70	µA
Input Low Current (Vin = 0.4 V)	IIL			−0.7	mA
Output High Voltage* (IOH = −2.0 mA)	VOH	2.5			Volts
Output Low Voltage* (IOL = 20 mA)	VOL			0.5	Volts
Three-State Output Current	IOZ				
Vout = VOHmin				10	µA
Vout = VOLmax				−10	µA
Output Capacitance			tbd		pF
Input Capacitance			tbd		pF
TTL VCC Supply Current	ICC		100	130	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

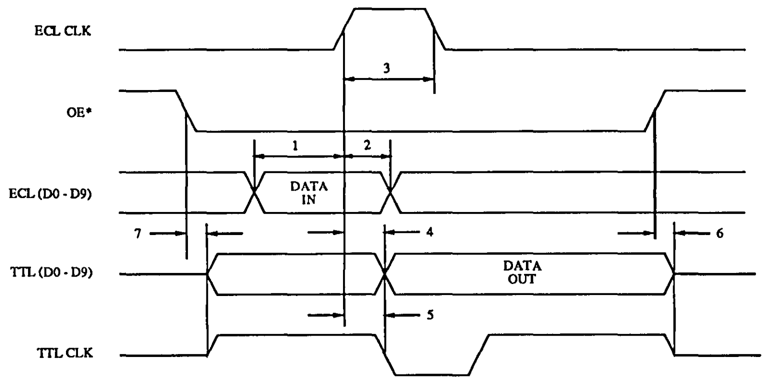
*Relative to GND.

AC Characteristics—Registered Operation

Parameter	Symbol	Min	Typ	Max	Units
ECL D0–D9 Setup Time	1	3			ns
ECL D0–D9 Hold Time	2	3			ns
ECL CLK High Time	3	10			ns
Clock Rate		tbd		27	MHz
TTL D0–D9 Output Delay	4	tbd		10	ns
TTL CLK Output Delay	5	tbd		10	ns
Output Disable Time	6	tbd		15	ns
Output Enable Time	7	tbd		15	ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions." ECL input values are –0.89 to –1.69 V, with input rise/fall times ≤ 4 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Timing Waveforms—Registered Operation



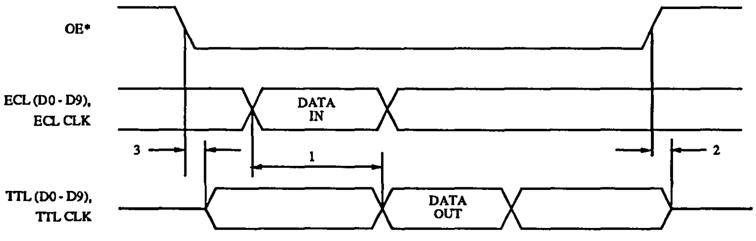
Registered Input/Output Timing.

AC Characteristics—Transparent Operation

Parameter	Symbol	Min	Typ	Max	Units
Output Delay	1	tbd		10	ns
Output Disable Time	2	tbd		15	ns
Output Enable Time	3	tbd		15	ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions." ECL input values are –0.89 to –1.69 V, with input rise/fall times ≤ 4 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Timing Waveforms—Transparent Operation



Transparent Input/Output Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt297KPJ	68-pin Plastic J-lead	0° to +70° C

Bt710

Scaler/Orthogonal Rotator Element (SCORE)

Advance Information

This document contains information on a product under development. Specifications are subject to change without notice.

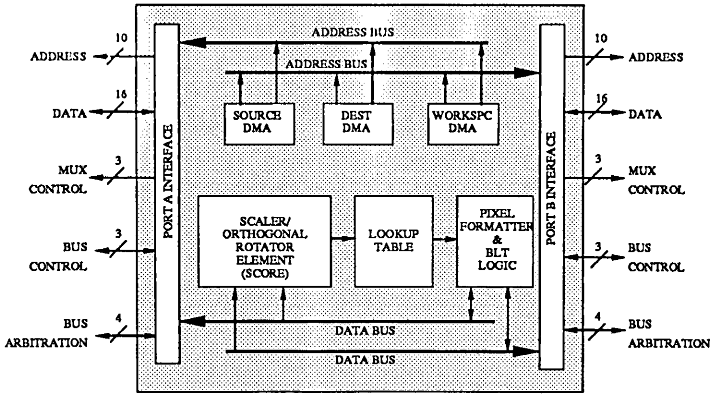
Distinguishing Features

- Arbitrary Scaling of Raster Bit Maps from 5% through 750%
- Scale Down (Reduce) and Scale Up (Enlarge) Capability
- Rotation of +/- 90° and 180°
- Output Image Cropping
- Output Image Bit-aligned Block Transfers (Bitblt)
- Scaler Output of 4-bit Gray Scale
- Output Mapping through Internal 8-bit Lookup Table for 1-, 4-, or 8-bit Output
- 132-pin PGA Package

Applications

- Raster Data Accelerator for Image Viewing and Printing
- Document Imaging Systems Requiring Fast Response Times
- Laser Printer Controllers

Functional Block Diagram


ADDRESS
10
DATA
16
MUX CONTROL
3
BUS CONTROL
3
BUS ARBITRATION
4
PORT A INTERFACE
ADDRESS BUS
ADDRESS BUS
SOURCE DMA
DEST DMA
WORKSPC DMA
SCALER/ ORTHOGONAL ROTATOR ELEMENT (SCORE)
LOOKUP TABLE
PIXEL FORMATTER & BLT LOGIC
DATA BUS
DATA BUS
PORT B INTERFACE
10
ADDRESS
16
DATA
3
MUX CONTROL
3
BUS CONTROL
4
BUS ARBITRATION

Product Description

The Bt710 is a high-speed raster data processor which performs scaling and rotation of bi-level (black and white) raster data. This data is typically raster images created via a scanner or via the expansion of CCITT-coded raster images. The Bt710 allows high-density raster images to be resampled (scaled down) to map to the desired screen or print resolution. Likewise, the Bt710 allows images to be expanded (scaled up) for pixel-level editing and other applications where an image larger than the original is desired.

The heart of the Bt710 is the Scaler/Orthogonal Rotator Engine. This raster engine performs both scaling and rotation functions. The scaler produces a 4-bit gray scale as a result of the scaling algorithm. This gray scale may be retained for output or may be thresholded via programmable threshold logic to bi-level data.

The output of the scaler engine is directed toward an internal look-up table (LUT). The look-up table maps the four bits from the scaler to the contents of the 16 x 8 look-up table. Either one, four, or eight bits may be extracted from the look-up table. The output of the look-up table is directed to DMA logic which supports both packed pixels as well as multiple bit planes.

Bus master interfaces on both ports use direct memory access (DMA) to move all data into and out of the Bt710.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121-2790
(619) 452-7580
(800) VIDEO IC
TLX: 383 596
FAX: (619) 452-1249
L710001 Rev. D

Brooktree®

Functional Overview

Architecture

Conceptually, the Bt710 is a processor which operates upon an input image (source) and creates an output image (destination). The operations which the Bt710 can perform on the source image include scaling, rotation, cropping, and pixel-aligned transfers (blt).

The Bt710 performs this function autonomously through bus master interfaces on its bus interfaces. Thus, the Bt710 is pointed to the start of the source buffer and destination buffer, and provided parameters which specify what operations to perform. Once initiated, the Bt710 will perform the function until completion. Termination can be determined under software polling or via interrupts.

Because the Bt710 operates upon images, the data from the Bt710 is assumed to have two dimensional attributes: width and length. Since images are often placed on pixel boundaries, bit-aligned transfers are performed by the Bt710.

Generally speaking, the Bt710 operates upon an image and outputs an image unless a special "strip" mode of operation is specified. This special mode of operation is described in the section entitled *Strip DMA Operation.*

Scaler/Orthogonal Rotator

The Scaler/Orthogonal Rotator is a raster engine which performs both scaling and rotation functions on a source bi-level image.

Scaler

The Bt710's scaler provides N/M scaling of bi-level raster bitmaps. N can range from 2 through 15. M can range from 2 through 31. Through various combinations of these two parameters, the Bt710 will scale up (enlarge) and scale down (reduce) by factors ranging from 5% through 750%.

When the Bt710 scales a bi-level image, it creates a 4-bit gray scale pixel as a result. The 4-bit gray scale can be taken directly from the scaler or be converted back to bi-level via a programmable threshold register. As an option, the output of the scaler can be mapped through the on-chip look-up table to either 1 bit, 4 bits, or 8 bits of output from the look-up table.

Rotator

The rotator will rotate +/- 90° and 180°. The rotator hardware is shared with the scaler. As a result, the Bt710 must make two passes through the data when both scaling and rotation are desired. A workspace buffer is defined where the Bt710 stores intermediate results during the scale and rotate process. If both scaling and rotation are not performed at once, the workspace buffer is not used.

Pixel Formatter

The pixel format from the SCORE unit or the look-up table is for packed pixels. That is, four 4-bit or two 8-bit or 16 1-bit pixels are contained in each 16-bit word. If the desired output is for separate bit planes, the pixel formatter contains the appropriate logic to separate multibit pixels into separate bit planes.

Blt Logic

The blt logic block provides pixel-aligned block transfer capability on the destination DMA channel. This allows output images to be placed in any position in the destination frame buffer. Additionally, common logic operations may be performed between the output image data and the existing frame buffer data.

Bus Interfaces

The Bt710 contains two complete bus interfaces for two-port operation. Both ports can function independently as bus masters for direct memory access (DMA) of source and destination data for maximum bandwidth. The Bt710 can also function with all bus activity from a single port. The source DMA, destination DMA, and workspace DMA channels can be independently mapped to either port.

The Bt710 utilizes a triple multiplexed address bus and 16-bit data bus on both of its bus interfaces. The address buses provide 24-bits of address allowing the Bt710 to address up to 16 megawords of memory.

The Bt710 can directly interface to 256K, 1M, and 4M DRAMs. The number of address bits output during each phase of the address multiplexing depends upon which RAM density is being supported (Table 1).

An extended cycle is performed during the first memory cycle following acquisition of the bus, or whenever there is a change in the value of the extended address. A row address cycle occurs every memory cycle and outputs the row address for the DRAM. A column address cycle also occurs every memory cycle and outputs the column address for the DRAM.

The Bt710 can also be programmed to provide CAS before RAS refresh of external DRAM and VRAM. When refresh is enabled, the Bt710 will initialize the external RAM with eight CAS before RAS cycles.

Functional Overview (continued)

RAM DENSITY	EXTENDED CYCLE	RAS CYCLE	CAS CYCLE
64K x 4	8	8	8
256K x 4	6	9	9
1024K x 4	4	10	10

Table 1. RAM Size vs. Multiplexing Cycle Sizes.

Bus Request Operation

When the Bt710 arbitrates for the external bus, external arbitration logic does not know if the request is for memory, or if a refresh cycle is pending. To provide this information to external arbitration logic, two bus request pins (REQ1* and REQ0*) are provided on each port. These pins encode the type of request being made as shown in Table 2.

	REQ1*	REQ0*
No Request	H	H
Memory Request	H	L
Initialization Request	L	H
Refresh Request	L	L

Table 2. REQ Encoding*

Strip DMA Operation

An attribute bit in a Bt710 register defines a special case of DMA, called strip DMA mode. Strip DMA mode is a form of DMA chaining where the Bt710 automatically chains between two source buffers. The Bt710 handshakes via two pins or register bits before beginning data transfer from the subsequent buffer area.

Strip DMA mode is intended for use with external processors, which can fill one source buffer while the Bt710 is processing the second source buffer. This pipelining operation allows overlapped processes which can substantially increase throughput. By using strip buffers, an image generated from the decoding of an encoded image, or read from disk, need not be completely buffered in system memory before scaling operations are performed. Thus, strip buffers can substantially reduce the amount of memory required in many applications.

Internal Registers

The Bt710 contains a set of programmable registers by which the Bt710 operational modes may be controlled by host software. A total of 45 registers exist which occupy only 32 consecutive locations. This is accomplished by selectable mapping of the last eight 16-bit locations, via map select bits in the BUS.CNTL Register. These bits select the register set (shown in Table 3) to be mapped to locations 0x08 through 0x0F.

The registers are accessible through port A, and are selected by pins AA3-AA0 during programmed I/O read and write cycles (see Figure 1).

RMAP2	RMAP1	RMAP0	SELECTED REGISTER BLOCK
0	0	0	Source DMA Parameters
0	0	1	Destination DMA Parameters
0	1	0	Workspace DMA Parameters
0	1	1	Engine Parameter Registers
1	0	0	Lookup Table Registers (low bank)
1	0	1	Lookup Table Registers (high bank)

Table 3. Register Select Bits - BUS.CNTL Register.

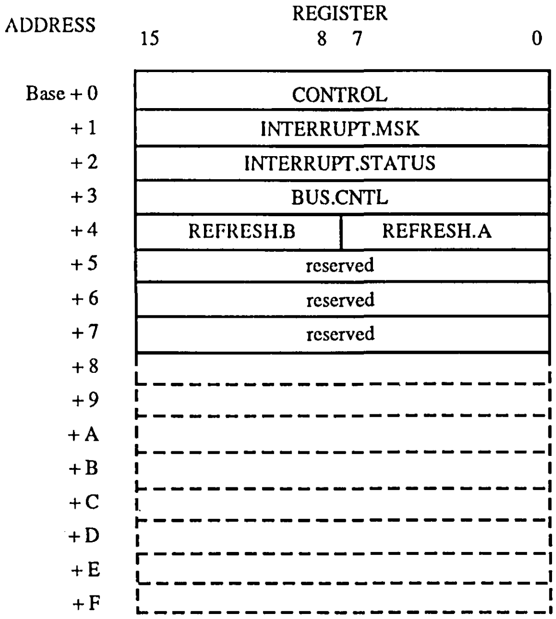

ADDRESS
REGISTER
15
8
7
0
Base + 0
CONTROL
+ 1
INTERRUPT.MSK
+ 2
INTERRUPT.STATUS
+ 3
BUS.CNTL
+ 4
REFRESH.B
REFRESH.A
+ 5
reserved
+ 6
reserved
+ 7
reserved
+ 8
+ 9
+ A
+ B
+ C
+ D
+ E
+ F

Figure 1. Bt701 Registers.

Internal Registers (continued)

CONTROL Register

The CONTROL Register contains several control bits as shown in Figure 2 below:

15 MSB	RUN
14	SCALE
13	ROTATE
12	R_VAL1
11	R_VAL0
10	PIXEL_MODE
9	PIXEL_LEN1
8	PIXEL_LEN0
7	–
6	–
5	–
4	–
3	–
2	–
1	TEST
0 LSB	RESET

Figure 2. CONTROL Register.

The bits in the CONTROL register have the following meanings:

Bit 15	RUN. This bit enables/disables Bt710 operation. 0 - Bt710 halted 1 - Bt710 start operations
Bit 14	SCALE. This bit enables or disables image scaling. 0 - Disable scaling 1 - Enable scaling
Bit 13	ROTATE. This bit enables or disables image rotation. 0 - Disable rotation 1 - Enable rotation
Bit 12,11	RVAL1,RVAL0. These bits select the clockwise rotation value for the Bt710. b'00' - none b'01' - 90° b'10' - 180° b'11' - 270°
Bit 10	PIXEL_MODE. This bit selects the format of multi-bit pixels when output from the Bt710. 1 - Packed pixels 0 - Plane pixels
Bit 9,8	PIXEL_LEN1,PIXEL_LEN0. These bits determine the number of bits to be extracted from the look-up table. b'00' - 1 bit per pixel b'01' - 4 bits per pixel b'10' - 8 bits per pixel b'11' - reserved
Bit 1	TEST. This bit reserved for manufacturing tests.
Bit 0	RESET. This bit provides a software reset function. After writing one to this bit, the 710 is reset, put in a halted state, and then this bit is automatically cleared.

Internal Registers (continued)

INTERRUPT.MSK Register

The INTERRUPT.MSK register is used to control the masking and generation of hardware interrupts presented on the INT* pin (see Figure 3).

15 MSB	MIE
14	SRC_HLT_MSK
13	DST_HLT_MSK
12	SBA_MSK
11	DBF_MSK
10	-
9	-
8	-
7	-
6	-
5	-
4	-
3	-
2	-
1	-
0 LSB	-

Figure 3. INTERRUPT.MSK Register.

The bits in the INTERRUPT.MSK register have the following meanings:

Bit 15 MIE. This bit provides a master interrupt enable for all interrupts.

0 - Disable all interrupts
1 - Enable all interrupts

Bit 14 SRC_HLT_MSK. This bit controls the masking of source DMA done interrupts.

0 - Disable this interrupt
1 - Enable this interrupt

Bit 13 DST_HLT_MSK. This bit controls the masking of destination DMA done interrupts.

0 - Disable this interrupt
1 - Enable this interrupt

Bit 12 SBA_MSK. This bit controls the masking of source buffer available interrupts.

0 - Disable this interrupt
1 - Enable this interrupt

Bit 11 DBF_MSK. This bit controls the masking of destination buffer available interrupts.

0 - Disable this interrupt
1 - Enable this interrupt

INTERRUPT.STATUS Register

The INTERRUPT.STATUS register is a read-only register which reports the cause of interrupts (Figure 4). Alternatively, this register may be polled under software control. Writing any value to this register causes the interrupt condition to be cleared.

15 MSB	SRC_HLT
14	DST_HLT
13	SBA
12	DBA
11	-
10	-
9	-
8	-
7	-
6	-
5	-
4	-
3	-
2	-
1	-
0 LSB	-

Figure 4. INTERRUPT.STATUS Register.

The bits in the INTERRUPT.STATUS register have the following meaning:

Bit 15 SRC_HLT. This bit indicates if the source DMA channel is done.

0 - Source DMA active
1 - Source DMA halted

Bit 14 DST_HLT. This bit indicates if the destination DMA channel is done.

0 - Destination DMA active
1 - Destination DMA halted

Internal Registers (continued)

Bit 13 SBA. This bit indicates if the source buffer is available for additional data. It is equivalent to the pin by the same name.

0 - Source buffer not available
1 - Source buffer available

BUS.CNTL Register

The BUS.CNTL register provides bits for controlling refresh operations, address multiplexing on both Port A and Port B, and shadow register mapping (see Figure 5). The bits in the BUS.CNTL register have the following meanings:

15 MSB	RAMSIZE_B_1
14	RAMSIZE_B_0
13	RAMSIZE_A_1
12	RAMSIZE_A_0
11	REFRESH_B
10	REFRESH_A
9	–
8	–
7	–
6	–
5	–
4	–
3	–
2	RMAP2
1	RMAP1
0 LSB	RMAP0

Figure 5. BUS.CNTL Register.

Bit 15,14 RAMSIZE_B_1,RAMSIZE_B_0. These bits define the size of the external DRAM on Port B. They affect address multiplexing as shown in Table 1.

b'00' - 64K x 4 DRAM
b'01' - 256K x 4 DRAM
b'10' - 4M x 4 DRAM

Bit 13,12 RAMSIZE_A_1,RAMSIZE_A_0. These bits define the size of the external DRAM on Port A. They affect address multiplexing as shown in Table 1.

b'00' - 64K x 4 DRAM
b'01' - 256K x 4 DRAM
b'10' - 4M x 4 DRAM

Bit 11 REFRESH_B. This bit enables refresh for DRAM on Port B. When refresh is enabled, the Bt710 performs DRAM initialization prior to beginning refresh operations.

0 - Disable refresh on Port B
1 - Enable refresh on Port B

Bit 10 REFRESH_A. This bit enables refresh for DRAM on Port A. When refresh is enabled, the Bt710 performs DRAM initialization prior to beginning refresh operations.

0 - Disable refresh on Port A
1 - Enable refresh on Port A

Bit 2-0 RMAP2,RMAP1,RMAP0. These bits control the mapping of registers to the last eight locations of the Bt710 register map (see Table 3).

REFRESH.A Register

The REFRESH.A register selects the refresh interval the Bt710 will use if DRAM refresh has been enabled for Port A. The refresh interval is given by the following equation:

$$\text{Interval (ns)} = 4 \cdot \text{CLOCK cycle time} \cdot \text{REFRESH.A}$$

REFRESH.B Register

The REFRESH.B register selects the refresh interval the Bt710 will use if DRAM refresh has been enabled for Port B. The refresh interval is given by the following equation:

$$\text{Interval (ns)} = 4 \cdot \text{CLOCK cycle time} \cdot \text{REFRESH.B}$$

Internal Registers (continued)

Source DMA Channel Registers

The source DMA channel registers are selected via the RMAP bits of the BUS.CNTL register (Figure 6).

ADDRESS	REGISTER 15–8	REGISTER 7–0
Base + 8	SRC.CNTL	SRC.ADR.1
+9	SRC.ADR.1	
+A	–	SRC.ADR.2
+B	SRC.ADR.2	
+C	SRC.PITCH	
+D	SRC.LINE.LEN	
+E	SRC.LINE.CNT	

Figure 6. Source DMA Channel Registers.

SRC.CNTL Register

This register provides additional control information for source DMA operations (Figure 7).

BIT	
7 MSB	SBF
6	STRIP2
5	STRIP1
4	STRIP0
3	–
2	PORT
1	SRC_ORD_1
0	SRC_ORD_0

Figure 7. SRC.CNTRL Register.

The bits in the SRC.CNTL register have the following meanings:

Bit 7 SBF. This bit is intended as a software handshake bit which can be used in lieu of the pin by the same name.

0 - Source buffer is not full
1 - Source buffer is full

Bit 6–4 STRIP2–STRIP0. These bits select the size, in image lines, of the strip buffer for the source data. These bits have the following encode:

b'000' - Strip Mode Disabled
b'001' - 32 line strip buffer
b'010' - 64 line strip buffer
b'011' - 128 line strip buffer
b'100' - 256 line strip buffer
b'101' - 512 line strip buffer
b'110' - 1024 line strip buffer
b'111' - 2048 line strip buffer

Bit 2 PORT. This bit selects to which port the source DMA will occur.

0 - Map source DMA on Port A
1 - Map source DMA on Port B

Bit 1,0 SRC_ORD1, SRC_ORD0. These bits define the bit and byte order of source data. See Figure 8.

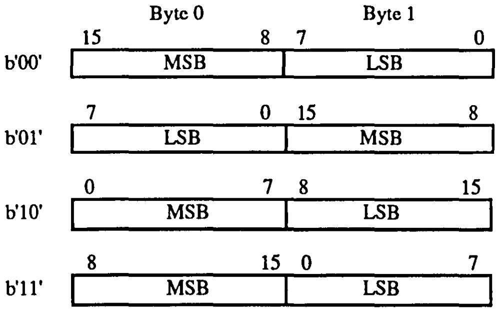


Figure 8. SRC_ORDER Decode.

Internal Registers (continued)

SRC.ADR.1 Register

The SRC.ADR.1 register contains the starting address of the first of two source buffers if strip mode is selected via the STRIP bits of the SRC.CNTRL register. If strip mode is not selected, then this register contains the normal starting address for source DMA operations. The least-significant bit of the address provides an address resolution of one 16-bit word.

SRC.ADR.2 Register

The SRC.ADR.2 register contains the starting address of the second of two source buffers if strip mode is selected via the STRIP bits of the SRC.CNTL register. If strip mode is not selected, then this register is ignored. The least-significant bit of the address provides an address resolution of one 16-bit word.

SRC.PITCH Register

The SRC.PITCH register contains the pitch of the frame buffer containing the source image. Pitch is the distance in words from one line to the next.

SRC.LINE.LEN Register

The SRC.LINE.LEN register specifies the line length of the source image. This parameter is the line length expressed in words.

SRC.LINE.COUNT Register

The SRC.LINE.COUNT register defines how many lines are contained in the source image. When the number of lines (as specified by this register) has been read by the Bt710, source DMA halts.

Destination DMA Channel Registers

These registers provide additional information for destination DMA operations (Figure 9).

ADDRESS	REGISTER	
	15 8	7 0
Base + 8	DST.CNTL	DST.ADR.1
+9	DST..ADR.1	
+A	–	–
+B	–	
+C	DST.PITCH	
+D	DST.LINE.LEN	
+E	DST.LINE.CNT	
+F	PLANE.PITCH	

Figure 9. Destination DMA Channel Registers.

Internal Registers (continued)

DST.CNTL Register

This register provides additional control information for destination DMA operations (Figure 10).

BIT	
7 MSB	DBA
6	STRIP2
5	–
4	–
3	–
2	PORT
1	DST_ORD_1
0	DST_ORD_0

Figure 10. DST.CNTL Register.

The bits in the DST.CNTL register have the following meanings:

Bit 7 DBA. This bit is intended as a software handshake bit which can be used in lieu of the pin by the same name.

0 - Destination buffer not available.
1 - Destination buffer available.

Bit 2 PORT. This bit selects to which port the destination DMA operations will be mapped.

1 - Destination DMA mapped to Port B
0 - Destination DMA mapped to Port A

Bit 1,0 DST_ORD1, DST_ORD0. These bits define the bit and byte order of destination data (see Figure 11).

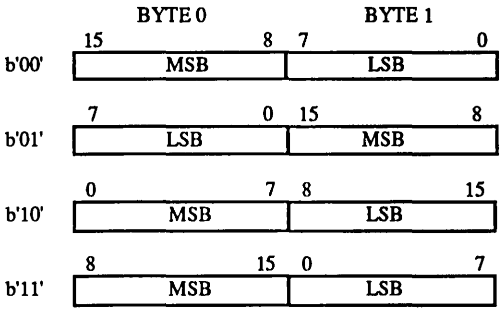


Figure 11. DST_ORDER Decode.

Internal Registers (continued)

DST.ADR.1 Register

This register contains the normal starting address for destination DMA operations. The least-significant bit of the address provides an address resolution of one 16-bit word.

DST.PITCH Register

The DST.PITCH register contains the pitch of the frame buffer in words. Pitch is the distance in words from one line to the next.

DST.LINE.LEN Register

The DST.LINE.LEN register specifies the line length of the destination image. This parameter is the line length expressed in words.

DST.LINE.COUNT Register

The DST.LINE.COUNT register defines how many lines are contained in the destination image. When the number of lines (as specified by this register) has been written by the Bt710, destination DMA halts.

PLANE.PITCH Register

This register specifies the pitch between bit planes when the Bt710 performs bit plane writes of 4-bit or 8-bit pixels. This parameter is the offset in words on a 32-word boundary (the five least-significant bits are not specified and assumed to be zero). For example, a value of 0x0001 for this parameter specifies a 32-word offset between consecutive bit planes. The actual offset is given by 32* PLANE.PITCH.

Workspace DMA Channel Registers

These registers provide additional information for workspace DMA operations (Figure 12).

ADDRESS	REGISTER 15 – 8	REGISTER 7 – 0
Base + 8	WORK.CNTL	WORK.ADR
+9	WORK.ADR	
+ A	WORK.LINE.LEN	

Figure 12. Workspace DMA Channel Registers.

Internal Registers (continued)

WORK.CNTL Register

This register provides additional control information for workspace DMA operations (Figure 13).

BIT	
7 MSB	REMOTE
6	PORT
5	—
4	—
3	—
2	—
1	—
0	—

Figure 13. WORK.CNTL Register.

The bits in the WORK.CNTL register have the following meanings:

Bit 7 REMOTE. This bit specifies whether the bus request should be local or remote (state of REQ1* and REQ0* during arbitration).

0 - local request
1 - remote request

Bit 6 PORT. This bit selects to which port the workspace DMA operations will be mapped.

0 - Workspace DMA mapped to Port A
1 - Workspace DMA mapped to Port B

WORK.ADR Register

This register contains the starting address of the workspace buffer. This address is 24 bits and is a word address parameter.

WORK.LINE.LEN Register

The WORK.LINE.LEN register specifies the number of words per line in the workspace buffer.

Engine Parameter Registers

The Engine Parameter registers provide additional information with regard to pixel-aligned block transfer operations on the destination buffer (Figure 14).

ADDRESS	REGISTER 15 8	 7 0
Base + 8	BLT.FNCTS	GREY.ADJ
+ 9	SRC.MARGINS	DST.MARGINS
+ A	NVAL	MVAL

Figure 14. BLT Parameter Registers.

Internal Registers (continued)

BLT.FNCTS Register

This register contains 4 bits which define the logical operation between the output image and the existing contents of the destination buffer (Figure 15 and Table 4).

BIT	
15 MSB	BLT_FNCT_3
14	BLT_FNCT_2
13	BLT_FNCT_1
12	BLT_FNCT_0
11	–
10	–
9	–
8	–

Figure 15. BLT.FNCTS Register.

3	2	1	0	FUNCTION
0	0	0	0	0
0	0	0	1	s AND d
0	0	1	0	s AND NOT d
0	0	1	1	s
0	1	0	0	NOT s AND d
0	1	0	1	d
0	1	1	0	s XOR d
0	1	1	1	s OR d
1	0	0	0	NOT s AND NOT d
1	0	0	1	s XNOR d
1	0	1	0	NOT d
1	0	1	1	s OR NOT d
1	1	0	0	NOT s
1	1	0	1	NOT s OR d
1	1	1	0	NOT s OR NOT d
1	1	1	1	1

Table 4. BLT.FNCTS Operations.

GRAY.ADJ Register

The GRAY.ADJ register contains bits which control the gray scale output from the scaler (Figure 16).

BIT	
7 MSB	SELECT2
6	SELECT1
5	SELECT0
4	GAIN4
3	GAIN3
2	GAIN2
1	GAIN1
0 LSB	GAIN0

Figure 16. GREY.ADJ Register.

SRC.MARGINS Register

The SRC.MARGINS register specifies a left and right margin offset into the 16-bit word at the start and end of each line (Figure 17).

BIT	
15 MSB	SRC_LM3
14	SRC_LM2
13	SRC_LM1
12	SRC_LM0
11	SRC_RM3
10	SRC_RM2
9	SRC_RM1
8 LSB	SRC_RM0

Figure 17. SRC.MARGINS Register.

Internal Registers (continued)

DST.MARGINS Register

The DST.MARGINS register specifies a left and right margin offset into the 16-bit word at the start and end of each line (Figure 18).

BIT	
7 MSB	DST_LM3
6	DST_LM2
5	DST_LM1
4	DST_LM0
3	DST_RM3
2	DST_RM2
1	DST_RM1
0 LSB	DST_RM0

Figure 18. DST.MARGINS Register.

NVAL Register

The NVAL register contains the numerator portion of the N/M scale factor. This 4-bit value is left justified within the byte (MSB is equal to bit 15, LSB is equal to bit 12). The full scale factor is given by:

SCALE FACTOR (%) = N/M • 100

N must be in the range from 2 through 15.

MVAL Register

The MVAL register contains the denominator portion of the /M scale factor. This 4-bit value is right justified within the byte (MSB is equal to bit 3, LSB is equal to bit 0). The full scale factor is given by :

SCALE FACTOR (%) = N/M • 100

M must be in the range from 2 through 31.

Lookup Table Registers

The lookup table registers specify the content of the lookup table used to map the 4 bits of scaler output to 1-, 4-, or 8-bit pixels (Figures 19 and 20). There are 16 eight-bit registers.

When 1 bit is extracted from each table location, the bit taken is the most-significant bit. When 4 bits are extracted from each table location, the 4 least-significant bits are taken.

These registers are selected via the RMAP bits of the CONTROL.1 register.

ADDRESS	REGISTER 15–8	REGISTER 7–0
Base + 8	reserved	LUT.0
+9	reserved	LUT.1
+ A	reserved	LUT.2
+ B	reserved	LUT.3
+ C	reserved	LUT.4
+ D	reserved	LUT.5
+ E	reserved	LUT.6
+ F	reserved	LUT.7

Figure 19. Lookup Table Registers Low.

ADDRESS	REGISTER 15–8	REGISTER 7–0
Base + 8	reserved	LUT.8
+9	reserved	LUT.9
+ A	reserved	LUT.10
+ B	reserved	LUT.11
+ C	reserved	LUT.12
+ D	reserved	LUT.13
+ E	reserved	LUT.14
+ F	reserved	LUT.15

Figure 20. Lookup Table Registers High.

Pin Descriptions

Pin Name	I/O	Description
AA<9–0>	I/O	Port A Address Bus. Pins AA9 (MSB) through AA0 (LSB) comprise a triple multiplexed address bus. The first phase is termed the extended address cycle. The next two phases are termed the RAS and CAS DRAM cycles. On the falling edge of AXAL*, AA9–AA0 contain the extended address bits. On the falling edge of ARAS*, AA9–AA0 contain the row address. On the falling edge of ACAS*, AA9–AA0 contain the column address. During programmed I/O operations, AA3–AA0 are inputs and select the internal register to be read or written by the MPU. When DMA is not active, this bus is high-7.
ARAS*	OUT	Port A Row Address Strobe. This pin is asserted when the row address has been placed on AA9–AA0. When DMA is not active, this pin is high-7.
ACAS*	OUT	Port A Column Address Strobe. This pin is asserted when the column address has been placed on AA9–AA0. When DMA is not active, this pin is high-7.
AXAL*	OUT	Port A Extended Address Latch Enable. This pin is asserted when an extended address cycle is performed to output the high-order address bits on AA9-AA0. AXAL is activated prior to the first cycle of each DMA transfer and thereafter as necessary (whenever the extended address changes). The number of bits which are output on an extended cycle depends upon the DRAM size specification provided in the CONTROL.2 register. The Bt710 will always output 24 bits of address in a triple multiplexed fashion. This output is never put in high-7 state.
AD<15–0>	I/O	Port A Data Bus. These pins comprise the 16-bit bi-directional data bus. AD15 is the most-significant bit and AD0 is the least-significant bit. When DMA is not active, this bus is high-7.
ADS*	I/O	Port A Data Strobe. During DMA operations, this pin is an output and is asserted when output data will be placed on the data bus during DMA writes. It is asserted during DMA reads to indicate to the slave device that input data may be placed on the data bus. During bus slave operations, this pin is an input and should be asserted when write data is valid or when read data should be output on the data bus.
ACS*	IN	Port A Chip Select. This pin, when active-low, enables access to the internal registers.
AR/W*	I/O	Port A Read Not Write Strobe. During DMA operations, this pin is an output. During programmed I/O operations, this pin is an input. During bus cycles, this signal differentiates between read and write cycles.
ARDY*	I/O	Port A Ready. During DMA operations, this pin is an input. During bus slave operations, this pin is an output. This signal is asserted to indicate that the current bus cycle may be completed. If not asserted prior to first being sampled by the Bt710, wait states will be added to the current DMA cycle.
AGNT*	IN	Port A Bus Grant. This pin is an input which grants the Bt710 access to the bus.
AREQ1*	OUT	Port A Bus Request 1. This pin, in conjunction with AREQ0*, requests access to the Port A and remains active until AGNT* is asserted. The encode for AREQ1* and AREQ0* is shown in Table 2.
AREQ0*	OUT	Port A Bus Request 0. This pin is the second of two encoded bus requests output when access to Port A is requested. Table 2 lists the encode for these two bus requests.

Pin Descriptions (continued)

Pin Name	I/O	Description
AOWN	OUT	Port A Bus Owned. This output goes active-high during DMA cycles to indicate to external devices that the Bt710 has control of the Port A bus. When DMA is not active, this pin is high-Z.
BA<9–0>	OUT	Port B Address Bus. Pins BA9 (MSB) through BA0 (LSB) comprise a triple multiplexed address bus. The first phase is termed the extended address cycle. The second two phases are termed the RAS and CAS DRAM cycles. On the falling edge of BXAL*, BA9–BA0 contain the extended address bits. On the falling edge of BRAS*, BA9–BA0 contain the row address. On the falling edge of BCAS*, BA9–BA0 contain the column address. When DMA is not active, this pin is high-Z.
BRAS*	OUT	Port B Row Address Strobe. This pin is asserted when the row address has been placed on BA9–BA0.
BCAS*	OUT	Port B Column Address Strobe. This pin is asserted when the column address has been placed on BA9–BA0. When DMA is not active, this pin is high-Z.
BXAL*	OUT	Port B Extended Address Latch Enable. This pin is asserted when an extended address cycle is performed to output the high-order address bits on BA9–BA0. BXAL* is activated prior to the first cycle of each DMA transfer and thereafter as necessary (i.e., whenever an increment of the DMA address counter causes a carry out of the lower bits). The number of bits which are output on an extended cycle depends upon the DRAM size specification provided in the control register. The Bt701 will always output 24 bits of address in a triple multiplexed fashion. This output is never put in a high-Z state.
BD<15–0>	I/O	Port B Data Bus. These pins comprise the 16-bit bi-directional data bus. BD15 is the most-significant bit and BD0 is the least-significant bit. When DMA is not active, this bus is high-Z.
BDS*	OUT	Port B Data Strobe. During DMA operations, this pin is an output and is asserted when output data will be placed on the data bus during DMA writes. It is asserted during DMA reads to indicate to the slave device that input data may be placed on the data bus. When DMA is not active, this bus is high-Z.
BR/W*	OUT	Port B Read Not Write Strobe. This pin differentiates between read and write cycles. When DMA is not active, this pin is high-Z.
BRDY*	IN	Port B Ready. During DMA operations, this input is asserted to indicate that the current bus cycle may be completed. If not asserted prior to first being sampled by the Bt710, wait states will be added to the the current DMA cycle.
BGNT*	IN	Port B Bus Grant. This pin is an input which grants the Bt710 access to the bus.
BREQ1*	OUT	Port B Bus Request 1. This pin, in conjunction with BREQ0*, requests access to the Port B and remains active until BGNT* is asserted. The encode for BREQ1* and BREQ0* is shown in Table 2.
BREQ0*	OUT	Port B Bus Request 0. This pin is the second of two encoded bus requests output when access to port B is requested. Table 2 lists the encode for these two bus requests.

Pin Descriptions (continued)

Pin Name	I/O	Description
BOWN	OUT	Port B Bus Owned. This output goes active-high during a DMA cycle to indicate to external devices that the Bt710 has control of the Port B bus. When DMA is not active, this pin is high-7.
SBF*	IN	Source Buffer Full. This input is from an external processor such as the Bt701 which, when driven low, indicates that the next available source buffer is full. This input must stay low until the SBA* output is driven low. When strip mode is not enabled, this input is ignored.
SBA*	OUT	Source Buffer Available. This output is driven low when the SBF* has been sampled low and the next available source buffer is available to the external processor. This output remains low until the SBF* input is sampled high. When strip mode is not enabled, this output remains high.
INT*	OUT	Interrupt. This active-low output indicates a request by the Bt701 for interrupt servicing by the host processor. The interrupt reason and interrupt enable/disable may be controlled via the register interface on the Bt710.
RESET*	IN	Reset. When driven low, the Bt710 operation is halted and put into a known state. This pin contains an internal pull-up resistor.
CLOCK	IN	External clock input. This input supplies the internal clock signal for timing the Bt701 state machines and bus timing. This clock is 2x the internal clock.
TEST*	IN	Test Pin. This pin is intended for manufacturing tests and should be left disconnected in normal use. This pin contains an internal pull-up resistor causing the input to remain high when unconnected.
VDD	IN	Power supply. All VDD pins must be connected to a common power supply system. This supply is nominally 5V.
VSS	IN	Ground Connections. All VSS pins must be connected to the common ground system.

Pin Descriptions (continued)

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
AD9	C3	SBF*	P7	BD10	D14
VSS	B2	RESET*	P8	VSS	D13
AD10	A1	n/c	N8	BD9	D12
AD11	D3	VDD	M8	n/c	C14
AD12	C2	BRDY*	P9	n/c	C13
AD13	B1	BGNT*	N9	n/c	B14
VSS	C1	VSS	M9	n/c	C12
VDD	E3	n/c	P10	n/c	B13
AD14	D2	SBA*	N10	n/c	A14
AD15	D1	VSS	M10	VDD	A13
AA0	E2	BREQ0*	P11	VDD	B12
AA1	F3	BREQ1*	N11	BD8	C11
VSS	E1	BOWN	M11	BD7	A12
AA2	F2	VDD	P12	BD6	B11
AA3	F1	BR/W*	N12	VSS	A11
AA4	G3	n/c	P13	BD5	C10
AA5	G2	n/c	M12	BD4	B10
AA6	G1	n/c	N13	BD3	A10
VSS	H1	BXAL	P14	VSS	C9
VDD	J1	BCAS*	N14	BD2	B9
AA7	K1	VSS	M13	BD1	A9
AA8	K2	BRAS*	L12	BD0	C8
AA9	L1	BDS*	M14	VSS	B8
ADS*	K3	BA9	L13	VDD	A8
ARAS*	M1	BA8	L14	AD0	A7
VSS	L2	BA7	K12	AD1	B7
ACAS*	N1	VDD	K13	VSS	C7
AXAL	L3	VSS	K14	AD2	A6
n/c	M2	BA6	J12	AD3	B6
n/c	M3	BA5	J13	VDD	C6
n/c	N2	BA4	J14	AD4	A5
n/c	P1	BA3	H12	AD5	B5
AR/W*	P2	BA2	H13	VSS	C5
VDD	N3	VSS	H14	AD6	A4
ARDY*	M4	BA1	G14	AD7	B4
AOWN	P3	BA0	G13	VDD	C4
VSS	N4	VSS	G12	AD8	A3
AREQ1*	P4	BD15	F14	n/c	B3
AREQ0*	M5	BD14	F13	n/c	A2
INT*	N5	VDD	F12	VSS	H2
VSS	P5	BD13	E14	VSS	H3
CLK	M6	BD12	E13	VDD	J2
VDD	N6	BD11	E12	VDD	J3
TEST	P6				
ACS*	M7				
AGNT*	N7				

Pin Descriptions (continued)

FOR EVALUATIVE PURPOSES ONLY. Contact the Factory for Final Pin Out.

Bt710

(TOP VIEW)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
14	nc	nc	nc	BD10	BD13	BD15	BA1	VSS	BA4	VSS	BA8	BDS*	BCAS*	BXAL
13	VDD	nc	nc	VSS	BD12	BD14	BA0	BA2	BA5	VDD	BA9	VSS	nc	nc
12	BD7	VDD	nc	BD9	BD11	VDD	VSS	BA3	BA6	BA7	BRAS*	nc	BR/W*	VDD
11	VSS	BD6	BD8									BOWN	BREQ1	BREQ0
10	BD3	BD4	BD5									VSS	SBA*	nc
9	BD1	BD2	VSS									VSS	BGNT*	BRDY*
8	VDD	VSS	BD0									VDD	nc	RESET*
7	AD0	AD1	VSS									ACS*	AGNT*	SBF*
6	AD2	AD3	VDD									CLK	VDD	TEST
5	AD4	AD5	VSS									AREQ0	INT*	VSS
4	AD6	AD7	VDD									ARDY*	VSS	AREQ1
3	AD8	nc	AD9	AD11	VDD	AA1	AA4	VSS	VDD	ADS*	AXAL	nc	VDD	AOWN
2	nc	VSS	AD12	AD14	AA0	AA2	AA5	VSS	VDD	AA8	VSS	nc	nc	AR/W*
1	AD10	AD13	VSS	AD15	VSS	AA3	AA6	VSS	VDD	AA7	AA9	ARAS*	ACAS*	nc

alignment marker (on top)

FOR EVALUATIVE PURPOSES ONLY. Contact the Factory for Final Pin Out.

(BOTTOM VIEW)

	P	N	M	L	K	J	H	G	F	E	D	C	B	A
14	BXAL	BCAS*	BDS*	BA8	VSS	BA4	VSS	BA1	BD15	BD13	BD10	nc	nc	nc
13	nc	nc	VSS	BA9	VDD	BA5	BA2	BA0	BD14	BD12	VSS	nc	nc	VDD
12	VDD	BR/W*	nc	BRAS*	BA7	BA6	BA3	VSS	VDD	BD11	BD9	nc	VDD	BD7
11	BREQ0	BREQ1	BOWN									BD8	BD6	VSS
10	nc	SBA*	VSS									BD5	BD4	BD3
9	BRDY*	BGNT*	VSS									VSS	BD2	BD1
8	RESET*	nc	VDD									BD0	VSS	VDD
7	SBF*	AGNT*	ACS*									VSS	AD1	AD0
6	TEST	VDD	CLK									VDD	AD3	AD2
5	VSS	INT*	AREQ0									VSS	AD5	AD4
4	AREQ1	VSS	ARDY*									VDD	AD7	AD6
3	AOWN	VDD	nc	AXAL	ADS*	VDD	VSS	AA4	AA1	VDD	AD11	AD9	nc	AD8
2	AR/W*	nc	nc	VSS	AA8	VDD	VSS	AA5	AA2	AA0	AD14	AD12	VSS	nc
1	nc	ACAS*	ARAS*	AA9	AA7	VDD	VSS	AA6	AA3	VSS	AD15	VSS	AD13	AD10

Application Information

Bt710 Parameters and Data Structures

Source DMA Parameters

Figure 21 illustrates the parameters used by the Bt710 for source DMA operations.

The SRC.PITCH parameter, specified in the register by the same name, defines the pitch of the frame buffer from which the source image is to be read. This parameter is the distance in words to the next line.

The SRC.ADR.1 parameter is a 24-bit address pointer to the first word of the source image. This parameter is specified in the register by the same name. *Note that the source image must be specified on a word boundary.*

The SRC.LINE.LEN parameter specifies the length of the source image line in 16-bit words. This parameter is specified in the register by the same name.

The SRC.LM and SRC.RM parameters specify the left and right margin offsets respectively. These parameters are found in the SRC.MARGINS register. See the description for DST.LM and DST.RM in the next section.

The SRC.LINE.COUNT parameter specifies the total number of raster lines in the source image. This parameter is specified in the register by the same name.

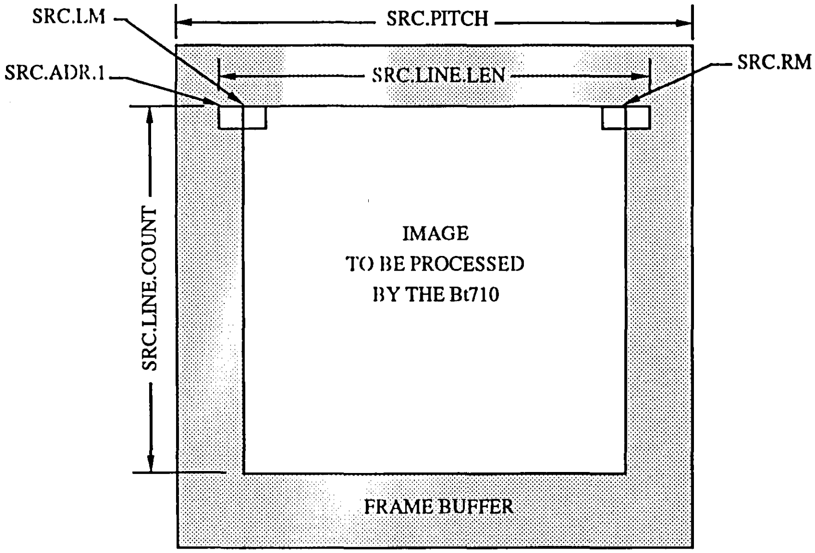


Figure 21. Source X-Y DMA Parameters.

Application Information (continued)

Destination DMA Parameters

Figure 22 illustrates the parameters used by the Bt710 for destination DMA transfers. The destination DMA channel is capable of full bit-aligned block transfer to a destination frame buffer.

The DST.PITCH parameter specifies the pitch of the frame buffer that will contain the destination image. The parameter is specified in the register by the same name. DST.PITCH is expressed in words.

The DST.ADR.1 parameter is a 24-bit address pointer to the first word of the destination image. This parameter is specified in the register by the same name. When rotation is performed, DST.ADR.1 points to the first word of the image.

The DST.LM parameter specifies the left pixel offset in the word pointed to the DST.ADR.1 in which the image is to be placed. This is illustrated in Figure 23. This parameter allows images to be placed on pixel boundaries in the destination frame buffer. The DST.LM parameter is contained in the DST.MARGINS register. If the output pixels are packed 4-bit or 8-bit pixels, the DST.LM register must be on a 4-bit or 8-bit boundary as appropriate. Other values in this case will cause unpredictable operation.

The DST.LINE.LEN parameter specifies the number of words in one output line. This parameter is specified in the register by the same name.

If a DST.LINE.LEN parameter is specified which is *not equal* to the line length as a result of scaling and rotation, then unpredictable operation will occur.

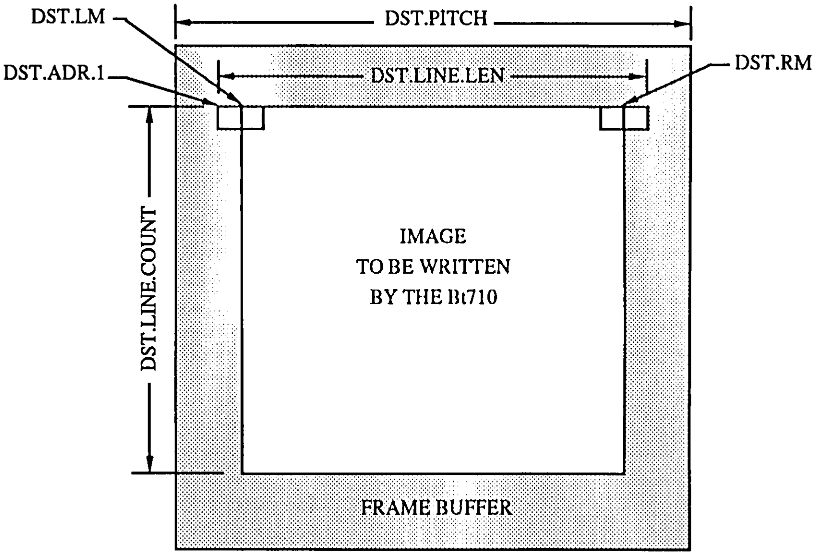


Figure 22. Destination X-Y DMA Parameters.

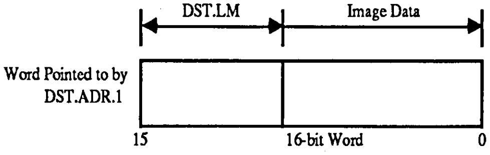


Figure 23. DST.LM Parameter.

Application Information (continued)

The DST.LINE.COUNT parameter specifies the total number of lines in the output image. If the end of image occurs before DST.LINE.COUNT occurs, Bt710 processing halts. If DST.LINE.COUNT is reached before the end of image occurs, the remaining lines of the output image are discarded.

The DST.RM parameter specifies the pixel boundary on the end of image as shown in Figure 24. The DST.RM parameter is contained in the DST.MARGINS register.

If 4-bit or 8-bit packed pixels are output, then the DST.RM parameter must be specified on a 4-bit or 8-bit boundary respectively. Other values will cause unpredictable operation.

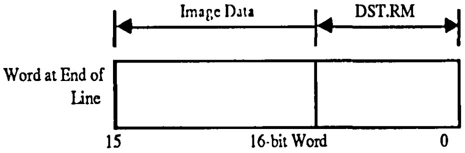


Image Data
DST.RM
Word at End of Line
15
16-bit Word
0

Figure 24. DST.RM Parameter.

Bt710 Buffer Options

The Bt710 functions with a source buffer, a destination buffer, and a workspace buffer. The workspace buffer is only needed when both scaling and rotation are to be performed on the source image.

These buffers can be independently mapped to either of the two bus ports on the Bt710. Figure 25 illustrates the basic configuration where all three buffers are mapped on one port.

Alternately, the Bt710 may be operated as a two-port device. Typically, the source image buffer and workspace buffer will be mapped to one port and the destination image buffer will be mapped to the second port. This example is shown in Figure 26.

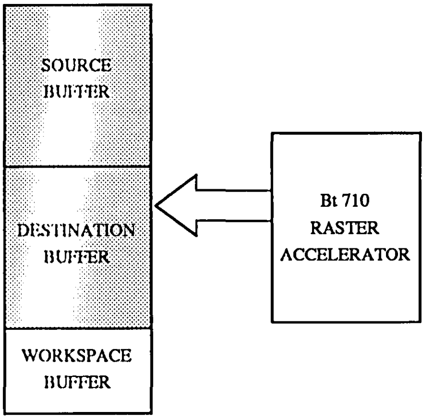

SOURCE BUFFER
DESTINATION BUFFER
WORKSPACE BUFFER
Bt 710 RASTER ACCELERATOR

Figure 25. Single Port Configuration.

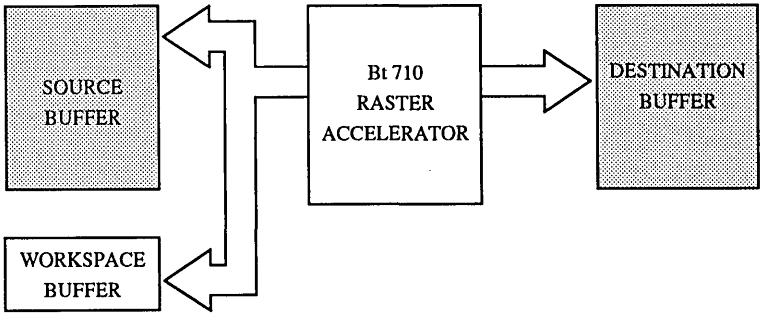

SOURCE BUFFER
WORKSPACE BUFFER
Bt 710 RASTER ACCELERATOR
DESTINATION BUFFER

Figure 26. Dual Port Configuration.

Application Information (continued)

Strip DMA Operation

The STRIP2–0 bits in the SRC.CNTL register enable a special case of DMA called Strip DMA Mode. This mode facilitates efficient transfer of image data to the Bt710 by allowing image data to be passed to the Bt710 in small buffers called "strips." Thus, if the image is to be scaled or manipulated in some fashion, it need not be completely stored in memory before beginning Bt710 operation.

Figure 27 illustrates strip buffer usage on the source.

When the source DMA channel has been programmed for strip DMA mode (STRIP2–STRIP0 bits in the control register non-zero), the channel performs a type of circular chained DMA operation. When DMA has been completed to one buffer, the channel chains to the second buffer. After the second buffer is read, DMA chains back to the first buffer. However, before DMA operations begin to a buffer, a handshake is performed by two pins on the bus interface or bits in a register to assure buffer availability. The size of the strip buffers is controlled by the STRIP2–STRIP0 bits (see the SRC.CNTL register).

Since there are two buffers, a pipeline operation may be configured if the two buffers are individually banked, or if the buffers are dual ported as would be the case if dual port video DRAM (VRAM) were used. Thus, while an external processor is filling one buffer, the Bt710 can be reading and processing the second buffer.

The handshake which occurs between an external processor is through two pins. The use of these two pins with the external hardware is shown in Figure 28.

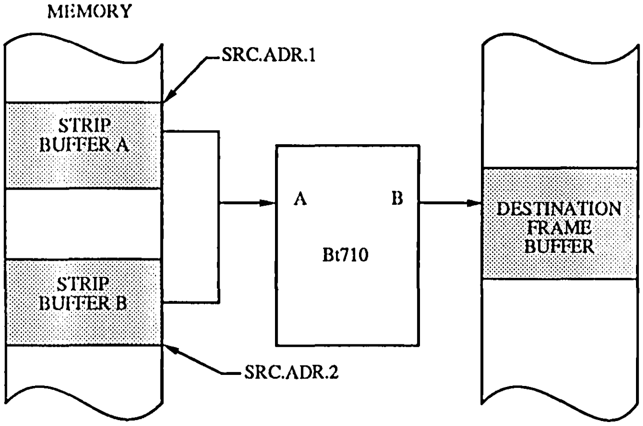


Figure 27. Bt710 with Strip Buffers.

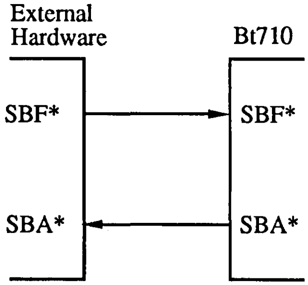


Figure 28. Strip Handshake with the External Hardware.

Application Information (continued)

The Source Buffer Full (SBF*) output of the external hardware indicates to the Bt710 that the current source buffer has been filled and is available for processing. The Source Buffer Available (SBA*) output from the Bt710 tells the external hardware that the next buffer is empty and should be filled. These two pins are level sensitive and have the relationship shown in Figure 29.

Pixel Format

The Bt710 supports 1-bit monochrome, and 4-bit and 8-bit gray scale output pixels. Two formats are used to store these pixels: packed pixels and plane pixels. Either mode is selectable via the PIXEL_MODE bit of the CONTROL register. Note that packed and plane formats are the same for monochrome output.

Packed Pixels

A packed pixel is one in which each bit of the pixel is contained in the same memory word. If 4 bits per pixel are output from the Bt710, then 4 pixels are contained in each 16-bit word. If 8 bits per pixel are output from the Bt710, then 2 pixels are contained in each 16-bit word. This is illustrated in Figure 30.

The order in which pixels are packed into words can be controlled via the DST_ORD bits of the DST.CNTL register and the on-chip look-up table.

Plane Pixels

Plane pixels separate each significant bit of the pixel into a separate bitmap. Frame buffers are often organized this way to allow incremental increases in the pixel depth via additional plane memory.

Figure 31 illustrates a 4-bit plane pixel. The Bt710 buffers 16 pixels internally, prior to beginning DMA writes to the frame buffer. When DMA writes occur, four 16-bit words are written to the frame buffer, one to each bit plane.

The DST.ADR.1 register points to the first bit plane. The Bt710 uses the PLANE.PITCH register to calculate the offset to the subsequent bit planes.

When 8 bit pixels are output, the operation is similar to that shown in Figure 31, with the exception that eight words are written to eight pixel planes.

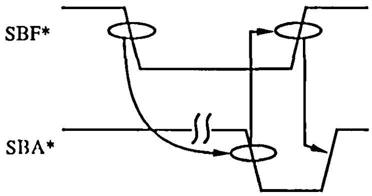


Figure 29. SBF/SBA* Handshake.*

Application Information (continued)

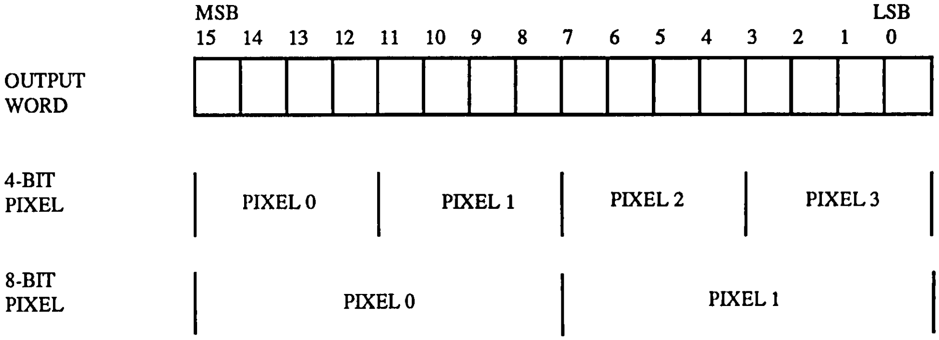

MSB
LSB
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
OUTPUT WORD
4-BIT PIXEL
PIXEL 0
PIXEL 1
PIXEL 2
PIXEL 3
8-BIT PIXEL
PIXEL 0
PIXEL 1

Figure 30. Packed Pixels.

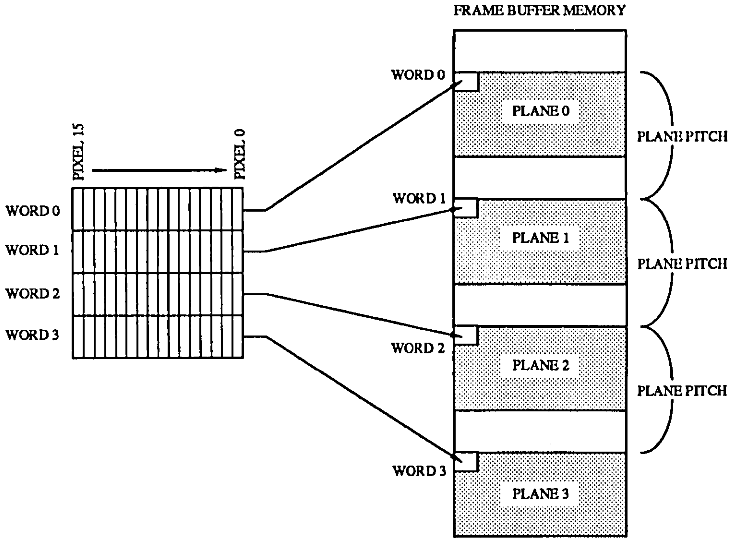

FRAME BUFFER MEMORY
PIXEL 15
PIXEL 0
WORD 0
WORD 1
WORD 2
WORD 3
WORD 0
WORD 1
WORD 2
WORD 3
PLANE 0
PLANE 1
PLANE 2
PLANE 3
PLANE PITCH
PLANE PITCH
PLANE PITCH

Figure 31. Plane Pixels.

Application Information (continued)

Gray Scale Control

The resultant output from the on-chip scaler is 4 bits of gray. This output is achieved through several steps.

The scaler engine actually creates a 10-bit gray scale result, which is converted through a bit selection process to 5 bits of gray. The 5 bits from the 10-bit word is user-selectable via the SELECT bits in the GRAY.ADJ register. When the SELECT bits are set to b'000', the most significant 5 bits of the 10-bit word are extracted (see Figure 32).

When the SELECT bits are set to something other than b'000', they define a left offset into the 10-bit superpixel from which to extract the 5 bits. Three 'phantom' bits exit beyond the LSB of the 10-bit superpixel so that if the SELECT bits are set to b'110' or greater, the least-significant bits of the 5-bit extracted value which overlap the phantom bits are set to zero (see Figure 32).

The 5-bit result obtained (as described above) is then multiplied by the GAIN4–GAIN0 bits in the GRAY.ADJ register. This 5 x 5 multiply results in a 10-bit product. The upper 4 bits of this product are the final output of the scaler. This is shown in Figure 33.

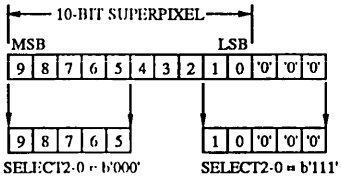

10-BIT SUPERPIXEL
MSB
LSB
9 8 7 6 5 4 3 2 1 0 '0' '0' '0'
9 8 7 6 5
1 0 '0' '0' '0'
SELECT2-0 = b'000'
SELECT2-0 = b'111'

Figure 32. SELECT Parameter.

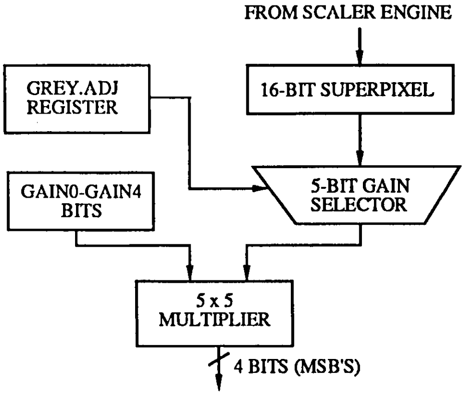

FROM SCALER ENGINE
GREY.ADJ REGISTER
16-BIT SUPERPIXEL
GAIN0-GAIN4 BITS
5-BIT GAIN SELECTOR
5 x 5 MULTIPLIER
4 BITS (MSB'S)

Figure 33. Gray Scale Generation.

Application Information (continued)

Table 5 provides a list of recommended values for the SELECT bits and the GAIN bits of the GRAY.ADJ register for the range of possible values for MVAL, the denominator portion of the scale factor.

Calculating Workspace Line Length

The WORK.LINE.LEN register must be loaded with the width of the workspace line length before Bt710 operation begins. This parameter must be specified properly or unpredictable operation may occur.

Through simulation tests, the following formula was determined to produce a correct calculation for the WORK.LINE.LEN parameter:

$$wll = \frac{((sll \cdot 16 - slm) \cdot n \cdot bpp) + (m \cdot 16 - 1))}{m \cdot 16}$$

where:

wll = workspace line length in words
sll = source line length in words (SRC.LINE.LEN)
slm = source left margin (SRC.LM)
n = scale factor numerator (NVAL)
m = scale factor denominator (MVAL)
bpp = 1 for monochrome output, 4 otherwise

Calculating Workspace Buffer Size

The workspace buffer stores 32 lines of the image. Thus, the workspace buffer size is determined by the WORK.LINE.LEN multiplied by 32.

Performance

Figure 34 provides a table of scaling times for various scale factors.

The performance depicted is based upon preliminary models of the scaling engine. Future performance reports will include actual benchmarked values.

The performance of the Bt710 will depend upon:

1. Scale factor
2. Number of parses required
3. Memory speed
4. Refresh rate
5. Bus accessibility

MVAL Register Value	SELECT Value	GAIN Value
2	7	31
3	6	28
4	5	31
5	5	20
6	4	28
7	4	21
8	3	31
9	3	25
10	3	20
11	3	17
12	2	28
13	2	24
14	2	21
15	2	18
16	1	31
17	1	28
18	1	25
19	1	23
20	1	20
21	1	18
22	1	17
23	1	31
24	0	28
25	0	26
26	0	24
27	0	23
28	0	21
29	0	19
30	0	18
31	0	17

Table 5. SELECT and GAIN Bit Selection.

Application Information (continued)

Input Size	Output Size	Scale Factor	Scale Time (Seconds) Bi-level	4-bit	8-bit
2550 x 3300	1024 x 768	7/30	.237	.237	.237
5100 x 6600	1640 x 1280	4/20	.756	.756	.756
10200 x 13200	1640 x 1280	2/19	2.1	2.1	2.1
2250 x 3300	640 x 480	4/27	.197	.197	.197
3300 x 5100	1024 x 768	6/30	.317	.317	.317
B	A	16/24	.594	.594	.750
C	B	16/24	1.346	1.346	1.683
D	B	8/16	1.346	1.346	1.683
A	C	14/7	2.690	2.690	3.366
A	A	31/31	.594	.594	.750

Figure 34. Scaling Performance.

Bt710EVK Evaluation Kit

The Bt710EVK is a kit for evaluation of the Bt710 that contains the Bt710EVM evaluation board, a set of evaluation software and complete chip and board documentation.

The Bt710EVM is an add-in board for the PC AT which contains the Bt710. The board provides a bus master interface to the PC bus, allowing the Bt710 to access system RAM through their direct memory access (DMA) capabilities.

On-board are sockets for up to eight megabytes of memory, mapped as extended system memory (at or above the 1M address boundary).

The Bt710EVK allows both hardware and software designers to evaluate the Bt710's capabilities without the need for breadboarding.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance.

Latchup can be prevented by assuring that all VCC pins are at the same potential, and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter		Symbol	Min	Nom	Max	Units
Supply Voltage		VDD	4.75	5	5.25	V
Supply Voltage		VSS		0		V
High-level Output Current		IOH			–400	µA
Low-level Output Current	ARAS*, ACAS*, ADS*, AR/W*, ARDY*, AREQ*<1:0> BRAS*, BCAS*, BDS*, BR/W*, BREQ*<1:0>	IOL			1.7	mA
	AA<9:0>, BA<9:0>				3	
	All other outputs				2	
High-level Input Voltage		VIH	2		VCC+.3	V
Low-level Input Voltage		VIL	–0.3		0.8	V
Load Capacitance	ARDY*, AREQ*<1:0> BREQ*<1:0> SBA*, DBF*, INT*, AXAL*, BXAL*	CL			30	pF
	ADS*, AR/W*, AOWN, BDS*, BR/W*, BOWN,				35	
	ARAS*, ACAS*, BRAS*, BCAS* AD<15:0>,BD<15:0>				50	
	AA<9:0>, BA<9:0>				65	
Operating Free-air Temperature		TA	0		70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage				7	V
Input Voltage Range*		VSS–0.3		VCC+.5	V
Output Voltage Range		–2		7	V
Operating Free-air Temperature Range	TA	0		70	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High-level output voltage	VOH	VDD=MIN, IOH=MAX	2.4			V
Low-level output voltage	VOL	VDD=MIN, IOL=MAX			0.4	V
Input leakage current, high	IIH	VDD=MAX, VIH=MIN			1	µA
Input Leakage current, low	IIL	VDD=MAX, VIL=MAX			–1	µA
Off-state output current	IOZ	VO = 0.4 V to 2.4 V			10	µA
Supply current	IDD	VDD=MAX, TA=25°			250	mA
Input capacitance	CI	f=1 MHz, all other inputs at 0 V.			15	pF

NOTE

Throughout these specifications, the first letter (A or B) is removed from the signal name if the identical signal on different Bt710 ports has the same behavior. For example, a column address strobe signal (CAS*) is present on both port A and port B of the Bt710. Since these signals behave identically, only the generic signal name CAS* will be used.

CLOCK Timing Parameters (See Note 1 and Figure 35)

No.	Parameter	Min	Max	Units
1	Cycle Time (tc)	19	21	ns
2	Pulse Width High	6		
3	Pulse Width Low	6		
4	Rise Time		2	
5	Fall Time		2	

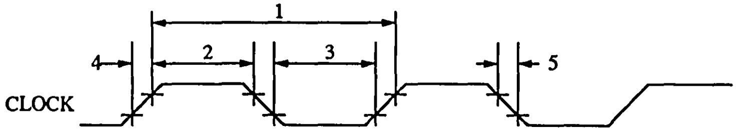


Figure 35. CLOCK Timing.

Bus Arbitration Timing Parameters (See Note 1 and Figures 36–37)

No.	Parameter	Min	Max	Units
6	Delay time, CLOCK to REQ1*/REQ2* high or low		45	ns
7	Delay time, CLOCK to OWN high		45	
8	Delay time, CLOCK to XAL* high		45	
9	Delay time, CLOCK to RAS* high		45	
10	Delay time, CLOCK to CAS* high		45	
11	Delay time, CLOCK to R/W*, DS* high		45	
12	Delay time, GNT* low to OWN high	4tc		
13	Delay time, CLOCK to address no longer hi-z.	5	45	
14	Delay time, GNT* low to XAL* high, first memory cycle (note 4)	8tc		
15	Hold time, REQ1*, REQ0* low after OWN high	0		
16	Hold time, GNT* low after OWN high (note 3)	0		
17	Delay time, GNT* high to OWN low, bus release (note 5)		30tc + 3w	
18	Delay time, CLOCK to OWN low, bus release		45	
19	Delay time, CLOCK to address, data, and control hi-z, bus release		45	
20	Delay time, OWN high to address no longer hi-z	tc		
21	Delay time, OWN high to XAL*, RAS*, CAS*, R/W*, DS* driven high or low	tc		

Notes:
1. All timing references are to the 0.8 V and 2 V levels.
2. If the GNT* input is taken high prior to state T1 of any cycle, the bus will be released at the end of that cycle; otherwise the bus release occurs at the end of the next bus cycle unless a refresh operation is pending. If a refresh is pending, the Bt710 will hold the bus until refresh is complete. If the Bt710 enters wait states after or when GNT* is taken high, OWN will remain high indefinitely as long as the Bt710 is in wait states.
3. Once GNT* is asserted to the Bt710, GNT* must remain low until parameter 16 is met.
4. After XAL is driven high, the bus timing is as shown for read, write, or refresh cycles unless this is the first bus request after enabling DRAM refresh for the first time. In this case, the first bus cycles following OWN going high will be eight CAS before RAS refresh cycles for DRAM initialization.
5. w = Number of wait states.

Bus Arbitration Timing Parameters (continued)

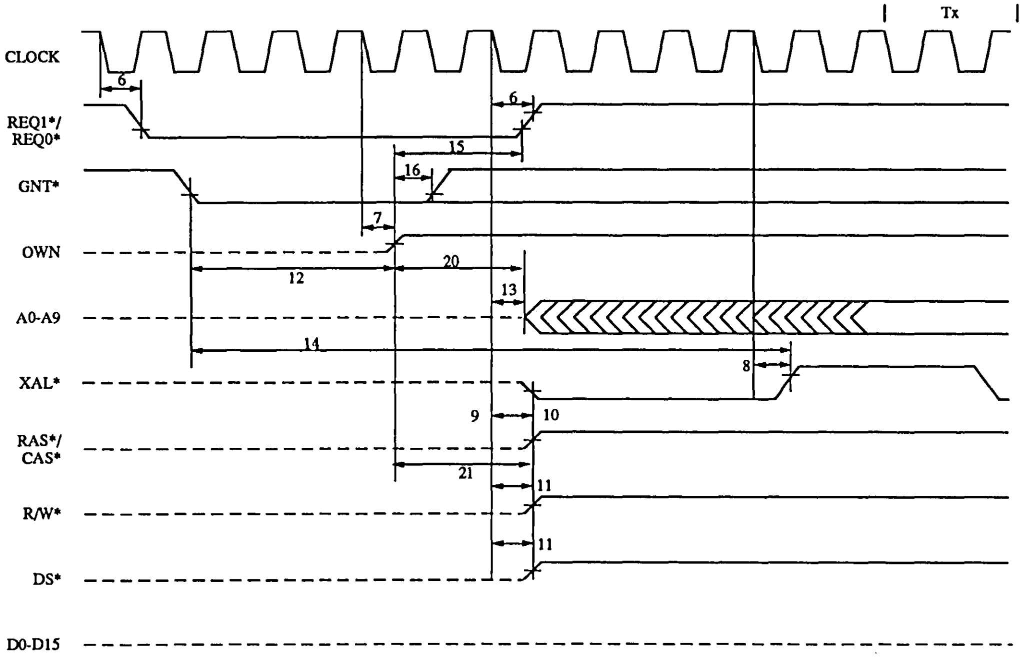

Tx
CLOCK
REQ1*/
REQ0*
GNT*
OWN
A0-A9
XAL*
RAS*/
CAS*
R/W*
DS*
D0-D15
6
6
15
16
7
20
12
13
14
8
9
10
21
11
11

Figure 36. Bt710 Acquires Bus.

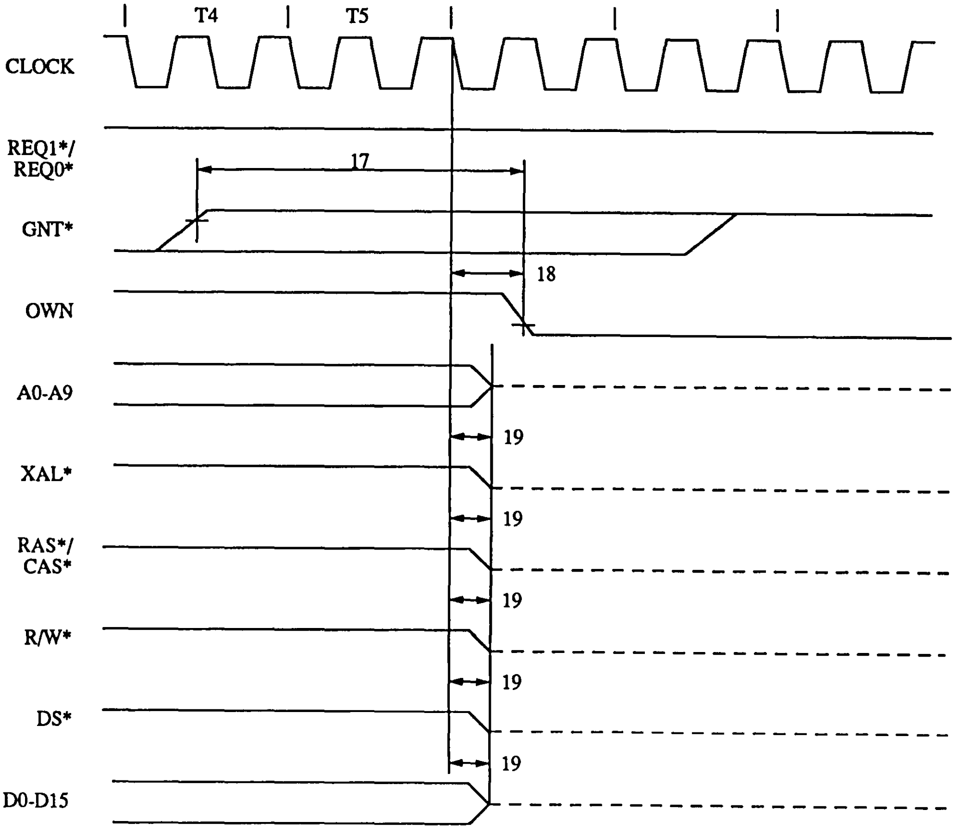

T4
T5
CLOCK
REQ1*/
REQ0*
GNT*
OWN
A0-A9
XAL*
RAS*/
CAS*
R/W*
DS*
D0-D15
17
18
19
19
19
19
19

Figure 37. Bt710 Releases Bus.

Read/Write Cycle Timing Parameters (See Note 1 and Figures 38–41)

No.	Parameter	Min	Max	Units
22	Delay time, CLOCK to XAL*, DS*, R/W* low or high		43	ns
23	Delay time, CLOCK to RAS* low		47	
24	Delay time, CLOCK to RAS* high		33	
25	Delay time, CLOCK to address valid, DS*, XAL* high or low		34	
26	Delay time, CLOCK to CAS* low		31	
27	Delay time, CLOCK to CAS* high		31	

Read/Write CycleTiming Parameters (continued)

No	Parameter	Min	Max	Unit
28	Delay time, row address valid to RAS* low	tc + 2		ns
29	Delay time, RAS* low to row address no longer valid	3tc – 10		
30	Delay time, RAS* low to CAS* low	4tc – 16		
31	Delay time, RAS* low to DS* low	2tc – 10		
32	Delay time, column address valid to CAS* low	tc – 3		
33	Delay time, CAS* low to column address no longer valid	5tc + 3		
34	Pulse width, RAS* low (note 2, 4)	6tc – 10		
35	Pulse width, CAS* low (note 2, 3)	4tc		
36	Pulse width, RAS* high (note 2, 5)	4tc + 2		
37	Delay time, extended address valid to XAL* low	tc – 2		
38	Delay time, XAL* low to extended address no longer valid	tc		
39	Access time, RAS* low to read data valid (note 2, 3)			
40	Pulse width, DS* low (note 2, 3)	6tc – 4		
41	Delay time, RAS* low to RDY* low to guarantee zero wait states	–5		
42	Delay time, RDY* low to DS* high with zero wait states	8tc – 9		
43	Pulse width low, RDY*	2tc		
44	Setup time, read data valid prior to CAS* no longer low	30		
45	Hold time, read data after CAS* high	0		
46	Delay time, R/W* high to CAS* low, read cycle	4tc – 12		
47	Read/Write cycle time (note 2)	10tc		
48	Access time, CAS* low to read data valid (note 2, 3)			
49	Delay time, CAS* high to RAS* no longer high	2tc + 3		

Read/Write CycleTiming Parameters (continued)

No	Parameter	Min	Max	Unit
50	Delay time, CAS* high to R/W* no longer high	2tc		ns
51	Delay time, column address valid to RAS* no longer low	3tc + 1		
52	Delay time, DS* low to CAS* low	2tc – 12		
53	Delay time, RAS* low to D0–D15 no longer hi-z	2tc – 6		
54	Delay time, CLOCK high to write data valid	9	40	
55	Delay time, DS* low to write data valid		5	
56	Delay time, write data valid to CAS* low	2tc – 11		
57	Delay time, DS* high to write data no longer valid	2tc + 1		
58	Delay time, R/W* high to D0–D15 hi-z		0	
59	Delay time, CAS* high to R/W* no longer low	2tc + 1		
60	Hold time, RDY* high after RAS* low to add one or more wait states	2tc		
61	Delay time, RDY* low to DS* high, one or more wait states	8tc		
62	Setup time, RDY* high prior to RAS* low for one or more wait states	tc + 1		

Notes:
1. All timing references are to 0.8 V and 2 V.
2. When one or more wait states are inserted, state T4w is automatically inserted. Only one T4w state is inserted irrespective of the number of wait states.
3. When wait states are inserted, 2n+2 additional tc cycles are added to this time where n is equal to the number of wait states. Minimum times are for zero wait states.
4. Times given are for zero wait states. When one or more wait states are inserted, the maximum and minimum times are extended by 2n tc cycles where n is equal to the number of wait states inserted.
5. The minimum time is when state T1 of the next cycle occurs following T5 of the current cycle. If a Tx cycle occurs, this parameter is increased by one tc period.

Read/Write CycleTiming Parameters (continued)

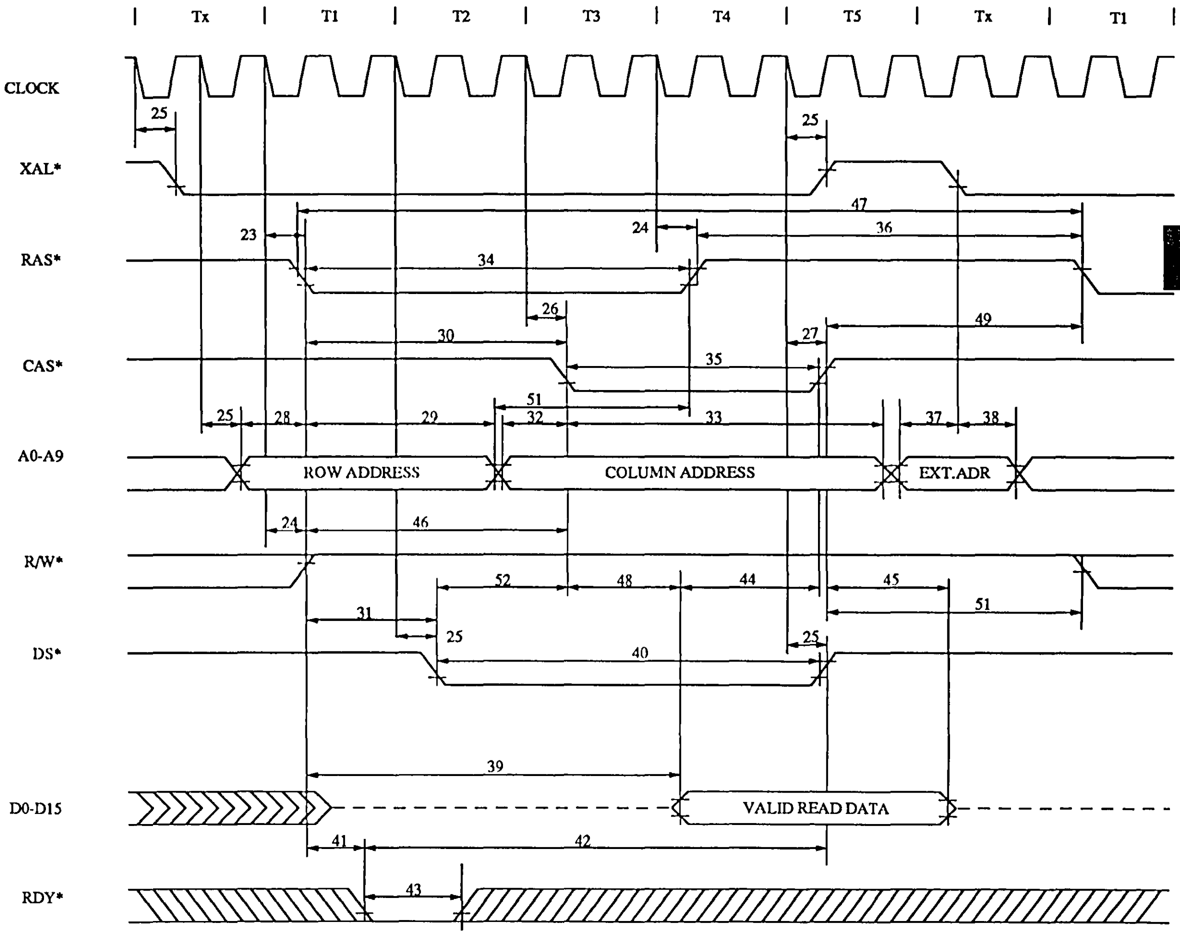

Tx
T1
T2
T3
T4
T5
Tx
T1
CLOCK
XAL*
RAS*
CAS*
A0-A9
R/W*
DS*
D0-D15
RDY*
ROW ADDRESS
COLUMN ADDRESS
EXT.ADR
VALID READ DATA
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
51
52

Figure 38. Read Cycle Timing—0 Wait States.

Read/Write CycleTiming Parameters (continued)

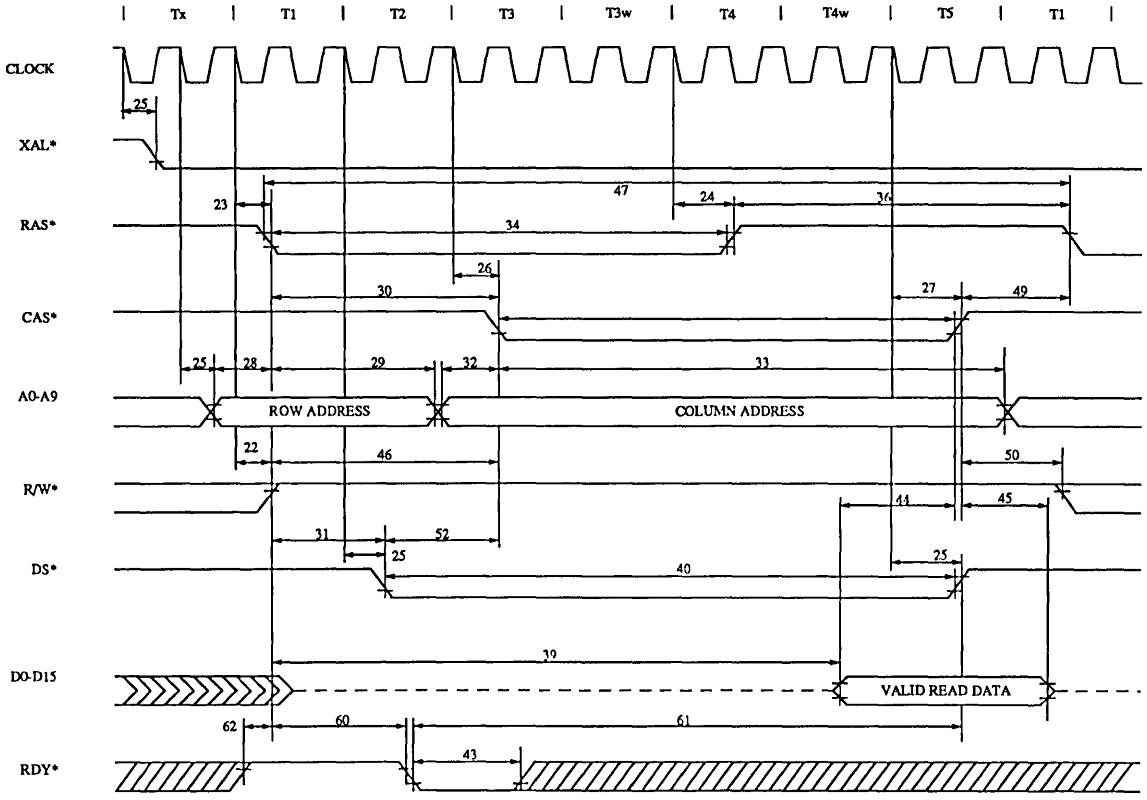

Tx
T1
T2
T3
T3w
T4
T4w
T5
T1
CLOCK
XAL*
RAS*
CAS*
A0-A9
R/W*
DS*
D0-D15
RDY*
25
47
23
24
36
34
26
30
27
49
25
28
29
32
33
ROW ADDRESS
COLUMN ADDRESS
22
46
50
44
45
31
52
25
25
40
39
VALID READ DATA
62
60
61
43

Figure 39. Read Cycle Timing with Wait States.

Read/Write CycleTiming Parameters (continued)

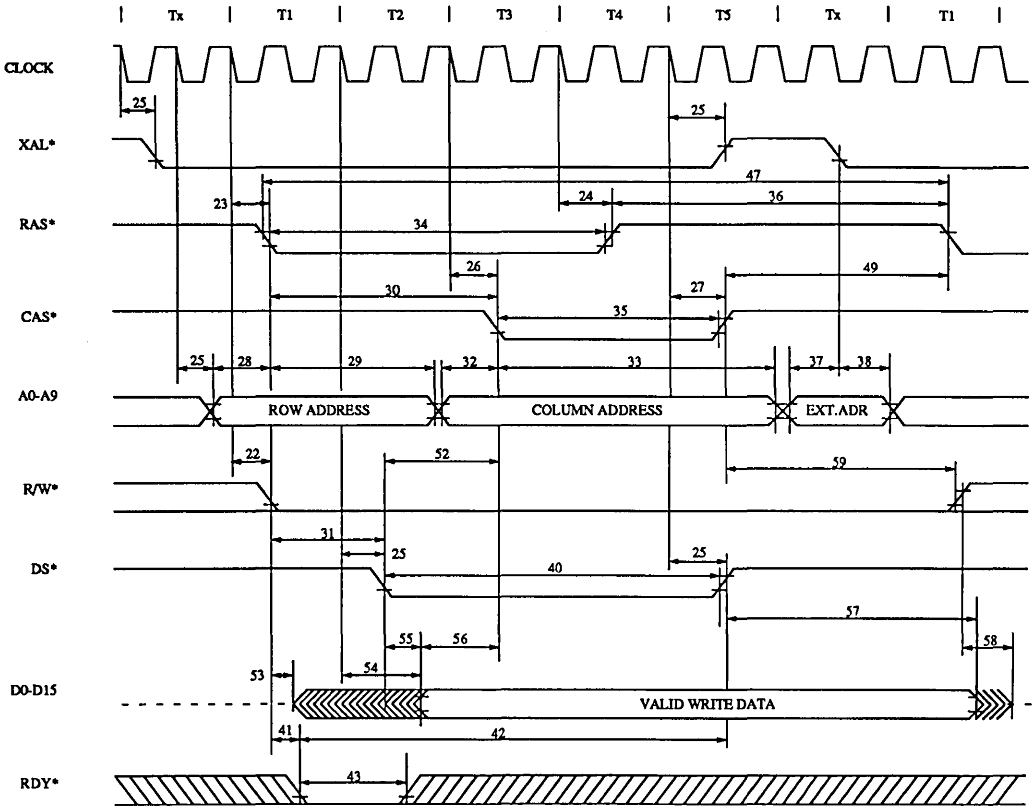

Tx
T1
T2
T3
T4
T5
Tx
T1
CLOCK
XAL*
RAS*
CAS*
A0-A9
R/W*
DS*
D0-D15
RDY*
ROW ADDRESS
COLUMN ADDRESS
EXT.ADR
VALID WRITE DATA
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
40
41
42
43
47
49
52
53
54
55
56
57
58
59

Figure 40. Write Cycle Timing—0 Wait States.

Read/Write CycleTiming Parameters (continued)

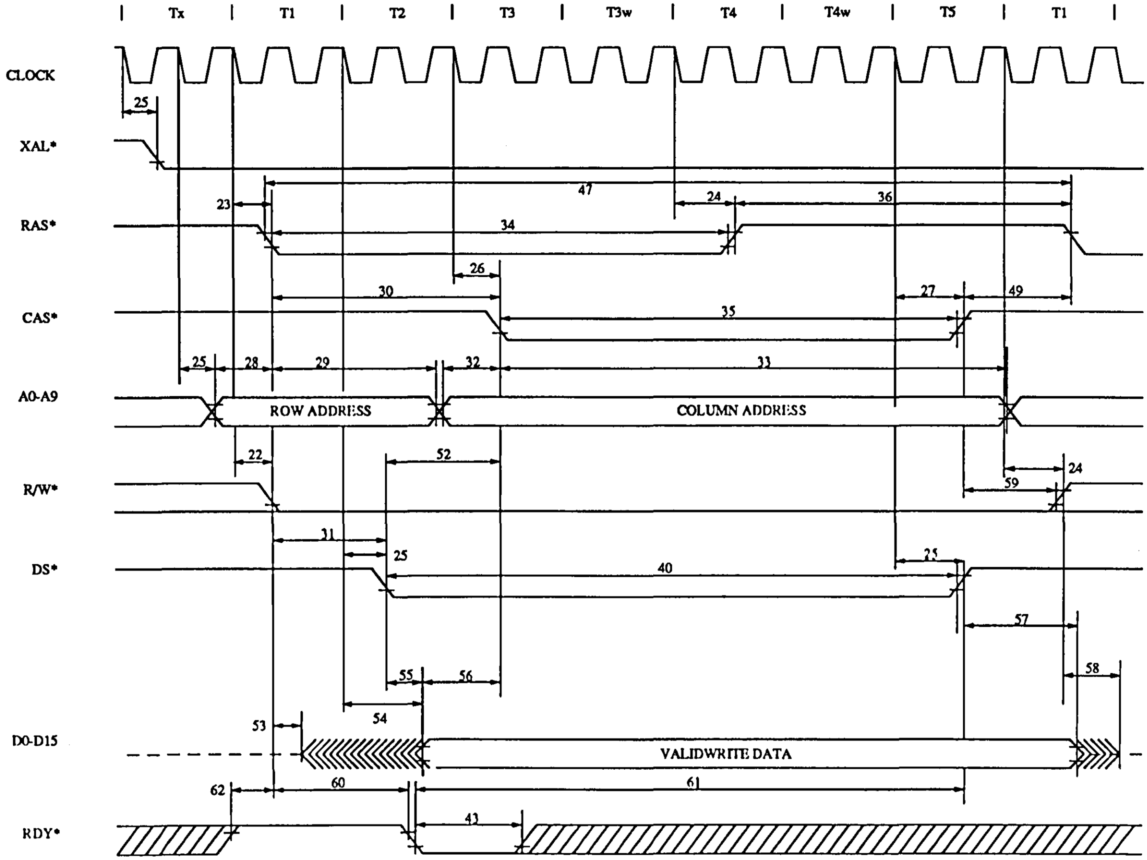

Tx
T1
T2
T3
T3w
T4
T4w
T5
T1
CLOCK
XAL*
RAS*
CAS*
A0-A9
R/W*
DS*
D0-D15
RDY*
ROW ADDRESS
COLUMN ADDRESS
VALIDWRITE DATA
25
47
23
24
36
34
26
30
27
49
35
25
28
29
32
33
22
52
24
59
31
25
25
40
57
55
56
58
54
53
62
60
61
43

Figure 41. Write Cycle Timing with Wait States.

DRAM Refresh Timing Parameters (See Note 1 and Figures 42–43)

No	Parameter	Min	Max	Unit
63	Delay time, CAS* low to RAS* low	2tc + 17		ns
64	Pulse width , RAS* low (note 3)	6tc – 10		
65	Pulse width, CAS* low (note 3)	8tc		
66	Pulse width, RAS* high (note 2)	4tc + 2		
67	Delay time, CAS* low to RDY* low to guarantee zero wait states	–5		
68	Delay time, RDY* low to CAS* high, zero wait states			
69	Hold time, RDY* high after CAS* low to guarantee one or more wait states	2tc		
70	Delay time, RDY* low to CAS* high, one or more wait states	8tc		

Notes:
1. All timing refererences are to the 0.8 V and 2 V levels.
2. When one or more wait states are inserted, state T5w is automatically inserted. Only one T5w state is inserted irrespective of the number of wait states.
3. When wait states are inserted, n+1 additional tc cycles are added to this time where n is equal to the number of wait states.
4. Times given are for zero wait states. When one or more wait states are inserted, the maximum and minimum times are extended by n tc cycles where n is equal to the number of wait states inserted.

DRAM Refresh Timing Parameters (continued)

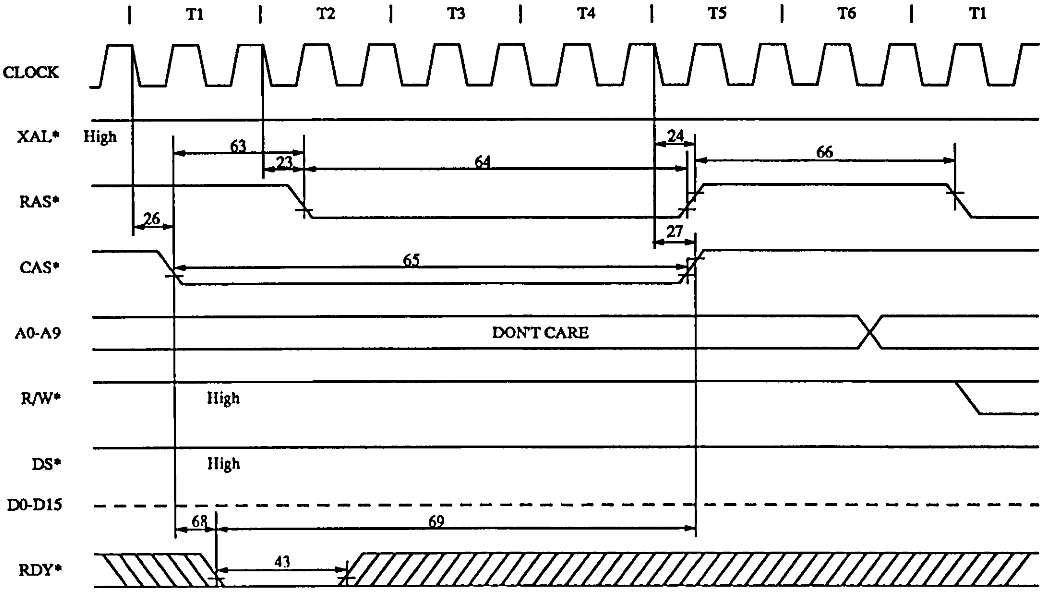

T1
T2
T3
T4
T5
T6
T1
CLOCK
XAL*
High
RAS*
CAS*
A0-A9
DON'T CARE
R/W*
High
DS*
High
D0-D15
RDY*
63
23
64
24
66
26
27
65
68
69
43

Figure 42. DRAM Refresh Timing—No Wait States.

DRAM Refresh Timing Parameters (continued)

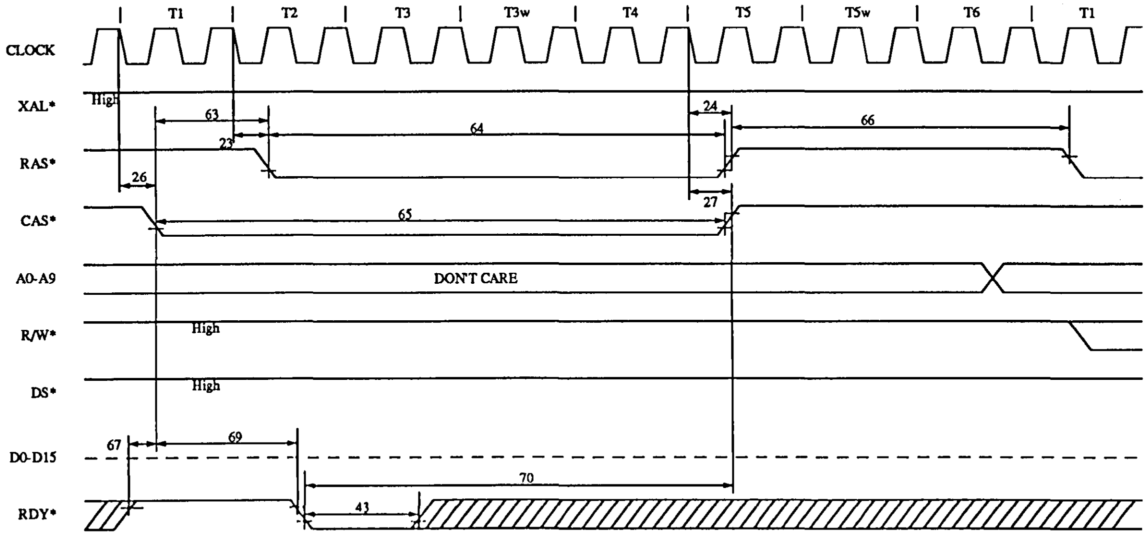

T1
T2
T3
T3w
T4
T5
T5w
T6
T1
CLOCK
XAL*
High
RAS*
CAS*
A0-A9
DON'T CARE
R/W*
High
DS*
High
D0-D15
RDY*
63
64
23
24
66
26
27
65
67
69
70
43

Figure 43. DRAM Refresh Timing—Wait States.

Programmed I/O Timing Parameters (See Note 1 and Figures 44–45)

No.	Parameter	Min	Max	Unit
75	Access time, register address valid to read data valid			ns
76	Access time, ACS* low to read data valid (note 2)		12tc	
77	Access time, ADS* low to to read data valid (note 2)		12tc	
78	Delay time, ACS* low to AOWN low		30tc + 3w	
79	Delay time, ADS* low to ARDY* low	120	183	
80	Hold time, register address valid after ADS* high	2tc		
81	Setup time, AR/W* high prior to ADS* low	2tc		
82	Hold time, AR/W* after ADS* high	0		
83	Pulse width, ADS* high between consecutive cycles	4tc		
84	Delay time, ADS* high to read data no longer valid	4		
85	Delay time, ADS* high to D0–D15 hi-z	4		
86	Delay time, ADS* high to ARDY* high	2tc		
87	Delay time, ADS* low to ARDY* active	100	163	
88	Setup time, register address prior to ADS* low	2tc		
89	Setup time, ACS* low prior to ADS* low	2tc		
90	Hold time, ACS* low after ADS* high	160		
91	Setup time, write data prior to ADS* no longer low	2tc		
92	Hold time, ADS* high after AOWN no longer high			
93	Pulse width, ADS* low, write cycle	4tc		
94	Hold time, write data valid after ADS* high	4		

Notes:
1. All timing references are to the 0.8 V and 2 V levels.
2. Register access begins when ACS*, ADS*, and AOWN are all low. If AOWN is high when ACS* is taken low, register access is delayed until the Bt701 takes AOWN low. The minimum times given are based upon AOWN being low when the ACS* or ADS* are taken low. The maximum times are the worst case delay times for the Bt710 to remove AOWN after sampling ACS* low.
3. OWN must be driven low by the Bt710 prior to driving the programmed I/O input signals.

Programmed I/O Timing Parameters (continued)

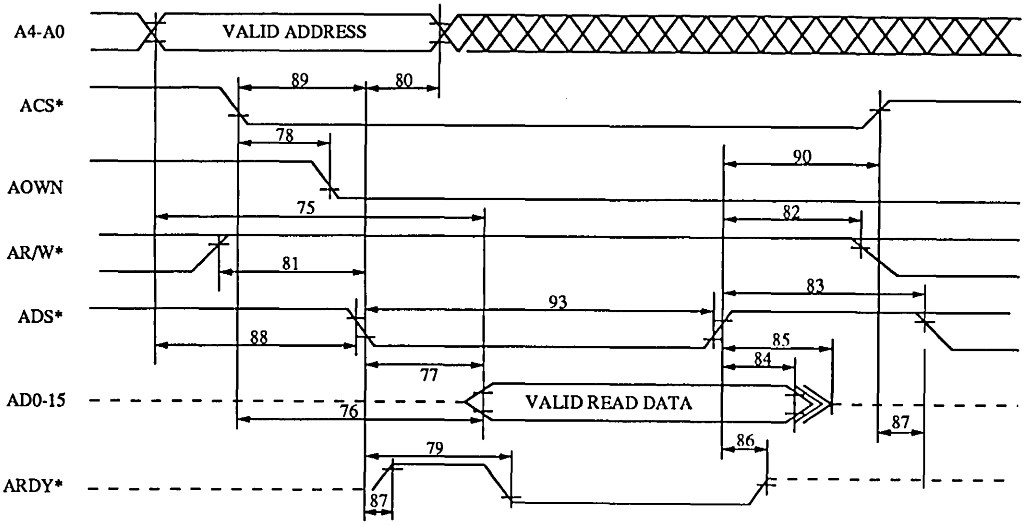

A4-A0
VALID ADDRESS
ACS*
AOWN
AR/W*
ADS*
AD0-15
VALID READ DATA
ARDY*
89
80
78
90
75
82
81
83
93
88
85
84
77
76
87
79
86
87

Figure 44. Programmed I/O Read Cycle.

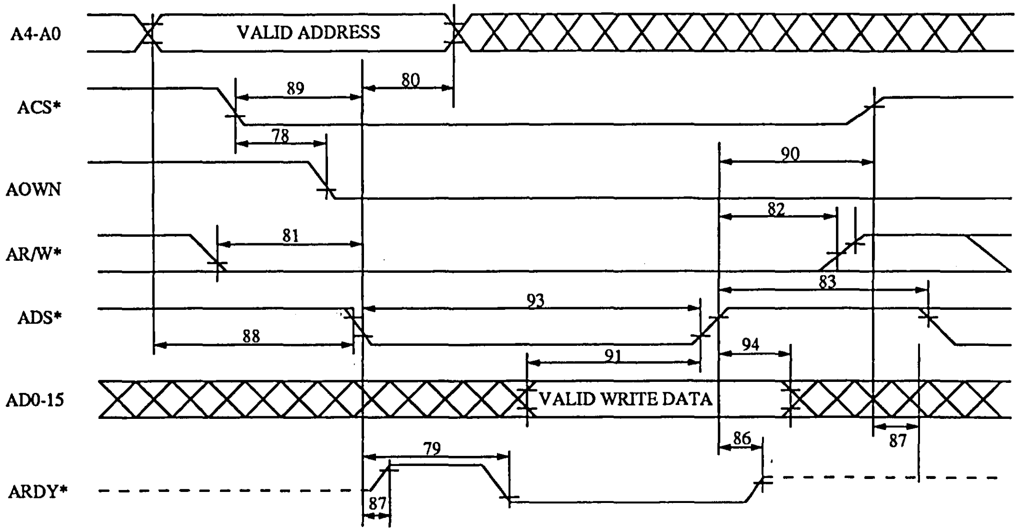

A4-A0
VALID ADDRESS
ACS*
AOWN
AR/W*
ADS*
AD0-15
VALID WRITE DATA
ARDY*
89
80
78
90
82
81
83
93
88
91
94
86
87
79
87

Figure 45. Programmed I/O Write Cycle.

Reset Timing Parameters (See Figure 46)

No.	Parameter	Min	Max	Unit
95	Pulse width, RESET low	8tc		ns

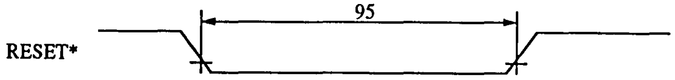


Figure 46. RESET Timing.

SBF/SBA DBA/DBF Timing Parameters (See Figure 47)

No.	Parameter	Min	Max	Unit
96	Pulse width, SBF*, DBA* low	8tc		ns
97	Delay time, SBA*, DBA* low to SBF*, DBF* low	7tc		

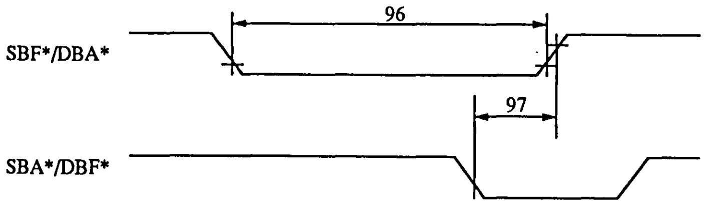


Figure 47. SBF/SBA DBA/DBF Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt710KG	132-pin PGA	0° to +70 °C
Bt700EVK	Evaluation Kit	0° to +70 °C

dvance Information

his document contains information on a product under development. The parametric
formation contains target parameters and is subject to change.

PixelVu™

Object-oriented Software Toolkit for Imaging

istinguishing Features

- C-callable library.
- Concise set of powerful functions.
- Multiple platform support: PC-AT, Macintosh and SUN.
- Multiple windowing environments: MS-Windows, Color QuickDraw, and X.
- Multiple operating systems: MS-DOS with third-party DOS extenders, Macintosh and UNIX.
- Object-oriented processing for maximum power and flexibility.
- Open Architecture: Support of application-specific image objects.
- Scale-to-gray algorithm for enhanced visual quality.
- Transparent hardware acceleration.

Product Description

PixelVu is a toolkit specifically designed for OEMs and systems integrators of imaging systems. PixelVu consists of a concise set of C-callable functions. Because of the small number of functions, the programmer can easily become familiar with this powerful library. Compressed images can be read, decompressed, scaled, rotated and BitBLTed directly into the frame buffer or print buffer. PixelVu contains all the image manipulation functions required to process bi-level images on a disk or in memory and output the result to memory or a display device.

The PixelVu toolkit was designed with portability as a key requirement. The same library is available for 286 and 386-based PCs, 68020- and 68030- based Macintosh computers, and SUN platforms. In addition, PixelVu supports multiple operating environments, including MS-DOS, MS-Windows, Color QuickDraw, and X.

PixelVu supports devices and system resources through programming structures called image objects (Figure 1). Brooktree's object-oriented software toolkit permits developers to reference an image object and select an operation to be performed on that image without having to know any details about how to read data from or write data to the object. In this way, software development is simplified because device-specific data need not be studied by the application developer.

OEMs and third party developers can create their own objects and interface them within the PixelVu environment. In this way, custom file formats or third party devices can be added to PixelVu's image management and image manipulation capabilities.

PixelVu provides scale-to-gray capabilities. Scaling a bi-level image to gray-scale display image provides anti-aliasing effects. This provides a much more readable image at resolutions less than that normally needed for readability.

PixelVu performance can be increased by adding image manipulation hardware into the system. Hardware acceleration can be transparent to the application. If supported hardware is present in the system it will be used to optimize function execution. If no hardware is present, image manipulation is executed in software. In this way, PixelVu provides a low-cost solution for moderate use environments and a high-performance solution for performance-critical applications. The Brooktree Bt710 scale-to-gray integrated circuit can be used to efficiently provide hardware scale-to-gray capability.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L700001 Rev. A

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Raster Image Manipulation

PixelVu includes the following raster image manipulation primitives:

- *Compression and Decompression.* CCITT Group 3 and Group 4 compression and decompression are provided to support existing standards.

- *Image Scaling.* A bitmap may be scaled down in increments of 1% to as small as 6% of its initial size. A bitmap may be scaled up to as much as 750% of its initial size.

- *Image Rotation.* Rotation of +/- 90 and 180 degrees is supported. Rotation facilitates conversion between landscape and portrait modes.

- *Cropping.* The input or output bitmap may be cropped to any pixel boundary, permitting any window area to be selected.

- *Reflection.* To provide correcting capabilities for reverse scanning of microfilm, bitmaps may also be reflected.

- *Conversion to Gray.* A binary bitmap may be converted to gray when scaling to provide improved display quality on gray scale or color monitors. This prevents loss of information inherent in decimation scaling algorithms.

- *BitBLT.* Bitwise Block Transfers are performed by PixelVu. Data can be copied into a destination area on pixel boundaries. Boolean operations can also be performed on images.

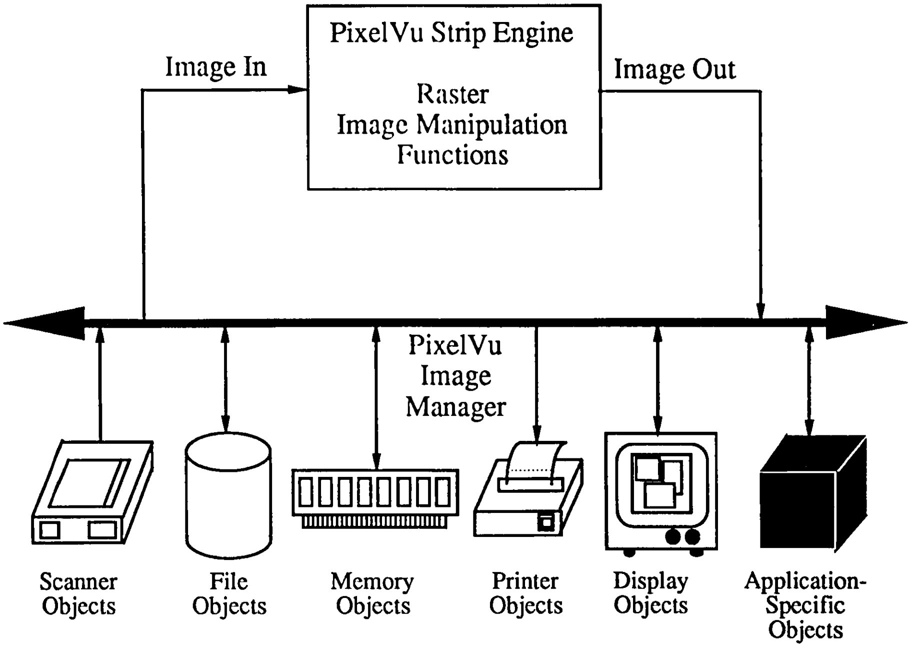
PixelVu Strip Engine
Raster Image Manipulation Functions
Image In
Image Out
PixelVu Image Manager
Scanner Objects
File Objects
Memory Objects
Printer Objects
Display Objects
Application-Specific Objects

Figure 1: PixelVu is an Object-Oriented Toolkit.

PixelVu Functions

There are four types of functions in the PixelVu library: Initialization and Termination Functions, Image Object Functions, Image Manipulation Functions and Support Utility Functions.

Initialization and Termination Functions

Initialization and termination functions provide the means to begin a session of PixelVu, terminate it and obtain error and status information.

Bt_Init	Initialize the PixelVu Software Toolkit.
Bt_Quit	Terminate PixelVu.
Bt_GetError	Obtain the last PixelVu error status.
Bt_Version	Obtain this PixelVu Version Number.
Bt_ErrorStr	Return a text error message.

Image Object Functions

Image Object Functions are used to open, create or dispose of image objects. The image objects supported include: file objects: TIFF (Tagged Image File Format) and Sun Raster file formats; memory objects; and window objects: Macintosh Color QuickDraw, Microsoft Windows 3.0 and X11.3.

Bt_OpenImageTiff	Open an existing TIFF file..
Bt_CreateImageTiff	Create a new TIFF file.
Bt_OpenImageSunR	Open an existing Sun Raster file.
Bt_CreateImageSunR	Create a new Sun Raster file.
Bt_CreateImageMem	Create a new memory Image Object.
Bt_OpenImageMem	Create a new memory Image Object from a user supplied memory pointer.
Bt_OpenImageWindow	Open a Macintosh Window.
Bt_OpenImageWindow	Open a Microsoft Windows 3.0 Window.
Bt_OpenImageXWindow	Open an X.11 Window.
Bt_FreeImage	Free up all memory resources previously allocated to an Object.

Image Manipulation Functions

All image manipulation functions in PixelVu are selected using a Parameter Block. Fields in a parameter block select different processing functions to take place. Bt_Transfer performs the selected image manipulation functions.

Bt_GetParamBlock	Create a new Parameter Block.
Bt_DisposeParamBlock	Deallocate all memory previously allocated to a parameter block.
Bt_Setup	Verify the validity of the fields in a parameter block.
Bt_Transfer	Perform image manipulation based upon the fields of the parameter block.
Bt_UpdateTransfer	Perform image manipulation based upon the fields of the parameter block but only affect a subset of the destination area.

Utility Functions

Utility functions are provided to facilitate the calculation of source and destination rectangles.

Bt_CalcDestRect	Calculate a destination rectangle based upon a given source rectangle and scale factor.
Bt_CalcSourceRect	Calculate a source rectangle based upon a given destination rectangle and scale factor.
Bt_CalcSourceClip	Adjust a source rectangle to conform to a destination clipping area, rotation, reflection and scale factor.

A detailed description of PixelVu functions and operations may be found in the PixelVu Programmers Reference Manual.

Ordering Information

Platforms:	PC-AT	SUN-3 SUN-4 SPARCstation	Macintosh II*
Operating System	MS-DOS V3.1*	UNIX	System 6.0.3*
Windowing Environments	Microsoft Windows 3.0 X11.3 Server	X11.3 Open Windows	Macintosh Windowing Environment X11.3 Server
Compilers Supported	Microsoft C V5.1 Turbo C V2.0 Watcom C Opt. Compiler/386 V7.0** High C-386**	SUN C	THINK's LightSpeedC
Extended Memory Support	Eclipse OS/286 DOS Extender** Eclipse OS/386 DOS Extender** Phar Lap 386IASM/Link and Phar Lap 386IVMM DOS Extenders**		Under System 7
Part Number	Bt700SDA	Bt700SSA	Bt700SMA

* Indicates a level of support and higher.
** Not running under Microsoft Windows.

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UNIX is a registered trademark of AT&T.
X Window System is a registered trademark of Massachusetts Institute of Technology.
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SECTION 4

RAMDACs

Contents

Bt450 80, 66, 50, 35 MHz Triple 4-bit RAMDAC with 16 x 12 RAM 4 - 7

Bt453 66, 40 MHz Triple 8-bit RAMDAC with 256 x 24 RAM 4 - 57

Bt453/883 40 MHz MIL-STD-883 Version of Bt453 4 - 75

Bt454 170, 135, 110 MHz Triple 4-bit RAMDAC with 16 x 12 RAM, 4:1 Multiplexed Pixel Inputs 4 - 91

Bt455 170, 135, 110 MHz single 4-bit RAMDAC with 16 x 4 RAM, 4:1 Multiplexed Pixel Inuts 4 - 91

Bt461 170, 135, 110, 80 MHz Single 8-bit RAMDAC with 1024 x 8 RAM, 256 x 8 Alternate RAM, 3:1, 4:1, or 5:1 Multiplexed Pixel Inputs 4 - 241

Bt462 170, 135, 110, 80 MHz Single 8-bit RAMDAC with 1024 x 8 RAM, 256 x 8 Alternate RAM, 3:1, 4:1, or 5:1 Multiplexed Pixel Inputs 4 - 241

Bt474 85, 66 MHz Triple 8-bit RAMDAC with 256 x 24 RAM, 4:1 Multiplexed Pixel Inputs 4 - 421

Bt492 360 MHz Single 8-bit RAMDAC with 256 x 8 RAM 4 - 515

Bt458 Family

Bt451 125, 110, 80 MHz Triple 4-bit RAMDAC with 256 x 12 RAM, 4:1 or 5:1 Multiplexed Pixel Inputs 4 - 23

Bt457 125, 110, 80 MHz Single 8-bit RAMDAC with 256 x 8 RAM, 4:1 or 5:1 Multiplexed Pixel Inputs 4 - 23

Bt458 165, 125, 110, 80 MHz Triple 8-bit RAMDAC with 256 x 24 RAM, 4:1 or 5:1 Multiplexed Pixel Inputs 4 - 23

Bt458/883 110 MHz MIL-STD-883 Version of Bt458 4 - 111

Bt459 Family

Bt459 135, 110, 80 MHz Triple 8-bit RAMDAC with 256 x 24 RAM, 1:1, 4:1, or 5:1 Multiplexed Pixel Inputs, 64 x 64 On-Chip Cursor 4 - 135

Bt460 135, 110, 80 MHz Triple 8-bit RAMDAC with 512 x 24 RAM, 1:1, 4:1, or 5:1 Multiplexed Pixel Inputs, 64 x 64 On-Chip Cursor 4 - 187

Bt468 200, 170 MHz Triple 8-bit RAMDAC with 256 x 24 RAM, 8:1 Multiplexed Pixel Inputs, 64 x 64 On-Chip Cursor 4 - 327

TrueVu Family

Bt463 170, 135, 110 MHz Triple 8-bit True Color Window RAMDAC with (3) 528 x 8 RAM, 1:1, 2:1, 4:1 Multiplexed Inputs 4 - 279

VGA Family

Bt471 80, 66, 50, 35 MHz Triple 6-bit RAMDAC with 256 x 18 RAM 4 - 371

Bt473 80, 66, 50, 35 MHz Triple 8-bit RAMDAC with 256 x 24 RAM, 8:1 Multiplexed Pixel Inputs 4 - 395

Bt475 80, 66, 50, 35 MHz Triple 6-bit Power-Down RAMDAC with 256 x 18 RAM 4 - 455

Bt476 66, 50, 35 MHz Triple 6-bit RAMDAC with 256 x 18 RAM 4 - 371

Bt477 80, 66, 50, 35 MHz Triple 8-bit Power-Down RAMDAC with 256 x 24 RAM 4 - 455

Bt478 80, 66, 50, 35 MHz Triple 8-bit RAMDAC with 256 x 24 RAM 4 - 371

Bt479 80, 66, 50, 35 MHz Triple 8-bit WindowVu RAMDAC with 1024 x 24 RAM 4 - 481

RAMDAC Selection Guide

D/A Organization	Speed (MHz)	Part Number	Page	RAM Size	Overlay Size	
triple 4-bit	80, 66, 50, 30	Bt450	4 - 7	16 x 12	3 x 12	4:1 muxed pixel inputs
triple 4-bit	125, 110, 80	Bt451	4 - 23	256 x 12	4 x 12	Bt458 pin compatible
triple 4-bit	170, 135, 110	Bt454	4 - 91	16 x 12	1 x 12	
triple 6-bit	80, 66, 50, 35	Bt471	4 - 371	256 x 18	15 x 12	Bt478 pin compatible
triple 6-bit	80, 66, 50, 35	Bt475	4 - 455	256 x 18	15 x 12	power-down Bt471
triple 6-bit	66, 50, 35	Bt476	4 - 371	256 x 18	-	Bt478 pin compatible
single 8-bit	170, 135, 110, 80	Bt461	4 - 241	1024 x 8	256 x 8	muxed pixel inputs
single 8-bit	170, 135, 110, 80	Bt462	4 - 241	1024 x 8	256 x 8	underlay capability
single 8-bit	125, 110, 80	Bt457	4 - 23	256 x 8	4 x 8	Bt458 pin compatible
single 8-bit	360	Bt492	4 - 515	256 x 8	16 x 8	2:1 muxed pixel inputs
triple 8-bit	66, 40	Bt453	4 - 57	256 x 24	3 x 24	
triple 8-bit	165, 125, 110, 80	Bt458	4 - 23	256 x 24	4 x 24	4:1, 5:1 muxed pixel inputs
triple 8-bit	135, 110, 80	Bt459	4 - 135	256 x 24	15 x 24	on-chip cursors
triple 8-bit	135, 110, 80	Bt460	4 - 187	512 x 24	15 x 24	on-chip cursors
triple 8-bit	200, 170	Bt468	4 - 327	256 x 24	15 x 24	8:1 muxed pixel inputs
triple 8-bit	85, 66	Bt474	4 - 421	256 x 24	15 x 24	4:1 muxed pixel inputs
triple 8-bit	80, 66, 50	Bt477	4 - 455	256 x 24	15 x 24	power-down feature
triple 8-bit	80, 66, 50, 35	Bt478	4 - 371	256 x 24	15 x 24	PS/2 RAMDAC
triple 8-bit	80, 66, 50, 35	Bt479	4 - 481	1024 x 24	15 x 24	Window RAMDAC
true color	170, 135, 110	Bt463	4 - 279	(3) 528 x 8	(3) 15 x 8	
true color	80, 66, 50, 35	Bt473	4 - 395	(3) 256 x 8	(3) 15 x 8	

RAMDAC Selection Guide *(continued)*

	Display Resolution				
DAC Size	Low (640 x 480)	Medium (1k x 800)	High (1280 x 1024)	Medium High (1600 x 1200)	Ultra High (2k x 2k)
4-bit	Bt450	Bt450 Bt451	Bt451 Bt454 Bt455	Bt454 Bt455	
6-bit	Bt471 Bt475 Bt476	Bt471 Bt475 Bt476			
8-bit	Bt453 Bt473 Bt474 Bt477 Bt478 Bt479	Bt453 Bt457 Bt458 Bt459 Bt460 Bt461 Bt462 Bt473 Bt474 Bt477 Bt478 Bt479	Bt457 Bt458 Bt459 Bt460 Bt461 Bt462 Bt463	Bt458 Bt461 Bt462 Bt463 Bt468	Bt492

Bt450

66 MHz
Monolithic CMOS
16 x 12 Color Palette
RAMDAC™

Distinguishing Features

- 66, 50, 30 MHz Operation
- Triple 4-bit D/A Converters
- 16 x 12 Dual Port Color Palette RAM
- 3 x 12 Dual Port Overlay Palette
- RS-343A/RS-170 Compatible Outputs
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 28-pin DIP Package
- Typical Power Dissipation: 900 mW

Applications

- Graphics Terminals
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Related Products

- Bt454, Bt451
- Bt453, Bt476, Bt477

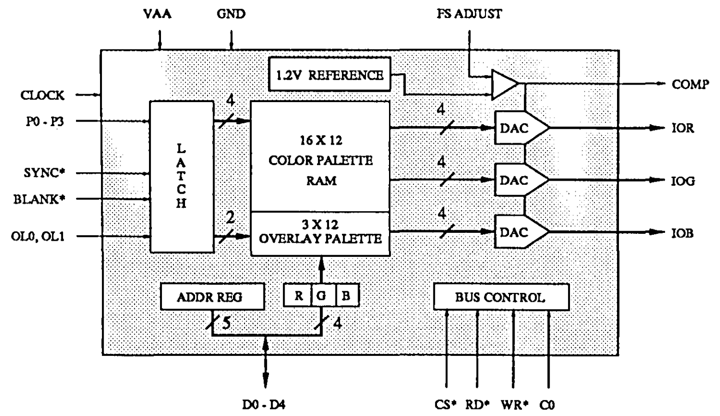
Product Description

The Bt450 is a triple 4-bit video RAMDAC, designed specifically for high-resolution color graphics, supporting up to 19 simultaneous colors from a 4096-color palette.

Three overlay registers provide for overlaying cursors, grids, menus, etc. The MPU bus operates asynchronously to the video data, simplifying the design interface to the system.

The Bt450 generates RS-343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering. Differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1/16 LSB and ±1/8 LSB, respectively, over the full temperature range.

Functional Block Diagram


VAA
GND
FS ADJUST
CLOCK
P0 - P3
SYNC*
BLANK*
OL0, OL1
1.2V REFERENCE
COMP
LATCH
4
16 X 12
COLOR PALETTE
RAM
3 X 12
OVERLAY PALETTE
2
4
4
4
DAC
DAC
DAC
IOR
IOG
IOB
ADDR REG
R
G
B
BUS CONTROL
5
4
D0 - D4
CS*
RD*
WR*
C0

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249

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Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt450 has an internal 16 x 12 color palette RAM, three 12-bit overlay registers, and three 4-bit D/A converters, allowing the display of up to 19 simultaneous colors from a 4096-color palette. The dual-port color palette RAM and dual-port overlay registers allow color updating without contention with the display refresh process.

The C0 input specifies whether the MPU is accessing the address register (logical zero), or the color palette RAM location or overlay register specified by the address register (logical one).

The 5-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. During color write cycles, color data is input from D0–D3, with D0 being the least significant bit. D4 is ignored. The MPU performs three successive write cycles (4 bits each of red, green, and blue), using C0 to select the color palette RAM and overlay registers. During the blue write cycle, the three bytes of color information are concatenated into a 12-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. During color read cycles, color data is output onto D0–D3, with D0 being the least significant bit. D4 is a logical zero. The MPU performs three successive read cycles (4 bits each of red, green, and blue), using C0 to select the color palette RAM and overlay registers. Following the blue read cycle, the address register increments to the next location, which the MPU may read by simply reading another sequence of red, green, and blue data.

The address register increments to $13 following a blue read or write cycle to location $12.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 1. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other five bits of the address register (ADDR0–4) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 1.

Figure 1 illustrates the MPU read/write timing.

Frame Buffer Interface

The P0–P3, OL0, and OL1 inputs are used to address the color palette RAM and overlay registers, as shown in Table 2. The addressed location provides 12 bits of color information to the three 4-bit D/A converters. Refer to Figure 2 for video input/output timing.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 3. Table 3 details how the SYNC* and BLANK* inputs modify the output levels.

The analog outputs of the Bt450 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Circuit Description (continued)

	Value	C0	CS*	RD*	WR*	Addressed by MPU
ADDRa, b (counts modulo 3)	00	1				red value
	01	1				green value
	10	1				blue value, increment ADDR0–4
ADDR0–4 (counts binary)	$xx	0	0	1	0	write to address register
	$00–$0F	1	0	1	0	write to color palette RAM
	$10	1	0	1	0	write to overlay color 1
	$11	1	0	1	0	write to overlay color 2
	$12	1	0	1	0	write to overlay color 3
	$xx	0	0	0	1	read address register
	$00–$0F	1	0	0	1	read color palette RAM
	$10	1	0	0	1	read overlay color 1
	$11	1	0	0	1	read overlay color 2
	$12	1	0	0	1	read overlay color 3
	$xx	x	0	0	0	invalid operation
	$xx	x	1	x	x	3-state D0–D4

Table 1. Address Register (ADDR) Operation.

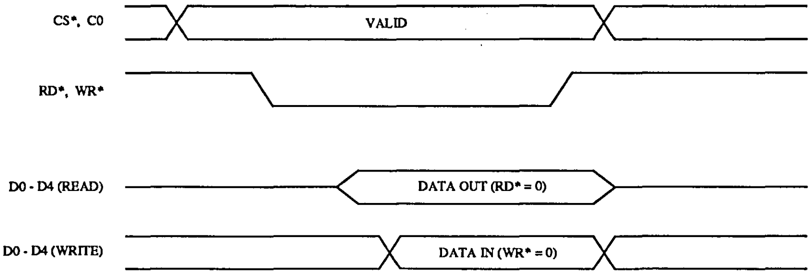


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

OL1	OL0	P0–P3	Addressed by frame buffer
0	0	$0	color palette RAM location $0
0	0	$1	color palette RAM location $1
:	:	:	:
0	0	$F	color palette RAM location $F
0	1	$x	overlay color 1
1	0	$x	overlay color 2
1	1	$x	overlay color 3

Table 2. Pixel and Overlay Control Truth Table.

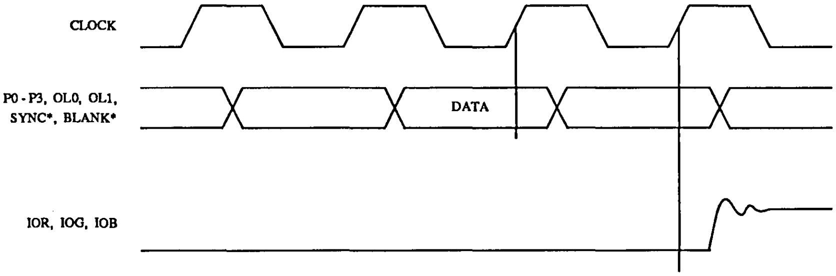
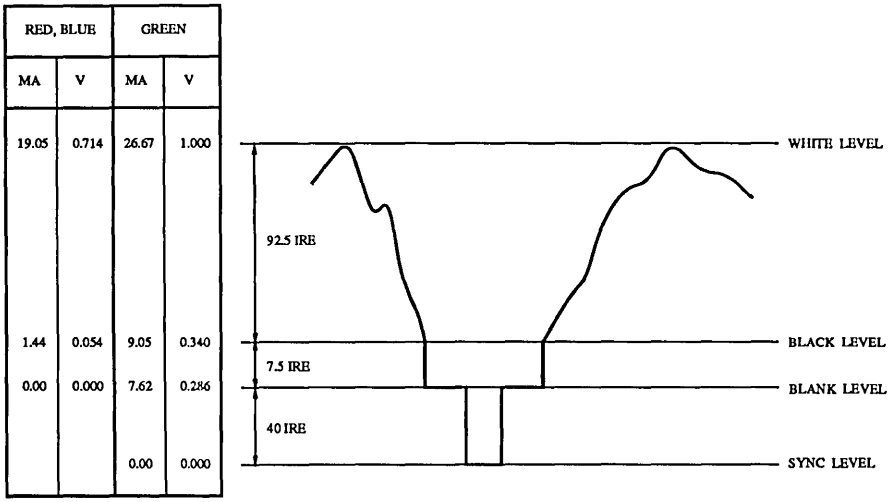

CLOCK
P0 - P3, OL0, OL1,
SYNC*, BLANK*
DATA
IOR, IOG, IOB

Figure 2. Video Input/Output Timing.

Circuit Description (continued)


RED, BLUE
GREEN
MA
V
MA
V
19.05
0.714
26.67
1.000
1.44
0.054
9.05
0.340
0.00
0.000
7.62
0.286
0.00
0.000
WHITE LEVEL
92.5 IRE
BLACK LEVEL
7.5 IRE
BLANK LEVEL
40 IRE
SYNC LEVEL

Note: 75 Ω doubly terminated load, RSET = 499 Ω. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$F
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$0
BLACK - SYNC	1.44	1.44	0	1	$0
BLANK	7.62	0	1	0	$x
SYNC	0	0	0	0	$x

Note: Typical with full-scale IOG = 26.67 mA. RSET = 499 Ω.

Table 3. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Table 3. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 3). SYNC* does not override any other control or data input, as shown in Table 3; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not to be generated on the IOG output, this pin should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P3, OL0, OL1, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
P0 - P3	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 16 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0, OL1	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 2. When accessing the overlay palette, the P0–P3 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources are capable of directly driving a doubly terminated 75-ohm coaxial cable (Figure 4). All outputs, whether used or not, should have the same output load.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 4). Note that the IRE relationships in Figure 3 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is: $\text{RSET}(\Omega) = 13{,}308 / \text{IOG (mA)}$ The amount of full-scale output current on IOR and IOB for a given RSET is: $\text{IOR, IOB (mA)} = 9{,}506 / \text{RSET}(\Omega)$

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and the adjacent VAA pin (Figure 4). The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to PC Board Layout Considerations for critical layout criteria.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.
CS*	Chip select control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. Note that the Bt450 will not function correctly while CS*, RD*, and WR* are simultaneously a logical zero.
WR*	Write control input (TTL compatible). To write data to the device, both CS* and WR* must be a logical zero. Data is latched on the rising edge of WR* or CS*, whichever occurs first. See Figure 1.
RD*	Read control input (TTL compatible). To read data from the device, both CS* and RD* must be a logical zero. See Figure 1.
C0	Command control input (TTL compatible). C0 specifies whether the MPU is accessing the address register (logical zero) or the color palettes (logical one).
D0–D4	Data bus (TTL compatible). Data is transferred into and out of the device over this 5-bit bidirectional data bus. D0 is the least significant bit.

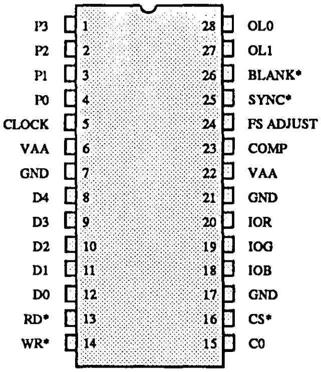

P3 1
P2 2
P1 3
P0 4
CLOCK 5
VAA 6
GND 7
D4 8
D3 9
D2 10
D1 11
D0 12
RD* 13
WR* 14
28 OL0
27 OL1
26 BLANK*
25 SYNC*
24 FS ADJUST
23 COMP
22 VAA
21 GND
20 IOR
19 IOG
18 IOB
17 GND
16 CS*
15 C0

Figure 4. 28-pin CERDIP Package.

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in *Bt451/7/8 Evaluation Module Operation and Measurements,* application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt450 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a 4-layer PC board is recommended with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

The optimum layout enables the Bt450 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8 inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground tub isolation technique is constrained by the noise margin degradation during digital readback of the Bt450.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

The analog ground plane should include all Bt450 ground pins, all reference circuitry and decoupling (external reference if used, RSET resistors, etc.), power supply bypass circuitry for the Bt450, analog output traces, and the video output connector.

Power Planes

A separate digital and analog power plane is necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt450 power pins, any reference circuitry, and COMP and reference decoupling. There should be at least a 1/8 inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 4. This bead should be located within 3 inches of the Bt450 and provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659064-3B, Fair-Rite 2743001111, or TKD BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.001 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device.

The 10 µF capacitor is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic chip capacitor. Low-frequency supply noise will require a larger value. Lead lengths should be minimized for best performance, so that the self-resonance frequency is greater than the LD* frequency.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may helpto fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt450 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10–50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10–50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt450 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt450 to minimize reflections. Unused analog outputs should be connected to GND.

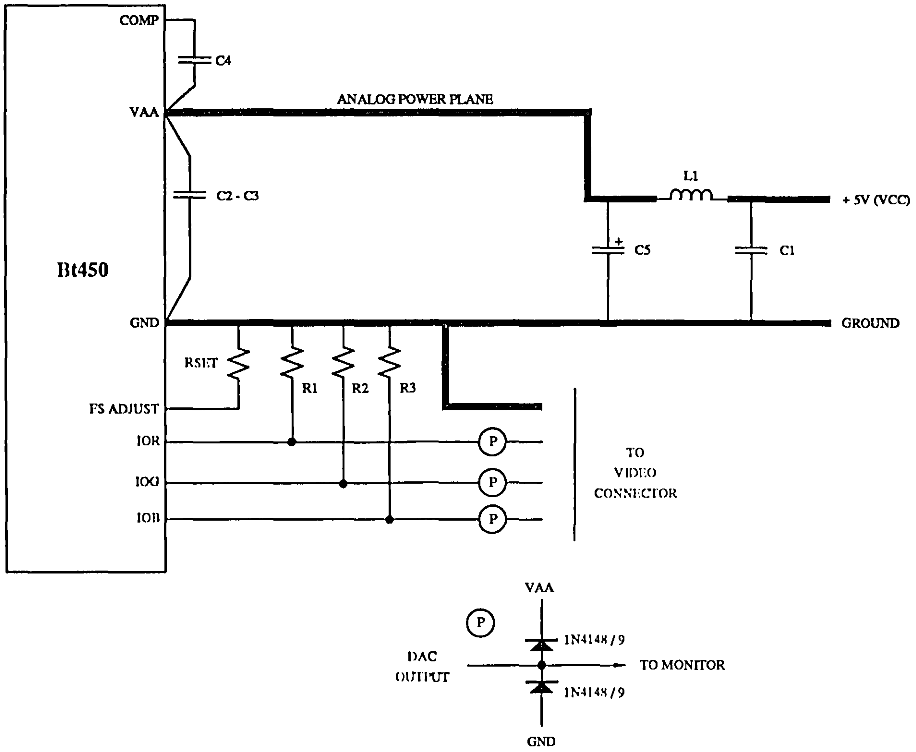
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, benefiting EMI and noise reduction.

Analog Output Protection

The Bt450 analog outputs should be protected against high energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 4 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)


COMP
C4
VAA
ANALOG POWER PLANE
L1
+ 5V (VCC)
C2 - C3
C5
C1
Bt450
GND
GROUND
RSET
R1
R2
R3
FS ADJUST
IOR
IOG
IOB
P
TO VIDEO CONNECTOR
VAA
P
1N4148/9
DAC OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description	Vendor Part Number
C1–C4	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C5	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	499 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt450.

Figure 4. Typical Connection Diagram and Parts List.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ohms
FS ADJUST Resistor	RSET		499		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND-0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		4	4	4	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1/8	LSB
Differential Linearity Error	DL			±1/16	LSB
Gray Scale Error				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			10	µA
Input Low Current (Vin = 0.4 V)	IIL			–10	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
Digital Outputs					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current	IOZ				µA
Output Capacitance	CDOUT		20		pF
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current					
White Level Relative to Blank		16.81	19.05	21.30	mA
White Level Relative to Black		15.86	17.62	19.40	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		–10	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		–10	5	50	µA
LSB Size			1.175		mA
DAC to DAC Matching			2		%
Output Compliance	VOC	–1.0		+1.4	Volts
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		30		pF
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 499 Ω. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min/Typ/Max				Units
Clock Rate	Fmax	max	66	50	30	MHz
CS*, C0 Setup Time	1	min	35	35	35	ns
CS*, C0 Hold Time	2	min	35	35	35	ns
RD*, WR* High Time	3	min	25	25	25	ns
RD* Asserted to Data Bus Driven	4	min	4	4	4	ns
RD* Asserted to Data Valid	5	max	100	100	100	ns
RD* Negated to Data Bus 3-Stated	6	max	30	30	30	ns
WR* Low Time	7	min	50	50	50	ns
Write Data Setup Time	8	min	35	35	35	ns
Write Data Hold Time	9	min	10	10	10	ns
Pixel and Control Setup Time	10	min	5	5	10	ns
Pixel and Control Hold Time	11	min	2	2	5	ns
Clock Cycle Time	12	min	15.1	20	33.3	ns
Clock Pulse Width High Time	13	min	5.8	7	10	ns
Clock Pulse Width Low Time	14	min	5.8	7	10	ns
Analog Output Delay	15	typ	15	15	25	ns
Analog Output Rise/Fall Time	16	max	7	7	7	ns
Analog Output Settling Time	17	max	20	20	25	ns
Clock and Data Feedthrough*		typ	–30	–30	–30	dB
Glitch Impulse*		typ	50	50	50	pV–sec
DAC-to-DAC Crosstalk		typ	–25	–25	–25	dB
Analog Output Skew		typ	0	0	0	ns
		max	2	2	2	ns
Pipeline Delay	18		2	2	2	Clocks
VAA Supply Current**	IAA	typ	175	140	110	mA
		max	220	175	135	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 499 Ω. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D4 output load ≤ 130 pF. See timing notes in Figure 6. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

Timing Waveforms

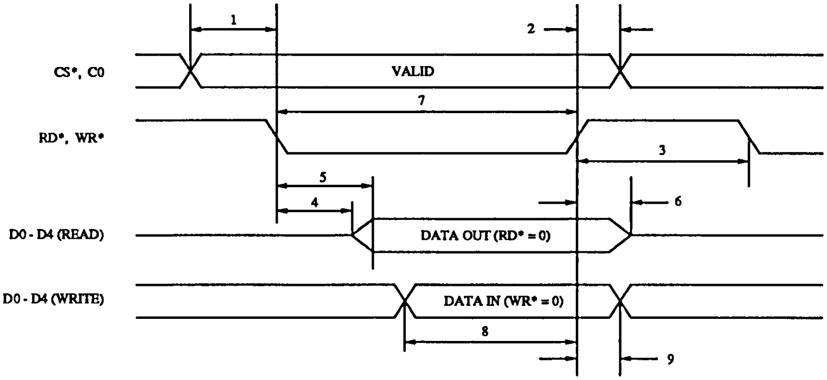
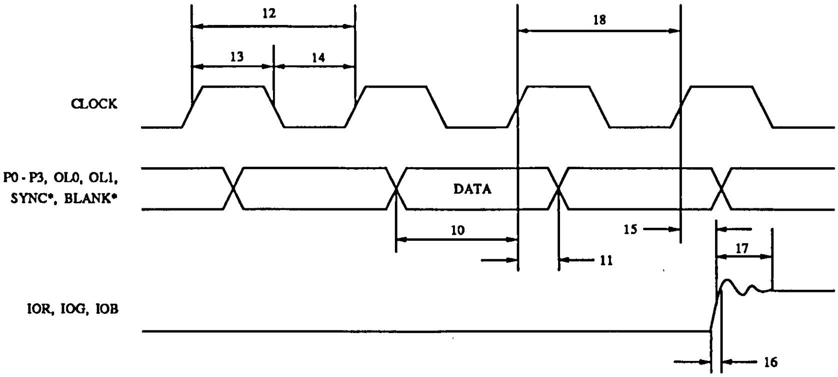

CS*, C0
RD*, WR*
D0 - D4 (READ)
D0 - D4 (WRITE)
VALID
DATA OUT (RD* = 0)
DATA IN (WR* = 0)
1
2
3
4
5
6
7
8
9

Figure 5. MPU Read/Write Timing Dimensions.


CLOCK
P0 - P3, OL0, OL1, SYNC*, BLANK*
IOR, IOG, IOB
DATA
10
11
12
13
14
15
16
17
18

Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1/8 LSB.

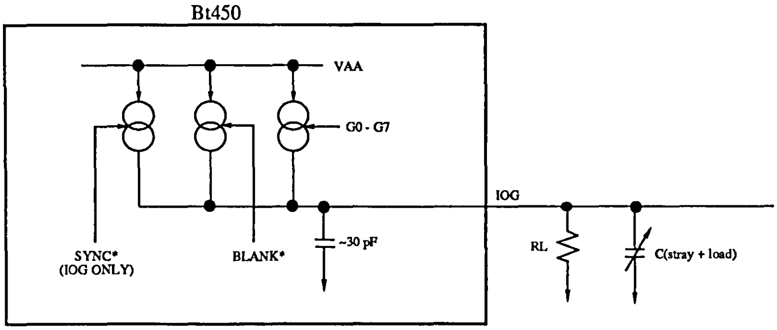
Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 6. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt450KC66	66 MHz	28-pin 0.6" CERDIP	0° to +70° C
Bt450KC50	50 MHz	28-pin 0.6" CERDIP	0° to +70° C
Bt450KC30	30 MHz	28-pin 0.6" CERDIP	0° to +70° C

Device Circuit Data


Bt450
VAA
G0 - G7
IOG
~30 pF
SYNC*
(IOG ONLY)
BLANK*
RL
C(stray + load)

Equivalent Circuit of the Current Output (IOG).

Revision History

Datasheet Revision	*Change from Previous Revision*
E	70 MHz speed grade replaced with 66 MHz. AC parameters: Clock Cycle Time (66 MHz) changed from 14.3 ns to 15.1 ns.
F	Expanded PCB layout section.
G	Changed 35 MHz operation to 30 MHz. RD* Asserted to Data Bus Driver changed from 10 ns to 4 ns. Pixel and Control Setup time changed to 5 ns for 66 MHz and 30 MHz operation.

Bt451

Bt457

Bt458

125 MHz / 165 MHz
Monolithic CMOS
256 Color Palette
RAMDAC™

Distinguishing Features

- 165, 125, 110, 80 MHz Operation
- 4:1 or 5:1 Input MUX
- 256-Word Dual Port Color Palette
- 4 Dual Port Overlay Registers
- RS-343A Compatible Outputs
- Bit Plane Read and Blink Masks
- Standard MPU Interface
- 84-pin PLCC or PGA Package
- +5 V CMOS Monolithic Construction

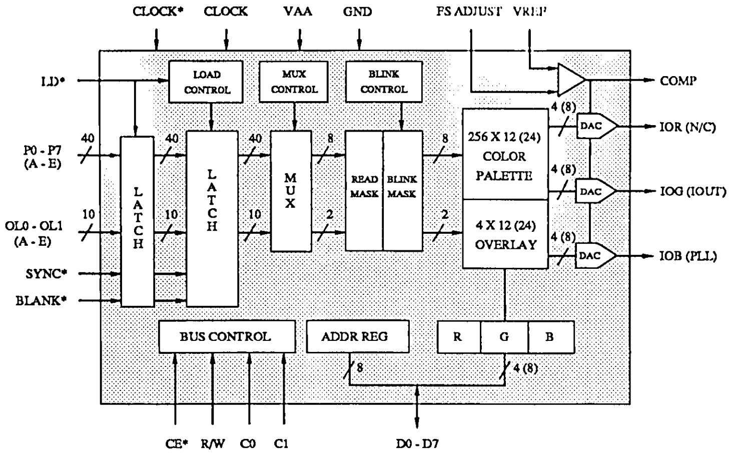
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt431, Bt438, Bt439
- Bt459, Bt460, Bt462, Bt468

Functional Block Diagram


CLOCK*
CLOCK
VAA
GND
FS ADJUST
VREF
LD*
P0 - P7 (A - E)
OL0 - OL1 (A - E)
SYNC*
BLANK*
LOAD CONTROL
MUX CONTROL
BLINK CONTROL
40
10
LATCH
MUX
8
2
READ MASK
BLINK MASK
256 X 12 (24) COLOR PALETTE
4 X 12 (24) OVERLAY
4 (8)
DAC
COMP
IOR (N/C)
IOG (IOUT)
IOB (PLL)
BUS CONTROL
ADDR REG
R
G
B
CE*
R/W
C0
C1
D0 - D7

Product Description

The Bt451, Bt457, and Bt458 are pin-compatible and software-compatible RAMDACs designed specifically for high-performance, high-resolution color graphics. The architecture enables the display of 1280 x 1024 bit-mapped color graphics (up to 8 bits per pixel plus up to 2 bits of overlay information), minimizing the use of costly ECL interfacing, as most of the high speed (pixel clock) logic is contained on chip. The multiple pixel ports and internal multiplexing enable TTL-compatible interfacing (up to 32 MHz) to the frame buffer, while maintaining the 165 MHz video data rates required for sophisticated color graphics.

The Bt451 has a 256 x 12 color lookup table with triple 4-bit video D/A converters.

The Bt458 contains a 256 x 24 color lookup table with triple 8-bit video D/A converters.

The Bt457 is a single-channel version of the Bt458 and has a 256 x 8 color lookup table with a single 8-bit video D/A converter. It includes a PLL output to enable sub-pixel synchronization of multiple Bt457s.

On-chip features include programmable blink rates, bit plane masking and blinking, color overlay capability, and a dual-port color palette RAM.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L458001 Rev. K

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt451/457/458 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and dual-port overlay registers allow color updating without contention with the display refresh process.

As illustrated in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register, color palette RAM entry, or overlay register will be accessed by the MPU.

The 8-bit address register (ADDR0–7) is used to address the internal RAM and registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Bt451/458 Reading/Writing Color Data

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. During the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word (12-bit word for the Bt451) and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. Note that the Bt451 uses only the four most significant bits of color data (D4–D7) and ignores D0–D3.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location, which the MPU may read by simply reading another sequence of red, green, and blue data. Note that the Bt451 outputs only 4 bits of color data onto D4–D7 and forces D0–D3 to a logical zero.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register 3. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR0–7) are accessible to the MPU.

ADDR0–7	C1	C0	Addressed by MPU
$xx	0	0	address register
$00–,$FF	0	1	color palette RAM
$00	1	1	overlay color 0
$01	1	1	overlay color 1
$02	1	1	overlay color 2
$03	1	1	overlay color 3
$04	1	0	read mask register
$05	1	0	blink mask register
$06	1	0	command register
$07	1	0	control/test register

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Bt457 Reading/Writing Color Data (Normal Mode)

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs a color write cycle, using C0 and C1 to select either the color palette RAM or the overlay registers. The address register then increments to the next location, which the MPU may modify by simply writing another color.

Reading color data is similar to writing, except the MPU executes read cycles.

This mode is useful if a 24-bit data bus is available, as 24 bits of color information (8 bits each of red, green, blue) may be read or written to three Bt457s in a single MPU cycle. In this application, the CE* inputs of all three Bt457s are connected together. If only an 8-bit data bus is available, the CE* inputs must be individually selected during the appropriate color write cycle (red CE* during red write cycle, blue CE* during blue write cycle, etc.).

When accessing the color palette RAM, the address register resets to $00 after a read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a read or write cycle to overlay register 3.

Bt457 Reading/Writing Color Data (RGB Mode)

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the color palette RAM or the overlay registers. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. Reading color data is similar to writing, except the MPU executes read cycles.

This mode is useful if only an 8-bit data bus is available. Each Bt457 is programmed to be a red, green, or blue RAMDAC, and will respond only to the assigned color read or write cycle. In this application, the Bt457s share a common 8-bit data bus. The CE* inputs of all three Bt457s must be asserted simultaneously only during color read/write cycles and address register write cycles.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register 3. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 8t bits of the address register (ADDR0-7) are accessible to the MPU.

Additional Information

Although the color palette RAM and overlay registers are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Accessing the control registers is also done through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt451/457/458 incorporate internal latches and multiplexers. As illustrated in Figure 1, on the rising edge of LD*, sync and blank information, color (up to 8 bits per pixel), and overlay (up to 2 bits per pixel) information, for either four or five consecutive pixels, are latched into the device. Note that, with this configuration, the sync and blank timing will be recognized only with four- or five-pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing.

Each clock cycle, the Bt451/457/458 outputs color information based on the {A} inputs, followed by the {B} inputs, etc., until all four or five pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external character or cursor generation logic.

To simplify the frame buffer interface timing, LD* may be phase shifted, in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by four or five, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than four, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*.

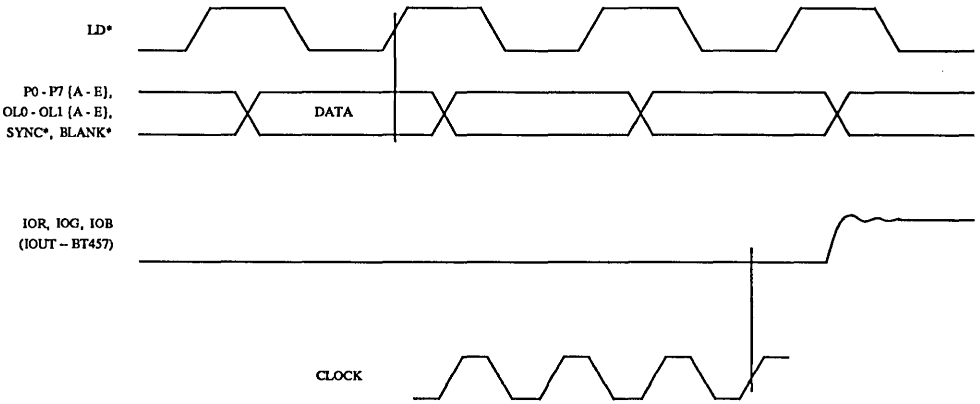


Figure 1. Video Input/Output Timing.

Circuit Description (continued)

Color Selection

Each clock cycle, 8 bits of color information (P0–P7) and 2 bits of overlay information (OL0, OL1) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual bit planes may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change due to blinking does not occur during the active display time (i.e., in the middle of the screen), the Bt451/457/458 monitors the BLANK* input to determine vertical retrace intervals. A vertical retrace interval is recognized by determining that BLANK* has been a logical zero for at least 256 LD* cycles.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAM. Table 2 illustrates the truth table used for color selection.

Video Generation

Every clock cycle, the selected color information from the color palette RAMs or overlay registers is presented to the D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 2.

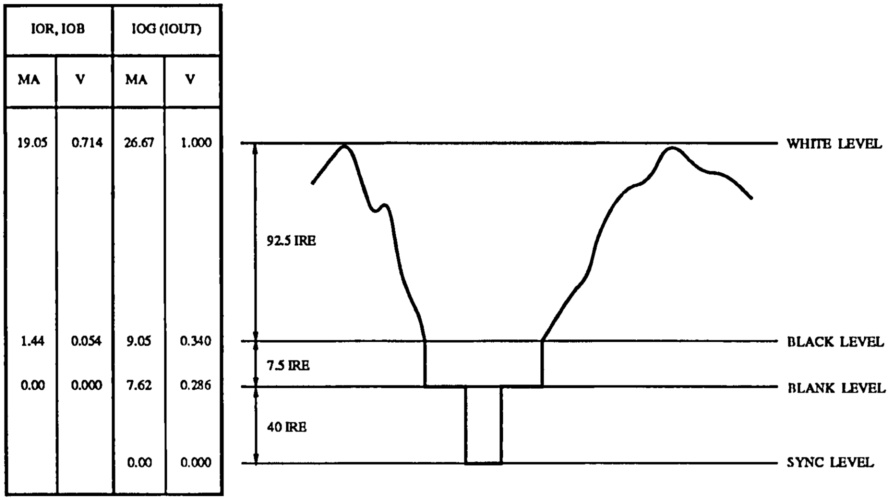
The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Note that only the green output (IOG) on the Bt451 and Bt458 contains sync information. Table 3 details how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt451, Bt457, and Bt458 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current-steering their outputs. An on-chip operational amplifier stabilizes the D/A converter's full scale output current against temperature and power supply variations.

CR6	OL1	OL0	P0–P7	Addressed by frame buffer
1	0	0	$00	color palette entry $00
1	0	0	$01	color palette entry $01
:	:	:	:	:
1	0	0	$FF	color palette entry $FF
0	0	0	$xx	overlay color 0
x	0	1	$xx	overlay color 1
x	1	0	$xx	overlay color 2
x	1	1	$xx	overlay color 3

Table 2. Palette and Overlay Select Truth Table.

Circuit Description (continued)


IOR, IOB
IOG (IOUT)
MA
V
MA
V
19.05
0.714
26.67
1.000
1.44
0.054
9.05
0.340
0.00
0.000
7.62
0.286
0.00
0.000
WHITE LEVEL
92.5 IRE
BLACK LEVEL
7.5 IRE
BLANK LEVEL
40 IRE
SYNC LEVEL

Note: 75 Ω doubly terminated load, RSET = 523 Ω, VREF = 1.235 V. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms.

Description	IOG (IOUT) (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 523 Ω, VREF = 1.235 V. Note that the Bt451 uses only the upper four DAC input data bits.

Table 3. Video Output Truth Table.

Internal Registers

Command Register

The command register may be written to or read by the MPU at any time, and is not initialized. CR0 corresponds to data bus bit D0.

CR7	Multiplex select (0) 4:1 multiplexing (1) 5:1 multiplexing	This bit specifies whether 4:1 or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 4:1 is specified, the {E} pixel and {E} overlay inputs are ignored and should be connected to GND, and the LD* input should be 1/4 the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be 1/5 the CLOCK rate. Note that it is possible to reset the pipeline delay of the Bt457/458 to a fixed eight clock cycles. In this instance, each time the input multiplexing is changed, the Bt457/458 must again be reset to a fixed pipeline delay.
CR6	RAM enable (0) use overlay color 0 (1) use color palette RAM	When the overlay select bits are 00, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information.
CR5, CR4	Blink rate selection (00) 16 on, 48 off (25/75) (01) 16 on, 16 off (50/50) (10) 32 on, 32 off (50/50) (11) 64 on, 64 off (50/50)	These 2 bits control the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (% on/off).
CR3	OL1 blink enable (0) disable blinking (1) enable blinking	If a logical one, this bit forces the OL1 {A–E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL1 {A–E} inputs. In order for overlay 1 bit plane to blink, bit CR1 must be set to a logical one.
CR2	OL0 blink enable (0) disable blinking (1) enable blinking	If a logical one, this bit forces the OL0 {A–E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL0 {A–E} inputs. In order for overlay 0 bit plane to blink, bit CR0 must be set to a logical one.

Internal Registers (continued)

Command Register (continued)

CR1	OL1 display enable (0) disable (1) enable	If a logical zero, this bit forces the OL1 {A-E} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL1 {A-E} inputs.
CR0	OL0 display enable (0) disable (1) enable	If a logical zero, this bit forces the OL0 {A-E} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL0 {A-E} inputs.

Read Mask Register

The read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. D0 corresponds to bit plane 0 (P0 {A-E}) and D7 corresponds to bit plane 7 (P7 {A-E}). Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized.

Blink Mask Register

The blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by the command register. D0 corresponds to bit plane 0 (P0 {A-E}) and D7 corresponds to bit plane 7 (P7 {A-E}). In order for a bit plane to blink, the corresponding bit in the read mask register must be a logical one. This register may be written to or read by the MPU at any time and is not initialized.

Internal Registers (continued)

Bt451/458 Test Register

The test register provides diagnostic capability by enabling the MPU to read the inputs to the D/A converters. It may be written to or read by the MPU at any time, and is not initialized. When writing to the register, the upper 4bits (D4–D7) are ignored.

The contents of the test register are defined as follows:

D7–D4	color information (4 bits of red, green, or blue)
D3	low (logical one) or high (logical zero) nibble
D2	blue enable
D1	green enable
D0	red enable

To use the test register, the host MPU writes to it, setting one, and only one, of the (red, green, blue) enable bits. These bits specify which 4 bits of color information the MPU wishes to read (R0–R3, G0–G3, B0–B3, R4–R7, G4–G7, or B4–B7). When the MPU reads the test register, the 4 bits of color information from the DAC inputs are contained in the upper 4 bits, and the lower 4 bits contain the (red, green, blue, low or high nibble) enable information previously written. Note that either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

For example, to read the upper 4 bits of red color information being presented to the D/A converters, the MPU writes to the test register, setting only the red enable bit. The MPU then proceeds to read the test register, keeping the pixel data stable, which results in D4–D7 containing R4–R7 color bits, and D0–D3 containing (red, green, blue, low or high nibble) enable information, as illustrated below:

D7	R7
D6	R6
D5	R5
D4	R4
D3	0
D2	0
D1	0
D0	1

Note that since the Bt451 has 4-bit D/A converters, bit D3 of the test register will always be a logical zero.

Internal Registers (continued)

Bt457 Control/Test Register

The control/test register provides diagnostic capability by enabling the MPU to read the inputs to the D/A converter. It may be written to or read by the MPU at any time, and is not initialized. When writing to the register, the upper 4 bits (D4–D7) are ignored.

The contents of the test register are defined as follows:

D7-D4	color information
D3	low (logical one) or high (logical zero) nibble
D2	blue channel enable
D1	green channel enable
D0	red channel enable

To use the control/test register, the MPU writes to it, specifying the low or high nibble of color information. When the MPU reads the register, the 4 bits of color information from the DAC inputs are contained in the upper 4 bits, and the lower 4 bits contain whatever was previously written to the register. Note that either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

The red, green, and blue enable bits are used to specify the mode of writing color data to, and reading color data from, the Bt457. If all three enable bits are a logical zero, each write cycle to the color palette RAM or overlay registers loads 8 bits of color data. During each read cycle of the color palette RAM or overlay registers, 8 bits of color data are output onto the data bus. If a 24-bit data bus is available, this enables three Bt457s to be accessed simultaneously.

If any of the red, green, blue enable bits are a logical one, the Bt457 assumes the MPU is reading and writing color information using red, green, blue cycles, such as are used on the Bt451 and Bt458. Setting the appropriate enable bit configures the Bt457 to output or input color data only for the color read/write cycle corresponding to the enabled color. Thus, if the green enable bit is a logical one, and a red, green, blue write cycle occurred, the Bt457 would input data only during the green write cycle. If a red, green, blue read cycle occurred, the Bt457 would output data only during the green read cycle. Note that CE* must be a logical zero during each of the red, green, blue cycles. One, and only one, of the enable bits must be a logical one. This mode of operation is useful where only an 8-bit data bus is available, and the software drivers are written for RGB operation.

Pin Descriptions

Pin Name — **Description**

BLANK*

Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Table 3. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.

SYNC*

Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 3; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of LD*. If sync information is not to be generated on the IOG output, this pin should be connected to GND.

LD*

Load control input (TTL compatible). The P0–P7 {A–E}, OL0–OL1 {A–E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD*, while it is either 1/4 or 1/5 the CLOCK rate, may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle, within the limits specified by the AC Characteristics section.

P0–P7 {A–E}

Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. Either four or five consecutive pixels (up to 8 bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND.

Note that the {A} pixel is output first, followed by the {B} pixel, etc., until all four or five pixels have been output, at which point the cycle repeats.

OL0–OL1 {A–E}

Overlay select inputs (TTL compatible). These control inputs are latched on the rising edge of LD*, and in conjunction with bit 6 of the command register, specify which palette is to be used for color information, as follows:

OL1	OL0	CR6 = 1	CR6 = 0
0	0	color palette RAM	overlay color 0
0	1	overlay color 1	overlay color 1
1	0	overlay color 2	overlay color 2
1	1	overlay color 3	overlay color 3

When accessing the overlay palette, the P0–P7 {A–E} inputs are ignored. Overlay information bits (up to 2 bits per pixel) for either four or five consecutive pixels are input through this port. Unused inputs should be connected to GND.

IOR, IOG, IOB, IOUT

Red, green, and blue video current outputs. These high -mpedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 3). The Bt457 outputs IOUT rather than IOR, IOG, and IOB.

PLL

Phase lock loop current output—Bt457 only. This high-impedance current source is used to enable multiple Bt457s to be synchronized with sub-pixel resolution when used with an external PLL. A logical one on the BLANK* input results in no current being output onto this pin, while a logical zero results in the following current being output:

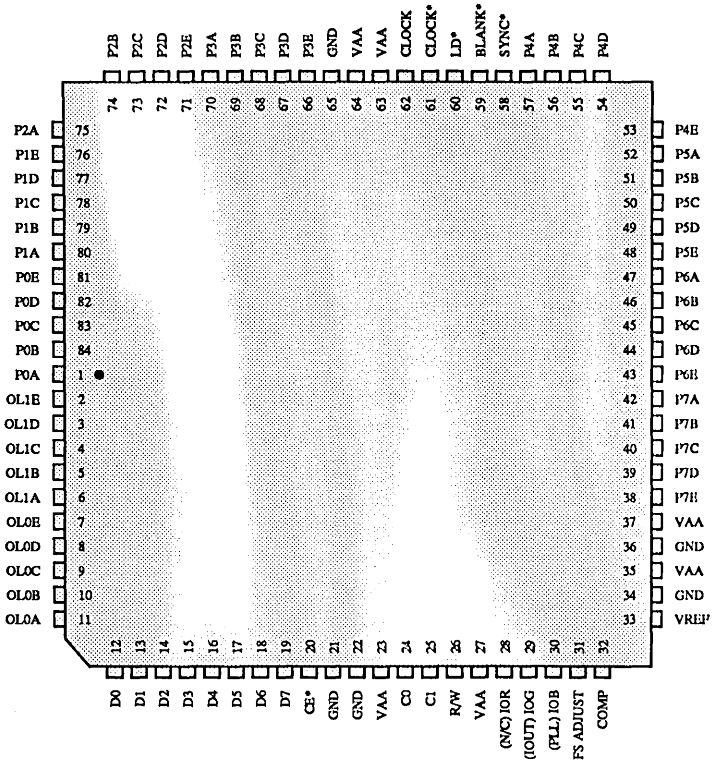
$$\text{PLL (mA)} = 3{,}227 * \text{VREF (V)} / \text{RSET } (\Omega)$$

If sub-pixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 Ω).

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 3). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. *Refer to PC Board Layout Considerations for critical layout criteria.*
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 3). Note that the IRE relationships in Figure 2 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG (or IOUT for the Bt457) is: $\text{RSET}\,(\Omega) = 11{,}294 * \text{VREF}\,(\text{V}) / \text{IOG}\,(\text{mA})$ The full scale output current on IOR and IOB (for the Bt451 and Bt458) for a given RSET is: $\text{IOR, IOB}\,(\text{mA}) = 8{,}067 * \text{VREF}\,(\text{V}) / \text{RSET}\,(\Omega)$
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 3, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 3. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Care should be taken to avoid glitches on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)—84-Pin J-Lead Package


P2B 74
P2C 73
P2D 72
P2E 71
P3A 70
P3B 69
P3C 68
P3D 67
P3E 66
GND 65
VAA 64
VAA 63
CLOCK 62
CLOCK* 61
LD* 60
BLANK* 59
SYNC* 58
P4A 57
P4B 56
P4C 55
P4D 54
P2A 75
P1E 76
P1D 77
P1C 78
P1B 79
P1A 80
P0E 81
P0D 82
P0C 83
P0B 84
P0A 1
OL1E 2
OL1D 3
OL1C 4
OL1B 5
OL1A 6
OL0E 7
OL0D 8
OL0C 9
OL0B 10
OL0A 11
53 P4E
52 P5A
51 P5B
50 P5C
49 P5D
48 P5E
47 P6A
46 P6B
45 P6C
44 P6D
43 P6E
42 P7A
41 P7B
40 P7C
39 P7D
38 P7E
37 VAA
36 GND
35 VAA
34 GND
33 VREF
12 D0
13 D1
14 D2
15 D3
16 D4
17 D5
18 D6
19 D7
20 CE*
21 GND
22 GND
23 VAA
24 C0
25 C1
26 R/W
27 VAA
28 (N/C) IOR
29 (IOUT) IOG
30 (PLL) IOB
31 FS ADJUST
32 COMP

Note: Bt457 pin names are in parentheses.

4

Pin Descriptions (continued)—84-pin PGA Package

Signal	Pin Number
BLANK*	L9
SYNC*	M10
LD*	M9
CLOCK*	L8
CLOCK	M8
P0A	G1
P0B	G2
P0C	H1
P0D	H2
P0E	J1
P1A	J2
P1B	K1
P1C	L1
P1D	K2
P1E	L2
P2A	K3
P2B	M1
P2C	L3
P2D	M2
P2E	M3
P3A	L4
P3B	M4
P3C	L5
P3D	M5
P3E	L6
P4A	M11
P4B	L10
P4C	L11
P4D	K10
P4E	M12
P5A	K11
P5B	L12
P5C	K12
P5D	J11
P5E	J12
P6A	H11
P6B	H12
P6C	G12
P6D	G11
P6E	F12
P7A	F11
P7B	E12
P7C	E11
P7D	D12
P7E	D11
OL0A	A1
OL0B	C2
OL0C	B1
OL0D	C1
OL0E	D2
OL1A	D1
OL1B	E2
OL1C	E1
OL1D	F1
OL1E	F2
IOG (IOUT)	A10
IOB (PLL)	A11
IOR (N/C)	B9
VAA	C12
VAA	C11
VAA	A9
VAA	L7
VAA	M7
VAA	A7
GND	B12
GND	B11
GND	M6
GND	B6
GND	A6
COMP	A12
FS ADJUST	B10
VREF	C10
CE*	A5
R/W	B8
C1	A8
C0	B7
D0	C3
D1	B2
D2	B3
D3	A2
D4	A3
D5	B4
D6	A4
D7	B5

Note: Bt457 pin names are in parentheses.

Pin Descriptions (continued)—84-pin PGA Package

Bt451/457/458

(TOP VIEW)

12	COMP	GND	VAA	P7D	P7B	P6E	P6C	P6B	P5E	P5C	P5B	P4E
11	IOB	GND	VAA	P7E	P7C	P7A	P6D	P6A	P5D	P5A	P4C	P4A
10	IOG	FS ADJ	VREF							P4D	P4B	SYNC*
9	VAA	IOR									BLK*	LD*
8	C1	R/W									CLK*	CLK
7	VAA	C0									VAA	VAA
6	GND	GND									P3E	GND
5	CE*	D7									P3C	P3D
4	D6	D5									P3A	P3B
3	D4	D2	D0							P2A	P2C	P2E
2	D3	D1	OL0B	OL0E	OL1B	OL1E	P0B	P0D	P1A	P1D	P1E	P2D
1	OL0A	OL0C	OL0D	OL1A	OL1C	OL1D	P0A	P0C	P0E	P1B	P1C	P2B
	A	B	C	D	E	F	G	H	J	K	L	M

alignment marker (on top)

(BOTTOM VIEW)

12	P4E	P5B	P5C	P5E	P6B	P6C	P6E	P7B	P7D	VAA	GND	COMP
11	P4A	P4C	P5A	P5D	P6A	P6D	P7A	P7C	P7E	VAA	GND	IOB
10	SYNC*	P4B	P4D							VREF	FS ADJ	IOG
9	LD*	BLK*									IOR	VAA
8	CLK	CLK*									R/W	C1
7	VAA	VAA									C0	VAA
6	GND	P3E									GND	GND
5	P3D	P3C									D7	CE*
4	P3B	P3A									D5	D6
3	P2E	P2C	P2A							D0	D2	D4
2	P2D	P1E	P1D	P1A	P0D	P0B	OL1E	OL1B	OL0E	OL0B	D1	D3
1	P2B	P1C	P1B	P0E	P0C	P0A	OL1D	OL1C	OL1A	OL0D	OL0C	OL0A
	M	L	K	J	H	G	F	E	D	C	B	A

Pin	Bt451/458	Bt457
A10	IOG	IOUT
A11	IOB	PLL
B9	IOR	N/C

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in *Bt451/457/458 Evaluation Module Operation and Measurements,* application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt451/457/458 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a 6-layer PC board is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane (preferable analog ground plane), layer 3 the analog power plane, using the remaining layers for digital traces and digital power supplies.

The optimum layout enables the Bt451/457/458 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8" inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground partitioning isolation technique is constrained by the noise margin degradation during digital readback of the Bt451/457/458.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

For maximum performance, a separate isolated ground plane for the analog output termination resistors, RSET resistor, and VREF circuitry should be used, as shown in Figure 3. Another isolated ground plane is used for the GND pins of the Bt451/457/458 and supply decoupling capacitors.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt451/457/458 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt451/457/458 and provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor decoupling each of three groups of VAA pins to GND. The capacitors should be placed as close as possible to the device.

The 33 µF capacitor is for low frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. Low frequency supply noise will require a larger value. Lead lengths should be minimized for best performance so that the self-resonance frequency is greater than the LD* frequency.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may helpto fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt451/457/458 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit by using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt451/457/458 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt451/457/458 to minimize reflections. Unused analog outputs should be connected to GND.

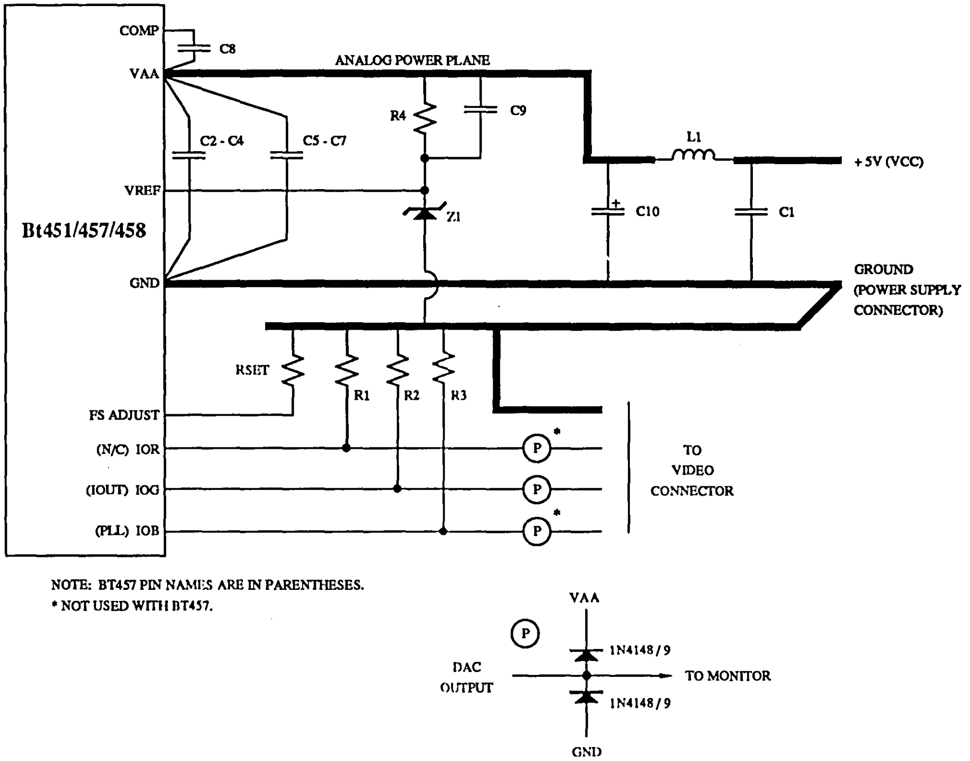
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

Analog Output Protection

The Bt451/457/458 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 3 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)


COMP
C8
VAA
ANALOG POWER PLANE
R4
C9
C2 - C4
C5 - C7
L1
+5V (VCC)
VREF
Z1
C10
C1
Bt451/457/458
GND
GROUND
(POWER SUPPLY
CONNECTOR)
RSET
R1
R2
R3
FS ADJUST
(N/C) IOR
(IOUT) IOG
(PLL) IOB
P
TO
VIDEO
CONNECTOR
VAA
1N4148/9
DAC
OUTPUT
TO MONITOR
GND

NOTE: BT457 PIN NAMES ARE IN PARENTHESES.
* NOT USED WITH BT457.

Location	Description	Vendor Part Number
C1–C4, C8, C9	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C5–C7	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C10	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt451/457/458. R3 not used with Bt457 (see Application Information section).

Figure 3. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Due to the high clock rates at which the Bt451/457/458 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (typically a 220 Ω resistor to VCC and a 330 Ω resistor to GND). The termination resistors should be as close as possible to the Bt451/457/458.

165 MHz applications require robust ECL clock signals with strong pull-down (~20 mA at VOH) and double termination for clock trace lengths greater than 2 inches.

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak due to the noise margins of the CMOS process. The Bt451/457/458 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by four or five (depending on whether 4:1 or 5:1 multiplexing was specified) and translating it to TTL levels. As LD* may be phase-shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

It is recommended that the Bt438 or Bt439 Clock Generator Chips be used to generate the clock and load signals. Both support the 4:1 and 5:1 input multiplexing of the Bt451/457/458, and set the pipeline delay of the Bt457 and Bt458 to eight clock cycles. Figures 4 and 5 illustrate using the Bt438 with the Bt451/457/458.

In applications using a single Bt457, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150 Ω).

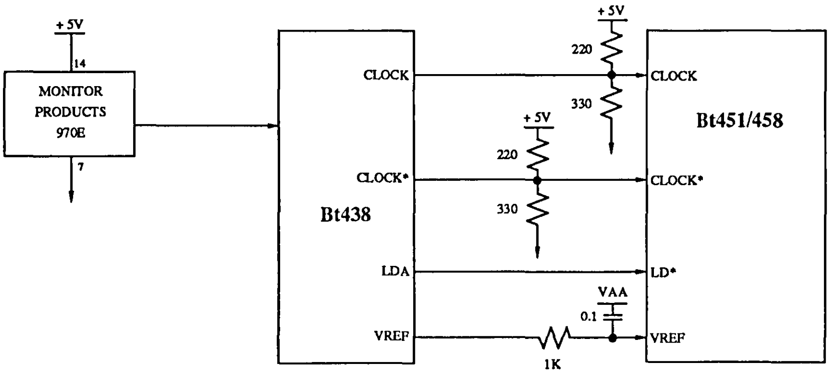


Figure 4. Generating the Bt451/458 Clock Signals.

Application Information (continued)

Setting the Pipeline Delay (Bt457, Bt458)

The pipeline delay of the Bt457/458, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The Bt457/458 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438 and Bt439 Clock Generator Chips support this mode of operation when used with the Bt457/458.

To reset the Bt457/458, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for at least three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than one clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

The resetting of the Bt457/458 to an eight clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if the multiple Bt457/458s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control via the read mask register and overlay display enable bits.

In standard operation, the Bt457/458 need be reset only following a power-up or reset condition. Under these circumstances the on-chip blink circuitry may be used.

Bt457 Color Display Applications

For color display applications where up to four Bt457s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1, and 5:1 input multiplexing of the Bt457, synchronizes them to sub-pixel resolution, and sets the pipeline delay of the Bt457 to eight clock cycles. The Bt439 may also be used to interface the Bt457 to a TTL clock. Figure 6 illustrates using the Bt439 with the Bt457.

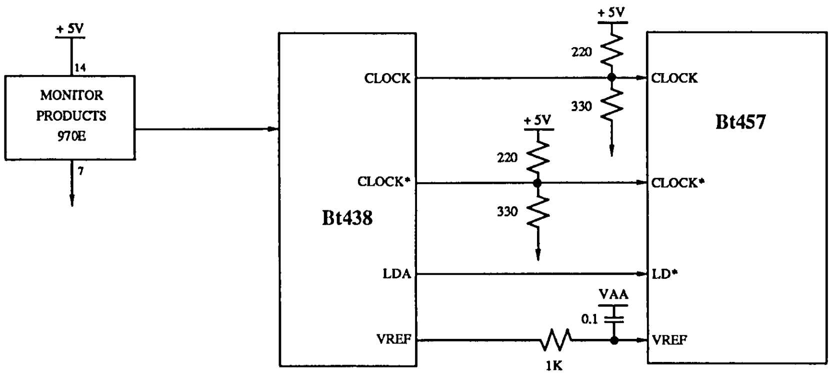


Figure 5. Generating the Bt457 Clock Signals (Monochrome Application).

Application Information (continued)

Sub-pixel synchronization is supported via the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt457, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt457s, and adjusts the phase of each of the CLOCK and CLOCK* signals to the Bt457s to minimize the PLL phase difference. There should be minimal layout skew in the CLOCK and PLL trace paths to assure proper clock alignment.

If sub-pixel synchronization of multiple Bt457s is not necessary, the Bt438 Clock Generator Chip may be used instead of the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt457s are connected together and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). The VREF inputs of the Bt457s must still have a 0.1 µF bypass capacitor to VAA. The PLL outputs would not be used and should be connected to GND (either directly or through a resistor up to 150 Ω).

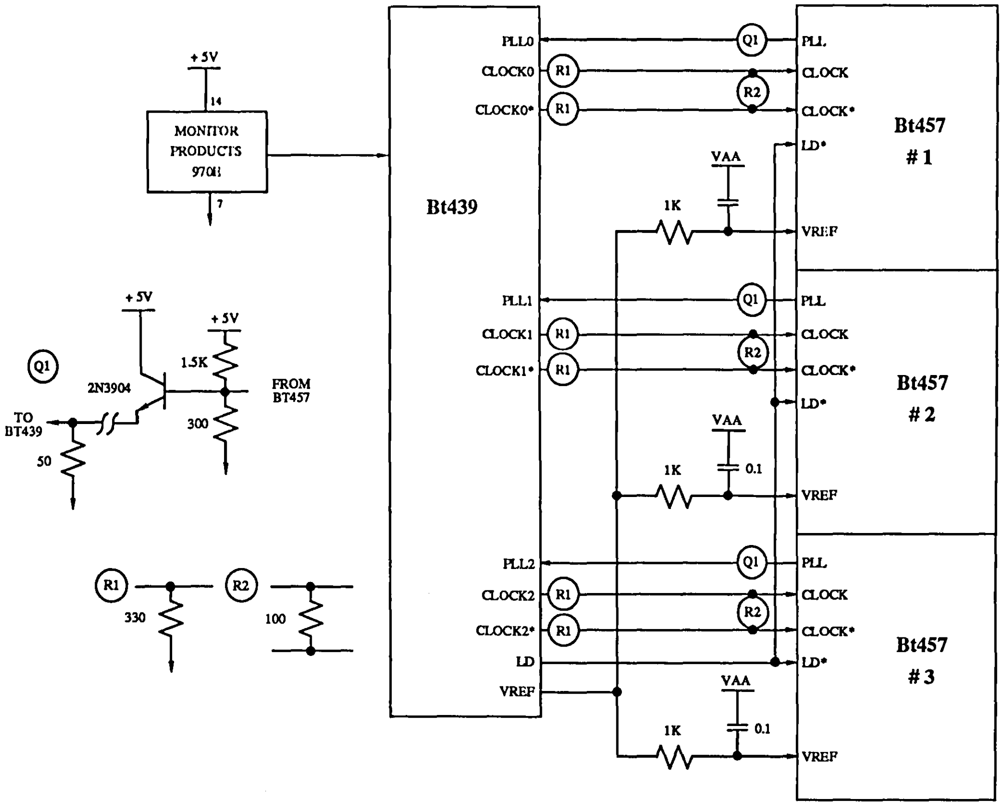

+5V
14
MONITOR PRODUCTS 970H
7
Bt439
PLL0
CLOCK0
CLOCK0*
PLL1
CLOCK1
CLOCK1*
PLL2
CLOCK2
CLOCK2*
LD
VREF
R1
R2
Q1
VAA
1K
0.1
PLL
CLOCK
CLOCK*
LD*
VREF
Bt457 #1
Bt457 #2
Bt457 #3
Q1
+5V
+5V
2N3904
1.5K
FROM BT457
TO BT439
300
50
R1
330
R2
100

Figure 6. Generating the Bt457 Clock Signals (Color Application).

Application Information (continued)

Using Multiple Devices

When using multiple RAMDACs, each RAMDAC should have its own power plane ferrite bead. In addition, a single voltage reference may drive multiple devices; however, isolation resistors are recommended to reduce color channel crosstalk.

Higher performance may be obtained if each RAMDAC has its own voltage reference. This may further reduce the amount of color channel crosstalk and color palette interaction.

Each RAMDAC must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

Bt457 Non-Video Applications

The Bt457 may be used in non-video applications by disabling the video-specific control signals. SYNC* should be a logical zero and BLANK* should be a logical one.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

$$\text{RSET}\ (\Omega) = 7{,}457 * \text{VREF}\ (\text{V}) / \text{Iout}\ (\text{mA})$$

With the DAC data inputs at $00, there is a DC offset current (Imin) defined as follows:

$$\text{Imin}\ (\text{mA}) = 610 * \text{VREF}\ (\text{V}) / \text{RSET}\ (\Omega)$$

Therefore, the total full-scale output current will be Iout + Imin.

Initializing the Bt451/458

Following a power-on sequence, the Bt451/458 must be initialized. If controlling the clock/LD* sequence to reset the pipeline delay of the Bt458 to a fixed pipeline delay of eight clock cycles, this initialization sequence must be performed after the reset sequence. The command register must also be re-initialized any time the multiplex selection is changed (i.e., from 4:1 to 5:1 input multiplexing).

This sequence will configure the Bt451/458 as follows:

4:1 multiplexed operation
no overlays
no blinking

Control Register Initialization	C1, C0
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $00 to test register	10

Color Palette RAM Initialization

Write $00 to address register	00
Write red data to RAM (location $00)	01
Write green data to RAM (location $00)	01
Write blue data to RAM (location $00)	01
Write red data to RAM (location $01)	01
Write green data to RAM (location $01)	01
Write blue data to RAM (location $01)	01
:	:
Write red data to RAM (location $FF)	01
Write green data to RAM (location $FF)	01
Write blue data to RAM (location $FF)	01

Overlay Color Palette Initialization

Write $00 to address register	00
Write red data to overlay (location $00)	11
Write green data to overlay (location $00)	11
Write blue data to overlay (location $00)	11
Write red data to overlay (location $01)	11
Write green data to overlay (location $01)	11
Write blue data to overlay (location $01)	11
:	:
Write red data to overlay (location $03)	11
Write green data to overlay (location $03)	11
Write blue data to overlay (location $03)	11

Application Information (continued)

Initializing the Bt457 (Monochrome)

Following a power-on sequence, the Bt457 must be initialized. If controlling the clock/LD* sequence to reset the pipeline delay of the Bt457 to a fixed pipeline delay of eight clock cycles, this initialization sequence must be performed after the reset sequence. The command register must also be re-initialized any time the multiplex selection is changed (i.e., from 4:1 to 5:1 input multiplexing).

This sequence will configure the Bt457 as follows:

4:1 multiplexed operation
no overlays
no blinking
color data written/read every cycle

Control Register Initialization	C1, C0
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $00 to test register	10

Color Palette RAM Initialization	
Write $00 to address register	00
Write data to RAM (location $00)	01
Write data to RAM (location $01)	01
:	:
Write data to RAM (location $FF)	01

Overlay Color Palette Initialization	
Write $00 to address register	00
Write data to overlay (location $00)	11
Write data to overlay (location $01)	11
:	:
Write data to overlay (location $03)	11

Initializing the Bt457 (Color) 24-bit MPU Data Bus

In this example, three Bt457s are being used in parallel to generate true color. A 24-bit MPU data bus is available for accessing all three Bt457s in parallel.

The operation and initialization are the same as for the Bt457 being used in a monochrome application.

Initializing the Bt457 (Color) 8-bit MPU Data Bus

In this example, three Bt457s are being used in parallel to generate true color. An 8-bit MPU data bus is available for accessing the Bt457s.

Note that while accessing the command, read mask, blink mask, and control/test, and address register, each Bt457 must be accessed individually. While accessing the color palette RAM or overlay registers, all three Bt457s are accessed simultaneously.

Following a power-on sequence, the Bt457s must be initialized. If controlling the clock/LD* sequence to reset the pipeline delay of the Bt457s to a fixed pipeline delay of eight clock cycles, this initialization sequence must be performed after the reset sequence. The command register must also be re-initialized any time the multiplex selection is changed (i.e., from 4:1 to 5:1 input multiplexing).

This sequence will configure the Bt457s as follows:

4:1 multiplexed operation
no overlays
no blinking
initialize each Bt457 as a red, green, or blue device

Control Register Initialization	C1, C0
Red Bt457	
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $01 to test register	10
Green Bt457	
Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $02 to test register	10

Application Information (continued)

Blue Bt457

Write $04 to address register	00
Write $FF to read mask register	10
Write $05 to address register	00
Write $00 to blink mask register	10
Write $06 to address register	00
Write $40 to command register	10
Write $07 to address register	00
Write $04 to test register	10

Color Palette RAM Initialization

Write $00 to all three address registers	00
Write red data to RAM (location $00)	01
Write green data to RAM (location $00)	01
Write blue data to RAM (location $00)	01
Write red data to RAM (location $01)	01
Write green data to RAM (location $01)	01
Write blue data to RAM (location $01)	01
:	:
Write red data to RAM (location $FF)	01
Write green data to RAM (location $FF)	01
Write blue data to RAM (location $FF)	01

Overlay Color Palette Initialization

Write $00 to all three address registers	00
Write red data to overlay (location $00)	11
Write green data to overlay (location $00)	11
Write blue data to overlay (location $00)	11
Write red data to overlay (location $01)	11
Write green data to overlay (location $01)	11
Write blue data to overlay (location $01)	11
:	:
Write red data to overlay (location $03)	11
Write green data to overlay (location $03)	11
Write blue data to overlay (location $03)	11

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	Volts
FS ADJUST Resistor	RSET		523		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND-0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8 (4)	8 (4)	8 (4)	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1 (1/8)	LSB
Differential Linearity Error	DL			±1 (1/16)	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	.6		6	Volts
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = –800 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	Volts
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG or IOUT		6.29	7.62	8.96	mA
Sync Level on IOG or IOUT		0	5	50	µA
LSB Size					
Bt451			1.175		mA
Bt457, Bt458			69.1		µA
DAC to DAC Matching*			2	5	%
Output Compliance	VOC	-1.0		+1.2	Volts
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.5		%/%ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Does not apply to the Bt457.

AC Characteristics

		165 MHz Devices			125 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			165			125	MHz
LD* Rate	LDmax			41.25			31.25	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	15			15			ns
CE* Low Time	3	50			50			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	7			7			ns
CE* Asserted to Data Valid	6			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	3			3			ns
Pixel and Control Setup Time	10	3			3			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	6.06			8			ns
Clock Pulse Width High Time	13	2.6			3.2			ns
Clock Pulse Width Low Time	14	2.6			3.2			ns
LD* Cycle Time	15	24.24			32			ns
LD* Pulse Width High Time	16	10			13			ns
LD* Pulse Width Low Time	17	10			13			ns
Analog Output Delay	18		12			12		ns
Analog Output Rise/Fall Time	19		2			2		ns
Analog Output Settling Time	20			8			8	ns
Clock and Data Feedthrough*			35			35		pV–sec
Glitch Impulse*			50			50		pV–sec
Analog Output Skew**			0	2		0	2	ns
Pipeline Delay		6		10	6		10	Clocks
VAA Supply Current***	IAA							
Bt451			n/a	n/a		310	400	mA
Bt458			310	370		225	330	mA
Bt457			n/a	n/a		200	250	mA

See test conditions on next page.

AC Characteristics (continued)

		110 MHz Devices			80 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			110			80	MHz
LD* Rate	LDmax			27.5			20	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	15			15			ns
CE* Low Time	3	50			50			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	7			7			ns
CE* Asserted to Data Valid	6			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	3			3			ns
Pixel and Control Setup Time	10	3			4			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	9.09			12.5			ns
Clock Pulse Width High Time	13	4			5			ns
Clock Pulse Width Low Time	14	4			5			ns
LD* Cycle Time	15	36.36			50			ns
LD* Pulse Width High Time	16	15			20			ns
LD* Pulse Width Low Time	17	15			20			ns
Analog Output Delay	18		12			12		ns
Analog Output Rise/Fall Time	19		2			2		ns
Analog Output Settling Time	20			8			8	ns
Clock and Data Feedthrough*			35			35		pV–sec
Glitch Impulse*			50			50		pV–sec
Analog Output Skew**			0	2		0	2	ns
Pipeline Delay		6		10	6		10	Clocks
VAA Supply Current***	IAA							
Bt451			295	385		265	355	mA
Bt458			210	315		200	285	mA
Bt457			190	240		170	220	mA

See test conditions on next page.

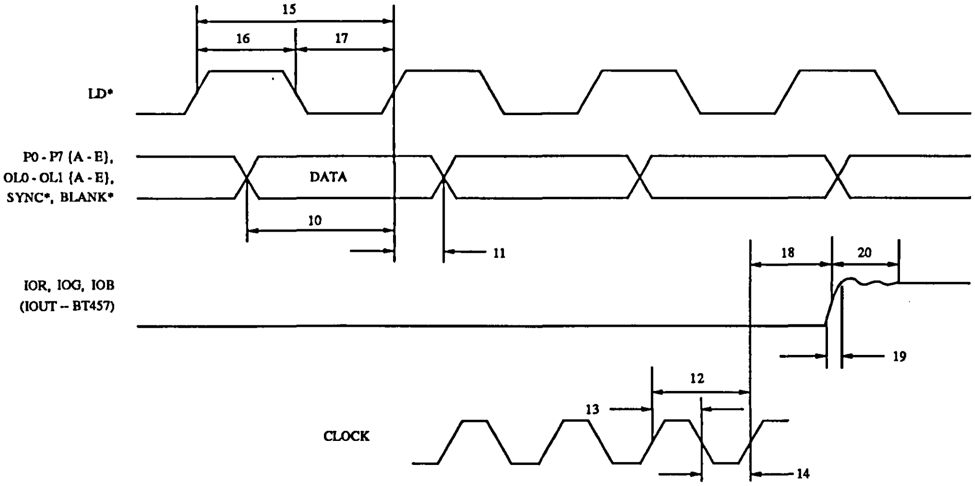
AC Characteristics (continued)

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are VAA–0.8 to VAA–1.8 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 75 pF. See timing notes in Figure 7. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 k-Ω resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**Does not apply to the Bt457.

***At Fmax. IAA (typ) at VAA = 5.0 V, TA = 20° C IAA (max) at VAA = 5.25 V, TA = 0° C



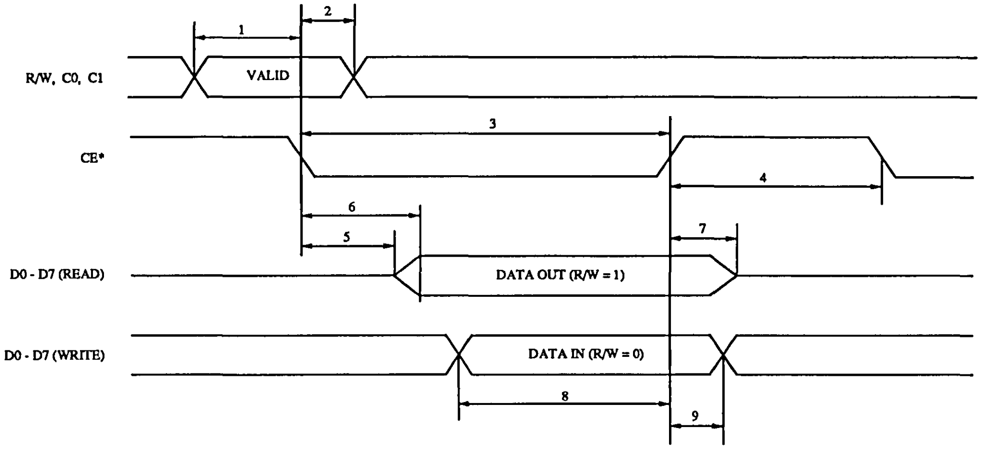
Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full-scale transition.

Note 2: Output settling time measured from 50% point of full-scale transition to output settling within ±1 LSB for the Bt457/458 or ± 1/8LSB for the Bt451.

Note 3: Output rise/fall time measured between 10% and 90% points of full-scale transition.

Figure 7. Video Input/Output Timing.

Timing Waveforms (continued)


1
2
R/W, C0, C1
VALID
3
CE*
4
6
5
7
D0 - D7 (READ)
DATA OUT (R/W = 1)
D0 - D7 (WRITE)
DATA IN (R/W = 0)
8
9

MPU Read/Write Timing.

Ordering Information

Model Number	RAM	DACs	Speed	Package	Ambient Temperature Range
Bt458LG165	256 x 24	triple 8-bit	165 MHz	84-pin Ceramic PGA	0° to +70° C
Bt458KG125	256 x 24	triple 8-bit	125 MHz	84-pin Ceramic PGA	0° to +70° C
Bt458KG110	256 x 24	triple 8-bit	110 MHz	84-pin Ceramic PGA	0° to +70° C
Bt458KG80	256 x 24	triple 8-bit	80 MHz	84-pin Ceramic PGA	0° to +70° C.

Ordering Information (continued)

Model Number	RAM	DACs	Speed	Package	Ambient Temperature Range
Bt458LPJ165	256 x 24	triple 8-bit	165 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt458LPJ125	256 x 24	triple 8-bit	125 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt458LPJ110	256 x 24	triple 8-bit	110 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt458LPJ80	256 x 24	triple 8-bit	80 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt451KG125	256 x 12	triple 4-bit	125 MHz	84-pin Ceramic PGA	0° to +70° C
Bt451KG110	256 x 12	triple 4-bit	110 MHz	84-pin Ceramic PGA	0° to +70° C
Bt451KG80	256 x 12	triple 4-bit	80 MHz	84-pin Ceramic PGA	0° to +70° C
Bt451KPJ125	256 x 12	triple 4-bit	125 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt451KPJ110	256 x 12	triple 4-bit	110 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt451KPJ80	256 x 12	triple 4-bit	80 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt457KG125	256 x 8	single 8-bit	125 MHz	84-pin Ceramic PGA	0° to +70° C
Bt457KG110	256 x 8	single 8-bit	110 MHz	84-pin Ceramic PGA	0° to +70° C
Bt457KG80	256 x 8	single 8-bit	80 MHz	84-pin Ceramic PGA	0° to +70° C
Bt457KPJ125	256 x 8	single 8-bit	125 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt457KPJ110	256 x 8	single 8-bit	110 MHz	84-Pin Plastic J-Lead	0° to +70° C
Bt457KPJ80	256 x 8	single 8-bit	80 MHz	84-Pin Plastic J-Lead	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
I	Expanded PCB layout section, changed AC parameter "CE* asserted to data bus driven" from 10 ns to 7 ns minimum.
J	Revised AC parameter "VAA Supply Current (Max)" for the Bt457: 80 MHz changed from 190 mA to 220 mA, 110 MHz changed from 210 mA to 240 mA and 125 MHz changed from 220 mA to 250 mA.
K	Changed speed grade from 170 MHz to 165 MHz, changed PLL feedback circuitry, consolidated Bt458 power specs. Changed AC Characteristics CLOCK, Load Cycle, and Pulse Width times, changed typical analog output delay times.

Bt453

Distinguishing Features

- 66, 40 MHz Operation
- Triple 8-bit D/A Converters
- 256 x 24 Color Palette RAM
- 3 x 24 Overlay Palette
- RS-343A/RS-170-Compatible Outputs
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 40-pin DIP or 44-pin PLCC Package
- Typical Power Dissipation: 1 W

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Related Products

- Bt477, Bt478

66 MHz
Monolithic CMOS
256 x 24 Color Palette
RAMDAC™

Product Description

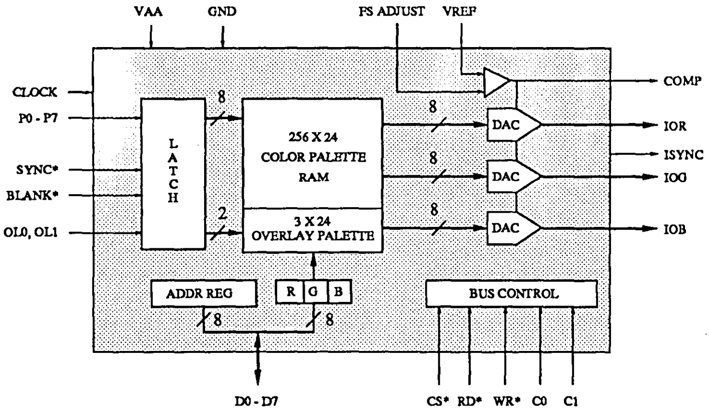
The Bt453 RAMDAC is designed specifically for high-resolution color graphics.

The Bt453 has a 256 x 24 color lookup table with triple 8-bit video D/A converters, supporting up to 259 simultaneous colors from a 16.8 million color palette. Three overlay registers provide for overlaying cursors, grids, menus, etc. The MPU bus operates asynchronously to the video data, simplifying the design interface to the system.

The Bt453 generates RS-343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering.

Both the differential and linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

Functional Block Diagram


VAA
GND
FS ADJUST
VREF
CLOCK
P0 - P7
SYNC*
BLANK*
OL0, OL1
LATCH
8
2
256 X 24
COLOR PALETTE
RAM
3 X 24
OVERLAY PALETTE
8
8
8
DAC
DAC
DAC
COMP
IOR
ISYNC
IOG
IOB
ADDR REG
R
G
B
BUS CONTROL
8
8
D0 - D7
CS*
RD*
WR*
C0
C1

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L453001 Rev. I

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt453 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers. The MPU interface operates asynchronously to the video data, simplifying the design interface.

The C0 and C1 control inputs specify whether the MPU is accessing the address register, color palette RAM, or the overlay registers, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location, which the MPU may read by simply reading another sequence of red, green, and blue data.

Note that any time the CS* input is a logical zero, the video outputs are forced to the black level. When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the six most significant bits of the address register (ADDR2–7) are ignored.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR0–7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 2.

Figure 1 illustrates the MPU read/write timing.

C1	C0	Addressed by MPU
0	0	address register
0	1	color palette RAM
1	0	address register
1	1	overlay registers

Table 1. Control Input Truth Table.

Circuit Description (continued)

	Value	C1	C0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10	x x x	1 1 1	red value green value blue value
ADDR0–7 (counts binary)	$00 - $FF xxxx xx00 xxxx xx01 xxxx xx10 xxxx xx11	0 1 1 1 1	1 1 1 1 1	color palette RAM reserved overlay color 1 overlay color 2 overlay color 3

Table 2. Address Register (ADDR) Operation.

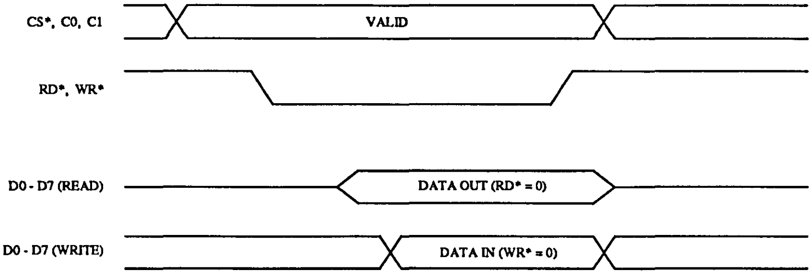

CS*, C0, C1
VALID
RD*, WR*
D0 - D7 (READ)
DATA OUT (RD* = 0)
D0 - D7 (WRITE)
DATA IN (WR* = 0)

Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

While CS* is a logical one, the P0–P7, OL0, and OL1 inputs are used to address the color palette RAM and overlay registers, as shown in Table 3. The addressed location provides 24 bits of color information to the three D/A converters. (See Figure 2 for timing information.)

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 3. Table 4 details how the SYNC* and BLANK* inputs modify the output levels.

The analog outputs of the Bt453 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

OL1	OL0	P0 - P7	Addressed by frame buffer
0	0	$00	color palette RAM location $00
0	0	$01	color palette RAM location $01
:	:	:	:
0	0	$FF	color palette RAM location $FF
0	1	$xx	overlay color 1
1	0	$xx	overlay color 2
1	1	$xx	overlay color 3

Table 3. Pixel and Overlay Control Truth Table.

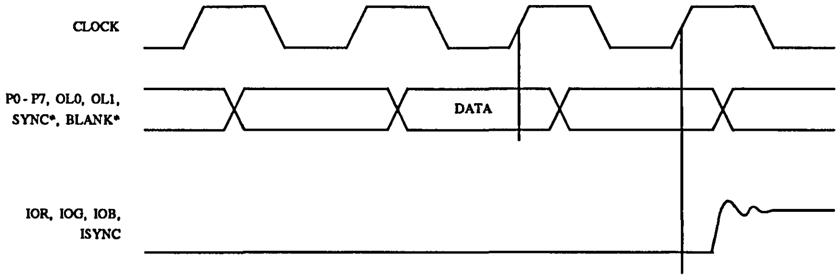
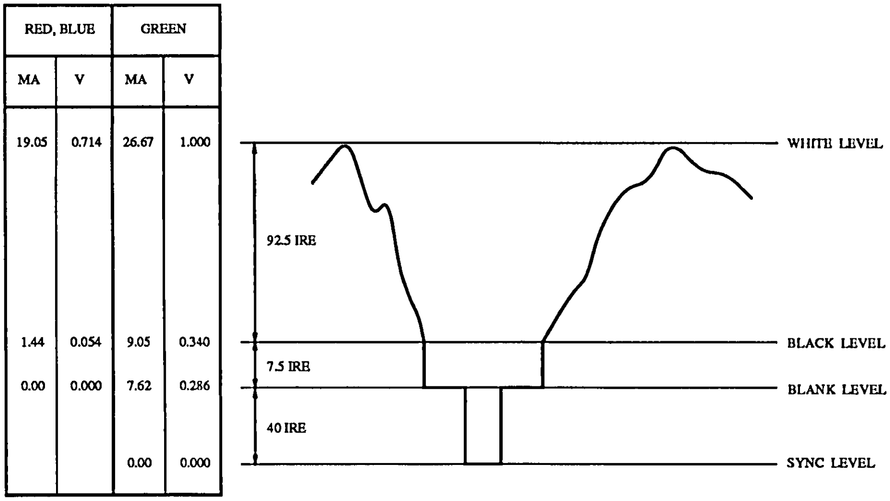


Figure 2. Video Input/Output Timing.

Circuit Description (continued)



RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

Note: 75 Ω doubly terminated load, RSET = 280 Ω, VREF = 1.235 V. ISYNC connected to IOG. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 280 Ω, VREF = 1.235 V. ISYNC connected to IOG.

Table 4. Video Output Truth Table.

Pin Descriptions

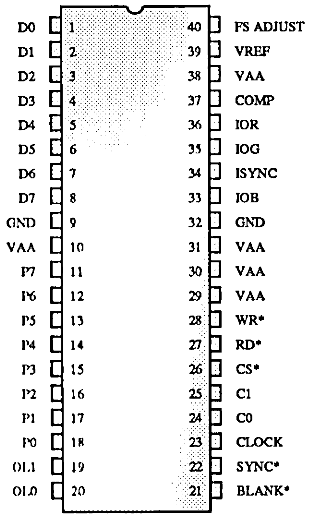
Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the IOR, IOG, and IOB outputs to the blanking level, as illustrated in Table 4. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the ISYNC output (see Figure 3). SYNC* does not override any other control or data input, as shown in Table 4; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0, OL1, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0, OL1	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 3. When accessing the overlay palette, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 4). All outputs, whether used or not, should have the same output load.
ISYNC	Sync current output. This high-impedance current source is typically connected directly to the IOG output (Figure 4), and is used to encode sync information onto the green channel. ISYNC does not output any current while SYNC* is a logical zero. The amount of current output while SYNC* is a logical one is: $\text{ISYNC (mA)} = 1{,}728 * \text{VREF (V)} / \text{RSET } (\Omega)$ If sync information is not required on the green channel, this output should be connected to GND.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 4). Note that the IRE relationships in Figure 3 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is (assuming ISYNC is connected to IOG): $\text{RSET } (\Omega) = 6{,}047 * \text{VREF (V)} / \text{IOG (mA)}$ The relationship between RSET and the full-scale output current on IOR and IOB is: $\text{IOR, IOB (mA)} = 4{,}319 * \text{VREF (V)} / \text{RSET } (\Omega)$

Pin Descriptions (continued)

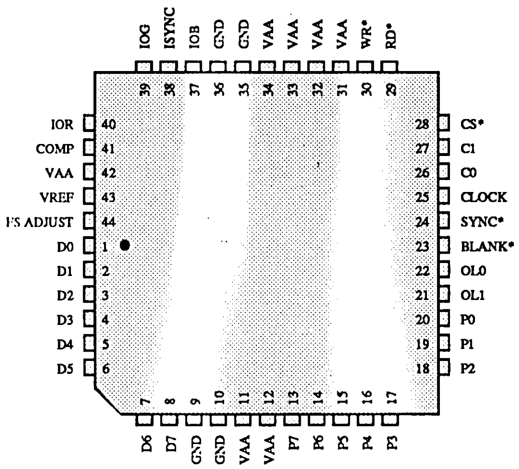
Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 4). The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *Refer to PC Board Layout Considerations for critical layout criteria.*
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 4, must supply this input with a 1.2 V (typical) reference. The Bt453 has an internal pull-up resistor between VREF and VAA. As the value of this resistor may vary slightly due to process variations, the use of a resistor divider network to generate the reference voltage is not recommended. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 4. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.
CS*	Chip select control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. While CS* is a logical zero, the IOR, IOG, and IOB outputs are forced to the black level. Note that the Bt453 will not function correctly while CS*, RD*, and WR* are simultaneously a logical zero.
WR*	Write control input (TTL compatible). To write data to the device, both CS* and WR* must be a logical zero. Data is latched on the rising edge of WR* or CS*, whichever occurs first. See Figure 1.
RD*	Read control input (TTL compatible). To read data from the device, both CS* and RD* must be a logical zero. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8 bit bidirectional data bus. D0 is the least significant bit.

Pin Descriptions (continued)

40-pin DIP Package


D0 1
D1 2
D2 3
D3 4
D4 5
D5 6
D6 7
D7 8
GND 9
VAA 10
P7 11
P6 12
P5 13
P4 14
P3 15
P2 16
P1 17
P0 18
OL1 19
OL0 20
40 FS ADJUST
39 VREF
38 VAA
37 COMP
36 IOR
35 IOG
34 ISYNC
33 IOB
32 GND
31 VAA
30 VAA
29 VAA
28 WR*
27 RD*
26 CS*
25 C1
24 C0
23 CLOCK
22 SYNC*
21 BLANK*

44-pin Plastic J-Lead (PLCC)
Package


IOG 39
ISYNC 38
IOB 37
GND 36
GND 35
VAA 34
VAA 33
VAA 32
VAA 31
WR* 30
RD* 29
IOR 40
COMP 41
VAA 42
VREF 43
FS ADJUST 44
D0 1
D1 2
D2 3
D3 4
D4 5
D5 6
28 CS*
27 C1
26 C0
25 CLOCK
24 SYNC*
23 BLANK*
22 OL0
21 OL1
20 P0
19 P1
18 P2
7 D6
8 D7
9 GND
10 GND
11 VAA
12 VAA
13 P7
14 P6
15 P5
16 P4
17 P3

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in *Bt451/7/8 Evaluation Module Operation and Measurements,* application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt453 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a 4-layer PC board is recommended with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

The optimum layout enables the Bt453 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8 inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground tub isolation technique is constrained by the noise margin degradation during digital readback of the Bt453.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

The analog ground plane should include all Bt453 ground pins, all reference circuitry and decoupling (external reference, RSET resistors, etc.), power supply bypass circuitry for the Bt453, analog output traces, and the video output connector.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt453 power pins, any reference circuitry, and COMP and reference decoupling. There should be at least a 1/8 inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 4. This bead should be located within 3 inches of the Bt453 and provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 μF ceramic capacitor decoupling each of the three groups of VAA pins to GND. The capacitors should be placed as close as possible to the device.

The 10 μF capacitor is for low-frequency power supply ripple; the 0.1 μF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% ofpower supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 μF ceramic chip capacitor. Low-frequency supply noise will require a larger value. Lead lengths should be minimized for best performance.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt453 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit by using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 ohms).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 ohms) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt453 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt453 to minimize reflections. Unused analog outputs should be connected to GND.

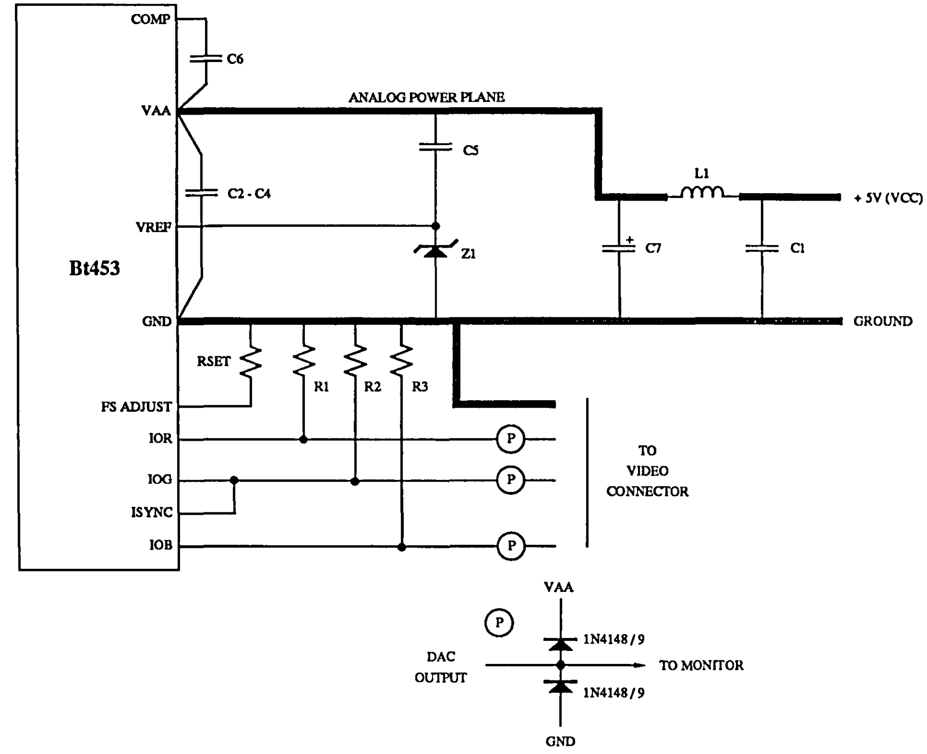
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

Analog Output Protection

The Bt453 analog outputs should be protected against high energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 4 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)


COMP
C6
VAA
ANALOG POWER PLANE
C5
L1
+ 5V (VCC)
C2 - C4
VREF
Z1
+
C7
C1
Bt453
GND
GROUND
RSET
R1
R2
R3
FS ADJUST
IOR
IOG
ISYNC
IOB
P
P
P
TO
VIDEO
CONNECTOR
VAA
P
1N4148/9
DAC
OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description	Vendor Part Number
C1–C6	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C7	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	280 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt453.

Figure 4. Typical Connection Diagram and Parts List.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.14	1.235	1.26	Volts
FS ADJUST Resistor	RSET		280		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
Digital Outputs					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current	IOZ			10	µA
Output Capacitance	CDOUT		20		pF
Analog Outputs					
Gray Scale Current Range		15		22	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching (25–70° C.)			2	5	%
Output Compliance	VOC	–1.0		+1.4	Volts
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		30		pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.12	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 280 Ω, VREF = 1.235 V, ISYNC connected to IOG. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	66 MHz Devices Min	66 MHz Devices Typ	66 MHz Devices Max	40 MHz Devices Min	40 MHz Devices Typ	40 MHz Devices Max	Units
Clock Rate	Fmax			66			40	MHz
CS*, C0, C1 Setup Time	1	35			35			ns
CS*, C0, C1 Hold Time	2	35			35			ns
RD*, WR* High Time	3	25			25			ns
RD* Asserted to Data Bus Driven	4	5			5			ns
RD* Asserted to Data Valid	5			100			100	ns
RD* Negated to Data Bus 3-Stated	6			15			15	ns
WR* Low Time	7	50			50			ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	5			5			ns
Pixel and Control Setup Time	10	5			7			ns
Pixel and Control Hold Time	11	2			3			ns
Clock Cycle Time	12	15			25			ns
Clock Pulse Width High Time	13	5			7			ns
Clock Pulse Width Low Time	14	5			7			ns
Analog Output Delay	15		20	30		20	30	ns
Analog Output Rise/Fall Time	16		3			3		ns
Analog Output Settling Time*	17		25			25		ns
Clock and Data Feedthrough*			–48			–48		dB
Glitch Impulse*			50			50		pV–sec
DAC-to-DAC Crosstalk			–22			–22		dB
Analog Output Skew			1	2		1	2	ns
Pipeline Delay	18	2	2	2	2	2	2	Clocks
VAA Supply Current**	IAA		220	275		190	250	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 280 ohms, VREF = 1.235 V, ISYNC connected to IOG. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 75 pF. See timing notes in Figure 6. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

Timing Waveforms

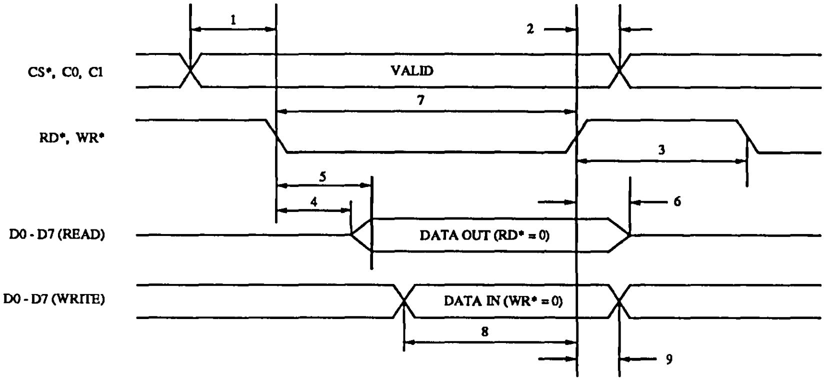
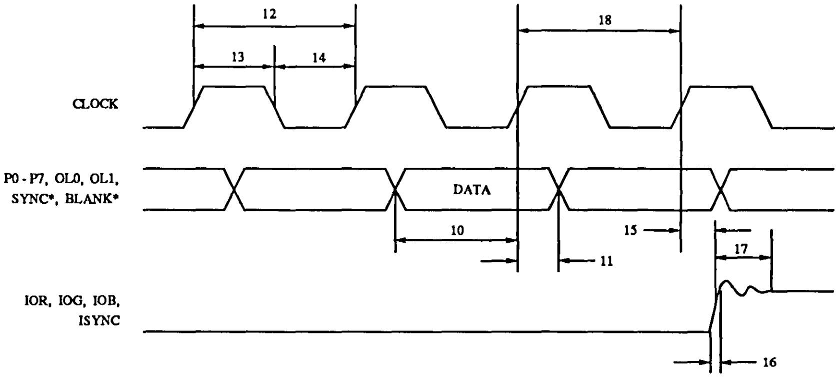

CS*, C0, C1
VALID
RD*, WR*
D0 - D7 (READ)
DATA OUT (RD* = 0)
D0 - D7 (WRITE)
DATA IN (WR* = 0)
1
2
3
4
5
6
7
8
9

Figure 5. MPU Read/Write Timing Dimensions.


CLOCK
P0 - P7, OL0, OL1, SYNC*, BLANK*
DATA
IOR, IOG, IOB, ISYNC
12
13
14
18
10
11
15
16
17

Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.

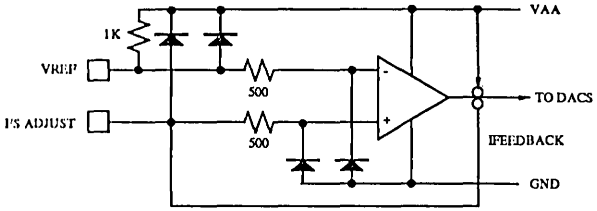
Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 6. Video Input/Output Timing.

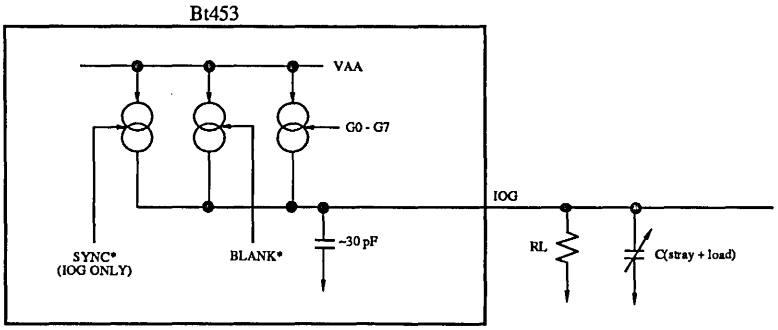
Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt453KP66	66 MHz	40-pin 0.6" Plastic DIP	0° to +70° C
Bt453KPJ66	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt453KC66	66 MHz	40-pin 0.6" CERDIP	0° to +70° C
Bt453KC	40 MHz	40-pin 0.6" CERDIP	0° to +70° C
Bt453KP	40 MHz	40-pin 0.6" Plastic DIP	0° to +70° C
Bt453KPJ	40 MHz	44-pin Plastic J-Lead	0° to +70° C

Device Circuit Data


VAA
1K
VREF
500
FS ADJUST
500
TO DACS
IFEEDBACK
GND
-
+

Equivalent Circuit of the Reference Amplifier.


Bt453
VAA
G0 - G7
IOG
~30 pF
RL
C(stray + load)
SYNC*
(IOG ONLY)
BLANK*

Equivalent Circuit of the Current Output (IOG).

Revision History

Datasheet Revision	*Change from Previous Revision*
H	Expanded PCB layout section.
I	Added ESD/latchup information. Expanded PCB Layout section.

Bt453/883

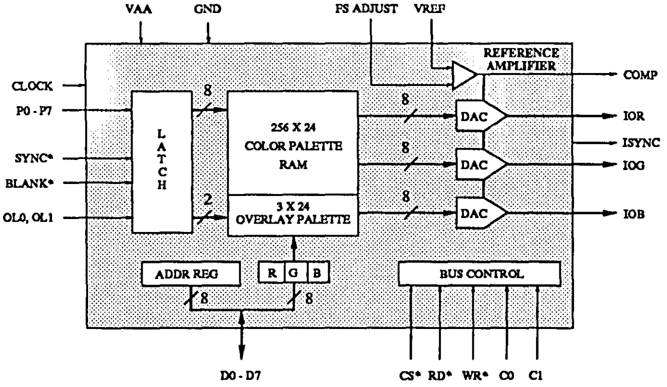
Distinguishing Features

- 40 MHz Pipelined Operation
- Triple 8-bit D/A Converters
- 256 x 24 Color Palette RAM
- 3 x 24 Overlay Palette
- RS-343A/RS-170-Compatible Outputs
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 40-pin Ceramic Sidebraze DIP Package
- Typical Power Dissipation: 950 mW

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Functional Block Diagram


VAA
GND
FS ADJUST
VREF
REFERENCE AMPLIFIER
COMP
CLOCK
P0 - P7
SYNC*
BLANK*
OL0, OL1
L A T C H
8
256 X 24 COLOR PALETTE RAM
2
3 X 24 OVERLAY PALETTE
8
DAC
IOR
ISYNC
IOG
IOB
ADDR REG
R G B
8
BUS CONTROL
D0 - D7
CS* RD* WR* C0 C1

MIL-STD-883C, Class B
Monolithic CMOS
256 x 24 Color Palette
40 MHz RAMDAC™

Product Description

The Bt453/883 RAMDAC is designed specifically for high-resolution color graphics.

It has a 256 x 24 color lookup table with triple 8-bit video D/A converters, supporting up to 259 simultaneous colors from a 16.8 million color palette. Three overlay registers provide for overlaying cursors, grids, menus, etc. The MPU bus operates asynchronously to the video data, simplifying the design interface to the system.

The Bt453/883 generates RS-343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering. Both the differential and linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L453M01 Rev. F

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt453/883 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers. The MPU interface operates asynchronously to the video data, simplifying the design interface.

The C0 and C1 control inputs specify whether the MPU is accessing the address register, color palette RAM, or the overlay registers, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. During the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location which the MPU may read by simply reading another sequence of red, green, and blue data.

Note that any time the CS* input is a logical zero, the video outputs are forced to the black level. When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the six most significant bits of the address register (ADDR2–7) are ignored.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR0–7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 2.

Figure 1 illustrates the MPU read/write timing.

C1	C0	Addressed by MPU
0	0	address register
0	1	color palette RAM
1	0	address register
1	1	overlay registers

Table 1. Control Input Truth Table.

Circuit Description (continued)

	Value	C1	C0	Addressed by MPU
ADDRa, b (counts modulo 3)	00	x	1	red value
	01	x	1	green value
	10	x	1	blue value
ADDR0–7 (counts binary)	$00 - $FF	0	1	color palette RAM
	xxxx xx00	1	1	reserved
	xxxx xx01	1	1	overlay color 1
	xxxx xx10	1	1	overlay color 2
	xxxx xx11	1	1	overlay color 3

Table 2. Address Register (ADDR) Operation.

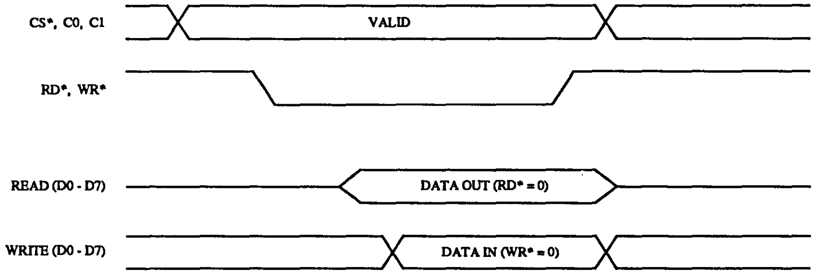

CS*, C0, C1
VALID
RD*, WR*
READ (D0 - D7)
DATA OUT (RD* = 0)
WRITE (D0 - D7)
DATA IN (WR* = 0)

Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

While CS* is a logical one, the P0–P7, OL0, and OL1 inputs are used to address the color palette RAM and overlay registers, as shown in Table 3. The addressed location provides 24 bits of color information to the three D/A converters. (See Figure 2.)

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 3. Table 4 details how the SYNC* and BLANK* inputs modify the output levels.

The analog outputs of the Bt453/883 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

OL1	OL0	P0–P7	Addressed by frame buffer
0	0	$00	color palette RAM location $00
0	0	$01	color palette RAM location $01
:	:	:	:
0	0	$FF	color palette RAM location $FF
0	1	$xx	overlay color 1
1	0	$xx	overlay color 2
1	1	$xx	overlay color 3

Table 3. Pixel and Overlay Control Truth Table.

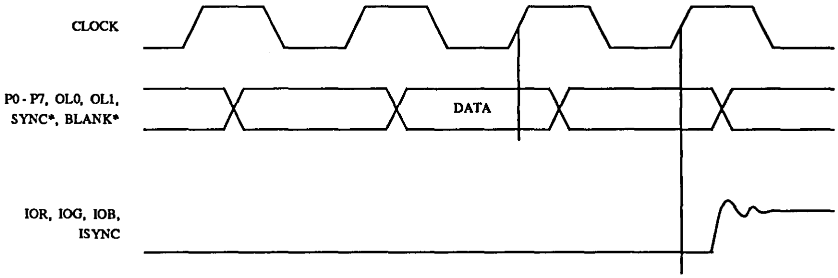
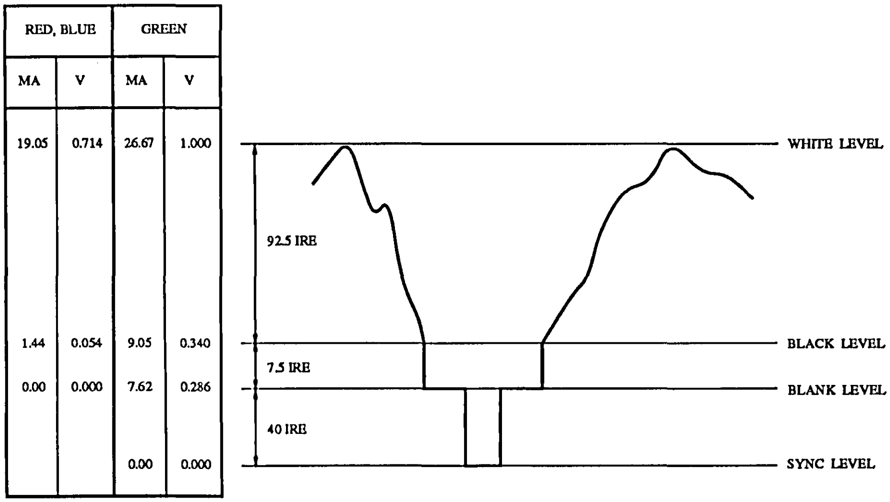


Figure 2. Video Input/Output Timing.

Circuit Description (continued)


RED, BLUE
GREEN
MA
V
MA
V
19.05
0.714
26.67
1.000
1.44
0.054
9.05
0.340
0.00
0.000
7.62
0.286
0.00
0.000
WHITE LEVEL
92.5 IRE
BLACK LEVEL
7.5 IRE
BLANK LEVEL
40 IRE
SYNC LEVEL

Note: 75 Ω doubly terminated load, RSET = 280 Ω, VREF = 1.235 V. ISYNC connected to IOG. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 280 Ω, VREF = 1.235 V ISYNC connected to IOG.

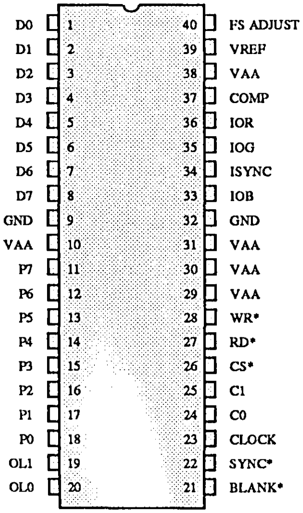
Table 4. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the IOR, IOG, and IOB outputs to the blanking level, as illustrated in Table 4. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the ISYNC output (see Figure 3). SYNC* does not override any other control or data input, as shown in Table 4; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0, OL1, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0, OL1	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 3. When accessing the overlay palette, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 4). All outputs, whether used or not, should have the same output load.
ISYNC	Sync current output. This high-impedance current source is typically connected directly to the IOG output (Figure 4), and is used to encode sync information onto the green channel. ISYNC does not output any current while SYNC* is a logical zero. The amount of current output while SYNC* is a logical one is: ISYNC (mA) = 1,728 * VREF (V) / RSET (Ω) If sync information is not required on the green channel, this output should be connected to GND.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 4). Note that the IRE relationships in Figure 3 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is (assuming ISYNC is connected to IOG): RSET (Ω) = 6,047 * VREF (V) / IOG (mA) The relationship between RSET and the full-scale output current on IOR and IOB is: IOR, IOB (mA) = 4,319 * VREF (V) / RSET (Ω)

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 4). The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *Refer to PC Board Layout Considerations for critical layout criteria.*
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 4, must supply this input with a 1.2 V (typical) reference. The Bt453/883 has an internal pull-up resistor between VREF and VAA. As the value of this resistor may vary slightly due to process variations, the use of a resistor divider network to generate the reference voltage is not recommended. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 4. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.
CS*	Chip select control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. While CS* is a logical zero, the IOR, IOG, and IOB outputs are forced to the black level. Note that the Bt453/883 will not function correctly while CS*, RD*, and WR* are simultaneously a logical zero.
WR*	Write control input (TTL compatible). To write data to the device, both CS* and WR* must be a logical zero. Data is latched on the rising edge of WR* or CS*, whichever occurs first. See Figure 1.
RD*	Read control input (TTL compatible). To read data from the device, both CS* and RD* must be a logical zero. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Tables 1 and 2.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.



PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in *Bt451/7/8 Evaluation Module Operation and Measurements,* application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt453/883 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a 4-layer PC board is recommended with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

The optimum layout enables the Bt453/883 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8 inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground tub isolation technique is constrained by the noise margin degradation during digital readback of the Bt453/883.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

The analog ground plane should include all Bt453/883/883 ground pins, all reference circuitry and decoupling (external reference, RSET resistors, etc.), power supply bypass circuitry for the Bt453, analog output traces, and the video output connector.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt453 power pins, any reference circuitry, and COMP and reference decoupling. There should be at least a 1/8 inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 4. This bead should be located within 3 inches of the Bt453/883 and provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the three groups of VAA pins to GND. The capacitors should be placed as close as possible to the device.

The 10 µF capacitor is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

PC Board Layout Considerations (continued)

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic chip capacitor. Low-frequency supply noise will require a larger value. Lead lengths should be minimized for best performance so that the self-resonance frequency is greater than the LD* frequency.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt453/883 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit by using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt453/883 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt453/883 to minimize reflections. Unused analog outputs should be connected to GND.

Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

Analog Output Protection

The Bt453/883 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 4 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

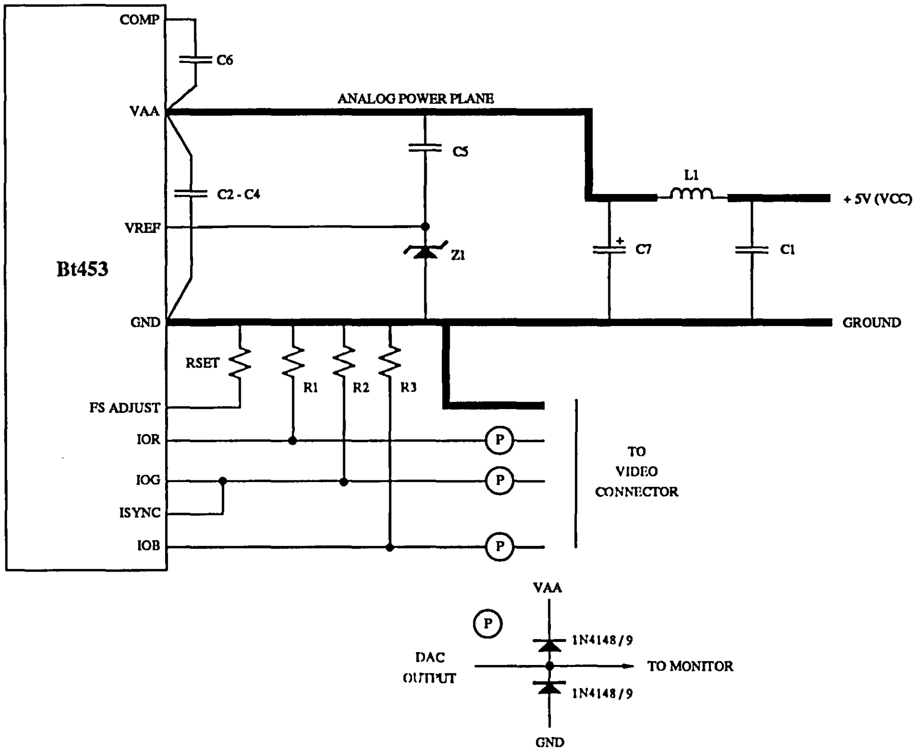
ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

PC Board Layout Considerations (continued)


COMP
C6
VAA
ANALOG POWER PLANE
C5
C2 - C4
L1
+5V (VCC)
VREF
Z1
C7
C1
Bt453
GND
GROUND
RSET
R1
R2
R3
FS ADJUST
IOR
IOG
ISYNC
IOB
P
TO VIDEO CONNECTOR
VAA
1N4148/9
DAC OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description
C1–C6	0.1 µF ceramic capacitor
C7	10 µF tantalum capacitor
L1	ferrite bead
R1, R2, R3	75 Ω 1% metal film resistor
RSET	280 Ω 1% metal film resistor
Z1	1.2 V voltage reference

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt453/883.

Figure 4. Typical Connection Diagram and Parts List.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.5	5.0	5.5	Volts
Ambient Operating Temperature	TA	-55		+125	°C
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.14	1.235	1.26	Volts
FS ADJUST Resistor	RSET		280		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on Any Digital Pin		GND-0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
θ JC				18	°C/W
θ JA				28	°C/W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH				
CLOCK		2.4			Volts
Other		2.0			Volts
Input Low Voltage	VIL			0.8	Volts
Input High Current (Vin = VAA)	IIH			1	µA
Input Low Current (Vin = 0 V)	IIL			–1	µA
Input Capacitance**	CIN			10	pF
Digital Outputs					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current	IOZ			10	µA
Output Capacitance**	CDOUT			30	pF
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		–10	1	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		–10	1	50	µA
LSB Size***		65.7	69.1	72.6	µA
DAC-to-DAC Matching			3.5	7	%
Output Compliance	VOC	–1.0		+1.4	Volts
Output Capacitance**	CAOUT			30	pF

Test conditions (unless otherwise specified): 100% tested at VAA = 4.5 V and 5.5 V, TA = -55°, +25°, and +125° C. RSET = 280 ± 0.1% Ω, VREF = 1.235 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

**Derived from characterization (TA = 25° C, VAA = 5 V ± 10%), not tested. These parameters are controlled via design or process parameters and are not directly tested. They are characterized upon initial design release and upon design changes which would affect them.

***Computed by the formula: (White Level Relative to Black) / 255.

AC Characteristics

Parameter	Symbol	–55° to +125° C. Min	–55° to +125° C. Max	Units
Clock Rate	Fmax		40	MHz
CS*, C0, C1 Setup Time	1	35		ns
CS*, C0, C1 Hold Time	2	35		ns
RD*, WR* High Time	3	25		ns
RD* Asserted to Data Bus Driven	4	2		ns
RD* Asserted to Data Valid	5		100	ns
RD* Negated to Data Bus 3-Stated	6		15	ns
WR* Low Time	7	50		ns
Write Data Setup Time	8	35		ns
Write Data Hold Time	9	5		ns
Pixel and Control Setup Time	10	7		ns
Pixel and Control Hold Time	11	3		ns
Clock Cycle Time	12	25		ns
Clock Pulse Width High	13	7		ns
Clock Pulse Width Low	14	7		ns
Analog Output Rise/Fall Time**	15		8	ns
VAA Supply Current***	IAA		300	mA

Test conditions (unless otherwise specified): 100% testing at VAA = 4.5 V and 5.5 V with TA = –55°, 25°, and 125° C. RSET = 280 Ω ± 0.1%, VREF = 1.235 V. Input values are 0.8–2.4 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Analog output load with doubly terminated 50 Ω line. D0–D7 output load ~ 75 pF. See timing notes in Figure 6. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

**Derived from characterization (TA = 25° C. VAA = 5 V ± 10%), not tested. These parameters are controlled via design or process parameters and are not directly tested. They are characterized upon initial design release and upon design changes which would affect them.

*** IAA (max) is measured at Fmax, with VAA = 5.5 V and is 100% tested at TA = 25° C.

Timing Waveforms

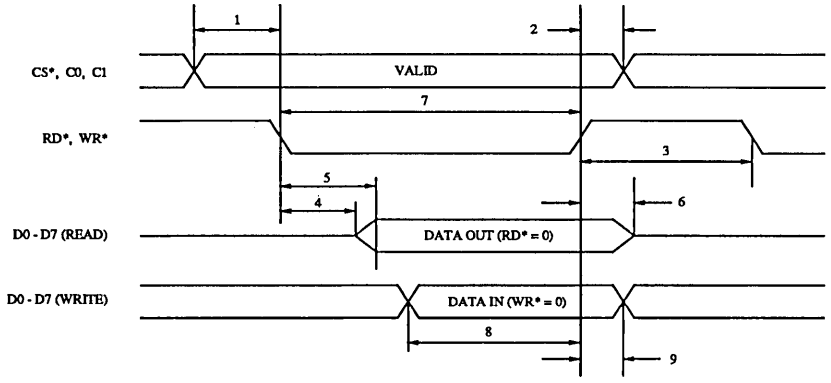
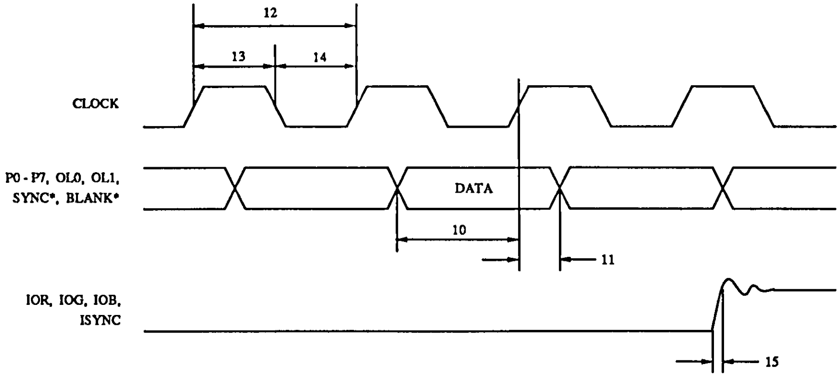

CS*, C0, C1
RD*, WR*
D0 - D7 (READ)
D0 - D7 (WRITE)
VALID
DATA OUT (RD* = 0)
DATA IN (WR* = 0)
1
2
3
4
5
6
7
8
9

Figure 5. MPU Read/Write Timing Dimensions.


CLOCK
P0 - P7, OL0, OL1,
SYNC*, BLANK*
IOR, IOG, IOB,
ISYNC
DATA
10
11
12
13
14
15

Note 1: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB for data only.

Note 2: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 6. Video Input/Output Timing.

Ordering Information

Model Number	MTBF* (hours)	Package	Ambient Temperature Range
Bt453SC883	0.54×10^6	40-pin 0.6" Ceramic Sidebraze DIP	–55° to +125° C.

*MTBF is calculated per MIL Handbook 217.

Bt454
Bt455

170 MHz
Monolithic CMOS
16 Color Palette
RAMDAC™

istinguishing Features

170, 135, 110 MHz Operation
4:1 Multiplexed TTL Pixel Ports
Triple 4-bit D/A Converters
16 Word Dual Port Color Palette
1 Dual Port Overlay Palette
RS-343A-Compatible Outputs
Standard MPU Interface
+5 V CMOS Monolithic Construction
44-pin PLCC Package
Typical Power Dissipation: 1 W

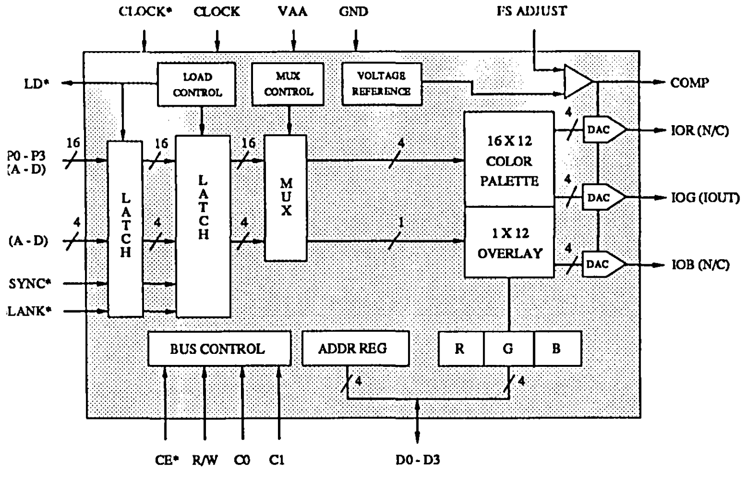
Applications

- High Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction
- Desktop Publishing

Related Products

- Bt451, Bt457, Bt458, Bt459 Bt460, Bt468

unctional Block Diagram


CLOCK*
CLOCK
VAA
GND
FS ADJUST
LD*
LOAD CONTROL
MUX CONTROL
VOLTAGE REFERENCE
COMP
P0 - P3
(A - D)
16
16
16
LATCH
LATCH
MUX
4
4
4
4
4
1
(A - D)
16 X 12 COLOR PALETTE
1 X 12 OVERLAY
DAC
DAC
DAC
IOR (N/C)
IOG (IOUT)
IOB (N/C)
SYNC*
LANK*
BUS CONTROL
ADDR REG
R
G
B
4
4
CE*
R/W
C0
C1
D0 - D3

Product Description

The Bt454 and Bt455 are pin-compatible and software-compatible RAMDACs designed specifically for high-performance, high-resolution color graphics. The architecture enables the display of 1600 x 1200 bit-mapped color graphics (up to 4 bits per pixel plus 1 bit of overlay information), minimizing the use of costly ECL interfacing, as most of the high-speed (pixel clock) logic is contained on chip. The multiple pixel ports and internal multiplexing enables TTL-compatible interfacing (up to 42.5 MHz) to the frame buffer, while maintaining the 170-MHz video data rates required for sophisticated color graphics.

The Bt454 is a triple 4-bit video RAMDAC, and supports up to 17 simultaneous colors from a 4096 color palette. On-chip features include a temperature-compensated precision voltage reference, divide-by-four of the clock for load generation, color overlay capability, and a dual-port color palette RAM.

The Bt455 is a single-channel version of the Bt454, well-suited for high-performance monochrome or gray-scale applications.

The Bt454/455 generates RS-343A-compatible video signals, and is capable of driving doubly terminated 75 Ω coax directly, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1/4 LSB over the full temperature range.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L454001 Rev. I

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt454/455 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and overlay register allow color updating without contention with the display refresh process.

As shown in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which color palette RAM entry or overlay register will be accessed by the MPU. The address register is used to address the internal RAM, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

To write color data to the color palette RAM, the MPU loads the address register with the desired RAM location to be modified. The MPU performs three successive write cycles (4 bits each of red, green, and blue), using C0 and C1 to select the color palette RAM. Following the blue write cycle, the address register increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read color data from the color palette RAM, the MPU loads the address register with the desired RAM location to be read. The MPU performs three successive read cycles (4 bits each of red, green, and blue), using C0 and C1 to select the color palette RAM. Following the blue read cycle, the address register increments to the next location, which the MPU may read by simply reading another sequence of red, green, and blue data.

When accessing the color palette RAM, the address register resets to $0 following the blue read or write cycle to location $F.

To read from or write to the overlay register, the MPU, using C0 and C1 to select the overlay register, performs three successive read or write cycles (4 bits each of red, green, and blue). ADDR0–3 are not used.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 1. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 4 bits of the address register (ADDR0–3) are accessible to the MPU, and are used to address the color palette RAM locations.

Although the Bt455 uses only the green channel, it must still go through the count modulo 3 write sequence. The values loaded into the red and blue color palette should be $0.

When reading or writing the color values, the RAM or overlay register is accessed each time a 4-bit color value is read or written.

Although the color palette RAM and overlay register are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU, it is possible for one or more of the pixels on the display screen to be disturbed.

Figure 1 illustrates the MPU read/write timing when accessing the device.

Circuit Description (continued)

	Value	C1	C0	CE*	R/W	Addressed by MPU
ADDRa, b (counts modulo 3)	00		1			red value
	01		1			green value
	10		1			blue value
ADDR0–3 (counts binary)	$x	0	0	0	0	write to address register
	$0–$F	0	1	0	0	write to color palette RAM
	$x	1	0	0	0	D0–D3 ignored, 0 --> ADDRa, b
	$x	1	1	0	0	write to overlay register
	$x	0	0	0	1	read address register
	$0–$F	0	1	0	1	read color palette RAM
	$x	1	0	0	1	0 --> D0–D3, 0 --> ADDRa, b
	$x	1	1	0	1	read overlay register
	$x	x	x	1	x	3-state D0–D3

Table 1. Address Register (ADDR) Operation.

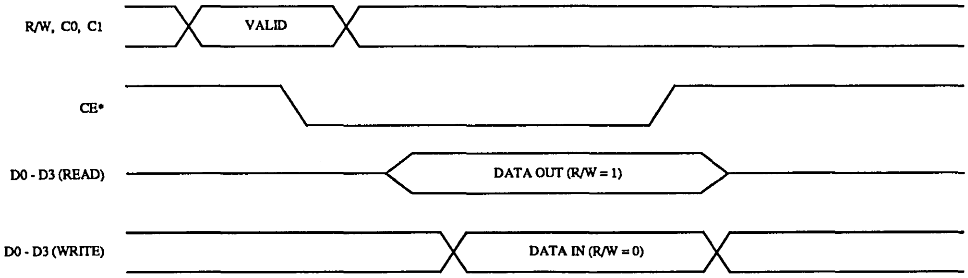

R/W, C0, C1
VALID
CE*
D0 - D3 (READ)
DATA OUT (R/W = 1)
D0 - D3 (WRITE)
DATA IN (R/W = 0)

Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at reasonable data rates (up to 42.5 MHz), the Bt454/455 incorporates internal latches and multiplexers. As illustrated in Figure 2, the SYNC*, BLANK*, P0–P3 {A–D}, and OL {A–D} inputs are latched on the rising edge of LDOUT. Note that with this configuration, the sync and blank timing will be recognized only with four pixel resolution. Typically, the LDOUT signal is used to clock external circuitry to generate the basic video timing and to clock the video DRAMs of the frame buffer.

The overlay inputs may have pixel timing, facilitating the use of an additional bit plane in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external character or cursor generation logic.

The Bt454/455 generates the LDOUT signal internally by dividing the clock by four. LDOUT is the setup-and-hold time reference for the pixel, overlay, sync, and blank inputs. It is recommended that LDOUT be buffered to clock the shift registers of the video DRAMs.

Once the pixel and overlay data are latched by LDOUT, they are internally multiplexed at the pixel clock rate. On each clock cycle, the Bt454/455 outputs color information based on the {A} inputs, followed by the {B} inputs, etc., until all four pixels have been output, at which point the cycle repeats.

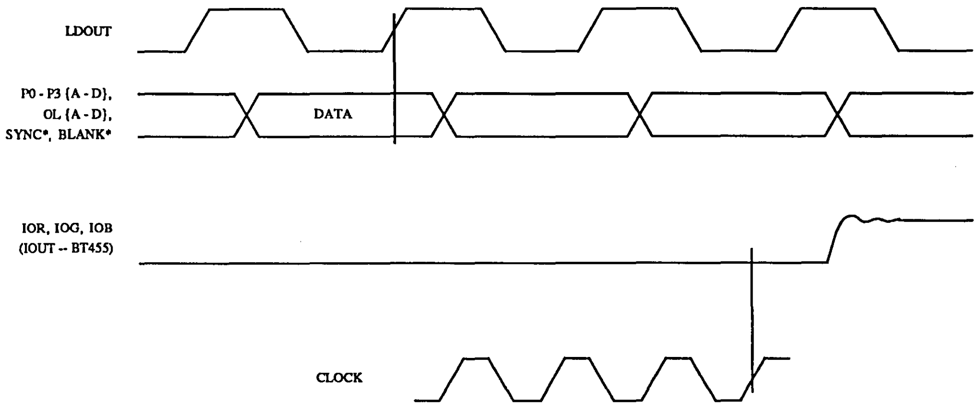


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Video Generation

Each clock cycle, 4bits of color information (P0–P3) and 1 bit of overlay information (OL) for each pixel are used to determine whether a color palette entry in the RAM or whether the overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAM. Table 2 illustrates the truth table used for color selection.

Every clock cycle, the selected information is presented to the three 4-bit D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 3.

The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Note that only the green output (IOG) on the Bt454 contains sync information. Table 3 details how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt454/455 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current-steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

CRT Monitor Interface

The analog outputs are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable, when soldered directly to a PC board. When the device is socketed, it is recommended that only a singly terminated 75 Ω load be used (unless air flow or heat sinking are available). Note that when driving a singly terminated 75 Ω load, the RSET value must be adjusted.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

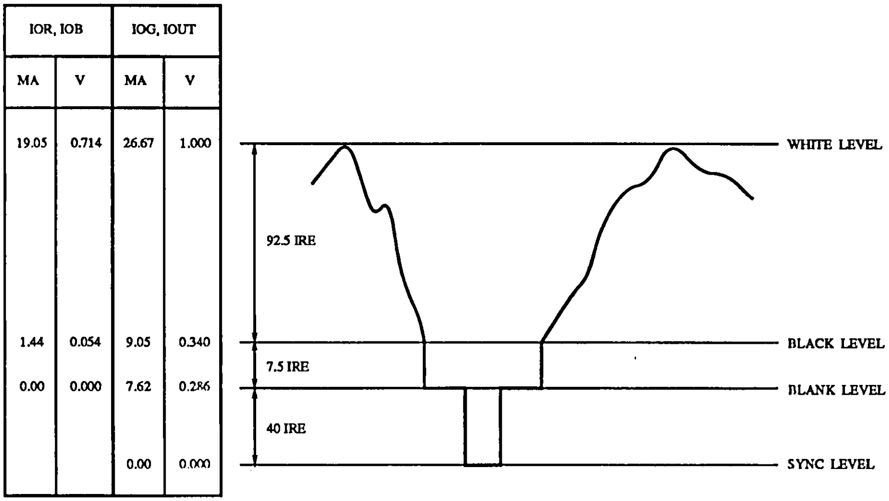
All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

OL	P0–P3	Addressed by frame buffer
0	$0	color palette entry $0
0	$1	color palette entry $1
:	:	:
0	$F	color palette entry $F
1	$x	overlay color

Table 2. Palette and Overlay Select Truth Table.

Circuit Description (continued)


IOR, IOB
IOG, IOUT
MA
V
MA
V
19.05
0.714
26.67
1.000
1.44
0.054
9.05
0.340
0.00
0.000
7.62
0.286
0.00
0.000
WHITE LEVEL
92.5 IRE
BLACK LEVEL
7.5 IRE
BLANK LEVEL
40 IRE
SYNC LEVEL

Note: 75 Ω doubly terminated load, RSET = 523 Ω. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms.

Description	IOG, IOUT (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$F
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$0
BLACK - SYNC	1.44	1.44	0	1	$0
BLANK	7.62	0	1	0	$x
SYNC	0	0	0	0	$x

Note: Typical with full-scale IOG = 26.67 mA. RSET = 523 Ω.

Table 3. Video Output Truth Table.

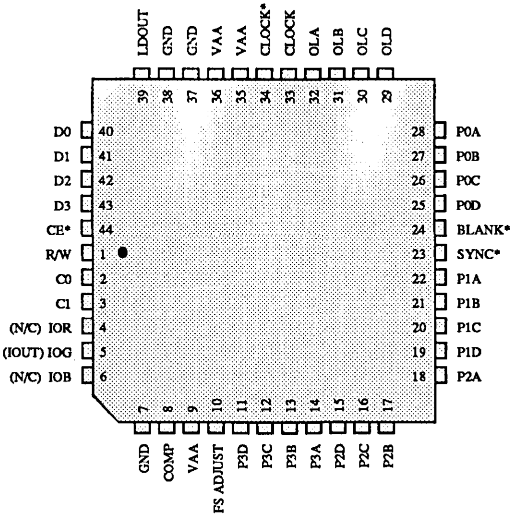
Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Table 3. It is latched on the rising edge of LDOUT. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 3). SYNC* does not override any other control or data input, as shown in Table 3; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of LDOUT. If sync information is not to be generated on the IOG output, this pin should be connected to GND.
LDOUT	Load control output (TTL compatible). The P0–P3 {A–D}, OL {A–D}, BLANK*, and SYNC* inputs are latched on the rising edge of LDOUT. LDOUT is internally generated by dividing the clock by four. LDOUT should have absolute minimal loading (one TTL load) to avoid display artifacts.
P0–P3 {A–D}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which one of the 16 entries in the color palette RAM is to be used to provide color information. Four consecutive pixels (up to 4 bits per pixel) are input through this port. They are latched on the rising edge of LDOUT. P0 is the LSB. Unused inputs should be connected to GND. Note that the {A} pixel is output first, followed by the {B} pixel, etc., until all four pixels have been output, at which point the cycle repeats.
OL {A–D}	Overlay select inputs (TTL compatible). These control inputs are latched on the rising edge of LDOUT, and specify which palette is to be used for color information. A logical zero indicates the color palette RAM is to provide color information, while a logical one indicates the overlay register is to provide color information. When accessing the overlay palette, the P0–P3 {A–D} inputs are ignored. Unused inputs should be connected to GND.
IOR, IOG, IOB, IOUT	Red, green, and blue video current outputs. These high-impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 4). All outputs, whether used or not, should have the same output load. The Bt455 outputs IOUT rather than IOR, IOG, and IOB.
GND	Analog ground. All GND pins must be connected.
VAA	Analog power. All VAA pins must be connected.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal (Figure 4). Note that the IRE relationships in Figure 3 are maintained, regardless of the full scale output current. The relationship between RSET and the full scale output current on IOG is: $\text{RSET}\ (\Omega) = 13{,}948\ /\ \text{IOG}\ (\text{mA})$ The full-scale output current on IOR and IOB for a given RSET is: $\text{IOR, IOB}\ (\text{mA}) = 9{,}963\ /\ \text{RSET}\ (\Omega)$

4

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and the adjacent VAA pin (Figure 4). Connecting the capacitor to VAA rather than to GND provides the highest possible low-frequency power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *Refer to PC Board Layout Considerations for critical layout criteria.*
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE* (Figure 1). Care should be taken to avoid glitches on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0 - D3	Data bus (TTL compatible). Data is transferred into and out of the device over this 4 bit bidirectional data bus. D0 is the least significant bit.


LDOUT 39
GND 38
GND 37
VAA 36
VAA 35
CLOCK* 34
CLOCK 33
OLA 32
OLB 31
OLC 30
OLD 29
D0 40
D1 41
D2 42
D3 43
CE* 44
R/W 1
C0 2
C1 3
(N/C) IOR 4
(IOUT) IOG 5
(N/C) IOB 6
28 P0A
27 P0B
26 P0C
25 P0D
24 BLANK*
23 SYNC*
22 P1A
21 P1B
20 P1C
19 P1D
18 P2A
7 GND
8 COMP
9 VAA
10 FS ADJUST
11 P3D
12 P3C
13 P3B
14 P3A
15 P2D
16 P2C
17 P2B

Note: Bt455 pin names are in parentheses.

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in Bt451/7/8 Evaluation Module Operation and Measurements, application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt454/455 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a 6-layer PC board is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane (preferably analog ground plane), layer 3 the analog power plane, using the remaining layers for digital traces and digital power supplies.

The optimum layout enables the Bt454/455 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8 inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground tub isolation technique is constrained by the noise margin degradation during digital readback of the Bt454/455.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

The analog ground plane should include all Bt454/455 ground pins, reference circuitry (RSET resistors, etc.), power supply bypass circuitry for the Bt454/455, analog output traces, and the video output connector. The Bt455 no-connect (N/C) pins should be tied directly to ground.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt454/455 power pins, any reference circuitry, and COMP and reference decoupling. There should be at least a 1/8 inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 4. This bead should be located within 3 inches of the Bt454/455 and provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor decoupling each of the two groups of VAA pins to GND. The capacitors should be placed as close as possible to the device.

The 10 µF capacitor is for low frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. Lead lengths should be minimized for best performance.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt454/455 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt454/455 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt454/455 to minimize reflections. Unused analog outputs should be connected to GND.

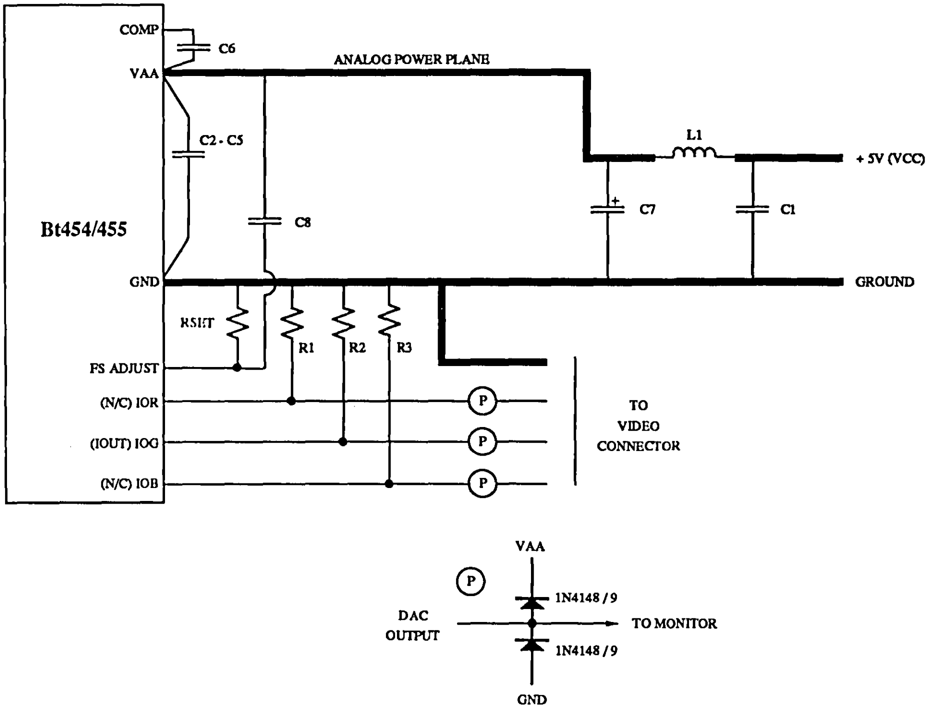
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

Analog Output Protection

The Bt454/455 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 4 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)


COMP
C6
VAA
ANALOG POWER PLANE
C2 - C5
L1
+5V (VCC)
C7
C1
C8
Bt454/455
GND
GROUND
RSET
R1
R2
R3
FS ADJUST
(N/C) IOR
(IOUT) IOG
(N/C) IOB
P
TO
VIDEO
CONNECTOR
VAA
P
1N4148/9
DAC
OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description	Vendor Part Number
C1, C7	10 µF tantalum capacitor	Mallory CSR13G106KM
C2, C3, C6, C8	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C4, C5	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R500S41W103KP
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt454/455.

Figure 4. Typical Connection Diagram and Parts List.

Application Information

LDOUT Termination

To reduce reflections on the LDOUT signal, it should be terminated at the point furthest from the Bt454/455. A 330 Ω resistor to VCC and a 470 Ω resistor to GND should work in most cases.

LDOUT should have absolute minimal loading (one TTL load) to avoid display artifacts.

Using Multiple Bt455s

When using multiple Bt455s, each Bt455 should have its own power plane ferrite bead.

Each Bt455 must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, and COMP capacitor.

TTL Clock Interfacing

Figure 5 illustrates interfacing the Bt454/455 to a TTL clock. The MC10H116 is operated from a single +5 V supply. The resistor network attenuates the TTL levels to MECL input levels. Although not shown, both the CLOCK and CLOCK* lines require termination resistors (220 Ω resistor to VCC and 330 Ω resistor to GND), located as close as possible to the Bt454/455.

ECL Clock Generation

Due to the high clock rates at which the Bt454/455 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (typically a 220 Ω resistor to VCC and a 330 Ω resistor to GND), located as close as possible to the Bt454/455.

170 MHz applications require robust ECL clock signals with strong pull-down (~20 mA at VOH) and double termination for clock trace lengths greater than 2 inches.

The CLOCK and CLOCK* inputs must be differential signals due to the noise margins of the CMOS process. The Bt454/455 will not function using a single-ended CLOCK with CLOCK* connected to ground.

A 10K or 10KH ECL crystal oscillator that generates differential outputs, operating between +5 V and ground, may be interfaced directly to the B454/455, as shown in Figure 6. If the crystal oscillator generates only a single-ended output, a MC10H116 may be used to generate the differential clock signals, as illustrated in Figure 7. If the MC10H116 is not readily available, a MC10H101, MC10H105, or MC10H107 may be used.

Although ECL works well using a single +5 V supply, care must be taken to isolate the TTL power supply lines from the ECL power supply. Further information on ECL design may be obtained in the MECL Device Data Catalog and the MECL System Design Handbook, by Motorola.

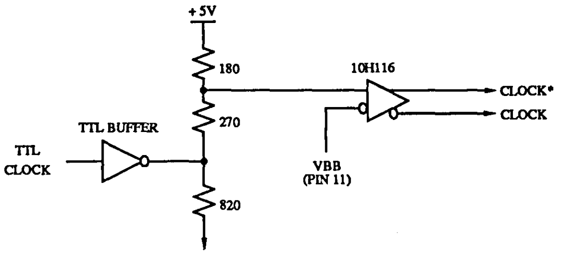


Figure 5. Interfacing the Bt454/455 to a TTL Clock.

Application Information (continued)

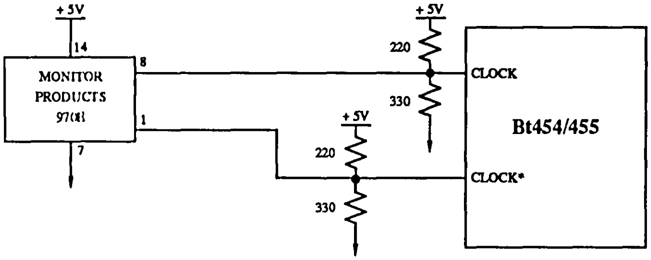

+5V
14
MONITOR
PRODUCTS
970B
7
8
1
+5V
220
330
+5V
220
330
CLOCK
CLOCK*
Bt454/455

Figure 6. Interfacing to a Differential ECL Oscillator.

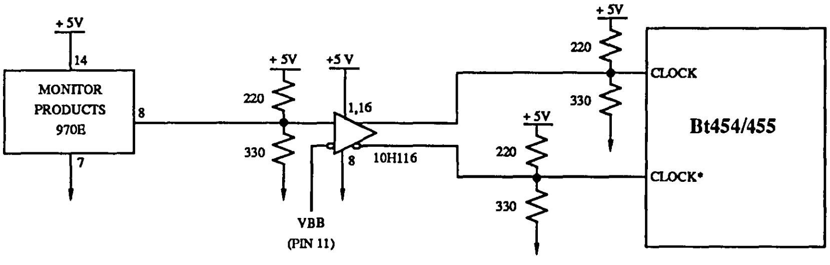

+5V
14
MONITOR
PRODUCTS
970B
7
8
+5V
220
330
+5V
1,16
8
10H116
VBB
(PIN 11)
+5V
220
330
+5V
220
330
CLOCK
CLOCK*
Bt454/455

Figure 7. Interfacing to a Single-Ended ECL Oscillator.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ohms
FS ADJUST Resistor	RSET		523		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		4	4	4	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1/4	LSB
Differential Linearity Error	DL			±1/4	LSB
Gray Scale Error				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
(except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance	CIN		10		pF
(f = 1 MHz, Vin = 2.4 V)					
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	.6		6	Volts
Input High Current (Vin = 4.2 V)	IKIH			1	µA
Input Low Current (Vin = 3.2 V)	IKIL			–1	µA
Input Capacitance	CKIN		10		pF
(f = 1 MHz, Vin = 4.2 V)					
Digital Outputs					
Output High Voltage	VOH				
D0–D3 (IOH = –400 µA)		2.4			Volts
LDOUT (IOH = -12 mA)		2.4			Volts
Output Low Voltage	VOL				
D0–D3 (IOL = 3.2 mA)				0.4	Volts
LDOUT (IOL = 24 mA)				0.5	Volts
3-state Current (D0–D3)	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		16.81	19.05	21.30	mA
White Level Relative to Black		15.86	17.62	19.40	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG or IOUT		6.29	7.62	8.96	mA
Sync Level on IOG or IOUT		0	5	50	µA
LSB Size			1.175		mA
DAC-to-DAC Matching				5	%
Output Compliance	VOC	−1.0		+1.4	Volts
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		20		pF
Internal Reference Voltage	VREF	1.18	1.22	1.26	Volts
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

		170 MHz Devices			135 MHz Devices			110 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			170			135			110	MHz
R/W, C0, C1 Setup Time	1	0			0			0			ns
R/W, C0, C1 Hold Time	2	15			15			15			ns
CE* Low Time	3	50			50			50			ns
CE* High Time	4	25			25			25			ns
CE* Asserted to Data Bus	5	10			10			10			ns
CE* Asserted to Data Valid	6			75			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15			15	ns
Write Data Setup Time	8	35			35			35			ns
Write Data Hold Time	9	10			10			10			ns
LDOUT Pulse Width High	10	9			11.5			13			ns
LDOUT Pulse Width Low	11	9			11.5			13			ns
Clock to LDOUT	12	4	7.5	14.3	4	7.5	14.3	4	7.5	14.3	ns
Pixel and Control Setup Time	13	0			0			0			ns
Pixel and Control Hold Time	14	3			5			5			ns
Clock Cycle Time	15	5.88			7.4			9			ns
Clock Pulse Width High	16	2			3			3.6			ns
Clock Pulse Width Low	17	2			3			3.6			ns
Analog Output Delay	18		20			20			20		ns
Analog Output Rise/Fall Time	19		2			2			2		ns
Analog Output Settling Time*	20			6			9			9	ns
Clock and Data Feedthrough*			70			70			70		pV - sec
Glitch Impulse*			50			50			50		pV - sec
Analog Output Skew			0	2		0	2		0	2	ns
Pipeline Delay		6	6	6	6	6	6	6	6	6	Clocks
VAA Supply Current**	IAA		200	tbd		150	tbd		120	200	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are 3.2–4.2 volts, with input rise/fall times ≤ 2 ns, measured between 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D3 output load ≤ 75 pF. See timing notes in Figure 9. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V, TA = 20° C. IAA (max) at VAA = 5.25 V, TA = 0° C.

Timing Waveforms

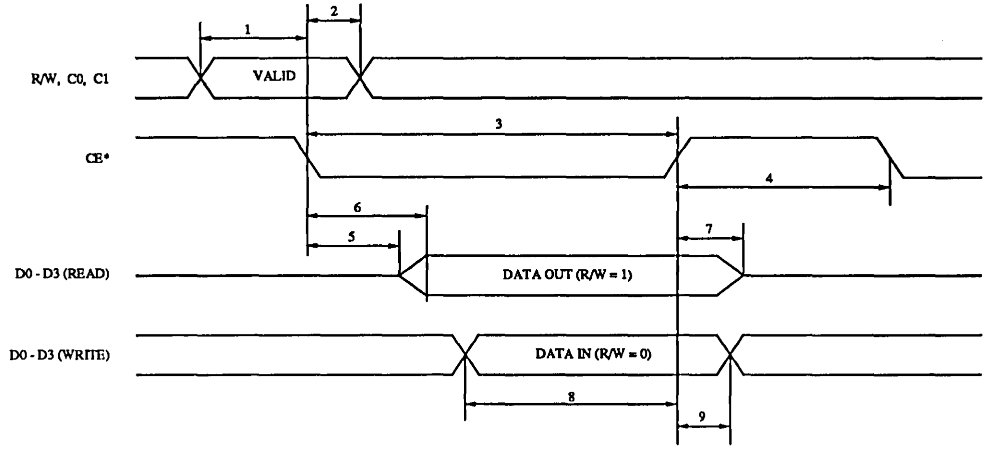
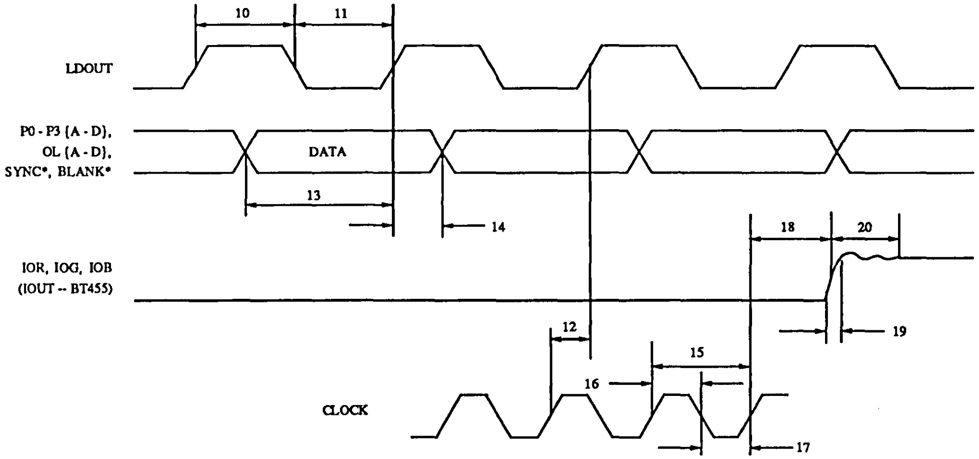

1
2
R/W, C0, C1
VALID
3
CE*
4
6
5
7
D0 - D3 (READ)
DATA OUT (R/W = 1)
D0 - D3 (WRITE)
DATA IN (R/W = 0)
8
9

Figure 8. MPU Read/Write Timing Dimensions..


10
11
LDOUT
P0 - P3 {A - D},
OL {A - D},
SYNC*, BLANK*
DATA
13
14
18
20
IOR, IOG, IOB
(IOUT -- BT455)
19
12
15
16
CLOCK
17

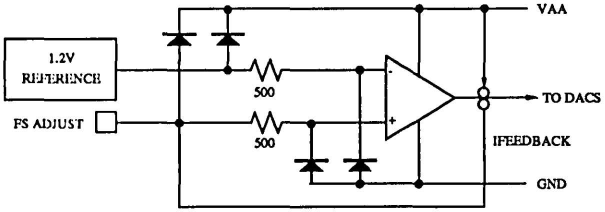
Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full scale transition.

Note 2: Output settling time measured from 50% point of full-scale transition to output settling within ±1/4LSB.

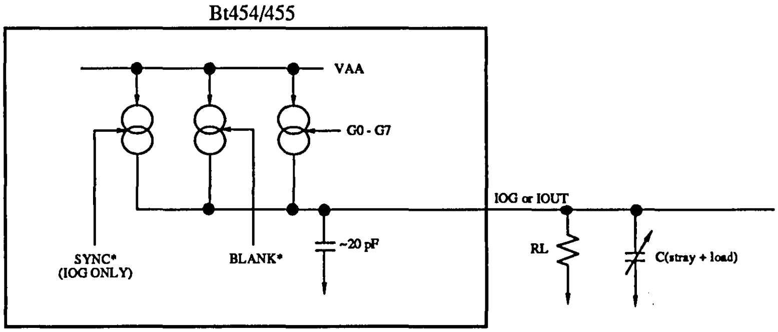
Note 3: Output rise/fall time measured between 10% and 90% points of full-scale transition.

Figure 9. Video Input/Output Timing.

Device Circuit Data


1.2V
REFERENCE
FS ADJUST
500
500
VAA
TO DACS
IFEEDBACK
GND

Equivalent Circuit of the Reference Amplifier.


Bt454/455
VAA
G0 - G7
IOG or IOUT
~20 pF
RL
C(stray + load)
SYNC*
(IOG ONLY)
BLANK*

Equivalent Circuit of the Current Output (IOG or IOUT).

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt454KPJ	110 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt454KPJ135	135 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt454KPJ170	170 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt455KPJ110	110 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt455KPJ135	135 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt455KPJ170	170 MHz	44-pin Plastic J-Lead	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
F	Note added to pin description and applications section that LDOUT should have absolute minimal loading (one TTL load) to avoid display artifacts.
G	Expanded PCB layout section.
H	Added Bt455 part and description.
I	Expanded ESD and PCB Layout sections.

Bt458/883

MIL-STD-883C, Class B
Monolithic CMOS
256 x 24 Color Palette
110 MHz RAMDAC™

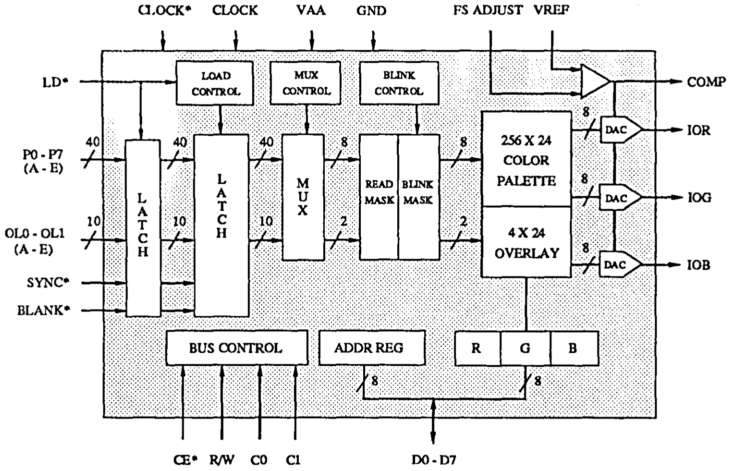
Distinguishing Features

- 110 MHz Pipelined Operation
- Multiplexed TTL Pixel Ports
- Triple 8-bit D/A Converters
- 256 x 24 Dual Port Color Palette
- 4 x 24 Dual Port Overlay Registers
- RS-343A Compatible RGB Outputs
- Bit Plane Read and Blink Masks
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 84-pin Ceramic PGA Package
- Typical Power Dissipation: 2 W

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Functional Block Diagram



CLOCK*
CLOCK
VAA
GND
FS ADJUST
VREF
LD*
P0 - P7
(A - E)
OL0 - OL1
(A - E)
SYNC*
BLANK*
40
10
LATCH
LOAD CONTROL
MUX CONTROL
BLINK CONTROL
MUX
8
2
READ MASK
BLINK MASK
256 X 24 COLOR PALETTE
4 X 24 OVERLAY
DAC
COMP
IOR
IOG
IOB
BUS CONTROL
ADDR REG
R
G
B
CE*
R/W
C0
C1
D0 - D7

Product Description

The Bt458/883 is a triple 8-bit RAMDAC designed specifically for high-performance, high-resolution color graphics.

The architecture enables the display of 1280 x 1024 bit-mapped color graphics (up to 8 bits per pixel plus up to 2 bits of overlay information), minimizing the use of costly ECL interfacing, as most of the high speed (pixel clock) logic is contained on chip. The multiple pixel ports and internal multiplexing enables TTL-compatible interfacing (up to 28 MHz) to the frame buffer, while maintaining the 110 MHz video data rates required for sophisticated color graphics.

The Bt458/883 has a 256 x 24 color lookup table with triple 8-bit video D/A converters. On-chip features include programmable blink rates, bit plane masking and blinking, color overlay capability, and a dual-port color palette RAM.

The Bt458/883 generates RS-343A-compatible red, green, and blue video signals, and is capable of driving doubly terminated 75 Ω coax directly, without requiring external buffering.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L458M01 Rev. I

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt458/883 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color/overlay palettes. The dual-port color palette RAM and dual-port overlay registers allow color updating without contention with the display refresh process.

As illustrated in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register, color palette RAM entry, or overlay register will be accessed by the MPU.

The 8-bit address register (ADDR0–7) is used to address the internal RAM and registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. During the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be read. The MPU performs three successive read cycles (red, green, and blue), using C0 and C1 to select either the color palette RAM or overlay registers. Following the blue read cycle, the address register increments to the next location, which the MPU may read by simply reading another sequence of red, green, and blue data.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register 3. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR0–7) are accessible to the MPU.

	Value	C1	C0	Addressed by MPU
ADDRa, b (counts modulo 3)	00	x	1	red value
	01	x	1	green value
	10	x	1	blue value
ADDR0–7 (counts binary)	$xx	0	0	address register
	$00 - $FF	0	1	color palette RAM
	$00	1	1	overlay color 0
	$01	1	1	overlay color 1
	$02	1	1	overlay color 2
	$03	1	1	overlay color 3
	$04	1	0	read mask register
	$05	1	0	blink mask register
	$06	1	0	command register
	$07	1	0	test register

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Additional Information

Although the color palette RAM and overlay registers are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the blue write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Accessing the control registers is also done through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations.

Note that if an invalid address in loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing when accessing the Bt458/883.

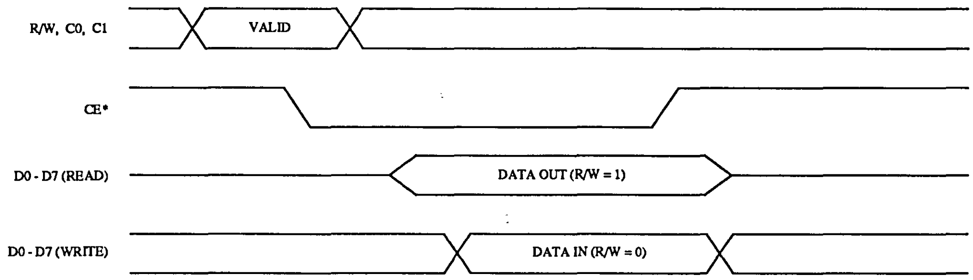


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at reasonable data rates (up to 28 MHz), the Bt458/883 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color (up to 8 bits per pixel), and overlay (up to 2 bits per pixel) information, for either four or five consecutive pixels, are latched into the device. Note that with this configuration, the sync and blank timing will be recognized only with four- or five-pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing.

Each clock cycle, the Bt458/883 outputs color information based on the {A} inputs, followed by the {B} inputs, etc., until all four or five pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external character or cursor generation logic.

To simplify the frame buffer interface timing, LD* may be phase shifted, in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by four or five, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than four, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate (up to 110 MHz).

If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*.

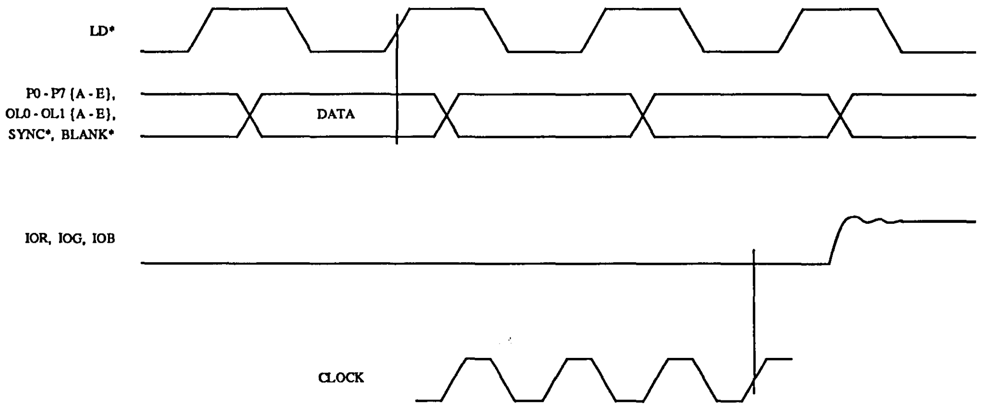


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Color Selection

Each clock cycle, 8 bits of color information (P0–P7) and 2 bits of overlay information (OL0, OL1) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual bit planes may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change due to blinking does not occur during the active display time (i.e., in the middle of the screen), the Bt458/883 monitors the BLANK* input to determine vertical retrace intervals. A vertical retrace interval is recognized by determining that BLANK* has been a logical zero for at least 256 LD* cycles.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAM. Table 2 illustrates the truth table used for color selection.

Video Generation

Every clock cycle, the selected 24 bits of color information (8 bits each of red, green, and blue) are presented to the three 8-bit D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 3.

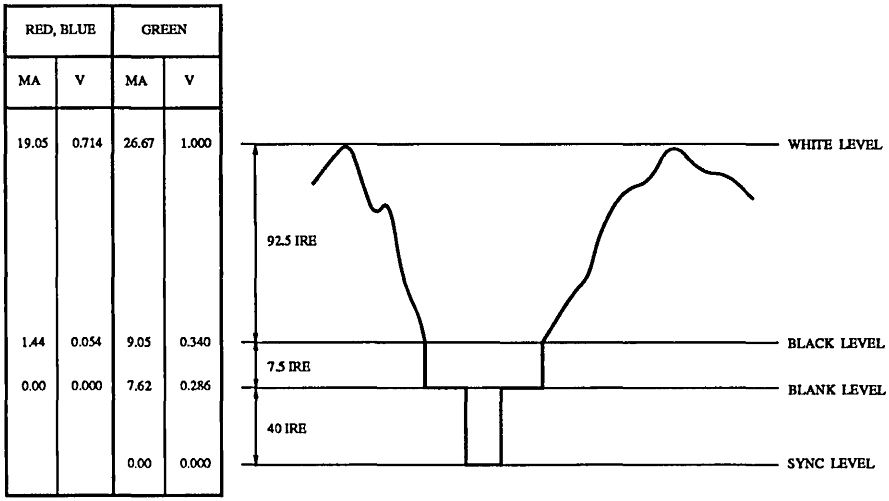
The varying output current from each of the D/A converters produces a corresponding voltage level, which is used to drive the color CRT monitor. Note that only the green output (IOG) contains sync information. Table 3 details how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt458/883 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the D/A converter's full scale output current against temperature and power supply variations.

CR6	OL1	OL0	P7–P0	Addressed by frame buffer
1	0	0	$00	color palette entry $00
1	0	0	$01	color palette entry $01
:	:	:	:	:
1	0	0	$FF	color palette entry $FF
0	0	0	$xx	overlay color 0
x	0	1	$xx	overlay color 1
x	1	0	$xx	overlay color 2
x	1	1	$xx	overlay color 3

Table 2. Palette and Overlay Select Truth Table.

Circuit Description (continued)



RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

Note: 75 Ω doubly terminated load, RSET = 523 Ω, VREF = 1.235 V. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 523 Ω, VREF = 1.235 V.

Table 3. Video Output Truth Table.

Internal Registers

Command Register

The command register may be written to or read by the MPU at any time, and is not initialized. CR0 corresponds to data bus bit D0.

CR7	Multiplex select (0) 4:1 multiplexing (1) 5:1 multiplexing	This bit specifies whether 4:1 or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 4:1 is specified, the {E} pixel and {E} overlay inputs are ignored and should be connected to GND, and the LD* input should be 1/4 the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be 1/5 the CLOCK rate. Note that it is possible to reset the pipeline delay of the Bt458/883 to a fixed eight clock cycles. In this instance, each time the input multiplexing is changed, the Bt458/883 must again be reset to a fixed pipeline delay.
CR6	RAM enable (0) use overlay color 0 (1) use color palette RAM	When the overlay select bits are 00, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information.
CR5, CR4	Blink rate selection (00) 16 on, 48 off (25/75) (01) 16 on, 16 off (50/50) (10) 32 on, 32 off (50/50) (11) 64 on, 64 off (50/50)	These two bits control the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (% on/off).
CR3	OL1 blink enable (0) disable blinking (1) enable blinking	If a logical one, this bit forces the OL1 {A–E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL1 {A–E} inputs. In order for overlay 1 bit plane to blink, bit CR1 must be set to a logical one.
CR2	OL0 blink enable (0) disable blinking (1) enable blinking	If a logical one, this bit forces the OL0 {A–E} inputs to toggle between a logical zero and the input value at the selected blink rate prior to selecting the palettes. A value of logical zero does not affect the value of the OL0 {A–E} inputs. In order for overlay 0 bit plane to blink, bit CR0 must be set to a logical one.

Internal Registers (continued)

Command Register (continued)

CR1	OL1 display enable (0) disable (1) enable	If a logical zero, this bit forces the OL1 {A–E} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL1 {A–E} inputs.
CR0	OL0 display enable (0) disable (1) enable	If a logical zero, this bit forces the OL0 {A–E} inputs to a logical zero prior to selecting the palettes. A value of a logical one does not affect the value of the OL0 {A–E} inputs.

Read Mask Register

The read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. D0 corresponds to bit plane 0 (P0 {A–E}) and D7 corresponds to bit plane 7 (P7 {A–E}). Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized.

Blink Mask Register

The blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by the command register. D0 corresponds to bit plane 0 (P0 {A–E}) and D7 corresponds to bit plane 7 (P7 {A–E}). In order for a bit plane to blink, the corresponding bit in the read mask register must be a logical one. This register may be written to or read by the MPU at any time and is not initialized.

Internal Registers (continued)

Test Register

The test register provides diagnostic capability by enabling the MPU to read the inputs to the D/A converters. It may be written to or read by the MPU at any time, and is not initialized. When writing to the register, the upper 4 bits (D4–D7) are ignored.

The contents of the test register are defined as follows:

D7–D4	color information (4 bits of red, green, or blue)
D3	low (logical one) or high (logical zero) nibble
D2	blue enable
D1	green enable
D0	red enable

To use the test register, the host MPU writes to it, setting one, and only one, of the (red, green, blue) enable bits. These bits specify which 4 bits of color information the MPU wishes to read (R0–R3, G0–G3, B0–B3, R4–R7, G4–G7, or B4–B7). When the MPU reads the test register, the 4 bits of color information from the DAC inputs are contained in the upper 4 bits, and the lower 4 bits contain the (red, green, blue, low or high nibble) enable information previously written. Note that either the CLOCK must be slowed down to the MPU cycle time, or the same pixel and overlay data must be presented to the device during the entire MPU read cycle.

For example, to read the upper 4 bits of red color information being presented to the D/A converters, the MPU writes to the test register, setting only the red enable bit. The MPU then proceeds to read the test register, keeping the pixel data stable, which results in D4–D7 containing R4–R7 color bits, and D0–D3 containing (red, green, blue, low or high nibble) enable information, as illustrated below:

D7	R7
D6	R6
D5	R5
D4	R4
D3	0
D2	0
D1	0
D0	1

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Table 3. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 3). SYNC* does not override any other control or data input, as shown in Table 3; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0–P7 {A–E}, OL0–OL1 {A–E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD*, while it is either 1/4 or 1/5 the CLOCK rate, may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle, within the limits specified by the AC Characteristics section.
P0–P7 {A–E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. Either four or five consecutive pixels (up to 8 bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Note that the {A} pixel is output first, followed by the {B} pixel, etc., until all four or five pixels have been output, at which point the cycle repeats.
OL0–OL1 {A–E}	Overlay select inputs (TTL compatible). These control inputs are latched on the rising edge of LD* and, in conjunction with bit 6 of the command register, specify which palette is to be used for color information, as follows:

OL1	OL0	CR6 = 1	CR6 = 0
0	0	color palette RAM	overlay color 0
0	1	overlay color 1	overlay color 1
1	0	overlay color 2	overlay color 2
1	1	overlay color 3	overlay color 3

When accessing the overlay palette, the P0–P7 {A–E} inputs are ignored. Overlay information bits (up to 2 bits per pixel) for either four or five consecutive pixels are input through this port. Unused inputs should be connected to GND.

Pin Name	Description
IOR, IOG, IOB	Red, green, and blue video current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75-ohm coaxial cable (Figure 4).
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic capacitor must be connected between this pin and VAA (Figure 4). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to *PC Board Layout Considerations* for critical layout criteria.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 4). Note that the IRE relationships in Figure 3 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is: $RSET\ (\Omega) = 11{,}294 * VREF\ (V) / IOG\ (mA)$ The full-scale output current on IOR and IOB for a given RSET is: $IOR, IOB\ (mA) = 8{,}067 * VREF\ (V) / RSET\ (\Omega)$
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 4, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.01 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 4. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE* (Figure 1). Care should be taken to avoid glitches on this edge triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.

Pin Descriptions (continued)

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	L9	P5A	K11	VAA	C12
SYNC*	M10	P5B	L12	VAA	C11
LD*	M9	P5C	K12	VAA	A9
CLOCK*	L8	P5D	J11	VAA	L7
CLOCK	M8	P5E	J12	VAA	M7
				VAA	A7
P0A	G1	P6A	H11		
P0B	G2	P6B	H12	GND	B12
P0C	H1	P6C	G12	GND	B11
P0D	H2	P6D	G11	GND	M6
P0E	J1	P6E	F12	GND	B6
				GND	A6
P1A	J2	P7A	F11		
P1B	K1	P7B	E12	COMP	A12
P1C	L1	P7C	E11	FS ADJUST	B10
P1D	K2	P7D	D12	VREF	C10
P1E	L2	P7E	D11		
				CE*	A5
P2A	K3	OL0A	A1	R/W	B8
P2B	M1	OL0B	C2	C1	A8
P2C	L3	OL0C	B1	C0	B7
P2D	M2	OL0D	C1		
P2E	M3	OL0E	D2	D0	C3
				D1	B2
P3A	L4	OL1A	D1	D2	B3
P3B	M4	OL1B	E2	D3	A2
P3C	L5	OL1C	E1	D4	A3
P3D	M5	OL1D	F1	D5	B4
P3E	L6	OL1E	F2	D6	A4
				D7	B5
P4A	M11	IOG	A10		
P4B	L10	IOB	A11		
P4C	L11	IOR	B9		
P4D	K10				
P4E	M12				

Pin Descriptions (continued)

Bt458/883

(TOP VIEW)

12	COMP	GND	VAA	P7D	P7B	P6E	P6C	P6B	P5E	P5C	P5B	P4E
11	IOB	GND	VAA	P7E	P7C	P7A	P6D	P6A	P5D	P5A	P4C	P4A
10	IOG	FS ADJ	VREF							P4D	P4B	SYNC*
9	VAA	IOR									BLK*	LD*
8	C1	R/W									CLK*	CLK
7	VAA	C0									VAA	VAA
6	GND	GND									P3E	GND
5	CE*	D7									P3C	P3D
4	D6	D5									P3A	P3B
3	D4	D2	D0							P2A	P2C	P2E
2	D3	D1	OL0B	OL0E	OL1B	OL1E	P0B	P0D	P1A	P1D	P1E	P2D
1	OL0A	OL0C	OL0D	OL1A	OL1C	OL1D	P0A	P0C	P0E	P1B	P1C	P2B
	A	B	C	D	E	F	G	H	J	K	L	M

alignment marker (on top)

(BOTTOM VIEW)

12	P4E	P5B	P5C	P5E	P6B	P6C	P6E	P7B	P7D	VAA	GND	COMP
11	P4A	P4C	P5A	P5D	P6A	P6D	P7A	P7C	P7E	VAA	GND	IOB
10	SYNC*	P4B	P4D							VREF	FS ADJ	IOG
9	LD*	BLK*									IOR	VAA
8	CLK	CLK*									R/W	C1
7	VAA	VAA									C0	VAA
6	GND	P3E									GND	GND
5	P3D	P3C									D7	CE*
4	P3B	P3A									D5	D6
3	P2E	P2C	P2A							D0	D2	D4
2	P2D	P1E	P1D	P1A	P0D	P0B	OL1E	OL1B	OL0E	OL0B	D1	D3
1	P2B	P1C	P1B	P0E	P0C	P0A	OL1D	OL1C	OL1A	OL0D	OL0C	OL0A
	M	L	K	J	H	G	F	E	D	C	B	A

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in *Bt451/7/8 Evaluation Module Operation and Measurements,* application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt458/883 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a 6-layer PC board is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane (preferably analog ground plane), layer 3 the analog power plane, using the remaining layers for digital traces and digital power supplies.

The optimum layout enables the Bt458/883 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8 inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground partitioning isolation technique is constrained by the noise margin degradation during digital readback of the Bt458/883.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

For maximum performance, a separate isolated ground plane for the analog output termination resistors, RSET resistor, and VREF circuitry should be used, as shown in Figure 13. Another isolated ground plane is used for the GND pins of the Bt458/883 and supply decoupling capacitors.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt458/883 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8 inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 13. This bead should be located within 3 inches of the Bt458/883 and provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor decoupling each of four groups of VAA pins to GND. The capacitors should be placed as close as possible to the device.

The 33 µF capacitor is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic chip capacitor. Low-frequency supply noise will require a larger value. Lead lengths should be minimized for best performance so that the self-resonance frequency is greater than the LD* frequency.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt458/883 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit by using lower speed logic (3-5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt458/883 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt458/883 to minimize reflections. Unused analog outputs should be connected to GND.

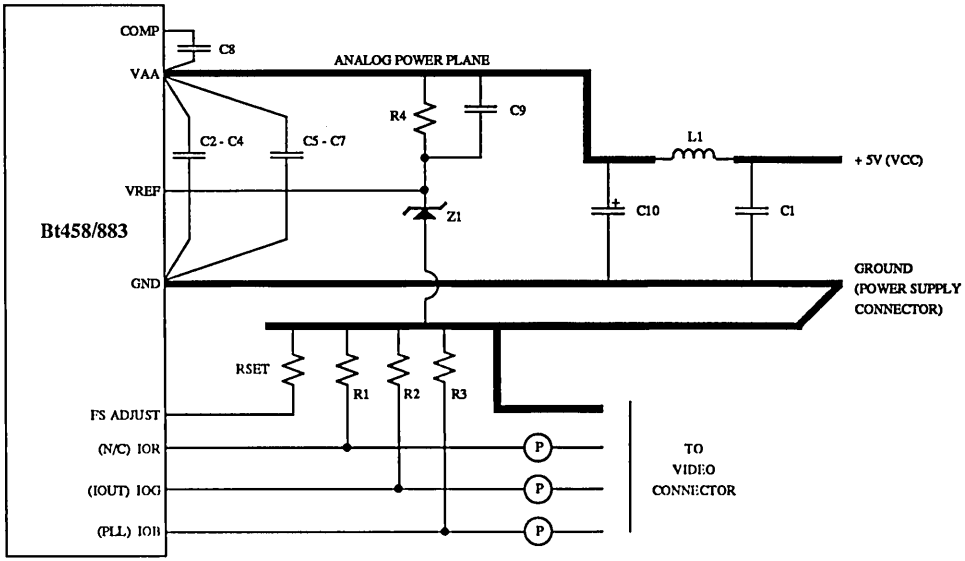
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

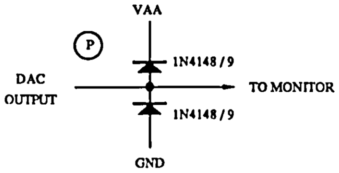
Analog Output Protection

The Bt458/883 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 4 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)


COMP
C8
VAA
ANALOG POWER PLANE
R4
C9
C2 - C4
C5 - C7
L1
+ 5V (VCC)
VREF
Z1
C10
C1
Bt458/883
GROUND
(POWER SUPPLY
CONNECTOR)
GND
RSET
R1
R2
R3
FS ADJUST
(N/C) IOR
(IOUT) IOG
(PLL) IOB
P
P
P
TO
VIDEO
CONNECTOR


VAA
P
1N4148/9
DAC
OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description
C1–C4	0.1 µF ceramic capacitor
C5–C7	0.01 µF ceramic chip capacitor
C8, C9	0.1 µF ceramic capacitor
C10	33 µF tantalum capacitor
L1	ferrite bead
R1, R2, R3	75 Ω 1% metal film resistor
R4	1000 Ω 1% metal film resistor
RSET	523 Ω 1% metal film resistor
Z1	1.2 V voltage reference

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt458/883.

Figure 4. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Due to the high clock rates at which the Bt458/883 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (220 Ω resistor to VCC and a 330 Ω resistor to GND). The termination resistors should be as close as possible to the Bt458/883.

The CLOCK and CLOCK* inputs must be differential signals due to the noise margins of the CMOS process. The Bt458/883 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by four or five (depending on whether 4:1 or 5:1 multiplexing was specified) and translating it to TTL levels. As LD* may be phase shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

It is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports both the 4:1 and 5:1 input multiplexing of the Bt458/883, and will also optionally set the pipeline delay of the Bt458/883 to eight clock cycles. The Bt438 may also be used to interface the Bt458/883 to a TTL clock. Figure 5 illustrates using the Bt438 with the Bt458/883.

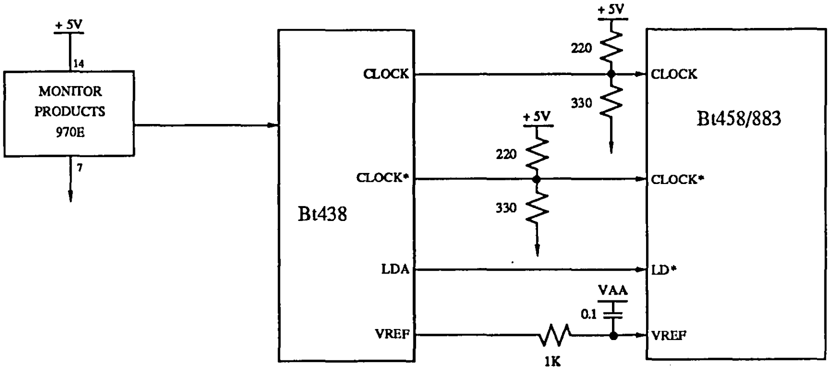


Figure 5. Generating the Bt458/883 Clock Signals.

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt458/883, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The Bt458/883 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438 Clock Generator Chip supports this mode of operation when used with the Bt458/883.

To reset the Bt458/883, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for at least three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

The resetting of the Bt458/883 to an eight clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if the multiple Bt458/883s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control via the read mask register and overlay display enable bits.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.5	5.0	5.5	Volts
Ambient Operating Temperature	TA	-55		+125	°C
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.20	1.235	1.26	Volts
FS ADJUST Resistor	RSET		523		Ohms
CLOCK, CLOCK* Inputs					
Input High Voltage		VAA-1.0		VAA+0.5	Volts
Input Low Voltage		GND-0.5		VAA-1.6	Volts
Differential Voltage		600			mV

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on Any Digital Pin		GND-0.5		VAA+0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
θ JC				15	°C/W
θ JA				25	°C/W
Power Dissipation				3.025	W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity**			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0			Volts
Input Low Voltage	VIL			0.8	Volts
Input High Current (Vin = VAA)	IIH			10	µA
Input Low Current (Vin = 0 V)	IIL			-10	µA
Input Capacitance***	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Input High Current (Vin = VAA)	IKIH			10	µA
Input Low Current (Vin = 0 V)	IKIL			-10	µA
Input Capacitance***	CKIN		4	10	pF
Digital Outputs (D0-D7)					
Output High Voltage (IOH = -800 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	Volts
3-state Current	IOZ			10	µA
Output Capacitance***	CDOUT			10	pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		-10	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		-10	5	50	µA
DAC-to-DAC Matching****					
TA = +25, +125 °C			3	5	%
TA = -55 °C				7	%
Output Compliance	VOC	-1.0		+1.2	Volts
Output Capacitance***	CAOUT			20	pF
Voltage Reference Input Leakage Current (VREF = 1.235 V)	IREF			10	µA
Power Supply Rejection Ratio*** (COMP = 0.01 µF, f = 1 KHz)	PSRR			0.5	% / % ΔVAA

Test conditions (unless otherwise specified): 100% tested at VAA = 4.5 V and 5.5 V, TA = -55°, 25°, and 125° C, RSET = 523 Ω ± 0.1%, VREF = 1.235 V. Typical values are based on nominal temperature, i.e., room and nominal voltage, i.e., 5 V.

**Guaranteed by design, not tested.

***Derived from characterization (TA = 25° C, VAA = 5 V ± 10%), not tested. These parameters are controlled via design or process parameters and are not directly tested. They are characterized upon initial design release and upon design changes which could affect them.

****Computed by the formula: (max refwhite – min refwhite / max ref-white) * 100

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate****	Fmax			110	MHz
LD* Rate****	LDmax			27.5	MHz
R/W, C0, C1 Setup Time	1	0			ns
R/W, C0, C1 Hold Time	2	15			ns
CE* Low Time	3	50			ns
CE* High Time	4	25			ns
CE* Asserted to Data Bus Driven	5	8			ns
CE* Asserted to Data Valid	6			75	ns
CE* Negated to Data Bus 3-Stated	7			15	ns
Write Data Setup Time	8	35			ns
Write Data Hold Time	9	3			ns
Pixel and Control Setup Time	10	3			ns
Pixel and Control Hold Time	11	2			ns
Clock Cycle Time	12	9.09			ns
Clock Pulse Width High Time	13	4			ns
Clock Pulse Width Low Time	14	4			ns
LD* Cycle Time****	15	36.36			ns
LD* Pulse Width High Time	16	15			ns
LD* Pulse Width Low Time	17	15			ns
Analog Output Rise/Fall Time****	18			4	ns
Clock and Data Feedthrough**				–23	db
VAA Supply Current***	IAA			550	mA

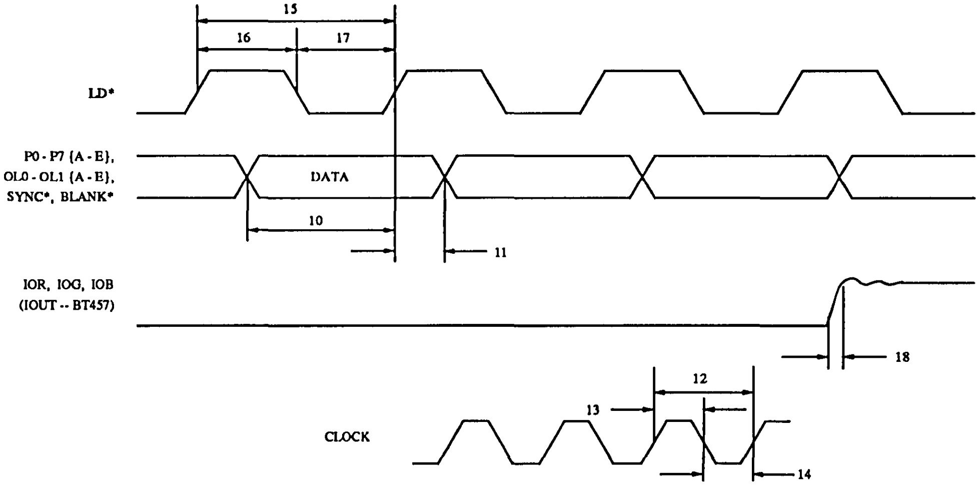
Test conditions (unless otherwise specified): 100% testing at VAA = 4.5 V and 5.5 V with TA = –55°, 25°, and 125°C. RSET = 523 Ω ± 0.1%, VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are VAA–0.8 to VAA–1.8 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Analog output with doubly terminated 50 Ω line. D0–D7 output load ~ 75 pF. See timing notes in Figure 6. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

**Derived from characterization (TA = 25°C, VAA = 5 V ± 10%), not tested. These parameters are controlled via design or process parameters and are not directly tested. They are characterized upon initial design release and upon design changes which could affect them.

***IAA (max) is measured at Fmax, with VAA = 5.5 V, 100% tested at TA = –55° C.

****Fmax 100% tested at TA = 125° C and VAA = 4.5 V.

Timing Waveforms


15
16
17
LD*
P0 - P7 {A - E},
OL0 - OL1 {A - E},
SYNC*, BLANK*
DATA
10
11
IOR, IOG, IOB
(IOUT -- BT457)
18
12
13
CLOCK
14

Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition for data only.

Note 2: Output rise/fall time measured between 10% and 90% points of full-scale transition.

Figure 6. Video Input/Output Timing.

Timing Waveforms (continued)

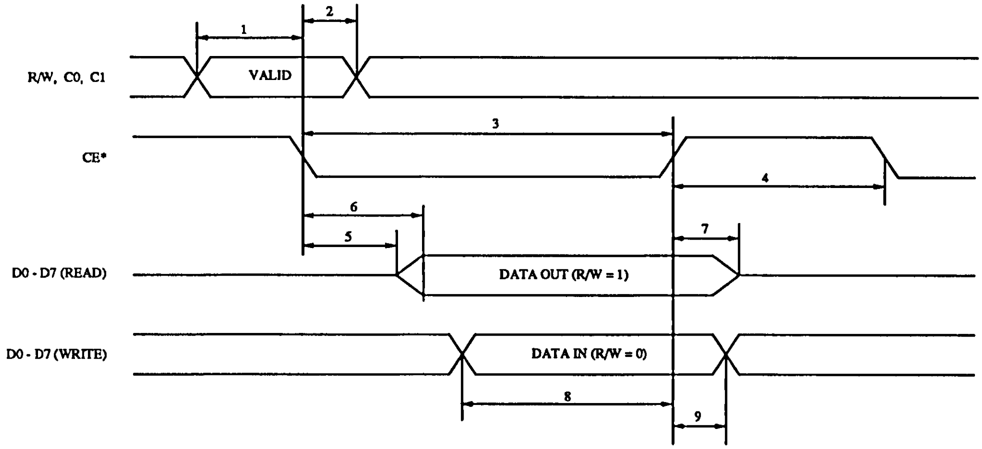

R/W, C0, C1
VALID
CE*
D0 - D7 (READ)
DATA OUT (R/W = 1)
D0 - D7 (WRITE)
DATA IN (R/W = 0)
1
2
3
4
5
6
7
8
9

Figure 7. MPU Read/Write Timing Dimensions.

Ordering Information

Model Number	MTBF* (hours)	Package	Ambient Temperature Range
Bt458SG883	$.510 \times 10^6$	84-pin Ceramic PGA	–55° to +125° C

*MTBF is calculated per MIL Handbook 217.

reliminary Information

is document contains information on a new product. The parametric information, ıough not fully characterized, is the result of testing initial devices.

Bt459

135 MHz
Monolithic CMOS
256 x 24 Color Palette
RAMDAC™

istinguishing Features

135, 110, 80 MHz Operation
1:1, 4:1, or 5:1 Multiplexed Pixel Ports
256 x 24 Color Palette RAM
16 x 24 Overlay Color Palette
1x to 16x Integer Zoom Support
1, 2, 4, or 8 Bits per Pixel
Frame Buffer Interleave Support
Pixel Panning Support
On-Chip User-Definable 64 x 64 Cursor
Programmable Setup (0 or 7.5 IRE)
X Windows Support for Overlays/Cursor
132-pin PGA or PQFP Package

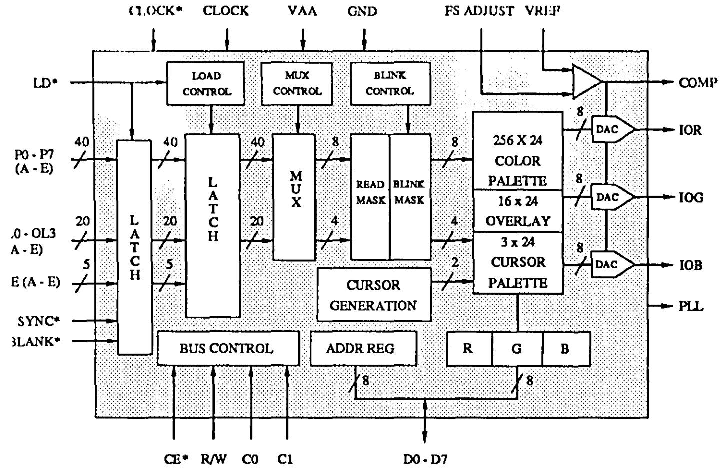
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt438, Bt439
- Bt460, Bt462, Bt468

unctional Block Diagram


CLOCK*
CLOCK
VAA
GND
FS ADJUST
VREF
LD*
LOAD CONTROL
MUX CONTROL
BLINK CONTROL
COMP
P0 - P7 (A - E)
40
40
40
8
8
8
L A T C H
L A T C H
M U X
READ MASK
BLINK MASK
256 X 24 COLOR PALETTE
16 x 24 OVERLAY
3 x 24 CURSOR PALETTE
DAC
IOR
8
DAC
IOG
8
DAC
IOB
.0 - OL3 (A - E)
20
20
20
4
4
E (A - E)
5
5
2
CURSOR GENERATION
PLL
SYNC*
3LANK*
BUS CONTROL
ADDR REG
R
G
B
8
8
CE*
R/W
C0
C1
D0 - D7

Product Description

The Bt459 triple 8-bit RAMDAC is designed specifically for high-performance, high-resolution color graphics. The multiple pixel ports and internal multiplexing enable TTL-compatible interfacing to the frame buffer, while maintaining the 135 MHz video data rates required for sophisticated color graphics.

On chip features include a 256 x 24 color palette RAM, 16 x 24 overlay color palette RAM, programmable 1:1, 4:1, or 5:1 input multiplexing of the pixel and overlay ports, bit plane masking and blinking, programmable setup (0 or 7.5 IRE), pixel panning support, 1x to 16x integer zoom support, and independent cursor generation.

Pixel data may be input as 1, 2, 4, or 8 bits per pixel. Overlay and cursor information may optionally be enabled on a pixel-by-pixel basis for X Windows hardware support.

The Bt459 has an on-chip three-color 64 x 64 pixel cursor and a three-color full-screen (or full-window) cross hair cursor.

The PLL current output enables the synchronization of multiple devices with sub-pixel resolution.

ooktree Corporation
50 Barnes Canyon Rd.
.n Diego, CA 92121
19) 452-7580 • (800) VIDEO IC
.X: 383 596 • FAX: (619) 452-1249
159001 Rev. K

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt459 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs and dual-port overlay RAM allow color updating without contention with the display refresh process.

As illustrated in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 16-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit.

To write color data, the MPU loads the address register with the address of the primary color palette RAM, overlay RAM, or cursor color register location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the primary color palette RAM, overlay RAM, or cursor color registers. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. Reading color data is similar to writing, except the MPU executes read cycles.

When accessing the color palette RAM, overlay RAM, or cursor color registers, the address register increments after each blue read or write cycle. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 12 bits of the address register (ADDR0–11) are accessible to the MPU. ADDR12–ADDR15 are always a logical zero. ADDR0 and ADDR8 correspond to D0.

The only time the address register resets to $0000 is after accessing location $0FFF (due to wraparound).

ADDR0–15	C1, C0	Addressed by MPU
$xxxx	00	address register (ADDR0–7)
$xxxx	01	address register (ADDR8–15)
$0000–$00FF	10	reserved
$0100	10	overlay color 0*
:	10	:
$010F	10	overlay color 15*
$0181	10	cursor color register 1*
:	:	cursor color register 2*
$0183	10	cursor color register 3*
$0200	10	ID register ($4A)
$0201	10	command register_0
$0202	10	command register_1
$0203	10	command register_2
$0204	10	pixel read mask register
$0205	10	reserved ($00)
$0206	10	pixel blink mask register
$0207	10	reserved ($00)
$0208	10	overlay read mask register
$0209	10	overlay blink mask register
$020A	10	interleave register
$020B	10	test register
$020C	10	red signature register
$020D	10	green signature register
$020E	10	blue signature register
$0220	10	revision register
$0300	10	cursor command register
$0301	10	cursor (x) low register
$0302	10	cursor (x) high register
$0303	10	cursor (y) low register
$0304	10	cursor (y) high register
$0305	10	window (x) low
$0306	10	window (x) high
$0307	10	window (y) low
$0308	10	window (y) high
$0309	10	window width low register
$030A	10	window width high register
$030B	10	window height low register
$030C	10	window height high register
$0400–$07FF	10	cursor RAM
$0000–$00FF	11	color palette RAM*

*Indicates requires three read/write cycles—RGB.

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Although the color palette RAM, overlay RAM, and cursor color registers are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Accessing the control registers and cursor RAM is also done through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. When accessing the control registers and cursor RAM, the address register increments following a read or write cycle.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing of the Bt459.

Bt459 Reading/Writing Color Data (RGB Mode)

To write color data, the MPU loads the address register with the address of the color palette RAM location or overlay register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the color palette RAM or the overlay registers. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. Reading color data is similar to writing, except the MPU executes read cycles.

This mode is useful if only an 8-bit data bus is available. Each Bt459 is programmed to be a red, green, or blue RAMDAC, and will respond only to the assigned color read or write cycle. In this application, the Bt459s share a common 8-bit data bus. The CE* inputs of all three Bt459s must be asserted simultaneously only during color read/write cycles and address register write cycles.

When accessing the color palette RAM, the address register resets to $00 after a blue read or write cycle to location $FF. When accessing the overlay registers, the address register increments to $04 following a blue read or write cycle to overlay register 3. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 8 bits of the address register (ADDR0–7) are accessible to the MPU.

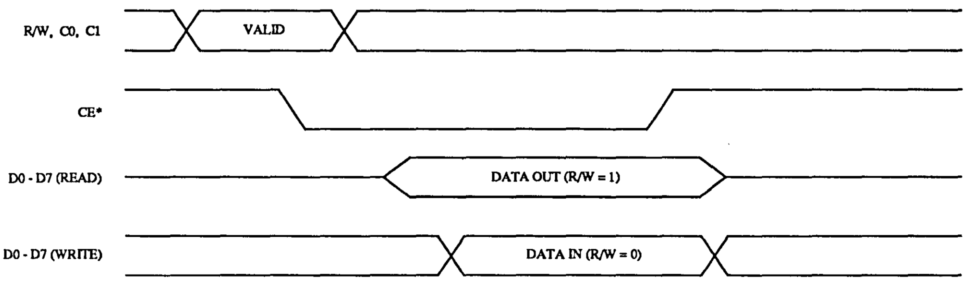


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt459 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, and overlay information, for either one, four, or five consecutive pixels, are latched into the device. Note that with this configuration, the sync and blank timing will be recognized only with one, four, or five pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing and to clock the video DRAMs.

For 4:1 or 5:1 input multiplexing, the Bt459 outputs color information each clock cycle based on the {A} inputs, followed by the {B} inputs, etc., until all four or five pixels have been output, at which point the cycle repeats. In the 1:1 input multiplexing mode, the {B}, {C}, {D}, and {E} inputs are ignored.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external circuitry.

To simplify the frame buffer interface timing, LD* may be phase shifted, in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by four or five, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than three, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*.

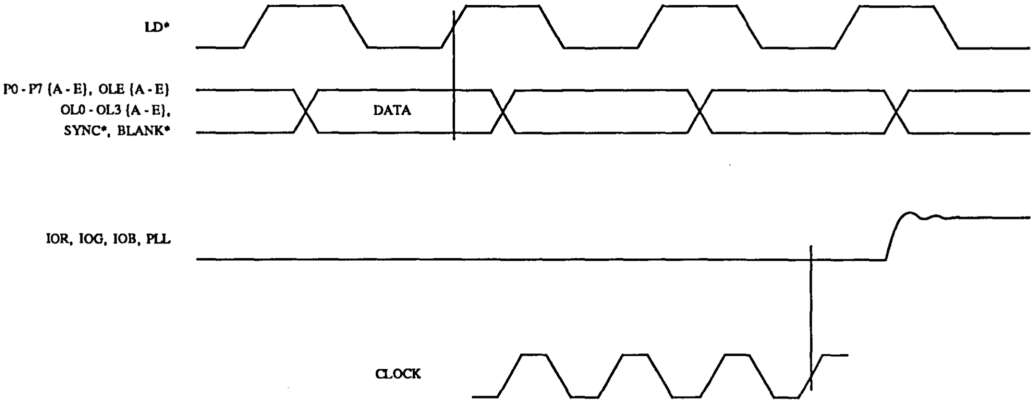


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

If 1:1 multiplexing is specified, LD* is also used for clocking the Bt459 (at a maximum of 50 MHz). The rising edge of LD* still latches the P0–P7 {A}, OL0–OL3 {A}, OLE {A}, SYNC*, and BLANK* inputs. However, analog information is output following the rising edge of LD* rather than CLOCK. Note that CLOCK must still run, but is ignored.

Read and Blink Masking

Each clock cycle, 8 bits of color information (P0–P7) and 4 bits of overlay information (OL0–OL3) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual pixel and overlay inputs may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change due to blinking does not occur during the active display time (i.e., in the middle of the screen), the Bt459 monitors the BLANK* input to determine vertical retrace intervals (any BLANK* pulse longer than 256 LD* cycles).

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAMs, and OL0 is the LSB when addressing the overlay palette RAM. Table 4 illustrates the truth table used for color selection.

Pixel Panning

To support pixel panning, command register_1 specifies by how many clock cycles to pan. Only the pixel inputs and underlays are panned—overlays and cursors are not. Panning is done by delaying SYNC* and BLANK* an additional one, two, three, or four clock cycles.

If 0 pixel panning is specified, pixel (A} is output first, followed by pixel {B}, etc., until all four or five pixels have been output, at which point the cycle repeats (note that this assumes the interleave select is pixel {A}).

If 1 pixel panning is specified, pixel (B} will be first, followed by pixel {C}, etc. Pixel {A} will have been processed during the last clock cycle of the blanking interval, and will not be seen on the display screen. At the end of the active display line, pixel {A} will be output. Pixels {B}, {C}, {D}, and {E} will be output during the blanking interval, and will not be seen on the display screen.

The process is similar for panning by two, three, or four pixels.

Note that when a panning value other than 0 pixels is specified, valid pixel data must be loaded into the Bt459 during the first LD* cycle that BLANK* is a logical zero.

In the 1:1 multiplex mode, 0 pixel panning should be specified.

Note that the cursor position does not change relative to the edge of the display screen during panning.

Bits per Pixel	Pixels per LD* (1:1 muxing)	Pixels per LD* (4:1 muxing)	Pixels per LD* (5:1 muxing)	Colors Displayed
1	8	32	40	2
2	N/A	16	20	4
4	N/A	8	10	16
8	N/A	4	5	256

Table 2. Block Mode Operation.

Circuit Description (continued)

Pixel Zoom

The Bt459 supports 1x to 16x integer zoom through the use of pixel replication. Only the P0–P7 inputs are zoomed.

If 2x zooming is specified, the {A} pixel is output for two clock cycles, followed by the {B} pixel for two clock cycles, etc. 3x zooming is similar, except each pixel is output for three clock cycles. For 1:1 multiplexing, only the {A} pixel is output.

Note that LD* must always be the pixel clock (1:1 multiplex mode) or 1/4 or 1/5 the CLOCK rate. Regardless of the zoom factor, P0–P7 data is latched every LD* cycle.

During 2x zoom, new P0–P7 data must be presented every two LD* cycles. During 3x zoom, new P0–P7 data must be presented every three LD* cycles. The pixel data must be held at the P0–P7 {A–E} inputs for the appropriate number of LD* cycles until new P0–P7 information is needed. OL0–OL3, OLE, SYNC*, and BLANK* information are still latched every LD* cycle.

Note that in the 1:1 multiplex mode, 1x zoom must be specified. Also, while in the block mode (1, 2, or 4 bits pixel), 1x zoom must be specified.

Figure 3 illustrates the zoom timing.

Block Mode Operation

The Bt459 supports loading of pixel data at 1, 2, 4, or 8 bits per pixel. Only the P0–P7 inputs are affected.

Note that LD* must always be the pixel clock (1:1 multiplex mode) or 1/4 or 1/5 the CLOCK rate, regardless of the block mode. Regardless of the block mode, P0–P7 data is latched every LD* cycle.

1 Bit per Pixel (RA1–RA7 = 0) RA0 =	2 Bits per Pixel (RA2–RA7 = 0) RA1, RA0 =	4 Bits per Pixel (RA4–RA7 = 0) RA3–RA0 =	8 Bits per Pixel RA7–RA0 =
P7A	P7A, P6A	P7A, P6A, P5A, P4A	P7A, P6A, P5A, P4A, P3A, P2A, P1A, P0A
P6A	P5A, P4A	P3A, P2A, P1A, P0A	P7B, P6B, P5B, P4B, P3B, P2B, P1B, P0B (4:1)
:	P3A, P2A	P7B, P6B, P5B, P4B (4:1)	P7C, P6C, P5C, P4C, P3C, P2C, P1C, P0C (4:1)
P0A	P1A, P0A	P3B, P2B, P1B, P0B (4:1)	P7D, P6D, P5D, P4D, P3D, P2D, P1D, P0D (4:1)
P7B (4:1)	P7B, P6B (4:1)	P7C, P6C, P5C, P4C (4:1)	P7E, P6E, P5E, P4E, P3E, P2E, P1E, P0E (5:1)
P6B (4:1)	P5B, P4B (4:1)	P3C, P2C, P1C, P0C (4:1)	
:	P3B, P2B (4:1)	P7D, P6D, P5D, P4D (4:1)	
P0B (4:1)	P1B, P0B (4:1)	P3D, P2D, P1D, P0D (4:1)	
P7C (4:1)	P7C, P6C (4:1)	P7E, P6E, P5E, P4E (5:1)	
P6C (4:1)	P5C, P4C (4:1)	P3E, P2E, P1E, P0E (5:1)	
:	P3C, P2C (4:1)		
P0C (4:1)	P1C, P0C (4:1)		
P7D (4:1)	P7D, P6D (4:1)		
P6D (4:1)	P5D, P4D (4:1)		
:	P3D, P2D (4:1)		
P0D (4:1)	P1D, P0D (4:1)		
P7E (5:1)	P7E, P6E (5:1)		
P6E (5:1)	P5E, P4E (5:1)		
:	P3E, P2E (5:1)		
P0E (5:1)	P1E, P0E (5:1)		

Note: Each line represents one pixel clock cycle. A column represents one LD* cycle loading new P0–P7 data. All entries with "4:1" descriptor are also valid for 5:1 mode.

Table 3. Block Mode Operation (RA = Color Palette RAM Address).

Circuit Description (continued)

For 8 bits per pixel, new P0–P7 information must be presented every LD* cycle. For 4 bits per pixel, new P0–P7 information must be presented every two LD* cycles. For 2 bits per pixel, new P0–P7 information must be presented every four LD* cycles. For 1 bit per pixel, new P0–P7 information must be presented every eight LD* cycles.

The pixel data must be held at the P0–P7 inputs for the appropriate number of LD* cycles until new P0–P7 information is needed. OL0–OL3, OLE, SYNC*, and BLANK* information are still latched every LD* cycle.

Tables 2 and 3 show the block mode operation, and the addressing of the color palette RAM.

Figure 4 illustrates the block mode timing (4 bits per pixel).

Note that in the 1:1 multiplex mode, 8 bits per pixel must be specified. Also, for block modes other than 8 bits per pixel, a 0 pixel interleave must be selected.

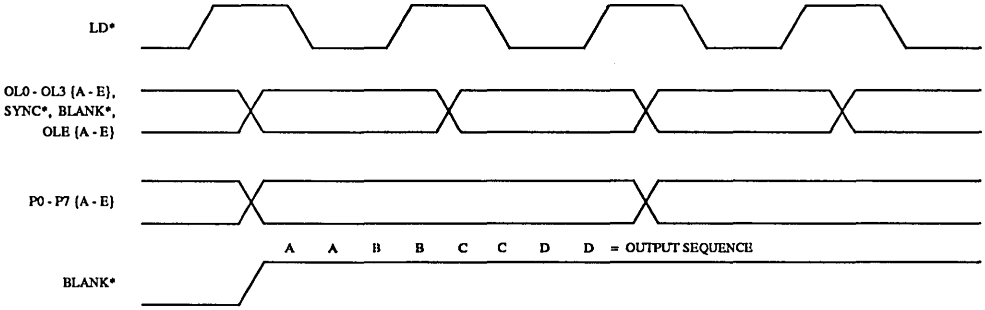

LD*
OL0 - OL3 {A - E},
SYNC*, BLANK*,
OLE {A - E}
P0 - P7 {A - E}
A A B B C C D D = OUTPUT SEQUENCE
BLANK*

Figure 3. Zoom Input Timing (8 Bits per Pixel, 2x Zoom).

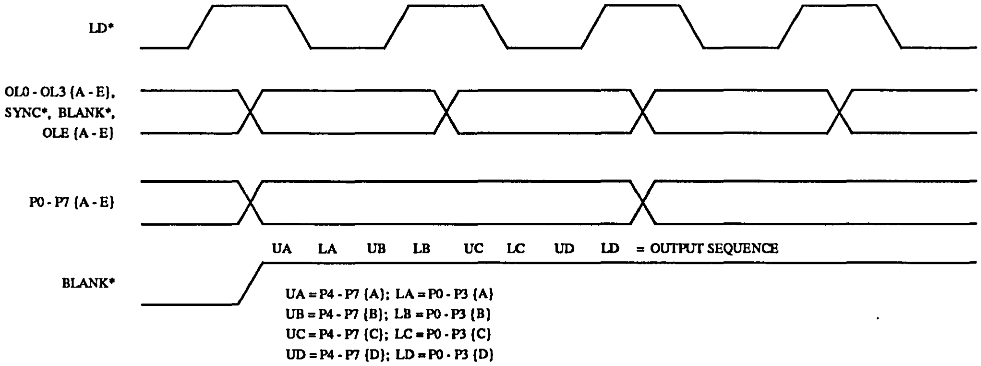

LD*
OL0 - OL3 {A - E},
SYNC*, BLANK*,
OLE {A - E}
P0 - P7 {A - E}
UA LA UB LB UC LC UD LD = OUTPUT SEQUENCE
BLANK*
UA = P4 - P7 {A}; LA = P0 - P3 {A}
UB = P4 - P7 {B}; LB = P0 - P3 {B}
UC = P4 - P7 {C}; LC = P0 - P3 {C}
UD = P4 - P7 {D}; LD = P0 - P3 {D}

Figure 4. Block Mode Input Timing (4 Bits per Pixel, 1x Zoom, 4:1 Multiplexing).

Circuit Description (continued)

On-Chip Cursor Operation

The Bt459 has an on-chip, three-color,, 64 x 64 pixel user-definable cursor. The cursor operates only with a noninterlaced video system.

The pattern for the cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. Cursor positioning is done via the cursor (x,y) register. Note that the Bt459 expects (x) to increase going right, and (y) to increase going down, as seen on the display screen. The cursor (x) position is relative to the first rising edge of LD* following the falling edge of SYNC*. The cursor (y) position is relative to the second sync pulse during vertical blanking. (See Figure 5.)

Three-Color 64 x 64 Cursor

The 64 x 64 x 2 cursor RAM provides2 bits of cursor information every clock cycle during the 64 x 64 cursor window, selecting the appropriate cursor color register as follows:

plane1	plane0	cursor color
0	0	cursor not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

(0,0) enables the color palette RAM and overlay RAM to be selected as normal. Each "plane" of cursor information may also be independently enabled or disabled for display via the cursor command register (bits CR47 and CR46).

The cursor pattern and color may be changed by changing the contents of the cursor RAM.

The cursor is centered about the value specified by the cursor (x,y) register. Thus, the cursor (x) register specifies the location of the 31st column of the 64 x 64 array (assuming the columns start with 0 for the left-most pixel and increment to 63). Similarly, the cursor (y) register specifies the location of the 31st row of the 64 x 64 array (assuming the rows start with 0 for the top-most pixel and increment to 63).

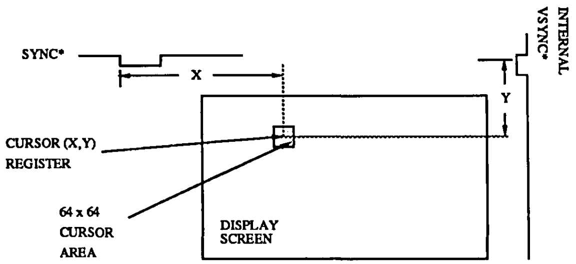


Figure 5. Cursor Positioning.

Circuit Description (continued)

Cross Hair Cursor

Cursor positioning for the three-color cross hair cursor is also done through the cursor (x,y) register. The intersection of the cross hair cursor is specified by the cursor (x,y) register. If the thickness of the cross hair cursor is greater than one pixel, the center of the intersection is the reference position.

During times that cross hair cursor information is to be displayed, the cursor command register (bits CR45 and CR44) is used to specify the color of the cross hair cursor.

CR45	CR44	cross hair color
0	0	cross hair not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

The cross hair cursor is limited to being displayed within the cross hair window, which is specified by the window (x,y), window width, and window height registers. Since the cursor (x,y) register must specify a point within the window boundaries, **it is the responsibility of the software to ensure that the cursor (x,y) register does not specify a point outside of the cross hair cursor window.**

If a full-screen cross hair cursor is desired, the window (x,y) registers should contain $0000 and the window width and height registers should contain $OFFF.

Again, the cursor (x) position is relative to the first rising edge of LD* following the falling edge of SYNC*. The cursor (y) position is relative to the second sync pulse during vertical blanking. (See Figure 6.)

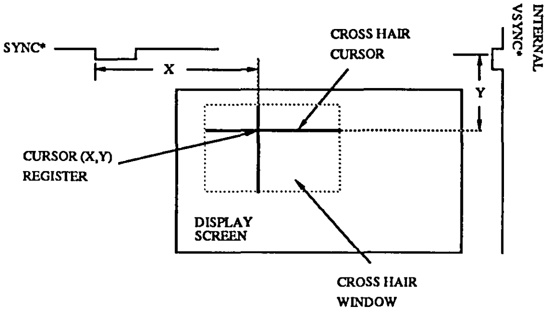


Figure 6. Cross Hair Cursor Positioning.

Circuit Description (continued)

Dual Cursor Positioning

Both the user-definable cursor and the cross hair cursor may be enabled for display simultaneously, enabling the generation of custom cross hair cursors.

As previously mentioned, the cursor (x,y) register specifies the location of bit (31, 31) of the cursor RAM. As the user-definable cursor contains an even number of pixels in the horizontal and vertical direction, it will be one pixel off from being truly centered about the cross hair cursor.

Figure 7 illustrates displaying the dual cursors.

In the 64 x 64 pixel area in which the user-definable cursor displayed, each plane of the 64 x 64 cursor may be individually logically ORed or exclusive-ORed with the cross hair cursor information. Thus, the color of the displayed cursor will be dependent on the cursor pattern, whether it is logically ORed or XORed, and the individual cursor display enable and blink enable bits.

Figure 8 shows the equivalent cursor generation circuitry.

X Windows Cursor Mode

In the X Windows mode, plane1 of the cursor RAM is a cursor display enable and plane0 of the cursor RAM selects either cursor color 2 or 3. The operation is as follows:

plane1	plane0	Selection
0	0	no cursor
0	1	no cursor
1	0	cursor color 2
1	1	cursor color 3

Refer to Figure 12 as to the organization of the cursor RAM while in the X Windows mode.

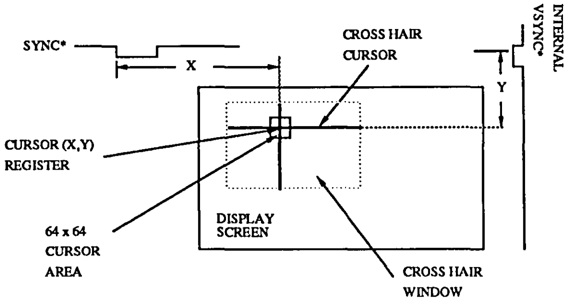


Figure 7. Dual Cursor Positioning.

Circuit Description (continued)

Overlay / Underlay Operation

The overlay inputs (OL0–OL3 and OLE) may operate in three modes: normal overlays, X Windows overlays, or provide an underlay, as shown in Tables 4 and 5.

Overlay and underlay information may be displayed on a pixel basis. Note that overlays and underlay may both be used. If using X Windows overlays, the underlay is not available.

The priority of display operation is:

cursor
overlays
pixel data
underlays

The resetting of the Bt459 to an eight-cycle pipeline delay is required for proper cursor pixel alignment.

Cursor1, Cursor0	CR30	CR22	OLE	CR05	OL0–OL3	P0–P7	Addressed by frame buffer	Overlay Mode
11	x	x	x	x	$x	$xx	cursor color 3	
10	x	x	x	x	$x	$xx	cursor color 2	
01	x	x	x	x	$x	$xx	cursor color 1	
00	0	0	x	x	$F	$xx	overlay color 15	normal
:	:	:	:	:	:	:	:	
00	0	0	x	x	$1	$xx	overlay color 1	
00	0	0	x	1	$0	$xx	overlay color 0	
00	0	0	x	0	$0	$00	RAM location $00	
00	0	0	x	0	$0	$01	RAM location $01	
:	:	:	:	:	:	:	:	
00	0	0	x	0	$0	$FF	RAM location $FF	
00	x	1	1	x	$F	$xx	overlay color 15	X Windows
:	:	:	:	:	:	:	:	
00	x	1	1	x	$1	$xx	overlay color 1	
00	x	1	1	x	$0	$xx	overlay color 0	
00	x	1	0	0	$x	$00	RAM location $00	
00	x	1	0	0	$x	$01	RAM location $01	
:	:	:	:	:	:	:	:	
00	x	1	0	0	$x	$FF	RAM location $FF	
00	1	0	x	x	$F	$xx	overlay color 15	underlay
:	:	:	:	:	:	:	:	
00	1	0	x	x	$1	$xx	overlay color 1	
00	1	0	1	x	$0	$00	overlay color 0 (underlay)	
00	1	0	0	0	$x	$00	RAM location $00	
00	1	0	x	0	$x	$01	RAM location $01	
:	:	:	:	:	:	:	:	
00	1	0	x	0	$x	$FF	RAM location $FF	

Note: Refer to Figure 8 for generation of Cursor1 and Cursor0 control bits.

Table 4. Palette and Overlay Select Truth Table.

Circuit Description (continued)

In normal overlay mode, the overlay enable inputs, OLE {A–E} are ignored, and typically only 15 overlays are available. Graphics information (P0–P7) is displayed only when no overlay information is present (OL0–OL3 = 0000).

In the X Windows overlay mode, the overlay enable inputs specify whether overlay information is present (OLE = 1) or not (OLE = 0). If OLE = 1, overlay information is displayed as determined by OL0–OL3. If OLE = 0, the OL0–OL3 inputs are ignored and P0–P7 pixel data is displayed.

In the underlay mode (CR30 = 1), if OLE = 0, pixel data is displayed. If OLE = 1, the underlay is displayed if P0–P7 = 0; if P0–P7 ≠ 0, then pixel data is displayed. Note that overlay color 0 is used for underlay color information.

	P0-P7 Pixel Inputs						
	1:1 Mux	Block Mode	Interleave	Panning	Zooming	Overlays	Underlay
Block Mode	no	-	yes	yes	n/s	n/a	n/a
Interleave	n/s	yes	-	yes	yes	yes	yes
Panning	n/s	n/s	yes	-	yes	n/a	yes
Zooming	n/s	n/s	yes	yes	-	n/a	n/a
Overlays	yes	yes	yes	n/a	n/a	-	yes
Underlay	yes	yes	yes	yes	n/a	yes	-
Cursor	n/a	n/a	n/a	n/a	n/a	n/a	n/a

yes: fully functional together.
n/s: functions not supported together.
n/a: functions operate together, but do not affect each other.

Table 5. Features and Function Compatibility Table.

Circuit Description (continued)

Video Generation

Every clock cycle, the selected 24 bits of color information are presented to the three 8-bit D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 9 and 10. Command register2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated, and whether or not sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converters produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 6 and 7 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt459 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

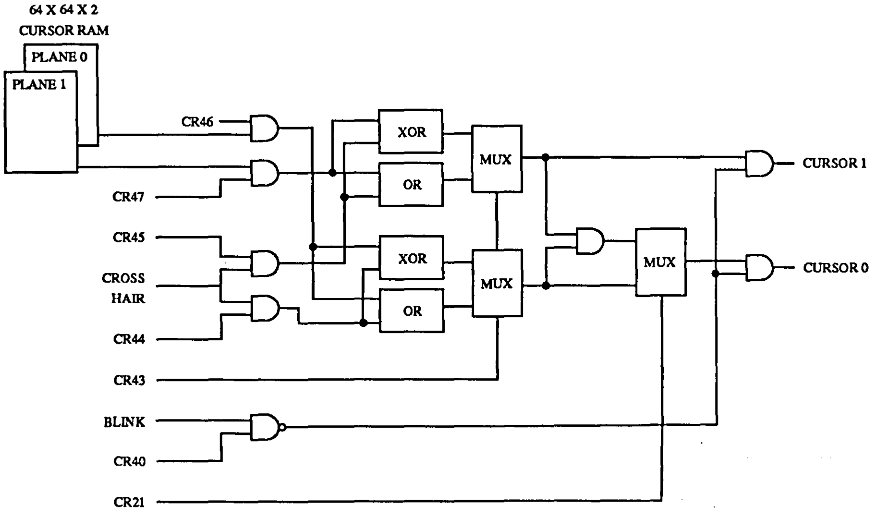
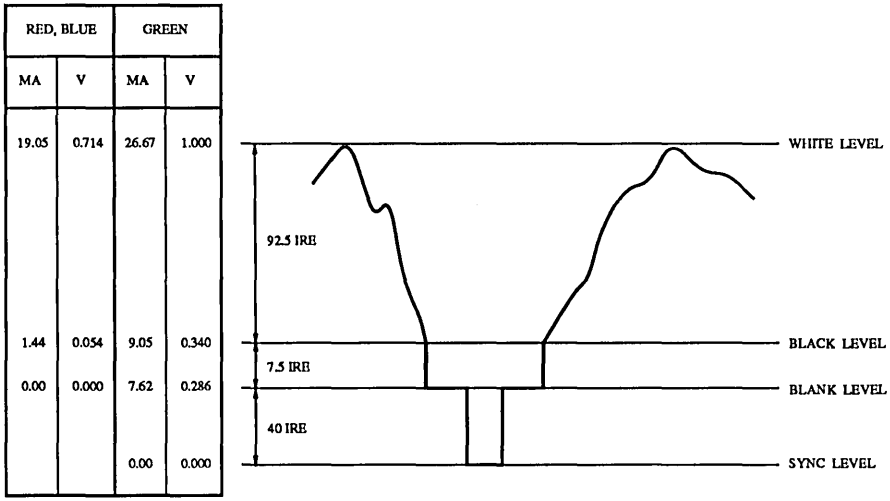


Figure 8. Cursor Control Circuitry.

Circuit Description (continued)


RED, BLUE
GREEN
MA
V
MA
V
19.05
0.714
26.67
1.000
1.44
0.054
9.05
0.340
0.00
0.000
7.62
0.286
0.00
0.000
92.5 IRE
7.5 IRE
40 IRE
WHITE LEVEL
BLACK LEVEL
BLANK LEVEL
SYNC LEVEL

Note: 75 Ω doubly terminated load, RSET = 523 Ω, VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances assumed on all levels.

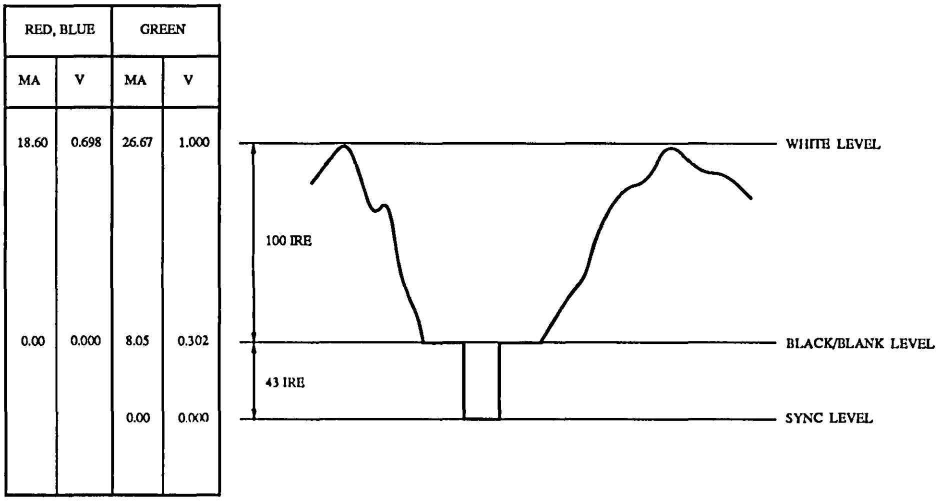
Figure 9. Composite Video Output Waveform (SETUP = 7.5 IRE).

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 523 Ω, VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 6. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)


RED, BLUE
GREEN
MA
V
MA
V
18.60
0.698
26.67
1.000
0.00
0.000
8.05
0.302
0.00
0.000
WHITE LEVEL
100 IRE
BLACK/BLANK LEVEL
43 IRE
SYNC LEVEL

Note: 75 Ω doubly terminated load, RSET = 495 Ω, VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances assumed on all levels.

Figure 10. Composite Video Output Waveform (SETUP = 0 IRE).

Description	IOG (mA)	IOR, IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 495 Ω, VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 7. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register_0

This register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to data bus bit D0.

CR07, CR06	Multiplex select (00) reserved (01) 4:1 multiplexing (10) 1:1 multiplexing (11) 5:1 multiplexing	These bits specify whether 1:1, 4:1, or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 4:1 is specified, the {E} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be 1/4 the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be 1/5 the CLOCK rate. If 1:1 is specified, the {B}, {C}, {D}, and {E} inputs are ignored. Note that in the 1:1 multiplex mode, the maximum clock rate is 66 MHz. LD* is used for the pixel clock. Although CLOCK is ignored in the 1:1 mode, it must remain running. Note that it is possible to reset the pipeline delay of the Bt459 to a fixed eight clock cycles. In this instance, each time the input multiplexing is changed, the Bt459 must again be reset to a fixed pipeline delay.
CR05	Overlay 0 enable (0) use color palette RAM (1) use overlay color 0	When in the normal overlay mode, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information when the overlay inputs are $0. See Table 4.
CR04	reserved (logical zero)	
CR03, CR02	Blink rate selection (00) 16 on, 48 off (25/75) (01) 16 on, 16 off (50/50) (10) 32 on, 32 off (50/50) (11) 64 on, 64 off (50/50)	These 2 bits specify the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (% on/off). The counters that determine the blink rate are reset when command register_0 is written to.
CR01, CR00	Block mode (00) 8 bits per pixel (01) 4 bits per pixel (10) 2 bits per pixel (11) 1 bit per pixel	These bits specify whether the pixel data is input as 1, 2, 4, or 8 bits per pixel. Note that only the P0–P7 inputs are affected.

Internal Registers (continued)

Command Register_1

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0.

CR17–CR15	Pan select (000) 0 pixels {pixel A} (001) 1 pixel {pixel B} (010) 2 pixels {pixel C} (011) 3 pixels {pixel D} (100) 4 pixels {pixel E} (101) reserved (110) reserved (111) reserved	These bits specify the number of pixels to be panned. These bits are typically modified only during the vertical retrace interval, and should be set to 000 in the 1:1 multiplex mode. The {pixel A} indicates pixel A will be output first following the blanking interval, {pixel B} indicates pixel B will be output first, etc. Note that only pixel and underlay information is panned. Overlay and cursor information is not panned. In the 1:1 multiplex mode, 0 pixels should be specified.
CR14	reserved (logical zero)	
CR13–CR10	Zoom factor (0000) 1x (0001) 2x : (1111) 16x	These bits specify the amount of zooming to implement. For 2x zoom, pixel {A} is output for two clock cycles, followed by pixel {B} for two clock cycles, etc. For 3x zoom, pixel {A} is output for three clock cycles, etc. In the 1:1 multiplex mode, only the {A} pixels are output, and 1x zoom should be selected. Note that only P0–P7 are zoomed.

Internal Registers (continued)

Command Register_2

This register may be written to or read by the MPU at any time and is not initialized. CR20 corresponds to data bus bit D0.

CR27	Sync enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto IOG (logical one) or not (logical zero).
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. 0 IRE specifies that the black and blank levels are the same.
CR25, CR24	Load palette RAM select (00) normal (01) red RAMDAC (10) green RAMDAC (11) blue RAMDAC	If (00) is specified, color data is loaded into the Bt459 using three write cycles (red, green, and blue), and color data is output using three read cycles (red, green, and blue). Modes (01), (10), and (11) enable the Bt459 to emulate a single-channel RAMDAC using only the green channel. The Bt459 expects color data to be input and output using (red, green, blue) cycles. The exact value indicates during which one of the three color cycles it is to load or output color information. The value is loaded into or read from the green color palette RAM.
CR23	PLL select (0) SYNC* (1) BLANK*	This bit specifies whether the PLL output uses SYNC* or BLANK* for generating PLL information.
CR22	X Windows overlay select (0) normal overlays (1) X-windows overlays	This bit specifies whether the overlays are to operate normally (logical zero) or in an X Windows environment (logical one).
CR21	X Windows cursor select (0) normal cursor (1) X Windows cursor	This bit specifies whether the cursor is to operate normally (logical zero) or in an X Windows compatible mode (logical one).
CR20	Test mode select (0) signature analysis test (1) data strobe test	This bit determines the method of high-speed test used. The signature analysis registers are used to hold the test result for both test methods.

Internal Registers (continued)

Interleave Register

This register may be written to or read by the MPU at any time and is not initialized. CR30 corresponds to data bus bit D0. The interleave register is for support of frame buffer systems configured for interleave operation.

CR37–CR35	Interleave select (000) 0 pixels (001) 1 pixel (010) 2 pixels (011) 3 pixels (100) 4 pixels (101) reserved (110) reserved (111) reserved	These bits specify the order in which the pixels are to be output, as shown in Table 8. The order is repeated every LD* cycle for a given scan line. Thus, if the output sequence is DABC, it is that sequence for all pixels on that scan line. The phrase "repeats every x" in table 8 means that the output sequence repeats every x scan lines. Thus, for 4:1 multiplexing and a 1 pixel interleave select, ABCD would be repeated every 4th scan line. In the 1:1 input multiplex mode, a value of 0 pixels (000) must be specified.
CR34–CR32	First pixel select (000) pixel {A} (001) pixel {B} (010) pixel {C} (011) pixel {D} (100) pixel {E} (101) reserved (110) reserved (111) reserved	These bits are used to support panning in the Y direction with an interleaved frame buffer. Due to the interleave capability, it is necessary to specify the value of the first pixel on the first scan line following a vertical retrace. The pixel {E} selection is only used in the 5:1 multiplex mode. These bits are ignored in the 1:1 multiplex mode.
CR31	Overlay interleave enable (0) interleaving disabled (1) interleave enabled	This bit specifies whether or not OL0–OL3 and OLE are to be interleaved or not. If interleaving is enabled, the interleave factor and first pixel selection are the same as for P0–P7. If interleaving is disabled, pixel {A} is always output first and no interleaving occurs.
CR30	Underlay enable (0) underlay disabled (1) underlay enabled	If command bit CR22 is a logical zero, this bit is used to enable or disable the underlay from being displayed. If CR22 is a logical one, this bit is ignored. If the underlay is enabled (and CR22 is a logical zero), the OLE inputs function as follows: If OLE = 0, P0–P7 data is displayed. If OLE = 1, the underlay is displayed if P0–P7 = 0, if P0–P7 ≠ 0 then normal pixel data is displayed. The underlay uses overlay color 0 to provide underlay color information.

Internal Registers (continued)

Interleave Register (continued)

	5:1 multiplexing		4:1 multiplexing	
interleave select	output sequence	scan line number	output sequence	scan line number
0	ABCDE	each line	ABCD	each line
1	ABCDE BCDEA CDEAB DEABC EABCD	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD BCDA CDAB DABC	n n + 1 n + 2 n + 3 (repeats every 4)
2	ABCDE CDEAB EABCD BCDEA DEABC	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD CDAB ABCD CDAB	n n + 1 n + 2 n + 3 (repeats every 2)
3	ABCDE DEABC BCDEA EABCD CDEAB	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD DABC CDAB BCDA	n n + 1 n + 2 n + 3 (repeats every 4)
4	ABCDE EABCD DEABC CDEAB BCDEA	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	invalid	invalid

Table 8. Interleave Operation (First Pixel Select = Pixel A).

Internal Registers (continued)

Interleave Zoom Enable

If zooming while interleaving, the IZE* input pin indicates when to change the interleave sequence.

For example, while interleaving with 3x zoom, the IZE* pin should be a logical zero during the blanking interval of every third scan line (as shown in Figure 11). IZE* may be asserted coincident with the falling edge of BLANK*, but must remain low at least 16 LD* cycles after the falling edge of BLANK*.

If no zooming is done (1x zoom), the IZE* should always be a logical zero or be connected directly to GND.

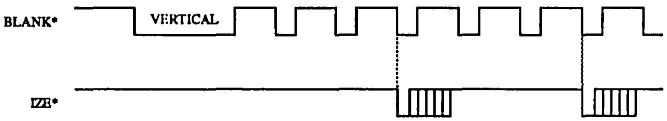


Figure 11. Interleave and Zoom Operation (3x Zoom Example).

Internal Registers (continued)

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt459, the value read by the MPU will be $4A. Data written to this register is ignored.

Pixel Read Mask Register

The 8-bit pixel read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P0.

Pixel Blink Mask Register

The 8-bit pixel blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P0.

Overlay Read Mask Register

The 8-bit overlay read mask register is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette RAM. D0 corresponds to overlay plane 0 (OL0 {A–E}) and D3 corresponds to overlay plane 3 (OL3 {A–E}). Bits D0–D3 are logically ANDed with the corresponding overlay plane input. D4–D7 are always a logical zero.

This register may be written to or read by the MPU at any time and is not initialized.

Overlay Blink Mask Register

The 8-bit overlay blink mask register is used to enable (logical one) or disable (logical zero) an overlay plane from blinking at the blink rate and duty cycle specified by command register_0. D0 corresponds to overlay plane 0 (OL0 {A–E}) and D3 corresponds to overlay plane 3 (OL3 {A–E}). In order for an overlay plane to blink, the corresponding bit in the overlay read mask register must be a logical one. D4–D7 are always a logical zero.

This register may be written to or read by the MPU at any time and is not initialized.

Revision Register (Revision B only)

This 8-bit register is a read-only register, specifying the revision of the Bt459. The four most significant bits signify the revision letter B, in hexidecimal form. The four least significant bits do not represent any value and should be ignored. Data written to this register is ignored.

Since Revision A device does not have a revision register, address $0220 will contain the last data read to or written from the internal bus.

Internal Registers (continued)

Red, Green, and Blue Signature Registers

Signature Operation

These three 8-bit signature registers (one each for red, green and blue) may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the three registers are concatenated and a 24-bit signature is acquired. The MPU may read from or write to the signature registers while BLANK* is a logical zero to load the seed value.

By loading a test display into the frame buffer, a deterministic value for the red, green, and blue signature registers will be read from these registers if all circuitry is working properly. Refer to the Application Information test register section for more information.

Data Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the signature registers changes slightly. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

Each LD* cycle, the three signature registers capture the color values being presented to the DACs. As only one of the (A–E) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–E) is to be captured.

Internal Registers (continued)

Test Register

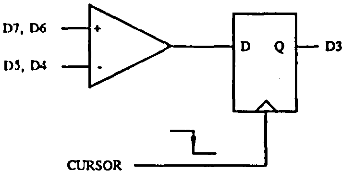
This 8-bit register is used for testing the Bt459. If 1:1 pixel multiplexing is specified, signature analysis is done on every pixel; if 4:1 pixel multiplexing is specified, signature analysis is done on every fourth pixel; if 5:1 pixel multiplexing is specified, signature analysis is done on every fifth pixel. D0–D2 are used for 4:1 and 5:1 multiplexing to specify whether to use the A, B, C, D, or E pixel inputs, as follows:

D2–D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	pixel E
101	reserved
110	reserved
111	reserved

In 1:1 multiplexing mode, D0–D2 should select pixel A.

D3–D7 are used to compare the analog RGB outputs to each other and to a 150 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs or not, and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	145 mV ref. select	result



D7–D4		If D3 = 1	If D3 = 0
0000	normal operation	-	-
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 150 mV reference	red > 150 mV	red < 145 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 150 mV reference	green > 150 mV	green < 145 mV

The above table lists the valid comparison combinations. A logical one enables that function to be compared; the result is D3. The comparison result is strobed into D3 on the left edge of the 64 x 64 cursor area. The output levels of the DACs should be constant for 5 µs before the left edge of the cursor.

For normal operation, D3–D7 must be a logical zero.

Internal Registers (continued)

Cursor Command Register

This command register is used to control various cursor functions of the Bt459. It is not initialized, and may be written to or read by the MPU at any time. CR40 corresponds to data bus bit D0.

CR47	64 x 64 cursor plane1 display enable (0) disable plane1 (1) enable plane1	Specifies whether plane1 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR46	64 x 64 cursor plane0 display enable (0) disable plane0 (1) enable plane0	Specifies whether plane0 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR45	Cross hair cursor plane1 display enable (0) disable plane1 (1) enable plane1	Specifies whether plane1 of the cross hair cursor is to be displayed (logical one) or not (logical zero).
CR44	Cross hair cursor plane0 display enable (0) disable plane0 (1) enable plane0	Specifies whether plane0 of the cross hair cursor is to be displayed (logical one) or not (logical zero). Note that plane0 and plane1 contain the same information.
CR43	Cursor format (0) XOR (1) OR	If both the 64 x 64 cursor and the cross hair cursor are enabled for display, this bit specifies whether the contents of the cursor RAM are to be logically exclusive-ORed (logical zero) or ORed (logical one) with the cross hair cursor.
CR42, CR41	Cross hair thickness (00) 1 pixel (01) 3 pixels (10) 5 pixels (11) 7 pixels	This bit specifies whether the vertical and horizontal thickness of the cross hair is one, three, five, or seven pixels. The segments are centered about the value in the cursor (x,y) register.
CR40	Cursor blink enable (0) blinking disabled (1) blinking enabled	This bit specifies whether the cursor is to blink (logical one) or not (logical zero). If both cursors are displayed, both will blink. The blink rate and duty cycle are as specified by command register_0.

Internal Registers (continued)

Cursor (x,y) Registers

These registers are used to specify the (x,y) coordinate of the center of the 64 x 64 pixel cursor window, or the intersection of the cross hair cursor. The cursor (x) register is made up of the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register is made up of the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). They are not initialized and may be written to or read by the MPU at any time. The cursor position is not updated until the vertical retrace interval after CYHR has been written to by the MPU.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are always a logical zero.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Cx = desired display screen (x) position + H–P

where

P = 37 if 1:1 input multiplexing, 52 if 4:1 input multiplexing, 57 if 5:1 input multiplexing
H = number of pixels between the first rising edge of LD* following the falling edge of SYNC* to active video.

Values from $0000 to $0FFF may be written into the cursor (x) register.

The cursor (y) value to be written is calculated as follows:

Cy = desired display screen (y) position + V–32

where

V = number of scan lines from the second sync pulse during vertical blanking to active video.

Values from $0FC0 (–64) to $0FBF (+4031) may be loaded into the cursor (y) register. The negative values ($0FC0 to $0FFF) are used in situations where V < 32, and the cursor must be moved off the top of the screen.

Internal Registers (continued)

Window (x,y) Registers

These registers are used to specify the (x,y) coordinate of the upper left corner of the cross hair cursor window. The window (x) register is made up of the window (x) low register (WXLR) and the window (x) high register (WXHR); the window (y) register is made up of the window (y) low register (WYLR) and the window (y) high register (WYHR). They are not initialized and may be written to or read by the MPU at any time. The window position is not updated until the vertical retrace interval after WYHR has been written to by the MPU.

WXLR and WXHR are cascaded to form a 12-bit window (x) register. Similarly, WYLR and WYHR are cascaded to form a 12-bit window (y) register. Bits D4–D7 of WXHR and WYHR are always a logical zero.

	Window (x) High (WXHR)				Window (x) Low (WXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window (y) High (WYHR)				Window (y) Low (WYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The window (x) value to be written is calculated as follows:

Wx = desired display screen (x) position + H–P

where

P = 5 if 1:1 input multiplexing, 20 if 4:1 input multiplexing, 25 if 5:1 input multiplexing
H = number of pixels between the first rising edge of LD* following the falling edge of HSYNC* to active video.

The window (y) value to be written is calculated as follows:

Wy = desired display screen (y) position + V

where

V = number of scan lines from the second sync pulse during vertical blanking to active video.

Values from $0000 to $0FFF may be written to the window (x) and window (y) registers. A full-screen cross hair is implemented by loading the window (x,y) registers with $0000 and the window width and height registers with $0FFF.

Internal Registers (continued)

Window Width and Height Registers

These registers are used to specify the width and height (in pixels) of the cross hair cursor window. The window width register is made up of the window width low register (WWLR) and the window width high register (WWHR); the window height register is made up of the window height low register (WHLR) and the window height high register (WHHR). They are not initialized and may be written to or read by the MPU at any time. The window width and height are not updated until the vertical retrace interval after WHHR has been written to by the MPU.

WWLR and WWHR are cascaded to form a 12-bit window width register. Similarly, WHLR and WHHR are cascaded to form a 12-bit window height register. Bits D4–D7 of WWHR and WHHR are always a logical zero.

	Window Width High (WWHR)				Window Width Low (WWLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window Height High (WHHR)				Window Height Low (WHLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The actual window width is 2, 8, or 10 pixels more than the value specified by the window width register, depending on whether 1:1, 4:1, or 5:1 input multiplexing is specified. The actual window height is 2 pixels more than the value specified by the window height register. Therefore, the minimum window width is 2, 8, or 10 pixels, for 1:1, 4:1, and 5:1 multiplexing, respectively, and the minimum window height is two pixels.

Values from $0000 to $0FFF may be written to the window width and height registers.

Internal Registers (continued)

Cursor RAM

This 64 x 64 x 2 RAM is used to define the pixel pattern within the 64 x 64 pixel cursor window, and is not initialized.

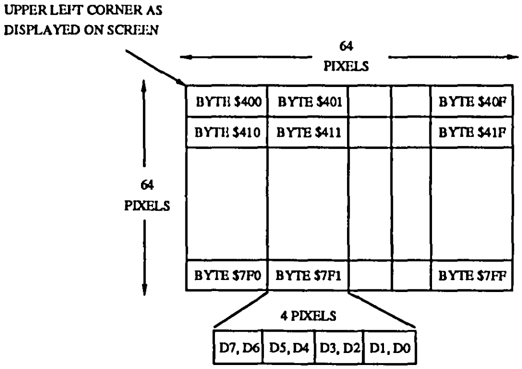
For Revision A, the cursor RAM should not be written to by the MPU during the horizontal sync time and for the two LD* cycles after the end of the horizontal sync. The cursor RAM may otherwise be written to or read by the MPU at any time without contention. If writing to the cursor RAM asynchronously to horizontal sync, it is recommended that the user position the cursor off-screen in the Y direction (write to the cursor (y) registers and wait for the vertical sync interval to move the cursor off-screen), write to the cursor RAM, then reposition the cursor back to the original position. An alternative is to perform a write then read sequence, and if the correct cursor RAM data was not written, perform another write then read sequence. Since the contention occurs only during horizontal sync at the Y locations coincident with the cursor, the second write/read sequence bypasses the window of time when cursor RAM is in contention.

For Revision B, cursor contention has been eliminated. The cursor RAM may be written to or read by the MPU at any time without contention.

During MPU accesses to the cursor RAM, the address register is used to address the cursor RAM. Figure 12 illustrates the internal format of the cursor RAM, as it appears on the display screen. Addressing starts at location $400 as shown in Table 1.

Note that in the X Windows mode, plane1 serves as a cursor display enable while plane0 selects one of two cursor colors (if enabled).

Note: in both modes of operation, plane1 = D7, D5, D3, D1; plane0 = D6, D4, D2, D0.



Normal Mode:

00 = color palette or overlay RAM
01 = cursor color 1
10 = cursor color 2
11 = cursor color 3

X-Windows Mode:

00 = color palette or overlay RAM
01 = color palette or overlay RAM
10 = cursor color 2
11 = cursor color 3

Figure 12. Cursor RAM as Displayed on the Screen.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as illustrated in Tables 6 and 7. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control inputs (TTL compatible). A logical zero typically switches off a 40 IRE current source on the IOG output (see Figures 9 and 10). SYNC* does not override any other control or data input, as shown in Tables 6 and 7; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0–P7 {A–E}, OL0–OL3 {A–E}, OLE {A–E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD*, while it is the output clock (1:1 multiplex mode) or is 1/4 or 1/5 of CLOCK, may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle, within the limits specified by the AC Characteristics section.
P0–P7 {A–E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which location of the color palette RAM is to be used to provide color information (see Table 4). Either one, four, or five consecutive pixels (up to 8 bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Note that typically the {A} pixel is output first, followed by the {B} pixel, etc., until all one, four, or five pixels have been output, at which point the cycle repeats.
OL0–OL3 {A–E}	Overlay select inputs (TTL compatible). These inputs are latched on the rising edge of LD* and, in conjunction with CR05 in command register_0, specify which palette is to be used for color information, as illustrated in Table 4. When accessing the overlay palette RAM, the P0–P7 {A–E} inputs are ignored. Overlay information (up to 4 bits per pixel) for either one, four, or five consecutive pixels are input through this port. Unused inputs should be connected to GND.
OLE {A–E}	Overlay enable inputs (TTL compatible). In the X Windows mode for overlays, a logical one indicates overlay information is to be displayed. A logical zero indicates to display P0–P7 information. In the normal mode for overlays, these inputs are ignored. They are latched on the rising edge of LD*. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 13). All outputs, whether used or not, should have the same output load.
PLL	Phase lock loop output current. This high-impedance current source is used to enable multiple Bt459s to be synchronized with sub-pixel resolution when used with an external PLL. A logical one for SYNC* or BLANK* (as specified by CR23 in command register_2) results in no current being output onto this pin, while a logical zero results in the following current being output: PLL (mA) = 3,227 * VREF (V) / RSET (Ω) If sub-pixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 Ω).
IZE*	Interleave zoom enable input (TTL compatible). This input should be a logical zero for a minimum of 16 LD* cycles after the falling edge of BLANK* during scan lines that require an interleave shift. If zoom while interleaving is not supported, this pin may be connected directly to GND.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 13). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. *Refer to PC Layout Considerations for critical layout criteria.*
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 13). Note that the IRE relationships in Figures 9 and 10 are maintained, regardless of the full-scale output current.

The relationship between RSET and the full-scale output current on IOG is:

$$RSET\ (\Omega) = K1 * VREF\ (V) / IOG\ (mA)$$

The full-scale output current on IOR and IOB for a given RSET is:

$$IOR, IOB\ (mA) = K2 * VREF\ (V) / RSET\ (\Omega)$$

where K1 and K2 are defined as:

Setup	IOG	IOR, IOB
7.5 IRE	K1 = 11,294	K2 = 8,067
0 IRE	K1 = 10,684	K2 = 7,457

Pin Name	Description
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 13, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 13. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Care should be taken to avoid glitches on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.

Pin Descriptions (continued)—132-pin PGA Package

Signal	Pin Number
BLANK*	L1
SYNC*	K3
LD*	A5
CLOCK	K1
CLOCK*	K2
IZE*	B5
P0A	E3
P0B	D2
P0C	D1
P0D	E2
P0E	F3
P1A	A1
P1B	D3
P1C	C2
P1D	B1
P1E	C1
P2A	A3
P2B	B3
P2C	A2
P2D	C3
P2E	B2
P3A	A8
P3B	A7
P3C	B7
P3D	A6
P3E	B6
P4A	C9
P4B	B9
P4C	A9
P4D	C8
P4E	B8
P5A	B11
P5B	A11
P5C	C10
P5D	B10
P5E	A10
P6A	A14
P6B	A13
P6C	B12
P6D	C11
P6E	A12
P7A	E13
P7B	E12
P7C	D14
P7D	D13
P7E	D12

Signal	Pin Number
OL0A	E1
OL0B	F2
OL0C	F1
OL0D	G3
OL0E	G2
OL1A	M1
OL1B	L2
OL1C	N1
OL1D	L3
OL1E	M2
OL2A	M3
OL2B	N2
OL2C	P1
OL2D	P2
OL2E	N3
OL3A	M4
OL3B	P3
OL3C	N4
OL3D	P4
OL3E	M5
OLEA	N5
OLEB	P5
OLEC	M6
OLED	N6
OLEE	P6
IOG	P10
IOB	P11
IOR	N10
PLL	N11
VAA	J1
VAA	J2
VAA	J3
VAA	C6
VAA	F12
VAA	M9
VAA	P7
VAA	P8
VAA	N8

Signal	Pin Number
GND	H1
GND	H2
GND	H3
GND	C7
GND	G12
GND	M8
GND	M7
GND	N7
COMP	N9
FS ADJUST	M10
VREF	P9
CE*	P13
R/W	N12
C1	P12
C0	M11
D0	L13
D1	M14
D2	L12
D3	M13
D4	N14
D5	P14
D6	N13
D7	M12
reserved	G14
reserved	G13
reserved	F14
reserved	F13
reserved	E14
reserved	J13
reserved	J14
reserved	H12
reserved	H13
reserved	H14
reserved	C5
reserved	A4
reserved	B4
reserved	C4
reserved	C14
reserved	C13
reserved	B14
reserved	C12
reserved	B13
reserved	L14
reserved	K12
reserved	J12
reserved	K14
reserved	K13

Pin Descriptions (continued)—132-pin PGA Package

Bt459

(TOP VIEW)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
14	P6A	N/C	N/C	P7C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	D1	D4	D5
13	P6B	N/C	N/C	P7D	P7A	N/C	N/C	N/C	N/C	N/C	D0	D3	D6	CE*
12	P6E	P6C	N/C	P7E	P7B	VAA	GND	N/C	N/C	N/C	D2	D7	R/W	C1
11	P5B	P5A	P6D									C0	PLL	IOB
10	P5E	P5D	P5C									FS ADJ	IOR	IOG
9	P4C	P4B	P4A									VAA	COMP	VREF
8	P3A	P4E	P4D									GND	VAA	VAA
7	P3B	P3C	GND									GND	GND	VAA
6	P3D	P3E	VAA									OLEC	OLED	OLEE
5	LD*	IZE*	N/C									OL3E	OLEA	OLEB
4	N/C	N/C	N/C									OL3A	OL3C	OL3D
3	P2A	P2B	P2D	P1B	P0A	P0E	OL0D	GND	VAA	SYNC*	OL1D	OL2A	OL2E	OL3B
2	P2C	P2E	P1C	P0B	P0D	OL0B	OL0E	GND	VAA	CLK*	OL1B	OL1E	OL2B	OL2D
1	P1A	P1D	P1E	P0C	OL0A	OL0C	N/C	GND	VAA	CLK	BLK*	OL1A	OL1C	OL2C

alignment marker (on top)

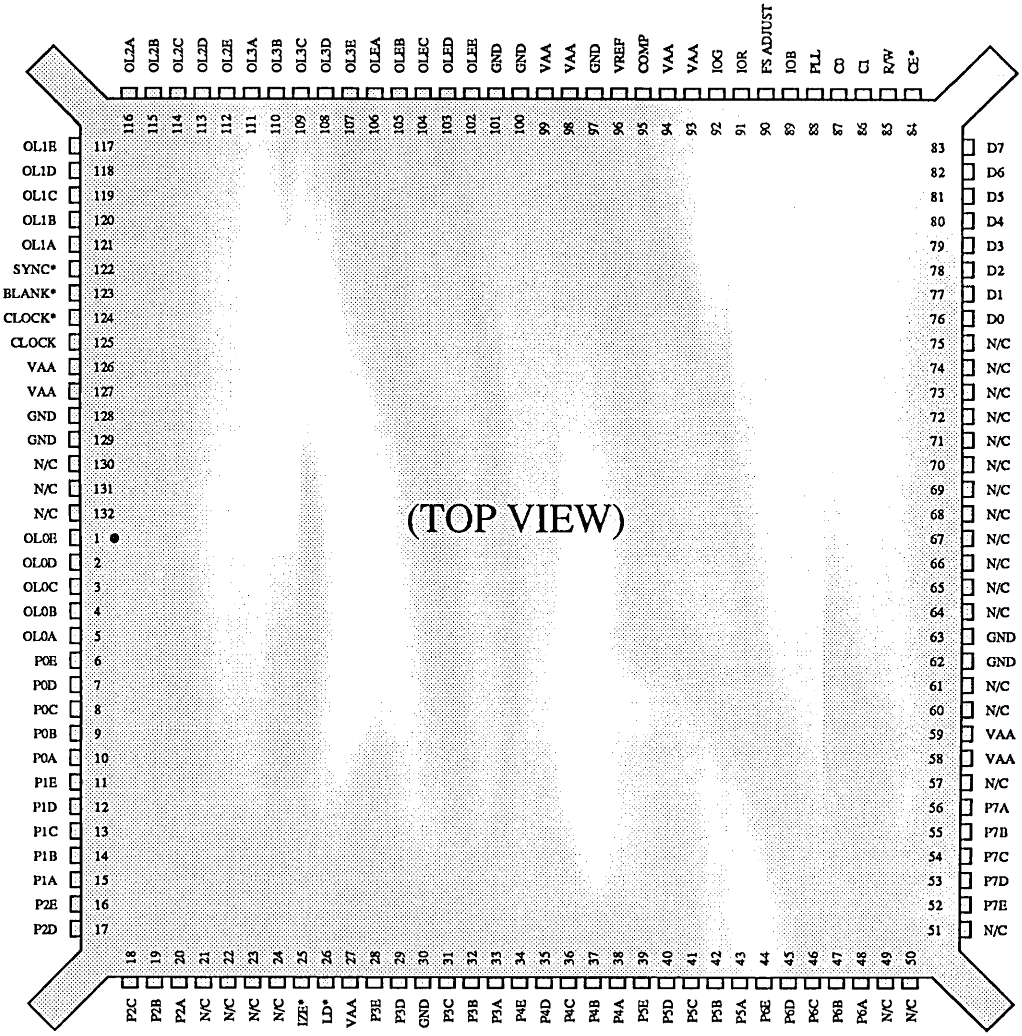
(BOTTOM VIEW)

	P	N	M	L	K	J	H	G	F	E	D	C	B	A
14	D5	D4	D1	N/C	N/C	N/C	N/C	N/C	N/C	N/C	P7C	N/C	N/C	P6A
13	CE*	D6	D3	D0	N/C	N/C	N/C	N/C	N/C	P7A	P7D	N/C	N/C	P6B
12	C1	R/W	D7	D2	N/C	N/C	N/C	GND	VAA	P7B	P7E	N/C	P6C	P6E
11	IOB	PLL	C0									P6D	P5A	P5B
10	IOG	IOR	FS ADJ									P5C	P5D	P5E
9	VREF	COMP	VAA									P4A	P4B	P4C
8	VAA	VAA	GND									P4D	P4E	P3A
7	VAA	GND	GND									GND	P3C	P3B
6	OLEE	OLED	OLEC									VAA	P3E	P3D
5	OLEB	OLEA	OL3E									N/C	IZE*	LD*
4	OL3D	OL3C	OL3A									N/C	N/C	N/C
3	OL3B	OL2E	OL2A	OL1D	SYNC*	VAA	GND	OL0D	P0E	P0A	P1B	P2D	P2B	P2A
2	OL2D	OL2B	OL1E	OL1B	CLK*	VAA	GND	OL0E	OL0B	P0D	P0B	P1C	P2E	P2C
1	OL2C	OL1C	OL1A	BLK*	CLK	VAA	GND	N/C	OL0C	OL0A	P0C	P1E	P1D	P1A

Pin Descriptions (continued)—132-pin PQFP Package

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	OL0E	44	P6E	88	PLL
2	OL0D	45	P6D	89	IOB
3	OL0C	46	P6C		
4	OL0B	47	P6B	90	FS ADJUST
5	OL0A	48	P6A	91	IOR
				92	IOG
6	P0E	49	reserved	93	VAA
7	P0D	50	reserved	94	VAA
8	P0C	51	reserved	95	COMP
9	P0B			96	VREF
10	P0A	52	P7E	97	GND
		53	P7D	98	VAA
11	P1E	54	P7C	99	VAA
12	P1D	55	P7B	100	GND
13	P1C	56	P7A	101	GND
14	P1B				
15	P1A	57	reserved	102	OLEE
		58	VAA	103	OLED
16	P2E	59	VAA	104	OLEC
17	P2D	60	reserved	105	OLEB
18	P2C	61	reserved	106	OLEA
19	P2B	62	GND		
20	P2A	63	GND	107	OL3E
		64	reserved	108	OL3D
21	reserved	65	reserved	109	OL3C
22	reserved			110	OL3B
23	reserved	66	reserved	111	OL3A
24	reserved	67	reserved		
25	IZE*	68	reserved	112	OL2E
		69	reserved	113	OL2D
26	LD*	70	reserved	114	OL2C
27	VAA			115	OL2B
		71	reserved	116	OL2A
28	P3E	72	reserved		
29	P3D	73	reserved	117	OL1E
30	GND	74	reserved	118	OL1D
31	P3C	75	reserved	119	OL1C
32	P3B			120	OL1B
33	P3A	76	D0	121	OL1A
		77	D1		
34	P4E	78	D2	122	SYNC*
35	P4D	79	D3	123	BLANK*
36	P4C	80	D4	124	CLOCK*
37	P4B	81	D5	125	CLOCK
38	P4A	82	D6		
		83	D7	126	VAA
39	P5E			127	VAA
40	P5D	84	CE*	128	GND
41	P5C	85	R/W	129	GND
42	P5B	86	C1		
43	P5A	87	C0	130	reserved
				131	reserved
				132	reserved

Pin Descriptions (continued)—132-pin PQFP Package


OL2A 116
OL2B 115
OL2C 114
OL2D 113
OL2E 112
OL3A 111
OL3B 110
OL3C 109
OL3D 108
OL3E 107
OLEA 106
OLEB 105
OLEC 104
OLED 103
OLEE 102
GND 101
GND 100
VAA 99
VAA 98
GND 97
VREF 96
COMP 95
VAA 94
VAA 93
IOG 92
IOR 91
FS ADJUST 90
IOB 89
PLL 88
C0 87
C1 86
R/W 85
CE* 84
OL1E 117
OL1D 118
OL1C 119
OL1B 120
OL1A 121
SYNC* 122
BLANK* 123
CLOCK* 124
CLOCK 125
VAA 126
VAA 127
GND 128
GND 129
N/C 130
N/C 131
N/C 132
OL0E 1
OL0D 2
OL0C 3
OL0B 4
OL0A 5
P0E 6
P0D 7
P0C 8
P0B 9
P0A 10
P1E 11
P1D 12
P1C 13
P1B 14
P1A 15
P2E 16
P2D 17
83 D7
82 D6
81 D5
80 D4
79 D3
78 D2
77 D1
76 D0
75 N/C
74 N/C
73 N/C
72 N/C
71 N/C
70 N/C
69 N/C
68 N/C
67 N/C
66 N/C
65 N/C
64 N/C
63 GND
62 GND
61 N/C
60 N/C
59 VAA
58 VAA
57 N/C
56 P7A
55 P7B
54 P7C
53 P7D
52 P7E
51 N/C
18 P2C
19 P2B
20 P2A
21 N/C
22 N/C
23 N/C
24 N/C
25 IZE*
26 LD*
27 VAA
28 P3E
29 P3D
30 GND
31 P3C
32 P3B
33 P3A
34 P4E
35 P4D
36 P4C
37 P4B
38 P4A
39 P5E
40 P5D
41 P5C
42 P5B
43 P5A
44 P6E
45 P6D
46 P6C
47 P6B
48 P6A
49 N/C
50 N/C
(TOP VIEW)

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in *Bt451/7/8 Evaluation Module Operation and Measurements,* application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt459 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a 6-layer PC board is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane (preferably analog ground plane), layer 3 the analog power plane, using the remaining layers for digital traces and digital power supplies.

The optimum layout enables the Bt459 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8 inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground partitioning isolation technique is constrained by the noise margin degradation during digital readback of the Bt459.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

For maximum performance, a separate isolated ground plane for the analog output termination resistors, RSET resistor, and VREF circuitry should be used, as shown in Figure 13. Another isolated ground plane is used for the GND pins of the Bt459 and supply decoupling capacitors.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt459 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8 inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 13. This bead should be located within 3 inches of the Bt459 and provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor decoupling each of four groups of VAA pins to GND. The capacitors should be placed as close as possible to the device.

The 33 µF capacitor is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high- frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 μF ceramic chip capacitor. Low-frequency supply noise will require a larger value. Lead lengths should be minimized for best performance so that the self-resonance frequency is greater than the LD* frequency.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt459 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit by using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt459 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt459 to minimize reflections. Unused analog outputs should be connected to GND.

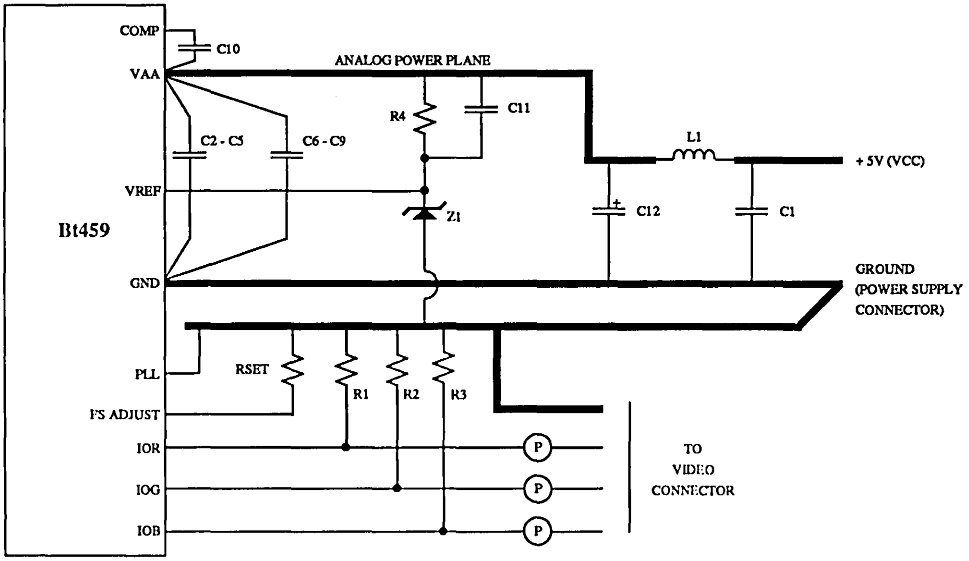
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

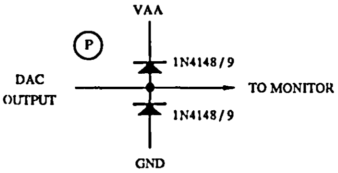
Analog Output Protection

The Bt459 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 13 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)


COMP
C10
VAA
ANALOG POWER PLANE
R4
C11
C2 - C5
C6 - C9
L1
+5V (VCC)
VREF
Z1
C12
C1
Bt459
GND
GROUND
(POWER SUPPLY
CONNECTOR)
PLL
RSET
R1
R2
R3
FS ADJUST
IOR
IOG
IOB
P
P
P
TO
VIDEO
CONNECTOR


VAA
P
1N4148/9
DAC
OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description	Vendor Part Number
C1–C5, C10, C11	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C6–C9	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C12	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt459.

Figure 13. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Due to the high clock rates at which the Bt459 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (typically a 220 Ω resistor to VCC and a 330 Ω resistor to GND). The termination resistors should be as close as possible to the Bt459.

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak due to the noise margins of the CMOS process. The Bt459 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by four or five (depending on whether 4:1 or 5:1 multiplexing was specified) and translating it to TTL levels. As LD* may be phase shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

For display applications where a single Bt459 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 and 5:1 input multiplexing of the Bt459, and will also optionally set the pipeline delay of the Bt459 to eight clock cycles. The Bt438 may also be used to interface the Bt459 to a TTL clock. Figure 14 illustrates using the Bt438 with the Bt459.

When using a single Bt459, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150 Ω).

Using Multiple Bt459s

For display applications where up to four Bt459s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 and 5:1 input multiplexing of the Bt459, synchronizes them to sub-pixel resolution and sets the pipeline delay of the Bt459 to eight clock cycles. The Bt439 may also be used to interface the Bt459 to a TTL clock. Figure 15 illustrates using the Bt439 with the Bt459.

Sub-pixel synchronization is supported via the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt459, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt459s, and adjusts the delay of each of the CLOCK and CLOCK* signals to the Bt459s to minimize the PLL delay difference. There should be minimal layout skew in the CLOCK and PLL trace paths to assure proper clock alignment.

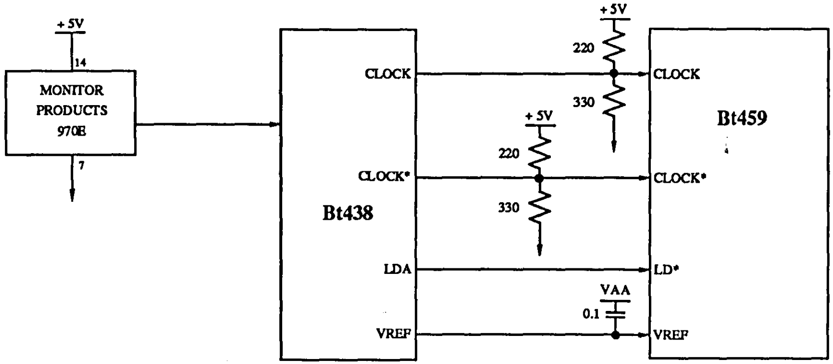


Figure 14. Generating the Bt459 Clock Signals.

Application Information (continued)

If sub-pixel synchronization of multiple Bt459s is not necessary, the Bt438 Clock Generator Chip may be used instead of the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt459s are connected together and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). The VREF inputs of the Bt459s must still have a 0.1 µF bypass capacitor to VAA, and have individual voltage references. The designer must take care to minimize skew on the CLOCK and CLOCK* lines. The PLL outputs of the Bt459s would not be used and should be connected to GND (either directly or through a resistor up to 150 Ω).

When using multiple Bt459s, each Bt459 should have its own power plane ferrite bead and voltage reference. Each Bt459 must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

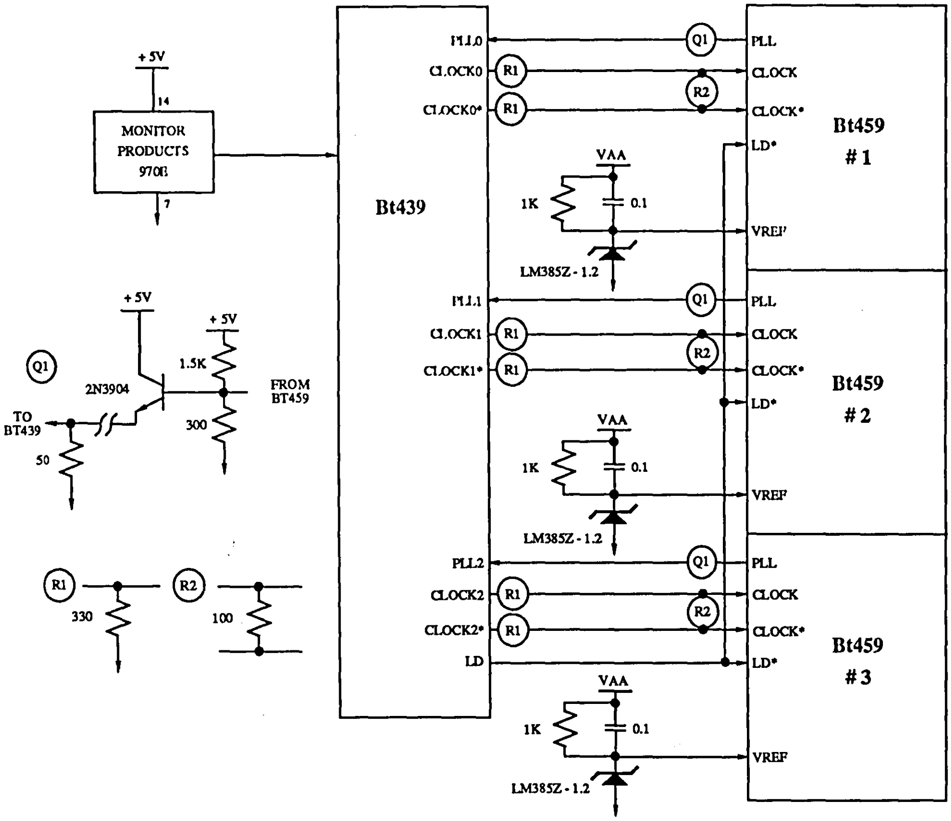

+5V
14
MONITOR PRODUCTS 970B
7
Bt439
PLL0
CLOCK0
CLOCK0*
PLL1
CLOCK1
CLOCK1*
PLL2
CLOCK2
CLOCK2*
LD
R1
R2
Q1
VAA
1K
0.1
LM385Z-1.2
PLL
CLOCK
CLOCK*
LD*
VREF
Bt459 #1
Bt459 #2
Bt459 #3
+5V
+5V
1.5K
2N3904
FROM BT459
TO BT439
300
50
330
100

Figure 15. Generating the Clock Signals for Multiple Bt459s.

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt459, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The Bt459 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438 and Bt439 Clock Generator Chips support this mode of operation when used with the Bt459.

To reset the Bt459, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for at least three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

In order to assure the Bt459 has the proper configuration, all the command registers must be initialized prior to a fixed pipeline reset. Because of this requirement, the power-up which occurs prior to initialization of the command registers cannot be used to assume the fixed pipeline. An additional reset is required after command register writes.

The resetting of the Bt459 to an eight clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if the multiple Bt459s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control via the read mask register and overlay display enable bits.

Resetting the Bt459 to an eight clock cycle pipeline delay is required for proper cursor pixel alignment.

Interleave Operation

To support interleaved frame buffers, the Bt459 may be configured for various interleave factors, as shown in Table 8. Table 9 shows an example of interleave operation for 4:1 multiplexing, an interleave select of 3, and starting with pixel {A}. Table 10 shows the same operation with pixel {B} selected as the starting pixel (the display has been panned down 3 scan lines).

Scan line number 0 corresponds to the top of the display screen and is the first displayed scan line after a vertical blanking interval. The output sequence is shown starting at the left-most displayed pixel.

Scan Line	Output Sequence
0	ABCDABCD...
1	DABCDABC...
2	CDABCDAB...
3	BCDABCDA...
4	ABCDABCD...
5	DABCDABC...
6	CDABCDAB...
7	BCDABCDA...
:	:

Table 9. Interleave Example.

Scan Line	Output Sequence
0	BCDABCDA...
1	ABCDABCD...
2	DABCDABC...
3	CDABCDAB...
4	BCDABCDA...
5	ABCDABCD...
6	DABCDABC...
7	CDABCDAB...
:	:

Table 10. Interleave Example.

Application Information (continued)

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Test Features of the Bt459

The Bt459 contains two dedicated test registers and an analog output comparator that assist the user in evaluating the performance and functionality of the part. This section is intended to explain the operating usage of these test features.

Signature Register (Signature Mode)

The signature register, in the active mode, operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel-color, and are presented as inputs simultaneously to the red, green, and blue signature analysis registers (SARs), as well as the three on-chip DACs.

The SARs act as a 24-bit wide Linear Feedback Shift Register on each succeeding pixel that is latched. It is important to note that in either the 4:1 or 5:1 multiplexed modes the SARs only latch one pixel per "load group." Thus the SARs are operating on only every fourth or fifth pixel in the multiplexed modes. The user determines which pixel phase (A, B, C, D, or E) is latched for generating new signatures by setting bits D0–D2 in the Test Register.

In 1:1 mux mode, the SARs will generate signatures truly on each succeeding pixel in the input stream. In this case, the user should always select pixel "A" (Test Register D0, D1, and D2 = 000) when in the 1:1 mode, since the "A" pixel pins are the only active pixel inputs.

The Bt459 will only generate signatures while in "active-display" (BLANK* negated). The SARs are available for reading and writing via the MPU port when the Bt459 is in a blanking state (BLANK* asserted). Specifically, it is safe to access the SARs after the DAC outputs are in the blanking state (up to 15 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 24-bit "seed" value into the SARs. Then, a known pixel stream will be input to the chip, say one scan-line or one frame buffer worth of pixels. Then, at the succeeding blank state, the resultant 24-bit signature can be read out by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, overlay and cursor data validity is also tested using the signature registers.

Assuming the chip is running 4:1 or 5:1 mux modes, the above process would be repeated with all different pixel phases—A, B, C, etc.—being selected.

It is not simple to speicfy the algorithm which descirbes the linear feedback shift operation used in the Bt459. The linear feedback configuration is shown in Figure 16. Note that each register internally uses XORs at each input bit (D_n) with the output (result) by one least significant bit (Q_{n-1}).

Experienced users have developed tables of specific seeds and pixel streams and recorded the signatures that result from those inputs applied to "known-good" parts. Note that a good signature from one given pixel stream can by used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed and the succeeding pixel stream fed to the SARs.

Signature Register (Data Strobe Mode)

Setting command bit CR20 to "1" puts the SARs into data strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the SARs from generating signatures. Instead, the SARs simply capture and hold the respective pixel phase that is selected.

Any MPU data written to the SARs is ignored. One use, however, is to directly check each pixel color value that is strobed into the SARs. To read out a captured color in the middle of a pixel stream, the user should first freeze all inputs to the Bt459. The levels of most inputs do not matter EXCEPT that CLOCK should be high, and CLOCK* should be low. Then, the user may read out the pixel color by doing three successive MPU reads from the red, green, and blue SARs, respectively.

Application Information (continued)

In general, the color read out will correspond to a pixel latched on the previous load. However, due to the pipelined data path, the color may come from an earlier load cycle. To read successive pixels, toggle LD*, pulse the CLOCK pins according to the mux state (1, 4, or 5 periods), then hold all pixel-related inputs and perform the three MPU reads as described. This overall process is best done on a sophisticated VLSI semiconductor Tester.

Analog Comparator

The other dedicated test structure in the Bt459 is the analog output comparator. It allows the user to measure the DACs against each other, as well as against a specific reference voltage.

Four combinations of tests are selected via the Test Register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the Test Register on each of the 64 scan lines of the 64 x 64 user-defined cursor block (the 64 x 64 cursor must be enabled for display). On each of these 64 scan lines, the capture occurs over one LD* period that corresponds to the cursor (x) position, set by the 12-bit cursor (x) register.

To obtain a meaningful comparison, the cursor should be located on the visible screen. There is no significance to the cursor pattern data in the cursor RAM. For a visual reference, the capture point actually occurs over the left-most edge of the 64 x 64 cursor block.

Due to the simple design of the comparator, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. In this case, the cursor (x) position should be set to well over 500 pixels to ensure an adequate supply of pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, up until capture.

Typically, users will create screen-wide test bands of various colors. Various comparison cases are set up by moving the cursor up and down (by changing the 12-bit cursor (y) register) over these bands. For each test, the result is obtained by reading Test Register bit D3.

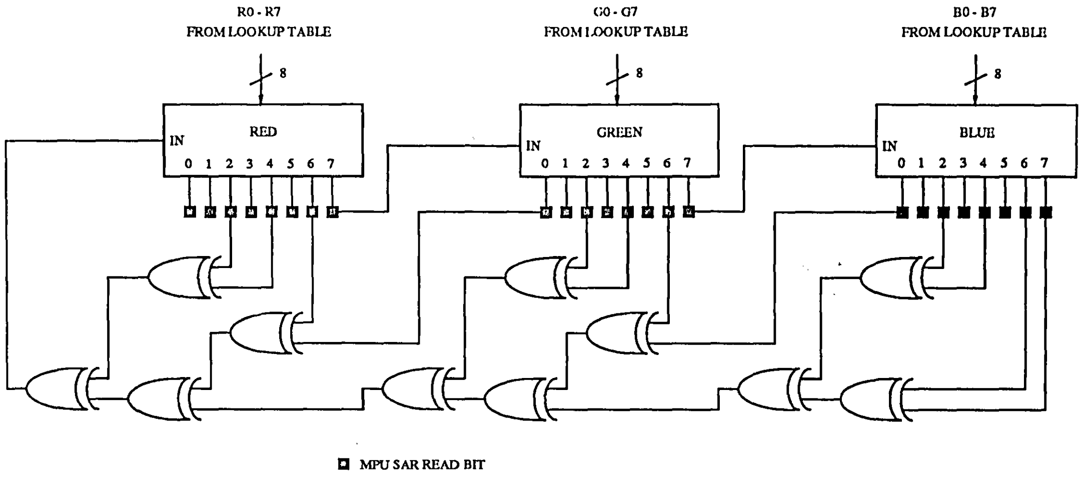


Figure 16. Signature Analysis Register Circuit.

Application Information (continued)

Initializing the Bt459

Following a power-on sequence, the Bt459 must be initialized. This sequence will configure the Bt459 as follows:

4:1 multiplexed operation
no overlays, no blinking, no interleave
64 x 64 block cursor, no cross hair cursor
8 bits per pixel, no panning, no zoom
sync enabled on IOG, 7.5 IRE blanking pedestal

Control Register Initialization

	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $00 to command register_1	10
Write $C0 to command register_2	10
Write $FF to pixel read mask register	10
Write $00 to reserved location	10
Write $00 to pixel blink mask register	10
Write $00 to reserved location	10
Write $00 to overlay read mask register	10
Write $00 to overlay blink mask register	10
Write $00 to interleave register	10
Write $00 to test register	10
Write $00 to address register low	00
Write $03 to address register high	01
Write $C0 to cursor command register	10
Write $00 to cursor (x) low register	10
Write $00 to cursor (x) high register	10
Write $00 to cursor (y) low register	10
Write $00 to cursor (y) high register	10
Write $00 to window (x) low register	10
Write $00 to window (x) high register	10
Write $00 to window (y) low register	10
Write $00 to window (y) high register	10
Write $00 to window width low register	10
Write $00 to window width high register	10
Write $00 to window height low register	10
Write $00 to window height high register	10

Load Cursor RAM Pattern

Write $00 to address register low	00
Write $04 to address register high	01
Write $FF to cursor RAM (location $000)	10
Write $FF to cursor RAM (location $001)	10
:	:
Write $FF to cursor RAM (location $3FF)	10

Color Palette RAM Initialization

Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $00)	11
Write green data to RAM (location $00)	11
Write blue data to RAM (location $00)	11
Write red data to RAM (location $01)	11
Write green data to RAM (location $01)	11
Write blue data to RAM (location $01)	11
:	:
Write red data to RAM (location $FF)	11
Write green data to RAM (location $FF)	11
Write blue data to RAM (location $FF)	11

Overlay Color Palette Initialization

Write $00 to address register low	00
Write $01 to address register high	01
Write red data to overlay (location $0)	10
Write green data to overlay (location $0)	10
Write blue data to overlay (location $0)	10
Write red data to overlay (location $1)	10
Write green data to overlay (location $1)	10
Write blue data to overlay (location $1)	10
:	:
Write red data to overlay (location $F)	10
Write green data to overlay (location $F)	10
Write blue data to overlay (location $F)	10

Cursor Color Palette Initialization

Write $81 to address register low	00
Write $01 to address register high	01
Write red data to cursor (location $0)	10
Write green data to cursor (location $0)	10
Write blue data to cursor (location $0)	10
Write red data to cursor (location $1)	10
Write green data to cursor (location $1)	10
Write blue data to cursor (location $1)	10
Write red data to cursor (location $2)	10
Write green data to cursor (location $2)	10
Write blue data to cursor (location $2)	10

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Reference Voltage	VREF	1.20	1.235	1.26	Volts
FS ADJUST Resistor	RSET		523		Ω

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	Volts
Voltage on Any Signal Pin*		GND-0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ				
PQFP	TJ			+150	°C
PGA	TJ			+175	°C
					°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	
					°C
Vapor Phase Soldering (1 minute)	TVSOL			220	

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			-1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	.6		6	Volts
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			-1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Blank Level on IOR, IOB		0	5	50	µA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	−0.5		+1.2	Volts
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
PLL Analog Output	PLL				
Output Current					
SYNC*/BLANK* = 0		6.00	7.62	9.00	mA
SYNC*/BLANK* = 1		0	5	50	µA
Output Compliance		−1.0		+2.5	Volts
Output Impedance			50		kΩ
Output Capacitance (f = 1 MHz, PLL = 0 mA)			8	15	pF
Voltage Reference Input Current	IREF				
Rev. A			500		µA
Rev. B			10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min/Typ/ Max	135 MHz	110 MHz	80 MHz	Units
Clock Rate	Fmax	max	135	110	80	MHz
LD* Rate	LDmax					
1:1 multiplexing		max	50	50	50	MHz
4:1 multiplexing		max	33.75	27.5	20	MHz
5:1 multiplexing		max	27	22	16	MHz
R/W, C0, C1 Setup Time	1	min	0	0	0	ns
R/W, C0, C1 Hold Time	2	min	10	10	10	ns
CE* Low Time	3	min	40	40	40	ns
CE* High Time	4	min	20	20	20	ns
CE* Asserted to Data Bus Driven	5	min	5	5	5	ns
CE* Asserted to Data Valid	6	max	40	40	40	ns
CE* Negated to Data Bus 3-Stated	7	max	12	12	12	ns
Write Data Setup Time	8	min	15	15	15	ns
Write Data Hold Time	9	min	2	2	2	ns
Pixel and Control Setup Time	10	min	3	3	3	ns
Pixel and Control Hold Time	11	min	2	2	2	ns
Clock Cycle Time	12	min	7.4	9.09	12.5	ns
Clock Pulse Width High Time	13	min	3.2	4	5	ns
Clock Pulse Width Low Time	14	min	3.2	4	5	ns
LD* Cycle Time	15					
1:1 multiplexing		min	15.15	20	20	ns
4:1 multiplexing		min	29.63	36.36	50	ns
5:1 multiplexing		min	37.04	45.45	62.5	ns
LD* Pulse Width High Time	16					
1:1 multiplexing		min	6	7	7	ns
4:1 or 5:1 multiplexing		min	12	15	20	ns
LD* Pulse Width Low Time	17					
1:1 multiplexing		min	6	7	7	ns
4:1 or 5:1 multiplexing		min	12	15	20	ns

See test conditions on next page.

AC Characteristics (continued)

Parameter	Symbol	Min/Typ/ Max	135 MHz	110 MHz	80 MHz	Units
Analog Output Delay	18	typ	12	12	12	ns
Analog Output Rise/Fall Time	19	typ	1.5	1.5	2	ns
Analog Output Settling Time	20	max	8	8	12	ns
Clock and Data Feedthrough*		typ	tbd	tbd	tbd	dB
Glitch Impulse*		typ	50	50	50	pV - sec
DAC to DAC Crosstalk		typ	tbd	tbd	tbd	dB
Analog Output Skew		typ	0	0	0	ns
		max	2	2	2	ns
Pipeline Delay		min	6	6	6	Clocks
		max	10	10	10	Clocks
VAA Supply Current**	IAA	typ	240	220	200	mA
		max	360	335	300	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. TTL input values are 0-3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are VAA-0.8 to VAA-1.8 volts, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 75 pF. See timing notes in Figure 18. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V, TA = 20° C. IAA (max) at VAA = 5.25 V, TA = 0° C.

4

Timing Waveforms

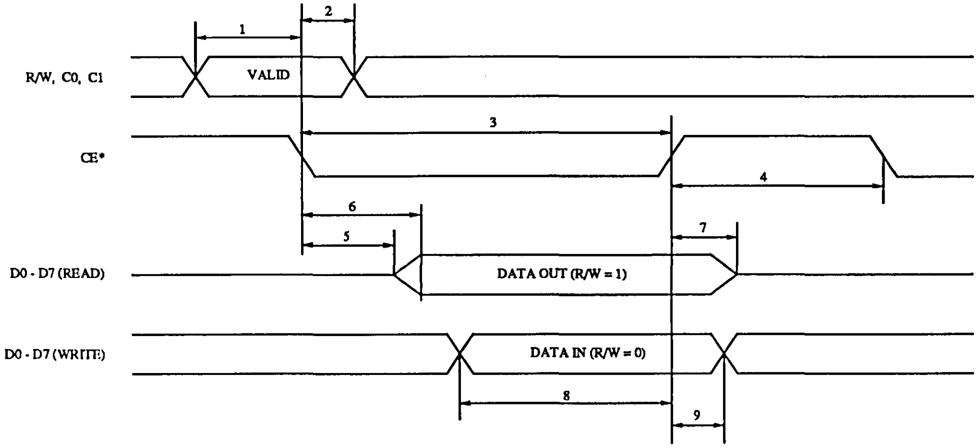
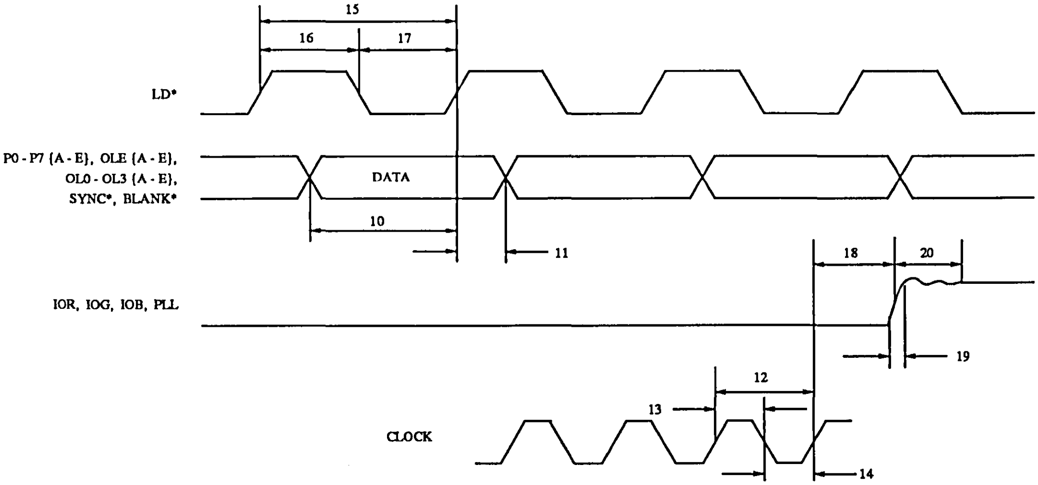

R/W, C0, C1
VALID
CE*
D0 - D7 (READ)
DATA OUT (R/W = 1)
D0 - D7 (WRITE)
DATA IN (R/W = 0)
1
2
3
4
5
6
7
8
9

Figure 17. MPU Read/Write Timing Dimensions.


LD*
P0 - P7 {A - E}, OLE {A - E},
OL0 - OL3 {A - E},
SYNC*, BLANK*
DATA
IOR, IOG, IOB, PLL
CLOCK
10
11
12
13
14
15
16
17
18
19
20

Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full-scale transition.

Note 2: Output settling time measured from 50% point of full-scale transition to output settling within ±1 LSB.

Note 3: Output rise/fall time measured between 10% and 90% points of full-scale transition.

Figure 18. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt459KG135	135 MHz	132-pin Ceramic PGA	0° to +70° C
Bt459KG110	110 MHz	132-pin Ceramic PGA	0° to +70° C
Bt459KG80	80 MHz	132-pin Ceramic PGA	0° to +70° C
Bt459KPF135	135 MHz	132-pin Plastic Quad Flatpack	0° to +70° C
Bt459KPF110	110 MHz	132-pin Plastic Quad Flatpack	0° to +70° C
Bt459KPF80	80 MHz	132-pin Plastic Quad Flatpack	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
G	Revised Figures 14 and 15.
H	Revised Figures 14 and 15.
I	Added 132-pin PQFP package, expanded PCB layout section, added using test features to Application Information Section, added Figure 16 and associated text in Application Information section. Revised Figure 15.
J	Clarified MPU contention with cursor RAM in Cursor RAM section of Internal Registers.
K	Added double reset, modified PLL feedback circuitry, added revision register section, reduced IREF, and eliminated write contention for revision B devices.

Device Revision	
B	Reduced IREF, eliminated write contention, enhanced CE* noise immunity. Added revision register.

Advance Information

This document contains information on a product under development. The parametric information contains target parameters and is subject to change.

Bt460

135 MHz
Monolithic CMOS
512 x 24 Color Palette
RAMDAC™

Distinguishing Features

- 135, 110, 80 MHz Operation
- 1:1, 4:1, or 5:1 Multiplexed Pixel Ports
- 512 x 24 Color Palette RAM
- 16 x 24 Overlay Color Palette
- 1x to 16x Integer Zoom Support
- Frame Buffer Interleave Support
- Pixel Panning Support
- On-Chip User-Definable 64 x 64 Cursor
- RS-343A Compatible Outputs
- Programmable Setup (0 or 7.5 IRE)
- X Windows Support for Overlays/Cursor
- Standard MPU Interface
- 132-pin PGA Package

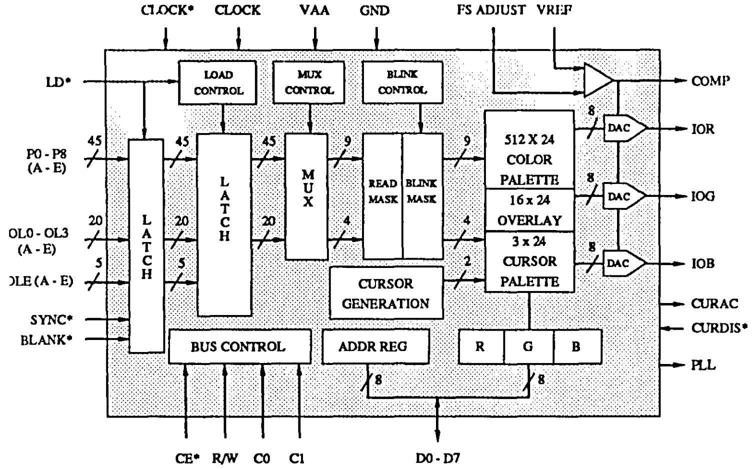
Applications

- High Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt438, Bt439
- Bt459, Bt462, Bt468

Functional Block Diagram


CLOCK*
CLOCK
VAA
GND
FS ADJUST
VREF
LD*
P0 - P8 (A - E)
OL0 - OL3 (A - E)
OLE (A - E)
SYNC*
BLANK*
45
20
5
LATCH
LOAD CONTROL
MUX CONTROL
BLINK CONTROL
MUX
9
4
READ MASK
BLINK MASK
512 X 24 COLOR PALETTE
16 x 24 OVERLAY
3 x 24 CURSOR PALETTE
2
CURSOR GENERATION
8
DAC
COMP
IOR
IOG
IOB
CURAC
CURDIS*
PLL
BUS CONTROL
ADDR REG
R
G
B
CE*
R/W
C0
C1
D0 - D7

Product Description

The Bt460 triple 8-bit RAMDAC is designed specifically for high-performance, high-resolution color graphics. The multiple pixel ports and internal multiplexing enable TTL-compatible interfacing to the frame buffer, while maintaining the 135 MHz video data rates required for sophisticated color graphics.

On-chip features include a 512 x 24 color palette RAM, 16 x 24 overlay color palette RAM, programmable 1:1, 4:1, or 5:1 input multiplexing of the pixel and overlay ports, bit plane masking and blinking, programmable setup (0 or 7.5 IRE), pixel panning support, and 1x to 16x integer zoom support.

The Bt460 has an on-chip three-color 64 x 64 pixel cursor and a three-color full screen (or full window) cross hair cursor.

The PLL current output enables the synchronization of multiple devices with sub-pixel resolution.

The Bt460 generates RS-343A compatible red, green, and blue video signals, and is capable of driving doubly terminated 75 Ω coax directly, without requiring external buffering. The differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ± LSB over the full temperature range.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt460 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs and dual-port overlay RAM allow color updating without contention with the display refresh process.

As illustrated in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 16-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit.

To write color data, the MPU loads the address register with the address of the primary color palette RAM, overlay RAM, or cursor color register location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the primary color palette RAM, overlay RAM, or cursor color registers. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. Reading color data is similar to writing, except the MPU executes read cycles.

When accessing the color palette RAM, overlay RAM, or cursor color registers, the address register increments after each blue read or write cycle. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 12 bits of the address register (ADDR0–11) are accessible to the MPU. ADDR12–ADDR15 are always a logical zero. ADDR0 and ADDR8 correspond to D0.

The only time the address register resets to $0000 is after accessing location $0FFF (due to wraparound).

ADDR0–15	C1, C0	Addressed by MPU
$xxxx	00	address register (ADDR0 - 7)
$xxxx	01	address register (ADDR8 - 15)
$0000–$00FF	10	reserved
$0100	10	overlay color 0*
:	10	:
$010F	10	overlay color 15*
$0181	10	cursor color register 1*
:	:	cursor color register 2*
$0183	10	cursor color register 3*
$0200	10	ID register ($4B)
$0201	10	command register_0
$0202	10	command register_1
$0203	10	command register_2
$0204	10	pixel read mask register low
$0205	10	pixel read mask register high
$0206	10	pixel blink mask register low
$0207	10	pixel blink mask register high
$0208	10	overlay read mask register
$0209	10	overlay blink mask register
$020A	10	interleave register
$020B	10	test register
$020C	10	red output signature register
$020D	10	green output signature register
$020E	10	blue output signature register
$020F	10	command register_3
$0210	10	input signature register
$0220	10	revision register ($B)
$0300	10	cursor command register
$0301	10	cursor (x) low register
$0302	10	cursor (x) high register
$0303	10	cursor (y) low register
$0304	10	cursor (y) high register
$0305	10	window (x) low
$0306	10	window (x) high
$0307	10	window (y) low
$0308	10	window (y) high
$0309	10	window width low register
$030A	10	window width high register
$030B	10	window height low register
$030C	10	window height high register
$0400–$07FF	10	cursor RAM
$0000–$01FF	11	color palette RAM*

*Indicates requires three read/write cycles—RGB.

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Although the color palette RAM, overlay RAM, and cursor color registers are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Accessing the control registers and cursor RAM is also done through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. When accessing the control registers and cursor RAM, the address register increments following a read or write cycle.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing of the Bt460.

Single Channel RAMDAC Operation

The Bt460 may be configured (via command register_2) to be a single-channel RAMDAC, enabling three Bt460s to be used in parallel for a 24-bit true-color system. The Bt460s share a common 8-bit data bus (D0–D7).

Each Bt460 must be configured to be either a red, green, or blue RAMDAC via command register_2. Only the green channel (IOG) of each RAMDAC is used; the IOR and IOB outputs should be connected to GND, either directly or through a resistor up to 75 Ω.

To load the color palettes, the MPU performs the normal (red, green, blue) write cycles to all three RAMDACs simultaneously. The red Bt460 loads color data only during the the red write cycle, the green Bt460 loads color data only during the green write cycle, and the blue Bt460 loads color data only during the blue write cycle.

To read the color palettes, the MPU performs the normal (red, green, blue) read cycles from all three RAMDACs simultaneously. The red Bt460 outputs color data only during the the red read cycle, the green Bt460 outputs color data only during the green read cycle, and the blue Bt460 outputs color data only during the blue read cycle.

External circuitry must decode when the MPU is reading or writing to the color palettes and assert CE* to all three Bt460s simultaneously.

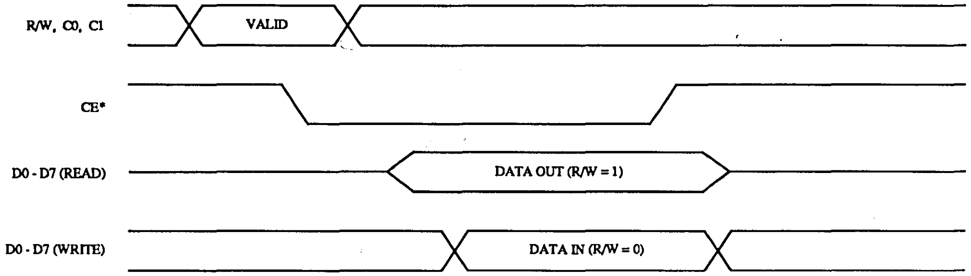


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt460 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, and overlay information, for either one, four, or five consecutive pixels, are latched into the device. Note that with this configuration, the sync and blank timing will be recognized only with one, four, or five pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing and to clock the video DRAMs.

For 4:1 or 5:1 input multiplexing, the Bt460 outputs color information each clock cycle based on the {A} inputs, followed by the {B} inputs, etc., until all four or five pixels have been output, at which point the cycle repeats. In the 1:1 input multiplexing mode, the {B}, {C}, {D}, and {E} inputs are ignored.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external circuitry.

To simplify the frame buffer interface timing, LD* may be phase shifted, in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by four or five, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than three, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*.

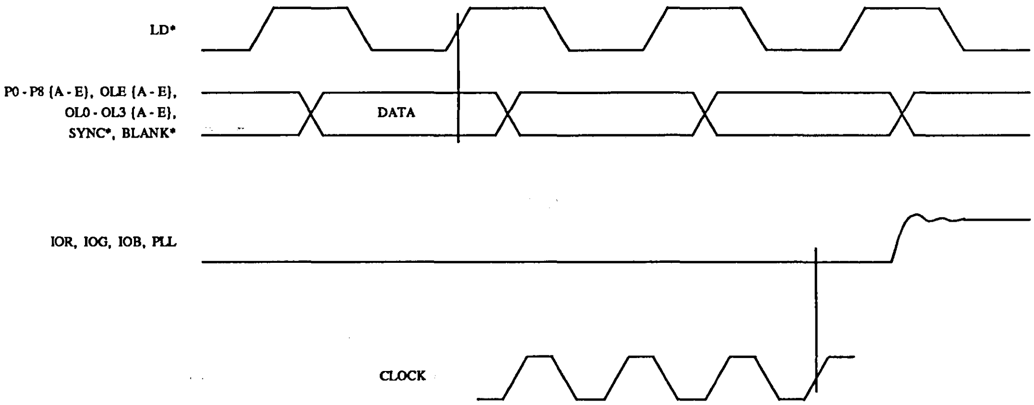


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

If 1:1 multiplexing is specified, LD* is also used for clocking the Bt460 (at a maximum of 50 MHz). The rising edge of LD* still latches the P0–P8 {A}, OL0–OL3 {A}, OLE {A}, SYNC*, and BLANK* inputs. However, analog information is output following the rising edge of LD* rather than CLOCK. Note that CLOCK must still run, but is ignored.

Pixel Addressing of Color Palette RAM

Typically, the P8 pixel input port is used to select the lower (P8 = 0) or upper (P8 = 1) 256 entries in the color palette RAM.

Alternately, the Bt460 can also use the cross hair cursor window to select the lower (outside the cursor window) or upper (inside the cursor window) 256 entries in the color palette RAM. In this case, the P8 pixel inputs are logically ORed with the lower/upper selection by the cursor window. Use of the P8 pixel inputs for palette selection can be disabled by the pixel read mask register (high).

Read and Blink Masking

Each clock cycle, 9 bits of color information (P0–P8) and 4 bits of overlay information (OL0–OL3) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual pixel and overlay inputs may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change due to blinking does not occur during the active display time (i.e. in the middle of the screen), the Bt460 monitors the BLANK* input to determine vertical retrace intervals (any BLANK* pulse longer than 256 LD* cycles).

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAMs, and OL0 is the LSB when addressing the overlay palette RAM. Table 4 illustrates the truth table used for color selection.

Pixel Panning

To support pixel panning, command register_1 specifies by how many clock cycles to pan. Only the pixel inputs and underlays are panned—overlays are not. Panning is done by delaying SYNC* and BLANK*, an additional 1, 2, 3, or 4 clock cycles.

If 0 pixel panning is specified, pixel {A} is output first, followed by pixel {B}, etc., until all four or five pixels have been output, at which point the cycle repeats (note that this assumes the interleave select is pixel {A}).

If 1 pixel panning is specified, pixel {B} will be first, followed by pixel {C}, etc. Pixel {A} will have been processed during the last clock cycle of the blanking interval, and will not be seen on the display screen. At the end of the active display line, pixel {A} will be output. Pixels {B}, {C}, {D}, and {E} will be output during the blanking interval, and will not be seen on the display screen.

The process is similar for panning by 2, 3, or 4 pixels.

Note that when a panning value other than 0 pixels is specified, valid pixel data must be loaded into the Bt460 during the first LD* cycle that BLANK* is a logical zero.

In the 1:1 multiplex mode, 0 pixel panning should be specified.

Note that the cursor position does not change relative to the edge of the display screen during panning.

Bits per Pixel	Pixels per LD* (1:1 muxing)	Pixels per LD* (4:1 muxing)	Pixels per LD* (5:1 muxing)	Colors Displayed
1 (2)	8	32	40	2 (4)
2 (3)	N/A	16	20	4 (8)
4 (5)	N/A	8	10	16 (32)
8 (9)	N/A	4	5	256 (512)

Numbers in parentheses indicate number of bits per pixel and number of colors if P8 pixel inputs are also used.

Table 2. P0–P7 Block Mode Operation.

Circuit Description (continued)

Pixel Zoom

The Bt460 supports 1x to 16x integer zoom through the use of pixel replication. Only the P0–P8 inputs are zoomed.

If 2x zooming is specified, the {A} pixel is output for two clock cycles, followed by the {B} pixel for two clock cycles, etc. 3x zooming is similar, except each pixel is output for three clock cycles. For 1:1 multiplexing, only the {A} pixel is output.

Note that LD* must always be the pixel clock (1:1 multiplex mode) or 1/4 or 1/5 the CLOCK rate. Regardless of the zoom factor, P0–P8 data is latched every LD* cycle.

During 2x zoom, new P0–P8 data must be presented every two LD* cycles. During 3x zoom, new P0–P8 data must be presented every three LD* cycles. The pixel data must be held at the P0–P8 {A–E} inputs for the appropriate number of LD* cycles until new P0–P8 information is needed. OL0–OL3, OLE, SYNC*, and BLANK* information are still latched every LD* cycle.

Note that in the 1:1 multiplex mode, 1x zoom must be specified. Also, while in the block mode (1, 2, or 4 bits per pixel), 1x zoom must be specified.

Figure 3 illustrates the zoom timing.

Block Mode Operation

The Bt460 supports loading of the P0–P7 pixel data at 1, 2, 4, or 8 bits per pixel.

Note that LD* must always be the pixel clock (1:1 multiplex mode) or 1/4 or 1/5 the CLOCK rate, regardless of the block mode. Regardless of the block mode, P0–P8 data is latched every LD* cycle.

1 Bit per Pixel (RA1–RA7 = 0) RA0 =	2 Bits per Pixel (RA2–RA7 = 0) RA1, RA0 =	4 Bits per Pixel (RA4–RA7 = 0) RA3–RA0 =	8 Bits per Pixel RA7–RA0 =
P7A	P7A, P6A	P7A, P6A, P5A, P4A	P7A, P6A, P5A, P4A, P3A, P2A, P1A, P0A
P6A	P5A, P4A	P3A, P2A, P1A, P0A	P7B, P6B, P5B, P4B, P3B, P2B, P1B, P0B (4:1)
:	P3A, P2A	P7B, P6B, P5B, P4B (4:1)	P7C, P6C, P5C, P4C, P3C, P2C, P1C, P0C (4:1)
P0A	P1A, P0A	P3B, P2B, P1B, P0B (4:1)	P7D, P6D, P5D, P4D, P3D, P2D, P1D, P0D (4:1)
P7B (4:1)	P7B, P6B (4:1)	P7C, P6C, P5C, P4C (4:1)	P7E, P6E, P5E, P4E, P3E, P2E, P1E, P0E (5:1)
P6B (4:1)	P5B, P4B (4:1)	P3C, P2C, P1C, P0C (4:1)	
:	P3B, P2B (4:1)	P7D, P6D, P5D, P4D (4:1)	
P0B (4:1)	P1B, P0B (4:1)	P3D, P2D, P1D, P0D (4:1)	
P7C (4:1)	P7C, P6C (4:1)	P7E, P6E, P5E, P4E (5:1)	
P6C (4:1)	P5C, P4C (4:1)	P3E, P2E, P1E, P0E (5:1)	
:	P3C, P2C (4:1)		
P0C (4:1)	P1C, P0C (4:1)		
P7D (4:1)	P7D, P6D (4:1)		
P6D (4:1)	P5D, P4D (4:1)		
:	P3D, P2D (4:1)		
P0D (4:1)	P1D, P0D (4:1)		
P7E (5:1)	P7E, P6E (5:1)		
P6E (5:1)	P5E, P4E (5:1)		
:	P3E, P2E (5:1)		
P0E (5:1)	P1E, P0E (5:1)		

Note: Each line represents one pixel clock cycle. A column represents one LD* cycle loading new P0–P7 data. All entries with "4:1" descriptor are also valid for 5:1 mode. The P8 pixel inputs are unaffected by the block mode and always address the RA8 inputs of the RAM.

Table 3. Block Mode Operation (RA = Color Palette RAM Address).

Circuit Description (continued)

For 8 bits per pixel (or 9 if using the P8 pixel inputs), new P0–P7 information must be presented every LD* cycle. For 4 (or 5) bits per pixel, new P0–P7 information must be presented every two LD* cycles. For 2 (or 3) bits per pixel, new P0–P7 information must be presented every four LD* cycles. For 1 (or 2) bits per pixel, new P0–P7 information must be presented every eight LD* cycles.

The pixel data must be held at the P0–P7 inputs for the appropriate number of LD* cycles until new P0–P7 information is needed. OL0–OL3, OLE, SYNC*, and BLANK* information are still latched every LD* cycle.

Tables 2 and 3 show the block mode operation, and the addressing of the color palette RAM.

Figure 4 illustrates the block mode timing (4 bits per pixel).

Note that in the 1:1 multiplex mode, 8 bits per pixel must be specified. Also, for block modes other than 8 bits per pixel, a 0 pixel interleave must be selected.

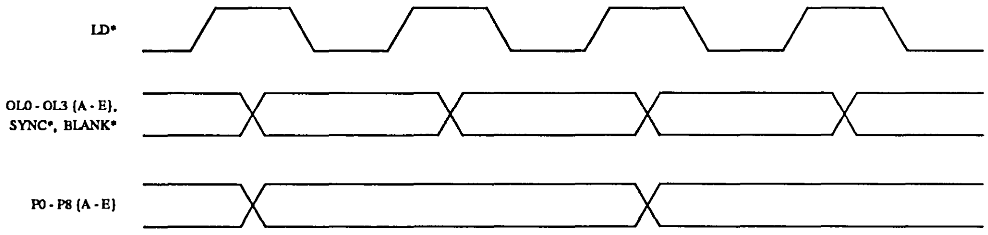

LD*
OL0 - OL3 {A - E},
SYNC*, BLANK*
P0 - P8 {A - E}

Figure 3. Zoom Input Timing (2x Zoom).

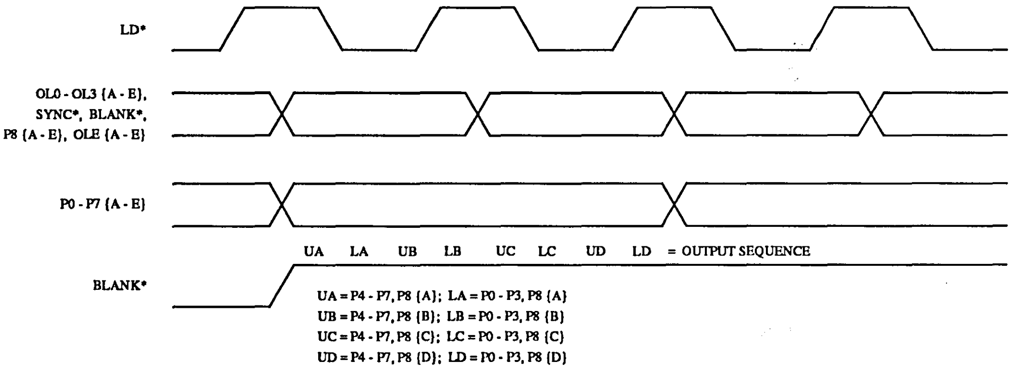

LD*
OL0 - OL3 {A - E},
SYNC*, BLANK*,
P8 {A - E}, OLE {A - E}
P0 - P7 {A - E}
UA LA UB LB UC LC UD LD = OUTPUT SEQUENCE
BLANK*
UA = P4 - P7, P8 {A}; LA = P0 - P3, P8 {A}
UB = P4 - P7, P8 {B}; LB = P0 - P3, P8 {B}
UC = P4 - P7, P8 {C}; LC = P0 - P3, P8 {C}
UD = P4 - P7, P8 {D}; LD = P0 - P3, P8 {D}

Figure 4. Block Mode Input Timing (4 Bits per Pixel, 1x Zoom, 4:1 Multiplexing).

Circuit Description (continued)

On-Chip Cursor Operation

The Bt460 has an on-chip, three-color, 64 x 64 pixel, user-definable cursor. The cursor operates only with a noninterlaced video system.

The pattern for the cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. Cursor positioning is done via the cursor (x,y) register. Note that the Bt460 expects (x) to increase going right, and (y) to increase going down, as seen on the display screen. The cursor (x) position is relative to the first rising edge of LD* following the falling edge of SYNC*. The cursor (y) position is relative to the second sync pulse during vertical blanking. (See Figure 5.)

Three Color 64 x 64 Cursor

The 64 x 64 x 2 cursor RAM provides 2 bits of cursor information every clock cycle during the 64 x 64 cursor window, selecting the appropriate cursor color register as follows:

plane1	plane0	cursor color
0	0	cursor not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

(0,0) enables the color palette RAM and overlay RAM to be selected as normal. Each "plane" of cursor information may also be independently enabled or disabled for display via the cursor command register (bits CR47 and CR46).

The cursor pattern and color may be changed by changing the contents of the cursor RAM.

The cursor is centered about the value specified by the cursor (x,y) register. Thus, the cursor (x) register specifies the location of the 31st column of the 64 x 64 array (assuming the columns start with 0 for the left-most pixel and increment to 63). Similarly, the cursor (y) register specifies the location of the 31st row of the 64 x 64 array (assuming the rows start with 0 for the top-most pixel and increment to 63).

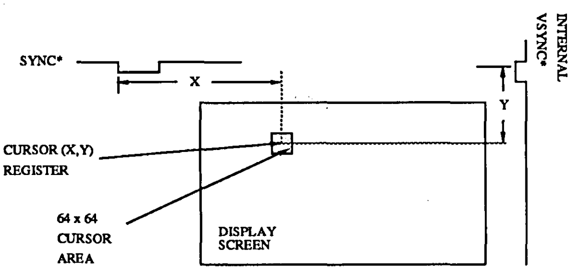


Figure 5. Cursor Positioning.

Circuit Description (continued)

Cross Hair Cursor

Cursor positioning for the three-color cross hair cursor is also done through the cursor (x,y) register. The intersection of the cross hair cursor is specified by the cursor (x,y) register. If the thickness of the cross hair cursor is greater than one pixel, the center of the intersection is the reference position.

During times that cross hair cursor information is to be displayed, the cursor command register (bits CR45 and CR44) is used to specify the color of the cross hair cursor.

CR45	CR44	cross hair color
0	0	cross hair not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

The cross hair cursor is limited to being displayed within the cross hair window, which is specified by the window (x,y), window width, and window height registers. Since the cursor (x,y) register must specify a point within the window boundaries, **it is the responsibility of the software to ensure that the cursor (x,y) register does not specify a point outside of the cross hair cursor window.**

If a full screen cross hair cursor is desired, the window (x,y) registers should contain $0000 and the window width and height registers should contain $0FFF.

Again, the cursor (x) position is relative to the first rising edge of LD* following the falling edge of SYNC*. The cursor (y) position is relative to the second sync pulse during vertical blanking. (See Figure 6.)

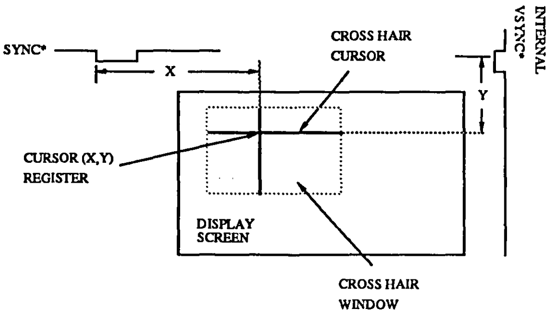


Figure 6. Cross Hair Cursor Positioning.

Circuit Description (continued)

Dual Cursor Positioning

Both the user-definable cursor and the cross hair cursor may be enabled for display simultaneously, enabling the generation of custom cross hair cursors.

As previously mentioned, the cursor (x,y) register specifies the location of bit (31, 31) of the cursor RAM. As the user-definable cursor contains an even number of pixels in the horizontal and vertical direction, it will be one pixel off from being truly centered about the cross hair cursor.

Figure 7 illustrates displaying the dual cursors.

In the 64 x 64 pixel area in which the user-definable cursor is displayed, each plane of the 64 x 64 cursor may be individually logically ORed or exclusive-ORed with the cross hair cursor information. Thus, the color of the displayed cursor will be dependent on the cursor pattern, whether it is logically ORed or XORed, and the individual cursor display enable and blink enable bits.

Figure 8 shows the equivalent cursor generation circuitry.

X Windows Cursor Mode

In the X Windows mode, plane1 of the cursor RAM is a cursor display enable and plane0 of the cursor RAM selects either cursor color 2 or 3. The operation is as follows:

plane1	plane0	Selection
0	0	no cursor
0	1	no cursor
1	0	cursor color 2
1	1	cursor color 3

Refer to Figure 12 as to the organization of the cursor RAM while in the X Windows mode.

Cursor Output (CURAC)

The Bt460 optionally outputs a TTL-compatible CURAC signal. Note that CURAC information precedes information output onto IOR, IOG, and IOB by five pixel clock cycles.

The CURAC pin may operate in one of two modes, as determined by command bit CR66. In the first mode, only cursor information is output onto CURAC. The cursor0 and cursor1 signals in Figure 8 are ORed together and output onto CURAC.

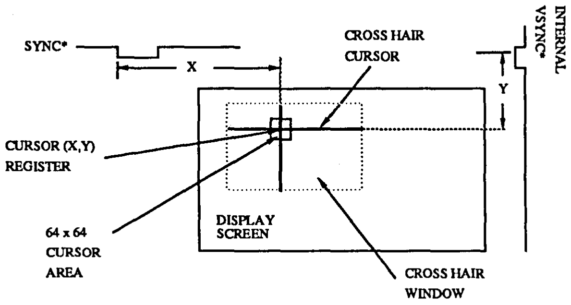


Figure 7. Dual Cursor Positioning.

Circuit Description (continued)

In the second mode, CURAC is also a logical one outside the cross hair window, including during blanking intervals. CURAC is a logical one inside the cross hair window when cursor information is being output.

The CURDIS* input pin is used to three-state the CURAC output asynchronously to the clocks.

For a cursor positioned over an edge of the screen, CURAC (if enabled) is not driven low by a blanking condition. To avoid display noise around the cursor, it is recommended to enable and use CURAC only with a full block pattern in the cursor RAM. In addition, CURAC should be disabled during active use of the cross hair cursor.

Cursor1, Cursor0	CR30	CR22	OLE	CR05	OL0–OL3	P0–P8	Addressed by frame buffer	Overlay Mode
11	x	x	x	x	$x	$xxx	cursor color 3	
10	x	x	x	x	$x	$xxx	cursor color 2	
01	x	x	x	x	$x	$xxx	cursor color 1	
00	0	0	x	x	$F	$xxx	overlay color 15	normal
:	:	:	:	:	:	:	:	
00	0	0	x	x	$1	$xx	overlay color 1	
00	0	0	x	1	$0	$xx	overlay color 0	
00	0	0	x	0	$0	$000	RAM location $000	
00	0	0	x	0	$0	$001	RAM location $001	
:	:	:	:	:	:	:	:	
00	0	0	x	0	$0	$1FF	RAM location $1FF	
00	x	1	1	x	$F	$xxx	overlay color 15	X Windows
:	:	:	:	:	:	:	:	
00	x	1	1	x	$1	$xxx	overlay color 1	
00	x	1	1	x	$0	$xxx	overlay color 0	
00	x	1	0	0	$x	$000	RAM location $000	
00	x	1	0	0	$x	$001	RAM location $001	
:	:	:	:	:	:	:	:	
00	x	1	0	0	$x	$1FF	RAM location $1FF	
00	1	0	x	x	$F	$xxx	overlay color 15	underlay
:	:	:	:	:	:	:	:	
00	1	0	x	x	$1	$xxx	overlay color 1	
00	1	0	1	x	$0	$000	overlay color 0 (underlay)	
00	1	0	0	0	$x	$000	RAM location $000	
00	1	0	x	0	$x	$001	RAM location $001	
:	:	:	:	:	:	:	:	
00	1	0	x	0	$x	$1FF	RAM location $1 FF	

Note: Refer to Figure 8 for generation of Cursor1 and Cursor0 control bits.

Table 4. Palette and Overlay Select Truth Table.

Circuit Description (continued)

Overlay / Underlay Operation

The overlay inputs (OL0–OL3 and OLE) may operate in three modes: normal overlays, X Windows overlays, or provide an underlay, as shown in Tables 4 and 5.

Overlay and underlay information may be displayed on a pixel basis. Note that overlays and underlay may both be used. If using X Windows overlays, the underlay is not available.

The priority of display operation is:

cursor
overlays
pixel data
underlays

The resetting of the Bt460 to an eight cycle pipeline delay is required for proper cursor pixel alignment.

In normal overlay mode, the overlay enable inputs, OLE {A–E} are ignored, and typically only 15 overlays are available. Graphics information (P0–P8) would be displayed only when no overlay information is present (OL0–OL3 = 0000).

In the X Windows overlay mode, the overlay enable inputs specify whether overlay information is present (OLE = 1) or not (OLE = 0). If OLE = 1, overlay information is displayed as determined by OL0–OL3. If OLE = 0, the OL0–OL3 inputs are ignored and P0–P8 pixel data is displayed.

In the underlay mode (CR30 = 1), if OLE = 0, pixel data is displayed. If OLE = 1, the underlay is displayed if P0–P8 = 0; if P0–P8 ≠ 0, then pixel data is displayed. Note that overlay color 0 is used for underlay color information.

	P0–P8 Pixel Inputs						
	1:1 Mux	Block Mode	Interleave	Panning	Zooming	Overlays	Underlay
Block Mode	no	-	yes	n/s	n/s	n/a	n/a
Interleave	n/s	yes	-	yes	yes	yes	yes
Panning	n/s	n/s	yes	-	yes	n/a	yes
Zooming	n/s	n/s	yes	yes	-	n/a	n/a
Overlays	yes	yes	yes	n/a	n/a	-	yes
Underlay	yes	yes	yes	yes	n/a	yes	-
Cursor	n/a	n/a	n/a	n/a	n/a	n/a	n/a

yes: fully functional together.
n/s: functions not supported together.
n/a: functions operate together, but do not affect each other.

Table 5. Features and Function Compatibility Table.

Circuit Description (continued)

Video Generation

Every clock cycle, the selected 24 bits of color information are presented to the three 8-bit D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 9 and 10. Command register_2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated, and whether or not sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converters produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 6 and 7 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt460 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

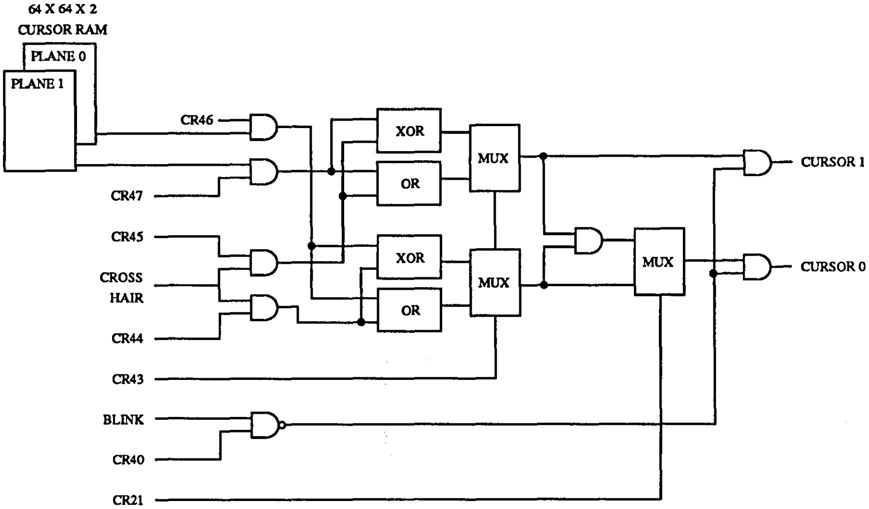
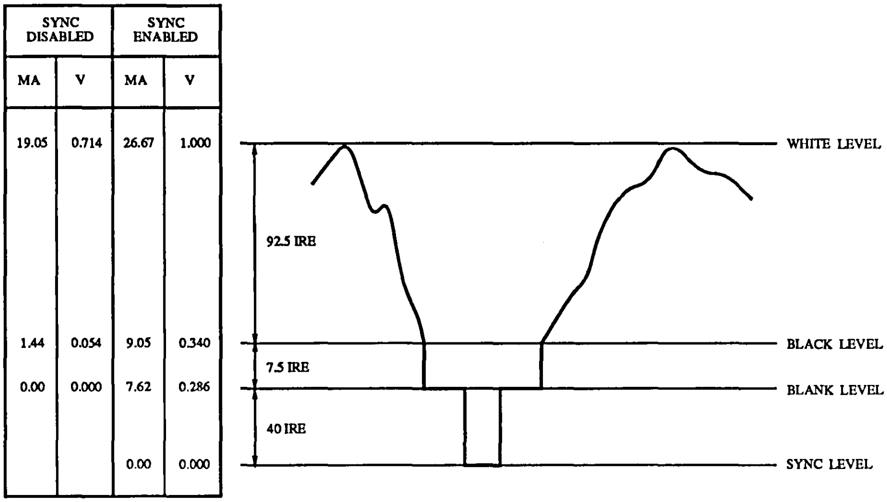


Figure 8. Cursor Control Circuitry.

Circuit Description (continued)



SYNC DISABLED		SYNC ENABLED	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

Note: 75 Ω doubly terminated load, RSET = 523 Ω, VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances assumed on all levels.

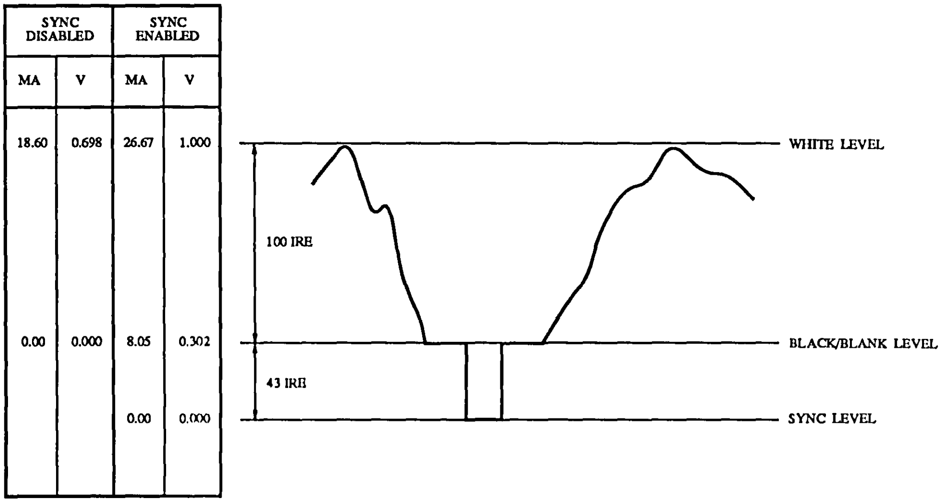
Figure 9. Composite Video Output Waveform (SETUP = 7.5 IRE).

Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 523 Ω, VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 6. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)



Note: 75 Ω doubly terminated load, RSET = 495 Ω, VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances assumed on all levels.

Figure 10. Composite Video Output Waveform (SETUP = 0 IRE).

Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 495 Ω, VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 7. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command register_0

This register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to data bus bit D0.

CR07, CR06	Multiplex select (00) reserved (01) 4:1 multiplexing (10) 1:1 multiplexing (11) 5:1 multiplexing	These bits specify whether 1:1, 4:1, or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 4:1 is specified, the {E} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be 1/4 the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be 1/5 the CLOCK rate. If 1:1 is specified, the {B}, {C}, {D}, and {E} inputs are ignored. Note that in the 1:1 multiplex mode, the maximum clock rate is 66 MHz. LD* is used for the pixel clock. Although CLOCK is ignored in the 1:1 mode, it must remain running. Note that it is possible to reset the pipeline delay of the Bt460 to a fixed eight clock cycles. In this instance, each time the input multiplexing is changed, the Bt460 must again be reset to a fixed pipeline delay.
CR05	Overlay 0 enable (0) use color palette RAM (1) use overlay color 0	When in the normal overlay mode, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information when the overlay inputs are $0. See Table 4.
CR04	reserved (logical zero)	
CR03, CR02	Blink rate selection (00) 16 on, 48 off (25/75) (01) 16 on, 16 off (50/50) (10) 32 on, 32 off (50/50) (11) 64 on, 64 off (50/50)	These 2 bits specify the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (% on/off).
CR01, CR00	Block mode (00) 8 bits per pixel (01) 4 bits per pixel (10) 2 bits per pixel (11) 1 bit per pixel	These bits specify whether the P0–P7 pixel data is input as 1, 2, 4, or 8 bits per pixel. Note that only the P0–P7 inputs are affected.

Internal Registers (continued)

Command register_1

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0.

CR17 - CR15	Pan select (000) 0 pixels {pixel A} (001) 1 pixel {pixel B} (010) 2 pixels {pixel C} (011) 3 pixels {pixel D} (100) 4 pixels {pixel E} (101) reserved (110) reserved (111) reserved	These bits specify the number of pixels to be panned. These bits are typically modified only during the vertical retrace interval, and should be set to 000 in the 1:1 multiplex mode. The {pixel A} indicates pixel A will be output first following the blanking interval, {pixel B} indicates pixel B will be output first, etc. Note that only pixel and underlay information is panned. Overlay and cursor information is not panned. In the 1:1 multiplex mode, 0 pixels should be specified.
CR14	reserved (logical zero)	
CR13–CR10	Zoom factor (0000) 1x (0001) 2x : (1111) 16x	These bits specify the amount of zooming to implement. For 2x zoom, pixel {A} is output for two clock cycles, followed by pixel {B} for two clock cycles, etc. For 3x zoom, pixel {A} is output for three clock cycles, etc. In the 1:1 multiplex mode, only the {A} pixels are output, and 1x zoom should be selected. Note that only P0–P8 are zoomed.

Internal Registers (continued)

Command register_2

This register may be written to or read by the MPU at any time and is not initialized. CR20 corresponds to data bus bit D0.

CR27	reserved (logical zero)	
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. 0 IRE specifies that the black and blank levels are the same.
CR25, CR24	Load palette RAM select (00) normal (01) red RAMDAC (10) green RAMDAC (11) blue RAMDAC	If (00) is specified, color data is loaded into the Bt460 using three write cycles (red, green, and blue), and color data is output using three read cycles (red, green, and blue). Modes (01), (10), and (11) enable the Bt460 to emulate a single-channel RAMDAC using only the green channel (IOG).
CR23	PLL select (0) SYNC* (1) BLANK*	This bit specifies whether the PLL output uses SYNC* or BLANK* for generating PLL information.
CR22	X Windows overlay select (0) normal overlays (1) X Windows overlays	This bit specifies whether the overlays are to operate normally (logical zero) or in an X Window environment (logical one).
CR21	X Windows cursor select (0) normal cursor (1) X Windows cursor	This bit specifies whether the cursor is to operate normally (logical zero) or in an X Window compatible mode (logical one).
CR20	Test mode select (0) signature analysis test (1) data strobe test	This bit determines the method of high-speed test used. The signature analysis registers are used to hold the test result for both test methods.

Internal Registers (continued)

Command Register_3

This register may be written to or read by the MPU at any time and is not initialized. CR60 corresponds to data bus bit D0.

CR67	reserved (logical zero)	
CR66	CURAC output format (0) cursor only (1) cursor + outside window	This bit specifies whether the CURAC output is a logical one only while cursor information is being output (logical zero) or also outside the cross hair cursor window (logical one).
CR65	Analysis register MSB select (0) P7 (1) P8	This bit specifies whether pixel input P7 or P8 is used as the most significant bit in the input signature analysis register. Bits D0–D6 of the input signature analysis register always test pixel inputs P0–P6, respectively.
CR64	Analysis register clock control (0) every LD* cycle (1) every CLOCK cycle	This bit controls the rate of operation of all signature analysis register (SAR) clocking. (0) is the normal mode, with pixel position (A, B, C, D, or E) determined by the test register. (1) is a special mode for chip testing (in this instance, SAR operation is not guaranteed for CLOCK rates above 30 MHz).
CR63	Red sync enable (0) disable sync on IOR (1) enable sync on IOR	This bit enables or disables sync information from being generated on the IOR output.
CR62	Green sync enable (0) disable sync on IOG (1) enable sync on IOG	This bit enables or disables sync information from being generated on the IOG output.
CR61	Blue sync enable (0) disable sync on IOB (1) enable sync on IOB	This bit enables or disables sync information from being generated on the IOB output.
CR60	Lookup table MSB select (0) P8 (1) cursor window	This bit specifies whether to use the P8 pixel inputs or the cursor window to provide the most significant bit of the 9-bit address to the 512-entry RAM.

Internal Registers (continued)

Interleave Register

This register may be written to or read by the MPU at any time and is not initialized. CR30 corresponds to data bus bit D0. The interleave register is for support of frame buffer systems configured for interleave operation.

CR37–CR35	Interleave select (000) 0 pixels (001) 1 pixel (010) 2 pixels (011) 3 pixels (100) 4 pixels (101) reserved (110) reserved (111) reserved	These bits specify the order in which the pixels are to be output, as shown in Table 8. The order is repeated every LD* cycle for a given scan line. Thus, if the output sequence is DABC, it is that sequence for all pixels on that scan line. The phrase "repeats every x" in Table 8 means that the output sequence repeats every x scan lines. Thus, for 4:1 multiplexing and a 1-pixel interleave select, ABCD would be repeated every 4th scan line. In the 1:1 input multiplex mode, a value of 0 pixels (000) must be specified.
CR34–CR32	First pixel select (000) pixel {A} (001) pixel {B} (010) pixel {C} (011) pixel {D} (100) pixel {E} (101) reserved (110) reserved (111) reserved	These bits are used to support panning in the Y direction with an interleaved frame buffer. Due to the interleave capability, it is necessary to specify the value of the first pixel on the first scan line following a vertical retrace. The pixel {E} selection is only used in the 5:1 multiplex mode. These bits are ignored in the 1:1 multiplex mode.
CR31	Overlay interleave enable (0) interleaving disabled (1) interleave enabled	This bit specifies whether or not OL0–OL3 and OLE are to be interleaved or not. If interleaving is enabled, the interleave factor and first pixel selection are the same as for P0–P8. If interleaving is disabled, pixel {A} is always output first and no interleaving occurs.
CR30	Underlay enable (0) underlay disabled (1) underlay enabled	If command bit CR22 is a logical zero, this bit is used to enable or disable the underlay from being displayed. If CR22 is a logical one, this bit is ignored. If the underlay is enabled (and CR22 is a logical zero), the OLE inputs function as follows: If OLE = 0, P0–P8 data is displayed. If OLE = 1, the underlay is displayed if P0–P8 = 0, if P0–P8 ≠ 0 then normal pixel data is displayed. The underlay uses overlay color 0 to provide underlay color information.

Internal Registers (continued)

Interleave Register (continued)

	5:1 multiplexing		4:1 multiplexing	
interleave select	output sequence	scan line number	output sequence	scan line number
0	ABCDE	each line	ABCD	each line
1	ABCDE BCDEA CDEAB DEABC EABCD	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD BCDA CDAB DABC	n n + 1 n + 2 n + 3 (repeats every 4)
2	ABCDE CDEAB EABCD BCDEA DEABC	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD CDAB ABCD CDAB	n n + 1 n + 2 n + 3 (repeats every 2)
3	ABCDE DEABC BCDEA EABCD CDEAB	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	ABCD DABC CDAB BCDA	n n + 1 n + 2 n + 3 (repeats every 4)
4	ABCDE EABCD DEABC CDEAB BCDEA	n n + 1 n + 2 n + 3 n + 4 (repeats every 5)	invalid	invalid

Table 8. Interleave Operation (First Pixel Select = Pixel A).

Internal Registers (continued)

Interleave Zoom Enable

If zooming while interleaving, the IZE* input pin indicates when to change the interleave sequence.

For example, while interleaving with 3x zoom, the IZE* pin should be a logical zero during the blanking interval of every third scan line (as shown in Figure 11). IZE* may be asserted coincident with the falling edge of BLANK*, but must remain low at least 16 LD* cycles after the falling edge of BLANK*.

If no zooming is done (1x zoom), the IZE* should always be a logical zero or be connected directly to GND.

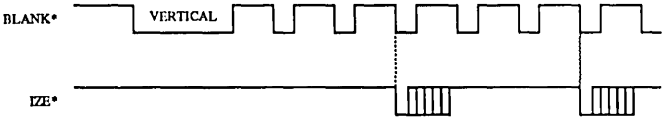


Figure 11. Interleave and Zoom Operation (3x Zoom Example).

Internal Registers (continued)

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt460, the value read by the MPU will be $4B. Data written to this register is ignored.

Pixel Read Mask Register Low

The 8-bit pixel read mask register low is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P0, and D7 corresponds to P7.

Pixel Read Mask Register High

The 8-bit pixel read mask register high is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P8, and D1–D7 are always a logical zero.

Pixel Blink Mask Register Low

The 8-bit pixel blink mask register low is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P0, and D7 corresponds to P7.

Pixel Blink Mask Register High

The 8-bit pixel blink mask register high is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P8, and D1–D7 are always a logical zero.

Overlay Read Mask Register

The 8-bit overlay read mask register is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette RAM. D0 corresponds to overlay plane 0 (OL0 {A–E}) and D3 corresponds to overlay plane 3 (OL3 {A–E}). Bits D0–D3 are logically ANDed with the corresponding overlay plane input. D4–D7 are always a logical zero.

This register may be written to or read by the MPU at any time and is not initialized.

Overlay Blink Mask Register

The 8-bit overlay blink mask register is used to enable (logical one) or disable (logical zero) an overlay plane from blinking at the blink rate and duty cycle specified by command register_0. D0 corresponds to overlay plane 0 (OL0 {A–E}) and D3 corresponds to overlay plane 3 (OL3 {A–E}). In order for an overlay plane to blink, the corresponding bit in the overlay read mask register must be a logical one. D4–D7 are always a logical zero.

This register may be written to or read by the MPU at any time and is not initialized.

Internal Registers (continued)

Revision Register (Revision B only)

This 8-bit register is a read-only register, specifying the revision of the Bt459. The four most significant bits signify the revision letter B, in hexadecimal form. The four least significant bits do not represent any value and should be ignored. Data written to this register is ignored.

Since Revision A device does not have a revision register, address $0220 will contain the last data read to or written from the internal bus.

Red, Green, and Blue Output Signature Registers

Signature Operation

These three 8-bit signature registers (one each for red, green, and blue) may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may read from or write to the signature registers while BLANK* is a logical zero to load the seed value.

By loading a test display into the frame buffer, a deterministic value for the red, green, and blue signature registers will be read from these registers if all circuitry is working properly. Refer to the Application Information test register section for more information.

Data Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the signature registers changes slightly. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

Each LD* cycle, the three signature registers capture the color values being presented to the DACs. As only one of the (A–E) pixels can be captured each LD* cycle, D0-D2 of the test register are used to specify which pixel (A–E) is to be captured.

Input Signature Register

Signature Operation

This 8-bit input signature register may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signature is being acquired. The MPU may write to the input signature register while BLANK* is a logical zero to load the seed value. The input signature register uses P0–P7 or P0–P6 and P8 data (selected by command bit CR65) addressing the palette RAM to calculate the signatures. The 8 bits of data latched in the input signature register may be masked (forced low) by the read mask registers.

When a test display is loaded into the frame buffer, a given value for the input signature register will be returned if all circuitry is working properly.

Data Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the input signature register changes slightly. Rather than determining the signature, it just captures and holds the 8 bits of pixel data addressing the color palette RAM.

Each LD* cycle, the input signature register captures the 8 bits of pixel data addressing the color palette RAM. As only one of the (A–E) pixels can be captured each LD* cycle (or clock cycle per command bit CR64), D0–D2 of the test register are used to specify which pixel (A–E) is to be captured.

Internal Registers (continued)

Test Register

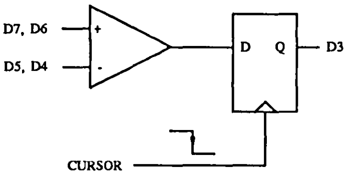
This 8-bit register is used for testing the Bt460. If 1:1 pixel multiplexing is specified, signature analysis is done on every pixel; if 4:1 pixel multiplexing is specified, signature analysis is done on every fourth pixel; if 5:1 pixel multiplexing is specified, signature analysis is done on every fifth pixel. D0–D2 are used for 4:1 and 5:1 multiplexing to specify whether to use the A, B, C, D, or E pixel inputs, as follows:

D2 - D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	pixel E
101	reserved
110	reserved
111	reserved

In 1:1 multiplexing mode, D0–D2 should be set to 000 (pixel A).

D3–D7 are used to compare the analog RGB outputs to each other and to a 150 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs or not, and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	150 mV ref. select	result



D7 - D4		If D3 = 1	If D3 = 0
0000	normal operation	-	-
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 150 mV reference	red > 150 mV	red < 150 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 150 mV reference	green > 150 mV	green < 150 mV

The above table lists the valid comparison combinations. A logical one enables that function to be compared; the result is D3. The comparison result is strobed into D3 on the left edge of the 64 x 64 cursor area. The output levels of the DACs should be constant for 5 µs before the left edge of the cursor.

For normal operation, D3–D7 must be a logical zero.

Internal Registers (continued)

Cursor Command Register

This command register is used to control various cursor functions of the Bt460. It is not initialized, and may be written to or read by the MPU at any time. CR40 corresponds to data bus bit D0.

CR47	64 x 64 cursor plane1 display enable (0) disable plane1 (1) enable plane1	Specifies whether plane1 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR46	64 x 64 cursor plane0 display enable (0) disable plane0 (1) enable plane0	Specifies whether plane0 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR45	Cross hair cursor plane1 display enable (0) disable plane1 (1) enable plane1	Specifies whether plane1 of the cross hair cursor is to be displayed (logical one) or not (logical zero).
CR44	Cross hair cursor plane0 display enable (0) disable plane0 (1) enable plane0	Specifies whether plane0 of the cross hair cursor is to be displayed (logical one) or not (logical zero). Note that plane0 and plane1 contain the same information.
CR43	Cursor format (0) XOR (1) OR	If both the 64 x 64 cursor and the cross hair cursor are enabled for display, this bit specifies whether the contents of the cursor RAM are to be logically exclusive-ORed (logical zero) or ORed (logical one) with the cross hair cursor.
CR42, CR41	Cross hair thickness (00) 1 pixel (01) 3 pixels (10) 5 pixels (11) 7 pixels	This bit specifies whether the vertical and horizontal thickness of the cross hair is one, three, five, or seven pixels. The segments are centered about the value in the cursor (x,y) register.
CR40	Cursor blink enable (0) blinking disabled (1) blinking enabled	This bit specifies whether the cursor is to blink (logical one) or not (logical zero). If both cursors are displayed, both will blink. The blink rate and duty cycle are as specified by command register_0.

Internal Registers (continued)

Cursor (x,y) Registers

These registers are used to specify the (x,y) coordinate of the center of the 64 x 64 pixel cursor window, or the intersection of the cross hair cursor. The cursor (x) register is made up of the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register is made up of the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). They are not initialized and may be written to or read by the MPU at any time. The cursor position is not updated until the vertical retrace interval after CYHR has been written to by the MPU.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are always a logical zero.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Cx = desired display screen (x) position + H–P

where

P = 37 if 1:1 input multiplexing, 52 if 4:1 input multiplexing, 57 if 5:1 input multiplexing
H = number of pixels between the first rising edge of LD* following the falling edge of SYNC* to active video.

Values from $0000 to $0FFF may be written into the cursor (x) register.

The cursor (y) value to be written is calculated as follows:

Cy = desired display screen (y) position + V–32

where

V = number of scan lines from the second sync pulse during vertical blanking to active video.

Values from $0FC0 (–64) to $0FBF (+4031) may be loaded into the cursor (y) register. The negative values ($0FC0 to $0FFF) are used in situations where V < 32, and the cursor must be moved off the top of the screen.

Internal Registers (continued)

Window (x,y) Registers

These registers are used to specify the (x,y) coordinate of the upper left corner of the cross hair cursor window. The window (x) register is made up of the window (x) low register (WXLR) and the window (x) high register (WXHR); the window (y) register is made up of the window (y) low register (WYLR) and the window (y) high register (WYHR). They are not initialized and may be written to or read by the MPU at any time. The window position is not updated until the vertical retrace interval after WYHR has been written to by the MPU.

WXLR and WXHR are cascaded to form a 12-bit window (x) register. Similarly, WYLR and WYHR are cascaded to form a 12-bit window (y) register. Bits D4–D7 of WXHR and WYHR are always a logical zero.

	Window (x) High (WXHR)				Window (x) Low (WXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window (y) High (WYHR)				Window (y) Low (WYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The window (x) value to be written is calculated as follows:

Wx = desired display screen (x) position + H–P

where

P = 5 if 1:1 input multiplexing, 20 if 4:1 input multiplexing, 25 if 5:1 input multiplexing
H = number of pixels between the first rising edge of LD* following the falling edge of HSYNC* to active video.

The window (y) value to be written is calculated as follows:

Wy = desired display screen (y) position + V

where

V = number of scan lines from the second sync pulse during vertical blanking to active video.

Values from $0000 to $0FFF may be written to the window (x) and window (y) registers. A full screen cross hair is implemented by loading the window (x,y) registers with $0000 and the window width and height registers with $0FFF.

The cursor window may also be used to specify whether P0–P7 address the lower (outside the cursor window) or upper (inside the cursor window) 256 entries in the color palette RAM.

Internal Registers (continued)

Window Width and Height Registers

These registers are used to specify the width and height (in pixels) of the cross hair cursor window. The window width register is made up of the window width low register (WWLR) and the window width high register (WWHR); the window height register is made up of the window height low register (WHLR) and the window height high register (WHHR). They are not initialized and may be written to or read by the MPU at any time. The window width and height are not updated until the vertical retrace interval after WHHR has been written to by the MPU.

WWLR and WWHR are cascaded to form a 12-bit window width register. Similarly, WHLR and WHHR are cascaded to form a 12-bit window height register. Bits D4–D7 of WWHR and WHHR are always a logical zero.

	Window Width High (WWHR)				Window Width Low (WWLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window Height High (WHHR)				Window Height Low (WHLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The actual window width is 2, 8, or 10 pixels more than the value specified by the window width register, depending on whether 1:1, 4:1, or 5:1 input multiplexing is specified. The actual window height is 2 pixels more than the value specified by the window height register. Therefore, the minimum window width is 2, 8, or 10 pixels, for 1:1, 4:1, and 5:1 multiplexing, respectively, and the minimum window height is two pixels.

Values from $0000 to $0FFF may be written to the window width and height registers.

Internal Registers (continued)

Cursor RAM

This 64 x 64 x 2 RAM is used to define the pixel pattern within the 64 x 64 pixel cursor window, and is not initialized.

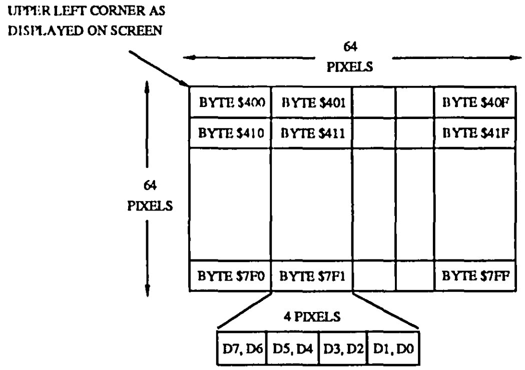
For Revision A, the cursor RAM should not be written to by the MPU during the horizontal sync time and for the two LD* cycles after the end of the horizontal sync. The cursor RAM may otherwise be written to or read by the MPU at any time without contention. If writing to the cursor RAM asynchronously to horizontal sync, it is recommended that the user position the cursor off-screen in the Y direction (write to the cursor (y) registers and wait for the vertical sync interval to move the cursor off-screen), write to the cursor RAM, then reposition the cursor back to the original position. An alternative is to perform a write then read sequence, and if the correct cursor RAM data was not written, perform another write then read sequence. Since the contention occurs only during horizontal sync at the Y locations coincident with the cursor, the second write/read sequence bypasses the window of time when cursor RAM is in contention.

For Revision B, cursor contention has been eliminated. The cursor RAM may be written to or read by the MPU at any time without contention.

During MPU accesses to the cursor RAM, the address register is used to address the cursor RAM. Figure 12 illustrates the internal format of the cursor RAM, as it appears on the display screen. Addressing starts at location $400 as shown in Table 1.

Note that in the X Windows mode, plane1 serves as a cursor display enable while plane0 selects one of two cursor colors (if enabled).

Note: in both modes of operation, plane1 = D7, D5, D3, D1; plane0 = D6, D4, D2, D0.



Normal Mode:

00 = color palette or overlay RAM
01 = cursor color 1
10 = cursor color 2
11 = cursor color 3

X-Windows Mode:

00 = color palette or overlay RAM
01 = color palette or overlay RAM
10 = cursor color 2
11 = cursor color 3

Figure 12. Cursor RAM as Displayed on the Screen.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as illustrated in Tables 6 and 7. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control inputs (TTL compatible). A logical zero typically switches off a 40 IRE current source on the IOG output (see Figures 9 and 10). SYNC* does not override any other control or data input, as shown in Tables 6 and 7; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0–P8 {A–E}, OL0–OL3 {A–E}, OLE {A–E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD*, while it is the output clock (1:1 multiplex mode) or is 1/4 or 1/5 of CLOCK, may be phase independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle, within the limits specified by the AC Characteristics section.
P0–P8 {A–E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which location of the color palette RAM is to be used to provide color information (see Table 4). Either one, four, or five consecutive pixels (up to 9 bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Note that typically the {A} pixel is output first, followed by the {B} pixel, etc., until all one, four, or five pixels have been output, at which point the cycle repeats. P8 {A–E} have internal pull-down devices so, if left floating, they assume a logical zero state.
OL0–OL3 {A–E}	Overlay select inputs (TTL compatible). These inputs are latched on the rising edge of LD* and, in conjunction with CR05 in command register_0, specify which palette is to be used for color information, as illustrated in Table 4. When accessing the overlay palette RAM, the P0–P8 {A–E} inputs are ignored. Overlay information (up to 4 bits per pixel) for either one, four, or five consecutive pixels are input through this port. Unused inputs should be connected to GND.
OLE {A–E}	Overlay enable inputs (TTL compatible). In the X Windows mode for overlays, a logical one indicates overlay information is to be displayed. A logical zero indicates to display P0–P8 information. In the normal mode for overlays, these inputs are ignored. They are latched on the rising edge of LD*. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 13). All outputs, whether used or not, should have the same output load.
IZE*	Interleave zoom enable input (TTL compatible). This input should be a logical zero for a minimum of 16 LD* cycles after the falling edge of BLANK* during scan lines that require an interleave shift. If zoom while interleaving is not supported, this pin should be connected directly to GND.
CURAC	Cursor active output. This output is a logical one while cursor or cross hair window information is being output. It is output following the rising edge of CLOCK. (See Figure 20.)
CURDIS*	Cursor disable input. A logical zero three-states the CURAC output asynchronously to the clocks. A logical one enables cursor information to be output onto CURAC. CURDIS* has an internal pull-down device so, if left floating, it assumes a logical zero state. (See Figure 20.)

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 13). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and maximize the capacitor's self-resonant frequency to be greater than the LD* frequency.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 13). Note that the IRE relationships in Figures 9 and 10 are maintained, regardless of the full-scale output current.

The relationship between RSET and the full-scale output current on IOG is:

$$\text{RSET}(\Omega) = \text{K1} * \text{VREF}(\text{V}) / \text{IOG}(\text{mA})$$

The full scale output current on IOR and IOB for a given RSET is:

$$\text{IOR, IOB}(\text{mA}) = \text{K2} * \text{VREF}(\text{V}) / \text{RSET}(\Omega)$$

where K1 and K2 are defined as:

Setup	IOG	IOR, IOB
7.5 IRE	K1 = 11,294	K2 = 8,067
0 IRE	K1 = 10,684	K2 = 7,457

Pin Name	Description
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 13, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 13. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.

Pin Descriptions (continued)

Pin Name	Description
PLL	Phase lock loop output current. This high-impedance current source is used to enable multiple Bt460s to be synchronized with sub-pixel resolution when used with an external PLL. A logical one for SYNC* or BLANK* (as specified by CR23 in command register_2) results in no current being output onto this pin, while a logical zero results in the following current being output: $\text{PLL (mA)} = 3{,}227 * \text{VREF (V)} / \text{RSET} (\Omega)$ If sub-pixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 Ω).
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Care should be taken to avoid glitches on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)

Signal	Pin Number
BLANK*	L1
SYNC*	K3
LD*	A5
CLOCK	K1
CLOCK*	K2
IZE*	B5
P0A	E3
P0B	D2
P0C	D1
P0D	E2
P0E	F3
P1A	A1
P1B	D3
P1C	C2
P1D	B1
P1E	C1
P2A	A3
P2B	B3
P2C	A2
P2D	C3
P2E	B2
P3A	A8
P3B	A7
P3C	B7
P3D	A6
P3E	B6
P4A	C9
P4B	B9
P4C	A9
P4D	C8
P4E	B8
P5A	B11
P5B	A11
P5C	C10
P5D	B10
P5E	A10
P6A	A14
P6B	A13
P6C	B12
P6D	C11
P6E	A12
P7A	E13
P7B	E12
P7C	D14
P7D	D13
P7E	D12
P8A	G14
P8B	G13
P8C	F14
P8D	F13
P8E	E14
OL0A	E1
OL0B	F2
OL0C	F1
OL0D	G3
OL0E	G2
OL1A	M1
OL1B	L2
OL1C	N1
OL1D	L3
OL1E	M2
OL2A	M3
OL2B	N2
OL2C	P1
OL2D	P2
OL2E	N3
OL3A	M4
OL3B	P3
OL3C	N4
OL3D	P4
OL3E	M5
OLEA	N5
OLEB	P5
OLEC	M6
OLED	N6
OLEE	P6
IOG	P10
IOB	P11
IOR	N10
PLL	N11
CURAC	A4
CURDIS*	C5
VAA	J1
VAA	J2
VAA	J3
VAA	C6
VAA	F12
VAA	M9
VAA	P7
VAA	P8
VAA	N8
GND	H1
GND	H2
GND	H3
GND	C7
GND	G12
GND	M8
GND	M7
GND	N7
COMP	N9
FS ADJUST	M10
VREF	P9
CE*	P13
R/W	N12
C1	P12
C0	M11
D0	L13
D1	M14
D2	L12
D3	M13
D4	N14
D5	P14
D6	N13
D7	M12
reserved	J13
reserved	J14
reserved	H12
reserved	H13
reserved	H14
reserved	B4
reserved	C4
reserved	C14
reserved	C13
reserved	B14
reserved	C12
reserved	B13
reserved	L14
reserved	K12
reserved	J12
reserved	K14
reserved	K13

Pin Descriptions (continued)

Bt460

(TOP VIEW)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
14	P6A	N/C	N/C	P7C	P8E	P8C	P8A	N/C	N/C	N/C	N/C	D1	D4	D5
13	P6B	N/C	N/C	P7D	P7A	P8D	P8B	N/C	N/C	N/C	D0	D3	D6	CE*
12	P6E	P6C	N/C	P7E	P7B	VAA	GND	N/C	N/C	N/C	D2	D7	R/W	C1
11	P5B	P5A	P6D									C0	PLL	IOB
10	P5E	P5D	P5C									FS ADJ	IOR	IOG
9	P4C	P4B	P4A									VAA	COMP	VREF
8	P3A	P4E	P4D									GND	VAA	VAA
7	P3B	P3C	GND									GND	GND	VAA
6	P3D	P3E	VAA									OLEC	OLED	OLEE
5	LD*	IZE*	CURD*									OL3E	OLEA	OLEB
4	CURAC	N/C	N/C									OL3A	OL3C	OL3D
3	P2A	P2B	P2D	P1B	P0A	P0E	OL0D	GND	VAA	SYNC*	OL1D	OL2A	OL2E	OL3B
2	P2C	P2E	P1C	P0B	P0D	OL0B	OL0E	GND	VAA	CLK*	OL1B	OL1E	OL2B	OL2D
1	P1A	P1D	P1E	P0C	OL0A	OL0C	N/C	GND	VAA	CLK	BLK*	OL1A	OL1C	OL2C

alignment marker (on top)

(BOTTOM VIEW)

	P	N	M	L	K	J	H	G	F	E	D	C	B	A
14	D5	D4	D1	N/C	N/C	N/C	N/C	P8A	P8C	P8E	P7C	N/C	N/C	P6A
13	CE*	D6	D3	D0	N/C	N/C	N/C	P8B	P8D	P7A	P7D	N/C	N/C	P6B
12	C1	R/W	D7	D2	N/C	N/C	N/C	GND	VAA	P7B	P7E	N/C	P6C	P6E
11	IOB	PLL	C0									P6D	P5A	P5B
10	IOG	IOR	FS ADJ									P5C	P5D	P5E
9	VREF	COMP	VAA									P4A	P4B	P4C
8	VAA	VAA	GND									P4D	P4E	P3A
7	VAA	GND	GND									GND	P3C	P3B
6	OLEE	OLED	OLEC									VAA	P3E	P3D
5	OLEB	OLEA	OL3E									CURD*	IZE*	LD*
4	OL3D	OL3C	OL3A									N/C	N/C	CURAC
3	OL3B	OL2E	OL2A	OL1D	SYNC*	VAA	GND	OL0D	P0E	P0A	P1B	P2D	P2B	P2A
2	OL2D	OL2B	OL1E	OL1B	CLK*	VAA	GND	OL0E	OL0B	P0D	P0B	P1C	P2E	P2C
1	OL2C	OL1C	OL1A	BLK*	CLK	VAA	GND	N/C	OL0C	OL0A	P0C	P1E	P1D	P1A

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in the *Bt451/7/8 Evaluation Module Operation and Measurements,* application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt460 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a 6-layer PC board is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane (preferably analog ground plane), layer 3 the analog power plane, using the remaining layers for digital traces and digital power supplies.

The optimum layout enables the Bt460 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8 inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground partitioning isolation technique is constrained by the noise margin degradation during digital readback of the Bt460.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

For maximum performance, a separate isolated ground plane for the analog output termination resistors, RSET resistor, and VREF circuitry should be used, as shown in Figure 13. Another isolated ground plane is used for the GND pins of the Bt460 and supply decoupling capacitors.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt460 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8 inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 13. This bead should be located within 3 inches of the Bt460 and provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor decoupling each of the four groups of VAA pins to GND. The capacitors should be placed as close as possible to the device.

The 33 µF capacitor is for low frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. Lead lengths should be minimized for best performance so that the self-resonance frequency is greater than the LD* frequency.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt460 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt460 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt460 to minimize reflections. Unused analog outputs should be connected to GND.

Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

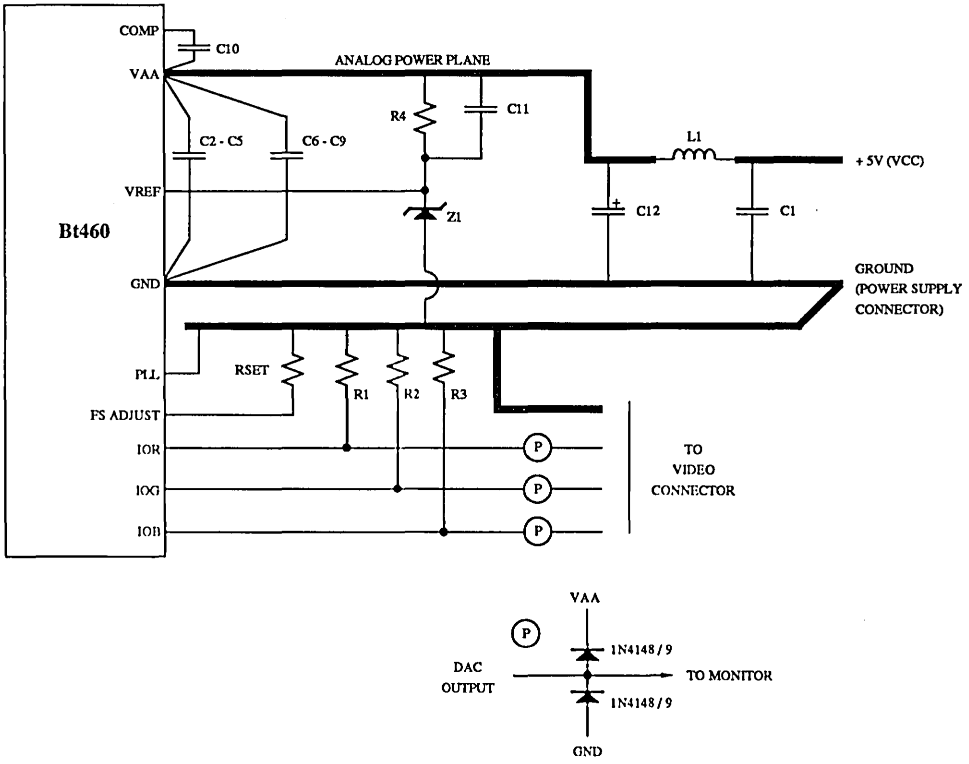
Analog Output Protection

The Bt460 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 13 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

4

PC Board Layout Considerations (continued)


COMP
C10
VAA
ANALOG POWER PLANE
R4
C11
C2 - C5
C6 - C9
L1
+5V (VCC)
VREF
Z1
C12
C1
Bt460
GROUND
(POWER SUPPLY
CONNECTOR)
GND
PLL
RSET
R1
R2
R3
FS ADJUST
IOR
IOG
IOB
P
TO
VIDEO
CONNECTOR
VAA
1N4148/9
DAC
OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description	Vendor Part Number
C1–C5, C10, C11	0.1 μF ceramic capacitor	Erie RPE110Z5U104M50V
C6–C9	0.01 μF ceramic chip capacitor	AVX 12102T103QA1018
C12	33 μF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt460.

Figure 13. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Due to the high clock rates at which the Bt460 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (typically a 220 Ω resistor to VCC and a 330 Ω resistor to GND). The termination resistors should be as close as possible to the Bt460.

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak due to the noise margins of the CMOS process. The Bt460 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by four or five (depending on whether 4:1 or 5:1 multiplexing was specified) and translating it to TTL levels. As LD* may be phase shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

For display applications where a single Bt460 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 and 5:1 input multiplexing of the Bt460, and will also optionally set the pipeline delay of the Bt460 to eight clock cycles. The Bt438 may also be used to interface the Bt460 to a TTL clock. Figure 14 illustrates using the Bt438 with the Bt460.

When using a single Bt460, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150 Ω).

Using Multiple Bt460s

For display applications where up to four Bt460s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 and 5:1 input multiplexing of the Bt460, synchronizes them to sub-pixel resolution, and sets the pipeline delay of the Bt460 to eight clock cycles. The Bt439 may also be used to interface the Bt460 to a TTL clock. Figure 15 illustrates using the Bt439 with the Bt460.

Sub-pixel synchronization is supported via the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt460, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt460s, and adjusts the phase of each of the CLOCK and CLOCK* signals to the Bt460s to minimize the PLL phase difference. There should be minimal layout skew in the CLOCK and PLL trace paths to assure proper clock alignment.

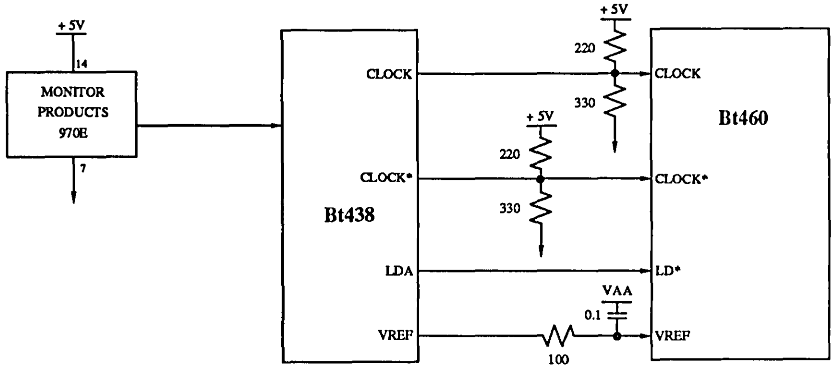


Figure 14. Generating the Bt460 Clock Signals.

Application Information (continued)

If sub-pixel synchronization of multiple Bt460s is not necessary, the Bt438 Clock Generator Chip may be used instead of the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt460s are connected together and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). The VREF inputs of the Bt460s must still be isolated by 100 Ω resistors, as shown in Figure 15, and have a 0.1 µF bypass capacitor to VAA. The designer must take care to minimize skew on the CLOCK and CLOCK* lines. The PLL outputs of the Bt460s would not be used and should be connected to GND (either directly or through a resistor up to 150 Ω).

When using multiple Bt460s, each Bt460 should have its own power plane ferrite bead. In addition, a single voltage reference may drive multiple devices; however, isolation resistors are recommended to reduce color channel crosstalk.

Higher performance may be obtained if each Bt460 has its own voltage reference. This may further reduce the amount of color channel crosstalk and color palette interaction.

Each Bt460 must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

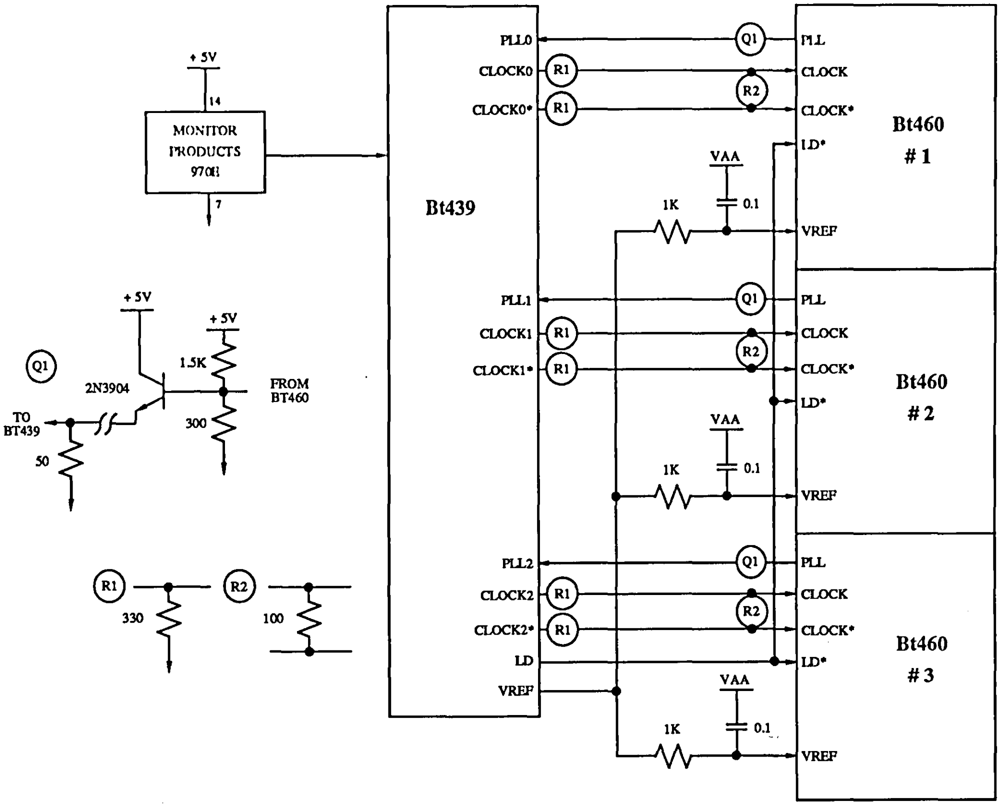

+5V
14
MONITOR PRODUCTS 9708
7
Bt439
PLL0
CLOCK0
CLOCK0*
PLL1
CLOCK1
CLOCK1*
PLL2
CLOCK2
CLOCK2*
LD
VREF
Q1
R1
R2
VAA
1K
0.1
PLL
CLOCK
CLOCK*
LD*
VREF
Bt460 #1
Bt460 #2
Bt460 #3
+5V
+5V
2N3904
1.5K
300
FROM BT460
TO BT439
50
R1
330
R2
100

Figure 15. Generating the Clock Signals for Multiple Bt460s.

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt460, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The Bt460 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438 and Bt439 Clock Generator Chips support this mode of operation when used with the Bt460.

To reset the Bt460, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for at least three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

In order to assure the Bt460 has the proper confiuration, all the command registers must be initialized prior to a fixed pipeline reset. Because of this requirement, the power up which occurs prior to initialization of the command registers cannot be used to assure the fixed pipeline. An additional reset is required after command register writes.

The resetting of the Bt460 to an eight clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if the multiple Bt460s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control via the read mask register and overlay display enable bits.

The resetting of the Bt460 to an eight cycle pipeline delay is required for proper cursor pixel alignment.

Interleave Operation

To support interleaved frame buffers, the Bt460 may be configured for various interleave factors, as shown in Table 8. Table 9 shows an example of interleave operation for 4:1 multiplexing, an interleave select of 3, and starting with pixel {A}. Table 10 shows the same operation with pixel {B} selected as the starting pixel (the display has been panned down three scan lines).

Scan line number 0 corresponds to the top of the display screen and is the first displayed scan line after a vertical blanking interval. The output sequence is shown starting at the left-most displayed pixel.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Scan Line	Output Sequence
0	ABCDABCD...
1	DABCDABC...
2	CDABCDAB...
3	BCDABCDA...
4	ABCDABCD...
5	DABCDABC...
6	CDABCDAB...
7	BCDABCDA...
:	:

Table 9. Interleave Example.

Scan Line	Output Sequence
0	BCDABCDA...
1	ABCDABCD...
2	DABCDABC...
3	CDABCDAB...
4	BCDABCDA...
5	ABCDABCD...
6	DABCDABC...
7	CDABCDAB...
:	:

Table 10. Interleave Example.

Application Information (continued)

Test Features of the Bt460

The Bt460 contains three dedicated test registers and an analog output comparator that assist the user in evaluating the performance and functionality of the part. This section is intended to explain the operating usage of these test features.

Signature Registers (Signature Mode)

The input signature register is 8 bits wide, capturing pixel information prior to the lookup table. Since the pixel path is 9 bits wide, the P7 or P8 pixel input, in conjunction with the P0–P6 pixel inputs, are selected for capture via command bit CR65.

The output signature register, in the active mode, operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel color, and are presented as inputs simultaneously to the red, green, and blue output signature analysis registers (output SARs), as well as the three on-chip DACs. The output SARs act as a 24-bit wide Linear Feedback Shift Register on each succeeding pixel that is latched.

It is important to note that in either the 4:1 or 5:1 multiplexed modes the SARs only latch one pixel per "load group." Thus the SARs are operating on only every fourth or fifth pixel in the multiplexed modes. The user determines which pixel phase (A, B, C, D, or E) is latched for generating new signatures by setting bits D0–D2 in the Test Register.

In 1:1 mux mode, the SARs will generate signatures truly on each succeeding pixel in the input stream. In this case, the user should always select pixel "A" (Test Register D0, D1, and D2 = 000) when in the 1:1 mode, since the "A" pixel pins are the only active pixel inputs.

The Bt460 will only generate signatures while in "active-display" (BLANK* negated). The SARs are available for reading and writing via the MPU port when the Bt460 is in a blanking state (BLANK* asserted). Specifically, it is safe to access the SARs after the DAC outputs are in the blanking state (up to 15 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 8-bit or 24-bit "seed" value into the SARs. Then, a known pixel stream will be input to the chip, say one scan-line or one frame buffer worth of pixels. Then, at the succeeding blank state, the resultant 8-bit or 24-bit signature can be read out by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, overlay and cursor data validity is also tested using the signature registers.

Assuming the chip is running 4:1 or 5:1 mux modes, the above process would be repeated with all different pixel phases—A, B, C, etc.—being selected.

It is not simple to specify the algorithm which specifies the linear feedback shift operations used in the Bt460. The linear feedback configurations are shown in Figures 16 and 17. Note that each register internally uses XORs at each input bit (D_n) with the output (result) by one least significant bit (Q_{n-1}).

Experienced users have developed tables of specific seeds and pixel streams and recorded the signatures that result from those inputs applied to "known-good" parts. Note that a good signature from one given pixel stream can be used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed and the succeeding pixel stream fed to the SARs.

Signature Registers (Data Strobe Mode)

Setting command bit CR20 to "1" puts the SARs into data strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the SARs from generating signatures. Instead, the SARs simply capture and hold the respective pixel phase that is selected.

Any MPU data written to the SARs is ignored. One use, however, is to directly check each pixel value that is strobed into the SARs. To read out values captured in the middle of a pixel stream, the user should first freeze all inputs to the Bt460. The levels of most inputs do not matter EXCEPT that CLOCK should be high, and CLOCK* should be low. Then, the user may read out the pixel color by doing three successive MPU reads from the red, green, and blue output SARs, respectively. Likewise, the input SAR may be read with one MPU read.

In general, the color read out will correspond to a pixel latched on the previous load. However, due to the pipelined data path, the color may come from an earlier load cycle. To read successive pixels, toggle LD*, pulse the CLOCK pins according to the mux state (1, 4, or 5 periods), then hold all pixel-related inputs and perform the three MPU reads as described. This overall process is best done on a sophisticated VLSI semiconductor Tester.

Application Information (continued)

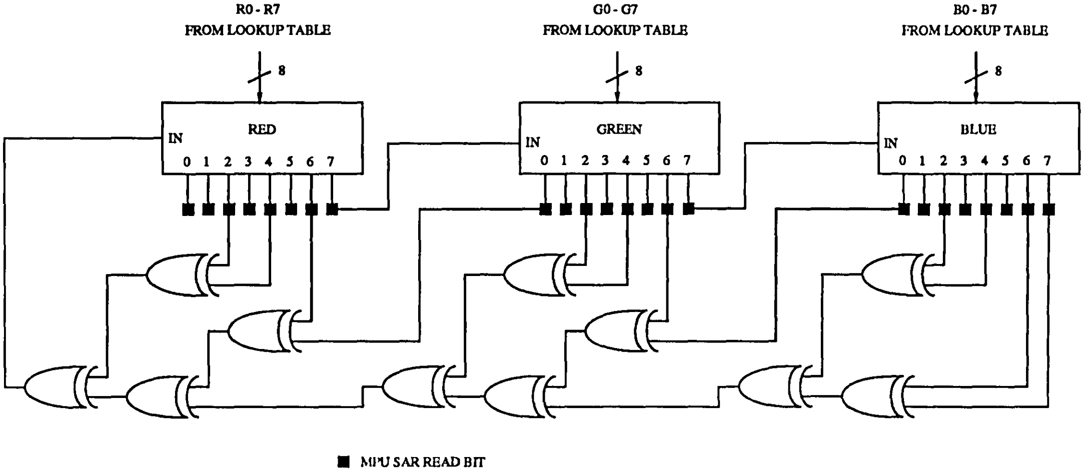

R0 - R7
FROM LOOKUP TABLE
G0 - G7
FROM LOOKUP TABLE
B0 - B7
FROM LOOKUP TABLE
8
8
8
RED
GREEN
BLUE
IN
IN
IN
0 1 2 3 4 5 6 7
0 1 2 3 4 5 6 7
0 1 2 3 4 5 6 7
■ MPU SAR READ BIT

Figure 16. Output Signature Analysis Register Circuit.

Application Information (continued)

Analog Comparator

The other dedicated test structure in the Bt460 is the analog output comparator. It allows the user to measure the DACs against each other, as well as against a specific reference voltage.

Four combinations of tests are selected via the Test Register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the Test Register on each of the 64 scan lines of the 64 x 64 user-defined cursor block (the 64 x 64 cursor must be enabled for display). On each of these 64 scan lines, the capture occurs over one LD* period that corresponds to the cursor (x) position, set by the 12-bit cursor (x) register.

To obtain a meaningful comparison, the cursor should be located on the visible screen. There is no significance to the cursor pattern data in the cursor RAM. For a visual reference, the capture point actually occurs over the left-most edge of the 64 x 64 cursor block.

Due to the simple design of the comparator, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. In this case, the cursor (x) position should be set to well over 500 pixels to ensure an adequate supply of pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, up until capture.

Typically, users will create screen-wide test bands of various colors. Various comparison cases are set up by moving the cursor up and down (by changing the 12-bit cursor (y) register) over these bands. For each test, the result is obtained by reading Test Register bit D3.

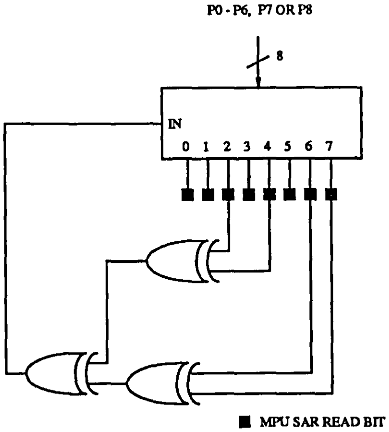


Figure 17. Input Signature Analysis Register Circuit.

Application Information (continued)

Initializing the Bt460

Following a power-on sequence, the Bt460 must be initialized. This sequence will configure the Bt460 as follows:

4:1 multiplexed operation
no overlays, no blinking, no interleave
64 x 64 block cursor, no cross hair cursor
9 bits per pixel, no panning, no zoom
sync enabled on IOG, 7.5 IRE blanking pedestal

Control Register Initialization

	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $00 to command register_1	10
Write $C0 to command register_2	10
Write $FF to pixel read mask register low	10
Write $01 to pixel read mask register high	10
Write $00 to pixel blink mask register low	10
Write $00 to pixel blink mask register high	10
Write $00 to overlay read mask register	10
Write $00 to overlay blink mask register	10
Write $00 to interleave register	10
Write $00 to test register	10
Write $0F to address register low	00
Write $14 to command register_3	10
Write $00 to address register low	00
Write $03 to address register high	01
Write $C0 to cursor command register	10
Write $00 to cursor (x) low register	10
Write $00 to cursor (x) high register	10
Write $00 to cursor (y) low register	10
Write $00 to cursor (y) high register	10
Write $00 to window (x) low register	10
Write $00 to window (x) high register	10
Write $00 to window (y) low register	10
Write $00 to window (y) high register	10
Write $00 to window width low register	10
Write $00 to window width high register	10
Write $00 to window height low register	10
Write $00 to window height high register	10

Load Cursor RAM Pattern

Write $00 to address register low	00
Write $04 to address register high	01
Write $FF to cursor RAM (location $000)	10
Write $FF to cursor RAM (location $001)	10
:	:
Write $FF to cursor RAM (location $3FF)	10

Color Palette RAM Initialization

Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $000)	11
Write green data to RAM (location $000)	11
Write blue data to RAM (location $000)	11
Write red data to RAM (location $001)	11
Write green data to RAM (location $001)	11
Write blue data to RAM (location $001)	11
:	:
Write red data to RAM (location $1FF)	11
Write green data to RAM (location $1FF)	11
Write blue data to RAM (location $1FF)	11

Overlay Color Palette Initialization

Write $00 to address register low	00
Write $01 to address register high	01
Write red data to overlay (location $0)	10
Write green data to overlay (location $0)	10
Write blue data to overlay (location $0)	10
Write red data to overlay (location $1)	10
Write green data to overlay (location $1)	10
Write blue data to overlay (location $1)	10
:	:
Write red data to overlay (location $F)	10
Write green data to overlay (location $F)	10
Write blue data to overlay (location $F)	10

Cursor Color Palette Initialization

Write $81 to address register low	00
Write $01 to address register high	01
Write red data to cursor (location $0)	10
Write green data to cursor (location $0)	10
Write blue data to cursor (location $0)	10
Write red data to cursor (location $1)	10
Write green data to cursor (location $1)	10
Write blue data to cursor (location $1)	10
Write red data to cursor (location $2)	10
Write green data to cursor (location $2)	10
Write blue data to cursor (location $2)	10

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.20	1.235	1.26	Volts
FS ADJUST Resistor	RSET		523		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	Volts
Voltage on Any Signal Pin*		GND - 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH				
P8 {A–E}, CURDIS*				60	µA
Other Inputs				1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	.6		6	Volts
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Digital Outputs (D0–D7, CURAC)					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

4

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level - Sync Enabled		6.29	7.62	8.96	mA
Blank Level - Sync Disabled		0	5	50	µA
Sync Level (If Enabled)		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	-0.5		+1.2	Volts
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
PLL Analog Output	PLL				
Output Current					
SYNC*/BLANK* = 0		6.00	7.62	9.00	mA
SYNC*/BLANK* = 1		0	5	50	µA
Output Compliance		-1.0		+2.5	Volts
Output Impedance			50		kΩ
Output Capacitance (f = 1 MHz, PLL = 0 mA)			8	15	pF
Voltage Reference Input Current	IREF		100		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min/Typ/ Max	135 MHz	110 MHz	80 MHz	Units
Clock Rate	Fmax	max	135	110	80	MHz
LD* Rate	LDmax					
1:1 multiplexing		max	50	50	50	MHz
4:1 multiplexing		max	33.75	27.5	20	MHz
5:1 multiplexing		max	27	22	16	MHz
R/W, C0, C1 Setup Time	1	min	0	0	0	ns
R/W, C0, C1 Hold Time	2	min	10	10	10	ns
CE* Low Time	3	min	40	40	40	ns
CE* High Time	4	min	20	20	20	ns
CE* Asserted to Data Bus Driven	5	min	5	5	5	ns
CE* Asserted to Data Valid	6	max	40	40	40	ns
CE* Negated to Data Bus 3-Stated	7	max	12	12	12	ns
Write Data Setup Time	8	min	15	15	15	ns
Write Data Hold Time	9	min	2	2	2	ns
Pixel and Control Setup Time	10	min	3	3	3	ns
Pixel and Control Hold Time	11	min	2	2	2	ns
Clock Cycle Time	12	min	7.4	9.09	12.5	ns
Clock Pulse Width High Time	13	min	3.2	4	5	ns
Clock Pulse Width Low Time	14	min	3.2	4	5	ns
LD* Cycle Time	15					
1:1 multiplexing		min	15.15	20	20	ns
4:1 multiplexing		min	29.63	36.36	50	ns
5:1 multiplexing		min	37.04	45.45	62.5	ns
LD* Pulse Width High Time	16					
1:1 multiplexing		min	6	7	7	ns
4:1 or 5:1 multiplexing		min	12	15	20	ns
LD* Pulse Width Low Time	17					
1:1 multiplexing		min	6	7	7	ns
4:1 or 5:1 multiplexing		min	12	15	20	ns
CURAC Output Delay	18	typ	18	18	18	ns
CURAC Disable Time	19	typ	tbd	tbd	tbd	ns
CURAC Enable Time	20	typ	tbd	tbd	tbd	ns

See test conditions on next page.

AC Characteristics (continued)

Parameter	Symbol	Min/Typ/ Max	135 MHz	110 MHz	80 MHz	Units
Analog Output Delay	21	typ	12	12	12	ns
Analog Output Rise/Fall Time	22	typ	1.5	1.5	2	ns
Analog Output Settling Time	23	max	8	8	12	ns
Clock and Data Feedthrough*		typ	tbd	tbd	tbd	dB
Glitch Impulse*		typ	50	50	50	pV - sec
DAC to DAC Crosstalk		typ	tbd	tbd	tbd	dB
Analog Output Skew		typ	0	0	0	ns
		max	2	2	2	ns
Pipeline Delay		min	6	6	6	Clocks
		max	10	10	10	Clocks
VAA Supply Current**	IAA	typ	390	360	320	mA
		max	420	400	370	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are VAA–0.8 to VAA–1.8 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 75 pF. CURAC output load ≤ 5 pF. See timing notes in Figure 19. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V, TA = 20° C. IAA (max) at VAA = 5.25 V, TA = 0° C.

Timing Waveforms

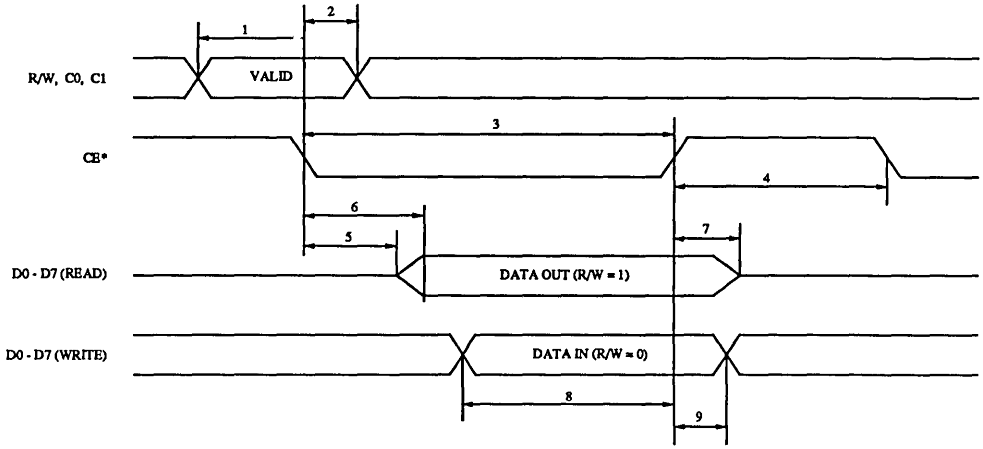
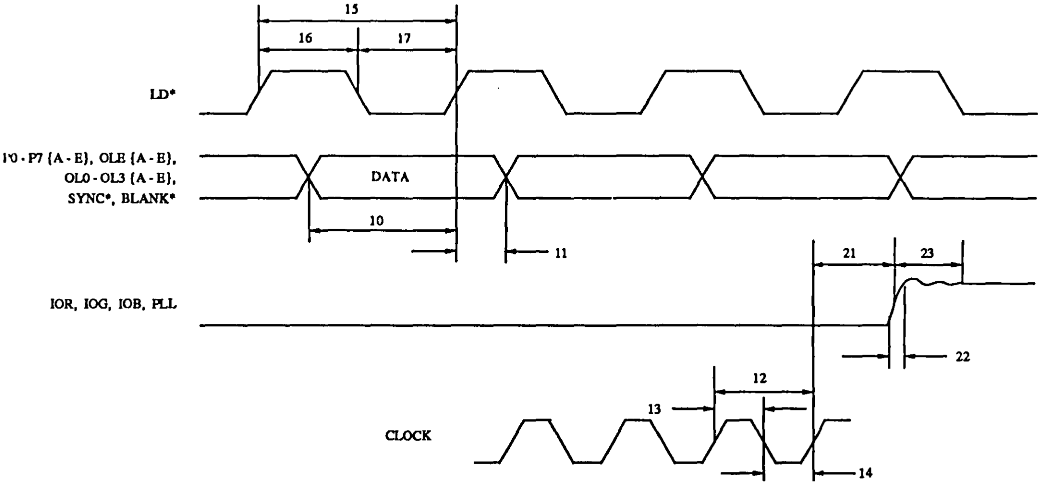

1
2
R/W, C0, C1
VALID
3
CE*
4
6
5
7
D0 - D7 (READ)
DATA OUT (R/W = 1)
D0 - D7 (WRITE)
DATA IN (R/W = 0)
8
9

Figure 18. MPU Read/Write Timing Dimensions.


15
16
17
LD*
P0 - P7 {A - E}, OLE {A - E},
OL0 - OL3 {A - E},
SYNC*, BLANK*
DATA
10
11
21
23
IOR, IOG, IOB, PLL
22
12
13
CLOCK
14

Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full-scale transition.

Note 2: Output settling time measured from 50% point of full-scale transition to output settling within ±1 LSB.

Note 3: Output rise/fall time measured between 10% and 90% points of full-scale transition.

Figure 19. Video Input/Output Timing.

Timing Waveforms (continued)

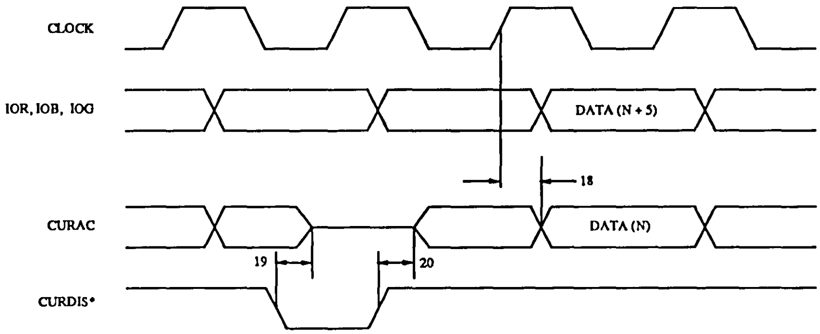

CLOCK
IOR, IOB, IOG
DATA (N + 5)
18
CURAC
DATA (N)
19
20
CURDIS*

Figure 20. Cursor Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt460KG135	135 MHz	132-pin Ceramic PGA	0° to +70° C
Bt460KG110	110 MHz	132-pin Ceramic PGA	0° to +70° C
Bt460KG80	80 MHz	132-pin Ceramic PGA	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
B	Full datasheet.
C	Expanded PCB layout section, added using test features to Application Information section. Clarified MPU contention with cursor RAM in Cursor RAM section of Internal Registers.
D	Added double reset, modified PLL feedback circuitry. Added revision register section and eliminated write contention for revision B devices.

Device Revision	
B	Added revision register, eliminated write contention.

Bt461
Bt462

170 MHz
Monolithic CMOS
1K x 8 Color Palette
RAMDAC™

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Distinguishing Features

- 170, 135, 110, 80 MHz Operation
- 3:1, 4:1, or 5:1 Pixel Input Muxing
- Single 8-bit D/A Converter
- 1024 x 8 Primary Color Palette RAM
- 256 x 8 Alternate Color Palette RAM
- 32 x 8 Overlay Color Palette RAM
- RS-343A-Compatible Output
- Pixel Panning Support
- Programmable Setup (0 or 7.5 IRE)
- Bit Plane Read and Blink Masks
- Two Load Color Palette Modes
- Standard MPU Interface
- 132-pin PGA or PQFP Package

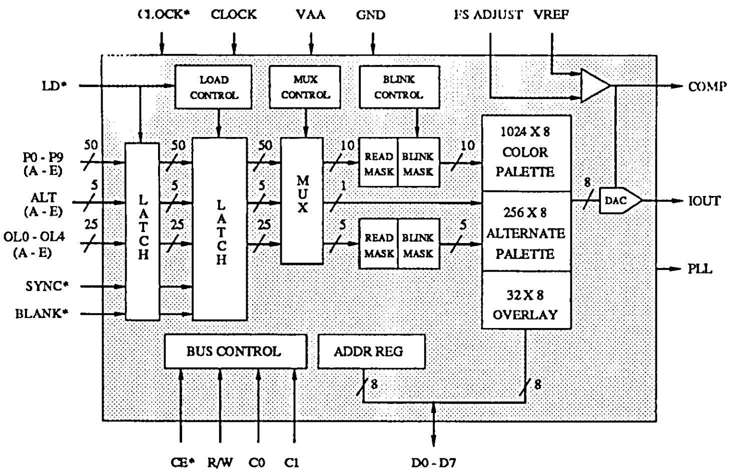
Applications

- High-Resolution Color Graphics
- True-Color Graphics Systems
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt431, Bt438, Bt439
- Bt459, Bt460, Bt468

Functional Block Diagram


CLOCK*
CLOCK
VAA
GND
FS ADJUST
VREF
LD*
LOAD CONTROL
MUX CONTROL
BLINK CONTROL
COMP
P0 - P9 (A - E)
ALT (A - E)
OL0 - OL4 (A - E)
SYNC*
BLANK*
50
5
25
LATCH
LATCH
MUX
10
1
READ MASK
BLINK MASK
1024 X 8 COLOR PALETTE
256 X 8 ALTERNATE PALETTE
32 X 8 OVERLAY
8
DAC
IOUT
PLL
BUS CONTROL
ADDR REG
CE*
R/W
C0
C1
D0 - D7

Product Description

The Bt461/462 single-channel RAMDACs are designed specifically for high-performance, high-resolution color graphics. The multiple pixel ports and internal multiplexing enable TTL-compatible interfacing (up to 45 MHz) to the frame buffer, while maintaining the 170-MHz video data rates required for sophisticated color graphics.

On chip features include a 1024 x 8 dual-port color palette RAM, a 256 x 8 dual-port alternate color palette RAM, 32 x 8 overlay color palette RAM, programmable 3:1, 4:1, or 5:1 input multiplexing of the pixel and overlay ports, bit plane masking and blinking, programmable setup (0 or 7.5 IRE), and pixel panning support.

The Bt462 also supports an optional underlay mode; only 15 overlays are available when the underlay is used.

Color data may be written to and read from the Bt461/462 by the MPU each cycle or using red, green, blue cycles. The MPU interface operates asynchronously to the pixel data, simplifying system design.

The PLL current output enables the synchronization of multiple Bt461/462s with sub-pixel resolution.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L461001 Rev. H

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt461/462 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs and dual-port overlay RAM allow color updating without contention with the display refresh process.

As illustrated in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 10-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit.

There are two ways of reading and writing color data to the device, as controlled by command register_0. The first mode (normal mode), loads color data into the device each write cycle, and outputs color data from the device each read cycle. The second mode (RGB mode) loads color data into the device using red, green, blue write cycles, and outputs data from the device using red, green, blue read cycles. The device is configured to respond only to the color cycle specified by the command register.

Reading/Writing Color Data (Normal Mode)

To write color data, the MPU loads the address register with the address of the primary color palette RAM, alternate color palette RAM, or overlay RAM location to be modified. The MPU performs a color write cycle, using C0 and C1 to select either the primary color palette RAM, alternate color palette RAM, or the overlay palette RAM. The address register then increments to the next location, which the MPU may modify by simply writing another color. Reading color data is similar to writing, except the MPU executes read cycles.

This mode is useful if a 24-bit data bus is available, as 24 bits of color information (8 bits each of red, green, blue) may be read or written to three Bt461/462s in a single MPU cycle. In this application, the CE* inputs of all three Bt461/462s are connected together. If only an 8-bit data bus is available, the CE* inputs must be individually selected during the appropriate color write cycle (red CE* during red write cycle, blue CE* during blue write cycle, etc.).

When accessing the primary color palette RAM, the address register resets to $0000 after a read or write cycle to location $03FF. When accessing the color palette RAMs or the overlay RAM, the address register increments after each read or write cycle.

ADDR0–15	C1	C0	Addressed by MPU
$xxxx	0	0	address register low (ADDR0–7)
$xxxx	0	1	address register high (ADDR8–9)
$0000–$00FF	1	0	alternate color palette RAM
$0100	1	0	overlay color 0
:	:	:	:
$011F	1	0	overlay color 31
$0200	1	0	ID register
$0201	1	0	command register_0
$0202	1	0	command register_1
$0203	1	0	command register_2
$0204	1	0	pixel read mask register low
$0205	1	0	pixel read mask register high
$0206	1	0	pixel blink mask register low
$0207	1	0	pixel blink mask register high
$0208	1	0	overlay read mask register
$0209	1	0	overlay blink mask register
$020C	1	0	test register
$0000–$03FF	1	1	primary color palette RAM

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Reading/Writing Color Data (RGB Mode)

To write color data, the MPU loads the address register with the address of the primary color palette RAM, alternate color palette RAM, or overlay RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the primary color palette RAM, alternate color palette RAM, or overlay RAM. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. Reading color data is similar to writing, except the MPU executes read cycles.

This mode is useful if only an 8-bit data bus is available. Each Bt461/462 is programmed to be a red, green, or blue RAMDAC, and will respond only to the assigned color read or write cycle. In this application, the Bt461/462s share a common 8-bit data bus. The CE* inputs of all three Bt461/462s must be asserted simultaneously only during color read/write cycles and address register write cycles.

When accessing the primary color palette RAM, the address register resets to $0000 after a blue read or write cycle to location $03FF. When accessing the color palette RAMs or the overlay RAM, the address register increments after each blue read or write cycle. To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits (ADDRa, ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 10 bits of the address register (ADDR0–9) are accessible to the MPU.

Command register0 is used to specify whether the device loads or outputs data during the red, green, or blue cycle. This mode is useful if only an 8-bit data bus is available, and the software drivers are written for RGB operation.

Note that CE* must be a logical zero during each of the red, green, blue read/write cycles.

Additional Information

Although the color palette RAMs and overlay RAM are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Accessing the control registers is also done through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. The address register does not increment following read or write cycles to the control registers, facilitating read-modify-write operations. ADDR0 and ADDR8 correspond to D0. ADDR10–ADDR15 are always a logical zero.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing of the Bt461/462.

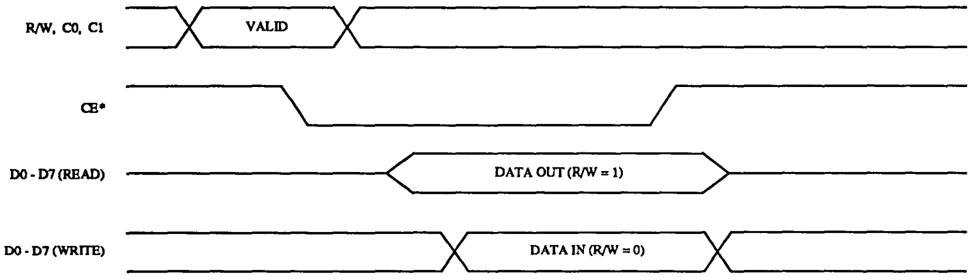


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt461/462 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, and overlay information, for either three, four, or five consecutive pixels, are latched into the device. Note that with this configuration, the sync and blank timing will be recognized only with three, four, or five pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing and to clock the video DRAMs.

Typically, the {A} pixel is output first, followed by the {B} pixel, etc, until all three, four, or five pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external circuitry.

To simplify the frame buffer interface timing, LD* may be phase-shifted, in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by three, four, or five, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than three, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 3:1 multiplexing is specified, only one rising edge of LD* should occur every three clock cycles. If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. If 5:1 multiplexing is specified, only one rising edge of LD* should occur every five clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*.

Note that 3:1 multiplexing may not be used at the 170 MHz pixel clock rate.

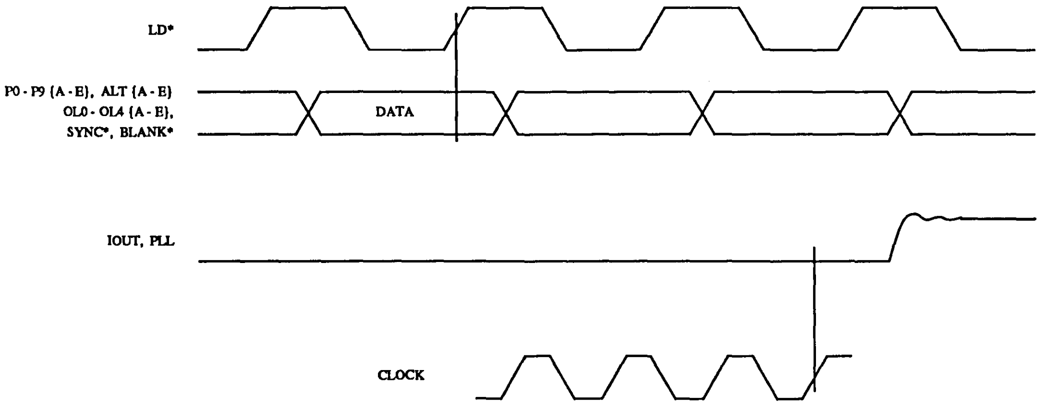


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Read and Blink Masking

Each clock cycle, 10 bits of color information (P0–P9, ALT) and 5 bits of overlay information (OL0–OL4) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual pixel and overlay inputs may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change due to blinking does not occur during the active display time (i.e., in the middle of the screen), the Bt461/462 monitors the BLANK* input to determine vertical retrace intervals. A vertical retrace interval is recognized by determining that BLANK* has been a logical zero for at least 256 LD* cycles.

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAMs, and OL0 is the LSB when addressing the overlay palette RAM. Table

Alternate Color Palette RAM

Note that the pixel read mask and blink mask registers can also be used when the pixel inputs are addressing the alternate color palette RAM.

If the ALT enable bit in command register_0 is a logical one, the alternate color palette RAM may be accessed on a pixel basis. A logical one on an ALT {A–E} input forces the P0–P7 {A–E} inputs to address the alternate color palette RAM. P8 and P9 {A–E} are ignored in this instance. If the ALT enable bit in command register_0 is a logical zero, the ALT {A–E} inputs are ignored, as shown in Tables 2 and 3.

Pixel bypassing of the primary color palette RAM may be implemented by using the ALT inputs. In this instance, the alternate color palette RAM should be loaded so that each byte contains its corresponding address ($00–$FF), or with a gamma correction factor. The ALT inputs would then specify, on a pixel basis, whether or not to bypass the primary color palette RAM.

CR04	ALT	CR05	OL0 - OL4	P0 - P9	Addressed by frame buffer
x	x	x	$1F	$xxx	overlay color 31
:	:	:	:	:	:
x	x	x	$01	$xxx	overlay color 1
x	x	1	$00	$xxx	overlay color 0
0	x	0	$00	$000	primary RAM location $000
0	x	x	$00	$001	primary RAM location $001
:	:	:	:	:	:
0	x	x	$00	$3FF	primary RAM location $3FF
x	0	0	$00	$000	primary RAM location $000
x	0	x	$00	$001	primary RAM location $001
:	:	:	:	:	:
x	0	x	$00	$3FF	primary RAM location $3FF
1	1	0	$00	$x00	alternate RAM location $00
:	:	x	:	$x01	alternate RAM location $01
:	:	:	:	:	:
1	1	x	$00	$xFF	alternate RAM location $FF

Table 2. Bt461—Palette and Overlay Select Truth Table.

Circuit Description (continued)

CR22	CR04	ALT	CR05	OL4	OL0–OL3	P0–P9	Addressed by Frame Buffer
x	x	x	x	1	1111	$xxx	overlay color 31
:	:	:	:	:	:	:	:
:	:	:	:	1	0000	:	overlay color 16
:	:	:	:	0	1111	:	overlay color 15
:	:	:	x	:	:	:	:
x	x	x	1	0	0000	$xxx	overlay color 0
0	0	x	0	0	0000	$000	primary RAM location $000
x	:	:	x	:	:	$001	primary RAM location $001
:	:	:	:	:	:	:	:
x	0	x	x	0	0000	$3FF	primary RAM location $3FF
0	x	0	0	0	0000	$000	primary RAM location $000
x	:	:	x	:	:	$001	primary RAM location $001
:	:	:	:	:	:	:	:
x	x	0	x	0	0000	$3FF	primary RAM location $3FF
x	1	1	x	0	0000	$x00	alternate RAM location $00
:	:	:	:	:	:	:	:
x	1	1	x	0	0000	$xFF	alternate RAM location $FF
1	x	x	x	0	1111	$xxx	overlay color 15
:	:	:	:	:	:	:	:
:	:	:	x	0	0001	$xxx	overlay color 1
1	x	x	0	1	0000	$000	overlay color 0 (underlay)

Table 3. Bt462—Palette and Overlay Select Truth Table.

Circuit Description (continued)

Pixel Panning

To support pixel panning, command register_1 specifies by how many clock cycles to pan.

If 0-pixel panning is specified, pixel {A} is output first, followed by pixel {B}, etc., until all 3, 4, or 5 pixels have been output, at which point the cycle repeats.

If 1-pixel panning is specified, pixel {B} will be first, followed by pixel {C}, etc. Pixel {A} will have been processed during the last clock cycle of the blanking interval, and will not be seen on the display screen. At the end of the active display line, pixel {A} will be output. Pixels {B}, {C}, {D}, and {E} will be output during the blanking interval, and will not be seen on the display screen.

The process is similar for panning by 2, 3, or 4 pixels.

Note that when a panning value other than 0 pixels is specified, valid pixel data must be loaded into the Bt461/462 during the first LD* cycle that BLANK* is a logical zero.

The pixel, overlay, and ALT inputs are all panned.

Underlay Operation (Bt462 Only)

An underlay plane can be obtained by converting overlay plane 4 (OL4) to underlay operation (command register bit CR22). In this mode of operation, only 15 overlays (OL0–OL3) are available, as shown in Table 3.

Note that, during underlay operation, the corresponding overlay plane 4 (OL4) overlay read mask register bit must be a logical zero for proper operation.

Underlays may be displayed on a pixel basis. Both overlays and the underlay may be used at the same time. The priority of the display information is:

overlays (OL0–OL3)
pixel data (P0–P9)
underlay (OL4)

Video Generation

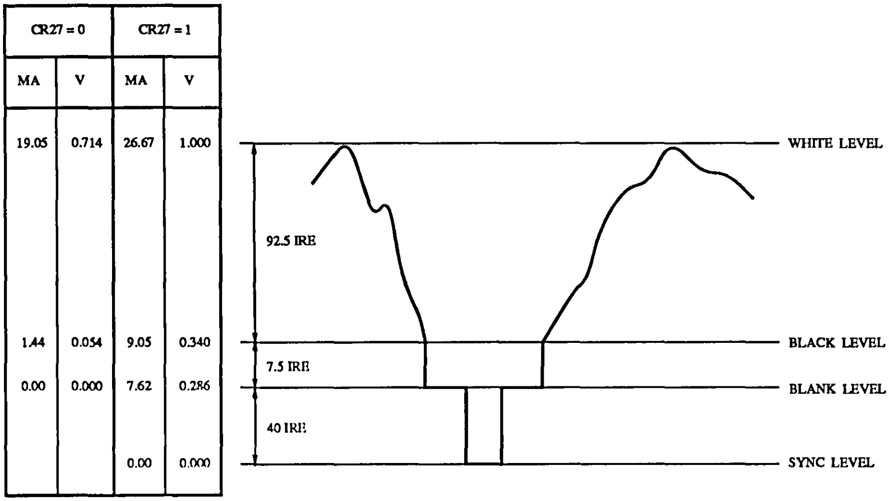
Every clock cycle, the selected 8 bits of color information are presented to the 8-bit D/A converter.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 3 and 4. Command register2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated, and whether or not sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converter produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 4 and 5 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converter on the Bt461/462 uses a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Circuit Description (continued)


CR27 = 0
CR27 = 1
MA
V
MA
V
19.05
0.714
26.67
1.000
1.44
0.054
9.05
0.340
0.00
0.000
7.62
0.286
0.00
0.000
WHITE LEVEL
92.5 IRE
BLACK LEVEL
7.5 IRE
BLANK LEVEL
40 IRE
SYNC LEVEL

Note: 75 Ω doubly terminated load, RSET = 523 Ω, VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances assumed on all levels.

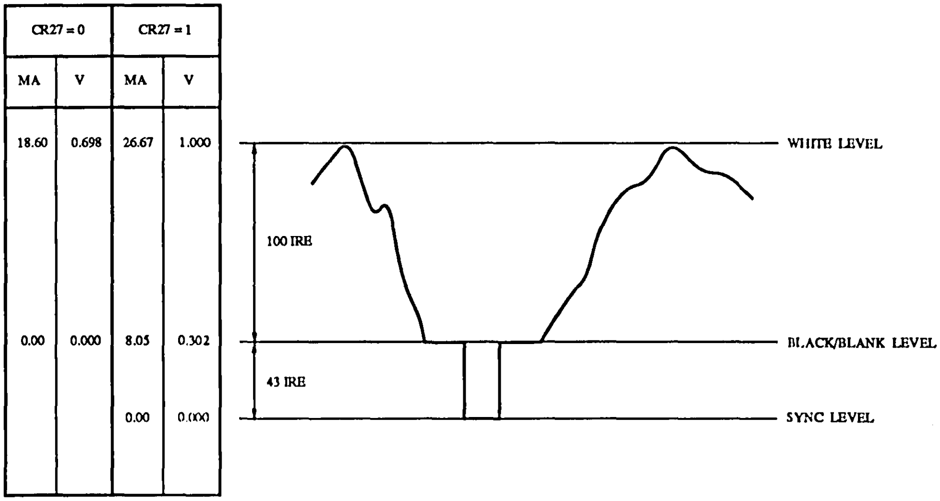
Figure 3. Composite Video Output Waveform (SETUP = 7.5 IRE).

Description	IOUT (mA) (CR27 = 1)	IOUT (mA) (CR27 = 0)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOUT = 26.67 mA. RSET = 523 Ω, VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 4. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)



Note: 75 Ω doubly terminated load, RSET = 495 Ω, VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances assumed on all levels.

Figure 4. Composite Video Output Waveform (SETUP = 0 IRE).

Description	IOUT (mA) (CR27 = 1)	IOUT (mA) (CR27 = 0)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOUT = 26.67 mA. RSET = 495 Ω VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 5. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register_0

This register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to data bus bit D0.

CR07, CR06	Multiplex select (00) 3:1 multiplexing (01) 4:1 multiplexing (10) reserved (11) 5:1 multiplexing	These bits specify whether 3:1, 4:1, or 5:1 multiplexing is to be used for the pixel and overlay inputs. If 3:1 is specified, the {D} and {E} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be 1/3 the CLOCK rate. If 4:1 is specified, the {E} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be 1/4 the CLOCK rate. If 5:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be 1/5 the CLOCK rate. Note that it is possible to reset the pipeline delay of the Bt461/462 to a fixed eight clock cycles. In this instance, each time the input multiplexing is changed, the Bt461/462 must again be reset to a fixed pipeline delay. **Note that 3:1 multiplexing may not be used at the 170 MHz pixel clock rate.**
CR05	Overlay 0 enable (0) use color palette RAMs (1) use overlay color 0	When the overlay bits are $00, this bit specifies whether to use the color palette RAMs or overlay color 0 to provide color information.
CR04	ALT enable (0) disable alternate palette (1) enable alternate palette	This bit specifies whether the alternate color palette RAM is enabled (logical one) or disabled (logical zero) from being addressed by the ALT {A–E} and P0–P7 {A–E} inputs.
CR03, CR02	Blink rate selection (00) 16 on, 48 off (25/75) (01) 16 on, 16 off (50/50) (10) 32 on, 32 off (50/50) (11) 64 on, 64 off (50/50)	These 2 bits specify the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (% on/off).
CR01	reserved (logical zero)	
CR00	reserved (logical zero)	

Internal Registers (continued)

Command Register_1

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0.

CR17–CR15	Pan select (000) 0 pixels {pixel A} (001) 1 pixel {pixel B} (010) 2 pixels {pixel C} (011) reserved (100) 3 pixels {pixel D} (101) 4 pixels {pixel E} (110) reserved (111) reserved	These bits specify the number of pixels to be panned. The {pixel A} indicates pixel A will be output first following the blanking interval, {pixel B} indicates pixel B will be output first, etc. These bits are typically modified only during the vertical retrace interval. Note that the pixel, overlay, and ALT inputs are all panned.
CR14–CR10	reserved (logical zero)	

Internal Registers (continued)

Command Register_2

This register may be written to or read by the MPU at any time and is not initialized. CR20 corresponds to data bus bit D0.

CR27	Sync enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto the video waveform (logical one) or not (logical zero).
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video waveform. 0 IRE specifies that the black and blank levels are the same.
CR25, CR24	Load palette RAM select (00) normal (01) red RAMDAC (10) green RAMDAC (11) blue RAMDAC	If (00) is specified, color data is loaded into the Bt461/462 each write cycle, and color data is output each read cycle. If (01), (10), or (11) is specified, the Bt461/462 expects color data to be input and output using (red, green, blue) cycles. The exact value indicates during which one of the three color cycles it is to load or output color information.
CR23	PLL select (0) SYNC* (1) BLANK*	This bit specifies whether the PLL output uses the SYNC* or BLANK* input for generating PLL information.
CR22	Bt461—reserved (logical zero) Bt462—Underlay enable (0) overlay plane 4 (1) underlay plane 0	This bit is always a logical zero on the Bt461. On the Bt462, this bit specifies whether overlay plane 4 (OL4) should be converted to an underlay plane (logical one) or be used as a normal overlay plane (logical 0).
CR21	reserved (logical zero)	
CR20	Test enable (0) disable test register (1) enable test register	A logical one enables the P9 {A–E} inputs to serve as a trigger for the test register. A logical zero enables normal operation.

Internal Registers (continued)

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt461/462, the value read by the MPU will be $4D for the Bt461 and $4C for the Bt462. Data written to this register is ignored.

Pixel Read Mask Register

The 16-bit pixel read mask register is configured as two 8-bit registers (pixel read mask low and pixel read mask high), and is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM.

pixel read mask register high								pixel read mask register low							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized.

Pixel Blink Mask Register

The 16-bit pixel blink mask register is configured as two 8-bit registers (pixel blink mask low and pixel blink mask high), and is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0.

pixel blink mask register high								pixel blink mask register low							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0

In order for a bit plane to blink, the corresponding bit in the pixel read mask register must be a logical one. This register may be written to or read by the MPU at any time and is not initialized.

Internal Registers (continued)

Overlay Read Mask Register

The 8-bit overlay read mask register is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette RAM. D0 corresponds to overlay plane 0 (OL0 {A–E}) and D4 corresponds to overlay plane 4 (OL4 {A–E}). Each register bit is logically ANDed with the corresponding overlay plane input. Bits D5–D7 are always a logical zero. This register may be written to or read by the MPU at any time and is not initialized.

On the Bt462, the overlay read mask register for overlay plane 4 (OL4) must be a logical zero when using the underlay mode.

Overlay Blink Mask Register

The 8-bit overlay blink mask register is used to enable (logical one) or disable (logical zero) an overlay plane from blinking at the blink rate and duty cycle specified by command register_0. D0 corresponds to overlay plane 0 (OL0 {A–E}) and D4 corresponds to overlay plane 4 (OL4 {A–E}). In order for an overlay plane to blink, the corresponding bit in the overlay read mask register must be a logical one. Bits D5–D7 are always a logical zero. This register may be written to or read by the MPU at any time and is not initialized.

Test Register

The test register enables the MPU to verify that the pixel and overlay ports are addressing the color palette RAM and overlay registers correctly at full speed.

P9 {A–E} is the fast port trigger when CR20 is a logical one. P0–P8 {A–E}, ALT {A–E}, and OL0–OL4 {A–E} address the primary color palette RAM, alternate palette RAM, and overlay registers. A logical one on P9A latches the {A} color data into the test register as it is passed from the color palette to the D/A converter. A logical one on P9B latches the {B} color data into the test register as it is passed from the color palette to the D/A converter, etc.

To test the entire color palette, bit D1 in the pixel read mask register high (P9) must be a logical zero to test the lower 512 entries. Next, bit D1 in the pixel read mask register high (P9) must be a logical one to test the higher 512 entries. There should be only a single "one" on the P9 inputs per test read cycle.

A recommended test read cycle is four LD* cycles long. The test register may be written whenever the test mode is disabled or while in the test mode when no "ones" are present on the P9 inputs. The test registers are not initialized.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as illustrated in Tables 4 and 5. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input typically switches off a 40 IRE current source on the IOUT output (see Figures 3 and 4). SYNC* does not override any other control or data input, as shown in Tables 4 and 5; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0–P9 {A–E}, OL0–OL4 {A–E}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD*, while it is either 1/3, 1/4, or 1/5 the CLOCK rate, may be phase-independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle, within the limits specified by the AC Characteristics section.
P0–P9 {A–E}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which location of the primary or alternate color palette RAMs is to be used to provide color information (see Table 2). Either three, four, or five consecutive pixels (up to 10 bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Note that typically the {A} pixel is output first, followed by the {B} pixel, etc., until all three, four, or five pixels have been output, at which point the cycle repeats.
OL0–OL4 {A–E}	Overlay select inputs (TTL compatible). These inputs are latched on the rising edge of LD*, and in conjunction with CR05 in command register_0, specify which palette is to be used for color information, as illustrated in Table 2. When accessing the overlay palette RAM, the P0–P9 {A–E} and ALT {A–E} inputs are ignored. Overlay information bits (up to 5 bits per pixel) for either three, four, or five consecutive pixels are input through this port. Unused inputs should be connected to GND.
ALT {A–E}	Palette select inputs (TTL compatible). These inputs are latched on the rising edge of LD* and specify which color palette RAM is to be used for color information, as illustrated in Table 2. When accessing the alternate color palette RAM, the P8–P9 {A–E} inputs are ignored. Unused inputs should be connected to GND.
IOUT	Analog current output. This high-impedance current source is capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 5).
PLL	Phase lock loop output current. This high-impedance current source is used to enable multiple Bt461/462s to be synchronized with sub-pixel resolution when used with an external PLL. A logical one on the SYNC* or BLANK* input (as specified by CR23 in command register_2) results in no current being output onto this pin, while a logical zero results in the following current being output: $\text{PLL (mA)} = 3{,}227 * \text{VREF (V)} / \text{RSET } (\Omega)$ If sub-pixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 Ω).

Pin Descriptions (continued)

Pin Name	Description
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 5). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. Refer to *PC Board Layout Considerations* for critical layout criteria.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 5). Note that the IRE relationships in Figures 3 and 4 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOUT for a 7.5 IRE blanking pedestal is: $\text{RSET}\ (\Omega) = 11{,}294 * \text{VREF}\ (\text{V}) / \text{IOUT}\ (\text{mA})$ The relationship between RSET and the full scale output current on IOUT for a 0 IRE blanking pedestal is: $\text{RSET}\ (\Omega) = 10{,}684 * \text{VREF}\ (\text{V}) / \text{IOUT}\ (\text{mA})$
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 5, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 5. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE* (Figure 1). Care should be taken to avoid glitches on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.

Pin Descriptions (continued)—132-pin PGA Package

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	L1	P8A	G14	VAA	J1
SYNC*	K3	P8B	G13	VAA	J2
LD*	A5	P8C	F14	VAA	J3
CLOCK	K1	P8D	F13	VAA	C6
CLOCK*	K2	P8E	E14	VAA	F12
				VAA	M9
P0A	E3	P9A	J13		
P0B	D2	P9B	J14	GND	H1
P0C	D1	P9C	H12	GND	H2
P0D	E2	P9D	H13	GND	H3
P0E	F3	P9E	H14	GND	C7
				GND	G12
P1A	A1	ALTA	L14	GND	M8
P1B	D3	ALTB	K12		
P1C	C2	ALTC	K13	COMP	N9
P1D	B1	ALTD	K14	FS ADJUST	M10
P1E	C1	ALTE	J12	VREF	P9
P2A	A3	OL0A	E1	CE*	P13
P2B	B3	OL0B	F2	R/W	N12
P2C	A2	OL0C	F1	C1	P12
P2D	C3	OL0D	G3	C0	M11
P2E	B2	OL0E	G2		
				D0	L13
P3A	A8	OL1A	M1	D1	M14
P3B	A7	OL1B	L2	D2	L12
P3C	B7	OL1C	N1	D3	M13
P3D	A6	OL1D	L3	D4	N14
P3E	B6	OL1E	M2	D5	P14
				D6	N13
P4A	C9	OL2A	M3	D7	M12
P4B	B9	OL2B	N2		
P4C	A9	OL2C	P1	reserved	G1
P4D	C8	OL2D	P2	reserved	N11
P4E	B8	OL2E	N3	reserved	M7
				reserved	N7
P5A	B11	OL3A	M4	reserved	P7
P5B	A11	OL3B	P3	reserved	P8
P5C	C10	OL3C	N4	reserved	N8
P5D	B10	OL3D	P4		
P5E	A10	OL3E	M5	reserved	B5
				reserved	C5
P6A	A14	OL4A	N5	reserved	A4
P6B	A13	OL4B	P5	reserved	B4
P6C	B12	OL4C	M6	reserved	C4
P6D	C11	OL4D	N6		
P6E	A12	OL4E	P6	reserved	C14
				reserved	C13
P7A	E13	IOUT	P10	reserved	B14
P7B	E12	reserved	P11	reserved	C12
P7C	D14	PLL	N10	reserved	B13
P7D	D13				
P7E	D12				

Pin Descriptions (continued)—132-pin PGA Package

Bt461/462

(TOP VIEW)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
14	P6A	N/C	N/C	P7C	P8E	P8C	P8A	P9E	P9B	ALTD	ALTA	D1	D4	D5
13	P6B	N/C	N/C	P7D	P7A	P8D	P8B	P9D	P9A	ALTC	D0	D3	D6	CE*
12	P6E	P6C	N/C	P7E	P7B	VAA	GND	P9C	ALTE	ALTB	D2	D7	R/W	C1
11	P5B	P5A	P6D									C0	N/C	N/C
10	P5E	P5D	P5C									FS ADJ	PLL	IOUT
9	P4C	P4B	P4A									VAA	COMP	VREF
8	P3A	P4E	P4D									GND	N/C	N/C
7	P3B	P3C	GND									N/C	N/C	N/C
6	P3D	P3E	VAA									OL4C	OL4D	OL4E
5	LD*	N/C	N/C									OL3E	OL4A	OL4B
4	N/C	N/C	N/C									OL3A	OL3C	OL3D
3	P2A	P2B	P2D	P1B	P0A	P0E	OL0D	GND	VAA	SYNC*	OL1D	OL2A	OL2E	OL3B
2	P2C	P2E	P1C	P0B	P0D	OL0B	OL0E	GND	VAA	CLK*	OL1B	OL1E	OL2B	OL2D
1	P1A	P1D	P1E	P0C	OL0A	OL0C	N/C	GND	VAA	CLK	BLK*	OL1A	OL1C	OL2C

alignment marker (on top)

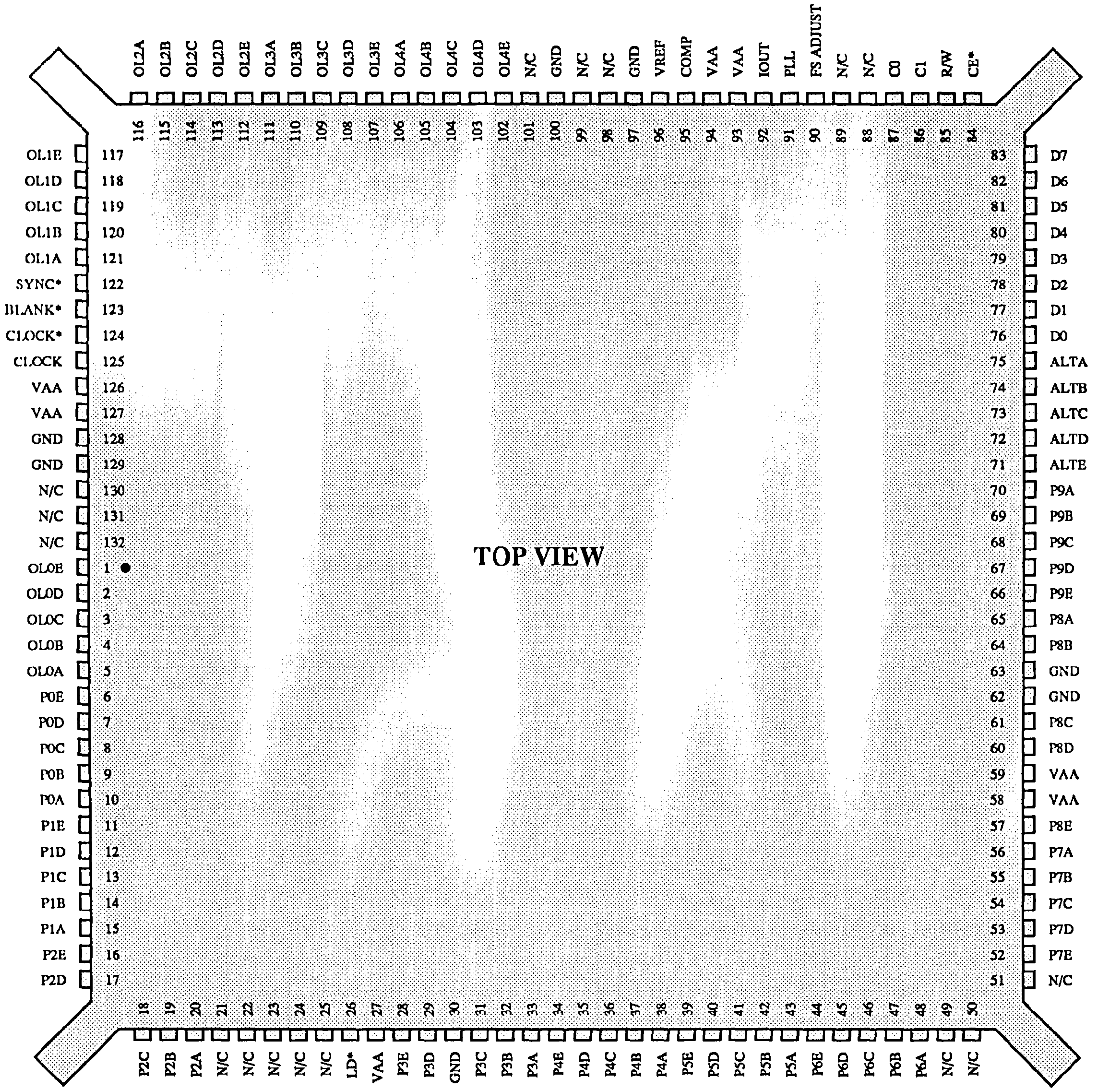
(BOTTOM VIEW)

	P	N	M	L	K	J	H	G	F	E	D	C	B	A
14	D5	D4	D1	ALTA	ALTD	P9B	P9E	P8A	P8C	P8E	P7C	N/C	N/C	P6A
13	CE*	D6	D3	D0	ALTC	P9A	P9D	P8B	P8D	P7A	P7D	N/C	N/C	P6B
12	C1	R/W	D7	D2	ALTB	ALTE	P9C	GND	VAA	P7B	P7E	N/C	P6C	P6E
11	N/C	N/C	C0									P6D	P5A	P5B
10	IOUT	PLL	FS ADJ									P5C	P5D	P5E
9	VREF	COMP	VAA									P4A	P4B	P4C
8	N/C	N/C	GND									P4D	P4E	P3A
7	N/C	N/C	N/C									GND	P3C	P3B
6	OL4E	OL4D	OL4C									VAA	P3E	P3D
5	OL4B	OL4A	OL3E									N/C	N/C	LD*
4	OL3D	OL3C	OL3A									N/C	N/C	N/C
3	OL3B	OL2E	OL2A	OL1D	SYNC*	VAA	GND	OL0D	P0E	P0A	P1B	P2D	P2B	P2A
2	OL2D	OL2B	OL1E	OL1B	CLK*	VAA	GND	OL0E	OL0B	P0D	P0B	P1C	P2E	P2C
1	OL2C	OL1C	OL1A	BLK*	CLK	VAA	GND	N/C	OL0C	OL0A	P0C	P1E	P1D	P1A

Pin Descriptions (continued)—132-pin PQFP Package (Bt462 Only)

Pin Number	Signal
1	OL0E
2	OL0D
3	OL0C
4	OL0B
5	OL0A
6	P0E
7	P0D
8	P0C
9	P0B
10	P0A
11	P1E
12	P1D
13	P1C
14	P1B
15	P1A
16	P2E
17	P2D
18	P2C
19	P2B
20	P2A
21	reserved
22	reserved
23	reserved
24	reserved
25	reserved
26	LD*
27	VAA
28	P3E
29	P3D
30	GND
31	P3C
32	P3B
33	P3A
34	P4E
35	P4D
36	P4C
37	P4B
38	P4A
39	P5E
40	P5D
41	P5C
42	P5B
43	P5A
44	P6E
45	P6D
46	P6C
47	P6B
48	P6A
49	reserved
50	reserved
51	reserved
52	P7E
53	P7D
54	P7C
55	P7B
56	P7A
57	P8E
58	VAA
59	VAA
60	P8D
61	P8C
62	GND
63	GND
64	P8B
65	P8A
66	P9E
67	P9D
68	P9C
69	P9B
70	P9A
71	ALTE
72	ALTD
73	ALTC
74	ALTB
75	ALTA
76	D0
77	D1
78	D2
79	D3
80	D4
81	D5
82	D6
83	D7
84	CE*
85	R/W
86	C1
87	C0
88	reserved
89	reserved
90	FS ADJUST
91	PLL
92	IOUT
93	VAA
94	VAA
95	COMP
96	VREF
97	GND
98	reserved
99	reserved
100	GND
101	reserved
102	OL4E
103	OL4D
104	OL4C
105	OL4B
106	OL4A
107	OL3E
108	OL3D
109	OL3C
110	OL3B
111	OL3A
112	OL2E
113	OL2D
114	OL2C
115	OL2B
116	OL2A
117	OL1E
118	OL1D
119	OL1C
120	OL1B
121	OL1A
122	SYNC*
123	BLANK*
124	CLOCK*
125	CLOCK
126	VAA
127	VAA
128	GND
129	GND
130	reserved
131	reserved
132	reserved

Pin Descriptions (continued)—132-pin PQFP Package (Bt462 Only)


TOP VIEW
117 OL1E
118 OL1D
119 OL1C
120 OL1B
121 OL1A
122 SYNC*
123 BLANK*
124 CLOCK*
125 CLOCK
126 VAA
127 VAA
128 GND
129 GND
130 N/C
131 N/C
132 N/C
1 OL0E
2 OL0D
3 OL0C
4 OL0B
5 OL0A
6 P0E
7 P0D
8 P0C
9 P0B
10 P0A
11 P1E
12 P1D
13 P1C
14 P1B
15 P1A
16 P2E
17 P2D
18 P2C
19 P2B
20 P2A
21 N/C
22 N/C
23 N/C
24 N/C
25 N/C
26 LD*
27 VAA
28 P3E
29 P3D
30 GND
31 P3C
32 P3B
33 P3A
34 P4E
35 P4D
36 P4C
37 P4B
38 P4A
39 P5E
40 P5D
41 P5C
42 P5B
43 P5A
44 P6E
45 P6D
46 P6C
47 P6B
48 P6A
49 N/C
50 N/C
51 N/C
52 P7E
53 P7D
54 P7C
55 P7B
56 P7A
57 P8E
58 VAA
59 VAA
60 P8D
61 P8C
62 GND
63 GND
64 P8B
65 P8A
66 P9E
67 P9D
68 P9C
69 P9B
70 P9A
71 ALTE
72 ALTD
73 ALTC
74 ALTB
75 ALTA
76 D0
77 D1
78 D2
79 D3
80 D4
81 D5
82 D6
83 D7
84 CE*
85 R/W
86 C1
87 C0
88 N/C
89 N/C
90 FS ADJUST
91 PLL
92 IOUT
93 VAA
94 VAA
95 COMP
96 VREF
97 GND
98 N/C
99 N/C
100 GND
101 N/C
102 OL4E
103 OL4D
104 OL4C
105 OL4B
106 OL4A
107 OL3E
108 OL3D
109 OL3C
110 OL3B
111 OL3A
112 OL2E
113 OL2D
114 OL2C
115 OL2B
116 OL2A

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in the *Bt451/7/8 Evaulation Module Operation and Measures*, application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt461/462 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a 6-layer PC board is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane (preferably analog ground plane), layer 3 the analog power plane, using the remaining layers for digital traces and digital power supplies.

The optimum layout enables the Bt461/462 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8 inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground partitioning isolation technique is constrained by the noise margin degradation during digital readback of the Bt461/462.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

For maximum performance, a separate isolated ground plane for the analog output termination resistors, RSET resistor, and VREF circuitry should be used, as shown in Figure 5. Another isolated ground plane is used for the GND pins of the Bt461/462 and supply decoupling capacitors.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt461/462 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8 inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 5. This bead should be located within 3 inches of the Bt461/462 and provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor decoupling each of four groups of VAA pins to GND. The capacitors should be placed as close as possible to the device.

The 33 µF capacitor is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. Lead lengths should be minimized for best performance so that the self-resonance frequency is greater than the LD* frequency.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt461/462 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt461/462 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt461/462 to minimize reflections. Unused analog outputs should be connected to GND.

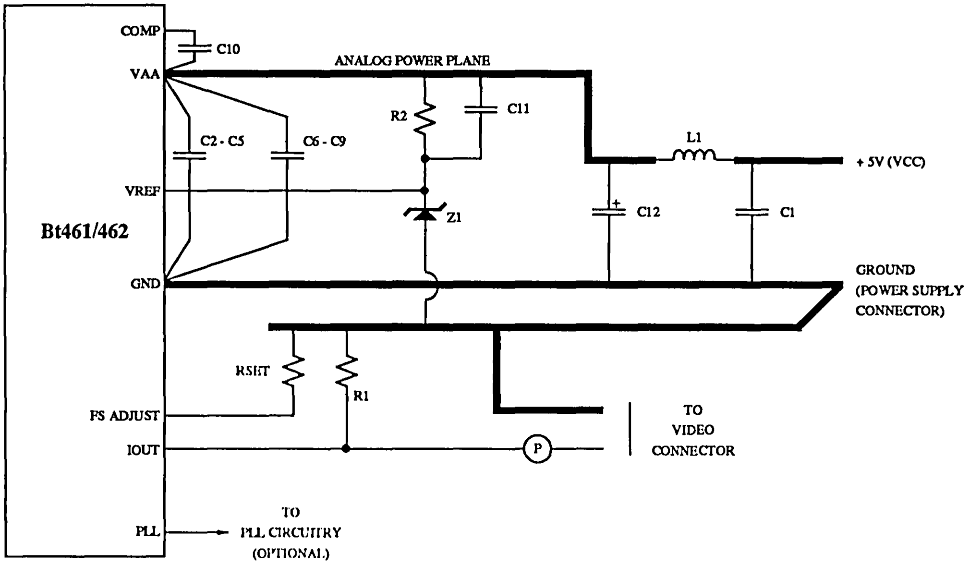
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

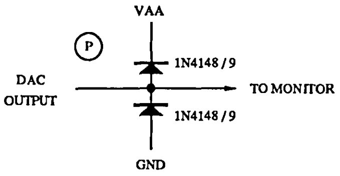
Analog Output Protection

The Bt461/462 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 5 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)


COMP
C10
VAA
ANALOG POWER PLANE
R2
C11
C2 - C5
C6 - C9
L1
+ 5V (VCC)
VREF
Z1
C12
C1
Bt461/462
GND
GROUND
(POWER SUPPLY
CONNECTOR)
RSET
R1
FS ADJUST
TO
VIDEO
CONNECTOR
IOUT
P
PLL
TO
PLL CIRCUITRY
(OPTIONAL)


VAA
P
1N4148 / 9
DAC
OUTPUT
TO MONITOR
1N4148 / 9
GND

Location	Description	Vendor Part Number
C1–C5, C10, C11	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C6–C9	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C12	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1	75 Ω 1% metal film resistor	Dale CMF-55C
R2	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt461/462.

Figure 5. Typical Connection Diagram and Parts List.

Application Information

Non-Video Applications

The Bt461/462 may be used in non-video applications by disabling the video-specific control signals. Set bits CR26 and CR27 in command register_2 to a zero (disabling the BLANK* and SYNC* inputs). SYNC* should be a logical zero and BLANK* should be a logical one.

The relationship between RSET and the full scale output current (Iout) in this configuration is as follows:

RSET (Ω) = 7,457 * VREF (V) / Iout (mA)

Using Multiple Devices

When using multiple Bt461/462s, each Bt461/462 should have its own power plane ferrite bead. In addition, a single voltage reference may drive multiple devices; however, isolation resistors are recommended to reduce color channel crosstalk.

Higher performance may be obtained if each Bt461/462 has its own voltage reference. This may further reduce the amount of color channel crosstalk and color palette interaction.

Each Bt461/462 must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

Due to differences in pipelining and analog output delay, it is recommended that Bt461s not be mixed with B462s.

Clock Interfacing

Due to the high clock rates at which the Bt461/462 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (typically a 220 Ω resistor to VCC and a 330 Ω resistor to GND). The termination resistors should be as close as possible to the Bt461/462.

170 MHz applications require robust ECL clock signals with strong pull-down (~20 mA at VOH) and double termination for clock trace lengths greater than 2 inches.

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak due to the noise margins of the CMOS process. The Bt461/462 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by three, four, or five (depending on whether 3:1, 4:1, or 5:1 multiplexing was specified) and translating it to TTL levels. As LD* may be phase-shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt461, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The pipeline delay of the Bt462, although fixed after a power-up condition, may be anywhere from eight to twelve clock cycles. The Bt461/462 contains additional circuitry enabling the pipeline delay to be fixed (eight clock cycles for the Bt461, ten clock cycles for the Bt462). The Bt438 and Bt439 Clock Generator Chips support this mode of operation when used with the Bt461/462.

To reset the Bt461/462, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for at least three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

The resetting of the Bt461/462 to a fixed pipeline delay also resets the blink counter circuitry. If the Bt461/462 is periodically reset (i.e., every vertical sync interval), the on-chip blink counter will not function correctly. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control via the read mask register and overlay display enable bits.

In standard operation, the Bt461/462 need be reset only following a power-up or reset condition. Under these circumstances the on-chip blink circuitry may be used.

Monochrome Display Applications

For monochrome display applications where a single Bt461/462 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 3:1, 4:1, and 5:1 input multiplexing of the Bt461/462, and sets the pipeline delay of the Bt461/462 to eight (Bt461) or ten (Bt462) clock cycles. The Bt438 may also be used to interface the Bt461/462 to a TTL clock. Figure 6 illustrates using the Bt438 with the Bt461/462.

In applications using a single Bt461/462, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150 Ω).

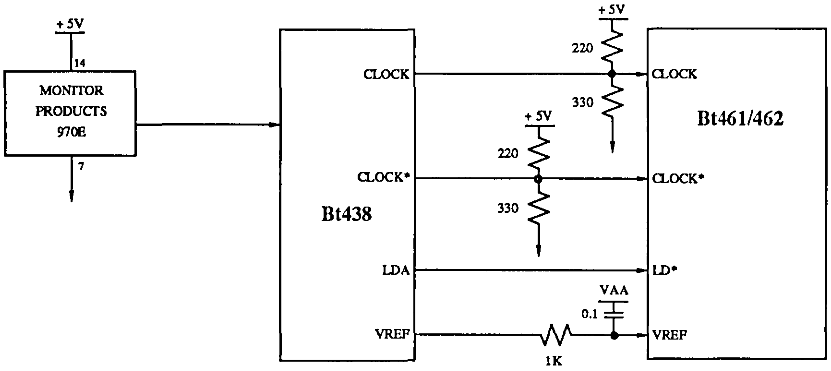


Figure 6. Generating the Bt461/462 Clock Signals (Monochrome Application).

Application Information (continued)

Color Display Applications

For color display applications where up to four Bt461/462s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 3:1, 4:1, and 5:1 input multiplexing of the Bt461/462, synchronizes them to sub-pixel resolution, and sets the pipeline delay of the Bt461 to eight clock cycles (ten clock cycles for the Bt462). The Bt439 may also be used to interface the Bt461/462 to a TTL clock. Figure 7 illustrates using the Bt439 with the Bt461/462.

Sub-pixel synchronization is supported via the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt461/462, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt461/462s, and adjusts the phase of the CLOCK and CLOCK* signals to each Bt461/462 to minimize the PLL phase difference. There should be minimal layout skew in the CLOCK and PLL trace paths to assure proper clock alignment.

If sub-pixel synchronization of multiple Bt461/462s is not necessary, the Bt438 Clock Generator Chip may be used instead of the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt461/462s are connected together, and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). The designer must take care to minimize skew on the CLOCK and CLOCK* lines. The PLL outputs would not be used and should be connected to GND (either directly or through a resistor up to 150 Ω).

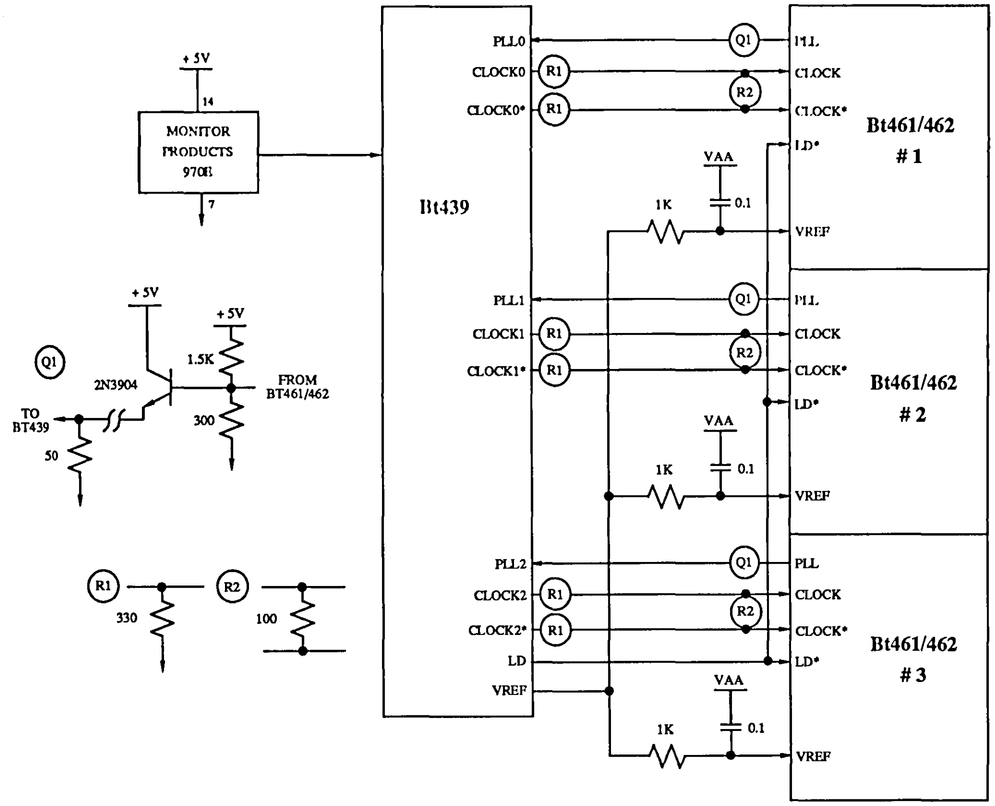

+5V
14
MONITOR PRODUCTS 970B
7
Bt439
PLL0
CLOCK0
CLOCK0*
PLL1
CLOCK1
CLOCK1*
PLL2
CLOCK2
CLOCK2*
LD
VREF
Q1
R1
R2
VAA
1K
0.1
PLL
CLOCK
CLOCK*
LD*
VREF
Bt461/462 #1
Bt461/462 #2
Bt461/462 #3
+5V
+5V
2N3904
1.5K
FROM BT461/462
300
TO BT439
50
330
100

Figure 7. Generating the Bt461/462 Clock Signals (Color Application).

Application Information (continued)

Initializing the Bt461/462 (Monochrome)

Following a power-on sequence, the Bt461/462 must be initialized. This sequence will configure the Bt461/462 as follows:

4:1 multiplexed operation
no overlays
no pixel masking, no blinking, no panning
color data written/read every cycle
sync enabled on IOUT, 7.5 IRE blanking pedestal

Control Register Initialization

	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $02 to address register low	00
Write $00 to command register_1	10
Write $03 to address register low	00
Write $C0 to command register_2	10
Write $04 to address register low	00
Write $FF to pixel read mask low	10
Write $05 to address register low	00
Write $03 to pixel read mask high	10
Write $06 to address register low	00
Write $00 to pixel blink mask low	10
Write $07 to address register low	00
Write $00 to pixel blink mask high	10
Write $08 to address register low	00
Write $00 to overlay read mask	10
Write $09 to address register low	00
Write $00 to overlay blink mask	10

Color Palette RAM Initialization

Write $00 to address register low	00
Write $00 to address register high	01
Write data to RAM (location $000)	11
Write data to RAM (location $001)	11
:	:
Write data to RAM (location $3FF)	11

Overlay Color Palette Initialization

Write $00 to address register low	00
Write $01 to address register high	01
Write data to overlay (location $00)	10
Write data to overlay (location $01)	10
:	:
Write data to overlay (location $1F)	10

Alternate Color Palette Initialization

Write $00 to address register low	00
Write $00 to address register high	01
Write data to alternate (location $00)	10
Write data to alternate (location $01)	10
:	:
Write data to alternate (location $FF)	10

Application Information (continued)

Initializing the Bt461/462 (Color) 8-bit MPU Data Bus

In this example, three Bt461/462s are being used in parallel to generate true color. An 8-bit MPU data bus is available for accessing the Bt461/462s.

Note that while accessing the command, read mask, blink mask, control/test, and address register, each Bt461/462 must be accessed individually. While accessing the color palette RAM, alternate RAM, or overlay registers, all three Bt461/462s may be accessed simultaneously.

Following a power-on sequence, the Bt461/462s must be initialized. This sequence will configure the Bt461/462s as follows:

4:1 multiplexed operation
no overlays
no blinking, no panning
initialize each one as a red, green, or blue device
sync on all outputs, 7.5 IRE blanking pedestal

Control Register Initialization

Red Bt461/462	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $02 to address register low	00
Write $00 to command register_1	10
Write $03 to address register low	00
Write $D0 to command register_2	10
Write $04 to address register low	00
Write $FF to pixel read mask low	10
Write $05 to address register low	00
Write $03 to pixel read mask high	10
Write $06 to address register low	00
Write $00 to pixel blink mask low	10
Write $07 to address register low	00
Write $00 to pixel blink mask high	10
Write $08 to address register low	00
Write $00 to overlay read mask	10
Write $09 to address register low	00
Write $00 to overlay blink mask	10

Green Bt461/462

Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $02 to address register low	00
Write $00 to command register_1	10
Write $03 to address register low	00
Write $E0 to command register_2	10
Write $04 to address register low	00
Write $FF to pixel read mask low	10
Write $05 to address register low	00
Write $03 to pixel read mask high	10
Write $06 to address register low	00
Write $00 to pixel blink mask low	10
Write $07 to address register low	00
Write $00 to pixel blink mask high	10
Write $08 to address register low	00
Write $00 to overlay read mask	10
Write $09 to address register low	00
Write $00 to overlay blink mask	10

Blue Bt461/462

Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $02 to address register low	00
Write $00 to command register_1	10
Write $03 to address register low	00
Write $F0 to command register_2	10
Write $04 to address register low	00
Write $FF to pixel read mask low	10
Write $05 to address register low	00
Write $03 to pixel read mask high	10
Write $06 to address register low	00
Write $00 to pixel blink mask low	10
Write $07 to address register low	00
Write $00 to pixel blink mask high	10
Write $08 to address register low	00
Write $00 to overlay read mask	10
Write $09 to address register low	00
Write $00 to overlay blink mask	10

Application Information (continued)

Color Palette RAM Initialization

Write $00 to all three address low registers	00
Write $00 to all three address high registers	01
Write red data to RAM (location $000)	11
Write green data to RAM (location $000)	11
Write blue data to RAM (location $000)	11
Write red data to RAM (location $001)	11
Write green data to RAM (location $001)	11
Write blue data to RAM (location $001)	11
:	:
Write red data to RAM (location $3FF)	11
Write green data to RAM (location $3FF)	11
Write blue data to RAM (location $3FF)	11

Alternate Color Palette Initialization

Write $00 to all three address low registers	00
Write $00 to all three address high registers	01
Write red data to alternate (location $00)	10
Write green data to alternate (location $00)	10
Write blue data to alternate (location $00)	10
Write red data to alternate (location $01)	10
Write green data to alternate (location $01)	10
Write blue data to alternate (location $01)	10
:	:
Write red data to alternate (location $FF)	10
Write green data to alternate (location $FF)	10
Write blue data to alternate (location $FF)	10

Overlay Color Palette Initialization

Write $00 to all three address low registers	00
Write $01 to all three address high registers	00
Write red data to overlay (location $00)	10
Write green data to overlay (location $00)	10
Write blue data to overlay (location $00)	10
Write red data to overlay (location $01)	10
Write green data to overlay (location $01)	10
Write blue data to overlay (location $01)	10
:	:
Write red data to overlay (location $1F)	10
Write green data to overlay (location $1F)	10
Write blue data to overlay (location $1F)	10

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.20	1.235	1.26	Volts
FS ADJUST Resistor	RSET		523		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	Volts
Voltage on Any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
PGA	TJ			+150	°C
PQFP	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C
Air Flow					
PGA		0			l.f.p.m.
PQFP		50			l.f.p.m.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
IOUT Analog Output					
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4V)	IIH			1	µA
Input Low Current (Vin = 0.4V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	.6		6	Volts
Input High Current (Vin = 4.0V)	IKIH			1	µA
Input Low Current (Vin = 0.4V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0V)	CKIN		4	10	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
IOUT Analog Output	IOUT				
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
Output Compliance	VOC	−1.0		+1.2	Volts
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
PLL Analog Output	PLL				
Output Current					
SYNC*/BLANK* = 0		6.00	7.62	9.00	mA
SYNC*/BLANK* = 1		0	5	50	µA
Output Compliance		−1.0		+2.5	Volts
Output Impedance			50		kΩ
Output Capacitance (f = 1 MHz, PLL = 0 mA)			15		pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 KHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	170 MHz Devices			135 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Rate	Fmax			170			135	MHz
LD* Rate	LDmax			42.5			45	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	15			15			ns
CE* Low Time	3	60			60			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	7			7			ns
CE* Asserted to Data Valid	6			75			75	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	35			35			ns
Write Data Hold Time	9	0			0			ns
Pixel and Control Setup Time	10	3			3			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	5.88			7.4			ns
Clock Pulse Width High Time	13	2.6			3.2			ns
Clock Pulse Width Low Time	14	2.6			3.2			ns
LD* Cycle Time	15	23.5			22.2			ns
LD* Pulse Width High Time	16	8			8			ns
LD* Pulse Width Low Time	17	8			8			ns
Analog Output Delay	18							
Bt461			11			11		ns
Bt462			5			5		ns
Analog Output Rise/Fall Time	19		2			2		ns
Analog Output Settling Time	20			6			8	ns
Clock and Data Feedthrough*			tbd			tbd		dB
Glitch Impulse*			50			50		pV - sec
Pipeline Delay								
Bt461		6		10	6		10	Clocks
Bt462		8		12	8		12	Clocks
VAA Supply Current**	IAA							
Bt461			350	470		330	445	mA
Bt462			295	380		270	355	mA

See test conditions on next page.

AC Characteristics (continued)

		110 MHz Devices			80 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			110			80	MHz
LD* Rate	LDmax			36.7			26.7	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	15			15			ns
CE* Low Time	3	60			60			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	7			7			ns
CE* Asserted to Data Valid	6			75			100	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	35			50			ns
Write Data Hold Time	9	0			0			ns
Pixel and Control Setup Time	10	3			4			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	9.09			12.5			ns
Clock Pulse Width High Time	13	4			5			ns
Clock Pulse Width Low Time	14	4			5			ns
LD* Cycle Time	15	27.27			37.5			ns
LD* Pulse Width High Time	16	10			12			ns
LD* Pulse Width Low Time	17	10			12			ns
Analog Output Delay	18							
Bt461			11			11		ns
Bt462			5			5		ns
Analog Output Rise/Fall Time	19		2			3		ns
Analog Output Settling Time	20			8			12	ns
Clock and Data Feedthrough*			tbd			tbd		dB
Glitch Impulse*			50			50		pV - sec
Pipeline Delay								
Bt461		6		10	6		10	Clocks
Bt462		8		12	8		12	Clocks
VAA Supply Current**	IAA							
Bt461			320	430		300	410	mA
Bt462			255	340		235	320	mA

See test conditions on next page.

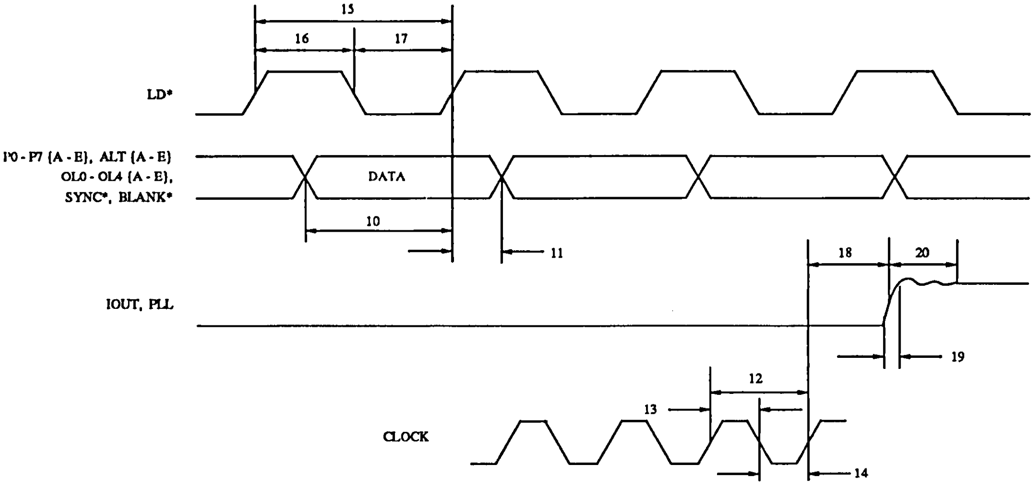
AC Characteristics (continued)

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are VAA–0.8 to VAA–1.8 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 75 pF. See timing notes in Figure 8. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V, TA = 20° C. IAA (max) at VAA = 5.25 V, TA = 0° C.

Timing Waveforms



Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full-scale transition.

Note 2: Output settling time measured from 50% point of full-scale transition to output settling within ±1 LSB.

Note 3: Output rise/fall time measured between 10% and 90% points of full-scale transition.

Figure 8. Video Input/Output Timing.

Timing Waveforms (continued)

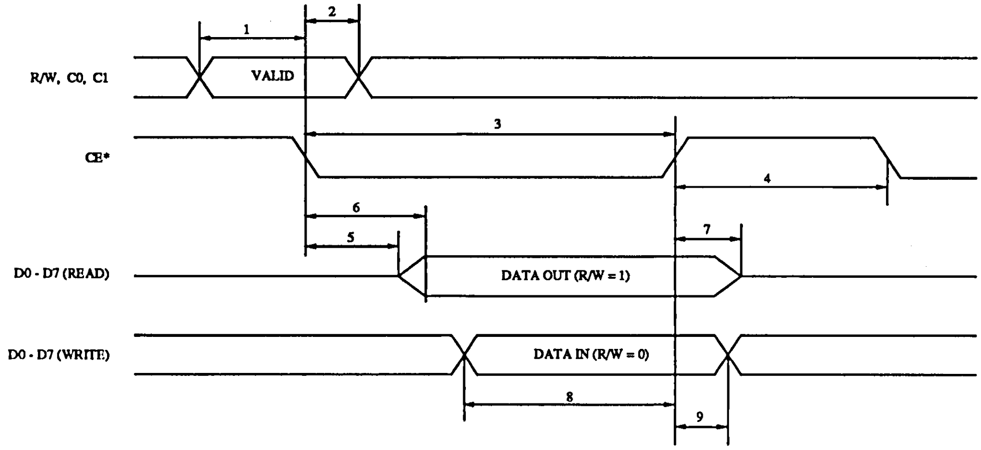

R/W, C0, C1
VALID
CE*
D0 - D7 (READ)
DATA OUT (R/W = 1)
D0 - D7 (WRITE)
DATA IN (R/W = 0)
1
2
3
4
5
6
7
8
9

Figure 9. MPU Read/Write Timing Dimensions.

Revision History

Datasheet Revision	*Change from Previous Revision*
F	Added Bt462 functionality, corrected Tables 1 and 2.
G	Added 132-pin PQFP package, expanded PCB layout section. Adjusted 170 MHz clock low and clock high times, power supply current on all speed grades, and AC parameters 3, 5, and 18.
H	Revised Application Information. Removed Input High and Low Voltage parameters and added Differential Input Voltage to DC Characteristics.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt461KG170	170 MHz	132-pin Ceramic PGA	0° to +70° C
Bt461KG135	135 MHz	132-pin Ceramic PGA	0° to +70° C
Bt461KG110	110 MHz	132-pin Ceramic PGA	0° to +70° C
Bt461KG80	80 MHz	132-pin Ceramic PGA	0° to +70° C
Bt462KG170	170 MHz	132-pin Ceramic PGA	0° to +70° C
Bt462KG135	135 MHz	132-pin Ceramic PGA	0° to +70° C
Bt462KG110	110 MHz	132-pin Ceramic PGA	0° to +70° C
Bt462KG80	80 MHz	132-pin Ceramic PGA	0° to +70° C
Bt462KPF170	170 MHz	132-pin Plastic Quad Flatpack	0° to +70° C
Bt462KPF135	135 MHz	132-pin Plastic Quad Flatpack	0° to +70° C
Bt462KPF110	110 MHz	132-pin Plastic Quad Flatpack	0° to +70° C
Bt462KPF80	80 MHz	132-pin Plastic Quad Flatpack	0° to +70° C

Bt463

170 MHz
Monolithic CMOS
TrueVu™ RAMDAC™

dvance Information

his document contains information on a product under development. The parametric and unctional information are target parameters and are subject to change without notice. lease consult Brooktree regarding the most updated datasheet before design.

Distinguishing Features

- 170, 135, 110 MHz Operation
- Multiple Display Modes on a Pixel Basis
- Multiple Color Maps
- Variable Palette Sizes
- Up to 8 Overlay Planes
- Reconfigurable Pixel Port
- 1:1, 2:1 or 4:1 Multiplexed Pixel Ports
- Three 528 x 8 Color Palette RAMs
- Programmable Setup (0 or 7.5 IRE)
- X Windows Support
- Input and Output Signature Registers
- JTAG Support
- 169-pin PGA Package

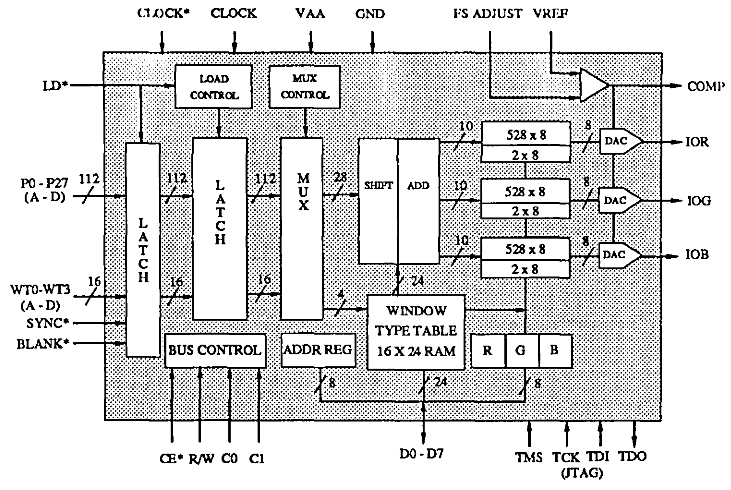
Applications

- High Resolution Color Graphics
- Medical Imaging
- Visualization
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt431, Bt438

Functional Block Diagram


CLOCK*
CLOCK
VAA
GND
FS ADJUST
VREF
LD*
LOAD CONTROL
MUX CONTROL
COMP
P0 - P27 (A - D)
112
LATCH
112
LATCH
112
MUX
28
SHIFT
ADD
10
528 x 8
2 x 8
8
DAC
IOR
10
528 x 8
2 x 8
8
DAC
IOG
10
528 x 8
2 x 8
8
DAC
IOB
WT0-WT3 (A - D)
16
16
16
4
24
SYNC*
BLANK*
WINDOW TYPE TABLE 16 X 24 RAM
BUS CONTROL
ADDR REG
R
G
B
8
24
8
CE*
R/W
C0
C1
D0 - D7
TMS
TCK
TDI
TDO
(JTAG)

Product Description

The Bt463 is a high performance RAMDAC designed specifically for true color and pseudo color graphics addressing multiple lookup tables for different windows. It has three 528 x 8 look-up tables with triple 8-bit D/A converters to support 24-bit true color and 9-bit pseudo color operation.

The TrueVu™ RAMDAC allows different display modes of operation for each pixel. Utilizing a proprietary window type scheme, each set of pixel and overlay data has four type bits which map the accompanying pixel data to a user-defined display mode. The type bits address a window type table which ultimately determines the description of the pixel data. With this scheme, arbitrary plane depth and unique visual display type can be achieved on a pixel basis. For example, separate windows displaying 24-plane true color, 8-plane pseudo color, and 12-plane double-buffer true color, each with a separate color map, can exist within a single frame. The size of each individual lookup table is user-configurable and can vary from 16 to 512 addresses.

On-chip features include programmable 1:1, 2:1, or 4:1 input multiplexing of the pixels, bit plane masking, and a programmable setup (0 or 7.5 IRE). The Bt463 has significant testability features, including input and output signature analysis registers, and fully supports the JTAG specification.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L463001 Rev. B

Brooktree®

Architecture

Introduction

With X Windows becoming the de facto standard, the need for each window to have its unique color map and display type becomes apparent. Each window should be able to use its own private color map and define its own interpretation of pixel values in the frame buffer using a variety of possible visual types. In addition, since each window is completely independent of other windows, the hardware must be able to accommodate multiple visual types within a single frame of graphics display. Thus, the ability to switch to different color maps and visual types on a pixel-by-pixel basis is essential. The Bt463 has been designed specifically to address multiple windows and display types. The Bt463 is extremely flexible, permitting multiple visual types to be displayed simultaneously and efficiently supporting multiple virtual color maps within the physical color map.

Overview

Window type data is sent to the TrueVu™ RAMDAC along with each pixel. The window type addresses a 16 x 24 window type table, which converts pixels from a virtual color map index to a physical color map index prior to sending them to the lookup table. In addition to specifying the physical color map location and display type, the window type table can determine the number of planes, location of the frame buffer data, location of overlay data, and select specific overlay planes for each window.

Even though the Bt463 has 24-plane true color capability, the assignment of red, green, and blue pins is not fixed to preassigned locations. The Bt463 is flexible, allowing pixel or overlay data to be in practically any location of the 28-bit pixel/overlay word and be shifted into position to address the lookup table. With this flexibility, the Bt463 can be configured in a variety of ways. A number of possible configurations are listed in Table 1.

Pixel Pin Location	Mapped Function	Display Mode
P0–P7 P8–P15 P16–P23 P24–P27	R0–R7 G0–G7 B0–B7 OL0–OL3	24-bit true color 4-plane overlay
P0–P8 P24–P27	P0–P8 OL0–OL3	9-bit pseudo color 4-plane overlay
P8–P15 P16–P19	P0–P7 OL0–OL3	8-bit pseudo color 4-plane overlay
P0–P7 P8–P15 P16–P23 P24–P27, WT0–WT3	R0–R7 G0–G7 B0–B7 OL0–OL7	24-bit true color 8-plane overlay
P4–P7 P12–P15 P20–P23 P24–P27	R0–R3 G0–G3 B0–B3 OL0–OL3	12-bit true color 4-plane overlay
P1–P7 P9–P15 P18–P23 P16, P8, P0, P17	R1–R7 G1–G7 B2–B7 OL0, OL1, OL2, OL3	24-bit true color 4-plane overlay

Table 1. Example Pixel/Overlay Configurations and Display Modes.

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt463 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers, window type table, and color palettes. The dual-port color palette RAMs allow color updating without contention with the display refresh process.

As illustrated in Table 2, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 12-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit. ADDR0 and ADDR8 correspond to data bus bit D0. ADDR12–ADDR15 are ignored during MPU write cycles and return a logical zero when read by the MPU.

The control registers and window type table are also accessed through the address register in conjunction with the C0 and C1 inputs, as shown in Table 2. All control registers may be written to or read by the MPU at any time. When accessing the control registers, window type table and the color palette RAM, the address register increments following a read or write cycle.

Writing/Reading Color Palette RAM

To write color data, the MPU loads the address register with the address of the color palette RAM or cursor color register to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select the color palette RAM or cursor color register. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data.

To read the color palette RAM or cursor color register, the MPU loads the address register with the address of the color palette RAM location or cursor color register to be read. Reading color data is similar to writing, except the MPU executes read cycles.

When accessing the cursor color registers, the address register increments to $0102 following a blue read or write cycle. The color palette RAM does not have a wraparound feature after the last valid address. However, any attempt to write past $020F does not affect previous data load cycles. The address register will reset to $0000 after incrementing past $0FFF.

Writing/Reading Window Type Table

To write the window type table, the MPU writes the address register with the table location to be modified. The MPU performs three successive write cycles (B0–B7, B8–B15, then B16–B23) with B0 being the least significant bit, using C0 and C1 to select the window type table. B0, B8, and B16 correspond to data bus bit D0. After the third write cycle, the three bytes of the table entry are concatenated into a 24-bit word and written to the window type table address specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of three bytes to the window type table. To avoid irregular window displays on the screen, MPU accesses to the window type table are restricted to horizontal and vertical retrace periods.

ADDR0 - 16	C1, C0	Addressed by MPU
$xxxx	00	address register (ADDR0–7)
$xxxx	01	address register (ADDR8–11)
$0100	10	cursor color 0*
$0101	10	cursor color 1*
$0200	10	ID register ($2A)
$0201	10	command register_0
$0202	10	command register_1
$0203	10	command register_2
$0205	10	P0–P7 read mask register
$0206	10	P8–P15 read mask register
$0207	10	P16–P23 read mask register
$0208	10	P24–P27 read mask register
$0209	10	P0–P7 blink mask register
$020A	10	P8–P15 blink mask register
$020B	10	P16–P23 blink mask register
$020C	10	P24–P27 blink mask register
$020D	10	test register
$020E	10	input signature register**
$020F	10	output signature register*
$0220	10	revision register ($A)
$0300–$030F	10	window type table*
$0000–$020F	11	color palette RAM*

*Indicates requires three read/write cycles
** Indicates 2 out of 3 valid read/write cycles

Table 2. Address Register (ADDR) Operation.

Circuit Description (continued)

To read the window type table data, the MPU loads the address register with the address of the type table to be read. Contents of the type table are copied into a 24-bit register and the address register is incremented to the next window type table entry. The MPU performs three successive read cycles (B0–B7, B8–B15, then B16–B23) with B0 being the least significant bit, using C0 and C1 to select the window type table. B0, B8, and B16 correspond to data bus bit D0.

Additional Information

When accessing the color palette RAM, window type table, signature analysis registers, or cursor color registers, the address register increments after every third read/write cycle for each addressable location. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 12 bits of the address register (ADDR0–11) are accessible to the MPU.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

For 8-bit registers, the address increments after every read/write cycle.

Figure 1 illustrates the MPU read/write timing of the Bt463.

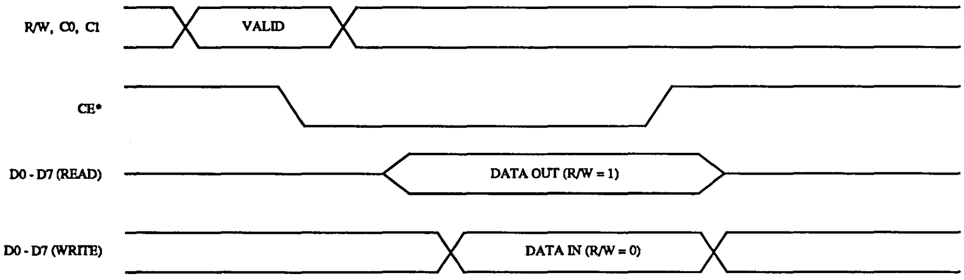


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt463 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, window type, and overlay information, for either one, two, or four consecutive pixels, are latched into the device. Note that with this configuration, the sync and blank timing will be recognized only with one, two, or four pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing and to clock the video DRAMs.

For 1:1, 2:1, or 4:1 input multiplexing, the Bt463 outputs color information each clock cycle based on the {A} inputs, followed by the {B} inputs, etc., until one, two, or four pixels have been output, at which point the cycle repeats.

To simplify the frame buffer interface timing, LD* may be phase-shifted, in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by two or four, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than three, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

If 1:1 multiplexing is specified, the CLOCK and CLOCK* signals are ignored and pixel data is latched on the rising edge of LD*. If 2:1 multiplexing is specified, only one rising edge of LD* should occur every two clock cycles. If 4:1 multiplexing is specified, only one rising edge of LD* should occur every four clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*.

Color Palette RAM

The color lookup table consists of three independent RAMs with variable size color maps. Multiple color maps can be assigned within each of the three 528 x 8 lookup tables with the minimum color map size being 16 colors. The color map can be as large as 512 colors.

Color generated by pixel or overlay data is independent of the absolute physical address of the lookup table. Pixel, overlay, and underlay data is referenced relative to its own color map. The start address indicating the beginning of each physical color map is added to the

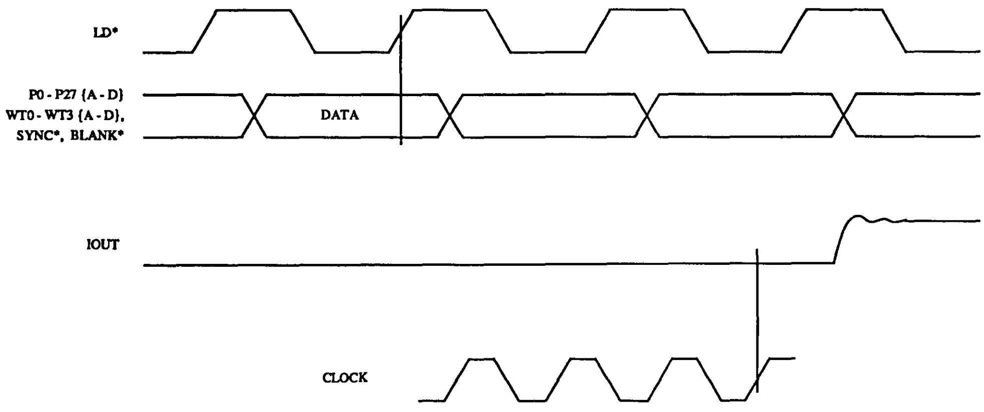


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

pixel data to generate the address for the final color. The start address is specified through the window type table.

Window Type Table

Window type data is sent to the RAMDAC along with each pixel. The window type addresses a 16 x 24 window type table selecting one of sixteen 24-bit window type words. The window type word reconfigures the mapping of the input pixels to the RAMDAC, pixel by pixel. Each color map requires a pointing index to convert pixels from a virtual color map index to a physical color map index. In addition to specifying the physical color map location and display type, the window type table can determine the number of planes, location of the frame buffer data, and location of overlay data, and can select specific overlay planes for each window.

Even though the Bt463 has 24-plane true color capability, the assignment of red, green, and blue pins is not fixed to preassigned locations. The Bt463 is flexible, providing capabilities to have pixel or overlay data in practically any location of the 28-bit pixel/overlay word. The pixels are shifted into position where they address the lookup table. With this flexibility, the Bt463 can be configured in a variety of ways, such as those listed in Table 1.

Associated with each set of pixel data is a 4-bit window type word (WT0–WT3). The window type addresses one of 16 possible entries of the window type table. Each 24-bit window type entry is associated with a particular configuration mode which specifies the number of planes, window display type, start address of the physical color map, shift constant, overlay location, and bypass operation. Multiple windows utilizing the same configuration mode can address the same entry of the window type table, as illustrated in Figure 3. It is recommended that the window type table be loaded by the MPU during vertical retrace to minimize disruptions during the display process.

The window type table provides the capability to switch back and forth between different display modes and individual color maps on a pixel-by-pixel basis. For example, the Bt463 can switch from 24-plane true color to 12-plane true color to 8-plane pseudo color, all within a single frame of graphic data. This allows users to personalize color maps specific to individual windows.

Users have the option of designating the 15th and 16th codes of the window type table to be used as a cursor. These two window type codes directly address the cursor palette, bypassing all pixel manipulation operations. This feature eliminates the need to use the overlay ports as an interface to a hardware cursor. Window type $E is defined as cursor color 0 and $F is cursor color 1.

The window type table words consist of 7 different fields which map the function of the accompanying pixel data. The 7 fields, shown in Figure 4 are: shift, number of planes, display mode, overlay location, overlay mask, start address and lookup table bypass. These fields are described in detail in the following sections.

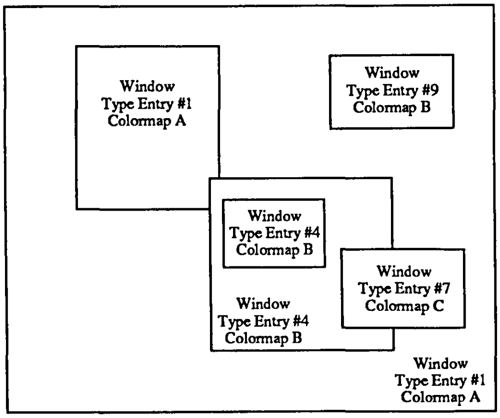


Figure 3. Multiple Windows Utilizing Different Color Maps.

Circuit Description (continued)

Window Type Table Fields

Shift <B4:B0>

This field specifies the plane position where active planes begin. If the active planes are in higher order bits, the shift field can shift these bits into the least significant position which will address the RAM. For instance, a value of 8 specifies active planes to begin at position P8. This field is particularly useful for double buffer applications. The shift value applies to the entire 28-bit pixel/overlay input. Legal values are 0 through 27. However, the number of planes plus the shift value should not exceed 28 within one window type table entry.

Number of Planes <B8:B5>

This field determines the number of active planes used for pixel data. Zeros will be inserted in bit planes above the specified MSB. For true color modes, the appropriate value in this field corresponds to the number of planes per channel. For instance, a 24-plane true color window should specify 8 as the number of planes. Legal values for this field are 0 through 8 for true color and 0 through 9 for pseudo color windows. Zero planes correspond to the color at the start address location regardless of pixel data, dependent on overlay and cursor data. This is useful for generating background color or flood color while the window is being changed or moved. The number of planes plus the shift value should not exceed 28 for the pseudo color mode. The number of planes times 3 plus the shift value shound not exceed 28 for the true color mode.

Display Mode <B11:B9>

This field determines the display mode of the pixel data. Valid display options are true color, pseudo color, bank select, 12-plane double buffer true color and pseudo color with load interleave. Refer to Table 3 for full display mode descriptions.

Overlay Location <B12>

The overlay location field specifies the source location of the overlay planes. A logic zero specifies overlay data to come from P<27:24>. The overlay location is fixed to these four pixel locations, unaffected by any shift in the shift fields. A logic one in this field specifies overlay data to come from the least significant bits of the pixel data (true color mode) or the four planes above the pixel planes (pseudo color mode). The overlay locations for the true color mode are P<17, 0, 8, 16>, with P16 being the LSB of the overlay word. The overlay location is affected by the shift value and only utilizes these variable locations after the shift operation has been completed.

Overlay Mask <B16:B13>

The overlay mask field is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette. B13 corresponds to OL0. B13–B16 are logically ANDed with the corresponding overlay plane input. The selected overlay planes are then compacted into the LSB positions with the higher significant bits filled with zeroes. This feature allows the user to assign specific overlay planes to individual windows. Two or more separate overlay images can be generated independently and switched on a pixel-by-pixel basis using the same or different overlay palette.

Start Address <B22:B17>

The start address specifies the beginning of the physical address of each individual color map. Pixel data addresses the lookup table independently of the absolute physical location of the color map. The start address constitutes the 6 MSBs of the start rows of the color maps. Color address is generated by adding the pixel data with the start address in the physical color map. The maximum valid physical address resulting from this addition is $020F. Color maps start on 16 row boundaries and are allocated in blocks of 16. Thus a binary value of 000001 corresponds to the physical address location of $0010. It is not necessary to fill the entire block with color map colors. The resultant value from pixel data plus the start address should not exceed the 528 address space of the lookup table. Various color maps can be disjoint, overlapping or subsets of other color maps. Minimum color map size is 16 while the maximum contiguous color map size is 512 colors. Legal values are 000000 through 100000.

Lookup Table Bypass <B23>

Up to 24 bits of pixel information are input via P0–P27 inputs. Even in the bypass mode, pixel manipulation still occurs with the 8 lowest significant bits used for each DAC. After shifting, pixels which are positioned in the LSB positions, P0–P7, are mapped as R0–R7, bypass the red color palette, and drive the red DAC directly. Similarly, P8–P15 pixels are mapped as G0–G7 and drive the green DAC directly. P16–P23 are mapped as B0–B7 and drive the blue DAC directly. The bypass mode can only be used in the 8-plane mode.

With the display mode set to pseudo color, the bypass bit will generate 256 shades of gray scale. Eight bits of color information are applied equally to each of the three DACs.

In the bypass mode, overlays are still effective in either the 4- or 8-plane mode and address the overlay palette.

Circuit Description (continued)

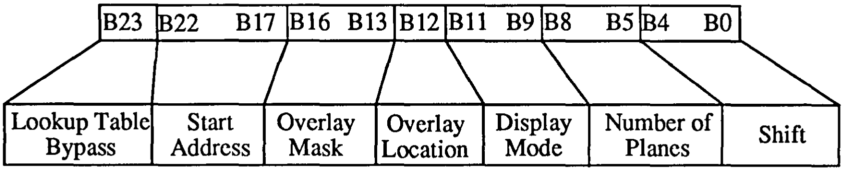
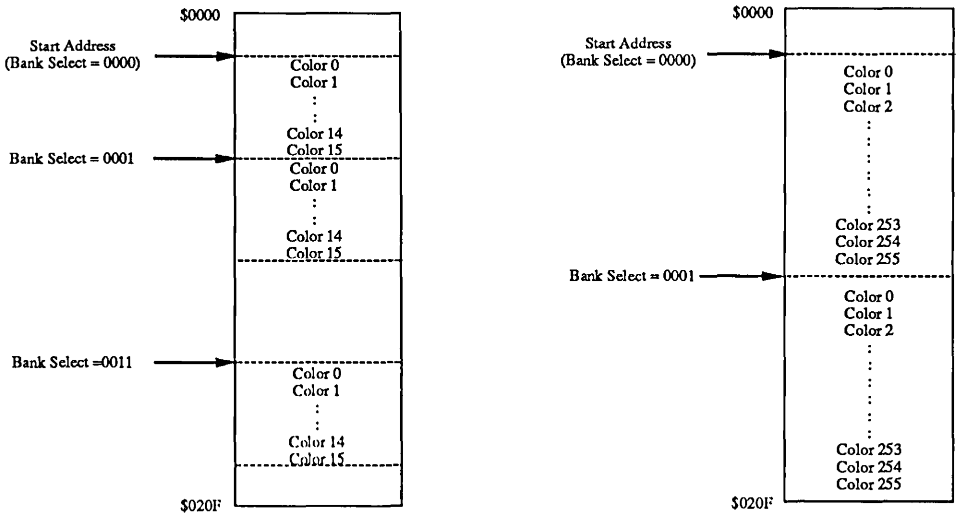


Figure 4. Window Type Table Fields.

Display Mode	Field	Description
True Color	000	An equal number of red, green, and blue pixel planes are input via the pixel port. The number of bits of true color is dependent on the "number of planes" field in the window type table. Eventually, pixel data must be shifted so that the least significant bit of the red pixel word is P0, green is P8, and blue is P16. Number of planes per channel is 0 to 8 for this mode. Correspondingly, the number of planes for the pixel data is three times the value in this field for true color. For example, a value of 8 in the plane field yields 24-plane true color. A value of 4 in the plane field yields a 12-plane true-color configuration.
Pseudo Color	001	All three color palette RAMs are addressed by the same planes of pixel data. Pixel data for the pseudo color must come from a contiguous set of planes. Maximum number of active planes is nine for the pseudo color mode. Number of available planes range from 0 to 9.
Bank Select	010	Overlay bits are concatenated as the MSBs to the pixel data to address a different portion of the lookup table without changing pixel data. Bank select is especially useful for highlighting or color contrasting by changing overlay inputs instead of regenerating the frame buffer image. Number of planes per channel is 0 to 8. Planes used for bank select are also dependent on the overlay mask. Refer to Figure 5 for more details on the bank select mode.
	011	Reserved
Twelve Plane True Color (Load Interleave) See Figure 6.	100	Twelve plane true color is generated by utilizing the lower or upper nibble (4 bits) from 8 bits each of red, green, and blue. Either the upper or lower nibbles are latched on each load clock across a scan line depending on the value of the shift field immediately after blank has been substantiated. The load cycle will begin with the lower nibble for a shift value of $00. If the shift value is $04 immediately after blank, the load cycle will begin with the upper nibble. The output sequence continues to alternate between lower nibble and upper nibble for each load sequence throughout the entire scan line. This display mode preassigns the mapped function for the pixel inputs. P0–P7 is red, P8–P15 is green, and P16–P23 is blue. Refer to Table 4 for more details.
Pseudo Color (Load Interleave) See Figure 6.	101	Eight plane pseudo color data is generated from either the lower nibble bits or upper nibble bits of red and green pixel data. The green nibble bits are concatenated with the red nibble bits to generate the 8 bit pseudo color pixel word. The red nibble comprise the least significant bits. Either the upper or lower nibbles are latched on each load clock across a scan line depending on the value of the shift field immediately after blank has been substantiated. The load cycle will begin with the lower nibble for a shift value of $00. If the shift value is $04 immediately after blank, the load cycle will begin with the upper nibble. The output sequence continues to alternate between lower nibble and upper nibble for each load sequence throughout the entire scan line. Refer to Table 5 for more details.
	110	Reserved
	111	Reserved

Table 3. Display Mode Options.

Circuit Description (continued)


$0000
Start Address
(Bank Select = 0000)
Color 0
Color 1
Color 14
Color 15
Bank Select = 0001
Color 0
Color 1
Color 14
Color 15
Bank Select =0011
Color 0
Color 1
Color 14
Color 15
$020F
$0000
Start Address
(Bank Select = 0000)
Color 0
Color 1
Color 2
Color 253
Color 254
Color 255
Bank Select = 0001
Color 0
Color 1
Color 2
Color 253
Color 254
Color 255
$020F

Number of Planes = 4

Number of Planes = 8

Figure 5. Color Map Allocation using Bank Select.

Pixel Location	Mapped Function	Pixel Word 12-bit True Color Lower Nibble	Lower Nibble Output Sequence	Pixel Word 12-bit True Color Upper Nibble	Upper Nibble Output Sequence
P0–P7 P8–P15 P16–P23	R0–R7 G0–G7 B0–B7	R0–R3 G0–G3 B0–B3	$A_LB_LC_LD_L$	R4–R7 G4–G7 B4–B7	$A_HB_HC_HD_H$

Table 4. 12-Bit True Color (Load Interleave) Mapping and Output Sequence.

Pixel Location	Mapped Function	Pixel Word 8-bit Pseudo Color Lower Nibble	Lower Nibble Output Sequence	Pixel Word 8-bit Pseudo Color Upper Nibble	Upper Nibble Output Sequence
P0–P7 P8–P15 P16–P23	R0–R7 G0–G7 B0–B7	G0–G3, R0–R3	$A_LB_LC_LD_L$	G4–G7, R4–R7	$A_HB_HC_HD_H$

Table 5. 8-Bit Pseudo Color (Load Interleave) Mapping and Output Sequence.

Circuit Description (continued)

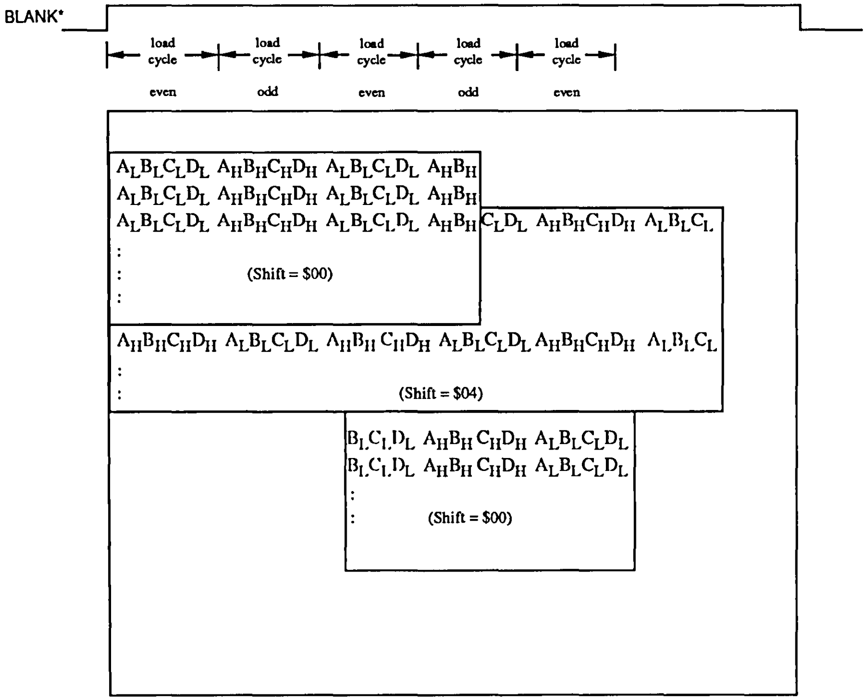

BLANK*
load cycle
even
load cycle
odd
load cycle
even
load cycle
odd
load cycle
even
$A_LB_LC_LD_L$ $A_HB_HC_HD_H$ $A_LB_LC_LD_L$ A_HB_H
$A_LB_LC_LD_L$ $A_HB_HC_HD_H$ $A_LB_LC_LD_L$ A_HB_H
$A_LB_LC_LD_L$ $A_HB_HC_HD_H$ $A_LB_LC_LD_L$ A_HB_H C_LD_L $A_HB_HC_HD_H$ $A_LB_LC_L$
(Shift = $00)
$A_HB_HC_HD_H$ $A_LB_LC_LD_L$ A_HB_H C_HD_H $A_LB_LC_LD_L$ $A_HB_HC_HD_H$ $A_LB_LC_L$
(Shift = $04)
$B_LC_LD_L$ A_HB_H C_HD_H $A_LB_LC_LD_L$
$B_LC_LD_L$ A_HB_H C_HD_H $A_LB_LC_LD_L$
(Shift = $00)

Figure 6. Load Interleave Output Sequence.

Video Generation

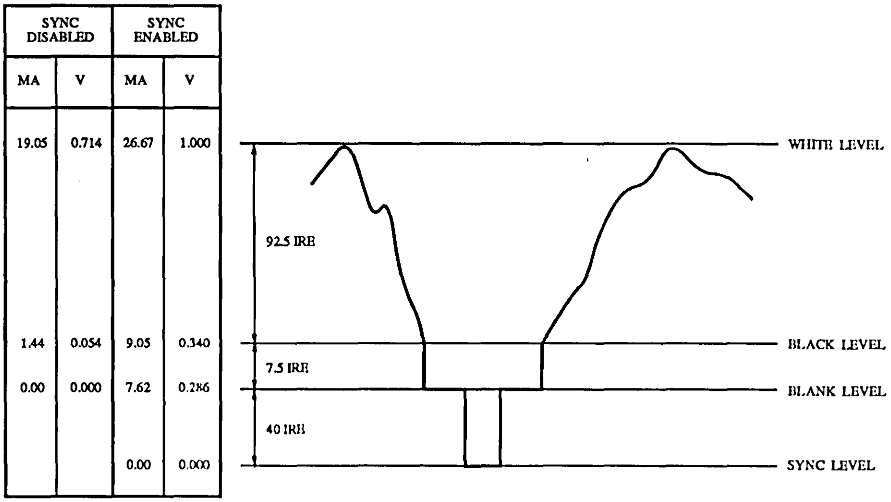
Every clock cycle, the color information (up to 24 bits) is presented to the three 8-bit D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 7 and 8. Command Register_2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated, and whether or not sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The varying output current from the D/A converters produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 6 and 7 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt463 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full scale output current against temperature and power supply variations.

Circuit Description (continued)


SYNC DISABLED
SYNC ENABLED
MA
V
MA
V
19.05
0.714
26.67
1.000
1.44
0.054
9.05
0.340
0.00
0.000
7.62
0.286
0.00
0.000
WHITE LEVEL
92.5 IRE
BLACK LEVEL
7.5 IRE
BLANK LEVEL
40 IRE
SYNC LEVEL

Note: 75 Ω doubly terminated load, RSET = 523 Ω, VREF = 1.235 V. Blank pedestal = 7.5 IRE. RS-343A levels and tolerances are assumed on all levels.

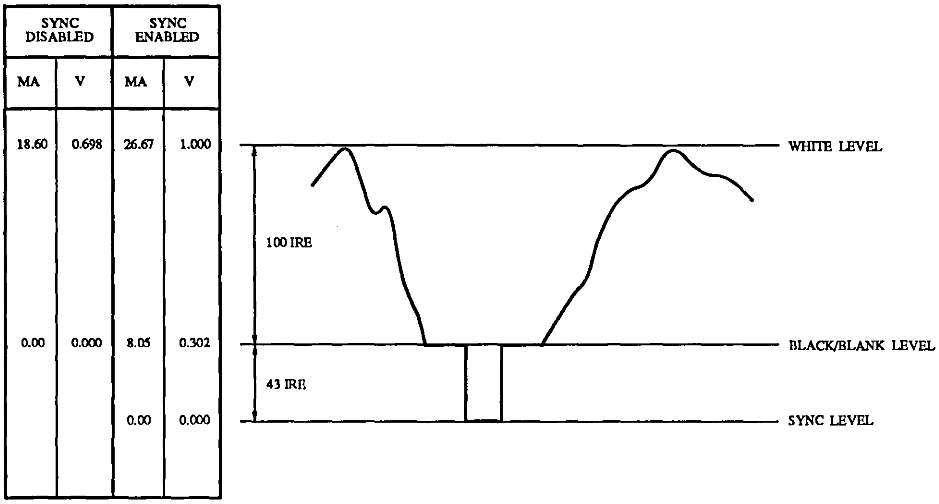
Figure 7. Composite Video Output Waveform (SETUP = 7.5 IRE).

Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	$FF
DATA	data + 9.05	data + 1.44	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	9.05	1.44	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	7.62	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 523 Ω, VREF = 1.235 V. Blank pedestal = 7.5 IRE.

Table 6. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)



Note: 75 Ω doubly terminated load, RSET = 495 Ω, VREF = 1.235 V. Blank pedestal = 0 IRE. RS-343A levels and tolerances are assumed on all levels.

Figure 8. Composite Video Output Waveform (SETUP = 0 IRE).

Description	Sync Iout (mA)	No Sync Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	18.60	1	1	$FF
DATA	data + 8.05	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	8.05	0	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	8.05	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with RSET = 495 Ω, VREF = 1.235 V. Blank pedestal = 0 IRE.

Table 7. Video Output Truth Table (SETUP = 0 IRE).

Circuit Description (continued)

Overlay and Underlay Operation

The Bt463 has capabilities for multiple plane overlay and underlay operation. Instead of a dedicated overlay color palette, the overlay palette may be indexed to each of the independent color maps as specified by the user. Overlay color is determined by subtracting $10 from the start address referenced in the window type table and adding the overlay value.

Overlay data can originate from a number of sources. The source location of the overlays is determined by the window type word and command register. All display modes have the capability of utilizing pixel ports 24 to 27 for the overlay address. In addition, for pseudo color applications, the overlay information can originate from the four planes above the pixel planes. For instance, if pixel information is being addressed from P0 to P7, then overlay planes may come from P8 through P11, with P8 being the LSB of the overlay word.

For true color applications, overlay information can also be addressed from the least significant bits of the red, green, and blue pixel data. Two LSBs are used from the blue pixel port. The overlay word <OL3:OL0> consists of P17, P0, P8, and P16 (after shift operation), with P16 being the LSB of the overlay word. The overlay enable mask bits designate whether some or all of the LSB pixel data is to be used as overlay planes.

Instead of multiple overlay palettes, the user can choose a fixed overlay location for all window type entries. The location of the common overlay palette is fixed, independent of the start address of the window type table. The common overlay palette is located at addresses $0201 to $020F.

Underlay operations with various planes can be achieved by changing command register bit CR12 to underlay operation. Once this bit is set for underlay operation, OL3 determines whether the remaining overlay planes should be interpreted as overlay or underlay. If underlays are unavailable as specified in the command register, then the overlay ports are restricted to cursor and overlay operation only. To obtain overlay and underlay operation, the overlay mask must be set to $F. All other values of the overlay mask would result in a compacted overlay word, yielding only underlay operation.

In the standard mode, the Bt463 utilizes 4 overlay/underlay planes providing a palette of 16 colors. However, the Bt463 has a special mode where the window type bits serve as the upper nibble to the overlay port. By setting a command register bit, 8 overlay planes become available. However, no window operation is available as these window type ports are used strictly for overlay ports. Hardware cursor is still available through OL0 and OL1. Both true color and pseudo color operation are available in the 8 overlay plane mode. The physical location of the overlay palette is fixed to a preassigned location.

If a color map start address is specified to be $0000, then overlay colors are located at physical address $0201 to $020F. For other start addresses, refer to Figure 9 for a diagram showing the overlay and pixel palette color map scheme. Tables 8 and 9 provide details of overlay operation for different modes of operation.

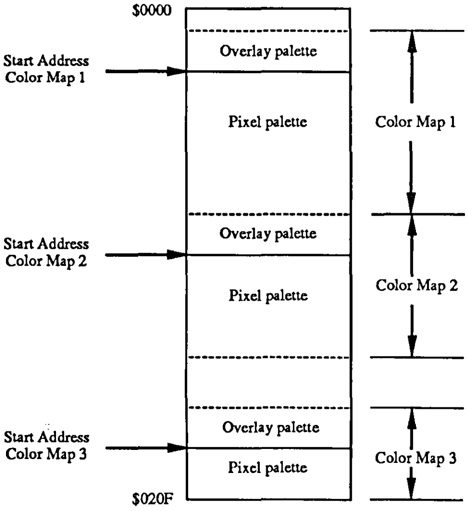


Figure 9. Overlay and Pixel Palette Color Map Scheme.

Circuit Description (continued)

Display Mode	Window Type Field <B11:B9>	Overlay Location <B12>	Overlay Location <OL3:OL0>
True Color	000 000	0 1	P <27:24> P <17, 0, 8, 16>
Pseudo Color	001 001	0 1	P <27:24> P <planes+3:planes>
Bank Select	010 010	0 1	P <27:24> P <17, 0, 8, 16>
12 Plane True Color (Load Interleave)	100 100	0 1	P <27:24> P <17, 0, 8, 16>
Pseudo Color (Load Interleave)	101 101	0 1	P <27:24> not available

Table 8. Overlay Location Truth Table.

Underlay Enable (CR12)	Mapped Function <OL3 : OL0>	Pixel Port <P9:P0>	Physical Ram location Addressed by frame buffer	Operating Mode
x	0000	$000	Start Address + $000	pixel data
x	0000	$001	Start Address + $001	
:	:	:	:	
x	0000	$1FF	Start Address + $1FF	
0	1111	$xxx	Start Address–$10+ $F	overlay only
:	:	:	:	
0	0010	$xxx	Start Address–$10 + $2	
0	0001	$xxx	Start Address–$10 + $1	
1	1111	$xxx	Start Address–$10 + $F	overlay
1	1110	$xxx	Start Address–$10 + $E	
1	1101	$xxx	Start Address–$10 + $D	
1	1100	$xxx	Start Address–$10 + $C	
1	1011	$xxx	Start Address–$10 + $B	
1	1010	$xxx	Start Address–$10 + $A	
1	1001	$xxx	Start Address–$10 + $9	
1	1000	$xxx	Start Address–$10 + $8	
1	0111	$000	Start Address– $10 + $7	underlay
1	0110	$000	Start Address–$10 + $6	
1	0101	$000	Start Address–$10 + $5	
1	0100	$000	Start Address–$10 + $4	
1	0011	$000	Start Address–$10 + $3	
1	0010	$000	Start Address–$10 + $2	
1	0001	$000	Start Address–$10 + $1	

Table 9. Palette and Overlay Select Truth Table
(No Hardware Cursor Interfacing the Overlay Port) CR<11:10> = 00, B<16:13> = $F.

Circuit Description (continued)

Hardware Cursor Interface

The Bt463 has numerous configurations for interfacing with a hardware cursor. Utilizing two entry codes of the window type table for a two-color cursor provides the best method of maximizing overlay plane availability without sacrificing a large number of window type entries.

Otherwise, the overlay ports can be used directly as cursor ports but require setting command register bits CR10 and CR11 to configure the RAMDAC for either a single plane cursor or dual-plane cursor through the overlay port. Adding cursor planes through the overlay port reduces the available colors for overlays and underlays.

One Plane Cursor (Overlay Port)

In the one-cursor plane mode, OL0 directly addresses the cursor color palette and overrides all other inputs. By setting a command register, mapped function OL3 determines whether OL1 and OL2 serve as overlay or underlays. Only seven combinations of overlays/ underlays are available. Refer to Table 10 for more details.

Underlay Enable (CR12)	Mapped Function <OL3 : OL0>	Pixel Port <P9:P0>	Physical Ram Location Addressed by Frame Buffer	Operating Mode
x	0000	$000	Start Address + $000	pixel data
x	0000	$001	Start Address + $001	
:	:	:	:	
x	0000	$1FF	Start Address + $1FF	
x	xxx1	$xxx	Cursor Color 0	cursor
0	1110	$xxx	Start Address–$10 + $E	overlay only
0	1100	$xxx	Start Address–$10 + $C	
0	1010	$xxx	Start Address–$10 + $A	
0	1000	$xxx	Start Address–$10 + $8	
0	0110	$xxx	Start Address–$10 + $6	
0	0100	$xxx	Start Address–$10 + $4	
0	0010	$xxx	Start Address–$10 + $2	
x	xxx1	$xxx	Cursor Color 0	cursor
1	1110	$xxx	Start Address–$10 + $E	overlay
1	1100	$xxx	Start Address–$10 + $C	
1	1010	$xxx	Start Address–$10 + $A	
1	1000	$xxx	Start Address–$10 + $8	
1	0110	$000	Start Address–$10 + $6	underlay
1	0100	$000	Start Address–$10 + $4	
1	0010	$000	Start Address–$10 + $2	

Table 10. Palette and Overlay Select Truth Table
(One Plane Hardware Cursor Interfacing the Overlay Port) CR<11:10> = 01, B<16:13> = $F.

Circuit Description (continued)

Two Plane Cursor (Overlay Port)

In the two-cursor plane mode, both mapped functions OL0 and OL1 become cursor planes with OL0 being the least significant bit. With the underlay enabled, OL3 determines whether OL2 serves as an overlay or an underlay. Refer to Table 11 for more details.

Underlay Enable (CR12)	Mapped Function <OL3 : OL0>	Pixel Port <P9:P0>	Physical Ram location Addressed by frame buffer	Operating Mode
x	0000	$000	Start Address + $000	pixel data
x	0000	$001	Start Address + $001	
:	:	:	:	
x	0000	$1FF	Start Address + $1FF	
x	xx01	$xxx	Cursor Color 0	cursor
x	xx1x	$xxx	Cursor Color 1	
0	1100	$xxx	Start Address–$10 + $C	overlay only
0	1000	$xxx	Start Address–$10 + $8	
0	0100	$xxx	Start Address–$10 + $4	
x	xx01	$xxx	Cursor Color 0	cursor
x	xx1x	$xxx	Cursor Color 1	
1	1100	$xxx	Start Address–$10 + $C	overlay
1	1000	$xxx	Start Address–$10 + $8	
1	0100	$000	Start Address–$10 + $4	underlay

Table 11. Palette and Overlay Select Truth Table
(Two Plane Hardware Cursor Interfacing the Overlay Port) CR<11:10> = 10, B<16:13> = $F.

Circuit Description (continued)

Boundary Scan Testability Structures

As the complexity of RAMDACs increases, the need to easily access the RAMDAC for functional verification is becoming vital. The Bt463 has incorporated special circuitry that allows it to be accessed in full compliance with standards set by the Joint Test Action Group (JTAG). Conforming to the IEEE P1149.1 "Standard Test Access Port and Boundary Scan Architecture," Bt463 has dedicated pins which are used for testability purposes only.

JTAG's approach to testability utilizes boundary scan cells placed at each digital pin, both inputs and outputs. All scan cells are interconnected into a boundary-scan register (BSR) which applies or captures test data used for functional verification of the RAMDAC. JTAG is particularly useful for board testers using functional testing methods.

JTAG consists of four dedicated pins comprising the Test Access Port (TAP). These pins are TMS (Test Mode Select), TCK (Test Clock), TDI (Test Data Input), and TDO (Test Data Out). Complete verification of the RAMDAC can be achieved through these four TAP pins. With boundary-scan cells at each digital pin, the Bt463 has the capability to apply and capture the logic level. Since all of the digital pins are interconnected as a long shift register, the TAP logic has access and control of all the necessary pins to verify functionality. The TAP controller can shift in any number of test vectors through the TDI input and apply them to the internal circuitry. The output result is scanned out on the TDO pin and externally checked. While isolating the Bt463 from the other components on the board, the user has easy access to all Bt463 digital pins through the TAP and can perform complete functionality tests without using expensive bed-of-nails testers.

The bidirectional MPU port is given special attention with respect to JTAG. Because JTAG requires control over each digital pin, an additional output enable (OE) function is included in the BSR for the MPU pins. In conjunction with the JTAG instruction, the output enable will configure the MPU port as an input or output.

With the JTAG bus, users also have access to a vital portion of the Bt463, the Output Signature Analysis Register (See Figure 10). With access to this register, users can easily verify expected video data serially through the JTAG port. The OSAR is located between the lookup table and the inputs to the DACs.

The power-on reset (POR) circuitry ensures that the Bt463 initializes each pin to operate in a RAMDAC mode instead of a JTAG test mode during power-up sequence.

A variety of verification procedures can be performed through the TAP Controller. Through a set of eight instructions, the Bt463 can verify board connectivity at all digital pins, generate artificial pixel vectors on-chip, check signatures on system pixel streams, and scan vectors in and out of the pixel shifter and signature analysis register. The instructions are accessible through the use of a simple state machine. For full explanation and details of the Bt463 JTAG instruction set, please consult the Application Note Bt463 JTAG Implementation, available in 1991.

Circuit Description (continued)

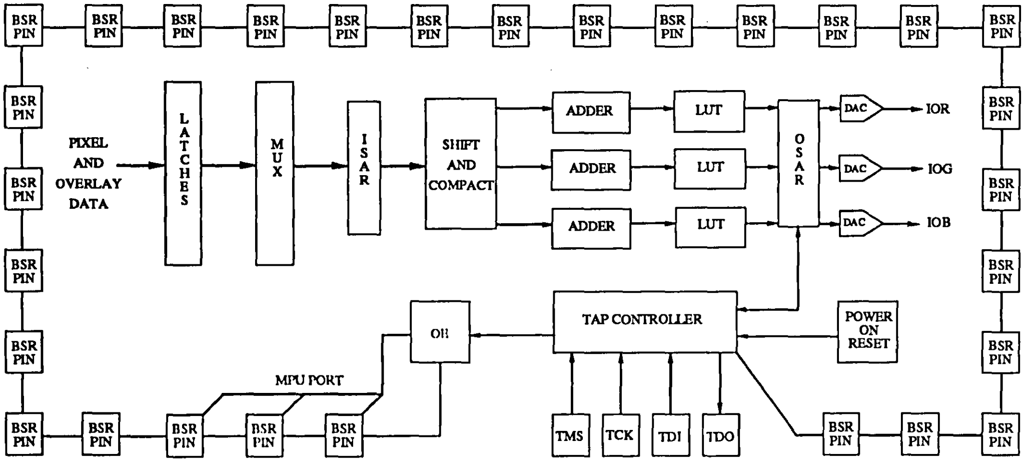

BSR PIN
PIXEL AND OVERLAY DATA
LATCHES
MUX
ISAR
SHIFT AND COMPACT
ADDER
LUT
OSAR
DAC
IOR
IOG
IOB
TAP CONTROLLER
POWER ON RESET
OR
MPU PORT
TMS
TCK
TDI
TDO

Figure 10. JTAG Block Diagram.

Internal Registers

Command Register_0

This register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to data bus bit D0.

CR07, CR06	Multiplex select (00) reserved (01) 4:1 multiplexing (10) 1:1 multiplexing (11) 2:1 multiplexing	These bits specify whether 1:1, 2:1, or 4:1 multiplexing is to be used for the pixel and overlay inputs. If 2:1 is specified, the {C} and {D} pixel and overlay inputs are ignored and should be connected to GND, and the LD* input should be 1/2 the CLOCK rate. If 4:1 is specified, all of the pixel and overlay inputs are used, and the LD* input should be 1/4 the CLOCK rate. If 1:1 is specified, the {B}, {C}, and {D} inputs are ignored. Note that in the 1:1 multiplex mode, the maximum clock rate is 66 MHz. LD* is used for the pixel clock. Although CLOCK is ignored in the 1:1 mode, it must remain running. Note that it is possible to reset the pipeline delay of the Bt463 to a fixed 13 clock cycles. In this instance, each time the input multiplexing is changed, the Bt463 must again be reset to a fixed pipeline delay.
CR05, CR04	reserved (logical zero)	
CR03, CR02	Blink rate selection (00) 16 on, 48 off (25/75) (01) 16 on, 16 off (50/50) (10) 32 on, 32 off (50/50) (11) 64 on, 64 off (50/50)	These two bits specify the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (% on/off). The counters that determine the blink rate are reset when command register_0 is written to.
CR01, CR00	reserved (logical zero)	

Internal Registers (continued)

Command Register_1

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0.

CR17	reserved (logical zero)	
CR16	Overlay mapping (0) Mapped to start address (1) Mapped to common palette	Determines the physical address location of the overlay. In the standard mode, overlays are addressed with respect to the start address specified in the start address field of the window type table. The alternate mapping option addresses the same portion of the color map for overlays regardless of the start address location. For this mode, the overlays must be located at physical address locations $0201 - $020F.
CR15	Contiguous Plane Configuration (0) 24/28 planes contiguous (1) 12/16 planes contiguous	Allows the Bt463 to be used with 12- or 16-plane systems with an easy field upgrade to 24/28 planes. In the 12/16 plane configuration, up to 12 planes of true color are available. Red must be entered at P<3:0>, blue at P<4:7>, and green at P<11:8>. No shift is of use with 12-plane true color and the shift value in the window type word should be set to zero. The standard pseudo color mode is available, up to nine planes. In this mode, the shift value should be between 0 and either 11 (12-plane systems) or 15 (16 plane systems). In 16-plane systems, the 4 planes of overlay should be entered at P<15:12>. If the alternate location overlay is selected, then overlays are input at P<5,0,8,4> for the true color mode or at P<P+3:P> for the pseudo color mode. Unused pixel pins must be grounded.
CR14	Overlay planes select (0) 4 overlay planes (1) 8 overlay planes	Special mode which configures the Bt463 for 8 overlay planes. This mode can be used for either the standard true color or pseudo color display modes. For true color applications, the red pixel port corresponds to P0–P7, green corresponds P8–P15, and blue corresponds to P16–P23. The four least significant overlay bits, OL0–OL3 are assigned pixel port P24–P27. The window type port is converted into the four most significant bits of the overlay port where WT0–WT3 correspond to OL4–OL7, respectively. All 16 window type entries must be loaded and must be set to the same value. The recommended configuration is true color, no shift, 8 planes, all overlay inputs enabled, and the standard overlay location. Although different window display modes are no longer available, pixel operation is still user-defined based on the window type word placed in all 16 type entries. The only field with a restriction is the start address, which should have a value of 010000 ($0100). Thus, the physical location of the pixel lookup table and the overlay palette are preassigned, with the pixel color palette starting from $0100 and ending at $01FF while the overlay palette RAM is located at $0000 to $00FF.

Internal Registers (continued)

Command Register_1 (continued)

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0.

CR13	Window type entries (0) 16 entries (1) 14 entries	Determines the number of entries available in the window type table. If 14 entries are selected, then the two window type codes, $E and $F, correspond to cursor color 0 and cursor color 1 respectively.
CR12	Underlay enable (0) underlays disabled (1) underlays enabled	Determines the underlay availability. Once this bit is set to a logic one, underlays operation is achieved when the OL3 plane is a logic zero.
CR11–CR10	Overlay configuration (00) no cursor (01) one cursor plane (10) two cursor planes (11) reserved	Configures the overlay port so that overlay pins may be used as a hardware cursor port. By configuring this register, these overlay ports will directly address the cursor palette. If the overlay ports are used for cursors, they must be used on OL0 and OL1. OL0 is the least significant cursor bit. OL0 must be used for the single cursor mode. This overlay configuration register applies to the standard 4-plane mode or the eight-plane overlay option.

Internal Registers (continued)

Command Register_2

This register may be written to or read by the MPU at any time and is not initialized. CR20 corresponds to data bus bit D0.

CR27	Sync enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto IOG (logical one) or not (logical zero).
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. 0 IRE specifies that the black and blank levels are the same.
CR25–CR23	reserved (logical zero)	
CR22	Input SAR capture selection (0) lower 16 bits (1) upper 16 bits	This bit specifies whether the 16-bit input signature analysis register (SAR) should capture the lower or upper 16 bits of the pixel path.
CR21	Analysis register clock control (0) every LD* cycle (1) every CLOCK cycle	This bit controls the rate of operation of all signature analysis register (SAR) clocking. Logical zero is the normal mode, with pixel position (A, B, C, or D) determined by the test register. Logical one is a special mode for chip testing (in this instance, SAR operation is not guaranteed for clock rates above 30 MHz).
CR20	Test mode select (0) signature analysis test (1) data strobe test	This bit determines the method of high-speed test used. The signature analysis registers are used to hold the test result for both test methods.

Internal Registers (continued)

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt463, the value read by the MPU will be $2A. Data written to this register is ignored.

Pixel Read Mask Register

The 28-bit pixel read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. The masking function is independent of all the operations specified by the window type entries, masking the pixel ports prior to pixel manipulation. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P0, P8, P16, and P24.

Pixel Blink Mask Register

The 28-bit pixel blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0. The blinking function is independent of all the operations specified by the window type entries, blinking the pixel ports prior to pixel manipulation. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P0, P8, P16, and P24.

Revision Register

This 8-bit register is a read-only register, specifying the revision of the Bt463. The four most significant bits signify the revision letter in hexadecimal form. The four least significant bits do not represent any value and should be ignored.

Internal Registers (continued)

Red, Green, and Blue Output Signature Registers (OSAR)

Signature Operation

These three 8-bit signature registers may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may write to the output signature registers while BLANK* is a logical zero to load the seed value. The output signature registers use data being loaded into the output DACs to calculate the signatures. JTAG logic can access the output signature analysis register independently of the MPU operation. MPU accesses to the output signature analysis registers require one address register load to address $020F followed by 3 reads or writes to the red, green, and blue signature registers, respectively. D0 corresponds to R0, G0, and B0.

When a test display is loaded into the frame buffer, a given value for the red, green, and blue signature registers will be returned if all circuitry is working properly.

Data Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the signature registers changes slightly. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

Each LD* cycle, the three signature registers capture the color values being presented to the DACs. As only one of the (A–D) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–D) is to be captured.

Input Signature Registers (ISAR)

Signature Operation

This 16-bit signature register may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may write to the input signature register while BLANK* is a logical zero to load the seed value. The input signature register uses P0–P15 or P16–P27 and WT0–WT3 (selected by command bit CR22) to calculate the signatures. The 16 bits of data latched in the input signature register may be masked (forced low) by the read mask registers. MPU accesses to the input signature analysis register require one Address register load to $020E followed by 3 reads or writes to, respectively, lower byte, upper byte, and dummy access. D0 corresponds to P0 and P8 or to P16 and P24.

When a test display is loaded into the frame buffer, a given value for the input signature register will be returned if all circuitry is working properly.

Data Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the input signature register changes slightly. Rather than determining the signature, it just captures and holds the 16 bits of pixel data addressing the color palette RAM.

Each LD* cycle, the input signature register captures the 16 bits of pixel data addressing the color palette RAM. As only one of the (A–D) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–D) is to be captured.

Internal Registers (continued)

Test Register

This 8-bit register is used for testing the Bt463. If 1:1 pixel multiplexing is specified, signature analysis is done on every pixel; if 2:1 pixel multiplexing is specified, signature analysis is done on every second pixel; if 4:1 pixel multiplexing is specified, signature analysis is done on every fourth pixel. D0–D2 are used for 2:1 and 4:1 multiplexing to specify whether to use the A, B, C, or D pixel inputs, as follows:

D2 - D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	reserved
101	reserved
110	reserved
111	reserved

In 1:1 multiplexing mode, D0–D2 should select pixel A.

D3–D7 are used to compare the analog RGB outputs to each other and to a 145 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs or not, and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	145 mV ref. select	result

D7–D4		If D3 = 1	If D3 = 0
0000	normal operation	-	-
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 145 mV reference	red > 145 mV	red < 145 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 145 mV reference	green > 145 mV	green < 145 mV

The table above lists the valid comparison combinations. A logical one enables that function to be compared; the result is D3. The output levels of the DACs should be constant for 5 µs to allow enough time for detection. The capture occurs over one LD* period set by a logic one at any of the pixel pins P16A, P16B, P16C, or P16D.

For normal operation, D4–D7 must be a logical zero.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL-compatible). A logical zero drives the analog output to the blanking level, as illustrated in Tables 6 and 7. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control inputs (TTL-compatible). A logical zero typically switches off a 40 IRE current source on the IOG output (see Figures 9 and 10). SYNC* does not override any other control or data input, as shown in Tables 6 and 7; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL-compatible). The P0–P27 {A–D}, WT0–WT3 {A–D}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD*, while it is the output clock (1:1 multiplex mode) or is 1/2 or 1/4 of CLOCK, may be phase-independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle, within the limits specified by the A.C. Characteristics section.
P0–P27 {A–D}	Pixel select inputs (TTL-compatible). These inputs are used to specify, on a pixel basis, which location of the color palette RAM is to be used to provide color information. The function of each of these pixel ports is configurable depending on the entry of the window type table. In fact, overlay data may exist from various locations of this pixel port. If data exists in the assigned overlay input port, then pixel data inputs are ignored. Overlay information (up to four bits per pixel) for either one, two, or four consecutive pixels are input through this port. Either one, two, or four consecutive pixels (up to 24 bits per pixel) are input through this port. All 4 pixels (112 bits) are latched on the rising edge of LD*. Unused inputs should be connected to GND. Note that typically the {A} pixel is output first, followed by the {B} pixel, etc., until all one, two, or four pixels have been output, at which point the cycle repeats.
WT0–WT3 {A–D}	Window type inputs (TTL-compatible). These inputs are latched on the rising edge of LD*. The window type references a location within the window type table which configures the corresponding pixel data or overlay data into user-defined display modes. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 13). All outputs, whether used or not, should have the same output load.
TCK	Test Clock (TTL-compatible). Used to synchronize all JTAG test structures. Maximum clock rate for this pin is 50 MHz. When not performing JTAG operations, this pin should be driven to a logic high.
TMS	Test Mode Select (TTL-compatible). JTAG input pin whose transitions drive the JTAG state machine through its sequences. When not performing JTAG operations, this pin should be driven to a logic high.
TDI	Test Data Input (TTL-compatible). JTAG input pin used for loading instructions to the TAP controller or for loading test vector data for boundary scan operation. When not performing JTAG operations, this pin should be driven to a logic high.
TDO	Test Data Output (TTL-compatible). JTAG output used for verifying test results of all JTAG sampling operations. This output pin is active for certain JTAG sequences, and will be 3-stated at all other times. When not performing JTAG operations, this pin should be left floating.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 11). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. Refer to *PC Board Layout Considerations* for critical layout criteria.
FS ADJUST	Full scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal (Figure 11). Note that the IRE relationships in Figures 9 and 10 are maintained, regardless of the full scale output current.

The relationship between RSET and the full scale output current on IOG is:

RSET (ohms) = K1 * VREF (V) / IOG (mA)

The full scale output current on IOR and IOB for a given RSET is:

IOR, IOB (mA) = K2 * VREF (V) / RSET (ohms)

where K1 and K2 are defined as:

Setup	IOG	IOR, IOB
7.5 IRE	K1 = 11,294	K2 = 8,067
0 IRE	K1 = 10,684	K2 = 7,457

Pin Name	Description
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 11, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 11. If VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL-compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. Care should be taken to avoid glitches on this edge-triggered input.
R/W	Read/write control input (TTL-compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*.
C0, C1	Command control inputs (TTL-compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL-compatible). Data is transferred into and out of the device over this eight-bit bidirectional data bus. D0 is the least significant bit.

Pin Descriptions (continued)—169-pin PGA Package

Signal	Pin Number
BLANK*	J1
SYNC*	H1
LD*	H3
CLOCK*	J3
CLOCK	J2
P0A	F2
P0B	G3
P0C	F1
P0D	G1
P1A	F3
P1B	D1
P1C	E2
P1D	E1
P2A	C2
P2B	B1
P2C	D2
P2D	C1
P3A	C3
P3B	D3
P3C	E3
P3D	B2
P4A	A1
P4B	B3
P4C	C4
P4D	D4
P5A	A3
P5B	C5
P5C	A2
P5D	B4
P6A	A5
P6B	B6
P6C	A4
P6D	B5
P7A	A7
P7B	C7
P7C	A6
P7D	C6
P8A	A9
P8B	B8
P8C	A8
P8D	B7
P9A	A10
P9B	B10
P9C	B9
P9D	C10
P10A	A12
P10B	C11
P10C	A11
P10D	B11
P11A	A14
P11B	B12
P11C	A13
P11D	C12
P12A	A16
P12B	C13
P12C	A15
P12D	B13
P13A	C14
P13B	B15
P13C	A17
P13D	B14
P14A	D15
P14B	B16
P14C	E15
P14D	C15
P15A	D16
P15B	C17
P15C	C16
P15D	B17
P16A	T16
P16B	T17
P16C	R16
P16D	R17
P17A	R15
P17B	R14
P17C	P15
P17D	U17
P18A	T14
P18B	U15
P18C	T15
P18D	U16
P19A	T13
P19B	U13
P19C	R13
P19D	U14
P20A	R12
P20B	U11
P20C	T12
P20D	U12
P21A	T11
P21B	U9
P21C	R11
P21D	U10
P22A	R10
P22B	U8
P22C	T10
P22D	T9
P23A	T7
P23B	U6
P23C	T8
P23D	U7
P24A	R6
P24B	U4
P24C	R7
P24D	U5
P25A	T5
P25B	U2
P25C	T6
P25D	U3
P26A	T4
P26B	R4
P26C	R5
P26D	U1
P27A	R3
P27B	N3
P27C	T3
P27D	T1
TMS	D17
TCK	E16
TDI	E17
TDO	F17

Pin Descriptions (continued)—169-pin PGA Package

Signal	Pin Number
WT0A	P1
WT0B	P3
WT0C	R1
WT0D	T2
WT1A	M1
WT1B	P2
WT1C	N1
WT1D	R2
WT2A	L1
WT2B	N2
WT2C	L3
WT2D	M3
WT3A	K1
WT3B	L2
WT3C	K3
WT3D	M2
D0	N17
D1	L16
D2	M17
D3	K16
D4	L17
D5	J16
D6	K17
D7	J17

Signal	Pin Number
IOR	F16
IOG	H15
IOB	F15
COMP	K15
FS ADJUST	H16
VREF	G16
CE*	N15
R/W	N16
C1	P17
C0	P16

Signal	Pin Number
VAA	C8
VAA	G17
VAA	H17
VAA	J15
VAA	K2
VAA	R8
VAA	M16
GND	C9
GND	G2
GND	G15
GND	H2
GND	L15
GND	M15
GND	R9

Pin Descriptions (continued)—169-pin PGA Package

Bt463

(TOP VIEW)

17	P13C	P15D	P15B	TMS	TDI	TDO	VAA	VAA	D7	D6	D4	D2	D0	C1	P16D	P16B	P17D
16	P12A	P14B	P15C	P15A	TCK	IOR	VREF	FSADJ	D5	D3	D1	VAA	R/W	C0	P16C	P16A	P18D
15	P12C	P13B	P14D	P14A	P14C	IOB	GND	IOG	VAA	COMP	GND	GND	CE*	P17C	P17A	P18C	P18B
14	P11A	P13D	P13A												P17B	P18A	P19D
13	P11C	P12D	P12B												P19C	P19A	P19B
12	P10A	P11B	P11D												P20A	P20C	P20D
11	P10C	P10D	P10B												P21C	P21A	P20B
10	P9A	P9B	P9D												P22A	P22C	P21D
9	P8A	P9C	GND												GND	P22D	P21B
8	P8C	P8B	VAA												VAA	P23C	P22B
7	P7A	P8D	P7B												P24C	P23A	P23D
6	P7C	P6B	P7D												P24A	P25C	P23B
5	P6A	P6D	P5B												P26C	P25A	P24D
4	P6C	P5D	P4C	P4D											P26B	P26A	P24B
3	P5A	P4B	P3A	P3B	P3C	P1A	P0B	LD*	CLK*	WT3C	WT2C	WT2D	P27B	WT0B	P27A	P27C	P25D
2	P5C	P3D	P2A	P2C	P1C	P0A	GND	GND	CLK	VAA	WT3B	WT3D	WT2B	WT1B	WT1D	WT0D	P25B
1	P4A	P2B	P2D	P1B	P1D	P0C	P0D	SYNC*	BLK*	WT3A	WT2A	WT1A	WT1C	WT0A	WT0C	P27D	P26D
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U

alignment marker (on top)

Pin Descriptions (continued)—169-pin PGA Package

(BOTTOM VIEW)

17	P17D	P16B	P16D	C1	D0	D2	D4	D6	D7	VAA	VAA	TDO	TDI	TMS	P15B	P15D	P13C
16	P18D	P16A	P16C	C0	R/W	VAA	D1	D3	D5	FSADJ	VREF	IOR	TCK	P15A	P15C	P14B	P12A
15	P18B	P18C	P17A	P17C	CE*	GND	GND	COMP	VAA	IOG	GND	IOB	P14C	P14A	P14D	P13B	P12C
14	P19D	P18A	P17B												P13A	P13D	P11A
13	P19B	P19A	P19C												P12B	P12D	P11C
12	P20D	P20C	P20A												P11D	P11B	P10A
11	P20B	P21A	P21C												P10B	P10D	P10C
10	P21D	P22C	P22A												P9D	P9B	P9A
9	P21B	P22D	GND												GND	P9C	P8A
8	P22B	P23C	VAA												VAA	P8B	P8C
7	P23D	P23A	P24C												P7B	P8D	P7A
6	P23B	P25C	P24A												P7D	P6B	P7C
5	P24D	P25A	P26C												P5B	P6D	P6A
4	P24B	P26A	P26B											P4D	P4C	P5D	P6C
3	P25D	P27C	P27A	WT0B	P27B	WT2D	WT2C	WT3C	CLK*	LD*	P0B	P1A	P3C	P3B	P3A	P4B	P5A
2	P25B	WT0D	WT1D	WT1B	WT2B	WT3D	WT3B	VAA	CLK	GND	GND	P0A	P1C	P2C	P2A	P3D	P5C
1	P26D	P27D	WT0C	WT0A	WT1C	WT1A	WT2A	WT3A	BLK*	SYNC*	P0D	P0C	P1D	P1B	P2D	P2B	P4A
	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in *Bt451/7/8 Evaluation Module Operation and Measurements*, application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt463 power and ground lines by shielding the digital inputs and providing good decoupling. Trace lengths between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a six-layer PC board is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane (preferably analog ground plane), layer 3 the analog power plane, with the remaining layers used for digital traces and digital power supplies.

The optimum layout enables the Bt463 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8 inch gap) connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inch from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground partitioning isolation technique is constrained by the noise margin constraint during digital readback of the Bt463.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk. For maximum performance, a separate isolated ground plane for the analog output termination resistors, RSET resistor, and VREF circuitry should be used, as shown in Figure 11. Another isolated ground plane should be used for the GND pins of the Bt463 and supply decoupling capacitors.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt463 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8 inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 11, located within three inches of the Bt463. This bead provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged such that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor decoupling each of four groups of VAA pins to GND. The capacitors should be placed as close as possible to the device.

The 33 µF capacitor is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. Low frequency supply noise will require a larger value. Lead lengths should be minimized for best performance so that the self-resonance frequency is greater than the LD* frequency.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt463 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot, which can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. Prevention is done by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt463 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a load resistor and a termination resistor equal to the transmission line impedance. The load resistor connection between the current output and GND should be as close as possible to the Bt463 to minimize reflections. Unused analog outputs should be connected to GND.

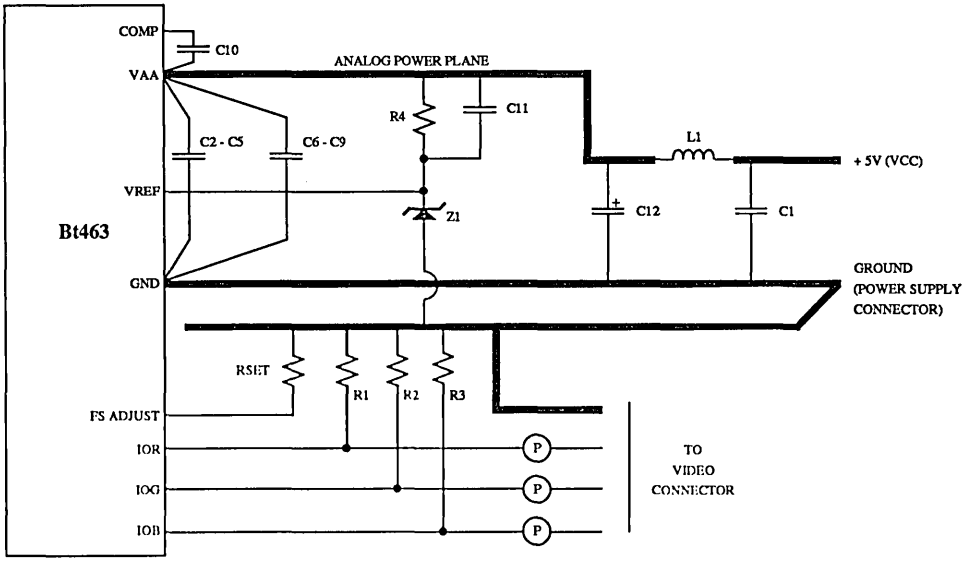
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, helping to alleviate EMI and noise problems.

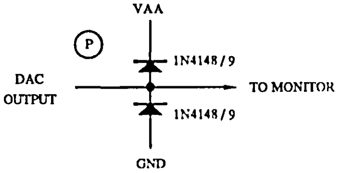
Analog Output Protection

The Bt463 analog outputs should be protected against high energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 11 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. This protection circuit should be located as close to the driver as possible. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)


COMP
C10
VAA
ANALOG POWER PLANE
R4
C11
C2 - C5
C6 - C9
L1
+ 5V (VCC)
VREF
Z1
C12
C1
Bt463
GROUND
(POWER SUPPLY
CONNECTOR)
GND
RSET
R1
R2
R3
FS ADJUST
IOR
IOG
IOB
P
TO
VIDEO
CONNECTOR


VAA
P
1N4148/9
DAC
OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description	Vendor Part Number
C1–C5, C10, C11	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C6–C9	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C12	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	523 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt463.

Figure 11. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Due to the high clock rates at which the Bt463 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (typically a 220-ohm resistor to VCC and a 330-ohm resistor to GND). The termination resistors should be as close as possible to the Bt463.

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak due to the noise margins of the CMOS process. The Bt463 will not function using a single-ended clock with CLOCK* connected to ground.

Typically, LD* is generated by dividing CLOCK by two or four (depending on whether 2:1 or 4:1 multiplexing was specified) and translating it to TTL levels. As LD* may be phase-shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

For display applications where a single Bt463 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 4:1 input multiplexing of the Bt463, and will also optionally set the pipeline delay of the Bt463 to 13 clock cycles. The Bt438 may also be used to interface the Bt463 to a TTL clock. Figure 12 illustrates using the Bt438 with the Bt463.

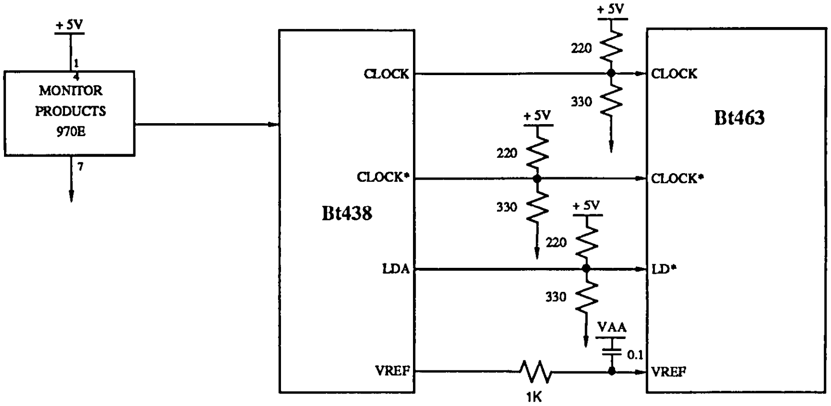


Figure 12. Generating the Bt463 Clock Signals.

Application Information (continued)

Setting the Pipeline Delay

The pipeline delay of the Bt463, although fixed after a power-up condition, may be anywhere from 11 to 15 clock cycles. The Bt463 contains additional circuitry enabling the pipeline delay to be fixed at 13 clock cycles. The Bt438 Clock Generator Chip supports this mode of operation when used with the Bt463.

To reset the Bt463, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for **at least** three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

Resetting the Bt463 to a 13 clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if multiple Bt463s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control via the read mask register and overlay display enable bits.

ESD and Latchup Considerations

ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Application Information (continued)

Test Features of the Bt463

The Bt463 contains two dedicated test registers and an analog output comparator that assist the user in evaluating the performance and functionality of the part. This section is intended to explain the operating usage of these test features.

Signature Registers (Signature Mode)

The input signature register is 16 bits wide, capturing pixel information prior to the lookup tables. Since the pixel path is 28 bits wide, the lower or upper 16 bits are selected for capture via command bit CR22.

The output signature register, in the active mode, operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel color, and are presented as inputs simultaneously to the red, green, and blue signature analysis registers (SARs), as well as the three on-chip DACs.

The SARs act as a 16-bit or 24-bit wide Linear Feedback Shift Register on each succeeding pixel that is latched. It is important to note that in either the 2:1 or 4:1 multiplexed modes the SARs only latch one pixel per "load group." Thus, the SARs are operating on only every second or fourth pixel in the multiplexed modes. The user determines which pixel phase (A, B, C, or D) is latched for generating new signatures by setting bits D0–D2 in the Test Register.

In 1:1 mux mode, the SARs will generate signatures on each succeeding pixel in the input stream. In this case, the user should always select pixel "A" (Test Register D0, D1, and D2 = 000) when in the 1:1 mode, since the "A" pixel pins are the only active pixel inputs.

The Bt463 will only generate signatures while in "active-display" (BLANK* negated). The SARs are available for reading and writing via the MPU port when the Bt463 is in a blanking state (BLANK* asserted). Specifically, it is safe to access the SARs after the DAC outputs are in the blanking state (up to 15 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 16-bit or 24-bit "seed" value into the SARs. Then, a known pixel stream will be input to the chip, say one scan-line or one frame buffer worth of pixels. Then, at the succeeding blank state, the resultant 16-bit or 24-bit signature canbe read out by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, overlay and cursor data validity is also tested using the signature registers.

Assuming the chip is running 2:1 or 4:1 mux modes, the above process would be repeated with all different pixel phases—A, B, C, or D—being selected.

It is not simple to describe algorithmically the specific linear feedback shift operation used in the Bt463. The linear feedback configurations are shown in Figures 13 and 14.

Experienced users have developed tables of specific seeds and pixel streams and recorded the signatures that result from those inputs applied to "known-good" parts. Note that a good signature from one given pixel stream can by used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed and the succeeding pixel stream fed to the SARs.

Signature Registers (Data Strobe Mode)

Setting command bit CR20 to a logic one puts the SARs into data strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the SARs from generating signatures. Instead, the SARs simply capture and hold the respective pixel phase selected.

Any MPU data written to the SARs is ignored. One use, however, is to directly check each pixel color value that is strobed into the SARs. To read out values captured in the middle of a pixel stream, the user should first freeze all inputs to the Bt463. The levels of most inputs do not matter EXCEPT that CLOCK should be high, and CLOCK* should be low. Then, the user may read out the pixel color by doing three successive MPU reads from the red, green, and blue SARs, respectively. Likewise, the input SAR may be read with 2 MPU reads.

In general, the color read-out will correspond to a pixel latched on the previous load. However, due to the pipelined data path, the color may come from an earlier load cycle. To read successive pixels, toggle LD*, pulse the CLOCK pins according to the mux state (1, 2, or 4 periods), then hold all pixel-related inputs and perform the three MPU reads as described. This process is best done on a sophisticated VLSI semiconductor tester.

Application Information (continued)

Analog Comparator

The other dedicated test structure in the Bt463 is the analog comparator. It allows the user to measure the DACs against each other, as well as against a specific reference voltage.

Four combinations of tests are selected via the Test Register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the Test Register. The capture occurs over one LD* period set by a logic one at pixel port P16 (A–D).

Due to the simple design of the comparator, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, up until capture.

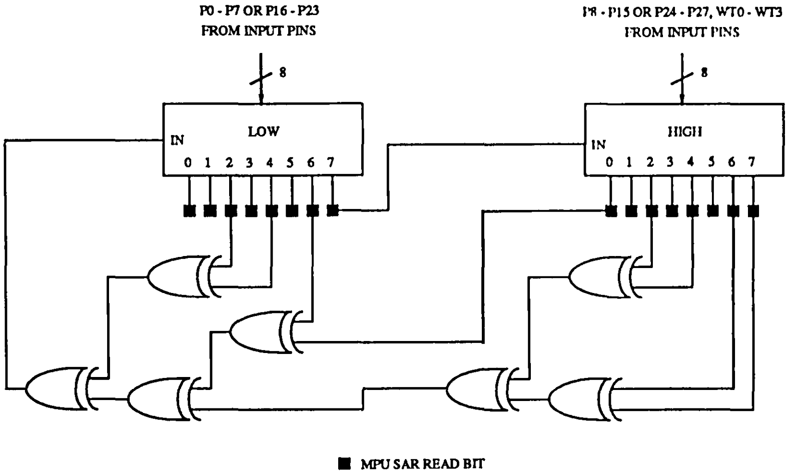

P0 - P7 OR P16 - P23
FROM INPUT PINS
8
P8 - P15 OR P24 - P27, WT0 - WT3
FROM INPUT PINS
8
LOW
IN
0 1 2 3 4 5 6 7
HIGH
IN
0 1 2 3 4 5 6 7
■ MPU SAR READ BIT

Figure 13. Input Signature Analysis Register Circuit.

Application Information (continued)

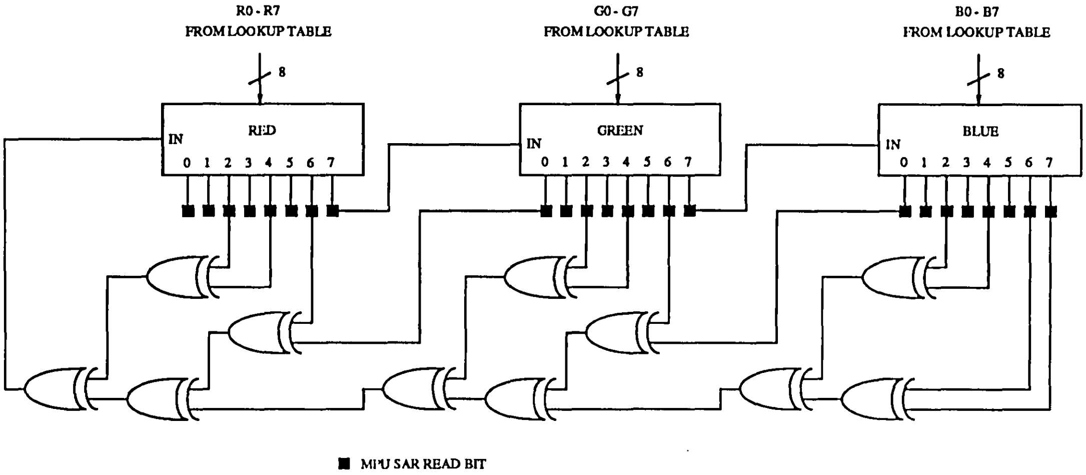

R0 - R7
FROM LOOKUP TABLE
G0 - G7
FROM LOOKUP TABLE
B0 - B7
FROM LOOKUP TABLE
8
8
8
RED
GREEN
BLUE
IN
IN
IN
0 1 2 3 4 5 6 7
0 1 2 3 4 5 6 7
0 1 2 3 4 5 6 7
■ MPU SAR READ BIT

Figure 14. Output Signature Analysis Register Circuit.

Application Information (continued)

Initializing the Bt463

Following a power-on sequence, the Bt463 must be initialized. This sequence will configure the Bt463 as follows:

4:1 multiplexed operation
4 overlay planes on P<27:23>
sync enabled on IOG, 7.5 IRE blanking pedestal
no cursor interface
24-plane true color
start address at $0001
16 window entries

Control Register Initialization

	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register 0	10
Write $00 to command register 1	10
Write $C0 to command register 2	10
Write $00 to reserved location	10
Write $FF to pixel read mask register P0- P7	10
Write $FF to pixel read mask register P8- P15	10
Write $FF to pixel read mask register P16- P23	10
Write $FF to pixel read mask register P24- P27	10
Write $00 to pixel blink mask register P0- P7	10
Write $00 to pixel blink mask register P8-P15	10
Write $00 to pixel blink mask register P16- P23	10
Write $00 to pixel blink mask register P24- P27	10
Write $00 to test register	10
Write $00 to address register low	00
Write $03 to address register high	01
Write $00 to B0-B7 register (location $0)	10
Write $E1 to B8-B15 register (location $0)	10
Write $03 to B16-B23 register (location $0)	10
Write $00 to B0-B7 register (location $1)	10
Write $E1 to B8-B15 register (location $1)	10
Write $03 to B16-B23 register (location $1)	10
:	:
Write $00 to B0-B7 register (location $F)	10
Write $E1 to B8-B15 register (location $F)	10
Write $03 to B16-B23 register (location $F)	10

Color Palette RAM Initialization

Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $000)	11
Write green data to RAM (location $000)	11
Write blue data to RAM (location $000)	11
Write red data to RAM (location $001)	11
Write green data to RAM (location $001)	11
Write blue data to RAM (location $001)	11
:	:
Write red data to RAM (location $20F)	11
Write green data to RAM (location $20F)	11
Write blue data to RAM (location $20F)	11

Cursor Color Palette Initialization

Write $00 to address register low	00
Write $01 to address register high	01
Write red data to cursor (location $0)	10
Write green data to cursor (location $0)	10
Write blue data to cursor (location $0)	10
Write red data to cursor (location $1)	10
Write green data to cursor (location $1)	10
Write blue data to cursor (location $1)	10
Write red data to cursor (location $2)*	10
Write green data to cursor (location $2)*	10
Write blue data to cursor (location $2)*	10
Write red data to cursor (location $3)*	10
Write green data to cursor (location $3)*	10
Write blue data to cursor (location $3)*	10

* Even though cursor locations $2 and $3 are not accessible, they must still be initialized in order for the cursor palette to operate correctly.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.20	1.235	1.26	Volts
FS ADJUST Resistor	RSET		523		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	Volts
Voltage on Any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
PGA	TJ			+170	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			60	µA
Input Low Current (Vin = 0.4 V)	IIL			-60	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Differential Input Voltage	ΔVIN	.6		6	Volts
Input High Current (Vin = 4.0V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			-1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0V)	CKIN		4	10	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = 400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Blank Level on IOR, IOB		0	5	50	µA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.2	Volts
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
Voltage Reference Input Current	IREF		90		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. SETUP = 7.5 IRE. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

A C Characteristics

Parameter	Symbol	Min/Typ/ Max	170 MHz	135 MHz	110 MHz	Units
Clock Rate	Fmax	max	170	135	110	MHz
LD* Rate	LDmax					
1:1 multiplexing		max	67.5	67.5	55	MHz
2:1 multiplexing		max	67.5	67.5	55	MHz
4:1 multiplexing		max	42.5	33.75	27.5	MHz
R/W, C0, C1 Setup Time	1	min	0	0	0	ns
R/W, C0, C1 Hold Time	2	min	15	15	15	ns
CE* Low Time	3	min	50	50	50	ns
CE* High Time	4	min	25	25	25	ns
CE* Asserted to Data Bus Driven	5	min	7	7	7	ns
CE* Asserted to Data Valid	6	max	75	75	75	ns
CE* Negated to Data Bus 3-Stated	7	max	15	15	15	ns
Write Data Setup Time	8	min	35	35	35	ns
Write Data Hold Time	9	min	3	3	3	ns
TMS, TDI Setup Time	10	min	8	8	8	ns
TMS, TDI Hold Time	11	min	6	6	6	ns
TCK Low Time	12	min	10	10	10	ns
TCK High Time	13	min	10	10	10	ns
TCK Asserted to TDO Driven	14	min	5	5	5	ns
TCK Asserted to TDO Valid	15	max	12	12	12	ns
TCK Negated to TDO 3-Stated	16	max	12	12	12	ns
Pixel and Control Setup Time	17	min	3	3	3	ns
Pixel and Control Hold Time	18	min	2	2	2	ns
Clock Cycle Time	19	min	5.88	7.4	9.09	ns
Clock Pulse Width High Time	20	min	2.5	3.2	4	ns
Clock Pulse Width Low Time	21	min	2.5	3.2	4	ns
LD* Cycle Time	22					
1:1 multiplexing		min	14.81	14.81	18.18	ns
2:1 multiplexing		min	14.81	14.81	18.18	ns
4:1 multiplexing		min	23.53	29.63	36.36	ns
LD* Pulse Width High Time	23					
1:1 multiplexing		min	6	6	7	ns
2:1 multiplexing		min	5	6	8	ns
4:1 multiplexing		min	9	12	15	ns
LD* Pulse Width Low Time	24					
1:1 multiplexing		min	6	6	7	ns
2:1 multiplexing		min	5	6	8	ns
4:1 multiplexing		min	9	12	15	ns

See test conditions on next page.

AC Characteristics (continued)

Parameter	Symbol	Min/Typ/ Max	170 MHz	135 MHz	110 MHz	Units
Analog Output Delay	25	typ	12	12	12	ns
Analog Output Rise/Fall Time	26	typ	1.5	1.5	1.5	ns
Analog Output Settling Time	27	max	8	8	8	ns
Clock and Data Feedthrough*		typ	tbd	tbd	tbd	dB
Glitch Impulse*		typ	50	50	50	pV - sec
DAC to DAC Crosstalk		typ	tbd	tbd	tbd	dB
Analog Output Skew		typ	0	0	0	ns
		max	2	2	2	ns
Pipeline Delay		min	11	11	11	Clocks
		max	15	15	15	Clocks
VAA Supply Current**	IAA	typ	550	500	450	mA
		max	tbd	tbd	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 523 Ω, VREF = 1.235 V. TTL input values are 0-3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are VAA–0.8 to VAA–1.8 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 75 pF. See timing notes in Figure 18. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V, TA = 20° C. IAA (max) at VAA = 5.25 V, TA = 0° C.

Timing Waveforms

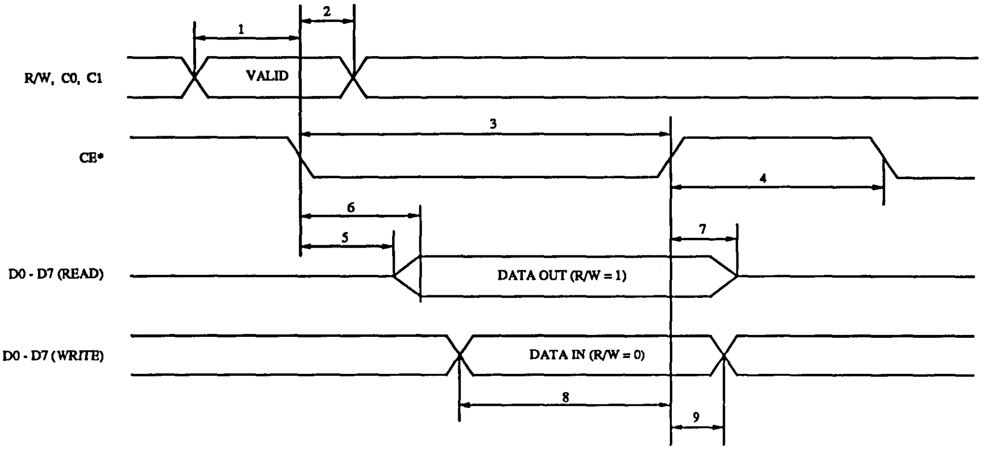
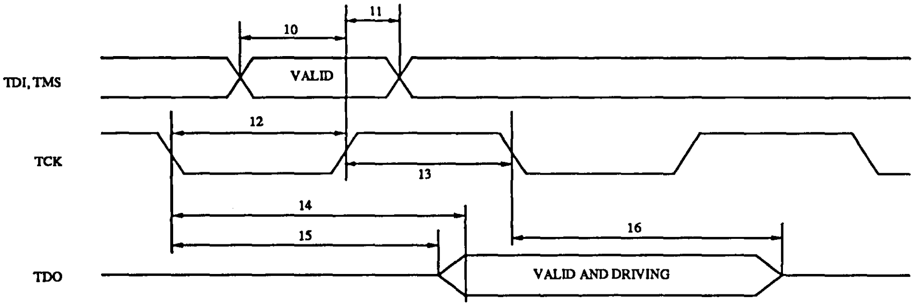

R/W, C0, C1
VALID
CE*
D0 - D7 (READ)
DATA OUT (R/W = 1)
D0 - D7 (WRITE)
DATA IN (R/W = 0)
1
2
3
4
5
6
7
8
9

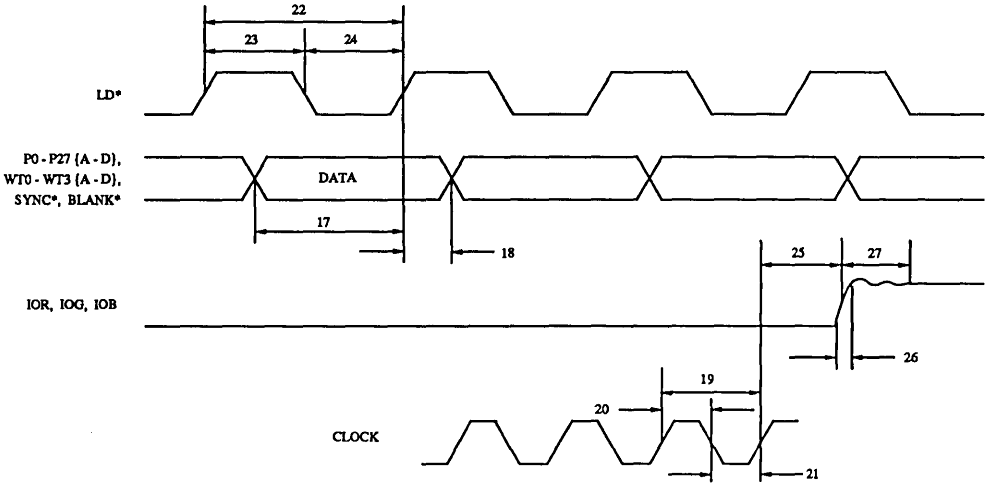
Figure 15. MPU Read/Write Timing Dimensions.


TDI, TMS
VALID
TCK
TDO
VALID AND DRIVING
10
11
12
13
14
15
16

Note 1: TMS and TDI are sampled on the rising edge of TCK

Note 2: TDO changes after the falling edge of TCK

Figure 16. JTAG Timing.


22
23
24
LD*
P0 - P27 {A - D},
WT0 - WT3 {A - D},
SYNC*, BLANK*
DATA
17
18
25
27
IOR, IOG, IOB
26
19
20
CLOCK
21

Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full-scale transition.

Note 2: Output settling time measured from 50% point of full-scale transition to output settling within ±1LSB.

Note 3: Output rise/fall time measured between 10% and 90% points of full-scale transition.

Figure 17. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt463KG170	170 MHz	169-pin Ceramic PGA	0° to +70° C
Bt463KG135	135 MHz	169-pin Ceramic PGA	0° to +70° C
Bt463KG110	110 MHz	169-pin Ceramic PGA	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
B	Additional information on start address and true-color operation.

reliminary Information

his document contains information on a product under development. The parametric formation contains target parameters and is subject to change.

Bt468

200 MHz
Monolithic CMOS
256 x 24 Color Palette
RAMDAC™

istinguishing Features

- 200, 170 MHz Operation
- 8:1 Multiplexed Pixel Ports
- 256 x 24 Color Palette RAM
- 16 x 24 Overlay Color Palette
- Pixel Panning Support
- On-Chip User-Definable Cursor
- RS-343A Compatible Outputs
- Programmable Setup (0 or 7.5 IRE)
- X Windows Support for Cursor
- Standard MPU Interface
- 145-pin PGA Package
- +5 V CMOS Monolithic Construction

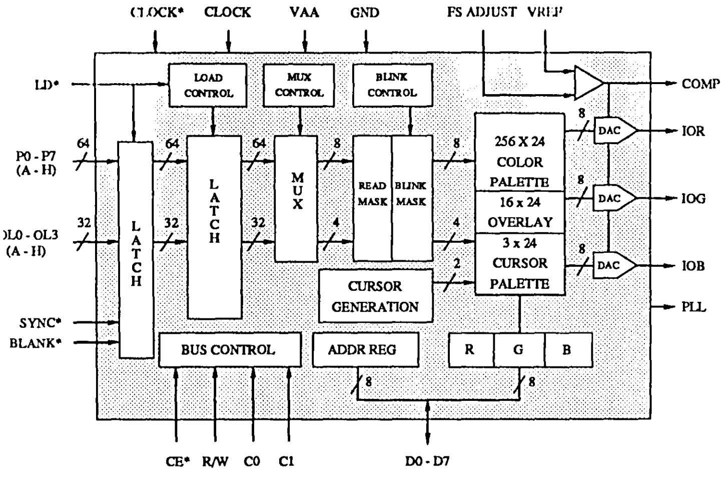
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

Related Products

- Bt438, Bt439

unctional Block Diagram


CLOCK*
CLOCK
VAA
GND
FS ADJUST
VREF
LD*
P0 - P7
(A - H)
)L0 - OL3
(A - H)
SYNC*
BLANK*
64
32
LOAD CONTROL
MUX CONTROL
BLINK CONTROL
LATCH
LATCH
MUX
READ MASK
BLINK MASK
8
4
2
256 X 24 COLOR PALETTE
16 x 24 OVERLAY
3 x 24 CURSOR PALETTE
CURSOR GENERATION
DAC
DAC
DAC
COMP
IOR
IOG
IOB
PLL
BUS CONTROL
ADDR REG
R
G
B
CE*
R/W
C0
C1
D0 - D7

Product Description

The Bt468 triple 8-bit RAMDAC is designed specifically for high-performance, high-resolution color graphics. The multiple pixel ports and internal multiplexing enables TTL-compatible interfacing to the frame buffer, while maintaining the 200 MHz video data rates required for sophisticated color graphics.

On-chip features include a 256 x 24 color palette RAM, 16 x 24 overlay color palette RAM, bit plane masking and blinking, programmable setup (0 or 7.5 IRE), and pixel panning support.

The Bt468 has an on-chip three-color 64 x 64 pixel cursor and a three-color full screen (or full window) cross hair cursor.

The PLL current output enables the synchronization of multiple devices with sub-pixel resolution.

The Bt468 generates RS-343A compatible red, green, and blue video signals, and is capable of driving doubly terminated 50 Ω or 75 Ω coax directly, without requiring external buffering. The differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

ooktree Corporation
50 Barnes Canyon Rd.
n Diego, CA 92121
19) 452-7580 • (800) VIDEO IC
X: 383 596 • FAX: (619) 452-1249
68001 Rev. D

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt468 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and color palettes. The dual-port color palette RAMs and dual-port overlay RAM allow color updating without contention with the display refresh process.

As illustrated in Table 1, the C0 and C1 control inputs, in conjunction with the internal address register, specify which control register or color palette location will be accessed by the MPU. The 16-bit address register eliminates the requirement for external address multiplexers. ADDR0 is the least significant bit.

To write color data, the MPU loads the address register with the address of the primary color palette RAM, overlay RAM, or cursor color register location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using C0 and C1 to select either the primary color palette RAM, overlay RAM, or cursor color registers. After the blue write cycle, the address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. Reading color data is similar to writing, except the MPU executes read cycles.

When accessing the color palette RAM, overlay RAM, or cursor color registers, the address register increments after each blue read or write cycle. To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three. They are reset to zero when the MPU reads or writes to the address register. The MPU does not have access to these bits. The other 12 bits of the address register (ADDR0–11) are accessible to the MPU. ADDR12–ADDR15 are always a logical zero. ADDR0 and ADDR8 correspond to D0.

ADDR0–15	C1, C0	Addressed by MPU
$xxxx	00	address register (ADDR0–7)
$xxxx	01	address register (ADDR8–15)
$0000–$00FF	10	reserved
$0100	10	overlay color 0*
:	10	:
$010F	10	overlay color 15*
$0181	10	cursor color register 1*
:	:	cursor color register 2*
$0183	10	cursor color register 3*
$0200	10	ID register ($4F)
$0201	10	command register_0
$0202	10	command register_1
$0203	10	command register_2
$0204	10	pixel read mask register
$0205	10	reserved ($00)
$0206	10	pixel blink mask register
$0207	10	reserved ($00)
$0208	10	overlay read mask register
$0209	10	overlay blink mask register
$020A	10	reserved ($00)
$020B	10	test register
$020C	10	red output signature register
$020D	10	green output signature register
$020E	10	blue output signature register
$0220	10	revision register
$0300	10	cursor command register
$0301	10	cursor (x) low register
$0302	10	cursor (x) high register
$0303	10	cursor (y) low register
$0304	10	cursor (y) high register
$0305	10	window (x) low
$0306	10	window (x) high
$0307	10	window (y) low
$0308	10	window (y) high
$0309	10	window width low register
$030A	10	window width high register
$030B	10	window height low register
$030C	10	window height high register
$0400–$07FF	10	cursor RAM
$0000–$00FF	11	color palette RAM*

*Indicates requires three read/write cycles—RGB.

Table 1. Address Register (ADDR) Operation.

Circuit Description (continued)

Additional Information

Although the color palette RAM, overlay RAM, and cursor color registers are dual-ported, if the pixel and overlay data is addressing the same palette entry being written to by the MPU during the write cycle, it is possible for one or more of the pixels on the display screen to be disturbed. A maximum of one pixel is disturbed if the write data from the MPU is valid during the entire chip enable time.

Accessing the control registers and cursor RAM is also done through the address register in conjunction with the C0 and C1 inputs, as shown in Table 1. All control registers may be written to or read by the MPU at any time. When accessing the control registers and cursor RAM, the address register increments following a read or write cycle.

Note that if an invalid address is loaded into the address register, data written to the device will be ignored and invalid data will be read by the MPU.

Figure 1 illustrates the MPU read/write timing of the Bt468.

Single-Channel RAMDAC Operation

The Bt468 may be configured (via command register_2) to be a single-channel RAMDAC, enabling three Bt468s to be used in parallel for a 24-bit true-color system. The Bt468s share a common 8-bit data bus (D0–D7).

Each Bt468 must be configured to be either a red, green, or blue RAMDAC via command register_2. Only the green channel (IOG) of each RAMDAC is used; the IOR and IOB outputs should be connected to GND, either directly or through a resistor up to 75 Ω.

To load the color palettes, the MPU performs the normal (red, green, blue) write cycles to all three RAMDACs simultaneously. The red Bt468 loads color data only during the the red write cycle, the green Bt468 loads color data only during the green write cycle, and the blue Bt468 loads color data only during the blue write cycle.

To read the color palettes, the MPU performs the normal (red, green, blue) read cycles from all three RAMDACs simultaneously. The red Bt468 outputs color data only during the the red read cycle, the green Bt468 outputs color data only during the green read cycle, and the blue Bt468 outputs color data only during the blue read cycle.

External circuitry must decode when the MPU is reading or writing to the color palettes and assert CE* to all three Bt468s simultaneously.

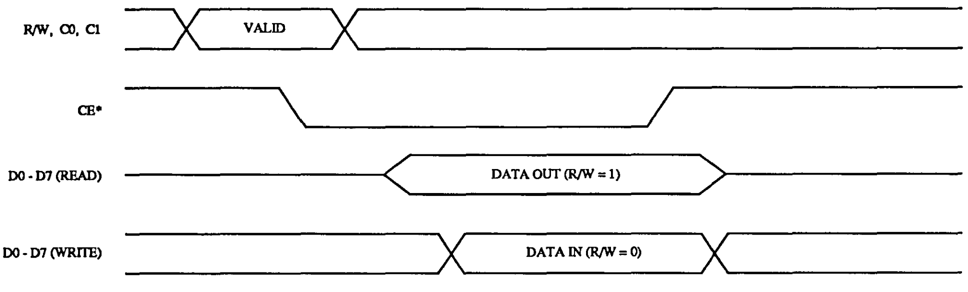


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

Frame Buffer Interface

To enable pixel data to be transferred from the frame buffer at TTL data rates, the Bt468 incorporates internal latches and multiplexers. As illustrated in Figure 2, on the rising edge of LD*, sync and blank information, color, and overlay information, for eight consecutive pixels are latched into the device. Note that with this configuration, the sync and blank timing will be recognized only with eight pixel resolution. Typically, the LD* signal is used to clock external circuitry to generate the basic video timing and to clock the video DRAMs.

Typically, the Bt468 outputs color information each clock cycle based on the {A} inputs, followed by the {B} inputs, etc., until all eight pixels have been output, at which point the cycle repeats.

The overlay inputs may have pixel timing, facilitating the use of additional bit planes in the frame buffer to control overlay selection on a pixel basis, or they may be controlled by external circuitry.

To simplify the frame buffer interface timing, LD* may be phase-shifted, in any amount, relative to CLOCK. This enables the LD* signal to be derived by externally dividing CLOCK by eight, independent of the propagation delays of the LD* generation logic. As a result, the pixel and overlay data are latched on the rising edge of LD*, independent of the clock phase.

Internal logic maintains an internal LOAD signal, synchronous to CLOCK, and is guaranteed to follow the LD* signal by at least one, but not more than six, clock cycles. This LOAD signal transfers the latched pixel and overlay data into a second set of latches, which are then internally multiplexed at the pixel clock rate.

Only one rising edge of LD* should occur every eight clock cycles. Otherwise, the internal LOAD generation circuitry assumes it is not locked onto the LD* signal, and will continuously attempt to resynchronize itself to LD*.

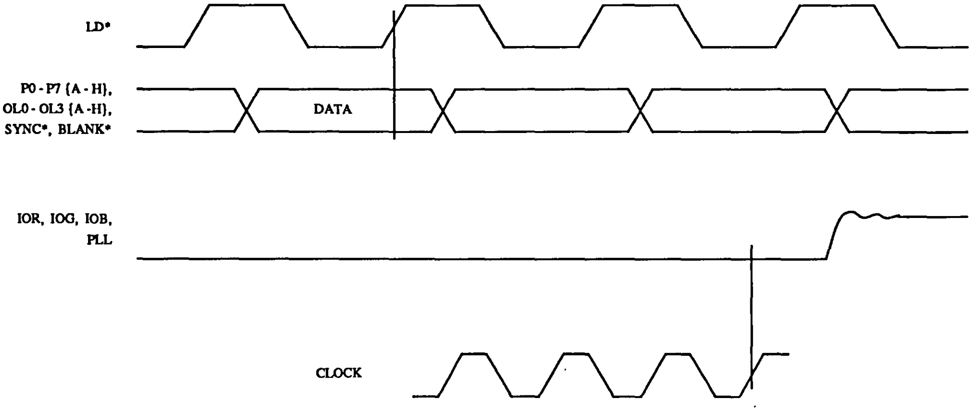


Figure 2. Video Input/Output Timing.

Circuit Description (continued)

Read and Blink Masking

Each clock cycle, 8 bits of color information (P0–P7) and 4 bits of overlay information (OL0–OL3) for each pixel are processed by the read mask, blink mask, and command registers. Through the use of the control registers, individual pixel and overlay inputs may be enabled or disabled for display, and/or blinked at one of four blink rates and duty cycles.

To ensure that a color change due to blinking does not occur during the active display time (i.e., in the middle of the screen), the Bt468 monitors the SYNC* and BLANK* input to determine vertical retrace intervals (any BLANK* pulse longer than 256 LD* cycles).

The processed pixel data is then used to select which color palette entry or overlay register is to provide color information. Note that P0 is the LSB when addressing the color palette RAMs, and OL0 is the LSB when addressing the overlay palette RAM. Table 2 illustrates the truth table used for color selection.

Pixel Panning

To support pixel panning, command register_1 specifies by how many clock cycles to pan.

If 0-pixel panning is specified, pixel {A} is output first, followed by pixel {B}, etc., until all eight pixels have been output, at which point the cycle repeats.

If 1-pixel panning is specified, pixel {B} will be first, followed by pixel {C}, etc. Pixel {A} will have been processed during the last clock cycle of the blanking interval, and will not be seen on the display screen. At the end of the active display line, pixel {A} will be output. Pixels {B} through {H} will be output during the blanking interval, and will not be seen on the display screen.

The process is similar for panning by two to seven pixels.

Note that when a panning value other than 0 pixels is specified, valid pixel data must be loaded into the Bt468 during the first LD* cycle that BLANK* is a logical zero.

The P0–P7 and OL0–OL3 inputs are all panned. Cursor position is also panned. If the user desires to keep the cursor position the same relative to the edge of the display, the X register of the cursor position should be updated at the same time the pixel panning register is updated.

Panning is done by delaying the SYNC* and BLANK* signals an additional one to seven clock cycles.

Circuit Description (continued)

On-Chip Cursor Operation

The Bt468 has an on-chip, three-color, 64 x 64 pixel, user-definable cursor. The cursor operates only with a noninterlaced video system.

The pattern for the cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. Cursor positioning is done via the cursor (x,y) register. Note that the Bt468 expects (x) to increase going right, and (y) to increase going down, as seen on the display screen. The cursor (x) position is relative to the first rising edge of LD* following the falling edge of SYNC*. The cursor (y) position is relative to the first falling edge of SYNC* that is after a vertical sync has been detected. Vertical sync is detected as the second falling edge during blank.

The resetting of the Bt468 to an eight-cycle pipeline delay is required for proper cursor pixel alignment.

Three Color 64 x 64 Cursor

The 64 x 64 x 2 cursor RAM provides 2 bits of cursor information every clock cycle during the 64 x 64 cursor window, selecting the appropriate cursor color register as follows:

plane1	plane0	cursor color
0	0	cursor not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

(0,0) enables the color palette RAM and overlay RAM to be selected as normal. Each "plane" of cursor information may also be independently enabled or disabled for display via the cursor command register (bits CR47 and CR46).

The cursor pattern and color may be changed by changing the contents of the cursor RAM. Either the cursor color registers, color palette RAM, or overlay RAM provides 24 bits of color information during the appropriate clock cycle, depending on the cursor pattern values.

The cursor is centered about the value specified by the cursor (x,y) register. Thus, the cursor (x) register specifies the location of the 31st column of the 64 x 64 array (assuming the columns start with 0 for the left-most pixel and increment to 63). Similarly, the cursor (y) register specifies the location of the 31st row of the 64 x 64 array (assuming the rows start with 0 for the top-most pixel and increment to 63). (See Figure 3.)

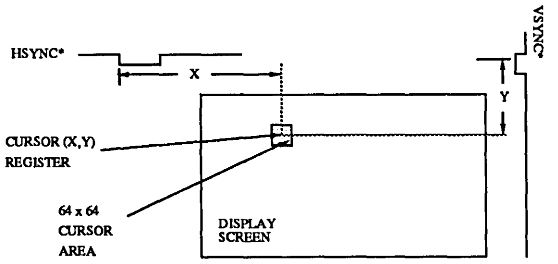


Figure 3. Cursor Positioning.

Circuit Description (continued)

Cross Hair Cursor

Cursor positioning for the three-color cross hair cursor is also done through the cursor (x,y) register. The intersection of the cross hair cursor is specified by the cursor (x,y) register. If the thickness of the cross hair cursor is greater than one pixel, the center of the intersection is the reference position.

During times that cross hair cursor information is to be displayed, the cursor command register (bits CR45 and CR44) is used to specify the color of the cross hair cursor.

CR45	CR44	cross hair color
0	0	cross hair not displayed
0	1	cursor color register 1
1	0	cursor color register 2
1	1	cursor color register 3

The cross hair cursor is limited to being displayed within the cross hair window, which is specified by the window (x,y), window width, and window height registers. Since the cursor (x,y) register must specify a point within the window boundaries, **it is the responsibility of the software to ensure that the cursor (x,y) register does not specify a point outside of the cross hair cursor window.**

If a full-screen cross hair cursor is desired, the window (x,y) registers should contain $0000 and the window width and height registers should contain $0FFF. (See Figure 4.)

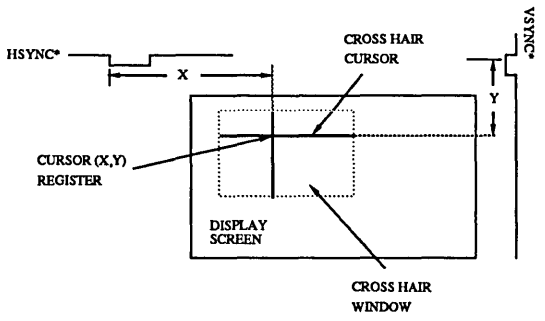


Figure 4. Cross Hair Cursor Positioning.

Circuit Description (continued)

Dual Cursor Positioning

Both the user-definable cursor and the cross hair cursor may be enabled for display simultaneously, enabling the generation of custom cross hair cursors. Both cursor planes utilize the same cursor (x,y) registers.

As previously mentioned, the cursor (x,y) register specifies the location of bit (31, 31) of the cursor RAM. As the user-definable cursor contains an even number of pixels in the horizontal and vertical direction, it will be one pixel off from being truly centered about the cross hair cursor.

Figure 5 illustrates displaying the dual cursors.

In the 64 x 64 pixel area in which the user-definable cursor would be displayed, each plane of the 64 x 64 cursor may be individually logically ORed or exclusive-ORed with the cross hair cursor information. Thus, the color of the displayed cursor will be dependent on the cursor pattern, whether they are logically ORed or XORed, and the individual cursor display enable and blink enable bits.

Figure 6 shows the equivalent cursor generation circuitry.

The resetting of the Bt468 to an eight cycle pipeline delay is required for proper cursor pixel alignment.

X Windows Cursor Mode

In the X Windows mode, plane1 of the cursor RAM is a cursor display enable and plane0 of the cursor RAM selects either cursor color 2 or 3. The operation is as follows:

plane1	plane0	Selection
0	0	no cursor
0	1	no cursor
1	0	cursor color 2
1	1	cursor color 3

Refer to Figure 9 as to the organization of the cursor RAM while in the X Windows mode.

Note that if the cursor is configured for X Windows mode, the cross hair cursor will not be displayed.

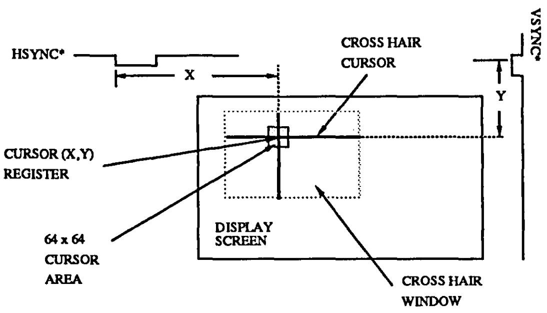


Figure 5. Dual Cursor Positioning.

Circuit Description (continued)

Video Generation

Every clock cycle, the selected 24 bits of color information are presented to the three 8-bit D/A converters.

The SYNC* and BLANK* inputs, pipelined to maintain synchronization with the pixel data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 7 and 8. Command register_2 specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be generated, and whether or not sync information is to be encoded on the video output. A 0 IRE pedestal will force the black level and the blank level to be the same.

The Bt468 can drive either doubly terminated 50 Ω or 75 Ω coax directly. If a 50 Ω double termination is used, then a typical RSET value is 348 Ω for a 7.5 IRE blanking pedestal or 332 Ω for a 0 IRE blanking pedestal. For a 75 Ω double termination, a typical RSET is 523 Ω for a 7.5 IRE blanking pedestal and 495 Ω for a 0 IRE blanking pedestal.

The varying output current from the D/A converters produces a corresponding voltage level, which is used to drive the CRT monitor. Tables 3 and 4 detail how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt468 use a segmented architecture in which bit currents are routed to either the current output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

Cursor1, Cursor0	CR05	OL0–OL3	P0–P7	Addressed by frame buffer
11	x	$x	$xx	cursor color 3
10	x	$x	$xx	cursor color 2
01	x	$x	$xx	cursor color 1
00	x	$F	$xx	overlay color 15
:	:	:	:	:
00	x	$1	$xx	overlay color 1
00	1	$0	$xx	overlay color 0
00	0	$0	$00	RAM location $00
00	0	$0	$01	RAM location $01
:	:	:	:	:
00	0	$0	$FF	RAM location $FF

Note: Refer to Figure 6 for generation of Cursor1 and Cursor0 control bits.

Table 2. Palette and Overlay Select Truth Table.

Circuit Description (continued)

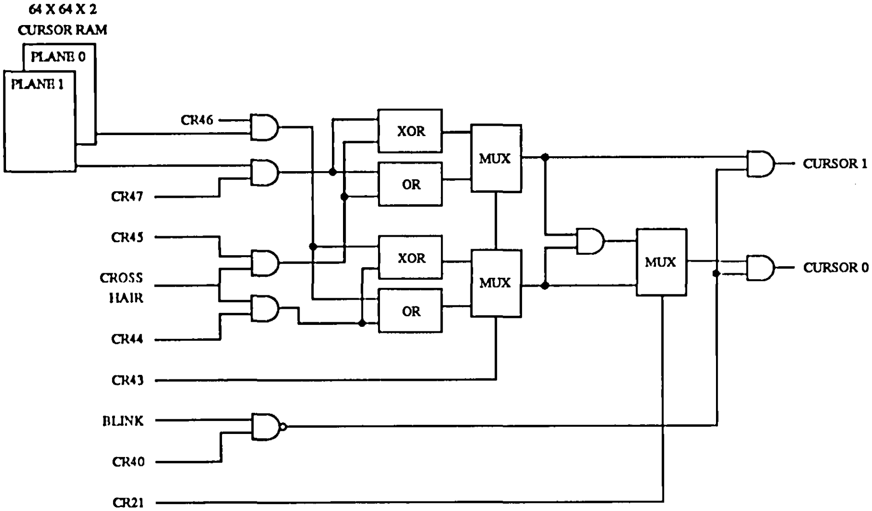
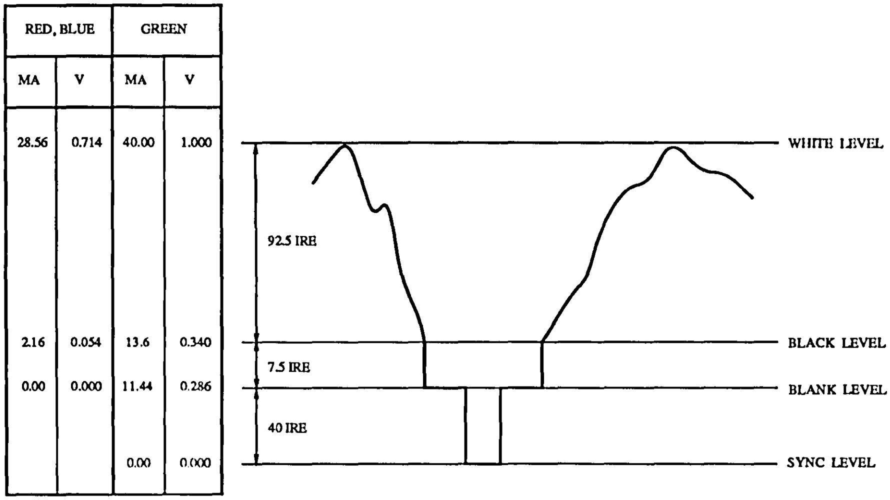

64 X 64 X 2
CURSOR RAM
PLANE 0
PLANE 1
CR46
CR47
CR45
CROSS
HAIR
CR44
CR43
BLINK
CR40
CR21
XOR
OR
XOR
OR
MUX
MUX
MUX
CURSOR 1
CURSOR 0

Figure 6. Cursor Control Circuitry.

Circuit Description (continued)


RED, BLUE
GREEN
MA
V
MA
V
28.56
0.714
40.00
1.000
2.16
0.054
13.6
0.340
0.00
0.000
11.44
0.286
0.00
0.000
92.5 IRE
7.5 IRE
40 IRE
WHITE LEVEL
BLACK LEVEL
BLANK LEVEL
SYNC LEVEL

Note: 50 Ω doubly terminated load, RSET = 348 Ω, VREF = 1.235 V. RS-343A levels and tolerances assumed on all levels.

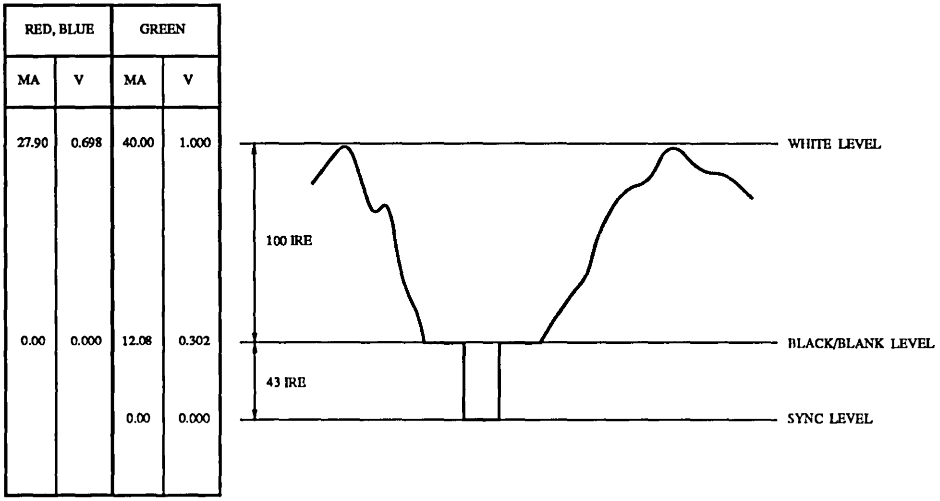
Figure 7. Composite Video Output Waveform (SETUP = 7.5 IRE).

Description	IOG (mA)	IOR, IOB (mA)	CSYNC*	BLANK*	DAC Input Data
WHITE	40	28.56	1	1	$FF
DATA	data + 13.6	data + 2.16	1	1	data
DATA - SYNC	data + 2.16	data + 2.16	0	1	data
BLACK	13.6	2.16	1	1	$00
BLACK - SYNC	2.16	2.16	0	1	$00
BLANK	11.44	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 40 mA. RSET = 348 Ω, VREF = 1.235 V.

Table 3. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)



Note: 50 Ω doubly terminated load, RSET = 332 Ω, VREF = 1.235 V. RS-343A levels and tolerances assumed on all levels.

Figure 8. Composite Video Output Waveform (SETUP = 0 IRE).

Description	IOG (mA)	IOR, IOB (mA)	CSYNC*	BLANK*	DAC Input Data
WHITE	40	27.9	1	1	$FF
DATA	data + 12.1	data	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	12.1	0	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	12.1	0	1	0	$xx
SYNC	0	0	0	0	$xx

Note: Typical with full-scale IOG = 40 mA. RSET = 332 Ω, VREF = 1.235 V.

Table 4. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register_0

This register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to data bus bit D0.

CR07	reserved (logical one)	
CR06	reserved (logical zero)	
CR05	Overlay 0 enable (0) use color palette RAM (1) use overlay color 0	When in the normal overlay mode, this bit specifies whether to use the color palette RAM or overlay color 0 to provide color information when the overlay inputs are $0. See Table 2.
CR04	reserved (logical zero)	
CR03, CR02	Blink rate selection (00) 16 on, 48 off (25/75) (01) 16 on, 16 off (50/50) (10) 32 on, 32 off (50/50) (11) 64 on, 64 off (50/50)	These 2 bits specify the blink rate cycle time and duty cycle, and are specified as the number of vertical retrace intervals. The numbers in parentheses specify the duty cycle (% on/off).
CR01, CR00	reserved (logical zero)	

Internal Registers (continued)

Command Register_1

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0.

CR17–CR15	Pan select (000) 0 pixels {pixel A} (001) 1 pixel {pixel B} (010) 2 pixels {pixel C} (011) 3 pixels {pixel D} (100) 4 pixels {pixel E} (101) 5 pixels {pixel F} (110) 6 pixels {pixel G} (111) 7 pixels {pixel H}	These bits specify the number of pixels to be panned. These bits are typically modified only during the vertical retrace interval. The {pixel A} indicates pixel A will be output first following the blanking interval, {pixel B} indicates pixel B will be output first, etc.
CR14–CR10	reserved (logical zero)	

Internal Registers (continued)

Command Register_2

This register may be written to or read by the MPU at any time and is not initialized. CR20 corresponds to data bus bit D0.

CR27	Sync Enable (0) disable sync (1) enable sync	This bit specifies whether sync information is to be output onto the IOG (logical one) or not (logical zero).
CR26	Pedestal enable (0) 0 IRE pedestal (1) 7.5 IRE pedestal	This bit specifies whether a 0 or 7.5 IRE blanking pedestal is to be generated on the video outputs. 0 IRE specifies that the black and blank levels are the same.
CR25, CR24	Load palette RAM select (00) normal (01) red RAMDAC (10) green RAMDAC (11) blue RAMDAC	If (00) is specified, color data is loaded into the Bt468 using three write cycles (red, green, and blue), and color data is output using three read cycles (red, green, and blue). Modes (01), (10), and (11) enable the Bt468 to emulate a single-channel RAMDAC using only the green channel (IOG).
CR23	PLL select (0) SYNC* (1) BLANK*	This bit specifies whether the PLL output uses SYNC* or BLANK* for generating PLL information.
CR22	reserved (logical zero)	
CR21	X Windows cursor select (0) normal cursor (1) X Windows cursor	This bit specifies whether the cursor is to operate normally (logical zero) or in an X Windows compatible mode (logical one).
CR20	Test mode select (0) signature analysis test (1) data strobe test	This bit determines the method of high-speed test used. The signature analysis registers are used to hold the test result for both test methods.

Internal Registers (continued)

ID Register

This 8-bit register may be read by the MPU to determine the type of RAMDAC being used in the system. The value is different for each RAMDAC. For the Bt468, the value read by the MPU will be $4F. Data written to this register is ignored.

Pixel Read Mask Register

The 8-bit pixel read mask register is used to enable (logical one) or disable (logical zero) a bit plane from addressing the color palette RAM. Each register bit is logically ANDed with the corresponding bit plane input. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P0.

Pixel Blink Mask Register

The 8-bit pixel blink mask register is used to enable (logical one) or disable (logical zero) a bit plane from blinking at the blink rate and duty cycle specified by command register_0. This register may be written to or read by the MPU at any time and is not initialized. D0 corresponds to P0.

Overlay Read Mask Register

The 8-bit overlay read mask register is used to enable (logical one) or disable (logical zero) an overlay plane from addressing the overlay palette RAM. D0 corresponds to overlay plane 0 (OL0 {A–H}) and D3 corresponds to overlay plane 3 (OL3 {A–H}). Bits D0–D3 are logically ANDed with the corresponding overlay plane input. D4–D7 are always a logical zero.

This register may be written to or read by the MPU at any time and is not initialized.

Overlay Blink Mask Register

The 8-bit overlay blink mask register is used to enable (logical one) or disable (logical zero) an overlay plane from blinking at the blink rate and duty cycle specified by command register_0. D0 corresponds to overlay plane 0 (OL0 {A–H}) and D3 corresponds to overlay plane 3 (OL3 {A–H}). In order for an overlay plane to blink, the corresponding bit in the overlay read mask register must be a logical one. D4–D7 are always a logical zero.

This register may be written to or read by the MPU at any time and is not initialized.

Revision Register (Revision B only)

This 8-bit is a read-only register, specifying the revision of the Bt468. The four most significant bits signify the revision letter B, in hexidecimal form. The four least significant bits do not represent any value and should be ignored. Data written to this register is ignored.

Since Revision A device does not have a revision register, address $0220 will contain the last data read to or written from the internal bus.

Internal Registers (continued)

Red, Green, and Blue Output Signature Registers

Signature Operation

These three 8-bit signature registers (one each for red, green, and blue) may be read by the MPU while BLANK* is a logical zero. While BLANK* is a logical one, the signatures are being acquired. The MPU may read from or write to the signature registers while BLANK* is a logical zero to load the seed value.

By loading a test display into the frame buffer, a deterministic value for the red, green, and blue signature registers will be read from these registers if all circuitry is working properly. Refer to the Application Information test register section for more information.

Data Strobe Operation

If command bit CR20 selects "data strobe testing," the operation of the signature registers changes slightly. Rather than determining the signature, they capture red, green, and blue data being presented to the three DACs.

Each LD* cycle, the three signature registers capture the color values being presented to the DACs. As only one of the (A–E) pixels can be captured each LD* cycle, D0–D2 of the test register are used to specify which pixel (A–E) is to be captured.

Internal Registers (continued)

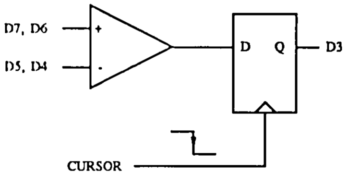
Test Register

This 8-bit register is used for testing the Bt468. D0–D2 are used to specify which pixel input to use, as follows:

D2–D0	Selection
000	pixel A
001	pixel B
010	pixel C
011	pixel D
100	pixel E
101	pixel F
110	pixel G
111	pixel H

D3–D7 are used to compare the analog RGB outputs to each other and to a 145 mV reference. This enables the MPU to determine whether the CRT monitor is connected to the analog RGB outputs or not, and whether the DACs are functional.

D7	D6	D5	D4	D3
red select	green select	blue select	145 mV ref. select	result



D7–D4		If D3 = 1	If D3 = 0
0000	normal operation	-	-
1010	red DAC compared to blue DAC	red > blue	blue > red
1001	red DAC compared to 145 mV reference	red > 145 mV	red < 145 mV
0110	green DAC compared to blue DAC	green > blue	blue > green
0101	green DAC compared to 145 mV reference	green > 145 mV	green < 145 mV

The table above lists the valid comparison combinations. A logical one enables that function to be compared; the result is D3. The comparison result is strobed into D3 on the left edge of the 64 x 64 cursor area. The output levels of the DACs should be constant for 5 µs before the left edge of the cursor.

For normal operation, D3–D7 must be a logical zero.

Internal Registers (continued)

Cursor Command Register

This command register is used to control various cursor functions of the Bt468. It is not initialized, and may be written to or read by the MPU at any time. CR40 corresponds to data bus bit D0.

CR47	64 x 64 cursor plane1 display enable (0) disable plane1 (1) enable plane1	Specifies whether plane1 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR46	64 x 64 cursor plane0 display enable (0) disable plane0 (1) enable plane0	Specifies whether plane0 of the 64 x 64 cursor is to be displayed (logical one) or not (logical zero).
CR45	Cross hair cursor plane1 display enable (0) disable plane1 (1) enable plane1	Specifies whether plane1 of the cross hair cursor is to be displayed (logical one) or not (logical zero).
CR44	Cross hair cursor plane0 display enable (0) disable plane0 (1) enable plane0	Specifies whether plane0 of the cross hair cursor is to be displayed (logical one) or not (logical zero). Note that plane0 and plane1 contain the same information.
CR43	Cursor format (0) XOR (1) OR	If both the 64 x 64 cursor and the cross hair cursor are enabled for display, this bit specifies whether the contents of the cursor RAM are to be logically exclusive-ORed (logical zero) or ORed (logical one) with the cross hair cursor.
CR42, CR41	Cross hair thickness (00) 1 pixel (01) 3 pixels (10) 5 pixels (11) 7 pixels	This bit specifies whether the vertical and horizontal thickness of the cross hair is one, three, five, or seven pixels. The segments are centered about the value in the cursor (x,y) register.
CR40	Cursor blink enable (0) blinking disabled (1) blinking enabled	This bit specifies whether the cursor is to blink (logical one) or not (logical zero). If both cursors are displayed, both will blink. The blink rate and duty cycle are as specified by command register_0.

Internal Registers (continued)

Cursor (x,y) Registers

These registers are used to specify the (x,y) coordinate of the center of the 64 x 64 pixel cursor window, or the intersection of the cross hair cursor. The cursor (x) register is made up of the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register is made up of the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). They are not initialized and may be written to or read by the MPU at any time. The cursor position is not updated until the vertical retrace interval after CYHR has been written to by the MPU.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are always a logical zero.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Cx = desired display screen (x) position + H–72

where H = number of pixels between the first rising edge of CLOCK following the falling edge of SYNC* to active video.

Values from $0000 to $0FFF may be written into the cursor (x) register.

The cursor (y) value to be written is calculated as follows:

Cy = desired display screen (y) position + V–32

where V = number of scan lines from the first falling edge of SYNC* that is two or more clock cycles after vertical sync to active video.

Values from $0FC0 (–64) to $0FBF (+4031) may be loaded into the cursor (y) register. The negative values ($0FC0 to $0FFF) are used in situations where V < 32, and the cursor must be moved off the top of the screen.

Internal Registers (continued)

Window (x,y) Registers

These registers are used to specify the (x,y) coordinate of the upper left corner of the cross hair cursor window. The window (x) register is made up of the window (x) low register (WXLR) and the window (x) high register (WXHR); the window (y) register is made up of the window (y) low register (WYLR) and the window (y) high register (WYHR). They are not initialized and may be written to or read by the MPU at any time. The window position is not updated until the vertical retrace interval after WYHR has been written to by the MPU.

WXLR and WXHR are cascaded to form a 12-bit window (x) register. Similarly, WYLR and WYHR are cascaded to form a 12-bit window (y) register. Bits D4–D7 of WXHR and WYHR are always a logical zero.

	Window (x) High (WXHR)				Window (x) Low (WXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window (y) High (WYHR)				Window (y) Low (WYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The window (x) value to be written is calculated as follows:

Wx = desired display screen (x) position + H–40

where H = number of pixels between the first rising edge of CLOCK following the falling edge of SYNC* to active video.

The window (y) value to be written is calculated as follows:

Wy = desired display screen (y) position + V

where V = number of scan lines from the first falling edge of SYNC* that is two or more clock cycles after vertical sync to active video.

Values from $0000 to $0FFF may be written to the window (x) and window (y) registers. A full-screen cross hair is implemented by loading the window (x,y) registers with $0000 and the window width and height registers with $0FFF.

Internal Registers (continued)

Window Width and Height Registers

These registers are used to specify the width and height (in pixels) of the cross hair cursor window. The window width register is made up of the window width low register (WWLR) and the window width high register (WWHR); the window height register is made up of the window height low register (WHLR) and the window height high register (WHHR). They are not initialized and may be written to or read by the MPU at any time. The window width and height are not updated until the vertical retrace interval after WHHR has been written to by the MPU.

WWLR and WWHR are cascaded to form a 12-bit window width register. Similarly, WHLR and WHHR are cascaded to form a 12-bit window height register. Bits D4–D7 of WWHR and WHHR are always a logical zero.

	Window Width High (WWHR)				Window Width Low (WWLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window Height High (WHHR)				Window Height Low (WHLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The actual window width is 16 pixels more than the value specified by the window width register. The actual window height is 16 pixels more than the value specified by the window height register. Therefore, the minimum window width is 16 pixels, and the minimum window height is 16 pixels.

Values from $0000 to $0FFF may be written to the window width and height registers.

Internal Registers (continued)

Cursor RAM

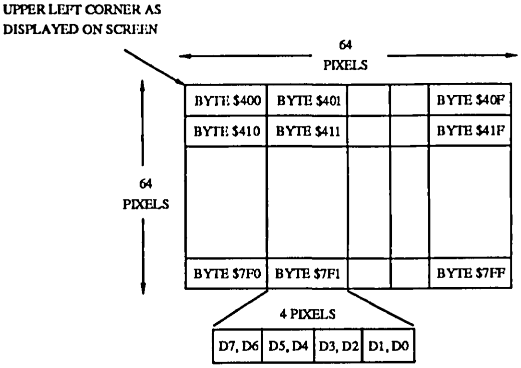
This 64 x 64 x 2 RAM is used to define the pixel pattern within the 64 x 64 pixel cursor window, and is not initialized. The cursor RAM should not be written to by the MPU during the horizontal sync time and for the two LD* cycles after the end of the horizontal sync. The cursor RAM may otherwise be written to or read by the MPU at any time without contention.

If writing to the cursor RAM asynchronously to horizontal sync, it is recommended that the cursor be positioned off-screen in the Y direction (write to the cursor (y) registers and wait for the vertical sync interval to move the cursor off-screen), write to the cursor RAM, then reposition the cursor back to the original position. An alternative is to perform a write then read sequence, and if the correct cursor RAM data was not written, perform another write then read sequence. Since the contention occurs only during horizontal sync at the Y locations coincident with the cursor, the second write/read sequence bypasses the window of time when cursor RAM is in contention.

During MPU accesses to the cursor RAM, the address register is used to address the cursor RAM. Figure 9 illustrates the internal format of the cursor RAM, as it appears on the display screen. Addressing starts at location $400 as shown in Table 1.

Note that in the X Windows mode, plane1 serves as a cursor display enable while plane0 selects one of two cursor colors (if enabled).

Note: in both modes of operation, plane1 = D7, D5, D3, D1; plane0 = D6, D4, D2, D0.



Normal Mode:

00 = color palette or overlay RAM
01 = cursor color 1
10 = cursor color 2
11 = cursor color 3

X-Windows Mode:

00 = color palette or overlay RAM
01 = color palette or overlay RAM
10 = cursor color 2
11 = cursor color 3

Figure 9. Cursor RAM as Displayed on the Screen.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog output to the blanking level, as illustrated in Tables 3 and 4. It is latched on the rising edge of LD*. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control inputs (TTL compatible). A logical zero typically switches off a 40 IRE current source on the IOG output (see Figures 7 and 8). SYNC* does not override any other control or data input, as shown in Tables 3 and 4; therefore, it should be asserted only during the blanking interval. SYNC* is latched on the rising edge of LD*.
LD*	Load control input (TTL compatible). The P0–P7 {A–H}, OL0–OL3 {A–H}, BLANK*, and SYNC* inputs are latched on the rising edge of LD*. LD*, while it is 1/8 of CLOCK, may be phase-independent of the CLOCK and CLOCK* inputs. LD* may have any duty cycle, within the limits specified by the AC Characteristics section.
P0–P7 {A–H}	Pixel select inputs (TTL compatible). These inputs are used to specify, on a pixel basis, which location of the color palette RAM is to be used to provide color information (see Table 2). Eight consecutive pixels (8 bits per pixel) are input through this port. They are latched on the rising edge of LD*. Unused inputs should be connected to GND. Note that typically the {A} pixel is output first, followed by the {B} pixel, etc., until all eight pixels have been output, at which point the cycle repeats.
OL0– OL3 {A–H}	Overlay select inputs (TTL compatible). These inputs are latched on the rising edge of LD* and, in conjunction with CR05 in command register_0, specify which palette is to be used for color information, as illustrated in Table 2. When accessing the overlay palette RAM, the P0–P7 {A–H} inputs are ignored. Overlay information (up to four bits per pixel) for eight consecutive pixels are input through this port. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly-terminated 50 Ω coaxial cable (Figure 10). All outputs, whether used or not, should have the same output load.
PLL	Phase lock loop output current. This high-impedance current source is used to enable multiple Bt468s to be synchronized with sub-pixel resolution when used with an external PLL. A logical one for SYNC* or BLANK* (as specified by CR23 in command register_2) results in no current being output onto this pin, while a logical zero results in the following current being output: PLL (mA) = 3,227 * VREF (V) / RSET (Ω) If sub-pixel synchronization of multiple devices is not required, this output should be connected to GND (either directly or through a resistor up to 150 Ω).
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between this pin and VAA (Figure 10). Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum and maximize the capacitor's self-resonant frequency to be greater than the LD* frequency. Refer to PC Board Layout Considerations for critical layout criteria.

Pin Descriptions (continued)

Pin Name	Description
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 10). Note that the IRE relationships in Figures 7 and 8 are maintained, regardless of the full-scale output current.

The relationship between RSET and the full-scale output current on IOG is:

$$RSET (\Omega) = K1 * VREF (V) / IOG (mA)$$

The full scale output current on IOR and IOB for a given RSET is:

$$IOR, IOB (mA) = K2 * VREF (V) / RSET (\Omega)$$

where K1 and K2 are defined as:

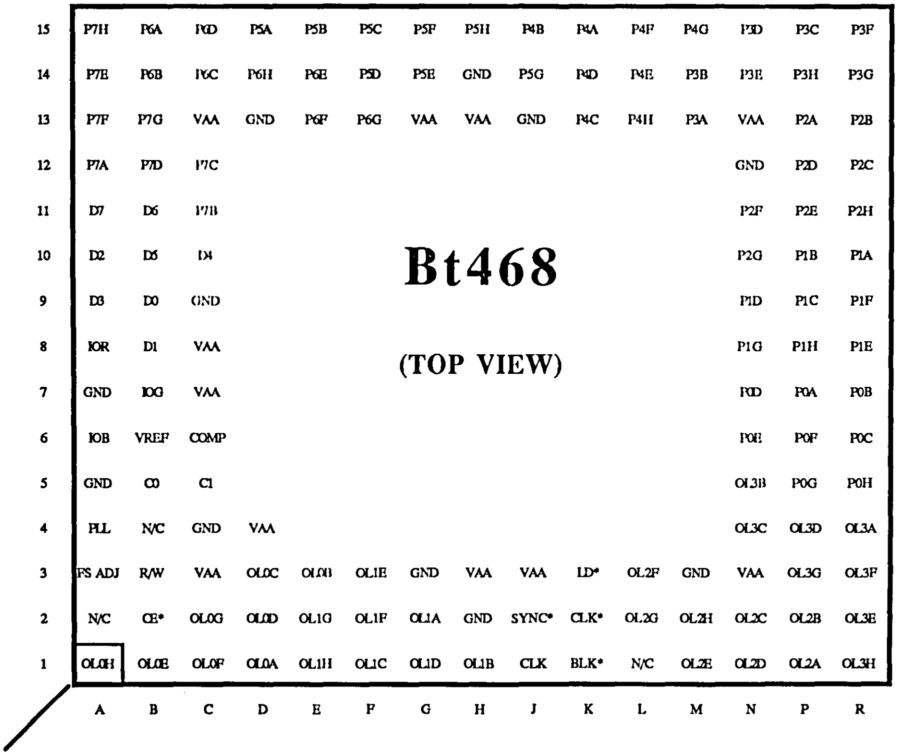
Setup	IOG	IOR, IOB
7.5 IRE	K1 = 11,294	K2 = 8,067
0 IRE	K1 = 10,684	K2 = 7,457

Pin Name	Description
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 10, must supply this input with a 1.235 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor is used to decouple this input to VAA, as shown in Figure 10. IF VAA is excessively noisy, better performance may be obtained by decoupling VREF to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
CLOCK, CLOCK*	Clock inputs. These differential clock inputs are designed to be driven by ECL logic configured for single supply (+5 V) operation. The clock rate is typically the pixel clock rate of the system.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE* (Figure 1). Care should be taken to avoid glitches on this edge-triggered input.
R/W	Read/write control input (TTL compatible). To write data to the device, both CE* and R/W must be a logical zero. To read data from the device, CE* must be a logical zero and R/W must be a logical one. R/W is latched on the falling edge of CE*. See Figure 1.
C0, C1	Command control inputs (TTL compatible). C0 and C1 specify the type of read or write operation being performed, as illustrated in Table 1. They are latched on the falling edge of CE*.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.

Pin Descriptions (continued)

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
BLANK*	K1	P5A	D15	OL2A	P1
SYNC*	J2	P5B	E15	OL2B	P2
LD*	K3	P5C	F15	OL2C	N2
CLOCK	J1	P5D	F14	OL2D	N1
CLOCK*	K2	P5E	G14	OL2E	M1
		P5F	G15	OL2F	L3
P0A	P7	P5G	J14	OL2G	L2
P0B	R7	P5H	H15	OL2H	M2
P0C	R6				
P0D	N7	P6A	B15	OL3A	R4
P0E	N6	P6B	B14	OL3B	N5
P0F	P6	P6C	C14	OL3C	N4
P0G	P5	P6D	C15	OL3D	P4
P0H	R5	P6E	E14	OL3E	R2
		P6F	E13	OL3F	R3
P1A	R10	P6G	F13	OL3G	P3
P1B	P10	P6H	D14	OL3H	R1
P1C	P9				
P1D	N9	P7A	A12	D0	B9
P1E	R8	P7B	C11	D1	B8
P1F	R9	P7C	C12	D2	A10
P1G	N8	P7D	B12	D3	A9
P1H	P8	P7E	A14	D4	C10
		P7F	A13	D5	B10
P2A	P13	P7G	B13	D6	B11
P2B	R13	P7H	A15	D7	A11
P2C	R12				
P2D	P12	OL0A	D1	VAA	C3
P2E	P11	OL0B	E3	VAA	C7
P2F	N11	OL0C	D3	VAA	C8
P2G	N10	OL0D	D2	VAA	C13
P2H	R11	OL0E	B1	VAA	D4
		OL0F	C1	VAA	G13
P3A	M13	OL0G	C2	VAA	H3
P3B	M14	OL0H	A1	VAA	H13
P3C	P15			VAA	J3
P3D	N15	OL1A	G2	VAA	N3
P3E	N14	OL1B	H1	VAA	N13
P3F	R15	OL1C	F1		
P3G	R14	OL1D	G1	GND	A5
P3H	P14	OL1E	F3	GND	A7
		OL1F	F2	GND	C4
P4A	K15	OL1G	E2	GND	C9
P4B	J15	OL1H	E1	GND	D13
P4C	K13			GND	G3
P4D	K14	IOR	A8	GND	H2
P4E	L14	IOG	B7	GND	H14
P4F	L15	IOB	A6	GND	J13
P4G	M15	PLL	A4	GND	M3
P4H	L13			GND	N12
		CE*	B2		
COMP	C6	R/W	B3	reserved	A2
FS ADJUST	A3	C0	B5	reserved	B4
VREF	B6	C1	C5	reserved	L1

Pin Descriptions (continued)



Bt468

(TOP VIEW)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R
15	P7H	P6A	P6D	P5A	P5B	P5C	P5F	P5H	P4B	P4A	P4F	P4G	P3D	P3C	P3F
14	P7E	P6B	P6C	P6H	P6E	P5D	P5E	GND	P5G	P4D	P4E	P3B	P3E	P3H	P3G
13	P7F	P7G	VAA	GND	P6F	P6G	VAA	VAA	GND	P4C	P4H	P3A	VAA	P2A	P2B
12	P7A	P7D	P7C										GND	P2D	P2C
11	D7	D6	P7B										P2F	P2E	P2H
10	D2	D5	D4										P2G	P1B	P1A
9	D3	D0	GND										P1D	P1C	P1F
8	IOR	D1	VAA										P1G	P1H	P1E
7	GND	IOG	VAA										P0D	P0A	P0B
6	IOB	VREF	COMP										P0E	P0F	P0C
5	GND	C0	C1										OL3B	P0G	P0H
4	PLL	N/C	GND	VAA									OL3C	OL3D	OL3A
3	FS ADJ	R/W	VAA	OL0C	OL0B	OL1E	GND	VAA	VAA	LD*	OL2F	GND	VAA	OL3G	OL3F
2	N/C	CE*	OL0G	OL0D	OL1G	OL1F	OL1A	GND	SYNC*	CLK*	OL2G	OL2H	OL2C	OL2B	OL3E
1	OL0H	OL0E	OL0F	OL0A	OL1H	OL1C	OL1D	OL1B	CLK	BLK*	N/C	OL2E	OL2D	OL2A	OL3H

alignment
marker
(on top)

Pin Descriptions (continued)

15	P3F	P3C	P3D	P4G	P4F	P4A	P4B	P5H	P5F	P5C	P5B	P5A	P6D	P6A	P7H
14	P3G	P3H	P3E	P3B	P4E	P4D	P5G	GND	P5E	P5D	P6E	P6H	P6C	P6B	P7E
13	P2B	P2A	VAA	P3A	P4H	P4C	GND	VAA	VAA	P6G	P6F	GND	VAA	P7G	P7F
12	P2C	P2D	GND										P7C	P7D	P7A
11	P2H	P2E	P2F										P7B	D6	D7
10	P1A	P1B	P2G										D4	D5	D2
9	P1F	P1C	P1D										GND	D0	D3
8	P1E	P1H	P1G										VAA	D1	IOR
7	P0B	P0A	P0D										VAA	IOG	GND
6	P0C	P0F	P0E										COMP	VREF	IOB
5	P0H	P0G	OL3B										C1	C0	GND
4	OL3A	OL3D	OL3C									VAA	GND	N/C	PLL
3	OL3F	OL3G	VAA	GND	OL2F	LD*	VAA	VAA	GND	OL1E	OL0B	OL0C	VAA	R/W	FS ADJ
2	OL3E	OL2B	OL2C	OL2H	OL2G	CLK*	SYNC*	GND	OL1A	OL1F	OL1G	OL0D	OL0G	CE*	N/C
1	OL3H	OL2A	OL2D	OL2E	N/C	BLK*	CLK	OL1B	OL1D	OL1C	OL1H	OL0A	OL0F	OL0E	OL0H
	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A

Bt468

(BOTTOM VIEW)

alignment
marker
(on top)

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in Bt451/7/8 Evaluation Module Operation and Measurements, application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt468 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a six-layer PC board is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) the analog traces, layer 2 the ground plane (preferably the analog ground plane), layer 3 the analog power plane, using the remaining layers for digital traces and digital power supplies.

The optimum layout enables the Bt468 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8-inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground partitioning isolation technique is constrained by the noise margin degradation during digital readback of the Bt468.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

For maximum performance, a separate isolated ground plane for the analog output termination resistors, RSET resistor, and VREF circuitry should be used, as shown in Figure 10. Another isolated ground plane is used for the GND pins of the Bt468 and supply decoupling capacitors.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt468 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 10. This bead should be located within 3 inches of the Bt468 and provides resistance to switching currents, acting as a low pass filter at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors have minimum inductance and are preferred. Radial lead ceramic capacitors may be substituted for chip capacitors. Axial lead capacitors are not recommended because of self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor decoupling each of the six groups of VAA pins to GND. The capacitors should be placed as close as possible to the device.

The 33 µF capacitor is for low-frequency power supply ripple; the 0.1 µF and 0.01 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. Lead lengths should be minimized for best performance so that the self-resonance frequency is greater than the LD* frequency.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt468 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit by using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt468 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt468 to minimize reflections. Unused analog outputs should be connected to GND.

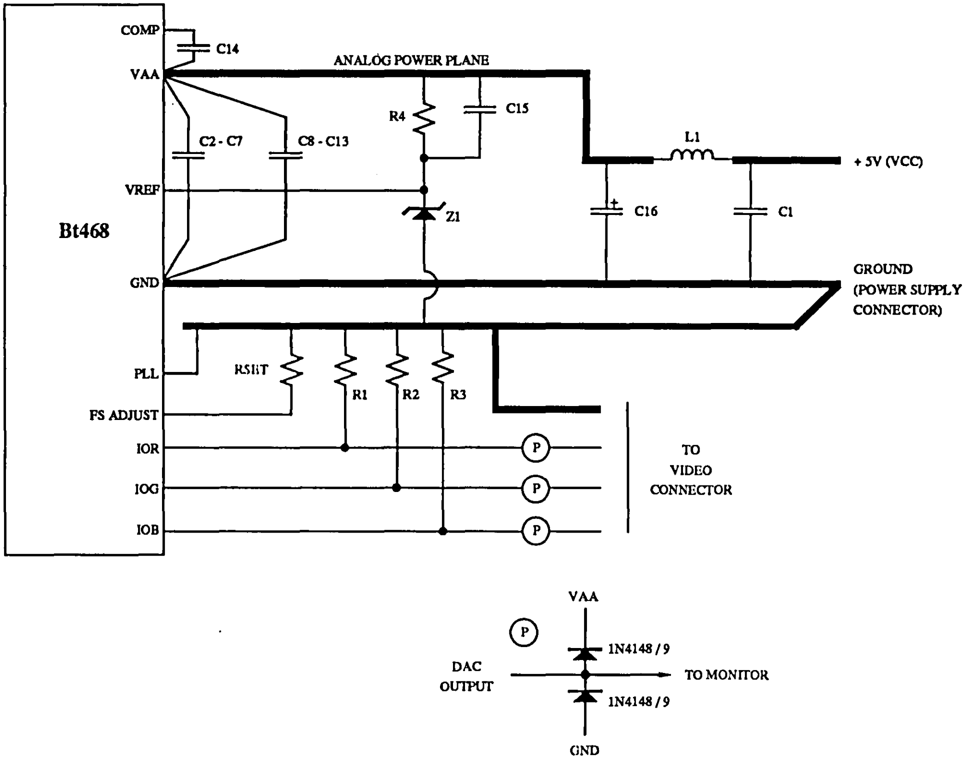
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

Analog Output Protection

The Bt468 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 10 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)


COMP
C14
VAA
ANALOG POWER PLANE
R4
C15
C2 - C7
C8 - C13
L1
+ 5V (VCC)
VREF
Z1
C16
C1
Bt468
GND
GROUND
(POWER SUPPLY
CONNECTOR)
PLL
RSET
R1
R2
R3
FS ADJUST
IOR
IOG
IOB
P
TO
VIDEO
CONNECTOR
VAA
P
1N4148 / 9
DAC
OUTPUT
TO MONITOR
1N4148 / 9
GND

Location	Description	Vendor Part Number
C1–C7, C14, C15	0.1 µF ceramic capacitor	Erie RPE110Z5U104M50V
C8–C13	0.01 µF ceramic chip capacitor	AVX 12102T103QA1018
C16	33 µF tantalum capacitor	Mallory CSR13F336KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	50 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET	348 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385Z-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt468.

Figure 10. Typical Connection Diagram and Parts List.

Application Information

Clock Interfacing

Due to the high clock rates at which the Bt468 may operate, it is designed to accept differential clock signals (CLOCK and CLOCK*). These clock inputs are designed to be generated by ECL logic operating at +5 V. Note that the CLOCK and CLOCK* inputs require termination resistors (typically a 220 Ω resistor to VCC and a 330 Ω resistor to GND). The termination resistors should be as close as possible to the Bt468.

The CLOCK and CLOCK* inputs must be differential signals and greater than 0.6 V peak-to-peak due to the noise margins of the CMOS process. The Bt468 will not function using a single-ended clock with CLOCK* connected to ground.

170 MHz and greater applications require robust ECL clock signals with strong pull-down (~20 mA at VOH) and double termination for clock trace lengths greater than 2 inches.

Typically, LD* is generated by dividing CLOCK by eight and translating it to TTL levels. As LD* may be phase-shifted relative to CLOCK, the designer need not worry about propagation delays in deriving the LD* signal. LD* may be used as the shift clock for the video DRAMs and to generate the fundamental video timing of the system (SYNC*, BLANK*, etc.).

For display applications where a single Bt468 is being used, it is recommended that the Bt438 Clock Generator Chip be used to generate the clock and load signals. It supports the 8:1 input multiplexing of the Bt468, and sets the pipeline delay of the Bt468 to eight clock cycles. Figure 11 illustrates using the Bt438 with the Bt468.

When using a single Bt468, the PLL output is ignored and should be connected to GND (either directly or through a resistor up to 150 Ω).

Using Multiple Bt468s

For display applications where up to four Bt468s are being used, it is recommended that the Bt439 Clock Generator Chip be used to generate the clock and load signals. It supports the 8:1 input multiplexing of the Bt468, synchronizes them to sub-pixel resolution, and sets the pipeline delay of the Bt468 to eight clock cycles. Figure 12 illustrates using the Bt439 with the Bt468.

Sub-pixel synchronization is supported via the PLL output. Essentially, PLL provides a signal to indicate the amount of analog output delay of the Bt468, relative to CLOCK. The Bt439 compares the phase of the PLL signals generated by up to four Bt468s, and adjusts the phase of each of the CLOCK and CLOCK* signals to the Bt468s to minimize the PLL phase difference. There should be minimal layout skew in the CLOCK and PLL trace paths to assure proper clock alignment.

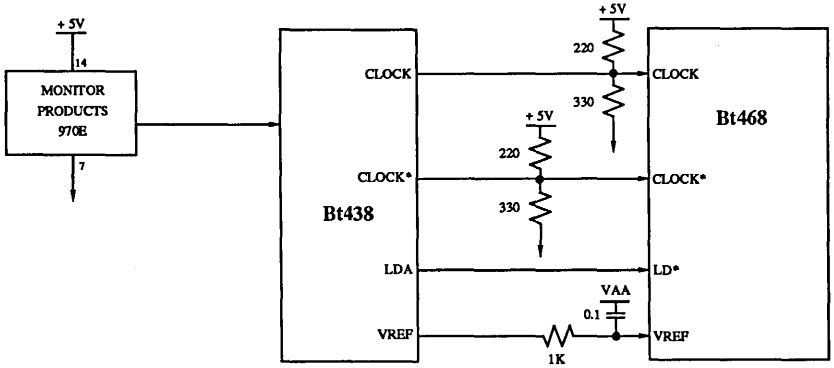


Figure 11. Generating the Bt468 Clock Signals.

Application Information (continued)

If sub-pixel synchronization of multiple Bt468s is not necessary, the Bt438 Clock Generator Chip may be used instead of the Bt439. In this instance, the CLOCK, CLOCK*, and LD* inputs of up to four Bt468s are connected together, and driven by a single Bt438 (daisy chain with single balanced termination for <100 MHz or through a 10H116 buffer for >100 MHz). The designer must take care to minimize skew on the CLOCK and CLOCK* lines. The PLL outputs would not be used and should be connected to GND (either directly or through a resistor up to 150 Ω). When using multiple Bt468s, each Bt468 should have its own power plane ferrite bead. In addition, a single voltage reference may drive multiple devices; however, isolation resistors are recommended to reduce color channel crosstalk.

Each Bt468 must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and VREF capacitor.

Setting the Pipeline Delay

The pipeline delay of the Bt468, although fixed after a power-up condition, may be anywhere from six to ten clock cycles. The Bt468 contains additional circuitry enabling the pipeline delay to be fixed at eight clock cycles. The Bt438 and Bt439 Clock Generator Chips support this mode of operation when used with the Bt468.

To reset the Bt468, it should be powered up, with LD*, CLOCK, and CLOCK* running. Stop the CLOCK and CLOCK* signals with CLOCK high and CLOCK* low for at least three rising edges of LD*. There is no upper limit on how long the device can be held with CLOCK and CLOCK* stopped.

Restart CLOCK and CLOCK* so that the first edge of the signals is as close as possible to the rising edge of LD* (the falling edge of CLOCK leads the rising edge of LD* by no more than 1 clock cycle or follows the rising edge of LD* by no more than 1.5 clock cycles). When restarting the clocks, care must be taken to ensure that the minimum clock pulse width is not violated.

In order to assure that the Bt468 has the proper configuration, all of the command registers must be initialized prior to a fixed pipeline reset. Because of this requirement, the power up which occurs prior to initialization of the command registers cannot be used to assure the fixed pipeline. An additional reset is required after command register writes.

The resetting of the Bt468 to an eight clock cycle pipeline delay does not reset the blink counter circuitry. Therefore, if the multiple Bt468s are used in parallel, the on-chip blink counters may not be synchronized. In this instance, the blink mask register should be $00 and the overlay blink enable bits a logical zero. Blinking may be done under software control via the read mask register and overlay display enable bits.

Resetting the Bt468 to an eight clock cycle pipeline delay is required for proper cursor pixel alignment.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Application Information (continued)

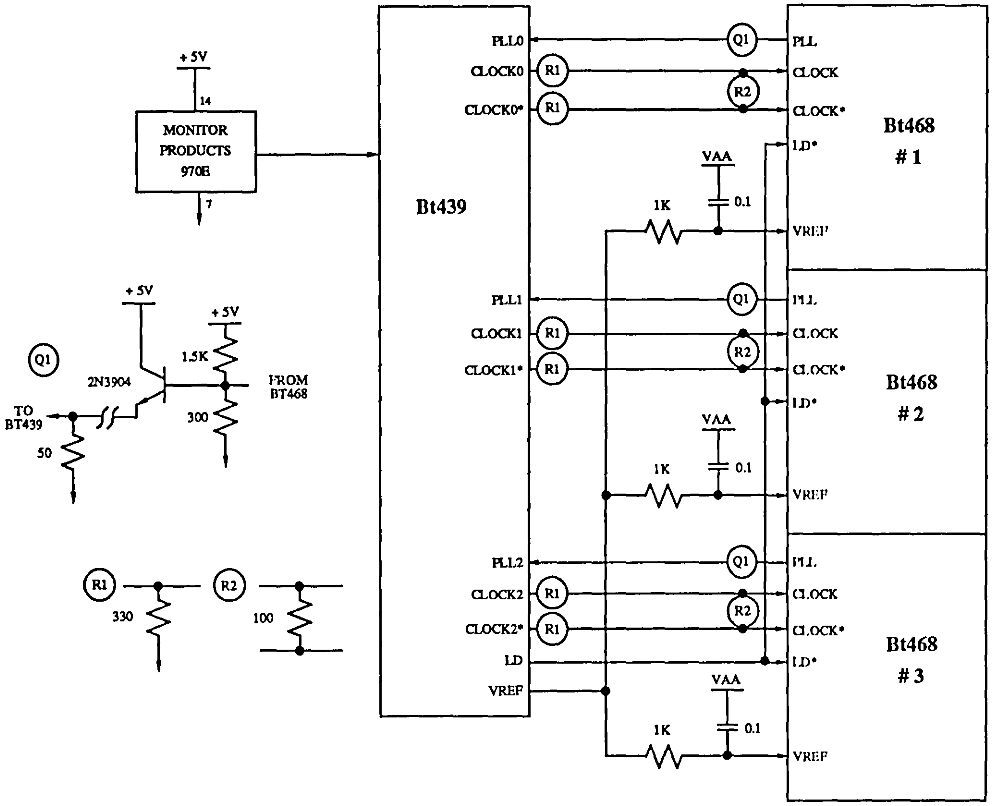

+5V
14
MONITOR PRODUCTS 970B
7
Bt439
PLL0
CLOCK0
CLOCK0*
PLL1
CLOCK1
CLOCK1*
PLL2
CLOCK2
CLOCK2*
LD
VREF
R1
R2
Q1
VAA
1K
0.1
PLL
CLOCK
CLOCK*
LD*
VREF
Bt468 #1
Bt468 #2
Bt468 #3
Q1
+5V
+5V
1.5K
2N3904
FROM BT468
TO BT439
300
50
R1
330
R2
100

Figure 12. Generating the Clock Signals for Multiple Bt468s.

Application Information (continued)

Test Features of the Bt468

The Bt468 contains two dedicated test registers and an analog output comparator that assist the user in evaluating the performance and functionality of the part. This section is intended to explain the operating usage of these test features.

Signature Register (Signature Mode)

The signature register, in the active mode, operates with the 24 bits of data that are output from the color palette RAM. These 24-bit vectors represent a single pixel color, and are presented as inputs simultaneously to the red, green, and blue signature analysis registers (SARs), as well as the three on-chip DACs.

The SARs act as a 24-bit wide Linear Feedback Shift Register on each succeeding pixel that is latched. It is important to note that the SARs only latch one pixel per "load group." Thus the SARs are operating on only every eighth pixel in the multiplexed modes. The user determines which pixel phase (A, B, C, D, E, F, G, or H) is latched for generating new signatures by setting bits D0–D2 in the Test Register.

The Bt468 will only generate signatures while in "active-display" (BLANK* negated). The SARs are available for reading and writing via the MPU port when the Bt468 is in a blanking state (BLANK* asserted). Specifically, it is safe to access the SARs after the DAC outputs are in the blanking state (up to 15 pixel clock periods after BLANK* is asserted).

Typically, the user will write a specific 24-bit "seed" value into the SARs. Then, a known pixel stream will be input to the chip, say one scan-line or one frame buffer worth of pixels. Then, at the succeeding blank state, the resultant 24-bit signature can be read out by the MPU. The 24-bit signature register data is a result of the same captured data that is fed to the DACs. Thus, overlay and cursor data validity is also tested using the signature registers.

The above process would be repeated with all different pixel phases—A, B, C, etc.,—being selected.

It is not simple to specify the algorithm which desceibes the linear feedback shift operation used in the Bt468. The linear feedback configuration is shown in Figure 13. Note that each register internally uses XORs at each input bit (D_n) with the output (result) by one least significant bit (Q_{n-1}).

Experienced users have developed tables of specific seeds and pixel streams and recorded the signatures that result from those inputs applied to "known-good" parts. Note that a good signature from one given pixel stream can be used as the seed for the succeeding stream to be tested. Any signature is deterministically created from a starting seed and the succeeding pixel stream fed to the SARs.

Signature Register (Data Strobe Mode)

Setting command bit CR20 to "1" puts the SARs into data strobe mode. In this instance, the linear feedback circuits of the SARs are disabled, which stops the SARs from generating signatures. Instead, the SARs simply capture and hold the respective pixel phase that is selected.

Any MPU data written to the SARs is ignored. One use, however, is to directly check each pixel color value that is strobed into the SARs. To read out a captured color in the middle of a pixel stream, the user should first freeze all inputs to the Bt468. The levels of most inputs do not matter EXCEPT that CLOCK should be high, and CLOCK* should be low. Then, the user may read out the pixel color by doing three successive MPU reads from the red, green, and blue SARs, respectively.

In general, the color read out will correspond to a pixel latched on the previous load. However, due to the pipelined data path, the color may come from an earlier load cycle. To read successive pixels, toggle LD*, pulse the CLOCK pins according to the mux state (eight periods), then hold all pixel-related inputs and perform the three MPU reads as described. This overall process is best done on a sophisticated VLSI semiconductor Tester.

Application Information (continued)

Analog Comparator

The other dedicated test structure in the Bt468 is the analog output comparator. It allows the user to measure the DACs against each other, as well as against a specific reference voltage.

Four combinations of tests are selected via the Test Register. With a given setting, the respective signals (DAC outputs or the 145 mV reference) will be continuously input to the comparator. The result of the comparator is latched into the Test Register on each of the 64 scan lines of the 64 x 64 user-defined cursor block (the 64 x 64 cursor must be enabled for display). On each of these 64 scan lines, the capture occurs over one LD* period that corresponds to the cursor (x) position, set by the 12-bit cursor (x) register.

To obtain a meaningful comparison, the cursor should be located on the visible screen. There is no significance to the cursor pattern data in the cursor RAM. For a visual reference, the capture point actually occurs over the left-most edge of the 64 x 64 cursor block.

Due to the simple design of the comparator, it is recommended that the DAC outputs be stable for 5 µs before capture. At a display rate of 100 MHz, 5 µs corresponds to 500 pixels. In this case, the cursor (x) position should be set to well over 500 pixels to ensure an adequate supply of pixels. Furthermore, either the color palette RAM or the pixel inputs (or both) should be configured to guarantee a single continuous output from the DACs under test, up until capture.

Typically, users will create screen-wide test bands of various colors. Various comparison cases are set up by moving the cursor up and down (by changing the 12-bit cursor (y) register) over these bands. For each test, the result is obtained by reading Test Register bit D3.

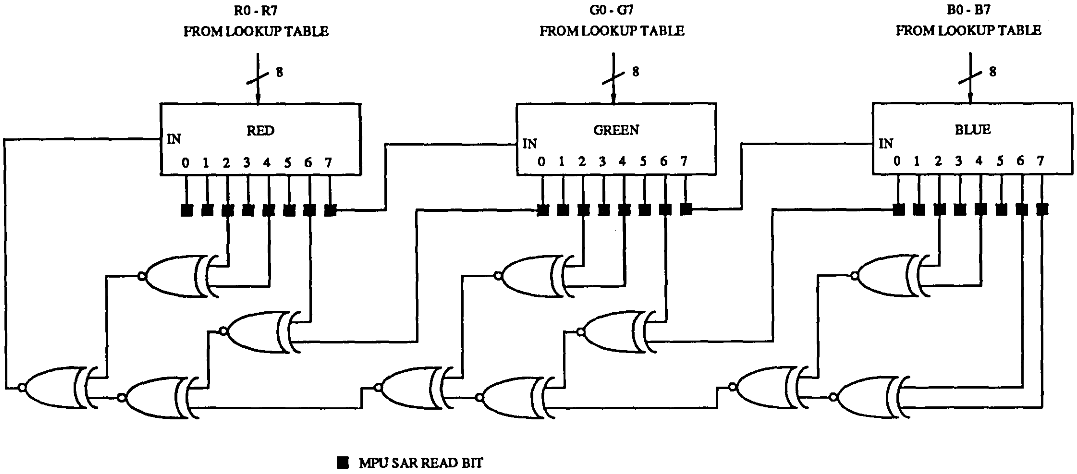


Figure 13. Signature Analysis Register Circuit.

Application Information (continued)

Initializing the Bt468

Following a power-on sequence, the Bt468 must be initialized. This sequence will configure the Bt468 as follows:

8:1 multiplexed operation
no overlays, no blinking, no panning
64 x 64 block cursor, no cross hair cursor
sync enabled on IOG, 7.5 IRE blanking pedestal

Control Register Initialization

	C1, C0
Write $01 to address register low	00
Write $02 to address register high	01
Write $40 to command register_0	10
Write $00 to command register_1	10
Write $C0 to command register_2	10
Write $FF to pixel read mask register	10
Write $00 to reserved location	10
Write $00 to pixel blink mask register	10
Write $00 to reserved location	10
Write $00 to overlay read mask register	10
Write $00 to overlay blink mask register	10
Write $00 to reserved location	10
Write $00 to test register	10

Write $00 to address register low	00
Write $03 to address register high	01
Write $C0 to cursor command register	10
Write $00 to cursor (x) low register	10
Write $00 to cursor (x) high register	10
Write $00 to cursor (y) low register	10
Write $00 to cursor (y) high register	10
Write $00 to window (x) low register	10
Write $00 to window (x) high register	10
Write $00 to window (y) low register	10
Write $00 to window (y) high register	10
Write $00 to window width low register	10
Write $00 to window width high register	10
Write $00 to window height low register	10
Write $00 to window height high register	10

Load Cursor RAM Pattern

Write $00 to address register low	00
Write $04 to address register high	01
Write $FF to cursor RAM (location $000)	10
Write $FF to cursor RAM (location $001)	10
:	:
Write $FF to cursor RAM (location $3FF)	10

Color Palette RAM Initialization

Write $00 to address register low	00
Write $00 to address register high	01
Write red data to RAM (location $00)	11
Write green data to RAM (location $00)	11
Write blue data to RAM (location $00)	11
Write red data to RAM (location $01)	11
Write green data to RAM (location $01)	11
Write blue data to RAM (location $01)	11
:	:
Write red data to RAM (location $FF)	11
Write green data to RAM (location $FF)	11
Write blue data to RAM (location $FF)	11

Overlay Color Palette Initialization

Write $00 to address register low	00
Write $01 to address register high	01
Write red data to overlay (location $0)	10
Write green data to overlay (location $0)	10
Write blue data to overlay (location $0)	10
Write red data to overlay (location $1)	10
Write green data to overlay (location $1)	10
Write blue data to overlay (location $1)	10
:	:
Write red data to overlay (location $F)	10
Write green data to overlay (location $F)	10
Write blue data to overlay (location $F)	10

Cursor Color Palette Initialization

Write $81 to address register low	00
Write $01 to address register high	01
Write red data to cursor (location $0)	10
Write green data to cursor (location $0)	10
Write blue data to cursor (location $0)	10
Write red data to cursor (location $1)	10
Write green data to cursor (location $1)	10
Write blue data to cursor (location $1)	10
Write red data to cursor (location $2)	10
Write green data to cursor (location $2)	10
Write blue data to cursor (location $2)	10

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		25		Ohms
Reference Voltage	VREF	1.20	1.235	1.26	Volts
FS ADJUST Resistor	RSET		348		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				6.5	Volts
Voltage on any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs (except CLOCK, CLOCK*)					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND – 0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4	10	pF
Clock Inputs (CLOCK, CLOCK*)					
Input Differntial Voltage	ΔVIN	.6		6	Volts
Input High Current (Vin = 4.0 V)	IKIH			1	µA
Input Low Current (Vin = 0.4 V)	IKIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CKIN		4	10	pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-state Current	IOZ			10	µA
Output Capacitance	CDOUT		10		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Blank		26.56	28.56	30.56	mA
White Level Relative to Black		25.08	26.40	27.72	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		1.48	2.16	2.84	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level on IOG		9.44	11.44	13.44	mA
Blank Level on IOR, IOB		0	5	50	µA
Sync Level on IOG		0	5	50	µA
LSB Size			103.5		µA
DAC-to-DAC Matching				5	%
Output Compliance	VOC	-0.5		+1.2	Volts
Output Impedance	RAOUT		50		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		13	20	pF
PLL Analog Output	PLL				
Output Current					
SYNC*/BLANK* = 0		9	11.44	14	mA
SYNC*/BLANK* = 1		0	5	50	µA
Output Compliance		-1.0		+2.5	Volts
Output Impedance			50		kΩ
Output Capacitance (f = 1 MHz, PLL = 0 mA)			10		pF
Voltage Reference Input Current	IREF		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.5		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 348 Ω, VREF = 1.235 V. SETUP = 7.5 IRE with 50 Ω double termination. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	200 MHz Devices			170 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Rate	Fmax			200			170	MHz
LD* Rate	LDmax			25			21.25	MHz
R/W, C0, C1 Setup Time	1	0			0			ns
R/W, C0, C1 Hold Time	2	10			10			ns
CE* Low Time	3	45			45			ns
CE* High Time	4	25			25			ns
CE* Asserted to Data Bus Driven	5	7			7			ns
CE* Asserted to Data Valid	6			45			45	ns
CE* Negated to Data Bus 3-Stated	7			15			15	ns
Write Data Setup Time	8	20			20			ns
Write Data Hold Time	9	0			0			ns
Pixel and Control Setup Time	10	3			3			ns
Pixel and Control Hold Time	11	2			2			ns
Clock Cycle Time	12	5			5.88			ns
Clock Pulse Width High Time	13	2.2			2.5			ns
Clock Pulse Width Low Time	14	2.2			2.5			ns
LD* Cycle Time	15	40			47			ns
LD* Pulse Width High Time	16	15			20			ns
LD* Pulse Width Low Time	17	15			20			ns
Analog Output Delay	18		12			12		ns
Analog Output Rise/Fall Time	19		1			1		ns
Analog Output Settling Time	20			tbd			tbd	ns
Clock and Data Feedthrough*			tbd			tbd		dB
Glitch Impulse*			50			50		pV - sec
DAC to DAC Crosstalk			tbd			tbd		dB
Analog Output Skew			0	1		0	1	ns
Pipeline Delay		6		13	6		13	Clocks
VAA Supply Current**	IAA		450	tbd		430	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 348 Ω, VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are VAA–0.8 to VAA–1.8 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 75 pF. See timing notes in Figure 15. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the TTL digital inputs have a 1 kΩ resistor to GND and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**at Fmax. IAA (typ) at VAA = 5.0 V, TA = 25° C. IAA (max) at VAA = 5.25 V, TA = 0° C.

Timing Waveforms

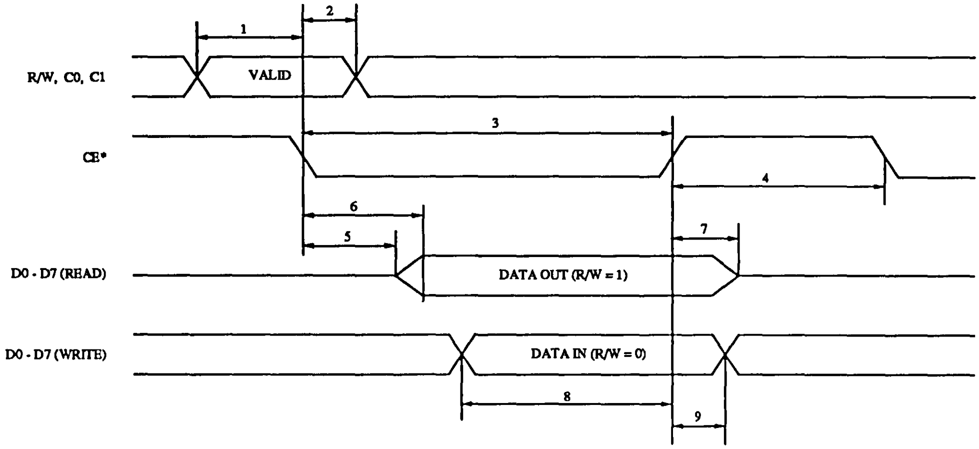
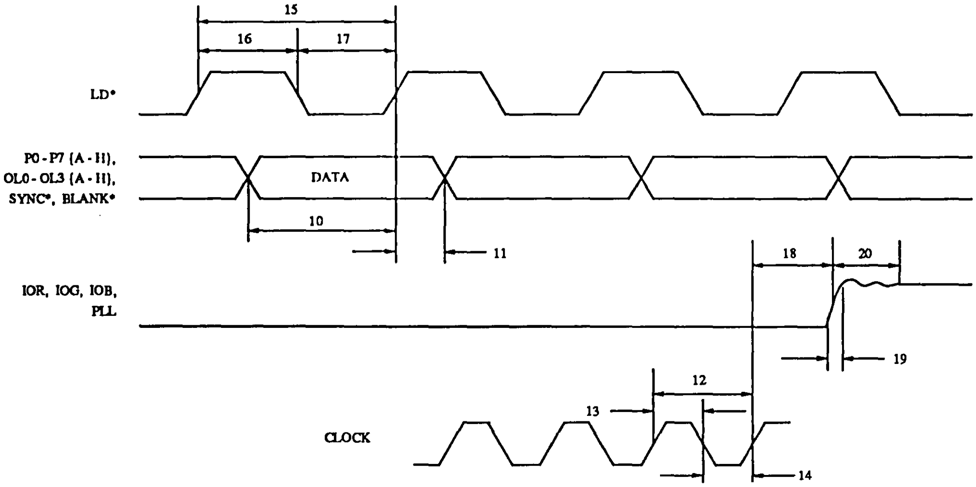

R/W, C0, C1
VALID
CE*
D0 - D7 (READ)
DATA OUT (R/W = 1)
D0 - D7 (WRITE)
DATA IN (R/W = 0)
1
2
3
4
5
6
7
8
9

Figure 14. MPU Read/Write Timing Dimensions.


LD*
P0 - P7 {A - H},
OL0 - OL3 {A - H},
SYNC*, BLANK*
DATA
IOR, IOG, IOB,
PLL
CLOCK
10
11
12
13
14
15
16
17
18
19
20

Note 1: Output delay time measured from 50% point of the rising clock edge to 50% point of full-scale transition.

Note 2: Output settling time measured from 50% point of full scale transition to output settling within ±1 LSB.

Note 3: Output rise/fall time measured between 10% and 90% points of full-scale transition.

Figure 15. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt468KG200	200 MHz	145-pin Ceramic PGA	0° to +70° C
Bt468KG170	170 MHz	145-pin Ceramic PGA	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
B	Full datasheet.
C	Cursor position panning, RSET value changed to match 50 Ω termination. Analog output DC parametrics.
D	Added double reset, modified PLL feedback circuitry.

Bt471
Bt476
Bt478

80 MHz
256 Color Palette
Personal System/2®
RAMDAC™

Distinguishing Features

- Personal System/2® Compatible
- 80, 66, 50, 35 MHz Operation
- Triple 6-bit or 8-bit D/A Converters
- 256-word Color Palette RAM
- RS-343A/RS-170-Compatible Outputs
- 15 Overlay Registers (Bt471/478)
- Sync on All Three Channels (Bt471/478)
- Programmable Pedestal (Bt471/478)
- External Voltage or Current Reference
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 44-pin PLCC or 28-pin DIP Package

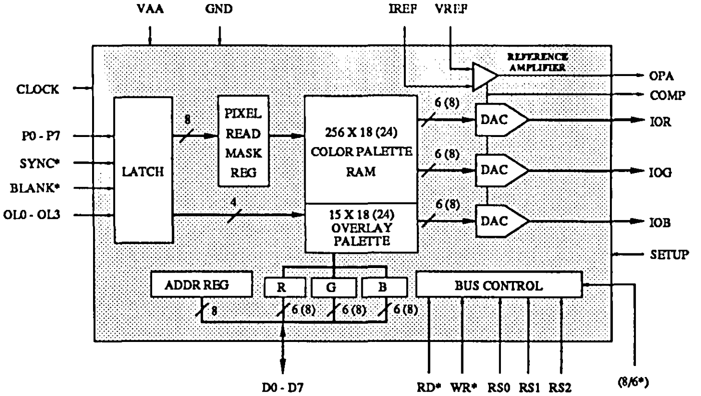
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Related Products

- Bt473, Bt477, Bt479
- Bt474, Bt475

Functional Block Diagram


VAA
GND
IREF
VREF
REFERENCE AMPLIFIER
CLOCK
P0 - P7
SYNC*
BLANK*
OL0 - OL3
LATCH
8
PIXEL READ MASK REG
256 X 18 (24) COLOR PALETTE RAM
4
15 X 18 (24) OVERLAY PALETTE
6 (8)
6 (8)
6 (8)
DAC
DAC
DAC
OPA
COMP
IOR
IOG
IOB
SETUP
ADDR REG
R
G
B
BUS CONTROL
8
6 (8)
6 (8)
6 (8)
D0 - D7
RD*
WR*
RS0
RS1
RS2
(8/6*)

Product Description

The Bt471/476/478 are pin-compatible and software-compatible RAMDACs designed specifically for Personal System/2® compatible color graphics. The Bt476 is also available in a 28-pin DIP package that is pin compatible with the IMS® G176.

The Bt471 has a 256 x 18 color lookup table with triple 6-bit video D/A converters. The Bt478 has a 256 x 24 color lookup table with triple 8-bit video D/A converters. It may be configured for either 6-bit or 8-bit D/A converter operation. The Bt476 is similar to the Bt471, but has no overlays, no programmable setup, or sync information on the analog outputs.

Additional features on the Bt471 and Bt478 include 15 overlay registers to provide for overlaying cursors, grids, menus, EGA emulation, etc. Also supported is sync generation on all three channels, a programmable pedestal (0 or 7.5 IRE), and use of either an external voltage or current reference.

The Bt471/476/478 generates RS-343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering.

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Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L478001 Rev. O

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt471/476/478 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU loads the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (18-bit word for the Bt471/476) and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written. (See Figure 7.)

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU loads the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word (18-bit word for the Bt471/476) and written to the overlay location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAM
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	reserved

Table 1. Control Input Truth Table.

Circuit Description (continued)

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the 4 most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. Occasional accesses to the color palette RAM can be made without noticeable disturbance on the display screen; however, operations requiring frequent access to the color palette (i.e., block fills of the color palette) should be done during the blanking interval.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00				red value
	01				green value
	10				blue value
ADDR0 - 7 (counts binary)	$00 - $FF	0	0	1	color palette RAM
	xxxx 0000	1	0	1	reserved
	xxxx 0001	1	0	1	overlay color 1
	:	:	:	:	:
	xxxx 1111	1	0	1	overlay color 15

Table 2. Address Register (ADDR) Operation.

Circuit Description (continued)

Bt471/476 Data Bus Interface

Color data is contained on the lower 6 bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

Bt478 Data Bus Interface

On the Bt478, the 8/6* control input is used to specify whether the MPU is reading and writing 8 bits (8/6* = logical one) or 6 bits (8/6* = logical zero) of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation (and also when using the Bt471/476), color data is contained on the lower 6 bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

Note that in the 6-bit mode, the Bt478's full-scale output current will be about 1.5% lower than when in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being a logical zero in the 6-bit mode.

Frame Buffer Interface

The P0–P7 and OL0–OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table 3. The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 24 bits (18 bits for the Bt471/476) of color information to the three D/A converters.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 1, 2, and 3. Tables 4, 5, and 6 detail how the SYNC* and BLANK* inputs modify the output levels.

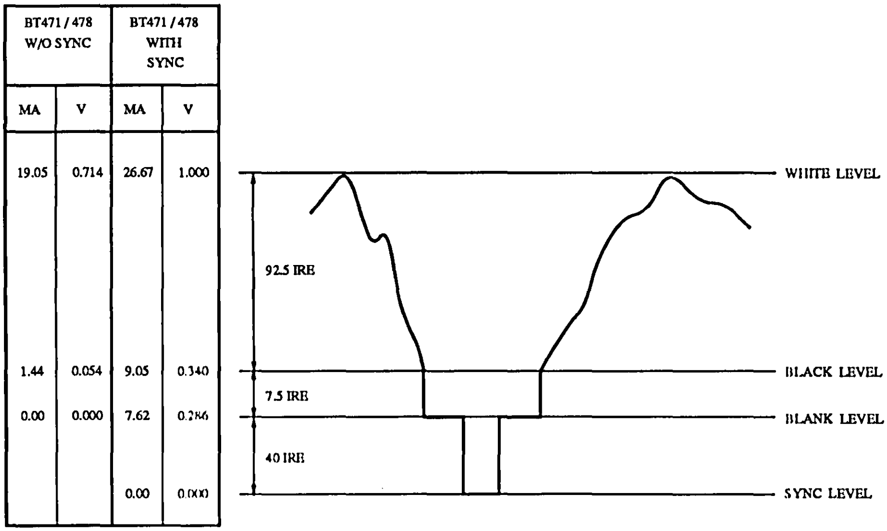
The SETUP input is used to specify whether a 0 IRE (SETUP = GND) or 7.5 IRE (SETUP = VAA) blanking pedestal is to be used. Note that the Bt476 generates only a 0 IRE blanking pedestal (Figures 2 and 3).

The analog outputs of the Bt471/476/478 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

OL0–OL3	P0–P7	Addressed by frame buffer
$0	$00	color palette RAM location $00
$0	$01	color palette RAM location $01
:	:	:
$0	$FF	color palette RAM location $FF
$1	$xx	overlay color 1
:	$xx	:
$F	$xx	overlay color 15

Table 3. Pixel and Overlay Control Truth Table (Pixel Read Mask Register = $FF).

Circuit Description (continued)


BT471 / 478 W/O SYNC
BT471 / 478 WITH SYNC
MA
V
MA
V
19.05
0.714
26.67
1.000
1.44
0.054
9.05
0.340
0.00
0.000
7.62
0.286
0.00
0.000
WHITE LEVEL
92.5 IRE
BLACK LEVEL
7.5 IRE
BLANK LEVEL
40 IRE
SYNC LEVEL

Note: 75 Ω doubly terminated load, SETUP = 7.5 IRE. VREF = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

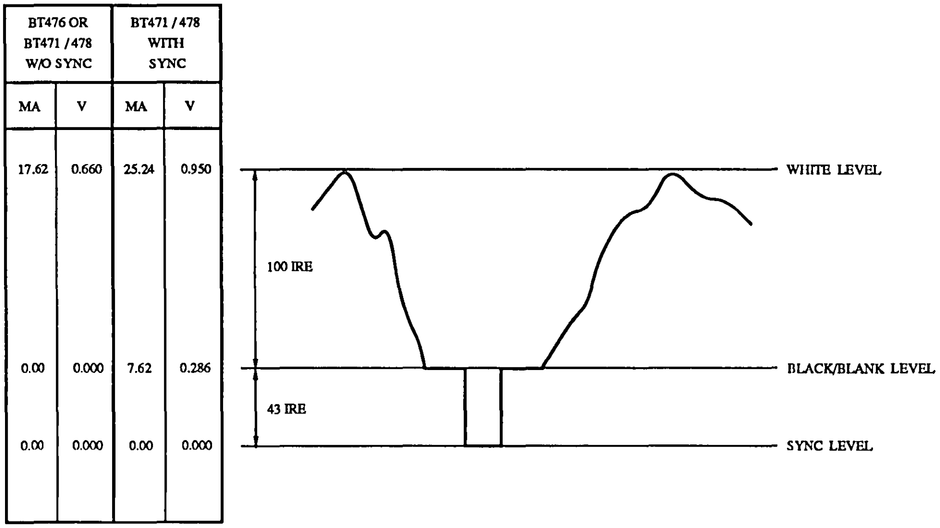
Figure 1. RS-343A Composite Video Output Waveforms (SETUP = 7.5 IRE).

Description	Bt471/478 Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	0	1	data
BLACK	9.05	1	1	$00
BLACK - SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: 75 Ω doubly terminated load, SETUP = 7.5 IRE. VREF = 1.235 V, RSET = 147 Ω.

Table 4. RS-343A Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)



BT476 OR BT471 / 478 W/O SYNC		BT471 / 478 WITH SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000

Note: 75 Ω doubly terminated load, SETUP = 0 IRE. VREF = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

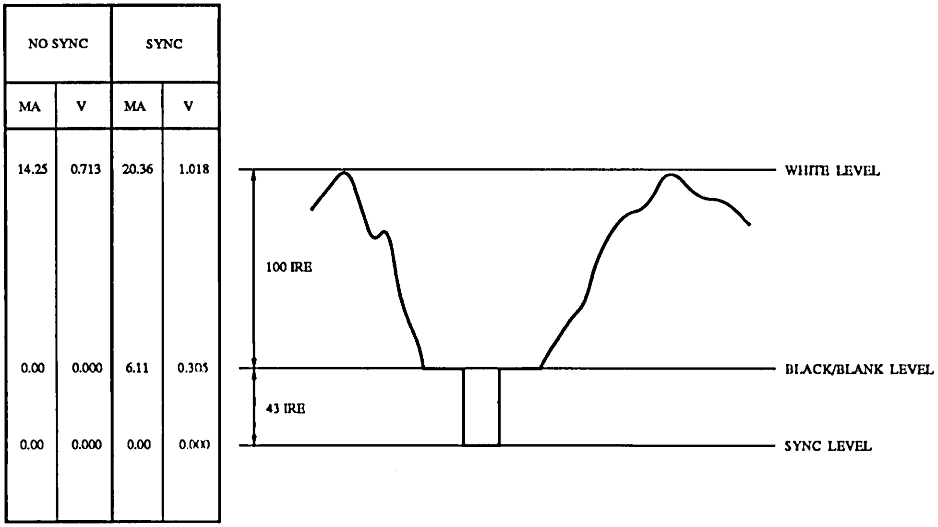
Figure 2. RS-343A Composite Video Output Waveforms. (SETUP = 0 IRE)

Description	Bt476	Bt471/478	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly terminated load, SETUP = 0 IRE. VREF = 1.235 V, RSET = 147 Ω.

Table 5. RS-343A Video Output Truth Table (SETUP = 0 IRE).

Circuit Description (continued)



NO SYNC		SYNC	
MA	V	MA	V
14.25	0.713	20.36	1.018
0.00	0.000	6.11	0.305
0.00	0.000	0.00	0.000

Note: 50 Ω load, SETUP = 0 IRE. VREF = 1.235 V, RSET = 182 Ω. PS/2 levels and tolerances assumed on all levels.

Figure 3. PS/2 Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	14.25	20.36	1	1	$FF
DATA	data	data + 6.11	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	6.11	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	6.11	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 50 Ω load, SETUP = 0 IRE. VREF = 1.235 V, RSET = 182 Ω.

Table 6. PS/2 Video Output Truth Table (SETUP = 0 IRE).

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 4, 5 and 6. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input (TTL compatible). Used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal. This pin should not be left floating.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 1, 2, and 3). SYNC* does not override any other control or data input, as shown in Tables 4, 5, and 6; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not required on the video outputs, SYNC* should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0–OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0–OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 3. When accessing the overlay palette, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
COMP	Compensation pin. If an external voltage reference is used (Figure 4), this pin should be connected to OPA. If an external current reference is used (Figure 5), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *Refer to PC Board Layout Considerations for critical layout criteria.*
VREF	Voltage reference input. If an external voltage reference is used (Figure 4), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 5), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor is used to decouple this input to GND, as shown in Figures 4. If the VAA supply is very clean, better performance may be obtained by decoupling VREF to VAA. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
OPA	Reference amplifier output. If an external voltage reference is used (Figure 4), this pin must be connected to COMP. When using an external current reference (Figure 5), this pin should be left floating.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figures 4, 5, and 6).
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)

Pin Name	Description
IREF	Full-scale adjust control. Note that the IRE relationships in Figures 1, 2, and 3 are maintained, regardless of the full-scale output current.

When using an external voltage reference (Figure 4), a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is:

$$RSET\ (\Omega) = K * 1{,}000 * VREF\ (V) / Iout\ (mA)$$

K is defined in the table below. It is recommended that a 147 Ω RSET resistor be used for doubly-terminated 75 Ω loads (i.e., RS-343A applications). For PS/2 applications (i.e., 0.7 V into 50 Ω with no sync), a 182 Ω RSET resistor is recommended.

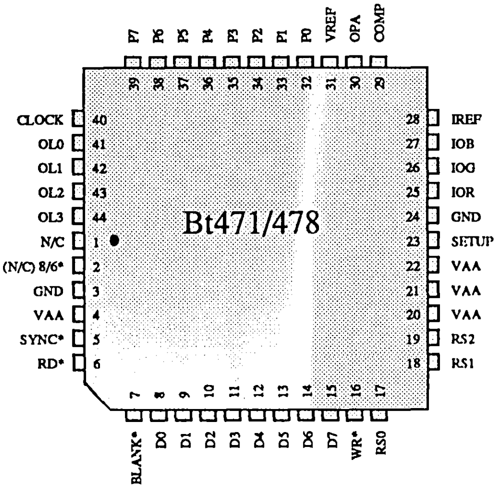
When using an external current reference (Figures 5 and 6), the relationship between IREF and the full-scale output current on each output is:

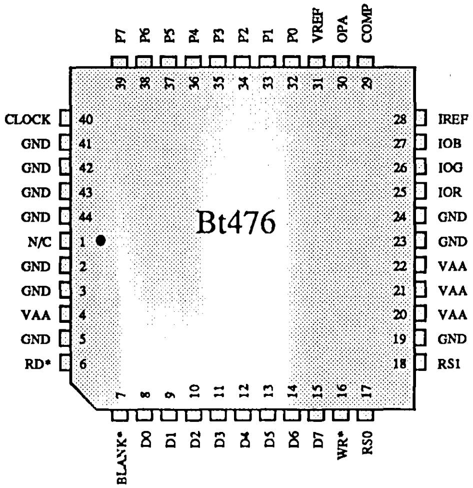
$$IREF\ (mA) = Iout\ (mA) / K$$

Part	Mode	Pedestal	K (with sync)	K (no sync)
Bt478	6-bit	7.5 IRE	3.170	2.26
	8-bit	7.5 IRE	3.195	2.28
	6-bit	0 IRE	3.000	2.10
	8-bit	0 IRE	3.025	2.12
Bt471	(6-bit)	7.5 IRE	3.170	2.26
		0 IRE	3.000	2.10
Bt476	(6-bit)	0 IRE	3.000	2.10

Pin Name	Description
WR*	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously.
RD*	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as illustrated in Tables 1 and 2.
D0 - D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
8/6*	8-bit/6-bit select input (TTL compatible). This bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles (D6 and D7 are ignored during color write cycles and a logical zero during color read cycles). Note: this pin should be connected to GND when using the Bt476.

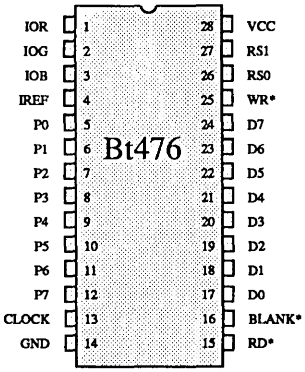
Pin Descriptions (continued)—44-Pin Plastic J-Lead (PLCC)


Bt471/478
P7 39
P6 38
P5 37
P4 36
P3 35
P2 34
P1 33
P0 32
VREF 31
OPA 30
COMP 29
CLOCK 40
OL0 41
OL1 42
OL2 43
OL3 44
N/C 1
(N/C) 8/6* 2
GND 3
VAA 4
SYNC* 5
RD* 6
28 IREF
27 IOB
26 IOG
25 IOR
24 GND
23 SETUP
22 VAA
21 VAA
20 VAA
19 RS2
18 RS1
7 BLANK*
8 D0
9 D1
10 D2
11 D3
12 D4
13 D5
14 D6
15 D7
16 WR*
17 RS0


Bt476
P7 39
P6 38
P5 37
P4 36
P3 35
P2 34
P1 33
P0 32
VREF 31
OPA 30
COMP 29
CLOCK 40
GND 41
GND 42
GND 43
GND 44
N/C 1
GND 2
GND 3
VAA 4
GND 5
RD* 6
28 IREF
27 IOB
26 IOG
25 IOR
24 GND
23 GND
22 VAA
21 VAA
20 VAA
19 GND
18 RS1
7 BLANK*
8 D0
9 D1
10 D2
11 D3
12 D4
13 D5
14 D6
15 D7
16 WR*
17 RS0

Names in parentheses are pin names for the Bt471.
N/C pins may be left unconnected without affecting the performance of the Bt471/476/478.

Pin Descriptions—28-Pin DIP


Bt476
IOR 1
IOG 2
IOB 3
IREF 4
P0 5
P1 6
P2 7
P3 8
P4 9
P5 10
P6 11
P7 12
CLOCK 13
GND 14
28 VCC
27 RS1
26 RS0
25 WR*
24 D7
23 D6
22 D5
21 D4
20 D3
19 D2
18 D1
17 D0
16 BLANK*
15 RD*

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in *Bt451/7/8 Evaluation Module Operation and Measurements,* application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt471/476/478 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a four-layer PC board is recommended with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

The optimum layout enables the Bt471/476/478 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8-inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground tub isolation technique is constrained by the noise margin degradation during digital readback of the Bt471/476/478.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

The analog ground plane should include all Bt471/476/478 ground pins, all reference circuitry and decoupling (external reference if used, RSET resistors, etc.), power supply bypass circuitry for the Bt471/476/478, analog output traces, and the video output connector.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt471/476/478 power pins, any reference circuitry, and COMP and reference decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 4, 5, and 6. This bead should be located within 3 inches of the Bt471/476/478 and provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.001 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device.

The 10 µF capacitor is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic chip capacitor. Low-frequency supply noise will require a larger value. Lead lengths should be minimized for best performance.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt471/476/478 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt471/476/478 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt471/476/478 to minimize reflections. Unused analog outputs should be connected to GND.

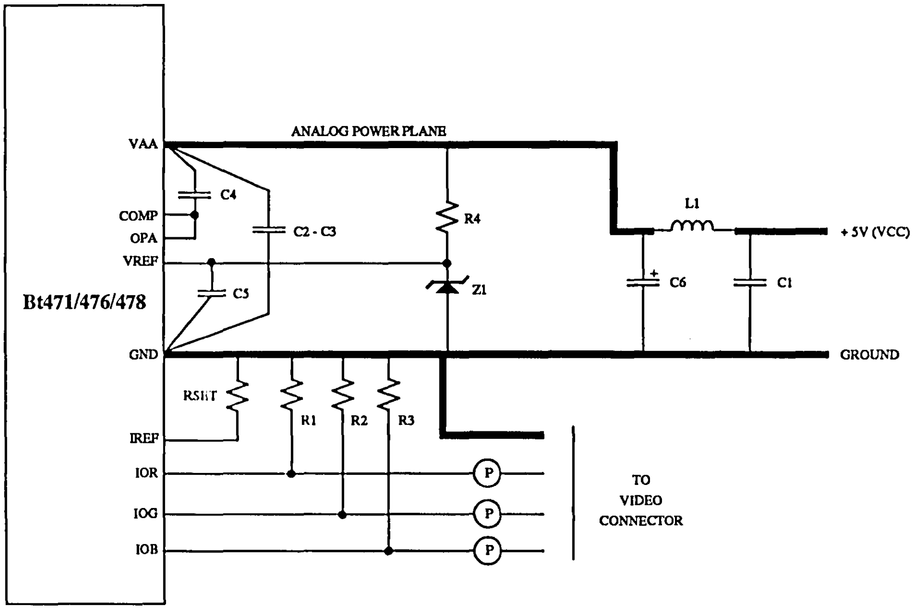
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

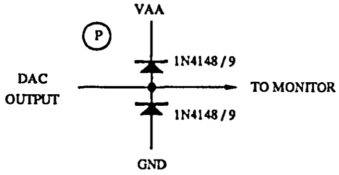
Analog Output Protection

The Bt471/476/478 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figures 4, 5, and 6 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued) — 44-Pin Plastic J-Lead (PLCC)


ANALOG POWER PLANE
VAA
COMP
OPA
VREF
Bt471/476/478
GND
IREF
IOR
IOG
IOB
C4
C2 - C3
C5
R4
Z1
L1
+5V (VCC)
C6
C1
GROUND
RSET
R1
R2
R3
P
P
P
TO
VIDEO
CONNECTOR

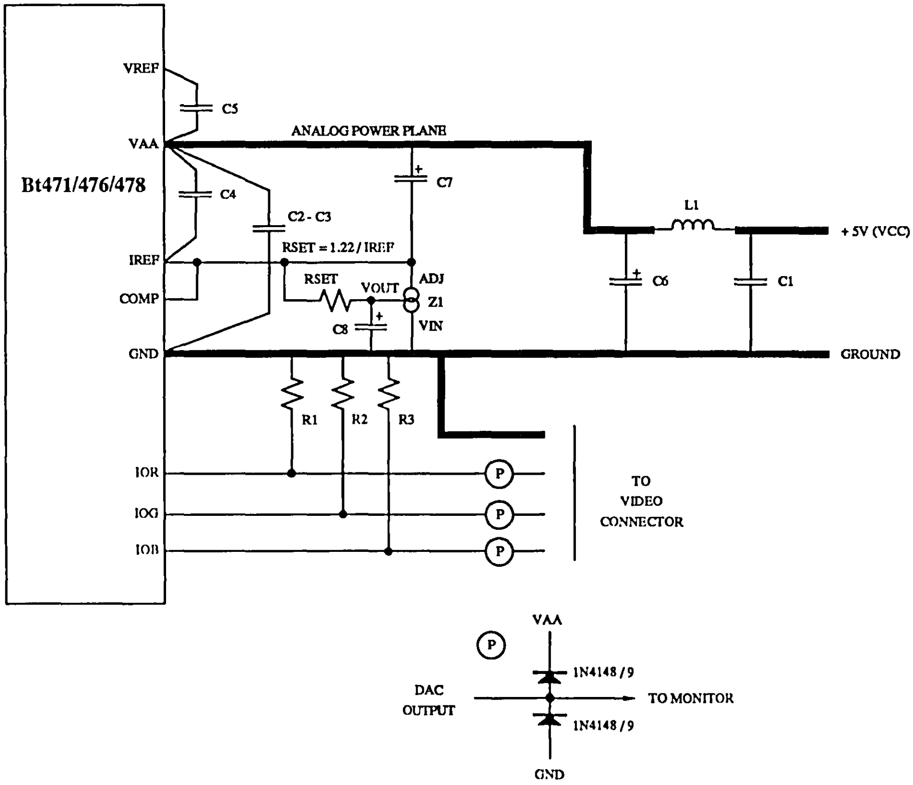

VAA
P
1N4148/9
DAC
OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt471/476/478.

Figure 4. Typical Connection Diagram and Parts List (External Voltage Reference).

PC Board Layout Considerations (continued) — 44-Pin Plastic J-Lead (PLCC)

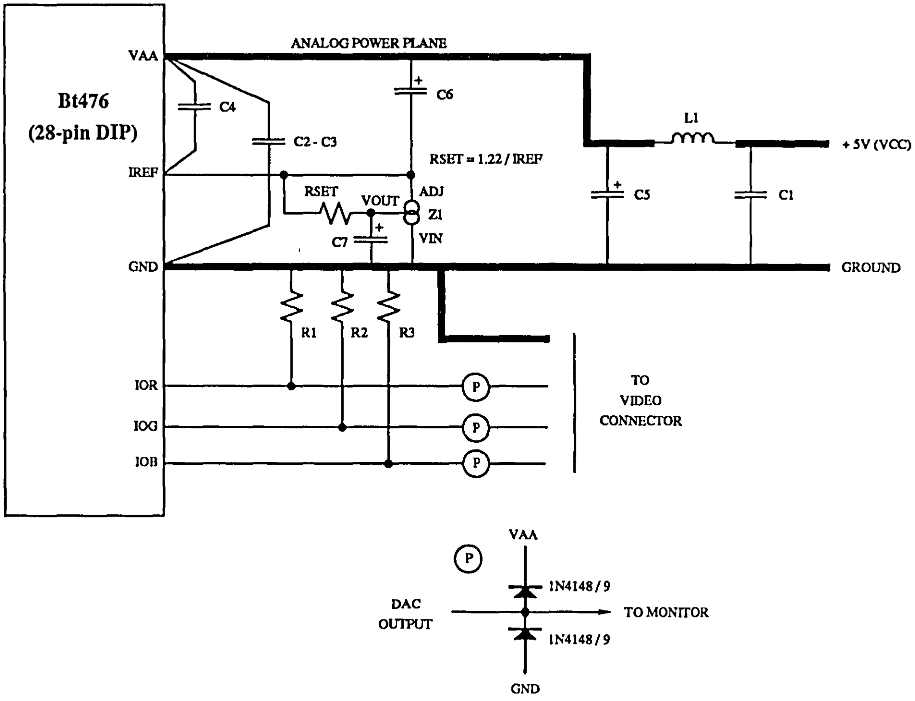

VREF
VAA
Bt471/476/478
IREF
COMP
GND
IOR
IOG
IOB
C5
C4
C2 - C3
C7
C8
C6
C1
ANALOG POWER PLANE
L1
+5V (VCC)
GROUND
RSET = 1.22 / IREF
RSET
VOUT
ADJ
Z1
VIN
R1
R2
R3
P
TO VIDEO CONNECTOR
VAA
1N4148/9
DAC OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description	Vendor Part Number
C1 - C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
C7, C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt471/476/478.

Figure 5. Typical Connection Diagram and Parts List (External Current Reference).

PC Board Layout Considerations (continued) — 28-Pin DIP


Bt476
(28-pin DIP)
VAA
IREF
GND
IOR
IOG
IOB
ANALOG POWER PLANE
C4
C2 - C3
C6
RSET = 1.22 / IREF
RSET
VOUT
ADJ
Z1
VIN
C7
L1
+5V (VCC)
C5
C1
GROUND
R1
R2
R3
P
TO VIDEO CONNECTOR
VAA
1N4148/9
DAC OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description	Vendor Part Number
C1–C4	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C5	10 µF capacitor	Mallory CSR13G106KM
C6, C7	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rité 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt476.

Figure 6. Typical Connection Diagram and Parts List (External Current Reference).

Application Information

Using Multiple Devices

When using multiple RAMDACs, each RAMDAC should have its own power plane ferrite bead. In addition, a single reference may drive multiple devices; however, isolation resistors are recommended to reduce color channel crosstalk.

Higher performance is obtained if each RAMDAC has its own reference. This may further reduce the amount of color channel crosstalk and color palette interaction.

Each RAMDAC must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

Reference Selection

An external voltage reference provides about 10x better power supply rejection on the analog outputs than an external current reference.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
80, 66 MHz Parts		4.75	5.00	5.25	Volts
50, 35 MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ohms
Voltage Reference Configuration					
Reference Voltage	VREF	1.14	1.235	1.26	Volts
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		–3	–8.39	–10	mA
PS/2 Compatible		–3	–8.88	–10	mA

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)					
Bt478		8	8	8	Bits
Bt471/476		6	6	6	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL				
Bt478				±1	LSB
Bt476				±1/2	LSB
Bt471				±1/4	LSB
Differential Linearity Error	DL				
Bt478				±1	LSB
Bt476				±1/2	LSB
Bt471				±1/4	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black*		16.74	17.62	18.50	mA
Black Level Relative to Blank					
Bt471/478					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Bt476		0	0	0	µA
Blank Level					
Bt471/478		6.29	7.62	8.96	mA
Bt476		0	5	50	µA
Sync Level (Bt471/478 only)		0	5	50	µA
LSB Size					
Bt478 (8/6* = logical one)			69.1		µA
Bt471/476			279.68		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	-1.0		+1.5	Volts
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Voltage Reference Input Current	IVREF		10		µA
Power Supply Rejection Ratio** (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, 8/6* = logical one. For 28-pin DIP version of the Bt476, IREF = –8.39 mA. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room and nominal voltage, i.e., 5 V.

*Since the Bt471 and Bt476 have 6-bit DACs (and the Bt478 in the 6-bit mode), the output levels are approximately 1.5% lower than these values.

**Guaranteed by characterization, not tested.

Analog Output Levels — PS/2 Compatibility

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
Bt471/478					
SETUP = 7.5 IRE		1.01	1.51	2.0	mA
SETUP = 0 IRE		0	5	50	µA
Bt476		0	5	50	µA
Blank Level					
Bt471/478		6.6	8	9.4	mA
Bt476		0	5	50	µA
Sync Level (Bt471/478 only)		0	5	50	µA

Test conditions to generate PS/2 compatible video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, 8/6* = logical one. For 28-pin DIP version of the Bt476, IREF = –8.88 mA.

AC Characteristics

Parameter	Symbol	80 MHz Devices			66 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	
Clock Rate	Fmax			80			66	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*p13			6*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	12.5			15.15			ns
Clock Pulse Width High Time	14	4			5			ns
Clock Pulse Width Low Time	15	4			5			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		13			13		ns
Clock and Data Feedthrough*			-30			-30		dB
Glitch Impulse*			75			75		pV - sec
DAC-to-DAC Crosstalk			-3			-23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA		180	220		180	220	mA

See test conditions on next page.

AC Characteristics (continued)

		50 MHz Devices			35 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			50			35	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*p13			6*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	20			28			ns
Clock Pulse Width High Time	14	6			7			ns
Clock Pulse Width Low Time	15	6			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		20			28		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			75			75		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
Average VAA Supply Current**	IAA		180	220		180	220	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, 8/6* = logical one. For 28-pin DIP version of the Bt476, IREF = –8.39 mA. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 75 pF. See timing notes in Figure 8. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**at Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA (max).

Timing Waveforms

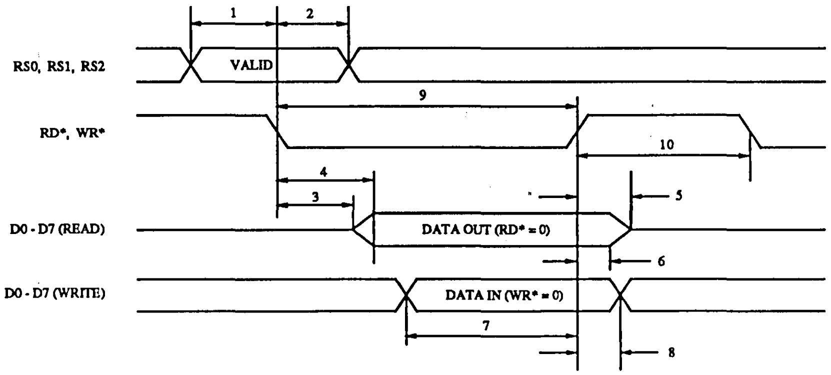
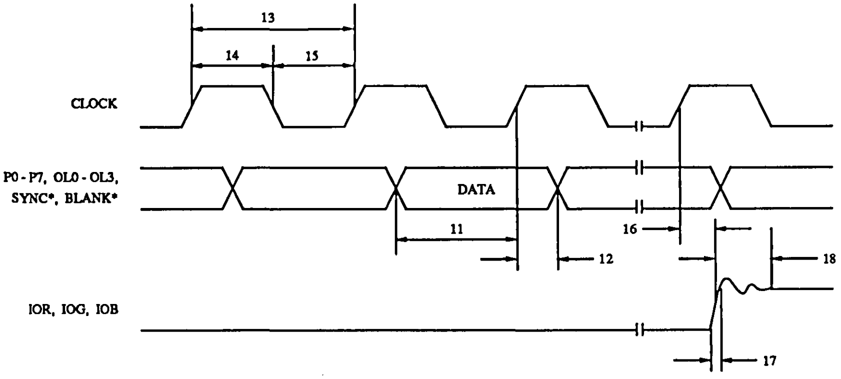

1
2
RS0, RS1, RS2
VALID
9
RD*, WR*
10
4
3
5
D0 - D7 (READ)
DATA OUT (RD* = 0)
6
D0 - D7 (WRITE)
DATA IN (WR* = 0)
7
8

Figure 7. MPU Read/Write Timing Dimensions.


13
14
15
CLOCK
P0 - P7, OL0 - OL3,
SYNC*, BLANK*
DATA
11
16
12
18
IOR, IOG, IOB
17

Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB (Bt478), ±1/4 LSB (Bt471), or ±1/2 LSB (Bt476).

Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 8. Video Input/Output Timing.

Ordering Information

Model Number	Color Palette RAM	Overlay Palette	Sync Generation	Speed	Package	Ambient Temperature Range
Bt471KPJ80	256 x 18	15 x 18	yes	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt471KPJ66	256 x 18	15 x 18	yes	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt471KPJ50	256 x 18	15 x 18	yes	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt471KPJ35	256 x 18	15 x 18	yes	35 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt476KPJ66	256 x 18	-	no	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt476KPJ50	256 x 18	-	no	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt476KPJ35	256 x 18	-	no	35 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt476KP66	256 x 18	-	no	66 MHz	28-pin 0.6" Plastic DIP	0° to +70° C
Bt476KP50	256 x 18	-	no	50 MHz	28-pin 0.6" Plastic DIP	0° to +70° C
Bt476KP35	256 x 18	-	no	35 MHz	28-pin 0.6" Plastic DIP	0° to +70° C
Bt478KPJ80	256 x 24	15 x 24	yes	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt478KPJ66	256 x 24	15 x 24	yes	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt478KPJ50	256 x 24	15 x 24	yes	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt478KPJ35	256 x 24	15 x 24	yes	35 MHz	44-pin Plastic J-Lead	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
N	Expanded PC Board Layout section.
O	Changed VREF decoupling from VAA to GND for external voltage reference PCB layout. Added ESD/latchup information.

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt473

80 MHz
Monolithic CMOS
Triple 8-bit
True-Color RAMDAC™

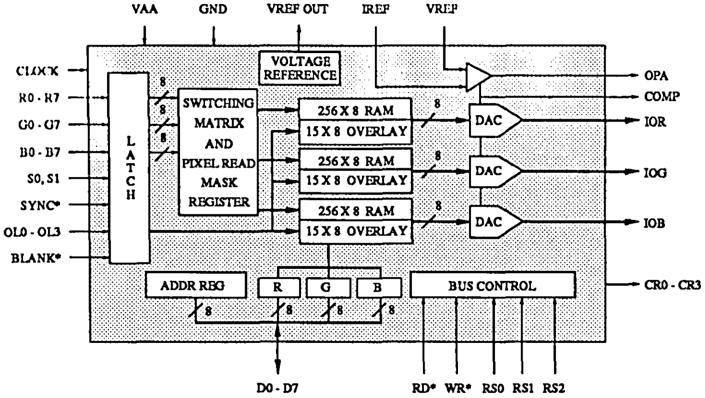
Distinguishing Features

- Bt471/478 Software Compatible
- 80, 66, 50, 35 MHz Operation
- Triple 8-bit D/A Converters
- Three 256 x 8 Color Palette RAMs
- Three 15 x 8 Overlay Registers
- RS-343A/RS-170 Compatible Outputs
- Sync on All Three Channels
- Programmable Pedestal (0 or 7.5 IRE)
- On-Chip Voltage Reference
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 68-pin PLCC Package
- Typical Power Dissipation: 900 mW

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Functional Block Diagram


VAA
GND
VREF OUT
IREF
VREF
CLOCK
R0 - R7
G0 - G7
B0 - B7
S0, S1
SYNC*
OL0 - OL3
BLANK*
LATCH
8
8
8
VOLTAGE REFERENCE
SWITCHING MATRIX AND PIXEL READ MASK REGISTER
256 X 8 RAM
15 X 8 OVERLAY
256 X 8 RAM
15 X 8 OVERLAY
256 X 8 RAM
15 X 8 OVERLAY
8
8
8
DAC
DAC
DAC
OPA
COMP
IOR
IOG
IOB
CR0 - CR3
ADDR REG
R
G
B
BUS CONTROL
8
8
8
8
D0 - D7
RD*
WR*
RS0
RS1
RS2

Product Description

The Bt473 true-color RAMDAC is designed specifically for true-color computer graphics. It has three 256 x 8 color lookup tables with triple 8-bit video D/A converters to support 24-bit true-color operation. In addition, 8-bit pseudo-color, 8-bit true-color, and 15-bit true-color operations are supported.

Features include a programmable pedestal (0 or 7.5 IRE) and optional on-chip voltage reference. The 15 overlay registers provide for overlaying cursors, grids, menus, EGA emulation, etc. Also supported are a pixel read mask register and sync generation on all three channels.

Either an external current reference, an external voltage reference, or the internal voltage reference may be used.

The Bt473 generates RS-343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering. Differential and integral linearity errors are guaranteed to be a maximum of ±1 LSB over the full temperature range.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L473001 Rev. H

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt473 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the overlay location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (8 bits each of

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAMs
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	command register

Table 1. Control Input Truth Table.

Circuit Description (continued)

red, green, and blue), using RS0–RS2 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the 4 most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. Occasional accesses to the color palette RAM can be made without noticeable disturbance on the display screen; however, operations requiring frequent access to the color palette (i.e., block fills of the color palette) should be done during the blanking interval.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register, incremented following a blue read or write cycle (ADDR0–7), are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

8-Bit / 6-Bit Operation

The command register specifies whether the MPU is reading and writing 8 bits or 6 bits of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero. Note that in the 6-bit mode, the Bt473's full-scale output current will be about 1.5% lower than when in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being a logical zero in the 6-bit mode.

Color Modes

Four color modes are supported by the Bt473: 24-bit true color, 15-bit true color, 8-bit true color, and 8-bit pseudo color. The mode of operation is determined by the S0 and S1 inputs, in conjunction with CR7 and CR6 of the command register. S0 and S1 are pipelined to maintain synchronization with the R0–R7, G0–G7, B0–B7, and OL0–OL3 pixel and overlay data inputs.

Table 3 lists the modes of operation.

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10	x x x	0 0 0	1 1 1	red value green value blue value
ADDR0 - 7 (counts binary)	$00 - $FF xxxx 0000 xxxx 0001 : xxxx 1111	0 1 1 : 1	0 0 0 : 0	1 1 1 : 1	color palette RAMs reserved overlay color 1 : overlay color 15

Table 2. Address Register (ADDR) Operation.

Circuit Description (continued)

OL3–OL0	S1, S0	CR7, CR6	Mode	R7–R0	G7–G0	B7–B0
1111	xx	xx	overlay color 15	$xx	$xx	$xx
:	:	:	:	:	:	:
0001	xx	xx	overlay color 1	$xx	$xx	$xx
0000	00	00	24-bit true color	R7–R0	G7–G0	B7–B0
0000	00	01	24-bit true color	R7–R0	G7–G0	B7–B0
0000	00	10	24-bit true color	R7- R0	G7–G0	B7–B0
0000	00	11	reserved	reserved	reserved	reserved
0000	01	00	24-bit true color bypass	R7–R0	G7–G0	B7–B0
0000	01	01	24-bit true color bypass	R7–R0	G7–G0	B7–B0
0000	01	10	24-bit true color bypass	R7–R0	G7–G0	B7–B0
0000	01	11	reserved	reserved	reserved	reserved
0000	10	00	8-bit pseudo color (red)	P7–P0	ignored	ignored
0000	10	01	8-bit pseudo color (green)	ignored	P7–P0	ignored
0000	10	10	8-bit pseudo color (blue)	ignored	ignored	P7–P0
0000	10	11	reserved	reserved	reserved	reserved
0000	11	00	8-bit true-color bypass (red)	rrrgggbb	ignored	ignored
0000	11	01	8-bit true-color bypass (green)	ignored	rrrgggbb	ignored
0000	11	10	8-bit true-color bypass (blue)	ignored	ignored	rrrgggbb
0000	11	11	15-bit true-color bypass	0rrrrrgg	gggbbbbb	ignored

Table 3. Color Operation Modes.

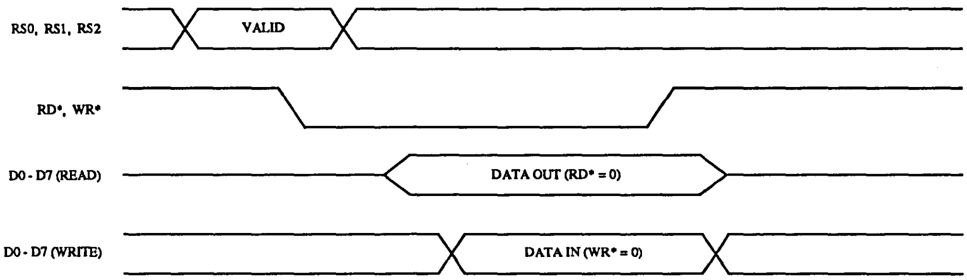


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

24-Bit True-Color Mode

Twenty-four bits of RGB color information may be input into the Bt473 every clock cycle. The 24 bits of pixel information are input via the R0–R7, G0–G7, and B0–B7 inputs. R0–R7 address the red color palette RAM, G0–G7 address the green color palette RAM, and B0–B7 address the blue color palette RAM. Each RAM provides 8 bits of color information to the corresponding D/A converter. The pixel read mask register is used in this mode.

24-Bit True-Color Bypass Mode

Twenty-four bits of pixel information may be input into the Bt473 every clock cycle. The 24 bits of pixel information are input via the R0–R7, G0–G7, and B0–B7 inputs. R0–R7 drive the red DAC directly, G0–G7 drive the green DAC directly, and B0–B7 drive the blue DAC directly. The color palette RAMs and pixel read mask register are bypassed.

8-Bit Pseudo-Color Mode

Eight bits of pixel information may be input into the Bt473 every clock cycle. The 8 bits of pixel information (P0–P7) are input via the R0–R7, G0–G7 or B0–B7 inputs, as specified by CR7 and CR6. All three color palette RAMs are addressed by the same 8 bits of pixel data (P0–P7). Each RAM provides 8 bits of color information to the corresponding D/A converter. The pixel read mask register is used in this mode.

8-Bit True-Color Bypass Mode

Eight bits of pixel information may be input into the Bt473 every clock cycle. The 8 bits of pixel information are input via the R0–R7, G0–G7 or B0–B7 inputs, as specified by CR7 and CR6:

R0–R7 Inputs Selected	G0–G7 Inputs Selected	B0–B7 Inputs Selected	Input Format
R7	G7	B7	R7
R6	G6	B6	R6
R5	G5	B5	R5
R4	G4	B4	G7
R3	G3	B3	G6
R2	G2	B2	G5
R1	G1	B1	B7
R0	G0	B0	B6

As seen in the table, 3 bits of red, 3 bits of green, and 2 bits of blue data are input. The 3 MSBs of the red and green DACs are driven directly by the inputs, while the 2 MSBs of the blue DAC are driven directly. The 5 LSBs for the red and green DACs, and the 6 LSBs for the blue DAC, are a logical zero. The color palette RAMs and pixel read mask register are bypassed.

15-Bit True-Color Bypass Mode

Fifteen bits of pixel information may be input into the Bt473 every clock cycle. The 15 bits of pixel information (5 bits of red, 5 bits of green, and 5 bits of blue) are input via the R0–R7 and G0–G7 inputs:

Pixel Inputs	Input Format
R7	0
R6	R7
R5	R6
R4	R5
R3	R4
R2	R3
R1	G7
R0	G6
G7	G5
G6	G4
G5	G3
G4	B7
G3	B6
G2	B5
G1	B4
G0	B3

The 5 MSBs of the red, green, and blue DACs are driven directly by the inputs. The 3 LSBs are a logical zero. The color palette RAMs and pixel read mask register are bypassed.

Overlays

The overlay inputs, OL0–OL3, have priority regardless of the color mode, as shown in Table 3.

Circuit Description (continued)

Pixel Read Mask Register

The 8-bit pixel read mask register is implemented as three 8-bit pixel read mask registers, one each for the R0–R7, G0–G7, and B0–B7 inputs. When writing to the pixel read mask register, the same data is written to all three registers. The read mask registers are located just before the color palette RAMs. Thus, they are used only in the 24-bit true-color and 8-bit pseudo-color modes since these are the only modes that use the color palette RAMs.

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the 8-bit inputs prior to addressing the color palette RAMs. Bit D0 of the pixel read mask register corresponds to pixel input P0 (R0, G0, or B0 depending on the mode). Bit D0 also corresponds to data bus bit D0.

Programmable Setup

The command register specifies whether a 0 IRE or 7.5 IRE blanking pedestal is to be used.

Video Generation

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data (see figure 2), add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 3 and 4. Tables 4 and 5 detail how the SYNC* and BLANK* inputs modify the output levels.

The analog outputs of the Bt473 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

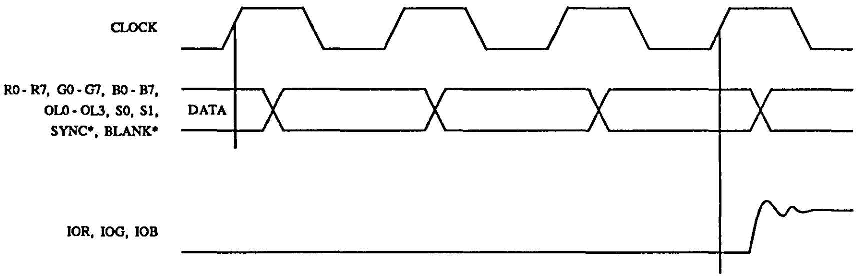
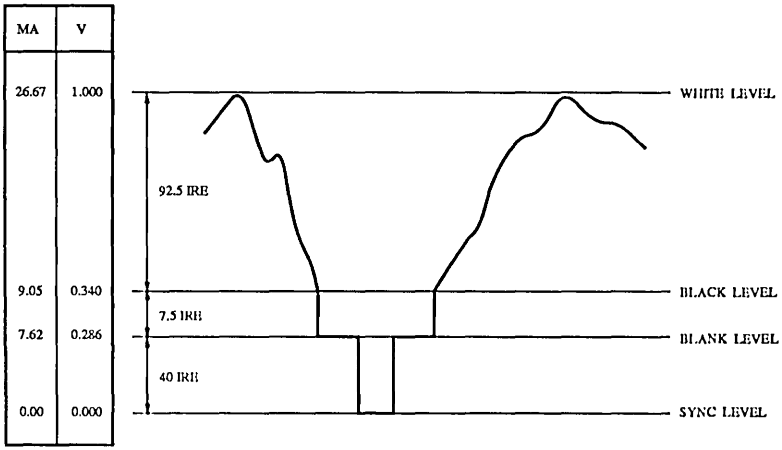


Figure 2. Video Input/Output Timing.

Circuit Description (continued)



Note: 75 Ω doubly terminated load, SETUP = 7.5 IRE, VREF = 1.235 V, RSET = 140 Ω. RS-343A levels and tolerances assumed on all levels.

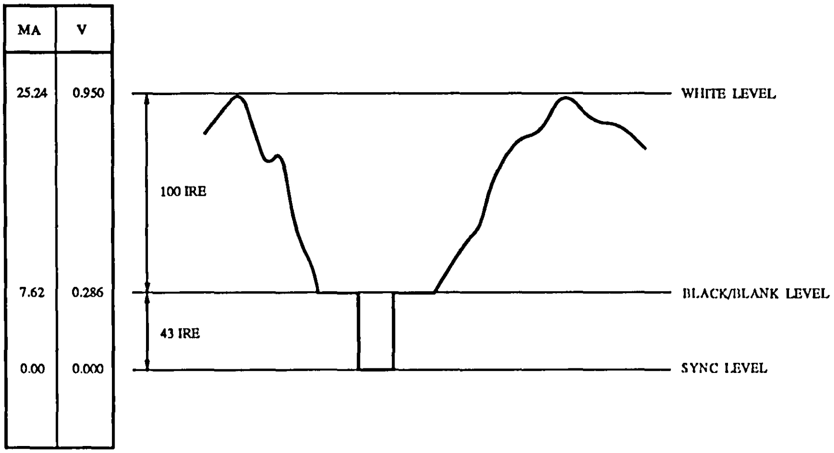
Figure 3. Composite Video Output Waveforms (SETUP = 7.5 IRE).

Description	Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	0	1	data
BLACK	9.05	1	1	$00
BLACK - SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: Typical with full-scale IOR, IOG, IOB = 26.67 mA, SETUP = 7.5 IRE, VREF = 1.235 V, RSET = 140 Ω.

Table 4. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)


MA
V
25.24
0.950
7.62
0.286
0.00
0.000
WHITE LEVEL
100 IRE
BLACK/BLANK LEVEL
43 IRE
SYNC LEVEL

Note: 75 Ω doubly terminated load, SETUP = 0 IRE, VREF = 1.235 V, RSET = 140 Ω. RS-343A levels and tolerances assumed on all levels.

Figure 4. Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	25.24	1	1	$FF
DATA	data + 7.62	1	1	data
DATA - SYNC	data	0	1	data
BLACK	7.62	1	1	$00
BLACK - SYNC	0	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: Typical with full-scale IOR, IOG, IOB = 25.24 mA, SETUP = 0 IRE, VREF = 1.235 V, RSET = 140 Ω.

Table 5. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register

The command register may be written to or read by the MPU at any time, and is not initialized. CR0 is the least significant bit and corresponds to D0.

CR7, CR6	Color mode select	These bits are used to control the various color modes, as shown in Table 3.
CR5	Setup select (0) 0 IRE (1) 7.5 IRE	Used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal.
CR4	8-bit / 6-bit color select (0) 6-bit (1) 8-bit	This bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. For 8-bit operation, D7 is the most significant data bit during color read/write cycles. For 6-bit operation, D5 is the most significant data bit during color read/write cycles (D6 and D7 are ignored during color write cycles and a logical zero during color read cycles).
CR3–CR0	CR3–CR0 outputs	These bits are output onto the CR3–CR0 pins.

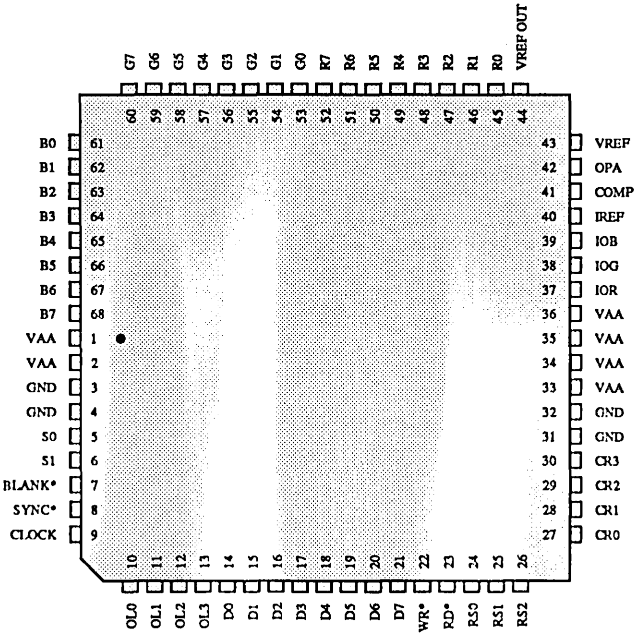
Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 4 and 5. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 3 and 4). SYNC* does not override any other control or data input, as shown in Tables 4 and 5; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not to be generated on the analog outputs, this pin should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, S0, S1, OL0–OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
R0–R7, G0–G7, B0–B7	Red, green, and blue pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the red, green, and blue color palette RAMs is to be used to provide color information. They are latched on the rising edge of CLOCK. R0, G0, and B0 are the LSBs. Unused inputs should be connected to GND.
S0, S1	Color mode select inputs (TTL compatible). These inputs specify the mode of operation as shown in Table 3. They are latched on the rising edge of CLOCK.
OL0–OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 3. When accessing the overlay palette, the R0–R7, G0–G7, B0–B7, S0, and S1 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figures 5, 6, and 7).
IREF	When using a voltage reference (Figures 5 and 6), a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is: for SETUP = 7.5 IRE: RSET (Ω) = 3,195 * VREF (V) / Iout (mA) for SETUP = 0 IRE: RSET (Ω) = 3,025 * VREF (V) / Iout (mA) When using an external current reference (Figure 7), the relationship between IREF and the full-scale output current on each output is: for SETUP = 7.5 IRE: IREF (mA) = Iout (mA) / 3.195 for SETUP = 0 IRE: IREF (mA) = Iout (mA) / 3.025

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. If an external voltage reference is used (Figures 5 and 6), this pin should be connected to OPA. If an external current reference is used (Figure 7), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *Refer to PC Board Layout Considerations for critical layout criteria.*
VREF	Voltage reference input. If a voltage reference is used (Figures 5 and 6), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 7), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor is used to decouple this input to GND, as shown in Figures 5 and 6. If the VAA supply is very clean, better performance may be obtained by decoupling VREF to VAA. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
OPA	Reference amplifier output. If a voltage reference is used (Figures 5 and 6), this pin must be connected to COMP. When using an external current reference (Figure 7), this pin should be left floating.
VREF OUT	Voltage reference output. This output provides a 1.2 V (typical) reference, and may be connected directly to the VREF pin. If the on-chip reference is not used, this pin may be left floating. See Figures 5 and 6. Up to four Bt473s may be driven by this output.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.
WR*	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously. See Figures 1 and 8.
RD*	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously. See Figures 1 and 8.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as illustrated in Tables 1 and 2.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
CR0–CR3	Control outputs (TTL compatible). These outputs are used to control application-specific features. The output values are determined by the command register. See Figure 8.

Pin Descriptions (continued)


G7 G6 G5 G4 G3 G2 G1 G0 R7 R6 R5 R4 R3 R2 R1 R0 VREF OUT
60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44
B0 61
B1 62
B2 63
B3 64
B4 65
B5 66
B6 67
B7 68
VAA 1
VAA 2
GND 3
GND 4
S0 5
S1 6
BLANK* 7
SYNC* 8
CLOCK 9
43 VREF
42 OPA
41 COMP
40 IREF
39 IOB
38 IOG
37 IOR
36 VAA
35 VAA
34 VAA
33 VAA
32 GND
31 GND
30 CR3
29 CR2
28 CR1
27 CR0
10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
OL0 OL1 OL2 OL3 D0 D1 D2 D3 D4 D5 D6 D7 WR* RD* RS0 RS1 RS2

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in Bt451/7/8 Evaluation Module Operation and Measurements, application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt473 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a four-layer PC board is recommended with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

The optimum layout enables the Bt473 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8-inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2-inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground tub isolation technique is constrained by the noise margin degradation during digital readback of the Bt473.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

For maximum performance, a separate isolated ground plane for the analog output termination resistors, RSET resistor, and reference circuitry (if used) should be used, as shown in Figures 5, 6, and 7. Another isolated ground plane is used for the GND pins of the Bt473 and supply decoupling capacitors.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt473 power pins, any reference circuitry, and COMP and reference decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 5, 6, and 7. This bead should be located within 3 inches of the Bt473 and provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged such that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.001 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device.

The 10 µF capacitor is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic chip capacitor. Low-frequency supply noise will require a larger value. Lead lengths should be minimized for best performance.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt473 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt473 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt473 to minimize reflections. Unused analog outputs should be connected to GND.

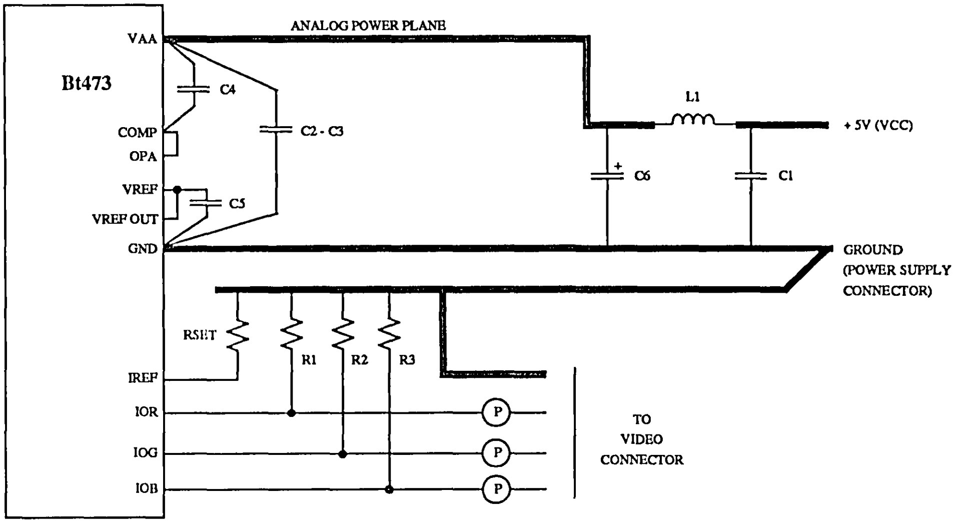
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

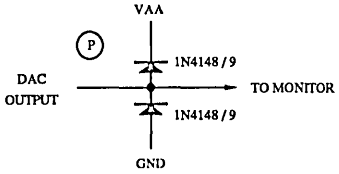
Analog Output Protection

The Bt473 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figures 5, 6, and 7 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)


Bt473
VAA
COMP
OPA
VREF
VREF OUT
GND
IREF
IOR
IOG
IOB
ANALOG POWER PLANE
C4
C2 - C3
C5
L1
+5V (VCC)
C6
C1
GROUND (POWER SUPPLY CONNECTOR)
RSET
R1
R2
R3
P
P
P
TO VIDEO CONNECTOR

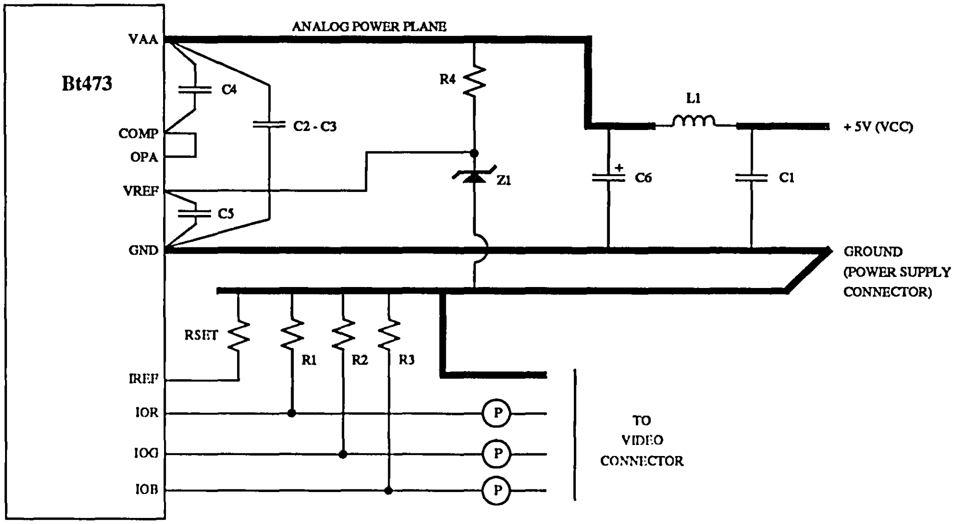

VAA
P
1N4148/9
DAC OUTPUT
TO MONITOR
1N4148/9
GND

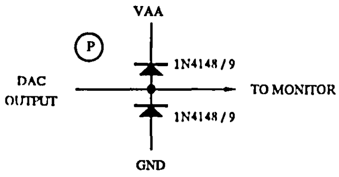
Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt473.

Figure 5. Typical Connection Diagram and Parts List (Internal Voltage Reference).

PC Board Layout Considerations (continued)


ANALOG POWER PLANE
VAA
Bt473
COMP
OPA
VREF
GND
IREF
IOR
IOG
IOB
C4
C2 - C3
C5
R4
Z1
L1
+5V (VCC)
C6
C1
GROUND
(POWER SUPPLY
CONNECTOR)
RSET
R1
R2
R3
P
P
P
TO
VIDEO
CONNECTOR

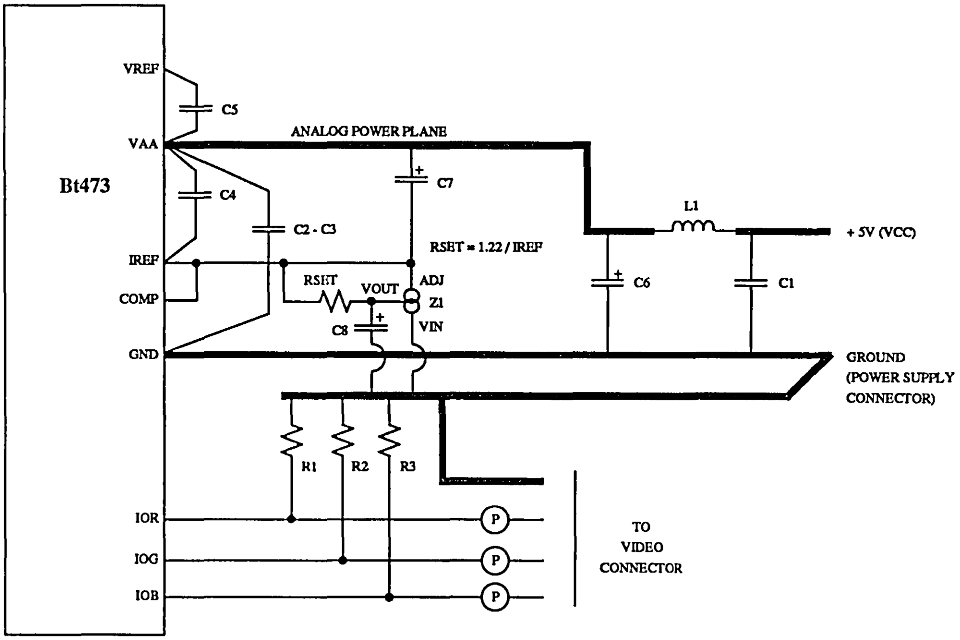

VAA
P
1N4148/9
DAC
OUTPUT
TO MONITOR
1N4148/9
GND

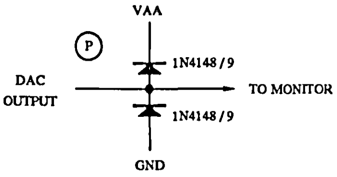
Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1k Ω 5% resistor	
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt473.

Figure 6. Typical Connection Diagram and Parts List (External Voltage Reference).

PC Board Layout Considerations (continued)


VREF
C5
VAA
ANALOG POWER PLANE
Bt473
C4
C7
C2 - C3
L1
+5V (VCC)
RSET = 1.22 / IREF
IREF
RSET
VOUT
ADJ
Z1
C6
C1
COMP
C8
VIN
GND
GROUND
(POWER SUPPLY
CONNECTOR)
R1
R2
R3
IOR
IOG
IOB
P
TO
VIDEO
CONNECTOR


VAA
P
1N4148/9
DAC
OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
C7, C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt473.

Figure 7. Typical Connection Diagram and Parts List (External Current Reference).

Application Information

Using Multiple Devices

When using multiple Bt473s, each Bt473 should have its own power plane ferrite bead.

Although the VREF OUT of a Bt473 may drive up to four Bt473s, higher performance may be obtained if each RAMDAC uses its own reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt473 must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

Reference Selection

An external voltage reference provides about 10x better power supply rejection on the analog outputs than an external current reference.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
80, 66 MHz Parts		4.75	5.00	5.25	Volts
50, 35 MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	TA	0		+ 70	°C
Output Load	RL		37.5		Ohms
Voltage Reference Configuration					
Reference Voltage	VREF	1.14	1.235	1.26	Volts
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		–3	–8.39	–10	mA
PS/2 Compatible		–3	–8.88	–10	mA

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error					
Using External Reference				±5	% Gray Scale
Using Internal Reference				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current (D0–D7)	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	-1.0		+1.5	Volts
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Voltage Reference Input Current	IVREF		10		µA
Reference Output Voltage	VREF OUT	1.08	1.2	1.32	Volts
Reference Output Current	IREF OUT		100		µA
Power Supply Rejection Ratio* (COMP = 0.1 µF, f = 1 KHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 Ω, VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note: When using the internal voltage reference, RSET may need to be adjusted to meet these limits. Also, the "gray-scale" output current (white level relative to black) will have a typical tolerance of ±10% rather than the ±5% specified above.

*Guaranteed but not tested.

Analog Output Levels — PS/2 Compatibility

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		1.01	1.51	2.0	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.6	8	9.4	mA
Sync Level		0	5	50	µA

Test conditions to generate PS/2 compatible video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 Ω, VREF = 1.235 V or external current reference with IREF = -8.88 mA.

AC Characteristics

		80 MHz Devices			66 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			80			66	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	3			3			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
CR0–CR3 Output Delay	9			100			100	ns
RD*, WR* Pulse Width Low	10	50			50			ns
RD*, WR* Pulse Width High	11	4*p14			4*p14			ns
Pixel and Control Setup Time	12	3			3			ns
Pixel and Control Hold Time	13	3			3			ns
Clock Cycle Time (p14)	14	12.5			15.15			ns
Clock Pulse Width High Time	15	4			5			ns
Clock Pulse Width Low Time	16	4			5			ns
Analog Output Delay	17			30			30	ns
Analog Output Rise/Fall Time	18		3			3		ns
Analog Output Settling Time*	19		13			13		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			150			150		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew			0	2		0	2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA		180	250		180	250	mA

See test conditions on next page.

AC Characteristics (continued)

		50 MHz Devices			35 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			50			35	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	3			3			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
CR0–CR3 Output Delay	9			100			100	ns
RD*, WR* Pulse Width Low	10	50			50			ns
RD*, WR* Pulse Width High	11	4*p14			4*p14			ns
Pixel and Control Setup Time	12	3			3			ns
Pixel and Control Hold Time	13	3			3			ns
Clock Cycle Time (p14)	14	20			28			ns
Clock Pulse Width High Time	15	6			7			ns
Clock Pulse Width Low Time	16	6			9			ns
Analog Output Delay	17			30			30	ns
Analog Output Rise/Fall Time	18		3			3		ns
Analog Output Settling Time*	19		13			13		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			150			150		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew			0	2		0	2	ns
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA		180	220		180	220	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 140 Ω, VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 75 pF. See timing notes in Figure 9. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA (max).

Timing Waveforms

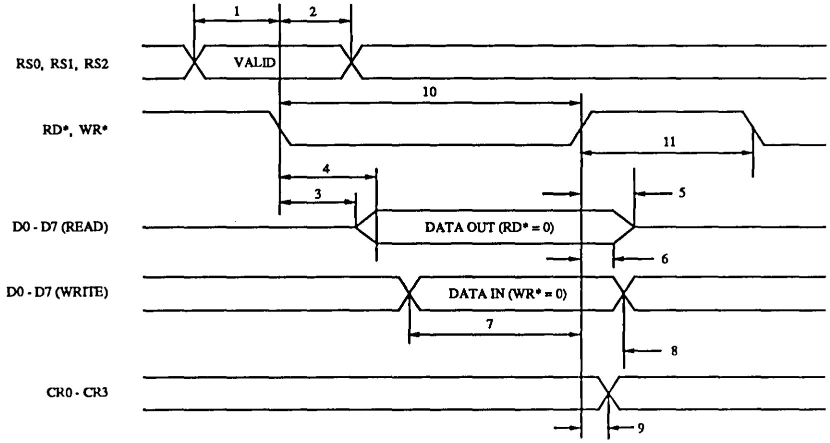
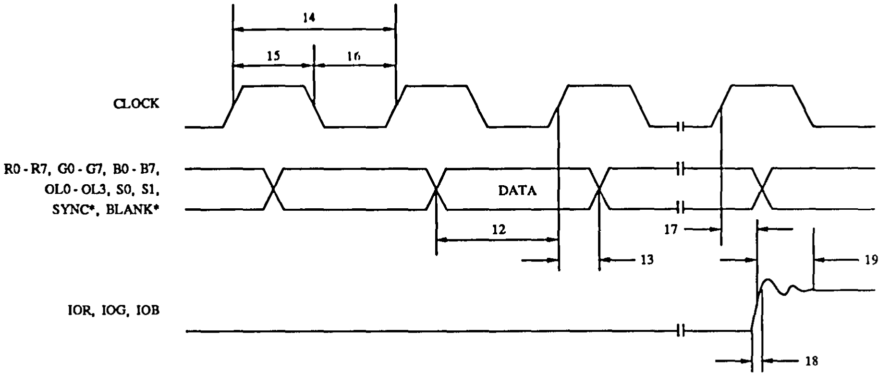

RS0, RS1, RS2
VALID
RD*, WR*
D0 - D7 (READ)
DATA OUT (RD* = 0)
D0 - D7 (WRITE)
DATA IN (WR* = 0)
CR0 - CR3
1
2
3
4
5
6
7
8
9
10
11

Figure 8. MPU Read/Write Timing.


CLOCK
R0 - R7, G0 - G7, B0 - B7,
OL0 - OL3, S0, S1,
SYNC*, BLANK*
DATA
IOR, IOG, IOB
12
13
14
15
16
17
18
19

Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 9. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt473KPJ80	80 MHz	68-pin Plastic J-Lead	0° to +70° C
Bt473KPJ66	66 MHz	68-pin Plastic J-Lead	0° to +70° C
Bt473KPJ50	50 MHz	68-pin Plastic J-Lead	0° to +70° C
Bt473KPJ35	35 MHz	68-pin Plastic J-Lead	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
F	AC parameters: RD* asserted to data bus driven time changed from 5 ns to 3 ns; maximum VAA supply current changed from 220 mA to 250 mA for 80 and 66 MHz devices.
G	Expanded PC Board Layout section.
H	Modified PC Board Layout recommendations. Modified Sync.

Advance Information

This document contains information on a product under development. The parametric information contains target parameters and is subject to change.

Bt474

85 MHz
Monolithic CMOS
256 x 24 Color Palette
RAMDAC™

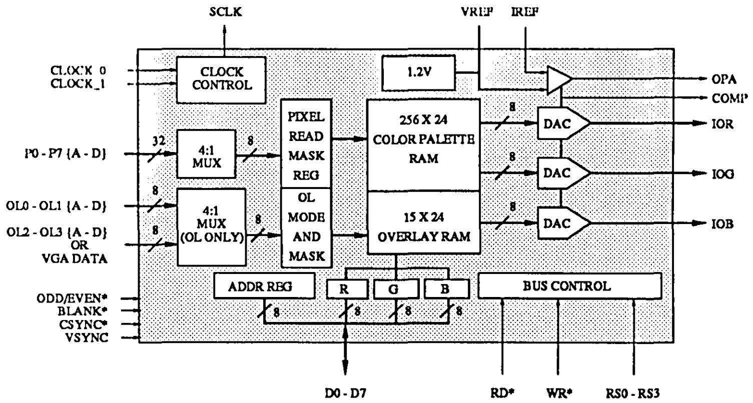
Distinguishing Features

- 85, 66 MHz Pipelined Operation
- 4:1 Multiplexed Pixel Ports
- VGA Pass-through Option via Overlays
- Triple 8-bit D/A Converters
- 256 x 24 Color Palette RAM
- 15 x 24 Overlay Color Palette
- Optional Sync on All Three Channels
- 0 or 7.5 IRE Blanking Pedestal
- Voltage or Current Reference
- Analog Output Comparators
- Anti-Sparkle Circuitry
- Power-Down Mode
- 84-pin PLCC Package

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Functional Block Diagram


SCLK
VREF
IREF
CLOCK 0
CLOCK_1
CLOCK CONTROL
1.2V
OPA
COMP
P0 - P7 {A - D}
32
4:1 MUX
8
PIXEL READ MASK REG
256 X 24 COLOR PALETTE RAM
DAC
IOR
IOG
IOB
OL0 - OL1 {A - D}
OL2 - OL3 {A - D} OR VGA DATA
4:1 MUX (OL ONLY)
OL MODE AND MASK
15 X 24 OVERLAY RAM
ADDR REG
R
G
B
BUS CONTROL
ODD/EVEN*
BLANK*
CSYNC*
VSYNC
D0 - D7
RD*
WR*
RS0 - RS3

Product Description

The Bt474 RAMDAC is designed specifically for high-performance color graphics.

Included are four byte-wide pixel input ports (multiplexed 4:1), a 256 x 24 color lookup table with triple 8-bit video D/A converters (configurable for either 6-bit or 8-bit D/A converter operation), and four overlay input ports (multiplexed 4:1) for supporting overlay/cursor information. The 4:1 multiplexed pixel ports ease interfacing to a high-resolution graphics frame buffer.

The Bt474 may alternately be configured for a lower performance VGA mode, where 8 bits of VGA pixel data (from a VGA controller) are input via two of the overlay input ports and displayed.

The Bt474 generates RS-343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L474001 Rev. B

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt474 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM. MPU data is transferred into and out of the Bt474 via the D0–D7 data pins. The read/write timing is controlled by the RD* and WR* inputs.

The RS0–RS3 select inputs specify which control register the MPU is accessing, as shown in Tables 1 and 2. The 8-bit address register is used to address the color palette RAM, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written. Refer to Figure 15 for MPU read write timing.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the overlay registers. After the blue write cycle, the 3 bytes of color information are concatenated into a 24-bit word and written to the overlay location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS3 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the

RS0 - RS3	Access	Addressed by MPU
$0	R/W	address register (RAM write mode)
$1	R/W	color palette RAM
$2	R/W	pixel read mask register
$3	R/W	address register (RAM read mode)
$4	R/W	address register (overlay write mode)
$5	R/W	overlay registers
$6	-	reserved
$7	R/W	address register (overlay read mode)
$8	R/W	command register_0
$9	R/W	command register_1
$A	read only	ID register ($11)
$B	read only	status register
$C	-	reserved
$D	-	reserved
$E	-	reserved
$F	-	reserved

Table 1. Control Input Truth Table.

Circuit Description (continued)

RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. To reduce noticeable sparkling on the CRT screen during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between lookup table RAMs and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

6-Bit / 8-Bit Operation

The command bit CR01 is used to specify whether the MPU is reading and writing 8 bits or 6 bits of color information each cycle.

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 are a logical zero.

Note that in the 6-bit mode, the Bt474's full-scale output current will be about 1.5% lower than when in the 8-bit mode. This is due to the two LSBs of each 8-bit DAC always being a logical zero in the 6-bit mode.

Power-Down Mode

The Bt474 incorporates a power-down capability, controlled by command bit CR03. While command bit CR03 is a logical zero, the Bt474 functions normally.

While command bit CR03 is a logical one, the DACs and power to the RAM are turned off. Note that the RAM still retains the data. Also, the RAM may be read or written to by the MPU as long as the pixel clock is running. The RAM automatically powers up during MPU read/write cycles, and shuts down when the MPU access is completed. SCLK is forced into the three-state mode, bidirectional buses are forced to be inputs, the DACs output no current, and the two command registers may still be written to or read by the MPU. Note that the output DACs require about one second to turn off (sleep mode) or turn on (normal).

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10				red value green value blue value
ADDR0–7 (counts binary)	$00–$FF	0	0	1	color palette RAM
	xxxx 0000	1	0	1	reserved
	xxxx 0001	1	0	1	overlay color 1
	:	:	:	:	:
	xxxx 1111	1	0	1	overlay color 15

Table 2. Address Register (ADDR) Operation (RS3 = 0).

Circuit Description (continued)

The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If using an external current reference, external circuitry should turn the current reference off (IREF = 0 mA) during sleep mode.

When using an external voltage reference, external circuitry should turn off the voltage reference (VREF = 0 V) to further reduce power consumption due to biasing of portions of the internal voltage reference.

Frame Buffer Clocking

The Video DRAM shift clock (SCLK) is generated by the Bt474. SCLK is 1/4 the pixel clock rate in overlay modes 2 and 3. In overlay modes 0 and 1, SCLK is equal to the pixel clock rate.

P0–P7 {A–D} are pixel data (8 bits per pixel) for four horizontally consecutive pixels. P0–P7 {A–D} are always latched on the rising edge of SCLK.

The pixel clock is specified to be either CLOCK_0 or CLOCK_1 by command bit CR12.

Frame Buffer Pixel Port Interface

There are four 8-bit pixel ports, P0–P7 {A–D}, used to interface to the frame buffer memory.

Video input data ports A through D are designated in this manner to represent the order of pixel data presentation. Port A always corresponds to the first pixel of the first line of the display. This would be the first pixel fed to the analog outputs, followed by B, then C, and finally D, repeating the pattern ABCD, ABCD, ABCD, etc. until the first scan line is completely displayed.

At this point, the output sequence is dependent on the CR05 command bit and the ODD/EVEN* input, i.e.,, whether interlaced or noninterlaced operation is selected, the current field being displayed, and whether or not an interleaved frame buffer memory is being used.

Scan line 0 is always displayed first in the interlaced mode and is considered the first line of the EVEN field. In the noninterlaced mode, scan line 1 immediately follows scan line 0. In the interlaced mode, scan line 1 is considered to be the first line of the ODD field and is displayed only after the entire EVEN field has been displayed.

Tables 3 and 4 demonstrate the display sequence. Table 3 shows the display sequence for interleaved frame buffer memory, while Table 4 shows the display sequence for noninterleaved frame buffer memory. The CR00 control bit determines whether or not the Bt474 uses an interleaved frame buffer memory configuration.

Figures 1 through 9 and Tables 3 and 4 show the interlaced and noninterlaced display timing including the interleave operation.

Pixel Read Mask

Each pixel clock cycle, P0-P7 pixel data is bit-wise logically ANDed with the contents of the pixel read mask register. The result is used to address the 256 x 24 color palette RAM. The addressed location provides 24 bits of color information to the three D/A converters.

Circuit Description (continued)

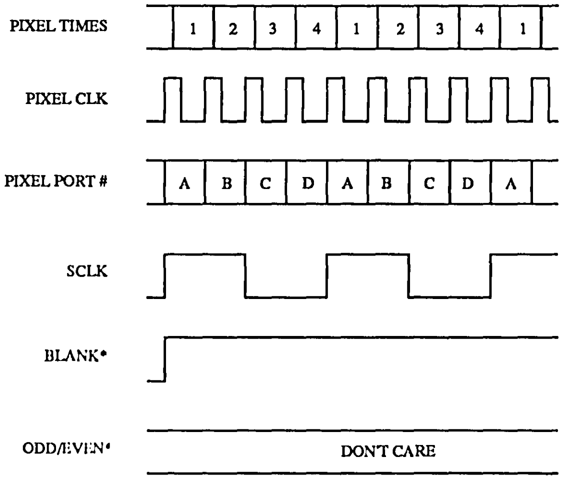

PIXEL TIMES
1
2
3
4
1
2
3
4
1
PIXEL CLK
PIXEL PORT #
A
B
C
D
A
B
C
D
A
SCLK
BLANK*
ODD/EVEN*
DON'T CARE

Figure 1. Timing, Interleaved (CR00 = 1), Noninterlaced (CR05 = 0), Scan Line 0.

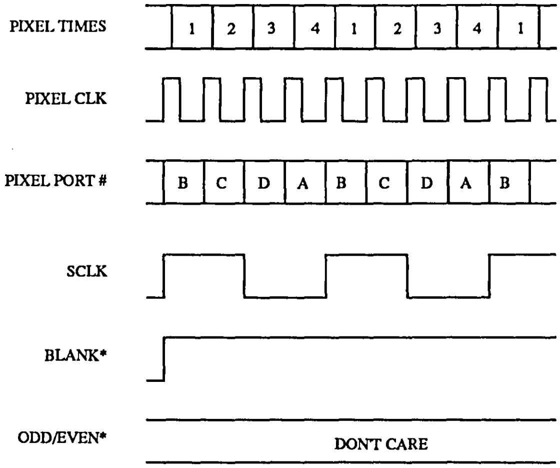

PIXEL TIMES
1
2
3
4
1
2
3
4
1
PIXEL CLK
PIXEL PORT #
B
C
D
A
B
C
D
A
B
SCLK
BLANK*
ODD/EVEN*
DON'T CARE

Figure 2. Timing, Interleaved (CR00 = 1), Noninterlaced (CR05 = 0), Scan Line 1.

Circuit Description (continued)

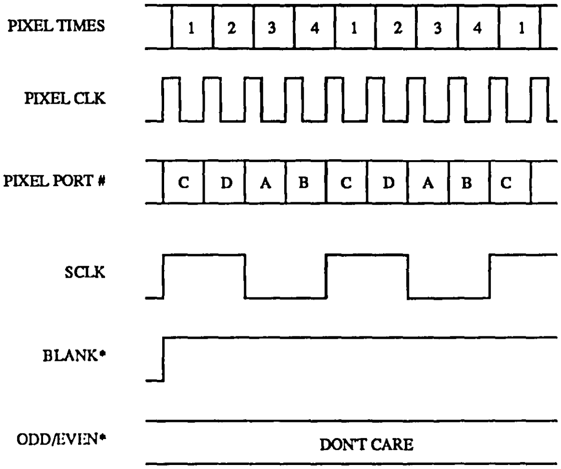

PIXEL TIMES
1
2
3
4
1
2
3
4
1
PIXEL CLK
PIXEL PORT #
C
D
A
B
C
D
A
B
C
SCLK
BLANK*
ODD/EVEN*
DON'T CARE

Figure 3. Timing, Interleaved (CR00 = 1), Noninterlaced (CR05 = 0), Scan Line 2.

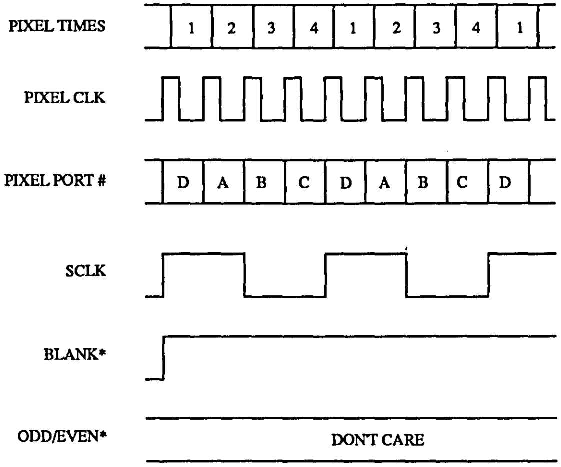

PIXEL TIMES
1
2
3
4
1
2
3
4
1
PIXEL CLK
PIXEL PORT #
D
A
B
C
D
A
B
C
D
SCLK
BLANK*
ODD/EVEN*
DON'T CARE

Figure 4. Timing, Interleaved (CR00 = 1), Noninterlaced (CR05 = 0), Scan Line 3.

Circuit Description (continued)

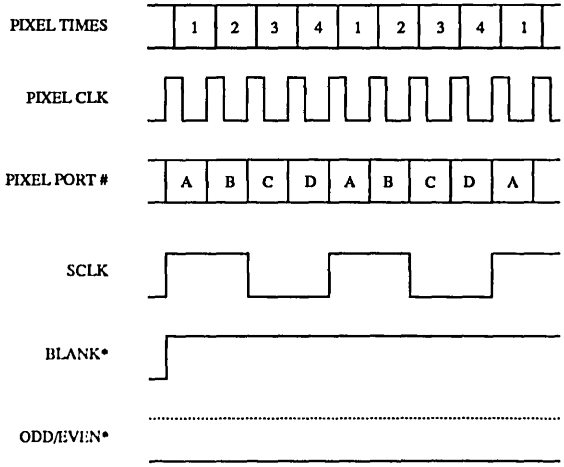

PIXEL TIMES
1 2 3 4 1 2 3 4 1
PIXEL CLK
PIXEL PORT #
A B C D A B C D A
SCLK
BLANK*
ODD/EVEN*

Figure 5. Timing, Interleaved (CR00 = 1), Interlaced (CR05 = 1), Even Field, Scan Line 0.

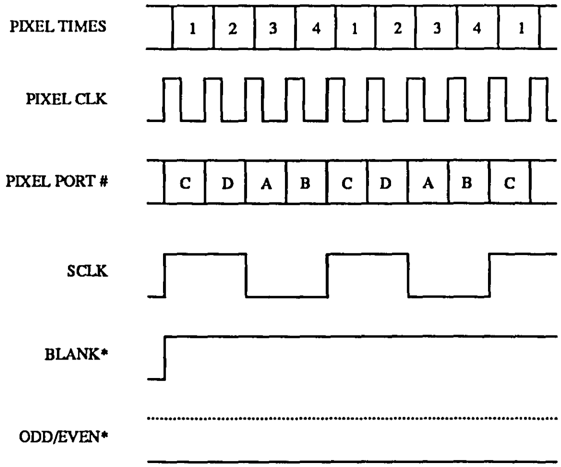

PIXEL TIMES
1 2 3 4 1 2 3 4 1
PIXEL CLK
PIXEL PORT #
C D A B C D A B C
SCLK
BLANK*
ODD/EVEN*

Figure 6. Timing, Interleaved (CR00 = 1), Interlaced (CR05 = 1) Even Field, Scan Line 2.

Circuit Description (continued)

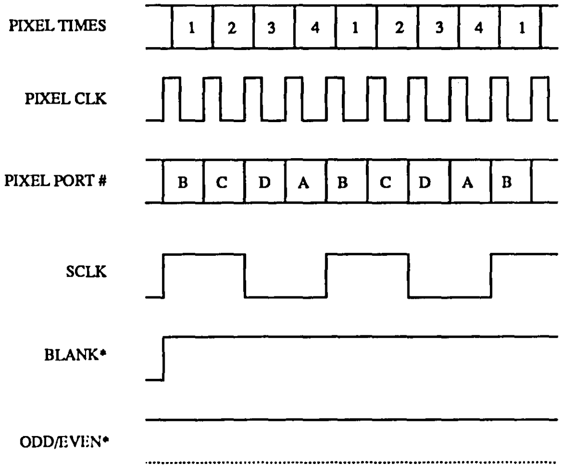

PIXEL TIMES
1
2
3
4
1
2
3
4
1
PIXEL CLK
PIXEL PORT #
B
C
D
A
B
C
D
A
B
SCLK
BLANK*
ODD/EVEN*

Figure 7. Timing, Interleaved (CR00 = 1), Interlaced (CR05 = 1), Odd Field, Scan Line 1.

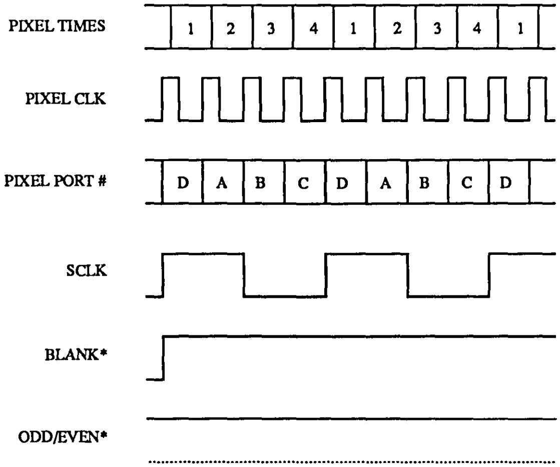

PIXEL TIMES
1
2
3
4
1
2
3
4
1
PIXEL CLK
PIXEL PORT #
D
A
B
C
D
A
B
C
D
SCLK
BLANK*
ODD/EVEN*

Figure 8. Timing, Interleaved (CR00 = 1), Interlaced (CR05 = 1), Odd Field, Scan Line 3.

Circuit Description (continued)

CR05	ODD/EVEN*	Scan Line #	Pixel Port Access Sequence		
Noninterlaced					
0	x	0	ABCD	ABCD	ABCD...
0	x	1	BCDA	BCDA	BCDA...
0	x	2	CDAB	CDAB	CDAB...
0	x	3	DABC	DABC	DABC...
0	x	4	ABCD	ABCD	ABCD...
0	x	5	BCDA	BCDA	BCDA...
0	x	6	CDAB	CDAB	CDAB...
0	x	7	DABC	DABC	DABC...
Interlaced, Even Field					
1	0	0	ABCD	ABCD	ABCD...
1	0	2	CDAB	CDAB	CDAB...
1	0	4	ABCD	ABCD	ABCD...
1	0	6	CDAB	CDAB	CDAB...
Interlaced, Odd Field					
1	1	1	BCDA	BCDA	BCDA...
1	1	3	DABC	DABC	DABC...
1	1	5	BCDA	BCDA	BCDA...
1	1	7	DABC	DABC	DABC...

Table 3. Interleaved Operation (CR00 = 1).

Circuit Description (continued)

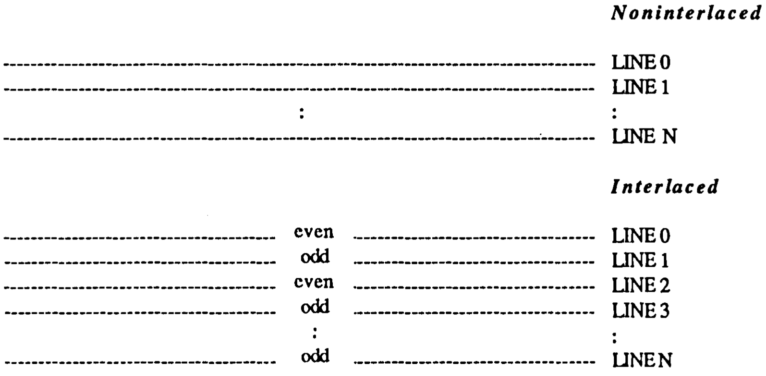

Noninterlaced
LINE 0
LINE 1
:
LINE N
Interlaced
even
LINE 0
odd
LINE 1
even
LINE 2
odd
LINE 3
:
odd
LINE N

Figure 9. Interlaced / Noninterlaced Display Operation.

CR05	ODD/EVEN*	Scan Line #	Pixel Port Access Sequence		
Noninterlaced					
0	x	0	ABCD	ABCD	ABCD
0	x	1	ABCD	ABCD	ABCD
0	x	2	ABCD	ABCD	ABCD
0	x	3	ABCD	ABCD	ABCD
0	x	4	ABCD	ABCD	ABCD
0	x	5	ABCD	ABCD	ABCD
0	x	6	ABCD	ABCD	ABCD
0	x	7	ABCD	ABCD	ABCD
Interlaced, Even Field					
1	0	0	ABCD	ABCD	ABCD
1	0	2	ABCD	ABCD	ABCD
1	0	4	ABCD	ABCD	ABCD
1	0	6	ABCD	ABCD	ABCD
Interlaced, Odd Field					
1	1	1	ABCD	ABCD	ABCD
1	1	3	ABCD	ABCD	ABCD
1	1	5	ABCD	ABCD	ABCD
1	1	7	ABCD	ABCD	ABCD

Table 4. Noninterleaved Operation (CR00 = 0).

Circuit Description (continued)

Overlay Operation

The four 4-bit overlay inputs, OL0–OL3 {A–D), are used to input overlay and other information. OL0, OL1, OL2, and OL3 inputs each have a read mask bit (CR14, CR15, CR16, and CR17, respectively). The mask bits are logically ANDed with the respective overlay bit after the overlay mode circuitry.

As shown in Table 5, the overlay inputs may be configured to operate in four different modes, as determined by the CR10 and CR11 command bits.

Note the overlay inputs are never interleaved.

Mode 0 Operation

In mode 0, the OL2 and OL3 inputs are used to input VGA pixel data from a VGA controller, while the OL0 and OL1 inputs are used to provide overlay (or a three-color cursor) information. (See Table 6.)

In this mode, the P0–P7 pixel inputs are ignored—pixel data is input using both OL2 and OL3 (as OL2 and OL3 provide a total of eight inputs, 8 bits per pixel of VGA pixel data may be input).

The selected clock input (CLOCK_0 or CLOCK_1) is output directly onto SCLK (without dividing by four) since the VGA pixel inputs will be input using a 1:1 multiplex mode. CLOCK_0 should be selected as the pixel clock while in this mode.

Mode	CR11	CR10	OL3 {A–D)	OL2 {A–D)	OL1 {A–D)	OL0 {A–D)
0	0	0	VGA data (4 bits)	VGA data (4 bits)	cursor data	cursor data
1	0	1	VGA data (4 bits)	VGA data (4 bits)	cursor enable	cursor data
2	1	0	cursor data	cursor data	cursor data	cursor data
3	1	1	cursor enable	cursor data	cursor enable	cursor data

Table 5. Overlay Configurations.

	VGA Data		Overlay Data		
	OL3D, OL3C, OL3B, OL3A	OL2D, OL2C, OL2B, OL2A	OL1	OL0	Color Palette Addressed
No Overlay	0000	0000	0	0	color palette RAM location $00
	0000	0001	0	0	color palette RAM location $01
	:	:	:	:	:
	1111	1111	0	0	color palette RAM location $FF
3-Color Overlay	xxxx	xxxx	0	1	overlay color 1
	xxxx	xxxx	1	0	overlay color 2
	xxxx	xxxx	1	1	overlay color 3

Table 6. Mode 0 (VGA Mode, 3-Color Overlay) Overlay Configuration.

Circuit Description (continued)

	VGA Data		Overlay Data		
	OL3D, OL3C, OL3B, OL3A	OL2D, OL2C, OL2B, OL2A	OL1	OL0	Color Palette Addressed
No Overlay	0000	0000	0	x	color palette RAM location $00
	0000	0001	0	x	color palette RAM location $01
	:	:	:	:	:
	1111	1111	0	x	color palette RAM location $FF
2-Color Overlay	xxxx	xxxx	1	0	overlay color 2
	xxxx	xxxx	1	1	overlay color 3

Table 7. Mode 1 (VGA Mode, 2-Color Overlay) Overlay Configuration.

	Overlay Data	Video	
	OL3–OL0	P7–P0	Color Palette Addressed
No Overlay	0000	0000 0000	color palette RAM location $00
	0000	0000 0001	color palette RAM location $01
	:	:	:
	0000	1111 1111	color palette RAM location $FF
15 Color Overlay	0001	xxxx xxxx	overlay color 1
	0010	xxxx xxxx	overlay color 2
	:	:	:
	1111	xxxx xxxx	overlay color 15

Table 8. Mode 2 (15-Color Overlay) Overlay Configuration.

	Enable	Data	Enable	Data	
	OL3	OL2	OL1	OL0	Color Palette Addressed
No Overlay	0	x	0	x	color palette RAM location specified by P0–P7
Dual 2-Color Overlays	0	x	1	0	overlay color 2
	0	x	1	1	overlay color 3
	1	0	0	x	overlay color 8
	1	1	0	x	overlay color 12
Overlay Collisions	1	0	1	0	overlay color 10
	1	0	1	1	overlay color 11
	1	1	1	0	overlay color 14
	1	1	1	1	overlay color 15

Table 9. Mode 3 (Dual 2-Color Overlays) Overlay Configuration.

Circuit Description (continued)

Mode 1 Operation

In mode 1, the OL2 and OL3 inputs are used to input VGA pixel data from a VGA controller, while the OL0 and OL1 inputs are used to provide overlay (or a two-color cursor) information. (See Table 7.)

In this mode, the P0–P7 pixel inputs are ignored —pixel data is input using both OL2 and OL3 (as OL2 and OL3 provide a total of eight inputs, 8 bits per pixel of VGA pixel data may be input).

The selected clock input (CLOCK_0 or CLOCK_1) is output directly onto SCLK (without dividing by four) since the VGA pixel inputs will be input using a 1:1 multiplex mode. CLOCK_0 should be selected as the pixel clock while in this mode.

Mode 2 Operation

In the normal overlay mode (mode 2), 4 bits of overlay (or cursor) information are used to enable 15 overlay colors to be displayed. If OL0–OL3 = 0000, P0–P7 pixel data is displayed; otherwise overlay data is displayed.

Table 8 shows the pixel and overlay color palette selection for this mode.

In this mode, OL0–OL3 {A–D} are latched on the rising edge of SCLK and have the same timing as the P0–P7 {A–D} pixel data.

SCLK is 1/4 the selected pixel clock (CLOCK_0 or CLOCK_1).

Mode 3 Operation

In mode 3, two two-color cursors may be displayed. Table 9 shows the operation of the pixel and overlay inputs in this mode. Note that OL3 and OL2 are logically ANDed together, while OL1 and OL0 are logically ANDed together. Thus, OL1 and OL3 become configured as enable bits for OL0 and OL2, respectively.

In this mode, OL0–OL3 {A–D} are latched on the rising edge of SCLK and have the same timing as the P0–P7 {A–D} pixel data.

SCLK is 1/4 the selected pixel clock (CLOCK_0 or CLOCK_1).

Video Generation

The CSYNC* and BLANK* inputs, also latched on the rising edge of SCLK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figures 10 and 11. Tables 10 and 11 detail how the CSYNC* and BLANK* inputs modify the output levels.

The CR04 command bit is used to specify whether a 0 or 7.5 IRE blanking pedestal is to be used. Command bit CR06 specifies whether or not the RGB outputs contain sync information.

The analog outputs of the Bt474 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

ESD and Latchup Considerations

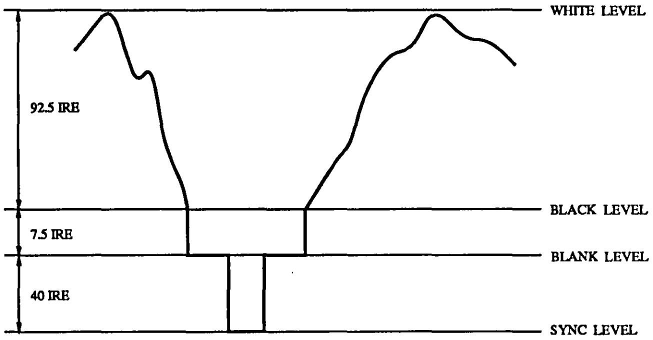
Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Circuit Description (continued)

NO SYNC		SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly terminated load, VREF = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

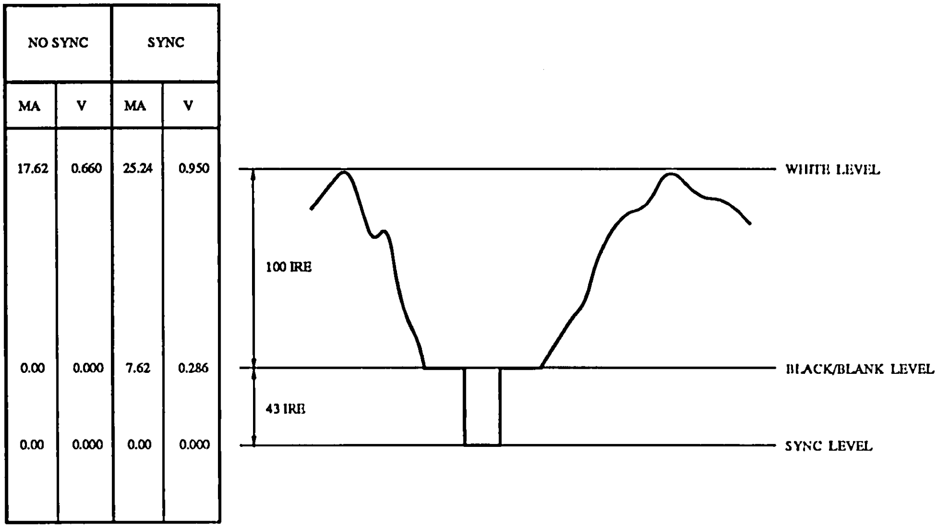
Figure 10. Composite Video Output Waveforms (SETUP = 7.5 IRE).

Description	Sync Disabled	Sync Enabled	CSYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	19.05	26.67	1	1	$FF
DATA	data + 1.44	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	1.44	9.05	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly terminated load, VREF = 1.235 V, RSET = 147 Ω.

Table 10. Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)



NO SYNC		SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000

Note: 75 Ω doubly terminated load, VREF = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances assumed on all levels.

Figure 11. Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled	Sync Enabled	CSYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly terminated load, VREF = 1.235 V, RSET = 147 Ω.

Table 11. Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register_0

This register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to data bus bit D0, the least significant data bit.

CR07	reserved (logical one)	A logical one must be written to this bit when writing to the command register.
CR06	Sync enable (0) no sync (1) sync	This bit specifies whether the RGB outputs are to contain sync information or not.
CR05	Display mode select (0) noninterlace (1) interlace	This bit specifies whether the display is interlaced or noninterlaced and selects the appropriate interleave patterns.
CR04	Setup select (0) 0 IRE (1) 7.5 IRE	This bit specifies whether the IOR, IOG, and IOB outputs contain a 0 or 7.5 IRE blanking pedestal.
CR03	Power down enable (0) normal operation (1) reduce power	While this bit is a logical zero, the Bt474 functions normally. If this bit is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data and CPU reads and writes can occur with no loss of data.
CR02	Nibble swap (0) normal input (1) swap MSN and LSN	When set, this bit swaps the two nibbles of color data addressing the color palette RAM. This bit affects only pixel ports P0–P7 {A–D}.
CR01	Color value select (0) 6-bit (1) 8-bit	When set, 8-bit color data is used in the color palette RAM. When reset, 6-bit color data is used.
CR00	Interleave enable (0) no interleave (1) interleave	A logical zero inhibits the internal logic from interleaving the P0–P7 {A–D} inputs. A logical one enables the P0–P7 {A–D} inputs to be interleaved.

Internal Registers (continued)

Command Register_1

This register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to data bus bit D0, the least significant data bit.

CR17	OL3 enable (0) force OL3 to logical zero (1) pass OL3 data	This bit is logically ANDed with OL3 data immediately after the overlay mode circuitry.
CR16	OL2 enable (0) force OL2 to logical zero (1) pass OL2 data	This bit is logically ANDed with OL2 data immediately after the overlay mode circuitry.
CR15	OL1 enable (0) force OL1 to logical zero (1) pass OL1 data	This bit is logically ANDed with OL1 data immediately after the overlay mode circuitry.
CR14	OL0 enable (0) force OL0 to logical zero (1) pass OL0 data	This bit is logically ANDed with OL0 data immediately after the overlay mode circuitry.
CR13	Test path enable (0) normal mode (1) test mode	A logical one enables certain test paths to be internally set up. This involves any input mode and any inputs which affect access to the color palette RAMs.
CR12	Clock selection (0) CLOCK_0 (1) CLOCK_1	This bit selects which pixel clock input to use.
CR11, CR10	Overlay operation select (00) mode 0 (01) mode 1 (10) mode 2 (11) mode 3	These bits select the mode of operation for the OL0–OL3 {A–D} inputs as shown in Tables 5–9. When selecting modes 0 or 1, the CLOCK_0 input should be selected to be the pixel clock.

Internal Registers (continued)

Pixel Read Mask Register

The 8-bit pixel read mask register may be written to or read by the MPU at any time, and is not initialized. D0 is the least significant bit. The contents of this register are bit-wise ANDed with the P0–P7 pixel data prior to addressing the color palette RAM.

ID Register

This 8-bit register may be read by the MPU at any time and contains the ID number $11. MPU write cycles to this register are ignored.

Status Register

The 8-bit status register may be read by the MPU at any time; MPU write cycles to this register are ignored. D0 is the least significant bit.

D1–D7 are always a logical zero.

D0 is the SENSE* bit. If it is a logical zero, one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). This bit is used to determine the presence of a CRT monitor and, via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned.

The 335 mV reference has a ±5% minimum tolerance when using an external voltage reference or a ±10% tolerance when using an external current reference or the internal voltage reference.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 10 and 11. It is latched on the rising edge of SCLK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
CSYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 10 and 11). CSYNC* does not override any other control or data input, as shown in Tables 10 and 11; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of SCLK. If sync information is not to be generated on the analog outputs, this pin should be connected to GND.
VSYNC	Vertical sync control input (TTL compatible). VSYNC is sampled on the falling edge of BLANK* in the first field/frame to determine the polarity of VSYNC. If a logical one is latched, VSYNC is assumed to be an active low signal; if a logical zero is latched, VSYNC is assumed to be an active high signal.
ODD/EVEN*	Odd/even field input (TTL compatible). This input is latched on the rising edge of SCLK. This input is ignored if noninterlaced operation (command bit CR05) is selected.
CLOCK_0, CLOCK_1	Pixel clock inputs (TTL compatible). It is recommended that each clock input be driven by a dedicated buffer to avoid reflection-induced jitter.
SCLK	Shift clock output (TTL compatible). SCLK is 1/4 the pixel clock rate, except when the overlays are in the VGA mode (overlay modes 0 and 1).
P0–P7 {A–D}	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of SCLK. P0 is the LSB. Unused inputs should be connected to GND.
OL0–OL3 {A–D}	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information. When accessing the overlay palette, the P0–P7 {A–E} inputs are ignored. They are latched on the rising edge of SCLK. OL0 is the LSB. Unused inputs should be connected to GND.
COMP	Compensation pin. If an external or the internal voltage reference is used (Figures 12 and 13), this pin should be connected to OPA. If an external current reference is used (Figure 14), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *Refer to PC Board Layout Considerations for critical layout criteria.*
VREF	Voltage reference input. If an external voltage reference is used (Figure 13), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 14), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor is used to decouple this input to GND, as shown in Figures 12 and 13. If the VAA supply is very clean, better performance may be obtained by decoupling VREF to VAA. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When using the internal reference, this pin should not drive any external circuitry, except for the decoupling capacitor (Figure 12).
OPA	Reference amplifier output. If an external or the internal voltage reference is used (Figures 12 and 13), this pin must be connected to COMP. When using an external current reference (Figure 14), this pin should be left floating.
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)

Pin Name	Description
IREF	Full-scale adjust control. Note that the IRE relationships in Figures 10 and 11 are maintained, regardless of the full-scale output current.

When using an external or the internal voltage reference (Figures 12 and 13), a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is:

RSET (Ω) = K * 1,000 * VREF (v) / Iout (mA)

K is defined in the table below. It is recommended that a 147 Ω RSET resistor be used for doubly terminated 75 Ω loads (i.e., RS-343A applications).

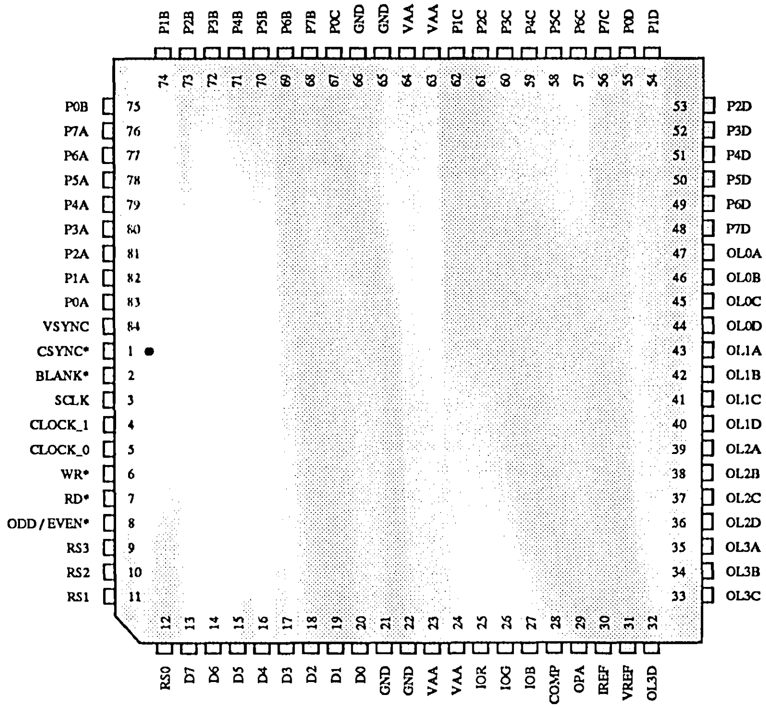
When using an external current reference (Figure 14), the relationship between IREF and the full-scale output current on each output is:

IREF (mA) = Iout (mA) / K

	Sync Enabled		Sync Disabled	
Setup	0 IRE	7.5 IRE	0 IRE	7.5 IRE
K=	3.025	3.195	3.000	3.170

Pin Name	Description
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figures 12, 13, and 14).
WR*	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS3 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously.
RD*	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS3 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously.
RS0–RS3	Register select inputs (TTL compatible). RS0–RS3 specify the type of read or write operation being performed, as illustrated in Tables 1 and 2.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.

Pin Descriptions (continued)


P1B
P2B
P3B
P4B
P5B
P6B
P7B
P0C
GND
GND
VAA
VAA
P1C
P2C
P3C
P4C
P5C
P6C
P7C
P0D
P1D
P0B
P7A
P6A
P5A
P4A
P3A
P2A
P1A
P0A
VSYNC
CSYNC*
BLANK*
SCLK
CLOCK_1
CLOCK_0
WR*
RD*
ODD/EVEN*
RS3
RS2
RS1
P2D
P3D
P4D
P5D
P6D
P7D
OL0A
OL0B
OL0C
OL0D
OL1A
OL1B
OL1C
OL1D
OL2A
OL2B
OL2C
OL2D
OL3A
OL3B
OL3C
RS0
D7
D6
D5
D4
D3
D2
D1
D0
GND
GND
VAA
VAA
IOR
IOG
IOB
COMP
OPA
IREF
VREF
OL3D
74 73 72 71 70 69 68 67 66 65 64 63 62 61 60 59 58 57 56 55 54
75 76 77 78 79 80 81 82 83 84 1 2 3 4 5 6 7 8 9 10 11
53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33
12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in Bt451/7/8 Evaluation Module Operation and Measurements, application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt474 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a four-layer PC board is recommended with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

The optimum layout enables the Bt474 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8-inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground tub isolation technique is constrained by the noise margin degradation during digital readback of the Bt474.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

For maximum performance, a separate isolated ground plane for the analog output termination resistors, RSET resistor, and reference circuitry (if used) should be used, as shown in Figures 12, 13, and 14. Another isolated ground plane is used for the GND pins of the Bt474 and supply decoupling capacitors.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt474 power pins, any reference circuitry, and COMP and reference decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 12, 13, and 14. This bead should be located within 3 inches of the Bt474 and provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.001 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device.

The 10 µF capacitor is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic chip capacitor. Low frequency supply noise will require a larger value. Lead lengths should be minimized for best performance.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt474 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt474 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt474 to minimize reflections. Unused analog outputs should be connected to GND.

Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

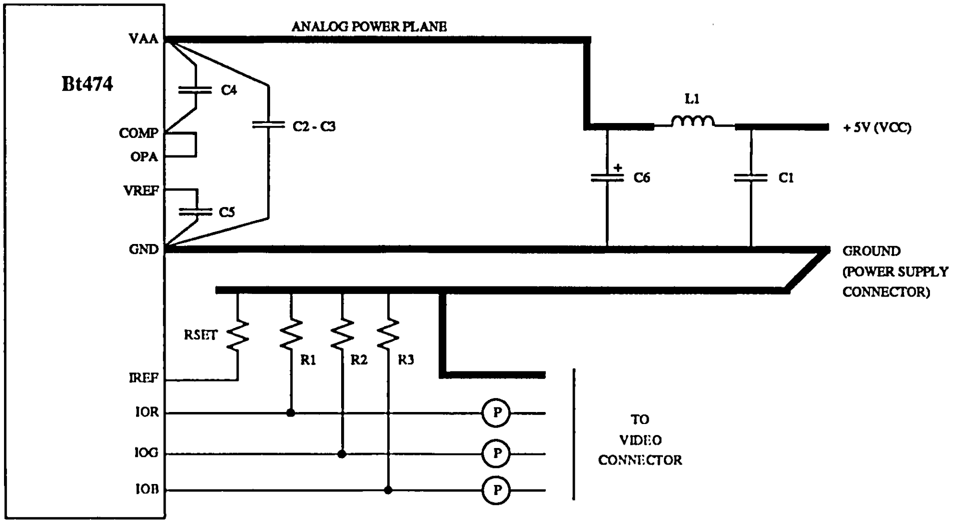
Analog Output Protection

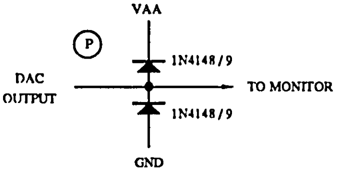
The Bt474 analog outputs should be protected against high energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figures 12, 13, and 14 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

4

PC Board Layout Considerations (continued)


Bt474
VAA
COMP
OPA
VREF
GND
IREF
IOR
IOG
IOB
ANALOG POWER PLANE
C4
C2 - C3
C5
L1
+5V (VCC)
C6
C1
GROUND
(POWER SUPPLY
CONNECTOR)
RSET
R1
R2
R3
P
P
P
TO
VIDEO
CONNECTOR

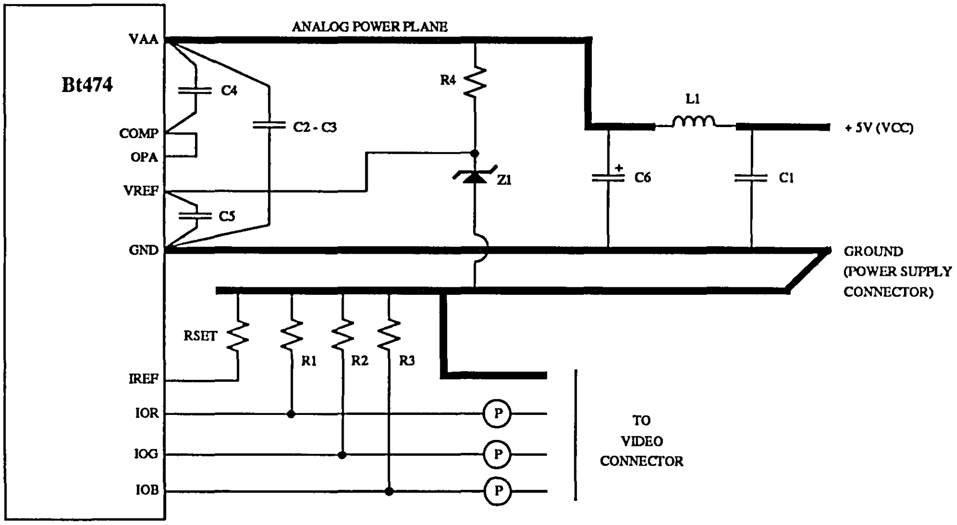

VAA
P
1N4148/9
DAC
OUTPUT
TO MONITOR
1N4148/9
GND

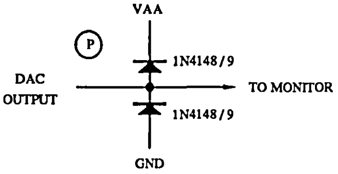
Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt474.

Figure 12. Typical Connection Diagram and Parts List (Internal Voltage Reference).

PC Board Layout Considerations (continued)


ANALOG POWER PLANE
VAA
Bt474
C4
C2 - C3
R4
L1
+5V (VCC)
COMP
OPA
VREF
Z1
C6
C1
C5
GND
GROUND
(POWER SUPPLY
CONNECTOR)
RSET
R1
R2
R3
IREF
IOR
IOG
IOB
P
P
P
TO
VIDEO
CONNECTOR

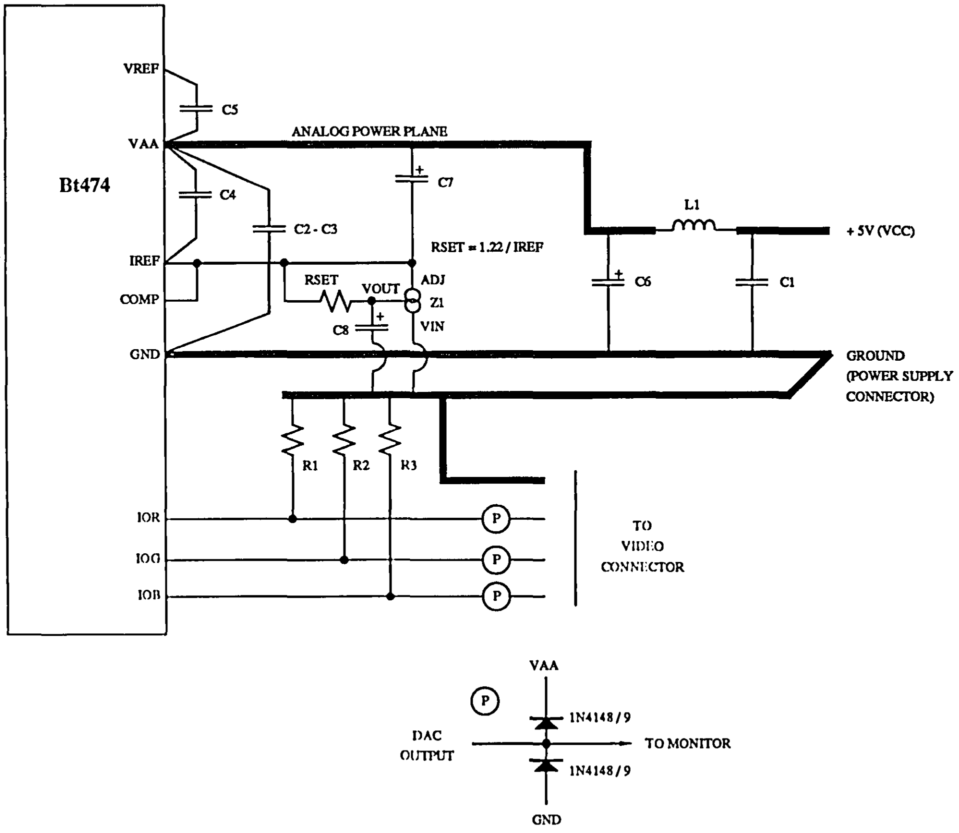

VAA
P
1N4148/9
DAC
OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description	Vendor Part Number
C1–C5	0.1 μF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 μF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	
RSET	147 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt474.

Figure 13. Typical Connection Diagram and Parts List (External Voltage Reference).

PC Board Layout Considerations (continued)


Bt474
VREF
VAA
IREF
COMP
GND
IOR
IOG
IOB
C5
C4
C2 - C3
ANALOG POWER PLANE
C7
RSET = 1.22 / IREF
RSET
VOUT
ADJ
Z1
VIN
C8
L1
+5V (VCC)
C6
C1
GROUND
(POWER SUPPLY
CONNECTOR)
R1
R2
R3
P
TO
VIDEO
CONNECTOR
VAA
1N4148/9
DAC
OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
C7, C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt474.

Figure 14. Typical Connection Diagram and Parts List (External Current Reference).

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ohms
Voltage Reference Configuration	VREF				
Reference Voltage		1.14	1.235	1.26	Volts
Current Reference Configuration	IREF				
IREF Current		-3	-8.88	-10	mA

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND-0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	−1.0		+1.5	Volts
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Voltage Reference Input Current	IREF IN		10		µA
Power Supply Rejection Ratio** (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with SETUP = 7.5 IRE, RSET = 147 Ω, VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note: When using the internal voltage reference, RSET may need to be adjusted to meet these limits. Also, the "gray-scale" output current (white level relative to black) will have a typical tolerance of ±10% rather than the ±5% specified above.

*In the 6-bit mode, the output levels are approximately 1.5% lower than these values.

**Guaranteed by characterization, not tested.

AC Characteristics

		85 MHz Devices			66 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
CLOCK_0, CLOCK_1 Rate	Fmax			85			66	MHz
RS0–RS3 Setup Time	1	10			10			ns
RS0–RS3 Hold Time	2	10			10			ns
RD* Asserted to D0–D7 Driven	3	2			2			ns
RD* Asserted to D0 -D7 Valid	4			40			40	ns
RD* Negated to D0–D7 3-Stated	5			20			20	ns
Read D0–D7 Hold Time	6	2			2			ns
Write D0–D7 Setup Time	7	10			10			ns
Write D0–D7 Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*pclk			6*pclk			ns
Setup Time (4:1 Mux Mode)	11	3			3			ns
P0–P7 and OL0–OL3 {A–D},								ns
CSYNC*, VSYNC, BLANK*,								
ODD/EVEN*								ns
Hold Time (4:1 Mux Mode)	12	3			3			ns
P0–P7 and OL0–OL3 {A–D},								ns
CSYNC*, VSYNC, BLANK*,								
ODD/EVEN*								ns
SCLK High Time (4:1 Mux Mode)	13	15			20			ns
SCLK Low Time (4:1 Mux Mode)	14	15			20			ns
SCLK Output Delay	15	4			4			ns
CLOCK_0, CLOCK_1 Low Time	16	4			5			ns
CLOCK_0, CLOCK_1 High Time	17	4			5			ns
CLOCK_0, CLOCK_1 Cycle Time	18	11.7			15.15			ns
Setup Time (1:1 Mux Mode)	19	3			3			ns
OL0A, OL1A, OL2–OL3 {A–D},								
CSYNC*, VSYNC, BLANK*,								
ODD/EVEN*								
Hold Time (1:1 Mux Mode)	20	3			3			ns
OL0A, OL1A, OL2–OL3 {A–D},								
CSYNC*, VSYNC, BLANK*,								
ODD/EVEN*								

Test conditions on next page.

AC Characteristics (continued)

Parameter	Symbol	85 MHz Devices			66 MHz Devices			Units
		Min	Typ	Max	Min	Typ	Max	
Analog Output Delay	21			30			30	ns
Analog Output Rise/Fall Time	22		3			3		ns
Analog Output Settling Time*	23		12			14		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			150			150		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
Pipeline Delay		5	5	5	5	5	5	Clocks
VAA Supply Current**	IAA							
Normal Operation			170	tbd		170	tbd	mA
"Sleep" Mode***			10	tbd		10	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with SETUP = 7.5 IRE, VREF = 1.235 V, RSET = 147 Ω. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF; D0–D7 output load ≤ 75 pF. SCLK output load = 80 pF. See timing notes in Figures 16 and 17. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

***External current or voltage reference disabled during sleep mode.

Note: "pclk" symbol refers to either CLOCK_0 or CLOCK_1 cycle time, whichever is selected.

Timing Waveforms

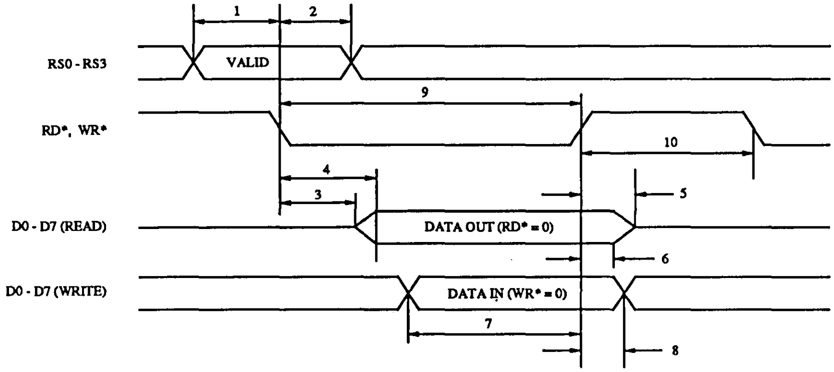
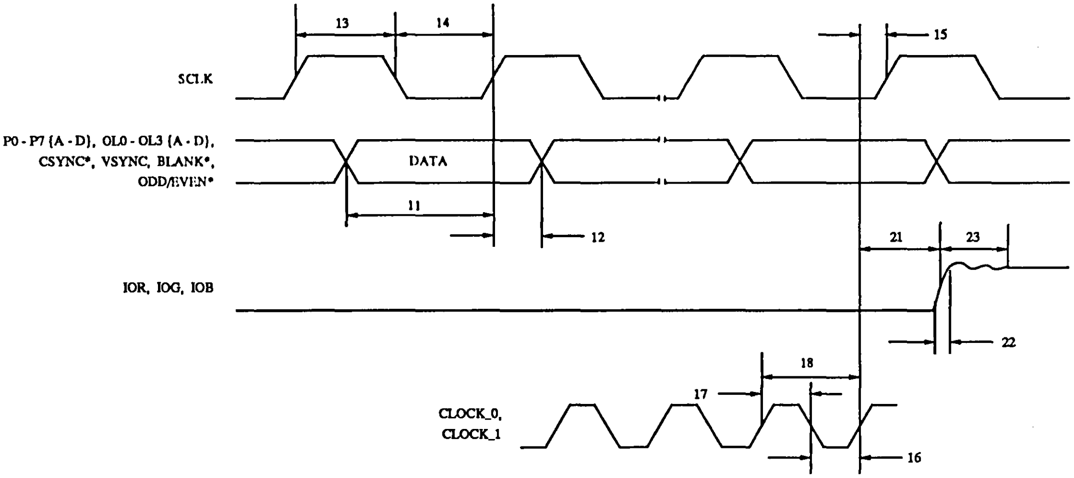

1
2
RS0 - RS3
VALID
9
RD*, WR*
10
4
3
5
D0 - D7 (READ)
DATA OUT (RD* = 0)
6
D0 - D7 (WRITE)
DATA IN (WR* = 0)
7
8

Figure 15. MPU Read/Write Timing.


13
14
15
SCLK
P0 - P7 {A - D}, OL0 - OL3 {A - D},
CSYNC*, VSYNC, BLANK*,
ODD/EVEN*
DATA
11
12
21
23
IOR, IOG, IOB
22
18
17
CLOCK_0,
CLOCK_1
16

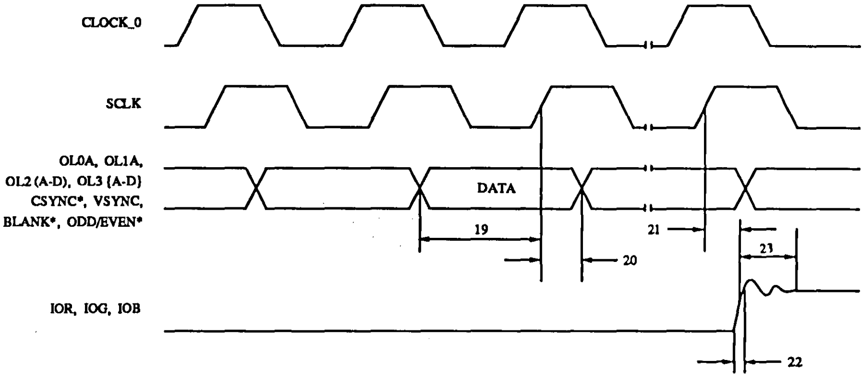
Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 16. Video Input/Output Timing.

Timing Waveforms (continued)


CLOCK_0
SCLK
OL0A, OL1A, OL2 (A-D), OL3 (A-D) CSYNC*, VSYNC, BLANK*, ODD/EVEN*
DATA
19
20
21
23
22
IOR, IOG, IOB

Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 17. Video Input/Output Timing (VGA Modes Operation).

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt474KPJ85	85 MHz	84-pin Plastic J-Lead	0° to +70° C
Bt474KPJ75	66 MHz	84-pin Plastic J-Lead	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
B	Changed speed grade listing from 75 MHz to 66 MHz. Revised PCB layout section.

Bt475

Bt477

80 MHz
256 Word Color Palette
Personal System/2®
Power-Down RAMDAC™

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

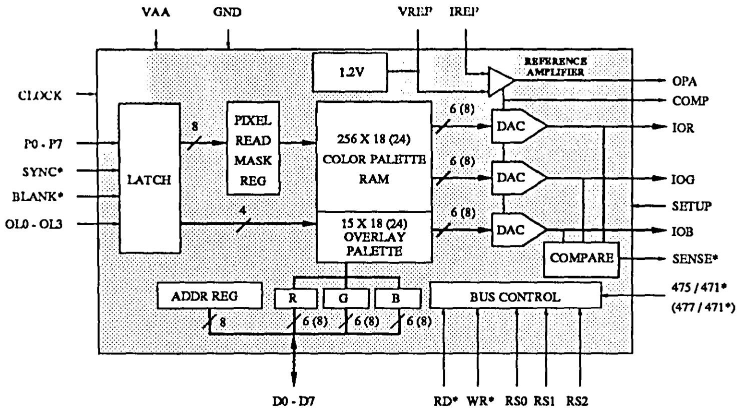
Distinguishing Features

- 80, 66, 50, 35 MHz Operation
- Bt471/476/478 Pin Compatible
- Power-Down Mode
- Anti-Sparkle Circuitry
- Analog Output Comparators
- Triple 6-bit (8-bit) D/A Converters
- 256 x 18 (24) Color Palette RAM
- RS-343A/RS-170-Compatible Outputs
- 15 x 18 (24) Overlay Registers
- Programmable Pedestal
- Optional Internal Reference
- 44-pin PLCC Package

Applications

- High Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing
- Laptop Computers

Functional Block Diagram


VAA
GND
VREF
IREF
CLOCK
P0 - P7
SYNC*
BLANK*
OL0 - OL3
LATCH
8
PIXEL READ MASK REG
4
1.2V
REFERENCE AMPLIFIER
256 X 18 (24) COLOR PALETTE RAM
15 X 18 (24) OVERLAY PALETTE
6 (8)
6 (8)
6 (8)
DAC
DAC
DAC
COMPARE
OPA
COMP
IOR
IOG
SETUP
IOB
SENSE*
475 / 471*
(477 / 471*)
ADDR REG
R
G
B
BUS CONTROL
8
6 (8)
6 (8)
6 (8)
D0 - D7
RD*
WR*
RS0
RS1
RS2

Product Description

The Bt475 and Bt477 RAMDACs are designed specifically for Personal System/2® compatible color graphics.

The Bt475 has a 256 x 18 lookup table RAM, 15 x 18 overlay registers, and triple 6-bit D/A converters.

The Bt477 has a 256 x 24 lookup table RAM, 15 x 24 overlay registers, and triple 8-bit D/A converters. Both 6-bit and 8-bit color modes are supported.

On-chip analog output comparators are included to simplify diagnostics and debugging, with the result output onto the SENSE* pin. Also included is an on-chip voltage reference to simplify using the device.

A power-down mode is available to reduce power requirements when the analog outputs are not used. This is useful in laptop computer systems that need the option of driving an external RGB monitor.

When the 475/471* input pin (477/471* on the Bt477) is floating or a logical zero, the Bt475 and Bt477 behave exactly as a Bt471 with anti-sparkle capabilities, on-chip reference, and analog comparators. When the pin is a logical one, the additional capabilities of the command register are available.

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Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L477001 Rev. E

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt475/477 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Table 1. The 8-bit address register is used to address the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the three bytes of color information are concatenated into a 18-bit or 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R,G,B write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. After the blue write cycle, the three bytes of color information are concatenated into a 18-bit or 24-bit word and written to the overlay location specified by the address register. The address register then increments to the next location which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R,G,B write cycles until the entire block has been written.

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM write mode)
0	1	1	address register (RAM read mode)
0	0	1	color palette RAM
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	command register*

Available only when the 475/471 (477/471*) pin is a logical one.

Table 1. Control Input Truth Table.

Circuit Description (continued)

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R,G,B read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the four most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. To reduce noticeable sparkling on the CRT screen during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between lookup table RAMs and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register, incremented following a blue read or write cycle, (ADDR0–7) are accessible to the MPU, and are used to address color palette RAM locations and overlay registers, as shown in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Note the pixel clock must be active for MPU accesses to the color palette RAM.

Bt471 Compatible Operation

If the 475/471* (477/471*) pin is a logical zero, the Bt475/477 operates as a Bt471 RAMDAC; the command register is disabled and 6-bit operation is selected. Color data is contained on the lower 6 bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero. Note that in the 6-bit mode, the Bt477's full scale output current will be about 1.5% lower than when in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being a logical zero in the 6-bit mode.

If the 475/471* (477/471*) input is a logical one, the command register is available. On the Bt477, the 6-bit/8-bit select bit in the command register may be used to specify whether 6-bit or 8-bit color data values are being used.

	Value	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00				red value
	01				green value
	10				blue value
ADDR0–7 (counts binary)	$00 - $FF	0	0	1	color palette RAM
	xxxx 0000	1	0	1	reserved
	xxxx 0001	1	0	1	overlay color 1
	:	:	:	:	:
	xxxx 1111	1	0	1	overlay color 15

Table 2. Address Register (ADDR) Operation.

Circuit Description (continued)

8-bit / 6-bit Color Selection

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

Note that in the 6-bit mode, the Bt477's full-scale output current will be about 1.5% lower than when in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being a logical zero in the 6-bit mode.

Power-Down Mode

The Bt475/477 incorporates a power-down capability, controlled by the SLEEP command bit. While the SLEEP bit is a logical zero, the Bt475/477 functions normally.

While the SLEEP bit is a logical one, the DACs and power to the RAM are turned off. Note that the RAM still retains the data. Also, the RAM may still be read or written to while sleeping as long as the pixel clock is running. The RAM automatically powers up during MPU read/write cycles, and shuts down when the MPU access is completed.

The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If using an external current reference, external circuitry should turn the current reference off (IREF = 0 mA) during sleep mode.

When using an external voltage reference, external circuitry should turn off the voltage reference (VREF = 0v) to further reduce power consumption due to biasing of portions of the internal voltage reference.

SENSE Output*

SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). This output is used to determine the presence of a CRT monitor and, via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 335 mV reference has a ± 5% tolerance (when using an external 1.235 V voltage reference). The tolerance is ± 10% when using the internal voltage reference or an external current reference. Note that SYNC* should be a logical zero for SENSE* to be stable.

Frame Buffer Interface

The P0–P7 and OL0–OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table 3. The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The addressed location provides 18 bits (Bt475) or 24 bits (Bt477) of color information to the three D/A converters.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs. This produces the specific output levels required for video applications, as illustrated in Figures 1–3. Tables 4–6 detail how the SYNC* and BLANK* inputs modify the output levels.

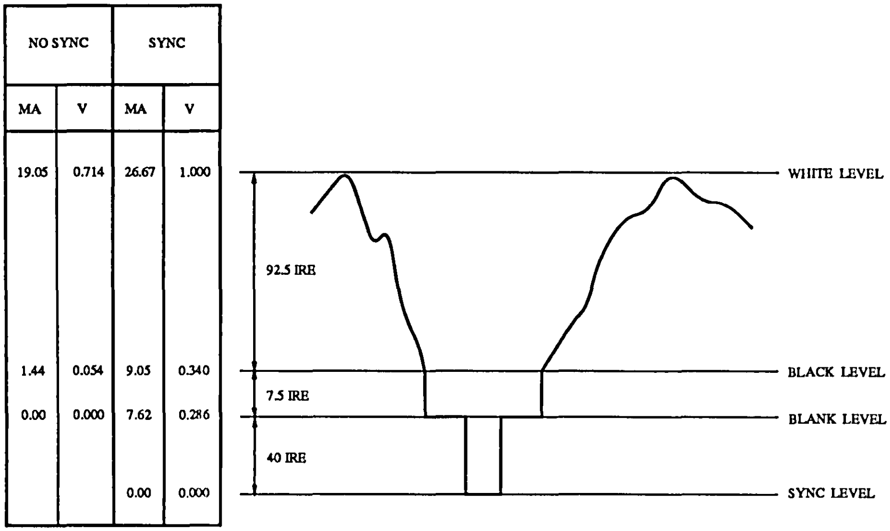
The SETUP input pin is logically ANDed with the SETUP command bit and is used to specify whether a 0 or 7.5 IRE blanking pedestal is to be used.

The analog outputs of the Bt475/477 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

OL0–OL3	P0–P7	Addressed by frame buffer
$0	$00	color palette RAM location $00
$0	$01	color palette RAM location $01
:	:	:
$0	$FF	color palette RAM location $FF
$1	$xx	overlay color 1
:	$xx	:
$F	$xx	overlay color 15

Table 3. Pixel and Overlay Control Truth Table.
(Pixel Read Mask Register = $FF)

Circuit Description (continued)


NO SYNC
SYNC
MA
V
MA
V
19.05
0.714
26.67
1.000
1.44
0.054
9.05
0.340
0.00
0.000
7.62
0.286
0.00
0.000
92.5 IRE
7.5 IRE
40 IRE
WHITE LEVEL
BLACK LEVEL
BLANK LEVEL
SYNC LEVEL

Note: 75 Ω doubly terminated load, SETUP = 7.5 IRE. VREF = 1.235 V, RSET = 147 Ω. RS-343A levels and tolerances are assumed on all levels.

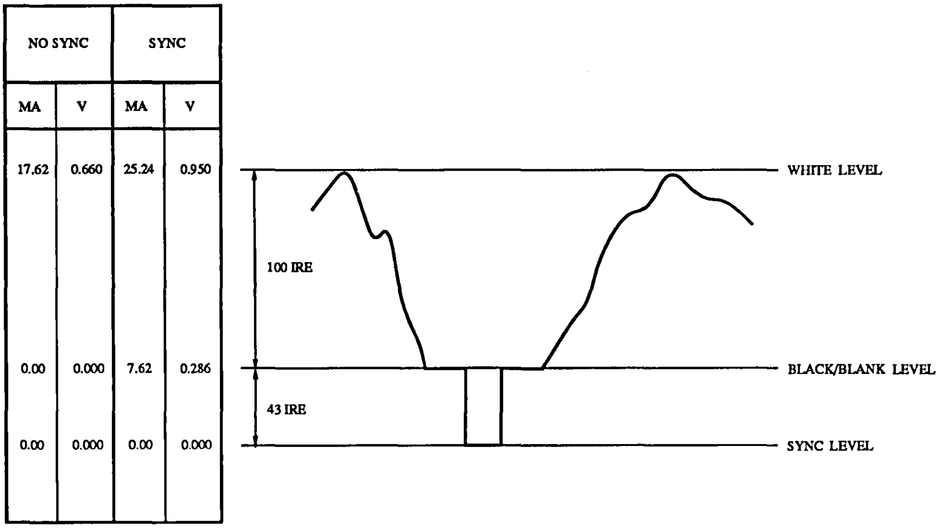
Figure 1. RS-343A Composite Video Output Waveforms (SETUP = 7.5 IRE).

Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	19.05	26.67	1	1	$FF
DATA	data + 1.44	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	1.44	9.05	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly terminated load, SETUP = 7.5 IRE. VREF = 1.235 V, RSET = 147 Ω.

Table 4. RS-343A Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description (continued)


NO SYNC
SYNC
MA
V
MA
V
17.62
0.660
25.24
0.950
0.00
0.000
7.62
0.286
0.00
0.000
0.00
0.000
100 IRE
43 IRE
WHITE LEVEL
BLACK/BLANK LEVEL
SYNC LEVEL

Note: 75 Ω doubly terminated load, SETUP = 0 IRE. VREF = 1.235V, RSET = 147 Ω. RS-343A levels and tolerances are assumed on all levels.

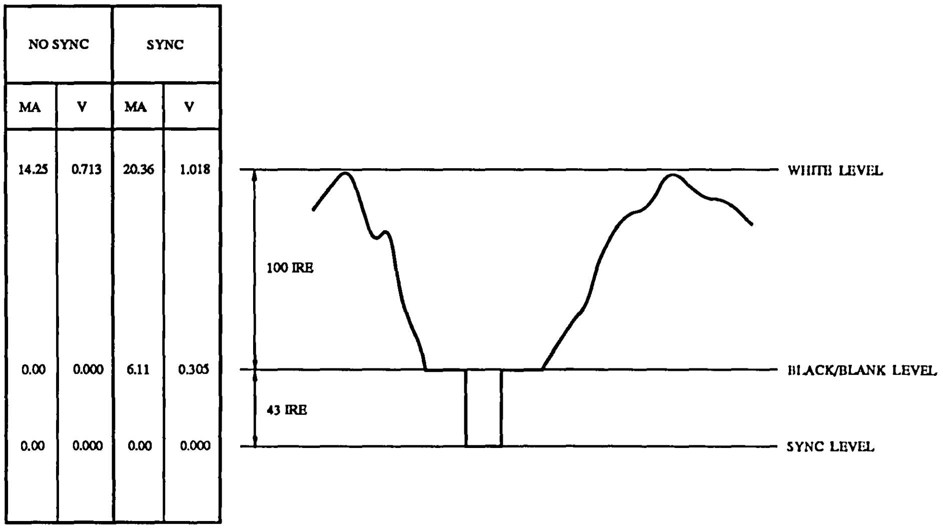
Figure 2. RS-343A Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly terminated load, SETUP = 0 IRE. VREF = 1.235 V, RSET = 147 Ω.

Table 5. RS-343A Video Output Truth Table (SETUP = 0 IRE).

Circuit Description (continued)


NO SYNC
SYNC
MA
V
MA
V
14.25
0.713
20.36
1.018
0.00
0.000
6.11
0.305
0.00
0.000
0.00
0.000
WHITE LEVEL
100 IRE
BLACK/BLANK LEVEL
43 IRE
SYNC LEVEL

Note: 50 Ω load, SETUP = 0 IRE. VREF = 1.235 V, RSET = 182 Ω. PS/2 levels and tolerances are assumed on all levels.

Figure 3. PS/2 Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	14.25	20.36	1	1	$FF
DATA	data	data + 6.11	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	6.11	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	6.11	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 50 Ω load, SETUP = 0 IRE. VREF = 1.235 V, RSET = 182 Ω.

Table 6. PS/2 Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

Command Register

This register is operational only while the 475/471* (477/471*) pin is a logical one. It may be written to or read by the MPU at any time and is not initialized.

D7	reserved (logical zero)	A logical zero must be written to this bit when writing to the command register to ensure proper operation.
D6	reserved (logical one)	A logical one must be written to this bit when writing to the command register to ensure proper operation.
D5	SETUP select (0) 0 IRE (1) 7.5 IRE	This bit specifies the blanking pedestal to be either 0 or 7.5 IRE. This bit is logically ANDed with the 475/471* (477/471*) input pin. Bit D5 controls the blanking pedestal only when in 475 (477) mode. The SETUP pin is disabled when operating inside this register.
D4	Blue sync enable (0) no sync on blue (1) sync on blue	This bit specifies whether the IOB output is to contain sync information or not.
D3	Green sync enable (0) no sync on green (1) sync on green	This bit specifies whether the IOG output is to contain sync information or not.
D2	Red sync enable (0) no sync on red (1) sync on red	This bit specifies whether the IOR output is to contain sync information or not.

Internal Registers (continued)

Command Register (continued)

D1	6-bit / 8-bit select (0) 6-bit (1) 8-bit	On the Bt477, this bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. On the Bt475, this bit must be a logical zero to ensure proper 6-bit operation.
D0	SLEEP enable (0) normal operation (1) sleep mode	While this bit is a logical zero, the Bt475/477 functions normally. If this bit is a logical one, the DACs and power to the RAM are turned off. Note that the RAM still retains the data. Also, the RAM may be read or written to as long as the pixel clock is running. The RAM automatically powers-up during MPU read/write cycles, and shuts down when the MPU access is completed. It requires about 1 second for the Bt475/477 to output valid video data after enabling normal operation (coming out of sleep mode). This time will vary depending on the size of the COMP capacitor. The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If using an external current reference, external circuitry should turn the current reference off during sleep mode.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 4, 5, and 6. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input (TTL compatible). Used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal. This pin should not be left floating.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 1, 2, and 3). SYNC* does not override any other control or data input, as shown in Tables 4, 5, and 6; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not required on the video outputs, SYNC* should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0–OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
P0 - P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0 - OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Table 3. When accessing the overlay palette, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
COMP	Compensation pin. If an external or the internal voltage reference is used (Figures 4 and 5), this pin should be connected to OPA. If an external current reference is used (Figure 6), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *Refer to PC Board Layout Considerations for critical layout criteria.*
VREF	Voltage reference input. If an external voltage reference is used (Figure 5), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 6), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor is used to decouple this input to GND, as shown in Figures 4 and 5. If the VAA supply is very clean, better performance may be obtained by decoupling VREF to VAA. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When using the internal reference, this pin should not drive any external circuitry, except for the decoupling capacitor (Figure 4).
OPA	Reference amplifier output. If an external or the internal voltage reference is used (Figures 4 and 5), this pin must be connected to COMP. When using an external current reference (Figure 6), this pin should be left floating.
IOR, IOG, IOB	Red, green, and blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figures 4, 5, and 6).
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)

Pin Name	Description
IREF	Full scale adjust control. Note that the IRE relationships in Figures 1, 2, and 3 are maintained, regardless of the full scale output current.

When using an external or the internal voltage reference (Figures 4 and 5), a resistor (RSET) connected between this pin and GND controls the magnitude of the full scale video signal. The relationship between RSET and the full scale output current on each output is:

RSET (Ω) = K * 1,000 * VREF (V) / Iout (mA)

K is defined in the table below. It is recommended that a 147 Ω RSET resistor be used for doubly terminated 75 Ω loads (i.e., RS-343A applications). For PS/2 applications (i.e., 0.7 V into 50 Ω with no sync), a 182 Ω RSET resistor is recommended.

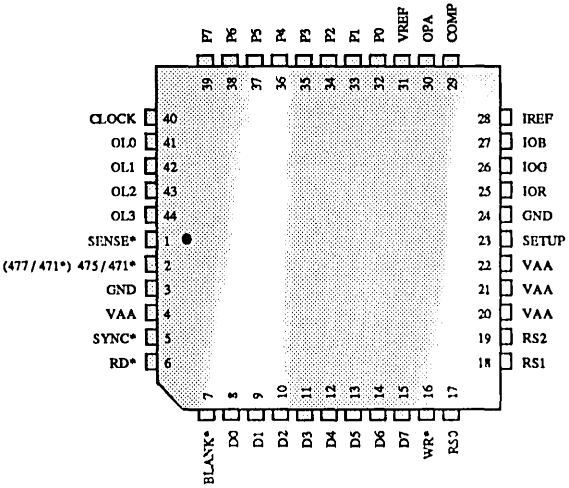
When using an external current reference (Figure 6), the relationship between IREF and the full scale output current on each output is:

IREF (mA) = Iout (mA) / K

Part	Mode	Pedestal	K (with sync)	K (no sync)
Bt477	6-bit	7.5 IRE	3.170	2.26
	8-bit	7.5 IRE	3.195	2.28
	6-bit	0 IRE	3.000	2.10
	8-bit	0 IRE	3.025	2.12
Bt475	(6-bit)	7.5 IRE	3.170	2.26
		0 IRE	3.000	2.10

Pin Name	Description
WR*	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously.
RD*	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously.
RS0, RS1, RS2	Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as illustrated in Tables 1 and 2.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
475/471* (477/471*)	Bt475 (Bt477) or B471 select input (TTL compatible). When the 475/471* (477/471*) input pin is floating or a logical zero, the Bt475/477 behaves exactly as a Bt471 with anti-sparkle capabilities. When the 475/471* (477/471*) input pin is a logical one, the extra capabilities of the Bt475/477 command register are available.
SENSE*	Sense output (CMOS compatible). SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). Note that SENSE* may not be stable while SYNC* is toggling.

Pin Descriptions (continued)


P7
P6
P5
P4
P3
P2
P1
P0
VREF
OPA
COMP
39
38
37
36
35
34
33
32
31
30
29
CLOCK 40
OL0 41
OL1 42
OL2 43
OL3 44
SENSE* 1
(477/471*) 475/471* 2
GND 3
VAA 4
SYNC* 5
RD* 6
28 IREF
27 IOB
26 IOG
25 IOR
24 GND
23 SETUP
22 VAA
21 VAA
20 VAA
19 RS2
18 RS1
7
8
9
10
11
12
13
14
15
16
17
BLANK*
D0
D1
D2
D3
D4
D5
D6
D7
WR*
RS0

Names in parentheses are pin names for the Bt477.

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in Bt451/7/8 Evaluation Module Operation and Measurements, application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt475/477 power and ground lines by shielding the digital inputs and providing good decoupling. Trace lengths between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a four-layer PC board is recommended with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

The optimum layout enables the Bt475/477 to be located as close to the power supply connector and the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8-inch gap) connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground tub isolation technique is constrained by the noise margin degradation during digital readback of the Bt475/477.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

The analog ground plane should include all Bt475/477 ground pins, all reference circuitry and decoupling (external reference if used, RSET resistors, etc.), power supply bypass circuitry for the Bt475/477, analog output traces, and the video output connector.

Power Planes

A separate digital and analog power plane is necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt475/477 power pins, any reference circuitry, and COMP and reference decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 4, 5, and 6. This bead should be located within 3 inches of the Bt475/477 and provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.001 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device.

The 10 µF capacitor is for low frequency power supply ripple; the 0.1 µF capacitors are for high frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that power supply hum and ripple noise less than 1 MHz will couple about 10% of the noise onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 μF ceramic chip capacitor. Low frequency supply noise will require a larger value. Lead lengths should be minimized for best performance.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt475/477 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt475/477 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt475/477 to minimize reflections. Unused analog outputs should be connected to GND.

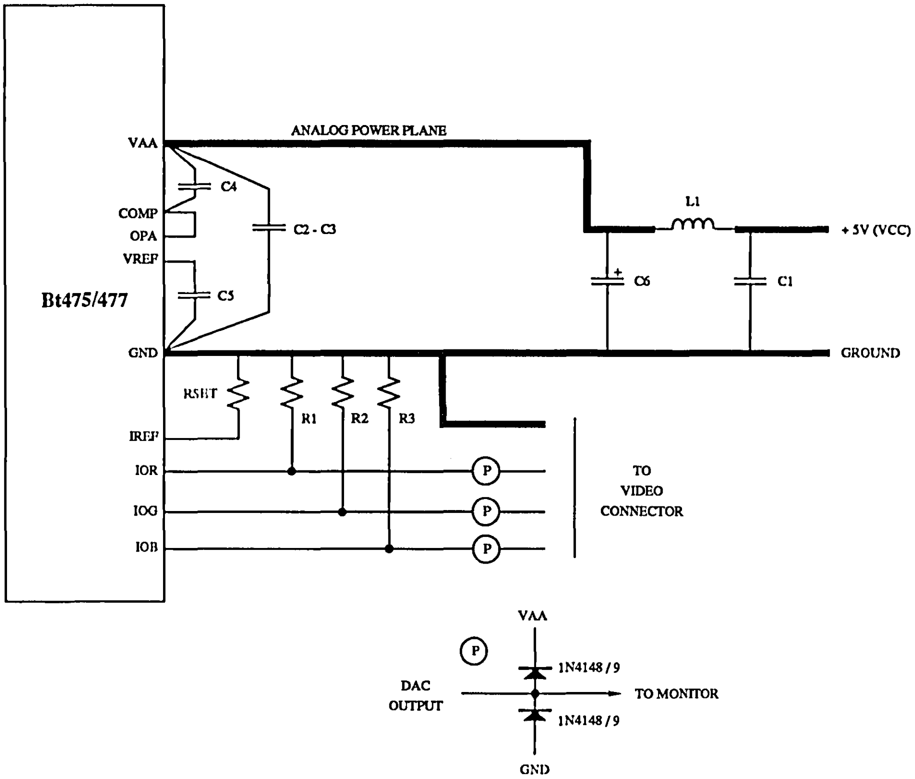
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, helping to alleviate EMI and noise problems.

Analog Output Protection

The Bt475/477 analog outputs should be protected against high energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figures 4, 5, and 6 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)

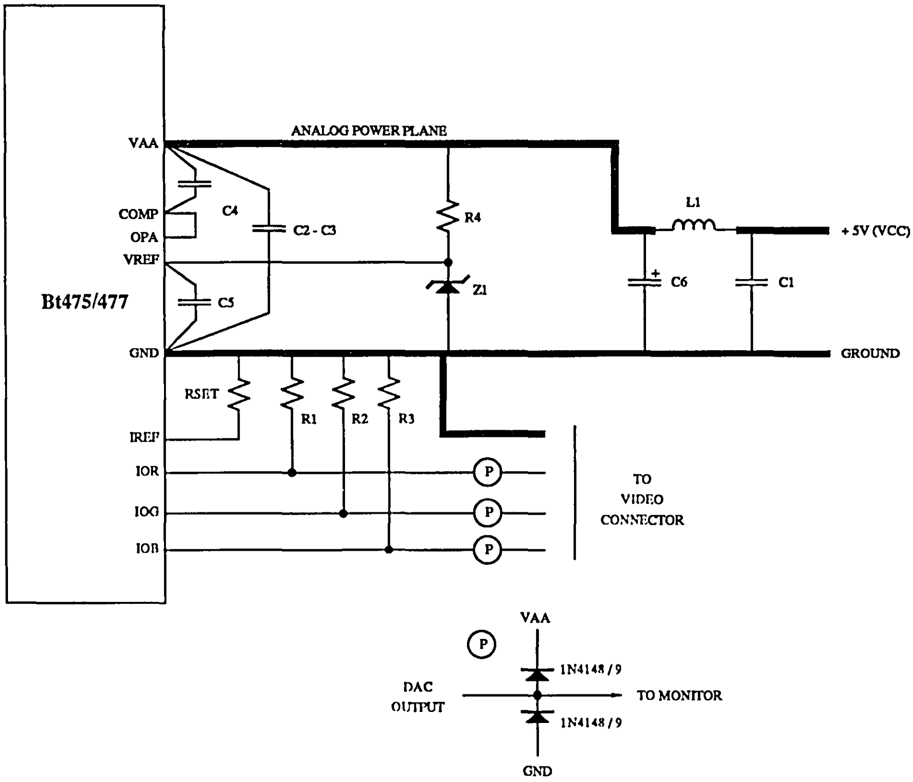

ANALOG POWER PLANE
VAA
COMP
OPA
VREF
Bt475/477
GND
C4
C2 - C3
C5
L1
+5V (VCC)
C6
C1
GROUND
RSET
R1
R2
R3
IREF
IOR
IOG
IOB
P
TO
VIDEO
CONNECTOR
VAA
P
1N4148/9
DAC
OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt475/477.

Figure 4. Typical Connection Diagram and Parts List (Internal Voltage Reference).

PC Board Layout Considerations (continued)

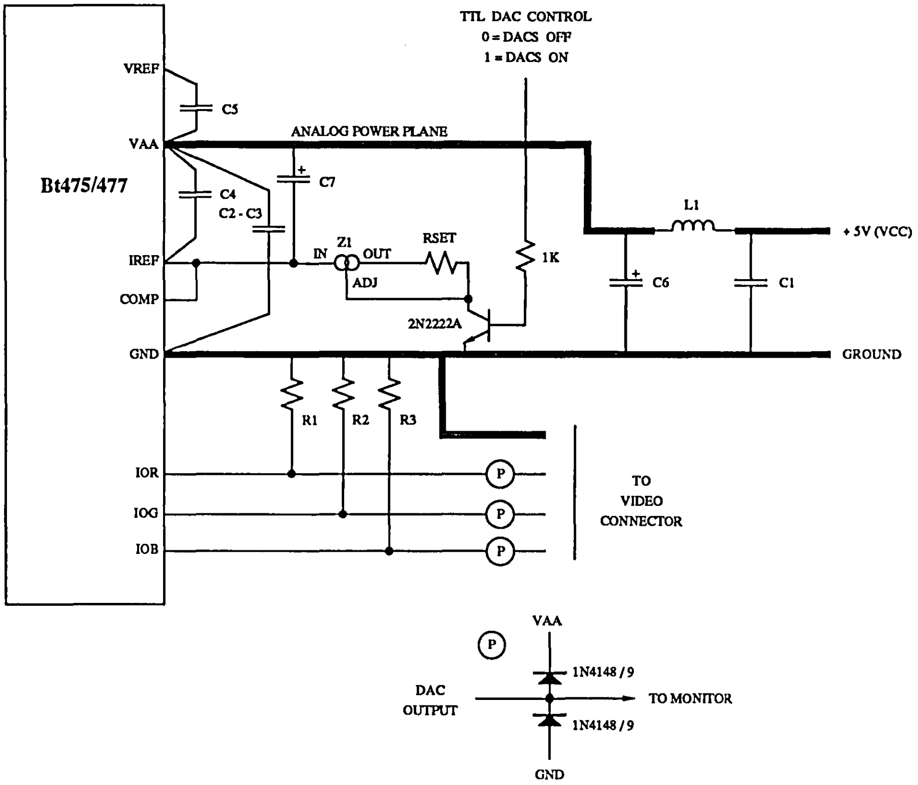

Bt475/477
VAA
COMP
OPA
VREF
GND
IREF
IOR
IOG
IOB
ANALOG POWER PLANE
C4
C2 - C3
C5
R4
Z1
L1
+5V (VCC)
C6
C1
GROUND
RSET
R1
R2
R3
P
TO VIDEO CONNECTOR
VAA
P
1N4148/9
DAC OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt475/477.

Figure 5. Typical Connection Diagram and Parts List (External Voltage Reference).

PC Board Layout Considerations (continued)


TTL DAC CONTROL
0 = DACS OFF
1 = DACS ON
VREF
C5
VAA
ANALOG POWER PLANE
Bt475/477
C7
C4
C2 - C3
L1
+5V (VCC)
Z1
IN
OUT
ADJ
RSET
1K
IREF
C6
C1
COMP
2N2222A
GND
GROUND
R1
R2
R3
IOR
IOG
IOB
P
TO
VIDEO
CONNECTOR
VAA
1N4148/9
DAC
OUTPUT
TO MONITOR
GND

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
C7, C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM317LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt475/477.

Figure 6. Typical Connection Diagram and Parts List (External Current Reference).

Application Information

Using Multiple Devices

When using multiple Bt475/477s, each Bt475/477 should have its own power plane ferrite bead. If using the internal reference, each Bt475/477 should use its own internal reference.

Although the multiple Bt475/477s may be driven by a common external voltage/current reference, higher performance may be obtained if each RAMDAC uses its own reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt475/477 must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

ESD and Latch-up Considerations

Correct ESD sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latch-up can be prevented by assuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Reference Selection

An external voltage reference provides about 10 times better power supply rejection on the analog outputs than an external current reference.

Sleep Operation

When using the internal or external voltage reference, the DACs will be turned off during sleep mode.

When using an external voltage reference, some internal circuitry will still be powered during the sleep mode, resulting in 0.5 mA of power supply current being drawn (above the rated supply current specifications). This unnecessary current drain can be disabled by turning off the external voltage reference during sleep mode.

When using an external current reference, the DACs are not turned off during the sleep mode. To disable the DACs during sleep mode, the current reference must be turned off. As shown in Figure 6, a TTL signal and the 2N2222 transistor are used to disable the current reference during sleep mode.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
80, 66 MHz Parts		4.75	5.00	5.25	Volts
50, 35 MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ohms
Voltage Reference Configuration					
Reference Voltage	VREF	1.14	1.235	1.26	Volts
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		–3	–8.39	–10	mA
PS/2 Compatible		–3	–8.88	–10	mA

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)					
Bt475		6	6	6	Bits
Bt477		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL				
Bt475				±1/4	LSB
Bt477				±1	LSB
Differential Linearity Error	DL				
Bt475				±1/4	LSB
Bt477				±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			-1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = -400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current					
White Level Relative to Black*		16.74	17.62	18.50	mA
Black Level Relative to Blank					
Setup = 7.5 IRE		0.95	1.44	1.90	mA
Setup = 0 IRE		0	5	50	µA
Blank Level					
Sync Enabled		6.29	7.62	8.96	mA
Sync Disabled		0	5	50	µA
Sync Level		0	5	50	µA
LSB Size					
Bt475			279.68		µA
Bt477			69.1		µA
DAC to DAC Matching			2	5	%
Output Compliance	VOC	−1.0		+1.5	Volts
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Internal Reference Output	VREF	1.1	1.235	1.3	V
Power Supply Rejection Ratio** (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, 475/471* (477/471*) pin = logical one. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note: When using the internal voltage reference, RSET may need to be adjusted to meet these limits. Also, the "gray-scale" output current (white level relative to black) will have a typical tolerance of ±10% rather than the ±5% specified above.

*Since the Bt475 have 6-bit DACs (and the Bt477 in the 6-bit mode), the output levels are approximately 1.5% lower than these values.

**Guaranteed by characterization, not tested.

AC Characteristics

Parameter	Symbol	80 MHz Devices Min	80 MHz Devices Typ	80 MHz Devices Max	66 MHz Devices Min	66 MHz Devices Typ	66 MHz Devices Max	Units
Clock Rate	Fmax			80			66	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*p13			6*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	12.5			15.15			ns
Clock Pulse Width High Time	14	4			5			ns
Clock Pulse Width Low Time	15	4			5			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		13			13		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			75			75		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
SENSE* Output Delay	19		1			1		µS
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA							
normal operation			180	220		180	220	mA
sleep enabled***			5	10		5	10	mA

See test conditions on page 4 - 478.
See also Figure 8.

AC Characteristics (continued)

		50 MHz Devices			35 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			50			35	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*p13			6*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	20			28			ns
Clock Pulse Width High Time	14	6			7			ns
Clock Pulse Width Low Time	15	6			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		20			28		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			75			75		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
SENSE* Output Delay	19		1			1		µS
Pipeline Delay		4	4	4	4	4	4	Clocks
VAA Supply Current**	IAA							
normal operation			180	220		180	220	mA
sleep enabled***			5	10		5	10	mA

See test conditions on next page.
See also Figure 8.

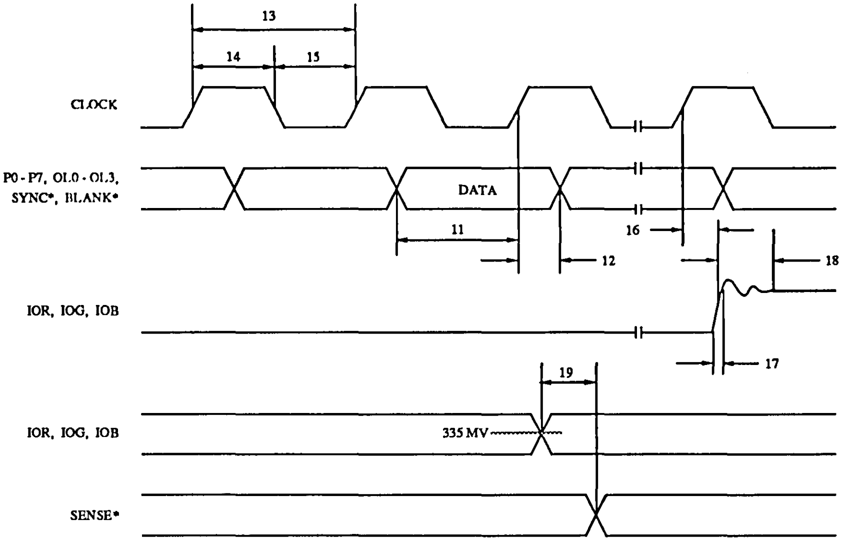
AC Characteristics (continued)

Test conditions (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, 475/471* (477/471*) pin = logical one. TTL input values are 0 to 3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points are at 50% for inputs and outputs. Analog output load ≤ 10 pF. SENSE*, D0–D7 output load ≤ 75 pF. See timing notes in Figure 7. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1k Ω resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA (max).

***External current or voltage reference disabled during sleep mode. Test Conditions: +25° to +70° C, pixel and data ports at 0.4 V.



Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.

Note 2: Settling time measured from the 50% point of full scale transition to the output remaining within ±1 LSB (Bt477) or ±1/4 LSB (Bt475).

Note 3: Output rise/fall time measured between the 10% and 90% points of full scale transition.

Figure 7. Video Input/Output Timing.

Timing Waveforms

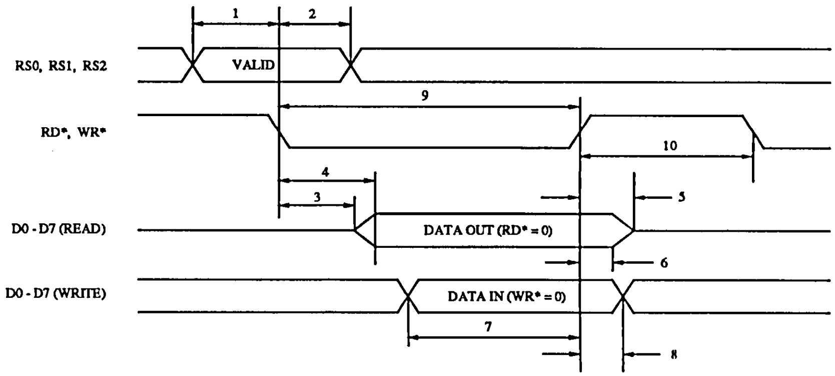

1
2
RS0, RS1, RS2
VALID
9
RD*, WR*
10
4
3
5
D0 - D7 (READ)
DATA OUT (RD* = 0)
6
D0 - D7 (WRITE)
DATA IN (WR* = 0)
7
8

Figure 8. MPU Read/Write Timing.

Ordering Information

Model Number	Color Palette RAM	Overlay Palette	Speed	Package	Ambient Temperature Range
Bt475KPJ80	256 x 18	15 x 18	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt475KPJ66	256 x 18	15 x 18	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt475KPJ50	256 x 18	15 x 18	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt475KPJ35	256 x 18	15 x 18	35 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt477KPJ80	256 x 24	15 x 24	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt477KPJ66	256 x 24	15 x 24	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt477KPJ50	256 x 24	15 x 24	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt477KPJ35	256 x 24	15 x 24	35 MHz	44-pin Plastic J-Lead	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
B	Bt475 added to specification.
C	Bit D5 controls the Blanking Pedestal only when the Command Register is operational. Maximum, minimum, and typical Internal VREF output voltages are added.
D	VAA supply currents with sleep enabled are corrected to 5 mA typical. Temperatures under which tests are conducted are +25° to +70° C while pixel and data ports are at 0.4 V. RD*/WR* pulse width high times are changed to 6* Clock Cycle Time for all accesses. The command register bit D6 is reserved and must be a logical one to ensure proper operation.
E	In PCB layout section, figures 4 and 5 now have VREF decoupled to GND. Revised DC Characteristics.

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt479

80 MHz
1024 x 24 Color Palette
Personal System/2®
WindowVu™ RAMDAC™

Distinguishing Features

- Bt471/476/478 Pin Compatible
- 80, 66, 50, 35 MHz Operation
- Triple 8-bit D/A Converters
- 1024 x 24 Color Palette RAM
- 16-Window Priority Encoder
- 15 Overlay Registers
- Sync Enable/Disable for Each Channel
- Programmable Pedestal
- On-Chip Analog Output Comparators
- Anti-Sparkle Circuitry
- Automatic Sync Polarity Detection
- 44-pin PLCC Package

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Product Description

The Bt479 RAMDAC is designed specifically for Personal System/2® compatible color graphics.

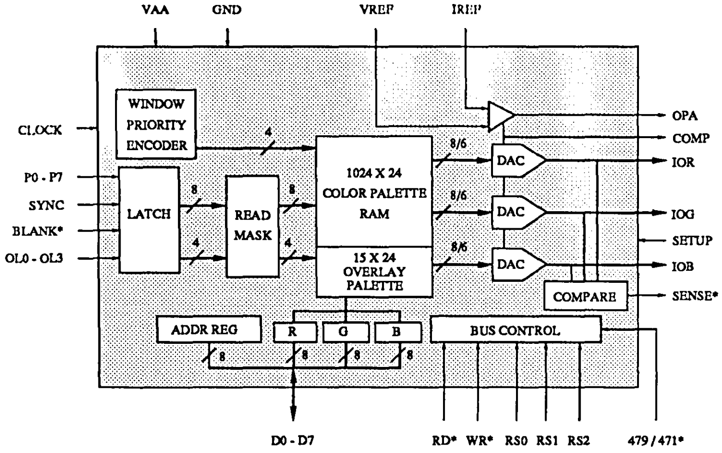
It supports up to 1,024 simultaneous colors out of a 16.8 million color palette through the 1K x 24 color palette RAM and triple 8-bit D/A converters.

The Bt479 may also be configured to display up to 16 windows (plus background), with flexible color palette control. An on-chip 16 window priority encoder provides window display priority, color palette selection, and window placement (with pixel resolution).

The 479/471* pin enables the Bt479 to emulate the Bt471 RAMDAC, and it is fully software-compatible and pin-compatible with the Bt471.

Additional features include up to 15 overlay registers to provide for overlaying cursors, grids, menus, EGA emulation, etc. Also supported is sync generation on all three channels (with each channel independently enabled or disabled), and a programmable pedestal (0 or 7.5 IRE).

Functional Block Diagram


VAA
GND
VREF
IREF
WINDOW PRIORITY ENCODER
CLOCK
P0 - P7
SYNC
BLANK*
OL0 - OL3
LATCH
READ MASK
8
4
1024 X 24 COLOR PALETTE RAM
15 X 24 OVERLAY PALETTE
8/6
DAC
OPA
COMP
IOR
IOG
SETUP
IOB
SENSE*
COMPARE
ADDR REG
R
G
B
BUS CONTROL
D0 - D7
RD*
WR*
RS0
RS1
RS2
479 / 471*

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Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L479001 Rev. E

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt479 supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Tables 1 and 2. The 8-bit address register is used to address the color palette RAM, overlay registers, and control registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Four additional bits in the command register are used to specify which one of four segments of the color palette RAM is being accessed by the MPU as shown in Table 2. Note that when accessing a block of more than 256 colors, the command register must be updated to select the appropriate one of four 256-color segments.

Writing Color Palette RAM Data

To write color data, the MPU loads the address register (RAM write mode) and optionally command register_0 (see Table 2) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register and command register_0. The address register (ADDR0–ADDR7) then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) and optionally command register_0 (see Table 2) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers and the address register (ADDR0–ADDR7) is incremented to the next RAM location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register and command register_0 are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Writing Overlay Color Data

To write overlay color data, the MPU loads the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the overlay location specified by the address register. The address register (ADDR0–ADDR7) then increments to the next location, which the MPU may modify by simply writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous R, G, B write cycles until the entire block has been written.

Reading Overlay Color Data

To read overlay color data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers and the address register (ADDR0–ADDR7) is incremented to the next overlay location. The MPU performs three successive read cycles (8 bits each of red, green, and blue), using RS0–RS2 to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous R, G, B read cycles until the entire block has been read.

Circuit Description (continued)

Writing Control Register Data

To write control register data, the MPU loads the address register (RAM write mode) with the address of the control register to be modified. The MPU performs a write cycle, using RS0–RS2 to select the control registers. After the write cycle, the address register (ADDR0–ADDR7) then increments to the next location, which the MPU may modify by simply writing another byte of data. A block of data in consecutive control registers may be written to by writing the start address and performing continuous write cycles until the entire block has been written.

Reading Control Register Data

To read control register data (except the pixel or overlay read mask register), the MPU loads the address register with the address of the control register to be read. The MPU performs a read cycle, using RS0–RS2 to select the control registers. After the read cycle, the address register (ADDR0–ADDR7) then increments to the next location, which the MPU may read by simply reading another byte of data. A block of data in consecutive control registers may be read by writing the start address and performing continuous read cycles until the entire block has been read.

Additional Information

When accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While accessing the overlay color registers, the four most significant bits of the address register (ADDR4–7) are ignored.

When accessing the control registers, the address register resets to $00 following a read or write cycle to address $FF. Data written to reserved locations are ignored; data read from reserved locations returns invalid data.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic, and occur in the period between MPU accesses. To reduce noticeable sparkling on the CRT screen during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between lookup table RAMs and the RGB registers occurs. Accessing of the control registers causes no disturbance on the display screen.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (ADDRa, ADDRb) that count modulo three, as shown in Table 2. The MPU does not have access to these bits. They are reset to zero when the MPU writes to the address register, and are not reset to zero when the MPU reads the address register. The other 8 bits of the address register (ADDR0–7), incremented following a blue read or write cycle, are accessible to the MPU and are used to address color palette RAM locations and overlay registers, as shown in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode.

Bt471 Compatible Operation

If the 479/471* pin is a logical zero, the Bt479 operates as a Bt471 RAMDAC; the command register is disabled and 6-bit operation is selected. Color data is contained on the lower 6 bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero. Note that in the 6-bit mode, the Bt479's full-scale output current will be about 1.5% lower than when in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being a logical zero in the 6-bit mode. (See Table 3.)

If the 479/471* input is a logical zero, the additional control registers are available, however, the contents of the control register will not effect the operation of the device.

Circuit Description (continued)

8-bit / 6-bit Color Selection

For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus, with D0 being the LSB and D5 the MSB of color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 are a logical zero.

Note that in the 6-bit mode, the Bt479's full-scale output current will be about 1.5% lower than when in the 8-bit mode. This is due to the 2 LSBs of each 8-bit DAC always being a logical zero in the 6-bit mode.

The 6-bit / 8-bit mode selection (available only while the 479/471* pin is a logical one) enables mixing 6-bit and 8-bit color data in the color palette RAM.

SENSE Output*

SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded 335 mV. This output is used to determine the presence of a CRT monitor and via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 335 mV reference has a ±5% tolerance (when using an external 1.235 V voltage reference). The tolerance is ±10% when using an external current reference. Note that SYNC* should be a logical zero for SENSE* to be stable.

Pixel Read Mask Register

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The contents of the overlay read mask bits in the command register are bit-wise logically ANDed with the OL0–OL3 inputs. The addressed RAM/overlay location provides 24 bits of color information to the three D/A converters. The pixel read mask register is written to by setting RS2–RS0 to 010, as in Table 1.

Note that the P0–P7 pixel read mask bits are accessed directly, not through the address register.

Window Priority Encoder

Each window is controlled by four window control registers. The location of each window is specified by its top/left and bottom/right (x,y) coordinates, as shown in Figure 1 and Table 6. To arbitrate overlapping windows, the priority of the window is the window number, with window_0 having the highest priority, and window_15 the lowest priority.

The Bt479 monitors the BLANK* input to determine the current display position (with pixel resolution). The window positions and sizes are compared to the current display position to determine which windows are being displayed. The window being displayed with the highest priority, in conjunction with P0–P7, addresses the color palette RAM.

If no window is being displayed for the current pixel, color palette addresses $000–$0FF (palette 0) are used, addressed by P0–P7.

Command bits CR10, CR16, and CR17 control the window and color palette RAM functions, as shown in Tables 4 and 5.

Circuit Description (continued)

Frame Buffer Interface

The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The contents of the overlay read mask bits in the command register are bit-wise logically ANDed with the OL0–OL3 inputs. The addressed RAM/overlay location provides 24 bits of color information to the three D/A converters.

The SYNC and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as illustrated in Figures 2, 3, and 4. Tables 7, 8, and 9 detail how the SYNC and BLANK* inputs modify the output levels.

The SETUP input pin specifies whether a 0 or 7.5 IRE blanking pedestal is to be used.

The analog outputs of the Bt479 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (RAM / control register write mode)
0	1	1	address register (RAM / control register read mode)
0	0	1	color palette RAM
0	1	0	pixel read mask register
1	0	0	address register (overlay write mode)
1	1	1	address register (overlay read mode)
1	0	1	overlay registers
1	1	0	control registers*

The Bt479-specific control registers may still be accessed by the MPU while the 479/471 pin is a logical zero; however, the contents of the control registers will not affect the operation of the device.

Table 1. Control Input Truth Table.

Circuit Description (continued)

	Value	CR07–CR04 (Command Register_0)	RS2	RS1	RS0	Addressed by MPU
ADDRa, b (counts modulo 3)	00		x	0	1	red value
	01		x	0	1	green value
	10		x	0	1	blue value
ADDR0–7 (counts binary)	$00–$FF	0000	0	0	1	RAM address $000–$0FF *
	$00–$FF	0001	0	0	1	RAM address $100–$1FF *
	$00–$FF	0010	0	0	1	RAM address $200–$2FF *
	$00–$FF	0011	0	0	1	RAM address $300–$3FF *
	$x0	xxxx	1	0	1	flood color *
	$x1	xxxx	1	0	1	overlay color 1 *
	:	:	:	:	:	:
	$xF	xxxx	1	0	1	overlay color 15 *
	$00	0000	1	1	0	window(0) x1 low
	$01	0000	1	1	0	window(0) x1 high
	$02	0000	1	1	0	window(0) x2 low
	$03	0000	1	1	0	window(0) x2 high
	$04	0000	1	1	0	window(0) y1 low
	$05	0000	1	1	0	window(0) y1 high
	$06	0000	1	1	0	window(0) y2 low
	$07	0000	1	1	0	window(0) y2 high
	$08	0000	1	1	0	window(1) x1 low
	$09	0000	1	1	0	window(1) x1 high
	$0A	0000	1	1	0	window(1) x2 low
	$0B	0000	1	1	0	window(1) x2 high
	$0C	0000	1	1	0	window(1) y1 low
	$0D	0000	1	1	0	window(1) y1 high
	$0E	0000	1	1	0	window(1) y2 low
	$0F	0000	1	1	0	window(1) y2 high
	:	:	:	:	:	:
	$78	0000	1	1	0	window(15) x1 low
	$79	0000	1	1	0	window(15) x1 high
	$7A	0000	1	1	0	window(15) x2 low
	$7B	0000	1	1	0	window(15) x2 high
	$7C	0000	1	1	0	window(15) y1 low
	$7D	0000	1	1	0	window(15) y1 high
	$7E	0000	1	1	0	window(15) y2 low
	$7F	0000	1	1	0	window(15) y2 high
	$80	xxxx	1	1	0	reserved
	$81	xxxx	1	1	0	reserved
	$82	xxxx	1	1	0	command register_0
	$83	xxxx	1	1	0	command register_1
	$84	xxxx	1	1	0	flood register low
	$85	xxxx	1	1	0	flood register high

*Requires three read/write cycles — R, G, B.

Table 2. Address Register (ADDR) Operation (479/471 = Logical One).*

Circuit Description (continued)

OL3–OL0	P0–P7	Addressed by frame buffer
0000	$00	color palette RAM location $000
0000	$01	color palette RAM location $001
:	:	:
0000	$FF	color palette RAM location $0FF
0001	$xx	overlay color 1
0010	$xx	overlay color 2
:	:	:
1111	$xx	overlay color 15

Table 3. Pixel and Overlay Control Truth Table (479/471 = Logical Zero).*

Command Register Bits for Color Palette and Window Configuration Selection			RA0–RA9 = 10-bit Address to 1K x 24 Color Palette RAM W0–W3 = Color Palette Selection From Window Priority Encoder P0–P7 = Pixel Inputs OL0–OL3 = Overlay Inputs										
CR10	CR17	CR16	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Window Mode
1	1	1	W3	W2	W1	W0	0	0	P3	P2	P1	P0	(16) 4-bit color palettes
1	1	0	W3	W2	W1	W0	P5	P4	P3	P2	P1	P0	(16) 6-bit color palettes
1	0	1											reserved
1	0	0	W3	W2	P7	P6	P5	P4	P3	P2	P1	P0	(4) 8-bit color palettes
0	1	1											reserved
0	1	0											reserved
0	0	1											reserved
0	0	0	OL3	OL2	P7	P6	P5	P4	P3	P2	P1	P0	(1) 10-bit color palette

Note: RA0–RA9 refer to 10-bit address for 1K x 24 color palette RAM (RA0 is the least significant address bit). Numbers in parentheses under Window Mode indicate number of windows available.

Table 4. Windowing Control Truth Table (479/471 = Logical One).*

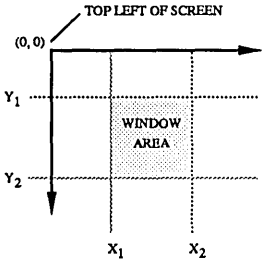
Circuit Description (continued)

CR10	CR17	CR16	OL3	OL2	OL1	OL0	RA9–RA0	Addressed by Frame Buffer
1	x	x	0	0	0	0	00 0000 0000	color palette RAM location $000
1	x	x	0	0	0	0	00 0000 0001	color palette RAM location $001
:	:	:	:	:	:	:	:	:
1	x	x	0	0	0	0	11 1111 1111	color palette RAM location $3FF
1	x	x	0	0	0	1	xx xxxx xxxx	overlay color 1
1	x	x	0	0	1	0	xx xxxx xxxx	overlay color 2
:	:	:	:	:	:	:	:	:
1	x	x	1	1	1	1	xx xxxx xxxx	overlay color 15
0	x	x	-	-	0	0	00 0000 0000	color palette RAM location $000
0	x	x	-	-	0	0	00 0000 0001	color palette RAM location $001
:	:	:	:	:	:	:	:	:
0	x	x	-	-	0	0	11 1111 1111	color palette RAM location $3FF
0	x	x	-	-	0	1	xx xxxx xxxx	overlay color 1
0	x	x	-	-	1	0	xx xxxx xxxx	overlay color 2
0	x	x	-	-	1	1	xx xxxx xxxx	overlay color 3

Note: RA0–RA9 refer to 10-bit address to 1K x 24 color palette RAM (RA0 is the least significant address bit). CR10, CR16, and CR17 are command register_1 control bits.

Table 5. Pixel and Overlay Control Truth Table (479/471 = Logical One).*

Circuit Description (continued)



NOTE: $Y_1 < Y_2$ AND $X_1 < X_2$

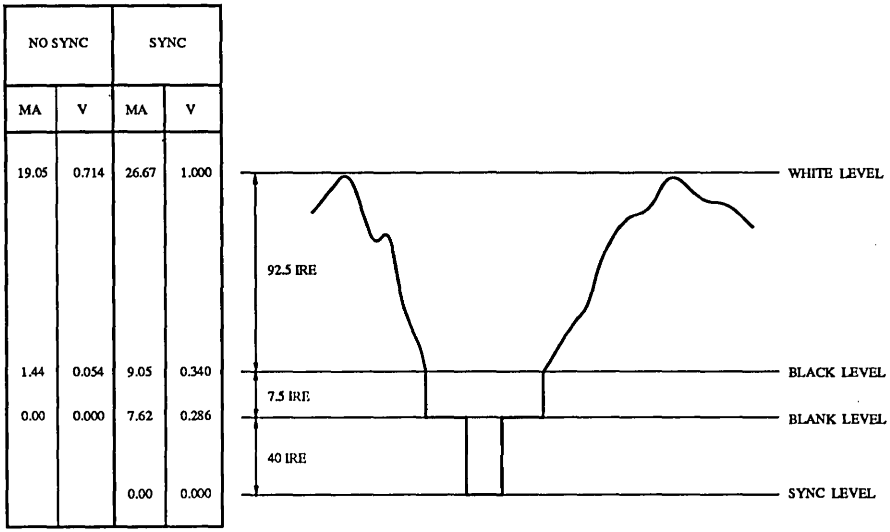
Figure 1. Window Boundary Example.

Priority Number	ADDR Starting Address	14-bit x1 Register		14-bit x2 Register		12-bit y1 Register		12-bit y2 Register	
0	$00	W3, W2, x11–x8	x7–x0	W1, W0, x11–x8	x7–x0	y11–y8	y7–y0	y11–y8	y7–y0
1	$08	:		:		:		:	
2	$10	:		:		:		:	
3	$18	:		:		:		:	
4	$20	:		:		:		:	
5	$28	:		:		:		:	
6	$30	:		:		:		:	
7	$38	:		:		:		:	
8	$40	:		:		:		:	
9	$48	:		:		:		:	
10	$50	:		:		:		:	
11	$58	:		:		:		:	
12	$60	:		:		:		:	
13	$68	:		:		:		:	
14	$70	:		:		:		:	
15	$78	W3, W2, x11–x8	x7–x0	W1, W0, x11–x0	x7–x0	y11–y8	y7–y0	y11–y8	y7–y0
		High Byte	Low Byte	High Byte	Low Byte	High Byte	Low Byte	High Byte	Low Byte
Starting Address Offset		+1	+0	+3	+2	+5	+4	+7	+6

Note: W0–W3 specify the color palette selection for the corresponding window. Refer to Internal Registers section for further information.

Table 6. Window Priority Encoder Register Organization.

Circuit Description (continued)


NO SYNC
SYNC
MA
V
MA
V
19.05
0.714
26.67
1.000
1.44
0.054
9.05
0.340
0.00
0.000
7.62
0.286
0.00
0.000
92.5 IRE
7.5 IRE
40 IRE
WHITE LEVEL
BLACK LEVEL
BLANK LEVEL
SYNC LEVEL

Note: 75 Ω doubly terminated load, SETUP = 7.5 IRE. RS-343A standard levels and tolerances assumed on all levels. These levels will yield an RSET ~ 147 Ω given a VREF = 1.235 V (See IREF pin description).

Figure 2. RS-343A Composite Video Output Waveforms (SETUP = 7.5 IRE).

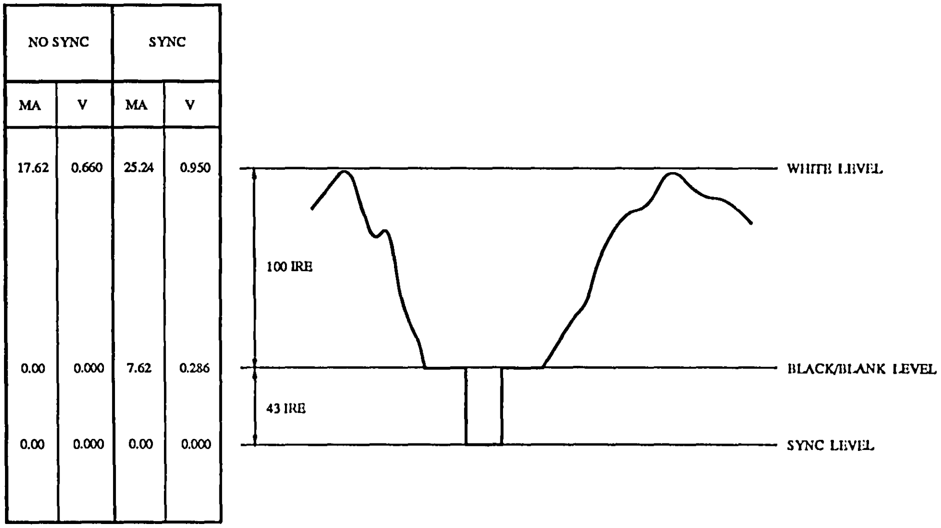
Description	Sync* Disabled	Sync* Enabled	SYNC**	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	19.05	26.67	x	1	$FF
DATA	data + 1.44	data + 9.05	x	1	data
BLACK	1.44	9.05	x	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly terminated load, SETUP = 7.5 IRE. SYNC assumed to be active low. These levels will yield an RSET of ~ 147 Ω given a VREF = 1.235 V (See IREF pin description).

Table 7. RS-343A Video Output Truth Table (SETUP = 7.5 IRE).

*Selected by Command Register 1
**See Sync Pin description in the Pin Description section.

Circuit Description (continued)


NO SYNC
SYNC
MA
V
MA
V
17.62
0.660
25.24
0.950
0.00
0.000
7.62
0.286
0.00
0.000
0.00
0.000
WHITE LEVEL
100 IRE
BLACK/BLANK LEVEL
43 IRE
SYNC LEVEL

Note: 75 Ω doubly terminated load, SETUP = 0 IRE. RS-343A standard levels and tolerances assumed on all levels. These levels will yield an RSET ~ 147 Ω given a VREF = 1.235 V (See IREF pin description).

Figure 3. RS-343A Composite Video Output Waveforms (SETUP = 0 IRE).

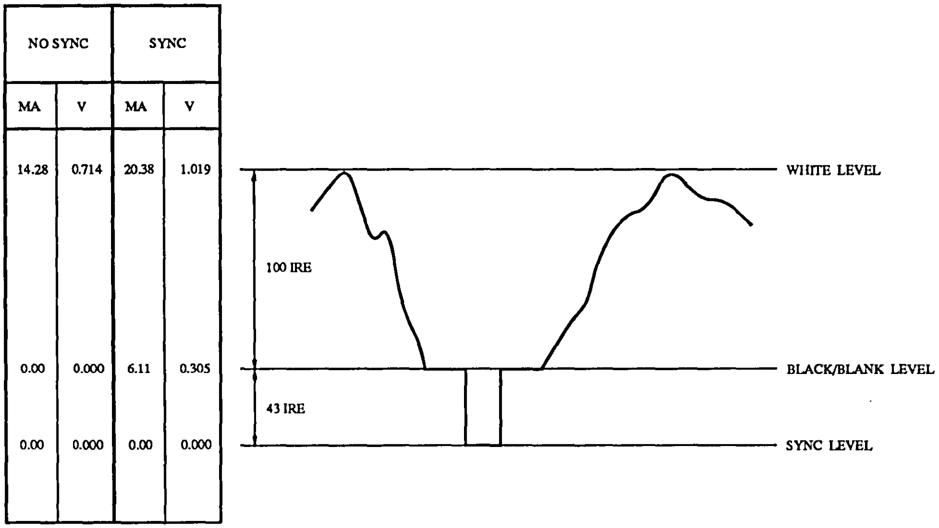
Description	Sync* Disabled	Sync* Enabled	SYNC**	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	17.62	25.24	x	1	$FF
DATA	data	data + 7.62	x	1	data
BLACK	0	7.62	x	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly terminated load, SETUP = 0 IRE. SYNC assumed to be active low. These levels will yield an RSET ~ 147 Ω given a VREF = 1.235 V (See IREF pin description).

Table 8. RS-343A Video Output Truth Table (SETUP = 0 IRE).

*Selected by Command Register 1
**See Sync Pin description in the Pin Description section.

Circuit Description (continued)


NO SYNC
SYNC
MA
V
MA
V
14.28
0.714
20.38
1.019
0.00
0.000
6.11
0.305
0.00
0.000
0.00
0.000
WHITE LEVEL
100 IRE
BLACK/BLANK LEVEL
43 IRE
SYNC LEVEL

Note: 50 Ω load, SETUP = 0 IRE. PS/2 standard levels and tolerances assumed on all levels. These levels will yield an RSET ~ 182 Ω given a VREF = 1.235 V (See IREF pin description).

Figure 4. PS/2 Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync* Disabled	Sync* Enabled	SYNC**	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	14.28	20.38	x	1	$FF
DATA	data	data + 6.11	x	1	data
BLACK	0	6.11	x	1	$00
BLANK	0	6.11	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 50 Ω load, SETUP = 0 IRE. SYNC assumed to be active low. These levels will yield an RSET ~ 182 Ω given a VREF = 1.235 V (See IREF pin description).

Table 9. PS/2 Video Output Truth Table (SETUP = 0 IRE).

*Selected by Command Register 1
**See Sync Pin description in the Pin Description section.

Internal Registers

Window_0–Window_15 x1 and x2 Registers

The 16-bit (x1) and (x2) registers are used to specify the left and right sides of each window by specifying the number of clock cycles from the rising edge of BLANK* to the left or right side of the window. The lower value of (x1) or (x2) specifies the left side, the higher value of (x1) or (x2) specifies the right side. If (x1) and (x2) are equal, the window is not displayed. These registers are ignored if the 479/471* pin is a logical zero. See Figure 1 and Table 6.

The window (x1) register is made up of the window (x1) low register (WX1LR) and the window (x1) high register (WX1HR); the window (x2) register is made up of the window (x2) low register (WX2LR) and the window (x2) high register (WX2HR).

WX1LR and WX1HR are cascaded to form a 12-bit window (x1) register. Similarly, WX2LR and WX2HR are cascaded to form a 12-bit window (x2) register.

	Window (x1) High (WX1HR)						Window (x1) Low (WX1LR)							
Data Bit	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X1 Address	W3	W2	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window (x2) High (WX2HR)						Window (x2) Low (WX2LR)							
Data Bit	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X2 Address	W1	W0	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

D6 and D7 of window(x1) and (x2) high registers are not used. When this register is read back, D6 and D7 will be unknown.

Values from $0000 to $0FFF may be written into the x1 and x2 registers.

For both (x1) and (x2), the MPU must write 8 bits to the low register, followed by 8 bits to the high register. After the high register write cycle, the 12 bits of (x) information are loaded into the registers along with 4 bits of window color palette addressing selection (W0–W3). The registers may be written to or read by the MPU at any time and are not initialized. The registers are implemented as a set of transparent latches. Therefore, to avoid display artifacts during the MPU write cycle, data should be written to these registers during retrace or, alternately, data written to these registers must be valid for the entire time WR* is asserted during active video.

Internal Registers (continued)

Window_0–Window_15 y1 and y2 Registers

The 16-bit (y1) and (y2) registers are used to specify the top and bottom of each window by specifying the number of scan lines from the top of the active display to the top or bottom of the window. The lower value of (y1) or (y2) specifies the top, the higher value of (y1) or (y2) specifies the bottom. If (y1) and (y2) are equal, the window is not displayed. These registers are ignored if the 479/471* pin is a logical zero. See Figure 1 and Table 6.

The window (y1) register is made up of the window (y1) low register (WY1LR) and the window (y1) high register (WY1HR); the window (y2) register is made up of the window (y2) low register (WY2LR) and the window (y2) high register (WY2HR).

WY1LR and WY1HR are cascaded to form a 12-bit window (y1) register. Similarly, WY2LR and WY2HR are cascaded to form a 12-bit window (y2) register.

	Window (y1) High (WY1HR)				Window (y1) Low (WY1LR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y1 Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

	Window (y2) High (WY2HR)				Window (y2) Low (WY2LR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y2 Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

D4–D7 of window (y2) high and (y1) high registers are not used. When this register is read back, D4–D7 will be unknown.

Values from $0000 to $0FFF may be written into the y1 and y2 registers.

For both (y1) and (y2), the MPU must write 8 bits to the low register, followed by 8 bits to the high register. During the high register write cycle, the 12 bits of (y) information are loaded into the registers. The registers may be written to or read by the MPU at any time and are not initialized. The registers are implemented as a set of transparent latches. Therefore, to avoid display artifacts during the MPU write cycle, data should be written to these registers during retrace or, alternately, data written to these registers must be valid for the entire time WR* is asserted during active video.

If BLANK* is a logical zero for 2,048 clock cycles, the Bt479 assumes that a vertical retrace interval is occurring.

Internal Registers (continued)

Command Register_0

This 8-bit register may be written to or read by the MPU at any time and is not initialized. The register is implemented as a set of transparent latches. Therefore, to avoid display artifacts during the MPU write cycle, data should be written to these registers during retrace or, alternately, data written to these registers must be valid for the entire time WR* is asserted during active video. The contents of this register are ignored if the 479/471* pin is a logical zero. CR00 corresponds to data bus bit D0 and is the least significant bit.

CR07–CR04	Color palette select (0000) RAM address $000–$0FF (0001) RAM address $100–$1FF (0010) RAM address $200–$2FF (0011) RAM address $300–$3FF (0100) reserved : : (1111) reserved	These bits specify which portion of the color palette RAM is to be accessed by the MPU. These bits must be 0000 to access the window (x,y) registers.
CR03	OL3 overlay read mask bit	This bit is logically ANDed with the OL3 inputs prior to addressing the overlay palettes.
CR02	OL2 overlay read mask bit	This bit is logically ANDed with the OL2 inputs prior to addressing the overlay palettes.
CR01	OL1 overlay read mask bit	This bit is logically ANDed with the OL1 inputs prior to addressing the overlay palettes.
CR00	OL0 overlay read mask bit	This bit is logically ANDed with the OL0 inputs prior to addressing the overlay palettes.

Internal Registers (continued)

Command Register_1

This 8-bit register may be written to or read by the MPU at any time and is not initialized. The register is implemented as a set of transparent latches. Therefore, to avoid display artifacts during the MPU write cycle, data should be written to these registers during retrace or, alternately, data written to these registers must be valid for the entire time WR* is asserted during active video. The contents of this register are ignored if the 479/471* pin is a logical zero. CR10 corresponds to data bus bit D0 and is the least significant bit.

CR17, CR16	Color palette / window configuration select	These 2 bits, in conjunction with CR10 and W0–W3 (for each window), specify the color palette RAM addressing mode, as shown in Tables 4 and 5.
CR15	Test enable bit (0) normal operation (1) test mode	If this bit is a logical one, the P0–P7 inputs are used to address the internal RAM, rather than the address counter and the data is output via the MPU port during MPU accesses. P0–P7 are still latched on the rising edge of CLOCK and pipelined. The RD* and WR* timing remains unchanged, except for the addressing delay due to pipelining.
CR14	Blue sync enable (0) no sync on blue (1) sync on blue	This bit specifies whether the IOB output is to contain sync information or not.
CR13	Green sync enable (0) no sync on green (1) sync on green	This bit specifies whether the IOG output is to contain sync information or not.
CR12	Red sync enable (0) no sync on red (1) sync on red	This bit specifies whether the IOR output is to contain sync information or not.
CR11	6-bit / 8-bit color operation (0) 6-bit (1) 8-bit	This bit specifies whether 6-bit or 8-bit color data is written or read from the Bt479. It enables mixing 6-bit and 8-bit color palette data. For 6-bit operation, 6 bits of color information are input and output each write/read cycle, with D5 being the MSB and D0 the LSB. D6 and D7 are ignored during write cycles, and are a logical zero during read cycles. For 8-bit operation, 8 bits of color information are input and output each write/read cycle, with D7 being the MSB and D0 the LSB.

Internal Registers (continued)

Command Register_1 (continued)

CR10	1024 Color palette / window configuration select (0) = normal palette mode (1) = windows mode	This bit, in conjunction with CR16, CR17, and W0–W3 (for each window), specify the color palette RAM addressing mode, as shown in Tables 4 and 5.

Flood Registers

The two 8-bit flood registers low and high are used to fill a window (or windows) with the color in the flood color register. Setting a bit to a logical one fills the corresponding window with the flood color.

Flood Register Low	Corresponding Window Number
D0	0
D1	1
D2	2
D3	3
D4	4
D5	5
D6	6
D7	7
Flood Register High	
D0	8
D1	9
D2	10
D3	11
D4	12
D5	13
D6	14
D7	15

The registers may be written to or read by the MPU at any time and are not initialized. The registers are implemented as a set of transparent latches; therefore, data written to these registers must be valid for the entire time WR* is asserted to avoid display artifacts during the MPU write cycle. They are ignored if the 479/471* pin is a logical zero.

These registers are typically used when moving windows. The old window position is filled with the flood color until the system has had time to move the graphics information from the old window location to the new window location.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as illustrated in Tables 7, 8 and 9. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SETUP	Setup control input (TTL compatible). Used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal. This pin should not be left floating.
SYNC	Composite sync control input (TTL compatible). SYNC is sampled while BLANK* is negated (tied high) to determine the sync polarity. If SYNC is a logical one while BLANK* is negated, SYNC is assumed to be active low; if SYNC is a logical zero while BLANK* is negated, SYNC is assumed to be active high. Active sync switches off a 40 IRE current source on the analog outputs (see Figures 2, 3, and 4). SYNC does not override any other control or data input, as shown in Tables 7, 8, and 9; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not required on the video outputs, SYNC should be connected to GND.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0–OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
P0–P7	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0–OL3	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as illustrated in Tables 4 and 5. When accessing the overlay palette, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND.
COMP	Compensation pin. If an external voltage reference is used (Figure 5), this pin should be connected to OPA. If an external current reference is used (Figure 6), this pin should be connected to IREF. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. *Refer to PC Board Layout Considerations for critical layout criteria.*
VREF	Voltage reference input. If an external voltage reference is used (Figure 5), it must supply this input with a 1.2 V (typical) reference. If an external current reference is used (Figure 6), this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor must always be used to decouple this input to GND, as shown in Figures 5 and 6. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
OPA	Reference amplifier output. If an external voltage reference is used (Figure 5), this pin must be connected to COMP. When using an external current reference (Figure 6), this pin should be left floating.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figures 5 and 6).
VAA	Analog power. All VAA pins must be connected.
GND	Analog ground. All GND pins must be connected.

Pin Descriptions (continued)

Pin Name **Description**

IREF

Full-scale adjust control. Note that the IRE relationships in Figures 2, 3, and 4 are maintained, regardless of the full-scale output current.

When using an external voltage reference (Figure 5), a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is:

$$\mathrm{RSET}\,(\Omega) = K * 1{,}000\,(\mathrm{mA/A}) * \mathrm{VREF}\,(\mathrm{V}) / \mathrm{Iout}\,(\mathrm{mA})$$

K is defined in the table below. It is recommended that a 147 Ω RSET resistor be used for doubly terminated 75 Ω loads (i.e., RS-343A applications). For PS/2 applications (i.e., 0.7 V into 50 Ω with no sync), a 182 Ω RSET resistor is recommended.

When using an external current reference (Figure 6), the relationship between IREF and the full-scale output current on each output is:

$$\mathrm{IREF}\,(\mathrm{mA}) = \mathrm{Iout}\,(\mathrm{mA}) / K$$

Mode	Pedestal	K (with sync)	K (no sync)
6-bit	7.5 IRE	3.170	2.270
8-bit	7.5 IRE	3.195	2.295
6-bit	0 IRE	3.000	2.100
8-bit	0 IRE	3.025	2.125

WR*

Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. Note: to avoid display artifacts during the MPU write cycle, the Bt479 specific control registers should be written during retrace or, alternately, data written to these registers must be valid for the entire time WR* is asserted during active video. RD* and WR* should not be asserted simultaneously.

RD*

Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously.

RS0, RS1, RS2

Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as illustrated in Tables 1 and 2.

D0–D7

Data bus (TTL compatible). Data is transferred into and out of the device over this 8 bit bidirectional data bus. D0 is the least significant bit.

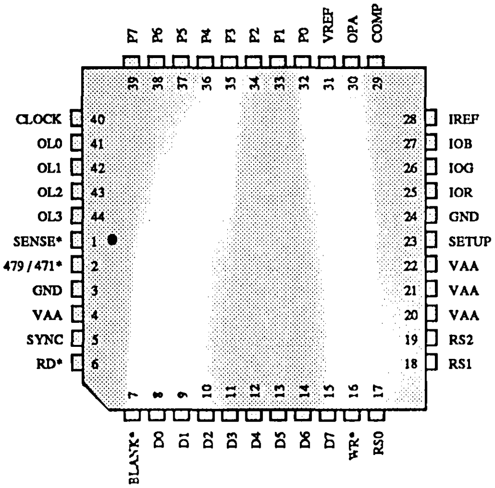
479/471*

Bt479 or B471 select input (TTL compatible). When the 479/471* input pin is a logical zero, the Bt479 behaves exactly as a Bt471 with anti-sparkle capabilities. When the 479/471* input pin is a logical one, the extra capabilities of the Bt479 are available. This pin must not be left floating.

SENSE*

Sense output (CMOS compatible). SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded 335 mV. Note that SENSE* may not be stable while SYNC* is toggling.

Pin Descriptions (continued)


P7 39
P6 38
P5 37
P4 36
P3 35
P2 34
P1 33
P0 32
VREF 31
OPA 30
COMP 29
CLOCK 40
OL0 41
OL1 42
OL2 43
OL3 44
SENSE* 1
479 / 471* 2
GND 3
VAA 4
SYNC 5
RD* 6
28 IREF
27 IOB
26 IOG
25 IOR
24 GND
23 SETUP
22 VAA
21 VAA
20 VAA
19 RS2
18 RS1
7 BLANK*
8 D0
9 D1
10 D2
11 D3
12 D4
13 D5
14 D6
15 D7
16 WR*
17 RS0

PC Board Layout Considerations

PC Board Considerations

This product requires special attention to proper layout techniques to achieve optimum performance. Before beginning PCB layout, refer to the CMOS RAMDAC layout example found in Bt451/7/8 Evaluation Module Operation and Measurements, application note (AN-16). This application note can be found in Brooktree's 1990 Applications Handbook.

The layout should be optimized for lowest noise on the Bt479 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of four layers is recommended with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

The optimum layout enables the Bt479 to be located as close to the power supply connector and as close to the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8-inch gap) and connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector to preserve digital noise margins during MPU read cycles. Thus, the ground tub isolation technique is constrained by the noise margin degradation during digital readback of the Bt479.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.

The analog ground plane should include all Bt479 ground pins, all reference circuitry and decoupling (external reference if used, RSET resistors, etc.), power supply bypass circuitry for the Bt479, analog output traces and the video output connector.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt479 power pins, any reference circuitry, and COMP and reference decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 5 and 6. This bead should be located within 3 inches of the Bt479. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low resistance bead should be used, such as Fair-Rite 2743001111, Ferroxcube 5659065-3B, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance, radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 μF ceramic capacitor decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 μF capacitor in parallel with a 0.001 μF chip capacitor is recommended. The capacitors should be placed as close as possible to the device.

The 10 μF capacitor is for low-frequency power supply ripple; the 0.1 μF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 200 mV or greater than 10 LSBs. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic chip capacitor. Low frequency supply noise will require a larger value. Lead lengths should be minimized for best performance.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt479 should be isolated from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit from using lower speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt479 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt479 to minimize reflections. Unused analog outputs should be connected to GND.

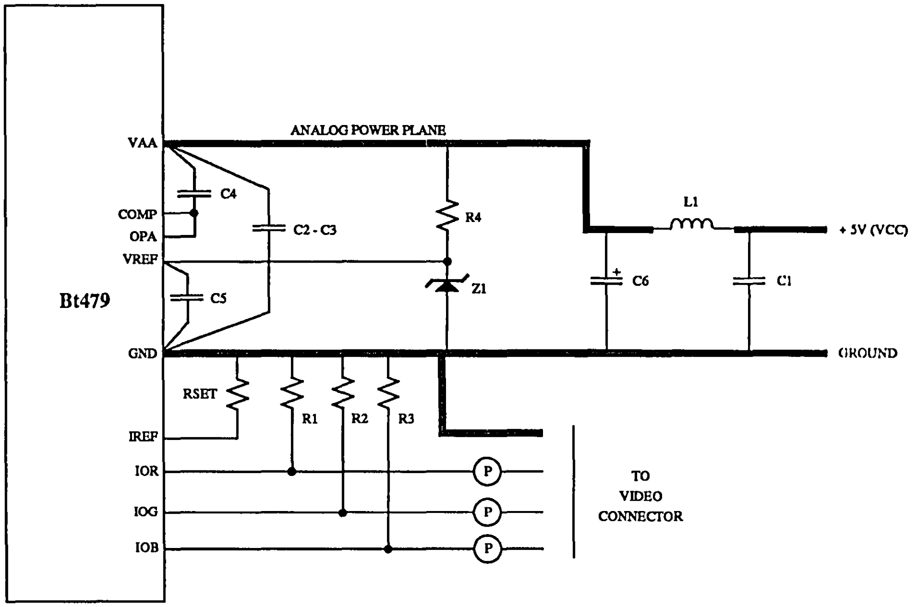
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise.

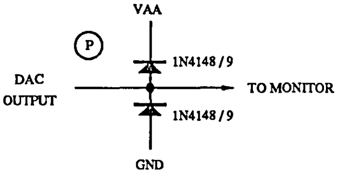
Analog Output Protection

The Bt479 analog outputs should be protected against high energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figures 5 and 6, can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)


ANALOG POWER PLANE
VAA
COMP
OPA
VREF
Bt479
GND
IREF
IOR
IOG
IOB
C4
C2 - C3
C5
R4
Z1
L1
+ 5V (VCC)
C6
C1
GROUND
RSET
R1
R2
R3
P
TO
VIDEO
CONNECTOR

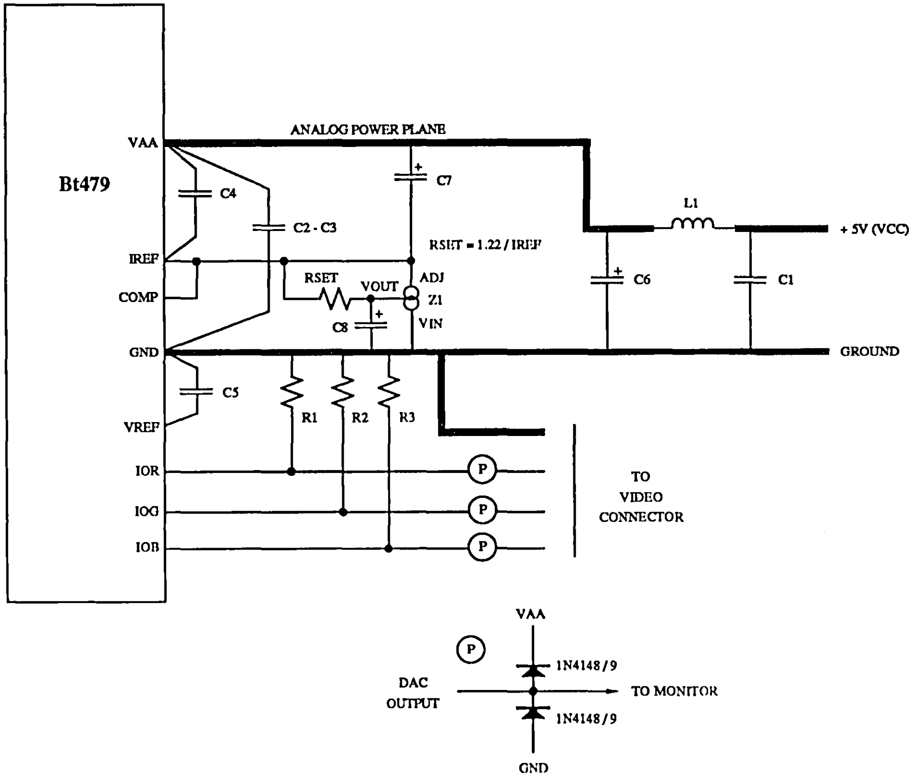

VAA
P
1N4148 / 9
DAC
OUTPUT
TO MONITOR
1N4148 / 9
GND

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt479.

Figure 5. Typical Connection Diagram and Parts List (External Voltage Reference).

PC Board Layout Considerations (continued)


ANALOG POWER PLANE
VAA
Bt479
C4
C2 - C3
C7
RSET = 1.22 / IREF
L1
+ 5V (VCC)
IREF
COMP
RSET
VOUT
ADJ
Z1
VIN
C8
C6
C1
GND
GROUND
C5
VREF
R1
R2
R3
IOR
IOG
IOB
P
TO VIDEO CONNECTOR
VAA
P
1N4148/9
DAC OUTPUT
TO MONITOR
1N4148/9
GND

Location	Description	Vendor Part Number
C1–C5	0.1 μF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 μF capacitor	Mallory CSR13G106KM
C7, C8	1 μF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM337LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt479.

Figure 6. Typical Connection Diagram and Parts List (External Current Reference).

Application Information

Initializing the Bt479

Following a power-on sequence, the Bt479 must be initialized. This sequence will configure the Bt479 as follows (479/471* pin must be a logical one):

no overlays
no sync
6-bit color data

Control Register Initialization	RS2–RS0
Write $00 to address register	000
Write $00 to window(0) x1 low register	110
Write $00 to window(0) x1 high register	110
Write $00 to window(0) x2 low register	110
Write $00 to window(0) x2 high register	110
Write $00 to window(0) y1 low register	110
Write $00 to window(0) y1 high register	110
Write $00 to window(0) y2 low register	110
Write $00 to window(0) y2 high register	110
Write $00 to window(1) x1 low register	110
Write $00 to window(1) x1 high register	110
Write $00 to window(1) x2 low register	110
Write $00 to window(1) x2 high register	110
Write $00 to window(1) y1 low register	110
Write $00 to window(1) y1 high register	110
Write $00 to window(1) y2 low register	110
Write $00 to window(1) y2 high register	110
	:
Write $00 to window(15) x1 low register	110
Write $00 to window(15) x1 high register	110
Write $00 to window(15) x2 low register	110
Write $00 to window(15) x2 high register	110
Write $00 to window(15) y1 low register	110
Write $00 to window(15) y1 high register	110
Write $00 to window(15) y2 low register	110
Write $00 to window(15) y2 high register	110
Write $82 to address register	000
Write $00 to command register_0	110
Write $01 to command register_1	110
Write $00 to flood register low	110
Write $00 to flood register high	110
Write $FF to pixel read mask register	010

Color Palette RAM Initialization	RS2–RS0
Write $82 to address register	000
Write $00 to command register_0	110
Write $00 to address register	000
Write red data to RAM (location $000)	001
Write green data to RAM (location $000)	001
Write blue data to RAM (location $000)	001
Write red data to RAM (location $001)	001
Write green data to RAM (location $001)	001
Write blue data to RAM (location $001)	001
:	:
Write red data to RAM (location $0FF)	001
Write green data to RAM (location $0FF)	001
Write blue data to RAM (location $0FF)	001
Write $82 to address register	000
Write $10 to command register_0	110
Write $00 to address register	000
Write red data to RAM (location $100)	001
Write green data to RAM (location $100)	001
Write blue data to RAM (location $100)	001
Write red data to RAM (location $101)	001
Write green data to RAM (location $101)	001
Write blue data to RAM (location $101)	001
:	:
Write red data to RAM (location $1FF)	001
Write green data to RAM (location $1FF)	001
Write blue data to RAM (location $1FF)	001
Write $82 to address register	000
Write $20 to command register_0	110
Write $00 to address register	000
Write red data to RAM (location $200)	001
Write green data to RAM (location $200)	001
Write blue data to RAM (location $200)	001
Write red data to RAM (location $201)	001
Write green data to RAM (location $201)	001
Write blue data to RAM (location $201)	001
:	:
Write red data to RAM (location $2FF)	001
Write green data to RAM (location $2FF)	001
Write blue data to RAM (location $2FF)	001

Application Information (continued)

	RS2–RS0
Write $82 to address register	000
Write $30 to command register_0	110
Write $00 to address register	000
Write red data to RAM (location $300)	001
Write green data to RAM (location $300)	001
Write blue data to RAM (location $300)	001
Write red data to RAM (location $301)	001
Write green data to RAM (location $301)	001
Write blue data to RAM (location $301)	001
:	:
Write red data to RAM (location $3FF)	001
Write green data to RAM (location $3FF)	001
Write blue data to RAM (location $3FF)	001

Overlay Color Palette Initialization

Write $00 to address register	100
Write red data to flood (location $00)	101
Write green data to flood (location $00)	101
Write blue data to flood (location $00)	101
Write red data to overlay (location $01)	101
Write green data to overlay (location $01)	101
Write blue data to overlay (location $01)	101
:	:
Write red data to overlay (location $FF)	101
Write green data to overlay (location $FF)	101
Write blue data to overlay (location $FF)	101

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Using Multiple Devices

When using multiple Bt479s, each Bt479 should have its own power plane ferrite bead.

Although the multiple Bt479s may be driven by a common external voltage/current reference, higher performance may be obtained if each RAMDAC uses its own separate reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt479 must still have its own individual RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

Reference Selection

An external voltage reference provides about 10x better power supply rejection on the analog outputs than an external current reference.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
80, 66 MHz Parts		4.75	5.00	5.25	Volts
50, 35 MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ohms
Voltage Reference Configuration					
Reference Voltage	VREF	1.14	1.235	1.26	Volts
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		–3	–8.39	–10	mA
PS/2 Compatible		–3	–8.88	–10	mA

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT			7	pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current (Standard RS-343A)					
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank					
SETUP = 7.5 IRE		0.95	1.44	1.90	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
DAC to DAC Matching			2	5	%
Output Compliance	VOC	-1.0		+1.5	Volts
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT			30	pF
Voltage Reference Input Current	IREF IN		10		µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with SETUP = 7.5 IRE, RSET = 147 Ω, VREF = 1.235 V, 479/471* pin = logical one. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Analog Output Levels — PS/2 Compatibility

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Output Current					
White Level Relative to Black		18.00	18.65	20.00	mA
Black Level Relative to Blank					
(SETUP = 7.5 IRE)		1.01	1.51	2.0	mA
SETUP = 0 IRE		0	5	50	µA
Blank Level		6.6	8	9.4	mA
Sync Level		0	5	50	µA

Test conditions to generate PS/2 compatible video signals (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with SETUP = 7.5 IRE, RSET = 140 Ω, VREF = 1.235 V or external current reference with IREF = -8.88 mA. 479/471* pin = logical one.

AC Characteristics

		80 MHz Devices			66 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			80			66	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time**	7	10			10			ns
Write Data Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	5*p13			5*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	12.5			15.15			ns
Clock Pulse Width High Time	14	4			5			ns
Clock Pulse Width Low Time	15	4			5			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		20			28		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			75			75		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
SENSE* Output Delay	19		1			1		µS
Pipeline Delay		8	8	8	8	8	8	Clocks
VAA Supply Current***	IAA		tbd	tbd		tbd	tbd	mA

See test conditions on next page.

A.C. Characteristics (continued)

		50 MHz Devices			35 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			50			35	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	5			5			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	5			5			ns
Write Data Setup Time **	7	10			10			ns
Write Data Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	5*p13			5*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
Clock Cycle Time (p13)	13	20			28			ns
Clock Pulse Width High Time	14	6			7			ns
Clock Pulse Width Low Time	15	6			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time*	18		20			28		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			75			75		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
SENSE* Output Delay	19		1			1		µS
Pipeline Delay		8	8	8	8	8	8	Clocks
VAA Supply Current***	IAA		tbd	tbd		tbd	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 147 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, 479/471* pin = logical one. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, D0–D7 output load ≤ 75 pF. See timing notes in Figure 8. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Clock and data feedthrough is a function of the edge rate, the amount of overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

** For the Bt479 control registers, write data set up time is with respect to falling edge of WR*. Therefore, to avoid display artifacts during the MPU write cycle, data should be written to registers during retrace or, alternately, data written to these registers must be valid for the entire time WR* is asserted during active video. See Figure 7. For the color lookup table, write data set up time is with respect to the rising edge of WR*.

Timing Waveforms

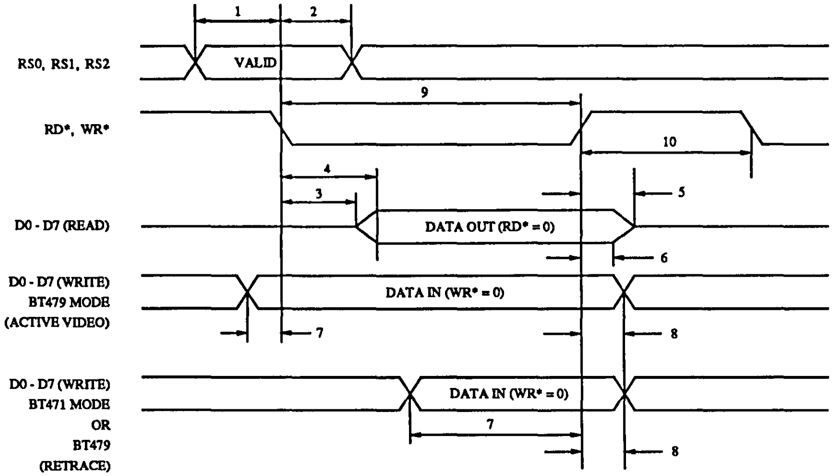
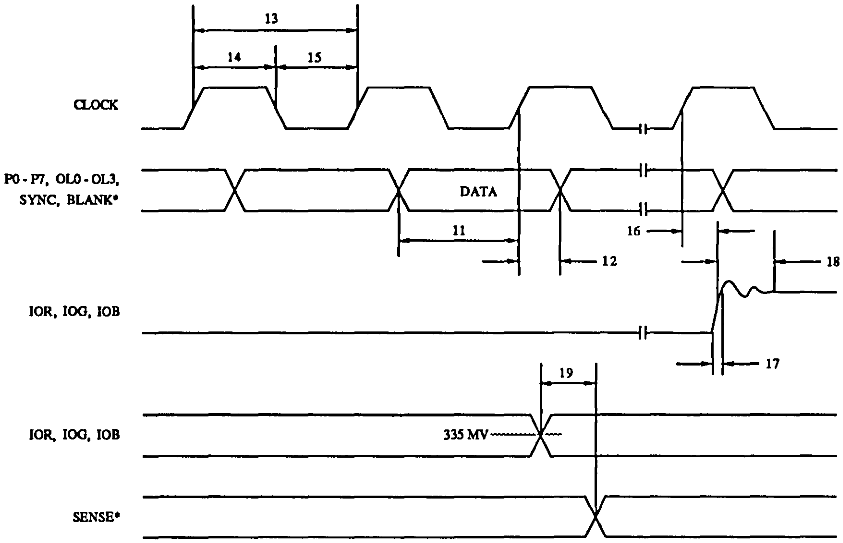

1
2
RS0, RS1, RS2
VALID
9
RD*, WR*
10
4
3
5
D0 - D7 (READ)
DATA OUT (RD* = 0)
6
D0 - D7 (WRITE)
BT479 MODE
(ACTIVE VIDEO)
DATA IN (WR* = 0)
7
8
D0 - D7 (WRITE)
BT471 MODE
OR
BT479
(RETRACE)
DATA IN (WR* = 0)
7
8

Figure 7. MPU Read/Write Timing.

Timing Waveforms (continued)


13
14
15
CLOCK
P0 - P7, OL0 - OL3, SYNC, BLANK*
DATA
11
12
16
18
IOR, IOG, IOB
17
19
IOR, IOG, IOB
335 MV
SENSE*

Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 8. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt479KPJ80	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt479KPJ66	66 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt479KPJ50	50 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt479KPJ35	35 MHz	44-pin Plastic J-Lead	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
B	W/C* references replaced with "bit D0 in command register_1," Tables 4 and 5 swapped. Bit D5 in command register_1 is a test enable bit.
C	Added analog output comparators, on-chip voltage reference, use of BLANK* rather than SYNC* to determine window placement, deleted Vertical Count Register, added anti-sparkle capability and polarity-independent SYNC*, and changed color palette RAM addressing operation.
D	Added Figure 1. Datasheet status went from Advanced to Preliminary. Updated to note that the window and command registers are transparent so MPU data must be valid during entire time WR* is asserted when writing to these registers. Changed decoupling of VREF to GND rather than VAA (decoupling to GND may result in better performance). Pipeline delay corrected from 4 to 8 clocks. RD* and WR* pulse width high values were corrected from a minimum of 4 clock cycles to 5 clock cycles. Removed all references to the internal Voltage Reference feature.
E	Revised the 479/471* pin description.

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt492

360 MHz
100K ECL-Compatible
256 x 8 Color Palette
RAMDAC™

Distinguishing Features

- 360 MHz Pipelined Operation
- 256 x 8 Color Palette RAM
- 16 x 8 Overlay RAM
- 350 ps Typical Rise/Fall Time
- RS-343A Compatible Output
- 0 or 7.5 IRE Blanking Pedestal
- Drives 1 V Into 25 Ω Output Loads
- 100K ECL-Compatible Pixel Inputs
- Divide-by-2 of Clock for Load Generation
- TTL-Compatible MPU Interface
- 68-pin Ceramic PGA Package with Heatsink and Alignment Pin
- Typical Power Dissipation: 3.5 W

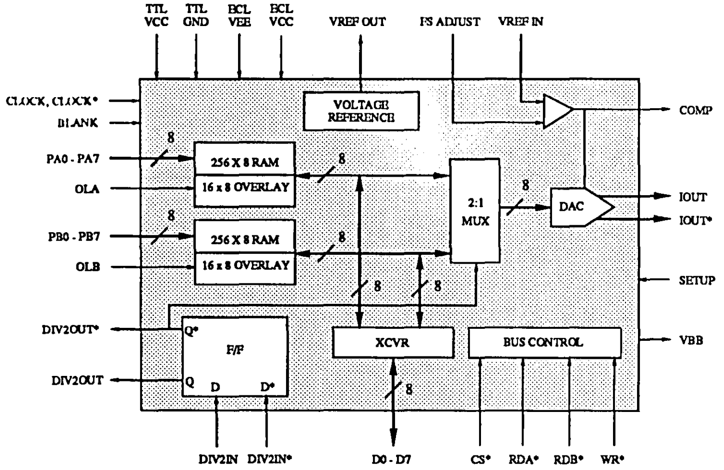
Applications

- Graphics Terminals
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing

Related Products

- Bt424

Functional Block Diagram


TTL VCC
TTL GND
ECL VEE
ECL VCC
VREF OUT
FS ADJUST
VREF IN
CLOCK, CLOCK*
BLANK
PA0 - PA7
OLA
PB0 - PB7
OLB
DIV2OUT*
DIV2OUT
VOLTAGE REFERENCE
256 X 8 RAM
16 x 8 OVERLAY
256 X 8 RAM
16 x 8 OVERLAY
8
2:1 MUX
DAC
F/F
Q*
Q
D
D*
XCVR
BUS CONTROL
COMP
IOUT
IOUT*
SETUP
VBB
DIV2IN
DIV2IN*
D0 - D7
CS*
RDA*
RDB*
WR*

Product Description

The Bt492 is an 8-bit RAMDAC, designed specifically for high-performance, high-resolution color graphics.

The 2:1 multiplexed pixel inputs enable interfacing to 180 MHz pixel data, simplifying interfacing to the frame buffer. On-chip divide by 2 of the clock is provided, generating the 180 MHz differential load clocks. The pixel, DIV2IN, and blank inputs, and the DIV2OUT and DIV2OUT* outputs, are 100K ECL-compatible. The blanking signal is pipelined to maintain synchronization with the pixel data.

The MPU interface signals (D0-D7, CS*, RDA*, RDB*, and WR*) are TTL compatible. During MPU accesses to the RAM, the address is input through the pixel ports (PA0-PA7, PB0-PB7).

An on-chip voltage reference is available or an external reference may be used. A single external resistor controls the full-scale output current.

The Bt492 generates an RS-343A compatible video signal, and is capable of driving either doubly terminated 75 Ω or 50 Ω coax directly, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1/2 LSB over the full temperature range.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L492001 Rev. E

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt492 has two 256 x 8 RAMs, a 2:1 multiplexer, a single 8-bit DAC, and MPU interface.

MPU data is input and output via the D0–D7 data lines. During MPU accesses to the color palette RAMs, the RAMs are addressed via the PAx, PBx, and OLx inputs and the internal pipeline registers are transparent. During MPU write cycles (WR* = 0), data is written to both RAMs. The MPU may read either RAM via the RDA* and RDB* control inputs. (See Figure 1.)

BLANK should be asserted during MPU accesses to prevent the data values associated with the MPU address from appearing at the analog outputs. Following an MPU cycle, BLANK should be asserted for at least one valid pixel cycle before the PAx and PBx inputs can be properly routed to the analog outputs.

Frame Buffer Interface

Pixel data on the PA0–PA7 and OLA inputs (even data) and PB0–PB7 and OLB inputs (odd data) are latched on the falling edge of DIV2OUT*, as illustrated in Figure 2.

The OLx inputs determine whether the Px0–Px7 inputs address the 256 x 8 color palette RAM (OLx = 0) or the 16 x 8 overlay palette RAM (OLx = 1). When addressing the overlay RAM, Px4–Px7 are ignored. The outputs of the RAMs are then multiplexed at the pixel clock rate and drive the 8-bit video D/A converter.

DIV2IN is defined to be 1/2 the CLOCK rate. To simplify system design, the Bt492 outputs a DIV2OUT* signal which, when connected to the DIV2IN pin, generates a clock equal to 1/2 the CLOCK rate. For a color system requiring three Bt492s, the DIV2OUT signals may be synchronized by connecting the DIV2OUT* signal on one of the devices to the DIV2IN pins of all three devices. Care should be taken to keep signal paths short and equal for each connection. The unused DIV2OUT signals from the remaining Bt492s can be used to clock the shift registers driving the Bt492 pixel inputs.

The BLANK input is also latched on the falling edge of DIV2OUT* and overrides the PA0–PA7, OLA, PB0–PB7, and OLB inputs. Blanking information is output synchronously with the even pixel data.

Full-scale output current is set by an external resistor (RSET) between the FS ADJUST pin and ECL VCC. RSET has a typical value of 1092 Ω for generation of RS-343A video into a 37.5 Ω load, or 729 Ω for generation of RS-343A video into a 25 Ω load. The on-chip voltage reference (VREF OUT) may be used to provide the reference for the VREF IN pins of up to three Bt492s, or an external reference may be used.

Both sides of the differential current outputs should have the same output load. A single-ended video signal may be generated by connecting the IOUT output through a 25 Ω resistor to ECL VCC(assuming a doubly terminated 50 Ω load). The IOUT* output is used to generate the positive video signal.

The D/A converter on the Bt492 uses a segmented architecture in which bit currents are routed to either IOUT or IOUT* by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt492 are capable of directly driving either a 37.5 Ω or 25 Ω load, such as a doubly terminated 75 Ω or 50 Ω coaxial cable.

Circuit Description (continued)

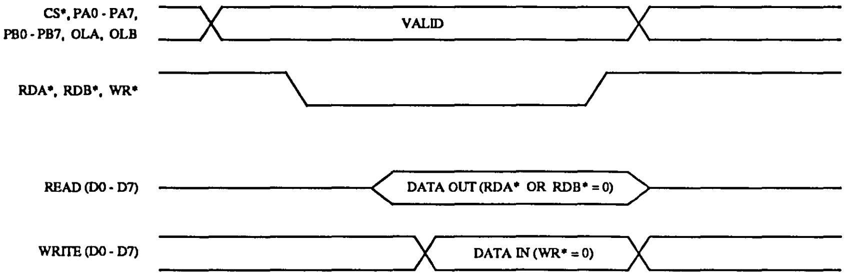

CS*, PA0 - PA7,
PB0 - PB7, OLA, OLB
VALID
RDA*, RDB*, WR*
READ (D0 - D7)
DATA OUT (RDA* OR RDB* = 0)
WRITE (D0 - D7)
DATA IN (WR* = 0)

Figure 1. MPU Read/Write Timing.

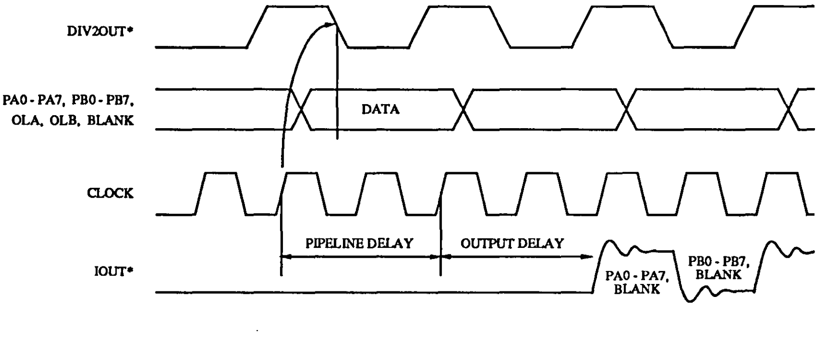
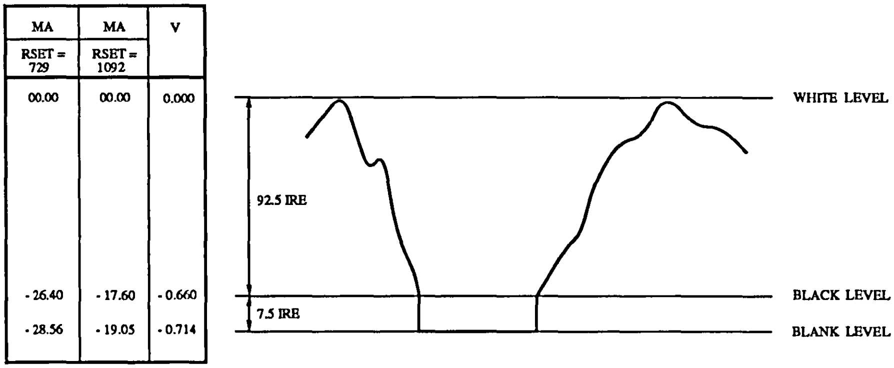

DIV2OUT*
PA0 - PA7, PB0 - PB7,
OLA, OLB, BLANK
DATA
CLOCK
PIPELINE DELAY
OUTPUT DELAY
IOUT*
PA0 - PA7,
BLANK
PB0 - PB7,
BLANK

Figure 2. Video Input/Output Timing.

Circuit Description (continued)



MA	MA	V
RSET = 729	RSET = 1092	
00.00	00.00	0.000
- 26.40	- 17.60	- 0.660
- 28.56	- 19.05	- 0.714

Note: RSET = 729 Ω (50 Ω doubly terminated load) or 1092 Ω (75 Ω doubly terminated load), VREF IN = –1.2 V. RS-343A levels and tolerances assumed on all levels.

Figure 3. Composite Video Output Waveforms (IOUT).*

	RSET = 729 Ω	RSET = 1092 Ω		
Description	IOUT* (mA)	IOUT* (mA)	BLANK	DAC Input Data
WHITE	0	0	0	$FF
DATA	data	data	0	data
BLACK	–26.40	–17.62	0	$00
BLANK			1	$xx
SETUP = ECL VCC	–26.40	–17.62		
SETUP = float	–28.56	–19.05		

Note: Typical with VREF IN = –1.2 V.

Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK	Composite blank control input (ECL compatible). A logic one drives the analog output to the blanking level, as illustrated in Table 1. It is latched on the falling edge of DIV2OUT*. When BLANK is a logical one, the PA0–PA7, PB0–PB7, OLA, and OLB inputs are ignored. Blanking information is output synchronously with the even pixel data.
PA0–PA7, PB0–PB7	Even and odd pixel data inputs (ECL compatible). D0 is the least significant data bit. They are latched on the falling edge of DIV2OUT* while CS* is a logical one. PAx represent the even pixel data, and PBx represent the odd pixel data. Even data represents the first (leftmost) pixel on the display screen. Coding is binary. PA0 and PB0 are the LSBs.
OLA, OLB	Even and odd overlay data inputs (ECL compatible). When OLA or OLB are a logical one, the 4 MSBs of the corresponding pixel inputs (Px4–Px7) are ignored and the 4 LSBs are used to select one of 16 available data words in the overlay palette. They are latched on the falling edge of DIV2OUT* while CS* is a logical one. If left floating, they will pull themselves to DVEE.
CLOCK, CLOCK*	Differential clock inputs (ECL compatible). They are typically the pixel clock rate of the video system.
DIV2IN, DIV2IN*	Differential CLOCK/2 inputs (ECL compatible). These clocks must be 1/2 the CLOCK rate. They may be configured for single-ended operation by connecting DIV2IN* to VBB.
DIV2OUT*, DIV2OUT	CLOCK/2 differential outputs (ECL compatible). When DIV2OUT* is connected to the DIV2IN pin, these outputs are 1/2 the CLOCK rate. When not connected to DIV2IN, they generate a signal that is DIV2IN synchronized to CLOCK and inverted.
IOUT, IOUT*	Differential video current outputs. These high-impedance current sources are capable of directly driving either a doubly terminated 50 Ω or 75 Ω coaxial cable (Figures 4 and 5). Both outputs, whether used or not, should have the same output load for best settling time.
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic chip capacitor and a 0.001 µF ceramic chip capacitor must be connected between this pin and AVEE (Figures 4 and 5). The COMP capacitors must be as close to the device as possible to keep lead inductance to an absolute minimum. *Refer to PC Board Layout Considerations for critical layout criteria.*
SETUP	Pedestal control input. If connected to ECL VCC, the blanking pedestal on the output is disabled, making the black and blanking levels the same (0 IRE). If left floating, the 7.5 IRE blanking pedestal is enabled. See Figure 3.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and ECL VCC controls the magnitude of the full-scale video signal (Figures 4 and 5). Note that the IRE relationships in Figure 3 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current is: RSET (Ω) = K * VREF IN (V) / IOUT (mA) where K = 17,205 if SETUP = float or 15,915 if SETUP = ECL VCC. Note: The RSET value may need to be adjusted to generate the specified video levels due to variations in processing and depending on whether the internal or an external reference is used.

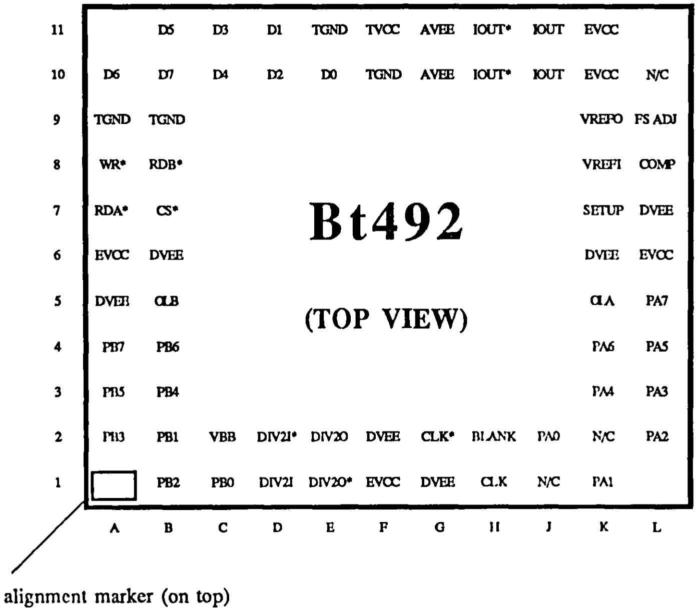
Pin Descriptions (continued)

Pin Name	Description
VREF OUT	Voltage reference output. This output provides a –1.2 V (typical) reference, and may be connected to the VREF IN inputs of up to three Bt492s. When driving multiple Bt492s, use 100 Ω interconnect resistance to minimize noise pick-up. If it is not used to provide a voltage reference, it should remain floating.
VREF IN	Voltage reference input. An external voltage reference, such as the one shown in Figure 6, or the VREF OUT pin must supply this input with a –1.2 V (typical) reference. A 0.01 µF ceramic chip capacitor in parallel with a 0.001 µF ceramic chip capacitor must be connected between this pin and ECL VCC, as shown in Figures 4 and 5. The decoupling capacitors must be as close to the device as possible to keep lead inductance to an absolute minimum.
CS*	Chip select control input (TTL compatible). This input must be a logical zero to enable MPU data to be written to or read from the device. When it is a logical one, D0–D7 are three-stated. While CS* is a logical zero, the PA0–PA7, PB0–PB7, OLA, and OLB inputs are used to address the color palette RAM and overlay RAM, and the internal pipeline registers are configured to be transparent.
RDA*, RDB*	Read control input (TTL compatible). To read data from RAM A, both CS* and RDA* must be a logical zero. To read data from RAM B, both CS* and RDB* must be a logical zero. MPU addressing on PAx, PBx, and OLx must be valid while RDA* or RDB* is a logical zero. CS*, RDA*, and RDB* must not be a logical zero simultaneously. (See Figure 8.)
WR*	Write control input (TTL compatible). To write data to the device, both CS* and WR* must be a logical zero. MPU addresses on PAx and PBx are accepted on the falling edge of WR* or CS*, whichever occurs first. Data is accepted on the rising edge of WR* or CS*, whichever occurs first. MPU addressing on PAx, PBx, and OLx must be valid while WR* is a logical zero. RDx* and WR* must not be a logical zero simultaneously. (See Figure 9.)
D0 - D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
VBB	–1.3 V output. A 0.01 µF decoupling capacitor to ECL VCC reduces threshold jitter.
TTL VCC	TTL power. All TTL VCC pins must be connected together.
TTL GND	TTL ground. All TTL GND pins must be connected together.
ECL VCC	ECL ground. All ECL VCC pins must be connected together. See Figures 4 and 5.
DVEE	ECL digital power. All DVEE pins must be connected together. See Figures 4 and 5.
AVEE	ECL analog power. All AVEE pins must be connected together. See Figures 4 and 5. **Warning: It is important that a ferrite bead be used to connect the AVEE power pins to the analog power plane as illustrated in Figures 4 and 5.**
Alignment Pin	The alignment pin is connected to the metallic cavity lid which is electrically isolated.

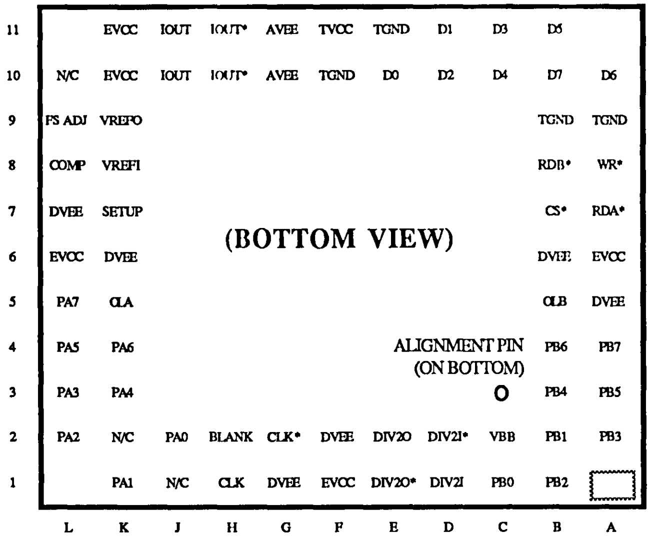
Pin Descriptions (continued)

Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
CLOCK	H1	D0	E10	VBB	C2
CLOCK*	G2	D1	D11		
		D2	D10	TTL VCC	F11
DIV2IN	D1	D3	C11		
DIV2IN*	D2	D4	C10	TTL GND	F10
DIV2OUT	E2	D5	B11	TTL GND	E11
DIV2OUT*	E1	D6	A10	TTL GND	A9
		D7	B10	TTL GND	B9
BLANK	H2				
		CS*	B7	ECL VCC	A6
PA0	J2	RDA*	A7	ECL VCC	F1
PA1	K1	RDB*	B8	ECL VCC	L6
PA2	L2	WR*	A8	ECL VCC	K10
PA3	L3			ECL VCC	K11
PA4	K3	IOUT	J10, J11		
PA5	L4	IOUT*	H10, H11	DVEE	A5
PA6	K4			DVEE	B6
PA7	L5	SETUP	K7	DVEE	F2
OLA	K5	COMP	L8	DVEE	G1
		VREF IN	K8	DVEE	K6
PB0	C1	VREF OUT	K9	DVEE	L7
PB1	B2	FS ADJUST	L9		
PB2	B1			AVEE	G10
PB3	A2	N/C	K2	AVEE	G11
PB4	B3	N/C	J1		
PB5	A3	N/C	L10	alignment pin (LID)	C3
PB6	B4				
PB7	A4				
OLB	B5				

Pin Descriptions (continued)



	A	B	C	D	E	F	G	H	J	K	L
11		D5	D3	D1	TGND	TVCC	AVEE	IOUT*	IOUT	EVCC	
10	D6	D7	D4	D2	D0	TGND	AVEE	IOUT*	IOUT	EVCC	N/C
9	TGND	TGND								VREFO	FS ADJ
8	WR*	RDB*								VREFI	COMP
7	RDA*	CS*								SETUP	DVEE
6	EVCC	DVEE								DVEE	EVCC
5	DVEE	CLB								CLA	PA7
4	PB7	PB6								PA6	PA5
3	PB5	PB4								PA4	PA3
2	PB3	PB1	VBB	DIV2I*	DIV2O	DVEE	CLK*	BLANK	PA0	N/C	PA2
1		PB2	PB0	DIV2I	DIV2O*	EVCC	DVEE	CLK	N/C	PA1	



	L	K	J	H	G	F	E	D	C	B	A
11		EVCC	IOUT	IOUT*	AVEE	TVCC	TGND	D1	D3	D5	
10	N/C	EVCC	IOUT	IOUT*	AVEE	TGND	D0	D2	D4	D7	D6
9	FS ADJ	VREFO								TGND	TGND
8	COMP	VREFI								RDB*	WR*
7	DVEE	SETUP								CS*	RDA*
6	EVCC	DVEE								DVEE	EVCC
5	PA7	CLA								CLB	DVEE
4	PA5	PA6								PB6	PB7
3	PA3	PA4								PB4	PB5
2	PA2	N/C	PA0	BLANK	CLK*	DVEE	DIV2O	DIV2I*	VBB	PB1	PB3
1		PA1	N/C	CLK	DVEE	EVCC	DIV2O*	DIV2I	PB0	PB2	

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt492 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of AVEE and ECL VCC pins should be as short as possible to minimize inductive ringing.

Sockets

Only flush mount sockets should be used, such as the Advanced Interconnect KS06985TG.

Ground Planes

The ground plane should encompass all Bt492 ground pins, any voltage reference circuitry, power supply bypass circuitry for the Bt492, the analog output traces, and all the digital signal traces leading up to the Bt492.

Power Planes

The Bt492 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figures 4 and 5. This bead should be located within 3 inches of the Bt492.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt492 power pins, any external voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged so that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

In addition to the ferrite beads between the analog and regular PCB power and ground planes, an additional ferrite bead must be installed between the AVEE power pins and the analog power plane, as illustrated in Figures 4 and 5. The ferrite bead must be located as close as possible to the AVEE pins.

For the best performance, three chip capacitors in parallel (0.1 µF, 0.01 µF, and 0.001 µF) should be placed as close as possible to each power pin for power supply bypassing. These capacitors should be connected on the analog power plane side of the ferrite bead for the AVEE pins as illustrated in Figures 4 and 5.

COMP Decoupling

Ceramic chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance.

Digital Signal Interconnect

The digital inputs to the Bt492 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Stripline or microstrip techniques should be used for the ECL interfacing. In addition, all ECL inputs should be terminated as closely as possible to the device to reduce ringing, crosstalk, and reflections.

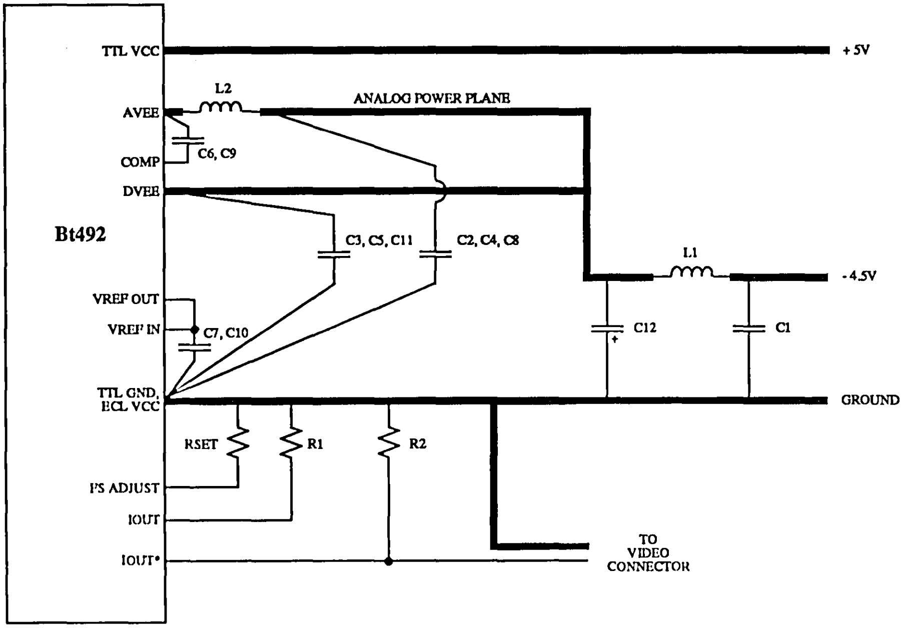
Any termination resistors for the digital inputs should be connected to the regular PCB power or termination and ground planes.

Analog Signal Interconnect

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

It is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed circuitry wiring and coaxial cable.

PC Board Layout Considerations (continued)

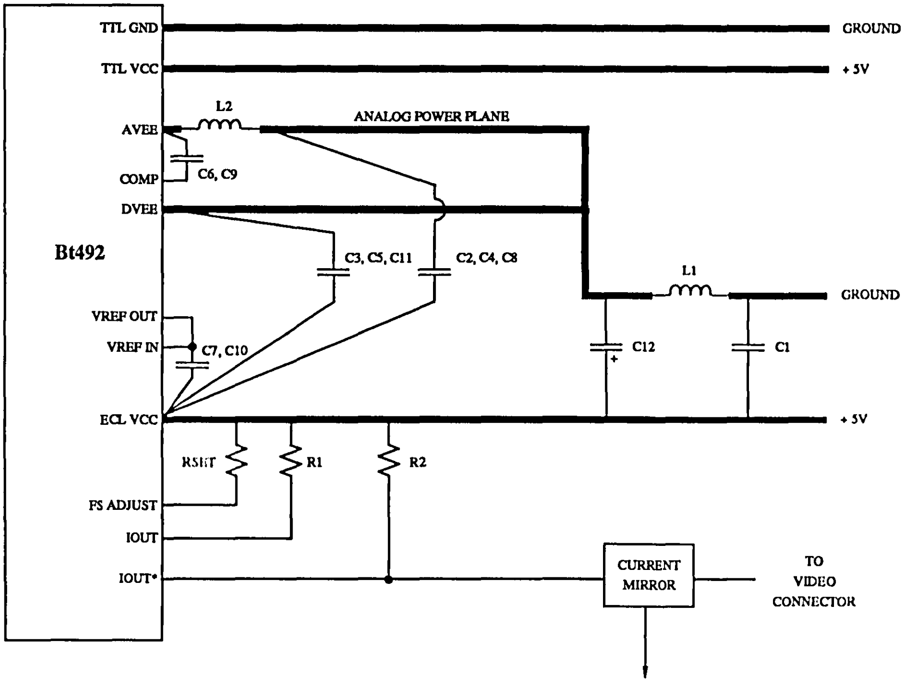

TTL VCC
+5V
L2
ANALOG POWER PLANE
AVEE
C6, C9
COMP
DVEE
Bt492
C3, C5, C11
C2, C4, C8
L1
-4.5V
VREF OUT
VREF IN
C7, C10
C12
+
C1
TTL GND,
ECL VCC
GROUND
RSET
R1
R2
FS ADJUST
IOUT
IOUT*
TO
VIDEO
CONNECTOR

Location	Description	Vendor Part Number
C1	0.1 µF ceramic capacitor	Mallory CK05BX104K
C2, C3	0.1 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W104KP
C4–C7	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W103KP
C8–C11	0.001 µF ceramic chip capacitor	Johanson Dielectrics NPO-500S41N102JP
C12	10 µF capacitor	Mallory CSR13G106KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1	24.9 Ω 1% metal film resistor	Dale CMF-55C
R2	49.9 Ω 1% metal film resistor	Dale CMF-55C
RSET	732 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt492. R1, R2, and RSET values assume doubly terminated 50 Ω load on IOUT*.

Figure 4. Typical Connection Diagram and Parts List (Dual Supply Operation).

PC Board Layout Considerations (continued)


TTL GND
TTL VCC
AVEE
COMP
DVEE
Bt492
VREF OUT
VREF IN
ECL VCC
FS ADJUST
IOUT
IOUT*
GROUND
+5V
L2
ANALOG POWER PLANE
C6, C9
C3, C5, C11
C2, C4, C8
L1
GROUND
C7, C10
C12
C1
+5V
RSET
R1
R2
CURRENT MIRROR
TO VIDEO CONNECTOR

Location	Description	Vendor Part Number
C1	0.1 µF ceramic capacitor	Mallory CK05BX104K
C2, C3	0.1 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W104KP
C4–C7	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W103KP
C8–C11	0.001 µF ceramic chip capacitor	Johanson Dielectrics NPO-500S41N102JP
C12	10 µF capacitor	Mallory CSR13G106KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1	24.9 Ω 1% metal film resistor	Dale CMF-55C
R2	49.9 Ω 1% metal film resistor	Dale CMF-55C
RSET	732 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt492. R1, R2, and RSET values assume doubly terminated 50 Ω load on IOUT*.

Figure 5. Typical Connection Diagram and Parts List (Single Supply Operation).

Application Information

Terminated ECL Inputs

All ECL inputs of the Bt492 should be terminated using normal ECL termination practices. In addition, all of the ECL digital inputs have internal pull-down junctions. Thus, if an ECL digital input is left floating, it assumes the logical zero state.

External Voltage Reference

An external voltage reference may be used with the Bt492, as shown in Figure 6. In this instance, the VREF OUT pin should be left floating.

Note that the VREF IN pin still requires bypass capacitors to ECL VCC.

Single Supply Operation

The Bt492 may be operated from a single +5 V supply by connecting the power supply pins as shown:

TTL VCC = +5 V
TTL GND = 0 V
ECL VCC = +5 V
DVEE, AVEE = 0 V

The current mirror on the analog output is required to reference the video signal to ground rather than +5 V.

Using Multiple Bt492s

For color applications, three Bt492s may be used, as illustrated in Figure 7. This example generates 256 simultaneous colors from a 16.8 million color palette and supports a 2k x 2k pixel resolution.

Both the even and odd pixel data require separate shift registers (Bt424s). The MPU TTL address bus is also interfaced to the Bt492 pixel inputs via the Bt424s.

Note the DIV2OUT–DIV2IN connections, generating CLOCK*/2 and ensuring the three Bt492s operate in a synchronous fashion. When analyzing the timing window for DIV2IN, be sure to include the propagation delay of the CLOCK and DIV2OUT signals through the transmission lines of the physical layout on the PC board.

The Bt492s may share the voltage reference and analog power/ground planes, but each Bt492 must have its own power supply decoupling, COMP decoupling, VREF IN decoupling, AVEE ferrite bead, RSET resistor, and IOUT termination resistors.

Optimum layout should minimize CLOCK and DIV2 line length. Low dielectric stripline is recommended, and the propagation delays between CLOCK and DIV2 should match as closely as possible.

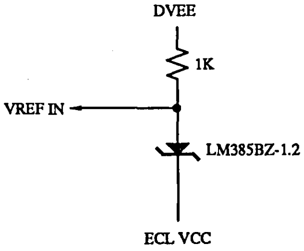


Figure 6. External Voltage Reference.

Application Information (continued)

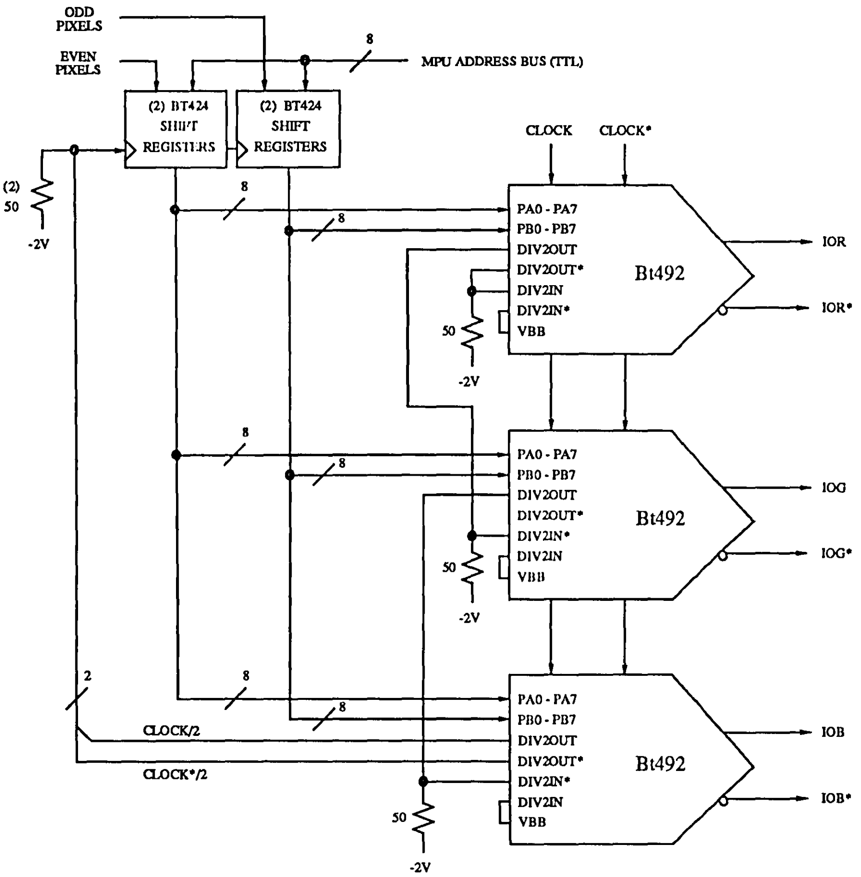

ODD PIXELS
EVEN PIXELS
8
MPU ADDRESS BUS (TTL)
(2) BT424 SHIFT REGISTERS
(2) BT424 SHIFT REGISTERS
(2) 50
-2V
CLOCK
CLOCK*
PA0 - PA7
PB0 - PB7
DIV2OUT
DIV2OUT*
DIV2IN
DIV2IN*
VBB
Bt492
IOR
IOR*
IOG
IOG*
IOB
IOB*
50
-2V
2
CLOCK/2
CLOCK*/2

Figure 7. Using Multiple Bt492s.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
ECL Power Supply	DVEE, AVEE	–4.2	–4.5	–5.5	Volts
ECL Ground	ECL VCC		0		Volts
TTL Power Supply	TTL VCC	4.75	5	5.25	Volts
TTL Ground	TTL GND		0		Volts
Ambient Operating Temperature	TA	0		+ 70	°C
Output Load	RL		25		Ω
Reference Voltage	VREF IN	–1.17	–1.23	–1.29	Volts
FS ADJUST Resistor	RSET		729		Ω

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
ECL Supply (measured to ECL VCC)	DVEE, AVEE			-6.5	Volts
TTL Supply (measured to GND)	TTL VCC			+7.0	Volts
Voltage on Any ECL Input Pin		ECL VCC		DVEE	Volts
Voltage on Any TTL Pin		TTL GND –0.5		TTL VCC +0.5	Volts
Analog Output Short Circuit Duration to Any Common			indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4 inch from pin)	TSOL			260	°C
Junction-to-Ambient					
Still Air				28	°C/W
400 LFM				13	°C/W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			±1/2	LSB
Differential Linearity Error	DL			±1/2	LSB
Gray Scale Error					
Internal Reference				±10	% Gray Scale
External Reference				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
TTL Digital Inputs					
Input High Voltage	VIH	2.0		TTL VCC +0.5	Volts
Input Low Voltage	VIL	TTL GND -0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			70	µA
Input Low Current (Vin = 0.4 V)	IIL			-700	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		6		pF
TTL Digital Outputs					
Output High Voltage (IOH = -2 mA)	VOH	2.4			Volts
Output Low Voltage (IOL = 20 mA)	VOL			0.4	Volts
3-State Current	IOZ	-50		50	µA
Output Capacitance	CDOUT		8		pF
ECL Digital Inputs					
Input High Voltage	VIH	-1165		-880	mV
Input Low Voltage	VIL	-1810		-1475	mV
Input High Current	IIH			220	µA
Input Low Current	IIL	0.5			µA
Input Capacitance (f = 1 MHz, Vin = VIHmax)	CIN		6		pF
CLOCK, CLOCK* Differential Input Voltage		±400			mV
ECL Digital Outputs					
Output High Voltage	VOH	-1025		-880	mV
Output Low Voltage	VOL	-1810		-1620	mV
Output Capacitance	CDOUT		7		pF

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Analog Output					
Gray Scale Current Range		−10		−40	mA
Output Current*					
White Level		0	-5	-50	µA
Black Level Relative to White		−25.08	−26.40	−27.72	mA
Blank Level Relative to Black					
SETUP = ECL VCC		0	0	0	mA
SETUP = float		−2.05	−2.16	−2.28	mA
Blank Level Relative to White		−27.13	−28.56	−30	mA
LSB Size			−103.5		µA
Output Compliance	VOC	−1.2		+ 1.5	Volts
Output Impedance	ROUT		10		KΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		9		pF
Reference Input Current	IREF IN			10	µA
Reference Output Voltage	VREF OUT	−1.175	−1.235	−1.295	Volts
Reference Output Current	IREF OUT	−200			µA
VREF OUT Tempco			± 75		ppm
VBB Output Voltage (load = 500 µA)	VBB	−1260	−1320	−1380	mV
Power Supply Rejection Ratio (COMP = 0.001 µF ‖ 0.01 µF, f = 1 kHz)	PSRR		0.1		% / % Δ AVEE

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for −28.56 mA full-scale output current, VREF IN = -1.21 V, SETUP = float. All ECL inputs have 50 Ω to −2.0 V. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*When using internal reference, RSET may need to be adjusted to meet these limits.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			360	MHz
CS* and Address Setup Time	1	10			ns
CS* and Address Hold Time	2	20			ns
RDx* Asserted to Data Bus Driven	3	10			ns
RDx* Asserted to Data Valid	4			30	ns
RDx* Negated to Data Bus 3-Stated	5			10	ns
WR* Pulse Width Low	6	75			ns
Write Data Setup Time	7	45			ns
Write Data Hold Time	8	10			ns
Pixel and Control Setup Time	9	0			ns
Pixel and Control Hold Time	10	1			ns
Clock Cycle Time	11	2.8			ns
Clock Pulse Width High	12	1			ns
Clock Pulse Width Low	13	1			ns
DIV2OUT Delay**	14	0.5		1.5	ns
DIV2IN Setup Time (to rising edge of CLOCK)	15	0.5			ns
DIV2IN Hold Time (to rising edge of CLOCK)	16	0.5			ns
Analog Output Delay	17		4		ns
Analog Output Rise/Fall Time				1	ns
Analog Output Settling Time	18		3	5	ns
Clock and Data Feedthrough*			tbd		dB
Glitch Impulse*			5		LSB - ns
Pipeline Delay		3	3	3	Clocks
DVEE + AVEE Supply Current	IEE			635	mA
TTL VCC Supply Current	ICC			65	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for –28.56 mA full-scale output current, VREF IN = –1.21 V, SETUP = float. ECL input values are –0.95 to –1.69 V, with input rise/fall times ≤ 1 ns, measured between the 20% and 80% points. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. All ECL inputs have 50 Ω to –2.0 V, unless other specified. Analog output load ≤ 10 pF. See timing notes in Figure 10. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Settling time does not include clock and data feedthrough. –3 dB test bandwidth = 720 MHz.

**Tested with three ECL loads.

Timing Waveforms

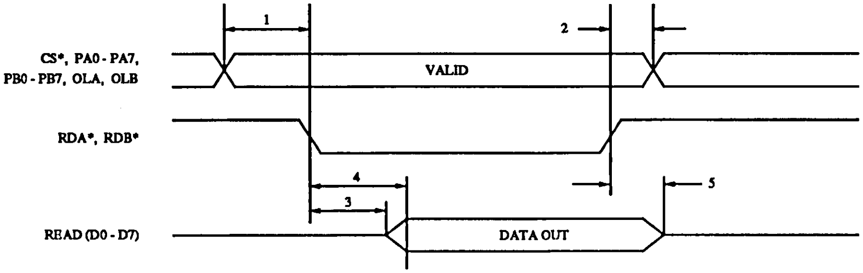

1
2
CS*, PA0 - PA7,
PB0 - PB7, OLA, OLB
VALID
RDA*, RDB*
4
3
5
READ (D0 - D7)
DATA OUT

Figure 8. MPU Read Timing.

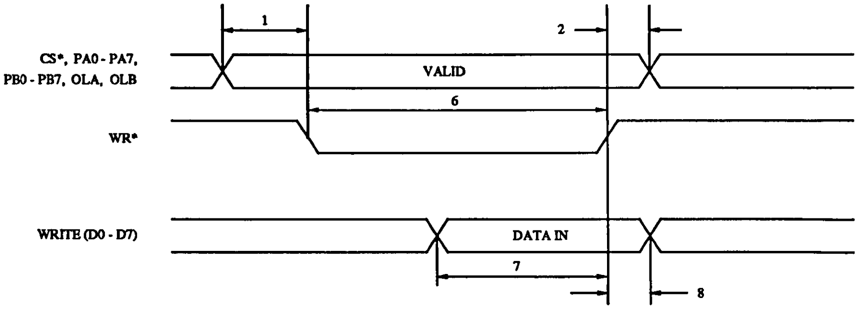
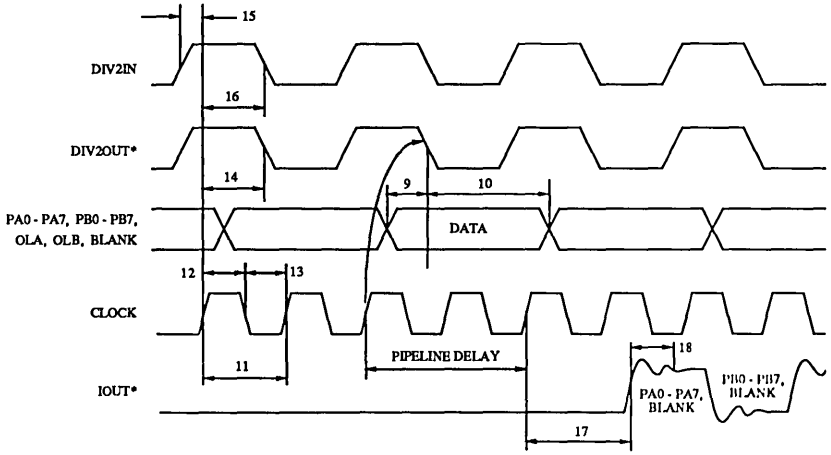

1
2
CS*, PA0 - PA7,
PB0 - PB7, OLA, OLB
VALID
6
WR*
WRITE (D0 - D7)
DATA IN
7
8

Figure 9. MPU Write Timing.

Timing Waveforms (continued)


15
DIV2IN
16
DIV2OUT*
14
9
10
PA0 - PA7, PB0 - PB7,
OLA, OLB, BLANK
DATA
12
13
CLOCK
11
PIPELINE DELAY
18
IOUT*
PA0 - PA7,
BLANK
PB0 - PB7,
BLANK
17

Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1%.

Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 10. Video Input/Output Timing.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt492KG360	360 MHz	68-pin Ceramic PGA with Alignment Pin and Heatsink	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
E	Added COMP Decoupling information to PCB layout section.

SECTION 5

VIDEODACs

Contents

Bt101 50, 30 MHz Triple 8-bit VIDEODAC 5 - 5

Bt102 75 MHz Single 8-bit VIDEODAC with Programmable Setup 5 - 19

Bt103 75, 30 MHz Triple 4-bit VIDEODAC 5 - 33

Bt106 50, 30 MHz Single 8-bit VIDEODAC 5 - 47

Bt107 400 MHz Single 8-bit VIDEODAC with 2:1 Multiplexed Pixel Inputs (10KH/100K ECL) 5 - 61

Bt109 250 MHz Triple 8-bit VIDEODAC, TDC1318 Pin Compatible (10KH ECL) 5 - 75

Bt121 80, 50, MHz Triple 8-bit VIDEODAC with Internal Voltage Reference and Analog Output Comparator 5 - 89

VIDEODAC Selection Guide

D/A Organization	Speed (MHz)	Part Number	Page	DL Error (LSB)	IL Error (LSB)	
triple 4-bit	75, 30	Bt103	5 - 33	±1/16	±1/8	monolithic CMOS
single 8-bit	400	Bt107	5 - 61	±1/2	±1/2	2:1 muxed inputs
single 8-bit	75	Bt102	5 - 19	±1/4	±1/2	programmable setup
single 8-bit	50, 30	Bt106	5 - 47	±1	±1	monolithic CMOS
triple 8-bit	250	Bt109	5 - 75	±1/2	±1/2	10KH ECL
triple 8-bit	80, 50	Bt121	5 - 89	±1	±1	internal reference
triple 8-bit	50, 30	Bt101	5 - 5	±1	±1	monolithic CMOS

	Display Resolution				
DAC Size	Low (640 x 480)	Medium (1k x 800)	High (1280 x 1024)	Medium High (1600 x 1200)	Ultra High (2k x 2k)
4-bit	Bt103	Bt103			
8-bit	Bt101 Bt102 Bt106 Bt121	Bt102 Bt121	Bt109	Bt109	Bt107

Bt101

50 MHz
Monolithic CMOS
Triple 8-bit
VIDEODAC™

Distinguishing Features

- 50, 30 MHz Operation
- Triple 8-bit D/A Converters
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- Guaranteed Monotonic
- RS-343A/RS-170 Compatible Outputs
- TTL Compatible Inputs
- +5 V CMOS Monolithic Construction
- 40-pin DIP or 44-pin PLCC Package
- Typical Power Dissipation: 600 mW

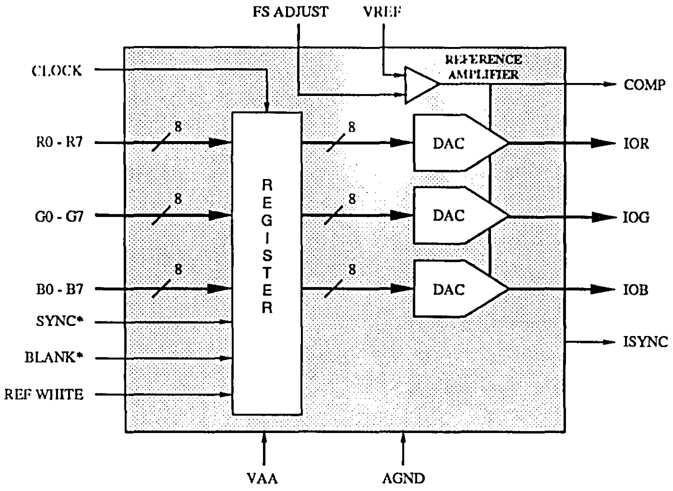
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction
- Instrumentation

Related Products

- Bt473, Bt121

Functional Block Diagram



Product Description

The Bt101 is a triple 8-bit VIDEODAC, designed specifically for high-performance, high-resolution color graphics.

Available control inputs include sync, blank, and reference white. The reference white input forces the analog outputs to the reference white level, regardless of the data inputs.

An external 1.2 V voltage reference and a single resistor control the full-scale output current. The sync, blank, and reference white inputs are pipelined to maintain synchronization with the digital input data.

The Bt101 generates RS-343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L101001 Rev. I

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt101 contains three 8-bit D/A converters, input registers, and a reference amplifier.

On the rising edge of each clock cycle, as shown below in Figure 1, 24 bits of color information (R0–R7, G0–G7, and B0–B7) are latched into the device and presented to the three 8-bit D/A converters. The REF WHITE input, also latched on the rising edge of each clock cycle, forces the inputs of each D/A converter to $FF.

Latched on the rising edge of CLOCK to maintain synchronization with the color data, the SYNC* and BLANK* inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as illustrated in Figure 2. Table 1 details how the SYNC*, BLANK*, and REF WHITE inputs modify the output levels.

The ISYNC current output is typically connected directly to the IOG output and is used to encode sync information onto the IOG output. If ISYNC is not connected to the IOG output, sync information will not be encoded on the green channel, and the IOR, IOG, and IOB outputs will have the same full-scale output current.

Full-scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 542 Ω for generation of RS-343A video into a 37.5 Ω load. The VREF input requires an external 1.2 V (typical) reference. For maximum performance, the voltage reference should be temperature compensated and provide a low-impedance output.

The D/A converters on the Bt101 use a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt101 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

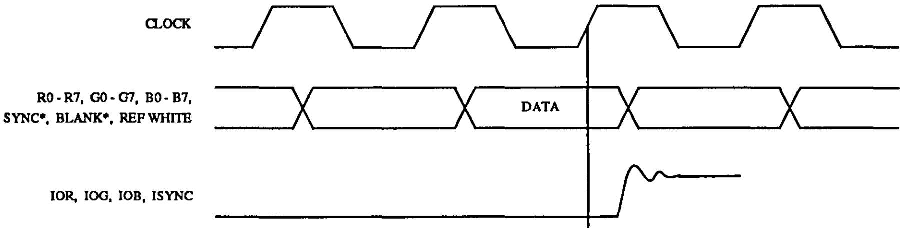
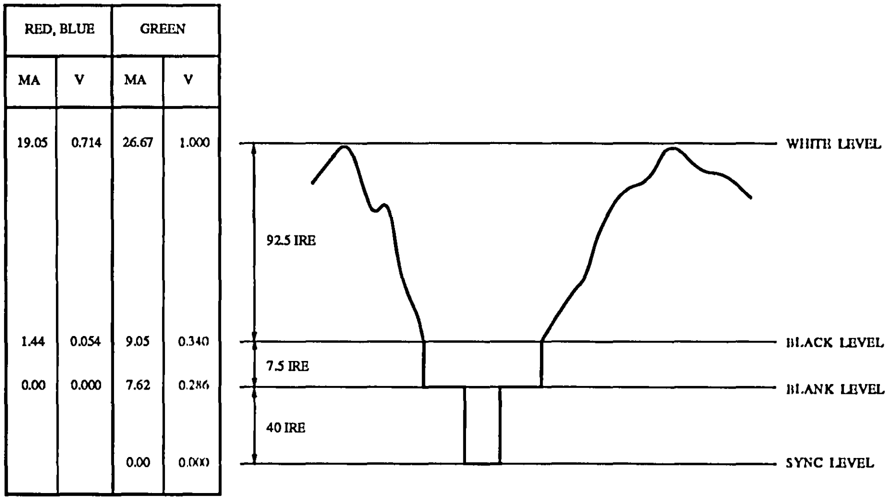


Figure 1. Input/Output Timing.

Circuit Description (continued)



Note: 75 Ω doubly terminated load, RSET = 542 Ω, VREF = 1.2 V. ISYNC connected to IOG. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms.

Description	IOG (mA)	IOR, IOB (mA)	REF WHITE	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	1	1	1	$xx
WHITE	26.67	19.05	0	1	1	$FF
DATA	data + 9.05	data + 1.44	0	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	0	1	data
BLACK	9.05	1.44	0	1	1	$00
BLACK - SYNC	1.44	1.44	0	0	1	$00
BLANK	7.62	0	x	1	0	$xx
SYNC	0	0	x	0	0	$xx

Note: Typical with full-scale IOG = 26.67 mA. RSET = 542 Ω, VREF = 1.2 V. ISYNC connected to IOG.

Table 1. Video Output Truth Table.

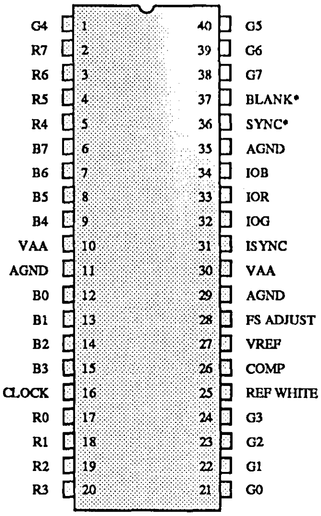
Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the IOR, IOG, and IOB outputs to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the R0–R7, G0–G7, B0–B7, and REF WHITE inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the ISYNC output (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 1; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
REF WHITE	Reference white control input (TTL compatible). A logical one on this input forces the IOR, IOG, and IOB outputs to the white level, regardless of the R0–R7, G0–G7, and B0–B7 inputs. It is latched on the rising edge of CLOCK. See Table 1.
R0–R7, G0–G7, B0–B7	Red, green, and blue data inputs (TTL compatible). R0, G0, and B0 are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary. Unused inputs should be connected to either the regular PCB power or ground plane.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, SYNC*, BLANK*, and REF WHITE inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 3). All outputs, whether used or not, should have the same output load.
ISYNC	Sync current output. Typically, this current output is directly wired to the IOG output, and enables sync information to be encoded onto the green channel. A logical zero on the SYNC* input results in no current being output onto this pin, while a logical one results in the following current being output: $\text{ISYNC (mA)} = 3{,}442 * \text{VREF (V)} / \text{RSET} (\Omega)$ If sync information is not required on the green channel, this output should be connected to AGND.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full-scale video signal (Figure 2). Note that the IRE relationships in Figure 2 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG (assuming ISYNC is connected to IOG) is: $\text{RSET} (\Omega) = 12{,}046 * \text{VREF (V)} / \text{IOG (mA)}$ The full-scale output current on IOR and IOB for a given RSET is defined as: $\text{IOR, IOB (mA)} = 8{,}604 * \text{VREF (V)} / \text{RSET} (\Omega)$

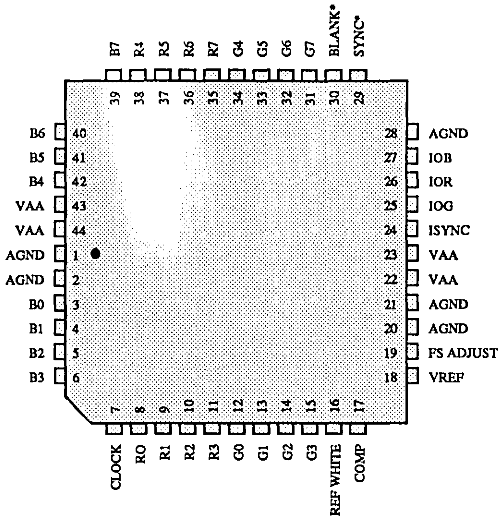
Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic capacitor in series with a resistor must be connected between this pin and the nearest VAA pin (Figure 3). Connecting the capacitor to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 3, must supply this input with a 1.2 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected.

40-pin CERDIP Package


G4 1
R7 2
R6 3
R5 4
R4 5
B7 6
B6 7
B5 8
B4 9
VAA 10
AGND 11
B0 12
B1 13
B2 14
B3 15
CLOCK 16
R0 17
R1 18
R2 19
R3 20
40 G5
39 G6
38 G7
37 BLANK*
36 SYNC*
35 AGND
34 IOB
33 IOR
32 IOG
31 ISYNC
30 VAA
29 AGND
28 FS ADJUST
27 VREF
26 COMP
25 REF WHITE
24 G3
23 G2
22 G1
21 G0

44-pin Plastic J-Lead (PLCC) Package


B7 39
R4 38
R5 37
R6 36
R7 35
G4 34
G5 33
G6 32
G7 31
BLANK* 30
SYNC* 29
B6 40
B5 41
B4 42
VAA 43
VAA 44
AGND 1
AGND 2
B0 3
B1 4
B2 5
B3 6
28 AGND
27 IOB
26 IOR
25 IOG
24 ISYNC
23 VAA
22 VAA
21 AGND
20 AGND
19 FS ADJUST
18 VREF
7 CLOCK
8 R0
9 R1
10 R2
11 R3
12 G0
13 G1
14 G2
15 G3
16 REF WHITE
17 COMP

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt101 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and AGND pins should be as short as possible to minimize inductive ringing.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8-inch gap) connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk. The analog ground plane should include all Bt101 ground pins, all reference circuitry and decoupling, power supply bypass circuitry for the Bt101, analog output traces, and the video output connector.

Power Planes

The Bt101 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt101.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt101 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged so that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 µF ceramic capacitor should be used to decouple each of the two groups of VAA pins to AGND. These capacitors should be placed as close as possible to the device.

It is important to note that while the Bt101 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three-terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt101 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Due to the high clock rates involved, long clock lines to the Bt101 should be avoided to reduce noise pickup.

Any termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

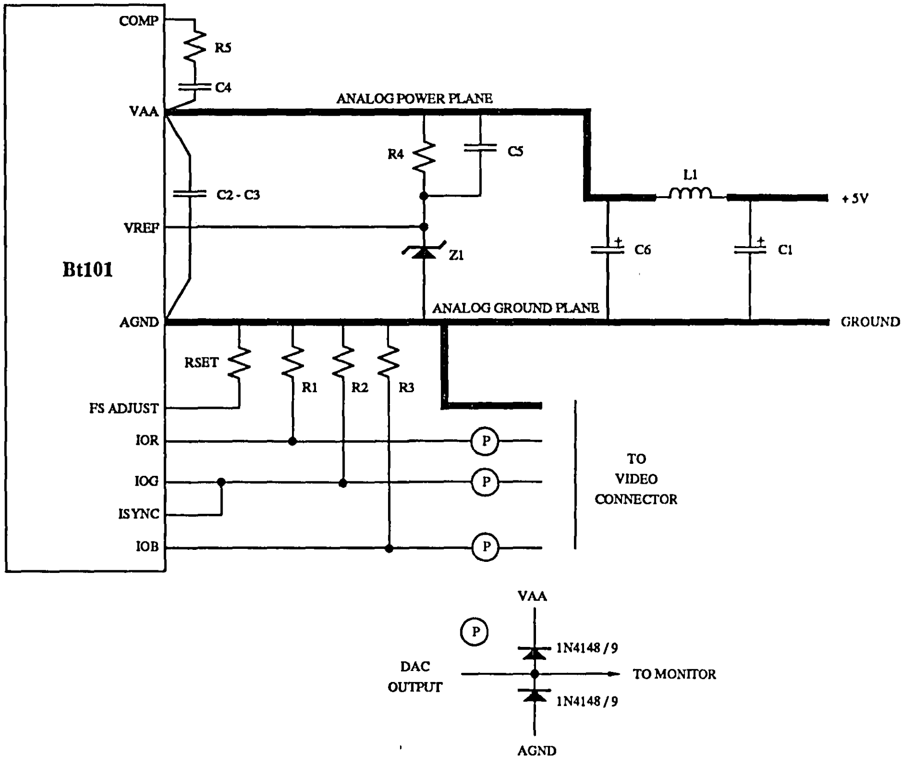
Analog Signal Interconnect

The Bt101 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75 Ω load resistor connected to AGND. The connection between the current output and AGND should be as close as possible to the Bt101 to minimize reflections.

PC Board Layout Considerations (continued)


COMP
R5
C4
VAA
ANALOG POWER PLANE
R4
C5
L1
+5V
C2 - C3
VREF
Z1
C6
C1
Bt101
ANALOG GROUND PLANE
AGND
GROUND
RSET
R1
R2
R3
FS ADJUST
IOR
IOG
ISYNC
IOB
P
TO VIDEO CONNECTOR
VAA
P
1N4148/9
DAC OUTPUT
TO MONITOR
1N4148/9
AGND

Location	Description	Vendor Part Number
C1	33 μF tantalum capacitor	Mallory CSR13F336KM
C2, C3, C5	0.1 μF ceramic capacitor	Eric RPE112Z5U104M50V
C4	0.01 μF ceramic capacitor	Eric RPE110Z5U103M50V
C6	10 μF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 1% metal film resistor	Dale CMF-55C
R5	15 Ω 1% metal film resistor	Dale CMF-55C
RSET	549 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt101.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that a singly terminated 75 Ω load be used with an RSET value of about 774 Ω. If the Bt101 is not driving a large capacitive load, there will be negligible difference in video quality between doubly terminated 75 Ω and singly terminated 75 Ω loads.

If driving a large capacitive load (load RC > 1/(20 $f_C\pi$))*, it is recommended that an output buffer be used to drive a doubly terminated 75 Ω load.

COMP Resistor

To optimize the settling time of the Bt101, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 15 Ω; however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time.

An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

Non-Video Applications

The Bt101 may be used in non-video applications by disabling the video-specific control inputs. SYNC* and REF WHITE should be a logical zero and BLANK* should be a logical one. ISYNC should be connected to AGND. All three outputs will have the same full-scale output current.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

RSET (Ω) = 7,958 * VREF (V) / Iout (mA)

With the data inputs at $00, there is a DC offset current (Imin) defined as follows:

Imin (mA) = 650 * VREF (V) / RSET (Ω)

Therefore, the total full-scale output current will be Iout + Imin. The REF WHITE input may optionally be used as a "force to full-scale" control.

*(f_C = clock frequency)

Analog Output Protection

The Bt101 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 3 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA				
Bt101KC30, Bt101KPJ		0		+70	°C
Bt101BC		–25		+85	°C
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.14	1.20	1.26	Volts
FS ADJUST Resistor	RSET		542		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
Voltage on any Signal Pin*		AGND – 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL		±0.3	±1	LSB
Differential Linearity Error	DL		±0.3	±1	LSB
Gray Scale Error			±1	±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	AGND – 0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
Analog Outputs					
Gray Scale Current Range		15		20	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			69.1		µA
DAC-to-DAC Matching			2		%
Output Compliance	VOC	–1.0		+1.4	Volts
Output Impedance	ROUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		30		pF
Voltage Reference Input Current	IREF			10	µA
Power Supply Rejection Ratio (COMP = 0.01 µF, f = 1 kHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 Ω, VREF = 1.200 V, ISYNC connected to IOG. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

		50 MHz Devices			30 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			50			30	MHz
Data and Control Setup Time	TSU	6			8			ns
Data and Control Hold Time	TH	2			2			ns
Clock Cycle Time	TCYC	20			33.3			ns
Clock Pulse Width High Time	TCLKH	8			10			ns
Clock Pulse Width Low Time	TCLKL	8			10			ns
Analog Output Delay	TDLY		25			25		ns
Analog Output Rise/Fall Time	TVRF			8			9	ns
Analog Output Settling Time	TS		12			15		ns
Clock and Data Feedthrough*			–28			–28		dB
Glitch Impulse*			100			100		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew			0	3		0	3	ns
Differential Gain Error	DG		1.8			1.8		% Gray Scale
Differential Phase Error	DP		1.2			1.2		Degrees
Pipeline Delay		1	1	1	1	1	1	Clock
VAA Supply Current**	IAA		120	175		100	140	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 Ω, VREF = 1.200 V, ISYNC connected to IOG. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. COMP resistor = 15 Ω. Analog output load ≤ 10 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

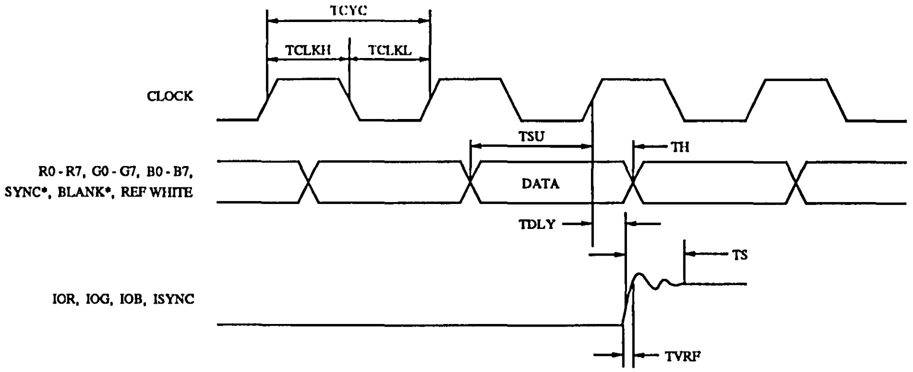
*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt101BC	50 MHz	40-pin 0.6" CERDIP	-25° to +85° C
Bt101KC30	30 MHz	40-pin 0.6" CERDIP	0° to +70° C
Bt101KPJ	30 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt101EVM	Evaluation Board for the Bt101		

Timing Waveforms


TCYC
TCLKH
TCLKL
CLOCK
TSU
TH
R0 - R7, G0 - G7, B0 - B7,
SYNC*, BLANK*, REF WHITE
DATA
TDLY
TS
IOR, IOG, IOB, ISYNC
TVRF

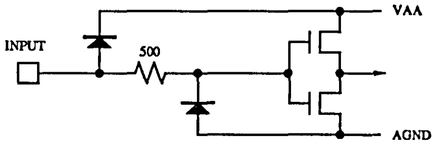
Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.

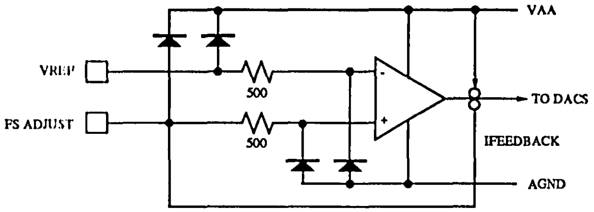
Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 4. Input/Output Timing.

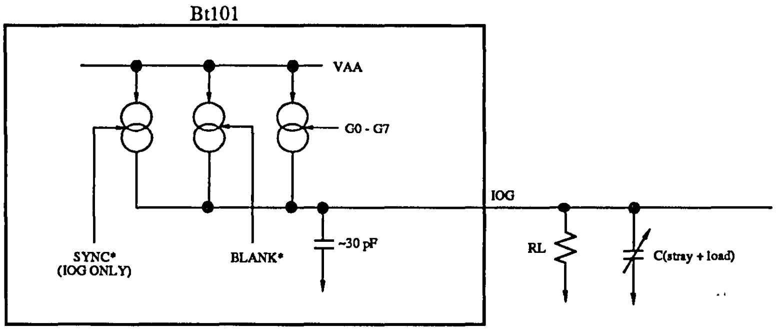
Device Circuit Data


VAA
INPUT
500
AGND

Equivalent Circuit of the Digital Inputs.


VAA
VREF
FS ADJUST
500
500
-
+
TO DACS
IFEEDBACK
AGND

Equivalent Circuit of the Reference Amplifier.


Bt101
VAA
G0 - G7
IOG
~30 pF
SYNC*
(IOG ONLY)
BLANK*
RL
C(stray + load)

Equivalent Circuit of the Current Output (IOG).

Bt102

75 MHz
Monolithic CMOS
Single 8-bit
VIDEODAC™

Distinguishing Features

- 75 MHz Pipelined Operation
- ±1/4 LSB Differential Linearity Error
- ±1/2 LSB Integral Linearity Error
- RS-343A/RS-170 Compatible Output
- 0, 7, or 10 IRE Programmable Setup
- +5 V CMOS Monolithic Construction
- 24-pin 0.3" DIP Package
- Typical Power Dissipation: 550 mW

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Conventional D/A

Product Description

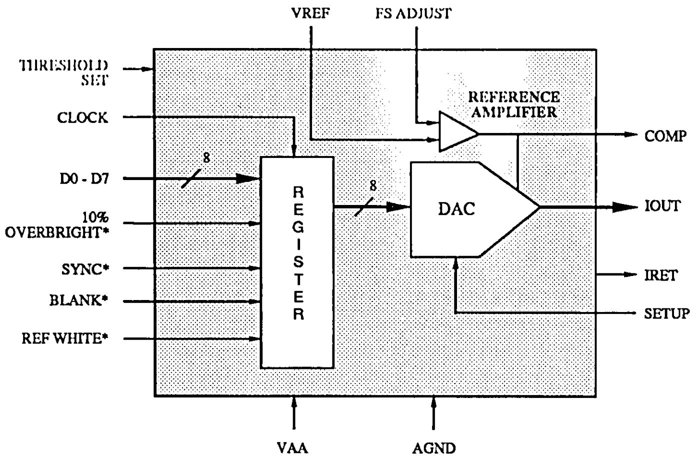
The Bt102 is an 8-bit multifunction VIDEODAC, designed specifically for color graphics and conventional D/A converter applications.

Available control inputs include sync, blank, reference white, and 10% overbright. Additional features include a threshold set input to configure the digital inputs to be either TTL or CMOS compatible, and a setup input to specify one of three available setups in the analog output.

An external 1.2 V voltage reference and a single resistor control the full-scale output current. The sync, blank, reference white, and 10% overbright inputs are pipelined to maintain synchronization with the input data.

The Bt102 generates RS-343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering. The differential and integral linearity errors of the D/A converter are guaranteed to be a maximum of ±1/4 LSB and ±1/2 LSB, respectively, over the full temperature range.

Functional Block Diagram



Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L102001 Rev. E

Circuit Description

As illustrated in the functional block diagram, the Bt102 contains a single 8-bit D/A converter, input registers, and a reference amplifier.

The THRESHOLD SET input controls the logic thresholds of the digital inputs. If it is left floating, the logic thresholds are TTL compatible; if connected to VAA, the thresholds are CMOS compatible.

On the rising edge of each clock cycle, as shown below in Figure 1, 8 bits of data (D0–D7) are latched into the device and presented to the 8-bit D/A converter. The REF WHITE* input, latched on the rising edge of CLOCK, forces the inputs of the D/A converter to $FF, regardless of the value of the D0–D7 inputs.

Latched on the rising edge of CLOCK to maintain synchronization with the data, the SYNC*, BLANK*, and 10% OVERBRIGHT* inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 2. Table 1 details how the SYNC*, BLANK*, REF WHITE*, and 10% OVERBRIGHT* inputs modify the output level.

The SETUP input is used to control the difference between the black and blanking level. Available setups include 10 IRE (SETUP = VAA), 7 IRE (SETUP = float), and 0 IRE (SETUP = AGND). A setup of 0 IRE specifies that the blanking level is the same as the black level.

Full-scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. The VREF input requires an external 1.2 V (typical) reference. For maximum performance, the voltage reference should be temperature compensated and provide a low-impedance output.

The D/A converter on the Bt102 uses a segmented architecture in which bit currents are routed to either the output or IRET by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog output of the Bt102 is capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

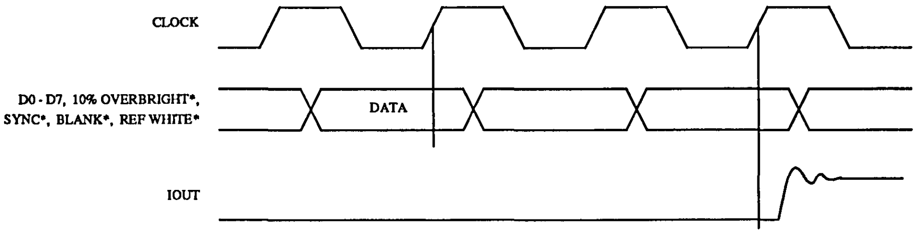
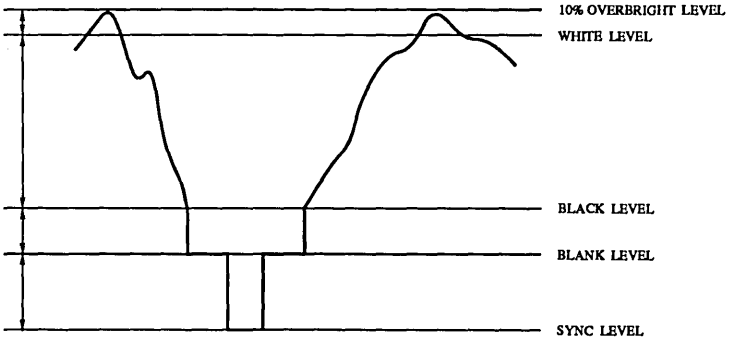


Figure 1. Input/Output Timing.

Circuit Description (continued)

RSET = 1130		RSET = 1110		RSET = 1050	
SETUP = VAA		SETUP = FLOAT		SETUP = AGND	
IRE	MA	IRE	MA	IRE	MA
	28.90		28.74		29.00
9.5		10		10.75	
	27.01		26.81		26.97
90		92.9		100	
	9.59		9.09		8.23
10		7.1		0	
	7.65		7.72		8.23
39.5		40.5		44	
	0.00		0.00		0.00



Note: 75 Ω doubly terminated load, VREF = 1.235 V. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveform.

Description	IOUT (mA)	10% OVERBRIGHT*	REF WHITE*	SYNC*	BLANK*	DAC Input Data
WHITE +10%	28.74	0	1	1	1	$FF
WHITE	26.81	1	0	1	1	$xx
WHITE	26.81	1	1	1	1	$FF
DATA + 10%	data + 11.0	0	1	1	1	data
DATA	data + 9.09	1	1	1	1	data
DATA - SYNC	data + 1.37	1	1	0	1	data
BLACK	9.09	1	1	1	1	$00
BLACK - SYNC	1.37	1	1	0	1	$00
BLANK	7.72	x	x	1	0	$xx
SYNC	0	x	x	0	0	$xx

Note: Typical with white level current = 26.81 mA. RSET = 1110 Ω, VREF = 1.235 V, SETUP = float.

Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL/CMOS compatible). A logical zero drives the output to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the D0–D7, REF WHITE*, and 10% OVERBRIGHT* inputs are ignored.
SYNC*	Composite sync control input (TTL/CMOS compatible). A logical zero on this input switches off a current source on the output equal to approximately 30% of the full-scale current (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 1; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
REF WHITE*	Reference white control input (TTL/CMOS compatible). A logical zero on this input forces the output to the white level, regardless of the D0–D7 inputs. It is latched on the rising edge of CLOCK. See Table 1.
10% OVERBRIGHT*	Overbright control input (TTL/CMOS compatible). A logical zero on this input causes the output current to increase by approximately 10 IRE units as shown in Table 1 and Figure 2. It is latched on the rising edge of CLOCK.
D0–D7	Data inputs (TTL/CMOS compatible). D0 is the least significant data bit. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (TTL/CMOS compatible). The rising edge of CLOCK latches the D0–D7, SYNC*, BLANK*, REF WHITE*, and 10% OVERBRIGHT* inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL or CMOS buffer to avoid reflection-induced jitter.
SETUP	Setup control input. This pin controls the difference between the black level and the blanking level. Available setups include 10 IRE units (SETUP = VAA), 7 IRE units (SETUP = float), and 0 IRE units (SETUP = AGND).
THRESHOLD SET	Threshold control input. This pin controls the logic thresholds of the digital inputs. If connected to VAA through a 0.1 µF ceramic capacitor, the logic thresholds are TTL compatible. If connected directly to VAA, the thresholds are CMOS compatible.
IOUT	Current output. This high-impedance current source is capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 3).
IRET	Current return. This pin must be connected to AGND through a ferrite bead, as illustrated in Figure 3.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected.
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 3, must supply this input with a 1.2 V (typical) reference. The use of a resistor network to generate the reference is not recommended, as any low-frequency power supply noise on VREF will be directly coupled onto the analog outputs. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.

Pin Descriptions (continued)

Pin Name — **Description**

COMP

Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 μF ceramic capacitor in series with a resistor must be connected between this pin and the adjacent VAA pin (Figure 3). Connecting the capacitor to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.

FS ADJUST

Full-scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full-scale video signal (Figure 3). Note that the IRE relationships in Figure 3 are maintained regardless of the full-scale output current.

The relationship between RSET and the white level output current is:

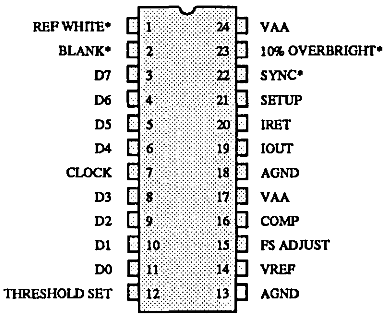
$$\text{RSET}\,(\Omega) = \text{K1} * \text{VREF}\,(\text{V}) / \text{IOUT}\,(\text{mA})$$

The amount of additional current generated to achieve the overbright level is:

$$\text{IOUT}'\,(\text{mA}) = \text{K2} * \text{VREF}\,(\text{V}) / \text{RSET}\,(\Omega)$$

K1 and K2 are defined as follows:

	SETUP		
	float	VAA	AGND
K1	24,096	24,713	22,930
K2	1,735	1,729	1,726


REF WHITE*
BLANK*
D7
D6
D5
D4
CLOCK
D3
D2
D1
D0
THRESHOLD SET
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
VAA
10% OVERBRIGHT*
SYNC*
SETUP
IRET
IOUT
AGND
VAA
COMP
FS ADJUST
VREF
AGND

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt102 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and AGND pins should be as short as possible so as to minimize inductive ringing.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8-inch gap) connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk. The analog ground plane should include all Bt101 ground pins, all reference circuitry and decoupling, power supply bypass circuitry for the Bt101, analog output traces, and the video output connector.

Power Planes

The Bt102 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt102.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt102 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged so that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 µF ceramic capacitor should be used to decouple each VAA pin to AGND. These capacitors should be placed as close as possible to the device.

It is important to note that, while the Bt102 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three-terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt102 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Due to the high clock rates involved, long clock lines to the Bt102 should be avoided to reduce noise pickup.

Any termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

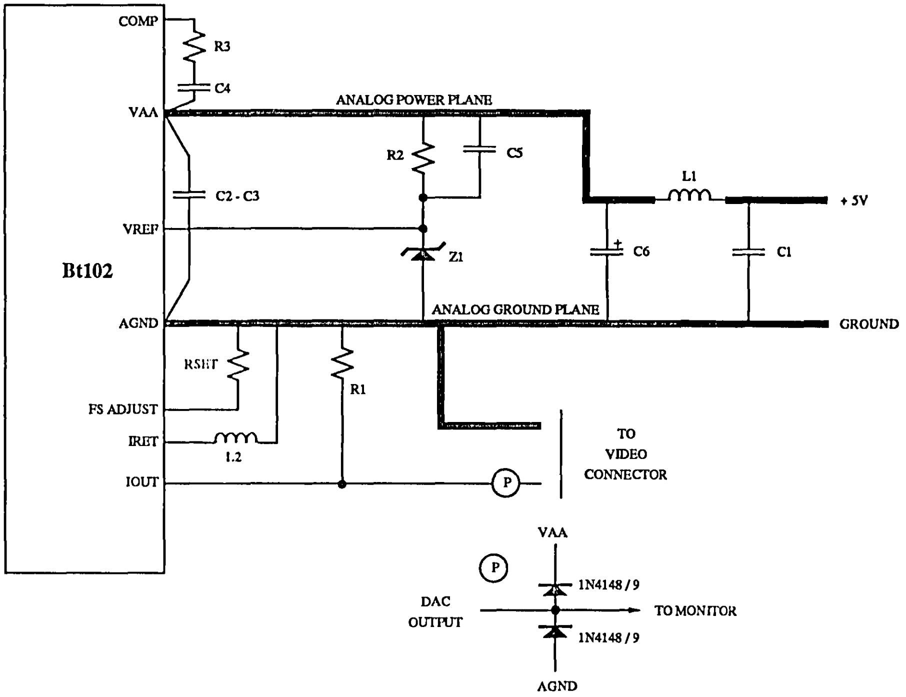
Analog Signal Interconnect

The Bt102 should be located as close as possible to the output connector to minimize noise pickup and reflections due to impedance mismatch.

The video output signal should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog output should have a 75 Ω load resistor connected to AGND. The connection between the current output and AGND should be as close as possible to the Bt102 to minimize reflections.

PC Board Layout Considerations (continued)


COMP
R3
C4
VAA
ANALOG POWER PLANE
R2
C5
L1
+5V
C2 - C3
VREF
Z1
C6
C1
Bt102
ANALOG GROUND PLANE
AGND
GROUND
RSET
R1
FS ADJUST
IRET
L2
TO
VIDEO
CONNECTOR
IOUT
P
VAA
P
1N4148/9
DAC
OUTPUT
TO MONITOR
1N4148/9
AGND

Location	Description	Vendor Part Number
C1, C2, C3, C5	0.1 µF ceramic capacitor	Eric RPE112Z5U104M50V
C4	0.01 µF ceramic capacitor	Eric RPE110Z5U103M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1	75 Ω 1% metal film resistor	Dale CMF-55C
R2	1000 Ω 1% metal film resistor	Dale CMF-55C
R3	27 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt102.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that a singly terminated 75 Ω load be used with the SETUP pin floating and an RSET value of about 1594 Ω. If the Bt102 is not driving a large capacitive load, there will be negligible difference in video quality between doubly terminated 75 Ω and singly terminated 75 Ω loads.

If driving a large capacitive load (load RC > 1/(20 $f_C\pi$))*, it is recommended that an output buffer be used to drive a doubly terminated 75 Ω load.

Color Applications

Note that in color applications, sync information is typically required only on the green channel. Therefore, the SYNC* inputs to the red and blue VIDEODACs may always be a logical zero. If SYNC* is always a logical zero, the relationship between RSET and the full-scale output current is:

IOUT (mA) = K * VREF (V) / RSET (Ω)

where K is equal to 17,714; 17,158; or 15,933 for SETUP = VAA, float, and AGND, respectively.

Using Multiple Devices

If located close together on the same PC board, multiple Bt102 devices may be connected to a single analog power and ground plane. In addition, a single voltage reference may be used to drive multiple devices.

Each Bt102 must still have its individual RSET resistor, IOUT termination resistor (R1 in Figure 3), IRET ferrite bead (L3 in Figure 3), power supply bypass capacitors (C2 and C3 in Figure 3), and COMP resistor and capacitor (C4 and R3 in Figure 3).

At high clock rates, individual ground beads (L2 in Figure 3) may be required to maintain TTL thresholds due to the high current return.

Non-Video Applications

The Bt102 may be used in non-video applications by disabling the video-specific control inputs. SYNC* should be a logical zero, while REF WHITE*, 10% OVERBRIGHT*, and BLANK* should be a logical one. SETUP should be connected to AGND. The output current will be determined solely by the D0–D7 inputs.

The relationship between RSET and the full-scale output current in this configuration is as follows:

RSET (Ω) = 15,933 * VREF (V) / IOUT (mA)

The BLANK* input may optionally be used as a "force to zero" control, and the REF WHITE* input may optionally be used as a "force to full-scale" control.

COMP Resistor

To optimize the settling time of the Bt102, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 27 Ω, however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time.

An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

Analog Output Protection

The Bt102 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 3 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

*(f_C = clock frequency)

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	–25		+85	°C
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.14	1.235	1.26	Volts

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
Voltage on Any Signal Pin*		AGND – 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			±1/2	LSB
Differential Linearity Error	DL			±1/4	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
TTL-Compatible Mode					
Input High Voltage	VIH				
CLOCK		3.0		VAA + 0.5	Volts
Other		2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	AGND – 0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH	–200		–1200	µA
Input Low Current (Vin = 0.4 V)	IIL	–200		–1200	µA
Input Capacitance	CIN		10		pF
CMOS-Compatible Mode					
Input High Voltage	VIH	3.5		AGND + 0.5	Volts
Input Low Voltage	VIL	AGND – 0.5		0.8	Volts
Input High Current (Vin = 3.5 V)	IIH			2	µA
Input Low Current (Vin = 1.5 V)	IIL			2	µA
Input Capacitance	CIN		10		pF
Analog Output					
Gray Scale Current Range		15		20.5	mA
Output Current					
Overbright Relative to White		1.60	1.93	2.40	mA
White Level Relative to Blank		17.90	19.09	20.31	mA
White Level Relative to Black		16.80	17.72	18.61	mA
Black Level Relative to Blank					
SETUP = float		1.10	1.37	1.70	mA
SETUP = AGND		0	5	50	µA
SETUP = VAA		1.6	1.93	2.4	mA
Blanking Level		7.2	7.72	8.3	mA
Sync Level		0	5	50	µA
LSB Size			69.5		µA
Output Compliance	VOC	–1.0		+1.4	Volts
Output Impedance	ROUT		33		KΩ
Output Capacitance	COUT		20		pF
Voltage Reference Input Current	IREF			10	µA
Power Supply Rejection Ratio (COMP = 0.01 µF, f = 1 kHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with SETUP = float, RSET = 1110 Ω, VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			75	MHz
Data and Control Setup Time	TSU	4			ns
Data and Control Hold Time	TH	1			ns
Clock Cycle Time	TCYC	13.33			ns
Clock Pulse Width Low	TCLKH	5			ns
Clock Pulse Width High	TCLKL	6			ns
Analog Output Delay	TDLY		20		ns
Analog Output Rise/Fall Time	TVRF		6		ns
Analog Output Settling Time*	TS				
to ± 1/2 LSB			15		ns
to ± 1 LSB			12		ns
Clock and Data Feedthrough*			–20		dB
Glitch Impulse*			100		pV - sec
Differential Gain Error	DG		1		% Gray Scale
Differential Phase Error	DP		1		Degree
Pipeline Delay		3	3	3	Clocks
VAA Supply Current**	IAA		110	175	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 1110 Ω, VREF = 1.235 V. THRESHOLD SET = TTL mode, SETUP = float. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. COMP resistor = 27 Ω. Analog output load ≤ 10 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

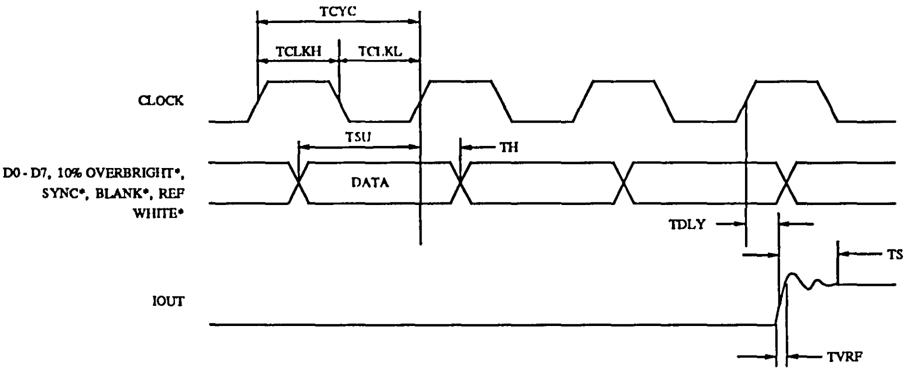
*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 150 MHz.

**At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt102BC	75 MHz	24-pin 0.3" CERDIP	–25° to +85° C
Bt102EVM	Evaluation Board for the Bt102		

Timing Waveforms


TCYC
TCLKH
TCLKL
CLOCK
TSU
TH
D0 - D7, 10% OVERBRIGHT*, SYNC*, BLANK*, REF WHITE*
DATA
TDLY
TS
IOUT
TVRF

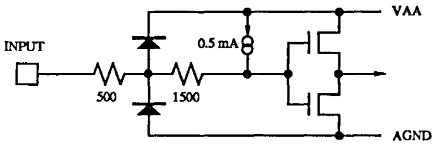
Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1/2 LSB or ±1 LSB.

Note 3: Output rise/fall time measured between the 20% and 80% points of full-scale transition.

Figure 4. Input/Output Timing.

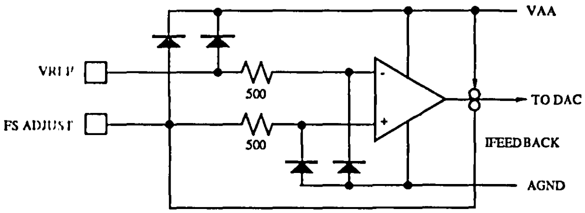
Device Circuit Data


VAA
INPUT
0.5 mA
500
1500
AGND

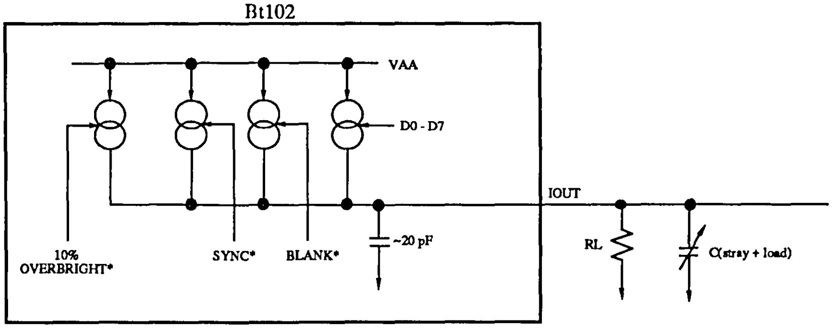
High-speed operation is accomplished through pipelining and a unique (patent pending) TTL input buffer. This input buffer features a resistive level shifter that uses a temperature and process-compensated current source.

The 0.5 mA bias current is disabled when THRESHOLD SET is connected to VAA, resulting in a standard high-impedance CMOS input.

Equivalent Circuit of the Digital Inputs.


VAA
VREF
FS ADJUST
500
500
TO DAC
IFEEDBACK
AGND

Equivalent Circuit of the Reference Amplifier.


Bt102
VAA
D0 - D7
IOUT
~20 pF
RL
C(stray + load)
10%
OVERBRIGHT*
SYNC*
BLANK*

Equivalent Circuit of the Current Output.

Bt103

75 MHz
Monolithic CMOS
Triple 4-bit
VIDEODAC™

Distinguishing Features

- 75, 30 MHz Operation
- Triple 4-bit D/A Converters
- ±1/16 LSB Differential Linearity Error
- ±1/8 LSB Differential Linearity Error
- RS-343A/RS-170 Compatible Outputs
- TTL-Compatible Inputs
- +5 V CMOS Monolithic Construction
- 28-pin DIP Package
- Typical Power Dissipation: 800 mW

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction

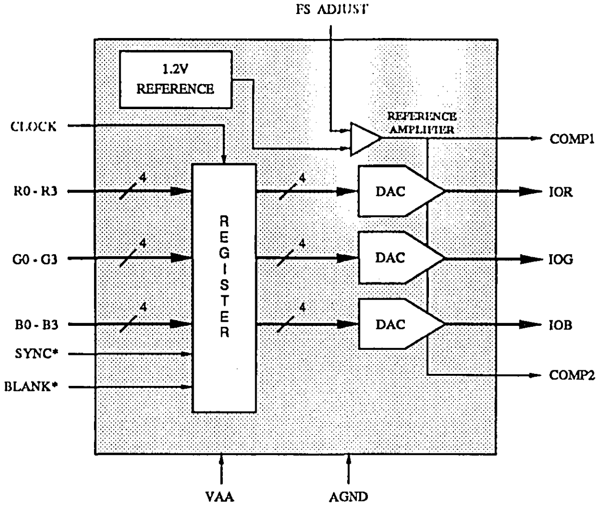
Product Description

The Bt103 is a triple 4-bit VIDEODAC, designed specifically for high-performance, high-resolution color graphics.

Available control inputs include sync and blank, both pipelined to maintain synchronization with the color data. An on-chip voltage reference simplifies design, and a single external resistor controls the full-scale output current.

The Bt103 generates RS-343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering. The differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1/16 LSB and ±1/8 LSB, respectively, over the full temperature range.

Functional Block Diagram



Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L103001 Rev. E

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt103 contains three 4-bit D/A converters, input registers, voltage reference, and a reference amplifier.

As shown below in Figure 1, on the rising edge of each clock cycle, 12 bits of color information (R0–R3, G0–G3, and B0–B3) are latched into the device and presented to the three 4-bit D/A converters.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK and pipelined to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 2. Table 1 details how the SYNC* and BLANK* inputs modify the output levels.

The full-scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 499 Ω for generation of RS-343A video into a 37.5 Ω load.

The D/A converters on the Bt103 use a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt103 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

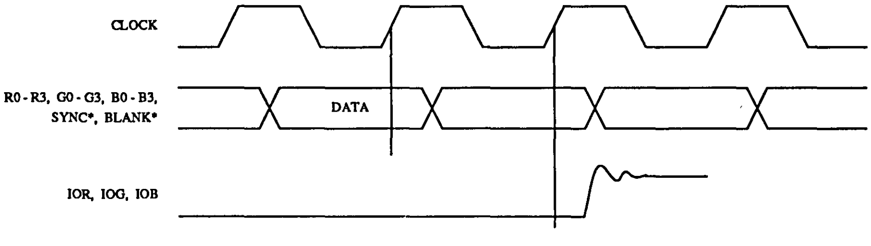
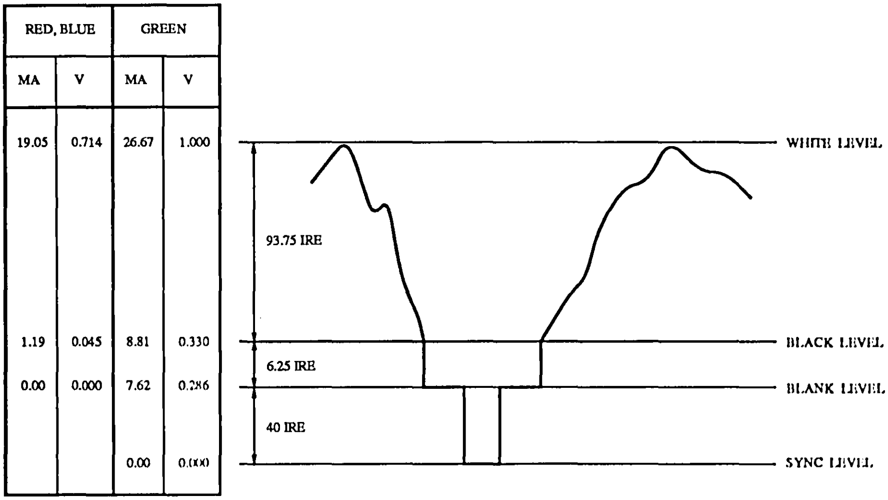


Figure 1. Input/Output Timing.

Circuit Description (continued)


RED, BLUE
GREEN
MA
V
MA
V
19.05
0.714
26.67
1.000
1.19
0.045
8.81
0.330
0.00
0.000
7.62
0.286
0.00
0.000
WHITE LEVEL
93.75 IRE
BLACK LEVEL
6.25 IRE
BLANK LEVEL
40 IRE
SYNC LEVEL

Note: 75 Ω doubly terminated load, RSET = 499 Ω. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms.

Description	IOG (mA)	IOR (mA)	IOB (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	19.05	19.05	1	1	$F
DATA	data + 8.81	data + 1.19	data + 1.19	1	1	data
DATA - SYNC	data+ 1.19	data + 1.19	data + 1.19	0	1	data
BLACK	8.81	1.19	1.19	1	1	$0
BLACK - SYNC	1.19	1.19	1.19	0	1	$0
BLANK	7.62	0	0	1	0	$x
SYNC	0	0	0	0	0	$x

Note: Typical with full-scale IOG = 26.67 mA. RSET = 499 Ω.

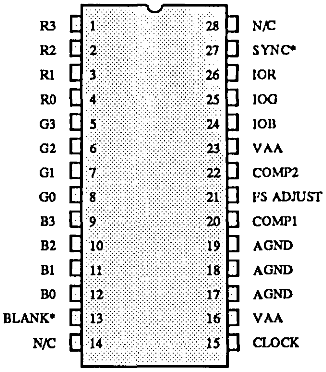
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the analog outputs to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the R0–R3, G0–G3, and B0–B3 inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOG output (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 1; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
R0–R3, G0–G3, B0–B3	Red, green, and blue data inputs (TTL compatible). R0, G0, and B0 are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R3, G0–G3, B0–B3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 3). All outputs, whether used or not, should have the same output load.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full-scale video signal (Figure 2). Note that the IRE relationships in Figure 2 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG is: RSET (Ω) = 13,308 / IOG (mA) The full-scale output current on IOR and IOB for a given RSET is defined as: IOR, IOB (mA) = 9,506 / RSET (Ω)

Pin Descriptions (continued)

Pin Name	Description
COMP1, COMP2	Compensation pins. These pins provide compensation for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between these two pins (Figure 3). The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.



R3 1
R2 2
R1 3
R0 4
G3 5
G2 6
G1 7
G0 8
B3 9
B2 10
B1 11
B0 12
BLANK* 13
N/C 14
28 N/C
27 SYNC*
26 IOR
25 IOG
24 IOB
23 VAA
22 COMP2
21 FS ADJUST
20 COMP1
19 AGND
18 AGND
17 AGND
16 VAA
15 CLOCK

Note: N/C pins may be left floating without affecting the performance of the Bt103.

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt103 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and AGND pins should be as short as possible to minimize inductive ringing.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8-inch gap) connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk. The analog ground plane should include all Bt101 ground pins, all reference circuitry and decoupling, power supply bypass circuitry for the Bt101, analog output traces, and the video output connector.

Power Planes

The Bt103 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt103.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt103 power pins and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged so that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 µF ceramic capacitor should be used to decouple each VAA pin to AGND. These capacitors should be placed as close as possible to the device.

It is important to note that, while the Bt103 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three-terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt103 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Due to the high clock rates involved, long clock lines to the Bt103 should be avoided to reduce noise pickup.

Any termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

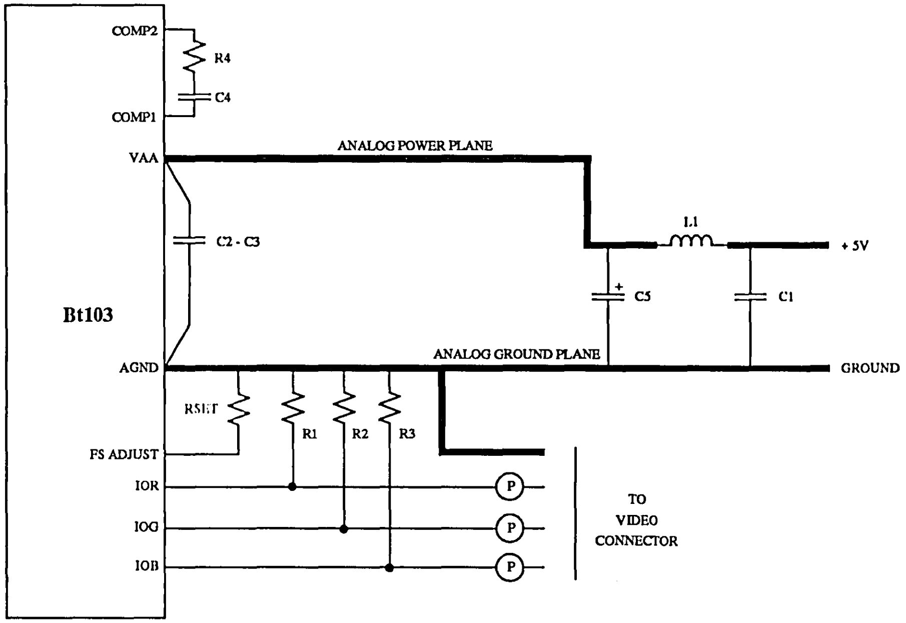
Analog Signal Interconnect

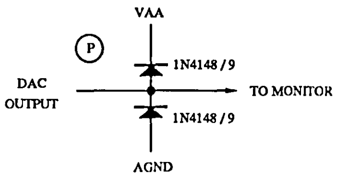
The Bt103 should be located as close as possible to the output connectors to minimize noise pickup, and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should each have a 75 Ω load resistor connected to AGND. The connection between the current output and AGND should be as close as possible to the Bt103 to minimize reflections.

PC Board Layout Considerations (continued)


COMP2
R4
C4
COMP1
VAA
ANALOG POWER PLANE
C2 - C3
L1
+5V
C5
C1
Bt103
ANALOG GROUND PLANE
AGND
GROUND
RSET
R1
R2
R3
FS ADJUST
IOR
IOG
IOB
P
P
P
TO
VIDEO
CONNECTOR


VAA
P
1N4148/9
DAC
OUTPUT
TO MONITOR
1N4148/9
AGND

Location	Description	Vendor Part Number
C1, C2, C3, C4	0.1 µF ceramic capacitor	Eric RPE112Z5U104M50V
C5	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	22 Ω 1% metal film resistor	Dale CMF-55C
RSET	499 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt103.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that a singly terminated 75 Ω load be used with an RSET value of about 713 Ω. If the Bt103 is not driving a large capacitive load, there will be negligible difference in video quality between doubly terminated 75 Ω and singly terminated 75 Ω loads.

If driving a large capacitive load (load RC > $1/(20\ f_C\pi)$)*, it is recommended that an output buffer be used to drive a doubly terminated 75 Ω load.

COMP Resistor

To optimize the settling time of the Bt103, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 22 Ω, however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time.

An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

Non-Video Applications

The Bt103 may be used in non-video applications by disabling the video-specific control inputs. SYNC* should be a logical zero and BLANK* should be a logical one. All three outputs will have the same full-scale output current.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

RSET (Ω) = 8,912 / Iout (mA)

With the data inputs at $00, there is a DC offset current (Imin) defined as follows:

Imin (mA) = 594 / RSET (Ω)

Therefore, the total full-scale output current will be Iout + Imin.

Analog Output Protection

The Bt103 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 3 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

---

*(f_C = clock frequency)

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA				
Bt103KC30		0		+70	°C
Bt103BC		–25		+85	°C
Output Load	RL		37.5		Ohms
FS ADJUST Resistor	RSET		499		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
Voltage on any Signal Pin*		AGND – 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		4	4	4	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1/8	LSB
Differential Linearity Error	DL			±1/16	LSB
Gray Scale Error				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	AGND – 0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH	–200		–1200	µA
Input Low Current (Vin = 0.4 V)	IIL	–200		–1200	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
Analog Outputs					
Gray Scale Current Range		15		20	mA
Output Current					
White Level Relative to Blank		16.88	19.05	20.69	mA
White Level Relative to Black		15.86	17.62	19.38	mA
Black Level Relative to Blank		1.02	1.19	1.31	mA
Blank Level on IOR, IOB		0	5	50	µA
Blank Level on IOG		6.29	7.62	8.96	mA
Sync Level on IOG		0	5	50	µA
LSB Size			1.175		mA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–1.0		+1.4	Volts
Output Impedance	ROUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		20		pF
Internal Voltage Reference	VREF		1.2		Volts
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 499 Ω. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	75 MHz Devices Min	75 MHz Devices Typ	75 MHz Devices Max	30 MHz Devices Min	30 MHz Devices Typ	30 MHz Devices Max	Units
Clock Rate	Fmax			75			30	MHz
Data and Control Setup Time	TSU	4			10			ns
Data and Control Hold Time	TH	1			2			ns
Clock Cycle Time	TCYC	13.3			33.3			ns
Clock Pulse Width High Time	TCLKH	5			10			ns
Clock Pulse Width Low Time	TCLKL	5			10			ns
Analog Output Delay	TDLY		12			12		ns
Analog Output Rise/Fall Time	TVRF			4			9	ns
Analog Output Settling Time*	TS		12			15		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			50			50		pV - sec
DAC-to-DAC Crosstalk			–25			–25		dB
Analog Output Skew			0	2		0	2	ns
Pipeline Delay		2	2	2	2	2	2	Clocks
VAA Supply Current**	IAA			175			110	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 499 Ω. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. COMP resistor = 22 Ω. Output load ≤ 10 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

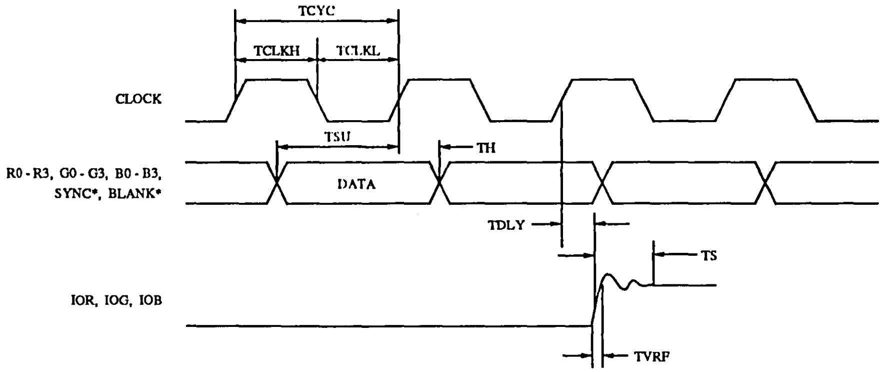
*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (max) at VAA = 5.25 V.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt103BC	75 MHz	28-pin 0.6" CERDIP	–25° to +85° C
Bt103KC30	30 MHz	28-pin 0.6" CERDIP	0° to +70° C
Bt103EVM	Evaluation Board for the Bt103		

Timing Waveforms


TCYC
TCLKH
TCLKL
CLOCK
TSU
TH
R0 - R3, G0 - G3, B0 - B3, SYNC*, BLANK*
DATA
TDLY
TS
IOR, IOG, IOB
TVRF

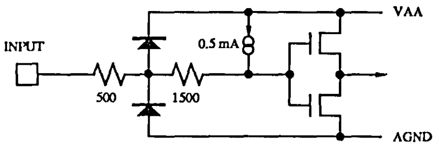
Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1/8 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

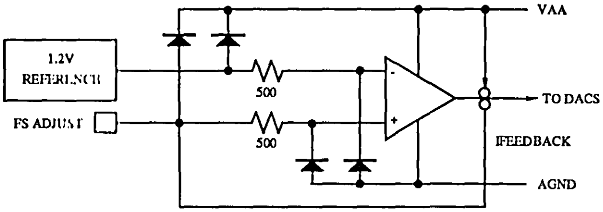
Figure 4. Input/Output Timing.

Device Circuit Data

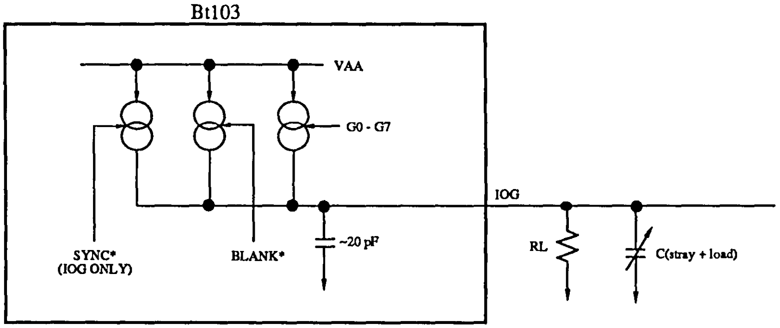

VAA
INPUT
0.5 mA
500
1500
AGND

High-speed operation is accomplished through pipelining and a unique (patent pending) TTL input buffer. This input buffer features a resistive level shifter that uses a temperature and process-compensated current source.

Equivalent Circuit of the Digital Inputs.


VAA
1.2V
REFERENCE
FS ADJUST
500
500
-
+
TO DACS
FEEDBACK
AGND

Equivalent Circuit of the Reference Amplifier.


Bt103
VAA
G0 - G7
IOG
SYNC*
(IOG ONLY)
BLANK*
~20 pF
RL
C(stray + load)

Equivalent Circuit of the Current Output (IOG).

Bt106

50 MHz
Monolithic CMOS
Single 8-bit
VIDEODAC™

Distinguishing Features

- 50, 30 MHz Operation
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- RS-343A/RS-170 Compatible Output
- TTL-Compatible Inputs
- +5 V CMOS Monolithic Construction
- 20-pin DIP Package
- Typical Power Dissipation: 400 mW

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction
- Instrumentation

Product Description

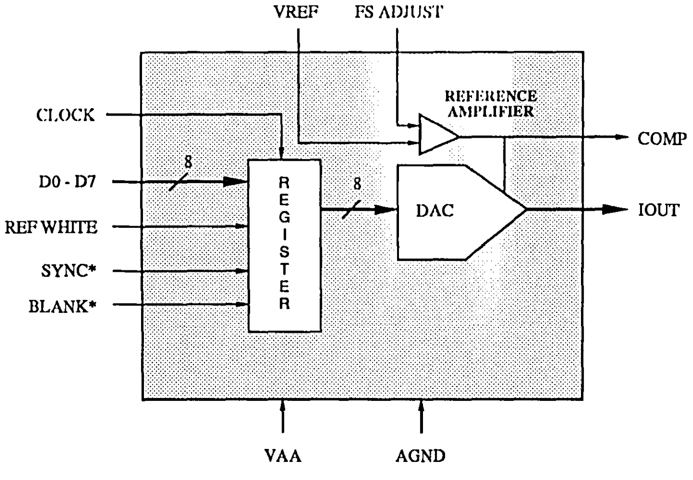
The Bt106 is an 8-bit VIDEODAC, designed specifically for high-performance, high-resolution color graphics.

Available control inputs include sync, blank, and reference white. The reference white input forces the analog output to the reference white level, regardless of the data inputs.

An external 1.2 V voltage reference and a single resistor control the full-scale output current. The sync, blank, and reference white inputs are pipelined to maintain synchronization with the digital input data.

The Bt106 generates RS-343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering. Both the differential and integral linearity errors of the D/A converter are guaranteed to be a maximum of ±1 LSB over the full temperature range.

Functional Block Diagram



Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L106001 Rev. G

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt106 contains an 8-bit D/A converter, input registers, and a reference amplifier.

On the rising edge of each clock cycle, as shown below in Figure 1, 8 bits of data are latched into the device and presented to the 8-bit D/A converter. The REF WHITE input, latched on the rising edge of CLOCK, forces the inputs of the D/A converter to $FF.

Latched on the rising edge of CLOCK to maintain synchronization with the data, the SYNC* and BLANK* inputs add appropriately weighted currents to the analog output, producing the specific output levels required for video applications, as illustrated in Figure 2. Table 1 details how the SYNC*, BLANK*, and REF WHITE inputs modify the output level.

Full-scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 542 Ω for generation of RS-343A video into a 37.5 Ω load. The VREF input requires an external 1.2 V (typical) reference. For maximum performance, the voltage reference should be temperature compensated and provide a low-impedance output.

The D/A converter on the Bt106 uses a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog output of the Bt106 is capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

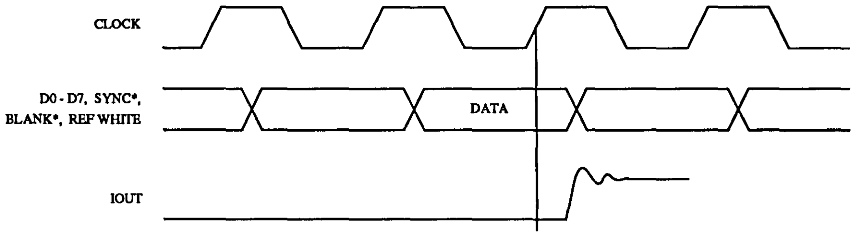
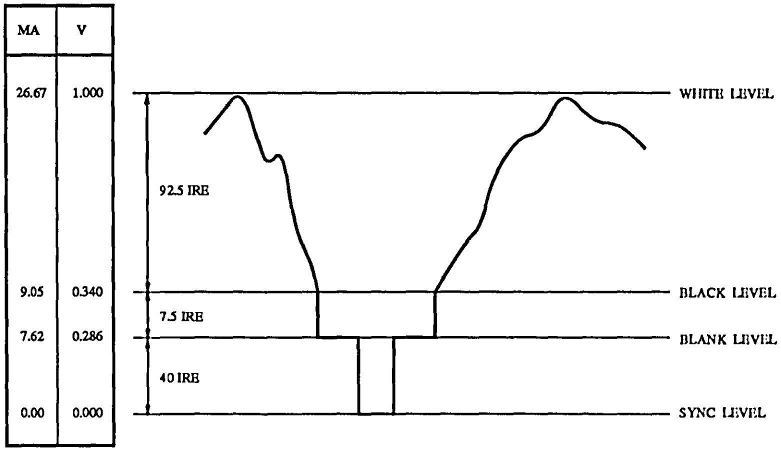


Figure 1. Input/Output Timing.

Circuit Description (continued)


MA
V
26.67
1.000
9.05
0.340
7.62
0.286
0.00
0.000
92.5 IRE
7.5 IRE
40 IRE
WHITE LEVEL
BLACK LEVEL
BLANK LEVEL
SYNC LEVEL

Note: 75 Ω doubly terminated load, RSET = 542 Ω, VREF = 1.2 V. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveform.

Description	IOUT (mA)	REF WHITE	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	1	$xx
WHITE	26.67	0	1	1	$FF
DATA	data + 9.05	0	1	1	data
DATA - SYNC	data + 1.44	0	0	1	data
BLACK	9.05	0	1	1	$00
BLACK - SYNC	1.44	0	0	1	$00
BLANK	7.62	x	1	0	$xx
SYNC	0	x	0	0	$xx

Note: Typical with full-scale IOUT = 26.67 mA. RSET = 542 Ω, VREF = 1.2 V.

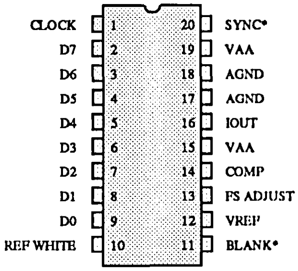
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the IOUT output to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the D0–D7 and REF WHITE inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the output (see Figure 2). SYNC* does not override any other control or data input, as shown in Table 1; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
REF WHITE	Reference white control input (TTL compatible). A logical one on this input forces the output to the white level, regardless of the D0–D7 inputs. It is latched on the rising edge of CLOCK. See Table 1.
D0–D7	Data inputs (TTL compatible). D0 is the least significant data bit. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the D0–D7, SYNC*, BLANK*, and REF WHITE inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
IOUT	Current output. This high-impedance current source is capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 3).
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full-scale video signal (Figure 2). Note that the IRE relationships in Figure 2 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current is: RSET (Ω) = 12,046 * VREF (V) / IOUT (mA)

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic capacitor in series with a resistor must be connected between this pin and the adjacent VAA pin (Figure 3). Connecting the capacitor to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF	Voltage reference input. An external voltage reference circuit, such as the one shown in Figure 3, must supply this input with a 1.2 V (typical) reference. The Bt106 has an internal pull-up resistor between VAA and VREF. As the value of this resistor may vary slightly due to process variations, the use of a resistor network to generate the reference is not recommended. A 0.1 µF ceramic capacitor must be used to decouple this input to VAA, as shown in Figure 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.


CLOCK 1
D7 2
D6 3
D5 4
D4 5
D3 6
D2 7
D1 8
D0 9
REF WHITE 10
20 SYNC*
19 VAA
18 AGND
17 AGND
16 IOUT
15 VAA
14 COMP
13 FS ADJUST
12 VREF
11 BLANK*

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt106 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and AGND pins should be as short as possible to minimize inductive ringing.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8-inch gap) connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk. The analog ground plane should include all Bt106 ground pins, all reference circuitry and decoupling, power supply bypass circuitry for the Bt106, analog output traces, and the video output connector.

Power Planes

The Bt106 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt106.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt106 power pins, voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged so that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

For the best performance, a 0.1 μF ceramic capacitor should be used to decouple each VAA pin to AGND. These capacitors should be placed as close as possible to the device.

It is important to note that while the Bt106 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three-terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt106 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Due to the high clock rates involved, long clock lines to the Bt106 should be avoided to reduce noise pickup.

Any termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

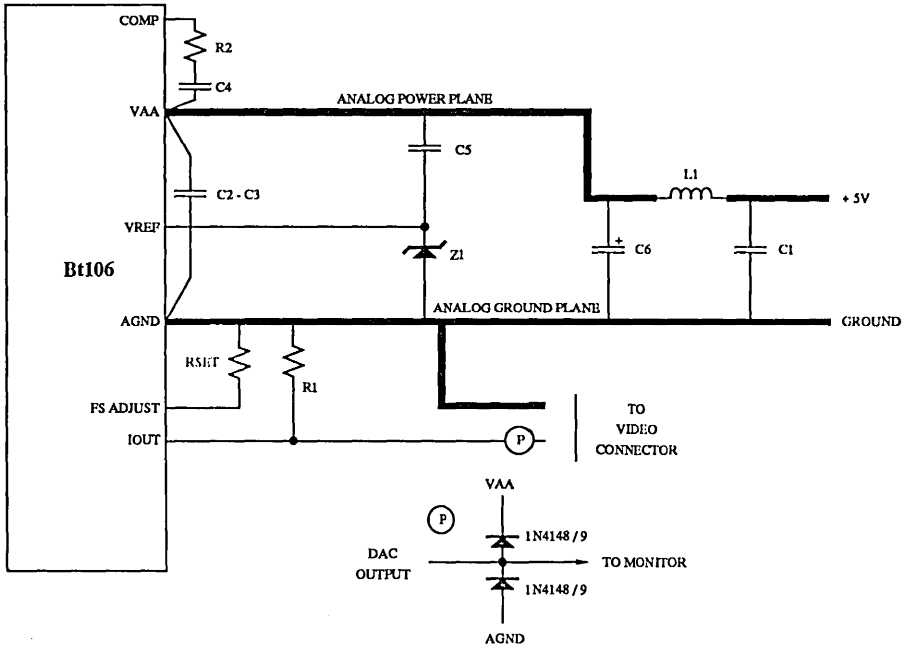
Analog Signal Interconnect

The Bt106 should be located as close as possible to the output connector to minimize noise pickup and reflections due to impedance mismatch.

The video output signal should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog output should have a 75 Ω load resistor connected to AGND. The connection between the current output and AGND should be as close as possible to the Bt106 to minimize reflections.

PC Board Layout Considerations (continued)


COMP
R2
C4
VAA
ANALOG POWER PLANE
C5
C2 - C3
L1
+ 5V
VREF
Z1
C6
C1
Bt106
ANALOG GROUND PLANE
AGND
GROUND
RSET
R1
FS ADJUST
IOUT
P
TO VIDEO CONNECTOR
VAA
P
1N4148 / 9
DAC OUTPUT
TO MONITOR
1N4148 / 9
AGND

Location	Description	Vendor Part Number
C1, C2, C3, C5	0.1 µF ceramic capacitor	Eric RPE112Z5U104M50V
C4	0.01 µF ceramic capacitor	Eric RPE110Z5U103M50V
C6	10 µF tantalum capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1	75 Ω 1% metal film resistor	Dale CMF-55C
R2	12 Ω 1% metal film resistor	Dale CMF-55C
RSET	542 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt106.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

RS-170 Video Generation

For generation of RS-170 compatible video, it is recommended that a singly terminated 75 Ω load be used with an RSET value of about 774 Ω. If the Bt106 is not driving a large capacitive load, there will be negligible difference in video quality between doubly terminated 75 Ω and singly terminated 75 Ω loads.

If driving a large capacitive load (load RC > 1/ ($20F_C$)),* it is recommended that an output buffer be used to drive a doubly terminated 75 Ω load.

Color Applications

Note that in color applications, sync information is typically required only on the green channel. Therefore, the SYNC* inputs to the red and blue VIDEODACs may be a logical zero. If SYNC* is always a logical zero, the relationship between RSET and the full scale output current is:

IOUT (mA) = 8,604 * VREF (V) / RSET (Ω)

Using Multiple Devices

If located close together on the same PC board, multiple Bt106 devices may be connected to a single analog power and ground plane. In addition, a single voltage reference may be used to drive multiple devices.

Each Bt106 must still have its individual RSET resistor, IOUT termination resistor (R1 in Figure 3), power supply bypass capacitors (C2 and C3 in Figure 3), and COMP resistor and capacitor (C4 and R2 in Figure 3).

At high clock rates, individual ground beads (L2 in Figure 3) may be required to maintain TTL thresholds due to high current return.

Non-Video Applications

The Bt106 may be used in non-video applications by disabling the video-specific control inputs. SYNC* and REF WHITE should be a logical zero and BLANK* should be a logical one.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

RSET (Ω) = 7,958 * VREF (V) / IOUT (mA)

With the data inputs at $00, there is a DC offset current (Imin) defined as follows:

Imin (mA) = 650 * VREF (V) / RSET (Ω)

Therefore, the total full-scale output current will be Iout + Imin. The REF WHITE input may optionally be used as a "force to full scale" control.

COMP Resistor

To optimize the settling time of the Bt106, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

The value of the resistor is typically 12 Ω; however, the exact value is dependent on the PC board layout, clock rate, etc., and should be optimized for minimal settling time.

An incorrect resistor value will result in degraded output performance, such as excessive ringing of the analog outputs or increased settling time.

Analog Output Protection

The Bt106 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 3 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low capacitance, fast switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

ESD and Latchup Considerations

Correct ESD sensitive handling procedures are required to prevent device damage which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

---

*(f_C = Clock Frequency)

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA				
Bt106KC30		0		+70	°C
Bt106BC		–25		+85	°C
Output Load	RL		37.5		Ohms
Reference Voltage	VREF	1.14	1.20	1.26	Volts
FS ADJUST Resistor	RSET		542		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
Voltage on Any Signal Pin*		AGND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	AGND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
Analog Output					
Gray Scale Current Range		15		20	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Blank Level		6.29	7.62	8.96	mA
Sync Level		0	5	50	µA
LSB Size			69.1		µA
Output Compliance	VOC	–1.0		+1.4	Volts
Output Impedance	ROUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		30		pF
Power Supply Rejection Ratio (COMP = 0.01 µF, f = 1 KHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 Ω, VREF = 1.200 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

		50 MHz Devices			30 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			50			30	MHz
Data and Control Setup Time	TSU	8			8			ns
Data and Control Hold Time	TH	2			2			ns
Clock Cycle Time	TCYC	20			33.3			ns
Clock Pulse Width High Time	TCLKH	8			10			ns
Clock Pulse Width Low Time	TCLKL	8			10			ns
Analog Output Delay	TDLY		25			25		ns
Analog Output Rise/Fall Time	TVRF			8			9	ns
Analog Output Settling Time*	TS		20			25		ns
Clock and Data Feedthrough*			-33			-33		dB
Glitch Impulse*			50			50		pV - sec
Differential Gain Error	DG		1.8			1.8		% Gray Scale
Differential Phase Error	DP		1.2			1.2		Degrees
Pipeline Delay		1	1	1	1	1	1	Clock
VAA Supply Current**	IAA		80	100		60	75	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 542 Ω, VREF = 1.200 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. COMP resistor = 12 Ω. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

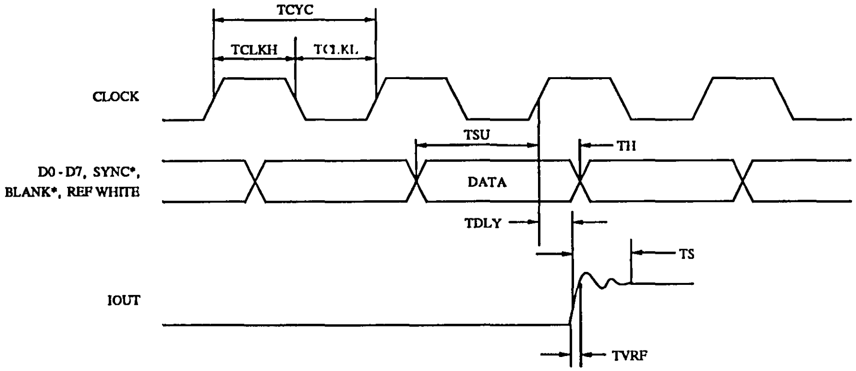
*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, -3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt106BC	50 MHz	20-pin 0.3" CERDIP	-25° to +85° C
Bt106KC30	30 MHz	20-pin 0.3" CERDIP	0° to +70° C
Bt106EVM	Evaluation Board for the Bt106		

Timing Waveforms


TCYC
TCLKH
TCLKL
CLOCK
TSU
TH
D0 - D7, SYNC*,
BLANK*, REF WHITE
DATA
TDLY
TS
IOUT
TVRF

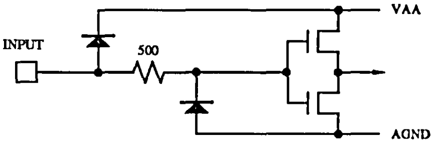
Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.

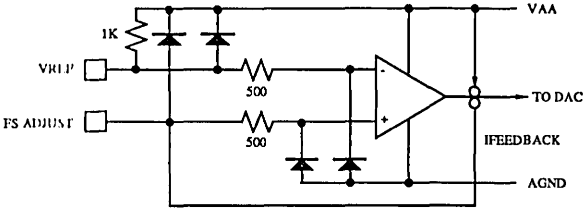
Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 4. Input/Output Timing.

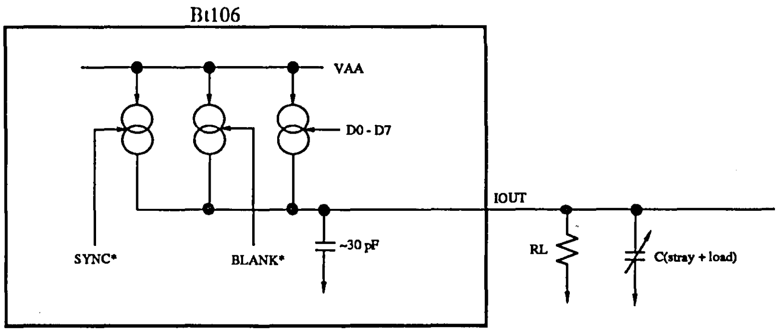
Device Circuit Data


VAA
INPUT
500
AGND

Equivalent Circuit of the Digital Inputs.


VAA
1K
VREF
500
FS ADJUST
500
TO DAC
IFEEDBACK
AGND

Equivalent Circuit of the Reference Amplifier.


Bt106
VAA
D0 - D7
IOUT
SYNC*
BLANK*
~30 pF
RL
C(stray + load)

Equivalent Circuit of the Current Output.

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt107

400 MHz
10KH/100K ECL
8-bit Multiplexed Input
VIDEODAC™

Distinguishing Features

- 400 MHz Pipelined Operation
- ±1/2 LSB Differential Linearity Error
- ±1/2 LSB Integral Linearity Error
- 500 ps Typical Rise/Fall Time
- RS-343A-Compatible Output
- 0 or 7.5 IRE Blanking Pedestal
- Handles 25-Ohm Output Loads
- 10KH and 100K ECL-Compatible I/O
- 2:1 Multiplexed Pixel Inputs
- 32-pin Flatpack Package
- Typical Power Dissipation: 1 W

Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM Applications
- Radar Processing
- Instrumentation

Related Products

- Bt424

Product Description

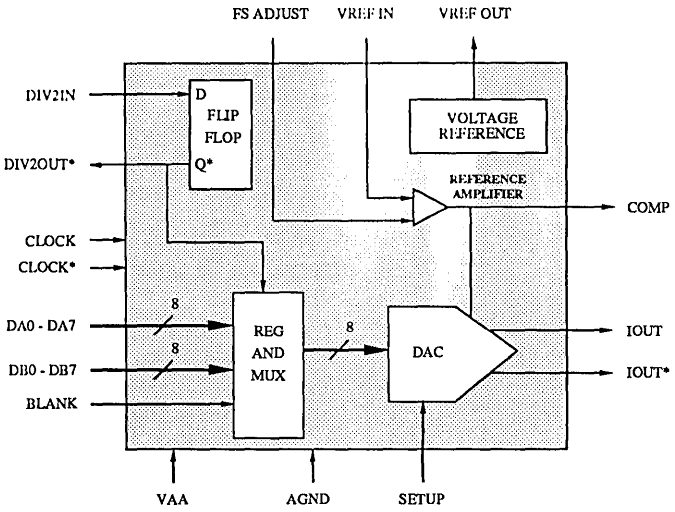
The Bt107 is an 8-bit VIDEODAC, designed specifically for high-performance, high-resolution color graphics.

Multiplexed pixel inputs enable pixel data to be latched into the Bt107 at a 200 MHz data rate, while maintaining the 400 MHz output rate necessary for high-resolution graphics. On-chip circuitry divides the pixel clock by two, generating the 200 MHz clock signal.

An on-chip voltage reference is available or an external reference may be used. A single external resistor controls the full-scale output current.

The Bt107 generates an RS-343A compatible video signal, and is capable of driving either doubly terminated 75 Ω or 50 Ω coax directly, without requiring external buffering. Both the differential and integral linearity errors of the D/A converter are guaranteed to be a maximum of ±1/2 LSB over the full temperature range.

Functional Block Diagram



Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249

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Circuit Description

As illustrated in the functional block diagram, the Bt107 contains a single 8-bit D/A converter, 2:1 multiplexed input register, a voltage reference, and a reference amplifier.

Pixel data on the DA0–DA7 (even data) and DB0- DB7 (odd data) are latched on the falling edge of DIV2OUT*, as illustrated in Figure 1.

DIV2IN is defined to be 1/2 the CLOCK rate. To simplify system design, the Bt107 outputs a DIV2OUT* signal which, when connected to the DIV2IN pin, generates a clock equal to 1/2 the CLOCK rate. For a color system requiring three Bt107s, the DIV2OUT* signals may be synchronized by connecting the DIV2OUT* signal on one of the devices to the DIV2IN pins of all three devices. Care should be taken to keep signal paths short and equal for each connection. The unused DIV2OUT* signals from the remaining Bt107s can be used to clock external lookup table RAMs.

The BLANK input is also latched on the falling edge of DIV2OUT*, and overrides the DA0–DA7 and DB0–DB7 data. Blanking information is output synchronously with the even pixel data.

Full scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 1092 Ω for generation of RS-343A video into a 37.5 Ω load, or 729 Ω for generation of RS-343A video into a 25 Ω load. The on-chip voltage reference (VREF OUT) may be used to provide the reference for the VREF IN pins of up to three Bt107s, or an external reference may be used.

Both sides of the differential current outputs should have the same output load. A single-ended video signal may be generated by connecting the IOUT output through a 25 Ω resistor to AGND (assuming a doubly terminated 50 Ω load). The IOUT* output is used to generate the video signal.

The D/A converter on the Bt107 uses a segmented architecture in which bit currents are routed to either IOUT or IOUT* by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt107 are capable of directly driving either a 37.5 Ω or 25 Ω load, such as a doubly terminated 75 Ω or 50 Ω coaxial cable.

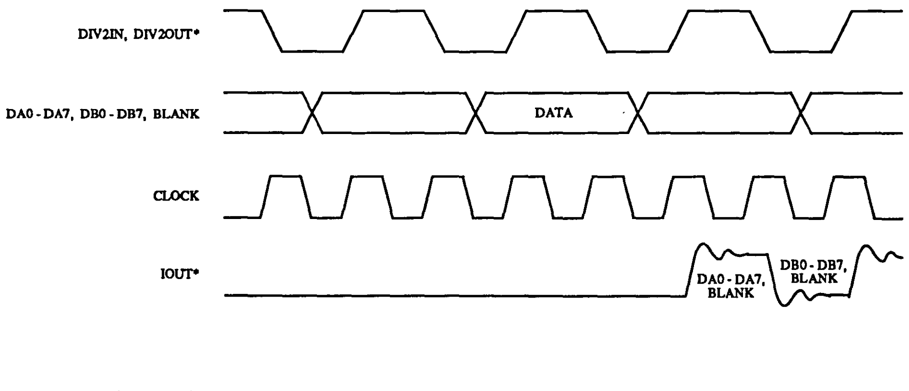
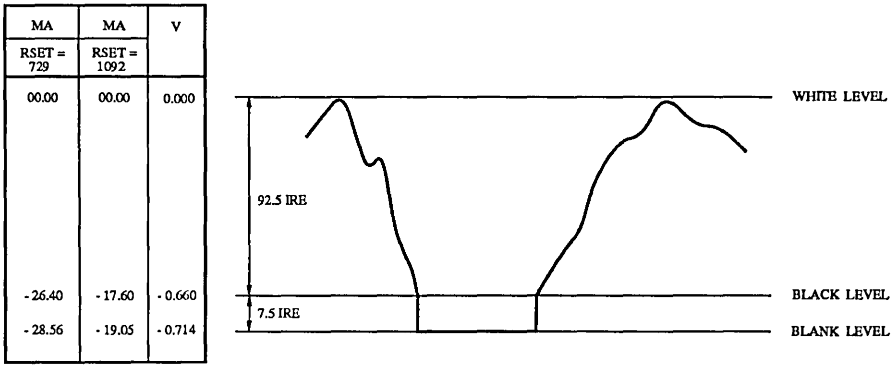


Figure 1. Input/Output Timing (DIV2IN connected to DIV2OUT).*

Circuit Description (continued)


MA
MA
V
RSET = 729
RSET = 1092
00.00
00.00
0.000
- 26.40
- 17.60
- 0.660
- 28.56
- 19.05
- 0.714
92.5 IRE
7.5 IRE
WHITE LEVEL
BLACK LEVEL
BLANK LEVEL

Note: RSET = 729 Ω (50 Ω doubly terminated load) or 1092 Ω (75 Ω doubly terminated load), VREF IN = –1.21 V. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveform (IOUT).*

	RSET = 729 Ω	RSET = 1092 Ω		
Description	IOUT* (mA)	IOUT* (mA)	BLANK	DAC Input Data
WHITE	0	0	0	$FF
DATA	data	data	0	data
BLACK	–26.40	–17.62	0	$00
BLANK			1	$xx
SETUP = AGND	–26.40	–17.62		
SETUP = float	–28.56	–19.05		

Note: Typical with VREF IN = –1.21 V.

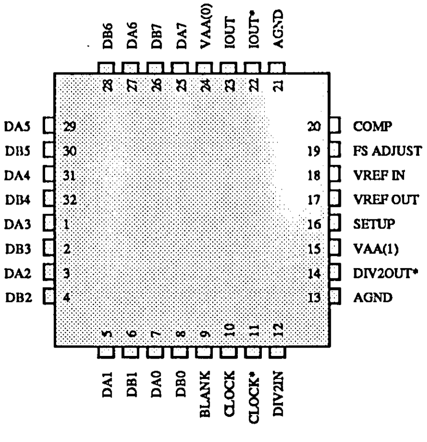
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK	Composite blank control input (ECL compatible). A logic one drives the analog output to the blanking level, as illustrated in Table 1. It is latched on the falling edge of DIV2OUT*. When BLANK is a logical one, the DA0–DA7 and DB0–DB7 inputs are ignored. Blanking information is output synchronously with the even pixel data.
DA0–DA7, DB0–DB7	Even and odd pixel data inputs (ECL compatible). D0 is the least significant data bit. They are latched on the falling edge of DIV2OUT*. Even data represents the first (leftmost) pixel on the display screen. DAx represent the even pixel data, and DBx represent the odd pixel data. Coding is binary.
CLOCK, CLOCK*	Differential clock inputs (ECL compatible). It is typically the pixel clock rate of the video system. The Bt107 may be operated with a single-ended clock by connecting CLOCK* to a –1.3 V VBB; however, common mode noise immunity at high clock rates may degrade.
DIV2IN	CLOCK/2 input (ECL compatible). This clock must be 1/2 the CLOCK rate. It is used to latch the BLANK, DAx, and DBx inputs. See Figure 1.
DIV2OUT*	CLOCK/2 output (ECL compatible). When connected to the DIV2IN pin, this output is 1/2 the CLOCK rate. When not connected to DIV2IN, it generates a signal that is DIV2IN synchronized to CLOCK and inverted. DIV2OUT* must be terminated to –2 V.
IOUT, IOUT*	Differential video current outputs. These high impedance current sources are capable of directly driving either a doubly terminated 50 Ω or 75 Ω coaxial cable (Figure 3). Both outputs, whether used or not, should have the same output load.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected. **Warning: It is important that a ferrite bead be used to connect the VAA(1) power pin to the analog power plane as illustrated in Figure 3. Connecting the decoupling capacitors directly to the VAA(1) pin will result in unstable operation.**
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic chip capacitor and a 0.001 ceramic chip capacitor must be connected between this pin and VAA(0) (Figure 3). Connecting the capacitors to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP capacitors must be as close to the device as possible to keep lead lengths to an absolute minimum.
SETUP	Pedestal control input. If connected to AGND, the blanking pedestal on the output is disabled, making the black and blanking levels the same (0 IRE). If left floating, the 7.5 IRE blanking pedestal is enabled. See Figure 2.

Pin Descriptions (continued)

Pin Name	Description
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full-scale video signal (Figure 3). Note that the IRE relationships in Figure 2 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current is: $\text{RSET}\ (\Omega) = K * \text{VREF IN}\ (V) / \text{IOUT}\ (mA)$ where K = 17,205 if SETUP = float or 15,915 if SETUP = AGND. Note: The RSET value may need to be adjusted to generate the specified video levels due to variations in processing and depending on whether the internal or an external reference is used.
VREF OUT	Voltage reference output. This output provides a –1.2 V (typical) reference, and may be connected to the VREF IN inputs of up to three Bt107s. When driving multiple Bt107s, use 100 Ω interconnect resistance to minimize noise pick-up. If it is not used to provide a voltage reference, it should remain floating.
VREF IN	Voltage reference input. An external voltage reference, such as the one shown in Figure 4, or the VREF OUT pin must supply this input with a –1.2 V (typical) reference. A 0.01 µF ceramic chip capacitor in parallel with a 0.001 µF ceramic chip capacitor must be connected between this pin and VAA(0), as shown in Figure 3. The decoupling capacitors must be as close to the device as possible to keep lead lengths to an absolute minimum.


DB6 28
DA6 27
DB7 26
DA7 25
VAA(0) 24
IOUT 23
IOUT* 22
AGND 21
DA5 29
DB5 30
DA4 31
DB4 32
DA3 1
DB3 2
DA2 3
DB2 4
20 COMP
19 FS ADJUST
18 VREF IN
17 VREF OUT
16 SETUP
15 VAA(1)
14 DIV2OUT*
13 AGND
5 DA1
6 DB1
7 DA0
8 DB0
9 BLANK
10 CLOCK
11 CLOCK*
12 DIV2IN

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt107 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and AGND pins should be as short as possible to minimize inductive ringing.

Ground Planes

The Bt107 and any associated analog circuitry should have its own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt107.

The analog ground plane area should encompass all Bt107 ground pins, power supply bypass circuitry for the Bt107, any external voltage reference circuitry, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the Bt107.

Power Planes

The Bt107 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt107.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt107 power pins, any external voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged so that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

In addition to the ferrite beads between the analog and regular PCB power and ground planes, an additional ferrite bead must be installed between the VAA(1) power pin and the analog power plane, as illustrated in Figure 3. The ferrite bead must be located as close as possible to the VAA(1) pin.

For the best performance, three chip capacitors in parallel (0.1 µF, 0.01 µF, and 0.001 µF) should be placed as close as possible to each power pin for power supply bypassing. These capacitors should be connected on the analog power plane side of the ferrite bead for the VAA(1) pin as illustrated in Figure 3. Connecting the bypass capacitors directly to the VAA(1) pin will result in unstable operation due to high-frequency oscillations.

Digital Signal Interconnect

The digital inputs to the Bt107 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Stripline or microstrip techniques should be used for the ECL interfacing. In addition, all ECL inputs should be terminated as closely as possible to the device to reduce ringing, crosstalk, and reflections.

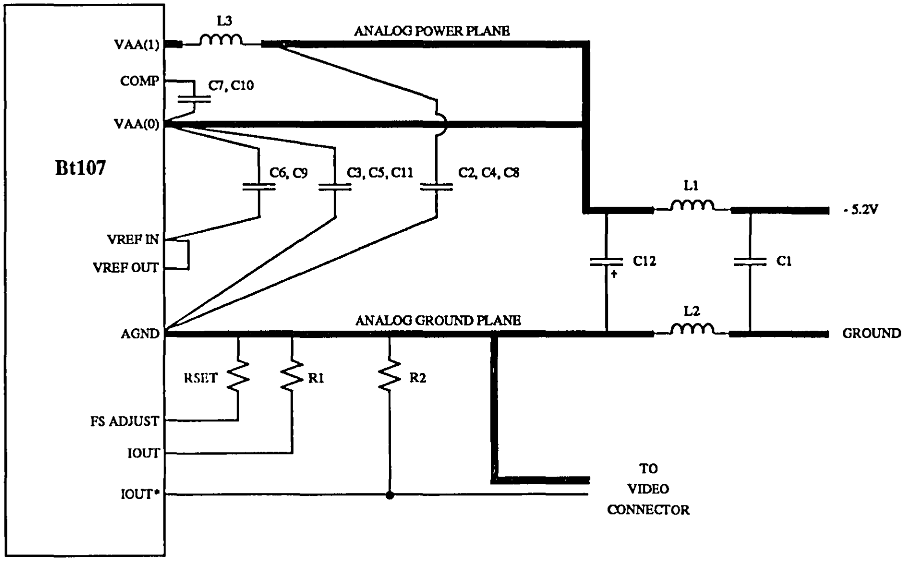
Any termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

It is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed circuitry wiring and coaxial cable.

PC Board Layout Considerations (continued)


L3
VAA(1)
ANALOG POWER PLANE
COMP
C7, C10
VAA(0)
Bt107
C6, C9
C3, C5, C11
C2, C4, C8
L1
- 5.2V
VREF IN
VREF OUT
C12
+
C1
L2
AGND
ANALOG GROUND PLANE
GROUND
RSET
R1
R2
FS ADJUST
IOUT
IOUT*
TO
VIDEO
CONNECTOR

Location	Description	Vendor Part Number
C1	0.1 µF ceramic capacitor	Mallory CK05BX104K
C2, C3	0.1 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W104KP
C4–C7	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W103KP
C8–C11	0.001 µF ceramic chip capacitor	Johanson Dielectrics NPO-500S41N102JP
C12	10 µF tantalum capacitor	Mallory CSR13G106KM
L1, L2, L3	ferrite bead	Fair-Rite 2743001111
R1	24.9 Ω 1% metal film resistor	Dale CMF-55C
R2	49.9 Ω 1% metal film resistor	Dale CMF-55C
RSET	732 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt107. R1, R2, and RSET values assume doubly terminated 50 Ω load on IOUT*.

Figure 3. Typical Connection Diagram and Parts List (Internal Reference).

Application Information

Terminated Inputs

All digital inputs of the Bt107 should be terminated using normal ECL termination practices. In addition, all of the digital inputs have internal pull-down junctions. Thus, if a digital input is left floating, it assumes the logical zero state.

External Voltage Reference

An external voltage reference may be used with the Bt107, as shown in Figure 4. In this instance, the VREF OUT pin should be left floating.

Note that the VREF IN pin still requires bypass capacitors to VAA(0) (C6 and C9 in Figure 3).

Package Heatsink

The stud heatsink is electrically isolated and should be connected to AGND for minimal noise.

Using Multiple Bt107s

For color applications, three Bt107s may be used, as illustrated in Figure 5. This example generates 256 simultaneous colors from a 16.8 million color palette and supports a 2k x 2k pixel resolution.

Both the even and odd pixel data require separate shift registers and color palette RAM (Bt404s are used in this illustration). The Bt502s interface the color palette RAM to the TTL-compatible MPU bus. If more than 256 colors are desired, additional Bt404s may be wired in parallel to expand each color palette RAM to 1024 x 8.

Note the DIV2OUT*-DIV2IN connections, generating CLOCK*/2 and ensuring the three Bt107s operate in a synchronous fashion. When analyzing the timing window for DIV2IN, be sure to include the propagation delay of the CLOCK and DIV2OUT* signals through the transmission lines of the physical layout on the PC board.

When DIV2OUT is to be used for system CLOCK, it is recommended that DIV2OUT* be buffered before distribution to the rest of the system to allow for adequate noise margins.

The Bt107s may share the voltage reference and analog power/ground planes, but each Bt107 must have its own power supply decoupling, COMP decoupling, VREF IN decoupling, VAA(1) ferrite bead, RSET resistor, and IOUT termination resistors.

Optimum layout should minimize CLOCK and DIV2* line length. Low E stripline is recommended, and the propagation delays between CLOCK and DIV2* should match as closely as possible.

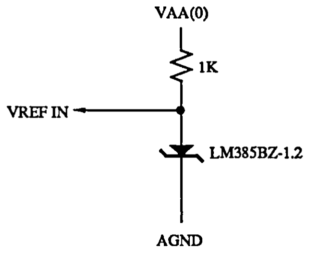


Figure 4. External Voltage Reference.

Application Information (continued)

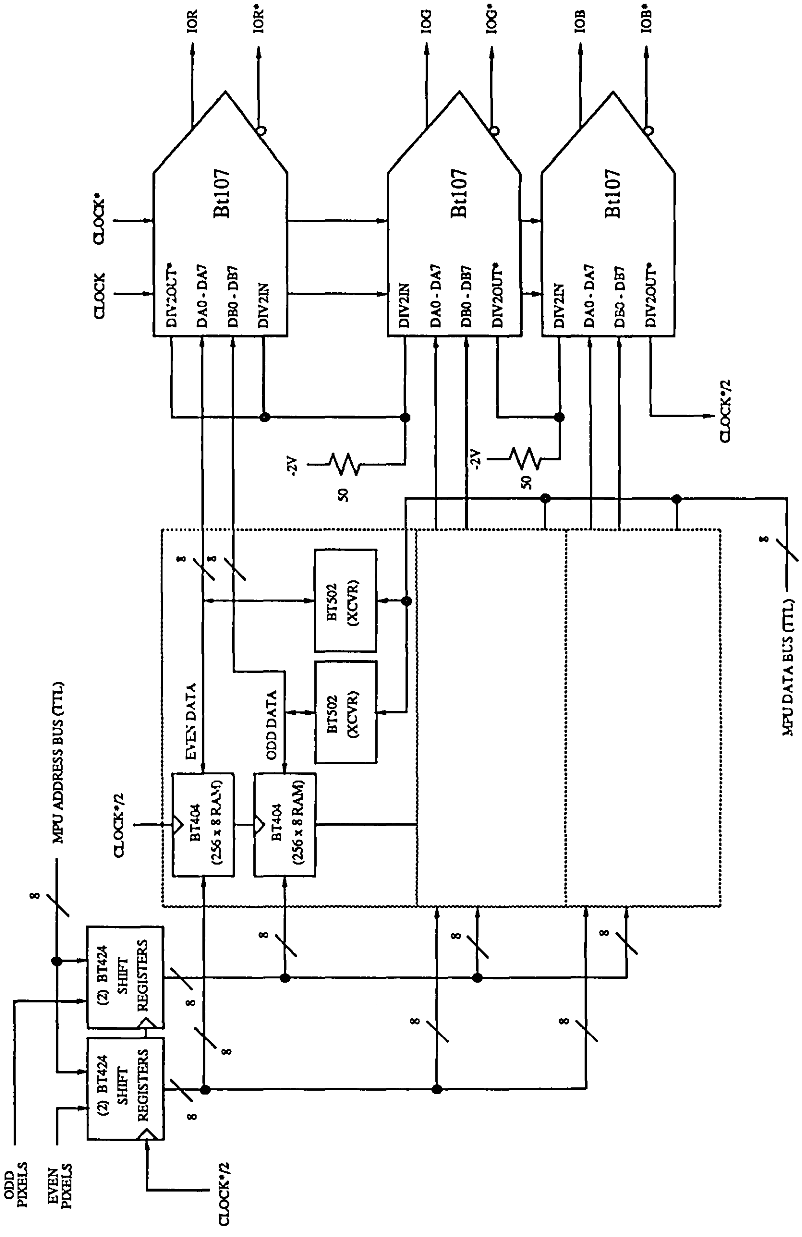

ODD PIXELS
EVEN PIXELS
CLOCK*/2
(2) BT424 SHIFT REGISTERS
(2) BT424 SHIFT REGISTERS
8
MPU ADDRESS BUS (TTL)
CLOCK*/2
BT404 (256 x 8 RAM)
BT404 (256 x 8 RAM)
EVEN DATA
ODD DATA
BT502 (XCVR)
BT502 (XCVR)
MPU DATA BUS (TTL)
CLOCK
CLOCK*
DIV2OUT*
DA0 - DA7
DB0 - DB7
DIV2IN
Bt107
IOR
IOR*
IOG
IOG*
IOB
IOB*
-2V
50
CLOCK*/2

Figure 5. Using Multiple Bt107s.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	-4.2	-5.2	-5.5	Volts
Ambient Operating Temperature	TA	-25		+85	°C
Output Load	RL		25		Ohms
Reference Voltage	VREF IN	-1.13	-1.2	-1.3	Volts
FS ADJUST Resistor	RSET		729		Ohms

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)	VAA			-6.5	Volts
Voltage on Any Digital Pin		AGND + 0.5		VAA -0.5	Volts
Analog Output Short Circuit Duration to Any Common			indefinite		
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+175	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution		8	8	8	Bits
Accuracy					
Integral Linearity Error	IL			±1/2	LSB
Differential Linearity Error	DL			±1/2	LSB
Gray Scale Error					
Using Internal Reference				±10	% Gray Scale
Using External Reference				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	-1160		-710	mV
Input Low Voltage	VIL	-1870		-1480	mV
Input High Current (Vin = VIHmax)	IIH				
Data				30	µA
All Other Inputs				150	µA
Input Low Current (Vin = VILmin)	IIL				
Blank				150	µA
All Other Inputs				5	µA
Input Capacitance (f = 1 MHz, Vin = VIHmax)	CIN			10	pF
Digital Output					
Output High Voltage	VOH	-1060	-955	-880	mV
Output Low Voltage	VOL	-1810	-1705	-1620	mV
Analog Output					
Gray Scale Current Range				-40	mA
Output Current					
White Level		0	-5	-50	µA
Black Level Relative to White		-25.08	-26.40	-27.72	mA
Blank Level Relative to Black					
SETUP = AGND		0	0	0	mA
SETUP = float		-2.05	-2.16	-2.28	mA
LSB Size			-103.5		µA
Output Compliance	VOC	-1.2		+1.5	Volts
Output Impedance	ROUT		10		K ohms
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		9		pF
Reference Input Current	IREF IN			10	µA
Reference Output Voltage	VREF OUT	-1.14	-1.22	-1.3	Volts
Reference Output Current	IREF OUT	-200			µA
Power Supply Rejection Ratio (COMP = 0.001 µF ‖ 0.01 µF, f = 1 kHz)	PSRR		0.03	0.5	%/%ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for –28.56 mA full-scale output current, VREF IN = –1.21 V, SETUP = float. All digital inputs have 50 Ω to –2.0 V. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			400	MHz
Data and Control Setup Time	TSU	1			ns
Data and Control Hold Time	TH	0			ns
Clock Cycle Time	TCYC	2.5			ns
Clock Pulse Width High	TCLKH	1			ns
Clock Pulse Width Low	TCLKL	1			ns
DIV2OUT Delay***	DDLY	1.5		2.2	ns
DIV2IN Setup Time	DSU	0			ns
DIV2IN Hold Time	DH	1			ns
Analog Output Delay	TDLY			2	ns
Analog Output Rise/Fall Time	TVRF		350	700	ps
Analog Output Settling Time	TS			2	ns
Clock and Data Feedthrough*			tbd		dB
Glitch Impulse*			10		LSB - ns
Non-Harmonic Spurious			–45		dBc
Pipeline Delay		2	2	2	Clocks
VAA Supply Current**	IAA			225	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for –28.56 mA full scale output current, VREF IN = –.21 V SETUP = float. ECL input values are –0.95 to –1.69 V, with input rise/fall times ≤ 1 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. All digital inputs have 50 Ω to –2.0 V, unless otherwise specified. Analog output load ≤ 10 pF. See timing notes in Figure 6. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 800 MHz.

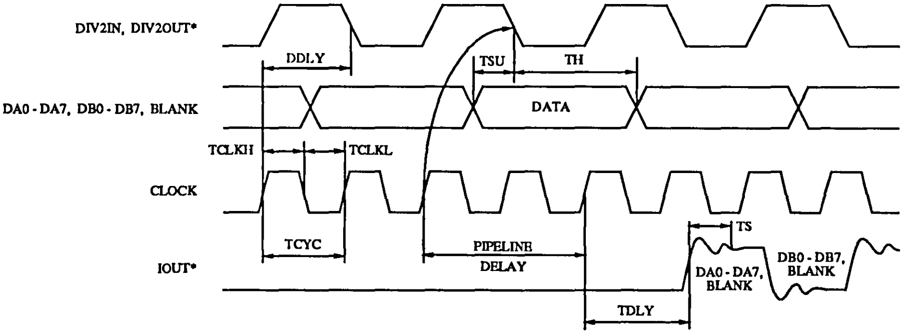
**At Fmax. IAA (typ) at VAA = –4.5 V. IAA (max) at VAA = –5.5 V.

***Tested with one ECL load.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt107BF400	400 MHz	32-pin Ceramic Flatpack w/heatsink	–25° to +85° C

Timing Waveforms


DIV2IN, DIV2OUT*
DDLY
TSU
TH
DA0 - DA7, DB0 - DB7, BLANK
DATA
TCLKH
TCLKL
CLOCK
TCYC
PIPELINE DELAY
TS
IOUT*
DA0 - DA7, BLANK
DB0 - DB7, BLANK
TDLY

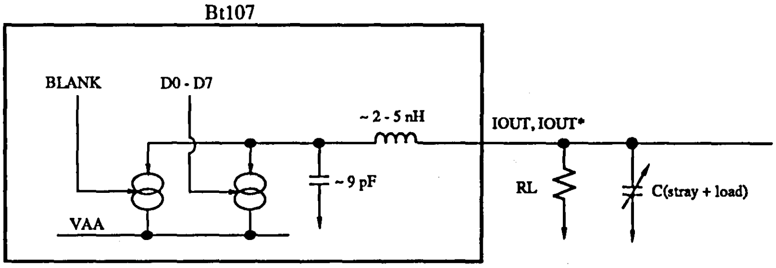
Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1/2 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

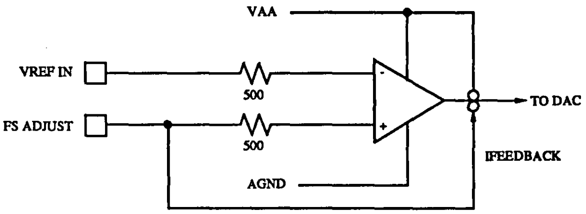
Figure 6. Input/Output Timing (DIV2IN connected to DIV2OUT).*

Device Circuit Data


Bt107
BLANK
D0 - D7
~ 2 - 5 nH
~ 9 pF
VAA
IOUT, IOUT*
RL
C(stray + load)

The output network of the Bt107 may be modeled as a three-pole low-pass filter. Settling time is tested on a sample basis with C(stray + load) tuned for optimum performance.

Equivalent Output Circuit of the Bt107.


VAA
VREF IN
FS ADJUST
500
500
-
+
TO DAC
IFEEDBACK
AGND

Equivalent Circuit of the Reference Amplifier.

Bt109

Distinguishing Features

- 250 MHz Pipelined Operation
- Triple 8-bit D/A Converters
- ±1/2 LSB Differential Linearity Error
- ±1/2 LSB Integral Linearity Error
- 350 ps Typical Rise/Fall Time
- RS-343A-Compatible Outputs
- 10KH ECL-Compatible Inputs
- 40-pin DIP Package
- Pin Compatible with TDC1318
- Typical Power Dissipation: 2 W

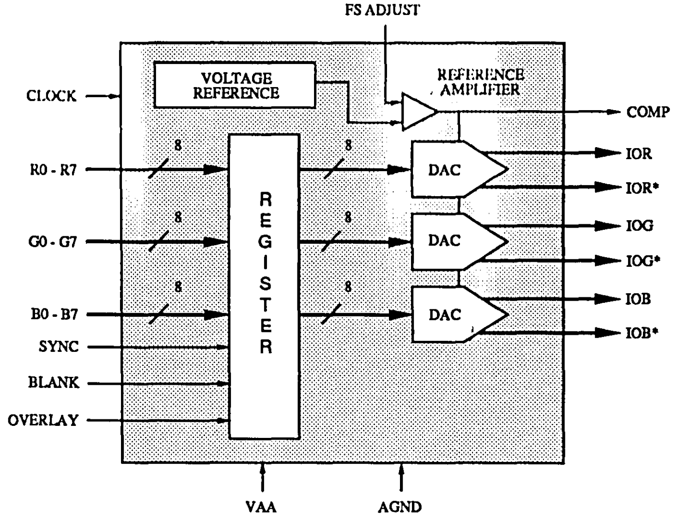
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction
- Instrumentation

Related Products

- Bt424

Functional Block Diagram



250 MHz
10KH ECL
Triple 8-bit
VIDEODAC™

Product Description

The Bt109 is a triple 8-bit VIDEODAC, designed specifically for high-performance, high-resolution color graphics.

Available control inputs include sync, blank, and overlay, all registered to maintain synchronization with the pixel data.

An internal 1.2 V voltage reference and a single external resistor control the full-scale output current.

The Bt109 generates RS-343A compatible red, green, and blue video signals, and is capable of driving doubly terminated 75 Ω coax directly, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1/2 LSB over the full temperature range.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L109001 Rev. G

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt109 contains three 8-bit D/A converters, input registers, a voltage reference, and a reference amplifier.

On the rising edge of each clock cycle, as shown below in Figure 1, 24 bits of color information (R0–R7, G0–G7, and B0–B7) are latched into the device and presented to the three 8-bit D/A converters.

The OVERLAY input, also latched on the rising edge of CLOCK, forces the analog outputs to the overlay level, regardless of the data inputs. This also permits blanking of the IOUT* outputs for analog summing.

Latched on the rising edge of CLOCK to maintain synchronization with the color data, the SYNC and BLANK inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications, as illustrated in Figure 2. Table 1 details how the SYNC, BLANK, and OVERLAY inputs modify the output levels.

The full-scale output current is set by an external resistor (RSET) between the FS ADJUST pin and AGND. RSET has a typical value of 1100 Ω for generation of RS-343A video into a 37.5 Ω load.

Both sides of the differential current outputs should have the same output load. A single-ended video signal may be generated by connecting the IOR, IOG, and IOB outputs through 37.5 Ω resistors to AGND (assuming IOR*, IOG*, and IOB* are driving a doubly terminated 75 Ω load). The IOR*, IOG*, and IOB* outputs are then used to generate the video signals.

The D/A converters on the Bt109 use a segmented architecture in which bit currents are routed to either IOUT or IOUT* by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt109 are capable of directly driving a doubly terminated 75 Ω coaxial cable or a singly terminated 50 Ω coaxial cable.

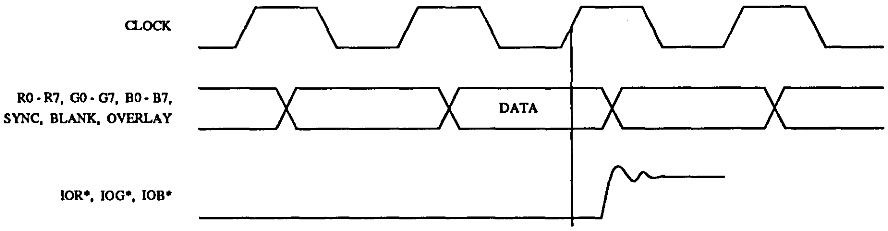
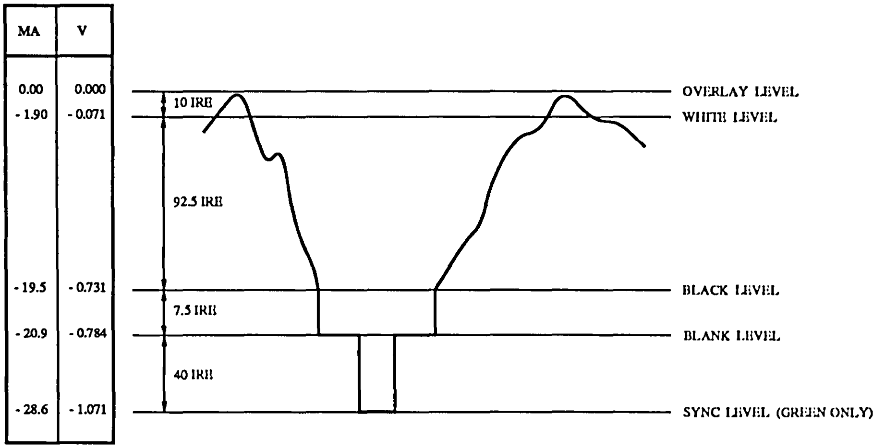


Figure 1. Input/Output Timing.

Circuit Description (continued)


MA
V
0.00
0.000
- 1.90
- 0.071
- 19.5
- 0.731
- 20.9
- 0.784
- 28.6
- 1.071
10 IRE
92.5 IRE
7.5 IRE
40 IRE
OVERLAY LEVEL
WHITE LEVEL
BLACK LEVEL
BLANK LEVEL
SYNC LEVEL (GREEN ONLY)

Note: 75 Ω doubly terminated load, RSET = 1100 Ω. RS-343A levels and tolerances assumed on all levels.

Figure 2. Composite Video Output Waveforms.

Description	IOG* (mA)	IOR*, IOB* (mA)	OVERLAY	SYNC	BLANK	DAC Input Data
OVERLAY	0	0	1	0	0	$xx
WHITE	–1.90	–1.90	0	0	0	$FF
DATA	data–1.90	data–1.90	0	0	0	data
BLACK	–19.50	–19.50	0	0	0	$00
BLANK	–20.90	–20.90	x	0	1	$xx
SYNC	–28.60	–20.90	x	1	1	$xx

Note: Typical with full-scale IOG* = –8.60 mA. RSET = 1100 Ω. Note that SYNC does not override data, as with the TDC1318.

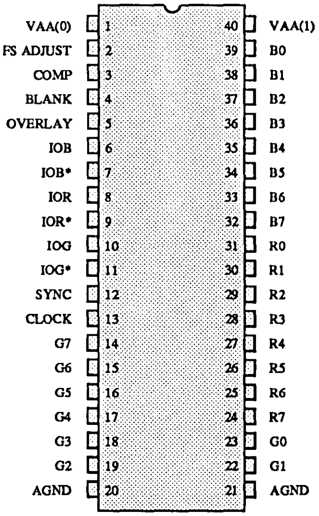
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK	Composite blank control input (ECL compatible). A logical one on this input drives the analog outputs to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When BLANK is a logical one, the data and OVERLAY inputs are ignored.
SYNC	Composite sync control input (ECL compatible). A logical one on this input switches on a 40 IRE current source on the green output (see Figure 2). SYNC does not override any other control or data input, as shown in Table 1; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
OVERLAY	Overlay control input (ECL compatible). A logical one on this input overrides the data inputs and forces the analog outputs to the overlay level. It is latched on the rising edge of CLOCK.
R0–R7, G0–G7, B0–B7	Red, green, and blue data inputs (ECL compatible). R0, G0, and B0 are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (ECL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, SYNC, BLANK, and OVERLAY inputs. It is typically the pixel clock rate of the video system.
IOR, IOG, IOB, IOR*, IOG*, IOB*	Red, green, and blue differential video current outputs. These high-impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figure 3). All outputs, whether used or not, should have the same output load.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected. **Warning: It is important that a ferrite bead be used to connect the VAA(1) power pin to the analog power plane as illustrated in Figure 3. Connecting the decoupling capacitors directly to the VAA(1) pin will result in unstable operation.**
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic chip capacitor and a 0.001 ceramic chip capacitor must be connected between this pin and VAA(0) (Figure 3). Connecting the capacitors to VAA rather than to AGND provides the highest possible power supply noise rejection. The COMP capacitors must be as close to the device as possible to keep lead lengths to an absolute minimum.

Pin Descriptions (continued)

Pin Name	Description
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and AGND controls the magnitude of the full-scale video signal (Figure 3). Note that the IRE relationships in Figure 2 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOG* is: $\text{RSET} (\Omega) = 31{,}460 / \text{IOG (mA)}$ The full-scale output current on IOR* and IOB* for a given RSET is defined as: $\text{IOR, IOB (mA)} = 22{,}990 / \text{RSET} (\Omega)$ Note: The RSET value may need to be adjusted to generate the specified video levels due to variations in processing.


VAA(0) 1
FS ADJUST 2
COMP 3
BLANK 4
OVERLAY 5
IOB 6
IOB* 7
IOR 8
IOR* 9
IOG 10
IOG* 11
SYNC 12
CLOCK 13
G7 14
G6 15
G5 16
G4 17
G3 18
G2 19
AGND 20
40 VAA(1)
39 B0
38 B1
37 B2
36 B3
35 B4
34 B5
33 B6
32 B7
31 R0
30 R1
29 R2
28 R3
27 R4
26 R5
25 R6
24 R7
23 G0
22 G1
21 AGND

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt109 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and AGND pins should be as short as possible to minimize inductive ringing.

Ground Planes

The Bt109 and any associated analog circuitry should have its own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt109.

The analog ground plane area should encompass all Bt109 ground pins, power supply bypass circuitry for the Bt109, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the Bt109.

Power Planes

The Bt109 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 3. This bead should be located within 3 inches of the Bt109.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt109 power pins and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged so that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

In addition to the ferrite beads between the analog and regular PCB power and ground planes, an additional ferrite bead must be installed between the VAA(1) power pin and the analog power plane, as illustrated in Figure 3. The ferrite bead must be located as close as possible to the VAA(1) pin.

For the best performance, three chip capacitors in parallel (0.1 µF, 0.01 µF, and 0.001 µF) should be placed as close as possible to each power pin for power supply bypassing. These capacitors should be connected on the analog power plane side of the ferrite bead for the VAA(1) pin as illustrated in Figure 3. Connecting the bypass capacitors directly to the VAA(1) pin will result in unstable operation due to high-frequency oscillations.

If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three-terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt109 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

Stripline or microstrip techniques should be used for the ECL interfacing. In addition, all ECL inputs should be terminated as closely as possible to the device to reduce ringing, crosstalk, and reflections.

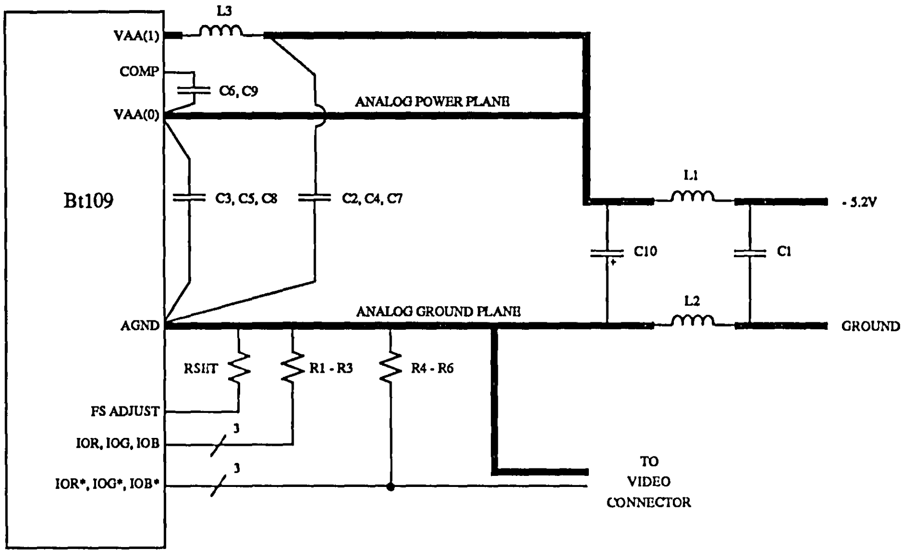
Any termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

The video output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

It is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed circuitry wiring and coaxial cable.

PC Board Layout Considerations (continued)


L3
VAA(1)
COMP
C6, C9
VAA(0)
ANALOG POWER PLANE
Bt109
C3, C5, C8
C2, C4, C7
L1
- 5.2V
C10
+
C1
L2
ANALOG GROUND PLANE
AGND
GROUND
RSET
R1 - R3
R4 - R6
FS ADJUST
IOR, IOG, IOB
3
IOR*, IOG*, IOB*
3
TO
VIDEO
CONNECTOR

Location	Description	Vendor Part Number
C1	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C2, C3	0.1 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W104KP
C4–C6	0.01 µF ceramic chip capacitor	Johanson Dielectrics X7R-500S41W103KP
C7–C9	0.001 µF ceramic chip capacitor	Johanson Dielectrics NPO-500S41N102JP
C10	10 µF tantalum capacitor	Mallory CSR13G106KM
L1, L2, L3	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	37.4 Ω 1% metal film resistor	Dale CMF-55C
R4, R5, R6	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1100 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt109.

Figure 3. Typical Connection Diagram and Parts List.

Application Information

Terminated Inputs

All digital inputs of the Bt109 should be terminated using normal ECL termination practices. In addition, all of the digital inputs have internal pull-down junctions. Thus, if a digital input is left floating, it assumes the logical zero state.

Non-Video Applications

The Bt109 may be used in non-video applications by disabling the video-specific control inputs. The SYNC, BLANK, and OVERLAY inputs should be a logical zero. All three outputs will have the same full-scale output current.

The relationship between RSET and the full-scale output current (Iout) in this configuration is as follows:

RSET (Ω) = 19,360 / Iout (mA)

With the data inputs at $00, there is a DC offset current (Imin) defined as follows:

Imin (mA) = 2,090 / RSET (Ω)

Therefore, the total full-scale output current will be Iout + Imin.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	–4.9	–5.2	–5.5	Volts
Ambient Operating Temperature	TA	0		+ 70	°C
Output Load	RL		37.5		Ω
FS ADJUST Resistor*	RSET		1100		Ω

*FS ADJUST set to 1.125 mA

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)	VAA			-6.5	Volts
Voltage on Any Digital Pin		AGND + 0.5		VAA–0.5	Volts
Analog Output Short Circuit Duration to Any Common			indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	TA (°C)	Min	Typ	Max	Units
Input High Voltage	VIH	0 +25 +70	-1170 -1130 -1070		-840 -810 -735	mV mV mV
Input Low Voltage	VIL	0 +25 +70	-1950 -1950 -1950		-1480 -1480 -1450	mV mV mV
Input High Current (Data, Sync) (Vin = VIHmax)	IIH	0 +25 +70			25 25 25	µA µA µA
Input High Current (Overlay) (Vin = VIHmax, VILmin)	IIH	0 +25 +70			210 210 210	µA µA µA
Input High/Low Current (Blank) (Vin = VIHmax, VILmin)	IIH / IIL	0 +25 +70			160 160 160	µA µA µA
Input Low Current (Data, Sync, Overlay) (Vin = VILmin)	IIL	0 25 + 70			5 5 5	µA µA µA
Input Capacitance (f = 1 MHz, Vin = VIHmax) BLANK All Others	CIN				20 7	pF pF
Internal Voltage Reference	VREF			-1.2		Volts

See test conditions on next page.

DC Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1/2	LSB
Differential Linearity Error	DL			±1/2	LSB
Gray Scale Error				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Analog Outputs					
Gray Scale Current Range:					
Black Level Relative to White				-20	mA
Blank Level Relative to White				-30	mA
Output Current					
Overlay Level		0	-5	-50	µA
White Level		-1.70	-1.90	-2.10	mA
Black Level Relative to White		-15.86	-17.62	-19.38	mA
Blank Level Relative to Black		-0.95	-1.44	-1.90	mA
Blank Level Relative to White		-16.81	-19.05	-21.28	mA
Sync Level Relative to Blank		-6.29	-7.62	-8.96	mA
LSB Size			-69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	-1.2		+1.5	Volts
Output Impedance	ROUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		9		pF
Power Supply Rejection Ratio (COMP = 0.001 µF ll 0.01 µF, f = 1 kHz)	PSRR			0.5	%/%ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for −17.62 mA full-scale output current (no sync information). Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note: The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

AC Characteristics

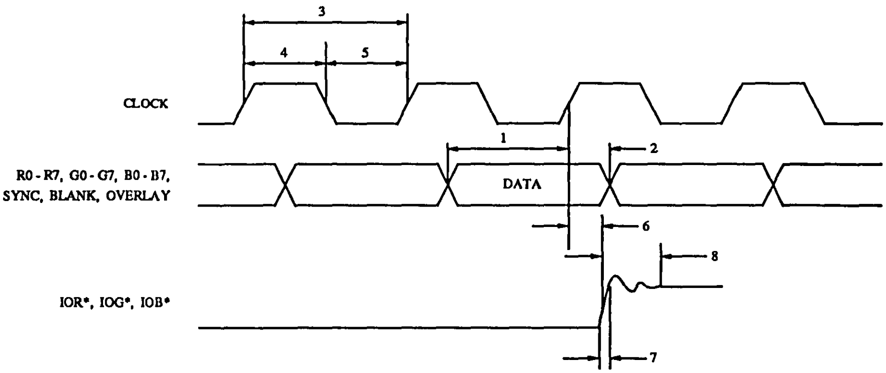
Parameter	Symbol	Min	Typ	Max	Units
Clock Rate				250	MHz
Data and Control Setup Time	1	1.5			ns
Data and Control Hold Time	2	0			ns
Clock Cycle Time	3	4			ns
Clock Pulse Width High	4	1.6			ns
Clock Pulse Width Low	5	1.6			ns
Analog Output Delay	6			3	ns
Analog Output Rise/Fall Time	7		0.5	1	ns
Analog Output Settling Time	8		4		ns
Glitch Impulse			50		pV - sec
VAA Supply Current	IAA			400	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET adjusted for –17.62 mA full-scale output current (no sync information). ECL input values are –0.89 to –1.69 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF. See timing notes in Figure 4. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt109KC	250 MHz	40-pin 0.6" Ceramic Cavity Down DIP	0° to +70° C

Timing Waveforms


3
4
5
CLOCK
1
2
R0 - R7, G0 - G7, B0 - B7,
SYNC, BLANK, OVERLAY
DATA
6
8
IOR*, IOG*, IOB*
7

Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1/2 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 4. Input/Output Timing.

Advance Information

This document contains information on a product under development. The parametric information contains target parameters and is subject to change.

Bt121

80 MHz
Monolithic CMOS
Triple 8-bit
VIDEODAC™

Distinguishing Features

- 80, 50 MHz Operation
- Triple 8-bit D/A Converters
- Optional Internal Voltage Reference
- On-Chip Analog Output Comparators
- RS-343A Compatible Outputs
- TTL-Compatible Inputs
- +5 V CMOS Monolithic Construction
- 44-pin PLCC Package
- Typical Power Dissipation: 600 mW

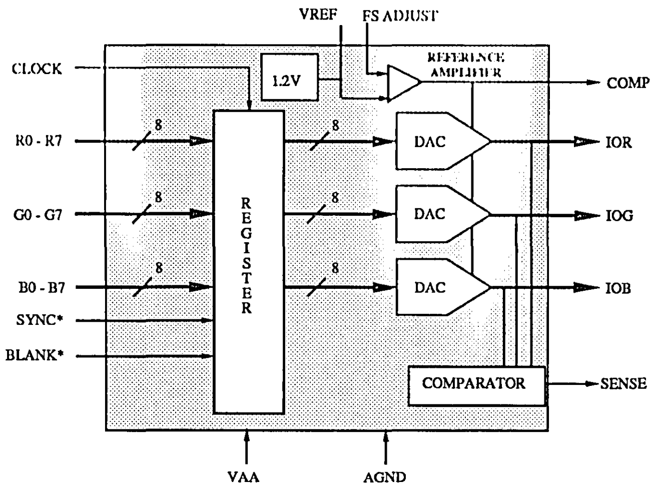
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Video Reconstruction
- Instrumentation

Related Products

- Bt473

Functional Block Diagram



Product Description

The Bt121 is a triple 8-bit VIDEODAC, designed specifically for high-performance, high-resolution color graphics.

This device offers a higher level of integration than previous VIDEODAC designs. On-chip analog output comparators are included to simplify diagnostics and debugging, with the resultant output on the SENSE* pin. Also included is an on-chip voltage reference to simplify using the device.

The Bt121 generates RS-343A compatible video signals into a doubly terminated 75 Ω load, and RS-170 compatible video signals into a singly terminated 75 Ω load, without requiring external buffering. Both the differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L121001 Rev. D

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt121 contains three 8-bit D/A converters, input registers, and a reference amplifier.

On the rising edge of CLOCK, 24 bits of color information (R0–R7, G0–G7, and B0–B7) are latched into the device and presented to the three 8-bit D/A converters.

Latched on the rising edge of CLOCK to maintain synchronization with the color data, the SYNC* and BLANK* inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as illustrated in Figure 1. Table 1 details how the SYNC* and BLANK* inputs modify the output levels.

The D/A converters on the Bt121 use a segmented architecture in which bit currents are routed to either the output or GND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

The analog outputs of the Bt121 are capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

SENSE Output*

SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). This output is used to determine the presence of a CRT monitor and, via diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The 335 mV reference has a ±5% tolerance (when using an external 1.235 V voltage reference). The tolerance is ±10% when using the internal voltage reference. Note that SYNC* should be a logical zero for SENSE* to be stable.

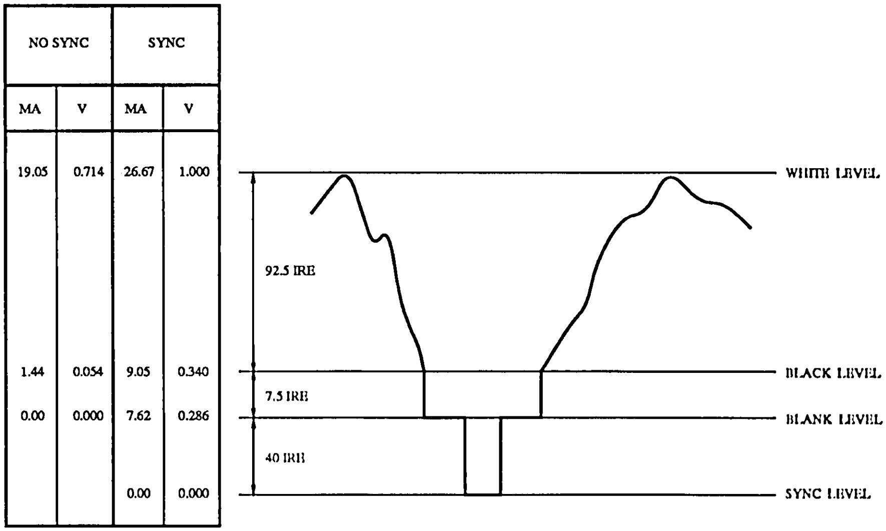
ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Circuit Description (continued)



Note: 75 Ω doubly terminated load, RSET ~ 143 Ω, VREF = 1.23 V. RS-343A levels and tolerances are assumed on all levels.

Figure 1. Composite Video Output Waveforms.

Description	Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	26.67	1	1	$FF
DATA	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	0	1	data
BLACK	9.05	1	1	$00
BLACK - SYNC	1.44	0	1	$00
BLANK	7.62	1	0	$xx
SYNC	0	0	0	$xx

Note: 75 Ω doubly terminated load, SETUP = 7.5 IRE. VREF = 1.23 V, RSET ~ 143 Ω.

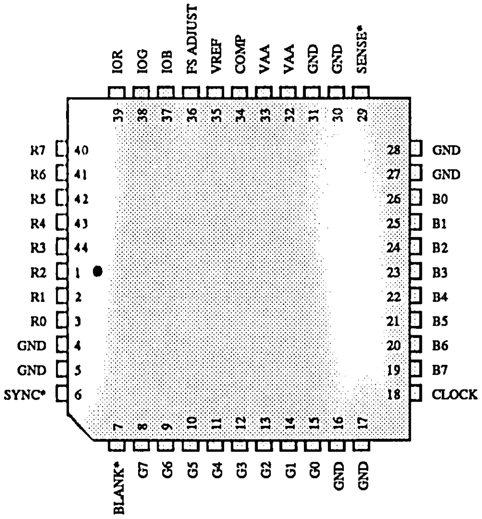
Table 1. Video Output Truth Table.

Pin Descriptions

Pin Name	Description
BLANK*	Composite blank control input (TTL compatible). A logical zero drives the IOR, IOG, and IOB outputs to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the R0–R7, G0–G7, and B0–B7 inputs are ignored.
SYNC*	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the IOR, IOG, IOB outputs (see Figure 1). SYNC* does not override any other control or data input, as shown in Table 1; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK.
R0–R7, G0–G7, B0–B7	Red, green, and blue data inputs (TTL compatible). R0, G0, and B0 are the least-significant data bits. They are latched on the rising edge of CLOCK. Coding is binary.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK latches the R0–R7, G0–G7, B0–B7, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
IOR, IOG, IOB	Red, green, and blue current outputs. These high-impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable (Figures 2 and 3). All outputs, whether used or not, should have the same output load.
SENSE*	Sense output (CMOS compatible). SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level (335 mV). Note that SENSE* may not be stable while SYNC* is toggling.
FS ADJUST	Full-scale adjust control. A resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal (Figure 1). Note that the IRE relationships in Figure 1 are maintained, regardless of the full-scale output current. The relationship between RSET and the full-scale output current on IOR, IOG and IOB is: RSET (Ω) = K * VREF (V) / IO (mA) Where; K = 2,295 with SYNC*=0 K = 3,195 with SYNC*=1

Pin Descriptions (continued)

Pin Name	Description
COMP	Compensation pin. This pin provides compensation for the internal reference amplifier. A 0.01 µF ceramic capacitor in series with a resistor should be connected between this pin and the nearest VAA pin (Figures 2 and 3) for optimum settling time. Connecting the capacitor to VAA rather than to GND provides the highest possible power supply noise rejection. The COMP resistor and capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum.
VREF	Voltage reference input. If an external voltage reference is used (Figure 3), it must supply this input with a 1.2 V (typical) reference. A 0.1 µF ceramic capacitor must always be used to decouple this input to GND, as shown in Figures 2 and 3. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When using the internal reference, this pin should not drive any external circuitry, except for the decoupling capacitor (Figure 2).
GND	Analog ground. All GND pins must be connected.
VAA	Analog power. All VAA pins must be connected.


IOR 39
IOG 38
IOB 37
FS ADJUST 36
VREF 35
COMP 34
VAA 33
VAA 32
GND 31
GND 30
SENSE* 29
R7 40
R6 41
R5 42
R4 43
R3 44
R2 1
R1 2
R0 3
GND 4
GND 5
SYNC* 6
28 GND
27 GND
26 B0
25 B1
24 B2
23 B3
22 B4
21 B5
20 B6
19 B7
18 CLOCK
BLANK* 7
G7 8
G6 9
G5 10
G4 11
G3 12
G2 13
G1 14
G0 15
GND 16
GND 17

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt121 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. Ground planes must provide a low-impedance return path for the digital circuits. A minimum of a four-layer PC board is recommended with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

The optimum layout enables the Bt121 to be located as close to the power supply connector and the video output connector as possible.

Ground Planes

For optimum performance, a common digital and analog ground plane with tub isolation (at least a 1/8 inch gap) connected together only at the power supply connector (or the lowest impedance source) is recommended. Ground plane partitioning should extend the analog ground plane no more than 2 inches from the power supply connector.

The digital ground plane should be under all digital signal traces to minimize radiated noise and crosstalk.
The analog ground plane should include all Bt121 ground pins, all reference circuitry and decoupling (external reference if used, RSET resistors, etc.), power supply bypass circuitry for the Bt121, analog output traces, and the video output connector.

Power Planes

Separate digital and analog power planes are necessary. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt121 power pins, any reference circuitry, and COMP and reference decoupling. There should be at least a 1/8 inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 2 and 3. This bead should be located within 3 inches of the Bt121. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Fair-Rite 2743001111, Ferroxcube 5659065-3B, or TDK BF45-4001.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the digital power and ground planes do not overlay portions of the analog power and ground planes, unless they can be arranged so that the plane-to-plane noise is common mode.

Device Decoupling

For optimum performance, all capacitors should be located as close to the device as possible, using the shortest leads possible (consistent with reliable operation) to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

Best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor decoupling each of the VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.001 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device.

The 10 µF capacitor is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

PC Board Layout Considerations (continued)

A linear regulator to filter the analog power supply is recommended if the power supply noise is ≥ 50 mV. This is especially important when a switching power supply is used and the switching frequency is close to the raster scan frequency. Note that about 10% of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically using a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. Lead lengths should be minimized for best performance.

If the display has a "ghosting" problem, additional capacitance in parallel with the COMP capacitor may help to fix the problem.

Digital Signal Interconnect

The digital inputs to the Bt121 should be isolated from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power and ground planes.

Most noise on the analog outputs will be caused by excessive edge speeds (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge speeds should be no faster than necessary, as feedthrough noise is proportional to the digital edge speeds. Lower speed applications will benefit from using lower speed logic (3-5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission line mismatch will exist if the line length reflection time is greater than 1/4 the signal edge time, resulting in ringing, overshoot, and undershoot that can generate noise onto the analog outputs. Line termination or reducing the line length is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without using termination. Ringing may be reduced by damping the line with a series resistor (10 to 50 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge speeds (rise/fall time), minimizing ringing by using damping resistors, and minimizing coupling through PC board capacitance by routing 90 degrees to any analog signals.

Ensure that the power pins for the clock driver are properly decoupled to minimize transients. Minimize edge speeds and ringing, using damping resistors (10 to 50 Ω) or parallel termination where necessary.

If using parallel termination on digital signals, the resistors should be connected to the digital power and ground planes, not the analog power and ground planes.

Analog Signal Interconnect

The Bt121 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the analog ground plane, not the analog power plane, to maximize the high-frequency power supply rejection.

For maximum performance, the analog outputs should have a source load resistor equal to the destination termination (via a clean isolated ground return path). The load resistor connection between the current output and GND should be as close as possible to the Bt121 to minimize reflections. Unused analog outputs should be connected to GND.

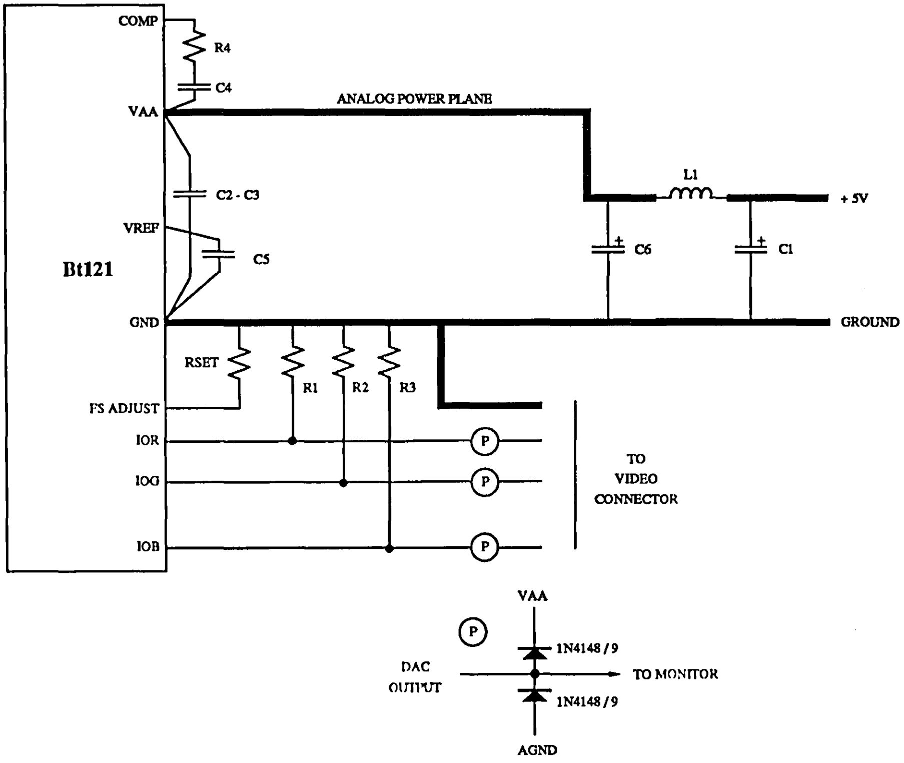
Analog edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise reduction.

Analog Output Protection

The Bt121 analog outputs should be protected against high-energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figures 2 and 3 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations (continued)

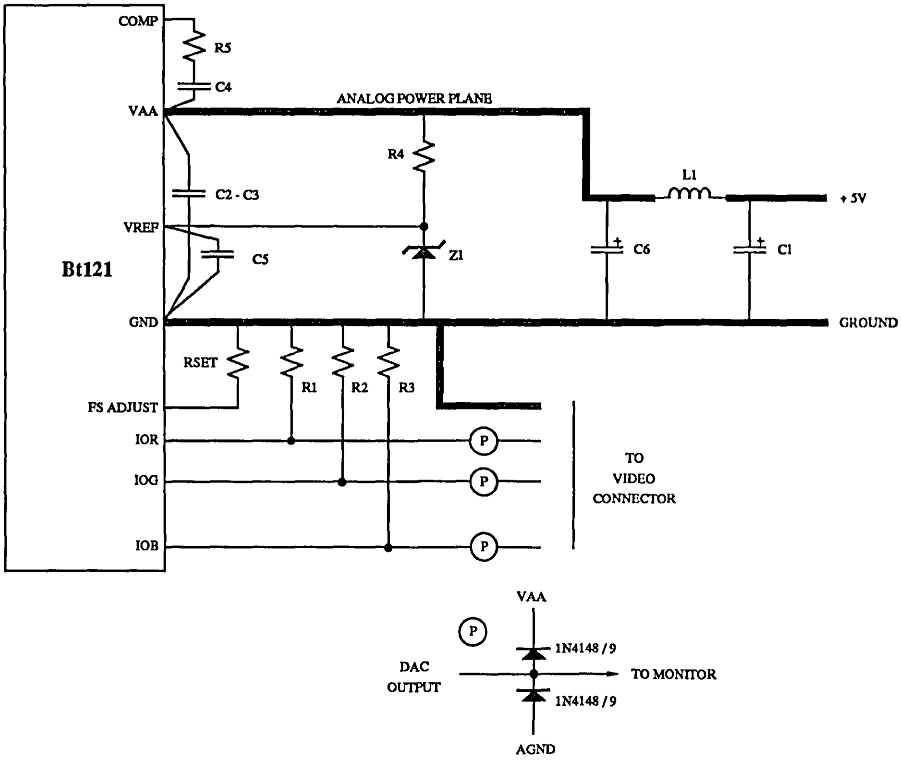

COMP
R4
C4
ANALOG POWER PLANE
VAA
L1
C2 - C3
+5V
VREF
C5
C6
C1
Bt121
GND
GROUND
RSET
R1
R2
R3
FS ADJUST
IOR
P
IOG
P
TO
VIDEO
CONNECTOR
IOB
P
VAA
P
1N4148 / 9
DAC
OUTPUT
TO MONITOR
1N4148 / 9
AGND

Location	Description	Vendor Part Number
C1	33 µF tantalum capacitor	Mallory CSR13F336KM
C2, C3, C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C4	0.01 µF ceramic capacitor	Erie RPE110Z5U103M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	15 Ω 1% metal film resistor	Dale CMF-55C
RSET	143 Ω 1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt121.

Figure 2. Typical Connection Diagram and Parts List (Internal Reference).

PC Board Layout Considerations (continued)


COMP
R5
C4
VAA
ANALOG POWER PLANE
R4
L1
+5V
C2 - C3
VREF
C5
Z1
C6
C1
Bt121
GND
GROUND
RSET
R1
R2
R3
FS ADJUST
IOR
IOG
IOB
P
TO
VIDEO
CONNECTOR
VAA
1N4148 / 9
DAC
OUTPUT
TO MONITOR
1N4148 / 9
AGND

Location	Description	Vendor Part Number
C1	33 µF tantalum capacitor	Mallory CSR13F336KM
C2, C3, C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C4	0.01 µF ceramic capacitor	Erie RPE110Z5U103M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1000 Ω 5% metal film resistor	
R5	15 Ω 1% metal film resistor	Dale CMF-55C
RSET	143 Ω 1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt121.

Figure 3. Typical Connection Diagram and Parts List (External Reference).

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
80, 66 MHz Parts		4.75	5.00	5.25	Volts
50, 35 MHz Parts		4.5	5.00	5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ohms
External Reference Voltage	VREF	1.14	1.235	1.26	Volts
FS ADJUST Resistor	RSET		143		Ohms

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND– 0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to Any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the absolute maximum ratings (especially relative to VAA or between VAA pins) can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Gray Scale Error					
External Reference				±5	% Gray Scale
Internal Reference				±10	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN			7	pF
Digital Output (SENSE*)					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 400 µA)	VOL			0.4	Volts
Output Capacitance	CDOUT			7	pF
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current					
White Level Relative to Blank		17.69	19.05	20.40	mA
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Blank		0.95	1.44	1.90	mA
Sync Level on IOR, IOG, IOB		6.29	7.62	7.94	mA
LSB Size			69.72		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	0		+1.4	Volts
Output Impedance	ROUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	COUT		30		pF
Voltage Reference Input Current	IVREF			10	µA
Power Supply Rejection Ratio* (COMP = 0.01 µF, f = 1 kHz)	PSRR		0.2	0.5	% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 143 Ω, VREF = 1.235 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note: When using the internal voltage reference, RSET may need to be adjusted to meet these limits.

*Guaranteed by characterization, not tested.

AC Characteristics

		80 MHz Devices			50 MHz Devices			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Units
Clock Rate	Fmax			80			50	MHz
Data and Control Setup Time	1	3			3			ns
Data and Control Hold Time	2	3			3			ns
Clock Cycle Time	3	12.5			20			ns
Clock Pulse Width High Time	4	4			7			ns
Clock Pulse Width Low Time	5	4			7			ns
Analog Output Delay	6			30			30	ns
Analog Output Rise/Fall Time	7		3			3		ns
Analog Output Settling Time	8		12.5			15.5		ns
Clock and Data Feedthrough*			–30			–30		dB
Glitch Impulse*			75			75		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew			0	3		0	3	ns
Pipeline Delay		2	2	2	2	2	2	Clock
SENSE* Output Delay	9		1			1		µS
VAA Supply Current**	IAA		tbd			tbd		mA

See test conditions on next page.

Test conditions (unless otherwise specified): "Recommended Operating Conditions" using external voltage reference with RSET = 143 Ω, VREF = 1.235 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF, SENSE* output load ≤ 50 pF. See timing notes in Figure 4. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

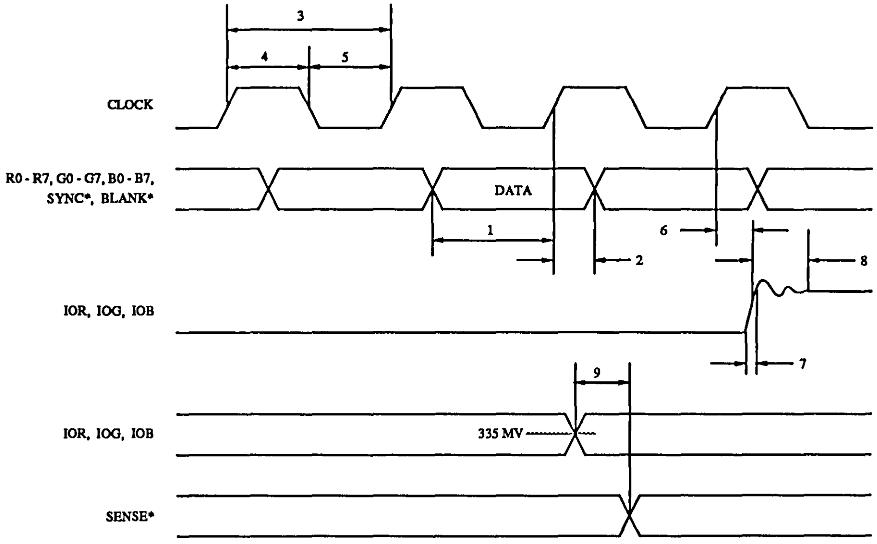
*Clock and data feedthrough is a function of the amount of edge rates, overshoot, and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to the regular PCB ground plane and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, –3 dB test bandwidth = 2x clock rate.

**At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

Ordering Information

Model Number	Speed	Package	Ambient Temperature Range
Bt121KPJ80	80 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt121KPJ50	50 MHz	44-pin Plastic J-Lead	0° to +70° C

Timing Waveforms


3
4
5
CLOCK
R0 - R7, G0 - G7, B0 - B7, SYNC*, BLANK*
DATA
1
2
6
8
IOR, IOG, IOB
7
9
IOR, IOG, IOB
335 MV
SENSE*

Note 1: Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 4. Input/Output Timing.

SECTION 6

PERIPHERALS

Contents

Data Conversion

Bt110 100 ns Monolithic CMOS Octal 8-bit D/A Converter 6 - 3

High Speed Lookup Tables

Bt401 250 MHz 10KH ECL 256 x 8 Pipelined Static RAM 6 - 17

Bt403 250 Mhz 10KH ECL 256 x 8 Pipelined Static RAM 6 - 17

High Speed Shift Registers

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Clock Generator Chips for 80+ MHz CMOS RAMDACs

Bt438 250 MHz Clock Generator Chip with Voltage Reference, + 3, 4, 5, or 8 for Load Generation (TTL compatible) 6 - 61

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ECL Compatible Adjustable Delay Lines

Bt622 Very High Speed, 10KH ECL Compatible, Dual Channel Delay Line 6 - 123

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Bt110

100 ns Monolithic CMOS Octal 8-bit D/A Converter

Distinguishing Features

- Eight 8-bit D/A Converters
- 100 ns Settling Time to ±1 LSB
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- Guaranteed Monotonic
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 44-pin PLCC Package
- Typical Power Dissipation: 150 mW

Applications

- Instrumentation
- Test Equipment
- Waveform Synthesis
- Data Acquisition Systems

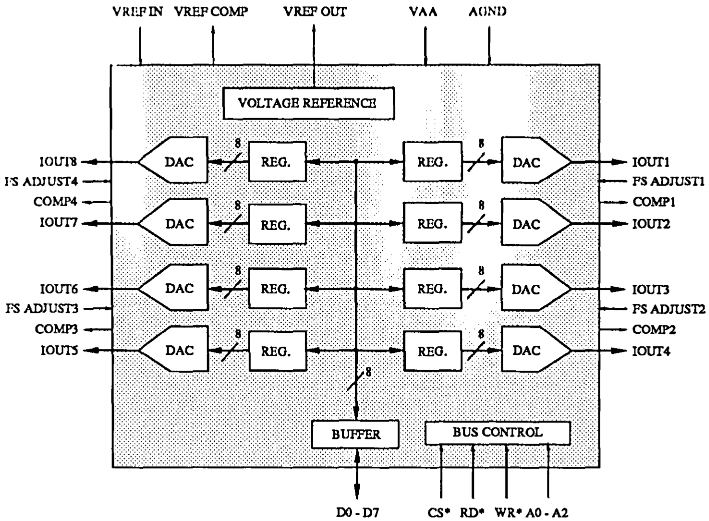
Product Description

The Bt110 is an octal 8-bit D/A converter. It provides eight independent D/A converters and has a standard MPU interface.

The D/A converters are arranged in pairs, with each pair sharing a common reference amplifier. This provides excellent matching and stability of the paired D/A converters.

An on-chip voltage reference is provided or an external reference may be used. Differential and integral linearity errors of the D/A converters are guaranteed to be a maximum of ±1 LSB over the full temperature range.

Functional Block Diagram


VREF IN
VREF COMP
VREF OUT
VAA
AGND
VOLTAGE REFERENCE
IOUT8
FS ADJUST4
COMP4
IOUT7
IOUT6
FS ADJUST3
COMP3
IOUT5
DAC
REG.
8
IOUT1
FS ADJUST1
COMP1
IOUT2
IOUT3
FS ADJUST2
COMP2
IOUT4
BUFFER
BUS CONTROL
D0 - D7
CS*
RD*
WR*
A0 - A2

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L110001 Rev. G

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt110 contains eight 8-bit D/A converters, eight nontransparent (D-type) octal data registers, and MPU bus interface logic. Also included on chip are four reference amplifiers and a voltage reference.

The Bt110 supports a conventional MPU bus interface through the use of the CS*, RD*, WR*, D0–D7, and A0–A2 pins. A0–A2 specify which one of the eight internal data latches the MPU is accessing. These data latches may be written to or read by the MPU at any time. The input/output timing is illustrated in Figure 1.

The data contained in the data latches is presented to the associated D/A converter and used to specify the output current level. The MPU may read these data latches to determine what data is present at each D/A converter.

The full-scale output current of each pair of D/A converters is set by an external resistor (RSET) between the FS ADJUST pin and AGND. FS ADJUST1 controls the full-scale output current of IOUT1 and IOUT2, FS ADJUST2 controls the full-scale output current of IOUT3 and IOUT4, FS ADJUST3 controls the full-scale output current of IOUT5 and IOUT6, and FS ADJUST4 controls the full-scale output current of IOUT7 and IOUT8.

The on-chip voltage reference (VREF OUT) may be used to provide the reference voltage for the VREF IN pin or an external reference circuit may be used. The on-chip reference should offer adequate performance for most applications.

Better temperature stability may be attainable by using an external voltage reference, such as the LM385BZ-1.2. The use of a resistor network to generate the reference voltage is not recommended, as any low frequency power supply noise on VREF IN will be directly coupled onto the analog outputs.

The D/A converters on the Bt110 use a segmented architecture in which bit currents are routed to either IOUT or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. The on-chip operational amplifiers stabilize the full-scale output currents against temperature and power supply variations.

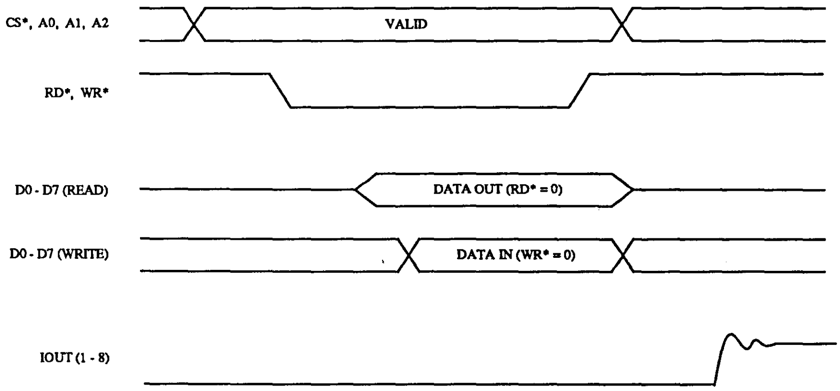


Figure 1. Input/Output Timing.

Pin Descriptions

Pin Name	Description
FS ADJUST (1–4)	Full-scale adjust controls. A resistor (RSET) between each of these pins and AGND controls the full-scale output currents. FS ADJUST1 controls the full-scale output current for IOUT1 and IOUT2, FS ADJUST2 controls the full-scale output current for IOUT3 and IOUT4, FS ADJUST3 controls the full-scale output current for IOUT5 and IOUT6, and FS ADJUST4 controls the full-scale output current for IOUT7 and IOUT8. The relationship between the full-scale output current of each D/A and RSET is defined as follows: $\text{RSET}(\Omega) = 1000 * \text{VREF IN (V)} / \text{IOUT (mA)}$
COMP (1–4)	Compensation pins. These pins provide compensation for the internal reference amplifiers. A 0.1 µF ceramic capacitor should be connected between each compensation pin and VAA, as illustrated in Figure 2. Decoupling the capacitors to VAA rather than to AGND provides the highest possible power supply noise rejection. COMP1 provides compensation for IOUT1 and IOUT2, COMP2 provides compensation for IOUT3 and IOUT4, COMP3 provides compensation for IOUT5 and IOUT6, and COMP4 provides compensation for IOUT7 and IOUT8.
IOUT (1–8)	High-impedance current outputs. These current outputs are designed to drive into a virtual ground, such as an operational amplifier.
VREF OUT	Voltage reference output. This output provides a 1.2 V (typical) reference, and may be directly connected to the VREF IN pin. When used to provide a reference voltage to VREF IN, an external 1000 Ω resistor must be connected between VREF OUT and AGND.
VREF IN	Voltage reference input. Either an external voltage reference circuit or the VREF OUT pin is used to supply this input with a 1.2 V (typical) reference. A 0.1 µF ceramic capacitor must be connected between this pin and VREF COMP.
VREF COMP	VREF IN compensation pin. A 0.1 µF ceramic capacitor must be connected between this pin and VREF IN.
AGND	Analog ground. All AGND pins must be connected.
VAA	Analog power. All VAA pins must be connected.
CS*	Chip select control input (TTL compatible). To enable data to be written to or read from the device, this input must be a logical zero. While it is a logical one, D0–D7 are three-stated. Note that the Bt110 will not function correctly while CS*, RD*, and WR* are simultaneously a logical zero.
RD*	Read control input (TTL compatible). To enable data to be read from the device, both CS* and RD* must be a logical zero. See Figure 1.

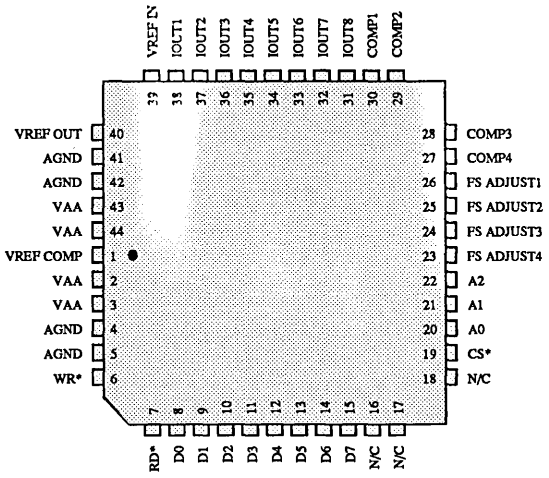
Pin Descriptions (continued)

Pin Name	Description
A0, A1, A2	Select control inputs (TTL compatible). These inputs specify which internal D/A latch will be written to or read, as follows:

A2, A1, A0	D/A Output
000	IOUT1
001	IOUT2
010	IOUT3
011	IOUT4
100	IOUT5
101	IOUT6
110	IOUT7
111	IOUT8

Pin Name	Description
WR*	Write control input (TTL compatible). To enable data to be written to the device, both CS* and WR* must be a logical zero. Data is internally latched on the rising edge of WR* or CS*, whichever occurs first. See Figure 1.
D0–D7	Bidirectional data bus (TTL compatible). Data is transferred into and out of the Bt110 over this 8-bit data bus. D0 is the least significant bit.

44-pin Plastic J-Lead (PLCC)
Package


VREF IN 39
IOUT1 38
IOUT2 37
IOUT3 36
IOUT4 35
IOUT5 34
IOUT6 33
IOUT7 32
IOUT8 31
COMP1 30
COMP2 29
VREF OUT 40
AGND 41
AGND 42
VAA 43
VAA 44
VREF COMP 1
VAA 2
VAA 3
AGND 4
AGND 5
WR* 6
28 COMP3
27 COMP4
26 FS ADJUST1
25 FS ADJUST2
24 FS ADJUST3
23 FS ADJUST4
22 A2
21 A1
20 A0
19 CS*
18 N/C
RD* 7
D0 8
D1 9
D2 10
D3 11
D4 12
D5 13
D6 14
D7 15
N/C 16
N/C 17

Note: N/C pins may be left floating without affecting the performance of the Bt110.

PC Board Layout Considerations

PC Board Considerations

The layout for the Bt110 should be optimized for lowest noise on the Bt110 power and ground lines by shielding the digital inputs and providing good decoupling. The trace length between groups of VAA and AGND pins should be as short as possible to minimize inductive ringing.

Ground Planes

The Bt110 and any associated analog circuitry should have its own ground plane, referred to as the analog ground plane. This ground plane should connect to the regular PCB ground plane at a single point through a ferrite bead, as illustrated in Figure 2. This bead should be located within 3 inches of the Bt110.

The analog ground plane area should encompass all Bt110 ground pins, any external voltage reference circuitry, power supply bypass circuitry for the Bt110, the analog output traces, and any output amplifiers.

The regular PCB ground plane area should encompass all the digital signal traces, excluding the ground pins, leading up to the Bt110.

Power Planes

The Bt110 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane at a single point through a ferrite bead, as illustrated in Figure 2. This bead should be located within 3 inches of the Bt110.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt110 power pins, any external voltage reference circuitry, and any output amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power or ground planes, unless they can be arranged so that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

For the best performance, a 0.1 µF ceramic capacitor should be used to decouple each VAA pin (or group of VAA pins if they are adjacent) to the adjacent AGND pins. The capacitor should be placed as close as possible to the device.

A 0.1 µF ceramic capacitor must also be connected between each COMP pin (COMP1–COMP4) and VAA. These capacitors should be placed as close as possible to the device.

A 0.1 µF ceramic capacitor must also be connected between the VREF COMP pin and the VREF IN pin. This capacitor should be placed as close as possible to the device.

It is important to note that while the Bt110 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the Bt110 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog ground and power planes.

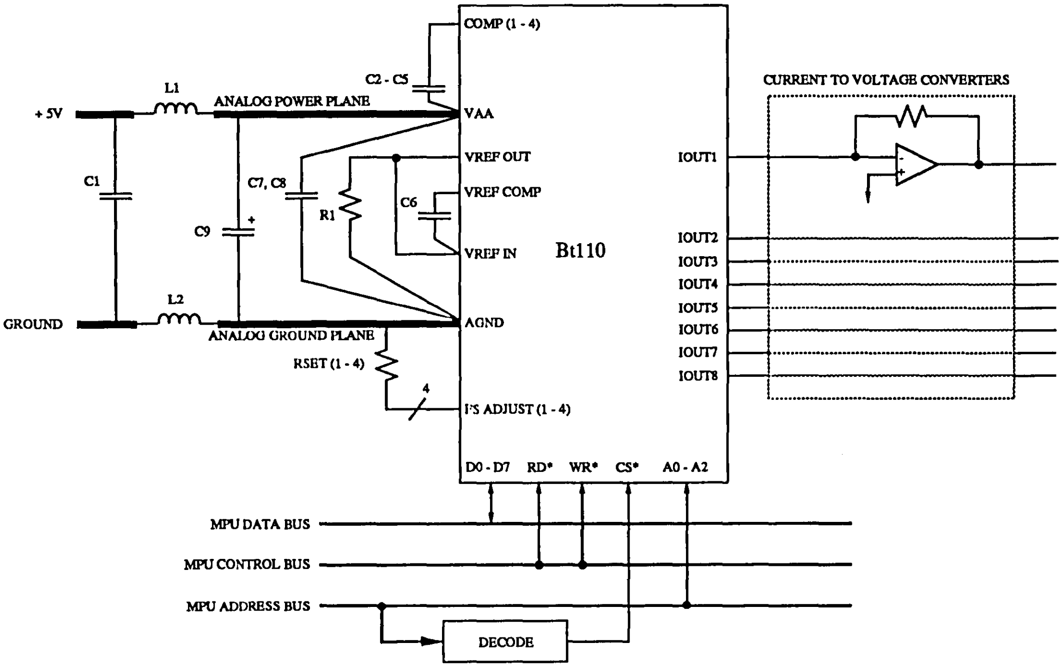
Any active termination resistors for the digital inputs should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

The Bt110 should be located as close as possible to the output amplifiers. Also, any external voltage reference circuitry should be as close as possible to the Bt110 to avoid noise pickup.

The analog output signals should overlay the analog ground plane, and not the analog power plane, to maximize the high-frequency power supply rejection.

PC Board Layout Considerations (continued)


COMP (1 - 4)
C2 - C5
L1
ANALOG POWER PLANE
+5V
VAA
VREF OUT
VREF COMP
C1
C7, C8
R1
C6
+
C9
VREF IN
Bt110
L2
GROUND
AGND
ANALOG GROUND PLANE
RSET (1 - 4)
4
FS ADJUST (1 - 4)
D0 - D7
RD*
WR*
CS*
A0 - A2
CURRENT TO VOLTAGE CONVERTERS
IOUT1
-
+
IOUT2
IOUT3
IOUT4
IOUT5
IOUT6
IOUT7
IOUT8
MPU DATA BUS
MPU CONTROL BUS
MPU ADDRESS BUS
DECODE

Location	Description	Vendor Part Number
C1–C8	0.1 µF ceramic capacitor	Eric RPE112Z5U104M50V
C9	22 µF tantalum capacitor	Mallory CSR13G226KM
L1, L2	ferrite bead	Fair-Rite 2743001111
R1	1000 Ω 1% metal film resistor	Dale CMF-55C
RSET (1–4)	1% metal film resistors	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt110.

Figure 2. Typical Connection Diagram and Parts List (Internal Reference).

Application Information

External Voltage Reference

For improved temperature stability, an external voltage reference may be used with the Bt110, as shown in Figure 3. In this instance, the VREF OUT pin should remain floating. The temperature stability of the internal reference is equivalent to about 1/4 LSB.

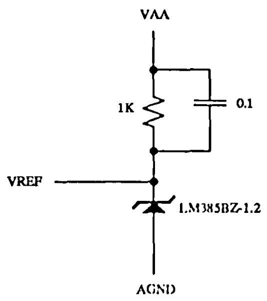


Figure 3. External Voltage Reference.

Programmable Window Comparator

The window comparator of Figure 4 is a circuit that may be used to determine whether the input voltage (Vin) lies within predefined limits. Using the Bt110, up to four programmable window comparators may be implemented.

One DAC of the matched pair is used to set the low limit and the other DAC is used to set the high limit. Thus, each pair of DACs form a window of programmable size. The output will be high while Vlow ≤ Vin ≤ Vhigh.

For a RSET value of 1200 Ω and a VREF IN voltage of 1.2 V, the Bt110 outputs a full scale output current of approximately 1 mA onto IOUT1 and IOUT2. The 1 kΩ resistor generates a 0 V to 1 V output voltage (for DAC codes $00 to $FF), which is amplified to 0 V to 5 V (5x) by the LM358 dual operational amplifier. In this configuration, the LM358 is operating from a single +5 V power supply.

The LM319 dual comparator is also operating from a single +5 V power supply and compares the Vlow and Vhigh voltage levels to Vin. The 500 Ω pull-up resistor is necessary as the LM319 has open-collector outputs.

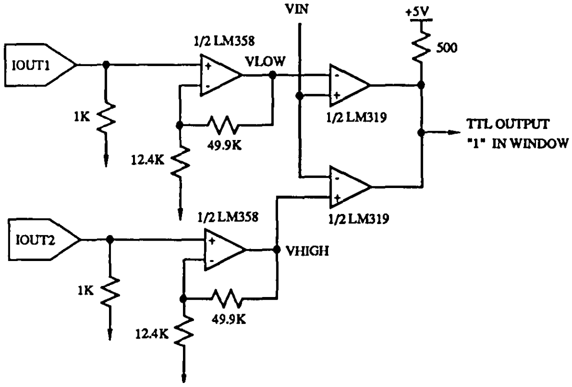


Figure 4. Programmable Window Comparator.

Application Information (continued)

Programmable Power Supply

The Bt110, when used with an external operational amplifier and power transistor, provides a way of generating voltages and currents outside of the Bt110's normal capability. Figure 5 illustrates a 0 V to 10 V programmable power supply.

For a RSET value of 1200 Ω and a VREF IN voltage of 1.2 V, the Bt110 outputs a full-scale output current of approximately 1 mA onto IOUT1. The 1 kΩ resistor is used to generate a 0 V to 1 V output voltage from the Bt110 (for DAC codes $00 to $FF). One of the operational amplifiers in the LM358 (A1) is used to multiply the voltage at IOUT1 by 10x, resulting in a 0 V to 10 V range. In this configuration, the LM358 is operating from a single +15 V power supply.

The other operational amplifier in the LM358 (A2) is used as a buffer and driver for the TIP31 transistor. RS is the current limiting resistor to shut down the output in case of an overload. The correct value for RS is determined as follows:

$$RS = 0.7 / IOUTmax$$

For output voltages down to or near 0 V, it is necessary to use a CMOS operational amplifier with a very low saturation voltage, or a plus/minus power supply and a bipolar operational amplifier to allow for output saturation, which is typically 2 V to 3 V below the supply voltage.

Driving Active Devices

If the Bt110 is driving an active device whose supply is outside the 0 V to 5 V range, the analog output(s) should be clamped to VAA (see Figure 5).

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VAA pins are at the same potential, and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

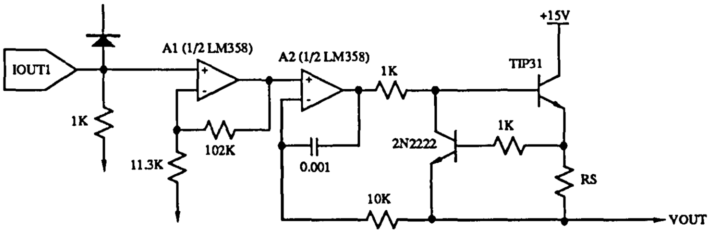


Figure 5. Programmable Power Supply.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Reference Voltage	VREF IN	1.0	1.2	1.3	Volts

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to AGND)				7.0	Volts
Voltage on any Signal Pin*		AGND–0.5		VAA + 0.5	Volts
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Full-Scale (Gain) Error	EG				
Using Internal Reference				±10	% of FSR
Using External Reference				±5	% of FSR
Zero Error	EZ			5	µA
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	Volts
Input Low Voltage	VIL	AGND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = –800 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	Volts
3-state Current	IOZ			1	µA
Output Capacitance	CDOUT		10		pF
Analog Outputs					
Output Current				1	mA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–1.0		+1.2	Volts
Output Impedance	RAOUT		125		kΩ
Output Capacitance (IOUT1–IOUT8 = 0 mA)	CAOUT		20		pF
Reference Output Voltage	VREF OUT	1.05	1.17	1.29	Volts
Reference Output Current	IREF OUT		1.2		mA
Reference Input Current	IREF IN			10	µA
Power Supply Rejection Ratio (COMP = 0.1 µF, f = 1 kHz)	PSRR		0.3		% / % ΔVAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 1000 Ω, VREF IN = 1.0 V. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

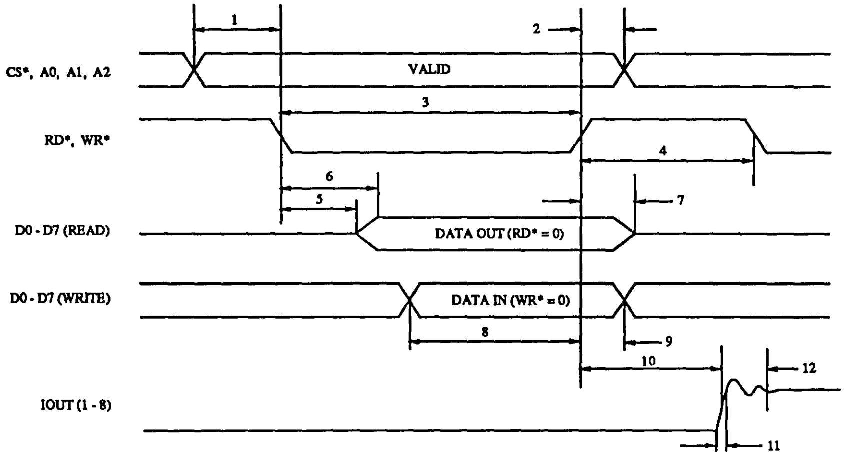
Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate	Tmax			100	ns
CS*, A0, A1, A2 Setup Time	1	30			ns
CS*, A0, A1, A2 Hold Time	2	5			ns
WR* Low Time	3	30			ns
RD*, WR* High Time	4	20			ns
RD* Asserted to Data Bus Driven	5	10			ns
RD* Asserted to Data Valid	6			60	ns
RD* Negated to Data Bus 3-Stated	7			40	ns
Write Data Setup Time	8	20			ns
Write Data Hold Time	9	10			ns
Analog Outputs					
Analog Output Delay	10		15		ns
Analog Output Rise/Fall Time	11				
into 50 Ω				10	ns
into 1 kΩ			350		ns
Analog Output Settling Time	12				
into 50 Ω				100	ns
into 1 kΩ			800		ns
Data Feedthrough			–30		dB
Glitch Impulse			75		pV–sec
DAC-to-DAC Crosstalk			–25		dB
VAA Supply Current*	IAA		30	38	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with RSET = 1000 Ω, VREF IN = 1.0 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF into a virtual ground, D0–D7 output load ≤ 130 pF. See timing notes in Figure 6. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*IAA (typ) at VAA = 5.0 V. IAA (max) at VAA = 5.25 V.

6

Timing Waveforms


CS*, A0, A1, A2
RD*, WR*
D0 - D7 (READ)
D0 - D7 (WRITE)
IOUT (1 - 8)
VALID
DATA OUT (RD* = 0)
DATA IN (WR* = 0)
1
2
3
4
5
6
7
8
9
10
11
12

Note 1: Output delay measured from the rising edge of WR* to the 50% point of full-scale transition.

Note 2: Settling time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.

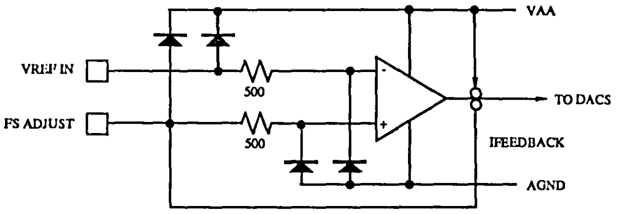
Note 3: Output rise/fall time measured between the 10% and 90% points of full-scale transition.

Figure 6. Input/Output Timing.

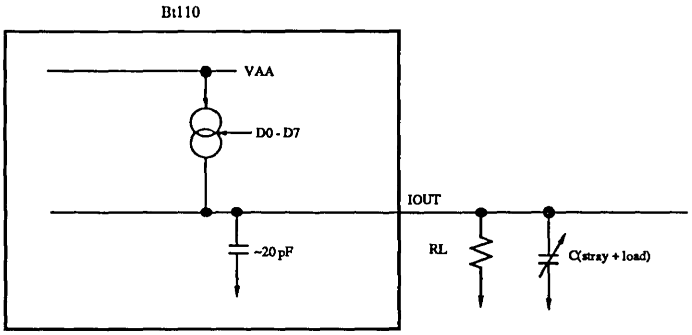
Ordering Information

Model Number	Package	Ambient Temperature Range
Bt110KPJ	44-pin Plastic J-Lead	0° to +70° C

Device Circuit Data


VAA
VREF IN
FS ADJUST
500
500
-
+
TO DACS
IFEEDBACK
AGND

Equivalent Circuit of the Reference Amplifier.


Bt110
VAA
D0 - D7
IOUT
~20 pF
RL
C(stray + load)

Equivalent Circuit of the Current Outputs.

Bt401

Bt403

250 MHz
10KH ECL
256 x 8 Pipelined
Static RAM

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Distinguishing Features

- 250 MHz Pipelined Operation
- Optional 3 x 8 Overlay Registers
- 10KH ECL Compatible
- Synchronous or Asynchronous Reading
- Asynchronous Writing
- 28-pin 0.6" or 24-pin 0.3" DIP Package
- Typical Power Dissipation: 1100 mW

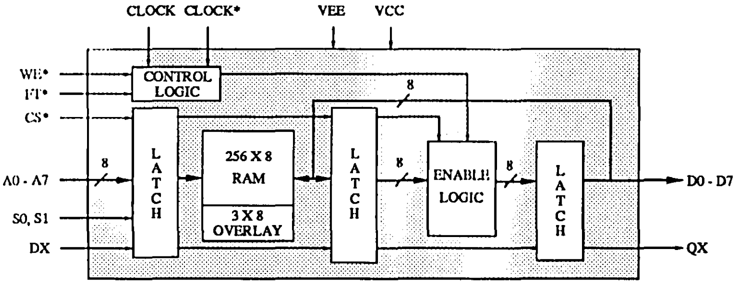
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Microcode Storage

Related Products

- Bt424, Bt501, Bt502

Functional Block Diagram



Product Description

The Bt401 is a pipelined 256 x 8 RAM designed for high-speed graphics applications. In addition to the 256 colors supported by the RAM, an additional three colors are available via the internal overlay registers, allowing for cursor support, highlighting, etc. Also incorporated is an input/output "pipe" for maintaining synchronization of video control signals.

Both the Bt401 and Bt403 are 10KH ECL compatible.

The Bt403 does not have the three overlay registers and input/output "pipe".

The devices may be read either synchronously or asynchronously and written to asynchronously. The asynchronous modes of operation simplify interfacing to an MPU.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L401001 Rev. D

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt401 and Bt403 each contain a pipelined 256 x 8 RAM and control logic.

The Bt401 has three 8-bit overlay registers, which may be used to overlay menus, cursors, etc. onto the display screen, and a "pipe" consisting of DX and QX to facilitate pipelining of control signals. Regardless of the value of FT*, the DX value is latched on the rising edge of CLOCK and output onto QX two clock cycles later.

The device operates in either a synchronous read, asynchronous read, or an asynchronous write mode, as determined by the state of the FT* input. The synchronous read mode is typically used only for high-speed (250 MHz) read operations, while the asynchronous read and write modes are used to enable the MPU to read and write to the device at relatively slower data rates.

Table 1 summarizes the various modes of operation.

A0–A7	S0	S1	FT*	WE*	CS*	Operation	Mode
$00	0	0	1	x	0	read RAM location $00	synchronous
:	:	:	:	:	:	:	:
$FF	0	0	1	x	0	read RAM location $FF	synchronous
$xx	0	1	1	x	0	read overlay register 1	synchronous
$xx	1	0	1	x	0	read overlay register 2	synchronous
$xx	1	1	1	x	0	read overlay register 3	synchronous
$xx	x	x	1	x	1	D0–D7 = 0	synchronous
$xx	x	x	0	x	1	D0–D7 = 0	asynchronous
$00	0	0	0	1	0	read RAM location $00	asynchronous
:	:	:	:	:	:	:	:
$FF	0	0	0	1	0	read RAM location $FF	asynchronous
$xx	0	1	0	1	0	read overlay register 1	asynchronous
$xx	1	0	0	1	0	read overlay register 2	asynchronous
$xx	1	1	0	1	0	read overlay register 3	asynchronous
$00	0	0	0	0	0	write RAM location $00	asynchronous
:	:	:	:	:	:	:	:
$FF	0	0	0	0	0	write RAM location $FF	asynchronous
$xx	0	1	0	0	0	write overlay register 1	asynchronous
$xx	1	0	0	0	0	write overlay register 2	asynchronous
$xx	1	1	0	0	0	write overlay register 3	asynchronous

Table 1. Control Truth Table.

Circuit Description (continued)

Synchronous Read Operation

The A0–A7, S0, S1, and CS* inputs are latched on the rising edge of CLOCK. S0 and S1 are used to specify whether the RAM or one of the overlay registers is to provide data, as illustrated in Table 1. When accessing the RAM, the A0–A7 inputs are used to specify which one of the 256 locations are to provide the data. When accessing the overlay registers, the A0–A7 inputs are ignored.

During synchronous operation, the WE* input is ignored.

Note that CS* must be a logical zero to enable the device to output data during synchronous operation. If CS* is a logical one, the D0–D7 pins are forced to a logical zero, and the A0–A7, S0, S1, and WE* inputs are ignored.

During synchronous read operation, the CS* may have the same timing as A0–A7, and is pipelined to maintain synchronization with these signals.

Figure 1 illustrates the read timing for synchronous operation.

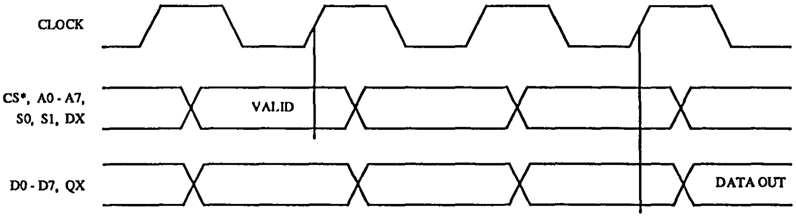


Figure 1. Read Timing (Synchronous Mode).

Circuit Description (continued)

Asynchronous Read/Write Operation

During asynchronous operation, the part may be both written to and read. In this instance, the internal input and output latches for the data and address paths are configured to be transparent.

The S0 and S1 inputs are used to specify whether the MPU is accessing the RAM or one of the overlay registers, as illustrated in Table 1. When accessing the RAM, A0–A7 specify which RAM location is being accessed, otherwise they are ignored.

The WE* input specifies whether the MPU is reading (WE* = 1) or writing (WE* = 0) to the RAM or overlay registers.

Figure 2 illustrates the read timing and Figure 3 illustrates the write timing during asynchronous operation.

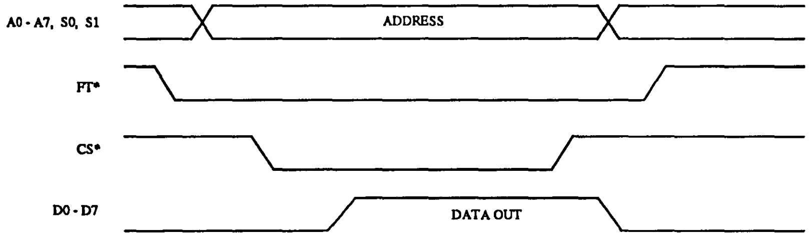


Figure 2. Read Timing (Asynchronous Mode, WE = 1).*

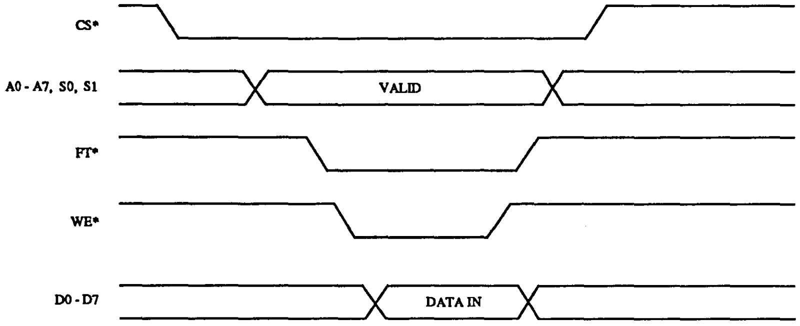
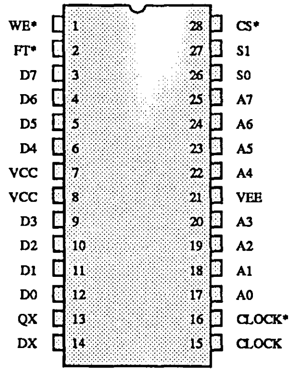


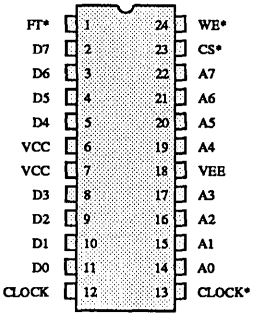
Figure 3. Write Timing (Asynchronous Mode).

Pin Descriptions

Pin Name	Description
CS*	Chip select control input (ECL compatible). A logical zero on this input enables data to be written to or read from the device. A logical one forces the D0–D7 pins to a logical zero. It is latched on the rising edge of CLOCK.
WE*	Write enable control input (ECL compatible). A logical zero on this input enables data to be written into the device. Data is internally latched on the rising edge of WE*. See Figure 1.
D0–D7	Bidirectional data bus (ECL compatible). D0 is the least significant bit. Data is transferred into and out of the device over this eight bit data bus.
FT*	Feedthrough control input (ECL compatible). A logical one configures the device for synchronous operation and a logical zero configures the device for asynchronous operation. Note that the setup and hold times must be met when switching between synchronous and asynchronous operation. While FT* is a logical one, the rising edge of CLOCK latches the CS*, A0–A7, S0, and S1 inputs, and data is output onto D0–D7 following the rising edge of CLOCK. While FT* is a logical zero, the internal latches for these signals are transparent.
CLOCK, CLOCK*	Differential clock inputs (ECL compatible). The device may be driven by a single-ended clock by connecting CLOCK* to VBB (–1.3 V).
A0–A7	Address inputs (ECL compatible). A0–A7 are used to specify which location in the RAM is being accessed, if both S0 and S1 are a logical zero. If either S0 or S1 are a logical one, A0–A7 are ignored. See Table 1.
S0, S1	Select control inputs (ECL compatible). On the Bt401, the S1 and S0 inputs specify whether the RAM or one of the overlay registers is being accessed. S0 and S1 are not incorporated on the Bt403. See Table 1.
DX, QX	Pipe input and output (ECL compatible). The value of the DX input is latched on the rising edge of CLOCK and output onto QX two clock cycles later, regardless of the state of FT*. These are typically used to maintain synchronization of data and control signals. DX and QX are not incorporated on the Bt403.
VEE	Device power. All VEE pins must be connected.
VCC	Device ground. All VCC pins must be connected.


WE* 1
FT* 2
D7 3
D6 4
D5 5
D4 6
VCC 7
VCC 8
D3 9
D2 10
D1 11
D0 12
QX 13
DX 14
28 CS*
27 S1
26 S0
25 A7
24 A6
23 A5
22 A4
21 VEE
20 A3
19 A2
18 A1
17 A0
16 CLOCK*
15 CLOCK

Bt401


FT* 1
D7 2
D6 3
D5 4
D4 5
VCC 6
VCC 7
D3 8
D2 9
D1 10
D0 11
CLOCK 12
24 WE*
23 CS*
22 A7
21 A6
20 A5
19 A4
18 VEE
17 A3
16 A2
15 A1
14 A0
13 CLOCK*

Bt403

Bt401/403—Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	VCC	0	0	0	Volts
Power Supply	VEE	–4.9	–5.2	–5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 liner feet per minute over the device either mounted in the test socket or on the printed circuit board.

Bt401/403—Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (measured to VCC)				–8.0	Volts
Voltage on any Pin (except D0 - D7, QX)		0		VEE	Volts
Output Current				–30	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Bt401/403—DC Characteristics

Parameter	Symbol	TA (°C.)	Min	Typ	Max	Units
Input High Voltage	VIH	0 +25 +70	–1170 –1130 –1070		–840 –810 –735	mV mV mV
Input Low Voltage	VIL	0 +25 +70	–1950 –1950 –1950		–1480 –1480 –1450	mV mV mV
Output High Voltage	VOH	0 +25 +70	–1020 –980 –920		–840 –810 –735	mV mV mV
Output Low Voltage	VOL	0 +25 +70	–1950 –1950 –1950		–1630 –1630 –1600	mV mV mV
Input High Current (Vin = VIHmax)	IIH	0 +25 +70		220 220 220		µA µA µA
Input Low Current (Vin = VILmin)	IIL	0 +25 +70	0.5 0.5 0.5			µA µA µA
VEE Supply Current	IEE	0 +25 +70			280 280 280	mA mA mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with output loading of 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Bt401/403—AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			250	MHz
Read (Synchronous Mode)					
Clock Cycle Time	1	4			ns
Clock Pulse Width High	2	1			ns
Clock Pulse Width Low	3	1			ns
Clock to Output Valid	4			2	ns
Input Setup Time	5	0			ns
Input Hold Time	6	1			ns
Pipeline Delay	7	3	3	3	Clocks
Read (Asynchronous Mode)					
A0–A7 Access Time	8			10	ns
CS* Access Time	9			5	ns
CS* Recovery Time	10			5	ns
FT* Setup Time	11	5			ns
Write (Asynchronous Mode)					
WE* Pulse Width Low	12	75			ns
A0–A7 Setup Time	13	5			ns
A0–A7 Hold Time	14	20			ns
D0–D7 Setup Time	15	55			ns
D0–D7 Hold Time	16	5			ns
CS* Setup Time	17	5			ns
CS* Hold Time	18	5			ns
FT* Setup Time	19	5			ns
FT* Hold Time	20	5			ns
Output Rise/Fall Time			2		ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with output loading of 50 Ω to –2.0 V. ECL input values are –0.89 to –1.69 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Output rise/fall time measured between the 20% and 80% points. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Timing Waveforms

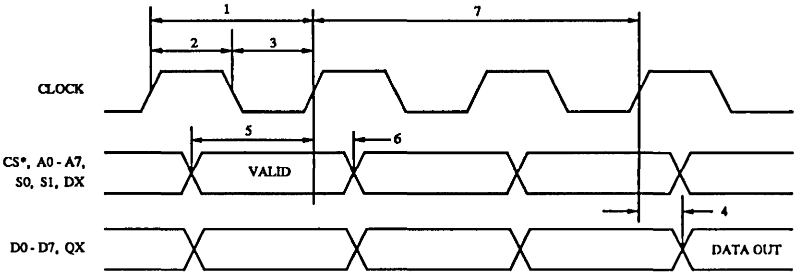

1
7
2
3
CLOCK
5
6
CS*, A0 - A7,
S0, S1, DX
VALID
4
D0 - D7, QX
DATA OUT

Figure 4. Read Timing (Synchronous Mode).

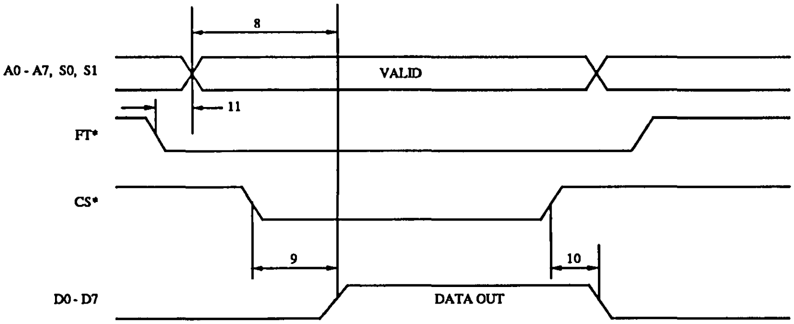

8
A0 - A7, S0, S1
VALID
11
FT*
CS*
9
10
D0 - D7
DATA OUT

Figure 5. Read Timing (Asynchronous Mode, WE = 1).*

Timing Waveforms (continued)

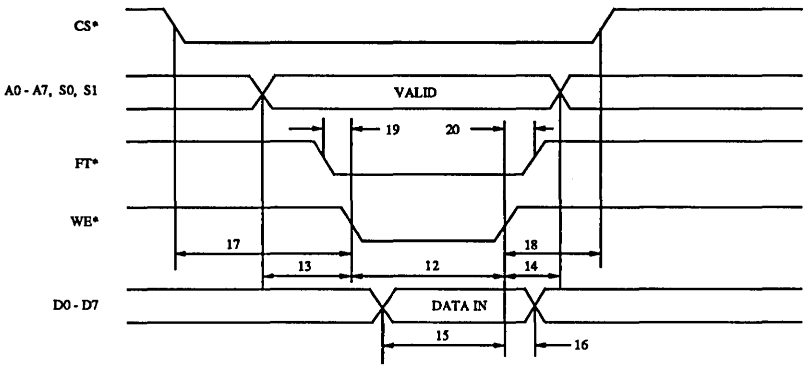

CS*
A0 - A7, S0, S1
VALID
FT*
19
20
WE*
17
18
13
12
14
D0 - D7
DATA IN
15
16

Figure 6. Write Timing (Asynchronous Mode).

Ordering Information

Model Number	Overlays	Compatibility	Package	Ambient Temperature Range
Bt401KC	3 x 8	10KH ECL	28-pin 0.6" CERDIP	0° to +70° C
Bt403KC	none	10KH ECL	24-pin 0.3" CERDIP	0° to +70° C

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt424

250 MHz
40-bit Multi-Tap TTL/ECL-Compatible Video Shift Register

Distinguishing Features

- 250 MHz Operation
- Overlay Support
- TTL Pixel Inputs
- TTL MPU Address Interface
- ECL Shift Register Outputs
- Shift Enable and Output Enable Controls
- Optional Single +5 V Operation
- 68-pin PGA Package with Alignment Pin
- Typical Power Dissipation: 1.25 W

Customer Benefits

- Flexible Power Supply
- Reduced Component Count
- Simplifies PCB Layout
- Reduces PCB Interconnect
- Low Bus Loading
- Increases System Reliability

Configurations

- One 40-bit Shift Register
- Two 16-bit or 20-bit Shift Registers
- Five 8-bit Shift Registers
- Four 10-bit Shift Registers

Related Products

- Bt401/403
- Bt107
- Bt109
- Bt492

Product Description

The Bt424 is a 40-bit multi-tap shift register. It is designed specifically for high-resolution graphics systems.

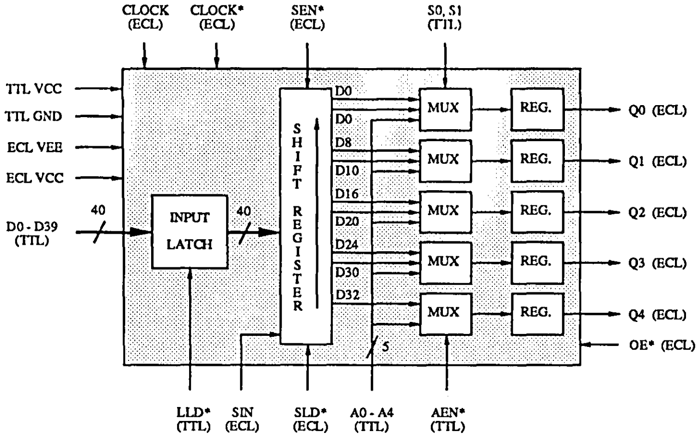
TTL pixel data from the frame buffer is typically loaded at either 1/8 or 1/10 the clock rate (up to about 32 MHz) using the TTL-compatible LLD* signal. Data is then transferred from the input latch to the shift register using the ECL-compatible load signal (SLD*). The double-buffering of incoming pixel data simplifies system timing.

The shift register is clocked by the ECL-compatible CLOCK and CLOCK* inputs, and features ECL-compatible serial input (SIN) and shift enable (SEN*) controls.

The Bt424 performs TTL-to-ECL translation of the MPU address (A0–A4), eliminating external address translators. The MPU address interface enables the MPU address(A0–A4) to be output onto the Q0–Q4 pins, overriding the shift register data. This interface is controlled by the TTL-compatible address enable (AEN*) signal.

The Bt424 has separate TTL and ECL supply pins, enabling operation from a single +5 V supply, or a +5 V and –5.2 V supply.

Functional Block Diagram


CLOCK (ECL)
CLOCK* (ECL)
SEN* (ECL)
S0, S1 (TTL)
TTL VCC
TTL GND
ECL VEE
ECL VCC
40
D0 - D39 (TTL)
INPUT LATCH
40
SHIFT REGISTER
D0
D0
D8
D10
D16
D20
D24
D30
D32
MUX
MUX
MUX
MUX
MUX
REG.
REG.
REG.
REG.
REG.
Q0 (ECL)
Q1 (ECL)
Q2 (ECL)
Q3 (ECL)
Q4 (ECL)
OE* (ECL)
5
LLD* (TTL)
SIN (ECL)
SLD* (ECL)
A0 - A4 (TTL)
AEN* (TTL)

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L424001 Rev. G

Brooktree®

Circuit Description

As illustrated in the functional block diagram, the Bt424 contains a 40-bit input latch, a 40-bit shift register, and control logic.

General Shift Register Operation

The 40-bit shift register has multiple taps, as illustrated in the functional block diagram. As illustrated in Figure 3, on the rising edge of LLD*, D0–D39 are latched into the input latch. Data is transferred from the input latch to the shift register synchronously on the rising edge of CLOCK while SLD* is a logical zero. Note that while LLD* is a logical zero, the input latch is transparent, as illustrated in Figure 4.

The multiplexers select one of two taps from the 40-bit shift register or a MPU address input. The output of the multiplexers are registered synchronously to CLOCK and output onto the Q0–Q4 pins.

The SEN* input may be used to synchronously enable (logical zero) or disable (logical one) the shift register from clocking. This is useful for implementing hardware zooming in a graphics application. Figure 5 shows the shift timing and SEN* timing.

The OE* input is used to enable (logical zero) or disable (logical one) the outputs asynchronously to CLOCK, as shown in Figure 6.

Single 40-bit Shift Register Operation

When used as a 40-bit shift register, only the Q0 output is used, and the Q1–Q4 outputs are ignored. D0 is the first bit output, followed by D1, etc. SLD* and LLD* should occur once every 40 clock cycles. The state of the S0 and S1 inputs is not important, and they may be connected to TTL GND.

Note that single shift registers of any length (up to 40 bits) may be implemented by simply loading the parallel data at the appropriate time. For example, a 32-bit shift register may be implemented by loading parallel data once every 32 clock cycles.

Dual 20-bit Shift Register Operation

When used as a dual 20-bit shift register, only the Q0 and Q2 outputs are used, and the Q1, Q3, and Q4 outputs are ignored. For Q0, D0 is the first bit output, followed by D1, etc. For Q2, D20 is the first bit output, followed by D21, etc. SLD* and LLD* should occur once every 20 clock cycles. S0 and S1 must configure the Bt424 as four 10-bit shift registers.

Dual 16-bit Shift Register Operation

When used as a dual 16-bit shift register, only the Q0 and Q2 outputs are used, and the Q1, Q3, and Q4 outputs are ignored. For Q0, D0 is the first bit output, followed by D1, etc. For Q2, D16 is the first bit output, followed by D17, etc. SLD* and LLD* should occur once every 16 clock cycles. S0 and S1 must configure the Bt424 as five 8-bit shift registers.

Quad 10-bit Shift Register Operation

When used as a quad 10-bit shift register, all output except Q4 are used (which is ignored). For Q0, D0 is the first bit output, followed by D1, etc. For Q1, D10 is the first bit output, followed by D11, etc. For Q2, D20 is the first bit output, followed by D21, etc. For Q3, D30 is the first bit output, followed by D31, etc. SLD* and LLD* should occur once every 10 clock cycles. S0 and S1 must configure the Bt424 as four 10-bit shift registers.

Quint 8-bit Shift Register Operation

When used as a quint 8-bit shift register, all outputs are used. For Q0, D0 is the first bit output, followed by D1, etc. For Q1, D8 is the first bit output, followed by D9, etc. For Q2, D16 is the first bit output, followed by D17, etc. For Q3, D24 is the first bit output, followed by D25, etc. For Q4, D32 is the first bit output, followed by D33, etc. SLD* and LLD* should occur once every eight clock cycles. S0 and S1 must configure the Bt424 as five 8-bit shift registers.

Circuit Description (continued)

MPU Address Interface

The Bt424 accepts TTL-compatible MPU addresses (A0–A4) and translates them to ECL-compatible levels, eliminating the need for external TTL/ECL translators along the address path.

While AEN* is a logical one, pixel data from the shift register is output onto the Q0–Q4 pins. While AEN* is a logical zero, A0–A4 are output onto the Q0–Q4 pins. Figure 7 illustrates the MPU address timing. Note that Q0–Q4 are always output following the rising edge of CLOCK regardless of the value of AEN*.

S0, S1 Select Inputs

S0 and S1 specify the configuration of the Bt424 as shown in Table 1.

S1	S0	Function
0	0	quad 10-bit
x	1	quint 8-bit
1	0	quad 8-bit, 8-bit overlay port

Table 1. S0, S1 Control Inputs.

Figure 1 shows using the Bt424 in a typical graphics system. In this instance, the RAMDAC has separate (nonmultiplexed) pixel and overlay data inputs. Therefore, all three Bt424s are configured for the same mode of operation (either quad 10-bit or quint 8-bit depending on the specific application).

Figure 2 shows a basic configuration using the Bt424 with a RAMDAC that has multiplexed pixel and overlay inputs. The OL input of the RAMDAC specifies whether pixel (OL = 0) or overlay (OL = 1) data is present on P0–P7.

The Bt424s interfaced to bit planes 0–7 are configured to support overlays (S1 = 1, S0 = 0). D0–D7, D8–D15, D16–D23, and D24–D31 are configured as four 8-bit pixel input ports, while D32–D39 are configured as an 8-bit overlay active input port. If D32–D39 contain a logical one on any bit, the Q0–Q3 outputs are disabled and forced to a logical zero, enabling overlay information to be wire-ORed onto the Q0–Q3 outputs.

The Bt424 interfaced to the overlay bit planes is configured as a quint 8-bit shifter, and serializes the overlay information. The Q0–Q3 outputs are wire-ORed onto the pixel data bus to the RAMDAC. The D32–D39 inputs are serialized to generate the overlay enable (OL) control signal for the RAMDAC. Note that if no overlay information is being displayed, the Q0–Q4 outputs are a logical zero, allowing normal pixel data to be displayed.

Eight four-input TTL OR gates are required to generate the overlay active signals to the Bt424s. D0, D8, D16, and D24 are ORed together to generate D32, etc.

Power Supply Operation

The Bt424 may operate from a +5 V and -5.2 V power supply or from a single +5 V power supply, as shown in Table 2.

	Nominal Voltages Applied	
Supply Pin	Single Supply System	Dual Supply System
TTL VCC	+5.0 V	+5.0 V
TTL GND	0 V	0 V
ECL VCC	+5.0 V	0 V
ECL VEE	0 V	–5.2 V

Table 2. Power Supply Operation.

Inputs and outputs are temperature and voltage compensated.

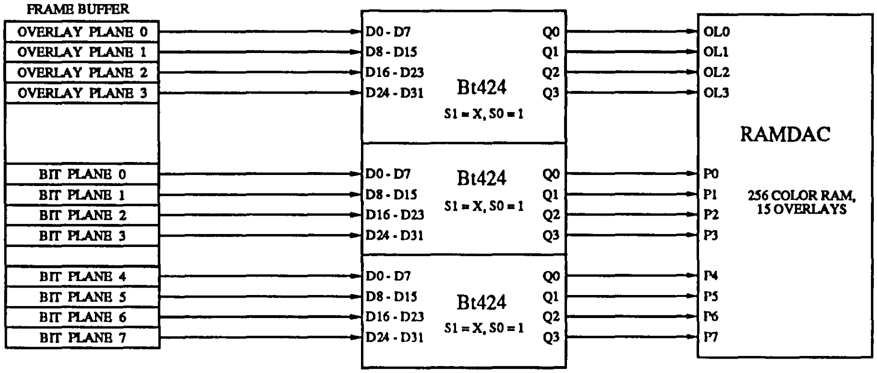

FRAME BUFFER
OVERLAY PLANE 0
OVERLAY PLANE 1
OVERLAY PLANE 2
OVERLAY PLANE 3
BIT PLANE 0
BIT PLANE 1
BIT PLANE 2
BIT PLANE 3
BIT PLANE 4
BIT PLANE 5
BIT PLANE 6
BIT PLANE 7
D0 - D7
D8 - D15
D16 - D23
D24 - D31
Bt424
S1 = X, S0 = 1
Q0
Q1
Q2
Q3
OL0
OL1
OL2
OL3
P0
P1
P2
P3
P4
P5
P6
P7
RAMDAC
256 COLOR RAM, 15 OVERLAYS

Figure 1. Using the Bt424 with Separate Pixel and Overlay Inputs (256 Colors, 15 Overlays).

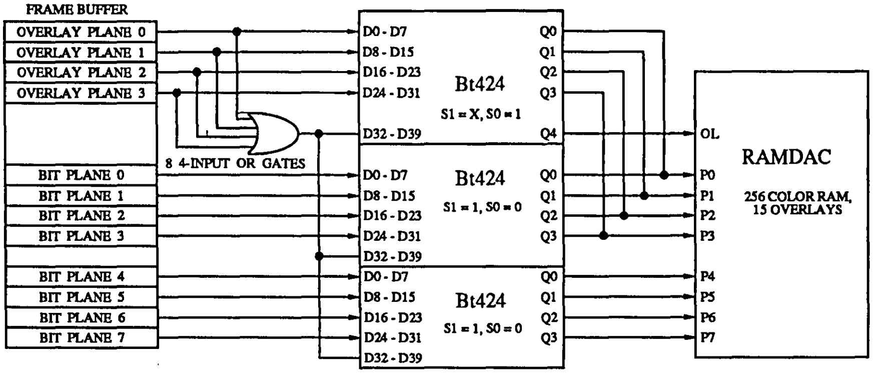

FRAME BUFFER
OVERLAY PLANE 0
OVERLAY PLANE 1
OVERLAY PLANE 2
OVERLAY PLANE 3
BIT PLANE 0
BIT PLANE 1
BIT PLANE 2
BIT PLANE 3
BIT PLANE 4
BIT PLANE 5
BIT PLANE 6
BIT PLANE 7
8 4-INPUT OR GATES
D0 - D7
D8 - D15
D16 - D23
D24 - D31
D32 - D39
Bt424
S1 = X, S0 = 1
S1 = 1, S0 = 0
Q0
Q1
Q2
Q3
Q4
OL
P0
P1
P2
P3
P4
P5
P6
P7
RAMDAC
256 COLOR RAM, 15 OVERLAYS

Figure 2. Using the Bt424 with Multiplexed Pixel/Overlay Inputs (256 Colors, 15 Overlays).

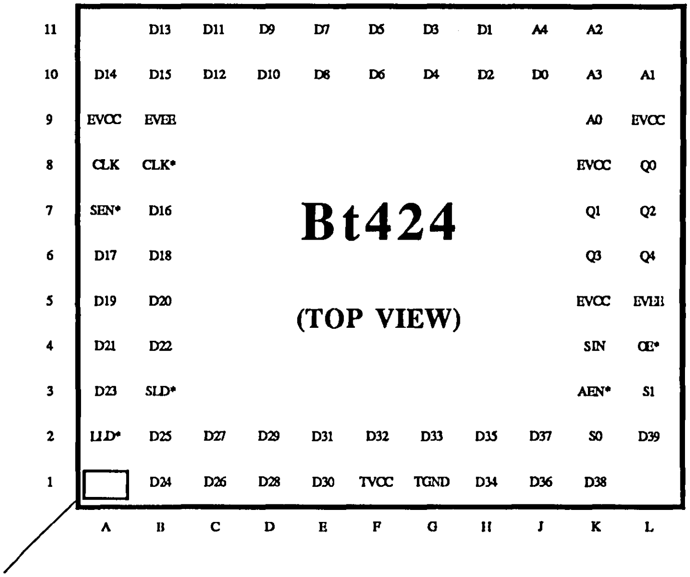
Pin Descriptions

Pin Name	Description
D0–D39	Parallel data inputs (TTL compatible). These inputs are latched into the input latch on the rising edge of LLD*, asynchronous to CLOCK.
SIN	Shift data input (ECL compatible). This input is latched on the rising edge of CLOCK, and may be used to serially load the shift register. If not used, it should be connected to ECL GND.
SEN*	Shift enable control input (ECL compatible). This input may be used to synchronously start or stop the shift register from clocking. A logical zero enables shifting, and a logical one disables shifting.
LLD*	Input latch load control input (TTL compatible). The rising edge of LLD* is used to latch D0–D39 into the input latch. While LLD* is a logical zero, the input latch is transparent.
SLD*	Shift register load control input (ECL compatible). SLD* is used to transfer data from the input latch to the shift register synchronously to CLOCK. Data is transferred on the rising edge of CLOCK while SLD* is a logical zero.
CLOCK, CLOCK*	Differential clock inputs (ECL compatible). The clock rate is typically the pixel clock rate of the video system. The Bt424 may be used with a single-ended clock by connecting CLOCK* to VBB (–1.3 V)
Q0–Q4	Shift register outputs (ECL compatible). These pins output either D0–D39 data (AEN* = logical one) or A0–A4 data (AEN* = logical zero). Data is output following the rising edge of CLOCK.
OE*	Output enable control input (ECL compatible). A logical one forces the Q0–Q4 outputs to a logical zero, while a logical zero enables data to be output onto Q0–Q4. The Q0–Q4 outputs are enabled and disabled asynchronously to CLOCK.
S0, S1	Select control inputs (TTL compatible). These inputs control the operation of the device as specified in Table 1.
A0–A4	Address inputs (TTL compatible). These are typically address inputs from the MPU, used to address the color palette RAM during MPU read/write cycles to the color palette RAM.
AEN*	Address enable control input (TTL compatible). While AEN* is a logical zero, A0–A4 are output onto Q0–Q4 following the rising edge of CLOCK. If AEN* is a logical one, A0–A4 are ignored.
TTL VCC	Power supply pins for the TTL-compatible circuitry.
TTL GND	Ground pins for the TTL-compatible circuitry.
ECL VEE	Power supply pins for the ECL-compatible circuitry.
ECL VCC	Ground pins for the ECL-compatible circuitry.

Pin Descriptions (continued)

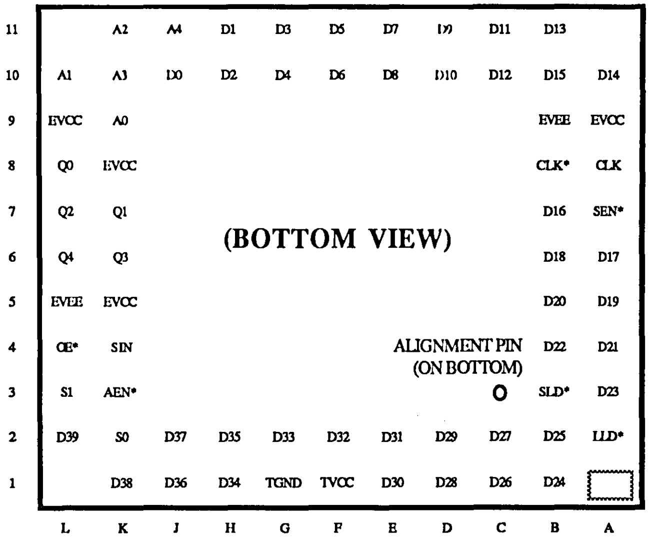
Signal	Pin Number	Signal	Pin Number	Signal	Pin Number
CLOCK	A8	D0	J10	D25	B2
CLOCK*	B8	D1	H11	D26	C1
		D2	H10	D27	C2
LLD*	A2	D3	G11	D28	D1
SLD*	B3	D4	G10	D29	D2
SEN*	A7				
SIN	K4	D5	F11	D30	E1
S0	K2	D6	F10	D31	E2
S1	L3	D7	E11	D32	F2
		D8	E10	D33	G2
AEN*	K3	D9	D11	D34	H1
A0	K9				
A1	L10	D10	D10	D35	H2
A2	K11	D11	C11	D36	J1
A3	K10	D12	C10	D37	J2
A4	J11	D13	B11	D38	K1
		D14	A10	D39	L2
Q0	L8				
Q1	K7	D15	B10	TTL VCC	F1
Q2	L7	D16	B7		
Q3	K6	D17	A6	TTL GND	G1
Q4	L6	D18	B6		
		D19	A5	ECL VEE	B9
OE*	L4			ECL VEE	L5
		D20	B5		
		D21	A4	ECL VCC	A9
		D22	B4	ECL VCC	K5
		D23	A3	ECL VCC	K8
		D24	B1	ECL VCC	L9

Pin Descriptions (continued)



	A	B	C	D	E	F	G	H	J	K	L
11		D13	D11	D9	D7	D5	D3	D1	A4	A2	
10	D14	D15	D12	D10	D8	D6	D4	D2	D0	A3	A1
9	EVCC	EVEE								A0	EVCC
8	CLK	CLK*								EVCC	Q0
7	SEN*	D16								Q1	Q2
6	D17	D18								Q3	Q4
5	D19	D20								EVCC	EVEE
4	D21	D22								SIN	OE*
3	D23	SLD*								AEN*	S1
2	LLD*	D25	D27	D29	D31	D32	D33	D35	D37	S0	D39
1		D24	D26	D28	D30	TVCC	TGND	D34	D36	D38	

alignment marker (on top)



	L	K	J	H	G	F	E	D	C	B	A
11		A2	A4	D1	D3	D5	D7	D9	D11	D13	
10	A1	A3	D0	D2	D4	D6	D8	D10	D12	D15	D14
9	EVCC	A0								EVEE	EVCC
8	Q0	EVCC								CLK*	CLK
7	Q2	Q1								D16	SEN*
6	Q4	Q3								D18	D17
5	EVEE	EVCC								D20	D19
4	OE*	SIN								D22	D21
3	S1	AEN*							O	SLD*	D23
2	D39	S0	D37	D35	D33	D32	D31	D29	D27	D25	LLD*
1		D38	D36	D34	TGND	TVCC	D30	D28	D26	D24	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
TTL Device Ground	TTL GND	0	0	0	Volts
ECL Device Ground	ECL VCC	0	0	0	Volts
TTL Power Supply	TTL VCC	+4.75	+5.0	+5.25	Volts
ECL Power Supply	ECL VEE	–4.2	–5.2	–5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
ECL VEE (measured to ECL VCC)				–8.0	Volts
TTL VCC (measured to TTL GND)				+7.0	Volts
Voltage on Any ECL Pin		0		ECL VEE	Volts
Voltage on Any TTL Pin		TTL GND –0.5		TTL VCC +0.5	Volts
Q0–Q4 Output Current				–30	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ECL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage*	VIH	–1165		–880	mV
Input Low Voltage*	VIL	–1810		–1475	mV
Output High Voltage*	VOH	–1025		–880	mV
Output Low Voltage*	VOL	–1810		–1620	mV
Input High Current (Vin = VIHmax)	IIH			500	µA
Input Low Current (Vin = VILmin)	IIL			400	µA
ECL VEE Supply Current	IEE			240	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with Q0–Q4 loading of 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Relative to ECL VCC.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

TTL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage*	VIH	2.0		TTL VCC +0.5	Volts
Input Low Voltage*	VIL	TTL GND –0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			70	µA
Input Low Current (Vin = 0.4 V)	IIL			–0.7	mA
TTL VCC Supply Current	ICC			100	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with Q0–Q4 loading of 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Relative to TTL GND.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate	Fmax			250	MHz
Clock Cycle Time	1	4			ns
Clock Pulse Width High Time	2	1.5			ns
Clock Pulse Width Low Time	3	1.5			ns
LLD* Pulse Width Low Time	4	7			ns
LLD* Setup Time	5	8			ns
SLD Setup Time	6	2			ns
SLD Hold Time	7	1			ns
D0–D39 Setup Time to LLD*	8	10			ns
D0–D39 Setup Time to Clock	9	15			ns
D0–D39 Hold Time to LLD*	10	0			ns
D0–D39 Hold Time to Clock	11	0			ns
Q0–Q4 Output Delay	12	1.5		4	ns
SEN* Setup Time	13	2			ns
SEN* Hold Time	14	1			ns
SIN Setup Time	15	2.5			ns
SIN Hold Time	16	1.5			ns
OE* Pulse Width Low Time	17	4			ns
OE* Enable Time	18			3.5	ns
OE* Disable Time	19			4	ns
A0–A4 Setup Time	20	12			ns
A0–A4 Hold Time	21	0			ns
AEN* Setup Time	22	5			ns
AEN* Hold Time	23	0			ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with Q0–Q4 loading of 50 Ω to –2.0 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are –0.89 to –1.69 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt424KG	68-pin Ceramic PGA with Alignment Pin	0° to +70° C

Timing Waveforms

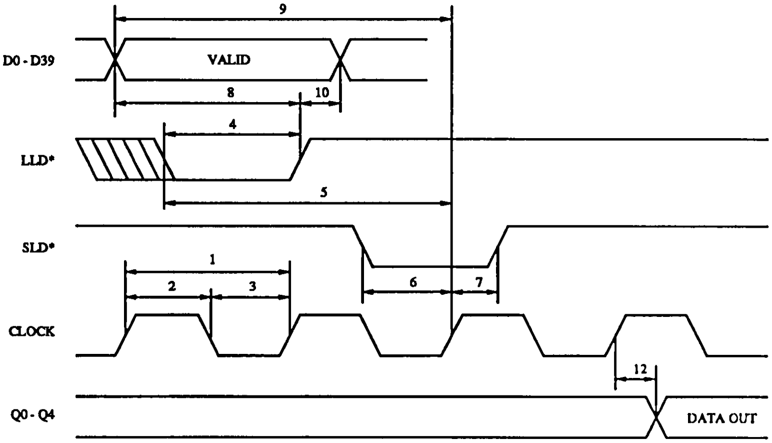

9
D0 - D39
VALID
8
10
4
LLD*
5
SLD*
1
2
3
6
7
CLOCK
12
Q0 - Q4
DATA OUT

Figure 3. Load Latch and Register Timing.

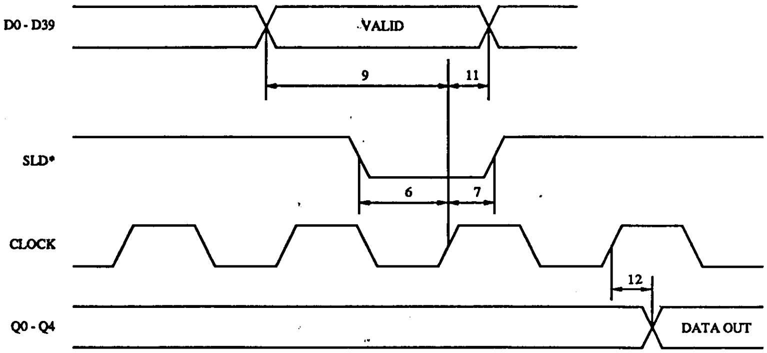

D0 - D39
VALID
9
11
SLD*
6
7
CLOCK
12
Q0 - Q4
DATA OUT

Figure 4. Transparent Latch Timing (LLD = Logical Zero).*

Timing Waveforms (continued)

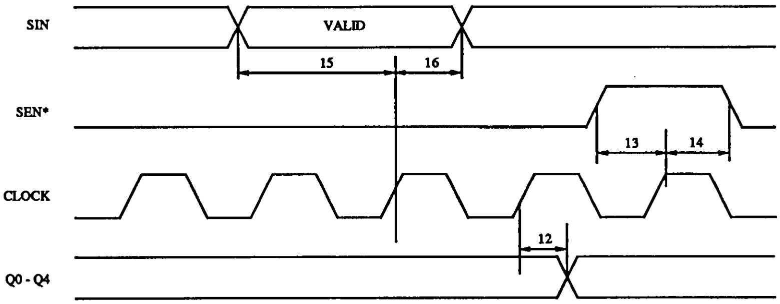

SIN
VALID
15
16
SEN*
13
14
CLOCK
12
Q0 - Q4

Figure 5. Shift Timing (SLD = Logical One).*

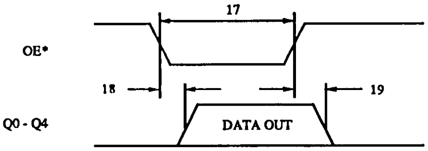

17
OE*
18
19
Q0 - Q4
DATA OUT

Figure 6. Output Enable Timing.

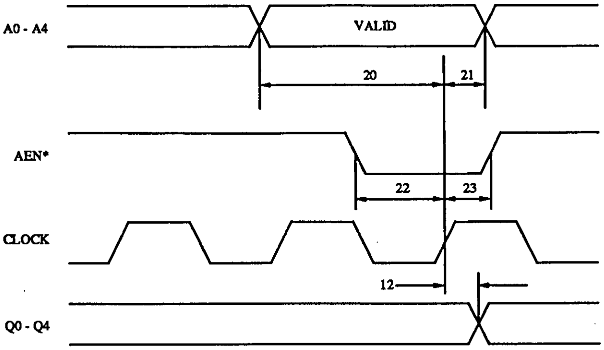

A0 - A4
VALID
20
21
AEN*
22
23
CLOCK
12
Q0 - Q4

Figure 7. Address Enable Timing.

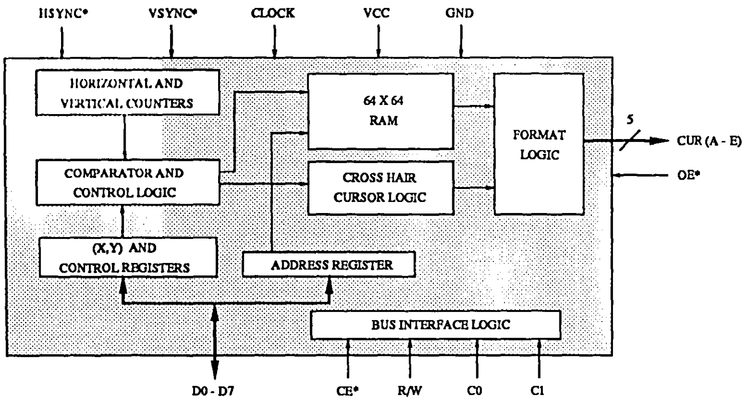
Bt431

Monolithic CMOS
64 x 64 Pixel
Cursor Generator

Distinguishing Features

- 64 x 64 Pixel User-Definable Cursor
- Full-Screen/Window Cross Hair Cursor
- Pixel Positioning of Cursors
- Supports Pixel Rates up to 175 MHz
- 1:1, 4:1, and 5:1 Output Multiplexing
- TTL-Compatible Inputs/Outputs
- Standard MPU Interface
- +5 V CMOS Monolithic Construction
- 24-pin 0.3" DIP or 28-pin PLCC Package
- Typical Power Dissipation: 450 mW

Functional Block Diagram


HSYNC*
VSYNC*
CLOCK
VCC
GND
HORIZONTAL AND VERTICAL COUNTERS
64 X 64 RAM
FORMAT LOGIC
5
CUR (A - E)
OE*
COMPARATOR AND CONTROL LOGIC
CROSS HAIR CURSOR LOGIC
(X,Y) AND CONTROL REGISTERS
ADDRESS REGISTER
BUS INTERFACE LOGIC
D0 - D7
CE*
R/W
C0
C1

Applications

- High-Resolution Color Graphics
- Image Processing

Customer Benefits

- Reduces Component Count
- Reduces PCB Area Requirements
- Simplifies Cursor Implementation
- Allows Fast Cursor Movement
- Simplifies Software Interface

Product Description

The Bt431 cursor generator provides a 64 x 64 pixel user-definable cursor and a cross hair cursor for high-resolution, noninterlaced, monochrome or color graphics systems. The cross hair cursor may be implemented as a full-screen or full-window cross hair cursor. Both cursors may be displayed simultaneously, with logical OR and exclusive-OR operations supported. Either cursor may be moved off the top, bottom, left, or right side of the display without wrap-around.

The cursors may be positioned with pixel resolution, and may be individually enabled or disabled from being displayed. A standard MPU bus interface is supported, simplifying system design.

The Bt431 may be programmed to output cursor information for one, four, or five horizontally consecutive pixels, enabling it to be interfaced to either the multiplexed or nonmultiplexed overlay inputs of Brooktree RAMDACs.

The 5:1 output multiplex mode enables support of pixel rates up to 175 MHz.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L431001 Rev. J

Brooktree®

Circuit Description

MPU Interface

As illustrated in the functional block diagram, the Bt431 supports a standard MPU bus interface, allowing the MPU direct access to the internal control registers and cursor RAM.

The MPU interface signals consist of D0–D7, CE*, R/W, C0, and C1. Table 1 illustrates the truth table for the control inputs, and Figure 1 illustrates the MPU read/write timing of the device.

Two 8-bit address registers (address register0 and address register1), cascaded to form a 16-bit address pointer register, are used to address the internal control registers and cursor RAM, as illustrated in Table 2. During read/write cycles to the cursor RAM, the 9 least significant bits of the address pointer register (ADDR0–ADDR8) are incremented following each read or write cycle to the cursor RAM. Thus, the MPU may load the address pointer register with the desired starting cursor RAM address, and burst load new cursor RAM data by writing up to 512 bytes of data to the device. Following a read or write cycle to RAM location $01FF, the address pointer register resets to $0000.

During accesses to the control registers, ADDR0–ADDR8 are incremented after any read or write cycle to a register. While accessing the control registers, the address pointer register will reset to $0000 only following a write cycle to location $01FF. The address register is not incremented when read or written to.

RAMDAC Interface

The Bt431 is designed to generate cursor information using the overlay input ports of Brooktree RAMDACs.

The Bt431 may be interfaced directly to RAMDACs with 4:1 or 5:1 multiplexed overlay ports, supporting display resolutions up to 1280 x 1024 pixels. In this instance, the CUR (A–E) outputs of the Bt431 would connect directly to the overlay inputs of the RAMDAC, and the CLOCK input of the Bt431 would typically be connected directly to the LD* or LDOUT pin of the RAMDAC. The Bt431 must be programmed to output either four or five horizontally consecutive pixels of cursor information each CLOCK cycle. This enables the Bt431 to output cursor information at an effective 175 MHz rate (using 5:1 mode).

To support RAMDACs with nonmultiplexed overlay inputs, the Bt431 may be programmed to output a single pixel of cursor information each CLOCK cycle. In this configuration, the CURA output of the Bt431 would connect directly to one of the overlay inputs of the RAMDAC. This configuration limits the cursor information to an effective 35 MHz rate. The CLOCK input of the Bt431 is typically connected directly to the CLOCK input of the RAMDAC.

The Bt431 may be configured for 4:1 or 5:1 output multiplexing, and an external shift register used (with appropriate control logic) to interface to RAMDACs whose input pixel rate is greater than 35 MHz. In this configuration, the CLOCK must be driven at 1/4 or 1/5 the pixel clock rate. Pixel rates up to 175 MHz may be supported using this technique.

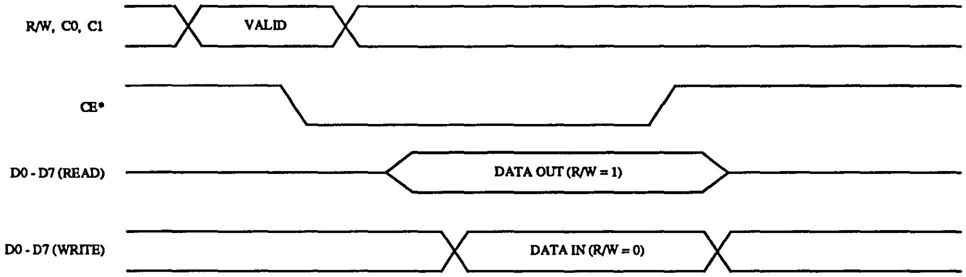


Figure 1. MPU Read/Write Timing.

Circuit Description (continued)

R/W	C1	C0	
0	0	0	write address register0
0	0	1	write address register1
0	1	0	write to RAM location specified by address pointer register
0	1	1	write to control register specified by address pointer register
1	0	0	read address register0
1	0	1	read address register1
1	1	0	read RAM location specified by address pointer register
1	1	1	read control register specified by address pointer register

Table 1. MPU Control Truth Table.

	Address Pointer Register (ADDR15–ADDR0)		
C0	Address Register1 (D7–D0)	Address Register0 (D7–D0)	Register/RAM location addressed
0	0000 0000	0000 0000	cursor RAM location $000
0	0000 0000	0000 0001	cursor RAM location $001
:	:	:	:
0	0000 0000	1111 1111	cursor RAM location $0FF
0	0000 0001	0000 0001	cursor RAM location $100
0	0000 0001	0000 0001	cursor RAM location $101
:	:	:	:
0	0000 0001	1111 1111	cursor RAM location $1FF
1	xxxx xxxx	xxxx 0000	command register
1	xxxx xxxx	xxxx 0001	cursor (x) low register
1	xxxx xxxx	xxxx 0010	cursor (x) high register
1	xxxx xxxx	xxxx 0011	cursor (y) low register
1	xxxx xxxx	xxxx 0100	cursor (y) high register
1	xxxx xxxx	xxxx 0101	window (x) low register
1	xxxx xxxx	xxxx 0110	window (x) high register
1	xxxx xxxx	xxxx 0111	window (y) low register
1	xxxx xxxx	xxxx 1000	window (y) high register
1	xxxx xxxx	xxxx 1001	window width low register
1	xxxx xxxx	xxxx 1010	window width high register
1	xxxx xxxx	xxxx 1011	window height low register
1	xxxx xxxx	xxxx 1100	window height high register

Table 2. Address Pointer Register.

Circuit Description (continued)

64 x 64 Cursor Positioning

When the cursor RAM is being displayed, the contents of the cursor RAM are output onto the CUR (A–E) outputs. A logical one in the cursor RAM results in a logical one being output onto the appropriate CUR (A–E) output during the appropriate clock cycle. The cursor pattern may be changed by changing the contents of the cursor RAM. (See Figure 2.)

The 64 x 64 cursor is centered about the value specified by the cursor (x,y) register. Thus, the cursor (x) register specifies the location of the 31st column of the 64 x 64 RAM (assuming the columns start with 0 for the left-most pixel and increment to 63). Similarly, the cursor (y) register specifies the location of the 31st row of the 64 x 64 RAM (assuming the rows start with 0 for the top-most pixel and increment to 63).

Note that the Bt431 expects (x) to increase going right, and (y) to increase going down, as seen on the display screen.

The cursor (x) position is relative to the first rising edge of CLOCK following the falling edge of HSYNC*. The software must take into account the internal pipeline delays, the amount of skew between the output cursor data and external pixel data, and whether 1:1, 4:1, or 5:1 output multiplexing is being done.

The cursor (y) position is relative to the first falling edge of HSYNC* that is at two or more clock cycles after the falling edge of VSYNC*. (See Figure 2.)

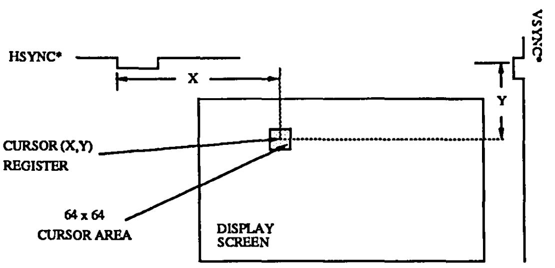


Figure 2. 64 x 64 Cursor Positioning.

Circuit Description (continued)

Cross Hair Cursor Positioning

Cursor positioning for the cross hair cursor is also done through the cursor (x,y) register. (See Figure 3.)

The intersection of the cross hair cursor is specified by the cursor (x,y) register. If the thickness of the cross hair cursor is greater than one pixel, the center of the intersection is the reference position.

During times that cross hair cursor information is to be displayed, a logical one is output onto the appropriate CUR (A–E) output during the appropriate clock cycle.

The cross hair cursor is limited to being displayed within the cross hair window, which is specified by the window (x,y), window width, and window height registers. Since the cursor (x,y) register must specify a point within the window boundaries, **it is the responsibility of the software to ensure that the cursor (x,y) register does not specify a point outside of the cross hair cursor window.**

If a full-screen cross hair cursor is desired, the window (x,y) registers should contain $0000 and the window width and height registers should contain $0FFF.

Again, the cursor (x) position is relative to the first rising edge of CLOCK following the falling edge of HSYNC*. The software must take into account the internal pipeline delays, the amount of skew between the output cursor data and the external pixel data, and whether 1:1, 4:1, or 5:1 output multiplexing is being done.

The cursor (y) position is relative to the first falling edge of HSYNC* that is two or more clock cycles after the falling edge of VSYNC*.

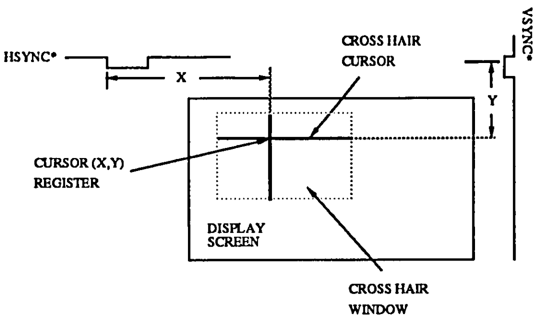


Figure 3. Cross Hair Cursor Positioning.

Circuit Description (continued)

Dual Cursor Positioning

Both the 64 x 64 cursor and the cross hair cursor may be enabled for display simultaneously, enabling the generation of custom cross hair cursors.

During the 64 x 64 pixel area in which the user-definable cursor would be displayed, the contents of the cursor RAM may be logically ORed or exclusive-ORed with the cross hair cursor information.

As previously mentioned, the cursor (x,y) register specifies the location of bit (31,31) of the cursor RAM. As the user-definable cursor contains an even number of pixels in the horizontal and vertical direction, there will be a one-pixel offset from being truly centered about the cross hair cursor.

Figure 4 illustrates displaying the dual cursors, and Figure 5 illustrates the video input/output timing of the Bt431.

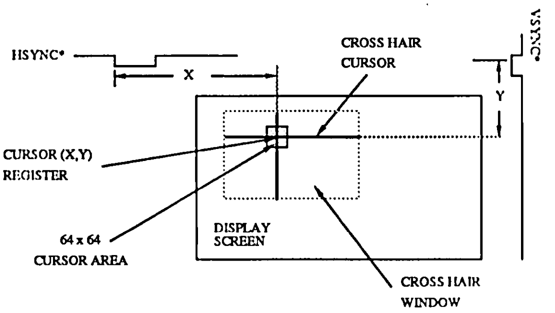

HSYNC*
X
CROSS HAIR CURSOR
VSYNC*
Y
CURSOR (X,Y) REGISTER
64 x 64 CURSOR AREA
DISPLAY SCREEN
CROSS HAIR WINDOW

Figure 4. Dual Cursor Positioning.

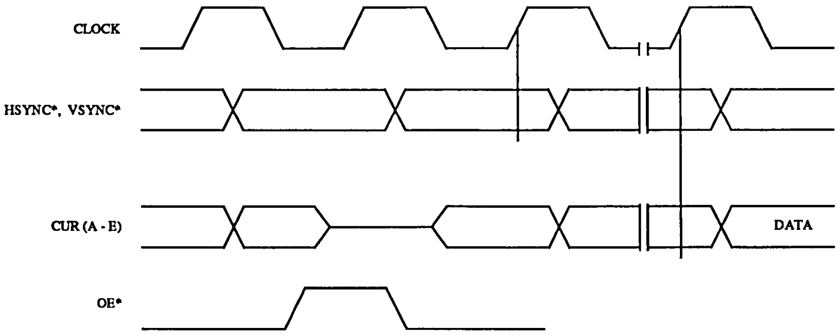

CLOCK
HSYNC*, VSYNC*
CUR (A - E)
DATA
OE*

Figure 5. Video Input/Output Timing.

Internal Registers

Cursor (x,y) Register

These registers are used to specify the (x,y) coordinate of the center of the 64 x 64 pixel cursor window, or the intersection of the cross hair cursor. The cursor (x) register is made up of the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register is made up of the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). They are not initialized and may be written to or read by the MPU at any time.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are always a logical zero.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Cx = desired display screen (x) position + D + H–P

where

P = 37 if 1:1 output multiplexing, 52 if 4:1 output multiplexing, 57 if 5:1 output multiplexing
D = skew (in pixels) between the output cursor data and external pixel data
H = number of pixels between the first rising edge of CLOCK following the falling edge of HSYNC* to active video.

The P value is 1/2 cursor RAM width + (internal pipeline delay in clock cycles * 1, 4, or 5 depending on multiplex selection)

Values from $0000 to $0FFF may be written into the cursor (x) register.

Internal Registers (continued)

The cursor (y) value to be written is calculated as follows:

Cy = desired display screen (y) position + V–32

where

V = number of scan lines from the first falling edge of HSYNC* that is two or more clock cycles after the falling edge of VSYNC* to active video.

Values from $0FC0 (–64) to $0FBF (+4031) may be loaded into the cursor (y) register. The negative values ($0FC0 to $0FFF) are used in situations where V < 32, and the cursor must be moved off the top of the screen.

The cursor (x,y) registers should be written to only during the vertical retrace interval. Note that a falling edge of VSYNC* should not occur between the time the MPU writes the first byte of (x,y) and the last (fourth) byte of (x,y) information. Otherwise, temporary "tearing" of the cursor may occur.

Internal Registers (continued)

Cursor RAM

This 64 x 64 RAM is used to define the pixel pattern within the 64 x 64 pixel cursor window. It is not initialized, and may be written to or read by the MPU at any time. As MPU accesses to the cursor RAM have priority over the cursor display process, the cursor RAM should not be accessed during the horizontal sync intervals to minimize contention of the cursor updating and displaying processes.

During MPU accesses to the cursor RAM, the address pointer register is used to address the cursor RAM, as illustrated below. Figure 6 illustrates the internal format of the cursor RAM, as it appears on the display screen.

Address Pointer Register Value	Address RAM Location
$0000	byte $000
$0001	byte $001
:	:
$01FF	byte $1FF

As shown below, bit D7 is the left-most pixel within a segment of eight pixels. This enables the software generation of cursor patterns without bit swapping to obtain the desired pattern.

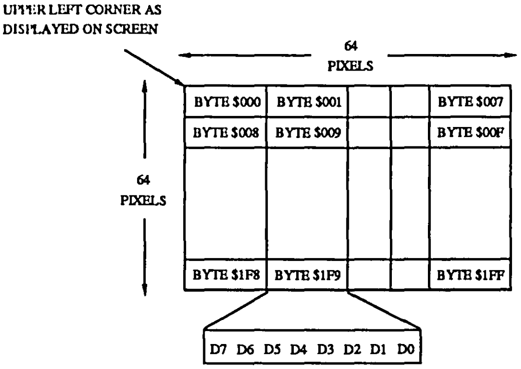

UPPER LEFT CORNER AS DISPLAYED ON SCREEN
64 PIXELS
64 PIXELS
BYTE $000
BYTE $001
BYTE $007
BYTE $008
BYTE $009
BYTE $00F
BYTE $1F8
BYTE $1F9
BYTE $1FF
D7 D6 D5 D4 D3 D2 D1 D0

Figure 6. Cursor RAM as Displayed on the Screen.

Internal Registers (continued)

Window (x,y) Register

These registers are used to specify the (x,y) coordinate of the upper left corner of the cross hair cursor window. The window (x) register is made up of the window (x) low register (WXLR) and the window (x) high register (WXHR); the window (y) register is made up of the window (y) low register (WYLR) and the window (y) high register (WYHR). They are not initialized and may be written to or read by the MPU at any time.

WXLR and WXHR are cascaded to form a 12-bit window (x) register. Similarly, WYLR and WYHR are cascaded to form a 12-bit window (y) register. Bits D4–D7 of WXHR and WYHR are always a logical zero.

	Window (x) High (WXHR)				Window (x) Low (WXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window (y) High (WYHR)				Window (y) Low (WYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The window (x) value to be written is calculated as follows:

$$Wx = \text{desired display screen (x) position} + D + H - P$$

where

P = 5 if 1:1 output multiplexing, 20 if 4:1 output multiplexing, 25 if 5:1 output multiplexing
D = skew (in pixels) between the output cursor data and external pixel data
H = number of pixels between the first rising edge of CLOCK following the falling edge of HSYNC* to active video.

The P value is the number of internal pipeline delays times 1, 4, or 5 depending on the multiplex selection.

The window (y) value to be written is calculated as follows:

$$Wy = \text{desired display screen (y) position} + V$$

where

V = number of scan lines from the first falling edge of HSYNC* that is two or more clock cycles after the falling edge of VSYNC* to active video.

Values from $0000 to $0FFF may be written to the window (x) and window (y) registers. A full-screen cross hair cursor is implemented by loading the window (x,y) registers with $0000 and the window width and height registers with $0FFF.

The window (x,y) registers should be written to only during the vertical retrace interval. Note that a falling edge of VSYNC* should not occur between the time the MPU writes the first byte of (x,y) and the last (fourth) byte of (x,y) information. Otherwise, temporary repositioning of the cross hair cursor may occur.

Internal Registers (continued)

Window Width and Height Registers

These registers are used to specify the width and height (in pixels) of the cross hair cursor window. The window width register is made up of the window width low register (WWLR) and the window width high register (WWHR); the window height register is made up of the window height low register (WHLR) and the window height high register (WHHR). They are not initialized and may be written to or read by the MPU at any time.

WWLR and WWHR are cascaded to form a 12-bit window width register. Similarly, WHLR and WHHR are cascaded to form a 12-bit window height register. Bits D4–D7 of WWHR and WHHR are always a logical zero.

	Window Width High (WWHR)				Window Width Low (WWLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Window Height High (WHHR)				Window Height Low (WHLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The actual window width is 2, 8, or 10 pixels more than the value specified by the window width register, depending on whether 1:1, 4:1, or 5:1 output multiplexing is specified. The actual window height is 2 pixels more than the value specified by the window height register. Therefore, the minimum window width is 2, 8, or 10 pixels, for 1:1, 4:1, and 5:1 multiplexing, respectively, and the minimum window height is 2 pixels.

Values from $0000 to $0FFF may be written to the window width and height registers.

The window width and height registers should be written to only during the vertical retrace interval. Note that a falling edge of VSYNC* should not occur between the time the MPU writes the first byte and the last (fourth) byte of information. Otherwise, temporary "resizing" of the cross hair cursor may occur.

Internal Registers (continued)

Command Register

The command register is used to control various functions of the Bt431. It is not initialized, and may be written to or read by the MPU at any time.

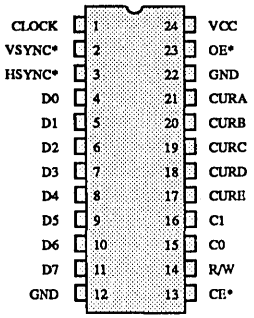
D7	Reserved. This bit should always be a logical zero.
D6	64 x 64 cursor enable. A logical one enables the contents of the cursor RAM to be output during times that user-definable cursor information is to be displayed. A logical zero disables the cursor RAM information from being output.
D5	Cross hair cursor enable. A logical one enables cross hair cursor information to be output. A logical zero disables the cross hair cursor information from being output.
D4	Cursor format control. If both the 64 x 64 cursor and the cross hair cursor are enabled for display, this bit specifies whether the contents of the cursor RAM are to be logically exclusive-ORed (logical zero) or ORed (logical one) with the cross hair cursor.
D3, D2	Multiplex control. These 2 bits specify whether 1, 4, or 5 bits of cursor information are output every clock cycle, as follows: (00) 1:1 multiplexing (01) 4:1 multiplexing (10) 5:1 multiplexing (11) reserved
D1, D0	Cross hair cursor thickness. These 2 bits specify whether the horizontal and vertical thickness of the cross hair is 1, 3, 5, or 7 pixels, as follows: (00) 1 pixel (01) 3 pixels (10) 5 pixels (11) 7 pixels The horizontal and vertical segments are centered about the value in the cursor (x,y) register.

Pin Descriptions

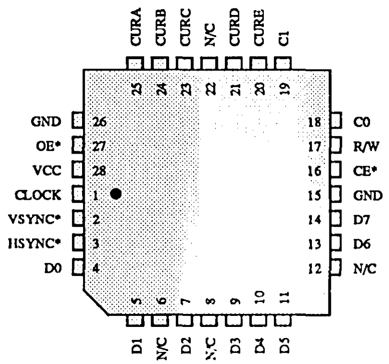
Pin Name	Description
VSYNC*	Vertical sync control input (TTL compatible). A logical zero indicates that the display is currently in the vertical sync interval. It is latched on the rising edge of CLOCK.
HSYNC*	Horizontal sync control input (TTL compatible). A logical zero indicates that the display is currently in the horizontal sync interval. It is latched on the rising edge of CLOCK.
CLOCK	Clock input (TTL compatible). The rising edge of CLOCK is used to latch the VSYNC* and HSYNC* inputs, and to output cursor information onto the CUR (A–E) outputs. It is recommended that the CLOCK input be driven by a dedicated TTL buffer. If programmed for 1:1 output multiplexing, CLOCK should be the pixel clock rate. When programmed for 4:1 or 5:1 output multiplexing, CLOCK should be 1/4 or 1/5 the pixel clock rate, respectively.
CUR (A–E)	Cursor outputs (TTL compatible). During the pixel times that cursor information is to be displayed, either cross hair cursor information or the contents of the cursor RAM are output onto these pins. If programmed for 4:1 output multiplexing, the CURE output will always be a logical zero. If programmed for 1:1 output multiplexing, the CURB, CURC, CURD, and CURE outputs will always be a logical zero. When programmed for 4:1 or 5:1 multiplexing, CURA corresponds to the left-most pixel, followed by CURB, etc., repeating every four or five pixels.
OE*	Output enable control input (TTL compatible). A logical one asynchronously three-states the CUR (A–E) outputs, and a logical zero asynchronously enables cursor data to be output on the cursor outputs.
R/W	Read/write control input (TTL compatible). A logical zero indicates that the MPU is writing data to the device and a logical one indicates that the MPU is reading data from the device. See Figure 1.
CE*	Chip enable control input (TTL compatible). This input must be a logical zero to enable data to be written to or read from the device. During write operations, data is internally latched on the rising edge of CE*. See Figure 1.
C0, C1	Control inputs (TTL compatible). These inputs specify the operation the MPU is performing. See Tables 1 and 2.
D0–D7	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
VCC	Power.
GND	Ground.

Pin Descriptions (continued)

24-pin DIP Package


CLOCK 1
VSYNC* 2
HSYNC* 3
D0 4
D1 5
D2 6
D3 7
D4 8
D5 9
D6 10
D7 11
GND 12
24 VCC
23 OE*
22 GND
21 CURA
20 CURB
19 CURC
18 CURD
17 CURE
16 C1
15 C0
14 R/W
13 CE*

28-pin Plastic J-Lead (PLCC) Package


CURA 25
CURB 24
CURC 23
N/C 22
CURD 21
CURE 20
C1 19
GND 26
OE* 27
VCC 28
CLOCK 1
VSYNC* 2
HSYNC* 3
D0 4
18 C0
17 R/W
16 CE*
15 GND
14 D7
13 D6
12 N/C
5 D1
6 N/C
7 D2
8 N/C
9 D3
10 D4
11 D5

Note: N/C pins may be left floating without affecting the performance of the Bt431.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. Avoid power decoupling networks with large time constants, which could delay VAA power to the device. Ferrite beads must only be used for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by assuring that all VCC pins are at the same potential, and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Application Information

Power-up Initialization

Following a power-up sequence, the Bt431 must be initialized. The following sequence is recommended:

1. Write $0000 to address pointer register
2. Do 13 write cycles to control registers
3. Write $0000 to address pointer register
4. Do 512 write cycles to the cursor RAM

Prior to the above sequence, the MPU may perform diagnostic checks on the device, such as checking that the RAM and control registers may be written to and read back.

Loading the Cursor RAM

When changing the cursor pattern, it is recommended that the following sequence be used to load the cursor RAM:

1. Write $0000 to address pointer register
2. Do 512 write cycles to the cursor RAM

Moving the Cursor

It is recommended that the following sequence be used to update the cursor (x,y) register:

1. Write $0001 to address pointer register
2. Read cursor (x) low
3. Read cursor (x) high
4. Read cursor (y) low
5. Read cursor (y) high
6. Calculate new (x,y) value
7. Write $0001 to address pointer register
8. Write new cursor (x) low
9. Write new cursor (x) high
10. Write new cursor (y) low
11. Write new cursor (y) high

The above sequence also applies to updating the window (x,y) register, except $0005 should be written to the address pointer register.

Changing the Window Size

To change the size of the cross hair window, it is recommended that the following sequence be used:

1. Write $0009 to address pointer register
2. Read window width low
3. Read window width high
4. Read window height low
5. Read window height high
6. Calculate new window width/height
7. Write $0009 to address pointer register
8. Write new window width low
9. Write new window width high
10. Write new window height low
11. Write new window height high

Using Multiple Devices

Multiple Bt431s may be used to generate more than one cursor, or to generate a multi-color cursor.

If using multiple devices to generate more than one cursor, the cursor outputs may be logically gated together, or each Bt431 may interface to a separate overlay input of the RAMDAC. If separate overlay inputs are used, the cursors will be automatically prioritized depending on which overlay is used for each cursor.

To generate a multi-color cursor (for example, using two Bt431s to generate a three-color cursor), each Bt431 must interface to a separate overlay input of the RAMDAC. Either a separate cursor (x,y) calculation for each Bt431 may be performed, or the same cursor (x,y) calculation used with the cursor information appropriately offset in the cursor RAM.

Interfacing to the Bt453 and Bt458

Figure 7 illustrates interfacing a single Bt431 to the Bt453 RAMDAC and Figure 8 illustrates interfacing to the Bt458 RAMDAC.

Interfacing to the Bt451, Bt454, Bt457, and Bt461/462 RAMDACs are similar to interfacing to the Bt458, due to the multiplexed overlay inputs of these devices. When interfacing to the Bt454, the CLOCK pin of the Bt431 should be connected to the LDOUT pin of the Bt454, and the Bt431 configured for 4:1 output multiplexing. Interfacing to the Bt450, Bt473, Bt475/477, Bt479, and Bt471/476/478 RAMDACs is similar to interfacing to the Bt453.

Application Information (continued)

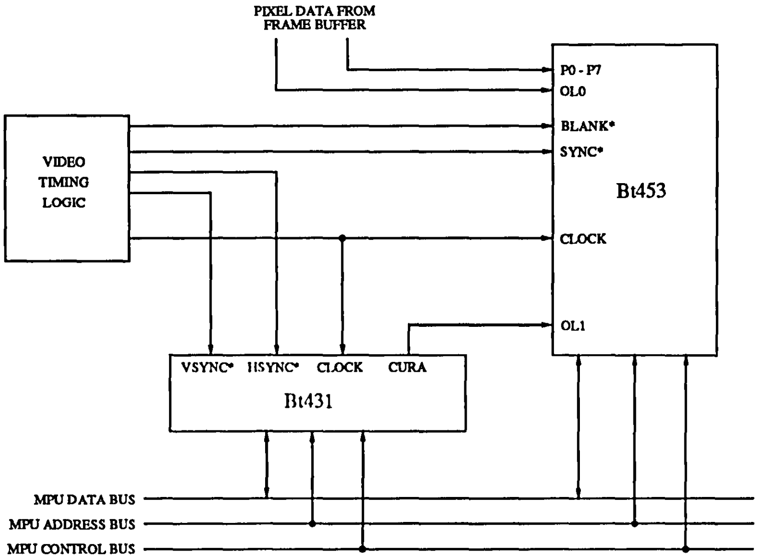

PIXEL DATA FROM FRAME BUFFER
VIDEO TIMING LOGIC
P0 - P7
OL0
BLANK*
SYNC*
Bt453
CLOCK
OL1
VSYNC*
HSYNC*
CLOCK
CURA
Bt431
MPU DATA BUS
MPU ADDRESS BUS
MPU CONTROL BUS

Figure 7. Interfacing to the Bt453.

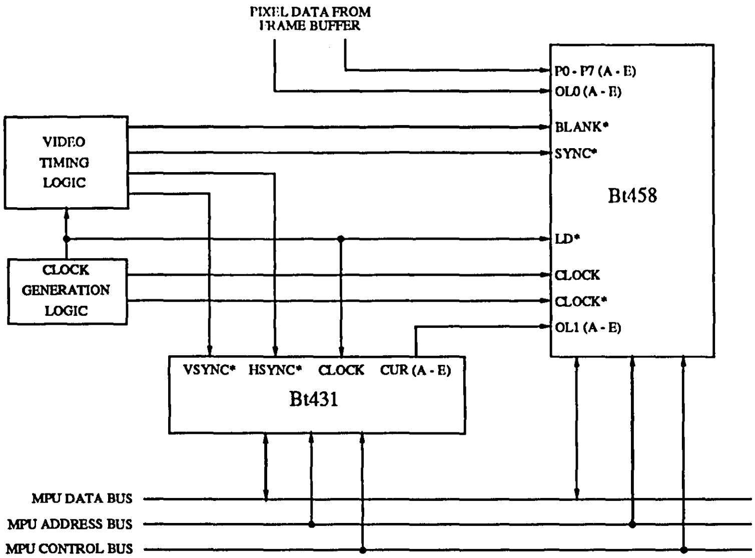

PIXEL DATA FROM FRAME BUFFER
VIDEO TIMING LOGIC
CLOCK GENERATION LOGIC
P0 - P7 (A - E)
OL0 (A - E)
BLANK*
SYNC*
Bt458
LD*
CLOCK
CLOCK*
OL1 (A - E)
VSYNC*
HSYNC*
CLOCK
CUR (A - E)
Bt431
MPU DATA BUS
MPU ADDRESS BUS
MPU CONTROL BUS

Figure 8. Interfacing to the Bt458.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	Volts
Voltage on Any Signal Pin*		GND–0.5		VCC + 0.5	Volts
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* This device employs high-impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
Digital Outputs (D0–D7)					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-state Current	IOZ			10	µA
Output Capacitance	COUT		20		pF
Digital Outputs (CURA–CURE)					
Output High Voltage (IOH = –400 µA)	VOH	2.4			Volts
Output Low Voltage (IOL = 1.6 mA)	VOL			0.4	Volts
3-state Current	IOZ			10	µA
Output Capacitance	COUT		20		pF

Test conditions (unless otherwise specified): "Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Clock Rate (per 1, 4, or 5 pixels)	Fmax			35	MHz
C0, C1, R/W Setup Time	1	10			ns
C0, C1, R/W Hold Time	2	15			ns
CE* Low Time	3	50			ns
CE* High Time	4	25			ns
CE* Asserted to Data Bus Driven	5	6			ns
CE* Asserted to Data Valid	6			100	ns
CE* Negated to Data Bus 3-Stated	7			15	ns
Write Data Setup Time	8	35			ns
Write Data Hold Time	9	4	2.5		ns
VSYNC*, HSYNC* Setup Time	10	10			ns
VSYNC*, HSYNC* Hold Time	11	5			ns
VSYNC*, HSYNC* Low Time		4			Clocks
VSYNC*, HSYNC* High Time		4			Clocks
Clock Cycle Time	12	28.6			ns
Clock Pulse Width High	13	10			ns
Clock Pulse Width Low	14	10			ns
Pipeline Delay	15			5	Clocks
Output Delay	16			20	ns
Three-State Disable Time	17			15	ns
Three-State Enable Time	18			15	ns
VCC Supply Current*	ICC			100	mA

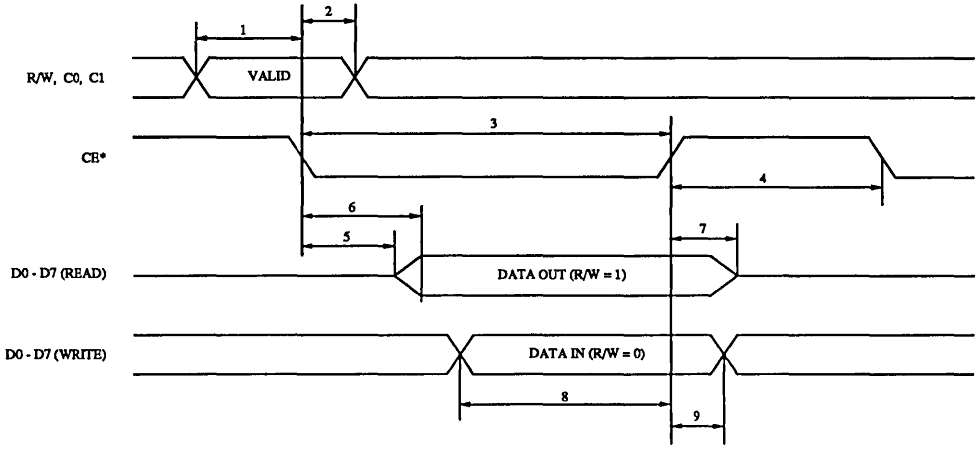
Test conditions (unless otherwise specified): "Recommended Operating Conditions." TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. CURA–CURE output load ≤ 10 pF, D0–D7 output load ≤ 130 pF. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*At Fmax. ICC (typ) at VAA = 5.0 V. ICC (max) at VAA = 5.25 V.

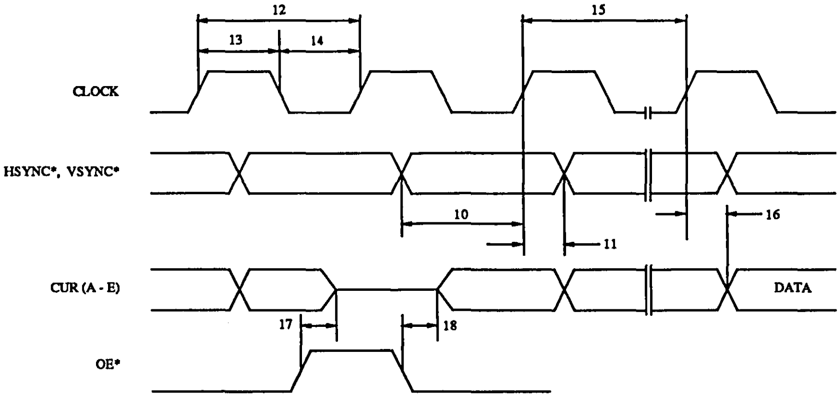
Ordering Information

Model Number	Package	Ambient Temperature Range
Bt431KC	24-pin 0.3" CERDIP	0° to +70° C
Bt431KPJ	28-pin Plastic J-Lead	0° to +70° C

Timing Waveforms


R/W, C0, C1
VALID
CE*
D0 - D7 (READ)
DATA OUT (R/W = 1)
D0 - D7 (WRITE)
DATA IN (R/W = 0)
1
2
3
4
5
6
7
8
9

MPU Read/Write Timing.


CLOCK
HSYNC*, VSYNC*
CUR (A - E)
DATA
OE*
10
11
12
13
14
15
16
17
18

Video Input/Output Timing.

Revision History

Datasheet Revision	*Change from Previous Revision*
G	Correct PLCC pinout.
H	Update Application Information Section to include interfacing to new RAMDACs.
I	Update three-state currents in DC section to be 10 µA.
J	Expanded ESD/Latchup information.

Bt438

Distinguishing Features

- 250 MHz Operation
- Differential ECL Clock Generation
- Divide by 3, 4, 5, or 8 of the Clock
- Divide by 2 and 4 of the Load
- Resets Pipeline Delay of the RAMDAC
- 1.2 V Voltage Reference Output
- Single +5 V Power Supply
- 20-pin DIP or 28-pin PLCC Package
- Typical Power Dissipation: 325 mW

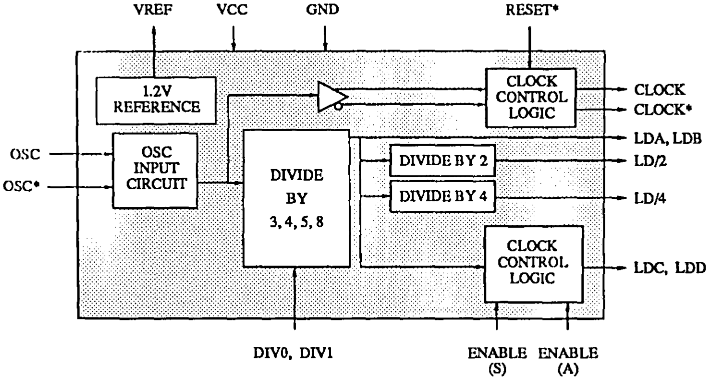
Customer Benefits

- Reduces PC Board Area
- Simplifies RAMDAC Design
- Cost Reduction over Discretes
- Increases System Reliability

Related Products

- Bt439

Functional Block Diagram


VREF
VCC
GND
RESET*
1.2V REFERENCE
CLOCK CONTROL LOGIC
CLOCK
CLOCK*
LDA, LDB
OSC
OSC*
OSC INPUT CIRCUIT
DIVIDE BY 3, 4, 5, 8
DIVIDE BY 2
LD/2
DIVIDE BY 4
LD/4
CLOCK CONTROL LOGIC
LDC, LDD
DIV0, DIV1
ENABLE (S)
ENABLE (A)

250 MHz Clock Generator Chip for CMOS RAMDACs™

Product Description

The Bt438 is a clock generator for the high-speed Brooktree CMOS RAMDACs. It interfaces a 10KH ECL oscillator operating from a single +5 V supply to the RAMDAC, generating the necessary clock and control signals.

The clock output may be divided by three, four, five, or eight to generate the load signal. The load signal is also divided by two and four for clocking video timing logic, etc.

A second load signal may be synchronously or asynchronously controlled to enable starting and stopping the clocking of the video DRAMs.

The Bt438 also optionally configures the pipeline delay of the RAMDAC to a fixed pipeline delay.

An on-chip 1.2 V voltage reference is also provided, and may be used to provide the reference voltage for up to four RAMDACs.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L438001 Rev. K

Brooktree®

Circuit Description

The Bt438 is designed to interface to a 10KH ECL crystal oscillator and generate the clock signals required by the RAMDACs. The OSC and OSC* inputs are designed to interface to a 10KH ECL oscillator operating from a single +5 V power supply.

The CLOCK and CLOCK* outputs are designed to interface directly to the CLOCK and CLOCK* inputs of the RAMDACs. The output levels are compatible with 10KH ECL logic operating from a single +5 V power supply.

DIV0 and DIV1 are used to specify whether the pixel clock is to be divided by three, four, five, or eight to generate the LDA and LDB signals. LDA is also divided by two and four to generate the LD/2 and LD/4 signals, respectively.

ENABLE (S) is internally synchronized to LDA and may be used to synchronously start and stop the LDC and LDD outputs. While ENABLE (S) is a logical zero, LDC and LDD will be a logical zero.

ENABLE (A) is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE (A) is a logical zero, the LDC and LDD outputs will remain in the state they were when the ENABLE (A) input went to a logical zero.

Note that both ENABLE (A) and ENABLE (S) should not be a logical zero simultaneously. If this occurs, synchronous control of LDC and LDD, via ENABLE (S), is not guaranteed.

While both ENABLE (S) and ENABLE (A) are a logical one, LDC and LDD will be free-running and in phase with LDA and LDB. This architecture allows the shift registers of the video DRAMs to be optionally non-clocked during the retrace intervals. Figure 1 illustrates the ENABLE implementation within the Bt438, while Figure 2 shows the load output timing.

The RESET* input is designed to enable the Bt438 to set the pipeline delay of the RAMDACs to a specified number of clock cycles (the exact number is dependent on the RAMDAC). Following the first rising edge of LD/4 after the rising edge of RESET*, the CLOCK and CLOCK* outputs are stopped in the high and low states, respectively. At the next rising edge of LD/4, the CLOCK and CLOCK* outputs are restarted. Figure 3 shows the operation of the RESET* input.

The Bt438 also generates a 1.2 V (typical) voltage reference, which may be used to drive the VREF input of up to four RAMDACs.

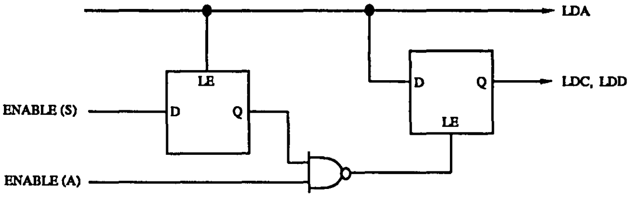


Figure 1. ENABLE Control Implementation.

Circuit Description (continued)

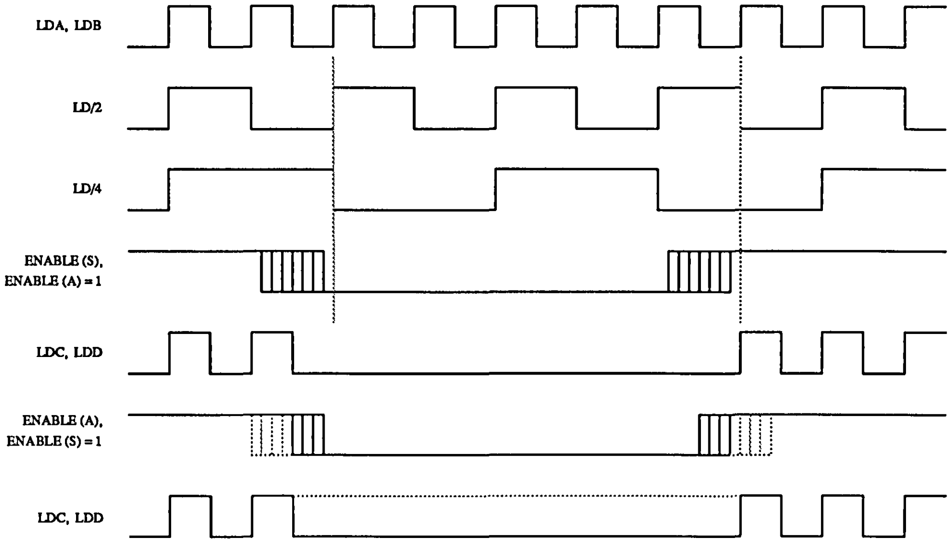

LDA, LDB
LD/2
LD/4
ENABLE (S), ENABLE (A) = 1
LDC, LDD
ENABLE (A), ENABLE (S) = 1
LDC, LDD

Figure 2. Load Output Timing.

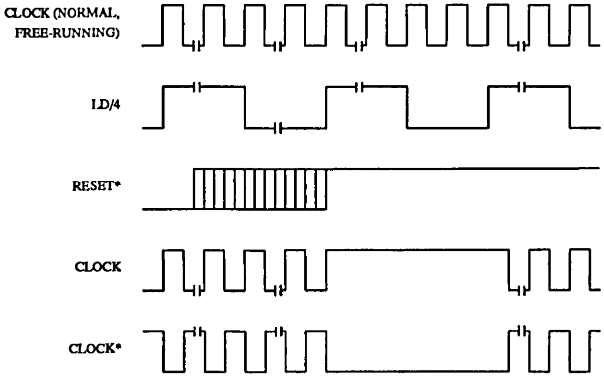

CLOCK (NORMAL, FREE-RUNNING)
LD/4
RESET*
CLOCK
CLOCK*

Figure 3. RESET Timing.*

Pin Descriptions

Pin Name	Description
VREF	Voltage reference output. This output provides a 1.2 V (typical) reference, and may be used to drive the VREF input of up to four RAMDACs.
OSC, OSC*	Differential ECL oscillator inputs. These inputs are designed to interface to a 10KH ECL crystal oscillator operating from a single +5 V supply.
CLOCK, CLOCK*	Differential clock outputs. These outputs connect directly to the CLOCK and CLOCK* inputs of the RAMDAC. The clock rate is equal to the OSC rate, and they are capable of driving up to four RAMDACs directly. The output levels are equivalent to 10KH ECL logic operating from a single +5 V supply.
DIV0, DIV1	Divide control inputs (TTL compatible). These inputs specify the division factor (3, 4, 5, or 8) for the generation of the LDA and LDB signals, as specified in below:

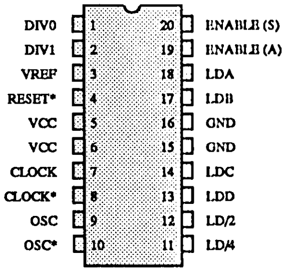
DIV1	DIV0	Division Factor	Clock Cycles Low	Clock Cycles High
0	0	+3	1	2
0	1	+4	2	2
1	0	+5	2	3
1	1	+8	4	4

Pin Name	Description
LDA, LDB	Load outputs (TTL compatible). LDA and LDB are generated by dividing CLOCK by three, four, five, or eight as determined by the DIV0 and DIV1 inputs. Each output may drive up to 20 video DRAMs without external buffering.
LD/2	Load output (TTL compatible). LD/2 is generated by dividing LDA by two. This output may drive up to 20 video DRAMs without external buffering.
LD/4	Load output (TTL compatible). LD/4 is generated by dividing LDA by four. This output may drive up to 20 video DRAMs without external buffering.
LDC, LDD	Load outputs (TTL compatible). When both ENABLE inputs are a logical one, these outputs have the same timing as the LDA and LDB outputs. Each output may drive up to 20 video DRAMs without external buffering.
ENABLE (S)	Synchronous load enable control input (TTL compatible). ENABLE (S) is internally synchronized to LDA and is used to synchronously start and stop the LDC and LDD outputs. While ENABLE (S) is a logical zero, LDC and LDD will be a logical zero. While both ENABLE (A) and ENABLE (S) are a logical one, LDC and LDD are free-running and in phase with the LDA and LDB outputs.
ENABLE (A)	Asynchronous load enable control input (TTL compatible). ENABLE (A) is used to asynchronously start and stop the LDC and LDD outputs. While ENABLE (A) is a logical zero, the LDC and LDD outputs will remain in the state they were when the ENABLE (A) input went to a logical zero. While both ENABLE (A) and ENABLE (S) are a logical one, LDC and LDD are free-running and in phase with the LDA and LDB outputs. Care should be taken to avoid glitches on this asynchronous input.

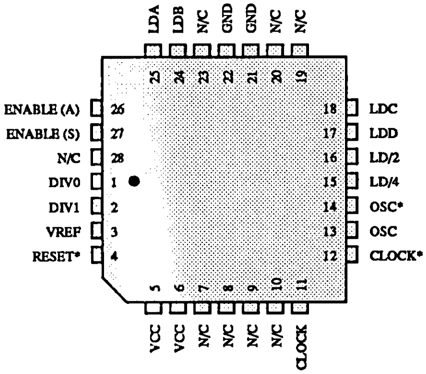
Pin Descriptions (continued)

Pin Name	Description
RESET*	Reset control input (TTL compatible). Following the first rising edge of LD/4 after the rising edge of RESET*, CLOCK and CLOCK* are stopped in the high and low states, respectively. At the next rising edge of LD/4, the CLOCK and CLOCK* outputs are set to be free-running. Care must be taken to avoid glitches on this edge-triggered input.
VCC	Device power. All VCC pins must be connected.
GND	Device ground. All GND pins must be connected.

20-pin DIP Package


DIV0 1
DIV1 2
VREF 3
RESET* 4
VCC 5
VCC 6
CLOCK 7
CLOCK* 8
OSC 9
OSC* 10
20 ENABLE (S)
19 ENABLE (A)
18 LDA
17 LDB
16 GND
15 GND
14 LDC
13 LDD
12 LD/2
11 LD/4

28-pin Plastic J-Lead
(PLCC) Package


LDA 25
LDB 24
N/C 23
GND 22
GND 21
N/C 20
N/C 19
ENABLE (A) 26
ENABLE (S) 27
N/C 28
DIV0 1
DIV1 2
VREF 3
RESET* 4
18 LDC
17 LDD
16 LD/2
15 LD/4
14 OSC*
13 OSC
12 CLOCK*
5 VCC
6 VCC
7 N/C
8 N/C
9 N/C
10 N/C
11 CLOCK

Note: N/C pins may be left floating without affecting the performance of the Bt438.

Application Information

Interfacing to the RAMDAC

Figure 4 illustrates interfacing the Bt438 to the RAMDAC when using a differential crystal oscillator. The Bt438 should be located as close as possible to the RAMDAC. The termination resistors for the OSC and OSC* inputs should be located as close as possible to the Bt438.

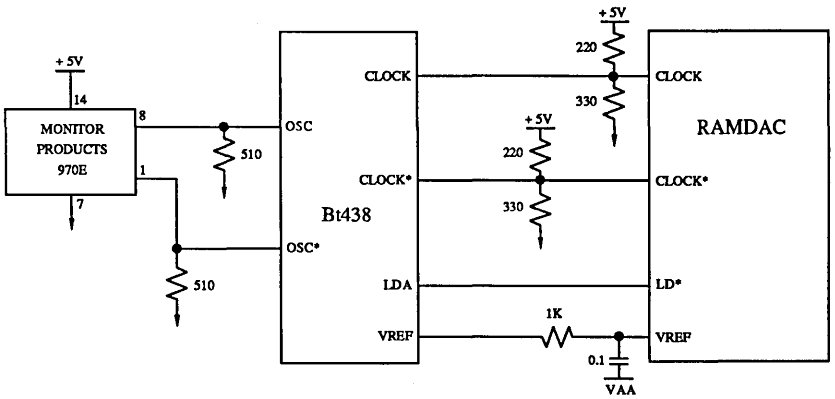
Termination resistors are also required on the CLOCK and CLOCK* lines, located as close as possible to the RAMDAC.

Figure 5 illustrates interfacing to a single-ended crystal oscillator, while Figure 6 shows interfacing to a TTL clock for applications less than 75 MHz.

The Bt438 may drive the CLOCK and CLOCK* inputs of up to four RAMDACs if they are located as close as possible to each other. Only one set of 220/330 termination resistors should be used, and these positioned at the RAMDAC furthest away from the Bt438.

Due to the inability to insure proper synchronization between Bt438s, multiple devices should not be used in applications where multiple RAMDACs drive the same monitor.

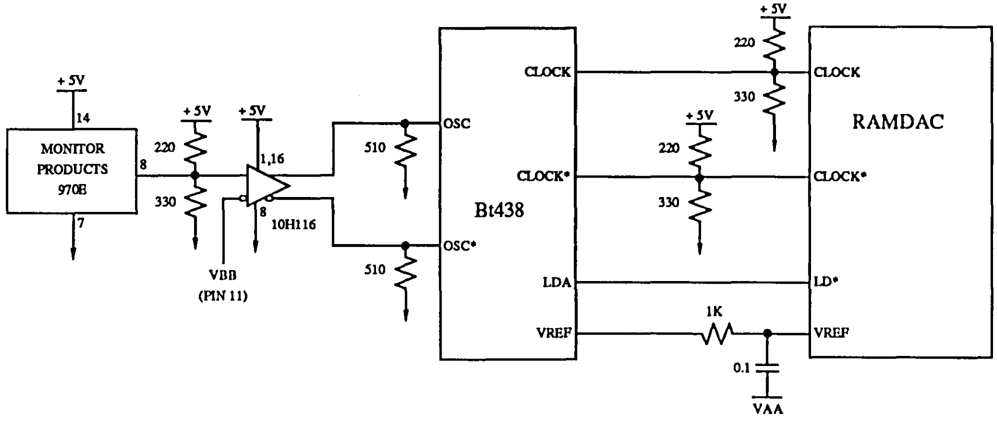
A 1 kΩ (typical) resistor must be used to isolate the VREF output of the Bt438 from the VREF input of the RAMDAC. This isolates noise from the Bt438 voltage reference from being coupled onto the RAMDAC VREF pin. The VREF input of the RAMDAC must still have a decoupling capacitor to VAA, as specified in the data sheet.



NOTE: CLOCK AND CLOCK* TERMINATION AT > 125 MHZ,
TYP 220 OHM PULL DOWN ONLY.

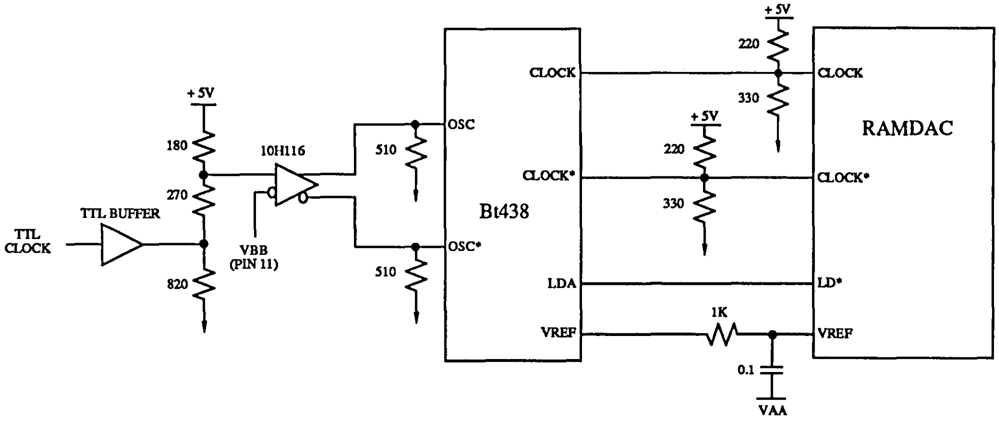
Figure 4. Interfacing to a Differential Crystal Oscillator.

Application Information (continued)


+5V
14
MONITOR
PRODUCTS
970B
8
7
+5V
220
330
+5V
1,16
8
10H116
VBB
(PIN 11)
510
510
OSC
OSC*
Bt438
CLOCK
CLOCK*
LDA
VREF
+5V
220
330
+5V
220
330
1K
0.1
VAA
CLOCK
RAMDAC
CLOCK*
LD*
VREF

NOTE: CLOCK AND CLOCK* TERMINATION AT > 125 MHZ, TYP 220 OHM PULL DOWN ONLY.

Figure 5. Interfacing to a Single-Ended Crystal Oscillator.


TTL
CLOCK
TTL BUFFER
+5V
180
270
820
10H116
VBB
(PIN 11)
510
510
OSC
OSC*
Bt438
CLOCK
CLOCK*
LDA
VREF
+5V
220
330
+5V
220
330
1K
0.1
VAA
CLOCK
RAMDAC
CLOCK*
LD*
VREF

NOTE: CLOCK AND CLOCK* TERMINATION AT > 125 MHZ, TYP 220 OHM PULL DOWN ONLY.

Figure 6. Interfacing to a TTL Clock.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
OSC/OSC* Duty Cycle		40			%

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	Volts
Voltage on any Pin		GND–0.5		VCC + 0.5	Volts
CLOCK, CLOCK* Output Current				30	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ				
Ceramic Package				+175	°C
Plastic Package				+150	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C
Air Flow		0			l.f.p.m.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification isnot implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL Inputs					
Input High Voltage (other pins)	VIH	2.0		VCC + 0.5	Volts
DIV0, DIV1		2.2		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			10	μA
Input Low Current (Vin = 0.4 V)	IIL			-0.7	mA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		4		pF
ECL Inputs (at 25° C.)					
Input High Voltage	VIH	VCC–1.1		VCC–0.8	Volts
Input Low Voltage	VIL	GND–0.5		VCC–1.5	Volts
Input High Current (Vin = 4.0 V)	IIH			15	μA
Input Low Current (Vin = 0.4 V)	IIL			15	μA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CIN		4		pF
Load Outputs					
Output High Voltage (IOH = –2 mA)	VOH	2.4			Volts
Output Low Voltage (IOL = 20 mA)	VOL			0.8	Volts
Output Capacitance			10		pF
Clock Outputs (at 25° C)					
Differential Output Voltage	ΔVOUT	.6			Volts
Output Capacitance	COUT		7		pF
Voltage Reference					
Output Voltage	VREF				
(Bt438 Rev. C)*		1.12	1.2	1.27	Volts
Output Current	IREF		100		μA
VCC Supply Current**	ICC		65	85	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions." CLOCK and CLOCK* have 50 Ω to VCC–2 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*RSET of the RAMDAC should be adjusted due to the output voltage of the Bt438 Rev. C being lower than the recommended VREF for the RAMDAC. IOG (mA) = $\frac{11294\ \text{VREF}}{\text{RSET}}$, IOG (typ) = 26.7 mA.

**Measured without 50 Ω to VCC–2 V on CLOCK and CLOCK*.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
OSC, OSC* Clock Rate	Fmax			250	MHz
LDA Output Delay (note 1)	1		4	10	ns
LDA, LDB Pulse Width Low (note 3)		5			ns
LDA to LDB Output Skew (note 2)		-2.0	0	2.0	ns
LDA to LDC Output Skew (note 2)		-1.0	1.5	4.0	ns
LDA to LD/2 Output Skew (note 2)		0	1.5	5.0	ns
LDA to LD/4 Output Skew (note 2)		0	1.5	6.0	ns
LDC to LDD Output Skew (note 2)		-2.0	0	2.0	ns
RESET* Active Low Time	2	15			ns
RESET* Setup Time	3	12			ns
ENABLE (S) Setup Time	4	12			ns
ENABLE (S) Hold Time	5	-2			ns
ENABLE (A) Setup Time	6	12			ns
ENABLE (A) Hold Time	7	-2			ns

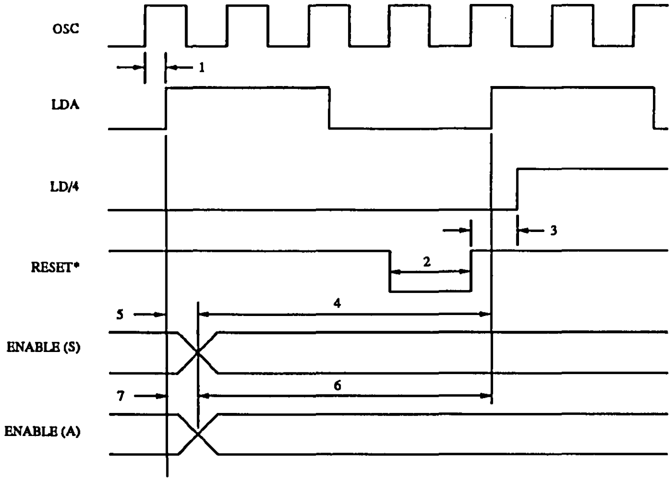
Test conditions (unless otherwise specified): "Recommended Operating Conditions". CLOCK and CLOCK* have 50 Ω to VCC–2 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between 10% and 90% points. ECL input values are 3.2–4.2 V, with input rise/fall times ≤ 1 ns, measured between 20% and 80% points. Timing reference points at 50% for inputs and outputs. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note 1: Output load = 50 pF.
Note 2: LD outputs equally loaded with 50 pF. Unequal loading may result in additional output skew.
Note 3: LD outputs not used in +3 over 200 MHz.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt438KC	20-pin 0.3" CERDIP	0° to +70° C
Bt438KPJ	28-pin Plastic J-Lead	0° to +70° C

Timing Waveforms


OSC
1
LDA
LD/4
3
2
RESET*
5
4
ENABLE (S)
7
6
ENABLE (A)

Input/Output Timing.

Revision History

Datasheet Revision	*Change from Previous Revision*
H	Thermal equilibrium notes added to Recommended Operating Conditions and DC Characteristics.
I	Rev. B silicon voltage reference limits changed.
J	Rev. C silicon voltage reference limits changed.
K	Upgraded datasheet status to Final. Added DIV0 and DIV1 to DC Characteristics.

Device Revision	
C	Changed VREF limits.

Bt439

200 MHz Clock Generator and Synchronizer Chip for CMOS RAMDACs™

Distinguishing Features

- 200 MHz Operation
- 4 Differential ECL Clock Outputs
- Synchronizes Multiple CMOS RAMDACs
- Divide by 3, 4, 5, or 8 of the Clock
- Divide by 2 and 4 of the Load
- Resets Pipeline Delay of the RAMDAC
- Reduces Skew Between Devices to < 2 ns
- 1.2 V Voltage Reference Output
- Single +5 V Power Supply
- 28-pin DIP Package

Customer Benefits

- Reduces PC Board Area
- Simplifies RAMDAC Design
- Cost Reduction over Discretes
- Increases System Reliability
- Eases Design of True Color Systems

Related Products

- Bt438

Product Description

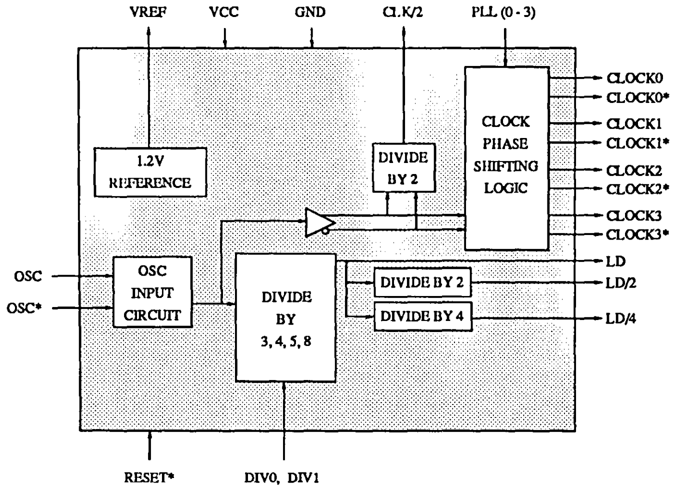
The Bt439 is a clock generator chip for the high-speed Brooktree single-channel CMOS RAMDACs. It interfaces a 10KH ECL oscillator operating from a single +5 V supply to the RAMDACs, generating the necessary clock and control signals.

Up to four CMOS RAMDACs may be synchronized with sub-pixel resolution. The Bt439 accepts a PLL signal from each RAMDAC, and adjusts the differential clocks to each RAMDAC to minimize the phase difference between the PLL signals.

The clock output may be divided by three, four, five, or eight to generate the load signal. The load signal is also divided by two and four for clocking video timing logic, etc.

The Bt439 optionally configures the pipeline delay of the RAMDAC to a fixed pipeline delay. An on-chip voltage reference is provided, and may be used to provide the reference voltage for up to four RAMDACs.

Functional Block Diagram


VREF
VCC
GND
CLK/2
PLL (0 - 3)
CLOCK0
CLOCK0*
CLOCK1
CLOCK1*
CLOCK2
CLOCK2*
CLOCK3
CLOCK3*
CLOCK PHASE SHIFTING LOGIC
DIVIDE BY 2
1.2V REFERENCE
OSC
OSC*
OSC INPUT CIRCUIT
DIVIDE BY 3, 4, 5, 8
DIVIDE BY 2
DIVIDE BY 4
LD
LD/2
LD/4
RESET*
DIV0, DIV1

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249

Brooktree®

Circuit Description

The Bt439 is designed to interface to a 10K ECL crystal oscillator and generate the clock signals required by up to four CMOS RAMDACs. The OSC and OSC* inputs are designed to interface to a 10K ECL oscillator operating from a single +5 V power supply.

All of the CLOCK and CLOCK* outputs are designed to interface directly to the CLOCK and CLOCK* inputs of the RAMDACs. The output levels are similar to 10KH ECL logic, operating from a single +5 V power supply.

DIV0 and DIV1 are used to specify whether the pixel clock is to be divided by three, four, five, or eight to generate the LD signal. LD is also divided by 2 and 4 to generate the LD/2 and LD/4 signals, respectively.

The RESET* input is designed to enable the Bt439 to set the pipeline delay of the RAMDACs to a fixed pipeline delay of eight clock cycles. Following the first rising edge of LD/4 after the rising edge of RESET*, the CLOCK and CLOCK* outputs are stopped in the high and low states, respectively. At the next rising edge of LD/4, the CLOCK and CLOCK* outputs are restarted. Figure 2 shows the operation of the RESET* input.

The Bt439 also generates a 1.2 V (typical) voltage reference, which may be used to drive the VREF input of up to four RAMDACs.

Synchronizing Multiple RAMDACs

The Bt439 is designed specifically to synchronize multiple CMOS RAMDACs that generate a PLL output signal. Typically, only single-channel RAMDACs will generate the PLL signal. The synchronization is necessary due to wide variations in output delays for CMOS devices due to the CMOS processing.

Following a reset input, the Bt439 sets the pipeline delay of all the RAMDACs to eight clock cycles. It then monitors the PLL inputs, PLL0–PLL3. On the rising edge of the last PLL input to go high, the Bt439 latches the relative time differences between the PLL inputs.

The Bt439 then stops the clocks to all the RAMDACs, with CLOCK low and CLOCK* high. The time differences between the PLL inputs are used to adjust the clock phases by selecting appropriate taps from internal delay lines (one set of delay lines for each clock signal). The Bt439 then restarts the clocks.

RESET Timing Sequence*

The following will occur when the RESET* input is asserted and remains low for at least 15 ns:

The LD, LD/2, and LD/4 outputs will be forced high (CLK/2 low) within 9 ns of the falling edge of RESET* and will remain so as long as RESET* is active low. Any programmed skew between the CLKx outputs will be zeroed at this point (anticipating a re-timing sequence), which may result in some non-valid CLKx pulses. For this reason, the RESET* input should be activated only during the blanking interval to avoid visible timing transients from the palette DACs.

When RESET* rises outside the prescribed setup/hold time before a rising OSC input, the LD output will toggle high-to-low after the fourth subsequent rising OSC input.

LD/2 will toggle high-to-low coincident with the first rising edge of LD. LD/4 will toggle high-to-low on the second rising edge of LD.

On the next rising edge of LD/4 all the ECL CLKx true outputs will be forced high (CLKx low) for one cycle of the LD/4, and will fall generally (1.5*OSC period–6 ns) after the following rising LD/4 and resume toggling.

RESET* transitions occurring within the setup/hold interval will delay the corresponding response one cycle of OSC In this way correct response to an asynchronous RESET* is assured. See Figure 1.

The Bt439 requires a minimum of two reset signals to assure clock operation, and correct pixel alignment operation, immediately after power up. The first reset signal is needed to start the CLK and CLK* signals. The system power-up RESET* can be used as CLK and CLK* initiators.

A second reset signal must be applied for initiating pixel alignment sequence. Please reference the pixel alignment sequence for proper timing requirements.

Should the multiplex factor change (as set by DIV0 and DIV1) after the initialization sequence, another reset should be applied to the Bt439.

Circuit Description (continued)

Pixel Alignment Sequence

A RESET* timing sequence must precede each pixel alignment sequence and should be completed within a blanking interval to avoid corruption of the pixel alignment sequence, which is triggered by the beginning of the ensuing active line. A pixel alignment sequence proceeds as follows:

The first falling PLLx input after a RESET* timing sequence initiates a delay-sampling process for the duration of the active (e.g. non-blanked) interval, which terminates with the last rising PLLx input (e.g. beginning of subsequent blank interval). The CLKx outputs maintain minimal delay through the duration of this active line; hence, any systematic delays between the PLL generators will not be corrected during this active line. Those applications which call for asserting RESET* on a line-by-line basis may consider toggling blank in the back porch interval after normal blanking to maintain CLKx alignment on each line (at least one LD* clock cycle should occur before the first rising PLL edge).

The first rising edge of CLK/2 following the last rising PLLx input initiates a pixel alignment sequence which takes up to two periods of CLK/2 to complete. During this sequence, the CLKx outputs are held low (false) and the TTL outputs are inhibited from toggling. No false or short CLKx pulses result because of controlled time delays on chip. The proper skew compensation for each CLKx channel is latched in the internal delay lines. Concluding this sequence, the CLKy corresponding to the last (slowest) PLLy input will resume toggling with about 2 ns additional skew relative to OSC while the CLKz associated with the first (fastest) PLLz will resume with up to (Δ + (err)) ns extra delay relative to CLKy. The TTL outputs resume toggling with a consistent relationship relative to the CLK, which is consistent with the palette DAC pipeline delay preservation requirement. Note that this will stretch the low LD clock duration by up to 5 pixels, which may momentarily affect any dependent synchronization timing counters.

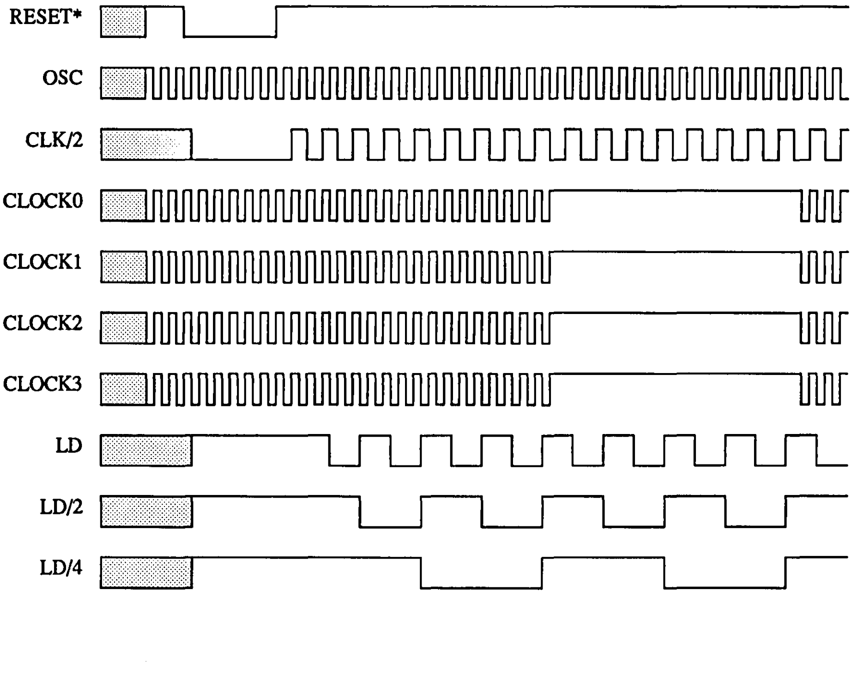


Figure 1. RESET Timing Sequence.*

Circuit Description (continued)

The slowest PLLy–CLKy channel defaults to the minimum delay setting. If the slowest PLLy input lags the other active PLLx inputs by an interval exceeding the alignment span of the Bt439, then the faster PLLx channels will default to the maximum delay setting. Hence, occurrence of any active PLLx input outside the alignment span will render skew compensation on the other channels inoperative. Unused PLLx inputs are internally pulled high and hence are not sampled, leaving their corresponding CLKx channel in the maximum delay condition. See Figure 2.

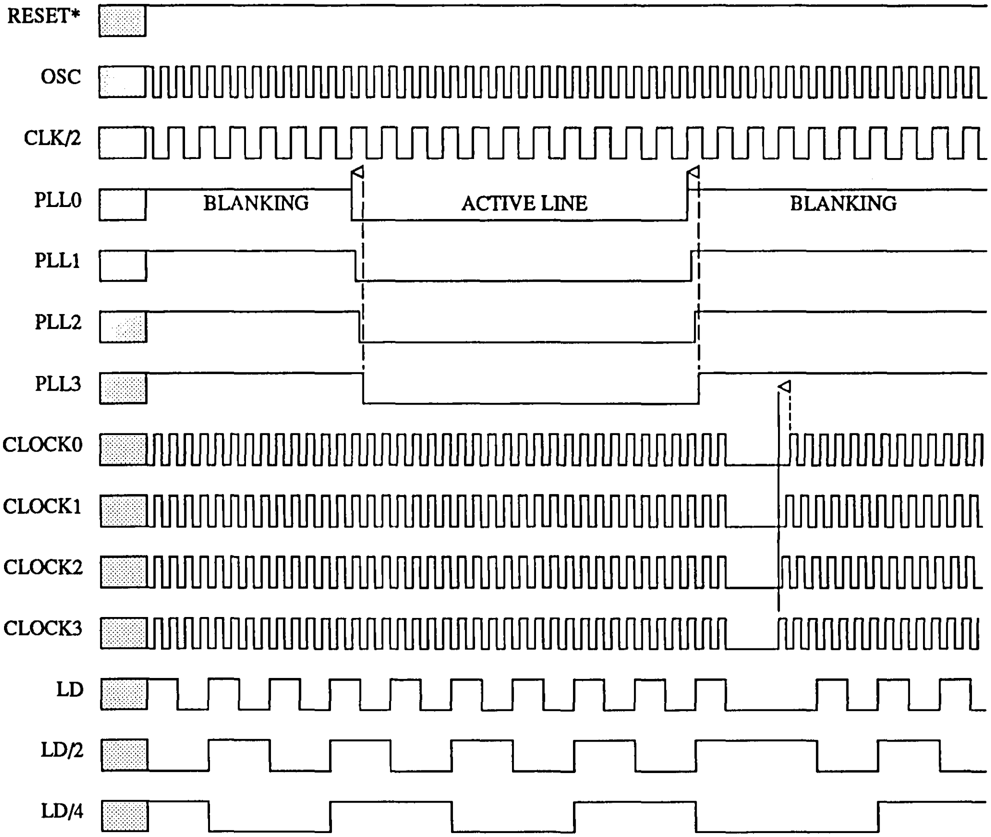

RESET*
OSC
CLK/2
PLL0
BLANKING
ACTIVE LINE
BLANKING
PLL1
PLL2
PLL3
CLOCK0
CLOCK1
CLOCK2
CLOCK3
LD
LD/2
LD/4

Figure 2. Pixel Alignment Sequence.

Pin Descriptions

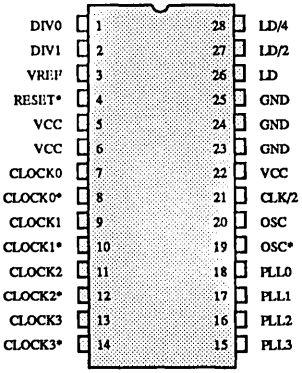
Pin Name	Description
VREF	Voltage reference output. This output provides a 1.2 V (typical) reference, and may be used to drive the VREF input of up to four RAMDACs.
OSC, OSC*	Differential ECL oscillator inputs (+5 V ECL compatible). These inputs are designed to interface to a 10K ECL crystal oscillator operating from a single +5 V supply.
CLOCK(0–3), CLOCK(0–3)*	Differential clock outputs (+5 V ECL compatible). These outputs connect directly to the CLOCK and CLOCK* inputs of up to four RAMDACs. The output levels are equivalent to 10K ECL logic operating from a single +5 V supply.
DIV0, DIV1	Divide control inputs (TTL compatible). These inputs specify the division factor for the generation of the LD signal, as specified below:

DIV1	DIV0	Division Factor	Clock Cycles Low	Clock Cycles High
0	0	+3	1	2
0	1	+4	2	2
1	0	+5	2	3
1	1	+8	4	4

Pin Name	Description
LD	Load output (TTL compatible). LD is generated by dividing CLOCK by three, four, five, or eight as determined by the DIV0 and DIV1 inputs. It may drive up to 20 video DRAMs without external buffering.
LD/2	Load output (TTL compatible). LD/2 is generated by dividing LD by two. This output may drive up to 20 video DRAMs without external buffering.
LD/4	Load output (TTL compatible). LD/4 is generated by dividing LD by four. This output may drive up to 20 video DRAMs without external buffering.

Pin Descriptions (continued)

Pin Name	Description
RESET*	Reset control input (TTL compatible). See RESET* Timing Sequence. Care must be taken to avoid glitches on this edge-triggered input.
PLL0–PLL3	Phase inputs. These inputs are used to determine the relative phases of the RAMDAC outputs. Each RAMDAC to be synchronized must generate a unique PLL signal. Unused PLL inputs should be connected to VCC through a 1K pullup resistor.
CLK/2	Clock/2 output (+5 V ECL compatible). The OSC input is divided by two and output onto this pin. It may be used as a general purpose clock for external circuitry.
VCC	Device power. All VCC pins must be connected.
GND	Device ground. All GND pins must be connected.


DIV0 1
DIV1 2
VREF 3
RESET* 4
VCC 5
VCC 6
CLOCK0 7
CLOCK0* 8
CLOCK1 9
CLOCK1* 10
CLOCK2 11
CLOCK2* 12
CLOCK3 13
CLOCK3* 14
28 LD/4
27 LD/2
26 LD
25 GND
24 GND
23 GND
22 VCC
21 CLK/2
20 OSC
19 OSC*
18 PLL0
17 PLL1
16 PLL2
15 PLL3

Application Information

Interfacing to the RAMDAC

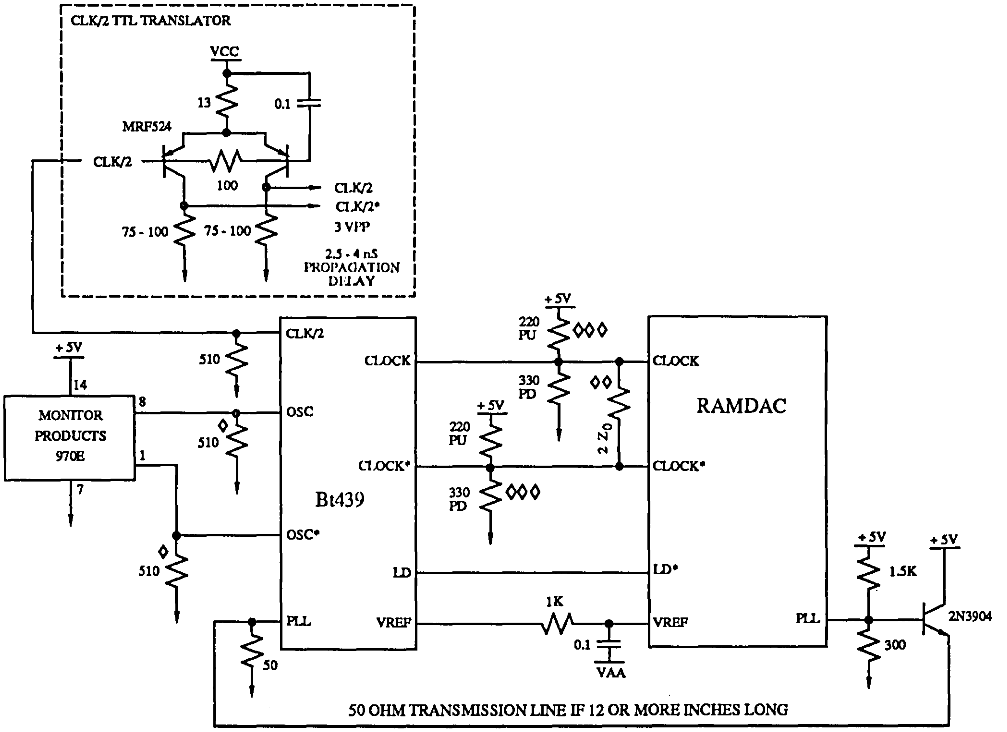
Figure 3 illustrates interfacing the Bt439 to a CMOS RAMDAC when using a differential crystal oscillator. The Bt439 should be located as close as possible to the RAMDACs. The termination resistors for the OSC and OSC* inputs should be located as close as possible to the Bt439.

Termination resistors are also required on the CLOCK and CLOCK* lines, located as close as possible to the RAMDAC For clock lines > 4", pulldowns at the Bt439 as well as balance lined termination at the palette are recommended. For striplines of Zo characteristic impedance separated by > 2d dielectric spacing, a balanced termination of 2Zo is appropriate.

Figure 4 illustrates interfacing to a single-ended crystal oscillator, while Figure 5 shows interfacing to a TTL clock for applications less than 75 MHz.

A 1 kΩ (typical) resistor must be used to isolate the VREF output of the Bt439 from the VREF input of the RAMDAC This isolates noise from the Bt439 voltage reference from being coupled onto the RAMDAC VREF pin. The VREF input of each RAMDAC must still have a decoupling capacitor to VAA, as specified in the data sheet.

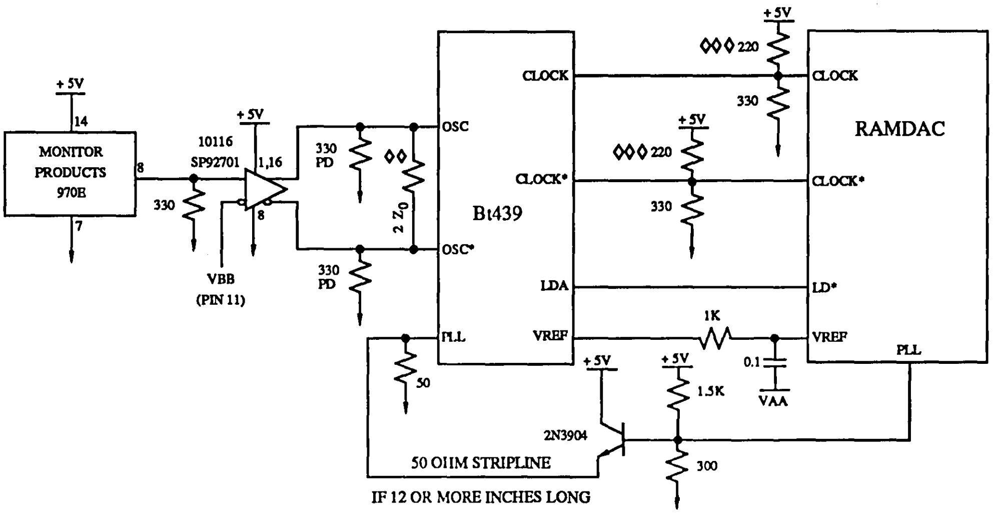
Due to the limited drive capability of the PLL output of the RAMDACs, the buffer circuitry should be located as close as possible to the RAMDAC


CLK/2 TTL TRANSLATOR
VCC
13
0.1
MRF524
CLK/2
100
CLK/2
CLK/2*
3 VPP
75 - 100
75 - 100
2.5 - 4 nS PROPAGATION DELAY
+5V
14
MONITOR PRODUCTS 970E
8
1
7
510
510
510
CLK/2
CLOCK
OSC
CLOCK*
Bt439
OSC*
LD
PLL
VREF
50
+5V
220 PU
330 PD
+5V
220 PU
330 PD
2 Zo
1K
0.1
VAA
CLOCK
RAMDAC
CLOCK*
LD*
VREF
PLL
+5V
1.5K
300
+5V
2N3904
50 OHM TRANSMISSION LINE IF 12 OR MORE INCHES LONG

◊ 510 OHM RESISTOR NEEDED IF THERE ARE NO INTERNAL PULL DOWNS IN OSCILLATOR.
◊◊ OPTIONAL BALANCED TERMINATION FOR HIGH IMPEDANCE DIFFERENTIAL LINES > 4 INCHES; OMIT 220 OHM PULL UP IF USED.
◊◊◊ CLOCK AND CLOCK* TERMINATION AT > 125 MHz, TYP 220 OHM PD ONLY.
Zo = UNBALANCED STRIPLINE IMPEDANCE >/= PD/6.

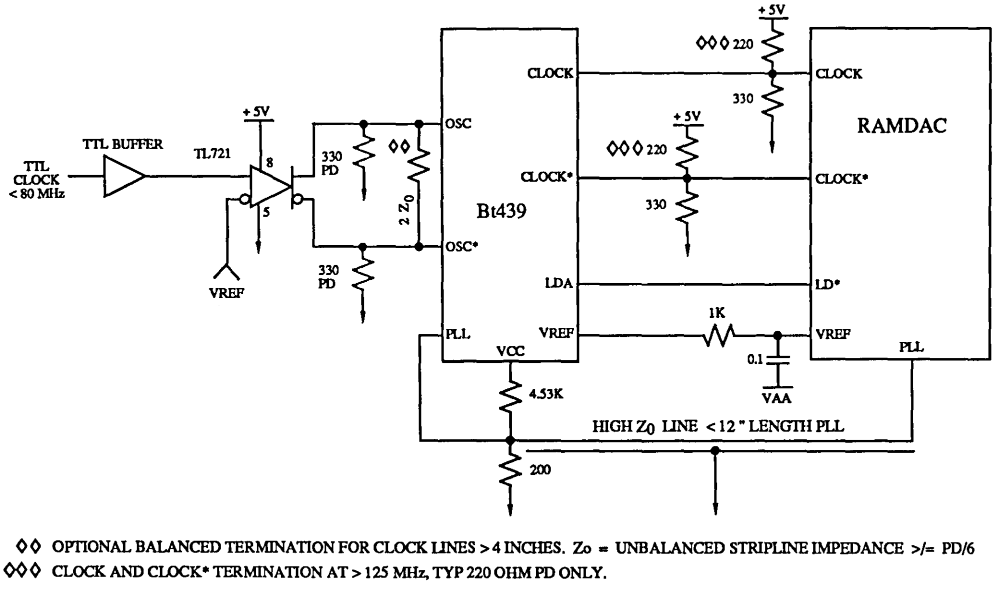
Figure 3. Interfacing to a Differential Crystal Oscillator.

Application Information (continued)


+5V
14
MONITOR PRODUCTS 970E
8
7
330
10116
SP92701
1,16
+5V
8
VBB
(PIN 11)
330 PD
◊◊
2 Z0
330 PD
OSC
OSC*
B t439
CLOCK
CLOCK*
LDA
PLL
VREF
50
+5V
2N3904
50 OHM STRIPLINE
IF 12 OR MORE INCHES LONG
+5V
1.5K
300
1K
0.1
VAA
+5V
◊◊◊ 220
330
+5V
◊◊◊ 220
330
RAMDAC
CLOCK
CLOCK*
LD*
VREF
PLL

◊◊ OPTIONAL BALANCED TERMINATION FOR CLOCK LINES > 4 INCHES. Zo = UNBALANCED STRIPLINE IMPEDANCE >/= PD/6
◊◊◊ CLOCK AND CLOCK* TERMINATION AT > 125 MHz, TYP 220 OHM PD ONLY.

Figure 4. Interfacing to a Single-Ended Crystal Oscillator.


TTL CLOCK < 80 MHz
TTL BUFFER
TL721
+5V
8
5
VREF
330 PD
◊◊
2 Z0
330 PD
OSC
OSC*
Bt439
CLOCK
CLOCK*
LDA
PLL
VREF
VCC
4.53K
200
HIGH Z0 LINE < 12" LENGTH PLL
1K
0.1
VAA
+5V
◊◊◊ 220
330
+5V
◊◊◊ 220
330
RAMDAC
CLOCK
CLOCK*
LD*
VREF
PLL

◊◊ OPTIONAL BALANCED TERMINATION FOR CLOCK LINES > 4 INCHES. Zo = UNBALANCED STRIPLINE IMPEDANCE >/= PD/6
◊◊◊ CLOCK AND CLOCK* TERMINATION AT > 125 MHz, TYP 220 OHM PD ONLY.

Figure 5. Interfacing to a TTL Clock < 80 MHz.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	Volts
Ambient Operating Temperature –Still Air	TA	0		+70	°C
OSC/OSC* Duty Cycle		40			%

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 50 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)				7.0	Volts
Voltage on any Pin		GND–0.5		VCC + 0.5	Volts
CLOCK, CLOCK* Output Current				30	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C
Air Flow		50			l.f.p.m.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			10	µA
Input Low Current (Vin = 0.4 V)	IIL	–0.7			mA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		10		pF
ECL Inputs					
Input High Voltage	VIH	VCC–1.1		VCC–0.8	Volts
Input Low Voltage	VIL	VCC–2		VCC–1.5	Volts
Input High Current (Vin = 4.0 V)	IIH		4	15	µA
Input Low Current (Vin = 0.4 V)	IIL	–15	0		µA
Input Capacitance (f = 1 MHz, Vin = 4.0 V)	CIN		10		pF
Load Outputs					
Output High Voltage (IOH =–2 mA)	VOH	2.4			Volts
Output Low Voltage (IOL = 20 mA)	VOL			0.8	Volts
Output Capacitance			10		pF
Clock Outputs					
Differential Output Voltage	ΔVOUT	.6			Volts
Output Capacitance	COUT		10		pF
Voltage Reference					
Output Voltage @ IREF = -100 µA	VREF	1.17	1.235	1.31	Volts
PLL Inputs					
Input High Voltage	VIH	1.5		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.4	Volts
Input High Current (Vin = 1.2 V)	IIH		0	10	µA
Input Low Current (Vin = 0.5 V)	IIL	–700	–180		µA
Input Capacitance			10		pF
VCC Supply Current*	ICC		275	300	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions." CLOCK, CLOCK*, and CLK/2 outputs have 50 Ω to VCC–2 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Measured without 50 ohms to VCC–2 volts on CLOCK, CLOCK, and CLK/2. At VCC = 5.25 V.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 50 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
OSC, OSC* Clock Rate (note 1)	Fmax			200	MHz
LD Output Delay (note 2)	1	6	10	12	ns
LD Pulse Width	2	9			ns
LD to LD/2 Output Skew (note 3)		0	1.5	3	ns
LD to LD/4 Output Skew (note 3)		0	1.5	3	ns
CLK/2 Output Delay	3		2	4	ns
RESET* Active Low Time	4	15			ns
RESET* Setup Time	5	10			ns
Alignment Span	6	5			ns
Residual Alignment Error (note 4)			1.5	2	ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions". CLOCK, CLOCK*, and CLK/2 outputs have 50 Ω to VCC–2 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between 10% and 90% points. ECL input values are (VCC–0.9) to (VCC–1.6) V, with input rise/fall times ≤ 1 ns, measured between 20% and 80% points. Timing reference points at 50% for inputs and outputs. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note 1: + 3 Mode LD outputs valid only to 100 MHz without significant distortion.
Note 2: Output load = 50 pF. Derate 1 ns for each additional 50 pF loading.
Note 3: Load outputs equally loaded with 50 pF. Unequal loading may result in additional output skew.
Note 4: Maximum deviation of any two dependent PLL inputs after alignment sequence (PLL inputs within span before alignment).

Timing Waveforms

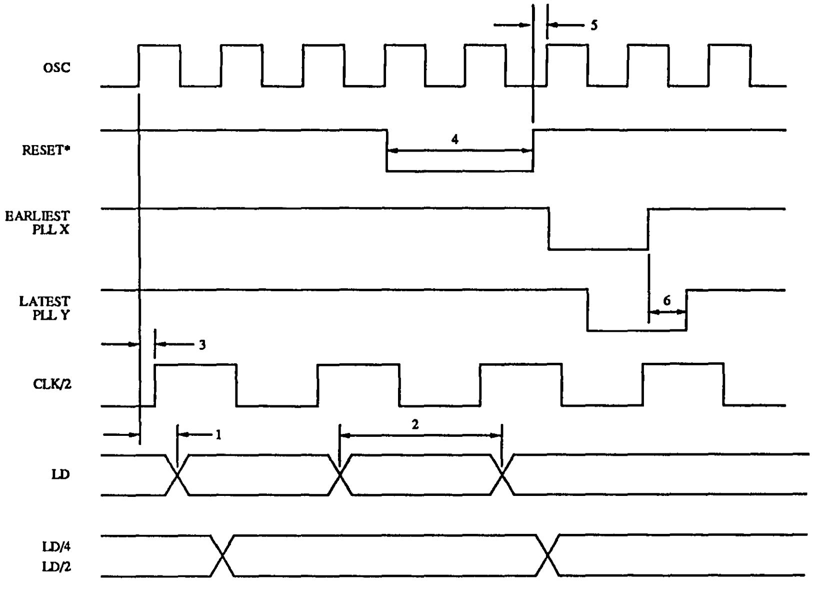


Figure 6. Input/Output Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt439KC	28-pin 0.6" CERDIP	0° to +70° C

Revision History

Datasheet Revision	*Change from Previous Revision*
E	Thermal equilibrium notes added to Recommended Operating Conditions and DC Characteristics.
F	Clarified reset requirements, changed VREF maximum, revised PLL feedback circuitry, reduced ILL maximum, added required airflow.

Datasheet Revision	
B	Changed pixel alignment sequence for longer period of deskew.

Bt501
Bt502

ECL / TTL Octal Transceiver and Translator

Distinguishing Features

- 10KH or 100K ECL Compatible
- Optional Single +5 V Operation
- Separate TTL and ECL Supply Pins
- Three-Statable TTL Pins
- TTL-Compatible Control Inputs
- 24-pin 0.3" DIP Package
- Typical Power Dissipation: 800 mW

Benefits

- Flexible Power Supply
- Reduced Component Count
- Simplifies PCB Layout
- Reduces PCB Interconnect
- Low Bus Loading

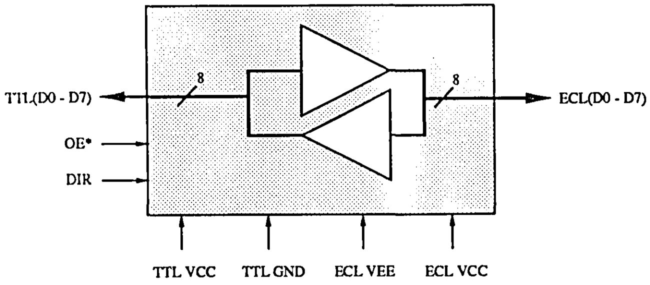
Product Description

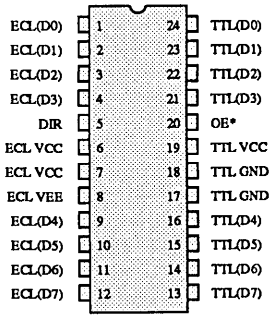
The Bt501 and Bt502 are octal ECL/TTL bidirectional transceivers and translators. The Bt501 is 10KH ECL compatible, and the Bt502 is 100K ECL compatible.

The direction and output enable control inputs are TTL compatible to simplify interfacing to a standard MPU.

Both devices provide a bidirectional interface between TTL signals and ECL signals. The ECL input/output signals may be generated from normal ECL, single +5 V, or split ECL supplies.

Functional Block Diagram


TTL(D0 - D7)
8
8
ECL(D0 - D7)
OE*
DIR
TTL VCC
TTL GND
ECL VEE
ECL VCC


ECL(D0) 1
ECL(D1) 2
ECL(D2) 3
ECL(D3) 4
DIR 5
ECL VCC 6
ECL VCC 7
ECL VEE 8
ECL(D4) 9
ECL(D5) 10
ECL(D6) 11
ECL(D7) 12
24 TTL(D0)
23 TTL(D1)
22 TTL(D2)
21 TTL(D3)
20 OE*
19 TTL VCC
18 TTL GND
17 TTL GND
16 TTL(D4)
15 TTL(D5)
14 TTL(D6)
13 TTL(D7)

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L501001 Rev. F

Brooktree®

Circuit Description

Supply Pin	Nominal Voltages Applied Single Supply System	Dual Supply System	Split ECL Supply System
TTL VCC	+5.0 V	+5.0 V	+5.0 V
TTL GND	0 V	0 V	0 V
ECL VCC	+5.0 V	0 V	+ 2.0 V
ECL VEE	0 V	–5.2 V	–3.2 V

Bt501 Supply Operation.

Supply Pin	Nominal Voltages Applied Single Supply System	Dual Supply System	Split ECL Supply System
TTL VCC	+5.0 V	+5.0 V	+5.0 V
TTL GND	0 V	0 V	0 V
ECL VCC	+5.0 V	0 V	+ 2.0 V
ECL VEE	0 V	–4.5 V	–2.5 V

Bt502 Supply Operation.

Note: The TTL (D0–D7), DIR, and OE* pins are TTL compatible regardless of the ECL power supply parameters. Changing the ECL power supply parameters affects the threshold levels of only the ECL (D0–D7) pins.

DIR	OE*	Function
0	0	TTL (D0–D7) --> ECL (D0–D7)
1	0	ECL (D0–D7) --> TTL (D0–D7)
x	1	TTL (D0–D7) three-stated, ECL (D0–D7) = 0

Control Truth Table.

Bt501—Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
TTL Device Ground	TTL GND	0	0	0	Volts
ECL Device Ground	ECL VCC	0	0	0	Volts
TTL Power Supply	TTL VCC	+4.75	+5.0	+5.25	Volts
ECL Power Supply	ECL VEE	–4.9	–5.2	–5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Bt501—Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
ECL VEE (measured to ECL VCC)				–8.0	Volts
TTL VCC (measured to TTL GND)				+7.0	Volts
Voltage on Any ECL Pin		ECL VCC		ECL VEE	Volts
Voltage on Any TTL Pin		TTL GND –0.5		TTL VCC +0.5	Volts
ECL(D0–D7) Output Current				–50	mA
TTL(D0–D7) Short Circuit Output Current	IOS	–50		–150	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Bt501—ECL DC Characteristics

Parameter	Symbol	TA (°C)	Min	Typ	Max	Units
Input High Voltage*	VIH	0 +25 +70	−1170 −1130 −1070		−840 −810 −735	mV mV mV
Input Low Voltage*	VIL	0 +25 +70	−1950 −1950 −1950		−1480 −1480 −1450	mV mV mV
Output High Voltage*	VOH	0 +25 +70	−1020 −980 −920		−840 −810 −735	mV mV mV
Output Low Voltage*	VOL	0 +25 +70	−1950 −1950 −1950		−1630 −1630 −1600	mV mV mV
Input High Current (Vin = VIHmax)	IIH	0 +25 +70			10 10 10	µA µA µA
ECL VEE Supply Current	IEE	0 +25 +70			75 75 75	mA mA mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL (D0–D7) loading of 50 Ω to −2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Relative to ECL VCC.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Bt501—TTL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage*	VIH	2.0		TTL VCC +0.5	Volts
Input Low Voltage*	VIL	TTL GND −0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			70	μA
Input Low Current (Vin = 0.4 V)	IIL			−0.7	mA
Output High Voltage* (IOH = −2.0 mA)	VOH	2.5			Volts
Output Low Voltage* (IOL = 20 mA)	VOL			0.5	Volts
Three-State Output Current	IOZ				
Vout = VOHmin				10	μA
Vout = VOLmax				−10	μA
TTL VCC Supply Current	ICC			85	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL (D0–D7) loading of 50 Ω to −2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

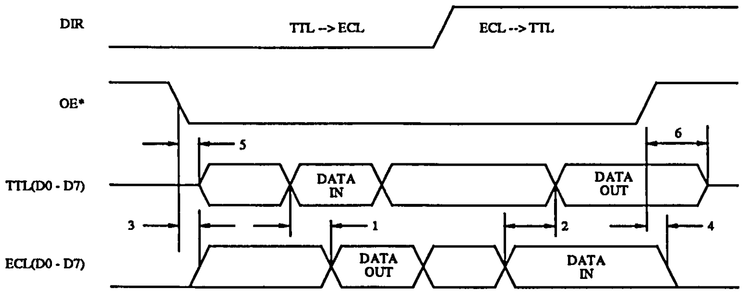
*Relative to TTL GND.

Bt501—AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL --> ECL Propagation Delay	1	2		7	ns
ECL --> TTL Propagation Delay	2	5		11	ns
ECL (D0–D7) Enable Time	3	7		13	ns
ECL (D0–D7) Disable Time*	4	7		13	ns
TTL (D0–D7) Enable Time	5	4		10	ns
TTL (D0–D7) Disable Time*	6	6		12	ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL (D0–D7) loading of 50 Ω to –2.0 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are –0.80 to –2.0 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Subject to capacitive loading.



Input/Output Timing.

Bt502—Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
TTL Device Ground	TTL GND	0	0	0	Volts
ECL Device Ground	ECL VCC	0	0	0	Volts
TTL Power Supply	TTL VCC	+4.75	+5.0	+5.25	Volts
ECL Power Supply	ECL VEE	–4.2	–4.5	–4.8	Volts
Ambient Operating Temperature	TA	0		+85	°C

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Bt502—Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
ECL VEE (measured to ECL VCC)				–8.0	Volts
TTL VCC (measured to TTL GND)				+7.0	Volts
Voltage on Any ECL Pin		ECL VCC		ECL VEE	Volts
Voltage on Any TTL Pin		TTL GND –0.5		TTL VCC +0.5	Volts
ECL (D0–D7) Output Current				–50	mA
TTL (D0–D7) Short Circuit Output Current	IOS	–50		–150	mA
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Bt502—ECL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage*	VIH	–1165		–880	mV
Input Low Voltage*	VIL	–1810		–1475	mV
Output High Voltage*	VOH	–1025	–955	–880	mV
Output Low Voltage*	VOL	–1810	–1705	–1620	mV
Input High Current (Vin = VIH max)	IIH			10	µA
ECL VEE Supply Current	IEE			75	mA

Bt502—TTL DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input High Voltage**	VIH	2.0		TTL VCC +0.5	Volts
Input Low Voltage**	VIL	TTL GND –0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			70	µA
Input Low Current (Vin = 0.4 V)	IIL			–0.7	mA
Output High Voltage** (IOH = –2.0 mA)	VOH	2.5			Volts
Output Low Voltage** (IOL = 20 mA)	VOL			0.5	Volts
Three-State Output Current	IOZ				
Vout = VOHmin				10	µA
Vout = VOLmax				–10	µA
TTL VCC Supply Current	ICC			85	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL (D0–D7) loading of 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Relative to ECL VCC.
**Relative to TTL GND.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

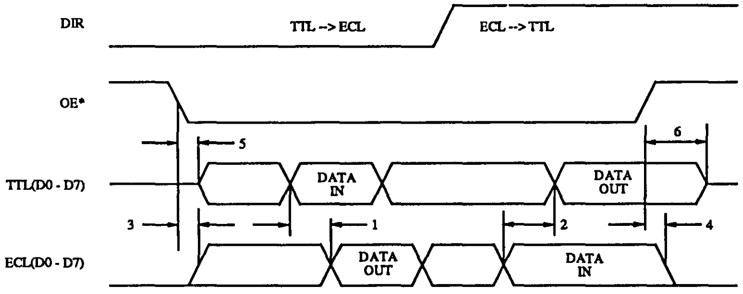
Bt502—AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL --> ECL Propagation Delay*	1	0.5		7	ns
ECL --> TTL Propagation Delay*	2	2		11	ns
ECL (D0–D7) Enable Time	3	2		11	ns
ECL (D0–D7) Disable Time*	4	3		11	ns
TTL(D0–D7) Enable Time	5	0.5		6.5	ns
TTL(D0–D7) Disable Time*	6	0.5		6.5	ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with ECL(D0–D7) loading of 50 Ω to –2.0 V. TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. ECL input values are –0.80 to –2.0 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Ordering Information

Model Number	Compatibility	Package	Ambient Temperature Range
Bt501KC	10KH ECL	24-pin 0.3" CERDIP	0° to +70° C
Bt502KC	100K ECL	24-pin 0.3" CERDIP	0° to +85° C



Input/Ouput Timing.

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt604

125 MHz
10KH ECL Compatible Dynamically Programmed Timing Edge Vernier

Distinguishing Features

- 125 MHz Maximum Trigger Rate
- Less than ±1 LSB Timing Accuracy
- 15 ps Delay Resolution (4 ns Span)
- Extendable Delay Span to 40 ns
- Differential Trigger Inputs
- 10KH ECL Compatible
- Monolithic Construction
- 28-pin Plastic J-Lead (PLCC) Package
- Typical Power Dissipation: 910 mW

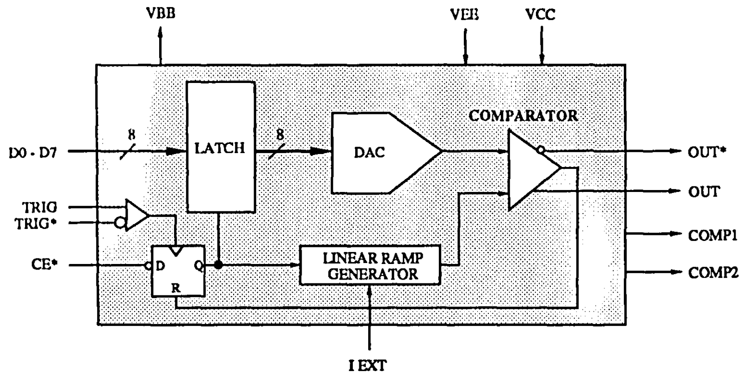
Applications

- Automatic Test Equipment
- Precision Timing Verniers
- Arbitrary Waveform Generators
- Multiple Phase Clock Generators
- Computer Backplane Timing

Related Products

- Bt605

Functional Block Diagram



Product Description

The Bt604 is a Dynamically Programmed Timing Edge Vernier, whose time delay is dynamically loaded upon each trigger of the circuit. In response to a trigger pulse, the Bt604 outputs a pulse of fixed width a programmable delay time later.

With the delay span set to 4 ns, the Bt604 features 15 ps of resolution (255 steps). The delay span is externally adjusted and is set in the range of 4 ns to 40 ns by IEXT.

The device is 10KH ECL compatible with ECL inputs and has a differential ECL input trigger and output pulse.

In applications for Automatic Test Equipment (ATE), the Bt604 forms the critical component in providing precise timing edges having fine resolution and excellent edge placement accuracy, and is suitable for use in testers featuring timing changes "on-the-fly."

The Bt604 also meets the need for programmable time delays in numerous electronic instruments that perform signal modulation, processing, and generation.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L604001 Rev. F

Brooktree®

Circuit Description

As illustrated in the block diagram, the Bt604 contains an 8-bit D/A converter, a linear ramp generator, and a comparator.

Functional Operation

Referring to Figures 1 and 2, if CE* is a logical zero, the differential input trigger (TRIG, TRIG*) initiates a linear ramp on the rising edge of TRIG and latches the D0–D7 input data which sets the DAC output voltage.

The comparator detects when the ramp reaches the DAC's programmed value, whereupon it initiates an output pulse of fixed width and resets the ramp. Upon resetting the ramp, the input data latch is made transparent, enabling D0–D7 to reprogram the DAC and permitting another trigger of the Bt604.

Delay Calculations

Referring to Figure 2, the output pulse delay consists of a minimum output delay (Tmin) and a programmable output delay (Tprog). For D0–D7 equal to $00 the output delay will be Tmin and for $FF the output delay will be Tmax.

The span of the delay range is:

$$\text{Tspan} = \text{Tmax} - \text{Tmin}$$

The output pulse delays are adjustable and are set by IEXT current flow through pin 12. Figure 3 shows the relationships Tspan vs. IEXT and Tspan vs. Tmin. The following equations apply to Figure 3:

$$\text{Tmin (max)} = \text{Tspan} * 0.217 + 2.7$$
$$\text{Tmin (min)} = \text{Tspan} * 0.187 + 1.6$$
$$\text{Tmin (max)} - \text{Tmin (min)} = \text{Tspan} * 0.03 + 1.1$$

Referring to Figure 4:

$$\text{IEXT} = (\text{VEXT} + 1.25\ \text{V}) / (\text{REXT} + 26\ \Omega)$$

Output Pulse Spacing

Consecutive output pulses must be spaced no less than 8 ns apart.

Conditions for Optimum Performance

The timing vernier is a mixed signal device and to obtain the maximum accuracy and stability over frequency there are specific conditions required. The following recommendations are for maintaining the lowest linearity errors and minimizing the absolute timing variations over frequency.

This product requires special attention to proper layout techniques to achieve correct operations. Before beginning PCB layout, please reference the ECL layout techniques in *Bt604/605/606 Evaluation Module Operation and Measurements* (AN-17), found in Brooktree's 1990 Applications Handbook.

Do not expect optimum performance when operating the device in a socket. Lead inductance, transmission line discontinuities and restricted air flow attributable to the use of a socket will degrade performance.

A transverse air flow of 400 linear feet per minute is very important when considering error sources in the magnitude of tens of picoseconds.

The ferrite chip bead selected for use with this device is critical. Use only the bead recommended. It is very important that this bead be mounted as close as possible to the VEE(1) power pins connecting the device to the power plane as illustrated in Figure 4. Connecting the decoupling capacitors directly to the VEE(1) pins will result in unstable operation.

Note that all components must be placed as close to the pins as possible, and that all VCC pins must be connected together.

The data set-up time for trigger of the device should be extended to 5 ns for on-the-fly applications. This will insure the best dynamic performance when making full-scale transitions from code $FF to $00, which is when the worst case settling time conditions occur.

A constant trigger pulse width should be maintained to achieve the best absolute time performance over frequency. A trigger pulse width of Tmin – 500 ps is required to keep the falling edge of the trigger pulse width from occurring during the ramp.

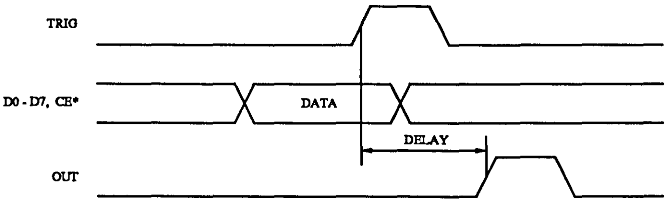


Figure 1. Input/Output Timing.

Circuit Description (continued)

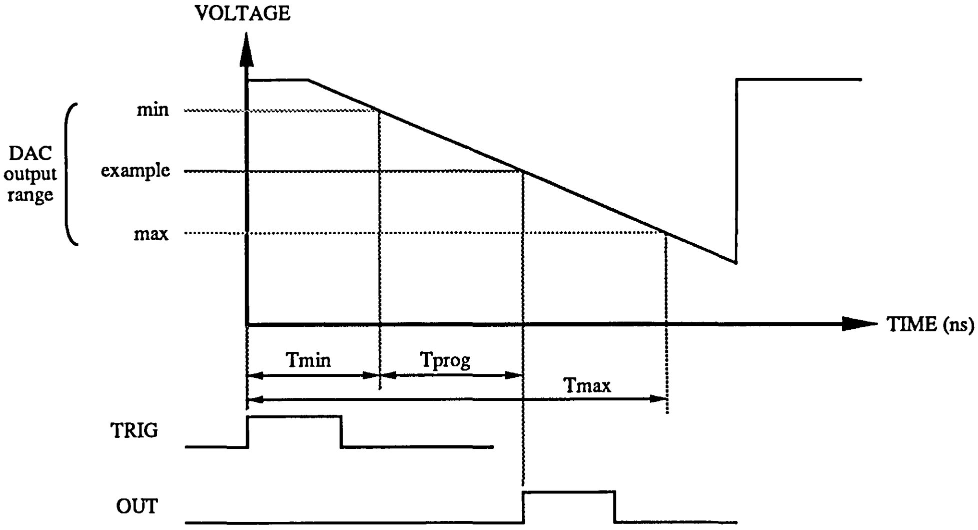

VOLTAGE
DAC output range
min
example
max
TIME (ns)
Tmin
Tprog
Tmax
TRIG
OUT

Figure 2. Linear Ramp and Output Pulse Timing.

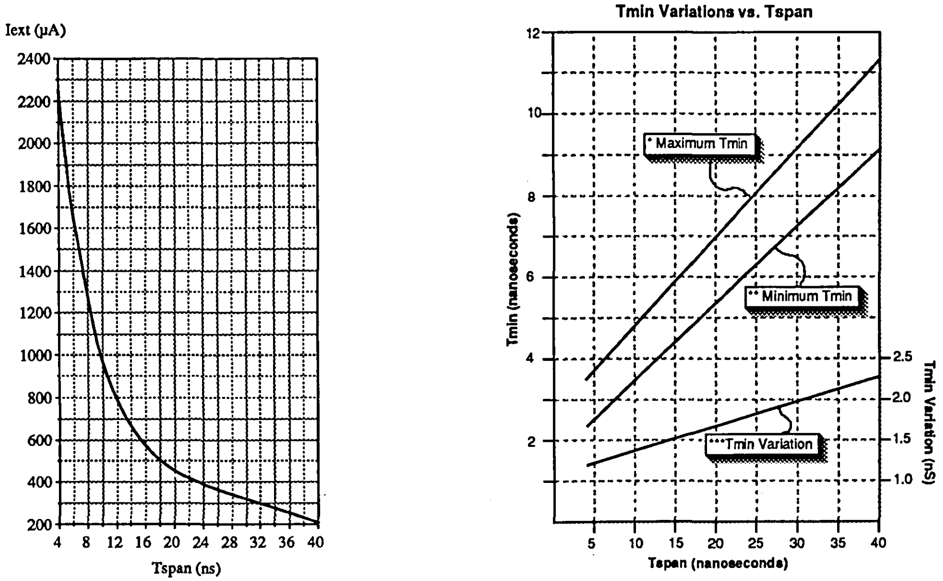
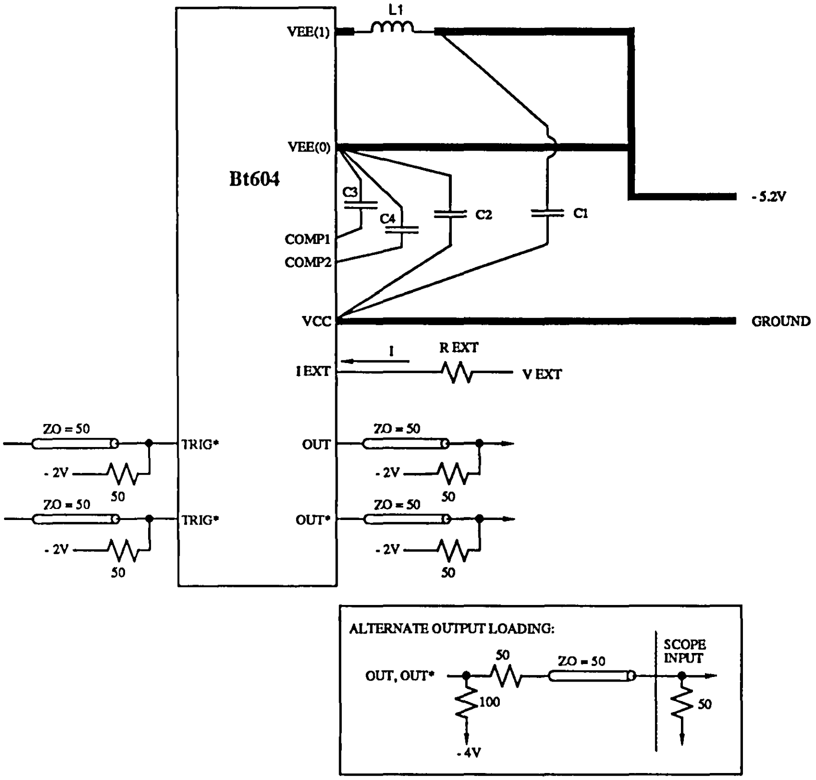


Figure 3. Typical Output Delays.

Circuit Description (continued)


L1
VEE(1)
VEE(0)
Bt604
C3
C4
C2
C1
-5.2V
COMP1
COMP2
VCC
GROUND
I
R EXT
I EXT
V EXT
ZO = 50
TRIG*
-2V
50
ZO = 50
TRIG*
-2V
50
OUT
ZO = 50
-2V
50
OUT*
ZO = 50
-2V
50
ALTERNATE OUTPUT LOADING:
OUT, OUT*
50
100
-4V
ZO = 50
SCOPE INPUT
50

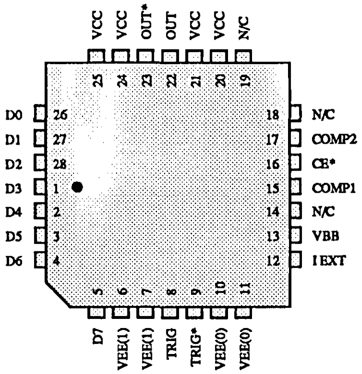
Location	Description	Vendor Part Number
C1–C4	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
L1	ferrite chip bead	TDK HF70ACB322513 or TDK CB301210
REXT	1% metal film resistor (selected for proper Tspan)	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt604. All devices should be as close as possible to the Bt604.

Figure 4. Typical Connection Diagram and Parts List.

Pin Descriptions

Pin Name	Description
D0–D7	Data input pins (ECL compatible). On the rising edge of TRIG, a ramp is initiated whereupon D0–D7 are latched into the device. D0 is the LSB. These inputs specify the amount of delay from the rising edge of TRIG to the output pulse. See Figure 1.
CE*	Chip enable input (ECL compatible). CE* must be a logical zero on the rising edge of the TRIG to enable the device to respond to the trigger. If CE* is floating, the trigger will always be enabled. See Figure 1.
TRIG, TRIG*	Differential trigger inputs (ECL compatible). The rising edge of TRIG is used to trigger the delay cycle if CE* is a logical zero. If CE* is a logical one, no operation occurs. It is recommended that triggering be performed using differential inputs.
OUT, OUT*	Differential outputs (ECL compatible).
IEXT	Current reference pin. The amount of current sourced into this pin determines the span of output delay. The voltage at IEXT is typically –1.25 V.
COMP1, COMP2	Compensation pins. A 0.1 µF ceramic capacitor must be connected between COMP1 and VEE(0) and also COMP2 and VEE(0). See Figure 4.
VEE	Device power. All VEE pins must be connected. **Warning: It is important that a ferrite chip bead be used to connect the VEE(1) power pins to the power plane as illustrated in Figure 4. Connecting the decoupling capacitors directly to the VEE(1) pins will result in unstable operation.**
VCC	Device ground. All VCC pins must be connected together.
VBB	–1.36 V (typical) output.



Note: N/C pins may be left floating without affecting the performance of the Bt604.

Application Information

Introduction

The Bt604 Timing Edge Vernier uses an external current source to set and calibrate the time delay span, Tspan. This section describes how Tspan may be set using external resistors and how an external diode may be used to improve, by a factor of approximately 3:1, the effects of temperature variations.

In applications where the output time delay may be measured, Tspan may be automatically calibrated using an external programmable current source. Also described is how this can be achieved in a cost effective manner using Brooktree's Bt110 CMOS Octal 8-bit DAC.

Tspan Temperature Compensation

The Bt604 exhibits small changes in Tspan with changes in temperature caused by temperature coefficient differences between the minimum time delay (Tmin) and the maximum time delay (Tmax), where:

$$\text{Tspan} = \text{Tmax} - \text{Tmin}$$

Tspan is set with an external current source (usually a resistor to a voltage VEXT) as shown in Figure 4. The Tspan positive temperature coefficient can be partially compensated with an external network exhibiting a negative temperature coefficient consisting of two resistors and an inexpensive 1N4148 diode (see Figure 5). Resistors R1 and R2 are selected from Table 1 according to the Tspan desired. R1 and R2 are metal film resistors. R2 is selected or trimmed to obtain the desired Tspan.

The 2 mV/°C decrease in the forward voltage drop across the diode provides the necessary small changes in current. This network is most effective over a temperature range of 40 to 60 °C. Also shown in Table 1 are the temperature coefficients that can be expected over this temperature range for a 10° change in temperature. This is not a linear function in all cases. For example, with a 5 ns Tspan, Tmin may decrease from 40 to 50 °C, and then increase from 50 to 60 °C. As a result, values shown are absolute values.

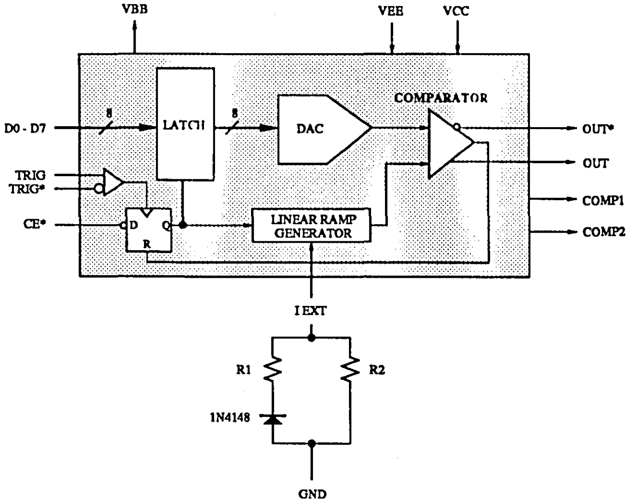


Figure 5. Typical Temperature Compensation Circuit.

Application Information (continued)

Tspan Calibration Using the Bt110

The accuracy and stability of the circuit providing the reference current (IEXT) directly affects the timing span accuracy. Computing values for R1 and R2 in Figure 5 results in a Tspan accuracy of better than ±20%. This may require the adjustment or trimming of R2 to set Tspan to the precision required by the application. Using the Bt110 CMOS Octal 8-bit DAC can eliminate the need to trim resistors and provides a cost-effective, low-power solution to Tspan calibration. The block diagram of the Bt110 is shown in Figure 6.

For example, the Bt604 requires a nominal external current of 1850 μA for a Tspan of 5 ns. When the span is set to 5 ns, the Tspan/IEXT ratio is typically 2.80 ps/μA. Setting Tspan with resistor values as per Table 1 could result in a Tspan error of ±20%, or ±1 ns. To correct for this error would require an adjustment of IEXT of ±1 ns divided by 0.0028 ns/μA or ±357 μA. If this IEXT adjustment is to be supplied by a DAC, then the full-scale range would need to be 2 x 357 = 714 μA. An 8-bit DAC with this range would have a calibration resolution of 714 μA divided by 255 or 2.8 μA per bit. This represents a calibration resolution of 2.8 μA times 2.8 ps/μA or 7.84 ps.

This can be stated more simply as:

- Setting Tspan with resistors results in an error of ±x%
- The Bt604 has 8 bits of resolution
- Calibrating with an 8-bit DAC results in a calibration resolution of 2x% of 1 LSB of the Bt604
- For Tspan = 5 ns
  1 LSB = 5 ns/255 = 19.6 ns
  Calibration resolution for ±x = ±20% is
  0.4 x 19.6 = 7.84 ps

The circuit shown in Figure 7 implements this using the Brooktree Bt110 CMOS Octal 8-bit DAC. Resistor R5 provides a voltage drop so that the ±1 V compliance range of the Bt110 is not exceeded; variations in R5 have no effect on IEXT.

The output range of the Bt110 is set by R6:

Range (μA) = 1000*VREF (V) / R6 (Ω)

where VREF into the Bt110 may be set by the internal 1.2v reference of the Bt110. Using this internal reference, the full-scale gain error of the Bt110 is ±10%. Table 2 shows resistor values for the circuit in Figure 7.

As the Bt110 has eight 8-bit DACs, it is capable of calibrating up to eight Bt604s.

Tspan (ns)	R1 (Ω)	R2 (Ω)	Tmin Tempco (ps/°C)	Tmax Tempco (ps/°C)	Tspan Tempco (ps/°C)
5	1000	1154	2.5	2.5	1.0
10	2000	2411	2.5	2.5	1.0
15	3300	3569	2.5	2.5	2.0
20	4700	4590	4.0	4.0	2.0

Table 1. Component Values for Figure 5.

Application Information (continued)

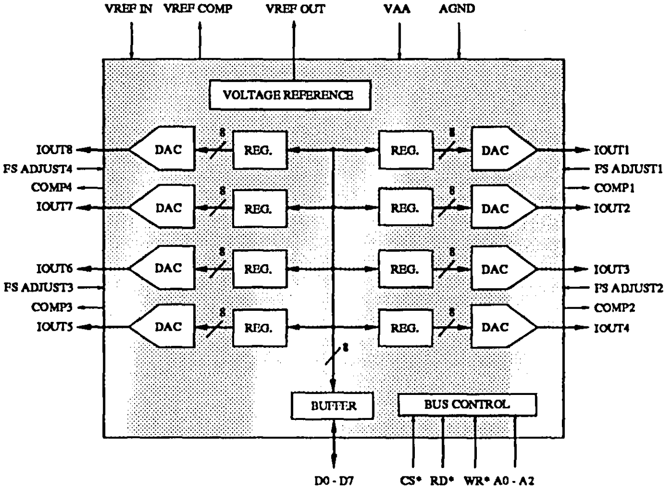

VREF IN
VREF COMP
VREF OUT
VAA
AGND
VOLTAGE REFERENCE
DAC
REG.
8
IOUT8
FS ADJUST4
COMP4
IOUT7
IOUT6
FS ADJUST3
COMP3
IOUT5
IOUT1
FS ADJUST1
COMP1
IOUT2
IOUT3
FS ADJUST2
COMP2
IOUT4
BUFFER
BUS CONTROL
D0 - D7
CS*
RD*
WR*
A0 - A2

Figure 6. Block Diagram of the Bt110 Octal 8-Bit DAC.

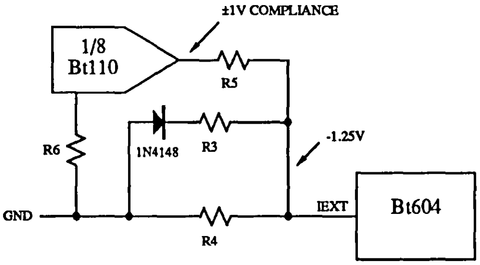

±1V COMPLIANCE
1/8
Bt110
R5
R6
1N4148
R3
-1.25V
IEXT
Bt604
GND
R4

Figure 7. Tspan Calibration Using the Bt110.

Tspan (ns)	R3 (Ω)	R4 (Ω)	R5 (Ω)	R6 (Ω)	Nominal Range of Bt110 DAC (μA)
5	1000	1200	2500	1500	800
10	2000	2700	4500	2660	450
15	3300	3900	8100	4800	250
20	4700	4700	17000	10000	120

Table 2. Component Values for Figure 6.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	VCC	0	0	0	Volts
Power Supply	VEE	–4.9	–5.2	–5.5	Volts
Reference Current	IEXT	150		2500	µA
Ambient Operating Temperature	TA	0		+70	°C

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (measured to VCC)				-8.0	Volts
Voltage on Any Digital Pin		0		VEE	Volts
Output Current				-30	mA
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	TA (°C.)	Min	Typ	Max	Units
Input High Voltage	VIH	0 +25 +70	-1170 -1130 -1070		-840 -810 -735	mV mV mV
Input Low Voltage	VIL	0 +25 +70	-1950 -1950 -1950		-1480 -1480 -1450	mV mV mV
Output High Voltage	VOH	0 +25 +70	-1020 -980 -920		-840 -810 -735	mV mV mV
Output Low Voltage	VOL	0 +25 +70	-1950 -1950 -1950		-1630 -1630 -1600	mV mV mV
Input High Current (Vin = VIH max) TRIG, TRIG*	IIH IIH	FULL FULL			20 30	µA µA
Input Low Current (Vin = VIL min) TRIG, TRIG*	IIL IIL	FULL FULL			20 25	µA µA
Output Delay Spans Differential Linearity Error** Integral Linearity Error**	 DL IL	 FULL +25°–70° 0°			 ±0.9 ±1.0 ±1.25	 LSB LSB LSB
VBB Output Voltage	VBB	FULL	-1.44		-1.30	Volts
IEXT for Tspans Tspan = 4 ns Tspan = 5 ns Tspan = 10 ns Tspan = 15 ns Tspan = 20 ns Tspan = 30 ns	 IEXT	 FULL	 2.1 1.6 0.80 0.53 0.39 0.25		 2.65 2.1 1.05 0.70 0.52 0.34	 mA mA mA mA mA mA
Tspan with IEXT = 1.7 mA (Tspan = Tmax – Tmin)		 FULL	 4.9		 6.2	 ns
Minimum Delay Time* Data = 00, Tspan = 5 ns Tspan = 10 ns	 Tmin	 FULL	 2.5 3.5		 3.8 4.9	 ns ns
VEE Supply Current	IEE	70° 0°, 25°		180	200 210	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions". OUT and OUT* loading with 50 Ω to -2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note: The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

*For other minimum time delay values, refer to delay calculation equations in the Circuit Description section.
**Tested at 10 MHz trigger rate with span at 5 ns.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Trigger Rate (note 1)	Fmax			125	MHz
Trigger Width High	TWI	2			ns
Output Pulse Width High Time	TWO	2.5		4.5	ns
Output Pulse Rise/Fall Time (20/80%)			550	750	ps
Output Pulse Spacing	TS	8			ns
Minimum Delay Time vs. Tspan					
ΔT00 / ns (Tspan = 5 ns to 10 ns)		180		220	ps / ns
Output Delay					
Tspan (Tspan = Tmax – Tmin)		4		40	ns
Resolution (Tspan / 255)		15.7		157	ps
Tempco (5 ns Span)					
ΔTspan / °C			6		ps / °C
ΔTmin / °C			4		ps / °C
Power Supply Rejection (Data = 0-FF HEX, Tspan = 5 ns)			100		ps / V
CE* Setup Time	TSU	2.0			ns
CE* Hold Time	TH	1.5			ns
WRITE Pulse Width High Time	TWH	2			ns
D0–D7 Setup Time	TDSU	1			ns
D0–D7 Hold Time	TDH	1.5			ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions". ECL input values are –0.89 to –1.69 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. OUT and OUT* loading with 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note 1: Maximum Tspan and Trigger Rates:

Maximum Tspan (ns) Maintaining Linearity		Maximum Trigger Rate (MHz)	Minimum Trigger Period (ns)
of ±2 LSB	of ±1 LSB		
4.0	—	125	8
5.1	4.6	100	10
5.8	5.5	90	11.1
6.75	6.3	80	12.5
8.1	7.7	70	14.3
9.9	8.7	60	16.6
12.0	10.5	50	20.0
15.5	14.1	40	25.0
22.0	20.5	30	33.3

The information in this table is guaranteed but not 100% production tested.
See Figures 8 and 9 for a graphic representation.

AC Characteristics (continued)

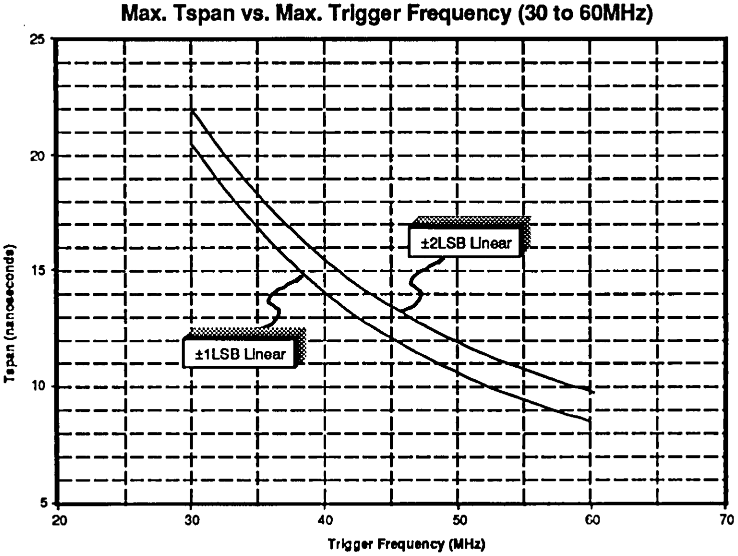


Figure 8. Bt604 Tspan vs. Frequency (30–60 MHz)

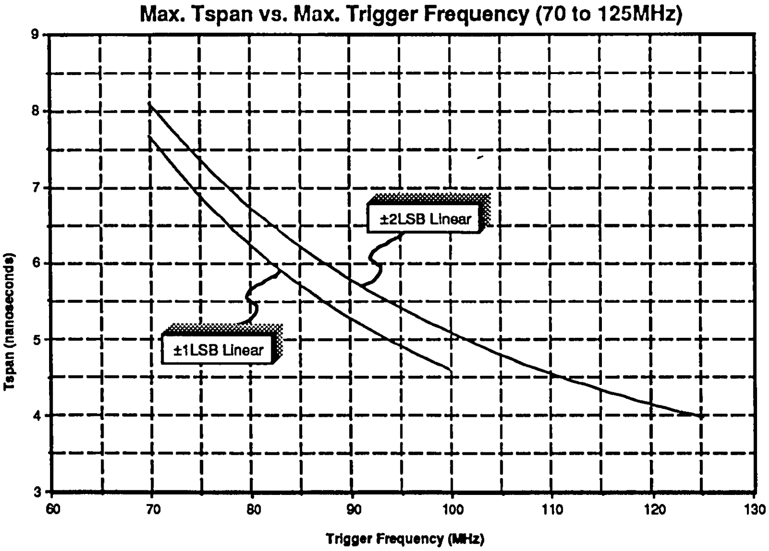
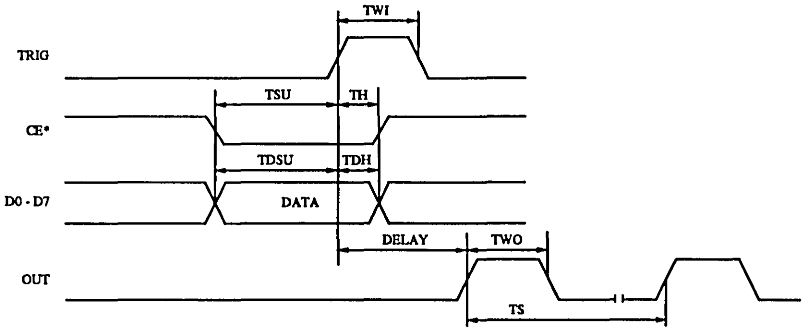


Figure 9. Bt604 Tspan vs. Frequency (70–125 MHz)

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt604KPJ	28-pin Plastic J-Lead	0° to +70° C

Timing Waveforms


TWI
TRIG
TSU
TH
CE*
TDSU
TDH
D0 - D7
DATA
DELAY
TWO
OUT
TS

Input/Output Timing.

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt605

125 MHz
10KH ECL Compatible Programmable Timing Edge Vernier

Distinguishing Features

- 125 MHz Maximum Trigger Rate
- Less than ±1 LSB Timing Accuracy
- 15 ps Delay Resolution (4 ns Span)
- Extendable Delay Span to 40 ns
- Differential Trigger Inputs
- 10KH ECL Compatible
- Monolithic Construction
- 28-pin Plastic J-Lead (PLCC) Package
- Typical Power Dissipation: 910 mW

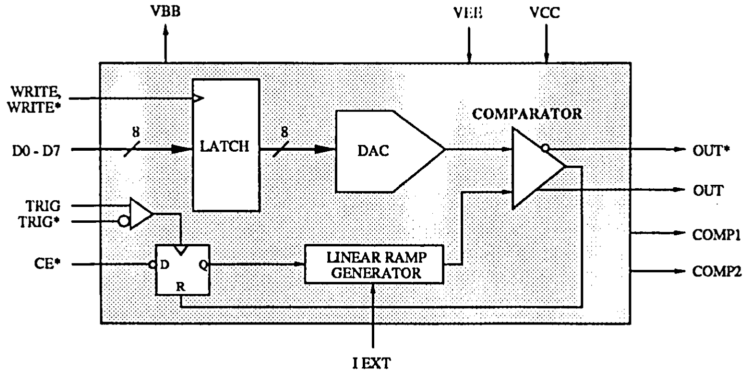
Applications

- Automatic Test Equipment
- Precision Timing Verniers
- Arbitrary Waveform Generators
- Multiple Phase Clock Generators
- Computer Backplane Timing

Related Products

- Bt604

Functional Block Diagram



Product Description

The Bt605 is a Programmable Timing Edge Vernier, whose time delay is loaded independently of triggering the circuit. In response to a trigger pulse, the Bt605 outputs a pulse of fixed width a programmable delay time later.

With the delay span set to 4 ns, the Bt605 features 15 ps of resolution (255 steps). The delay span is externally adjusted and is set in the range of 4 ns to 40 ns by IEXT.

Separate to triggering of the device, a new 8-bit value of delay is written in parallel (D0–D7).

The device is 10KH ECL compatible with ECL inputs and has a differential ECL input trigger, output pulse, and write input.

In applications for Automatic Test Equipment (ATE), the Bt605 forms the critical component in providing precise timing edges having fine resolution and excellent edge placement accuracy.

The Bt605 also meets the need for programmable time delays in numerous electronic instruments that perform signal modulation, processing, and generation.

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249

L605001 Rev. F

Brooktree®

Circuit Description

As illustrated in the block diagram, the Bt605 contains an 8-bit D/A converter, a linear ramp generator, and a comparator.

Functional Operation

Referring to Figures 1 and 2, the linear ramp determines the span of delay and the DAC's output sets the delay value. The programmed value of delay is written into the DAC input register via D0–D7 and WRITE.

If CE* is a logical zero, the differential input trigger (TRIG, TRIG*) initiates a linear ramp on the rising edge of TRIG. The comparator detects when the ramp reaches the DAC's programmed value, whereupon it initiates an output pulse of fixed width and resets the ramp. Resetting the ramp permits another trigger of the Bt605.

Delay Calculations

Referring to Figure 2, the output pulse delay consists of a minimum output delay (Tmin) and a programmable output delay (Tprog). For D0–D7 equal to $00 the output delay will be Tmin and for $FF the output delay will be Tmax.

The span of the delay range is:

$$\text{Tspan} = \text{Tmax} - \text{Tmin}$$

The output pulse delays are adjustable and are set by IEXT current flow through pin 12. Figure 3 shows the relationships Tspan vs. IEXT and Tspan vs. Tmin. The following equations apply to Figure 3:

$$\text{Tmin (max)} = \text{Tspan} * 0.217 + 2.7$$
$$\text{Tmin (min)} = \text{Tspan} * 0.187 + 1.6$$
$$\text{Tmin (max)} - \text{Tmin (min)} = \text{Tspan} * 0.03 + 1.1$$

Referring to Figure 4:

$$\text{IEXT} = (\text{VEXT} + 1.25\ \text{V}) / (\text{REXT} + 26\ \Omega)$$

Output Pulse Spacing

Consecutive output pulses must be spaced no less than 8 ns apart.

Conditions for Optimum Performance

The timing vernier is a mixed signal device and to obtain the maximum accuracy and stability over frequency there are specific conditions required to achieve maximum performance.

This product requires special attention to proper layout techniques to achieve correct operations. Before beginning PCB layout, please reference the ECL layout techniques in *Bt604/605/606 Evaluation Module Operation and Measurements* (AN-17), found in Brooktree's 1990 Applications Handbook.

Do not expect optimum performance when operating the device in a socket. Lead inductance, transmission line discontinuities and restricted air flow attributable to the use of a socket will degrade performance.

A transverse air flow of 400 linear feet per minute is very important when considering error sources in the magnitude of tens of picoseconds.

The ferrite chip bead selected for use with this device is critical. Use only the bead recommended. It is very important that this bead be mounted as close as possible to the VEE(1) power pins connecting the device to the power plane as illustrated in Figure 4. Connecting the decoupling capacitors directly to the VEE(1) pins will result in unstable operation.

Note that all components must be placed as close to the pins as possible, and that all VCC pins must be connected together.

A constant trigger pulse width should be maintained to achieve the best absolute time performance over frequency. A trigger pulse width of Tmin – 500 ps is required to keep the falling edge of the trigger pulse width from occurring during the ramp.

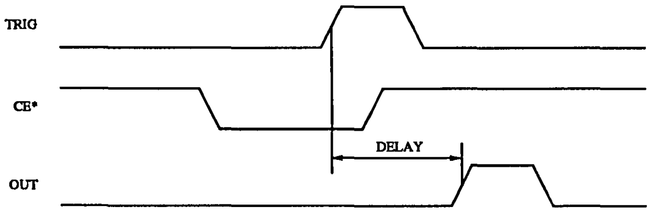


Figure 1. Delay Timing.

Circuit Description (continued)

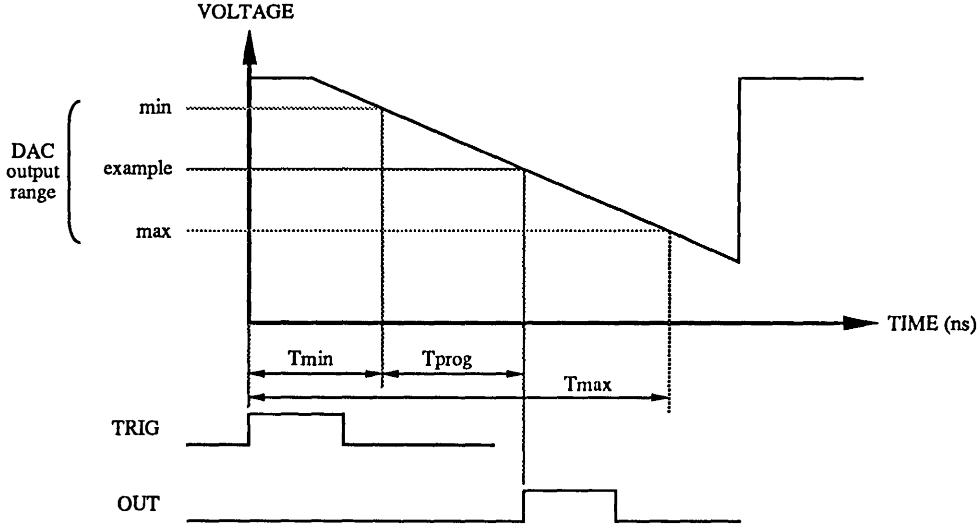

VOLTAGE
DAC output range
min
example
max
TIME (ns)
Tmin
Tprog
Tmax
TRIG
OUT

Figure 2. Linear Ramp and Output Pulse Timing.

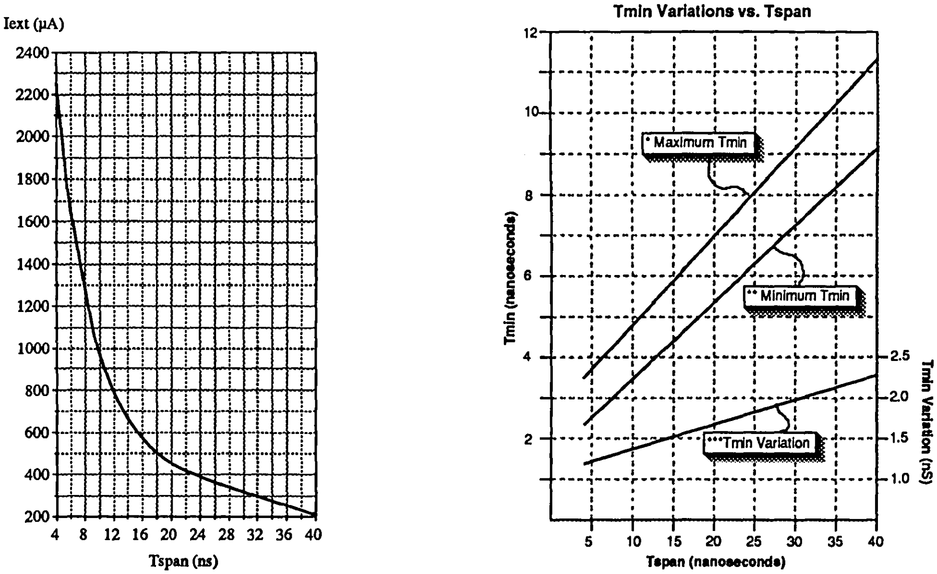
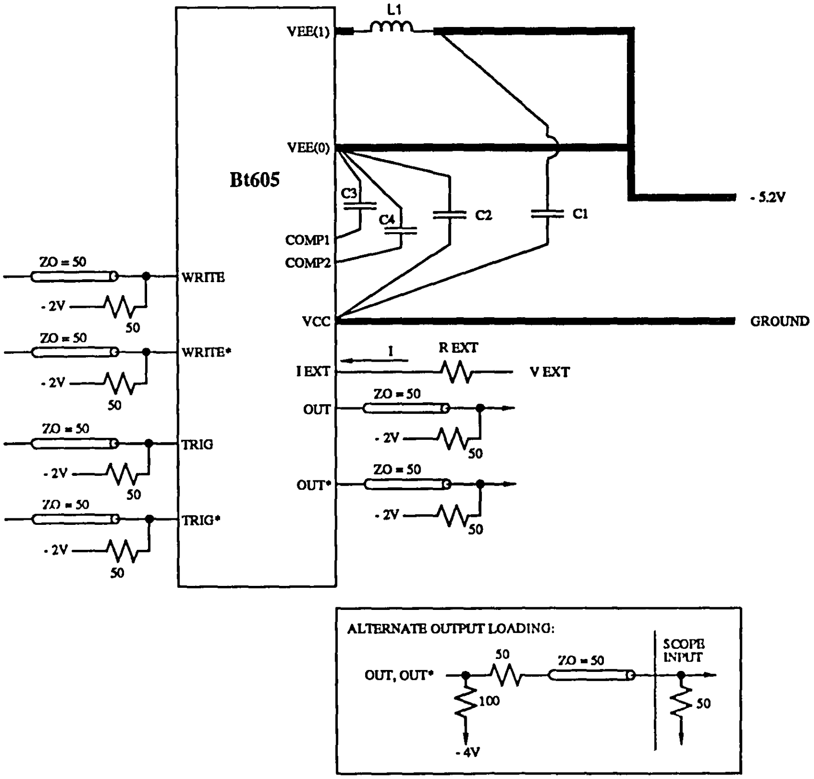


Figure 3. Typical Output Delays.

Circuit Description (continued)


L1
VEE(1)
VEE(0)
Bt605
C3
C4
C2
C1
COMP1
COMP2
- 5.2V
VCC
GROUND
I
R EXT
I EXT
V EXT
ZO = 50
OUT
- 2V
50
ZO = 50
OUT*
- 2V
50
ZO = 50
WRITE
- 2V
50
ZO = 50
WRITE*
- 2V
50
ZO = 50
TRIG
- 2V
50
ZO = 50
TRIG*
- 2V
50
ALTERNATE OUTPUT LOADING:
OUT, OUT*
50
100
- 4V
ZO = 50
SCOPE INPUT
50

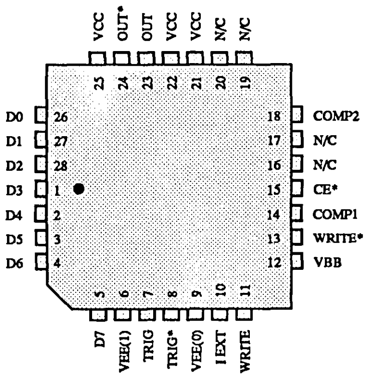
Location	Description	Vendor Part Number
C1–C4	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
L1	ferrite chip bead	TDK HF70ACB322513 or TDK CB301210
REXT	1% metal film resistor (selected for proper Tspan)	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt605. All devices should be as close as possible to the Bt605.

Figure 4. Typical Connection Diagram and Parts List.

Pin Descriptions

Pin Name	Description
D0–D7	Data input pins (ECL compatible). On the falling edge of WRITE, D0–D7 are latched into the DAC input register. D0 is the LSB. These inputs specify the amount of delay from the rising edge of TRIG to the output pulse.
WRITE, WRITE*	Differential write inputs (ECL compatible). These inputs control the parallel data input latch. When WRITE is a logical one, the data latch is transparent. Data is latched on the falling edge of WRITE. A single-ended write may be used by connecting WRITE* to VBB.
CE*	Chip enable input (ECL compatible). CE* must be a logical zero on the rising edge of TRIG to enable the device to respond to the trigger. If CE* is floating, the trigger will always be enabled.
TRIG, TRIG*	Differential trigger inputs (ECL compatible). The rising edge of TRIG is used to trigger the delay cycle if CE* is a logical zero. If CE* is a logical one, no operation occurs. It is recommended that triggering be performed using differential inputs.
OUT, OUT*	Differential outputs (ECL compatible).
IEXT	Current reference pin. The amount of current sourced into this pin determines the span of output delay. The voltage at IEXT is typically –1.25 V.
COMP1, COMP2	Compensation pins. A 0.1 µF ceramic capacitor must be connected between COMP1 and VEE(0) and also COMP2 and VEE(0). See Figure 4.
VEE	Device power. All VEE pins must be connected.
	Warning: It is important that a ferrite chip bead be used to connect the VEE(1) power pins to the power plane as illustrated in Figure 4. Connecting the decoupling capacitors directly to the VEE(1) pins will result in unstable operation.
VCC	Device ground. All VCC pins must be connected together.
VBB	–1.36 V (typical) output.



Note: N/C pins may be left floating without affecting the performance of the Bt605.

Application Information

Introduction

The Bt605 Timing Edge Vernier uses an external current source to set and calibrate the time delay span, Tspan. This section describes how Tspan may be set using external resistors and how an external diode may be used to improve, by a factor of approximately 3:1, the effects of temperature variations.

In applications where the output time delay may be measured, Tspan may be automatically calibrated using an external programmable current source. Also described is how this can be achieved in a cost effective manner using Brooktree's Bt110 CMOS Octal 8-bit DAC.

Tspan Temperature Compensation

The Bt605 exhibits small changes in Tspan with changes in temperature caused by temperature coefficient differences between the minimum time delay (Tmin) and the maximum time delay (Tmax), where:

$$\text{Tspan} = \text{Tmax} - \text{Tmin}$$

Tspan is set with an external current source (usually a resistor to a voltage VEXT) as shown in Figure 4. The Tspan positive temperature coefficient can be partially compensated with an external network exhibiting a negative temperature coefficient consisting of two resistors and an inexpensive 1N4148 diode (see Figure 5). Resistors R1 and R2 are selected from Table 1 according to the Tspan desired. R1 and R2 are metal film resistors. R2 is selected or trimmed to obtain the desired Tspan.

The 2 mV/°C decrease in the forward voltage drop across the diode provides the necessary small changes in current. This network is most effective over a temperature range of 40 to 60 °C. Also shown in Table 1 are the temperature coefficients that can be expected over this temperature range for a 10° change in temperature. This is not a linear function in all cases. For example, with a 5 ns Tspan, Tmin may decrease from 40 to 50 °C, and then increase from 50 to 60 °C. As a result, values shown are absolute values.

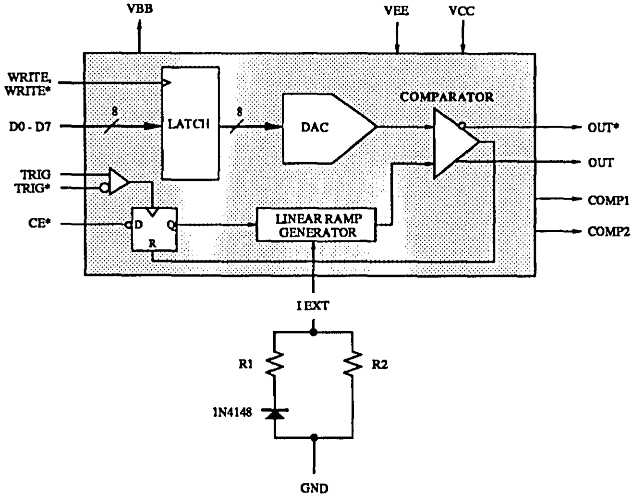


Figure 5. Typical Temperature Compensation Circuit.

Application Information (continued)

Tspan Calibration Using the Bt110

The accuracy and stability of the circuit providing the reference current (IEXT) directly affects the timing span accuracy. Computing values for R1 and R2 in Figure 5 results in a Tspan accuracy of better than ±20%. This may require the adjustment or trimming of R2 to set Tspan to the precision required by the application. Using the Bt110 CMOS Octal 8-bit DAC can eliminate the need to trim resistors and provides a cost-effective, low-power solution to Tspan calibration. The block diagram of the Bt110 is shown in Figure 6.

For example, the Bt605 requires a nominal external current of 1850 µA for a Tspan of 5 ns. When the span is set at 5 ns, the Tspan/IEXT ratio is typically 2.80 ps/µA. Setting Tspan with resistor values as per Table 1 could result in a Tspan error of ±20%, or ±1 ns. To correct for this error would require an adjustment of IEXT of ±1 ns divided by 0.0028 ns/µA or ±357 µA. If this IEXT adjustment is to be supplied by a DAC, then the full-scale range would need to be 2 x 357 = 714 µA. An 8-bit DAC with this range would have a calibration resolution of 714 µA divided by 255 or 2.8 µA per bit. This represents a calibration resolution of 2.8 µA times 2.8 ps/µA or 7.84 ps.

This can be stated more simply as:

- Setting Tspan with resistors results in an error of ±x%
- The Bt605 has 8 bits of resolution
- Calibrating with an 8-bit DAC results in a calibration resolution of 2x% of 1 LSB of the Bt605
- For Tspan = 5 ns
  1 LSB = 5 ns/255 = 19.6 ns
  Calibration resolution for ±x = ±20% is
  0.4 x 19.6 = 7.84 ps

The circuit shown in Figure 7 implements this using the Brooktree Bt110 CMOS Octal 8-bit DAC. Resistor R5 provides a voltage drop so that the ±1 V compliance range of the Bt110 is not exceeded; variations in R5 have no effect on IEXT.

The output range of the Bt110 is set by R6:

Range (µA) = 1000*VREF (V) / R6 (Ω)

where VREF into the Bt110 may be set by the internal 1.2 V reference of the Bt110. Using this internal reference, the full-scale gain error of the Bt110 is ±10%. Table 2 shows resistor values for the circuit in Figure 7.

As the Bt110 has eight 8-bit DACs, it is capable of calibrating up to eight Bt605s.

Tspan (ns)	R1 (Ω)	R2 (Ω)	Tmin Tempco (ps/°C)	Tmax Tempco (ps/°C)	Tspan Tempco (ps/°C)
5	1000	1154	2.5	2.5	1.0
10	2000	2412	2.5	2.5	1.0
15	3300	3569	2.5	2.5	2.0
20	4700	4590	4.0	4.0	2.0

Table 1. Component Values for Figure 5.

Application Information (continued)

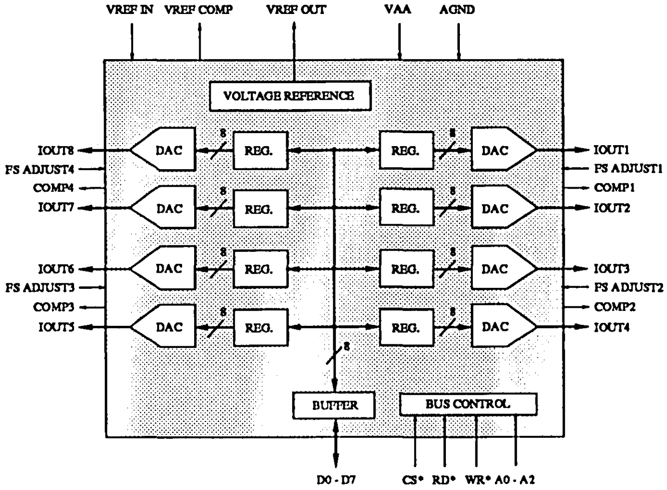

VREF IN
VREF COMP
VREF OUT
VAA
AGND
VOLTAGE REFERENCE
DAC
REG.
8
IOUT8
FS ADJUST4
COMP4
IOUT7
IOUT6
FS ADJUST3
COMP3
IOUT5
IOUT1
FS ADJUST1
COMP1
IOUT2
IOUT3
FS ADJUST2
COMP2
IOUT4
BUFFER
BUS CONTROL
D0 - D7
CS* RD* WR* A0 - A2

Figure 6. Block Diagram of the Bt110 Octal 8-Bit DAC.

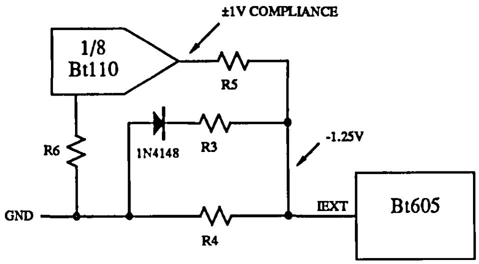

±1V COMPLIANCE
1/8
Bt110
R5
R6
1N4148
R3
-1.25V
GND
R4
IEXT
Bt605

Figure 7. Tspan Calibration Using the Bt110.

Tspan (ns)	R3 (Ω)	R4 (Ω)	R5 (Ω)	R6 (Ω)	Nominal Range of Bt110 DAC (μA)
5	1000	1200	2500	1500	800
10	2000	2700	4500	2660	450
15	3300	3900	8100	4800	250
20	4700	4700	17000	10000	120

Table 2. Component Values for Figure 6.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	VCC	0	0	0	Volts
Power Supply	VEE	–4.9	–5.2	–5.5	Volts
Reference Current	IEXT	150		2500	μA
Ambient Operating Temperature	TA	0		+70	°C

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (measured to VCC)				–8.0	Volts
Voltage on Any Digital Pin		0		VEE	Volts
Output Current				–30	mA
Ambient Operating Temperature	TA	-55		+125	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	TA (°C.)	Min	Typ	Max	Units
Input High Voltage	VIH	0	–1170		–840	mV
		+25	–1130		–810	mV
		+70	–1070		–735	mV
Input Low Voltage	VIL	0	–1950		–1480	mV
		+25	–1950		–1480	mV
		+70	–1950		–1450	mV
Output High Voltage	VOH	0	–1020		–840	mV
		+25	–980		–810	mV
		+70	–920		–735	mV
Output Low Voltage	VOL	0	–1950		–1630	mV
		+25	–1950		–1630	mV
		+70	–1950		–1600	mV
Input High Current (Vin = VIH max)	IIH	FULL			20	µA
TRIG, TRIG*	IIH	FULL			30	µA
Input Low Current (Vin = VIL min)	IIL	FULL			20	µA
TRIG, TRIG*	IIL	FULL			25	µA
Output Delay Spans						
Differential Linearity Error**	DL	FULL			±0.9	LSB
Integral Linearity Error**	IL	+25°–70°			±1.0	LSB
		0°			±1.25	LSB
VBB Output Voltage	VBB	FULL	–1.44		–1.30	Volts
IEXT for Tspans						
Tspan = 4 ns	IEXT	FULL	2.1		2.65	mA
Tspan = 5 ns			1.6		2.1	mA
Tspan = 10 ns			0.80		1.05	mA
Tspan = 15 ns			0.53		0.70	mA
Tspan = 20 ns			0.39		0.52	mA
Tspan = 30 ns			0.25		0.34	mA
Tspan with IEXT = 1.7 mA						
(Tspan = Tmax – Tmin)		FULL	4.9		6.2	ns
Minimum Delay Time*						
Data = 00, Tspan = 5 ns	Tmin	FULL	2.5		3.8	ns
Tspan = 10 ns			3.5		4.9	ns
VEE Supply Current	IEE	70°		180	200	mA
		0°, 25°			210	

Test conditions (unless otherwise specified): "Recommended Operating Conditions." OUT and OUT* loading with 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note: The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

*For other minimum time delay values, refer to delay calculation equations in the Circuit Description section.
**Tested at 10 MHz trigger rate with span at 5 ns.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Trigger Rate (note 1)	Fmax			125	MHz
Trigger Width High	TWI	2			ns
Output Pulse Width High Time	TWO	2.5		4.5	ns
Output Pulse Rise/Fall Time (20/80%)			550	750	ps
Output Pulse Spacing	TS	8			ns
Minimum Delay Time vs. Tspan					
ΔT00 / ns (Tspan = 5 ns to 10 ns)		180		220	ps / ns
Output Delay					
Tspan (Tspan = Tmax – Tmin)		4		40	ns
Resolution (Tspan / 255)		15.7		157	ps
Tempco (5 ns Span)					
ΔTspan / °C			6		ps / °C
ΔTmin / °C			4		ps / °C
Power Supply Rejection (Data = 0–FF HEX, Tspan = 5 ns)			100		ps / V
CE* Setup Time	TSU	2.0			ns
CE* Hold Time	TH	1.5			ns
WRITE Pulse Width High Time	TWH	2			ns
D0–D7 Setup Time	TDSU	1			ns
D0–D7 Hold Time	TDH	1.5			ns

Test conditions (unless otherwise specified): "Recommended Operating Conditions." ECL input values are –0.89 to –1.69 V, with input rise/fall times ≤ 2 ns, measured between the 20% and 80% points. Timing reference points at 50% for inputs and outputs. OUT and OUT* loading with 50 Ω to –2.0 V. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

Note 1: Maximum Tspan and Trigger Rates:

Maximum Tspan (ns) Maintaining Linearity		Maximum Trigger Rate (MHz)	Minimum Trigger Period (ns)
of ±2 LSB	of ±1 LSB		
4.0	—	125	8
5.1	4.6	100	10
5.8	5.5	90	11.1
6.75	6.3	80	12.5
8.1	7.7	70	14.3
9.9	8.7	60	16.6
12.0	10.5	50	20.0
15.5	14.1	40	25.0
22.0	20.5	30	33.3

The information in this table is guaranteed but not 100% production tested.
See Figures 8 and 9 for a graphic representation.

AC Characteristics (continued)

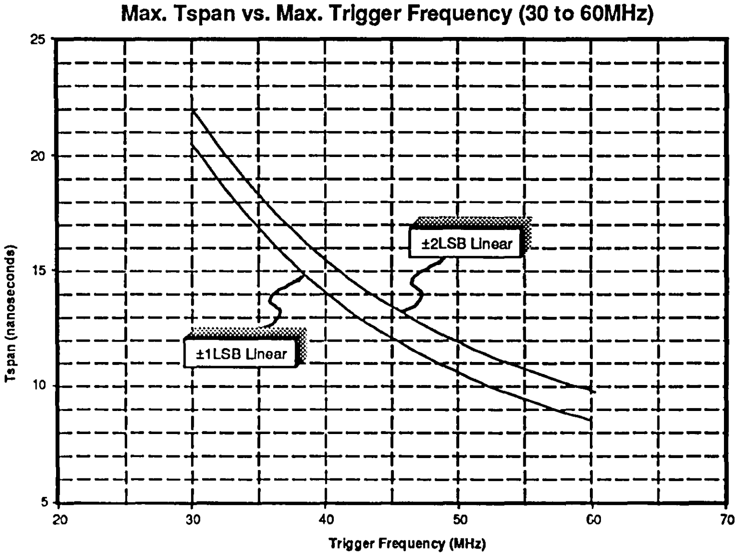


Figure 8. Bt605 Tspan vs. Frequency (30–60 MHz).

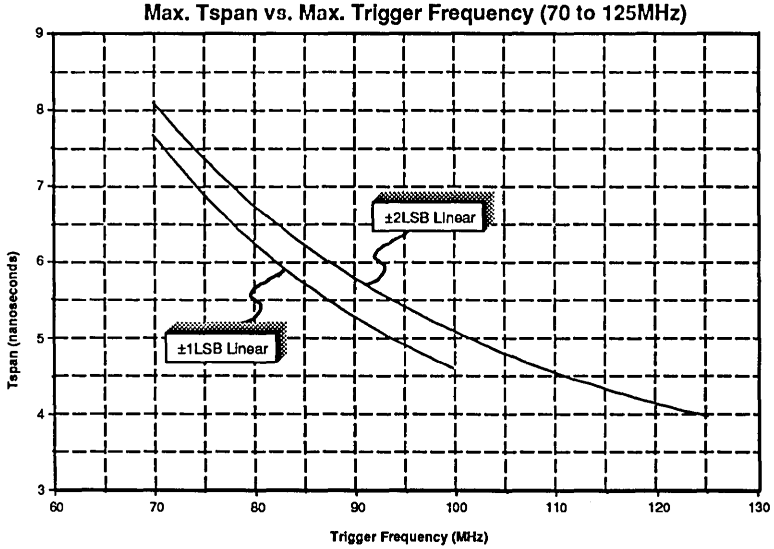
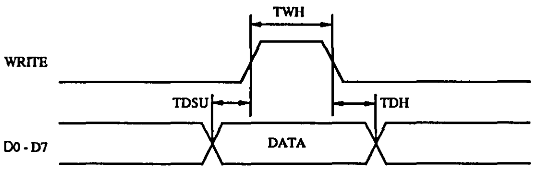
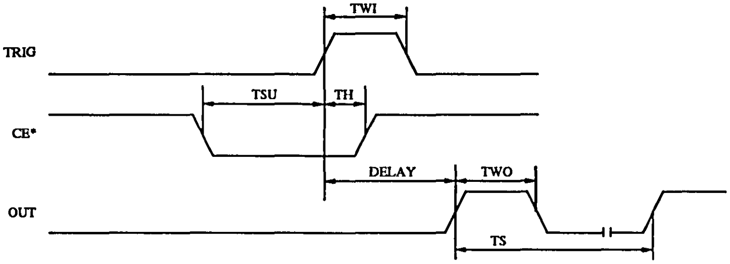


Figure 9. Bt605 Tspan vs. Frequency (70–125 MHz).

Timing Waveforms


TWH
WRITE
TDSU
TDH
D0 - D7
DATA

Parallel Load Timing.


TWI
TRIG
TSU
TH
CE*
DELAY
TWO
OUT
TS

Delay Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt605KPJ	28-pin Plastic J-Lead	0° to +70° C

Bt622

Bt624

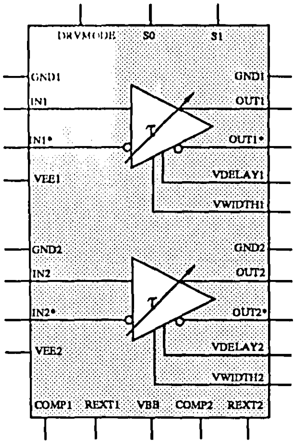
Advance Information

his document contains information on a product under development. The parametric nformation contains target parameters and is subject to change.

Distinguishing Features

- Greater than 200 MHz Bandwidth
- 4 Adjustable Delay Lines in One Package
- Independently Adjusts Positive- and Negative-Going Transition Delays
- Three Selectable Delay Ranges: 10 ns, 20 ns, and 30 ns
- Mode Control for Common Signal Distribution to All Channels
- Delays Adjustable via External Voltages or Currents
- Individual GND/VEE Pins per Delay Section for Superior Crosstalk Performance
- ECL 10KH Compatible
- Cascadable for Greater Delays and/or Multiple Taps

Bt622 Dual Channel

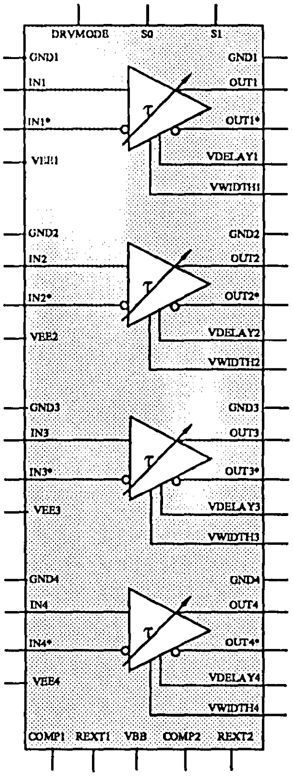

DRVMODE
S0
S1
GND1
IN1
IN1*
VEE1
GND1
OUT1
OUT1*
VDELAY1
VWIDTH1
GND2
IN2
IN2*
VEE2
GND2
OUT2
OUT2*
VDELAY2
VWIDTH2
T
COMP1
REXT1
VBB
COMP2
REXT2

Brooktree Corporation
9950 Barnes Canyon Rd.
San Diego, CA 92121-2790
(619) 452-7580 • (800) VIDEO IC
TLX: 383 596 • FAX: (619) 452-1249
L622001 Rev. F

Applications

- Automatic Test Equipment
- Clocked ECL Circuitry
- CPU System Timing

Bt624 Quad Channel


DRVMODE
S0
S1
GND1
IN1
IN1*
VEE1
GND1
OUT1
OUT1*
VDELAY1
VWIDTH1
GND2
IN2
IN2*
VEE2
GND2
OUT2
OUT2*
VDELAY2
VWIDTH2
GND3
IN3
IN3*
VEE3
GND3
OUT3
OUT3*
VDELAY3
VWIDTH3
GND4
IN4
IN4*
VEE4
GND4
OUT4
OUT4*
VDELAY4
VWIDTH4
T
COMP1
REXT1
VBB
COMP2
REXT2

Very High Speed 10KH ECL-Compatible Dual and Quad Channel Delay Lines

Product Description

The Bt622 and Bt624 Adjustable Delay Lines are designed for high-performance delay adjustments of high-frequency ECL signals. The Bt622 is a dual delay line and the Bt624 is a quad version. Their varied applications include use in ATE as the prime method of de-skewing multiple channels of a shared resource system, and the common need of signal timing adjustments in many clocked ECL circuits.

The Bt622/624 Delay Lines maintain ECL edge quality and clock duty cycles at high frequencies, in contrast to limited-bandwidth passive delay lines.

There are two external delay adjustments available for each channel, VDELAY and VWIDTH. Depending on the selected mode of operation, the adjustment inputs have two different functions. When trailing edge adjustment is not required, VDELAY will simply delay the input waveform over the selected ranges and VWIDTH is not operational. When the trailing edge adjustment is enabled, VDELAY and VWIDTH adjust the delays of the leading (positive-going) and trailing (negative-going) edges respectively.

These devices allow for fine de-skew control of multiple signal paths and permit compensation for differences in positive- versus negative-going signal delays through system paths.

The overlapping delay ranges allow for maximum versatility to optimize for the necessary delays while maintaining the required resolutions of adjustments.

Brooktree®

Pin Descriptions

Pin Name	Description
	The signals that are individually assigned for each channel are suffixed by the channel number: 1 through 2 for the Bt622, 1 through 4 for the Bt624.
IN, IN*	Differential 10KH ECL-compatible inputs. The negative polarity input is indicated by the *. The signal to be delayed is input to the device through this differential pair. Internal pull-ups and pull-downs ensure that, when left floating, IN will be pulled low and IN* will be pulled high to yield a stable differential low at the outputs.
OUT, OUT*	Differential 10KH ECL-compatible outputs. The negative polarity input is indicated by the *. The signal to be delayed is output from the device through this differential pair.
DRVMODE	A single-ended 10KH ECL-compatible input. The input is internally pulled low. If left floating or at ECL logic 0, the device acts as multiple independent delay channels. A logic one on this pin will distribute the signal input to channel 2 of the Bt624 to all other channels. The inputs to the other channels are also ORed into the signal path. The Bt622 channel 1 is driven to channel 2. In this mode the device acts as a skewable signal distribution component and minimizes the number of necessary connections to the package which would degrade the input signal quality. Since the other channels are also ORed into the signal path, the fanned-out input signal may act as a "modulation" to all channels.
VDELAY	Voltage node input used to adjust the delay through the channel. Nominal voltage range for this node is 0 V to –1.0 V, for short and long delays respectively. Positive- and negative-going transitions through the delay channel are both adjusted via this control pin equally. A 0.01 µf ceramic capacitor to GND is recommended on this pin for noise reduction. A constant current is mirrored internally at these pins via the current set by REXT1.
VWIDTH	Voltage node input used to adjust the delay for negative-going transitions through the delay channel. Negative-going transitions only are affected. Nominal voltage range for this pin is 0 V to –1.0 V. The positive-going transition delays are not affected. A 0.01 µf ceramic capacitor to GND is recommended on this pin for noise reduction. The VWIDTH pins are active only if S1 is a logical one or connected to VEE.. A constant current is mirrored internally at these pins via the current set by REXT1.
COMP1	Compensation pin. A 0.1 µf ceramic capacitor must be connected between COMP1 and VEE.
COMP2	Compensation pin. A 0.1 µf ceramic capacitor must be connected between COMP2 and VEE.
S0	A single ended 10KH ECL-compatible input. A logical zero selects the lower range of delay adjustment, 4 ns to 14 ns. A logical one selects the upper range of delay adjustment, 8 ns to 28 ns. The input may be connected to GND or VEE for a hard-wired range selection. Floating this input will select a logical zero. This is a global input which affects all channels. Used in conjunction with the S1 input pin, the S0 input selects the range of group delay for given control voltages at the VDELAY and VWIDTH input pins.
S1	A single-ended triple-state input pin. An ECL logical zero disables the VWIDTH pins. Negative transitions will have the same delays as positive transitions. A logical one (or tied to GND) will allow the VWIDTH pins to adjust the delays of the negative transitions through the delay channels. Exceeding the –3.2 V at this input (tie to VEE, or leave floating) will enable extended delay ranges Modes 4 and 5. In these modes, the VWIDTH input pins do not adjust the delay of the negative transition. The VWIDTH pins act as extensions to the VDELAY control pins. See text for a further explanation of the function of this pin. This is a global input which affects all channels.

Pin Descriptions (Continued)

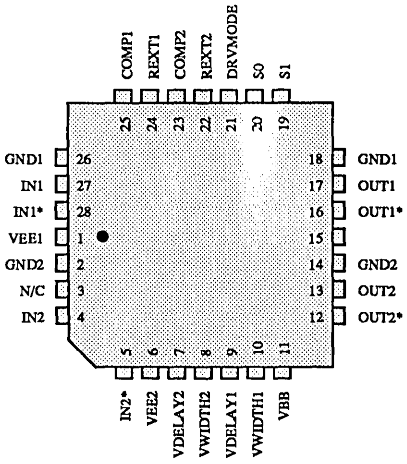
Pin Name	Description
VBB	Nominal–1.3 V output. When driving delay channels single-endedly, the complementary input may be connected to VBB. (Single-ended operation is not recommended for high-frequency or high-accuracy applications). A 0.01 µf ceramic bypass capacitor is recommended for applications using this pin.
GND	Device ground. All GND pins must be connected to ground.
VEE	Negative supply, typically –5.2 V. A 0.1 µf ceramic chip bypass capacitor to ground for all channels is essential for lowest crosstalk performance.
REXT1	This connection sets up internal current sources. A 1.3 kΩ resistor to ground will develop a 1 mA reference current. The nominal voltage at this node is –1.2 V.
REXT2	This connection is used to develop an internal current source. A 2.94 kΩ resistor to ground will develop a 500 µA reference current. The nominal voltage at this pin is –1.47 V.

Pinouts for Bt622 and Bt624

Pinouts Subject to Change

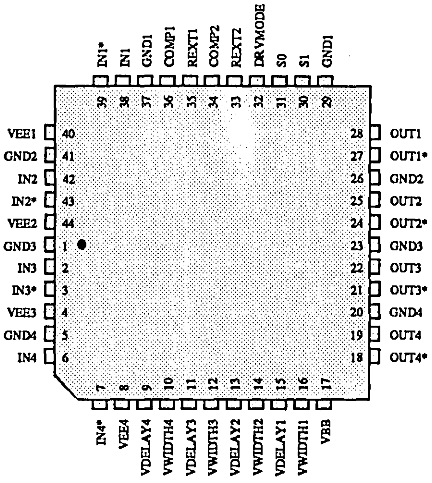
Bt622

28-pin CLCC

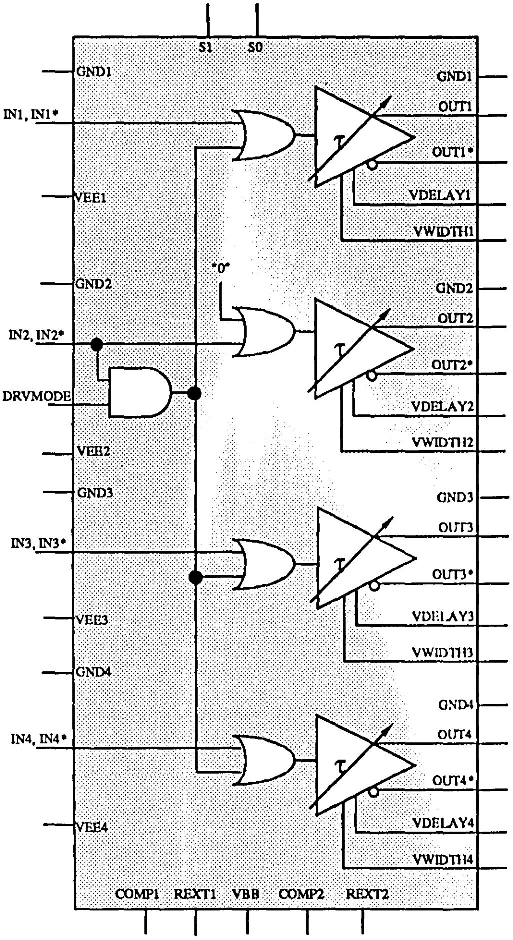

COMP1 25
REXT1 24
COMP2 23
REXT2 22
DRVMODE 21
S0 20
S1 19
GND1 26
IN1 27
IN1* 28
VEE1 1
GND2 2
N/C 3
IN2 4
18 GND1
17 OUT1
16 OUT1*
15
14 GND2
13 OUT2
12 OUT2*
5 IN2*
6 VEE2
7 VDELAY2
8 VWIDTH2
9 VDELAY1
10 VWIDTH1
11 VBB

Bt624

44-pin CLCC


IN1* 39
IN1 38
GND1 37
COMP1 36
REXT1 35
COMP2 34
REXT2 33
DRVMODE 32
S0 31
S1 30
GND1 29
VEE1 40
GND2 41
IN2 42
IN2* 43
VEE2 44
GND3 1
IN3 2
IN3* 3
VEE3 4
GND4 5
IN4 6
28 OUT1
27 OUT1*
26 GND2
25 OUT2
24 OUT2*
23 GND3
22 OUT3
21 OUT3*
20 GND4
19 OUT4
18 OUT4*
7 IN4*
8 VEE4
9 VDELAY4
10 VWIDTH4
11 VDELAY3
12 VWIDTH3
13 VDELAY2
14 VWIDTH2
15 VDELAY1
16 VWIDTH1
17 VBB

Detailed Block Diagram


S1
S0
GND1
IN1, IN1*
VEE1
GND2
IN2, IN2*
DRVMODE
VEE2
GND3
IN3, IN3*
VEE3
GND4
IN4, IN4*
VEE4
"0"
GND1
OUT1
OUT1*
VDELAY1
VWIDTH1
GND2
OUT2
OUT2*
VDELAY2
VWIDTH2
GND3
OUT3
OUT3*
VDELAY3
VWIDTH3
GND4
OUT4
OUT4*
VDELAY4
VWIDTH4
COMP1
REXT1
VBB
COMP2
REXT2

Bt624 Detailed Block Diagram

Application Information

Power Supply Decoupling

ALL VEE supply pins should be separately decoupled to GND with a 0.1 µF ceramic chip capacitor. The bypass capacitors should be as close as possible to the device.

A ground plane is recommended to provide a low-inductance ground return path. The individual channels have separate GND and VEE pins to maintain superior crosstalk performance. The bypass capacitor for each channel should be placed between GND1 and VEE1, GND2 to VEE2, etc.

Internal Fanout

The DRVMODE control input is used to internally distribute the signal present at Channel 2 of the Bt624 (Channel 1 of the Bt622) to Channels 1, 3, and 4 (Channel 2 of the Bt622). This allows the user to terminate a high-quality signal at only one input, avoiding the larger lumped capacitances involved if multiple package inputs were daisy-chained.

Refer to the detailed block diagram for the Bt624. DRVMODE enables the AND gate at Channel 2 to drive the OR gate at the other channels, thereby buffering the signal and maintaining signal integrity. The unused channel inputs are still active. They have internal pull-ups and pull-downs to create a logical 0 at the inputs. This allows the user to float these inputs by leaving them unconnected. They may be driven with signals of their own, however. The application may be for a gated signal, such as a clock. The clock signal applied to Channel 2 and fanned out through Channel 1 may be controlled and gated ON or OFF at Channel 1's output by asserting a logical 0 or 1 respectively at Channel 1's input.

Once the signal is internally buffered and distributed to the other channel inputs, the signal may be delayed independently through each channel according to the mode selected and the signals present at the VDELAY and VWIDTH control inputs.

Ranges of Delay

The S0, S1 control inputs select the range of delay for the signals through the Bt624. There are two types of delay available, one where the input signal is simply delayed and the output signal is identical to the input signal, and the other where independent delay of the leading and trailing edges is available.

Refer to Table 1 for the descriptions of modes versus control inputs. Modes 0, 1, 4, and 5 are delays of type 1—group delays are imposed upon the input signal with NO independent leading and trailing edge adjustment. The criteria dictating which of these modes the application deserves are range of delay needed and the minimum pulse widths expected. Roughly, Mode 0 is a 10-ns delay range, Modes 1 and 4 are 20-ns delay ranges, and Mode 5 is an extended 30-ns delay range. Modes 0 and 1 delays are adjusted via the channel VDELAY inputs only. The VWIDTH control inputs are nonfunctional and unused. Modes 4 and 5 delays utilize both the VDELAY and VWIDTH inputs for control. When implementing Modes 4 or 5, the VDELAY and VWIDTH inputs should be shorted together and a common control voltage applied.

The minimum pulse widths through the channels of delay are related to the chosen range of delay. The longer the range of delay, the longer a very small pulse width may be delayed before incurring inaccurate tracking and subsequent pulse swallowing.

Minimum Pulse Widths

The delay elements have bandwidth constraints for different range configurations and group delay control voltages. These bandwidth differences exhibit themselves as limitations to the acceptable minimum pulse widths (TPW(min)) for a delay channel.

Figure 1 illustrates the minimum pulse widths which may be passed through the delay channels. These are nominal graphs of TPW(min) for the ranges achievable from the S0 and S1 input pins for modes 0 through 5.

The result of violating these minimum curves is a missing output pulse, as the pulse is swallowed.

The mode selection of a particular range of delay and trailing edge adjustment offers the user great flexibility in optimizing the needs of the applications at hand. Different range modes utilize more or less of the Bt622/624 circuitry. Unused on-chip circuitry is powered down to allow cooler operation.

Independent Edge Delays

Modes 2 and 3 offer the capability to adjust the delays of the leading (rising) and trailing (falling) edges. Mode 2 is a 10 ns delay range and Mode 3 is a 20 ns range. The selection of range depends on the desired range of overall delay (group delay) of the signal and how much trailing edge adjustment will be required.

Application Information (continued)

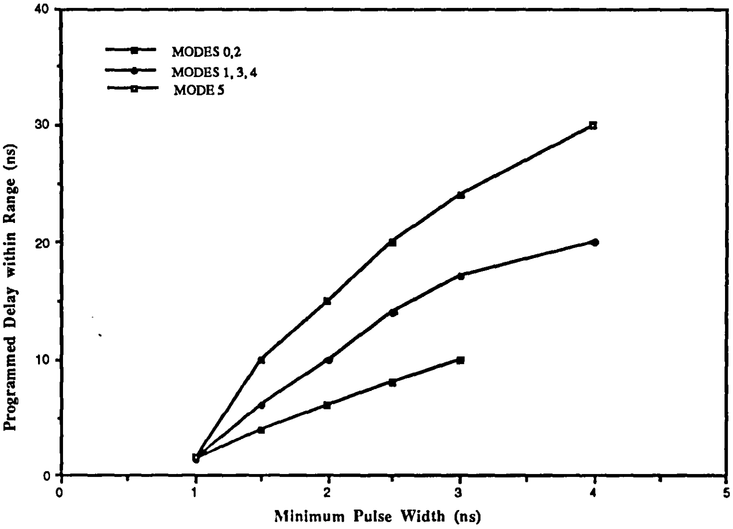


Figure 1. Minimum Pulse Width vs. Group Delay.

Figure 2 is a clear representation of the circuit topology of Modes 2 and 3. Notice that the number of delay cells for the trailing edge adjustment remains constant. The VWIDTH delay range of adjustment is fixed and is the same for both Modes 2 and 3 at 10 delay elements. The number of delay cells for the leading edge adjustments changes from 15 to 25 for Modes 2 and 3 respectively. The positive-going edge triggers the set input to the S-R flip-flop. The signal is inverted after it is delayed for the negative-going edge and triggers the reset input to the flip-flop.

The trailing edge adjustment (via VWIDTH) controls the trailing edge delay only; it has no effect on the leading edge. The VDELAY control has an effect on both the leading and trailing edges. For this reason, delay calibration should be performed first with VDELAY, then with VWIDTH. This will be covered more fully in *Calibrating a System Channel.*

Figure 3 is a useful tool to determine whether Mode 2 or 3 should be implemented in a particular application. When VDELAY is at minimum delay, the range of adjustment of the trailing edge is 0 to +8 ns at the VWIDTH input. When VDELAY is at maximum delay, the trailing edge has –8 to 0 ns of adjustability. These points set the ranges of adjustment that are available at the VWIDTH pin. The shaded area indicates the operating zone. The user should first determine the required range of adjustability of the trailing edge versus the leading edge position. This will dictate what range of overall group delay is available for the particular mode. As an example, if ±2 ns of trailing edge adjustment is required, the intercepts for the operating range are at 25% and 75% of the VDELAY range. This relates to the center 50% range of overall VDELAY. For Mode 2, this would allow 5 ns of "group delay," and for Mode 3 it would be 10 ns, each calculated as 50% of the available range. Similarly, if ±1 ns of trailing edge adjustment is required, 12.5% and 87.5% are the intercepts. These would allow 7.5 ns and 15 ns of adjustment range for Modes 2 and 3 respectively.

(Numbers in blocks are numbers of delay cells.)

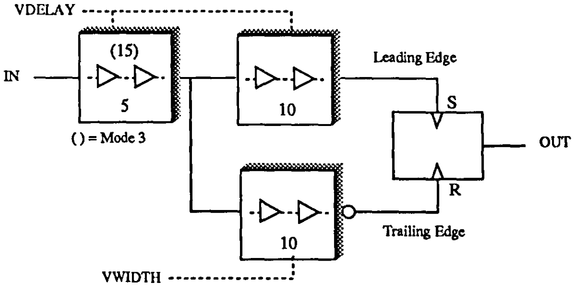


Figure 2. Modes 2, 3 Detailed Channel Block Diagram.

Application Information (continued)

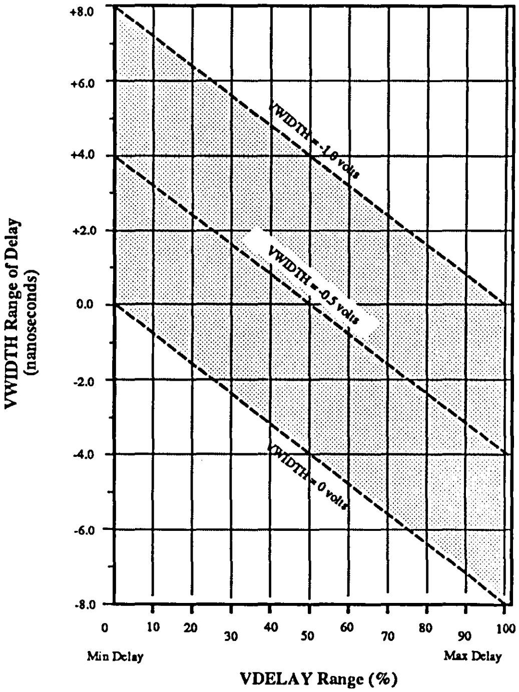


Figure 3. VWIDTH Delay Range vs. VDELAY.

Figure 4 depicts the Bt622 in a variety of applications.

The S1 input pin is connected to GND. This programs a logical one, which enables the VWIDTH pins for adjustment of negative transitions through all channels.

The DRVMODE input is set to a logical low (tied to –5.2 V) which allows Channel 1 and Channel 2 inputs to both be valid. If the pin had been a logical one, the input to Channel 1 would also be ORed into Channel 2.

Channel 1 is being driven with a differential ECL input as a high-performance application. The S0 input is set low (tied to –5.2 V) to enable the lower delay span, 8 to 18 ns, for both channels. The VDELAY and VWIDTH control inputs are being driven from a current output DAC (e.g., a Bt110 Octal DAC) with 1 mA full-scales. This offers complete digital programmability of both the group delay (VDELAY) and the fine adjustment of the negative transitions only (VWIDTH). R1 and R2 are 1 kΩ. The 1 mA current sources at these pins are summed with the DAC output currents to enable voltages from 0 V to –1.0 V, the entire adjustment range.

Channel 2, in contrast, is a lower-performance application. The input is driven single-endedly. The inverting input (IN2*) is connected to the VBB output of the Bt622 to allow proper ECL switching at the –1.3 V point. The delay control inputs are adjusted by the trimming resistor (R4) to ground. The VDELAY and VWIDTH control inputs are shorted together and tied to this same controlling resistor. Since two control inputs are tied together, 2 mA of node current results (1 mA for each input). Therefore, the 500 Ω trimming resistor will allow a range of 0 to –1 V. This type of connection is used for less demanding applications where the relevant timing is only to a single edge and the need for independent adjustment of leading and trailing edges does not exist. With the two inputs commoned to the same voltage node, the delays of the leading and trailing edge will track and be approximately equal.

The Bt622/624 have open-emitter outputs; thus, they must be terminated through 50-Ω resistors to –2 V at the end of the transmission paths or the equivalent. Microstrip layout techniques are recommended. The input signals should also abide by proper high-frequency layout rules. Minimize any possible reflection sources and maintain a constant low-impedance transmission line up to the device.

Application Information (continued)

Figure 4 has both channels' differential outputs terminated. Single-ended terminations of the outputs are not recommended for maximum performance. All differential stages should be equally loaded. Figure 4 also shows each termination resistor having its own bypass capacitor to ground for the -2 V termination voltage. The use or nonuse of individual capacitors for each termination resistor is a function of the actual layout and the resultant ground and -2 V path impedances. Adjacent termination resistors (chip resistors are always recommended for maximum performance) may get by with a single bypass capacitor. Under no conditions are common resistor networks recommended for optimum operation.

Although the Bt622/624 is designed to operate with constant power dissipation, the airflow requirement of 400 LFPM is recommended to minimize any thermal variations which may result in tens of picoseconds of delay variations.

Maximum performance from the Bt622/624 can only be obtained by careful layout and evaluation. Timing measurements in the sub-100 picosecond range are valid only if great care in the total environment of the device is observed. Great care was taken to design and specify these devices for maximum performance and ease of use. It is up to the user to follow these recommendations in the applications and evaluations of the devices.

Delay Channel Linearity

Figure 5 is a graph of the delay versus VDELAY control voltage. The transfer curve is not an ideal straight line—there is a characteristic nonlinearity to the curve. The Bt622/624 was not designed to be ultra-linear. It is guaranteed monotonic: any decrease in control voltage will increase the programmed delay.

A further aid in visualizing the flexibility of ranges available is shown in Table 1. Given the two input pins, S1 and S0, six different range configurations are possible. Since these ranges are all unique in group delay and trailing edge adjustment capability, they are enumerated as mode numbers—Modes 0 through 5.

The AC Characteristics section of this document specifies the sensitivities at the endpoints of the transfer function for given voltages at the VDELAY control inputs. A further aid for determination of the required DAC resolution necessary for adjustment resolution is offered in Figure 6. The figure shows

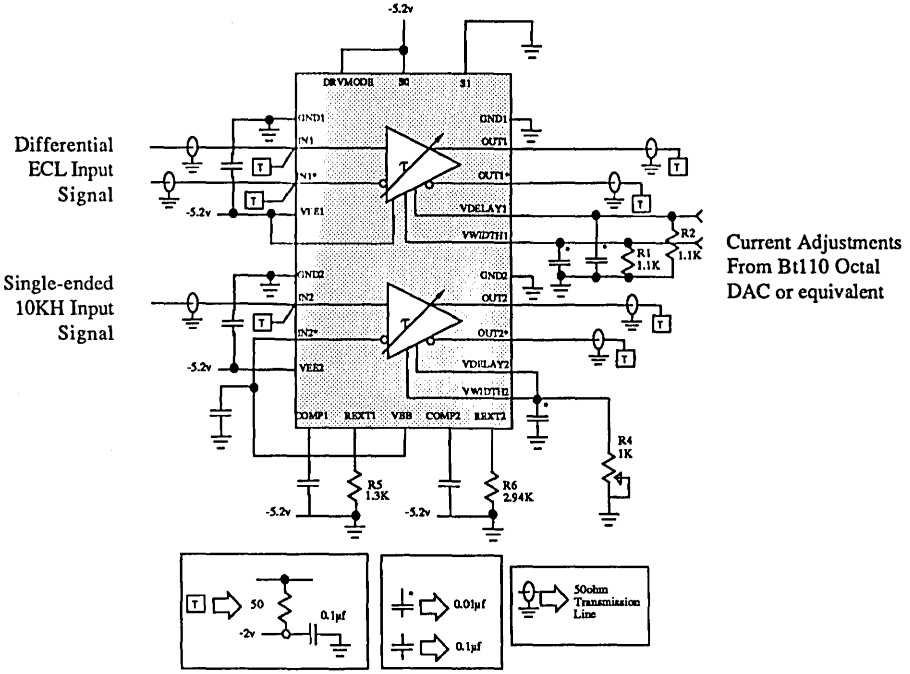

-5.2v
DRVMODE
S0
S1
GND1
IN1
IN1*
VEE1
GND1
OUT1
OUT1*
VDELAY1
VWIDTH1
GND2
IN2
IN2*
VEE2
GND2
OUT2
OUT2*
VDELAY2
VWIDTH2
COMP1
REXT1
VBB
COMP2
REXT2
Differential ECL Input Signal
Single-ended 10KH Input Signal
-5.2v
-5.2v
R2 1.1K
R1 1.1K
Current Adjustments From Bt110 Octal DAC or equivalent
R4 1K
R5 1.3K
R6 2.94K
-5.2v
-5.2v
T
50
-2v
0.1µf
0.01µf
0.1µf
50ohm Transmission Line

Figure 4. Bt622 Typical Applications.

Application Information (continued)

resolutions of time attainable given different resolutions of current output DACs programming the VDELAY input pins. The figure separates the DAC resolutions necessary for both low and high span ranges. The VDELAY control input is a voltage-dependent input. Since the node has an internal 1 mA current source, a controlling current may also be used. A 1 kΩ resistor to ground will generate –1.0 V at the VDELAY or VWIDTH inputs. Variable currents injected into this node will supply currents to the current source and therefore reduce the voltage created at the control inputs. If only 8-bit DACs are available, two current outputs may be summed together, with one output having a 1 mA full-scale and the other DAC having a 125 µA full-scale output. The effective resolution would then be equivalent to a single 11-bit DAC driving the VDELAY pin.

Another method for obtaining greater resolution, this time at the expense of overall range, is to use a fixed resistor to ground as a coarse adjustment to the beginning of the required range. A DAC current output then summed into the node will act as a fine "dither" adjustment.

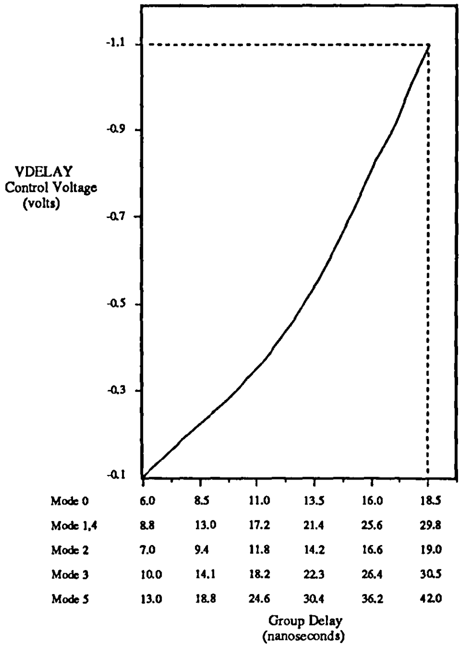


Figure 5. Bt622/624 Delay vs. VDELAY /

Calibrating a System Channel

When using the Bt622/624 delay lines to calibrate positive- and negative-going transitions it is necessary to calibrate the positive-going transitions first. This is the case when implementing Modes 2 or 3.

Figure 7 is a graphic representation of how to calibrate channels using these devices. In 7a, the adjustment is made at the VDELAY pin to move both polarities of transitions from t0 to t1. The trailing edge moves less than the leading edge, but calibration is being accomplished only for the positive-going edges. Both edge polarities are being adjusted, but only the positive-going edge is relevant to the system at this point in the calibration. The VWIDTH adjustment pin is programmed for mid-scale while the positive edge is calibrated.

Once the positive-going edge has been calibrated, the negative-going edges are calibrated via the VWIDTH pin. The VWIDTH pin can now be adjusted to provide more delay or less delay for the negative-going edges. Figure 7b indicates that the edge is being moved more positive by t3 ns. The leading edge delay remains constant when adjusting the VWIDTH pin.

When this calibration is complete, the channel has been de-skewed to other channels and any variation of delay between positive- and negative-going signals from the beginning to the end of the system channel have been accounted for and adjusted out.

MODE #	Input Pins		Group Delay (ns)			WIDTH Adj. Range (ns)
	S1	S0	TMIN	TMAX	TSPAN	
0	0	0	6.0	18.5	10	±0
1	0	1	8.8	29.8	20	±0
2	1	0	7.0	19.0	10	±4
3	1	1	10.0	30.5	20	±4
4	VEE	0	8.8	29.8	20	±0
5	VEE	1	13.0	42.0	28	±0

Table 1. Nominal Delay Ranges vs. Input Configurations (TSPAN = TMAX-TMIN).

Application Information (continued)

Control Voltage Circuits

The user has several options in which to interface to the output delay control pins VDELAY and VWIDTH. The interface options include a current output DAC (as in the Bt110), a voltage output DAC, or simply a resistor connection to ground.

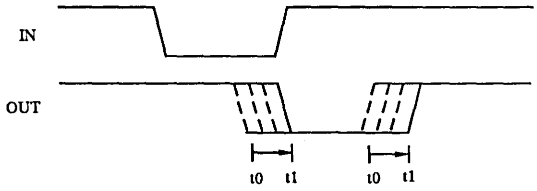
The VDELAY and VWIDTH nodes, as described in the pin description section, are inputs to internal current sinks. This is indicated in Figure 8.

Figure 8a shows the connection to a current output DAC. For the sake of this discussion, let Vcntrl equal VDELAY or VWIDTH. The resistor value for R1 should be chosen so that the required full-scale control voltage, Vcntrl, is generated by the referenced current I. This full-scale voltage will be generated with the DAC outputting zero current. As the DAC sources more current into the node, less current flows through the resistor R1 and therefore the voltage generated across the resistor decreases and generates the minimum control voltage. So, simply put, the equation is:

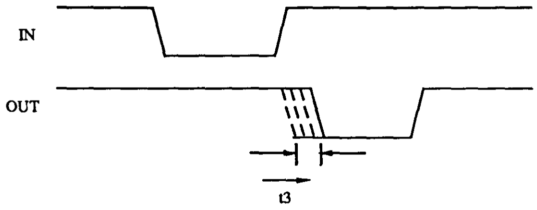
$$\text{Vcntrl} = (\text{Idac} - \text{I}) * \text{R1}.$$

	DAC Resolution (# of bits)	
Picoseconds/ DAC LSB	Modes 0, 2	Modes 1, 3, 4
156.0	6	7
78.0	7	8
39.0	8	9
19.0	9	10
9.7	10	11
4.9	11	12
2.4	12	

Figure 6. Bt622/624 Delay vs. DAC Resolution.



a. Servo the Group Delay via VDELAY Pin.



b. Servo the Negative Transition via VWIDTH Pin.

Figure 7. Bt622/624 Channel Calibration.

Application Information

Figure 8b indicates the connection for a positive voltage output DAC controlling Vcntrl. As shown, the combination of current source I and resistor R1 generates the proper offset voltage, and resistor R2 generates the required attenuation.

The method with which to calculate the resistor values R1 and R2, given the DAC output voltages and Vcntrl endpoints, is as follows:

Vcntrl = Vdac*(R2/(R1 + R2) – *R1*R2/(R1 + R2)
Let
A = R2/(R1 + R2) and B = R1*R2/(R1 + R2)
so
Vcntrl = Vdac*A–I*B
and assume,
0 V ≤ Vdac ≤ Vdac(max) and,
Vcntrl(min) ≤ Vcntrl ≤ Vcntrl(max),

then, isolating A and B and substituting yields,

B = –Vcntrl(min)/I ,
A = [Vcntrl(max) + B*I]/Vdac(max),
and
R2 = B*(1 + 1/(1 – A))
R1 = R2*(1 – A)/A.

Example:

0 V ≤ Vdac ≤ 7 V,
–1.0 V ≤ Vcntrl ≤ –0.1 V, and,
I = 1.0 mA.
Substituting into the above equation
B = 1.0 V/1.0 mA = 1000 Ω,
A = (–0.1 V + 1000 Ω*1.0 mA)/7 V = 0.128 V,
R2 = 1000*[1 + 0.128/(1 – 0.128)] = 1148 Ω
and,
R1 = 1148*(1 – 0.128)/0.128 = 7776 Ω

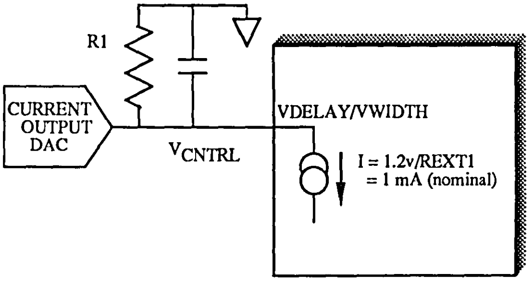

R1
CURRENT OUTPUT DAC
V_{CNTRL}
VDELAY/VWIDTH
I = 1.2v/REXT1
= 1 mA (nominal)

Figure 8a. Control Voltage from IOUT DAC.

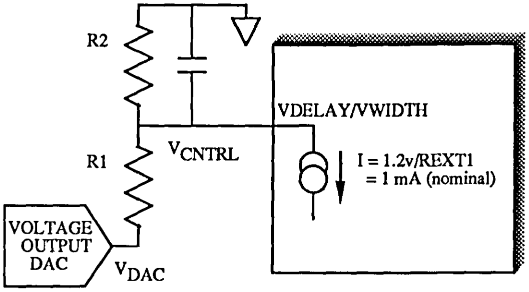

R2
R1
V_{CNTRL}
VOLTAGE OUTPUT DAC
V_{DAC}
VDELAY/VWIDTH
I = 1.2v/REXT1
= 1 mA (nominal)

Figure 8b. Control Voltage from VOUT DAC.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Device Ground	GND	0	0	0	Volts
Negative Power Supply	VEE	-4.9	-5.2	-5.5	Volts
Ambient Operating Temperature	TA	0		+70	°C

Note: Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VEE (relative to GND)		0		-6.0	Volts
Voltage on any Digital Pin				VEE	Volts
Output Current				-50	mA
Ambient Operating Temperature	TA	-55		+70	°C
Storage Temperature	TS	-65		+150	°C
Junction Temperature	TJ			+175	°C
Soldering Temperature (5 seconds, 1/4" from pin)	TSOL			260	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Parameter	Symbol	TA (°C)	Min	Typ	Max	Units
Digital Input High Voltage* IN, IN*	VIH	0 +25 +70	–1170 –1130 –1070		–840 –810 –735	mV mV mV
Digital Input High Voltage* DRVMODE, S0, S1	VIH	0 +25 +70	–1170 –1130 –1070		0 0 0	mV mV mV
Digital Input Low Voltage* IN, IN*	VIL	0 +25 +70	–1950 –1950 –1950		–1480 –1480 –1450	mV mV mV
Digital Input Low Voltage* DRVMODE, S0, S1	VIL	0 +25 +70	VEE VEE VEE		–1480 –1480 –1450	mV mV mV
S1 Third State (Extended Delay)		FULL	VEE		-3.2	V
Digital Output High Voltage*	VOH	0 +25 +70	–1020 –980 –920		–840 –810 –735	mV mV mV
Digital Output Low Voltage*	VOL	0 +25 +70	–1950 –1950 –1950		–1630 –1630 –1600	mV mV mV
Input High Current (Vin =VIHmax) IN, DRVMODE, S0, S1 IN*	 IIH IIH	 FULL FULL		 250 –20		 µA µA
Input Low Current (Vin =VILmin) IN, DRVMODE, S0, S1 IN*	 IIL IIL	 FULL FULL		 100 –40		 µA µA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with all OUT and OUT* outputs terminated through 50 Ω to –2.0 V, REXT1 = 1.21 kΩ, REXT2 = 2.43 kΩ. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

*Relative to GND.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

DC Characteristics (continued)

Parameter	Symbol	TA (°C)	Min	Typ	Max	Units
Power Supply Rejection Ratio	PSRR	FULL		0.5		% Tpd/volt
VEE Supply Current						
Quad Channel (Bt624)						
Mode 0	IEE	FULL		235		mA
Modes 1, 2		FULL		300		mA
Modes 3, 4, 5		FULL		360		mA
Dual Channel (Bt622)						
Mode 0	IEE	FULL		130		mA
Modes 1, 2		FULL		160		mA
Modes 3, 4, 5		FULL		200		mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with all OUT and OUT* outputs terminated through 50 Ω to –2.0 V, REXT1 = 1.3 kΩ, REXT2 = 2.94 kΩ. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delays (note 1) *MODE S1 S0 VDELAY*					
0 0 0 –0.1 V	TPD min	5.5		6.5	ns
0 0 0 –1.1 V	TPDmax	17.8		19.3	ns
1 0 1 –0.1 V	TPDmin	8.3		9.3	ns
1 0 1 –1.1 V	TPDmax	29.0		30.5	ns
2 1 0 –0.1 V	TPDmin	6.5		7.5	ns
2 1 0 –1.1 V	TPDmax	18.3		19.8	ns
3 1 1 –0.1 V	TPDmin	9.5		10.5	ns
3 1 1 –1.1 V	TPDmax	30.0		31.5	ns
4 VEE 0 –0.1 V	TPDmin	8.3		9.3	ns
4 VEE 0 –1.1 V	TPDmax	29.0		30.5	ns
5 VEE 1 –0.1 V	TPDmin	12.5		13.5	ns
5 VEE 1 –1.1 V	TPDmax	41.0		43.0	ns
Rising Edge Delay vs. VWIDTH Delay Change (Modes 2, 3)		–10		+10	ps/3ns
Delay vs. Frequency (note 2)					
S0 = low		–20		+20	ps
S0 = high		–40		+40	ps
VWIDTH Range of Adjustment (VDELAY = –0.5 volts, Mode 2 or 3)					
VWIDTH = 0 volts		–4.3		–3.7	ns
VWIDTH = –1.0 volts		+3.7		+4.3	ns
Rising to Falling Edge Delay Matching Modes 0, 1, 4, 5		–100		+100	ps
Propagation Delay Tempco (note 3)			0.05		% TPD/°C
Output Rise/Fall Times (20% to 80%)	Tr, Tf		850		ps
Delay vs. Input Rise/Fall Time (@ 700 ps TrTf Input)				5	ps/100ps

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with TA = 25 °C and all outputs terminated with 50 Ω to –2.0 V. Timing reference points at the differential crossing points for input and output signals, REXT1 = 1.3 kΩ, REXT2 = 2.94 kΩ. Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

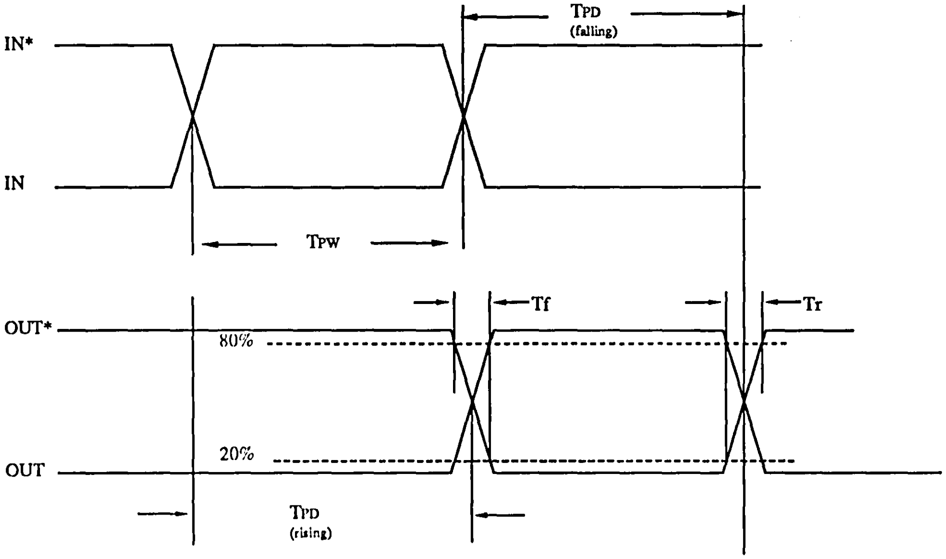
Note 1: Propagation delay minimums and maximums measured with VWIDTH = VDELAY for both leading and trailing edges.

Note 2: Delay versus frequency characteristics are measured by setting VDELAY = VWIDTH = –0.5 V. The delay is measured for both rising and falling edges of a pulse at a 10 MHz repetition rate (100 ns period). The rising and falling edge delays are again measured at a 100 MHz repetition rate (10 ns period). The variation in delays is the delay versus frequency. Measurements are performed using a pulse width of 5 ns.

Note 3: For example, 5 ps/°C when programmed for a 10 ns delay.

The specified limits shown can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes while maintaining a transverse air flow of 400 linear feet per minute over the device either mounted in the test socket or on the printed circuit board.

Timing Waveforms


TPD
(falling)
IN*
IN
TPW
OUT*
OUT
80%
20%
Tf
Tr
TPD
(rising)

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt622KCJ	28-pin Ceramic Leaded Chip Carrier	0° to +70° C
Bt624KCJ	44-pin Ceramic Leaded Chip Carrier	0° to +70° C

SECTION 7

PACKAGING INFORMATION

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Ceramic Cavity Down DIP 7 - 14

Plastic J-Lead (PLCC) 7 - 15

Ceramic J-Lead (CERQUAD) 7 - 19

Ceramic Pin Grid Array (PGA) 7 - 20

Plastic Quad Flatpack (PQFP) 7 - 23

Ceramic Flatpack with Heatsink 7 - 24

Part Numbering System

Bt458 K G 125 883

optional MIL-STD 883C, Class B processing for the S temperature range.

optional speed gradeout information. For VIDEODACs and RAMDACs, specifies MHz.

package type:

C	CERDIP
CJ	ceramic J-lead (CERQUAD)
D	ceramic sidebraze DIP
F	ceramic flatpack (with heatsink)
FN	ceramic flatpack (no heatsink)
G	ceramic PGA
L	ceramic leadless chip carrier
P	plastic DIP
PJ	plastic J-lead (PLCC)
PF	plastic Quad flatpack
S	150 mil SOIC
SW	300 mil SOIC
HJ	plastic J-lead (PLCC with heatsink)

performance gradeout:

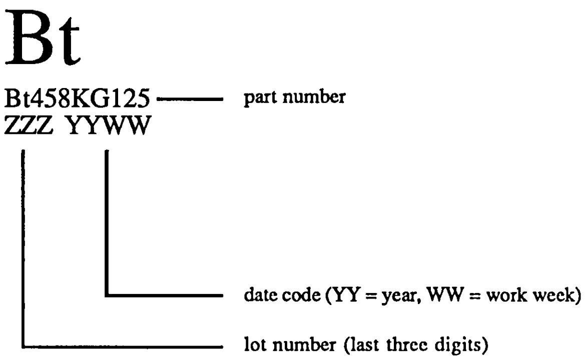
B	–25 to +85 °C
K	0 to +70 °C (0 to +85 °C for 100K ECL)
L	0 to +70 °C, Low power
S	–55 to +125 °C

For other than standard grades, refer to the individual datasheet for letter designation.

basic model number

100–149	D/A converters
200–249	A/D converters
250–299	imaging components
300–399	reserved
400–449	graphics peripherals
450–499	RAMDACs
500–599	general components
600–699	ATE components
700–799	reserved
800–899	reserved
900–999	reserved

Device Marking (Top)


Bt
Bt458KG125
ZZZ YYWW
part number
date code (YY = year, WW = work week)
lot number (last three digits)

Thermal Resistance Information

Power Dissipation Calculations

The maximum power dissipation that an IC can tolerate is determined by the thermal impedance characteristics of the package. The equation to find the allowable power dissipation at a given ambient operating temperature is:

$$PD = (TJ{-}TA) / \theta JA$$

where:
PD = power dissipation at ambient operating temperature
TJ = maximum junction operating temperature (typically 150 °C is used)
TA = maximum ambient operating temperature (free air)
θ JA = typical thermal resistance of junction to ambient (°C / W)

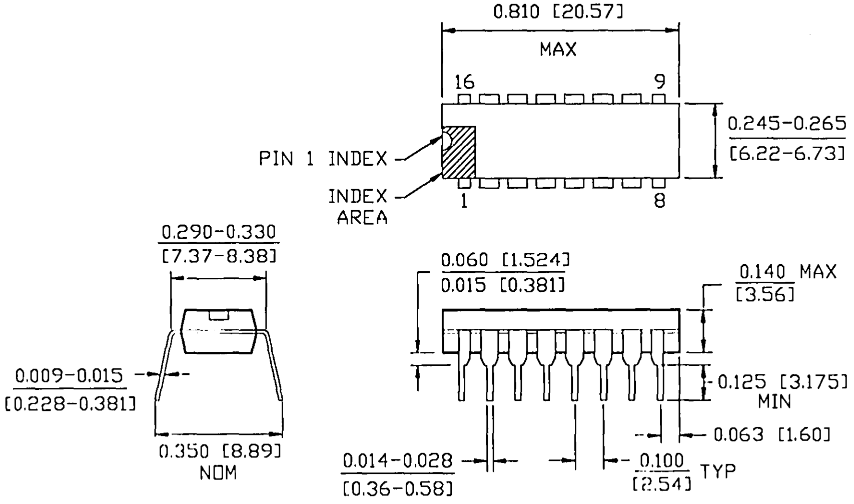
Packaging Notes

1. Unless otherwise indicated, all thermal impedances listed are typical range values or values in static free air for the package only. These impedances will vary when additional heat-sinking capability is provided through PCB solder attachment or air flow.

Plastic DIP Packages

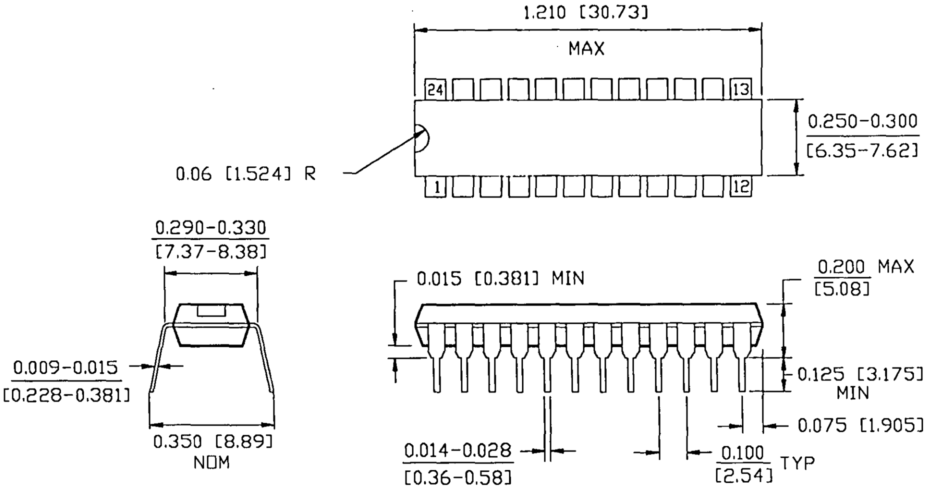
16-Pin 0.3" Plastic DIP

θ JA = 75 °C / W


0.810 [20.57]
MAX
16
9
1
8
PIN 1 INDEX
INDEX AREA
0.245-0.265
[6.22-6.73]
0.290-0.330
[7.37-8.38]
0.009-0.015
[0.228-0.381]
0.350 [8.89]
NOM
0.060 [1.524]
0.015 [0.381]
0.140 MAX
[3.56]
0.125 [3.175]
MIN
0.063 [1.60]
0.014-0.028
[0.36-0.58]
0.100
[2.54]
TYP

24-Pin 0.3" Plastic DIP

θ JA = 60 °C / W


1.210 [30.73]
MAX
24
13
1
12
0.06 [1.524] R
0.250-0.300
[6.35-7.62]
0.290-0.330
[7.37-8.38]
0.009-0.015
[0.228-0.381]
0.350 [8.89]
NOM
0.015 [0.381] MIN
0.200 MAX
[5.08]
0.125 [3.175]
MIN
0.075 [1.905]
0.014-0.028
[0.36-0.58]
0.100
[2.54]
TYP

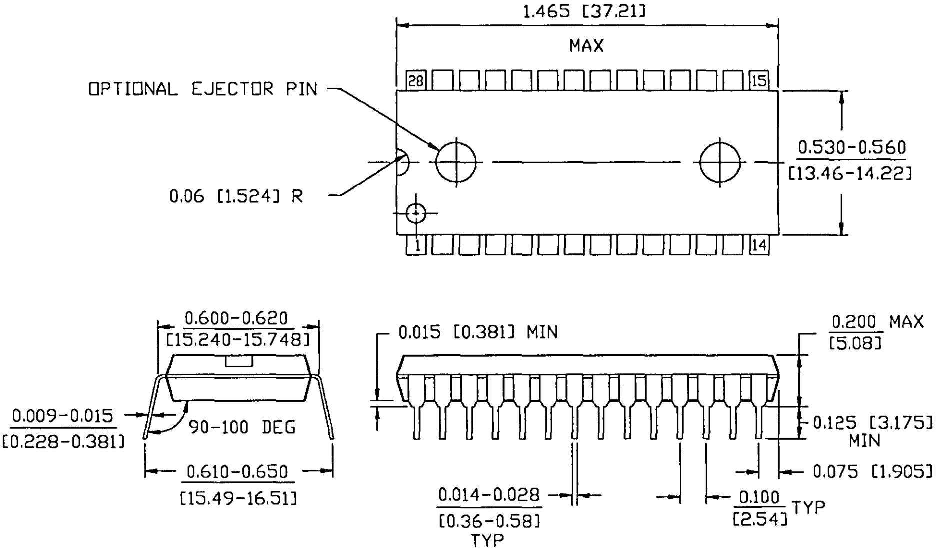
NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.300 [7.62] centers.

Plastic DIP Packages (continued)

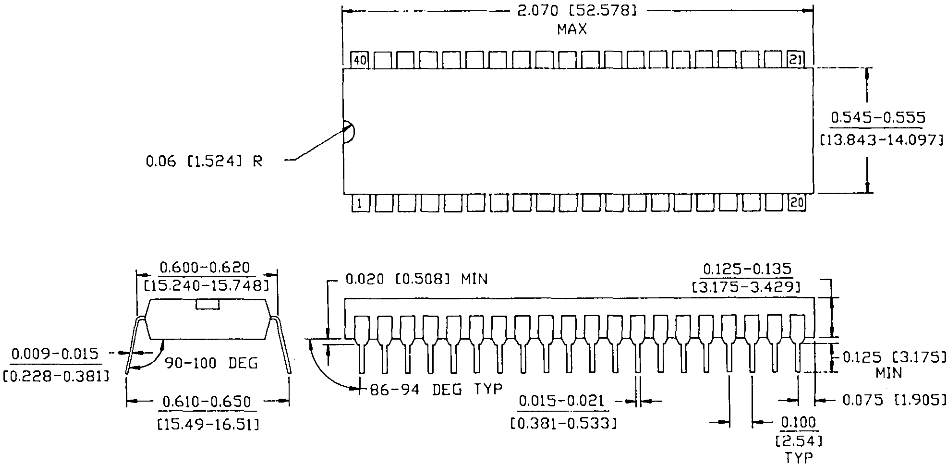
28-Pin 0.6" Plastic DIP

θ JA = 50 °C / W


1.465 [37.21]
MAX
28
15
OPTIONAL EJECTOR PIN
0.530-0.560
[13.46-14.22]
0.06 [1.524] R
1
14
0.600-0.620
[15.240-15.748]
0.015 [0.381] MIN
0.200 MAX
[5.08]
0.009-0.015
[0.228-0.381]
90-100 DEG
0.125 [3.175]
MIN
0.610-0.650
[15.49-16.51]
0.075 [1.905]
0.014-0.028
[0.36-0.58]
TYP
0.100
[2.54]
TYP

40-Pin 0.6" Plastic DIP

θ JA = 45 °C / W


2.070 [52.578]
MAX
40
21
0.545-0.555
[13.843-14.097]
0.06 [1.524] R
1
20
0.600-0.620
[15.240-15.748]
0.020 [0.508] MIN
0.125-0.135
[3.175-3.429]
0.009-0.015
[0.228-0.381]
90-100 DEG
0.125 [3.175]
MIN
86-94 DEG TYP
0.015-0.021
[0.381-0.533]
0.075 [1.905]
0.610-0.650
[15.49-16.51]
0.100
[2.54]
TYP

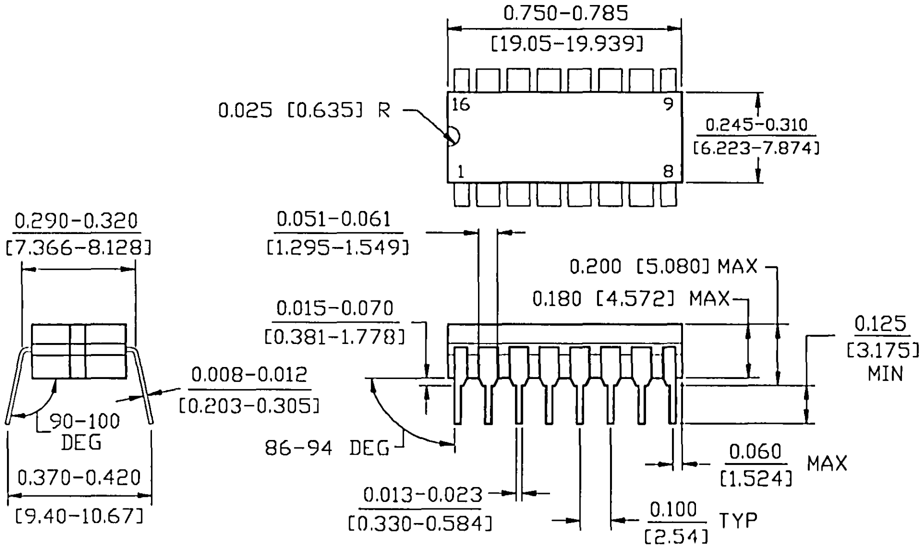
NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

CERDIP Packages

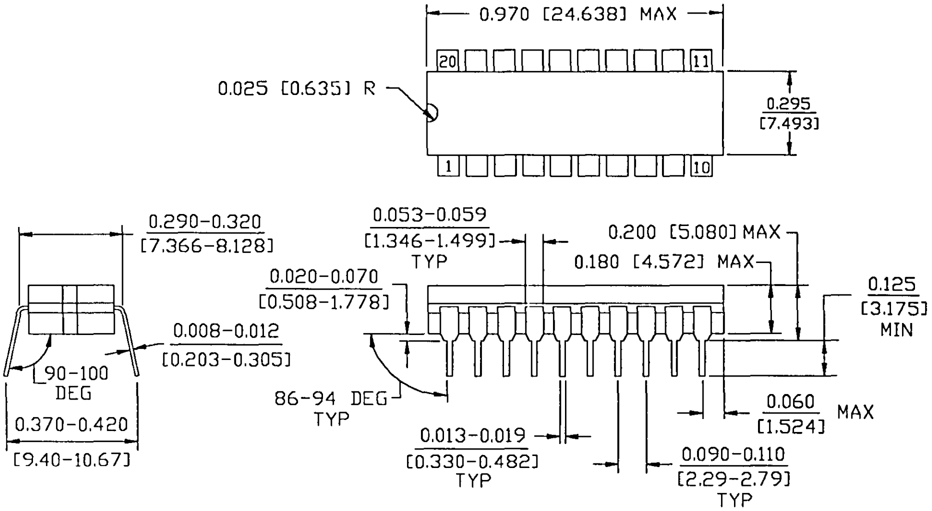
16-Pin 0.3" CERDIP

θ JA = 90–95 °C/W


0.750–0.785
[19.05–19.939]
0.025 [0.635] R
16
9
1
8
0.245–0.310
[6.223–7.874]
0.290–0.320
[7.366–8.128]
0.051–0.061
[1.295–1.549]
0.200 [5.080] MAX
0.180 [4.572] MAX
0.015–0.070
[0.381–1.778]
0.125
[3.175]
MIN
0.008–0.012
[0.203–0.305]
90–100
DEG
86–94 DEG
0.370–0.420
[9.40–10.67]
0.060
[1.524]
MAX
0.013–0.023
[0.330–0.584]
0.100
[2.54]
TYP

20-Pin 0.3" CERDIP

θ JA = 85–90 °C/W


0.970 [24.638] MAX
20
11
0.025 [0.635] R
0.295
[7.493]
1
10
0.290–0.320
[7.366–8.128]
0.053–0.059
[1.346–1.499]
TYP
0.200 [5.080] MAX
0.180 [4.572] MAX
0.020–0.070
[0.508–1.778]
0.125
[3.175]
MIN
0.008–0.012
[0.203–0.305]
90–100
DEG
86–94 DEG
TYP
0.370–0.420
[9.40–10.67]
0.060
[1.524]
MAX
0.013–0.019
[0.330–0.482]
TYP
0.090–0.110
[2.29–2.79]
TYP

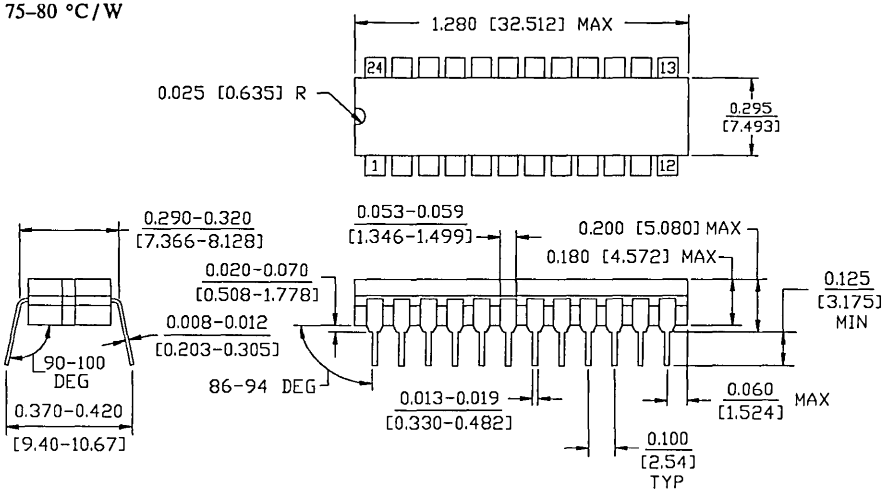
NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.300 [7.62] centers.

CERDIP Packages (continued)

24-Pin 0.3" CERDIP

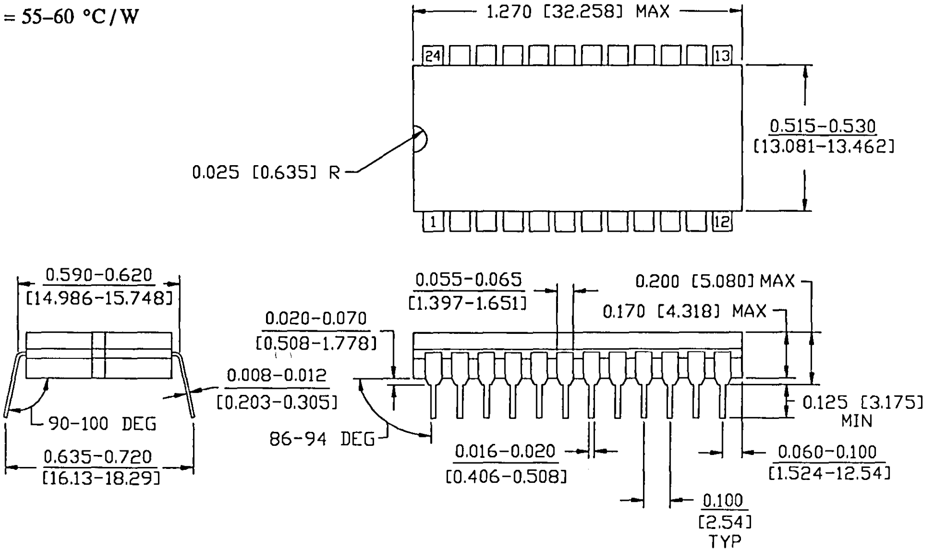
θ JA = 75–80 °C/W


1.280 [32.512] MAX
24
13
1
12
0.025 [0.635] R
0.295
[7.493]
0.290-0.320
[7.366-8.128]
0.020-0.070
[0.508-1.778]
0.008-0.012
[0.203-0.305]
90-100
DEG
0.370-0.420
[9.40-10.67]
0.053-0.059
[1.346-1.499]
0.200 [5.080] MAX
0.180 [4.572] MAX
0.125
[3.175]
MIN
86-94 DEG
0.013-0.019
[0.330-0.482]
0.060
[1.524]
MAX
0.100
[2.54]
TYP

NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.300 [7.62] centers.

24-Pin 0.6" CERDIP

θ JA = 55–60 °C/W

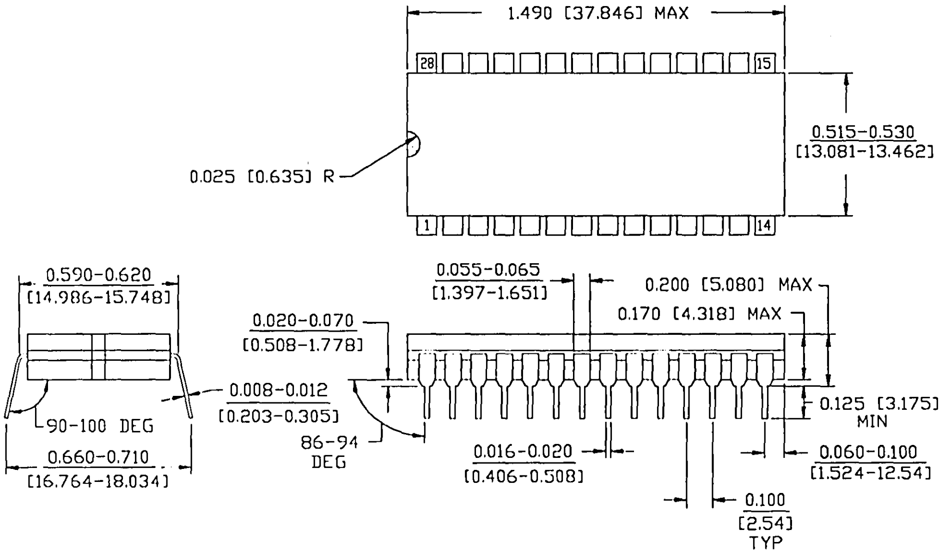

1.270 [32.258] MAX
24
13
1
12
0.515-0.530
[13.081-13.462]
0.025 [0.635] R
0.590-0.620
[14.986-15.748]
0.020-0.070
[0.508-1.778]
0.008-0.012
[0.203-0.305]
90-100 DEG
0.635-0.720
[16.13-18.29]
0.055-0.065
[1.397-1.651]
0.200 [5.080] MAX
0.170 [4.318] MAX
0.125 [3.175]
MIN
86-94 DEG
0.016-0.020
[0.406-0.508]
0.060-0.100
[1.524-12.54]
0.100
[2.54]
TYP

NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

CERDIP Packages (continued)

28-Pin 0.6" CERDIP

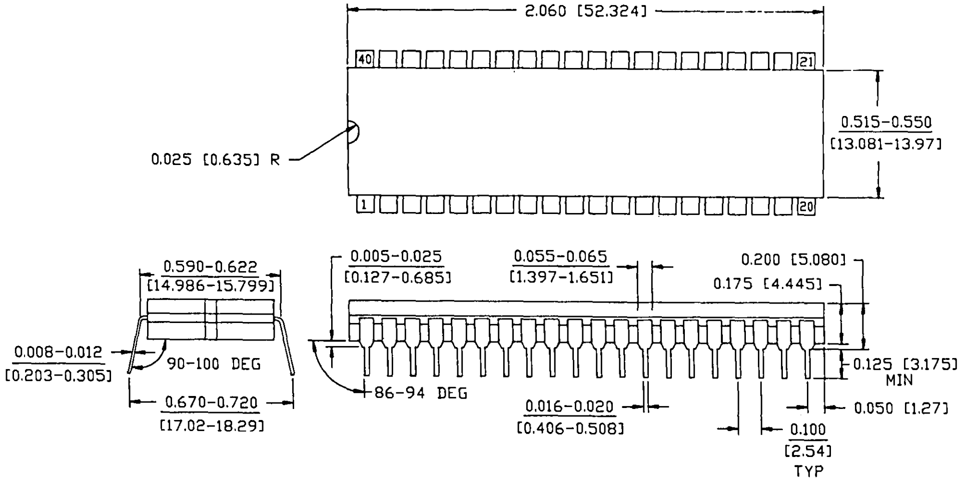
θ JA = 55–60 °C / W



1.490 [37.846] MAX
28
15
1
14
0.515–0.530
[13.081–13.462]
0.025 [0.635] R
0.590–0.620
[14.986–15.748]
90–100 DEG
0.660–0.710
[16.764–18.034]
0.008–0.012
[0.203–0.305]
0.020–0.070
[0.508–1.778]
86–94
DEG
0.055–0.065
[1.397–1.651]
0.200 [5.080] MAX
0.170 [4.318] MAX
0.125 [3.175]
MIN
0.016–0.020
[0.406–0.508]
0.060–0.100
[1.524–12.54]
0.100
[2.54]
TYP

40-Pin 0.6" CERDIP

θ JA = 50–55 °C / W



2.060 [52.324]
40
21
1
20
0.515–0.550
[13.081–13.97]
0.025 [0.635] R
0.590–0.622
[14.986–15.799]
0.008–0.012
[0.203–0.305]
90–100 DEG
0.670–0.720
[17.02–18.29]
0.005–0.025
[0.127–0.685]
86–94 DEG
0.055–0.065
[1.397–1.651]
0.200 [5.080]
0.175 [4.445]
0.125 [3.175]
MIN
0.016–0.020
[0.406–0.508]
0.050 [1.27]
0.100
[2.54]
TYP

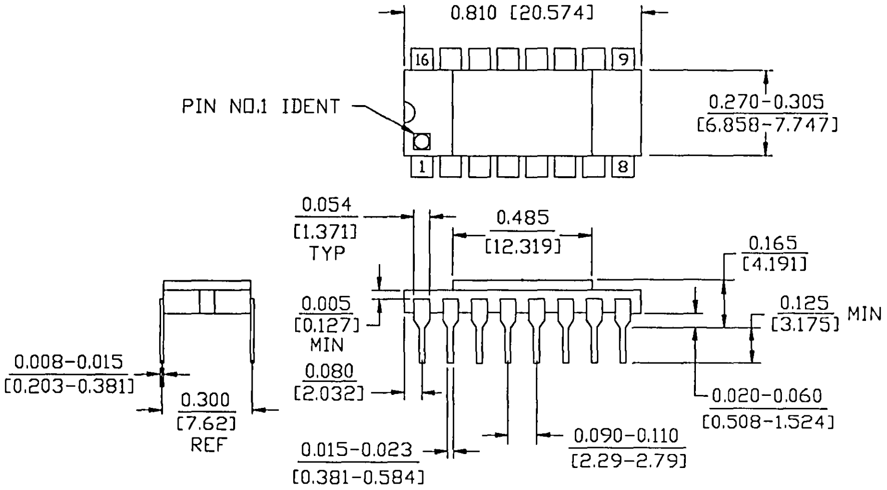
NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

Ceramic Sidebraze DIP Packages

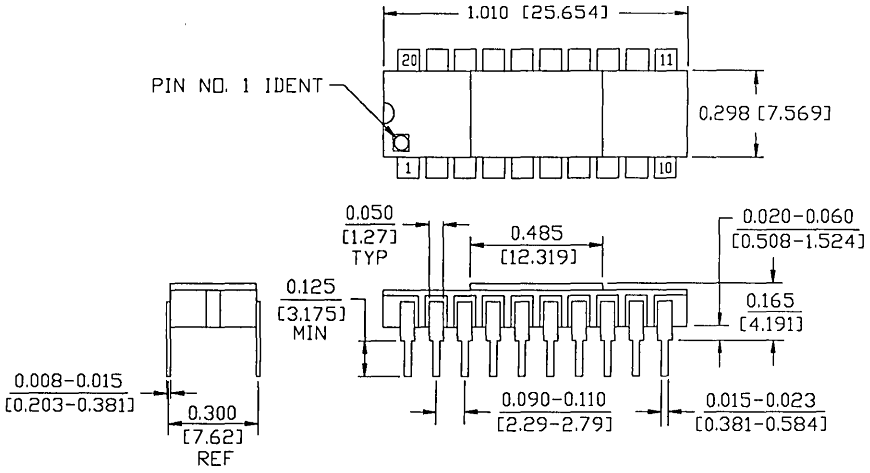
16-Pin 0.3" Ceramic Sidebraze DIP

θ JA = 95 °C/W


0.810 [20.574]
16
9
PIN NO.1 IDENT
1
8
0.270-0.305
[6.858-7.747]
0.054
[1.371]
TYP
0.485
[12.319]
0.165
[4.191]
0.005
[0.127]
MIN
0.125
[3.175]
MIN
0.008-0.015
[0.203-0.381]
0.300
[7.62]
REF
0.080
[2.032]
0.020-0.060
[0.508-1.524]
0.090-0.110
[2.29-2.79]
0.015-0.023
[0.381-0.584]

20-Pin 0.3" Ceramic Sidebraze DIP

θ JA = 85–90 °C/W


1.010 [25.654]
20
11
PIN NO. 1 IDENT
1
10
0.298 [7.569]
0.050
[1.27]
TYP
0.485
[12.319]
0.020-0.060
[0.508-1.524]
0.125
[3.175]
MIN
0.165
[4.191]
0.008-0.015
[0.203-0.381]
0.300
[7.62]
REF
0.090-0.110
[2.29-2.79]
0.015-0.023
[0.381-0.584]

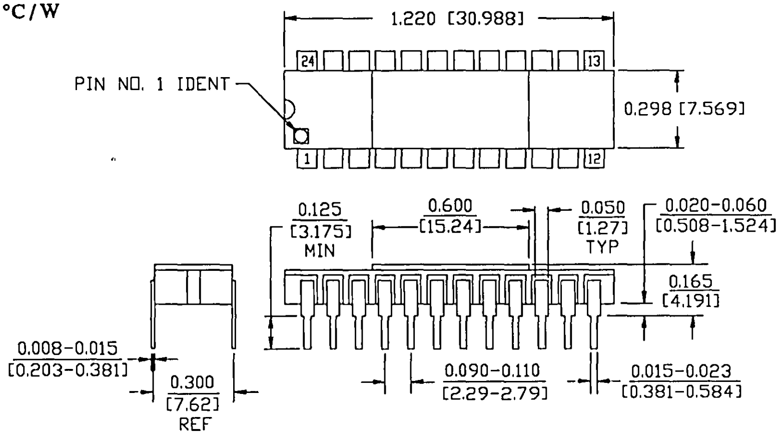
NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.300 [7.62] centers.

Ceramic Sidebraze DIP Packages (continued)

24-Pin 0.3" Ceramic Sidebraze DIP

θ JA = 60–65 °C/W

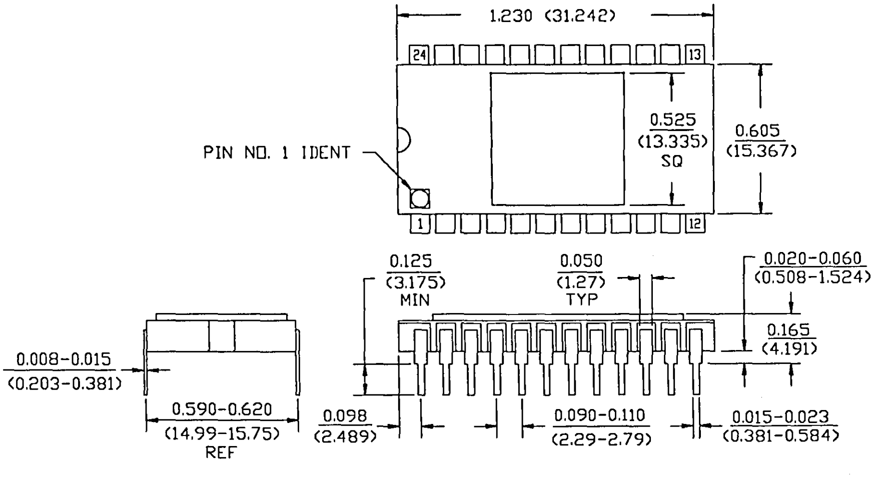

1.220 [30.988]
24
13
PIN NO. 1 IDENT
0.298 [7.569]
1
12
0.125 [3.175] MIN
0.600 [15.24]
0.050 [1.27] TYP
0.020-0.060 [0.508-1.524]
0.165 [4.191]
0.008-0.015 [0.203-0.381]
0.300 [7.62] REF
0.090-0.110 [2.29-2.79]
0.015-0.023 [0.381-0.584]

24 PIN 0.3' CERAMIC SIDEBRAZE DIP

NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.300 [7.62] centers.

24-Pin 0.6" Ceramic Sidebraze DIP

θ JA = 55–60 °C/W

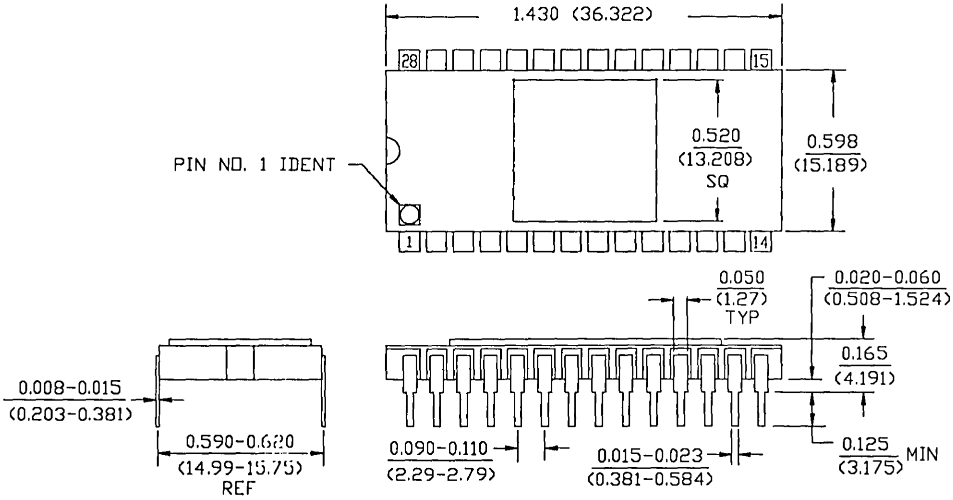

1.230 (31.242)
24
13
0.525 (13.335) SQ
0.605 (15.367)
PIN NO. 1 IDENT
1
12
0.125 (3.175) MIN
0.050 (1.27) TYP
0.020-0.060 (0.508-1.524)
0.165 (4.191)
0.008-0.015 (0.203-0.381)
0.590-0.620 (14.99-15.75) REF
0.098 (2.489)
0.090-0.110 (2.29-2.79)
0.015-0.023 (0.381-0.584)

NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

Ceramic Sidebraze DIP Packages (continued)

28-Pin 0.6" Ceramic Sidebraze DIP

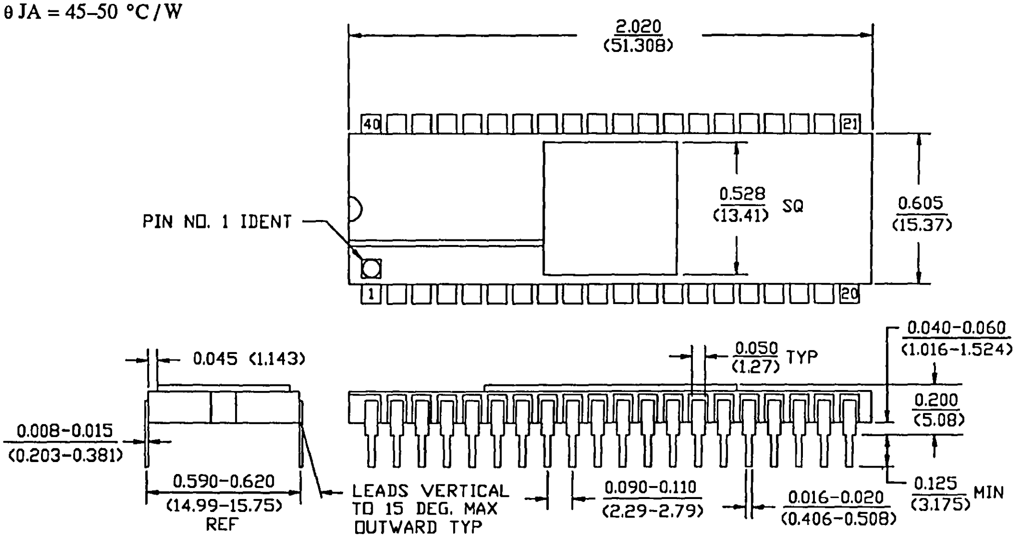
θ JA = 50–55 °C / W



1.430 (36.322)
28
15
1
14
PIN NO. 1 IDENT
0.520
(13.208)
SQ
0.598
(15.189)
0.050
(1.27)
TYP
0.020-0.060
(0.508-1.524)
0.165
(4.191)
0.008-0.015
(0.203-0.381)
0.590-0.620
(14.99-15.75)
REF
0.090-0.110
(2.29-2.79)
0.015-0.023
(0.381-0.584)
0.125
(3.175)
MIN

40-Pin 0.6" Ceramic Sidebraze DIP

θ JA = 45–50 °C / W



2.020
(51.308)
40
21
1
20
PIN NO. 1 IDENT
0.528
(13.41)
SQ
0.605
(15.37)
0.045 (1.143)
0.050
(1.27)
TYP
0.040-0.060
(1.016-1.524)
0.200
(5.08)
0.008-0.015
(0.203-0.381)
0.590-0.620
(14.99-15.75)
REF
LEADS VERTICAL
TO 15 DEG. MAX
OUTWARD TYP
0.090-0.110
(2.29-2.79)
0.016-0.020
(0.406-0.508)
0.125
(3.175)
MIN

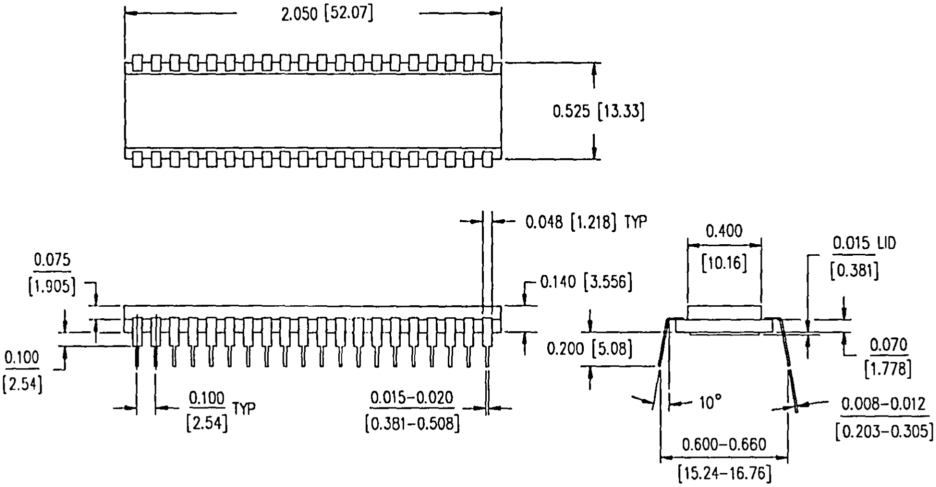
NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

Ceramic Cavity Down DIP Packages

40-Pin 0.6" Ceramic Cavity Down DIP

θ JA = 30–40 °C/W


2.050 [52.07]
0.525 [13.33]
0.048 [1.218] TYP
0.075 [1.905]
0.140 [3.556]
0.100 [2.54]
0.100 [2.54] TYP
0.015-0.020 [0.381-0.508]
0.400 [10.16]
0.015 LID [0.381]
0.200 [5.08]
0.070 [1.778]
10°
0.008-0.012 [0.203-0.305]
0.600-0.660 [15.24-16.76]

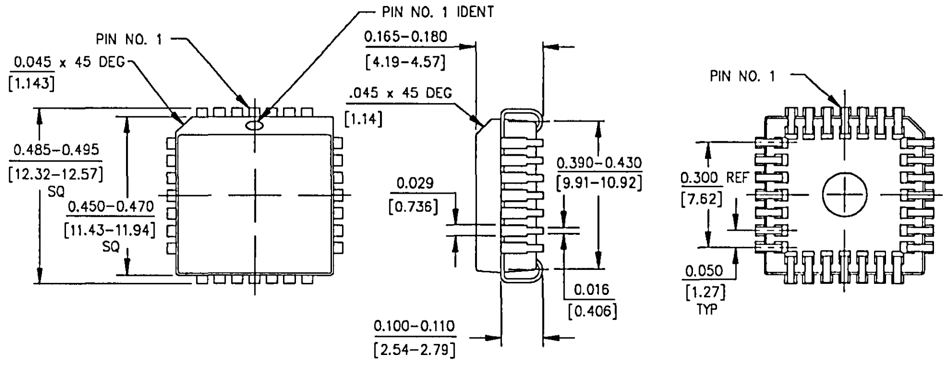
NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. Pins are intended for insertion in hole rows on 0.600 [15.24] centers.

Plastic J-Lead (PLCC) Packages

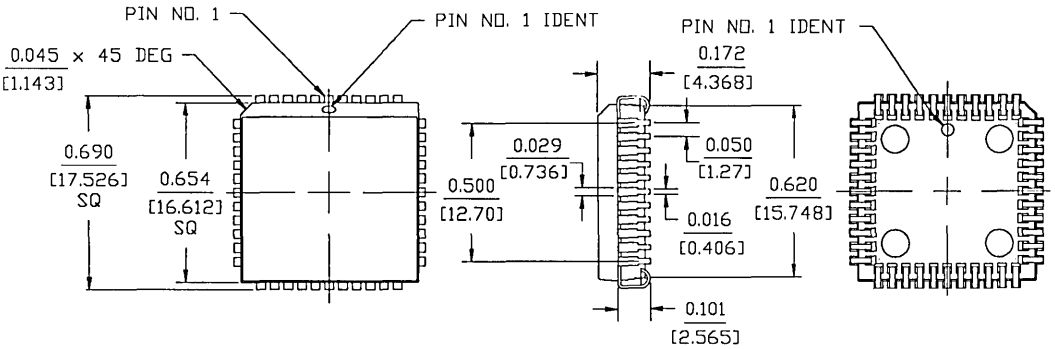
28-Pin Plastic J-Lead

θ JA = 65–70 °C/W


PIN NO. 1
0.045 x 45 DEG
[1.143]
PIN NO. 1 IDENT
0.165–0.180
[4.19–4.57]
.045 x 45 DEG
[1.14]
0.485–0.495
[12.32–12.57]
SQ
0.450–0.470
[11.43–11.94]
SQ
0.029
[0.736]
0.390–0.430
[9.91–10.92]
0.016
[0.406]
0.100–0.110
[2.54–2.79]
PIN NO. 1
0.300 REF
[7.62]
0.050
[1.27]
TYP

44-Pin Plastic J-Lead

θ JA = 50–55 °C/W


PIN NO. 1
0.045 x 45 DEG
[1.143]
PIN NO. 1 IDENT
0.690
[17.526]
SQ
0.654
[16.612]
SQ
0.500
[12.70]
0.029
[0.736]
PIN NO. 1 IDENT
0.172
[4.368]
0.050
[1.27]
0.016
[0.406]
0.620
[15.748]
0.101
[2.565]

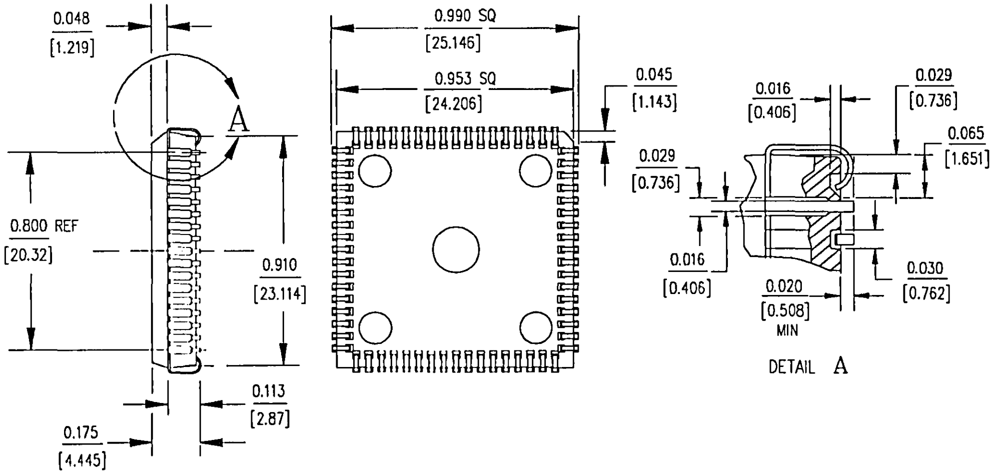
NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Plastic J-Lead (PLCC) Packages (continued)

68-Pin Plastic J-Lead

θ JA = 45–50 °C/W


0.048
[1.219]
A
0.800 REF
[20.32]
0.910
[23.114]
0.175
[4.445]
0.113
[2.87]
0.990 SQ
[25.146]
0.953 SQ
[24.206]
0.045
[1.143]
0.029
[0.736]
0.016
[0.406]
0.016
[0.406]
0.029
[0.736]
0.065
[1.651]
0.030
[0.762]
0.020
[0.508]
MIN
DETAIL A

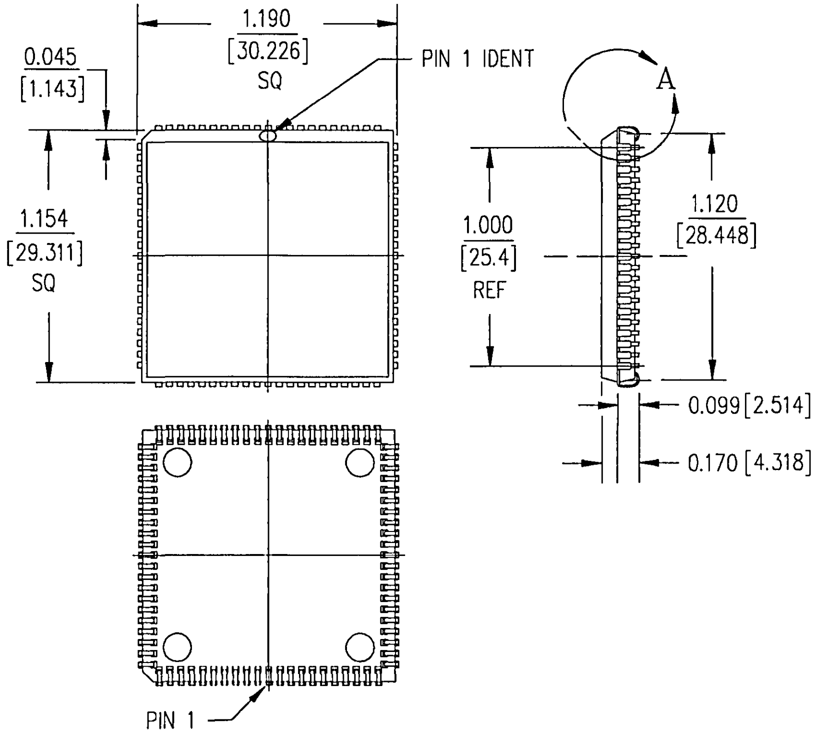
NOTES - Unless otherwise specified:

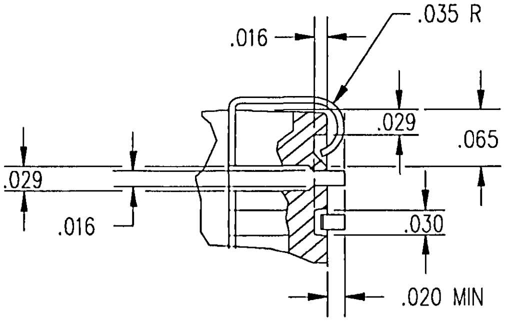
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Plastic J-Lead (PLCC) Packages (continued)

84-Pin Plastic J-Lead

θ JA = 35–40 °C / W


1.190
[30.226]
SQ
0.045
[1.143]
PIN 1 IDENT
A
1.154
[29.311]
SQ
1.000
[25.4]
REF
1.120
[28.448]
0.099 [2.514]
0.170 [4.318]
PIN 1


.016
.035 R
.029
.065
.029
.016
.030
.020 MIN

DETAIL A

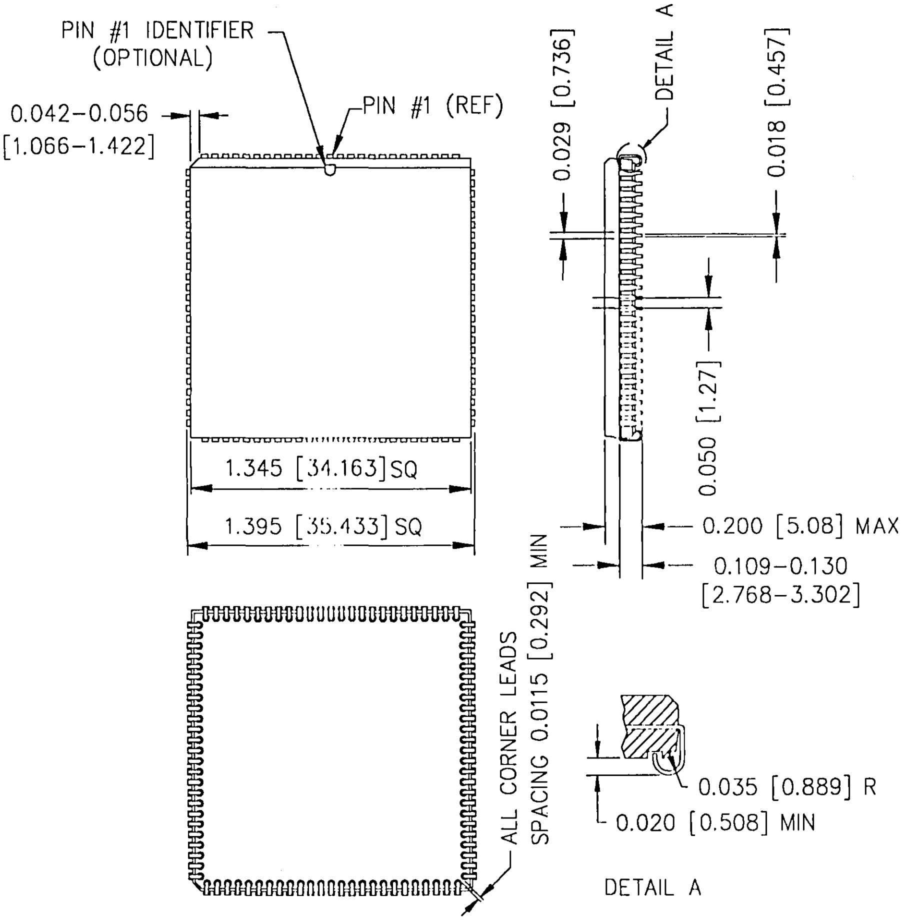
NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Plastic J-Lead (PLCC) Packages (continued)

100-Pin Plastic J-Lead

0 JA = To be determined.


PIN #1 IDENTIFIER (OPTIONAL)
0.042–0.056 [1.066–1.422]
PIN #1 (REF)
1.345 [34.163] SQ
1.395 [35.433] SQ
ALL CORNER LEADS SPACING 0.0115 [0.292] MIN
0.029 [0.736]
DETAIL A
0.018 [0.457]
0.050 [1.27]
0.200 [5.08] MAX
0.109–0.130 [2.768–3.302]
0.035 [0.889] R
0.020 [0.508] MIN
DETAIL A

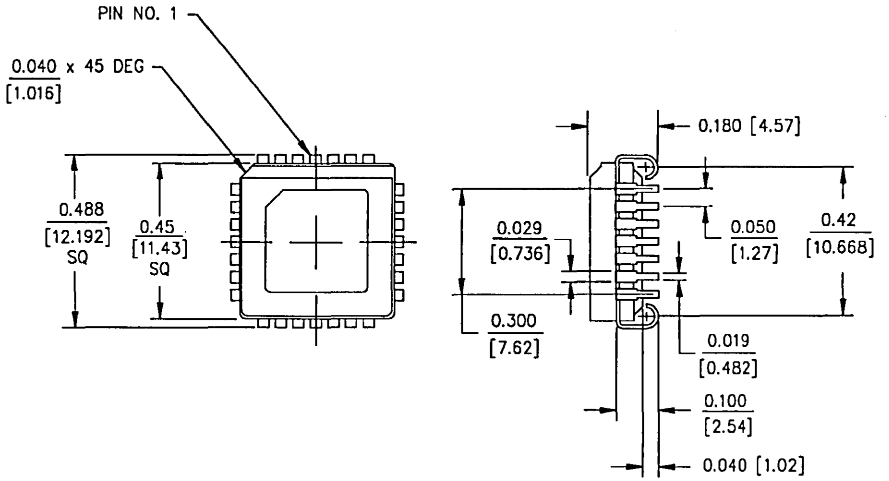
NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Ceramic J-Lead (CERQUAD) Packages

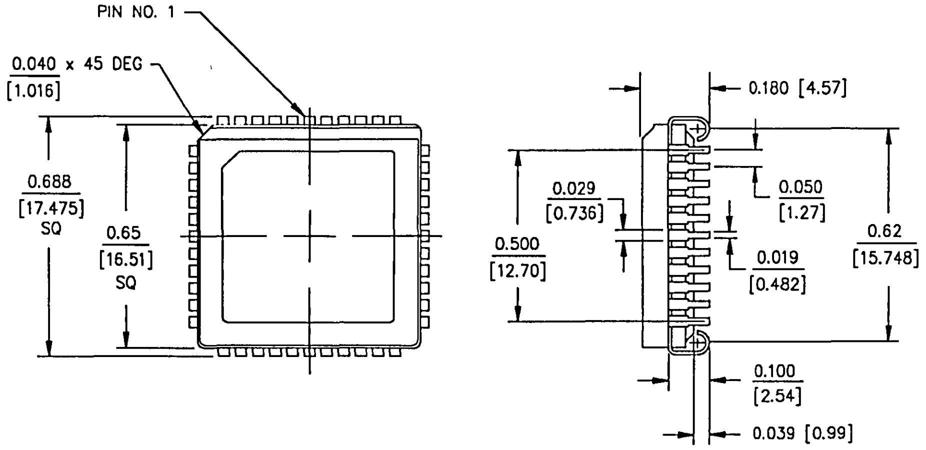
28-Pin Ceramic J-Lead

θ JA = 75–80 °C / W


PIN NO. 1
0.040 x 45 DEG
[1.016]
0.488
[12.192]
SQ
0.45
[11.43]
SQ
0.180 [4.57]
0.029
[0.736]
0.300
[7.62]
0.050
[1.27]
0.42
[10.668]
0.019
[0.482]
0.100
[2.54]
0.040 [1.02]

44-Pin Ceramic J-Lead

θ JA = 58–62 °C / W


PIN NO. 1
0.040 x 45 DEG
[1.016]
0.688
[17.475]
SQ
0.65
[16.51]
SQ
0.180 [4.57]
0.029
[0.736]
0.500
[12.70]
0.050
[1.27]
0.019
[0.482]
0.62
[15.748]
0.100
[2.54]
0.039 [0.99]

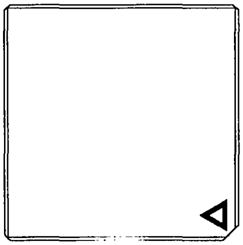
NOTES - Unless otherwise specified:

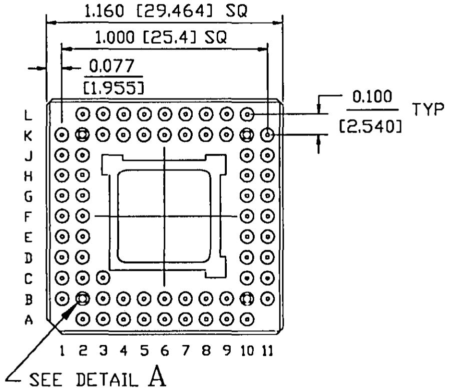
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XX ± 0.01 [0.254] .XXX ± 0.005 [0.127]
3. CERQUAD packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

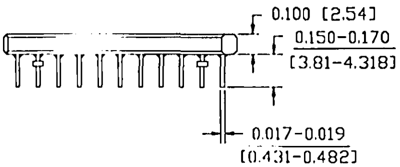
Ceramic Pin Grid Array (PGA) Packages

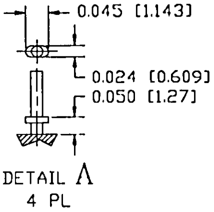
68-Pin Ceramic PGA

θ JA = 35–40 °C/W



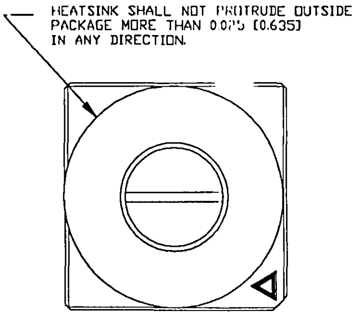

1.160 [29.464] SQ
1.000 [25.4] SQ
0.077
[1.955]
0.100
[2.540]
TYP
L
K
J
H
G
F
E
D
C
B
A
1 2 3 4 5 6 7 8 9 10 11
SEE DETAIL A

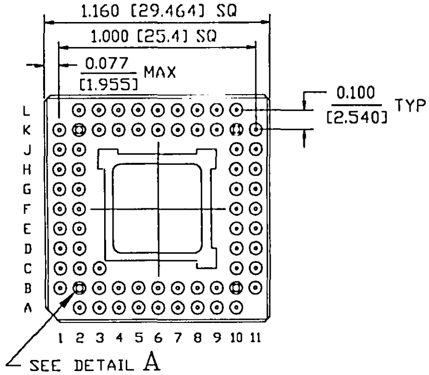

0.100 [2.54]
0.150-0.170
[3.81-4.318]
0.017-0.019
[0.431-0.482]

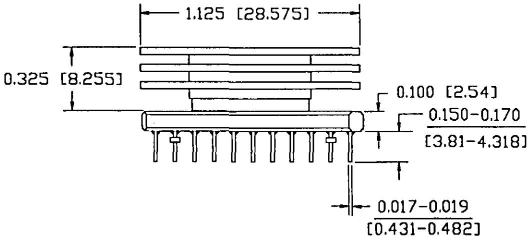

0.045 [1.143]
0.024 [0.609]
0.050 [1.27]
DETAIL A
4 PL

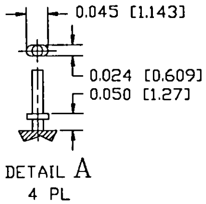
68-Pin Ceramic PGA with Heatsink and Alignment Pin

θ JA = 25–28 °C/W


HEATSINK SHALL NOT PROTRUDE OUTSIDE
PACKAGE MORE THAN 0.025 [0.635]
IN ANY DIRECTION.


1.160 [29.464] SQ
1.000 [25.4] SQ
0.077
[1.955]
MAX
0.100
[2.540]
TYP
L
K
J
H
G
F
E
D
C
B
A
1 2 3 4 5 6 7 8 9 10 11
SEE DETAIL A


1.125 [28.575]
0.325 [8.255]
0.100 [2.54]
0.150-0.170
[3.81-4.318]
0.017-0.019
[0.431-0.482]

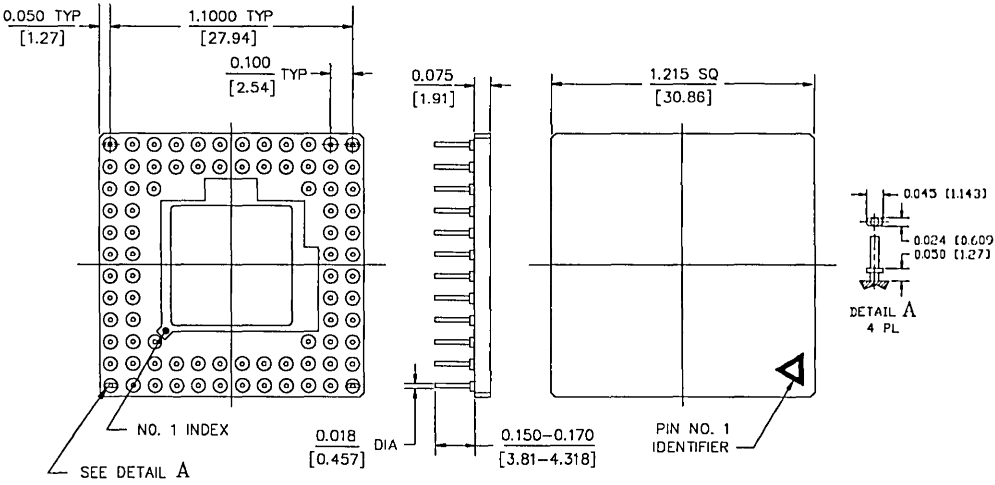

0.045 [1.143]
0.024 [0.609]
0.050 [1.27]
DETAIL A
4 PL

NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]

Ceramic Pin Grid Array (PGA) Packages (continued)

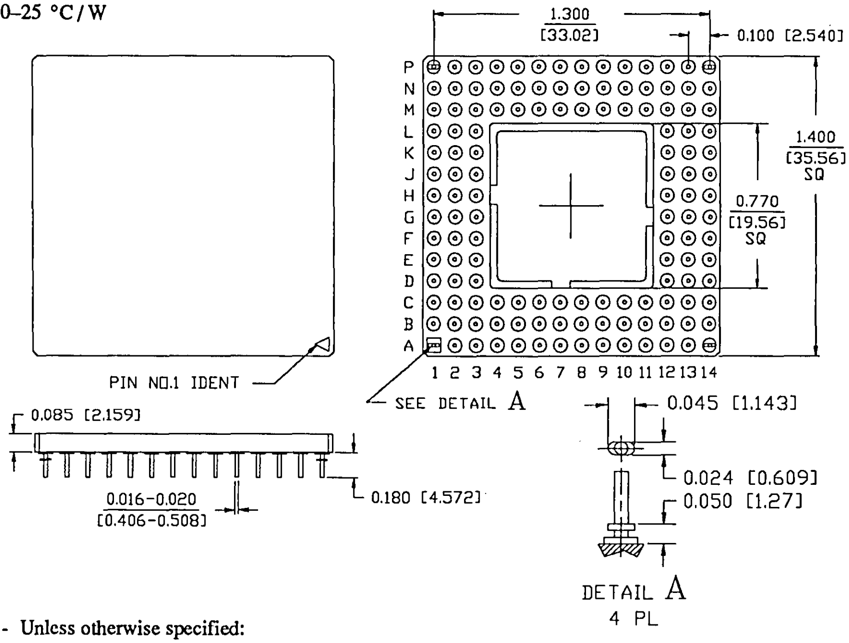
84-Pin Ceramic PGA

θ JA = 30–35 °C / W


0.050 TYP
[1.27]
1.1000 TYP
[27.94]
0.100 TYP
[2.54]
0.075
[1.91]
1.215 SQ
[30.86]
0.045 [1.143]
0.024 [0.609]
0.050 [1.27]
DETAIL A
4 PL
NO. 1 INDEX
SEE DETAIL A
0.018 DIA
[0.457]
0.150–0.170
[3.81–4.318]
PIN NO. 1
IDENTIFIER

132-Pin Ceramic PGA

θ JA = 20–25 °C / W


1.300
[33.02]
0.100 [2.540]
P
N
M
L
K
J
H
G
F
E
D
C
B
A
1 2 3 4 5 6 7 8 9 10 11 12 13 14
1.400
[35.56]
SQ
0.770
[19.56]
SQ
PIN NO.1 IDENT
SEE DETAIL A
0.085 [2.159]
0.016–0.020
[0.406–0.508]
0.180 [4.572]
0.045 [1.143]
0.024 [0.609]
0.050 [1.27]
DETAIL A
4 PL

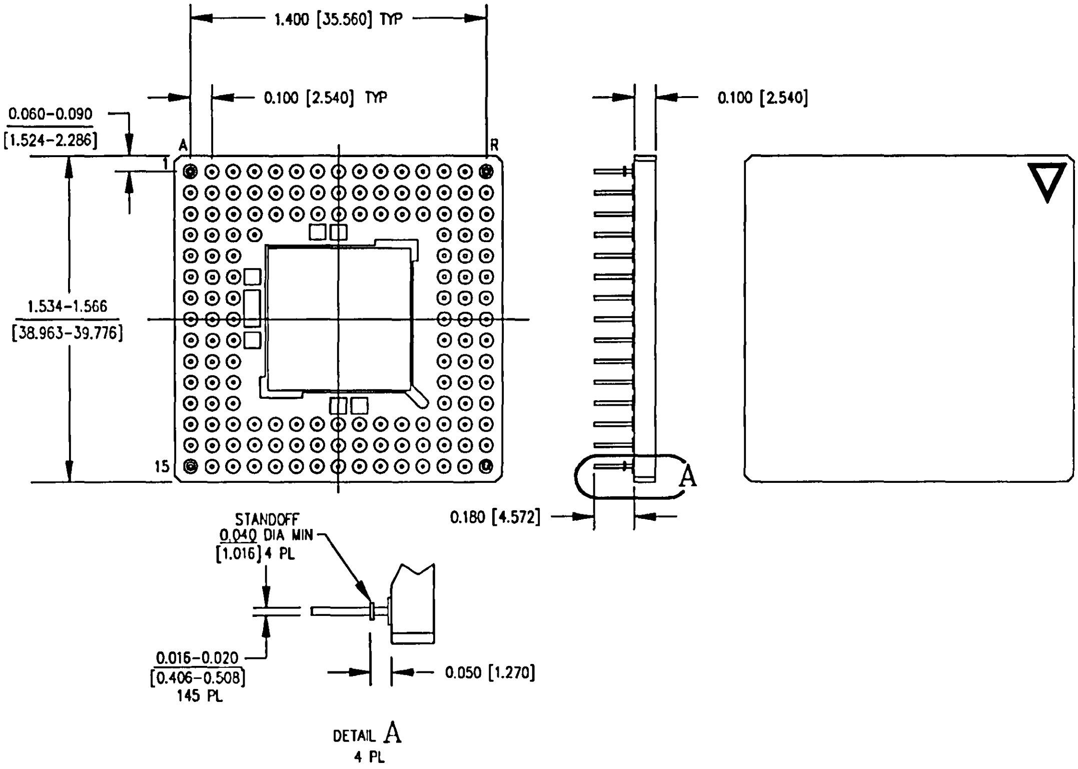
NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]

Ceramic Pin Grid Array (PGA) Packages (continued)

144-Pin Ceramic PGA with Alignment Pin

θ JA = 18–23 °C / W


1.400 [35.560] TYP
0.100 [2.540] TYP
0.060-0.090
[1.524-2.286]
A
R
1
1.534-1.566
[38.963-39.776]
15
0.100 [2.540]
A
0.180 [4.572]
STANDOFF
0.040 DIA MIN
[1.016] 4 PL
0.016-0.020
[0.406-0.508]
145 PL
0.050 [1.270]
DETAIL A
4 PL

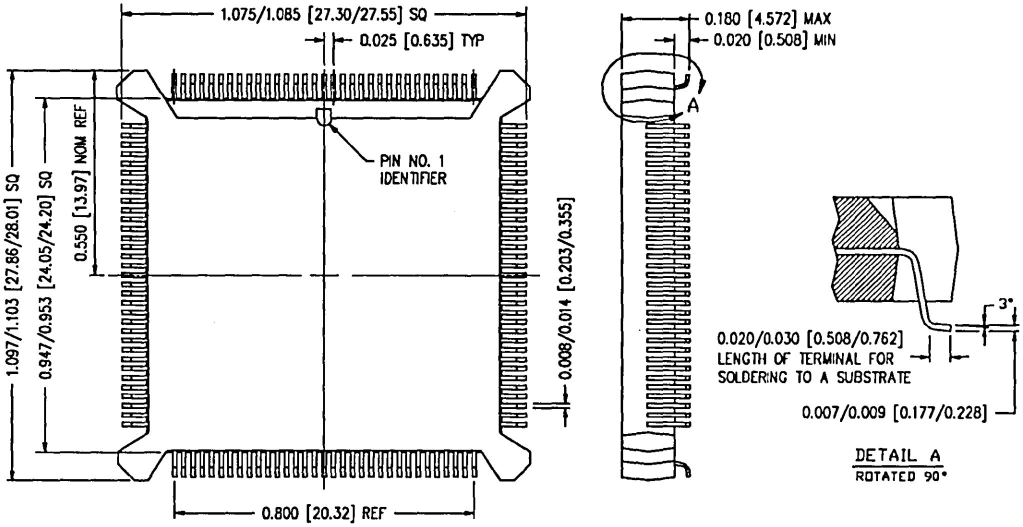
NOTES - Unless otherwise specified:

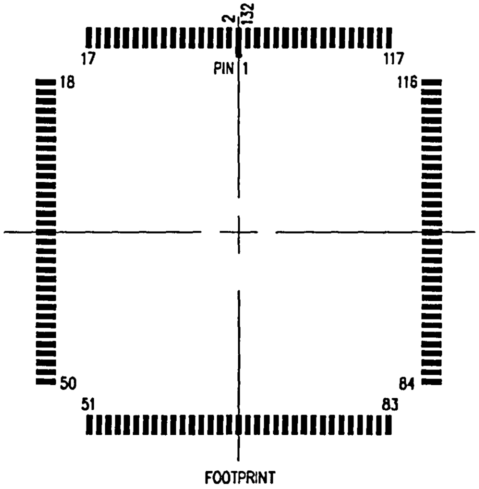
1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]

Plastic Quad Flatpack (PQFP) Packages

132-Pin Plastic Quad Flatpack

θ JA = 35–40 °C / W

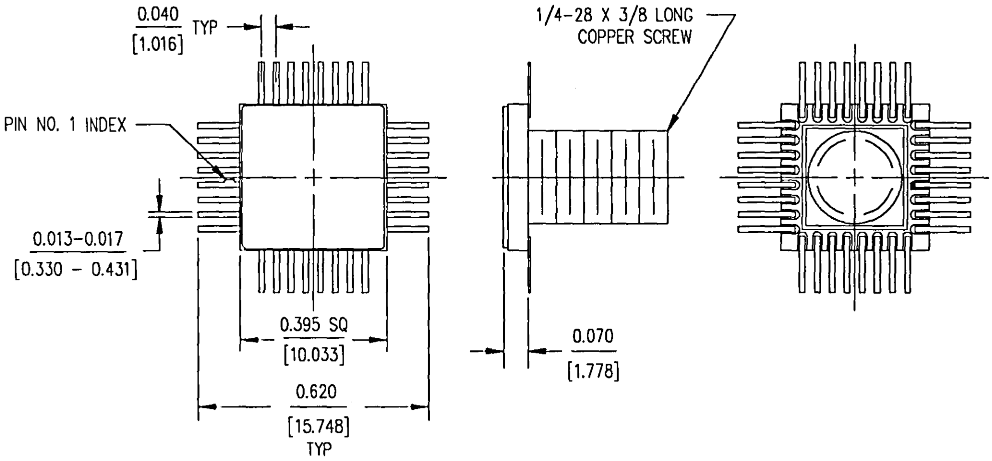

1.075/1.085 [27.30/27.55] SQ
0.025 [0.635] TYP
PIN NO. 1 IDENTIFIER
1.097/1.103 [27.86/28.01] SQ
0.947/0.953 [24.05/24.20] SQ
0.550 [13.97] NOM REF
0.008/0.014 [0.203/0.355]
0.800 [20.32] REF
0.180 [4.572] MAX
0.020 [0.508] MIN
A
3°
0.020/0.030 [0.508/0.762] LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE
0.007/0.009 [0.177/0.228]
DETAIL A
ROTATED 90°


2
132
17
PIN 1
117
18
116
50
84
51
83
FOOTPRINT

Ceramic Flatpack Packages

32-Pin Ceramic Flatpack with Heat Sink

θ JA = 30–35 °C / W


0.040
[1.016]
TYP
PIN NO. 1 INDEX
0.013-0.017
[0.330 - 0.431]
0.395 SQ
[10.033]
0.620
[15.748]
TYP
1/4-28 X 3/8 LONG
COPPER SCREW
0.070
[1.778]

NOTES - Unless otherwise specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: .XXX ± 0.005 [0.127]

SECTION 8

SALES OFFICES

Brooktree Sales Offices

Eastern US Office

Brooktree Corporation
2000 Regency Parkway, Suite 144
Cary, NC 27511
Contact: Bruce Bradford
(919) 467-7418
FAX: (919) 460-9858

Northeastern US Offices

Brooktree Corporation
7 Buckskin Drive
Westboro, MA 01581
Contact: Paul Feldman
Contact: Alan Germain
(508) 870-5999
FAX: (508) 870-5897

Northwestern US Office

Brooktree Corporation
4701 Patrick Henry Drive
Building 12
Santa Clara, CA 95054
Contact: Paul Van Eynde
(408) 980-0812
(408) 732-0923
FAX: (408) 927-9273
Contact: David Kern
(408) 980-0812
(408) 247-1469
FAX: (408) 748-1163

Central US Office

Brooktree Corporation
14785 Preston Road Suite 550
Dallas, TX 75240
Contact: Marc Sultzbaugh
Tel. (214) 490-1945
FAX: (214) 490-8030

Western US Office

Brooktree Corporation
1557 W. 208th St. #A
Torrance, CA 90501
Contact: John Somoza
(213) 320-7427
FAX: (213) 320-7506

European Offices

Brooktree Ltd.
17 Thame Park Road
Thame, Oxon OX9 3XD
United Kingdom
Contact: Lauren Schlicht
Steve Bull
44 844-261989
FAX: 44 844-261906

Brooktree Corporation
Kronstadter Str. 9
D8000 Munchen 80
West Germany
Contact: Reiner Pohl
49 89 937520
FAX: 49 89 9302123

Japanese Office

Brooktree Corporation
Kowa Building No. 9, 4th Floor
1-8-10 Akasaka, Minato-ku
Tokyo 107
Japan
Contact: Jerry Coan
(813) 588-0414
FAX: (813) 505-4120

Asian Office

Brooktree Corporation
9950 Barnes Canyon Road
San Diego, CA 92121
Contact: Dennis Packard
(619) 452-7580
FAX: (619) 452-1249

Die Sales / Nonstandard Packages

Chip Supply
7725 N. Orange Blossom Trail
Orlando, FL 31810-2696
(407) 298-7100
FAX: (407) 290-0164

North American Representatives

Alabama

Novus Group
2905 Westcorp Blvd., Suite 120
Huntsville, AL 35805
(205) 534-0044
FAX: (205) 534-0186
TLX: 910 380 632 9

Arkansas

OM Assoc.
2323 N. Central Expressway
Suite 150
Richardson, TX 75080
(214) 690-6746
FAX: (214) 690-8721

Arizona

Oasis Sales
301 E. Bethany Home Road
Suite A-135
Phoenix, AZ 85012
(602) 277-2714
FAX: (602) 263-9352

California
San Diego / Imperial Co.

Gary Chilcote Assoc.
P.O. Box 1795
2010 Winterwarm Road
Fallbrook, CA 92028
(619) 728-7678
FAX: (619) 728-3738

California
Northern

Quorum
4701 Patrick Henry Dr.
Bldg. 12
Santa Clara, CA 95054
(408) 980-0812
FAX: (408) 748-1163

Colorado

Promotional Tech
4840 Pearl East Circle
Suite 301-E
Boulder, CO 80301
(303) 447-2474
FAX: (303) 447-2033

Promotional Tech
6920 Hillridge Place
Parker, CO 80134
(303) 841-4664
FAX: (303) 841-4202

Connecticut

Comp Rep Associates
117 Church Street
Yalesville, CT 06492
(203) 269-1145
FAX: (203) 269-2819

Delaware

Deltatronics
921 Penllyn Pike
Blue Bell, PA 19422
(215) 641-9930
FAX: (215) 641-9934

District of Columbia

Deltatronics
24048 Sugar Cane Lane
Gaithersburg, MD 20882
(301) 253-0615
FAX: (301) 253-9108

Florida

Dyne-A-Mark
500 E. Semoran Blvd. #18
Casselberry, FL 32707
(407) 831-2822
FAX: (407) 834-4524

Dyne-A-Mark
573 S. Duncan Avenue
Clearwater, FL 34616
(813) 441-4702
FAX: (813) 447-4120

Dyne-A-Mark
1001 NW 62nd St. #108
Ft. Lauderdale, FL 33309
(305) 771-6501
FAX: (305) 772-0114

Georgia

Novus Group
6115-A Oakbrook Parkway
Norcross, GA 30093
(404) 263-0320
FAX: (404) 263-8946

Idaho
Northern

Westerberg & Assoc.
12505 NE Bel-Red Rd. #112
Bellevue, WA 98005
(206) 453-8881
FAX: (206) 453-8758

Idaho
Southern

Promotional Tech
7304 South 300 West #203
Midvale, UT 84047
(801) 566-8919
FAX: (801) 566-9081

Illinois
Northern

Oasis Sales
1101 Tonne Road
Elk Grove Village, IL 60007
(708) 640-1850
FAX: (708) 640-9432

Illinois
Southern

Stan Clothier Co
10000 W. 76th St., Suite D
Eden Prairie, MN 55344
(612) 944-3456
FAX: (612) 944-6904

North American Representatives *(continued)*

Indiana

Valentine Associates
1638 Lincoln Way East
South Bend, IN 46613
(219) 288-7070
FAX: (219) 233-1779

Valentine Associates
P.O. Box 242
1000 N. Madison Ave., #S-2
Greenwood, IN 46142
(317) 888-2260
FAX: (317) 881-4904

Iowa

Stan Clothier Co.
1930 St. Andrews NE
Cedar Rapids, IA 52402
(319) 393-1576
FAX: (319) 393-7317

Kansas

Stan Clothier Co.
805 Clairborne
Olathe, KS 66062
(913) 829-0073
FAX: (913) 829-0429

Kentucky

Valentine Associates
P.O. Box 242
1000 N. Madison Ave., #S-2
Greenwood, IN 46142
(317) 888-2260
FAX: (317) 881-4904

Louisiana

OM Assoc
10500 Richmond Ave., #115
Houston, TX 77042
(713) 789-4426
FAX: (713) 789-4825
TLX: 829 234 50

Maine

Boucher Associates
3 Littleton Road
Westford, MA 01886
(508) 692-7503
FAX: (508) 692-5081

Maryland

Deltatronics
24048 Sugar Cane Lane
Gaithersburg, MD 20882
(301) 253-0615
FAX: (301) 253-9108

Massachusetts

Boucher Associates
3 Littleton Road
Westford, MA 01886
(508) 692-7503
FAX: (508) 692-5081

Michigan

A.P. Associates
P.O. Box 777
810 East Grand River Ave.
Brighton, MI 48116
(313) 229-6550
FAX: (313) 229-9356

Minnesota

Stan Clothier Company
10000 W. 76th St., Suite D
Eden Prairie, MN 55344
(612) 944-3456
FAX: (612) 944-6904

Mississippi

Novus Group
2905 Westcorp Blvd., Suite 120
Huntsville, Al 35805
(205) 534-0044
FAX: (205) 534-0186

Missouri

Stan Clothier Co.
3910 Old Hwy 94 S. Suite 116
St. Charles, MO 63303
(314) 928-8078
FAX: (314)-447-5214

Nebraska

Stan Clothier Co.
10000 W. 76th St., Suite D
Eden Prairie, MN 55344
(612) 944-3456
FAX: (612) 944-6904

Nevada
Excluding Clark Co.

Quorum Technical Sales
4701 Patrick Henry Dr.
Bldg. 12
Santa Clara, CA 95054
(408) 980-0812
FAX: (408) 748-1163

Nevada
Clark Co.

Oasis Sales
301 E. Bethany Home Road
Suite A-135
Phoenix, AZ 85012
(602) 277-2714
FAX: (602) 263-9352

New Hampshire

Boucher Associates
3 Littleton Road
Westford, MA 01886
(508) 692-7503
FAX: (508) 692-5081

New Jersey
Northern

ERA
354 Veterans Memorial Hwy.
Commack, NY 11725
(516) 543-0510
FAX: (516) 543-0758

North American Representatives *(continued)*

New Jersey
Southern

Deltatronics
921 Penllyn Pike
Blue Bell, PA 19422
(215) 641-9930
FAX: (215) 641-9934

New Mexico

Oasis Sales
301 E. Bethany Home Road
Suite A-135
Phoenix, AZ 85012
(602) 277-2714
FAX: (602) 263-9352

New York
Metropolitan

ERA
354 Veterans Memorial Hwy.
Commack, NY 11725
(516) 543-0510
FAX: (516) 543-0758

New York

Quality Components
3343 Harlem Road
Buffalo, NY 14225
(716) 837-5430
FAX: (716) 837-0662
Quality Components
P.O. Box 71
116 Fayette Street
Manlius, NY 13104
(315) 682-8885
FAX: (315) 682-2277

North Carolina

Novus Group
102 L Commonwealth Court
Cary, NC 27511
(919) 460-7771
FAX: (919) 460-5703

North Dakota

Stan Clothier Company
10000 W. 76th St., Suite D
Eden Prairie, MN 55344
(612) 944-3456
FAXL: (612) 944-6904

Ohio

Lyons
4812 Frederick Rd., #101
Dayton, OH 45414
(513) 278-0714
FAX: (513) 278-3609

Lyons
4615 W. Streetsboro Rd.
Richfield, OH 44286
(216) 659-9224
FAX: (216) 659-9227

Lyons
248 N. State Street
Westerville, OH 43081
(614) 895-1447

Oklahoma

OM Assoc
2323 N. Central Expressway
Suite 150
Richardson, TX 75080
(214) 690-6746
FAX: (214) 690-8721
TLX: 629 234 47

Oregon

Westerberg & Assoc.
7165 SW Fir Loop
Portland, OR 97223
(503) 620-1931
FAX: (503) 684-5376

Pennsylvania
Eastern

Deltatronics
921 Penllyn Pike
Blue Bell, PA 19422
(215) 641-9930
FAX: (215) 641-9934

Pennsylvania
Western

Lyons
4615 W. Streetsboro Rd.
Richfield, OH 44286
(216) 659-9224
FAX: (216) 659-9227

Rhode Island

Boucher Associates
3 Littleton Road
Westford, MA 01886
(508) 692-7503
FAX: (508) 692-5081

South Carolina

Novus Group
102 L Commonwealth Court
Cary, NC 27511
(919) 460-7771
FAX: (919) 460-5703

South Dakota

Stan Clothier Company
10000 W. 76th St., Suite D
Eden Prairie, MN 55344
(612) 944-3456
FAX: (612) 944-6904

Tennessee
Eastern

Novus Group
6115-A Oakbrook Parkway
Norcross, GA 30093
(404) 263-0320
FAX: (404) 263-8946

North American Representatives *(continued)*

Tennessee
Western

Novus Group
2905 Westcorp Blvd., Suite 120
Huntsville, AL 35805
(205) 534-0044
FAX: (205) 534-0186

Texas

OM Assoc.
11044 Research Blvd. # A-103
Austin, TX 78759
(512)794-9971
FAX: (512)794-9987

OM Assoc.
10500 Richmond Ave., #115
Houston, TX 77042
(713) 789-4426
FAX: (713) 789-4825

OM Assoc.
2323 N. Central Expressway
Suite 150
Richardson, TX 75080
(214) 690-6746
FAX: (214) 690-8721

Utah

Promotional Tech.
7304 South 300 West #203
Midvale, UT 84047
(801) 566-8919
FAX: (801) 566-9081

Virginia

Deltatronics
1439 Gills Rd.
Powhatan, VA 23139
(804)492-9027
FAX: (804) 492-9422

Vermont

Boucher Associates
3 Littleton Road
Westford, MA 01886
(508) 692-7503
FAX: (508) 692-5081

Washington

Westerberg & Assoc.
12505 NE Bel-Red Rd., #112
Bellevue, WA 98005
(206) 453-8881
FAX: (206) 453-8758

West Virginia

Lyons
248 N. State St.
Westerville, OH 43081
(614)895-1447
FAX: (614)895-1447

Wisconsin
Eastern

Oasis Sales
1305 N. Barker Road
Brookfield, WI 53005
(414) 782-6660
FAX: (414) 782-7921

Wisconsin
Western

Stan Clothier Company
10000 W. 76th St., Suite D
Eden Prairie, MN 55344
(612) 944-3456
FAX: (612) 944-6904

North American Distributors

Alabama

Marshall
3313 Memorial Parkway South
Huntsville, AL 35801
(205) 881-9235
FAX: (205) 881-1490

Reptron
4950 Corporate Drive
Suite 105C
Huntsville, AL 35805
(205)722-9500
FAX: (205) 722-9565

Alaska

Marshall
11715 Northcreek Parkway S.
Suite 112
Bothell, WA 98011
(206) 486-5747
FAX: (206) 486-6964
TLX: 910 443 301 4

Arizona

Anthem
1555 W. 10th Place, Suite 101
Tempe, AZ 85281
(602) 966-6600
FAX: (602) 966-4826

Marshall
9830 S. 51st St., Suite B121
Phoenix, AZ 85044
(602) 496-0290
FAX: (602) 893-9029

Arkansas

Anthem
651 N. Plano Road, Suite 429
Richardson, TX 75081
(214) 238-7100
FAX: (214) 238-0237

Marshall
2045 Chenault Street
Carrollton, TX 75006
(214) 770-0600
FAX: (214) 770-0675

California
LA / Orange / Ventura Co.

Anthem
9131 Oakdale Ave.
Chatsworth, CA 91311
(818) 775-1333
FAX: (818) 775-1302

Anthem
1 Oldfield Drive
Irvine, CA 92718-2809
(714) 768-4444
FAX: (714) 380-4747

Marshall
9710 De Soto Avenue
Chatsworth, CA 91311
(818) 407-0100
FAX: (818) 709-5334

Marshall
One Morgan Circle
Irvine, CA 92718
(714) 458-5305
FAX: (714) 581-5255

California
Northern

Anthem
580 Menlo Drive Suite 8
Rocklin, CA 95677
(916) 624-9744
FAX: (916) 624-9750

Marshall
336 Los Coches Street
Milpitas, CA 95035
(408) 942-4659
FAX: (408) 262-1224

Marshall
3039 Kilgore Avenue, #140
Rancho Cordova, CA 95670
(916) 635-9700
FAX: (916) 635-6044

California
San Diego / Imperial Co.

Anthem
9369 Carroll Park Dr.
San Diego, CA 92121
(619) 453-9005
FAX: (619) 546-7893

Marshall
10105 Carroll Canyon Road
San Diego, CA 92131
(619) 578-9600
FAX: (619) 586-0469

Colorado

Alliance Electronics
10510 Research Ave., S.E.
Albuquerque, NM 87123
(505) 292-3360
FAX: (505) 275-6392

Anthem
770 Wooten Rd. #103
Colorado Springs, CO 80915
(719) 597-4205
FAX: (719) 597-3207

Anthem
373 Inverness Dr. S.
Inglewood, CO 80112
(303) 790-4500
FAX: (303) 790-4532

Marshall
12351 N. Grant Street
Thornton, CO 80241
(303) 451-8383
FAX: (303) 457-2899

Connecticut

Anthem
61 Mattatuck Heights
Waterbury, CT 06705
(203) 575-1575
FAX: (203) 596-3232

Marshall
20 Sterling Dr, Barns Ind. Pk.
P.O. Box 200
Wallingford, CT 06492
(203) 265-3822
FAX: (203) 284-9285

North American Distributors *(continued)*

Delaware

Anthem
Horsham Business Center
355 Business Center Dr.
Horsham, PA 19044
(215) 443-5150
FAX: (215) 675-9875

Marshall
2221 Broadbirch Dr., Suite G
Silver Spring, MD 20904
(301) 622-1118
FAX: (301) 622-0451

District of Columbia

Anthem
9020A Mendenhall Court
Columbia, MD 21045
(301) 995-6640
FAX: (301) 381-4379

Marshall
2221 Broadbirch Dr., Suite G
Silver Spring, MD 20904
(301) 622-1118
FAX: (301) 622-0451

Florida

Marshall
380 S. North Lake Blvd., #1024
Altamonte Springs, FL 32701
(407) 767-8585
FAX: (407) 767-8676

Marshall
2700 W. Cypress Creek Road
Suite D114
Ft. Lauderdale, FL 33309
(305) 977-4880
FAX: (305) 977-4887

Marshall
2840 Scherer Dr., Suite 410
St. Petersburg, FL 33716
(813) 573-1399
FAX: (813) 573-0069

Reptron
3320 N.W. 53rd Street
Suite 206
Fort Lauderdale, FL 33309
(305) 735-1112
FAX: (305) 735-1121

Reptron
14401 McCormick Dr.
Tampa, FL 33626
(813) 855-4656
FAX: (813) 855-7660

Georgia

Marshall
5300 Oakbrook Parkway #140
Norcross, GA 30093
(404) 923-5750
FAX: (404) 923-2743

Reptron
3040 Business Park
Suite H
Norcross, GA 30071
(404) 446-1300
FAX: (404) 446-2991

Idaho

Anthem
1279 W. 2200 S.
Salt Lake City, UT 84119
(801) 973-8555
FAX: (801) 973-8909

Marshall
466 Lawndale Drive, Suite C
Salt Lake City, UT 84115
(801) 485-1551
FAX: (801) 487-0936

Idaho Northern

Anthem
1907 120th Ave. NE, Suite 102
Bothell, WA 98011
(206) 483-1700
FAX: (206) 486-0571

Marshall
11715 Northcreek Parkway S.
Suite 112
Bothell, WA 98011
(206) 486-5747
FAX: (206) 486-6964

Illinois

Anthem
1300 Remington Rd. Suite A
Schaumburg, IL 60173
(708) 884-0200
FAX: (708) 884-0480

Marshall
50 E. Commerce Dr., Unit 1
Schaumburg, IL 60173
(708) 490-0155
FAX: (708) 490-0569

Reptron
1000 E. State Parkway
Suite K
Schaumburg, IL 60195
(708) 882-1700
(708) 882-8904

Indiana

Marshall
6990 Corporate Drive
Indianapolis, IN 46278
(317) 297-0483
FAX: (317) 297-2787

Kansas

Alliance Electronics
10510 Research Ave., S.E.
Albuquerque, NM 87123
(505) 292-3360
FAX: (505)275-6392

Marshall
10413 W. 84th Terrace
Lenexa, KS 66214
(913) 492-3121
FAX: (913) 492-6205

North American Distributors *(continued)*

Kentucky

Marshall
10413 W. 84th Terrace
Lenexa, KS 66214
(913) 492-3121
FAX: (913) 492-6205

Marshall
6990 Corporate Drive
Indianapolis, IN 46278
(317) 297-0483
FAX: (317) 297-2787

Louisiana

Marshall
3313 Memorial Parkway South
Huntsville, AL 35801
(205) 881-9235
FAX: (205) 881-1490

Reptron
4950 Corporate Drive #105C
Huntsville, AL 35805
(205) 722-9500
FAX: (205) 722-9565

Anthem
651 N. Plano Road Suite 429
Richardson, TX 75081
(214) 238-7100
FAX: (214) 238-0237

Maine

Anthem
36 Jonspin Road
Wilmington, MA 01887
(508) 657-5170
FAX: (508) 657-6008

Marshall
33 Upton Drive
Wilmington, MA 01887
(508) 658-0810
FAX: (508) 657-5931

Maryland

Anthem
9020A Mendenhall Court
Columbia, MD 21045
(301) 995-6640
FAX: (301) 381-4379

Marshall
2221 Broadbirch Dr., Suite G
Silver Spring, MD 20904
(301) 622-1118
FAX: (301) 622-0451

Massachusetts

Anthem
36 Jonspin Road
Wilmington, MA 01887
(508) 657-5170
FAX: (508) 657-6008

Marshall
33 Upton Drive
Wilmington, MA 01887
(508) 658-0810
FAX: (508) 657-5931

Michigan

Marshall
31067 Schoolcraft
Livonia, MI 48150
(313) 525-5850
FAX: (313) 525-5855

Reptron
34403 Glendale
Livonia, MI 48150
(313) 525-2700
FAX: (313) 525-3209

Minnesota

Anthem
10025 Valley View Rd., #160
Eden Prairie, MN 55344
(612) 944-5454
FAX: (612) 944-3045

Marshall
3955 Annapolis Lane
Plymouth, MN 55447
(612) 559-2211
FAX: (612) 559-8321

Reptron
5959 Baker Road
Suite 360
Minnetonka, MN 55345
(612) 938-0000
FAX: (612) 938-3995

Mississippi

Marshall
3313 Memorial Parkway South
Huntsville, AL 35801
(205) 881-9235
FAX: (205) 881-1490

Reptron
4950 Corporate Drive #105C
Huntsville, AL 35805
(205) 722-9500
FAX: (205) 722-9565

Missouri

Marshall
3377 Hollenberg Drive
Bridgeton, MO 63044
(314) 291-4650
FAX: (314) 291-5391

Nebraska

Alliance Electronics
10510 Research Ave., S.E.
Albuquerque, NM 87123
(505) 292-3360
FAX: (505) 375-6392

Marshall
10413-15 W. 84th Terrace
Pine Ridge Business Park
Lenexa, KS 66214
(913) 492-3121
FAX: (913) 492-6205

North American Distributors *(continued)*

New Hampshire

Anthem
36 Jonspin Road
Wilmington, MA 01887
(508) 657-5170
FAX: (508) 657-6008

Marshall
33 Upton Drive
Wilmington, MA 01887
(508) 658-0810
FAX: (508) 657-5931

New Jersey
Northern

Anthem
311 Route 46 West
Fairfield, NJ 07006
(201) 227-7960
FAX: (201) 227-9246

Marshall
101 Fairfield Road
Fairfield, NJ 07006
(201) 882-0320
FAX: (201) 882-0095

New Jersey
Southern

Anthem
311 Route 46 West
Fairfield, NJ 07006
(201) 227-7960
FAX: (201) 227-9246

Marshall
158 Gaither Drive
Mt. Laurel, NJ 08054
(609) 234-9100
FAX: (609) 778-1819

Nevada

Anthem
1555 W. 10th Place, Suite 101
Tempe, AZ 85281
(602) 966-6600
FAX: (602) 966-4826

Marshall
9830 S. 51st St., Suite B121
Phoenix, AZ 85044
(602) 496-0290
FAX: (602) 893-9029

Marshall
3039 Kilgore Avenue, #140
Rancho Cordova, CA 95670
(916) 635-9700
FAX: (916) 635-6044

Anthem
580 Menlo Drive Suite 8
Rocklin, CA 95677
(916) 624-9744
FAX: (916) 624-9750

New Mexico

Alliance Electronics
10510 Research Ave., S.E.
Albuquerque, NM 87123
(505) 292-3360
FAX: (505) 275-6392

Marshall
9830 S. 51st St., Suite B121
Phoenix, AZ 85044
(602) 496-0290
FAX: (602) 893-9029

Marshall
1220 Barranca Suite 5-A
El Paso, TX 79935
(915) 593-0706
FAX: (915) 594-1894

New York

Anthem
47 Mall Drive
Commack, NY 11725
(516) 864-6600
FAX: (516) 493-2244

Marshall
275 Oser Avenue
Hauppauge, NY 11788
(516) 273-2424
FAX: (516) 434-4775

Marshall
129 Brown Street
Johnson City, NY 13790
(607) 798-1611
FAX: (607) 797-7031

Marshall
1250 Scottsville Road
Rochester, NY 14624
(716) 235-7620
FAX: (716) 235-0052

North Carolina

Marshall
5224 Green's Dairy Road
Raleigh, NC 27604
(919) 878-9882
FAX: (919) 872-2431

Reptron
5954-A Six Forks Road
Raleigh, NC 27609
(919) 870-5189
FAX: (919) 870-5210

North Dakota

Anthem
10025 Valley View Rd., #160
Eden Prairie, MN 55344
(612) 944-5454
FAX: (612) 944-3045

Marshall
3955 Annapolis Lane
Plymouth, MN 55441
(612) 559-2211
FAX: (612) 559-8321

Ohio

Marshall
3520 Park Center Drive
Dayton, OH 45414
(513) 898-4480
FAX: (513) 898-9363

Marshall
30700 Bainbridge Road, Unit A
Solon, OH 44139
(216) 248-1788
FAX: (216) 248-2312

North American Distributors *(continued)*

Reptron
30640 Bainbridge Road
Solon, OH 44139
(216) 349-1415
FAX: (216) 349-1634

Reptron
404 E. Wilson Bridge Road
Suite A
Worthington, OH 43085
(614) 436-6675
FAX: (614) 436-4285

Oregon

Marshall
9705 S.W. Gemini Dr.
Beaverton, OR 97005
(503) 644-5050
FAX: (503) 646-8256

Anthem
9705 SW Sunshine Court #900
Beaverton, OR 97005
(503) 643-1114
FAX: (503) 626-7928

Pennsylvania
Eastern

Anthem
Horsham Business Center
355 Business Center Drive
Horsham, PA 19044
(215) 443-5150
FAX: (215) 675-9875

Marshall
158 Gaither Drive
Mt. Laurel, NJ 08054
(609) 234-9100
FAX: (609) 778-1819

Pennsylvania
Western

Marshall
401 Parkway View Dr.
Pittsburgh, PA 15205
(412) 788-0441
FAX: (412) 788-0447

Rhode Island

Anthem
36 Jonspin Road
Wilmington, MA 01887
(508) 657-5170
FAX: (508) 657-6008

Marshall
33 Upton Drive
Wilmington, MA 01887
(508) 658-0810
FAX: (508) 657-5931

South Carolina

Marshall
5224 Green's Dairy Road
Raleigh, NC 27604
(919) 878-9882
FAX: (919) 872-2431

Reptron
5954-A Six Forks Road
Raleigh, NC 27609
(919) 870-5189
FAX: (919) 870-5210

South Dakota

Marshall
3955 Annapolis Lane
Plymouth, MN 55441
(612) 559-2211
FAX: (612) 559-8321

Anthem
10025 Valley View Rd., #160
Eden Prairie, MN 55344
(612) 944-5454
FAX: (612) 944-3045

Tennessee
Eastern

Marshall
5300 Oakbrook Parkway #140
Norcross, GA 30093
(404) 923-5750
FAX: (404) 923-2743

Reptron
3040 Business Bark, Suite H
Norcross, GA 30071
(404) 446-1300
FAX: (404) 446-2991

Tennessee
Western

Marshall
3313 Memorial Parkway South
Huntsville, AL 35801
(205) 881-9235
FAX: (205) 881-1490

Reptron
4950 Corporate Drive #105C
Huntsville, AL 35805
(205) 722-9500
FAX: (205) 722-9565

Texas

Marshall
8504 Cross Park Drive
Austin, TX 78754
(512) 837-1991
FAX: (512) 832-9810

Marshall
2045 Chenault Street
Carrollton, TX 75006
(214) 770-0600
FAX: (214) 770-0675

Marshall
2150 Trawood, Suite B160
El Paso, TX 79935
(915) 593-0706
FAX: (915) 594-1894

Marshall
7250 Langtry
Houston, TX 77040
(713) 895-9200
FAX: (713) 462-6714

Anthem
651 N. Plano Rd. Suite 429
Richardson, TX 75081
(214) 238-7100
FAX: (214) 238-0237

North American Distributors *(continued)*

Utah

Anthem
1279 W. 2200 S.
Salt Lake City, UT 84119
(801) 973-8555
FAX: (801) 973-8909

Marshall
466 Lawndale Drive, Suite C
Salt Lake City, UT 84115
(801) 485-1551
FAX: (801) 487-0936

Vermont

Marshall
33 Upton Drive
Wilmington, MA 01887
(508) 658-0810
FAX: (508) 657-5931

Anthem
36 Jonspin Road
Wilmington, MA 01887
(508) 657-5170
FAX: (508) 657-6008

Virginia

Marshall
2221 Broadbirch Dr.
Suite G
Silver Spring, MD 20904
(301) 622-1118
FAX: (301) 622-0451

Anthem
716 A Columbia
Columbia, MD 21046
(301) 995-6640
FAX: (301) 290-9862

Washington

Marshall
11715 Northcreek Parkway S.
Suite 112
Bothell, WA 98011
(206) 486-5747
FAX: (206) 486-6964

Anthem
1907 120th Ave. N.E. Suite 102
Bothell, WA 98011
(206) 483-1700
FAX: (206) 486-0571

West Virginia

Reptron
404 E. Wilson Bridge Road #A
Worthington, OH 43085
(614) 436-6675
FAX: (614) 436-4285

Marshall
2221 Broadbirch Dr.
Suite G
Silver Spring, MD 20904
(301) 622-1118
FAX: (301) 622-0451

Wisconsin
Eastern

Marshall
20900 Swenson Drive
Waukesha, WI 53186
(414) 797-8400
FAX: (414) 797-8270

Wisconsin
Western

Anthem
10025 Valley View Rd. #160
Eden Prairie, MN 55344
(612) 944-5454
FAX: (612) 944-3045

Marshall
3955 Annapolis Lane
Plymouth, MN 55447
(612) 559-2211
FAX: (612) 559-8321

Canada

Marshall
4 Paget Road, Units 10 & 11
Building 1112
Brampton, Ontario CN L6T 5G3
(416) 458-8046
FAX: (416) 458-1613

European Representatives/Distributors

Austria

Moor Lackner
Lamezanstr. 10
Vienna A-1232
Tel. 43 (1) 610.62 x139
FAX: 43 (1) 610.62151
TLX: 847135701

Belgium

Master Chips
Bld. St. Lazare 4
1210 Bruxelles
Tel. 32 (2) 219.14.84
FAX: 32 (2) 217.92.01
TLX: 846 625 00

Denmark

C-88
Kokkedal Industripark 101
2980 Kokkedal
Tel. 45 (42) 244.888
FAX: 45 (42) 244.889
TLX: 855 411 98

C-88 Jylland
Poul Gernessvej 17
7430 Ikast
Tel. 45 (97) 250.816
FAX: 45 (97) 250.815

France

Tekelec Airtronic
BP No. 2
1 Rue Carle Vernet
92315 Sevres Cedex
Tel. 331 (45) 34 7535
FAX: 331 (45) 07 2191
TLX: 842 204 552

Ireland

Memec
Innovation Ctr. Enterprise House
Plassey Technological Park
Limerick
Tel: 353 61 330742/5
FAX: 353 61 331888

Israel

Vectronics, Ltd.
POB 2024
60 Medinat Hayehudim St.
Herzlia B 46120
Tel. 972 52 55 6070
FAX: 972 52 55 6508
TLX: 922 342 579

Italy

Comprel s.p.a.
viale Fulvio Testi, 115
20092 Cinisello Balsamo
Milano
Tel. 39 (02) 6120641
FAX: 39 (02) 6128158
TLX: 843 332484

The Netherlands

Alcom
Esse Baan 1, POB 358
2900 LJ Capelle A/D Ijssel
Tel. 31 (10) 451.9533
FAX: 31 (10) 458.6482
TLX: 844 261 60

Norway

Eltron
Aslakveien 20 F
N-0753 Oslo 7
Tel. 47 (2) 500.650
FAX: 47 (2) 502.777
TLX: 856 771 44

Spain

Semiconductores, S. A.
Ronda General Mitre, 240
08006 Barcelona
Tel. 34 (3) 217.2340
FAX: 34 (3) 217.6598
TLX: 831 977 87

Semiconductores
Talia, 7
28022 Madrid
Tel. 34 (1) 742.2313
FAX: 34 (1) 742.3681
TLX: 831 (52) 47331

Sweden

Martinsson Electronik AS
Instrumentvagen 16, Box 9060
S-12609 Hagersten
Tel. 46 (8) 744.0300
FAX: 46 (8) 744.3403
TLX: 854 130 77

Switzerland

Kontron Electronics AG
In der Luberzen 1
CH-8902 Urdorf
Tel. 441.736.41.11
FAX: 441.734.25.79
TLX: 845822196

United Kingdom

Thame Components Ltd.
Thame Park Road
Thame, Oxon 0X9 3XD
Tel. 44 (84) 426.1188
FAX: 44 (84) 426.1681
TLX: 851 837 917

West Germany

Tekelec Airtronic GmbH
Postfach 152027
Kapuzinerstr. 9
8000 Munchen 2
Tel. 49 (89) 51.640
FAX: 49 (89) 51.6410
TLX: 841 522 241

Tekelec - Essen
Klarastr 1-2
4300 Essen 1
Tel. 49 (201) 791.030
FAX: 49 (201) 791.044
TLX: 8418579954

Tekelec - Frankfurt
Max-Planck-Str 19
6072 Dreieich 1
Tel. 49 (6103) 352.57
FAX: 49 (6103) 352.56
TLX: 8414185858

Tekelec - Hamburg
Neumann-Reichardt Str. 34
2000 Hamburg 70
Tel. 49 (40) 656.7091
FAX: 49 (40) 656.7096
TLX: 8412173605

Tekelec-Ludwigsburg
Leonberger Strasse 46
7140 Ludwigsburg
Tel: 49 (7141) 29391
FAX: 49 (7141) 28683

Japanese Representatives/Distributors

H.Y. Associates
1-10, Sekimachi-kita
3 Chome
Nerima-ku
Tokyo 177
Tel. 81 (3) 929.7111
FAX: 81 (3) 928.0301
TLX: 781 232 268 1

Nissei Electronics
Hitachi Atago Bldg.
15-12, Nishi-Shimbashi
2-Chome
Minato-ku, Tokyo 105
Tel. 81 (3) 504.7921
FAX: 81 (3) 504.7900
TLX: 781 274 81

Asia-Pacific Representatives/Distributors

Australia

Energy Control Pty Ltd
26 Boron Street
Sumner Park Q4074
Brisbane
Tel. 61 (7) 376 2955
FAX: 61 (7) 376 3286
TLX: 790 43778

Promark Electronics-Sidney
P.O. Box 381
Crows Nest N.S.W. 2065
Tel. 612 439 6477
FAX: 612 436 0863
TLX: 790 204 74

Promark Electronics-Melbourne
POB 115, 366 Whitehorse Road
Nunawading Vic 3131
Tel. 613 868-1255
FAX: 613 877-4236
TLX: 79035045

Hong Kong

Lestina International, Ltd.
Room 405, Park Tower
15 Austin Road
Tsimshatsui, Kowloon
Tel. 852 735 1736
FAX: 852 730 5260
TLX: 780 578 15

India

Oriole Services
PB #9275
4 Kurla Industrial Estate
Ghatkopar, Bombay
400 086
Tel. 91 22 511 2973
TLX: 953 117 210 2
FAX: 91 22 511-5810

Korea

Kortronics Enterprise
Room 202, Seojung Bldg.
830-24, Yoksam-Dong
Kangnam-ku 135-080
Seoul
Tel. 82 (2) 562.9055
FAX: 82 (2) 557.1096
TLX: 787 26759

Singapore

Desner Electronics
42 MacTaggart Road
#04-01 MacTaggart Building
Singapore 1336
Tel. 65 285 1566
FAX: 65 284 9466
TLX: 786 391 91

Taiwan R.O.C.

Sertek
5FL 135 Sec. 2,
Chien Kuo N. Rd.
Taipei 10479
Tel. 886 (2) 501.0055
FAX: 886 (2) 501.2521
TLX: 785 237 56

Taiwan EI-EN
3F, No. 70 Sec 2, Jen-ai Road
Taipei
Tel. 886 (2) 322.5970
FAX: 886 (2) 392.3028

SECTION 9

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Bt462	170, 135, 110, 80 MHz Single 8-bit RAMDAC with 1024 x 8 RAM, 256 x 8 Alternate RAM, 3:1, 4:1, or 5:1 Multiplexed Pixel Inputs	4 - 241
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	Low Resolution				Medium Resolution		High Resolution			Ultra High Resolution		
RESOLUTION	512x512	640x400	640x480	768x576	1024x768	1024x800	1Kx1K	1152x900	1280x1K	1536x1152	2Kx1536	2Kx2K
VIDEORATE	20 MHz	20 MHz	25 MHz	35 MHz	66 MHz	75 MHz	95 MHz	95 MHz	110 MHz	165 MHz	250 MHz	360 MHz
LINERATE	31.5 KHz	24 KHz	31.5 KHz	37 KHz	48 KHz	52 KHz	63 KHz	63 KHz	65 KHz	85 KHz	110 KHz	150 KHz
REFRESHRATE	60 Hz	60 Hz	60 Hz	60 Hz	60 Hz	60 Hz	60 Hz	66 Hz	60 Hz	60 Hz	60 Hz	60 Hz
#256KVDRAMS	1	1	2	2	3	4	4	4	5	8	12	16
APPLICATION	Imaging	PC-AT	VGA	EVGA	PC Add-on	PC Add-on	Imaging	SUN WS	Eng WS	Eng WS	Super-Res	FAA
VIDEODACS												
Triple 8	Bt103	Bt103	Bt103	Bt103	Bt103	Bt103	Bt109	Bt109	Bt109	Bt109	Bt109	
Single 8	Bt102 Bt106	Bt102 Bt106	Bt102 Bt106	Bt102 Bt106	Bt102	Bt102						Bt107
SHIFTER												
5 x 8 OR 4 x 10										Bt424	Bt424	Bt424
CURSOR GEN												
64 x 64	Bt431	Bt431	Bt431	Bt431	Bt431	Bt431	Bt431	Bt431	Bt431	Bt431		
CLOCK GEN												
250 MHz					Bt438	Bt438	Bt438	Bt438	Bt438	Bt438	Bt438	
200 MHz					Bt439	Bt439	Bt439	Bt439	Bt439	Bt439		
RAMDACS												
16 x 12	Bt450	Bt450	Bt450	Bt450	Bt450							
256 x 12 4/5:1					Bt451	Bt451	Bt451	Bt451	Bt451			
256 x 24	Bt453 Bt473 Bt478 Bt477	Bt453 Bt473 Bt478 Bt477	Bt453 Bt473 Bt478 Bt477	Bt453 Bt473 Bt478 Bt477	Bt453 Bt473 Bt478 Bt477 Bt474	Bt473 Bt478 Bt477 Bt474	Bt468	Bt468	Bt468	Bt468		
16 x 12 4:1					Bt454 Bt455	Bt454 Bt455	Bt454 Bt455	Bt454 Bt455	Bt454 Bt455	Bt454 Bt455		
256 x 12	Bt456	Bt456	Bt456	Bt456	Bt456							
256 x 8 4/5:1					Bt457	Bt457	Bt457	Bt457	Bt457			
256 x 24 4/5:1					Bt458	Bt458	Bt458	Bt458	Bt458			
256 x 24 1/4/5:1					Bt459	Bt459	Bt459	Bt459	Bt459			
1K x 83 3/4/5:1					Bt461 Bt462	Bt461 Bt462	Bt461 Bt462	Bt461 Bt462	Bt461 Bt462	Bt461 Bt462		
1024 x 24	Bt479	Bt479	Bt479	Bt479	Bt479	Bt479						
256 x 18	Bt471 Bt475 Bt476	Bt471 Bt475 Bt476	Bt471 Bt475 Bt476	Bt471 Bt475 Bt476	Bt471 Bt475 Bt476	Bt471 Bt475 Bt476						
256 x 8										Bt492	Bt492	Bt492
512 x 24					Bt460	Bt460	Bt460	Bt460	Bt460			
528 x 8 1/2/4:1							Bt463	Bt463	Bt463	Bt463		
ECL/TTL TRANSCEIVER												
OCTAL 10KH							Bt501	Bt501	Bt501	Bt501	Bt501	Bt501
OCTAL 100KH							Bt502	Bt502	Bt502	Bt502	Bt502	Bt502

Brooktree Sales Offices

Eastern US Office

Brooktree Corporation
2000 Regency Parkway, Suite 144
Cary, NC 27511
Contact: Bruce Bradford
(919) 467-7418
FAX: (919) 460-9858

Northeastern US Offices

Brooktree Corporation
7 Buckskin Drive
Westboro, MA 01581
Contact: Paul Feldman
Contact: Alan Germain
(508) 870-5999
FAX: (508) 870-5897

Northwestern US Office

Brooktree Corporation
4701 Patrick Henry Drive
Building 12
Santa Clara, CA 95054
Contact: Paul Van Eynde
(408) 980-0812
(408) 732-0923
FAX: (408) 927-9273
Contact: David Kern
(408) 980-0812
(408) 247-1469
FAX: (408) 748-1163

Central US Office

Brooktree Corporation
14785 Preston Road Suite 550
Dallas, TX 75240
Contact: Marc Sultzbaugh
Tel. (214) 490-1945
FAX: (214) 490-8030

Western US Office

Brooktree Corporation
1557 W. 208th St. #A
Torrance, CA 90501
Contact: John Somoza
(213) 320-7427
FAX: (213) 320-7506

European Offices

Brooktree Ltd.
17 Thame Park Road
Thame, Oxon OX9 3XD
United Kingdom
Contact: Lauren Schlicht
Steve Bull
44 844-261989
FAX: 44 844-261906

Brooktree Corporation
Kronstadter Str. 9
D8000 Munchen 80
West Germany
Contact: Reiner Pohl
49 89 937520
FAX: 49 89 9302123

Japanese Office

Brooktree Corporation
Kowa Building No. 9, 4th Floor
1-8-10 Akasaka, Minato-ku
Tokyo 107
Japan
Contact: Jerry Coan
(813) 588-0414
FAX: (813) 505-4120

Asian Office

Brooktree Corporation
9950 Barnes Canyon Road
San Diego, CA 92121
Contact: Dennis Packard
(619) 452-7580
FAX: (619) 452-1249

Brooktree®
Brooktree Corporation
9950 Barnes Canyon Road
San Diego, CA 92121-2790
(619) 452-7580
1 (800) VIDEO-IC
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