B 1700

DISK PACK CONTROL I

TECHNICAL MANUAL

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INTRODUCTION AND OPERATION

INTRODUCTION

The B 1700 Disk Pack Control I, also referred to as DPC, is part of the B 1700 Disk Pack Subsystem. This subsystem consists of the following units.

a. B 1700 Disk Pack Control I (DPC).

b. Disk Pack Electronics Controller (DPEC).

c. Disk Pack Drives (DPD).

The disk pack subsystem (figure 1-1) is comprised of one DPC, one DPEC, and from one to eight disk pack drives.

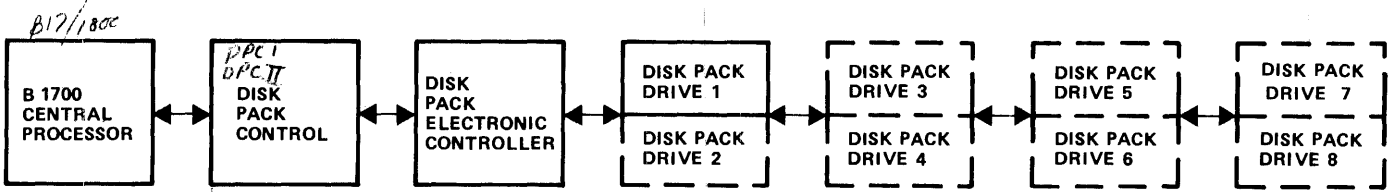


Figure 1-1. B 1700 Disk Pack Subsystem

DISK PACK CONTROL I

The disk pack control I consists of three B 1700 size cards in an independent four-card backplane. The disk pack control performs the following functions:

a. Provides an interface between the B 1700 Central Processor and the DPEC.

b. Provides data storage for three sectors of disk pack information.

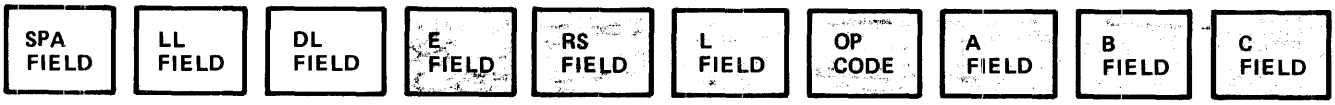
c. Decodes and interprets the operation (op) code from the central processor to the DPEC.

d. Assembles a result descriptor based on information received from the DPEC.

The DPC receives the I/O descriptor operators that are fetched by the I/O driver from main memory. The DPC interprets the operation specified by the descriptor operator and its variants, and initiates the required action in the DPEC. At the completion of the operation, the DPC generates a result descriptor, using information received from the DPEC. The I/O driver stores the result descriptor in the result status (RS) field of the I/O descriptor. The I/O driver also returns an interrupt message, if requested.

I/O DESCRIPTOR

The I/O descriptor consists of ten 24-bit fields as shown in figure 1-2. The following is a detailed description of the functions and usage of each field.



SPA ADDRESS OF SEARCH PARAMETERS (SEARCH OP).
LL RESERVED.
DL RESERVED.
E ENDING ADDRESS.
RS RESULT STATUS (ALSO LOCATION OF RESULT DESCRIPTOR).
L LINK ADDRESS.
OP OP, VARIANTS AND UNIT NUMBER.
A START ADDRESS OF DATA
B END PLUS ONE, ADDRESS OF DATA.
C START ADDRESS OF DATA(FILE ADDRESS).

Figure 1-2. DPC I/O Descriptor

SPA Field

The search parameters field contains the address of the search parameters.

(LL) Field

This 24-bit field is reserved for future assignment.

DL Field

This 24-bit field is reserved for future assignment.

E Field

After an operation, the I/O driver stores the final incremented A address in the E field. The address in this field points to the memory location where the next bit of data would normally be stored. For Read, Write, and Search operations, the E field address is normally equal to the B address unless the operation is terminated because of a "not-ready", address error, time-out, command transmission error, write lock-out (Write operation only), or the end of the search table or entry (Search operation only). The E field is not defined after a Test operation or Stop operation.

During some operations the E field is used by the I/O driver to save the incremented A address between buffer loads to the DPC.

RS Field

After completion of an operation and after the actual ending address has been stored in the E field, the I/O driver exchanges the result status information in the result status field, with the interrupt control information.

Prior to and during an operation, the first 15 bits of the RS field are used to store temporary flags for the I/O driver. The last nine bits are used to indicate dynamic interrupt information.

L Field

After storing the result status information and after returning any requested interrupt message, the I/O driver normally fetches the Link address from the L field. The Link address is a 24-bit address pointing to the RS field of the next I/O descriptor to be executed.

OP Code, Variant(s) and Unit Number

The op code, variant(s) and unit number are contained in a 24-bit field. The leftmost three bits are used to designate the majority of operator codes; the rightmost four bits are used to designate the unit. Operator codes extending beyond three bits are indicated by 111 in the first three bit positions. The remaining bits are used for variants, discussed under the description of the individual operators.

All bits unassigned are reserved and must be zeros.

A and B Fields

For most operators, the A and B fields are 24-bit fields containing the beginning and ending memory bit addresses, respectively, for a given operation. These addresses normally define the number of bits to be transferred. If the value in A equals the value in B, no data is transferred.

For the test descriptor the A-field and B-field addresses are not used.

C Field (File Address)

The File address, a binary sequential address contained in a 24-bit field, is used to designate a particular sector on a disk pack as the starting point for all operations except Test and Stop.

For type-225 Disk Pack Drives, the maximum binary file address is 485,169, corresponding to a maximum capacity of 87,330,600 eight bit bytes for each removable disk pack.

On each track there are 60 primary sectors, except for the first head (head 0) which has 55 primary sectors followed by five alternate sectors. The alternate sectors are used for relocating sectors which were unrecordable in an original position. The DPEC provides automatic switching from a sector flagged as unrecordable to the spare sector assigned as its alternate.

The DPEC provides for continuous operation from sector to sector, from track to track (surface to surface), and from cylinder to cylinder, but not from unit to unit. The format for each track is shown in figure 1-3.

The binary sequential file address corresponds to contiguous sectors (excluding spares) beginning at sector 0 (first sector after index) on head 0, cylinder 0 and continuing by sector, head, and cylinder in that order. Although 60 sectors are on the first surface (head 0), only 55 are addressable by means of the binary file address. Alternate sectors are not addressable in this address group unless they have been assigned by relocation. The sequential binary file address is related to the actual disk pack cylinder, head, and sector, as follows:

$0 \leq$	FA modulo 1195 <55	= head 0.	
$55+(n-1)\ (60) \leq$	FA modulo 1195 <55 +(n) (60)	= head n	n = 1 to 19.
$(n-1)\ (1195) \leq$	FA <(n) (1195)	= cylinder n	n = 0 to 405.

Sectors are 0 through 54 for head 0.
Sectors are 0 through 59 for heads other than 0.
Heads are 0 through 19.
Cylinders are 0 through 405 for Type 225 Disk Drives, and 0 through 203 for Type 215 Disk Drives.

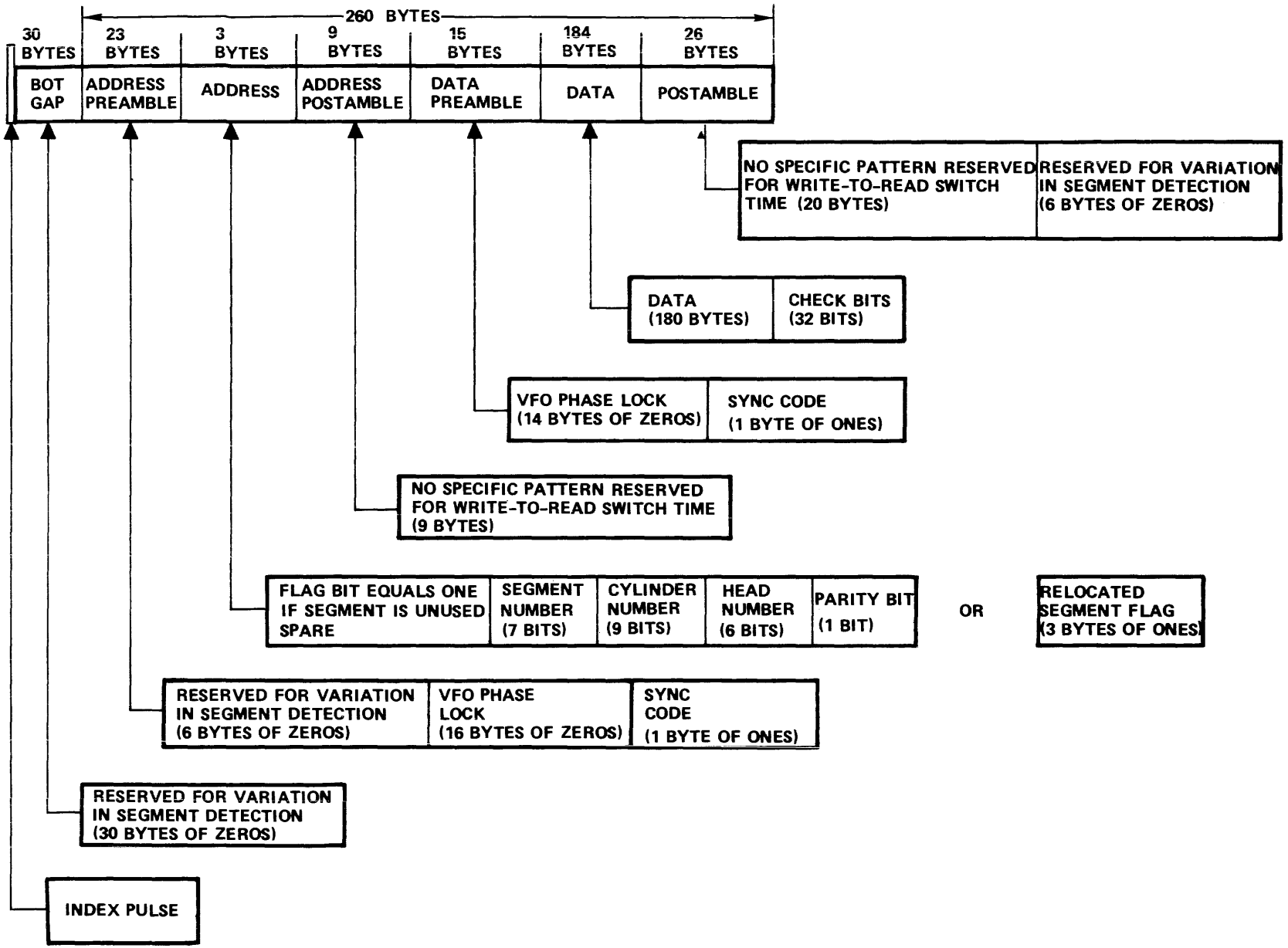


Figure 1-3. Disk Pack Format

I/O OPERATORS

The following are the operators for the B 1700 Disk Pack Control I:

a. Read.

b. Write.

c. Initialize.

d. Relocate.

e. Test.

f. Pause.

g. Stop.

h. Search.

Each operator consists of a 24-bit field. The first three bit positions (leftmost three bit positions as displayed on the B 1700 console) are reserved for the type of operation. The last four bit positions are reserved for the unit number. The rest of the positions are reserved for variants.

Read Operator

The read operator (figure 1-4) provides the capability to read data from the disk pack, starting at the given file address (C field), into ascending memory locations that begin at the location specified by the A address and ends at the location specified by the B address minus one. A complete segment need not be stored but will be parity checked. The DPEC transmits 90 sixteen-bit data words and two error-code words to the DPC for each sector read. In addition, one 16-bit result status word reflecting the accumulation status of the entire operation up to that point is transmitted immediately following the error code for each sector. Only the data bits are stored, however, unless specified otherwise by variant E = 1 or M = 1.

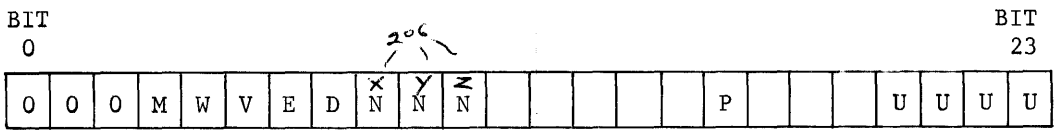


Figure 1-4. Read Operator

Variant Control Function

The functions of the read operator variants are as follows:

M = 0 Reads data as previously described.

M = 1 Reads the actual sync code, the actual address, and, whenever possible, the actual data, the data check bits, and postamble as recorded at the designated segment. In addition, the control returns the 16-bit result from the DPEC. In the case of a relocated sector, the sync code and the address field returned will contain all 1's. If NNN ≠ 000, the address field read is the one designated by NNN (figure 1-4). A parity error or an incorrect address does not terminate the operation. The position of the sector is obtained in the DPEC by counting from the index. If M = 1, variants EP must equal 00.

Variant	Control Function
W = 0	Does not wait if "busy exchange" condition exists. If the interface line exchange busy is true, the I/O control terminates the operation and returns the final result status with bits 0, 1, and 16 equal to 110 respectively.
W = 1	Waits if a busy exchange condition exists.
V = 0	Enables automatic restore after a seek error.
V = 1	Disables automatic restore after a seek error.
E = 0	Reads data as described in this subsection.
E = 1	Returns the data, the 32-bit error-check code, and the DPEC 16-bit result word for each segment read. Returns the final result status for the operation with bits 16, 21, 22, and 23 equal to 0001 respectively. If E = 1, all other variants (except W) must be equal to 0.
NNN = 000	Normal sector address. No diagnostic nor offset read.
NNN = 1-5	Indicates the spare sector on head 0 of the designated cylinder when M = 1 or P = 1. The file address must designate a sector on head 0.
NNN = 1&5	Indicates offset right (in) and offset left (out), respectively, if MP = 00.
P = 1	Verify. The DPC treats this operation identically to that of a read operation except that the verify operator is sent to the DPEC. P = 1 with N = 1-5 is not permitted if the specified spare sector has been assigned. If P = 1, variant M must equal 0.
UUUU = 0...15	Indicates unit number (spindle).
D = 0	Reads data as described in the first paragraph of "Read Operator".
D = 1	Transfers eight bytes (64-bits) of disk pack subsystem status information to the I/O driver. The data is received from the DPEC and stored in the read buffers, as in a normal read operation. The status condition indicated by each bit of the data is as follows:

Bit	Status or Condition
1	Reserved for cylinder 512 address decode (not presently used).
2	Cylinder 256 address decode.
3	Cylinder 128 address decode.
4	Cylinder 64 address decode.
5	Cylinder 32 address decode.
6	Cylinder 16 address decode.
7	Cylinder 8 address decode.
8	Cylinder 4 address decode.

Bit	Status or Condition
9	Cylinder 2 address decode.
10	Cylinder 1 address decode.
11	Head 16 address decode.
12	Head 8 address decode.
13	Head 4 address decode.
14	Head 2 address decode.
15	Head 1 address decode.
16	Reserved (spare).
17	Segment 32 address decode.
18	Segment 16 address decode.
19	Segment 8 address decode.
20	Segment 4 address decode.
21	Segment 2 address decode.
22	Segment 1 address decode.
23	Old cylinder ≠ new cylinder.
24	Op 1.
25	Op 2.
26	Op 3.
27	Unit 2^2.
28	Unit 2^1.
29	Unit 2^0.
30	N^1.
31	N^2.
32	N^3.
33	Address sync start fault.
34	Data sync start fault.
35	Head equal fault.
36	Cylinder equal fault.
37	Head forced to zero.

Bit	Status or Condition
38	Missing sector pulse fault.
39	Write drive data is not present.
40	Read data has not been received.
41	DPEC DC low voltage warning.
42	Seek incomplete.
43	Sequence count = 1-9.
44	Missing R/W clock.
45	Fan blower failure.
46	Spare.
47	Spare.
48	Spare.
49-64	Reserved for future use.

Write Operator

The write operator (figure 1-5) provides the capability to write data to the disk pack, starting at the given file address (C field), from ascending memory locatons, beginning at the location specified by the A address and ending at the location specified by the B address minus one. Zero-fill bits are written to complete the last segment. The DPC transmits 90, sixteen-bit data words per sector to the DPEC. In addition, the DPC sends two dummy words at the end of each sector, during which time the DPEC is writing an error code on the disk.

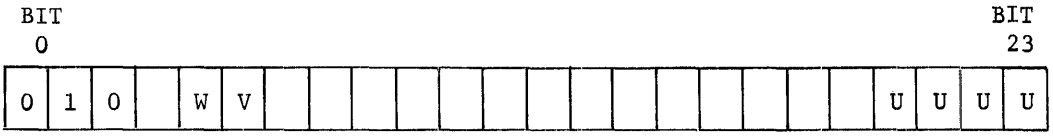


Figure 1-5. Write Operator

The functions of the write operator variants are as follows:

Variants	Control Function
W = 0	Does not wait if a busy exchange condition exists. If the interface line "exchange busy" is true, terminates the operation and returns the final result status with bits 0, 1, and 16 equal to 110.
W = 1	Wait if a busy exchange condition exists.
V = 0	Enables automatic restore after a seek error.
V = 1	Disables automatic restore after a seek error.
UUUU = 0....15	Unit number (spindle).

Initialize Operator

The initialize operator (figure 1-6) provides the capability to write all format bits in all tracks starting after the index pulse on the track decoded from the given file address (C field) and continuing through the entire track or pack. Spare sectors are also initialized. The data pattern consists of the sync code (eight 1's) and the actual sector address (repeated 45 times for each sector). The DPC treats this operation exactly as if it were a write operation. However, the DPEC does normally not accept more than one 16-bit data transfer.

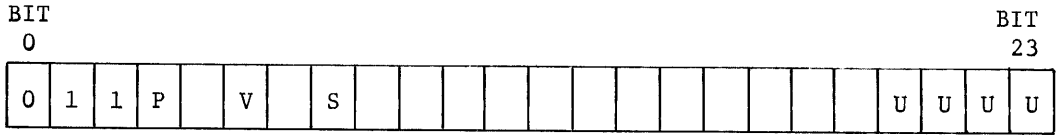


Figure 1-6. Initialize Operator

The functions of the initialize operator variants are as follows:

Variants	Control Function
P = 1	Initializes the entire disk pack.
P = 0	Initializes one track only.
V = 0	Enables automatic restore after a seek error.
V = 1	Disables automatic restore after a seek error.
S = 0	Initializes as described previously in the subsection "Initialize Operator" and ignores the data received from the system.
S = 1	Initializes as described previously in the subsection "Initialize Operator," except the data pattern is written with the first 16 bits of data received from the system and the data is repeated 90 times for each sector.
UUUU = 0...15	Unit number (spindle).

Relocate Operator

The relocate operator (figure 1-7) provides the capability to flag the address field of the sector designated by the given file address (C field) with a relocated address flag pattern. In addition, the relocate operator writes the spare sector on the track specified by NNN with the address of the relocated sector and with a data pattern. This portion consists of the sync code (eight 1's) and the sector address of the relocated sector repeated 45 times. Both the original sector and the relocated sector are located by counting from the index; other sectors are unaffected. Spare sectors are to be allocated in reverse order, that is, N = 5 first. N = 5 designates the last physical sector on the track.

The DPC treats this operation exactly as if it were a write operation. However, the DPEC normally does not accept more than one 16-bit data transfer.

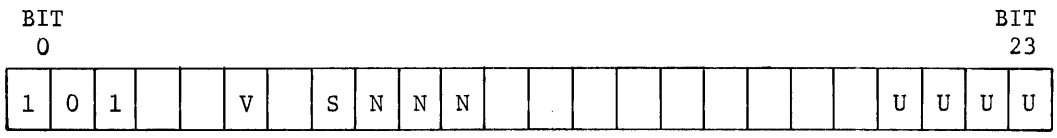


Figure 1-7. Relocate Operator

The functions of the relocate operator are as follows:

Variants	Control Function
V = 0	Enables automatic restore after a control function/description seek error.
V = 1	Disables automatic restore after a seek error.
S = 0	Initializes as described above and ignores the data received from the system.
S = 1	Initializes as described above, but writes the data pattern with the first 16 bits of data received from the system and repeats the data 90 times.
NNN = 1-5	Indicates the spare sector on track 0 of the designated cylinder.
UUUU = 0...15	Indicates unit number (spindle).

Test Operator

The test operator (figure 1-8) examines a selected disk drive and returns a result descriptor containing the following information:

a. The "ready" status of the disk drive.

b. Disk drive identification (ID).

c. Whether the disk drive has a write-lockout condition.

d. The disk drive exchange configuration.

e. Whether the disk drive is in a seek status.

f. Whether the disk drive has a transmission error.

g. The DPC identification.

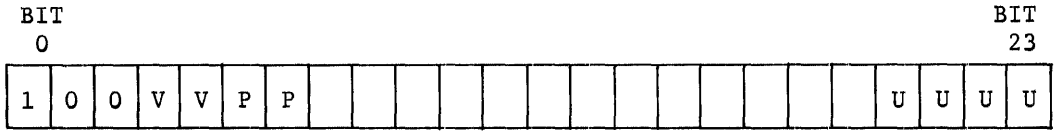


Figure 1-8. Test Operator

The functions of the test operator variants are as follows:

Variants	Control Function
VVPP = 0000	A result is returned immediately and unconditionally.
VVPP = 1000	A result is returned only if the disk drive is present, ready, and not seeking. Otherwise, the next I/O descriptor is unlocked and fetched.
VVPP = 0100	A result is returned only if the disk drive is not present or not ready. Otherwise, the next I/O descriptor is unlocked and fetched.

Variants	Control Function
VVPP = 0001	The disk drive is placed off-line for disk pack removal, if the disk drive is present and available.
VVPP = 0010	A 1 to 2 millisecond pause is effected before a service request (SR) is returned to the I/O driver. Bit 16 of the result descriptor is suppressed.
VVPP = XXXX	Combinations other than those previously specified must not be used.

Pause Operator

The pause operator (figure 1-9) provides the capability for the control to pause 1 to 2 milliseconds before a service request (SR) is returned to the system. Bit 16 of the result descriptor is suppressed to indicate that the result is not to be stored.

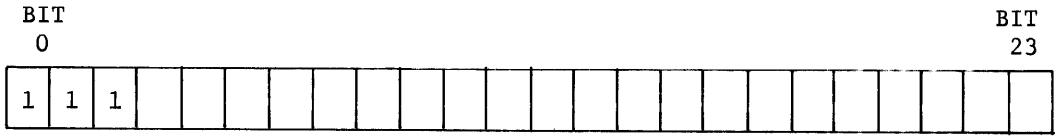


Figure 1-9. Pause Operation

Stop Operator

The stop operator (figure 1-10) provides the capability for the control to idle after returning a result. If requested, it can generate an interrupt. The stop operator is interpreted by the I/O driver and is not sent to the DPC.

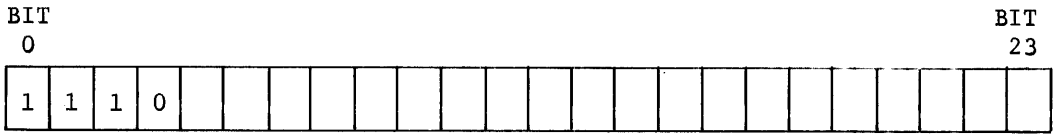


Figure 1-10. Stop Operator

Search Operator

The search operator (figure 1-11) provides the capability to read data from the disk pack. The data read starts at the given file address (C field) and is placed into ascending memory locations beginning at the location specified by the A address and ending at the end location specified by the B address minus one. As the data is being read and stored, the search operator binarily compares the key field in the memory location given in the search parameters with the key field in each table entry. This comparison starts with the specified entry number until an equal condition is detected or until the entry list is exhausted. Detection of an equal condition does not terminate the storing of data. The search operator is generated by system software and is not contained in the linked list of I/O descriptors.

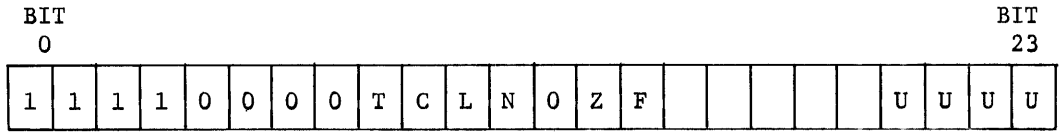


Figure 1-11. Search Operator

The functions of the search operator variants are as follows:

Variant	Control Function/Description
T = 0	Does not store the entire table but stores only the table entry, if any, which terminated the search operation. If there is no such entry, stores only the control information following the last table entry.
T = 1	Reads data as described in the first paragraph of "Search Operator."
C = 0	Reads data as described in the first paragraph of "Search Operator."
C = 1	Reads data as described in the first paragraphs of "Search Operator" but also terminates the comparison portion of the operation if a key field is encountered that is less than the key given in memory.
L = 0	Causes an exit from the operation in a normal manner.
L = 1	Causes an exit from the operation, using the Link-M address if a match is detected and if the first bit of the 17-bit file address displacement in the matched entry is a zero; otherwise, the exit occurs in a normal manner. If the exit is by means of the Link-M address, modifies the file address in memory for the next operation by adding to it the 17-bit file address displacement obtained from this operation.
N = 0	Uses the number of table entries given in the I/O descriptor search parameters field.
N = 1	Uses the number of table entries given by the first 16 bits read from the disk. The number of table entries given in the I/O descriptor search parameter field is ignored.
Z = 0	Reads data as described in the first paragraph of "Search Operator."
Z = 1	Does not compare zone bits (upper four bits) of each 8-bit group.
F = 0	Reads data as described in the first paragraph of "Search Operator.
F = 1	Reads first entry following offset; does not compare.

For additional information on the search operator, refer to the B 1700 Data Management System II (DMSII) Reference Manual, Form Number 1089794.

The following search parameters and associated bit lengths are included for reference only.

Bits	Description
8	Byte displacement from start of the table to the table entry number.
16	Enter number of the first table entry to be searched.
12	Reserved for I/O driver use.
12	Length, in bytes, of a table entry.
12	Bit displacement from start of the table entry to the key field.
12	Length, in bits, of the key field.

Bits	Description
16	Total number of table entries. At the conclusion of the operation the number is set to 0 if no match is detected; otherwise, it is set to 1 plus the number of table entries left and not searched.
24	Memory address of key.
12	Reserved for I/O driver use.
12	Bit displacement from start of table entry to a 17-bit segment displacement field which is to be added to the base segment address in the descriptor pointed to by Link-M, if the Link-M branch is taken.
24	Link-M address which points to the I/O descriptor to be executed if a match is encountered and if the first bit in the 17-bit segment displacement field in the matched entry is a 0. The OC bit in the RS field for this descriptor will be preset to "1" and must be ignored.

RESULT DESCRIPTOR

The end of a disk pack operation occurs when either the DPC or the DPEC terminates. The DPEC will terminate by dropping the Ready line. The DPC will terminate by dropping the Select line. Whichever device terminates, the other device will also terminate by dropping the applicable line. At termination, the DPEC places the 16-bit DPEC result descriptor on the information lines between the DPEC and the DPC and also generates a clock pulse. The 16-bit DPEC Result descriptor is listed in table 1-1.

Table 1-1. DPEC Result Descriptor

Information Line	Result Descriptor
0	Read data error (Fire Code error).
1	Write-lockout.
2	Seek status flip-flop.
3	Drive not ready (Positioner not settled).
4	Drive off-line.
5	Drive unsafe.
6	Address parity or sync-code error.
7	Sector address error.
8	Seek timeout.
9	Drive not present.
10	Not used.
11	Not used.
12	Not used.
13	Not used.
14	Transmission parity error.
15	Try Diagnostic routine.

The DPEC result descriptor is used by the DPC to produce a 24-bit result descriptor that is stored in the RS field at the completion of an operation.

The bit structure and usage of the 24-bit result descriptor used by the B 1700 processor are listed in tables 1-2 and 1-3.

Table 1-2. DPC 24-Bit Result Descriptor

Bit Position	Usage
0	Operation completed.
1	Exception condition (3 thru 7 or 9 thru 16 set except 8-9-10 on Test).
2	Not Ready
3	Read Data error (Read-Search) or Busy (test).
4	Try Diagnostics (all operators).
5	Memory parity error (write-initialize-relocate) set by software.
6	Write lockout (Write-Initialize-Relocate-Test).
7	Slip occurred (Read, Write, Search).
7,8,9	Unit ID (Test). The following bit configurations can be used: 000: Not present. 001: 60 sector - 203 cylinder disk pack device (215 - type disk drive). 010: 60 sector - 406 cylinder disk pack device (225 - type disk drive).
9	Address parity or sync code error (Read-Write-Search).
10	Sector address error (Read-Write-Search-Relocate).
11	Timeout (Read-Write-Search-Initialize-Relocate).
10,11	Configuration (Test). 00: No exchange (all other combinations are invalid).
12	Seeking (Test).
13	Reserved.
14	Seek status flip-flop set (Test) or Exception (Search).
15	Transmission parity error (all operators).
16	Operation completed.

Table 1-2. DPC 24-Bit Result Descriptor (Cont)

Bit Position	Usage
17,23	ID = 0011\1110 (Test).
22	Special flag (all operations except test if bit number 4 is set).
23	Special flag (all operations except test if bit number 4 is set and on Read E = 1).

DISK PACK ELECTRONIC CONTROLLER

The DPEC consists of 19 logic cards (B 3700 size) mounted in an independent cabinet. The cabinet also contains two off-line maintenance cards with switches and indicators, a self-contained power supply, and a power panel with OFF/ON and LOCAL/REMOTE switches.

The DPEC performs the following functions:

a. Converts the 16-bit parallel data from the DPC into serial data to the disk drive(s).

b. Converts the serial data from the disk drive(s) into 16-bit parallel data to the DPC.

c. Provides op code detection and implementation.

d. Provides decoding of the file address.

e. Generates a 16-bit result descriptor for each operation.

f. Provides format compatibility between the DPC and the disk drive(s).

g. Generates bus and tag bit information for the disk drive(s).

h. Provides read and write control for the disk drive(s).

i. Provides relocation of data to spare disk drive sectors.

j. Detects errors and generates error code.

k. Provides off-line maintenance capabilities.

l. Supplies ac power to the disk drives.

DPEC OPERATION (OP) CODES

The op code is sent from the DPC to the DPEC in two 16-bit transfers. The DPC initiates the procedure by setting the Select level true and placing the first 16-bit op word on the information lines. The DPEC responds to Select being true by accepting the first op word, generating a clock pulse, and setting the Ready level true. These actions provide the gating to the DPC so that the second 16-bit op word is placed on the information lines. The DPEC accepts the second op word, generates another clock pulse and sets Busy true. The two 16-bit op words are listed in table 1-4. The bit configurations of these op words are listed in table 1-5.

Table 1-3. Disk Pack Control Result Descriptor

	Bit	I/O Exchange Position	Test OP	Description Read	Write
	1	7	OP Complete	OP Complete	OP Complete
S	2	6	Exception Condition	Exception Condition	Exception Condition
T	3	5	Disk Pack Not Operational	Disk Pack Not Operational	Disk Pack Not Operational
C	4	4	Exchange Busy	Fire Code Error	Reserved
	5	3	Reserved	Reserved	Reserved
2	6	2	Reserved	~~Reserved~~	~~Reserved~~
1	7	1	Write Lockout	Reserved	Write Lockout
	8	0	~~Reserved~~	~~Slip Occurred~~	~~Slip Occurred~~
	9	7	Bit 9 Bit 10 (Disk ID)	Reserved	Reserved
S	10	6		Address Parity Error or Sync Code Error	Address Parity Error or Sync Code Error
T					
C	11	5	Bit 11 Bit 12		
			0 | 0 | No exch		
2					
2	12	4		Seek Timeout	Seek Timeout
	13	3	Seeking	Seeking	Seeking
	14	2	Reserved	Reserved	Reserved
	15	1	Seek Complete	Seek Complete	Seek Complete
	16	0	Tx Parity Error	Tx Parity Error	Tx Parity Error
	17	7	OP Complete	OP Complete (If E = 1, will = 0)	OP Complete
S	18	6	ID = 0	Reserved	Reserved
T	19	5	ID = 0	Reserved	Reserved
C	20	4	ID = 1	Reserved	Reserved
	21	3	ID = 1	Reserved	Reserved
2	22	2	ID = 1	Reserved	Reserved
3	23	1	ID = 1	Reserved	Reserved
	24	0	ID = 0	If E variant is on, will = 1	Reserved

Table 1-4. DPEC OP Words

Information Lines	First OP Word	Second OP Word
Info 0	OP1	File address bit 6
Info 1	OP2	File address bit 7
Info 2	OP3	File address bit 8
Info 3	V	File address bit 9
Info 4	U1 (Unit select bit 1)	File address bit 10
Info 5	U2 (Unit select bit 2)	File address bit 11
Info 6	U4 (Unit select bit 4)	File address bit 12
Info 7	U8 (Unit select bit 8)	File address bit 13
Info 8	N1	File address bit 14
Info 9	N2	File address bit 15
Info 10	N3	File address bit 16
Info 11	File address bit 1	File address bit 17
Info 12	File address bit 2	File address bit 18
Info 13	File address bit 3	File address bit 19
Info 14	File address bit 4	Spare
Info 15	File address bit 5	Spare

Table 1-5. Bit Configuration of DPEC OP Words

Operation	OP1	OP2	OP3	V	N1	N2	N3
Read	0	0	0	V	-	D	-
Read Absolute	0	0	1	V	-	-	-
Write	0	1	0	V	-	D	-
Initialize	0	1	1	-	-	S	P
*Relocate	1	0	0	V	n	n	n
*Relocate	1	0	1	V	n	n	n
Verify	1	1	0	V	n	n	n
Test	1	1	1	-	-	C	W

Legend:

V = 0	Enables automatic restore.
V = 1	Disables automatic restore.
n = (1-5)	Spare sector number.
C = 1	Clears seek-status-flip-flops.
D = 1	Diagnostics testing (not used at present).
P = 0	Single track only.
P = 1	Full pack.
W = 1	Remote power down.
S = 0	Uses DPEC data.
S = 1	Uses DPC data.

*Relocate 1 uses DPC data.
*Relocate 2 uses address for data.

DPEC FUNCTIONAL COMPONENTS

The functional components of the DPEC are as follows:

a. Run counter.

b. Sequencer counter.

c. Word counter.

d. Other counter.

e. 54 adder.

f. Scratch pad.

g. Address decoder.

h. Address counter.

i. Serial-to-Parallel Shift (SPS).

j. Error encode.

Run Counter

The primary function of the run counter is to clock the sequence counter. The run counter steps from R0 through R15 and is clocked by the 5-MHz clock.

Sequencer Counter

The sequencer counter steps from S0 through S10, incrementing one step for every cycle of the run counter. The basic function performed at each sequencer count is as follows:

Count	Function
S0	This sequencer count is used to transfer the first and second op words into the DPEC. When the second op word has been transferred, the sequencer counter steps to S1.
S1	During this sequencer count, the DPEC performs the following checks: a. Is the selected disk drive settled? b. Did a transmission parity error occur? c. If the op was a write, is the drive write enabled?
S2	If any error conditions have occurred during this sequencer count, the DPEC will terminate the operation by setting the Ready line false.
S3	During this sequencer count the following checks are made: a. Is the Seek Status flip-flop set? b. Does the old address equal the new address? If the conditions are correct, the DPEC will initiate a Seek start to the bus and tag generator.

Count	Function
S4 and S5	No major functions in these two sequencer counts.
S6	During this sequencer count the DPEC checks for a test op. If the op is a Test, the DPEC terminates.
S7	During this sequencer count the DPEC checks for a Test op with the N3 bit set. If these conditions are met, the selected disk drive is powered off.
S8 and S9	No major functions are performed in these two sequencer counts.
S10	During this sequencer count the received op is performed.

Word Counter

The word counter is used to synchronize the DPEC with the data on the disk drive.

Other Counter

The Other counter is used to keep track of the sector location or the disk drive. The Other counter is cleared by the index pulse and upcounted by sector pulses.

54 Adder

The 54 Adder is used by the Relocate operators when reading or writing of a relocated sector is performed.

Scratchpad

The Scratchpad is used to store the file address of each operation.

Address Decoder

The Address Decoder is used to decode the file address sent from the DPC.

Address Counter

The Address counter is used to store the decoded file address and to up-count the decoded address for serial operations.

Switch-to-Parallel Shift (S.P.S.)

The S.P.S. register is used to convert parallel data from the DPC into serial data to the disk drive. This register is also used to convert serial data from the disk drive into parallel data to the DPC.

Error Encode

The Error Encode components generate the 32-bit Fire Code (a cyclic redundancy-checking circuit) on a write operation and checks the Fire Code on a read operation.

DISK PACKS AND DISK DRIVES

The disk drive unit (figure 1-12) provides random storage capabilities for the B 1700 System by replaceable disk packs. Each disk drive unit provides a drive assembly (spindle) for either one or two disk packs. The maximum configuration for the B 1700 system consists of four disk drive units, each containing two spindles to provide eight disks drives. The B 1700 maximum disk pack subsystem configuration is shown in figure 1-13.

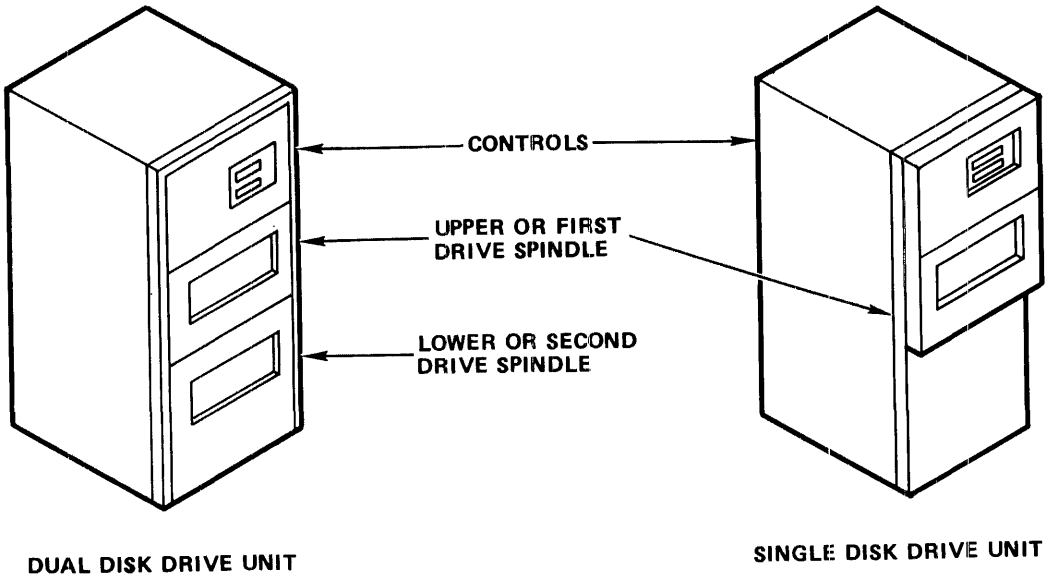


Figure 1-12. B 9486 Disk Pack Drive Unit

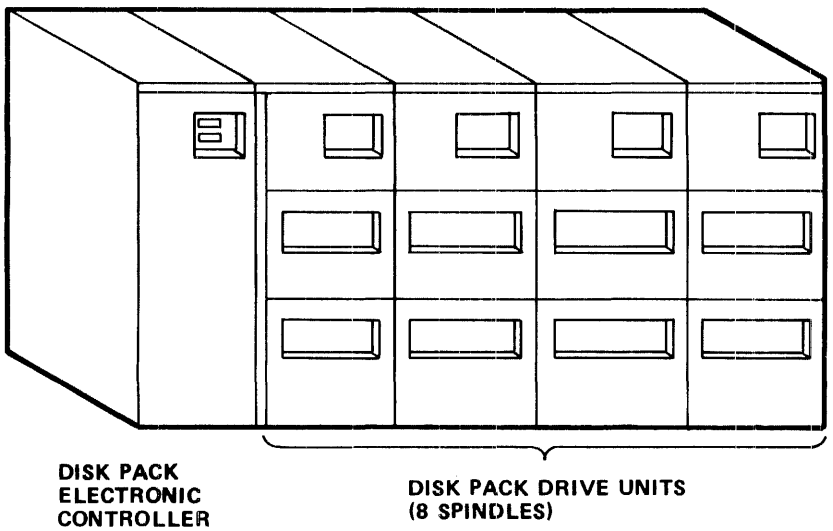


Figure 1-13. Maximum B 1700 Disk Pack Subsystem

DISK DRIVE PARAMETERS

There are two types of disk pack drives as follows: B 9486-2 and B 9486-4.

The basic parameters for each of these drives are listed in table 1-6.

Table 1-6. Disk Drive Parameters

Parameter	B 9486-2	B 9486-4
Number of spindles per drive	1 or 2	1 or 2
Number of cylinders	203	406
Number of heads	20	20
Number of sectors per track	*60	*60
Rotation time	25 ms	25 ms
Average seek time	30 ms	30 ms
Average access time	42.5 ms	42.5 ms
Number of 8-bit bytes per disk pack	43,665,300	87,330,600
*On track 0, only 55 sectors are usable; the other five sectors are reserved for relocating defective sectors.		

NOTE

Both types of disk pack drives must use only a B 9974-4 type Disk Pack. This disk pack is identical to a 225-type disk pack and provides a maximum of 406 cylinders and a recording density of 4400 BPI.

DISK DRIVE CONTROL SWITCHES

The control switches and indicators for each spindle in a disk drive unit are located in a recessed chamber at the top right-hand side of the disk drive unit.

These switches and indicators are shown in figure 1-14 and listed as follows:

a. Read/Write Protect Enable switch.

b. Write Enable Status indicator.

c. Select Lock indicator.

d. Drive Status indicator.

e. Drive ON/OFF switch.

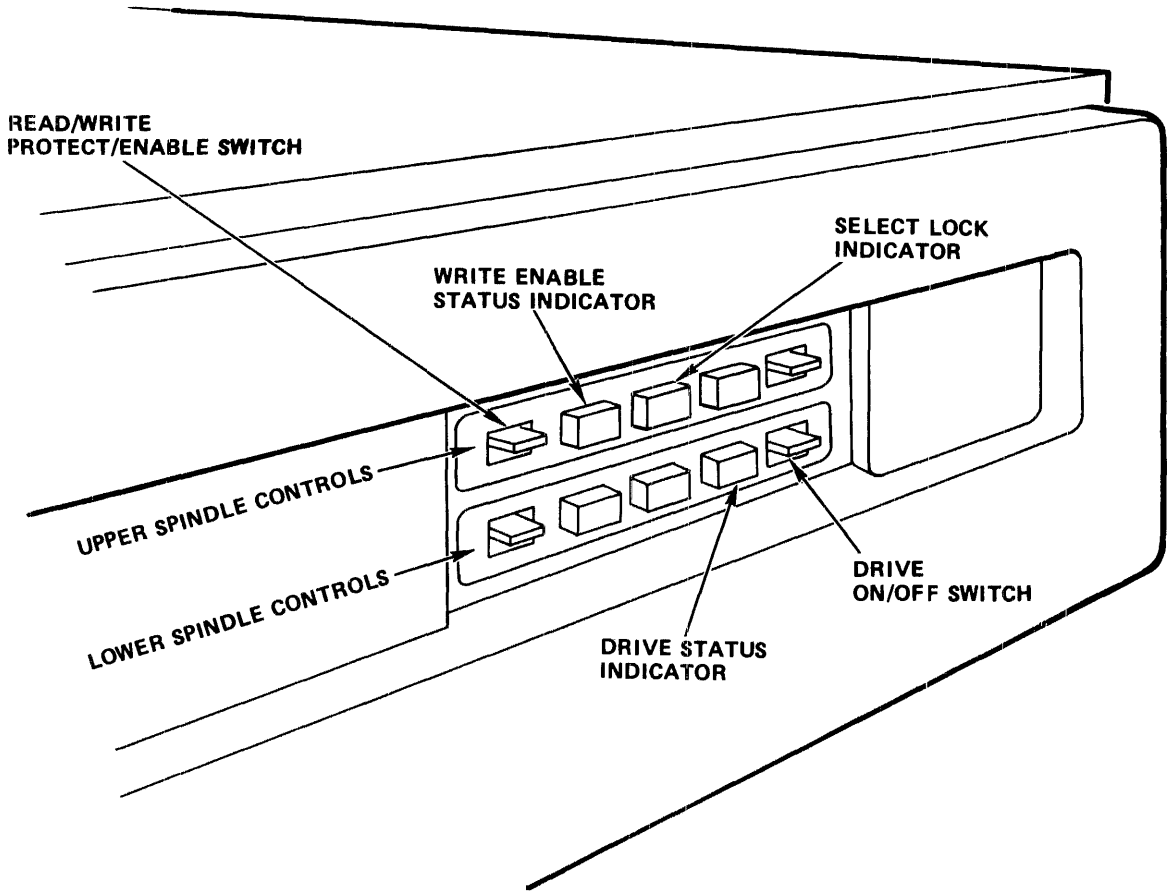


Figure 1-14. Disk Drive Control Switches

Read/Write Protect Enable Switch (R/W-PRT)

This yellow switch is a momentary action toggle switch, labelled "R/W" above and "PRT" below. When the disk drive is started, the drive electronics must be initially in the Protect (PRT) position, which inhibits any write operation. Actuating the switch momentarily downward (return to horizontal is automatic) will place the disk drive electronics in a Write Enable state only if the Select Lock indicator for that disk drive is OFF. The Module Select line from the controller must not be true; otherwise, the switch will not effect a change of state of the drive electronics. Repeated actuation of the switch downward places the disk drive electronics alternately in the Protect and Enable states only when the Module Select line is false.

Write Enable Status Indicator (WRITE ENABLE)

The WRITE ENABLE (yellow) indicator is illuminated when the disk drive is in the WRITE ENABLE state, allowing data to be written on the disk pack.

Select Lock Indicator (SELECT-LOCK)

The SELECT LOCK (red) indicator, labeled "SELECT LOCK," is illuminated if any of the fault conditions, monitored by the disk drive safety circuits is detected. The Select Lock state can only be cleared by stopping and restarting the disk drive.

The fault conditions which are checked by the safety circuits include the following:

a. Any dc power supply output low.

b. A head is not selected in response to Select Head signal.

c. More than one head is selected.

d. A head is selected without a Select Head signal.

e. The disk drive is not ready for operation when the write or erase gate is true.

f. The read gate is true simultaneously with the write or erase gates true.

g. The erase current is on for more than 60 $\pm$12 microseconds after the write current goes off.

h. The erase current is off and the write current is on.

i. The erase gate is true and the erase current is off.

j. The erase gate is false and the erase current is on.

k. The write gate is true and the write current is off.

l. The write gate is false and the write current is on.

m. The seek is unsafe because the heads are extended and the disk is not up to speed; a seek error occurred during Restore, or forward motion of the drive following a power ON.

n. An air filter system fault sensed.

In addition to the previous error conditions listed, the disk drive unit automatically retracts the heads if any of the following conditions occur while the heads are extended:

a. AC power failure.

b. Turning of spindle power.

c. Air system fault.

d. Low spindle speed.

e. Opening front drawer.

f. Remote power-down.

g. DC voltage failure.

Drive Status Indicator

The Drive Status (green) indicator is illuminated when the spindle is ready for operation and the heads have been initially positioned to cylinder 000. The Drive Status indicator will remain illuminated until the spindle braking has been completed when the spindle is powered down.

On-Off Switch (ON/OFF)

The ON-OFF (white) switch (figure 1-14) is a toggle switch labeled ON above and OFF below. When in the ON position, the switch starts the disk drive motor if the following conditions are met:

a. AC power switch is in the ON position (This switch is located on the power distribution assembly.)

b. AC power is applied from the controller.

c. A disk pack is installed.

d. The spindle drawer is closed.

e. Signal, dc, and ac cables are installed.

When the disk pack rotation is up to speed, the head actuator positions the read write heads on cylinder 000, and the ACCESS READY indicator turns on, indicating the drive is ready for operation.

When the switch is turned OFF, the heads are retracted and the motor comes to a complete stop in less than 30 seconds. To open the drawer for pack removal and replacement the motor must be completely stopped. This is indicated by the green indicator turning off.

With ac power applied from the controller and the ac switch in the ON position, the blower motor must be running and all dc supplies internal to the drive must be on. For normal operation the ac switch must be in the ON position and ac power must be controlled from the controller.

DISK PACK DESCRIPTION

General

A disk pack consists of an assembled stack of 11 iron-oxide-coated disk plates of approximately 14 inches in diameter, spaced approximately 0.40 inch apart, with protective disk plates mounted flush against the top and bottom surfaces. The pack includes the necessary parts to interface with a spindle in the bottom of a drive unit, a removable heavy duty top and bottom protective cover, and a changeable filter element located on the underside of the pack. A disk pack and its protective case are shown in figure 1-15. Figures 1-16 and 1-17 depict a fully disassembled disk pack and recording surfaces respectively.

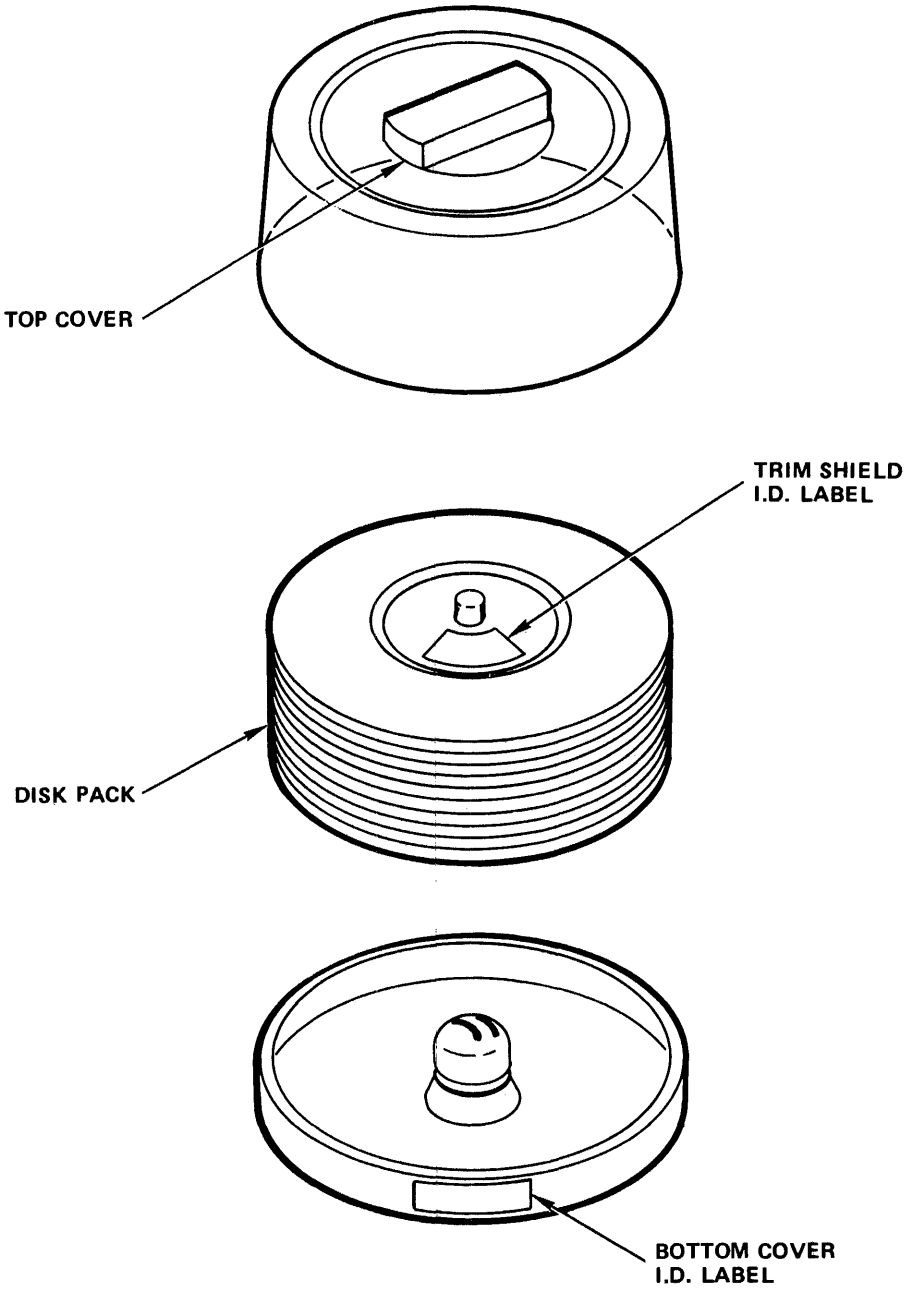


Figure 1-15. Disk Pack and Disk Pack Case

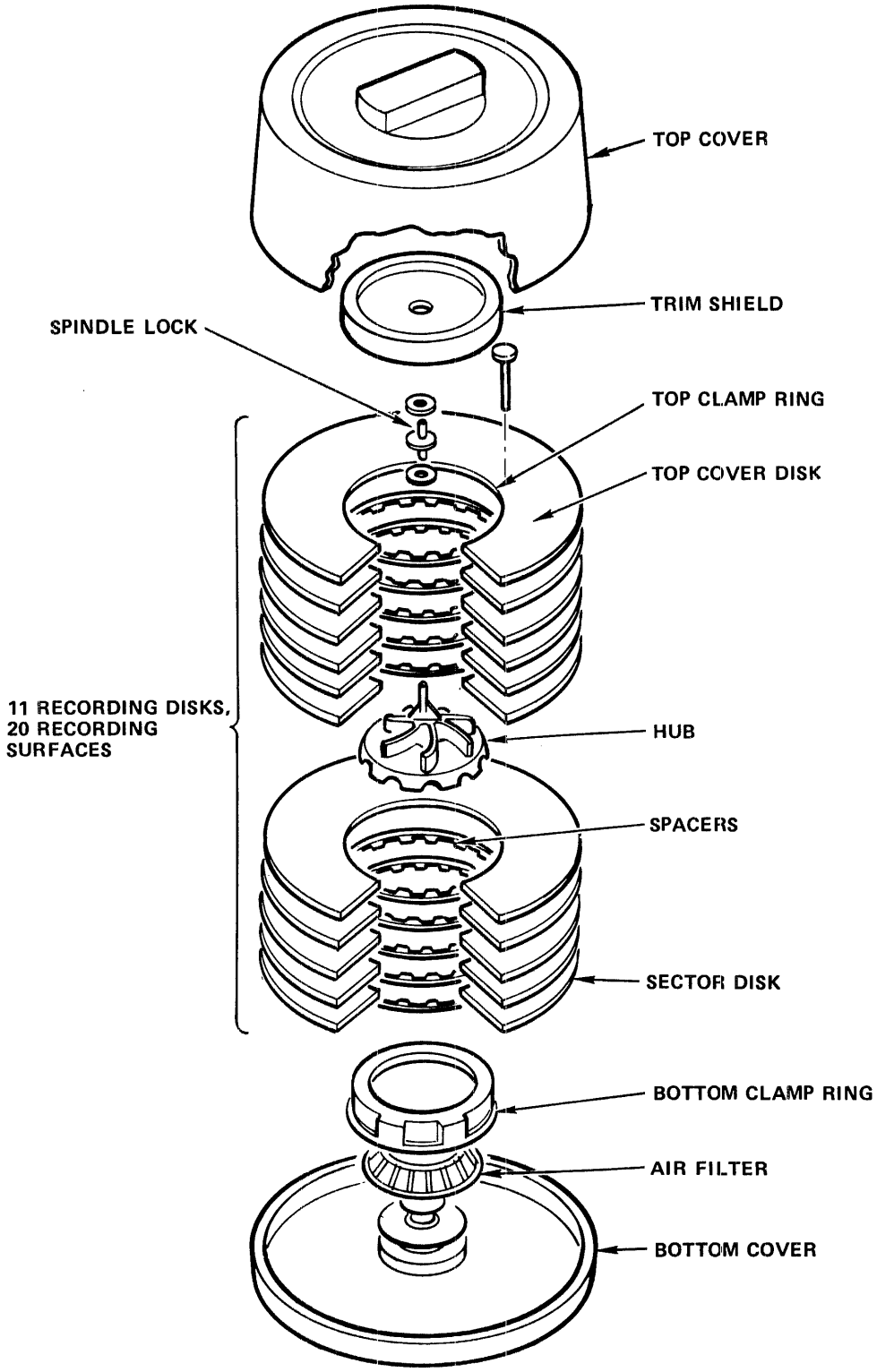


Figure 1-16. Disk Pack (Dissassembled)

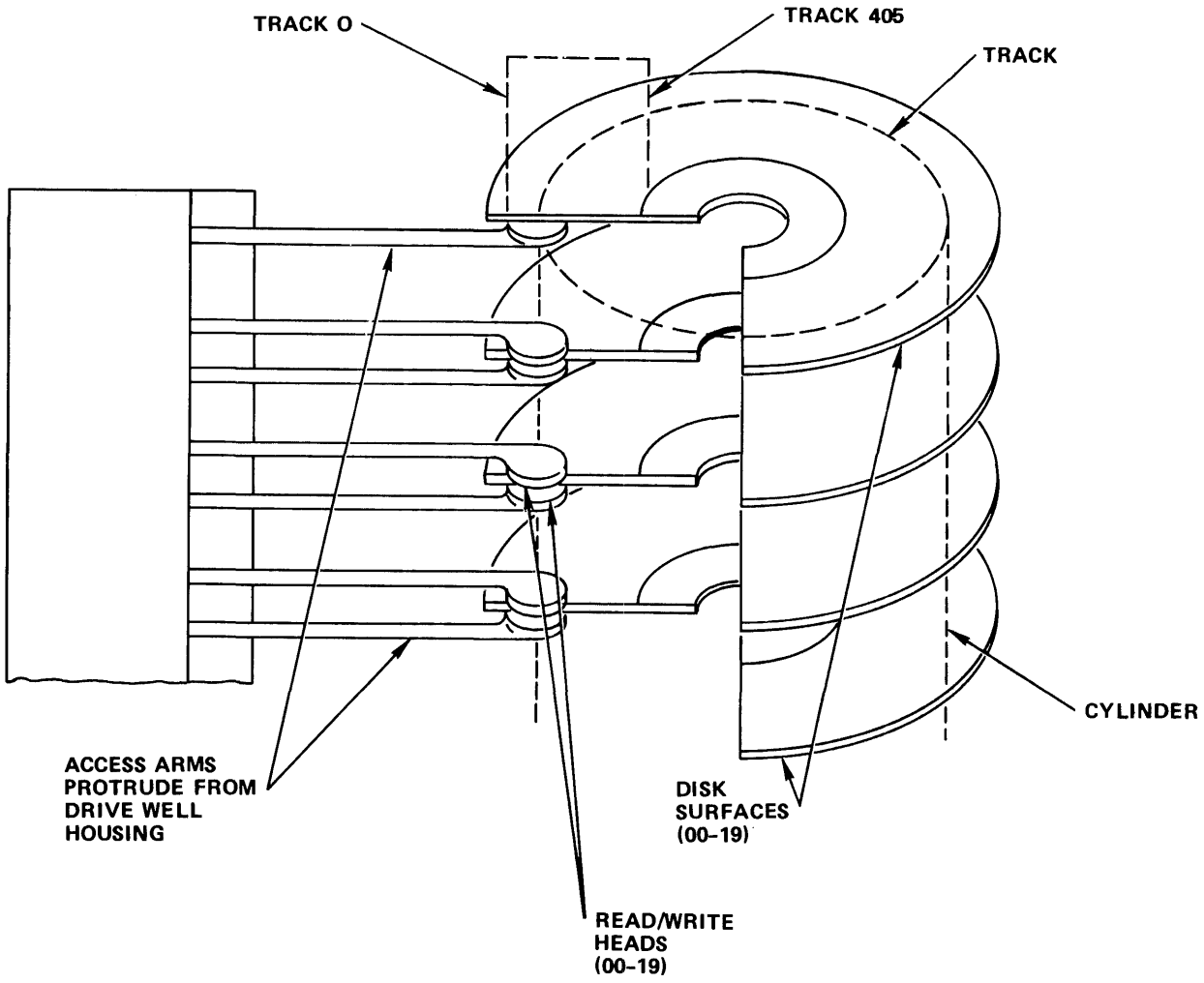


Figure 1-17. Disk Pack Read and Write Heads

Disk packs are manufactured with data recording tracks on each surface (see figure 1-17), similar to the track concept of the head-per-track disk file. There are 406 tracks on each surface, recorded at 200 tracks per inch. These are numbered, starting with the outside track, from 000 to 405. The disk pack drive unit has 10 access arms, each with two read/write heads, one pointing upward and the other downward. These heads are magnetically actuated to penetrate between the plates of a pack, to the correct track, prior to a read or write operation. This action is called a seek operation, and the time required to do it is called seek time. Minimum seek time is 10 milliseconds, maximum seek time is 59 milliseconds, and average seek time is 30 milliseconds.

Within the drive unit mechanism, all arms are mounted on a single arm mount block; therefore, all read/write heads always align over the same track number, on different disk surfaces. Because of this feature, all tracks of the same number, on different surfaces, are said to be in the same "cylinder." As with tracks, cylinders are numbered from 000 through 405.

All of the 11 recording disk plates have recording surfaces on both sides, except for the top and bottom ones. The top plate is encoded only on the under surface, and the bottom is encoded only on the upper side. The read/write heads are numbered from 00, which accesses the underside of the top disk plate through 19, which accesses the top of the bottom disk plate. (See figure 1-17.)

Since the packs rotate within a drive unit at 2400 revolutions per minute, the maximum time it takes for a given point on a track to come beneath a read/write head during this rotation is 25 milliseconds. On the average, this time will be 12.5 milliseconds. The term for this rotational wait time is called latency time. Latency is, therefore, the time it takes, after a head is positioned at the correct track, to physically commence the transfer of data to or from a disk pack.

Access time is the total time it takes from initiation of a pack I/O action until the transfer of data begins. (Seek time plus the latency time is equal to access time.)

Each track of each cylinder is divided into sixty, 180-byte segments. These segments are named "sectors" and are shown in figure 1-18.

DISK PACK ADDRESSING

Each sector on each track has an assigned address. Since there are 60 sectors on each track, addressing is sequential from track 0, sector 0 through track 405, sector 59, with one exception. The zero head of each cylinder reserves five sectors for relocation purposes. If a sector within a cylinder either is, or becomes, defective, a flag is written in the sector address, and the information and sector address are relocated to one of the five spare sectors allocated to that cylinder.

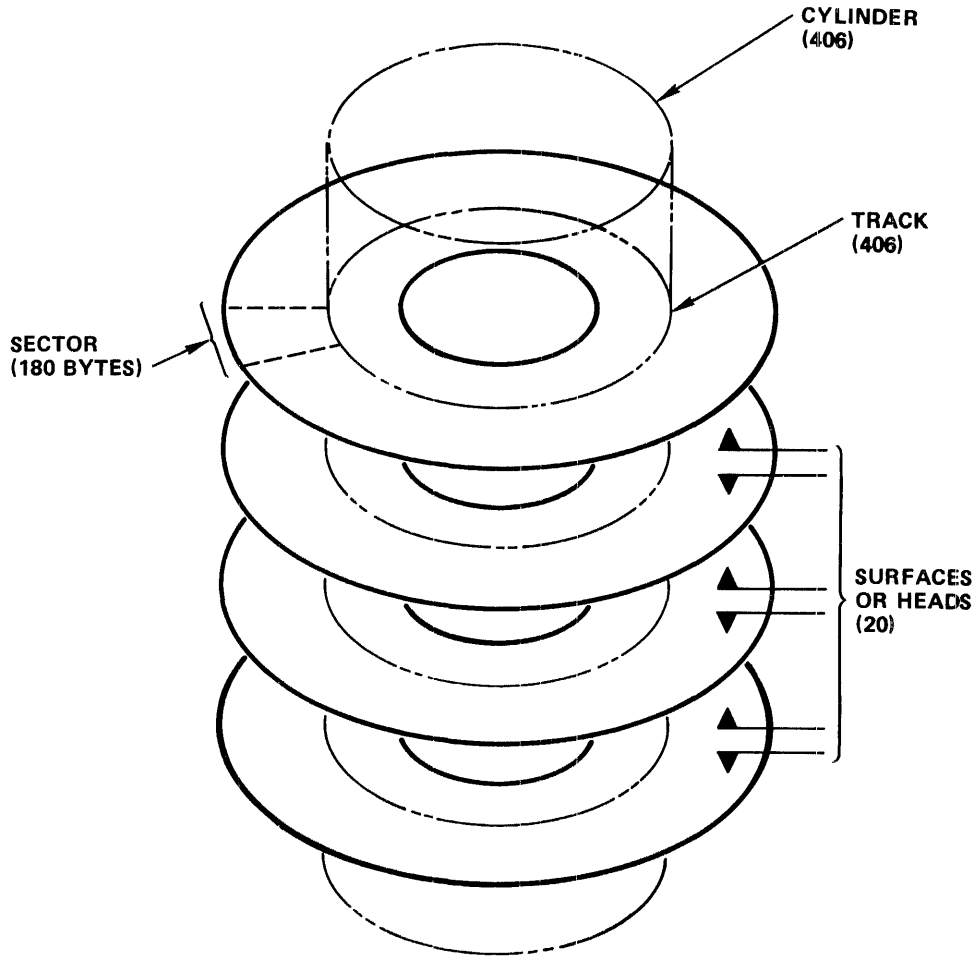


Figure 1-18. Disk Pack Structure

The first track of each cylinder, therefore, contains only 55 sequential sector addresses. Sector 000000 is located at head 0, track 0, and progresses through sector 0000054 on head 0, track 0. Sector address 000055 is located at head 1, track 0. Heads 1 through 19 on this cylinder have 60 sectors each, providing a total of 1195 sector address per cylinder. Since there are 406 cylinders this provides a total of 485,170 sector addresses, or a total of 87,330,600 eight-bit bytes. However, customer storage area is limited to 87,200,000 eight-bit bytes, the other 130,600 bytes being reserved for system software applications.

DISK PACK TRACK FORMAT

Each sector on the disk pack contains 260 byte locations, of which 180 bytes are used for data storage. The other 80 bytes are used primarily as delays for read-to-write or write-to-read switching. The bit allocation of a sector is listed in table 1-7.

Table 1-7. Disk Pack Sector Bit Allocation

Sequential Byte Positions	Usage
23	Sector address preamble.
3	Sector address.
9	Sector address postamble.
15	Data preamble.
184	Data plus check bits.
26	Data postamble.

In addition to the 260 byte positions, at the beginning of each track, 30 bytes are also reserved for the beginning-of-track gap that occurs immediately after the index pulse.

DISK PACK CONTROL TO DISK PACK ELECTRONIC CONTROLLER INTERFACE

The interface between the DPC and the DPEC (figure 1-19) consists of 16 information lines, one parity line and six control lines contained in a 25-coaxial conductor cable terminated on both ends with card-edge connectors.

INFORMATION LINES

The information lines consist of 16 bidirectional lines over which the op code, read and write data, and the DPEC result descriptor (16 bits) are passed between the DPC and the DPEC.

PARITY

The parity line consists of one bidirectional line that provides odd parity for the 16 information lines.

READY

The Ready control level is generated by the DPEC after receipt of the first op word. Ready will not go false unless the DPEC desires to terminate the operation or the DPC terminates. The Ready level going false informs the DPC that the DPEC is in the result descriptor phase. This implies that the result descriptor will be gated to the information lines.

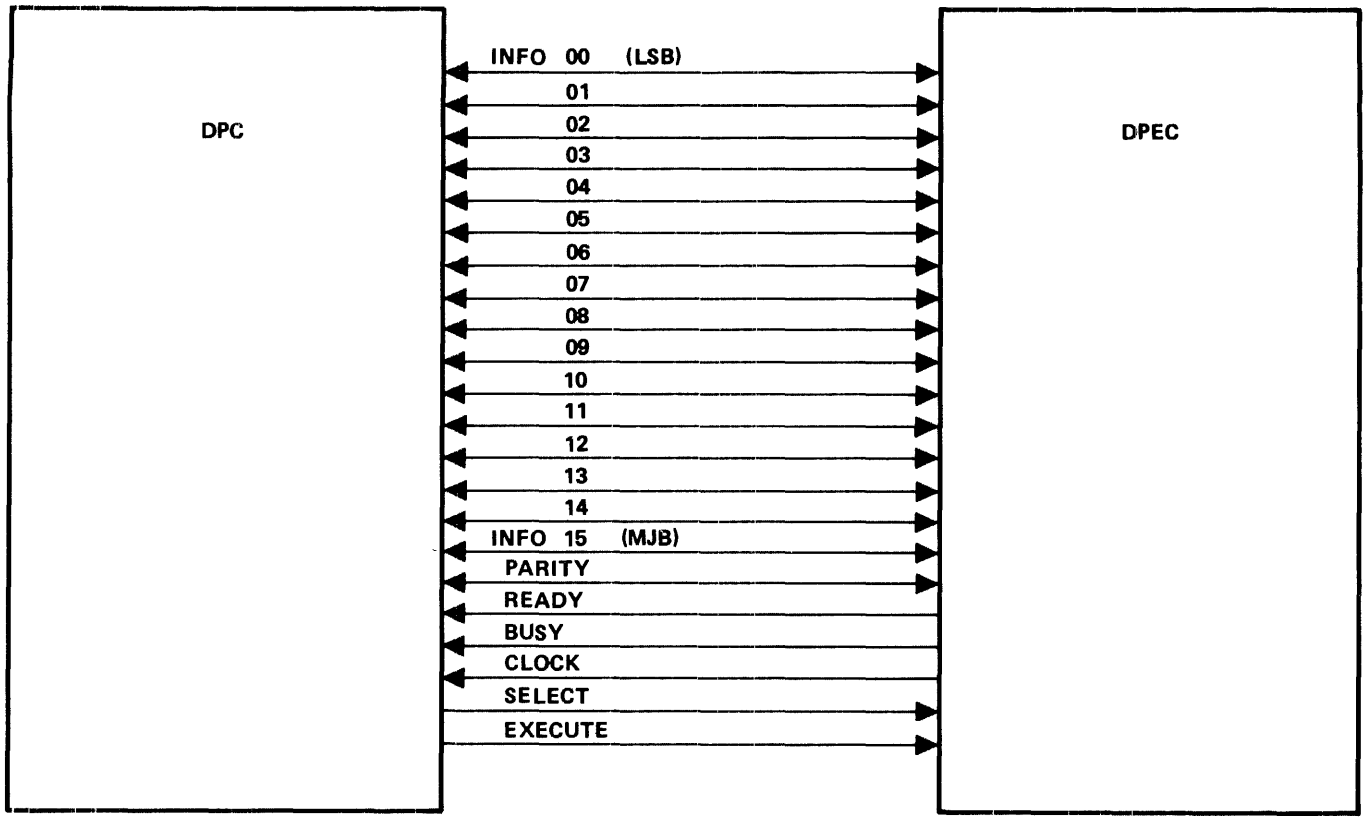


Figure 1-19. DPC-to-DPEC Interface Lines

BUSY

The Busy control level is generated by the DPEC after receipt of the second op word. This level indicates to the DPC that the DPEC is conditioned for the operation. This would normally be a transfer of data for either a read or write op. Busy level will remain true until the end of the operation (including the result descriptor phase).

SELECT

The Select control level is generated by the DPC. When this level is off, this line starts a new operation. The Select level going true with the Busy and Ready levels false indicates that the first word of the op code is on the information lines. The Select level will remain true until the DPC desires to terminate the operation. (This is the normal ending of an operation.) After the DPEC detects the fall of Select, it will continue to send or receive data until the entire 180 characters have been sent or received. At this time, the DPEC causes the Ready level to drop and places the result descriptor on the information lines.

EXECUTE

The Execute control level, generated by the DPC, informs the DPEC that the DPC is unable to send or receive any more data at the sector time. This would occur if all buffers were full in the control during a read op or if all buffers were empty during a write op. When the Execute level drops, this informs the DPEC to go into a Slip mode. Slip mode continues until the Execute level goes true again.

CLOCK

Clock is generated by the DPEC. Its purpose is to synchronize the 16 information lines. This clock is not free running. For example, during Idle or Slip mode, no clock pulses will be generated.

INTERFACE CONTROL LEVELS INTERACTION

Table 1-8 lists the interaction of the three control levels: Select, Busy and Execute.

Table 1-8. Select, Busy, and Execute Interaction

Control Lines	Function	Description
Select/ * Busy/ * Ready/	Idle	
Select * Busy/ * Execute	Initiate phase	Ready/ equals the DPEC receiving the first initiate word Ready equals the DPEC receiving second initiate word
Select * Busy * Ready* Execute	Data transfer phase	Execute/ = Slip Mode
Select/ * Busy * Ready/	Result status phase	
Select/ * Busy * Ready	Wait for result status phase	Operation terminated by Disk Pack Control (DPC)
Select/ * Busy/ * Ready	Sequence error	DPEC failure
Select * Busy * Ready/	Go to result status phase	Operation terminated by the DPEC

The operation begins with the interface in an Idle state defined as READY/*BUSY/*SELECT/. The DPC enables the Send line to begin the operation at the same time the first initiate word is placed on the information (0-15) lines. The first initiate word is:

Information Line Number	Function
INFO(0)	OP1 (op bit 1).
INFO(1)	OP2 (op bit 2).
INFO(2)	OP3 (op bit 3).
INFO(3)	V (variant bit).
INFO(4)	U1 (unit bit 1).
INFO(5)	U2 (unit bit 2).
INFO(6)	U4 (unit bit 3).
INFO(7)	U8 (unit bit 4, for future expansion).
INFO(8)	N1 (spare sector bit 1).
INFO(9)	N2 (spare sector bit 2).
INFO(10)	N3 (spare sector bit 3).'

Information Line Number	Function
INFO(11)	B1 (file address bit 1).
INFO(12)	B2 (file address bit 2).
INFO(13)	B3 (file address bit 3).
INFO(14)	B4 (file address bit 4).
INFO(15)	B5 (file address bit 5).

Within 166-500 nanoseconds after bringing up the Send line, the DPC brings up the Select line. The interface lines now are SELECT*BUSY/*READY/. This logic indicates that the first initiate word is on the information lines to the DPEC. When the DPEC has accepted the first initiate word, a clock pulse is sent to the DPC. The leading edge of the clock indicates the word has been accepted and causes the DPEC to enable the Ready line. (The leading edge of the clock must be received by the DPC before the Ready line changes.) Within 500 nanoseconds after the falling edge of the clock, assuming Ready is on, the second initiate word will be put on the information lines. The second initiate word contains the rest of the file address bits as follows:

Information Line Number	Function
INFO(0)	B6 (file address bit 6).
INFO(1)	B7 (file address bit 7).
INFO(2)	B8 (file address bit 8).
INFO(3)	B9 (file address bit 9).
INFO(4)	B10 (file address bit 10).
INFO(5)	B11 (file address bit 11).
INFO(6)	B12 (file address bit 12).
INFO(7)	B13 (file address bit 13).
INFO(8)	B14 (file address bit 14).
INFO(9)	B16 (file address bit 15).
INFO(10)	B17 (file address bit 16).
INFO(11)	B18 (file address bit 17).
INFO(12)	B19 *file address bit 18).
INFO(13)	B20 (file address bit 19).
INFO(14)	Spare.
INFO(15)	Spare.

The leading edge of the clock indicates that the second initiate word has been accepted. This causes the Busy line from the DPEC to come true. This action places the disk pack subsystem in the data mode defined as SELECT*BUSY*READY.

If the operation is a Read, the DPC will now drop the Send line and wait for the first data entry. If the operation is a write, the DPC will put the first two bytes of data on the lines. If the operation cannot be performed, that is, a seek is required, the unit is still seeking, etc., the DPEC drops the Ready line. The DPC will drop the Select line within 1 millisecond (and the Send line if it is still on) and wait for the DPEC result descriptor. The interface is now in the result state of SELECT/*READY/*BUSY. The clock indicates the result word is on the lines. It is stable for the entire clock period. Sometime after the leading edge of the clock, the Busy level drops, and the subsystem is returned to the idle state. Sometime being defined as the indeterminate time that is dependent on the response time of the individual disk pack drive assembly.

If the operation can be performed after the Initiate phase, the Ready line stays on. Each clock indicates that data is on the information lines for a read operation or data has been accepted for a write operation. On a write operation, the data may change any time after the leading edge of the clock. On a read operation, the data must be stable for the entire clock width. If the DPEC wants to terminate for any reason (end of initialize, relocate,

read maintenance operation, or any error condition), it drops the Ready line. The DPC then drops the Select line and waits for the DPEC result descriptor. If the DPC wants to terminate the operation, it drops the Select line on or before the 90th data transfer for any sector. The DPEC finishes the transferring for that sector, drops Ready, and sends the DPEC result descriptor back to the I/O controls. If the Select line is still on after the 90th transfer, the DPEC will continue reading or writing into the next sector. There is only one result descriptor for each operation. During a read on the data transfer mode, the DPEC sends a result descriptor for each segment that is read.

DISK PACK ELECTRONICS CONTROLLER TO DISK PACK DRIVE INTERFACE

The interface between the DPEC and the DPD is two cables: a dc power cable and a logic signal cable.

The logic interface between the DPEC and the DPD is listed in table 1-9. The signal cable is located at J3U or J3L of the disk pack drive unit.

Table 1-9. DPEC-to-DPD Interface

Signal Pin Number	Ground Pin Number	Function/Name
1	2	Drive bus 1.
3	2	Drive bus 2.
4	5	Drive bus 3.
7	5	Drive bus 4.
8	10	Drive bus 5.
11	10	Drive bus 6.
12	13	Drive bus 7.
14	13	Drive bus 8.
15	16	Drive bus 0.
17	16	Set cylinder tag.
18	20	Set head tag.
21	20	Control tag.
22	23	Spare.
24	23	Spare.
52	53	Drive ready.
54	53	On-line.
55	56	Index.
57	56	Drive unsafe.
58	59	Seek incomplete.
60	59	End of cylinder.
62	63	Sector mark (reserved).
64	63	Write current sense.
67	66	Read only.
65 } Twisted Pair.		Heads extended.
76 }		Controlled ground.
77 } Twisted Pair.		Sequence pick.
78 }		+36 Volt sequence power.
79		Terminator, +5 volt.
40	41	+36V sequence pick out.
42	41	Spare.
43	44	Spare.
45	44	Spare.
46	47	Spare.
48	47	Spare.
49	50	Spare.
	80	Shield ground.
	82	Shield ground.

CYCLIC REDUNDANCY CHECKING (FIRE CODE)

A four-byte (32-bit) error code is generated and checked by the DPEC. This code is similar to the cyclic redundancy character code on magnetic tape. Upon detecting a fire code error, the DPEC sets a bit in the result descriptor. The MCP upon recognition of the error performs a read operation with the E-variant set. This variant directs the DPC to perform a read of the sector in error and to return to the processor the four bytes of fire code. (In normal operation the fire-code bytes are not sent to the processor.) The MCP manipulates the sector within S-memory and attempts to correct the data. Up to a five-bit drop can be corrected.

SECTION 2

FUNCTIONAL DESCRIPTION

INTRODUCTION

The B 1700 Disk Pack Control I (DPC) provides control and interface logic between the B 1700 Central Processor and the B 9480 series Disk Pack Electronics Controller/Disk Pack Drive units (DPEC/DPD). The interface between the DPC and the central processor consists of two 25-conductor ribbon cables. One of the ribbon cables is used for information (data) transfer. The other ribbon cable is used for control lines. The pin location and names for interface lines of these two cables are listed in tables 2-1 and 2-2.

The interface between the DPC and the DPEC consists of a 25-conductor coaxial cable containing 16 information lines, one parity line, and six control lines. These interface lines and their functions are shown in table 1-9.

The interface between the DPEC and a DPD consists of a dc power cable and a logic signal cable. The pin locations and names for the interface lines of the logic signal cable are listed in table 1-9.

Table 2-1. CP-to-DPC Control Interface Cable ($Y)

Pin Location	Line Name
Y$A	RC.....1 (Response Clear).
Y$B	CA.....1 (Channel Active).
Y$C	CLRB...1 (Clear Bus).
Y$D	SR.....1 (Service Request).
Y$E	PWRON..1 (Power On).
Y$I	1US...R1 (One-Microsecond Bus).
Y$J	4US...R1 (Four-Microsecond Bus).
Y$K	32US..R1 (Thirty-Two Microsecond Bus).
Y$L	1024USR1 (One-Thousand-and-Twenty-Four Microsecond Bus).
Y$H	8MHZ...1 (Eight-Megahertz Clock).

Table 2-2. CP-to-DPC Information Interface Cable ($X)

Pin Location	Line Name
X$A	EXCH00.1 (Exchange Information Line 00).
X$B	EXCH01.1 (Exchange Information Line 01).
X$C	EXCH02.1 (Exchange Information Line 02).
XSD	EXCH03.1 (Exchange Information Line 03).
X$E	EXCH04.1 (Exchange Information Line 04).
X$F	EXCH05.1 (Exchange Information Line 05).
X$G	EXCH06.1 (Exchange Information Line 06).
X$H	EXCH07.1 (Exchange Information Line 07).
X$I	EXCH08.1 (Exchange Information Line 08).
X$J	EXCH09.1 (Exchange Information Line 09).
X$K	EXCH10.1 (Exchange Information Line 10).
X$L	EXCH11.1 (Exchange Information Line 11).
X$M	EXCH12.1 (Exchange Information Line 12).
X$N	EXCH13.1 (Exchange Information Line 13).
X$P	EXCH14.1 (Exchange Information Line 14).
X$Q	EXCH15.1 (Exchange Information Line 15).
X$R	EXCH16.1 (Exchange Information Line 16).
X$S	EXCH17.1 (Exchange Information Line 17).
X$T	EXCH18.1 (Exchange Information Line 18).
X$U	EXCH19.1 (Exchange Information Line 19).
X$U	EXCH20.1 (Exchange Information Line 20).
X$W	EXCH21.1 (Exchange Information Line 21).
X$X	EXCH22.1 (Exchange Information Line 22).
X$Y	ESCH23.1 (Exchange Information Line 23).

DISK PACK CONTROL FUNCTIONS

The sequence of events that occur during the execution of a DPC I/O operator is determined by the following counters:

a. Status Counter.

b. Sequence Counter.

c. Read and Write Sequencers.

An overall flow block diagram for the DPC is shown in figure 2-1.

STATUS COUNTER

The status counter (STC00 through STC23) is primarily used to control the flow of data and information between the DPC and the central processor (I/O driver). The function of each status count is discussed below:

Status Count	Function/Description
STC00	Used only to increment the status counter to SC01.
STC01	Used to provide the following: a. Idle state of the DPC. b. The logic to transfer the first byte (eight bits) of the 24-bit operation (OP) code from the I/O driver to the DPC. c. The logic to check for completed Seek operations when the DPC is idle (STC01 *No-Operations-Requested). If a completed Seek is found (SEEKF set to 1), a service request flag is set to 1 (SRF←1). d. The logic to increment the status counter to STC02.
STC02	Used to transfer the second byte of the op code from the I/O driver to the DPC and increment the status counter to STC03.
STC03	Used to transfer the third byte of the op code from the I/O driver to DPC and increment the status counter to STC04.
STC04	Used to transfer the first byte of the file address from the I/O driver to the DPC and increment the status counter to STC05.
STC05	Used to transfer the second byte of the file address from the I/O driver to the DPC and increment the status counter to STC06.

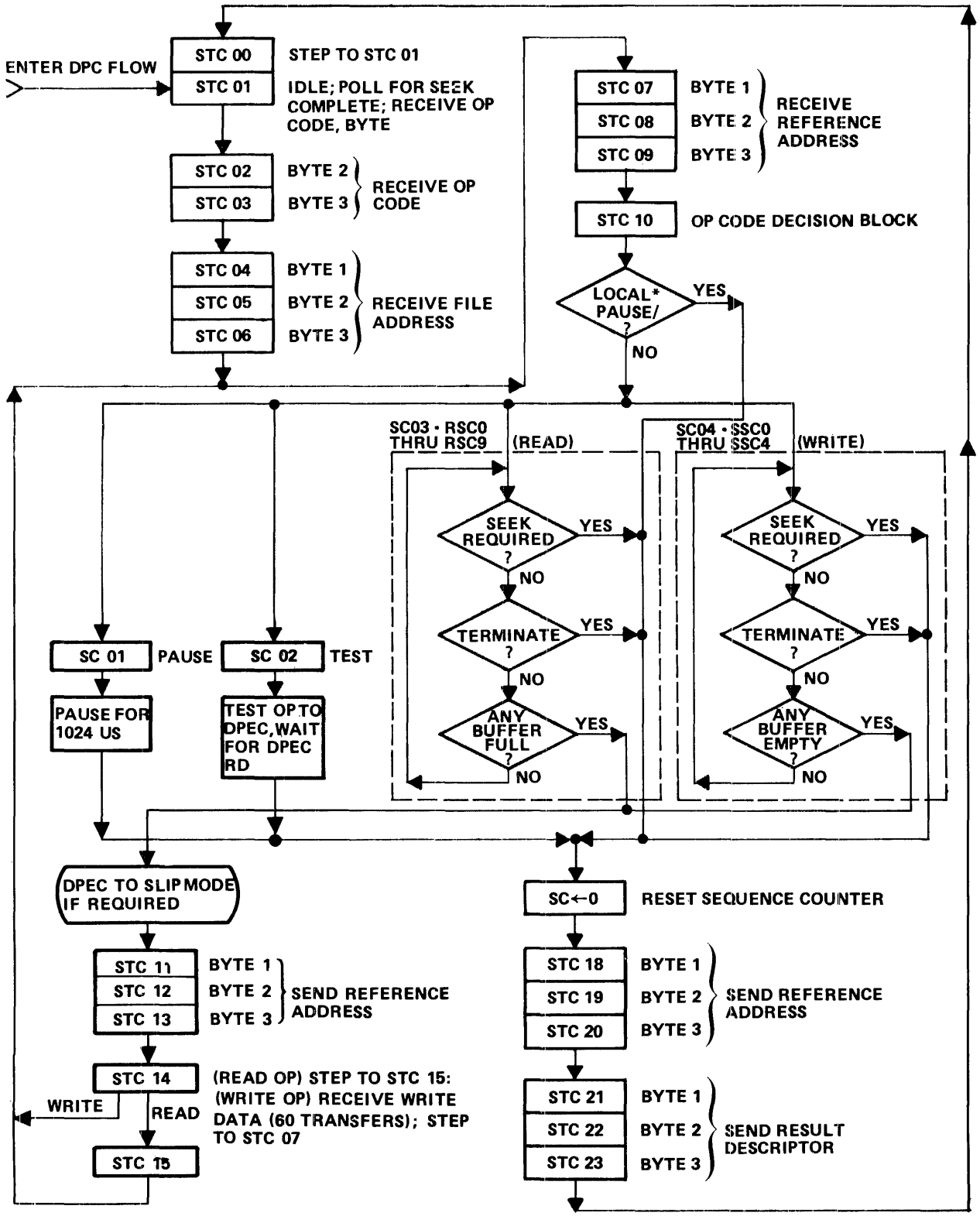


Figure 2-1. DPC Block Flow

Status Count	Function/Description
STC06	Used to transfer the third byte of the file address from the I/O driver to the DPC and increment the status counter to STC07.
STC07	Used to transfer the first byte of the reference address from the I/O driver to the DPC and increment the status counter to STC08. This status count also provides logic to set STC64F to 1, if the status counter is not in step with the I/O driver. The out-of-step condition will be indicated in the Test-Status phase of the I/O driver.
STC08	Used to transfer the second byte of the reference address from the I/O driver to the DPC and increment the status counter to STC09.
STC09	Used to transfer the third byte of the reference address from the I/O driver to the DPC and increment the status counter to STC10.
STC10	Used to initiate the sequence counter or respond to a not-ready DPEC as listed in the following conditions: a. If the operation requested is a pause, set the sequence counter to SC01. b. If the operation requested is not a pause and the DPEC LOCAL/REMOTE switch is in LOCAL, set the status counter to STC18. c. If the operation requested is a Test and the DPEC LOCAL/REMOTE switch is in REMOTE, set the sequence counter to SC02. d. If the operation requested is a read and the DPEC LOCAL/REMOTE switch is in REMOTE, set the sequence counter to SC03. e. If the operation requested is a write and the DPEC LOCAL/REMOTE switch is in LOCAL, set the sequence counter to SC04.
STC11	Used to transfer the first byte of the reference address from the DPC to the I/O driver and increment the status counter to STC12.
STC12	Used to transfer the second byte of the reference address from the DPC to the I/O driver and increment the status counter to STC13.
STC13	Used to transfer the third byte of the reference address from the DPC to the I/O driver and increment the status counter to STC14.

Status Count	Function/Description
STC14	Used to provide 60 transfers of write data from the I/O driver into a write buffer. When the write buffer is full, or if a terminate signal is received, the status counter is set to STC07. During a read operation, status count STC14 is used only to increment the status counter to STC15.
STC15	Used to transfer read data from a read buffer into the I/O driver. The number of read data characters is dependent on the M and E variants of the read operator.
STC16 & STC17	Not used for the DPC flow.
STC18	Used to transfer the first byte of the reference address from the DPC to the I/O driver and increment the status counter to STC19.
STC19	Used to transfer the second byte of the reference address from the DPC to the I/O driver and increment the status counter to STC20.
STC20	Used to transfer the third byte of the reference address from the DPC to the I/O driver and increment the status counter to STC21.
STC21	Used to transfer the first byte of the result descriptor from the DPC to the I/O driver and increment the status counter to STC22.
STC22	Used to transfer the second byte of the result descriptor from the DPC to the I/O driver and increment the status counter to STC23.
STC23	Used to transfer the third byte of the result descriptor from the DPC to the I/O driver and set the status counter to STC00 (CLRCHAN).

SEQUENCE COUNTER

The Sequence Counter (SC00 through SC04) is used to provide the necessary logic for the flow of information and data between the DPC and the DPEC. The function of each of the sequence counts is described below:

Sequence Count	Function
SC00	Used as the Idle state for the sequence counter.
SC01	Provides a microsecond delay for a Pause operation. At the end of this delay the sequence counter is set to SC00 and the status counter is set to STC18.

Sequence Count	Function
SC02	The Test operator is transferred from the DCP to the DPEC. When the Test operator result descriptor is received from the DPEC, the sequence counter is set to SC00 and the status counter is set to STC18.
SC03	Used for a read operation. The operations that occur during SC03 are described in the following paragraphs:

a. The first time that the DPC is at STC10*SC03 for any read operation, the op code and file address are transferred from the DPC to the DPEC.

b. If a seek operation is required, the DPEC goes to the result status phase. The result status phase consists of the following DPEC logic: (SELECT*BUSY*READY/). The DPEC then transfers a 2-byte result descriptor to the DPC. Upon receipt of the DPEC result descriptor, the DPC sets the status counter to STC18 and the sequence counter to SC00.

c. The first time that the DPC is at STC10*SC03 for a read operation and the seek operation is completed, the op code and file address are transferred from the DPC to the DPEC. The DPC then waits for read data to be transferred from the DPD through the DPEC to the read buffers.

d. If any read buffer becomes full while the DPC is at STC10*SC03, the status counter is incremented to STC11. In addition, a service request flag is set (SRF←1) indicating to the I/O driver that a buffer full of read data is available for transfer to the I/O driver. The status count, however, remains at SC03 to provide read gating between the DPEC and the DPC.

e. Read data is transferred from the DPEC in two-byte (16-bit) increments. Read data, however, must be stored in the read buffers in 3-byte (24-bit) increments. The read data conversion and shifting from the DPEC to the DPC is controlled by the read sequencer (RSC0 through RSC9).

Sequence Count	Function
	f. When a terminate signal is received in the DPC, it sets the terminate flip-flop (TERMF). The terminate flip-flop is used to notify the DPEC to go into the result status phase by setting the SELECT signal FALSE. During the result status phase, the DPEC transfers a two-byte result descriptor to the DPC. Upon receipt of the DPEC result descriptor, the DPC sets the status counter to STC18 and the sequence counter to SC00. The terminate signal is normally used to end a read operation.
	g. During SC03, if all three read buffers are full, the DPEC goes into Slip mode of operation.
SC04	Used for a write operation. The operations that occur during SC04 are described below:
	a. The first time that the DPC is at STC10*SC04 for any write operation, the op code and file address are transferred from the DPC to the DPEC (Initiate word 1 and initiate word 2). When initiate word 2 is transferred from the DPC to the DPEC, a 64-microsecond timer (TIMERF) is set.
	b. If a seek operation is required, the DPEC goes to the result status phase. The DPEC then transfers a two-byte result descriptor to the DPC. Upon receipt of the two-byte DPEC result descriptor, the DPC does the following: sets the Status counter to STC18, sets the sequence counter to SC00, resets TIMERF, and sets the request service flip-flop to 1.
	c. The first time that the DPC is at STC10*SC04 for a write operation and the seek operation is complete, the operation code and file address are transferred from the DPC to the DPEC. When the last 14 bits of the file address are transferred from the DPC to the DPEC, the 64-microsecond timer (TIMERF) is set. When TIMERF times out, the status counter is incremented to STC11. However, the sequence counter remains at SC04 to provide write gating between the DPC and the DPEC.
	d. The write buffers are filled with write data during STC14. The first time that any write buffer is filled with write data, write gating is enabled. The write data is transferred from the write buffers through the DPEC to the selected DPD.

Sequence Count	Function
	e. Write data is transferred from the write buffers in three-byte increments. Write data to the DPEC, however, must be provided in two-byte increments. The write data shifting and converting from three-byte to two-byte increments is provided by the write sequencer (SSC0 through SSC4).
	f. If any write buffer is empty while the DPC is at STC10*SC04, the status counter will be incremented to STC11. However, the sequence counter remains at SC04 to provide write gating between the DPC and the DPEC.
	g. When a terminate signal is received in the DPC, it sets the terminate flip-flop (TERMF). The terminate flip-flop is used to notify the DPEC to go into the result status phase. During the result status phase, the DPEC transfers a 2-byte result descriptor to the DPEC. Upon receipt of the DPEC result descriptor, the DPC sets the status counter to STC18 and the sequence counter to SC00. The terminate signal is normally used to end a write operation.
	h. During SC04, if all of the write buffers are empty, the DPEC goes into Slip mode of operation.

READ SEQUENCER

The read sequencer consists of a counter, gated to count from 0 to 9 (RSC0 through RSC9) and four read gates (RG1 through RG4). The counter and gates are used to provide read data shift control between the DPEC and the read buffers in the DPC. Information from the DPEC is transferred in 16-bit (two-byte) increments. Information is stored in the read buffer in 24-bit (three-byte) increments. The read sequencer also provides synchronization between the asynchronous read data from the DPEC and the B 1700 I/O clock.

The DPC contains three 300-character data buffers (used as read buffers for a read operation). For a standard read operation (as determined by the E and M variants), only 186 characters (bytes) of storage are used in each read buffer. Each 300-character read buffer is divided into three sections. Each section provides 100 characters of storage. Therefore, for a standard read operation, each section of the selected read buffer contains 62 characters.

Figure 2-2, the read sequencer block diagram, contains the following:

a. The 16 DPEC interface lines.

b. Read gates RG1 through RG4.

c. The DPC input register (24 bits).

d. The input of one of read buffers (24 bits high by 100 bits long).

The read sequencer timing diagram is shown in figure 2-3. The operation of the read sequencer during a read operation is described in the following paragraphs.

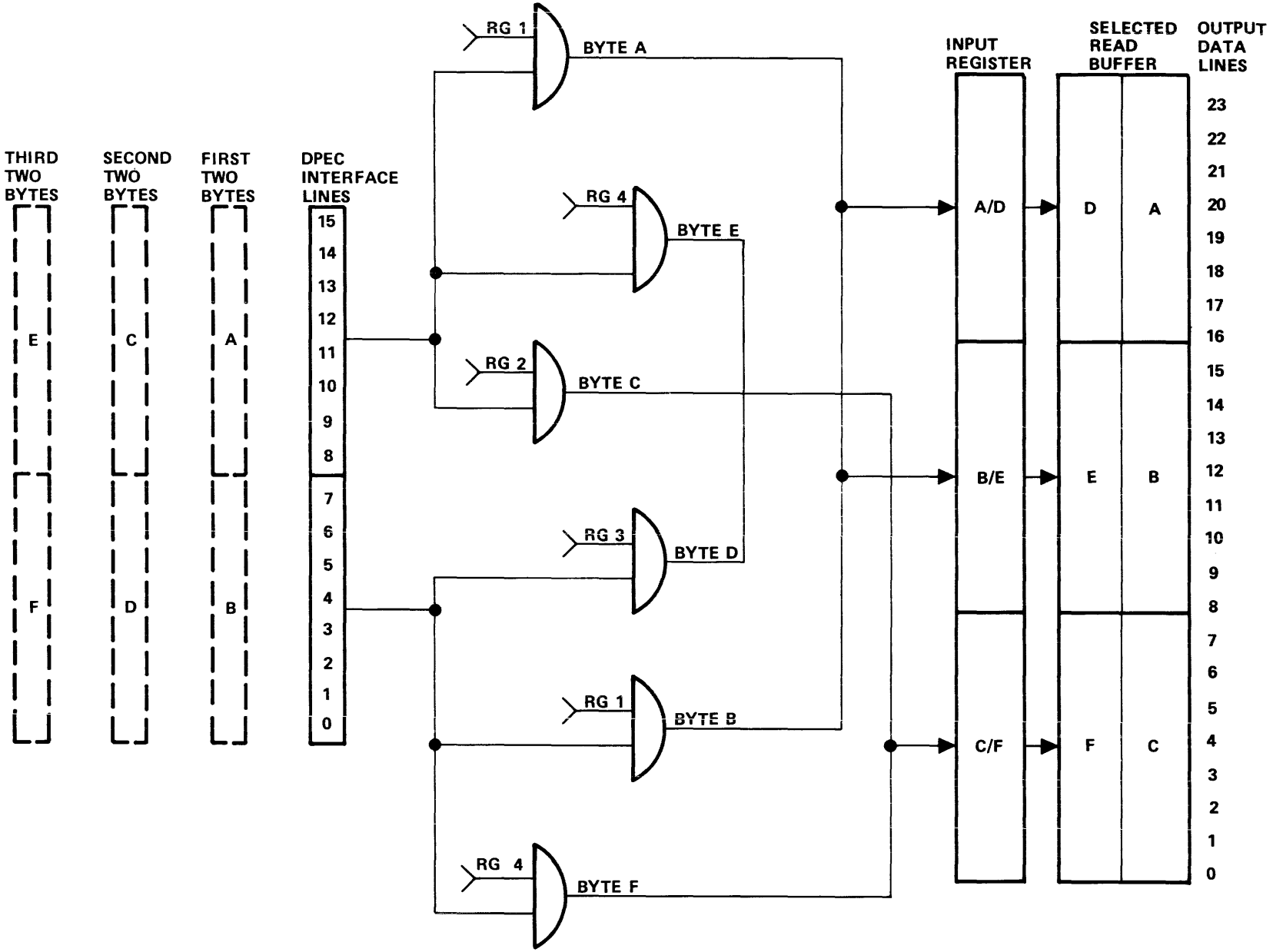


Figure 2-2. Read Sequencer Block Diagram

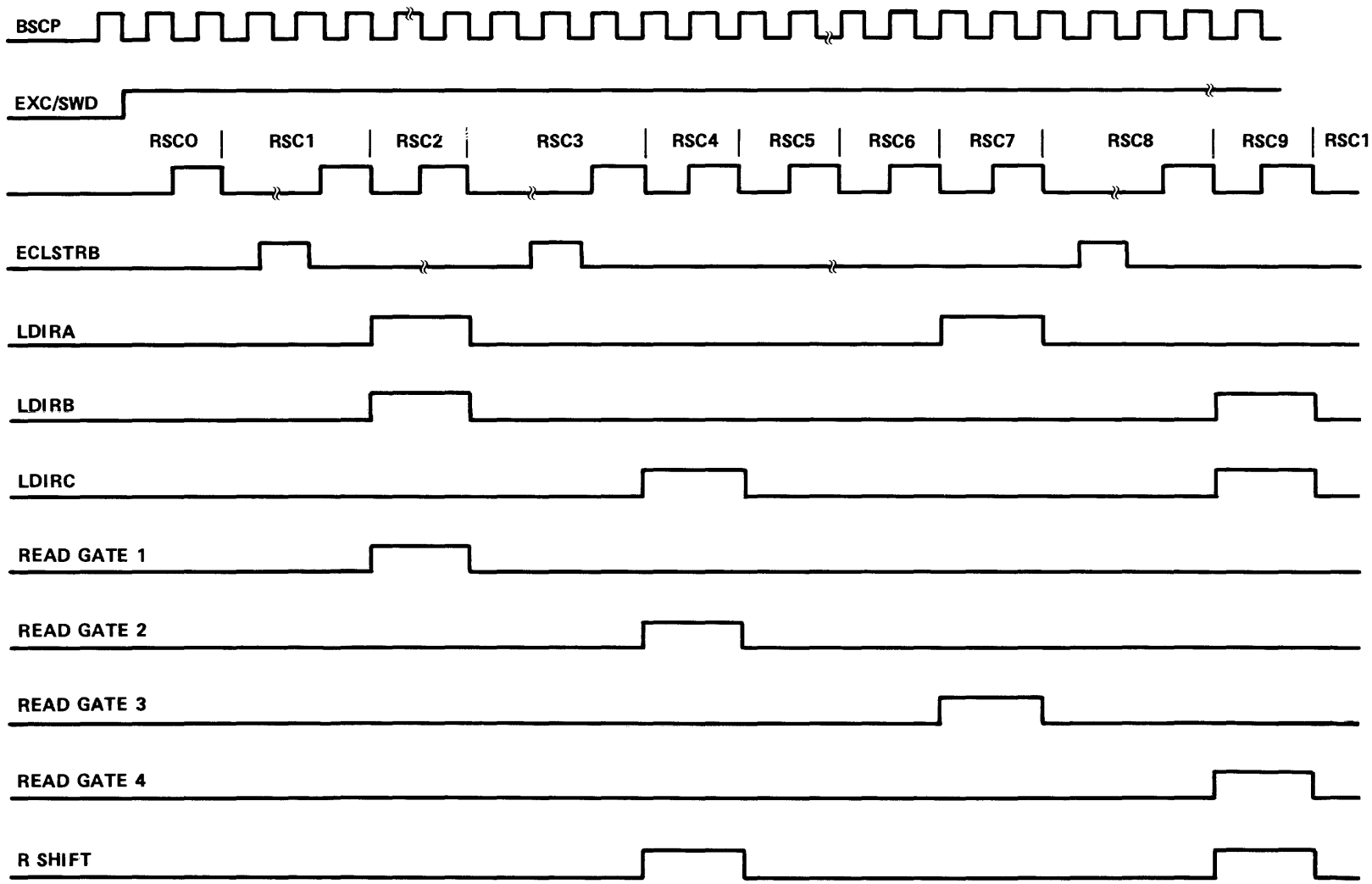


Figure 2-3. Read Sequencer Timing Diagram

The read sequencer logic is initiated by SC03, STC10, and the term Execute/Send (EXC/SND). The EXC/SND term results when the DPC Execute line is set true. When the execute line is true, the DPC is logically ready to receive read data from the DPEC. The EXC/SND* (System Clock) logic increments the read sequencer from RSC0 to RSC1. The DPC remains in RSC1 until a clock pulse (ECLSTRB) is received from the DPEC. This clock pulse is used to indicate that read data is on the 16-bit interface lines from the DPEC. The DPEC clock pulse (ECLSTRB) increments the read sequencer from RSC1 to RSC2.

During RSC2, the 16 bits of read data are shifted from the DPEC interface into the DPC input register by means of read gate 1. The A-portion of the read data is latched to the A/D section of the input register. The B-portion of the read data is latched into the B/E section of the input register. In addition, the read sequencer is incremented from RSC2 to RSC3.

The DPC remains in RSC3 until another ECLSTRB is received from the DPEC. The second DPEC clock pulse is used to indicate that the second group of read data is on the 16-bit interface lines from the DPEC. This same DPEC clock pulse also increments the read sequencer from RSC3 to RSC4. During RSC4, the C portion of the read data (eight bits) on the DPEC interface lines is latched to the CF section of the input register. At this time, the input register contains the following:

a. Section A/D contains the A byte from the DPEC.

b. Section B/E contains the B byte from the DPEC.

c. Section C/F contains the C byte from the DPEC.

The B 1700 I/O clock then shifts the contents of the input register into the D, E, and F portions of the read buffer. In addition, the read sequencer is incremented to RSC5. The next two I/O clock pulses count the read sequencer to RSC6, then to RSC7.

During RSC7, the D portion of the read data (eight bits) on the DPEC interface lines is latched to the A/D section of the input register by means of read gate 3. In addition, the read sequencer is incremented from RSC7 to RSC8.

The DPC remains at RSC8 until another ECLSTRB is received from the DPEC. This clock pulse is used to indicate that the third two bytes of read information are on the DPEC interface lines. In addition, ECLSTRB increments the read sequencer from RSC8 to RSC9.

During RSC9, the 16 bits of read data are latched from the DPEC interface into the DPC input register by means of read gate 4. The E portion of the read data is latched into the B/E section of the input register. The F portion of the read data is shifted into the C/F section of the input register. At this time the input register contains the following:

a. Section A/D contains the D-byte from the DPEC.

b. Section B/E contains the E-byte from the DPEC.

c. Section C/F contains the F-byte from the DPEC.

The B 1700 I/O clock then shifts the contents of the input buffer into the D, E, and F portions of the read buffer. The same clock also is used to shift the contents of the D, E, and F portions of the read buffer into the A, B, and C portions, respectively. In addition, the read sequence is set to 1 (RSC1).

The read buffer now contains the A, B, C, D, E, and F bytes of read data from the DPEC as indicated in figure 2-2.

This six-byte read data sequence is repeated 31 times for a one-sector read operation, providing 180 data bytes, four bytes of Fire Code, and two bytes of DPEC result descriptor.

WRITE SEQUENCER

The write sequencer consists of a counter gated to count from 0 through 4 (SSC0 through SSC4) and three write gates (WG1 through WB3). The counter and gates are used to provide write data shift control between the write buffers in the DCP and the DPEC interface lines. Information is stored in 24-bit (three-byte) increments in the write buffers. Information to the DPEC interface lines must be transferred in 16-bit (two-byte) increments.

The same three 300-character buffers in the DPC that are used as read buffers for a read operation are also used as write buffers for a write operation. Each of the three write buffers is divided into three sections. Each section provides 100 bytes of write data storage. For explanatory purposes regarding the write sequencer operation, only one write buffer will be used.

Figure 2-4, the write sequencer block diagram, contains the following:

a. The output of a write buffer (24 bits high by 100 bits long).

b. The DPC output register.

c. Write gates WG1, WG2, and WG3.

d. The 1C DPEC interface lines.

The write sequencer timing diagram is shown in figure 2-5.

The operation of the write sequencer is described in the following paragraphs:

The write sequencer logic is initiated by SC04, STC10, and the term Execute/Send (EXC/SND). The EXC/SND term is the output of the execute flip-flop and indicates that the DPC is ready to send write data to the DPEC interface lines.

The next I/O clock (DSCP) increments the write sequencer from SSC0 to SSC1.

The first DSCP during SSC1 shifts the contents of the write buffers to the left, accomplishing the following:

a. The contents of A are latched into the A/D section of the output register.

b. The contents of B are latched into the B/E section of the output register.

c. The contents of C are latched into the C/F section of the output register.

d. The D, E, and F portions of the write buffer are shifted in the A, B, and C portions, respectively.

e. The write sequencer is incremented from SSC1 to SSC2.

The first DSCP during SSC2 sets write gate 1 (WG1) TRUE. Write gate 1 gates the A and B bytes from the output register to the DPEC Interface Lines. The DPC remains in SSC2 until a DPEC clock pulse (ECLSTRB) is received. This ECLSTRB indicates to the DPC that the write data (A and B bytes) has been transferred to the DPEC.

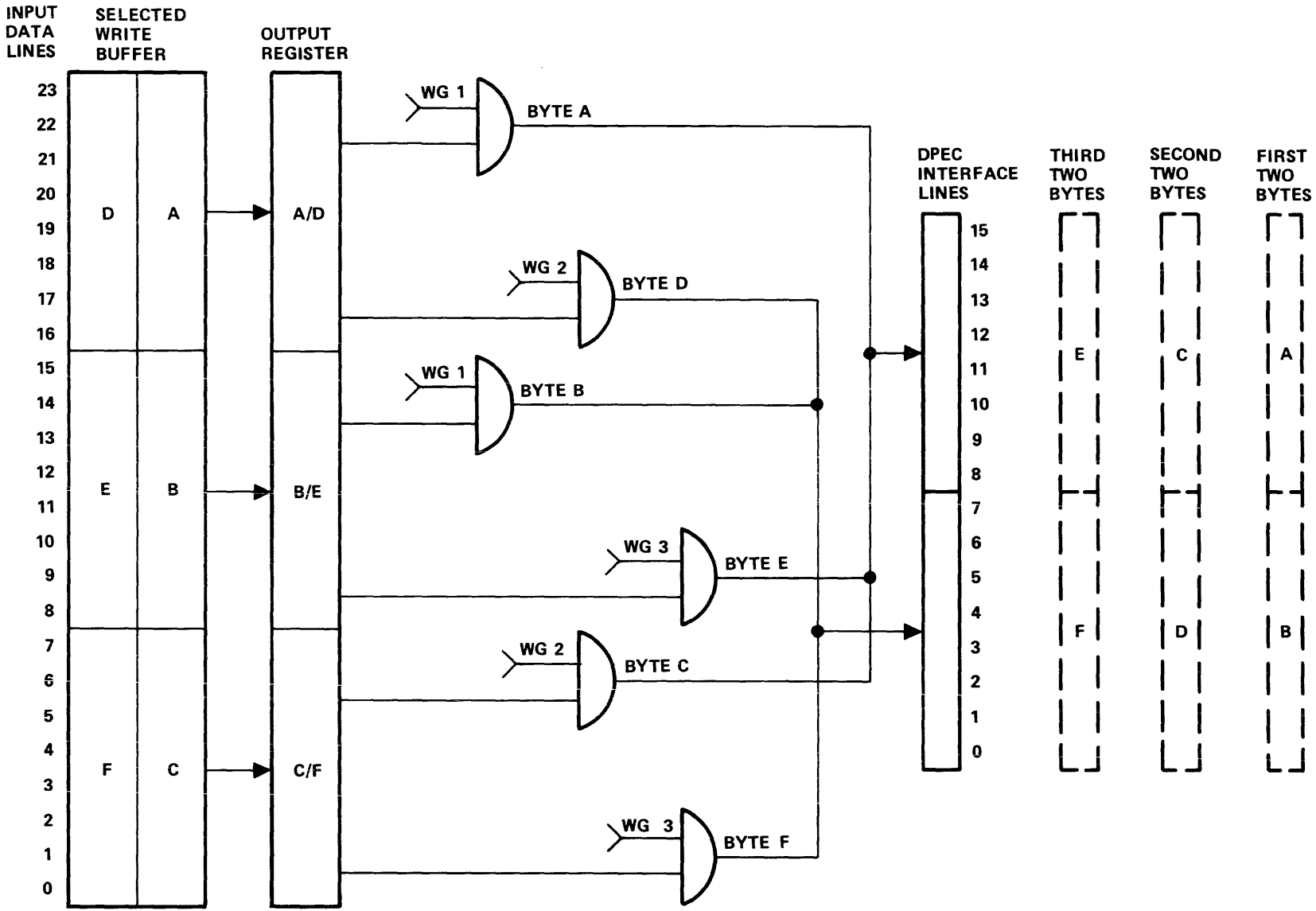


Figure 2-4. Write Sequencer Block Diagram

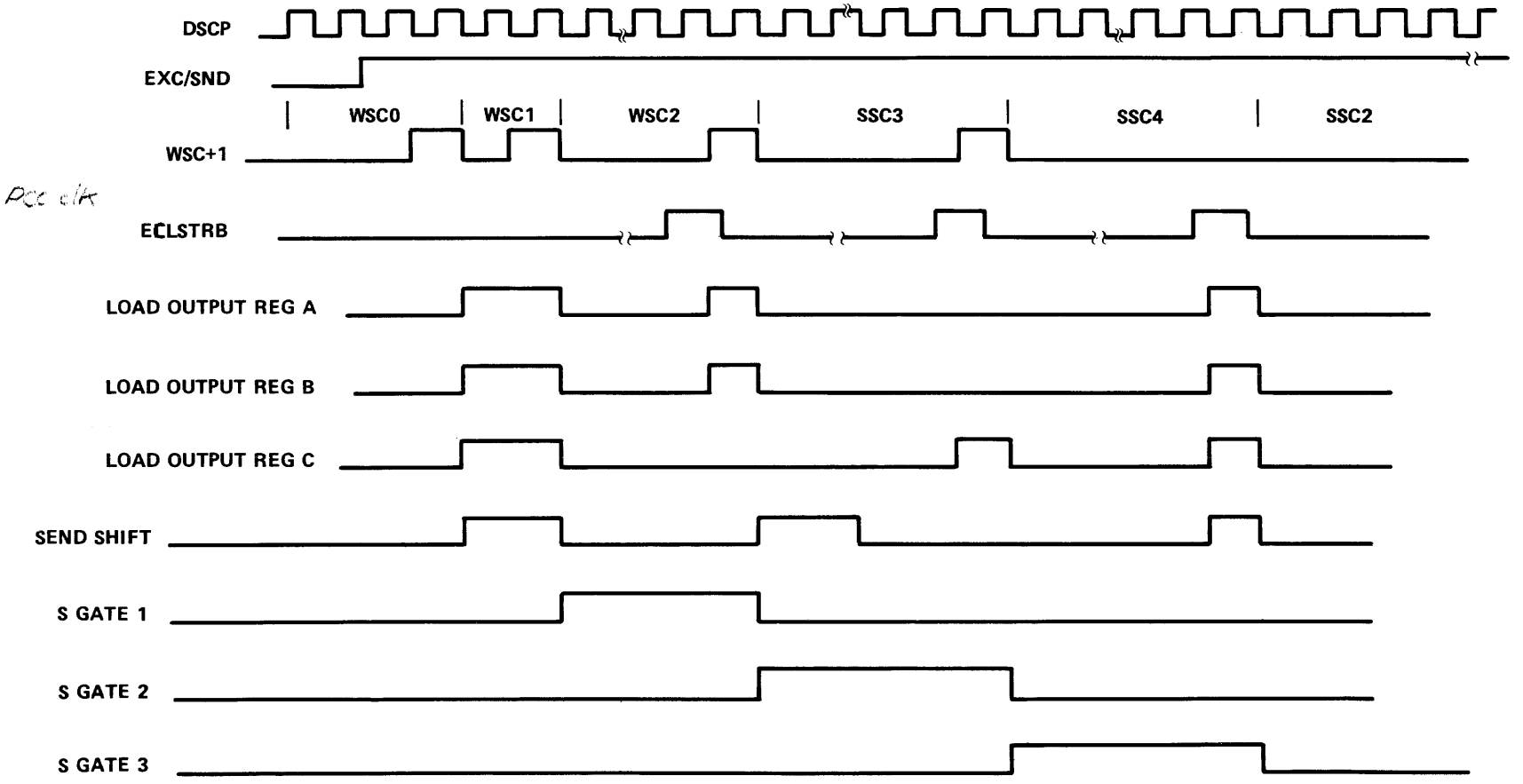


Figure 2-5. Write Sequencer Timing Diagram

The next DSCP following ECLSTRB increments the write sequencer from SSC2 to SSC3 and performs the following:

a. The A portion of the write buffer (containing the D-write data byte) is latched into the A/D section of the output register.

b. The D portion of the write buffer (containing the 7th write data byte) is shifted into the A portion.

c. The B portion of the write buffer (containing the E-write data byte) is latched into the B/E section of the output register.

Write gate 2 gates the C and D bytes from the output register to the DPEC interface lines. The DPC remains in SSC3 until an ECLSTRB is received from the DPEC. This ECLSTRB is used to indicate to the DPC that the write data (C and D bytes) has been transferred to the DPEC.

The next DSCP following ECLSTRB increments the write sequencer from SSC3 to SSC4 and latches the C-portion of the write buffer (containing the F-write data byte) into the D/F section of the output register.

During SSC4, write gate 3 (WG3) is true. Write gate 3 gates the E and F bytes from the output register to the DPEC interface lines. The DPC remains in SSC4 until an ECLSTRB is received from the DPEC. This ECLSTRB indicates to the DPC that the write data (E and F bytes) has been transferred to the DPEC.

The next DSCP after ECLSTRB performs the following:

a. The write sequencer is set to SSC2.

b. The contents of the A, B, and C portions of the write buffer (containing the 7th, 8th, and 9th write data bytes) are latched into the A/D, B/E, and C/F sections of the output buffer respectively.

c. The write buffer is shifted one place left, placing the 10th, 11th, and 12th bytes in the A, B, and C portions of the write buffer, respectively.

DISK PACK CONTROL OPERATIONS

The four basic DPC operations are listed as follows:

a. Pause operation.

b. Test operation.

c. Read operation (includes search operations).

d. Write operation (includes initialize and relocate operations).

Each of these four operations are described in detail in the following paragraphs.

TEST AND PAUSE OPERATORS

The test and pause operators are combined into a single flow block diagram (figure 2-6). The idle state of the DPC is STC01. During this status count, the DPEC is polled to determine if any Seek operations are complete. In addition, when the DCP is initiated, STC01 is used to transfer the first byte (eight bits) of the operation code from the I/O driver to the DCP. At the completion of this transfer, the status counter is incremented to STC02.

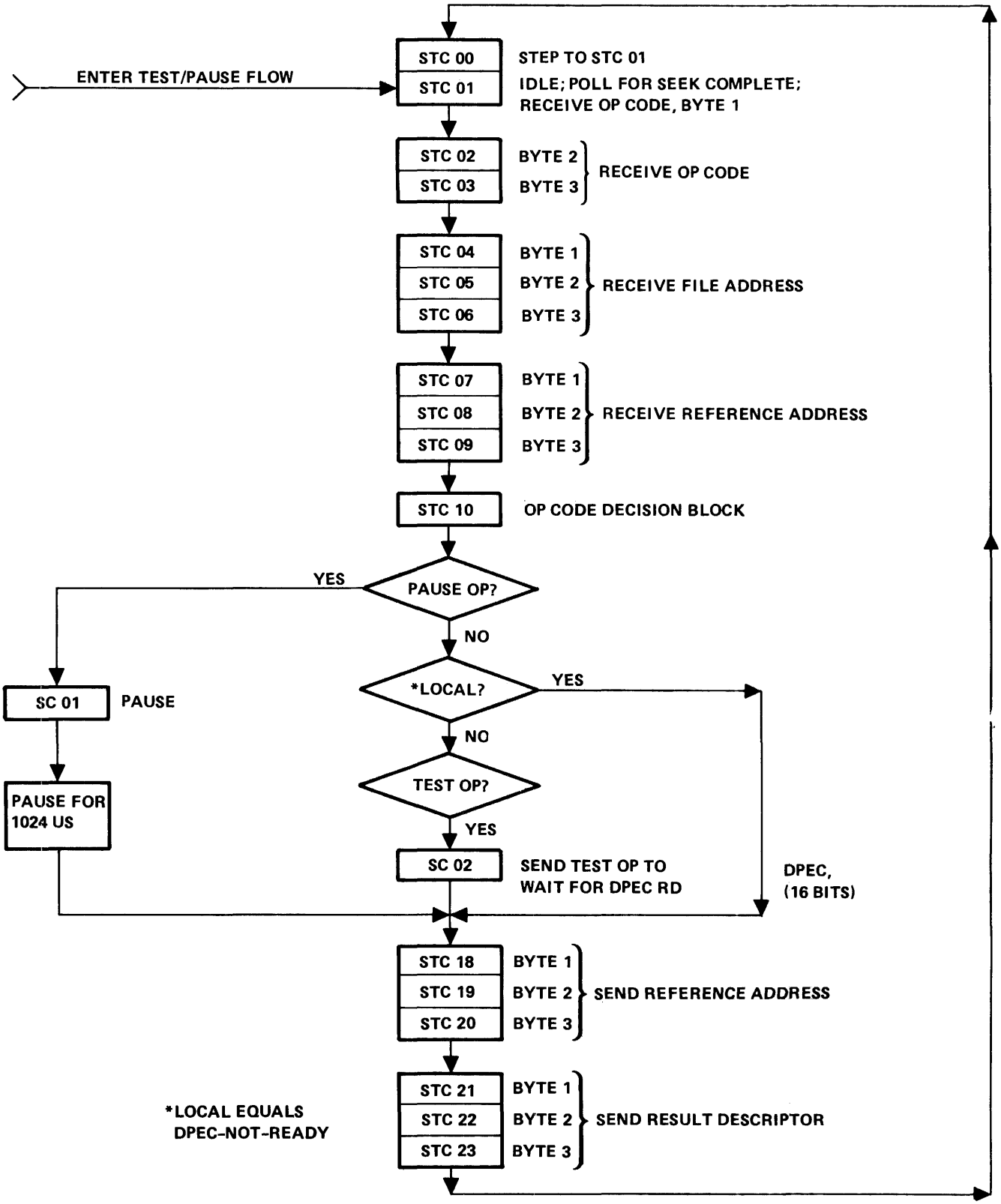


Figure 2-6. Disk Pack Control Test/Pause Flow

During STC02 and STC03, the second and third bytes of the op code are transferred from the I/O driver to the DPC. Status counts STC04 through STC06 are used to transfer the three-byte file address from the I/O driver to the DPC.

Status counts STC07 through STC09 are used to transfer the three-byte reference address from the I/O driver to the DPC.

Status count STC10 is used to set the sequence counter to perform the operation specified by the op code. For a pause operator, the sequence counter is set to SC01. A test operator sets the sequence counter to SC02.

If the operator is a test, this operator is transferred from the DPC to the DPEC. The DPC stays in STC10*SC02 until the DPEC transmits the 16-bit result descriptor to the DPC. When the DPC receives the DPEC result descriptor, the status counter is set to STC18 and the sequence counter is set to SC00.

During STC18 through STC20, the three-byte reference address is transferred from the DPC to the I/O driver.

During STC21 through STC23, the three-byte result descriptor is transferred from the DPC to the I/O driver.

At the completion of the transfer in STC23, the status counter is set to STC00. The status counter is then incremented from STC00 to STC01 (idle state of the DPC).

READ OPERATOR

The flow block diagram for the read operator is shown in figure 2-7. The idle state of the DPC is STC01. During this status count, the DPC is polled to determine if any seek operations are complete. In addition, when the DPC is initiated, STC01 is used to transfer the first byte of the code from the I/O driver to the DPC. At the completion of this transfer, the status counter is incremented from STC01 to STC02.

During STC02 and STC03, the second and third bytes of the op code are transferred from the I/O driver to the DPC. Status counts STC04 through STC06 are used to transfer the three-byte file address from the I/O driver to the DPC.

Status counts STC07 through STC09 are used to transfer the three-byte reference address from the I/O driver to the DPC.

Status count STC10 is used to set the sequence counter to perform the operation specified by the op code. The sequence counter is set to SC03 for a read operator.

During STC10*SC03, the read operator and the file address are transferred from the DPC to the DPEC. If a seek operation is required for this read operation, the DPEC initiates the result status phase, indicated by the DPEC control logic (SELECT*BUSY*READY/). When the two-byte DPEC result descriptor is transferred from the DPEC to the DPC, the status counter is set to STC18 and the sequence counter is set to SC00.

If the seek operation for this read operation is completed and all read buffers are empty, the DPC waits for read data from the DPEC. Read data is transferred from the DPEC by using the DPEC clock pulses. Read data from the DPEC is transferred into a read buffer under control of the read sequencer logic. This logic provides shift control of the two-byte increments of read data from the DPEC to the three-byte increments stored in the DPC read buffers.

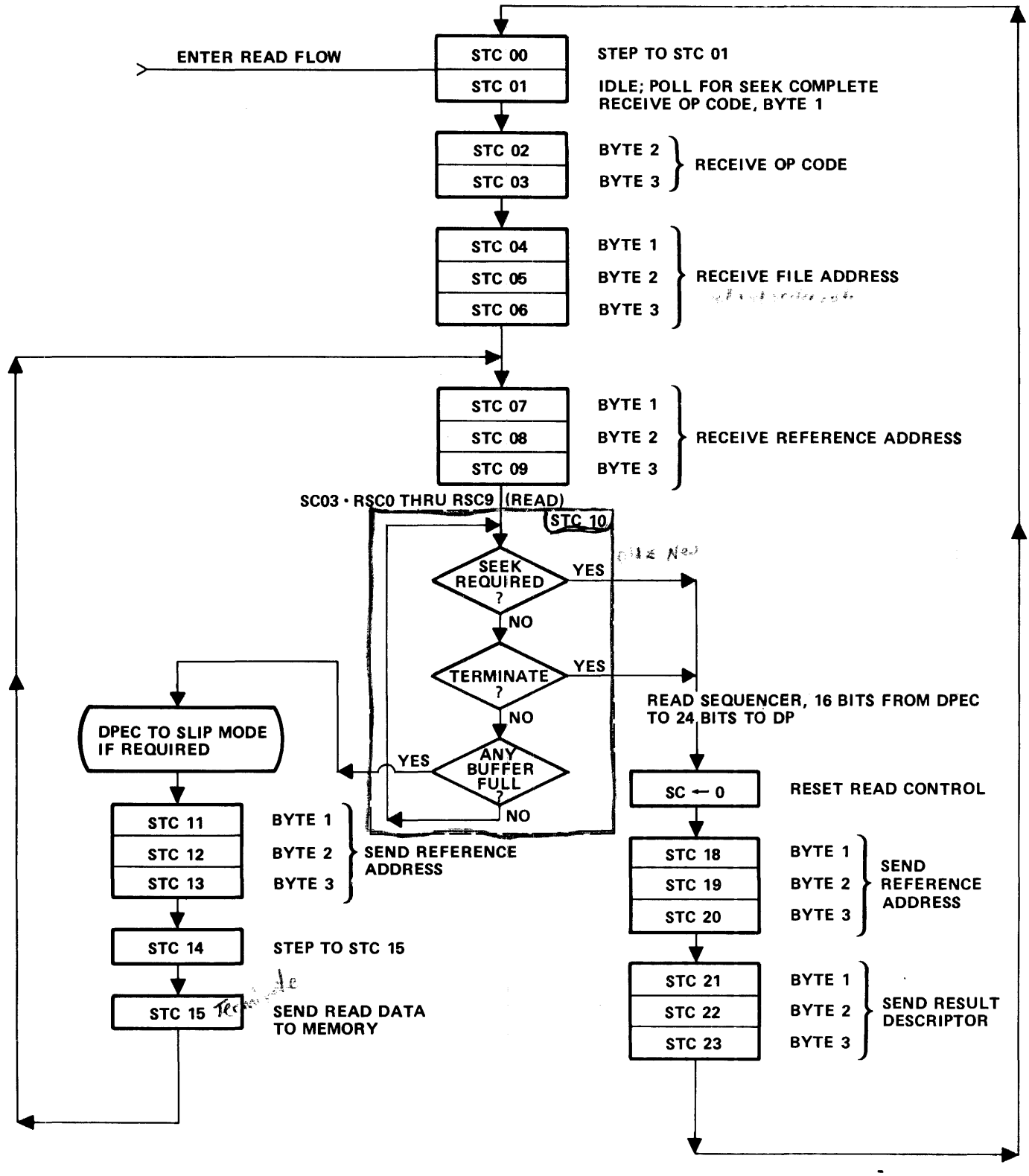


Figure 2-7. Disk Pack Control Read Flow

When any read buffer is full, the DPC increments the status counter to STC11. The sequence counter remains at SC03, however, to provide logic gating for the read data from the DPEC. When a terminate signal is detected during STC10*SC03, the DPC sets the status counter to STC18 and the sequence counter to SC00. A terminate signal from the DPC is normally used to end a read operation.

During status counts STC11 through STC13, the three-byte reference address is transferred from the DPC to the I/O driver.

During status count STC14, the status counter is incremented to STC15.

During status count STC15, the contents of a full read buffer are transferred from the DPC to the I/O driver. The number of read data bytes to be transferred is determined by the read operator M and E variants as described in the following paragraphs:

a. If the M variant is equal to 0 and the E variant is equal to 0, the read data consists of 60 bytes of data.

b. If the M variant is equal to 1 and the E variant is equal to 0, the read data consists of all the information written in the selected segment including preambles, postambles, address, read data and sync bits. See figure 1-3 for the contents of a DPD segment.

c. If the M variant is equal to 0 and the E variant is equal to 1, the read data consists of 60 bytes of data, two-bytes of DPEC result descriptor, and four bytes of Fire Code (error check code).

At the completion of the transfer, the status counter is set to STC07.

During status counts STC07 through STC09, the three-byte reference address is sent from the I/O driver to the DPC.

WRITE OPERATOR

Figure 2-8 is the flow chart for the DPC write operation. The idle state for the DPC is status count STC01. During this status count, the DPEC is polled to determine if any seek operations are completed. When the DPC is initiated, STC01 is used to transfer the first byte of the op code into the DPC and increment the status counter to STC02.

During STC02 and STC03, the second and third bytes of the op code are transferred from the I/O driver to the DPC.

Status counts STC04 through STC06 are used to transfer the three-byte file address from the I/O driver to the DPC.

Status counts STC07 through STC09 are used to transfer the three-byte reference address from the I/O driver to the DPC.

Status count STC10 sets the sequence counter to perform the operation specified by the op code.

During status count STC10, the sequence counter will be set to SC04 if this is a write operation. During STC10*SC04, the first two initiate words are transferred from the DPC to the DPEC. The first initiate word consists of the op code and variants; the second initiate word consists of the file address. Transferring the second initiate word from the DPC to the DPEC sets a 64-microsecond timer (TIMERF). If a seek operation is required on the selected DPD, the DPEC goes to the result status phase (RESULTP). The result status phase is indicated by the following DPEC control logic: (SELECT*BUSY*READY/).

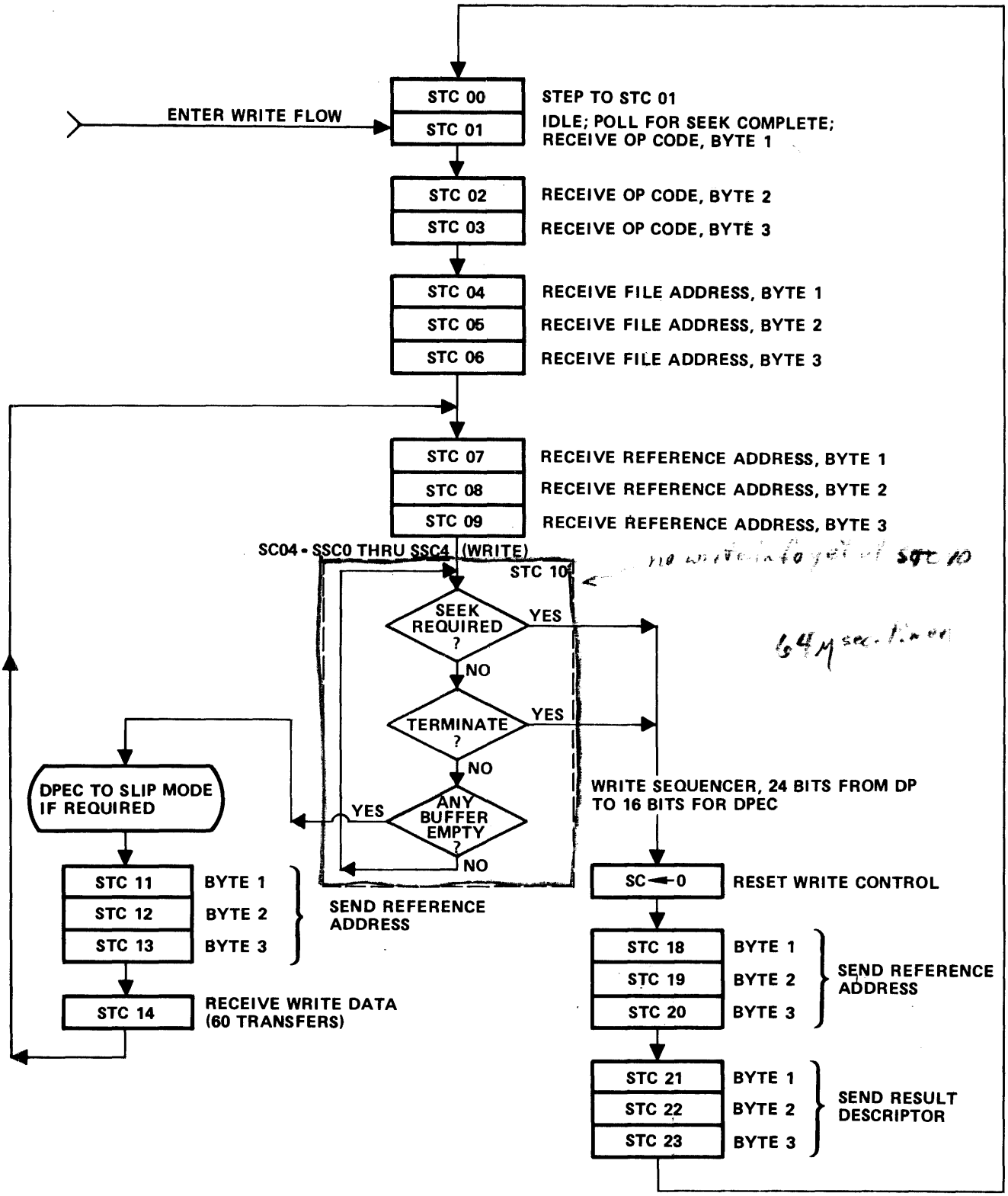


Figure 2-8. DPC Write Operation Flow

If the DPEC goes to the result status phase, the DPC waits for a two-byte result descriptor from the DPEC. When the DPEC result descriptor is transferred to the DPC, the status counter is set to STC18 and the sequence counter is set to STC00.

If a seek operation is completed or not required, the DPC waits until the timer times out (64 nanoseconds), and then the status counter is incremented to STC11. However, the sequence counter remains at SC04 to provide DPC-to-DPEC write gating. Once the DPC is in the write cycle (sequence counter remains at SC04), the timer will not be restarted.

If any buffer is full and the DPC is in sequence count SC04, write data is transferred from one of the (full) write buffers to the DPEC, under the control of the write sequence logic (SSC0 through SSC4). This transfer of write data continues until all write buffers are empty or, until a terminate signal is detected while the DPC is in STC10*SC04.

Each time that the DPC is in STC10*SC04, a check is made to ascertain if any write buffers are empty. If any write buffers are empty and a terminate signal has not been received, the status counter is incremented to STC11. In addition, a service request flag is set (SRF←1) indicating to the I/O driver that write data is needed for an empty write buffer in the DPC.

If a terminate signal is detected, the status counter is set to STC18 and the sequence counter is set to SC00, terminating the write operation.

During status counts STC11 through STC13, the three-byte reference address is transferred from the DPC to the I/O driver. During status count STC14, one of the empty write buffers receives sixty 24-bit transfers of write data from the I/O driver. When the transfer operation is complete, the status counter is set to STC07.

During STC07 through STC09 the three-byte reference address is transferred from the I/O driver to the DPC. The status counter is then incremented to STC10 and the operation is repeated as previously described.

During STC18 through STC20 the three-byte reference address is transferred from the DPC to the I/O driver.

During STC21 through STC23, the three-byte result descriptor is transferred from the DPC to the I/O driver. When the transfer is completed, the status counter is reset (cleared) to STC00. During STC00 the status counter is incremented to STC01 (idle state for the DPC).

SLIP MODE

The slip mode of operation allows the disk pack subsystem to remain in a read or write status, even when no data is being transferred between the DPC and the DPEC.

During slip mode, the selected DPD remains on the same cylinder, but reading or writing operations are suspended. The address is monitored, however, by the DPEC. The last disk pack address used for a read or write operation just prior to entering the slip mode is retained in a register in the DPEC. On each revolution when address coincidence is achieved, the DPEC checks to ascertain if the condition that caused the slip mode has been corrected. The logic term that indicates slip mode is SELECT*BUSY*READY*EXECUTE/.

Entering the slip mode is accomplished by the DPC setting the Execute level false. This will occur under the following conditions:

a. If the DPC is executing a read operation and all three read buffers are full.

b. If the DPC is executing a write operation and all three write buffers are empty.

When the necessary transfers between these buffers and I/O driver occur, the DPC will set the Execute level true. The first address coincidence in the DPEC with Select, Busy, Ready, and Execute true will provide the logic to exit the slip mode and resume reading or writing.

SEEK OPERATION

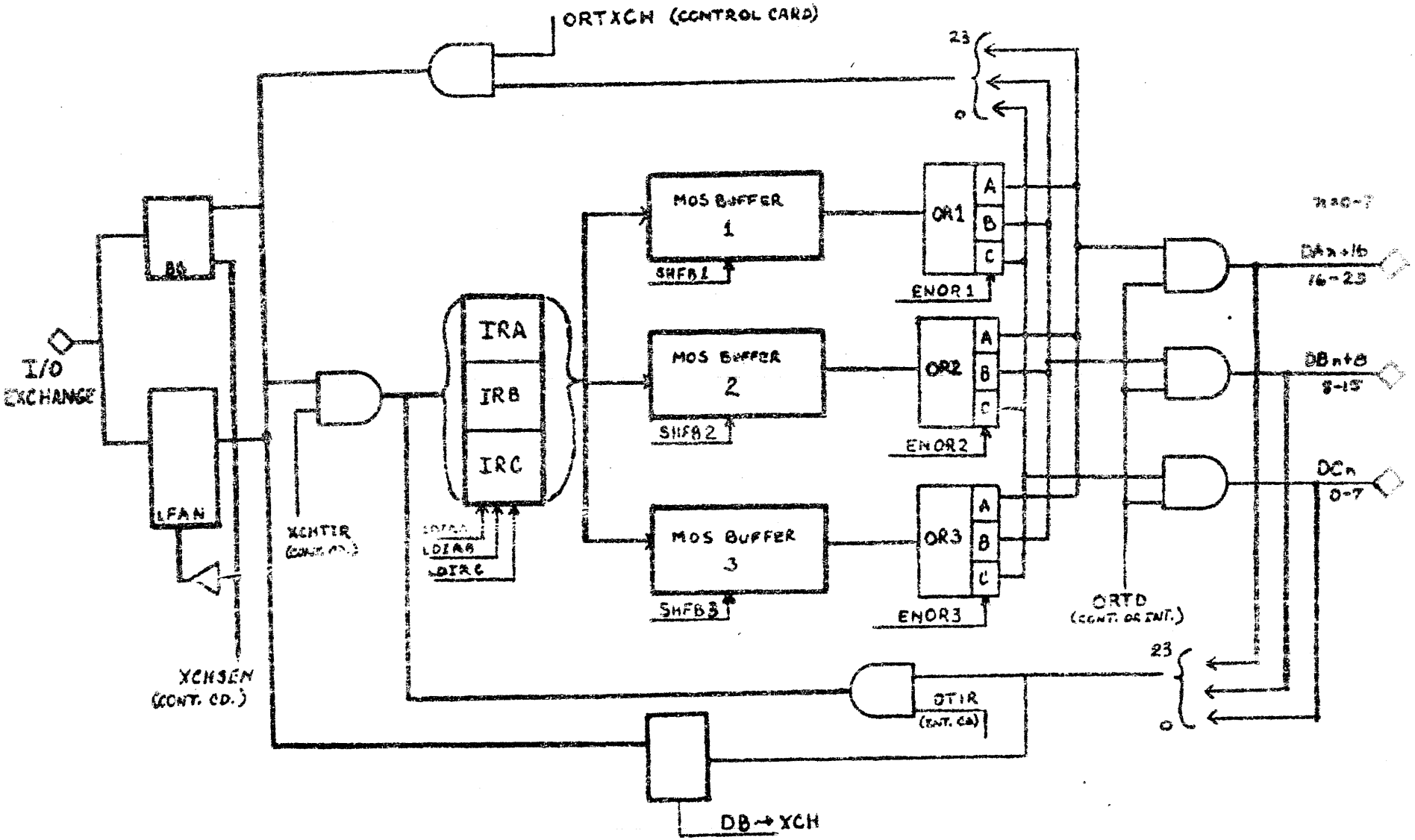
The disk pack subsystem consists of one DPC, one DPEC, and one-to-eight DPD's. The file address and unit select are used by the DPEC to determine the DPD and the cylinder required for the requested operation. The relocation of the selected DPD read/write heads to the correct cylinder is called a seek operation. When the DPD read/write heads are positioned at the cylinder requested by the file address, the seek operation is complete. While the DPD read/write heads are being repositioned, a Seek-in-progress bit will be set in the result descriptor of any requesting operator.

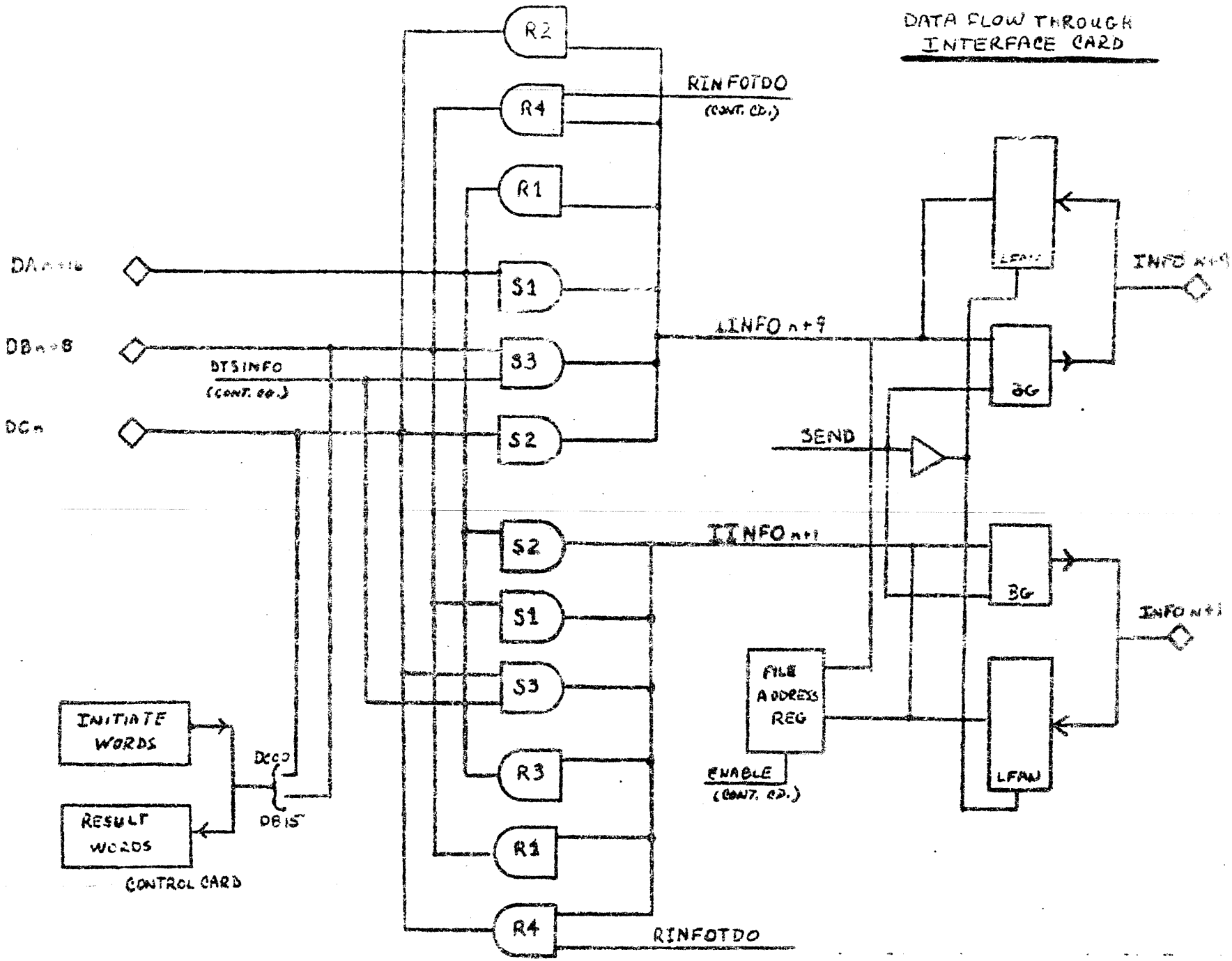
During the idle state (STC01*No-Operation-Requested), the DPC generates test descriptors to each of the DPD's in sequence. If any seek operations are complete, the service request flip-flop is set to one (SRF←1), which, in turn, sets the interrupt flip-flop in the central processor to 1. The MCP activates the I/O driver to handle the interrupt. The I/O driver issues DPC operators from the disk pack queue until the operator that requested the address of the completed seek operation is found. The selected operator is then executed. At the completion of the operation the DPEC seek status flip-flop is reset to 0.

POLLING

The DPC provides the ability to poll for a Seek complete while the DPC is in the idle state (STC01*No-Operation-Requested). The start flip-flop is used to allow a polling sequence. Any DPC operator sets the start flip-flop to 1. Therefore, if the start flip-flop is set to 0 and the DPC is at STC01, a poll sequence is initiated. Each time that the DPC is idle at STC01, a test descriptor is generated. This test descriptor is transferred to the DPEC by setting the Select line in the DPC to 1. The DPEC (in response to a test descriptor) goes into the result status phase, during which the DPEC returns a 16-bit result descriptor to the DPC. If any seek operation is completed, the DPEC interface lines contain the following logic: (02*031). This logic is used to set the service request flip-flop to 1 (SRF←1) which in turn, sets the interrupt flip-flop in the central processor to 1. The MCP detects the interrupt flip-flop and initiates the I/O driver. If the DPC is at STC01 and the service request flip-flop is set to 1, the I/O driver sends a DPC descriptor to the DPC. The DPC descriptors are contained in a queue within the I/O driver. Each descriptor is sent sequentially from the queue. If any seek operation is completed for any disk pack descriptor, that descriptor is executed. Since a seek operation may be in progress (or completed) on every disk drive unit (spindle), the disk pack descriptor that is executed is not necessarily the one for which the seek complete was reported. When the DPC returns to the idle state, however, another test descriptor is generated and the process described previously is repeated.

H/S BUFFER CARD




DATA FLOW THROUGH INTERFACE CARD
R2
R4
R1
RINFOTDO
(CONT. CD.)
DA n+16
DB n+8
DC n
S1
S3
S2
DTSINFO
(CONT. CD.)
LINFO n+9
LFAN
INFO n+9
BG
SEND
IINFO n+1
S2
S1
S3
R3
R1
R4
RINFOTDO
BG
INFO n+1
FILE ADDRESS REG
ENABLE
(CONT. CD.)
LFAN
INITIATE WORDS
RESULT WORDS
CONTROL CARD
DC 0
DB 15

SECTION 3

CIRCUIT DETAIL

INTRODUCTION

A detailed description of the logic circuitry used in the B 1700 Disk Pack Control I is contained in the Hardware Rules book issued as part of the Field Test and Reference documentation.

SECTION 4

ADJUSTMENTS

INTRODUCTION

There are no adjustments for the B 1700 Disk Pack Control I used in the B 1700 Disk Pack Subsystem. There is, however, an initial clock adjustment that must be made during the installation of this control. Refer to the installation section of this manual (section 6) and the Field Test and Reference documentation for information on this initial adjustment.

SECTION 5

MAINTENANCE PROCEDURES

INTRODUCTION

The B 1700 Disk Pack Control I is a part of the B 1700 Disk Pack Subsystem, therefore, although maintenance and preventive maintenance can be done on an individual unit basis, troubleshooting and confidence testing should be done on the entire disk pack subsystem whenever possible.

PREVENTIVE MAINTENANCE

There is no preventive maintenance required for the B 1700 Disk Pack Control I.

MAINTENANCE CONCEPT

The B 1700 Disk Pack Control I is a soft control and does not contain any off-line testing capabilities. The maintenance concept for this I/O control is structured around the diagnostic test routines used in conjunction with the B 1700 Field Card Tester.

SPECIAL MAINTENANCE TOOLS

The following list of test routines and tools are required to maintain a B 1700 Disk Pack Control I.

a. I/O Debug Test Routine (I/O Debut).

b. Disk Pack Control Diagnostic Routine (DSKPAC/TEST).

c. B 1700 Field Card Tester.

d. Tetronix-type-465 oscilloscope or equivalent.

e. Tripplet-type 630 VOM or equivalent.

DISK PACK CONTROL DIAGNOSTIC ROUTINE

Instructions on the use of the DPC diagnostic routine are contained in DSKPAC/TEST listing provided as part of the Field Test and Reference (FT & R) documentation. The routine consists of 13 sections (0 through 12). The function of each section is as follows:

Section	Function
0	Single track initialize and full pack initialize.
1	Verifies the initialize operation and verify the relocation function.
2	Writes, then reads multiple segments.

Section	Function
3	Writes, then reads partial segment.
4	Writes multiple segments, but reads each segment after it is written.
5	Performs a continuous read, write, test or pause operation continuously (for maintenance testing).
6	Checks DPD arm movement while writes and reads of partial segments are being performed.
7	Copies data from one disk drive to another disk drive. Data is then compared to ensure drive compatability.
8	Determines if the data is correct and relocates data to all spare sectors in the disk pack.
9	Provides a diagnostic test of write, read or a read/write buffer.
10	Determines if the Fire Code is correct on each segment.
11	Provides seek operations for segments. The sequential segments are obtained by inserting a beginning segment address and an ending segment address on the SPO.
12	Checks DPD arm movement while performing three segment writes and reads.

TROUBLESHOOTING PROCEDURES

Troubleshooting procedures for the B 1700 Disk Pack Control I must initially be performed for the entire disk pack subsystem. The disk pack subsystem consists of the following units:

a. Disk Pack Control I (DPC).

b. Disk Pack Electronics Control (DPEC).

c. Disk Pack Drives (DPD).

The Field Engineering Log (FE LOG) is a useful aid in determining operation code failures and address failures. Most of the DPD-related problems cause errors that are listed in the FE Log. For example, a history of Fire-Code errors from a particular read/write head indicates a defective head or defective preamplifier.

The set of troubleshooting guides in this section provides logical procedures for troubleshooting and problem isolation for the B 1700 Disk Pack Subsystem. If the problem area is

determined to be in either the DPEC or a DPD, the troubleshooting information provided in the applicable Field Engineering Technical Manuals (TETM's) for the DPEC and DPD units must also be referenced.

The troubleshooting guide consists of figures 5-1 through 5-10, notes 1 through 59, and tables 5-1 through 5-4. Each figure contains entry and exit points referencing another figure or a note contained in the text.

For example, an exit labeled as note 13 points to a discussion in the text labeled note 13. In-text notes are listed in numerical sequence.

Some of the references in the notes use the word "disk" or "disk subsystem," rather than a specific unit such as a disk file, disk pack or disk cartridge. Unless otherwise noted, a disk or disk subsystem refers to the unit that is used to store the MCP and program information.

To use the troubleshooting guides proceed as follows:

a. Refer to figure 5-1, disk pack troubleshooting guide.

b. Follow the referenced flows, notes, and tables to determine the problem area.

c. Use applicable test routines and the B 1700 Field Card Tester to determine the cause of the failure.

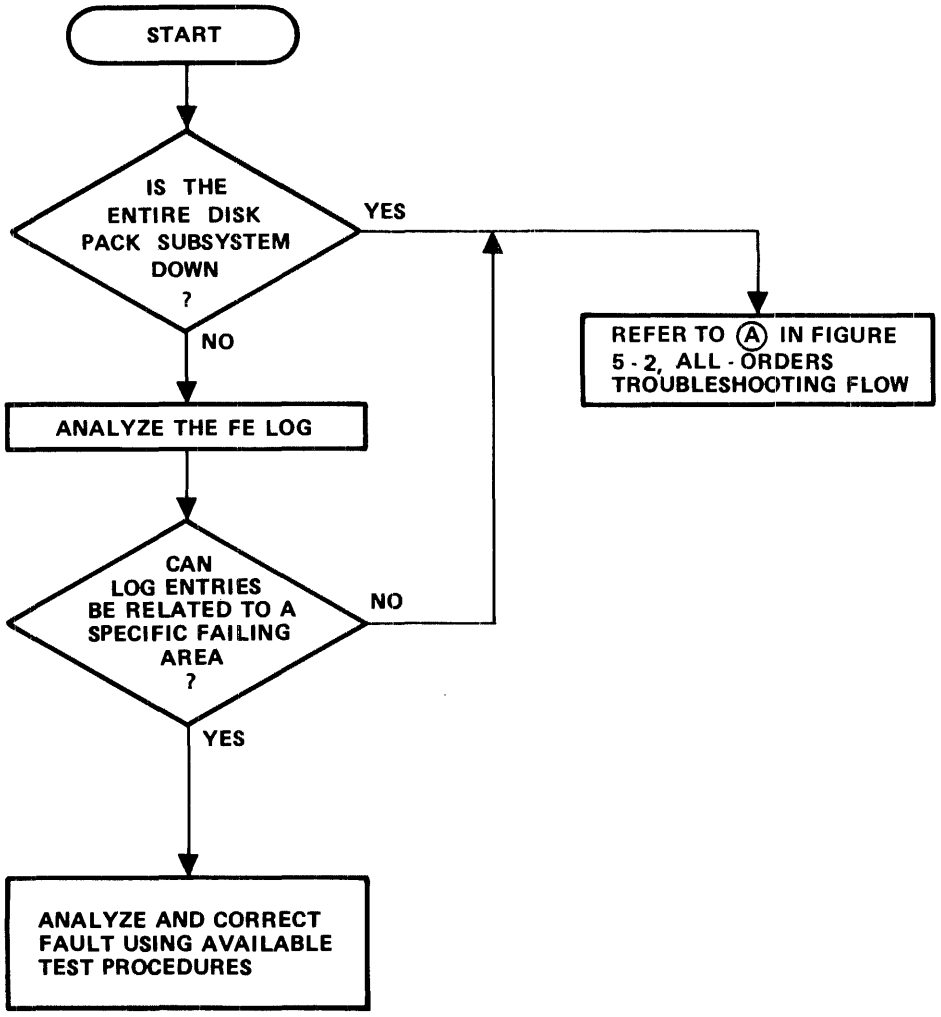


Figure 5-1. Disk Pack Subsystem Troubleshooting Guide

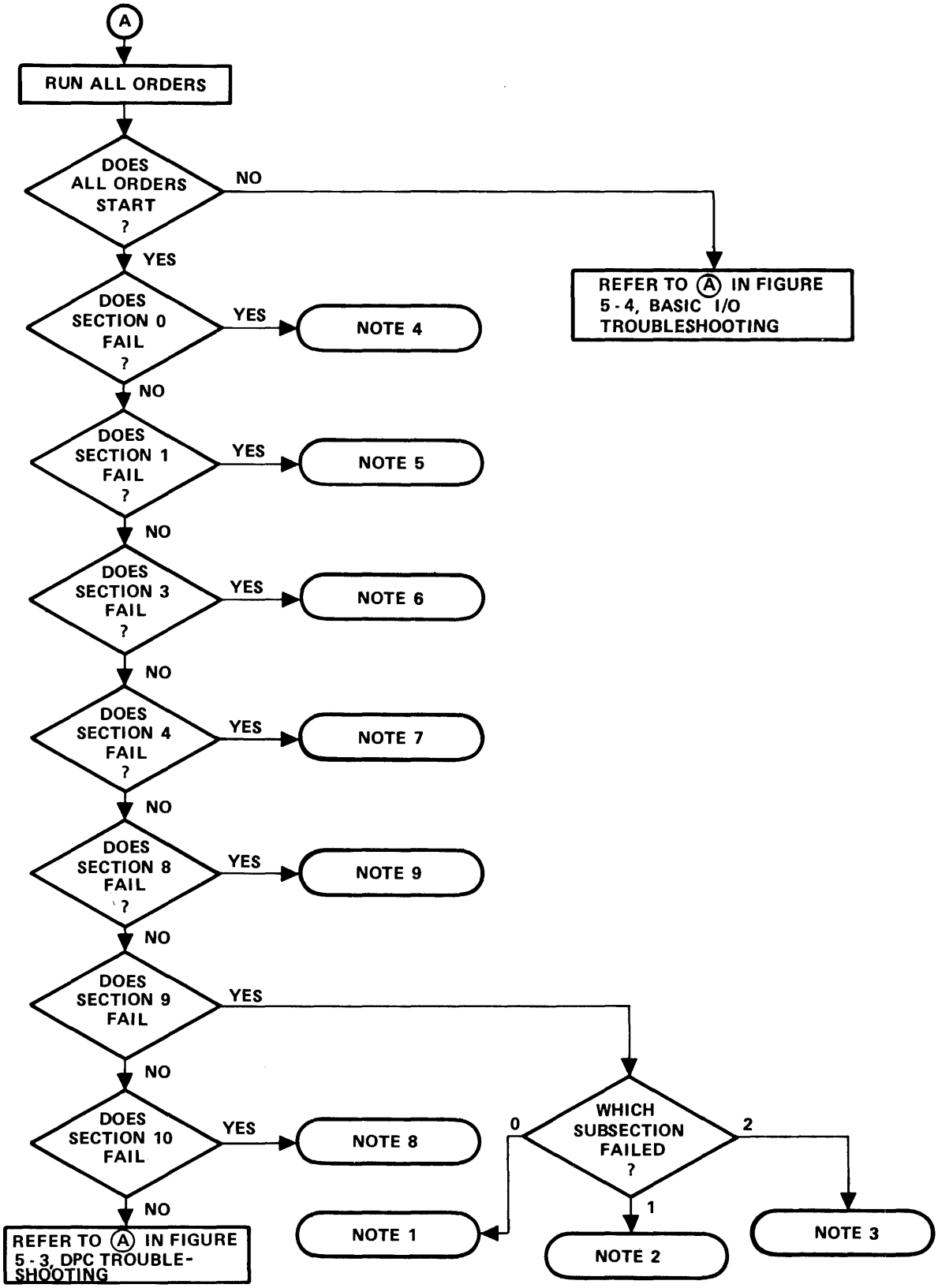


Figure 5-2. All-Orders Troubleshooting Flow

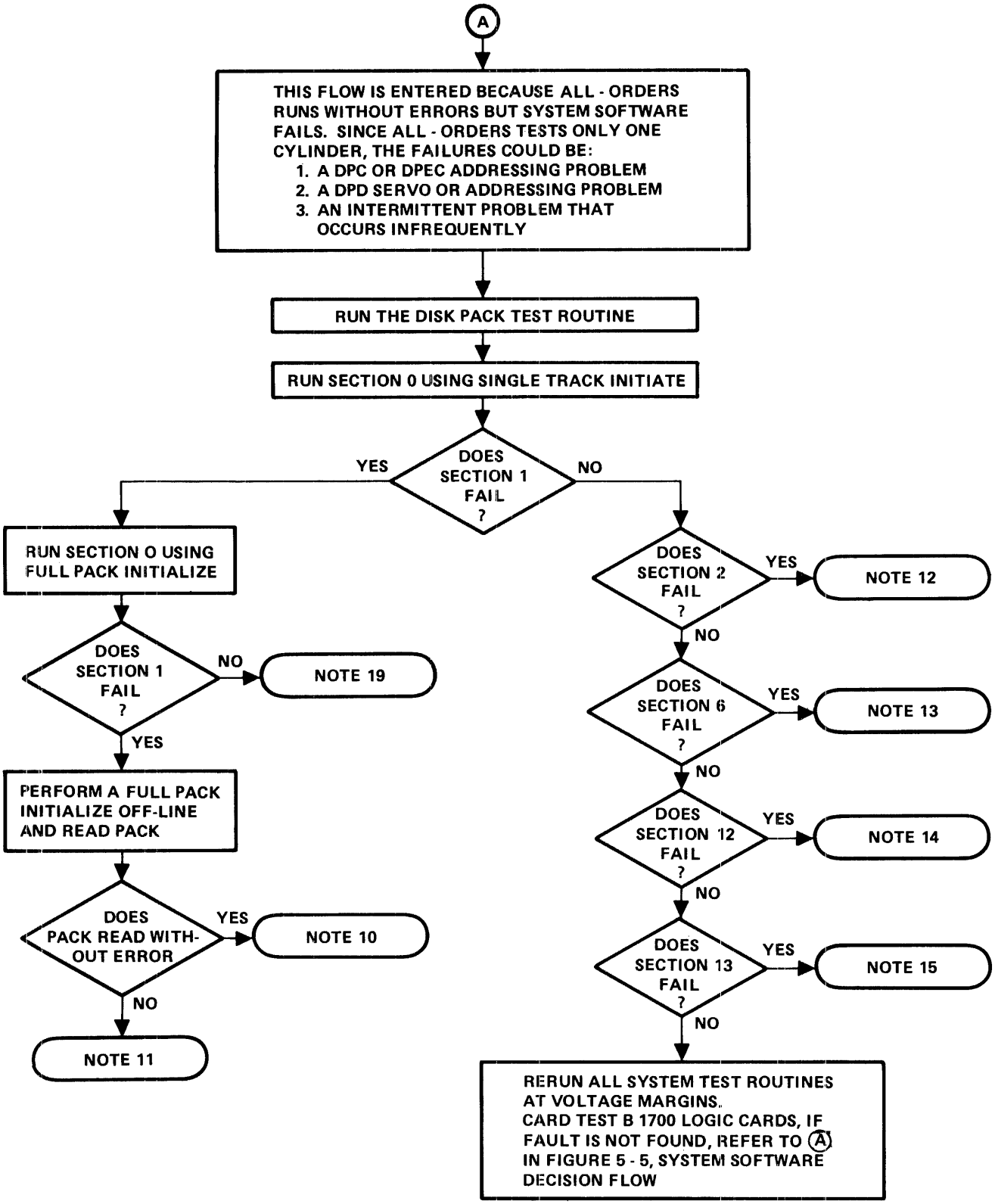


Figure 5-3. DPC Test Routine Troubleshooting Flow

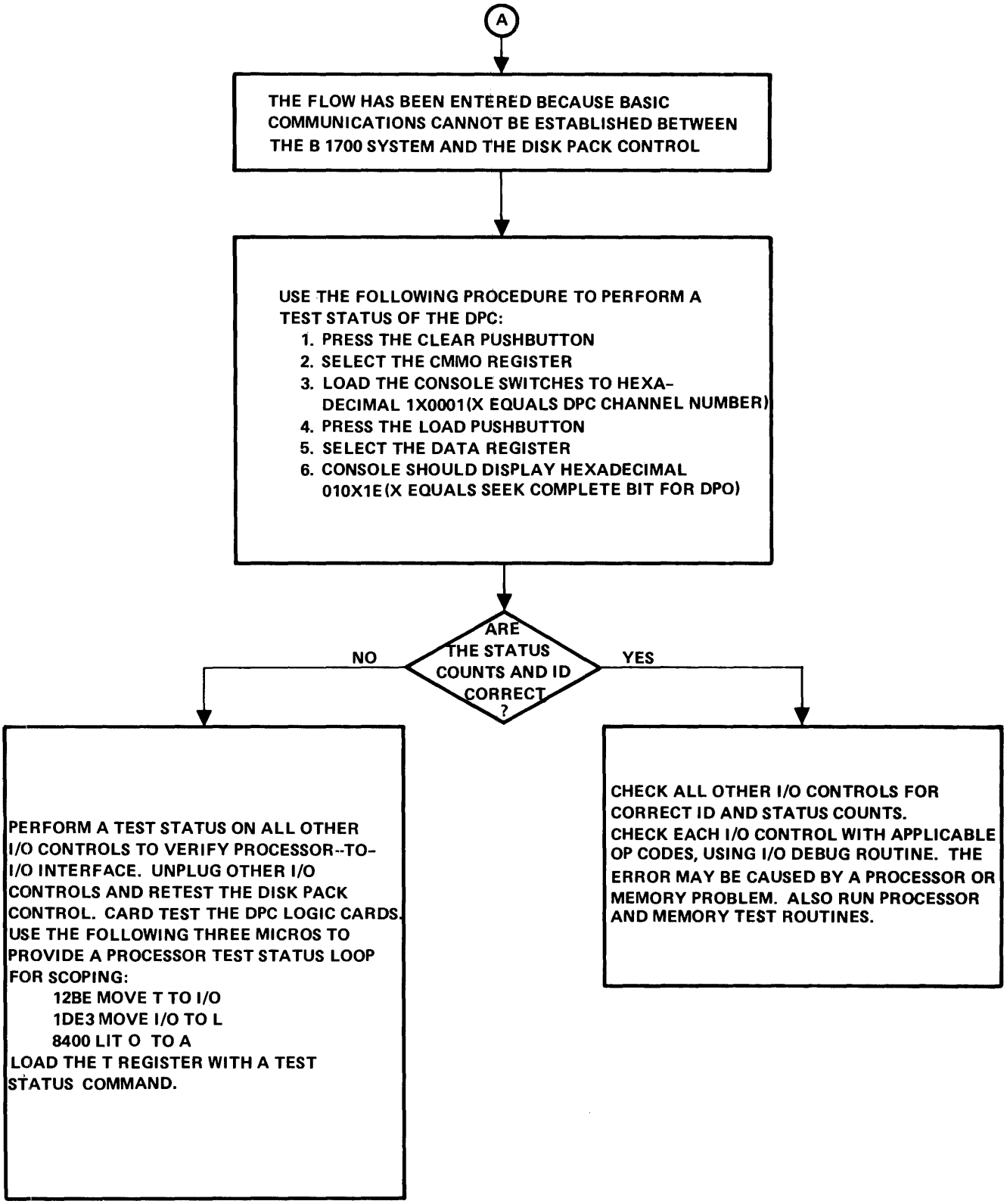


Figure 5-4. Basic I/O Troubleshooting Flow

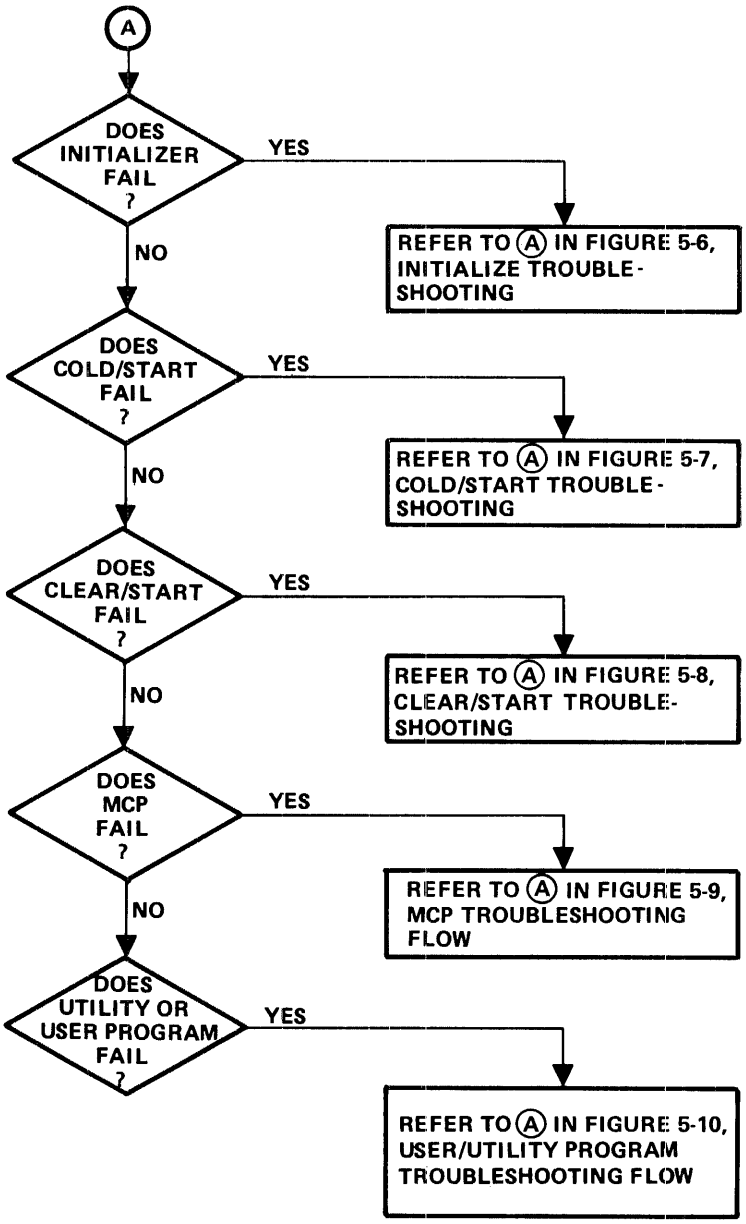


Figure 5-5. System Software Decision Flow

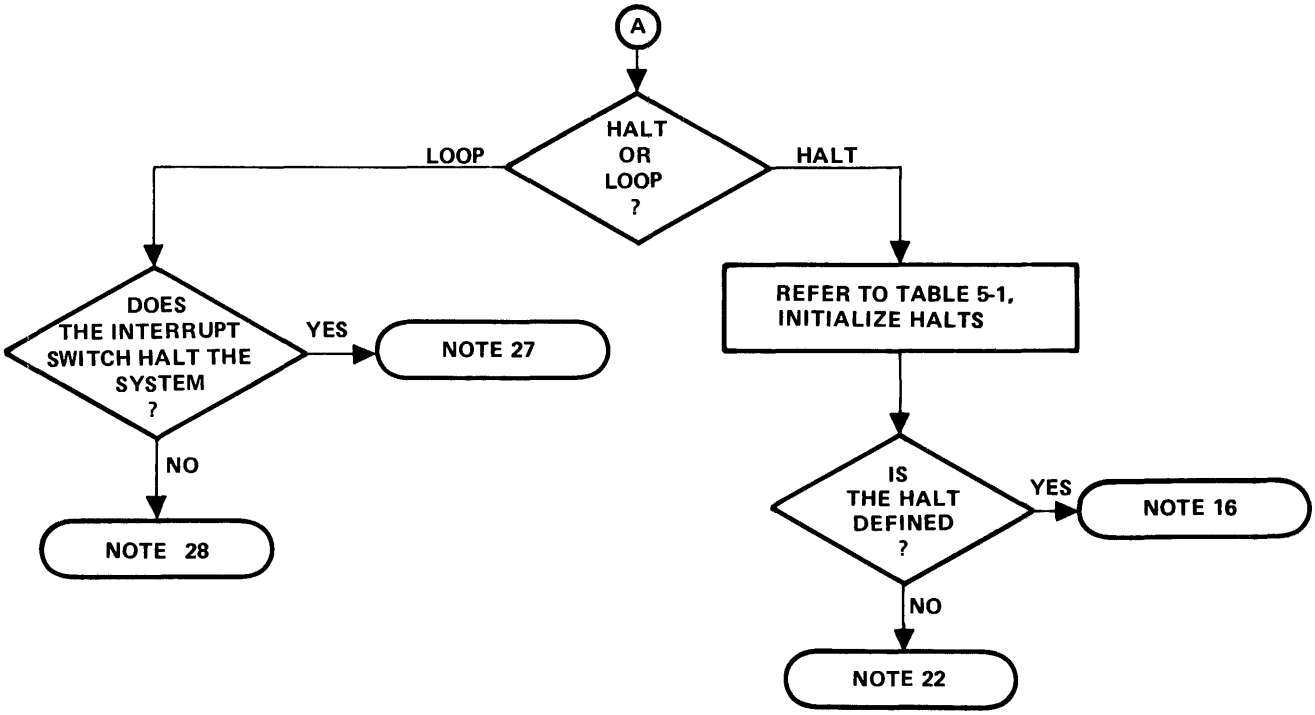


Figure 5-6. Initialize Troubleshooting Flow

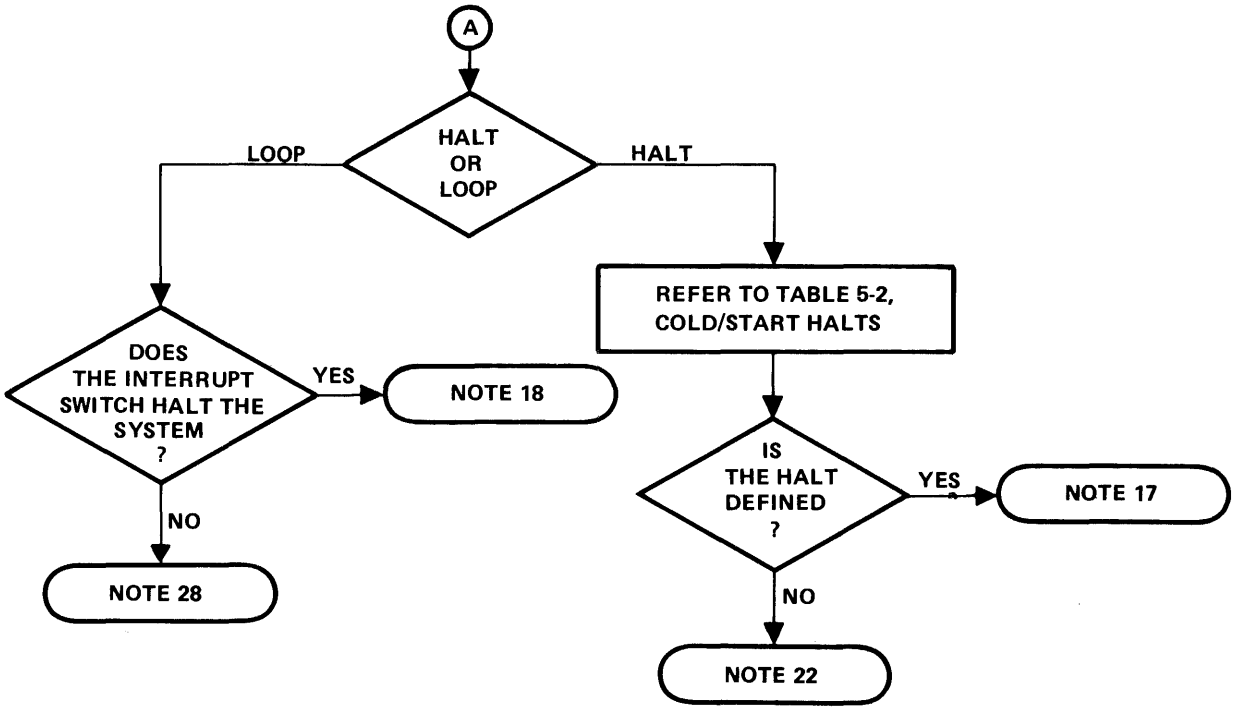


Figure 5-7. Cold/Start Troubleshooting Flow

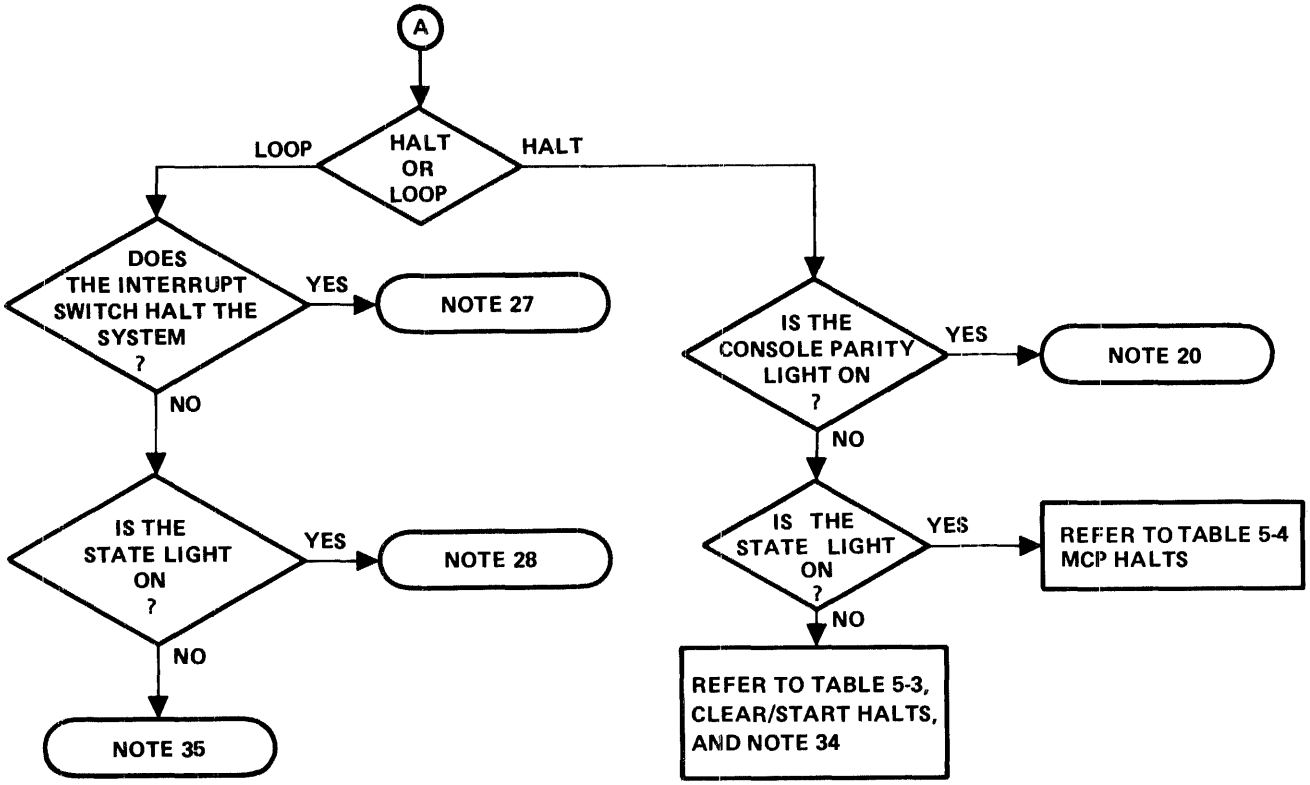


Figure 5-8. Clear/Start Troubleshooting Flow

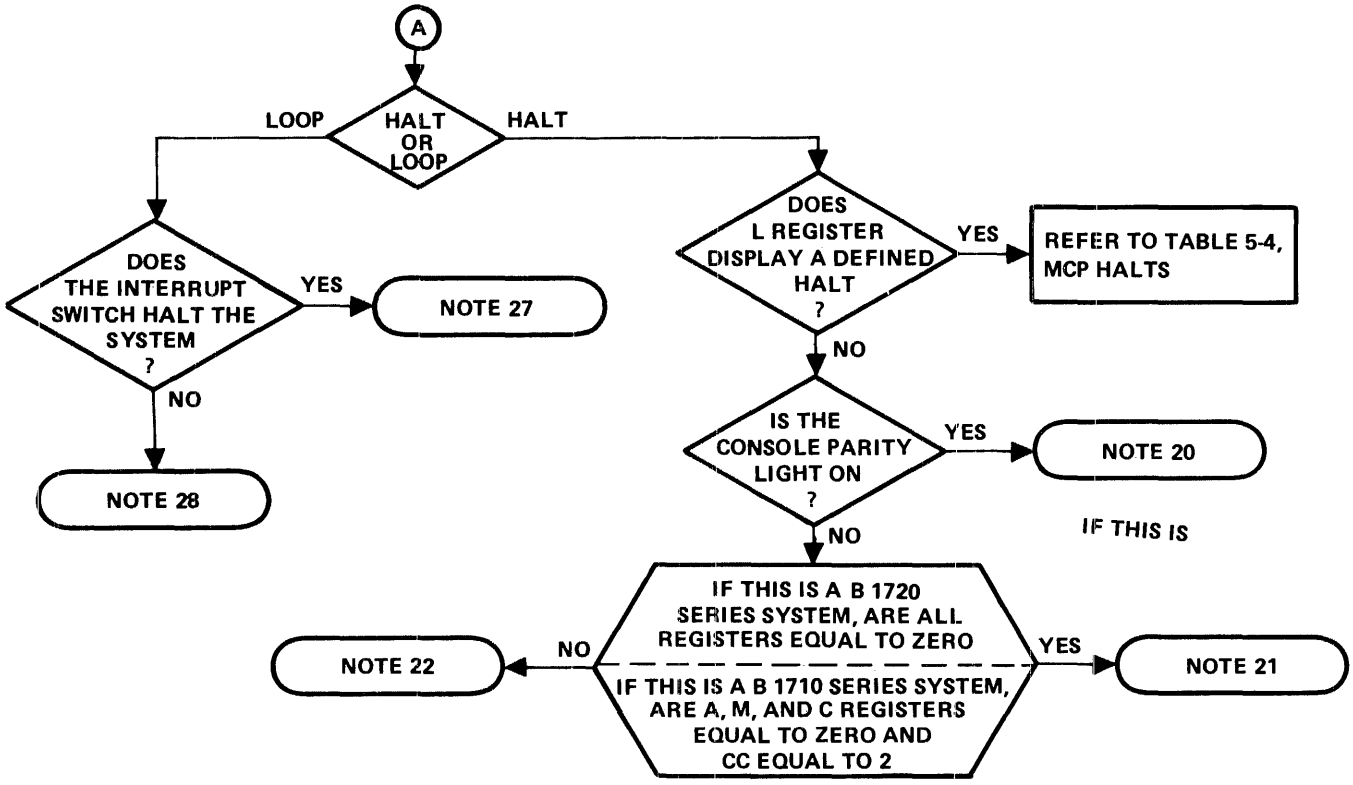


Figure 5-9. MCP Troubleshooting Flow

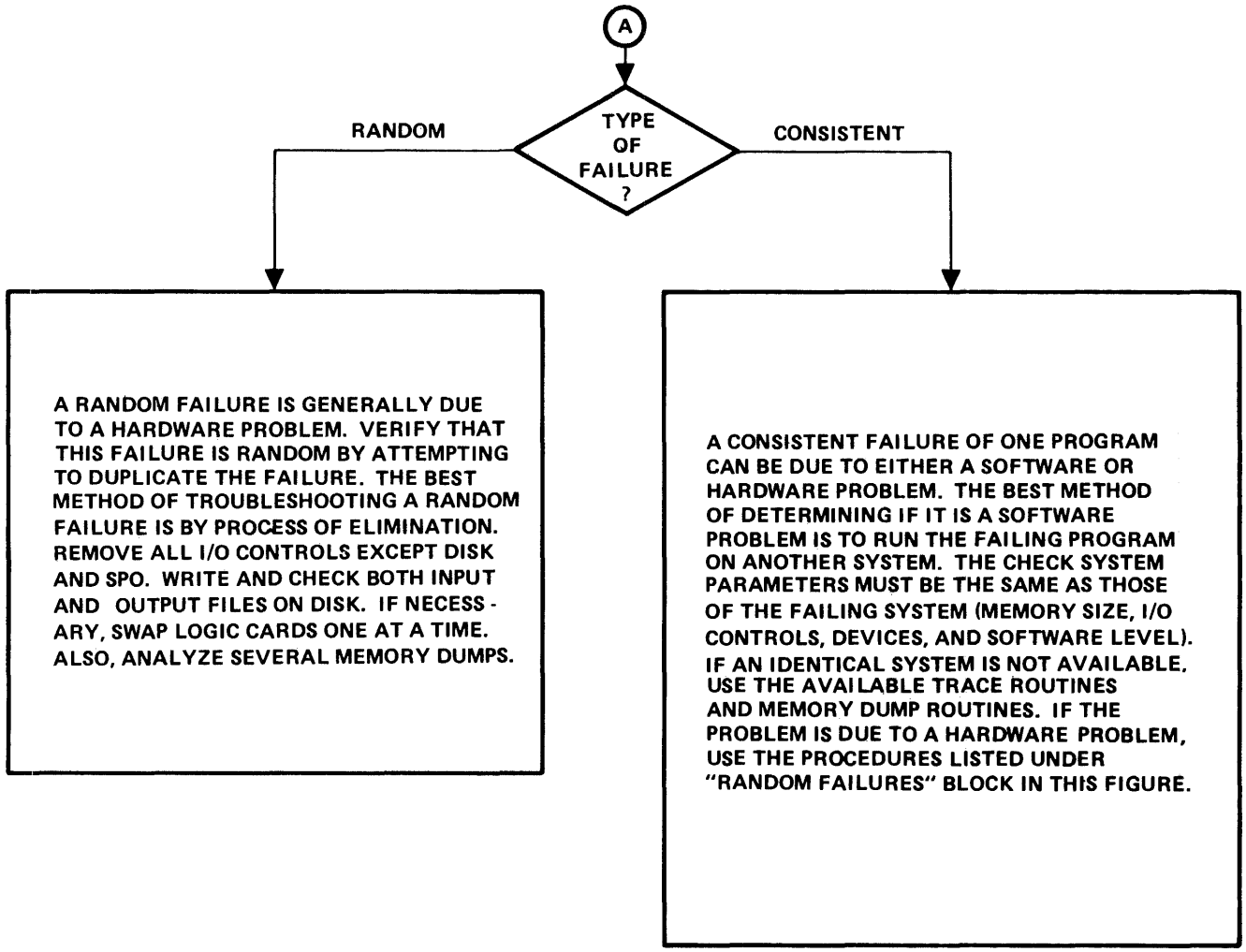


Figure 5-10 Utility/User Troubleshooting Flow

Table 5-1. Initialize Halts

L Register	T Register	Halt Condition
@000011@	@000003@	SPO Not Ready.
@000011@	@000003@	No SPO on system.

In addition to the listed Initialize halts, other halts with an accompanying message may occur. Initialize halt is indicated if the L register contains a hexadecimal 000011. Two examples of Ilitialize halts messages are DISK NOT READY and CORRECT AND HIT START.

The system can also halt due to a standard MCP halt. An MCP halt is identified if a halt occurs and the L register contains other than a hexadecimal 000011.

Table 5-2. Cold/Start Halts

L Register	T Register	Halt Condition
@000011@	@041817@	Missing port or channel.
@000011@	@000008@	SPO Not Ready.
@000011@	@000015@	No SPO on system.
@000011@	@00000F@	Directory overflow.

If the halt coding in the T register does not match any of the four listed Cold/Start halts, refer to the MCP halt table (table 5-4). If the halt is not listed in either the Cold/Start halt table or the MCP halt table, the reason for the halt is undefined.

Table 5-3. Clear/Start Halts

L-Register Value	Error Description	In-Text Note Reference
@000001@	No device on the designated I/O channel.	36
@000002@	I/O device on channel is not disk. (See T register.)	37
@000003@	Disk is not idle. (See T register for status.)	38
@000004@	Time-out while waiting for service request.	39
@000005@	Bad reference address. (X = good, Y = bad.)	40
@000006@	Bad status count after service request. (See T register.)	41
@000007@	Bad result status from I/O control. (See T Register.)	42

Table 5-3. Clear/Start Halts (Cont)

L-Register Value	Error Description	In-Text Note Reference
@000008@	Seek time-out (timed by system software).	43
@000009@	Memory parity error in I/O descriptor.	44
@00000A@	Memory parity error in I/O data.	44
@00000B@	Time-out waiting for I/O operation to complete.	45
@00000C@	Exception condition after 15 retries. (See T register.)	46
@00000D@	Exception on test I/O operation.	46
@00000E@	Designated port and channel are not assigned to disk.	47
@00000F@	No disk on system.	48
@000010@	Designated port is invalid.	47
@000011@	Designated channel is invalid.	47
@000012@	Not enough memory for this program.	49
@000013@	Memory parity after CSM overlay.	44
@000014@	Parity error somewhere in memory.	44
@000015@	NAME TABLE entry (number in T register) is zero or blank.	50
@000016@	Memory dumpfile port not equal to 7.	51
@000017@	Memory dumpfile address is equal to zero.	51
@000018@	Disk address in INITIALIZER IPB is equal to zero.	52
@000019@	MCP type contained in HINTS is zero.	52
@00001A@	Invalid stand-alone program specified.	53
@00001B@	Stand-alone SDL file not available.	53
@00001C@	No console printer on system.	54
@000080@	Segment dictionary is larger than the available main memory.	55

Table 5-3. Clear/Start Halts (Cont)

L-Register Value	Error Description	In-Text Note Reference
@000081@	LR is greater than the allowable maximum size.	56
@000083@	Need a segment of CSM that is not on disk.	57
@000084@	Wrong system software in name table.	58
@000085@	Wrong Clear/Start or Memory dump.	59
Other	Invalid.	23

Table 5-4 contains all the controlled MCP halts. If a halt occurs during the Cold/Start or the Clear/Start operation, attempt to use the applicable table before using the MCP Halts table. Use the In-Test Note Reference for additional information on MCP halts.

Table 5-4. MCP Halts

Halt Code	Description of Halt	In-Text Note Reference
@000001@	Evaluation/Program pointer stack overflow.	29
@000002@	Control stack overflow.	29
@000003@	Name/value stack overflow.	29
@000004@	Cassette data error.	30
@000005@	Invalid parameter passed to a procedure.	31
@000006@	Invalid substring.	29
@000007@	Invalid subscript.	29
@000008@	Invalid value returned from a procedure.	31
@000009@	Invalid case.	29
@00000A@	Divide by zero.	31
@00000B@	Invalid index.	31
@00000C@	Memory parity. The T register will contain the address of the parity error.	24
@00000D@	Invalid operator.	31

Table 5-4. MCP Halts (Cont)

Halt Code	Description of Halt	In-Test Note Reference
@0000010A	Console halt (INTERRUPT switch). To continue processing, turn the INTERRUPT switch to the OFF position and press START.	31
@0000011@	This is a controlled halt. The T register will contain a message from the MCP.	25
@0000012@	Attempt has been made by the program to write outside of the MCP base or limit register.	31
@0000022@	Invalid service request.	32
@0000025@	Second operation complete bit is missing from the result status field. Result descriptor is continued in the T register.	33
@0D0020@	Reference address invalid.	26
Other Codes	Invalid halt.	22

NOTE 1

Subsection 0 of section 9 is a diagnostic test of the buffer circuitry in the B 1700 DPC. By the use of special diagnostic commands, the first data buffer is loaded with data and then read back to the central processor. This subsection must be performed with more than one data pattern. A failure during this test indicates either a buffer or a DPC-to-processor interface problem. If a failure occurs, test the control boards in the B 1700 Field Card Tester. If the system is a new installation, check the wiring of the header chips as a possible cause of failure.

NOTE 2

Subsection 1 of section 9 provides a diagnostic test of the read circuitry and the first data buffer. This test uses bits 3 through 18 of the file address register as read data.

Refer to the read gate circuitry in section 2 of this manual for an explanation of how the 16-bit word is transferred into the 24-bit control buffer.

After subsection 0 is run without error, a failure of subsection 1 indicates a failure of the read logic from the central processor interface to the DPC input register. Subsection 0 of section 9 uses a set data pattern. To assure that a read problem exists and a buffer problem does not exist, run subsection 0 with several different sets of data.

NOTE 3

Subsection 2 of section 9, a diagnostic test of the write circuitry, uses all three data buffers. The buffers are loaded during STC 14, as in a normal write operation. The program then empties the buffers by the transfer of the data through the write gate logic to the interface and back to the exchange lines. However, since the data used is contained in the program, several different sets of data should be used to provide a thorough checkout of the write operation. In addition, refer to section 2 of this manual for a detailed description of the write gate logic.

NOTE 4

A valid initialize operation cannot be verified until section 1 has been executed. The DPEC completes an initialize operation, even though invalid data was written. If the clock is missing from the DPD, the DPEC will not operate. Visually check the drive to determine if the DPEC indicators are cycling and that the disk drive head positioning arm is moving. The All-Orders test routine does not move the head-positioning arm, since only one cylinder is addressed. Refer also to note 19.

NOTE 5

A failure that occurred during the running of section 1 indicates that either the data was written incorrectly on disk or a valid read problem exists. Run section 0 with the full pack option set, which allows the DPEC to control the entire operation. The single-track initialize operation performed by the All-Orders section requires the transfer of a separate address at the start of each track. If section 1 now runs (after a full-pack initialize operation), the DPC is the most probable cause of the failure. If section 1 still fails to run without errors, take the DPEC off-line and perform a full-pack initialize operatin. After the full-pack initialize operation is complete, attempt to read back the data. If the read operation fails, try reading a disk pack that is known to have valid information. This check determines if the problem occurs during a read or write operation. If the error is due to a DPEC or DPD problem, proceed to the applicable FETM for troubleshooting procedures. Refer also to the information concerning the read maintenance operator described in this section under "Read Maintenance Op Code."

NOTE

Section 1 performs multisector read and write operations. If a buffer problem is suspected in the DPC, use section 4 of the test routine to check the operation of the buffers. For additional troubleshooting procedures refer to note #7.

NOTE 6

A failure during section 3 indicates a comparison error. This error may have been detected by a Fire Code error. This test routine provides a printout of the result descriptor and the contents of the read/write buffers. Section 3 performs a partial-segment write and read operation. This section is basically a control check, since the DPC must fill the rest of a segment with zeros. In general, an error with a result descriptor including a fire-code error is a DPD problem. The only exception to this error indication are a DPEC interface problem to the DPD, or a DPEC Fire Code problem. Refer also to Note 8.

A failure consisting of incorrect data, but with the result descriptor not reflecting the error, generally is due to a problem in the DPC. Analyze the failure and determine if the failure is in the first or second data buffer. The following areas of control logic could cause this problem: the byte counter, interface logic, or the data buffers.

Run section 4 to determine if an operation using a complete sector operates without error. If section 4 fails, the problem is probably due to (1) a failure to right-justify the data within the data buffer, (2) a byte counter problem, or (3) a terminate problem. In addition, test the DPC logic cards on the Field Card Tester, and also refer to Notes 7 and 12.

NOTE 7

If section 4 fails and sections 1 and 3 do not fail, check for a problem in the multi-sector read and write operation. Section 1 can also fail if a multi-sector read or write error occurs. If sections 1 and 4 both fail, troubleshoot the problem through use of section 4. Prior to troubleshooting, determine whether the disk pack is defective. If another initialized scratch pack is not available, use the DPEC off-line to initialize another disk pack. If a control problem prevents running section 1, however, the problem could be due to valid errors on the disk pack that are not relocated.

The basic troubleshooting approach using section 4 is to determine which buffer is at fault. There are two ways to do this:

a. Run section 4 at 1-sector-per-access to increase the speed of operation. Set the beginning and ending toggles and keep the test cycling in a small section of disk. Run the test until failures develop. At the segment count where failure starts (usually 1, 2, or 3), apply this count to the buffer number.

b. Run the test, using nine segments. When a failure occurs, check to determine how many error-free segments were read before the failure occured. The number of error-free segments were read before the failure occurred. The number of error-free segments should relate to a given buffer. In addition, test the DPC control cards in the card tester. Refer to notes 5 and 6 for additional troubleshooting procedures.

NOTE 8

A failure during section 10 indicates that the Fire Code generated by the test routine does not match the Fire Code generated by the DPEC. Three probable causes for this failure are:

a. The DPEC is generating fire code improperly.

b. The control has transferred erroneous information to the processor.

c. A processor or memory problem has resulted in the test routine generating invalid code.

The best way to resolve this problem is to read a pack created on another system. If the DPEC is generating an incorrect Fire Code, the fire-code errors will occur on every read operation.

NOTE 9

Section 8 determines if the spare sectors are good, relocates data to all spare locations, and then verifies whether the relocated data is correct.

A failure of section 8 normally indicates a DPEC failures. If section 8 fails, check the DPEC off-line as follows:

a. Perform a single-track initialize to cylinder 0.

b. Verify whether the contents of the five spare sectors is correct, using the verify operation code.

c. Relocate five addresses within cylinder 0 to these spares.

d. Reverify using the verify op code. A time-out will be reported in the result descriptor.

If the DPEC off-line check does not produce an error, test the DPC control cards in the Field Card Tester.

NOTE 10

An exit from the flows to this Note indicates that a full disk pack initialize is performed without errors during off-line operation but not during on-line operation. Two possible reasons for this condition are:

a. The failure is due to an on-line read failure.

b. The op code (initialize or read) is not properly transferred to the DPEC. Run section 1 using a disk pack that was created off-line. Also, test the DPC logic cards in the Field Card Tester. The problem also could be a buffer problem. In addition, run section 4 of the diagnostic.

NOTE 11

Exiting the flows to this Note indicates a DPEC or DPD problem. Refer to the applicable FETM's for troubleshooting procedures.

NOTE 12

Failure of section 2 indicates one of the following conditions:

a. A data sensitivity problem exists in one of the DPC buffers.

NOTE

Section 2 provides logic to write the entire disk.
Section 4 provides logic to write and then read
the data before the file address is incremented.

b. An addressing problem caused by data that is overwritten.

The test routine prints the result descriptor, the read buffer contents, and the write buffer contents, if a failure occurs. A data sensitivity problem is indicated by the picking up or the dropping of bits in a character(s). For example, a 3 character becomes a 1 character if the 2 bit is dropped. If the result descriptor indicates no errors, the problem is in the DPC.

The first few characters in the segment contain the segment address. If the printout shows these address characters to be different than the desired address, an address decoding problem is indicated.

Determine also if certain bits are always dropped in the address. Since this type of problem could be in the DPC, DPEC, or DPD, card test the DPC logic cards, and run the test routine on the second disk drive to eliminate the DPD as a cause of failure.

NOTE 13

The operations performed in section 6 of the test routine are similar to the operations performed in section 3. The difference is that section 6 of the test routine moves the disk pack read/write arm. If a failure occurs during section 6 of the test routine, refer to Note 6 of this procedure. Determine also if the failure is shown in the result descriptor. If the arm movement has resulted in servo problems or mis-addressing in the DPD, the result descriptor

should indicate time-outs, address synchronization error, or address parity error. The disk drive arm may have been returning to the home position. If there are Fire Code errors in the result descriptor, a drive alignment problem may be the cause of the failure.

NOTE 14

The operations performed in section 12 of the test routine are similar to the operations performed in section 6. The difference between the operation of these two sections is that section 12 writes a segment and then checks sectors 0, 1, and 2 to determine if an overwrite occurred. If an overwrite did occur, the first few characters should contain the segment address. This problem is probably due to a DPEC address decoding error. Refer to Notes 6 and 13 for additional information.

NOTE 15

Section 13 of the test routine attempts to simulate MCP operation by the concurrent operation of two disk drives.

This test provides the capability to write and read-compare data written on two disk packs. In addition, this test initiates a seek operation on both disk drives between write operations. A failure during this test indicates a unit-select problem, an address decoding problem, or that the DPEC may have reported the "OP complete" with no transfer of data. This latter condition leaves the DPEC in a Seek status on the drive in which the error occurred.

NOTE 16

A defined halt should indicate a particular section of logic. For example, Halt 2 indicates SPO NOT READY. If, however, the halt is apparently erroneous (for example, a Halt 3 indicating NO SPO ON SYSTEM when the SPO test routine has run without error), a processor or memory problem can be suspected. Note that during an initialize operation, all software instructions and data are resident in S-memory.

NOTE 17

Determine the cause of the halt and attempt to relate it to a section of logic. For example, a halt of @D00020@ indicates a reference address problem. The T register points to the channel number.

A halt containing @000015@ in the T register indicates NO SPO ON SYSTEM. If the SPO was, in fact, on the system, this halt might have been caused by an I/O base, processor, memory, or M-string failures. In this case, the best approach is to try and duplicate this failure by means of the I/O debug test routine.

NOTE 18

The Cold/Start routine is looping while waiting for an I/O device. The Cold/Start routine uses a set discipline. This routine initiates a Test op to a disk file first, then a Test op to a disk pack, and then a Test op to a disk cartridge. This loop may be caused by a not-ready DFSU on the system during an attempt to Cold/Start a disk pack. If this condition occurs, check the status of all I/O controls and unplug all controls except those required. Refer also to notes 27 and 43.

NOTE 19

Exiting the flows to note 19 indicates that the single-track initialize failed, but a full disk pack initialize was performed without error. The difference between full disk pack initialize and single-track initialize is that with a full pack initialize the DPEC is issued only one op code. The DPEC then initializes the entire disk pack before reporting op complete. Single-track initialize initiates only one track at a time. The DPC must send the

beginning track address for each initialize operation. Therefore, the failure of both single track initialize and full disk pack initialize would usually imply a DPEC problem. The failure of single-track initialize only is probably due to a DPC or interface problem. A read absolute op code might provide the data that is written at a certain sector's address header. Refer also to notes 4, 5, 10, and 11.

NOTE 20

This indicates a parity error on the fetch of a micro-operator. If this error occurs on a B 1710 series system, check the address in A register for the failing memory location. If this error occurs on a B 1720 series system, the A register will be executing from M-memory unless the numerical value in the A register is equal to or greater than the numerical value in TOPM. If the A-register numerical value is equal to or greater than the numerical value stored in TOPM, add the numerical value in MBR to the numerical value stored in the A register to obtain an S-memory address. In addition, the erroneous byte can be found by examining the test points for memory and parity at front-plane connector $X of memory control card A.

If the memory address is out of bounds, the most probable cause of this problem is the processor, memory, or a misread from the disk.

NOTE 21

The most probable cause of this problem is power-up-clear failure. The power-up-clear term is derived from either the -2 Volt board in the Logic Power Supply 1, or the regulator board in the Logic Power Supply 2. This problem could be the result of a faulty power-up-clear circuit, a power interruption (ac), or a related power supply problem.

NOTE 22

An undefined halt can occur for any of the following reasons:

a. The execution of a valid halt micro-operator due to execution of invalid code by the MCP. This failure could be due to an error in the processor, M-string memory or S-memory. If this type of halt occurs during Clear/Start or MCP operation, the disk and I/O base should also be checked as a possible source of error.

b. The run flip-flop is inadvertently reset by dc power fluctuations or static electricity. An ungrounded stacker on a printer can cause this problem. In addition refer to note 21.

c. This type of halt could also be a special software halt used for debugging. If no other cause can be found for this halt, check with a Software representative.

NOTE 23

This halt does not decode as a Clear/Start halt. Refer to the MCP Halts table; if the halt is invalid, refer to note 22.

NOTE 24

The MCP detected the parity flag set in CD register, then read the failing address out of memory and placed it in the T register. If the parity error could not be found, the T-register contents would equal @FFFFFF@, in which case the problem could be an invalid reference address, a processor, memory, disk, or MCP problem. To troubleshoot this problem, run the system with the reference address trap and analyze several memory dumps. Also, card test the logic boards and run the system at voltage margins. Information on B 1700 voltage margins is contained in TIN 4468 Rev., dated 8/12/74.

NOTE 25

If this halt occurs, T-register will contain a message. This message is the result descriptor (in most cases) of a disk operation. If the TA register contains a value less than @C@, the value in the register is a sequence number. The meaning of this segment number varies according to the level of the MCP. Check with a software representative for a listing of sequence numbers.

NOTE 26

An invalid reference address has been detected. The channel number associated with this invalid reference address is contained in the T-register. The X-register contains the valid address, and the Y-register contains the invalid address. The reference address trap must be set to troubleshoot this problem, unless it occurred during a Cold/Start procedure. (The reference address is checked during the Cold/Start procedure.)

NOTE 27

The fact that the INTERRUPT switch halts the system indicates that the executing software is still operating correctly. In most cases the looping program indicates that the software is waiting for a response from an I/O device. To troubleshoot this problem, check the command/data functions of all I/O controls by means of a test status command. No I/O control in use should be at STC 10, except that card reader, printer, and punch card I/O controls may be at STC 10 during Test-and-Wait-for-Ready operation. In addition, an SPO I/O control may be at STC 10 in a Test-and-Wait for inquiry.

A common problem with disk cartridge is a "cylinder-not-equal" condition. This condition occurs when the disk arm is over the right cylinder but the address header has a problem associated with the cylinder bits. (The data discriminator could cause this problem.) The disk control detects a mis-match between the cylinder address in the FAR and segment header. The control exits from STC 10 and sends a seek execute command to the drive. The disk drive does not move since the read/write arm is already positioned over the proper cylinder. The software then reinitiates the operation, and the system remains locked in a loop.

The best method to check for this condition is to interrupt the system and check the status of the disk cartridge I/O control. The I/O control will probably be at STC 18. If it is not at STC 18, press the START pushbutton and try again. With the I/O control in STC 18, do a series of six transfer-ins by the use of the console switches and command/data functions. The first three transfers involve the reference address. The last three transfers involve the result descriptor. A "cylinder-not-equal" condition will provide a result descriptor containing @800000@.

A similar problem can occur on disk pack if the seek status flip-flop in the DPEC remains in the on state.

In addition, operate the system under MCP control with the reference address trap set, and analyze several memory dumps. The information contained in the dump will determine the control for which the system is waiting.

NOTE 28

The MCP has lost control of the system. The probable problem areas are processor, memory, or port interchange. If by pressing the HALT pushbutton fails to halt the processor, the machine is "locked" waiting for a micro-operator to finish executing. The micro-operator is probably a memory read or write operator. In this case, the system can be halted by forcing true the term FINISH. If this method is used the file address can be obtained. Attempt alo to duplicate the problem by using the S-memory processor and M-memory test routines.

A note 28 condition can also be caused by a disk misread during a Clear/Start operation or a tape misread during a Cold/Start operation. These conditions result in invalid MCP code. Unplug all unneeded I/O controls to eliminate interaction problems. In addition, operate the system under MCP control with the reference address trap and analyze several memory dumps. For example, place a source deck on disk and compile the job, forcing the information to be stored on the Printed Backup File. With the exception of SPO and disk controls all I/O controls should be unplugged for this operation.

NOTE 29

This halt can be due to either a software or hardware problem. To troubleshoot this error, take a memory dump. The failure of only one program could imply a software error if the halt can be duplicated. Possible hardware areas that could cause this problem are processor, M or S memory, or the disk subsystem. This type of error could also be due to destroyed information on the system disk. If the failing parameter cannot be defined, executing the program on another system, if available, may help determine the error.

NOTE 30

The B 1700 software Hamming code has detected a data error on cassette from the console reader and not the cassette I/O control. The error was not detected by the cassette logic, since the parity error flip-flop was not turned on.

NOTE 31

This halt is normally caused by a processor, M, or S memory, or a disk subsystem problem. Possibly the system disk information is destroyed. If the problem appears to be program-related, attempt to define the failure parameters and rerun the program on another system. In addition, take a memory dump to aid in defining the problem.

NOTE 32

The service request bit was set in the CC register. However, when CSM initiated a Test Service Request, no channel responded. To troubleshoot this problem, check the status of all controls using the Command-Data functions. Record any control that is in STC 11 or STC 18, and perform a test service request from the console. Any control in STC 18 or SCT 11 must have the associated service request bit true. If above procedure does not reveal the faulty control, extend and tap the control borads while the applicable test routine is executing. Repeat this procedure while operating the MCP with all I/O controls unplugged except disk and SPO.

NOTE 33

Bit 16 (the second op complete bit) is suppressed (1) by the disk controls to indicate a Seek is in progress or (2) by the disk and magnetic tape I/O controls during the pause operation.

A Single-Line I/O control will also suppress this bit during an Auto-Poll operation.

If the second op complete bit is missing at any other time, an MCP (@000025@) halt will occur. A memory dump will indicate the control and op code that are the cause of this halt. In addition, attempt to duplicate this error condition, using the applicable test routine.

NOTE 34

The Clear/Start procedure consists of:

a. Loading a bootstrap routine from the cassette tape.

b. Finding the disk control.

c. Reading the Cold/Start variables from sector 5 of the disk.

d. Reading in the system initializer from disk.

e. Reading the SDL interpreter and CSM (under direction of the system initializer.)

Up to this point (as described in steps a through e), any halts would be Clear/Start halts. From this point on, the halts would be MCP halts. When the STATE lamp is lit, the system is under MCP control. If a failure (halt or looping) occurs during the Clear/Start procedure, the leftmost 16 bits of the L register contain a code pointing to the failing section of the Clear/Start procedure. The bit coding and associated failure area for each are listed as follows:

L Register (Leftmost 16 Bits)	Program Identification (Failure Area)
@0000XX@	CSM
@000FXX@	SYSTEM/INITIALIZER
@00F0XX@	BOOTSTRAP
@0F00XX@	MEM/DUMP

NOTE 35

The Clear/Start routine has lost control of the processor. Since the Clear/Start routine checks service requests from I/O devices, the problem is not due to an I/O control locked in status count 10. (This condition could have resulted in a @00F004@ halt indicated in the L register.)

The problem is probably due to a tape cassette problem, a S-memory or M-memory problem, or a processor problem. Check to assure that the system was Cold/Started properly and retry Clear/Start using another system pack. In addition, unplug all I/O controls except disk pack and SPO controls. Refer also to Note 28.

NOTE 36

The channel allocated in Cold/Start variables has no I/O device attached. This problem occurs because:

a. The disk is being Clear/Started with a different channel number than the channel number allocated to the disk during the Cold/Start procedure, or

b. The Cold/Start variables read into memory are incorrect. This problem could be caused by a disk misread, memory error, processor or I/O base problem, or incorrect data on the system disk.

NOTE 37

The channel number read in the Cold/Start variable is not assigned to a disk control. The device code is shown in the T register. Refer to note 36 for a description of other conditions that could cause this problem.

NOTE 38

The disk control is not at status count 1. The following areas should be checked as a probable cause for this problem: I/O base, I/O clock, disk control, or another I/O control interferring with disk control operation.

NOTE 39

The disk control has not returned a service request. The control is probably locked in STC 10. This could be caused by missing clock pulses from the DPEC. Other probable reasons for this condition are listed in note 38.

NOTE 40

The disk control has returned a bad reference address. A probable cause for this error is a DPC problem, I/O base problem, interference from another I/O control, or possibly a processor or memory problem.

NOTE 41

This halt indicates the disk control is not at STC 11 or STC 18, and is requesting service. A probable cause of this problem is DPC, I/O base, another control bringing the service request true, or a processor problem involving the I/O interrupt bit.

NOTE 42

The I/O driver has detected an invalid state count from the disk control. A probable cause of this problem is the DPC, I/O base, or interference from another control.

NOTE 43

This halt indicates the disk control is locked in a loop reporting to the DCP that a seek operation is in progress. If the system is using a disk cartridge, the problem is probably due to a "cylinder-not-equal" condition. If the system is using a disk pack, a probable cause is that the seek-complete bit is continuously on. If the system is using a disk cartridge, a probable cause is a faulty address header on the cartridge. If the system is using a disk pack, it is probable that the DPEC has positioned the head to a different address than the address that was requested.

NOTE 44

This halt indicates that a memory parity error was detected. The address is not given. If no failures can be obtained by using the memory and processor test routines, the CD-3 bit can be connected to the Stop Clock logic to provide the memory address when the parity error occurs.

NOTE 45

This halt indicates a dispatch was sent to a port device (probably a multi-line control) and no response was received. To troubleshoot this problem, attempt to duplicate it by using the applicable port device test routine.

NOTE 46

A D halt indicates an exception condition on the initial test op to the system disk. The T register contains the result descriptor with the exception conditions. A C halt also indicates an exception condition. The T register contains the result descriptor, including the exception conditions. A C halt normally points at a disk or SPO error.

NOTE 47

This halt indicates that the port and channel address entered into the X-register is either invalid, or that a disk control is not connected to the port or channel.

NOTE 48

This halt indicates that the Find-Disk routine contained in the Clear/Start routine has tested all channels and cannot find a disk control connected to any of these channels.

NOTE 49

This halt indicates there is not enough memory for the Clear/Start operation.

NOTE 50

This halt indicates that the name table entry selected in the T register is blank.

NOTE 51

These halts are obtained by taking a memory dump. The memory dump routine uses the Cold/Start variables stored in S-memory. These two halts indicate that this area of S-memory does not contain the Cold/Start variables data.

NOTE 52

These two halts usually indicate that MCP information on disk is destroyed. To recover from this halt, try another system pack or cartridge. These halts could also be due to a disk control problem.

NOTE 53

Halt 1A indicates that the Stand-Alone program selected in T register at Clear/Start time is invalid. Halt 1B indicates that the selected Stand-Alone program is not available on disk. Refer also to the MCP's Name table.

NOTE 54

A 1C halt indicates the Clear/Start routine did not find a channel connected to a SPO I/O control. The Clear/Start routine has found the disk I/O control and assumes that the I/O interface is operable. The SPO I/O control should be checked as a possible cause of error.

NOTE 55

An 80 halt indicates that the disk segment dictionary contains too much information for a Clear/Start to be performed. This halt is probably an indication that the information on the disk has been destroyed. A disk misread can also cause this halt.

NOTE 56

This halt indicates that the value for MAX-S loaded into the LR register at Clear/Start time exceeds the true MAX-S value.

NOTE 57

This halt indicates that a desired segment of CSM is not available on disk. Such a halt can result when a tract is attempted using a CSM that does not contain a trace subroutine.

NOTE 58

The CSM routine is stored in the Clear/Start routine name table. The location of CSM for a B 1710 series system is at G1. The location of CSM for a B 1720 series system is at G2. This halt indicates that the CSM routine stored in the selected location is not applicable to the existing B 1700 system. This error generally is caused when an operator or field engineer has used the CM command to replace a CSM routine in the Clear/Start name table.

NOTE 59

This halt indicates that the level of the Clear/Start tape does not match the level of the MCP contained on disk.

FIELD ENGINEERING LOG

The Field Engineering Log (FE LOG) is an integral procedure within the MCP that is active whenever the MCP is executing. The FE LOG records the following types of messages:

a. Clear/Start.

b. User I/O error.

c. MCP disk error.

d. Operator.

CLEAR/START

Each Clear/Start operation is recorded in the FE LOG. The system configuration is recorded with the first Clear/Start or with the first Clear/Start after the system configuration is changed. The recorded date and time may be inaccurate, however, if they have not been reset.

USER I/O ERROR AND MCP DISK ERROR

If an exception condition exists in the result descriptor of an I/O device, the complete I/O descriptor is recorded in the FE LOG. If an MCP disk device error is not recoverable, the system halts with a @000011@ contained in the L register. If the MCP halts, however, the error is not recorded in the FE LOG, since the MCP must be executing to record errors in the FE LOG. If the MCP halts, check the MCP halt table; also check the FE LOG prior to this halt condition for indications that might provide the reason for the MCP failure.

OPERATOR MESSAGE

A 72-character (one-line) message can be recorded in the FE LOG by the use of an EM message which allows the Field Engineer to make entries into the FE LOG.

TROUBLESHOOTING PROCEDURES USING THE FE LOG

Each FE LOG entry resulting from an I/O error contains a portion of the I/O descriptor. The disk pack control I/O descriptor consists of ten 24-bit fields as shown in figure 1-2. Only the last seven fields of the disk pack control I/O descriptor are contained in the FE LOG. The seven fields are shown in figure 5-11. A description of each field and applicable troubleshooting procedures relating to these fields are contained in the following paragraphs.

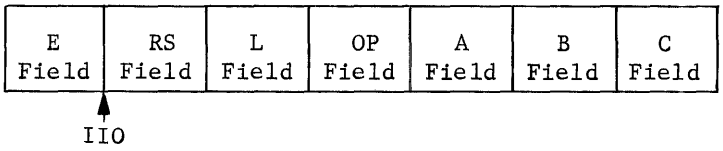


Figure 5-11. I/O Descriptor in the FE LOG

IIO ADDRESS

The IIO address (initiate I/O address) is used by the B 1700 system software. The IIO address, also referred to as the reference address, indicates the beginning location of the RS (result status) field of an I/O descriptor. The IIO (pointing to the beginning of the RS field) is shown in figure 5-11.

C FIELD

The C field contains the file address for a disk file, disk cartridge, or disk pack. The file address is the starting address of a segment on a disk device. Disk operation, however, may require more than one segment for a given operation. To determine the number of segments for any disk operation, subtract the A-field address from the B-field address and divide the remainder by 1448 (bits per segment). Any remainder from the division, must be counted as an additional segment. The CP message can be used for this computation.

To decode the C address into the DFSU-head-track for a disk file subsystem, or the cylinder-head for a disk pack subsystem, use the applicable test routine to print the address decode table. The decoding procedures for a disk cartridge are contained in the B 1700 Disk Cartridge Control I FETM, form number 1058310.

B FIELD

The B field contains the end address (plus 1) of the allocated buffer in memory.

A FIELD

The A field contains the beginning address of the allocated buffer in memory. The A and B addresses may be used for troubleshooting purposes since they define the area in memory that contains data pertinent to a given disk operation.

OP FIELD

The OP field contains the operation code (op code), variants, and unit number (spindle) that are used to determine the type of operation to be performed in the disk device. The op codes for the disk pack control are listed in table 5-5.

Table 5-5. Disk Pack Control OP Codes

OP Code	Figure Reference
Read	1-4
Write	1-5
Initialize	1-6
Relocate	1-7
Test	1-8
Stop	1-9
Search	1-10

The device type is listed in the FE LOG immediately following the time field. The device type is identifies as shown in the following examples:

Subsystem	Identifier
Disk pack subsystem	DPA
Disk cartridge subsystem	DCA
Disk file subsystem	DKA

NOTE

The letter at the end of an identifier (A as shown in the three listed subsystems) indicates a selected spindle for a disk pack or disk cartridge subsystem. However, this letter identifies a head-per-track disk file control for a disk file subsystem. If there are two disk file subsystems on a system, the first subsystem is identified as A, the second subsystem identified as B. The last four bits of the op code are used to determine the unit assigned for that particular op code.

L FIELD

The L field contains the link address. The link address points to the beginning of the RS field of the next I/O descriptor in sequence. An example of linked (chained) I/O descriptors is shown in figure 5-12.

RS FIELD

The RS (result status) field is used by the I/O Driver for two purposes: (1) to store the result descriptor from the I/O device at the completion of an operation, and (2) to store flag bits after the dispatch operation and prior to the completion of an operation.

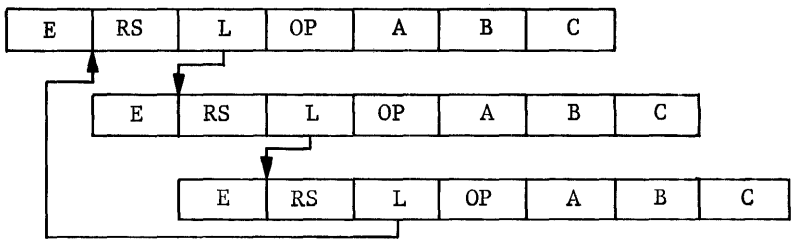


Figure 5-12. Example of a Linked List of I/O Descriptors

The FE LOG contains the result descriptor (24 bits) but not the flag bits. The flag bits are used by the software during an I/O operation to flag interrupts, channel address, and device type. The I/O driver checks the contents of the RS field periodically to determine whether the I/O descriptor is in use. If this descriptor is in use, the I/O driver uses the L-field address as an exit to initiate a new I/O descriptor.

E FIELD

The E field is used to store the actual ending address of the information in memory. Normally this address is the same as the address contained in the B field. If, however, the operation is terminated prior to the designated end of operation, the E field will contain the last-used memory address (plus 1). Premature termination is generally due to an access error or an address parity error. In some error conditions the E-field contents are equal to the B-field contents because the error (parity or Fire Code) occurred at the beginning of the operation but is not reported until the end of the operation.

TROUBLESHOOTING AIDS

The following paragraphs provide information on specific areas that can be used to aid in troubleshooting problems.

DISK PACK SUBSYSTEM FUNCTIONS

The Disk Pack Control I(DPC) provides the following functions:

a. The DPC interfaces the central processor to the DPEC.

b. The DPC provides three segments of data storage.

c. The DPC decodes the op code and provides the necessary interface logic to the DPEC.

d. The DPC assembles a 24-bit result descriptor based on 16 bits of information provided by the DPEC.

The disk pack electronics control (DPEC) provides the following functions:

a. Converts 16-bit parallel data from the DPC into serial data to the DPD. Conversely, the DPEC converts serial data from the DPD into 16-bit parallel data to the DPC.

b. Provides the logic to receive and execute op codes from the DPC.

c. Provides the logic for file address decoding.

d. Provides a 16-bit result descriptor to the DPC.

e. Provides format compatibility for the type-225 disk packs.

f. Generates bus and tag information for the disk packs.

g. Provides read and write control for the DPD's.

h. Provides logic to relocate up to five defective segments on each cylinder.

i. Detects errors and generates error codes.

j. Provides for off-line maintenance.

k. Supplies ac power for the disk pack drives.

ADDRESS DECODING

Each cylinder on a disk pack contains five spare segments that are used to relocate defective segments within that cylinder. These five spare segments are located on head 0. Head 0, therefore, contains only 55 usable addresses (segments). Heads 2 through 10 contain 60 usable addresses.

To obtain a head/cylinder location from a given file address, use the disk pack test routine variant, that points to the file address conversion chart. If this method is not possible, the following procedure can be used to ascertain a head/cylinder location from a given file address. For this example, a decimal file address of 20787 is used.

a. Divide the file address by the number of segments per cylinder (1195) to obtain a cylinder address.

```
          17.
1195 ) 20787.0
       1195

        8837
        8365
         472
```

This division provides a cylinder number of 17 and a remainder of 472.

b. Subtract 55 from the remainder to account for the 55 segments contained in head 0. If the remainder was less than 55, the location would be in head 0.

```
 472
-  55
 417
```

c. Divide the remainder achieved in step b by 60 to obtain a head number.

```
          6
      ------
60 )  417.
      360
      ---
       57
```

The head number is 6, and the remainder (57) is the segment number. However, since 55 was subtracted in step b to account for head 0, add 1 to the head number obtained in this step to provide the actual head number.

This computation indicates that the decimal file address of 20787 is located at cylinder 17, head 7, segment 57.

MCP OPERATION

The MCP provides two disk pack subsystem functions that are tested during section 13 of the disk pack test routine. These functions are overlapping seek operations, and polling.

Overlapping Seek Operations

The MCP provides a linked list of disk pack I/O descriptors. These I/O descriptors may contain several operators for each disk pack drive that is ready. If a seek operation is required for a designated DPD, the seek operation is initiated and the DPEC returns a result descriptor to the DPC indicating that a seek on the selected drive is in progress. The DPC transfers the result descriptor to the I/O driver and both the DPC and the DPEC return to the idle state. The I/O driver checks the result descriptor and, recognizing that a seek operation is in progress on this DPD, links to the next I/O descriptor in sequence. If the new I/O descriptor is designated to a different DPD and a seek operation is required, the seek is initiated and the process described previously is repeated. If the I/O descriptor is designated for the DPD that is doing a seek operation, a result descriptor is generated and both the DPEC and the DPC return to the idle state. The I/O driver will continue to sequence through the set of linked I/O descriptors, initiating seek operations and executing I/O descriptors that do not require a seek operation. After one pass through the linked list of I/O descriptors, the I/O driver will exit.

When any seek operation is complete, the service request flag is set in the DPC. The service request flag, in turn, sets the interrupt flip-flop in the central processor. The I/O driver, in response to the interrupt, reinitiates the linked list of disk pack I/O descriptors. When the address of a selected I/O descriptor equals the address of the selected DPD that has a seek complete, the seek complete flip-flop is reset and the descriptor is executed. The ability of the system to have more than one DPD performing a seek operation is called "overlapping seeks."

Polling

The I/O driver exits from the DPC after completing one pass through the linked list of I/O descriptors. The only communication link existing between the DPC and the central processor at this point is the disk pack control service request flip-flop. If this flip-flop is set true, the interrupt flip-flop in the central processor is set true. The MCP detects the interrupt and initiates the I/O driver.

The DPC generates test operators if the control is in the idle state (STC01) and the I/O driver is not transferring a I/O operator to the control.

The test operators test the status of each DPD in numerical sequence. If the seek status flip-flop is true and the arm-in-motion bit is false on the selected DPD, this indicates that the seek operation is complete. This logic is used to prevent the DCP from generating test operators and sets the service request flip-flop to false. The I/O driver responds by initiating the linked list of I/O descriptors. The I/O descriptor containing the correct file address is executed on the DPD that has completed the seek operation. When an I/O descriptor is executed, the seek status flip-flop of the selected DPD is reset. At the completion of the operation the DPC returns to the idle state and continues generating test operators.

DISABLING OVERLAPPING SEEK OPERATIONS

If the "overlapping seek" ability is disabled, the DPC and DPEC perform the seek operation and execution of one I/O operator at a time. This mode of operation may be useful as a troubleshooting aid. To disable the "overlapping seek" function connect the DPEC backplane pin AAE5 (Pin 1V of the control board) to ground.

DISABLING POLLING

If the polling function is disabled while the system is executing under MCP control, this may cause the I/O driver to ignore service requests from the disk pack subsystem.

If possible, the polling function should only be disabled during the hang-up of DPEC. The DPEC can either be hung in a loop or hung waiting for specific logic term to continue operation.

Disabling the polling function allows the Field Engineer to check test points and indicators in the DPEC that normally would not be available. The polling function changes the status of the indicators in the DPEC.

The polling function can be disabled by connecting backplane pin Xa7N (pin INX) to a true level.

READ MAINTENANCE OPERATION CODE

The read maintenance (read absolute) op code is a variant of the read operation. If the M variant of a read operator is set, the read operator becomes a read maintenance operator. This operator provides the ability to read all of the information contained in any segment on disk. The read maintenance operator is unique in that it does not require the normal address coincidence for locating a given address on disk. Instead, the decoded address is compared to the sector counter to establish the segment to be read.

The read maintenance operator does not provide synchronization with the data within a segment. Instead, the read-enable gate is turned ON at the beginning of the selected segment and turned OFF at the beginning of the next segment encountered. The read data, therefore, includes sync characters or partial sync characters, determined by when the read-enable gate is turned on. If the read data is printed in hexadecimal, the address sync code may be printed as FF, 03FC, or any other combination of 8 one-bits in succession. If a number of read maintenance operations are performed on the same segment, it is possible that one or more of the resultant printouts will contain valid sync characters at the beginning of the data. The characters that follow the sync characters are the actual characters that were written on disk.

The read maintenance operator is generally used in conjunction with either the I/O debug test routine or section 5 of the DPC test routine. The hexadecimal printout option should also be used with this option.

DISK PACK CONTROL FLOW (DETAILED)

A detailed DPC flow is shown in figure 5-13. This flow provides information on the actions that occur in the DPC during applicable status and sequence counts.

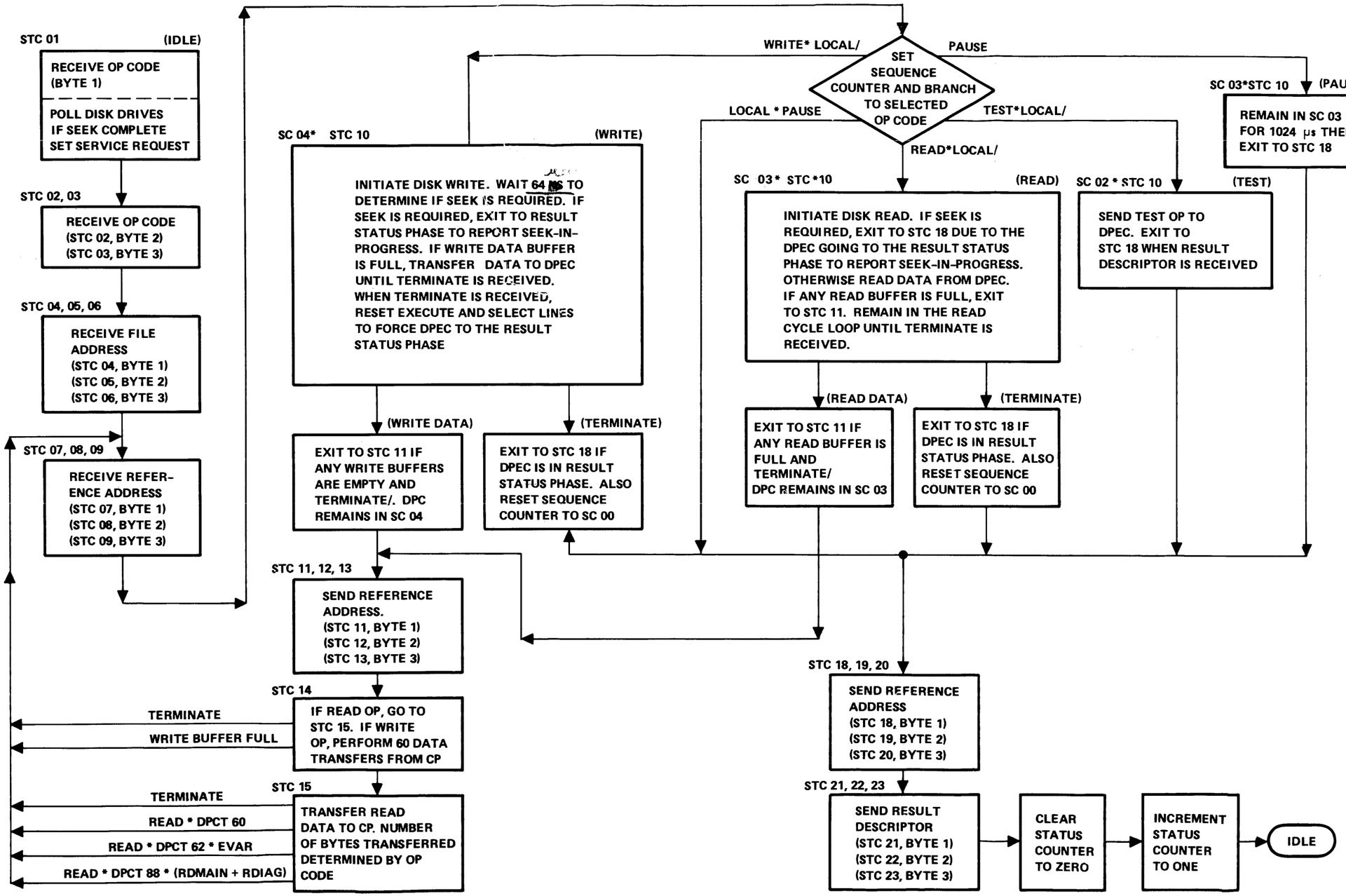


Figure 5-13. Disk Pack Control Flow (Detailed)

SECTION 6

INSTALLATION

INTRODUCTION

The successful installation of a B 1700 Disk Pack Control I is dependent on following the instructions and procedures provided in both the installation section of this manual and the Field Test and Reference (FT&R) documentation package supplied with the control, the B 1700 system or both. Since the installation section of this manual contains generalized information applicable to all B 1700 systems, pertinent data and instructions for a specific B 1700 system must be obtained from the accompanying FT&R package.

B 1700 DISK PACK CONTROL I

The DPC consists of three B 1700-size logic cards mounted in an independent four-card backplane as shown in figure 6-1.

The four-card backplane is mounted in the B 1700 card chassis. Use the following procedure to install a disk pack control in a B 1700 system:

a. Power down the B 1700 mainframe.

b. Install the four-card independent backplane in the B 1700 card chassis, using eight mounting screws (four on the top, four on the bottom).

c. Install the three DPD cards in the backplane as shown in figure 6-1.

d. Install a coaxial clock cable from one of the six available clock positions located on the I/O distribution card to the clock receptacle located on the high-speed buffer card in card location. 1.

e. Connect the two I/O ribbon cables to the high-speed buffer card in card location 1 as follows:

   1. If the ribbon cables are from the I/O distribution card, connect from distribution card $Y to high-speed buffer card $X; and from distribution card #Y to high-speed buffer card $Y.

   2. If the ribbon cables are from another I/O control, connect from previous control #X to high-speed buffer card $X and from previous control #Y to high-speed buffer card $Y.

   3. If the DPC is not the last control in the I/O distribution chain, connect from the high-speed buffer card $X the next control $X and from the high-speed buffer card #Y to the next control $Y.

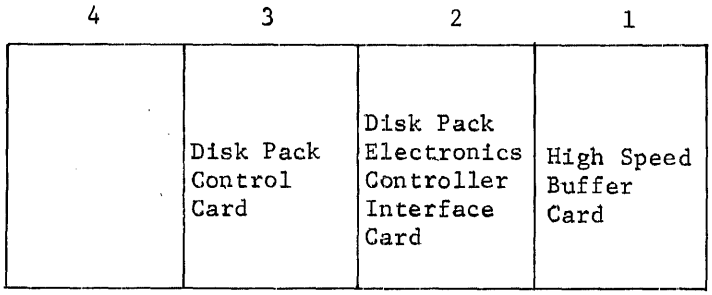


Figure 6-1. Disk Pack Control Backplane (Card Insertion View)

4. If the DPC is the last control in the I/O distribution chain, termination resistors must be installed in the control.

f. Install the DPC interface cable from the DPEC card, location #Y to the I/O interface plate. The interface cable from the DPEC connects to the DPC. The interface cable connector is mounted on the I/O interface plate.

JUMPER CHIP STRAPPING

The jumper chips that require strapping are as follows:

a. Channel designate jumper chip.

b. Card test jumper chips.

c. Exchange jumper chip.

d. Number-of-units-present jumper chip.

e. Appropriate-unit-type jumper chip.

CHANNEL DESIGNATE JUMPER CHIP

The channel designate jumper chip is located at C9 on the DPC card (card location 3). Available channels are 8 through 14 (channel 15 is reserved for parity error notification). To achieve inter-system disk pack compatibility, however, the disk pack channel designate on all applicable systems must be the same number. It is strongly recommended, therefore, that all B 1700 disk pack subsystems be assigned channel designate number 8. The channel designate jumper configurations are shown in figure 6-2.

CARD TEST JUMPER CHIPS

The card test jumper chips are used to allow testing of some of the internal card circuitry that otherwise would not be completely tested. The card test jumper chips for the DPC card are located at C1, D6, E5 and G3. Detailed instructions for the wiring and placement of these jumper chips are contained in FT&R documentation.

The card test jumper chips for the DPEC interface card (EC interface card) are located at C2, G3, H0, E1, and A9. Some of these jumper chips are used for logic wiring that is not part of the card testing logic. Refer to the FT&R documentation for detailed information on the configuration of these jumper chips.

EXCHANGE JUMPER CHIP

The exchange jumper chip is located at H5 on the DPC card. Since currently there is no disk pack exchange available (future expansion), the chip must be disconnected to reflect a "no exchange" condition.

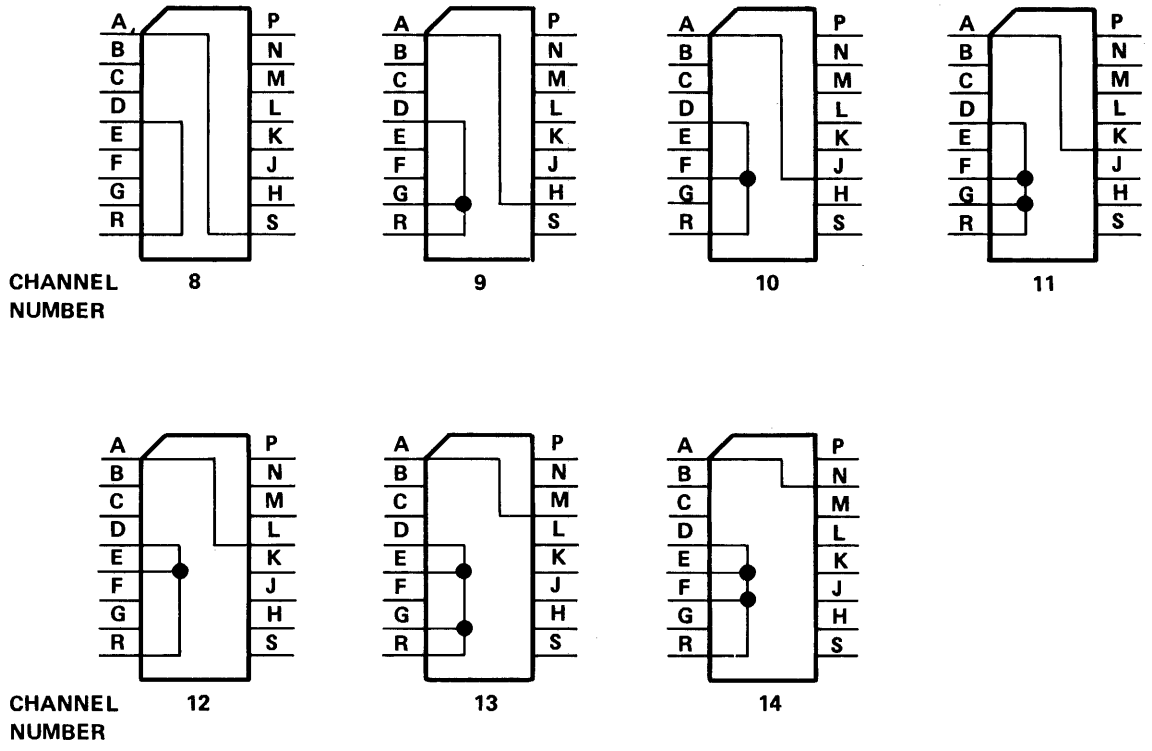


Figure 6-2. Disk Pack Control Channel Designate Configuration

NUMBER-OF-UNITS-PRESENT JUMPER CHIP

The number-of-units-present jumper chip is located at E8 on the DPC card. This jumper chip is wired to reflect the number of spindles (two spindles possible in each drive unit). There are two possible jumper configurations: one reflects 1 through 4 spindles; the other reflects 5 through 8 spindles. For example, if a disk pack subsystem contained three DPD units (two spindles per unit), the number-of-units-present jumper chip should be jumpered to provide the "5 through 8 spindles" configuration. The jumber-of-units-present jumper chip configurations are shown in figure 6-3.

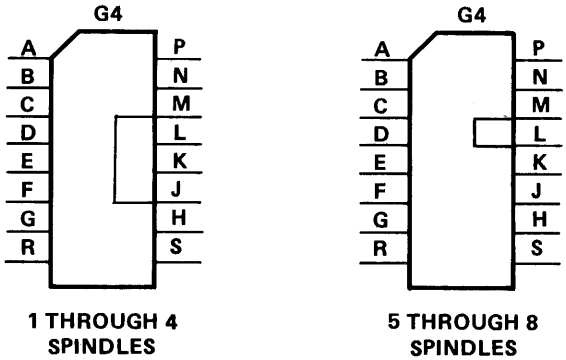


Figure 6-3. Number-Of-Units-Present Jumper Chip Configurations

APPROPRIATE-UNIT-TYPE JUMPER CHIP

The appropriate-unit-type jumper chip located at G4 of the DPC card (same chip as the number-of-units-present chip) is used in the result descriptor for a test operator This chip is configured to reflect the types of disk pack drive units (type 215 or type 225) in the disk-pack subsystem. The "type 225 and type 215" labeling on the FT&R documentation is misleading. The "type-225" disk pack drive contains the same storage capacity and provides the same bit density as the type-225 disk pack drive; that is, 406 cylinders and 4400 BPI. Both disk pack drive units use the B 9974-4 Disk Pack. The disk pack that is used on a type-disk 225 disk pack drive is also called a full-capacity disk pack.

The "type-215" disk pack drive provides the same bit density but only one-half the capacity of the type-225 disk pack drive; that is, 203 cylinders and 4400 BPI. The disk pack used on a "type-215" disk pack drive is also called a half-capacity disk pack.

The appropriate-unit-type jumper chip configurations are shown in figure 6-4.

NOTE

Chip G4 is configured to reflect the first and second disk pack drive units (spindles 0 through 3) as type-215 drives, the fourth disk pack drive unit (spindles 6 and 7) as type-225 drive, and the third disk pack drive unit (spindles 4 and 5) not present.

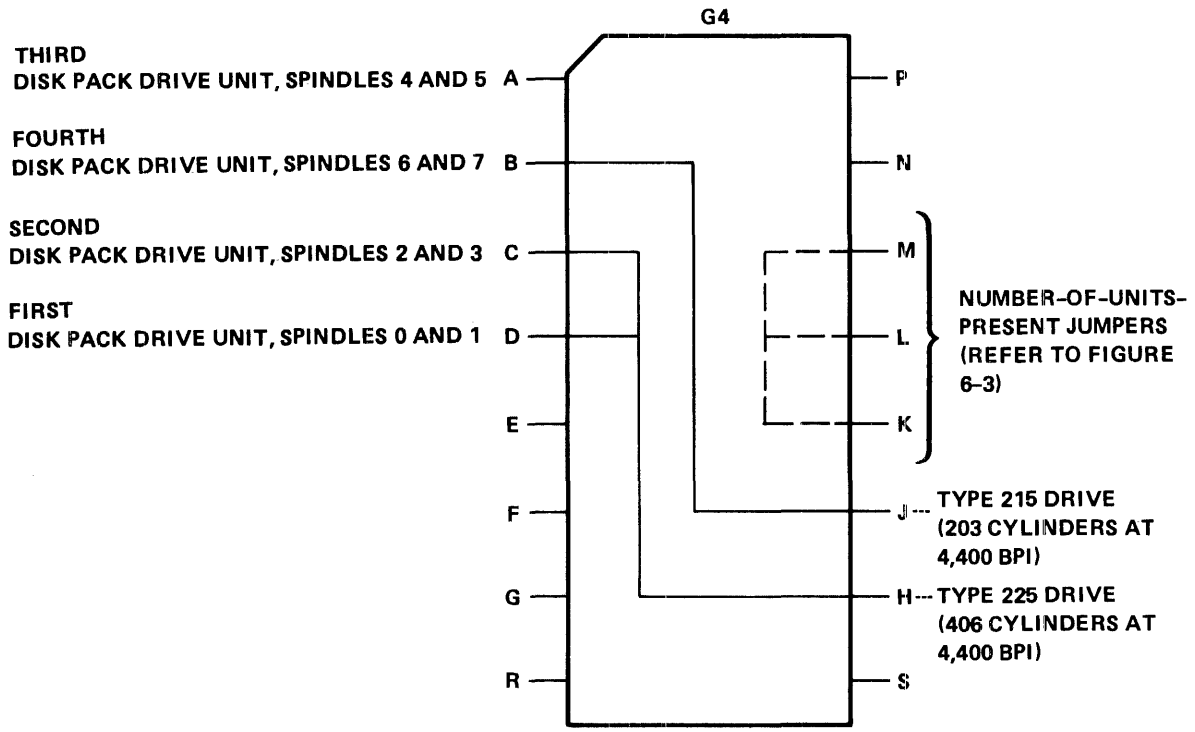


Figure 6-4. Appropriate-Unit-Type Jumper Chip Configuration

CLOCK SKEW ADJUSTMENT PROCEDURE

The SCPM...0 clock located at pin OWX of the DPC backplane must be within ±5 nanoseconds, from the SCPM...0 clock located at pin OWX on the I/O base distribution card.

Adjustment of the clock skew is accomplished by selecting the proper tap of the DL2N chip located at G9 of the high-speed buffer card in the DPC backplane. The DL2N is a 20-nanosecond delay line containing 10 two-nanosecond incremented tap positions. The sequential delays are listed in the table below.

Pin	Amount Of Delay In Nanoseconds From Input (SCPS....)
H	2
F	4
J	6
E	8
K	10
L	12
C	14
M	16
B	18
N	20

Normally the tape (installed in manufacturing) is connected to pin K as shown in figure 6-5. If the SCPM...0 at the DPC is earlier than the SCPM...0 at the I/O distribution card, move the tap from pin K to one of the larger delays (L, C, M, B, or N). If the SCPM...0 at the DPC is delayed more than 5 nanoseconds from the SCPM...0 at the I/O distribution card, move the tape from pin K to one of the smaller delays (E, J, F, or H). Although the allowable range ±5 is nanoseconds, the most reliable results will be achieved if the clock delay is set as close as possible to SCPM...0.

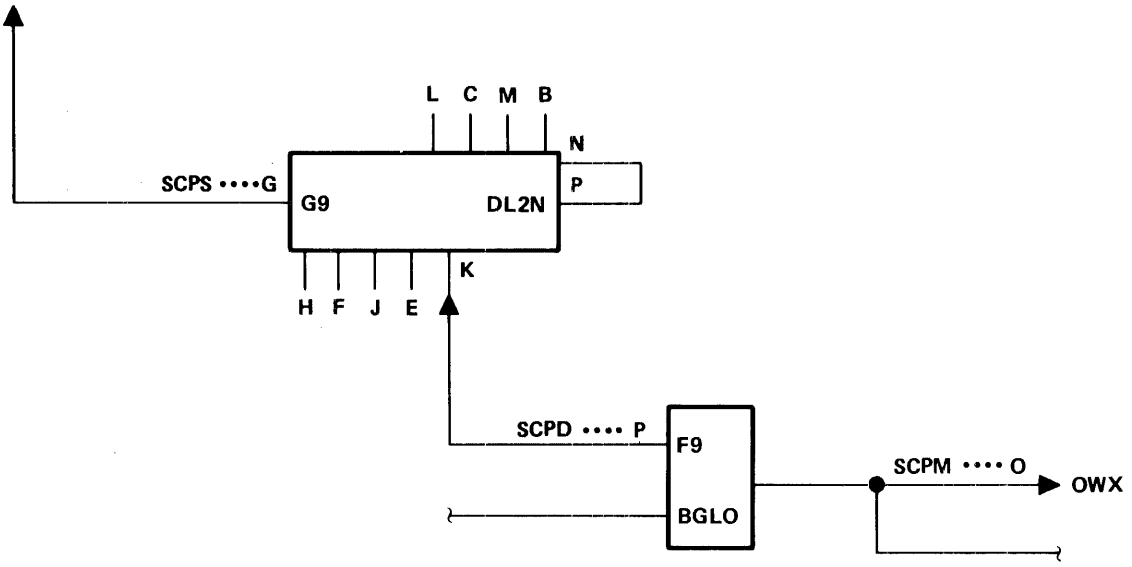


Figure 6-5. Disk Pack Control Clock Skew Circuitry

12 bit Register — 8-bit register — 6 bit latch.

BIT POSITION	CARRY	19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	−1 −2	STATE
					0
					0
					0
			0 0 1 1 0		1
					1
		4 1 7	D C	6	1
A INPUT		0 0 1 0 0 0 1 1 1 1 1 1 0 1 1 1 1 0 0 0 1 1 0		X	2
B INPUT		1 1 0 0 1 0 0 0 0 0 1 1 0			2
Sum	0	1 1 1 0 1 1 0 0 0 1 0 0			2
		0 1 0 0 0 1 1 1 1 1 1 0 1 1 1 1 0 0 0 1 1 0		X 0	3
		1 1 0 0 1 0 0 0 0 0 1 1 0			3
X = don't care	1	0 0 0 1 0 0 0 0 0 0 0 1 1			3
		0 0 1 0 0 0 0 0 0 0 1 1 1 1 1 0 0 0 1 1 0		X 0 1	4
		1 1 0 0 1 0 0 0 0 0 1 1 0			4
	0	1 1 1 0 1 0 0 0 1 1 0 1			4
		0 1 0 0 0 0 0 0 1 1 1 1 0 0 0 1 1 0		X 0 1 0	5
		1 1 0 0 1 0 0 0 0 0 1 1 0			5
	1	0 0 0 0 1 0 0 1 0 1 0 1			5
		0 0 0 1 0 0 1 0 1 0 1 0 0 0 1 1 0		X 0 1 0 1	6
		1 1 0 0 1 0 0 0 0 0 1 1 0			6
	0	1 1 0 1 1 0 1 1 0 0 1 0			6
		0 0 1 0 0 1 0 1 0 1 0 0 0 1 1 0		X 0 1 0 1 0	7
		1 1 0 0 1 0 0 0 0 0 1 1 0			7
	0	1 1 1 0 1 1 0 1 1 0 1 0			7
		0 1 0 0 1 0 1 0 1 0 0 0 1 1 0		X 0 1 0 1 0 0	8
		1 1 0 0 1 0 0 0 0 0 1 1 0			8
	1	0 0 0 1 0 0 1 0 1 1 1 0			8
		0 0 1 0 0 1 0 1 1 1 0 1 1 0		X 0 1 0 1 0 0 1	9
		1 1 0 0 1 0 0 0 0 0 1 1 0			9
	0	1 1 1 0 1 1 1 0 0 0 1 1			9
		0 1 0 0 1 0 1 1 1 0 1 1 0		X 0 1 0 1 0 0 1 0	10
		1 1 0 0 1 0 0 0 0 0 1 1 0			10
	1	0 0 0 1 0 1 0 0 0 0 0 1			10
		0 0 1 0 1 0 0 0 0 0 1 0		X 0 1 0 1 0 0 1 0 1	11
		1 1 0 0 1 0 0 0 0 0 1 1 0			11
	0	1 1 1 1 0 0 0 0 1 0 0 0			11
		0 1 0 1 0 0 0 0 0 1 0 X 0 1 0 1 0 0 1 0 1 0			12
		1 1 0 0 1 0 0 0 0 0 1 1 0			12
	1	0 0 0 1 1 0 0 0 1 0 1 0			12
		0 0 1 1 0 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 1			13
		1 0 1 0 0 1 1 0 0 0 0 0			13
	0	1 1 0 1 0 1 1 1 0 1 0 0			13
		0 1 1 0 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 1 0			14
		1 0 1 0 0 1 1 0 0 0 0 0			14
	1	0 0 0 0 1 0 0 0 1 0 0 1			14
		0 0 0 1 0 0 0 1 0 0 1 0 1 0 0 1 0 1 0 1 0 1			15
		1 0 1 0 0 1 1 0 0 0 0 0			15
	0	1 0 1 1 0 1 1 1 0 0 1 0			15
		0 0 1 0 0 0 1 0 1 0 0 1 0 1 0 1	0 1 0	1 0	0
		SECTOR	CYLINDER	HEAD	

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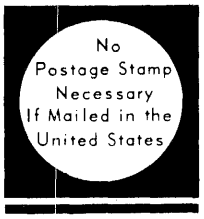

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