CADLINC

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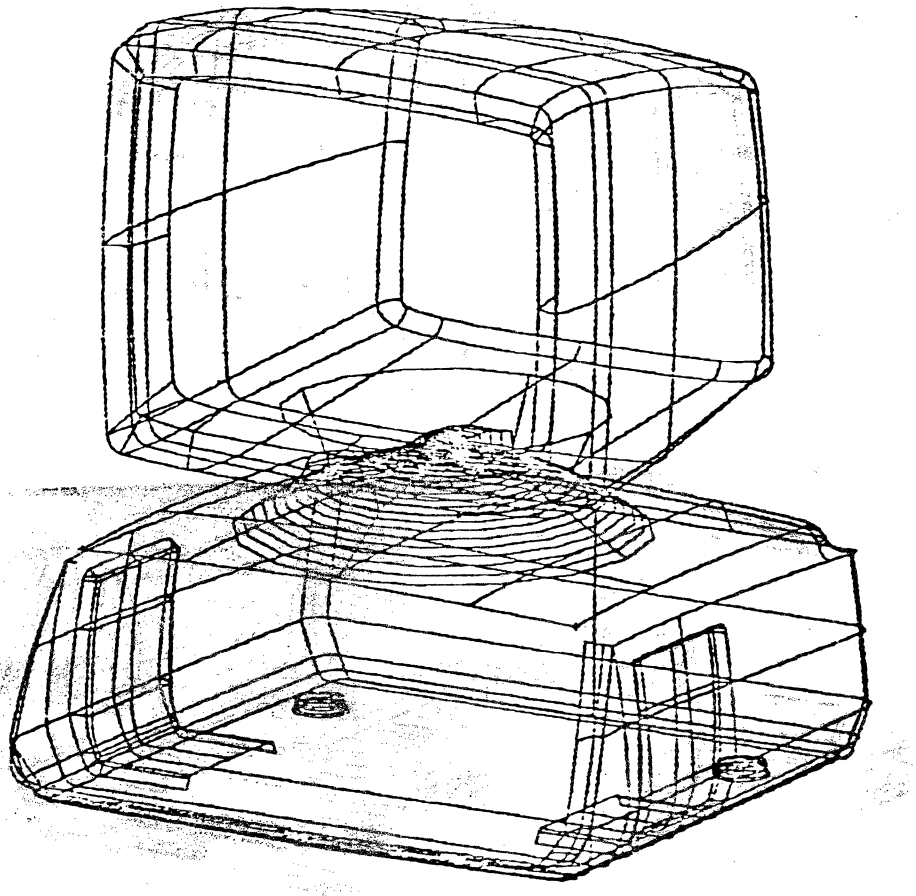

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312/693-6700

CADLINC INC.

Processor Specifications

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1. Introduction

The CADLINC Series 80A Processor board consists of a Motorola 68000 central processing unit, RAM and PROM memory, some I/O facilities, a local HIGHSPEED memory bus and an IEEE-796 MULTIBUS * interface. Onboard memory consists of 4 JEDEC style byte-wide PROM sockets, and 256K bytes of dynamic RAM. The I/O facilities are two serial communications ports, a 16-bit bidirectional port and a 5 channel programmable timer.

The Series 80A Processor can be used as a standalone system with only a power supply, backplane and serial terminal, or as part of a fully integrated computer system that can include the CADLINC GRAPHICS CONTROLLER, ETHERNET board, MULTIFUNCTION board, DUAL PORT MEMORY boards, FLOATING POINT Processor board, INTELLIGENT SERIAL CONTROLLER board and many other MULTIBUS compatible peripherals.

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* MULTIBUS is a trademark of Intel Corp.

2. Overview of Operation

2.1. Central Processing Unit (CPU)

The Motorola 68000 has a 16-bit data bus and a 23-bit address bus. The internal registers are 32-bits in length. It has 8 data and 7 address registers, 2 stack pointers, a program counter, plus a 16-bit status word. Operations on data may be byte (8), word (16), or long word (32 bits). Operations on addresses may be of word or long word length. All registers may be used as indexes. The 68000 has 2 states of operation: Supervisor and User for enhanced system integrity and security.

2.2. Memory

Onboard PROM consists of 4 JEDEC style PROM sockets that can accept 2732, 2764, 27128 or 27256 type ROMs (total capacity of 16K, 32K, 64K or 128K bytes respectively).

Onboard RAM consists of 36 64K x 1 dynamic rams giving a capacity of 256K bytes with parity. RAM refreshing is done by a PROM monitor routine that executes 128 NOP instructions every 2 milliseconds. The programmable timer generates the Non-Maskable- Interrupt.

2.3. Buses

The CADLINC Series 80A Processor has 3 bus structures. The first is the internal synchronous bus for System accessed I/O and Memory Management; the second is a proprietary synchronous HIGHSPEED BUS on the Auxiliary MULTIBUS connector for expanded DUAL PORT MEMORY, FLOATING POINT and ENHANCED SERIAL Processor boards; and the third is the MULTIBUS for expanded off-the-shelf peripherals, i.e. Disc controllers, ETHERNET, GRAPHICS CONTROLLER, etc. System I/O devices and onboard RAM do not require the use of the MULTIBUS.

Advantages are:

1. Onboard memory accesses are faster than the Multibus.

2. The MULTIBUS is then available for use by other bus masters without having to contend for priority very often.

3. DUAL PORT MEMORY responds as fast as onboard RAM and is immediately available to other bus masters.

The System I/O devices, onboard PROM and 256K bytes of Local RAM are not accessible to other bus masters.

2.4. Input - Output Devices

The Series 80A Processor board has a dual channel UART chip, 5 programmable timers, and a 16-bit bidirectional port for general purpose use. One of the UART's channels is configured to communicate with a terminal or CADLINC keyboard depending on the PROM monitor supplied. The other channel can be jumpered with another computer or a second terminal. The line drivers and receivers are RS-423 compatible and the connector pinouts are RS-232-C configuration. Two of the five 16-bit counter/timers are dedicated baud-rate generators for the UART chip, one timer channel for each serial channel. One timer is dedicated to generate a 2-millisecond interrupt to refresh dynamic RAM. One of the two remaining timers is available for user applications. The other acts as a "Watchdog" timer to automatically reset the system if the PROM monitor program has lost control. The 16-bit bidirectional port is designed for reading options selections from a bank of switches and to write status information to a static display.

2.5. Interrupts

The 68000 has seven interrupt levels and a current interrupt level mask. An interrupt will be processed if its level is greater than the current mask. Level 7, the highest priority, is Non-Maskable and will always interrupt any task. This level is reserved for the dynamic RAM refresh routine.

The standard MULTIBUS configuration defines interrupt levels INT0 to INT7, with INT0 being the highest priority. The CADLINC Series 80A Processor defines priorities according to the Motorola conventions with INT7 as the highest. INT0, then, is not implemented and INT1 is the lowest priority.

Preassigned interrupts on the CADLINC Series 80A Processor are as follows:

INT7: Refresh timer (Non-Maskable)
INT6: User programmable timer
INT5: UART generated interrupts

Interrupts are processed by the 68000 in "Auto-Vector" mode only. Transfer vectors are supplied from an internal table, so the interrupting device need not supply a vector.

2.6. Boot State

At power-on or whenever a hardware reset is done, the Processor enters Boot State. In Boot State, the first onboard PROM pair overlays RAM starting at location 0. All reads then come from PROM, but writes can go to RAM. This enables the 68000 to fetch its initial program counter and system stack pointer from PROM locations 0-3. RAM, then, may also be initialized. All interrupts, including the Non-Maskable INT7, are disabled by hardware. When Boot State is exited, Non-Maskable interrupt is enabled, but maskable interrupts will depend on the current mask level.

Boot State is terminated by one write to the System Access location CLEARBOOT. See Device addresses.

2.7. Memory Management

The Memory Management system has been designed to support a multi-tasking operating system. The concept, in short, is that of translating, or mapping, Processor address bits A12-A21 (or A22) into physical address bits MA12-MA23, along with Protection, Address Space Allocation and Page Control information about each Page.

All accesses to local RAM and to MULTIBUS memory and I/O are translated and protected in the same manner.

Managed Address access is initiated by Processor address bit A23. When it is 'on', Memory Management is disabled and indicates a System Access is to be performed. When it is 'off', then the Processor addresses A12-A21 (or A22) combine with pre-programmed Context bits to form a pointer into a 4K x 20 bit Array. The output of this Array contains the 12-bit Mapped physical address and 8 Protection and allocation bits. The 12 Managed Addresses combine with the lower 11 Processor addresses to form the 23-bit physical address, giving a full 16M bytes of physical space.

There are two modes of combining Context bits with Processor addresses: One with 1 Context bit, hence 2 levels of Context; the other with 2 Context bits having 4 levels of Context. In the first mode, Context bit CX0 combines with Processor address bits A22 and A21 as the most significant bits into the Array. In the second, Context bits CX1, CX0 and Processor address A21 are the most significant. Hence, the first mode yields 2 Contexts of 8M bytes each and the second yields 4 Contexts of 4M bytes each.

Context bits CX0 and CX1 are accessable via a System Access location. See Device Addresses.

During a System Access, hardware automatically swaps the upper Processor address and Context bit(s) with lower Processor address bits A2-A13. This allows a program in Supervisor state to access every Context by manipulation of A12 and A13 during a read or write to the System Access Map location.

3. Theory Of Operation

3.1. Introduction

The Processor divides up its 16 Mbytes of address space into two 8 Mbyte regions: System Space and Managed Space. System space comprises the on-board PROMs, Timer, Uart, Parallel Port and Memory Management registers. Managed space consists of Local Memory, the Highspeed bus and Multibus accesses.

Managed space is divided into 2 (or 4) Contexts, each capable of containing processes as large as 8 Mbytes (or 4 Mbytes) in physical memory. The Memory Management Unit contains 4096 entries that filter Virtual Processor addresses into Physical addresses and supports the full 16 Mbytes of physical space.

3.2. Control Logic

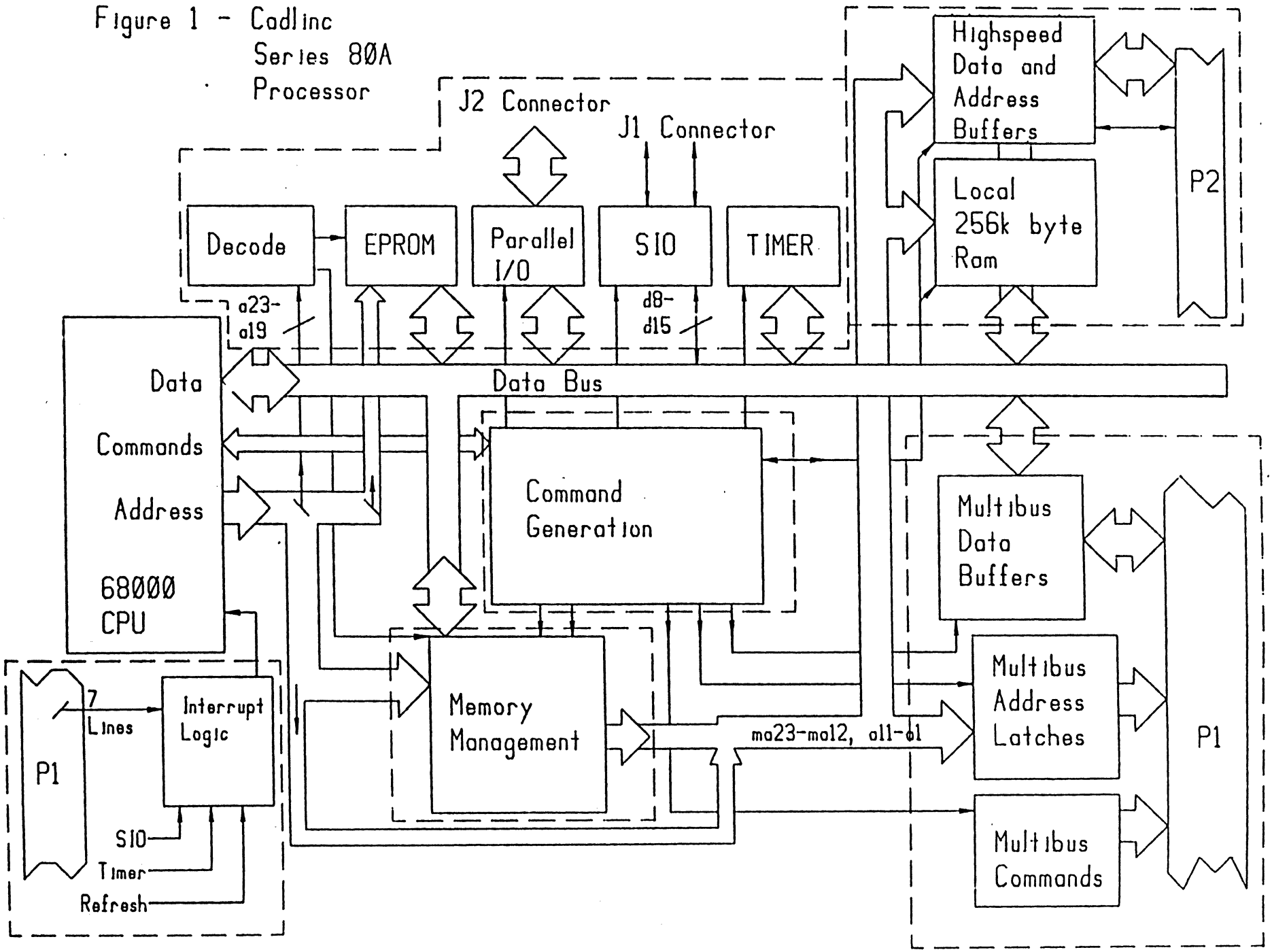
See schematic drawings #SD295014
See Appendices F and G for firmware codes.
See Figure 1 Control Block Diagram

The Series 80A Processor board makes extensive use of Programmable Array Logic I.C.s to perform necessary command timing and direction control. Figure 1 is an overall block diagram that shows the flow of input control and output command signals.

The following State Tables and Timing Diagrams describe in general the actions of the control logic. Refer to the PAL equations in Appendix G.

After leaving Boot State, the control logic decides what Space a virtual address will attempt to access on every 68000 cycle by the main Address Strobe (as-) and the level of address bit a23. If a23 is high, a System Access is requested and, if the 68000 is in supervisor state, then On-board devices, Memory Management ram and Boot clear accesses are allowed. If a23 is low, then some Managed Access is requested and different logic is enabled based on the state of Page Control bits (Bus ! Local: b/l-, and I/O ! Memory: io/m-). They are stored in the Memory Management Ram along with each page of the translated Virtual to Physical addresses.

Figure 1 - Codlinc
Series 80A
Processor



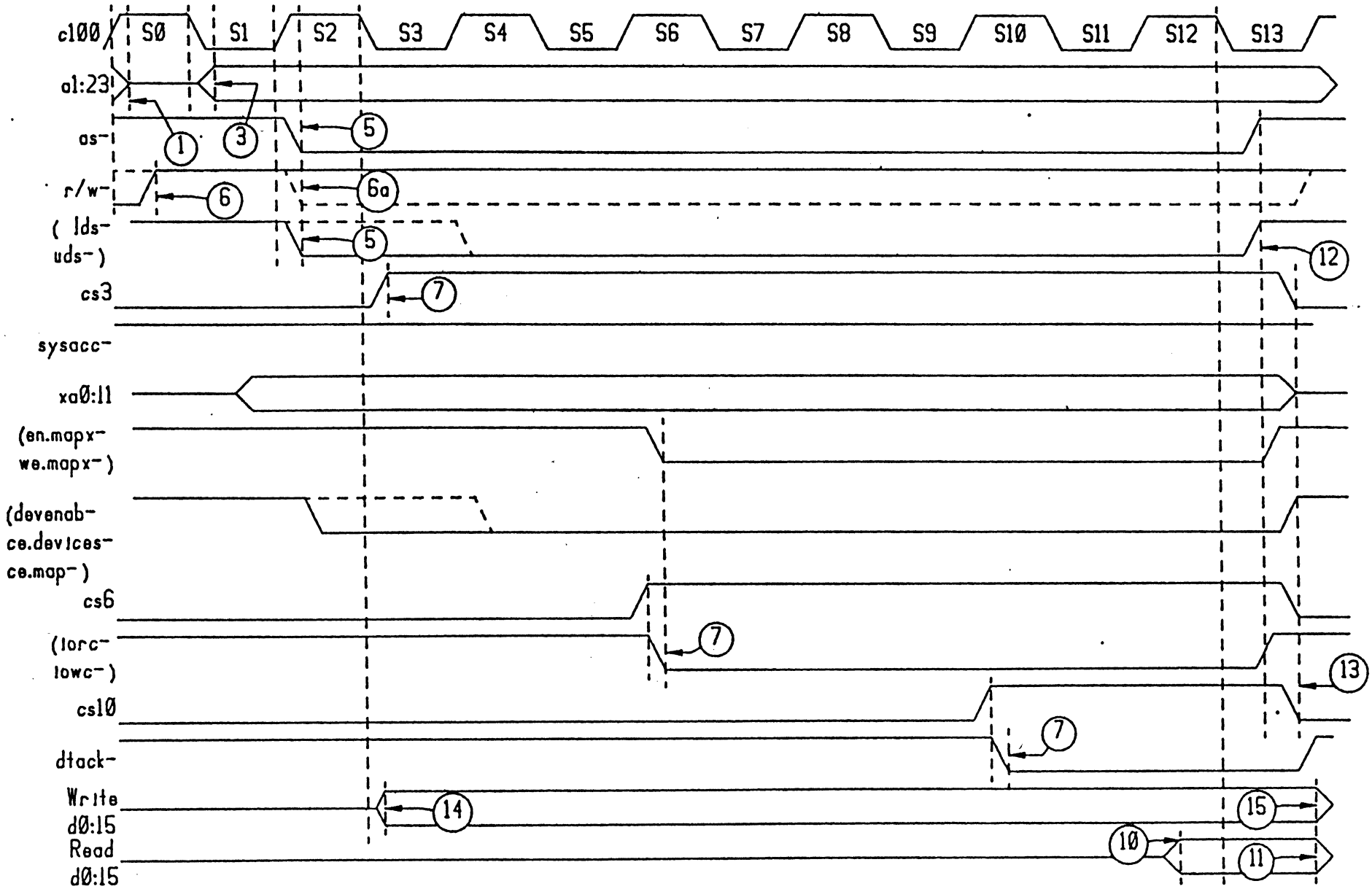


Figure 2 System Space Access Timing

State	Description (See Figure 2)
State 0.	Processor addresses a1 thru a23 are negated (#1). r/w- is asserted to a Read (#6) at the end of every cycle.
State 1.	Processor addreses a1 thru a23 are asserted (#3). a23 is high indicating a System access request. System device address decodes.
State 2.	Processor strobes (as- for all cycles, lds:uds- for read cycles) become valid (#5). sysacc is asserted 'high'. ds generated in a Read cycle. For a Write cycle, r/w- is asserted (#6a).
State 3.	cs3 asserted (#7). Processor drives Data Bus d0:d15 for a Write cycle (#14).
State 4.	cs4 (#7) asserted. Multiplexed Addresses now switch to upper Processor addresses (#8c). lds:uds- asserted on a Write cycle. ds generated in a Write cycle.
State 5.	cs5 (#7) asserted. m_cs5- asserted (#8b) indicating the Multiplexed Address Bus is valid.

Table 1 - System Access State Flow

Note: Numbers within '()' refer to ballooned numbers in the Figures.

State	Description (See Figure 2)
State 6.	cs6 asserted. iorc- or iowc- accerted for access to the Timer or UART.
State 7.	cs7 asserted. No action.
State 8.	cs8 asserted. No action.
State 9.	cs9 asserted. No action.
State 10.	cs10 asserted. cs10 generates dtack- to the 68000.
State 11.	No action.
State 12.	Cycle terminates. Negate all strobes (#12). Negate all Clock States (#13). Slave keeps Data bus valid until #11. Negate Data Bus on a Write cycle (#15).

Table 1 - System Access State Flow cont'd

Note: Numbers within '()' refer to ballooned numbers in the Figures.

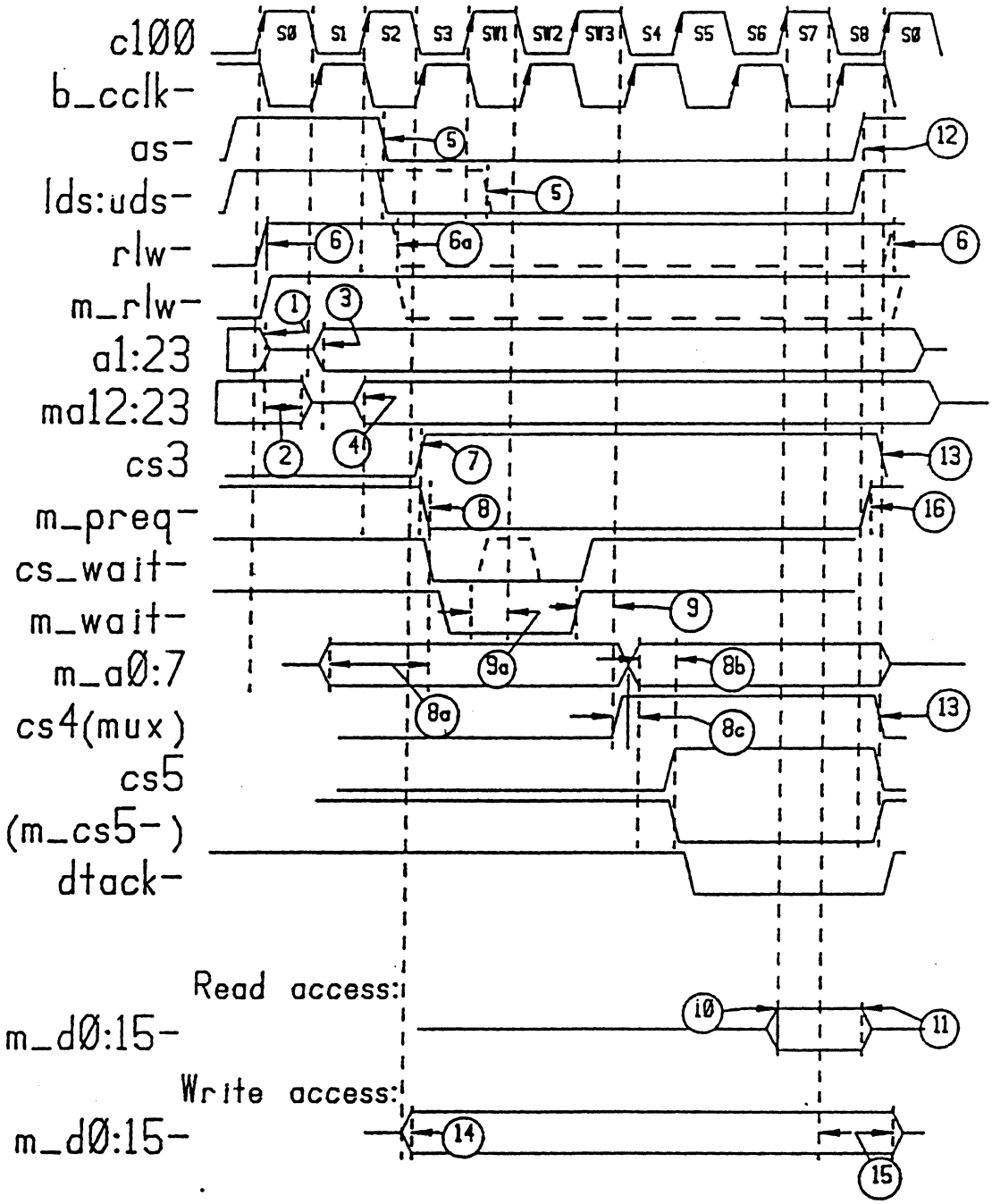


Figure 3 - Ram and Highspeed Access Timing

State:	Description: (See Figure 3)
State 0.	Processor addresses a1 thru a23 are negated (#1). Highspeed Bus High Order Addresses are negated (#2). r/w- is asserted to a Read (#6) at the end of every cycle.
State 1.	Processor addreses a1 thru a23 are asserted (#3). Highspeed Multiplexed Addresses m_a0:7 become valid. Highspeed Bus High Order Addresses m_ma17:23 become valid after Memory Management translation (#4). Page Control bits b/l- and io/m- also become valid (#4).
State 2.	Processor strobes (as- for all cycles, lds:uds- for read cycles) become valid (#5). Clock State generator reset is deactivated. For Write cycle, r/w- is asserted (#6a).
State 3.	cs3 asserted (#7). m_preq- and cs_wait- asserted from cs3 (#8). Processor drives Data Bus m_d0:d15- for a Write cycle (#14).
State Wait.	One Wait inserted automatically by cs_wait- following c100. Clock State generator skips one advance. For a Write cycle, strobes lds:uds- are asserted (#5). cs_wait- is negated to allow the next system clock edge to bump the generator.

Table 2 - Managed Access State Flow for Highspeed Access

Note: Numbers within '()' refer to ballooned numbers in the Figures.

State:	Description: (See Figure 3)
State 4.	cs4 (#7) asserted. Multiplexed Addresses now switch to upper Processor addresses (#8c). cs_wait- disabled.
State 5.	cs5 (#7) asserted. m_cs5- asserted (#8b) indicating the Multiplexed Address Bus is valid. Processor dtack- asserted.
State 6.	No action.
State 7.	Data Bus m_d0:15- captured on a Read cycle (#10 & #11).
State 8.	Cycle terminates. Negate strobes (#12). Negate all Clock States (#13). Negate m_preq- (#16). Negate Data Bus m_d0:15- on a Write cycle (#15).

Table 2 - Managed Access State Flow for Highspeed Access cont'd

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Note: Numbers within '()' refer to ballooned numbers in the Figures.

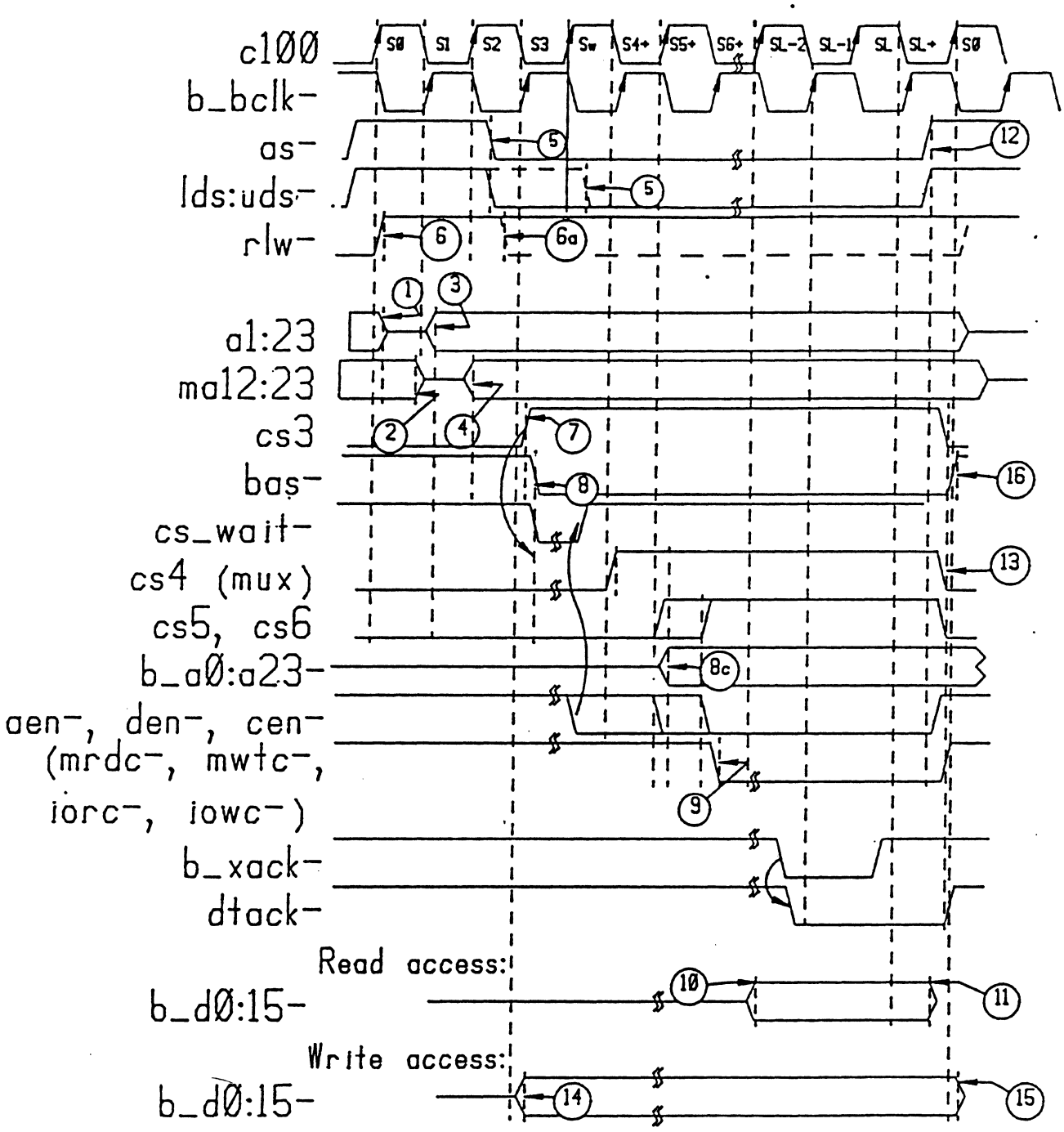


Figure 4 - Multibus Access Timing

State:	Description: (See Figure 4)
State 0.	Processor addresses a1 thru a23 are negated (#1). r/w- is asserted to a Read (#6) at the end of every cycle.
State 1.	Processor addreses a1 thru a23 are asserted (#3). Manased high order addresses ma12:23 become valid after Memory Management translation (#4). Page Control bits b/l- and io/m- also become valid (#4).
State 2.	Processor strobes (as- for all cycles, lds:uds- for read cycles) become valid (#5). Clock State generator reset is deactivated. For Write cycle, r/w- is asserted (#6a).
State 3.	cs3 asserted (#7). bas- and cs_wait- asserted from cs3 (#8). Bus arbitration by the 8289 begun. Processor drives Data Bus d0:d15- for a Write cycle (#14). If aen- is asserted, then the Multibus command shift register is enabled.
State Wait.	One Wait inserted automatically by cs_wait- following c100. Clock State generator skips one advance. For a Write cycle, strobes lds:uds- are asserted (#5). cs_wait- is negated to allow the next system clock edge to bump the generator.
State 4 + Wait.	cs4 (#7) asserted. cs_wait- disabled. lds- is latched to produce a00. If aen- is asserted, then the Multibus Data bus b_d0:d15- is activated by den-. Byte or Word transfers are determined by the state of a00. Direction is determined by r/w-.

Table 3 - Manased Access State Flow for Multibus Access

Note: Numbers within '()' refer to ballooned numbers in the Figures.

State:	Description: (See Figure 4)
State 5 + Wait.	cs5 (#7) asserted. Processor addresses a01:a11, Mapped addresses ma12:23 and the state of the a00 latch are clocked into the Multibus Address registers. If aen- is asserted, the Addresses are driven onto the Multibus b_a0:a23-. cen- is also generated and enables the Multibus command driver.
State 6 + Wait.	A Multibus command (iowc-, iorc-, mwtc- or mrdc-) is generated and buffered to the Multibus (b_iowc-, b_iorc-, b_mwtc- or b_mrdc-) if cen- is asserted. All command, data and address drivers and receivers now remain active until b_xack- is received from the target device.
State Last -2.	b_xack- is received from the Multibus. Processor dtack- is asserted. Current cycle begins to terminate. If the command was iowc-, dtack- asserted will negate it earlier than the other commands.
State Last -1.	No action.
State Last.	Cycle terminates. Negate strobes (#12). Negate all Clock States (#13). Negate current command. Negate bas- (#16) and allow other Multibus Masters to be granted. Negate Data Bus b_d0:15- on a Write cycle (#15).

Table 3 - Mapped Access State Flow for Multibus Access, cont'd

---

Note: Numbers within '()' refer to ballooned numbers in the Figures.

3.2.1. Command Generation
See Schematic #295014 Pages 5 and 1 for specific IC's ant their locations.
See Figure 5 - Clock State Generator and Figure 6 - Command Generation for an overview of the logic.
See Appendices G.1 through G.5 for detailed PAL codes.

The major system clocks on the Processor board (c100, c200 and c400) are produced by dividing the Raw crystal oscillator output c50 (Pg 5 IC E1) by 2, 4 and 8, respectively, by a fast four-bit counter (IC F2)

Command Timing relationships are synchronized by the use of a Clock State Generator (Pg 5 IC H2), which is a 74S299 Octal Shift Register with controls. The clock into the Generator is c50 double buffered, so that when shifts are enabled, their outputs will go to the "high" state on each edge of the 68000 system clock c100.

The outputs of the generator are Clock State signals, labeled cs3 to cs10. The 68000 drives its commands, as-, lds- and uds-, relative to "high" states of the system clock c100. A cycle begins at State 0 with negating the address bus and drives the commands at State 2. The first State after as- is asserted is always cs3.

The reset input of the Clock State Generator is none other than as- from the 68000, inverted, thus enabling it on every 68000 cycle.

The chip has two operating states once enabled, "Shift" and "Do Nothing", controlled by cswait- from PALP3 (Pg 5 IC F6). System Accesses do not require inihibiting the Clock State generator, so only Managed Accesses (those with address a23 low and Boot off) need control cswait-.

When cswait- is used, it must come before cs4 is shifted in. cs3 generates RAS-, cs4 multiplexes the Dynamic Ram address lines and cs5 generates CAS- on the bank selected by Managed Address ma17.

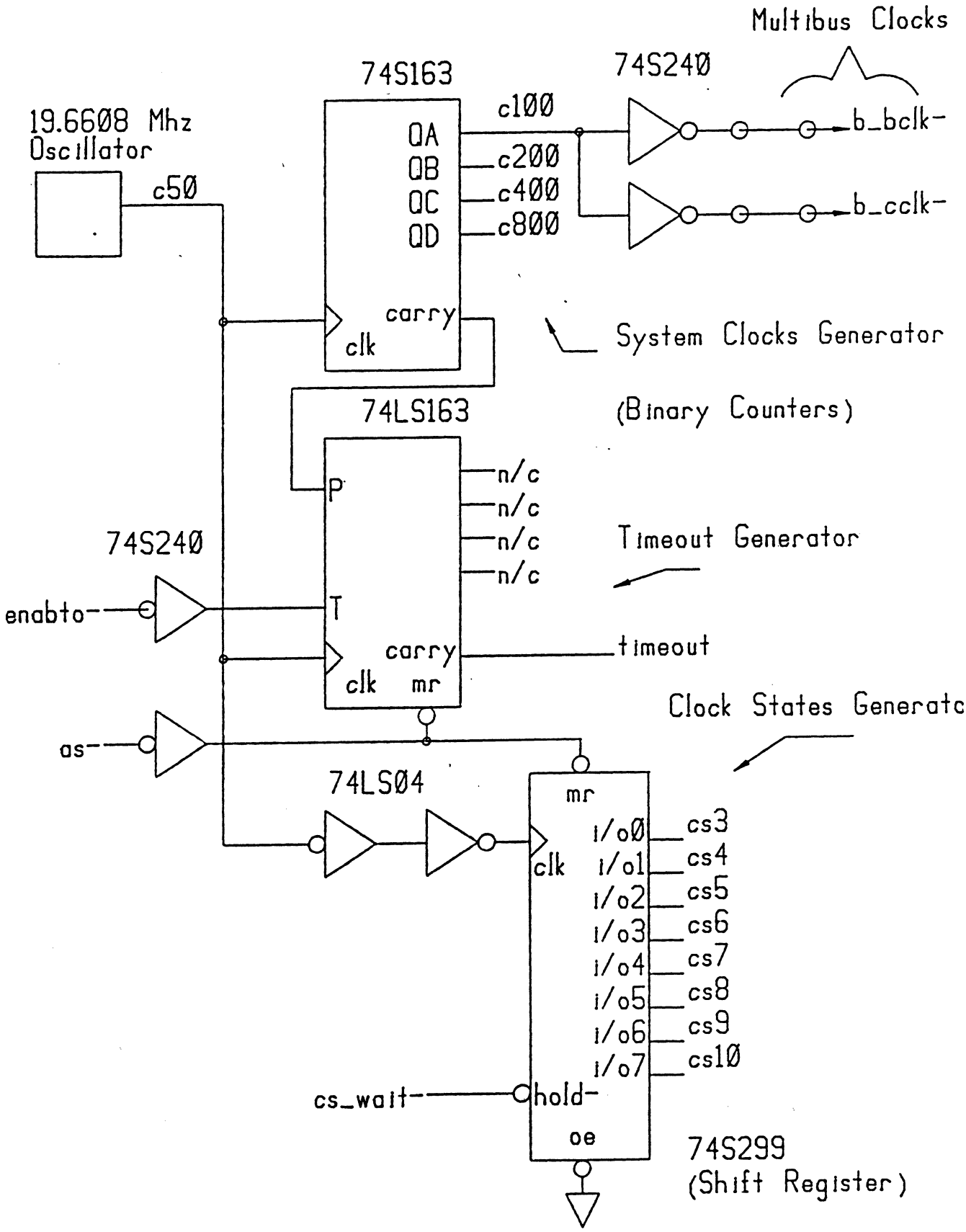


Figure 5 - Clock State Generator Circuit

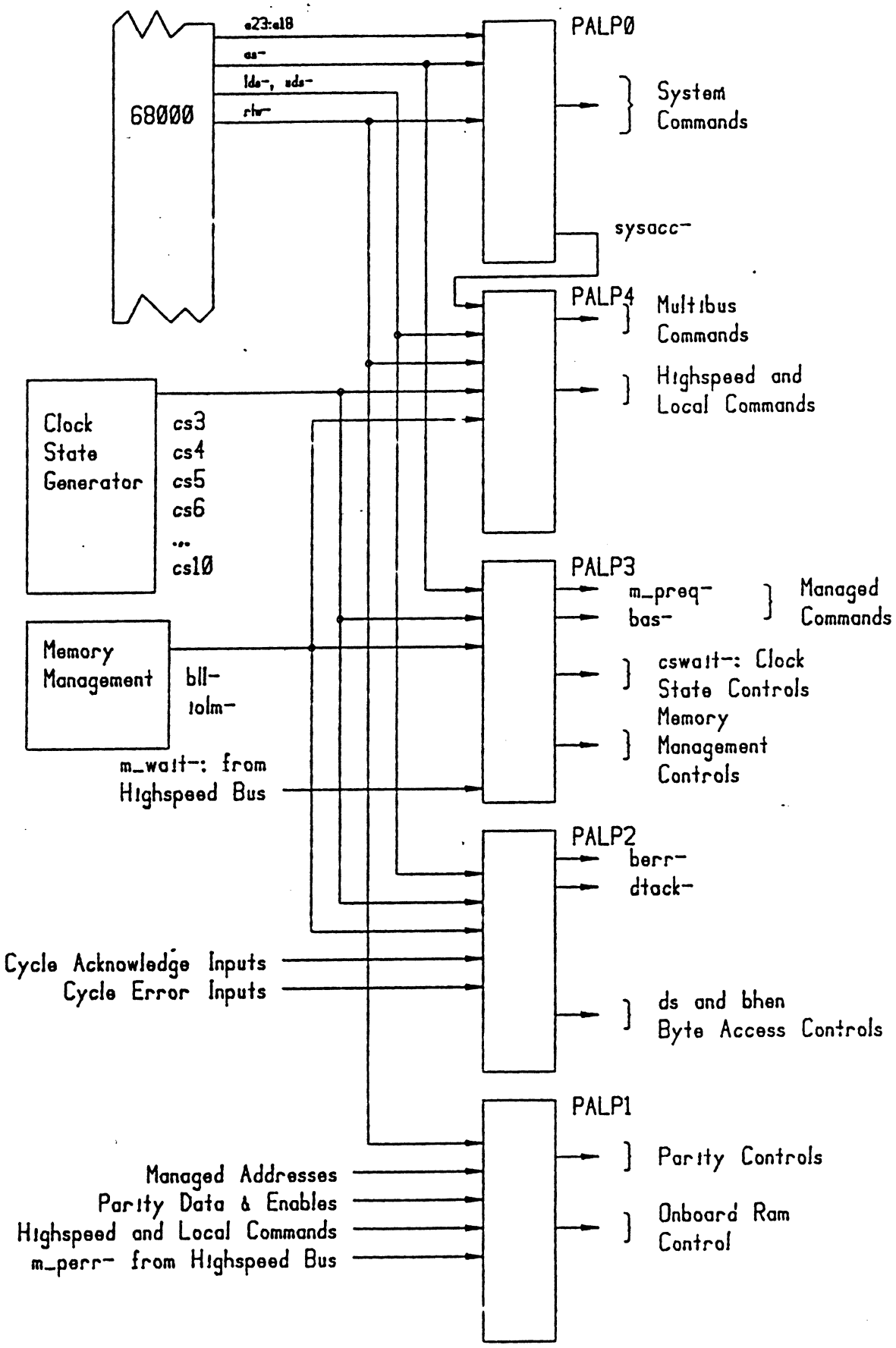


Figure 6 - Command Generation

3.2.1.1. Status Commands
See Appendices G.1 through G.5 for detailed PAL codes.
See Figure 6 - Command Generation for layout of logical functions.

The Status Commands returned to the 68000 are reset-, halt-, berr- and dtack-. halt- and reset- are discussed below.

To acknowledge the 68000's data transfer to the various spaces, dtack- is enabled by two Clock States: cs5 always and cs10 for System Accesses and the special mode if an I-O Write to Multibus.

During a Mapped Access, dtack- will latch itself on if no error is present (by berrx-). Page Control bits b/l- and io/m-, and Multibus response signals aen- and xack complete the necessary logic. The use of cswait- will delay asserting cs5 (and cs10)

During a System Access, berrx- is actually asserted, but dtack- is now generated by cs10 and is not latched.

Error signals berr- (to the 68000) and berrx- (Extended berr-) are generated independently but share the same error conditions. The berrx- signal is the simple "or" of the four basic errors that can happen: two (2) hardware faults - Timeout and Parity Error, and two (2) Memory Management faults - Protection Error (smaperr-) and Invalid Page attempt.

Parity Error means that something is very wrong with Local or Highspeed Memory and should be investigated further. Timeout, however, can be useful in locating what Multibus devices and memory are actually installed by touching standard locations and waiting for a response.

The two Memory Management faults keep the Operating System and the User honest by stopping access to Virtual Addresses that are Protected or mapped Invalid. This gives the Processor board power for complex Operation Systems to easily manage Memory and Devices.

When berr- occurs, the states of timeout, smaperr-, parerr- and berrx- are latched into the Context Register and can be valuable in software when handling the error. (See 3.3.1.2 for Context Register definitions.)

3.2.1.2. System Access Commands

See Appendices G.4 and G.1 for complete logic equations.

The major System Access Commands are initiated in two PALs, PALP3 and PALP0 (Pg 5 IC F6, and Pg 1 IC F5, respectively). System Access Commands are those that control the access and direction of data for On-board devices. Most are based on address a23 in the high state and decode the specific device with a22:a19.

Since access to On-board devices is privilaged, the 68000's Function Code fc2 is gated to enable the command only when the 68000 is in Supervisor state. The User, then, has access to these devices only through System calls or Interrupts.

The current equation for the sysacc- and devenab- signals are clarified as follows:
sysacc- will be low true (Managed Access) when:

```
sysacc- = as                          (Address Strobe off, no cycle)
     + as- * boot- * a23-          (Not in Bootstate and a23 low)
     + as- * boot * rw- * a23-  (1)
```

devenab- will be low true when:

```
deveanb- = fc2 * ds * a23 * a22   (2)
         + fc2 * ds * a23- * a22- * a21- * a20- * a19- * boot * rw  (3)
```

Product line (1) enables a Managed Access Write during Bootstate to initialize On-board Dynamic Ram. This needs to be done early in the Power-on Reset routines to setup valid memory parity for the Stack area. Up to that point, subroutines could not be called and variables had to be in 68000 registers.

Product line (2) enables for Supervisor addresses starting at 0xC00000.

Product line (3) enables for Supervisor address 0x0 during a Bootstate Read. This branch forces access to PROM 0 as the 68000 begins to come up after Power-on or Reset.

3.2.1.3. Managed Access Commands

The majority of Managed Commands are generated in PALP4 (Pg. 1 IC F4) and in PALP3 (Pg. 5 IC F6). These commands include:

Control Clock States: m_wait-, cswait-.

Multibus Memory and I/O commands: mrdc-, mwtc-, iorc-, iowc-, bas-.

Ram and Highspeed: oe.ram-, we.ram[1:0]-, m_preq-, onbrd-.

Page Accesses: we.mapx-, en.mapx-.

All of the above commands are enabled by the 'low' state of sysacc-, which in turn was enabled by the 'low' state of the 68000 address a23. The target bus is selected by b/l- and io/m- from the Page map Rams. mpreq- and bas- are generated by all of the same signals, except for the state of b/l- (See PALP3).

See Section 3.2.1 for discussion of cswait- and m_wait-.

Multibus commands are not made active until cs6 is asserted. The sequence of events for a Multibus acces are detailed in Table 3.

The I/O Write command is a special case. There are many devices available for the Multibus and have similar command response logic for Memory, but I/O logic on some vary considerably in their compliance to the Multibus specification. When doing an iowc- command, b_xack- asserted by the target board will cancel iowc- early. bas- and data drivers will stay asserted until the normal end of the cycle (dtack- asserted and as- negated two (2) high clock states later).

we.ram[1:0]- are directly buffered to the onboard Rams during all valid Local or Highspeed accesses. onbrd- discriminates between Local and Highspeed accesses and controls generating CAS- to the onboard Rams. oe.ram- enables the data buffers for the Local Ram and the Highspeed connector. m_preq- is the overall command that starts some Local or Highspeed access.

The Page Access commands allow the automatic updating of the 'used' and the 'dirty' status lines for the Page being updated. Every time a valid access to a Page is made, it is marked as 'used'. When that Page is written to, it is marked 'dirty' so that the operating system can keep track of memory allocations.

3.2.2. Reset Logic
See Schematic #295014 Page 4.
See Figure 7 for layout of Reset functions

In order to satisfy the 68000 requirements for a hard Reset, both reset- and halt- must be driven at the same time.

Hard Reset is generated by 'or-ing' several conditions together to form setinit- then buffered through two open-collector drivers.

Conditions that generate setinit- are as follows:

Reason:	Control:
Power On	IC D22 is a voltage comparator that will trip its output when the main Power Supply voltage drops below 4.75 Volts. R1 and C5 have the effect of slowing the turn-on time of the Supply.
External Reset	External connections on the J2 Connector and, through Jumper Block JB3, the Multibus b.init-.
Watchdog Timer	Programmable Timer Channel 1. Usually setup to be some large count value that is restarted every Refresh Interrupt. If the counter is allowed to count all the way down, then the Refresh function has somehow stopped, invalidating all of Local and Highspeed Memory.

3.2.3. Boot Logic
See Schematic #295014 Page 4.
See Figure 8

At power-up or Reset to the 68000, the Processor board is in Boot State. A hardware Reset condition (low-voltage comparator, external Reset switch or Programmable Watch-dog timer output) is the signal that sets the Boot flip-flop (Pg 4 IC H4) and is also buffered to drive reset- and halt- into the 68000, causing a hard Reset. (This does not affect the 68000 Reset instruction since reset- is then driven by the 68000 itself.)

This is a temporary condition that allows for loading the initialization information into the 68000 at Virtual memory address 0x0. Boot State makes the first Prom address enabled at 0x0 as well as its normal System Access address of 0xC00000. Once the Prom monitor loads the initial starting address (somewhere above 0xC00000) then the Boot flip-flop is reset and is only re-entered by a hardware reset.

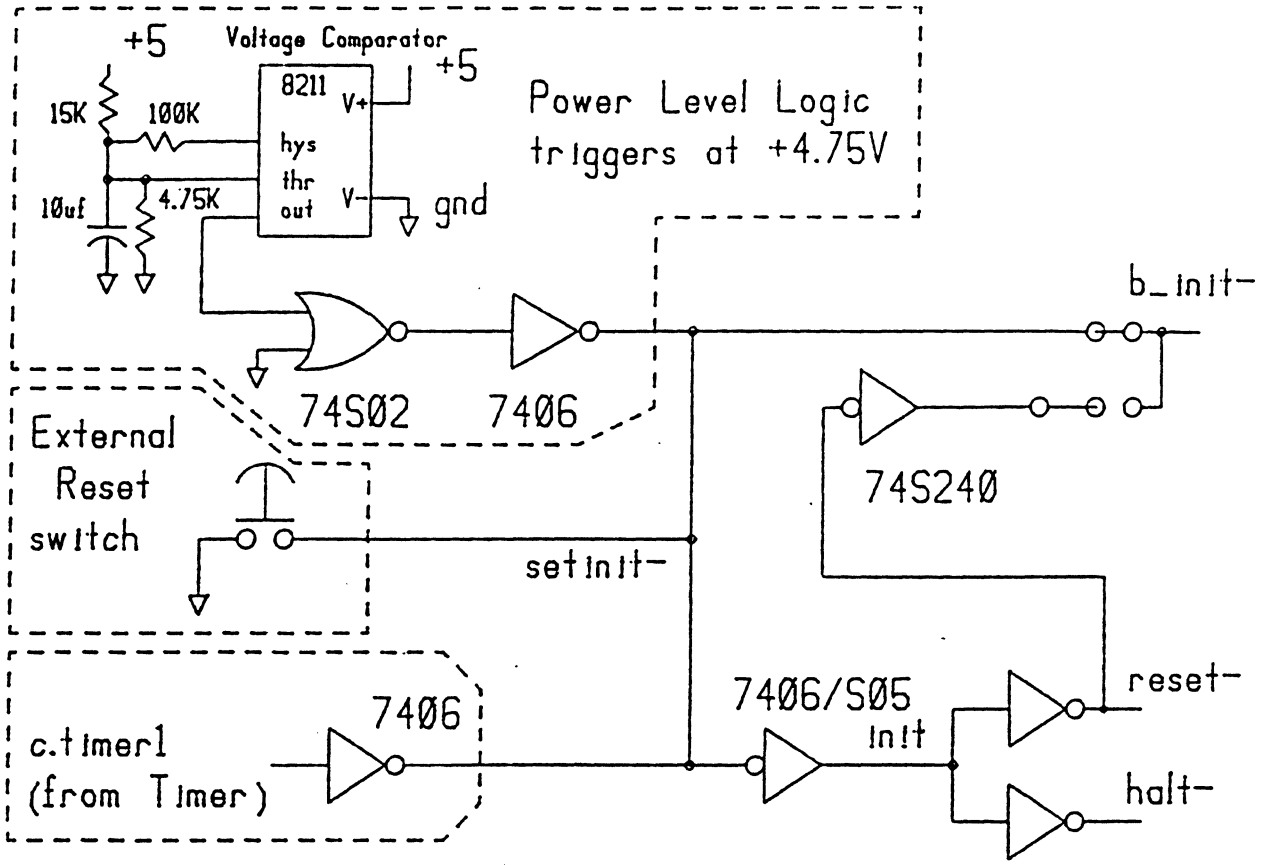


Figure 7 - Reset Circuit

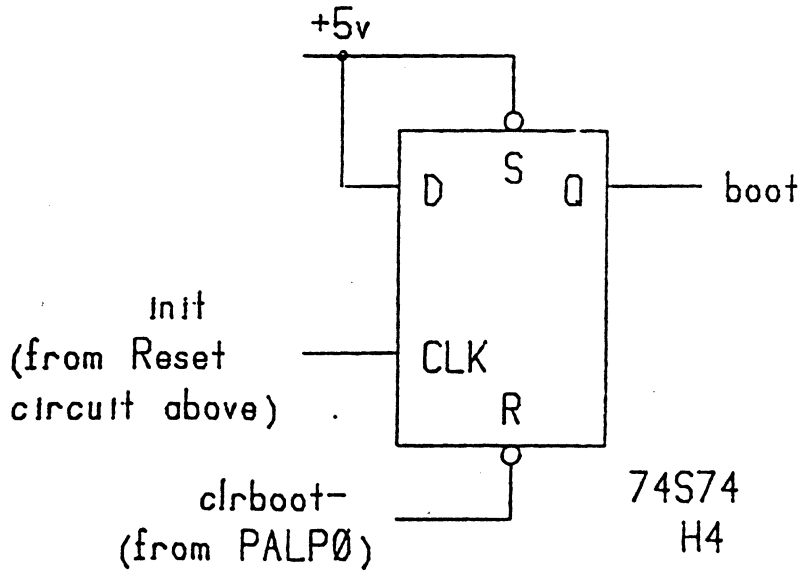


Figure 8 - Boot Circuit

3.2.4. Interrupt Logic

There are 7 allowable Interrupt levels into the 68000 CPU. The highest (Int 7) is reserved for executing the Refresh Routine every 2 (or 4) milliseconds. The next level (Int 6) is a general purpose programmable output of the AMD 9513 timer, as is the Refresh Interrupt.

Level 5 Interrupts are defaulted to the UART for communications.

Interrupt Levels 5 through 1 are hardware wired to the Multibus, with jumpers available to add 6 and 7. All 7 Interrupt signals are then latched into a register (Pg 5 IC K6) using the 68000 system clock c100. These Latched signals go to a priority encoder (Pg 5 IC K7) to provide a three-bit Interrupt code to the 68000 that is synchronous with the system clock to avoid spurious traps.

Another function of Boot State is to disable all interrupts just after power-up or Reset. It's always possible for some On-board device or devices on the Multibus to have an interrupt level active at power-up, and that can cause havoc if Memory has not yet been initialized. The boot signal in the off state enables the Priority Encoder I.C. output.

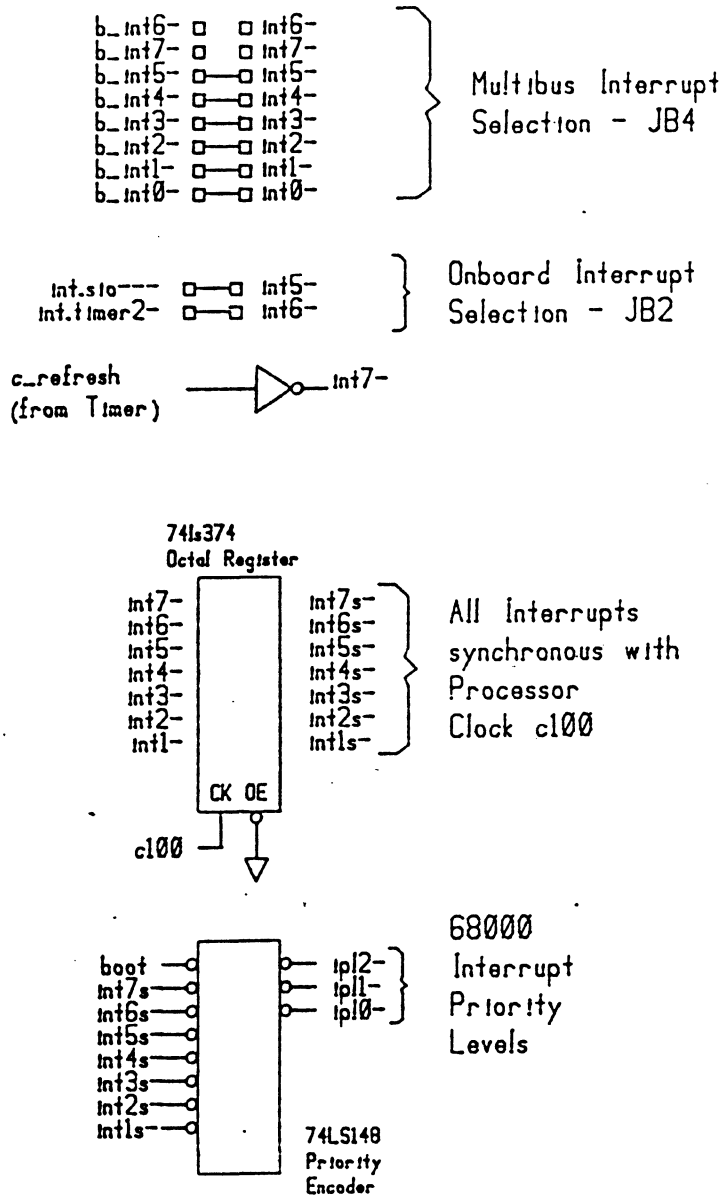


Figure 9 - Interrupt Control Circuit

3.3. Memory Management

The Series 80A Processor Memory Management unit consists of three address multiplexors, 5 fast 4096 x 4 static Rams, buffers for High and Low word access and a 512 x 4 PROM programmed to decode Page Access rights.

The processor is provided with a map that can map pages of 4K bytes anywhere in the 16 Mbyte address space. During initialization, the PROM Monitor sets up the Page map tables in a standard way that makes all memory and I/O devices available to user programs. User programs may change these maps as desired; however, page 0 and whatever pages are likely to contain the top of the Supervisor Stack should not be remapped, otherwise memory refresh may fail.

3.3.1. System Accesses

Every 68000 bus cycle accesses some Virtual memory location within the 16 Mbyte addressing range. When address bit a23 is "on", or "high", then the current cycle is a System Access, hence occupying the upper 8 Mbytes of available Virtual memory.

3.3.1.1. Memory Map

The starting address for System Access to the Memory Map is 0x800000. The signals ce.map- and we.map- are generated by PALP0 (IC F5). When access into the Memory Map Rams is requested, the lower address bus into those Rams is multiplexed by the following table:

Managed Access (a23 Low)	System Access (a23 High)	Translated Map Address:
cx0/cx1	a13	xa11
a22/cx0	a12	xa05
a21	a11	xa04
a20	a10	xa00
a19	a09	xa01
a18	a08	xa02
a17	a07	xa03
a16	a06	xa07
a15	a05	xa06
a14	a04	xa08
a13	a03	xa10
a12	a02	xa09

Table 4 - Memory Management Address Translation

Initially, each page of on-board RAM is mapped so that its physical and virtual addresses are identical. This means that each segment, starting at segment 0, is fully mapped (up to the limit of available memory). Pages are only initialized for context 0. Page protection is set so that both Supervisor and User modes have Read, Write, and Execute access to every segment.

The enable control to the 4K x 4 is permanently active to allow fast access during a Managed cycle. The Write commands are separated into Upper and Lower enables, depending on address bit a1 (Schem Pg-1).

Writing to the Ram that contains the four Page Control information is split into two conditions to generate we.mapx-: one for the normal System access write (we.mapl-) and the other for updating the used and dirty bits (en.mapx-).

The preferred access to the Memory Map is via long-word (32 bit) moves. This format places the Protection Code data bits in the "Low word", or internal data 31-16, and the Page Control and Managed Addresses in the "High word" or internal data 15-0. Consequently, Map 0 is located at address 0x0, Map 1 is at 0x4, etc.

The format of the data bus into the Memory Map is as follows:

Map Entry:	System Data:
Protection Code:	
PROT3	d19
PROT2	d18
PROT1	d17
PROT0	d16
Page Control:	
used	d15
dirty	d14
bus!local (b/l-)	d13
IO!Memory (io/m-)	d12
Mapped Addresses:	
ma23	d11
ma22	d10
ma21	d9
ma20	d8
ma19	d7
ma18	d6
ma17	d5
ma16	d4
ma15	d3
ma14	d2
ma13	d1
ma12	d0

Table 5 - Page Map Data Entries

3.3.1.2. Context Register

The starting address for a System Access into the Context Register is 0x880000.

The Context Register is a one-word field whose bits reflect various status information about Memory Management integration, Refreshing of dynamic memory and Bus Error generation.

The format of data in the Context Register is as follows:

Data:	Function:
Read-Write:	
d15	Refresh Enable - When 'one', indicates to Slave boards on the Highspeed Bus to override Upper Address decoding to permit refreshing of Dynamic rams, if any.
d14	Parity Enable - When 'one', allows either Local Parity Error detection or Highspeed Parity Error (m.perr-) to generate berr- to the 68000, indicating a bad Read has taken place.
d13	Context bit cx1.
d12	Context bit cx0.
Read Only:	Latched Error:
d8	smaperr- (Low True). Indicates a Protection Code violation.
d7	Parity Error parerr- (Low true).
d6	Timeout (High true). Too much time taken on a Managed Access (Multibus or 'Local' ram access).
d5	Bus Error extention berrx- (Low true). True on any of the above three error conditions, but is also valid alone when access to a Page mapped 'Invalid', that is, mapped as 'Local I/O', has been attempted.

Table 6 - Context Register Data Format

Context bits cx0 and cx1 provide latched address bits into the Memory Map when a Managed Access is initiated. This gives the operating system, like UNIX, the flexibility of switching Memory Maps easily between processes.

Hardware default enables one context bit, allowing 2 Contexts, each 8M bytes per process. A second context bit, cx1, can be used to provide 4 Contexts, each 4M bytes per process.

3.3.1.3. Proms

The four 28-pin on-board PROM sockets support the JEDEC standard pin assignments for ROMs and EPROMs. The Jumper block JB1 (See Appendix A) selects address bits a14 and a15 to the sockets.

Default Jumpers select 2732/2764 type 4K/8K EPROMs and allow expansion upwards to 27128 (16K) and 27256 (32K) type devices.

Access to the first Logical PROM pair is allowed under two conditions: one, immediately after Reset, decodes the PROM 0 starting address at 0x0; the second decodes the PROM 0 address at 0xC00000.

The PROM 1 address is defaulted to 0xC80000 at all times.

3.3.1.4. AMD 9513 Timer
See 'The Am9513 System Timing Controller Handbook' from Advanced Micro Devices for a compleat description of all of the functions of the chip.
See Figure 10 for AMD's Function Diagram of the 9513 Timer.

3.3.1.4.1. Introduction

This discussion gives a quick overview of the functions of the chip that the Series 80A Processor Board makes use of.

The 9513 is a support device for processor oriented systems that is designed to enhance the available capability with respect to counting and timing operations. It provides the capability for programmable frequency synthesis, high resolution programmable duty cycle waveforms, retriggerable digitial timing functions, time-of-day clockings, coincidence alarms, complex pulse generation, high resolution baud rate generation, frequency shift keying, stop-watch timing, event count accumulation and many more. A variety of programmable operation modes and control features allow the 9513 to be personalized for particular applications as well as dynamically reconfigured under program control.

3.3.1.4.2. Functional Description
See Figure 10 for AMD's Function Diagram of the 9513 Timer.

The oscillator's frequency is controlled at the X1 and X2 interface pins by the System Clock divided by 2, giving a reference frequency of 4.9152 Mhz. The internal oscillator's output is devided by the Frequency Scalar to provide several sub-frequencies.

The 9513 is addressed by the external system as two locations: a Control port and a Data port. the Control port provides direct access to the Status and Command Registers, as well as allowing the user to update the Data Pointer register. The Data port is used to communicate with all other addressable internal locations. The Data Pointer register controls the Data port addressing.

Among the registers accessible through the Data port are the Master Mode register and five (5) Counter Mode registers, one for each counter. The Master Mode register controls the programmable options that are not controlled by the Counter Mode registers.

Each of the five general-purpose counters is 16-bits long and is independantly controlled by the Counter Mode register. Through this register, a user can software select one of 16 sources as the counter input, a variety of gating and repetition modes, up or down counting in binary or BCD and active-high or active-low input and output polarities.

Associated with each counter are a Load register and a Hold register, both accessible through the Data port. The Load register is used to automatically reload the counter to any predefined value, thus controlling the effective count period. The Hold register is used to save the count values without disturbing the count process, permitting the host Processor to read intermediate counts.

All five counters have the same basic control logic and control registers. Counters 1 and 2 have additional Alarm registers and comparators associated with them, plus the extra logic necessary for operatiing in a 24-hour time-of-day mode.

Each general counter has a single dedicated outpin. It may be turned off when the output is not of interest or may be configured in a variety of ways to drive interrupt controllers, buffers, etc.

3.3.1.4.3. Timer Commands

A powerful command structure simplifies user interaction with the counters.

A counter must be armed by one of the ARM commands before counting can commence. Once armed, the counting process may be further enabled or disabled using hardware gating facilities. (The Series 80A Processor necessarily ties all Gates and Sources to one unchanging state. Sorry.) The ARM and DISARM commands permit software gating of the count process in some modes.

The LOAD command causes the counter to be reloaded with the value in either the associated Load register or the associated Hold register. It can often be used as a software retrigger.

The DISARM command disables further counting independent of any hardware gating. A disarmed counter may be reloaded using the LOAD command, may be incremented or decremented using the STEP command and may be read using the SAVE command. A count process may be resumed using an ARM command.

The SAVE command transfers the contents of a counter to its associated Hold register. This command will overwrite any previous Hold register contents. TheSAVE command is designed to allow an accumulated count to be preserved so that it can be read by the host Processor at a later time.

Two combinations of basic commands exist to either LOAD AND ARM or to DISARM AND SAVE any combination of counters.

Additional commands are provided to: step an individual counter by one count; set and clear an output toggle; issue a software Reset; clear and set special bits in the Master Mode register; and load the Data Pointer register.

3.3.1.4.4. Cadlinc Operating Modes

The 9513 has been hardware configured to provide a variety of services on the Series 80A Processor board. Two (2) of the channels are dedicated Baud rate generators, using Master Mode D, and do not generate interrupts. Two (2) other channels use Mode A to toggle their associated outputs and provide interrupts to the 68000 at level 7 (for refreshing Dynamic Rams) and level 6 (user programmable). The interrupt routines must set the output inactive and leave the count run free to interrupt again at the proper rate (every 2 milli-seconds for INT 7, for example).

The fifth channel can be configured to pulse the 68000 Reset whenever the count reaches zero. This is called the Watchdog Timer function. It is meant to be used in an operating system that monitors the Refresh counter interrupts and reloads the Count into the Watchdog Timer. If the operating system hangs and no longer services these, then the Board will automatically Resets.

Channel 2 of the 9513 is the only one buffered to a jumper allowing connection to anything. Its default is to level 6 interrupt.

Channel 1 is the Watchdog Timer; channel 3 is the Refresh Timer connected to level 7 interrupt. Channels 4 and 5 are the Baud rate generators.

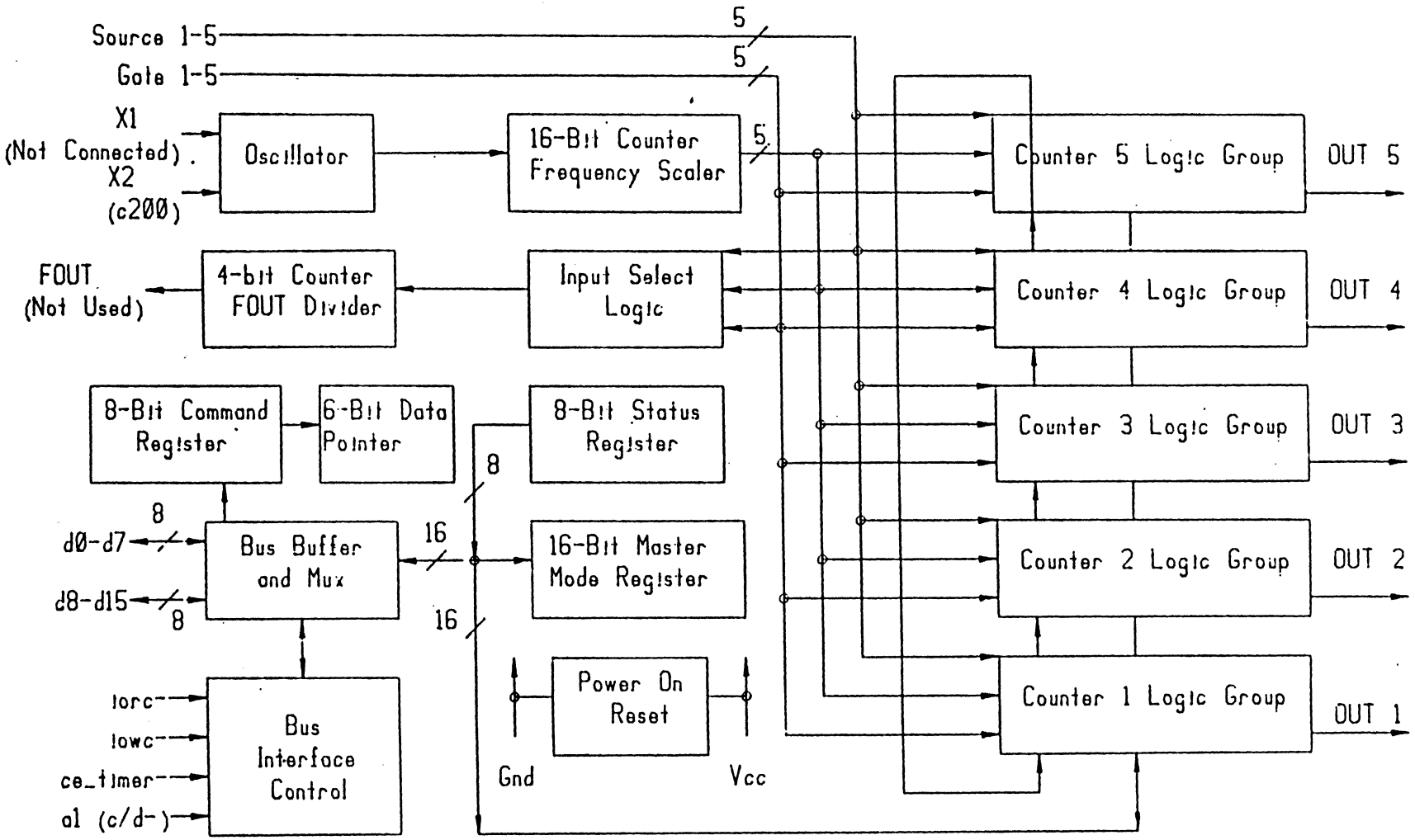


Figure 10 - Timer Function Diagram

3.3.1.5. Intel 8274 UART
See specification sheets on the Intel 8274 or NEC 7201 for a compleat description of all of the functions of the chip.
See Figure 11 for UART Block Diagram.

3.3.1.5.1. Introduction

This discussion gives a quick overview of the functions of the chip that the Series 80A Processor Board makes use of.

The Dual-Channel UART chip supports Asyschronous (Start-Stop), Byte Synchronous (Monosync, IBM Bisync), and Bit Synchronous (ISO's HDLC, IBM's SDLC) protocols. The Cadlinc Series 80A Processor configures the UART to use only the Asynchronous, Polled or Interrupt driven and non-DMA features.

3.3.1.5.2. Functional Description

The system interface to the host Processor consists of 8 ports or buffers:

a2	a1	Read Operation	Write Operation
0	0	Ch. A Data Read	Ch.A Data Write
1	0	Ch. A Status Read	Ch. A Command-Parameter
0	1	Ch. B Data Read	Ch.B Data Write
1	1	Ch. B Status Read	Ch. B Command-Parameter

Data buffers are addresed by a2 = 0, and Command ports by a2 = 1.

Command, status and parameter information is held in 22 registers within the UART (8 Write register and 3 Read registers for each channel).

An internal pointer register selects which of the command or status registers will be read or written during a command-status access to a channel.

After Reset, the contents of the pointer register are zero. The first write to a command register causes the data to be loaded into Write Register 0 (WR0). The three least significant data bits of WR0 are loaded into the Command Status Pointer. The next Read or Write operation accesses the read or write register selected by the pointer. This pointer is reset after the operation is completed.

3.3.1.5.3. UART Commands

For operating in the Asynchronous mode, the UART must be initialized with the following information: character length (WR3; d7, d6 and WR5; d6, d5), clock rate (WR4; d7, d6), number of stop bits (WR4; d3, d2), odd, even or no parity (WR4; d1, d0), interrupt mode (WR1, WR2), and receiver (WR3; d0) or transmitter (WR5; d3) enable. When loading these parameters into the UART, WR4 information must be written before the WR1, WR3, WR5 parameters-commands.

3.3.1.5.4. Cadlinc Operating Modes

The Processor board does not enable any DMA functions of the UART. Both channels are allowed to use Polled and Interrupt operating modes. Interrupts for all serial communications, including multiple Multifuction boards, are handled via INT 5.

Both channels transmit and receive using RS-423 compatible drivers and receivers, transmitting at +5 V to -5 V level and able to receive standard RS-232 levels of +12 V to -12 V. The receiver device is a two-input balanced level comparator that has the + input grounded and the - input connected to the active signal. The transmitter device drives a single line per input.

Channel A is reserved for the Console terminal (either a Cadlinc Keyboard and CRT monitor or a dumb terminal) and does not use any hardware to enable modem controls. This port can then be used in a simple three-wire communication scheme (TxD, RxD, ground).

Channel B allows the use of these modem control signals: DTR, RTS, CTS, and DCD.

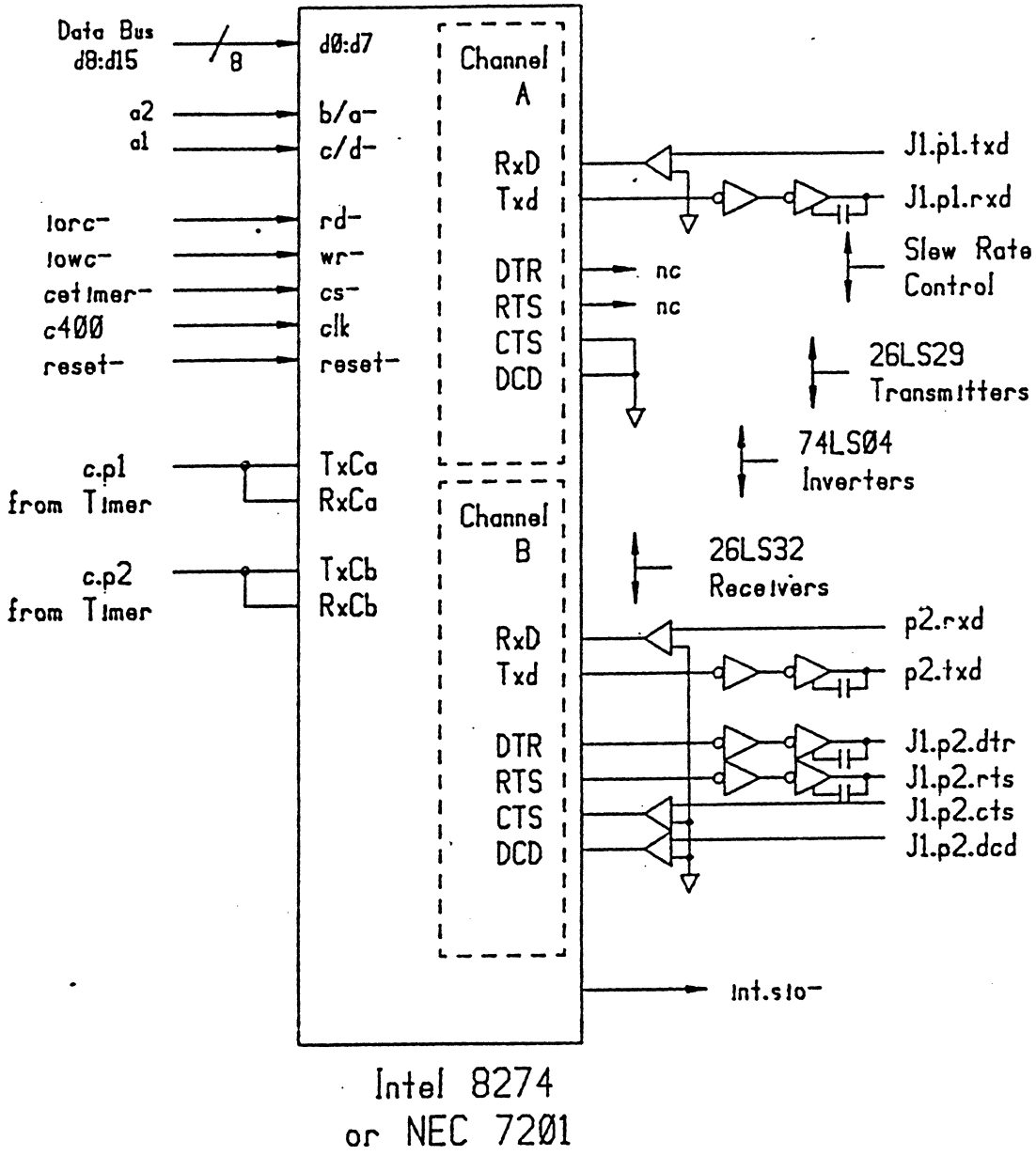


Figure 11 - UART Block Diagram

3.3.1.6. Parallel Input Port

See Appendix E for pin assignments.

The Parallel Port currently reads 16 external switches from which the PROM Monitor interprets Root devices and Console configuration.

The default access address for oe.port- is 0x900000.

Control signals as-, r/w- and oe.port- are buffered through Open Collectored drivers for interface handshaking. The halt- signal is also buffered to drive an external LED.

The Parallel Port receives set.init- from an external Reset switch and is then wire-ored to generate the 68000 reset- signal.

3.3.1.7. Hardware VPA

The signal vpa- is a System Access address at 0xF80000. It is only used during the 68000's Autovector Interrupt handling. When an Interrupt occurs and is accepted, the 68000 sets the Higher Order address bits to "one". The signal vpa- is received by the 68000 as Valid Peripheral Address.

3.3.2. Managed Accesses

Refer to Schematic drawing #295014 pages 1 and 5

When a Managed Access is requested, the used and dirty bits of the Page Control Static ram must be updated to show that a particular page was accessed (used) and if was written to (dirty). These signals are multiplexed by r/w and multiplexor chip (IC H7) is enabled by en.mapx- from PALP3 (IC 6). If there is a page fault on the cycle, i.e. Protected from Read, Write or Execute, then the write is not done, leaving the status unchanged for further processing. If the cycle is okay by cs6 time, then b/l- and io/m- are unchanged, used is always written as 'one' and dirty is changed to 'one' during a write only.

The static Rams write on the trailing edge of its write-enable input. To resolve the Page Control updates, en.mapx- is delayed from going active until cs6. This allows the Bus error logic time to decide that the Managed cycle is good.

3.3.2.1. Ram Memory

Ram Memory accesses imply either Local RAM data located on-board the Processor, or Highspeed accesses located on Dual-Ported Memory boards, the Floating Point board or other devices responding to Highspeed bus requests.

3.3.2.1.1. Local Memory

The Local Ram unit consists of 36 x 64Kbit Dynamic Ram devices (Pg 2) giving a total of 262,144 bytes of Parity checked memory. The Multiplexed addresses and Data driven into the Rams are also directly connected to the Highspeed bus. This makes the Highspeed bus a functional extension of the Local Ram.

The Ram cycle begins when cs3 is buffered (Pg 1 - IC F03 and Pg 2- IC E14) to drive ras- to all the Rams. At cs4, the Lower Address driver (Pg 2- IC A14) is shut off, and the Upper Address driver (Pg 2- IC C14) is enabled. At cs5, cas0- or cas1- is selected and driven (page 2- ICs K14 and E14) to the appropriate bank of 18 Rams.

The addresses into the Rams are not a straight-forward swap of address bits. The following table details the address translation:

Bus Address	At cs3 (ras-)	At cs5 (cas-)
m_a0	a4	a9
m_a1	a1	ma15
m_a2	a6	ma14
m_a3	a7	a10
m_a4	a3	ma12
m_a5	a2	ma16
m_a6	a5	a11
m_a7	a8	ma13

Table 7 - Multiplexed Ram Addresses

3.3.2.1.2. Local Parity Logic
See Schematic #295014 Page 5
See Figure 12 for Local Parity Block Diagram.

The 256K bytes of On-board dynamic ram is provided with Parity checking on every byte. A Parity bit is generated on a write by resolving the even parity of the byte with two 82S62 Parity Generator/Checkers (IC B15 and B17), with the r/w- line as the ninth bit of both bytes. The output of this logic goes to the data-in of the Parity Dynamic Ram, and is written with the rest of memory. When a Read is done, the data-out of the Parity ram now becomes the ninth bit, and the output of the logic should indicate correct Parity.

When an error does occur, PALP1 (IC B19) provides the input to a flip-flop, enlperr-, that will be clocked on the trailing edge of as- from the 68000 to generate lperr-.

The signal used to generate berr- to the 68000, parerr-, is enabled in PALP1 by the Context Register bit prtyenab, lperr- from the Local Parity logic and by m.perr- from the Highspeed bus.

The parerr- signal will actually be seen on the cycle after the occurance of the error. Software handling of bus errors must be able to tell Parity Errors from every other error to recover control. The Cadlinc Prom Monitor resident on the board prints an error message any time a berr- occurs and stops the process. Other errors indicate violation of various Protection or Allocation rights, but Parity Error is always significant.

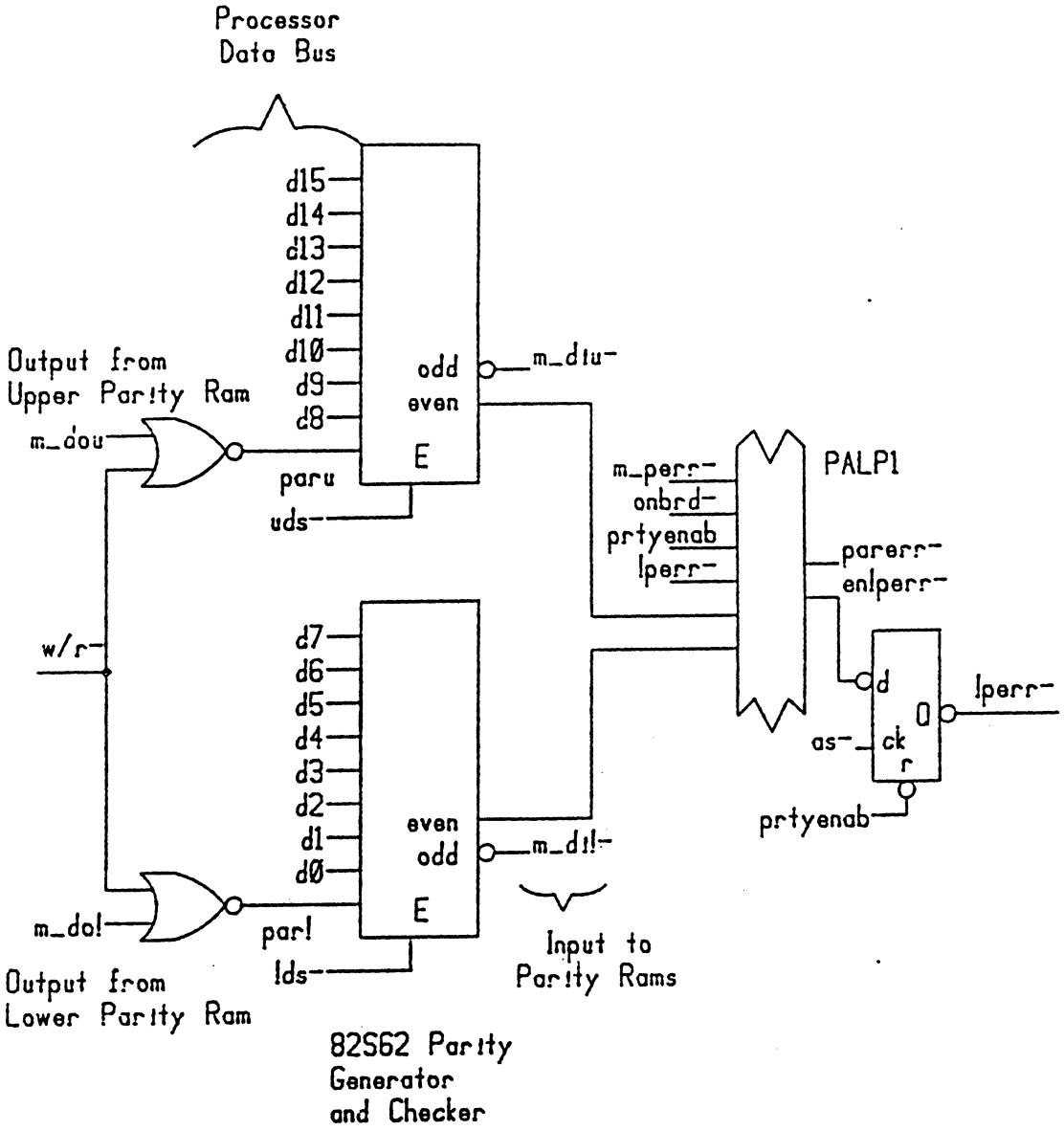


Figure 12 - Parity Logic Block Diagram

3.3.2.1.3. Highspeed Bus Interface

The Cadlinc Highspeed Bus allows the Processor to access more fast memory than physically resides on the CPU board. The Highspeed Bus is meant to respond as fast as the On-board memory and to respond to control signals as if it were an extention of the Dynamic Ram memory chips. This gives the Processor a full 16 Mbytes of highspeed memory on one bus while freeing the Multibus for other Master devices. Cadlinc Dual-Ported Memory boards are an integral part of the high-performance system for their accessibility by both this Highspeed bus and by the Multibus.

When the current 68000 address cycle selects 'Local' memory through Memory Management, i. e., the m_preq- command is asserted, the high-order Managed Address bits m_ma23 through m_ma17 specify memory somewhere out on the Highspeed bus. If a board has responded to the address range, then it will drive or receive data on the Highspeed bus, on a write or a read, respectively.

There is no explicit 'acknowledge' of the cycle by the slave board on the Highspeed bus, just as there is no explicit acknowledge of an On-board memory request when the addresses there happen to compare. The Highspeed bus interface relies on m_wait- from the slave board to indicate whether it is ready to accept the Multiplexed Ram addresses. m_wait- directly controls the Clock State generator by generating cswait- in PALP3 (Pg 5 - ICF6), thereby preventing the shift register from advancing until it goes away, synchronous with the 68000 clock c100. If there happens to be no slave board to respond to the address, then no m_wait- would be generated and the cycle terminates normally without data being transfered or error.

The slave board will usually generate m_wait- when it is being accessed on the other bus it is connected to, e.g., Multibus for Dual-Port Memory or the 8086 processor on the Floating-Point board. Also, for boards with Dynamic Ram devices, as opposed to Static Rams, a period of time after the actual bus access ends must be inserted to maintain the Rams' 'precharge' requirements.

When all delays on the slave board are resolved, it will begin to drive its local addresses based on the Multiplexed Ram addresses, now in the Low Address state. m_wait- will be negated at this time and the next high state of c100 effectively lets the Clock State generator advance, driving the new High Address states onto the bus.

From that point, the cycle terminates normally without any further control from the slave board.

3.3.2.2. Multibus Interface

When the current 68000 cycle selects a 'Bus' access through Memory Management, the Control Logic generates bas-, which is used to as the request to start Multibus arbitration. The particular command to be driven out to the Multibus is dependant on the how the Memory Map for that page was setup.

3.3.2.2.1. Bus Master Arbitration

See Schematic #295014 Page 3

The Arbitration Logic uses an 8289-type Bus Arbitor (IC K3). The chip is used in a simple mode, where there is one input (bas-) and one output (aen-) actually used by the Processor board.

The Status Line Inputs are all tied to bas-, thereby going idle when the 68000 cycle ends and allowing another Bus Master access through it. It is intended the Processor make the most use of faster Local and Highspeed Memories so that the bulk of Multibus accesses are done by other standard devices.

The b.prn- (Priority In) signal into the 8289 is selectable to allow the Processor board Highest Priority for access to the Multibus, or to receive the b.pro- (Priority Out) from the board immediately above it in the card case. In both cases, the 8289 drives its own b.pro- to the board immediately below the Processor. This scheme also allows for higher speed Parallel Arbitration that can accomodate as many as 8 Masters on the Bus.

All the rest of the Multibus Arbitration signals (b.init-, b.breq-, b.busy-, and b.creq-) are used internally by the 8289 to satisfy the Intel requirements.

Once control of the Multibus is established, aen- goes active and stays on until another Bus Master request takes control away. The Address Bus is directly enabled by aen-, and the Data and Command driver delays are enabled by bas- and aen-. When bas- and aen- are both asserted, a shift register (IC K1) is enabled and is clocked by the 20MHZ base clock. The second shifted output enables the Data drivers (den-), the third shift enables the Command drivers (cen-).

The Processor board supports Multibus byte accesses by latching in the state of the 68000's lds- line at cs4 time, generating Multibus address ba0, and providing a local bhen (Byte High Enable) from both lds- and uds- in PALP2 (Pg - 5 ICF1). These two lines are latched along with the Managed Address bus (ma23:ma12) and the lower 68000 address bus (a11:a1) at cs5 time to provide the full 24 bits of Multibus accesses. All four of the Multibus commands (mrdc-, mwtc-, iorc-, iowc-) are then gated, in PALP4 (Pg 1 - IC F4), to begin at cs6 time.

All 24 bits of the Multibus Address bus are driven for either Memory or I-O accesses.

When b.xack- is driven by the target board as the acknowledge, dtack- is generated in PALP2 (IC F1). dtack- then latches itself asserted until the end of the 68000 cycle.

3.3.2.2.2. Memory Access

PALP4 (IC F4) decodes mrdc- and mwtc- on the proper state of b/l-, io/m- and r/w-.

3.3.2.2.3. I-O Access

Many Mulitbus products use either 16 or 8 bits to decode I-O addresses. The Processor board drives all 24.

PALP4 (IC F4) decodes iorc- and iowc- on the proper states of b/l-, io/m- and r/w-. There is a special mode for terminating the iowc- command early. When b.xack- is returned and dtack- is asserted, the iowc- command is terminated, but the 68000 cycle still has 2+ clock states of Multibus control.

This was done to accommodate Multibus boards that return b.xack- immediately after receiving the iowc- command, allowing a wide margin of data hold time on the bus.

4. Board Mnemonics

(Note: Schematic drawings and the printed format of the wirelist are slightly different in notation. Mnemonic 'b.init\' on the schematic corresponds to 'b_init-' on the wirelist, etc. This is because UNIX editors, through which these documents were prepared, differ slightly in their handling of special characters, i.e. '\', '.' and '-'. In general, then, '_' or '.' in a mnemonic signify an off-board connection, and '-' or '\' as the last character of the mnemonic mean it is 'low' true.)

Processor Board Signal Names:

(Mu) -12vdc	(Mu) bhen	(Co) cs7
(Mu) -5vdc	(Co) boot	(Co) cs8
(Mu) 12vdc	(MM) bll-	(Co) cs9
(Bu) a0	(Co) c100	(Co) cs10
(Bu) a1:a23	(Co) c200	(Co) cswait-
(Bu) a1-	(Co) c400	(Cm) ctsb-
(Mu) aen	(Co) c50	(MM) cx0:1
(Mu) aen-	(Co) c50-	(Bu) d0:15
(Co) as	(Co) c50--	(Mu) d1aen
(Co) as-	(Co) c800	(Mu) d2aen
(Mu) b_a0:23-	(Cm) c.p1:2	(Mu) d3aen
(Mu) b_bclk-	(Co) c_refresh	(Cm) dcdb-
(Mu) b_bhen-	(Co) c_timer1:2	(Mu) den-
(Mu) b_bprn-	(Co) carry	(Dv) devenab-
(Mu) b_bpro-	(Co) cas0:1-	(MM) dirty
(Mu) b_brea-	(Mu) cclk-	(Co) ds
(Mu) b_busy-	(Mu) ce_byte-	(Co) dtack-
(Mu) b_cbra-	(MM) ce_map-	(Cm) dtrb-
(Mu) b_cclk-	(MM) ce_mapl-	(Cm) dtrb--
(Mu) b_d0:15-	(MM) ce_mapu-	(MM) en_mapx-
(Mu) b_inh1-	(Dv) ce_prom0:1-	(Co) enabto
(Mu) b_inh2-	(Dv) ce_sio-	(Co) enabto-
(Mu) b_init-	(Dv) ce_timer-	(Co) enlperr-
(Mu) b_int0:7-	(Mu) ce_word-	(Co) fc0:2
(Mu) b_inta-	(Mu) cen-	(Mu) gnd
(Mu) b_iorc-	(Mu) cen1-	(Co) halt
(Mu) b_iowc-	(Co) ckberr	(Co) halt-
(Mu) b_mrdc-	(Co) clrboot-	(Co) hardreset
(Mu) b_mwtc-	(Co) cs3	(Co) hardreset-
(Mu) b_xack-	(Co) cs3-	(Co) hyst
(Mu) bas-	(Co) cs4	(Co) init
(Mu) bclk-	(Co) cs4-	(Co) init-
(Co) berr-	(Co) cs5	(Co) int0:7-
(Co) berrx-	(Co) cs6	(Co) intls:7s-

Symbols Used:
- Bu - Buses
- Cm - Communications
- Co - Commands
- Dv - Devices
- Hs - Highspeed
- MM - Memory Management
- Mu - Multibus

Processor Board Signal Names cont'd:

(Co) int_sio--	(Hs) m_uds-	(MM) smaperr-
(Co) int_sio---	(Hs) m_wait-	(Co) sysacc-
(Co) int_timer2-	(MM) ma12:23	(Co) thr
(Dv) iorc-	(Co) mcas0:1-	(Co) timeout
(Dv) iowc-	(Co) mras-	(Cm) txda:b
(MM) iolm-	(Mu) mrdc-	(Cm) txda:b-
(Co) ipl0:2-	(Co) mweraml-	(Co) uds-
(Cm) j1_p1_rxd	(Co) mweramu-	(MM) used
(Cm) j1_p1_txd	(Mu) mwtc-	(Mu) vcc
(Cm) j1_p2_cts	(Co) nc	(Bu) vccla14
(Cm) j1_p2_dcd	(MM) oe_cx-	(Bu) vccla15
(Cm) j1_p2_dtr	(Dv) oe_port-	(Co) vpa-
(Cm) j1_p2_rts	(Co) oe_ram-	(MM) we_cx-
(Cm) j1_p2_rxd|txd	(Co) onbrd-	(MM) we_map-
(Cm) j1_p2_txd|rxd	(Cm) p2_rxd	(MM) we_mapl-
(Bu) j2_as	(Cm) p2_txd	(MM) we_mapu-
(Bu) j2_halt	(Co) parerr-	(MM) we_mapx-
(Bu) j2_in0:15	(Co) parerrl	(Co) we_raml-
(Bu) j2_r-|w1	(Co) parerru	(Co) we_ramu-
(Co) lds-	(Co) parl-	(Co) wir-
(Co) lperr-	(Co) paru-	(MM) xa0:11
(Hs) m_a0:7	(MM) prot0:3	(Mu) xack
(Hs) m_cs5-	(Co) prtyenab	(Cm) xca:b
(Hs) m_d0:15-	(Co) r-|w	
(Co) m_dil-	(Co) reset	
(Co) m_diu-	(Co) reset-	
(Co) m_dol-	(Co) rfenab	
(Co) m_dou-	(Cm) rtsb-	
(Hs) m_lds-	(Cm) rtsb--	
(Hs) m_ma17:23	(Cm) rxda	
(Hs) m_perr-	(Cm) rxdb	
(Hs) m_preq-	(Co) r|w-	
(Hs) m_rfenab	(Cm) sa:d	

Symbols Used:

Bu - Buses
Cm - Communications
Co - Commands
Dv - Devices
Hs - Highspeed
MM - Memory Management
Mu - Multibus

4.1. Buses

The following names are organized to describe onboard 'bus' signals. Multibus and Highspeed Bus names are described in separate sections.

General Bus Names:	
a0	Produced by latching lds- with cs4.
a1-	Inverted 68000 a1, for Map Long words.
a1:a23	68000 Address Bus.
d0:15	68000 Data Bus.
J2_as	68000 Address Strobe, Hi true command for parallel Port
J2_halt	Signal for LED Halt indicator
J2_in0:15	Hi true data bus for Parallel Port
J2_r-|w1	Read (low) Write (Hi) command for Parallel Port
oe_port-	Chip Enable for the Parallel Port
vcc|a14	Select High Address 14 for PROMS.
vcc|a15	Select High Address 15 for PROMS.

4.2. Commands

The following names describe the majority of Command and Control signals used by the 68000 and by all other logic onboard.

Command Names:	
as	68000 Address Strobe
as-	
berr-	Bus Error to the 68000
berrx-	Bus Error Extention
boot	Boot State register
c100	System Clock at 10 Mhz
c200	Timer Clock at 5 Mhz
c400	UART Clock at 2.5 Mhz
c800	1.25 Mhz Clock
c50	Raw Crystal output at 19.6608 Mhz
c50-	Inverted and delayed Crystal
c50--	Inverted and delayed Crystal
c_refresh	Timer output producing INT7
c_timer1	Watchdog Timer output produces Reset when low
c_timer2	User Programmable Timer output produces INT6
carry	Carry from System Clock counter
cas0:1-	Column Address Strobe for Onboard Ram
ckberr	Clock Bus Error. Invertec berr-
clrboot-	Clear Boot. See PALP0.
cs3:10	Clock States cs3, cs4, ... cs10
cs3-	Inverted cs3. Produces RAS to local Rams.
cs4-	Inverted cs4. Multiplex control for Ram Addreses.

Command Names cont'd:	
cswait-	Clock State Wait. Makes the Clock State generator wait before cs4 sets generated. See PALP3 for eqns.
ds	Data Strobe (High true). Produced by lds- OR uds-.
dtack-	Data Transfer Ack. to the 68000. See PALP2 for eqns.
enabto enabto-	Enable Timeout Generator. See PALP3 for eqns.
enlperr-	Enable Latched Parity Error. If 'low' when goes away, then a Parity Error in Onboard Ram has occured. See PALP1 for eqns.
fc0:2	68000 Function Codes: 2 1 0 0 0 0 Undefined 0 0 1 User Data 0 1 0 User Program 0 1 1 Undefined 1 0 0 Undefined 1 0 1 Supervisor Data 1 1 0 Supervisor Program 1 1 1 Interrupt Ack

Command Names cont'd	
halt	
halt-	68000 halt signal
hardreset	
hardreset-	
hyst	Power level hysterises
init	
init-	
int0:7-	Interrupts allowed to be latched
int1s:7s-	Latched Interrupts to encoded to the 68000
int_sio-	O.C interrupt from the UART
int_sio--	Buffered
int_sio---	Select UART Interrupt to INT5
int_timer2-	Select c_timer2 to INT6
ipl0:2-	68000 Interrupt Priority bits

Command Names cont'd:	
lds-	68000 Lower Data Strobe
lperr-	Latched Parity Error. Latched when enlperr- was asserted on an Onboard Ram access, indicating a Parity Error. This signal will be gated with the Parity enable line in PALP1 to generate parerr-.
m_dil-	Lower Byte Parity input
m_diu-	Upper Byte Parity input
m_dol-	Lower Byte Parity output
m_dou-	Upper Byte Parity output
mcas0:1-	Buffered cas0:1- to drive Onboard Ram CAS pin.
mras-	Buffered cs3- to drive Onboard Ram RAS pin.
mweraml-	Buffered weraml- to drive Onboard Ram WRITE Low Byte pin.
mweramu-	Buffered weramu- to drive Onboard Ram WRITE High Byte pin.
nc	No Connect.
oe_ram-	Device Select for enabling Onboard Ram data drivers.
onbrd-	Onboard Access Enabled. See PALP1 for eqns.

Command Names cont'd:	
parerr-	Parity Error. See PALP1 for eqns. Generates berr- when either an Onboard Ram access or Highspeed bus access has reported a Parity Error. See PALP2 for its use.
parerrl	Output of Low Byte Parity checker. High true
parerru	Output of High Byte Parity checker. High true
parl-	9th bit into Low Parity generator/checker. Always Low when writing, follows m_dol (inverted) when reading.
paru-	9th bit into High Parity generator/checker. Always Low when writing, follows m_dou (inverted) when reading.
prtyenab	Parity Error Enable bit in the Context Register. When low, PALP1 disables parerr- from going active.

Command Names cont'd:	
r-lw	Inverted 68000 rlw- for PROMs direction
reset	
reset-	68000 hardware Reset
rfenab	Refresh Enable bit in the Context Register. Buffered to the Highspeed bus, this allows a Highspeed bus target board to override Address compare with the intention of refreshing Dynamic Rams through the system. Boards with Static Rams as their Dual Ported memories can ignore this.
rlw-	68000 Read (Low) Write (high) command signal
setinit-	Clock boot and issue hardware Reset.
sysacc-	System Access. See PALP0 for eqns. When High, a System Access is requested, mostly when 68000 address a23 is high. When low, a Managed Access is requested.
thr	Power Level threshold
timeout	Cycle Timeout Error.
uds-	68000 Upper Data Strobe
vpa-	Valid Peripheral Address - Interrupt ack only
we_raml- we_ramu-	Local Ram write enable. See PALP4.
wlr-	Inverted 68000 rlw-. Used for Multibus data

4.3. Communications

The followins names are related to serial communications onboard.

Communication Signals:	
c.p1:2	Baud rate Clocks for Port A and B
ctsb-	Clear to Send Port B
dcdb-	Carrier Detect Port B
dtrb- dtrb--	Data Terminal Ready Port B
j1_p1_rxd	Port A Receive
j1_p1_txd	Port A Xmit
j1_p2_cts	Port B Clear to Send
j1_p2_dcd	Port B Carrier Detect
j1_p2_dtr	Port B Data Terminal Ready
j1_p2_rts	Port B Request to Send
j1_p2_rxd|txd	Port B (Receive) or Xmit
j1_p2_txd|rxd	Port B (Xmit) or Receive

Communication Signals cont'd:	
p2_rxd	Selected Port B Receive
p2_txd	Selected Port B Xmit
rtsb-	Request to Send Port B
rtsb--	
rxda:b	Receive Data Port A and B
sa:d	Xmit chip slew rate inputs
txda:b	Xmit Data Port A and B
txda:b-	

4.4. Highspeed Bus

The followings names describe the Highspeed Bus.

Highspeed Bus Signals:	
m_a0:7	Multiplexed Dynamic Ram Addresses. See Table 7.
m_cs5-	Buffered Clock State 5 for valid CAS address.
m_d0:15-	Data Bus. Connected directly the the onboard Rams data lines.
m_lds-	Buffered 68000 lds-
m_ma17:23	Buffered Upper Manaaed Addresses
m_perr-	Parity Error
m_preq-	Processor Request. This signal indicates to the Target board that m_ma17:23 are valid to enable responding. See PALP3 for eans.

Highspeed Bus Signals cont'd:	
m_rfenab	Buffered Refresh Enable. Indicates that the Target board should override the Upper Manaded Address compare and start responding. This is to allow the refreshing of Dynamic Rams out on the Highspeed Bus at the same time that the Local Ram is refreshing.
m_r|w-	Buffered 68000 r|w-
m_uds-	Buffered 68000 uds-
m_wait-	Highspeed Wait. Indicates to the Processor board that the Target board is not ready to have the Multiplexed Ram addresses m_a0:7 switch to the upper address bits. This stops the Clock State generator from advancing by extending cswait-. m_wait- is not an acknowledge of valid address compare, but a command to wait until the Target board can CAS the upper address bits. See PALP3 for its use in creating cswait-.

4.5. Multibus

The following names describe the Multibus Command, Address, and Data lines as well as onboard signals that support them.

Multibus Signals:	
-12vdc -5vdc 12vdc	Power Supplies
b_a0:23-	24 bit Address bus
b_bclk-	Bus Arbitor Clock
b_bhen-	Byte High Enable
b_bprn-	Bus Priority In
b_bpro-	Bus Priority Out
b_brea- b_busy- b_cbra-	Multibus Master arbitration handshaking signals. Used only by IC A3 (8289). See chip specifications.
b_cclk-	Constant Clock
b_d0:15-	Data bus
b_inh1- b_inh2-	Not Used
b_init-	Reset

Multibus Signals cont'd:	
b_int0:7-	Interrupts
b_inta-	Not used
b_iorc- b_iowc-	IO Commands
b_mrdc- b_mwtc-	Memory Commands
b_xack-	Command Acknowledge
aen	Address Enable from 8289 arbitor (High true).
aen-	Address Enable from 8289 Arbitor (Low true).
bas-	Bus Address Strobe. This is the request to the 8289 arbitor to become the Multibus Master. Generated through PALP3, it corresponds to m_preq- but bil- is now in the 'bus' state.
bclk-	Bus Arbitor Clock into the 8289 chip.
bhen	Byte High Enable. Generated by lds- and uds- both true, that is, when a word access is requested.
cclk-	Constant Clock. Buffered 68000 System Clock c100.
ce_byte- ce_word-	Enable Byte and Enable Word.

Multibus Signals cont'd:	
cen-	Command Enable delay to gate on one of 4 Commands
cen1-	Physical output enable for the four (4) Multibus commands. cen1 won't be gated on until aen- from the 8289 arbitor is true.
d1aen d2aen d3aen	aen Delays 1, 2, and 3. Part of the Address, Data and Command delay register for the Multibus. These are the inputs to the next register element, from the previous elements' output.
den-	Data Enable delay to gate ce_byte- and ce_word-
gnd	Power Supply ground
iorc- iowc- mrdc- mwtc-	Commands to buffer to the Multibus.
vcc	Power Supply +5 Volts.
xack	Buffered Multibus Command Acknowledge

4.6. Devices

The following names describe Command Enables and related direction control lines for onboard devices.

Device Signal Names:	
ce_prom0:1-	Chip enable for the onboard PROM sockets. ce_prom1- corresponds to Virtual address 0xC80000. ce_prom0-, however, corresponds to two (2) address: 0x0 during Boot State only, and 0xC00000 when not in Boot State.
ce_sio-	Chip Enable for the UART, address 0xD00000.
ce_timer-	Chip enable for the Timer, address 0xD80000
devenab-	Enables the 1-8 decoder to drive the five (5) Device addresses.
iorc-	Used by the UART and the TIMER as well as the Multibus as the Read command.
iowc-	Used by the UART and the TIMER as well as the Multibus as the Write command.
pe_port-	Chip Enable for the Parallel Port, address 0x900000.

4.7. Memory Management

The followins names describe Memory Management Command and Control sisnals.

Memory Management Signals:	
bil-	Bus (High) or Local (Low) tas of the current Pase
ce_map-	Chip Enable for Map Rams, address 0x800000
ce_mapl- ce_mapu-	Chip enable for Upper and Lower Pase Map words.
cx0:1	Context bits latched in the Context Resister
dirty	Indicates Pase has been written to.
en_mapx-	Enable Map Extention. Allows IC H7 (multiplexor) to over-write Pase Map Status bits used and dirty. See PALP3 for eans.
iolm-	IO (High) or Memory (low) tas of the current Pase
ma12:23	Manased Addresses. Output of the Pase Map Rams. See Table 5 for translation to data bus scheme.
oe_cx-	Output Enable for Context Resister, address 0x880000
prot0:3	Protection Code entries into the Pase Map Rams. See Table 5 for translation to data bus scheme, and Appendix F for code that senerates smaperr-.

Memory Management Signals cont'd	
smaperr-	Map Error. See Appendix F for code.
used	Indicates Page has been accessed successfully.
we_cx-	Write command for Context Register, address 0x880000
we_map-	Write Enable for Map Rams, address 0x800000
we_mapl- we_mapu-	Write enables for Upper and Lower Page Map words.
we_mapx-	Write Map Extention. The write control to the Page Map Ram holding the four Page Status bits. See PALP3 for eans.
xa0:11	Page Rams physical addresses. See Table 4.

Appendix A - Jumper Options

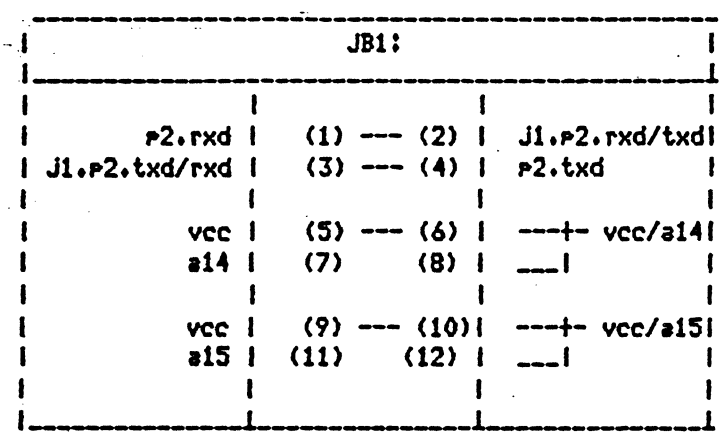
The following tables describe onboard Options available. The defaults (etched in on the circuit card) are shown as '(n) --- (n+1)'.

Appendix A.1 - JB1

This Jumper block allows selection of:

1) Serial Port B Transmit and Receive Pins on connector J1

2) Extended Addresses for the Prom sockets.



The communications default ultimately selects Pin 3 of the RS-232 connector as Receive, and Pin 2 as Transmit.

To swap Port B Transmit and Receive:

1) Cut (1) from (2) and (3) from (4).

2) Jumper (1) to (3) and (3) to (4).

The Prom addresses are defaulted for 2764 (8192 x 8) JEDEC devices.

To select 27128's:

1) Cut (5) from (6) and Jumper (7) to (8) together.

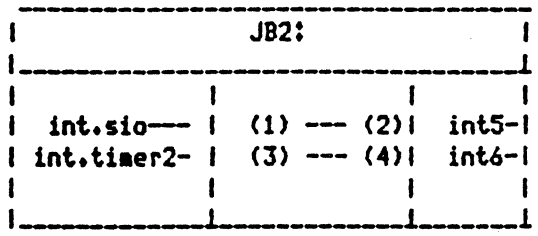
To select 27256's:

1) Cut (5) from (6) and Jumper (7) to (8) together.

2) Cut (9) from (10) and Jumper (11) to (12) together.

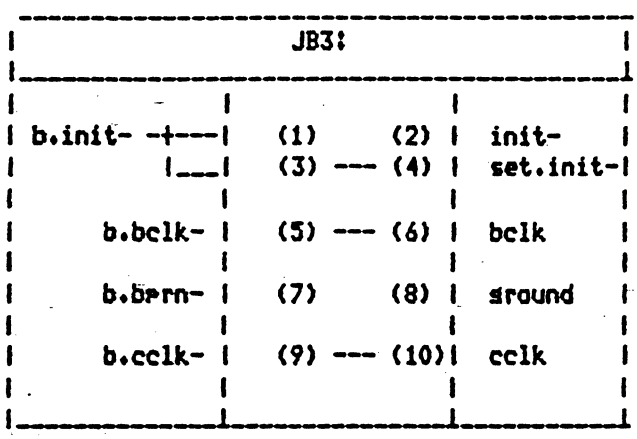
Appendix A.2 - JB2

Jumper JB2 sets the Interrupt level of the UART at INT 5 and sets the Timer Channel 2 to INT 6.



Appendix A.3 - JB3

Jumper JB3 selects various Multibus commands and controls.



The top 2 pairs select the source for the Multibus Reset signal b_init-. The default is for set.init- to drive it. This allows lets the external Reset Switch, Watchdog Timer and Power Level Comparator to reset the Multibus. The other option is to cut (3) from (4) and connect (1) to (2) together to source init- to the Multibus. This option will add the 68000's Reset instruction to the first three.

The third pair defaults the source of the Multibus Bus Arbitor clock b_bclk- to come from the Processor itself. If another device on the Multibus is selected to drive this signal, then you must cut (5) from (6).

The fourth pair default is Multibus Master Priority not at the Highest level. This option assumes one of the following:

1) There is a Higher Priority Bus Master in one slot above the Processor board in a Serial Priority scheme.

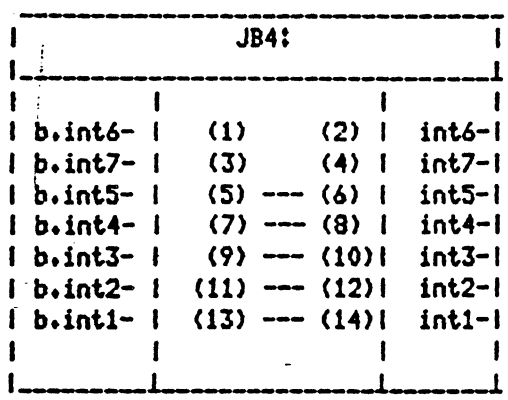
2) There is a Parallel Priority Scheme, one whose Arbitration is determined by logic on the Multibus motherboard.

For a Single Board configuration, or one that has the Processor as the Highest Priority Master, then you must Jumper (7) to (8) together.

The fifth pair defaults the source of the Multibus Constant Clock b_cclk- as the Processor itself. This clock is used by other Cadlinc Board products to synchronize Multibus and Highspeed bus timing with the Processor board and should not be cut. However, when more than one Procesor board is plugged into one card-case (for various reasons), then the Master Processor (the one that drives the Highspeed bus) should have this line intact and all of the others must cut (9) from (10).

Appendix A.4 - JB4

Jumper JB4 selects Interrupts from the Multibus. (Note that int6- and int7- are out of sequence at the top of the block.)



Interrupts int6- and int7- are not defaulted through because those levels on the Processor have predefined functions that should not change. If they are enabled, then the User must take care in handling the Refresh routines (int7-) and the Programmable Interrupt (int6-) so as not to conflict with the Processor.

Appendix B - Initial Memory Mapping

The CADLINC BASIC MONITOR will establish the following memory map.

The Page map preserves virtual addresses in all contexts, and allows all access types to all users for all addresses except the on-board RAM holding the 4014 emulator, which is protected against all user-state accesses but allows all supervisor-state accesses.

Virtual Low Addr	Bytes	Mapped to:	Physical Address	Normal Contents
000000	256	HS bus	000000	Pre-defined vectors
000100	256	HS bus	000100	RAM refresh routine
000200	512	HS bus	000200	Global data, rastor0
000400	3k	HS bus	000400	Supervisor stack
001000	252K or more, less emulator to max of 604K	HS bus	001000	All installed highspeed bus Ram
Top of ram HS to 097FFF	-	-	-	Invalid

Initial Processor Memory Map cont'd

Virtual Low Addr	Bytes	Mapped to:	Physical Address	Normal Contents
098000	32k	HS bus	(top of installed highspeed bus RAM) - 32k	4014 emulator code
0A0000	64k	MB I-O	0000	SMD Disk controllers, followed by Ethernet modules, extra serial I/O ports, timers, etc.
0B0000	64k	MB mem	FD0000	3Com ethernet modules
0C0000	128k	MB mem	FE0000	Raster Display Module
0E0000	128k	HS bus	7E0000	Floating Point Module

Initial Processor Memory Map cont'd

Virtual Low Addr	Bytes	Mapped to:	Physical Address	Normal Contents
100000	5M	HS bus	098000	Remaining highspeed bus RAM
600000	2M or 1920k	MB mem	000000	Multibus RAM, etc.
7E0000	128k	MB mem	FA0000	MltFunct board 0 proms, NVRAM
800000	512k	-	-	Page Map Registers
880000	512k	-	-	Context Register
900000	512k	-	-	Parallel I/O Registers

Initial Processor Memory Map cont'd

Virtual Low Addr	Bytes	Mapped to:	Physical Address	Normal Contents
980000	512k	-	-	Clear Boot State
C00000	512k	-	-	PROM 0
C80000	512k	-	-	PROM 1
D00000	512k	-	-	On-board UARTs
D80000	512k	-	-	On-board Timer
F80000	512k	-	-	VPA (not used by programs)

Initial Processor Memory Map cont'd

The standard physical address settings used by Cadlinc are as follows:

Address Range	Space	Module
000000 - 03FFFF	Local bus	On-board ram
040000 - FDFFFF	HS bus	Dual-ported ram; high-speed bus access
FE0000 - FFFFFF	HS bus	Floating Point Module

Address Range	Space	Int. Level	Module
000000 - 79FFFF (Maximum) top to next module	MB mem		Dual-ported ram, multibus access
	MB mem		Multibus ram
F80000 - F9FFFF	MB mem	-	MltFunct 1 , 2764's
F80000 - F8FFFF	MB mem	-	MltFunct 1 , 2732's
FA0000 - FBFFFF	MB mem	-	MltFunct 0 , 2764's
FA0000 - FAFFFF	MB mem	-	MltFunct 0 , 2732's
FD0000 - FD1FFF	MB mem	2	3Com ethernet module 0
FD2000 - FD3FFF	MB mem	2	3Com ethernet module 1
FD4000 - FD5FFF	MB mem	2	3Com ethernet module 2
FD6000 - FD7FFF	MB mem	2	3Com ethernet module 3
FE0000 - FFFFFF	MB mem	1**	Raster Display Module

Standard Physical Addresses - Memory

Note that all of the Floating Point Module is mapped; floating point operations are normally initiated in the logical processor partition at virtual address 0F0000. Due to module constraints, there is always a partition at this address.

Address range	Int	Module
00D0 - 00D1	3	CPC Tapemaster tape cntrl
__E0 - __E7	3 or 4	DTC-510A/DTC-86 disk cntrl 0
__E8 - __EF	3 or 4	DTC-510A/DTC-86 disk cntrl 1
__F0 - __F3	4	Interphase SMD-2180 disk cntrl 0
__F4 - __F7	4	Interphase SMD-2180 disk cntrl 1
00F8 - 00FB	4	Interphase SMD-2181 disk cntrl 0
00FC - 00FF	4	Interphase SMD-2181 disk cntrl 1
01_0 - 01_6	2**	3 Mbit Ethernet Module
0200 - 025F	1	Anti-aliased Raster Display Module
8000 - 801F	5	MltFunct board 0 i/o ports
8200 - 821F	5	MltFunct board 1 i/o ports
FF00 - FF7F	1	Dual-ported memory multibus parity flags/fault

Standard Physical Addresses - Multibus I-O

** - These interrupt levels are user-programmable; not Jumper selected; these are the default levels used.

Appendix C - Multibus Bus Pin Assignments (P1)

Mnemonic (IC Side)	Pin #	Pin #	Mnemonic (Solder Side)
gnd	1	2	gnd
vcc	3	4	vcc
vcc	5	6	vcc
12vdc	7	8	12vdc
-5vdc	9	10	-5vdc
gnd	11	12	gnd
b_bclk-	13	14	b_init-
b_bprn-	15	16	b_bpro-
b_busy-	17	18	b_breq-
b_mrdc-	19	20	b_mwtc-
b_iorc-	21	22	b_iowc-
b_xack-	23	24	b_inh1-
nc	25	26	b_inh2-
b_bhen-	27	28	b_a16-
b_cbrq-	29	30	b_a17-
b_cclk-	31	32	b_a18-
b_intq-	33	34	b_a19-
b_int6-	35	36	b_int7-
b_int4-	37	38	b_int5-
b_int2-	39	40	b_int3-
b_int0-	41	42	b_int1-
b_a14-	43	44	b_a15-
b_a12-	45	46	b_a13-
b_a10-	47	48	b_a11-
b_a8-	49	50	b_a9-
b_a6-	51	52	b_a7-
b_a4-	53	54	b_a5-
b_a2-	55	56	b_a3-
b_a0-	57	58	b_a1-
b_d14-	59	60	b_d15-
b_d12-	61	62	b_d13-
b_d10-	63	64	b_d11-
b_d8-	65	66	b_d9-
b_d6-	67	68	b_d7-
b_d4-	69	70	b_d5-
b_d2-	71	72	b_d3-
b_d0-	73	74	b_d1-
gnd	75	76	gnd
nc	77	78	nc
-12vdc	79	80	-12vdc
vcc	81	82	vcc
vcc	83	84	vcc
gnd	85	86	gnd

Appendix D - Highspeed Bus Pin Assignments (P2)

Mnemonic (IC Side)	Pin #	Pin #	Mnemonic (Solder Side)
m_preq-	1	2	m_wait-
m_ma20	3	4	m_ma23
m_r/w-	5	6	m_ma21
m_ma19	7	8	m_ma22
m_uds-	9	10	m_lds-
m_rfenab	11	12	m_cs5-
nc	13	14	m_ma18
m_perr-	15	16	m_ma17
m_d1-	17	18	m_d0-
m_d3-	19	20	m_d2-
nc	21	22	m_a0
m_d4-	23	24	nc
nc	25	26	m_d5-
m_a3	27	28	nc
m_d7-	29	30	m_d6-
nc	31	32	m_a1
nc	33	34	m_a6
m_d8-	35	36	m_d9-
m_a7	37	38	nc
nc	39	40	m_a2
m_d10-	41	42	m_d11-
gnd	43	44	gnd
nc	45	46	m_a4
m_d12-	47	48	m_d13-
nc	49	50	nc
nc	51	52	m_a5
m_d14-	53	54	m_d15-
b_a22-	55	56	b_a23-
b_a20-	57	58	b_a21-
nc	59	60	nc

Symbols used:
nc = No Connection
gnd = Ground

Appendix E - Communications and Parallel Ports

J1 Communication Port:				J2 Parallel Port:			
	1	2		J2.in0	1	2	gnd
J1.p1.txd	3	4		J2.in1	3	4	gnd
J1.p1.rxd	5	6		J2.in2	5	6	gnd
	7	8		J2.in3	7	8	gnd
	9	10		J2.in4	9	10	gnd
	11	12		J2.in5	11	12	gnd
gnd	13	14		J2.in6	13	14	gnd
	15	16		J2.in7	15	16	gnd
	17	18		J2.in8	17	18	gnd
	19	20		J2.in9	19	20	gnd
	21	22		J2.in10	21	22	gnd
	23	24		J2.in11	23	24	gnd
	25	26		J2.in12	25	26	gnd
	27	28	J1.p2.txd/rxd	J2.in13	27	28	gnd
	29	30	J1.p2.rxd/txd	J2.in14	29	30	gnd
	31	32	J2.p2.rts	J2.in15	31	32	gnd
	33	34	J2.p2.cts	oe.port-	33	34	gnd
	35	36			35	36	gnd
	37	38	gnd		37	38	gnd
J1.p2.dtr	39	40			39	40	gnd
	41	42		w/r-	41	42	gnd
	43	44		J2.as	43	44	gnd
	45	46		set.init-	45	46	gnd
	47	48		J2.halt-	47	48	gnd
	49	50		vcc	49	50	gnd

Appendix F - Protection PROM Code

```
/* Protection Prom for Enhanced Processor */
/*  21-JAN-83   George Kiewicz     Changed state of sysacc_i  */

#include <cad68/prom1.h>

#define prot1 a2
#define prot2 a8
#define prot3 a1
#define prot0 a0
#define sysacc_i                a7
#define fc1                     a5
#define fc0                     a4
#define read  a3
#define fc2                     a6

#define prot  (prot0*d0 + prot1*d1 + prot2*d2 + prot3*d3)
#define sys_access  (sysacc_i)
#define execute_cycle  (fc1 && !fc0 && read)
#define read_cycle     (!fc1 && fc0 && read)
#define write_cycle    (!fc1 && fc0 && !read)

char protcode[16][7] =
            {
                                0  '______',
                                1  '__x___',
                                2  'r_____',
                                3  'r_x___',
                                4  'rw____',
                                5  'rwx___',
                                6  'r__r__',
                                7  'rw_r__',
                                8  'r__rw_',
                                9  'rw_rw_',
                                a  'rw_r_x',
                                b  'rw_rwx',
                                c  'r_xr_x',
                                d  'rwxr_x',
                                e  'rwx__x',
                                f  'rwxrwx'
            } ;
```

```
smaperr(add)
int add;
{
        int res = 0;

        res |= (fc2 && read_cycle && (protcode[prot][0] == 'r'))?1:0;
        res |= ( fc2 && write_cycle && (protcode[prot][1] == 'w'))?1:0;
        res |= (fc2 && execute_cycle && (protcode[prot][2] == 'x'))?1:0;
        res |= (!fc2 && read_cycle && (protcode[prot][3] == 'r'))?1:0;
        res |= (!fc2 && write_cycle && (protcode[prot][4] == 'w'))?1:0;
        res |= (!fc2 && execute_cycle && (protcode[prot][5] == 'x'))?1:0;
        res = (res && !sys_access)?1:0;
        return(res);
}

main()
{
        size(512);
        prom(d4,0);
        prom(d5,0);
        prom(d6,smaperr(add));
        prom(d7,!smaperr(add));
        prologblast;
}
```

Appendix G - PAL Codes

The Series 80A Processor makes extensive use of PALs (Programmable Array Logic I.C.) to perform most of the necessary discrete logic. Each PAL is coded to use its inputs as elements of a logic equation, in either '1' state or '0' state, logically 'anded' into 'product' lines that can be 'ored' with as many as 6 more 'product' lines. The tri-state output can be controlled by an 8th 'product' line. Six of the eight outputs can be fed-back into the internal matrix and used as more input elements. Two pins are then dedicated as outputs only, and ten as inputs only.

PALs give the Processor great flexibility by eliminating a great many discrete I.C.s and consolidating their functions into a small number of programmable chips. Board layout is aided by the mostly arbitrary pin assignment structure, which can be better manipulated by firmware than by artwork.

The following pages are the logic equations for the individual PALs on board the Series 80A Processor. The format here is as the Structured Design SD20/24 PAL programmer requires, called PALASM. Some mnemonics have been abbreviated for clarity and all are in upper-case letters.

One type of PAL chip is used for all 5 Processor PALS, the PAL16L8-A, and programmed with individual code. All equations are evaluated to yield 'low true' results. This reduces the requirement for extra logic inverters since most IC's with control signals are 'low true' anyway. A few mnemonics, e.g. DS, SYSACC and BHEN, are written for a 'high true' output, so their logic equations tend not to be as straightforward as the others. The logic symbols used are:

'/' When mnemonic is low true, otherwise high true.
'*' Logical AND.
'+' Logical OR.
'=' When Right side of equation is true, make the Left mnemonic low.

Appendix G.1 - PALP0

PAL16L8

```
palp0    prod 3   rev 0.0   george kiewicz

system control pal
cadlinc, inc.;  55 park st.;  troy, mich   48083

rw as fc2 boot a23 a22 a21 a20 ds gnd

a19 clrboot oecx devenab cemap oeport wemap wecx sysacc vcc

/sysacc=as + /as * /boot * /a23
       +/as * boot * /rw * /a23

/cemap=fc2 * ds * a23 * /a22 * /a21 * /a20 * /a19

/wemap=fc2 * ds * a23 * /a22 * /a21 * /a20 * /a19 * /rw * /as

/oecx=fc2 * ds * a23 * /a22 * /a21 * /a20 * a19 * rw

/wecx=fc2 * ds * a23 * /a22 * /a21 * /a20 * a19 * /rw * /as

/oeport=fc2 * ds * a23 * /a22 * /a21 * a20 * /a19

/clrboot=fc2 * ds * a23 * /a22 * /a21 * a20 * a19 * /rw * /as

/devenab=fc2 * ds * a23 * a22
        +fc2 * ds * /a23 * /a22 * /a21 * /a20 * /a19*boot*rw

description
18-apr-83  changing -oeport- to read-write, and changing -clrboot-
           address to 0x980000.
sysacc changed to high for system, low for managed  20-Jan-83

system addresses:
800000 - pagemap registers  r-w
880000 - context register   r-w
900000 - parallel port      r-w
980000 - clear boot         w
c00000 - prom 0             r
c80000 - prom 1             r
d00000 - uart               r-w
d80000 - timer              r-w
f80000 - hardware vpa       not used by software
```

Appendix G.2 - PALP1

PAL16L8

```
palp1  prod 5   rev 0.0   george kiewicz

parity control
cadlinc inc, 55 park st., troy,, mich.  48083

oeram bl ma20 ma22 ma19 mperr prtyenab parerru parerrl gnd
lperr enlperr parerr onbrd ma18 rw ma21 ma23 wr vcc

/onbrd = /ma18 * /ma19 * /ma20 * /ma21 * /ma22 * /ma23 * /oeram

/wr = rw

/enlperr = /onbrd * /oeram * parerru * rw
         + /onbrd * /oeram * parerrl * rw

/parerr = /lperr * prtyenab
        + /mperr * prtyenab

description
version 2 of parity implementation.
version 4 of parity stuff for the box (sorry, don).  trying bl in
  generating /onbrd to avoid getting /cas during multibus access.
  16-mar-83
version 5  getting rid of /bl in /onbrd ad replacing with /oeram.
  18-mar-83
```

Appendix G.3 - PALP2

```
PAL16L8

palp2    prod 5   gak

bus status

cadlinc, inc.,  55 park st., troy mich    48083

bl parerr smaperr lds timeout uds sysacc aen cs5 gnd
cs10 bhen xack ds berrx iom dtack fc2 berr vcc

/berr = cs5 * ds * sysacc * /fc2
      + cs5 * ds * /parerr
      + cs5 * ds * /sysacc * /smaperr
      + ds * timeout
      + cs5 * ds * /sysacc * iom * /bl

/berrx = timeout
       + /parerr
       + /smaperr
       + iom * /bl * ds

/dtack = cs5 * sysacc * cs10
       + cs5 * /sysacc * /iom * /bl * berrx
       + cs5 * /sysacc * bl * iom * /aen * xack * berrx * cs10
       + cs5 * /sysacc * bl * /iom * /aen * xack * berrx
       + cs5 * /dtack * berrx

/ds = lds * uds

/bhen = lds + uds

description
11-may-83   qualify -dtack- with -cs10- during a multibus io access
            only. multibus memory is unchanged.
28-mar-83   latched dtack with cs5.  also insert berrx into dtaack.
generate bus controls dtack and berr for the 68000
on clockstate cs5, sysacc, and error info.

also produce data strobe -ds- and multibus byte high enable -bhen-
from 68000 data strobes -lds- ad -uds-.

sysacc sense changed. high for system, low for managed. 20-Jan-83.
```

Appendix G.4 - PALP3

PAL16L8

```
palp3   prod 6   george kiewicz

request and wait generators
cadlinc, inc.,  55 park st.,   troy, mich   48083

bl as smaperr cs6 c100 wempl aen cs3 cs4 gnd
mwait mpreq bas wempx enablto cswait boot a23 enpx vcc

/wempx = /wempl * /as
       + cs6 * smaperr * /as

/enpx = cs6 * smaperr

/cswait = /as * /a23 * /c100 * /cs4 * /boot
        + /as * /a23 * /bl * /mwait * /cs4 * /boot
        + /as * /a23 * bl * aen * cs3 * /cs4 * /boot

/enablto = /as * /a23 * /bl
        + /as * /aen * bl * /a23

/mpreq = /as * /a23 * /bl * /boot * cs3

/bas = cs3 * /a23 * bl * /boot

description
23-may-83  remove -cs3- from -cswait equation. this allows for a
    sloppier -as- to synchronize back to generate -cs3- on a low
    state of -c100-. initially to fix fluke inability to access
    dual port memory, this will also clean any marginal 68000 parts
    whose timings are at the long end of the spec.
12-may-83
    add -aen- and -bl- into equation for -cswait- to squeeze out
    a bit more time for multibus accesses.
produce highspeed bus request -mpreq- and multibus
request -bas- only during a managed access (/a23).

generate -cswait- to insert a wait when the highspeed bus
is not ready (mwait).
4-mar   improve -enabto- generation on managed request to multibus
```

Appendix G.5 - PALP4

PAL16L8

```
palp4   prod 4    gak

multibus, local ram and io read-write controls
cadlinc

sysacc iom bl rw berrx cs6 lds uds cesio gnd
cetimer mwtc dtack weramu oeram weraml iowc iorc mrdc vcc

/mwtc = cs6 * /rw * bl * /iom * berrx * /sysacc * /lds
      + cs6 * /rw * bl * /iom * berrx * /sysacc * /uds

/mrdc = cs6 * rw * bl * /iom * berrx * /sysacc * /lds
      + cs6 * rw * bl * /iom * berrx * /sysacc * /uds

/iorc = cs6 * rw * bl * iom * berrx * /sysacc * /lds
      + cs6 * rw * bl * iom * berrx * /sysacc * /uds
      + cs6 * rw * sysacc * /cetimer * /lds
      + cs6 * rw * sysacc * /cetimer * /uds
      + cs6 * rw * sysacc * /cesio * /uds

/iowc = cs6 * /rw * bl * iom * berrx * /sysacc * /lds * dtack
      + cs6 * /rw * bl * iom * berrx * /sysacc * /uds * dtack
      + cs6 * /rw * sysacc * /cetimer * /lds
      + cs6 * /rw * sysacc * /cetimer * /uds
      + cs6 * /rw * sysacc * /cesio * /uds

/oeram = /bl * /iom * berrx * /sysacc * /lds
       + /bl * /iom * berrx * /sysacc * /uds

/weramu = /rw * /bl * /iom * berrx * /sysacc * /uds

/weraml = /rw * /bl * /iom * berrx * /sysacc * /lds

description
28-mar-83   added dtack to multibus writes to turn command off.
            also swapped pins 12 and 13 to make room for dtack.
sysacc sense changed to high for system, low for managed.
```

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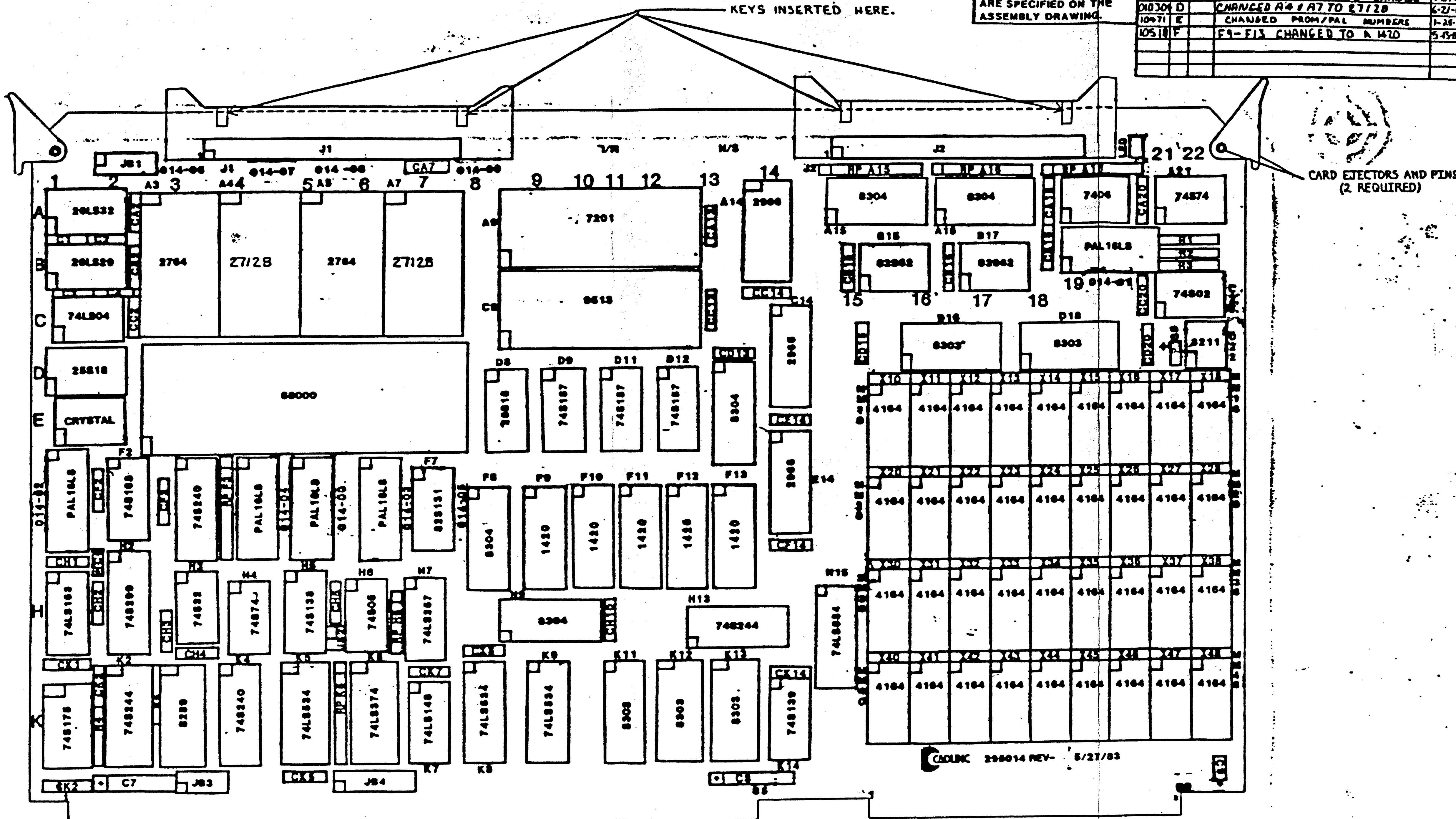
Mail to:

CADLINC Inc.
55 Park St.
Troy, MI 48083

SCHEMATIC DRAWING	E
DETAIL DRAWING	D
PARTS LIST	F

THE SCHEMATIC DRAWING, DETAIL DRAWING AND PARTS LIST REV. LEVELS ARE SPECIFIED ON THE ASSEMBLY DRAWING.

2005	A		RELEASED	5/10/83	MC
10190	B		ADDED REVISION LEVEL REFERENCE	7/26/83	JM
010260	C		ADDED CONNECTORS J1 & J2	3/5/84	JM
10244	C1		CHANGE IN DETAIL DRAWING		JM
010266	C2		BAD ECO # FOR REV C ABOVE	4-3-84	JN
010271	C3		SCHEMATIC DRAWING CHANGE	4-27-84	JN
010304	D		CHANGED A4 & A7 TO 27128	6-21-84	JN
10471	E		CHANGED PROM/PAL NUMBERS	1-25-85	JGM
10518	F		F9-F13 CHANGED TO A 1420	5-15-85	JM



NOTES:

1. LEAD SPACING OF ALL DISCRETE RESISTORS IS 0.50".
2. SEE BOX FOR HEADER STRIP BREAK REQUIREMENTS
3. CRYSTAL IS TO BE HAND SOLDERED AFTER WAVE SOLDERING.

COMPONENT	PIN ARRANGEMENT
JB1	2X6
JB2	2X2
JB3	2X5
JB4	2X8

MATERIAL	SEE PARTS LIST
FINISH	
CADLINC	TROY, MICHIGAN 48084
DRAWN BY	JGM
CHECKED BY	GAK
APPROVED	GAK
DATE	6/1/83
SHEET NO	1 OF 1
SCALE	2X
TITLE	ENHANCED 68000 PROCESSOR ASSEMBLY DRAWING
DRAWING NO	AD295014
REV	F

DOC	REV	ZONE	DESCRIPTION	DATE	APPROVED
8005	A		RELEASED	6/1/83	MK
10137	B		PULL UP H6-13 WITH RPH6-6	3/2/83	RA
010211	C		COMPATIBILITY W/II SLOT CARD CHGS	4-27-84	JN
10471	D		PAL/PROM PART NOS. CHANGE	4-22-85	JBM
10518	E		F9-F13 CHANGED TO 1420	5-13-85	JN

D3 — MC68000

D0	5	D0
D1	4	D1
D2	3	D2
D3	2	D3
D4	1	D4
D5	64	D5
D6	63	D6
D7	62	D7
D8	61	D8
D9	60	D9
D10	59	D10
D11	58	D11
D12	57	D12
D13	56	D13
D14	55	D14
D15	54	D15
A1	29	A1
A2	30	A2
A3	31	A3
A4	32	A4
A5	33	A5
A6	34	A6
A7	35	A7
A8	36	A8
A9	37	A9
A10	38	A10
A11	39	A11
A12	40	A12
A13	41	A13
A14	42	A14
A15	43	A15
A16	44	A16
A17	45	A17
A18	46	A18
A19	47	A19
A20	48	A20
A21	50	A21
A22	51	A22
A23	52	A23
AS\	6	AS\
UDS\	7	UDS\
LDS\	8	LDS\
R/W\	9	R/W\
FC0	28	FC0
FC1	27	FC1
FC2	26	FC2
GND	53	GND
GND	16	GND

DTACK\	10	DTACK\
IPL0\	25	IPL0\
IPL1\	24	IPL1\
IPL2\	23	IPL2\
VCC	13	BR\
VCC	12	BGK\
VCC	14	
VCC	49	
VPA\	21	VPA\
C100.50	15	CLK
BERR\	22	BERR\
HALT\	17	HALT\
RESET\	18	RESET\

74S157 — D9, D10, D11, D12

CX0.1X1	2	
A13	3	
A13	5	
A3	6	
A12	11	
A2	10	
A14	14	
A4	13	
A16	2	
AC	3	
A15	8	
A5	6	
A22 CX11	11	
A12	10	
A21	14	
A11	13	
A17	2	
A7	3	
A18	5	
A8	6	
A19	11	
A9	10	
A20	14	
A10	13	
SYS ACC\		

IMS1420-40 — F13, F12, F11, F10, F9

XA11	1	4			
XA10	7	4			
XA9	5	8			
XA8	12	3			
XA7	4	6			
XA6	7	5			
XA5	5	7			
XA4	12	8			
XA3	4	17			
XA2	7	16			
XA1	9	19			
XA0	12	18			
WE.MAPU\	11	WE			
MA19	12				
MA18	13				
MA17	14				
MA16	15				
MA15	13				
MA14	14				
MA13	15				
MA12	16				
MA23	12				
MA22	15				
MA21	13				
MA20	14				
WE MAPX\	11				
USED	12				
DIRTY	13				
B/L\	14				
IO/M\	15				
WE MAPU\	11				
PROT3	12				
PROT2	13				
PROT1	14				
PROT0	15				
WE		1	4	2	3
I/O		6	5	7	8
I/O		9	9	6	17
I/O		8	9	5	16
I/O		17	9	7	19
I/O		16	8	8	18

014-00 — F5 — PAL16L8A

A19	11	
A20	8	
A21	7	
A22	6	
A23	5	
FC2	3	
BOOT	4	
R/W\	1	
DS	9	
AS\	2	
SYS ACC\		19
CE.MAP\		18
WE.MAP\		17
OE.CX\		13
WE.CX\		18
OE.PORT\		16
CLR BOOT\		12
DEVENAB		14

74S248 — F2

A1	4	
ENABLE TOI\	15	
AS\	15	
CS3	11	
BERR\	3	
CS4	8	
NC	4	
R/W\	17	
A1\		16
ENABTO		7
AS		5
CS3\		9
CKBERR		18
CS4\		12
NC		14
R/W		3
G1 G2		1 10

014-05 82S131 — F7 PROM

PROT0	5	
PROT1	7	
PROT2	11	
PROT3	6	
SYS ACC\	15	
FC1	2	
FC0	3	
FC2	1	
R/W\	4	
SMAPERR\		10
N.C.		9
N.C.		11
N.C.		12
E		13

74LS257 — H7

VCC	16	
VCC	5	
IO/M\	11	
B/L\	14	
VCC	5	
DIRTY	6	
IO/M\	10	
B/L\	15	
R/W\	1	
EN.MAPX\		
USED		4
DIRTY		7
IO/M\		9
B/L\		12
OE		15

74S138 — H5

VCC	6	
A21	3	
A22	2	
A15	1	
CE.PROM\		15
CE.PROM1\		14
CE.SIO\		13
CE.TIMER		12
NC		11
NC		10
NC		9
VPA\		7

25LS2518 — D8

D15	4	
D14	1	
D13	10	
D12	13	
WE.CX\		9
OE.CX\		7
RFENAB		5
PRTYENAB		2
CX1		11
CX0		14
D15		6
D14		3
D13		12
D12		15

014-04 — F4 — PAL 16L8A

R/W\	4	
D/A\	3	
IO/M\	2	
SYS ACC\	1	
LDS\	7	
UDS\	8	
CE.TIMER\	11	
CE.SIO\	9	
BERR\	5	
CS6	6	
DTACK\	13	
MWTC\		12
MRDC\		19
IOWC\		17
IORC\		18
OE.RAM\		13
WE.RAMU\		16
WE.RAML\		14

F8

D0	14	
D1	12	
D2	13	
D3	15	
PROT0		6
PROT1		8
PROT2		5
PROT3		7

CE.MAPU\ — F9

D0	16	
D1	17	
D2	18	
D3	19	
D4	12	
D5	14	
D6	13	
D7	15	
MA12		1
MA13		3
MA14		4
MA15		2
MA16		8
MA17		6
MA18		7
MA19		5

8304

D13

D8	13	
D9	14	
D10	12	
D11	15	
D12	16	
D13	17	
D14	18	
D15	15	
CE.MAPL\		9
R/W\		
MA20		7
MA21		6
MA22		8
MA23		1
IO/M\		4
B/L\		3
DIRTY		2
USED		5

74S32 H3

CE.MAP\	2	
A1\	1	
		3 CE.MAPL\
	9	
A1	10	
		8 CE.MAPU\
WE MAP\	5	
A1\	4	
		6 WE.MAPL/
	12	
A1	13	
		11 WE.MAPU

S0295014

MATERIAL —
FINISH —
UNLESS OTHERWISE SPECIFIED TOLERANCES ON DIMENSIONS 2 PLACES ± .010 3 PLACES ± .005 ANGLES ± 2° BREAK ALL SHARP EDGES APPROX .005 REMOVE ALL BURRS

DO NOT SCALE

CADLINC
TROY, MICHIGAN 48084

DRAWN BY JOEL NETT
CHECKED BY
ENGINEER GAK
DATE 6/1/83
SHEET NO 1 OF 8
SCALE —

TITLE ENHANCED 68000 CPU & MEMORY MANAGEMENT.
SIZE C
DRAWING NO SD295014
REV E

DCO	REV	ZONE	DESCRIPTION	DATE	APPROVED
2005	A		RELEASED	6/10/83	MK
10137	B		PULL UP M6-13 WITH RPH6-6	7/12/83	RA
010271	C		SEE PAGE ONE	4-27-84	JN
10471	D		SEE PAGE ONE	4-23-85	JGM
10518	E		SEE PAGE ONE	5-15-85	JN

4164 DRAMS (36 TOTAL)

AM2966 A19: A8→1A1, A7→1A2, A1→1A3, A4→1A4, A5→2A1, A6→2A2, A3→2A3, A2→2A4; 1Y1→M.A7, 1Y2→M.A3, 1Y3→M.A1, 1Y4→M.A0, 2Y1→M.A6, 2Y2→M.A2, 2Y3→M.A4, 2Y4→M.A5; 1G, 2G → CS4

AM2966 L14: A10→1A1, A9→1A2, A11→1A3, MA14→1A4, MA15→2A1, MA13→2A2, MA12→2A3, MA16→2A4; 1Y1→M.A3, 1Y2→M.A0, 1Y3→M.A6, 1Y4→M.A2, 2Y1→M.A1, 2Y2→M.A7, 2Y3→M.A4, 2Y4→M.A5; 1G, 2G → CS4\

AM2966 E14: C93\→1A1, CAS1\→1A2, CAS0\→1A3, MA23→1A4, MA22→2A1, WERAM1\→2A2, WERAM0\→2A3, RFENAB→2A4; 1Y1→M.RAS\, 1Y2→M.CAS1\, 1Y3→M.CAS0\, 1Y4→M.MA23, 2Y1→M.MA22, 2Y2→M.WEL\, 2Y3→M.WEU\, 2Y4→M.RFENAB; 1G, 2G

74S139 K14: MA17→A, ONBRD\→B, G→M.CS5\; Y0→CAS0\, Y1→CAS1\, Y2, Y3

M14, M10, M20, M11, M21, M12, M22, M13, M23: M.A0, M.A1, M.A2, M.A3, M.A4, M.A5, M.A6, M.A7, VCC, M.WEL\, M.CAS0\, M.RAS\ → A0, A1, A2, A3, A4, A5, A6, A7, REF, WE, CAS, RAS

M34, M30, M40, M31, M41, M32, M42, M33, M43: M.A0, M.A1, M.A2, M.A3, M.A4, M.A5, M.A6, M.A7, VCC, M.WEL\, M.CAS1\, M.RAS\ → A0, A1, A2, A3, A4, A5, A6, A7, REF, WE, CAS, RAS

M.DIL\, M.DOL\ → M.D0\

M24, M15, M25, M16, M26, M17, M27, M18, M28: M.A0, M.A1, M.A2, M.A3, M.A4, M.A5, M.A6, M.A7, VCC, M.WEU\, M.CAS0\, M.RAS\ → A0, A1, A2, A3, A4, A5, A6, A7, REF, WE, CAS, RAS

M44, M35, M45, M36, M46, M37, M47, M38, M48: M.A0, M.A1, M.A2, M.A3, M.A4, M.A5, M.A6, M.A7, VCC, M.WEU\, M.CAS1\, M.RAS\ → A0, A1, A2, A3, A4, A5, A6, A7, REF, WE, CAS, RAS

M.DIU\, M.DOU\ → M.D8\

8303 D16: M.D0\→B0, M.D1\→B1, M.D2\→B2, M.D3\→B3, M.D4\→B4, M.D5\→B5, M.D6\→B6, M.D7\→B7, CS, AB; A0→D0, A1→D1, A2→D2, A3→D3, A4→D4, A5→D5, A6→D6, A7→D7

8303 D18: M.D8\→B0, M.D9\→B1, M.D10\→B2, M.D11\→B3, M.D12\→B4, M.D13\→B5, M.D14\→B6, M.D15\→B7, CS, AB; A0→D8, A1→D9, A2→D10, A3→D11, A4→D12, A5→D13, A6→D14, A7→D15

OE.RAM\, R/W\

74S244 H13: UDS\→1A3, LDS\→1A2, MA17→1A1, MA18→2A1, MA19→2A2, MA20→2A3, MA21→2A4, R/W\→1G, 2G; 1Y4→M.UDS\, 1Y3→M.LDS\, 1Y2→M.MA17, 1Y1→M.MA18, 2Y1→M.MA19, 2Y4→M.MA20, 2Y3→M.MA21, 2Y2→M.R/W\

295014

CADLINC, TROY, MICHIGAN 48084

DRAWN BY	PSK
CHECKED BY	JGM
ENGINEER	GAK
DATE	7/25/83
SHEET NO	2 OF 8
SCALE	
TITLE	ENHANCED 68000 PROCESSOR BOARD ON BOARD RAM
SIZE	C
DRAWING NO	SD295014
REV	E

DOC	REV	ZONE	DESCRIPTION	DATE	APPROVED
10518	E		SEE PAGE ONE	5-13-85	JN

DOC	REV	ZONE	DESCRIPTION	DATE	APPROVED
2005	A		RELEASED		
10137	B		PULL UP H6-13 WITH RPH6-6		
010271	C		SEE PAGE ONE	4-27-84	JN
10471	D		SEE PAGE ONE	6-21-85	JGM

014-06 2732/64/128/256 — A3
014-08 2732/64/128/256 — A5
014-07 2732/64/128/256 — A4
014-09 2732/64/128/256 — A7

VCC 1, VCC/15 27, VCC/14 26, A1 10, A2 9, A3 8, A4 7, A5 6, A6 5, A7 4, A8 3, A9 2, A10 24, A11 21, A12 23, A13 2
D0 11, D1 12, D2 13, D3 15, D4 16, D5 17, D6 18, D7 19
OE CE
CE.PROM0 22 20
CE.PROM1 22 20
R/W

RPA15 4.7K — 8304 A15
J2.IN0 19, J2.IN1 18, J2.IN2 17, J2.IN3 16, J2.IN4 15, J2.IN5 14, J2.IN6 13, J2.IN7 12
B0 B1 B2 B3 B4 B5 B6 B7 CS AB
A0 1, A1 2, A2 3, A3 4, A4 5, A5 6, A6 7, A7 8, AB 9, 11
D0 D1 D2 D3 D4 D5 D6 D7

RPA16 4.7K — 8304 A16
J2.IN8 19, J2.IN9 18, J2.IN10 17, J2.IN11 16, J2.IN12 15, J2.IN13 14, J2.IN14 13, J2.IN15 12
B0 B1 B2 B3 B4 B5 B6 B7 CS AB
A0 1, A1 2, A2 3, A3 4, A4 5, A5 6, A6 7, A7 8, AB 9, 11
D8 D9 D10 D11 D12 D13 D14 D15
OE.PORT\ 9
W/R\ 11

8289 — K3
BAS\ 18, PU 16, C100.50 17, CRQL\ 15, RESB 4, ANYR 14, IOB\ 2
S0\ 19, S1\ 1, S2\ LOCK\, CLK, INIT\, BCLK\, BREQ\, BPRN\, BPRO\, BUSY\, CBRQ\, SYSB, AEN\
B.INIT\ 6, B.BCLK\ 5, B.BREQ\ 7, B.BPRN\ 9, B.BPRO\ 8, B.BUSY\ 11, B.CBRQ\ 12, AEN\ 13

7406 — A19
AS\ 1 → 2 J2.AS
HALT\ 8, 74S02 C21 9, 10, 5 → A19 → J2.HALT
LED

74LS534 — K9
A5 3, A4 4, A6 7, A7 8, A3 13, A2 14, A1 17, A0 18
D1 D2 D3 D4 D5 D6 D7 D8, EN OE, 11 1
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
B.A5\ 2, B.A4\ 5, B.A6\ 6, B.A7\ 9, B.A3\ 12, B.A2\ 15, B.A1\ 16, B.A0\ 19

74LS534 — K8
MA12 3, MA13 4, MA14 7, MA15 8, A11 13, A10 14, A9 17, A8 18
B.A12\ 2, B.A13\ 5, B.A14\ 6, BA15\ 9, B.A11\ 12, B.A10\ 15, B.A9\ 16, B.A8\ 19

74LS534 — K5
BHEN 8, MA16 13, MA17 14, MA18 17, MA19 18
B.BHEN\ 9, BA16\ 12, B.A17\ 15, B.A18\ 16, B.A19\ 19

74LS534 — H15
MA23 3, MA22 4, MA21 7, MA20 8
B.A23\ 2, B.A22\ 5, B.A21\ 6, B.A20\ 9
C85 13, AEN\ 14

8303 — K13
B.D0\ 19, B.D1\ 18, B.D2\ 17, B.D3\ 16, B.D4\ 15, B.D5\ 14, B.D6\ 13, B.D7\ 12
B0 B1 B2 B3 B4 B5 B6 B7 CS AB
A0 1, A1 2, A2 3, A3 4, A4 5, A5 6, A6 7, A7 8, AB 9, 11
D0 D1 D2 D3 D4 D5 D6 D7

8303 — K11
B.D8\ 19, B.D9\ 18, B.D10\ 17, B.D11\ 16, B.D12\ 15, B.D13\ 14, B.D14\ 13, B.D15\ 12
B0 B1 B2 B3 B4 B5 B6 B7 CS AB
A0 1, A1 2, A2 3, A3 4, A4 5, A5 6, A6 7, A7 8, AB 9, 11
D8 D9 D10 D11 D12 D13 D14 D15
CE.WORD\ 9

8303 — K12
B.D0\ 19, B.D1\ 18, B.D2\ 17, B.D3\ 16, B.D4\ 15, B.D5\ 14, B.D6\ 13, B.D7\ 12
B0 B1 B2 B3 B4 B5 B6 B7 CS AB
A0 1, A1 2, A2 3, A3 4, A4 5, A5 6, A6 7, A7 8, AB 9, 11
D8 D9 D10 D11 D12 D13 D14 D15
CE.BYTE\ 9
R/W

C50
CLRAEN
MR CP, GO 15, GO\ 14 DBAS1, BAS1\ 13 D0 Q0 10 DBAS2, DBAS1\ 12 D1 Q1 11 DEN\, DBAS2 5 D2 Q2 4, 4 D3 Q3 6 CEN\, Q4 2, Q5 3
K1 74S175

K2 74S244
MWTC\ 2, MRDC\ 4, IORC\ 6, IOWC\ 8, CEN\ 11, 13, 15, 17, 16 2G, 1 18
1A1 1A2 1A3 1A4 2A1 2A2 2A3 2A4
1Y1 1Y2 1Y3 1Y4 2Y1 2Y2 2Y3 2Y4
B.MWTC\ 18, B.MRDC\ 16, B.IORC\ 14, B.IOWC\ 12, CEN1\ 9, 7, 5, 3
CEN1\, AEN\
470Ω R4

K4 74S240
CS5 2, 4, RESET 6, AEN\ 8, C100.50 11, 13, RESET 15, B.XACK\ 17, 1G 2G
1A1 1A2 1A3 1A4 2A1 2A2 2A3 2A4
1Y1 1Y2 1Y3 1Y4 2Y1 2Y2 2Y3 2Y4
M.CS5\ 18, 16, RESET 14, CLRAEN 12, CCLK\ 9, BCLK\ 7, INIT\ 5, XACK 3

PUC
H4 74S74 R
LDS\ 2, CS4 3, D S, CLK, Q 5, Q\ 8, R 4
A0
PUC

74S139 — K14
A0 2, DEN\ 3, AEN\
A Y0 4 CE.WORD\, Y1 5 CE.BYTE\, Y2 6, Y3 7, B, G 1

SD295014

DO NOT SCALE

UNLESS OTHERWISE SPECIFIED TOLERANCES ON DIMENSIONS 2 PLACES ± .010 3 PLACES ± .005 ANGLES ± 2° BREAK ALL SHARP EDGES APPROX .005 REMOVE ALL BURRS

MATERIAL
FINISH

CADLINC
TROY, MICHIGAN 48084

DRAWN BY	PSK
CHECKED BY	JGM
ENGINEER	GAK
DATE	7/25/83
SHEET NO	3 OF 8
SCALE	—

TITLE: ENHANCED 68000 PROCESSOR BOARD BUSS INTERFACE

SIZE C | DRAWING NO SD295014 | REV E

ECO	REV	ZONE	DESCRIPTION	DATE	APPROVED
10518	C		SEE PAGE ONE	5-15-85	JN
2005	A		RELEASED	6/10/83	MK
10137	B		PULL UP INT.SIO\ CH6-13 W/RPH6-6	7/12/83	RB
0102711	C		SEE PAGE ONE	9-27-84	JN
10471	D		SEE PAGE ONE	4-22-85	JGM

AM9513 C9 — 7201 A9 — 8211 D22 — 26LS29 B1 — 26LS32 A1 — 25S18 D1 — RPH6 SIP4.7K — RPA19 SIP4.7K — RPF3 SIP4.7K — 74LS04 C1 — 74LS05 H6 — 7406 A19 — 74S02 C21 — 74374 H4

DO NOT SCALE

MATERIAL	
FINISH	
UNLESS OTHERWISE SPECIFIED TOLERANCES ON DIMENSIONS 2 PLACES ± .010 3 PLACES ± .005 ANGLES ± 2° BREAK ALL SHARP EDGES APPROX .005 REMOVE ALL BURRS	

CADLINC
TROY, MICHIGAN 48084

DRAWN BY	PSK
CHECKED BY	JGM
ENGINEER	GAK
DATE	7/25/83
SHEET NO	4 of 8
SCALE	—

TITLE: ENHANCED 68000 PROCESSOR BOARD SIO-TIMER AND INT

SIZE	DRAWING NO	REV
C	SD295014	E

SD295014

DOC	REV	ECN#	DESCRIPTION	DATE	APPROVED
2005	A		EXPOSED	6/06	MK
10137	B		PULL UP H6-13 WITH RPH6-7	7/10	KA
010711	C		SEE PAGE ONE	4-27-84	JN
10471	D		SEE PAGE ONE	4-23-85	JN
10518	E		SEE PAGE ONE	5-13-85	JN

F2 74S163 — QA C100.50, QB C200.100, QC C400.200, QD NC. — PUA, PUB, ENAB T0, CARRY, LOAD, CLK, CL

H1 74LS163 — QA N.C., QB N.C., QC N.C., QD N.C. — CARRY 15 TIMEOUT

E1 19.6608 MHZ — C50

74LS04 C1 C1 — 4 C50\ — A3

H2 74S299 — CS WAIT\ — 7 CS3, 13 CS4, 6 CS5, 14 CS6, 5 CS7, 15 CS8, 4 CS9, 16 CS10

K6 74LS374 — INT7\ INT6\ INT5\ PU3 INT1\ INT2\ INT3\ INT4\ — 2 INT 7\, 6 INT 6\, 5 INT 5\, 2 N.C., 12 INT 1\, 15 INT 2\, 16 INT 3\, 19 INT 4\ — CLK OE — C100.50

B15 82S62 — D0 D1 D2 D3 D4 D5 D6 D7 PARL — INH — LDS\

B17 82S62 — D8 D9 D10 D11 D12 D13 D14 D15 PARU — INH — UDS\

74S02 C21 — W/R\ M.DEN — M.DIL\ — 5 PARERRL\

74S02 C21 — W/R\ M.DEU — 6 M.DIU\ — 9 PARERRU\

F1 D14-02 PAL16L8A — FC2 C310 TIMEOUT 10/M\ B/L\ SMAPERR\ PARERR\ AEN\ XACK\ SYSACK\ CS5 LDS\ UDS\ — 19 BERR\ 15 DERR\ 17 DTACK\ 13 DS 12 BHEN

B19 D14-01 PAL16L8A — MA18 MA19 MA20 MA21 MA22 MA23 PARERRU PARERRL OE.RAM\ M.PERR\ R/W\ PRTYENAB NC LPERR\ — 10 WR 12 PARERR 14 ONBRD\ 12 ONLPERR

A21 — AS\ — 5 LPERR\ — PRTYENAB — 74LS74

F6 D14-03 PAL16L8A — C100.50 CS3 CS4 CS6 D/L\ AS\ A23 SMAPERR WE.MAP\ M.WAIT\ AEN BOOT — 14 WE.MAP\ 13 EN.MAP\ 14 CS WAIT\ 15 ENABTO 12 M.PREQ 13 BAS

K7 74LS148 — GND INT1S\ INT2S\ INT3S\ INT4S\ INT5S\ INT6S\ INT7S\ BOOT — A0 A1 A2 — 9 IP1\ 7 IPU\ 6 IPL2\

+5v RPK.5 — INT 4\ INT 7\ INT 6\ INT 3\ INT 2\ INT 1\ PU 3 INT 1\ NC

MATERIAL ~	DRAWN BY JOEL NETT	TITLE ENHANCED 68000 CLOCK & CONTROL	
FINISH ~	CHECKED BY GAK		
UNLESS OTHERWISE SPECIFIED TOLERANCES ON DIMENSIONS 3-PLACES ± .014, 2-PLACES ± .030 ANGLES ± 2° BREAK ALL SHARP EDGES APPROX. .005 REMOVE ALL BURRS	ENGINEER GAK		
CADLINC TROY, MICHIGAN 48084	DATE 6/1/83	SIZE C	DRAWING NO. SD295014
	SHEET NO. 5 OF 8		REV. E
	SCALE ~		

ECO	REV	ZONE	DESCRIPTION	DATE	APPROVED
10518	E		SEE PAGE ONE	5-13-85	JV

ECO	REV	ZONE	DESCRIPTION	DATE	APPROVED
2005	A		RELEASED	6/6/83	MK
10137	B		PULL UP H6-6 WITH RPH6-6	7/12/83	RJ
10271	C		SEE PAGE ONE	4-27-84	JN
10471	D		SEE PAGE ONE	4-22-85	TLM

J1

	1	2	
J1.P1.TXD	3	4	
J1.P1.RXD	5	6	
	7	8	
	9	10	
	11	12	
GND	13	14	
	15	16	
	17	18	
	19	20	
	21	22	
	23	24	
	25	26	
J1.P2.TXD/RXD	27	28	
J1.P2.RXD/TXD	29	30	
J1.P2.RTS	31	32	
J1.P2.CTS	33	34	
	35	36	
GND	37	38	
J1.P2.DTR	39	40	J1.P2.DCD
	41	42	
	43	44	
	45	46	
	47	48	
	49	50	

J2.IN0	1	2	
J2.IN1	3	4	
J2.IN2	5	6	
J2.IN3	7	8	
J2.IN4	9	10	
J2.IN5	11	12	
J2.IN6	13	14	
J2.IN7	15	16	
J2.IN8	17	18	
J2.IN9	19	20	
J2.IN10	21	22	
J2.IN11	23	24	
J2.IN12	25	26	
J2.IN13	27	28	
J2.IN14	29	30	
J2.IN15	31	32	
OE.PORT\	33	34	
	35	36	
	37	38	
	39	40	
W/R\	41	42	
J2.AS	43	44	
SET.INT\	45	46	
J2.HALT\	47	48	
VCC	49	50	

JB1

P2.RXD	1	2	J1.P2.RXD/TXD
J1.P2.TXD/RXD	3	4	P2.TXD
VCC	5	6	VCC/A14
A14	7	8	
VCC	9	10	VCC/A15
A15	11	12	

JB3

B.INIT\	1	2	INIT\
	3	4	SET.INT\
B.BCLK\	5	6	B.CLK
B.BPRN\	7	8	GND
B.CCLK\	9	10	CCLK\

JB2

INT.910\	1	2	INT5\
INT.TIMER2\	3	4	INT6\

JB4

B.INT6\	1	2	INT6\
B.INT7\	3	4	INT7\
B.INT5\	5	6	INT5\
B.INT4\	7	8	INT4\
B.INT3\	9	10	INT3\
B.INT2\	11	12	INT2\
B.INT1\	13	14	INT1\
B.INT0\	15	16	INT0\

VCC+5 — 1 | 1 | 1 | 1

GND — 2 | .1µF | 2 | .1µF | 2 | .1µF | 2 | .1µF

CA2, CA13, CA20, CB13, CB18, CC2, CC20, CD13, CD15, CE14, CF3, CH9, CH3, CH10, CK3, CK7, CK14, X10, X12, X14, X16, X18, X23, X25, X27, X30, X32, X34, X36, X38, X41, X43, X45, X47 (36 TOTAL)

VCC+5 — 1 | C | 1 | C | 1 | C | 1 | C

GND — 2 | .001µF | 2 | .001µF | 2 | .001µF | 2 | .001µF

CA7, CA18, CB2, CB16, CC13, CC14, CD20, CF2, CF14, CH2, CH4, CH5, CK1, CK5, CK8, X11, X13, X15, X17, X20, X22, X24, X26, X28, X31, X33, X35, X37, X40, X42, X44, X46, X48. (35 TOTAL)

VCC+5V — + | C7 | + | C8 | + | C9

GND — − | 10µF | − | 10µF | − | 10µF

-5V — 1 | CR2 | − | C6

GND — 2 | .1µF | + | 10µF

SD295014

DO NOT SCALE

MATERIAL

FINISH

UNLESS OTHERWISE SPECIFIED
TOLERANCES ON DIMENSIONS
2 PLACES ± .010 3 PLACES ± .005
ANGLES ± 2°
BREAK ALL SHARP EDGES APPROX .005
REMOVE ALL BURRS

CADLINC
TROY, MICHIGAN 48084

DRAWN BY	PSK
CHECKED BY	JGM
ENGINEER	GAK
DATE	7/22/83
SHEET NO	6 OF 8
SCALE	

TITLE: ENHANCED 68000 PROCESSOR J CONNECTORS AND JUMPERS

SIZE: C | DRAWING NO: SD295014 | REV: E

MULTI-BUS
P1 CONNECTOR

	PIN	MNEMONIC	DESCRIPTION (COMPONENT SIDE)	PIN	MNEMONIC	DESCRIPTION (SOLDER SIDE)
POWER SUPPLIES	1	GND	SIGNAL GND	2	GND	SIGNAL GND
	3	+5V	+5VDC	4	+5V	+5VDC
	5	+5V	+5VDC	6	+5V	+5VDC
	7		+12VDC	8		+12VDC
	9	-5V	-5VDC	10	-5V	-5VDC
	11	GND	SIGNAL GND	12	GND	SIGNAL GND
BUS CONTROLS	13	B.BCLK\	BUS CLOCK	14	B.INIT\	INITIALIZE
	15	B.BPRN\	BUS PRI. IN	16	B.PRO\	BUS PRI OUT
	17	B.BUSY\	BUS BUSY	18	B.BREQ\	BUS REQUEST
	19	B.MRDC\	MEM. READ CMD	20	B.MWTC\	MEM WRITE CMD
	21	B.IORC\	I/O READ CMD	22	B.IOWC\	I/O WRITE CMD
	23	B.XACK\	XFER ACKNOWLEDGE	24		INHIBIT 1 (DISABLE RAM)
BUS CONTROLS AND ADDRESS	25	B.LOCK\	LOCK	26		INHIBIT 2 (DISABLE PROM)
	27	B.BHEN\	BYTE HIGH ENABLE	28	B.A16\	ADDRESS BUS
	29	B.CBRQ\	COMMON BUS REQUEST	30	B.A17\	
	31	B.CCLK\	CONSTANT CLK	32	B.A18\	
	33		INTR ACKNOWLEDGE	34	B.A19\	
INTERRUPTS	35	B.INT6\	PARALLEL	36	B.INT7\	PARALLEL
	37	B.INT4\	INTERRUPT	38	B.INT5\	INTERRUPT
	39	B.INT2\	REQUEST	40	B.INT3\	REQUEST
	41			42	B.INT1\	
ADDRESS	43	B.A14\	ADDRESS BUS	44	B.A15\	ADDRESS BUS
	45	B.A12\		46	B.A13\	
	47	B.A10\		48	B.A11\	
	49	B.A8\		50	B.A9\	
	51	B.A6\		52	B.A7\	
	53	B.A4\		54	B.A5\	
	55	B.A2\		56	B.A3\	
	57	B.A0\		58	B.A1\	
DATA	59	B.D14\	DATA BUS	60	B.D15\	DATA BUS
	61	B.D12\		62	B.D13\	
	63	B.D10\		64	B.D11\	
	65	B.D8\		66	B.D9\	
	67	B.D6\		68	B.D7\	
	69	B.D4\		70	B.D5\	
	71	B.D2\		72	B.D3\	
	73	B.D0\		74	B.D1\	
POWER SUPPLIES	75	GND	SIGNAL GND	76	GND	SIGNAL GND
	77		RESERVED, BUSSED	78		RESERVED: BUSSED
	79		-12VDC	80		-12V DC
	81	+5V	+5VDC	82	+5V	+5VDC
	83	+5V	+5VDC	84	+5V	+5V DC
	85	GND	SIGNAL GND	86	GND	SIGNAL GND

PINS NOT SUPPLIED WITH MNEMONICS ARE UNUSED

DWG	REV	ZONE	DESCRIPTION	DATE	APPROVED
2005	A		RELEASED	6/10/83	MK
10137	B		PULLUP H6-12 WITH RDH6-6	7/12/83	RB
10271	C		SEE PAGE ONE	4-27-84	JN
10471	D		SEE PAGE ONE	5-23-85	JGM
10518	E		SEE PAGE ONE	5-13-85	JN

MATERIAL

FINISH

UNLESS OTHERWISE SPECIFIED TOLERANCES ON DIMENSIONS 3 PLACES ± .010 2 PLACES ± .005 ANGLES ± 2° BREAK ALL SHARP EDGES APPROX .005 REMOVE ALL BURRS

DO NOT SCALE

CADLINC
TROY, MICHIGAN 48084

DRAWN BY	PSK
CHECKED BY	JGM
ENGINEER	GAK
DATE	7/25/83
SHEET NO	7 OF 8
SCALE	

TITLE: ENHANCED 68000 PROCESSOR BOARD MULTIBUS CONNECTIONS

SIZE: C | DRAWING NO: SD295D14 | REV: E

SD295D14

ECO	REV	ZONE	DESCRIPTION	DATE	APPR'D.
2005	A		RELEASED	6/16/83	MZ
10137	B		PULL UP R6-13 WITH RPH6-6	7-12-83	
010271	C		SEE PAGE ONE	4-27-84	JN
10471	D		SEE PAGE ONE	4-22-85	JDM
10518	E		SEE PAGE ONE	5-13-85	JN

P2
(COMPONENT SIDE)

PIN #	SIGNAL NAME
1	M.PREQ\
3	M.A20
5	M.R/W\
7	M.A19
9	M.UDS
11	M.REFENAB
13	N.C.
15	M.PERR\
17	M.D1\
19	M.D3\
21	N.C.
23	M.D4\
25	N.C.
27	M.A3
29	M.D7\
31	N.C.
33	N.C.
35	M.D8\
37	M.A7
39	N.C.
41	M.D10\
43	GND
45	N.C.
47	M.D12\
49	N.C.
51	N.C.
53	M.D14\
55	B.A22
57	B.A20
59	N.C.

P2
(SOLDER SIDE)

PIN #	SIGNAL NAME
2	M.WAIT
4	M.A23
6	M.A21
8	M.A22
10	M.LDS\
12	M.CSS
14	M.A18
16	M.A17
18	M.D0\
20	M.D2\
22	M.AS
24	N.C.
26	M.DS\
28	N.C
30	M.D6\
32	M.A1
34	M.A6
36	M.D9\
38	N.C.
40	M.A2
42	M.D11\
44	GND
46	M.A4
48	M.D13\
50	N.C
52	M.A5
54	M.D15\
56	B.A23
58	B.A21
60	N.C

MATERIAL ~

FINISH ~

UNLESS OTHERWISE SPECIFIED
TOLERANCES ON DIMENSIONS
2 PLACES ± .010 3 PLACES ± .005
ANGLES ± 2°
BREAK ALL SHARP EDGES APPROX. .005
REMOVE ALL BURRS

CADLINC
TROY, MICHIGAN 48084

DRAWN BY: JOEL NETT
CHECKED BY: GAK
ENGINEER: GAK
DATE: 6/1/80
SHEET NO.: H of 8
SCALE: ~

TITLE: ENHANCED HIGH SPEED P2 BUS CONNECTOR 68000 CPU

SIZE: D
DRAWING NO.: SD295014
REV.: E