

Equipment Diagrams

CONTROL DATA 8092
TELEPROGRAMMER

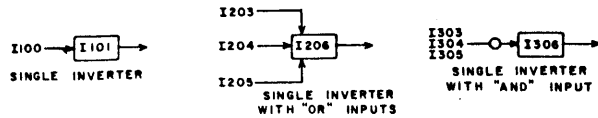
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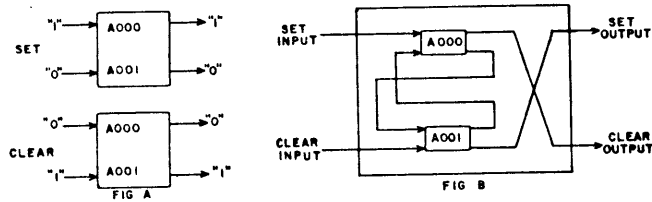
<u>Page</u>	<u>Title</u>
23	8092 Display
24	8092 Display
25	8092 Display
26	8092 Display

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47032300, sheet 1 of 4
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SINGLE INVERTER - A single inverter inverts input signals so that a "1" input results in a "0" output and a "0" input results in a "1" output. Inputs to symbols are identified by arrowheads.

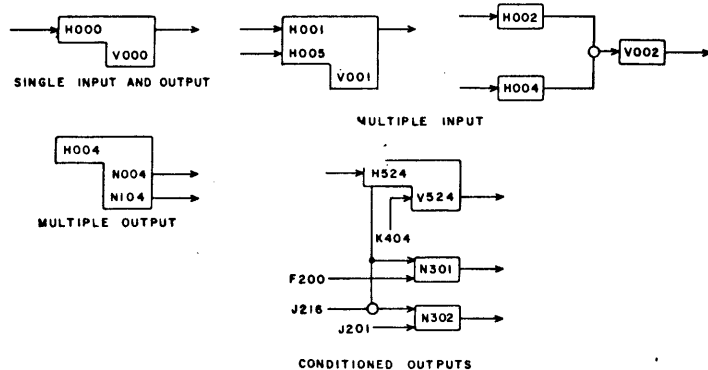


FLIP FLOP (FF) - The flip flop is a storage device with two stable states, designated "1" or Set, and "0" or Clear. It is composed of two inter-connected inverters; the logical symbol (figure A) is a square formed by the combination of the two single inverter symbols. By convention, "1" (or Set) inputs and outputs are shown with the upper part of the symbol and "0" (or Clear) inputs and outputs are shown with the lower part of the symbol. This diagrammatic convention simplifies the actual interconnection of the two inverters as shown in figure B.

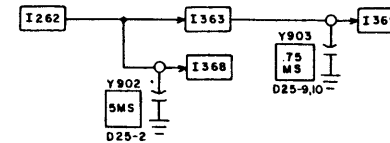


CONTROL DELAY - A control delay consists of an H--- part, which receives the input, and a V--- or N--- part, which provides the output. The output is a clocked pulse which is delayed with respect to the input pulse by one phase time of the clock (0.2 microsecond). Conventions which apply to control delays are:

1. Clock pulse inputs to control delays are not shown on the diagrams and must be obtained from the equation file.
2. The logical number designation indicates the clock phase of the output signal. An odd number indicates an odd clock phase; an even number indicates an even clock phase.
3. The time scales shown on all sequence diagrams are in 0.2 microsecond (1 clock phase time) intervals.

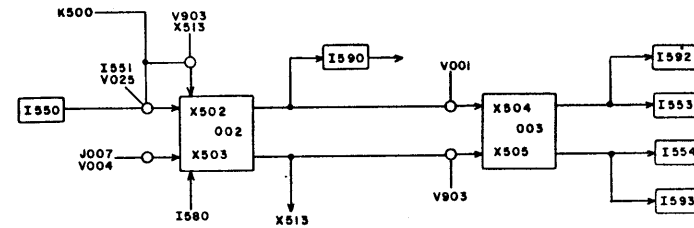


CAPACITIVE DELAY - A capacitive delay is used in an AND configuration to delay the "1" input to a logic element. The capacitor is shown with the curved (negative) plate adjoining the AND symbol. A small box shows the equation file symbol assigned to that delay, the duration of the delay, and the coordinate jack and pin number where physical connection to the capacitor(s) is made.



SYMBOLICAL REPRESENTATION OF TYPICAL EQUATIONS

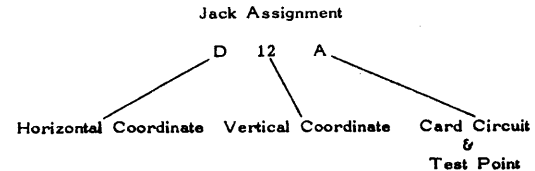
$$\begin{aligned}
 X504 &= V001 X503 & X505 &= V903 X502 \\
 31 \ 003A: 1554: 1593: & & 31 \ 003C: 1592: 1553 & \\
 \\
 X502 &= V903 X513 X500 + 1550 1551 V025 X500 \\
 32 \ 002A: X513: X505: & & & \\
 \\
 X503 &= 1580 + J007 V004 \\
 32 \ 002C: 1590: X504 & & &
 \end{aligned}$$



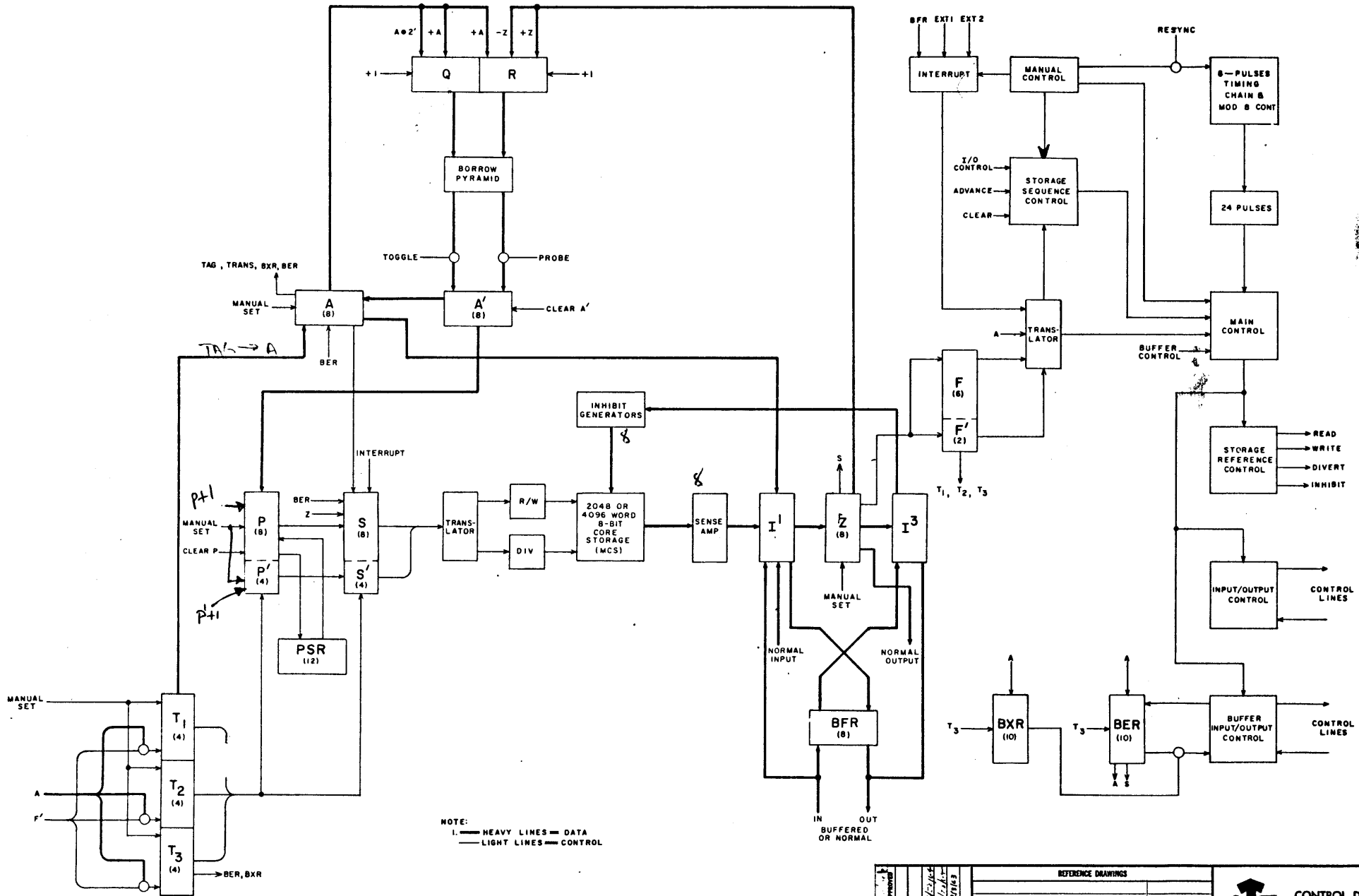
JACK ASSIGNMENTS - The jack assignments of the printed circuit cards associated with each logic symbol appear near the logical designation on the diagram. Jack assignments indicate the physical location of a printed circuit card.

Plug-in cards are designed with from one to four circuits, denoted by the letters A, B, C, or D. The omission of the circuit letter denotes a one circuit card. Two circuit inverter cards are labeled (top circuit, as card is viewed in the chassis connector) and C. Three circuit input (M---) and output (L---) amplifiers are labeled A, B, and C.

Single flip flop cards are not identified by circuit, but it is understood that the even-numbered inverter is associated with circuit A, the odd-numbered inverter with circuit C.

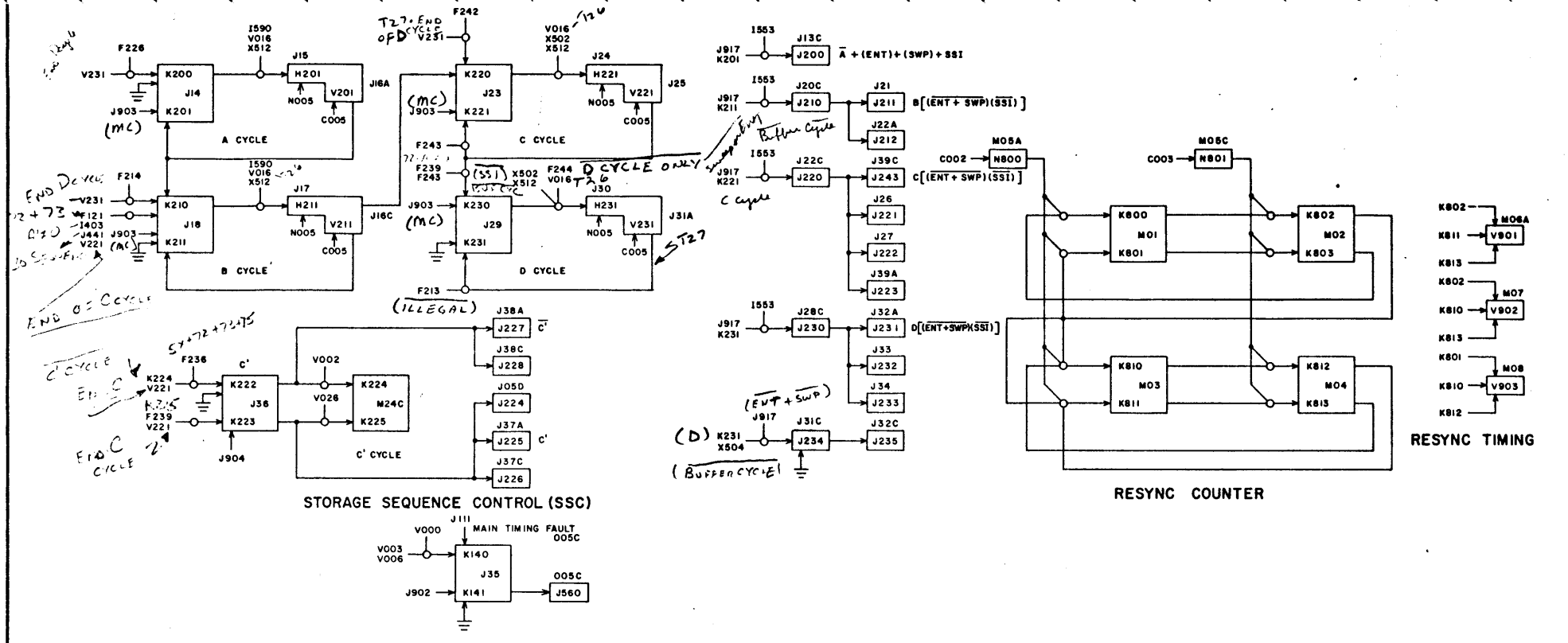


KEY TO SYMBOLS USED ON LOGIC DIAGRAMS



NOTE:
 1. — HEAVY LINES — DATA
 — LIGHT LINES — CONTROL

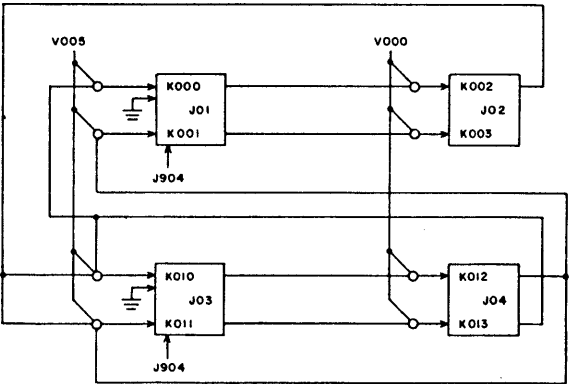
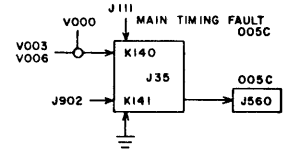
DESIGNED BY DRAWN BY CHECKED BY APPROVED BY DATE REV. DATE REV. DATE REV. DATE	REFERENCE DRAWINGS			CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT DRAWING NUMBER 364038 REV A PAGE 1
	COMPONENTS (UNLESS OTHERWISE INDICATED)			
	RESISTORS	TOLERANCE	VALUE SIZE	
	CAPACITORS			
TITLE BLOCK DIAGRAM, TELE PROGRAMMER— MODEL 8092				



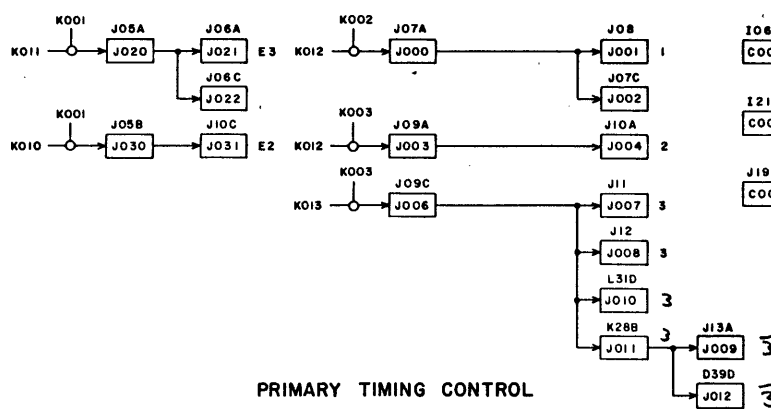
END OF CYCLE
 END OF CYCLE
 END OF CYCLE
 START OF CYCLE
 D CYCLE ONLY
 (ILLEGAL)

STORAGE SEQUENCE CONTROL (SSC)

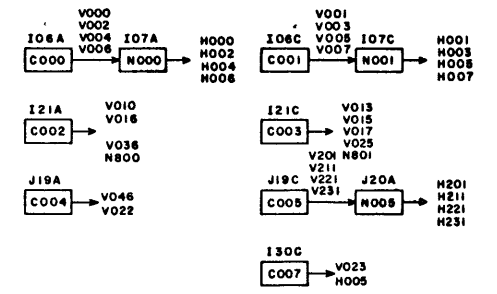
RESYNC COUNTER



TIMING CHAIN EXCURSION COUNTER (EK)

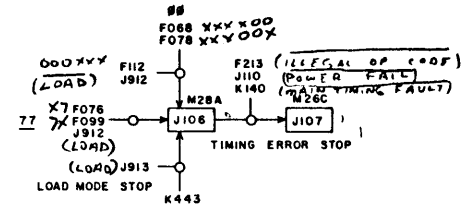
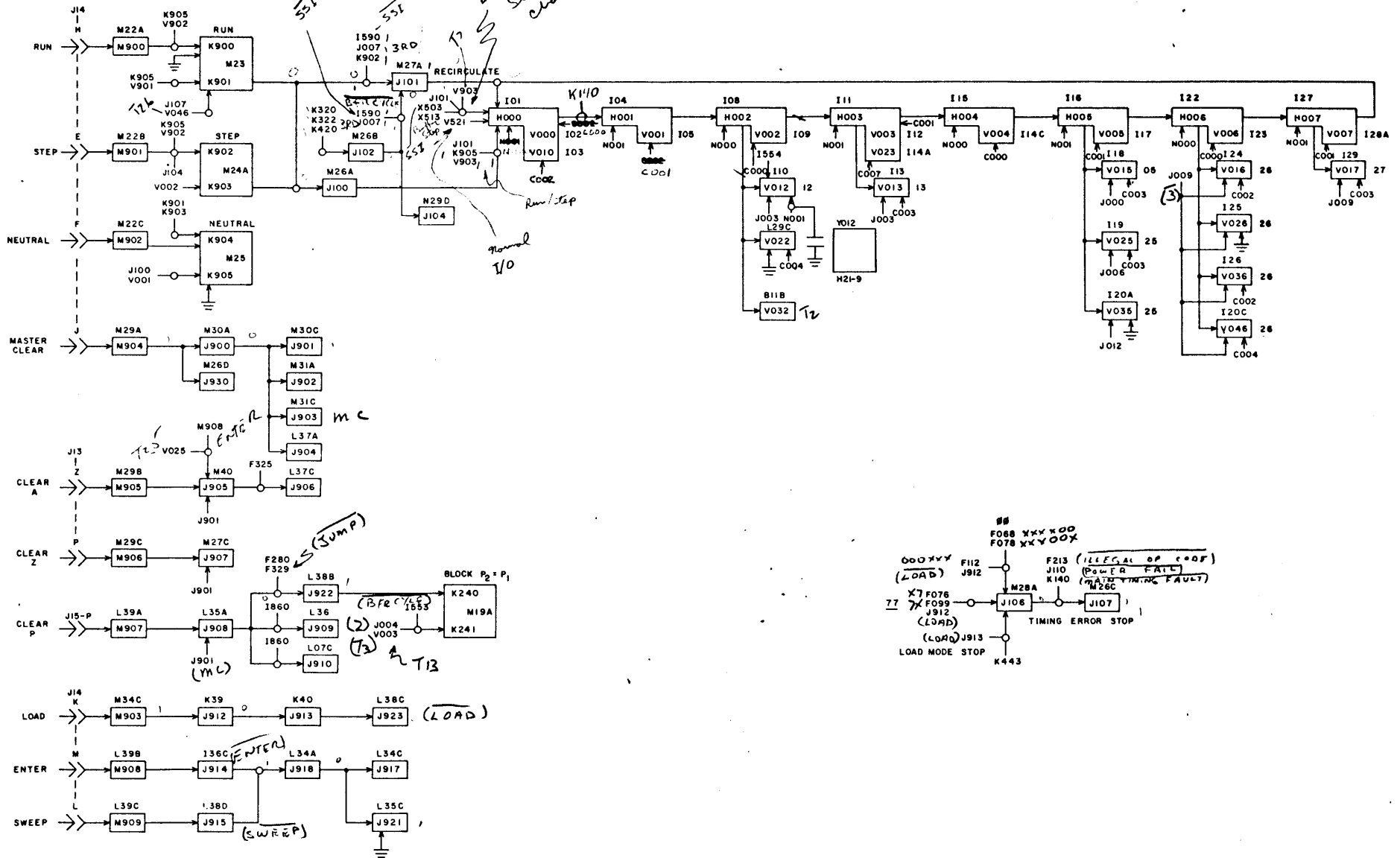


PRIMARY TIMING CONTROL

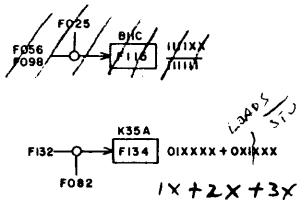
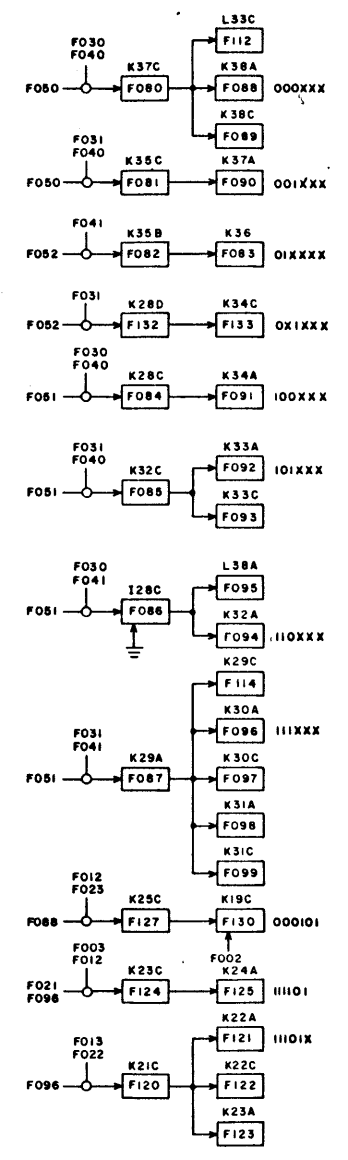
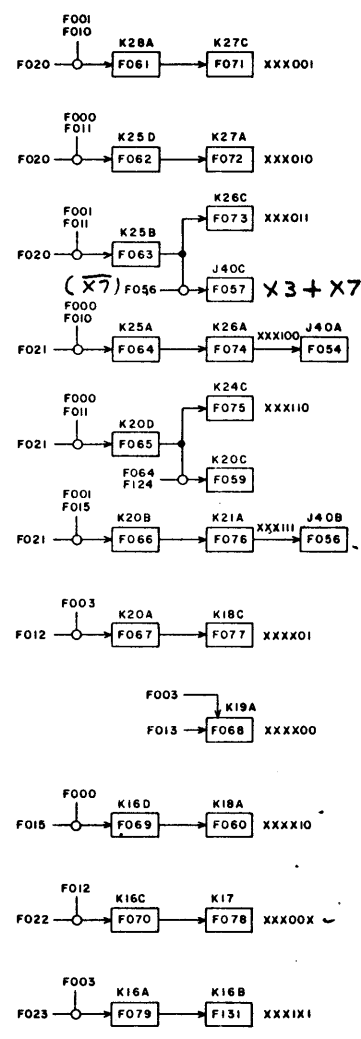
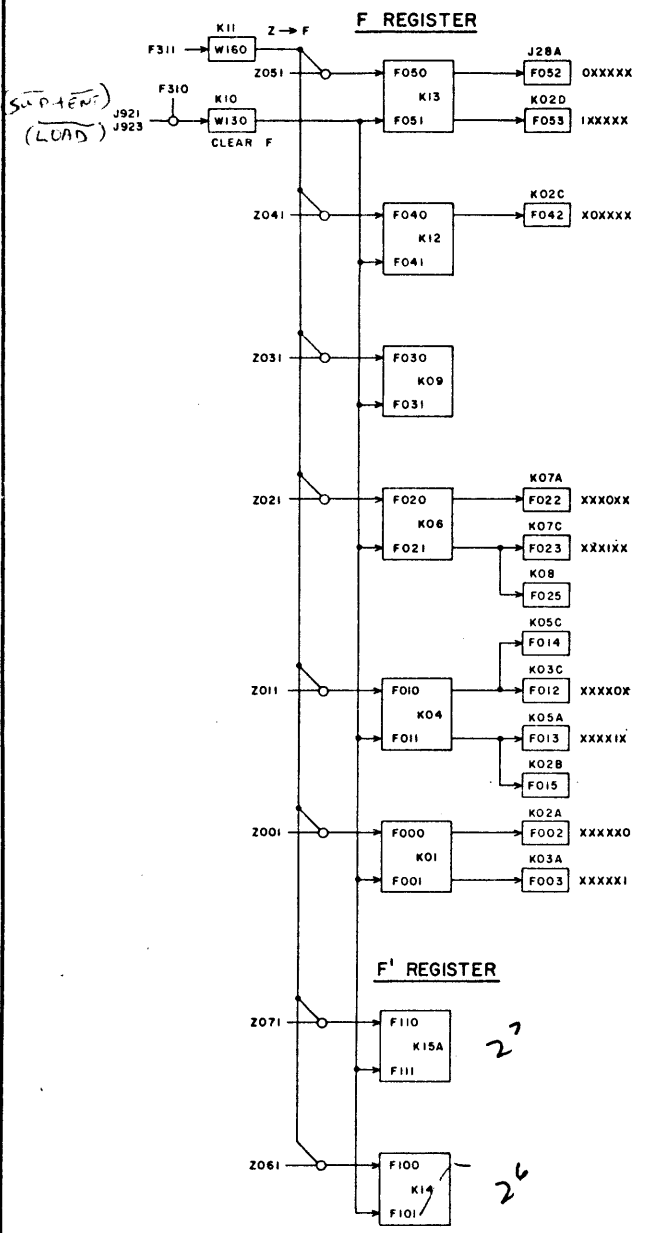


CLOCK

REFERENCE DRAWINGS			
COMPONENTS (UNLESS OTHERWISE INDICATED)			
RESISTORS	TOLERANCE	VALUE	SIZE
CAPACITORS			
TITLE	LOGIC DIAGRAM, MAIN CONTROL		
DATE	3/2/76	REV	A
APPROVED	J. R. NIPP	DATE	2/24/64
DESIGNED	J. R. BECK	DATE	2/24/64
CHECKED	J. R. BECK	DATE	2/24/64
DESIGNED	J. R. BECK	DATE	2/24/64
CONTROL DATA CORPORATION		I D P DIVISION	
PROJECT OR PRODUCT		8092 TELEPROGRAMMER	
DRAWING NUMBER		360426	
SHEET	2	PAGE	2

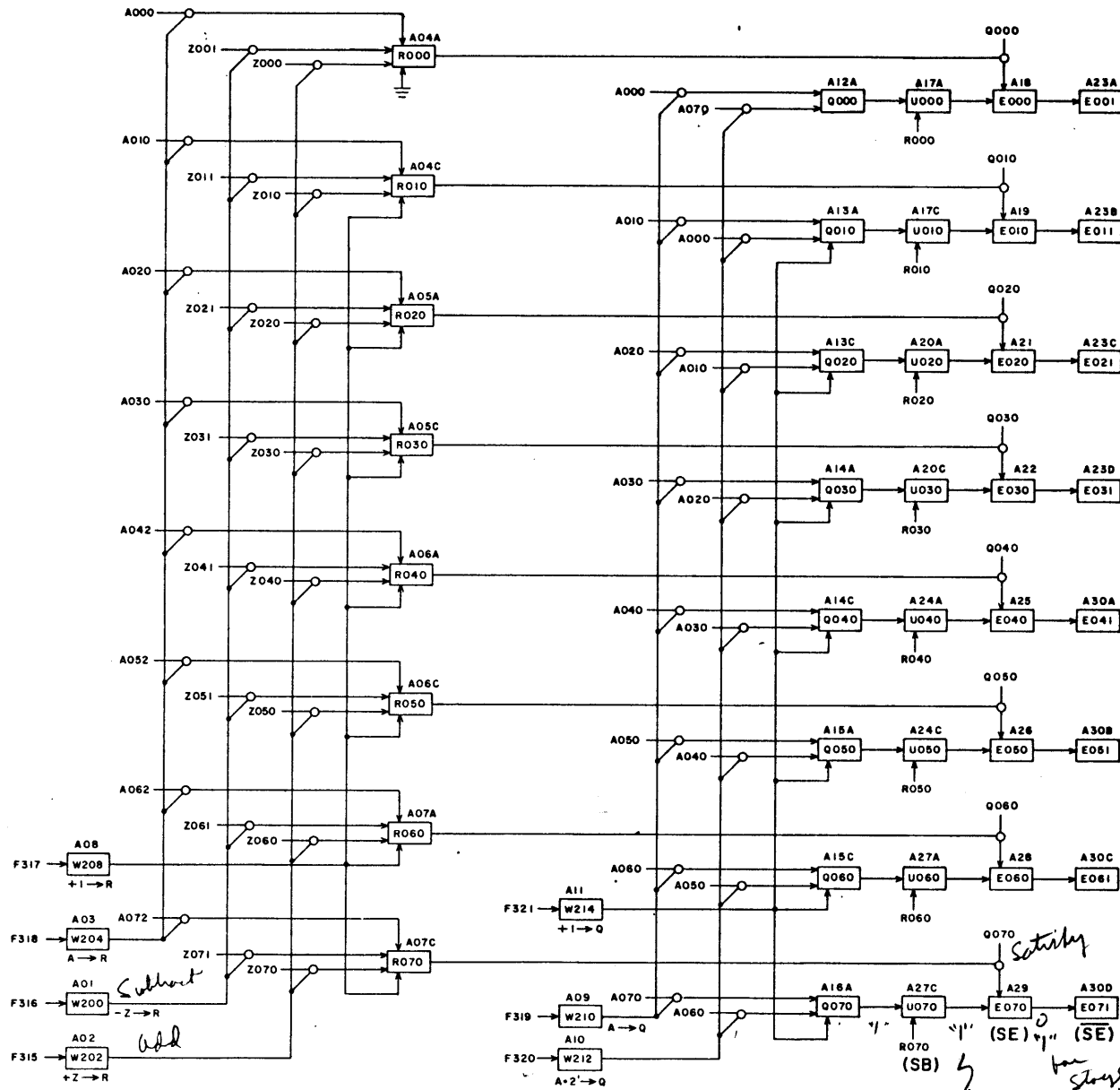


APPROVED: [Signature] DESIGNED: J. H. NIPP DRAWN: N. K. BECK DATE: 2/24/64	REFERENCE DRAWINGS	
	COMPONENTS (UNLESS OTHERWISE INDICATED)	
	RESISTORS	TOLERANCE VALUE SIZE
	CAPACITORS	TOLERANCE VALUE SIZE
TITLE		CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT 8092 TELEPROGRAMMER DRAWING NUMBER 364156 SHEET 3



XXXXXX
XXXXXX

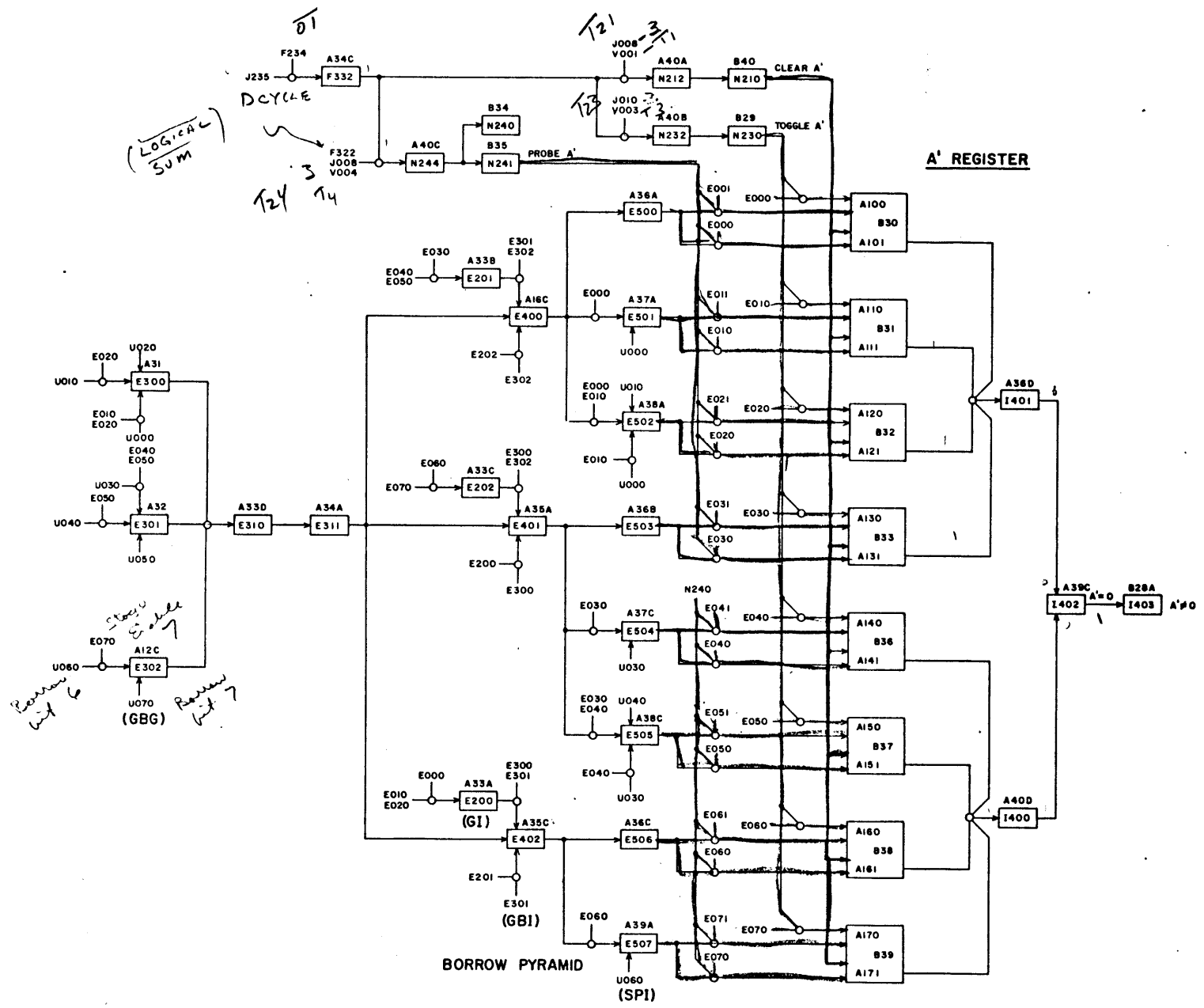
REV. NO.		DATE		BY		CHECKED		DATE		BY		DESIGNED		DATE		BY													
B	1585	3/15/68	KH	2/1/68	W.L.	J.H. NIPP	J.H. NIPP	2/24/68	J.H. NIPP	J.H. NIPP	2/14/64	J.H. NIPP	J.H. NIPP	J.H. NIPP	J.H. NIPP	J.H. NIPP	J.H. NIPP												
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REFERENCE DRAWINGS		COMPONENTS (UNLESS OTHERWISE INDICATED)																											
RESISTORS	TOLERANCE	VALUE	SIZE																										
CAPACITORS																													
TITLE LOGIC DIAGRAM, REGISTERS, F & F' & TRANSLATORS																PROJECT OR PRODUCT 8092 TELEPROGRAMMER													
DRAWING NUMBER 360449																REV 4													



SUBTRACT
 OUTPUTS → R = \bar{E}
 L → Q = A

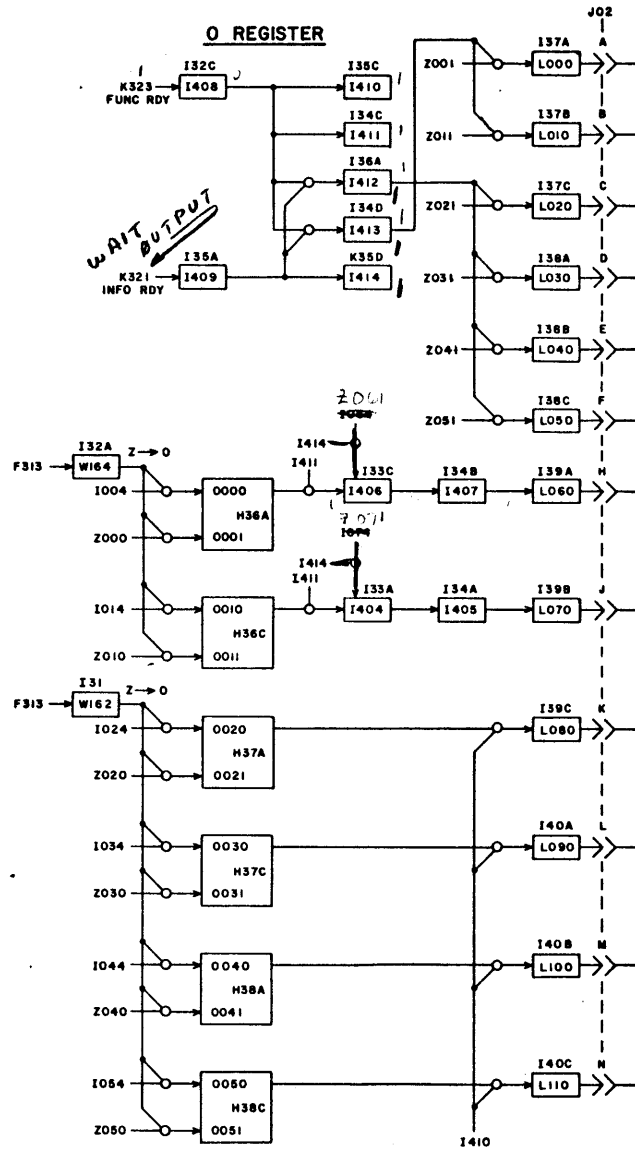
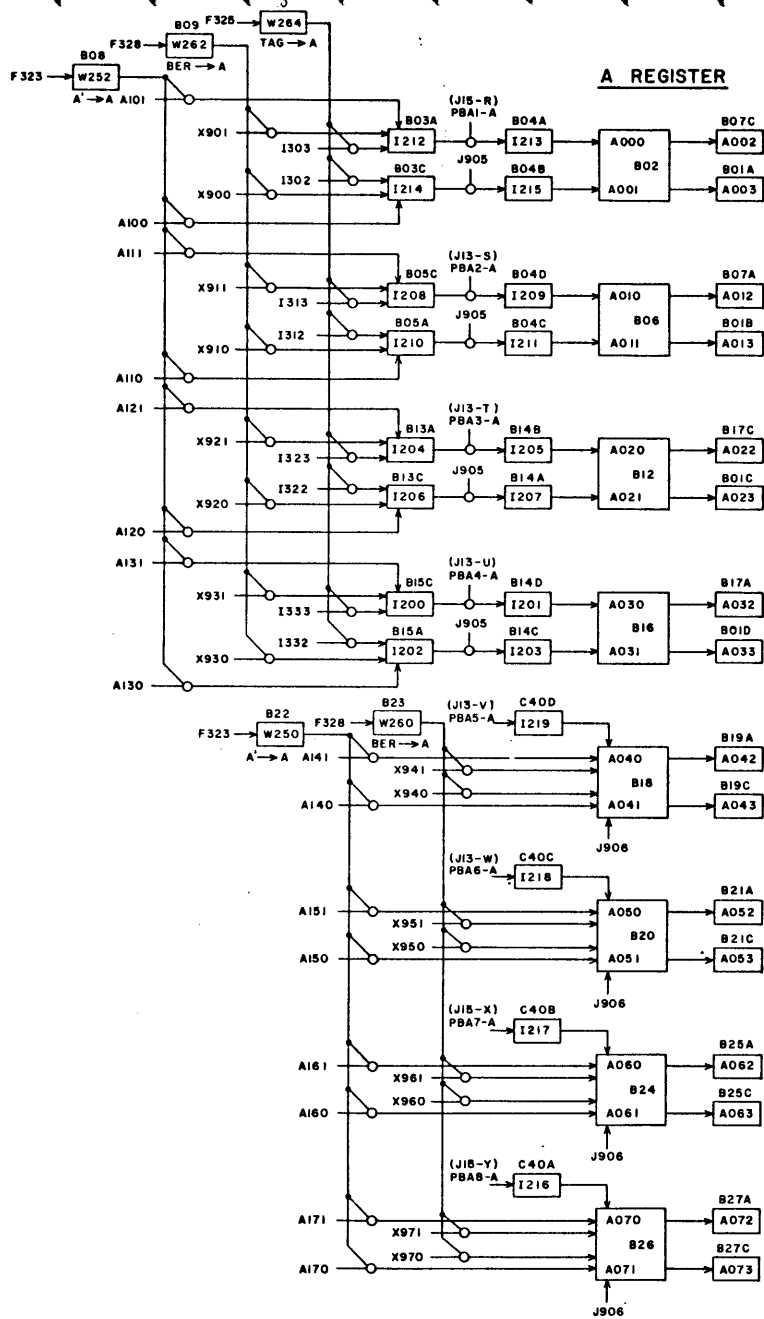
ADD
 R = Z
 Q = A

REV. DATE DESIGNED APPROVED CHECKED DRAWN ENGRAVED	2/24/64 J. H. NIPP J. H. NIPP 2/18/64	REFERENCE DRAWINGS		CONTROL DATA CORPORATION I D P DIVISION PRODUCT OR PRODUCT 8092 TELEPROGRAMMER DRAWING NUMBER 360428 REV
	COMPONENTS (UNLESS OTHERWISE INDICATED)		RESISTORS CAPACITORS	
	TITLE LOGIC DIAGRAM, R AND Q INVERTERS		SHEET PAGE 6	
	REV. DATE DESIGNED APPROVED CHECKED DRAWN ENGRAVED		TOLERANCE VALUE SIZE	



REFERENCE DRAWINGS			
COMPONENTS (DIMENSIONS OTHERWISE INDICATED)			
RESISTORS	TOLERANCE	VALUE	SIZE
CAPACITORS			
TITLE LOGIC DIAGRAM, REGISTER - A'			
PROJECT OR PRODUCT 8092 TELEPROGRAMMER			REV
DRAWING NUMBER 364157			7

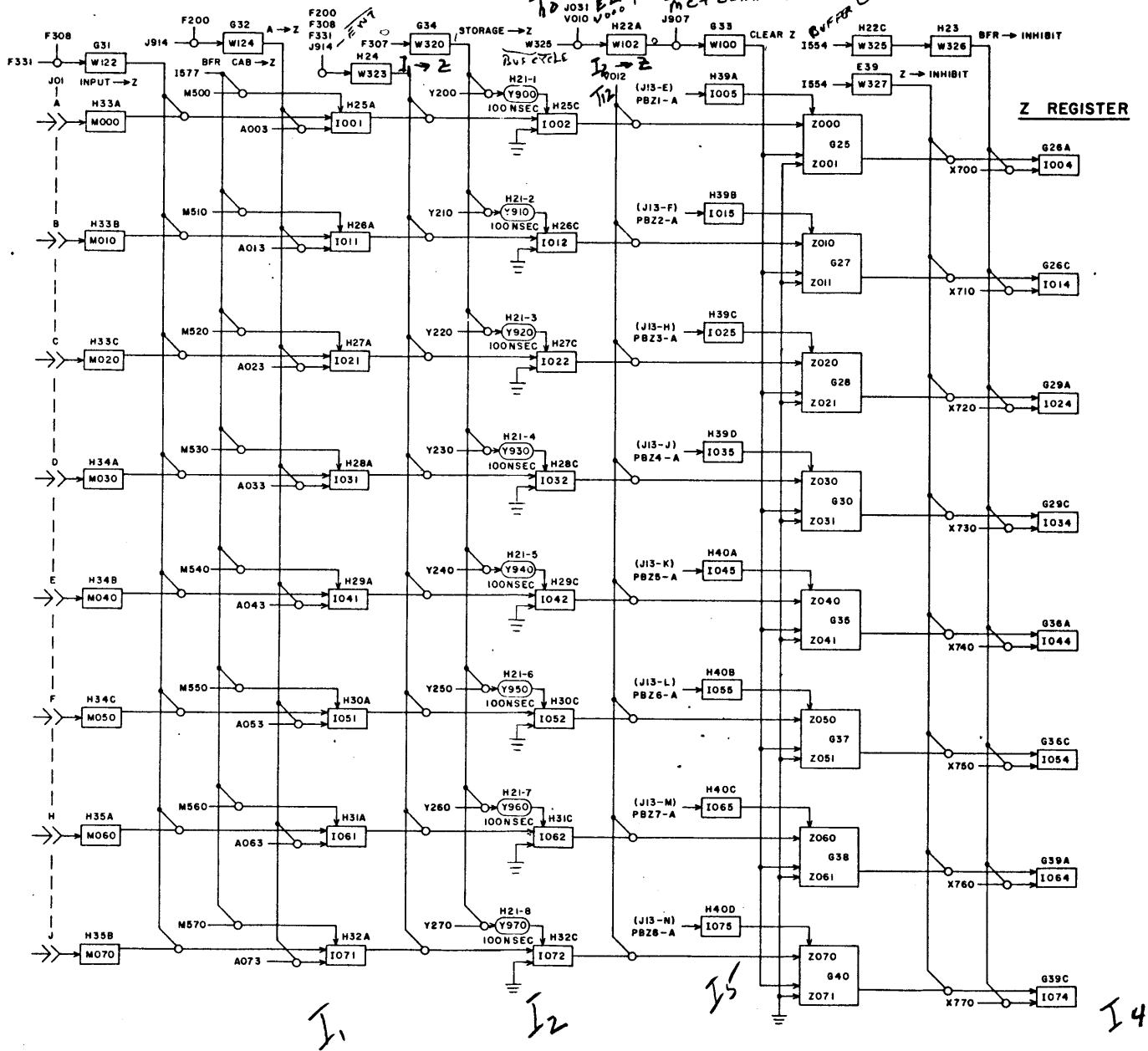
CONTROL DATA CORPORATION
IDP DIVISION
8092 TELEPROGRAMMER
364157
7




B 1585 3/15 A 1354 7/79 REV. DATE APPROVED: W.B. MUE CHECKED: J.H. NIPP DRAWN: N.K. BECK DESIGNED:				REFERENCE DRAWINGS COMPONENTS (UNLESS OTHERWISE INDICATED) RESISTORS CAPACITORS TITLE LOGIC DIAGRAM REGISTERS - A AND O				CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT 8092 TELEPROGRAMMER DRAWING NUMBER 360429 REV B					
REV.	DATE	BY	CHK.	DESC.	APPROVED	TOLERANCE	VALUE	OHM	REV	DATE	BY		
TITLE LOGIC DIAGRAM REGISTERS - A AND O										DRAWING NUMBER 360429		REV B	
DATE 2/26/64										PAGE 8			

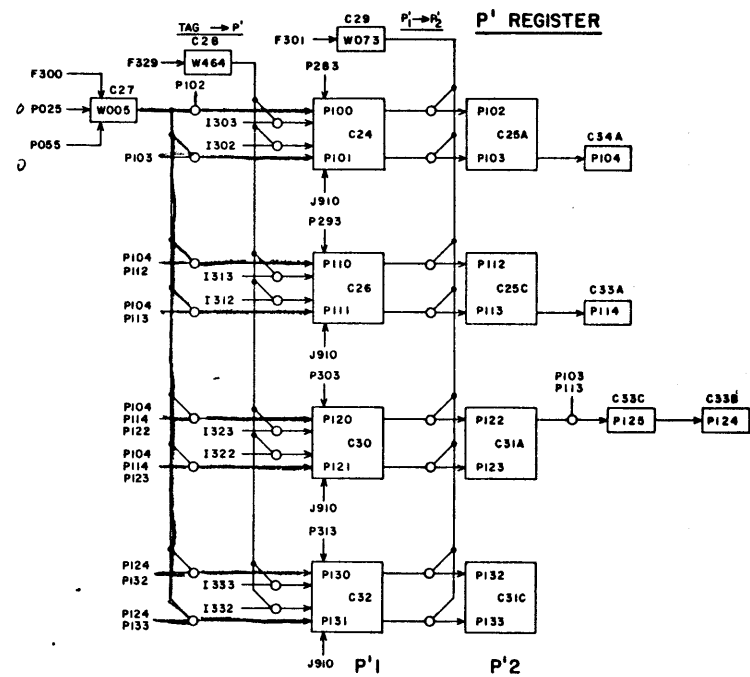
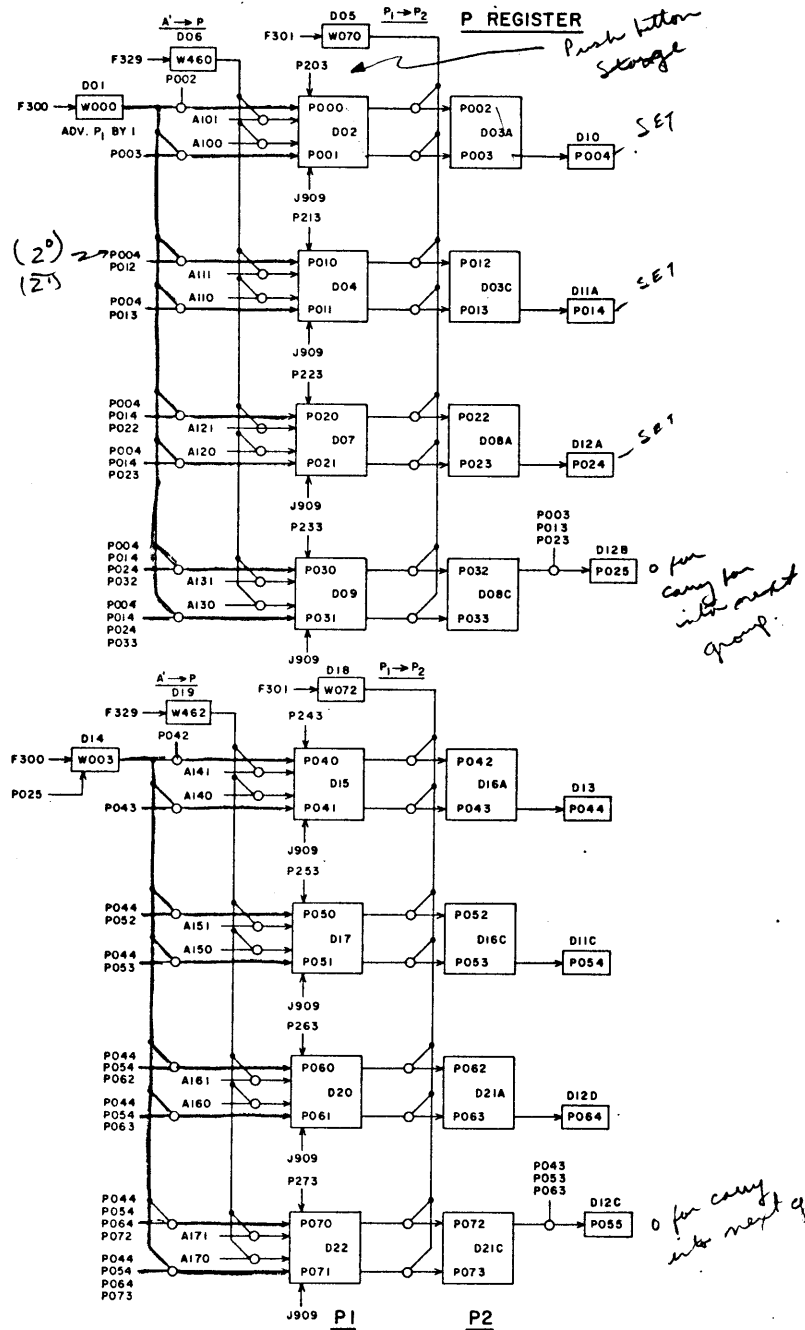
SENSE AMPLIFIERS

- H01
Y200
- H02
Y210
- H03
Y220
- H04
Y230
- H05
Y240
- H06
Y250
- H07
Y260
- H08
Y270



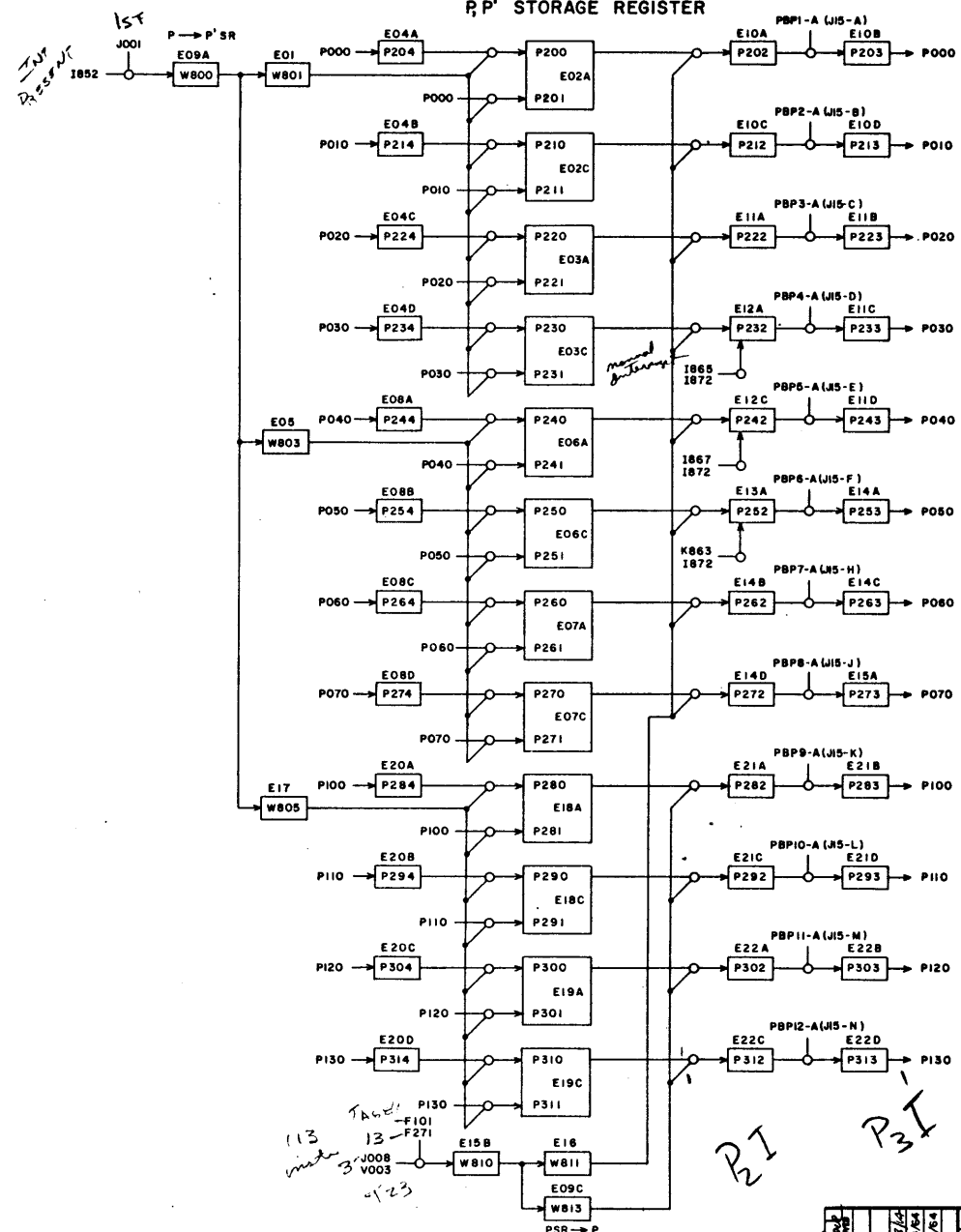
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TITLE LOGIC DIAGRAM REGISTER-Z		DRAWING NUMBER 364158	
REV. 15851 65 A 1402 80 REV. APRIL DATE DES. ENGR. CHK. APPROVED		REV. B SHEET PAGE 9	


CONTROL DATA CORPORATION
I D P DIVISION
 PROJECT OR PRODUCT
8092 TELEPROGRAMMER
 DRAWING NUMBER
364158
 REV. **B**



APPROVED: <i>[Signature]</i> DESIGNED: J. H. NIPP DRAWN: N. K. BECK CHECKED: <i>[Signature]</i> DATE: 2/4/64	REFERENCE DRAWINGS			CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT 8092 TELEPROGRAMMER DRAWING NUMBER 360430 REV A	
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	RESISTORS	TOLERANCE	VALUE		SIZE
	CAPACITORS	TOLERANCE	VALUE		SIZE
TITLE LOGIC DIAGRAM REGISTERS - P AND P'				SHEET 10	

R, P' STORAGE REGISTER

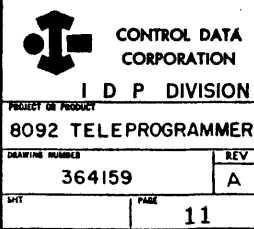


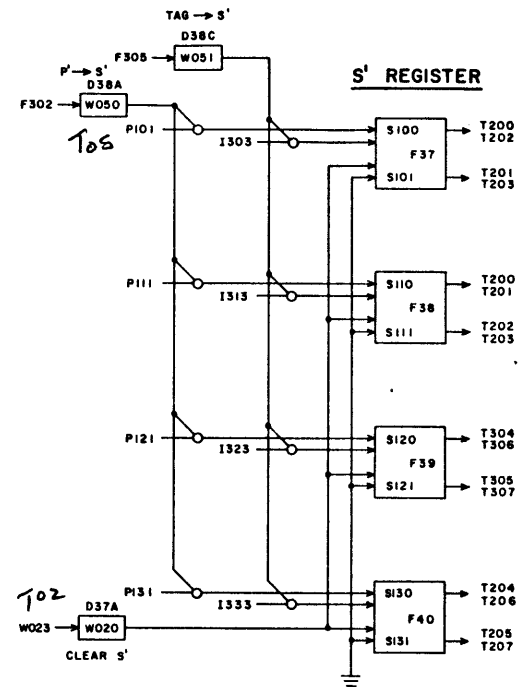
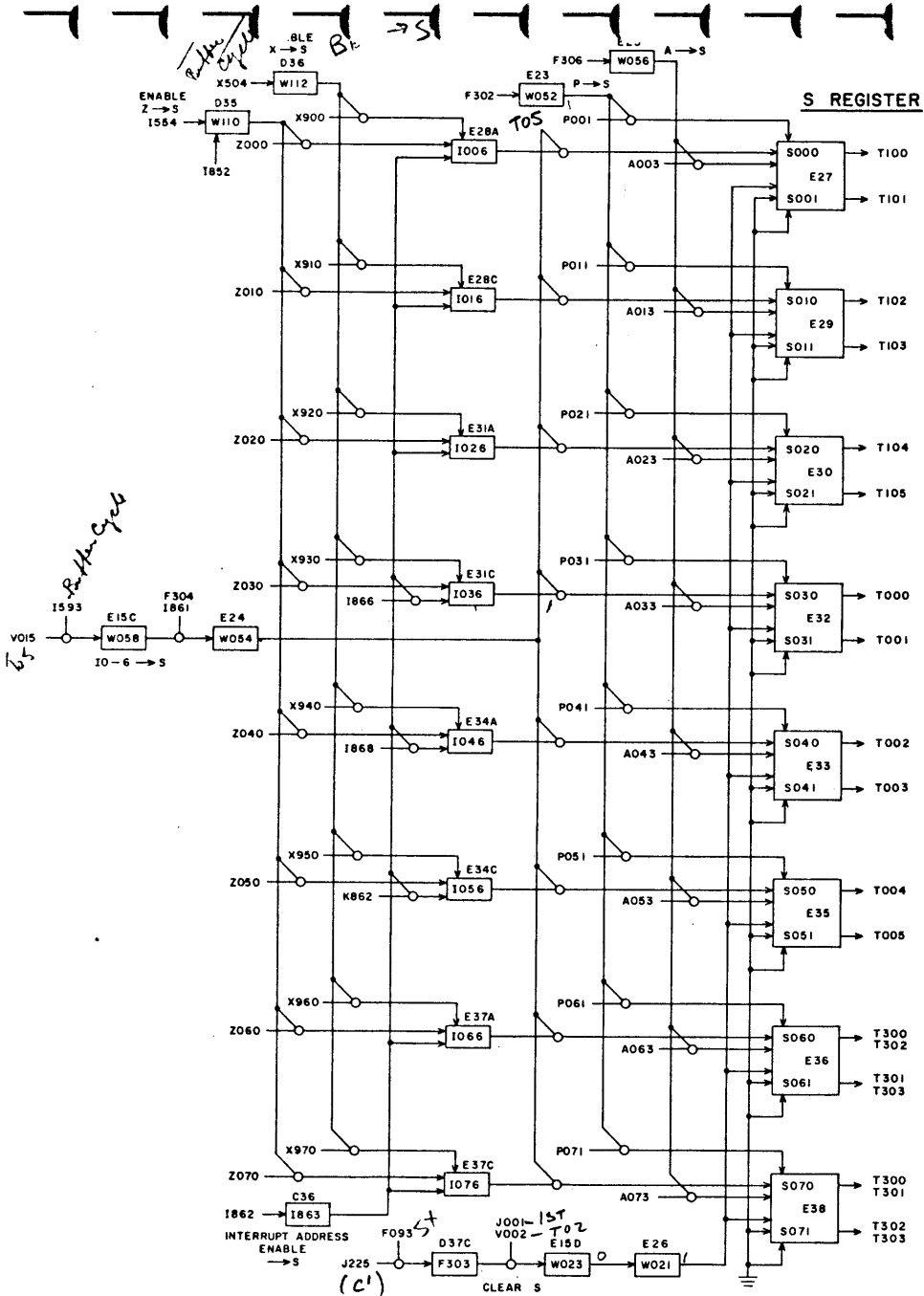
113
13
3
123

P2I

P3I

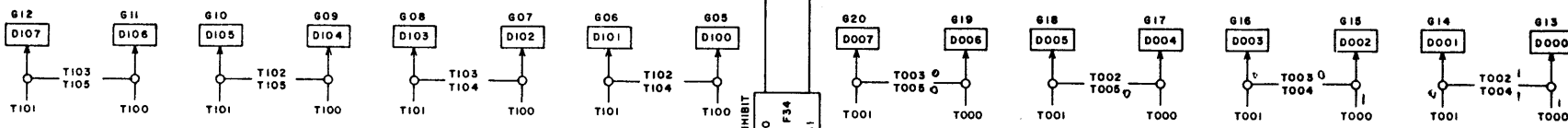
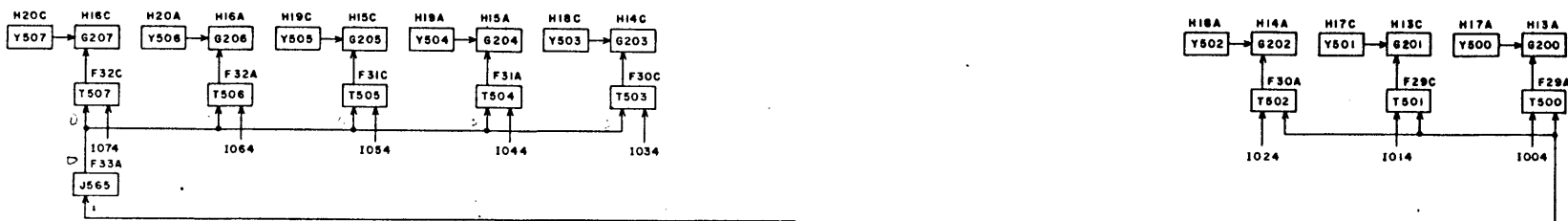
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	CAPACITORS			
TITLE LOGIC DIAGRAM REGISTER - PSR		DRAWING NUMBER 364159		
PROJECT OF PRODUCT 8092 TELEPROGRAMMER		REV A		
SHEET 11		PAGE 11		





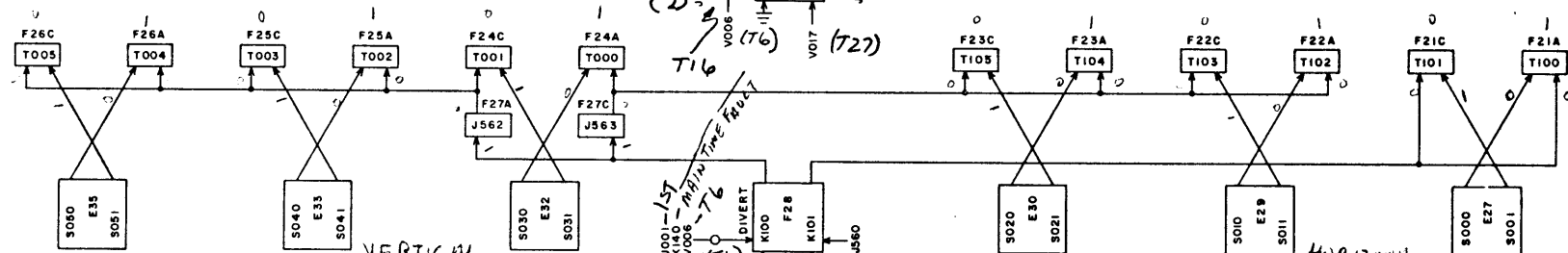
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	TOLERANCE	VALUE SIZE
	RESISTORS	
	CAPACITORS	
TITLE		PROJECT OR PRODUCT
LOGIC DIAGRAM		8092 TELEPROGRAMMER
REGISTERS - S AND S'		DRAWING NUMBER
		364160
		REV. A
		PAGE 12

INHIBIT DRIVERS

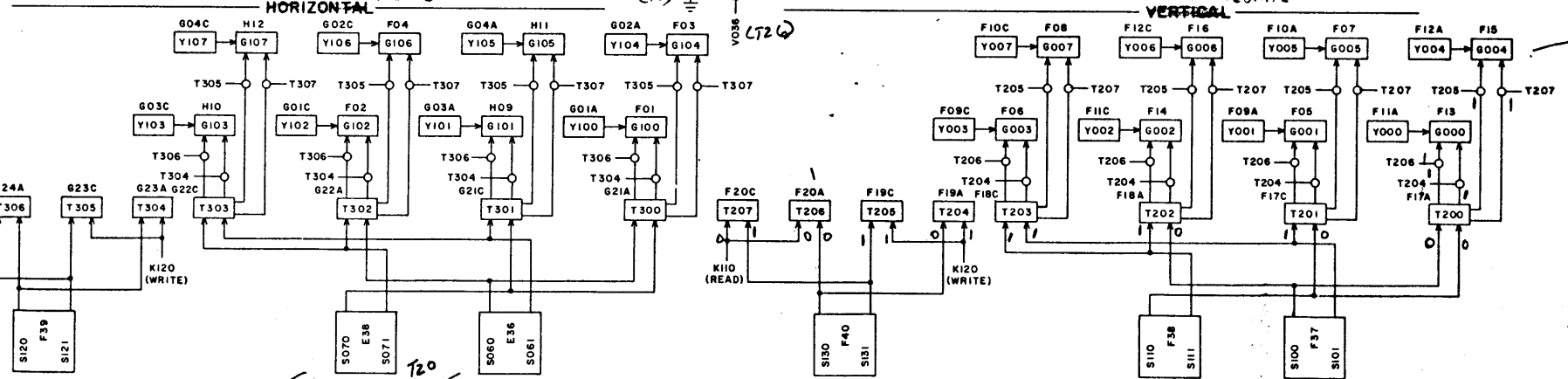


DIVERTE

DIVERT

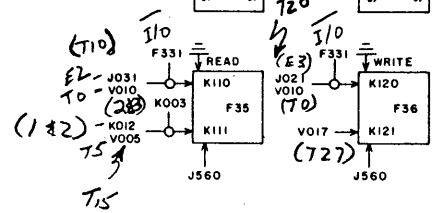


TRANSLATORS



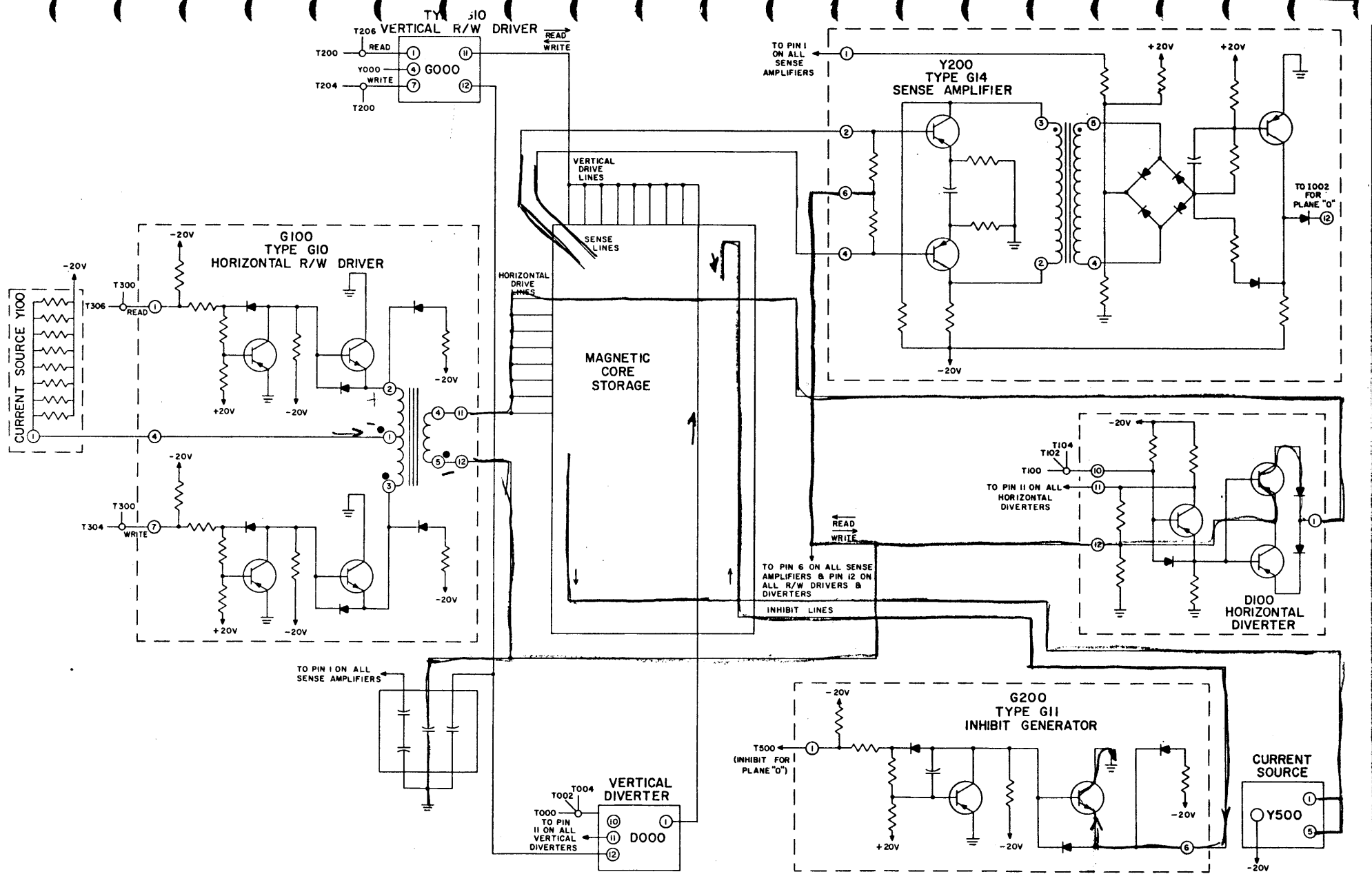
R/W DRIVE

VERTICAL DRIVERS



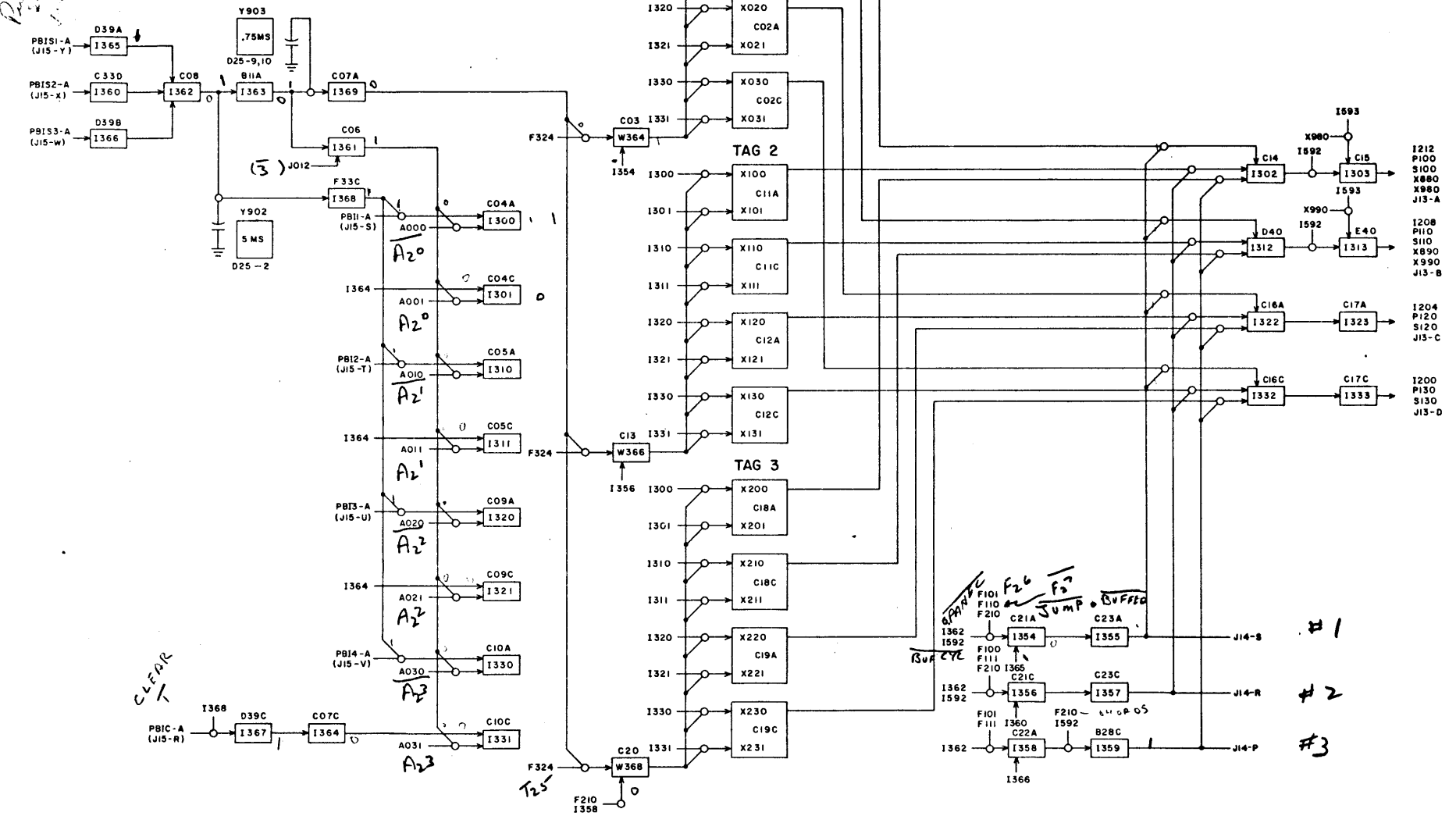
HORIZONTAL DRIVERS

REVISIONS		REFERENCE DRAWINGS		CONTROL DATA CORPORATION I D P DIVISION																								
REV.	DATE	BY	DESCRIPTION																									
A	5/85	J.H. NIPP	2/13/84	PROJECT OR PRODUCT 8092 TELEPROGRAMMER																								
		J.H. NIPP	2/13/84																									
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COMPONENTS (UNLESS OTHERWISE INDICATED)																												
RESISTORS	TOLERANCE	VALUE	SIZE																									
TITLE LOGIC DIAGRAM STORAGE TRANSLATORS				REV A																								
APPROVED: J.H. NIPP CHECKED: J.H. NIPP DRAWN: M.K. BECK DESIGNED: M.K. BECK				REV A 13																								



APPROVED: <i>W.P.M.G.</i> CHECKED: <i>J.P.H.N.P.P.</i> DRAWN: <i>N.K.BECK</i> DESIGNED:	REFERENCE DRAWINGS	CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT 8092 TELEPROGRAMMER DRAWING NUMBER 360442 REV A
	COMPONENTS (UNLESS OTHERWISE INDICATED)	
	RESISTORS: TOLERANCE: NONE SIZE:	
	CAPACITORS:	
TITLE SCHEMATIC DIAGRAM, TYPICAL STORAGE CIRCUITS	SHEET: PAGE: 14	

Parts
list
found



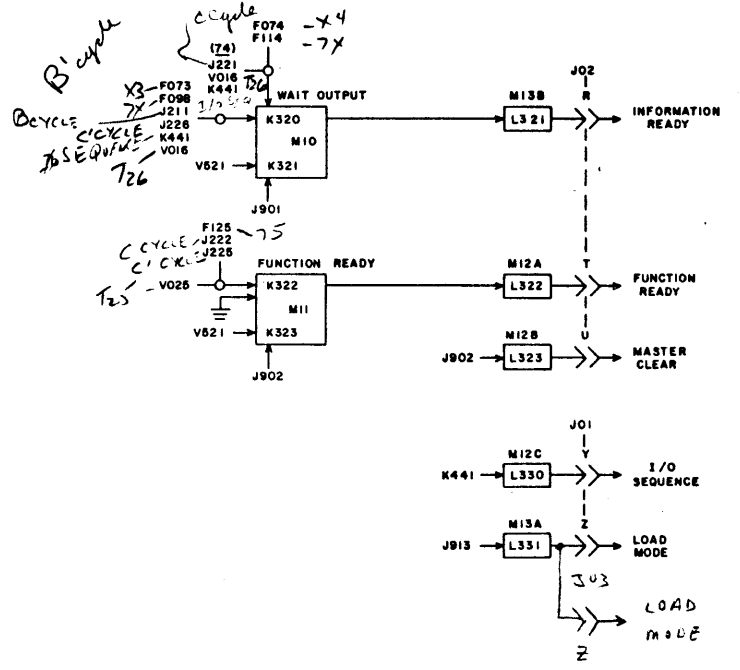
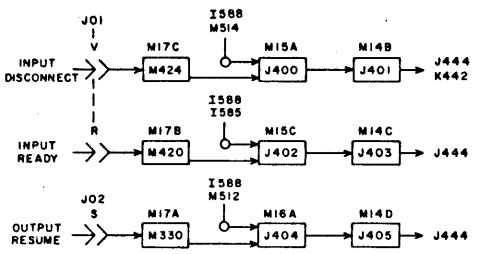
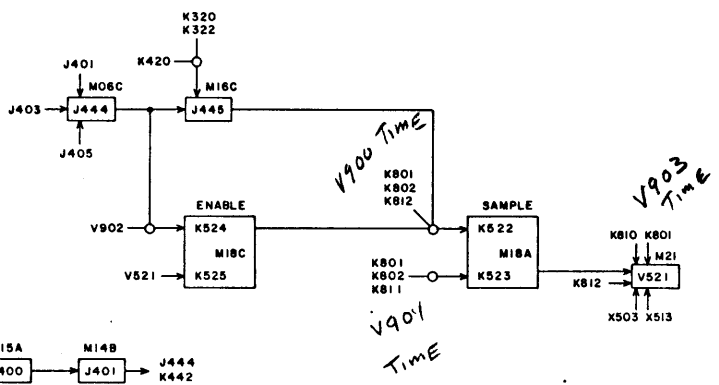
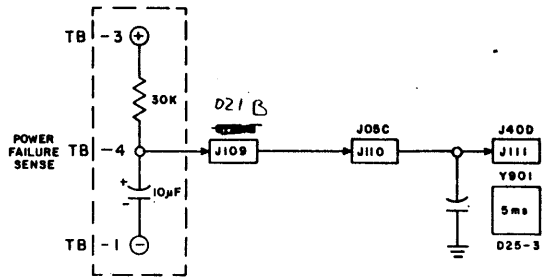
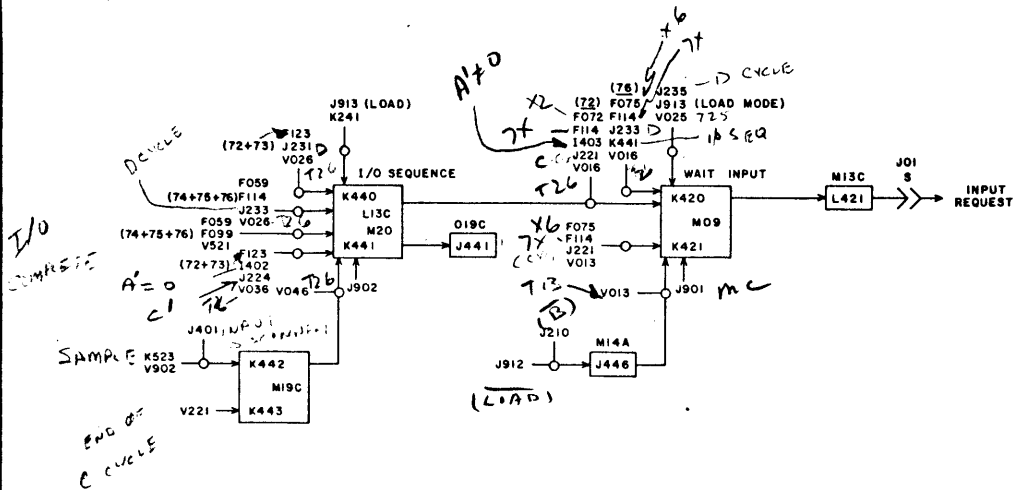
TAG REGISTERS

CLEAR

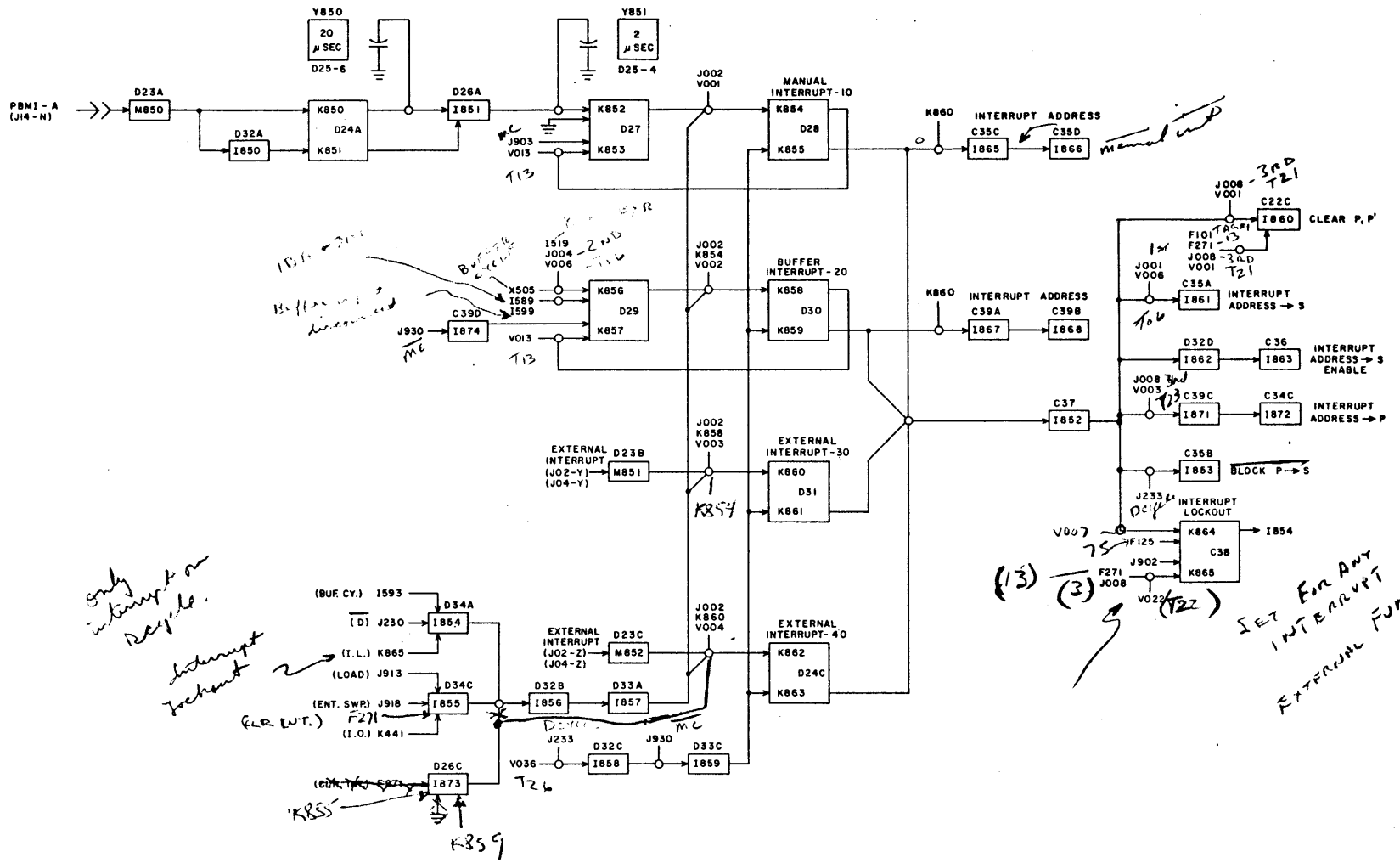
APPROX
F26
F3
JUMP
Bu Ff10
BURN EYE

#1
#2
#3

<p>APPROVED: [Signature] CHECKED: J.H. NIPP DRAWN: N.K. BECK DESIGNED: [Signature]</p>	REFERENCE DRAWINGS				<p>CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT 8092 TELEPROGRAMMER DRAWING NUMBER 360433 REV A</p>
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	CAPACITORS				
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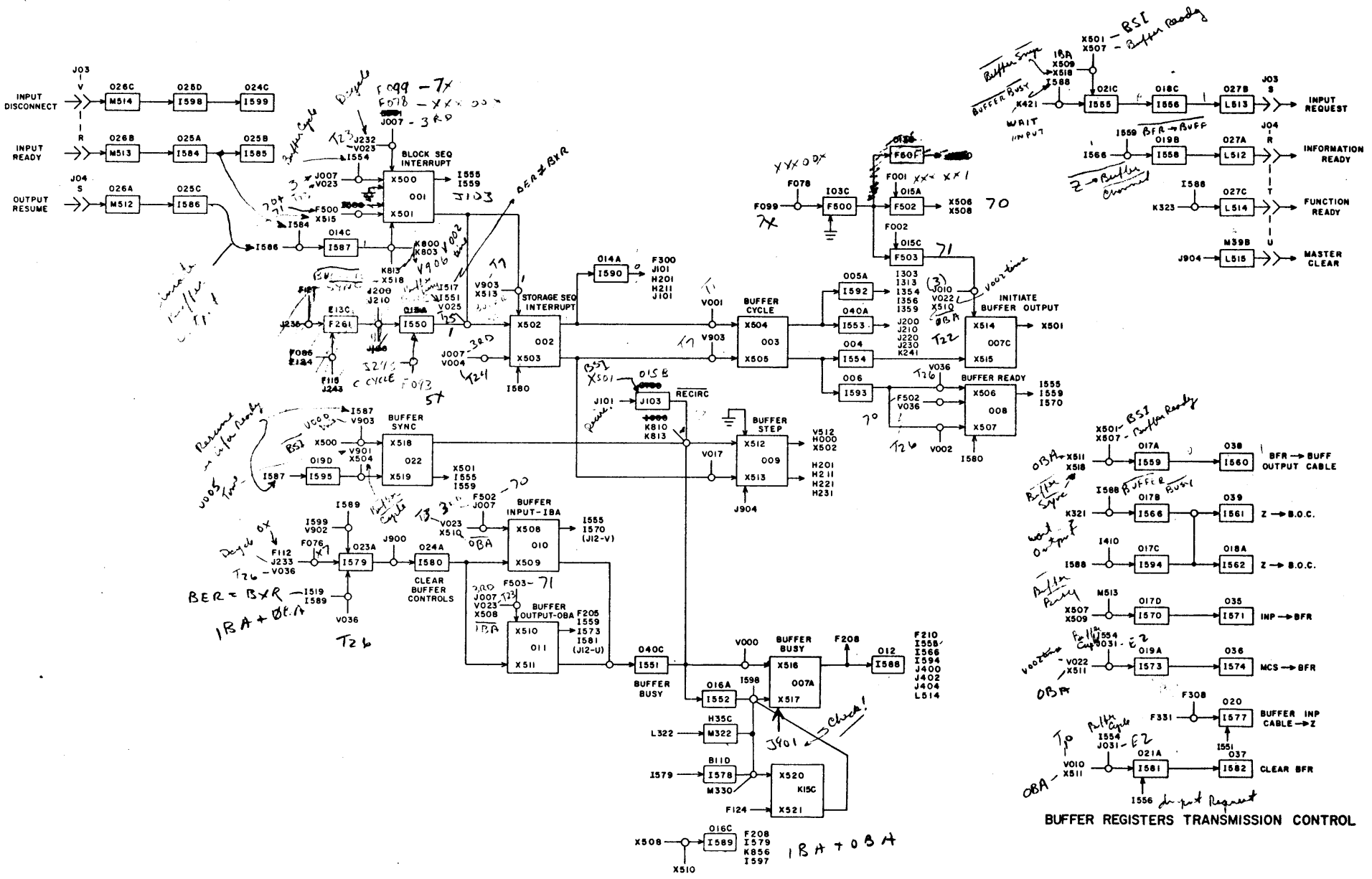
APPROVED: <i>[Signature]</i> CHECKED: J. H. NIPP DRAWN: J. K. BECK DATE: 2/21/64			REFERENCE DRAWINGS		
TITLE: LOGIC DIAGRAM, INPUT/OUTPUT CONTROL			CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT: 8092 TELEPROGRAMMER DRAWING NUMBER: 360425 REV: <i>[initials]</i>		
COMPONENTS (INCLUDE OTHERS IF INDICATED)			TOLERANCE VALUE SIZE		
RESISTORS			CAPACITORS		
SHEET: 16 OF 16			PAGE: 16		



only interrupt on recycle.
 Interrupt lockout

(3) (3) (122)
 SET FOR ANY EXTERNAL FUNCTION

<table border="1"> <tr><td>REV.</td><td>DATE</td><td>BY</td><td>CHK.</td></tr> <tr><td>A</td><td>1/31/64</td><td>...</td><td>...</td></tr> <tr><td>B</td><td>2/24/64</td><td>...</td><td>...</td></tr> <tr><td>C</td><td>1/31/64</td><td>...</td><td>...</td></tr> </table>				REV.	DATE	BY	CHK.	A	1/31/64	B	2/24/64	C	1/31/64	<table border="1"> <tr><td>APPROVED</td><td>DATE</td></tr> <tr><td>J. H. NIPP</td><td>2/24/64</td></tr> <tr><td>DRAWN</td><td>DATE</td></tr> <tr><td>N. K. BECK</td><td>1/31/64</td></tr> </table>				APPROVED	DATE	J. H. NIPP	2/24/64	DRAWN	DATE	N. K. BECK	1/31/64	<table border="1"> <tr><td colspan="4">REFERENCE DRAWINGS</td></tr> <tr><td colspan="4">COMPONENTS (UNLESS OTHERWISE INDICATED)</td></tr> <tr><td>RESISTORS</td><td>TOLERANCE</td><td>VALUE</td><td>SIZE</td></tr> <tr><td>CAPACITORS</td><td></td><td></td><td></td></tr> </table>				REFERENCE DRAWINGS				COMPONENTS (UNLESS OTHERWISE INDICATED)				RESISTORS	TOLERANCE	VALUE	SIZE	CAPACITORS				<table border="1"> <tr><td colspan="4">CONTROL DATA CORPORATION</td></tr> <tr><td colspan="4">I D P DIVISION</td></tr> <tr><td colspan="4">PROJECT OR PRODUCT</td></tr> <tr><td colspan="4">8092 TELEPROGRAMMER</td></tr> <tr><td colspan="4">DRAWING NUMBER</td></tr> <tr><td colspan="4">360434</td></tr> <tr><td colspan="4">REV</td></tr> <tr><td colspan="4">C</td></tr> </table>				CONTROL DATA CORPORATION				I D P DIVISION				PROJECT OR PRODUCT				8092 TELEPROGRAMMER				DRAWING NUMBER				360434				REV				C			
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REV.	NO.	DATE	BY	CHK.	REVISIONS
F	1585	7-15	JH	WJ	Initial Design
E	505	7-15	JH	WJ	Revise for 1589
D	1470	11-9	JH	WJ	Revise for 1589
C	1451	6-4	JH	WJ	Revise for 1589
B	1411	8-4	JH	WJ	Revise for 1589
A	1334	7-28	JH	WJ	Initial Design

REFERENCE DRAWINGS		
COMPONENTS (UNLESS OTHERWISE INDICATED)		
TOLERANCE	VALUE	SIZE
RESISTORS		
CAPACITORS		
TITLE		
LOGIC DIAGRAM		
BUFFER CONTROLS		

CONTROL DATA CORPORATION

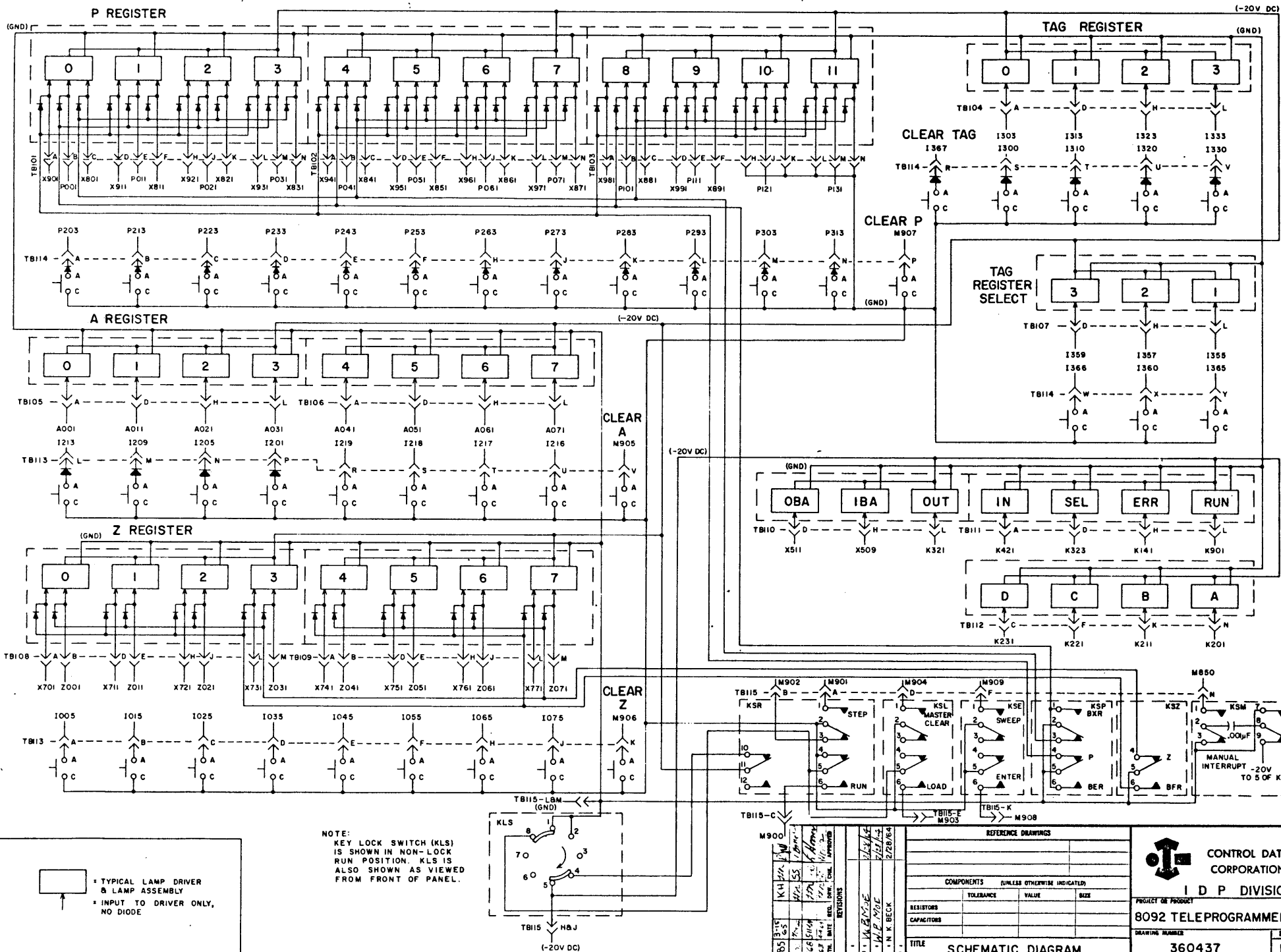
IDP DIVISION

PROJECT OR PRODUCT
8092 TELEPROGRAMMER

DRAWING NUMBER
360447

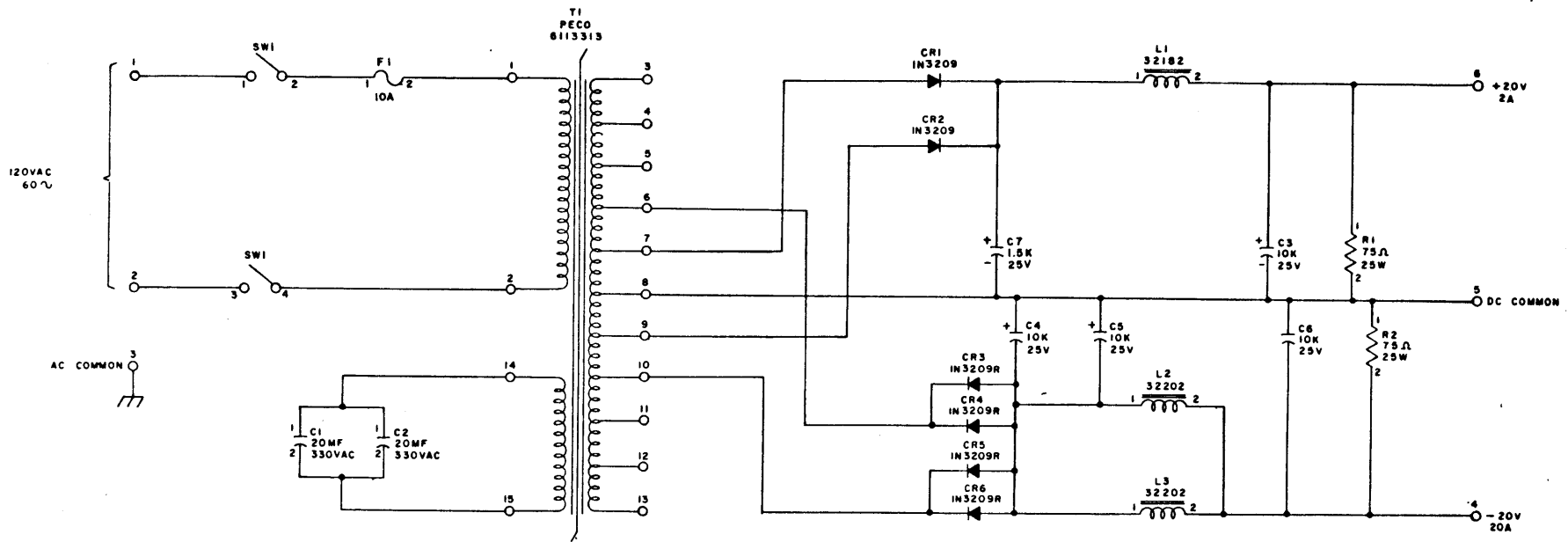
REV. **1**

SHEET **18**




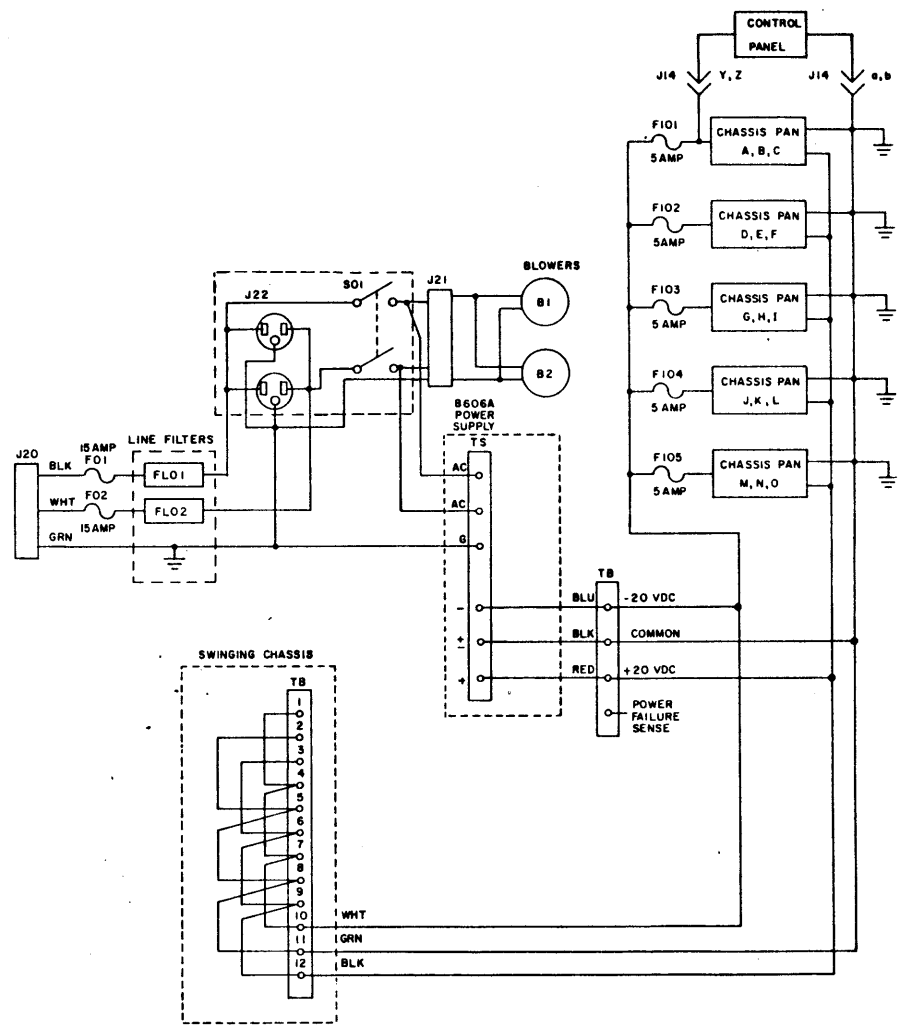
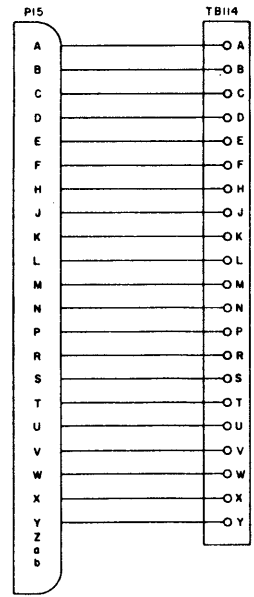
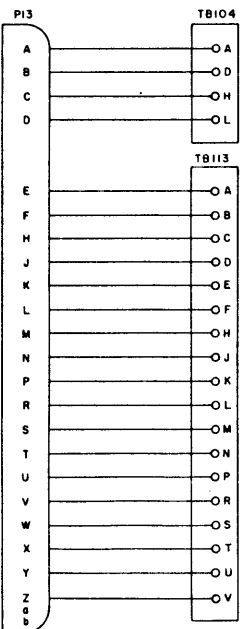
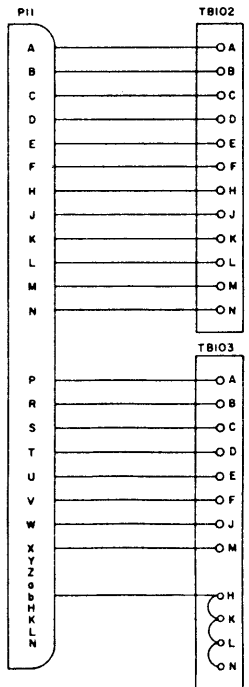
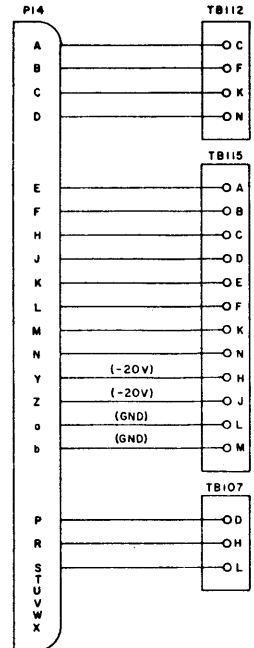
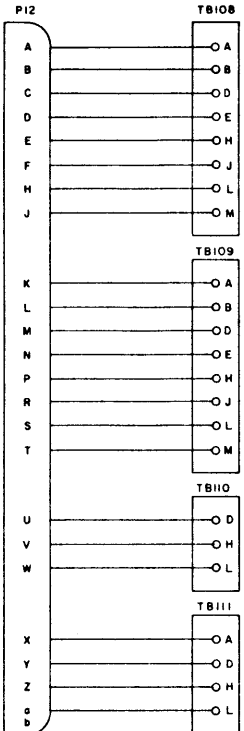
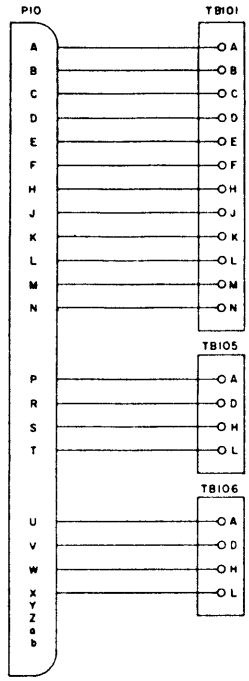
NOTE:
KEY LOCK SWITCH (KLS)
IS SHOWN IN NON-LOCK
RUN POSITION. KLS IS
ALSO SHOWN AS VIEWED
FROM FRONT OF PANEL.

□ = TYPICAL LAMP DRIVER
& LAMP ASSEMBLY
▲ = INPUT TO DRIVER ONLY,
NO DIODE



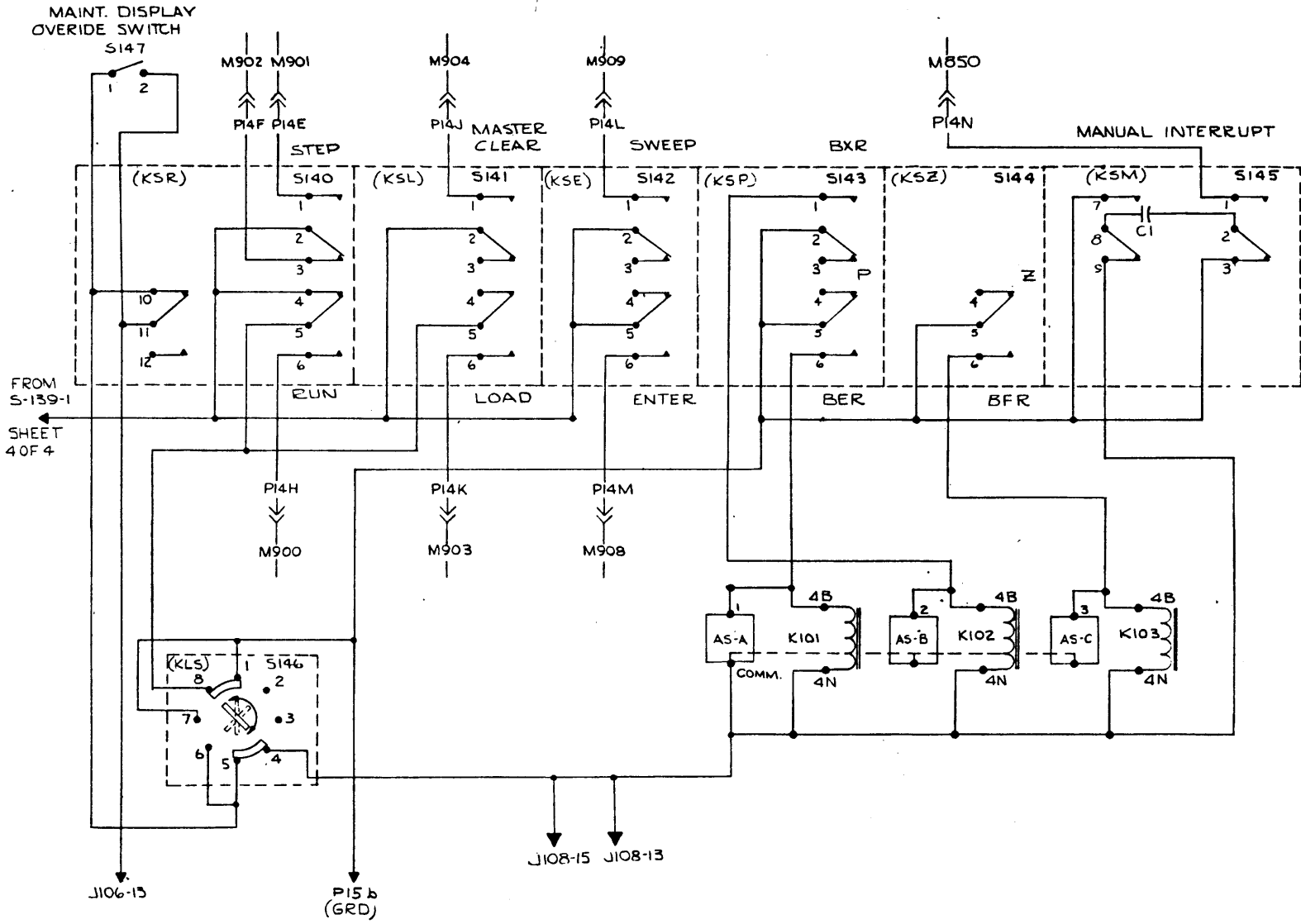
REV. DATE DES. BY: CHS. APPROVED BY: [Signature]	REFERENCE DRAWINGS		
	COMPONENTS (UNLESS OTHERWISE INDICATED)		
	TOLERANCE	VALUE	SIZE
RESISTORS			
CAPACITORS			
TITLE			DRAWING NUMBER
SCHEMATIC, POWER SUPPLY- MODEL 8606-A			364071
			REV
			21


CONTROL DATA CORPORATION
IDP DIVISION
 PRODUCT OR PROJECT



APPROVED: <i>[Signature]</i> REV. DATE: 3/4/68 DESIGNED:	REFERENCE DRAWINGS		CONTROL DATA CORPORATION I D P DIVISION PROJECT OR PRODUCT 8092 TELEPROGRAMMER DRAWING NUMBER 360441 REV A
	COMPONENTS (UNLESS OTHERWISE INDICATED) RESISTORS CAPACITORS		
TITLE CABLING & AC-DC DIST	SHEET 22	DATE: 3/4/68 CHECKED: H. J. BECK DRAWN: H. J. BECK	REV A

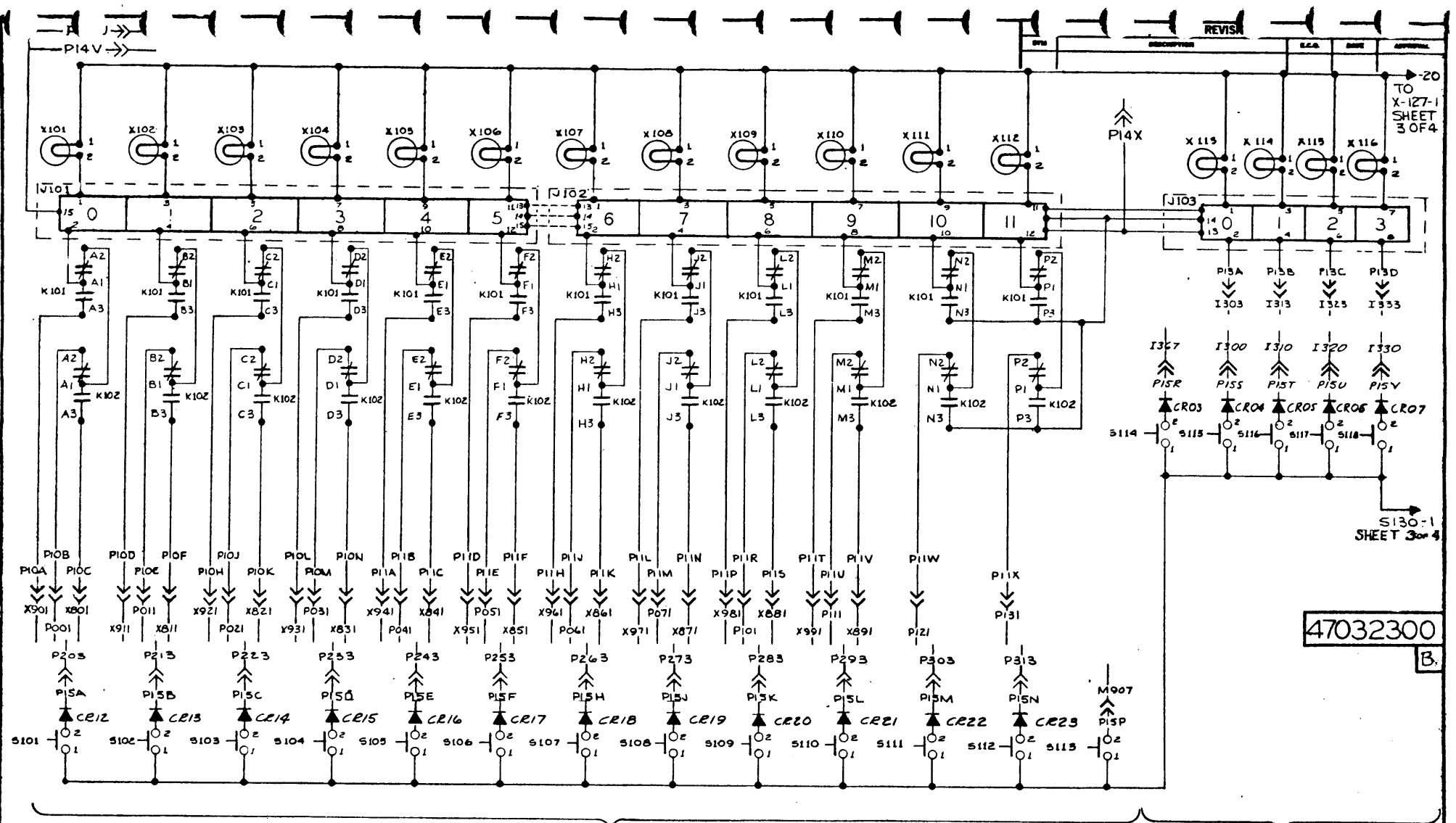
REVISIONS						
REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	APP.
A	-	-	RELEASED	-	11-13-64	WAM
B	2232	-	REVISED PER ECO	RAH	11-15-64	FES



FROM S-139-1
SHEET 4 OF 4

2. DOTTED LINES SHOW CONNECTIONS WITHIN A CONNECTOR OR COMPONENT.
1. KEY LOCK SWITCH KLS IS SHOWN IN NON-LOCK RUN POSITION. KLS IS ALSO SHOWN AS VIEWED FROM FRONT OF PANEL.
NOTES:

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES FRACTIONS: DECIMALS: ANGLES: * * *		CONTROL DATA CORPORATION		TITLE	
DO NOT SCALE DRAWING		CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MINNEAPOLIS, MINNESOTA		SCHEMATIC DIAGRAM 8092 DISPLAY	
MATERIAL	PRODUCT	8092 DISPLAY	SIZE	DRAWING NO.	REV
	DRAWN	<i>P. Blum</i> 11-13-64	C	47032300	B
	CHECKED	<i>J. Blum</i> 11-13-64	SCALE		
	ENGINEER	<i>J. Blum</i> 11-13-64	SHEET 1 OF 4		
	APPROVED				



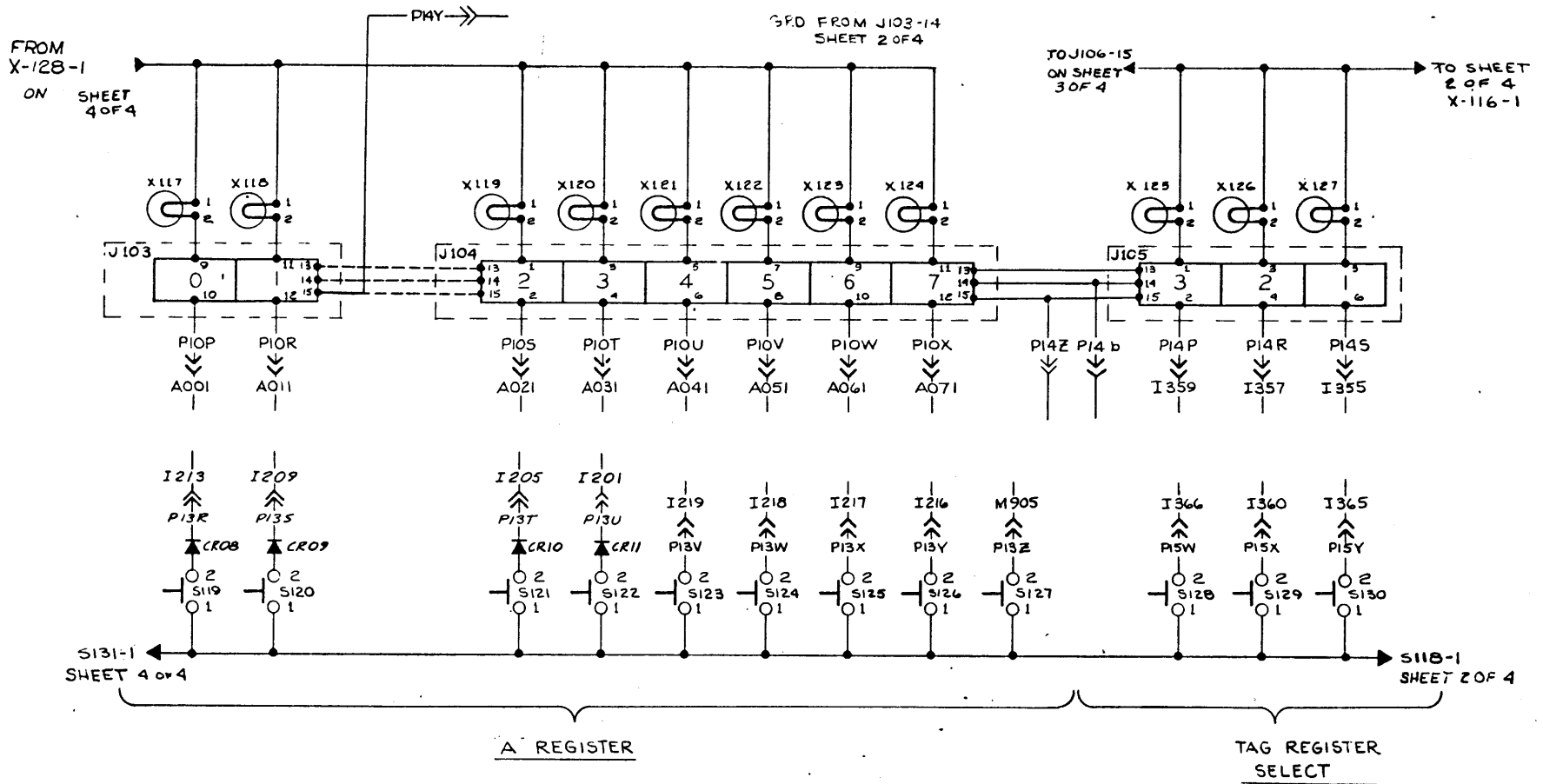
"P" REGISTER

TAG REGISTER

47032300
B.

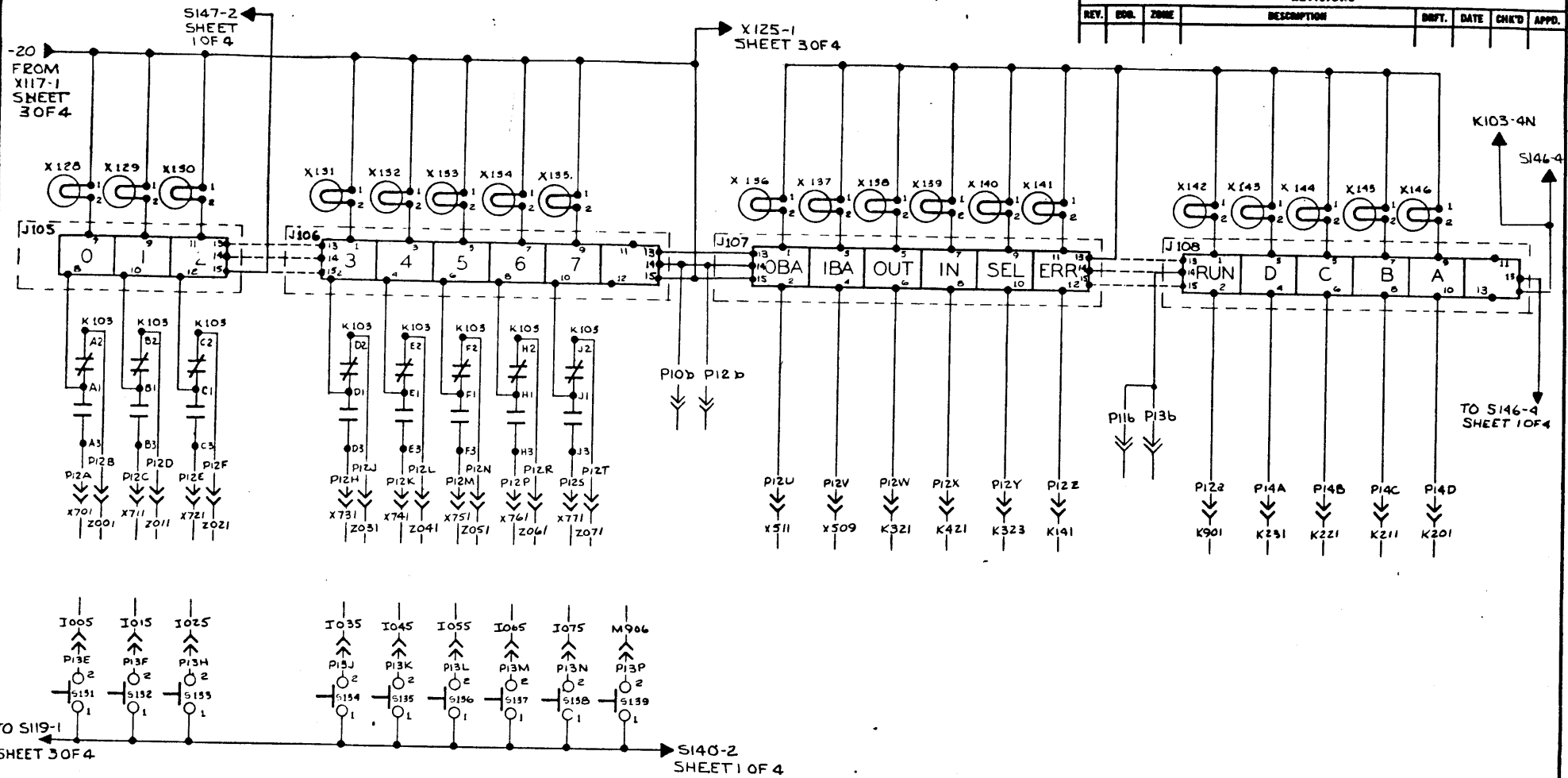
ITEM	REQD.	PART NO.	DESCRIPTION	MATL.	MATL. SPEC.	REVT. AMT.	USED ON	FORM. ASST.	REVT. ASST.
LIST OF MATERIAL									
UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES AND TOLERANCES ARE: FRACTIONS: DECIMALS: 1/64 .001-.001 .01			DRAWN BY		DATE		NAME		
BREAK ALL EDGES AND SPACED CORNERS DIP JETS.			CHECKED				APPLICATION		
DIMENSIONS APPLY AFTER PLATING OR HEAT TREAT.			ENG.				QTY. REQD.		
SURF. FINISH: V ALL INSIDE SURFACES V ALL OUTSIDE SURFACES			PROD.				SCHEMATIC DIAGRAM		
			FINISH				CONTROL DATA CORP.		
							CEDAR ENGINEERING DIVISION		
							8000 WEST 80th ST.		
							MINNEAPOLIS 16, MINNESOTA		
							47032300		
							2 OF 4		

REVISONS							
REV.	ECO.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D	APP.



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES: * ± *		CONTROL DATA		TITLE	
DO NOT SCALE DRAWING		CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MINNEAPOLIS, MINNESOTA		8092 DISPLAY	
MATERIAL	PRODUCT	8092 DISPLAY	SIZE	DRAWING NO.	REV
FINISH	DRAWN		C	47032300	B
	CHECKED		SCALE		
	ENGINEER				
	APPROVED				
				SHEET	3 OF 4

REV.	ISS.	ZONE	DESCRIPTION	DRFT.	DATE	CHK'D	APPD.



'Z' REGISTER

LEGENDS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS: DECIMALS: ANGLES:			TITLE SCHEMATIC DIAGRAM 8092 DISPLAY	
DO NOT SCALE DRAWING			CEDAR ENGINEERING DIVISION DIGITAL ENGINEERING DEPARTMENT MINNEAPOLIS, MINNESOTA	
MATERIAL	PRODUCT	8092 DISPLAY	SIZE	DRAWING NO.
FRESH	DRAWN		C	47032300
	CHECKED			REV
	ENGINEER			B
	APPROVED			SHEET 4 OF 4