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CONTROL DATA CORPORATION

CDC® MICROCIRCUITS

GENERAL THEORY
LOGIC SYMBOLOGY
DATA SHEETS

NORMANDALE CIRCUITS MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A	Manual released. This manual replaces and updates the information previously
(1-10-77)	contained in the Logic Symbology subsection and the Integrated Circuit Package
	Configurations section of Hardware Reference manuals produced at CDC's
	Normandale facility.
B	Add 24 microcircuit descriptions. Revise several descriptions for consistent
(2-21-77)	symbology. Make various editorial changes.
C	Add seven microcircuit descriptions. Make various editorial and technical
(5-1-77)	changes.
D	Add six microcircuit descriptions. Revise certain Op Amp data sheets to view
(8-8-77)	metal-can configurations from the bottom of the IC. Make various editorial
	and technical changes.

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or use Comment Sheet in the back of this manual.

PREFACE

This manual provides the customer engineer with a functional understanding of the microcircuits used in equipment manufactured by the Normandale facility. It is not intended to be a logic designer's handbook and does not include design ground rules for using the microcircuits.

Section 1 discusses the characteristics, operational theory, and physical packaging of TTL (transistor-transistor logic), ECL (emitter-coupled logic), and CMOS (complementary metal oxide semiconductor) microcircuit families. It concludes with some general information on operational amplifiers.

Section 2 describes the symbology used on the individual data sheets in section 3, including the meanings of the various modifiers and qualifiers found within each logic symbol.

Section 3 contains the data sheets.

Appendix A is a glossary of microcircuit terminology used in this manual.

NOTE

The data sheets in section 3 incorporate the latest CDC-approved symbology. As such, some of the symbols may be at variance with those found in the logic diagrams sections of less-recent product support manuals. This in no way lessens the validity of the data sheets with respect to those earlier manuals.

SPECIAL NOTE TO READER

Despite every reasonable effort by us, a manual of this scope may contain errors, omissions, or ambiguities. To a very large extent, we depend upon feedback from the field to correct those situations. We urge you, therefore, to let us know about what you consider to be deficiencies in this manual. And the surest way to do that is to use the postage-paid comment sheet just inside the back cover.

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SECTION 1

GENERAL THEORY

INTRODUCTION

A microcircuit is an electronic circuit in a miniature package that performs a specific binary or linear function. Microcircuit complexity varies from a few logic gates to more than 100 gates on a single silicon chip. The term small-scale integration (SSI) is sometimes used to refer to a level of complexity of up to 12 logic gates. Medium scale integration (MSI) refers to circuits containing from 13 to 100 gates. Large scale integration (LSI) generally indicates circuits containing 100 or more gates. These gates may be interconnected within a microcircuit to form flip-flops, multivibrators, etc., which in turn are further interconnected, again within an individual microcircuit, to form registers, counters, coders/decoders, multiplexers/demultiplexers, etc. Thus it is possible for a microcircuit to provide simple gating functions (AND, OR, NAND, NOR) as in SSI, or to provide complex functions (registers, counters, arithmetic logic units, memories, etc.) as in LSI.

TRANSISTOR-TRANSISTOR-LOGIC (TTL)

TTL microcircuits provide small physical size and high performance-to-cost ratio. Reliability also improves because relatively few interconnections are necessary. Most TTL microcircuits are of the monolithic type. That is, a complete circuit or group of circuits is fabricated on a single silicon chip. Another type of microcircuit is the hybrid. Hybrid circuits consist of small discrete components mounted on a ceramic substrate. A metallization pattern on the substrate forms the interconnections. Hybrid circuits usually appear in relatively small quantities. Ordinarily, microcircuits cannot be opened for repair or trouble-shooting.

STANDARD TTL CHARACTERISTICS

There are five series of TTL circuits: Standard, Low-Power, High-Speed, Schottky-Clamped and Low-Power Schottky TTL circuits. These series are functionally identical except for propagation time and power consumption. All five series are compatible; circuits from any series can interface with any other series. These series are described under their individual headings further in this section. A circuit of a series normally drives 10 circuits of the same series. However, combining circuits of different series varies the output drive capability (fan-out) from 1 to over 50. Typical values of the essential characteristics for all series are:

	Min	Nom	Max
Supply voltage	+4.75	+5.0	+5.25
High output voltage	+2.4	+3.3	
Low output voltage		+0.2	+0.4
High input voltage	+2.0	+3.3	
Low input voltage		+0.2	+0.8

The logic levels may be observed as indicated below, depending on the circuit load:

HIGH - from +2.0 to +3.3 volts.

LOW - from +0.2 to +0.8 volts.

TRI-LEVEL CIRCUITS

Tri-Level (tristate) circuits are similar to conventional TTL circuits. In addition to the normal high or low, tri-level circuits have a special control input that places the output of the circuit into an "off" (high impedance) state. In the off state, the circuit effectively disconnects from the output line. This characteristic is useful in a bus or party-line application where a number of driving circuits connect to a common transmission line, but only one circuit is active at any given time. A tri-level circuit draws significantly less input current when it is in the "off" state.

OPEN COLLECTOR CIRCUITS AND WIRED LOGIC

Some TTL microcircuits have an open-collector output. That is, the collector load or active pull-up portion of the ouput is not present. The output pin of the package connects only to the collector of an npn transistor. An open-collector output can go low only. It cannot drive the input of a following circuit high. To operate properly, an open-collector output must connect to an external pull-up resistor tied to Vcc.

More than one open-collector output may connect to the same pull-up resistor to form wired logic. This is sometimes called "collector dotting". Figure 1-1 illustrates open-collector circuits and a wired - AND gate. Each gate accomplishes the NAND operation for active-high inputs, and the NOR operation for active-low inputs. The expression for the function performed at the wired output is $Y = \overline{AB+CD}$ or $\overline{Y} = AB+CD$. Although sometimes referred to as "wired - OR" or "dot - OR", "wired - AND" is the correct description of the logic performed by this circuit.

UNUSED INPUTS

Generally unused inputs of TTL microcircuits are terminated in one of the following methods:

- Unused inputs are connected to used inputs if this does not exceed the fan-out of the driving output,
- unused inputs are connected to Vcc through a 1 kΩ resistor. The resistor protects the input from transients. Up to 25 inputs may be connected to one 1 kΩ resistor,
- unused inputs are connected to the output of an unused gate. This output must always be high.
- Unused inputs are connected to a separate supply voltage between 2.4 V and 3 V.

Leaving unused inputs open degrades the switching and noise characteristics of TTL microcircuits.

DUALITY OF FUNCTION

Figure 1-2 shows the four basic TTL gates (NAND, NOR, AND, OR). As implied by the logic symbols and truth tables, each of the two inverting gates may be considered as performing either the NAND function or the NOR function, depending upon which of the input states (high-or low-level) is regarded as being more significant-- that is, "active". Likewise, the two non-inverting gates can perform either the AND or the OR function, depending upon the polarity of the active inputs.

This principal of duality applies to all of the microcircuit families, not just to TTL. Later in this manual, these symbols are used in either representation to illustrate the logical construction of more complex circuits. When each of these composite circuits is constructed a new symbol is generated. These symbols are then used to construct yet a more complex circuit, such as flip-flops being used to construct registers, counters, etc.

BASIC TTL CIRCUITS

Generally, all TTL microcircuits are derived by using combinations of the four basic (or "standard") gates shown on figure 1-2. These standard gates may be modified in various ways to meet the requirements for faster switching speed or lower power consumption. The several "series" thus produced are differentiated as follows:

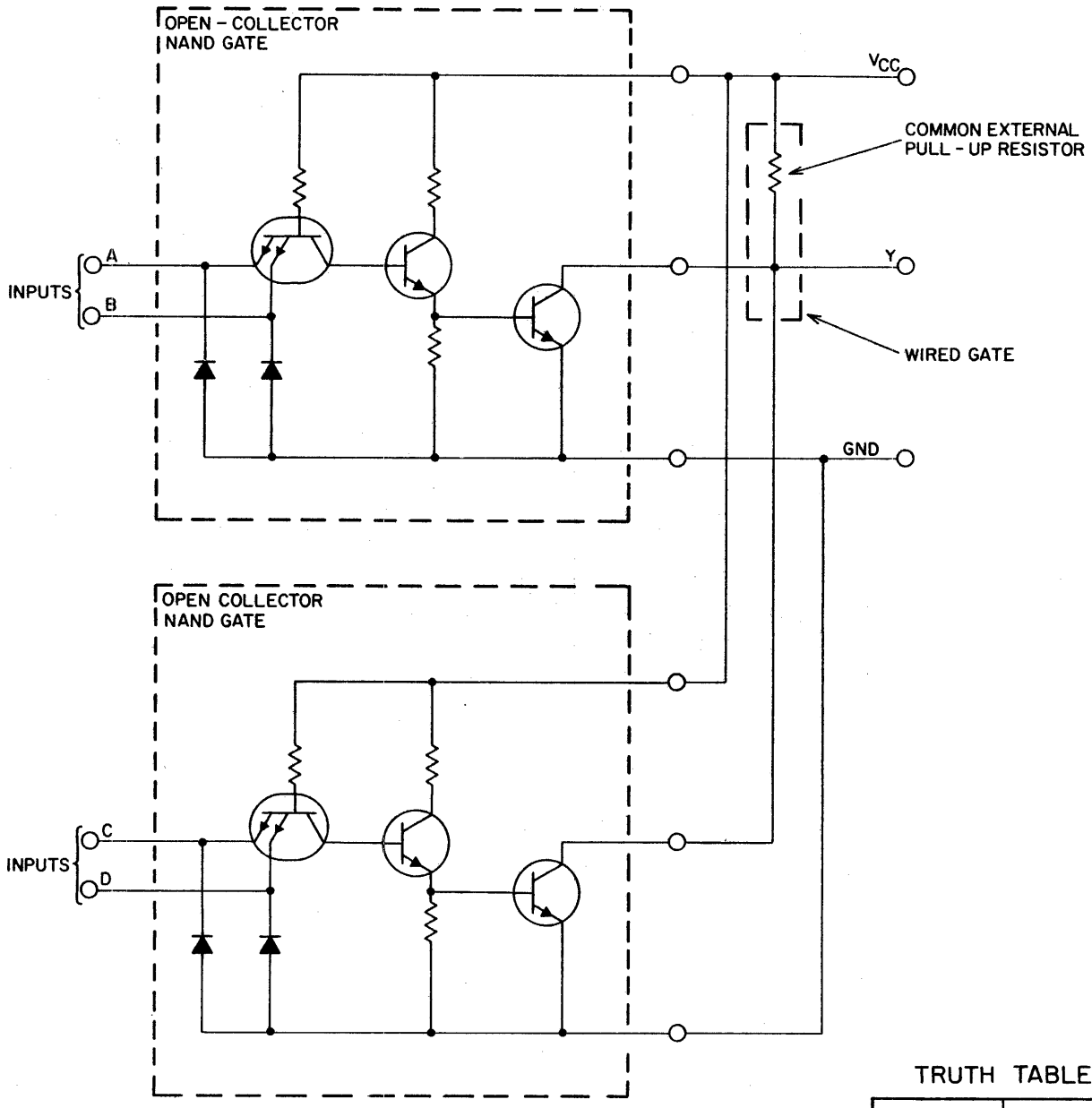
- XXX = Standard series
- XXXL = Low-Power series
- XXXH = High-Speed series
- XXXS = Schottky Clamped series
- XXXLS = Low-Power Schottky series

The following paragraphs describe the characteristics of each series. Electrical schematic diagrams are included to show how the standard NAND gate (depicted at the top of figure 1-2) is modified for each series. The other basic gate types would, of course, undergo similar alterations.

Standard Series

Because of the effect of capacity, decreasing the impedance of a circuit tends to make the circuit switch faster. However, decreasing the circuit impedance also tends to increase power consumption. The Standard Series TTL attempts to compromise speed and power requirements. Typical switching speed is 10 ns. Power consumption is 10 mW per gate. The standard-series NAND gate, shown it the top of figure 1-2, operates as follows: If one or both inputs are low, Q1 conducts, bringing the base voltage of Q2 close to ground. Q2 turns off, causing Q3 to be off and Q4 to be on. Thus, the output is high. If both inputs are high, the base-collector junction of Q1 is forward biased. This allows current to flow through R1 into the base of Q2 turning Q2 on. When Q2 is on, base current flows into Q3, and it turns on, causing the output to be low.

The multiple-emitter input transistor, Q1, replaces combinations of resistors, diodes, and transistors found in other types of logic. This configuration results in smaller size, which reduces stray capacity. Low stray capacity and low circuit impedances help to increase switching speed. At the output, Q3 and Q4 form an active pull-up or totem pole drive circuit. When the output is low, Q3 is saturated, providing a low source impedance. If the output is



TRUTH TABLE

INPUTS				OUTPUT
A	B	C	D	Y
H	H	X	X	L
X	X	H	H	L
L	X	L	X	H
L	X	X	L	H
X	L	L	X	H
X	L	X	L	H

X = IRRELEVANT

9K I A

Figure 1-1. Open-Collector Circuits and a Wired AND

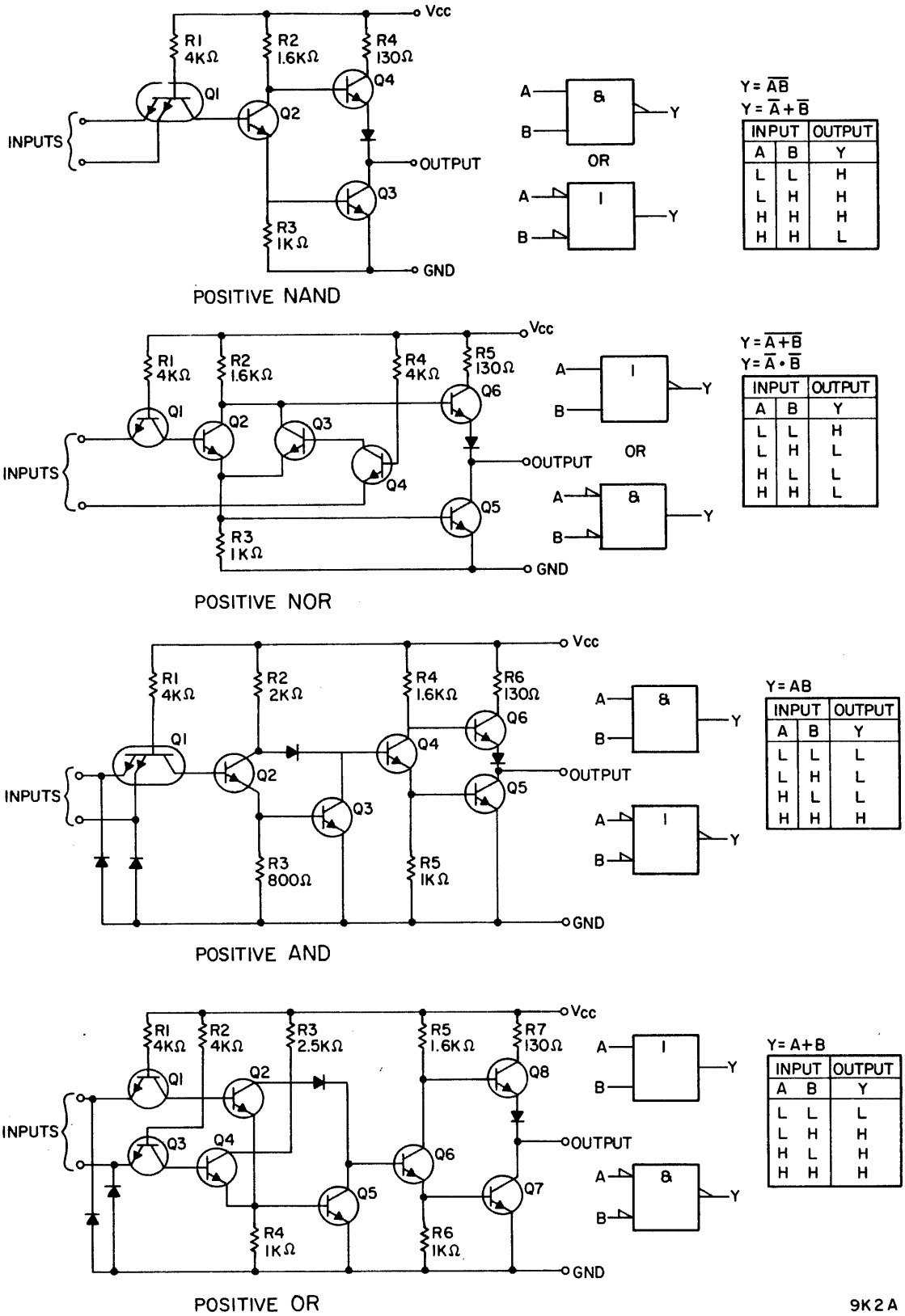


Figure 1-2. Basic TTL Gates

high, Q4 acts as an emitter-follower that also provides a low source impedance. This arrangement permits driving several loads and reduces the effect of capacity on switching time.

Low-Power Series

The low-power gate circuit is shown in figure 1-3. Typical switching speed is 33 ns, and power consumption is 1 mW per gate. Generally, an L suffix on the element identifier number indicates the low-power series.

High-Speed Series

Figure 1-4 shows the basic high-speed gate. Typical switching speed is 6 ns. Power consumption is 22 mW per gate. Usually, an H suffix on the element identifier indicates the high-speed series.

Schottky Clamped Series

Figure 1-5 shows the basic Schottky series gate. This series uses Schottky-barrier diodes as base-collector clamps. Clamping the collector prevents a transistor from saturating and thereby improves switching time. Switching time is 3 ns and power dissipation is 20 mW per gate. An S suffix on the element identifier indicates the Schottky series.

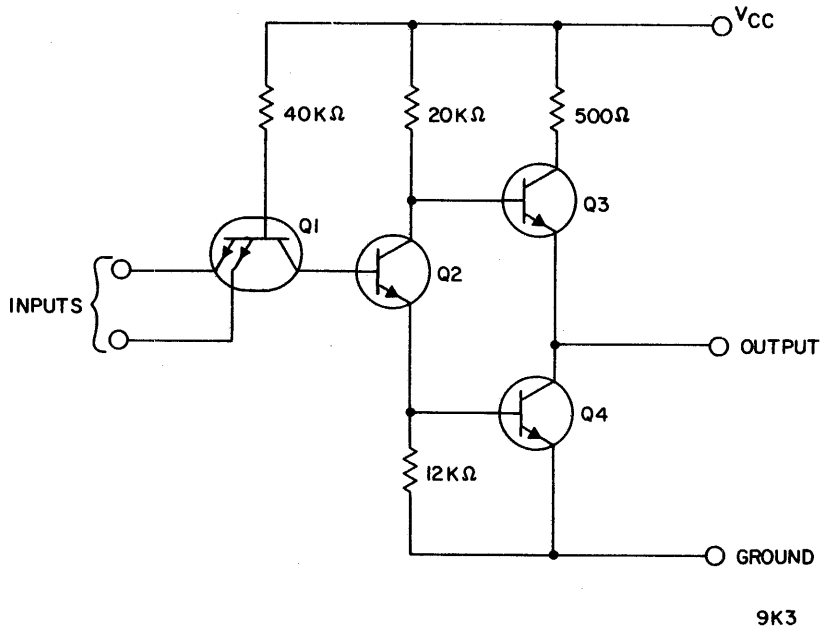


Figure 1-3. TTL NAND Circuit, Low-Power Series

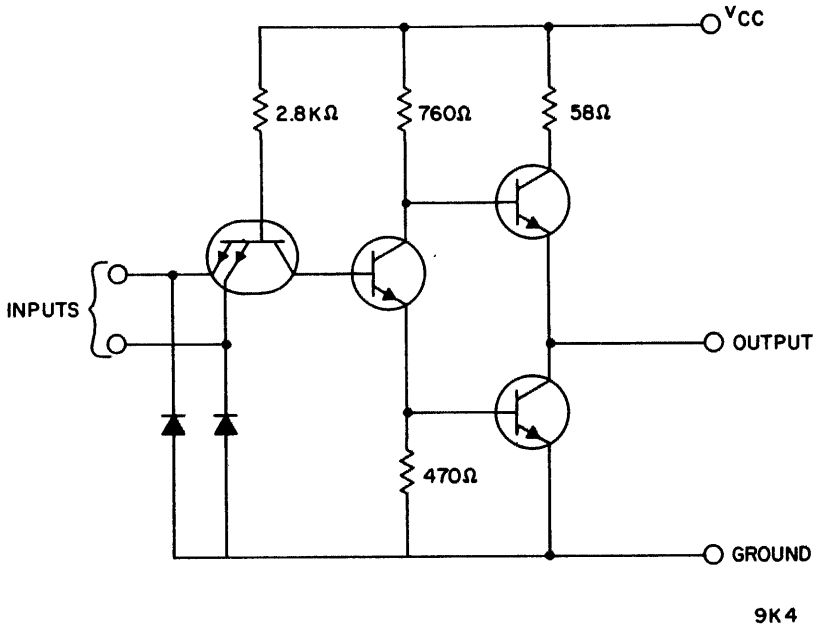
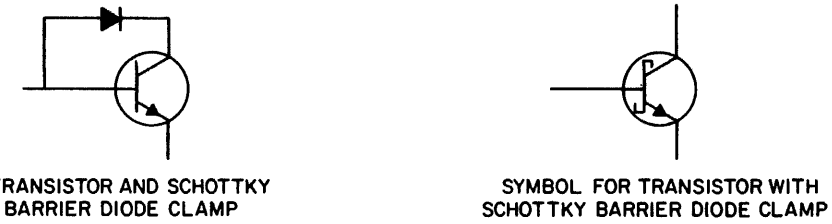


Figure 1-4. TTL NAND Circuit, High-Speed Series



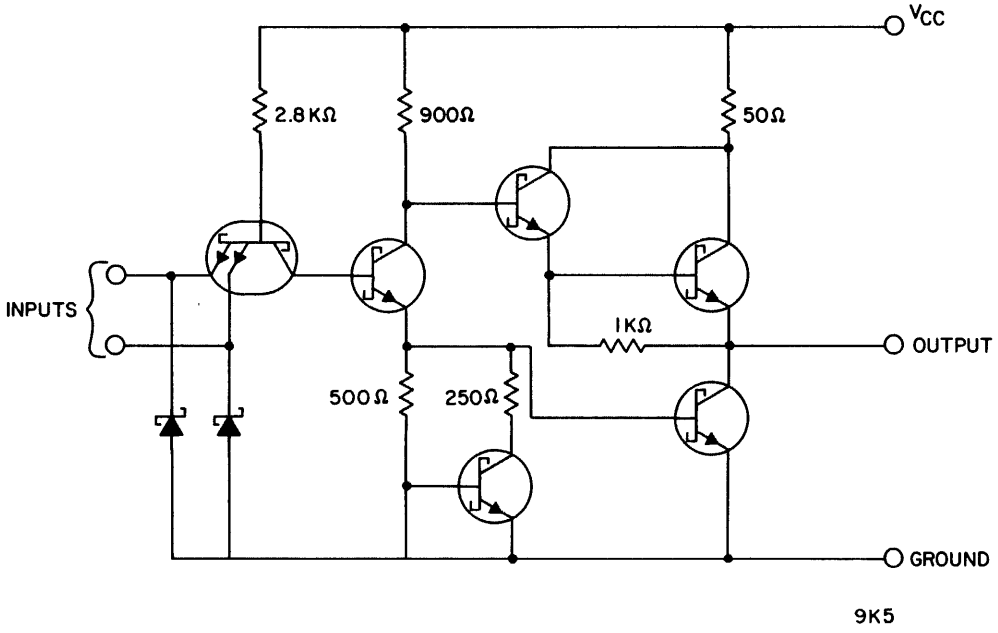


Figure 1-5. TTL NAND Circuit, Schottky Series

Low-Power Schottky Series

The low-power Schottky gate is shown in figure 1-6. The suffix letters LS on the element identifier denote this series of microcircuit. The LS series offers a happy substitute for the standard TTL microcircuits, and in fact enjoys the best speed-power product of any of the five TTL series. Switching time is typically 9.5 ns per gate (as against 10 ns for the standard series), while power dissipation is 2 mW per gate as opposed to 10 mW for the standard TTL gate.

LOGIC INTERFACE CIRCUITS

Special microcircuits are used to interface different families of microcircuits. In the case of interfacing TTL (logic levels of HIGH = +3.3 volts, LOW = +0.2 volt) to ECL (logic levels of HIGH = -0.5 volt, LOW = 1.75 volts), circuits such as illustrated in figure 1-7 are used.

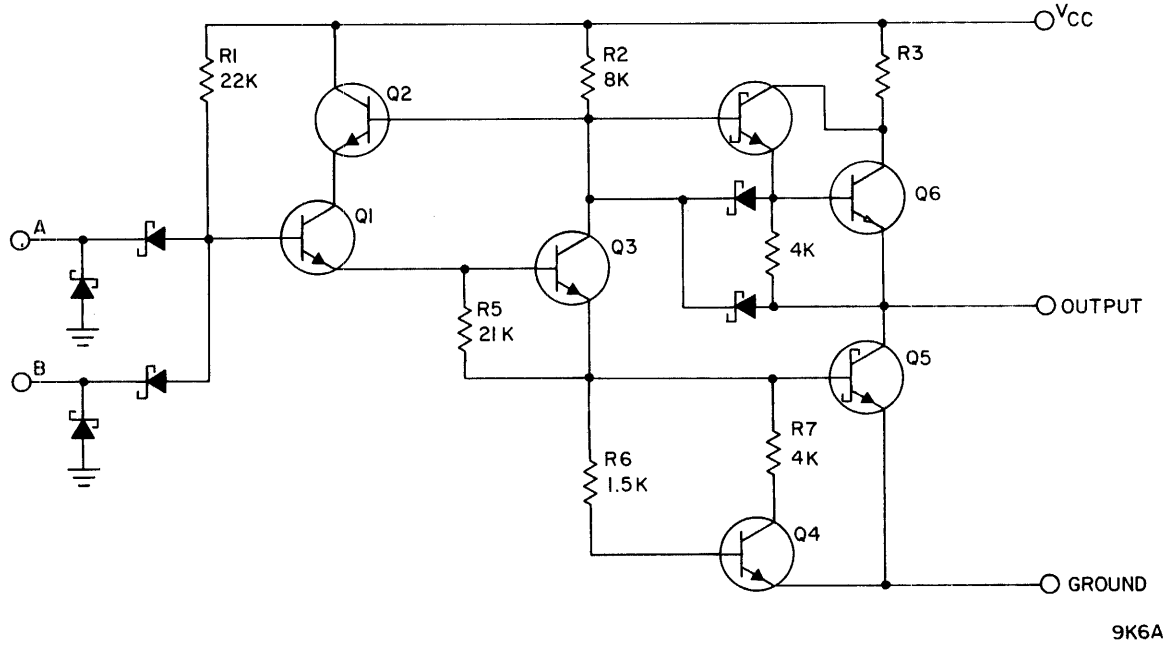


Figure 1-6. TTL NAND Circuit, Low-Power Schottky Series

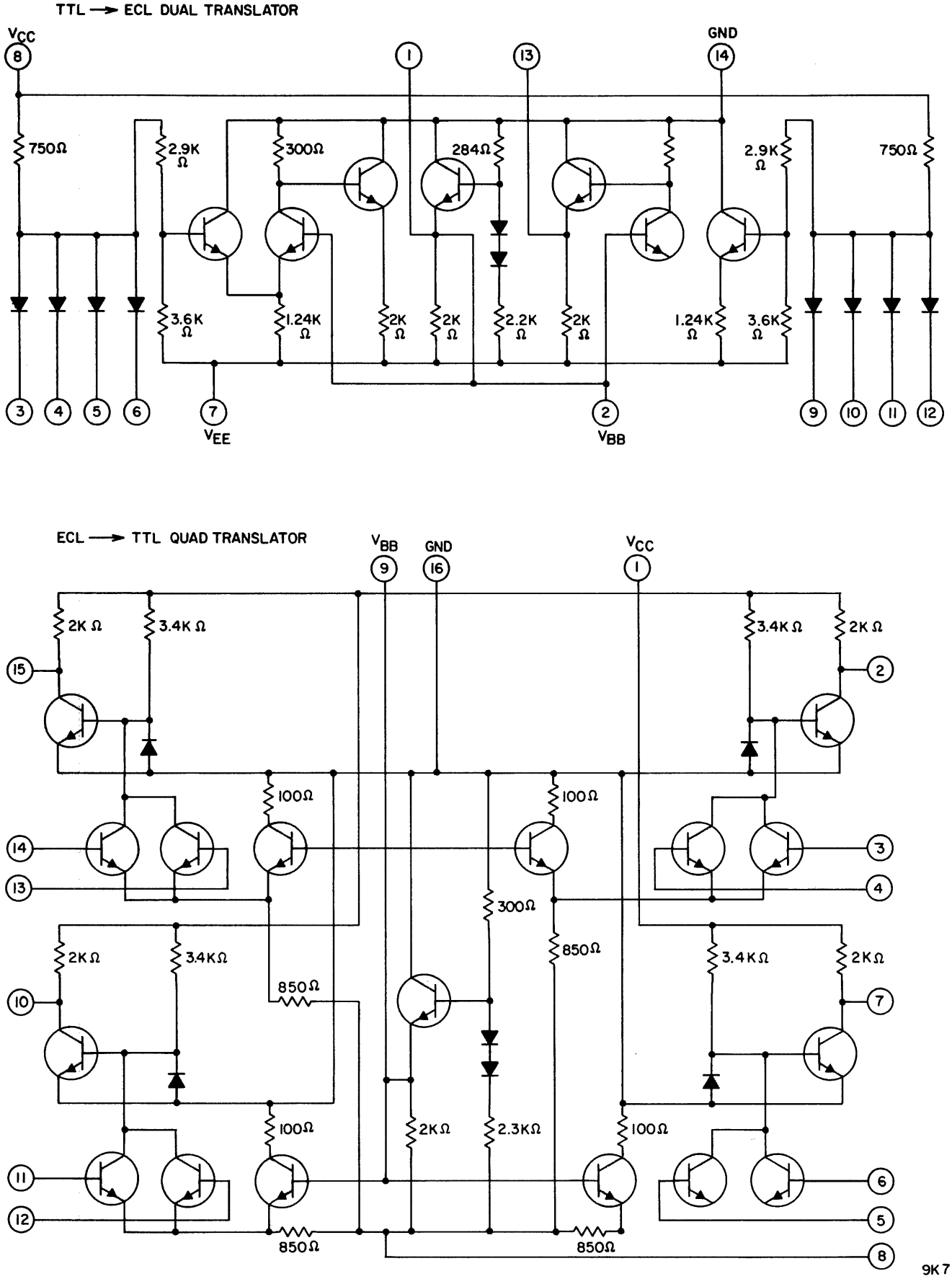


Figure 1-7. TTL/ECL Interface

TTL PACKAGING

TTL microcircuits are manufactured in several physical configurations. Three common ones are the dual-in-line packages, flat packages, and plug-in packages. These units are hermetically sealed and have from 8 to 40 pins. Flat packages and plug-in packages are available with various numbers of leads. Figure 1-8 shows an example of each package.

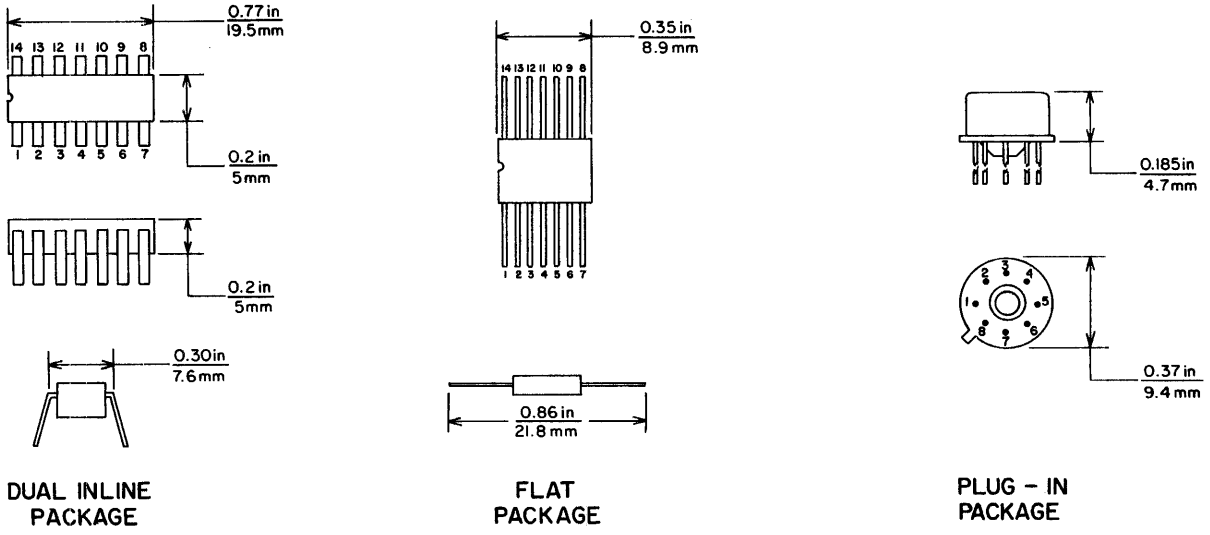


Figure 1-8. Typical TTL Packaging

EMITTER-COUPLED-LOGIC (ECL)

The emitter-coupled-logic (ECL) microcircuit is, by design, nonsaturating, and therefore avoids transistor storage time and its attendant speed limitation, characteristic of transistor-transistor logic (TTL). The high speed of ECL microcircuits has either or both of two characteristics; switching rates of over 50 megahertz and/or gate propagation delays of less than 6 nanoseconds. In general, the gate propagation delays of ECL logic are approximately 2 nanoseconds.

Some of the salient features of ECL microcircuits are as follows:

- High input impedance/low output impedance properties enable large fanout and versatile drive characteristics.
- Minimal power supply noise generation due to differential amplifier design.
- Nearly constant power supply current drain.
- Minimal crosstalk due to low-current switching on signal path.
- Low on-chip power consumption (e.g., less than 8 milliwatts in some complex function chips)
- No line drivers needed due to open emitter outputs of ECL
- Capability of driving twisted pair transmission lines of up to 1000 feet in length.
- Simultaneous complementary outputs available at logic element output without using external inverters.

LOGIC AND POWER LEVELS

	Nom	Min	Max
Supply voltage (V_{EE})	-5.2		
Noise immunity	*	*	*
High output voltage	-0.924	-0.96	-0.81
Low output voltage	-1.75	-1.65	-1.85
High input voltage		-1.105	
Low input voltage		-1.85	-1.475

*Noise immunity of a system involves line impedances, circuit output impedances, propagation delays, and noise margin specifications. Noise margin is a dc parameter calculated from specified points tabulated on an ECL data sheet for the particular microcircuit in question.

CIRCUIT THEORY

A typical ECL gate circuit is shown in figure 1-9 and consists of a differential amplifier input circuit, a temperature and voltage compensated bias network, and emitter-follower buffering transistors for transmission line driving. To explain operation of the gate, each of the major sections is discussed in the following paragraphs.

The differential amplifier is an emitter-coupled current switch consisting of transistors Q1 through Q5. The multiple gate inputs provide an OR function (Q1 through Q4) which is amplified by current switch Q5. To understand the gate's operation, assume that all gate inputs are low (-1.75 V and Q1 through Q4 therefore cutoff). Under this condition, Q5 is forward biased, the base being held at -1.29 volts by the bias supply voltage (V_{BB}), and its emitter is at one diode voltage drop (0.8 V) more negative than its base (-2.09 volts total). The base-to-emitter differential then becomes the difference between the low logic level (-1.75 V) and V_{BB} (-1.29 V), or 0.34 volt. Since this voltage is less than the threshold voltage to turn Q1 through Q4 on, they remain in the cutoff state. The current through Q5 will be about 4 milliamperes with a voltage of -2.09 volts at the emitter nodes of Q1 through Q4 using an emitter resistor R_E of about 780 ohms.

The emitter-follower outputs buffer the current switch from loading and restore output voltages to proper ECL levels. The OR output is obtained through Q8 producing the low-level logic signal of -1.75 volts. Similarly, the NOR output is obtained through Q7 producing the high-level logic signal of -0.924 volt.

When any or all of the logic inputs is switched to the high logic level, the appropriate input transistor turns on, a current flows through resistor RC1 in the differential amplifier, and transistor Q5 cannot sustain conduction due to forward biasing, so is cut off. After translating through the emitter followers, the NOR output is a nominal -1.75 volts and the OR output a nominal -0.924 volt.

The differential action of the switching transistors (one section off when the other is on) produces simultaneous complementary signals at the output.

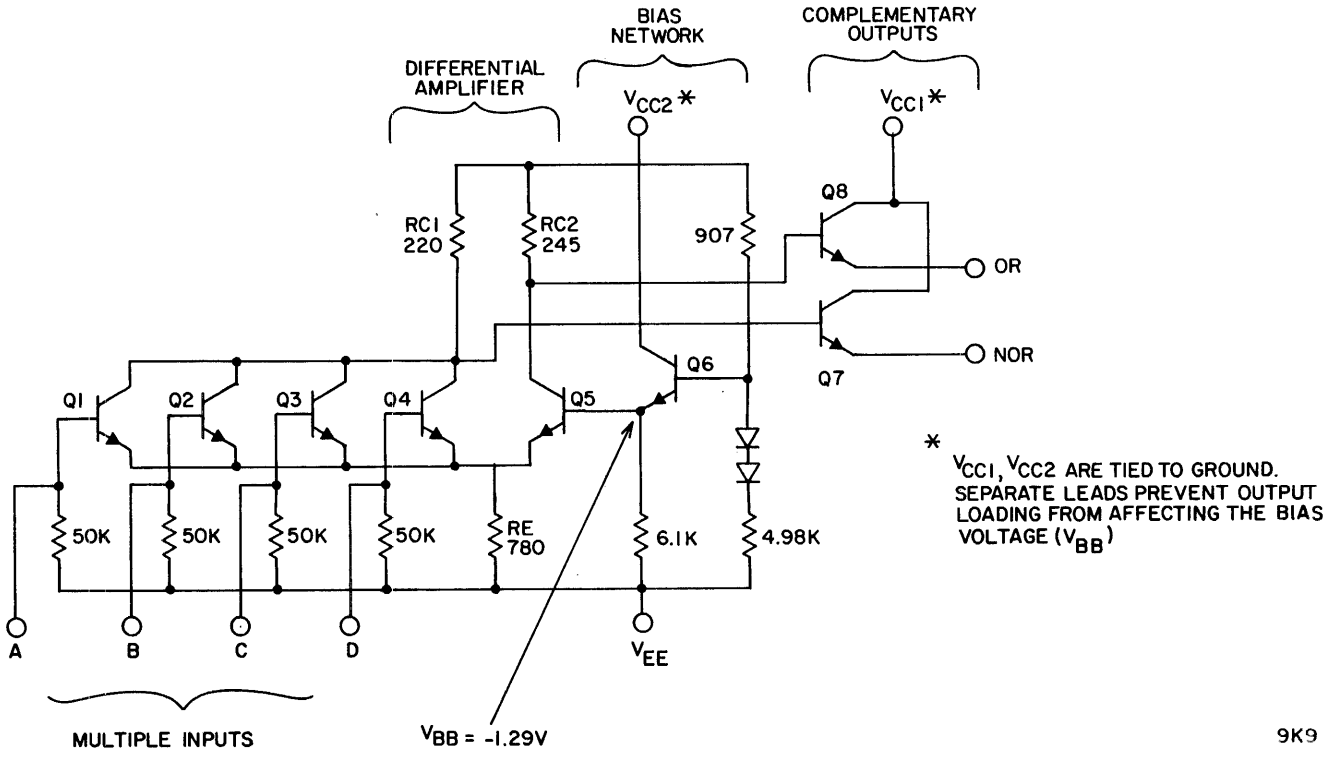


Figure 1-9. Typical ECL Gate

The bias network provides a reference voltage (V_{BB}) of -1.29 volts. This network compensates for variations in power supply voltage and temperature changes to ensure that the bias voltage threshold point remains in the proper operating region.

LOADING CHARACTERISTICS

The differential input to ECL circuits offers several advantages. Its common mode rejection feature offers immunity against power supply noise, and its relatively high input impedance enables any circuit to drive a large number of gate inputs without deterioration of noise margins. The dc loading factor (the number of gate inputs of the same family that can be driven by a circuit output) for ECL circuits is 90. While dc loading causes a change in output voltage levels, thereby tending to affect noise margins, ac loading increases the capacitances associated with the circuit, and therefore affects circuit speed. For ECL circuits, best performance at fanouts of greater than 10 will occur with the use of transmission lines. The propagation delay and rise time of a driving gate are affected very little by capacitance loading along a matched parallel-terminated transmission line. However, the delay and characteristic impedance (Z_o) of the transmission line itself are affected by the distributed capacitance and loading due to stubs off the line. Maximum allowable stub lengths for loading of an ECL transmission line vary with line impedance. For example, a transmission line with a Z_o of 50 ohms will accept stubs 4.5 inches (114.3 mm) long. When the Z_o of the line is changed to 100 ohms, stubs may be only 2.8 inches (71.1 mm) long.

The input loading capacitance of an ECL 10109 is 2.9 picofarads. Therefore, fanouts in a non-transmission line environment should be limited to a maximum of 10 loads due to line delay increases which in turn limit speed.

UNUSED INPUTS

The input impedance of the differential amplifier used in the typical ECL circuit is high when the applied signal level is low. Under low signal conditions, any leakage to the input capacitance of the gate may cause a gradual buildup of voltage on the input lead, thereby adversely affecting switching characteristics at low repetition rates. All but a few of the ECL circuits contain input pull-down resistors between the input transistor bases and the -5.2 volt power supply (V_{EE}). Therefore, unused inputs may be left unconnected because leakage current is dissipated by the resistor, keeping inputs sufficiently negative so that circuits will not trigger due to noise coupled into those inputs.

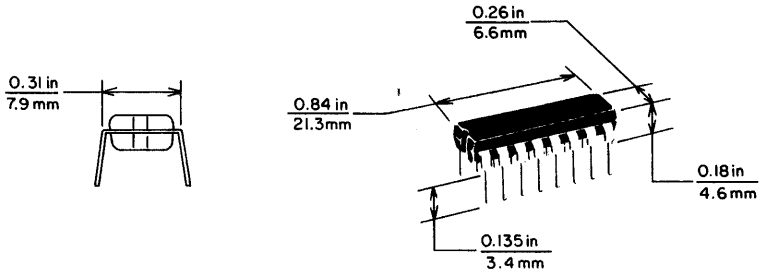
Input pull-down resistors must not be used as pull-down resistors for preceding open-emitter outputs. If an ECL circuit (such as the 10116) does not contain input pull-down resistors, one input of a circuit must be connected to the reference bias supply voltage (V_{BB}) and the other input to V_{EE}.

WIRED LOGIC

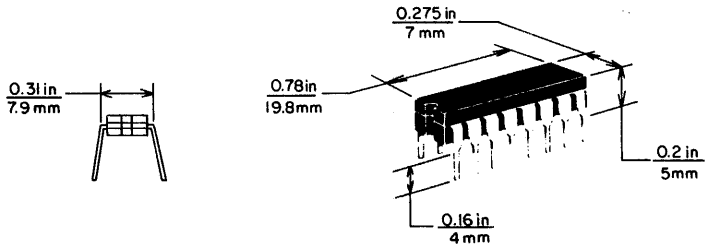
Wired-OR gates can be produced in ECL microcircuits by wiring output emitters together (to a maximum of 10) outside their respective packages. Wired-OR gates can be connected directly to a bus, also. Propagation delay is increased by approximately 50 picoseconds per wired-OR gate. To economize on power dissipation, a single output pull-down resistor is used per wired-OR gate. Normally, wired-OR gates are connected between gates on the same logic board.

ECL PACKAGING

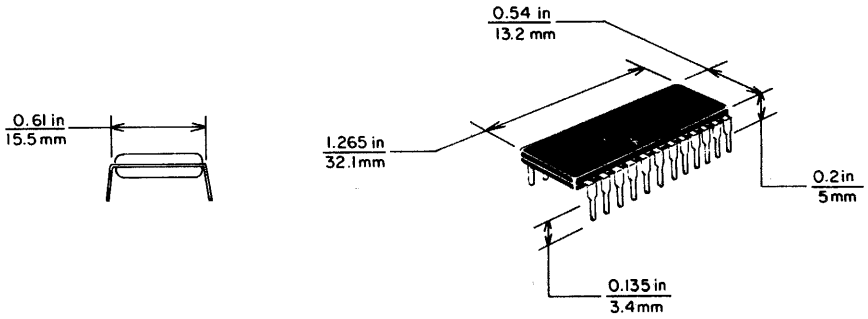
ECL microcircuits are manufactured in a variety of physical configurations. Two of the more common ones used for the ECL microcircuits described in this manual are the ceramic dual in-line and the plastic dual in-line cases having both 16 and 24 pins, depending upon the size of the package. Figure 1-10 illustrates these packages.



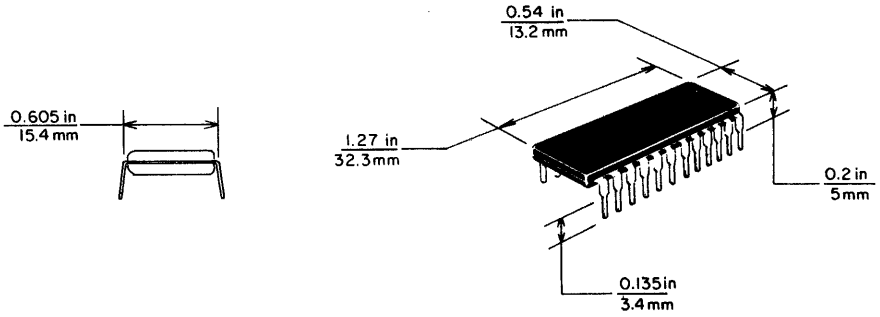
16-PIN DUAL INLINE PLASTIC (CASE 648)



16-PIN DUAL INLINE CERAMIC (CASE 620)



24-PIN DUAL INLINE PLASTIC (CASE 649)



24-PIN DUAL INLINE CERAMIC (CASE 623)

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Figure 1-10. Typical ECL Packaging

COMPLEMENTARY METAL-OXIDE SEMICONDUCTOR (CMOS)

CMOS microcircuits use four-terminal, enhancement-type field effect transistors (FETs), the symbol for which is given in figure 1-11, to form the basic inverter.

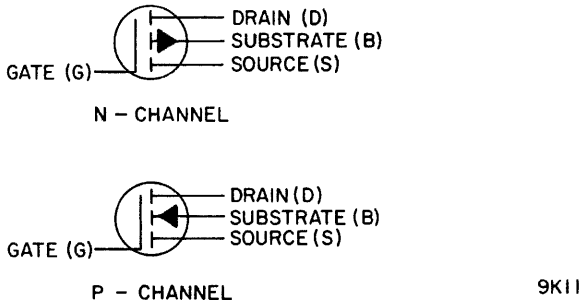


Figure 1-11. FET Symbol

As shown in figure 1-12, a complementary inverter may be formed by applying the input signal to the gates of two opposite-polarity FETs.

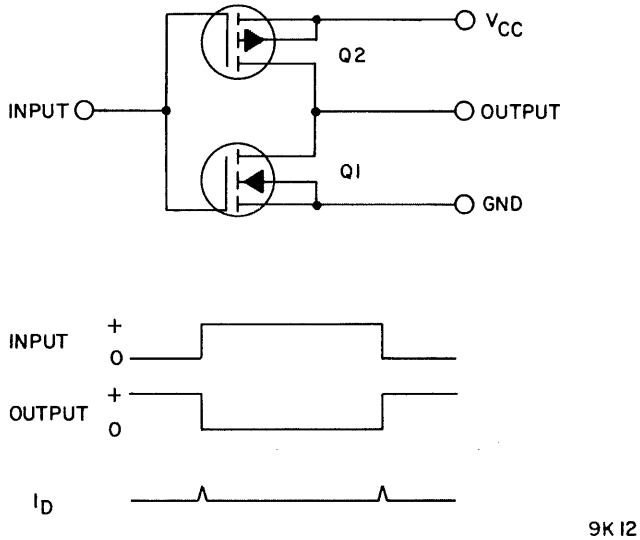


Figure 1-12. Typical CMOS Inverter

In this circuit, a low input signal turns the N-channel transistor Q1 off, and turns the P-channel transistor (Q2) on. The output is shorted to the positive supply, but virtually no load current is drawn if the load is assumed to be another CMOS device with high-impedance input. When the input signal goes high, Q1 is turned on and Q2 is turned on. The output is pulled to ground, but no steady-state current is drawn. Power dissipation in the circuit is thus limited to the crossover points as the device changes state, and with proper design is typically 2 nanowatts per gate.

ADVANTAGES/DISADVANTAGES

Advantages

- High circuit density
- High noise immunity
- Lower power dissipation (2.5 nW per gate, typical)
- High fan-out to other CMOS elements (>50)
- Logic swing independent of fanout
- Input threshold is constant over wide temperature range (5% variation, typical)

Disadvantages

- Fabrication complex and more costly than TTL or ECL
- Buffering required when driving several TTL loads
- Level translation required when driving ECL loads
- Characteristic complementary output configuration precludes use of "wired OR" schemes.
- Inputs extremely electrostatic sensitive -- require special precautions when handling.

OPERATING VOLTAGES

An additional advantage of the CMOS family is its wide range of operation voltage (V_{DD}), which may vary from 3 V dc to 16 V dc although, as is shown later, operating

speed suffers for the lower supply voltages. Noise immunity is typically 45% of the supply voltage. The range of input and output voltages is shown below for a Vcc of +5 V.

	Min	Nom	Max
High output voltage	4.99	5.0	-
Low output voltage	-	0	0.01
High input voltage	3.5	5.0	-
Low input voltage	-	0	1.5

INPUT PROTECTION NETWORK

CMOS devices can be seriously damaged if subjected to high electrical fields in the gate oxide region. Any potential over about 100 V between the gate and the substrate breaks down the oxide, resulting in permanent damage. The input protection network shown in figure 1-13 protects the CMOS against voltages in the hundreds region, which is normally sufficient for ICs mounted on a circuit card that is already plugged into a logic-chassis connector. When removing, replacing, shipping, or otherwise handling these electrostatic-sensitive cards, special precautions should be observed to prevent static buildup between the handler and the card. These precautions are outlined in the maintenance manual for any equipment using such cards. The CE is strongly advised against attempting to remove and replace CMOS ICs on these cards; adequate measures to avoid harmful electrostatic discharges during such repair procedures are simply not realizable in the field.

The diode-resistor input protection network shown in figure 1-13 is built into every external input lead as part of the fabrication process. The circuit, while adding some delay time, provides protection by clamping positive and negative potentials to V_{DD} and ground, respectively. (The protection network is not usually shown in CMOS electrical schematic diagrams.)

The series isolation resistor, R_S, is typically 1500 ohms. Diodes D1 and D2 clamp the input voltages between Vcc and ground. Diode D3 is a useful parasitic structure resulting from the diffusion fabrication of R_S. The 6 to 7 ns delay of R_S allows excess energy present at the input pin to be diverted through the protective diodes before reaching the sensitive gate dielectric.

Diodes D1 and D2 have a sharp 30-35 volt avalanche breakdown characteristic. Positive (breakdown mode) and negative (forward conduction) over-voltage protection, with respect to ground when V_{DD} is open, is provided by D1.

Diode D2 similarly provides positive (forward conduction) and negative (breakdown mode) protection with respect to V_{DD} when ground is left open. Both diodes limit the applied voltages to well within the critical breakdown potentials of the gate dielectric. The avalanche characteristic of D3 and D4 is typically 120 V.

REPRESENTATIVE CMOS GATES

Figure 1-14 contrasts a 2-input NAND with a 2-input NOR. The dashed-line boxes enclose the output buffer that is usually a part of the gate. Buffering achieves high performance, standardized output drive, highest noise immunity, and decreased sensitivity to output loading.

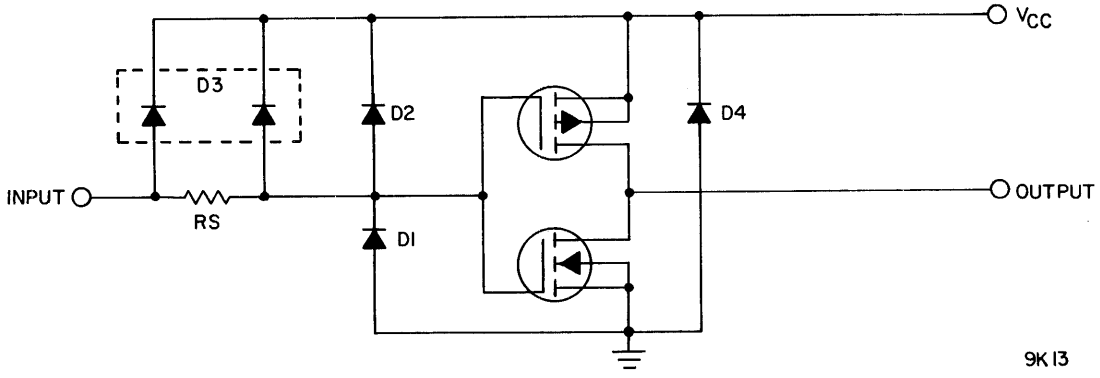


Figure 1-13. Diode-Resistor Input Protection

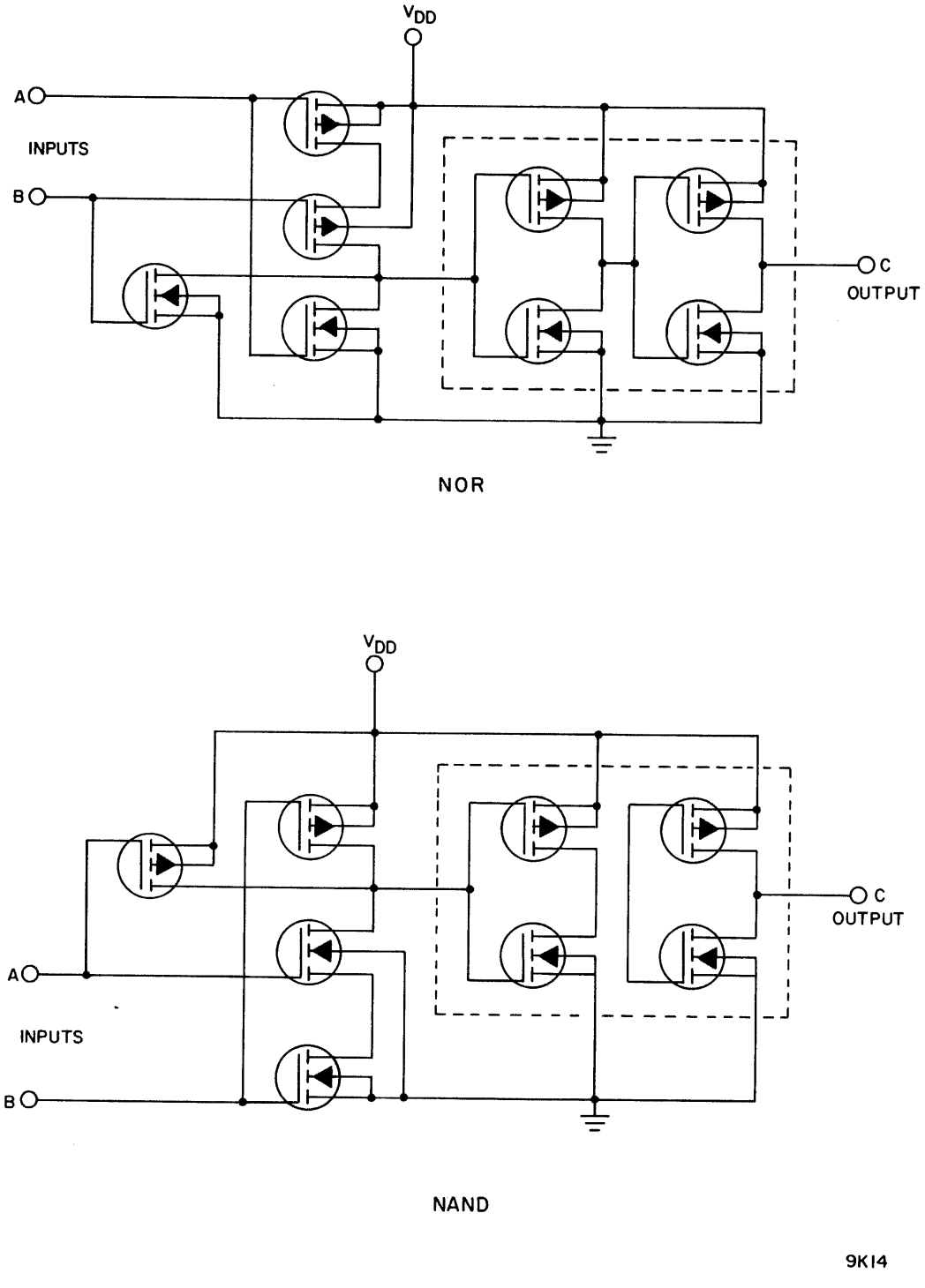


Figure 1-14. Typical CMOS Gates

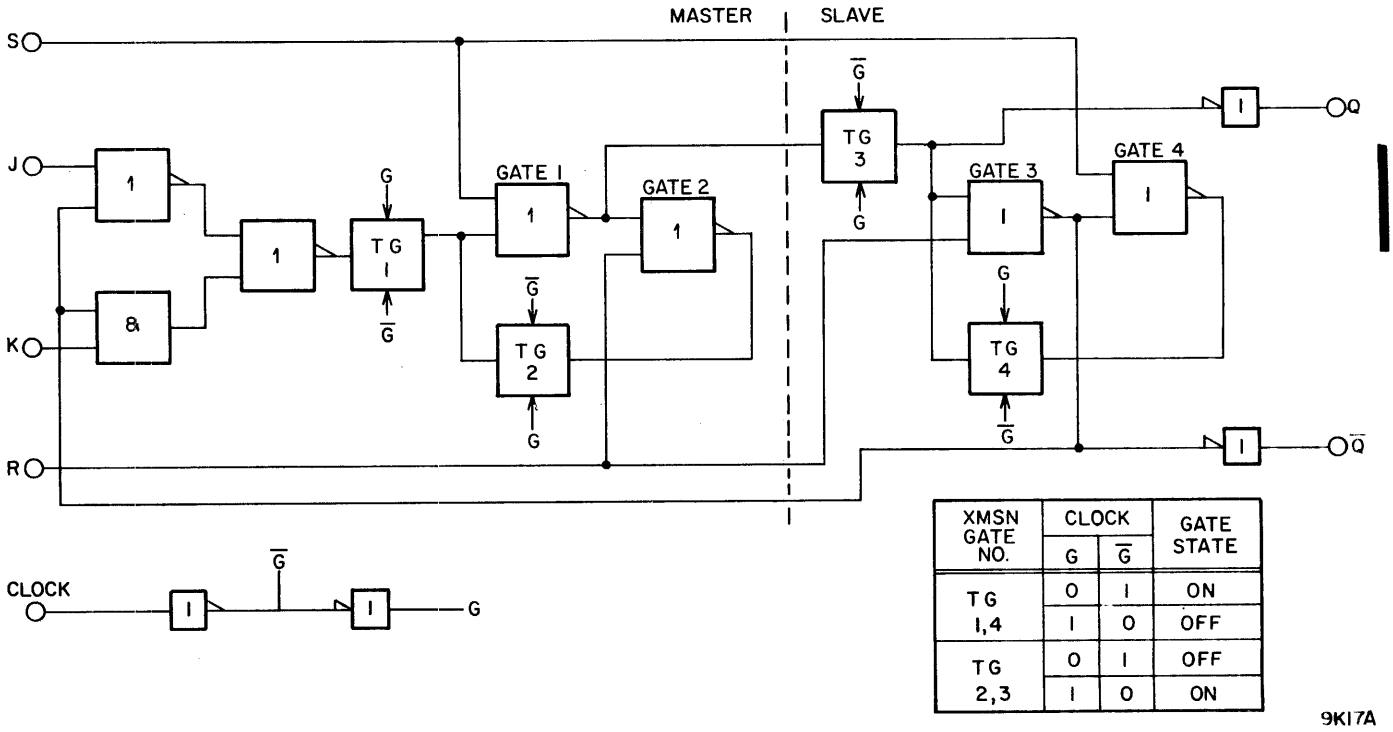
TRANSMISSION GATE

The transmission gate (TG) is a valuable tool in CMOS design. Two representations of the gate, as found in vendor literature, are shown below. The symbol on the left is used in functional diagrams in this manual.

The two control inputs, one on the top and the other on the bottom of the symbol, are most usually fed complementary signals. A high on the top control input turns the gate off; a high on the bottom control input turns the gate on.

A typical use of the transmission gate is shown in figure 1-15, which depicts a positive-edge-triggered J-K master-slave FF (circuit 4027). Here, four transmission gates are controlled by complementary clock signals (G, $\overline{G}$). When the clock is low, TG1 and TG4 are on, while TG2 and TG3 are off. This logically disconnects the Master from the Slave. Gates 3 and 4, however, are cross-coupled through TG4 (which is on), and the output state remains stable. Assuming that the S and R inputs are inactive, TG1 transmits the state of the J and K inputs to Gates 1 and 2.

When the clock goes high, TG2 and TG3 turn on, while TG1 and TG4 turn off. Now gates 1 and 2 are cross-coupled through TG2, and latch into the state they held when the low-to-high clock transition took place. With TG3 on, the logic state of the Master section (output of Gate 1) is fed through an inverter to the Q output. Simultaneously, the $\overline{Q}$ output receives the double inverted output of Gate 1.



XMSN GATE NO.	CLOCK G	CLOCK $\overline{G}$	GATE STATE
TG 1,4	0	1	ON
	1	0	OFF
TG 2,3	0	1	OFF
	1	0	ON

Figure 1-15. Use of Transmission Gates in J-K Flip-Flop Circuit

OPERATING SPEED

Propagation delay and rise/fall times are functions of the device temperature, operating voltage, and output load capacitance. Delay and transition times increase approximately 1/4 of one percent for each degree Celsius above +25°C, and decrease approximately as the inverse of the operating voltage. For a given V_{DD}, the rise, fall, turn-on and turn-off times are about equal for a load capacitance of 15 picofarads and increase at different rates above that point. The table below gives representative figures.

DELAY/TRANSITION TIMES FOR VARIOUS OPERATING VOLTAGES

Time Measured	V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V			Units
	Load Capacitance									
	15	50	100	15	50	100	15	50	100	pF
Turn off/on	60	120	200	20	40	65	10	25	40	ns
Fall	60	130	220	30	60	110	20	40	70	ns
Rise	60	220	320	30	90	170	20	60	120	ns

UNUSED INPUTS

Unused CMOS inputs should be connected to an appropriate logic voltage, depending upon the function of the logic device. Unused NAND inputs should be connected to the +5 V bus, unused NOR inputs to ground. This prevents the input protection structure from floating to some undesired voltage level that prevents the device from functioning properly. In addition, "floating" inputs may be subjected to electrostatic potentials that will permanently damage the device.

CMOS/TTL INTERFACE

The majority of CMOS devices will not sink the 1.6 mA required for the logical zero input (+0.4 V) to a TTL device. The sinking capability is usually increased by using a 2- or 4-input NOR gate (CMOS) to drive the TTL input. For multiple TTL inputs, special CMOS buffers are used. Sourcing the µA-range needed for a TTL logical one is no problem for the CMOS device.

When converting from TTL to CMOS, it is important that the TTL output device does not source other TTL circuits, but only the CMOS input. (Sourcing 400 µA for a TTL logical one drops the TTL output to about 2.4 V, considerably below the 3.5 V CMOS threshold required for a logical one.) Sourcing the 10 pA for a CMOS logical one results in a TTL output of around 3.6 V. This is adequate, but provides little noise margin. For this reason, a 2000-ohm pull-up resistor is usually inserted between the TTL output and Vcc.

CMOS/ECL INTERFACE

The -5.2 V typical for an ECL supply is easily handled by a CMOS device. If higher negative voltages are advisable because of required CMOS speed, a diode clamp on each ECL input is required to prevent the input from going below the -5.2 V ECL supply.

Level translation is required when going from ECL to CMOS. The 800-mV output swing of an ECL device is not sufficient to drive a CMOS input, so a pnp transistor is used (figure 1-16). A diode in series with the transistor's emitter provides a reverse bias of about 900 mV, which is beyond the output voltage typical of an ECL logical one (-0.924 V). The transistor switches from about -0.9 V to -5.2 V, which is well within the -1.7 V typical for an ECL logical zero output.

CMOS PACKAGING

CMOS microcircuits are manufactured in dual-inline ceramic (DIC) and dual-inline plastic (DIP) packages with 14, 16, or 24 pins. Figure 1-17 shows the various packaging dimensions.

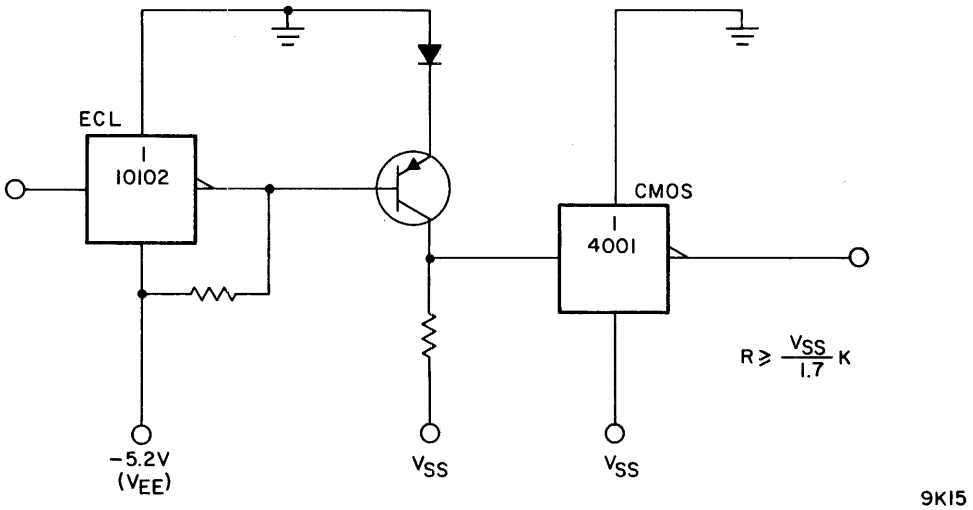
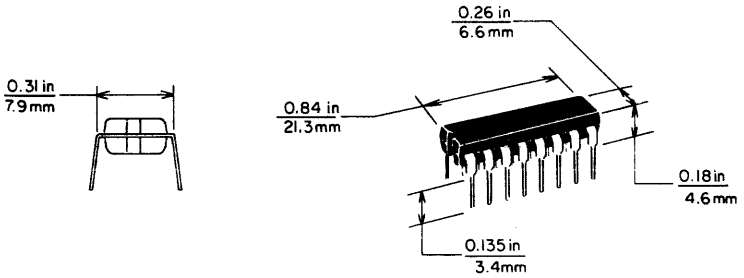
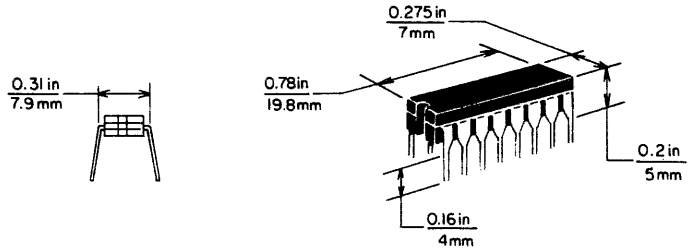


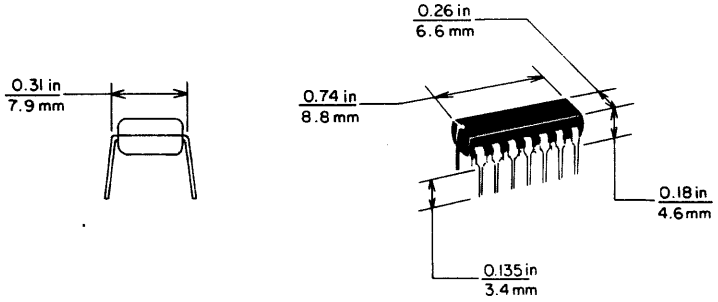
Figure 1-16. ECL-To-CMOS Interface



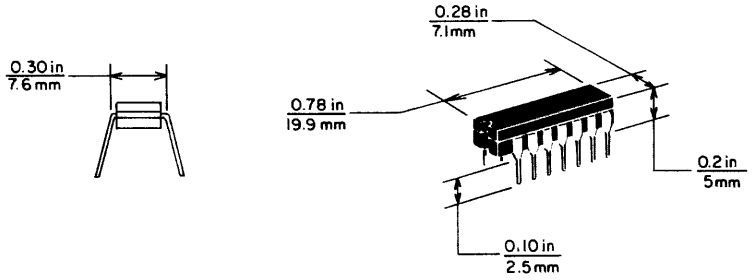
16-PIN DUAL INLINE PLASTIC (DIP) (CASE 648)



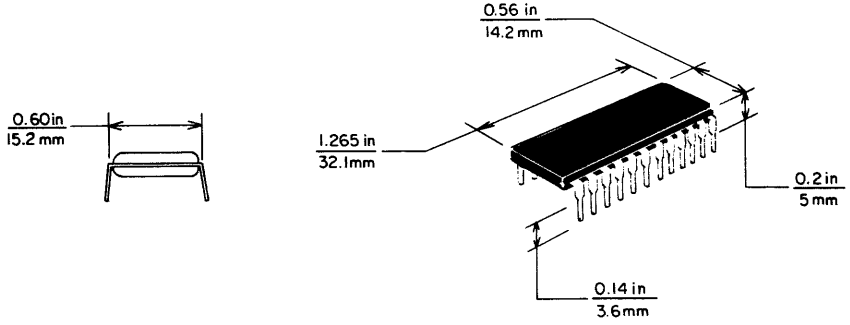
16-PIN DUAL INLINE CERAMIC (DIC) (CASE 620)



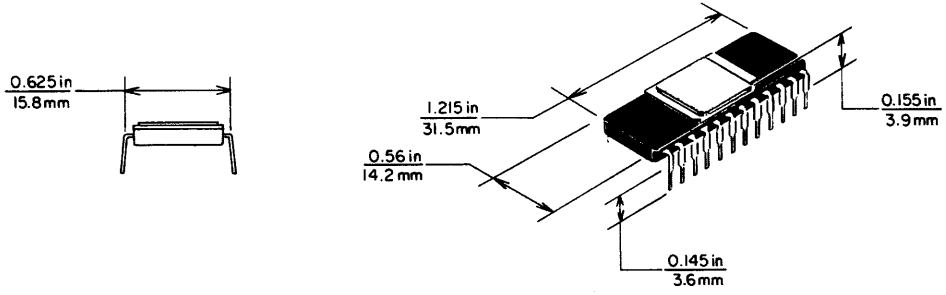
14-PIN DUAL INLINE PLASTIC (DIP) (CASE 646)



14-PIN DUAL INLINE CERAMIC (DIC) (CASE 632)



24-PIN DUAL INLINE PLASTIC (DIP) (CASE 709)



24-PIN DUAL INLINE CERAMIC (DIC) (CASE 684)

9K16-1

9K16-2

Figure 1-17. Typical CMOS Packaging

OPERATIONAL AMPLIFIERS

INTRODUCTION

The operational amplifier (op amp) is a high-gain integrated circuit that can apply signals ranging in frequency from dc to its upper frequency limit, which may be more than one megahertz. It is used frequently in a disk drive as a linear amplifier of servo analog signals. Because of its versatility, however, it has multiple applications.

The op amp approaches the following characteristics of an ideal amplifier:

1. Infinite voltage gain
2. Infinite input resistance
3. Zero output resistance
4. Zero offset: output is zero when input is zero
5. High bandwidth frequency response

BASIC CIRCUIT ELEMENTS

Figure 1-18 is a simplfied schematic of a typical op amp with its basic feedback network. Detailed circuit analysis information may be obtained by referring to the manuals prepared by the applicable manufacturers.

INPUT STAGE

All op amps utilize a differential amplifier in the input stage. This circuit may be relatively simple, as shown, or may consist of multiple circuits with FETs or Darlington-connected transistors. The advantage of this type of amplifier is that it amplifies the difference between the two input signals. For example, if 10 mV are applied to the non-inverting input while 9 mV are applied to the inverting input, the 1 mV difference is amplified. The amplification, which may be a voltage gain of up to 100000, is linear until the op amp saturates or until increasing frequency causes rolloff.

If the same input is applied to both input terminals, the signal is referred to as the common-mode input signal. In the preceding example, 9 mV is the common-mode input, while 1 mV is the differential input. In the ideal op amp, the output is zero with identical inputs; only the difference (1 mV in this case) is amplified. Since the common-mode input is not amplified, signals common to both, such as noise and hum, are cancelled.

SECOND STAGE

Not all op amps have a second stage. If used, however, it may contain additional amplification and level shifting.

BASIC CIRCUIT FUNCTIONS

Resistors R1 and R2 provide degenerative feedback to control the overall gain of the circuit. As long as the ratio R2/R1 is low compared to the open loop gain at the operating frequency, circuit gain is independent of the characteristics of the specific op amp.

Rapid analysis of this circuit is possible if two basic principles of op amps are assumed:

1. Insignificant current flows into either input terminal; therefore it is assumed to be zero.
2. The differential voltage (V3) is insignificant and therefore is assumed to be zero.

Rule #1 may be presumed since the input impedance is very high. As a result, all current (I1) entering the summing point must leave it (I2). These currents are:

$$I1 = V1/R1$$

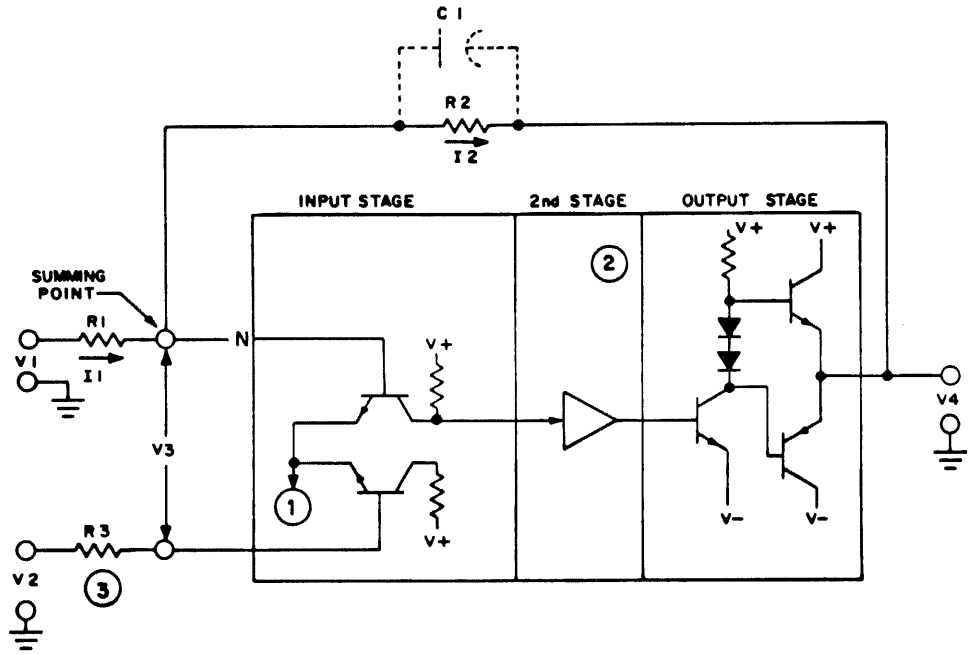
$$I2 = -V4/R2$$

The minus (-V4) indicates that the output is the inversion of the input. Since no current flows into the op amp, I1 must be equal to I2. By Ohm's Law:

$$V4/V1 = -R2/R1 \text{ or } V4 = -V1\ (R2/R1)$$

Therefore, the output is simply the ratio of R2/R1. This linear output/input relationship holds true as long as the input (V1) is not of sufficient amplitude to saturate the op amp.

Resistor R2 is frequently shunted by a capacitor. This controls the roll-off characteristics of the circuit where the full op amp bandwidth is not required. The effective feedback to the input is the resistance of R2 in parallel with the capacitive reactance of C1. Capacitive reactance decreases as frequency increases. Therefore, as frequency increases, the effective impedance of R2/C1 decreases to reduce overall gain.



NOTES;

(1) TO COMMON CONSTANT-CURRENT SOURCE.

(2) NOT APPLICABLE TO ALL TYPES. REFER TO MANUFACTURER'S DATA SHEET.

(3) FOR BALANCED INPUT IMPEDANCE,

$$R3 = \frac{R1\ R2}{R1+R2}$$

7J133A

Figure 1-18. Simplified Op Amp Schematic

If C1 is large enough, its charging time becomes more of a factor. The output cannot react as fast as the input may change. This is the integrating or low pass function. For example, doubling the frequency halves the gain. The output is the mathematical integral of the input when the effects of C1 predominate over the effects of R2. Thus, if the input voltage is proportional to velocity, the output is proportional to distance.

Since there is actually a slight current (measured in nanoamperes) entering the differential stage, the difference or unbalance between the two input currents would be amplified. This results in an error known as dc offset; that is, the output would be non-zero with a zero common-mode input. If, however, the currents are made equal, that is, the same input impedance is presented to both, they are therefore common-mode and are cancelled. Resistor R3 is selected to balance out the offset voltage and current by making the impedance to ground of the two inputs equal.

Rule 2 holds true as long as feedback is provided by R2 or its equivalent. As long as the amplifier is not saturated, it will adjust its output voltage to maintain the differential voltage V3 at zero. Therefore, the summing point is at V2. Since V2 is usually at ground potential, the summing point is also at ground. This is a virtual ground; that is, it is at ground potential even though there is no connection between this point and true ground. If the summing point is monitored with an oscilloscope, little or no signal can be observed.

Typical op amp circuit functions are illustrated in figure 1-19.

SCHMITT TRIGGER CIRCUITS

Operational amplifiers can also be connected in the Schmitt trigger configuration (figure 1-20). Note that the degenerative feedback path is not provided. It is replaced by a regenerative feedback path. This is the open-loop configuration: if the voltage at the non-inverting input is greater than the voltage at the inverting input, the output is saturated at its most positive value. Reversing the inputs causes the circuit to slew (change) at its maximum possible rate to saturate negatively.

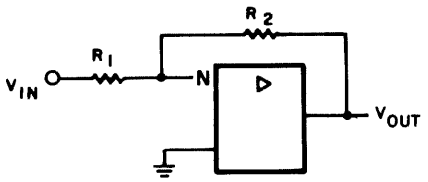
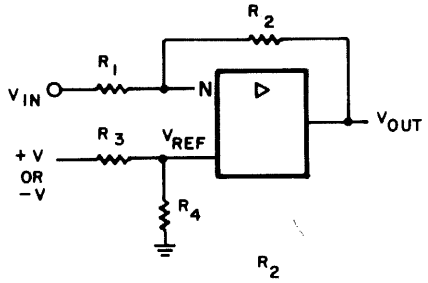
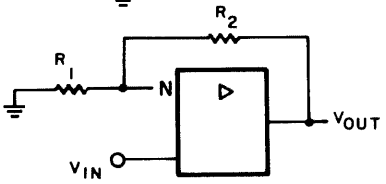
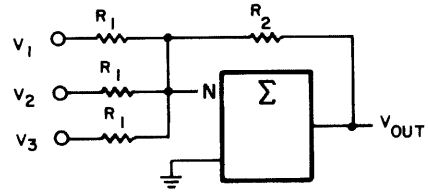
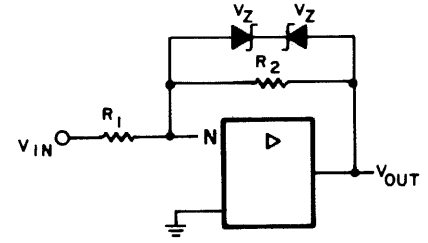
All Schmitt triggers have hysteresis. Hysteresis is supplied by regenerative feedback from the output to the non-inverting input.

Consider A376 of figure 1-20. Assume the voltage at A is zero. A voltage divider network (not shown) sets point B at +1.28 V. Without feedback and, since the non-inverting input is more positive than the inverting input, the output is saturated positively.

As the input A goes more positive, the output does not change until A equals B (+1.28 V). The differential voltage is then zero, so the output starts to switch to a zero-volt output. However, there is now a path from Y to B; the B input becomes less positive than the A input. The output very quickly saturates negatively.

With about -14 V available at Y, the voltage at B is reduced to +1.10 V. The input must now swing to less than +1.10 V for the output to change its state back to positive saturation.

The remaining circuits work in a similar manner.

CIRCUIT TYPE	SYMBOL	OUTPUT ①
INVERTING AMP		$V_{OUT} = -\frac{R_2}{R_1} V_{IN}$
INVERTING AMP WITH REFERENCE VOLTAGE		$V_{OUT} = V_{REF} + \frac{R_2 (V_{REF} - V_{IN})}{R_1}$ OBSERVE ALGEBRAIC SIGNS IF COMPUTING $V_{OUT} = 0$ IF $V_{IN} = V_{REF}$ $V_{REF} = \pm V\left(\frac{R_3}{R_3 + R_4}\right)$
NON INVERTING AMPLIFIER		$V_{OUT} = \frac{V_{IN} (R_1 + R_2)}{R_1}$
SUMMING AMPLIFIER		$V_{OUT} = -\left[\frac{R_2}{R_1} (V_1 + V_2 + V_3)\right]$
INVERTING AMPLIFIER WITH OUTPUT LIMITING		$V_{OUT} = -\frac{R_2}{R_1} V_{IN}$ IF $\pm V_{OUT} \leq V_Z$

NOTE:

① MINUS SIGN (-) INDICATES THAT OUTPUT IS INVERTED.

7J91-IA

Figure 1-19. Op Amp Circuit Functions (Sheet 1 of 3)

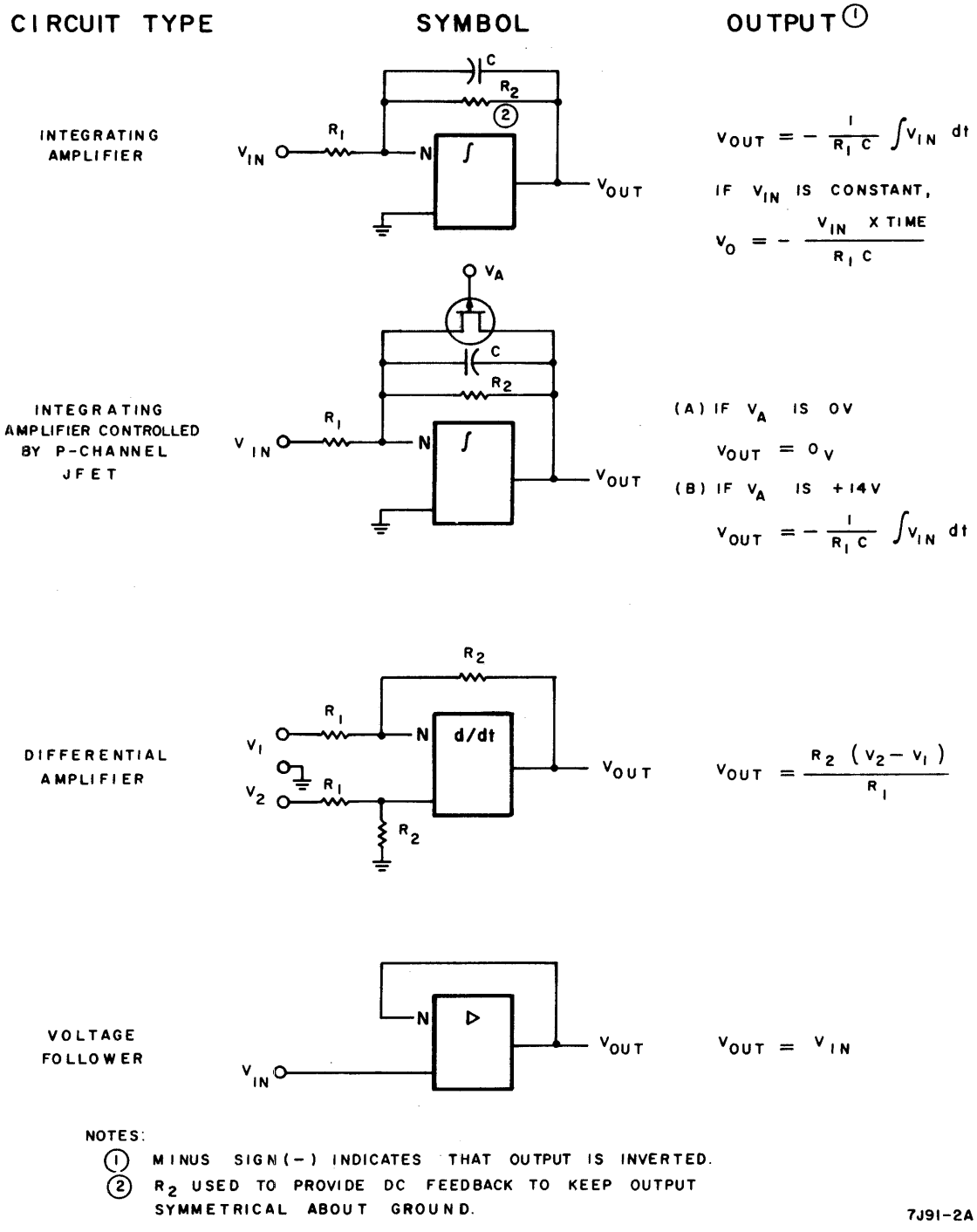
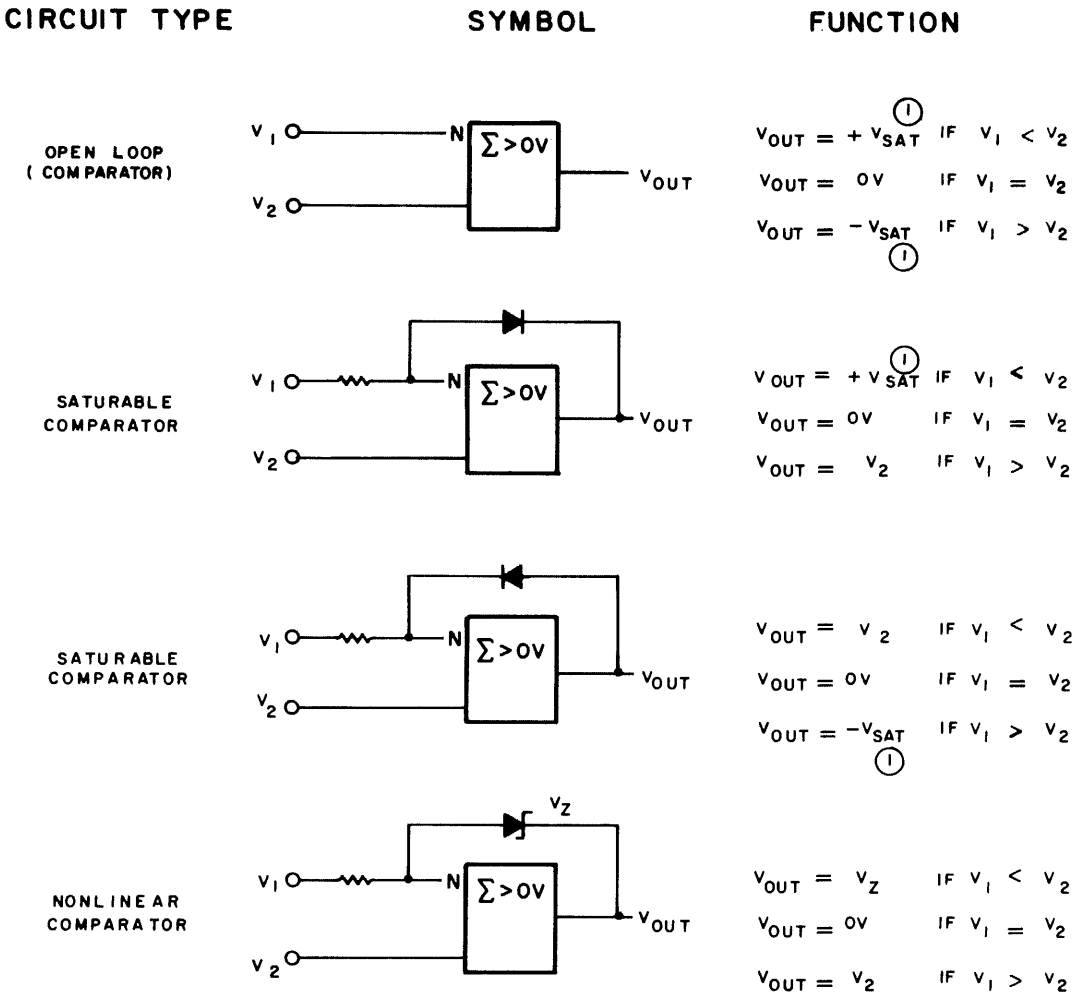


Figure 1-19. Op Amp Circuit Functions (Sheet 2 of 3)



NOTE:

(1) V_{OUT} IS ACTUALLY PRODUCT OF $|V_1| - |V_2|$ X AMPLIFIER OPEN LOOP VOLTAGE GAIN (A_V). $A_V \approx 10{,}000$. V_{OUT} CANNOT ACTUALLY EXCEED THE SATURATION VOLTAGE (V_{SAT}), WHICH IS ABOUT 2 VOLTS LESS THAN THE SUPPLY VOLTAGE.

7J91-3A

Figure 1-19. Op Amp Circuit Functions (Sheet 3 of 3)

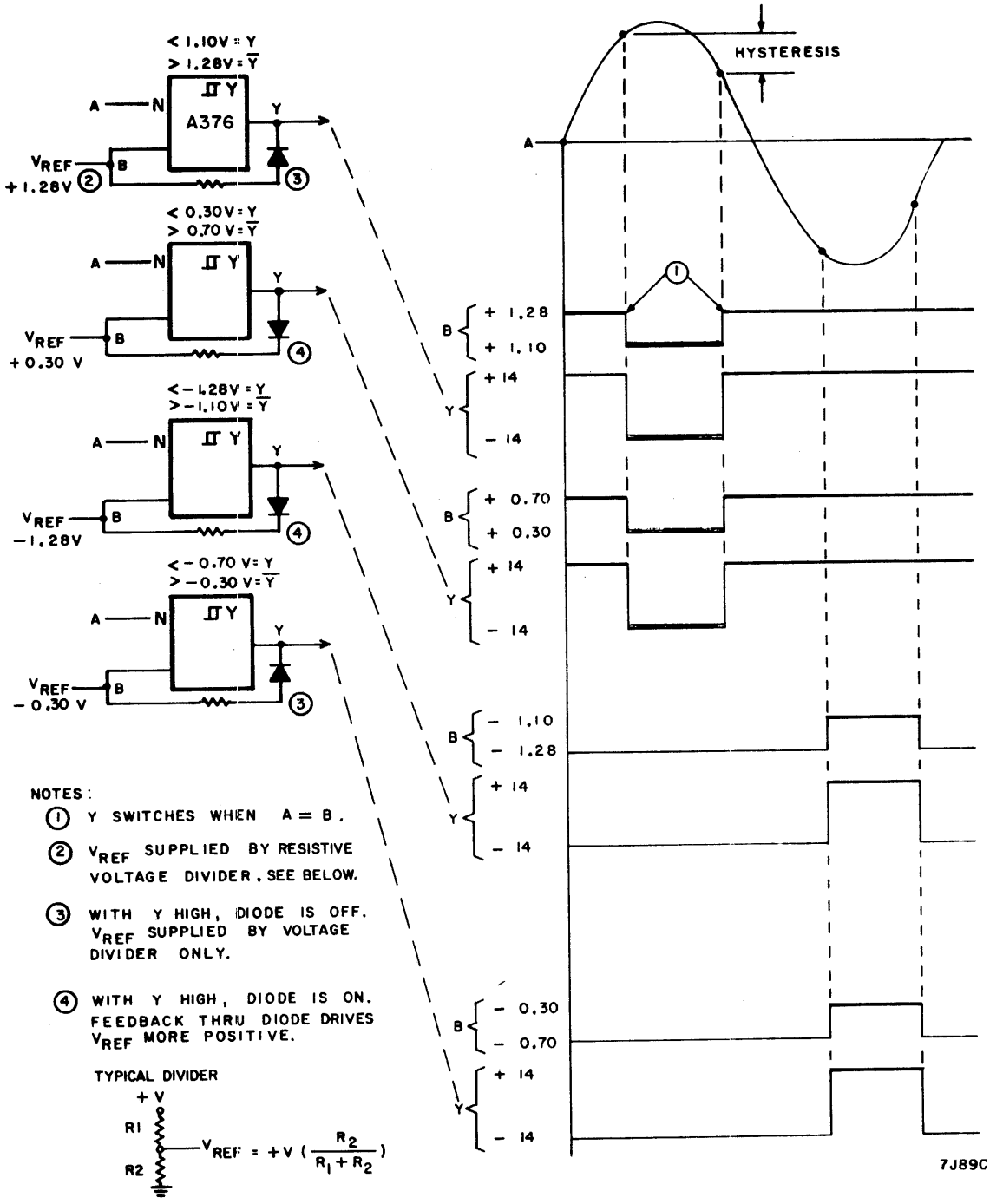


Figure 1-20. Op Amp Used as Schmitt Trigger

SECTION 2

LOGIC SYMBOLOGY

GENERAL

Logic symbols are used to portray various types of electronic circuits and are composed of the following parts:

- Symbol outline
- Qualifying symbol(s)
- Modifier(s)
- Indicator(s)
- Internal tagging information
- External pin assignments

All of these items are briefly explained in the following paragraphs.

As is shown in figure 2-1, the symbol outline merely determines the limits and shape of the logic symbol. In some cases, the outlines used to represent certain functions in a logic diagram set will differ from the standard ones shown in this manual. However, the pin numbers and meanings are the same.

The qualifying symbols shown in the figure denote basic operations being performed by the function. A 1 indicates an OR circuit, while an & indicates an AND circuit. A complete listing of the many meanings of qualifying symbols appears later in this explanation. In some cases, a functional name may replace a qualifying symbol (e.g., ALU, meaning Arithmetic Logical Unit.) The qualifying symbol appears in the neck of the common control block of certain symbol outlines, as shown.

QUALIFYING SYMBOLS

Qualifying symbols and functional names used in binary combinational logic are listed below. Combinational logic means that for each function or interconnection of binary functions at the input of a logical device, there corresponds only one binary state at its output.

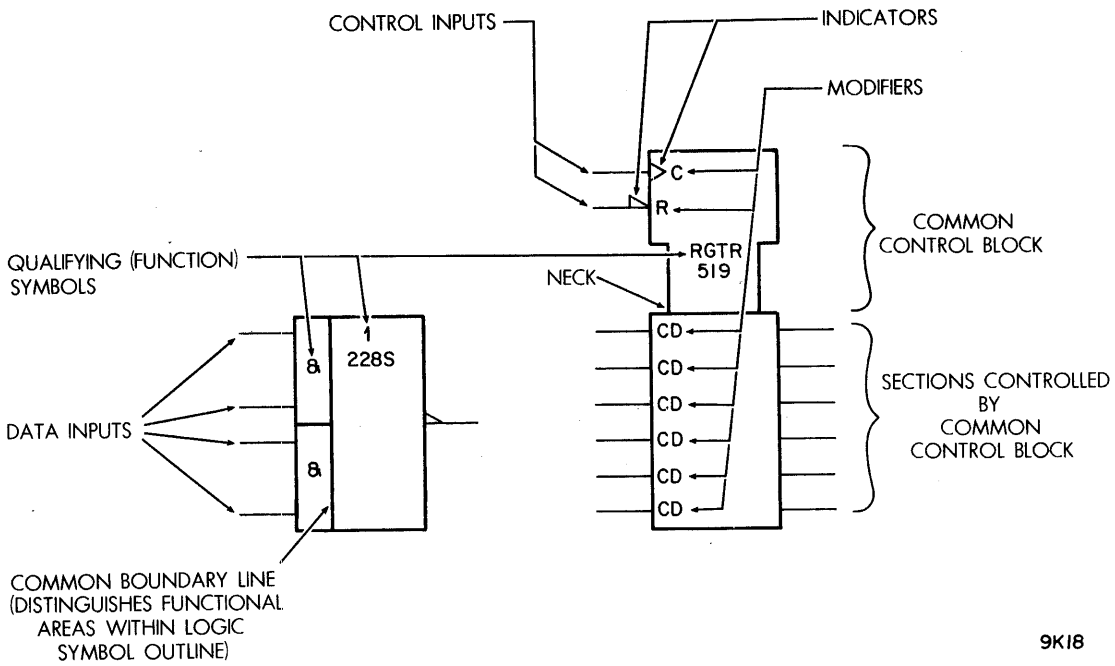


Figure 2-1. Typical Logic Symbols

COMBINATIONAL LOGIC QUALIFYING SYMBOLS

&-AND: Output of element assumes its active state if and only if (IFF) all inputs are in active states.

&-Wired AND: Same as AND gate above except ◇ that AND function is accomplished by wiring outputs together rather than by using gates involving other elements. Output of a Wired AND cannot be an input to a Wired OR.

1-OR: Output of element assumes its active state IFF one or more of its inputs assumes its active state.

1-Wired OR: Same as OR gate above except ◇ that OR function is accomplished by wiring outputs together rather than by using gates of other elements.

=1-Exclusive OR: Output assumes its active state IFF one of its two inputs becomes active.

≥m-Logic Threshold: Output assumes its active state IFF the number of inputs which assume their active states reaches or exceeds the number (m) specified in the qualifying symbol.

=m-m and only m: Output assumes its active state IFF m of its n inputs (where n > m) assume their active state.

=Logic identity: Output assumes its active state IFF all inputs assume same state.

2K+1-Odd and only odd: Output assumes its active state IFF an odd number of inputs assume their active states.

2K-Even and only even: Output assumes its active state IFF an even number of inputs assume their active states.

X/Y-Level converter: Converts binary signal of one pair of states to corresponding levels of second pair of logical states.

X→Y-Coder: Input code X converted to output code Y per weighting technique of modifiers or table. Logic sets using common control block as shown here may use the functional name CODER.

X MAX→Y-Priority Coder: An element with multiple inputs and outputs in which resultant outputs are a representation of the active input with the largest coefficient.

DEMUX-Demultiplexer: A function or array of functions in which data input is selectively routed to one of several outputs as determined by control lines.

MUX-Multiplexer: A function or array of functions in which control lines determine which one of several inputs is selectively routed to the output.

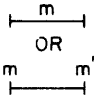
ALU-Arithmetic and Logic Unit: Performs either arithmetic or logic functions (or both) according to internal notations or by external reference data.

SEQUENTIAL LOGIC QUALIFYING SYMBOLS

Qualifying symbols and functional names designated as sequential logic qualifiers are listed and explained below. Sequential logic means that for at least one combination of states of the input(s), there exists more than one possible state of the output(s). Outputs are also affected by time and previous internal states of the element as well as the normal inputs.

 - Schmitt trigger: Output of element assumes its active state IFF its hysteresis type input exceeds its active threshold value as it changes from inactive to active state. One threshold exists for positive-going signals, and another for negative-going signals.

 - Monostable element: A one-shot monostable retriggerable multivibrator which assumes its active state if the input changes from inactive to active state. Its output remains active for time period determined by element characteristics and externally connected RC components. It may be reset at any time by an input labeled R (Reset).

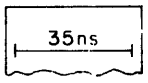


- Time delay: Output of element assumes its active state only after the period of time (m) following the transition of the input to its active state. Output reverts to inactive state only after time period (m or m' in alternate symbol) following the transition of the input to its inactive state.

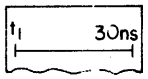
If one or both delay times are not fixed values, they are indicated by t_1 or t_2, as appropriate. Where tapped delays are used and

delay time is equal in both directions, the appropriate time period replaces m in first version of symbol and a corresponding numerical value of delay is used as an output modifier. The second version of the qualifying symbol is used IFF delays are unequal in opposite directions.

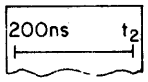
EXAMPLES:



Both zeros and ones are delayed by 35 nsec.

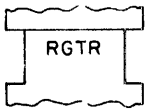


Zeros delayed by 30 nsec when input becomes a 0.

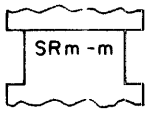


Ones delayed by 200 nsec when input becomes a 1.

(No Symbol) **Flip flop: A binary element with two stable states.** One is called set (or active) state and the other is reset (or inactive) state. Flip flops are identified by one or more of the following input signal modifiers: C,D,J,K,R,S,T.

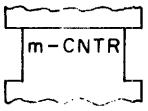


-Register: An array of flip flops having common input connections, such as reset, clock, or other gating functions.

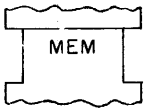


-Shift Register: m arrays of flip flops, each containing m' bits. The SR has at least one input used for transferring information in a specified direction from one bit position to another. The direction of shifting and number of bit positions shifted is indicated by input modifier which activates the shifting. IFF the shift register is dynamic, the qualifying symbol (▷ SRm-m') is used.

⟶ - Shift Register: An array of flip flops comprised of m bits similar to other SR, but with only serial input and output.



- Counter: An array of flip flops in which the states represent a number that may be increased or decreased by inputs designated by +m or -m. The counter modulus is indicated by the number used to replace m.



- Memory: An addressable array of flip flops in which input(s) and output(s) are multiplexed to and from bit positions. The number of addresses at which bits are located is indicated by address (A) modifier suffixes in common control block. Number of bits at each address is indicated by number of flip flops abutted vertically to common control block.

ANALOG QUALIFYING SYMBOLS AND FUNCTIONAL NAMES

▷m - Amplifier: A single input amplifier having a gain of m. Inversion of the signal is indicated by an N at the appropriate input or output(s).

∑▷m - Summing or Differential Amplifier: The basics of single input amplifiers apply, but with additional provision for multiple inputs. Output is algebraic sum of weighted values of inputs, times the gain factor m. Weighting values are implied to be unity if omitted from symbol.

∫▷m - Integrating Amplifier: An amplifier whose output is proportionate to the integral parts of the input signal times the gain factor m.

>m or ∑<m' - Threshold or Comparator: A circuit with one analog input that provides an output proportional to the amount the input passes a predetermined threshold (applies to analog circuits).

For comparator circuits, the binary output remains inactive until the input either exceeds or becomes less than a predetermined value.

In the symbol, m is replaced by the applicable value and units of measurement.

Threshold circuits and comparators are differentiated from each other by indicators or modifiers at their outputs. Directly to the right of the symbol outline, the threshold circuit (analog output) may have an N or ∩ indicator while the comparator (binary output) may have either a # or indicator. If the output connects to another input across a common boundary line, the threshold circuit output is indicated by an N or P; the comparator output by a polarity (◺) indicator,

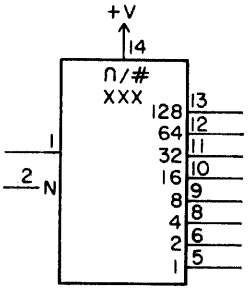
or by a modifier such as G,R, or S, or by a - (minus) across the common boundary line.

NOTE

N is never used with single-input threshold or comparator circuits.

|Π|>m
|Σ|>m - Rectifying Threshold Circuit: Analog output is proportional to the amount the rectified input exceeds the predetermined value,m.

Π/# - Analog to Digital Converter: Summation of the weighting factors of the active binary outputs is a representation of the analog inputs. The minimum value of analog input that corresponds to all weighted outputs inactive, and the maximum value of analog input that corresponds to all weighted outputs active, is indicated next to the symbol. For example:



ALL HI=+9.96V

If pin 1=+9.96V relative to pin 2, all outputs will be HI. If pins 1 and 2 same voltage, all outputs will be LO.

#/Π - Digital to Analog Converter: Analog output is a representation of the summation of the weighting factors of the active binary inputs. A voltage value is stated next to symbol as it is for A/D converter previously explained.

λ/# - Optical to Digital Converter: The binary output is active for analog or binary light inputs greater than stated threshold value. The binary output is inactive for inputs less than threshold. The output is indeterminate for light input values within the defined threshold tolerance of the element.

#/λ - Digital to Optical Converter: The optical output has the highest light intensity for an active binary input and the lowest intensity for an inactive binary input.

λ/Π - Optical to Analog Converter: The analog output (No N indicator) is more positive in proportion to increasing analog light inputs, and conversely more negative for decreasing light inputs.

Π/λ - Analog to Optical Converter: The optical output has an increasing light intensity in proportion to the analog input (No N indicator) becoming more positive and a decreasing light intensity in proportion to the analog input becoming more negative.

mVR
mAR - Regulator or Reference: The output provides a regulated or reference value of m amperes or m volts including the effect of external components.

V/V
m - Voltage to Voltage Converter: Output voltage is isolated from power supply connections at top or bottom of symbol outline. A value is substituted for m.

m
⊢——⊣ - Delay element: An analog function similar to that used in Sequential Logic except that the delayed output is not usable for unequal delays in both positive and negative directions, but must allow for continuous analog values (not just binary states). A value or a time unit such as ns replaces the time delay period, m.

>——< - Bilateral Switch: A binary-controlled switch which passes or blocks analog or binary signals in either direction. It passes signals if the affecting inputs are active and does not amplify.

F▷m - Amplifier: An amplifier with special transfer functions. Mathematical symbols are preferred as a replacement for F. Appropriate values are used to replace m. Some typical functions for F are:

SIN	Sine
COS	Cosine
d/dt	differentiation
$\int$	integration
Π^m	exponential power
LN	Log natural
LOG_{10}	Logarithm to base 10
×	multiply

÷ divide

m m' band pass

m m' band reject

m/m' positive & negative clamping function

m/m' bidirectional threshold circuit

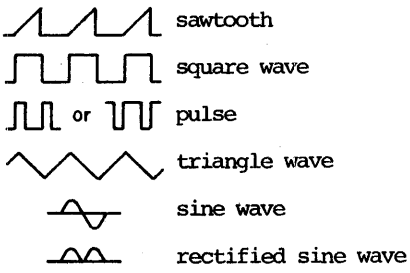
m resonant circuit

m notch filter

GENERATOR QUALIFYING SYMBOLS

The following symbols apply to both binary logic or analog functions.

G
m
m' - Generator: A cyclic or static signal source as indicated by m. The m is replaced by an appropriate graphical signal or static value generated. The m' is replaced by the frequency, such as 6 kHz. Some typical graphics for m are:



!G! - Generator: A synchronously started and stopped generator.

OTHER QUALIFYING SYMBOLS

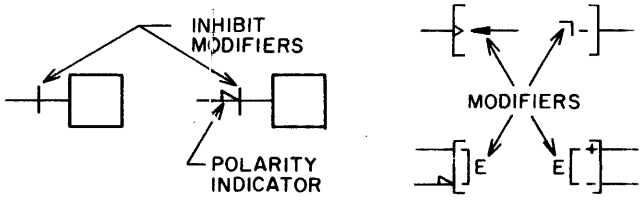
/m
m/
/m/ - Variable Parameter Function: A parameter of the basic function, m, is variable.

m*
m**
F - Incomplete Symbol: A symbol requiring additional information to interpret, but with similarity to any symbol m shown.

MODIFIERS

Modifiers are identifiers used to describe any special relation of an input or output to other input(s) or output(s) and/or to the qualifying symbol. They pertain to the virtual inputs or outputs as contrasted to indicators which pertain to the real or measurable inputs or outputs.

All modifiers (except the inhibit) are placed inside the symbol outline. The inhibit modifier is placed outside the symbol (see below).



BASIC MODIFIERS

Unless otherwise noted, the basic modifiers described in the following paragraphs are active, IFF:

1. Their input is active and the necessary A,C,F, and G affecting inputs prefixing the modifier are also active according to dependency notation, or,

2. One or more of the V (OR) relationship affecting inputs prefixing the modifier are active.

D - Data: Analog or binary input clocked in by a control (C) input.

E - Extender: Input or output used to expand the inputs of one element with outputs of another.

I - Initial Conditions: An analog initial conditions input which is always gated by a control (C) input, and whose analog value causes the sequential analog function to take on a proportionate analog value.

S - Set Input: A binary input that causes a sequential analog or binary element (such as a flip flop) to assume its set condition.

T - Toggle Input: A binary input that causes a flip flop or other sequential binary function to change its state each time the T input assumes its active state.

R - Reset Input: A binary input that causes a sequential analog or binary element (such as a flip flop) to assume its reset condition.

J - Input: A binary input analagous to the S input, but modified such that if both J and K inputs assume their active states simultaneously, the flip flop changes to the opposite state.

K - Input: A binary input analagous to the R input, affecting a flip flop in the same way as a J input.

÷ - Divisor Input: An analog divisor input for use with a function that includes analog division.

↗ - Parameter Input: An analog input which controls a variable characteristic of the function as denoted by the qualifying symbol or by tagging.

+m, -m - Increment or Decrement Input: A binary input that causes the states of flip flops serving as a counter to change the binary number by +m or -m each time the +m or -m input is active.

→ m, ← m - Shift Down (Right) or Shift Up (Left) Input: A binary input that causes the flip flops forming a shift register to shift m positions down (or right) or up (or left) each time the appropriate input is active.

⊣ - Inhibit Input: A binary input used to block the active state outputs of a non-sequential binary function.

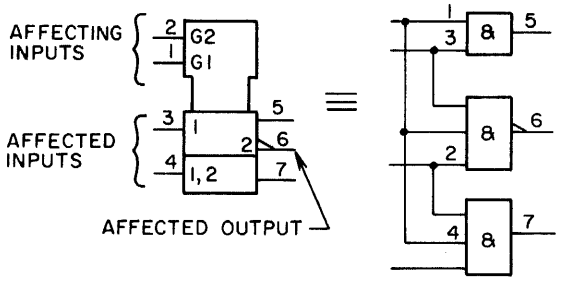
m ⌐ - Output Delay: A binary output which changes state only after the referenced input (m) returns to its inactive state (whether HI or LO).

Øm - Phase Relationship: A binary output which is active according to the phase relationship denoted by m.

(m) - Coincident Input or Output: A restrictive modifier that is not associated with any input or output, but restricts the number of inputs or outputs which may be active simultaneously.

DEPENDENCY MODIFIERS

Dependency notation is a means for obtaining simplified symbols to represent complex elements by denoting the relationships between inputs, or between inputs and outputs, without showing all elements or interconnections. The input or output that is dependent upon another input is called the affected input or output, and the input on which it depends is called the affecting input. An affecting input has an effect only on those inputs or outputs which relate to it according to the notations discussed in the following paragraphs.



A - Address: A binary affecting input, or affected input(s) and output(s) used as data ports of addressable memories.

C - Control (Clock): A binary affecting input or affected input(s) used where more than a simple AND relationship is implied to those inputs or outputs labeled with the same identifier. Also, it is used as a data gate as contrasted to an active state gate (See G).

G - Gate or AND: A binary affecting input having an AND relationship to the active state. Two affecting inputs labeled G but having different identifier suffixes stand in no relation to each other. IFF they have the same identifying character, they stand in an OR relationship.

NOTE

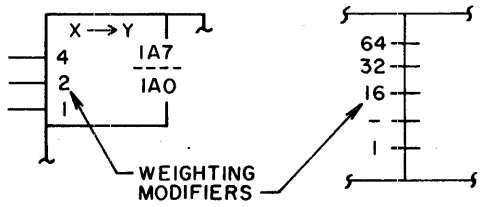
When inputs are affected by both G and C modifiers (e.g., data -- or D -- input), the AND relationship is between G and the active state of the input signal. G does not affect control (C modifier) inputs.

V - OR: A binary affecting input having an OR relationship to those inputs or outputs which are labeled with the same identifier. Two inputs labeled V having different identifying characters stand in no relation to each other.

F - Free: A binary affecting input, or affected analog or binary inputs or outputs, acting as a connect switch when active or a disconnect when inactive.

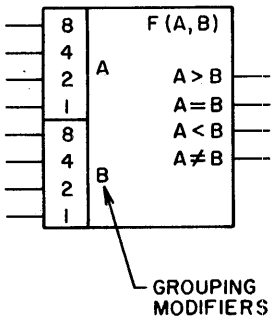
WEIGHTING MODIFIERS

Weighting modifiers show the relative coefficients applicable to various inputs and/or outputs. For example:



GROUPING MODIFIERS

Grouping modifiers are used to designate a group of two or more inputs or two or more outputs to simplify reference to that group of inputs or outputs. For example:



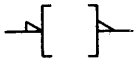
INDICATORS

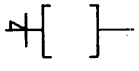
An indicator is a symbol used to specify physical values and/or properties of an input or output connection. Explanations of various groups of indicators follow:

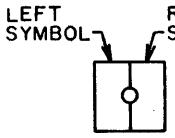
BINARY INDICATORS

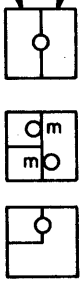
All binary inputs or outputs have active state indicators (implicit or explicit) to specify the active state relative to the logic function.

 - Implied Indicator: The absence of the polarity indicator (▷) implies a static logical HI.

 - Polarity Indicator: Indicates the active state is a static LO.

 - Inhibit/Polarity Indicator: Same as polarity indicator above, except signal is blocked when a static LO.

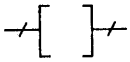


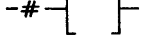


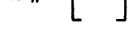
- Negating Indicator (internal connections only): Used to indicate a negating type of internal connection. The bubble indicates the inactive state output of the left symbol will provide an active state input for the right symbol. The m in the second symbol represents a modifier.

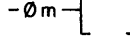
 - Dynamic Active State: The triangle represents the transition from the inactive to active static state of the input (not merely the presence of the active static state).

SUPPLEMENTARY BINARY INDICATORS

 - Non-Standard Logic Level: Slash mark used on signal lines (input and/or output) to indicate binary levels that differ from those defined as standard.

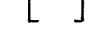
 - Binary Logic: This indicator differentiates binary from analog logic levels.

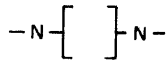
 - Serial Binary Bit: This indicator denotes a line carrying m bits of binary information in serial form. The m is replaced by the number of bits in each repetitive pattern.

 - Phase Line: This indicator denotes a line carrying a phase reference signal that must be differentiated from other binary or analog signals. The m is replaced with the appropriate character.

 Grouping Bracket: This indicator represents two or more grouped lines (such as a differential pair) carrying only one bit of binary information and represents a single input.

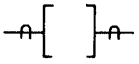
ANALOG INDICATORS

 Implied Indicator: The absence of the N indicator implies a non-inverting input relative to other inputs or outputs.



Sign Indicator: Indicates an inverting input or output.

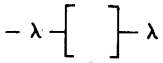
Internal Sign Indicator: This indicator is similar to the polarity indicator used in binary circuits. Here N means inversion, and P means non-inversion.



Analog Signal: This indicator is used to differentiate analog signals from binary (#).

SUPPLEMENTARY ANALOG AND BINARY INDICATORS

Wired Connection: This indicator represents an analog or binary line that enters a wired function when necessary to distinguish that its value or state may be affected by one or more outputs elsewhere.



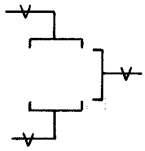
Optical Signal Path: This indicator shows that a path of light is the conductor rather than an electrical wire.

LO Output Only: The minus sign denotes that an element's output is capable of supplying LOs only (binary) or negative-going drive signals (analog).

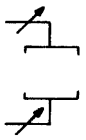
HI Output Only: The plus sign denotes that an element's output is capable of supplying HIs only (binary) or positive-going drive signals (analog).

Implied HI-LO Output: The absence of plus or minus indicates the element is capable of supplying HIs or LOs or positive or negative-going drive signals.

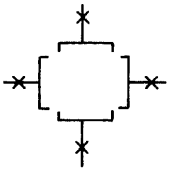
MISCELLANEOUS INDICATORS



Voltage Indicator: Denotes that this line carries a power supply or reference voltage when necessary to differentiate it from binary or analog signals.



Parameter Control: This indicator denotes a line used for varying the characteristic(s) of an analog or binary function indicated by a qualifying symbol.

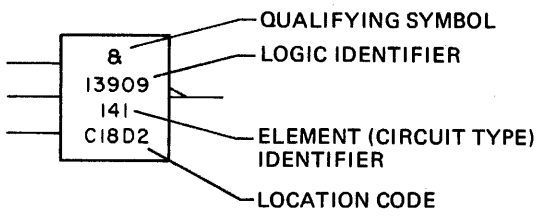


Non-Binary and Non-Analog Indicator: Denotes that the line so marked does not carry binary or analog information (when necessary to distinguish it from other lines, and no other indicators apply).

INTERNAL TAGGING

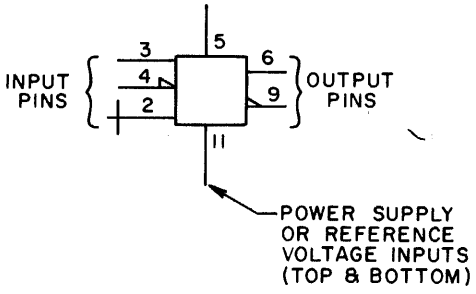
Internal tagging information, as applicable, is placed on successive lines within the symbol outline in the following order:

1. Qualifying symbol representing a function (when used). Circuits such as flip flops do not have a qualifying symbol.
2. Logic identifier such as I3909, K3900, etc. (Optional.)
3. Element (circuit type) identifier.
4. Physical location code.



In symbols having a common control block, tagging information is placed in the neck of the symbol, as shown in Figure 2-1.

EXTERNAL PIN ASSIGNMENTS



SECTION 3

DATA SHEETS

INTRODUCTION

This section contains two cream-colored divider sheets, separating the information into three subsections:

1. Introductory remarks
2. Data sheets arranged by CDC element identifier
3. Data sheets arranged by vendor reference number.

Subsection 2 is arranged numerically by CDC element identifier. This identifier also appears as a page number at the bottom of the data sheet. Speed variations (H,L,LS, S, etc.) are shown on the same page as the basic circuit. When an element requires more than one data-sheet page, the page identifer is followed by a dash number. For example, 141 indicates a single data sheet, but 941-4 indicates the fourth page of the data sheet for the 941 microcircuit.

Subsection 3 contains information on microcircuits for which no CDC element identifiers presently exist. The data sheets in this subsection are arranged numerically first, and alphabetically second. Thus, 74H51 precedes 74173, but both appear before the alphanumeric identifiers such as IM6503, MC426, SG82, and so on. The "dash number" scheme is also used here to show multiple sheets.

DATA SHEET INTERPRETATION

All of the data sheets in this section contain the following kinds of information:

1. LOGIC SYMBOL - The ANSI/CDC symbol for the high-active version of the microcircuit and, where applicable, the alternate low-active version. Pin numbers are included as part of the symbol. Special notations to clarify the various input and output functions are added when helpful, but are not to be construed as part of the symbol.
2. DESCRIPTION - An explanation of the function or functions performed by the microcircuit.
3. NOTES - Helpful information, such as:
   - Vendor reference number
   - Package pin configuration. Defines pins used for external voltage sources (V_{CC}, V_{EE}, GND, etc.) and keys, slots or marks used to orient the microcircuit.

In addition, the following information is included on individual data sheets, when applicable:

4. FUNCTIONAL DIAGRAM - Basic logic symbols (NAND, NOR, FF, etc.) arranged to show the internal logic of the microcircuit.
5. TRUTH TABLE - A table showing the state(s) of the microcircuit's output for varying input conditions.
6. TIMING DIAGRAM - Used to clarify complex timing relationships between inputs and outputs.

DATA SHEET LIST

The list on the following pages shows the order in which the data sheets appear, and also provides a quick reference to the family (TTL, ECL, CMOS) to which a particular microcircuit belongs. If a circuit requires more than one data sheet, the number of sheets is given in parentheses.

TTL

139
140
141
142 (2)
143
144
145
146
147
148
149

158 (3)
159 (3)

161
162 (2)
163
164 (2)
166 (2)
167 (2)

170 (2)
172
173
175
176

180
182 (2)
188
189

191 (2)
193
195

200
201
202
203
205
206
207
208
209

210
212
213
216 (2)
218

220
222
223
224
225
226
228
229
230

242 (2)
243

OP AMPS

300
301
302
304
306
307
308
309

310
313
315
316
318

320 (2)
321
322
324
326
327 (2)
329

330
331
332/353
333
334 (2)
338 (2)
339

340
341

356
357

386

TTL

500 (3)
501 (2)
502
505 (2)
506 (3)
507 (2)
508 (2)
509 (2)

510 (2)
512 (3)
514
515 (2)
519 (2)

520 (2)
521
522
524 (2)
525 (3)
527 (2)
528 (3)
529
530
531 (2)
532 (2)
537
538
539 (2)

542 (2)
543 (3)

550 (2)
551
554 (2)
559

563 (3)
568

571 (3)
572
579

581
582

768

774
775 (2)
779

TTL

902
905
909

910
911
912
915
916 (3)

921
922
923
926
927

930
939

949

986 (2)

ARRAYS

3046
3096

CMOS

4001
4011
4016
4017 (2)
4023
4027
4049

ECL

5100/5200/
5300/5400 (9)
5600/7500 (3)

10101
10102
10104
10105
10106
10107
10109
10114
10116
10117
10124
10125
10131
10141 (3)
12040 (2)
50255700 (2)

MISCELLANEOUS

74H51
74153
74LS221

IM 5603

MC 426 (2)
MC 1648

SNG 82 } see MC 426
SNG 83 }

DATA SHEETS

ARRANGED BY

CDC ELEMENT IDENTIFIER NO.

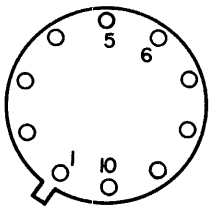
DESCRIPTION

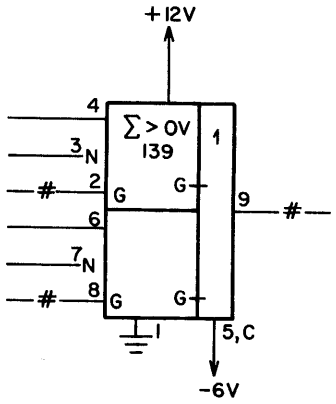
The 139 circuit consists of two high-gain voltage comparators with separate differential inputs and a common output. Individual strobes (G) allow independent gating of the inputs to each section.

The circuit has a voltage gain of 500.

NOTES:

1. Vendor identification: 711C
2. Package pin configuration:





(# IDENTIFIES BINARY LOGIC SIGNAL)

LOGIC SYMBOL

139
Rev A
Sheet 1 of 1

DESCRIPTION

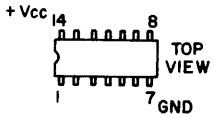
The 140 circuit is a four-section (quad), 2-input, positive NAND gate.

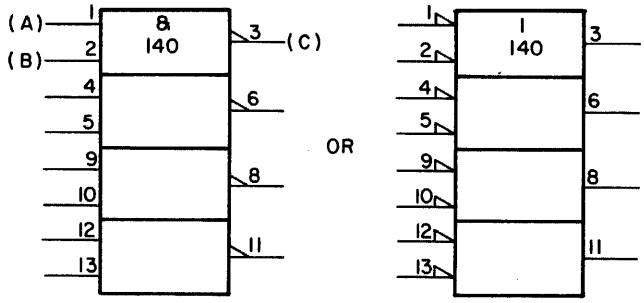
NOTES:

1. Symbol Sections may appear separately.
2. Vendor identification:

Element	Vendor Number
140	7400,9002
140H	74H00
140L	74L00
140LS	74LS00
140S	74S00

3. Package pin configuration.



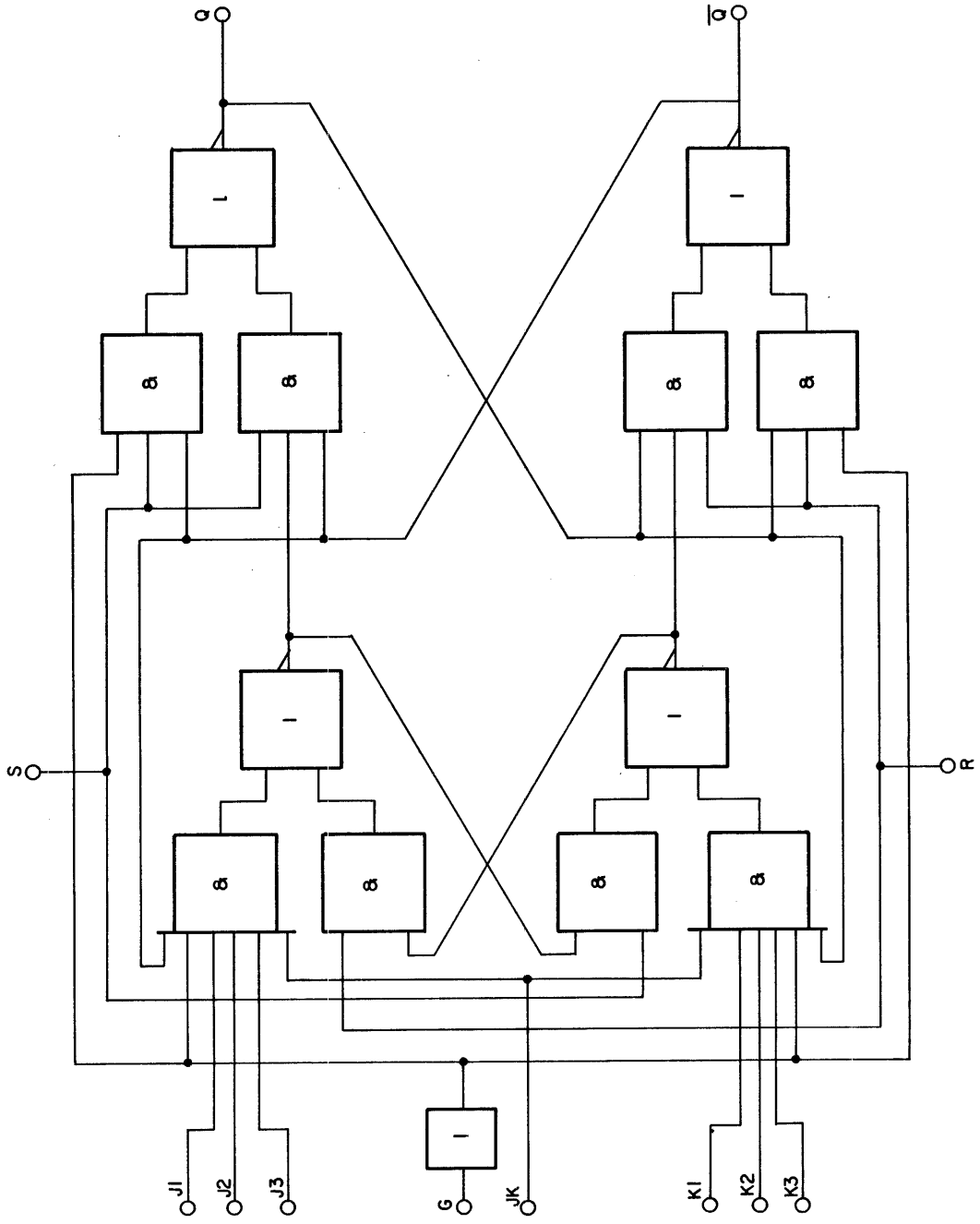


LOGIC SYMBOL

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

TRUTH TABLE
(FOR ONE GATE)

140
Rev D
Sheet 1 of 1



FUNCTION DIAGRAM

142
Rev B
Sheet 2 of 2

DESCRIPTION

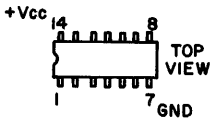
The 141 circuit is a three-section, 3-input, positive NAND gate.

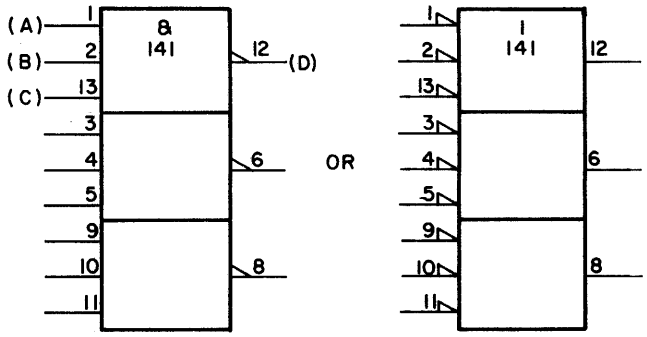
NOTES:

1. Symbol Sections may appear separately.
2. Vendor identification:

Element	Vendor Number
141	7410,9003
141H	74H10
141L	74L10
141LS	74LS10
141S	74S10

3. Package pin configuration.





LOGIC SYMBOL

A	B	C	D
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

TRUTH TABLE

141
Rev C
Sheet 1 of 1

DESCRIPTION

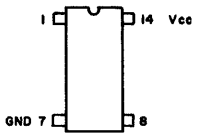
The 142 circuit is a J-K master-slave flip-flop with asynchronous set (S) and clear (R) inputs. Input J-K is common to both the J- and the K- input AND networks, and may be used as a gating input.

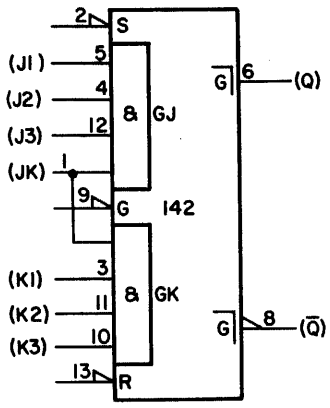
Information is received by the master while the clock (G) is low, and transferred to the slave section on the leading edge (negative-to-positive transition) of the clock pulse. On the trailing edge of the clock pulse, information is transferred to the outputs.

Bringing S or R low will cause the FF to set or clear, respectively. Conflicting synchronous inputs may cause spikes at the output during the preset-preclear operation, but these will disappear with the clock pulse.

NOTES:

1. Vendor identification: 74104/9000
2. Package pin configuration:





LOGIC SYMBOL

INPUTS AT tn			OUTPUTS AT tn+1	
JK	J *	K *	Q	$\overline{Q}$
L †	X	X	Qn	$\overline{Qn}$
H	L †	L †	Qn	$\overline{Q}$
H	L	H	L	H
H	H	L	H	L
H	H	H	$\overline{Qn}$	Qn

* J = J1 J2 J3
K = K1 K2 K3

† THESE LOW LEVELS MUST BE MAINTAINED WHILE THE CLOCK IS LOW

tn BIT TIME BEFORE CLOCK PULSE

tn+1 BIT TIME AFTER CLOCK PULSE

TRUTH TABLE

142
Rev A
Sheet 1 of 2

DESCRIPTION

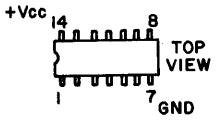
The 143 circuit is a two-section, 4-input, positive NAND gate.

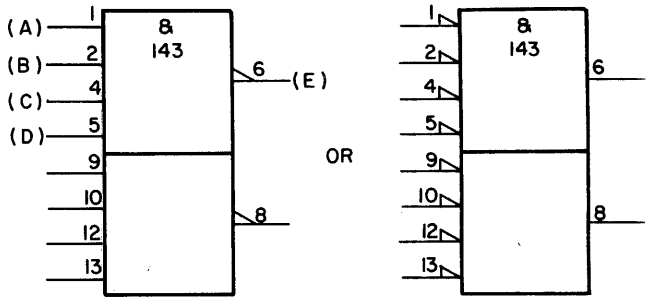
NOTES:

1. Symbol Sections may appear separately.
2. Vendor identification:

Element	Vendor Number
143	7440,9009
143H	74H40
143S	74S40

3. Package pin configuration.





LOGIC SYMBOL

A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

TRUTH TABLE
(FOR ONE GATE)

143
Rev C
Sheet 1 of 1

DESCRIPTION

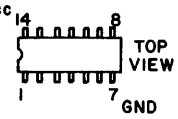
The 144 circuit is a positive-edge-triggered JK flip-flop with separate (asynchronous) set and clear inputs. The asynchronous inputs control the state of the flip-flop independent of static conditions of the clock and synchronous inputs. With pin 13 or pin 2 LOW one output will be high, but if opposing data is present at the synchronous inputs and the flip-flop is clocked, the low output may momentarily spike HIGH synchronous with a positive transition of the clock. A low level to the set input (pin 2) will set pin 6 to high level regardless of the level at the clock (pin 9) input. A low level to the reset (pin 13) input will clear pin 6 to low level regardless of the level of the clock input.

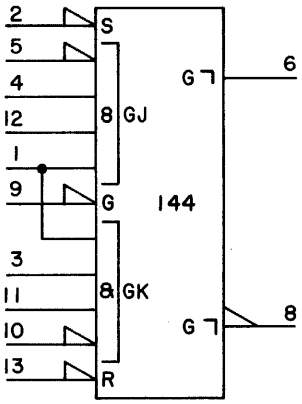
Data is accepted by the master while the clock is in the low state. Transfer from the master to the slave occurs on the LOW to HIGH transition of the clock. When the clock is HIGH, the J and K inputs are inhibited.

NOTES:

1. Vendor identification:
   74105
   9001

2. Package pin configuration.





GJ-J OUTPUT CONDITIONED BY LEADING EDGE OF DYNAMIC TOGGLE(G)

GK-K OUTPUT CONDITIONED BY LEADING EDGE OF DYNAMIC TOGGLE(G)

G-GATE INPUT, HAS NO DIRECT EFFECT ON CIRCUIT, BUT MUST PRESENT BEFORE SIGNALS PRESENT ON INPUT(S) CAN BE TRANSFERRED TO OUTPUT(S)

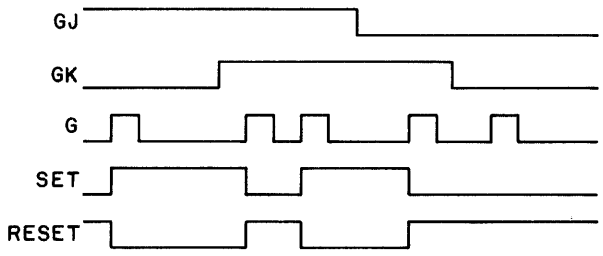
S-SET INPUT, WHEN "0", FF IS SET REGARDLESS OF INPUTS AND GATE STATES

R-RESET (CLEAR) INPUT, WHEN "0", FF IS CLEARED REGARDLESS OF INPUTS AND GATE STATES

LOGIC SYMBOL

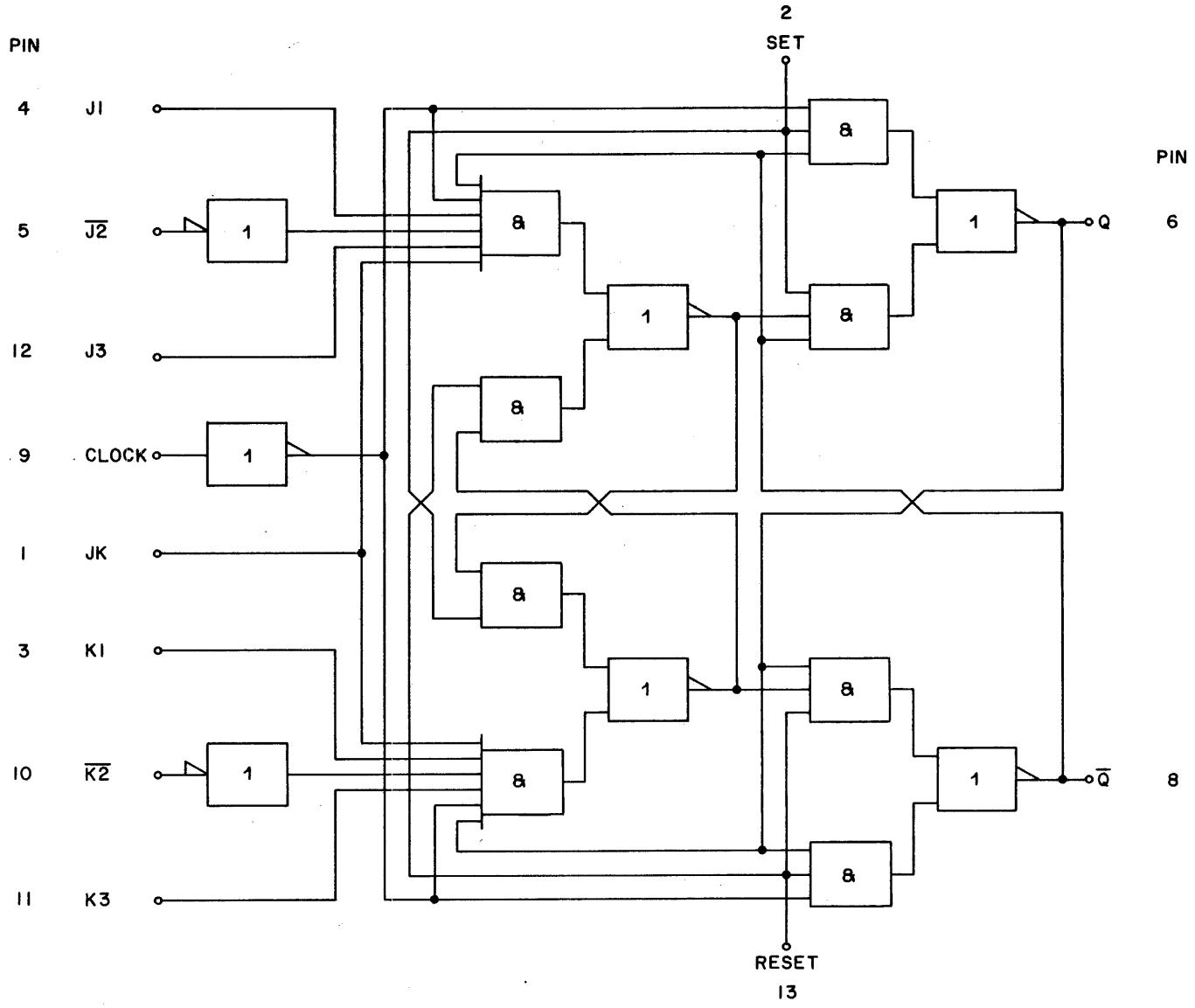
INPUTS		OUTPUTS BEFORE TOGGLE		OUTPUTS AFTER TOGGLE	
GJ	GK	SET	RESET	SET	RESET
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

TRUTH TABLE



TIMING SEQUENCE

144
Rev B
Sheet 1 of 2



FUNCTION DIAGRAM

144
Rev C
Sheet 2 of 2

DESCRIPTION

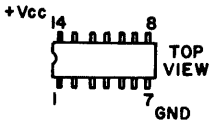
Circuit 145 is a dual, expandable AND-OR-INVERT gate. Section B of this circuit is expandable. If not expanded pins 11 and 12 are open.

NOTES:

1. If not used, expander pins may not be shown.
2. Vendor identification:

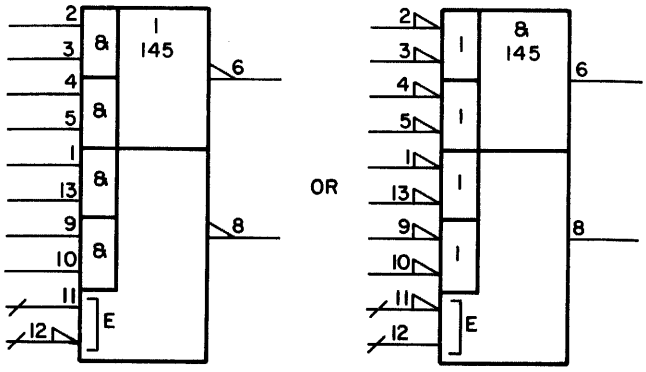
Element	Vendor Number
145	9005
145H	74H50

3. Package pin configuration.

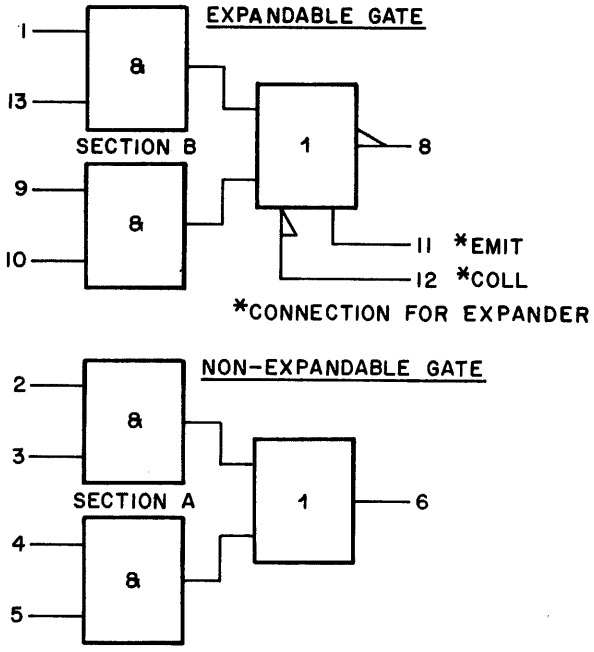


A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

TRUTH TABLE



LOGIC SYMBOL



PIN ASSIGNMENTS

145
Rev B
Sheet 1 of 1

DESCRIPTION

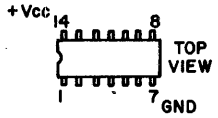
The 146 circuit is a six-section (hex) inverter.

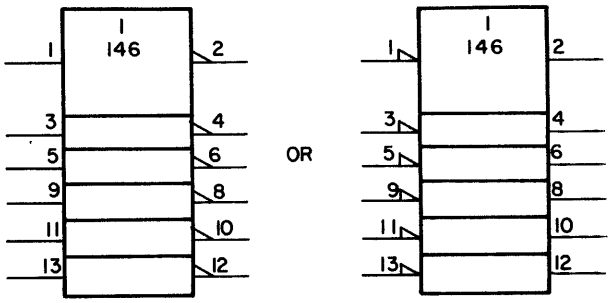
NOTES:

1. Symbol Sections may appear separately.
2. Vendor identification:

Element	Vendor Number
146	7404,9016
146H	74H04
146L	74L04
146LS	74LS04
146S	74S04

3. Package pin configuration.





LOGIC SYMBOL

146
Rev C
Sheet 1 of 1

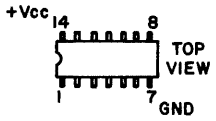
DESCRIPTION

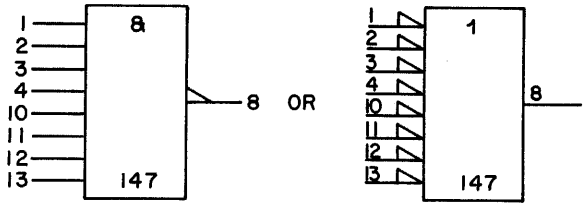
The 147 circuit is an 8-input, positive NAND gate.

NOTES:

1. Vendor identification: 9007

2. Package pin configuration.





LOGIC SYMBOL

147
Rev C
Sheet 1 of 1

DESCRIPTION

Element 148 is a quad, 2-input, positive NOR gate.

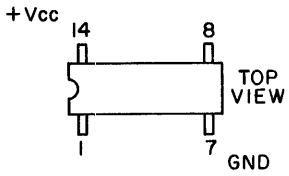
NOTES:

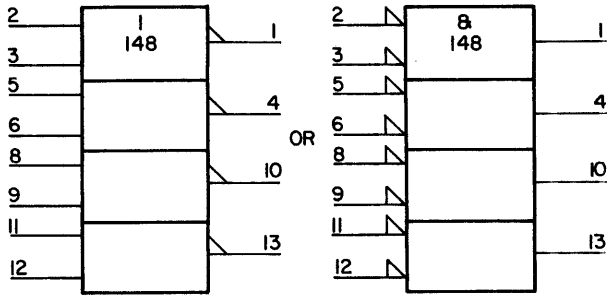
1. Symbols may appear separately.

2. Vendor identification:

Element	Vendor Number
148	7402
148L	74L02
148LS	74LS02
148S	74S02

3. Package pin configuration.





LOGIC SYMBOL

148
Rev C
Sheet 1 of 1

DESCRIPTION

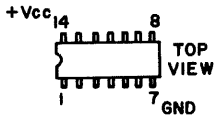
The 149 circuit is a quad 2-input Exclusive OR gate that performs the function $Y=A\overline{B} + \overline{A}B$. When the input states are complementary, the output goes to the high level.

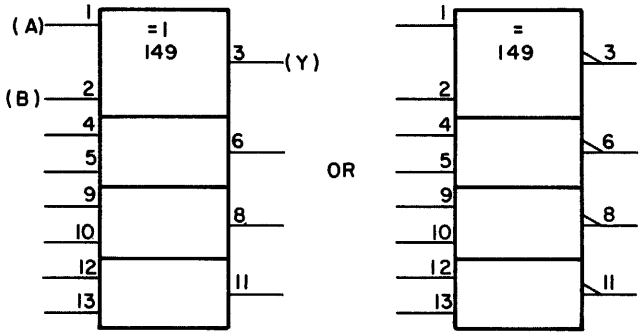
NOTES:

1. Symbol Sections may appear separately.
2. Vendor identification:

Element	Vendor Number
149	7486
149H	3021
149LS	74LS86
149S	74S86

3. Package pin configuration.





LOGIC SYMBOL

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

TRUTH TABLE

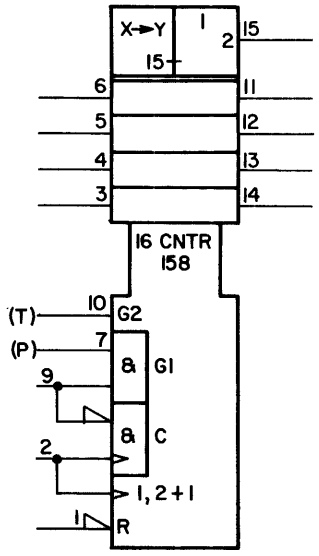
149
Rev C
Sheet 1 of 1

DESCRIPTION

The 158 circuit is a 4-bit synchronous binary counter. This circuit can be preloaded with data at the data inputs when the load input is low. This disables the counter and enables the data inputs. Input data will be transferred to the outputs the next time the clock input has a low to high transition.

In order for the counter to count, the load (pin 9), clear (R), and P and T enable inputs must be high. A low level to the clear input will clear the outputs to low level regardless of the level to any other input.

When P is low, the clock input is disabled so that the counter can not count. When T is low, the clock input and carry output are both disabled.



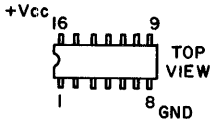
LOGIC SYMBOL

NOTES:

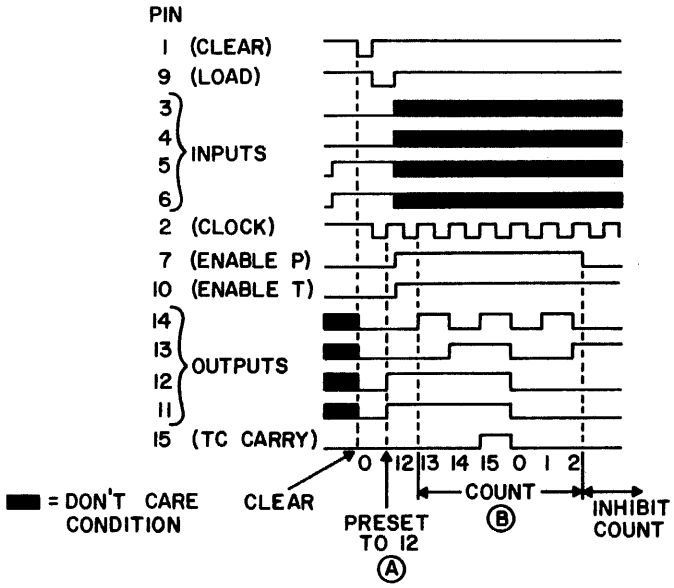
1. Vendor identification:

Element	Vendor Number
158	74161,9316
158A	74161
158LS	74LS161

2. Package pin configuration.



158
Rev C
Sheet 1 of 3



NOTES:

Ⓐ MODE SELECTION WITH POSITIVE-GOING CLOCK IS:

PINS 7 & 10	PIN 9	MODE
1	1	COUNT UP
0	1	NO CHANGE
1	0	PRESET
0	0	PRESET

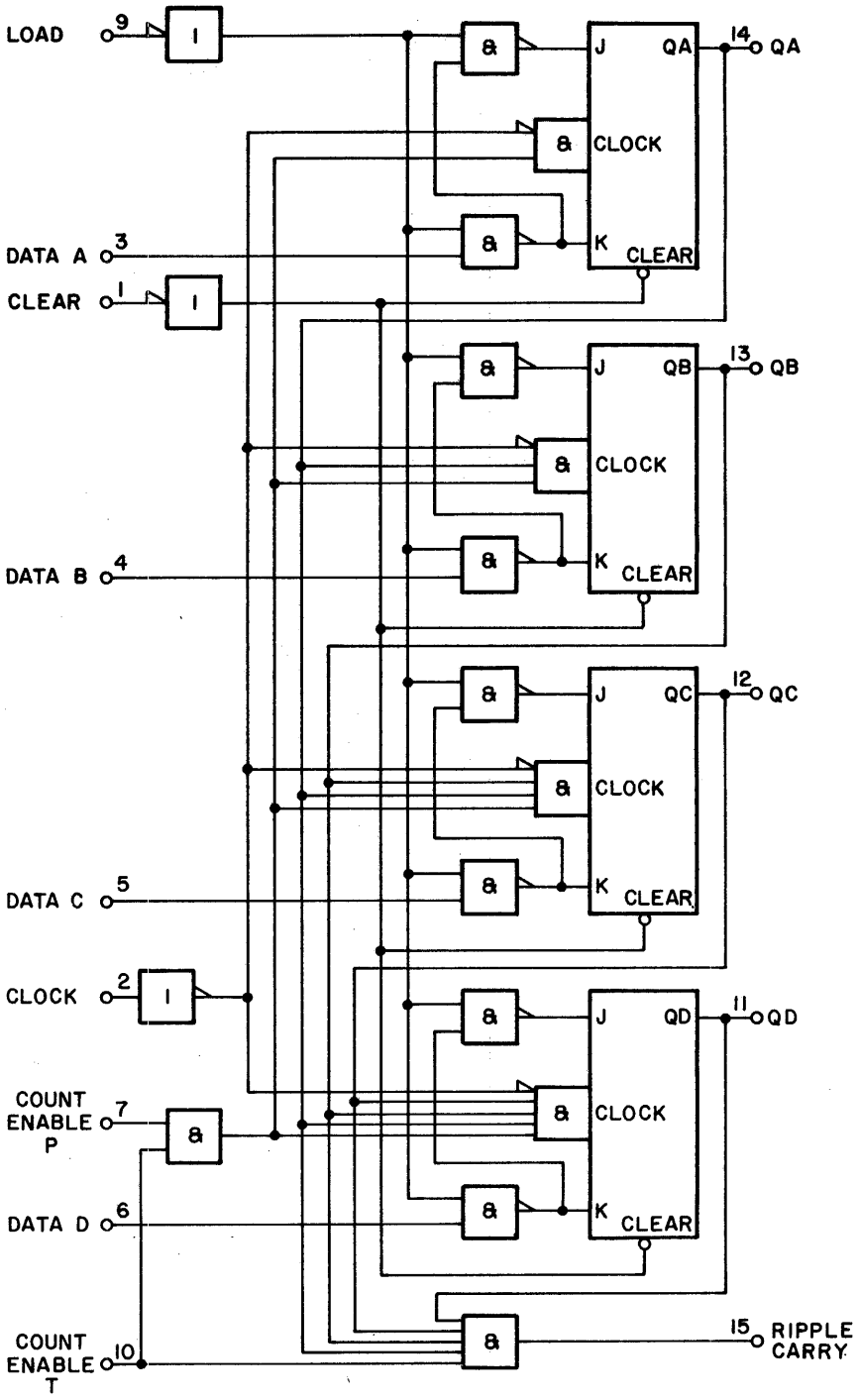
Ⓑ PIN 15 IS HIGH WHEN ALL OF THE FOLLOWING PINS ARE HIGH: 10, 11, 12, 13, AND 14.

Ⓒ ILLUSTRATED ABOVE IS THE FOLLOWING:
1. CLEAR OUTPUTS TO ZERO
2. PRESET TO BINARY 12
3. COUNT TO 13, 14, 15, 0, 1 AND 2
4. INHIBIT

Ⓓ

PIN(S)	FUNCTION
1	MASTER RESET (ACTIVE LOW) INPUT (CLEAR)
2	CLOCK ACTIVE HIGH GOING EDGE INPUT
3, 4, 5, 6	PARALLEL INPUTS
7	COUNT ENABLE PARALLEL INPUT
9	PARALLEL ENABLE (ACTIVE LOW) INPUT
10	COUNT ENABLE TRICKLE INPUT
11, 12, 13, 14	PARALLEL OUTPUTS
15	TERMINAL COUNT OUTPUT (CARRY)

TIMING SEQUENCE



FUNCTION DIAGRAM

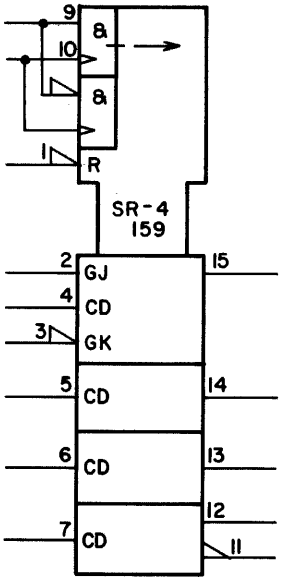
158
Rev B
Sheet 3 of 3

DESCRIPTION

The 159 circuit is a synchronous 4-bit shift register capable of shifting, counting, storage, and serial code conversion.

Data entry is synchronous; the outputs change state after each low to high transition of the clock. When the load/shift input is low, the parallel inputs determine the next condition of the shift register. When the load/shift input is high, the shift register performs a one bit shift to the right, with data entering the first stage flip-flop through the J-K (serial) inputs. By tying the J and K inputs together, D-type entry is obtained.

A low level to the clear input will clear the outputs to a low level regardless of the levels to any input.



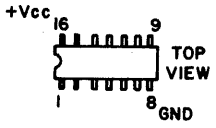
LOGIC SYMBOL

NOTES:

1. Vendor identification:

Element	Vendor Number
159	74195,9300
159LS	74LS195

2. Package pin configuration.



Pin	Function
1	Master Reset (clear)
2	First stage J input
3	First stage K input
4,5,6,7	Parallel data inputs
9	Load/Shift control
10	Clock
12,13,14,15	Parallel outputs
11	Complementary output ($\overline{12}$) for last stage

159
Rev B
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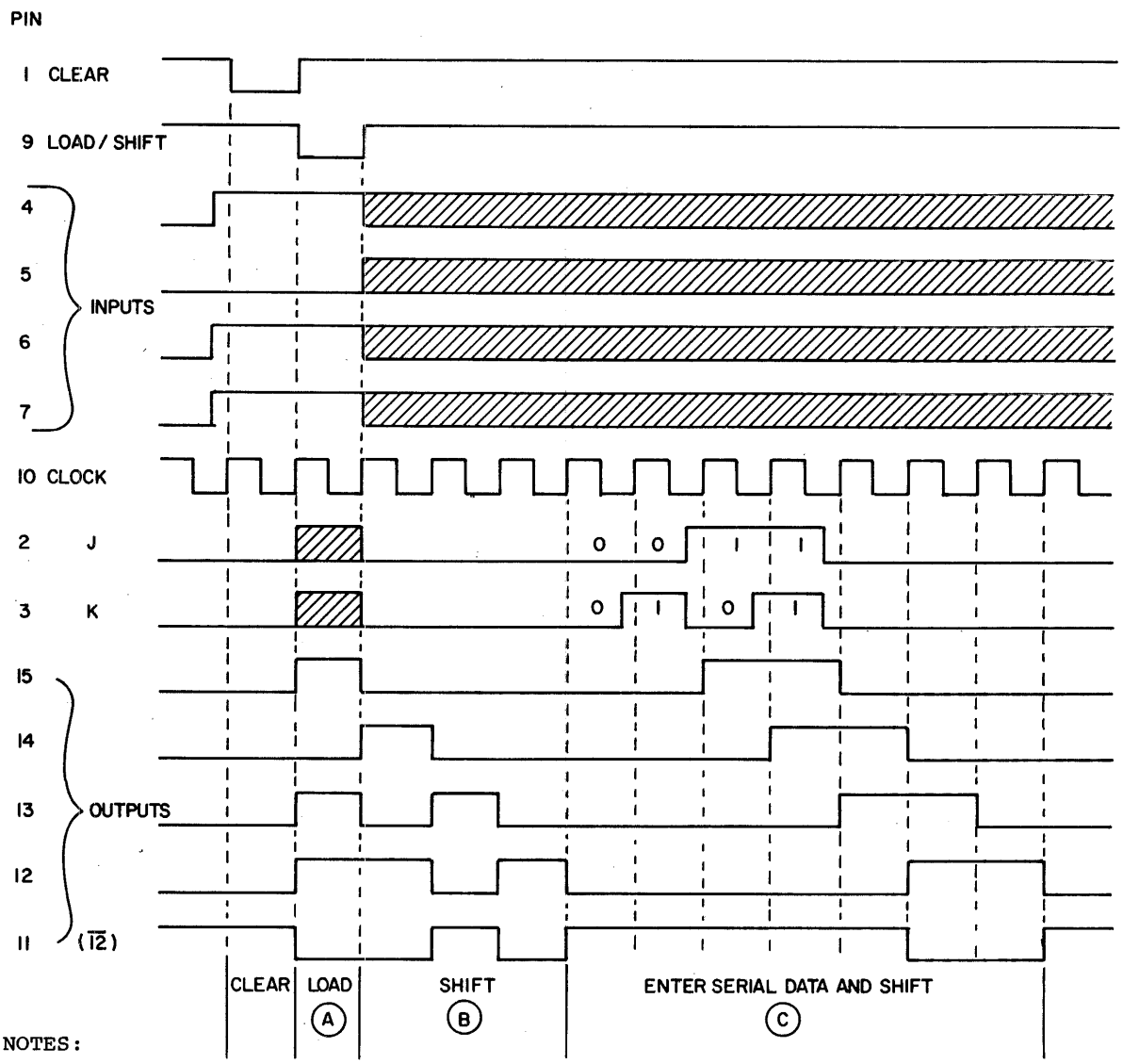


NOTES:

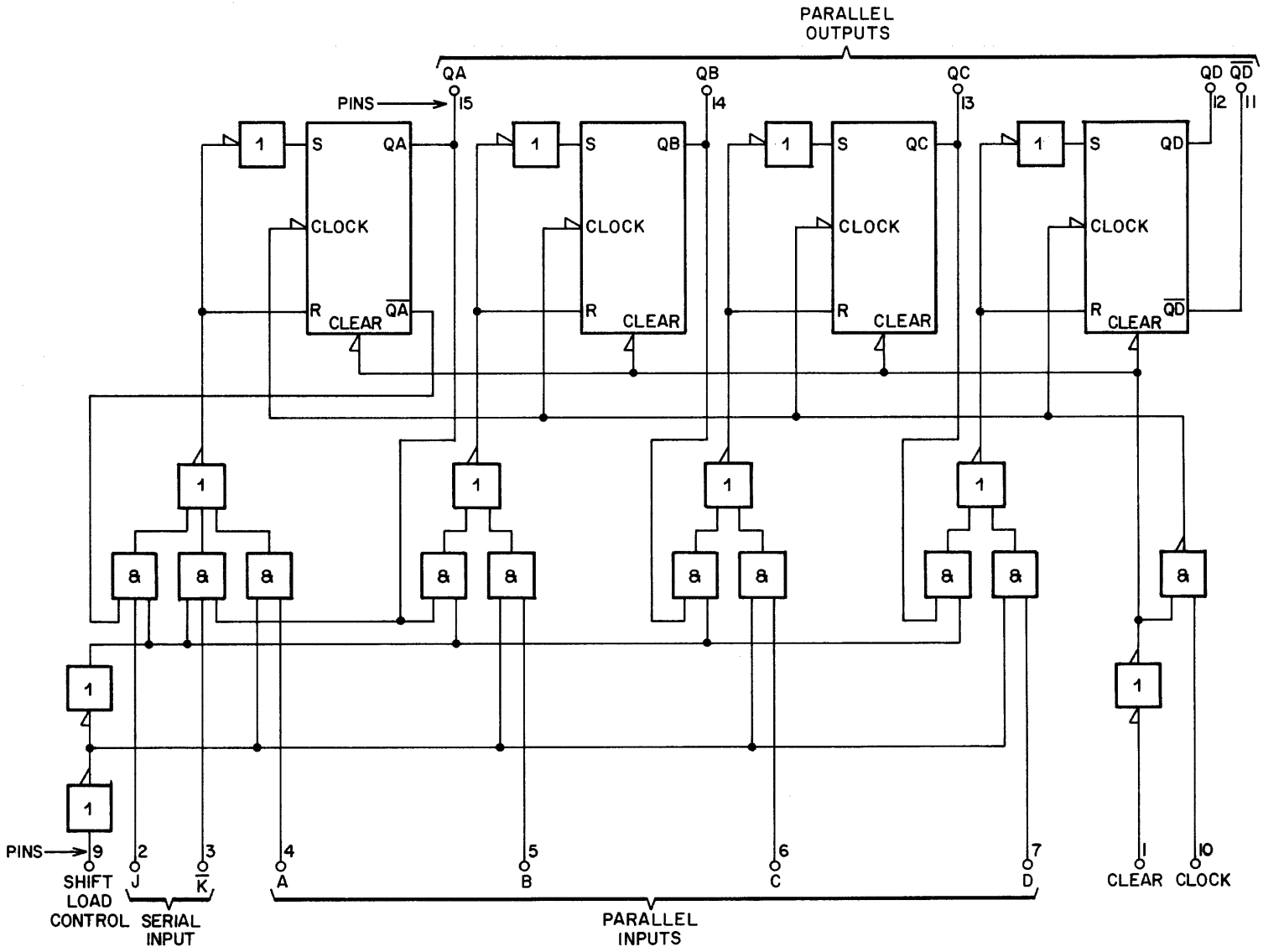
(A) Parallel data entered via CD inputs by pin 9 low and positive-going signal on pin 10.

(B) Data shifts down (Pin 15→Pin 14, etc.) with clock.

(C) Serial data entered into J-K inputs by pin 9 high and positive-going clock. Pin 4 input inhibited because pin 9 is high. Outputs follow Truth Table shown below. (Were J and K tied together, output at pin 15 would track the J input with no deviation from the Truth Table.)

INPUT PINS		OUTPUT PIN
2	3	15
0	0	0
0	1	0(NO CHANGE)
1	0	1(TOGGLES)
1	1	1

159
Rev B
Sheet 2 of 3

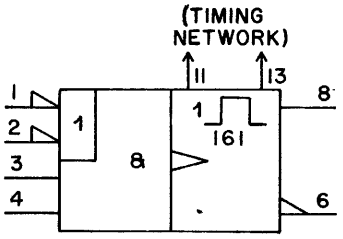


FUNCTION DIAGRAM

DESCRIPTION

The 161 circuit is a monostable retriggerable multivibrator that provides an output pulse whose duration is a function of external timing components.

Input pins 3 and 4 trigger on the positive going edge of the input pulse and pins 1 and 2 trigger on the negative going input pulse. The 161 circuit will retrigger while in the pulse timing state (pin 8 high); the end of the last pulse will be timed from the last input.

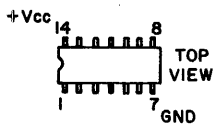


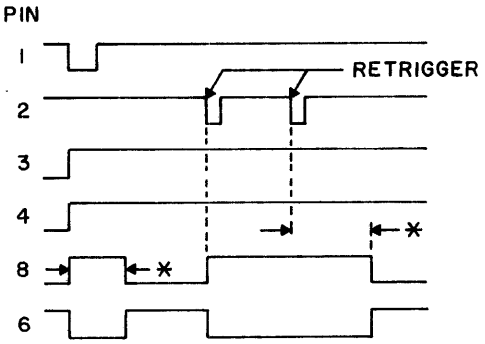
LOGIC SYMBOL

NOTES:

1. Vendor identification: 9601

2. Package pin configuration.





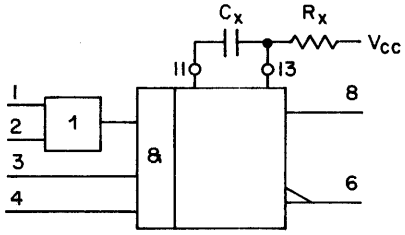
*PULSE WIDTH DETERMINED BY RC TIMING NETWORK

TIMING SEQUENCE

INPUT PINS				OPERATION	OUTPUT PINS	
1	2	3	4		8	6
H→L	H	H	H	TRIGGER	⎍	⎍
H	H→L	H	H	TRIGGER	⎍	⎍
L	X	L→H	H	TRIGGER	⎍	⎍
X	L	L→H	H	TRIGGER	⎍	⎍
L	X	H	L→H	TRIGGER	⎍	⎍
X	L	H	L→H	TRIGGER	⎍	⎍
H	H	H	H		L	H
X	X	L	X		L	H
X	X	X	L		L	H

X=DON'T CARE

TRUTH TABLE



OUTPUT PULSE WIDTH (t) IS DEFINED AS FOLLOWS:

$$t = 0.32\ R_x\ C_x \left[1 + \frac{0.7}{R_x}\right]$$

R_x IS IN kΩ, C_x IS IN pF, t IS IN ns

FUNCTION DIAGRAM

161
Rev C
Sheet 1 of 1

DESCRIPTION

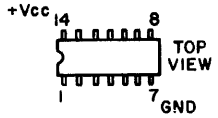
The 162 circuit is a dual differential line receiver. A minimum differential voltage of 25 mV is required to insure a high or low output level. Common mode voltages of ±3V or less will be rejected. The maximum allowable differential input voltage is 5 volts. The 162C features open-collector outputs.

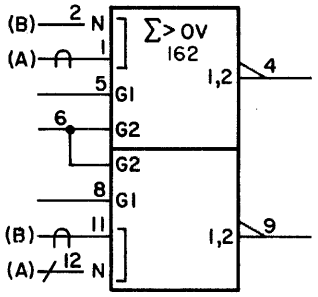
NOTES:

1. The two sections may be shown separately.
2. Vendor identification:

Element	Vendor Number
162	75107
162C	75108 *
162S	NE521F

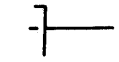
3. Package pin configuration.

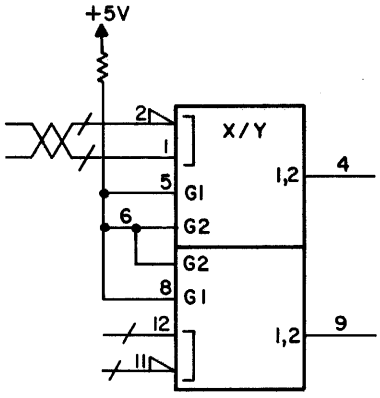




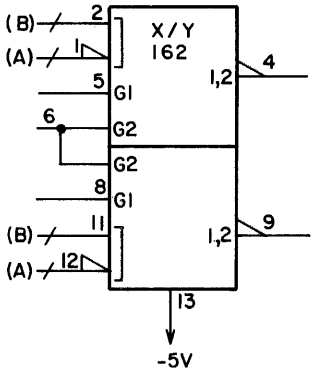
ANALOG TO DIGITAL CONVERTER APPLICATION

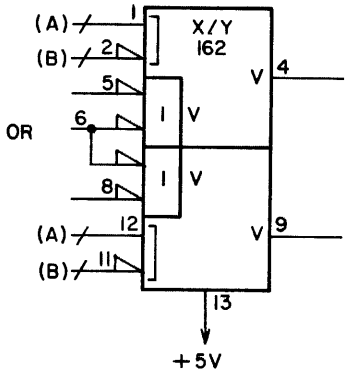
* 162C symbol is similar to others, but has the open-collector modifier by each output:

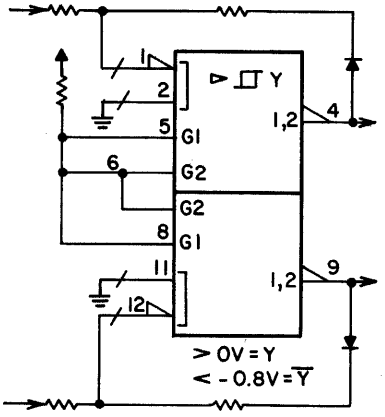




TWISTED PAIR RECEIVER APPLICATION

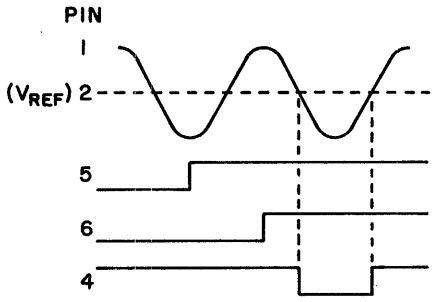






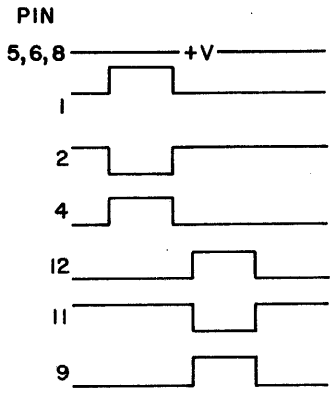
162 DUAL DIFFERENTIAL RECEIVER USED AS A SCHMITT TRIGGER WITH EXTERNAL FEEDBACK NETWORKS AND FIXED BIAS ENABLING G1 AND G2 STROBE INPUTS.

LOGIC SYMBOLS

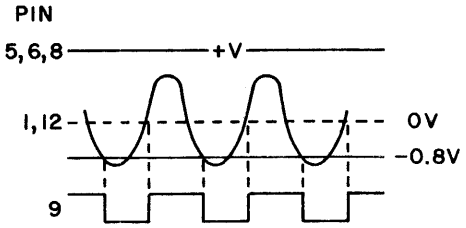


PIN 4 IS LOW ONLY IF G1 AND G2 ARE HIGH AND PIN 1 IS MORE NEGATIVE THAN PIN 2. G2 IS COMMON TO BOTH CONVERTERS.

162 DIGITAL TO ANALOG CONVERTER APPLICATION



162 TWISTED PAIR RECEIVER APPLICATION



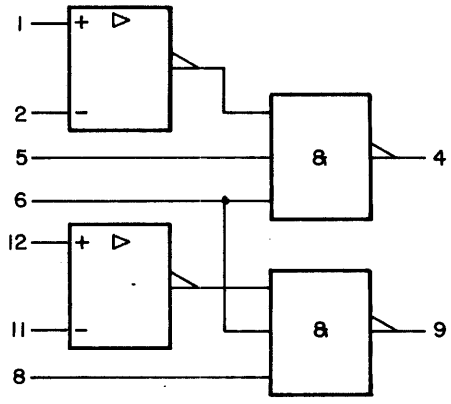
162 SCHMITT TRIGGER

TIMING SEQUENCE

DIFFERENTIAL INPUTS	STROBES		OUTPUT
	G1	G2	
$V_{ID} \geq 25MV$	L OR H	L OR H	H
$-25MV < V_{ID} < 25MV$	L OR H	L	H
	L	L OR H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25MV$	L OR H	L	H
	L	L OR H	H
	H	H	L

THE DIFFERENTIAL INPUT VOLTAGE POLARITIES SHOWN MEASURED AT PIN A WITH RESPECT TO PIN B. A MINUS POLARITY INDICATES THAT PIN A IS MORE NEGATIVE THAN PIN B.

TRUTH TABLE
(RCVR APPLICATION)



FUNCTION DIAGRAM

162
Rev B
Sheet 2 of 2

DESCRIPTION

Element 163 is a 4-bit binary counter, the first stage of which is independently clocked. This permits utilizing the first stage as an independent FF while using the other stages as an 8-counter, or using the IC as a 16-counter by cascading the first stage output to the input of the second stage.

For symbol outline and truth table, refer to the data sheet for element 182.

NOTES:

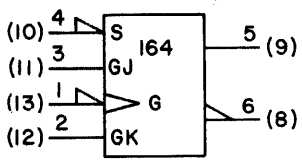
1. Vendor identification: 8281

2. Package pin configuration:

   14-pin DIP (see element 182)

DESCRIPTION

The 164 circuit is a dual negative-edge-triggered JK flip-flop. Each flip-flop is provided with a direct SET input. These direct inputs provide a means of presetting the flip-flop to initial conditions.



LOGIC SYMBOL

Data may be applied to or changed at the clocked inputs at any time during the clock cycle, except during the time interval between the set-up and hold-times. The inputs are inhibited when the clock is low and enabled when the clock rises. The JK inputs continuously respond to input information when the clock is high. The data state at the inputs throughout the interval between set-up and hold time is stored in the flip-flop when the clock pulse goes low. Each flip-flop may be set at any time without regard to the clock state by applying a low level to the SET input.

INPUT		OUTPUT BEFORE G		OUTPUT AFTER G	
J	K	SET	CLEAR	SET	CLEAR
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

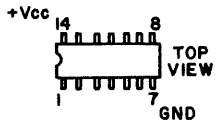
TRUTH TABLE

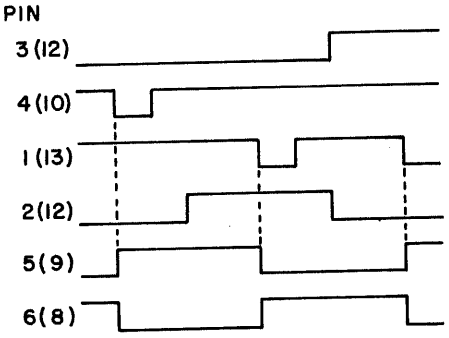
NOTES:

1. Symbol repeated for each flip-flop.
2. Vendor identification:

Element	Vendor Number
164H	3062
164S	74S113

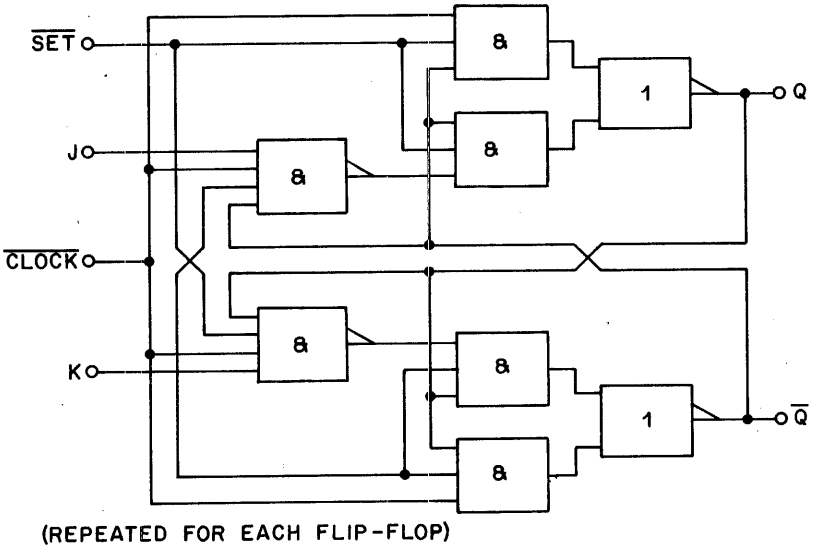
3. Package pin configuration.

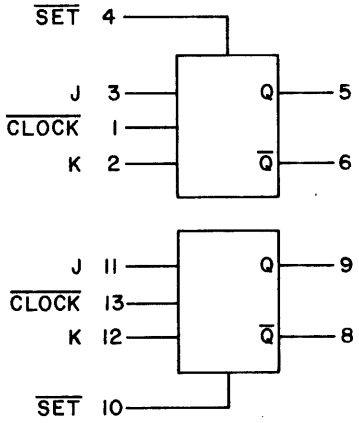




TIMING SEQUENCE

164
Rev C
Sheet 1 of 2





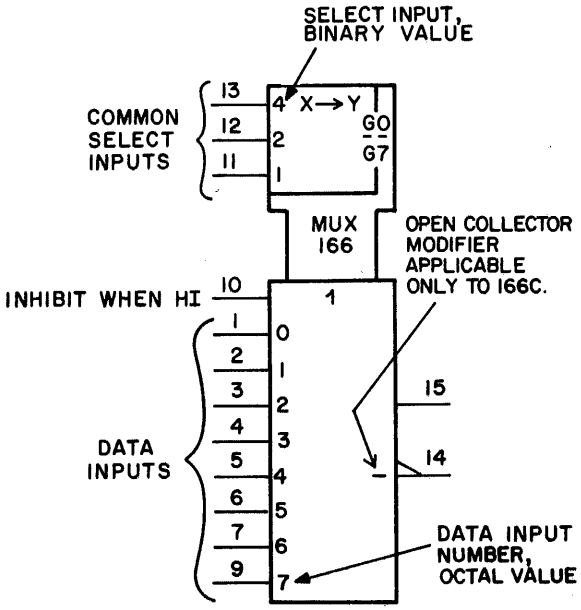
FUNCTION DIAGRAM

164
Rev C
Sheet 2 of 2

DESCRIPTION

The 166 circuit is a 1-of-8 (8-bit) multiplexer that can select one bit of data from up to eight sources. It has complementary outputs, an active low enable, and internal select decoding. With the enable inactive (high), output pin 15 is low and the complementary output pin 14 is high regardless of all input conditions. Data is routed from a particular data input to the outputs according to the binary code applied to the three select inputs.

Element 166C is identical in pin configuration and function, but provides an open-collector output on pin 14.



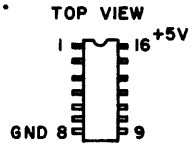
LOGIC SYMBOL

NOTES:

1. Vendor identification:

Element	Vendor Number
166	9312
166C	9313,8231

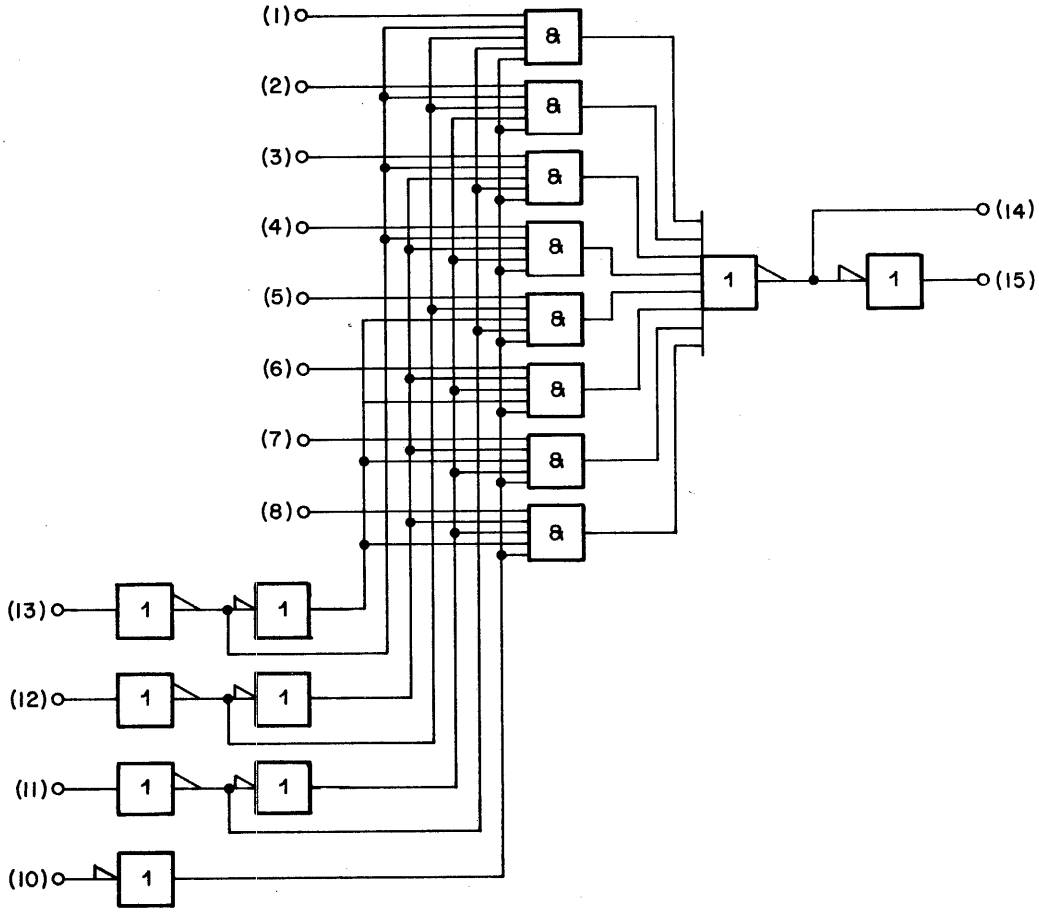
2. Package Pin configuration.



COMMON SELECT PIN			INPUT PIN GATED TO OUTPUT PIN 15 WHEN PIN 10 IS LOW *
13	12	11	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	9

* PIN 14 OUTPUT IS THE COMPLEMENT OF PIN 15. IF PIN 10 IS HIGH, PIN 15 IS LOW AND PIN 14 IS HIGH, REGARDLESS OF SELECT/DATA INPUTS.

TRUTH TABLE



FUNCTION DIAGRAM

166
Rev B
Sheet 2 of 2

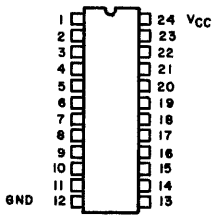
DESCRIPTION

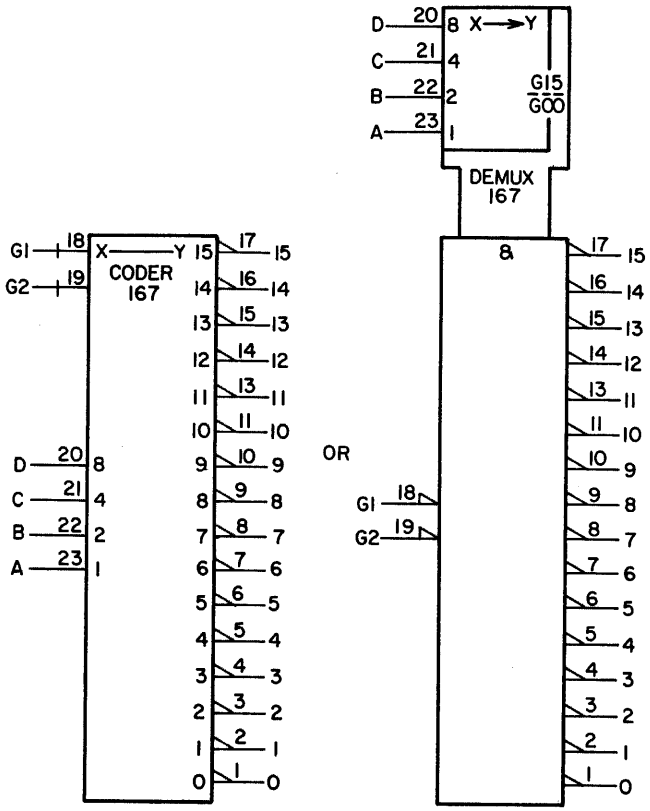
The 167 circuit is a 4-line-to-16-line decoder/demultiplexer. When inputs G1 and G2 are both low, the 167 decodes binary-coded data appearing on inputs A, B, C, and D. As shown in the truth table, one of the outputs 0 through 15 will be low corresponding to the binary coded data on the inputs.

This circuit also performs a demultiplexing function. To do this, it uses the A, B, C, D inputs to address an output, and routes data from the G1 or G2 input to the addressed output. When either G1 or G2 is high, all outputs are high. Thus data may enter at either G1 or G2 with the other input held low.

NOTES:

1. Vendor identification: 74154
2. Package pin configuration:



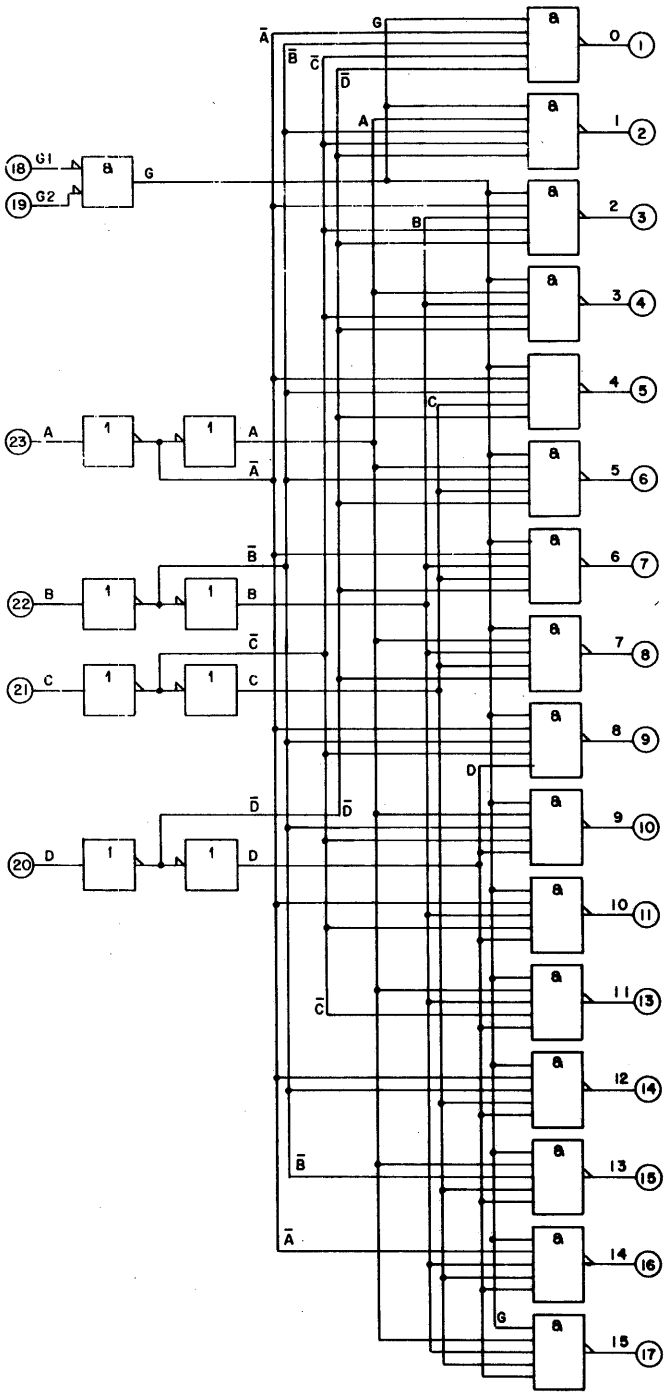


LOGIC SYMBOL

INPUTS						OUTPUTS														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

TRUTH TABLE

167
Rev A
Sheet 1 of 2



FUNCTIONAL DIAGRAM

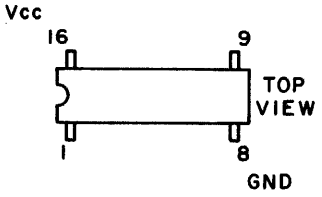
167
Rev A
Sheet 2 of 2

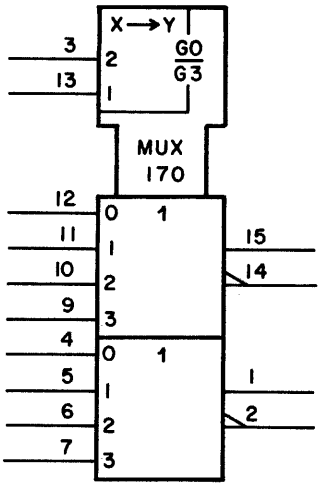
DESCRIPTION

The 170 circuit is a dual 4-input multiplexer. The binary code at select inputs (pins 3 and 13) determines the input selected.

NOTES:

1. Vendor identification: 9309
2. Package pin configuration.





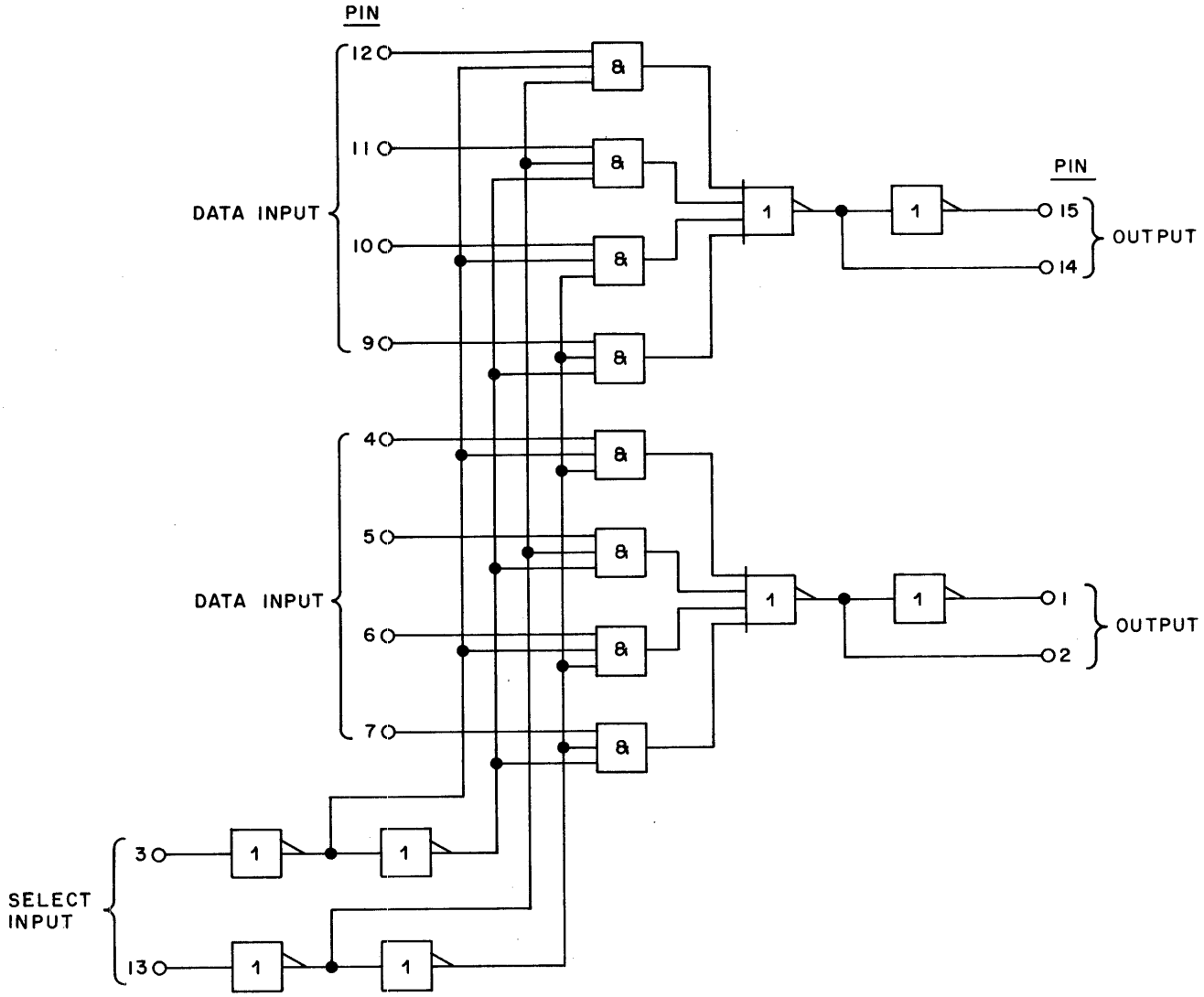
LOGIC SYMBOL

SELECT INPUTS		INPUTS				OUTPUTS	
3	13	4	5	6	7	1	2
		12	11	10	9	15	14
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = HIGH OR LOW LEVEL

TRUTH TABLE

170
Rev B
Sheet 1 of 2



FUNCTION DIAGRAM

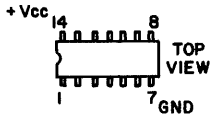
170
Rev B
Sheet 2 of 2

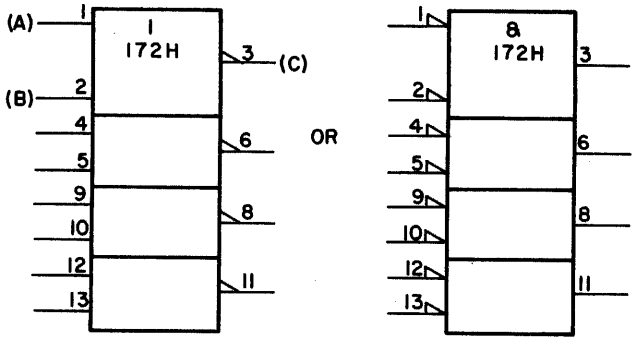
DESCRIPTION

The 172H circuit is a quad, 2-input, positive NOR gate.

NOTES:

1. Symbol Sections may appear separately.
2. Vendor identification: 3002
3. Package pin configuration.





LOGIC SYMBOL

A	B	C
0	0	1
1	0	0
0	1	0
1	1	0

TRUTH TABLE

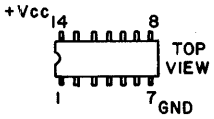
172
Rev D
Sheet 1 of 1

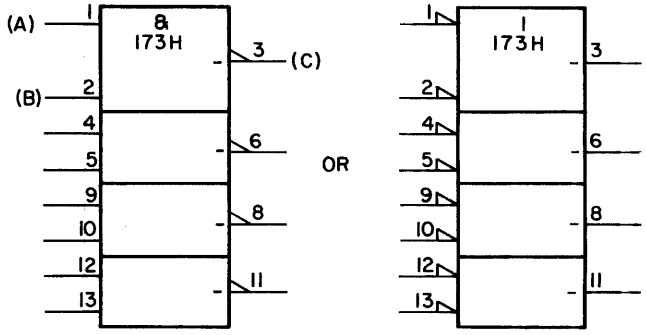
DESCRIPTION

The 173H circuit is a quad, 2-input,positive NAND gate with an open collector output.

NOTES:

1. Symbol Sections may appear separately.
2. Vendor identification: 3004
3. The output of each gate is an open collector.
4. Package pin configuration.





LOGIC SYMBOL

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

TRUTH TABLE

173
Rev C
Sheet 1 of 1

DESCRIPTION

The 175 circuit is a dual, positive-edge-triggered, D-type flip-flop. This device consists of two completely independent D flip-flops, both having direct SET and RESET inputs for asychronous operations such as parallel data entry in shift register application.

Information at input CD is transferred to output Q (pin 5/9) on the positive-going edge of the clock pulse. Clock pulse triggering occurs at a voltage level of the pulse and is not directly related to the transition time of the positive-going pulse. When the clock is at either the high or low level, the CD-input signal has no effect.

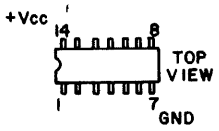
The flip-flop can also be set or cleared directly at any time regardless of the state of the clock by applying a low input to the SET or RESET inputs.

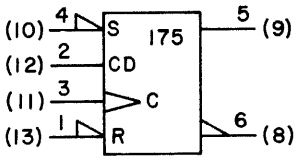
NOTES:

1. Symbol repeated for each flip-flop.
2. Vendor identification:

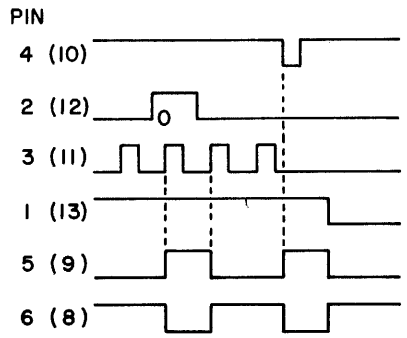
Element	Vendor Number
175	7474
175H	3060
175LS	74LS74
175S	74S74

3. Package pin configuration.

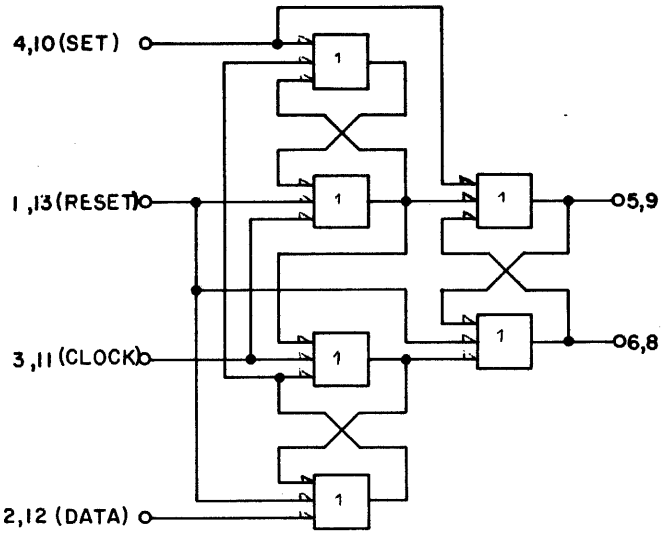




LOGIC SYMBOL



TIMING SEQUENCE



FUNCTION DIAGRAM
(EACH FLIP-FLOP)

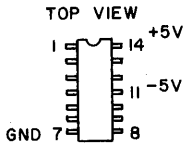
175
Rev B
Sheet 1 of 1

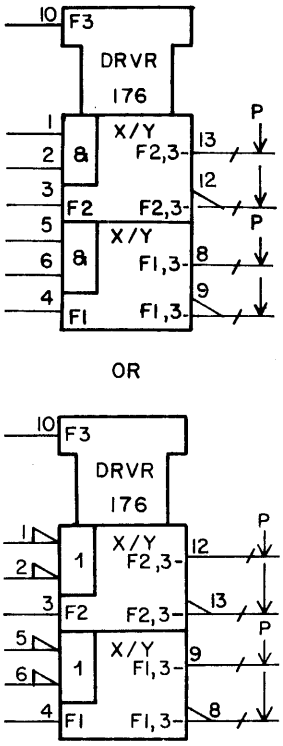
DESCRIPTION

The 176 circuit is a dual differential line driver. This circuit accepts a DTL or TTL logic signal and transmits it over a differential line pair. "On" state output current is typically 12 mA. "Off" state output current is 100 µA max. The output common mode voltage range is -3V to +10V with respect to the circuit ground.

NOTES:

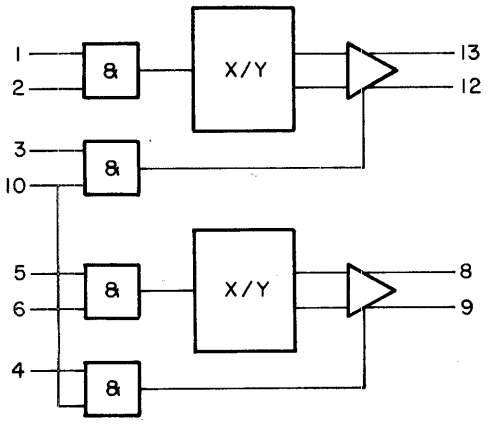
1. Type 176 Vendor identification: 75110
2. Package pin configuration.



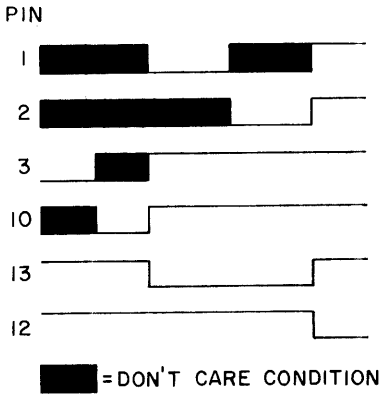


OR

LOGIC SYMBOL



FUNCTION DIAGRAM



TIMING SEQUENCE

LOGIC INPUTS		INHIBIT INPUTS		OUTPUTS *		OUTPUT CONDITION
1, 5	2, 6	3, 4	10	9, 12	8, 13	
1 OR 0 1 OR 0	1 OR 0 1 OR 0	0 1 OR 0	1 OR 0 0	1 1	1 1	INHIBITED
0 1 OR 0 1	1 OR 0 0 1	1 1 1	1 1 1	0 0 1	1 1 0	ACTIVE DATA STATE

* LOW OUTPUT REPRESENTS THE CURRENT ON STATE.
HIGH OUTPUT REPRESENTS THE CURRENT OFF STATE.

TRUTH TABLE

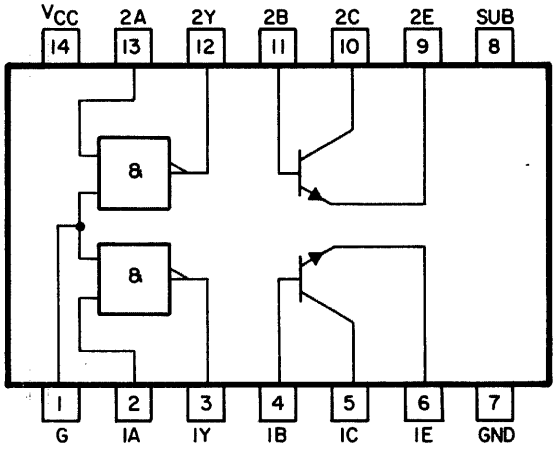
176
Rev D
Sheet 1 of 1

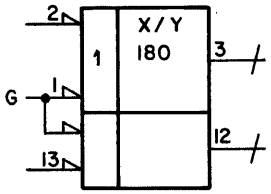
DESCRIPTION

Element 180 consists of two positive NAND drivers with a common strobe (G), as shown in the Basic Symbol. The package also provides two high-current, high-voltage n-p-n transistors with separate pin-outs. The representation of the transistor-only function depends upon how each transistor is connected (see Supplemental Symbols).

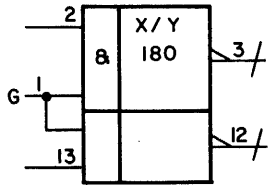
NOTES:

1. Vendor identification: 75450A
2. Package pin configuration and functional diagram:

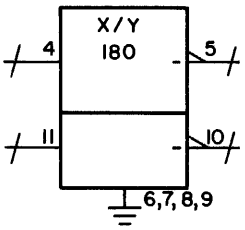




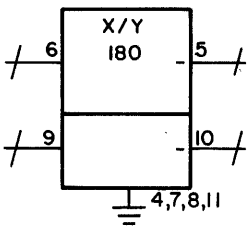
OR



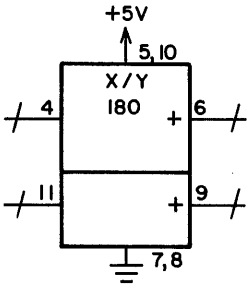
BASIC SYMBOL



GROUNDED EMITTER



GROUNDED BASE



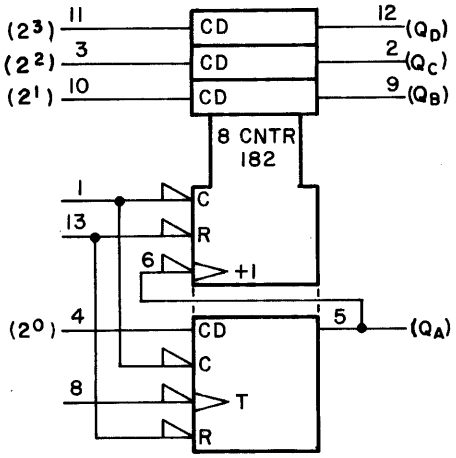
EMITTER FOLLOWER

SUPPLEMENTAL SYMBOLS

180
Rev A
Sheet 1 of 1

DESCRIPTION

Circuit type 182 is a 4-bit binary counter. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. The direct clear (pin 13), when taken low, sets all outputs low regardless of the states of the clocks (pins 8 and 6). The 182 is fully programmable; that is, the counter may be preset to any state by placing a low ("0") on the count/load input (pin 1) and entering the desired data at the inputs. The outputs will then change to agree with the data inputs independent of the state of the clock inputs. This allows the 182 to be used as a 4-bit latch (register application) by inactivating the clock inputs and using the count/load input as a data strobe.



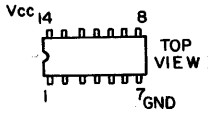
LOGIC SYMBOL

NOTES:

1. Vendor identification:

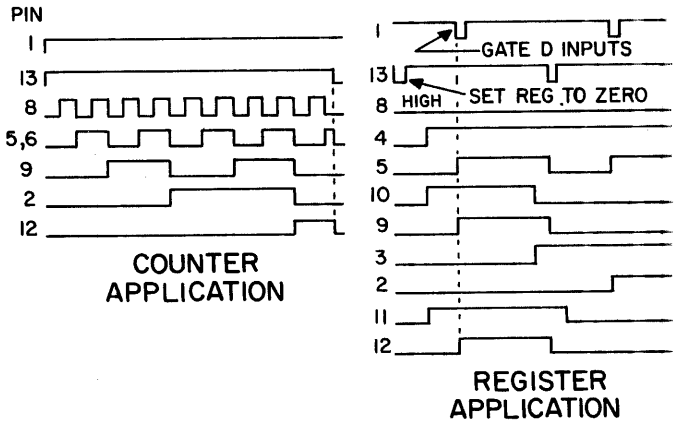
Element	Vendor Number
182	74197,8291
182S	82S91

2. Package pin configuration.



COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

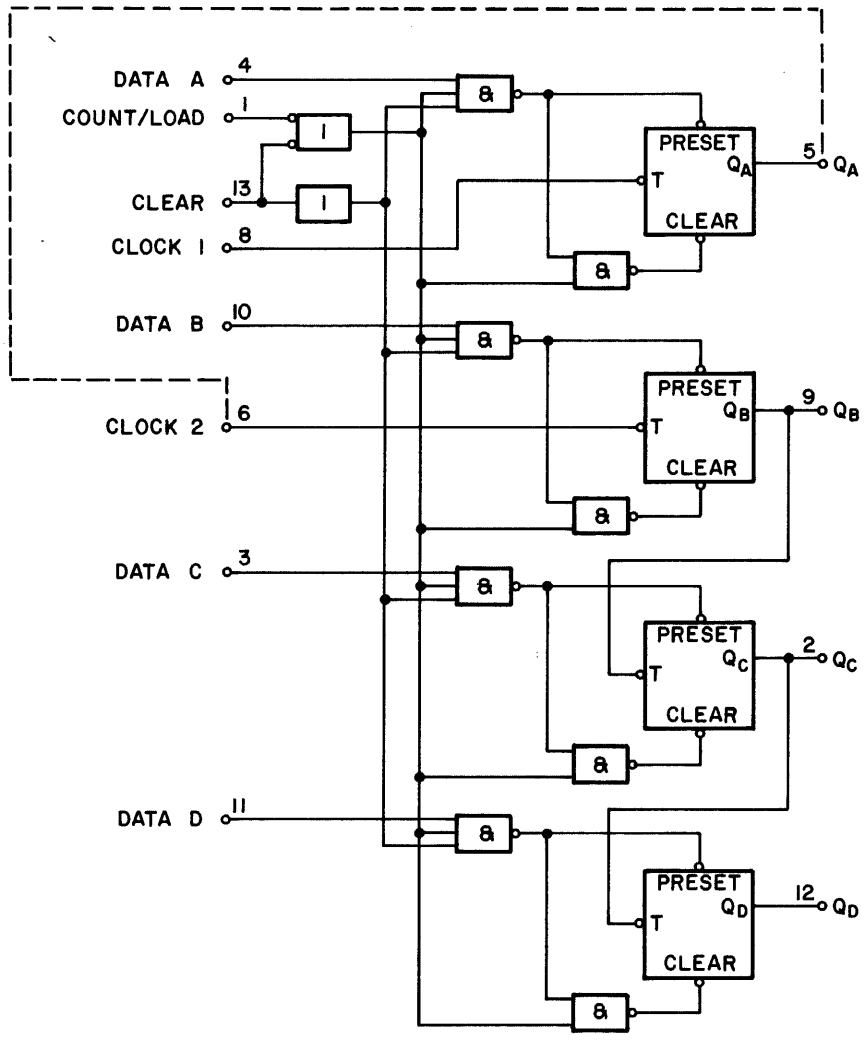
TRUTH TABLE
(WITH PINS 5 AND 6 WIRED TOGETHER)



TIMING SEQUENCE

182
Rev B
Sheet 1 of 2

CONNECT PINS 5 & 6 FOR 4-BIT COUNTING, USING DATA INPUT A. AS A 3-BIT COUNTER, DATA INPUT B IS USED. FIRST STAGE MAY THEN BE USED AS AN INDEPENDENT DATA LATCH IF COUNT/LOAD AND CLEAR FUNCTIONS COINCIDE WITH THOSE OF THE COUNTER.



FUNCTION DIAGRAM

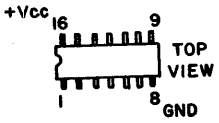
182
Rev B
Sheet 2 of 2

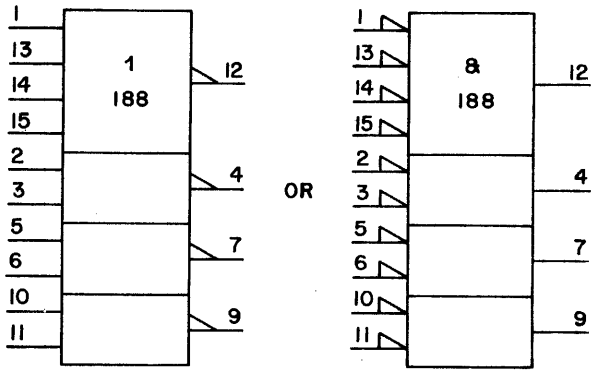
DESCRIPTION

The 188 circuit consists of one 4-input and three 2-input positive NOR gates.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 9015
3. Package pin configuration.





LOGIC SYMBOL

188
Rev C
Sheet 1 of 1

DESCRIPTION

Circuit type 189 is a quad 1-of-2 (2-input) multiplexer.

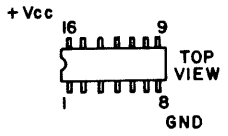
When the inhibit (pin 15) is high all outputs are held low.

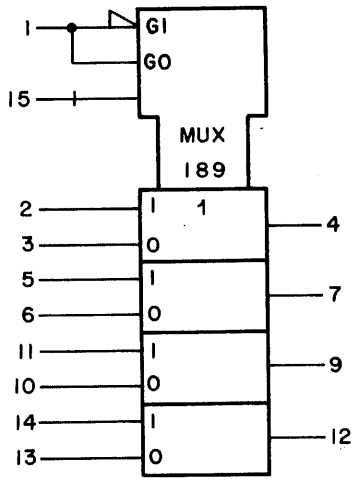
NOTES:

1. Vendor identification:

Element	Vendor Number
189	74157/9322
189L	74L157
189LS	74LS157
189S	74S157

2. Package pin configuration.

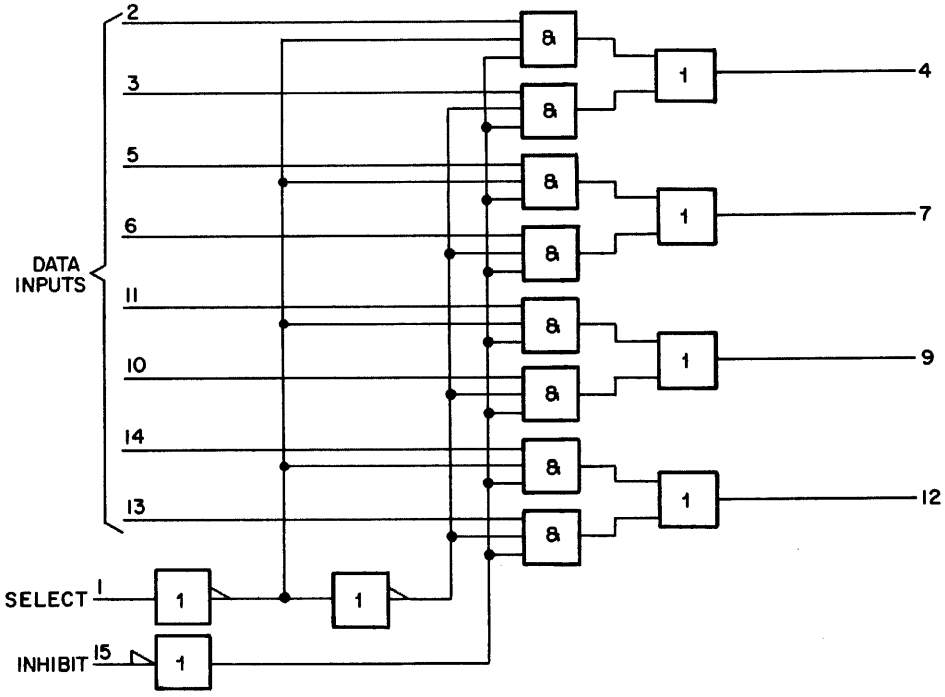




LOGIC SYMBOL

INH	SEL	INPUTS		OUTPUT
		0	1	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

TRUTH TABLE
(ANY SECTION)
L = LOW LEVEL
H = HIGH LEVEL
X = IRRELEVANT



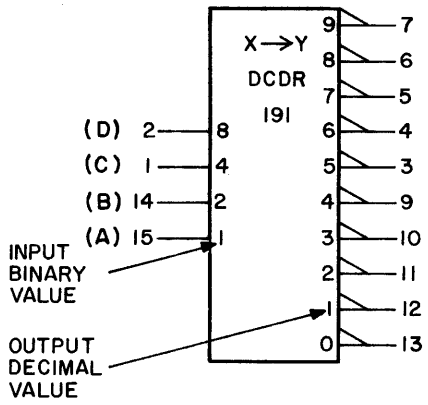
FUNCTION DIAGRAM

189
Rev D
Sheet 1 of 1

DESCRIPTION

Circuit type 191 is a BCD-to-decimal (1-of-10) decoder. Four active-high BCD inputs provide one of ten mutually exclusive active-low outputs. When a binary code greater than 9 is applied, all outputs are high. This facilitates BCD to decimal conversions and eight-channel demultiplexing and decoding.

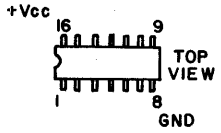
The 191 circuit can serve as a one-of-eight decoder with the D input acting as the active-low enable. Eight-channel demultiplexing then results when the desired output is addressed by inputs A, B, and C.



LOGIC SYMBOL

NOTES:

1. Vendor identification: 9301
2. Package pin configuration.

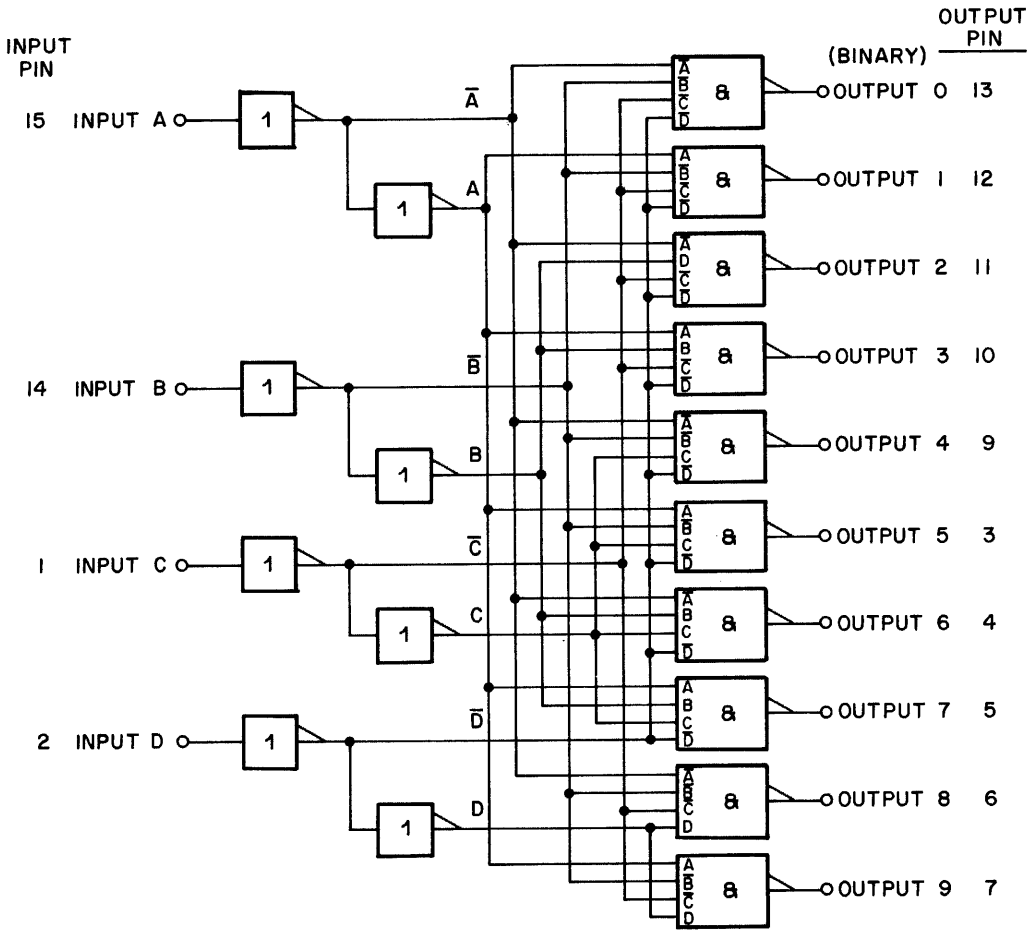


INPUT PIN				LO ("0") OUTPUT PIN (OTHER OUTPUTS = "1")
2	1	14	15	
0	0	0	0	13
0	0	0	1	12
0	0	1	0	11
0	0	1	1	10
0	1	0	0	9
0	1	0	1	3
0	1	1	0	4
0	1	1	1	5
1	0	0	0	6
1	0	0	1	7
1	0	1	0	*
1	0	1	1	*
1	1	0	0	*
1	1	0	1	*
1	1	1	0	*
1	1	1	1	X

* = ALL OUTPUT PINS HIGH

TRUTH TABLE

191
Rev B
Sheet 1 of 2



FUNCTION DIAGRAM

191
Rev B
Sheet 2 of 2

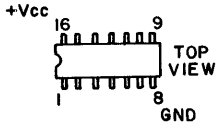
DESCRIPTION

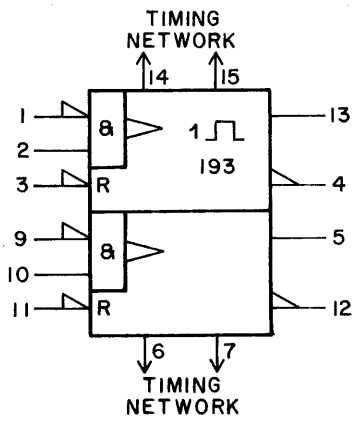
The 193 circuit is a two-section retriggerable monostable multivibrator. Triggering the input before the output pulse is terminated extends the output pulse duration. The overriding clear input (pin 3/11) immediately terminates any output pulse.

Successive inputs having a cycle time shorter than the delay time produce a constant high output from pin 13/5.

NOTES:

1. Vendor identification: 74123
2. Package pin configuration.

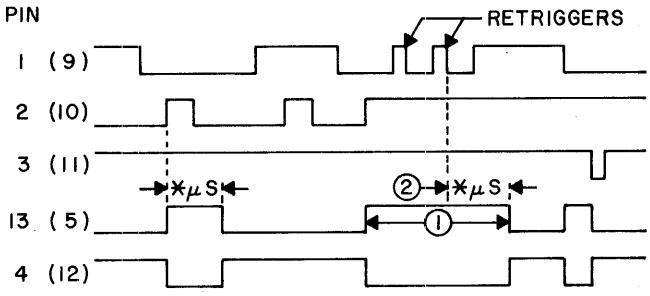




LOGIC SYMBOL

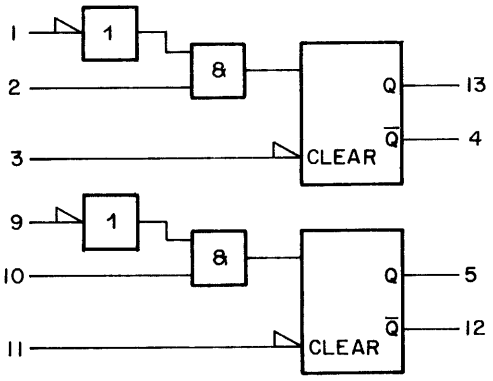
INPUT PINS		OUTPUT PINS	
1 (9)	2 (10)	13 (5)	4 (12)
H	X	L	H
X	L	L	H
L	↑	⊓	⊓
↓	H	⊓	⊓

TRUTH TABLE



* PULSE DURATION IS A FUNCTION OF THE RC TIMING NETWORK.
① OUTPUT HELD HIGH DURING RETRIGGER PULSE.
② OUTPUT TIMES OUT FROM EDGE OF LAST TRIGGER PULSE.

TIMING SEQUENCE

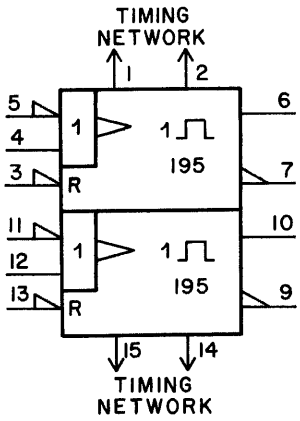


FUNCTION DIAGRAM

193
Rev B
Sheet 1 of 1

DESCRIPTION

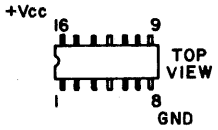
The 195 circuit is a dual retriggerable monostable multivibrator. Input pins 4 and 12 trigger on the positive-going edge of the input pulse and pins 5 and 11 trigger on the negative-going edge. The 195 circuit will retrigger while in the pulse timing state (pin 3/13 high) and the end of the last pulse will be timed from the last input. A low level to the reset input (pin 3/13) resets pin 6/10 to low level and inhibits data inputs.



LOGIC SYMBOL

NOTES:

1. The full timing network would be shown on the logic diagram.
2. Vendor identification: 9602
3. Package pin configuration.

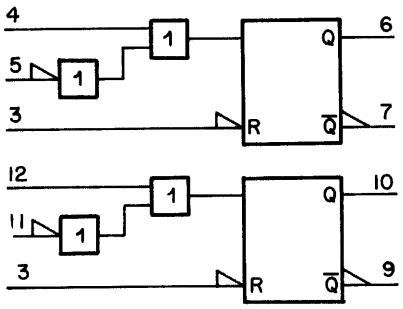


4. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎏ = one low level pulse, X = irrelevant (any input, including transitions).

5. Output pulse width (t) is defined as follows:

$$t = 0.32\ R_X\ C_X \left[1 + \frac{0.7}{R_X}\right]$$

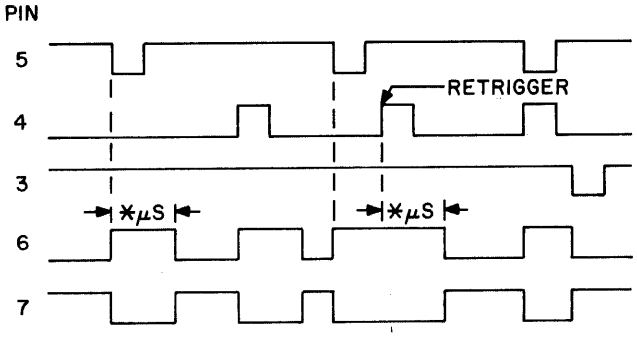
R_X is in kΩ, C_X is in pF t is in ns



FUNCTION DIAGRAM

INPUT PINS			OUTPUT PINS	
5(11)	4(12)	3(13)	6(7)	10(9)
↓	L	H	⎍	⎏
H	↑	H	⎍	⎏
X	X	L	L	H

TRUTH TABLE
(SEE NOTE 4)



* PULSE DURATION IS A FUNCTION OF THE RC TIMING NETWORK.

TIMING SEQUENCE

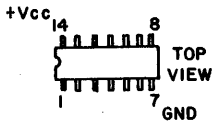
195
Rev B
Sheet 1 of 1

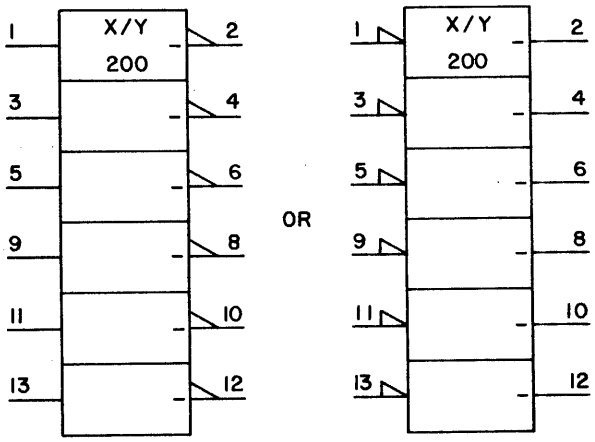
DESCRIPTION

The 200 circuit is a hex inverter buffer/ driver with an open-collector output.

NOTES:

1. Symbol sections may be shown separately.
2. Vendor identification: 7406
3. Package pin configuration.





LOGIC SYMBOL

200
Rev B
Sheet 1 of 1

DESCRIPTION

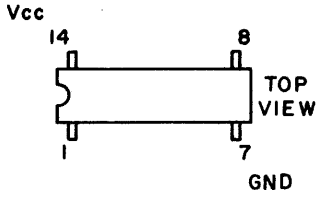
The 201 circuit is a quad, 2-input, positive AND gate. Version 201C provides open-collector outputs.

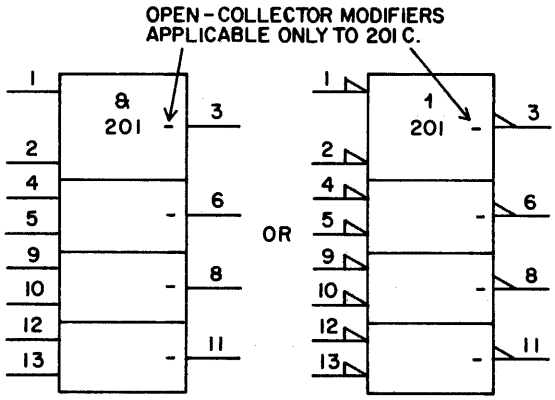
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
201	7408
201H	74H08
201L	74L08
201LS	74LS08
201C	7409

3. Package pin configuration.





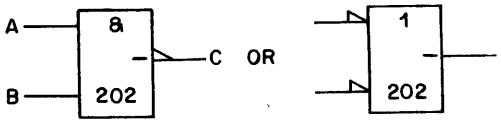
LOGIC SYMBOL

INPUT	OUTPUT
0 0	0
0 1	0
1 0	0
1 1	1

TRUTH TABLE
(FOR ONE GATE)

DESCRIPTION

The 202 circuit is an quad, 2-input,positive NAND gate with an open-collector output.



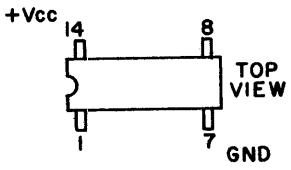
LOGIC SYMBOL

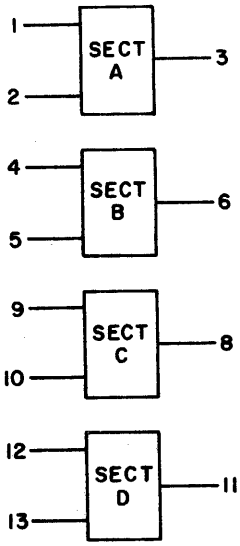
NOTES:

1. Symbol repeated for each gate.
2. Vendor identification:

Element	Vendor Number
202	7403
202H	74H01
202LS	74LS03
202S	74S03

3. Package pin configuration.





FUNCTION DIAGRAM

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

TRUTH TABLE

202
Rev B
Sheet 1 of 1

DESCRIPTION

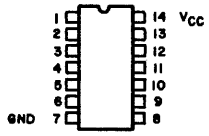
The 203 circuit consists of six individual inverters with open-collector outputs. Each output must be connected to an external pull-up resistor tied to VCC. Each inverter performs the function $Y=\overline{A}$.

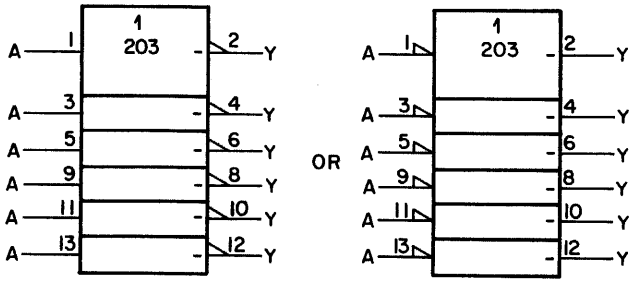
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
203	7405
203H	74H05
203LS	74LS05
203S	74S05

3. Package pin configuration:





LOGIC SYMBOL

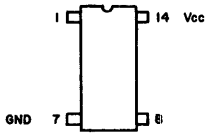
203
Rev A
Sheet 1 of 1

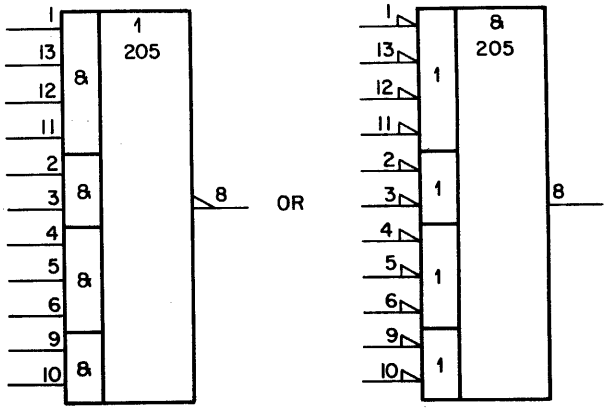
DESCRIPTION

The 205S circuit is a 4-2-3-2-input AND-OR-INVERT gate.

NOTES:

1. Vendor identification: 74S64
2. Package pin configuration:





LOGIC SYMBOL

205
Rev A
Sheet 1 of 1

DESCRIPTION

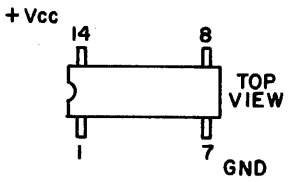
Element 206 is an 8-input,positive NAND gate.

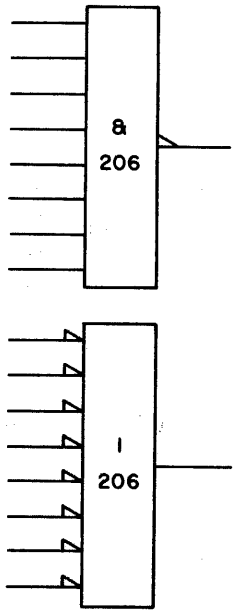
NOTES:

1. Vendor identification:

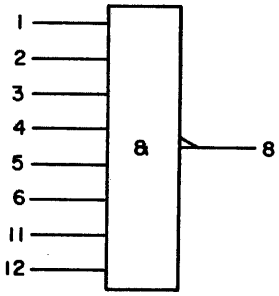
Element	Vendor Number
206	7430
206H	74H30
206L	74L30
206LS	74LS30
206S	74S30

2. Package pin configuration.





LOGIC SYMBOL



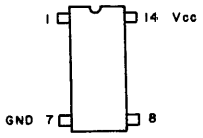
206
Rev B
Sheet 1 of 1

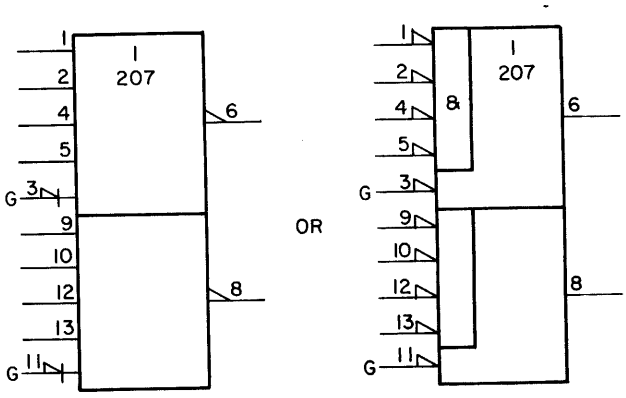
DESCRIPTION

The 207 circuit is a dual, 4-input, positive NOR gate with a separate strobe input (G) for each section.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 7425
3. Package pin configuration:

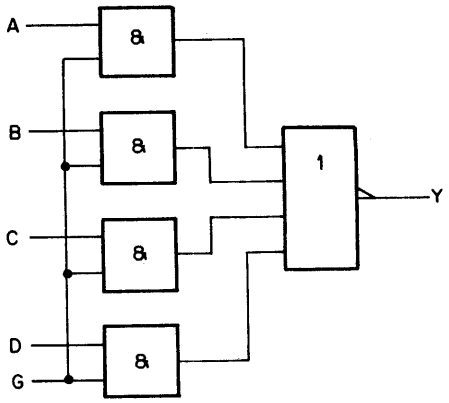




LOGIC SYMBOL

INPUTS					OUTPUT
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

TRUTH TABLE

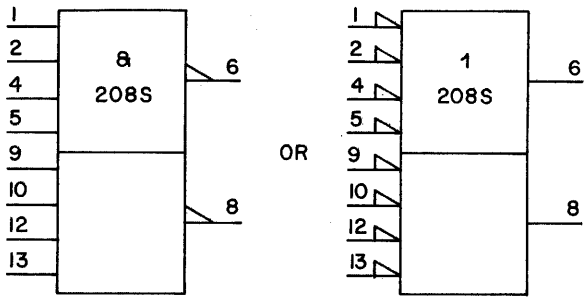


FUNCTIONAL DIAGRAM
(HIGH ACTIVE LOGIC)

207
Rev B
Sheet 1 of 1

DESCRIPTION

Type 208 is a dual, 4-input, positive NAND gate.



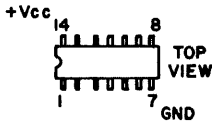
LOGIC SYMBOL

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
208	7420
208H	74H20
208L	74L20
208LS	74LS20
208S	74S20

3. Package pin configuration.



INPUTS				OUTPUT
A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

TRUTH TABLE

208
Rev B
Sheet 1 of 1

DESCRIPTION

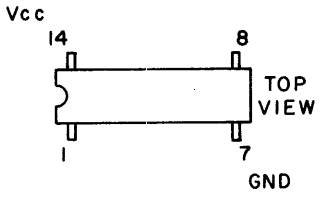
The 209 circuit is a 4-wide, 2-input AND-OR-INVERT gate. Expander gates can be connected to pins 11 and 12, otherwise these pins are left open.

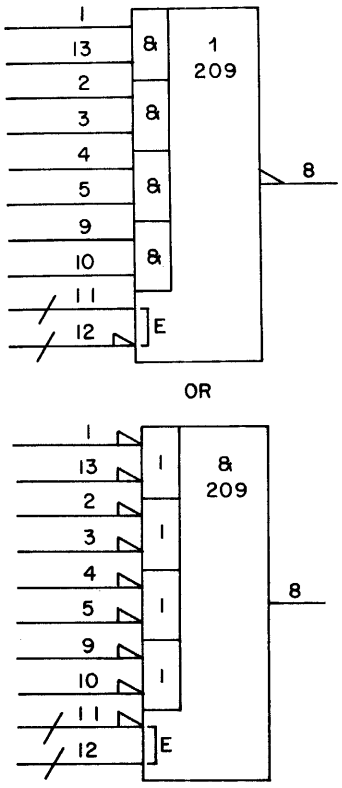
NOTES:

1. Vendor identification:

Element	Vendor Number
209	7453
209H	74H53

2. Package pin configuration.



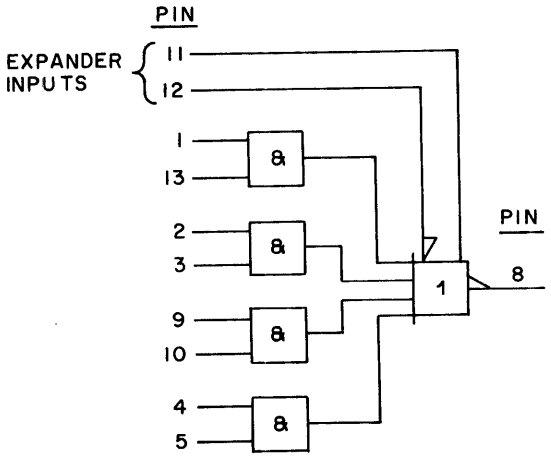


LOGIC SYMBOL

INPUT PINS								OUTPUT
1	13	2	3	9	10	4	5	8
H	H	X	X	X	X	X	X	L
X	X	H	H	X	X	X	X	L
X	X	X	X	H	H	X	X	L
X	X	X	X	X	X	H	H	L
L	X	L	X	L	X	L	X	H

H=HIGH LEVEL
L=LOW LEVEL
X=EITHER HIGH OR LOW LEVEL

TRUTH TABLE



FUNCTION DIAGRAM

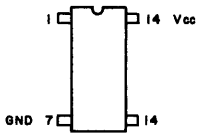
209
Rev C
Sheet 1 of 1

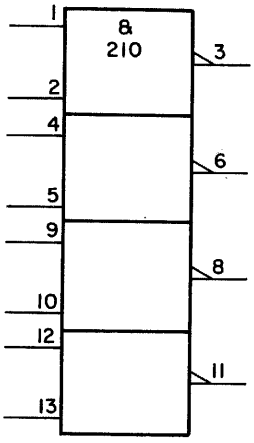
DESCRIPTION

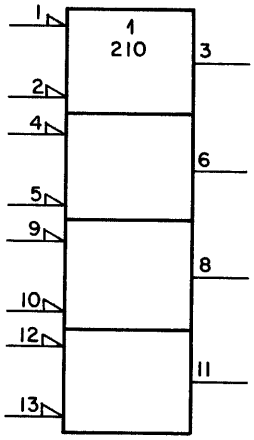
The 210 circuit is a quad, 2-input, positive NAND buffer. The buffered output provides a maximum fan-out of 30 for each section.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 7437
3. Package pin configuration:







210
Rev A
Sheet 1 of 1

DESCRIPTION

The 212 circuit is a dual, 4-input, positive AND gate.

The AND function is: $Y=ABCD$

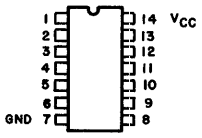
The OR function is: $\overline{Y}=\overline{A}+\overline{B}+\overline{C}+\overline{D}$

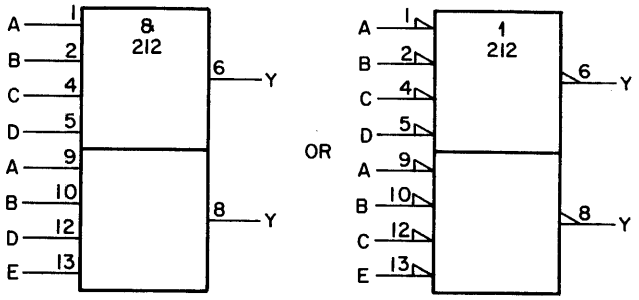
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
212	7421
212H	74H21

3. Package pin configuration:





LOGIC SYMBOL

212
Rev B
Sheet 1 of 1

DESCRIPTION

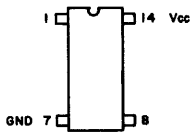
Element 213 is a triple, 3-input, positive AND gate.

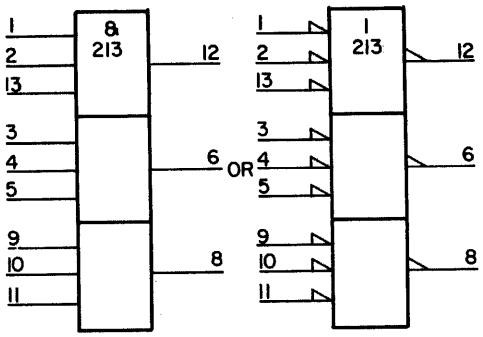
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
213H	74H11
213LS	74LS11
213S	74S11

3. Package pin configuration:



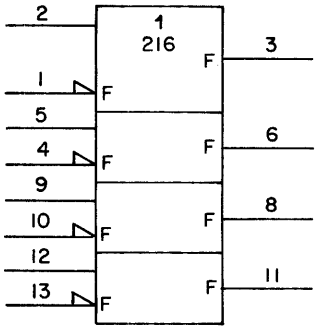


LOGIC SYMBOL

213
Rev A
Sheet 1 of 1

DESCRIPTION

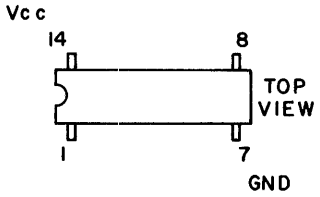
Circuit type 216 is a tri-state,quad,2-input buffer. Each buffer section has a control input and data input. A low level at the control input pin enables non-inverting data to pass through from the data input pin. A high level at the control input pin switches the buffer to the high impedance state, thus inhibiting signals applied to the data input pin. Input data applied to the buffer output pin also sees a high impedance; this is significant in applications that transmit in both directions on a common line.



LOGIC SYMBOL

NOTES:

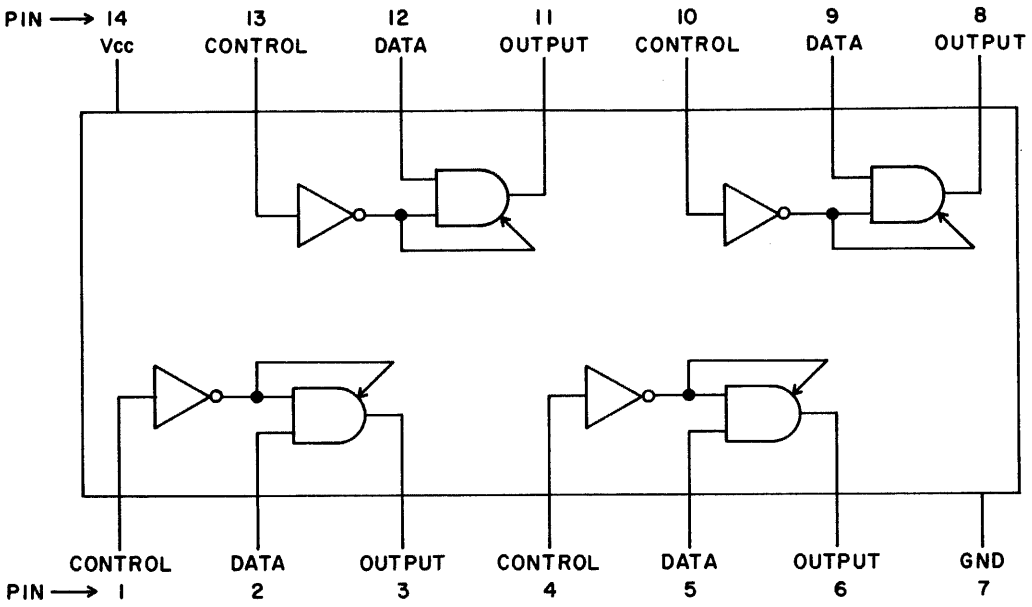
1. Symbol sections may appear separately.
2. Vendor identification: 8093
3. Package pin configuration.



DATA	CONTROL	OUTPUT
PIN 2	PIN 1	PIN 3
1	0	1
0	0	0
X	1	Hi-Z

X = EITHER HIGH OR LOW LEVEL
Hi-Z = HIGH IMPEDANCE STATE

TRUTH TABLE
(FOR ONE SECTION)



FUNCTION DIAGRAM

DESCRIPTION

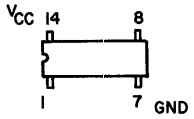
Element 218 is a quad, 2-input, positive OR gate.

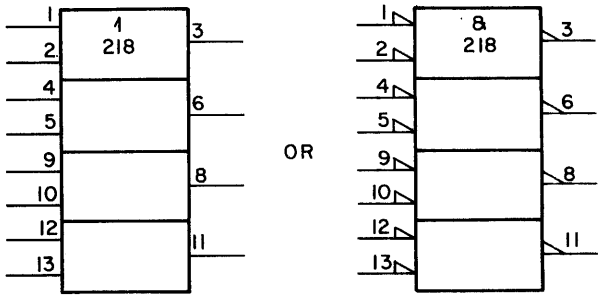
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
218	7432
218H	3003
218LS	74H32

3. Package pin configuration.





LOGIC SYMBOL

218
Rev B
Sheet 1 of 1

DESCRIPTION

The 220H circuit is an expandable, 2-wide, positive AND-OR-INVERT (AOI) gate. The number of inputs can be increased by an external "expander" circuit (e.g. 214H) that, in essence, shorts inputs X and $\overline{X}$. If the expansion feature is not used, X and $\overline{X}$ must be left open.

For AOI, the circuit function is:

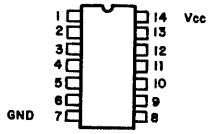
$$Y=\overline{ABCD+EFGH+X}.$$

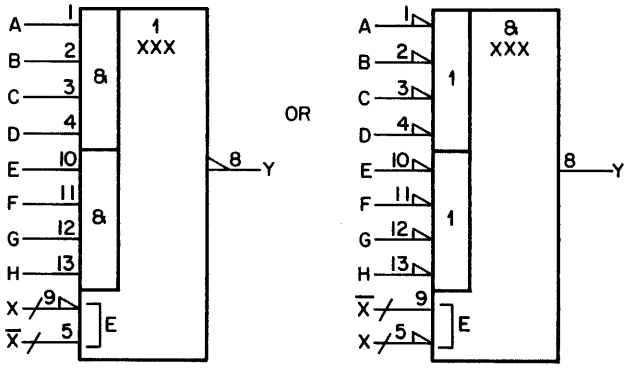
For OAI, the circuit function is:

$$Y=\overline{(A+B+C+D)(E+F+G+H)X}.$$

NOTES:

1. Vendor identification: 74H55
2. Package pin configuration:





LOGIC SYMBOL

INPUTS									OUTPUT
A	B	C	D	E	F	G	H	X	Y
X	X	X	X	X	X	X	X	H	L
X	X	X	X	H	H	H	H	X	L
H	H	H	H	X	X	X	X	X	L
L	X	X	X	←Z→				L	H
X	L	X	X	←Z→				L	H
X	X	L	X	←Z→				L	H
X	X	X	L	←Z→				L	H
←Z→				L	X	X	X	L	H
←Z→				X	L	X	X	L	H
←Z→				X	X	L	X	L	H
←Z→				X	X	X	L	L	H

H = HIGH X = DONT CARE
L = LOW Z = ANY INPUT LOW

TRUTH TABLE
(AND-OR-INVERT ONLY)

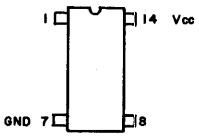
220
Rev A
Sheet 1 of 1

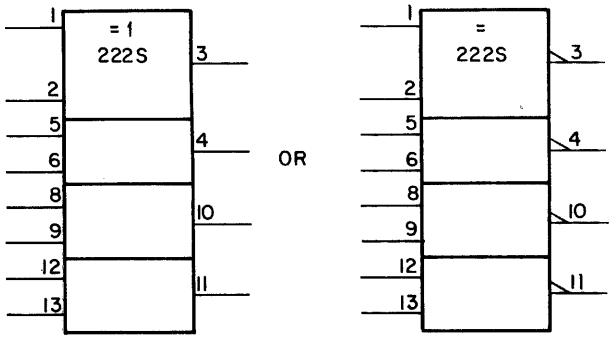
DESCRIPTION

Element 222S is a quad, 2-input, positive Exclusive OR. The 222S may also be used as an equivalence gate for low-active outputs.

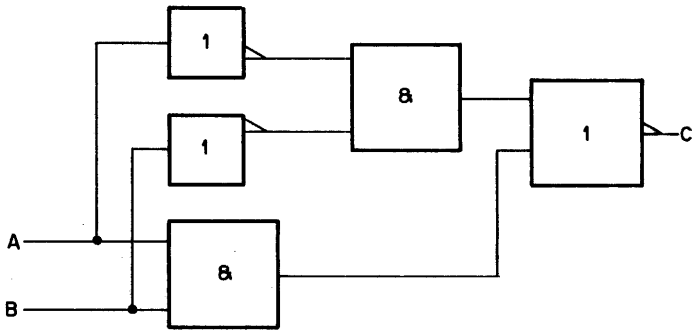
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 82S41
3. Package pin configuration:





LOGIC SYMBOL



FUNCTIONAL DIAGRAM
(ONE SECTION)

A	B	C
0	0	0
1	0	1
0	1	1
1	1	0

TRUTH TABLE

222S
Rev A
Sheet 1 of 1

DESCRIPTION

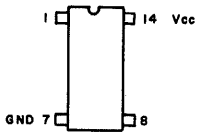
Element 223 is a dual, 2-wide, positive AND-OR-INVERT gate.

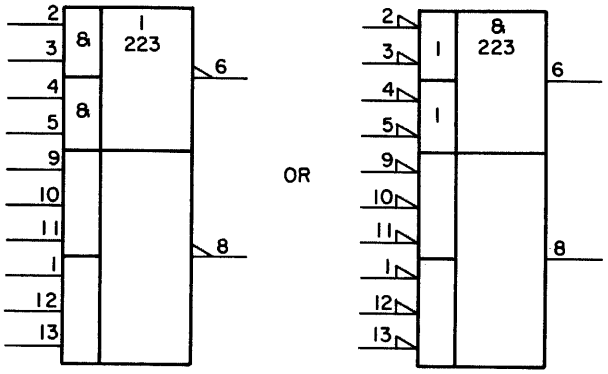
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
223L	74L51
223P	74LS51

3. Package pin configuration:





LOGIC SYMBOL

223
Rev A
Sheet 1 of 1

DESCRIPTION

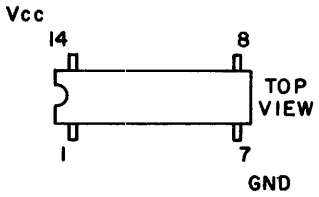
The 224 circuit is a triple, 3-input, positive NOR gate.

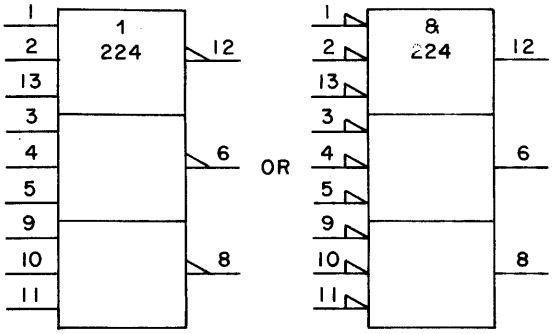
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
224	7427
224LS	74LS27

3. Package pin configuration.





LOGIC SYMBOL

INPUT			OUTPUT
1	2	13	12
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

TRUTH TABLE
(FOR ONE GATE)

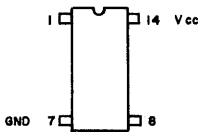
224
Rev C
Sheet 1 of 1

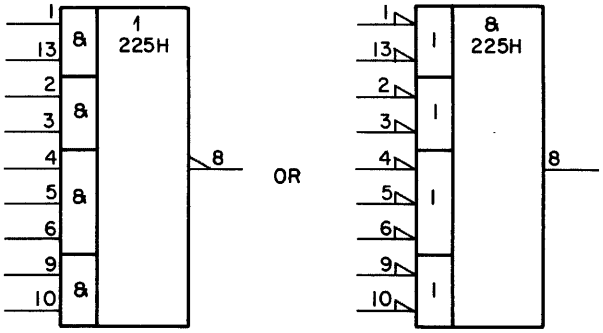
DESCRIPTION

Element 225H is a positive AND-OR-INVERT gate with a 2-2-3-2 input configuration.

NOTES:

1. Vendor identification: 74H54
2. Package pin configuration:





LOGIC SYMBOL

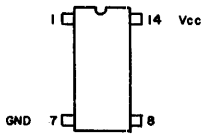
225
Rev A
Sheet 1 of 1

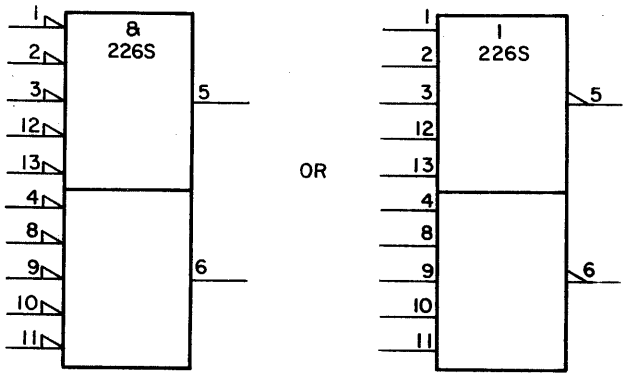
DESCRIPTION

Element 226S consists of two 5-input positive NOR gates.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 74S260
3. Package pin configuration:





LOGIC SYMBOL

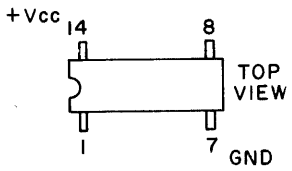
226
Rev A
Sheet 1 of 1

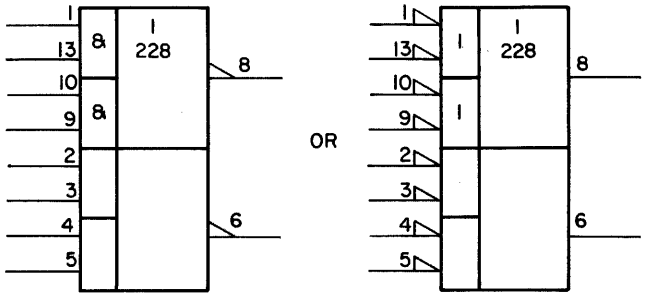
DESCRIPTION

Element 228S is a dual, 2-wide, 2-input AND-OR-INVERT gate.

NOTES:

1. Vendor identification: 74S51
2. Package pin configuration:





LOGIC SYMBOL

228
Rev D
Sheet 1 of 1

DESCRIPTION

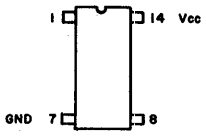
Element 229 consists of four 2-input AND gates with open-collector outputs.

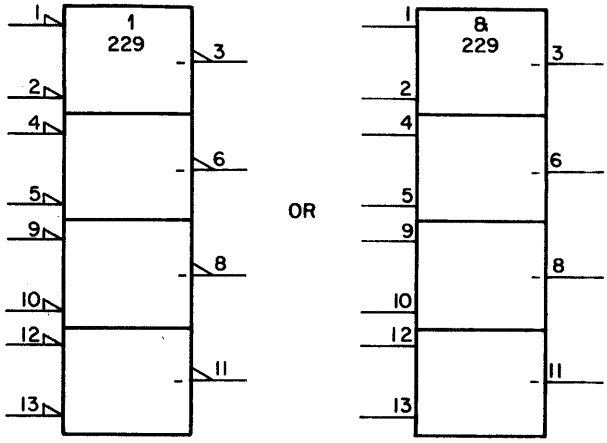
NOTES

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
229LS	74LS09
229S	74S09

3. Package pin configuration:





LOGIC SYMBOL

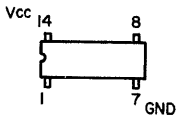
229
Rev A
Sheet 1 of 1

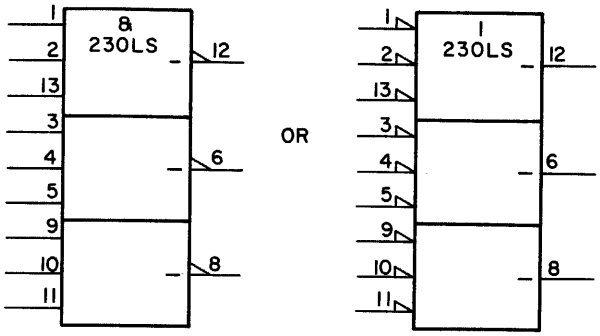
DESCRIPTION

Element 230LS is a triple, 3-input, positive NAND gate with open-collector outputs.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 74LS12
3. Package pin configuration:





LOGIC SYMBOL

230LS
Rev A
Sheet 1 of 1

DESCRIPTION

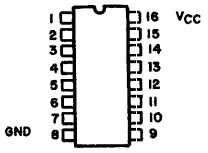
The 242H package consists of two edge-trigered J-K flip-flops with asynchronous set (S) and clear (R) inputs. Data from the J or K inputs is loaded into the FF when the clock is high, and is available at the outputs when the clock goes low.

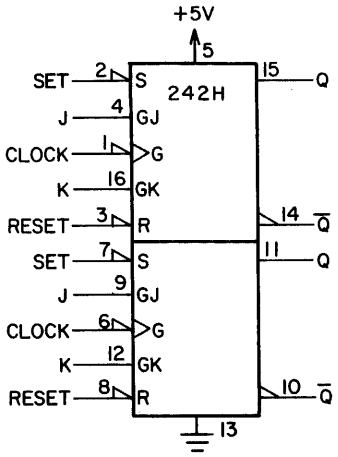
Data at J and K may change while the clock is high, but must be stable for a period of 13 nsec prior to the clock going low.

Data at the S and R inputs will override any clocked data inputs, providing that the S or R data is stable for 2 minimum of 16 nsec.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 74H106
3. Package pin configuration:





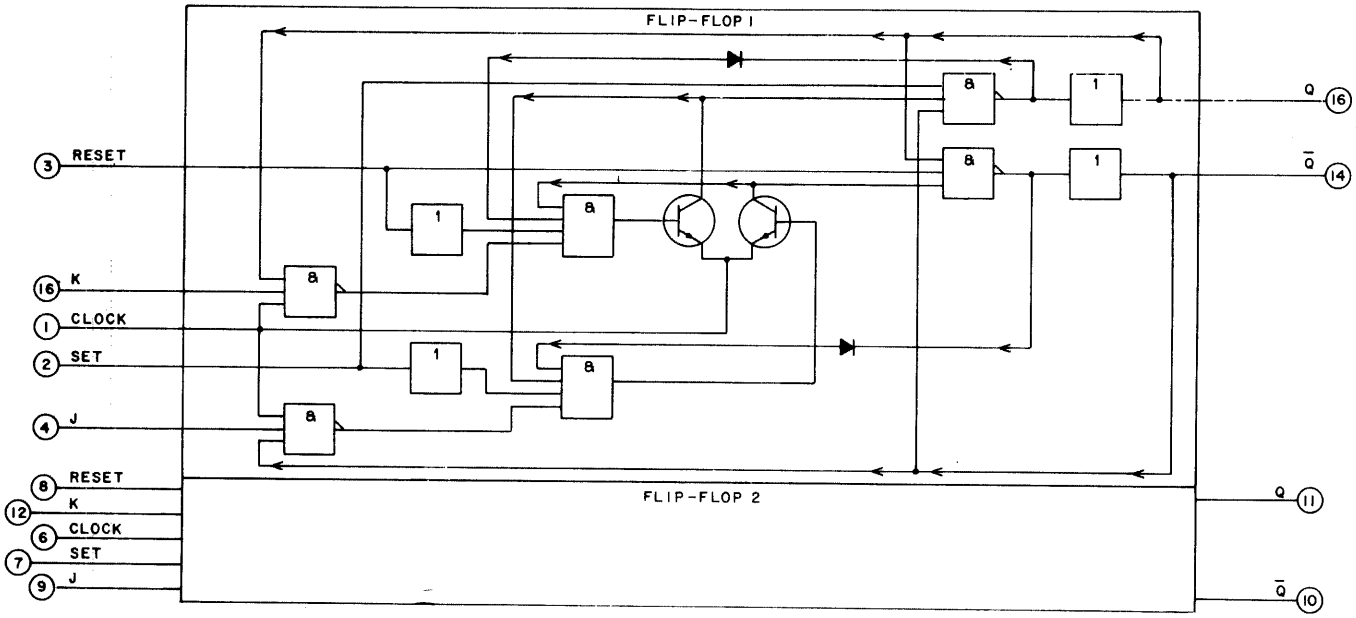
LOGIC SYMBOL

INPUTS		OUTPUT
Tn		Tn + 1
J	K	Q
L	L	Qn
L	H	L
H	L	H
H	H	$\overline{Qn}$

Tn = BIT TIME BEFORE CLOCK PULSE
Tn + 1 = BIT TIME AFTER CLOCK PULSE

TRUTH TABLE

242H
Rev A
Sheet 1 of 2



FUNCTIONAL DIAGRAM

242H
Rev A
Sheet 2 of 2

DESCRIPTION

The 243 package consists of two Schottky-type, edge-triggered flip-flops with asynchronous set (S) and clear (R) inputs. Data from the J and K inputs is loaded into the FF while the clock is high, and is available at the outputs when the clock goes low.

Data at J and K may change while the clock is high, but must be stable during the input set-up time, which is just prior to the clock going low. Typical set-up times are 10 nsec for the 243LS, and 3 nsec for the 243S.

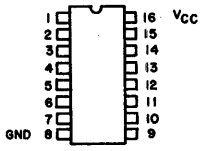
Data at the S and R inputs will override any clocked data (J-K) inputs.

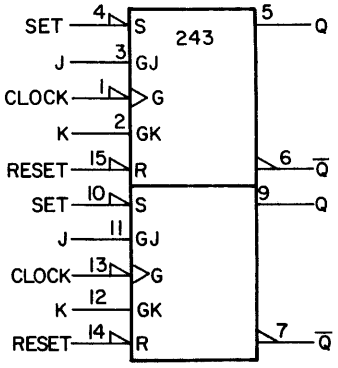
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:
3.

Element	Vendor Number
243LS	74LS112
243S	74S112

3. Package pin configuration:

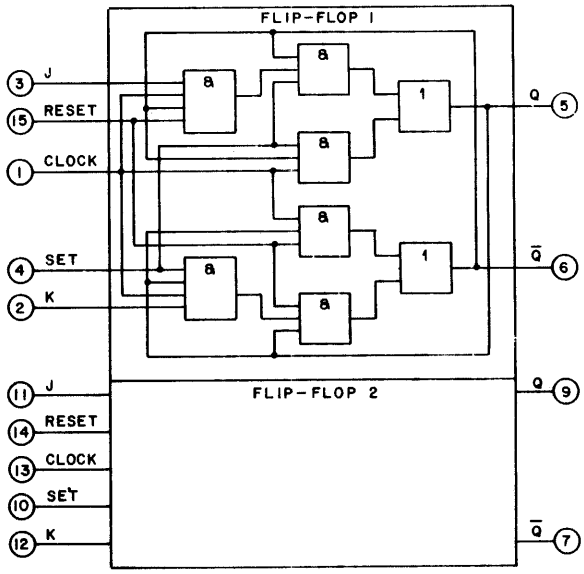




LOGIC SYMBOL

INPUTS		OUTPUT
T_n		T_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

TRUTH TABLE



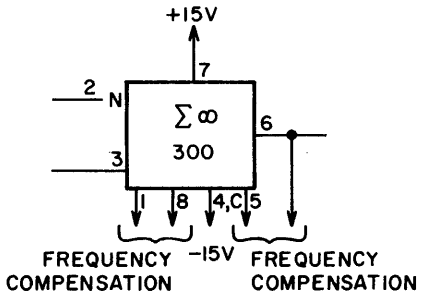
FUNCTIONAL DIAGRAM
(EITHER SECTION)

243
Rev A
Sheet 1 of 1

DESCRIPTION

Element 300 is a high-gain operational amplifier mounted on a single chip.

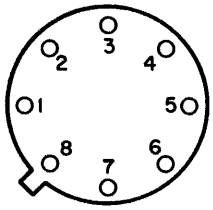
Pin	Function
1	Input Frequency Comp.
2	Inverting Input
3	Non-inverting Input
4	-V (Connected to Case)
5	Output Frequency Comp.
6	Output
7	+V
8	Input Frequency Comp.



LOGIC SYMBOL

NOTE:

1. Vendor Identification: 709C



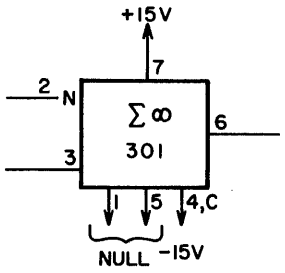
PACKAGE PIN CONFIGURATION

300
Rev. D
Sheet 1 of 1

DESCRIPTION

Element 301 is a frequency compensated, high gain, operational amplifier.

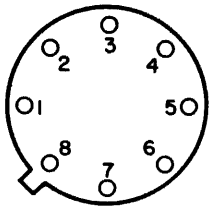
Pin	Function
1	Offset Null
2	Inverting Input
3	Non-inverting Input
4	-V
5	Offset Null
6	Output
7	+V
8	Not Used (no connection)



LOGIC SYMBOL

NOTE:

1. Vendor Identification: 741C



PACKAGE PIN CONFIGURATION

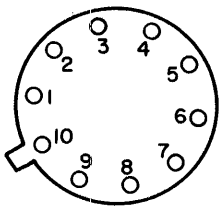
301
Rev. C
Sheet 1 of 1

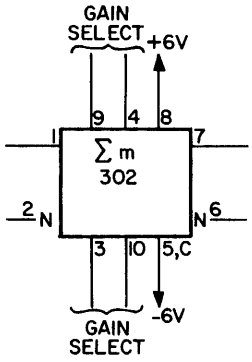
DESCRIPTION

Element 302 is a high performance, wide-band amplifier with differential inputs and outputs. Fixed gains of 100 and 400 are obtained by jumpering gain select pins 3 and 10, or 4 and 9, respectively. A gain of 10 is realized if the four gain select pins are left open. Other gains within this 10-400 range may be obtained by using an external resistor. Emitter-Follower outputs provide low output impedance for driving capacitive loads.

NOTES:

1. Vendor identification: 733C
2. Package pin configuration:
   (pin 5 connects to case)





LOGIC SYMBOL

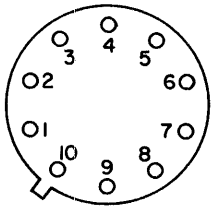
302
Rev B
Sheet 1 of 1

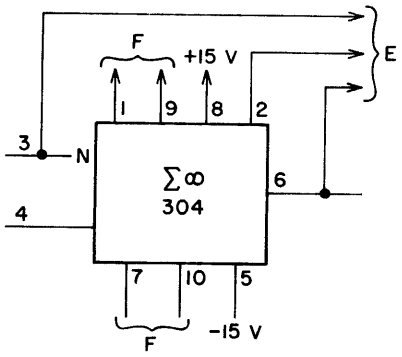
DESCRIPTION

Element 304 is a high-speed, high-gain operational amplifier for use where fast signal acquisition or wide band width is required. The 304 features fast setting time, high slew rate (100 V/μs), low offsets and high output swing for large signal applications.

NOTES:

1. Vendor identification: μA715C
2. Package pin configuration:





E = EXTERNAL COMPONENTS
F = FREQ COMPENSATION

LOGIC SYMBOL

304
Rev A
Sheet 1 of 1

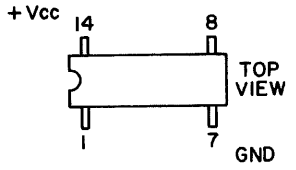
DESCRIPTION

Element 306 is a pair of frequency compensated, high gain, operational amplifier.

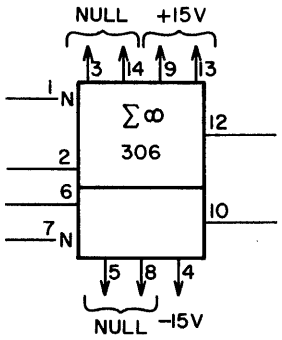
Pin	Function
1	Inverting Input A
2	Non-inverting Input A
3	Offset Null A
4	-V
5	Offset Null B
6	Non-inverting Input B
7	Inverting Input B
8	Offset Null B
9	+V (B)
10	Output B
11	No Connections
12	Output A
13	+V (A)
14	Offset Null A

NOTE:

1. Vendor Identification: 747C



PACKAGE PIN CONFIGURATION



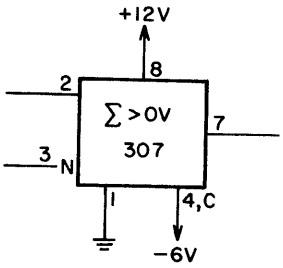
LOGIC SYMBOL

306
Rev. B
Sheet 1 of 1

DESCRIPTION

Element 307 is a differential voltage comparator.

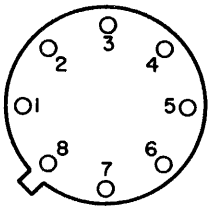
Pin	Function
1	GND
2	Non-inverting Input
3	Inverting Input
4	-V
5	No Connection
6	No Connection
7	Output
8	+V



LOGIC SYMBOL

NOTE:

1. Vendor Identification: 710



PACKAGE PIN CONFIGURATION

307
Rev. C
Sheet 1 of 1

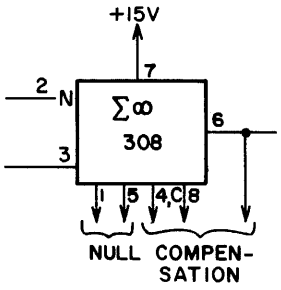
DESCRIPTION

Element 308 is a hi-slew-rate operational amplifier.

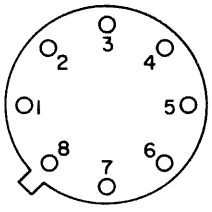
Pin	Function
1	Offset Null
2	Inverting Input
3	Non Inverting Input
4	V-
5	Offset Null
6	Output
7	V+
8	Frequency Compensation

NOTES:

1. Vendor identification: 531T



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

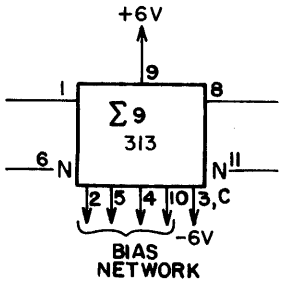
308
Rev C
Sheet 1 of 1

DESCRIPTION

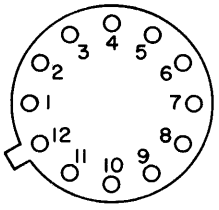
Element 309 is a wide-band differential amplifier with a nominal voltage gain of 9.

NOTES:

1. Vendor identification: 3001



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

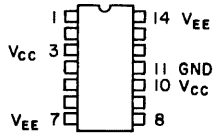
309
Rev C
Sheet 1 of 1

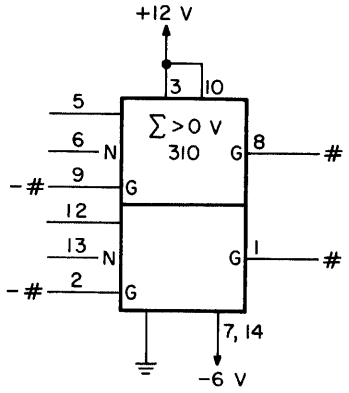
DESCRIPTION

Element 310 is a dual differential-voltage comparator. Maximum common-mode input voltage range is ±7 V. Maximum differential input voltage range is ±5 V. A minimum differential input voltage of 5.0 mV is required to switch the output.

NOTES

1. To show symbol sections separately, duplicate the V_{CC} and V_{EE} pins (2 each) and Ground symbol for each section.
2. Vendor identification: MC1414
3. Package pin configuration:





LOGIC SYMBOL

DIFFERENTIAL INPUT	STROBE (G)	OUTPUT
$V_{ID} \geq 5.0$ mV	L	L
	H	H
-5.0 mV $< V_{ID} < 5.0$ mV	L	L
	H	?
$V_{ID} \leq -5.0$ mV	L	L
	H	L

? = INDETERMINATE OUTPUT

TRUTH TABLE

310
Rev B
Sheet 1 of 1

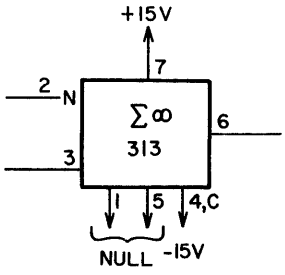
DESCRIPTION

Element 313 is a frequency compensated, high gain, operational applifier.

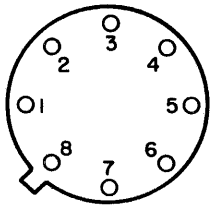
Pin	Function
1	Offset Null
2	Inverting Input
3	Non-inverting Input
4	-V
5	Offset Null
6	Output
7	+V
8	Not Used (no connection)

NOTE:

1. Vendor Identification: 741



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

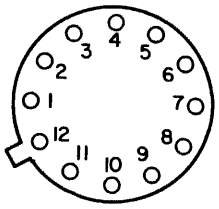
313
Rev. D
Sheet 1 of 1

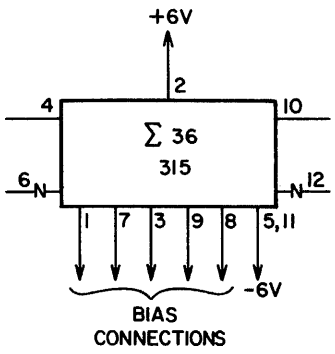
DESCRIPTION

Element 315 is a wide-band amplifier for frequencies up to 200 MHz.

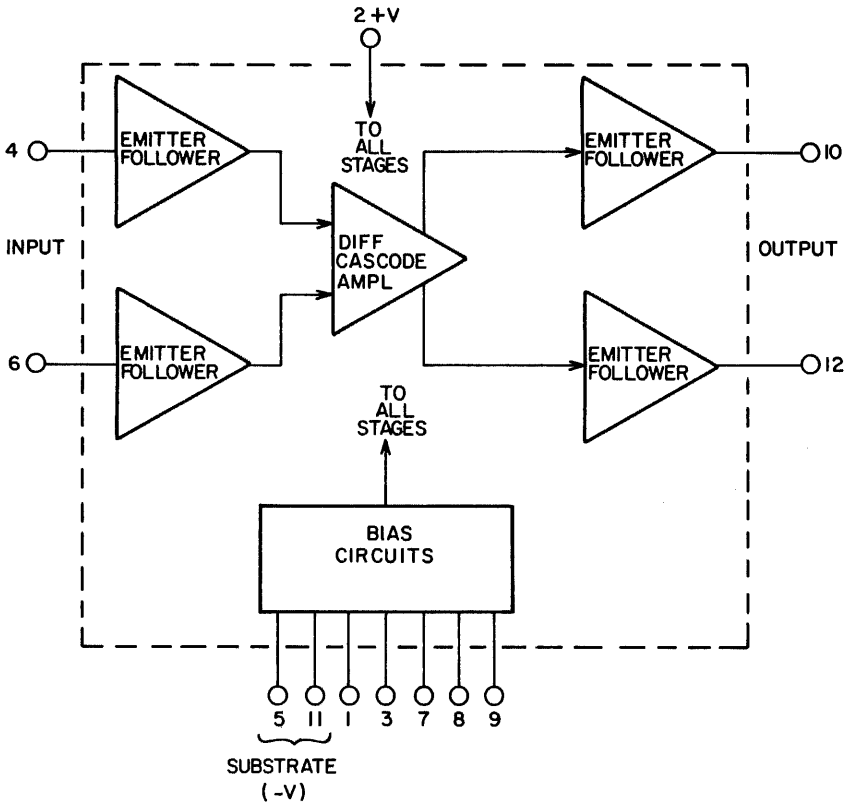
NOTES:

1. Vendor identification: CA3040
2. Package pin configuration:





LOGIC SYMBOL



FUNCTIONAL DIAGRAM

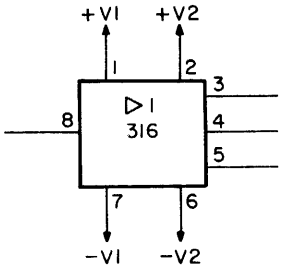
315
Rev A
Sheet 1 of 1

DESCRIPTION

Element 316 is a wide band, unity-gain current amplifier capable of providing peak currents of ±200 mA into a 50-ohm load. The symmetrical class-B output provides a constant low output impedance for both the positive and negative slopes of the output pulses.

Separate connections are provided for + (Vcc) and - (V_{EE}) voltages to both the input and output stages (see electrical schematic diagram). This increases the versatility of operation by allowing a decreased voltage to be applied to the output stage (Q3, Q4), thereby minimizing the power dissipation.

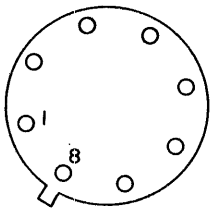
Typical applications: differential input/output op amp, booster amplifier, level shifter, pulse-transformer driver, and transmission-line driver.

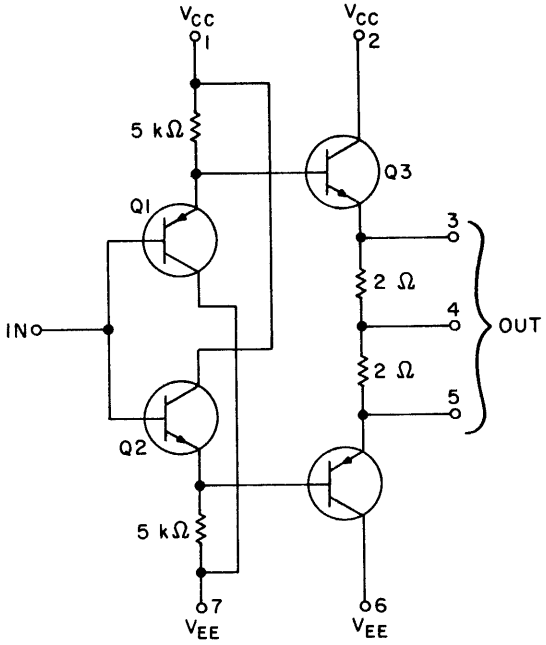


LOGIC SYMBOL

NOTES

1. Vendor identification: LH0002CH
2. Package pin configuration:





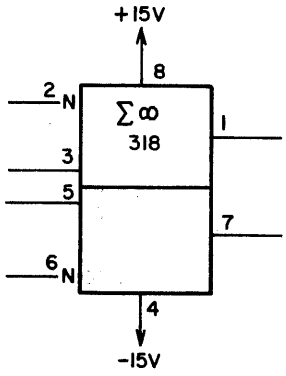
ELECTRICAL SCHEMATIC DIAGRAM

316
Rev B
Sheet 1 of 1

DESCRIPTION

Element 318 is a dual, high-performance operational amplifier.

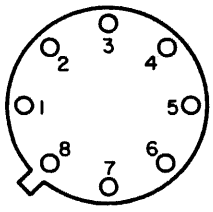
Pin	Function
1	Output A
2	Inverting Input A
3	Non Inverting Input A
4	V-
5	Non Inverting Input B
6	Inverting Input B
7	Output B
8	V+



LOGIC SYMBOL

NOTES:

1. Vendor identification: 72558



PACKAGE PIN CONFIGURATION

318
Rev B
Sheet 1 of 1

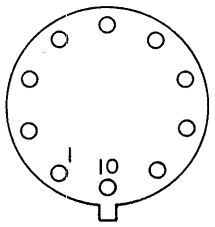
DESCRIPTION

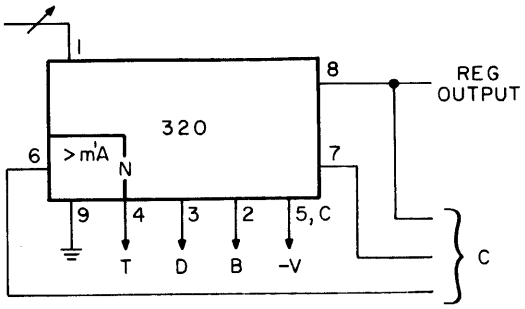
The 320 circuit is a negative voltage regulator that can be programmed by an external resistor to provide any voltage from -40 V to 0 V while operating from a single unregulated supply. Regulation is 1 mV, no load to full load. The full-load current of 25 mA can be increased by adding external transistors.

See page 320-2 for typical applications.

NOTES:

1. Vendor identification: LM304
2. Package pin configuration: (pin 10 is unused)

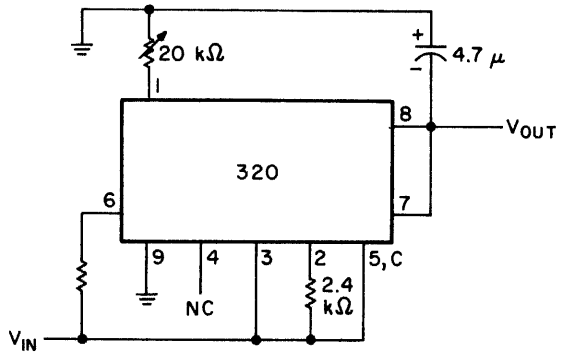




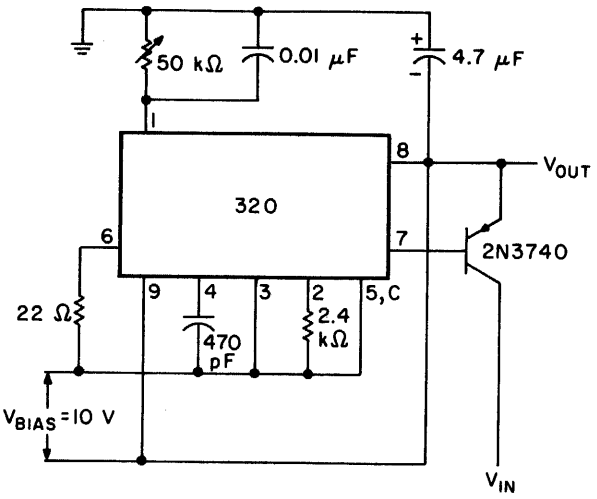
T = TERMINATION
D = DIVIDER COMPONENTS
B = BIAS CIRCUIT (REFERENCE VOLTAGE)
-V = UNREGULATED INPUT
C = CURRENT MONITOR
REPLACE m WITH NOMINAL VOLTAGE AS DETERMINED BY D
REPLACE m' WITH NOMINAL CURRENT AS DETERMINED BY C

LOGIC SYMBOL

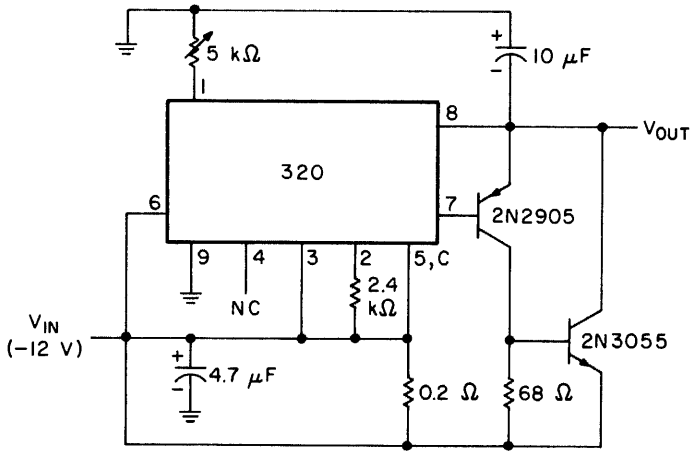
320
Rev B
Sheet 1 of 2



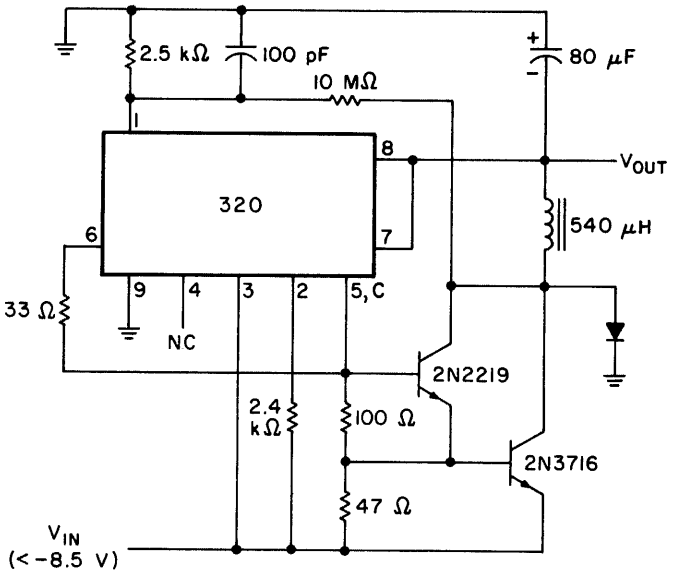
BASIC REGULATOR



SEPARATE BIAS SUPPLY



HIGH-CURRENT REGULATOR



SWITCHING REGULATOR

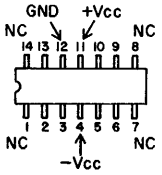
320
Rev B
Sheet 2 of 2

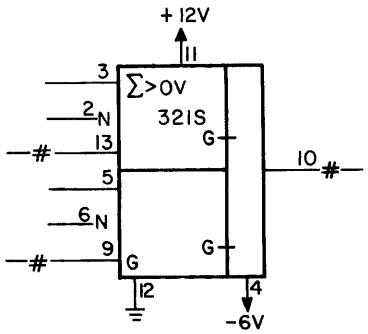
DESCRIPTION

The 321S is a dual differential comparator. Output (pin 10) is high when either pin 2 is at a lower potential than pin 3 and pin 13 is high, or pin 6 is at a lower potential than pin 5 and pin 9 is high. A low level to pin 9 or 13 will inhibit operation of that section.

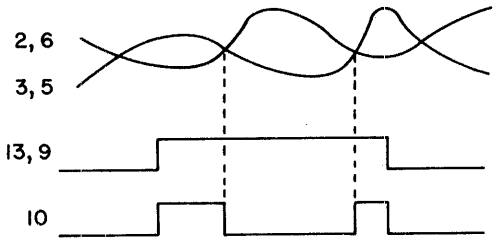
NOTES:

1. Vendor identification: TSC 5711
2. Package pin configuration.





LOGIC SYMBOL



FUNCTION SEQUENCE

321
Rev D
Sheet 1 of 1

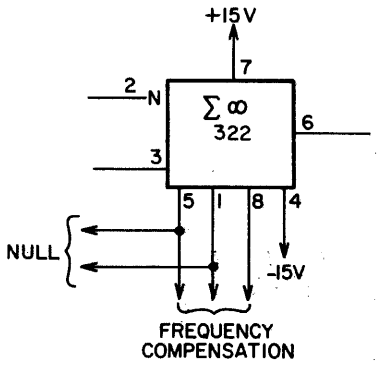
DESCRIPTION

Element 322 is a frequency compensated, high speed, operational amplifier.

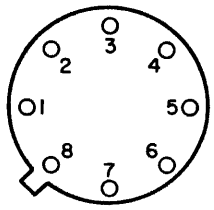
Pin	Function
1	Offset Null/Compensation 1
2	Inverting Input
3 3	Non-inverting Input
4	-V
5	Offset Null/Compensation 3
6	Output
7	+V
8	Compensation 2

NOTE:

1. Vendor Identification: LM318



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

322
Rev. B
Sheet 1 of 1

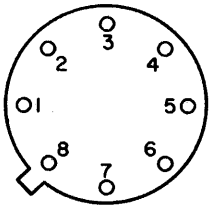
DESCRIPTION

The 324 circuit is a dual, internally compensated, high-performance operational amplifier.

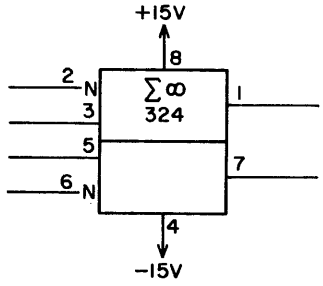
Pin	Function
1	Output A
2	Inverting Input A
3	Non-inverting Input A
4	V_{EE}
5	Non-inverting Input B
6	Inverting Input B
7	Output B
8	V_{CC}

NOTE:

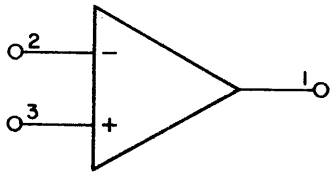
Vendor Identification: MC1458/N5558



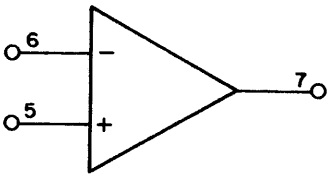
PACKAGE PIN CONFIGURATION



LOGIC SYMBOL



SECTION A



SECTION B

FUNCTION DIAGRAM

324
Rev C
Sheet 1 of 1

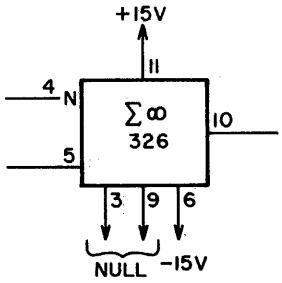
DESCRIPTION

Element 326 is a high-gain operational amplifier.

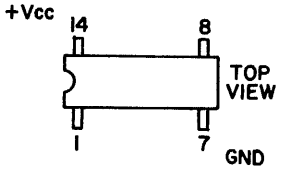
Pin	Function
1	No Contact
2	No Contact
3	Offset Null
4	Inverting Input
5	Non-Inverting Input
6	V-
7	No Contact
8	No Contact
9	Offset Null
10	Output
11	V+
12	No Contact
13	No Contact
14	No Contact

NOTE:

1. Vendor Identification: 741C



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

326
Rev. C
Sheet 1 of 1

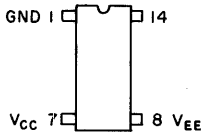
DESCRIPTION

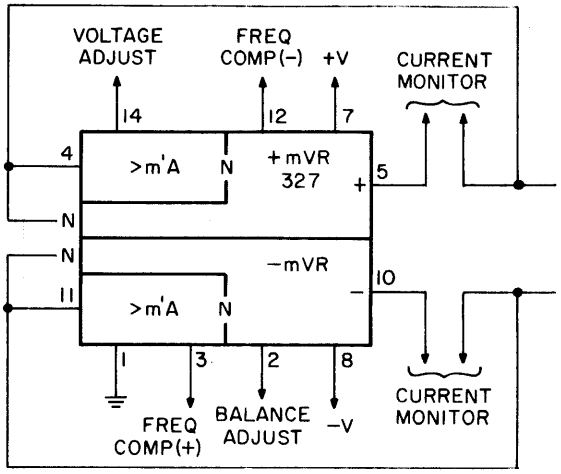
Element 327 is a dual-polarity voltage regulator for providing balanced positive and negative output voltages at currents up to 100 mA. Internally, the device is set for ±15 V outputs, but voltage and balance pins permit simultaneous adjustments from 8 to 20 volts. Input voltages up to ±30 V can be used, and current monitor connections provide for adjustable current limiting.

For typical applications, see page 327-2.

NOTES

1. Vendor identification: MC1468L
2. Package pin configuration

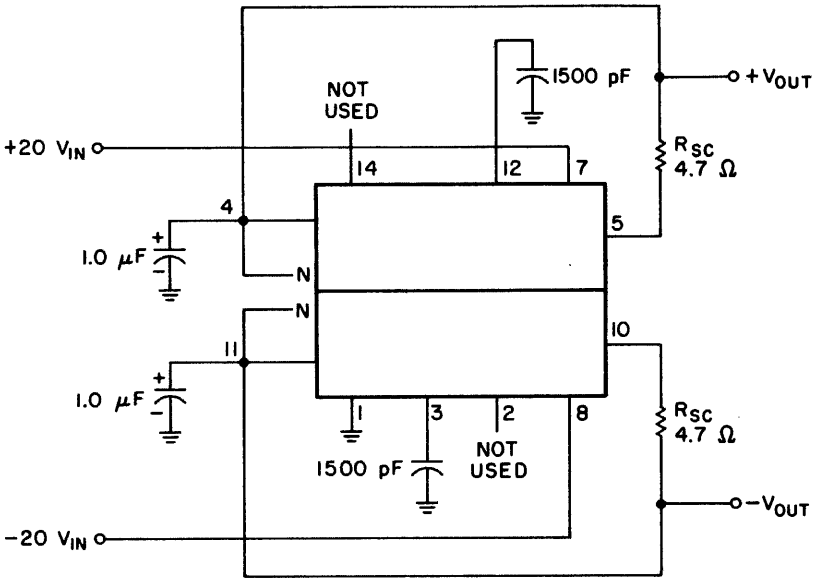




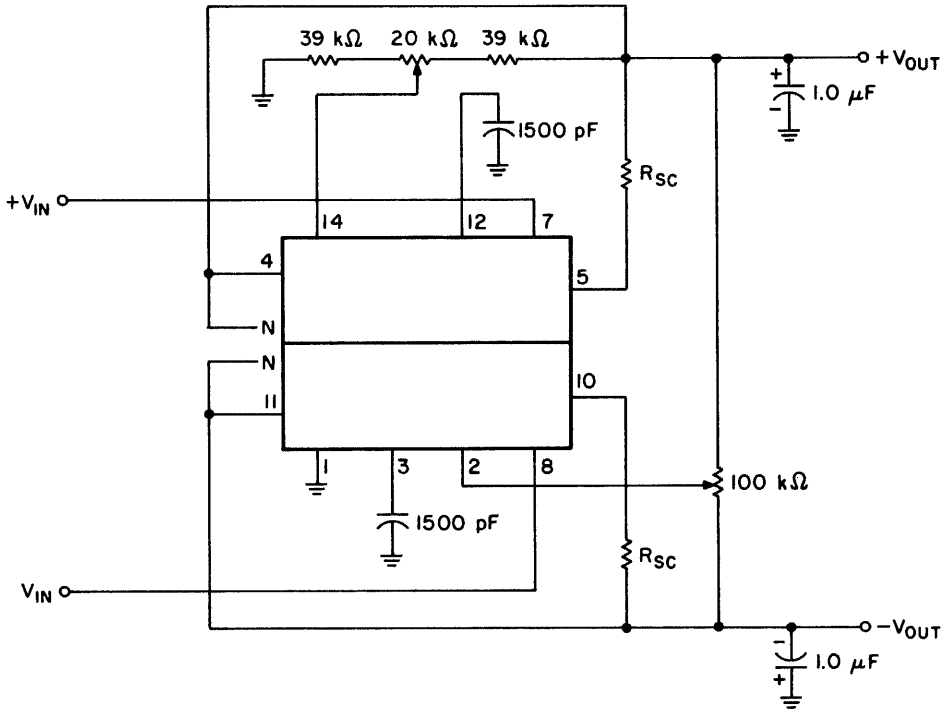
REPLACE m WITH NOMINAL VOLTAGE AS DETERMINED BY VOLTAGE AND BALANCE ADJUST COMPONENTS.
REPLACE m' WITH NOMINAL CURRENT AS DETERMINED BY CURRENT MONITOR COMPONENTS.

LOGIC SYMBOL

327
Rev B
Sheet 1 of 2



BASIC 50 mA REGULATOR



VOLTAGE ADJUST/BALANCE CIRCUIT

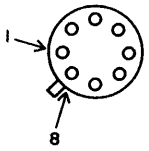
327
Rev B
Sheet 2 of 2

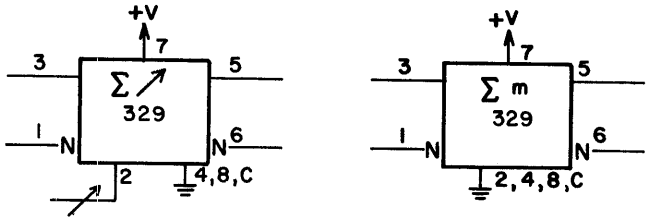
DESCRIPTION

The 329 circuit is a wide-band RF/IF/Audio amplifier with external AGC control.

NOTES:

1. Vendor identification: 1590
2. Package pin configuration. (TO-99 metal case)





LOGIC SYMBOL

329
Rev C
Sheet 1 of 1

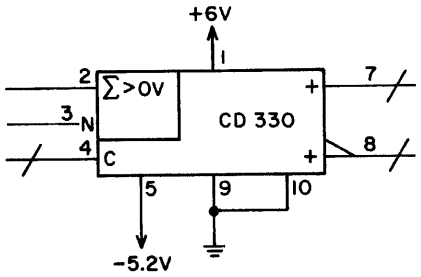
DESCRIPTION

The 330 circuit is a differential voltage comparator. The circuit has differential analog inputs and complementary logic outputs compatible with ECL. A latch function allows the comparator to be used in a sample-hold mode. If the latch enable input is high, the comparator functions normally. When the latch enable goes low, the comparator outputs are locked in their existing logical states.

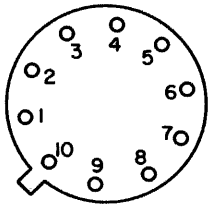
Pin	Function
1	+V
2	Non-inverting Input
3	Inverting Input
4	Latch Enable
5	-V
6	No Connection
7	Q Output
8	$\overline{Q}$ Output
9	GND
10	GND

NOTE:

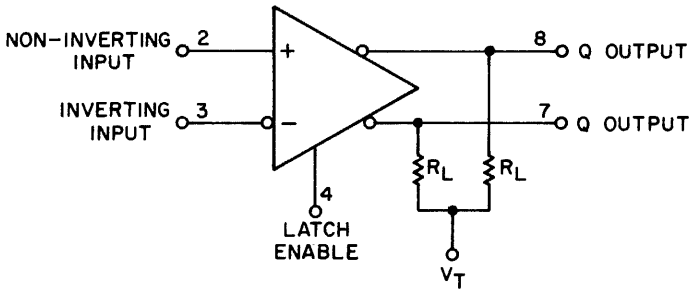
1. Vendor identification: AM685



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION



FUNCTION DIAGRAM

330
Rev A
Sheet 1 of 1

DESCRIPTION

Element 331A is a dual-polarity tracking voltage regulator that provides balanced or unbalanced positive and negative output voltages at currents up to 200 mA. A single external resistor adjustment changes both outputs between the limits of ±50 mV and ±42 V. The 331A comes in a 9-pin (type H) "top hat" package that can dissipate up to 3 W.

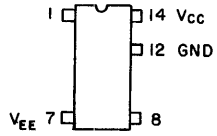
Element 331 is similar to the 331A, except that it comes in a 14-pin DIP that can dissipate up to 900 mW.

NOTES

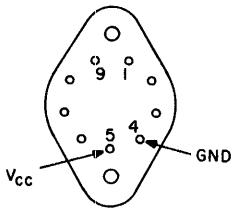
1. Vendor identification:

Element	Vendor Number
331	RC4194D
331A	RC4194TK

2. Package pin configuration:

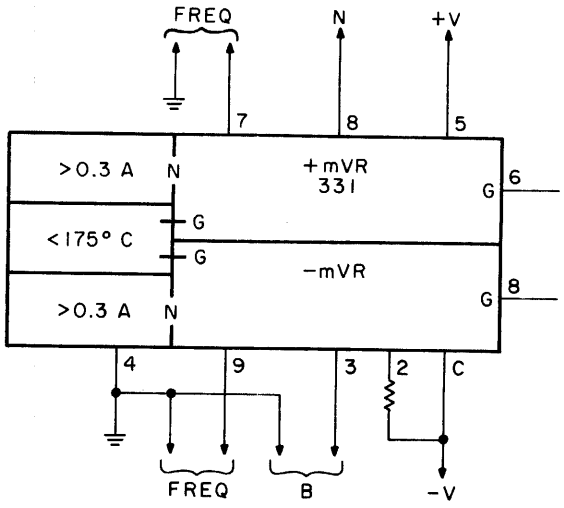


331



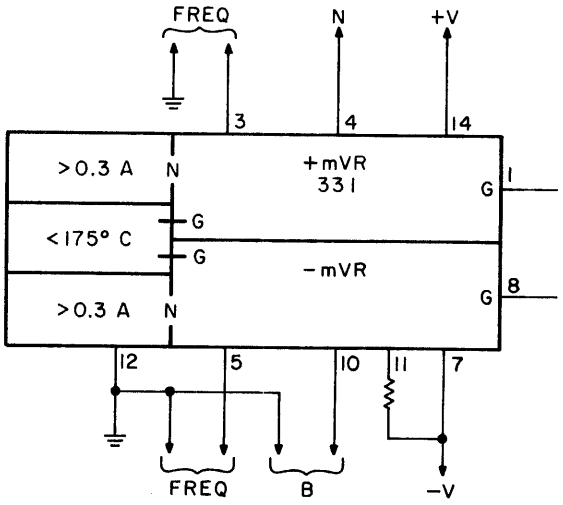
331A

331A



OR

331



REPLACE m WITH NOMINAL VOLTAGE AS DETERMINED BY BIAS (B) AND BALANCE (N) COMPONENTS

LOGIC SYMBOL

331
Rev B
Sheet 1 of 1

DESCRIPTION

The 332 and 353 circuits are positive voltage regulators. Output voltage is adjustable from 4.5 to 40 volts. The full-load output current of the 332 is 45 mA, that of the 353 is 25 mA. Either of these may be increased in excess of 10A by using an external pass transistor.

The 332 comes in an 8-pin metal can, the 353 in an 8-pin DIP.

Pin	Function
1	Current Limit
2	Booster Output
3	Unregulated Input
4	Ground
5	Reference Bypass
6	Feedback
7	Compensation
8	Regulated Output

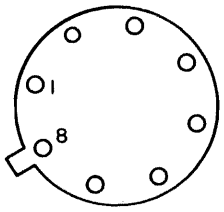
NOTES

1. Vendor identification:

Element	Vendor Number
332	LM305A
353	LM376

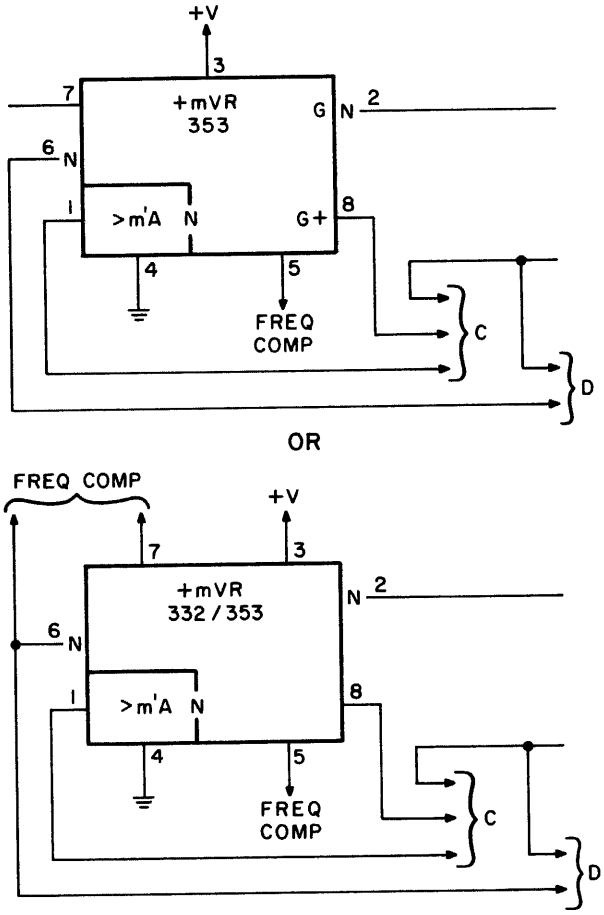
2. Package pin configurations:

353



PIN 4 CONNECTED TO CASE

332



REPLACE m WITH NOMINAL VOLTAGE AS DETERMINED BY D DIVIDER.
REPLACE m' WITH NOMINAL CURRENT AS DETERMINED BY C.

LOGIC SYMBOL

332/353
Rev A
Sheet 1 of 1

DESCRIPTION

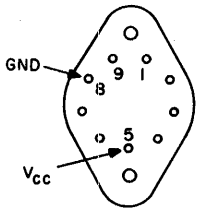
Element 333 is a dual-polarity tracking voltage reulator that provides balanced positive and negative 15 V outputs at currents up to 100 mA. The type-H packaging permits heat dissipation of up to 2.4 W.

The 333 circuit may also be used as a single-output regulator with up to +50 V output, where:

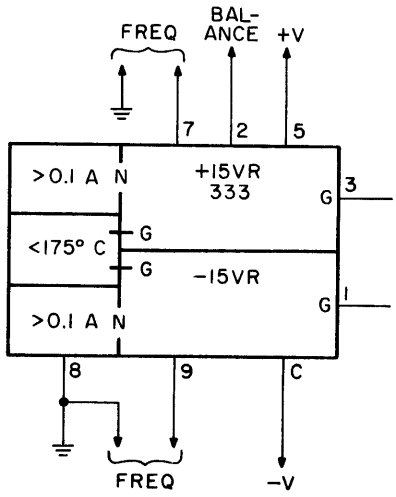
(V out +3 V) <V in <60 V

NOTES

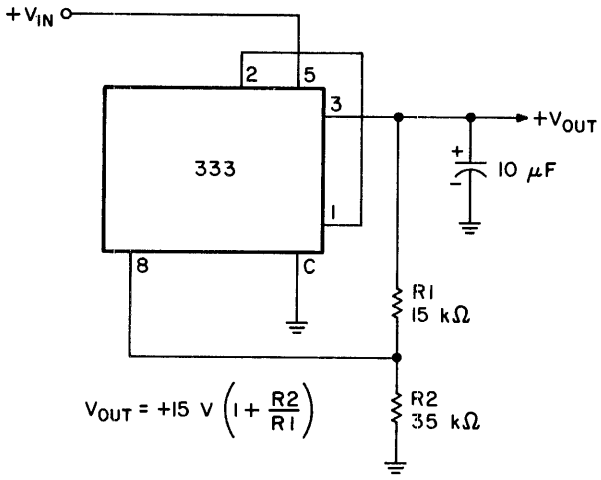
1. Vendor identification: RC1495TK
2. Package pin configuration:



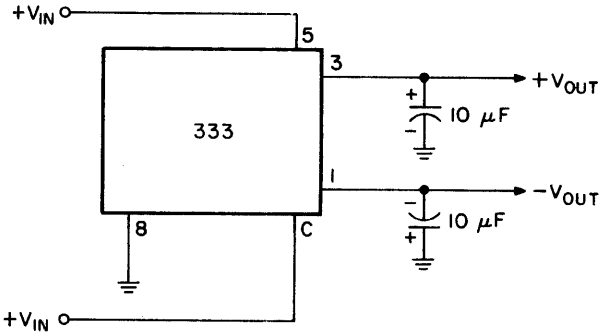
V_{EE} CONNECTED TO CASE



LOGIC SYMBOL



SINGLE +50 V OUTPUT
($I_O \leq 100$ mA)



BALANCED OUTPUT
($\pm I_O \leq 100$ mA)

TYPICAL APPLICATIONS

333
Rev B
Sheet 1 of 1

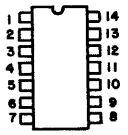
DESCRIPTION

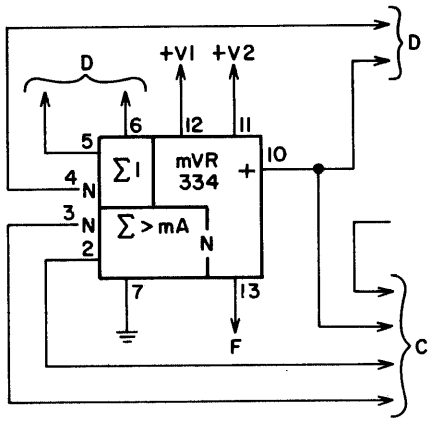
The 334 circuit is a monolithic voltage regulator. Internal circuitry consists of a voltage reference, a differential error amplifier, and a series pass transistor. Typical applications for this device are shown in figures A and B on page 334-2.

Pin	Function
1	No Connection
2	Current Limit
3	Current Sense
4	Inverting Input
5	Non-inverting Input
6	Voltage Reference
7	Ground
8	No Connection
9	Not Used
10	+V out
11	+V1 (V_C)
12	+V2 (V_{CC})
13	Compensation
14	No Connection

NOTES:

1. Vendor identification: MC1723C
2. Package pin configuration:





C=CURRENT MONITOR COMPONENTS
D=DIVIDER COMPONENTS
F=FREQUENCY COMPENSATION COMPONENTS

	Nom.	Min.	Max.	Units
Output Current			150	mA
Input Voltage Range		9.5	40.0	V
Output Voltage Range		2.0	37.0	V
Load Regulation*		0.03	0.2	%VO
Reference Voltage	7.15	6.8	7.5	V
In/Out Voltage Differential		3.0	38.0	V

* IL = 1 mA to 50 mA

LOGIC SYMBOL

334
Rev B
Sheet 1 of 2

Typical Application:

Figure A provides an output current up to 150 mA. For higher currents, figure B is substituted, using an extermal transistor to source the high current. Here, the series output resistor, RSC, senses the output current. Output voltage is applied to one input (pin 4) of the error amplifier. Resistors R1 and R2 drop the internal reference voltage to the desired output reference voltage, which is applied to the other error amplifier input (pin 5).

In this example, the output voltage is compared with the output reference voltage. Any difference voltage is amplified, and the resulting regulator output drives the series pass transistor in direct proportion to the output load. If the current limit is reached, the output current remains constant, and the output voltage decreases for a greater load. Capacitor 'C' provides for frequency compensation.

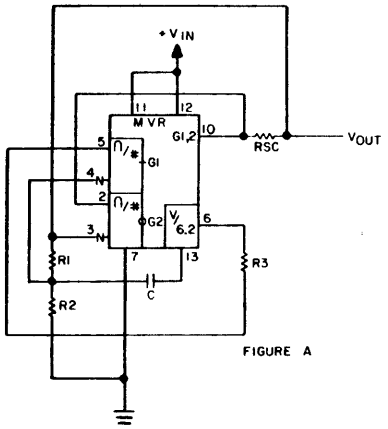


FIGURE A

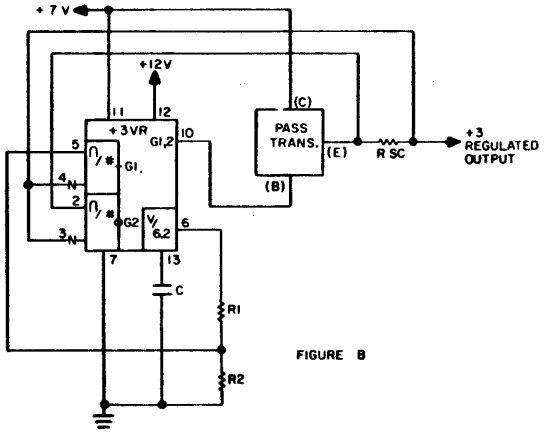


FIGURE B

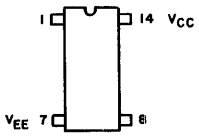
334
Rev A
Sheet 2 of 2

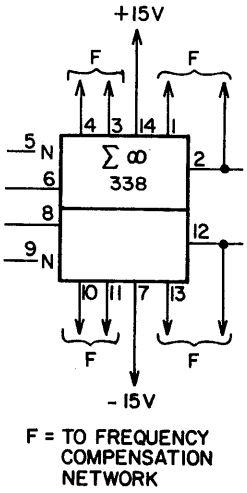
DESCRIPTION

Element 338 is a dual high-gain operational amplifier.

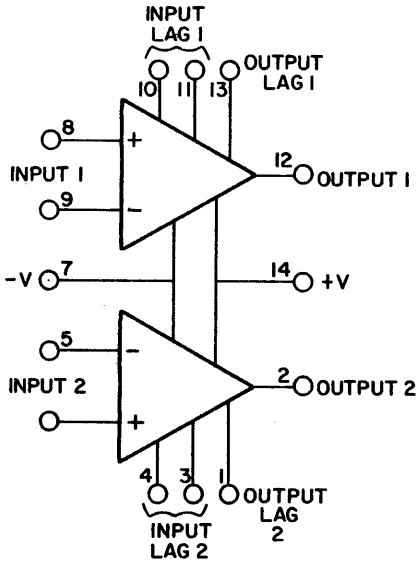
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: MC1437
3. Package pin configuration:



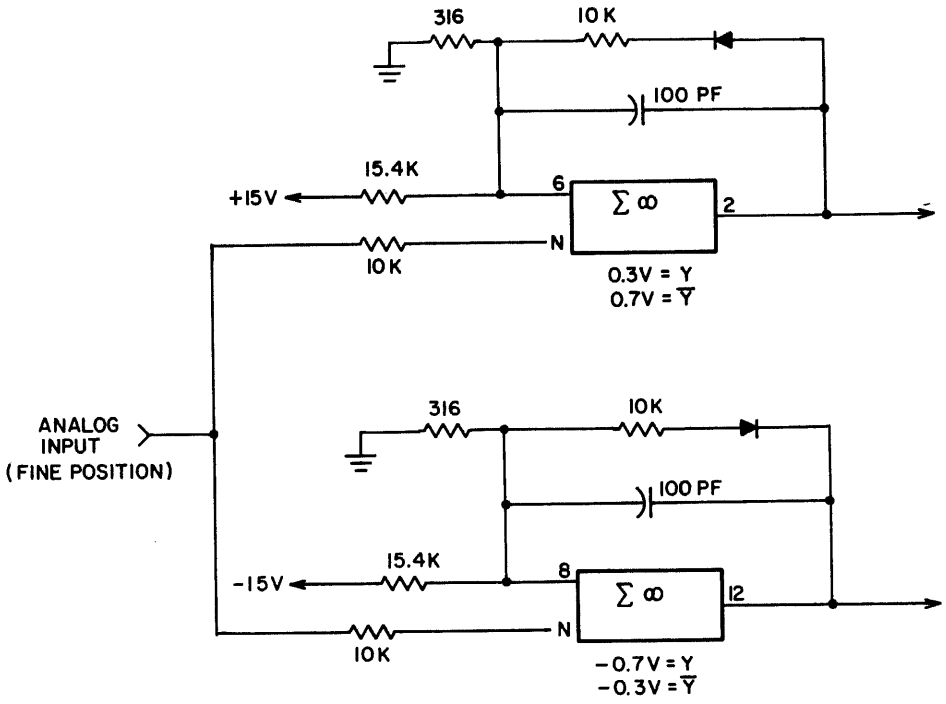


LOGIC SYMBOL



EQUIVALENT CIRCUIT

338
Rev A
Sheet 1 of 2



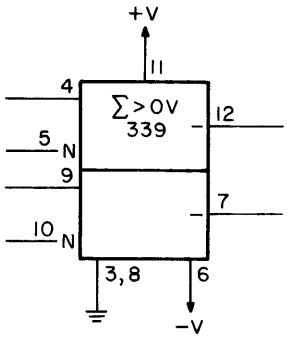
TYPICAL APPLICATION

338
Rev A
Sheet 2 of 2

DESCRIPTION

Element 339 consists of two high-speed voltage comparators in one package. Each section provides an open-collector output capable of driving lamps or relays requiring up to 25 mA. Inputs and outputs can be isolated from system ground.

The 339 can operate from a single +5 V supply, or from ± supplies with a total potential difference of up to 36 V. Maximum differential input voltage is ±5 V.



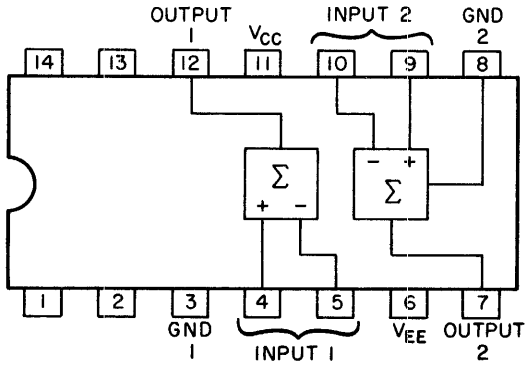
LOGIC SYMBOL

NOTES

1. If sections appear separately, the supply-voltage pins are repeated as needed and only the applicable ground pin is shown for each section.

2. Vendor identification: LM319

3. Package pin configuration and functional diagram:



339

339
Rev B
Sheet 1 of 1

DESCRIPTION

Element 340 is a high-performance operational amplifier with high open-loop gain, high common-mode range, internal frequency compensation, and exceptional temperature stability. Internal short-circuit protection allows for nulling of the offset voltage.

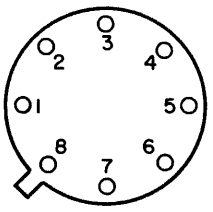
NOTES:

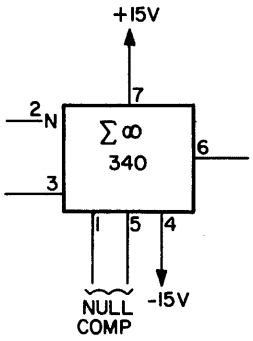
1. Vendor identification:

Element	Vendor Number
340	741C
340A	741S

2. Package pin configuration:

(pin 8 not connected)





LOGIC SYMBOL

340
Rev B
Sheet 1 of 1

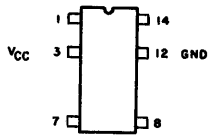
DESCRIPTION

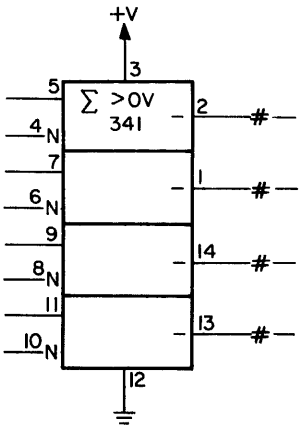
Element 341 consists of four independent precision voltage comparators, each having an offset voltage specification as low as 2 mV, maximum. The 341 interfaces directly with TTL and CMOS. Operating range is +2 V dc to +36 V dc, or ±1 V dc to ±18 V dc. Current drain (0.8 mA) is independent of supply voltage.

The input common-mode voltage range includes ground, even when operating from a single po power supply.

NOTES:

1. Sections may appear separately (V_{CC} and GND connections repeated).
2. Vendor identification: LM339
3. Package pin configuration:





LOGIC SYMBOL

341
Rev A
Sheet 1 of 1

DESCRIPTION

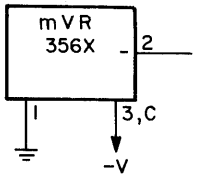
Element 356 is a negative-voltage regulator. Output currents in excess of 1A can be delivered with adequate heat sinking. Thermal overload and short circuit protection is provided internally, and "safe area" compensation at the output reduces the short-circuit as the voltage across the pass transistor is increased.

NOTES:

1. Vendor identification:

Element	Vendor Number
356A	MC7905C/LM320T-5
356B	MC7905.2C/LM320T-5.2
356C	MC7912C/LM320T-12
356D	MC7915C/LM320T-15

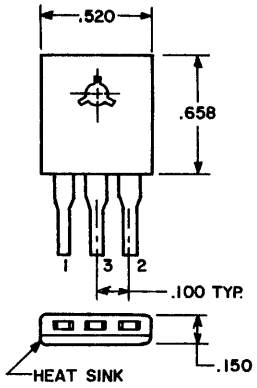
2. Package pin configuration:
   (heat sink connected to pin 3)



Replace 'm' in qualifying symbol according to the value in parentheses below for the element used:

356A (-5)
356 B (-5.2)
356 C (-12)
356 D (-15)

LOGIC SYMBOL



T0220

356
Rev A
Sheet 1 of 1

DESCRIPTION

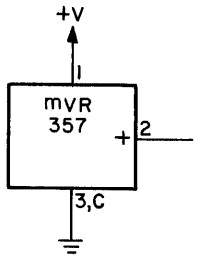
Element 357 is a positive-voltage regulator featuring internal current limiting, thermal shutdown, and safe-area compensation. Output currents in excess of 1A are possible with adequate heat sinking.

NOTES:

1. Vendor identification:

Element	Vendor Number
357A	7805C/LM340T+5
357B	7806C/LM340T+6
357C	7808C/LM340T+8
357D	7812C/LM340T+12
357E	7815C/LM340T+15
357F	7818C/LM340T+18
357E	7824C/LM340T+24

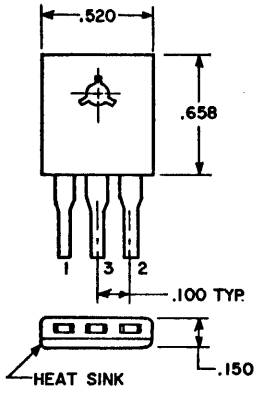
2. Package pin configuration:
   (heat sink connected to pin 3)



Replace 'm' in qualifying symbol according to the value in parentheses below for the element used:

357A (+5)
357B (+6)
357C (+8)
357D (+12)
357E (+15)
357F (+18)
357G (+24)

LOGIC SYMBOL



TO220

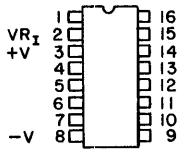
357
Rev A
Sheet 1 of 1

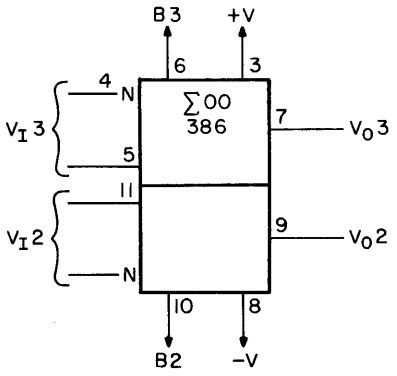
DESCRIPTION

Element 386 consists of three independent operational transconductance amplifiers and an independent bias regulator. Maximum potential between +V and -V pins is 14 volts. Typical common-mode input voltage range is +4.6 to -5.2 volts.

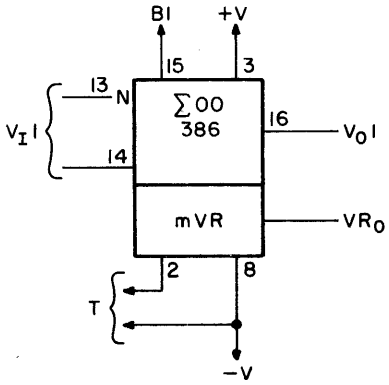
NOTES

1. Vendor identification: CA3060AD
2. Package pin configuration:





AND



B=BIAS COMPONENTS
T=TERMINATION COMPONENTS
m=-V + 7 V

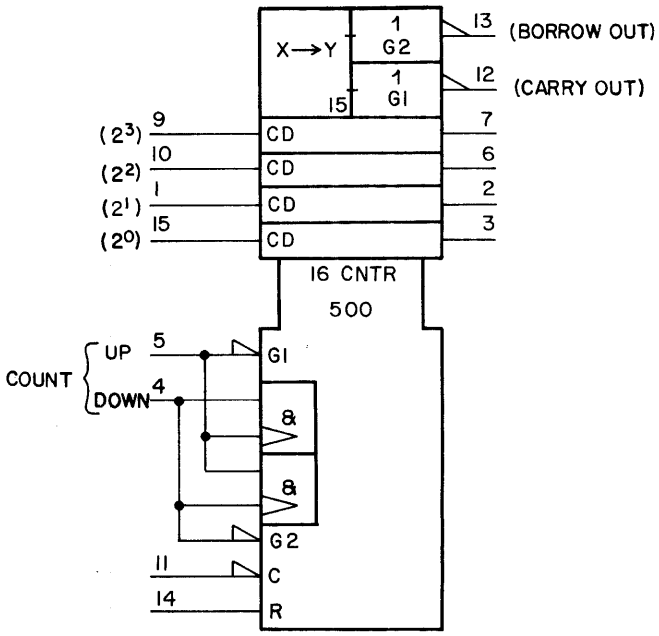
LOGIC SYMBOL

386
Rev B
Sheet 1 of 1

DESCRIPTION

The 500 circuit is a synchronous 4-bit up/down counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

The counter is fully programmable; that is, the counter may be preset to any state by entering the desired data at the data inputs while the load input (pin 11) is low. The output will then change to agree with the data inputs independently of the count pulses. A high level applied to the clear input forces all outputs to the low level. The clear function is independent of the count and load inputs.



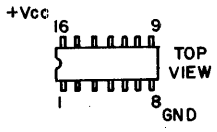
LOGIC SYMBOL

NOTES:

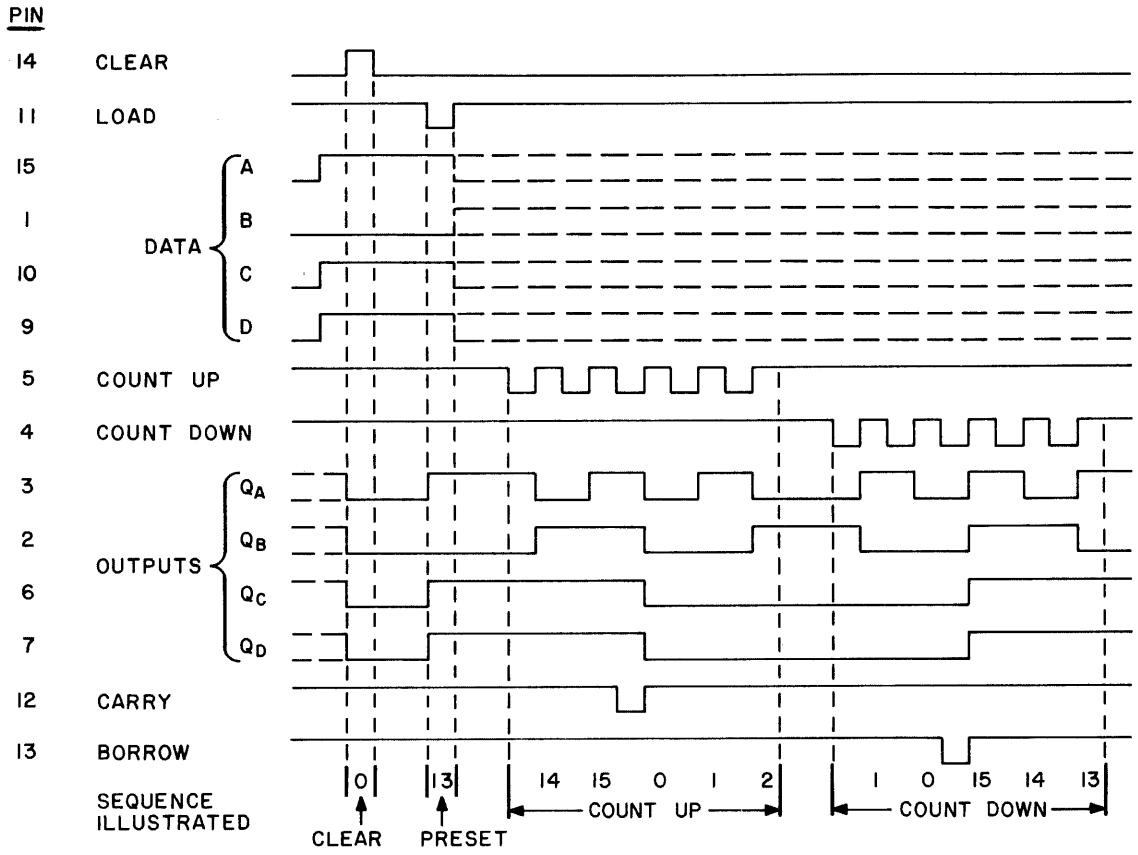
1. Input/Output identifiers are not part of the symbol.
2. Vendor identification:

Element	Vendor Number
500	74193,9366
500LS	74LS193

3. Package pin configuration.



500
Rev B
Sheet 1 of 3



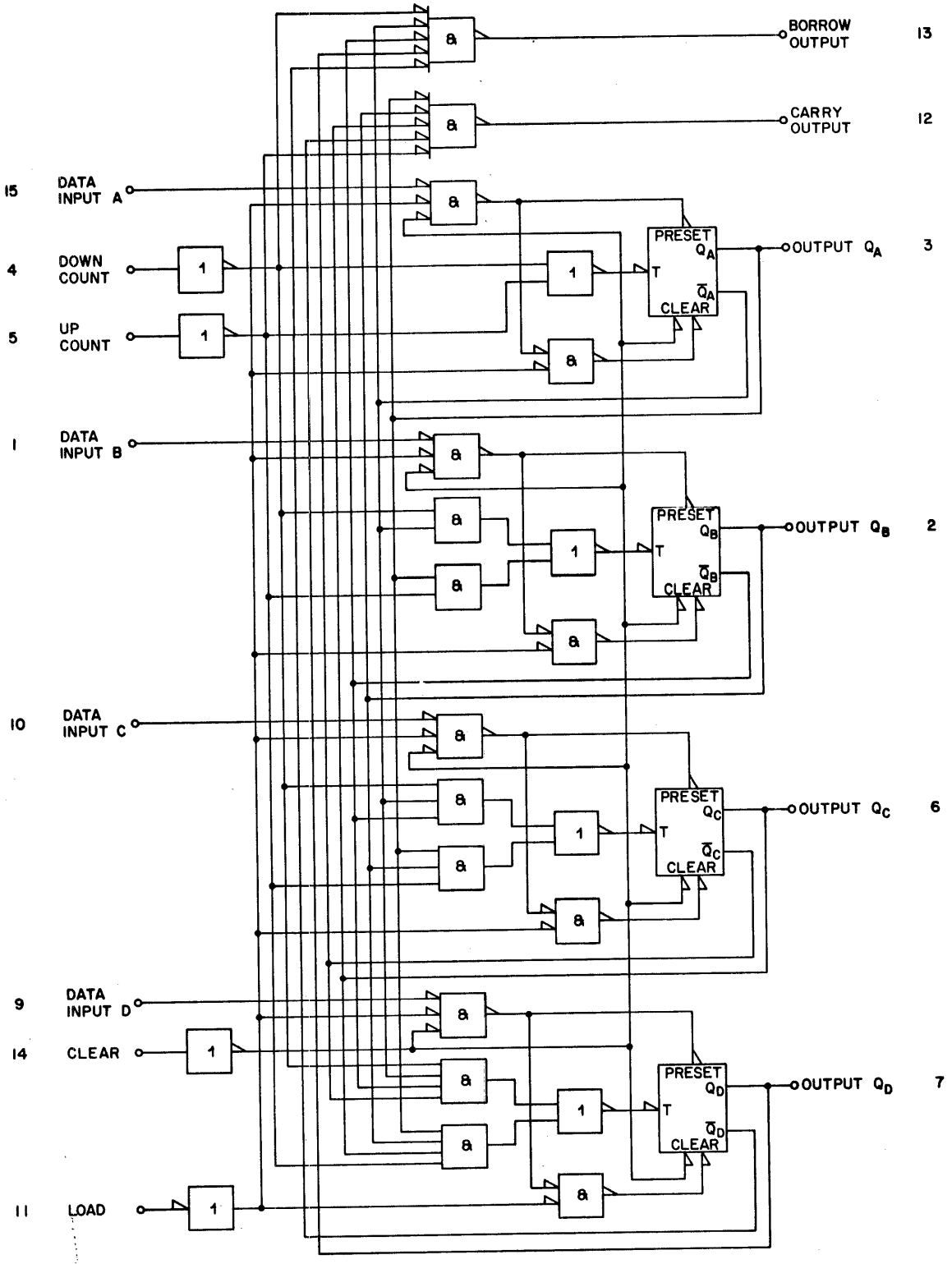
NOTE:

① ILLUSTRATED ABOVE IS THE FOLLOWING SEQUENCE:

1. CLEAR OUTPUTS TO ZERO.
2. LOAD (PRESET) TO BCD THIRTEEN.
3. COUNT UP TO FOURTEEN, FIFTEEN, CARRY, ZERO, ONE AND TWO.
4. COUNT DOWN TO ONE, ZERO, BORROW, FIFTEEN, FOURTEEN AND THIRTEEN.

COUNTING SEQUENCE

500
Rev B
Sheet 2 of 3



FUNCTION DIAGRAM

500
Rev B
Sheet 3 of 3

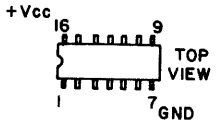
DESCRIPTION

The 501 circuit is a 5-bit comparator that provides comparison between two 5-bit words and gives three outputs: "less than", "greater than", and "equal to". A high level on the active low enable (pin 1) forces all three outputs low.

NOTES:

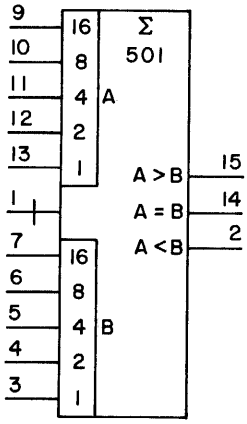
1. Vendor identification: 9324

2. Package pin configuration.



3. Pin names:

Pin	Function
1	Enable (active low) input
9,10,11,12,13	Word A parallel inputs
3,4,5,6,7	Word B parallel inputs
2	A Less Than B (A < B) output
14	A Equal to B (A=B) output
15	A Greater Than B (A > B) output



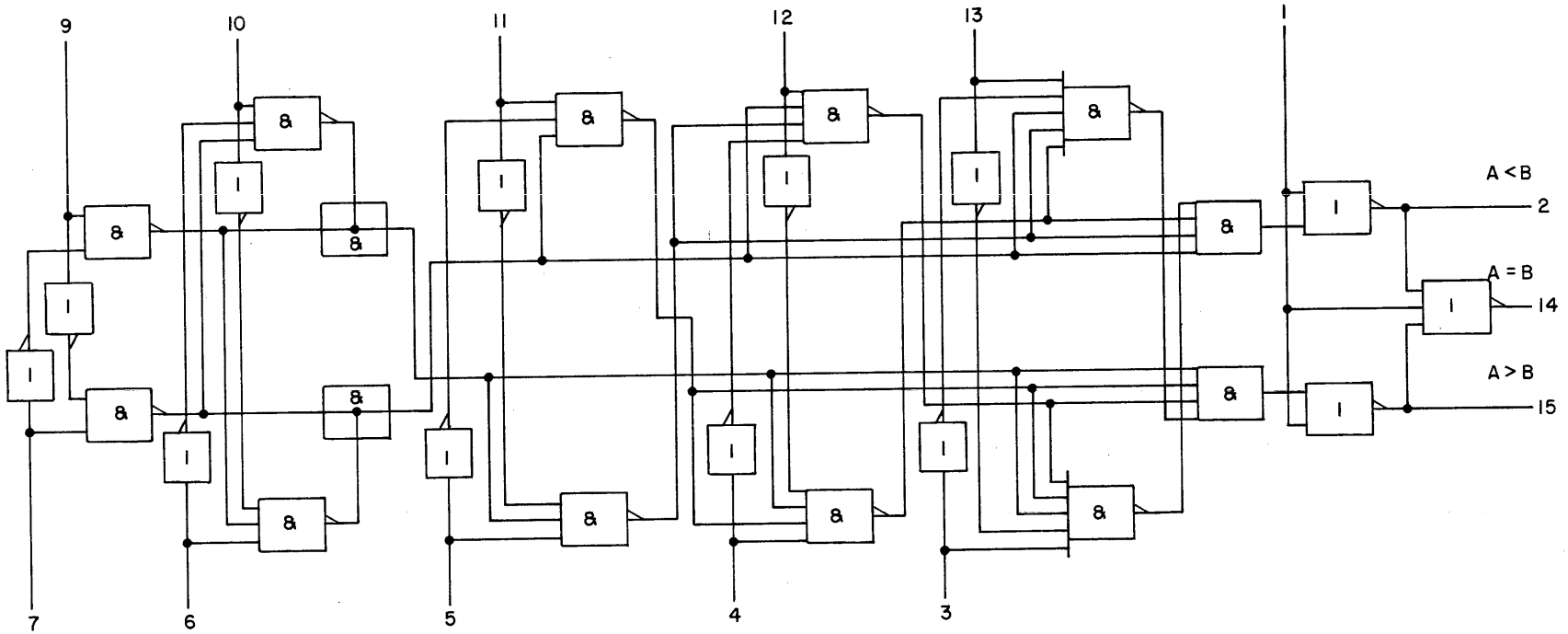
LOGIC SYMBOL

	INPUT		OUTPUT		
I	A	B	A<B	A>B	A=B
H	X		L	L	L
L	WORD A = WORD B		L	L	H
L	WORD A > WORD B		L	H	L
L	WORD A < WORD B		H	L	L

H = HIGH LEVEL
L = LOW LEVEL
X = EITHER HIGH OR LOW LEVEL

TRUTH TABLE

501
Rev B
Sheet 1 of 2



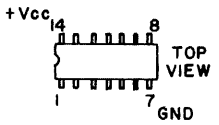
FUNCTION DIAGRAM

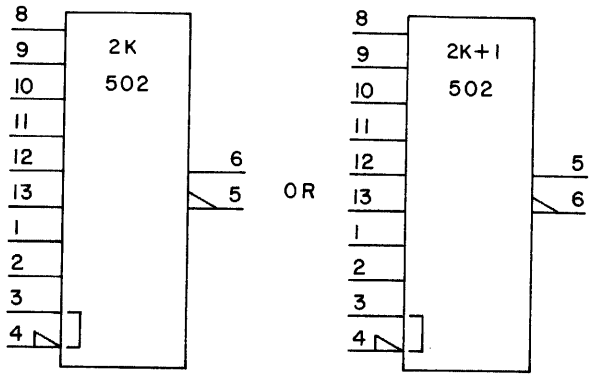
DESCRIPTION

The 502 circuit is an 8-bit parity generator/checker with complementry outputs and control inputs to facilitate operation in either odd-or even-parity applications.

NOTES:

1. Vendor identification: 74180
2. Package pin configuration.



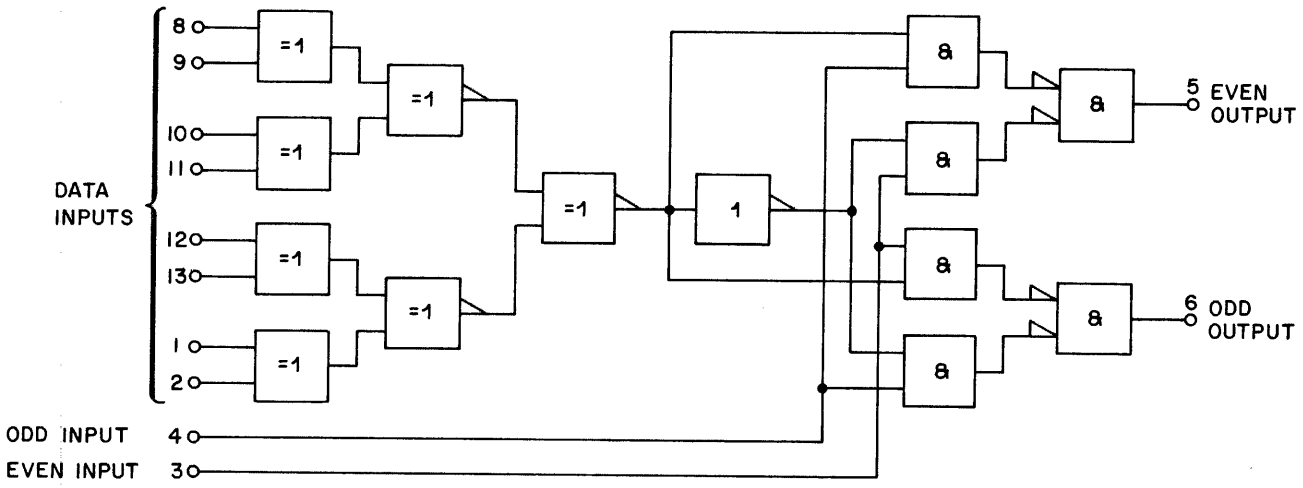


LOGIC SYMBOL

INPUTS			OUTPUTS	
Σ OF 1's AT PINS 1, 2, 8 THRU 13	PIN 3	PIN 4	PIN 5	PIN 6
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = IRRELEVANT

TRUTH TABLE

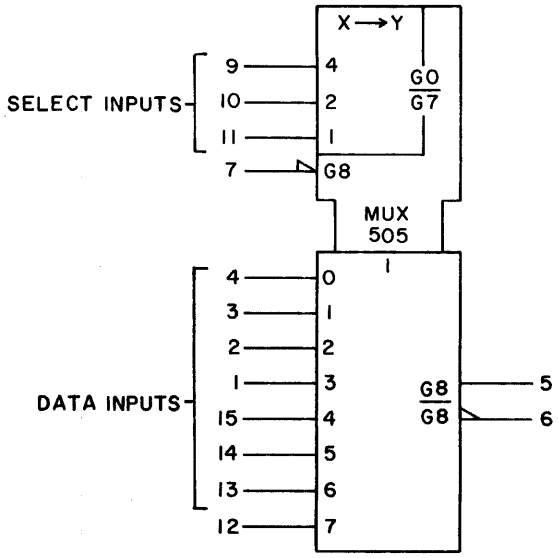


FUNCTION DIAGRAM

502
Rev C
Sheet 1 of 1

DESCRIPTION

Element 505 is a 1-of-8 multiplexer/selector that takes data from one of eight data inputs, depending upon the state of the select inputs, and gates it to pin 5 when G8 (strobe input) goes low. When the strobe input is high,pin 5 will be low. Pin 6 is the complement of pin 5.



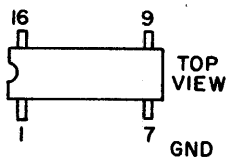
LOGIC SYMBOL

NOTES:

1. Vendor identification:

Element	Vendor Number
505	74151
505S	74S151

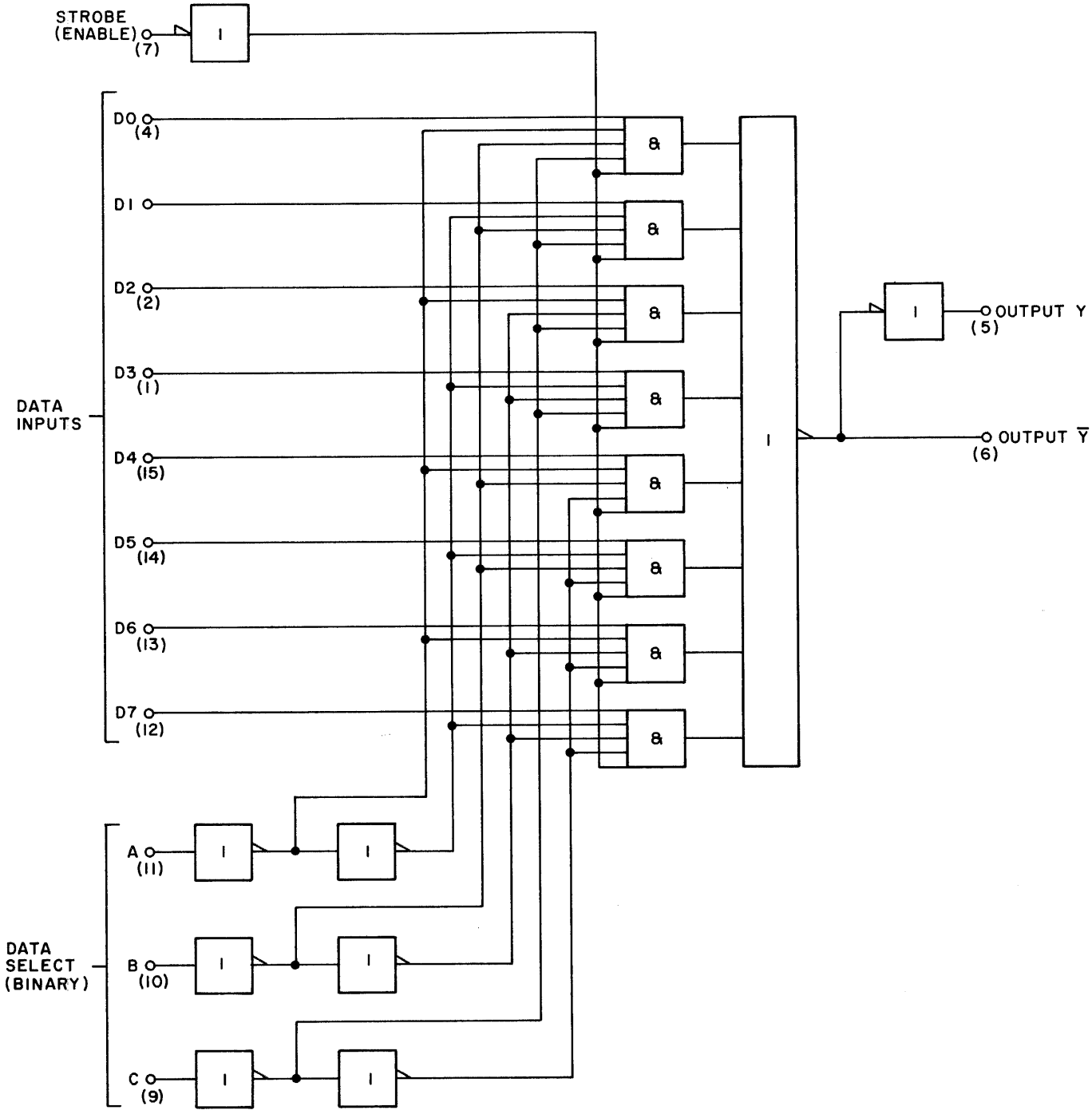
2. Package pin configuration. +Vcc



INPUTS												OUTPUTS	
C	B	A	STROBE	D0	D1	D2	D3	D4	D5	D6	D7	Y	$\overline{Y}$
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	0	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

TRUTH TABLE

505
Rev B
Sheet 1 of 2



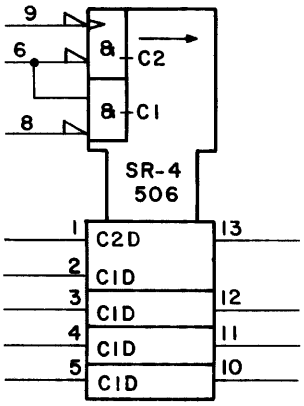
FUNCTIONAL DIAGRAM

505
Rev B
Sheet 2 of 2

DESCRIPTION

The 506 circuit is a 4-bit shift register capable of shifting right, shifting left, or parallel-in, parallel-out operations. When the mode input (pin 6) is low, the parallel inputs (pins 2 through 5) and clock 2 input (pin 8) are disabled. Serial data may then be entered at pin 1 and shifted right from pin 10 toward pin 13 under control of the right shift clock (pin 9). When the clock input is high, the serial input is enabled. When the clock goes low, the serial input is disabled, and the data is transferred to output pin 13. The right shift of data at the outputs also occurs at this time.

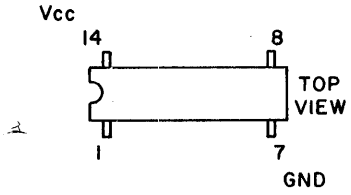
When the mode input is high, the serial input and right shift clock are disabled and the circuit now functions as four R-S master-slave FF's with a common clock input, clock 2 (pin 8). By connecting pin 10 to pin 4, pin 11 to pin 3, and pin 12 to pin 2, a left-shift register is formed with input pin 5 as the serial input and pin 8 as the left shift clock. Thus, the circuit can shift left or right at independent clock rates by controlling the mode input.



LOGIC SYMBOL

NOTES:

1. Vendor identification: 7495A
2. Package pin configuration:



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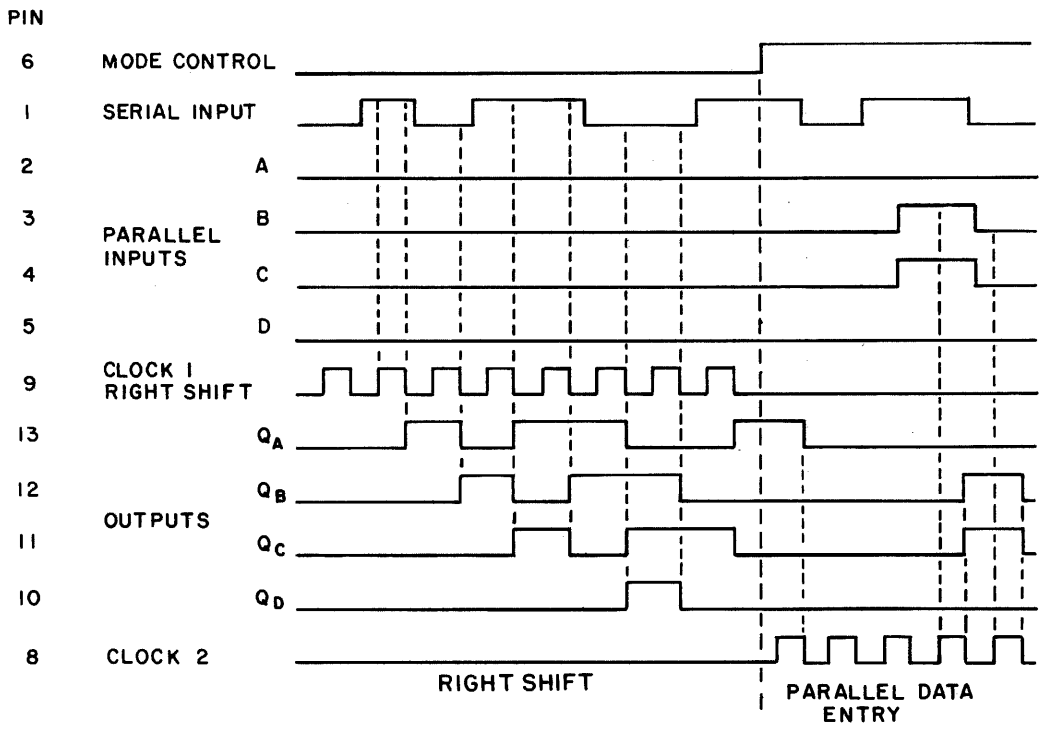
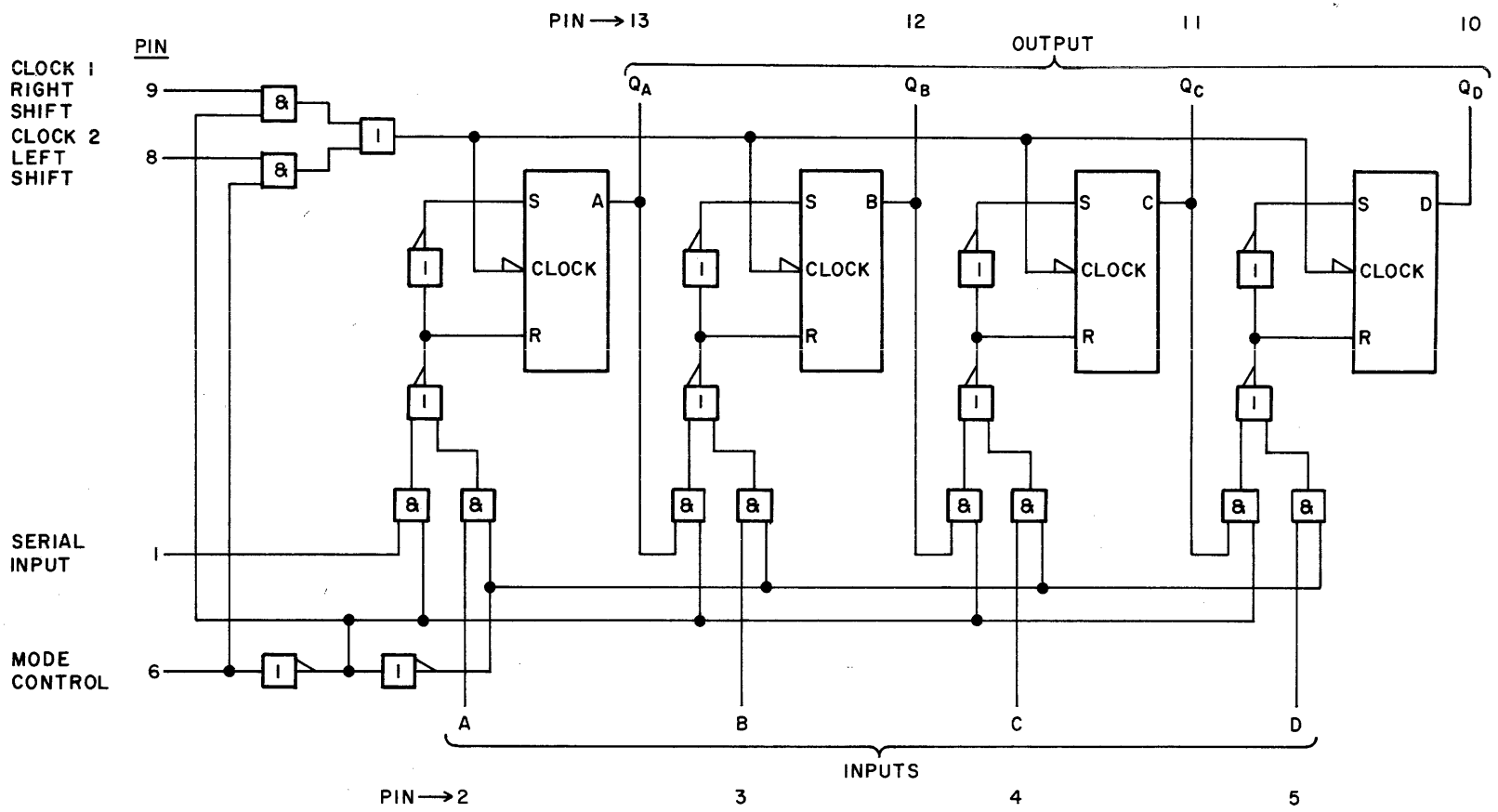


FUNCTION SEQUENCE

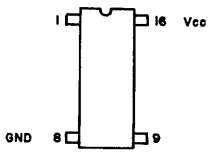

PIN → 13
12
11
10
OUTPUT
PIN
CLOCK 1
RIGHT
SHIFT
9
CLOCK 2
LEFT
SHIFT
8
Q_A
Q_B
Q_C
Q_D
S A
S B
S C
S D
CLOCK
R
SERIAL
INPUT
1
MODE
CONTROL
6
A
B
C
D
INPUTS
PIN → 2
3
4
5

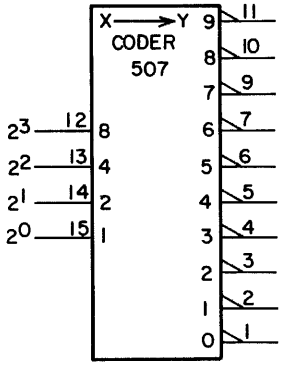
DESCRIPTION

The 507 circuit is a 4-line-to-10-line (BCD-to-decimal) decoder. For encoded input counts of 0 through 9 (0000-1001), the appropriate decimal output goes low. For other input states (1010-1111), all outputs are high.

NOTES:

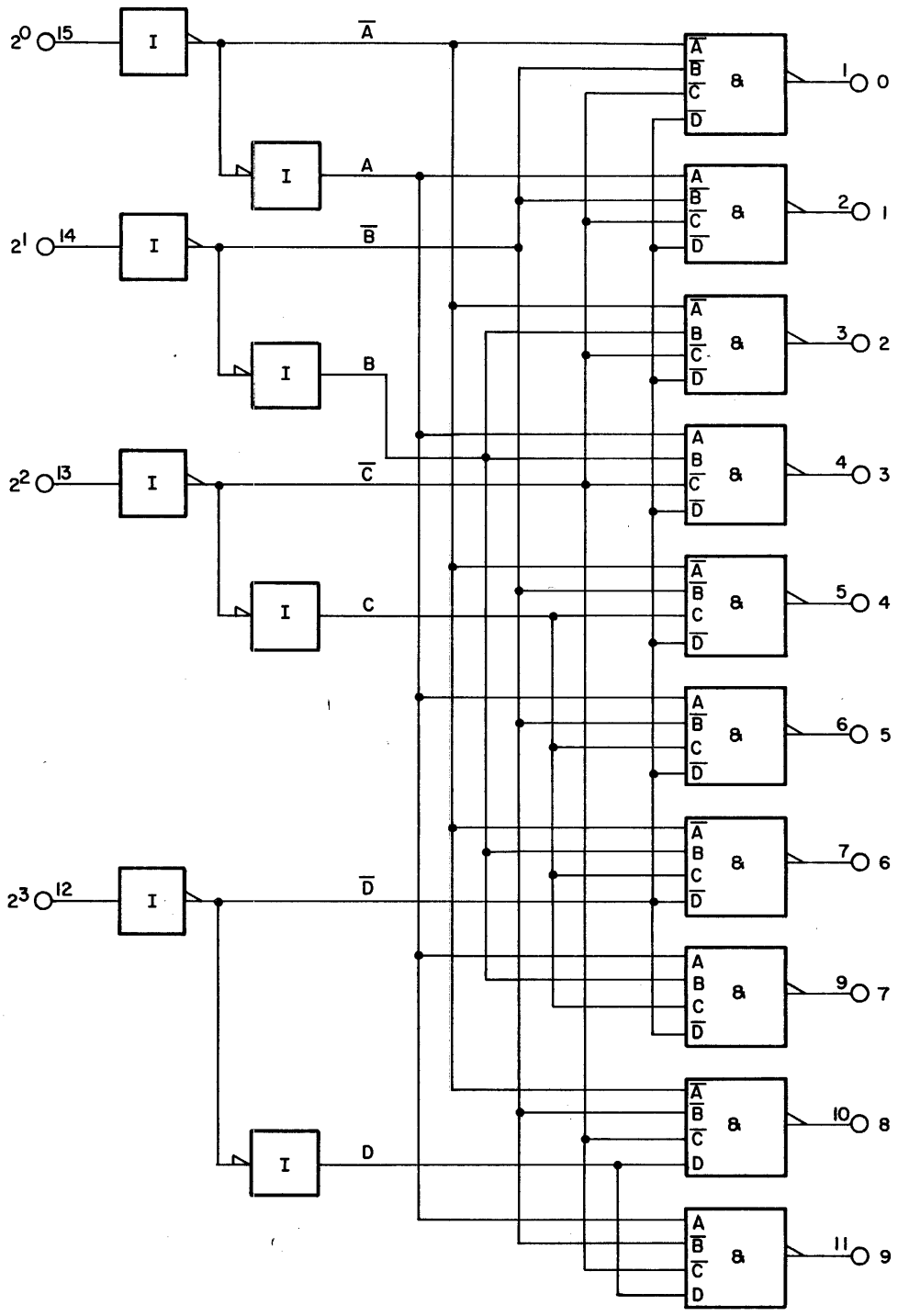
1. Vendor identification: 7442/9352
2. Package pin configuration:





LOGIC SYMBOL

507
Rev A
Sheet 1 of 2

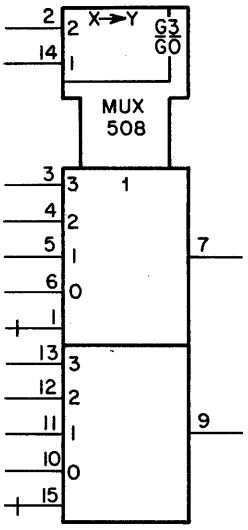


FUNCTIONAL DIAGRAM

507
Rev A
Sheet 2 of 2

DESCRIPTION

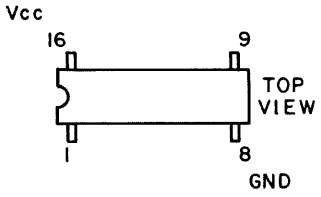
Element 508 consists of two 4-line-to-1-line multiplexers with common select inputs and a separate low-active enable (high-active inhibit) input for each section. When either inhibit/enable input (pins 1, 15) is high, the output from that section will be low, regardless of which data input has been selected. When inhibit/enable is low, the output follows that of the selected data input.



LOGIC SYMBOL

NOTES:

1. Vendor Identification: 74153
2. Package pin configuration.



SELECT INPUTS		DATA INPUTS				ENABLE	OUTPUT
2	14	6	5	4	3	1	7
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH
L = LOW
X = EITHER HIGH OR LOW

TRUTH TABLE

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Rev. B
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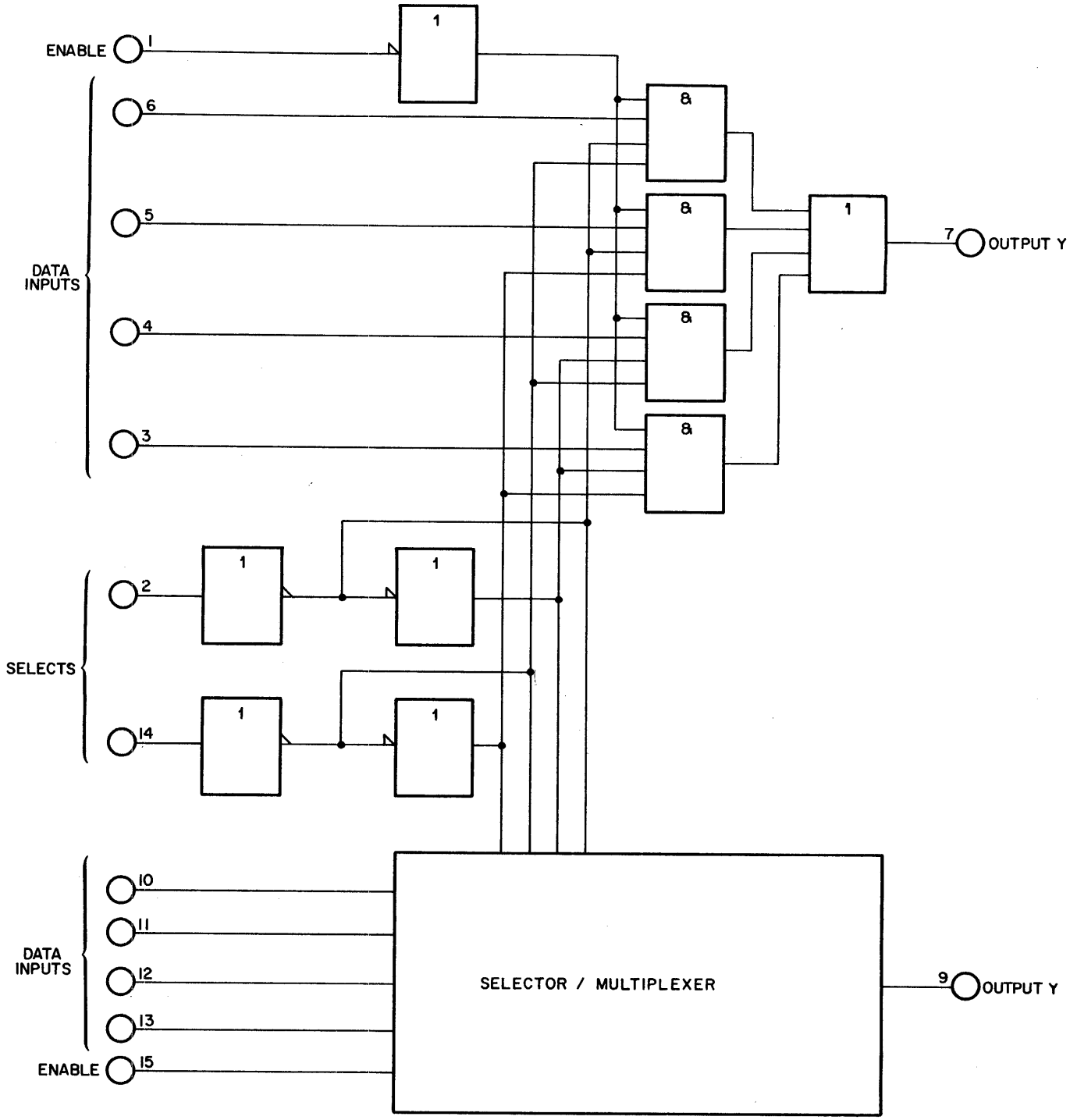


LOGIC DIAGRAM

508
Rev. A
Sheet 2 of 2

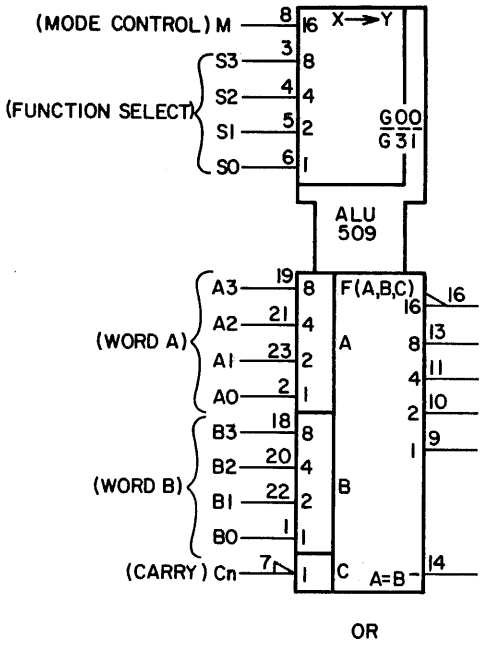
DESCRIPTION

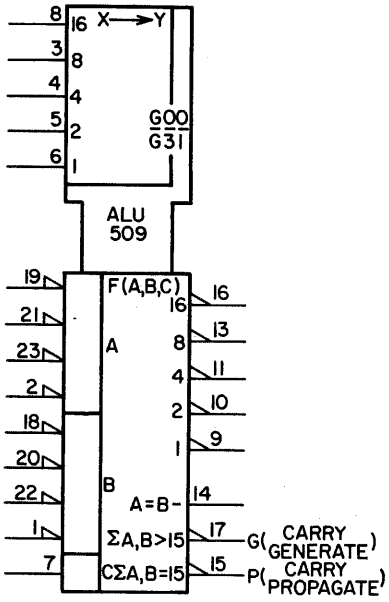
The 509 circuit is a 4-bit, high-speed, parallel arithmetic logic unit (ALU). It can perform 16 different arithmetic operations or 16 different logic operations on active high or active low data. The function table on page 509-2 lists these operations.

Placing a high on the mode control input (M) causes the 509 circuit to perform logic operations on the individual bits as listed. When the mode control input is low, the device performs arithmetic operations on the two 4-bit words. The carry out Cn+4 signal provides for ripple carry between devices, or for carry look-ahead between packages using the carry propagate (P) and carry generate (G) signals. In slower circuits, the 509 circuit may be used in a ripple carry mode by connecting the $\overline{Cn+4}$ signal to the carry input ($\overline{Cn}$) of the next unit. Using the 509 circuit in conjunction with the 510 circuit, carry look-ahead circuit makes possible high speed operation. Each group of four 509's requires one 510.

The 509 circuit subtracts by 1's complement addition and generates the 1's complement of the subtrahend internally. The resultant output is A-B-1, which requires an end-around or forced carry to provide A-B.

Logic equivalence between the four bits of A and the four bits of B is indicated by the A = B output being high when the unit is in the subtract mode. The open-collector A = B output can be wire-AND connected to other A = B outputs to give a comparison for more than four bits. Used with the carry out signal, the A = B signal can indicate A > B and A < B. The A = B output must connect to a pull-up resistor tied to Vcc.





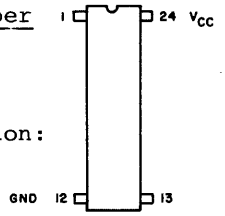
LOGIC SYMBOL

NOTES:

1. Vendor identification:

Element	Vendor Number
509	74181
509S	74S181

2. Package pin configuration:



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MODE SELECT INPUTS				ACTIVE LOW INPUTS AND OUTPUTS		ACTIVE HIGH INPUTS AND OUTPUTS	
S3	S2	S1	S0	LOGIC (M=H)	ARITHMETIC (M=L)(Cn=L) (1)	LOGIC (M=H)	ARITHMETIC (M=L)(Cn=H) (1)
L	L	L	L	$\overline{A}$	A MINUS 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB MINUS 1	$\overline{A + B}$	A + B
L	L	H	L	$\overline{A + B}$	$A\overline{B}$ MINUS 1	$\overline{A}B$	A + $\overline{B}$
L	L	H	H	LOGICAL 1	MINUS 1	LOGICAL 0	MINUS 1
L	H	L	L	$\overline{A + B}$	A PLUS (A + $\overline{B}$)	$\overline{AB}$	A PLUS $A\overline{B}$
L	H	L	H	$\overline{B}$	AB PLUS (A + $\overline{B}$)	$\overline{B}$	(A + B) PLUS $A\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A MINUS B MINUS 1	$A \oplus B$	A MINUS B MINUS 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$	$A\overline{B}$	$A\overline{B}$ MINUS 1
H	L	L	L	$\overline{A}B$	A PLUS (A + B)	$\overline{A}$ + B	A PLUS AB
H	L	L	H	$A \oplus B$	A PLUS B	$\overline{A \oplus B}$	A PLUS B
H	L	H	L	B	$A\overline{B}$ PLUS (A + B)	B	(A + $\overline{B}$) PLUS AB
H	L	H	H	A + B	A + $\overline{B}$	AB	AB MINUS 1
H	H	L	L	LOGICAL 0	A PLUS A (2)	LOGICAL 1	A PLUS A (2)
H	H	L	H	$A\overline{B}$	AB PLUS A	A + $\overline{B}$	(A + B) PLUS A
H	H	H	L	AB	$A\overline{B}$ PLUS A	A + B	(A + $\overline{B}$) PLUS A
H	H	H	H	A	A	A	A MINUS 1

(1) Add "plus 1" to arithmetic operation when Cn is active.

(2) Each bit is shifted to the next more significant position.

FUNCTION TABLE

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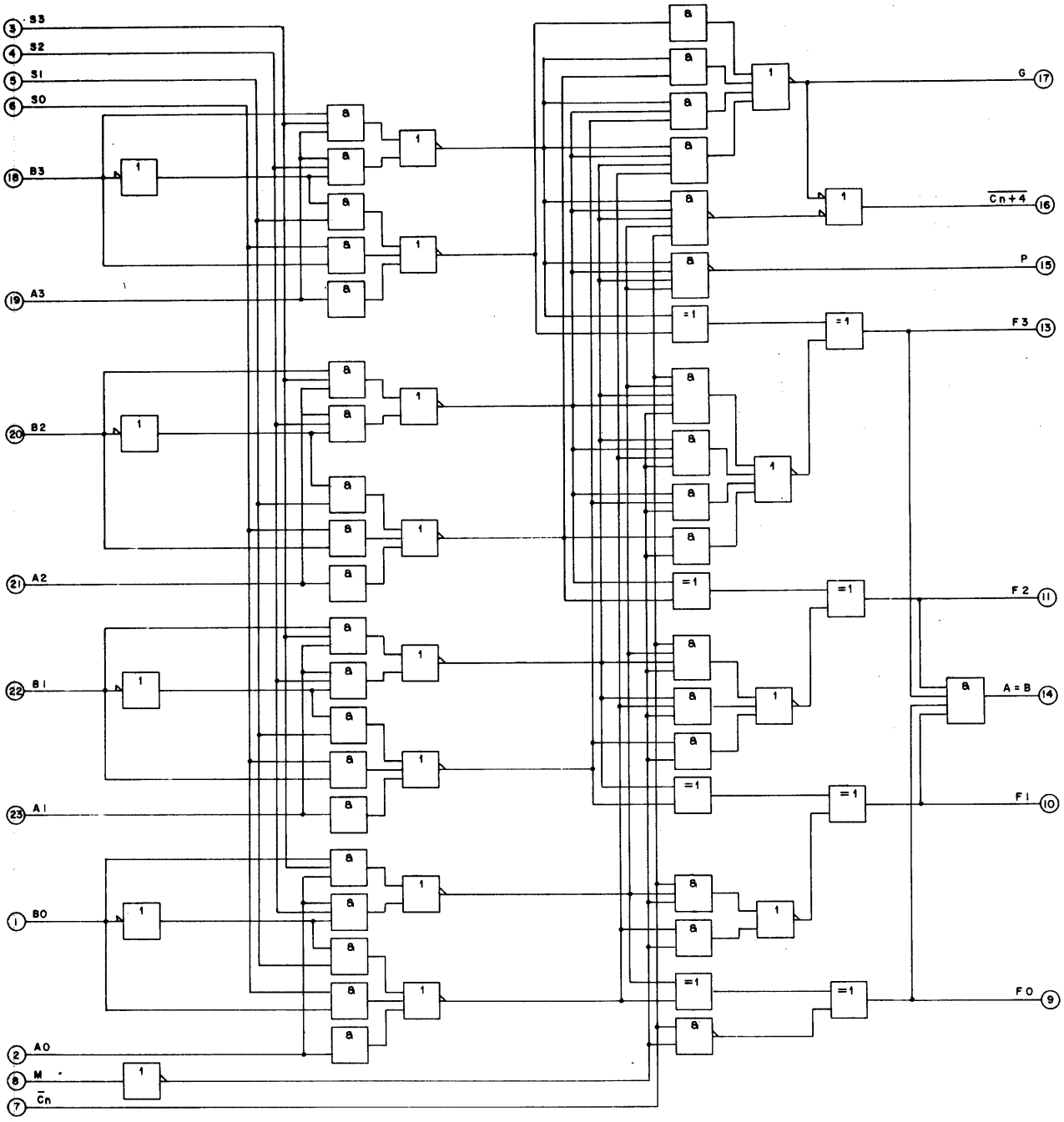

FUNCTIONAL DIAGRAM

509
Rev A
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DESCRIPTION:

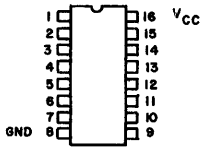
The 510 circuit is a look-ahead carry generator. It is generally used with the type 509 arithmetic logic unit circuit to provide carry look-ahead capability. Each 510 circuit accepts up to four pairs of active-low carry propagate (P_0, P_1, P_2, P_3) and carry generate (G_0, G_1, G_2, G_3) signals and an active-high carry input (Cn). The 510 circuit can anticipate a carry across four adders or groups of adders, and provides the anticipated active-high carries (C_{n+X}, C_{n+Y}, C_{n+Z}). The 510 circuit also has active-low carry propagate (P) and carry generate (G) outputs for cascading. Cascaded 510 circuits can provide look-ahead across N-bit adders.

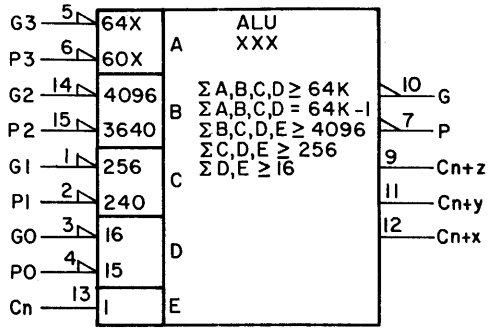
NOTES

1. Vendor identification:

Element	Vendor Number
510	74182
510S	74S182

2. Package pin configuration:





G0, G1, G2 AND G3 — CARRY GENERATE INPUTS

P0, P1, P2 AND P3 — CARRY PROPAGATE INPUTS

C - CARRY INPUT

Cn+x, Cn+y, AND Cn+z — CARRY OUTPUTS

G - CARRY GENERATE OUTPUT

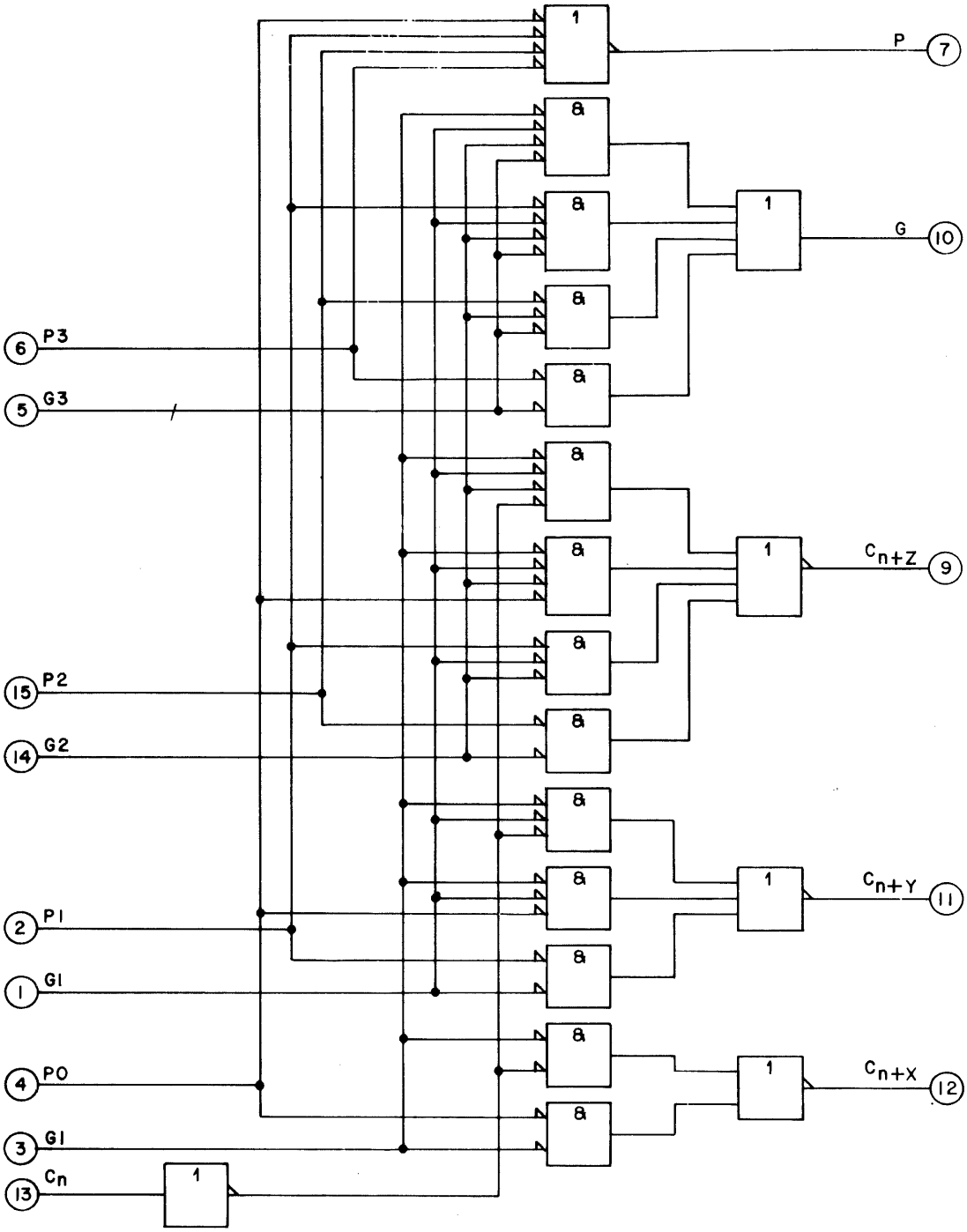
P - CARRY PROPAGATE OUTPUT

LOGIC SYMBOL

INPUTS									OUTPUTS				
C_n	G_0	P_0	G_1	P_1	G_2	P_2	G_3	P_3	C_{n+X}	C_{n+Y}	C_{n+Z}	G	P
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

TRUTH TABLE

510
Rev A
Sheet 1 of 2



FUNCTIONAL DIAGRAM

510
Rev A
Sheet 2 of 2

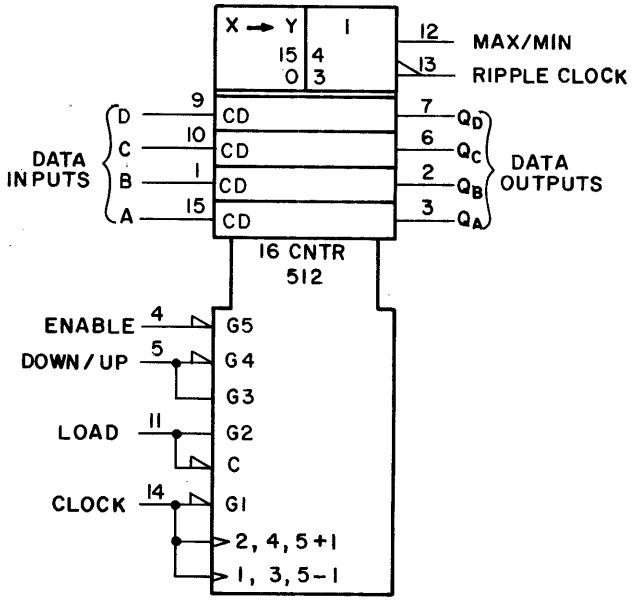
DESCRIPTION

The 512 circuit is a 4-bit binary, synchronous, reversible up/down counter having a complexity of 58 equivalent gates. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic.

The outputs of the four master-slave flip-flops are triggered on a low-to-high transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the state of the down/up input. When low, the counter counts up and when high, it counts down.

The counter is fully programmable; that is, the outputs may be preset to any state by placing a low on the load input and entering the desired data at the data inputs. The output will then change to agree with the data inputs independently of the state of the clock input.

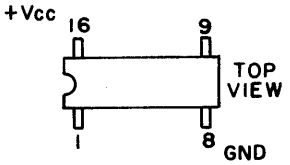
Two outputs are available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. Power dissipation is typically 325 milliwatts for either the decade or binary version. Maximum input clock frequency is typically 25 megahertz and is guaranteed to be at least 20 megahertz.



LOGIC SYMBOL

NOTES:

1. Vendor identification: 74191, 9336
2. Package pin configuration:



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Rev B
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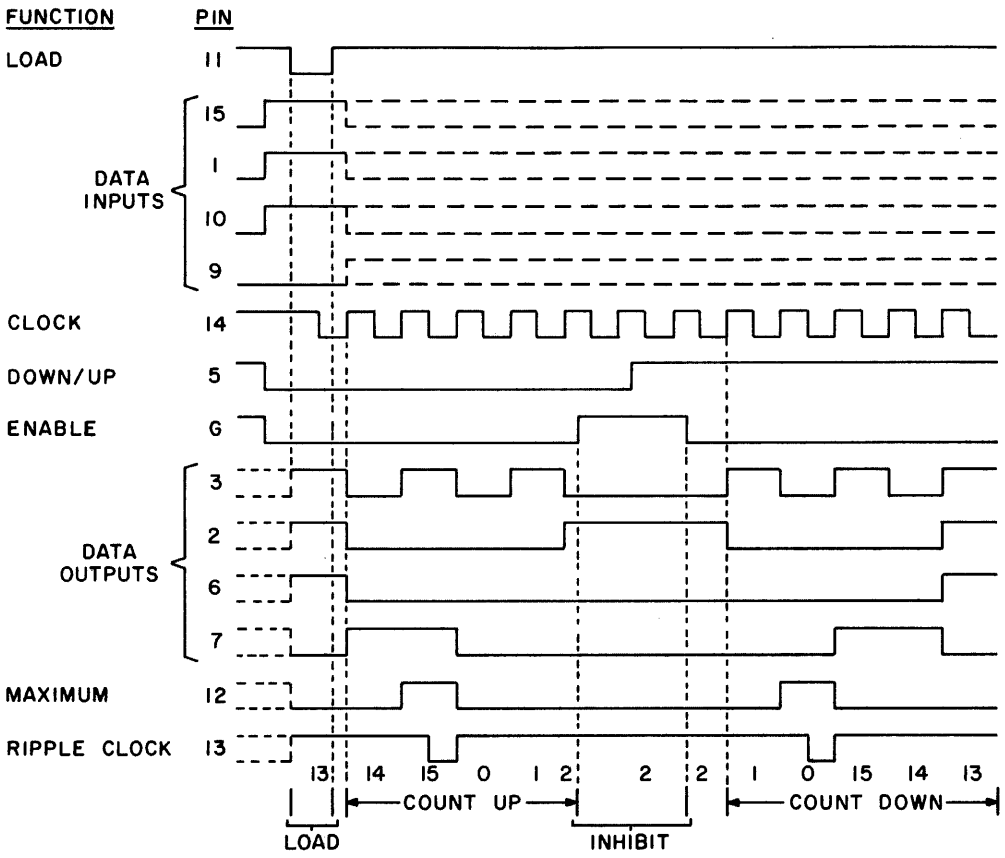
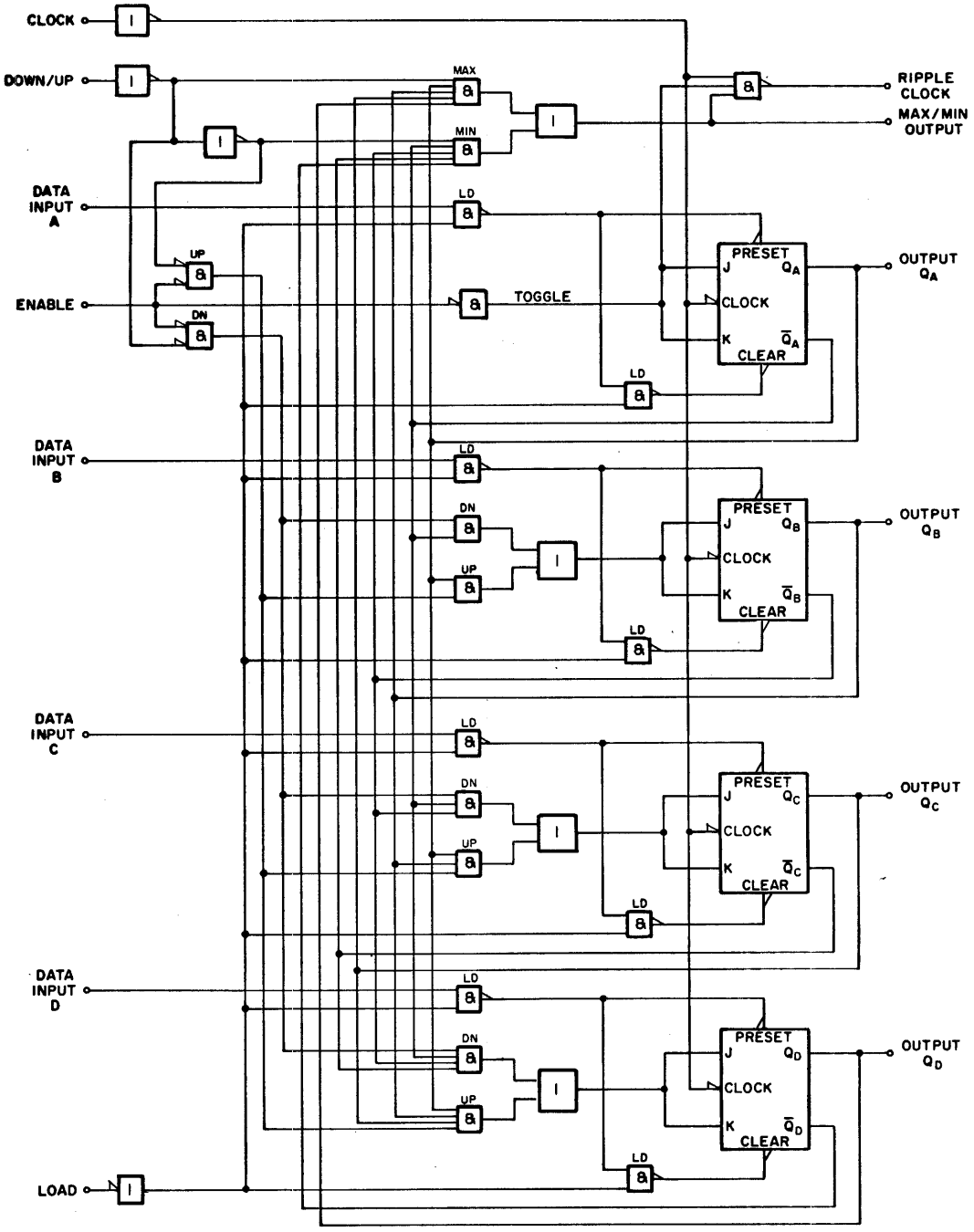


1. LOAD (PRESET) TO BINARY THIRTEEN.
2. COUNT UP TO FOURTEEN, FIFTEEN (MAXIMUM) ZERO, ONE, AND TWO.
3. INHIBIT.
4. COUNT DOWN TO ONE, ZERO (MINIMUM), FIFTEEN, FOURTEEN, AND THIRTEEN.

TYPICAL, LOAD, COUNT, AND INHIBIT SEQUENCES



FUNCTION DIAGRAM

512
Rev C
Sheet 3 of 3

DESCRIPTION

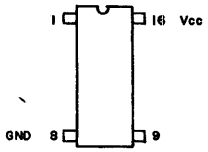
Element 514 is a 16-bit (4x4) random-access register file/memory with open-collector outputs and non-destructive readout. Separate Read/Write addressing permits reading from one 4-bit word location while simultaneously writing into another location.

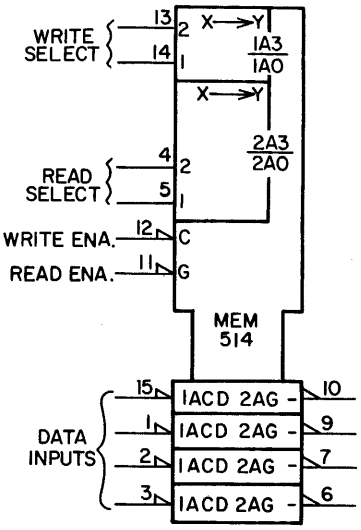
Writing or reading is accomplished when the corresponding enable signal is low. When the Read enable is high, all outputs will be high (see function tables).

Maximum read and write times are 35 and 45 ns, respectively.

NOTES:

1. Vendor identification: 74170
2. Package pin configuration:





LOGIC SYMBOL

READ FUNCTION

INPUTS			OUTPUT PINS			
2	1	G	10	9	7	6
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

WRITE FUNCTION

INPUTS			WORD			
2	1	C	0	1	2	3
L	L	L	Q=D	Qn	Qn	Qn
L	H	L	Qn	Q=D	Qn	Qn
H	L	L	Qn	Qn	Q=D	Qn
H	H	L	Qn	Qn	Qn	Q=D
X	X	H	Qn	Qn	Qn	Qn

1. L = LOW, H= HIGH, X= DON'T CARE
2. W0B1: WORD 0, BIT 1, ETC.
3. Q=D: THE FOUR STORED BITS WILL ASSUME THE BINARY VALUE OF THE FOUR DATA INPUT BITS.
4. Qn: NO CHANGE

514
Rev A
Sheet 1 of 1

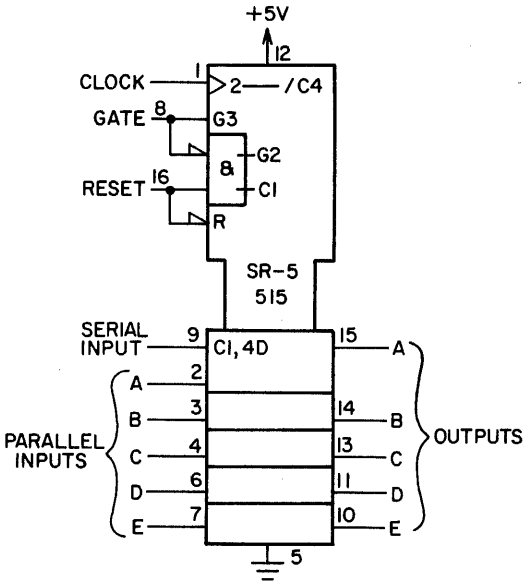
DESCRIPTION

The 515 shift resister consists of five set-reset, master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both the inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to the low state by applying a low voltage to the reset input (pin 16). This condition may be applied independent of the clock input (pin 1).

The flip-flops may be independently set to the high state by applying a high to both the set input of the specific flip-flop and the common Gate input G3 (pin 8). Input G3 is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. G3 is also independent of the clock input or clear input.

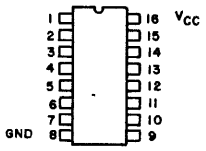
Transfer of information to the output pins occurs when the clock input goes from a low to a high. Since the flip-flops are J-K master-slave circuits, the proper information must appear at the two inputs of each flip-flop prior to the rising edge of the clock. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining flip-flop inputs. The reset input (pin 16) must be at a high and the gate G3 input must be at a low when clocking occurs.



LOGIC SYMBOL

NOTES:

1. Vendor identification:
2. Package pin configuration:



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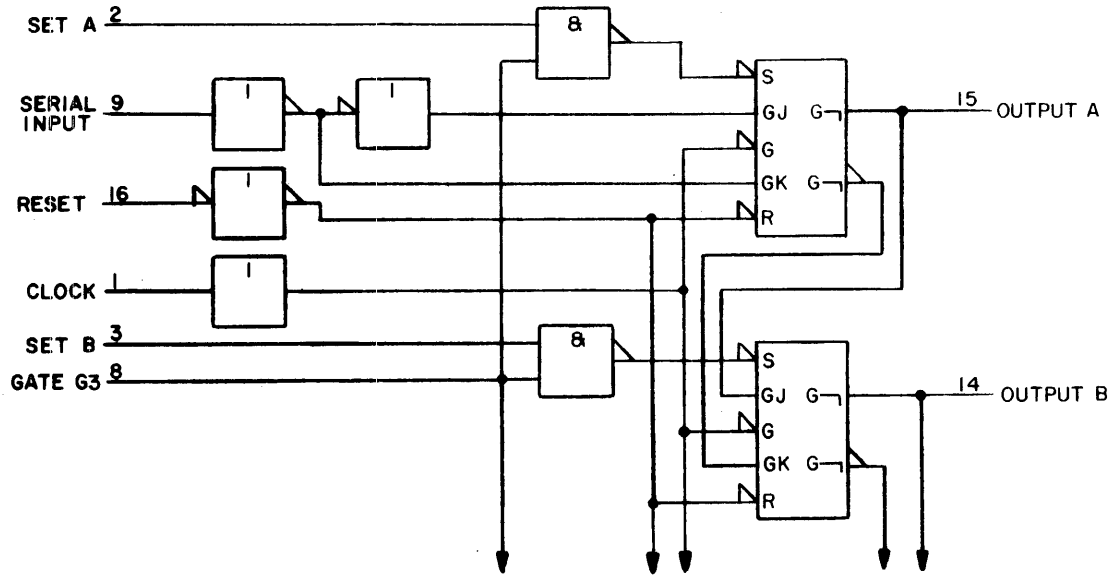
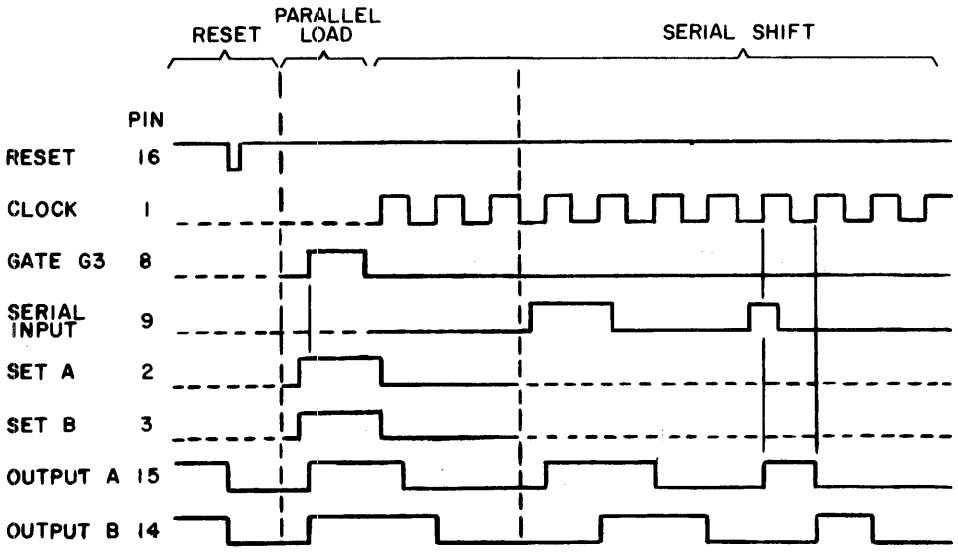


NOTE: FLIP-FLOPS C, D, AND E NOT SHOWN. THEY ARE IDENTICAL TO A AND B.

FUNCTIONAL DIAGRAM



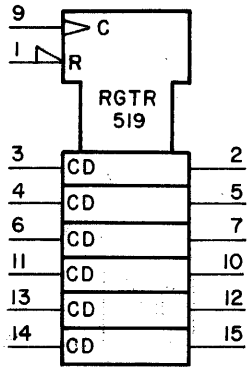
____ = LEVEL HAS NO EFFECT

TIMING DIAGRAM

515
Rev A
Sheet 2 of 2

DESCRIPTION

The 519 circuit is a register made up of six D-type flip-flops with common clock and clear inputs.



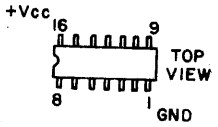
LOGIC SYMBOL

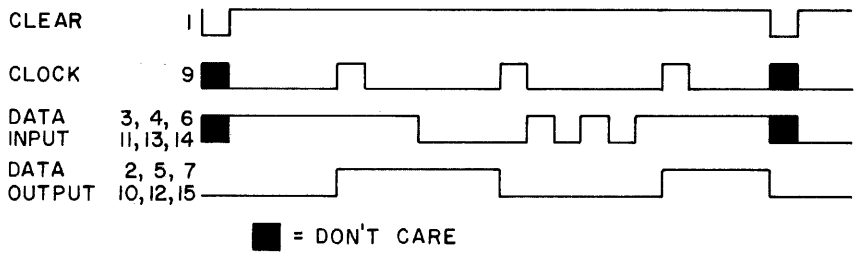
NOTES:

1. Vendor identification:

Element	Vendor Number
519	74174
519S	74S174

2. Package pin configuration.





FUNCTION SEQUENCE

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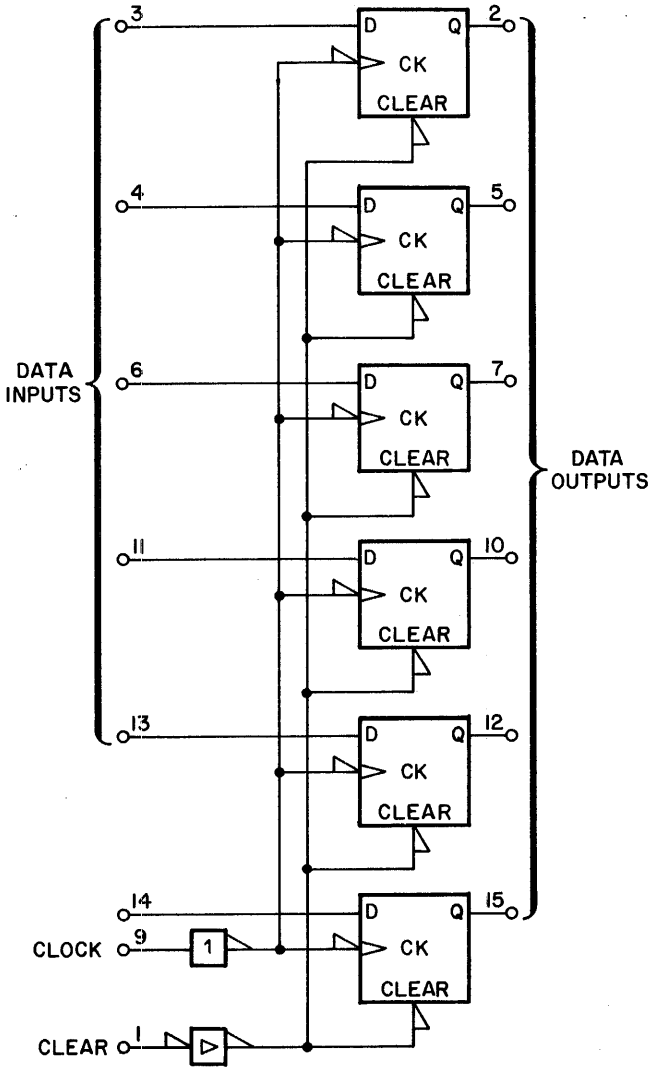
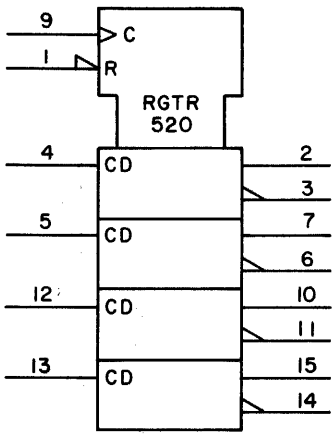


FUNCTION DIAGRAM

519
Rev B
Sheet 2 of 2

DESCRIPTION

Element 520 contains four positive-edge-triggered D-type flip-flops with common clock and reset (clear) inputs. Each FF has complementary outputs. Information at the input is transferred to the output on the positive-going transition of the clock pulse. When the clock is either high or low, input data has no effect on the outputs.



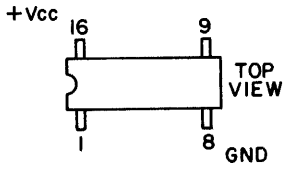
LOGIC SYMBOL

NOTES:

1. Vendor identification:

Element	Vendor Number
520	74175
520LS	74LS175
520S	74S175

2. Package pin configuration:



INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	NC	NC

↑ = TRANSITION FROM LOW TO HIGH LEVEL

X = DON'T CARE

NC = SAME AS BEFORE INDICATED INPUT CONDITIONS WERE ESTABLISHED

TRUTH TABLE

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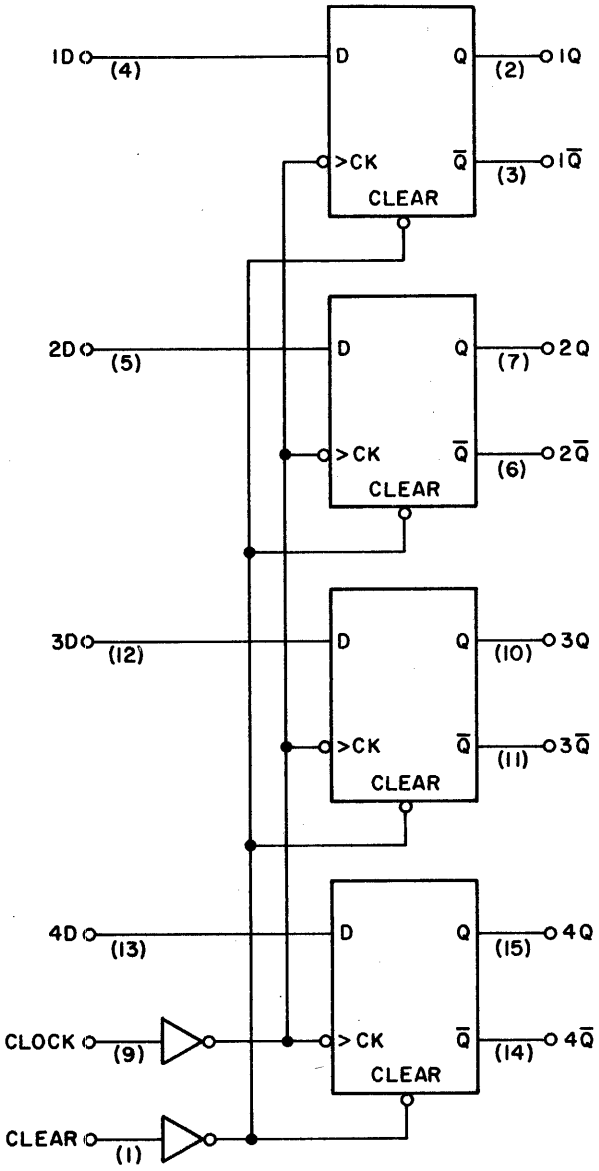
Rev C
Sheet 1 of 2



FUNCTIONAL DIAGRAM

520
Rev B
Sheet 2 of 2

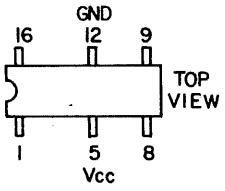
DESCRIPTION

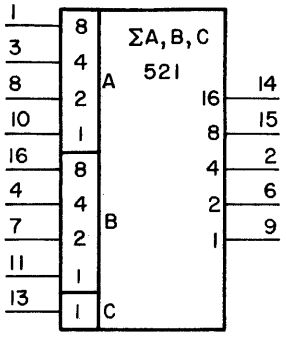
The 521 circuit performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit.

NOTES:

1. Vendor identification: 7483

2. Package pin configuration.



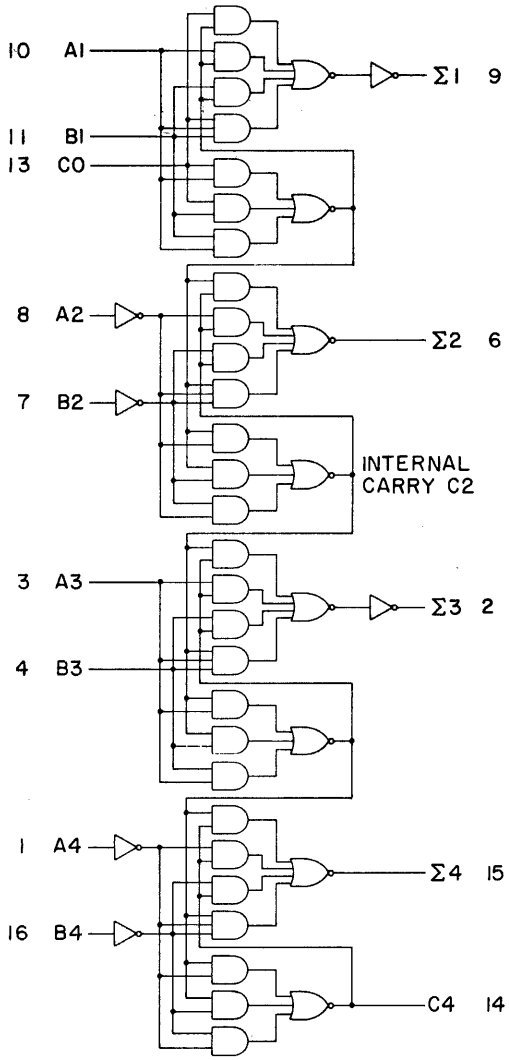


LOGIC SYMBOL

INPUT				OUTPUT					
				WHEN CO=L			WHEN CO=H		
						WHEN C2=L			WHEN C2=H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

NOTE 1: INPUT CONDITIONS AT A1, A2, B1, B2, AND CO ARE USED TO DETERMINE OUTPUTS Σ1 AND Σ2 AND THE VALUE OF THE INTERNAL CARRY C2. THE VALUES AT C2, A3, B3, A4, AND B4, ARE THEN USED TO DETERMINE OUTPUTS Σ3, Σ4, AND C4.

TRUTH TABLE

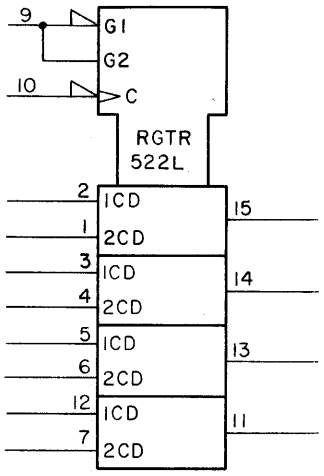


FUNCTION DIAGRAM

521
Rev C
Sheet 1 of 1

DESCRIPTION

Circuit type 522L is a quad 2-input selector/ storage register that allows four bits of data to be switched in parallel to the appropriate outputs from four 2-bit data sources. The outputs consist of four S-R morter-slave flip-flops that hold the data output states until new data is gated in.



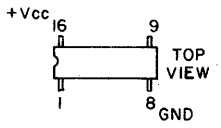
LOGIC SYMBOL

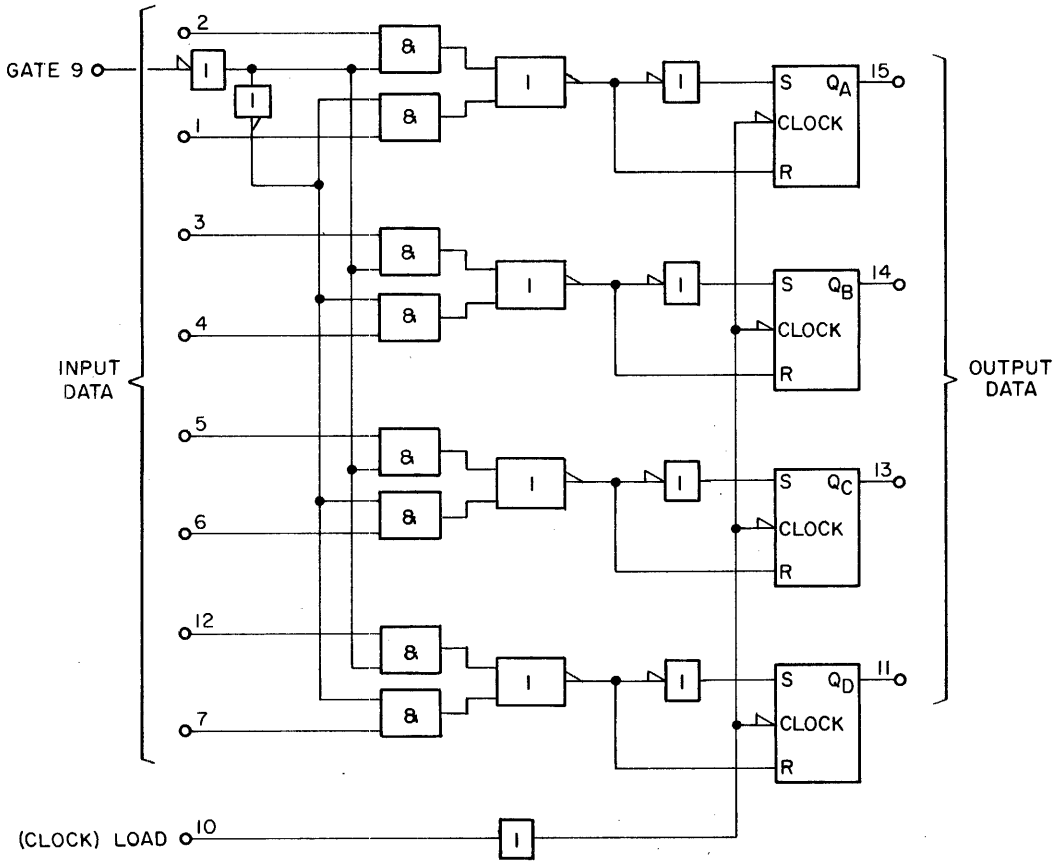
NOTES:

1. Vendor Identification

Element	Vendor Number
522	74L98

2. Package pin configuration.





FUNCTION DIAGRAM

522
Rev D
Sheet 1 of 1

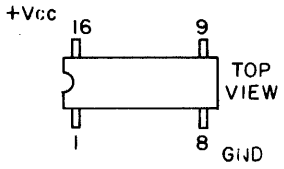
DESCRIPTION

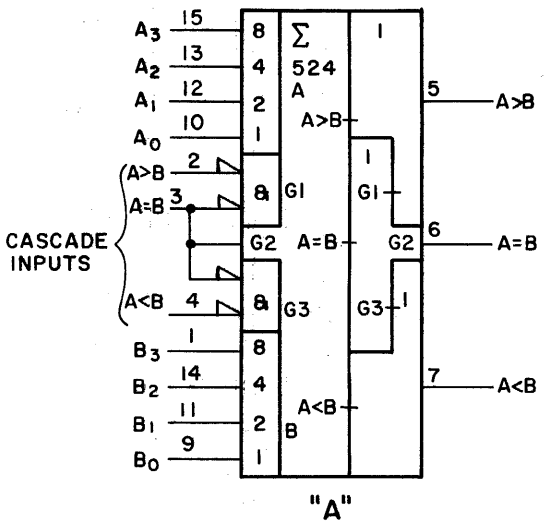
Element 524 performs a magnitude comparison of two 4-bit words (word A and word B). One of three conditions will exist and the output corresponding to that condition will be high (the other two will be low). For words greater than 4 bits, two or more circuits are cascaded using the cascade input (pins 2, 3 and 4).

For applications requiring only an equality indication, the logic symbol may appear as in "B". In this usage, the grounded pins may not always be shown.

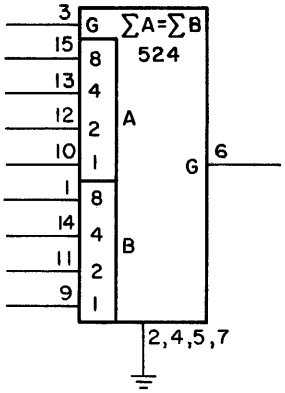
NOTES:

1. Vendor identification: 7485
2. Package pin configuration.





"A"



"B"

LOGIC SYMBOLS

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3 B3	A2 B2	A1 B1	A0 B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	H	L	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	H	L	L	H

TRUTH TABLE

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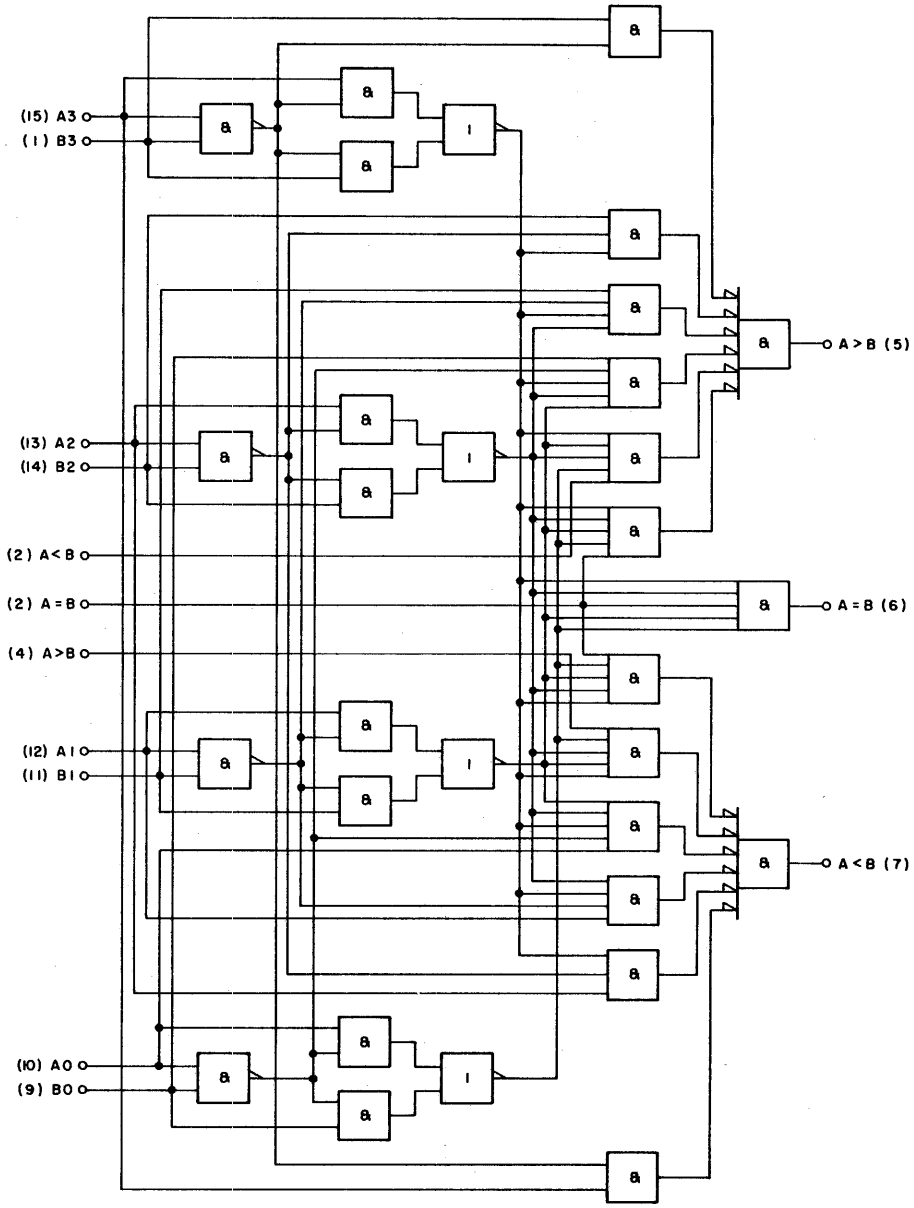
Rev D
Sheet 1 of 2



FUNCTIONAL DIAGRAM

524
Rev B
Sheet 2 of 2

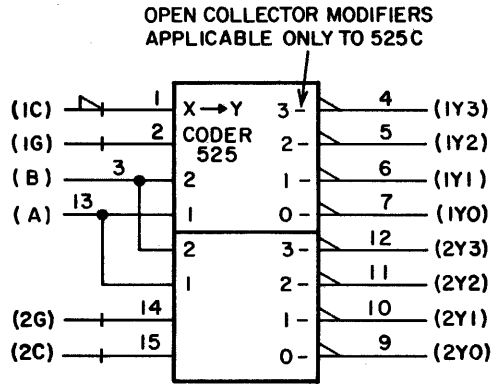
DESCRIPTION

General

Element 525* consists of two separate sections that are used as either 2-to-4 decoders or 1-to-4 demultiplexers. Each section has individual strobes and data inputs; however, they have common code inputs (select A and B). These circuits may also be used in combination to form either a 3-to-8 decoder or a 1-to-8 demultiplexer circuit. Figure 1 shows the functional diagram for this chip, with pin numbers in parentheses. The following paragraphs discuss each of the possible applications.

Dual Two-Line to Four-Line Decoder

When used in this manner (refer to Figure 2), the two-line code is applied to the common select inputs, A and B. The two output sections are then enabled individually via their strobe and data inputs. Outputs 1Y0-1Y3 are enabled when strobe input 1G is low and data input 1C is high. The other four-line output section (2Y0-2Y3) is enabled when both strobe 2G and data 2C are low.



LOGIC SYMBOL

*Element 525C is identical in pin configuration and function to 525, but provides open-collector outputs.

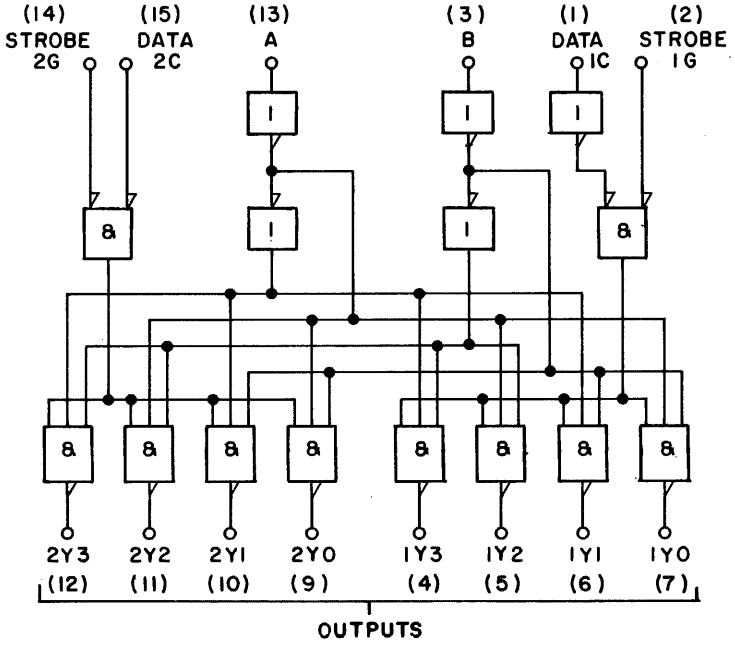


Figure 1. FUNCTIONAL DIAGRAM

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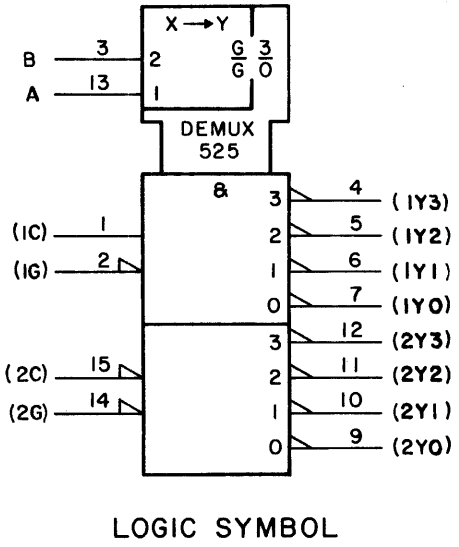
Rev C
Sheet 1 of 3

Dual One-Line to Four-Line Demultiplexer

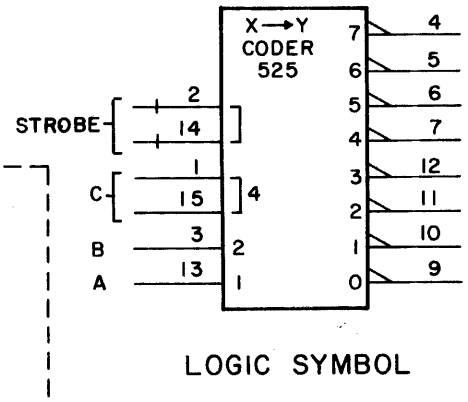
When used as a demultiplexer (refer to Figure 2), the serial input data is applied to each section via the data inputs 1C or 2C and what appears at the outputs is controlled by the A and B select lines. The two sections are enabled individually by their strobe inputs 1G or 2G.

Three-Line to Eight-Line Decoder

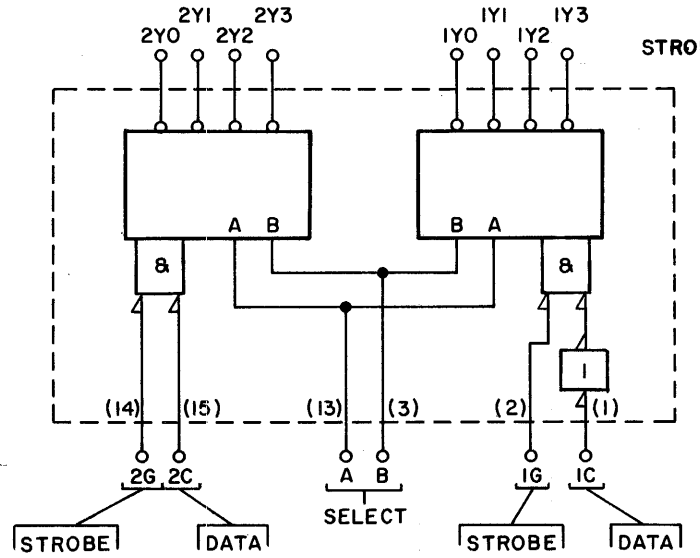
When used as a 3-to-8 decoder (Figure 3), the data inputs 1C and 2C are connected together and serve as a third select line (C). The strobes 1G and 2G are also connected together forming a common strobe. The code is then applied to the select inputs and the outputs are enabled when the strobe is low.



LOGIC SYMBOL



LOGIC SYMBOL



INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

Figure 2. Two Line to Four Line Decoder/ One Line to Four Line Demultiplexer

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Rev C
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One-Line to Eight-Line Demultiplexer

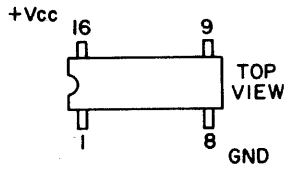
This application uses the same configuration as the 3-to-8 decoder; however, the common strobe line now serves as the data input and the outputs are controlled by the select lines (A, B and C). Refer to Figure 3.

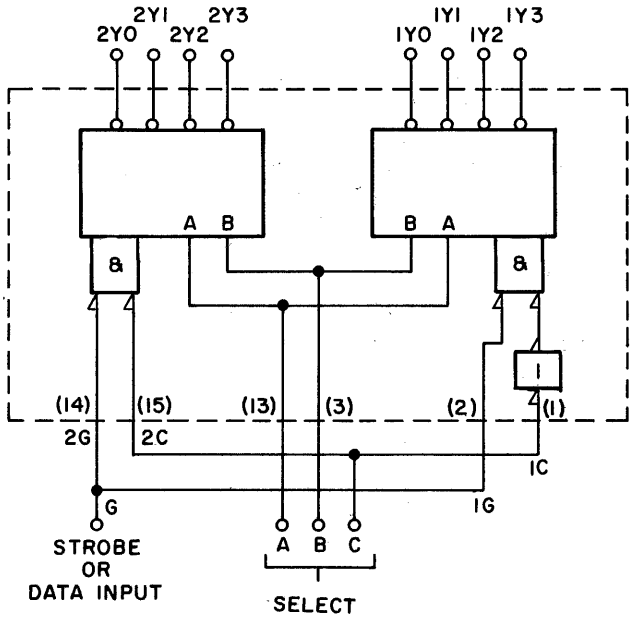
NOTES:

1. Vendor identification:

Element	Vendor Number
525	74155
525C	74156

2. Package pin configuration.



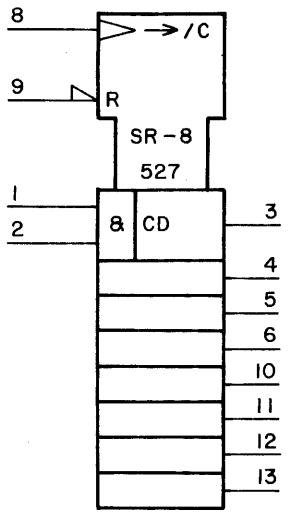


INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C	B	A	G	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Figure 3. Three Line to Eight Line Decoder/ One Line to Eight Line Demultiplexer

DESCRIPTION

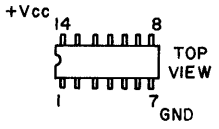
The 527 circuit is an 8-bit shift register with gated serial inputs and an asychronous clear. The gated serial inputs (pins 1 and 2) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requrements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

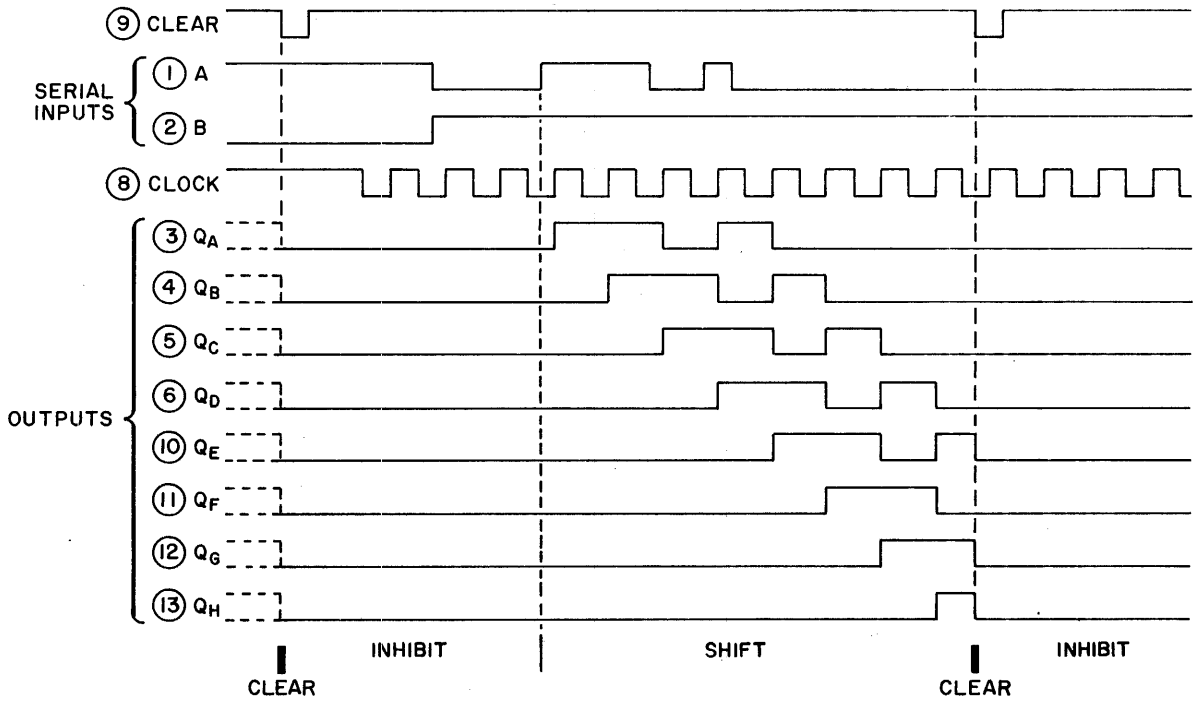


LOGIC SYMBOL

NOTES:

1. Vendor identification: 74164,8570
2. Package pin configuration.





NOTES: 1. TYPICAL CLEAR, INHIBIT, SHIFT, CLEAR, AND INHIBIT SEQUENCES.
2. ◯ = PIN ASSIGNMENTS.

FUNCTION SEQUENCE

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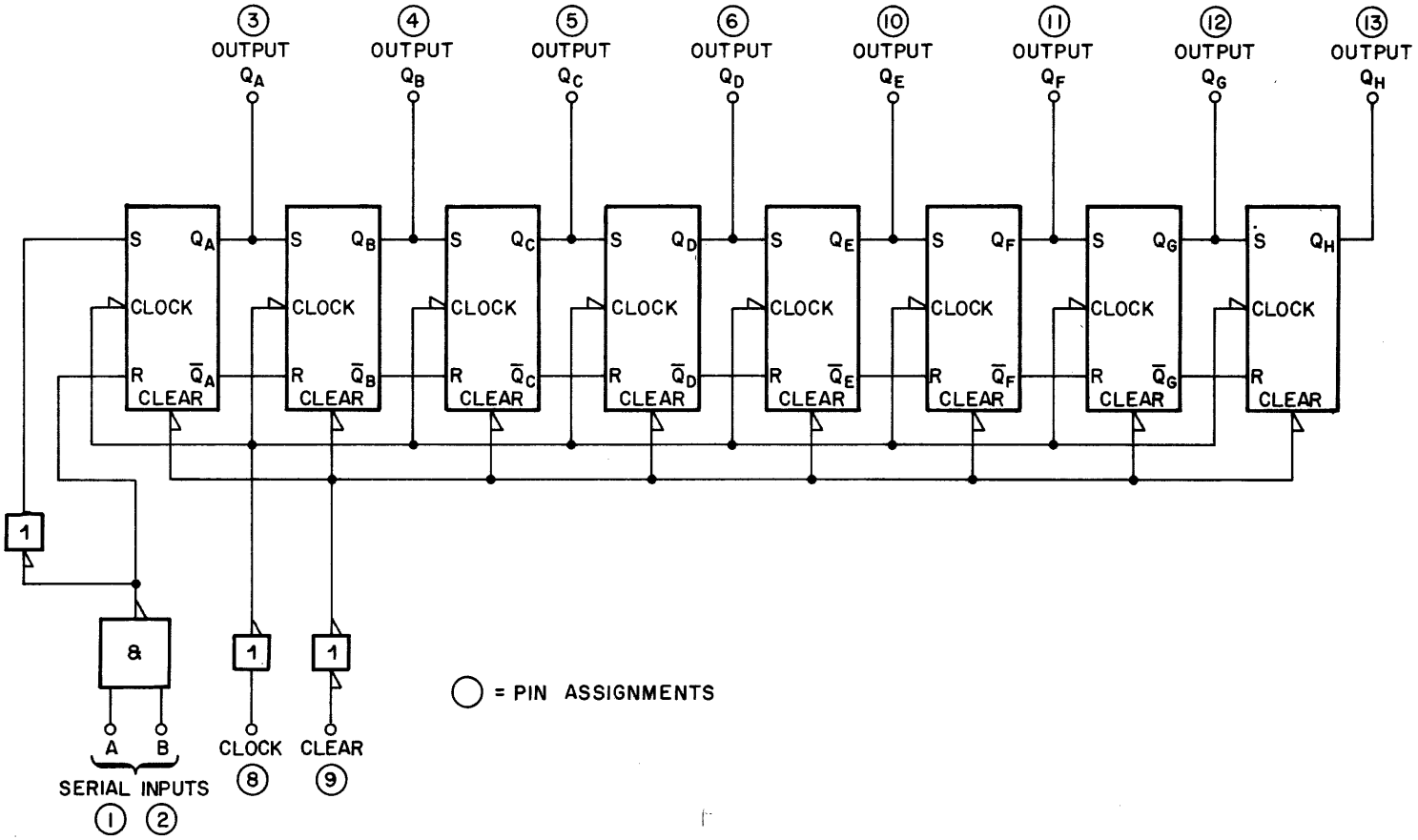
Rev C
Sheet 1 of 2



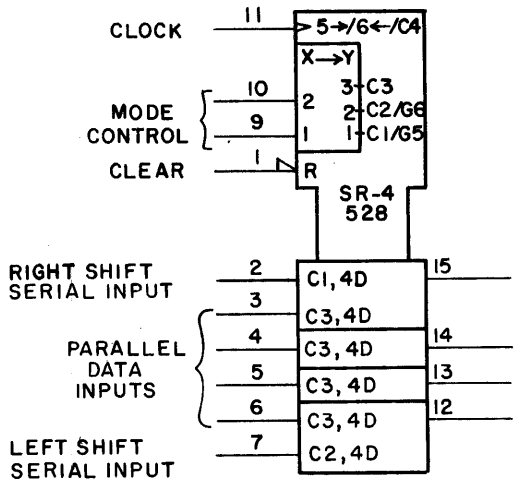
FUNCTION DIAGRAM

DESCRIPTION

The 528 is a bidirectional shift register that has 4 distinct modes of operation.

	Mode Control	
	Pin 10	Pin 9
Parallel (Broadside) Load (Pins 2-7)	H	H
Shift Right (Pin 15 Towards Pin 12)	L	H
Shift Left (Pin 12 Towards Pin 15)	H	L
Inhibit Clock (Do nothing)	L	L

In the parallel load mode, data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when pin 9 is high and pin 10 is low. Serial data for this mode is entered at the shift right data input. When pin 9 is low and pin 10 is high, data shifts left synchronously and new data is entered at the shift left serial input. Clocking (and hence data entry) is inhibited when both mode control inputs are low. The mode controls should be changed only when the clock is high.



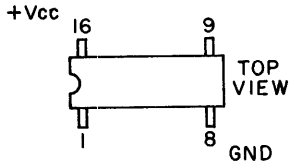
LOGIC SYMBOL

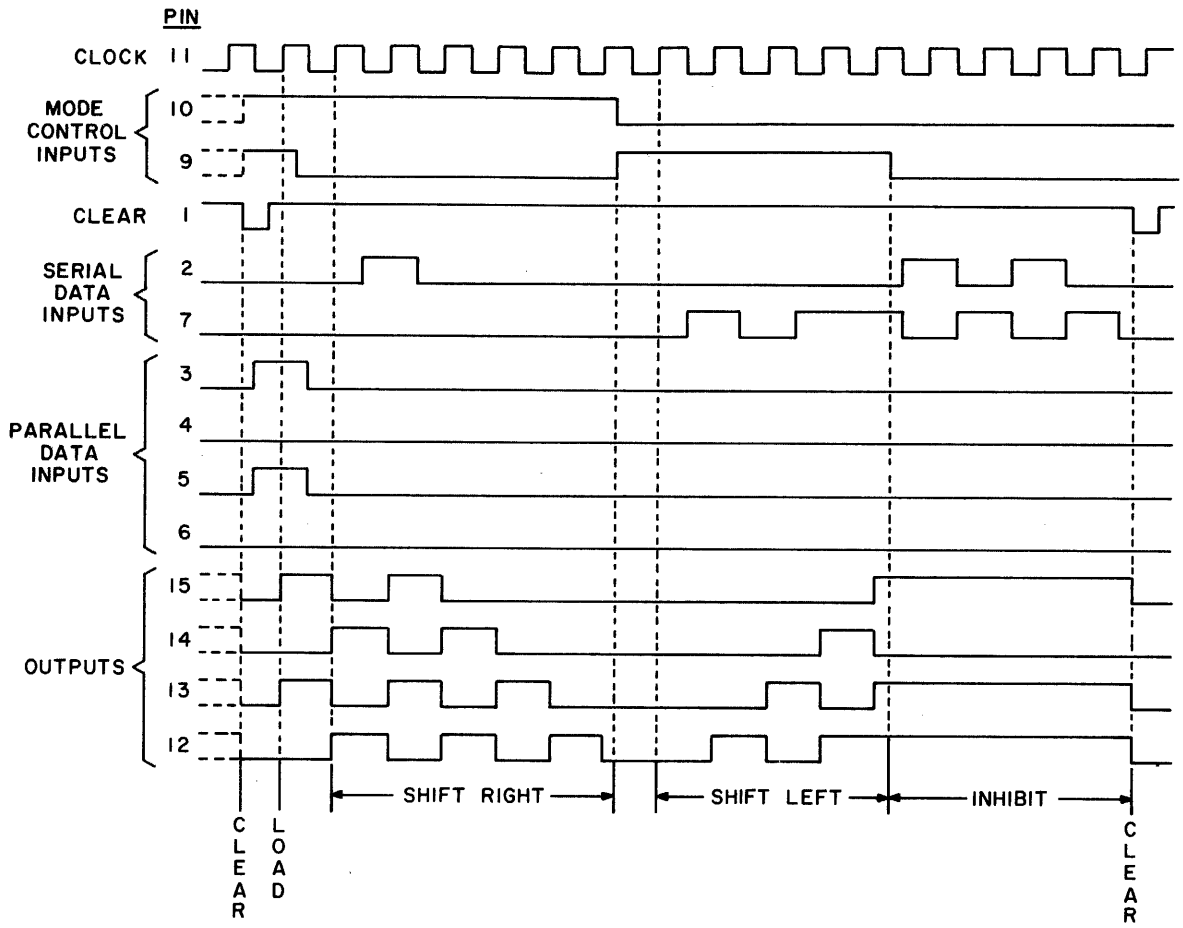
NOTES:

1. Vendor identification:

Element	Vendor Number
528	74194
528S	74S194

2. Package pin configuration.





TYPICAL CLEAR, LOAD, SHIFT RIGHT, SHIFT LEFT, INHIBIT AND CLEAR SEQUENCES

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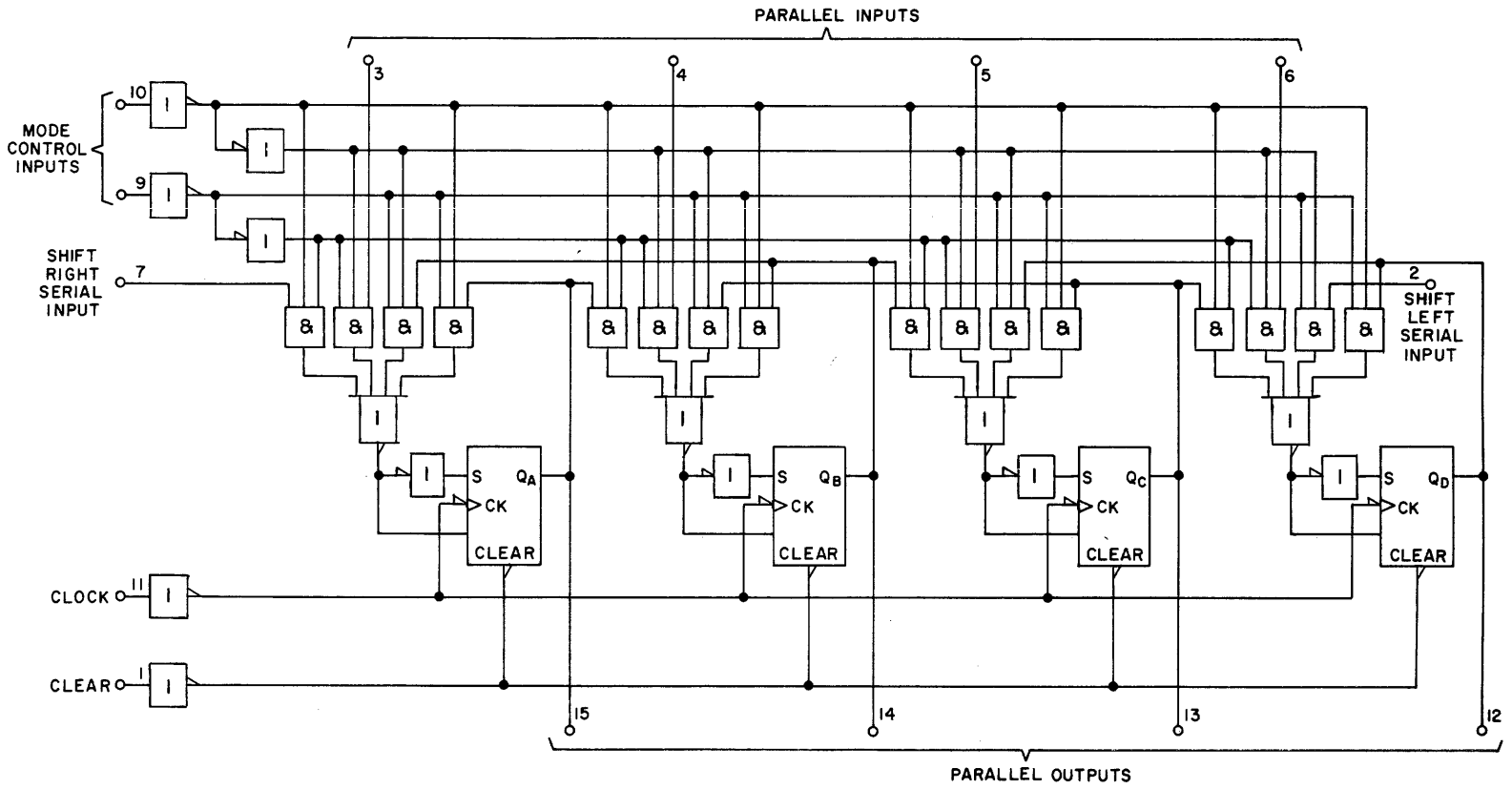
Rev B
Sheet 2 of 3



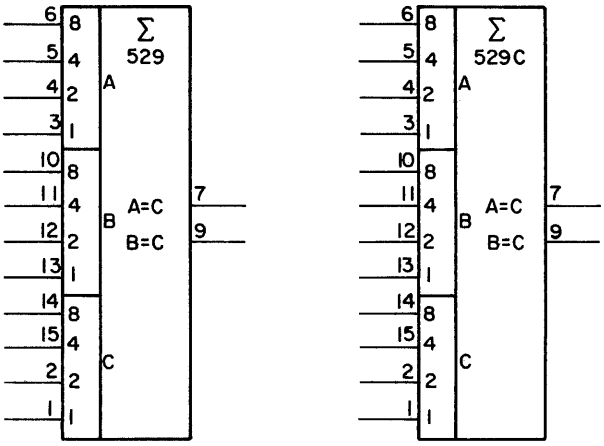
FUNCTIONAL BLOCK DIAGRAM

DESCRIPTION

Element 529 simultaneously and independently compares two 4-bit inputs, A and B, against a 4-bit reference input, C.

Output pin 7 (A=C) will go high when all four A inputs equal the respective reference inputs; output pin 9 (B=C) will go high when all four B inputs equal the respective reference inputs.

Element 529C is logically similar, but provides open-collector outputs that require external pull-up resistors to attain the high-active state.



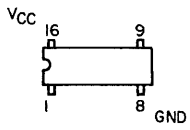
LOGIC SYMBOL

NOTES:

1. Vendor identification:

Element	Vendor Number
529	MC 4022
529C	MC 4021

2. Package pin configuration:



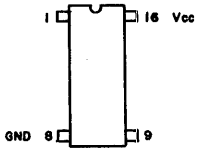
529
Rev A
Sheet 1 of 1

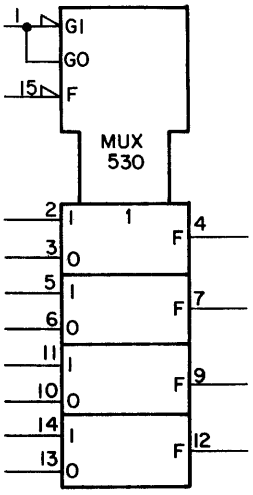
DESCRIPTION

Element 530 is a quad 2-input multiplexer with tri-state outputs. The input select and strobe (output enable) lines are common to all four sections. A high on the strobe input (F) puts all outputs in the Hi-Z state, regardless of the state of the select (G) or data inputs.

NOTES

1. Vendor identification: 8123
2. Package pin configuration:





LOGIC SYMBOL

INPUTS				OUT-PUT
CONTROL		DATA		
F	G	O	I	F
H	X	X	X	HI-Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

TRUTH TABLE

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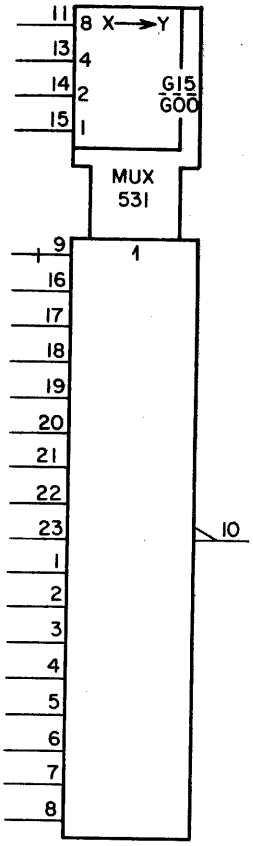
Rev A
Sheet 1 of 1

DESCRIPTION

The type 531 is a 16-bit multiplexer. It selects one of sixteen data sources. The output is determined by the encoded BCD gating on pins 11, 13, 14, and 15. The output is inverted from the input. The multiplexer is inhibited by a logic high on pin 9.

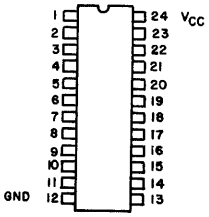
INPUT PINS																				OUTPUT PIN
GATING				I	DATA INPUTS															
11	13	14	15	9	8	7	6	5	4	3	2	1	23	22	21	20	19	18	17	16	10
X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	H	L	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	H	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	L	L	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	L	L	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	H	L	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	H	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	L	L	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	H
L	H	L	L	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	H	L	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	H
L	H	L	H	L	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	L
L	H	H	L	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	H
L	H	H	L	L	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	L
L	H	H	H	L	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
L	H	H	H	L	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	L
H	L	L	L	L	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	H
H	L	L	L	L	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	L
H	L	L	H	L	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	H
H	L	L	H	L	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	L
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	H
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	L
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	H
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	L
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	H
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	L
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	H
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	L
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	H
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	L
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	H
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L



LOGIC SYMBOL

NOTES:

1. Vendor identification: 74150
2. Package pin configuration:



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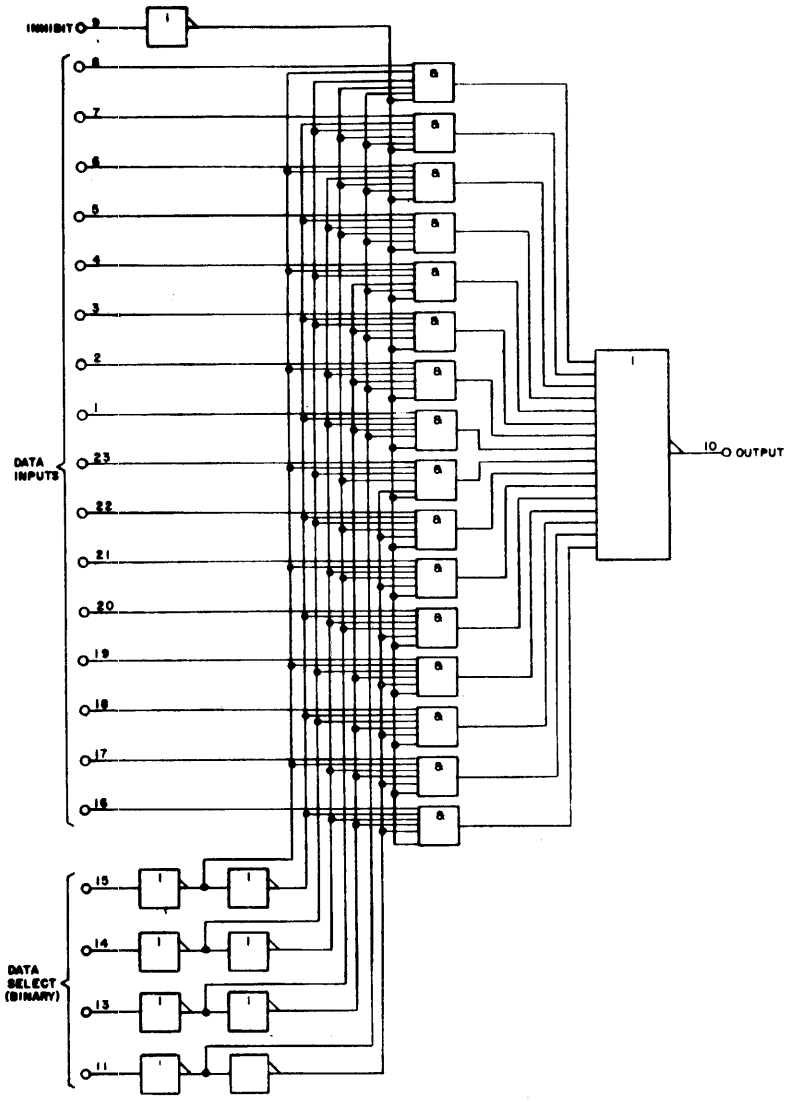
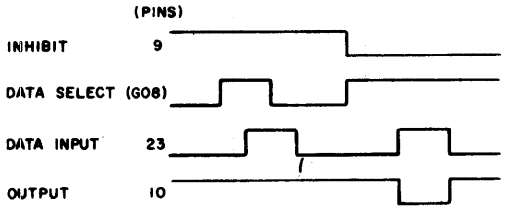


FUNCTIONAL DIAGRAM



TIMING DIAGRAM

531
Rev A
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DESCRIPTION

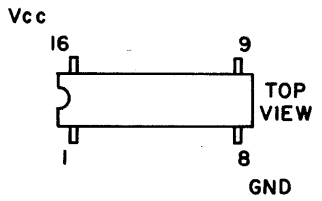
The 532 circuit is a priority encoder that accepts eight active-low inputs and produces a binary weighted output code reflecting the highest-order input. A weight is assigned to each active-low input so that when two or more inputs are simultaneously active, only the input with the highest weight is represented on the output. Weight priorities are in descending order with input 7 having the highest weight. An active-low input enable (pin 5) and an active-low output enable (pin 15) are provided to expand priority encoding to more inputs.

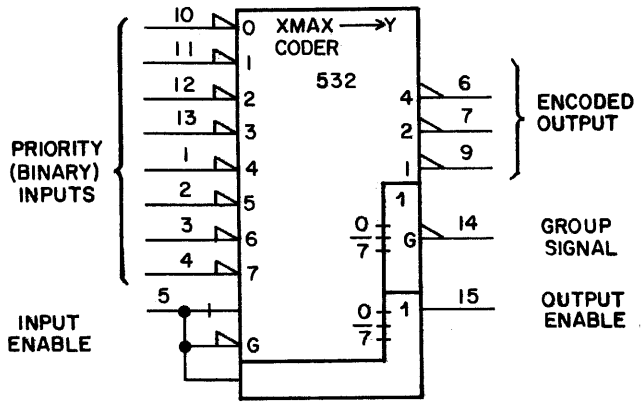
A group signal output (pin 14) will be low if any input is low. This active-low output differentiates between a case where there is no active input and the case where only the lowest-priority input (pin 10) is active, since both of these cases cause the three encoded output pins to go high.

Pin 15 is low when all inputs are high. Using the output enable along with the input enable allows priority encoding of N input signals. Both pin 15 and pin 14 are inactive (high) when the input enable is high.

NOTES:

1. Vendor identification: 9318
2. Package pin configuration.





LOGIC SYMBOL

INPUT									OUTPUT				
5	10	11	12	13	1	2	3	4	14	9	7	6	15
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = EITHER HIGH OR LOW VOLTAGE LEVEL

TRUTH TABLE

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Rev B
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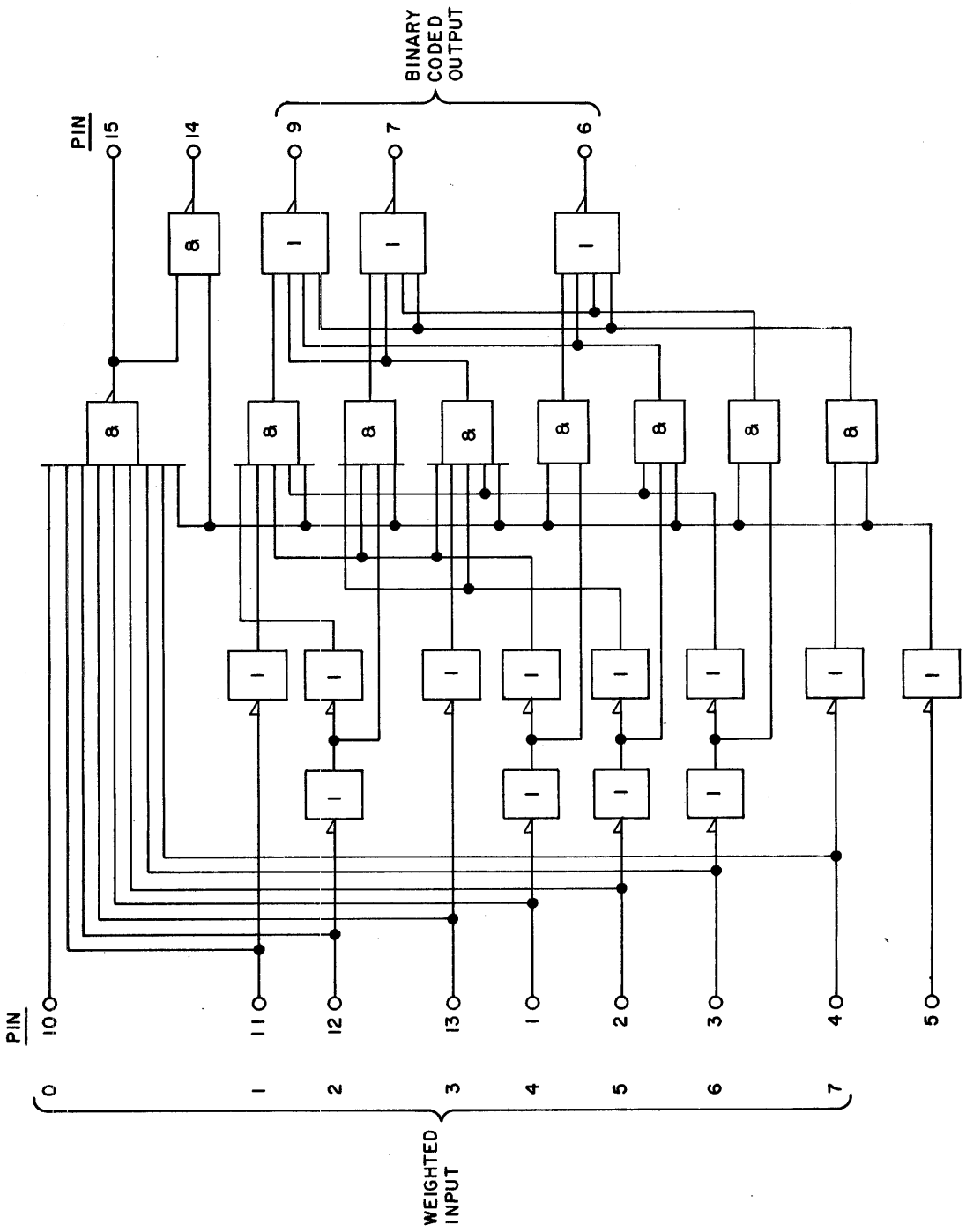

FUNCTION DIAGRAM

532
Rev C
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DESCRIPTION

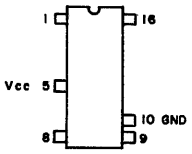
The 537 circuit is a binary counter capable of either 4-bit or 3-bit operation. (See functional diagram and truth tables on sheet 2.) As a 4-bit counter, pin 12 is connected to pin 1, and pin 14 is used as the count-pulse input. For 3-bit operation, pins 12 and 14 are not used, the count pulse being brought in on pin 1.

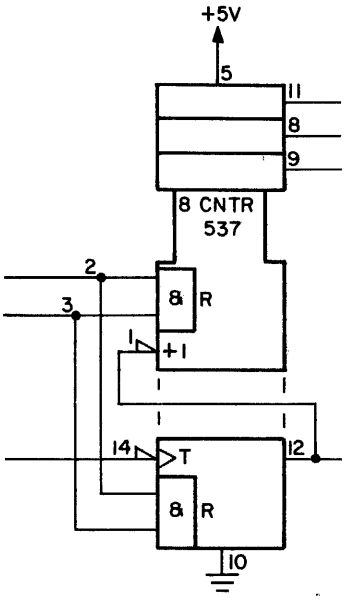
The count advances on the negative-going edge of the input pulse,,provided that the counter is enabled by a low level or either of the Reset inputs, pins 2 and 3.

During 3-bit operation, the toggle-input FF may be used independently, provided that its Reset function coincides with that of the octal counter.

NOTES:

1. Vendor identification: 7493
2. Package pin configuration:





LOGIC SYMBOL

NOTE

If the toggle-input FF is used independently, the Element Identifier is repeated within the FF symbol.

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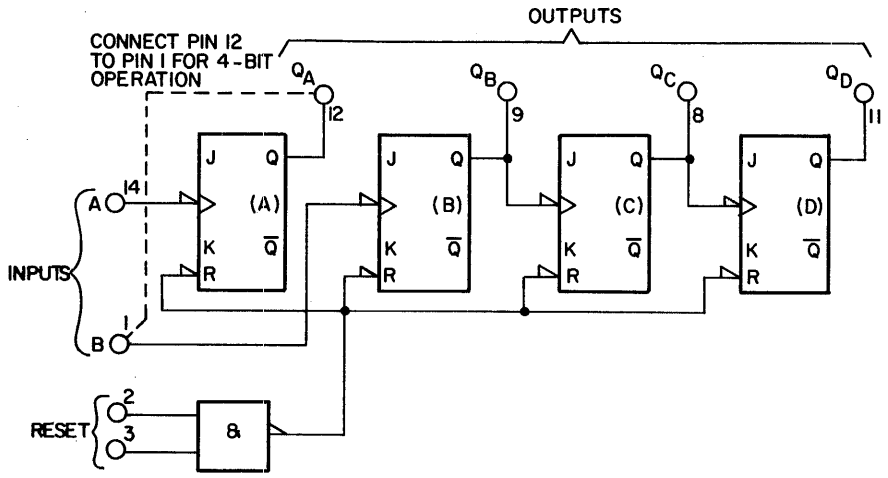


FUNCTIONAL DIAGRAM

COUNT	OUTPUTS			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

4-BIT OPERATION, INPUT A
(CONNECT Q_A TO INPUT B)

COUNT	OUTPUTS		
	Q_D	Q_C	Q_B
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H
4	H	L	L
5	H	L	H
6	H	H	L
7	H	H	H

3-BIT OPERATION, INPUT B
(INPUT A AND OUTPUT Q_A UNUSED)

TRUTH TABLES

DESCRIPTION

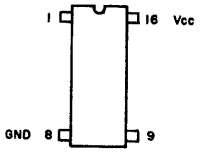
Element 538 is a dual 1-of-4 decoder with low-active outputs.

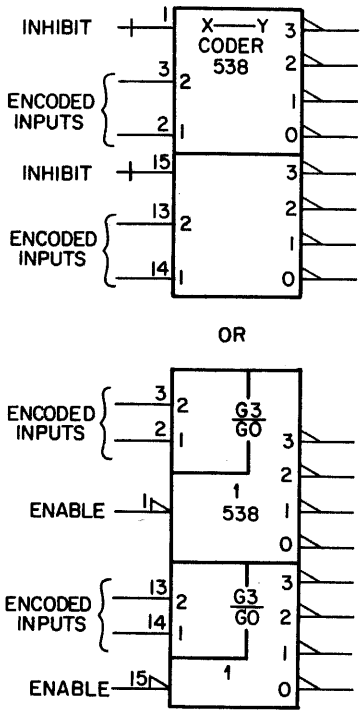
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
538	9321
538S	74S139
538LS	74LS139

3. Package pin configuration:





LOGIC SYMBOL

INPUTS			OUTPUTS			
INH/ ENA	1	2	0	1	2	3
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

TRUTH TABLE

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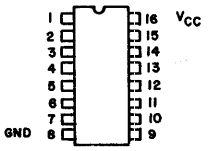
Rev A
Sheet 1 of 1

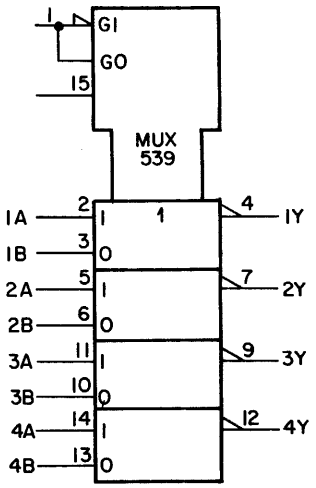
DESCRIPTION

The 539S circuit is a quad, 2-to-1 selector/ multiplexer with inverting outputs that act in accordance with the truth table at the right.

NOTES:

1. Vendor identification: 74S158
2. Package pin configuration:





LOGIC SYMBOL

INPUTS				OUTPUT
ENABLE	SELECT	A	B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

TRUTH TABLE

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Rev A
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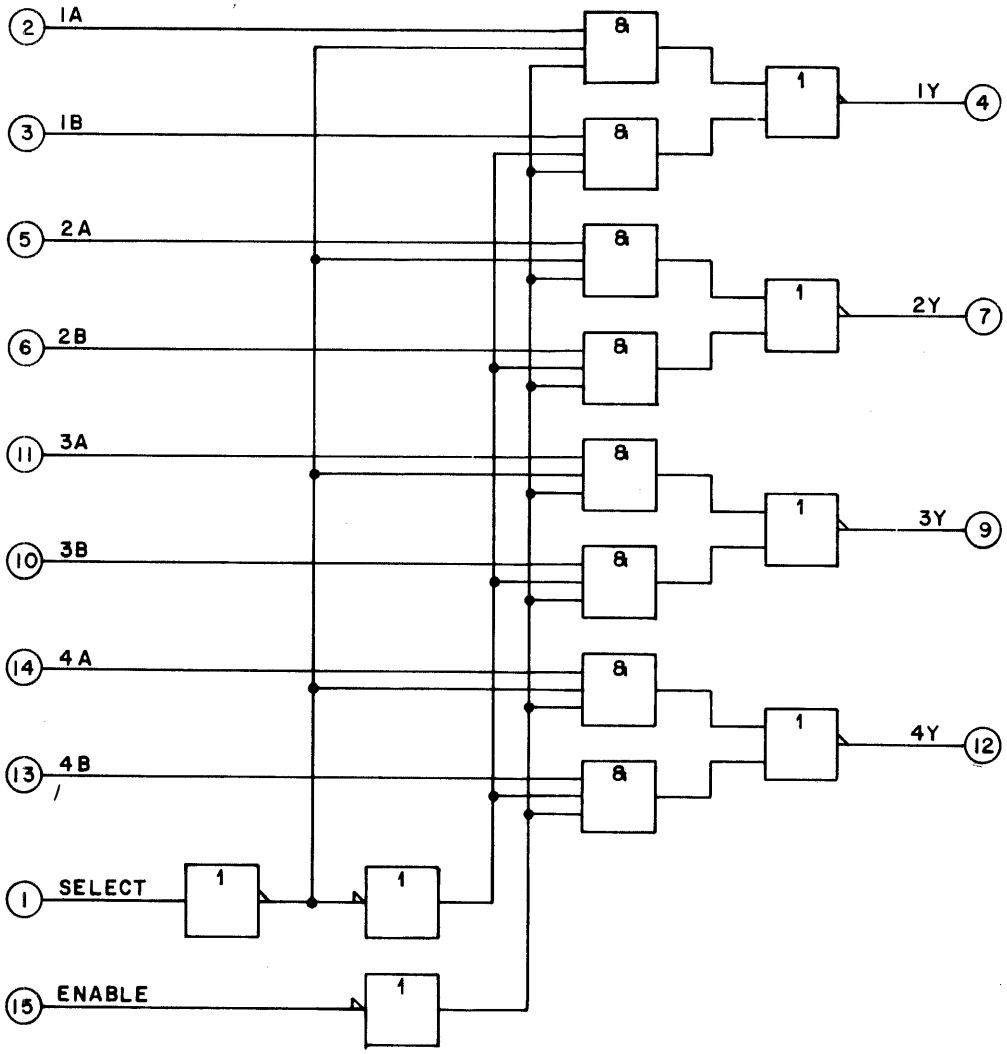

FUNCTIONAL DIAGRAM

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DESCRIPTION

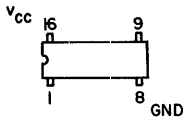
The 542 circuit is a tri-state, dual 4-to-1 multiplexer. The two binary select inputs are common to both sections. A separate strobe line for each section holds the output of that section in the Hi-Z state when the strobe input is high.

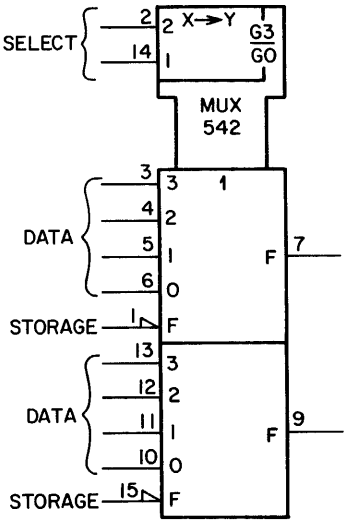
The tri-state feature allows the outputs from as many as 128 sections to be connected, providing a 512-line-to-1-line multiplexing function. Appropriate control of the select and strobe inputs then converts the data from parallel-in to serial-out.

Figure 1 shows two 542 ICs connected in this manner to serialize 16 data input bits.

NOTES:

1. Vendor identification: DM8214
2. Package pin configuration:





LOGIC SYMBOL

INPUTS							OUT-PUT
DATA				SELECT		STROBE	
0	1	2	3	2	1	F	
X	X	X	X	X	X	H	HI-Z
0	X	X	X	0	0	L	0
1	X	X	X	0	0	L	1
X	0	X	X	0	1	L	0
X	1	X	X	0	1	L	1
X	X	0	X	1	0	L	0
X	X	1	X	1	0	L	1
X	X	X	0	1	1	L	0
X	X	X	1	1	1	L	1

TRUTH TABLE
(ONE SECTION)

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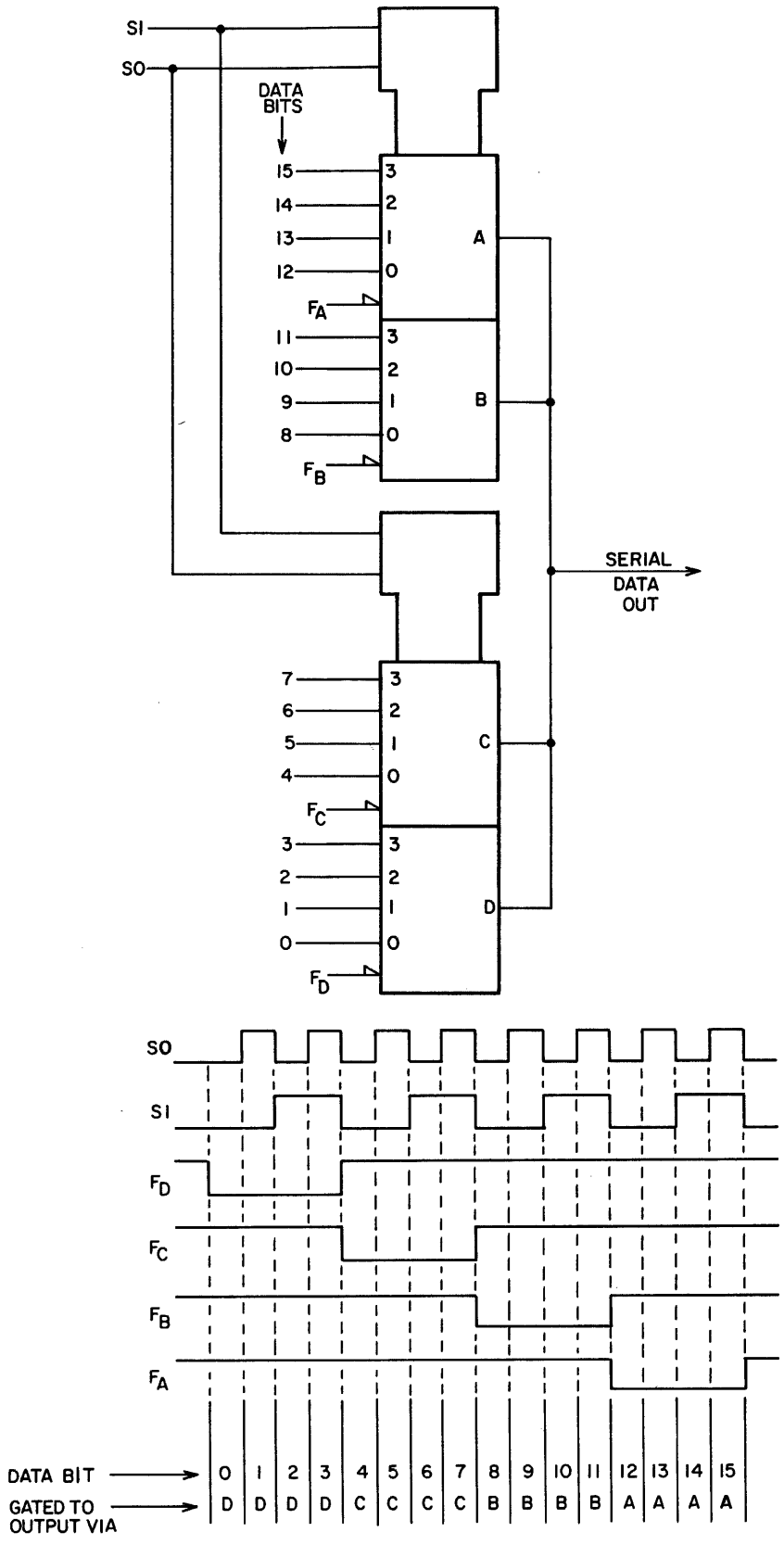

Figure 1 Serializing 16 Data Bits

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Rev A
Sheet 2 of 2

DESCRIPTION

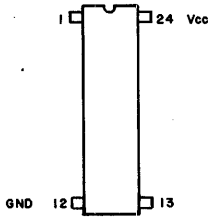
Element 543 is an 8-bit parallel/serial-in, parallel-out shift register. Loading and shifting is accomplished on the positive-going edge of the clock pusse, provided that the clock enable input is held low. Neither loading nor shifting is possible when the clock enable input is high.

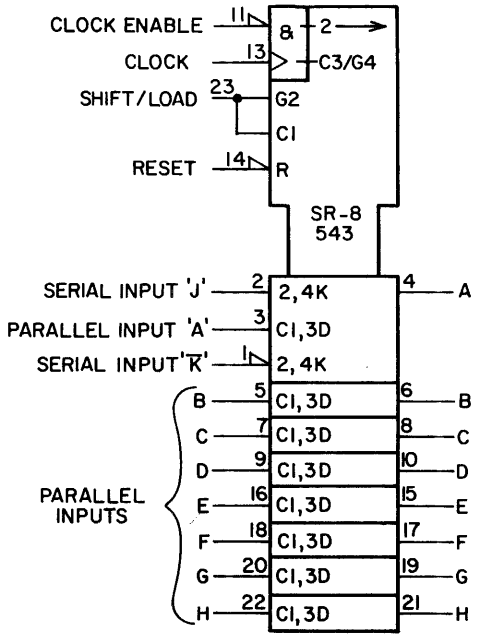
For shifting, the shift/load input must be high. During shifting, serial data is entered at the J-$\overline{K}$ inputs. See the J-$\overline{K}$ truth table for states needed to enter data into the first FF stage.

For parallel loading, the shift/load input must be low. Serial data flow is inhibited during loading.

NOTES:

1. Vendor identification: 74199
2. Package pin configuration:





LOGIC SYMBOL

INPUTS AT tn		OUTPUT AT tn + 1
J	$\overline{K}$	QA
L	H	QAn
L	L	L
H	H	H
H	L	$\overline{QAn}$

tn = BIT TIME BEFORE CLOCK PULSE

tn+1 = BIT TIME AFTER CLOCK PULSE

J-$\overline{K}$ TRUTH TABLE

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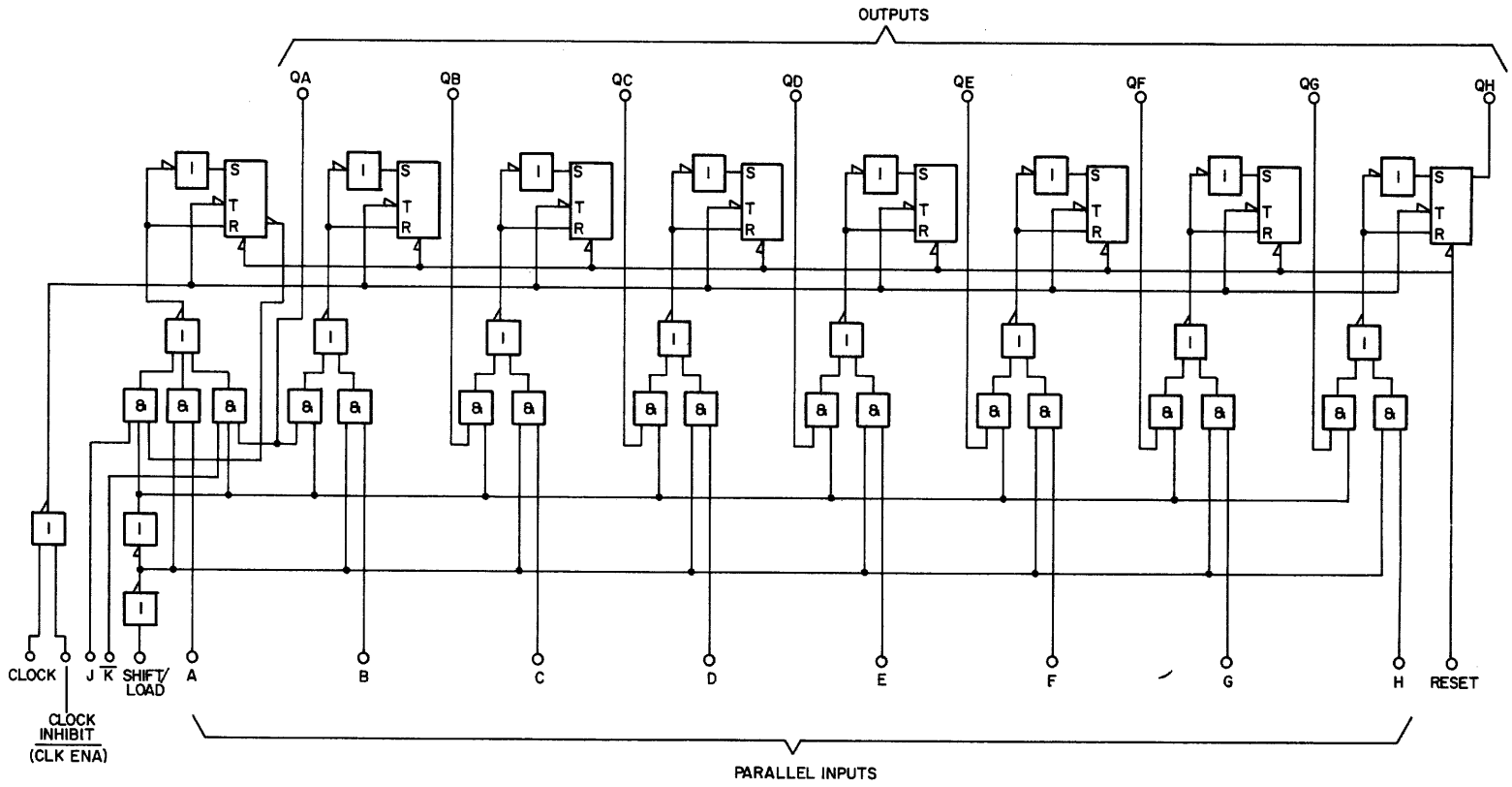
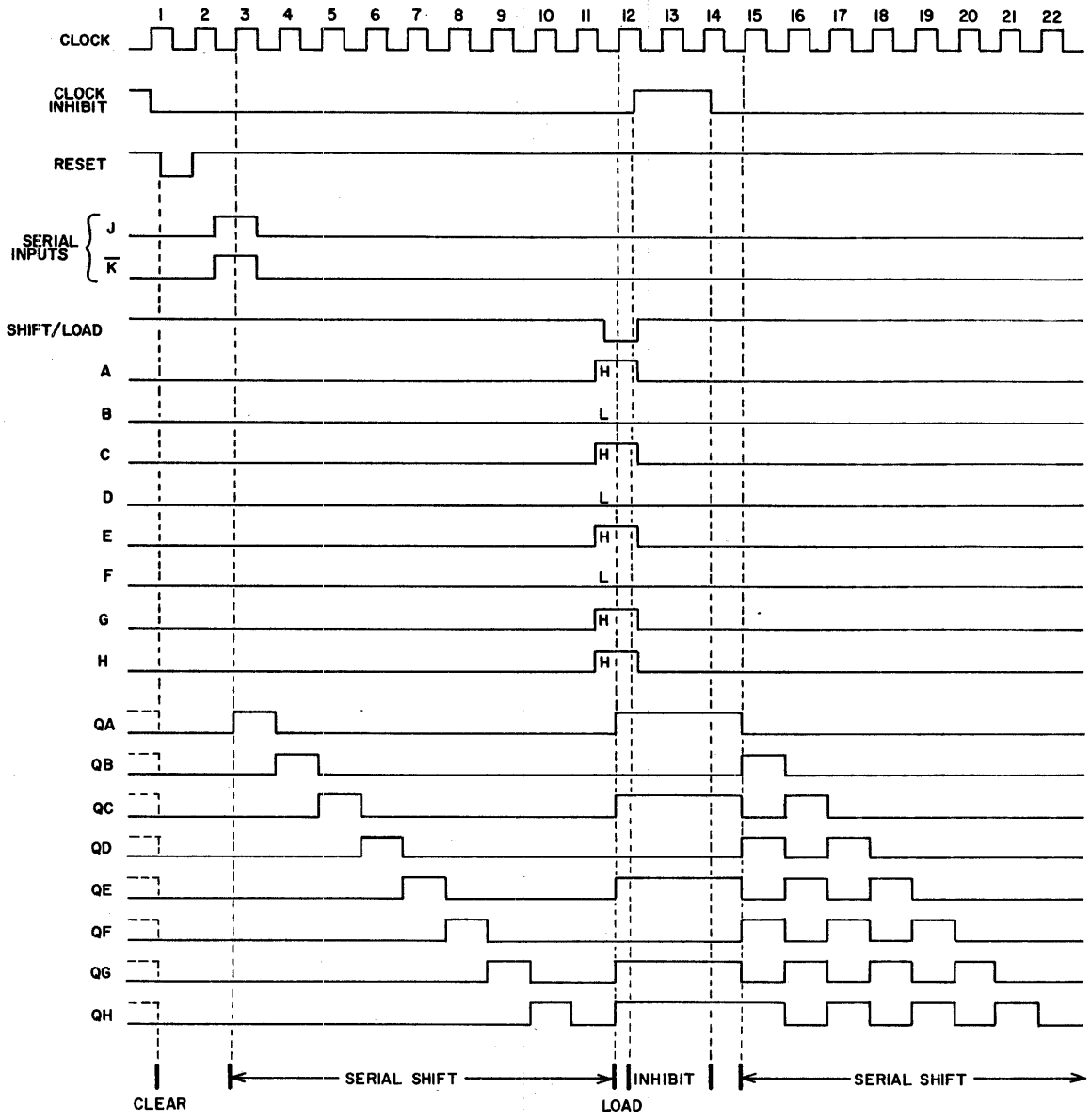


FUNCTIONAL DIAGRAM



TIMING DIAGRAM

543
Rev A
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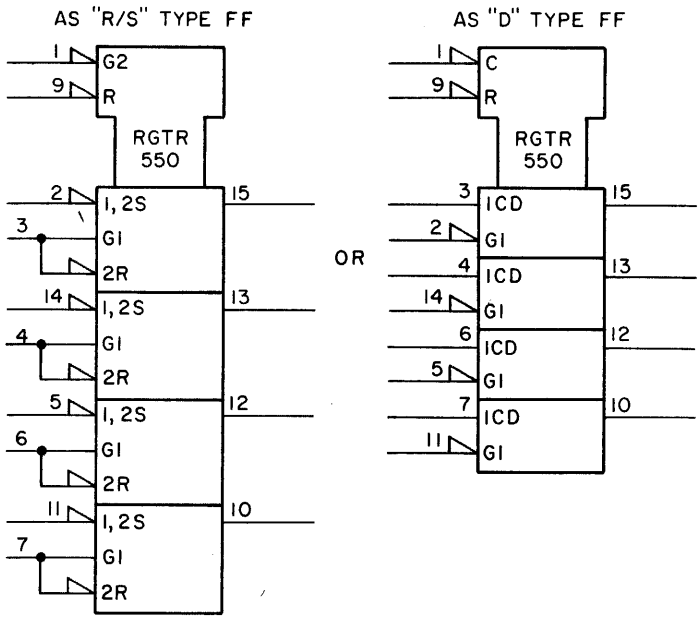
DESCRIPTION

The 550 circuit is a 4-bit latch. It can be used as single input D latches or set/reset latches. The four latches have a common active low enable and an active low master reset. When the common enable goes high, data present in the latches is stored and the state of a latch is no longer affected by the not S and D inputs. The master reset, when activated, overrides all other input conditions forcing all latch outputs low.

Each of the four latches can be operated in one of two modes: D-type latch or set/reset latch. For D-type operation the not S input of a latch is held low. While the common enable is active the latch output follows the D input. Information present at the latch output is stored in the latch when the enable goes high. During set/reset operation, when the common enable is low, a latch is reset by a low on the D input, and can be set by a low on the not S input if the D input is high. If both not S and D inputs are low, the D input will dominate and the latch will be reset. When the enable goes high, the latch remains in the last state prior to the low to high transition.



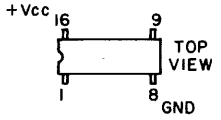
LOGIC SYMBOL

NOTES:

1. Vendor identifications:

Element	Vendor Number
550	9314

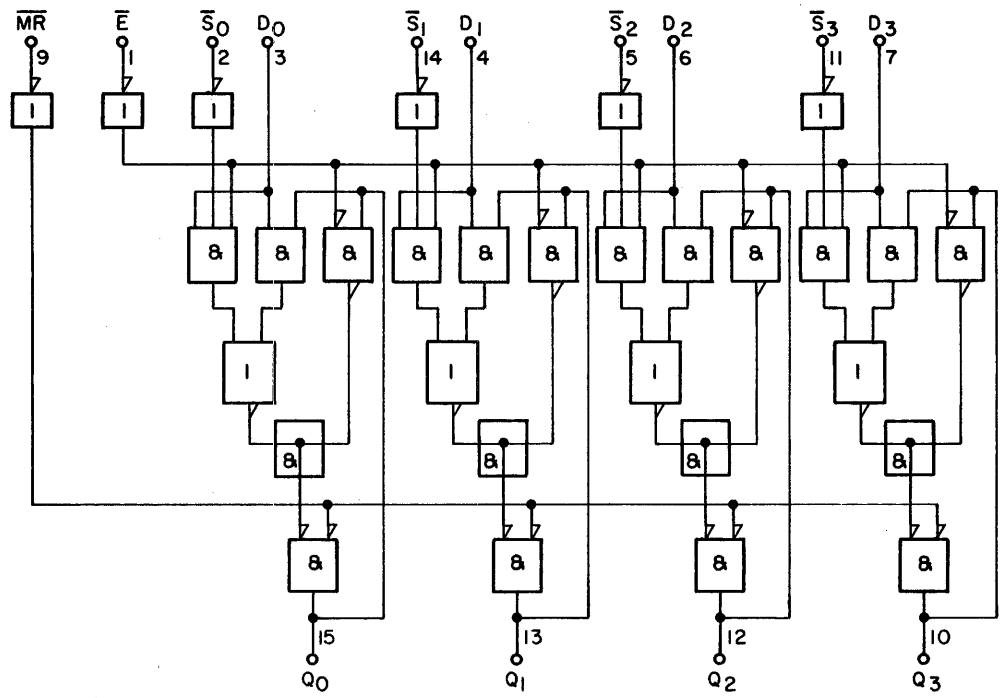
2. Package pin configuration.



$\overline{MR}$	$\overline{E}$	D	$\overline{S}$	Q_N	OPERATION
H	L	L	L	L	D MODE
H	L	H	L	H	
H	H	X	X	Q_{N-1}	
H	L	L	L	L	R/S MODE
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	Q_{N-1}	
H	H	X	X	Q_{N-1}	
L	X	X	X	L	RESET

X = DON'T CARE
L = LOW VOLTAGE LEVEL
H = HIGH VOLTAGE LEVEL
Q_{N-1} = PREVIOUS OUTPUT STATE
Q_N = PRESENT OUTPUT STATE

TRUTH TABLE



FUNCTION DIAGRAM

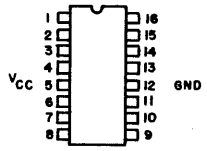
550
Rev B
Sheet 2 of 2

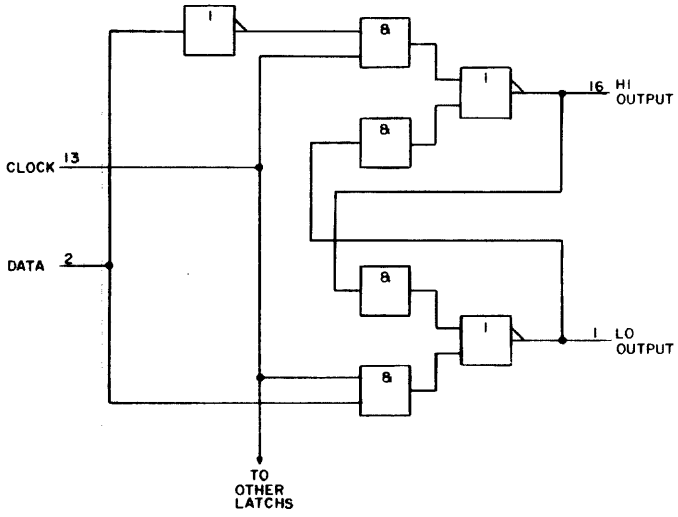
DESCRIPTION

The 551 latch may be used as a temporary storage device for binary information. Information present at a data (D) input is transferred to the high output when the clock is high. The high output follows the data input as long as the clock remains high. When the clock goes low, the information that was present at the data input at the time the transition occurred is retained at the high output until the clock goes high. The latch has complementary high and low outputs.

NOTES:

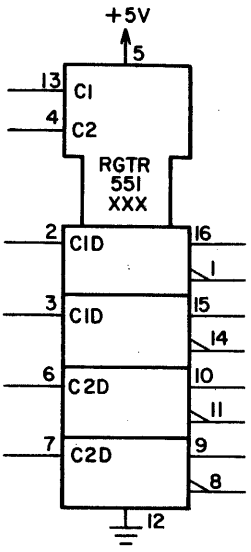
1. Vendor identification: 7475
2. Package pin configuration:





NOTE: LOGIC DIAGRAM FOR ONE LATCH ONLY

FUNCTIONAL DIAGRAM



LOGIC SYMBOL

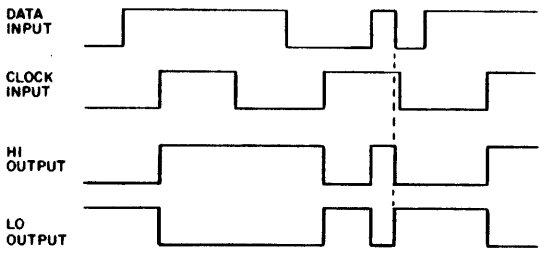
EACH LATCH

Tn	Tn + 1
DATA	HI OUTPUT
H	H
L	L

Tn = BIT TIME BEFORE NEGATIVE-GOING TRANSITION OF CLOCK

Tn + 1 = BIT TIME AFTER NEGATIVE-GOING TRANSITION OF CLOCK

TRUTH TABLE



TIMING DIAGRAM

551
Rev A
Sheet 1 of 1

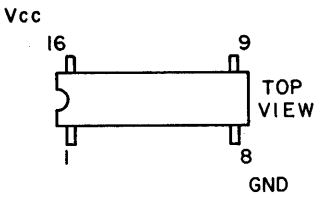
DESCRIPTION

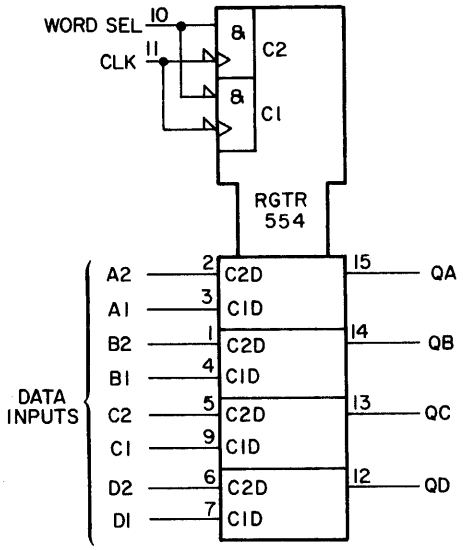
The 554 circuit is a 1-of-2 selector/multiplexer with storage. Data is entered into the R-S flipflops on the negative-going clock transition. Data set-up time is approximately 15 nsec; word select set-up time is approximately 25 nsec. Data gated to the FF outputs by the clock signal remains there until the next clock transition. The FFs are not directly resettable.

NOTES:

1. Vendor Identification: 74298

2. Package pin configuration.





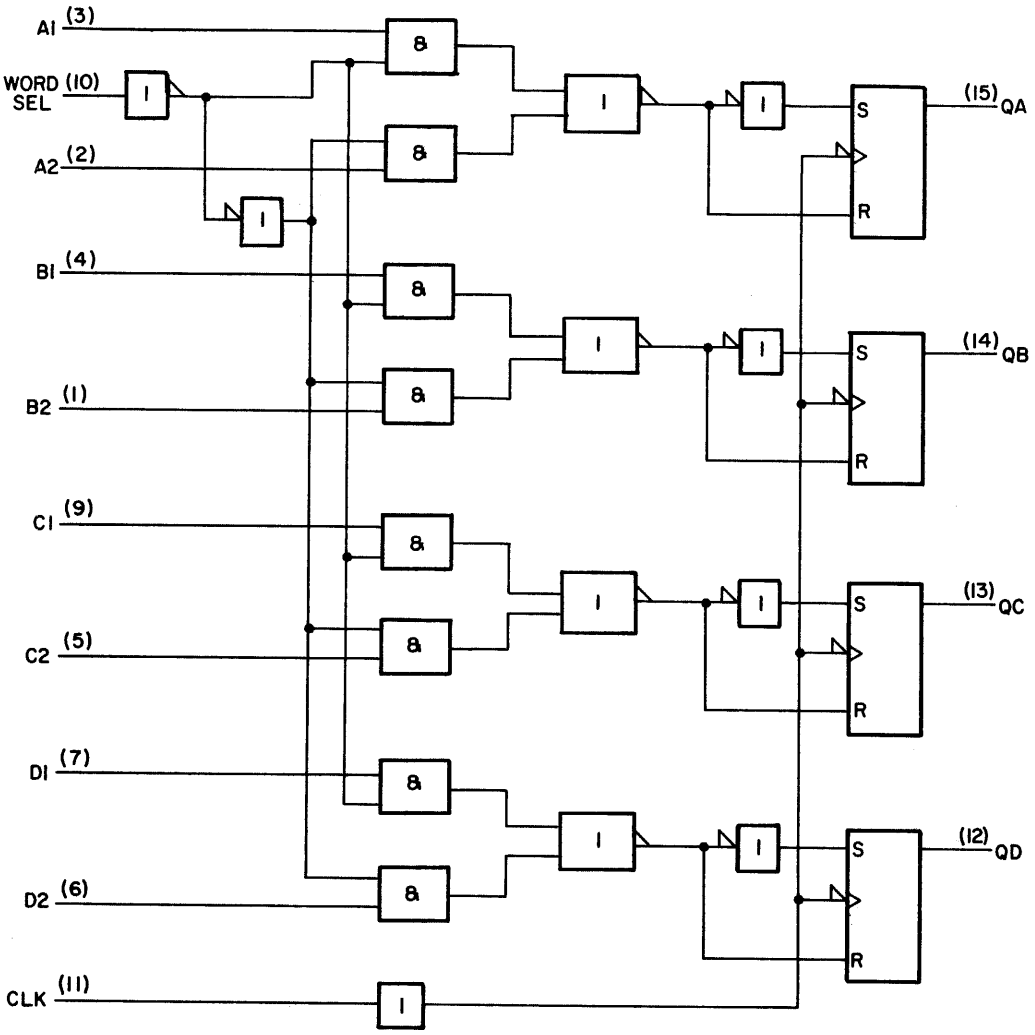
LOGIC SYMBOL

TRUTH TABLE

INPUTS		OUTPUTS			
WD SEL	CLK	QA	QB	QC	QD
L	↓	A1	B1	C1	D1
H	↓	A2	B2	C2	D2
X	H	QA0	QB0	QC0	QD0

L = low level, steady state
H = high level, steady state
↓ = transition from high to low level
X = irrelevant
A1,A2,etc. = steady-state level of data input signal
QA0,QB0,etc. = the level of QA,QB,etc. entered on last high-to-low transition of clock.

554
Rev. A
Sheet 1 of 2



PIN NUMBERS ARE IN PARENTHESES

LOGIC DIAGRAM

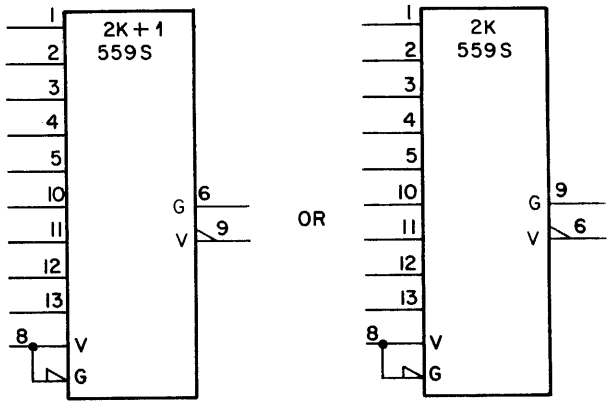
554
Rev. B
Sheet 2 of 2

DESCRIPTION

The 559S circuit is a 9-bit parity generator/ checker. This circuit is commonly used to generate a parity bit (if necessary) which is transmitted along with the associated data word. This circuit can also be used as a parity checker indicating that data has been received correctly or that an error has been detected.

Referring to the functional (logic) diagram, note that if an odd number of inputs are high, the odd output is high (the even output is low). If an even number of inputs are high, the even output is high (the odd output is low).

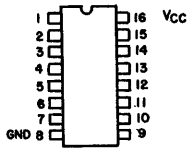
A high on the inhibit input (pin 8) forces both outputs low).

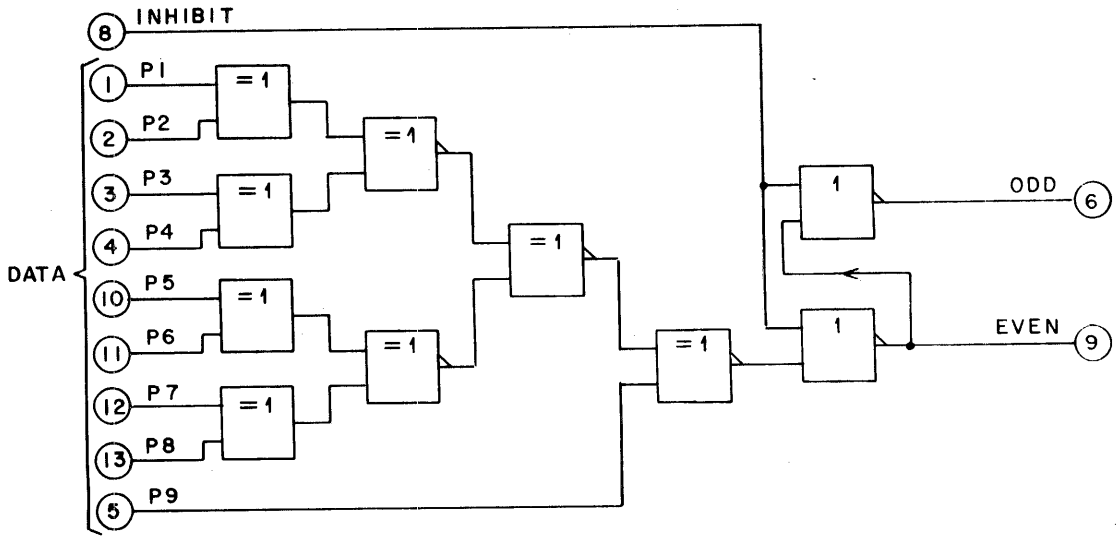


LOGIC SYMBOL

NOTES:

1. Vendor identification: 82S62
2. Package pin configuration:





FUNCTIONAL DIAGRAM

559
Rev B
Sheet 1 of 1

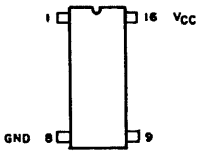
DESCRIPTION

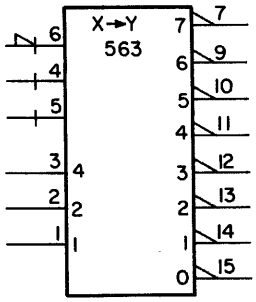
Element 563LS is a 3-to-8-line decoder that also functions as a 1-to-8-line demultiplexer. One active-high and two active-low enable inputs reduce the need for external inverters when cascading for larger words. (See example on sheet 3.)

An enable input can be used as a data input when demultiplexing.

NOTES:

1. Vendor identification: 74LS138
2. Package pin configuration:





LOGIC SYMBOL

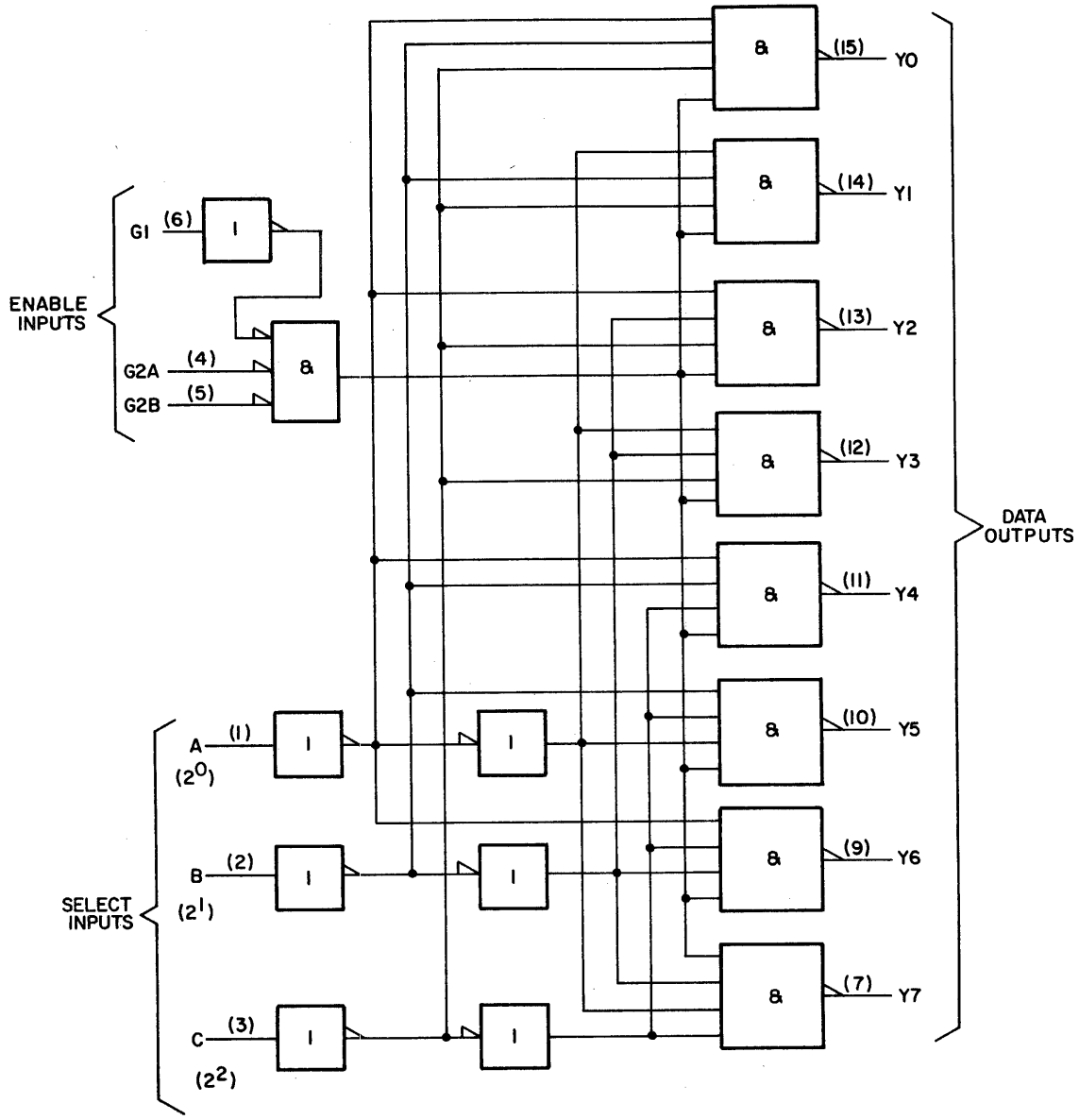
INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H = High, L = Low, X = Irrelevant

* G2 = G2A & G2B

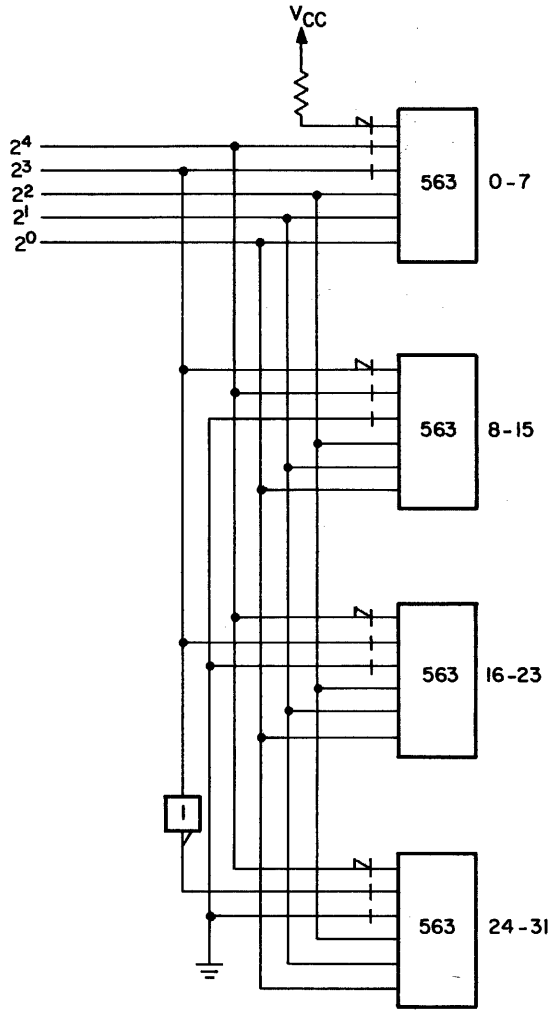
Input/output labels refer to functional diagram on sheet 2.

TRUTH TABLE



FUNCTIONAL DIAGRAM

	"ENABLE" INPUTS				
	2^4	2^3	2^2	2^1	2^0
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0
21	1	0	1	0	1
22	1	0	1	1	0
23	1	0	1	1	1
24	1	1	0	0	0
25	1	1	0	0	1
26	1	1	0	1	0
27	1	1	0	1	1
28	1	1	1	0	0
29	1	1	1	0	1
30	1	1	1	1	0
31	1	1	1	1	1



CASCADING FOR 5-TO-32-LINE DECODE

563
Rev A
Sheet 3 of 3

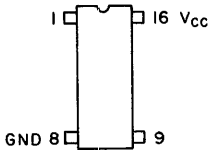
DESCRIPTION

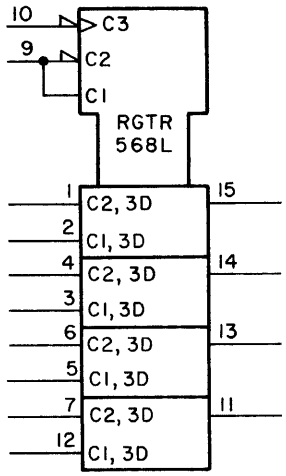
Element 568L is a 4-bit wide, 2-word data selector with storage properties. If the Word select input (pin 9) is low, Word 1 inputs (C1, 3D) are selected. When pin 9 is high, Word 2 inputs (C2, 3D) are selected.

The selected 4-bit word is stored in four S-R masterslave FFs and passed to the outputs on the negative-going edge of the clock (pin 10). Stored data is then available until the next high-to-low transition of the clock.

NOTES

1. Vendor identification: 74L98
2. Package pin configuration:





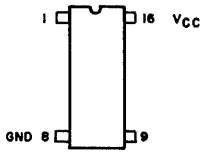
LOGIC SYMBOL

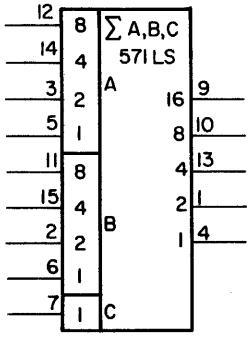
DESCRIPTION

The 571LS circuit is a 4-bit binary full adder, featuring a full look-ahead that generates a fast carry in 10 ns, typically. See sheets 2 and 3 for function table and functional diagram.

NOTES:

1. Vendor identification: 75LS283
2. Package pin configuration:





LOGIC SYMBOL

571
Rev B
Sheet 1 of 3

INPUT				OUTPUT					
				WHEN CO = L			WHEN CO = H		
						WHEN C2 = L			WHEN C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ4	Σ2 / Σ8	C2 / C4	Σ1 / Σ4	Σ2 / Σ8	C2 / C4
L	L	L	L	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = High, L = Low

C0 = Carry in (pin 7)

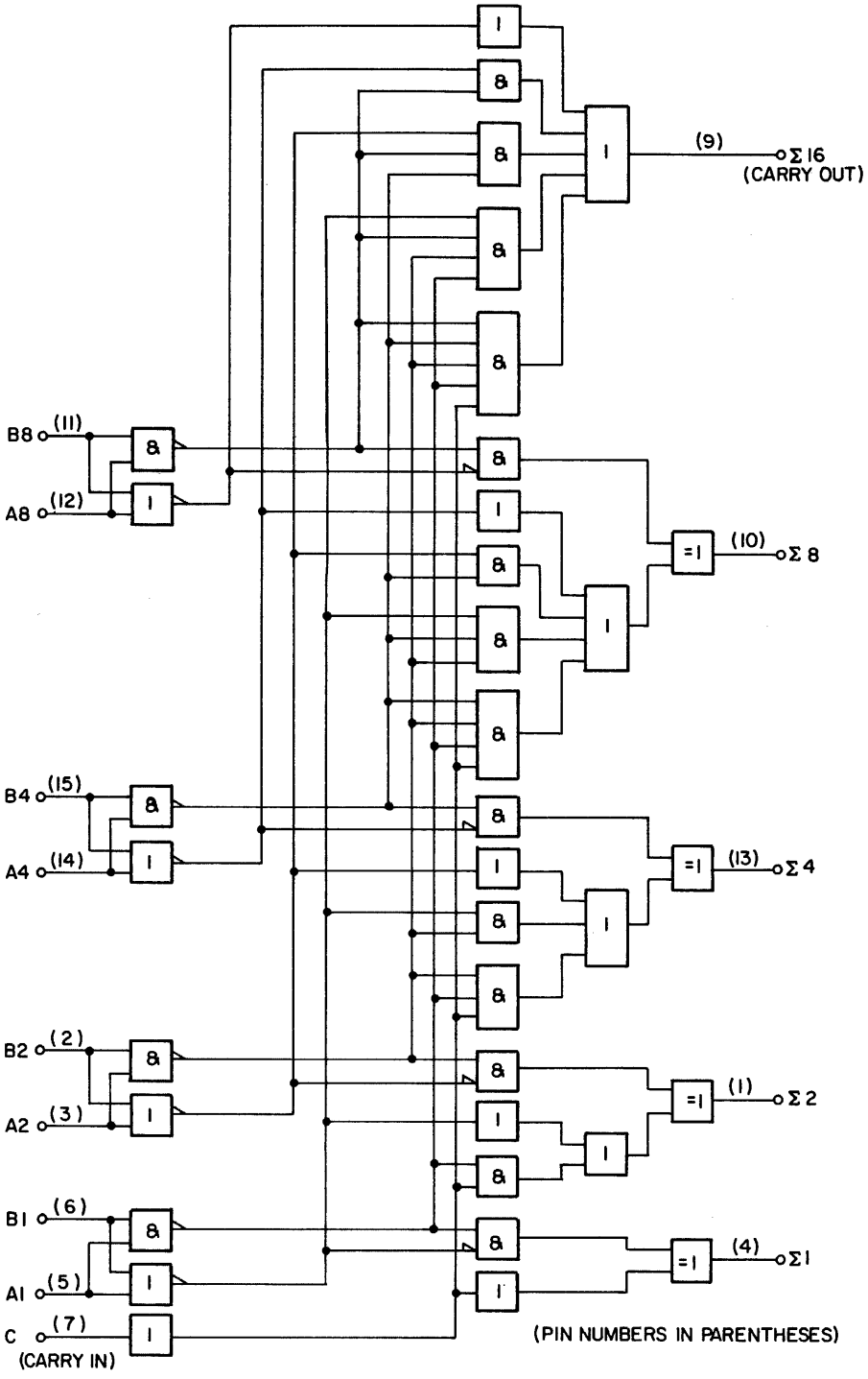
C2 = Internal carry

C4 = Carry out (E16, pin 9)

NOTE

Input conditions at A1, B1, A2, B2 and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry, C2. The values at C2, A3, B3, A4 and B4 then determine outputs Σ4, Σ8, and C4 (Σ16).

FUNCTION TABLE



FUNCTIONAL DIAGRAM

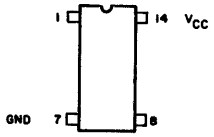
571
Rev A
Sheet 3 of 3

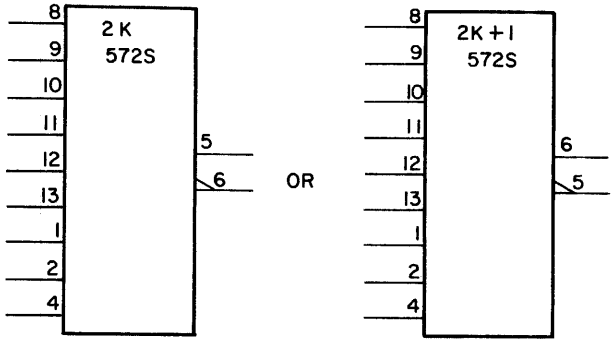
DESCRIPTION

Element 572S is a nine-bit parity generator/ checker. These devices can be eascaded to provide parity for up to 81-bit words in typically 25 ns.

Notes:

1. Vendor identification: 74S280
2. Package pin configuration:





LOGIC SYMBOL

NUMBER OF INPUTS THAT ARE HIGH	OUTPUTS	
	EVEN (5)	OOD (6)
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

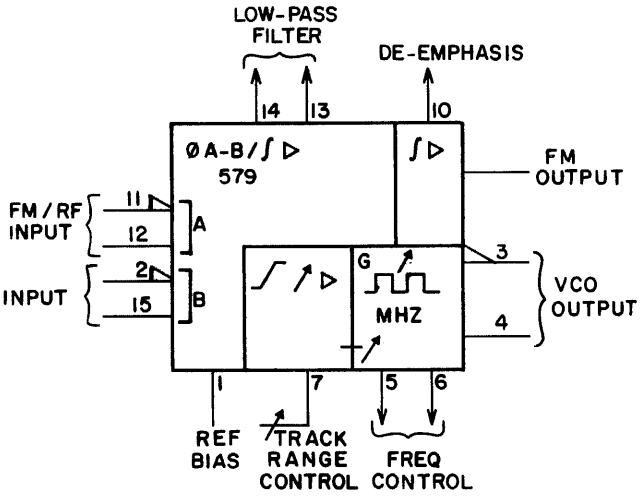
TRUTH TABLE

572
Rev A
Sheet 1 of 1

DESCRIPTION

The 579 phase-locked loop (PLL) is a monolithic signal conditioner and demodulator system. As shown in the block diagram on sheet 2, the PLL comprises a VCO (voltage-controlled oscillator), phase comparator, amplifier and low-pass filter. The center frequency of the PLL is determined by the free-running frequency (fo) of the VCO. This VCO frequency is set by an external capacitor attached to the Frequency Control, pins 5 and 6. The low-pass filter, which determines the capture characteristics of the loop, is formed by an external RC network connecting pins 13 and 14.

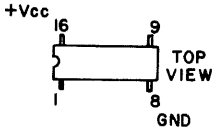
The 579 has two sets of differential inputs, one for the FM/RF input and one for the phase comparator input. Both sets of inputs can be used in either a differential or single-ended mode. The FM/RF inputs to the comparator are self-biased. An internally regulated voltage source (pin 1) is provided to bias the phase comparator inputs. The VCO output, at high level and in differential form, is available for driving logic circuits in signal conditioning and synchronization, frequency multiplication and division application. Pin 7 is provided for the optional extension of the tracking range.



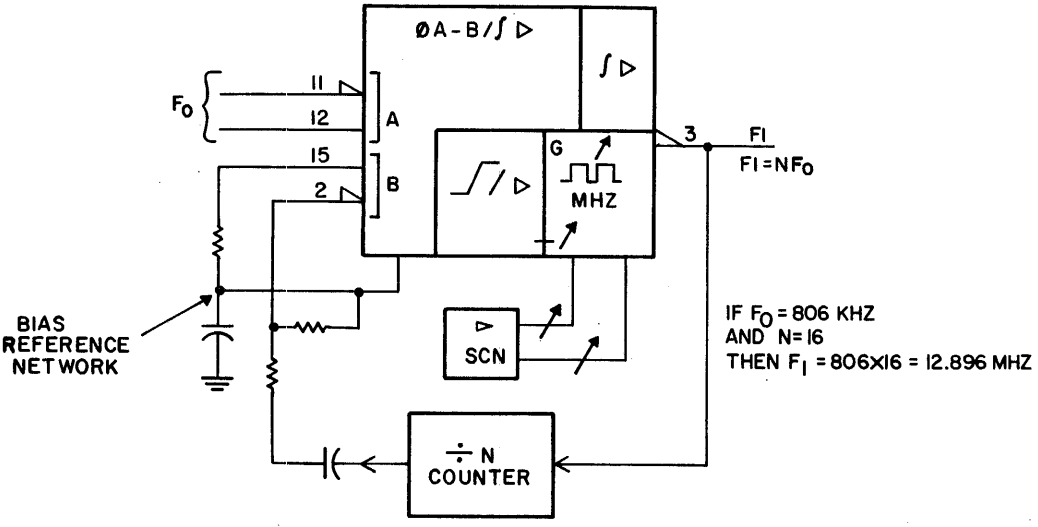
LOGIC SYMBOL

NOTES:

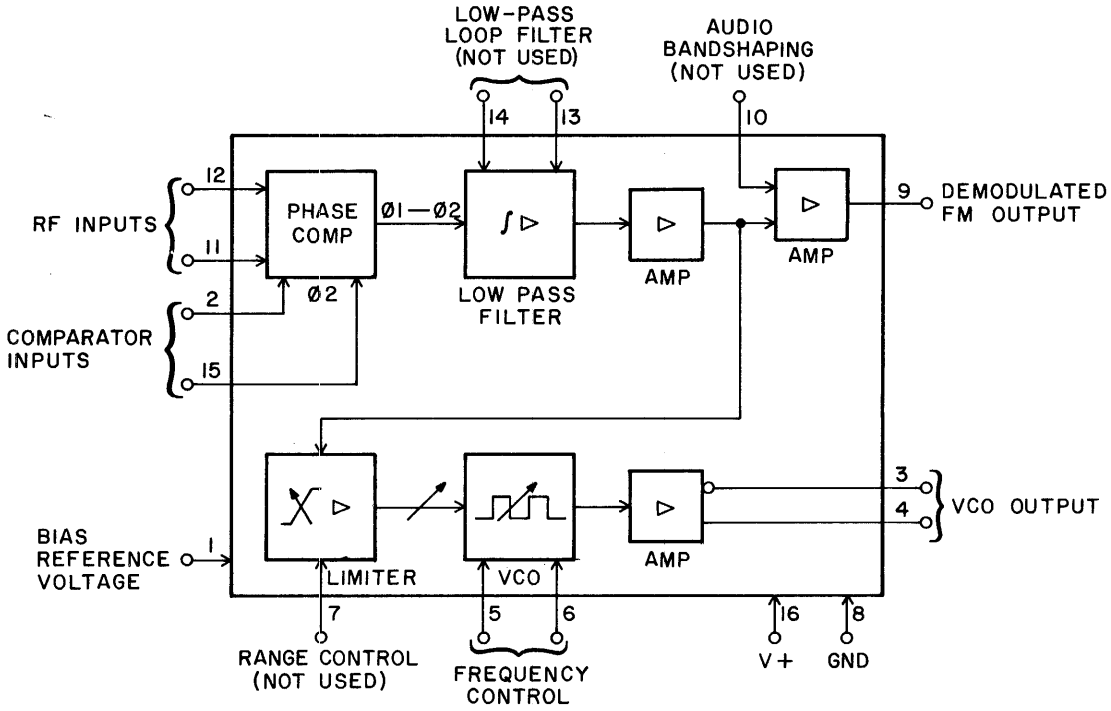
1. Vendor identification: 562B
2. Package pin configuration.



579
Rev B
Sheet 1 of 2



APPLICATION



BLOCK DIAGRAM

579
Rev B
Sheet 2 of 2

DESCRIPTION

The 581 circuit is a phase-frequency detector. This device contains two digital phase detectors, an emitter follower amplifier, and a charge pump circuit that converts TTL inputs to a dc voltage for use in frequency discrimination and phase-locked-loop applications.

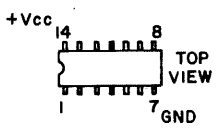
The two phase detectors have common inputs. Phase-frequency detector A is locked in (indicated by both outputs high) when the negative transitions of the variable input (pin 3) and the reference input (pin 1) are equal in frequency and phase. If the variable input is lower in frequency or lags in phase, output pin 13 goes low; conversely, output pin 2 goes low when the variable input is higher in frequency or leads the reference input in phase. The variable and reference inputs to phase detector A are not affected by duty cycles because negative transitions control operations.

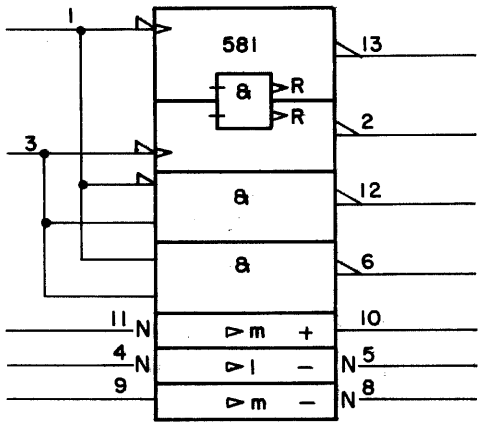
Phase detector B is locked in when the variable input phase lags the reference phase by 90° (indicated by output pins 6 and 12 alternately going low with equal pulse widths). If the variable input lags by more than 90°, pin 12 will remain low longer than pin 6. Conversely, if the variable input phase lags the reference phase by less than 90°, pin 6 remains low longer. In phase detector B, the variable input and the reference input must have 50% duty cycles.

The charge pump accepts the phase detector outputs and converts them to fixed-amplitude positive and negative pulses.

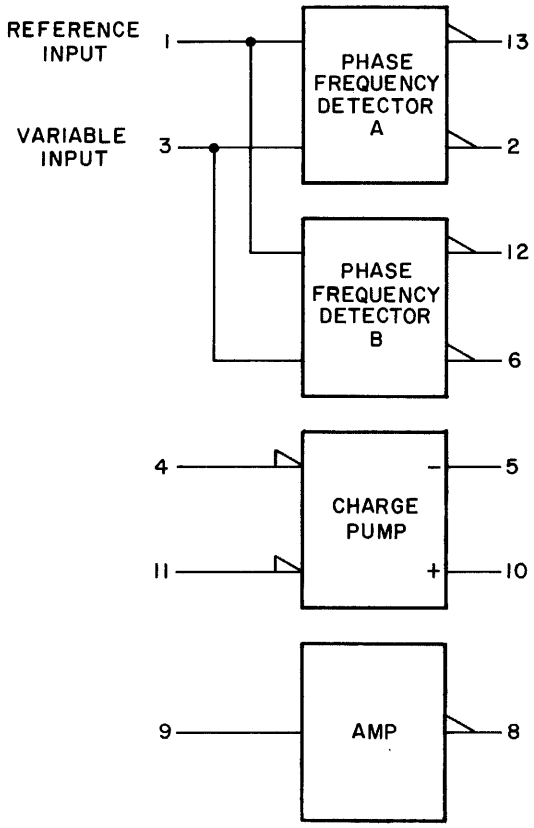
NOTES:

1. Vendor identification: 4044, 4344
2. Package pin configuration.





LOGIC SYMBOL



FUNCTION DIAGRAM

581
Rev B
Sheet 1 of 1

DESCRIPTION

The 582 circuit is a dual voltage-controlled multivibrator. The dc control input on pins 2 and 12 determines the precise frequency of the multivibrator. The value of the external capacitor between pins 3 and 4 or 10 and 11 determines the operating frequency range. Variation of the output frequency over a 3.5 to 1 range is possible with an input dc control voltage of +1.0 to +5.0 volts. The value of the external capacitor may be determined by either of two equations:

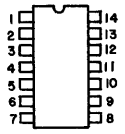
$$C = \frac{500}{F\ max}\ uF \text{ or } C = \frac{100}{F\ min}\ uF,$$

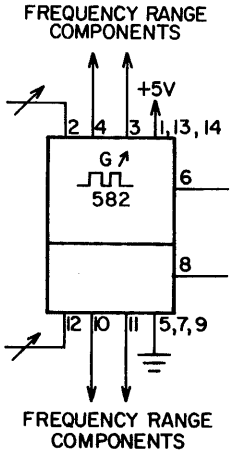
with F given in hertz. The maximum operation frequency is 30 megahertz.

The 582 has three power and three ground connections. Each multivibrator has its separate power (pins 1 and 13) and ground (pins 5 and 9) connection. The two output buffers have a common power (pin 14) and ground (pin 7) connections. All grounds must always be connected. The output buffer transforms the logic levels.

NOTES:

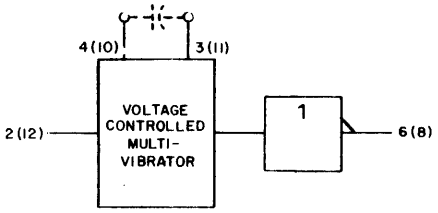
1. Symbol sections may appear separately.
2. Vendor identification: MC4024
3. Package pin configuration:





LOGIC SYMBOL

NOTE: Lines to pins 2 and 12 could be thus: —X— , —/— , or —↗— depending upon whether the input is analog or non-logic level, non-standard logic level, or from a variable parameter control, respectively.



FUNCTIONAL DIAGRAM

FIGURE 1
INPUT VOLTAGE VERSUS OUTPUT FREQUENCY
(15pF FEEDBACK CAPACITOR)

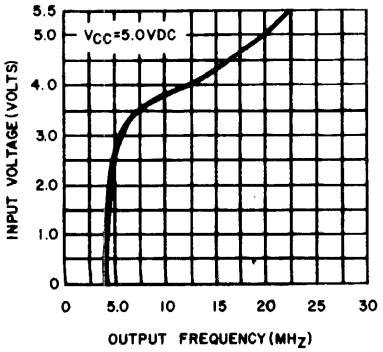


FIGURE 2
INPUT VOLTAGE VERSUS OUTPUT FREQUENCY
(100pF FEEDBACK CAPACITOR)

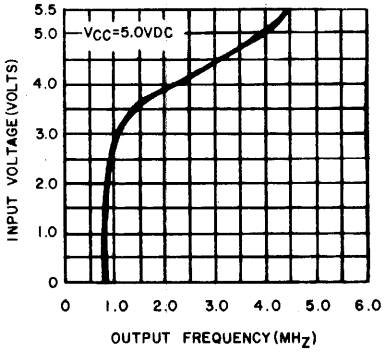
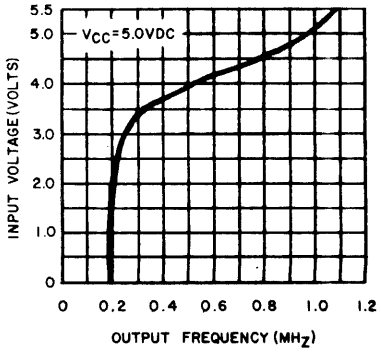


FIGURE 3
INPUT VOLTAGE VERSUS OUTPUT FREQUENCY
(430pF FEEDBACK CAPACITOR)



582
Rev A
Sheet 1 of 1

DESCRIPTION

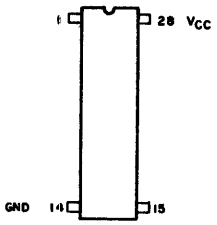
Element 768 is a 576-bit random access memory, organized as 64 words of 9 bits each. Input data appears at the open-collector outputs in inverted form.

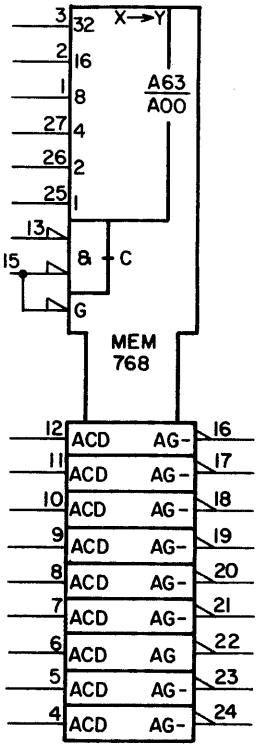
Data is written when pins 13 and 15 are both low. Data is read when pin 15 is low and pin 13 is high. Access time is typically 30 ns.

NOTES:

1. Vendor identification:

2. Package pin configuration:





LOGIC SYMBOL

768
Rev A
Sheet 1 of 1

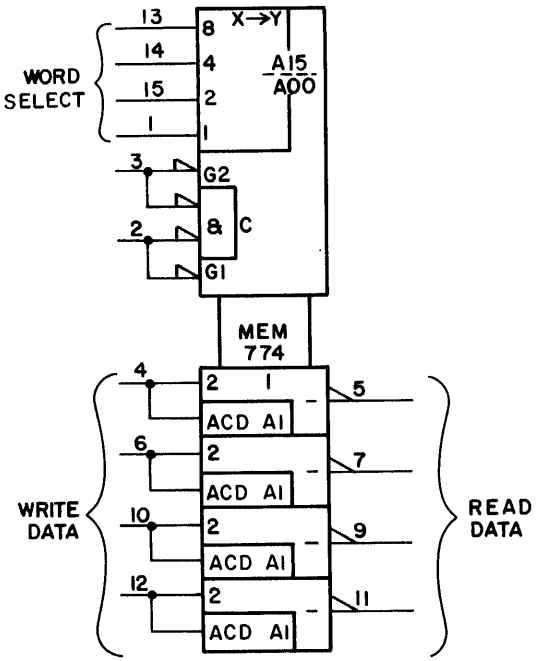
DESCRIPTION

The 774 is a TTL 64-bit Read/Write Random Access Memory organized as 16 words of 4 bits each.

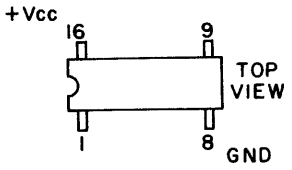
Words are selected through a 4-input binary decoder when the Chip Select input (2) is at logical 0. Data is written into the memory when Read Enable (3) is at logical 0 and read from the memory when pin 3 is at logical 1. The complement of the Write Data inputs is available at the Read Data outputs whenever Read Enable is a logical 0, regardless of the State of Chip Select.

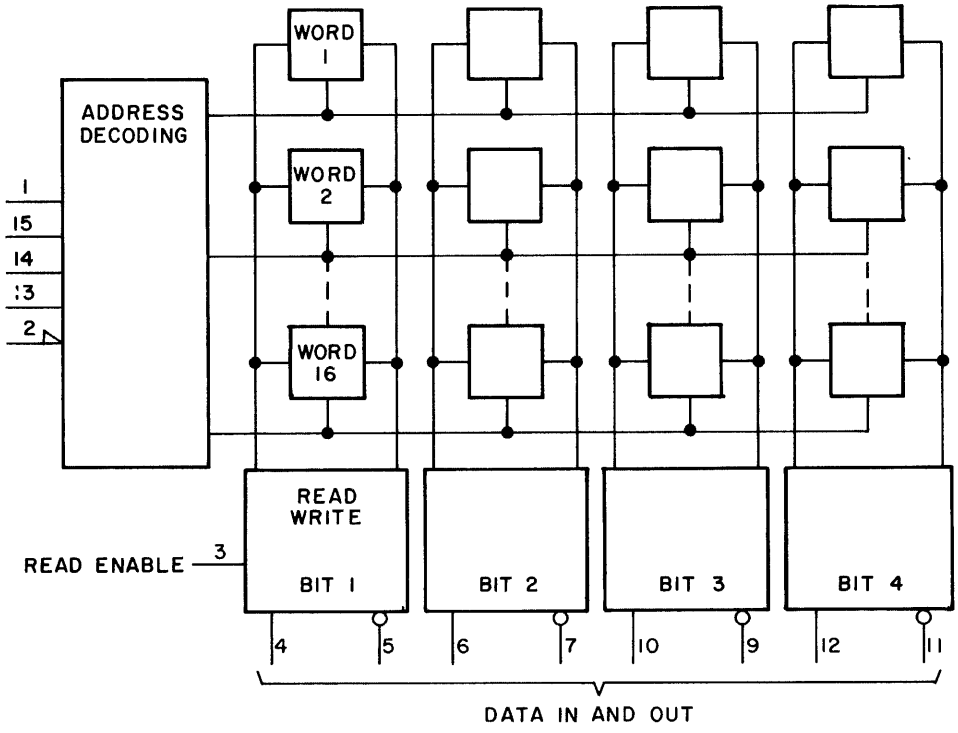
NOTES:

1. Vendor identification: 7489
2. Package pin configuration.



LOGIC SYMBOL





FUNCTION DIAGRAM

774
Rev B
Sheet 1 of 1

DESCRIPTION

The 775 circuit is a 256-bit read/write memory with a tri-state input. The inputs to this memory consist of eight address lines, a write enable and three memory enables (all three must be low to read from or write into a memory location). This memory provides three output states; high or low (depending on stored data) and a high-impedance state. The high-impedance state permits bus connecting to similar outputs.

A Write operation is performed by placing a low on the write enable input, a low on all three memory enable inputs and selecting a memory address. This stores the complement of the input data in the selected location.

A Read operation is performed by placing a high on the write enable input, a low on all three memory enable inputs and selecting a memory address. This places the complement of the stored information at the output.

The output is held in a high-impedance state when the write enable is low or if any one of the three memory enables is high

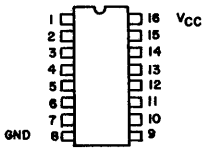
The two circuits (775 and 775A) are functionally identical except for cycle time.

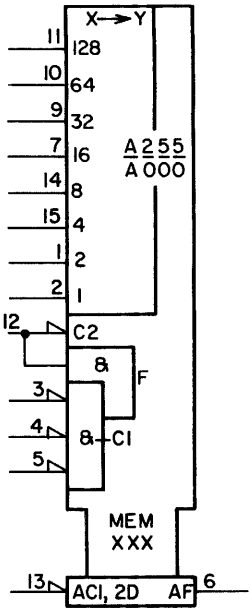
NOTES:

1. Vendor identification:

Element M	Vendor Number
775	74200
775A	82S06

2. Package pin configuration:





NOTE:
SEE FUNCTIONAL DIAGRAM FOR PIN FUNCTIONS

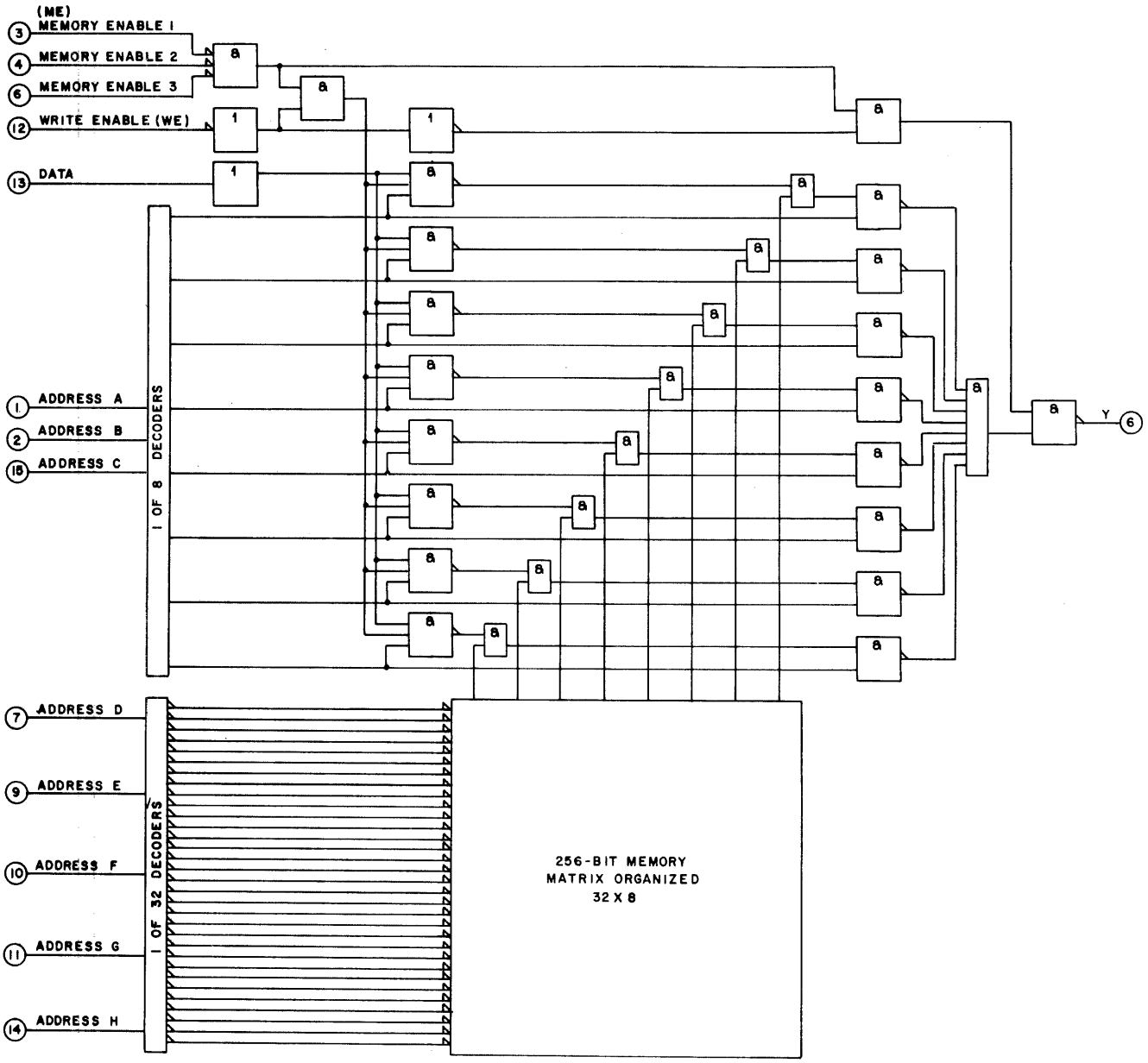
LOGIC SYMBOL

FUNCTION	INPUTS		OUTPUT
	MEMORY ENABLE*	WRITE ENABLE	
WRITE (STORE COMPLEMENT OF DATA)	L	L	HIGH IMPEDANCE
READ	L	H	STORED DATA
INHIBIT	H	X	HIGH IMPEDENCE

* FOR MEMORY ENABLE:
L = ALL ME INPUTS LOW
H = ONE OR MORE ME INPUTS HIGH

TRUTH TABLE

775
Rev A
Sheet 1 of 2



FUNCTION DIAGRAM

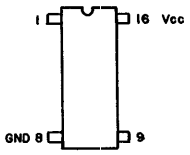
775
Rev A
Sheet 2 of 2

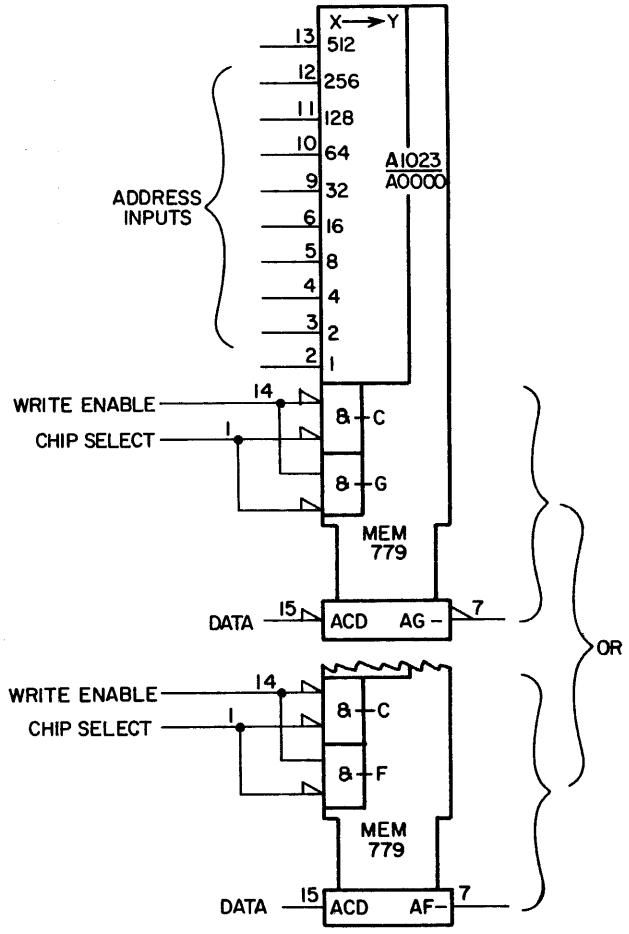
DESCRIPTION

Element 779 is a 1024-word by 1-bit (1024x1) random-access memory with an open-collector output. On-chip address selection is made when the Chip Select input goes low. Read and Write operations are controlled by the low-active Write Enable signal, as given in the truth table. Information read from the selected address is real (non-inverted) data. As in all open-collector elements, a pull-up resistor is required to provide a High output.

NOTES:

1. Vendor identification: 93415
2. Package pin configuration:





LOGIC SYMBOL

INPUTS			OUTPUT	MODE
CHIP SELECT	WRITE ENABLE	DATA (PIN 15)	PIN 7	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D	READ

D = DATA STORED AT SELECTED ADDRESS

TRUTH TABLE

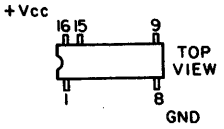
779
Rev A
Sheet 1 of 1

DESCRIPTION

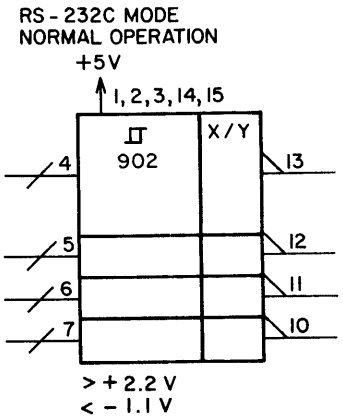
The 902 is a monolithic quadruple line receiver satisfying interface requirements for equipments as defined by EIA Standard RS-232C. The receiver is DTL/TTL compatible on inputs and inverting outputs.

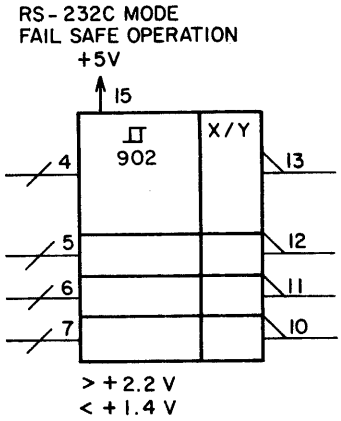
NOTES:

1. Vendor identification: 75154
2. Package pin configuration.

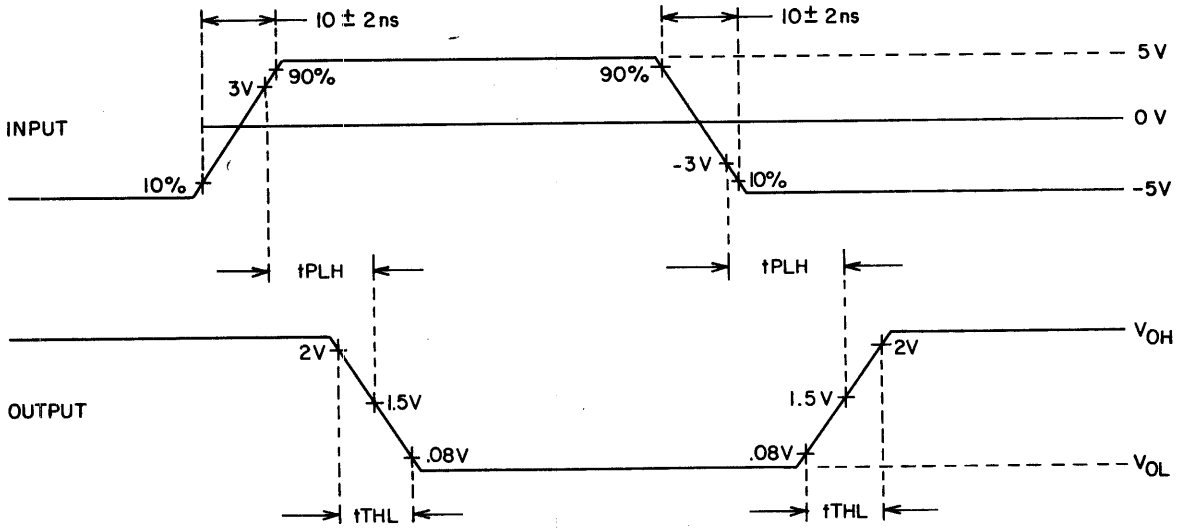


3. For normal operation connect threshold-control terminals to Vcc 1, pin 15.
4. For fail-safe operation threshold-control terminals are open.





LOGIC SYMBOLS



VOLTAGE WAVEFORMS

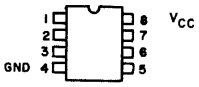
902
Rev. B
Sheet 1 of 1

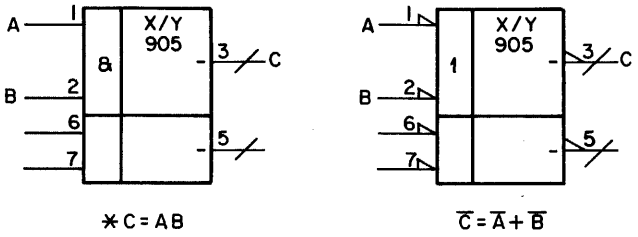
DESCRIPTION

The 905 circuit is a dual driver incorporating TTL logic with open-collector output. The output is low when either or both inputs are low. The output is I (indeterminate) when both inputs are high. When an external pull-up resistor is used the output is high, instead of I. The propagation delay from a low to a high output is typically 45 ns. The total power dissipation is 800 mW (continuous). The input threshold is approximately 1.4V. Output drive current in the low state is 150 mA. The input or output may be open or grounded for troubleshooting without damage to the chip.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 75451AP
3. Package pin configuration:





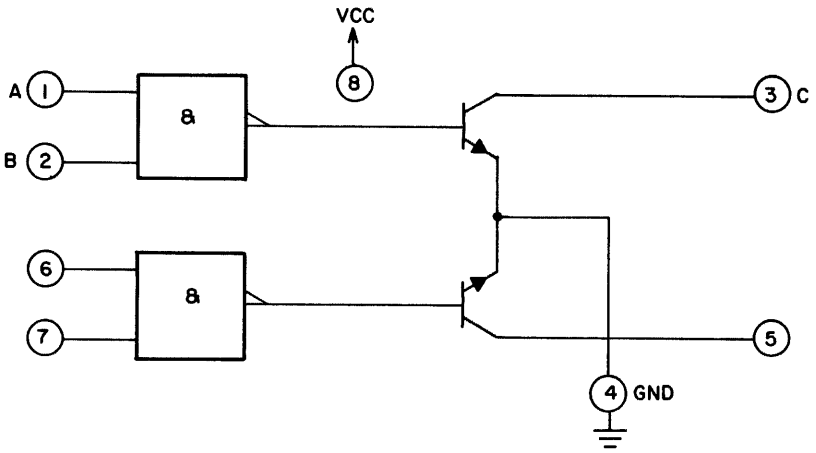
* Depends upon external output circuitry. A high is supplied when an external pull-up resistor is used in the output. The maximum voltage that the resistor can be connected to is 30 V.

LOGIC SYMBOL

INPUT PINS		OUTPUT PINS
A(1,6)	B(2,7)	C(3,5)
L	L	L
L	H	L
H	L	L
H	H	I

I=Indeterminate-the open-collector output supplies neither a high nor a low. A high is supplied when an external pull-up resistor is used in the output.

TRUTH TABLE



FUNCTIONAL DIAGRAM

905
Rev B
Sheet 1 of 1

DESCRIPTION

Element 909 is a dual differential-line driver featuring a 4-input positive AND gate.

NOTES:

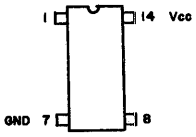
1. Symbol sections may appear separately.
2. Vendor identification:

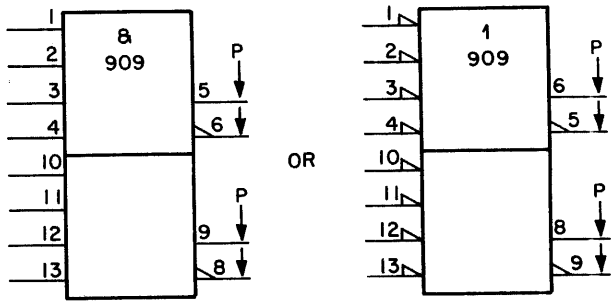
Element	Vendor Number
909	7830
909A	8830

3. Temperature range:

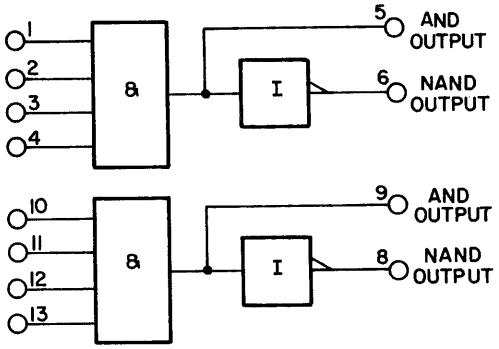
   909(7830): $-55^{o}C$ to $+125^{o}C$
   909A(8830): $0^{o}C$ to $70^{o}C$

4. Package pin configuration:





LOGIC SYMBOL

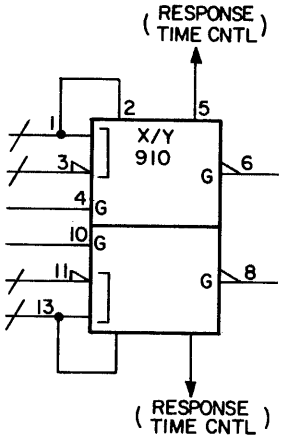


FUNCTIONAL DIAGRAM
(POSITIVE LOGIC)

909
Rev A
Sheet 1 of 1

DESCRIPTION

Element 910 is a dual differential-line receiver with an independent strobe (G) for each section. Response time can be controlled by an external capacitor to reject input noise spikes. The output is forced High if both differential input pins are open, or if the strobe is held Low.



LOGIC SYMBOL

NOTES:

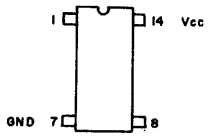
1. Symbol sections may appear separately.
2. Vendor identification:

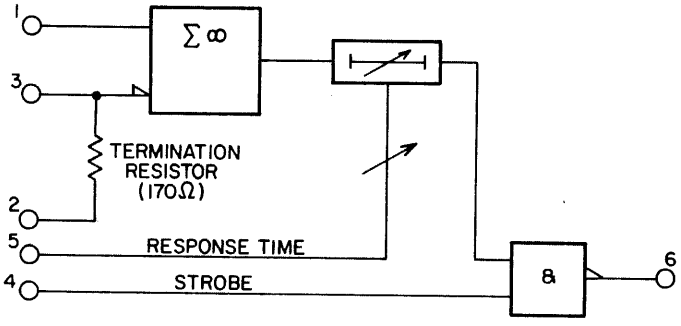
Element	Vendor Number
910	7820
910A	8820

3. Temperature range:

   910 (7820): $-55^{o}C$ to $+125^{o}C$.
   910A (8820): $0^{o}C$ to $+70^{o}C$.

4. Package pin configuration:





FUNCTIONAL DIAGRAM
(ONE SECTION)

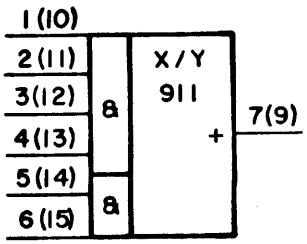
910
Rev B
Sheet 1 of 1

DESCRIPTION

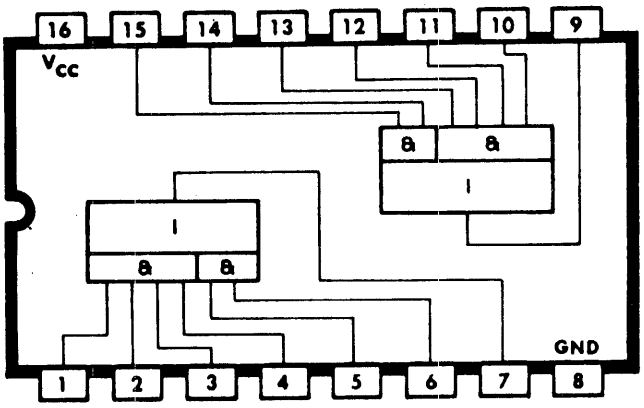
Element 911 consists of two dual input, non-inverting AND/OR line drivers mounted on a single chip.

NOTES:

1. Pin numbers in parentheses are for second section.
2. Sections may appear separately.
3. Vendor identification: 9743 (Honeywell)



LOGIC SYMBOL



PACKAGE PIN CONFIGURATION

	IN	OUT
0	0V	0V
1	3V	2.5–3.5V

LOGIC VOLTAGES

INPUT PINS						OUTPUT (PIN 7)
1	2	3	4	5	6	
1	1	1	1	X	X	1
X	X	X	X	1	1	1

X = DON'T CARE CONDITION
ALL OTHER INPUT CONDITIONS RESULT IN "0" OUTPUT

TRUTH TABLE

911
Rev B
Sheet 1 of 1

DESCRIPTION

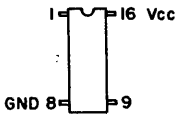
Element 912 consists of three line receivers mounted on a single chip.

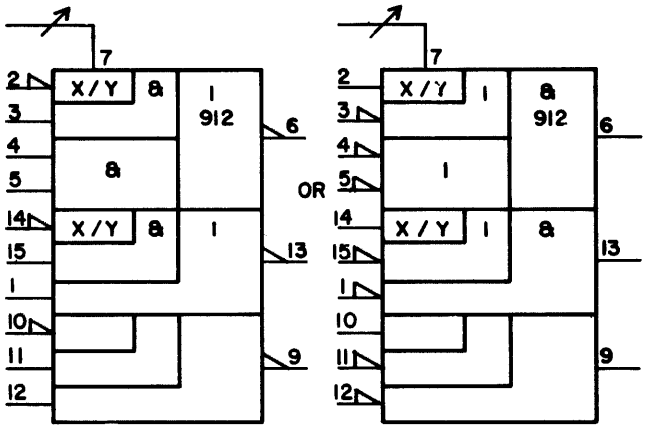
NOTES:

1. Symbol sections may appear separately.
2. Vendor identification:

Element	Vendor Number
912	9748
912R	9749

3. Package pin configuration:





LOGIC SYMBOLS

TRUTH TABLE

INPUT PINS										OUTPUT PINS					
										HI-ACTIVE			LO-ACTIVE		
14	15	1	2	3	4	5	10	11	12	13	6	9	13	6	9
L	H	X								L	–	–	H	–	–
X	X	H								L	–	–	H	–	–
			X	X	H	H				–	L	–	–	H	–
			L	H	X	X				–	L	–	–	H	–
							L	H	X	–	–	L	–	–	H
							X	X	H	–	–	L	–	–	H

L = LOW, H = HIGH, X = DON'T CARE
INPUT CONDITIONS OTHER THAN THOSE SHOWN RESULT IN "H" OUTPUT FOR HI-ACTIVE-OUT CONFIGURATION AND "L" OUTPUT FOR LO-ACTIVE-OUT CONFIGURATION.

LOGIC VOLTAGES

	INPUT (PINS 2, 10, 14)	OUTPUT
L	<1.5 V ± 0.2 V	0.5 V MAX
H	>1.5 V ± 0.2 V	3.0–3.9 V

912
Rev C
Sheet 1 of 1

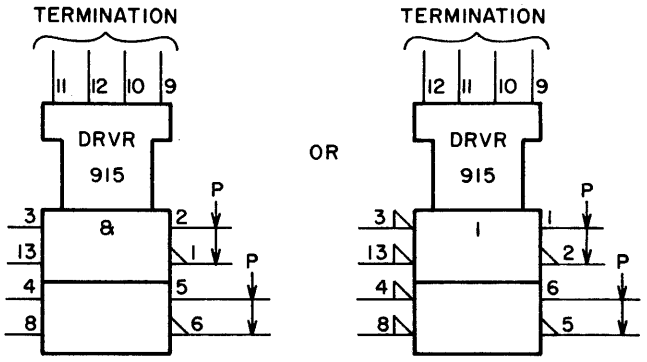
Sheet 1 of 1

DESCRIPTION

The 915 circuit consists of two monolithic TTL line drivers in one package. A 20-ohm, 1 percent resistor is connected between each of the TERMINATION pins (see logic symbol) and Vcc. Thus terminated, the relationship between the two inputs and the two outputs of either section are as follows (second-section pin numbers in parentheses):

a. With both inputs in a High state, pin 2(5) is at a higher potential than pin 1(6).

b. With either or both inputs in a Low state, pin 1(6) is at a higher potential than pin 2(5).

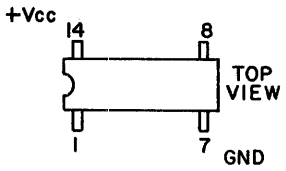


LOGIC SYMBOL

NOTES:

1. Vendor Identification: 5065989

2. Package pin configuration:



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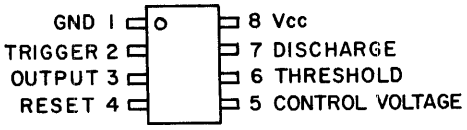
Rev. C
Sheet 1 of 1

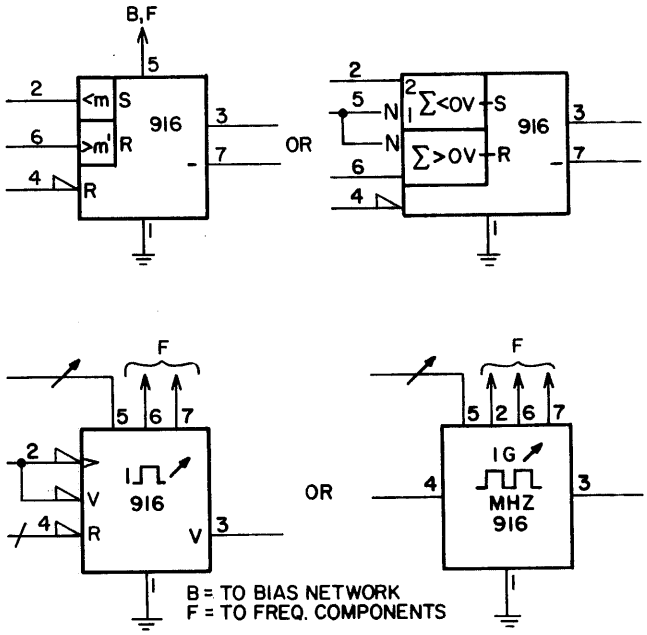
DESCRIPTION

The 916 circuit may be used as a one-shot, a free-running multivibrator, or a comparator-input FF. Descriptions are provided for each of these applications.

NOTES:

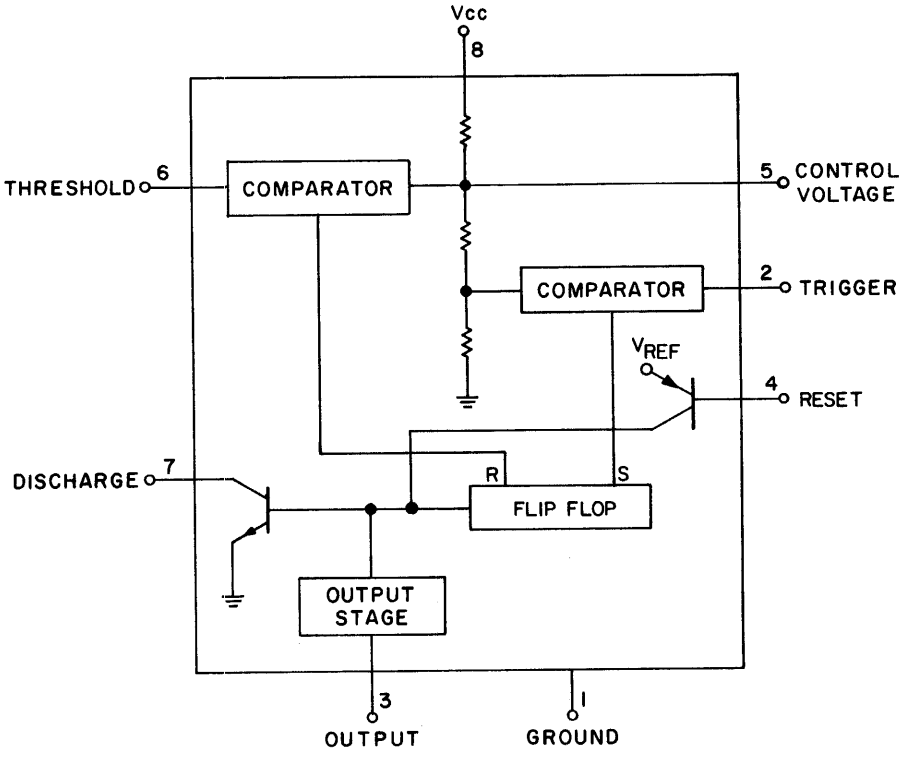
1. Vendor identification: NE555
2. Package pin configuration.





Arrows within the symbol outline and in the line to pin 5 are omitted for fixed-frequency or fixed delay applications.

LOGIC SYMBOLS



BLOCK DIAGRAM

916
Rev C
Sheet 1 of 3

Monostable Operation

In this mode of operation, the timer functions as a one-shot. Referring to Figure 1a the external capacitor is initially held discharged by a transistor inside the timer.

Upon application of a negative trigger pulse to pin 2, the flip-flop is set. This releases the short circuit across the external capacitor and drives the output high. The voltage across the capacitor now increases exponentially with the time constant $\tau=R_AC$. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which,in turn,discharges the capacitor rapidly and drives the output to its low state. Figure 1b shows the actual waveforms generated in this mode of operation.

The circuit triggers on a negative going input signal when the level reaches 1/3 V_{CC}. Once triggered, the circuit will remain in this state until the set time is elapsed, even if it is triggered again during this interval. The time that the output is in the high state is given by $t=1.1\ R_AC$. Because the charge rate and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply. Applying a negative pulse simultaneously to the reset terminal (pin 4) and the trigger terminal (pin 2) during the timing cycle discharges the external capacitor and causes the cycl to start over again. The timing cycle will now commence on the positive edge of the reset pulse. During the time the reset pulse is applied, the output is driven to its low state.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

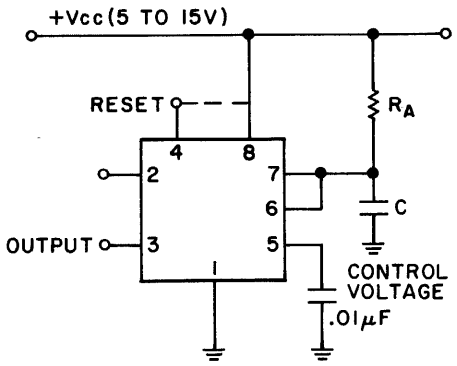


Figure 1a.

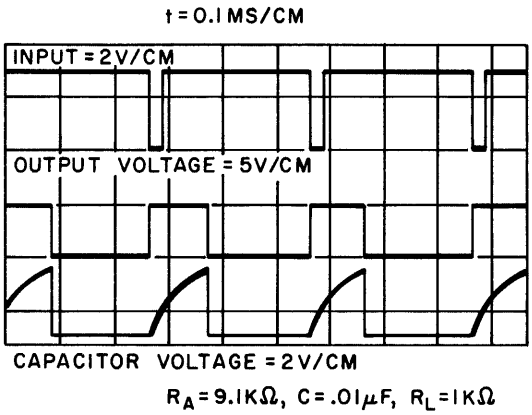


Figure 1b.

Astable Operation

If the circuit is connected as shown in Figure 2a (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors.

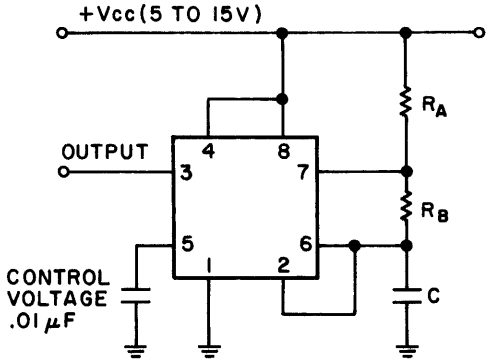


Figure 2a.

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 2b shows actual waveforms generated in this mode of operation.

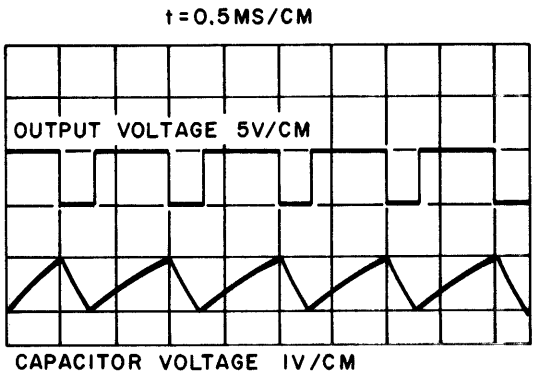


Figure 2b.

The charge time (output high) is given by:

$$t1 = 0.693\ (R_A + R_B)\ C$$

and the discharge time (output low) by:

$$t2 = 0.693\ (R_B)\ C.$$

Comparator-Input Flip-Flop

This application is depicted by the top two symbol drawings on sheet 1. Pin 5 determines the quiescent voltage levels of the trigger (pin 2) and the threshold (pin 6). In practice:

$$Vpin6 = Vpin5;\ Vpin2 = \frac{Vpin5}{2}$$

When the level at pin 6 exceeds that at pin 5, the FF sets. When the level at pin 2 exceeds one-half of that at pin 5, the FF resets.

916
Rev C
Sheet 3 of 3

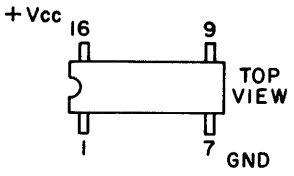
DESCRIPTION

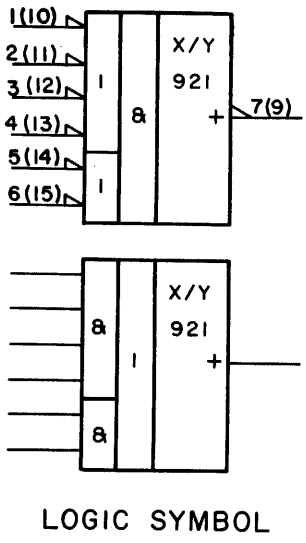
Element 921 is a line driver capable of driving terminated lines such as coaxial cable or twisted pairs. The outputs can also be used in wired OR circuits.

NOTES:

1. Vendor identification: 8T23

2. Package pin configuration.





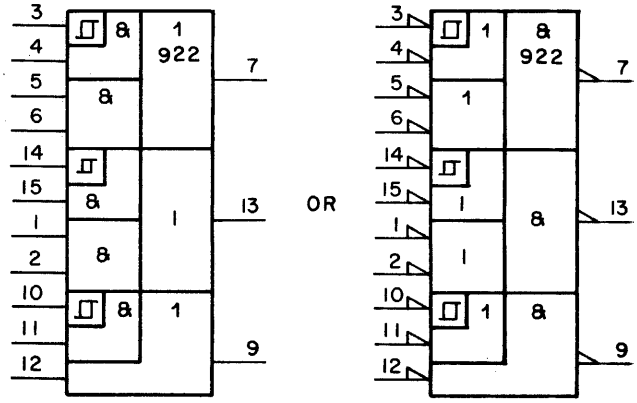
LOGIC SYMBOL

921
Rev B
Sheet 1 of 1

DESCRIPTION

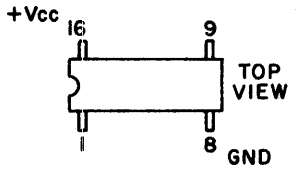
The 922 is a triple Line Receiver. Each receiver incorporates hysteresis to provide high noise immunity and high input impedance to minimize loading on the drive circuit.

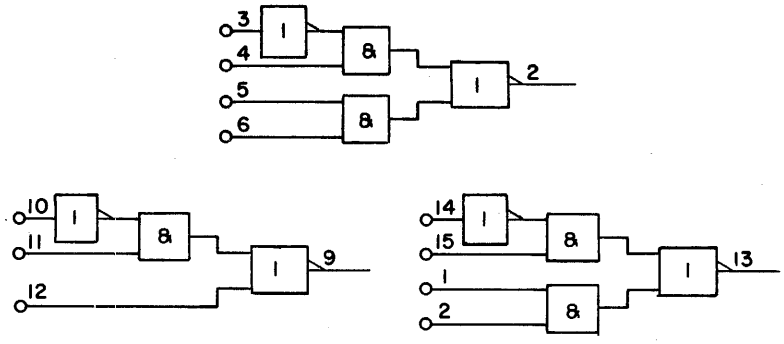
An input voltage of +1.8 volts or more is interpreted as a logical one; an input of +1.2 volts or less is interpreted as a logical zero, and is an open-circuited input.



NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 8T24
3. Package pin configuration.





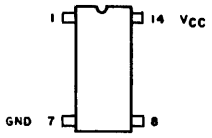
922
Rev C
Sheet 1 of 1

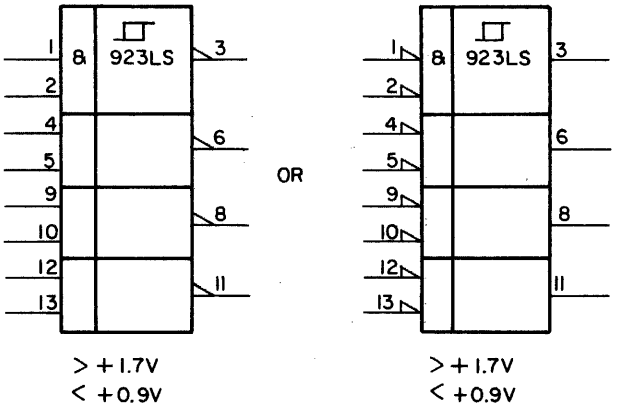
DESCRIPTION

Element 923LS consists of four 2-input, Schmitt trigger, positive NAND gates. The input threshold levels, which differ by typically 800 mV for positive-and negative-going signals because of hysteresis (backlash) in the trigger circuit, are a part of the logic symbol.

NOTES:

1. Sections may appear separately.
2. Vendor identification: 74LS132
3. Package pin configuration:





LOGIC SYMBOL

923
Rev B
Sheet 1 of 1

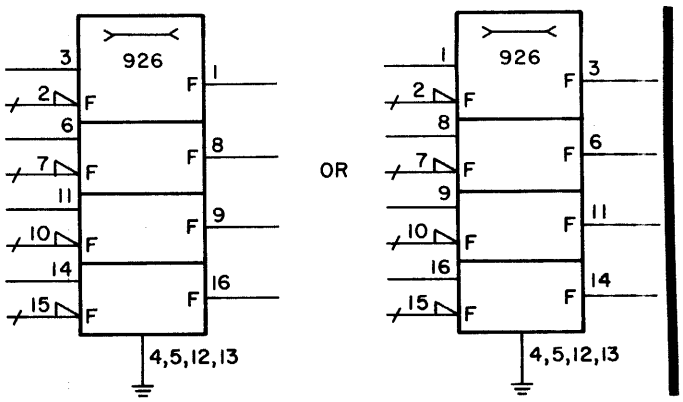
DESCRIPTION

Element 926 is an analog gate that switches on and off under the control of a binary input. A logic "0" turns the gate on and allows it to pass an analog signal from input to output. A logic "1" turns the gate off and causes it to block the analog signal.

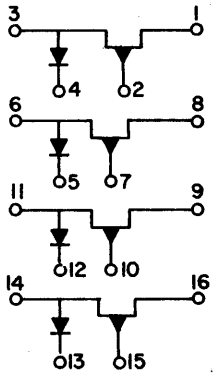
Pins	Function
3,6,11,14	Analog Inputs
1,8,9,16	Analog Outputs
2,7,10,15	Binary Inputs
4,5,12,13	Ground

NOTES:

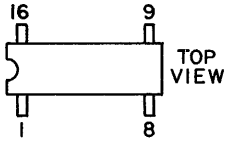
1. Symbol sections may appear separately.
2. Vendor Identification: IH5012



LOGIC SYMBOL



FUNCTIONAL DIAGRAM



PACKAGE PIN CONFIGURATION

BINARY INPUT	FUNCTION
1	BLOCKS ANALOG SIGNAL
0	PASSES ANALOG SIGNAL

TRUTH TABLE

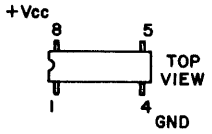
926
Rev. D
Sheet 1 of 1

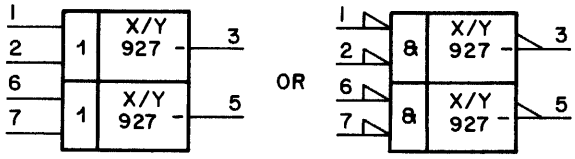
DESCRIPTION

The 927 is a dual peripheral positive-OR driver with DTL/TTL compatible inputs and an open-collector output.

NOTES:

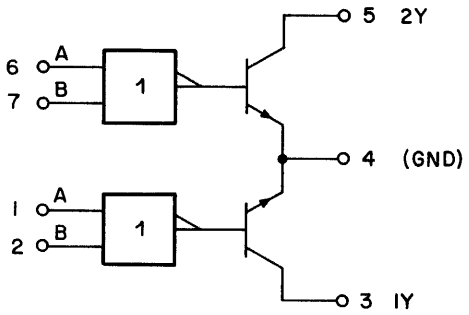
1. Vendor identification: 75453
2. Package pin configuration.





INPUTS		OUTPUT
A	B	Y
L	L	L (ON STATE)
L	H	H (OFF STATE)
H	L	H (OFF STATE)
H	H	H (OFF STATE)

TRUTH TABLE



FUNCTION DIAGRAM

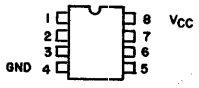
927
Rev C
Sheet 1 of 1

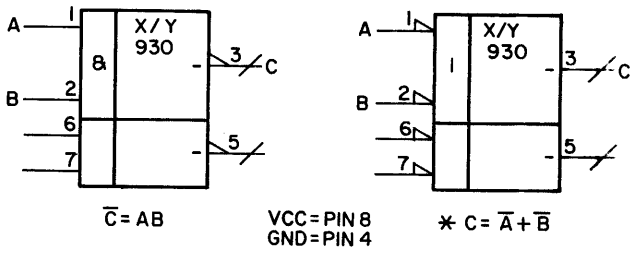
DESCRIPTION

The 930 circuit is a dual driver incorporating TTL logic with an open-collector output. The output is low when both inputs are high. The output is I (indeterminate) when either of both inputs are low. When an external pull-up output resistor is used, the output is high instead of I. The propagation delay time from a low to a high output is typically 50 ns. The power dissipation is 800 mW (continuous). The input threshold voltage is approximately 1.4 V. Output drive current in the low state is 150 mA. The input or output may be open or grounded for troubleshooting without damage.to the chip.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 75452
3. Package pin configuration:





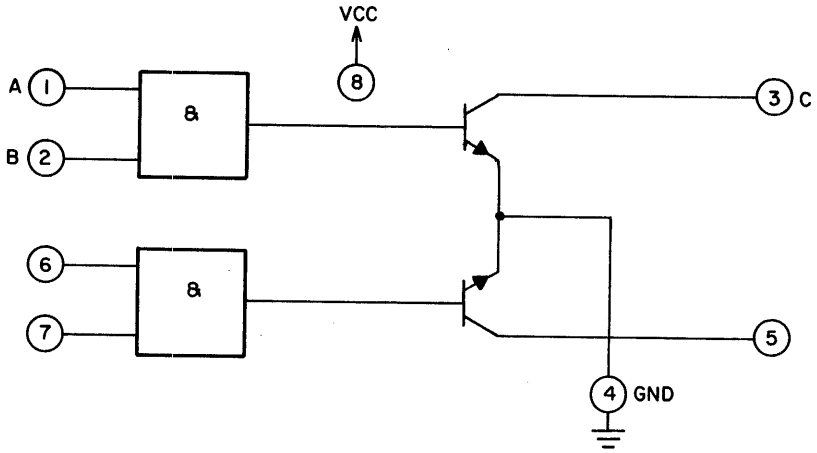
* Depends upon external output circuitry. A high is supplied when an external pull-up resistor is used in the output. The maximum voltage that the resistor can be connected to is 30 V.

LOGIC SYMBOL

INPUT PINS		OUTPUT PINS
A(1,6)	B(2,7)	C(3,5)
L	L	I
L	H	I
H	L	I
H	H	L

I=Indeterminate-the open-collector output supplies neither a high nor a low. A high is supplied when an external pull-up resistor is used in the output.

TRUTH TABLE



FUNCTIONAL DIAGRAM

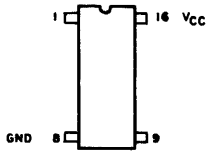
930
Rev A
Sheet 1 of 1

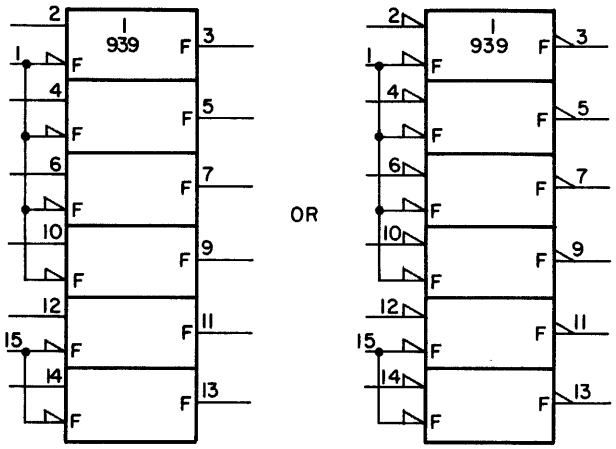
DESCRIPTION

Element 939 is a TTL non-inverting hex buffer with tri-state outputs.

NOTES:

1. Vendor identification: 8097/74367
2. Package pin configuration:





LOGIC SYMBOL

INPUTS		OUTPUT
F	DATA	
H	X	HI-Z
L	H	H
L	L	L

TRUTH TABLE
(EACH SECTION)

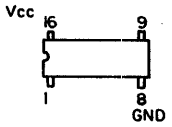
939
Rev A
Sheet 1 of 1

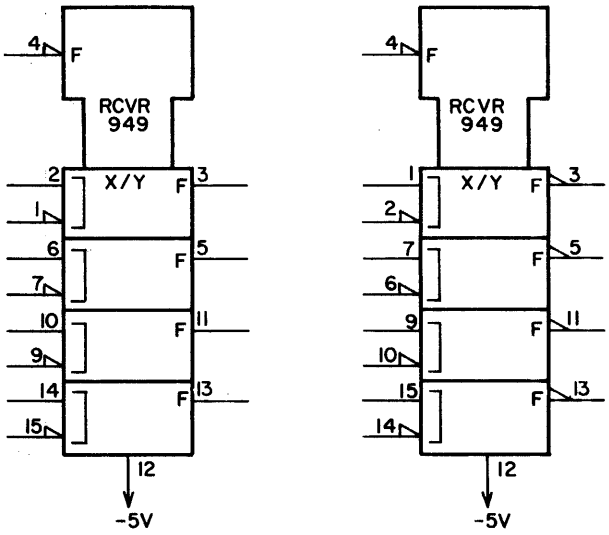
DESCRIPTION

The 949 circuit is a quad differential line receiver with tri-state outputs and a common strobe input. When the strobe input (Pin 4) is low, the output of each receiver section is determined by the differential voltage across its line inputs. With the strobe input high, all receiver outputs are in the high -impedance (Hi-Z) state.

NOTES:

1. Vendor identification: MC3450
2. Package pin configuration:





LOGIC SYMBOL

INPUT	STROBE	OUTPUT
VID ≥ +25mV	L	H
	H	HI-Z
-25 mV < VID < +25mV	L	I
	H	HI-Z
VID ≤ -25mV	L	L
	H	HI-Z

I = INDETERMINATE STATE

TRUTH TABLE

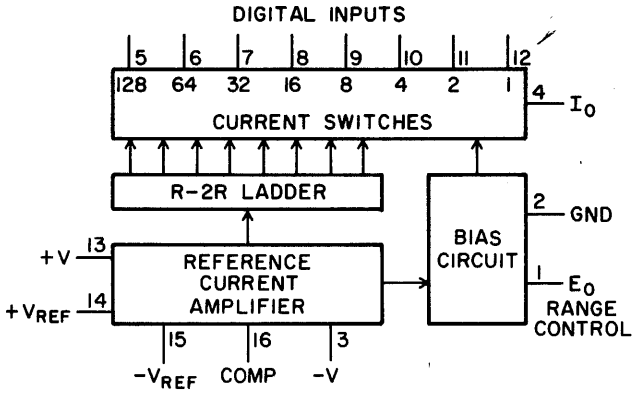
949
Rev B
Sheet 1 of 1

DESCRIPTION

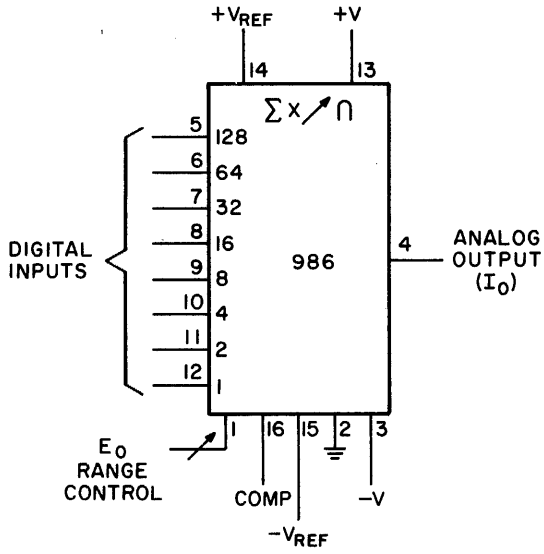
The 986 circuit is an eight-input digital-to-analog converter that provides its maximum output current (I_0) when all digital inputs are high (K=255), decreasing in discrete steps as the count goes from 255 to zero.

A reference current amplifier provides a constant current into the R-2R ladder, which divides the current into binary-related components that are fed to the current switches. Current from the reference amplifier is controlled by adjusting the positive/negative reference voltages. The output voltage (E_0) range may be varied by the voltage applied to pin 1. The compensation input, pin 16, maintains correct phase margin throughout the range.

The Typical Application diagram shows the 986 connected to provide 128 discrete output current values to an op amp (not a part of the 986 circuit). The op amp feed-back resistor is selected to provide an E_0 of 10 volts when input current to the op amp is maximum – that is, for a count of 127.



BLOCK DIAGRAM



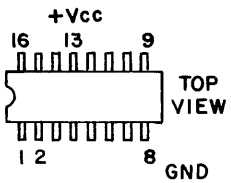
LOGIC SYMBOL

NOTES:

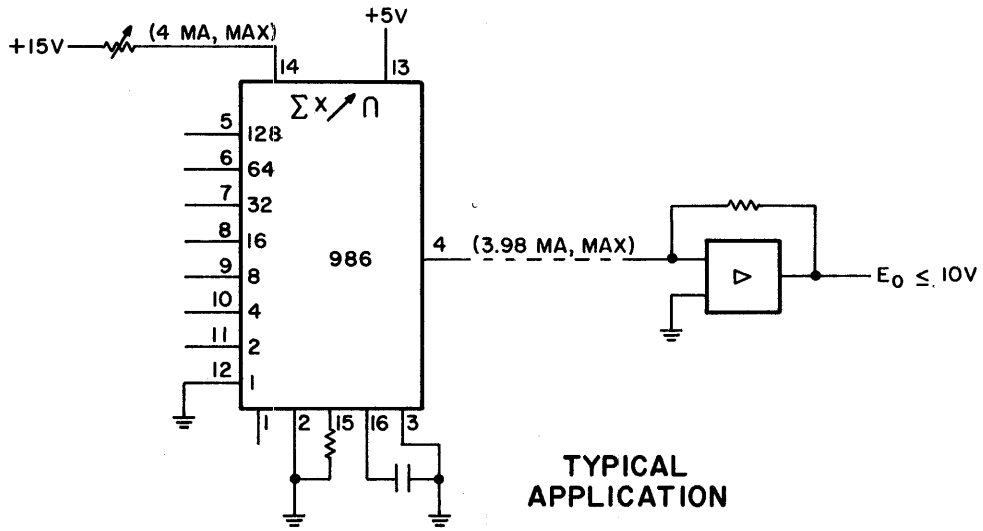
1. On a logic diagram, usually only the digital input and analog output pins are shown.
2. Vendor identification:

Element	Vendor Number
986A (6-Bit)	MC1408L-6
986B (7-Bit)	MC1408L-7
986D (8-Bit)	MC1408L-8
986E (8-Bit)	MC1408L-7.5

3. Package pin configuration.



986
Rev C
Sheet 1 of 2



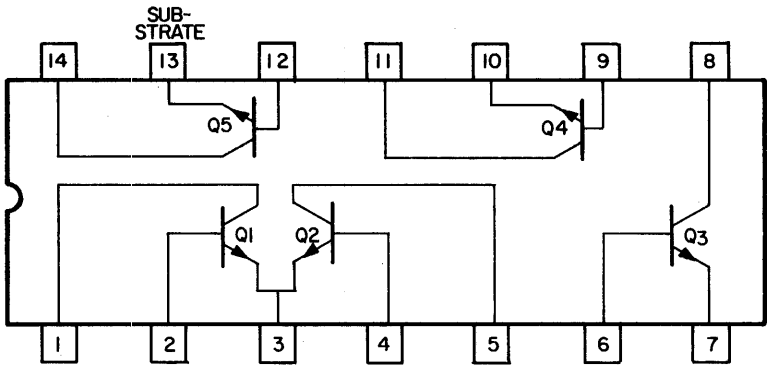
TYPICAL APPLICATION

DESCRIPTION

Element 3046 consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected as a differential pair.

NOTES:

1. The substrate (pin 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to ensure normal transistor action.
2. Vendor identification: CA3046
3. Pin connections are shown below.



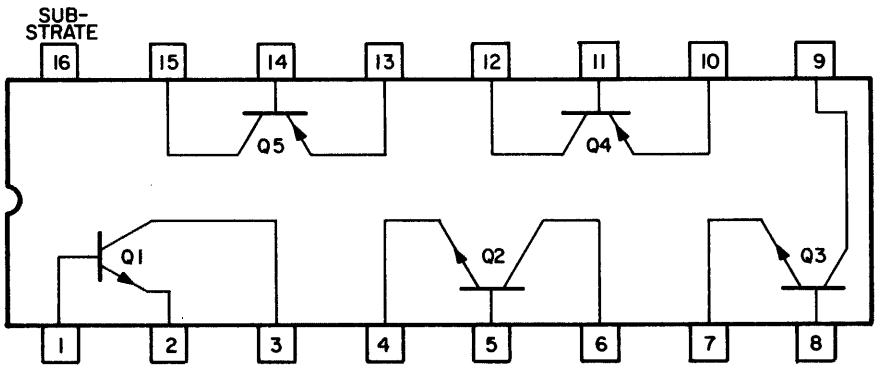
3046
Rev A
Sheet 1 of 1

DESCRIPTION

Element 3096 consists of five high-voltage, general-purpose silicon transistors mounted on a common substrate, which has a separate connection. The five-transistor array comprises three n-p-n and two p-n-p types. Typical collector-to-emitter breakdown voltage is 100 V.

NOTES:

1. Vendor identification: CA3096E
2. Pin connections are shown below.



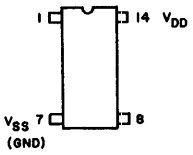
3096
Rev A
Sheet 1 of 1

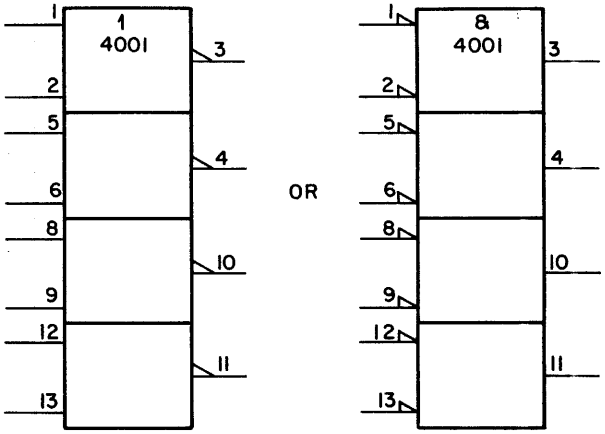
DESCRIPTION

The 4001 circuit is a CMOS package consisting of four 2-input positive NOR gates.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 4001
3. Package pin configuration:





LOGIC SYMBOL

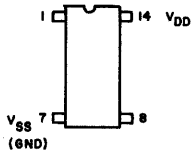
4001
Rev A
Sheet 1 of 1

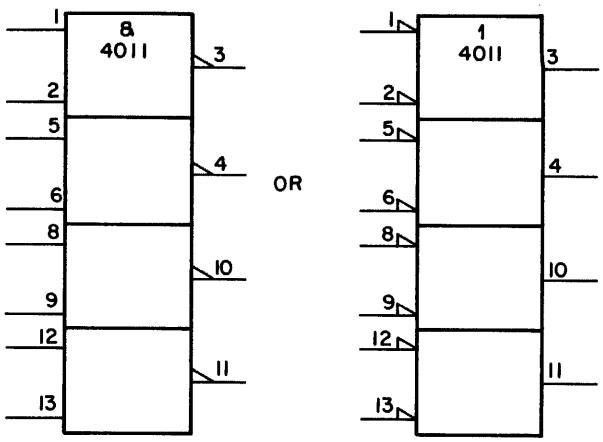
DESCRIPTION

The 4011 Circuit is a CMOS package consisting of four 2-input positive NAND gates.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 4011
3. Package pin configuration:





LOGIC SYMBOL

4011
Rev A
Sheet 1 of 1

DESCRIPTIONS:

Element 4016 consists of four independent CMOS bilateral switches. As shown in the functional diagram, a transmission gate (TG) responds to control input V_C (usually a binary signal) to pass or cut off the input data V_{IN}. V_{IN} may be either an analog or a binary signal with frequencies up to 54 MHz. The maximum effective pulse frequency of V_C depends upon V_{DD}, as shown below:

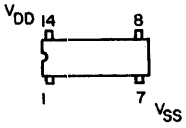
V_{DD}	V_C freq (max)
+5 V	5 MHz
+10 V	10 MHz
+15 V	12 MHz

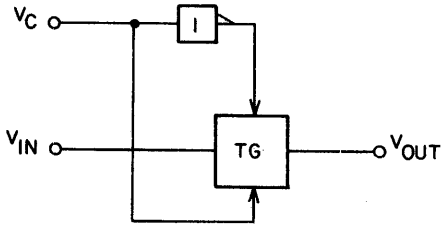
NOTES:

1. V_C high = TG ON
   V_C low = TG OFF
   (See Transmission Gate description on page 1-17)

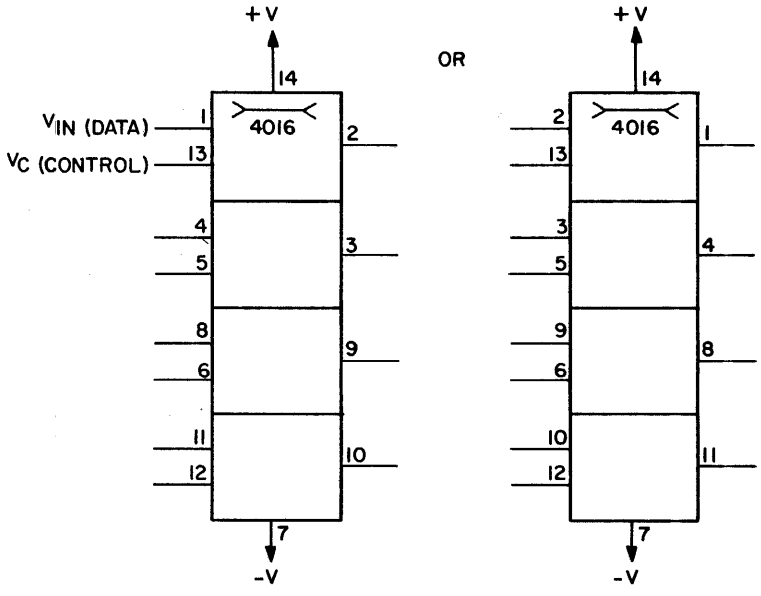
2. Vendor identification: MC14016B

3. Package pin configuration:





FUNCTIONAL DIAGRAM
(EACH SECTION)



LOGIC SYMBOL

4016
Rev A
Sheet 1 of 1

DESCRIPTION

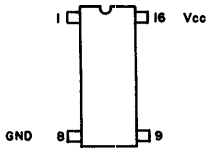
The 4017 circuit is a CMOS decode counter with an asynchronous, active-high reset and a built-in count decoder. Changes in the output occur on the positive-going edge of the Clock, pin 14, provided that the Clock Enable, pin 13 is low.

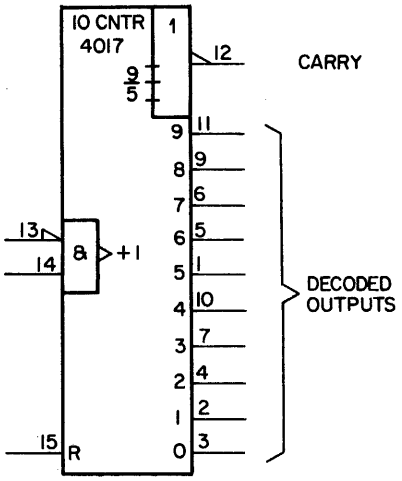
Outputs are normally low, going high only at the appropriate decimal count time.

A Carry output is provided that is high for all counts less than 5, and low for counts 5 through 9.

NOTES:

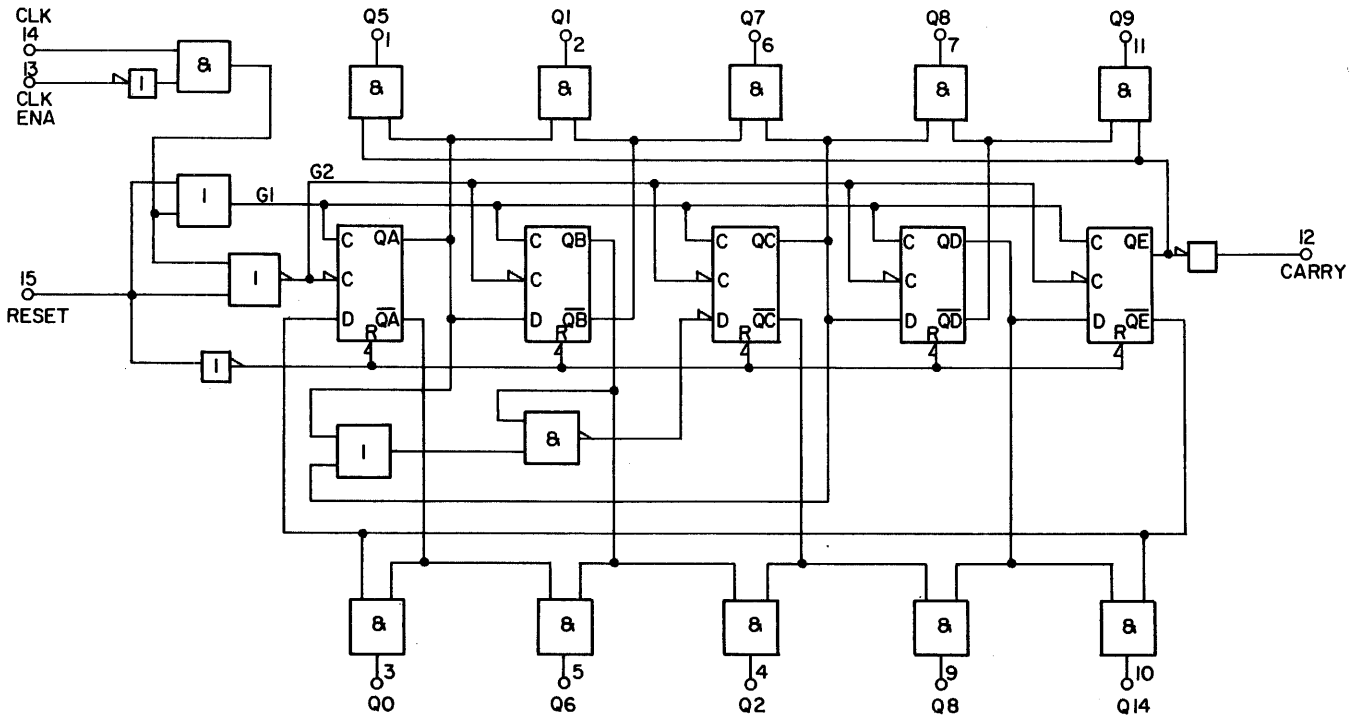
1. Vendor identification: 4017
2. Package pin configuration:



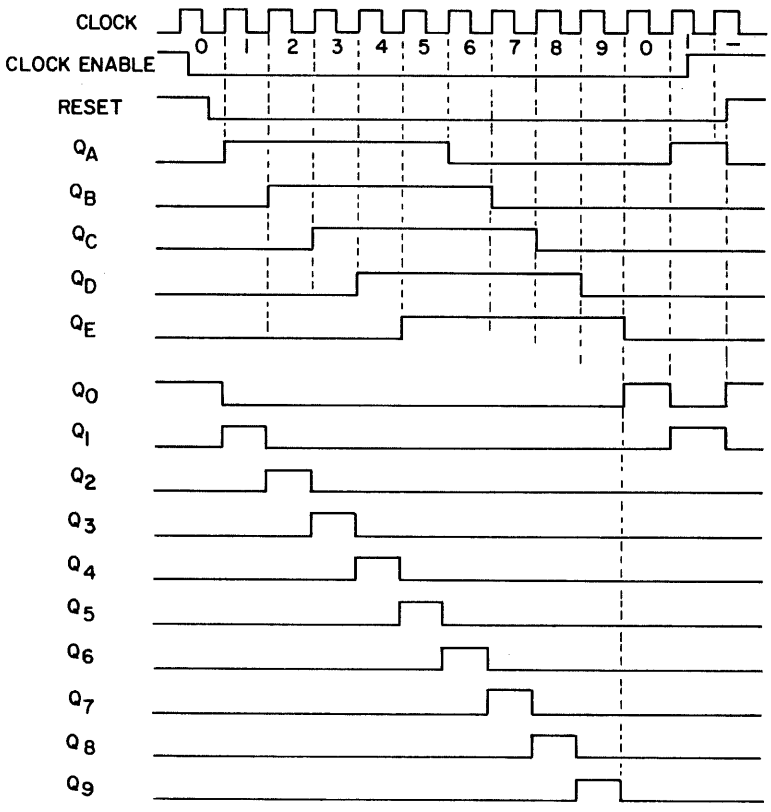


LOGIC SYMBOL

4017
Rev A
Sheet 1 of 2



FUNCTIONAL DIAGRAM



TIMING DIAGRAM

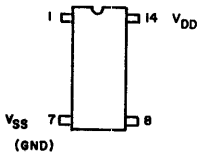
4017
Rev A
Sheet 2 of 2

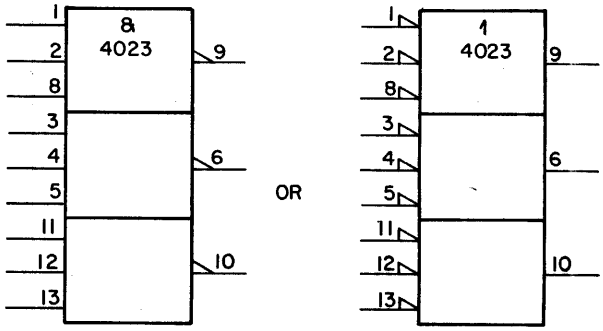
DESCRIPTION

The 4023 circuit is a CMOS package consisting of three 3-input positive NAND gates.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 4023
3. Package pin configuration:





LOGIC SYMBOL

4023
Rev A
Sheet 1 of 1

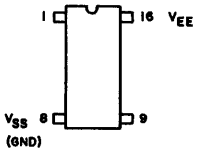
DESCRIPTION

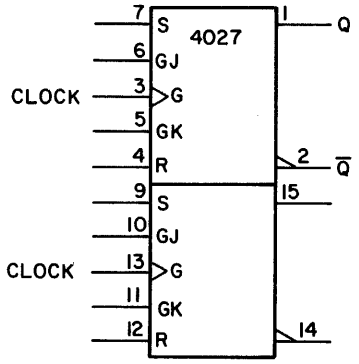
The 4027 circuit is a CMOS package consisting of two positive-edge-triggered J-K flip-flops with asynchronous set and clear inputs.

The functional (logic) diagram for the 4027 circuit appears as figure 1-15 in section 1 of this manual.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 4027
3. Package pin configuration:





LOGIC SYMBOL

INPUTS					OUTPUT Qn+1		
G	GJ	GK	S	R	Q	$\overline{Q}$	
X	X	X	0	1	0	1	
X	X	X	1	0	1	0	
X	X	X	1	1	1	1	
⌐	0	0	0	0	Qn	$\overline{Qn}$	NO CHANGE
⌐	1	0	0	0	1	0	
⌐	0	1	0	0	0	1	
⌐	1	1	0	0	$\overline{Qn}$	Qn	TOGGLE

Qn = STATE OF Q OUTPUT PRIOR TO CLOCK TIME.

Qn + 1 = STATE OF QUTPUT AFTER CLOCK TIME.

⌐ = CLOCK TIME (L-TO-H TRANSITION)

X = DON'T CARE

TRUTH TABLE

4027
Rev A
Sheet 1 of 1

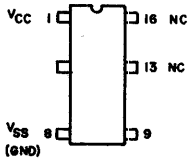
DESCRIPTION

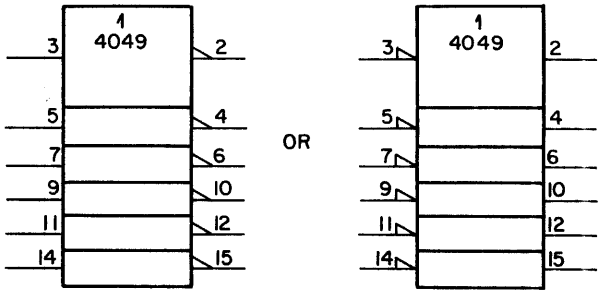
The 4049 circuit is a CMOS package consisting of six inverting buffers, each capable of driving up to two TTL loads when used as a CMOS-to-TTL converter. For that application, the high-level input voltage may exceed the TTL supply voltage (V_{CC}).

Pin 16 (normal V_{DD}) is not connected internally in this circuit, nor is pin 13.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 4049
3. Package pin configuration:





LOGIC SYMBOL

4049
Rev A
Sheet 1 of 1

Elements 5100, 5200, 5300, and 5400 constitute a phase-locked-loop oscillator (PLO), a simplified diagram of which is shown in figure 1. Table 1 gives a list of center frequencies for typical applications of the oscillator. A schematic diagram of the PLO is presented in figure 2, and subsequent sheets in this series provide the symbols and descriptions for each of the four elements, with frequent references to the schematic.

GENERAL DESCRIPTION, PLO

The phase-locked-loop oscillator affords a means of locking the timing of internal logic circuits to an external signal frequency. Typical usage is in the read/write circuits of disk memories, where the external signal is a series of servo-clock or data pulses from the rotating disk.

The essential elements of a PLO are 1) the current pump, which either pumps current into or out of a filter (R2/C2), depending upon the state of a Comparator FF (not a part of the PLO), and 2) a voltage-controlled oscillator (VCO), the frequency of which is determined by the charge across the aforementioned filter capacitor.

Supplemental elements include a constant-current source to minimize VCO frequence shifts due to power supply fluctuations, and a fast-start circuit that increases loop gain to achieve rapid lock-in -- typically with 20 pulses. When the low-active fast start signal disappears, the inertia of the PLO returns to normal so that it continues to track at the locked-in frequency despite data shift, gaps, or uneven spots in the data.

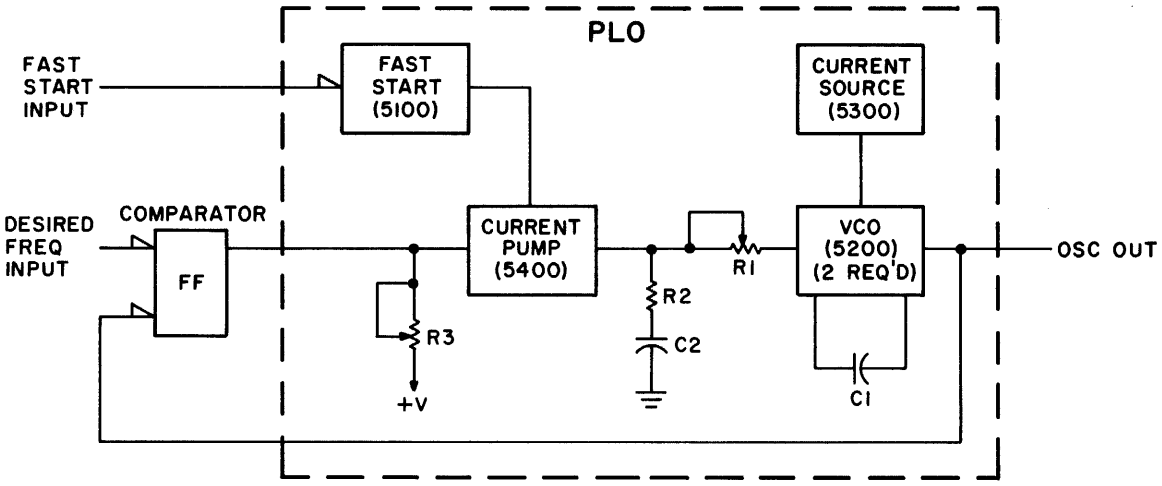


Figure 1. PLO, Simplified Block Diagram

The desired frequency and the VCO frequency will be 180 degrees out of phase when the PLO is locked in. Resistor R3 allows for precise adjustment of this relationship.

NOTE

R3 is adjusted for optimum phase relationship at the time the PLO is fabricated at the factory. This potentiometer must not be altered or adjusted in the field.

The capture range and response time of the VCO are determined by filter R2/C2. Rapid lock-in is provided to frequencies that deviate by up to 20% from the center frequency.

The center frequency of the VCO is determined by R1 and C1, and can be varied from 1 MHz to 40 MHz.

NOTE

At the time the PLO is fabricated, R1 is adjusted to the center frequency for the particular application. This potentiometer must not be altered or adjusted in the field.

Typical center frequencies (fc), with R1 and C1 values for each, are given in table 1 for various PLO applications.

TABLE 1. TYPICAL VCO/PLO CENTER FREQUENCIES

Application	fc (MHz)	R1 (Ω)	C1 (pF)
DMD Data Recovery	7.09	590	68
FMD Data Recovery	9.58	590	51
DMD Servo Input (x2)	0.886	590	680
x2	1.773	590	330
x2	3.545	590	150
x2	7.09	590	47
FMD Servo Input (x8)	2.4	590	220
x2	4.79	590	110
x2	9.58	590	68

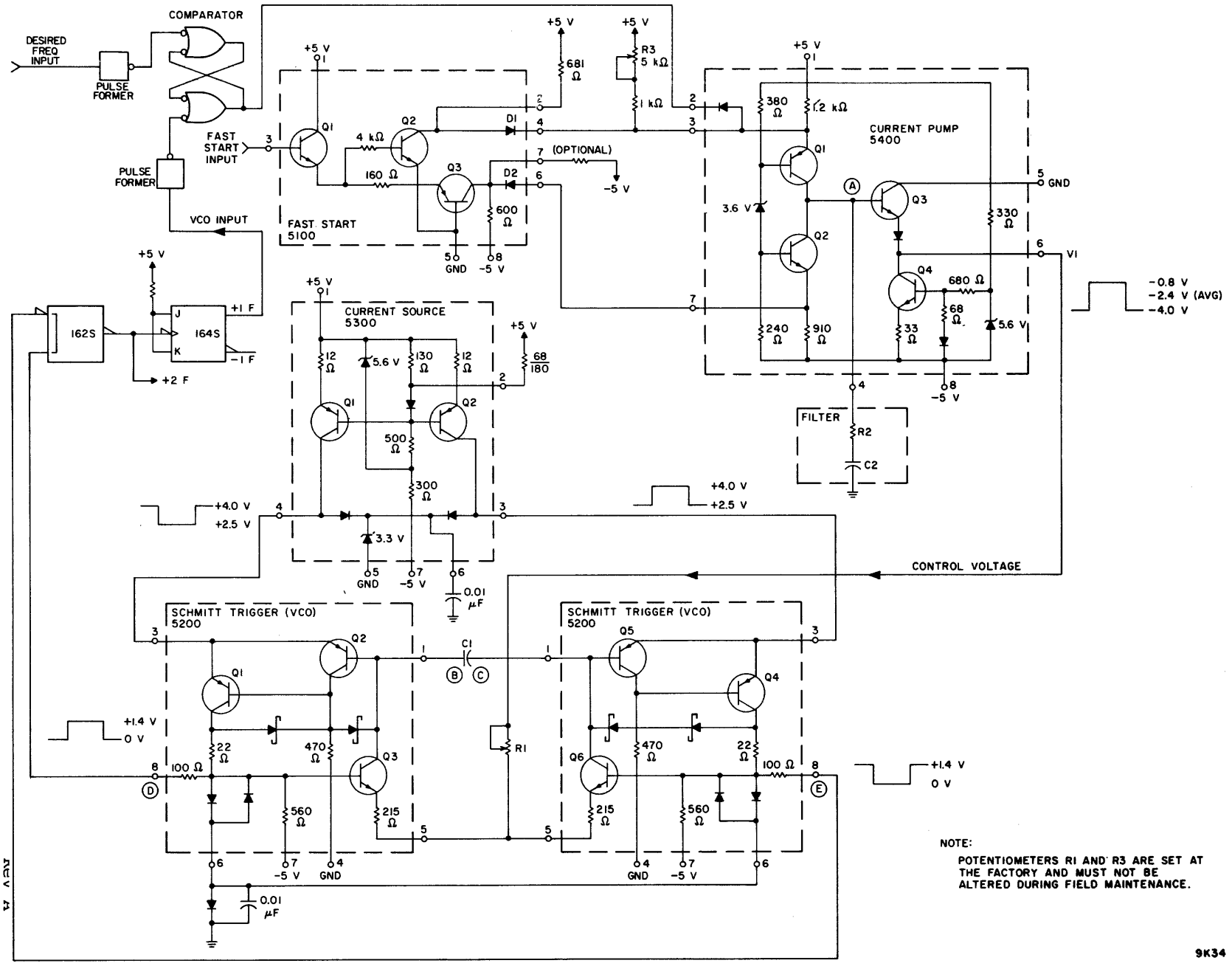
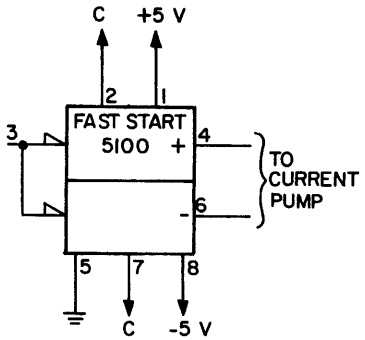


Figure 1. Schematic Diagram, Phase-Locked Oscillator (PLO)

DESCRIPTION

Element 5100 is a Fast Start circuit that accelerates the locking in of a phase-locked oscillator (PLO), usually to a data or servo-clock signal from a disk drive. It accomplishes this by increasing the current handled by the current pump (element 5400), which increases the current going into (and out of) filter R2/C2, thereby increasing the voltage swing of the pump's output (V1). This, in turn, extends the band width of the PLO, allowing it to move quickly capture, and then synchronize itself with, the desired input frequency.

In figure 2 (schematic, sheet 4), note the interconnections between elements 5100 and 5400. When diodes D1 and D2 are forward biased by a low input (Fast Start) signal to pin 3 of element 5100, the external 681 Ω resistor connected to +5 V is paralleled with the 1.2 kΩ resistor in element 5400 (via pin 4). Likewise the 600 Ω resistor is paralleled with the pump's 910 Ω resistor via pin 6. As a result, current flowing in the integrating circuit of the pump (see 5400 description) increases.

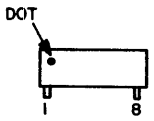


LOGIC SYMBOL

NOTES:

1. Vendor identification is the CDC part number -- 50225100.

2. Package pin configuration:



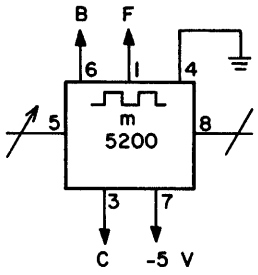
DESCRIPTION

Element 5200 consists of a Schmitt trigger and a current switch. Two 5200 elements are cross-coupled to form a voltage-controlled oscillator (VCO) for the PLO network, as shown in figure 2 on sheet 4. The transistor labellings in figure 2 are merely to aid in the circuit analysis. If the analysis applies to both the left-hand and right-hand elements in the VCO, the left-side transistors are given first, with those for the right side shown in parentheses.

Transistors Q1 and Q2 (Q4, Q5) always assume opposite states, as is typical of a Schmitt-trigger configuration. The ON state of the circuit is considered to be that in which Q1 (Q4) conducts. In this state, output pin 8 is held about two deode-drops above ground (approximately +1.4 V). This positive voltage also appears at the base of Q3 (Q6) which, because its emitter is connected to the negative control voltage from element 5400, turns Q3 (Q6) on. Q3 (Q6) then acts as a switch to sink current from the associated terminal of capacitor C1.

The OFF state of the Schmitt trigger exists when Q1 (Q4) is off and Q2 (Q5) is on. In this state, the output voltage at pin 8 falls to ground and base current through Q2 (Q5), as well as excess collector current through the associated Schottky diode, charges the capacitor.

In the ON state, the relatively heavy current through Q1 (Q4) holds the current-source voltage from element 5800 (as seen at pin 3) to +2.5 V. In the OFF state, Q2, (Q5) draws little current, so pin 3 rises to +4.0 V and is clamped there by the 5300 element. These voltage waveforms are shown in figure 2 and are important to understanding the following circuit analysis, which examines one complete cycle of the VCO.



F: TO FREQUENCY - DETERMINING COMPONENTS.

C: TO CONSTANT - CURRENT SOURCE

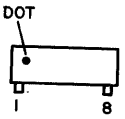
B: TO BIAS COMPONENTS

LOGIC SYMBOL

NOTES:

1. Vendor identification is the CDC part number -- 50225200.

2. Package pin configuration:



Let's assume that, as shown in figure 3, t1 has transpired and point B is more positive than point C. In this state, Q2 is off, Q1 and Q3 are on, with Q3 sinking current out of point B, while the output at point D rises to +1.4 V. Meanwhile, Q5 and the associated Schottky diode are conducting current into point C, which is held at +3.3 V by the base-emitter drop in Q5 (+4.40 -0.7 = +3.3 V).

As the ramping action passes t2, the charge across C1 actually reverses, making point C more positive than point B. Ramping continues until, at t3, point B reaches the switching point of Q2 (+2.5 -0.7 = +1.8 V). Schmitt trigger action between Q1 and Q2 causes Q2 to rapidly turn on, while Q1 turns off. (With Q2 conducting, the base-emitter junction of Q1 is biased below its conduction level by the emitter-to-collector drop in Q2.)

Meanwhile, the output at point D has fallen from +1.4 V to ground, turning off Q3, while pin 3 has risen sharply from +2.5 V to +4.0 V.

This 1.5-volt rise is reflected through Q2 and the associated Schottky diode to point B.

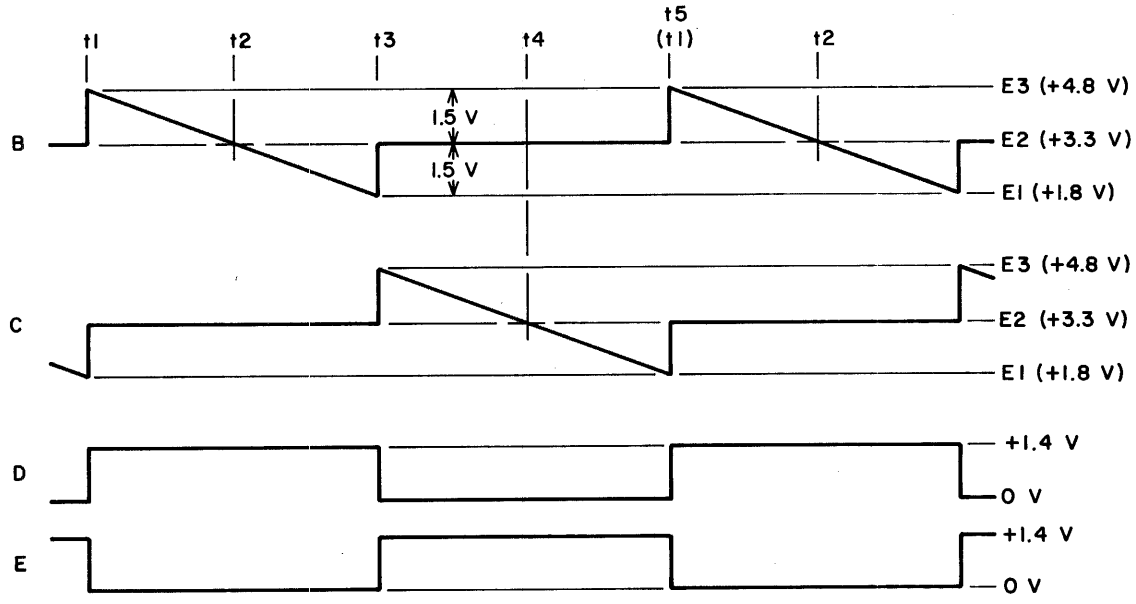
Because the charge across a capacitor cannot change instantaneously, point C is also raised 1.5 volts -- from +3.3 V to +4.8 V.

As a result, Q5 turns off, causing Q4 and Q6 to conduct. The output at point E now rises to +1.4 V, while Q6 ramps current out of point C.

When point C reaches +1.8 V (at t5), Q5 turns on. The resultant increase in voltage at pin 3 of the right-hand 5200 chip is reflected to point B, cutting off Q2 and turning on Q1 and Q3. The VCO has now passed through one complete cycle.

If the control voltage at pin 5 goes more negative, more current is sinked via Q3 (Q6), causing C1 to reach +1.8 V sooner. Thus, the VCD frequency increases. The opposite condition (a frequency decrease) results if pin 5 goes less negative.

The Schottky diodes enhance the switching time of the circuit by preventing Q1 and Q2 (Q4, Q5) from going into saturation.



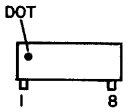
DESCRIPTION

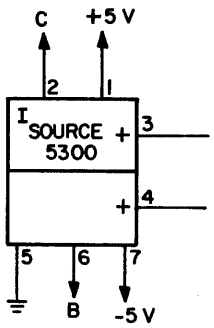
Element 5300 provides a stable current source for the VCO (element 5200), regardless of fluctuations in the logic-power-supply voltage(s). As shown in the schematic diagram of the 5300 element on page 5100-2, this is accomplished by using a zener diode that allows the base potentials of Q1 and Q2 to track voltage variations in the +5 V supply. The external resistor (connected to pin 2) is selected at the time the logic board is fabricated, and provides base drive in accordance with the output current requirement.

NOTES:

1. Vendor identification is the CDC part number -- 50225300.

2. Package pin configuration:





B: TO BIAS COMPONENTS
C: TO CURRENT-ADJUST COMPONENTS

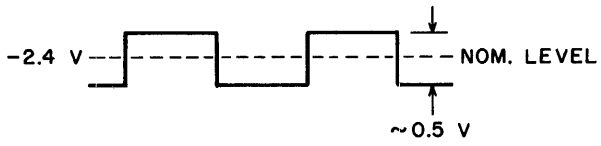
LOGIG SYMBOL

DESCRIPTION

Element 5400, in conjunction with filter R2/C2, is an integrating circuit that raises or lowers its output voltage (V1) in response to the phase relationship between 2 desired input frequency and that of the associated VCO.

Transistors Q1 and Q2 of element 5400 form a current pump, biased such that Q2 always conducts a current equal to I, regardless of whether or not Q1 is also conducting. When Q1 conducts, it supplies a current equal to 2I, half of which sources Q2 and the other half of which charges filter R2/C2. When Q1 is cut off, the current through Q2 is supplied by the filter.

Current through R2, in charging and discharging C2, causes a small-amplitude digital signal that rides on the nominal level maintained by C2.

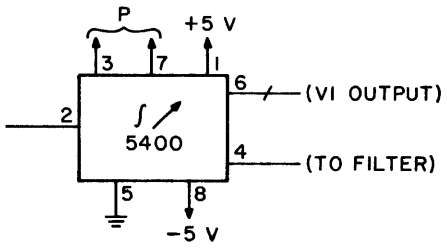


This is called the "proportional" component of the control voltage, V1. The nominal level maintained by C2 is the "integral" component.

The amplitude of the proportional component determines how quickly the PLO can respond to peak shifts in the individual pulses of the desired input frequency. The rate at which the integral component can change determines how quickly the PLO can respond to input frequency variations.

The Comparator FF (top left in the schematic) is set by a positive-going pulse from the desired input frequency. This puts the emitter of Q1 essentially at ground, and Q1 is cut off. The filter now pumps current through Q2, causing the voltage at point A to decrease. This voltage is passed through emitter-follower Q3 to output pin 6. (Q3 and Q4 constitute a buffer that minimizes the effect of output loading up on point A.) The voltage at pin 6 (V1) is referred to as the "control voltage" input to the VCO.

When the Comparator FF is cleared by a positive-going pulse from the VCO, Q1 turns on, conducting a current equal to 2I. Because the current through Q2 is limited by the 910-ohm resistor, the excess current (2I-I=I) is pumped into the filter, thereby raising the voltage at point A.



P: TO INPUT-PHASE-DETERMINING COMPONENTS

LOGIC SYMBOL

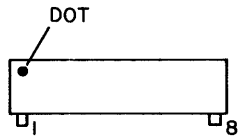
If the Comparator is in a set state longer than it is reset (Desired Freq > VCO Freq), the voltage at point A becomes less positive, causing the frequency of the VCO to increase. If the Comparator is reset (cleared) longer than it is set (Desired Freq < VCO Freq), the voltage at point A becomes more positive, and the VCO frequency decreases.

When the Comparator is in a set state reach an equilibrium (square-wave output is symmetrical), the voltage at point A stabilizes.

The Fast Start input to the 5400 (pins 3 and 7) increase the current through Q1 and Q2, as described in the description of the 5100 circuit. The proportional component, as well as the rate of change of the integral component, of the control voltage are thereby increased, reducing the PLO response time and allowing it to lock in more quickly to the desired frequency.

NOTES:

1. Vendor identification is the CDC part number -- 50225400.
2. Package pin configuration.



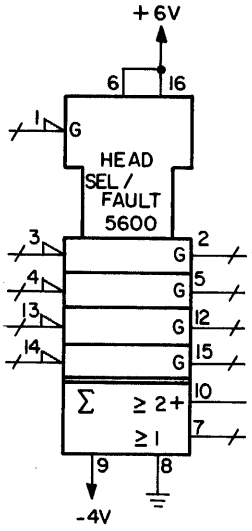
(PIN 2 UNUSED)

Rev A
Sheet 9 of 9

DESCRIPTION

Element 5600, or its improved version, element 7500, consists of four head-select buffers having high-current capability, and a comparator for determining when multiple heads have been selected. A high on the low-active Chip Select input (pin 1) forces all output pins low, as seen in the truth table on sheet 3.

Pin 10 is an open-emitter that can provide only a high-level output. The low level must be supplied by the IC (or other component) to which pin 10 is connected.



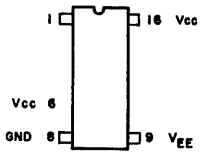
LOGIC SYMBOL

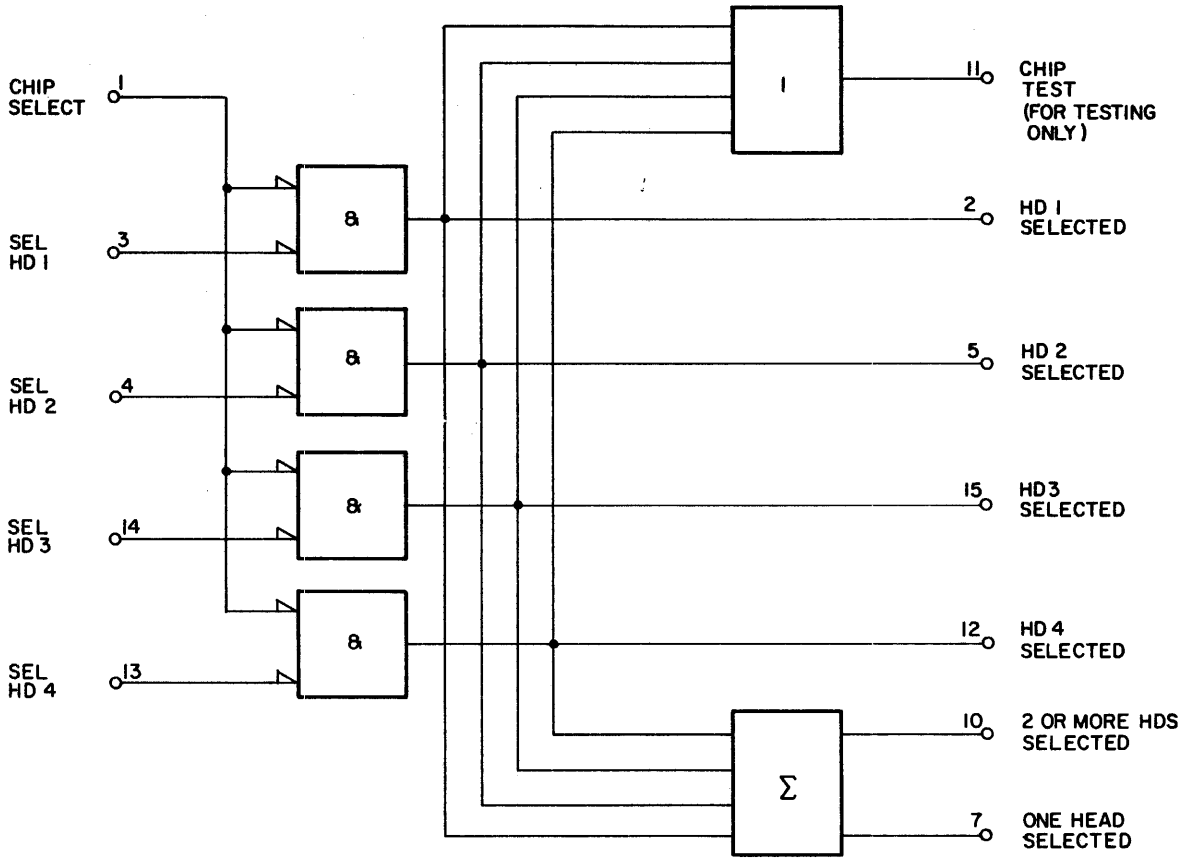
NOTES:

1. Vendor identification:

Element	Part Number
5600	50255600
7500	15157500

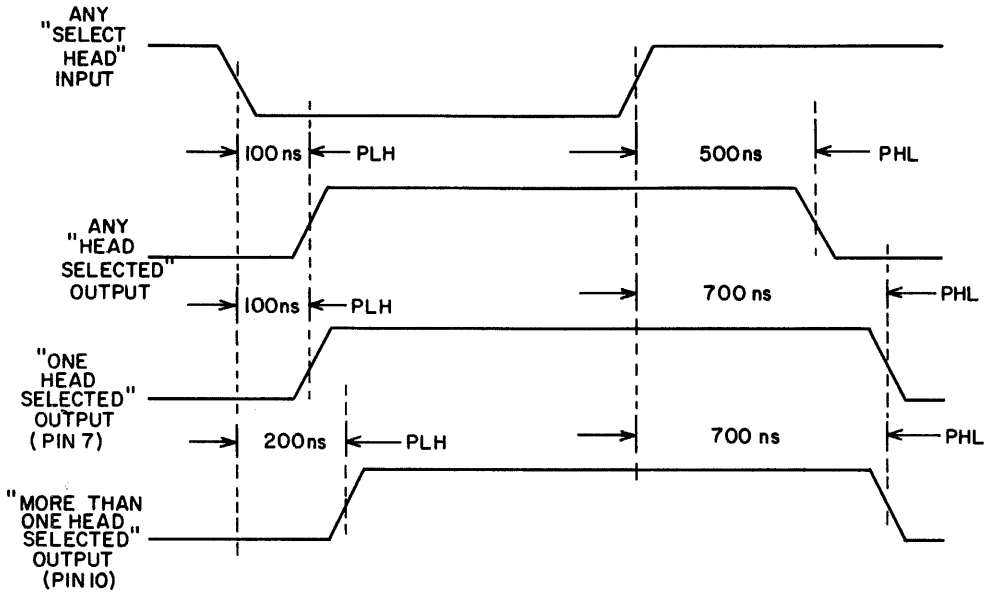
2. Package pin configuration:





FUNCTIONAL DIAGRAM

5600/7500
Rev A
Sheet 2 of 3



PLH: PROPAGATION DELAY, L-TO-H

PHL: PROPAGATION DELAY, H-TO-L

TIMING DIAGRAM

CONDITIONS	CHIP SEL	HEAD-SELECT INPUTS	HEAD SELECTED OUTPUTS	LOGIC OUTPUTS
	(1)	(3)(4)(13)(14)	(2)(5)(12)(15)	(7) (10)
CHIP NOT SELECTED	H	X X X X	L L L L	L L
CHIP SELECTED NO HEAD SELECTED	L	H H H H	L L L L	L L
CHIP SELECTED ONE HEAD SELECTED	L	ONE INPUT LOW ALL OTHERS HIGH	INVERSE OF RESPECTIVE INPUT VOLTAGE	H L
CHIP SELECTED $\geqslant$ 2 HEADS SELECTED	L	$\geqslant$ 2 INPUTS LOW ALL OTHERS HIGH	INVERSE OF RESPECTIVE INPUT VOLTAGE	H H

X = IRRELEVENT
L = LOW LEVEL VOLTAGE
H = HIGH LEVEL VOLTAGE
( ) = PIN NUMBERS

TRUTH TABLE

5600/7500
Rev A
Sheet 3 of 3

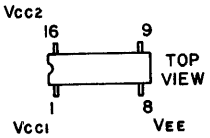
DESCRIPTION

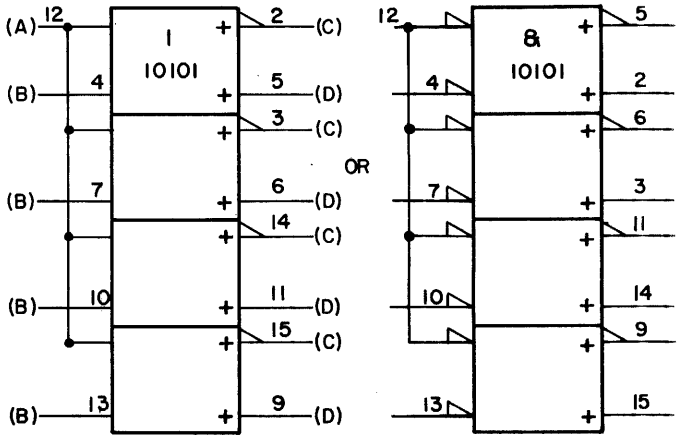
The 10101 is a ECL quad OR/NOR gate with one input from each gate common to pin 12. All sections provide complementary outputs.

NOTES:

1. Vendor identification: MC 10101L

2. Package pin configuration.





LOGIC SYMBOL

INPUT PINS		OUTPUT PINS	
A	B	C	D
0	0	1	0
1	0	0	1
0	1	0	1
1	1	0	1

TRUTH TABLE

10101
Rev D
Sheet 1 of 1

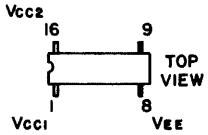
DESCRIPTION

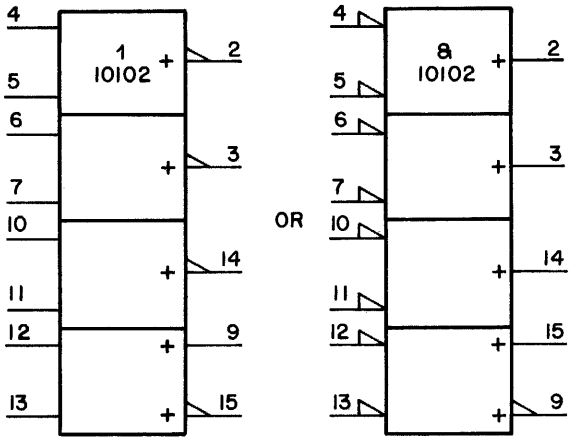
The 10102 is a ECL quad 2-input NOR gate. The last section provides complementary (OR/NOR) outputs.

NOTES:

1. Vendor identification: MC10102L

2. Package pin configuration





LOGIC SYMBOL

INPUT PINS		OUTPUT PINS	
12	13	9	15
0	0	0	1
1	0	1	0
0	1	1	0
1	1	1	0

TRUTH TABLE
(LAST SECTION)

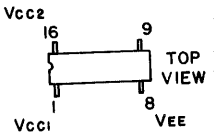
10102
Rev D
Sheet 1 of 1

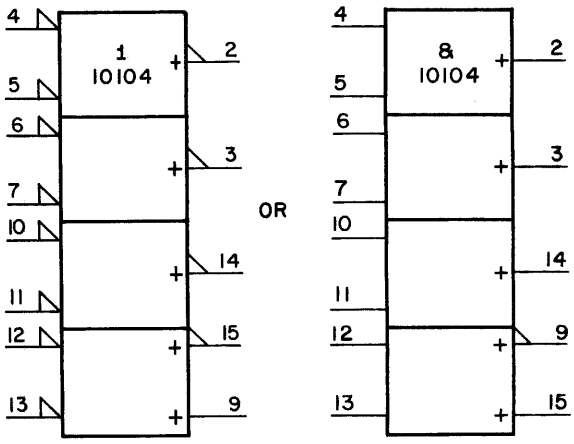
DESCRIPTION

The 10104 is a ECL quad 2-input AND gate. The last section provides complementary (AND/NAND) outputs.

NOTES:

1. Vendor identification: MC10104L
2. Package pin configuration.





LOGIC SYMBOL

INPUT PINS		OUTPUT PINS	
12	13	9	15
0	0	1	0
1	0	1	0
0	1	1	0
1	1	0	1

TRUTH TABLE
(LAST SECTION)

10104
Rev D
Sheet 1 of 1

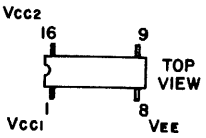
DESCRIPTION

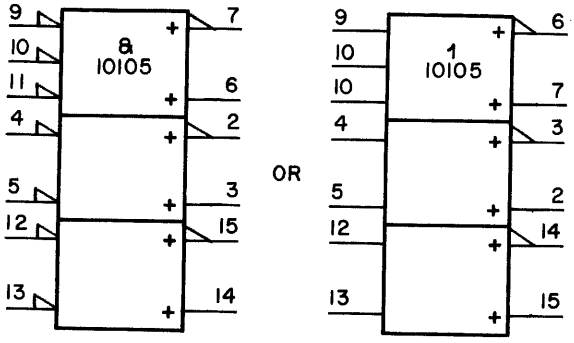
The 10105 is an ECL triple OR/NOR gate with a 3-2-2 input configuration. All sections provide complementary outputs.

NOTES:

1. Vendor identification: MC10105L

2. Package pin configuration.





LOGIC SYMBOL

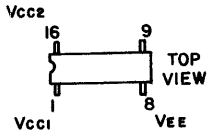
10105
Rev D
Sheet 1 of 1

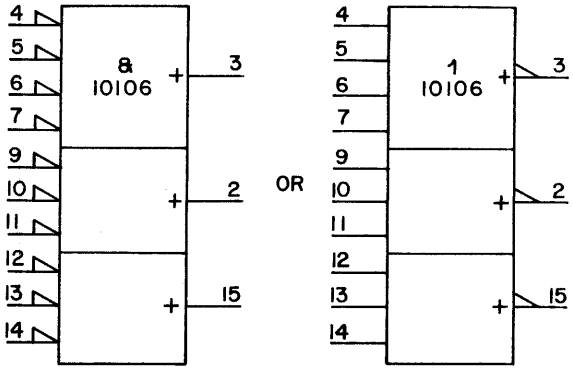
DESCRIPTION

The 10106 is a ECL, triple, 4-3-3-input NOR gate.

NOTES:

1. Vendor identification: MC10106L
2. Package pin configuration.





LOGIC SYMBOL

10106
Rev D
Sheet 1 of 1

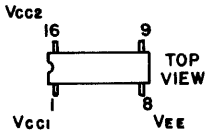
DESCRIPTION

The 10107 circuit features three Exclusive OR/NOR gates with complementary outputs. For low-active inputs, the outputs labelled C and D provide the X-OR and X-NOR functions, respectively. For high-active inputs, these output-pin functions are reversed (D=X-OR, etc.).

A high active Exclusive OR/NOR output (=1) equates to a low-active Coincidence-gate output (=) from the same pin, as shown in the truth table.

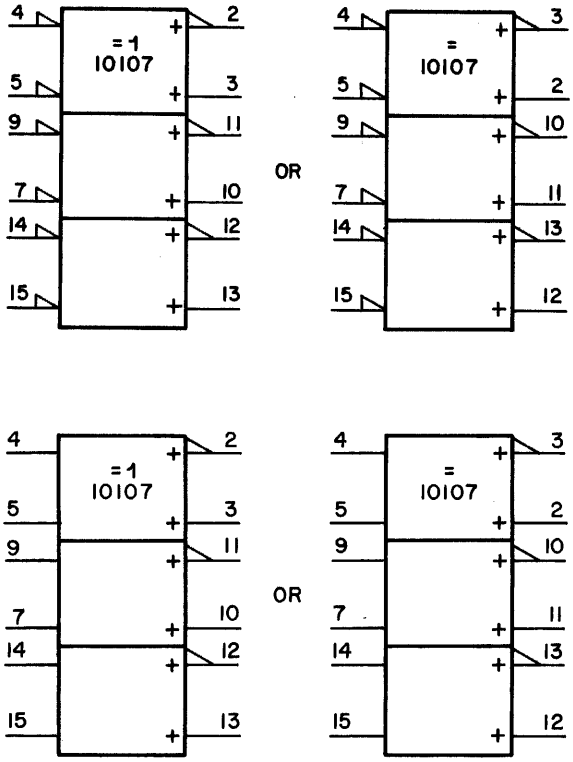
NOTES:

1. Vendor identification: MC10107L
2. Package pin configuration.



INPUT PINS		OUTPUT PINS	
A	B	C	D
0	0	1	0
1	0	0	1
0	1	0	1
1	1	1	0

TRUTH TABLE
(ANY SECTION)



LOGIC SYMBOL

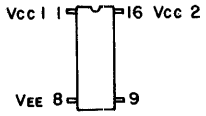
10107
Rev D
Sheet 1 of 1

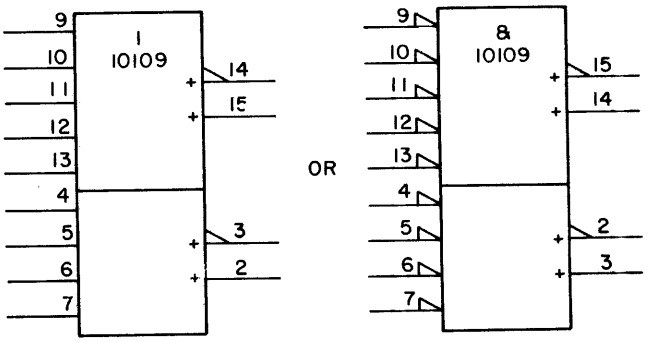
DESCRIPTION

Element 10109 is a dual ECL OR/NOR gate with 4 and 5 inputs, respectively. Complementary outputs are provided from each section.

NOTES

1. Sections may be shown separately.
2. Vendor identification: MC10109
3. Package pin configuration:





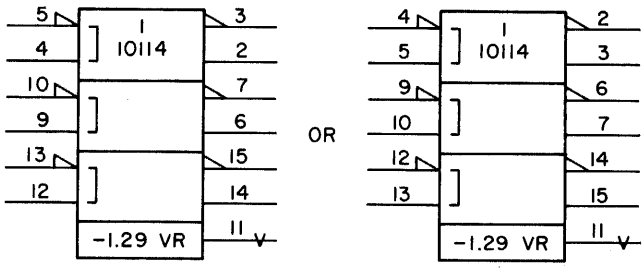
LOGIC SYMBOL

10109
Rev A
Sheet 1 of 1

DESCRIPTION

Element 10114 is an ECL triple line receiver for sensing differential signals. Common-mode noise rejection of 1 volt in either the positive or negative direction allows a large amount of common-mode noise immunity over long lines.

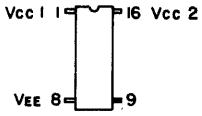
The OR output pins (3,7,15) go low whenever the inputs are left floating. Pin 11 provides a V_{BB} reference that is useful for making the 10114 a Schmitt trigger, allowing single-ended driving of the inputs. The 10114 can also be used as a MOS to ECL interface.



LOGIC SYMBOL

NOTES

1. If sections are shown separately, show the -VR (pin 11) reference in but one section.
2. Vendor identification: MC10114
3. Package pin configuration:



10114
Rev A
Sheet 1 of 1

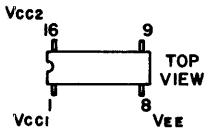
DESCRIPTION

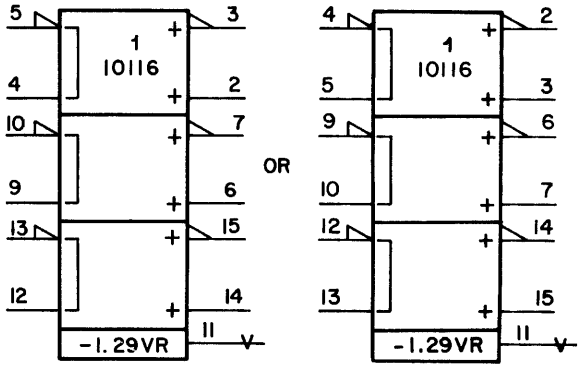
The 10116 is a ECL, triple differential line receiver. The line receivers are essentially very high speed linear differential amplifiers with standard ECL outputs.

If any amplifier is unused, one input of that amplifier must be tied to V_{BB} (pin 11) to prevent upsetting the current source bias network. In this respect, contrast with element 10114.

NOTES:

1. Vendor identification: MC10116L
2. Package pin configuration.





LOGIC SYMBOL

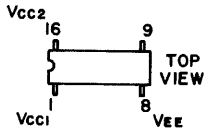
10116
Rev D
Sheet 1 of 1

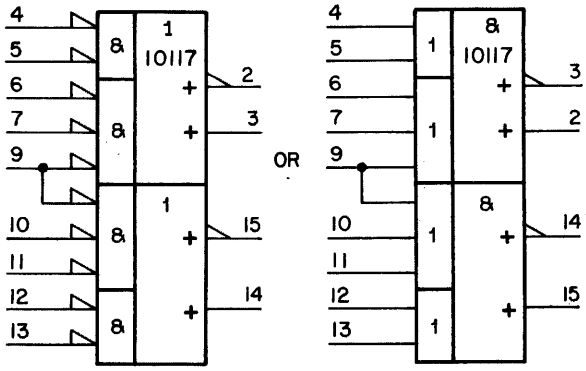
DESCRIPTION

The 10117 is a ECL,dual 2-wide,2-3-input AND-OR / AND-OR-INVERT gate.

NOTES:

1. Vendor identification: MC10117L
2. Package pin configuration:





LOGIC SYMBOL

INPUT PINS					OUTPUT PINS	
4	5	6	7	9	2	3
0	0	X	X	X	0	1
X	X	0	0	0	0	1
ALL OTHER COMBINATIONS					1	0

X = DONT CARE

TRUTH TABLE

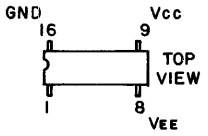
10117
Rev C
Sheet 1 of 1

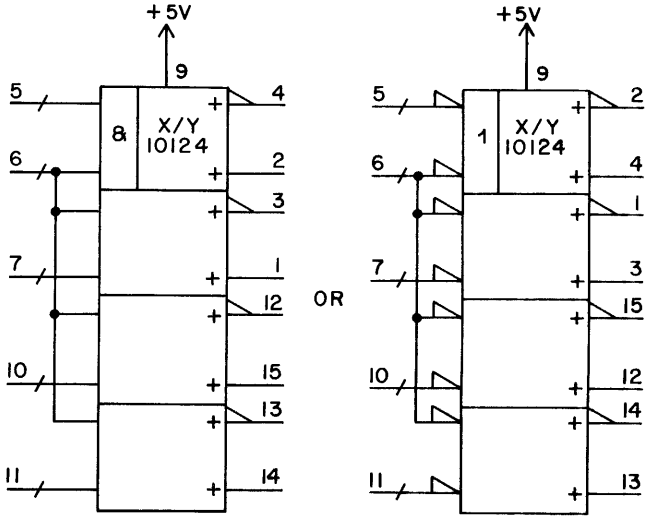
DESCRIPTION

The 10124 is a quad TTL to ECL level translator.

NOTES:

1. Vendor identification: MC10124L
2. Package pin configuration:





LOGIC SYMBOL

10124
Rev C
Sheet 1 of 1

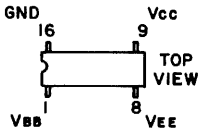
DESCRIPTION

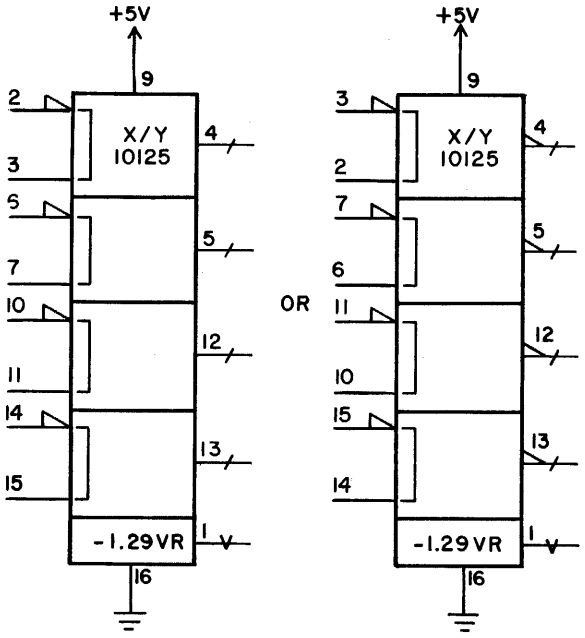
The 10125 is a quad ECL to TTL level translator.

NOTES:

1. Vendor identification: MC10125L

2. Package pin configuration.





LOGIC SYMBOL

10125
Rev C
Sheet 1 of 1

DESCRIPTION

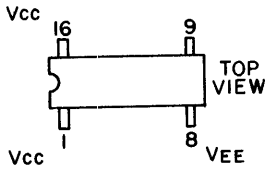
The 10131 is an ECL circuit containing two master-slave, type-D FFs. The FFs are controlled either by the set and reset inputs or by the clock input used in conjunction with the CD (data) input (refer to functional diagram and truth tables).

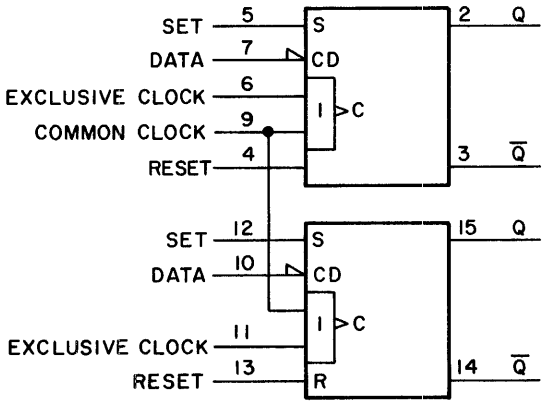
When both the set and reset inputs are low, the FFs are in the clocked mode and their output states change on the positive transition of the clock. The resulting change depends on the information present at the data (CD) input.

The FFs have both common and exclusive clock inputs. The FFs change separately,under control of their exclusive clock inputs, whenever the common clock input is held low. They change states simultaneously, under control of the common clock,whenever the exclusive clock inputs are held low. In either case, the final state of each FF depends on the information present at its data (CD) input at the time of the clock.

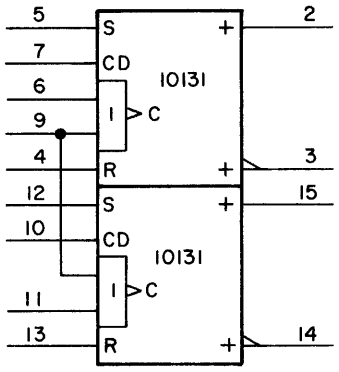
NOTES:

1. Vendor identification: MC10131
2. Package pin configuration.

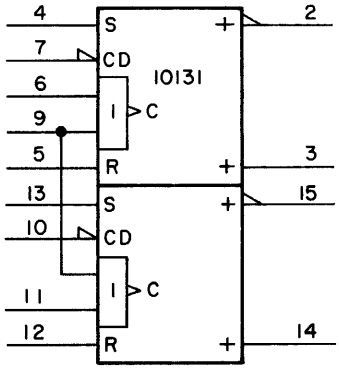




FUNCTIONAL DIAGRAM



OR



LOGIC SYMBOL

X=DON'T CARE
ND=NOT DEFINED
NC=NO CHANGE

H=LOGICAL ONE
L=LOGICAL ZERO

DATA	COMMON CLOCK	EXCLUSIVE CLOCK	Q	$\overline{Q}$
H	L	H	H	L
L	L	H	L	H
H	H	L	H	L
L	H	L	L	H
X	L	L	NC	NC
X	H	H	ND	ND

CLOCKED OPERATION

SET	RESET	Q	$\overline{Q}$
H	L	H	L
L	H	L	H
H	H	ND	ND
L	L	NC	NC

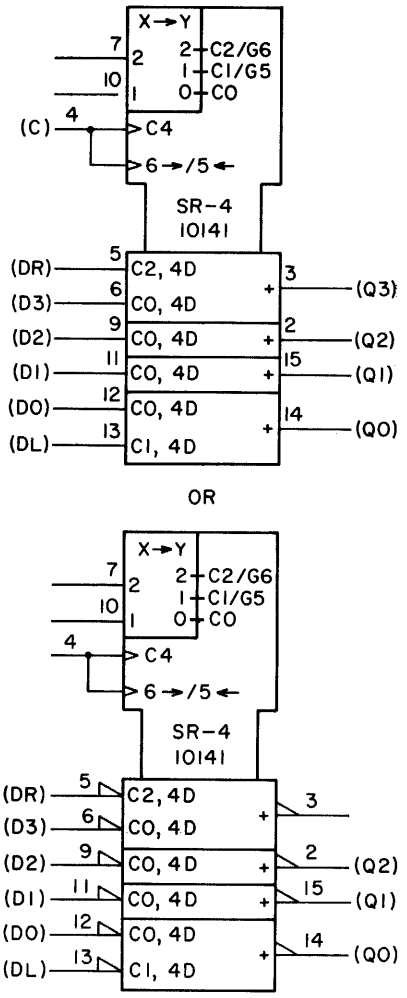
SET/RESET OPERATION

TRUTH TABLES

10131
Rev C
Sheet 1 of 1

DESCRIPTION

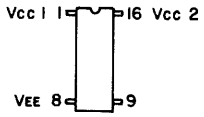
The 10141 circuit is an ECL 4-bit universal shift register. Inputs are provided for right shift (DR), left shift (DL), or parallel entry (D0-D3). Outputs are provided from each stage in the register, allowing a choice of parallel or serial output for either shift mode, as well as parallel in/ parallel out operation. Input data is asynchronous, and is shifted to the output on the positive-going edge of the clock pulse (C). Control inputs S1 and S2 determine the operating mode, as given in the truth table. A timing diagram is shown on sheet 2.



NOTES

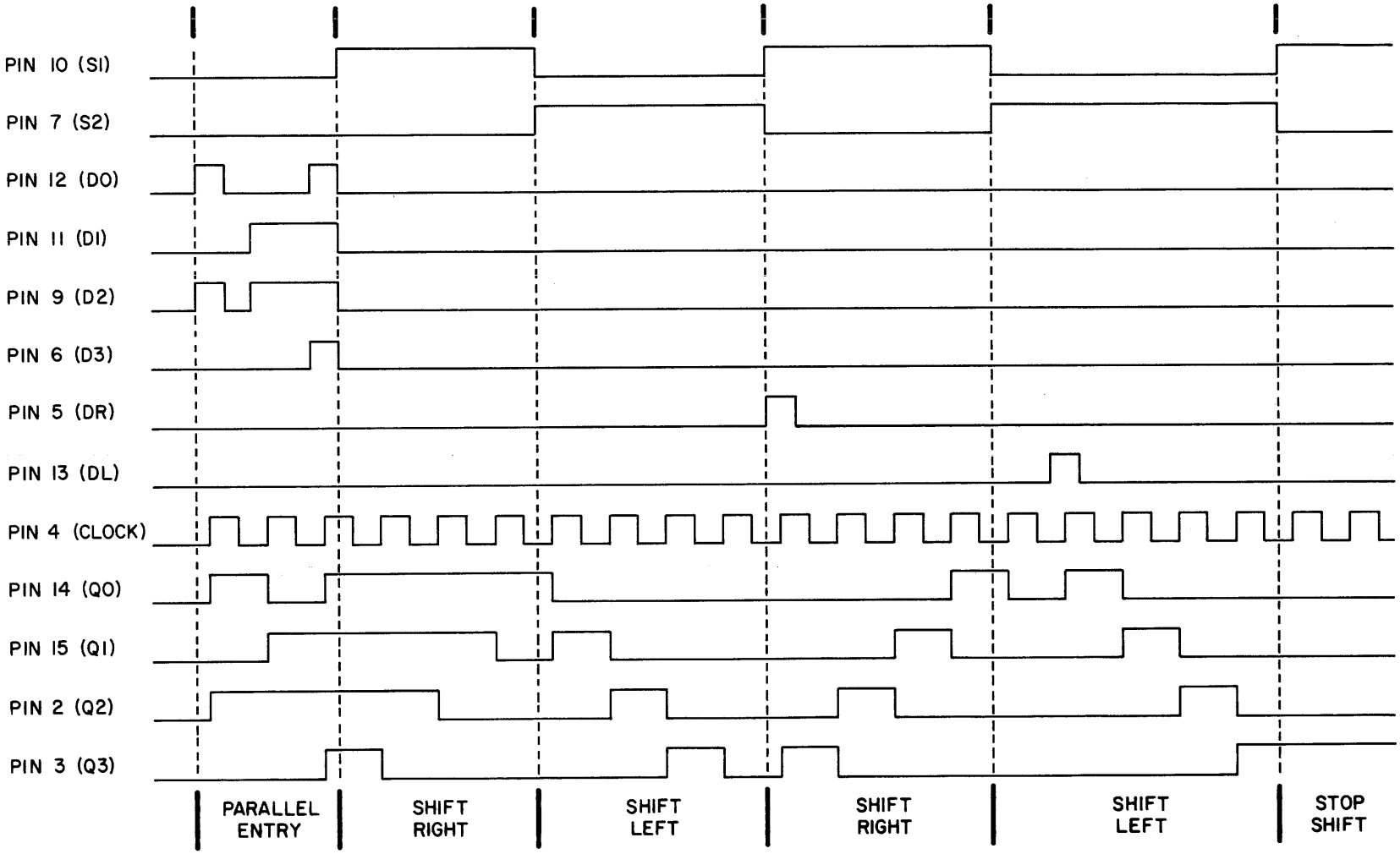
1. Vendor identification: MC10141

2. Package pin configuration:

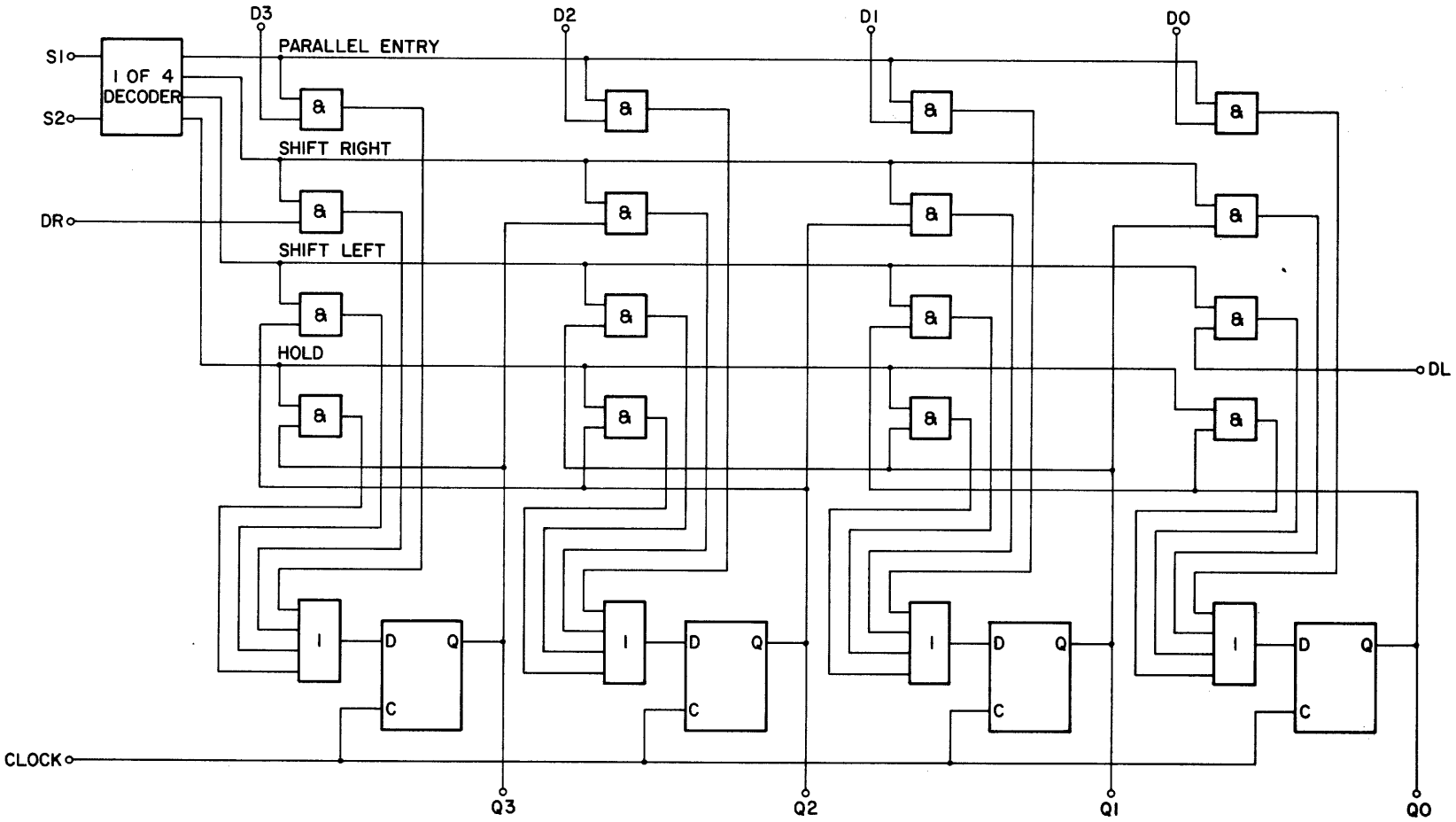


SELECT INPUTS		OPERATING MODE	OUTPUTS			
S2	S1		Q0n 1 (PIN 14)	Q1n 1 (PIN 15)	Q2n 1 (PIN 2)	Q3n 1 (PIN 3)
L	L	PARALLEL ENTRY	D0	D1	D2	D3
L	H	SHIFT LEFT	DL	Q0n	Q1n	Q2n
H	L	SHIFT RIGHT	Q1	Q2n	Q3n	DR
H	H	STOP SHIFT	Q0n	Q1n	Q2n	Q3n

n = BIT TIME BEFORE CLOCK PULSE
n+1 = BIT TIME AFTER CLOCK PULSE



TIMING DIAGRAM



FUNCTIONAL DIAGRAM

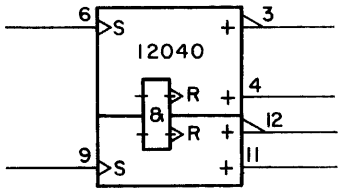
DESCRIPTION

The 12040 is a logic network designed for use as a phase comparator for ECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms.

Operation of the 12040 is best described by assuming that two waveforms of the same frequency, but differing in phase, are applied to input pins 6 and 9 (see timing diagram). If the logic had established by past history that the waveform at pin 6 was leading the waveform at pin 9, the output of the comparator at pin 4 would be a positive pulse whose width is equal to the phase difference; and the output at pin 11 would remain low.

If the logic had established by past history that the waveform at pin 9 was leading the waveform at pin 6, the output of the comparator at pin 11 would be a positive pulse width equal to the phase difference; and the output at pin 4 would remain low.

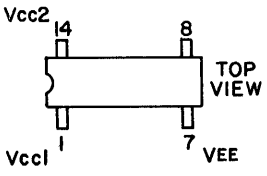
Both outputs for the sample condition are valid, since the determination of lead or lag is dependent on past edge crossings and initial conditions at start-up. A stable phase-locked loop will result from either condition. Phase error information is contained in the output duty cycle - that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the comparator, and by shifting the level to accommodate ECL swings, usable analog information for a voltage-controlled oscillator can be developed.

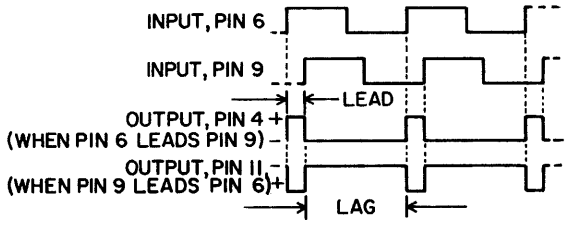


LOGIC SYMBOL

NOTES:

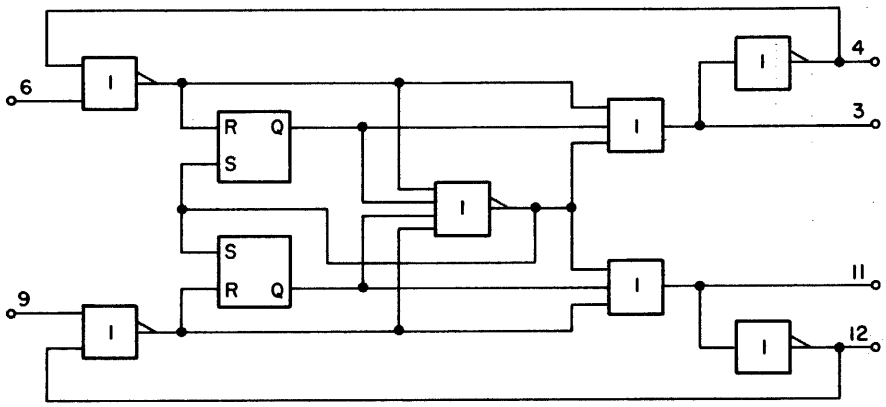
1. Vendor identification: MC12040
2. Package pin identification.





TIMING DIAGRAM

12040
Rev B
Sheet 1 of 2



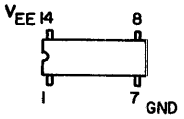
LOGIC DIAGRAM

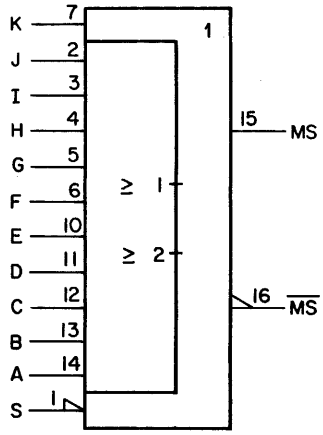
DESCRIPTION

This ECL circuit functions as an 11-input, multiple-select fault defector. Ten of the inputs, A through J, are monitored according to the state of S (mode select) when input K is low: If S is low, one or more of the ten inputs being in the high state will produce a fault indication (MS=H, $\overline{MS}$=L). If S is high, two or more of the ten inputs must be high to give the fault indication. A high on input K produces a fault indication regardless of the state of any of the other inputs, including S.

NOTES:

1. The part number is also the vendor number - 50255700.
2. Package pin configuration:

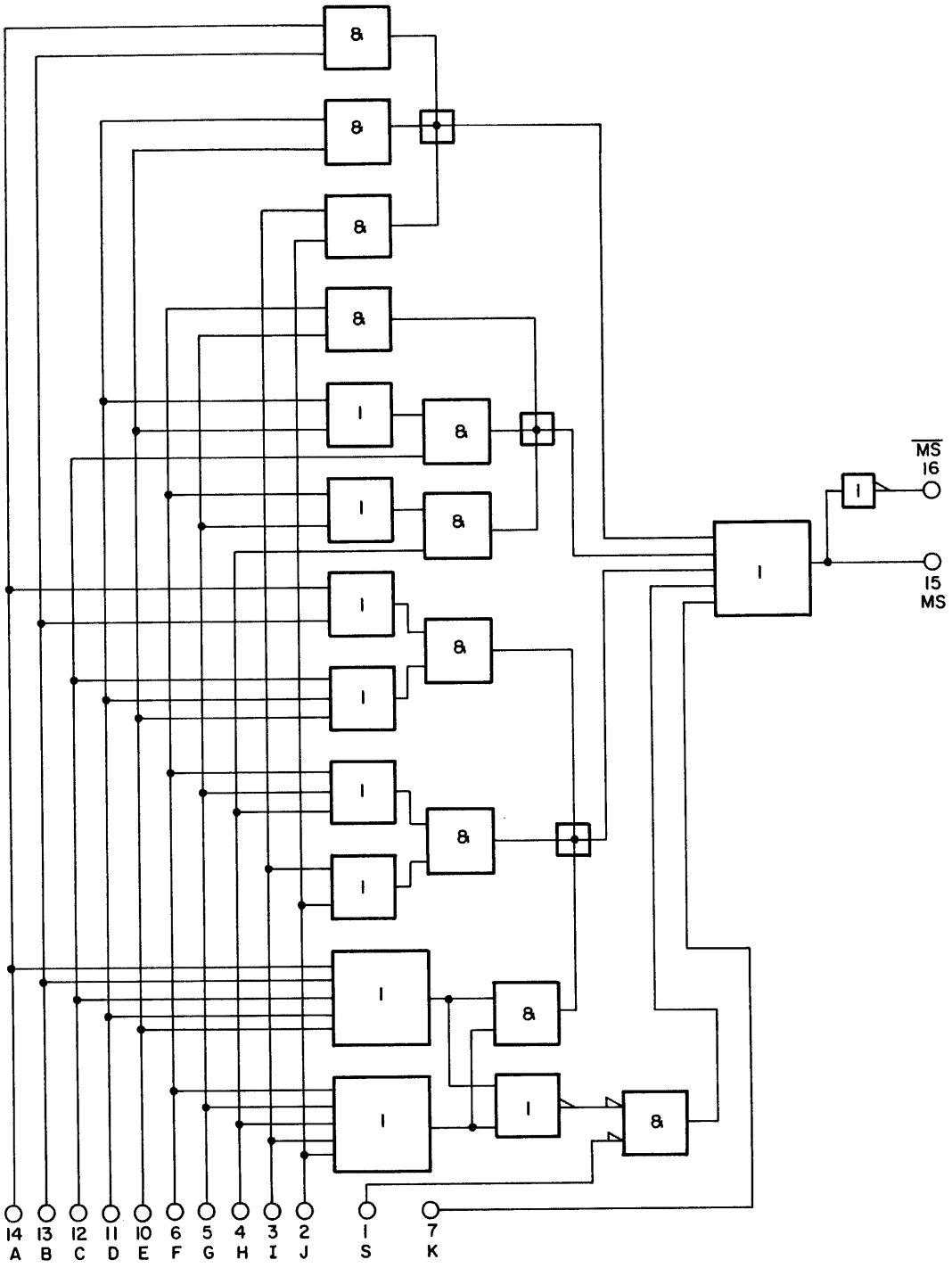




LOGIC SYMBOL

INPUTS			OUTPUTS		OUTPUT CONDITION
S	K	A THRU J	MS	$\overline{MS}$	
X	L	ALL INPUTS LOW	L	H	NO FAULT
H	L	ONLY ONE INPUT HIGH	L	H	NO FAULT
H	L	TWO OR MORE INPUTS HIGH	H	L	FAULT
L	L	ONE OR MORE INPUTS HIGH	H	L	FAULT
X	H	←——X——→	H	L	FAULT

TRUTH TABLE



FUNCTIONAL DIAGRAM

50255700
Rev A
Sheet 2 of 2

DATA SHEETS

ARRANGED BY

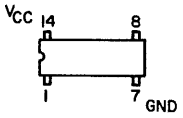
VENDOR IDENTIFICATION NO.

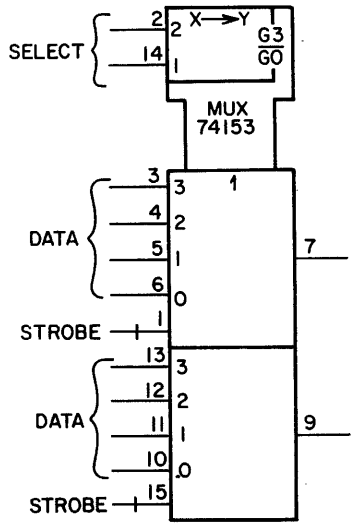
DESCRIPTION

The 74153 circuit is a dual 4-to-1 multiplixer with common binary select inputs and a separate inhibiting strobe input for each section. A logical one on the strobe holds the output pin for that section at a logical zero, regardless of the states of the select and data inputs.

NOTES:

1. Vendor identification: 74153/74S153
2. Package pin configuration:





LOGIC SYMBOL

INPUTS							OUTPUT
DATA				SELECT		STROBE	
0	1	2	3	2	1	⊓	
X	X	X	X	X	X	H	L
0	X	X	X	0	0	L	0
1	X	X	X	0	0	L	1
X	0	X	X	0	1	L	0
X	1	X	X	0	1	L	1
X	X	0	X	1	0	L	0
X	X	1	X	1	0	L	1
X	X	X	0	1	1	L	0
X	X	X	1	1	1	L	1

TRUTH TABLE

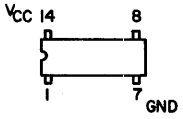
74153
Rev A
Sheet 1 of 1

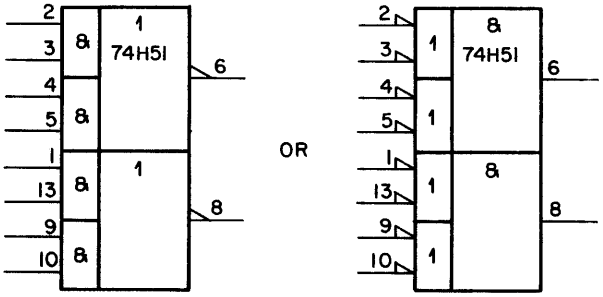
DESCRIPTION

The 74H51 circuit consists of two 2-wide, 2-input, positive AND-OR-INVERT gates in one package.

NOTES:

1. Symbol sections may appear separately.
2. Vendor identification: 74H51
3. Package pin configuration:





LOGIC SYMBOL

INPUT PINS				OUT-PUT PIN
2 (1)	3 (13)	4 (9)	5 (10)	6 (8)
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

AND-OR-INVERT

INPUT PINS				OUT-PUT PIN
2 (1)	3 (13)	4 (9)	5 (10)	6 (8)
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

OR-AND-INVERT

TRUTH TABLES

74H51
Rev A
Sheet 1 of 1

DESCRIPTION

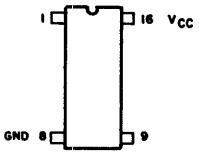
The 74LS221 circuit is a dual monostable multivibrator (one shot) with Schmitt-trigger inputs. Each section features a positive-transition-triggered input (A) and a negative-transition-triggered input (B), either of which can act as an inhibit input.

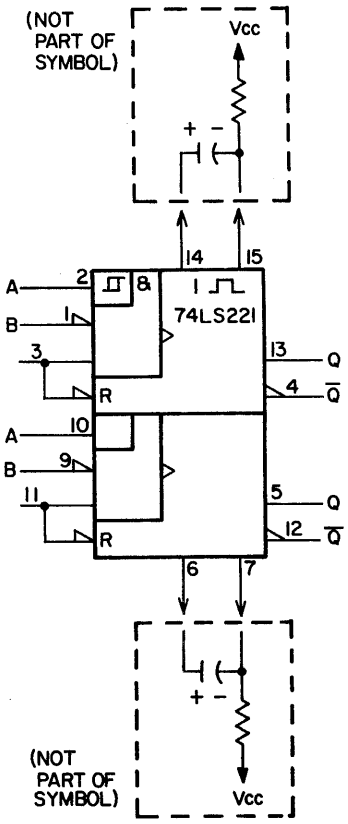
Triggering occurs at a particular voltage level and is not related to the transition time of the input pulse. Once fired, the outputs are independent of further input transitions (that is, the one-shot is not retriggerable). Bringing the Reset input low terminates any high-level output pulse.

Pulses from 30 ns to as long as 70 seconds are available with the proper external RC network.

NOTES:

1. Sections may appear separately.
2. Vendor identification: 74LS221
3. Package pin configuration:





LOGIC SYMBOL

INPUTS			OUTPUTS	
RESET	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	X	H	L	H
X	L	X	L	H
H	↑	L	⎍	⎏
H	H	↓	⎍	⎏

L = Low

H = High

↑ = L-to-H transition (input)

↓ = H-to-L transition (input)

⎍ = one high-level pulse (output)

⎏ = one low-level pulse (output)

X = don't care

TRUTH TABLE

74LS221
Rev A
Sheet 1 of 1

DESCRIPTION

The IM5603 circuit is a 1024-bit programmable read-only memory (PROM) organized as 256 words of 4 bits each. Open-collector outputs are provided.

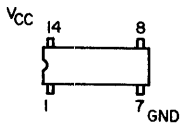
Logical ones are written into the memory using special equipment. Reading is accomplished by bringing the selected address bits high, while bringing both enable inputs (G) low.

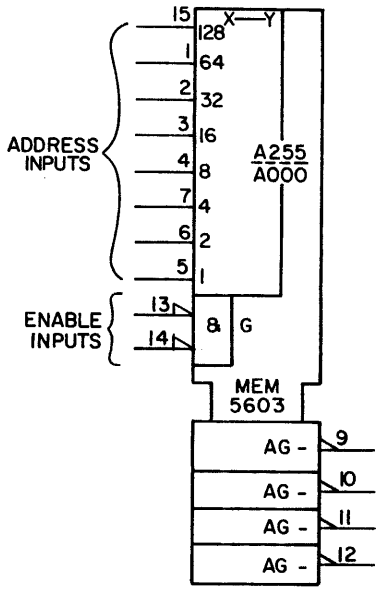
With either or both G-inputs high, the outputs are floating. Typical access time is 40 ns.

NOTES:

1. Vendor identification: IM5603

2. Package pin configuration.





LOGIC SYMBOL

IM5603
Rev A
Sheet 1 of 1

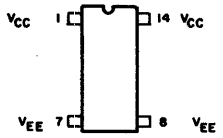
DESCRIPTION

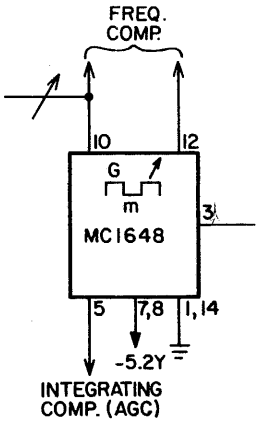
The MC 1648 circuit is an ECL voltage-controlled oscillator that may be operated from a +5 Vdc or a -5.2 Vdc supply, depending upon system requirements. The external tank circuit connected between pins 10 and 12 may also contain a varactor diode to provide a voltage-variable input for the VCO.

Maximum output frequency (typical) is 225 MHz.

NOTES:

1. Vendor identification: MC1648
2. Package pin configuration:





Replace 'm' with frequency or frequency range

LOGIC SYMBOL

MC1648
Rev A
Sheet 1 of 1

DESCRIPTION

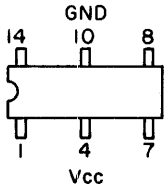
Element MC426 is a dual 3-input AND gate that may serve as a pulse shaper or a "1's" delay. The shaping function results from the inherent hysteresis of the Schmitt-trigger circuit. Note the threshold levels, which are a part of the pulse-shaper symbol.

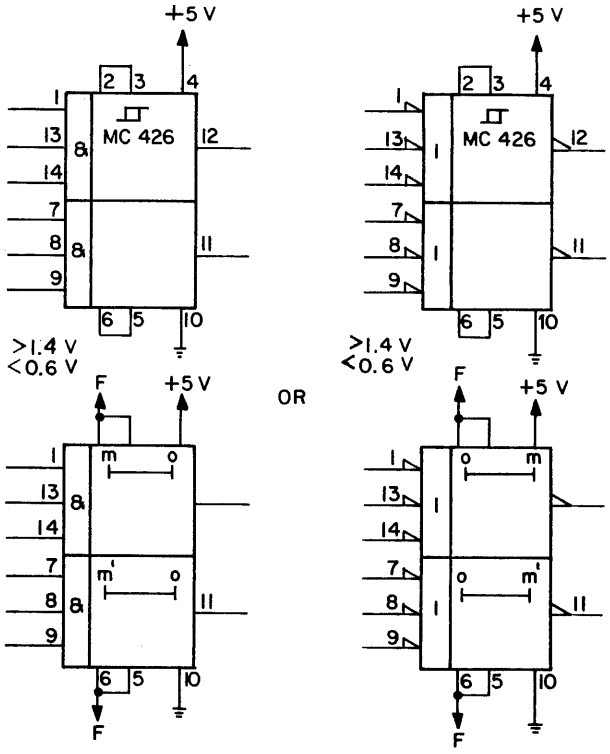
As a "1's" delay, a high input signal appears at the output after a delay period determined by the RC network. As shown by the timing diagram, the falling H-to-L) edge of the input signal is not delayed; if the signal drops before the expiration of the delay period, the output remains low.

The MC426 and the SNG83 are identical. The SNG82 differs in that it has a fan-out capability of 12, as opposed to 6 for the MC426/SNG83.

NOTES:

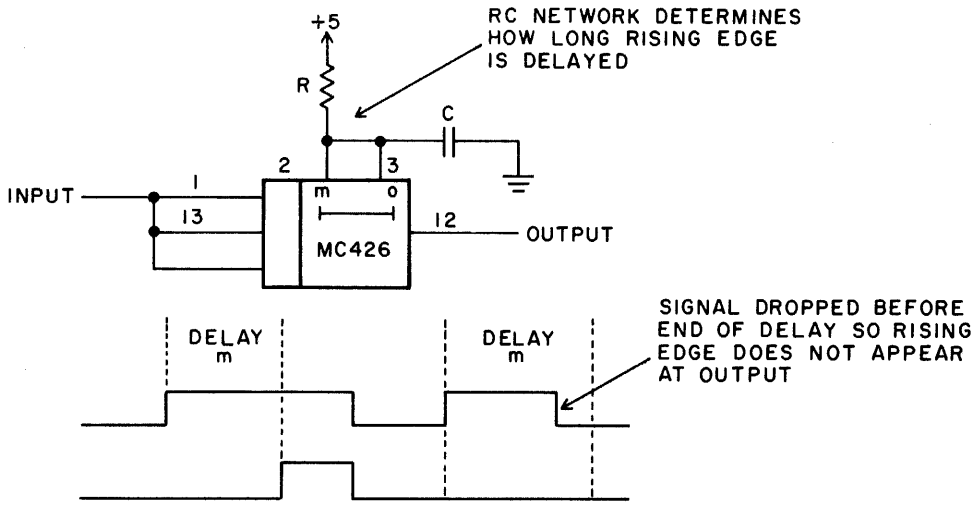
1. Replace m and m' with appropriate delay periods.
2. Vendor identification: MC426/SNG83, SNG82
3. Package pin configuration:





LOGIC SYMBOLS

MC426
Rev C
Sheet 1 of 2



FUNCTIONAL DIAGRAM
(FIRST SECTION)

APPENDIX A

GLOSSARY OF MICROCIRCUIT TERMINOLOGY

APPENDIX A

GLOSSARY OF MICROCIRCUIT TERMINOLOGY

The following terminology is used in this manual to describe microcircuit function and design.

base - (symbol B) The region that lies between an emitter and a collector of a transistor, and into which minority carriers are injected. It corresponds to the grid of an electron tube.

chip - The shaped and processed semiconductor die that is mounted on a substrate to form a transistor, diode, or other semiconductor device.

clock - A source of accurately timed pulses, used for synchronization in a digital computer or as a time base in a transmission system.

clocked flip-flop - Two flip-flops connected in a master-slave combination, to eliminate lay elements. The master flip-flop stores the input information when the clock voltage is high and transfers it to the slave when the clock voltage is low.

clock frequency - The master frequency of the periodic pulses that schedule the operation of a digital computer.

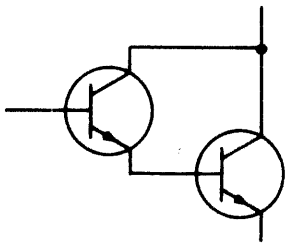
clock rate - The rate at which bits or words are transferred from one internal element of a computer to another.

collector - (symbol C) A semiconductor region through which a primary flow of charge carriers leaves the base of a transistor. The electrode or terminal connected to this region is also called the collector, and corresponds to the anode of an electron tube.

counter - A complete instrument for detecting, totalizing and indicating a sequence of events.

counter circuit - A circuit that receives uniform pulses representing units to be counted and produces a voltage proportional to the total count.

Darlington amplifier - A current amplifier consisting essentially of two separate transistors, often mounted in a single transistor housing. A Darlington amplifier has the same terminations as a single transistor.



decoder - A matrix network in which a combination of inputs produces a single output.

delay multivibrator - A monostable multivibrator that generates an output pulse a predetermined time after it is triggered by an input pulse.

demultiplexer - A device used to separate two or more signals that were previously combined by a compatible multiplexer and transmitted over a single channel.

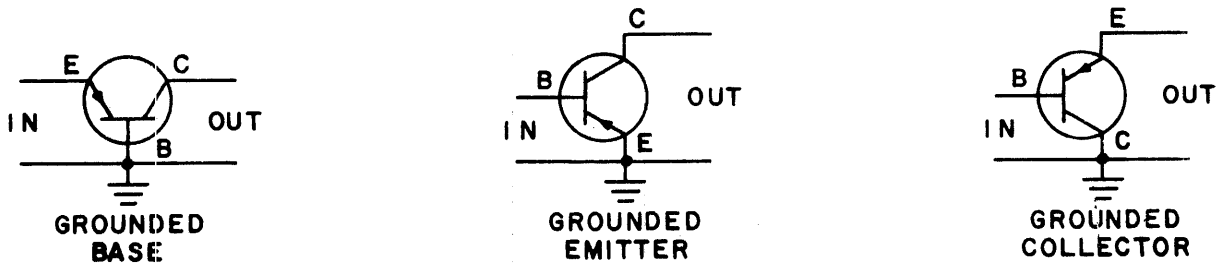
emitter - (symbol E) A transistor region from which charge carries that are minority carriers in the base are injected into the base. The emitter roughly corresponds to the cathode of an electron tube.

emitter follower - A grounded-collector transistor amplifier whose operation is similar to a cathode follower using a vacuum tube.

flip-flop circuit - A two-stage multivibrator circuit having two stable states. In one state, the first stage is conducting and the second is cut off. In the other state, the second stage is conducting and the first stage is cut off. A trigger signal changes the circuit from one state to the other, and the next trigger signal changes it back to the first state. For counting and scaling purposes, a flip-flop can be used to deliver one output pulse for each two input pulses. Also called bistable multivibrator, Eccles-Jordan circuit, and trigger circuit.

grounded-base amplifier - An amplifier that uses a transistor in a grounded-base connection.

grounded-base connection - A transistor circuit in which the base electrode is common to both the input and output circuits. The base need not be directly connected to circuit ground. Also called common-base connection.



grounded-collector amplifier - An amplifier that uses a transistor in a ground-collector connection.

grounded-collector connection - A transistor circuit in which the collector electrode is common to both the input and output circuits. The collector need not be directly connected to circuit ground. Also called common-collector connection.

grounded-emitter amplifier - An amplifier that uses a transistor in a grounded-emitter connection.

grounded-emitter connection - A transistor circuit in which the emitter electrode is common to both the input and output circuits. The emitter need not be directly connected to circuit ground. Also called common-emitter connection.

integrated circuit - An interconnected array of active and passive elements integrated with a single semiconductor substrate or deposited on the substrate by a continuous series of compatible processes, and capable of performing at least one complete electronic circuit function. Normally, only the input, output, and supply terminations are accessible. Also called monolithic circuit and monolithic integrated circuit. When transistors or other discrete components are separately mounted and connected, it is a hybrid integrated circuit.

microcircuit - Generic term for all types of microminiature or microelectronic circuits, including hybrid microcircuits, integrated circuits, thin-film circuits, and monolithic circuits.

microcircuitry - The complete assembly of microcircuits used in a piece of electronic equipment. Also called microelectronic circuitry and microminiature circuitry.

microcircuit wafer - A microwafer containing one or more complete operating microcircuits or stages.

monostable multivibrator - A multivibrator with one stable and one unstable state. A trigger signal is required to drive the unit into the unstable state, where it remains for a predetermined time before returning to the stable state. Also called one-shot multivibrator, single-shot multivibrator, and start-stop multivibrator.

multiplexer - A device for combining two or more signals.

multivibrator - A relaxation oscillator using two tubes, transistors, or other electron devices, with the output of each coupled to the input of the other through resistance-capacitance elements or other elements to obtain in-phase feedback voltage. The fundamental frequency is determined by the time constants of the coupling elements and may be further controlled by an external voltage. When such circuits are normally in a nonoscillating state and a trigger signal is required to start a single cycle of operation, the circuit is commonly called a one-shot multivibrator, a flip-flop circuit, or a start-stop multivibrator.

reference voltage - Reference voltages are typically specified with respect to ground. Unfortunately, there is no industry standard for the various symbols that denote these voltages. Meanwhile, the explanations below hold for this manual, and are generally applicable.

V_{BB} - (Bias) The bias voltage may be produced by an external bias supply or generated internally on each card (or within each IC package). In the latter case, V_{BB} is usually brought out to a connecting pin so as to provide a uniform bias to all applicable circuits.

V_{CC} - (In bipolar (TTL,DTL) and ECL circuits, this term indicates the most-positive supply voltage. In ECL circuits, V_{CC} is typically ground.

V_{DD} - (Drain) In CMOS circuits, this term is generally used in place of V_{CC} to indicate the most-positive supply voltage. When CMOS is used in combination with ECL, V_{DD} is typically ground.

V_{EE} - In ECL circuits, this term indicates the most-negative supply voltage.

V_{SS} - (Source) In CMOS circuits, this term indicates the most-negative supply voltage. When CMOS is used in conjunction with ECL, both V_{SS} and V_{EE} may be used to identify the same (-5.2 V) supply voltage. Often, however, the -5.2 V ECL supply (V_{EE}) may not offer sufficient potential to gain the required speed from the CMOS circuits, and a higher-potential supply (V_{SS}) is necessary. In such cases, V_{SS} and V_{EE} specify different voltages.

reset - Clear.

reset pulse - 1. A drive pulse that tends to reset a magnetic cell in the storage section of a digital computer. 2. A pulse used to reset an electronic counter to zero or to some predetermined position.

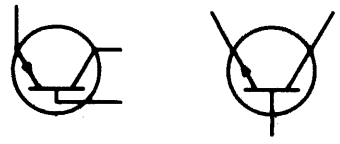
Schmitt trigger - A bistable trigger circuit that converts an a-c input signal into a square-wave output signal by switching action, triggered at a predetermined point in each positive and negative swing of the input signal.

shift - Displacement of an ordered set of characters one or more places to the left or right in a digital computer. If the characters are the digits of a numerical expression, a shift may be equivalent to multiplying by a power of the base.

shift pulse - A drive pulse that initiates shifting of characters in the register of a digital computer.

shift register - A computer circuit that converts a sequence of input signals into a parallel binary number or vice versa, by moving stored characters to the right or left.

transistor - (TRANSfer resISTOR) An active semiconductor device having three or more electrodes. The three main electrodes used are the emitter, collector, and base.



Conduction is by means of electrons and carriers or holes. Germanium and silicon are the materials most often used as the semiconductor material. Transistors can perform practically all the functions of tubes, including amplification and rectification.

transistor-transistor logic - A logic circuit containing two transistors, for driving large output capacitances at high speed.

triggering - Initiation of an action in a circuit, which then functions for a predetermined time.

trigger circuit - 1. A circuit or network in which the output changes abruptly with an infinitesimal change in input at a predetermined operating point. Also called trigger. 2. A circuit in which an action is initiated by an input pulse, as in a radar modulator. 3. Flip-flop circuit.

truth table - A table that describes a function by listing all possible combinations of input values and indications for the output.

AND

B	A	C
L	L	L
L	H	L
H	L	L
H	H	H

OR

B	A	C
L	L	L
L	H	H
H	L	H
H	H	H

NAND

B	A	C
L	L	H
L	H	H
H	L	H
H	H	L

Truth tables for three gating functions.

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