GENERAL DESCRIPTION OF THE 274 DISPLAY CONSOLE AND THE 1744 CONTROLLER

CONTROL DATA CORPORATION

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PREFACE

This document contains a general description of the 274 display console and the 1744 controller. Since the 274/1744 system is designed to operate interfaced to a Control Data® 1700 Computer System, the following references are given to assist the reader in understanding this document.

1. Control Data 1700 Computer System, Computer Reference Manual, Publication No. 60153100.

2. Control Data 1700 Computer System, Operating System Manual, Publication No. 60174600.

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1.0 INTRODUCTION

The 274/1744 Digigraphic hardware consists of the 274 graphic console, the 1744 controller, an AQ channel and/or a 1706 data channel for communication with the 1700. Although the hardware interface allows the 1744 controller to use an AQ channel, the high speed 1706 buffered data channel is recommended and required in order to make use of the standard Control Data Corporation graphic software.

1708 storage modules are used for core storage in the 1700 computer and the 1744 controller. To avoid confusion within this document, the core memory contained in the controller is referred to as buffer memory. The 1700 memory is referred to as core memory.

Data can be transferred from the 1700 to the display by two routes. The principle route is from the 1700 to the buffer memory for off-line storage of display information. Once the buffer memory holds the desired display information, the display at the console is refreshed in an off-line mode without intervention by the 1700. The 1700 is used only in short bursts to change display information and process operator inputs.

Data can also be transferred from the 1700 directly to the display console. This route uses the 1700 core memory as the buffer memory and data is transferred across the data channel, through the controller, to the console for every refresh cycle. The data transfer rate is a function of a 600 KC clock in the controller. This allows

the transfer of a 16-bit word every 1.67 microseconds and requires a 1706 buffered data channel.

The refresh rate is set in the controller at a maximum of 40 cycles per second. If a display requires more than 25 milliseconds per cycle, the controller allows as much time as is required to reach the end of display command before starting the next cycle. The time between the end of display command and the start of the next display cycle can be used for display editing functions.

2.0 274 CONSOLE

The 274 console is the input/output and human control center of the system. The console is designed for maximum operator utilization, and it can be used efficiently at normal room light levels.

2.1 274 PHYSICAL CHARACTERISTICS

The console cabinet is a desk size unit which mounts a rectangular housing assembly, off-centered to the left, providing desk space to the right. The housing assembly contains a magnetic shield and a 20-inch useable diameter CRT centered on the front panel housing. Options are available to allow the console to be adjusted manually. The range of adjustment allows the tube face and front panel to be moved through approximately 60 degrees of slope, at increments of 10 degrees, starting at 15 degrees from the horizontal.

The console cabinet is equipped with fixtures to mount the complement of logic cards required to receive and transmit logic levels, convert digital input to analog signals for deflecting the CRT beam, and to control beam intensity. The console is equipped with a light-pen as described in paragraph 2.1.1 and has options for an alphanumeric keyboard, numeric keyboard, and a variable function keyboard. The optional keyboards are described in Appendix A.

A set of switches along the top rim of the housing assembly panel are used to control system operation. One of the switches

can be used as a "push to talk" switch for remote communication. A loudspeaker, located to the left of these switches, can be connected to an intercom.

The 20-inch CRT is a precision, 52-degree, high resolution unit having a nearly flat display surface to minimize parallax error. The CRT is equipped with an implosion shield for the protection of the operator.

2.1.1 Lightpen

The lightpen is attached to a fiber optics cable which is terminated with a photo-multiplier. The lightpen is held in the hand and is used to identify display items. The lightpen contains no shutter device to restrict passage of light. It is fitted with a switch that can be programmed to control lightpen operations.

2.2 Phosphor

The CRT is coated with a P-7 phosphor which is deposited in two layers. One layer produces blue-violet light with a short persistence to facilitate lightpen operations. The other layer produces yellow-green light with a considerably longer persistence. The two layers displayed together appear light-blue to the human eye.

2.3 Display Addressing, Resolution, and Repeatability

The deflection yoke and driving circuitry of the console provide a full 52 degrees of beam deflection to make the entire 314

square inches of display surface available for display. The CRT has a resolution of 1000 lines in 20 inches and the position of any point within a 14 by 14 inch centered square can be specified to one-tenth of one percent.

The position of the beam is determined by 12-bit X and Y accumulators. The spacing between each addressable point is approximately .005 inch (20 inches divided by 4096 addressable coordinates in X and Y). Since the resolution of the CRT is 1000 lines in 20 inches, the least significant bit of the X and Y accumulator values is dropped for display purposes. Therefore, the CRT is addressed by a 4096 x 4096 grid but has a resolution of a 2048 x 2048 grid. Figure 1 illustrates the display grid system.

The normal bright line width is .02 inch when measured at the 50% intensity levels with an image splitting microscope. The stability of the display is such that the image does not shift more than a line width over an 8-hour period. The short term repeatability, that is from frame to frame, is such that the image does not shift more than one-half of a line width in a 40-frame period.

3.0 1744 CONTROLLER

The 1744 controller interfaces with a 1700 AQ channel and/or a 1706 buffered data channel to accept commands and display information received from the 1700 for one 274 console. The peripheral equipment device code used to select the controller is manually set with four toggle switches on the front of the controller. The controller is selected under program control when the equipment code matching the toggle switch setting is set into bits 7 - 10 of the computer Q register as described in paragraph 3.2. Figures 2 and 3 describe the system in block diagram form and indicate the cable lengths allowed between the 1700, 1744, and 274.

The controller uses a 1708 storage module of 4096 16-bit words for the buffer memory. This memory can be expanded to 8192 16-bit words by adding another storage module in the controller. Since the storage module in the controller is the same as the storage modules in the 1700, controller memory can be used as buffer memory for display or as auxiliary storage. When the controller memory is used as buffer memory, only bits 0 through 11 (with the exception of function and status codes) are interpreted by the display. When the controller memory is used as auxiliary storage, all 16-bits can be used as random access storage.

3.1 1744 Control Registers

The controller has three main registers that are used to process the control comands stored in its buffer memory.

3.1.1 S Register

The S register is used to address the storage module(s) and select the locations for input or output. It is a 13-bit register capable of being incremented by one or set to a new value. Thirteen bits are required to address up to 8192 locations.

3.1.2 P Register

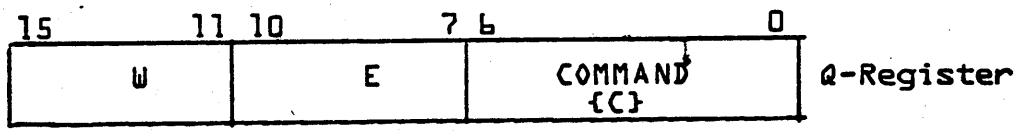
The P register is a 13-bit register which maintains the address of a location within the display commands. The P register can be incremented by one or set to a new value.

3.1.3 Z Register

The Z register is a 16-bit register used as the central data holding register. All data except the function codes and interrupt status codes pass through the Z register.

3.2 1744 Input/Output

The 1744 controller reacts to 1700 input (INP) and output (OUT) instructions. The input/output operation is specified by the contents of the A and Q registers in the 1700 as described in Table 1. The A register holds function codes, accepts status bits, or serves to transfer data in and out of the computer when the AQ channel is used. The addition of the 1706 buffered data channel enables data transfer to and from memory independent of the internal operation of the computer. In the buffered mode, the A and Q registers are only used to initiate the operation. The A register contains an address indicating the area of memory in the 1700 from which data will be output or in which data will be read. The format of the 16-bit Q register is given below for both AQ channel and 1706 buffered data channel input/output operations. Appendix B of this document contains additional 1700 input/output information.



1. W - Zero for all communication with the 1744 when the AQ/1705 transfer path is used and the 1706 equipment code when the 1706 transfer path is used.
2. E- The peripheral equipment device code of the desired 1744 controller on the channel.
3. Command (C)- Controls and directs the data transfer to and from the 1744.

3.2.1 AQ Input/Output

Input/Output operations on an AQ channel may be performed on

a maximum of 8 devices. Input on the AQ channel is initiated by an input to A instruction. The 4-bit code assigned to the desired 1744 controller is the E portion of the Q register as described in paragraph 3.2.

Bits 0 through 6 of the Q register are used to specify the desired operations such as data transfer, control functions, and status requests.

Output on the AQ channel begins with an output from A instruction with the 4-bit code assigned to the 1744 controller in the E portion of the Q register. When an input to A instruction is executed, the data from the 1744 is loaded into the A register.

3.2.2 1706 Buffered Input/Output

Buffered input/output may be performed on a maximum of 8 peripheral devices per channel through the use of the 1706 buffered data channel. The 1706 receives commands via the 1705 interrupt data channel and transfers blocks of data directly in and out of storage using the direct storage access bus. The maximum data rate is one word every storage cycle (1.1 microseconds). Input/Output on the 1744 controller is timed at a maximum of one word every 1.67 microseconds to allow the same timing between the 1700 and 1744 as exists between the 1744 controller and the 274 console. This rate is required for on-line display operations. The function code which enables the on-line display sets the 1700 priority pause condition to assure the high speed transfer. Normal data transfers between the 1700 and 1744 are at a slower rate.

3.2.3 1744 Input

The 7 input operations available on the 1744 are specified by the A and Q registers. The A register holds the input data on AQ channel requests or the address specifying the input data area for 1706 buffered requests. The Q register has W = 0 or the 1706 equipment code (bits 11 - 15), E = the 1744 device code (bits 7 - 10), and C = to the code for the specific operation (bits 0 - 6). The following paragraphs describe the specific input operations.

3.2.3.1 Read Status (C = 0). The 1744 status word is input. The interpretation of the 1744 status word is defined in Table 2.

3.2.3.2 Read Buffer Memory (C = 1). The contents of the 1744 buffer memory specified by the S register are input. The S register is incremented by one after each word is transferred.

3.2.3.3 Read S and P Control Registers (C = 2, C = 3). When C = 2, the contents of the S register are read into the low order 13-bits of the A register or computer memory. When C = 3, the contents of the P register are read into the low order 13-bits of the A register or computer memory.

3.2.3.4 Read X and Y (Beam Position) Registers (C = 4, C = 5). When C = 4, the contents of the 1744 controller X register are transferred to the low order 12-bits of the A register or computer memory. When C = 5, the contents of the 1744 controller Y register are transferred. The contents of the X and Y registers allows the software to obtain the coordinate locations for lightpen operations (i.e. strikes).

3.2.3.5 Search and Read Identification Bytes (C = 6). The 1744 controller initiates a search for identification bytes as described in paragraph 3.4.4. The search starts at the location in the S register. When the first identification byte is found, it and the following identification bytes are transferred until the number of bytes specified by the input operation are reached. Non-identification bytes are not transferred.

The search and read identification bytes capability allows the software to obtain additional information about a lightpen strike beyond the normal X, Y coordinate information. This identification information can be used by the software to initiate the response required for a lightpen selection. The amount and type of information stored in the identification bytes is under software control.

3.2.4 1744 Output

The 5 output operations available on the 1744 are specified by the A and Q registers. These registers function for output operations similar to their input functions described in paragraph 3.2.3. The following paragraphs describe the specific output operations.

3.2.4.1 Function Codes (C = 0). The function codes direct the 1744 controller to perform specific operations as described in Table 3. The function code is broken down into groups with the least significant digit used for clearing interrupts. Another hexidecimal digit is the enable digit and is used to set the enable flip-flops for interrupts. There are two flip-flops associated with lightpen

interrupts. One flip-flop allows a lightpen interrupt to occur without stopping the display. A stop display flip-flop is the second lightpen flip-flop which allows the software to identify a lightpen strike. When the stop display flip-flop is set and a lightpen strike occurs, the display logic stops and locks the X and Y coordinates of the display as well as the S and P registers. An interrupt is generated to allow the software to interrogate the 1744 status and the X, Y, S, and P registers to determine the position of the lightpen strike. The lightpen switch has interrupt logic associated with it to allow the software to determine when to prepare for a lightpen strike interrupt (i.e. when the lightpen switch is depressed).

3.2.4.2. Write Buffer Memory (C = 1). Sixteen bits of data are written in the 1744 buffer memory starting at the location specified by the S register. The S register is automatically incremented by one after each word is transferred. If the data transferred is a display byte, the 12-bit byte must be right justified since the control byte logic of the 1744 controller does not interpret bits 12 through 15.

3.2.4.3 Set the S Register (C = 2). Thirteen bits of data are written into the S register. This allows the S register to be initialized for 1744 data transfers.

3.2.4.4 Computer Display (C = 3, C = 4). When C = 3, the low order 12-bits of data from the 1700 is sent through the 1744 controller to the 274 console and the display is refreshed on-line. The on-line

display returns to the off-line or controller display on completion of the data transfer. When C = 4, the 1744 controller remains connected for on-line display after completion of the data transfer.

3.3 1744 Commands Bytes

The 1744 controller recognizes the following commands while stepping through its memory during a display cycle:

1. S jump *
2. M jump *
3. P jump *
4. RTM (return to main) *
5. EDB (end of display byte)
6. ROD (return to off-line display)
7. ELP (enable lightpen sense)
8. DLP (disable lightpen sense)

NOTE: * These command bytes should not occur in an on-line 1700 display buffer.

The X's shown in the bit configurations in paragraphs 3.3.1 through 3.3.8 indicate the specific bit is ignored by the controller. The 12-bit configuration is referred to as a command byte and is right justified in the 16-bit controller memory.

3.3.1 S Jump (Byte = X001 1100 1XXX)

This command is identical to the unconditional jump in a computer. The 1744 executes a jump to the location specified by the next byte and continues stepping sequentially from there.

3.3.2 M Jump {Byte = X001 1110 1XXX}

This command, in conjunction with the return to main command {paragraph 3.3.4}, provides a capability equivalent to a return jump in a computer. When the 1744 encounters an M jump at location S, it executes a jump to the location specified by S + 1, and holds the address S + 2 in the 1744 P register. When a return to main command is encountered, a jump to the address in the P register is executed.

3.3.3 P Jump {Byte = X001 1101 1XXX}

The P jump provides an efficient way to operate a series of macro routines as described in paragraph 3.3.9. When the 1744 encounters a P jump, the 1744 initiates a jump to the address which is stored at the location specified by the P register and then increments the P register by 1. The P jumps can be used in this manner until a return to main command is encountered.

3.3.4 Return to Main {Byte = X001 1111 1X10}

This command is used in conjunction with the M jump and P jump commands. When the 1744 encounters a return to main command, it initiates a jump to the address in the P register and continues stepping sequentially from there.

3.3.5 End of Display Byte {Byte = X001 1111 1000}

This command used with the interrupt system allows the byte stream to generate an interrupt when the end of display byte is

processed. This allows the software to process input/output operations during the time following the end of display up to the start of the next 25 millisecond refresh period. When the 25 millisecond clock in the 1744 elapses and no input/output or display bytes are being processed, a 5 microsecond pause occurs, the S and P registers in the 1744 are set to zero, and the display processing starts again at address 0 in the 1744 buffer memory. This 25 millisecond clock provides the 40 cycles per second refresh rate.

3.3.6 Return to Off-Line Display {Byte = X001 1111 1100}

This command can be used along with other display data transferred to the 1744 controller during on-line or computer display. This command returns the on-line display to the 1744 controller off-line display.

3.3.7 Enable Lightpen Sense {Byte = X001 0100 1001}

The enable lightpen command allows the display bytes following the command to be sensitive to the lightpen. The lightpen interrupt in the 1744 controller must be enabled to allow the lightpen strike to interrupt the 1700.

3.3.8 Disable Lightpen Sense {Byte = X001 0100 1000}

The disable lightpen command inhibits the display bytes following the command to be sensitive to the lightpen.

3.3.9 Macros

Display items that are used in various areas of the CRT can be stored in the buffer memory as macros to obtain maximum utilization

of the core space in the buffer. The macros can then be referenced by a macro call {M jump}. The M jump causes a return address to be held in a 1744 register and initiates a transfer of display control to the addressed macro. The macro can either return directly to the return address by using a return to main command byte or transfer control to another macro addressed from the location held in the 1744 register. Since the return address is held in a 1744 register, only one level of macro calls is provided {i.e. a macro may not include a call to another macro}.

The following example describes a sequence of commands to display the word CAT.

S	M jump
S+1	Address of C macro
S+2	Address of A macro
S+3	Address of T macro
S+4	Address of Return to Main macro
S+5	Continue

The byte stream for each character in the above example is terminated with a P jump. The return to main macro is required to get out of the P jump loop and back to normal display sequencing. The return to main macro is a one word macro which contains the return to main command byte described in paragraph 3.3.4.

3.4 1744 Display Control Bytes

The following 7 display control bytes are interpreted by the

display logic of the 1744 controller.

1. Reset - Coarse beam positioning
2. Increment - Fine beam positioning
3. Intensity - Establish one of three intensity levels
4. Identity - Allows display identification within the display byte stream
5. Terminate - Terminate the display until a reset byte is encountered (should not be in an on-line 1700 display buffer)
6. Blink - Enables a selected graphic to blink
7. No-blink - Terminates blinking

3.4.1 Reset Byte

The reset byte is usually the first byte in any series. It is a coarse positioning byte which moves the CRT beam to an approximate position on the display surface and sets the beam to one-half normal intensity. Reset bytes are usually followed by increment bytes (paragraph 3.4.2) within the byte series to establish the precise point for display initiation.

The format for the reset byte is as follows:

11	10	09	08	07	06	05	04	03	02	01	00
1	0	0	0	X	X	X	X	Y	Y	Y	Y

When bits 11, 10, 09, and 08 = 1000, a reset byte is designated and bits 07, 06, 05, and 04 are jammed into the high order bit positions of the controller X accumulator with the remaining bits set to zero. Bits 03, 02, 01, and 00 are jammed into the high order bit

positions of the controller Y accumulator with the remaining bits set to zero. If the sign bit is 1 (negative), the value bits are in 1's complement form. The reset byte has no control over the beam on/off state and will follow the beam state of the previous byte.

3.4.2 Increment Byte

The increment byte is the primary beam moving control byte. In normal operations, an initializing reset byte is used for coarse positioning of a displayed graphic. Increment bytes with the beam off establish the precise display starting coordinates. Intensity bytes (paragraph 3.4.3), lightpen enable/disable bytes (paragraphs 3.3.7 and 3.3.8), and the blink/no-blink bytes (paragraph 3.4.6) can be in the reset section of the byte stream for a displayed graphic. Once the desired starting coordinates and display control are established, increment bytes, the first of which turns the beam on, display the desired graphic.

The format for the increment byte is as follows:

11	10	09	08	07	06	05	04	03	02	01	00
B	SF			X	Δx			Y	ΔY		

Bit 11 (B) is the beam control bit; 0 = beam off, 1 = beam on. Bits 10, 09, and 08 are binary weighted scale factors and function

as the Δx and Δy value multipliers. The scale factor range is from 2 through 7, corresponding to scale factors of 1:1 through 32:1, respectively.

The following values clarify the scale factors:

SF=7, 32:1= .16 inch
SF=6, 16:1= .08 inch
SF=5, 8:1= .04 inch
SF=4, 4:1= .02 inch
SF=3, 2:1= .01 inch
SF=2, 1:1=.005 inch

} per 1 unit in Δx or Δy

The smallest ratio for CRT beam motion is 2:1 because the electronics in the 1744 controller maintain an accuracy of 4096 x 4096 addressable points while the 274 console maintains a resolution of 2048 x 2048 points.

Bit 07 is the X sign bit and bits 06, 05, and 04 are added to the current X accumulator value after being shifted left the number of bit places specified by the scale factor.

Bit 03 is the Y sign bit and bits 02, 01, and 00 are added to the current Y accumulator value after being shifted left the number of bit places specified by the scale factor.

A delay function is performed by a special case increment byte. The following code:

0XXX 1111 1111, where X is any valid scale factor, produces a 25 microsecond delay to facilitate beam settling time

and should be used before the first increment byte following a reset byte.

3.4.3 Intensity Byte

The intensity byte sets the beam intensity control to one of three levels; one-half normal intensity, normal intensity, or twice normal intensity. Once the intensity is established, the intensity level remains unchanged until a reset byte is processed or another intensity byte occurs. The codes for the three cases are given below.

B001 XXXX 0001 1/2 normal

B001 XXXX 001X normal

B001 XXXX 01XX 2 x normal

The X's in all cases are the bits that are ignored by the controller. Bit 11 (B) controls the beam on/off state. A 1 turns the beam on and a 0 turns the beam off.

3.4.4 Identification Byte

The identification byte has an 8-bit identification parameter in its format. The high order four bits (11-8) are all zeroes, indicating that this is an identification byte. The low order 8-bits (7-0) contain the identification parameter. The system can be programmed to perform an ID read operation which searches for these bytes and stores them in a system buffer (paragraph 3.2.3.5).

3.4.5 Terminate Byte

The terminate byte is used to terminate display until a reset byte is encountered. The 1744 controller "simulates" a terminate byte

whenever the normal display byte stream is interrupted for an input/output transfer or any other reason. The section of the display that was interrupted is non-displayed until a reset byte is decoded and a new section of the display is started. The code is:

X001 0100 11XX, where X indicates the bit is ignored by the controller.

3.4.6 Blink/No-Blink Bytes

The blink and no-blink bytes are used when a displayed graphic is selected to blink. Blinking consists of a graphic being displayed for 10 frames and non-displayed for 10 frames. The formats are given below.

Blink	X001 0100 1011
No-Blink	X001 0100 1010

X's in both formats indicate the ignored bit.

3.5 Summary of 1700/1744/274 Operation

Figure 2 shows a general block diagram of the 1700/1744/274 graphic system. During display mode, the command decoder and the byte decoder interpret each byte. If the byte is an incremental, brightness control, or reset, the byte decoder interprets each one individually with no action by the command control decoder. If

the byte is a command byte, the command control decoder decodes the byte and initiates the next step in the internal program with no action by the byte decoder. An identity byte is ignored by both decoders. With an incremental byte, the 12-bit decoder breaks open the 12-bits, determines the scale factor and the delta X and delta Y quantities, and transmits them to the high speed adder.

The high speed adder takes the delta X information first and adds it to the present X coordinate and generates a new position which is transmitted to the console interface. It then returns and sums the delta Y information with the present Y coordinate and enters this into the console interface. At the same time that the Y coordinate is entered into the console interface and transmitted across the interface to the display unit, the new X coordinate is transferred with it.

The entire controller operates at a basic clock frequency of 600 KC and has a refresh rate of 40 cycles per second. This 40 cycle per second rate is used to initiate a redisplay of information which is stored in the 1744 buffer memory. When the display is completed, the priority status bit is set. The priority bit may also be used to generate an interrupt if a function code has previously been issued. This priority bit can be used to signal the software that the display has been completed. The software can then enter or extract information from the 1744 controller during the non-display time.

4.0 REFERENCES

1. "Control Data® 1700 Computer System Manual", Control Data Corporation, Publication Number 60152900, February 1967.

2. "Preliminary Study Guide for the 1744 Digigraphic System", Control Data Corporation, January 17, 1968.

3. "Product Specification for the Digigraphic System 1744 Controller with 1700 Series Interface", Control Data Corporation, Revised November 1967.

4. "External Reference Specification, 33/3500 Master Mark 4.0, Digigraphic Control Package", Control Data Corporation, June 5, 1968.

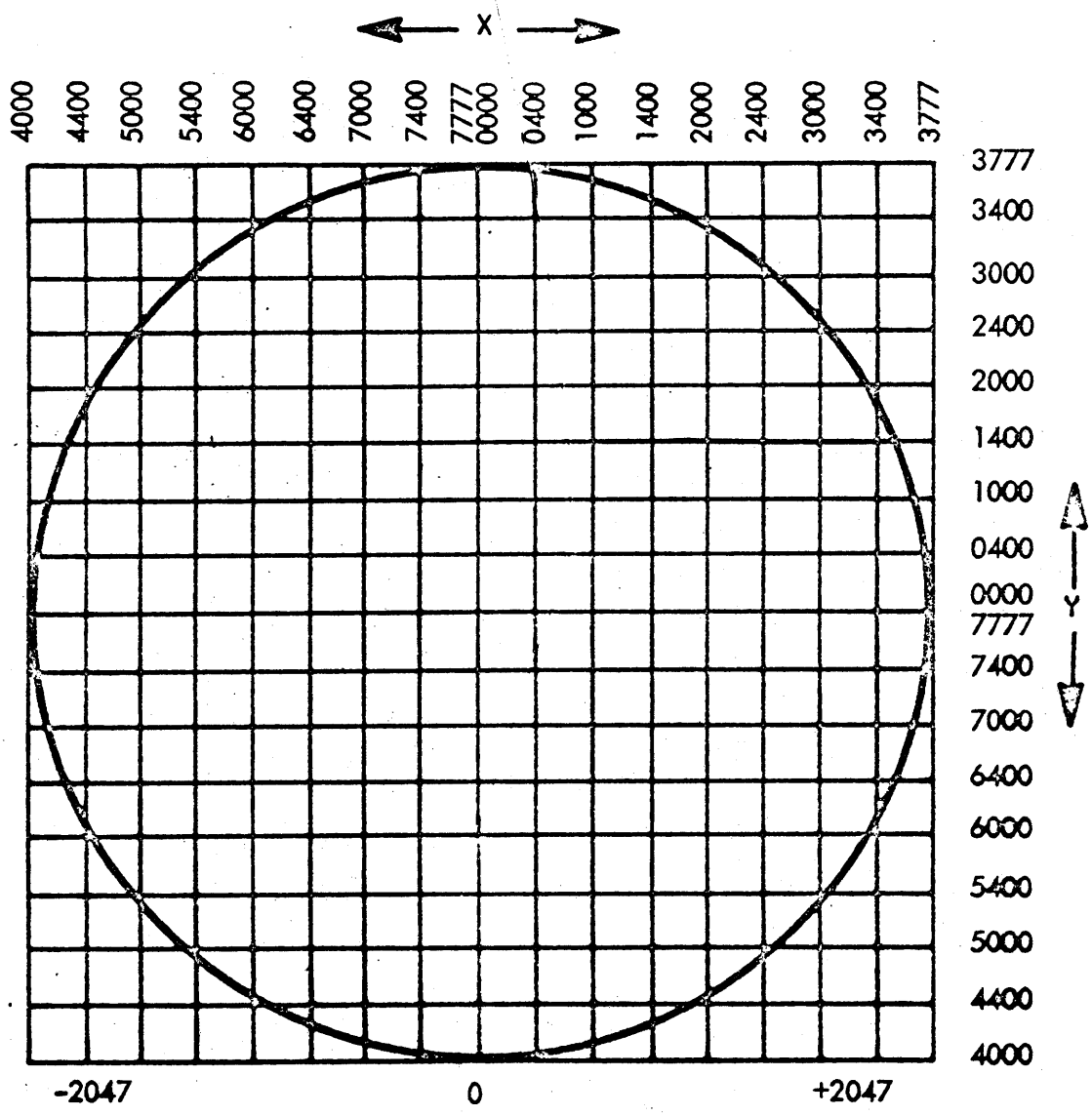


Figure 1. DISPLAY GRID SYSTEM

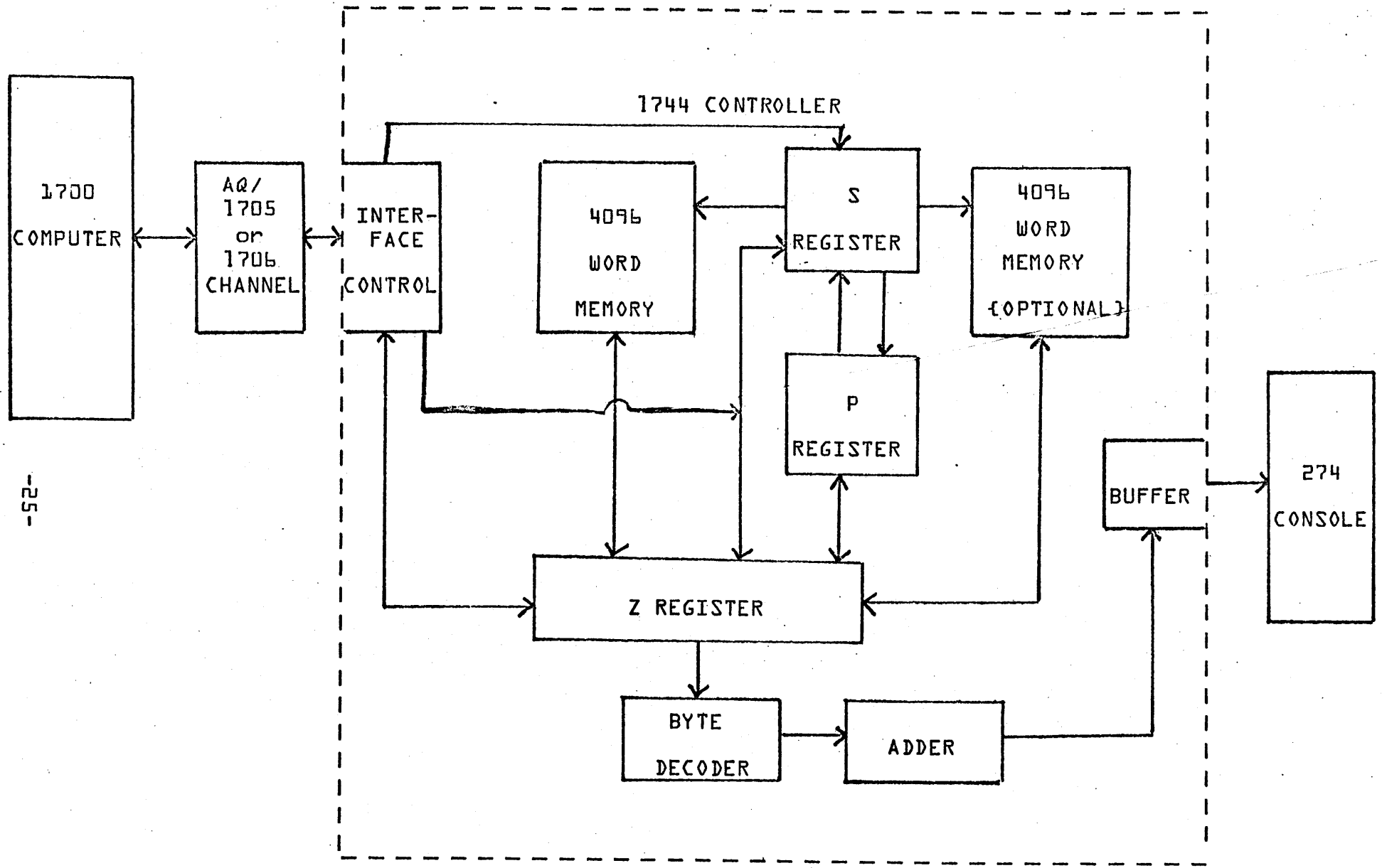
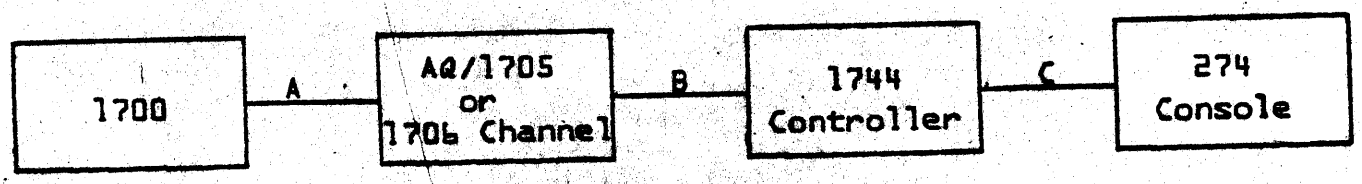


Figure 2 . 1700/1744/274 GRAPHIC SYSTEM BLOCK DIAGRAM

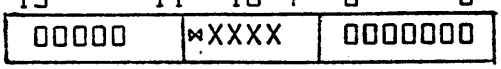
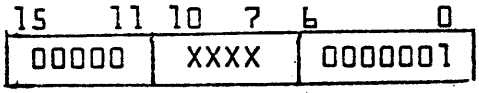
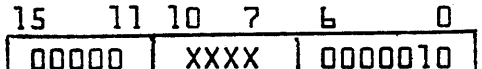
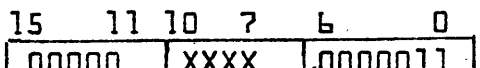
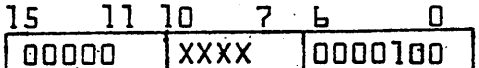
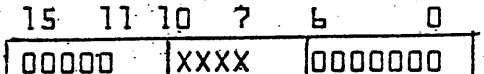
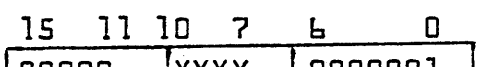
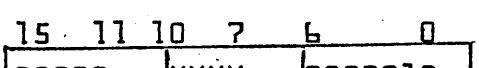
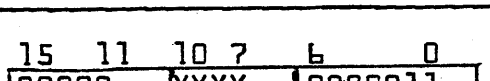
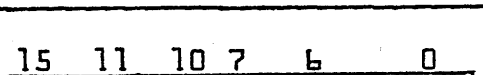
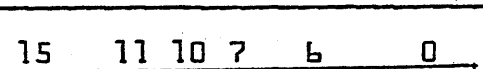
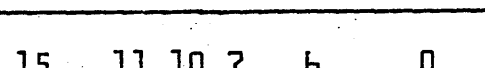


	CABLE A LENGTH	CABLE B LENGTH	CABLE C LENGTH
Nominal Standard	10 Ft.	50 Ft.	200 Ft.
Standard Option	10 Ft.	200 Ft.	1000 Ft.

When the standard option length cable is used, the use of on-line computer display is not possible.

Figure 3. 1700/1744/274 CABLE LENGTH

TABLE 1. 1744 COMMAND STRUCTURE

1700 Command	Contents of Q-Register	Data Format in A-Register or Core Memory	Meaning to 1744
OUT		Function Code	Perform the function as indicated by the code
OUT		Bits 00 thru 15	Store 16 data bits in buffer memory
OUT		Bits 00 thru 12 used as address bits	Write 13 bits in "S" register (I/O starting location)
OUT		Bits 00 thru 11 on-line control bytes	1700 display, return to off-line display after current on-line display
OUT		Bits 00 thru 11	Connect interface data to do a 1700 display only
INP		Bits 00 thru 15	Read Status
INP		Bits 00 thru 15	Read 16 data bits from buffer memory
INP		Bits 00 thru 12	Read "S" Register
INP		Bits 00 thru 12	Read "P" Register
INP		Bits 00 thru 11	Read "X" Register
INP		Bits 00 thru 11	Read "Y" Register
INP		Bits 00 thru 15	Search for identity bytes

*XXXX = Peripheral equipment device code

TABLE 2. STATUS WORD CODE INTERPRETATION

Bit	STATUS ASSIGNMENT
00	Status of 274 console. If reset, power is on and lightpen strike, lightpen switch, priority, and keyboard interrupts are allowed. If set, high or low voltage power off.
01	Delay interrupt
02	Lightpen strike interrupt
03	Priority interrupt (end of display byte)
04	Enable lightpen switch interrupt
05	Enable delay interrupt
06	Enable lightpen strike interrupt
07	0 = continue display after lightpen strike 1 = terminate display after lightpen strike
08	Reserved for keyboard options
09	
10	
11	Lightpen switch status
12	Reserved for keyboard options
13	
14	Enable priority interrupt (end of display byte)
15	Lightpen switch interrupt

NOTE: The delay interrupt is an 8 millisecond interrupt which can be used for tracking.

TABLE 3. FUNCTION CODE INTERPRETATION

Bit	Function to be Performed When Bit is Set
00	Clear lightpen switch interrupt
01	Clear delay interrupt
02	Clear lightpen strike interrupt
03	Clear priority interrupt (end of display byte)
04	Enable lightpen switch interrupt
05	Enable delay interrupt
06	Enable lightpen strike interrupt
07	Continue display when = 0
	Stop display when bits 06 and 07 set and lightpen strike occurs
08	Disable lightpen switch interrupt
09	Disable delay interrupt
10	Disable lightpen strike interrupt
11	Not used
12	Start display
13	Clear controller
14	Enable priority interrupt (end of display byte)
15	Disable priority interrupt

NOTE: The 1700 MASTER CLEAR switch will clear the controller interrupts and interrupt enable flip-flops.

APPENDIX A

1.0 OPTIONAL EQUIPMENT

The 274 may have any combination of three types of optional keyboards attached.

1. 16-key function keyboard
2. full alphanumeric keyboard
3. numeric keyboard

All the keyboards are in low-silhouette boxes that may be moved about on the console table top. The boxes are easily connected to the console and interconnected with each other.

1.1 Function Keyboard

The 16-key function keyboard (Figure A-1) provides a conventional task initiation and mode selection input. Fourteen buttons contain a snap action, latching type switch that sets its status on on initial press, and off on the second press. Two of the 16 buttons are equipped with momentary, snap action contacts that give an on status with the button down, and off status with the button up. An integral status light in each button indicates to the operator which buttons are on. Removable plastic overlay cards may be placed over the keys to label their function.

Each change in status of any function keyboard key may produce a keyboard interrupt at the 1744 controller. The software may then interrogate for keyboard status, and receive the on/off

status of all 16 buttons as bits in the status word.

1.2 Alphanumeric Keyboard

The alphanumeric keyboard (Figure A-2) provides typewriter-like symbolic input to the system. The keyboard layout is similar to a conventional teletypewriter. Each key has a switch to simulate the feel of an electric typewriter, and produces an interrupt and an 8-bit ASCII character code at the 1744 controller. The software may obtain the character code in the keyboard status word.

1.3 Numeric Keyboard

The numeric keyboard is similar to the alphanumeric keyboard except that it has fewer keys.

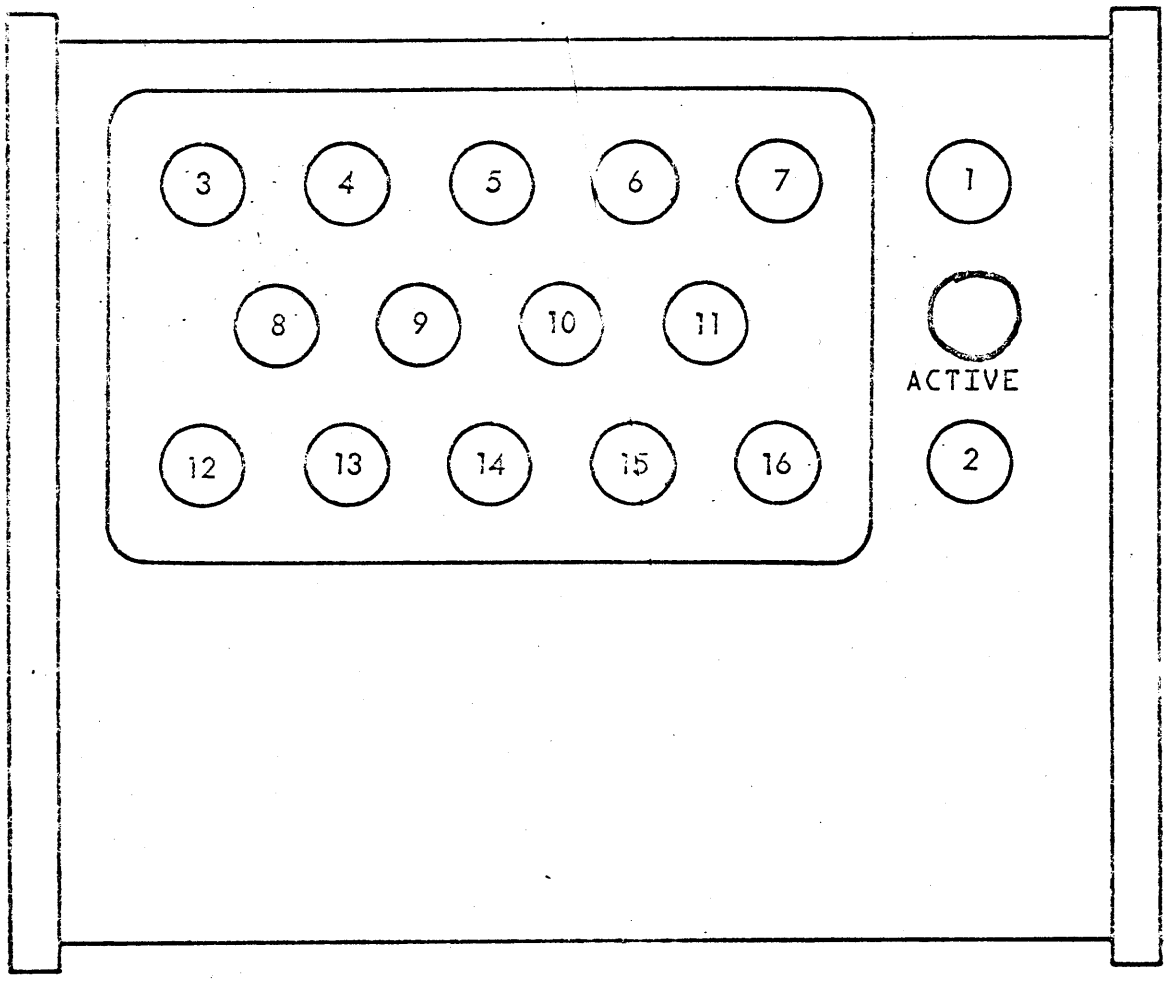


Figure A-1. Function Keyboard Layout

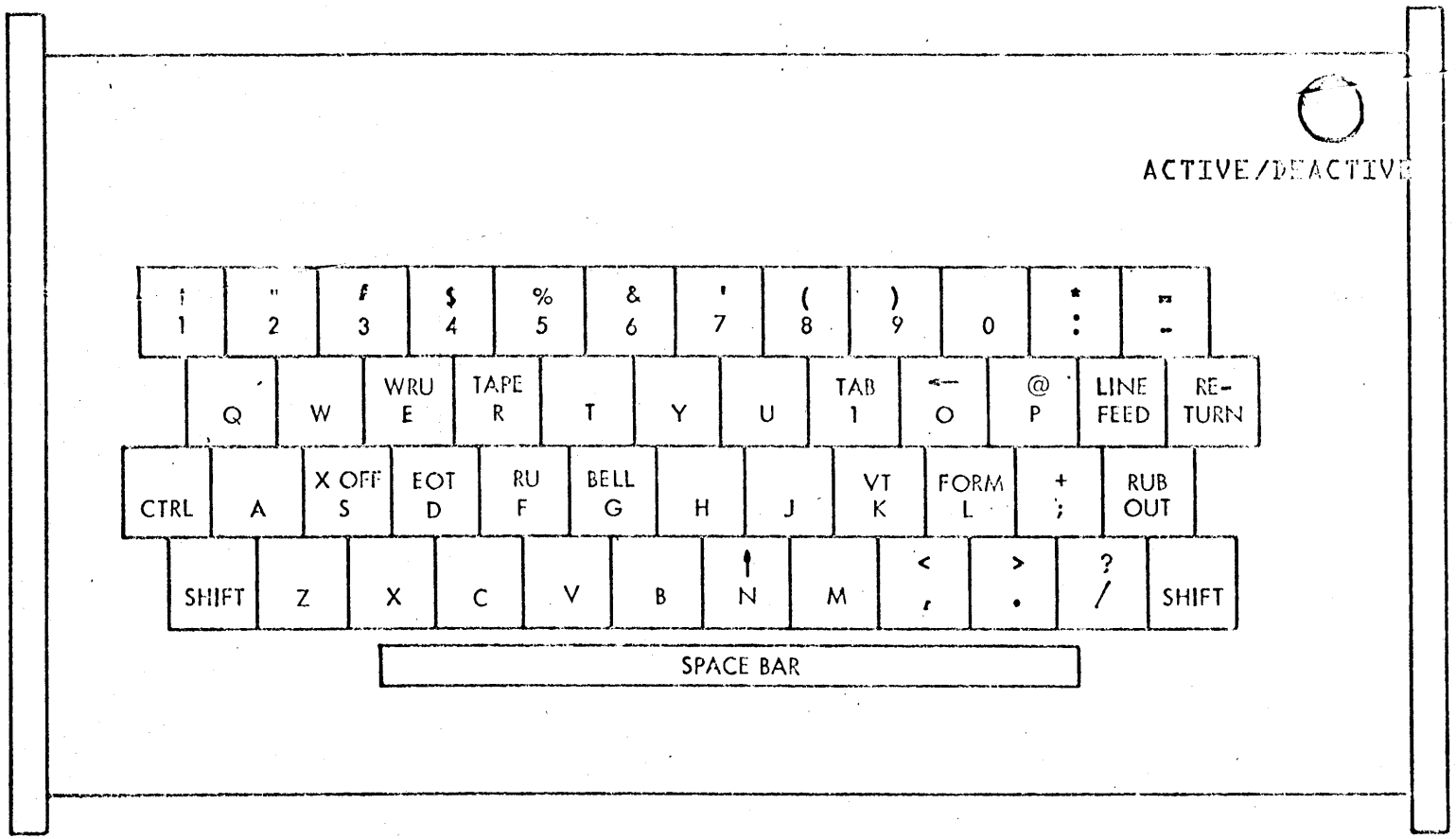


Figure A-2. Alphanumeric Keyboard Layout

APPENDIX B

1.0 1700 INPUT/OUTPUT

The 1700 Computer provides two ways to attach peripheral equipment: The AQ channel and the buffered data channel. characteristics of the peripheral equipment and its use in system determines the data path used. A 1705 interrupt data channel is required to implement the AQ channel and also provide an additional 14 interrupts to the computer. The 1706 buffered data channel is a converter and connects to the 1705 to provide direct access to storage for buffered operations or single-word transfers through the AQ channel. A maximum of three 1706 buffered data channels can be on a 1700.

Various 1700 peripheral equipments such as the 1721/1722 Paper Tape Reader, 1723/1724 Paper Tape Punch, and the 1711/1712/1713 teletypewriter are attached internally to the A and Q registers with a common synchronizer. Therefore, it is possible to have a 1700 with these peripherals, which appear to the programmer as if they operated on the AQ channel. Any additional peripherals require the addition of the 1705 interrupt data channel.