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i thru iii	A
iv Blank	A
1-1 thru 1-18	A
2-1 thru 2-20	A
3-1 thru 3-321	A
3-322 Blank	A
A-1 thru A-10	A
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PAGE	REV
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ru iii	A
lank	A
thru 1-18	A
thru 2-20	A
thru 3-321	A
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thru A-10	A
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SCOPE

This Peripheral Equipment Reference Manual has been prepared to aid trained maintenance personnel in the service and repair of the LaserDrive 1200 Intelligent Digital Optical Disk with Small Computer System Interface (SCSI), also referred to as the LD 1200. Comments, suggestions for improvement, and corrections to this manual are solicited. Forms are provided for those purposes at the end of this document.

ORGANIZATION OF INFORMATION

Section 1 - General Description
Section 2 - Operation
Section 3 - Theory of Operation

RELATED PUBLICATIONS

The following documents may be used to supplement the LD 1200 Peripheral Equipment Reference Manual:

PUBLICATION	PUBLICATION NUMBER
LD 1200 Hardware Maintenance Manual, Volume 1	75114907
LD 1200 Hardware Maintenance Manual, Volume 2	75114908
LD 1200 Customer User Manual	75114905
LD 1200 Site Preparation Manual	75114903
Small Computer System Interface (SCSI) Specification	ANSC X3T9.2
System Interface Assembly (SIA) Specification	75110948

Contents

1. GENERAL DESCRIPTION 1-1

1.1. INTRODUCTION 1-1

1.2. PHYSICAL DESCRIPTION 1-1

1.3. LD 1200 UNIT 1-3

1.4. CARD RACK 1-6

1.5. LD 1200 PCA DESCRIPTIONS 1-8

1.6. POWER SUPPLY 1-12

1.7. BASEPLATE 1-12

1.8. LD 1200 FRONT PANEL 1-18

1.9. LD 1200 REAR PANEL 1-18

2. OPERATION 2-1

2.1. INTRODUCTION 2-1

2.2. CONTROLS AND INDICATORS 2-1
2.2.1. Operator Panel 2-1
2.2.2. Maintenance Panel 2-4
2.2.3. Power Supply 2-8

2.3. POWER ON/OFF PROCEDURES 2-8
2.3.1. Power-On Procedure 2-8
2.3.2. Power-Off Procedure 2-8

2.4. DATA CARTRIDGE LOADING/UNLOADING PROCEDURES 2-8

2.5. OPERATOR PANEL OPERATING PROCEDURES 2-10
2.5.1. Data Write Protection 2-10
2.5.2. Disk Spin-Up/Down 2-11
2.5.3. Running Operator Diagnostic Tests 2-11

2.6. MAINTENANCE PANEL OPERATING PROCEDURES 2-12
2.6.1. Diagnostic Test Operating Procedure (Performed Only by the Customer Engineer) 2-13
2.6.2. Firmware Overview 2-15
2.6.2.1. Normal Mode 2-15
2.6.2.2. CE Mode 2-16
2.6.2.3. Stopped Mode 2-16
2.6.3. Selecting a Test 2-16
2.6.4. Selecting an Option 2-16
2.6.5. Starting a Test or Option 2-17
2.6.6. Entering Parameters 2-17
2.6.7. Stopping/Resuming a Test 2-18
2.6.8. Displaying a Subfailure Code 2-18
2.6.9. Displaying/Modifying Memory 2-18

3. THEORY OF OPERATION 3-1

3.1. INTRODUCTION 3-1

3.2. LD 1200 GENERAL BLOCK DIAGRAM 3-1
3.2.1. Interfaces 3-4
3.2.2. LD 1200 SCSI Adapter PCA 3-4
3.2.3. Error Correction Code and Common Memory Interface Unit PCA 3-4
3.2.4. Servo/Drive Control PCA 3-4
3.2.5. Servo Systems PCA 3-5
3.2.6. Error Signal Generator PCA 3-5
3.2.7. Read/Write Control PCA 3-5
3.2.8. Modulator Demodulator Synchronizer PCA 3-6
3.2.9. Carriage 3-6
3.2.10. Media 3-6
3.2.11. Baseplate 3-6
3.2.12. Power Supply 3-7
3.2.13. Operator Panel 3-7
3.2.14. Maintenance Panel (Optional) 3-7

3.3. LD 1200 FUNCTIONS 3-7
3.3.1. Drive Initialization and Focus 3-7
3.3.2. Seek 3-7
3.3.2.1. Seek Initialization 3-10
3.3.2.2. Seek 3-10
3.3.2.3. Jumpbacks 3-15
3.3.3. Read/Write 3-17
3.3.3.1. Initialization 3-20
3.3.3.2. Synchronization and Sector Identification 3-23
3.3.3.3. Read Data Operation 3-27
3.3.3.4. Write Data Operation 3-27
3.3.4. Error/Fault Handling 3-31
3.3.4.1. Direct Read During Write 3-35
3.3.4.2. Track Miscompare Error 3-35
3.3.4.3. Missing Data Field Error 3-35
3.3.4.4. Power Supply Overtemperature 3-35
3.3.4.5. Card Rack Overtemperature 3-35
3.3.4.6. Laser Read Power Error/Fault 3-36
3.3.4.7. Laser Write Power Error/Fault 3-36
3.3.4.8. Quad Sum High Fault 3-36

3.3.4.9. Verify Header Error/Fault 3-36
3.3.4.10. Motor Speed Fault 3-36
3.3.4.11. MPU Timeout Fault 3-37
3.3.4.12. MPU Self-Test Fault 3-37
3.3.4.13. Wobble Error/Fault 3-37
3.3.4.14. Phase-Locked Loop Error/Fault 3-37
3.3.4.15. Focus Error/Fault 3-37
3.3.4.16. Seek Error/Fault 3-38
3.3.4.17. Tracking Error/Fault 3-38
3.3.4.18. Line Sync Fault 3-38
3.3.4.19. Data Synchronization Error/Fault 3-38
3.3.4.20. Quad Sum Low Fault 3-39
3.3.4.21. Illegal Operation Code 3-39
3.3.4.22. Invalid Logical Unit number 3-39
3.3.4.23. Illegal Seek Address 3-39
3.3.4.24. Illegal Command Descriptor Block Parameter 3-39
3.3.4.25. End of Media Reached 3-39
3.3.4.26. Illegal Transfer Length 3-39
3.3.4.27. SCSI I/O Parity Error 3-39
3.3.4.28. Unable to Read Data Error 3-40
3.3.4.29. Logical Block Address Not Found 3-40
3.3.4.30. Unable to Write Data Error 3-40
3.3.4.31. Internal Parity Error 3-40
3.3.4.32. Servo/Drive Control Parity Error 3-40
3.3.4.33. Modulator/Demodulator Synchronizer Parity Error 3-40
3.3.4.34. Error Correction Code Circuitry Fault 3-41
3.3.4.35. Voltage Fault 3-41
3.3.4.36. Invalid Bootstrap Load Error 3-41
3.3.4.37. Laser Degraded 3-41
3.3.4.38. Power-Up Diagnostics Aborted 3-41
3.3.4.39. Diagnostic Fault Detected 3-41
3.3.4.40. Illegal Sequence (Device Not Ready) 3-42
3.3.4.41. Write Protected Device Error 3-42
3.3.4.42. Data Field Overwrite Error 3-42
3.3.4.43. Empty Sector Detected 3-42
3.3.4.44. Device Error 3-42

3.4. INTERFACES 3-43
3.4.1. Definitions 3-43
3.4.2. Small Computer System Interface (SCSI) 3-43
3.4.2.1. SCSI Hardware 3-43
3.4.2.2. SCSI Signal Definitions 3-44
3.4.2.3. SCSI Bus Phases 3-45
3.4.2.4. SCSI Bus Conditions 3-50
3.4.2.5. SCSI Bus Phase Sequences 3-52
3.4.2.6. SCSI Pointers 3-55
3.4.2.7. Message System Specification 3-55
3.4.2.8. SCSI Command Implementation 3-58
3.4.2.9. Command Descriptor Block 3-59
3.4.2.10. Command Examples 3-61
3.4.2.11. Group 0 Commands 3-62
3.4.2.12. Group 1 Commands 3-63
3.4.2.13. Completion Status Byte 3-64
3.4.2.14. Sense Description 3-65
3.4.3. Internal Device Interface/System Interface Assembly Bus 3-71

3.4.3.1. SIA Bus Line Descriptions 3-73
3.4.3.2. SIA Bus Timing 3-74
3.4.3.3. Bus Module Priority System 3-74
3.4.3.4. IDI Sequences 3-76
3.4.3.5. Track and Sector Identification Registers 3-84
3.4.3.6. Read/Write Command Registers 3-84
3.4.3.7. Drive Status and Control Registers 3-85

3.5. LD 1200 ADAPTER PCA 3-92
3.5.1. Interface Signals 3-95
3.5.2. I/O Ports 3-97
3.5.3. Microprocessor Control 3-99
3.5.3.1. MPU Memory Control System 3-101
3.5.3.2. MPU/SIA Address Buses 3-102
3.5.3.3. Address Decoder 3-102
3.5.3.4. MPU Timing Control 3-103
3.5.3.5. MPU Interrupt Register 3-103
3.5.4. SCSI Interface Control 3-104
3.5.4.1. SCSI Interface Circuit 3-106
3.5.4.2. SCSI/SIA Write and Read Registers 3-115
3.5.4.3. SCSI/Common Memory Direct Memory Access 3-115
3.5.4.4. SCSI/SIA Bus Arbitrator 3-116
3.5.4.5. Parity Checker/Generator 3-117
3.5.4.6. Command Register 1 (Port Write-97 hex) 3-117
3.5.4.7. Status Register 1 (Port Read-94 hex) 3-118
3.5.5. SIA Clock Generator 3-118
3.5.6. Operator and Maintenance Panel External Registers 3-119
3.5.6.1. Device Address Switch Register (Port Read-95 hex) 3-121
3.5.6.2. Operator Panel Hexadecimal Display Register (Port Write-94 hex) 3-121
3.5.6.3. Maintenance Panel LED Register (Port Write-95 hex) 3-122
3.5.6.4. Maintenance Panel Hexadecimal Display Register (Port Write-96 hex) 3-122
3.5.6.5. Maintenance Panel Keyboard Register (Port Read-97 hex) 3-123

3.6. ERROR CORRECTION AND COMMON MEMORY INTERFACE UNIT PCA 3-124
3.6.1. Signal Interface Descriptions 3-127
3.6.2. SIA/IDI Bus 3-128
3.6.2.1. SIA/IDI Address Bus 3-128
3.6.2.2. SIA/IDI Data Bus 3-128
3.6.2.3. SIA/IDI Bus Control Signals 3-128
3.6.2.4. SIA/IDI Bus Clock Signals 3-128
3.6.3. Common Memory Interface 3-129
3.6.3.1. Address Receivers 3-129
3.6.3.2. Data Bus Transceiver 3-130
3.6.3.3. Bank 1 Index Registers 3-130
3.6.3.4. Bank 2 Index Registers 3-130
3.6.3.5. Adders 3-130
3.6.3.6. Control and Timing Logic 3-130
3.6.3.7. Dynamic Memory Controller 3-130
3.6.3.8. Memory Address Driver 3-132
3.6.3.9. Memory Control Driver 3-132
3.6.3.10. Common Memory 3-132
3.6.3.11. Memory Data Buffer 3-133
3.6.3.12. Memory Driver 3-133

3.7.14. 8039 Output Latches 3-165
3.7.15. 8039 I/O Address Decode 3-168
3.7.16. Sector Interrupt 3-169
3.7.17. 8039 Watchdog Circuit 3-170
3.7.18. Track LSB Compare Logic 3-170
3.7.19. Decision Logic 3-170
3.7.19.1. Decision Logic Interface Signals 3-170
3.7.19.2. Input S-R Latches 3-176
3.7.19.3. Error Status Transfer Latch 3-176
3.7.19.4. Decision Logic Control Register 3-177
3.7.19.5. Field Programmable Logic Array (FPLA) 3-177
3.7.20. 8031 Input Buffers 3-177
3.7.21. 12-MHz Oscillator 3-180
3.7.22. 8031 Microprocessor and Program Memory 3-180
3.7.23. 8031 Output Latches 3-180
3.7.24. 8031 I/O Address Decode 3-183
3.7.25. 8031 Watchdog Circuit 3-184

3.8. SERVO SYSTEMS PCA 3-184
3.8.1. Signal Descriptions 3-184
3.8.2. Focus Servo Loop 3-189
3.8.2.1. Focus Servo Error Recovery 3-191
3.8.3. Fine Tracking Servo Loop 3-193
3.8.3.1. Tracking Servo Loop Error Recovery 3-196
3.8.4. Coarse Tracking Servo Loop 3-198
3.8.4.1. Coarse Tracking Loop Error Recovery 3-200

3.9. ERROR SIGNAL GENERATOR PCA 3-202
3.9.1. Interface Signal Descriptions 3-203
3.9.2. Focus and Tracking AGCs 3-206
3.9.2.1. Focus AGC 3-206
3.9.2.2. AGC Reference 3-206
3.9.2.3. Tracking AGC 3-206
3.9.2.4. High-Pass Filter 3-206
3.9.3. Tracking Wobble Circuitry 3-208
3.9.3.1. Wobble Sample and Hold 3-208
3.9.3.2. Low-Pass Filter 3-208
3.9.4. Summing Amplifier and Low Pass Filter 3-208
3.9.5. Track Crossing Circuitry 3-210
3.9.6. FSM Position Offset Circuitry 3-210
3.9.7. Overtemperature Circuitry 3-210
3.9.8. Diagnostics 3-211
3.9.8.1. D S-Curve In 3-211
3.9.8.2. D S-Curve Out 3-211
3.9.8.3. D P-P In 3-212
3.9.8.4. D P-P Out 3-212
3.9.8.5. D POS IN 3-212

3.10. READ/WRITE CONTROL PCA 3-213
3.10.1. Interface Signals 3-217
3.10.2. Initialization Circuit 3-223
3.10.3. Initialization Switch 3-223
3.10.4. Laser Power Check Circuit 3-223
3.10.5. Read Power Control Disable 3-224
3.10.6. Read Power Control Circuit 3-224

3.10.7. Read Power Switch 3-224
3.10.8. Read Power Current Source 3-225
3.10.9. Read Current Detection 3-225
3.10.10. Write Power Control Disable 3-225
3.10.11. Write Power Control Circuit 3-226
3.10.12. Write Power Switch 3-226
3.10.13. Write Power Current Source 3-226
3.10.14. Write Current Detection 3-226
3.10.15. Dying Status Circuit 3-227
3.10.16. Quad Sum Too High Detection 3-227
3.10.17. Logic 3-227
3.10.18. Write Pulse Delay Setting 3-227
3.10.19. Write Pulse Width Setting 3-228
3.10.20. DRDW Delay Setting 3-229
3.10.21. Automatic Gain Control 3-229
3.10.22. Phase-Locked Loop and VCO Frequency Delay Setting 3-230
3.10.23. Wobble Detection 3-232
3.10.24. Carriage Power Supply Interconnect 3-232

3.11. MODULATOR DEMODULATOR SYNCHRONIZER PCA 3-233
3.11.1. Interface Signals 3-236
3.11.2. TOON Counter 3-241
3.11.3. Nibble Counter and Sequence Logic 3-241
3.11.4. Timing Circuit 3-246
3.11.4.1. Sector Mark Detection Timing 3-246
3.11.4.2. Data Read Timing 3-247
3.11.4.3. Write Verify Timing 3-249
3.11.5. Sample and Hold 3-250
3.11.6. Comparators 3-250
3.11.7. Transition Detectors 3-253
3.11.8. Binary Registers 3-253
3.11.8.1. Sector Mark Search Mode 3-253
3.11.8.2. Data Read Mode 3-253
3.11.8.3. Write Verify Mode 3-254
3.11.9. Sector Mark Register and Decoder 3-254
3.11.10. Nibble-to-Byte Conversion 3-256
3.11.11. Interleave Table 3-258
3.11.12. Write Logic and TOON Encoder 3-264
3.11.13. Rewrite Logic 3-267
3.11.14. SIA Interface 3-267
3.11.15. Pre-PIP Detection 3-272
3.11.16. Certify Flag Detection 3-273
3.11.17. Data Detection Circuit 3-273
3.11.18. Write Verify Circuit 3-273
3.11.19. Wobble Byte Verification 3-276

3.12. CARRIAGE 3-278
3.12.1. Interface Signals 3-280
3.12.2. Optical System 3-282
3.12.3. Electronics System 3-284
3.12.3.1. ECL Differential Receiver 3-284
3.12.3.2. Laser Driver 3-284
3.12.3.3. Laser Diode 3-285
3.12.3.4. Sense Diode 3-285
3.12.3.5. Relay 3-285

3.12.3.6. Blanking Circuit 3-285
3.12.3.7. Quad Detector 3-286
3.12.3.8. Write Sense Sample and Hold 3-287
3.12.3.9. Position Sensor, Position Flag, and LED 3-287
3.12.3.10. Servo Preamplifier 3-287
3.12.3.11. Servo Signal Trim 3-287
3.12.3.12. Read Preamplifier 3-289
3.12.4. Electromechanical System 3-289

3.13. MEDIA 3-290
3.13.1. Surface Format 3-291
3.13.2. Data Recording Format 3-297

3.14. BASEPLATE 3-301
3.14.1. Signal Descriptions 3-301
3.14.2. Functional Description 3-303

3.15. POWER SUPPLY 3-304
3.15.1. Input Specifications 3-305
3.15.2. Output Specifications 3-305
3.15.3. Interface Signals 3-305
3.15.4. Block Diagram Description 3-311
3.15.4.1. AC Circuit Breaker 3-311
3.15.4.2. Line Filter 3-311
3.15.4.3. Bulk Power Supply 3-311
3.15.4.4. Self-Oscillating Forward Converter 3-312
3.15.4.5. Pulse Width Modulator, 50-kHz Oscillator, +5V Regulator 3-312
3.15.4.6. High-Frequency Step-Down Transformer 3-312
3.15.4.7. DC-to-DC Buck Converters 3-312
3.15.4.8. Filters 3-312
3.15.4.9. Linear Regulator 3-312
3.15.4.10. Margin Controls 3-313
3.15.4.11. Overvoltage Protection 3-313
3.15.4.12. Undervoltage Protection 3-313
3.15.4.13. Shutdown Circuit 3-313
3.15.4.14. Supply Operative Status 3-313
3.15.4.15. Autotransformer 3-313
3.15.4.16. Power Supply Fan 3-314
3.15.4.17. Motor Control 3-314
3.15.4.18. Line Sync 3-314
3.15.4.19. Brake Solenoid Control 3-314
3.15.4.20. Carriage Lock Solenoid Pick-Hold Circuit 3-314
3.15.4.21. Interlock Solenoid Pick-Hold Circuit 3-314
3.15.4.22. Power Supply Temperature Sensor 3-314

3.16. OPERATOR PANEL 3-315

3.17. MAINTENANCE PANEL 3-318

APPENDIX A. GLOSSARY A-1

Figures

Figure 1-1. LD 1200 and Data Cartridge 1-4
Figure 1-2. LD 1200 Major Assemblies 1-5
Figure 1-3. Card Cage, Front View 1-6
Figure 1-4. Card Rack, Rear View 1-7
Figure 1-5. LD 1200 SCSI Adapter PCA, Component Side 1-9
Figure 1-6. Modulator Demodulator Synchronizer PCA, Component Side 1-10
Figure 1-7. Read/Write Control PCA, Component Side 1-11
Figure 1-8. Power Supply Cable Connections 1-14
Figure 1-9. Baseplate, Top View 1-15
Figure 1-10. Baseplate, Bottom View 1-17
Figure 1-11. LD 1200 Rear Panel 1-18
Figure 2-1. LD 1200 Controls/Indicators and Cartridge Loading 2-2
Figure 2-2. Data Cartridge Write Protection 2-10
Figure 2-3. LD 1200 Maintenance Panel Access 2-14
Figure 2-4. LD 1200 Diagnostic Modes of Operation 2-15
Figure 2-5. Memory Access Maps 2-19
Figure 3-1. LD 1200 Block Diagram 3-2
Figure 3-2. Drive Control Microprocessor Ready/Idle State 3-8
Figure 3-3. Error Signal Generator Circuitry 3-11
Figure 3-4. Quad Detector Tracking Signal 3-12
Figure 3-5. Servo Microprocessor Seek Flow Chart 3-14
Figure 3-6. Jumpback Operation 3-16
Figure 3-7. Read and Write Protocol Paths 3-18
Figure 3-8. LD 1200/Internal Controller Read/Write Sequence 3-19
Figure 3-9. Read/Write Initialization Path 3-22
Figure 3-10. Read Data Path 3-24
Figure 3-11. Write Data Path 3-29
Figure 3-12. Termination for Single-Ended Devices 3-44
Figure 3-13. SCSI Interface Signals 3-45
Figure 3-14. Attention Condition Sequence 3-52
Figure 3-15. Phase Sequence with Arbitration 3-54
Figure 3-16. Simplified SCSI System 3-55
Figure 3-17. Single Command Example with Data Transfer to the Host 3-61
Figure 3-18. LD 1200 SIA/IDI Bus Configuration 3-72
Figure 3-19. SIA Bus Timing Diagram 3-75
Figure 3-20. LD 1200 SIA Bus Priority 3-76
Figure 3-21. LD 1200 SCSI Adapter PCA Block Diagram 3-94
Figure 3-22. Microprocessor Control 3-100
Figure 3-23. MPU Memory Map 3-101
Figure 3-24. SCSI Interface Control 3-105
Figure 3-25. SIA Clock Generator 3-119
Figure 3-26. Operator and Maintenance Panel External Registers 3-120
Figure 3-27. Error Correction and Common Memory Interface Unit PCA Block Diagram 3-125
Figure 3-28. Common Memory 3-131
Figure 3-29. Read or Write to Common Memory 3-133
Figure 3-30. Control and Status Ports 3-135
Figure 3-31. I/O Logic Decode 3-139
Figure 3-32. Servo/Drive Control PCA Block Diagram 3-142
Figure 3-33. IDI Bus Decode and Control Logic 3-148
Figure 3-34. 8039 Input Buffers 3-160
Figure 3-35. 8039 Output Buffers 3-166
Figure 3-36. Track LSB Compare Logic 3-171

Figure 3-37. Decision Logic 3-172
Figure 3-38. 8031 Input Buffers 3-178
Figure 3-39. 8031 Output Latches 3-182
Figure 3-40. Servo Systems PCA Block Diagram 3-188
Figure 3-41. Focus Loop Block Diagram 3-189
Figure 3-42. Focus "S" Curve 3-190
Figure 3-43. Focus Status Timing Diagram 3-191
Figure 3-44. Focus Error Recovery Functional Flow Chart 3-192
Figure 3-45. Focus Failure Timing Diagram 3-192
Figure 3-46. Initialization Failure During Focus 3-193
Figure 3-47. Tracking Block Diagram 3-194
Figure 3-48. Seek Arrival Mode Timing Diagram 3-195
Figure 3-49. Tracking Initialization Timing Diagram 3-196
Figure 3-50. Tracking Error Recovery Functional Flow Chart 3-197
Figure 3-51. Initialization Failure Timing Diagram 3-198
Figure 3-52. Tracking Failure Timing Diagram 3-198
Figure 3-53. Coarse Loop Block Diagram 3-199
Figure 3-54. Seek Profile 3-200
Figure 3-55. Coarse Loop Error Recovery Functional Flow Chart 3-201
Figure 3-56. Track Following or Seek Failure Timing Diagram 3-202
Figure 3-57. Error Signal Generator PCA Block Diagram 3-204
Figure 3-58. Focus Error and Tracking Signal Circuit 3-207
Figure 3-59. Wobble Circuitry 3-209
Figure 3-60. Track Crossing Circuitry 3-210
Figure 3-61. Diagnostic S Curve 3-211
Figure 3-62. Diagnostic Push-Pull Curve 3-212
Figure 3-63. Read/Write Control PCA Block Diagram 3-215
Figure 3-64. Write Pulse Width Setting Block Diagram 3-228
Figure 3-65. Automatic Gain Control Block Diagram 3-230
Figure 3-66. PLL and VCO Frequency Delay Setting Block Diagram 3-231
Figure 3-67. Wobble Bytes 3-233
Figure 3-68. Modulator Demodulator Synchronizer PCA Block Diagram 3-235
Figure 3-69. Simplified Nibble Counter and Sequence Logic 3-243
Figure 3-70. Sequence Signal Timing 3-244
Figure 3-71. Sample and Hold Timing Sequence Example 3-249
Figure 3-72. Data Path Simplified Logic 3-252
Figure 3-73. Sector Mark Decode Simplified Logic 3-255
Figure 3-74. TOON Decode Simplified Logic 3-257
Figure 3-75. Interleave Theory 3-261
Figure 3-76. Write Interleave Process Example 3-262
Figure 3-77. Read Interleave Process Example 3-263
Figure 3-78. Simplified Write Logic and TOON Encoder 3-265
Figure 3-79. SIA Interface Simplified Logic 3-270
Figure 3-80. Write Verify Circuit Simplified Logic 3-275
Figure 3-81. Wobble Byte Verification Simplified Logic 3-277
Figure 3-82. Carriage Block Diagram 3-279
Figure 3-83. Carriage Optical System 3-283
Figure 3-84. Quad Detector Signals 3-288
Figure 3-85. Electromechanical System Model 3-289
Figure 3-86. LD 1200 Data Cartridge 3-291
Figure 3-87. Disk Construction 3-292
Figure 3-88. Recording Surface Format 3-293
Figure 3-89. Media Track Structure 3-295
Figure 3-90. Data Representation in the Media 3-296
Figure 3-91. LD 1200 Sector Format (One Sector) 3-298

Figure 3-92. Sector Mark Code Definition 3-299
Figure 3-93. Wobble Bytes 3-299
Figure 3-94. Baseplate Block Diagram 3-302
Figure 3-95. Power Supply Block Diagram 3-307
Figure 3-96. Operator Panel Block Diagram 3-317
Figure 3-97. Maintenance Panel Block Diagram 3-320

Tables

Table 1-1. LD 1200 Mechanical and Electrical Characteristics 1-2
Table 2-1. Operator Panel Controls and Indicators 2-3
Table 2-2. Maintenance Panel Controls and Indicators 2-5
Table 3-1. Reported LD 1200 Errors and Faults 3-34
Table 3-2. Information Transfer Phases 3-48
Table 3-3. Operation Code 3-59
Table 3-4. Typical Group 0 Command Descriptor Block for Six-Byte Commands 3-59
Table 3-5. Typical Group 1 Command Descriptor Block for Ten-Byte Commands 3-60
Table 3-6. Status Byte 3-64
Table 3-7. Status Byte Code Bit Values 3-65
Table 3-8. Status Categories 3-78
Table 3-9. Error Action Overview 3-80
Table 3-10. Write Error Categories 3-81
Table 3-11. Control Bit Categories 3-82
Table 3-12. SCSI I/O Port Definitions 3-98
Table 3-13. Command Byte 3-136
Table 3-14. IDI Bus Address Decode 3-149
Table 3-15. 8039 Address Decode 3-169
Table 3-16. 8031 Address Decode 3-183
Table 3-17. Common Memory Data Buffer Format (One Sector) 3-258
Table 3-18. TOON Code Definition 3-301

1. GENERAL DESCRIPTION

1.1. INTRODUCTION

The purpose of this section is to familiarize the user or Customer Engineer (CE) with the SCSI LaserDrive 1200 Intelligent Digital Optical Disk (LD 1200) and its field replaceable units (FRUs). This section includes an illustrated physical description of the overall unit and its FRUs.

1.2. PHYSICAL DESCRIPTION

The LD 1200 is a random-access, optical disk drive with removable Media and a Small Computer System Interface (SCSI). It stores up to two gigabytes of data on a disk that can be written on once and read multiple times.

The write process consists of melting holes into the Media by means of a laser beam. The read process consists of sensing the change in light reflected from the Media by means of photodetectors. This information is sent to the logic. A hole reflects very little light and represents a binary ONE. The absence of a hole reflects most of the laser beam and represents a binary ZERO.

Table 1-1 provides a list of the mechanical and electrical characteristics of the LD 1200.

Table 1-1 LD 1200 Mechanical and Electrical Characteristics

Minimum Usable Data Cartridge Capacity	Single-sided Media: 1 gigabyte; Double-sided Media: 2 gigabytes.
Number of Disks	1
Disk Construction	Pregrooved, glass sandwich
Disk Diameter	12 in (306 mm)
Data Surfaces	Single-sided Media: 1; Double-sided Media: 2
Recording:	
Tracks per Disk	Single-sided Media: 32,000; Double-sided Media: 64,000.
Sector Size	1,025 user bytes
Sectors per Track	32
Interface	Small Computer System Interface
Maximum Host Transfer Rate	Write: 2 MB/s; Read: 1.33 MB/s
Average Data Transfer Rate	262 kB/s
Average Access Time	150 ms
Average Rotational Latency	62.5 ms
Spindle Speed	480 +4.8/-9.6 rpm
Spindle Power Up/Down Time	Up: 8 sec maximum Down: 3 sec maximum
Data Reliability Error Rate with (ECC)	10^{-12} during 10 years
Drive Reliability Mean Time Between Failures (MTBF)	12,000 hours
Media Life - Total Storage Time	10 years
Power Options	100V, 50/60 Hz 110V, 50/60 Hz 120V, 60 Hz 200V, 50 Hz 220V, 50 Hz 240V, 50 Hz
Power Dissipation	250W average (217 kcal/hr; 860 BTU/hr) 400W maximum (347 kcal/hr; 1376 BTU/hr)
Environmental:	
Operating Temperature	10 to 40°C (50 to 104°F)
Nonoperating Temperature	-40 to 60°C (-40 to 140°F)
Operating Humidity	20 to 80% relative humidity (no condensation allowed)
Nonoperating Humidity	10 to 90% relative humidity (no condensation allowed)
Operating Altitude	-983 to 8200 ft (-300 to 2500 m)
FCC Rating	Class B
Physical Characteristics: (Rack-Mountable Model)	
Height	5.25 in. (13.3 cm)
Width	19 in. (48.3 cm)
Depth	25.6 in. (65 cm)
Weight	55 lbs (25 kg)
Physical Characteristics: (Desk-Top Model):	
Height	5.25 in. (13.3 cm)
Width	18.5 in. (46.9 cm)
Depth	25.88 in. (65.7 cm)
Weight	55 lbs (25 kg)

The LD 1200 is either a rack-mountable or desk-top unit with an internal power supply, Spindle Motor, logic chassis (card rack), and an optical Read/Write head (Carriage).

Data is stored on a 12-inch diameter disk. The Media consists of a sandwich of two glass disks, coated internally with a metallic layer on which the data is written. This Media is contained in a plastic Data Cartridge (cassette type).

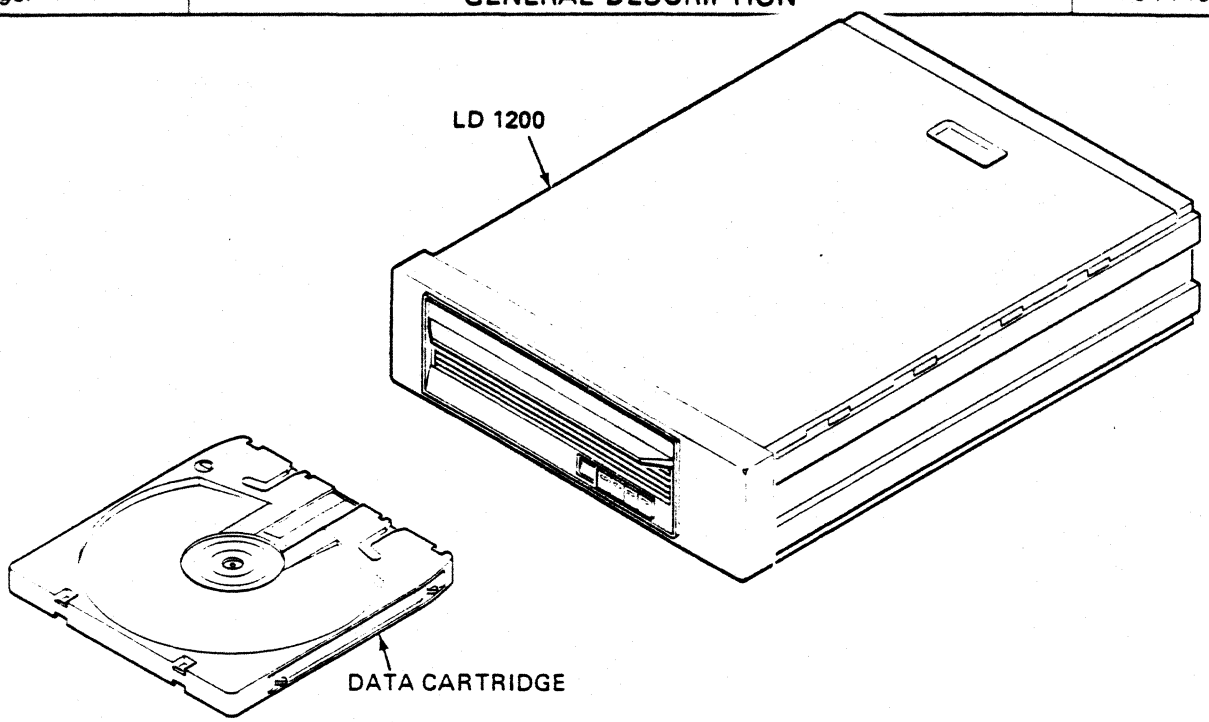
The Data Cartridge is provided with optical access doors that open when the cartridge is inserted into the unit, exposing the Media to the laser beam. Safety interlocks protect the user from exposure to the laser beam. The unit does not operate unless the Data Cartridge is properly inserted and seated, and the disk is spinning at the proper speed.

The Carriage Assembly, in the LD 1200, contains a laser pen. This pen emits a light beam that is routed through an objective lens, mounted in the Fine Servo Motor, to the Media. The Fine Servo Motor focuses the laser beam on the Media and keeps it in the center of the data track. The Coarse Actuator moves the Carriage Assembly underneath the disk surface for Seek operations.

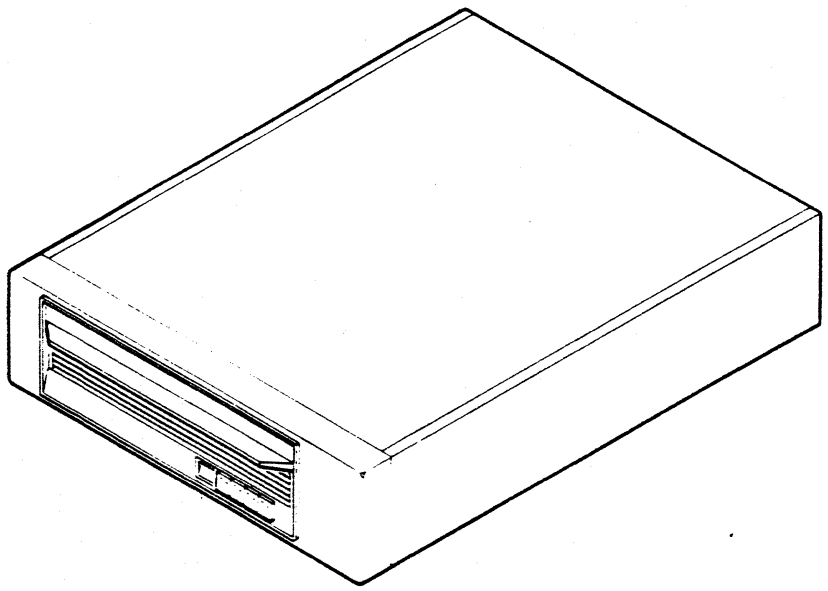
1.3. LD 1200 UNIT

Figure 1-1 illustrates the LD 1200 Unit and Data Cartridge. A general physical and functional description of the LD 1200 unit and Data Cartridge is given in the Physical Description subsection.

The major assemblies of the LD 1200 are shown in figure 1-2. These assemblies are described in the following subsections.



a. RACK-MOUNTABLE MODEL



b. DESK-TOP MODEL PB002253-1

Figure 1-1 LD 1200 and Data Cartridge

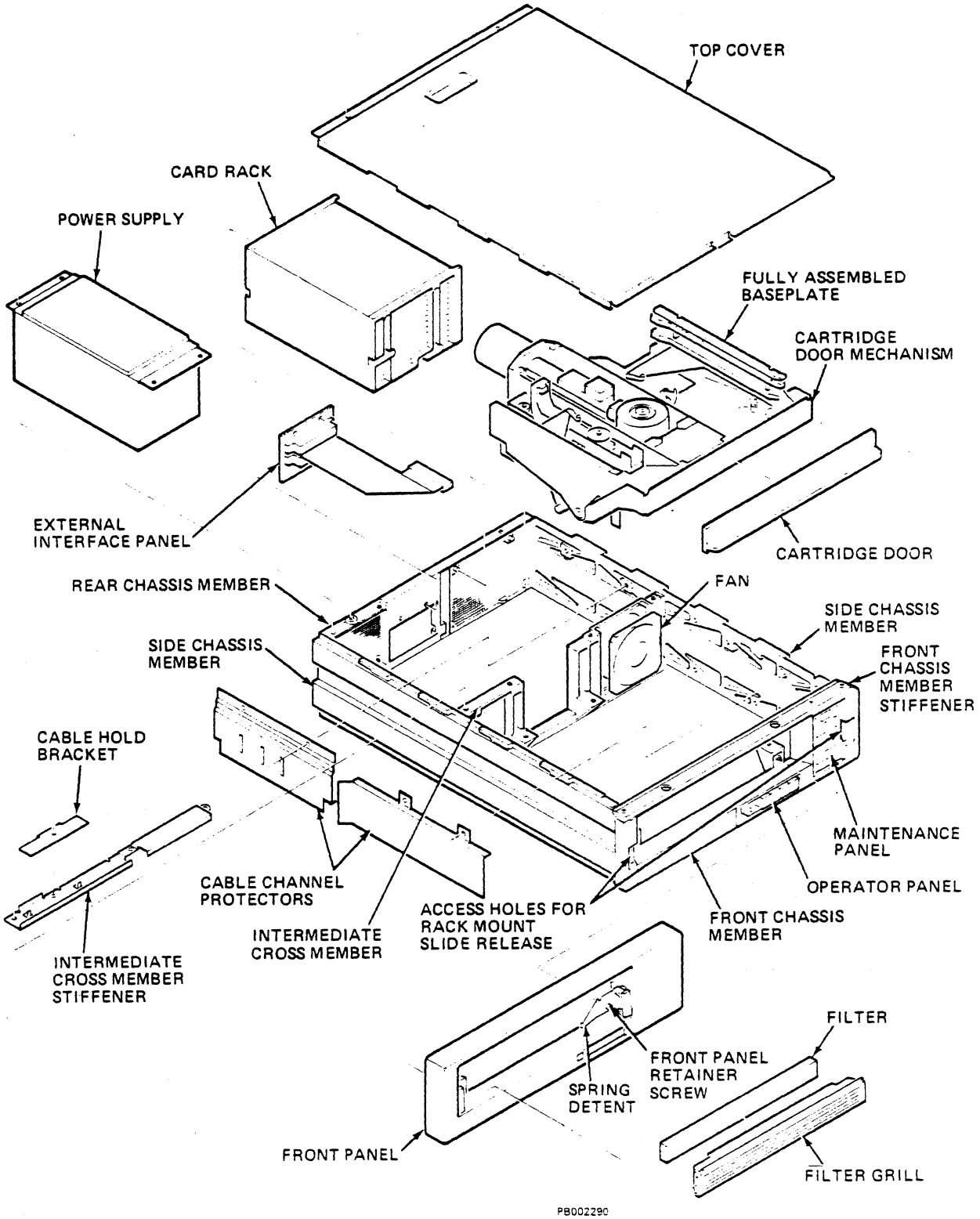


Figure 1-2. LD 1200 Major Assemblies

1.4. CARD RACK

The Card Rack is located in the right, rear corner of the LD 1200. It contains seven printed circuit assemblies (PCAs) and the logic interconnect board into which the PCAs are connected (the Backplane PCA). These seven PCAs are as follows:

- Error Correction and Common Memory Interface Unit (ECC) PCA
- LD 1200 SCSI Adapter (SCSI) PCA (also known as Internal Controller Interface PCA or ICI PCA)
- LD 1200 SCSI Adapter PCA (SCSI PCA), also known as the Internal Controller Interface PCA or ICI PCA.
- Modulator Demodulator Synchronizer (MDS) PCA
- Read/Write Control (R/WC) PCA
- Error Signal Generator (ESG) PCA
- Servo Systems (SS) PCA

The Card Rack and PCAs are shown in figure 1-3. The Backplane PCA is shown in figure 1-4.

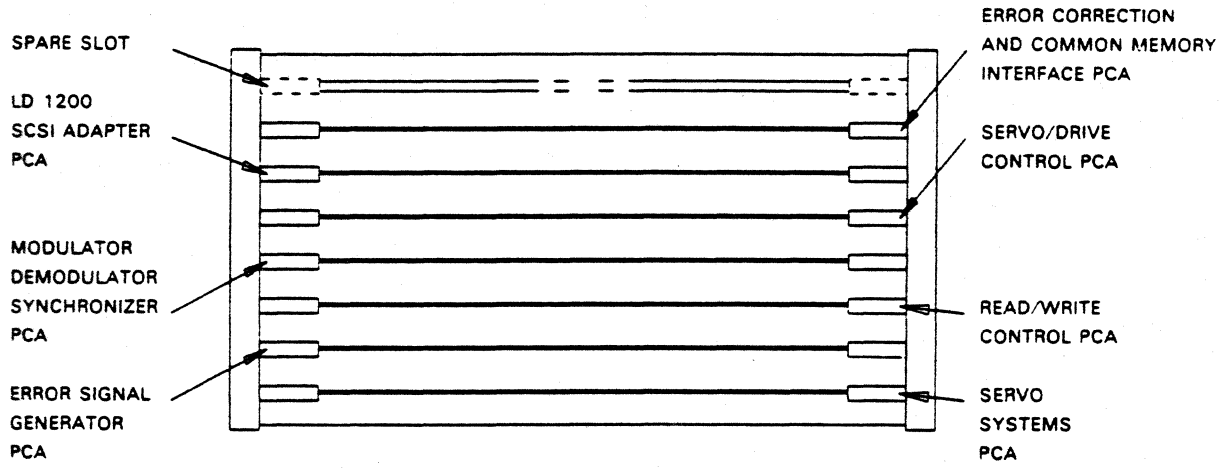


Figure 1-3. Card Cage, Front View

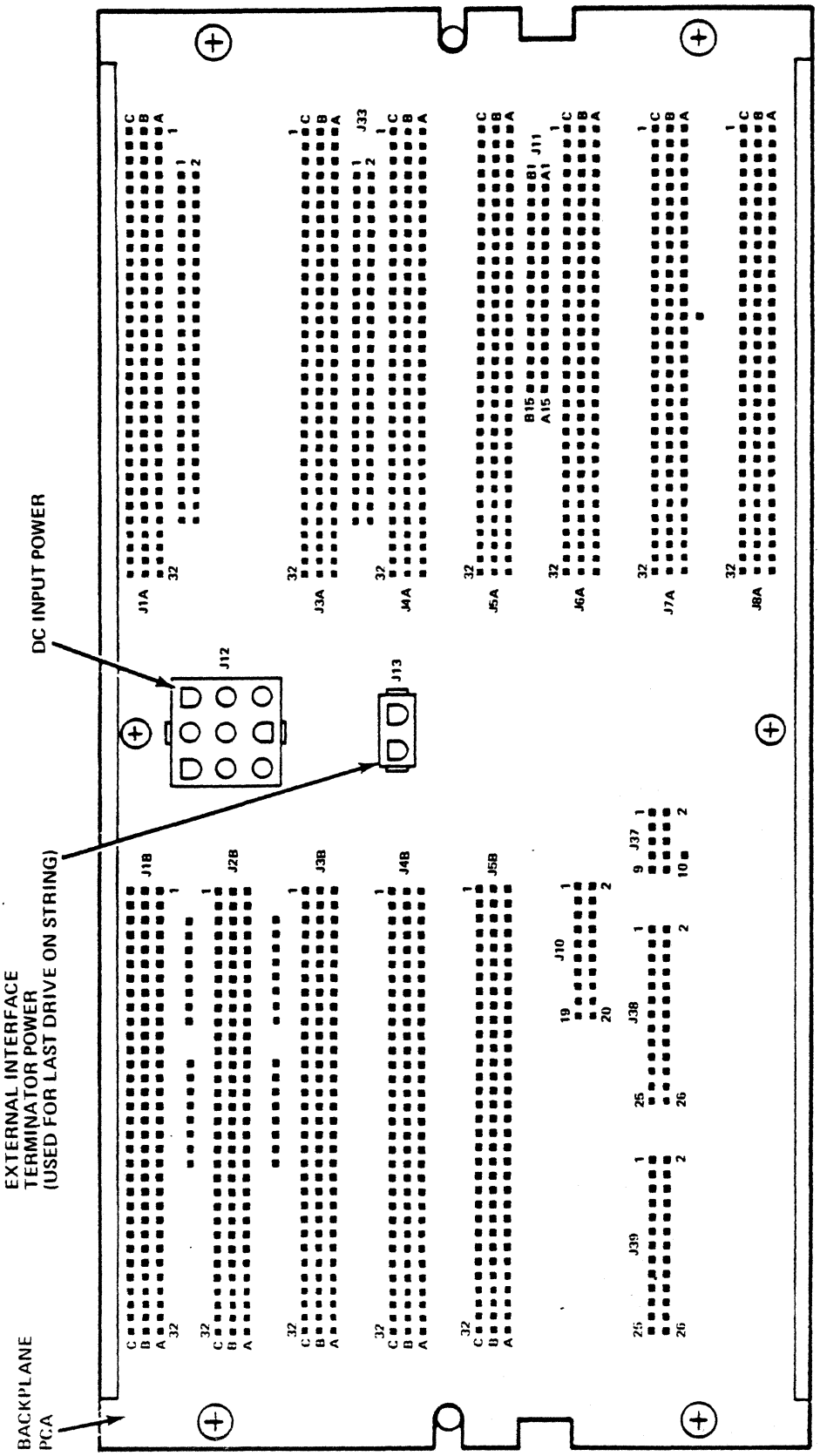


Figure 1-4 Card Rack, Rear View

1.5. LD 1200 PCA DESCRIPTIONS

The following is a brief description of the major LD 1200 PCAs and the Backplane PCA contained in the Card Rack:

- Error Correction and Common Memory Interface Unit PCA - This PCA generates error correction characters which are loaded into Common Memory with write data and performs error detection and correction on read data. It also provides Common Memory to buffer data and status transfers between the LD 1200 and the Host Adapter.

- LD 1200 SCSI Adapter PCA - This PCA contains the majority of the Internal Controller logic, enabling the LD 1200 to communicate with a Host over an SCSI interface. It interfaces with the Host Adapter, ECC, MDS, and Servo/Drive Control PCAs, the Operator Panel, and (when installed) the Optional Maintenance Panel. This PCA also provides for termination of the external (SCSI) interface (refer to figure 1-5).

- Servo/Drive Control PCA - This PCA provides the logic for the servo and drive functions, controlling laser power and Carriage movement.

- Modulator Demodulator Synchronizer PCA - This PCA performs the basic data manipulation functions of the LD 1200.

  The following jumpers are located on this PCA (refer to figure 1-6 for jumpers locations).

  - (H147,G643) Wobble Formatting Jumper - Allows the selection of different wobble formats when using a Media also provided with this option.

  - (F553) Continuous Rewrite Jumper - Used during testing only, this jumper allows the Rewrite function to continue beyond one sector.

- Read/Write Control PCA - This PCA controls Read and Write laser power, provides automatic gain control of read data, and provides timing signals for the Read/Write channel.

  The following jumpers are located on this PCA (refer to figure 1-7 for jumper locations).

  - (F003, F005) Laser Pen Selection Jumper - Provides compatability between the characteristics of different Laser Pens supplied by different manufacturers.

  - (H138) VCO Delay Setting Jumper - Provides selected time delay allowing adjustment of the phase of the internal clocks with relation to the disk clock.

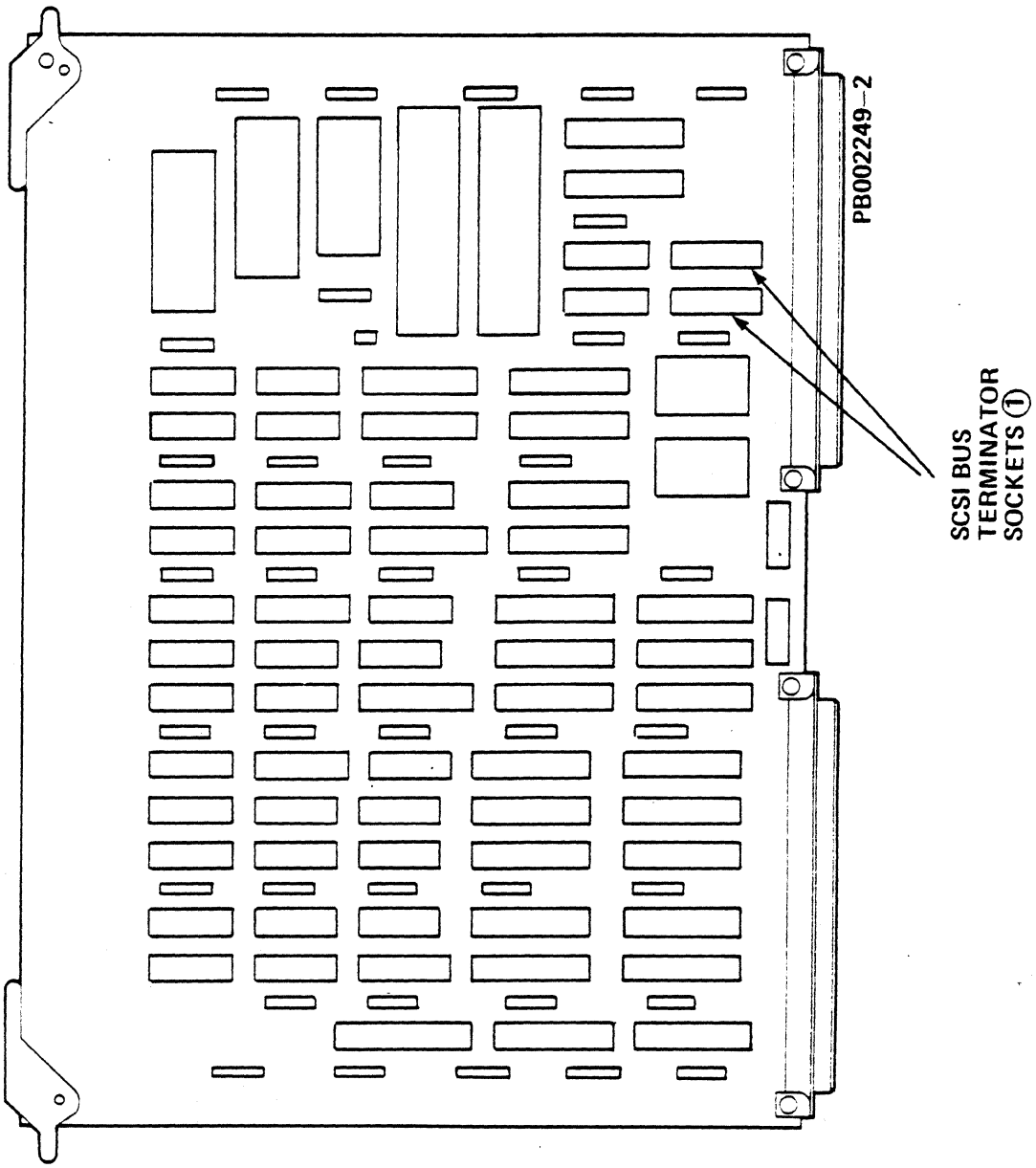
  - (D151) Write Pulse Delay Setting Jumper - Allows an adjustable time delay to be produced between the receipt of 2CLK and the output of write data to the Carriage.

  - (B332) DRDW Delay Setting Jumper - Allows an adjustable time delay to be produced between the output of the Modulator Demodulator Synchronizer PCA and the input to the Automatic Gain Control.

- Error Signal Generator PCA - This PCA generates and amplifies the servo error signals that are used by the Servo Systems PCA to control Carriage movement.

- Servo Systems PCA - This PCA controls the Carriage servo functions.

- Backplane PCA - This PCA interconnects the major LD 1200 PCAs.



NOTE:
① SCSI Terminator Assemblies must be installed in both sockets to terminate the SCSI Bus.

Figure 1-5. LD 1200 SCSI Adapter PCA, Component Side

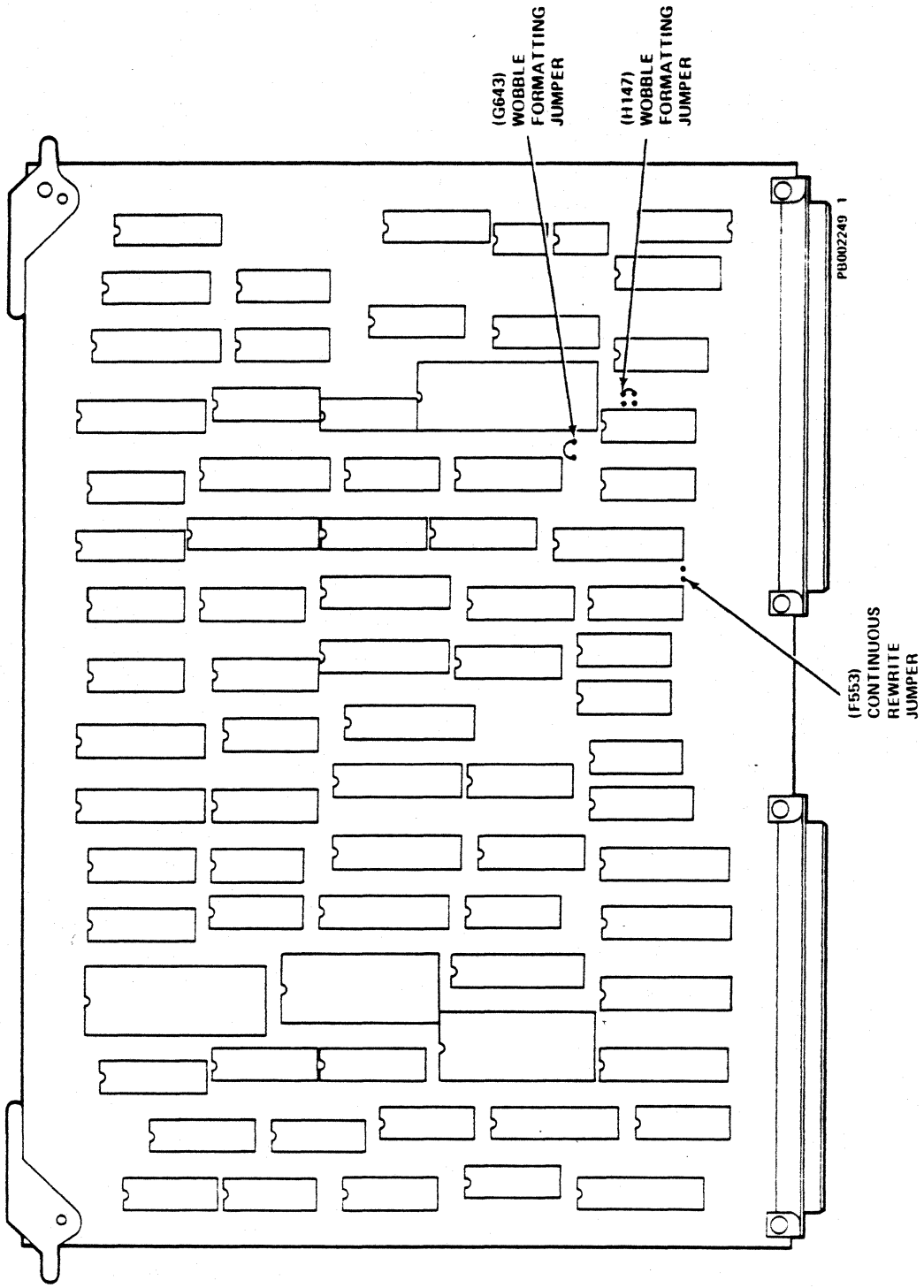
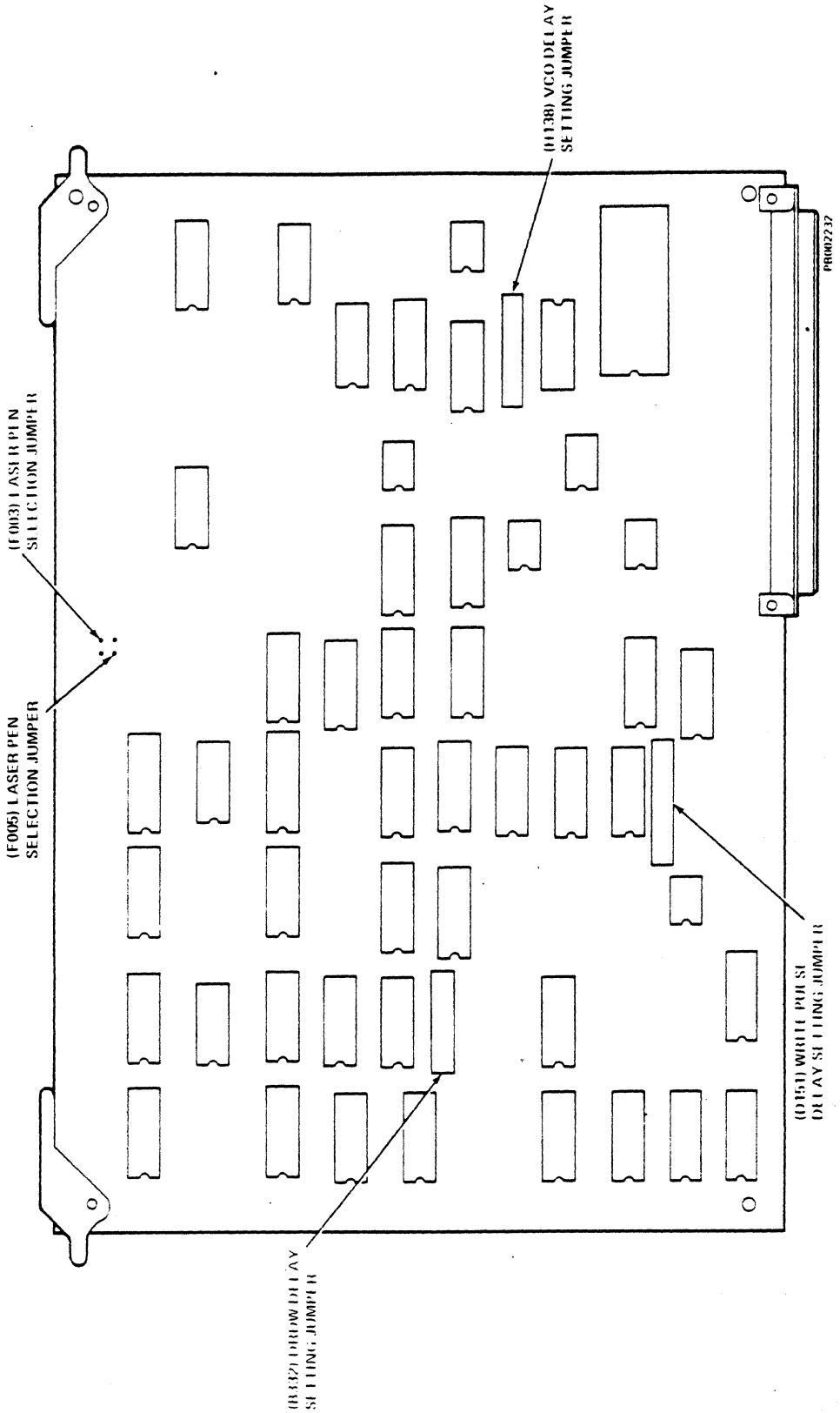


Figure 1-6. Modulator Demodulator Synchronizer PCA, Component Side



NOTE: Refer to R/W C PCA Theory for Description of Jumper Functions

Figure 1-7. Read/Write Control PCA, Component Side

1.6. POWER SUPPLY

The LD 1200 Power Supply is located in the left, rear corner of the unit. It is a switching type of supply, accepting ac input of 100 V, 50/60 Hz; 110 V, 50/60 Hz; 120 V, 60 Hz; 200 V, 50 Hz; 220 V, 50 Hz; or 240 V, 50 Hz. It supplies dc output voltages of +5, -5, +12, -12, and +40 Vdc, and an ac output voltage of 115 Vac.

The Power Supply is shown in figure 1-2. Power Supply cable connections are shown in figure 1-8.

1.7. BASEPLATE

The Baseplate provides the main supporting structure and mounts for the critical mechanical, electromechanical, and optomechanical assemblies in the LD 1200. It is designed as a stable and rigid reference to aid in ease of assembly and alignment of interrelated subassemblies.

The FRUs located on the top of the Baseplate are shown in figure 1-9. A brief description of these FRUs follows:

- Motor Cover - Covers the top of the Spindle Motor.
- Spindle Pulley Belt - Wraps around the Spindle Motor Pulley and the Spindle. When the motor is running, the belt rotates the Spindle.
- Spindle Motor - Rotates the Spindle by means of the Spindle Pulley Belt.
- Tachometer Sensor - Senses the speed of the Spindle Motor.
- Spindle Assembly - Provides the means for securing and rotating the Media.
- Motor/Brake Assembly - Used to brake the Spindle Assembly to a stop.
- Guardband Sensor - Indicates when the Carriage is retracted to the guardband area of the Media.
- Carriage - Provides the Read/Write/Servo head for the LD 1200. The Carriage moves between different areas of the Media when a Seek function is performed.
- Positioner Motor Magnet - Interacts with the Carriage to form a voice coil motor, which moves the Carriage during Seek operations.
- Write Protect Switch - When the Write Protect Tab on the Data Cartridge is set to the write protect position, this switch is activated, indicating to the logic that the write protect function has been activated.
- Baseplate Terminator PCA (known as Baseplate PCA) - Distributes logic signals from the Baseplate to the Card Rack. This PCA includes the Emergency Retract Capacitor, Write Protect Switch, and Data Cartridge Flag.

- Data Cartridge Flag - Indicates to the logic when the Data Cartridge is inserted.
- Cartridge Door - Opens to allow insertion of the Data Cartridge into the LD 1200. The guide rails in the door mechanism position the Data Cartridge over the Spindle Assembly and separate the cartridge halves, freeing the Media, when the door is closed.
- Cartridge Door Actuators - Open the optical access doors in the Data Cartridge when it is inserted into the LD 1200, allowing the laser beam direct access to the Media.
- Cartridge Eject Mechanism - Ejects the Data Cartridge approximately one inch when the Cartridge Door is opened.

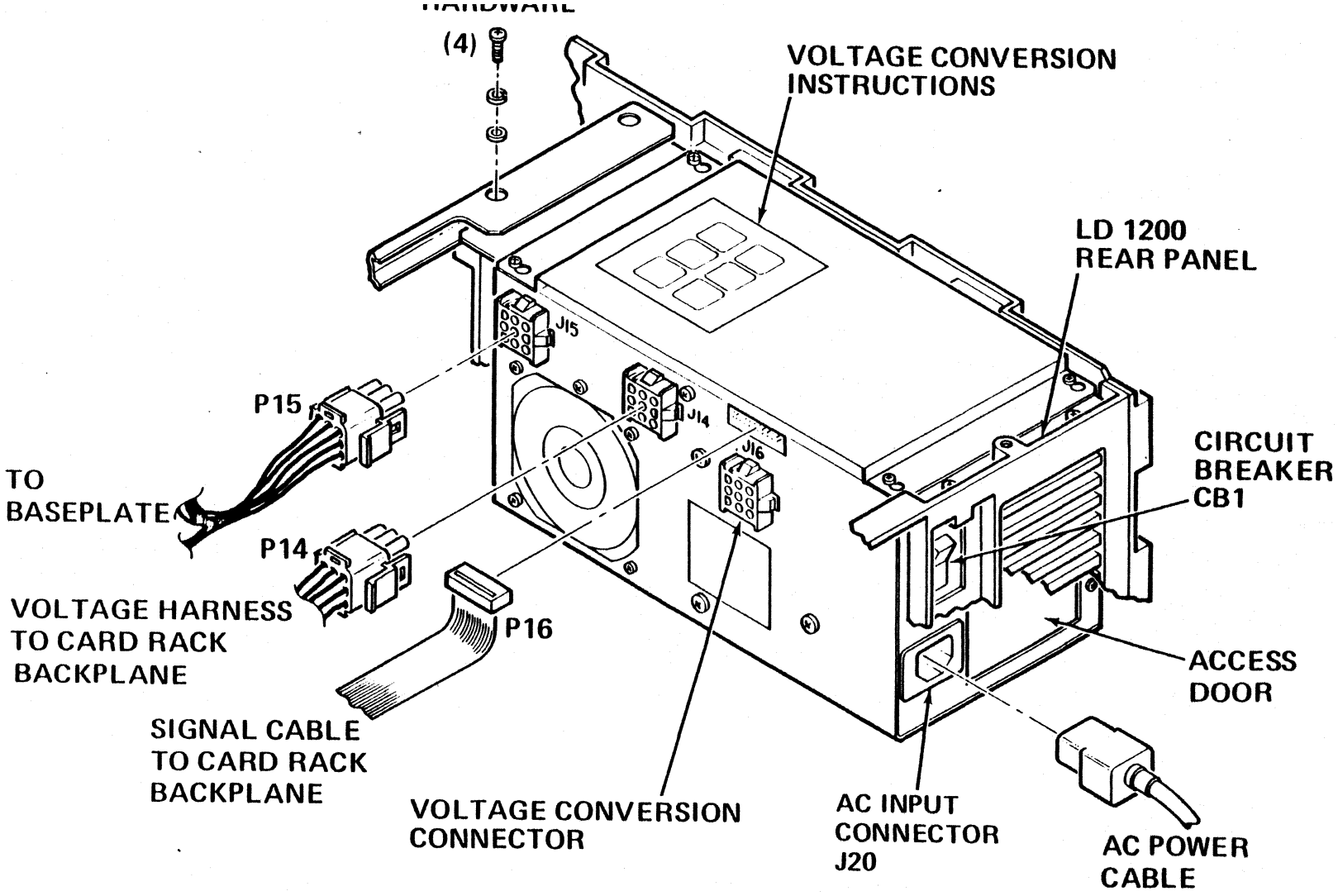


Figure 1-8. Power Supply Cable Connections

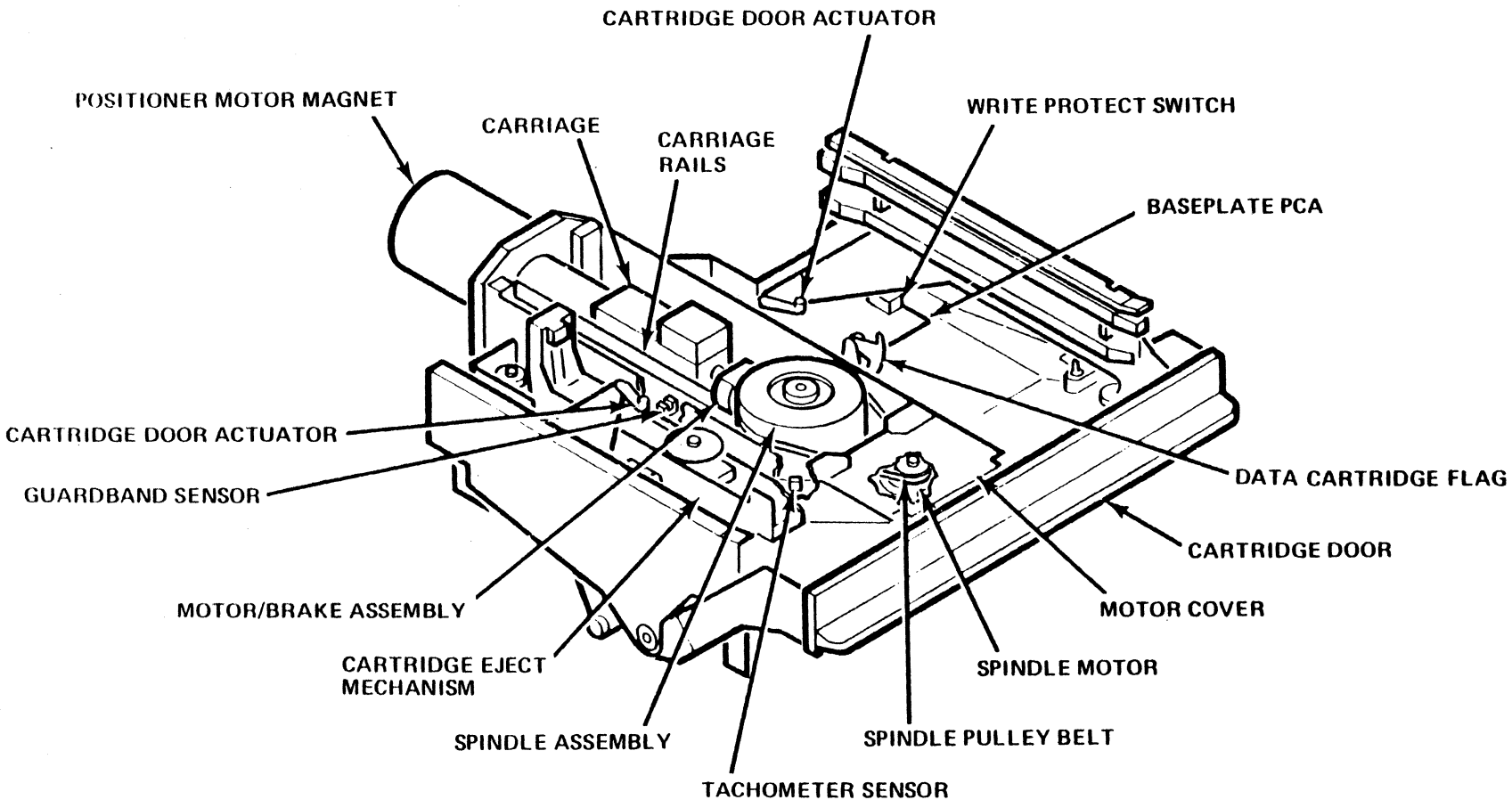


Figure 1-9 Baseplate, Top View

The FRUs located on the bottom of the Baseplate are shown in figure 1-10. A brief description of these items follows:

- Carriage Lock Solenoid - Locks the Carriage in the Home position after a power failure or normal shut down.
- Interlock Solenoid - Prevents removal of the Data Cartridge when the Spindle is spinning.
- Manual Door Release - Provides a manual means for opening the Cartridge Door in case of a power failure.
- Emergency Retract Capacitor - Fully retracts the Carriage when a power failure occurs.
- Motor Run Capacitor - Enables the Spindle Motor to spin up the Spindle smoothly.
- Electrical Contact Brush - Protects the Spindle from electrostatic buildup and discharge.
- Ball Bearing - The replaceable rotating contact point on the Spindle for the Contact Brush.
- Captivating Screws - Secure the Baseplate to the LD 1200 chassis.

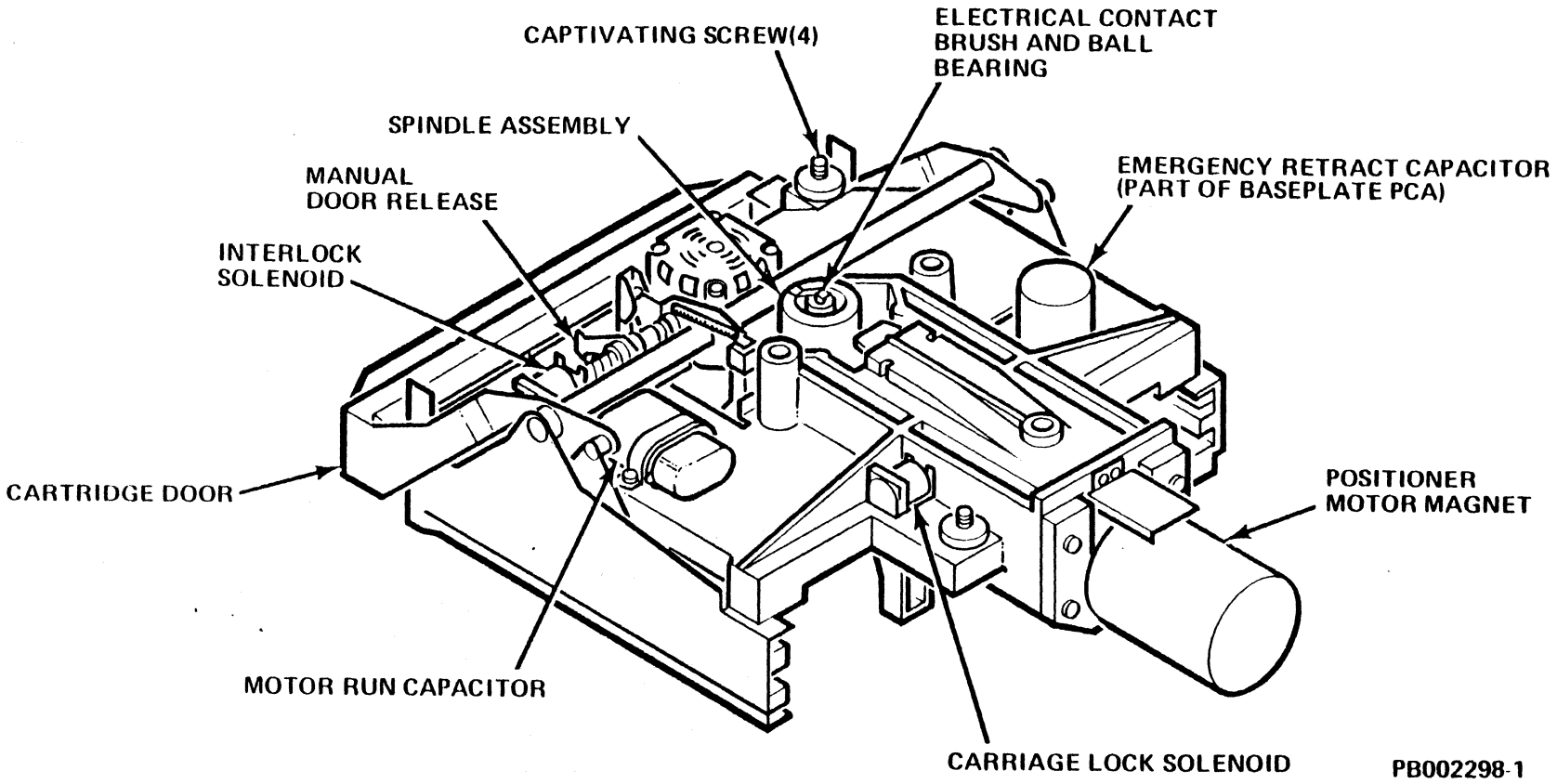


Figure 1-10. Baseplate, Bottom View

1.8. LD 1200 FRONT PANEL

The front panel of the LD 1200 includes the Operator Panel, opening for the Cartridge Door, Filter Grill, and Air Filter (refer to figure 1-2). The Operator Panel provides the user/machine interface necessary to operate the LD 1200. The Filter Grill contains the Air Filter which provides primary air filtration for the LD 1200.

Behind the front panel is located the optional Maintenance Panel (refer to figure 1-2). The Maintenance Panel enables the Customer Engineer (CE) to run diagnostic tests to troubleshoot the LD 1200.

1.9. LD 1200 REAR PANEL

The LD 1200 rear panel includes the Air Filter Grill, the Ground Strap (E2), external interface Connectors (J17 and J18), Circuit Breaker (CB1), AC Power Connector (J20), and Terminator Power Connector (J19). The rear panel is shown in figure 1-11.

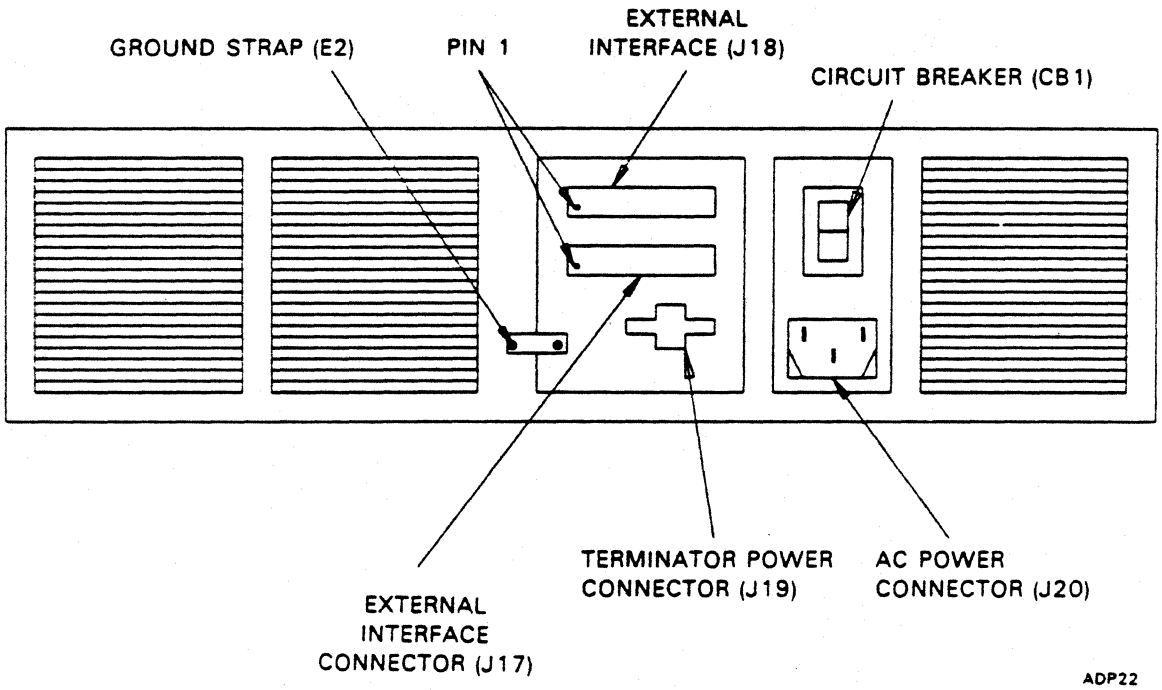


Figure 1-11. LD 1200 Rear Panel

2. OPERATION

2.1. INTRODUCTION

This section describes the controls and indicators for the Operator Panel, the Maintenance Panel, and the Power Supply. It also includes the procedures for SCSI LaserDrive 1200 Intelligent Digital Optical Disk (LD 1200) Power-On and Power-Off, and Data Cartridge loading and unloading.

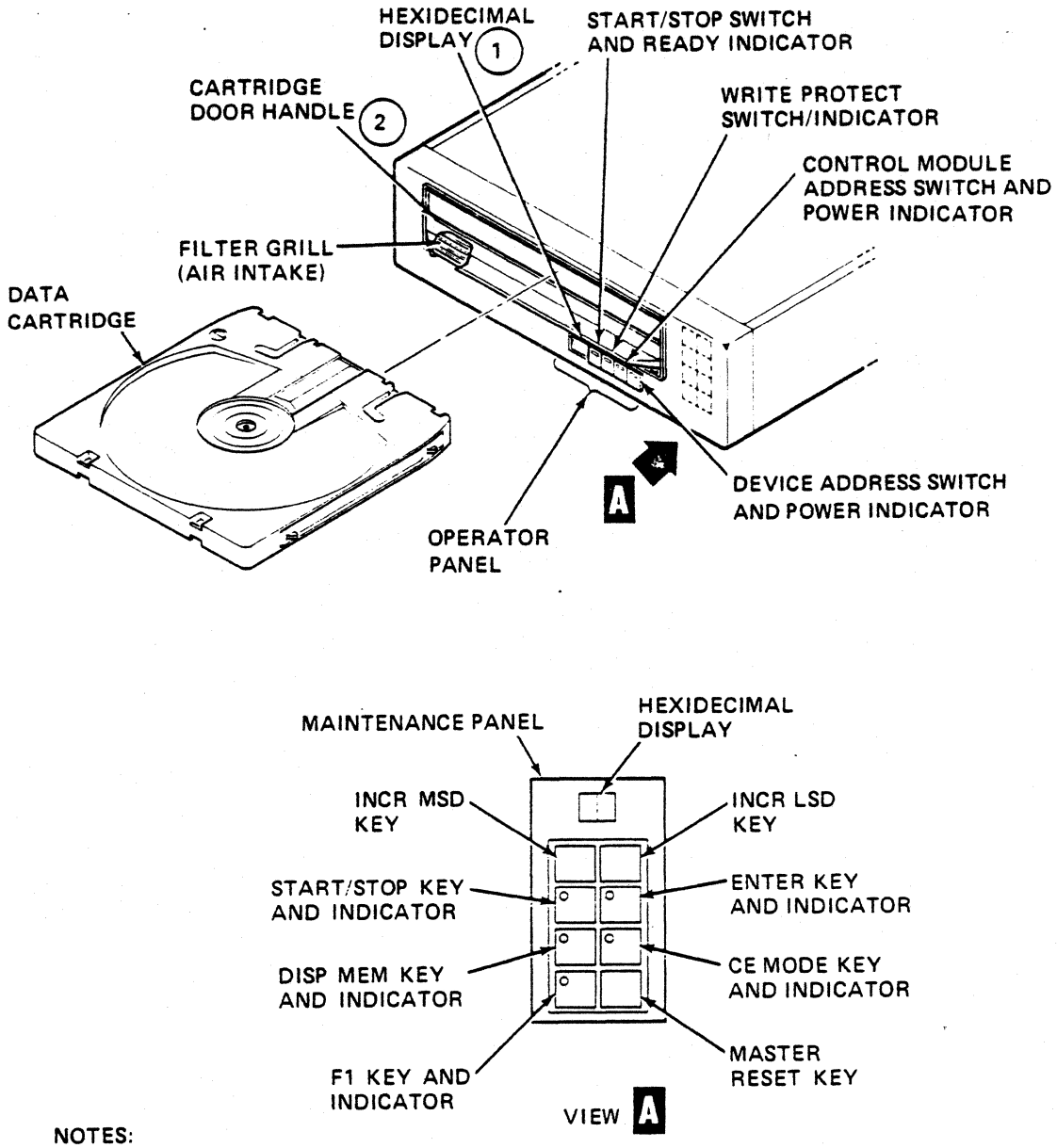
NOTE

The Maintenance Panel controls and indicators may be used ONLY by trained service personnel.

2.2. CONTROLS AND INDICATORS

2.2.1. Operator Panel

The Operator Panel is located on the front of the LD 1200. It contains a hexadecimal display, controls, and indicators as described in table 2-1 (see figure 2-1):



NOTES:

1. Display of 0 0 indicates successful test completion.
2. Pull down to open.

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Figure 2-1 LD 1200 Controls Indicators and Cartridge Loading

Table 2-1. Operator Panel Controls and Indicators

CONTROL/INDICATOR	DESCRIPTION	PURPOSE	COMMENT
Hexadecimal Display	Two-character LED display	Displays failure and subfailure codes and the state of normal machine operation.	When a failure is detected, the failure code remains on the display until the beginning of a diagnostic test.
START/STOP Switch	Alternate Action	Powers-up the Spindle Motor when depressed and locked into position. Powers-down the Spindle Motor when depressed and released from the locked position.	Used after the Data Cartridge is inserted into the LD 1200. The Host can also control the Spindle Motor.
READY Indicator	Green LED	Flashes during Spindle Motor power-up or power-down. When Spindle Motor is up to speed and the LD 1200 is ready, the indicator remains illuminated. When the Spindle Motor is powered down, it is extinguished.	Located within the START/STOP switch. Also extinguishes when a device fault occurs.
WRITE PROTECT Switch	Alternate Action	Provides media write protection when depressed and locked into position.	Write protection can also be achieved by Host interface commands and by rotating the Write Protect Tab on the Data Cartridge counter-clockwise (see Data Cartridge Write Protection illustration in this section). Any one, two, or three of the methods can be used at the same time.

Table 2-1. Operator Panel Controls and Indicators (continued)

CONTROL/INDICATOR	DESCRIPTION	PURPOSE	COMMENT
(Cont)			The tab is used before Data Cartridge insertion, the switch after Data Cartridge insertion.
WRITE PROTECT Indicator	Yellow LED	Illuminates when the write protect function is activated.	
CONTROL MODULE ADDRESS Switch	Consists of switch-cap press-fit onto the CONTROL MODULE ADDRESS receptacle.	Allows the user to select one of eight LD 1200 Control Module addresses.	The switch is installed during initial LD 1200 installation. It is externally marked 0 to 7. This switch cap selects the SCSI ID to which the LD 1200 will respond.
POWER Indicator	Green LED	Illuminates when power is applied to the LD 1200, indicating power is present in the unit.	Located within the CONTROL MODULE ADDRESS Switch.
DEVICE ADDRESS Switch	Consists of switch-cap press-fit onto DEVICE ADDRESS receptacle.	Not used on the LD 1200 with SCSI.	
POWER Indicator	Green LED	Illuminates when power is applied to the LD 1200, indicating power is present in the unit.	Located within the DEVICE ADDRESS Switch.

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2.2.2. Maintenance Panel

The Maintenance Panel is located in the front, right corner of the LD 1200, behind the front panel. It contains a hexadecimal display, controls, and indicators as shown in figure 2-1.

The Hexadecimal Display is used to display data input to the subsystem. This data includes test numbers, test options, test parameters, and memory locations. The display extinguishes during depression of the ENTER key, indicating the subsystem has received the input data. When appropriate, the subsystem outputs data in reply to the input data. The output data is also displayed on the Hexadecimal Display.

During diagnostic test execution, the Hexadecimal Display displays two-digit hexadecimal values. These values are the test and/or subtest numbers of the test currently being executed.

Table 2-2 describes Maintenance Panel controls and indicators. For more information on LD 1200 modes of operation mentioned in the following table, refer to the Firmware Overview subsection in this section of the manual.

Table 2-2. Maintenance Panel Controls and Indicators

CONTROL/INDICATOR	DESCRIPTION	PURPOSE	COMMENT
Hexadecimal Display	Two-character LED display	Displays data inputs and outputs	Extinguishes during depression of the ENTER Key.
INCR MSD Key	Membrane Key	Increments most-significant digit of the Hexadecimal Display.	The data input is represented as a hexadecimal value from 0 to F. It is displayed as the left or most-significant digit on the two-character Hexadecimal Display. Stepped or continuous key depression cycles the digit from 0 to F, restarting at 0 once F is reached.
INCR LSD Key	Membrane Key	Increments least-significant digit of the Hexadecimal Display.	The data input is represented as a hexadecimal value from 0 to F. It is displayed as the right or least-significant digit on the two-character Hexadecimal Display. Stepped or continuous key depression cycles the digit from 0 to F, restarting at 0 once F is reached.
START/STOP Key	Membrane Key	Depressing this key when in the Idle Mode, begins execution of a diagnostic test or validates an option.	

Table 2-2. Maintenance Panel Controls and Indicators (continued)

CONTROL/INDICATOR	DESCRIPTION	PURPOSE	COMMENT
		Depressing this key when in the Run Mode, enters the Stopped Mode. This stops execution of the diagnostic test currently running. Depressing this key when in the Stopped Mode restarts the test or subtest.	
START/STOP Indicator	LED	Illuminates to indicate the START/STOP key has been depressed	Located within the START/STOP key. Flashes while a test or subtest executes.
ENTER Key	Membrane Key	This key causes the firmware to save the data byte currently displayed on the Maintenance Panel. Depressing this key exits the Stopped Mode and enters the Idle Mode, allowing selection of a test or option.	Selecting a test in the Stopped Mode terminates the current test and places the subsystem in the Idle Mode. The new test number replaces the last test number entered.
ENTER Indicator	LED	Extinguishes while the ENTER key is depressed.	Located within the ENTER key.
DISP MEM Key	Membrane Key	Depressing this key when in the Idle Mode, enters the Display Mode. This allows a memory or parameter location to be displayed and/or modified. Depressing this key when in the Stopped Mode, enters the Display Mode.	Depressing the key when in the Display Mode after a memory location or parameter is displayed, returns to the Idle Mode. Depressing this key when in the Display Mode, returns to the Stopped Mode.

Table 2-2. Maintenance Panel Controls and Indicators (continued)

CONTROL/INDICATOR	DESCRIPTION	PURPOSE	COMMENT
DISP MEM Indicator	LED	Illuminates when DISP MEM key has been depressed.	Located within the DISP MEM key.
CE MODE Key	Membrane Key	Depressing this key when in the Normal Mode, enters the CE Mode.	All Maintenance Panel functions except Master Reset are enabled or disabled via the CE Mode key.
CE MODE Indicator	LED	Illuminates to indicate the LD 1200 is in the CE Mode.	Located within the CE Mode key. Upon entry to CE Mode, all Maintenance Panel indicators illuminate while the Hexadecimal Display cycles a display of 00, 11, 22, ... FF). This is followed by a similar check of the Operator Panel Hexadecimal Display.
F1 Key	Membrane Key	Depressing this key when in the Stopped or Idle Mode, allows subfailure codes to be displayed on the Operator Panel. Depressing this key when in the Display Mode, allows the most-significant byte of the current memory address to be displayed on the Operator Panel.	
F1 Indicator	LED	Illuminates when the F1 key has been depressed.	Located within the F1 key.
MASTER RESET Key	Membrane Key	Depressing this key causes the LD 1200 to go through a Power-On Reset sequence.	This key can be used anytime, regardless of current operations.

2.2.3. Power Supply

The ON/OFF switch (circuit breaker CB1) is located on the LD 1200 rear panel (refer to figure 1-11 in the General Description section). When this switch is set to the ON position (1), LD 1200 power is applied. Power is removed when it is in the OFF position (0).

2.3. POWER ON/OFF PROCEDURES

This subsection describes the procedures for powering-on and powering-off the LD 1200.

2.3.1. Power-On Procedure

(1) Refer to the Power and Grounding Requirements subsection, in Volume 1 of the Hardware Maintenance Manual, to determine the proper operating frequency and ac input voltage.

(2) Connect the LD 1200 to a standard convenience outlet with the proper facility power.

(3) At the LD 1200 rear panel, set circuit breaker CB1 to the ON position (1).

(4) At the Operator Panel verify that the two Power indicators are now illuminated (see figure 2-1) and that air is flowing out of the LD 1200 rear panel filter grill, indicating power is present.

The Power indicators remain illuminated until power is removed or the presence of a malfunction of the Power Supply causes them to extinguish.

At this time, a series of tests are automatically initiated by the LD 1200, establishing confidence in the internal components and determining that the unit is functioning properly.

2.3.2. Power-Off Procedure

(1) Wait until current LD 1200 activity is complete. Observe that the Operator Panel READY Indicator is extinguished (refer to figure 2-1).

(2) If a Data Cartridge is inserted in the unit, pull down the Cartridge Door on the front panel and remove the Data Cartridge.

(3) At the LD 1200 rear panel, set circuit breaker CB1 to the OFF position (0). The Operator Panel indicators extinguish and air no longer comes out of the rear panel filter grill vents, indicating that power to the unit is removed.

2.4. DATA CARTRIDGE LOADING/UNLOADING PROCEDURES

Before loading the Data Cartridge, data write protection can be manually activated, as follows:

(1) Each side of a Data Cartridge can be individually write protected. To write protect a given side, orient the Data Cartridge such that the label which identifies the side to be accessed is upside down. Rotate the Write Protect tab, which is now on the top side of the Data Cartridge, to the WRITE PROTECT position, as shown in figure 2-2.

(2) The alternate action WRITE PROTECT switch on the Operator Panel of the LD 1200 may be activated by the operator to write protect the Media in the unit (refer to figure 2-1.

The Data Cartridge may be loaded after the LD 1200 is powered-on and is idling. To load the Data Cartridge, proceed as follows (refer to figures 2-1 and 2-2):

(1) At the Operator Panel, verify that the START/STOP switch is in the STOP (out) position and the READY indicator is extinguished.

(2) Open the Cartridge Door by pressing down on the handle.

(3) Insert the Data Cartridge into the LD 1200 with the optical access doors to the rear and the label for the side to be accessed oriented right-side up. Push the Data Cartridge in until it snaps into place.

(4) Close the Cartridge Door by lifting the handle.

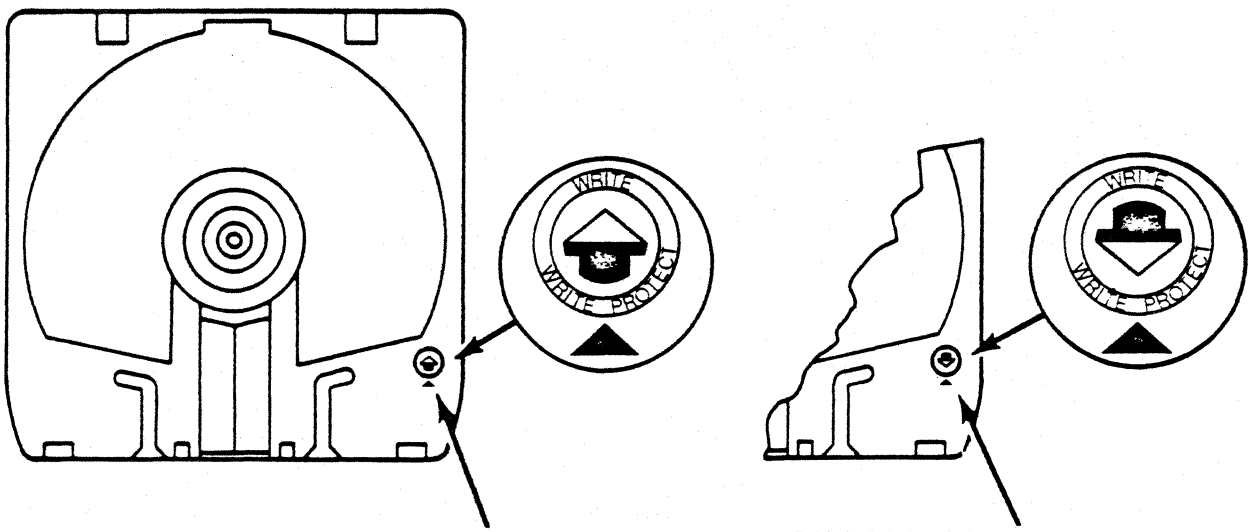
(5) At the Operator Panel, press the START/STOP switch to spin up the LD 1200. The READY indicator flashes during Spindle Motor power-up and initialization and remains illuminated after successful LD 1200 initialization.

To unload the Data Cartridge, proceed as follows (refer to figures 2-1 and 2-2):

(1) At the Operator Panel, verify that the START/STOP switch is in the STOP (out) position and the READY indicator is extinguished. This indicates the disk is not spinning and the LD 1200 is idle.

(2) Open the Cartridge Door by pressing down on the handle. The Data Cartridge ejects about one inch.

(3) Remove the Data Cartridge and close the door.



WRITE PROTECT SWITCH TAB SHOWN IN WRITE ENABLE (NOT WRITE PROTECTED POSITION)

WRITE PROTECT TAB SHOWN IN WRITE PROTECT POSITION

PB002128-4

Figure 2-2. Data Cartridge Write Protection

2.5. OPERATOR PANEL OPERATING PROCEDURES

Procedures for use of the Operator Panel are provided in the following subsections.

2.5.1. Data Write Protection

The Operator Panel may be used to write protect data. Write protection can be achieved anytime after the LD 1200 has been powered-on by depressing the WRITE PROTECT switch (refer to figure 2-1). The WRITE PROTECT indicator illuminates.

Write protection of data can also be achieved through commands issued by the Host interface or by activating the Write Protect Tab, located on the Data Cartridge (refer to the Cartridge Loading/Unloading subsection of this manual).

All three write protect features may be activated to function simultaneously, providing further assurance of write protection.

2.5.2. Disk Spin-Up/Down

To spin up the disk, proceed as follows (refer to figure 2-1):

(1) Verify that power is applied to the LD 1200 (POWER indicators in CONTROL MODULE and DEVICE ADDRESS switches illuminated. To apply POWER, refer to the Power-On Procedure subsection of this manual).

(2) Verify that a Data Cartridge is loaded in the LD 1200 (to load a Data Cartridge, refer to Data Cartridge Loading/Unloading Procedures subsection of this manual).

(3) At the Operator Panel, depress the START/STOP switch. The READY indicator flashes until spin-up is completed and the LD 1200 is fully ready. It then illuminates and remains illuminated until the Spindle Motor is spun down.

To spin down the disk depress the START/STOP switch located on the Operator Panel. The READY indicator flashes until spin down is completed. It then extinguishes and the subsystem returns to the Idle mode.

2.5.3. Running Operator Diagnostic Tests

The Operator Diagnostic Tests (also known as Automatic Self-Tests) are a series of functional tests run by the operator from the Operator Panel. It is the responsibility of the Customer Engineer (CE) to verify that the operator performs these tests before a service call is made, and to determine from the operator which failure codes appear during testing.

Operator Diagnostic Tests are divided into two groups. One groups runs with the disk at rest (not spinning). The other runs when the disk is spinning.

These tests are run from the Operator Panel using the START/STOP switch. If a failure code appears during testing, the operator can refer to the Trouble Isolation Guide subsection in the Customer User Manual for corrective action.

A failure code indicates that one or more of the following have occurred:

- Environment or Media Problems - This requires the operator to clean the LD 1200 interior and/or replace the Data Cartridge with one that is known to be good.
- Operator Errors - These require the operator to check for conditions such as the Cartridge Door left open, the Write Protect Tab on the Data Cartridge set to the Write Protect position, incorrect Data Cartridge insertion, etc.
- LD 1200 Circuit Problems - These require CE intervention.

The following operating instructions are presented as a general guideline for the running of Operator Diagnostic Tests. The Operator Panel subsection and figure 2-1 contain descriptions of the Operator Panel controls/indicators used in tests run by the operator.

(1) Verify that the LD 1200 is powered on (POWER indicators in CONTROL MODULE and DEVICE ADDRESS switches illuminated).

(2) Verify that a Data Cartridge is loaded in the LD 1200.

(3) At the Operator Panel, verify that the START/STOP switch is in the STOP position (button out, unlocked).

(4) Verify that the disk is not spinning.

(5) At the Operator Panel, momentarily press the START/STOP switch twice, setting it first to START, then to STOP. This action runs diagnostic tests. When all tests have run successfully, 00 is displayed on the Operator Panel.

(6) If a failure code is displayed on the Operator Panel, go to step 8.

(7) If successful completion code 00 is displayed, return the unit to online status and note the incident in the repair log.

(8) Write down the failure code.

(9) Gather as much information about the fault as possible, e.g.:

- All failure codes that have been displayed during this failure.
- The frequency at which the failure codes appeared.
- If possible, the name of the operation in progress when the failure occurred.
- If the failure is intermittent, collect the information received from the operating system at the Host during the times the failure occurred.

(10) Contact Customer Engineering for assistance. At this time, provide the CE with the failure code and as much information on the failure as possible. Also, describe the steps taken in attempting to analyze and correct the fault.

2.6. MAINTENANCE PANEL OPERATING PROCEDURES

The Maintenance Panel is for use, by the CE only, in diagnosing LD 1200 failures. It is located behind the LD 1200 front panel. To gain access to the Maintenance Panel:

(1) At the right side of the Filter Grill, located on the LD 1200 front cover, push and hold the Filter Grill Latch outward to release the Filter Grill (refer to figure 2-3).

(2) Grasp the right side of the grill and pull it away from the latch.

(3) Pull the left side of the grill free of the Filter Grill Retainer and remove the grill from the unit.

(4) Inside the front cover of the LD 1200, loosen the two captive screws that hold the cover to the unit and remove the cover. Removing the cover allows access to the Maintenance Panel, located on the right side of the LD 1200.

Before using diagnostic tests for trouble isolation, visually inspect the LD 1200 for abnormal conditions, as described in the Inspection subsection of the LD 1200 Hardware Maintenance Manual, Volume 1. Before initiating a given diagnostic test, LD 1200 operational status must be as specified in the associated table, provided in the Structured Analysis Method (SAM) Tables subsection of the LD 1200 Hardware Maintenance Manual, Volume 1.

Controls and indicators used in running diagnostic tests are illustrated in figure 2-1.

2.6.1. Diagnostic Test Operating Procedure (Performed Only by the Customer Engineer)

(1) At the Operator Panel, verify that the START/STOP switch is in the STOP (button out, unlocked) position (see figure 2-1).

(2) Gain access to the Maintenance Panel as described previously in this subsection.

(3) At the Maintenance Panel, press the CE MODE key until the CE MODE indicator illuminates. This indicates the LD 1200 is in the CE Mode.

On entry to the CE Mode, the following occur:

- All the indicator LEDs on the Maintenance Panel illuminate.
- At the same time, the Maintenance Panel and Operator Panel Hexadecimal Displays cycle through their hexadecimal character sets (00 through FF).
- Test number "10" (run all tests) is displayed on the Maintenance Panel Display.

The LD 1200 now enters the Idle Mode, under control of the Maintenance Panel.

(4) Select or change a test or an option. This is done by pressing the INCR MSD and INCR LSD keys until the desired test number or option is displayed. Available test options are described in the Selecting an Option subsection of this manual.

(5) Enter the desired test or option by pressing the ENTER key. The Hexadecimal Display blanks while the key is pressed and displays the desired test or option number after it is released. A blinking FF is displayed if an invalid option number is entered.

Once an option is entered, all tests executed use that option until it is changed.

(6) To run the test or validate the option indicated on the Hexadecimal Display, press the START/STOP key.

If the DISP MEM indicator does not illuminate, no input parameters are required and the test is executed. A 00 is displayed on the Operator Panel Hexadecimal Display upon successful test completion.

(7) To stop test execution, press the START/STOP key. The test stops, the START/STOP indicator illuminates, and LD 1200 operation enters the Stopped Mode.

(8) To resume test execution after stopping, press the START/STOP key. The currently active test resumes execution.

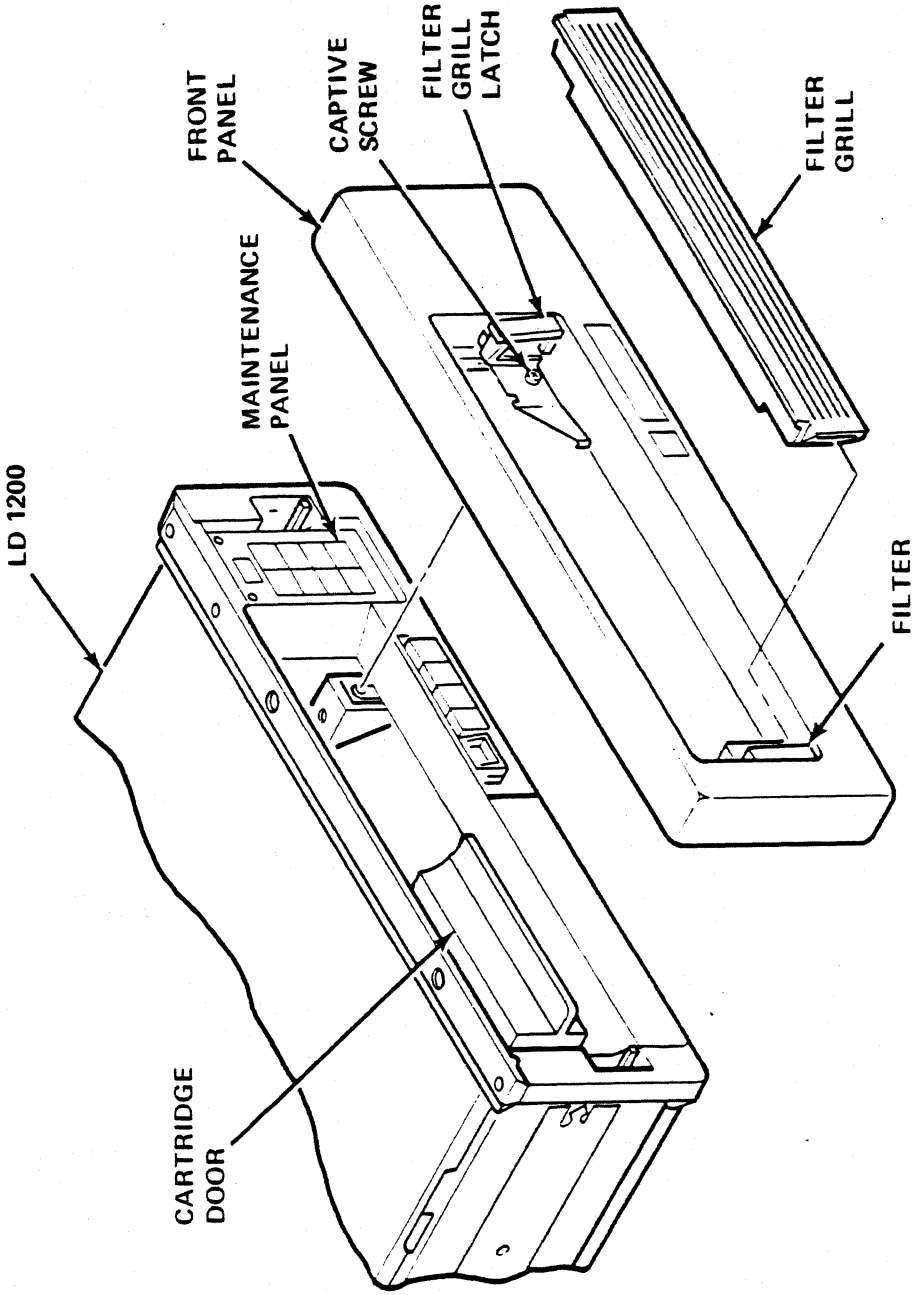


Figure 2-3 LD 1200 Maintenance Panel Access

2.6.2. Firmware Overview

The following subsection describes LD 1200 diagnostic modes of operation (refer to figure 2-4).

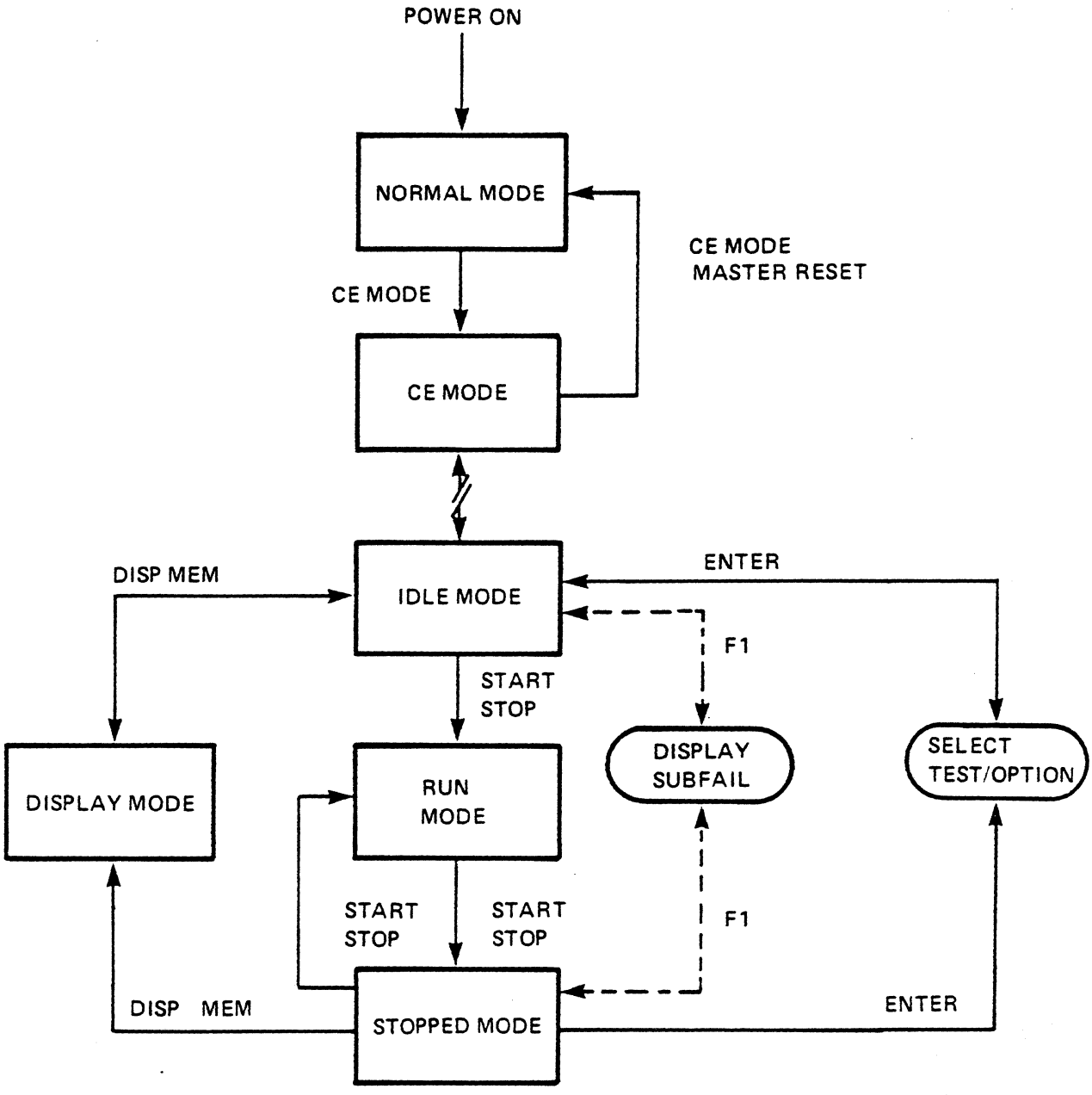


Figure 2-4. LD 1200 Diagnostic Modes of Operation

2.6.2.1. Normal Mode

Immediately following a Power-On or Reset, and until entry to the CE Mode, the LD 1200 is in the Normal Mode. To enter the CE Mode from the Normal Mode, the CE MODE key is pressed and held until the CE MODE indicator illuminates.

2.6.2.2. CE Mode

The CE Mode is entered from the Normal Mode, illuminating the CE MODE indicator. Before entry into the CE Mode is allowed, the Spindle must be at rest (not spinning) and the START/STOP switch, located on the Operator Panel must be set to the STOP position (out, unlocked).

- Idle Mode - The subsystem enters the Idle Mode immediately on entry to the CE Mode, completion of a diagnostic test, or termination of a diagnostic test. In the Idle Mode, only the CE MODE indicator is illuminated.

  In the Idle Mode, the Maintenance Panel may be used to select a diagnostic test or option, display a memory location parameter, subfailure code, or start a test.

- Run Mode - When a test is started, the Run Mode is entered, the CE MODE indicator is illuminated, the START/STOP indicator flashes, the current test number is displayed on the Maintenance Panel, and the Operator Panel Hexadecimal Display is blanked.

  While in the Run Mode, a test can be stopped or the MASTER RESET key can be used to reset the machine. No other Maintenance Panel functions are permitted.

- Display Mode - While in the stopped or Idle Mode, pressing the DISP MEM key places the LD 1200 in the Display Mode and illuminates the DISP MEM indicator.

2.6.2.3. Stopped Mode

The subsystem enters this mode when a test is stopped, and remains in this mode until the test is resumed or another test or option is selected.

2.6.3. Selecting a Test

A new test may be selected when the LD 1200 is in either the Idle or Stopped Mode. The Maintenance Panel Hexadecimal Display must be changed to show the new test number. This is done by using the INCR MSD and INCR LSD keys to change the display to the desired test number, then by pressing the ENTER key once, to enter the new test number.

Test selection in the Stopped Mode terminates the current test, places the subsystem in the Idle Mode, and replaces the current test number with the last test number entered.

2.6.4. Selecting an Option

The procedure for selecting an option is the same as for selecting a test. The Maintenance Panel Hexadecimal Display must be changed to show the new option number and the ENTER key pressed once to enter the number.

Each option has its own number preventing possible subsystem or user confusion. Tests are numbered 10 through FF, while options are numbered 00 through 0F. Once an option is selected, all tests run with it until it is changed.

Options use three variables to determine test module flow:

- TRC (Test Repetition Count) - Determines the number of times the test will be repeated (looped). The TRC default value is one.

- PC (Pass Count) - An internal count of the number of times a test or subtest executes without a detectable failure.

- FC (Fail Count) - An internal count of the number of times a test or subtest executes with detectable failures.

Available options are:

- Option 00 (Loop Until FC=1 or PC=TRC) - The test executes repeatedly until FC equals one or PC equals TRC.

- Option 01 (Loop Until FC = TRC or PC = 1) - The test executes repeatedly until FC equals TRC or PC equals one.

- Option 02 (Loop Until FC = TRC or PC = 255 Decimal) - The test executes repeatedly until FC equals TRC or PC equals 255.

- Option 03 (Loop Until PC = TRC or FC = 255 Decimal) - The test executes repeatedly until PC equals TRC or the FC equals 255.

- Option 04 (Loop Forever Until FC = 1) - The test executes repeatedly until FC equals one or it is stopped.

- Option 05 (Loop Forever and Ignore Errors) - Failures are ignored and the test is executed repeatedly until stopped.

2.6.5. Starting a Test or Option

Pressing the START/STOP key located on the Maintenance Panel, causes the LD 1200 to run the current test or validate the current option.

When an illegal test or option is selected, the Maintenance Panel flashes the illegal number, the Operator Panel displays a blinking FF, and the LD 1200 returns to the Idle Mode. At this point, the CE must verify whether the test number selected exists or whether the option selected is legal.

When a legal test is selected, the LD 1200 automatically enters the Run Mode, beginning test execution.

2.6.6. Entering Parameters

Parameters can be entered into the ECC Parameter Block using the Display/Modify Memory feature of the subsystem, described in the Displaying/Modifying Memory subsection of this manual. Initially, the ECC Parameter Block contains default values for the test.

2.6.7. Stopping/Resuming a Test

A test currently being executed may be stopped by pressing the START/STOP key, located on the Maintenance Panel. This action causes the LD 1200 to enter the Stopped Mode and illuminates the START/STOP indicator.

A test that is currently stopped but still active (LD 1200 in the Stopped Mode) may be resumed by pressing the START/STOP key.

2.6.8. Displaying a Subfailure Code

When the LD 1200 is in the Idle or Stopped Mode, with a failure code displayed on the Operator Panel, the associated subfailure code (if applicable) can be displayed on the Operator Panel by pressing and holding the F1 key on the Maintenance Panel. The subfailure code replaces the failure code on the Operator Panel Hexadecimal Display as long as the F1 key is pressed.

Subfailure codes provide more specific information on the failure. A subfailure display of 00 indicates there is no associated subfailure code.

2.6.9. Displaying/Modifying Memory

Any ROM, RAM, or Common Memory location in the LD 1200 may be displayed on the Maintenance Panel Hexadecimal Display. RAM and Common Memory contents can be changed using the Modify Memory feature of the subsystem.

The display or change of memory involves a series of three bytes of information. The first byte defines the type of memory access:

00 30K PROM, 2K RAM, and Lower Common Memory Page
01 30K PROM, Hidden ROM, and Lower Common Memory Page
02 30K PROM, 2K RAM, and Upper Common Memory Page
03 30K PROM, Hidden ROM, and Upper Common Memory Page
04 ECC Parameter Block
05 Voltage Margin Parameter
06 TRC, Pass Count, Fail Count, Run Option

Refer to figure 2-5 for graphic representation of memory access types 00 through 03.

The second byte defines the most-significant byte (MSB) of the memory address being accessed. The third byte defines the least-significant byte (LSB) of the memory address being accessed.

NOTE

The full Z80 address space of 64K is available in all memory access types. Consequently, there are no illegal address entries.

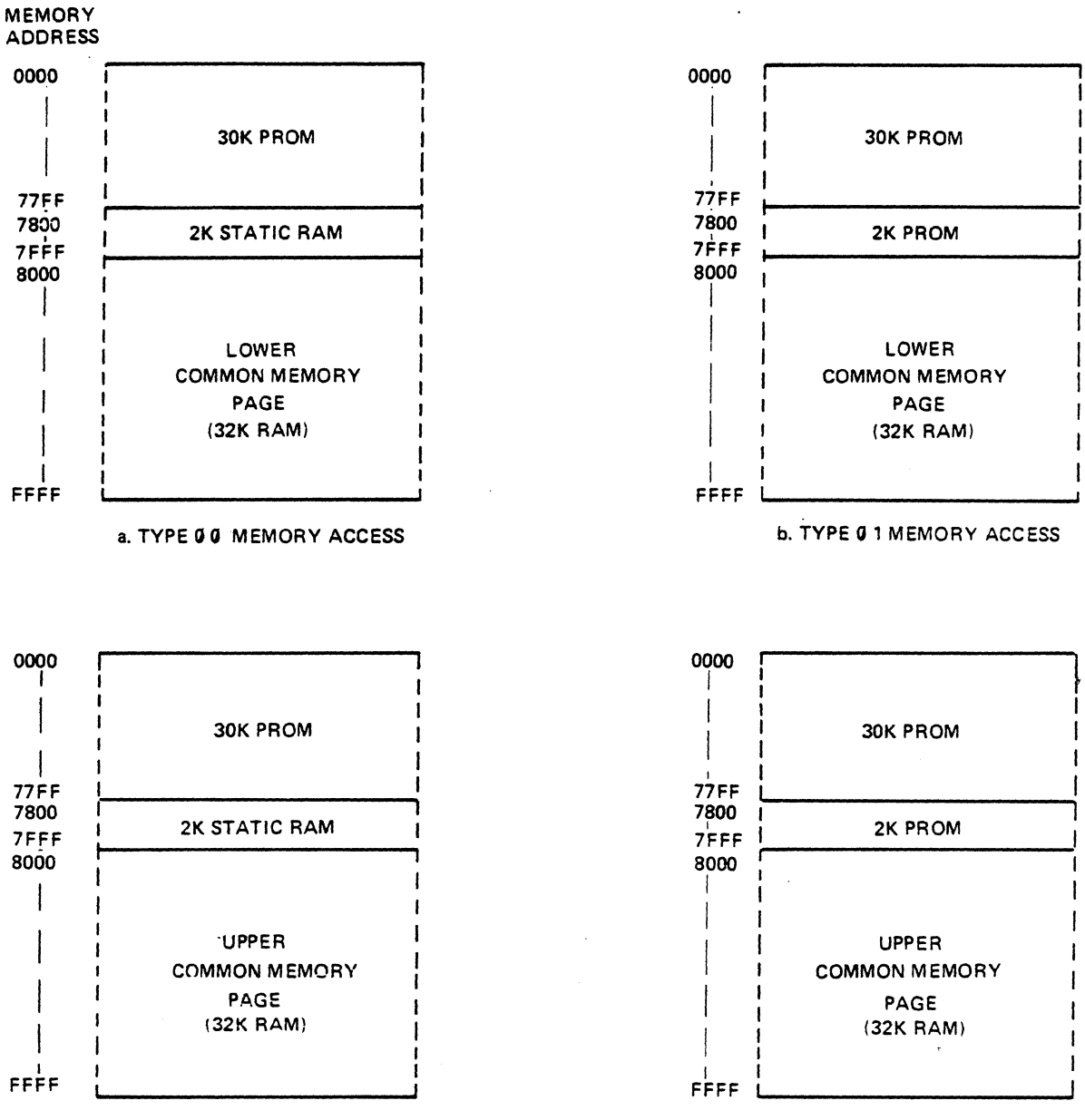


Figure 2-5. Memory Access Maps

The procedure for displaying or modifying memory is as follows:

(1) At the Maintenance Panel, press the DISP MEM key until the DISP MEM indicator illuminates. This causes the LD 1200 to enter the Display Mode and display the current memory access type on the Maintenance Panel Hexadecimal Display. The subsystem now expects three bytes to be entered to define the location in memory to be displayed.

(2) If the memory access type displayed is to be modified, modify it using the INCR MSD and INCR LSD keys to change the display to the desired value. If not, go to step 3.

(3) Press the ENTER key to save the contents of the display to the subsystem. The MSB of the current memory address is now displayed on the Maintenance Panel Hexadecimal Display.

(4) If this byte is to be modified, modify it using the INCR MSD and INCR LSD keys to change the display to the desired value. If not, go to step 5.

(5) Press the ENTER key to save the contents of the display to the subsystem. The LSB of the current memory address is now displayed on the Maintenance Panel Hexadecimal Display.

(6) If this byte is to be modified, modify it using the INCR MSD and INCR LSD keys to change the display to the desired value. If not, go to step 7.

(7) Press the ENTER key to save the contents of the display to the subsystem. The subsystem displays the first byte of the selected memory location on the Maintenance Panel Hexadecimal Display and the MSB of the address on the Operator Panel. To display the LSB of the address on the Operator Panel, press and hold the F1 key. The LSB replaces the MSB as long as F1 is pressed.

(8) To enter a new value in the displayed memory location:

(a) Use the INCR MSD and INCR LSD keys to change the value displayed to the new value.

(b) Press the ENTER key. The displayed (new) value is written in memory and the contents of the next memory location in sequence are displayed on the Maintenance Panel Hexadecimal Display. The LSB of the new memory address is displayed on the Operator Panel. The MSB of the address can be displayed using the F1 key, as described in step 7.

To display the next memory location in sequence, leaving the displayed value unchanged, press the ENTER key. The displayed (unchanged) value is written in memory and the contents of the next memory location are displayed on the Maintenance Panel. The new memory address is displayed on the Operator Panel as described in step 7.

(9) To exit the Memory Display/Modify Mode, press the DISP MEM key until the DISP MEM indicator extinguishes.

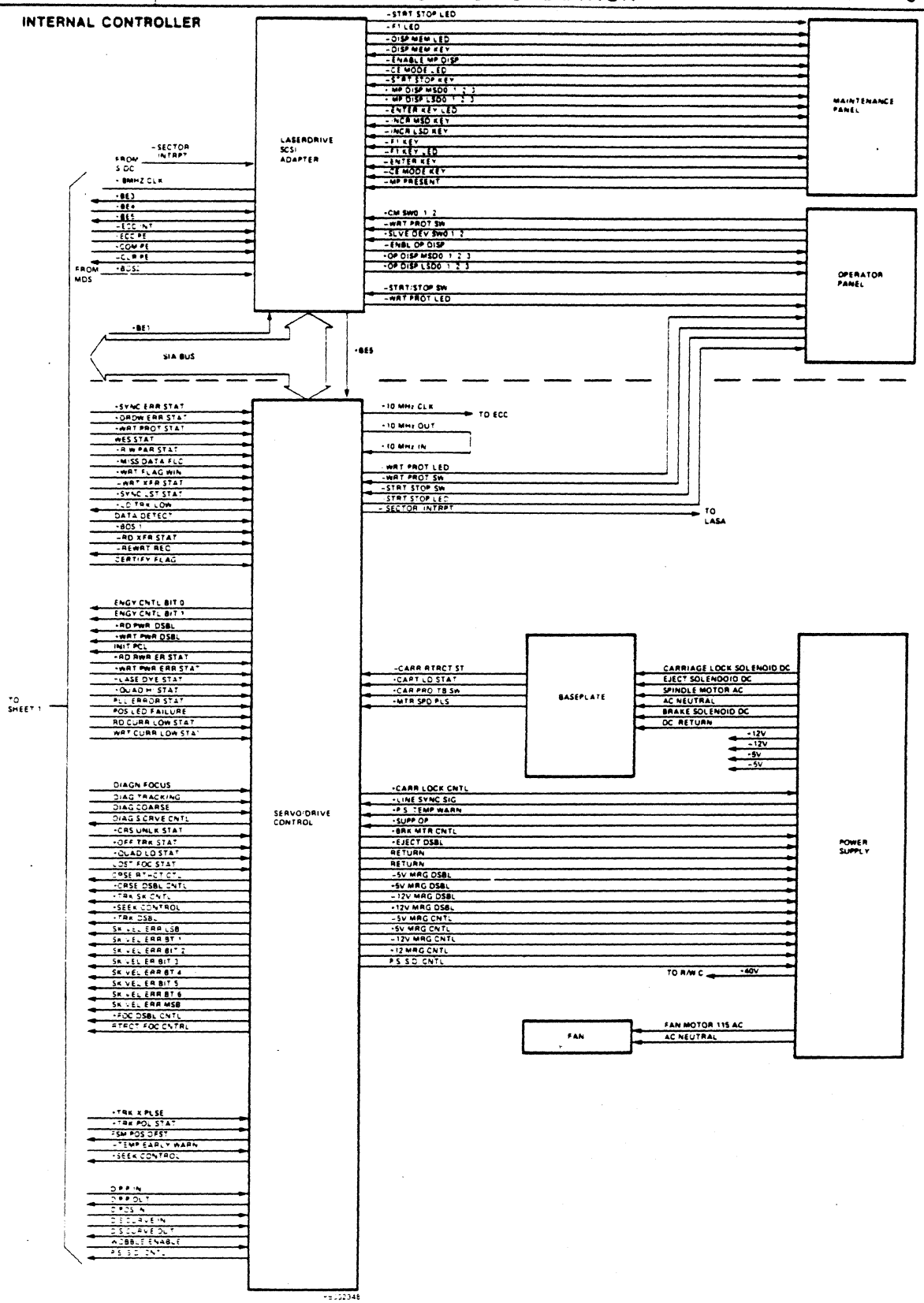


Figure 3-1 LD 1200 Block Diagram
(Sheet 2 of 2)

- Operator Panel
- Maintenance Panel

A brief functional description of each of these major components is provided in the following subsections. These descriptions are followed by subsections containing detailed circuit descriptions and accompanying diagrams.

3.2.1. Interfaces

The LD 1200 includes two major interfaces, the Small Computer System Interface (SCSI) and Internal Device Interface (IDI)/System Interface Assembly (SIA). The SCSI is the external interface that enables the LD 1200 to communicate with the Host. The IDI/SIA is the internal interface that enables major components of the LD 1200 to communicate data and status with one another.

3.2.2. LD 1200 SCSI Adapter PCA

This PCA contains the majority of the LD 1200 internal controller logic, which performs the following functions:

- Interfaces with the Host via the SCSI for command, data, and status transfers
- Interfaces with the ECC PCA, MDS PCA, and Servo/Drive Control PCA via the IDI/SIA for command, data, and status transfers
- Interfaces the Operator Panel with the remainder of the LD 1200

3.2.3. Error Correction Code and Common Memory Interface Unit PCA

This PCA generates error correction characters which are loaded into Common Memory with write data. Functionally, the ECC facility divides the Data Field into 5 segments of 205 bytes each and operates on each segment. The encoding function generates 20 bytes of parity check characters from the 205-byte segment and appends them to the segment in Common Memory, creating a 225-byte codeword.

As data is read from the Media, the ECC PCA generates 20 bytes of syndromes for each 225-byte codeword. A syndrome that equals zero implies that a segment contains no errors. Nonzero syndromes are processed by the ECC PCA to locate and correct the bits in error. The ECC PCA also provides Common Memory to buffer data and status transfers between the LD 1200 and Host.

3.2.4. Servo/Drive Control PCA

The Servo/Drive Control PCA provides the intelligence for the LD 1200 servo and drive functions, controlling laser power and Carriage movement. Functions provided by the Servo/Drive Control PCA include:

- Coarse and fine tracking
- Seek velocity adjustment
- Focus control

- Laser power level control
- Quad sum monitoring
- Write retries
- Fault and error handling
- Operator Panel switch and indicator control
- Header address filtering
- Power supply monitoring
- Carriage retract control
- Status accumulation
- Diagnostic self-checking of drive circuits

3.2.5. Servo Systems PCA

The Servo Systems PCA controls Carriage servo functions by providing the following:

- Focus Servo Loop
- Fine Tracking Servo Loop
- Coarse Tracking Servo Loop

These three functions are controlled by the Servo Microprocessor on the Servo/Drive Control PCA.

3.2.6. Error Signal Generator PCA

The Error Signal Generator PCA generates and amplifies the servo error signals that are used by the Servo Systems PCA to control Carriage movement:

- Fine Servo Motor Position Offset signal
- Fine Servo Motor Error signal
- Quad Sum signal
- Focus Error signal
- Tracking Error signal

3.2.7. Read/Write Control PCA

The Read/Write Control PCA controls Read and Write laser power, provides automatic gain control of read data, and provides timing signals for the Read/Write Channel. Laser power is monitored and adjustments are made by varying the Read and Write Power Current Sources on the PCA. Write data pulses from the Modulator Demodulator Synchronizer (MDS) PCA are shaped on this PCA and routed to the Carriage.

3.2.8. Modulator Demodulator Synchronizer PCA

The MDS PCA performs basic data manipulation functions in the LD 1200:

- Sector Mark decoding, synchronizing the Read/Write Channel to the beginning of each sector
- Sector identification
- Two-Out-of-Nine (TOON) encoding and decoding of data
- Data serialization and deserialization
- Data interleaving and de-interleaving
- Direct Read During Write (DRDW) detection of written monoholes
- Automatic rewrite operations

3.2.9. Carriage

The Carriage consists of three interdependent systems:

- Optical System
- Carriage Electronics
- Electromechanical System

The Carriage reacts to control signals from the Servo Systems PCA to move the laser pen to the area of the disk on which data is to be read or written. Write pulses from the Read/Write Control PCA modulate Laser Diode power, enabling the laser light beam to melt data monoholes in the Media. To read data from the Media, the Laser Diode supplies a light beam to the Media at the read power level. Reflected light from this beam is converted to read data pulses by the Optical System and Carriage Electronics and is routed through the Read/Write Control PCA to MDS PCA.

3.2.10. Media

The Media provides the physical medium in which data is written. It consists of a 12-inch diameter glass sandwich disk which includes two substrates, separated by circular spacers, a polymer intermediate layer, and a sensitive Tellurium Alloy layer, in which data can be written. Sector Header and clock information are prestamped in grooves on the disk.

3.2.11. Baseplate

The cast aluminum Baseplate provides the main supporting structure and mounts for the critical mechanical, electromechanical, and electroptical components of the LD 1200.

3.2.12. Power Supply

The switch mode type Power Supply provides dc power for LD 1200 logic, electro-optical, and electromechanical components. All dc outputs except +40 volts are protected against overvoltage and undervoltage conditions.

3.2.13. Operator Panel

The Operator Panel provides controls and indicators which give an operator limited control over LD 1200 operation and allow monitoring of diagnostic self-test results.

3.2.14. Maintenance Panel (Optional)

The Maintenance Panel provides controls and indicators which enable a Customer Engineer to perform LD 1200 diagnostic tests. Using this panel the Customer Engineer can select and initiate diagnostic self-tests.

3.3. LD 1200 FUNCTIONS

An overview of primary LD 1200 functions is provided in the following subsections. The overview of a given function follows that function through all the circuitry used to implement it. If more information is required on a particular circuit, it can be found in the detailed theory subsection for the appropriate PCA.

3.3.1. Drive Initialization and Focus

LD 1200 initialization is described in the Seek subsection.

3.3.2. Seek

A Seek may be initiated by the Host (normal Seek) or by the Internal Controller (Jumpback Operation). Both types of Seeks are described in the following subsections.

Prior to a Host-Initiated Seek, a Data Cartridge must be installed in the LD 1200, and the START/STOP switch pressed. When the START/STOP switch is pressed, LD 1200 initialization begins and is controlled by the Drive Control Microprocessor on the Servo/Drive Control PCA. During initialization, Focus is established, Fine and Coarse Tracking are initialized, and the Drive Control Microprocessor directs a Seek to Track 0. Once this occurs, the LD 1200 is ready for a Host-Initiated Seek.

After LD 1200 initialization, the Drive Control Microprocessor goes into a Ready Idle state while waiting for a Read, Write, or Seek request from the Host. During this time, it maintains Drive operation, proper focus, and tracking. When an error is detected, it conducts error recovery procedures. The Drive Control Microprocessor monitors Drive status, such as Operator Panel switch settings and LD 1200 error statuses. It reports these statuses to the Internal Controller Interface (ICI) PCA after Sector Interrupts. It also determines the position of the Fine Servo Motor (FSM) relative to the desired sector and executes a Jumpback, if needed. Refer to figure 3-2 for a flow chart of this Ready Idle state.

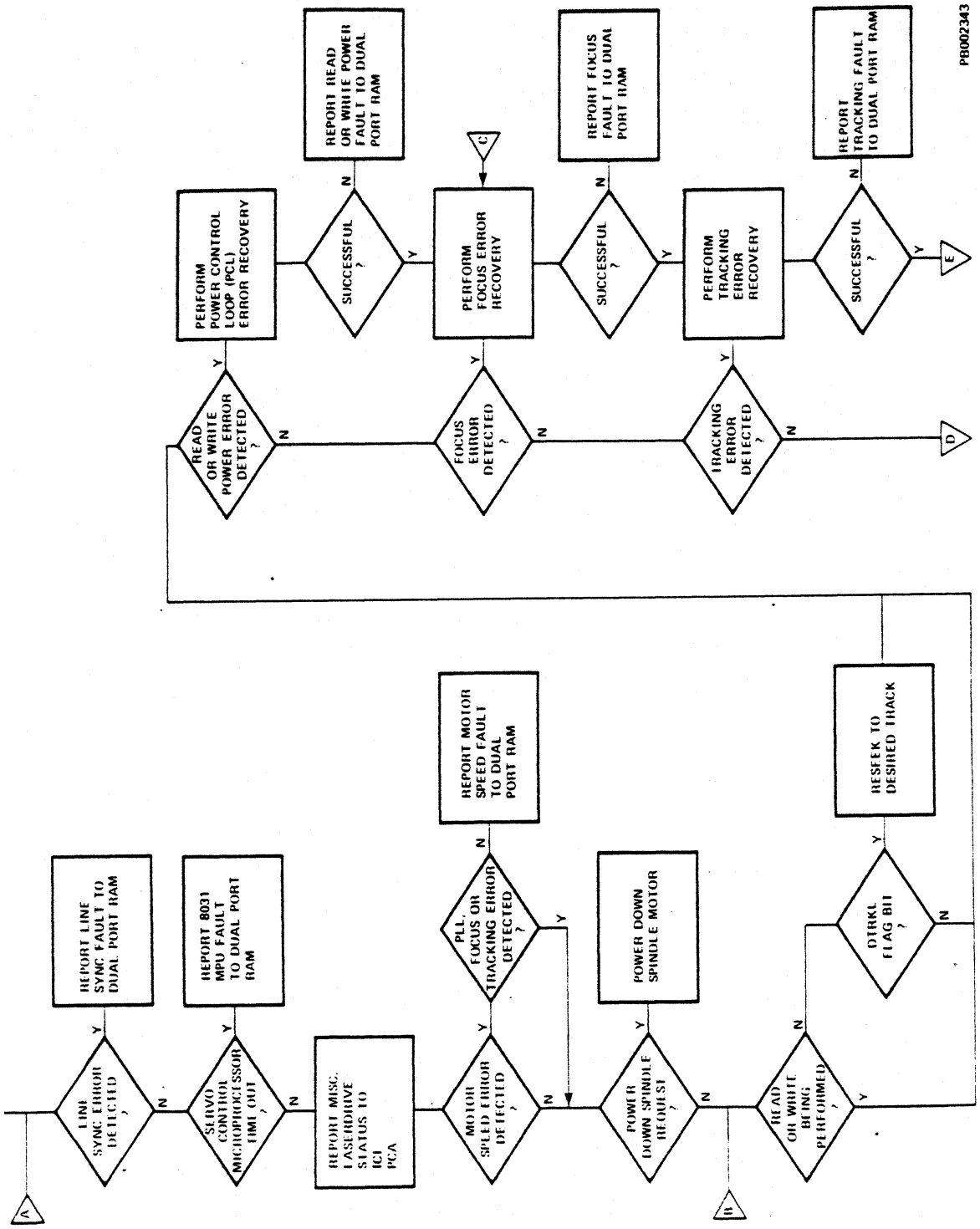


Figure 3-2 Drive Control Microprocessor Ready/Idle State (Sheet 1 of 2)

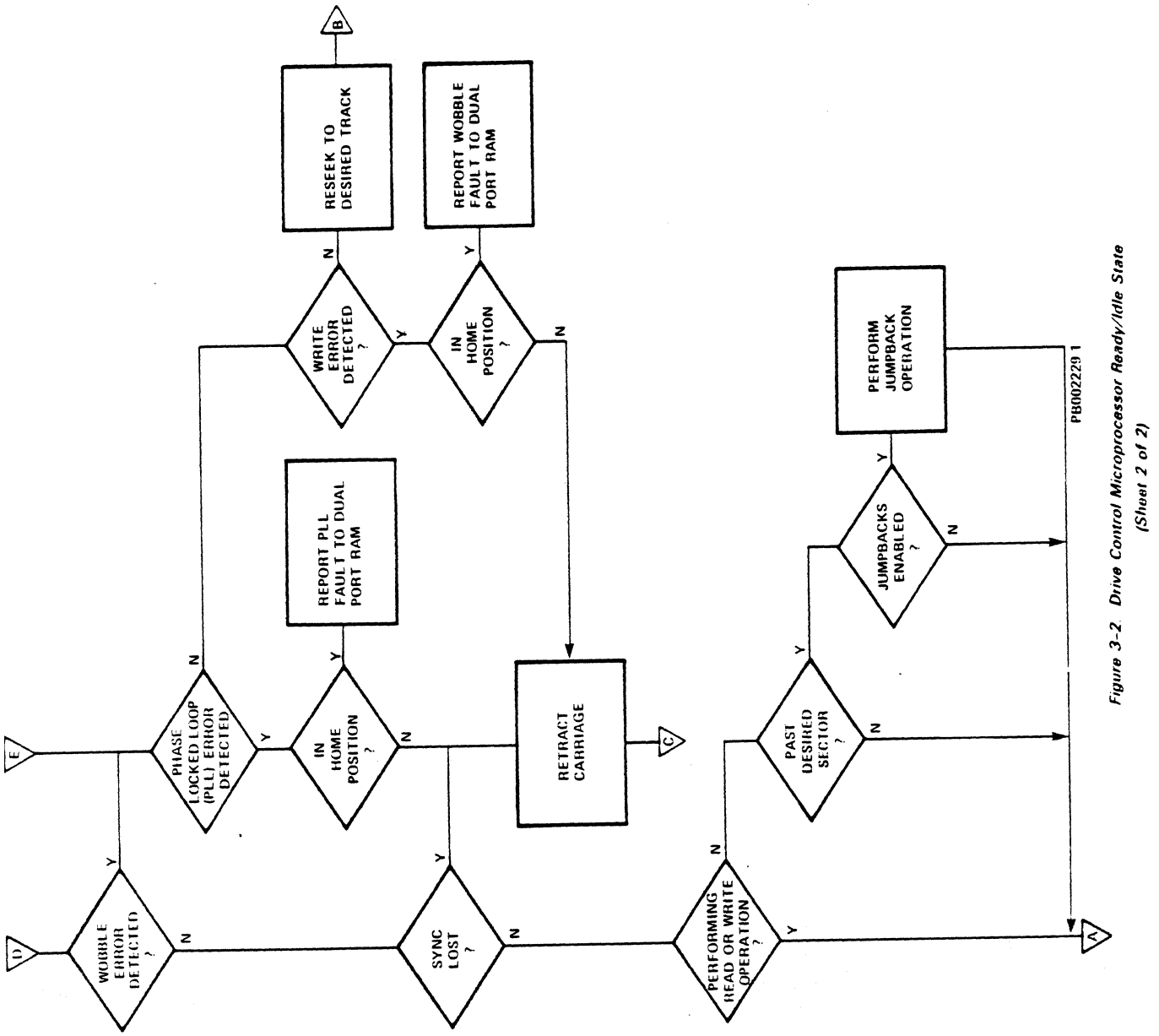


Figure 3-2. Drive Control Microprocessor Ready/Idle State (Sheet 2 of 2)

When the Host requests a Read or Write operation for a particular sector, the request is interpreted by the ICI PCA. The ICI PCA checks for a legal Seek address, then sends a Seek command to the Servo/Drive Control PCA, followed by a Read or Write command to the Modulator Demodulator Synchronizer (MDS) PCA.

The Servo/Drive Control PCA contains two microprocessors: a Servo Control Microprocessor, and a Drive Control Microprocessor. The Servo Control Microprocessor determines the Seek Velocity Profile during Seeks, and reports tracking errors to the Drive Control Microprocessor. The Drive Control Microprocessor sequences LD 1200 initialization procedures, receives Seek commands from the ICI PCA, verifies that it is a legal Seek address, and directs the Seek. It also directs error recovery, sends error status to the ICI PCA, and controls Jumpbacks.

3.3.2.1. Seek Initialization

When the Servo Control Microprocessor receives a Seek request from the Drive Control Microprocessor and the desired track address from the Dual Port RAM, it places the Servo Systems PCA in a Seek mode. The Servo Control Microprocessor then controls the Seek with the Seek Velocity Error Signal.

The Seek Initialization routine determines the magnitude (length) and direction of the Seek, and which Seek routine is used. There are three routines for each direction, depending on the length of the Seek: fast, medium, or slow. Once in the selected routine, control is given to the next routine, depending on tracks remaining (i.e., fast routine switches to medium, etc.).

Once the Seek magnitude and direction are determined, a Seek is initiated.

3.3.2.2. Seek

The Servo Control Microprocessor notifies the Drive Control Microprocessor of a Seek in progress. As the Servo Control Microprocessor controls the Seek, the Drive Control Microprocessor monitors the progress of the Servo Control Microprocessor.

During Seek operations, the Servo Control Microprocessor outputs an 8-bit Seek Velocity Error signal to a digital-to-analog converter (DAC) on the Servo Systems PCA. The DAC then drives the FSM toward the desired track.

The FSM Error Signal, generated by the Position Sensor on the Carriage, indicates the relative shift of the FSM with respect to the carriage body. When the FSM Error Signal does not equal zero, the Coarse Servo Loop drives the Coarse Actuator to correctly reposition the Carriage under the FSM. In this manner, the Carriage follows the movement of the FSM.

As the FSM moves, the light beam crosses tracks, generating the Push-Pull Signal. The Push-Pull Signal, from the System Optics/Quad Detector (figure 3-3), carries track crossing information. The Quad Detector detects deviation of the focused light beam from the center of the track. As the beam crosses a track, the distribution of light intensity reflected at the Quad Detector changes from side to side a proportional amount (refer to figure 3-4). The Push-Pull Signal is generated by summing the quadrants of the Quad Detector as shown in figure 3-4. The amplitude of the Push-Pull Signal is then normalized, and Wobble Byte information is summed with it, by the Error Signal Generator Circuitry (refer to figure 3-3). The resultant Tracking Error Signal is sent to the Track Crossing Detection Circuitry, where a pulse is generated each time the Tracking Error Signal crosses a zero threshold. This pulse is sent to the Servo Control Microprocessor, indicating how many tracks have been crossed at any point during a Seek.

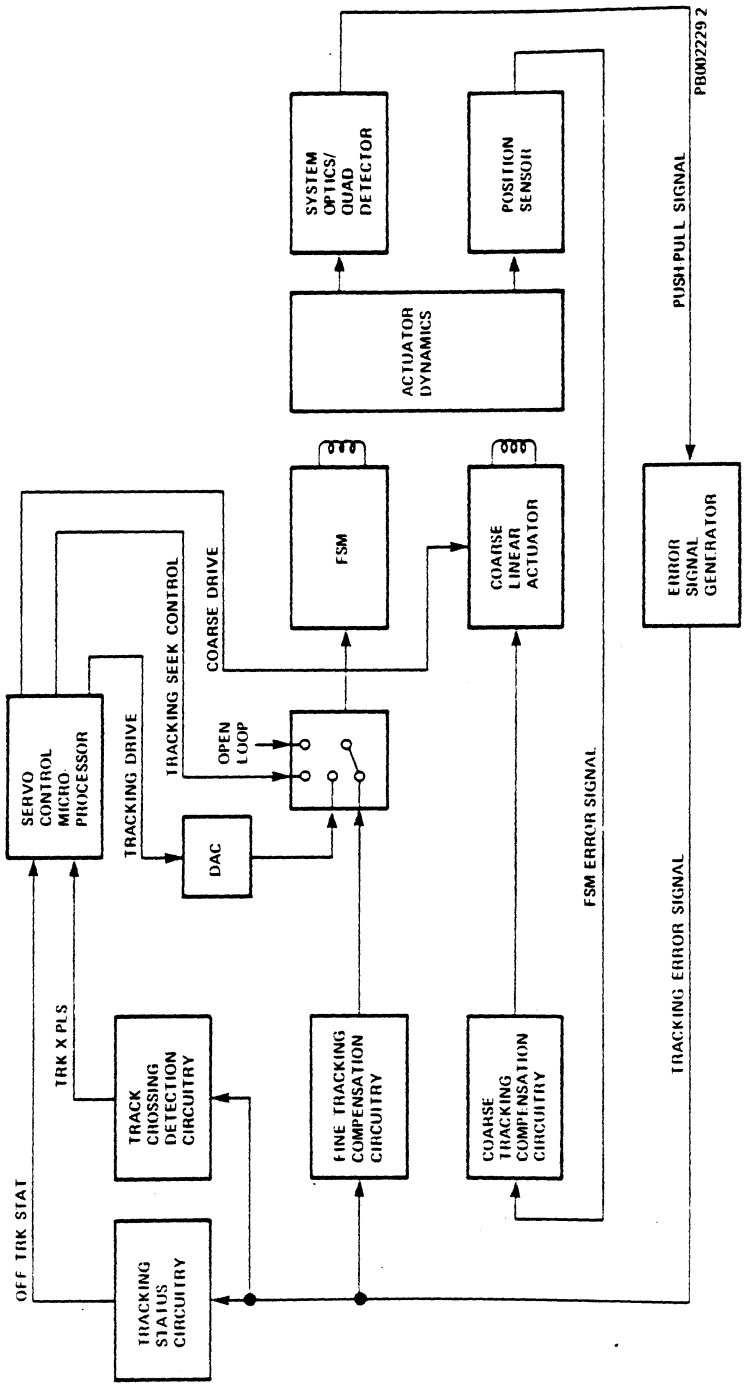


Figure 3-3 Error Signal Generator Circuitry

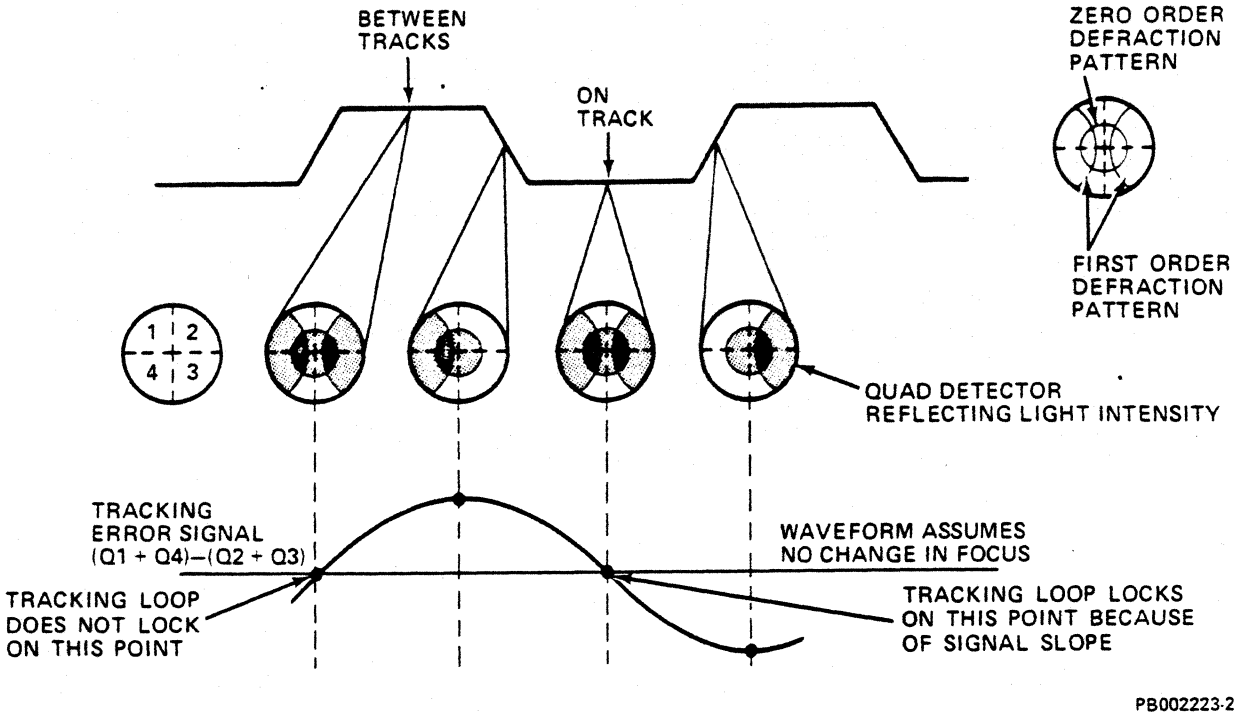


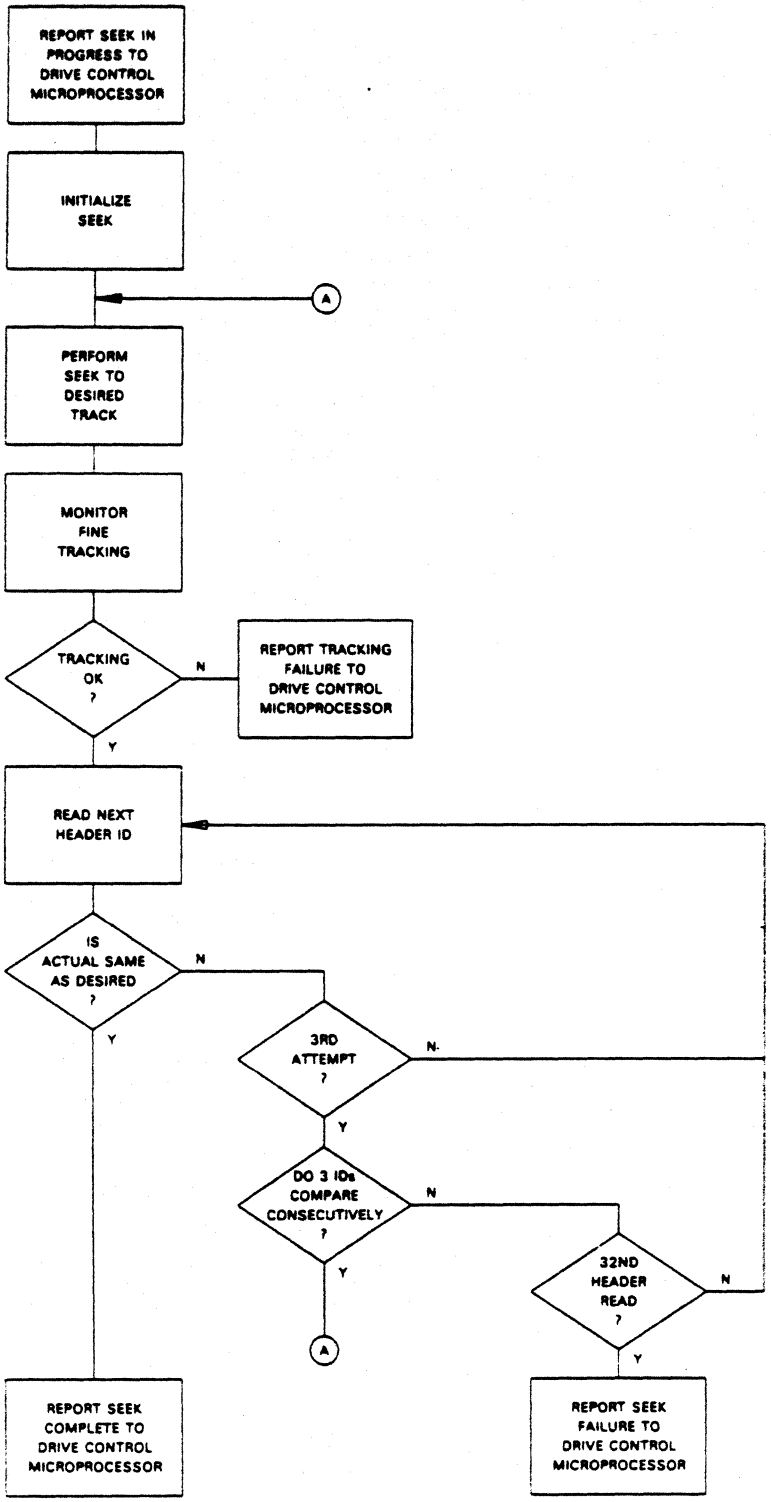
Figure 3-4. Quad Detector Tracking Signal

The Servo Control Microprocessor measures the time between the track crossing pulses to determine the average velocity of the FSM. This calculated velocity is compared against a desired velocity that is stored in ROM. The appropriate Seek Velocity Error Signal is then sent to a DAC on the Servo Systems PCA, to accelerate or brake the FSM as necessary (Seek Velocity Error Signal = calculated velocity - desired velocity). This pattern is followed until the FSM is within one-half track of the proper destination. At this time, the software switches from a velocity mode to a Seek Arrival Mode.

Once switched from a velocity mode, after a calculated delay from the Track Crossing Pulse, a 75-microsecond full braking current is supplied to the FSM to quickly slow it down. Twenty-five microseconds into this braking pulse from the DAC, the Tracking Servo Loop is allowed to lock onto the track. During the final 50 microseconds of the braking pulse, both the Seek Velocity Loop (microprocessor controlled) and the Fine Tracking Loop are closed to alleviate overshooting the desired track. The Seek Velocity Loop is opened after the 75-microsecond braking pulse, allowing the Fine Tracking Loop full control of the FSM.

When the FSM has arrived at the end of a Seek, Tracking Status is monitored by the Servo Control Microprocessor. Tracking status is determined by two comparators in the Tracking Status Circuitry that check the Tracking Error Signal (refer to figure 3-3). They determine if the status is within the required tracking thresholds. If not, Off Track Status is sent to the Servo Control Microprocessor and reports a Tracking Failure to the Drive Control Microprocessor, which then performs Tracking Error Recovery procedures.

Once the status is within the required tracking threshold, the Servo Control Microprocessor verifies that the Seek was made to the desired Seek address. The Reading Header status is also monitored. Refer to figure 3-5 for a simplified flowchart of Servo Control Microprocessor activity during a Seek.



ADP39

Figure 3-5 Servo Microprocessor Seek Flow Chart

When the actual track address and the desired track address are the same, a Seek Complete response is sent to the Drive Control Microprocessor. The Drive Control Microprocessor then reports the status to the ICI PCA.

The Seek is completed when the outcome of the Seek is reported to the ICI PCA. Appropriate actions are taken by the Servo/Drive Control PCA to continue Drive operation. The Servo Control Microprocessor continues to monitor error signal status to ensure Seek completions, and to verify that a stable tracking state exists.

3.3.2.3. Jumpbacks

Once a Seek is completed, the Drive Control Microprocessor maintains the current track by commanding the Servo Control Microprocessor to perform a Jumpback operation in the sector following the desired sector.

The ICI PCA may enable Jumpbacks when no Read, Write or Seek operations are in progress. With Jumpbacks enabled, and after passing the desired sector, the Drive Control Microprocessor requests a one track backward Seek. This compensates for the spiral track on the Media, making it appear to be concentric circles.

When the Host requests a Seek to Track 2/Sector 0 (figure 3-6), the Servo Drive Control PCA initiates a Seek to Track 2. At the end of the Seek, the Fine Servo Motor could be anywhere from Sector 0 to Sector 31 on Track 2. The Fine Servo Motor radially jumps back (or performs a Jumpback Operation) as follows:

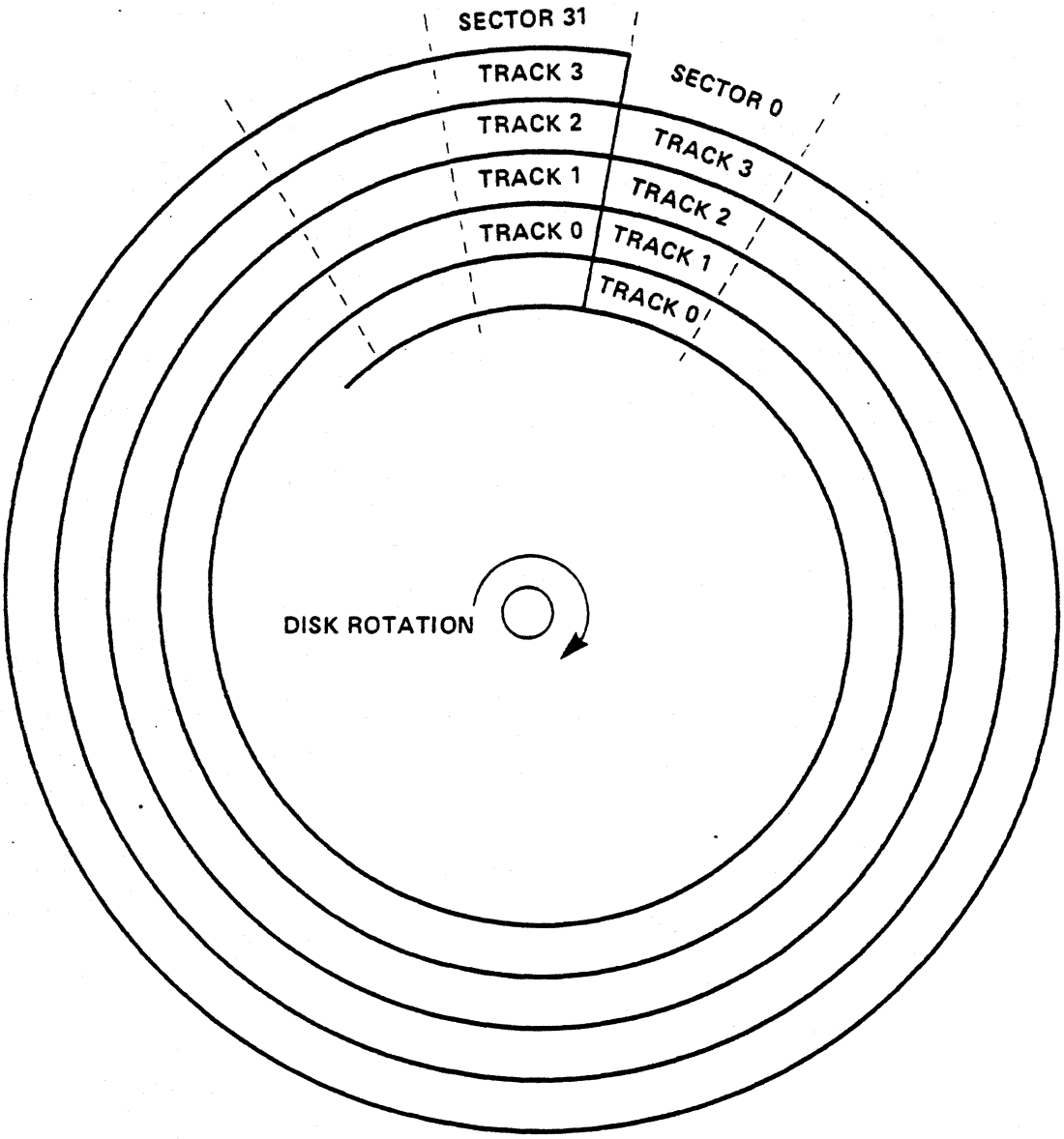


Figure 3-6. Jumpback Operation

PB002231-1

- When the actual sector is greater than the desired sector, but is not the last sector on the track, a Jumpback occurs immediately. Subsequent Jumpbacks occur one sector after the desired sector.

- When the actual sector is greater than the desired sector and is the last sector on the track, a Jumpback occurs when the desired sector plus one is reached on the next track.

- When the actual sector is less than or equal to the desired sector, a Jumpback occurs one sector after the desired sector.

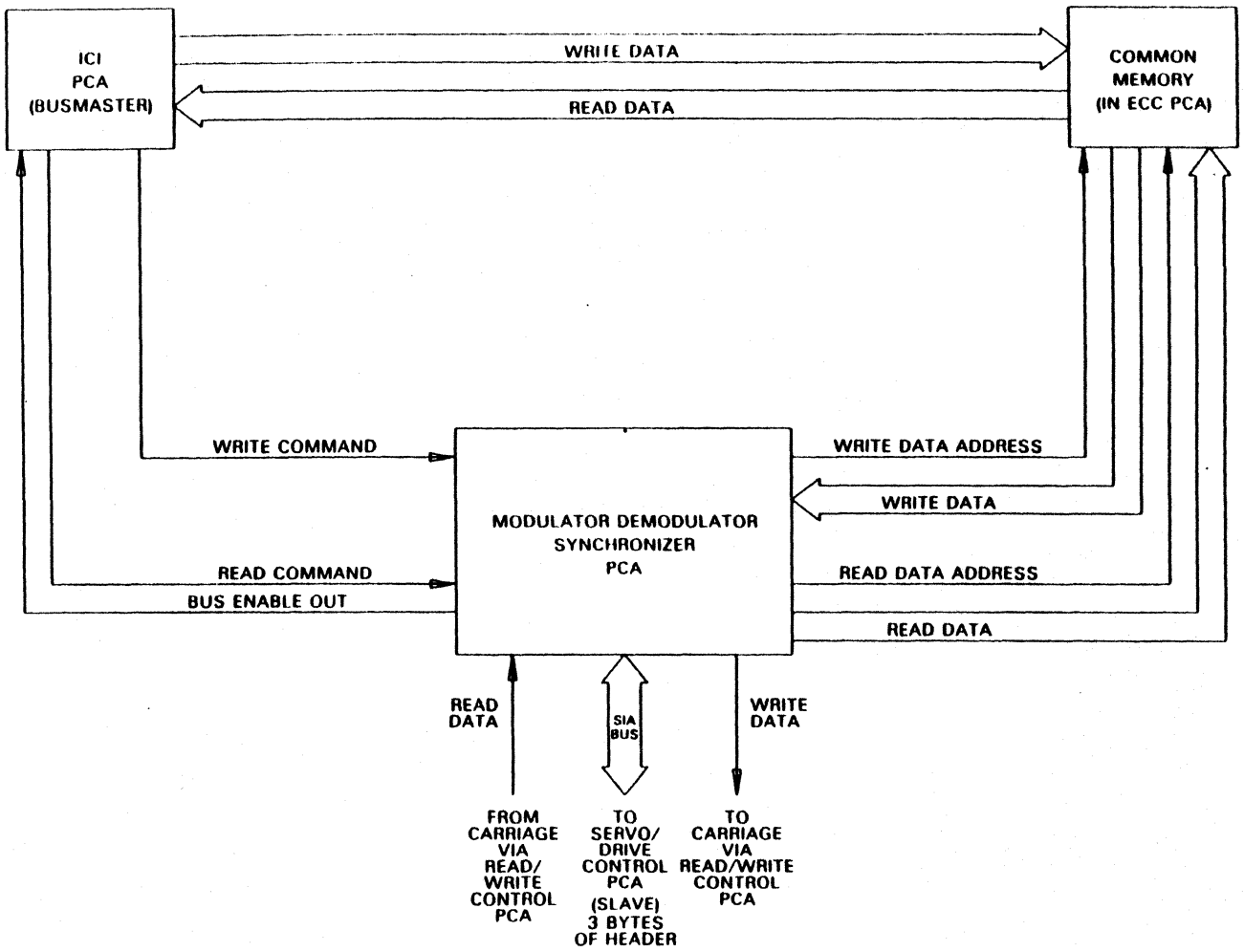
If the desired address is Track 0/Sector 1, a Jumpback occurs to Track -1/Sector 2. This is the only time the user is allowed access to a nonuser track.

3.3.3. Read/Write

The primary functions of the LD 1200 are to write data in the disk Media, and to read back data that has been written in the Media. At the LD 1200, Read and Write operations are performed on a per sector basis. A new command is sent to the Modulator Demodulator Synchronizer (MDS) PCA for each physical sector.

To request a Read or Write operation, the Host sends a command to the LD 1200 over the Small Computer System Interface (SCSI) Bus during an Information Transfer phase. (Refer to the Small Computer System Interface subsection in this manual for details on LD 1200 Commands and SCSI Bus protocol.) From the LD 1200 command, the ICI PCA in the LD 1200 generates a series of sector oriented Read/Write commands. (Refer to the Internal Device Interface subsection of this manual for details on Read/Write Commands and IDI Bus protocol.) These commands are then sent to the MDS PCA over the IDI Bus (refer to figure 3-7).

The sequence of events that occur within the LD 1200 during a Read/Write operation is shown in figure 3-8. The period of time defined by a physical sector is partitioned into two periods of activity. The first period, from Sector Mark to Sector Interrupt, is dedicated to MDS PCA overhead activity. The second period, from Sector Interrupt to next Sector Mark, is dedicated to the ICI PCA Command/Status Window. Data transfers overlap both activity periods. During the Command/Status Window, the MDS PCA interrupts ICI PCA activity on the IDI Bus for transfers of data.

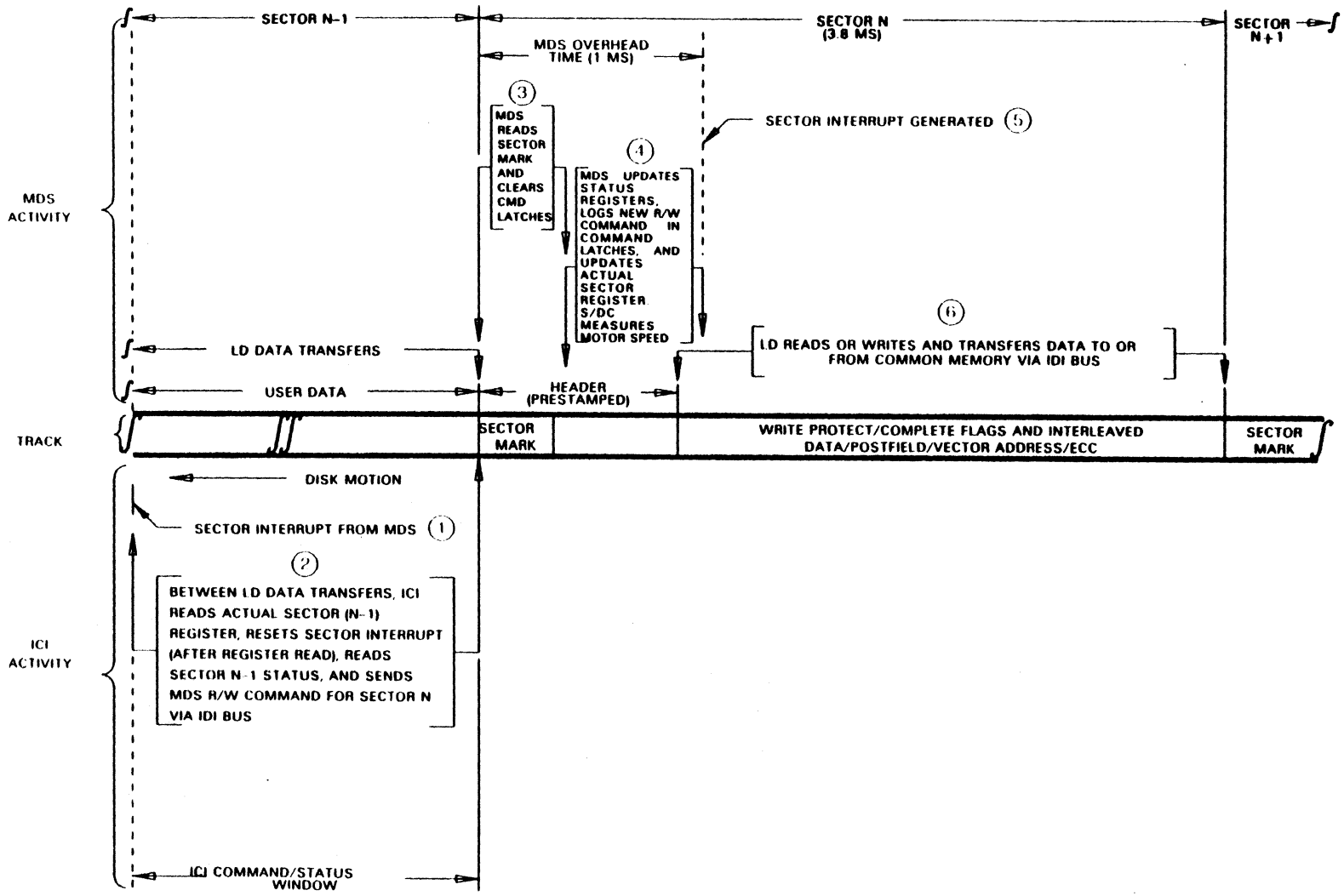


NOTE:

Commands, address, and data are transferred over the IDI bus.

ADP15

Figure 3-7. Read and Write Protocol Paths



NOTE

Circled numbers indicate sequence of events for one sector
ICI = Internal Controller Interface PCA
LD = LD 1200
MDS = Modulator Demodulator Synchronizer PCA
S/DC = Servo/Drive Control PCA

ADP16

The Read/Write operation sequence for a sector begins when a Sector Interrupt is sent from the Servo/Drive Control PCA to the ICI PCA. It is generated when the Servo/Drive Control PCA receives an active Read or Write Transfer Status from the MDS PCA. This interrupt indicates that valid sector status is available, and that the ICI PCA is authorized to send a Read/Write command for the next sector (Sector N in figure 3-8) to the MDS PCA. Between current sector data transfers, the ICI PCA:

- Reads Servo/Drive Control PCA status registers, which include MDS status. These registers contain status pertaining to both the current and previous sectors.
- Deactivates the Sector Interrupt by writing to the Clear Sector Interrupt Register in the Servo/Drive Control PCA.
- Sends the Read/Write command for the next sector.

At the beginning of the next sector (N), the MDS PCA decodes the Sector Mark and clears the Command Latches in the MDS PCA. Once the Sector Mark has been decoded, the LD 1200:

- Updates LD 1200 status registers
- Logs the new Read/Write command into the MDS command latches
- Measures Spindle Motor speed
- Updates the Actual Sector Register
- Activates the Sector Interrupt

During the MDS overhead activity period, data transfer via the IDI Bus begins. Header information is sent to the Servo/Drive Control PCA. User data is transferred between the MDS PCA and Common Memory on the ECC PCA (refer to figure 3-7).

On receipt of the Sector Interrupt, the ICI PCA reads sector status and sends the Read/Write command for the next sector (N+1). If a command is not sent, the LD 1200 goes into the Idle mode.

Detailed theory describing each of the functional blocks comprising the Read/Write Channel is provided in the Modulator Demodulator Synchronizer PCA and Read/Write Control PCA subsections of this manual. The following subsections describe the flow of Read and Write functions through the LD 1200 circuits.

3.3.3.1. Initialization

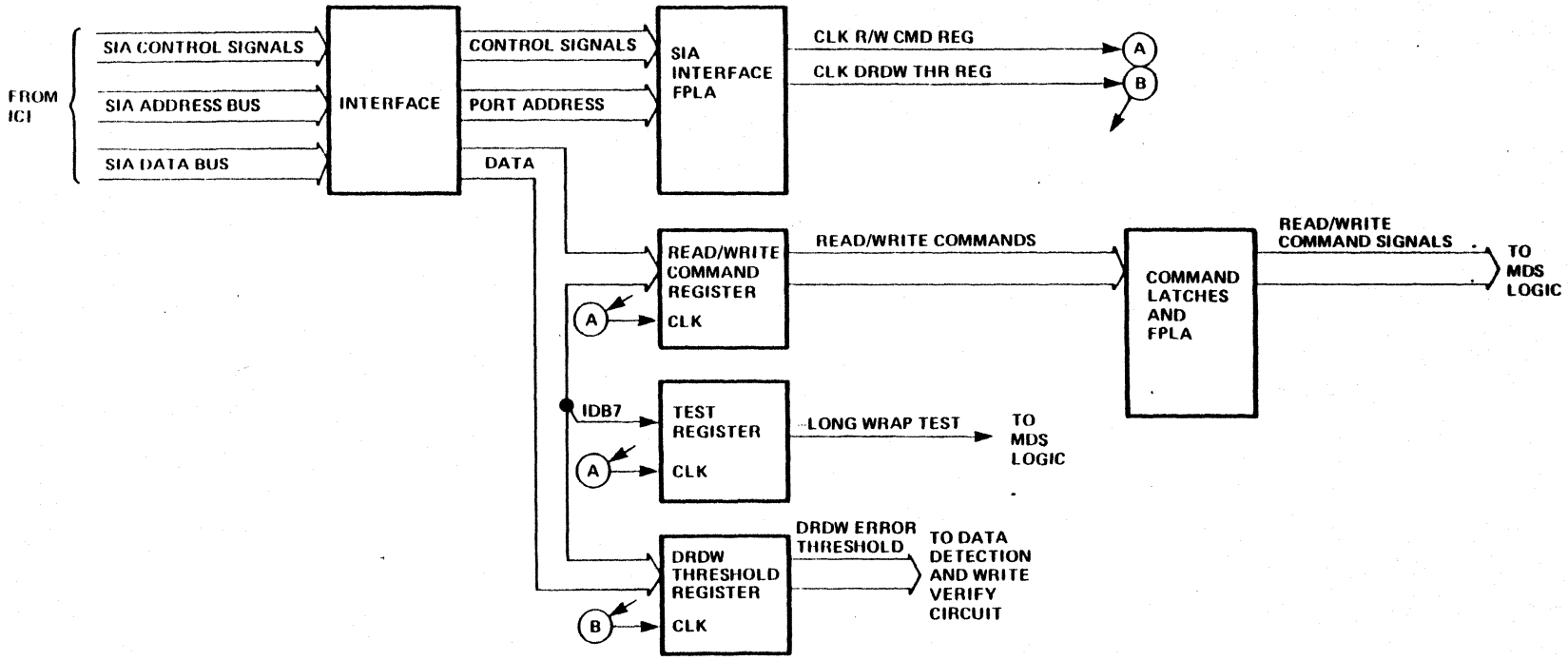
Before the LD 1200 can read or write data, the MDS PCA must be initialized. Initialization consists of loading Read/Write Control Registers during the Command/Status Window of the sector prior to the one where the Read or Write operation is to take place.

As shown in figure 3-9, SIA control signals, port address, and register data from the ICI PCA are applied to the SIA Interface in the MDS PCA. This logic produces a clock signal which steers the register data from the ICI PCA to the appropriate SIA Interface Register:

- Read/Write Command Register: Read or Write command for the next sector.
- Test Register: Long Wrap Test enable

- DRDW Threshold Register: (1) Maximum number of DRDW errors allowable in each field (user data, Vector Address, and Postfield) plus one. One indicates no errors are allowed. Zero prevents all writing in the sector. (2) Minimum number of bytes allowable for the sector to be classified as containing data.

The Read or Write command from the Read/Write Command Register is loaded (logged) into the Command Latches at the beginning of the sector where the operation is to be performed. An associated FPLA produces a Read or Write command signal which enables the MDS PCA to perform the specified operation.



LEGEND:

ICI Internal Controller Interface PCA
MDS Modulator Demodulator Synchronizer PCA

PB002344

Figure 3-9. Read/Write Initialization Path

3.3.3.2. Synchronization and Sector Identification

At the LD 1200, all Read and Write operations are sector oriented. The MDS PCA resynchronizes itself to the disk at the beginning of each sector.

Each disk sector is identified with prestamped header information which begins with a Sector Mark (refer to Surface Format subsection).

All Sector Marks are encoded with the same Two-Out-of-Nine (TOON) cell pattern, as shown in figure 3-92 in the Surface Format subsection). This coding scheme is different than that used for data TOON cells, which must be encoded with one hole in an odd monohole position and one in an even position to be recognized as valid data.

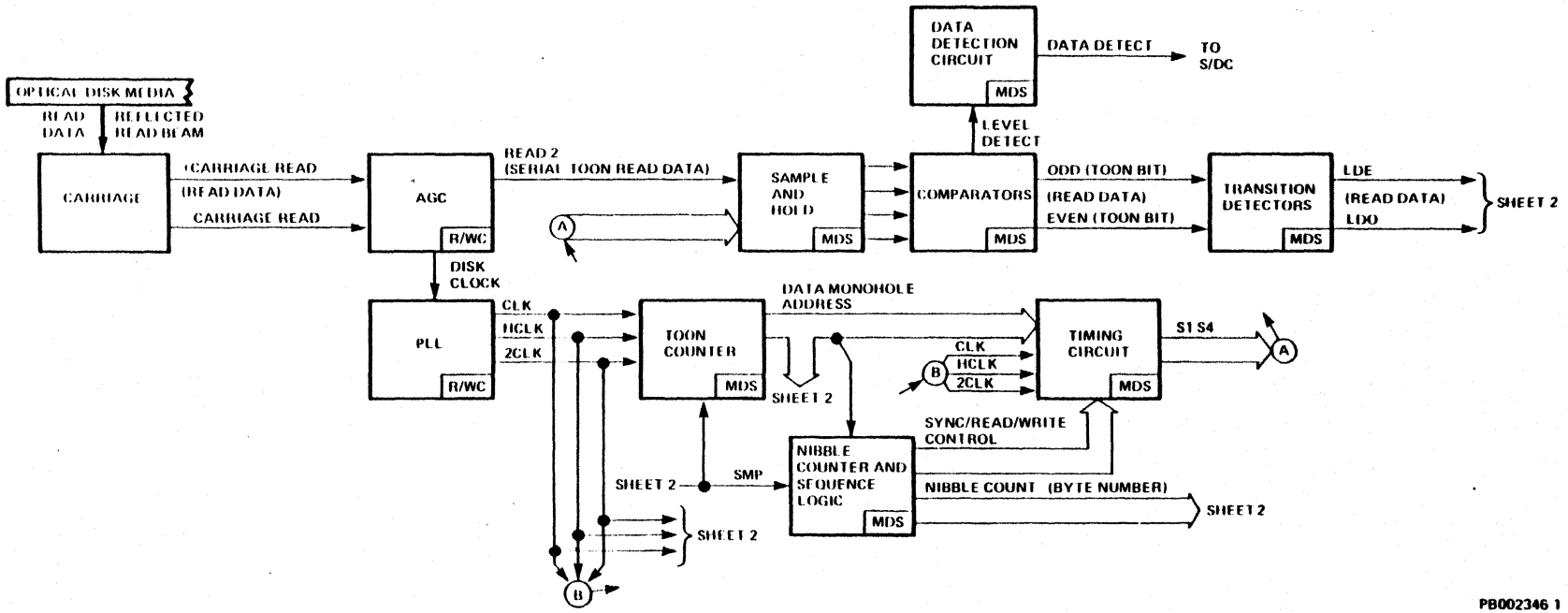
As shown in figure 3-10, the Sector Mark is read from the optical disk Media by the reflected read laser beam. The Carriage electronics convert the intelligence in the read laser beam to analog electrical signals +CARRIAGE READ and -CARRIAGE READ. These signals are routed to the Automatic Gain Control (AGC) on the Read/Write Control PCA.

The AGC stabilizes the gain of the read signal and produces two signals from it, disk clock and READ2. The disk clock is input to the Phase-Locked Loop (PLL) to synchronize MDS PCA timing with that of the disk. The PLL produces timing signals CLK, HCLK, 2CLK, and -2CLK, which provide the basic timing for the Read/Write Channel.

The PLL clocks drive the TOON Counter, which keeps track of the monohole positions in a TOON cell (nibble). At the end of each nibble, the TOON Counter increments the Nibble Counter with TNC3. The Nibble Counter keeps track of the nibbles in a sector. The nibble count is input to the Sequence Logic, which produces control signals to sequence the MDS PCA through the operations required to read or write during the sector.

The monohole address from the TOON Counter is input to the Timing Circuit to generate sample signals S1 through S4. These signals determine the sequence in which the Sample and Hold circuit samples READ2.

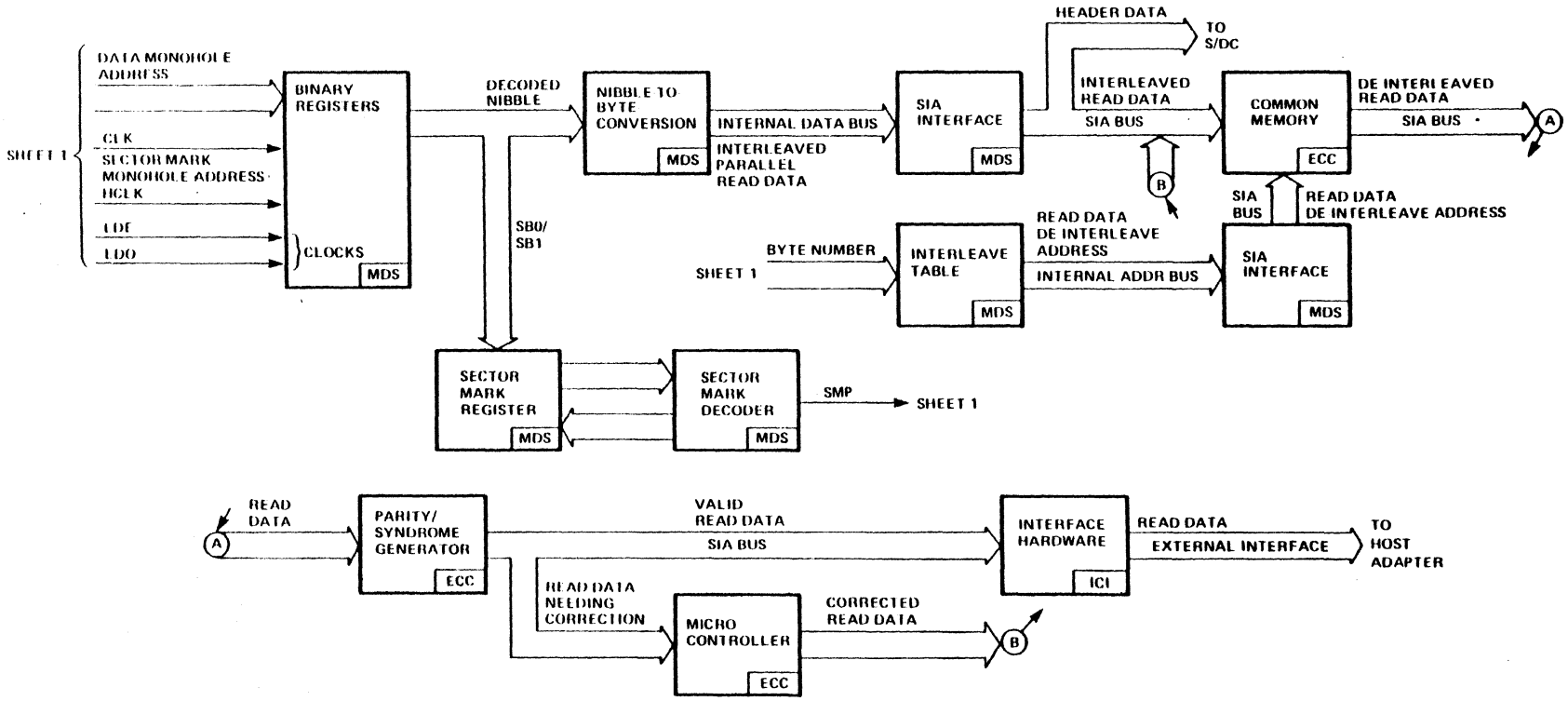
READ2, carrying Sector Mark monohole information read from the Media, is input to the Sample and Hold circuit. This circuit samples READ2 at each monohole position of the Media. The first sample is taken by S1 at position 1 of the first nibble in the Sector Mark and is held. Next, a sample is taken by S3 at position 2 and is compared with the one taken at position 1 by the Odd Comparator. Whichever sample has the higher signal level, that one is now held. Detection of a higher signal level, indicates the presence of a monohole in that position, making the ODD signal high. Next, position 3 is sampled and compared with the signal level held from the previous sample. The higher signal level from the current comparison is now held. This sampling process is repeated for four monohole positions, then the sampling sequence begins again with S1.



LEGEND

ECC	Error Correction and Common Memory Interface Unit PCA Function
ICI	Internal Controller Interface PCA
MDS	Modulator Demodulator Synchronizer PCA Function
R/WC	Read/Write Control PCA Function
S/DC	Servo/Drive Control PCA

Figure 3-10. Read Data Path
(Sheet 1 of 2)



LEGEND

ECC	Error Correction and Common Memory Interface Unit PCA Function
ICI	Internal Controller Interface PCA
MDS	Modulator Demodulator Synchronizer PCA Function
R/WC	Read/Write Control PCA Function
S/DC	Servo/Drive Control PCA

PB002346 2

Figure 3-10. Read Data Path
(Sheet 2 of 2)

Because the TOON-cell format of a Sector Mark differs from that of data, the addresses of the monoholes in the nibbles are specified by the phase relationships of the CLK and HCLK signals during Sector Mark decoding. As a monohole position is sampled, the associated HCLK/CLK address is applied to the inputs of the Odd Binary Register. The presence of a monohole in a position, is detected by the Odd Transition Detector, which produces the signal LDO. This signal clocks the address of the monohole into the Odd Binary Register, producing SB0 and SB1. These signals, which represent the monohole address, are input to the Sector Mark Register. The Sector Mark Register and Decoder decode the Sector Mark by recognizing a predetermined sequence of monohole addresses, and produce -SMP (Sector Mark Pulse).

The Sector Mark Pulse is the point to which all sector timing is referenced. This signal sets the TOON Counter to a known state, and initializes the Nibble Counter to begin counting at Nibble Count 8 (Nibble Counts 0 through 7 are the Sector Mark).

Once synchronization has been established, the LD 1200 continues the operation by reading the Sector Header, which consists of:

- Sector number (one byte)
- Track number LSB (one byte)
- Track number MSB (one byte)

READ2 is input to the Sample and Hold circuit, which now samples the signals relative to TOON data criteria, one even and one odd monohole per nibble. The first sample is taken by S1 at position 1 (odd) and is held. The next is taken by S2 at position 2 (even) and held. Next, a sample is taken by S3 at position 3 and is compared with the one taken at position 1. The sample that has the higher signal level, is held, indicating the presence of a monohole at that position. Detection of an odd monohole causes the ODD signal to go high.

The Odd Transition Detector detects the change in state of ODD and produces LDO (Load Data Odd). As each monohole position is sampled, the associated position address is generated by the TOON Counter and applied to the Binary Registers. When LDO goes high, indicating an odd monohole, it loads the position address into the Odd Binary Register, producing two binary bits of the decoded nibble.

Next, a sample is taken by S4 at position 4 and is compared with the one taken at position 2. The sample that has the higher signal level is held, indicating the presence of a monohole at that position. Detection of an even monohole causes the EVEN signal to go high. The Even Transition Detector produces LDE (Load Data Even) in response to the change in state of signal EVEN. LDE loads the address of the even monohole into the Even Binary Register, producing the remaining two bits of the decoded nibble. At this time, the decoding of one nibble is complete.

The next sample is taken with the sample signal associated with the lower of the two values previously compared. For example, if S3 had the higher signal value when compared with S1, S1 is used to take the next sample. Sampling continues in this manner until all the monohole positions in the nibble have been read.

The outputs of the Binary Registers, representing the decoded nibble, are input to the Nibble-to-Byte Conversion circuit which converts them to an eight-bit byte. The Header bytes are sent to the SIA Interface for transfer to the SIA Bus in byte serial form.

Control signals from the Write Logic cause the SIA Interface to request an I/O data transfer over the SIA Bus. The Interleave Table generates the port addresses of the Servo/Drive Control registers to which the header information is to be sent. When the MDS PCA gains control of the SIA Bus, the Sector Header information is transferred to the Servo/Drive Control PCA.

3.3.3.3. Read Data Operation

At the LD 1200, a Read operation consists of:

(1) Initializing the MDS PCA

(2) Synchronizing the MDS PCA to the beginning of the sector

(3) Reading the Sector Header to identify the sector

(4) Reading the data from the User Data Field

The User Data Field of a sector on the Media contains the following information written in TOON format:

(1) Write Protect Flags for User Data, Vector Address, and Postfield fields

(2) User Data, Vector Address, Postfield, and associated ECCs interleaved

(3) Write Complete Flags for User Data, Vector Address, and Postfield fields

As shown in figure 3-10, data is read from the Media, processed by the Read/Write circuits, and routed to the TOON decoding circuits. This process is further described in the Synchronization and Sector Identification subsection of this manual.

When comparison of two even samples indicates the presence of a monohole, LEVEL DETECT goes high and is sent to the Data Detection Circuit. This circuit includes a threshold counter, which is preset to a value representing the minimum number of bytes allowable in a sector for that sector to be classified as containing data. Each valid byte decoded decrements the counter by one. When the preset value has been reached, DATA DETECT is sent to the Servo/Drive Control PCA, indicating that the current sector contains data.

Serial read data from the Media is converted to parallel data bytes and routed to the SIA Interface. Control signals from the Write Logic request a memory data transfer over the SIA Bus. As each byte of read data is placed on the SIA Data Bus, the Interleave Table places the associated de-interleave Common Memory address on the SIA Address Bus. When the MDS PCA gains control of the SIA Bus, the data byte on the bus is transferred to Common Memory on the ECC PCA and stored at the location specified by the associated address.

On request of the ICI PCA, the data is fetched from Common Memory and input to the Parity/Syndrome Generator on the ECC PCA. In this circuit, ECC syndromes (check characters) are generated from the data read from the Media. These syndromes are then compared with the ECC characters read from the Media. If the two match, the data requires no correction and is sent over the external interface bus to the Host Adapter. If the syndromes and ECC characters do not match, the data requires correction and is sent to the Microcontroller on the ECC PCA. If possible, the data is corrected by the Microcontroller and sent to the Host Adapter.

3.3.3.4. Write Data Operation

At the LD 1200, a Write operation consists of:

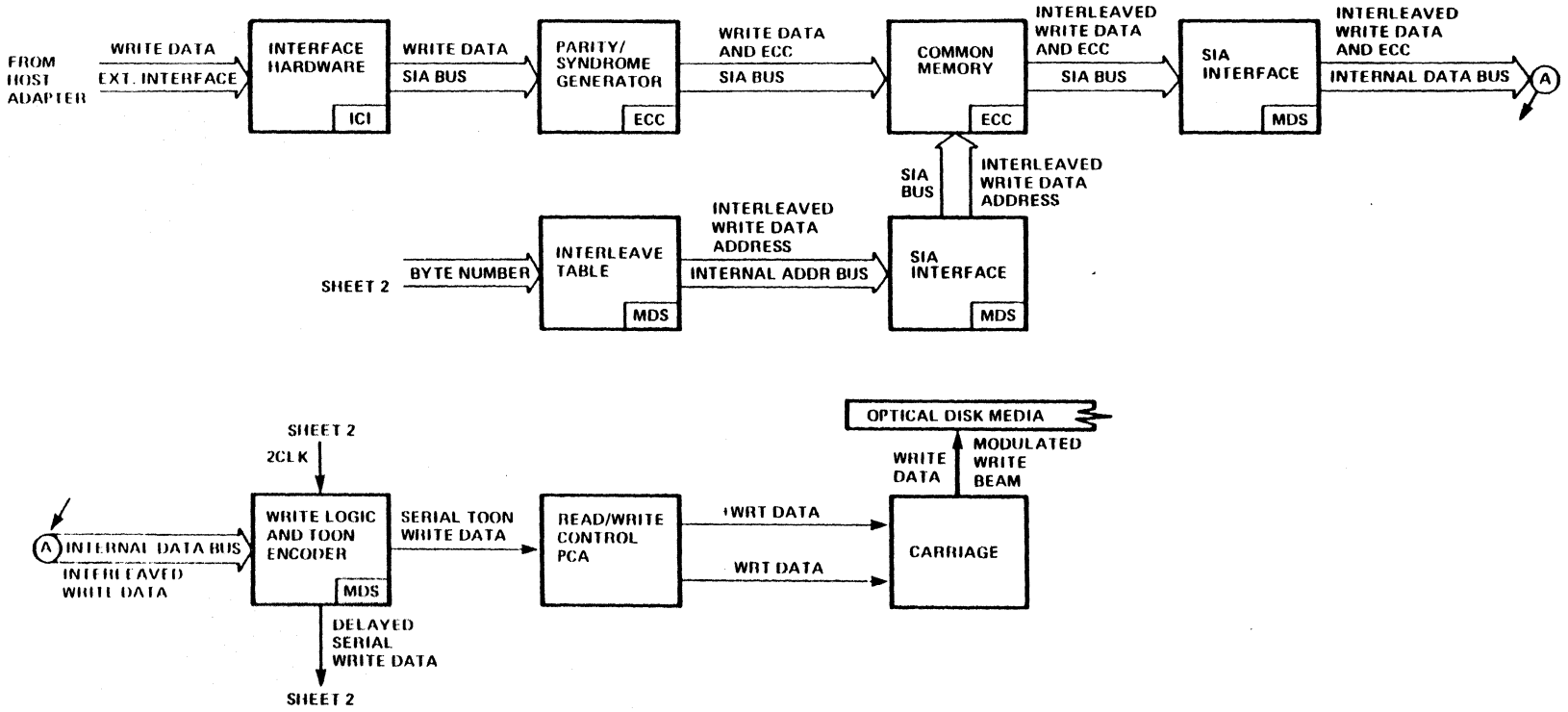
- Initializing the MDS PCA
- Synchronizing the MDS PCA to the beginning of the sector

- Reading the Sector Header to identify the sector
- Writing data in the Data Field of the sector
- Verifying the writing of each data monohole through Direct Read During Write (DRDW)

The Sector Header on the disk is a read-only area. The LD 1200 never writes in this area. The Data Field is both a read and write area.

As shown in figure 3-11, data to be written on the disk is transferred from the Host Adapter to the LD 1200 ICI PCA over the external interface bus. From the Interface Hardware, the data is input to the Parity/Syndrome Generator on the ECC PCA. This circuit generates ECC characters for User Data, Vector Address, and Postfield and appends them to the data. The write data and ECC characters are then loaded into Common Memory on the ECC PCA.

The MDS PCA establishes synchronization with the beginning of the sector to be written in, as described in the Synchronization and Sector Identification subsection. Once synchronization is achieved, the Write command supplied by the ICI PCA during initialization is converted into write control signals by the Write Logic.

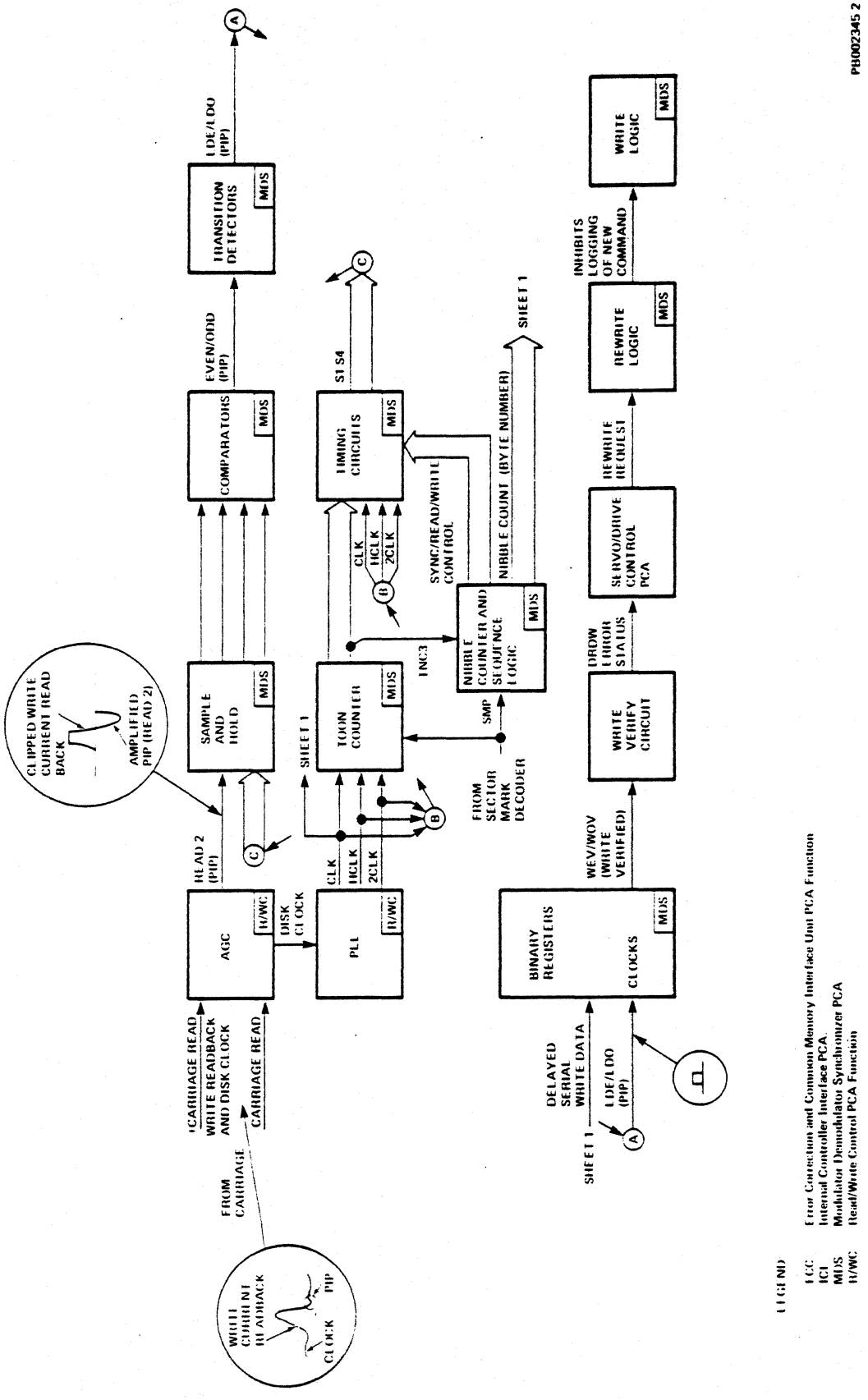


LEGEND:

ECC Error Correction and Common Memory Interface Unit PCA
ESG Error Signal Generator PCA
ICI Internal Controller Interface PCA
R/WC Read/Write Control PCA
S/DC Servo/Drive Control PCA

PB002345 1

Figure 3-11. Write Data Path
(Sheet 1 of 2)



LEGEND

ECC	Error Correction and Common Memory Interface Unit PCA Function
ICI	Internal Controller Interface PCA
MDS	Modulator Demodulator Synchronizer PCA
R/WC	Read/Write Control PCA Function

Figure 3-11. Write Data Path
(Sheet 2 of 2)

Control signals from the Write Logic are applied to the SIA Interface logic to request a memory data transfer from Common Memory. The Nibble Counter generates a count which identifies the first byte to be written by the current Write operation. This count is used to address the Interleave Table, which produces the Common Memory address of the location containing the data to be written. The interleave algorithm in the Interleave Table enables the data to be transferred from Common Memory in a sequence that interleaves the bytes on the Media. This address is placed on the SIA Address Bus and sent to Common Memory. When the MDS PCA gains control of the SIA Bus, a data byte is transferred from the addressed location in Common Memory to the MDS PCA.

Write data is received from Common Memory, one byte per transfer. From the SIA Interface, the write data is routed to the TOON Encoder. In the TOON Encoder, the data byte from two four-bit nibbles is converted to two 9-position TOON cells. The TOON cells are then sent to the Read/Write Control PCA in a serial bit stream.

When a write data signal is generated by the Write Logic and TOON Encoder, it sends a delayed write signal to the Binary Registers. This signal indicates that write data was sent to the Media, therefore a write readback PIP is expected on Read Data line READ2.

On the Read/Write Control PCA, the digital write data is converted to analog write pulses and sent to the Carriage. On the Carriage, the write pulses are used to modulate the Write laser beam which writes the data monoholes in the Media.

As a data monohole is melted in the Media, the light absorbed by the trailing edge of the forming hole causes a drop in the reflected write current readback signal which is called a PIP. The preamplifier on the Carriage clips the extreme positive swing of the write current readback signal and amplifies the PIP. The readback signal, including PIP, is sent from the Carriage to the Read/Write Control PCA on the ±CARRIAGE READ lines. The PIP is sent to the MDS PCA as READ2 and is processed as read data, resulting in the generation of LDE or LDO. LDE/LDO clocks the delayed write data signal into the Binary Registers generating WEV or WOV (Write Even or Odd Verified) high.

The absence of a PIP causes WEV and WOV to remain low, which allows the DRDW Threshold Counter in the Write Verify Circuit to be clocked. This counter is preset with a value representing the maximum number of DRDW errors allowable in a sector. Each time the counter is clocked, it decrements by one. When the DRDW Threshold Counter is decremented to zero. DRDW Error Status is sent to the Servo/Drive Control PCA.

When an error status is received, the Servo/Drive Control PCA, if so enabled, can request a retry of the Write operation being attempted. The Rewrite Request Signal is sent to the Rewrite Logic in the MDS PCA. This circuit prevents the new Read/Write command in the Read/Write Command Register from being logged into the Command Latches in the Write Logic. When the MDS PCA is synchronized to the next sector, the previous Write command (still in the Command latches) is executed to retry the Write operation.

3.3.4. Error/Fault Handling

The LD 1200 has both data error detection/correction capabilities and machine error/fault handling capabilities. The Internal Controller in the LD 1200 includes an error correction code circuit (on the ECC PCA) for the detection of data errors during Read operations with the Drive. This circuit is also used to correct data fields if the error falls within the correction capabilities of the circuit. The error correction circuit is based on a Reed-Solomon error correction code, enabling it to detect and correct both random bit and multiple burst errors that occur within a given sector. This circuit can correct at least 10, and up to 50, independent byte errors in the User Data Field of a given physical sector.

LD 1200 malfunctions are initially reported in the Completion status Byte that is sent to the Host on completion of a command. A malfunction causes termination of the command and indication of a Check Condition in the Completion Status Byte. (Refer to the Small Computer System Interface subsection in this manual for more information on the Completion Status Byte.)

LD 1200 malfunctions are classified as either errors or faults (refer to tables 3-8 through 3-10 in the Internal Device Interface/System Interface Assembly Bus subsection). The term error refers to any abnormal condition that occurs during normal operation of the LD 1200. Because it is possible for intermittent errors to occur, from which recovery is possible, further testing is performed before an error is declared permanent, that is a fault. In most cases, the LD 1200 automatically performs testing and recovery algorithms on detection of an error.

Errors are indicated in the Error Registers, on the Servo/Drive Control PCA, and can be read by the Internal Controller via the IDI Bus. Before the Drive enters the Ready state, all error bits are made high (set). They remain high, even when the error condition is corrected, until cleared by the Internal Controller. After the Drive enters the Ready state, some of the errors are cleared before the next sector begins and some remain high until cleared by the Internal Controller.

Generally, if an error occurs during a Write operation to the Media, the operation is halted immediately, and remains so until the problem is resolved. For certain errors, if the problem is resolved by the start of the next sector, a Rewrite operation is attempted. If not, a recovery algorithm is initiated. If the recovery algorithm fails to resolve the problem, a fault is declared.

Most errors do not cause the termination of a Read operation. In this case, the error correction circuitry in the LD 1200 is used to maintain data integrity.

The term fault refers to a malfunction from which the LD 1200 cannot recover. In most cases, a fault is declared only after all attempts to recover from an error that has occurred have failed. Due to their nature, some malfunctions are immediately declared faults, with no attempt made to recover from them.

Faults are indicated in the Fault Registers, on the Servo/Drive Control PCA, and can be read by the Internal Controller via the IDI Bus. When a fault occurs, all ongoing LD 1200 operations are halted and the fault is reported to the Host. The Drive automatically shuts off the Laser read and write power, defocuses the laser beam, and retracts the Carriage to the Home position. The Drive remains in this mode of operation until the fault has been cleared by the Host and a new command is issued to the LD 1200.

Drive (device) malfunctions are detected by diagnostic circuits in the Drive and are reported to the Error and Fault Registers on the Servo/Drive Control PCA. The contents of these registers are read by the Internal Controller and passed to the Host, along with additional error, fault, and status information, in Device Status, Error Status, and Fault Code Bytes. LD 1200 errors, faults, and status conditions which predict possible malfunctions are shown in table 3-1.

In table 3-1, malfunctions reported by the LD 1200 are listed in the leftmost column. To the right of a given malfunction are columns indicating where and how it is reported in the subsystem. For example, on the fourteenth line of the table, Phase-Locked Loop (PLL) is listed. To the right of this malfunction, there are Xs in all the columns, indicating:

- Second Column: A PLL Error is reported in LD 1200 Internal Controller status as a Device Error. If the LD 1200 fails to correct the error, it becomes a fault and is reported as a Device Fault status.

- Third Column: A PLL Error is reported to the LD 1200 Internal Controller as a PLL Error.

- Fourth Column: A PLL Fault is reported to the LD 1200 internal Controller as a PLL Fault.
- Fifth Column: A PLL Error is reported to the Host in Device Status as a Device Error. A PLL Fault is reported to the Host in Device Status as a Device Fault.
- Sixth Column: A PLL Error is reported to the Host in Error status as a PLL Error.
- Seventh Column: A PLL Fault is reported to the Host in a Fault Code byte as a PLL Fault.

The LD 1200 malfunctions listed in table 3-1 are described in more detail in the following subsections. The status structure used to communicate this information within the LD 1200 and to the Host is described more fully in the Interfaces subsection.

Table 3-1. Reported LD 1200 Errors and Faults

TYPE OF MALFUNCTION OR CONDITION	WHERE REPORTED					
	LD 1200 INTERNAL CONTROLLER			HOST		
	STATUS	ERROR	FAULT	DEVICE STATUS	ERROR STATUS	FAULT CODE
DRDW Error	X[2]	X		X[2]		
Track Miscompare Error	X[2]			X[2]	X	
Missing Data Field Error	X	X				
Power Supply Overtemperature	X			X		
Card Rack Overtemperature	X			X		
Laser Read Power Error/Fault	X[2,3]	X	X	X[2,3]	X	01
Laser Write Power Error/Fault	X[2,3]	X	X	X[2,3]	X	02
Quad Sum High Fault	X[3]		X	X[3]		03
Verify Header Error/Fault	X[2,3]	X	X	X[2,3]	X	04
Motor Speed Fault	X[3]		X	X[3]		05
MPU Timeout Fault	X[3]		X	X[3]		06
MPU Self-Test Fault	X[3]		X	X[3]		07
Wobble Error/Fault	X[2,3]	X	X	X[2,3]	X	08
PLL Error/Fault	X[2,3]	X	X	X[2,3]	X	09
Focus Error/Fault	X[2,3]	X	X	X[2,3]	X	0A
Seek Error Fault	X[2,3]	X	X	X[2,3]	X	21/0B
Tracking Error/Fault	X[3,3]	X	X	X[2,3]	X	0C
Line Sync Fault	X[3]		X	X[3]		0D
Data Synchronization Error/Fault	X[2,3]	X	X	X[2,3]	X	0E
Quad Sum Low Fault	X[3]		X	X[3]		0F
Illegal Operation Code						22
Invalid Logical Unit Number						23
Illegal Seek Address						24
Illegal Command Descriptor Block Parameter						25
End of Media Reached						28
Illegal Transfer Length						29
SCSI I/O Parity Error						41
Unable to Read Data[1]						43
Logical Block Address Not Found						44
Unable to Write Data[1]						63
Internal Parity Error						65
S/DC Parity Error	X[2]	X		X[2]	X	65
MDS Parity Error	X[2]	X		X[2]	X	65
ECC Fault						66
Voltage Fault						67
Invalid Bootstrap Load Error						69
Laser Degraded				X		6B
Power-Up Diagnostics Aborted						A5
Diagnostic Fault Detected						A6
Illegal Sequence (Device Not Ready)						C1
Write Protected Device Error						C2
Data Field Overwrite Error						C6
Empty Sector Detected						E5
Device Error	X[2]			X[2]		E6

1 These statuses result from the detection of other errors
2 Reported in status as a Device Error
3 Reported in status as a Device Fault

3.3.4.1. Direct Read During Write

A DRDW Error is indicated when more than the allowable number of DRDW errors have been detected during the writing of the previous sector. When the DRDW threshold is reached, the Write operation is terminated. If there were no other errors and Rewrite operations have been enabled by the Internal Controller, the Drive automatically attempts to rewrite the data in the next sector in sequence. When a Rewrite is to occur, the Internal Controller does not have to retransmit the command that was not completed successfully. The Drive retains and re-executes the command.

Any error that inhibits writing to the Media can cause a DRDW Error as well. This occurs because the DRDW circuitry continues to search for errors after the laser is inhibited. Because no monoholes are written during this time, the error threshold may be exceeded.

3.3.4.2. Track Miscompare Error

A Track Miscompare Error is indicated when the Drive detects a miscompare between the internally calculated track least-significant byte and the lower byte of the track address read from the Media. This error can occur during Read or Write operation with the Media only. If a Track Miscompare Error is detected during a Write operation and no data has been written in the affected sector, the operation is inhibited.

A Track Miscompare Error indicates a momentary loss of header information due to a Media flaw in the Sector Header. If this error occurs at a particular Media location repeatedly during Read operations, the information in that sector should be relocated before the Media degrades further. Repeated Track Miscompare Errors may be due to a track positioning error which may be corrected by a Reseek.

3.3.4.3. Missing Data Field Error

A Missing Data Field Error is indicated when an attempt is made to write a Postfield Byte in a sector which does not contain a previously written Data Field Write Protect Byte.

3.3.4.4. Power Supply Overtemperature

This status indicates that the overtemperature sensor in the LD 1200 Power Supply detected an overtemperature condition. All Internal Controller operations must be completed within 1 second of receiving this status, because the Power Supply automatically shuts down at the end of that period. This status acts as an early warning to the Internal Controller, which should shut down the Spindle Motor until the problem is corrected.

3.3.4.5. Card Rack Overtemperature

This status indicates that the overtemperature sensor in the LD 1200 Card Rack detected an overtemperature condition. All Internal Controller operations must be completed within 1 second, and the Internal Controller should not issue any new commands to the Drive as long as this condition is present. This status acts as an early warning to the Internal Controller, which should shut down the Spindle Motor until the problem is corrected. If the condition worsens, the LD 1200 automatically powers down.

3.3.4.6. Laser Read Power Error/Fault

A Laser Read Power Error is indicated when the Drive detects that the laser read power is too high or too low. Laser read power and write power are disabled and the Carriage is retracted to the Home position. The Drive attempts to regain proper read power level while the Carriage is in the Home position. If the Drive is successful, a Seek is performed to the track where the error occurred. The Internal Controller issues appropriate command information to continue the operation that was interrupted. If recovery is not possible, a Laser Read Power Fault is declared. This fault indicates that the Laser Diode is nearing the end of its useful life, or that there is a malfunction in the Power Control Loop circuitry (on the Read/Write Control PCA).

3.3.4.7. Laser Write Power Error/Fault

A Laser Write Power Error is indicated when the Drive detects that the laser write power is too high or too low. Laser write power and read power are immediately disabled and the Carriage is retracted to the Home position. The Drive attempts to regain the proper power level while the Carriage is in the Home position. If the Drive is successful, a Seek is performed to the track where the error occurred. The Internal Controller issues appropriate command information to continue the operation that was interrupted. If recovery is not possible, a Laser Write Power Fault is declared. This fault indicates that the Laser Diode is nearing the end of its useful life, or that there is a malfunction in the Power Control Loop circuitry (on the Read/Write Control PCA).

3.3.4.8. Quad Sum High Fault

A Quad Sum High Fault indicates that the Quad Sum signal has exceeded its allowable upper limit. The Drive immediately turns off all laser read and write power and inhibits the tracking and focus circuitry when this fault is detected. If the Quad Sum High Fault signal goes high, the Laser Read and Write Power Fault signals also go high. If both the Laser Read and Write Power Fault signals go high and the Quad Sum High Fault signal remains low, a faulty Sense Diode in the Drive Quad Sum network is indicated.

3.3.4.9. Verify Header Error/Fault

A Verify Header Error is indicated when the Drive is unable to verify the track address values from the headers read from the Media as part of a normal Seek routine. The Drive must verify three consecutive track/sector values on the target track or this error is indicated. This error indicates the Media is defective in the affected area and should be avoided by the user. If this error occurs during a Write operation, the Drive inhibits laser write power. Otherwise, the LD 1200 takes no corrective action after a Verify Header Error is reported.

When the Drive is unable to verify the track address portion of the Sector Header while attempting a Seek to Track 0, a Verify Header Fault is declared. This fault can occur only during Drive initialization or error recovery procedures. The Verify Header Fault indicates the Media is unusable by the Drive and must be replaced.

3.3.4.10. Motor Speed Fault

A Motor Speed Fault indicates that the Spindle Motor speed is out of tolerance (more than 2.5% lower or higher than allowed). A Motor Speed Fault is also declared if the Spindle Motor does not attain the proper speed within 3 seconds of a Spindle Power Up command.

3.3.4.11. MPU Timeout Fault

An MPU Timeout Fault indicates that the timeout circuit in the Drive has detected a probable hang-up condition in one of the microprocessors (MPUs). A special timer for each MPU in the Drive is reinitialized periodically by the MPU when it is operating normally. Should the microprogram hang up or become lost or an MPU malfunction, the timer times out alerting the Internal Controller.

3.3.4.12. MPU Self-Test Fault

An MPU Self-Test Fault indicates that one of the MPUs in the Drive has detected a failure during the execution of one of its self-tests. Self-tests are performed during LD 1200 Power Up and Drive Reset operations.

3.3.4.13. Wobble Error/Fault

A Wobble Error is indicated when the Drive has detected errors in reading the servo wobble bytes for two or more consecutive sectors. Wobble bytes are used to ensure proper centering of the laser beam in the spiral track on the Media. If this error is detected during a Write operation, the operation is aborted. The affected area of the Media indicated by this error must be avoided by the user. No relocation action is performed by the LD 1200.

A Wobble Fault indicates the Drive is unable to properly read wobble bytes during initialization or error recovery. This fault indicates that the Media is unusable by the Drive and must be replaced.

3.3.4.14. Phase-Locked Loop Error/Fault

A PLL Error is indicated when the PLL in the Drive has lost, and has been unable to regain, synchronization with the preformatted disk clock for 30 microseconds or more. If this error occurs during a Write operation, the operation is inhibited. When the error is cleared, the Drive attempts to perform Rewrite operations, if Rewrites are enabled. If synchronization is not regained within a specified length of time (approximately 5 sectors), the Drive initiates a recovery algorithm. If use of the algorithm does not resolve the problem, a PLL Fault is declared. This indicates the PLL circuit is unable to obtain synchronization with the disk clock from the Media.

3.3.4.15. Focus Error/Fault

A Focus Error is indicated when the Drive is unable to keep the laser beam focused on the Media. If this error occurs during a Write operation, the operation is aborted. If the error is resolved within 1 millisecond, the Internal Controller may clear the error and continue the operation. If the error is not resolved within that time, a recovery algorithm is initiated by the Drive, which includes three attempts to focus the laser beam at the present Carriage location, followed if necessary by a Carriage Retract to the Home position and up to three attempts to focus the laser beam at that location. If the recovery process is unsuccessful, a Focus Fault is declared. If the recovery is successful, the Drive performs a Seek to the track where the error occurred. The Internal Controller then continues the original operation and reports the error to the Host at the termination of the Command Block.

3.3.4.16. Seek Error/Fault

A Seek Error is indicated when the Drive is unable to successfully complete a Seek operation requested by the Internal Controller. A successful Seek involves resynchronization to the Sector Marks read from the Media and proper validation of at least one Header Address. If a Seek is unsuccessful, the Drive attempts two local Seeks to locate the requested track, then declares a Seek Error. If the Drive successfully Seeks to the desired track during one of the local Seeks, the Internal Controller continues the operation and makes the Seek Error status available, where it can be monitored by the Host at the termination of the command. If the Drive is unsuccessful, the operation is aborted and the error is reported as a Check End status.

When the Drive is unable to perform a Seek to Track 0 as part of initialization or an error recovery procedure, a Seek Fault is declared. A Seek Fault can also be declared if the Drive is unable to perform a Carriage Retract operation.

3.3.4.17. Tracking Error/Fault

A Tracking Error is indicated when the servo circuitry in the Drive has allowed the Carriage to drift off-track. If this error occurs during a Write operation, the Drive terminates the operation and initiates a recovery algorithm. This algorithm includes an attempt to regain tracking at the present Carriage position followed if necessary by Carriage Retract to the Home position and an attempt there to initialize tracking. If all recovery attempts fail, a Tracking Fault is declared. If the recovery process is successful, the Drive performs a Seek to the track where the error occurred. The Internal Controller can then continue the original operation and report the error to the Host at the termination of the Command Block.

3.3.4.18. Line Sync Fault

A Line Sync Fault indicates that the LD 1200 Power Supply has detected the loss of at least two consecutive ac supply input cycles. When this fault occurs, the operation currently in progress (Read or Write) is aborted at the next Sector Mark and a Carriage Retract is performed. If a Seek operation is in progress when the fault occurs, the Seek is aborted and the Carriage is retracted. Host recovery from this fault (when possible) is essentially the same as the Power-Up Start procedure.

This fault is also reported to the Host in Manual Intervention Status as a Voltage Fault. Total loss of power may make it impossible for the LD 1200 to report this fault because dc reserves may not provide enough time for error reporting to the Host.

3.3.4.19. Data Synchronization Error/Fault

A Data Synchronization Error is indicated when the Drive has detected a loss of synchronization with respect to the serial data to or from the Media. The Drive monitors the four-byte Sector Mark, read from the Media at the beginning of each sector, to ensure that synchronization is maintained. If a Data Synchronization Error is detected during a Write operation, the operation is inhibited. If Rewrites are enabled by the Internal Controller, and the data synchronization problem has been resolved before the beginning of the next sector, the Drive attempts a Rewrite operation in the next sector. If recovery from the error does not occur, the Drive initiates a Resynchronization routine at the Carriage Home position. If all attempts at resynchronization fail, a Data Synchronization Fault is declared.

3.3.4.20. Quad Sum Low Fault

A Quad Sum Low Fault indicates that the Quad Sum signal has fallen below its allowable lower limit. The Drive immediately turns off all laser read and write power and inhibits the tracking and focus circuitry when this fault is detected.

3.3.4.21. Illegal Operation Code

This condition is reported whenever the LD 1200 receives an Operation Code that is not defined in the firmware. This code is also used if the Host sends a Spindle Power-Up or -Down command when the START/STOP switch is in the Stop position.

3.3.4.22. Invalid Logical Unit number

This condition is reported in conjunction with a Not Ready Sense Key in response to a command received with a Logical Unit Number other than zero.

3.3.4.23. Illegal Seek Address

This condition is reported whenever the LD 1200 receives a Command Descriptor Block with a Seek Address that is outside the range of addresses allowed.

3.3.4.24. Illegal Command Descriptor Block Parameter

This condition is reported whenever the LD 1200 receives a Command Descriptor Block that is illegal for the Operation Code specified.

3.3.4.25. End of Media Reached

This condition may be reported only during device data transfer operations and indicates that the Seek address has been incremented to its maximum value. The LD 1200 will not transfer data beyond the physical end of the Media. This code does not necessarily indicate an error condition unless the Host did not anticipate the end of the Media.

3.3.4.26. Illegal Transfer Length

This condition is reported when the LD 1200 receives a Command Block with a Transfer Length and Logical Block Address that specify a data transfer which extends beyond the end of the Media.

3.3.4.27. SCSI I/O Parity Error

This error is reported when the LD 1200 receives a word from the Host over the SCSI Bus with an invalid Parity bit. All SCSI transfers are accompanied by an odd parity bit for each byte.

Before terminating a command with this error, the LD 1200 attempts to correct the condition using the SCSI message system.

If a parity error occurs during the transfer of write data from the Host to the Media, the LD 1200 Internal Controller terminates the transfer with the Host at the end of that sector. The transfer from the Internal Controller to the Media continues until the erroneous information is reached. The Host is alerted to the problem at this point and the command is aborted.

3.3.4.28. Unable to Read Data Error

This error is reported when the LD 1200 is unable to read one or more fields in a sector. This is normally caused by detection of a nonrecoverable ECC error. This error can also be caused by an unreadable Vector Address Field. The Host has the option of inhibiting the LD 1200 Error Correction Code circuit.

3.3.4.29. Logical Block Address Not Found

This error is reported when the next Logical Block Address cannot be found. This condition occurs when a Read command attempts to read across the boundary between successive Writes, where the first attempt to Write resulted in a Rewrite and the Address Skip Enable Mode Select Option is disabled. In other words, this error results from trying to read a lost Logical Address.

3.3.4.30. Unable to Write Data Error

This error is reported when a Write operation, including retries, fails. If the LD 1200 is enabled for Rewrites, it exhausts the Write Retry Count prior to reporting this error. This error is also reported if an attempt to write a Postfield is unsuccessful.

3.3.4.31. Internal Parity Error

This error is reported whenever the LD 1200 detects a parity error on one of its internal data busses. The Host might want to retry the operation that was in progress by issuing a command to pick up where the error occurred. If recovery is possible, the problem was probably transient in nature. If the problem is not recoverable, the LD 1200 must be repaired. If the parity error occurred in the device hardware, bytes of the Sense Data Block provide additional information.

3.3.4.32. Servo/Drive Control Parity Error

A Servo/Drive Control (S/DC) Parity Error is indicated when S/DC logic in the Drive detects a parity error during receipt of a data byte or control transfer over the internal SIA/IDI Bus. If this error is detected during a Write operation, the LD 1200 aborts the ongoing operation and reports the problem to the Host. The Internal Controller clears the error and attempts a Rewrite on the next revolution.

3.3.4.33. Modulator/Demodulator Synchronizer Parity Error

A Modulator/Demodulator Synchronizer (MDS) Parity Error is indicated when MDS logic in the Drive detects a parity error during receipt of a data byte over the internal SIA/IDI Bus. If the error is detected during a Write operation, the operation is aborted and the problem is reported to the Host The Internal Controller clears the error and attempts a Rewrite on the next revolution.

3.3.4.34. Error Correction Code Circuitry Fault

This fault is reported by the LD 1200 if a malfunction in the Error Correction Code circuitry is detected during normal online (nondiagnostic) operation. The LD 1200 can execute diagnostic tests on this circuitry when the circuit is not engaged in a normal encoding or decoding function. These are used to ensure that the circuit works properly. If this circuit were to malfunction during a Write operation, improper error correction characters could be generated for a period of time before the Host detected a malfunction.

3.3.4.35. Voltage Fault

This fault is reported whenever the LD 1200 detects a line sync fault (loss of ac line voltage for two or more cycles). Total loss of power may make it impossible for the LD 1200 to report this fault because dc reserve may not allow enough time for error reporting to the Host.

3.3.4.36. Invalid Bootstrap Load Error

To accommodate future diagnostic testing using nonresident microcode, the LD 1200 allows the down-loading of microcode via the SCSI interface. The LD 1200 verifies the validity of all microprograms using a CRC check prior to execution (this includes LD 1200 microcode as well as down-loaded programs). When a CRC error is detected on a down-loaded program, the LD 1200 declares an invalid Bootstrap Load Error and terminates the execution of the command.

3.3.4.37. Laser Degraded

This condition is reported when the LD 1200 has detected degradation of the laser such that laser replacement is required. The Host may continue to use the LD 1200 for Read operations, but should eliminate or severely restrict all Write operations until the laser is replaced.

The degraded condition is detectable only during Write operations. Therefore, the Host system should log and take appropriate action on the status code immediately. If the LD 1200 is powered off, it will not detect the degraded condition until it is powered back on and the problem is again detected during a Write operation.

3.3.4.38. Power-Up Diagnostics Aborted

This fault Code is reported in conjunction with a UNIT ATTENTION when the power-up diagnostics are not completed because the LD 1200 responded to a Selection.

If this Fault Code is received and the self-test results are important, the Host can use the Send Diagnostic command to explicitly request a self-test. This form of diagnostic performs the same tests but cannot be interrupted.

3.3.4.39. Diagnostic Fault Detected

This Fault Code is reported as a result of a diagnostic fault. The diagnostic tests are executed during dc power-up, when requested by the Host, or initiated from the Maintenance Panel. When this fault is reported, the Host can issue a Receive Diagnostic Results command to determine the problem. This code can be reported in conjunction with a UNIT ATTENTION caused by a power-up.

3.3.4.40. Illegal Sequence (Device Not Ready)

This Fault Code is reported when a device fault has occurred that has not been cleared by the Host and a new Command Descriptor Block is put into execution for the faulted device. This fault is also reported when the Host attempts an operation with a LD 1200 that does not have its Spindle powered up or is otherwise not ready. This code is also reported when the Host attempts to start the Spindle while the START/STOP switch is in the Stop position.

3.3.4.41. Write Protected Device Error

This error is reported when the Host attempts a Write operation using a hardware write-protected LD 1200. Hardware write protection may be selected using the WRITE PROTECT switch on the LD 1200 Operator Panel or by loading a write-protected Data Cartridge into the LD 1200. Write protection initiated using either hardware or software causes the Write Protect indicator on the Operator Panel to illuminate.

3.3.4.42. Data Field Overwrite Error

An Overwrite Error is indicated when a write error, detected by the DRDW circuitry, is encountered during the attempt to write one of the Write Protect Bytes in a sector. This error may occur because there is a Media flaw at that location or because the sector was previously written in. The cause of the error can be determined using the Data Detect and Overwrite Error bits from the Drive. If only the Overwrite Error Bit is high, the error is probably a Media flaw in the Write Protect Byte. In this case, if Rewrites are enabled by the Internal Controller, the Drive attempts a Rewrite operation in the next sector. This operation results in a one revolution latency, to allow the internal Controller to clear errors and reissue the function. If both the Data Detect and Overwrite Error bits are high, an actual data overwrite has been attempted. In this case, the operation is aborted.

3.3.4.43. Empty Sector Detected

This code is reported only during Read operations with the Drive and indicates that the LD 1200 has encountered an empty sector (one with an unwritten User Data Field that is followed by a sector containing an unwritten Vector Address Field). Stop On Empty Sector is optionally disabled by setting the Blank Skip Enable bit with the Mode Select command.

3.3.4.44. Device Error

This code is reported when the LD 1200 detects a device error. Device errors, unlike device faults, do not necessarily terminate the ongoing operation of the LD 1200. When an error recovery procedure is started, the LD 1200 temporarily halts the current command until successful error recovery or the recovery operation has continued without success for 10 seconds, whichever comes first. If error recovery is successful, the command is continued and the Host can read the Sense Block at the completion of the command to determine what kind of errors occurred. If error recovery is unsuccessful or if it continues for more than 10 seconds, the command is aborted and the error is reported with HARDWARE ERROR (Sense Key 04).

The LD 1200 saves all device Error bits (Bytes 14, 15 of the Sense Data Block) until the Host reads the sense data. Receipt of a new command from the same Host that issued the errored command causes sense to be cleared.

3.4. INTERFACES

There are two primary interfaces associated with the LD 1200:

(1) SCSI - Small Computer System Interface

(2) IDI - Internal Device Interface

3.4.1. Definitions

The following are definitions of terms used in descriptions of LD 1200 interfaces:

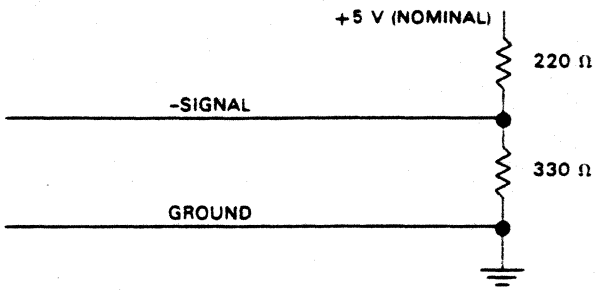
Initiator/Host:	A SCSI device which requests an operation to be performed by another SCSI device.
Target:	A SCSI device (the LD 1200) which performs an operation requested by an Initiator.
Logical Unit:	A physical or virtual device addressable through a target.
Host Computer Adapter:	The hardware and software necessary to interface the Host CPU to the SCSI interface.
CM (Control Module):	The intelligent control logic that interfaces with the Host system via an SCSI interface. In this description, the CM is the controller within the LD 1200.
Command Descriptor Block:	The data structure used to communicate requests from an Initiator to a Target.
SCSI Device:	A host computer adapter, peripheral controller, or an intelligent peripheral which can be attached to the SCSI bus.

3.4.2. Small Computer System Interface (SCSI)

3.4.2.1. SCSI Hardware

The SCSI cables are of the round, shielded, twisted-pair type with shielded connectors. One cable is required between each LD 1200 in a daisy-chain, and one cable is required between the Host and the first LD 1200.

The Driver/Receiver combination is a single-ended open-collector transceiver system. A terminator assembly is required at the last unit in the system, whether the system is daisy-chained or not. A terminator is needed at the Host Adapter as well. Figure 3-12 is a diagram of the termination used in the LD 1200.



ADP50

Figure 3-12. Termination for Single-Ended Devices

3.4.2.2. SCSI Signal Definitions

Figure 3-13 is a functional diagram of the SCSI signal lines. There are nine (9) control signals and nine (9) data signals, including parity. The signal lines are defined as follows:

BSY (BUSY) - This signal indicates that the data bus is being used.

SEL (SELECT) - This signal is used by an Initiator to select a Target, or by a Target to reselect an Initiator.

C/D (CONTROL/DATA) - This is a signal which is driven by a Target to indicate whether CONTROL or DATA information is on the data bus.

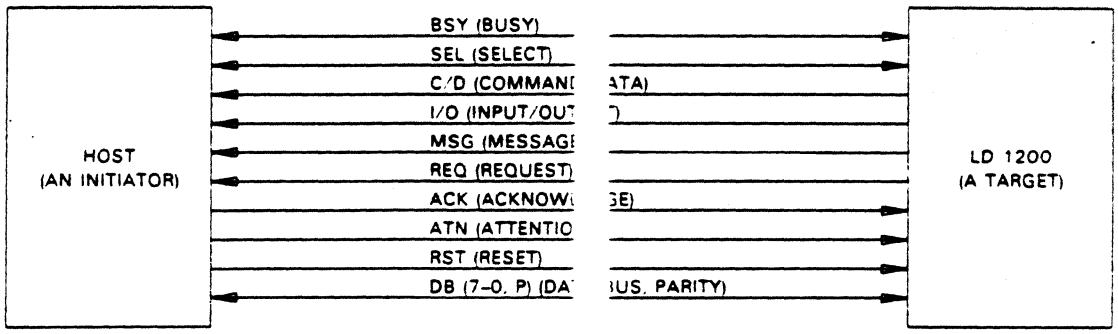
I/O (INPUT/OUTPUT) - This signal is driven by a Target to control the direction of data movement on the data bus. A true signal indicates input to the Initiator.

MSG (MESSAGE) - This signal is driven by the Target to indicate that a message byte is to be transferred to or from the Initiator.

REQ (REQUEST) - This is a signal driven by a Target requesting a REQ/ACK data transfer handshake.

ACK (ACKNOWLEDGE) - This is a signal driven by an Initiator acknowledging a REQ/ACK data transfer handshake.

ATN (ATTENTION) - This is a signal from the Initiator to indicate that the Initiator has a message ready for the Target to accept.



ADP51

Figure 3-13. SCSI Interface Signals

RST (RESET) - This is a signal driven by the Initiator which causes the Target to stop all operations and return to the Idle condition.

DB(7-0,P)(DATA BUS) - The Data Bus consists of eight (8) data bit signals plus a parity bit. DB(7) is the most significant bit. Bit number, significance and priority decreases downward to DB(0).

3.4.2.3. SCSI Bus Phases

The SCSI interface includes eight distinct phases. The SCSI Bus can never be in more than one phase at a time.

The eight bus phases are as follows:

(1) BUS FREE

(2) ARBITRATION

(3) SELECTION

(4) RESELECTION

(5) COMMAND

(6) DATA

(7) STATUS

(8) MESSAGE

BUS FREE Phase

The BUS FREE phase is used to indicate that no SCSI Device is actively using the SCSI Bus and that it is available for subsequent users.

SCSI Devices detect the BUS FREE phase after SEL and BSY are both False for at least a Bus Settle Delay.

The SCSI Device releases all SCSI Bus signals within a Bus Clear Delay after BSY and SEL become continuously False for a Bus Settle Delay. If a SCSI Device requires more than a Bus Settle Delay to detect BUS FREE phase, then it shall release all SCSI Bus signals within a Bus Clear Delay minus the excess time to detect BUS FREE phase. The total time to clear the SCSI Bus shall not exceed a Bus Settle Delay plus a Bus Clear Delay.

ARBITRATION Phase

The ARBITRATION phase allows one SCSI Device to gain control of the SCSI Bus so that it can assume the role of an initiator or Target.

The procedure for a SCSI Device to obtain control of the SCSI Bus is as follows:

(1) The SCSI Device first waits for the BUS FREE phase to occur. The BUS FREE phase is detected whenever both BSY and SEL are simultaneously and continuously False for a minimum of a Bus Settle Delay.

(2) The SCSI Device then waits a minimum of a Bus Free Delay after detection of the Bus Free phase (i.e., after BSY and SEL are both False for a Bus Settle Delay) before driving any signal.

(3) Following the Bus Free Delay in step 2, the SCSI Device may arbitrate for the SCSI Bus by asserting both BSY and its own SCSI ID. However, the SCSI Device does not arbitrate (i.e., assert BSY and its SCSI ID) if more than a Bus Set Delay has passed since the BUS FREE phase was last detected.

(4) After waiting at least an Arbitration Delay (measured from its assertion of BSY) the SCSI Device examines the DATA BUS. If a higher priority SCSI ID bit is True on the DATA BUS, then the SCSI Device has lost the arbitration and the SCSI Device may release its signals and return to step 1. If no higher priority SCSI ID bit is True on the DATA BUS, then the SCSI Device has won the arbitration and it asserts SEL. Any other SCSI Device which is participating in the ARBITRATION phase has lost the arbitration and releases BSY and its SCSI ID bit within a Bus Clear Delay after SEL becomes True. A SCSI Device that loses arbitration may return to step 1.

(5) The SCSI Device that wins arbitration waits at least a Bus Clear Delay plus a Bus Settle Delay after asserting SEL before changing any signals.

NOTE

The SCSI ID bit is a single bit on the DATA BUS that corresponds to the SCSI Devices' unique SCSI Address. All other seven Data Bus bits are released by the SCSI Device. Parity is not valid during the ARBITRATION phase. During the ARBITRATION phase, D8(P) may be undriven or driven to the True state, but is not driven to the False state.

SELECTION Phase

The SELECTION phase allows an Initiator to select a Target for the purpose of initiating some Target function (e.g., read or write data).

NOTE

During the SELECTION phase, I/O is negated so that this phase can be distinguished from the RESELECTION phase.

In systems with ARBITRATION phase implemented, the SCSI Device that won the arbitration has both BSY and SEL asserted and has delayed at least a Bus Clear Delay plus a Bus Settle Delay before a ending the ARBITRATION phase. The SCSI Device that won the arbitration becomes an initiator by releasing I/O. The Initiator sets the DATA BUS to a value which is the "OR" of its SCSI ID bit and the Target's SCSI ID bit. The Initiator then waits at least two Deskew Delays and releases BSY. The Initiator then waits at least a Bus Settle Delay before looking for a response from the Target.

In all systems, the Target determines that it is selected when SEL and its SCSI ID bit are True and BSY and I/O are False for at least a Bus Settle Delay. The selected Target may examine the DATA BUS in order to determine the SCSI ID of the selecting Initiator. The selected Target then asserts BSY within a Selection Abort Time of its most recent detection of being selected; this is required for correct operation of the timeout procedure. In systems with parity implemented, the Target does not respond to a selection if bad parity is detected. Also, if more than two SCSI ID bits are on the DATA BUS, the Target does not respond to selection.

At least two Deskew Delays after the Initiator detects BSY is True. It releases SEL and may change the DATA BUS.

Two optional selection timeout procedures are used to clear the SCSI Bus if the initiator waits a minimum of a Selection Timeout Delay and there has been no BSY response from the Target:

- The Initiator may assert the RST signal.
- The Initiator continues asserting SEL and releases the DATA BUS. If the initiator has not detected BSY to be True after at least a Selection Abort Time plus two Deskew Delays, the Initiator releases SEL, allowing the SCSI Bus to go the BUS FREE phase.

RESELECTION Phase

RESELECTION allows the LD 1200 to reconnect to a Host for the purpose of continuing some operation that was previously started by the Host, but was suspended by the LD 1200.

Upon completing the ARBITRATION phase, the winning SCSI Device has both BSY and SEL asserted and has delayed at least a Bus Clear Delay plus a Bus Settle Delay. The winning SCSI Device becomes a Target by asserting the I/O signal. The Target also sets the DATA BUS to a value which is the "OR" of its SCSI ID bit and the Initiator's SCSI ID bit. The Target then waits at least two Deskew Delays and releases BSY. The Target again waits at least a Bus Settle Delay before looking for a response from the Initiator.

The Initiator determines that it is reselected when SEL I/O, and its SCSI ID bit are True and BSY is False for at least a Bus Settle Delay. The reselection Initiator may examine the DATA BUS in order to determine the SCSI ID of the reselecting Target. The reselected Initiator then asserts BSY within a Selection Abort Time of its most recent detection of being reselected: this is

required for correct operation of the timeout procedure. In systems with parity implemented, the Initiator does not respond to a reselection if bad parity is detected. Also, the Initiator does not respond to a reselection if more than two SCSI ID bits are on the DATA BUS.

After the Target detects BSY, it also asserts BSY and waits at least two Deskew Delays and then releases SEL. The Target may then change I/O and the DATA BUS. After the reselected Initiator detects SEL False, it releases BSY. The Target continues asserting BSY until the Target is ready to relinquish the SCSI Bus.

Two RESELECTION timeout procedures are available to clear the SCSI Bus during a RESELECTION phase if the Target waits a minimum of a Selection Timeout Period and there has been no BSY response from the Initiator.

(1) The Target may reassert the RST signal.

(2) The Target may continue asserting SEL and I/O and release all DATA BUS signals.

INFORMATION TRANSFER Phase

The COMMAND, DATA, STATUS and MESSAGE phases are all grouped together as the information transfer phases because they are all used to transfer data or control information via the Data Bus. The C/D, I/O and MSG signals are used to distinguish between the different Information Transfer phases, as shown in Table 3-2.

Table 3-2. Information Transfer Phases

SIGNAL MSG	SIGNAL C/D	SIGNAL I/O	PHASE NAME	DIRECTION OF TRANSFER	COMMENT
0	0	0	DATA OUT	Host to LD 1200	DATA
0	0	1	DATA IN	LD 1200 to Host	Phases
0	1	0	COMMAND	Host to LD 1200	
0	1	1	STATUS	LD 1200 to Host	
1	0	0	*		
1	0	1	*		
1	1	0	MESSAGE OUT	Host to LD 1200	MESSAGE
1	1	1	MESSAGE IN	LD 1200 to Host	Phases
			NOTES: 0 = False	1 = True * = Not Used	

TBL48

The INFORMATION TRANSFER phases use one or more REQ/ACK handshakes to control information transfer. Each REQ/ACK allows the transfer of one byte of information. During the INFORMATION TRANSFER phases, BSY remains True and SEL remains False. Additionally, during the Information Transfer phases, the LD 1200 continuously envelopes the REQ/ACK handshake(s) with C/D, I/O and MSG in such a manner that these control signals are valid for a Bus Settle Delay before the REQ of the first handshake, and remain valid until the negation of ACK at the end of the last handshake.

The LD 1200 controls the direction of information transfer by means of the I/O signal. When I/O is True, information is transferred from the LD 1200 to the Host. When I/O is False, information is transferred from the Host to the LD 1200.

If I/O is True (transfer to the Host), the LD 1200 first drives DB(7-0,P) to their desired values. delay at least one Deskew Delay plus a Cable Skew delay, the assert REQ. DB(7-0,P) remains

valid until ACK is True at the LD 1200. The Host reads DB(7-0,P) after REQ is True, then signals its acceptance of the data by asserting ACK. When ACK becomes True at the LD 1200, the LD 1200 may change or release DB(7-0,P) and negates REQ. After REQ is False the Host then negates ACK. After ACK is False the LD 1200 may continue the transfer by driving DB(7-0,P) and asserting REQ.

If I/O is False (transfer to the LD 1200) the LD 1200 requests information by asserting REQ. The Host drives DB(7-0,P) to their desired values, delay at least one Deskew Delay plus a Cable Skew Delay and asserts ACK. The Host continues to drive DB(7-0,P) until REQ is False. When ACK becomes True at the LD 1200, the LD 1200 reads DB(7-0,P), then negates REQ. When REQ becomes False at the Host, the Host may change or release DB(7-0,P) and negates ACK. The LD 1200 may continue the transfer by asserting REQ, as described above.

COMMAND Phase

The COMMAND phase allows the LD 1200 to request command information from the Host. The LD 1200 asserts the C/D signal and negates the I/O and MSG signals during the REQ/ACK handshakes of this phase.

DATA Phase

The DATA phase is a term that covers both the Data In and Data Out operations.

The DATA IN phase allows the LD 1200 to request that data be sent to the Host from the LD 1200. The controller asserts I/O and negates C/D and MSG, during the REQ/ACK handshake(s) of this phase. The controller will first drive DATA(0-7,P) to the desired values, delay at least one Deskew Delay, then assert REQ. DATA(0-7,P) remains valid until ACK is received at the controller. The Host reads DATA(0-7,P) after REQ is asserted, then indicates its acceptance of the data by asserting ACK. When ACK becomes asserted at the controller, the DATA BUS may change and REQ will be negated. After REQ is negated, the Host then negates ACK. After ACK is negated, the controller continues the data transfer by driving DATA(0-7,P) and asserting REQ as described previously. The controller compensates for any internal skew by extending the Deskew Delay.

The DATA OUT phase allows the LD 1200 to request that data be sent from the Host to the LD 1200. The controller negates I/O, C/D and MSG during the REQ/ACK handshake(s) of this phase. After receiving a REQ the Host first drives DATA(0-7,P) to their desired values, waits at least one Deskew Delay, then asserts ACK. The Host holds DATA(0-7,P) valid for at least one Deskew Delay plus one Hold Time after the assertion of ACK. The controller then reads the value of DATA(0-7,P) within one Hold Time of the transition of ACK to be asserted. The Host may then negate ACK and change or release DATA(0-7,P). The Host extends the Deskew Delay as necessary to compensate for its own internal skew and the maximum cable skew.

STATUS Phase

The STATUS phase allows the LD 1200 to request that status information be sent from the LD 1200 to the Host. The LD 1200 asserts C/D and I/O and negates the MSG signal during the REQ/ACK handshake of this phase.

MESSAGE Phase

The MESSAGE phase is a term that references either a MESSAGE IN, or a MESSAGE OUT phase. The first byte transferred in either of these phases is either a single byte message or the first byte of a multiple byte message. Multiple byte messages are wholly contained within a single MESSAGE phase. The message system allows communication between a Host and the LD 1200 for the purpose of physical path management.

The MESSAGE IN phase allows the LD 1200 to request that messages be sent to the Host from the LD 1200. The LD 1200 asserts C/D, I/O and MSG during the REQ/ACK handshake(s) of this phase.

The MESSAGE OUT phase allows the LD 1200 to request that a message be sent from the Host to the LD 1200. The LD 1200 may invoke this phase at its convenience in response to the ATTENTION condition created by the Initiator.

In response to the Attention Condition, the LD 1200 asserts C/D and MSG and negates I/O during the REQ/ACK handshake(s) of this phase. The LD 1200 handshakes byte(s) in this phase until ATN goes False.

If the LD 1200 detects one or more parity error(s) on the message byte(s) received, it may indicate its desire to retry the message by asserting REQ after detecting that ATN has gone False, and prior to changing to any other phase. The Host, upon detecting this condition, will re-send all of the previous message byte(s) sent during this phase. When re-sending more than one message byte, the Host asserts ATN prior to asserting ACK on the first byte, and maintains ATN asserted until the last byte is sent.

If the LD 1200 receives all of the message byte(s) successfully (i.e., no parity errors), it will indicate that it does not with to retry by changing to any INFORMATION TRANSFER phase other than MESSAGE OUT phase, and transfers at least one byte. The LD 1200 may also indicate that it has successfully received the message byte(s) by changing to the BUS FREE phase (e.g., ABORT or BUS DEVICE RESET messages).

3.4.2.4. SCSI Bus Conditions

The SCSI Bus has two asynchronous conditions: the Attention Condition and the Reset Condition. These conditions cause certain SCSI Device actions and can alter the phase sequence.

- Attention Condition (See Figure 3-14.)

  The Attention Condition allows a Host to inform the LD 1200 that the Host has a Message ready. The LD 1200 will get this message by performing a MESSAGE OUT phase.

  The Host creates the Attention Condition by asserting ATN at any time except during the ARBITRATION or BUS FREE phases.

  The Host may negate the ATN signal at any time, except that it shall not negate the ATN signal while the ACK signal is asserted during a MESSAGE OUT phase.

  If the ATTENTION condition is detected during the DATA IN or DATA OUT phase the LD 1200 may continue data transfers until an orderly termination point occurs within the LD 1200 before responding with the MESSAGE OUT phase. To guarantee that the LD 1200 responds to ATN with a MESSAGE OUT phase, ATN should remain asserted until the Host detects the assertion of REQ in the MESSAGE OUT phase.

  NOTE

  Asserting ATN does not relieve the Host of the responsibility to answer each DATA IN or DATA OUT phase REQ with an ACK.

- Reset Condition

The Reset Condition is used to immediately clear all SCSI Devices from the bus. This condition takes precedence over all other phases and conditions. Any SCSI Device may create the Reset Condition by asserting RST for a minimum of a Reset Hold Time. During the Reset Condition, the state of all SCSI Bus signals other than RST is not defined.

All SCSI Devices will release all SCSI Bus signals (except RST) within a Bus Clear Delay of the transition of RST to True. The BUS FREE phase always follows the Reset Condition.

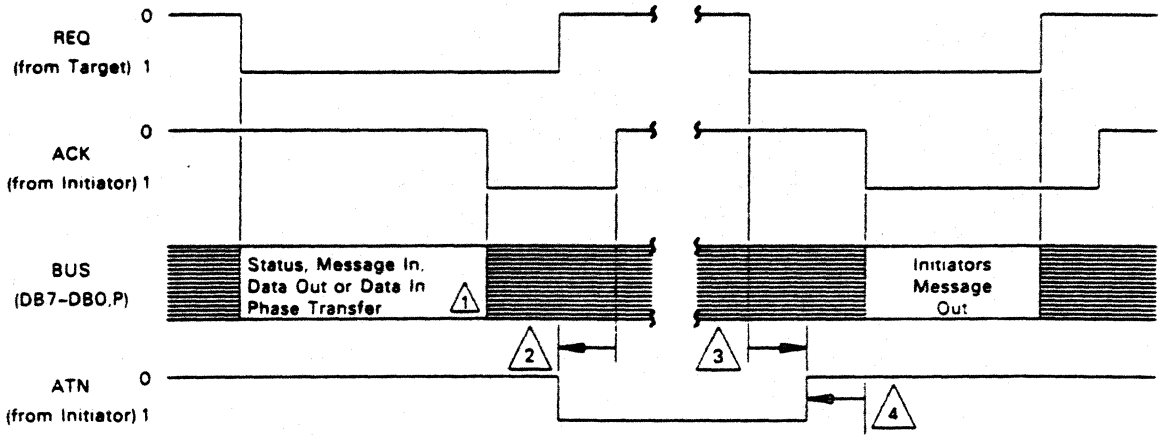
"Hard" Reset is implemented in this machine. Upon detection of the Reset Condition, it completes the following:

(1) Clear all uncompleted commands.

(2) Release all SCSI Logical Unit and Extent reservations.

(3) Return any SCSI Device operating modes to their default states.

(4) Set up UNIT ATTENTION sense data in place of previous sense data.



1. More REQ/ACK transfers may follow the transfer during which the Attention Condition is created in the Data In, or Data Out phase. The Target may continue REQ/ACK transfers in these phases until an orderly termination point is reached in the Target before responding with the Message Out Phase.

2. The Initiator may assert ATN at any time except during the Arbitration or Bus Free Phases. The Initiator should assert ATN Prior to its release of ACK during the REQ/ACK handshake of a status or message in transfer or the last REQ/ACK handshake of a data transfer to insure the next phase is Message Out.

3. The Initiator may deassert the ATN signal at any time. To guarantee that the Target responds with a Message Out Phase, ATN should remain asserted until the Initiator detects the assertion of REQ in the Message Out Phase.

4. The Initiator must Deassert the ATN signal prior to asserting the ACK signal for the last message byte.

ADP52

Figure 3-14. Attention Condition Sequence

3.4.2.5. SCSI Bus Phase Sequences

The order in which the phases are used on the SCSI bus follow a definite sequence. In all systems, the Reset Condition can abort any phase and is always followed by the BUS FREE phase. Also, any other phase can be followed by the BUS FREE phase.

- Arbitrating Systems

  In this system, where the ARBITRATION phase is implemented, the allowable sequences are as shown in Figure 3–15. The normal progression is from the BUS FREE phase to ARBITRATION, from ARBITRATION to SELECTION or RESELECTION, and from SELECTION or RESELECTION to one or more of the INFORMATION TRANSFER phases (COMMAND, DATA, STATUS or MESSAGE).

- All Systems

  There are no restrictions on the sequences between INFORMATION TRANSFER phases. In some cases, the same phase may follow itself (e.g., a DATA phase may be followed by another DATA phase).

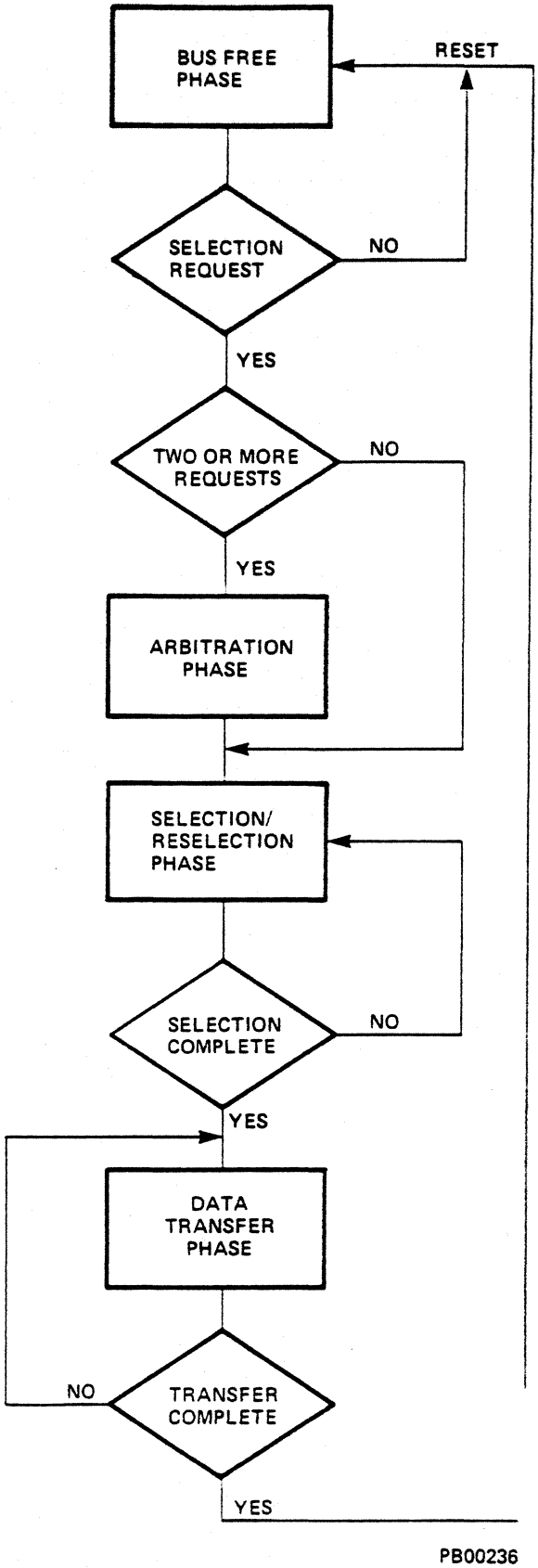


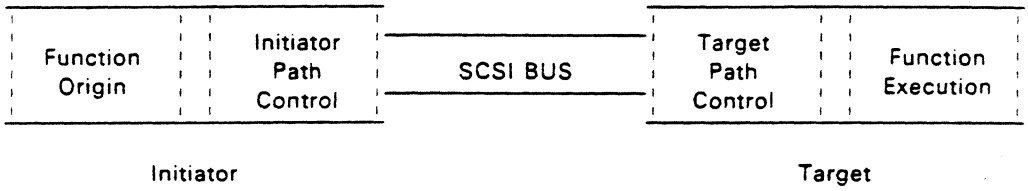
Figure 3-15. *Phase Sequence with Arbitration*

3.4.2.6. SCSI Pointers

Figure 3-16 is a diagram of a situation where an Initiator and a Target communicate on the SCSI Bus in order to execute a command.

Three pointers exist in the SCSI architecture; a Command Pointer, a Data Pointer, and a Status Pointer. The pointers are used to represent the state of the interface and point to the next command, data or status byte to be accessed. The pointers reside in the Initiator path control.

After the pointers are initially loaded by the Initiator, their movement is under control of the Target. When the Target transfers a command, data or status byte, the Initiator increments the corresponding pointer.



ADP53

Figure 3-16. Simplified SCSI System

3.4.2.7. Message System Specification

The message system allows communication between an Initiator and Target for the purpose of physical path management.

NOTE

For the LD 1200, Logical Unit and physical device are synonymous; however, the requirements of the SCSI protocol to identify a Logical Unit still hold. The logical Unit Number field must be 0 in identify messages (or Command Descriptor Blocks when Identify is not used).

SCSI Devices indicate their ability to accommodate more than the COMMAND COMPLETE message by asserting or responding to the ATN signal. The Initiator indicates this in the SELECTION phase by asserting ATN prior to the SCSI Bus condition of SEL True, and BSY. The Target indicates its ability to accommodate more messages by responding to the Attention Condition with the MESSAGE OUT phase after going through the SELECTION phase.

Normally, the first message sent by the Initiator after the SELECTION phase is the IDENTIFY message. This allows the establishment of the physical path for a particular Logical Unit specified by the Initiator. After RESELECTION, the Target's first message is also IDENTIFY. This allows the physical path to be reestablished for the Target's specified Logical Unit Number. Under some

exceptional conditions, an Initiator may send the ABORT message or the BUS DEVICE RESET message instead of the IDENTIFY message, as the first message. Only one logical Unit Number shall be identified for any one selection sequence; a second IDENTIFY message with a new Logical Unit Number shall not be issued before the SCSI Bus has been released (BUS FREE phase).

The single byte messages are listed along with their coded values and their definitions.

COMMAND COMPLETE 00_H — This message is sent from a LD 1200 to a Host to indicate that the execution of a command (or series of linked commands) has terminated, and that valid status has been sent to the Host. After successfully sending this message, the LD 1200 shall go to BUS FREE phase.

NOTE

The command may have been executed successfully or unsuccessfully as indicated in the status.

SAVE DATA POINTER 02_H — This message is sent from a LD 1200 to direct the Host to save a copy of the present active data pointer for the currently attached Logical Unit.

RESTORE POINTERS 03_H — This message is sent from a LD 1200 to direct the Host to restore the most recently saved pointers (for the currently attached Logical Unit) to the active state. Pointers to the Command, Data, and Status locations for the Logical Unit are restored to the active pointers. Command and Status pointers are restored to the beginning of the present command and status areas. The Data Pointer is restored to the value at the beginning of the data area in the absence of a SAVE DATA POINTER message or at the point at which the last SAVE DATA POINTER message occurred for that Logical Unit. This function is also required in response to the IDENTIFY message on Reconnection.

DISCONNECT 04_H — This message is sent from a LD 1200 to inform a Host that the present physical path is going to be broken (the LD 1200 plans to disconnect by releasing BSY), but that a later reconnect will be performed in order to complete the current operation. This message does not cause the Host to save the Data Pointer. When DISCONNECT messages are used to break a long data transfer into two or more shorter transfers, a SAVE DATA POINTER message is issued before each DISCONNECT message.

HOST DETECTED ERROR 05_H — This message is sent from a Host to inform a LD 1200 that a bus parity error has occurred that does not preclude the LD 1200 from retrying the operation. Although present pointer integrity is not assured, a RESTORE POINTERS message or a disconnect followed by a reconnect, causes the pointers to be restored to their defined prior state.

ABORT 06_H

This message is sent from the Host to the LD 1200 to clear the present operation. If a Logical Unit has been identified, any active command, all pending data and any previously set Sense Data for that Host are cleared. The Logical Unit becomes identified by the Identify message or by the LUN field of a Command Descriptor Block. The LD 1200 will go to the BUS FREE phase. Operating mode selections and reservations will remain intact. No status or ending message will be sent.

If a Logical Unit has not been identified, the LD 1200 will go to the BUS FREE phase with no effect on the state of active commands, or other information. It is not an error to issue this message (with or without identification of a Logical Unit) to a LD 1200 that is not currently performing an operation for the Host.

When a LD 1200 receives an ABORT message while processing a Read or Write command, the operation ceases and the Sense Data will indicate Aborted Command (Sense Key $0B_H$). The Sense Data Information Bytes will indicate the first Logical Block Address not completed. Note that command ending status is not sent in this case, so the Host must issue the Sense command without CHECK CONDITION ending status.

MESSAGE REJECT 07_H

This message is sent from either the Host or LD 1200 to indicate that the last message it received was inappropriate or has not been implemented.

In order to indicate its intentions of sending this message, the Host asserts the ATN signal prior to its release of ACK for the REQ/ACK handshake of the message that is to be rejected.

When a LD 1200 sends this message, it changes to MESSAGE IN phase and sends this message prior to requesting additional message bytes from the Host. This provides an interlock so that the Host can determine which message is rejected.

NOTE

During the DATA phase, the LD 1200 may ignore inappropriate messages such as NO OPERATION, MESSAGE REJECT and MESSAGE PARITY ERROR. HOST DETECTED ERROR, ABORT and BUS DEVICE RESET will not be ignored.

NO OPERATION 08_H

This message is sent from a Host in response to a LD 1200's request for a message when the Host does not currently have any other valid message to send.

MESSAGE PARITY ERROR 09_H

This message is sent from the Host to the LD 1200 to indicate that one or more bytes in the last message it received had a parity error.

	In order to indicate its intentions of sending this message, the Host asserts the ATN signal prior to its release of ACK for the REQ/ACK handshake of the message that has the parity error. This provides an interlock so that the LD 1200 can determine which message has the parity error.
BUS DEVICE RESET $0C_H$	This message is sent from a Host to direct a LD 1200 to clear all current commands on that SCSI Device. This message forces the SCSI Device to an initial state with no operations pending for any Host. Upon recognizing this message, the LD 1200 goes to the BUS FREE phase.
IDENTIFY 80_H to FF_H	This message is sent by either the Host or the LD 1200 to establish the physical path connection between a Host and LD 1200 for a particular Logical Unit. Bit 7 - This bit is always set to one to distinguish this message from the other messages. Bit 6 - This bit is only set to one by the Host. When set to one, it indicates that the Host has the ability to accommodate disconnection and reconnection. Bits 5-3 - RESERVED Bits 2-0 - These bits specify the Logical Unit Number. For the LD 1200 they must be 0. Only one Logical Unit Number shall be identified for any one selection sequence; a second IDENTIFY message with a new Logical Unit Number shall not be issued before the bus has been released (BUS FREE phase). When sent from a LD 1200 to a Host during reconnection, an implied RESTORE POINTERS message is performed by the Host prior to completion of this message.

3.4.2.8. SCSI Command Implementation

The first byte of any SCSI command will contain an Operation Code. Three bits (Bits 7 - 5) of the second byte of a SCSI command are reserved for specifying the Logical Unit, if it has not been specified in the IDENTIFY message. The last byte of all SCSI commands will contain a Control Byte.

RESERVED bits, bytes, fields, and code values are set aside for possible future usage. A RESERVED bit, field, or byte is set to zero.

A LD 1200 that receives a RESERVED bit, field, or byte that is not zero or receives a RESERVED code value will terminate the command with a CHECK CONDITION status. The Sense Key is set to ILLEGAL REQUEST.

A single command may transfer one or more logical blocks of data. A LD 1200 may disconnect from the SCSI Bus to allow activity by other SCSI Devices while a Logical Unit is being prepared to transfer data.

Upon command completion (successful or unsuccessful), the LD 1200 returns a status Byte to the Host. Since most error and exception conditions cannot be adequately described with a single Status Byte, one status Code (CHECK CONDITION) indicates that additional information is available. The Host must issue a Request Sense command to retrieve this additional information.

3.4.2.9. Command Descriptor Block

A request to a Peripheral Device is performed by sending a Command Descriptor Block to the LD 1200. For several commands the request is accompanied by a list of parameters sent during the DATA OUT phase.

The Command Descriptor Block always has an Operation Code as the first byte of the command. This is followed by a Logical Unit Number, command parameters (if any), and a Control Byte.

Operation Code

The Operation Code of the Command Descriptor Block has a Group code field and a Command Code field (see table 3-3). The three-bit Group Code field provides for eight groups of command codes (see table 3-4). The five-bit Command Code field provides for thirty-two command codes in each group (see table 3-5). Thus a total of 256 possible Operation Codes exist.

The Group Code specifies one of the following groups:

Group 0 - Six-byte commands
Group 1 - Ten-byte commands

Table 3-3. Operation Code

BIT / BYTE	7	6	5	4	3	2	1	0
0	Group Code			Command Code				

TBL43

Table 3-4. Typical Group 0 Command Descriptor Block for Six-Byte Commands

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			Logical Block Address Bits if Required (MSB)				
2	Logical Block Address if Required							
3	Logical Block Address if Required (LSB)							
4	Transfer Length if Required							
5	Control Byte						0	0

TBL44

Table 3-5. Typical Group 1 Command Descriptor Block for Ten-Byte Commands

BIT / BYTE	7	6	5	4	3	2	1	0
0	Operation Code							
1	Logical Unit Number			Command Specific Bits				0
2	Logical Block Address if Required (MSB)							
3	Logical Block Address if Required							
4	Logical Block Address if Required							
5	Logical Block Address if Required (LSB)							
6	RESERVED							
7	Transfer Length if Required (MSB)							
8	Transfer Length if Required (LSB)							
9	Control Byte						0	0

TBL45

Logical Unit Number

The Logical Unit Number addresses one of up to eight physical or virtual devices attached to a Target. For the LD 1200, the Logical Unit specified must be 0 or the command will be rejected with BUSY status. The Logical Unit Number field of the Command Descriptor Block is provided for systems that do not implement the identify message. A Target which receives an IDENTIFY message uses the Logical Unit Number specified within the IDENTIFY message. In this case, the Target ignores the Logical Unit Number specified within the Command Descriptor Block.

Logical Block Address

The Logical Block Address on Logical Units begins with Block zero and continues up to the last logical block on that Logical Unit.

Group 0 Command Descriptor Blocks contain 21-bit Logical Block Addresses. Group 1 Command Descriptor Blocks contain 32-bit Logical Block Addresses.

The Logical Block concept implies that the initiator and Target have previously established the number of data bytes per logical block — either 1024 or 1025 bytes. This may be established through the use of Read Capacity command or Mode Sense command. The LD 1200 default block length is 1024 bytes.

Transfer Length

The Transfer Length specifies the amount of data to be transferred, usually the number of blocks. For several commands, the transfer Length indicates the requested number of bytes to be sent as defined in the command description. For these commands the Transfer Length field may be identified by a different name.

Commands that use one byte for Transfer Length allow up to 256 blocks of data to be transferred by one command. A Transfer Length value of 1 to 255 indicates that number of blocks is to be transferred. A value of zero indicates 256 blocks.

Commands that use two bytes for Transfer Length allow up to 65,535 blocks of data to be transferred by one command. In this case a Transfer Length of zero indicates no data transfer is to take place. A value of 1 to 65,535 indicates that number of blocks be transferred.

Control Byte

The Control Byte is the last byte of every Command Descriptor Block. Control Byte bits 7 through 0 are Reserved and must be 0.

3.4.2.10. Command Examples

A typical operation on the SCSI Bus is likely to include a single Read command to a Peripheral Device. This operation is described in detail starting with a request from the Host. This example assumes that no malfunctions or errors occur.

The Host has active pointers and a set of stored pointers representing active disconnected SCSI Devices. The Host sets up the active pointers for the operation requested, arbitrates for the SCSI Bus, and selects the LD 1200. Once this process is completed, the LD 1200 assumes control of the operation.

The LD 1200 obtains the command from the Host (in this case a Read command). The LD 1200 interprets the command and executes it. In this case, the LD 1200 sends the data to the Host. At the completion of the Read command, the LD 1200 sends a Status Byte to the Host. To end the operation, the LD 1200 sends a COMMAND COMPLETE message to the Host.

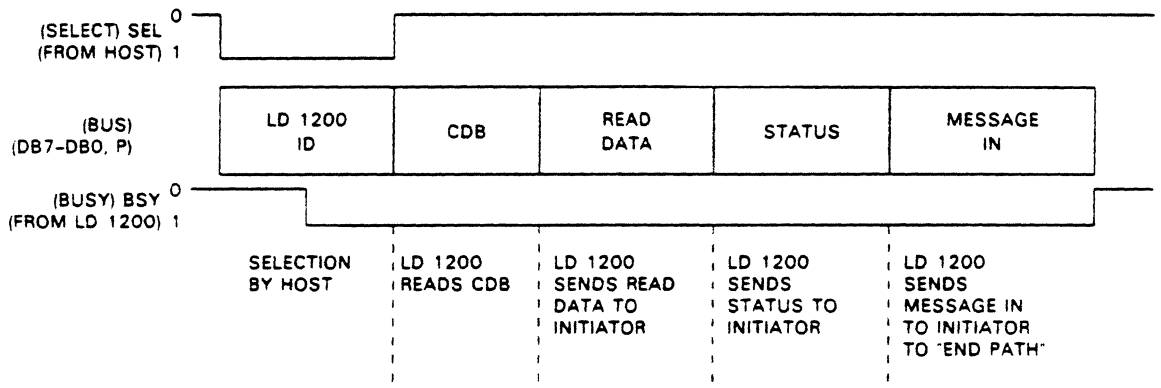


Figure 3-17. Single Command Example with Data Transfer to the Host

In the single command example, (figure 3-17), the read function may require a time-consuming physical Seek. In order to improve system throughput, the LD 1200 disconnects from the Host, freeing the SCSI Bus to allow other requests to be sent to other Logical Units. To do this, the Host needs to be reselectable and capable of restoring the pointers upon reconnection. The LD 1200 needs to be capable of arbitrating for the SCSI Bus and reselecting the Host.

After the LD 1200 has received the Read command (and determined that there will be a delay), it disconnects.

When data is ready to be transferred, the LD 1200 reconnects to the Host. As a result of this reconnection, the Host restores the pointers (to the initial state) and the LD 1200 continues to finish the operation. The Host recognizes that the operation is complete when the COMMAND COMPLETE message is received.

3.4.2.11. Group 0 Commands

The following is a brief description of the Group 0 commands and their operation codes in hexadecimal:

Test Unit Ready - 00

The Test Unit Ready command provides a means to check if the logical Unit is ready. "Ready" for the LD 1200 means that the spindle is up to speed, with no faults present. This is not a request for self test. If the Logical Unit is ready, the command is terminated with GOOD STATUS.

Rezero Unit -01

This command causes the LD 1200 to position its actuator at track zero. This command completes within 350 ms maximum.

Request Sense - 03

The Request Sense command requests that the LD 1200 Logical Unit transfer Sense Data to the Host. The Sense Data is valid for ending status returned on the prior command from this Host. This Sense Data is preserved by the LD 1200 for the Host until receipt of any other command from the Host. Sense Data is cleared upon receipt of any subsequent command to the Logical Unit from the Host receiving the ending status.

Read - 08

The Read command requests that the LD 1200 transfer data to the Host.

Seek - 0B

The Seek command requests that the logical Unit seek to the specified Logical Block Address. Upon successful completion, good ending status is sent to the Host.

Search for Empty Blocks - 0C

The Search for Empty Blocks command directs the LD 1200 to scan the Media for the first instance of a continuous unwritten area, a Number of Empty Blocks in length. The scan commences with the Starting Logical Block Address and continues for Number of Blocks to Scan blocks, as necessary.

Inquiry - 12

The Inquiry command requests that information regarding parameters of the LD 1200 be sent to the Host.

Mode Select - 15

The Mode Select command provides a means for the Host to specify the operating parameters of the LD 1200. The command specifies the number of bytes of Parameter List data which is to be transferred from the Host to the LD 1200.

Reserve - 16

The Reserve command is used to reserve Logical Units, or extents within Logical Units, for the use of the Host. Queued reservations are not supported by the LD 1200.

Release - 17

The Release command is used to release a previously reserved LD 1200, or previously reserved extents within a LD 1200. It is not an error for an Initiator to try to release a reservation which is not currently active or queued.

Copy - 18

This command causes the LD 1200 to transfer data from one location on its Media to another location, for purposes of duplicating all or portions of user files.

Salvage Data - 19

If a Read operation with the LD 1200 has been unsuccessful (e.g., unable to read data or data uncorrectable with ECC), the system may call upon the LD 1200 to execute the Salvage Data command in an attempt to recover the data. The Salvage Data command causes the LD 1200 to perform one read of the designated sector and to provide the entire contents of the sector (excluding the header) to the Host.

Mode Sense - 1A

The Mode Sense command provides a means for a LD 1200 to report is current operating parameters. It is a complementary command to the Mode Select command. Sixteen bytes of data are required for the full Mode Sense data block.

Start/Stop Unit - 1B

The Start/Stop Unit command requests that a LD 1200 be enabled or disabled for further Media accessing operations.

Receive Diagnostics Results - 1C

The Receive Diagnostic Results command requests analysis data be sent to the Host after completion of a Send Diagnostic command or a power-up self test. The Receive Diagnostic Result command will be rejected with CHECK CONDITION Status and a Sense Key of ILLEGAL REQUEST if Diagnostic Results data are not available.

Send Diagnostic - 1D

The Send Diagnostic command requests the LD 1200 to perform diagnostic tests on itself.

3.4.2.12. Group 1 Commands

Read Capacity - 25

The Read Capacity command provides a means for the Host to request information regarding the capacity of the Logical Unit. Eight bytes of Read Capacity data are sent during the Data In phase of the command, giving the maximum logical block address and the block length.

Read - 28

The Read command requests that the LD 1200 transfer data to the Host.

Write - 2A

The Write command requests that the LD 1200 write the data transferred from the Host to the medium.

Seek - 2B

The Seek command requests that the Logical Unit seek to the specified Logical Block address. Upon successful completion, good ending status is sent to the Host.

Write and Verify - 2E

The Write and Verify command requests that the LD 1200 write the data transferred from the Host to the medium and then verify that data.

3.4.2.13. Completion Status Byte

The Completion Status Byte will be sent by the LD 1200 at the completion of a command. A status of GOOD STATUS will be returned at the end of a single command execution provided no fault conditions have occurred during the execution of the command. Fault conditions encountered during command execution will cause termination of the command and one of the status conditions listed will be reported in the Completion Status Byte. More than one status may be reported. Tables 3-6 and 3-7 show the status and byte code values.

Table 3-6. Status Byte

BIT / BYTE	7	6	5	4	3	2	1	0
0	0	0	0	Status Byte Code				0

TBL46

Table 3-7. Status Byte Code Bit Values

BITS OF STATUS BYTE								STATUS REPRESENTED
7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	GOOD STATUS
0	0	0	0	0	0	1	0	CHECK CONDITION
0	0	0	0	0	1	0	0	CONDITION MET/GOOD STATUS
0	0	0	0	0	1	1	0	RESERVED
0	0	0	0	1	0	0	0	BUSY
0	0	0	0	1	0	1	0	RESERVED
0	0	0	0	1	1	0	0	RESERVED
0	0	0	0	1	1	1	0	RESERVED
0	0	0	1	0	0	1	0	RESERVED
0	0	0	1	0	1	1	0	RESERVED
0	0	0	1	1	0	0	0	RESERVATION CONFLICT
0	0	0	1	1	0	1	0	RESERVED
0	0	0	1	1	1	0	0	RESERVED
0	0	0	1	1	1	1	0	RESERVED

TBL47

A description of the Status Byte Codes is given below:

GOOD STATUS - The status indicates that the LD 1200 successfully completed the command.

CHECK CONDITION - Any error, exception or abnormal condition which causes Sense Data to be set, will cause CHECK CONDITION status. The Request Sense command should be issued following CHECK CONDITION status, to determine the nature of the condition.

CONDITION MET - The Search commands will send this status whenever a search condition is satisfied. The Logical Block Address of the logical block which satisfies the search may be determined with a Request Sense command.

BUSY - The LD 1200 is busy with another (currently disconnected) command and this command indicates that the Target should not disconnect or the prior command is from this Host. BUSY is also used to reject a command requesting a nonexistent Logical Unit Number.

RESERVATION CONFLICT - This status will be sent to any command which attempts to access a Logical Unit or an extent within a Logical Unit which is reserved by another Initiator for that type of access.

3.4.2.14. Sense Description

Byte ten of the Sense Data block contains information on recovered errors and unit attention conditions as described in the following:

Seek Retry Applied

This is reported whenever the LD 1200 has attempted to recover from a seek, tracking, focus or phase error. A seek retry may be accompanied by data retry status and/or error recovery applied status.

Data Retry Applied

This is reported whenever the LD 1200 has incurred rotational latency as the result of performing a reread or rewrite of a sector of data due to an error on the original read or write of that sector. The LD 1200 must be authorized by the Host to perform retries. Normally, a read retry is attempted only after a data correction (ECC) attempt has failed. A read retry may be accompanied by seek retry status and/or error recovery applied status.

Error Recovery Applied

This is reported whenever (1) the ECC circuit has applied correction to the data being transferred; or (2) SCSI Bus parity error(s) caused retransmission of one or more blocks of data. If the Sense Key is RECOVERED ERROR, the recovery was successful.

Unit Attention: State Reset

The UNIT ATTENTION condition being reported caused a LD 1200 control microprocessor reset. The state of the device is now the initial default configuration. Commands, status data and reservations which may have been active or pending are reset.

Unit Attention: Cartridge Change

The UNIT ATTENTION condition being reported implies that the cartridge may have been changed.

Unit Attention: Power-Up

The UNIT ATTENTION condition being reported is an initial power-up. The self-test diagnostics have been attempted. The Fault Code byte should be examined for the results of these tests.

FAULT CODE

Byte eleven of the Sense Data block is the Fault Code. This is used by the LD 1200 to report the reason for terminating a command in more detail than possible with the Sense Key. The codes used are listed below:

BYTE 11

FAULT CODE	HEX CODE
No Fault Code	00
Laser Read Power Fault	01
Laser Write Power Fault	02
Quad Sum High Fault	03
Verify Header Fault	04
Motor Speed Fault	05
MPU Time Out Fault	06
MPU Self-Test Fault	07
Wobble Fault	08
PLL Fault	09
Focus Fault	0A
Seek Fault	0B
Tracking Fault	0C
Line Sync Fault	0D
Data Synchronization Fault	0E
Quad Sum Low Fault	0F
Seek Error	21
Illegal Operation Code	22
Invalid Logical Unit Number	23
Illegal Seek Address	24
Illegal Command Description Block Parameter	25
End of Media Reached	28
Illegal Transfer Length	29
Reservation Table Full	2F
SCSI I/O Parity Error	41
Unable to Read Data	43
Logical Block Address Not Found	44
Unable to Write Data	63
Internal Parity Error	65
ECC Fault	66
Voltage Fault	67
Invalid Bootstrap Load Error	69
Laser Degraded	6B
Skip Count Overflow	6C
Power-Up Diagnostics Aborted	A5
Diagnostic Fault Detected	A6
Illegal Sequence (Device Not Ready)	C1
Write Protected Device Error	C2
Data Field Overwrite	C6
Empty Sector Detected	E5
Device Error	E6

Fault Codes are described in the Error/Fault Handling subsection of this manual.

DEVICE STATUS 1 (Byte 12)

The bit definitions are as follows:

Bit 0 - Unit Ready
Bit 1 - On Track
Bit 2 - Start/Stop Request

Bit 3 - Device Fault
Bit 4 - Cartridge Loaded
Bit 5 - Write Protect Switch
Bit 6 - Cartridge Write Protect
Bit 7 - Device Error

Bit 0, Unit Ready

When set, this bit indicates that the LD 1200 is ready for operation. The term "Ready" means that the spindle motor is up to speed, all drive initialization and power up diagnostic routines have completed successfully, and all drive faults are cleared.

Bit 1, On Track

When set, this bit indicates that the LD 1200 servo and tracking circuits are locked onto the target track. Due to the spiral nature of the tracks used with the media for the LD 1200, the term "On Track" is defined as being 31 or fewer sectors prior to the desired sector. "On Track" is indicated whenever the laser is in this defined zone. On Track is indicated only after the LD 1200 is synchronized with the data on the target track and has verified at least one header address. The On Track signal goes inactive during seeks, automatic jumpbacks, and if focus, tracking, or synchronization is lost. The On Track signal remains active if a seek is issued to a track that the actuator is already on.

Bit 2, Start/Stop Request

This bit reflects the state of the Start/Stop switch on the LD 1200's front panel. When set, this bit indicates that the switch is in the Start position (spindle power up requested). When cleared, the switch is in the Stop position (spindle power down requested).

Bit 3, Device Fault

When set, this bit indicates that a device fault exists in the LD 1200. A fault implies that a malfunction exists that requires servicing in order to restore proper drive operation. Faults differ from Device Errors in that errors may be recoverable conditions.

Bit 4, Cartridge Loaded

When set, this bit indicates that there is a cartridge present in the LD 1200 and that it is fully seated with the cartridge loading door closed.

Bit 5, Write Protect Switch

When set, this bit indicates that the write protect switch on the front panel is active.

Bit 6, Cartridge Write Protected

When set, this bit indicates that the cartridge in the LD 1200 has its write protect tab activated and, accordingly, that the media is unavailable for write operations.

Bit 7, Device Error

When set, this bit indicates that the one or more device errors exist in the LD 1200.

DEVICE STATUS 2 (Byte 13)

The bit definitions are as follows:

Bit 0 - Power Supply Overtemperature
Bit 1 - Cage Overtemperature
Bit 2 - Laser Degraded
Bit 3 - Not Used
Bit 4 - Not Used
Bit 5 - Not Used
Bit 6 - Not Used
Bit 7 - Eject Enabled

Bit 0, Power Supply Overtemperature

When set, this bit indicates that the overtemperature sensor in the LD 1200 power supply detected an overtemperature condition. This bit indicates that Read/Write operations should no longer be done after TBD seconds. The Host should not issue any new commands until this bit is reset by the LD 1200.

Bit 1, Cage Overtemperature

When set, this bit indicates that the overtemperature sensor in the LD 1200 card cage detected an overtemperature condition. This bit indicates that Read/Write operations should no longer be done after TBD seconds. The Host should not issue any new commands until this bit is reset by the LD 1200.

Bit 2, Laser Degraded

When set, this bit indicates that the laser in the LD 1200 has degraded in capability and should be replaced before attempting any more writes. The read capability of the laser is not necessarily affected by this condition.

Bit 7, Eject Enabled

This bit, when set, indicates that the eject solenoid is engaged and, accordingly, the media cartridge may be removed. This status bit is provided for systems that employ automatic cartridge loading mechanisms (jukebox).

ERROR STATUS 1 (Byte 14)

Bit 0, Seek Error

When set, this bit indicates that the LD 1200 was unable to successfully complete a seek operation. A successful seek involves the resynchronization to sector marks and the proper validation of at least one header address.

Bit 1, Reserved

Bit 2, Wobble Error

When set, this bit indicates that there have been errors in reading the servo wobble bytes in the last two sector headers. Wobble bytes are used to ensure proper centering of the laser in the spiral track on the media. Any write operations in progress will be aborted.

Bit 3, Reserved

Bit 4, Overwrite Error

When set, this bit indicates that a DRDW (Direct Read During Write) error was encountered during an attempted write of one of the three Write Protect Flag Bytes in the previous sector. This may be the result of a media flaw at that location or because the sector was previously written. The data rewrite resulting from this error will cause one revolution latency for the CM to clear errors and to reissue the function.

Bit 5, Verify Header Error

When set, this bit indicates that during a seek process the servo processor was unable to read header addresses while verifying the desired track address.

Bit 6, DRDW Error

When set, this bit indicates that more than the allowable number of DRDW (Direct Read During Write) errors were detected during the write of the previous sector.

Bit 7, Track Miscompare Error

When set, this bit indicates that the LD 1200 has detected a miscompare between an internally calculated track LSB, and the lower byte of the track address read from the disk (header value). This error can occur only during read or write operations with the disk.

ERROR STATUS 2 (Byte 15)

Bit 0, Focus Error

When set, this bit indicates that the LD 1200 has been unsuccessful in maintaining focus of the laser beam on the media. If the error is not resolved within one millisecond, a recovery algorithm is initiated by the LD 1200. If the recovery is unsuccessful, a Focus Fault is declared.

Bit 1, Data Synchronization Error

When set, this bit indicates that the LD 1200 has detected a loss of synchronization with respect to the serial data stream to/from the disk. If the LD 1200 is unable to resynchronize, a Data Synchronization Fault is reported.

Bit 2, PLL Error

When set, this bit indicates that the LD 1200's phase-locked oscillator has lost synchronization with the preformatted data clock for a period of 30 μsec or more. If synchronization is not regained within a specified length of time (approximately 5 sectors), the LD 1200 initiates a recovery algorithm. A PLL Fault is declared if recovery is not possible.

Bit 3, Laser Read Power Error

When set, this bit indicates that the LD 1200 has detected that the laser read current is too high or too low. The LD 1200 attempts to regain proper laser read levels at the home position and, if successful, a seek is issued to the track where the error occurred. If recovery is not possible at the home position, a Laser Read Power Fault is declared.

Bit 4, Laser Write Power Error

When set, this bit indicates that the LD 1200 has detected that the write laser current is too high or too low. The LD 1200 attempts to regain proper write laser levels at the home position and, if successful, a seek is issued to the track where the error occurred. If recovery is not possible at the home position, a Laser Write Power Fault is declared.

Bit 5, S/DC Parity Error

When set, this bit indicates that the S/DC board detected a parity error when receiving a data byte on the SIA bus.

Bit 6, MDS Parity Error

When set, this bit indicates that the data Modulator/Demodulator/Synchronizer board detected a parity error when receiving a data byte on the SIA bus.

Bit 7, Tracking Error

When set, this bit indicates that the drive was unable to maintain tracking. If all attempts to recover fail, a Tracking Fault is declared.

3.4.3. Internal Device Interface/System Interface Assembly Bus

The Internal Device Interface (IDI) defines protocol for local communication (within the same backplane) between the group of bus modules comprising the LD 1200 Internal Controller and Drive (refer to figure 3-18). Bus modules are circuits that are attached to and communicate via the SIA Bus. The IDI Interface uses the System Interface Assembly (SIA) Bus architecture for information exchange and further defines the bus protocol by establishing a status and control format for all Drive operations.

As shown in figure 3-18, bus transactions between the bus modules in the Internal Controller or in the Drive are considered to be SIA Bus transactions. These information exchanges do not involve interaction between the Internal Controller and the Drive, and are therefore accomplished using basic SIA Bus timing and protocol (refer to the SIA Bus Timing subsection in this manual).

SIA Bus transactions between Internal Controller and Drive bus modules are further governed by IDI protocol. These exchanges involve interaction between the Internal Controller and the Drive, and are thus restricted by the real time constraints imposed by the rotating Media.

The bus modules connected to the SIA/IDI Bus include both Bus Masters and Bus Slaves, as shown in figure 3-18. A Bus Master is capable of arbitrating for control of the bus. This bus module can select either another Bus Master or a Bus Slave for an information exchange. A Bus Slave cannot arbitrate for control of the bus. It can use the bus only when instructed to do so by a Bus Master.

The structure of the IDI allows the LD 1200 to be interfaced with various system interfaces through the replacement of the ICI PCA with an appropriate interface conversion circuit.

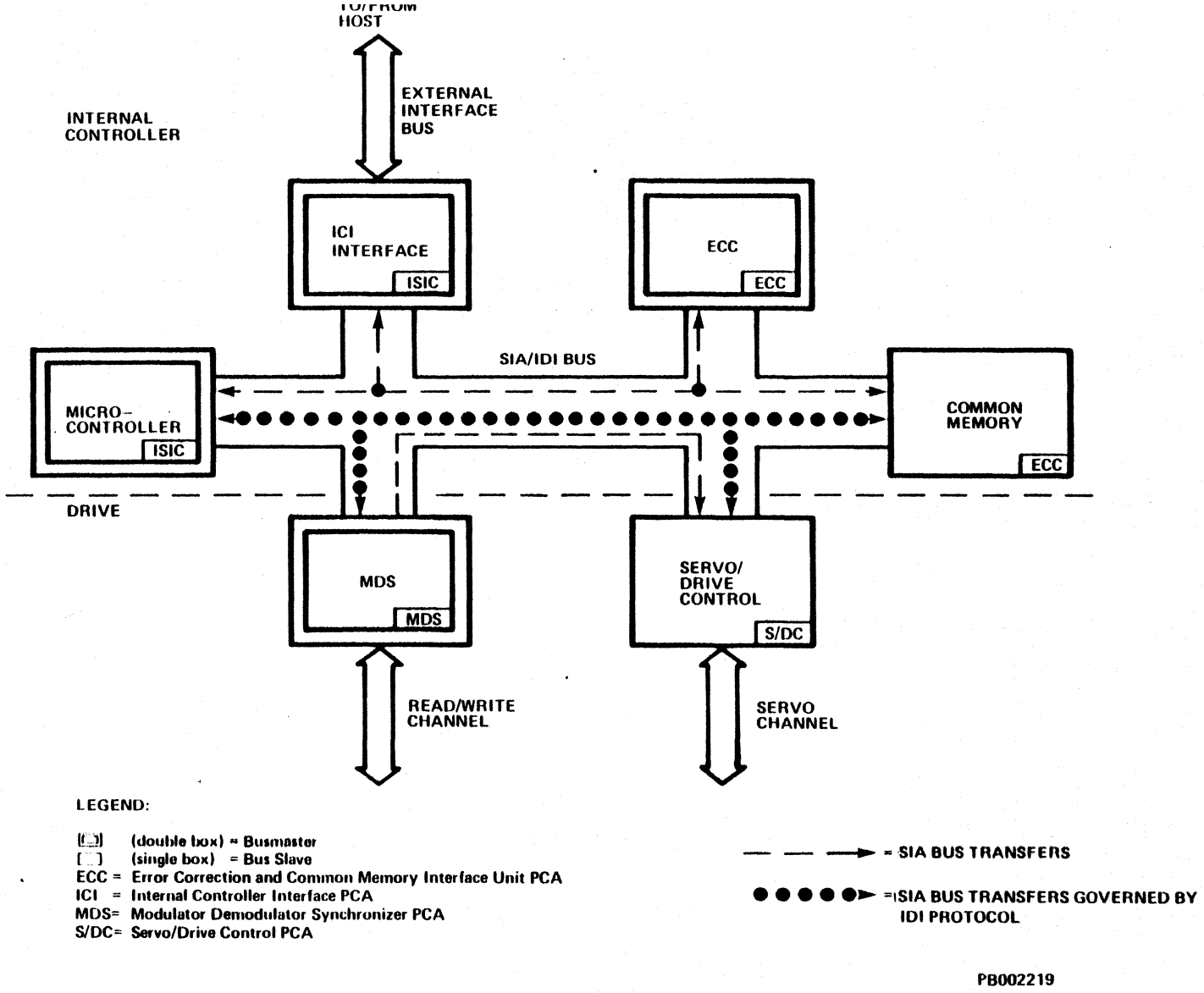


Figure 3-18. LD 1200 SIA/IDI Bus Configuration

3.4.3.1. SIA Bus Line Descriptions

The SIA Bus consists of the following signals:

+SIA R/W (Read/Write)

This signal is generated by the controlling Bus Master. When high, it specifies a bus read operation to transfer information from the addressed bus module to the Bus Master. When low, the signal specifies a write operation from the Bus Master to the addressed bus module.

+SIA MEM I/O (Memory-I/O Transfer)

This signal is generated by the controlling Bus Master. When high, it specifies a transfer of information over the bus between the Bus Master and Common Memory. When low, the signal specifies an information transfer between the Bus Master and the addressed bus module register (I/O port). The state of +SIA R/W determines the direction of the transfer.

-SIA RESET

This signal is used to reset all the bus modules on the SIA/IDI Bus to a known state.

+CLK1, +CLK2, and +CLK3 (SIA Bus Clocks)

These signals are generated by the Internal Controller. They synchronize the bus modules connected to the SIA Bus. The frequency of the SIA Bus Clocks is 2 MHz. One clock cycle corresponds to one bus cycle (one bus transfer).

+SIA D0 through +SIA D7 (SIA Data Bus)

These eight bidirectional lines are used for the transfer of information between bus modules.

+SIA DATA PARITY

This line carries SIA Data Bus parity (odd parity is used).

+SIA ADRS0 through +SIA ADRS15 (SIA Address Bus)

These signals are generated by the controlling Bus Master and provide the address required for the next information transfer (either a Common Memory address or the address of a particular I/O port). The transfer can be a bus read or write operation, as specified by the +SIA R/W signal. The bus module selected can be either Common Memory or a bus module register (port). When the address is for a transfer to Common Memory, all address signals are valid. For a transfer to a bus module register, only +SIA ADRS0 through +SIA ADRS7 are valid.

+BE1 through +BE5 (Bus Enable)

These signals are generated by SIA Bus Masters. They are used in a priority system of bus arbitration to avoid contention when more than one Bus Master is requesting bus access. In general, a higher priority Bus Master prevents a lower priority Bus Master access by deactivating its bus enable signal. Refer to the Bus Module Priority System subsection in this manual for additional details.

3.4.3.2. SIA Bus Timing

SIA Bus timing is shown in figure 3-19. A SIA bus cycle is started with a bus request at the leading edge of CLK3. Provided no higher priority Bus Module is also requesting access (bus enable inputs to the requesting module are true), the bus is granted at the leading edge of the following CLK1. Bus activity occurs, following the bus grant, from the leading edge of CLK1 until the leading edge of the following CLK2. The intervening CLK3 leading edge is used to clock bus data into receiving data buffers in addition to initiating the bus arbitration portion of the next bus cycle.

3.4.3.3. Bus Module Priority System

The transfer of information over the SIA/IDI Bus can be initiated by any of the Bus Masters connected to the bus. The bus priority system prevents contention among Bus Masters.

The priority of the Bus Masters on the bus is established through the use of the Bus Enable (+BEn) signal. The highest priority Bus Master (the MDS PCA) sends Bus Enable to the next lower bus module. This bus module regenerates Bus Enable and sends it to the next lower bus module. This action is repeated until the signal has been propagated through all Bus Masters on the bus, from highest to lowest priority.

The priority of modules on the SIA Bus is as follows (refer to figure 3-20):

(1) Modulator Demodulator Synchronizer (MDS) PCA (highest priority)

(2) ICI Microprocessor (MPU)

(3) Error Correction Code Logic

(4) External Interface Logic

Common Memory (on the ECC PCA) and the Servo/Drive Control PCA are Bus Slaves and therefore are not included in the priority system.

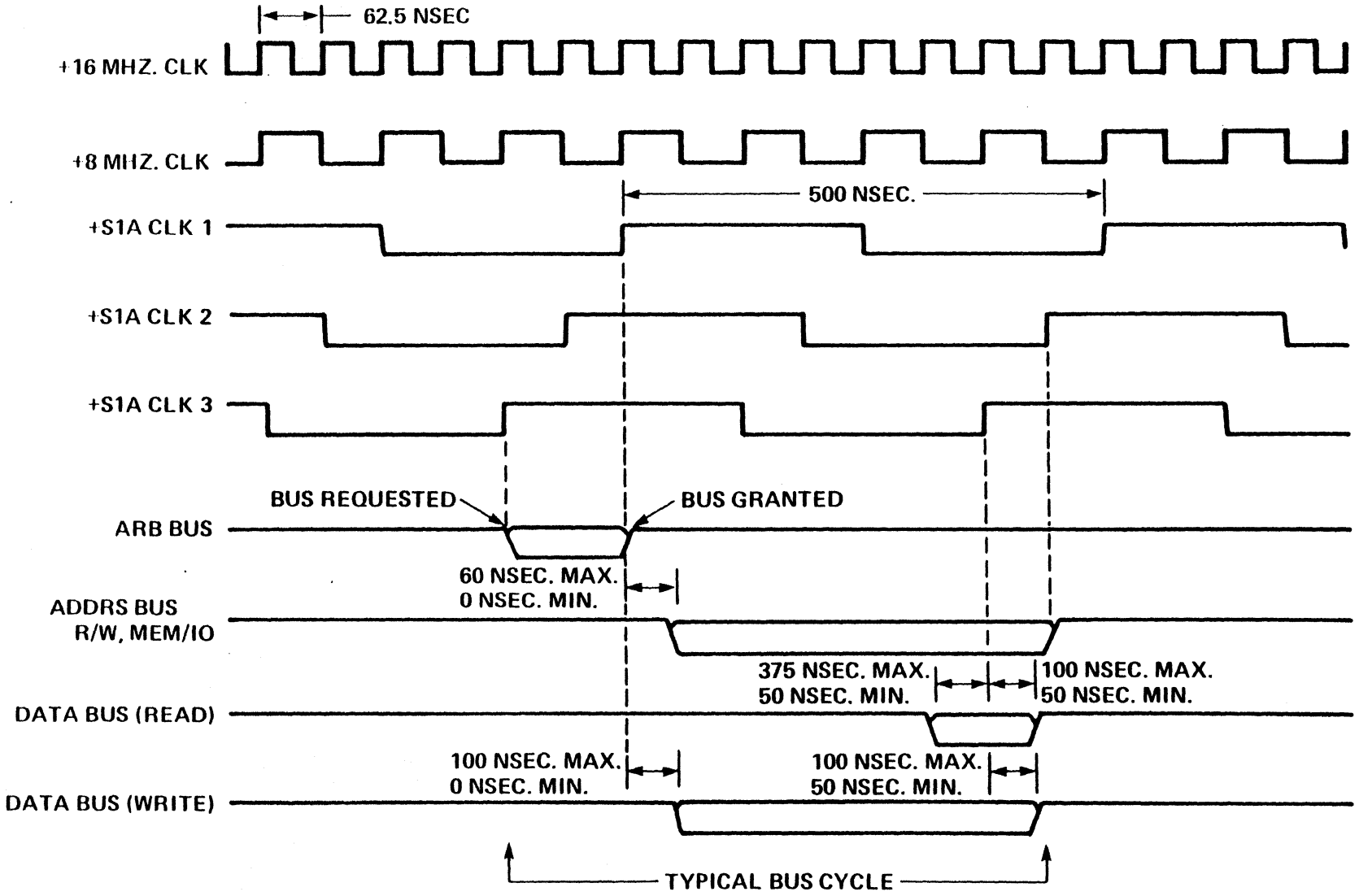
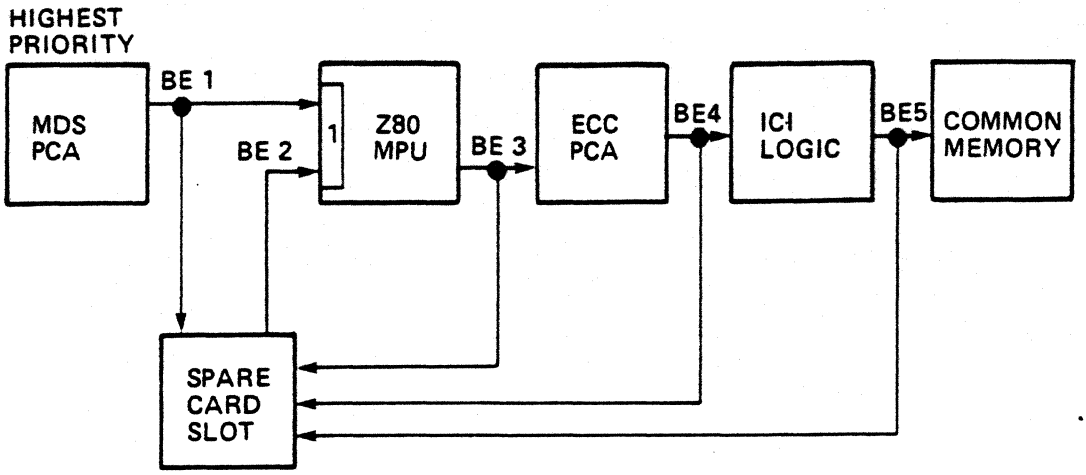


Figure 3-19. SIA Bus Timing Diagram



NOTE:

1. Spare card slot (if used) may steal bus cycles by using BE2 (MDS PCA still has higher priority in this case). The spare card slot may also be used to monitor bus activity, since all five bus enables are wired to this slot.

2. BE5 is wired to Common Memory so that dynamic RAMrefresh can occur during periods of nonactivity on the SIA bus.

Figure 3-20. LD 1200 SIA Bus Priority PB002318-1

When a Bus Master requires control of the SIA Bus, it makes Bus Enable low, preventing all lower priority Bus Masters from acquiring the bus. If a Bus Master of higher priority than the one in control of the bus requires the bus, it makes Bus Enable low. This action gives the higher Bus Master control of the bus. When the higher priority Bus Master releases the bus, the former Bus Master can resume control.

3.4.3.4. IDI Sequences

Communication between the Internal Controller and the Media must be performed on a real-time, sector by sector, basis and must conform to the constraints of the timing generated by the Media. The following subsections describe the timing and sequencing of events on the IDI.

Spindle Power-Up/Power-Down - The Spindle Motor which rotates the Media Disk must be up to operational speed (480 rpm) within three seconds of receiving a Spindle Power Up command. If the Spindle Motor does not attain operating speed within five seconds of the command, the drive logic declares a Motor Speed Fault.

The Spindle must come to a complete stop within three seconds of receiving a Spindle Power Down command. The Unit Ready bit (in Drive Status Register No. 1) goes inactive within one millisecond after the command is received, unless error recovery procedures are in progress.

Sector Interrupt - The Drive provides a Sector Interrupt to the Internal Controller which defines the start of a timing window within each sector (the Command/Status Window). During this window, valid stable drive status can be read by the Internal Controller and it can transfer a new command to the Drive for the upcoming sector operation. The Command/Status Window exists

until the next sector begins.

The worst case timing from one sector to the next is slightly more than 3.8 milliseconds. The Drive is afforded one millisecond at the beginning of each sector to perform its functions (register updating). This leaves a guaranteed window of 2.8 milliseconds for the Internal Controller to perform status and command transfers.

Because the Internal Controller does not know where the sectors on the Media begin and end, its status and command register actions are based on Sector Interrupts. Because sector operations occur in real-time, the Internal Controller must complete sector associated operations within the Command/Status Window.

At the beginning of each sector, the Drive decodes the Sector Mark from the Media, starts a routine which updates drive status registers, and logs any new read or write command received from the Internal Controller. After the command has been logged, status has been prepared for the Internal Controller, Spindle Motor speed has been measured, and the Actual Sector Register has been updated, the Drive activates the Sector Interrupt. At this point, the Internal Controller may read drive status and send the command for the next sector.

Sector Interrupts are present only when the Unit Ready signal is active. When the Unit Ready bit is active, drive status bits are updated only at the beginning of each sector and are stable during the Command/Status Window.

Status Registers - Listed in tables 3-8 through 3-10 are drive status, error, and fault conditions, categorized by their availability and impact on LD 1200 operations. Not all drive status conditions are valid at all times. The validity of a status condition is determined by the states of the Spindle Power Up and Unit Ready bits from the Drive. Drive status conditions and the conditions under which they are valid are listed in table 3-8. Drive error conditions and associated drive responses are listed in table 3-9. Error conditions that can occur during a Write operation to the Media are further defined in table 3-10.

When the Unit Ready bit is inactive, all applicable status (table 3-8, Category 1) is reported by the Drive whenever available. When a fault condition is reported to the Internal controller, that bit remains active until faults are cleared by the Internal Controller. When the Unit Ready bit is active, the Drive updates the status registers only at the beginning of each sector, to ensure that their contents are stable during the Command/Status Window. In this case, some of the device errors that occur are automatically cleared by the Drive, while others are not (refer to the Clearing Errors subsection in this manual for details). When the Unit Ready bit is active, all status reported to the Internal Controller, except the following, refers to the condition of the Drive at the end of the previous sector:

- Read/Write in Progress bit
- Contents of the Actual Sector Register
- Contents of the Header Sector
- Contents of the Header Track LSB and MSB Registers
- Certify Flag Status

Table 3-8. Status Categories

STATUS DESCRIPTION	PORT (HEX)	BIT	CATEGORY		
			1	2	3
Header Sector	12	D4-D0			X
Header Track LSB	13	D7-D0			X
Header Track MSB	14	D7-D0			X
Unit Ready	15	D0		X	
On Track	15	D1			X
Start/Stop Request	15	D2	X		
Device Fault	15	D3	X		
Cartridge Loaded	15	D4	X		
Write Protect Switch	15	D5	X		
Cartridge Write Protected	15	D6	X		
Device Error	15	D7	X		
Rewrite Requested	16	D0			X
Write Not Started	16	D1			X
Laser Degraded	16	D2		X	
Error Recovery In Progress	16	D3		X	
Illegal Seek	16	D4			X
Data Detect	16	D5			X
R/W In Progress	16	D6			X
Eject Enable	16	D7	X		
Power Supply Over Temp	17	D0	X		
Cage Over Temperature	17	D1	X		
Certify Flag	17	D2			X
Seek Error	18	D0			X
Wobble Error	18	D2		X	
Missing Data Field Error	18	D3			X
Overwrite Error	18	D4			X
Verify Header Error	18	D5		X	
DRDW Error	18	D6			X

Table 3-8. Status Categories (continued)

STATUS DESCRIPTION	PORT (HEX)	BIT	CATEGORY 1	CATEGORY 2	CATEGORY 3
Track Miscompare Error	18	D7			X
Focus Error	19	D0			X
Data Synchronization Error	19	D1			X
PLL Error	19	D2			X
Laser Read Power Error	19	D3			X
Laser Write Power Error	19	D4			X
S/DC Parity Error	19	D5	X		
MDS Parity Error	19	D6			X
Tracking Error	19	D7			X
Laser Read Power Fault	18	D0		X	
Laser Write Power Fault	18	D1		X	
Quad Sum High Fault	18	D2		X	
Verify Header Fault	18	D3		X	
Motor Speed Fault	18	D4		X	
MPU Timeout Fault	18	D5	X		
MPU Self-Test Fault	18	D6	X		
Wobble Fault	18	D7		X	
PLL Fault	19	D0		X	
Focus Fault	19	D1		X	
Seek Fault	19	D2		X	
Tracking Fault	19	D3		X	
Line Sync Fault	19	D4	X		
Data Synchronization Fault	19	D5		X	
Quad Sum Low Fault	19	D6		X	
Actual Sector Register	1E	D4-D0			X

Category 1. Status conditions which may be valid regardless of the states of the Spindle Power Up and Unit Ready bits.

Category 2. Status conditions which may be valid only if the Spindle Power Up bit is active. The Drive may or may not be ready.

Category 3. Status conditions which may be valid only if the Spindle is powered up and the Drive is ready.

TBL22

Table 3-9. Error Action Overview

ERROR DESCRIPTION	RESULTING ACTION CATEGORY 1	2	3	4
DRDW Error	X			X
PLL Error	X			X
Data Sync Error	X			X
Verify Header Error		X		
Track Miscompare Error			X	
Overwrite Error			X	
Laser Read Power Error			X	
Seek Error			X	
Focus Error			X	
Tracking Error			X	
Laser Write Power Error			X	
S/DC Parity Error			X	
MDS Parity Error			X	
Missing Data Field Error			X	
Wobble Error			X	

Category 1. Errors that inhibit writing immediately upon detection, but cause a Rewrite in the next sector if the error is resolved and Rewrites are enabled.

Category 2. Errors that are reported to the Internal Controller but cause no action within the Drive.

Category 3. Errors that abort the operation immediately, regardless of other conditions, and must be cleared by the Internal Controller (these errors cause pseudowrites).

Category 4. Errors that may be overridden by the Write Error Override bit in Drive Control Register No. 1.

TBL23

Table 3-10. Write Error Categories

ERROR DESCRIPTION	ERROR CATEGORY 1	ERROR CATEGORY 2
Focus Error	X	
Tracking Error	X	
Laser Read Power Error	X	
Laser Write Power Error	X	
MDS Parity Error	X	
S/DC Parity Error	X	
Missing Data Field Error	X	
Seek Error	X	
Verify Header Error	X	
Wobble Error	X	
Track Miscompare Error	X	
PLL Error		X
DRDW Error		X
Data Sync Error		X
Overwrite Error		X

Category 1. Errors that, if they occur during a Write operation, must be cleared by the Internal Controller and always cause rotational latency.

Category 2. Errors that, if they occur during a Write operation, are cleared by the Drive if Rewrites are enabled. If Rewrites are not enabled, they are handled like Category 1 errors (Internal Controller must clear them).

TBL24

Control Registers - The following three drive registers are loaded with control information by the Internal Controller to control various drive functions:

- Read/Write Control Register, SIA Bus Port 00 hex
- Control Register No. 1, SIA Bus Port 1F hex
- Control Register No. 2, SIA Bus Port 20 hex

The Read/Write Control Register is initialized with 20 hex after a Reset operation, which clears the register of read and write commands. The Drive cannot respond to control register contents loaded within 50 microseconds of a LD 1200 Power-On or Reset operation. Therefore, the Internal Controller must not attempt to load Control Register No. 1 within that period of time.

The bits in the control registers fall into two categories, as shown in table 3-11. Category 1 includes those control bits that may be activated at any time. Category 2 includes those bits that may be activated only during the 2.8-millisecond Command/Status Window.

Table 3-11. Control Bit Categories

CONTROL FUNCTION	PORT (HEX)	BIT	CATEGORY 1	CATEGORY 2
Write Data Field	00	D0		X
Write Vector Address Field	00	D1		X
Write Postfield	00	D2		X
Diagnostic R/W	00	D3		
Read Sector	00	D4		X
Clear R/W Command	00	D5	X	
Long Wrap Test	00	D7	X	
Spindle Power Up	1F	D0	X	
Clear Errors	1F	D1	X	
Report Faults	1F	D2	X	
Enable Jumpbacks	1F	D3	X	
Write Protect	1F	D4	X	
Write Error Override	1F	D5	X	
Latch First Error	1F	D6	X	
Diagnostic Mode	1F	D7	X	
Drive Reset	20	D0	X	
Rewrite Enable	20	D1	X	

Category 1. Control bits that may be activated or deactivated by the Internal Controller at any time.

Category 2. Control bits that may be activated by the Internal Controller only during the Command Status Window (refer to the Sector Interrupt subsection for details).

TBL25

Seek Operations - A Seek operation moves the read/write mechanism in the Carriage from its current position to the desired position for the next data access. Generally, a Seek causes the Carriage to move across tracks to a new location. However, a Seek can be from one sector to another in the same track.

The Internal Controller can initiate a Seek whenever the Unit Ready bit (in Drive Status Register No. 1) is active. The Drive can also initiate a Seek (for a Jumpback, Reseek, etc.) during this time. To avoid contention, a Seek from the Internal Controller is performed in the following sequence:

(1) Load the Desired Sector Register in the Drive.

(2) Wait 15 microseconds.

(3) Check the Desired Track Hi Flag bit. If this bit is high, the Drive is performing a Seek and the Internal Controller must wait until the Drive completes its Seek. If the bit is low, the Internal Controller can load the Desired Track Hi and Low Registers. Loading the Desired Track Low Register initiates the Seek.

When the Seek is complete and the Drive is synchronized, the On Track signal becomes active. Synchronization involves the detection of at least one Sector Mark and the verification of at least one Header Address. After a Seek is complete, the On Track signal is not sampled again until the desired Track Low Flag bit is made low.

If a Seek is requested while a Read or Write operation is in progress, the Seek does not take place until the operation is complete. The Internal Controller should not initiate a Seek when an error or fault condition exists in the Drive or when a Read or Write operation is in progress.

Jumpback Operations - To enable the spiral structure of the Media tracks to appear as concentric circles to the Host, the Jumpback operation causes the Carriage to perform a one-track backward Seek at a predetermine point. The Drive allows the Internal Controller to specify whether Jumpbacks are to be performed during idle periods (no Read, Write, or Seek operations in progress).

A Jumpback starts in the sector following the one specified by the desired Sector Register, if a Read, Write, or Seek operation has not been started by that time. When the Internal Controller finishes a Read, Write, or Seek, the Drive reinstates the Jumpback feature (if enabled by the Internal Controller). In this case, the point where the Jumpback occurs is determined as follows:

- If the last sector written or read was greater than the contents of the Desired Sector Register and was not the last sector on the track, the Jumpback occurs immediately. Jumpbacks then continue at the sector following the desired sector on the track where the operation completed.

- If the last sector written or read was greater than the contents of the Desired Sector Register and was the last sector on the track, the Jumpback occurs when the desired sector plus one is reached on the next track.

- If the last sector written or read was less than or equal to the contents of the Desired Sector Register, the Jumpback occurs one sector after the desired sector on the current track.

Clearing Errors - When a device error occurs, the corresponding status bit is latched into the appropriate register (refer to Status Register descriptions in IDI Interface Sequences subsection). The bit remains active until the Internal Controller clears the error condition, a Reset occurs, or the Drive automatically clears the condition (refer to table 3-10, Category 2). Automatic clearing of errors by the Drive occurs when Rewrites are enabled and PLL, DRDW, Data Sync or Overwrite errors, are encountered. Under these conditions, the Drive reports the error(s) which caused the Rewrite only during the Command/Status Window for that sector. The errors are cleared and new status posted for the sector in which the Rewrite occurred. For this reason, the internal controller must maintain a cumulative record of the error status reported so that error conditions causing the rewrites can be reported to the Host.

Errors are cleared within one millisecond of the activation of the Clear Errors command, assuming an error recovery procedure is not in progress.

If the Internal Controller is performing a Write operation to the Media and an error occurs that aborts writing (refer to table 3-9, Category 3), the Internal Controller must abort the operation before clearing the errors, to prevent enabling the Laser Diode for a pseudowrite.

Drive Reset - When high, the Drive Reset bit (in Control Register No. 2) causes the Drive to perform the initialization routine performed during Power Up. The Drive is kept in a Reset state while this bit is high (active) and begins initialization when the bit goes low. Drive status registers are initialized during the first part of the initialization routine and become stable within 50 microseconds of the trailing edge of the Reset pulse. The contents of the status registers are not valid during the 50-microsecond period. Therefore, Control Register No. 1 (SIA Bus Port 1F hex) is not loaded by the Internal Controller during this 50-microsecond period (refer to Control Register descriptions in the IDI Bus Sequences subsection).

3.4.3.5. Track and Sector Identification Registers

When the Drive is in a Ready state (Spindle Motor is up to speed, no drive faults exist, and Sector Interrupts present), it reads the contents of each Sector Header from the Media, regardless of whether a command has been issued by the Internal Controller. The Drive uses the information in the header to establish data synchronization, track centering, and sector location. During the Command/Status Window, the MDS PCA reads track and sector identification (contained in the header) and transfers it to registers in the Servo/Drive Control PCA (SIA Bus Ports 12, 13, and 14 hex). After a Sector Interrupt is received, the Internal Controller can monitor the track and sector location by reading the contents of these registers. The Servo/Drive Control PCA filters the sector identification value from the Media and provides the new value to the Internal Controller via the Actual Sector Register (SIA Bus Port 1E hex). Filtering of the sector identification is necessary to compensate for errors that can occur while the header is being read.

Refer to the Dual Port RAM description in the Servo/Drive Control PCA subsection of this manual for detailed information on the track and sector identification registers.

3.4.3.6. Read/Write Command Registers

The Read/Write Command Registers (located on the MDS PCA) control the operation of the Read/Write Channel. These registers are described in the following subsections:

Read/Write Control Register, SIA Bus Port 00 Hex - The Read/Write Control Register is used by the Internal Controller to specify what Read or Write operation is to be performed in the next sector in sequence. This register is loaded during the Command/Status Window of the sector prior to the one in which the Read or Write operation is to take place.

NOTE

If the Internal Controller fails to issue a new command during the Command/Status Window, the Drive goes into an Idle mode.

At the beginning of each sector, the Drive relocates (logs) the contents of the Read/Write Control Registers into an internal register, making the Read/Write Control Register available for the next command from the Internal Controller.

If an error that causes an automatic Rewrite occurs during a Write operation, it is not necessary for the Internal Controller to reissue the command for the sector being written. The Drive retains the pending command and executes it when the Rewrite operation completes successfully. In the case of a Rewrite operation, the Internal Controller need only monitor the Rewrite Request bit to determine when a Rewrite operation is being attempted.

If the Internal Controller inadvertently requests both a Read and Write operation, the Drive executes the Read command.

Write activity can be terminated immediately by setting the Clear Read/Write Command bit in the Read/Write Control Register.

The Read/Write Control Register is configured as follows:

Bit 0	Write Data Field and associated Write Protect and Write Complete Bytes
Bit 1	Write Vector Address Field and associated Write Protect and Write Complete Bytes
Bit 2	Write Postfield and associated Write Protect and Write Complete Bytes
Bit 3	Diagnostic Read/Write
Bit 4	Read Sector
Bit 5	Clear Read/Write Command
Bit 6	Reserved
Bit 7	Long Wrap Test (diagnostic)

Refer to the SIA Interface description in the Modulator Demodulator Synchronizer PCA subsection for detailed information.

DRDW Threshold Register, SIA Bus Port 02 Hex - This register is used to specify the number of Direct Read During Write (DRDW) errors that are allowed to occur, during the Write of a sector, before the Drive declares a DRDW error. If the Drive encounters the number of errors specified in the DRDW Threshold Register, the Write operation is terminated and a Rewrite operation is attempted in the next sector, if authorized.

The DRDW threshold value for the Data Field is also used in processing write errors. The Drive declares the presence of data in the Data Field when the number of correctly decoded bytes from the Media equals or exceeds the DRDW threshold value.

The DRDW Threshold Register is configured as follows:

Bits 0 through 3	DRDW Threshold for the Data Field
Bits 4 through 7	DRDW Threshold for the Vector Address Field and Postfield

Refer to the SIA Interface description in the Modulator Demodulator Synchronizer PCA subsection for detailed information.

3.4.3.7. Drive Status and Control Registers

The Drive Status Registers are used to accumulate status information from various areas of the Drive for use by the Drive and Internal Controller. The Drive Control Registers are used in the transfer of commands from the Internal Controller to the Drive. Commands loaded into these registers control Drive operations other than reading and writing data. The Drive Status and Control Registers are located on the Servo/Drive Control PCA.

Status Bits that pertain to the ongoing operation of the Drive are updated at the beginning of each sector and are read by the Internal Controller during the Command/Status Window following each Sector Interrupt. When the Drive is in the Ready state, error and fault status read by the Internal Controller pertain to the previous sector. When the Drive is not Ready, error and fault status are subject to change at any time.

SIA Bus Ports 10 through 1F hex are registers that can be both written into and read from by the Drive. SIA Bus Ports 20 through 22 hex can only be written into by the Internal Controller and read from by the Drive. Ports 10 and 11 hex are flag registers which contain flag bits for each of Ports 12 through 1F hex.

The flag bits enable the exchange of information between the Internal Controller and the Drive to be controlled in a handshake manner. When a bus module writes to an interface register, the flag bit corresponding to that register is automatically set. When the exchange of information is complete, the receiving bus module has responsibility for resetting the flag bit. To reset one flag bit in a register, a ZERO is written to the bit and ONEs are written to the remaining bits in the register. Flag bits can be cleared directly by the Internal Controller, but not set by it.

The individual Drive Status and Control Registers are described briefly in the following subsections. For more detailed information, refer to the Dual Port RAM description in the Servo/Drive Control PCA subsection of this manual.

Flag Register No. 1, SIA Bus Port 10 Hex - This register contains flags for each of Ports 12 through 17 hex, configured as follows:

Bit 0	Reserved for system use (must be ZERO)
Bit 1	Reserved for system use (must be ZERO)
Bit 2	Port 12 hex Flag Bit (Header Sector)
Bit 3	Port 13 hex Flag Bit (Header Track LSB)
Bit 4	Port 14 hex Flag Bit (Header Track MSB)
Bit 5	Port 15 hex Flag Bit (Status Register No. 1)
Bit 6	Port 16 hex Flag Bit (Status Register No. 2)
Bit 7	Port 17 hex Flag Bit (Status Register No. 3)

Flag Register No. 2, SIA Bus Port 11 Hex - This register contains the flags for each of Ports 18 through 1F hex, configured as follows:

Bit 0	Port 18 hex Flag Bit (Error/Fault Register No. 1)
Bit 1	Port 19 hex Flag Bit (Error/Fault Register No. 2)
Bit 2	Port 1A hex Flag Bit (Error/Fault Register No. 3)
Bit 3	Port 1B hex Flag Bit (Desired Sector)
Bit 4	Port 1C hex Flag Bit (Desired Track Lo)
Bit 5	Port 1D hex Flag Bit (Desired Track Hi)
Bit 6	Port 1E hex Flag Bit (Actual Sector)
Bit 7	Port 1F hex Flag Bit (Control Register No. 1)

Header Sector Register, SIA Bus Port 12 Hex - When the Drive is in Ready, this register contains the sector number read from the last Sector Header. The register is configured as follows:

Bits 0 through 4	Sector Number
Bits 5 through 7	Not used

Header Track LSB Register, SIA Bus Port 13 Hex - When the Drive is in Ready, this register contains the Track Least-Significant Byte read from the last Sector Header.

Header Track MSB Register, SIA Bus Port 14 Hex - When the Drive is in Ready, this register contains the Track Most-Significant Byte read from the last Sector Header.

Status Register No. 1, SIA Bus Port 15 Hex - This register contains status bits which describe the present condition of the Drive. The register is configured as follows:

Bit 0	Unit Ready
Bit 1	On Track
Bit 2	Start/Stop Request
Bit 3	Device Fault
Bit 4	Cartridge Loaded
Bit 5	Write Protect Request
Bit 6	Cartridge Write Protected
Bit 7	Device Error

Status Register No. 2, SIA Bus Port 16 Hex – This register contains status bits which describe the present condition of the Drive. The register is configured as follows:

Bit 0	Rewrite Requested
Bit 1	Write Not Started
Bit 2	Laser Degraded
Bit 3	Error Recovery in Progress
Bit 4	Illegal Seek
Bit 5	Data Detect
Bit 6	Read/Write in Progress
Bit 7	Eject Enabled

Status Register No. 3, SIA Bus Port 17 Hex – This register contains status bits which describe the present condition of the Drive. The register is configured as follows:

Bit 0	Power Supply Overtemperature
Bit 1	Cage Overtemperature
Bit 2	Certify Flag
Bits 3 through 7	Reserved For Future Use

Error Register No. 1, SIA Bus Port 18 Hex – This register contains status bits which define various device error or fault conditions within the Drive. Error status is available in this register only when the Report Faults bit is ZERO (Control Register No. 1, Bit 2). Error Register No. 1 is configured as follows:

Bit 0	Seek Error
Bit 1	Reserved For Future Use
Bit 2	Wobble Error
Bit 3	Missing Data Field
Bit 4	Overwrite Error
Bit 5	Verify Header Error
Bit 6	DRDW Error
Bit 7	Track Miscompare Error

Error Register No. 2, SIA Bus Port 19 Hex – This register contains status bits which define various device error or fault conditions within the Drive. Error status is available in this register only when the Report Faults bit is ZERO (Control Register No. 1, Bit 2). Error Register No. 2 is configured as follows:

Bit 0	Focus Error
Bit 1	Data Synchronization Error
Bit 2	PLL Error
Bit 3	Laser Read Power Error
Bit 4	Laser Write Power Error
Bit 5	S/DC Parity Error
Bit 6	MDS Parity Error
Bit 7	Tracking Error

Error Register No. 3, SIA Bus Port 1A Hex – This register contains status bits which define various device error or fault conditions within the Drive. Error status is available in this register only when the Report Faults bit is ZERO (Control Register No. 1, Bit 2). All the bits in Error Register No. 3 are reserved for future use.

Fault Register No. 1, SIA Bus Port 18 Hex – This register contains status bits which define various device fault or error conditions within the Drive. Fault status is available in this register only when the Report Faults bit is ONE (Control Register No. 1, Bit 2). Fault Register No. 1 is configured as follows:

Bit 0	Laser Read Power Fault
Bit 1	Laser Write Power Fault
Bit 2	Quad Sum High Fault
Bit 3	Verify Header Fault
Bit 4	Motor Speed Fault
Bit 5	MPU Timeout Fault
Bit 6	MPU Self-Test Fault
Bit 7	Wobble Fault

Fault Register No. 2, SIA Bus Port 19 Hex – This register contains status bits which define various device fault or error conditions within the Drive. Fault status is available in this register only when the Report Faults bit is ONE (Control Register No. 1, Bit 2). Fault Register No. 2 is configured as follows:

Bit 0	PLL Fault
Bit 1	Focus Fault
Bit 2	Seek Fault
Bit 3	Tracking Fault
Bit 4	Line Sync Fault
Bit 5	Data Synchronization Fault
Bit 6	Quad Sum Low Fault
Bit 7	Reserved For Future Use

Fault Register No. 3, SIA Bus Port 1A Hex – This register contains status bits which define various device fault or error conditions within the Drive. Fault status is available in this register only when the Report Faults bit is ONE (Control Register No. 1, Bit 2). All the bits in Fault Register No. 3 are reserved for future use.

Desired Sector Register, SIA Bus Port 1B Hex – This register is loaded with the number of the sector to be written to or read from in a subsequent data Write or Read operation. The Desired Sector Register is also used to determine On-Track Status associated with a Seek operation. The register is configured as follows:

Bits 0 through 4	Desired Sector Number
Bits 5 through 7	Not used (must be ZERO)

Desired Track Registers, SIA Bus Ports 1C and 1D Hex – These registers are loaded with the number of the target track for a Seek operation. The registers are configured as follows:

Port 1C hex:

Bits 0 through 7	Lower half of the target track address

Port 1D hex:

Bits 8 through 13	Upper half of the target track address
Bit 14	Sign bit. Specifies track location relative to the start of the User Data Band.

Actual Sector Register, SIA Bus Port 1F Hex - This register contains the computed sector address and a sequential sector bit. The contents of this register are valid only when the On Track signal from the Drive is active. The register is configured as follows:

Bits 0 through 4	Actual Sector
Bits 5 and 6	Reserved For Future Use
Bit 7	Sequential Sectors

Control Register No. 1, SIA Bus Port 1F Hex - This register is loaded by the Internal Controller with commands to control various Drive functions. The register is configured as follows:

Bit 0	Spindle Power-Up
Bit 1	Clear Errors
Bit 2	Report Faults
Bit 3	Enable Jumpbacks
Bit 4	Write Protect
Bit 5	Write Error Override
Bit 6	Latch First Error
Bit 7	Diagnostic Mode

Control Register No. 2, SIA Bus Port 20 Hex - This register is loaded by the Internal Controller with commands to control various Drive functions. The register is configured as follows:

Bit 0	DOD Drive Reset
Bit 1	Rewrite Enable
Bits 2 through 7	Reserved For Future Use

Power Supply Margin Control Register, SIA Bus Port 21 Hex - This register is used by the Internal Controller for diagnostic purposes. Using the register, the Internal controller can select high and low dc power margins to test Drive circuits. The register is configured as follows:

Bit 0	-5-Vdc Margin Test Enable	
Bit 1	+5-Vdc Margin Test Enable	
Bit 2	-12-Vdc Margin Test Enable	
Bit 3	+12-Vdc Margin Test Enable	
Bit 4	-5-Vdc Margin Control	1 = -5% Margin
Bit 5	+5-Vdc Margin Control	
Bit 6	-12-Vdc Margin Control	0 = +5% Margin
Bit 7	+12-Vdc Margin control	

Clear Sector Interrupt Register, SIA Bus Port 22 Hex - Writing to this register clears the Sector Interrupt.

Device Address Switches Register, SIA Bus Port EA Hex - This optional register is not implemented in the Drive.

3.5. LD 1200 ADAPTER PCA

The SCSI PCA (also known as the Internal Controller Interface PCA or ICI PCA) is the resident controller in the LD 1200. This subsection describes SCSI PCA theory of operation in terms of the four major functions implemented on the PCA:

- Microprocessor (MPU) Control: The MPU is the controller for both internal and external interface operations. The Z80B[1] is the microprocessor used on the SCSI PCA.
- SCSI Interface Control: The Small Computer System Interface (SCSI) provides the external Host-to-LD 1200 interconnection. Interface functions are implemented primarily by the SCSI Interface Circuit under MPU control.
- System Interface Assembly (SIA) Bus Timing Circuit: Communication between PCAs in the LD 1200 is primarily performed via the SIA Bus. These exchanges are synchronized via three SIA Bus clocks. SIA Bus clocks are also used by SCSI control logic to synchronize DMA operations to Common Memory (64K RAM) on the Error Correction and Common Memory Unit Interface PCA (ECC PCA).
- Maintenance and Operator Panel External Registers: These registers record and report switch and keypad conditions and are used to control associated indicators on the Maintenance and Operator Panels.

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1. Z80B is a registered trademark of Zilog Inc.

The SCSI PCA performs device controller functions for the Drive. The MPU controls information transfer in and out of the LD 1200. Data is sent to and from the Common Memory data buffer via Direct Memory Access controlled by the MPU.

All SCSI functions, such as Arbitration, Selection, and Information Transfer are implemented by the SCSI PCA. These SCSI functions are described in detail in the Small Computer System Interface subsection of this manual. The SCSI interface is an American National Standard interface, and is described in detail in American National Standard specification ANSC X3T9.2.

The functional block diagram of the SCSI PCA is shown in figure 3-21. Descriptions of the interface signals and the functional blocks shown in the illustration are provided in the following subsections.

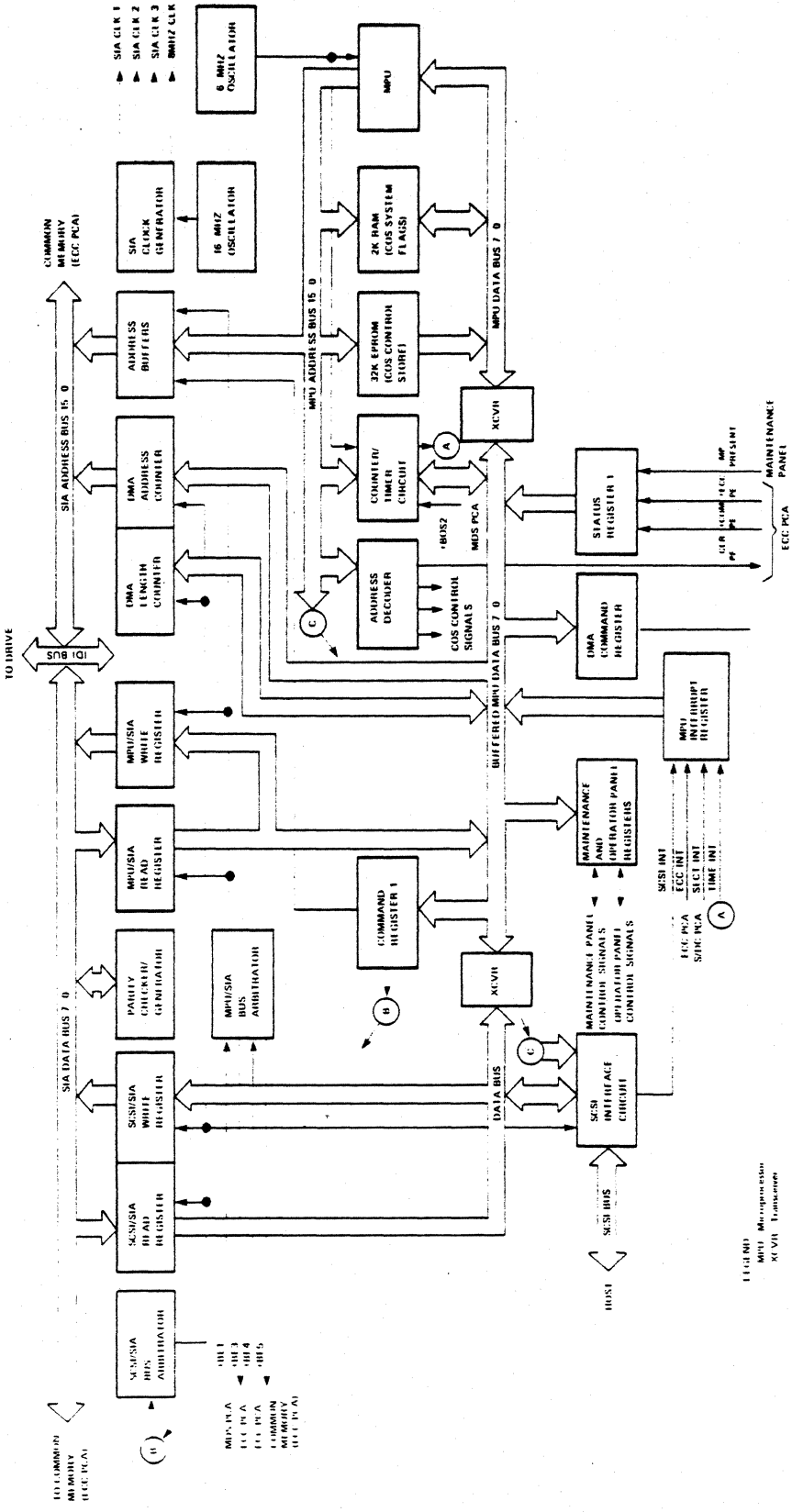


Figure 3-21. LD 1200 SCSI Adapter PCA Block Diagram

3.5.1. Interface Signals

The SCSI PCA interfaces with the Host and other LD 1200 functions using the following signals (refer to figure 3-13):

SCSI BUS

The SCSI Bus includes the following signals:

- BSY (Busy)
- SEL (Select)
- C/D (Command/Data)
- I/O (Input/Output)
- MSG (Message)
- REQ (Request)
- ACK (Acknowledge)
- ATN (Attention)
- RST (Reset)
- DB7 through DB0, DBP (Data Bus, Data Bus Parity)

These signals are described in the Small Computer System Interface subsection of this manual.

IDI/SIA BUS

The IDI/SIA Bus includes the following signals:

- +SIA R/W (Read/Write)
- +SIA MEM I/O (Memory-I/O Transfer)
- -SIA RESET
- +CLK1, +CLK2, +CLK3 (SIA Bus Clocks)
- +SIA D0 through +SIA D7 (SIA Data Bus)
- +SIA DATA PARITY
- +SIA ADRS0 through +SIA ADRS15 (SIA Address Bus)

These signals are described in the Internal Device Interface/System Interface Assembly subsection of this manual.

+BE1 (Bus Enable Out 1)

This signal is generated by the Modulator Demodulator Synchronizer (MDS) PCA. It is made low by the MDS PCA to take control of the SIA Bus.

+BE3 (Bus Enable Out 3)

This signal is output to the ECC PCA. It is made low by the MPU to take control of the SIA Bus.

+BE4 (Bus Enable Out 4)

This signal is generated by the ECC PCA. When this signal is high, the SCSI PCA may perform a DMA operation to access Common Memory via the IDI/SIA Bus.

+BE5 (Bus Enable Out 5)

This signal is output to Common Memory (on the ECC PCA). When this signal is high, the IDI/SIA Bus is not requested, and the Dynamic Memory Controller issues a Refresh command.

NOTE

Refer to the Bus Module Priority System subsection of this manual for information on the use of +BE1, +BE3, +BE4, and +BE5 for SIA Bus arbitration.

MAINTENANCE PANEL CONTROL SIGNALS

These signals are used for monitoring of switches and control of indicators on the Maintenance Panel. Refer to the Operator and Maintenance Panel External Registers subsection in this manual for descriptions of these signals.

OPERATOR PANEL CONTROL SIGNALS

These signals are used for monitoring of switches and control of indicators on the Operator Panel. Refer to the Operator and Maintenance Panel External Registers subsection in this manual for descriptions of these signals.

-ECC INT (ECC Interrupt)

This signal is generated by the ECC PCA. When low, this signal indicates the ECC PCA has sent an interrupt to the MPU.

-SECT INT (Sector Interrupt)

This signal is generated by the Servo/Drive Control (S/DC) PCA. When low, this signal indicates sector status is ready to be read. The SCSI PCA acknowledges the interrupt and clears it after the status has been read.

+BOS2 (Beginning of Sector Pulse)

This signal is generated by the MDS PCA. When high, this signal indicates the start of a sector.

-CLR PE (Clear ECC Parity Error)

This signal is output to the ECC PCA. When low, this signal clears parity errors on the ECC PCA.

+COM PE (Common Memory Parity Error)

This signal is generated by ECC PCA. When high, this signal indicates that an error has been detected in data being sent to Common Memory.

+ECC PE (ECC Parity Error)

This signal is generated by the ECC PCA. When high, this signal indicates one of the following has occurred:

- A parity error was detected in a command received from the SCSI PCA.
- A parity error was detected in data written into the Bank 1 Index Register on the ECC PCA.
- A parity error was detected in data read from Common Memory by the Error Correction Unit.

-MP PRESENT (Maintenance Panel Present)

This signal is generated by the Maintenance Panel. When low, this signal indicates a Maintenance Panel is installed in the Drive and must be included in the normal polling process.

3.5.2. I/O Ports

Data movement and various control functions are managed by means of I/O Ports on the SCSI PCA. The functions of these ports can vary depending on whether they are being read or written into by the MPU.

I/O Ports are divided into five groups, as shown in table 3-12. Detailed descriptions of the ports are provided in the following subsections:

- SCSI Ports: SCSI Interface Circuit subsection
- CTC Ports: MPU Timing Control subsection

- SIA/SCSI Control Ports:
  - DMA Address and Byte Count Registers: SCSI/Common Memory Direct Memory Access subsection
  - Status Register 1: Status Register 1 (Port Read-94 hex) subsection
  - Command Register 1: Command Register 1 (Port Write-97 hex) subsection
  - DMA Command Registers: SCSI/Common Memory Direct Memory Access subsection
- Display Panel Ports: Operator and Maintenance Panel External Registers subsection
- Device Address Switch Port: Operator and Maintenance Panel External Registers subsection

Table 3-12. SCSI I/O Port Definitions

PORT NUMBER (HEX)	DESCRIPTION	
	READ	WRITE
	SCSI PORTS	
80	Current SCSI Data	Output Data Register
81	Initiator Command Register	Initiator Command Register
82	Mode Register	Mode Register
83	Target Command Register	Target Command Register
84	Current SCSI Bus Status	Select Enable Register
85	Bus and Status Register	Start DMA Send
86	Input Data Register	Start Target Receive DMA
87	Clear Parity and Interrupts	Start Initiator Receive DMA
	CTC PORTS	
88	Software Timer Port 0	Software Timer Port 0
89	Software Timer Port 1	Software Timer Port 1
8A	Software Timer Port 2	Software Timer Port 2
8B	Software Timer Port 3	Software Timer Port 3
	SIA/SCSI CONTROL PORTS	
90	Not used	DMA Address Register 0 - 7
91	Not used	DMA Address Register 8 - 15
92	DMA Byte Count 0 - 7	DMA Byte Count 0 - 7
93	DMA Byte Count 8 - 11	DMA Byte Count 8 - 11
94	Status Register 1	
96	Clear ECC Parity Errors	
97		Command Register 1
98	Not used	DMA Command Register
	DISPLAY PANEL PORTS	
94		Operator Panel Hexadecimal Display Register
95		Maintenance Panel LED Register
96		Maintenance Panel Hexadecimal Display Register
97	Maintenance Panel Keyboard Register	
95	Device Address Switch Register	

3.5.3. Microprocessor Control

The MPU and associated support circuits control data flow to and from the Host, Common Memory, and the Operator and Maintenance Panels. MPU control is implemented by the following:

- MPU Memory Control System:
  - 32K Erasable and Programmable Read-Only Memory (EPROM, referred to functionally as the ROM) which is the Control Store area where Command Operating System (COS) microcode resides.
  - 2K Random-Access Memory (RAM) which is a scratchpad used by the COS for volatile system status flags.
- MPU Address Bus and SIA Address Bus: These two buses are used in conjunction, for Common Memory requests and I/O Port accesses which are external to the SCSI PCA.
- Address Decoder: This circuit decodes MPU Address Bus inputs to produce control signals for I/O Port selection.
- MPU Timing Control:
  - MPU System Clock, 6-MHz Oscillator.
  - Programmable Counter/Timer Circuit (Z8430 CTC) for software timing operations.
- MPU Interrupt Register:
  - ECC Interrupt
  - SCSI Interrupt
  - Sector Interrupt
  - Timer Interrupt

The MPU and associated circuits are shown in figure 3-22. Descriptions of the functions performed by these circuits are given in the following subsections.

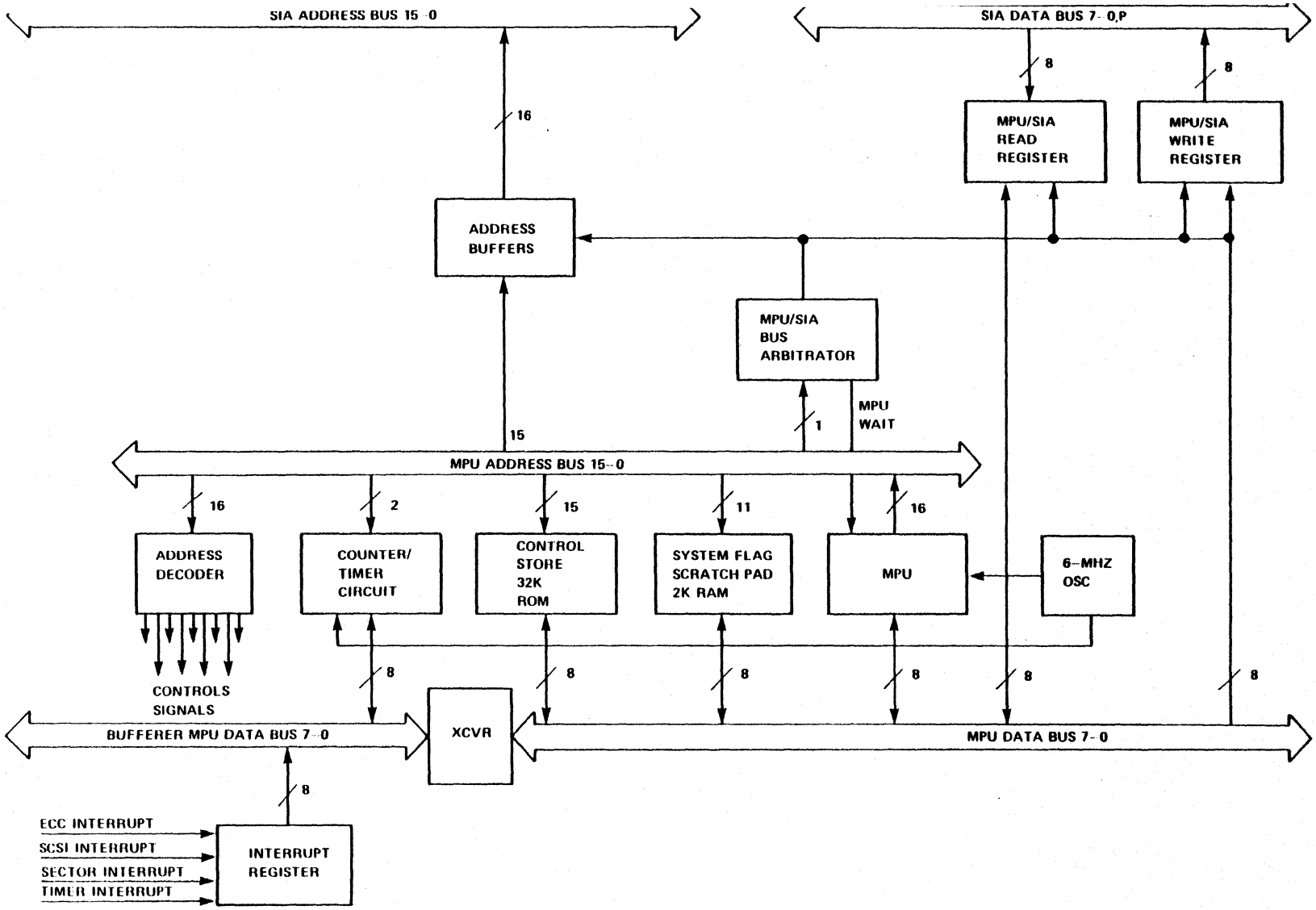


Figure 3-22. Microprocessor Control

PB002352

3.5.3.1. MPU Memory Control System

Basically, the MPU has two buses: the MPU Data Bus (7 through 0), within the PCA, and the MPU Address Bus (15 through 0). The 16-bit unidirectional address bus is connected within the MPU to address pointers and the program counter. This bus communicates with the Counter/Timer Circuit, ROM, RAM which stores control data, Address Decoder, MPU/SIA Arbitrator, and the 16-bit SIA Address Bus.

Although the MPU communicates with more than one type of memory (RAM, ROM), memory selection circuitry provides a complete 64-kilobyte addressing capability. The MPU Memory Map in figure 3-23 shows the addressing plan for the MPU Address Bus.

The MPU has a 64K address range. The lower half of this range, addresses 0000 through 7FFF hex, accesses the operating system Control Store (firmware ROM) and scratchpad RAM. Addresses 8000 through FFFF hex access either the upper or lower half of Common Memory located on the ECC PCA, via the SIA Address Bus.

The lower 30k of the MPU address range access the lower 30K of the 32K-by-8-bit Control Store ROM where Command Operating System firmware and diagnostic programs reside. The upper 2K of the ROM is overlayed with a 2K-by-8-bit static scratchpad RAM after power-up. Addresses 7800 through 7FFF hex thus access either ROM or RAM.

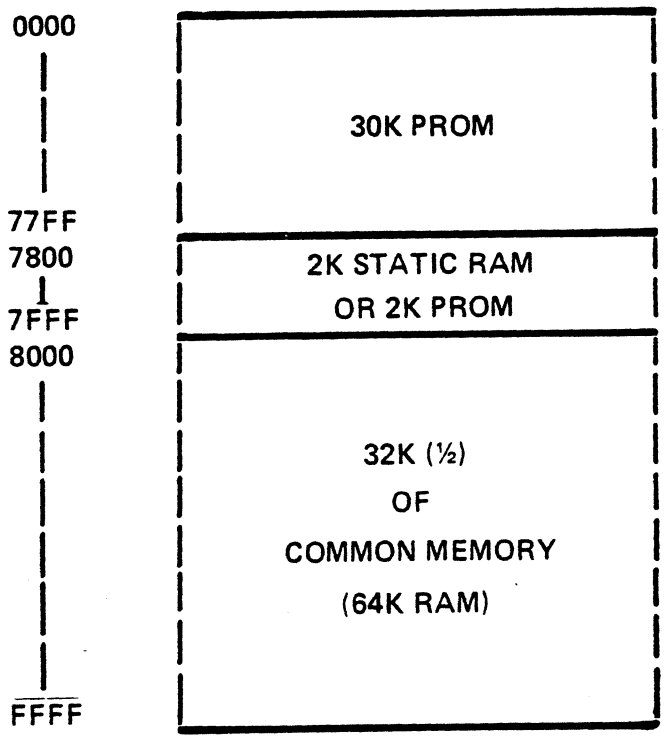


Figure 3-23. MPU Memory Map

During normal operation, COS uses the RAM scratchpad memory to buffer alterable operating system flags that are written to and read by the MPU. COS firmware modules exchange information with each other via the system flags residing in the scratchpad RAM.

The 2K-ROM hidden behind the scratchpad RAM is accessible to the unit only during initialization. This ROM contains power-up diagnostic code. After power-up tests pass, COS switches to the scratchpad RAM for normal Drive operations. This ROM/RAM exchange is controlled by bit 6 of SCSI Command Register 1 (I/O Port Write-97 hex).

The upper 32K of the MPU address range accesses either the upper or lower half of Common Memory, the 64K-RAM on the ECC PCA. COS views either the upper or lower half of Common Memory, as controlled by Bit 7 of Command Register 1 (I/O Port Write-97 hex). When bit 7 is cleared, the lower half is viewed. This is the default condition on MPU reset.

3.5.3.2. MPU/SIA Address Buses

Both the MPU Address Bus and the SIA Address Bus are 16-bit buses. Address buffers route MPU addresses onto the SIA Bus, when enabled by the MPU/SIA Bus Arbitrator.

MPU addresses are enabled onto the SIA Bus for Common Memory requests and I/O Port accesses that are external to the PCA (excluding Operator and Maintenance Panels). When transferring data to Common Memory, the address bus defines the required memory location. When accessing an I/O Port on another PCA, the transfer is to one of the other SIA Bus modules and the address bus is encoded with the desired module and register location.

All Common Memory requests are in the upper address range (8000 through FFFF hex). When Bit 15 of the address bus is high, and the MPU is performing a memory cycle, a Common Memory location is specified and a SIA Bus request is automatically generated. SIA Bus requests are also made for all external I/O Ports by the MPU/SIA Bus Arbitrator.

The MPU/SIA Bus Arbitrator handles requests for the SIA Bus via the SIA Bus daisy-chain priority scheme. When the MPU is granted the SIA Bus, the address bus and data bus buffers are enabled. Either the MPU/SIA Read Register or MPU/SIA Write Register is enabled depending on the operation required (write or read). The address and data are simultaneously enabled to these registers. The transaction is completed during the bus cycle, while arbitration is in progress for the next bus cycle.

During the bus cycle, the MPU is in a Wait state; the arbitrator gives bus access back to the MPU by raising the Wait line. While in the Wait state, data and address values the MPU has queued remain stable.

The Wait signal puts the MPU on real-time hold. This allows synchronization of the 16-MHz oscillator with the asynchronous timing of the SIA Bus. The Wait signal goes low when the MPU is granted control of the bus. The MPU then continues executing the interrupted operational sequence.

The MPU/SIA Write Register enables data onto the SIA Bus at the appropriate time. Data coming in is latched on a Read operation from the SIA Data Bus. At the end of the bus cycle, the data is available and must be latched or lost. When the MPU exits the Wait state, it continues operation, sensing and accepting data.

3.5.3.3. Address Decoder

The Address Decoder is a general purpose circuit that takes MPU Address Bus inputs and converts them to control signals to select I/O ports. When a particular I/O Port is addressed, 3-to-8 decoders in this circuit generate the control signals to select the appropriate register. The register is either read, or written into, under COS control.

3.5.3.4. MPU Timing Control

MPU timing is supplied by a Programmable Counter/Timer Circuit (Z8430 CTC) that is used for various software timing operations. This circuit has four independently programmable 8-bit ports. Each port can be set with a time constant from 1 to 256 by the MPU. The MPU clock is provided by the 6-MHz Oscillator (167-ns cycle).

Each port can run in either the timer mode or counter mode. In the timer mode, the 8-bit counter is clocked from 1 to 256 by a prescaled MPU system clock. The input clock to the timer can be selected by MPU software to divide by 16 or 256.

In the counter mode, the counter is incremented from an external trigger source without prescaling. This mode times asynchronous events. The Command Operating System accesses Software Timer Ports 0 through 3 to clock normal system events. If a normal system event is not accomplished within predetermined time limits, COS stops the operation with a system timeout.

COS Timer Port 0 (Port Read/Write-88 hex) - COS Timer Port 0 is configured in the timer mode. The 6-MHz (167 ns) local clock input is prescaled (expanded) by 256. The counter time constant delay of 256 expands the signal further. This port produces a 10.92-ms free-running clock which is the timing input for the remaining software timer ports.

COS Timer Ports 1 and 2 (Ports Read/Write-89 and -8A hex) - COS Timer Ports 1 and 2 run in the counter mode. They divide the 10.92-ms output clock from COS Timer Port 0 by 256. This produces a timing range of from 0 to 2.8 seconds. COS Timer Port 1 clocks system events. COS Timer Port 2 is identical to COS Timer Port 1, and is used as a second timing reference. The output of COS Timer Port 2 is connected to the trigger input of COS Timer Port 3 (Port Read/Write-8B hex). These ports are used to flash the Maintenance Panel and Operating Panel displays at a 1-Hz rate.

COS Timer Port 3 (Port Read/Write-8B hex) - This port runs in the counter mode. It divides the 2.8-second output clock from COS Timer Port 2 by 256 to produce a maximum timing value of 11.9 minutes for timing system events. COS uses this port for timing lengthy timeouts such as the 10-second error-recovery-in-progress limit.

3.5.3.5. MPU Interrupt Register

There are four sources of interrupts at the MPU; the Sector Interrupt from the Drive, the ECC Interrupt (indicating completion of an assigned task), the SCSI Interrupt, and the Timer Interrupt from the Counter Timer circuit. Any of these interrupts causes a maskable interrupt of the MPU. When the MPU acknowledges the interrupt(s), an 8-bit interrupt vector is placed on the MPU Data Bus. This interrupt vector has the following format:

Bits 5 through 7	=	ZERO (grounded permanently)
Bit 4	=	Timer Interrupt (active low)
Bit 3	=	Sector Interrupt (active low)
Bit 2	=	SCSI Interrupt (active low)
Bit 1	=	ECC Interrupt (active low)
Bit 0	=	ZERO (grounded permanently)

An ECC Interrupt is received from the ECC PCA when the Error Correction Unit on that PCA finishes an encode operation or the decode of a Vector Address Field, Data Field, or Postfield.

An SCSI Interrupt is received from the SCSI Interface Circuit on completion of either a Function Buffer or Data Buffer DMA Read or Write operation.

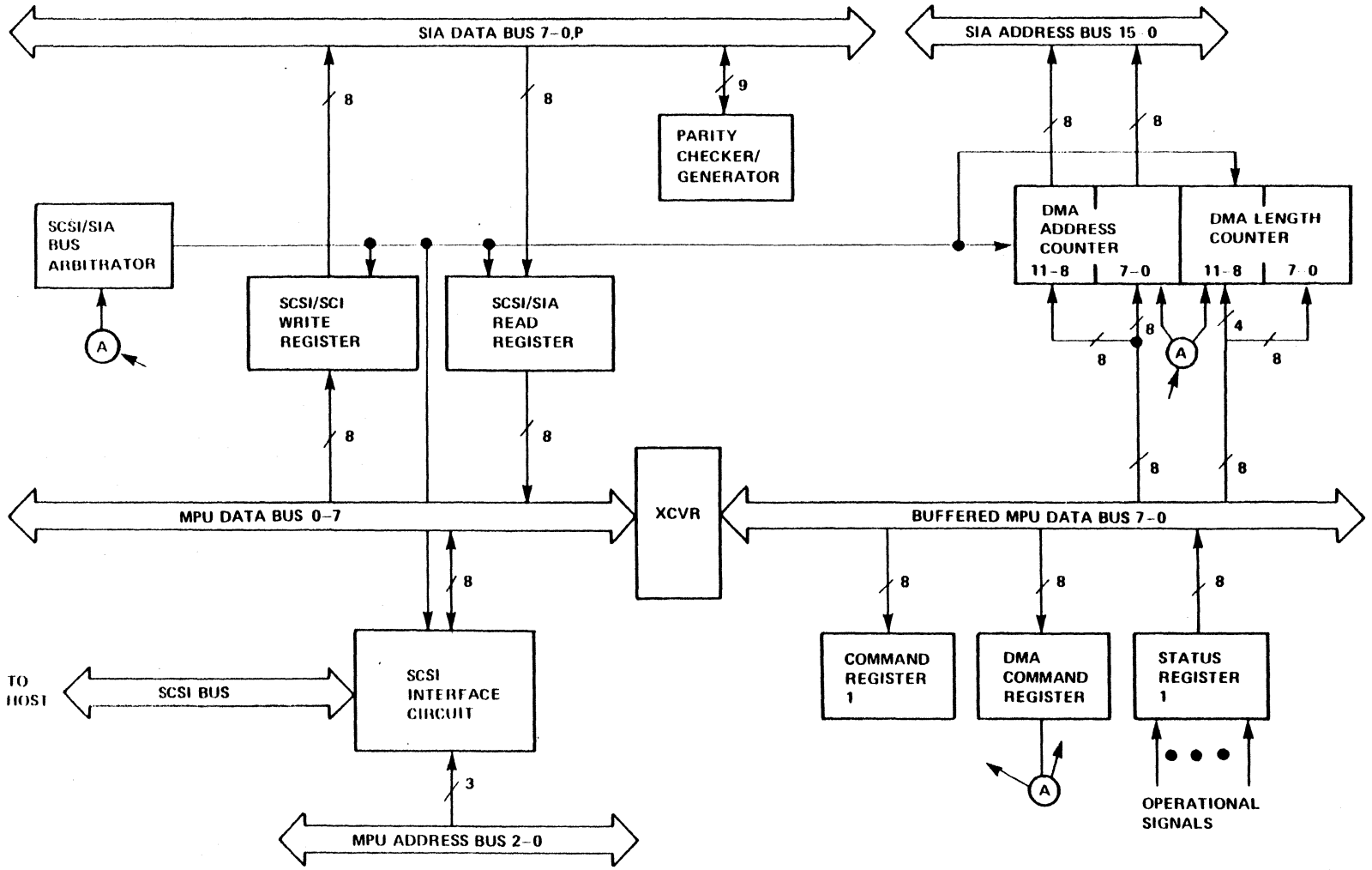
A Sector Interrupt is received from the Servo/Drive Control PCA shortly after the beginning of a sector on the Media. This interrupt defines the start of a timing window within the sector (the Command/Status Window). During this window, valid Drive status can be read by the Internal Controller and it can transfer a new command to the Drive for the upcoming sector operation.

A Timer Interrupt is received from the Counter/Timer Circuit when a system event has timed out.

3.5.4. SCSI Interface Control

The SCSI interface is the external connection between the Host and the LD 1200. This Interface is controlled by the following elements (refer to figure 3-24):

- SCSI Interface Circuit
- SCSI/SIA Write and Read Registers
- DMA Address and Word Length Counters and DMA Command Register
- SCSI/SIA Bus Arbitrator
- Parity Checker/Generator
- Command and Status Registers



LEGEND:

MPU = Microprocessor
XCVR = Transceiver

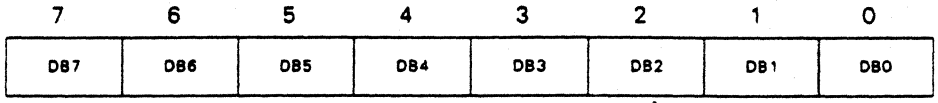
Figure 3-24. SCSI Interface Control

PB002353-1

3.5.4.1. SCSI Interface Circuit

The SCSI Interface Circuit is an NCR 5380 IC which provides SCSI Bus signals and protocol necessary for communication between the Host and LD 1200. (Refer to the Small Computer System Interface subsection in this manual for details on the operation of the SCSI Bus.) This circuit communicates with the MPU as a peripheral device. The MPU controls the SCSI Interface Circuit by reading and writing various registers within the IC. These registers are addressed by the MPU through the SCSI Ports. A detailed description of these registers follows.

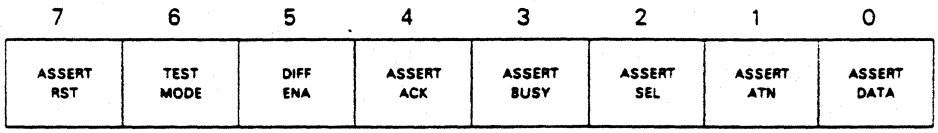
Output Data Register (Port Write–80 hex) – The bit format of this register is as follows:



INTX02

Output data to be placed on the SCSI Data Bus for transmission to the Host is first loaded into this register. This operation can be done as a port write or under DMA control. The register is also used during Arbitration and Selection to store identification (ID) bits.

Initiator Command Register (Port Write–81 hex) – The bit format of this register is as follows:



INTX03

This register contains signals normally driven by an Initiator to assert (activate) associated SCSI control signals:

Bit 7 = Asserts the Reset line

Bit 6 = Puts the Initiator in the Test Mode

Bit 5 = Not used for the LD 1200

Bit 4 = Asserts the Acknowledge line

Bit 3 = Asserts the Busy line

Bit 2 = Asserts the Select line

Bit 1 = Asserts the Attention line

Bit 0 = Asserts the Data Bus

Mode Register (Port Write-82 hex) - The bit format of this register is as follows:

7	6	5	4	3	2	1	0
BLOCK MODE DMA	TARGET MODE	ENABLE PARITY CHECK	ENABLE PARITY INT	ENABLE EOP INT	MONITOR BUSY	DMA MODE	ARBIT

INTX04

This register controls the operation of the SCSI interface, interrupt conditions, and parity checking as follows:

Bit 7 = Block Mode DMA - This bit controls DMA protocol parameters. Normally, the deactivation of -DACK signal indicates the end of a DMA transfer. Setting this bit to ONE puts the interface in the Block DMA Mode. In this mode, the deactivation of the -IOR or -IOW signal indicates the end of a DMA transfer. In the Block DMA Mode, only an initial DRQ/-DACK signal exchange is required to transfer data.

Bit 6 = Target Mode - This bit selects either the Target (ONE) or Initiator (ZERO) Mode.

Bit 5 = Enable Parity Checking - This bit controls whether parity errors are ignored (ZERO) or saved in the Parity Error Latch (ONE).

Bit 4 = Enable Parity Error Interrupt - This bit controls whether a parity error causes an interrupt (ONE) or not (ZERO). Parity checking must be enabled (Bit 5 = ONE) to allow detection of parity errors.

Bit 3 = Enable EOP Interrupt - This bit enables an interrupt to be generated when the IC receives an End-of-Process signal from the DMA Controller.

Bit 2 = Monitor Busy - This bit is used to detect an unexpected loss of the SCSI Busy signal. When this bit equals ONE, the loss of the Busy signal causes an interrupt and resets the lower six bits of the Initiator Command Register. reset of the Initiator Command Register removes the SCSI Interface Circuit from the SCSI Bus.

Bit 1 = DMA Mode - This bit enables a DMA transfer. This bit must be set to ONE before a start pulse is issued to any of Ports Write-85 through -87 hex. The DMA Mode bit must be set to ZERO when a DMA transfer finishes.

During the DMA Mode, the Request and Acknowledge signals are controlled automatically. The Target Mode Bit (Bit 6 of this register), however, must be set to the correct state, depending on whether the SCSI Interface Circuit is acting as a Target or an Initiator. For bus operations that output data, Assert Data Bus Bit 0 of the Initiator Command Register must be set to ONE.

Bit 0 = Arbitrate - To initiate an Arbitration operation, the correct ID bits are loaded into the Output Data Register (Port Write–80 hex) and this bit is set to ONE. The SCSI interface waits for a Bus Free phase then starts the Arbitration operation.

Target Command Register (Port Write–83 hex) - The bit format of this register is as follows:

7	6	5	4	3	2	1	0
XXX	XXX	XXX	XXX	ASSERT REQ	ASSERT MSG	ASSERT C/D	ASSERT I/O

XXX indicates a don't care bit.

INTX05

This register contains signals normally driven by a Target to assert associated SCSI control signals:

NOTE

The following register bits can be set, but the associated SCSI control signals are not asserted unless Target Mode Bit 6 of the Mode Register (Port Write–82 hex) is set to ONE.

Bits 7 through 4 = Don't care

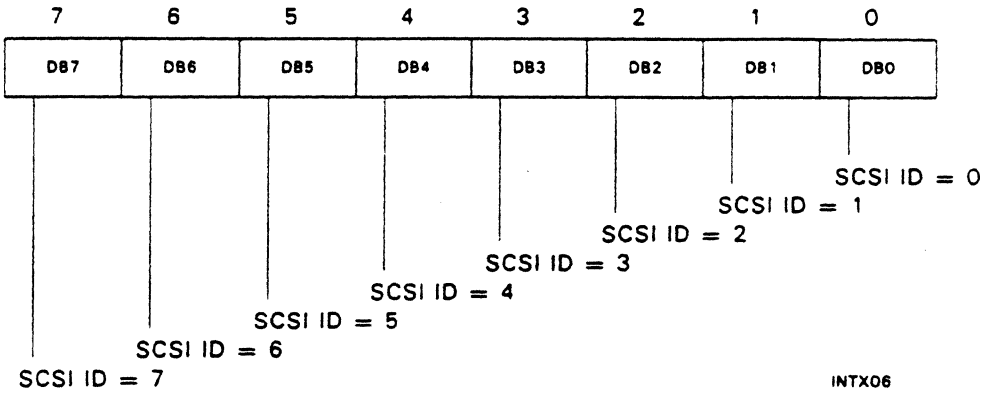
Bit 3 = Asserts the Request line

Bit 2 = Asserts the Message line

Bit 1 = A ONE asserts the Command Data line, indicating control information is on the Data Bus. A ZERO deasserts (deactivates) the line, indicating data is on the bus.

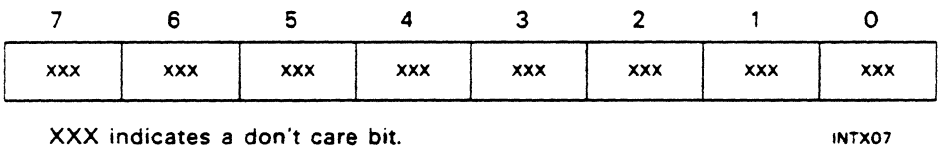
Bit 0 = A ONE asserts the Input/Output line, indicating data is on the Data Bus for input to the Initiator. A ZERO deasserts the line, indicating data output from the Initiator is on the bus.

Select Enable Register (Port Write–84 hex) - The bit format of this register is as follows:



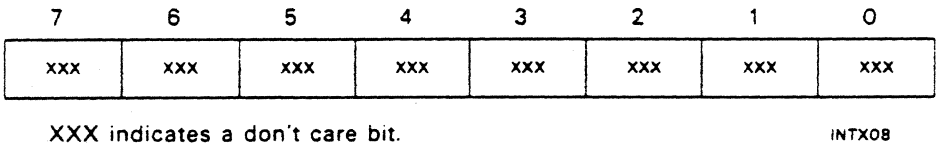
This register is used as a mask to monitor a single ID bit during a Selection attempt. Simultaneous occurrence of the correct ID bit, Busy deasserted, and Select asserted on the SCSI Bus causes an interrupt to be generated. Using this register as a mask allows an SCSI device to ignore Selection attempts meant for other devices on the bus. To disable the Select Interrupt, all bits in this register are set to ZERO.

Start DMA Send (Port Write–85 hex) – The bit format of this port is as follows:



After the DMA Mode has been set (Port Write–82 hex, Bit 1 = ONE), a Write operation to this port starts a data transfer.

Start Target Receive DMA (Port Write–86 hex) – The bit format of this port is as follows:



After the DMA Mode has been set (Port Write–82 hex, Bit 1 = ONE), a Write operation to this port starts a data receive transfer to the Target.

Start Initiator Receive DMA (Port Write–87 hex) – The bit format of this port is as follows:

7	6	5	4	3	2	1	0
XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX

XXX indicates a don't care bit.

INTX09

After the DMA Mode has been set (Port Write-82 hex, Bit 1 = ONE), a Write operation to this port starts a data receive transfer to the Initiator.

Current SCSI Data (Port Read-80 hex) - The bit format of this port is as follows:

7	6	5	4	3	2	1	0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

INTX10

This port enables the MPU to read the SCSI Data Bus directly. When parity checking is enabled (Port Write-82 hex, Bit 5 = ONE), SCSI Bus parity is checked at the beginning of the Read cycle.

Initiator Command Register (Port Read-81 hex) - The bit format of this register is as follows:

7	6	5	4	3	2	1	0
ASSERT RST	ARBIT IN PROG	LOST ARBIT	ASSERT ACK	ASSERT BUSY	ASSERT SEL	ASSERT ATN	ASSERT DATA

INTX11

This port enables the MPU to read the contents of the Initiator Command Register. Bits 5 and 6 of this port are not part of the Initiator Command Register. These bits indicate the status of an Arbitration operation. The bits of this port are defined as follows:

Bit 7 = Indicates the state of the Assert Reset bit.

Bit 6 = Arbitration In Progress - An SCSI device has attempted to gain control of the SCSI Bus by entering an Arbitration phase after detection of a Bus Free phase. The SCSI device ID and Busy signal may still be asserted on the SCSI Bus. This bit is ZERO when the Arbitrate bit (Port Write-82 hex, Bit 0) is ZERO.

Bit 5 = Lost Arbitration – An Arbitration phase was attempted to gain control of the SCSI Bus, but was lost to another SCSI device. A Bus Free phase has been detected and another SCSI device has asserted the Select signal. The action of the other SCSI device forced this device to remove its ID bit from the SCSI Data Bus and deassert the Busy signal. The Lost Arbitration bit is ZERO when the Arbitrate bit (Port Write–82 hex, Bit 0) is ZERO.

Bit 4 = Indicates the state of the Assert Acknowledge bit.

Bit 3 = Indicates the state of the Assert Busy bit.

Bit 2 = Indicates the state of the Assert Select bit.

Bit 1 = Indicates the state of the Assert Attention bit.

Bit 0 = Indicates the state of the Assert Data Bus bit.

Refer to the Initiator Command Register (Port Write–81 hex) description in this subsection for descriptions of Bits 7 and 4 through 0.

Mode Register (Port Read–82 hex) – The bit format of this register is as follows:

7	6	5	4	3	2	1	0
BLOCK MODE DMA	TARGET MODE	ENABLE PARITY CHECK	ENABLE PARITY INT	ENABLE EOP INT	MONITOR BUSY	DMA MODE	ARBIT

INTX12

This port enables the MPU to read the contents of the Mode Register:

Bit 7 = Indicates the state of the Block Mode DMA bit.

Bit 6 = Indicates the state of the Target Mode bit.

Bit 5 = Indicates the state of the Enable Parity Checking bit.

Bit 4 = Indicates the state of the Enable Parity Interrupt bit.

Bit 3 = Indicates the state of the End–of–Process Interrupt bit.

Bit 2 = Indicates the state of the Monitor Busy bit.

Bit 1 = Indicates the state of the DMA Mode bit.

Bit 0 = Indicates the state of the Arbitrate bit.

Refer to the Mode Register (Port Write–82 hex) description in this subsection for descriptions of Mode Register bits.

Target Command Register (Port Read-83 hex) - The bit format of this register is as follows:

7	6	5	4	3	2	1	0
0	0	0	0	ASSERT REQ	ASSERT MSG	ASSERT C/D	ASSERT I/O

INTX13

This port enables the MPU to read the contents of the Target Command Register:

Bits 7 through 4 = ZERO

Bit 3 = Indicates the state of the Assert Request bit.

Bit 2 = Indicates the state of the Assert Message bit.

Bit 1 = Indicates the state of the Assert Command/Data bit.

Bit 0 = Indicates the state of the Input/Output bit.

Refer to the Target Command Register (Port Write-83 hex) description in this subsection for descriptions of Bits 3 through 0.

Current SCSI Bus Status (Port Read-84 hex) - The bit format of this port is as follows:

7	6	5	4	3	2	1	0
RST	BSY	REQ	MSG	C/D	I/O	SEL	DBP

INTX14

This port enables the MPU to read the current states of the SCSI Bus lines:

Bus 7 = Indicates the state of the SCSI Reset line.

Bus 6 = Indicates the state of the SCSI Busy line.

Bus 5 = Indicates the state of the SCSI Request line.

Bus 4 = Indicates the state of the SCSI Message line.

Bus 3 = Indicates the state of the SCSI Command/Data line.

Bus 2 = Indicates the state of the SCSI Input/Output line.

Bus 1 = Indicates the state of the SCSI Select line.

Bus 0 = Indicates the state of the SCSI Data Bus Parity line.

Refer to the Small Computer System Interface subsection for descriptions of these lines.

Bus and Status Register (Port Read-85 hex) - The bit format for this register is as follows:

7	6	5	4	3	2	1	0
END OF DMA	DMA REQ	PARITY ERROR	INT REQ	PHASE MATCH	BUSY ERROR	ATN	ACK

INTX15

This register enables the MPU to read several status conditions and two SCSI control lines not provided by the Current SCSI Bus Status (Port Read-84 hex):

Bus 7 = End of DMA Transfer - This bit is set to ONE during the last byte of a DMA transfer, indicating only that the SCSI transfer is complete. During a DMA Write to Common Memory, the last byte may not be written in memory yet when this bit becomes ONE. DMA In Progress Bit 7 in Status Register 1 (Port Read-94 hex) goes to ZERO after the byte has been transferred to Common Memory. The End of DMA Transfer bit is set to ZERO when DMA Mode Bit 1 in the Mode Register (Port Write-82 hex) is set to ZERO.

Bit 6 = DMA Request - This bit enables the MPU to sample the DRQ (DMA Request) output pin on the SCSI Interface IC. DRQ can be deactivated by activating -DACK or by setting DMA Mode Bit 1 in the Mode Register (Port Write-82 hex) to ZERO.

Bit 5 = Parity Error - This bit is set to ONE if a parity error occurs during a data transfer or Selection operation. Parity checking must be enabled to detect a parity error (Port Write-82 hex, Bit 5 = ONE). A parity error can be cleared by reading Port Read-87 hex.

Bit 4 = Interrupt Request Active - This bit is set to ONE when an enabled interrupt condition occurs. The bit displays the current state of the IRQ (Interrupt Request) output pin on the SCSI Interface IC. An interrupt can be cleared by reading Port Read-87 hex.

Bit 3 = Phase Match - Three signals define the current SCSI Bus phase: Message, Command/Data, and Input/Output. A ONE in this bit position indicates that the current SCSI Bus phase matches the phase specified by the three lower bits of the Target Command Register (Port Write-83 hex). These signals (lines) are driven by a Target and received by an Initiator. The Phase Match bit is significant only when the SCSI device is acting as an Initiator.

Bit 2 = Busy Error - This bit indicates an unexpected loss of the Busy signal has occurred. The Busy Error Latch is set to ONE whenever Monitor Busy Bit 2 in the Mode Register (Port Write-82 hex) is ONE and the Busy signal is deasserted. The Busy Error bit is set to ZERO by reading Port Read-87 hex.

Bit 1 = Attention From SCSI Bus - Indicates the current state of the SCSI Attention signal.

Bit 0 = Acknowledge From SCSI Bus - Indicates the current state of the SCSI Acknowledge signal.

Input Data Register (Port Read-86 hex) - The bit format of this register is as follows:

7	6	5	4	3	2	1	0
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

INTX16

Input data received from the Host via the SCSI Bus and previously latched into this register can be read by the MPU. This can be done through a port Read operation or under DMA control.

Clear Parity and Interrupt (Port Write-87 hex) - The bit format of this register is as follows:

7	6	5	4	3	2	1	0
XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX

XXX indicates a don't care bit.

INTX17

Reading this register sets to ZERO Parity Error Bit 5, Interrupt Request Bit 4, and Busy Error Bit 2 in the Bus and Status Register (Port Read-85 hex).

SCSI Bus Interface - The SCSI Interface IC includes high current outputs which drive the SCSI Bus directly in the open-collector mode. SCSI Bus timing is asynchronous, therefore, there is no clock input to the SCSI Interface IC.

MPU/SCSI Interface Circuit Operations - The MPU loads control information into the registers inside the SCSI Interface IC via the SCSI Ports. The IC uses this information to control the protocol sequence necessary to perform the required operation. A typical operation involves Arbitration for the SCSI Bus and Selection of the LD 1200 by the Host, followed by the transfer of commands, data, status, and a message between the Host and LD 1200.

The MPU loads SCSI control information into the MPU/SIA Write Register. The information is then transferred via the SIA Bus and latched into the SCSI/SIA Read Register. The MPU addresses the applicable SCSI Ports and thereby loads the appropriate registers within the SCSI Interface IC with the control information.

After the LD 1200 is Selected, command data from the Host (eight data bits and one parity bit) is received through the open-collector drivers in the SCSI Interface IC and loaded into the Input Data Register (Port Read-86 hex). One command byte is transferred to the LD 1200 with each REQ/ACK (Request/Acknowledge) exchange. The MPU addresses Port Read-86 hex to latch the byte of command data from the Input Data Register into the SCSI/SIA Write Register. The MPU then reads the command data via the SIA Bus through the MPU/SIA Read Register.

Data being transferred from the LD 1200 to the Host is loaded from the SIA Bus into the SCSI/SIA Read Register. The data is then written into the Output Data Register (Port Write-80 hex) in the SCSI Interface IC by the MPU. The SCSI Interface IC reconnects with the Host and transfers the data to the Host through the open-collector drivers.

3.5.4.2. SCSI/SIA Write and Read Registers

These registers, shown in figure 3-24, buffer data moving between the LD 1200 and Host onto and off of the SIA Bus. Data being sent to the Host is transferred from Common Memory (on the ECC PCA) via the SIA Bus to the SCSI/SIA Read Register. From there, the data is written into the Output Data Register in the SCSI Interface Circuit by the MPU. This circuit then transmits the data to the Host.

Data received from the Host is read from the Input Data Register in the SCSI Interface Circuit and latched into the SCSI/SIA Write Register. From there, the data is transferred to Common Memory via the SIA Bus.

3.5.4.3. SCSI/Common Memory Direct Memory Access

Incoming data from the SCSI Bus is sent to Common Memory by Direct Memory Access (DMA) operations controlled by COS. COS uses Bits 7 and 1 of the Mode Register and Bits 1 and 0 of the DMA Command Register for these operations. Mode Register bits applicable to DMA are described in the SCSI Interface Circuit subsection.

The DMA Command Register (Port Write-98 hex) is formatted as follows:

7	6	5	4	3	2	1	0
—	—	—	—	—	—	DMA TO SCSI	DMA FROM SCSI

INTX18

Bits 7 through 2 = Unused

Bit 1 = DMA to SCSI - Starts a DMA transfer to the SCSI Bus from Common Memory (on the ECC PCA).

Bit 0 = DMA From SCSI - Starts a DMA transfer from the SCSI Bus to Common Memory.

These two bits initiate a DMA transfer between the Host and LD 1200 Common Memory. Activation of either of these bits is the last step in setting up a DMA transfer. The direction of the transfer is specified by which bit is set to ONE. Because the bits are mutually exclusive, both cannot be ONE at the same time. When a DMA operation is allowed to finish normally, the MPU is interrupted by the SCSI Interface Circuit and the DMA Command Register is cleared at the end of the final transfer.

Writing 00 hex to this port aborts a DMA operation in progress. The values in the DMA Address and DMA Length Counters are not affected by this port.

DMA operation is controlled by the DMA Address and Length Counters which are I/O Ports loaded by the MPU via the Buffered MPU Data Bus under COS control. These counters provide the starting address and byte count for the data transfer between the SCSI Interface and Common Memory. The MPU loads these counters before the DMA operation is initiated.

NOTE

These counters should not be loaded while a DMA is in progress.

The DMA Address Counter is a 16-bit counter that is loaded with the starting address minus one of the sector for which the DMA operation is pending. The address range of this counter is 0 to 64K. The MPU cannot read the contents of the DMA Address Counter, but can use the value in the DMA Length Counter to calculate the address counter value if a DMA operation is suspended.

The DMA Length Counter is a 12-bit counter that is loaded with the desired byte count for a DMA Read operation or the byte count minus one for a DMA Write operation. The byte count is limited to a maximum of 4096 byte transfers. The upper four bits of this counter are not used and appear as ONEs when read.

The MPU loads the Mode Register (Port Write-82 hex) to enable the DMA Mode and specify the type of transfer to take place (Bits 7, 6, and 1). Next, the DMA Address Counter (Ports Write-90 and -91 hex) and DMA Length Counter (Ports Write-92 and -93 hex) are loaded by the MPU. The DMA Command Register (Port Write-98 hex) is then loaded by the MPU to specify the direction of the DMA transfer and to enable the counters. To start the DMA operation, either Port Write-85, -86, or -87 hex is written to by the MPU:

Port Write-85: Starts a DMA operation to send data to the Host.

Port Write-86: Starts a DMA operation to receive data as a Target.

Port Write-87: Starts a DMA operation to receive data as an Initiator.

At this point, the SCSI Interface Circuit begins an Information Transfer sequence with the Host (refer to the Small Computer System Interface subsection for details). One byte of data is transferred between the Host and LD 1200 with each REQ/ACK exchange. Just before each DMA exchange with Common Memory, the DMA Length Counter is decremented by one. As each byte is transferred, the DMA Address Counter is incremented. When the DMA Length Counter is decremented to zero, the SCSI Interface Circuit interrupts the MPU with an SCSI Interrupt and the DMA operation is stopped. The transfer of data is resumed when the MPU reloads the DMA Address and Length Counters and initiates another DMA operation.

3.5.4.4. SCSI/SIA Bus Arbitrator

After a DMA operation has been set up and enabled, the SCSI/SIA Bus Arbitrator gains control of the SIA Bus and issues memory requests that enable data transfers between the SCSI Bus and Common Memory. Refer to the Bus Module Priority System subsection in this manual for a description of SIA Bus priority system operation.

3.5.4.5. Parity Checker/Generator

This circuit checks and generates parity for data transfers over the SIA Bus. When a SIA Bus module (MDS PCA, S/DC PCA, ECC PCA, MPU, or Common Memory) is written to, odd parity is generated and sent with the data on the SIA Data Bus Parity line. When the SIA Bus is read, parity is checked on the data received.

3.5.4.6. Command Register 1 (Port Write–97 hex)

Command Register 1 is used to control operation of the Internal Controller. The bit format of this register is as follows:

7	6	5	4	3	2	1	0
COMEM PAGE SEL	RAM/ROM SEL	FORCE SIA PE	—	—	—	DIAG DMA	RESET

INTX19

Bit 7 = Common Memory Page Select – This bit is used by the MPU to select which half of Common Memory is to be available for access. Common Memory is 64 kilobytes in size, but only 34 kilobytes are available to the MPU for access at any given time. When this bit is ZERO, the MPU has access to the lower half of Common Memory. When it is ONE, the MPU has access to the upper half. After an MPU Reset, the lower half of Common Memory is available until this bit is changed. An MPU Reset is the result of a power–up condition or an SCSI Bus Reset.

Bit 6 = RAM/ROM Select – This bit is used by the MPU to select either the 2K scratchpad RAM or the upper 2K of the 32K ROM (addresses 7800 through 7FFF hex) on the SCSI PCA. When this bit is ZERO, the MPU has access to the RAM. When it is ONE, the MPU has access to the ROM. After an MPU Reset, the MPU has access to the RAM until this bit is changed.

Bit 5 = Force SIA Bus Parity Error – This bit is used to force a SIA Bus parity error during Diagnostic Mode operation.

Bits 4 through 2 = Not used.

Bit 1 = Diagnostic DMA – This bit enables the initialization of a DMA transfer to Common Memory for the purpose of checking the DMA logic.

Bit 0 = Reset – This pulsed bit initializes the SCSI Interface Circuit. This signal must be issued in response to a nonrecoverable error. The Reset bit is active low.

3.5.4.7. Status Register 1 (Port Read-94 hex)

Status Register 1 is used to monitor Internal Controller operation. The bit format of this register is as follows:

7	6	5	4	3	2	1	0
DMA IN PROGRESS	ECC PARITY ERROR	COMMON MEMORY PARITY ERROR	SIA PARITY ERROR	0	0	MAINTENANCE PANEL NOT PRESENT	0

INTX20

Bit 7 = DMA In Progress - Indicates that a previously initiated DMA transfer has not yet terminated. A DMA terminates when the Length Counter (Ports Write-92 and -93 hex) is decremented to zero. A DMA operation can be prematurely terminated by the MPU or SCSI Interface.

Bit 6 = ECC Parity Error - Indicates that a parity error has been detected by the ECC circuit during a transfer of information from the SIA Bus. This bit can be cleared by reading Clear ECC Parity Error Port Read-96 hex.

Bit 5 = Common Memory Parity Error - Indicates that a parity error has been detected by Common Memory circuitry during a write into memory.

Bit 4 = SIA Parity Error - Indicates that a parity error was detected by the MPU or SCSI/SIA control logic during a transfer of information from the SIA Bus. This bit can be cleared by reading Clear ECC Parity Error Port Read-96 hex.

Bits 3 and 2 = Not used (always set to ZERO).

Bit 1 = Maintenance Panel Not Present - When set to ZERO, this bit indicates that a Maintenance Panel is installed in the LD 1200 and must be included in the normal polling process. Set to ONE, this bit indicates a Maintenance Panel is not installed.

Bit 0 = Not used (always set to ZERO).

3.5.5. SIA Clock Generator

System Interface Assembly (SIA) clock generation modules and the asynchronous relationship these clocks have with the MPU clock modules are described in this subsection (refer to figure 3-25).

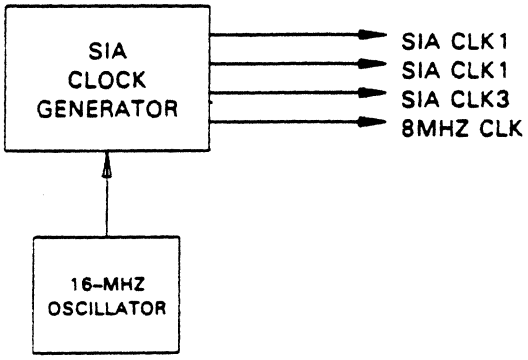


Figure 3-25. SIA Clock Generator

The 16-MHz Oscillator drives the SIA Clock Generator which provides four clocks: an 8-MHz clock, which is sent to the ECC PCA, and three 2-MHz, 50% duty cycle SIA Bus clocks (SIACLK1, SIACLK2, and SIACLK3) used to synchronize SIA Bus transactions.

On the SCSI PCA, the SIA Bus clocks are used by the SIA Bus arbitration logic to obtain control of the SIA Bus for data transfers. Refer to the SIA Bus Timing subsection in this manual for more information on SIA Bus clocks.

3.5.6. Operator and Maintenance Panel External Registers

The following Operator and Maintenance Panel External Registers, implemented on the SCSI PCA, are described in this subsection (refer to figure 3-26):

- Operator Panel:
  - Operator Panel Hexadecimal Display Register
  - Device Address Switch Register
- Maintenance Panel:
  - Maintenance Panel LED Register
  - Maintenance Panel Hexadecimal Display Register
  - Maintenance Panel Keyboard Register

Refer to the Operator Panel and Maintenance Panel subsections in this manual for operation and interface information.

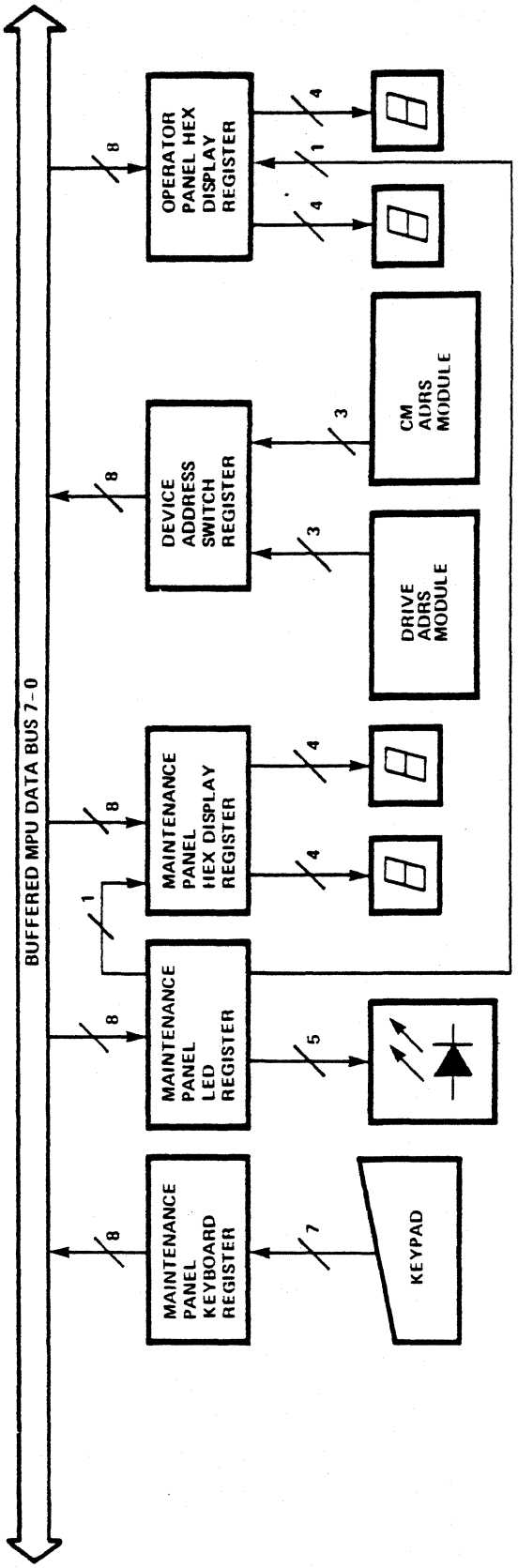
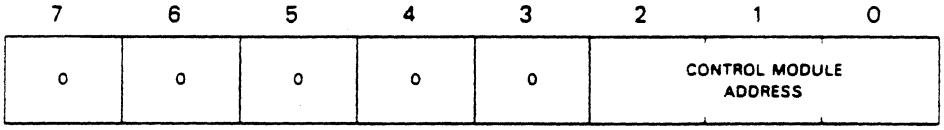


Figure 3-26. Operator and Maintenance Panel External Registers

3.5.6.1. Device Address Switch Register (Port Read–95 hex)

The bit format of this register is as follows:



INTX21

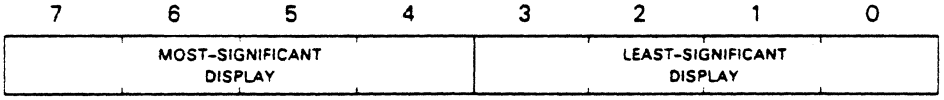
Bits 7 through 3 = Not used (always ZERO).

Bits 2 through 0 = Control Module Address – These bits provide the Target ID for the Internal Controller. A 000 address indicates SCSI ID 0 hex, 111 indicates SCSI ID 7 hex.

CONTROL MODULE ADDRESS switch cap inputs from the Operator Panel are routed to the Internal Controller via this register. DEVICE ADDRESS switch cap inputs are not used.

3.5.6.2. Operator Panel Hexadecimal Display Register (Port Write–94 hex)

The bit format of this register is as follows:



INTX22

Bits 7 through 4 = Most-Significant Display – Left-hand character displayed on the Operator Panel Hexadecimal Display.

Bits 3 through 0 = Least-Significant Display – Right-hand character displayed on the Operator Panel Hexadecimal Display.

The 8-bit value loaded into this register is displayed on the Operator Panel Hexadecimal Display. The display reports codes corresponding to normal operating, fault, and error conditions. The register consists of two four-bit binary patterns.

This display is enabled by Operator Panel Display Enable Bit 7 of the Maintenance Panel LED Register (Port Write–95 hex) which is used by COS to blank or blink the display.

This output register is cleared upon power-up reset. A display of zeros on the Operator Panel Hexadecimal display indicates that MPU control processing is not underway

3.5.6.3. Maintenance Panel LED Register (Port Write–95 hex)

The bit format of this register is as follows:

7	6	5	4	3	2	1	0
OPERATOR PANEL DISPLAY ENABLE	MAINTENANCE PANEL HEX DISPLAY ENABLE	NOT USED	F1 KEY LED	CE MODE KEY LED	DISPLAY MEMORY KEY LED	START/ STOP KEY LED	ENTER KEY LED

INTX23

Bit 7 = Operator Panel Display Enable – Enables the hexadecimal display on the Operator Panel to display the two–character code specified in the Operator Panel Hexadecimal Display Register.

Bit 6 = Maintenance Panel Hex Display Enable – Enables the hexadecimal display on the Maintenance Panel to display the two–character code specified in the Maintenance Panel Hexadecimal Display Register.

Bit 5 = Not used.

Bit 4 = F1 Key LED – ZERO illuminates the F1 LED. ONE extinguishes it.

Bit 3 = CE Mode Key LED – ZERO illuminates the CE Mode LED. ONE extinguishes it.

Bit 2 = Display Memory Key LED – ZERO illuminates the Display Memory LED. ONE extinguishes it.

Bit 1 = Start/Stop Key LED – ZERO illuminates the Start/Stop LED. One extinguishes it.

Bit 0 = Enter Key LED – ZERO illuminates the Enter LED. ONE extinguishes it.

This register is used by the MPU to control the LEDs on the Maintenance Panel keys and to blank or blink the Maintenance Panel and Operator Panel Hexadecimal Displays.

During SIA and SCSI Bus Resets, this register is initialized to a state that illuminates all Maintenance Panel LEDs and enables the displays on both panels.

3.5.6.4. Maintenance Panel Hexadecimal Display Register (Port Write–96 hex)

The bit format of this register is as follows:

7	6	5	4	3	2	1	0
MOST-SIGNIFICANT DISPLAY				LEAST-SIGNIFICANT DISPLAY			

INTX24

Bits 7 through 4 = Most-Significant Display - Left-hand character displayed on the Maintenance Panel Hexadecimal Display.

Bits 3 through 0 = Least-Significant Display - Right-hand character displayed on the Maintenance Panel Hexadecimal Display.

The two-character hexadecimal display on the Maintenance Panel reports status during the execution of diagnostics and codes being entered using the ENTER key. This register drives the hexadecimal display on the Maintenance Panel. The display is blanked or blinked by toggling Bit 6 of the Maintenance Panel LED Register (Port Write-95 hex). The display is enabled on power-up. Use of this display is described in the Structured Analysis Method (SAM) Tables subsection of SCSI LD 1200 Hardware Maintenance Manual - Volume 1.

3.5.6.5. Maintenance Panel Keyboard Register (Port Read-97 hex)

The bit format of this register is as follows:

7	6	5	4	3	2	1	0
INCREMENT MSD KEY	INCREMENT LSD KEY	1	F1 KEY	CE MODE KEY	DISPLAY MEMORY KEY	START/ STOP KEY	ENTER KEY

INTX25

Bit 7 = Increment MSD Key - ZERO indicates the Increment MSD key has been pressed.

Bit 6 = Increment LSD Key - ZERO indicates the Increment LSD key has been pressed.

Bit 5 = Not used (always set to ONE).

Bit 4 = F1 Key - ZERO indicates the F1 key has been pressed.

Bit 3 = CE Mode Key - ZERO indicates the CE Mode key has been pressed.

Bit 2 = Display Memory Key - ZERO indicates the Display Memory key has been pressed.

Bit 1 = Start/Stop Key - ZERO indicates the Start/Stop key has been pressed.

Bit 0 = Enter Key - ZERO indicates the Enter key has been pressed.

Each bit of this register corresponds to a key on the Maintenance Panel membrane keypad. When a key is pressed, the associated line is grounded. The output is pulled up by a pullup resister into an active low state.

Switch debouncing is handled by the operating system. COS firmware collects the status of the Maintenance Panel Keyboard Register through regular interrupts generated by the counter-timer

circuit (at approximately 30-millisecond intervals). The bit pattern in this register at the time of the interrupt is saved by the MPU in RAM with the two most current register samples. A bit that remains stable for two interrupt periods is considered valid and not noise. Physical debounce time at the switch is 20 milliseconds.

When the firmware detects that CE Mode Key Bit 3 has remained active for two consecutive interrupts, CE Mode is valid and ongoing operations are terminated. Then, Maintenance Panel requests are honored exclusively. The Diagnostic Handler in the firmware keeps polling for a second depression of the CE Mode Key which, when detected, terminates CE Mode. At this point, the entire unit is Master Reset.

3.6. ERROR CORRECTION AND COMMON MEMORY INTERFACE UNIT PCA

The Error Correction and Common Memory Interface Unit (ECC) PCA communicates with the ICI PCA and Modulator Demodulator Synchronizer (MDS) PCA via the SIA/IDI Bus.

The ECC PCA has two major elements:

- Common Memory Interface: contains Common Memory to store data during data manipulation and DMA transfers, and associated circuitry.
- Error Correction Unit: contains a VLSI Error Correction Encode/Decode unit to ensure quality read data in the LD 1200, and associated circuitry.

Data can be sent to Common Memory from the Error Correction Unit, and from the MDS and ICI PCAs. The Common Memory Interface for the MDS PCA is controlled by a Z80 Microprocessor (MPU) on the ICI PCA.

The Error Correction Unit is controlled by an 8x305 Microcontroller. It controls all encoding, error correction, ECC PCA diagnostics and I/O functions for the Error Correction Unit.

The ECC PCA is shown in block diagram form in figure 3-27. Detailed descriptions of the ECC PCA circuits are in the following subsections.

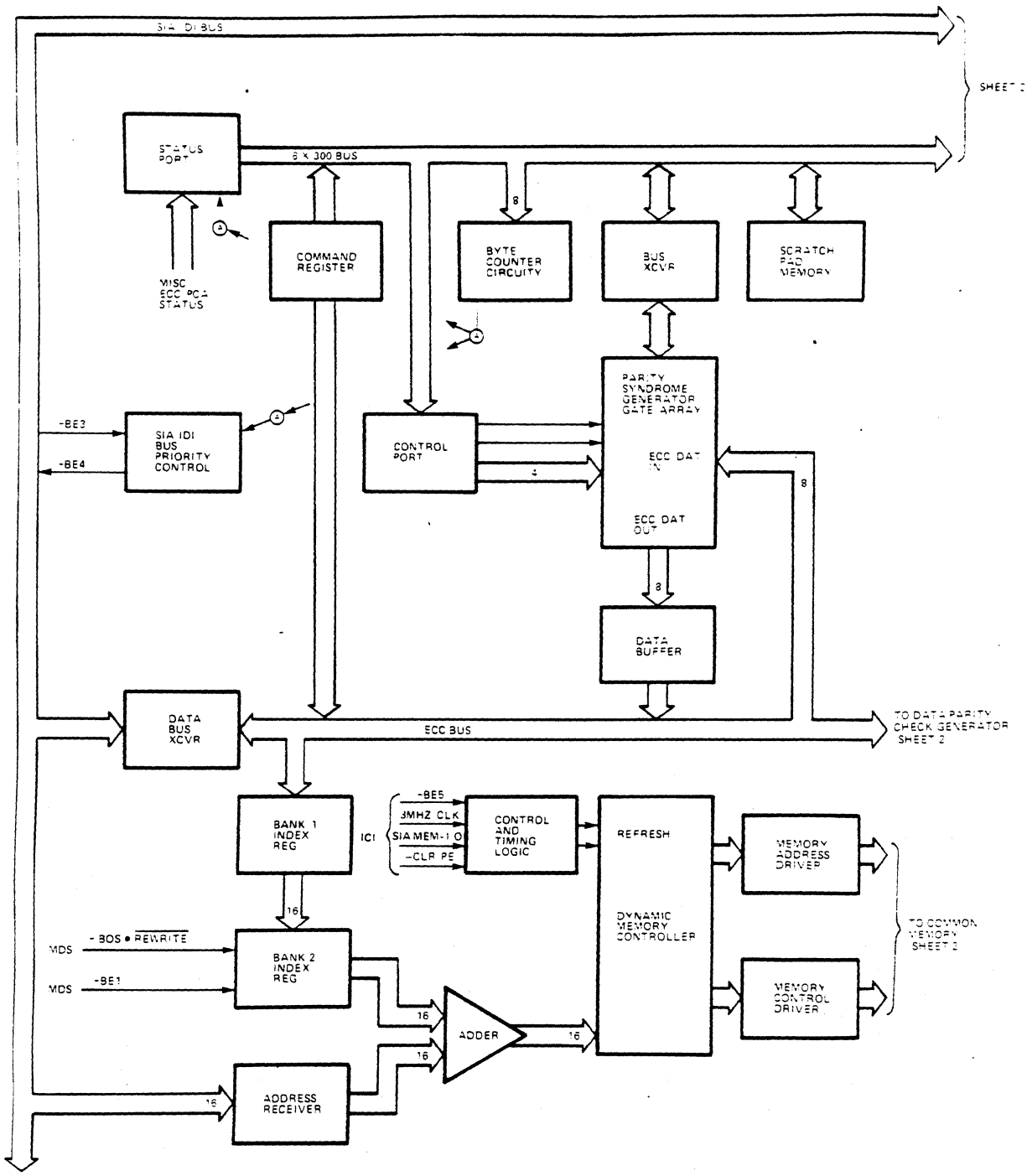


Figure 3-27. Error Correction and Common Memory Interface Unit PCA Block Diagram
(Sheet 1 of 2)

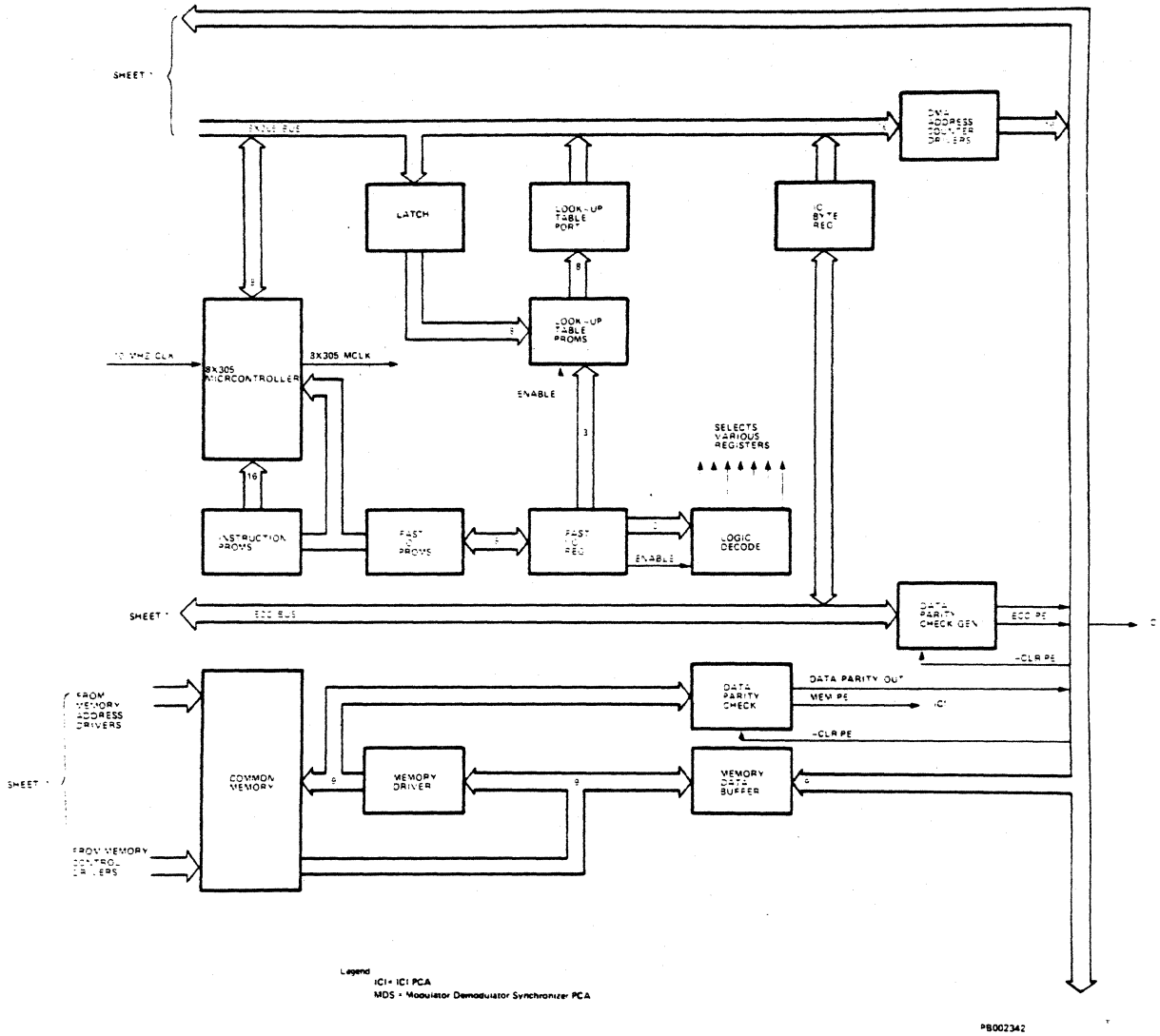


Figure 3-27. Error Correction and Common Memory Interface Unit PCA Block Diagram
(Sheet 2 of 2)

3.6.1. Signal Interface Descriptions

+BOS ● $\overline{\text{REWRITE}}$ (Beginning of Sector AND Rewrite Not)

This signal is generated by the MDS PCA at the beginning of a sector in which a Rewrite operation is to be attempted. It is used to assure that the data for the Rewrite is taken from the same physical data buffer as that used for the original Write attempt.

-CLR PE

This signal is generated by the ICI PCA. When low, it clears parity errors on the ECC PCA.

+ECC PE

This signal is sent to the ICI PCA. It goes high when one of the following has occurred: a parity error was detected in a command received from the ICI PCA, a parity error was detected in data written into the Bank 1 Index Register, or a parity error was detected in data read from Common Memory by the Error Correction Unit.

+ SIA DATA PARITY

This signal is generated by any PCA while it puts data onto the SIA/IDI Data Bus. It carries parity information. The SIA/IDI Data Bus plus this bit should always contain ODD parity.

+MEM PE (Memory Parity Error)

This signal is sent to the ICI PCA. When high, it indicates that an error is detected in data that is being sent to Common Memory.

+SIA MEM/IO

This signal, when high, indicates a Common Memory data transfer.

-ECC INT

This signal is sent to the ICI PCA. It signals that the ECC PCA has sent an interrupt.

+BE1 (Bus Enable 1)

This signal is generated by the MDS PCA. When low, it enables the Bank 2 Index Registers, sending a supplementary address to the Adders.

+BE3 (Bus Enable 3)

This signal is generated by the ICI PCA. When high, the Error Correction Unit may access Common Memory via the SIA/IDI Bus.

+BE4 (Bus Enable 4)

This signal is sent to the ICI PCA. When high, the SCSI DMA Control Unit, on the ICI PCA, may access Common Memory via the SIA/IDI Bus.

+BE5 (Bus Enable 5)

This signal is generated by the ICI PCA. When high, the SIA/IDI is not requested, and the Dynamic Memory Controller issues a Refresh command.

8-MHz CLOCK

The 8-MHz Clock signal, generated by the ICI PCA, is the clock for the Dynamic Memory Controller.

10-MHz CLOCK

The 10-MHz Clock signal is generated by the Servo/Drive Control PCA. This signal is the clock to the 8x305 Microcontroller.

3.6.2. SIA/IDI Bus

The ECC PCA communicates with the ICI and MDS PCAs via the SIA/IDI Bus. This Bus consists of:

- Sixteen-bit address bus
- Eight-bit data bus plus one-bit parity
- Control signals
- Clock signals

3.6.2.1. SIA/IDI Address Bus

The SIA/IDI Address Bus is a bidirectional bus between the ECC PCA and the MDS and ICI PCAs. It carries address information to control which location in Common Memory, or which I/O port is accessed.

3.6.2.2. SIA/IDI Data Bus

This eight-line plus parity bidirectional bus transfers data between the MDS and ICI PCAs and the ECC PCA.

3.6.2.3. SIA/IDI Bus Control Signals

The IDI Bus control Signals indicate whether a Read or Write operation is to be performed, and whether an I/O operation or a memory access is to occur. The control signals can also cause each bus module to re-initialize.

3.6.2.4. SIA/IDI Bus Clock Signals

SIA/IDI Bus Clock signals SIA CLK 1, SIA CLK 2 and SIA CLK 3 are generated by the ICI PCA. These clock signals are used to synchronize data transfers between the several PCAs that are connected to the SIA/IDI Bus.

3.6.3. Common Memory Interface

Common Memory is a common storage buffer for data received from the MDS and ICI PCAs. It temporarily stores data that is received, via the SIA/IDI Bus, through the Memory Data Buffer and Memory Driver.

The Common Memory Interface portion of the ECC PCA performs the following:

- Modifies the address information received from the MDS PCA to be compatible with the addresses in Common Memory.
- Reads data into and out of Common Memory.
- Checks parity as it enters Common Memory.

Common Memory can be addressed by the Error Correction Unit of the ECC PCA, and the MDS and ICI PCAs. Address information to direct data storage is buffered by Address Receivers. Address information from the Error Correction Unit and the ICI PCA is complete and does not need modification. Address information from the MDS PCA contains only sector address information, and must be modified.

Prior to the MDS PCA sending the sector address information, the ICI PCA sends a supplementary address through the Data Bus Transceiver to Index Registers where the data is stored (refer to figure 3-27). The MDS PCA then sends the sector address information to the Address Receivers. The supplementary address and the sector address information are added together, resulting in a complete address.

When an address is received by the Address Receivers from the ICI PCA or the Error Correction Unit, it is a complete address. When this occurs, the three-state Bank 1 and Bank 2 Index Registers are not enabled. As a result, the supplementary address received in the Adders is zero.

The Adders send a Row Address (bits 0 through 7) and a Column Address (bits 8 through 15) to the Dynamic Memory Controller. The Dynamic Memory Controller multiplexes the row and column addresses. It sends first the multiplexed Row Address, then the multiplexed Column Address to Common Memory.

This process is described in greater detail in the following subsections.

3.6.3.1. Address Receivers

Address Receivers receive address information from the Error Correction Unit, the MDS PCA, and the ICI PCA via the SIA/IDI Bus.

Address information from the Error Correction Unit portion of the ECC PCA, and from the ICI PCA contains 16 significant bits. Address information from the MDS PCA contains only 13 significant bits of sector address information. The MDS PCA zero-fills the most-significant-bits when the address information is placed on the SIA/IDI Bus.

Information buffered by the Address Receivers is used to direct data storage in Common Memory.

3.6.3.2. Data Bus Transceiver

SIA/IDI Bus information is buffered via the Data Bus Transceiver. The buffered information is placed on the Internal Buffered SIA/IDI Bus.

3.6.3.3. Bank 1 Index Registers

Bank 1 Index Registers contain a supplemental address, sent by the ICI PCA. These registers are loaded prior to the MDS PCA sending an address to the Address Registers.

The supplemental address is used to modify the address sent by the MDS PCA, allowing the MDS PCA access to Common Memory.

3.6.3.4. Bank 2 Index Registers

The supplementary address is transferred from the Bank 1 Index Registers to the Bank 2 Index Registers at the beginning of each sector in which a Rewrite operation is not to occur by +BOS ● REWRITE. It is sent to the Adder when Bus Enable 1, the MDS PCA bus priority signal, goes low.

The contents of these three-state registers is not used when the Error Correction Unit or the ICI PCA are accessing Common Memory.

3.6.3.5. Adders

The address from the Address Receivers and the supplementary address, from the Bank 2 Index Registers, are added together. The Adder outputs a Row Address (bits 0 through 7) and a Column Address (bits 8 through 15) to the Dynamic Memory Controller.

3.6.3.6. Control and Timing Logic

The Control and Timing Logic buffers various clock and control signals. It generates the necessary timing signals for the Common Memory Interface portion of the ECC PCA.

3.6.3.7. Dynamic Memory Controller

The Dynamic Memory Controller determines access to Common Memory. It contains address multiplexers, refresh counters, and timing generation logic necessary to control the access to Common Memory.

Row and column addresses are latched into the Dynamic Memory Controller from the Adders when ALE goes low. The Dynamic Memory Controller multiplexes the row and column addresses. It sends first the multiplexed Row Address, then the multiplexed Column Address to the Memory Address Driver.

The Dynamic Memory Controller sends the appropriate control signals to the Memory Control Driver. Row Address Strobe goes low when the Row Address is being sent to the Memory Address Driver. Column Address Strobe goes low when the Column Address is being sent to the Memory Address Driver (refer to figure 3-28). The Dynamic Memory Controller performs a Refresh cycle when Bus Enable 5 goes high. CLK provides master timing to generate the Refresh cycle timing and refresh rate.

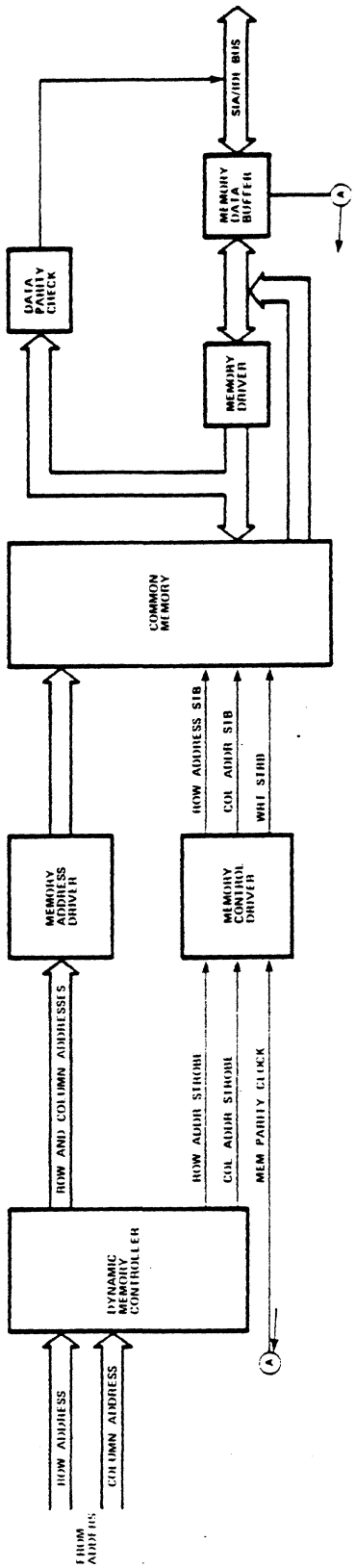


Figure 3-28 Common Memory

3.6.3.8. Memory Address Driver

The Memory Address Driver drives the multiplexed row and column addresses, from the Dynamic Memory Controller, to Common Memory.

3.6.3.9. Memory Control Driver

The Memory Control Driver drives the following control signals to Common Memory (refer to figure 3-28):

- Row Address Clock - When this signal goes low, the Row Address is latched into Common Memory.
- Column Address Clock - When this signal goes low, the Column Address is latched into Common Memory.
- Write Strobe - When this signal is low, Common Memory receives data from the Memory Data Buffer. When high, Common Memory sends data to the Memory Data Buffer.

3.6.3.10. Common Memory

Common Memory is configured as 64K x 9-bit RAM that is used as a buffer, temporarily storing data as it is transferred between the Host and the LD 1200. It is the common storage buffer for data transferred between the Error Correction Unit, the MDS PCA and the ICI PCA.

Access to Common Memory is determined by control signals received from the Dynamic Memory Controller, via the Memory Control Driver. Data is written to Common Memory when Write Strobe is low, and address information is received. When this occurs, data is sent to Common Memory, via the SIA/IDI Bus, through the Memory Data Buffer and Memory Driver.

Data is read from Common Memory when Write Strobe is high, and address information is received. When this occurs, Data plus parity is sent to the Memory Data buffer. The basic Read and Write timing sequences for Common Memory are shown in figure 3-29.

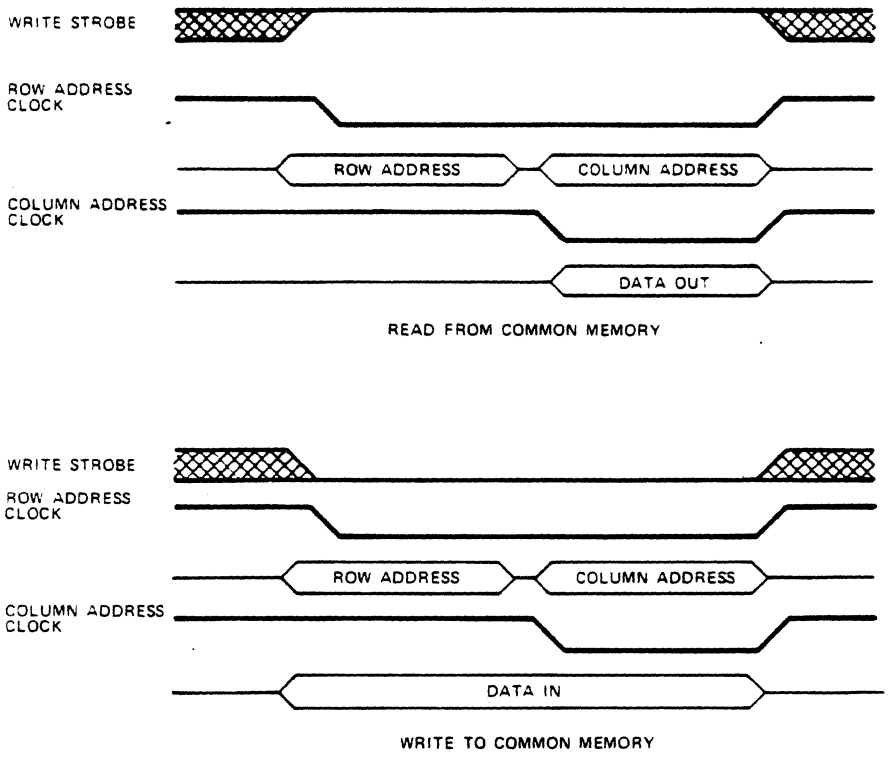


Figure 3-29. Read or Write to Common Memory PB002226-2

3.6.3.11. Memory Data Buffer

The Memory Data Buffer buffers data that is either read from Common Memory, or is to be written into it from the SIA/IDI Bus.

3.6.3.12. Memory Driver

The Memory drivers buffer the outputs of the Memory Data Buffers, before they are placed in the 64K RAMs composing Common Memory.

3.6.3.13. Data Parity Check

Parity checking of each data byte is done as it enters Common Memory. When a parity error is detected, a parity error flag is set, and reported to the ICI PCA via the Memory Parity Error signal.

3.6.4. Error Correction Unit

The Error Correction Unit of the ECC PCA assures data quality on data that is read from the Media. It receives commands from the ICI PCA and manipulates data within Common Memory.

The Error Correction portion of the ECC PCA performs three functions:

- Encodes data (generates parity check symbols)
- Decodes data (generates syndrome bytes)
- Corrects errors

Data quality is assured through the use of the Reed-Solomon Error Correction Code. The Reed-Solomon Error Correction Code allows the LD 1200 to limit unrecoverable data errors to 1 in 10^{12}. Unrecoverable data errors include errors that are detected but uncorrectable, as well as undetected or mishandled errors.

The Error Correction Unit divides a User Data Field into five segments of 205 bytes each. It then performs the following for each of the five segments:

- It encodes data by generating 20 bytes of parity check symbols from the 205-byte segment, resulting in a 225-byte codeword that is ready to write on the Media. The codewords are held in Common Memory until they are written on the Media.
- When a 225-byte codeword is read from the Media, the Error Correction Unit decodes the data, producing 20 bytes of syndromes from the 225 bytes. Syndromes equal to zero indicate no errors, while syndromes not equal to zero indicate an error.
- The 8x305 Microcontroller, in the Error Correction Unit, processes the nonzero syndromes to locate and correct the bit or bits in error.

The capabilities and limitations of the Error Correction Unit in detecting and correcting errors in the 225 bytes are as follows:

- Recoverable Data Errors - The Error Correction Unit can detect and correct errors when the number of data bytes in error is 10 or less in a 225-byte codeword.
- Unrecoverable Data Errors - When the Error Correction Unit correctly detects that more than 10 bytes are in error in a 225-byte codeword, an uncorrectable error is signalled to the ICI PCA. When more than 20 bytes are in error, the Error Correction Unit can possibly misinterpret the errors and report a false correction status.

The probability of misdetecting or miscorrecting errors in a codeword is very low (1×10^{-20}).

Refer to the Modulator Demodulator Synchronizer PCA subsection of this manual for details on how data is interleaved on the Media.

3.6.4.1. Status Port

The Status Port collects status from various circuits on the ECC PCA. It reports the status to the 8x305 Microcontroller. Refer to figure 3-30.

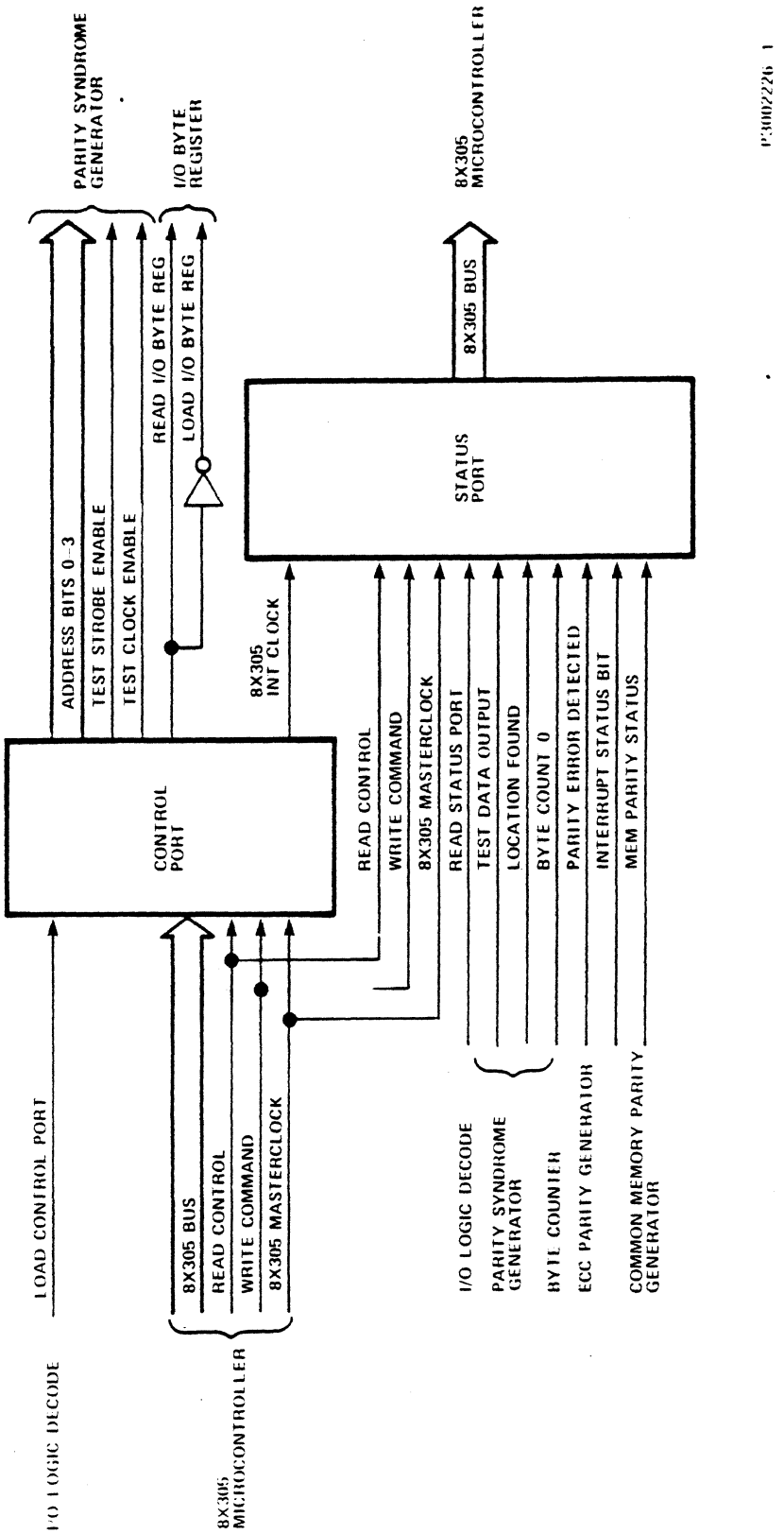


Figure 3-30. Control and Status Ports

3.6.4.2. Command Register

Commands sent by the ICI PCA, via the SIA/IDI Bus, are latched into the Command Register. The 8x305 Microcontroller controls the operation of the Parity Syndrome Generator based on the Command Byte in this register. Refer to table 3-13 for specific decodes.

Table 3-13. Command Byte

BIT	DESCRIPTION
0	Encode/Decode Postfield
1	Encode/Decode User Data Field
2	Encode/Decode Vector Address Field
3	Type of Command: 00 = Reply with ECC PCA Identifier Code 01 = Perform Encode Operation 10 = Perform Decode Operation 11 = Perform Diagnostics
4	
5	New Command Bit
6	Clear Interrupt (active low)
7	Reset ECC (active low)

TBL26

3.6.4.3. Control Port

The Parity Syndrome Generator is programmed for parity or syndrome generation by information sent by the 8x305 to the Control Port. Refer to figure 3-30.

3.6.4.4. 8x305 Bus Transceiver

The 8x305 Bus Transceiver buffers data from the 8x305 Bus to the Parity Syndrome Generator.

3.6.4.5. Parity Syndrome Generator

The Parity Syndrome Generator, a VLSI array, performs encode and decode functions on a specified block of data. The Parity Syndrome Generator encodes by generating 20 bytes of parity check symbols for a given block of data. The block of data with these 20 bytes is called a Codeword. This operation is performed on all data prior to it being written on the Media. The Parity Syndrome Generator decodes data by checking a codeword (data plus parity check symbols) for any errors. This operation results in the generation of 20 syndrome bytes. The syndrome bytes will either indicate that no errors exist, or can be used to locate and correct the existing errors if the number of errors detected is within the correction capabilities of the system.

Actual locating and correction of errors is performed by the 8x305 Microcontroller. Data is transferred into and out of the Parity Syndrome Generator via Direct Memory Access (DMA). The location in Common Memory where the data to be worked on is determined by a start address that is read from a dedicated memory location in Common Memory. The MPU, on the ICI PCA, writes this start address into Common Memory before any commands are given to the Error Correction Unit.

3.6.4.6. Data Buffer

The Data Buffer buffers the data from the Parity Syndrome Generator to the ECC Bus.

3.6.4.7. Byte Counter

The Byte Counter is used to control DMA transfers on the SIA/IDI Bus. The Byte Counter is loaded with the number of bytes minus one that is required for the current operation (Buffer Data Storage or data Assurance Process). The number of bytes is decremented as each byte is fetched from Common Memory. When the number of bytes equals zero, the current operation is complete.

3.6.4.8. Scratchpad Memory

The Scratchpad Memory holds variables that are used by the Error Correction Unit encode and decode operations.

3.6.4.9. 8x305 Microcontroller

The 8x305 Microcontroller and associated stored program control the functions of the error correction process. It controls all encoding, error correction, ECC PCA diagnostics and I/O functions for the Error Correction Unit, as follows:

(1) The ICI PCA loads a dedicated ECC Block Address Location in Common Memory with the address of the desired block of Common Memory.

(2) The ICI PCA issues a command to the Error Correction Unit via the Command Register.

(3) The 8x305 Microcontroller stores the command data in a register internal to itself, then clears the Command Register. The microcontroller processes the command data, and sends control information to the Control Port.

(4) The 8x305 Microcontroller generates parity check symbols as follows:

(a) It looks at the type of command, and obtains a data field offset address from the ECC Block Address Location.

(b) It adds the offset address to the block address, resulting in the desired memory location in Common Memory.

(c) It instructs the Parity Syndrome Generator to perform the appropriate operation. The DMA from Common Memory to the Parity Syndrome Generator begins at the calculated memory location.

(5) When performing a decode operation, the 8x305 Microcontroller determines which byte, if any, is in error. It calculates the location and magnitude of the error and corrects it as follows:

(a) The 8x305 Microcontroller stores syndrome data in the Scratchpad Memory.

(b) The 8x305 searches for the starting address (which was obtained by adding the offset address to the block address as described previously).

(c) It processes subsequent nonzero bytes, using a Chien Search Algorithm, which uses a logorithm from the Look-Up Table PROMs, to find the location of data bytes in Common Memory that are in error. A software algorithm creates a magnitude and location for each byte in error.

(d) A byte in error is read by the 8x305 Microcontroller via the I/O Byte Register.

(e) The 8x305 Microcontroller modifies the erroneous byte by exclusive-ORing it with the error magnitude.

(f) The corrected byte is then sent back to Common Memory via the I/O Registers and the Data Bus Transceiver.

After the execution of the error correction related command, the 8x305 loads status, that is a result of the operation, into an ECC Status Byte in Common Memory. The address of the ECC Status Byte is determined by adding the ECC Status Byte Offset Address to the block address.

When a new Command Byte is issued to the Command Register, and the Clear Interrupt Bit is inactive (high), the 8x305 Microcontroller sets an interrupt, signifying that the operation is complete.

The 8x305 Microcontroller performs diagnostics on the Parity Syndrome Generator (while running diagnostics on the ECC PCA) when requested by the ICI PCA. The results are placed in a Diagnostic Status Byte. The address of the Diagnostic Status Byte is determined by adding the Diagnostic Status Byte Offset Address to the block address.

The 8x305 Microcontroller controls associated circuitry by means of the 8x305 Bus. It generates a 5-MHz 8x305 Master Clock to clock I/O devices and to synchronize external logic.

3.6.4.10. Instruction PROMs

The Instruction PROMs contain the microcode instruction set for the 8x305 Microcontroller.

3.6.4.11. Fast I/O PROMs

The Fast I/O PROMs contain the data for I/O selection (via the I/O Logic Decode circuitry) and Look-Up Table Addresses. The data requested is latched into the Fast I/O Register.

3.6.4.12. Fast I/O Register

The Fast I/O Register latches data from the Fast I/O PROMs. This data is held for one cycle of the 8x305 Microcontroller.

3.6.4.13. I/O Logic Decode

The I/O Logic Decode decodes three bits received from the Fast I/O Register. It is used to load various registers in the Error Correction Unit. Refer to figure 3-31 for specific decodes.

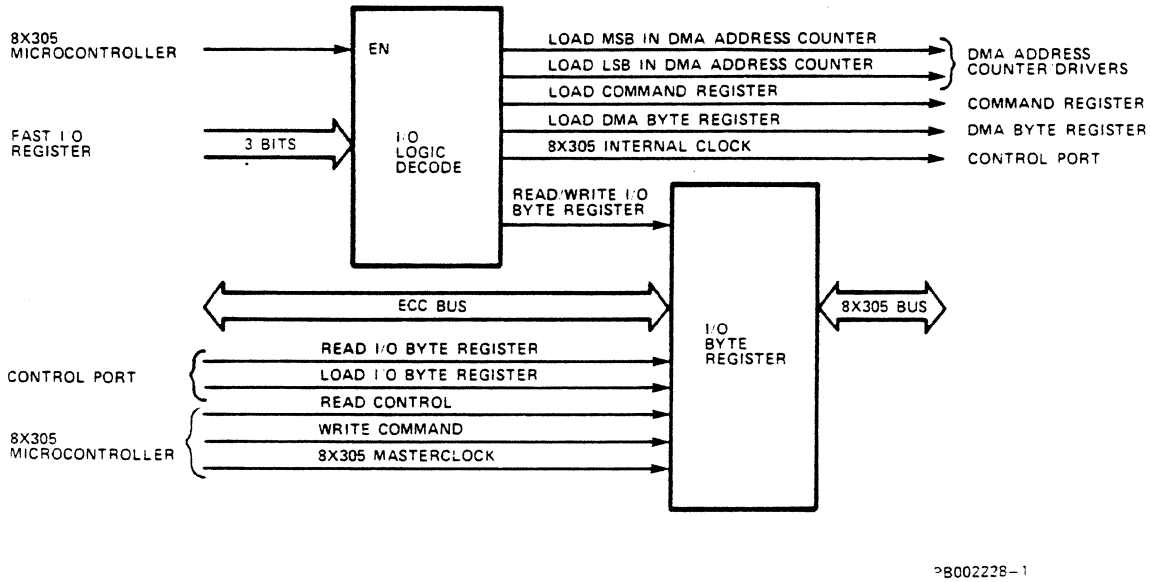


Figure 3-31. I/O Logic Decode

3.6.4.14. Latch

The 8x305 Microcontroller loads the address for the desired logorithm in the Look-Up Table into the Latch.

3.6.4.15. Look-Up Table PROMs

The Look-Up Table PROMs contain logorithms that are used by the Chien Search Algorithm for processing syndrome data. These PROMs are addressed via the 8x305 Bus and Fast I/O Register.

3.6.4.16. Look-Up Table Port

The Look-Up Table Port provides access to the Look-Up Table PROMs.

3.6.4.17. I/O Byte Register

The I/O Byte Register transfers data between Common Memory and the 8x305 Microcontroller. The microcontroller reads the beginning memory location for use in performing encode and decode operations. When data is corrected by the 8x305 Microcontroller, one byte at a time of corrected data is transferred to Common Memory via the I/O Byte Register.

3.6.4.18. DMA Address Counter/Drivers

The DMA Address Counter is used for DMA address generation during DMA transfers to and from Common Memory. It is enabled when the Error Correction Unit portion of the ECC PCA is enabled, and ECC PCA Reset is inactive. It is clocked by the 8x305 master clock.

3.6.4.19. Data Parity Check Generator

The Data Parity Check Generator generates and checks data parity on the Buffered SIA Bus for any data that is being written to Common Memory.

3.7. SERVO/DRIVE CONTROL PCA

The Servo/Drive Control PCA is a processing card between the ICI PCA and the slave Drive. It is the intelligence of the slave Drive. It communicates with the ICI PCA via the IDI Bus, receiving commands and sending Drive status.

The Servo/Drive Control PCA contains two microprocessors. The 8039 Microprocessor, referred to as the Drive Control Microprocessor throughout these subsections, provides the Drive control functions for the LD 1200. The 8031 Microprocessor, referred to as the Servo Control Microprocessor throughout these subsections, controls the servo functions of the LD 1200.

The Servo/Drive Control PCA controls the Seek Velocity Profile of the LD 1200. It provides seek velocity data to the Servo Systems PCA.

The Servo/Drive Control PCA performs the LD 1200 initialization sequences. It initiates data Rewrites and fault and error handling.

The Servo/Drive Control PCA monitors and controls the following, taking appropriate action when necessary:

- Monitors the Operator Panel switches and controls the switch LEDs
- During data transfer, it monitors read/write error status, Drive error status, and track LSB miscompare

- Monitors slave device status
- Monitors focus and tracking status
- Monitors Power Supply status
- Controls error recovery procedures
- Controls coarse and fine tracking
- Controls long and short Seeks
- Controls focus
- Controls laser power levels

Detailed descriptions of the Servo/Drive Control circuitry are in the following subsections.

3.7.1. Interface Signal Descriptions

Interface signal descriptions for the Servo/Drive Control PCA are as follows (refer to figure 3-32):

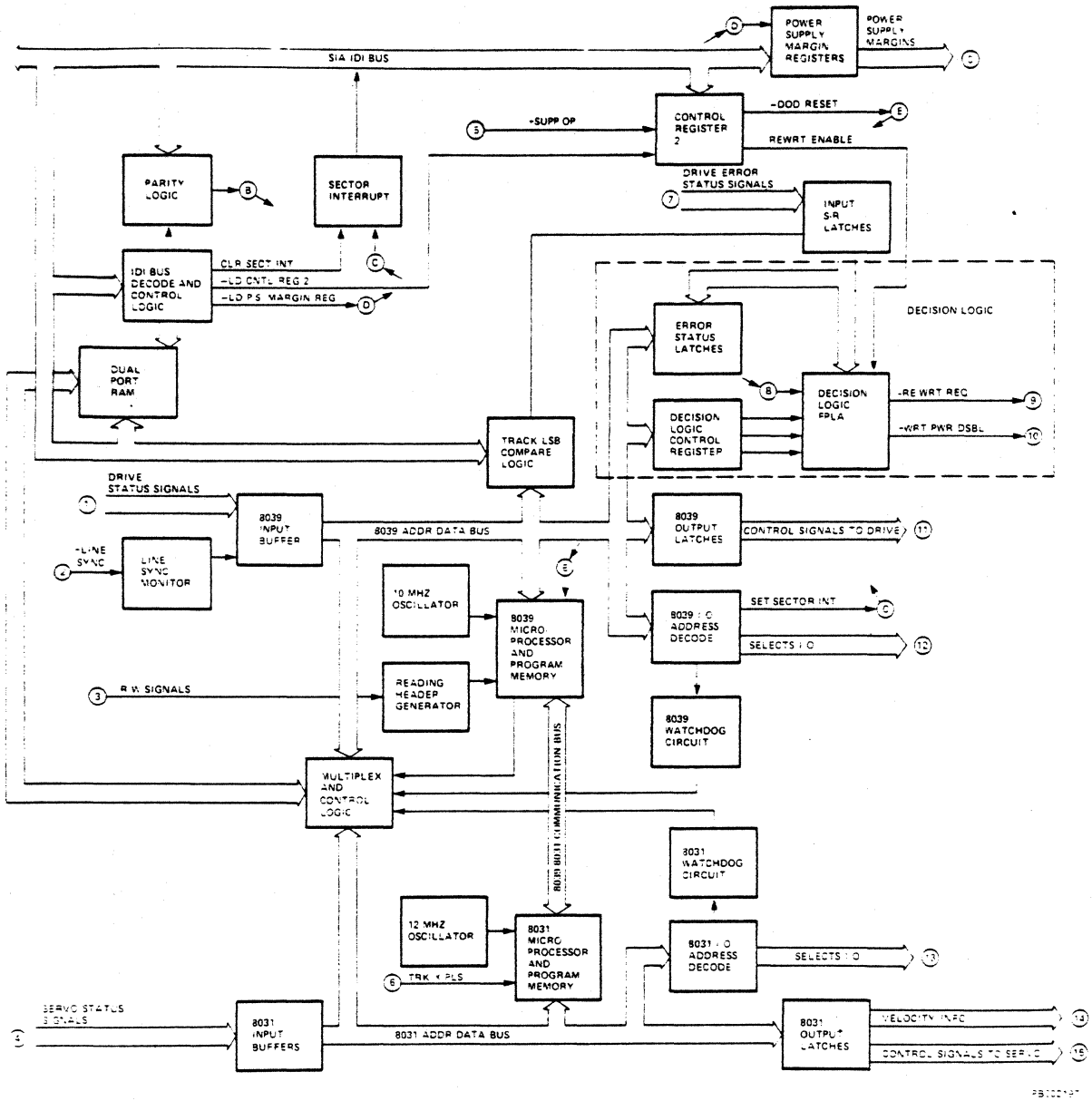


Figure 3-32. Servo Drive Control PCA Block Diagram

(1) MISCELLANEOUS DRIVE STATUS SIGNALS - The Servo/Drive Control PCA monitors the following Drive status via the 8039 Input Buffers:

- Sync pulses
- Motor speed
- Laser intensity
- Drive temperature
- AC from the Power Supply
- Operator Panel switches
- Cartridge status: installed, write protected

Refer to the 8039 Input Buffer subsection for greater detail.

(2) +LINE SYNC - This signal, generated by the Power Supply, is the same frequency as the ac input. It is active when the input ac amplitude is above the minimum level. The Servo/Drive Control PCA monitors this signal and generates a Line Sync Fault if two consecutive line sync pulses are missing. This allows the current sector Read or Write operation to be completed, then causes a retract and laser power shutdown to occur. This signal is also used as a timing reference in the Watchdog Circuits.

(3) R/W SIGNALS - The following Read/Write signals are received from the Modulator Demodulator Synchronizer (MDS) PCA:

LOAD TRACK LOW
BEGINNING OF SECTOR PULSE

The Servo/Drive Control PCA uses these signals to determine when the Modulator Demodulator Synchronizer PCA has transferred the header.

Beginning of Sector Pulse also starts a Sector Interrupt Routine, allowing the Drive Control Microprocessor to gather Drive status.

Refer to the Reading Header Generator subsection for greater details on these signals.

(4) SERVO STATUS SIGNALS - The Servo/Drive Control PCA receives servo status signals from the Servo Systems PCA via the 8031 Input Buffers. Refer to 8031 Input Buffer subsection for greater detail.

(5) +SUPP OP (Supply Operative Status) - This signal is used by the Servo/Drive Control PCA to generate a Power-On Reset for the Servo Control and Drive Control Microprocessors and the IDI Bus. It is generated by the Power Supply, and goes high a minimum of 1 millisecond after all dc supplies are within operating range. It goes low within 5 microseconds after any of the supplies drop out of operating range specifications.

(6) +TRK X PLS (Track Crossing Pulse) - This signal is generated by the Error Signal Generator PCA. A pulse is generated each time the Tracking Error signal (TRK ERROR) crosses a zero threshold. The Servo/Drive Control PCA uses this signal to measure Seek velocity at any given time during a Seek. This signal also carries information as to how many tracks have been crossed at any point during a Seek.

(7) DRIVE ERROR STATUS SIGNALS - The following signals carry current Drive status to the Servo/Drive Control PCA from various PCAs in the LD 1200:

STATUS SIGNAL	ORIGIN
WRITE TRANSFER STATUS	MDS PCA
WOBBLE ERROR STATUS	MDS PCA
CERTIFY FLAG	MDS PCA
MISSING DATA FIELD	MDS PCA
WRITE PROTECT STATUS	MDS PCA
DATA DETECT	MDS PCA
DRDW ERROR STATUS	MDS PCA
TRACK MISCOMPARE STATUS	S/DC PCA
LOST FOCUS STATUS	SS PCA
SYNC ERROR STATUS	MDS PCA
PLL ERROR STATUS	R/WC PCA
READ POWER ERROR STATUS	R/WC PCA
WRITE POWER ERROR STATUS	R/WC PCA
QUAD HIGH STATUS	R/WC PCA
MDS PARITY ERROR STATUS	MDS PCA
OFF TRACK STATUS	SS PCA

Refer to the Decision Logic subsection for greater detail on these signals.

(8) POWER SUPPLY MARGINS - The Servo/Drive Control PCA supplies power supply margin controls, via these signal lines, for diagnostic purposes. Refer to the Power Supply Margin Register subsection for greater detail.

(9) -REWRT REQ (Rewrite Request) - This signal is sent to the Modulator Demodulator Synchronizer (MDS) PCA. It is made low to request a Rewrite operation for the next sector. This signal may go low at any time during a sector, and is cleared at the beginning of the next sector.

Rewrite Request is enabled by the ICI PCA via Control Register #2. The ICI PCA counts the number of Rewrites performed and disables further Rewrites when the maximum number allowed per sector has occurred.

A Rewrite occurs when any of the following conditions occur:

PLL ERROR
DRDW ERROR
SYNC ERROR

If any other errors also occurs, the Rewrite Request is cancelled.

(10) +WRT PWR DSBL (Write Power Disable) - This signal is sent to the Read/Write Control PCA. When high, the Read/Write Control PCA disables laser write power. Write power is disabled when the Drive is write protected.

When a PLL, DRDW or Sync Error occurs, this signal goes high, and writing is disabled until the end of the current sector. A Rewrite is attempted in the next sector if enabled. When rewrites are not enabled, writing is disabled until a CLR ERRORS command is received from the ICI PCA.

Write power is also disabled and this signal goes high when any of the following conditions occur:

WRITE POWER ERROR
READ POWER ERROR
OVERWRITE ERROR
QUAD HIGH STATUS
FOCUS ERROR
TRACKING ERROR
TRACK MISCOMPARE ERROR
WOBBLE ERROR
PARITY ERROR
MISSING DATA FIELD

When one of these errors occurs, Rewrites are not performed and write power remains disabled until a CLR ERRORS command is received from the ICI PCA via Control Register #1.

Write power is disabled, and this signal is high, at the end of a sector in which a fault occurs. It remains disabled until a Reset is issued.

(11) CONTROL SIGNALS TO DRIVE - The Servo/Drive Control PCA provides control signals to the Baseplate, Operator Panel, Power Supply, Focus Servo Loop on the Servo Systems PCA, and the Power Control Loop on the Read/Write Control (R/WC) PCA. Refer to the 8039 Output Latch Subsection for greater detail.

(12) 8039 I/O SELECTS - These signals allow the Drive Control Microprocessor to select output latches and input buffers. Refer to the 8039 Address Decode subsection for greater detail.

(13) 8031 I/O SELECTS - These signals allow the Servo Control Microprocessor to select the output latches and input buffers. Refer to the 8031 Address Decode Subsection for greater detail.

(14) VELOCITY INFORMATION TO TRACKING SERVO - These signal lines carry velocity error data to the Servo Systems PCA. The Servo/Drive Control PCA uses track crossing information, generated by the Error Signal Generator (ESG) PCA, to calculate the actual velocity of the Fine Servo Motor. This calculated velocity is compared against an ideal velocity curve that is stored in ROM. The appropriate Seek Velocity Error is then sent to the Servo Systems PCA to accelerate or brake the Fine Servo Motor as necessary. Refer to the 8031 Output Latch subsection for greater detail.

(15) CONTROL SIGNALS TO SERVO - The Servo/Drive Control PCA sends signals to the Servo Systems PCA, the ESG PCA and the Read/Write Control PCA. Refer to the 8031 Output Latch subsection for detailed information.

3.7.2. IDI Bus

The Servo/Drive Control PCA communicates with the ICI PCA and the MDS PCA via the IDI Bus. The IDI Bus consists of:

- Thirteen-bit address bus
- Eight-bit data bus (plus one bit parity)
- Control signals
- Clock signals

Refer to the Interfaces subsection in this manual for signal and protocol details.

3.7.2.1. IDI Address Bus

The IDI Address Bus is a bidirectional bus between the ICI PCA, the MDS PCA, the ECC PCA, and the Servo/Drive Control PCA. In relation to the Servo/Drive Control PCA, it carries address information to control which IDI input/output (I/O) port (i.e., which Dual Port RAM register, etc.) will be written into or read by the ICI PCA.

The Servo/Drive Control PCA uses IDI Address Bits 0 through 7, the eight least-significant bits of thirteen total on the IDI Address Bus, to decode which I/O ports are being addressed by the IDI Bus.

3.7.2.2. IDI Data Bus

The Servo/Drive Control PCA communicates with the ICI PCA and the MDS PCA via the IDI Data Bus. This eight-line bidirectional bus transfers data from the ICI PCA and the MDS PCA to the Servo/Drive Control PCA I/O ports and from the Servo/Drive Control PCA to the ICI PCA (i.e., Dual Port RAM registers, etc.).

3.7.2.3. IDI Bus Control Signals

The IDI Bus Control signals indicate whether a Read or Write operation is to be performed, and whether an I/O operation or a memory access is to occur. The control signals can also cause each PCA to re-initialize.

3.7.2.4. IDI Bus Clock Signals

The clock signals are used to synchronize data transfers between the several PCAs that are connected to the IDI Bus.

3.7.3. Power Supply Margin Registers

The Power Supply Margin Register is an IDI input/output (I/O) port, and is controlled by the ICI PCA. It supplies power supply margin controls to the Power Supply for diagnostic purposes.

MARGIN DISABLES

These four signals (+5V MRG DSBL, -5V MRG DSBL, +12V MRG DSBL, -12V MRG DSBL) are sent to the Power Supply. A margin disable allows the associated margin control line to force the pertinent output voltage up or down 5% from nominal value.

MARGIN DISABLE	ASSOCIATED MARGIN CONTROL
Low	Enabled
High	Disabled (associated output nominal)
Open	Disabled (associated output nominal)

MARGIN CONTROLS

These four signals (+5V MRG CNTL, -5V MRG CNTL, +12V MRG CNTL, -12V MRG CNTL) are sent to the Power Supply. A margin control forces the associated power supply output voltage up or down by 5% when the associated margin disable line is enabled (low):

POWER SUPPLY OUTPUT	MARGIN DISABLE	MARGIN CONTROL	ASSOCIATED OUTPUT VOLTAGE
+5V	low	low	+5.355 Vdc ±2%
+5V	low	high or open	+4.847 Vdc ±2%
+5V	high or open	disabled	5 Vdc (nominal)
-5V	low	low	-5.25 Vdc ±2%
-5V	low	high or open	-4.75 Vdc ±2%
-5V	high or open	disabled	-5 Vdc (nominal)
+12V	low	low	+12.6 Vdc ±2%
+12V	low	high or open	+11.4 Vdc ±2%
+12V	high or open	disabled	+12 Vdc (nominal)
-12V	low	low	-12.6 Vdc ±2%
-12V	low	high or open	-11.4 Vdc ±2%
-12V	high or open	disabled	-12 Vdc ±2%

3.7.4. IDI Bus Decode and Control Logic

The IDI Bus Decode and Control Logic generates the gating signals for the Dual Port RAM register file and Control Register #2. It also generates a parity strobe to clock Parity Logic, and a Clear Sector Interrupt strobe to clear the Sector Interrupt Logic. Refer to figure 3-33.

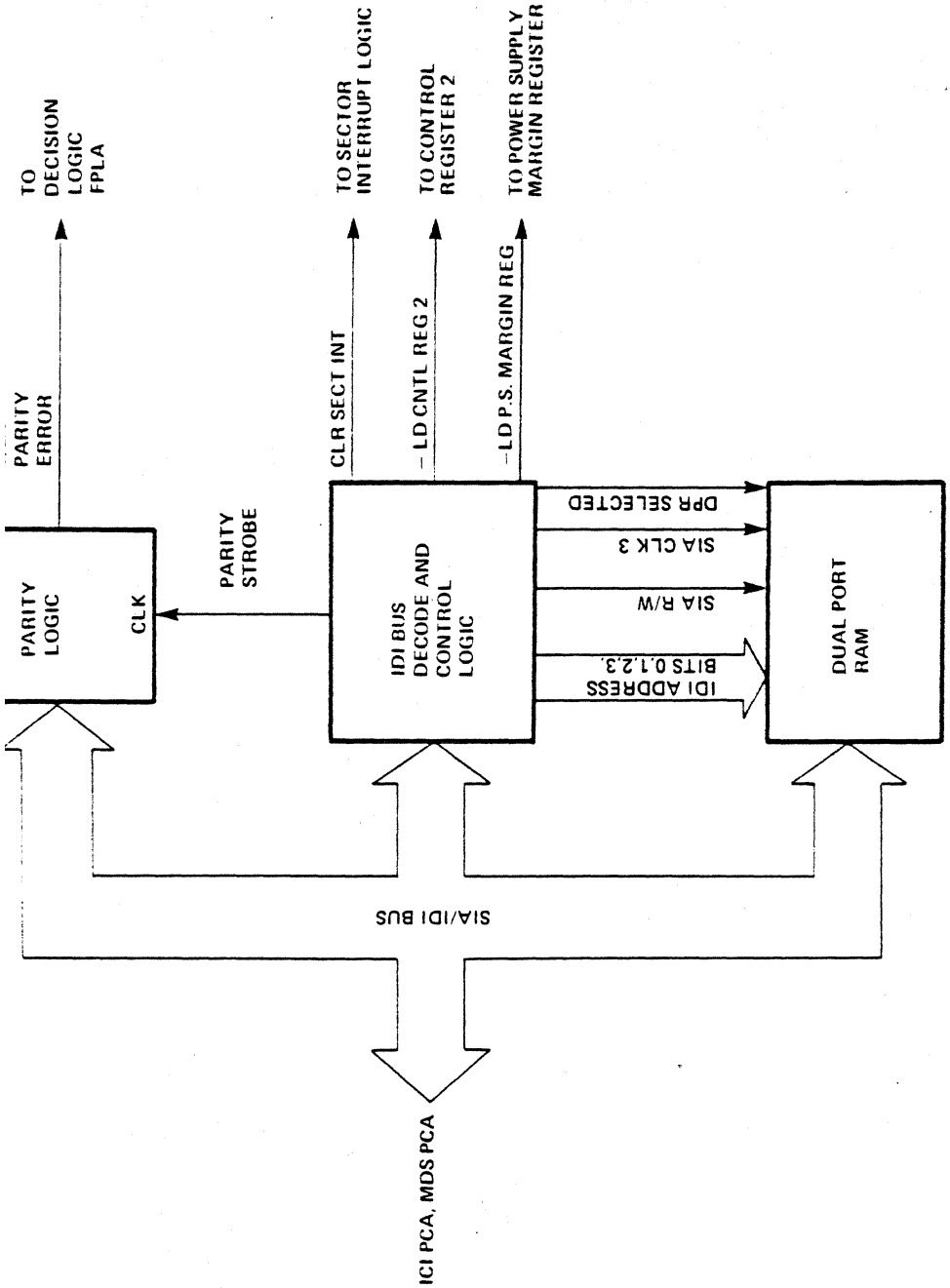


Figure 3-33 IDI Bus Decode and Control Logic

The IDI Bus Decode and Control Logic decodes IDI Address Bus bits 0 through 4 to generate a specific address decode as shown in table 3-14.

Table 3-14. IDI Bus Address Decode

IDI ADDRESS BITS (HEX)		
6-4	3-0	DUAL PORT RAM REGISTERS
1	0	Flag Register #1
1	1	Flag Register #2
1	2	Header Sector
1	3	Header Track Low
1	4	Header Track High
1	5	Status Register #1
1	6	Status Register #2
1	7	Status Register #3
1	8	Fault/Error Register #1
1	9	Fault/Error Register #2
1	A	Fault/Error Register #3
1	B	Desired Sector
1	C	Desired Track Low
1	D	Desired Track High
1	E	Actual Sector
1	F	Control Register #1
		Individual Registers
2	0	Control register #2
2	1	Load Power Supply Register
2	2	Clear Sector Interrupt

TBL09

3.7.5. Parity Logic

The Parity Logic circuitry generates parity for all data placed on the IDI Bus by the Servo/Drive Control PCA and checks the parity of all IDI data received by that PCA.

3.7.6. Control Register #2

Control Register #2 provides control signals to the hardware on the Servo/Drive Control PCA for busmasters on the SIA/IDI BUS. It is clocked by -LD CNTL REG 2 (from the IDI Bus Decode and Control Logic), and controls the following Drive functions:

Bit 0 = LD 1200 Reset - When set, the Drive is in reset condition. When set, then cleared, the Drive is released from reset and performs an initialization routine that is equivalent to a Power-on Reset. This bit is used to clear Drive faults.

Bit 1 = Rewrite Enable - When a PLL error, sync error, or DRDW error is detected, during writing, and this bit is high, an attempt is made to rewrite data in the next sequential sector.

Bits 2 through 7 = Reserved for future use.

Control Register #2 is reset by the absence of +SUPP OP, which is generated by the Power Supply. +SUPP OP goes high a minimum of 1 millisecond after all dc supplies are within operating range. It goes low within 5 microseconds after any of the supplies drop out of operating range specifications.

3.7.7. Dual Port RAM

The Dual Port RAM, via the IDI bus, is the communication link between the Servo/Drive Control PCA and the ICI and MDS PCAs. Both the Drive Control and the Servo Control Microprocessors have access to the Dual Port RAM.

At the beginning of each sector, the Drive Control Microprocessor gathers information from the previous sector and puts it in the Dual Port RAM. It then generates a Sector Interrupt to the ICI PCA via the Sector Interrupt Logic. The ICI PCA acknowledges the interrupt by selecting the Clear Sector Interrupt I/O port.

The Dual Port RAM is also used for the following:

- The ICI PCA sends various commands to the Servo/Drive Control PCA via a register in the Dual Port RAM.
- During Seeks, Desired and Actual Header addresses are transferred from the Drive Control Microprocessor (8039) to the Servo Control Microprocessor (8031) via the Dual Port RAM.
- Each time a header is read from the Media, the MDS PCA sends the header information over the IDI Bus to registers in the Dual Port RAM.
- During diagnostics, the Dual Port RAM is used to transfer test numbers and status between the Drive Control Microprocessor, Servo Control Microprocessor, and IDI Controller PCA.

The Dual Port RAM contains sixteen eight-bit register files:

FLAG REGISTER #1
FLAG REGISTER #2
HEADER SECTOR REGISTER
HEADER TRACK LOW REGISTER
HEADER TRACK HIGH REGISTER
STATUS REGISTER #1
STATUS REGISTER #2
STATUS REGISTER #3
FAULT/ERROR REGISTER #1
FAULT/ERROR REGISTER #2
FAULT/ERROR REGISTER #3
DESIRED SECTOR REGISTER
DESIRED TRACK LOW REGISTER
DESIRED TRACK HIGH REGISTER
ACTUAL SECTOR REGISTER
CONTROL REGISTER #1

The contents of these registers are described in the following subsections:

3.7.7.1. Flag Register #1

Flag Register #1 contains write protect bits for the Actual Sector Register and Control Register #1, and flag bits for the Header Sector Register, Header Track Lo and Hi Registers, and Status Registers #1, 2, and 3. The flag bits are used for handshaking (control and acknowledgement) between the Servo/Drive Control PCA and the ICI PCA.

3.7.7.2. Flag Register #2

Flag Register #2 contains flag bits for the Desired Sector Register, Desired Track Low and High Registers, Actual Register, Control Register #1, and Fault/Error Registers #1, 2, and 3.

3.7.7.3. Header Sector

Header Sector Register contains the sector number read from the header of the current sector when the Drive is READY. Bits 0 through 4 specify sector number; bits 5 through 7 are unused. This register is loaded by the MDS PCA.

3.7.7.4. Header Track LSB

Header Track LSB Register contains the track least-significant byte of the header of the current sector when the Drive is READY. This register is loaded by the MDS PCA.

3.7.7.5. Header Track MSB

Header Track MSB Register contains the track most-significant byte of the header of the current sector when the Drive is READY. This register is loaded by the MDS PCA.

3.7.7.6. Status Register #1

Status Register contains status bits concerning the present condition of the LD 1200.

Bit 0 = Unit Ready - This bit is high when the Spindle is up to speed and all Drive initialization routines have completed successfully.

Bit 1 = On Track - When low, this bit indicates that the Drive servo and tracking circuits are not locked onto the target track as specified by the Desired Track Registers. This occurs during Seeks, automatic Jumpbacks, and when focus, tracking, or synchronization is lost.

Bit 2 = Start/Stop Request - This bit reflects the state of the START/STOP switch on the Operator Panel. When set, the switch is in the START position. The ICI PCA uses this bit to monitor manual requests for Spindle power up and down, then converts these requests into Spindle Motor actions.

Bit 3 = Device Fault - When set, this bit indicates that one or more device faults exist in the Drive.

Bit 4 = Cartridge Loaded - When set, this bit indicates that a Data Cartridge is installed.

Bit 5 = Write Protect Switch - When set, this bit indicates that the WRITE PROTECT switch on the Operator Panel is active. The ICI PCA converts this status to a Write Protect command.

Bit 6 = Cartridge Write Protected - When set, this bit indicates that the Data Cartridge in the LD 1200 has the Write Protect Tab in write protect position.

Bit 7 = Device Error - When set, this bit indicates that one or more error conditions exist in the LD 1200. When a PLL, DRDW, Data Sync, or Overwrite Error occurs during a Write operation, it is cleared in the next sector if Rewrites are enabled. If Rewrites are not enabled, or when any other error occurs during a Write operation, the laser is disabled until the error is cleared by the ICI PCA.

3.7.7.7. Status Register #2

Bit 0 = Rewrite Requested - When set, this bit indicates that an automatic Rewrite is being performed in the current sector. The ICI PCA monitors this bit to determine when to inhibit Rewrites, and to identify when a Rewrite has been successful.

Bit 1 = Write Not Started - When set, this bit indicates that a Write operation intended for the previous sector was aborted prior to anything being written in the sector. The sector is therefore still usable for future Write operations. If a Write was started and this bit is clear, the sector was at least partially written and is unusable for future Write operations.

Bit 2 = Laser Degraded - When set, this bit indicates that the laser should be replaced prior to attempting a Write operation. The read capability of the laser is not necessarily affected by the presence of this status bit.

Bit 3 = Error Recovery in Progress - When set, this bit indicates that the LD 1200 is in the process of attempting an error recovery procedure.

Bit 4 = Illegal Seek - When set, this bit indicates that the Servo/Drive Control PCA received an illegal address as part of a request for a Seek.

Bit 5 = Data Detect - This bit is only active during Write operations. When set, this bit indicates that enough data was detected in the previous physical sector to cause the DRDW threshold criteria to be met. This status is used in the case of an Overwrite to determine whether the sector contained data or no data and a defect in the Write Protect Byte.

Bit 6 = Read or Write in Progress - This bit, when set, indicates that a Read or Write is being performed during the sector in which this bit is reported. The ICI PCA uses this bit to verify that a command is received by the LD 1200.

Bit 7 = Quad Sum Low - When set, this bit indicates that the reflected light from the Media has fallen below an acceptable level, therefore the output from the quad sum network is below an allowable level.

3.7.7.8. Status Register #3

Bit 0 = Power Supply Overtemperature - When set, this bit indicates that an overtemperature condition has been detected in the LD 1200 Power Supply.

Bit 1 = Cage Overtemperature - When set, this bit indicates that an overtemperature condition exists in the LD 1200 Card Rack.

Bit 2 = Certify Flag - When set, this bit indicates that a Certify Flag was read in the current sector signifying a flaw in the next sector. The ICI PCA will therefore not issue a Write command for the next sector.

Bits 3 through 7 = Reserved for future use.

3.7.7.9. Fault/Error Register #1

Fault/Error Register #1 contains status bits that define various LD 1200 error and fault conditions. When Bit 2 (Report Fault Bit) of Control Register #1 is high, faults are available in this register. When the Report Fault Bit is low, errors are available in this register. The specific fault and error conditions defined as Fault/Error Register #1 are as follows:

ERROR BITS

Bit 0 = Seek Error - When set, this bit indicates that the LD 1200 was unable to successfully complete a Seek operation requested by the ICI PCA.

Bit 1 = Reserved for future use.

Bit 2 = Wobble Error - When set, this bit indicates that an error was detected while reading the Wobble Bytes in previous Sector Headers. When this occurs, any current Write operation is aborted.

Bit 3 = Missing Data Field Error - When set, this bit indicates that, in the previous sector, an attempt was made to write a Postfield and no Data Field had previously been written.

Bit 4 = Overwrite Error - When set, this bit indicates that a DRDW error was encountered during an attempted Write of one of the three Write Protect bytes in the previous sector. This may be the result of a Media flaw at that location, or because the sector was previously written. The data Rewrite resulting from this error causes one revolution latency for the ICI PCA to reissue the function.

Bit 5 = Read Header Error - When set, this bit indicates that during a Seek, the Servo Microprocessor was unable to read Header addresses while verifying the desired track address.

Bit 6 = DRDW Error - When set, this bit indicates that more than the allowable number of DRDW errors were detected during the Write of the previous sector. The Write operation is terminated when the DRDW threshold is reached. If Rewrites are enabled, an automatic Rewrite occurs in the next sequential sector.

Bit 7 = Track Miscompare Error - When set, this bit indicates that a miscompare has been detected between an internal track LSB and the lower byte of the track address read from the Media. If this error is detected, Writing is inhibited.

Reads continue when this error occurs. A momentary loss of header information may occur due to a Media flaw in the Header. If a track miscompare occurs repeatedly during Read operations at a particular Media location, the information at this location should be relocated before further Media degradation. Repeated track miscompares may be due to a track positioning error which may be corrected by a Reseek.

FAULT BITS

Bit 0 = Laser Read Power Fault - When set, this bit indicates that an irrecoverable Laser Read Power Error has occurred (laser read power is detected as being too high or too low).

Bit 1 = Laser Write Power Fault - When set, this bit indicates that an irrecoverable Laser Write Power Error has occurred (laser write power is detected as being too high or too low).

Bit 2 = Quad Sum High Fault - When set, this bit indicates that the Quad Sum Signal has exceeded an acceptable tolerance. When this occurs, laser read and write power is immediately disabled, and the focus and tracking circuitry is inhibited.

Bit 3 = Read Header Fault - When set, this bit indicates that the LD 1200 is unable to read the desired track address from the Header, while performing a Seek during LD 1200 initialization or error recovery procedures.

Bit 4 = Motor Speed Fault - When set, this bit indicates that the motor speed is out of tolerance, or that the Spindle Motor did not attain proper speed within 5 seconds of Spindle power up.

Bit 5 = MPU Timeout Fault - When set, this bit indicates that one of the watchdog circuits in the LD 1200 has detected no microprocessor activity for the specified time.

Bit 6 = MPU Self-Test Fault - When set, this bit indicates that one of the microprocessors in the LD 1200 has detected a failure while performing self-tests.

Bit 7 = Wobble Fault - When set, this bit indicates that the Drive is unable to read Servo Wobble Bytes during LD 1200 initialization or error recovery procedures.

3.7.7.10. Fault/Error Register #2

Fault/Error Register #2 contains status bits that define various LD 1200 error and fault conditions. When Bit 2 (Report Fault Bit) of Control Register #1 is high, faults are available in this register. When the Report Fault Bit is low, errors are available in this register. The specific fault and error conditions defined in Fault/Error Register #2 are as follows:

ERROR BITS

Bit 0 = Focus Error Bit - When set, this bit indicates that the LD 1200 has been unsuccessful in maintaining focus on the Media. If the error occurs during a Write operation, the operation is aborted. If the error is resolved within 1 millisecond, the ICI PCA clears the error and the operation continues. If the error is not cleared within 1 millisecond, recovery procedures are attempted. If the recovery is unsuccessful, a Focus Fault is declared.

Bit 1 = Data Synchronization Error - When set, this bit indicates that loss of synchronization has been detected, with respect to the serial data stream to and from the Media. If this error is detected during a Write operation, writing is inhibited and Rewrite attempts are initiated, if enabled. If all attempts to resynchronize fail, a Data Synchronization Fault is declared.

Bit 2 = PLL Error - When set, this bit indicates that the Phase-Locked Loop error has exceeded 30 degrees. When a PLL Error is detected, write power to the Laser Diode is disabled, the error is reported to the ICI PCA, and a Rewrite is performed, if enabled. A PLL Fault is declared if recovery is not possible.

Bit 3 = Laser Read Power Error - When set, this bit indicates that laser read power is detected too high or too low. When this occurs, the laser is disabled and a retract is performed. If the proper laser read power level is regained at Home position, a Seek is reissued to the track where the error occurred. If recovery is not possible at the fully retracted position, a Laser Read Power Fault is declared.

Bit 4 = Laser Write Power Error - When set, this bit indicates that the laser write power has been detected too high or too low. When this occurs, the laser is immediately disabled and a retract is performed. If the proper laser write power level is regained at Home position, a Seek is reissued to the track where the error occurred. If recovery is not possible at the Home position, a Laser Write Power Fault is declared.

Bit 5 = Servo/Drive Control Parity Error - When set, this bit indicates that a parity error was detected when the Servo/Drive Control PCA received a data byte on the IDI Bus. When this error occurs during a Write operation, the operation is aborted. The ICI PCA clears the error and attempts a Rewrite on the next revolution.

Bit 6 = MDS Parity Error - When set, this bit indicates that a parity error was detected when the MDS PCA received a data byte on the IDI Bus. When this error occurs during a Write operation, the operation is aborted. The ICI PCA clears the error and attempts a Rewrite on the next revolution.

Bit 7 = Tracking Error - When set, this bit indicates that the LD 1200 was unable to maintain tracking. When this occurs, a recovery attempt is initiated at the current Carriage position. If tracking is not recovered, the Carriage is retracted and tracking initialization occurs from Home position. When the recovery procedures are successful, a Seek is reissued to the track where the error occurred. When the recovery procedures are unsuccessful, a Tracking Fault is declared.

FAULT BITS

Bit 0 = PLL Fault - When set, this bit indicates that the Phase-Locked Loop (PLL) Circuit, on the Read/Write Control PCA, is unable to synchronize with the Media servo clock.

Bit 1 = Focus Fault - When set, this bit indicates that an irrecoverable focus error has occurred.

Bit 2 = Seek Fault - When set, this bit indicates that the LD 1200 is unable to perform a Seek to Track 0 during LD 1200 Initialization or error recovery procedures. This bit is also set if the LD 1200 is unable to perform a Carriage Retract.

Bit 3 = Tracking Fault - When set, this bit indicates that an irrecoverable tracking error has occurred.

Bit 4 = Line Sync Fault - When set, this bit indicates that the Power Supply has detected a loss of at least two consecutive ac cycles. When this occurs, the current Read or Write operation is stopped at the next Sector Mark, and the Carriage is retracted.

Bit 5 = Data Synchronization Fault - When set, this bit indicates that an irrecoverable Data Synchronization Error has occurred.

Bit 6 = Quad Sum Low Fault - When set, this bit indicates that the Quad Sum Signal has fallen below an acceptable tolerance. When this occurs, laser read and write power is immediately disabled, and the tracking and focus circuitry is inhibited.

Bit 7 = Reserved for future use.

3.7.7.11. Fault/Error Register #3

Fault/Error Register #3 contains status bits that define various LD 1200 error and fault conditions. When Bit 2 (Report Fault Bit) of Control Register #1 is high, faults are available in this register. When the Report Fault Bit is low, errors are available in this register. The specific fault and error conditions defined in Fault/Error Register #3 are as follows:

ERROR BITS

Bit 0 = Missing Data Field - When this bit is set, it indicates that a Postfield Write was attempted in a sector that did not contain a previously written Data Field Write Protect Byte.

Bits 1 through 7 = Reserved for future use.

FAULT BITS

Bits 0 through 7 = Reserved for future use.

3.7.7.12. Desired Sector Register

This register is loaded with the sector number to be read for the pending data operation with the Media. Bits 0 through 4 specify sector number. Bits 5 through 7 are unused.

If the ICI PCA does not begin the Read or Write operation at the specified sector, a one track Jumpback is performed, if enabled, to maintain the relative Fine Servo Motor position on the Media.

This register is also used to determine On-Track status.

3.7.7.13. Desired Track LSB and MSB

These registers are loaded with the track number of the desired track for Seek operations.

MSB - Bits 8 through 14 of the track address are loaded into this register. Bit 15 is a sign bit that specifies the track location relative to the start of the user data band.

LSB - Bits 0 through 7 are loaded into this register. The MSB register must be loaded prior to the LSB. When the LSB is loaded, the LD 1200 initiates a Seek to the specified track.

If an illegal track address is received (not within tracks 0 - 31,999 decimal), the ON TRACK error signal is deactivated, and an illegal Seek and Seek Error are indicated (Status Register #2, Bit 4). Greater Seek ranges are allowed when the LD 1200 is in diagnostic mode.

3.7.7.14. Actual Sector Register

This register contains a sector address computed by the Drive Control Microprocessor representing the actual sector location on the Media. The contents of this register are valid only when the ON TRACK signal is active.

Bits 0 through 4 = Actual sector

Bits 5 through 6 = Not used

Bit 7 = Sectors sequential bit

3.7.7.15. Control Register #1

This register is loaded by the ICI PCA to control various Drive functions as follows:

Bit 0 = Spindle Power Up - When this bit is set, the Spindle Motor powers up if a Data Cartridge is properly loaded, the START/STOP switch is in START position, and no faults or errors exist. When cleared, the Spindle Motor halts regardless of the position of the START/STOP switch.

Bit 1 = Clear Errors - When set, this bit causes all Drive errors to be reset. This is independent of sector timing. Drive faults must be cleared by resetting the Drive.

Bit 2 = Report Faults - When set, this bit causes the Drive to display faults in the Fault/Error Registers.

Bit 3 = Enable Jumpbacks - When set, the LD 1200 performs the required Jumpback whenever a Read or Write operation is not being performed.

Bit 4 = Write Protect - When set, the Media is write protected. When cleared, the Media is available for writing, unless the Data Cartridge Write Protect Tab is activated.

Bit 5 = Write Error Override - When set, PLL, Sync, and DRDW Errors are overridden and Rewrites are inhibited. This bit is for use during testing and fault isolation only.

Bit 6 = Latch First Error - This bit is only used when the Drive is in diagnostic mode (bit 7 is set). When this bit is set, only the first error that occurs in a sector is reported to the ICI PCA.

Bit 7 = Diagnostic Mode - When set, the Drive is in diagnostic mode.

3.7.8. Multiplex and Control Logic

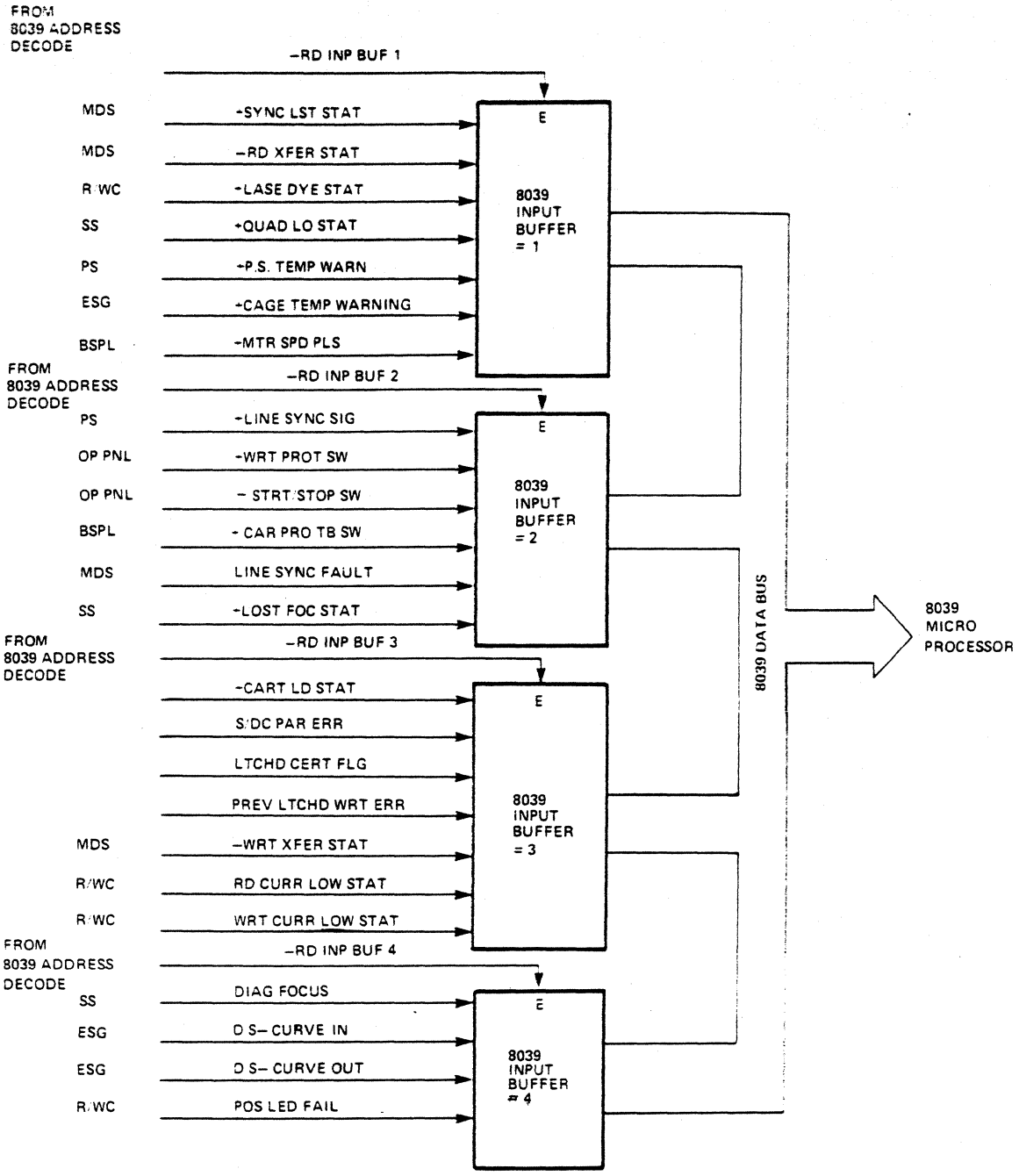
The Multiplex and Control Logic circuitry allows the Servo Control Microprocessor or the Drive Control Microprocessor to communicate with the Dual Port RAM.

3.7.9. Line Sync Monitor

When the Line Sync Monitor detects that two consecutive Line Sync Pulses are missing, indicating a two cycle loss of ac power in the Power Supply, it generates a Line Sync Fault to the 8039 Input Buffers.

3.7.10. 8039 Input Buffers

The 8039 Input Buffers allow the Drive Control Microprocessor to monitor the following Drive status (refer to figure 3-34):



LEGEND:

MDS = MODULATOR DEMODULATOR SYNCHONIZER PCA
R/WC = READ/WRITE CONTROL PCA
SS = SERVO SYSTEMS PCA
PS = POWER SUPPLY
ESG = ERROR SIGNAL GENERATOR PCA
BSPL = BASEPLATE
OP PNL = OPERATOR PANEL

Figure 3-34 8039 Input Buffers PB002202-1

+SYNC LST STAT (Sync Lost Status)

This status is generated by the MDS PCA. It is monitored during the start-up sequence after tracking is initialized. Synchronization should occur within 10 milliseconds after tracking is established. If this does not occur, this signal goes high and a Sync Fault is declared.

If synchronization is lost when tracking, other than during start-up, the current operation is halted. If no other higher priority errors have occurred, the Carriage is retracted and the start-up is re-executed. If a higher priority error has occurred, the appropriate error recovery procedure is performed.

-RD XFER STAT (Read Transfer Status)

This signal, generated by the MDS PCA, is low during a sector in which a Read operation is occurring. It is activated or deactivated at the beginning of each sector. This signal is used in reporting status, generating a Rewrite Request, and to prevent Jumpbacks.

+LASE DYE STAT (Laser Dying Status)

This status is high when the Power Control Loop on the Read/Write Control PCA is reaching the maximum current limit, and cannot go higher. This condition indicates Laser Diode performance is degrading to the point where Read and Write operations of the LD 1200 will be affected.

+QUAD LO STAT (Quad Low Status)

This signal is generated by the Servo Systems PCA. It is high when the QUAD SUM signal goes below an acceptable level. When this occurs, the error is reported to the ICI PCA.

+P.S. TEMP WARN (Power Supply Temperature Warning)

This signal, generated by the Power Supply, is an early warning signal indicating that the ambient temperature of the Power Supply has reached 65 degrees Centigrade. The Power Supply automatically shuts down 1 second after this signal is activated.

+CAGE TEMP WARNING

This signal, generated by the Error Signal Generator PCA, is high when the Card Rack temperature has gone above an acceptable level.

+MTR SPD PLS (Motor Speed Pulse)

This signal is generated by a sensor positioned over the spindle. It is used by the Drive Control Microprocessor to determine when the Spindle is up to speed during spin-up, and when it has come to rest during spin-down.

+LINE SYNC SIG (Line Sync Signal)

This signal is generated by the Power Supply. It indicates that the input voltage to the Power Supply is equal to or greater than the minimum range value required for reliable operation of the LD 1200. This signal toggles at the frequency of the ac power input when that input is acceptable.

+WRT PROT SW (Write Protect Switch)

This signal is high when the Write Protect Switch on the Operator Panel is in the Write Protect position. It is low when the Drive is not write protected.

-STRT/STOP SW (Start/Stop Switch)

This signal is low when the START/STOP switch on the Operator Panel is in the START position. When low, with Data Cartridge installed, the Drive initiates spin-up. When high, it initiates spin-down. These functions are enabled by the Drive Control Microprocessor.

+CAR PRO TB SW (Cartridge Protect Tab Switch)

This signal indicates the position of the Write Protect Tab on the Data Cartridge. When high, the Data Cartridge is write protected, and may not be written upon.

LINE SYNC FAULT

This signal, generated by the Line Sync Monitor, goes high when two consecutive Line Sync pulses are missing. When this occurs, it indicates that a two cycle loss of ac power has occurred in the Power Supply.

+LOST FOC STAT (Lost Focus Status)

This signal, generated by the Servo Systems PCA, is monitored during initialization (nontracking) and all tracking states. It is not monitored during Seeks. When low, it indicates that the Focus Servo Loop is maintaining a Media to lens distance within tolerance. The astigmatic signal must be within an acceptable tolerance, and the QUAD SUM Signal must indicate reflected light from the Media (slightly less than the quad low status).

When +LOST FOC STAT is high, writing of the current sector is terminated. The line is then monitored over a period of time after loss of focus to determine if focus recovered. No recovery results in error recovery procedures being initiated.

+CART LD STAT (Cartridge Loaded Status)

This signal is high when a Data Cartridge is installed. It is used by the Servo/Drive Control PCA to determine if a spin-up is allowed. The cartridge must be installed prior to spin-up.

S/DC PAR ERR (Servo/Drive Control Parity Error)

This signal goes high when a parity error is detected on the SIA/IDI Data Bus. When this occurs, the Servo/Drive Control PCA immediately stops all write activity and reports the status to the ICI PCA. This status is cleared at the beginning of each new sector.

LTCHD CERT FLG (Latched Certify Flag)

This signal is high when the Certify Flag is latched into the S-R latches in the Decision Logic.

PREV LTCHD WRT ERR (Previous Latched Write Error)

This signal is high when any of the following occur during the previous sector:

PLL ERROR
DRDW ERROR
SYNC ERROR
WRITE POWER ERROR
READ POWER ERROR
OVERWRITE ERROR
QUAD HIGH STATUS
FOCUS ERROR
TRACKING ERROR
TRACK MISCOMPARE ERROR
WOBBLE ERROR
PARITY ERROR

When this signal is high, write laser power is disabled until a CLR ERRORS command is received from the ICI PCA.

-WRT XFER STAT (Write Transfer Status)

This signal, generated by the MDS PCA, is low during a sector in which a Write operation is occurring. It is activated or deactivated at the beginning of each sector. This signal is used in reporting status, generating a Rewrite Request, and to prevent Jumpbacks.

RD CURR LOW STAT (Read Current Low Status)

This signal is generated by the Read/Write Control PCA. When high, it indicates there is insufficient read current flowing through the laser diode, or that read current is too low.

WRT CURR LOW STAT (Write Current Low Status)

This signal is generated by the Read/Write Control PCA. When high, it indicates there is insufficient write current flowing through the laser diode, or the write current is too low.

DIAG FOCUS (Diagnostic Focus)

This signal, generated by the Servo Systems PCA, reflects the performance of the fine power amplifier. It is low when the Focus Servo Loop (on the Servo Systems PCA) drives the Fine Servo Motor against either of the crash stops.

D S-CURVE IN (Diagnostic S-Curve In)

This signal is generated by the Error Signal Generator PCA. It allows the Servo/Drive Control PCA to monitor the amplitude of the Focus signal from the Carriage. When high, it indicates the amplitude is below the minimum level.

D S-CURVE OUT (Diagnostic S-Curve Out)

This signal is generated by the Error Signal Generator PCA. It allows the Servo/Drive Control PCA to monitor the amplitude of the Focus Error signal at the output of the ESG PCA. When high, it indicates the amplitude is below a minimum level.

POS LED FAIL

This signal is generated by the Read/Write Control PCA. When high, it indicates that the output of the Position Sensor on the Carriage is too low.

3.7.11. 10-MHz Oscillator

The 10-MHz Oscillator provides external clock input for Drive Control Microprocessor. The 10-MHz Oscillator goes through a backplane connector, allowing it to be disconnected from the Drive Control Microprocessor for diagnostic and testing purposes.

The 10-MHz Oscillator also provides clock input to the ESG PCA.

3.7.12. Reading Header Generator

The Reading Header Generator issues an interrupt to the Drive Control Microprocessor at the beginning of a sector, causing it to update previous sector status. This indicates that the MDS PCA is transferring the Header.

The Reading Header Generator receives the following interface signals:

+LD TRK LOW

This signal, generated by the MDS PCA, is high when the Track Least-Significant Byte, read from the Header, is being transferred to the Servo/Drive Control PCA over the SIA/IDI Bus. This signal terminates the Reading Header signal.

+BOS 1 (Beginning of Sector Pulse)

This signal, generated by the MDS PCA, is active high during the first nibble of a sector. It latches the accumulated error count of the previous sector into the Servo/Drive Control PCA, and starts the Reading Header signal.

3.7.13. 8039 Microprocessor and Program Memory

The 8039 microprocessor (referred to as Drive Control Microprocessor throughout these subsections) provides the Drive control functions for the LD 1200. It generates commands for and receives Drive status from the slave Drive. It transmits data, commands, parameters, and status to and from the ICI PCA via the bidirectional SIA/IDI data bus.

The Drive Control Microprocessor has access to all registers in the Dual Port RAM. At the beginning of each sector, the Drive Control Microprocessor gathers status from the previous sector and puts it in the registers of the Dual Port RAM. It then generates a Sector interrupt via the Sector Interrupt Logic to the ICI PCA, indicating that status is ready to be read.

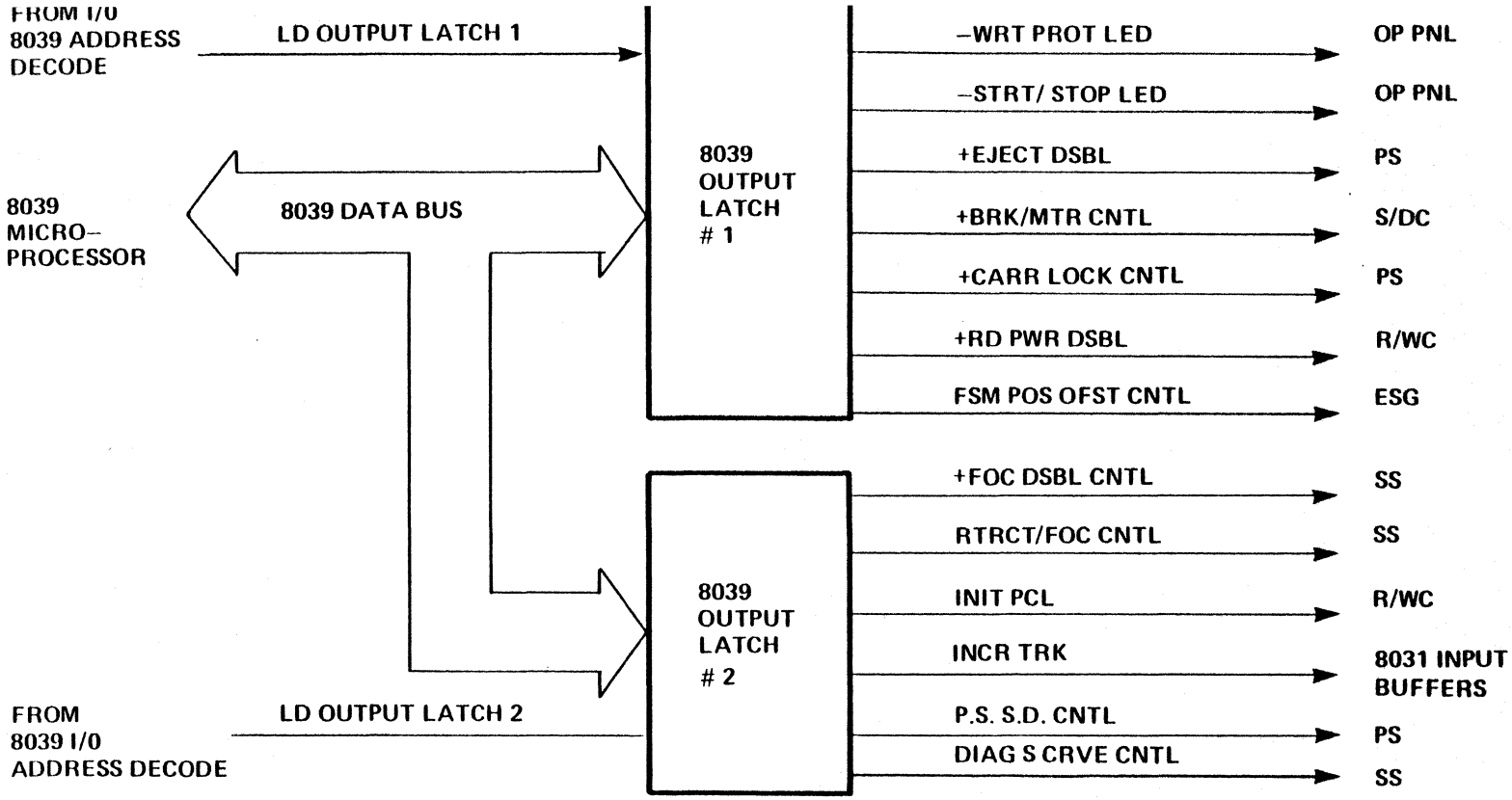
The Drive Control Microprocessor directs error recovery, controls Jumpbacks, and monitors and reports error status to the ICI PCA. It performs diagnostics as requested by the ICI PCA.

The Drive Control Microprocessor sends tracking and Seek commands to the Servo Control Microprocessor and receives servo status from it via the 8031/8039 communications bus.

The Drive Control Microprocessor has 8K of program memory.

3.7.14. 8039 Output Latches

The 8039 Output Latches provide the following control signals to Drive (refer to figure 3-35):



LEGEND:

OP PNL	= OPERATOR PANEL
PS	= POWER SUPPLY
S/DC	= SERVO DRIVE CONTROL
R/WC	= READ WRITE CONTROL PCA
ESG	= ERROR SIGNAL GENERATOR
SS	= SERVO SYSTEMS PCA

PB002201–1

Figure 3-35. 8039 Output Buffers

-WRT PROT LED (Write Protect Light-Emitting-Diode)

This signal illuminates the LED in the Write Protect Switch on the Operator Panel. When the Write Protect Switch is pressed, the Drive Control Microprocessor reports the condition to the ICI PCA. The ICI PCA, in turn, write protects the LD 1200 and this signal goes high.

This signal is also high, and the LED is illuminated, when a write protected Data Cartridge is installed, or when the LD 1200 is write protected by the host. When either of these conditions occur, there is no intervention by the ICI PCA.

-STRT/STOP LED (Start/Stop Light-Emitting-Diode)

This signal illuminates the LED in the START/STOP switch on the Operator Panel. When the Spindle Motor is idle, this signal is high (LED extinguished). When the motor is spinning up to speed or spinning down to a stop, this signal oscillates at a predetermined rate. When the Drive is ready for operation, this signal is low (LED illuminated). When the Drive is in a fault state, this signal oscillates any time the motor is spinning.

+EJECT DSBL (Eject Disable)

This signal is sent to the Power Supply. When high, it controls a solenoid that locks the Cartridge Door when an eject is not allowed. Ejects are allowed only when the Spindle is not spinning.

+BRK/MTR CNTL (Brake/Motor Control)

Controlled by the Servo/Drive Control PCA, this signal sends a message to the Power Supply to turn on or off the Spindle Motor and the brake. The motor is turned on, and this signal is low, when the START/STOP switch is pressed and the function is enabled by the ICI PCA. The motor is turned off by releasing the START/STOP switch or when commanded by the ICI PCA.

+CARR LOCK CNTL (Carriage Lock Control)

This signal, when high, locks the Carriage into Home position when the Drive is not running or is powered down.

+RD PWR DSBL (Read Power Disable)

This signal is sent to the Read/Write Control PCA. When high, it is used by the Power Control Loop to turn off read power to the Laser Diode. Read power is disabled when the Drive Spindle Motor is spun down or when a fault occurs. Read power is automatically disabled when a high Read Power Error or Quad Sum High occurs.

FSM POS OFST CNTL (FSM Position Offset Control)

This digital control signal is sent to the Error Signal Generator PCA. When low, it enables the FSM Position Offset circuitry.

+FOC DSBL CNTL (Focus Disable Control)

This signal is used during focus initialization and when the Drive is spun down. When this signal goes high, the Focus Servo Loop is opened and the focus actuator is moved to rest position.

RTRCT/FOC CNTL (Retract/Focus Control)

This signal requires an enabled Focus Servo Loop. When low, it initiates a slow Seek with the focus actuator from the retract position, until capture range and closed loop focus are obtained. When high, it drives the focus actuator to the retract position.

INIT PCL (Initialize Power Control Loop)

This signal is sent to the Read/Write Control PCA and is used to reset and initialize the Power Control Loop (PCL). During PCL initialization, the focus actuator is in the retract position, and both laser read and write power are enabled (Read Power Error Status is low and Write Power Error Status is high). Upon initialization, Write Power Error goes low, indicating that PCL Initialization is complete.

INCR TRK (Increment Track)

This signal, sent to the Servo Control Microprocessor, goes high each time a track boundary (Sector 31 to Sector 0) is crossed. The Servo Control Microprocessor uses this signal to update its internal track address.

P.S. S.D. CNTL (Power Supply Shut Down Control)

This signal is sent to the Power Supply. When Low, it shuts down Power Supply outputs when an unsafe condition (such as Cage Overtemperature) is detected in the LD 1200.

DIAG S CRVE CNTL (Diagnostic S-Curve Control)

This signal must be low for normal focus to be attained. When high, the Drive is in the diagnostic state. At this time, the focus actuator is allowed to sweep from the fully retracted position to the fully extended position without locking into the focus state. The entire Focus S-Curve can thus be observed to determine if the Carriage is functioning properly.

3.7.15. 8039 I/O Address Decode

The 8039 I/O Address Decode Logic decodes Address Bus Bits 0 through 4. This allows the Servo/Drive Control PCA to select buffers which receive status from and send control signals to the slave Drive. Refer to table 3-15 for specific decodes.

Table 3-15. 8039 Address Decode

8039 ADDRESS BUS BITS						
5	4	3	2	1	0	INDIVIDUAL REGISTERS
0	0	0	0	0	0	Read Input Buffer #1
0	0	0	0	0	1	Read Input Buffer #2
0	0	0	0	1	0	Read Input Buffer #3
0	0	0	0	1	1	Read Input Buffer #4
0	0	0	1	0	0	Watchdog Pulse
0	0	0	1	0	1	Load Output Latch #1
0	0	0	1	1	0	Load Output Latch #2
0	0	0	1	1	1	Load Output Latch #3
0	0	1	0	0	0	Load Decision Logic Register
0	0	1	0	0	1	Load Track LSB Register
0	0	1	0	1	0	Load SIA Access FF
0	0	1	0	1	1	Set Sector Interrupt
0	0	1	1	0	0	Clear S-R Latches
0	0	1	1	0	1	Clear Line Sync Monitor
0	0	1	1	1	0	Read Error Status Register #1
0	0	1	1	1	1	Read Error Status Register #2
						DUAL PORT RAM REGISTERS
1	1	0	0	0	0	Flag Register #1
1	1	0	0	0	1	Flag Register #2
1	1	0	0	1	0	Header Sector
1	1	0	0	1	1	Header Track Low
1	1	0	1	0	0	Header Track High
1	1	0	1	0	1	Status Register #1
1	1	0	1	1	0	Status Register #2
1	1	0	1	1	1	Status Register #3
1	1	1	0	0	0	Fault/Error Register #1
1	1	1	0	0	1	Fault/Error Register #2
1	1	1	0	1	0	Fault/Error Register #3
1	1	1	0	1	1	Desired Sector
1	1	1	1	0	0	Desired Track Low
1	1	1	1	0	1	Desired Track High
1	1	1	1	1	0	Actual Sector
1	1	1	1	1	1	Control Register #1

TBL10

3.7.16. Sector Interrupt

Once the Drive Microprocessor has loaded sector status into the Dual Port RAM, it sets sector interrupt. This signal is then sent to the ICI PCA via the IDI Bus, indicating that sector status is ready to be read. The ICI PCA acknowledges the interrupt, and clears it after the Dual Port Ram is read.

3.7.17. 8039 Watchdog Circuit

The 8039 watchdog circuit issues a fault when there is no Drive Control Microprocessor activity for 128 milliseconds. When this occurs, Servo Loops are opened, the laser is disabled, and the Servo Control Microprocessor is given access to the Dual Port RAM.

3.7.18. Track LSB Compare Logic

This circuitry compares the actual header address with the desired address. The Track LSB Register is loaded by the Drive Control Microprocessor with the track least-significant byte of the last Seek address (refer to figure 3-36). When the track least-significant byte is transferred during the Header of each sector via the SIA/IDI Bus, it is compared with the value stored in the Track LSB Register.

When a miscompare occurs during a Read or Write operation, a high signal is sent to the S-R latches. TRK MISCOMPARE STATUS is routed to the Decision Logic which disables the laser write power, preventing a Write from occurring.

3.7.19. Decision Logic

The Decision Logic monitors Drive status and instructions from the Drive Control Microprocessor. It determines whether to Rewrite a sector in which an error occurred, or to disable writing. Refer to figure 3-37 for a block diagram of the Decision Logic.

3.7.19.1. Decision Logic Interface Signals

The Decision Logic has the following input and output signals (refer to figure 3-37):

WRT FLG WIN (Write Flag Window)

This signal, generated by the MDS PCA, is high while the laser beam is moving through the Write Protect Flag field. The Servo/Drive Control PCA uses WRT FLG WIN to latch the current Write Power Disable status. This status is sent to the ICI PCA (as Write Not Started Status) which uses it to determine whether an error prevented writing on the Media before or after the Write operation was to start in a sector.

+WRT XFER STAT (Write Transfer Status)

This signal, generated by the MDS PCA, is low during a Write operation. It is set or cleared at the beginning of each sector. This status is used in status reporting, Rewrite Request generation, and to prevent Jumpbacks during a Write operation.

REWRITE ENABLE

This signal is received from Control Register No. 2. It goes high when a PLL error, Sync error, or DRDW error is detected during writing and an attempt to rewrite the data is authorized. The rewrite attempt is made in the next sequential sector.

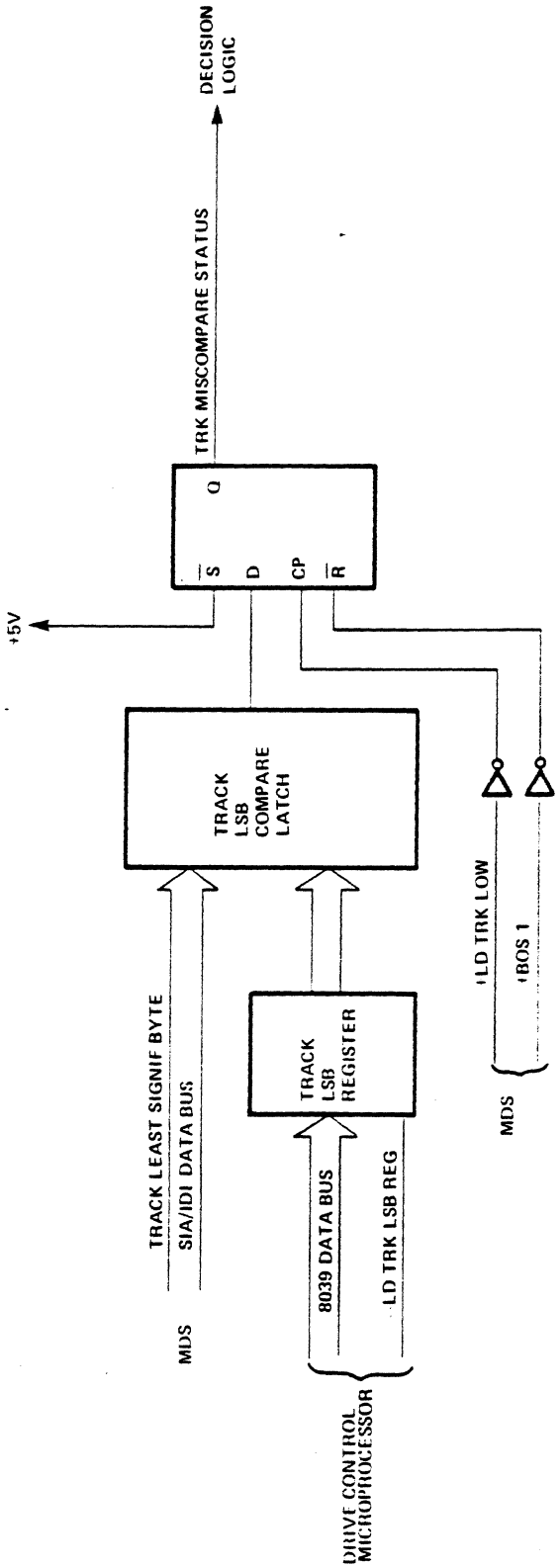
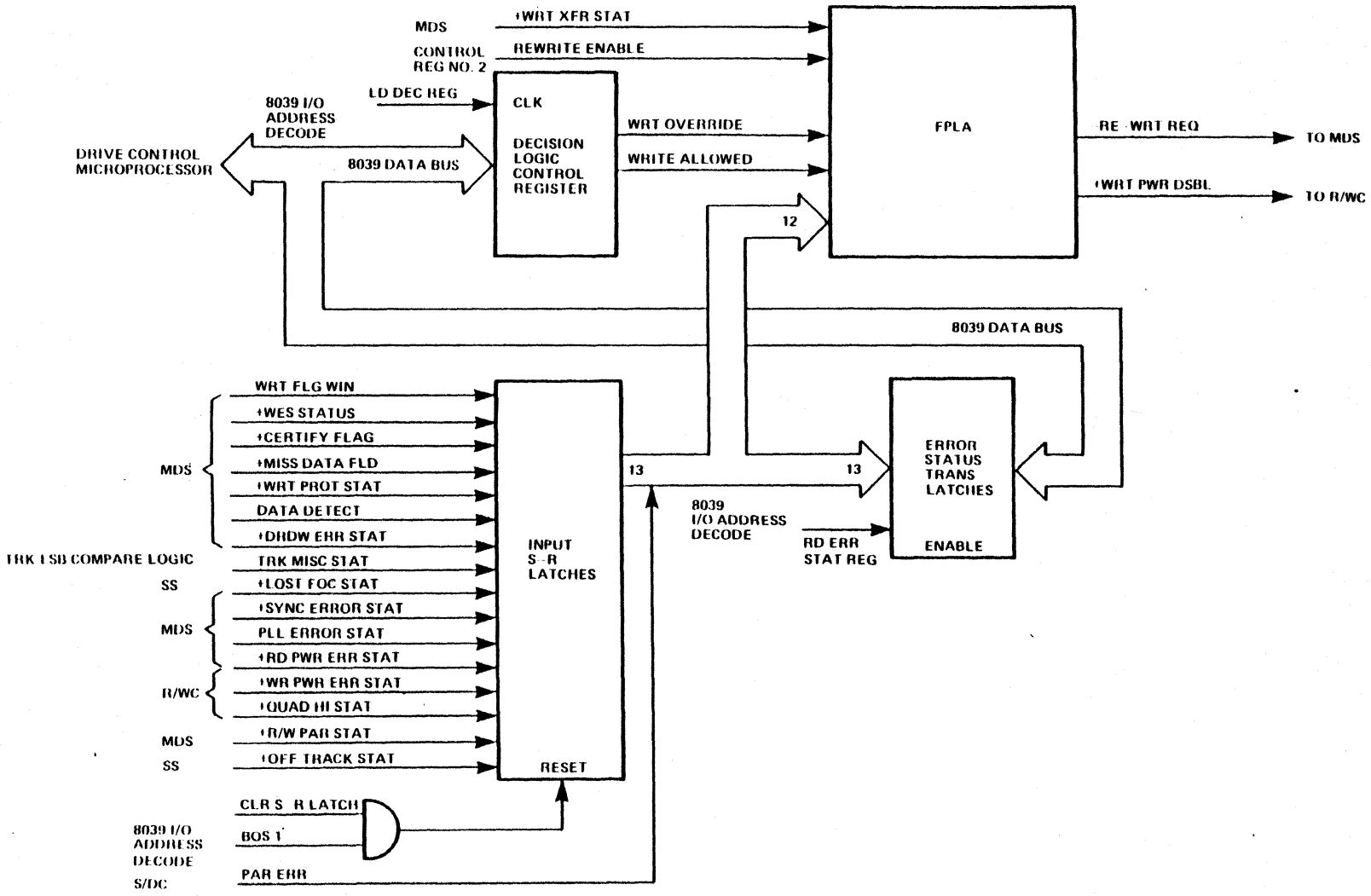


Figure 3-36. Track LSB Compare Logic



LEGEND: MDS - MODULATOR DEMODULATOR SYNCHRONIZER PCA
SS - SERVO SO SYSTEMS PA PCA
R/WC - READ/WRITE CONTROL PCA

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REV A

Figure 3-37 Decision Logic

+WES STATUS (Wobble Error Signal Status)

This signal is generated by the MDS PCA. It goes high when the MDS PCA has difficulty in reading the wobble bytes in the Sector Header. When the Servo/Drive Control PCA receives a high WES STATUS, all write activity is immediately stopped, and the error is reported to the ICI PCA. Error recovery procedures are then performed.

+CERTIFY FLAG

This signal, generated by the MDS PCA, is high when a Certify Flag byte is detected in the sector Header. The Servo/Drive Control PCA reports this status to the ICI PCA during the sector in which the flag is detected. When this signal is high, the Decision Logic inhibits writing in the next sector.

+MISS DATA FLD (Missing Data Field)

This signal is generated by the MDS PCA. When high, it indicates an attempt was made to write in the Postfield of a sector in which the data field has not previously been written. The Servo/Drive Control PCA inhibits writing and reports the condition to the ICI PCA. The error must be cleared by the SCSI Controller PCA before writing can again be attempted.

+WRT PROT STAT (Write Protect Status)

This signal is generated by the MDS PCA. It goes high when a Write has been attempted in a field which has previously been written. Upon receipt of this status, laser power is disabled and the error is reported to the ICI PCA. The write laser power is disabled until the error is cleared by the ICI PCA.

DATA DETECT

This signal is generated by the MDS PCA. It is high when data is detected in a sector during a Write operation, and is low when no data is detected. The status of this signal is reported to the ICI PCA at the end of each sector.

When an Overwrite status occurs, this signal is used to determine whether the sector has been previously written or if there is a defect in the Write Protect Byte area.

+DRDW ERR STAT (Direct Read During Write Error Status)

This signal is generated by the MDS PCA. It goes high when a predetermined number of write (DRDW) errors has occurred during a Write operation. Upon receipt of this status, the laser is immediately disabled, the error is reported to the ICI PCA, and a Rewrite is performed in the next sector, if enabled.

TRACK MISCOMPARE STATUS

This signal is generated by the Track LSB Compare Logic. When high, it indicates that the actual track address LSB (read from the Header of a sector in which a Read or Write was attempted) does not compare with the desired track LSB. This status is cleared on the leading edge of the Beginning of Sector Pulse (+BOS1) of each sector. When a track miscompare is detected, laser write power is disabled and the error is reported to the ICI PCA. The error must be cleared by the ICI PCA before laser write power is re-enabled.

+LOST FOC STAT (Lost Focus Status)

This signal is generated by the Servo Systems PCA. When low, the focus servo system is maintaining the Media to lens distance within tolerance.

When +LOST FOC STAT is high, writing of the current sector is terminated and the Focus Error is reported to the ICI PCA. The Servo/Drive Control PCA monitors this status line over a period of time, after loss of focus, to determine if focus recovered. No recovery results in focus error recovery procedures being initiated. The error must be cleared by the ICI PCA before writing can continue.

+SYNC ERR STAT (Sync Error Status)

This status is generated by the MDS PCA. It goes high if the Sector Mark is not decoded within a predefined window of time. It is cleared on the leading edge of the Beginning of Sector Pulse (+BOS1). Upon receipt of a sync error, laser write power is disabled, the error reported to the ICI PCA, and a Rewrite is performed, if enabled.

PLL ERROR STAT (Phase-Locked Loop Error Status)

This signal is generated by the MDS PCA. When high, it indicates that the PLL phase error has exceeded 30 degrees. When a PLL Error is detected, write current to the Laser Diode is disabled, the error is reported to the ICI PCA, and a Rewrite is performed, if enabled.

+RD PWR ER STAT (Read Power Error Status)

This signal is generated by the Read/Write Control PCA. It goes high when read power is too high or too low. When this occurs, reading is immediately disabled, tracking loops are opened, and the error is reported to the ICI PCA. Error recovery procedures for this error are then performed.

+WR PWR ERR STAT (Write Power Error Status)

This signal is generated Read/Write Control PCA. When high, it indicates the write power level, sensed at the Laser Diode, is not within required limits. When this occurs, writing is immediately disabled, tracking loops are opened, and the error is reported to the ICI PCA. Error recovery procedures for this error are then performed.

QUAD HI STAT (Quad High Status)

This signal is generated by the Read/Write Control PCA. It goes high when the laser beam is on track and the QUAD SUM signal goes above a predetermined level. On receiving this status, the Servo/Drive Control opens tracking loops, disables writing, and reports the fault to the ICI PCA. This is an unrecoverable condition. When this occurs, the Drive is defocused and the Carriage is retracted. This signal remains high until a LD 1200 Reset occurs.

MDS PAR STAT (MDS Parity Error Status)

This signal is generated by the MDS PCA. It goes high when a parity error is detected on data sent to or received from the MDS PCA over the SIA/IDI Data Bus. Upon receipt of this status, the Servo/Drive Control PCA immediately stops all write activity and reports the status to the ICI PCA. This signal is cleared at the beginning of each new sector.

+OFF TRACK STAT (Off Track Status)

This signal is generated by the Servo Systems PCA. It reflects the status of the Fine Servo Motor. It is high during failure or Seeks. OFF TRACK STATUS is used to complete Seeks and to monitor error conditions. At the end of a Seek, the Servo Control Microprocessor verifies that an on-track status has been achieved.

Once on track, +OFF TRACK STAT goes low. The Drive Control Circuitry and the Servo Control Microprocessor monitor this status. If this signal goes high, an off-track condition exists, writing is immediately disabled and the error is reported to the ICI PCA. The error must be cleared by the ICI PCA before laser write power is re-enabled.

S/DC PARITY ERR (Servo/Drive Control Parity Error)

This signal is generated by the Parity Logic on the Servo/Drive Control PCA. It is high when a parity error is detected on data sent or received by the SIA/IDI Data Bus. Upon receipt of the Servo/Drive Control PCA over this status, the Servo/Drive Control PCA immediately stops all write activity and reports the status to the ICI PCA. This signal is cleared at the beginning of each new sector.

-REWRT REQ (Rewrite Request)

This signal is sent to the Modulator Demodulator Synchronizer (MDS) PCA. It is made low to request a Rewrite operation for the next sector. This signal may go low at any time during a sector, and is cleared at the beginning of the next sector.

Rewrite Request is enabled by the ICI PCA via Control Register #2. The ICI PCA counts the number of Rewrites performed and disables Rewrites when the maximum number allowed per sector has occurred.

A Rewrite occurs when any of the following conditions occur:

PLL ERROR
DRDW ERROR
SYNC ERROR

If any other errors also occur, the Rewrite Request is cancelled.

+WRT PWR DSBL (Write Power Disable)

This signal is sent to the Read/Write Control PCA. When high, the Read/Write Control PCA disables laser write power. Write power is disabled when the Drive is write protected.

When a PLL, DRDW, or Sync Error occurs, this signal goes low, and writing is disabled until the end of the current sector. A Rewrite is attempted in the next sector, if enabled. When rewrites are not enabled, writing is disabled until a CLR ERRORS command is received from the ICI PCA.

Write power is disabled and this signal goes low when any of the following conditions occur:

WRITE POWER ERROR
READ POWER ERROR
OVERWRITE ERROR
QUAD HIGH STATUS
FOCUS ERROR
TRACKING ERROR
TRACK MISCOMPARE ERROR
WOBBLE ERROR
PARITY ERROR

When one of these errors occurs, write power remains disabled until a CLR ERRORS command is received from the ICI PCA via Control Register #1.

Write power is disabled, and this signal is high, at the end of a sector in which a fault occurs. It remains disabled until a Reset is issued.

3.7.19.2. Input S–R Latches

The S–R latches monitor current Drive status. They are cleared at the beginning of each sector. Errors that occur during the sector are accumulated by the S–R latches and sent to the FPLA where a decision is made as the errors occur.

At the end of each sector, the contents of the S–R latches are latched into the Error Status Transfer Latch. The Input S–R latches are then cleared at the beginning of the next sector and begin accumulating errors for that sector.

3.7.19.3. Error Status Transfer Latch

Drive status for the previous sector is held in the Error Status Transfer Latch until it is requested by the Drive Control Microprocessor. This occurs during a Sector Interrupt routine, and is reported to the ICI PCA along with other status for the previous sector. After previous sector status has been requested, the latches become transparent until the end of the next sector and present sector status may be read by the microprocessor.

3.7.19.4. Decision Logic Control Register

The Decision Logic Control Register provides the following inputs to the FPLA from the Drive Control Microprocessor:

(a) Write Allowed - This signal allows a Write operation to be performed.

(b) Write Override - When this signal is set, PLL, Sync, and DRDW errors are overridden and Rewrites are inhibited. This is used during testing and fault isolation only.

(c) Trap First Error - When the first error occurs, this signal freezes the status of all registers. It is used in diagnostics to identify the first error that occurs.

(d) Clear Errors - This signal clears errors.

3.7.19.5. Field Programmable Logic Array (FPLA)

The FPLA receives LD 1200 error status, and mode parameters (i.e., Write Error Override, Rewrite Enable, Write Protected, Clear Errors) from the host, via the ICI PCA.

The FPLA decodes the errors and determines whether to issue a Rewrite Request, to disable laser write current, or to disable servo loops.

3.7.20. 8031 Input Buffers

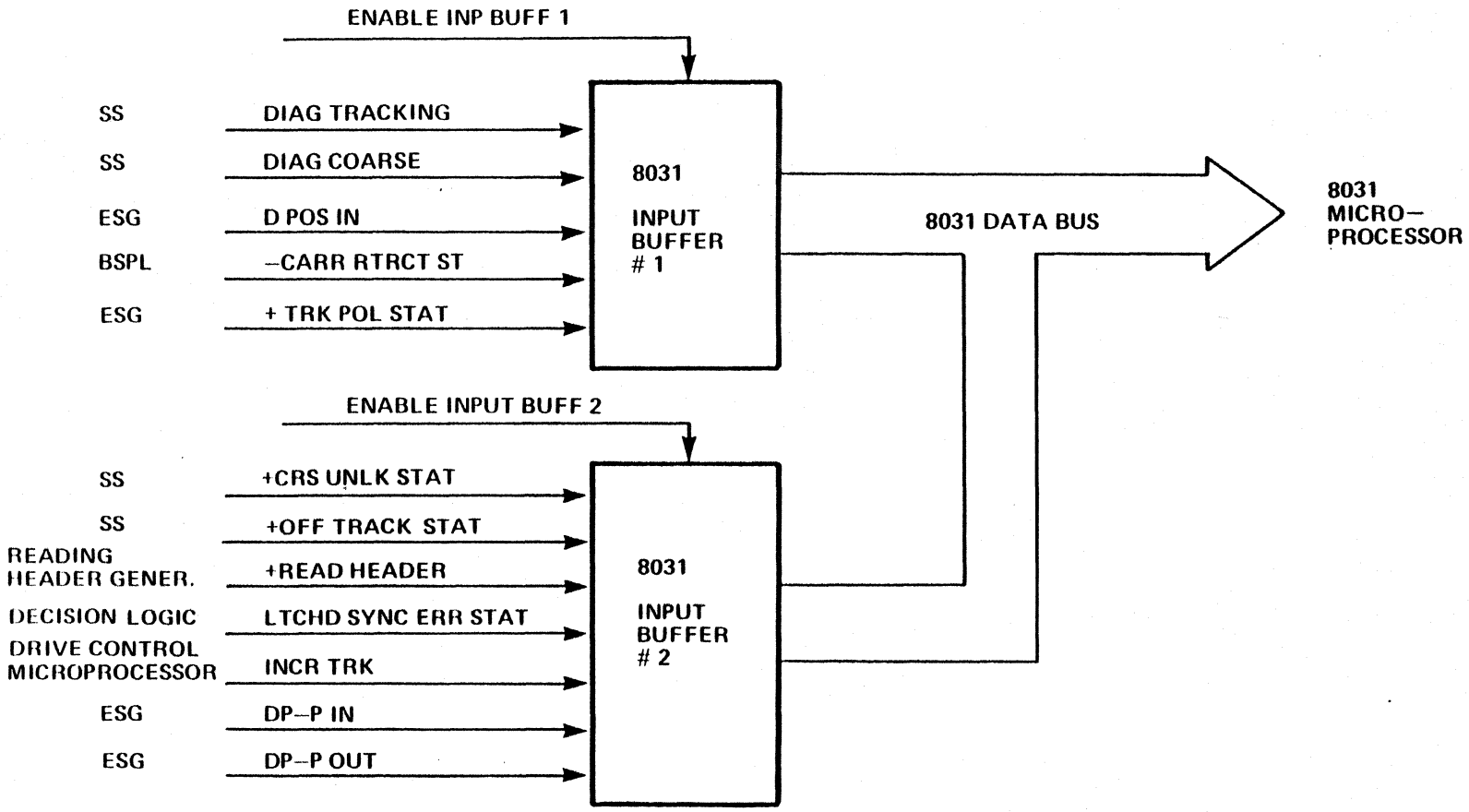
The 8031 Input Buffers receive Drive status from the Servo Systems PCA and the Error Signal Generator PCA via the following signal lines: (Refer to figure 3-38 for a block diagram.)

DIAG TRACKING (Diagnostic Tracking)

This signal, generated by the Servo Systems PCA, reflects the performance of the Tracking Power Amplifier. It is low when proper current is detected when the fine tracking actuator is forced against the inner and outer crash stops.

DIAG COARSE (Diagnostic Coarse)

This signal, generated by the Servo Systems PCA, reflects the performance of the Coarse Power Amplifier. A high indicates that the circuit is not operating properly. It is low when proper current is detected when the coarse tracking actuator is forced against the inner and outer crash stops.



LEGEND:

SS= SERVO SYSTEMS PCA
ESG= ERROR SIGNAL GENERATOR PCA
BSPL= BASEPLATE

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REV A

Figure 3-38 8031 Input Buffers

D POS IN (Diagnostic Position-In)

This signal is generated by the Error Signal Generator PCA. It allows the Servo/Drive Control PCA to monitor the amplitude of the FSM ERROR SIGNAL. When high, it indicates that the amplitude is below a minimum level.

-CARR RTRCT ST (Carriage Retract Status)

This signal, generated by a sensor on the Baseplate, goes low when the Carriage is retracted.

+TRK POL STAT (Tracking Polarity Status)

This signal, generated by the Error Signal Generator PCA, reflects the current polarity of the Tracking Error Signal (TRK ERROR). When TRK ERR is high, +TRK POL STAT is used by the Servo/Drive Control PCA to determine whether the FSM is entering or leaving a track when completing a Seek.

+CRS UNLK STAT (Coarse Unlock Status)

This status indicates that the Coarse Servo and Position Sensor are functioning properly. It is high during a failure, low when an on-track condition exists, and toggles on Seeks or Jumpbacks. This signal is used in completing Seeks and for monitoring error conditions. At the end of a Seek, the Servo Control Microprocessor verifies that an on-track condition has been achieved.

Once on-track, the Servo Control Microprocessor monitors this status for an off-track error. When detected, writing is disabled, the error is reported to the ICI PCA, and error recovery procedures are performed.

+OFF TRACK STAT (Off Track Status)

This signal, generated by the Servo Systems PCA, reflects the status of the fine actuator. It is high during failure or Seeks. Off Track Status is used to complete Seeks and to monitor error conditions. At the end of a Seek, the Servo Control Microprocessor verifies that an on-track status has been achieved.

Once on track, +OFF TRACK STAT is low. The Drive Control Circuitry and the Servo Microprocessor monitor this status. If this signal goes high, an off-track condition exists, writing is disabled and the error is reported to the ICI PCA. If the error exceeds a given time limit, error recovery procedures are also performed. Once tracking is re-established, a Reseek is performed.

LTCHD SYNC ERR STAT (Latched Sync Error Status)

This signal is high when the Sync Error Status is latched into the S-R Latches in the Decision Logic. This status is used to verify good synchronization when the Servo Control Microprocessor reads Headers.

INCR TRK (Increment Track)

This signal, generated by the Drive Control Microprocessor, goes high each time a track boundary (Sector 31 to Sector 0) is crossed. The Servo Control Microprocessor uses this signal to update its internal track address.

+READ HEADER

This signal is generated by the Reading Header Generator. It is active once per sector, during the time the Sector ID field is read from the Media. At the completion of a Seek, this signal is monitored by the Servo Control Microprocessor while it is reading the Header.

D P-P IN (Diagnostic Push-Pull In)

This signal is generated by the Error Signal Generator PCA. It allows the Servo/Drive Control PCA to monitor the amplitude of the Push-Pull signal (or Fine Tracking Error signal) from the Carriage. When high, it indicates that the amplitude is below a minimum level. When the laser beam is focused and crossing tracks on the Media, this status toggles, indicating the Push-Pull signal is exceeding a minimum amplitude.

D P-P OUT (Diagnostic Push-Pull Out)

This signal is generated by the Error Signal Generator PCA. It allows the Servo/Drive Control PCA to monitor the amplitude of the Tracking Signal as it is output from the ESG PCA. When high, it indicates that the amplitude is below a minimum level. When the laser beam is first focused, and crossing tracks on a Media, this status toggles, indicating the Tracking signal is exceeding a minimum amplitude.

3.7.21. 12-MHz Oscillator

The 12-MHz Oscillator provides external clock input for the Servo Control Microprocessor. The 12-MHz Oscillator goes through a backplane connector, allowing it to be disconnected from the Servo Control Microprocessor for diagnostic and testing purposes.

3.7.22. 8031 Microprocessor and Program Memory

The 8031 Microprocessor (referred to as the Servo Control Microprocessor throughout these subsections) controls the servo functions in the LD 1200. It also determines the seek velocity profile during Seeks, and reports any tracking errors to the Drive Control Microprocessor.

The Servo Control Microprocessor receives commands from the Drive Control Microprocessor and sends servo status to it via the 8031/8039 communication bus.

The Servo Control Microprocessor has access to all registers in the Dual Port RAM via the Multiplex and Control Logic.

The Servo Control Microprocessor has 8K of program memory.

3.7.23. 8031 Output Latches

The Output latches provide Seek velocity data to the Servo Systems PCA, and send the following servo control signals to the Drive (refer to figure 3-39):

SK VEL ERR (Seek Velocity Error)

This eight-line bus is used only during Seeks. It carries the binary velocity control signals to the Fine Tracking Servo Loop on the Servo Systems PCA. This information is used to accelerate or brake the Fine Servo Motor as necessary to reach the desired location.

+TRK DSBL (Tracking Disable)

This signal, sent to the Servo Systems PCA, is only used when the Drive is idle with no Data Cartridge installed. It is low when fine tracking is enabled. It is not used for defect control. When this signal is high, the tracking actuator is at the rest position.

+TRK/SK CNTL (Tracking/Seek Control)

This signal is sent to the Servo Systems PCA. When high, it puts the Carriage in a track following mode (maintaining itself under the center of the track) or is involved in Seek capture (moving to and acquiring a specified track).

+CRSE/DSBL CNTL (Coarse Disable Control)

This signal is sent to the Servo Systems PCA. When disabled, the Carriage can either be at Rest position under the Media, or at Home position (fully retracted). When enabled, this signal is high and the Coarse Actuator is in closed loop operation with respect to the FSM Position Sensor, or is retracted.

CRSE RTRCT CNTL

Coarse Disable must be low for a controlled retract to occur. A controlled retract is initiated by the Servo Control Microprocessor during error recovery procedures, when a fault occurs, and during Drive spin-down. During a retract, this signal is pulse-width modulated to control the amount of force that is applied to the coarse tracking actuator. The Carriage moves off the Media into a mechanically latched, fully retracted position at the inner radius of the disk..

ENGY CNTL BIT0, ENGY CNTL BIT1 (Energy Control Bits 0 and 1)

These signals, sent to the Read/Write Control PCA, are used to control write pulse width. Write pulse width is varied to compensate for the increase in the physical length of the sectors as the track spirals outward from the center of the Media. Track ranges and associated pulse widths are given in the Read/Write Control PCA subsection of this manual.

3.7.24. 8031 I/O Address Decode

The 8031 I/O Address Decode logic allows the Servo Control Microprocessor to select the output latches and input buffers. It decodes 8031 Address Bus Bits 0 through 5. It is enabled by the command 8031 READ or 8031 WRITE. Refer to table 3-16 for specific decodes.

Table 3-16. 8031 Address Decode

BITS 5-4	HEX 3-0	INDIVIDUAL REGISTERS
0	0	Error Velocity Output to DAC on Servo Systems PCA
0	1	8031 Output Latch #1
0	2	8031 Output Latch #2
0	3	8031 Status Register #1
0	4	8031 Status Register #2
0	5	8031 Status Register #3
		DUAL PORT RAM REGISTERS
3	0	Flag Register #1
3	1	Flag Register #2
3	2	Header Sector Register
3	3	Header Track Low
3	4	Header Track High
3	5	Status Register #1
3	6	Status Register #2
3	7	Status Register #3
3	8	Fault/Error Register #1
3	9	Fault/Error Register #2
3	A	Fault/Error Register #3
3	B	Desired Sector
3	C	Desired Track Low
3	D	Desired Track High
3	E	Actual Sector
3	F	Control Register #1

TBL11

3.7.25. 8031 Watchdog Circuit

The 8031 Watchdog circuit issues a fault if there is no Servo Control Microprocessor activity for 50 milliseconds. When this occurs, servo loops are opened by clearing the 8031 Output Latches, the Drive Control Microprocessor is given access to the Dual Port RAM, and a Microprocessor Unit (MPU) timeout fault is reported to the ICI PCA.

3.8. SERVO SYSTEMS PCA

The Servo Systems PCA processes error signals providing coarse and fine tracking and proper focus. It consists of three major elements:

- Focus Servo Loop - controls the vertical position of the objective lens for proper focus.
- Fine Tracking Servo Loop - controls the radial or horizontal position of the objective lens for track positioning and following.
- Coarse Tracking Servo Loop - controls Coarse Linear Actuator movement, for bulk carriage movement.

Each circuit is controlled exclusively by the two microprocessors on the Servo/Drive Control PCA. Each circuit contains a lead/lag network that prevents loop oscillations from occurring.

The microprocessors initialize, close, and control each of the servo loops through steering logic, which controls a series of analog switches. Each loop in turn determines its own status, which is reported to the microprocessors on the Servo/Drive Control PCA. Each Servo Loop on the Servo Systems PCA responds to Drive Error Signals. Power Amplifiers serve as current drivers to control the Fine Servo Motor (FSM) and Carriage in response to these error signals.

Detailed descriptions of the Servo Systems circuits are provided in the Focus Servo Loop, Fine Tracking Servo Loop, and Coarse Tracking Servo Loop subsections that follow.

3.8.1. Signal Descriptions

Signal descriptions are as follows (refer to figure 3-40):

(1) FOCUS ERR SIG (Focus Error Signal) - This signal is derived from the output of the Quad Detector (mounted in the Carriage). It indicates the relative shift of the Focus Actuator from an in-focus region. This signal also serves as the error signal to Drive the Focus Actuator into the focus region.

(2) QUAD SUM SIG (Quad Sum Signal) - This signal is derived from the output of the Quad Detector. It indicates the total signal power received at the Quad Detector. The Quad Sum signal is used for the following:

- To provide the gain control voltage to the Error Signal Generator PCA.
- To provide Quad Low Status.
- To provide Quad High Status to the Read/Write Control PCA.

(3) TRK ERR SIGNAL (Tracking Error Signal) - This signal is derived from the output of the Quad Detector that is mounted in the Carriage. It indicates the offset of the Fine Tracking Actuator from the track center. This signal also serves as the error signal to Drive the Fine Actuator to the center of the track.

(4) SK VEL ERR (Seek Velocity Error) - This signal is used only during Seeks. It carries the binary velocity control signal through a DAC, then to the Fine Tracking Servo Loop.

(5) +SEEK CONTROL - During a Seek, this signal is low and the Fine Actuator is Driven by the microprocessor Drive signal. The microprocessor is given control during Seeks, Seek capture, and Jumpbacks.

(6) +TRK/SK CNTL (Tracking/Seek Control) - This signal is high during tracking and during a part of Seek capture. During a Seek, this line is disabled and the Fine Actuator is Driven by the microprocessor velocity Drive signal. This signal toggles during the required Jumpbacks, which are controlled Seeks.

(7) +TRK DSBL (Tracking Disable) - This line is only used when the Drive is idle, with no cartridge installed. It is not used for defect control. When this line is high, Fine Tracking is disabled and the Tracking Actuator is at its rest position.

(8) EM RETR VLT (Emergency Retract Voltage) - This signal is +12 Vdc supplied by a 20,000 uf emergency retract capacitor. It is a passive function which occurs when Power Supply voltage drops below an acceptable level. It initiates a semicontrolled retract into the latched position. This signal is not microprocessor controlled.

(9) +SUPP OP (Supply Operative) - This signal is used in conjunction with emergency retract. When this status goes low, indicating a power supply problem or power up, Emergency Retract Voltage initiates a retract.

(10) +CRSE/DSBL CNTL (Coarse/Disable Control) - When this signal is high, the Coarse Servo Loop is disabled and the Carriage can be either at rest position under the disk, or at the home position. When low, the Coarse Actuator is in close looped operation with respect to the FSM Position Sensor or retracted.

(11) CRSE RTRCT CTL (Coarse Retract Control) - When this line is low, a controlled retract occurs. It is initiated by the microprocessor for other than voltage faults, and when powering up or down the LD 1200. Coarse Disable must be low for a retract to occur. During a retract, the Carriage moves off the disk into a mechanically latched home position at the inner radius of the disk.

(12) FSM ERROR SIG (FSM Error Signal) - This signal is the error signal that drives the Coarse Linear Actuator. It is derived from the Position Sensor mounted on the Fine Servo Motor. The signal indicates the relative shift of the Fine Tracking Actuator from the Coarse Linear Actuator.

(13) +FOC DSBL CNTL (Focus Disable) - This signal is only used when the LD 1200 is idle with no cartridge installed. When high, the Focus Servo Loop is disabled, and the Focus Actuator sits at its rest position.

(14) RTRCT FOC CTL (Retract/Focus Control) - This signal requires an enabled Focus Servo Loop. When low, it initiates a slow Seek of the Focus Actuator from the retracted position until capture range and closed loop focus are obtained. The entire ramping function is contained on the Servo Systems PCA. Diagnostic S-curve control must be low for the Focus Servo Loop to close.

(15) DIAG S CRVE CNTL (Diagnostic S Curve) - This signal must be low for normal focus to be attained. When high, the LD 1200 is in the diagnostic state and the Focus Actuator is moved from a fully retracted position to a fully extended one, allowing the Focus S-Curve to be observed to determine functionality.

(16) DIAG FOCUS (Diagnostic Focus) - This signal reflects the performance of the Focus Power Amplifier. This signal toggles in response to controls from the Servo/Drive Control PCA, indicating the circuit is operating correctly.

(17) FOCUS DRIVE - This signal carries the Focus Actuator Drive current from the power amplifier.

(18) FOCUS RETURN - This signal is the return path for the Focus Actuator, carrying current feedback to the Focus Servo Loop.

(19) FOCUS GND - This signal ties the Focus Servo Loop ground reference to Backplane ground.

(20) +LOST FOC STAT (Lost Focus Status) - This signal is monitored during initialization (nontracking) and all tracking states. The signal is not monitored during Seeks. When low, it indicates that the Focus Servo Loop is maintaining the disk to lens distance within tolerance. The astigmatic signal must be within acceptable tolerance and the Quad Sum signal must indicate reflected light from the disk.

This signal is also used as an interrupt. When the Servo/Drive Control PCA detects Lost Focus Status is high, writing of the current sector is terminated. The Servo Drive/Control PCA monitors this status line over a period of time after loss of focus to determine if focus has been recovered. No recovery results in error recovery procedures being initiated.

(21) +QUAD LO STAT (Quad Low Status) - When the Quad Sum signal drops below a minimum level, this signal goes high, and the Servo Drive/Control PCA reports an error to the ICI PCA. The source of the problem may be poor Media or an obstructed optical path.

(22) +OFF TRK STAT (Off Track Status) - This status signal indicates the status of the Fine Actuator. It is high during failure or Seek, and low when an on-track condition exists. This signal is monitored only during the on-track state. The Coarse Linear Actuator is not monitored, because if it goes off track, the Fine Actuator is pulled off track also. This line toggles on Seeks and Jumpbacks, and is hardwired to enable a Write operation.

Off Track Status is used in completing Seeks and in monitoring error conditions. At the end of a Seek, this signal is used by the Servo Microprocessor to verify that an on-track condition exists.

When a Seek is completed, the Servo Microprocessor monitors this status for an off-track error. If an error is detected, writing is immediately disabled, the error is reported to the ICI PCA, and a Rewrite request is generated.

At the same time, the Servo Microprocessor is measuring the length of time the off-track status has existed. When the time is excessive, the microprocessor opens tracking loops, causing Coarse and Fine Tracking Error Recovery to be performed. If the off-track status clears prior to a time out, a Reseek is performed to the track where the error occurred.

(23) DIAG TRACKING (Diagnostic Tracking) - This signal reflects the performance of the Tracking Power Amplifier. It is low when proper current is flowing.

(24) TRACK DRIVE (Tracking Drive) - This signal carries the Drive current from the power amplifier to the Fine Tracking Actuator.

(25) TRACK RETURN (Tracking Return) - This is the return path for the Fine Tracking Actuator, carrying current feedback to the Fine Tracking Servo Loop.

(26) TRACKING GND - This signal ties the Fine Tracking Servo Loop ground reference to Backplane ground.

(27) FSM POS OFFST (FSM Position Offset) - This signal is generated by the Error Signal Generator PCA. The Fine Servo Motor uses this information to compensate for mechanical displacement caused by tilt or suspension spring deterioration of the FSM.

(28) DIAG COARSE (Diagnostic Coarse) - This signal reflects the performance of the Coarse Power Amplifier. It is low when proper current is flowing.

(29) COARSE DRIVE - This signal carries the Drive current from the power amplifier to the Coarse Linear Actuator.

(30) COARSE RETURN - This is the return path for the Coarse Linear Actuator, carrying feedback to the Coarse Tracking Servo Loop.

(31) COARSE GND - This signal ties the Coarse Tracking Servo Loop ground reference to Backplane ground.

(32) +CRS UNLK STAT (Coarse Unlock Status) - This signal, when low, indicates that the Coarse Servo and Position Sensor are functioning properly. It is checked during the Coarse Tracking mode, prior to a Seek. This signal verifies that the Coarse Linear Actuator has settled prior to initiating another Seek.

3.8.2. Focus Servo Loop

The Focus Servo Loop controls the vertical position of the objective lens for proper focus. It verifies the Focus Error Signal is within the required focus threshold, and attempts to recover focus if necessary.

Focus status is derived from the Focus Error Signal as shown in figure 3-41. Two comparators determine if the Focus Error Signal is within the required focus threshold. Due to the "S" shaped curve of the Focus Error Signal, this condition could occur at any one of three places as shown in figure 3-42.

"In focus" status is generated only when the focus error is within its threshold. The actuator is retracted to its bottom crash stop on the innermost portion of the disk. This allows the focus actuator to ramp up towards the disk. When the focus threshold goes low (sensing the Focus-S-Curve) then goes high, the focus capture region is obtained and an in-focus condition exists. Refer to figure 3-43.

The status detection circuit has a hysteresis of 100 microseconds to prevent erroneous toggling of the focus status lines.

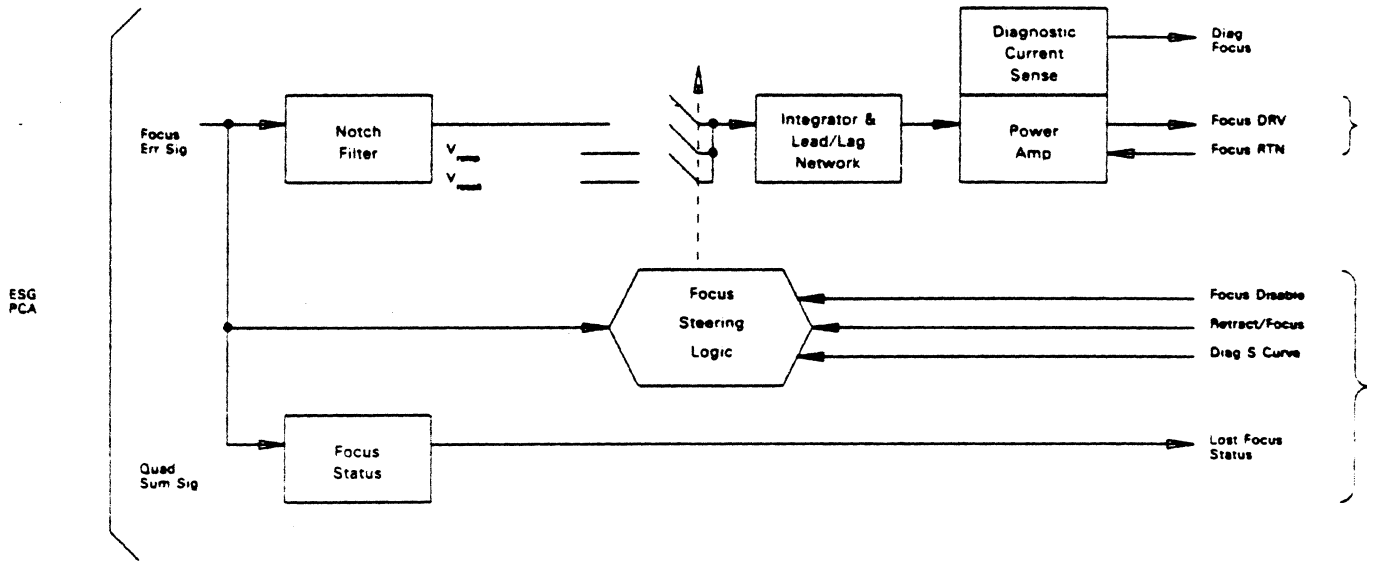


Figure 3-41. Focus Loop Block Diagram

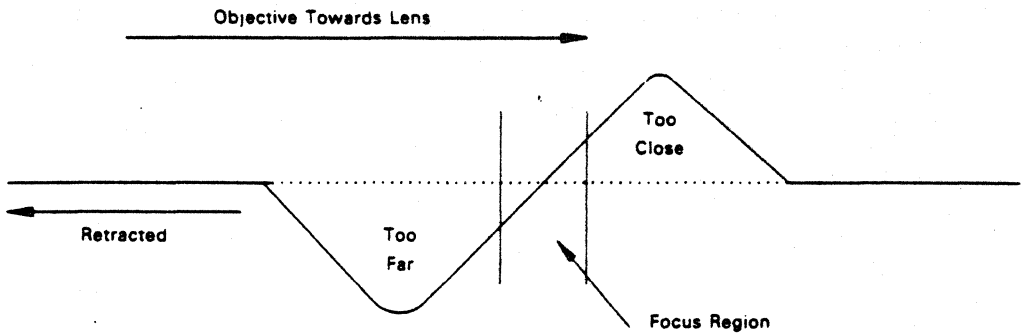


Figure 3-42. Focus "S" Curve

The Focus Servo Loop has four possible states:

(1) Disabled - This state allows the Focus Actuator to be at its rest position. It occurs when the LD 1200 is idle, with no cartridge installed, and when it is off.

(2) Actuator Retracted to Bottom Crash Stop - During LD 1200 initialization, the actuator is retracted to its bottom crash stop on the innermost portion of the disk. This allows the Focus Actuator to begin focus operation from a known condition, and to ramp up towards the disk to obtain focus.

(3) Actuator Ramping up Towards the Disk - Once recoiled, the microprocessor initiates a slow Seek until the focus capture region is obtained (refer to figure 3-43). The capture region is determined by a comparator which triggers a latch when the focus "S" curve falls within a certain threshold value.

(4) Operating Closed Loop in Focus - With the capture region obtained, the Focus Servo Loop switches from a ramping mode to a closed loop focus mode and focus is established.

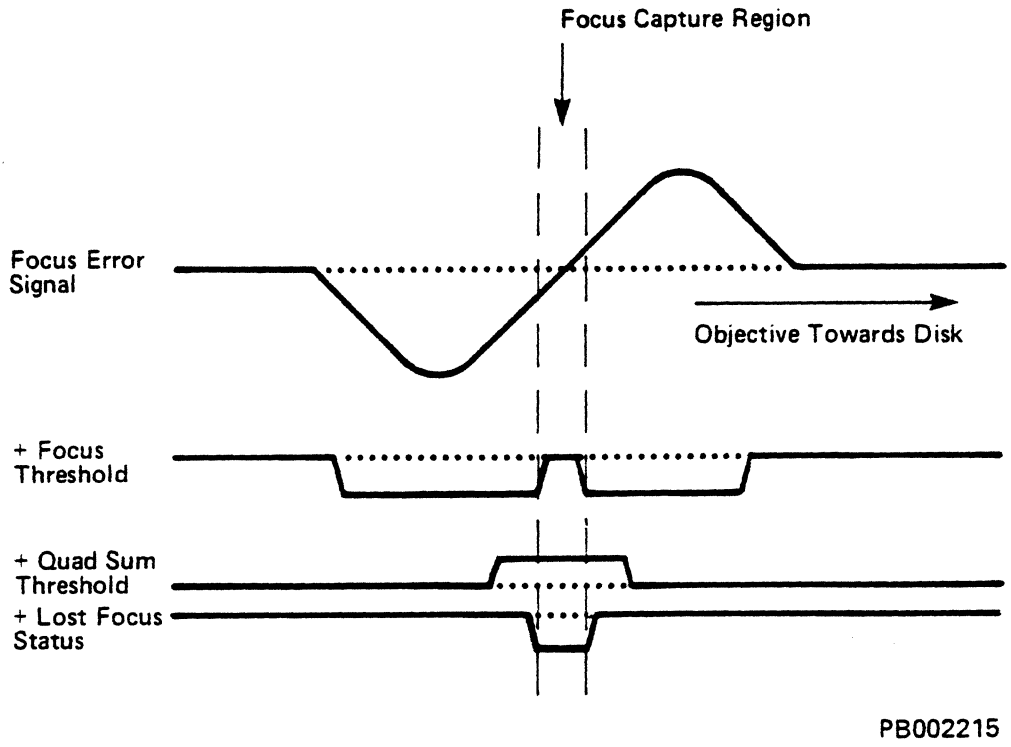


Figure 3-43. Focus Status Timing Diagram

3.8.2.1. Focus Servo Error Recovery

Focus error recovery may be attempted in the data region on the disk. Refocusing is accomplished by recoiling and ramping the Focus Actuator until the lost focus signal goes low, and focus is regained (refer to figure 3-44). Refer to figures 3-45 and 3-46 for timing diagrams of an initialization failure and a focus failure.

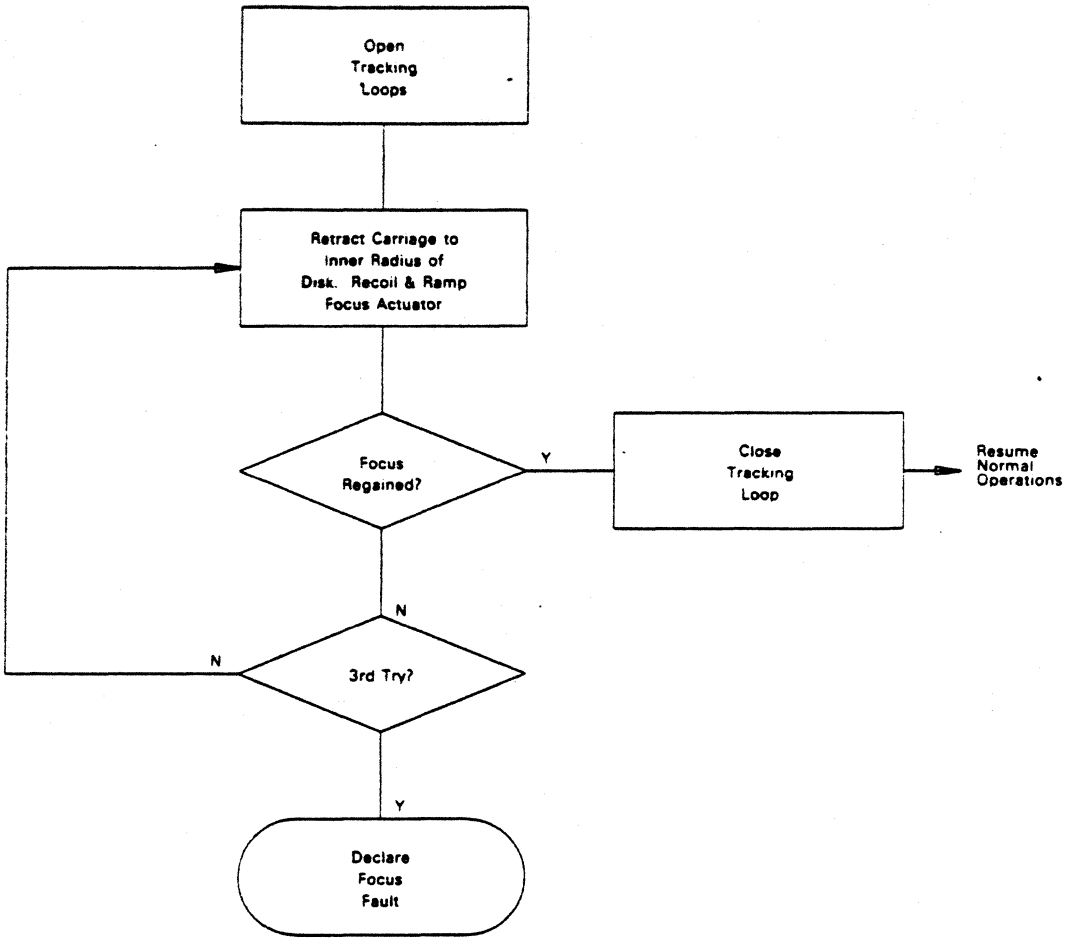


Figure 3-44. Focus Error Recovery Functional Flow Chart

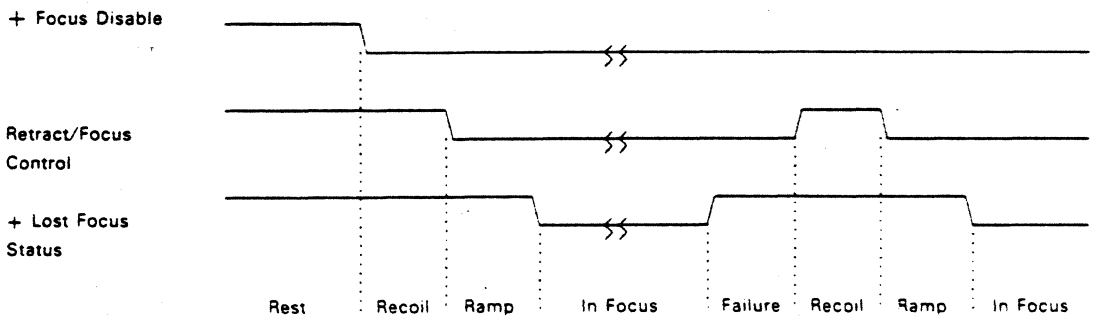


Figure 3-45 Focus Failure Timing Diagram

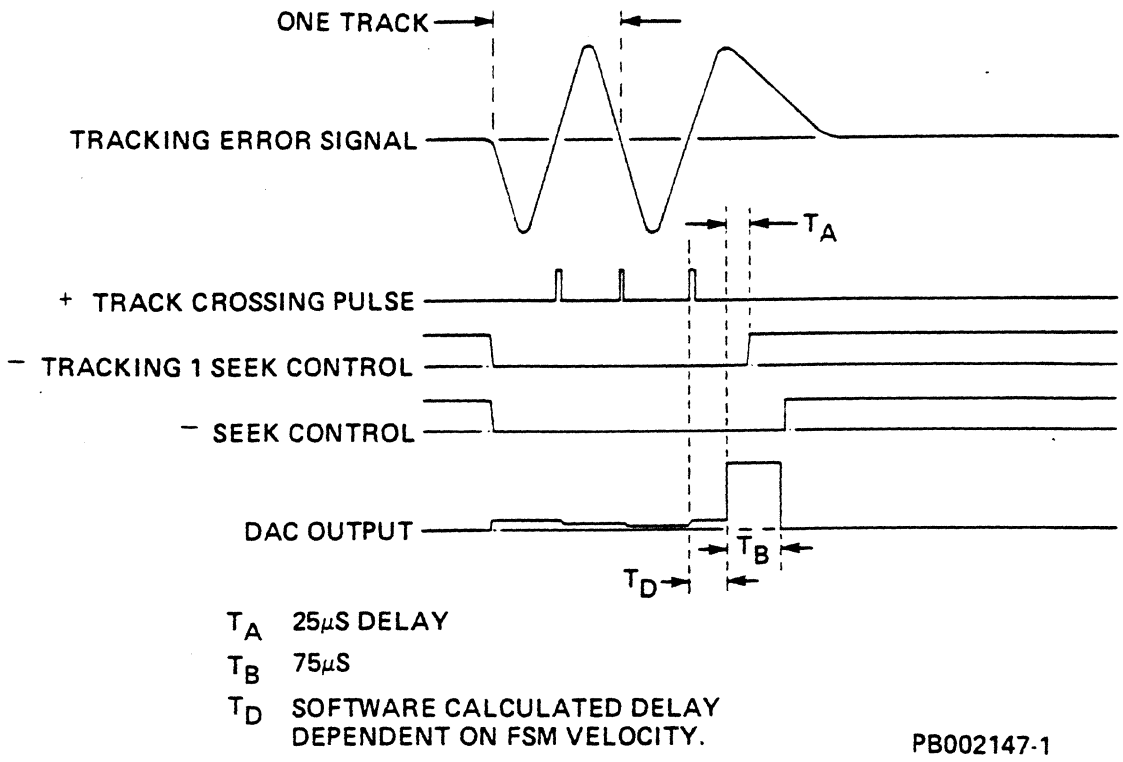


Figure 3-48. Seek Arrival Mode Timing Diagram (Two Track Seek)

(4) Closed Loop Track Following - After initialization procedures have been completed on the ESG PCA, and focus has been attained, the Fine and Coarse Tracking Servo Loops are closed and allowed to lock onto a track (refer to figure 3-49). The header information is then read off the disk to verify track location, and the appropriate actions are taken by the Servo/Drive Control PCA to continue LD 1200 operation.

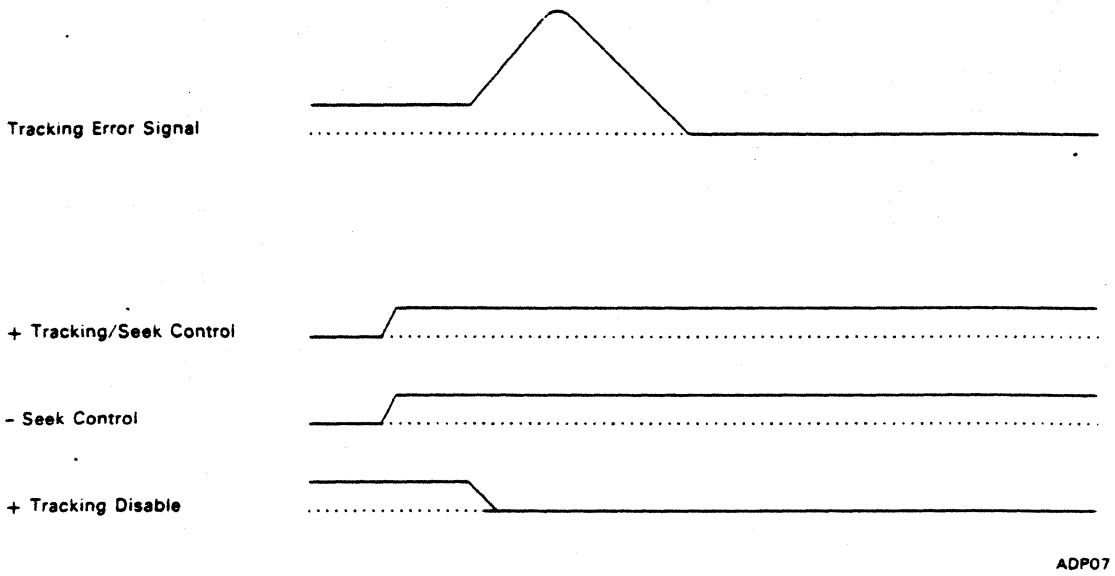


Figure 3-49. Tracking Initialization Timing Diagram

3.8.3.1. Tracking Servo Loop Error Recovery

During a tracking error recovery, the commanding Servo Microprocessor re-initializes tracking (refer to figure 3-50).

See figures 3-51 and 3-52 for initialization and tracking failure timing diagrams.

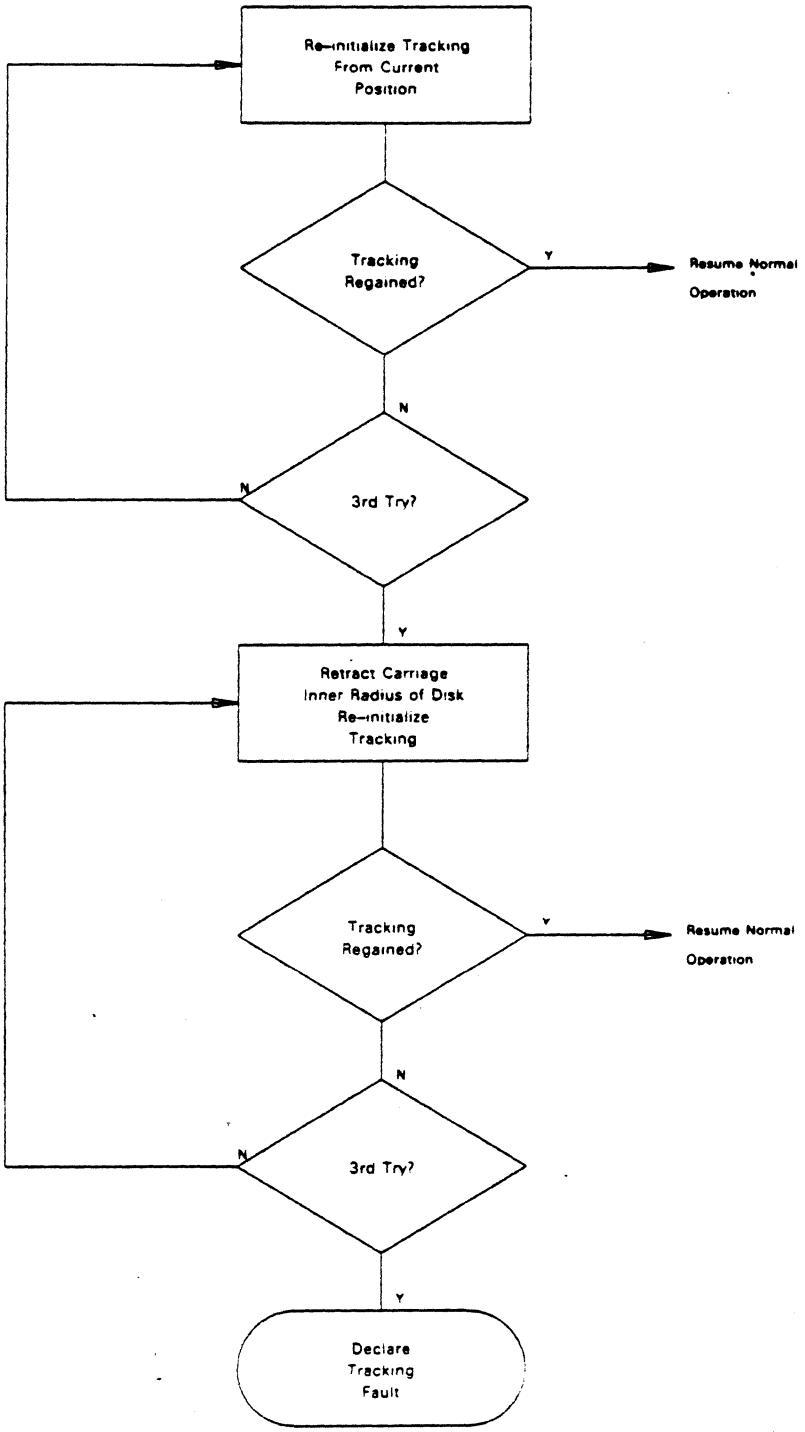


Figure 3-50. Tracking Error Recovery Functional Flow Chart

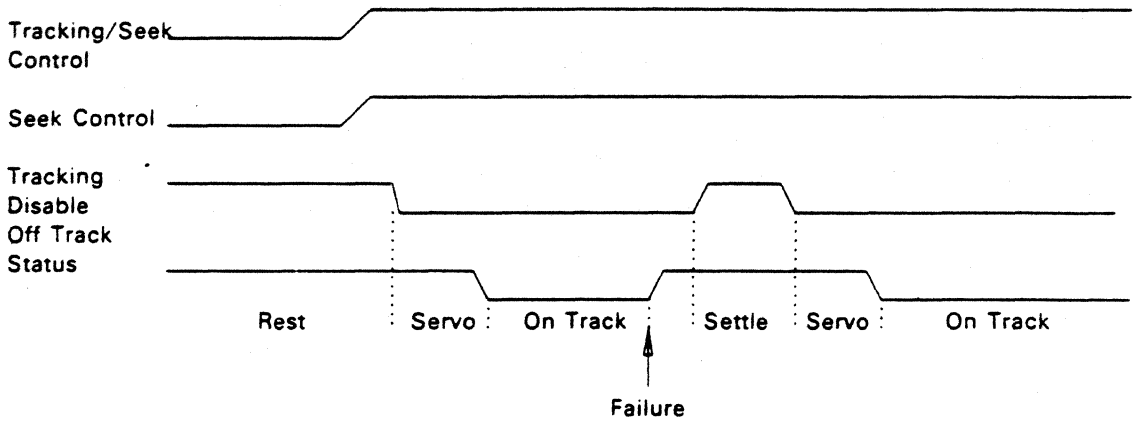


Figure 3-51. Initialization Failure Timing Diagram

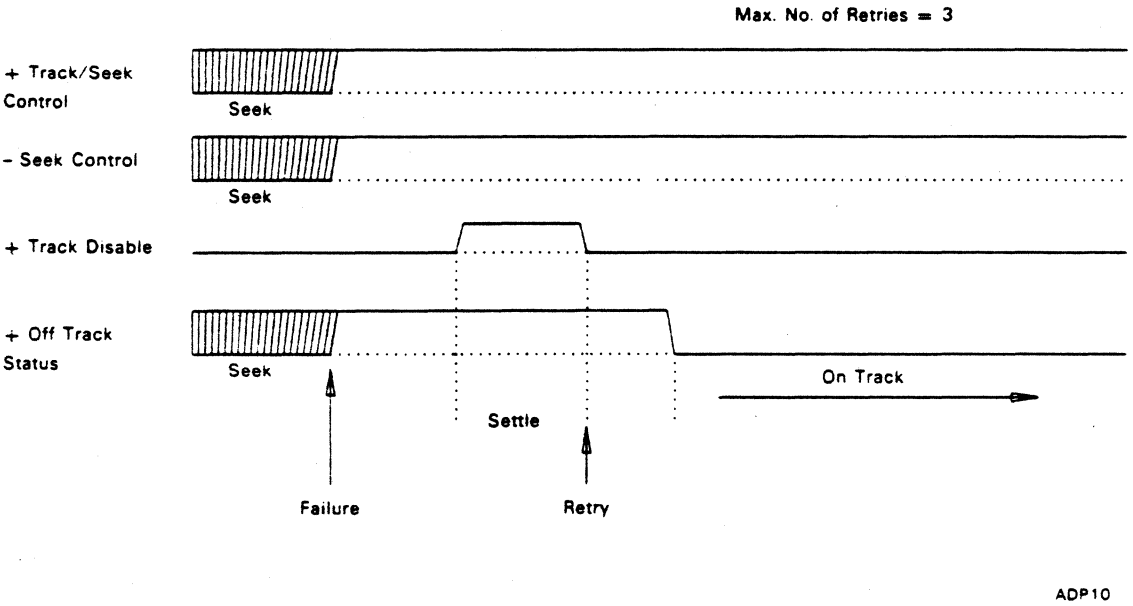


Figure 3-52. Tracking Failure Timing Diagram

3.8.4. Coarse Tracking Servo Loop

The Coarse Tracking Servo Loop controls the movement of the Coarse Linear Actuator, or bulk carriage. It drives the Coarse Linear Actuator in response to the FSM Position Signal, keeping the carriage properly aligned with the FSM.

The Coarse Tracking Servo Loop (shown in figure 3-53) has four possible modes:

(1) Disabled - This mode occurs when the Drive is idle, with no cartridge installed, and when it is off. In this mode, the coarse carriage can either be at rest position under the disk, or be latched in the retracted position.

(2) Controlled Retract - A controlled retract results in the carriage moving off the disk and into a mechanically latched "home" position at the disks inner radius. This mode is initiated by the Servo Microprocessor for faults other than voltage faults. Coarse loop mode must be enabled for a controlled retract to occur.

Controlled retract is active during Drive initialization and power down. It becomes disabled when good focus and fine tracking status have been attained. At this time it is switched from retracted mode to a closed loop servo mode, and is allowed to lock on track.

(3) Closed Loop Mode - While in closed loop mode, the Coarse Linear Actuator is Driven in response to the FSM position signal. When the FSM position signal equals zero the carriage is properly aligned with the fine servo motor. The FSM position signal senses carriage drift, then functions as the driving signal to properly reposition the carriage under the FSM.

During a seek, the microprocessor drives the FSM towards its destination. The Coarse Linear Actuator responds to the initial shift of the FSM, and follows. When the seek is complete, the Coarse Actuator settles beneath the FSM at the proper track location. Refer to figure 3-54 for an illustration of this seek profile.

(4) Emergency Retract - This mode initiates a semi-controlled retract into the latch when a power supply fault occurs. An emergency retract is not dependent on microprocessor control, and only occurs when "Supply Operative" becomes false.

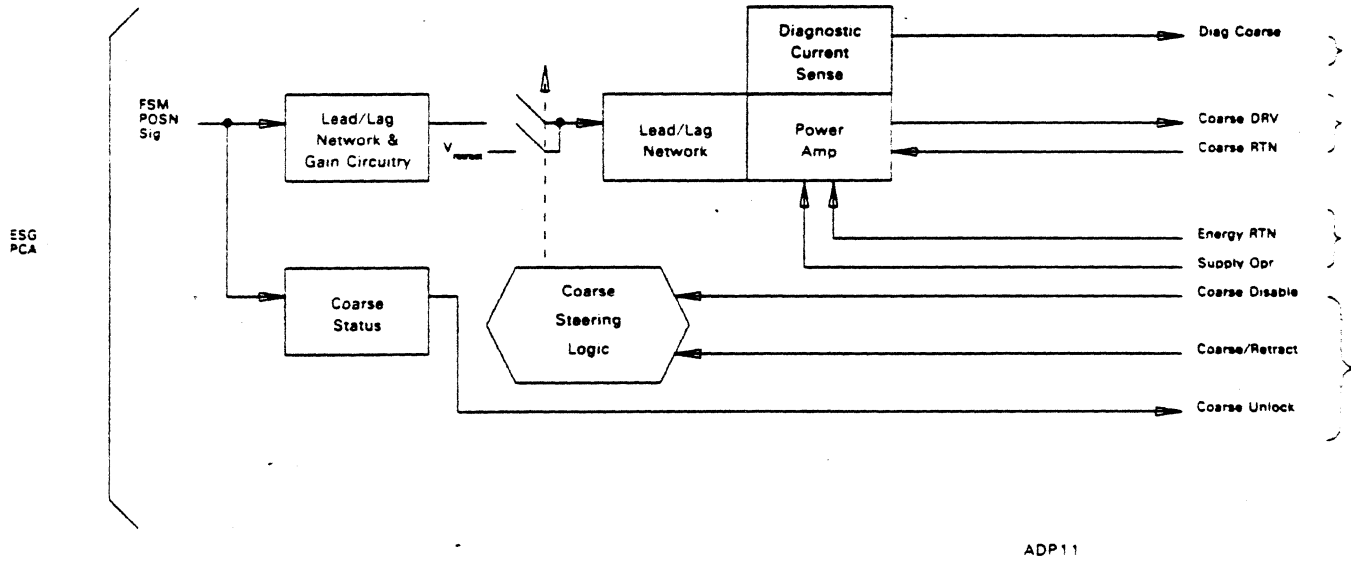


Figure 3-53. Coarse Loop Block Diagram

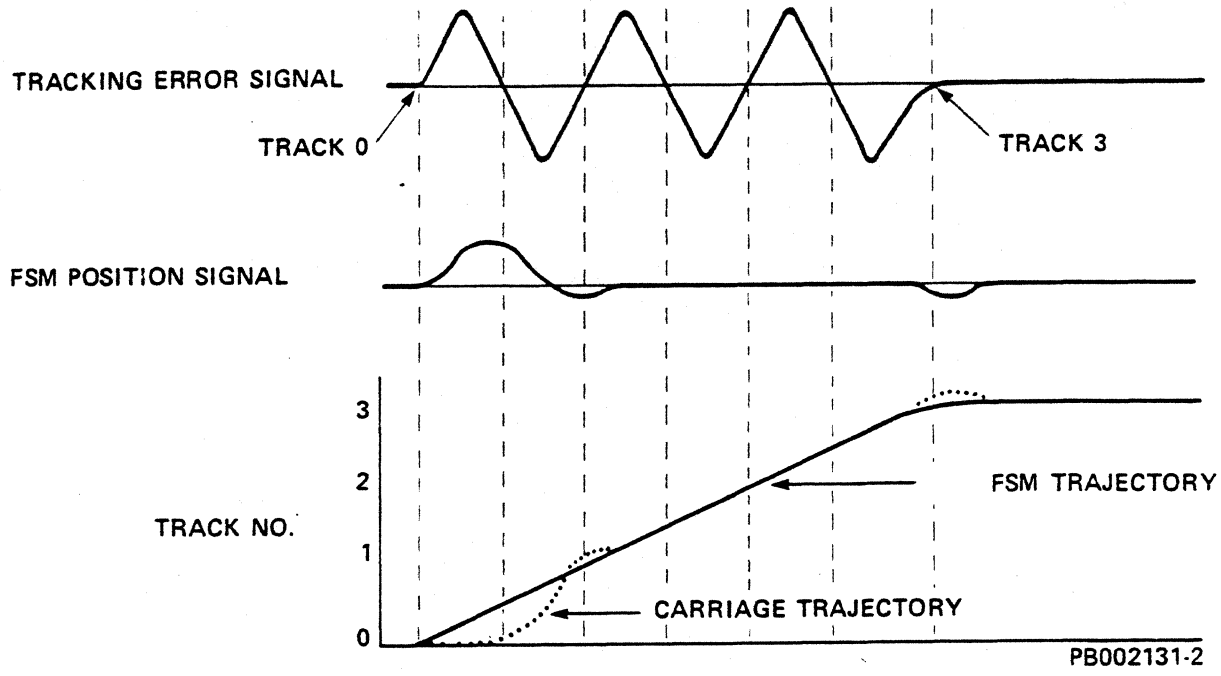
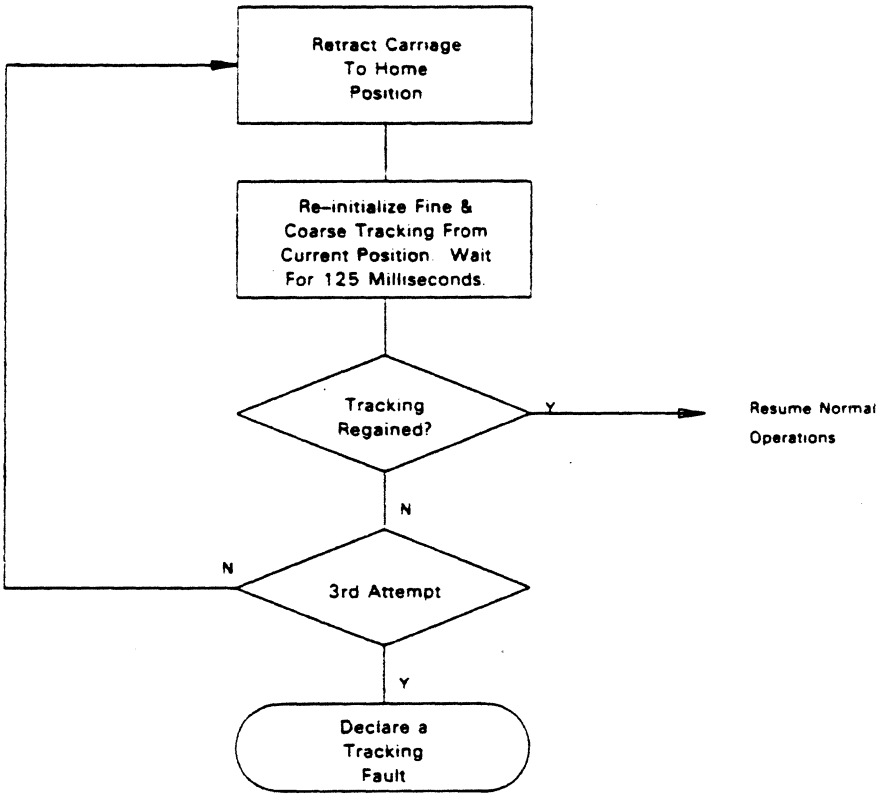


Figure 3-54. Seek Profile (Three Track Seek)

3.8.4.1. Coarse Tracking Loop Error Recovery

During coarse error recovery, the Servo Processor re-initializes coarse tracking (refer to figures 3-55 and 3-56).



ADP12

Figure 3-55. Coarse Loop Error Recovery Functional Flow Chart

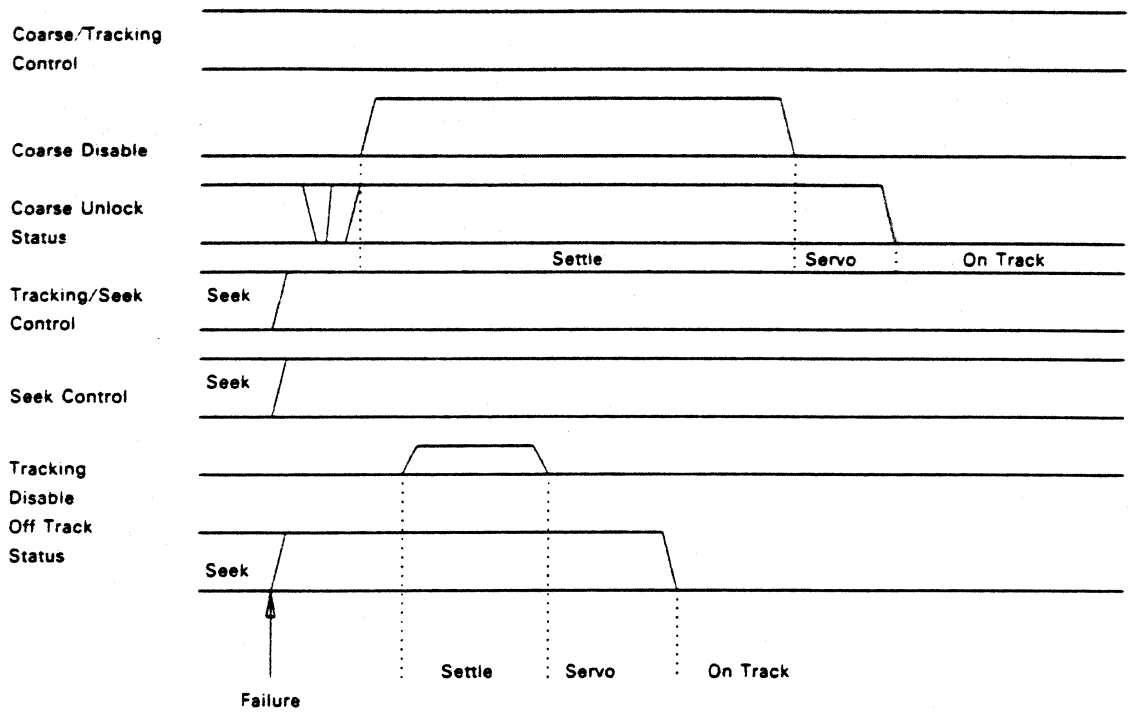


Figure 3-56. Track Following or Seek Failure Timing Diagram

3.9. ERROR SIGNAL GENERATOR PCA

The Error Signal Generator (ESG) PCA normalizes and provides offset compensation for the following servo error signals that are sent to the Servo Systems PCA:

- FOCUS ERROR signal
- TRACKING ERROR signal
- FSM ERROR signal
- FSM POSITION OFFSET signal

These error signals are used in controlling the positioning of the Fine Servo Motor and the Coarse Linear Actuator.

Detailed descriptions of the circuits on the ESG PCA, and how these error signals are generated, are provided in the subsections that follow.

(20) FSM POS ERR SIG (FSM Position Error Signal) - This signal is derived from the FSM Position Sensor on the Carriage. It indicates the relative shift of the Fine Tracking Actuator from the Coarse Linear Actuator. This signal is used to Drive the Coarse Linear Actuator.

(21) FSM POS OFFST SIG (FSM Position Offset Signal) - This signal is sent to the Fine Servo Motor to compensate for mechanical displacement caused by tilt or suspension spring deterioration in the FSM.

(22) +CAGE TEMP WARNING - This signal is high when the Card Cage temperature has gone above an acceptable level.

(23) -P.S. S.D. CNTL (-POWER SHUTDOWN CNTL) - This signal is low when an overtemperature condition exists in the LD 1200.

3.9.2. Focus and Tracking AGCs

The Focus and Tracking AGCs use a dual FET in a single package as a voltage controlled resistor. The AGCs normalize the amplitude of the Focus and Push-Pull signals received from the Carriage. Refer to figure 3-58.

3.9.2.1. Focus AGC

The Focus AGC normalizes the amplitude of the FOCUS signal coming from the carriage. The FOCUS signal changes at the same ratio as the QUAD SUM signal. The QUAD SUM signal is therefore used to control the Focus AGC, giving the FOCUS ERROR signal a constant signal amplitude.

3.9.2.2. AGC Reference

The QUAD SUM signal is used as a reference. As it decreases in amplitude, the FOCUS signal and the PUSH PULL signal decrease at the same ratio. The QUAD SUM is therefore used as a control voltage for the Focus and Tracking AGCs.

3.9.2.3. Tracking AGC

The Tracking AGC is used to normalize the amplitude of the PUSH-PULL signal coming from the Carriage. The PUSH-PULL signal changes at the same ratio as the QUAD SUM signal. The QUAD SUM signal is therefore used to control the Tracking AGC, giving the PUSH-PULL signal a constant signal amplitude.

3.9.2.4. High-Pass Filter

The normalized push-pull signal is ac coupled, via a high pass filter, to eliminate possible offsets. This ensures stability over the entire bandwidth, required by the Tracking Servo Loop, to prevent destructive Carriage oscillations.

3.9.3. Tracking Wobble Circuitry

Under certain conditions, the Wobble Error Signal can become unreliable causing the Servo/Drive Control PCA to disable the Wobble Circuitry via the WOBBLE ENABLE signal (Refer to figure 3-59).

3.9.3.1. Wobble Sample and Hold

When the Wobble Circuitry is enabled, a Wobble Qualifier Pulse clears counters D3 when the wobble bytes are detected at the beginning of a sector. This makes CT1 low, closing the switch to a Storage Capacitor where a sample of the WOBBLE ERROR signal is held.

After 32 clocks of 338 kHz (95 microseconds), output CT1 goes high, opening the switch and disconnecting the Wobble Error signal from the Storage Capacitor.

3.9.3.2. Low-Pass Filter

The combination of the resistor in series with the analog switch, the on/off time of the switch, and the storage capacitor, act as a low pass filter to eliminate any offset.

3.9.4. Summing Amplifier and Low Pass Filter

The summing amplifier adds the ac-coupled, normalized PUSH-PULL signal and the dc-coupled WOBBLE ERROR signal together (refer to figure 3-58). The resultant full bandwidth TRACKING ERROR signal (≥ 200 Khz) travels through a low-pass tracking filter to eliminate write noise. The signal is then sent to the Servo Systems PCA, where it is used for counting tracks during a Seek, and to the Track Crossing Circuitry.

3.9.8. Diagnostics

The Servo Drive Control PCA uses five diagnostic status lines on the ESG PCA to detect the following failing Field Replaceable Units (FRUs): Carriage, Error Signal Generator PCA, and Servo Systems PCA).

Five window comparators measure the amplitude of Servo Error signals on the Error Signal Generator PCA. The Servo/Drive Control PCA commands the Servo Systems PCA to Drive the FSM and the Coarse Linear Actuator in a particular direction. In the meantime, the Servo Drive Control PCA monitors the diagnostic status lines for predetermined changes. If those changes do not occur, the FRU is determined by the Servo/Drive Control PCA.

3.9.8.1. D S-Curve In

A detection circuit monitors the amplitude of the Focus Signal as it comes from the carriage. The resultant D S-CURVE IN signal is used by the Servo/Drive control PCA for diagnosing a problem and determining the FRU.

During focus initialization ramp-up, the S-Curve Control line on the Servo Systems' PCA is high, putting the LD 1200 in a diagnostic state. The Focus Actuator is allowed to sweep from a fully retracted position to a fully extended position, allowing the Focus S-Curve to be observed on the Focus Signal. If the amplitude of this S-Curve does not exceed a certain minimum amplitude, focus cannot be achieved.

During focus initialization ramp-up, the D S-CURVE IN goes through the sequence 1-0-1-0-1 (refer to figure 3-61). If the amplitude is too low, the status remains high.

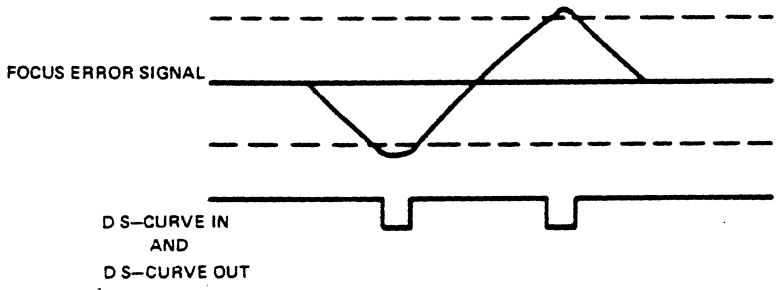


Figure 3-61. Diagnostic S Curve

3.9.8.2. D S-Curve Out

A detection circuit monitors the amplitude of the Focus Error Signal. The resultant D S-CURVE OUT signal is used by the Servo/Drive Control for diagnosing a problem and determining a FRU.

During focus initialization ramp-up, the D S-CURVE OUT goes through the sequence 1-0-1-0-1 (refer to figure 3-61). If the amplitude is too low, the status remains high.

3.9.8.3. D P-P In

A detection circuit monitors the amplitude of the PUSH-PULL signal as it comes from the Carriage. The resultant D P-P IN signal is used by the Servo/Drive control PCA for diagnosing a problem and determining a FRU.

When the laser beam is focused and crossing tracks on a disk, this status should be toggling, indicating that the PUSH-PULL signal is exceeding a minimum amplitude level (refer to figure 3-62).

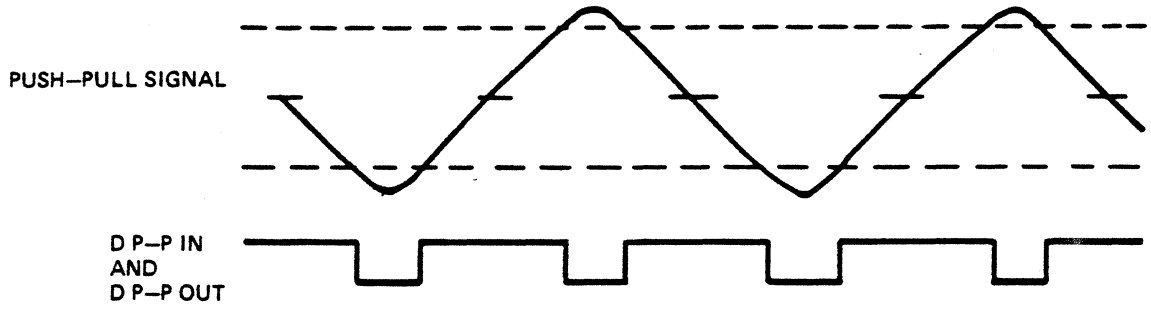


Figure 3-62. Diagnostic Push-Pull Curve

3.9.8.4. D P-P Out

A detection circuit monitors the amplitude of the TRACKING ERROR SIGNAL. The resultant D P-P OUT signal is used by the Servo/Drive Control PCA for diagnosing a problem and determining a FRU.

When the laser beam is focused and crossing tracks on a disk, this status should be toggling, indicating that the TRACKING ERROR signal is exceeding a minimum amplitude level (refer to figure 3-62).

3.9.8.5. D POS IN

A detection circuit monitors the amplitude of the POST DIFF (Position Difference) signal as it comes from the carriage. The resultant D POS IN signal is used by the Servo/Drive Control PCA for diagnosing a problem and determining a FRU.

With the laser out of focus, the Focus, Fine, and Coarse Servo Loops are disabled. The FSM Position Offset is compensated and this status is high. The Fine Tracking Servo Loop is then put into Seek mode and Driven forward and backwards in response to a maximum Seek Velocity Error. D POS IN goes low when the FSM is extended in the forward and backwards direction.

3.10. READ/WRITE CONTROL PCA

The main functions of the Read/Write Control (R/WC) PCA are:

- Control of Laser Diode read and write power
- Control of write pulse width and delay
- Control and distribution of read signals from the Carriage
- Phase-locked loop timing for Read and Write operations
- Wobble detection
- Generation of Read/Write Control status to the Servo/Drive Control PCA

Functionally, the Read/Write Control PCA can be divided into the following major sections (refer to figure 3-63):

- Read Power Control Loop, which includes the following circuits:
  - Laser Power Check Circuit
  - Initialization Circuit
  - Initialization Switch
  - Read Power Control Disable
  - Read Power Control Circuit
  - Read Power Switch
  - Read Power Current Source
  - Read Current Detection
  - Dying Status Circuit
  - Quad Sum Too High Detection
- Write Power Control Loop, which includes the following circuits:
  - Laser Power Check Circuit
  - Initialization Circuit
  - Initialization Switch
  - Write Power Control Disable
  - Write Power Control Circuit
  - Write Power Switch

- Write Power Current Source
- Write Current Detection
- Dying Status Circuit
- Quad Sum Too High Detection

- Write Pulse Logic and Delay Setting
- Write Pulse Width Setting and Direct Read During Write (DRDW) Offset, which include the following circuits:
  - Write Pulse Width Setting
  - DRDW Delay Setting
  - Write Pulse Counter
- Read Automatic Gain Control (AGC) circuit
- Phase-Locked Loop (PLL), which includes the following circuits:
  - Phase-Locked Loop
  - VCO Frequency Delay Setting
- Wobble Detection
- Carriage Power Supply Interconnect

The functions comprising the Read/Write Control PCA are described in the following subsections.

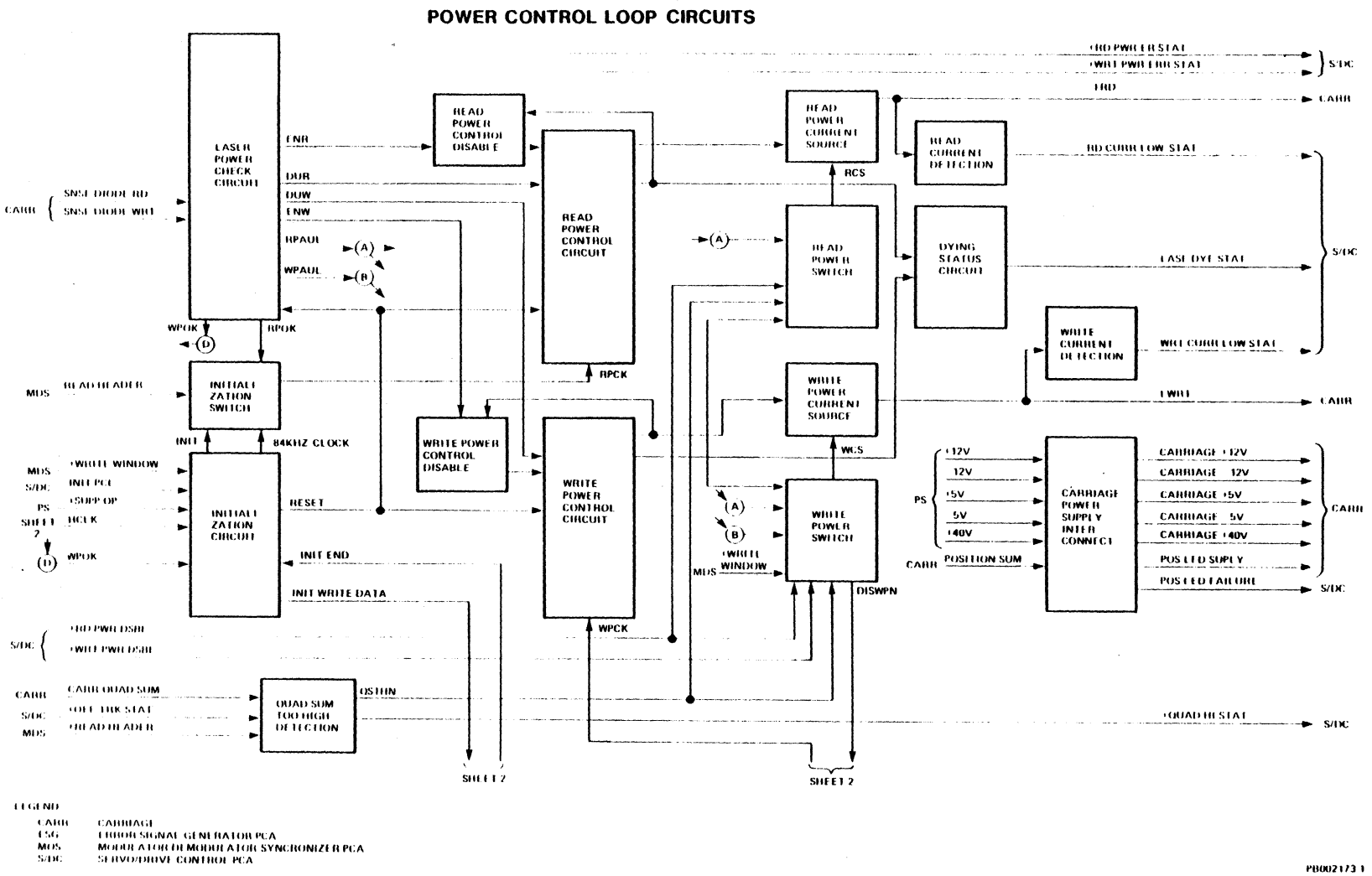


Figure 3-63 Read/Write Control PCA Block Diagram
(Sheet 1 of 2)

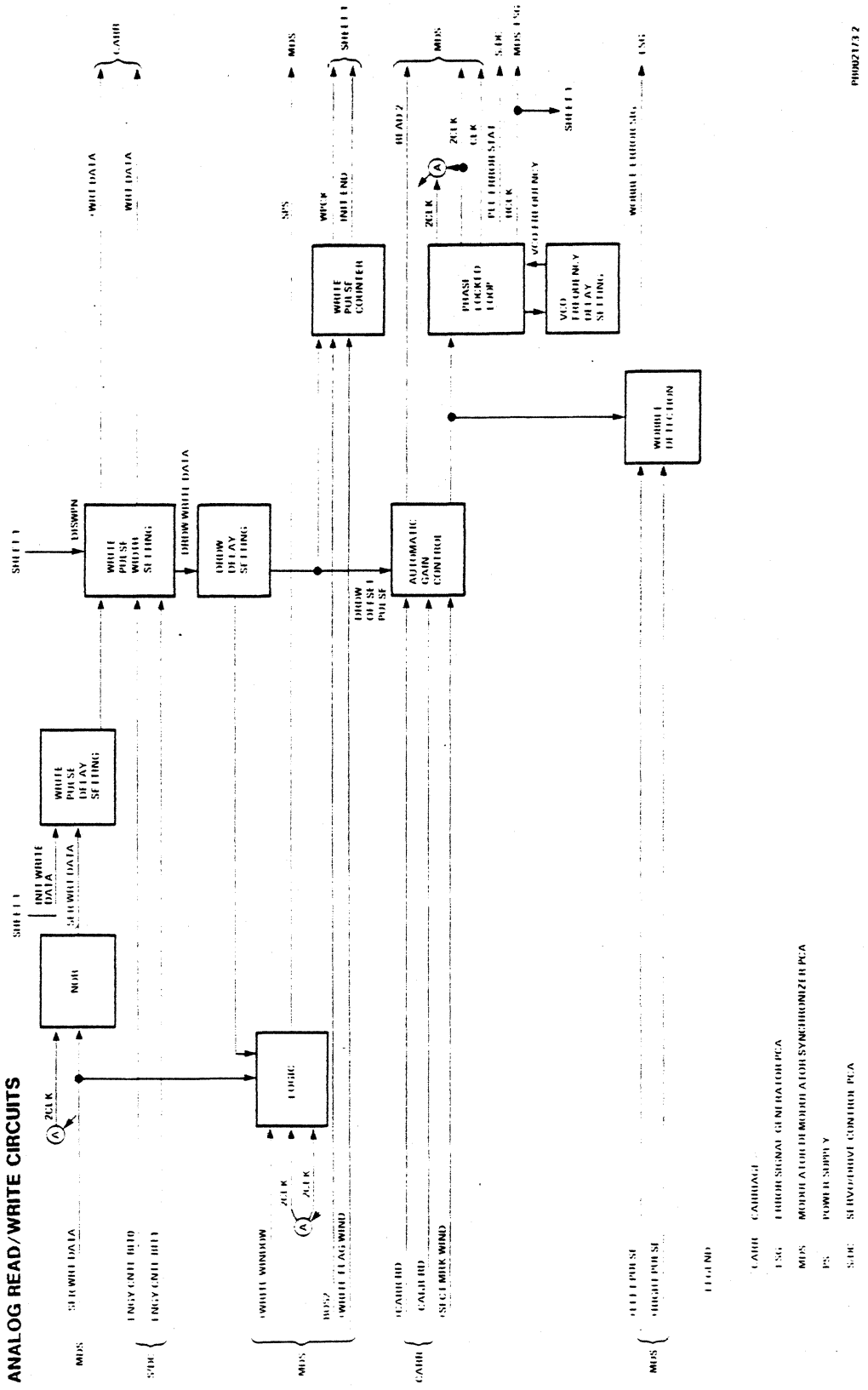


Figure 3-63 Read/Write Control PCA Block Diagram (Sheet 2 of 2)

3.10.1. Interface Signals

The Read/Write Control PCA interfaces with the remainder of the LD 1200 using the following signals (refer to figure 3-63):

SNSE DIODE RD (Sense Diode Read)

This signal is generated by the Carriage. It is a voltage which represents Laser Diode output power during the read mode.

SNSE DIODE WRT (Sense Diode Write)

This signal is generated by the Carriage. It is a sampled and held voltage which represents Laser Diode output power during the write mode.

BOS 2 (Beginning of Sector Pulse)

This signal is generated by the Modulator Demodulator Synchronizer PCA. It is active high during the first nibble in a sector, indicating the beginning of the sector. BOS 2 is used to reset the Write Pulse Counter which generates WPCK (Write Power Clock).

+WRITE WINDOW

This signal is generated by the Modulator Demodulator Synchronizer PCA. It is active high during the time writing is allowed in the Data Field of a sector.

+WRT FLAG WIND (Write Flag Window)

This signal is generated by the Modulator Demodulator Synchronizer PCA. It is high while the laser beam is moving through the Write Protect Flag field. It is used by the Write Power Control Circuit to inhibit write power updates during this time.

INIT PCL (Initialize Power Control Loop)

This signal is generated by the Servo/Drive Control PCA. It is used for reset and initialization of the Power Control Loop. When initializing the Power Control Loop, the focus actuator is in the retract position and both read and write power must be enabled. (Read Power Error Status is low and Write Power Error Status is high.) On initialization, Write Power Error Status goes low. This action indicates that Power Control Loop initialization is complete.

The Power Control Loop is reset when INIT PCL goes high.

+SUPP OP (Power Supply Operative)

This signal is generated by the Power Supply. It goes high 1 to 2 milliseconds after all dc voltages output from the Power Supply are within operating range. The signal goes low within 5 microseconds after any of the dc voltages drops out of the operating range.

+RD PWR DSBL (Read Power Disable)

This signal is generated by the Servo/Drive Control PCA. When high, it is used by the Power Control Loop to turn off both the read and write current to the Laser Diode. Read power is disabled when the Carriage is out of focus, due to a fault, or when the Carriage is at rest in the retract position. Read power is automatically disabled when a high Read Power Error or Quad Sum High Status occurs.

+WRT PWR DSBL (Write Power Disable)

This signal is generated by the Servo/Drive Control PCA. When high, it is used by the Power Control Loop to turn off write current to the Laser Diode.

Write power is disabled by the Power Control Loop as a result of any of the following conditions:

- The LD 1200 is write protected
- When any of the following conditions occur during a sector:
  - PLL Error
  - DRDW Error
  - Sync Error

  When only these errors occur, writing is disabled to the end of the current sector. If a Rewrite is enabled, writing is enabled again in the next sector to allow a rewrite of the information if the error no longer exists. If a Rewrite is not enabled, writing is disabled until a Clear Errors command is received from the ICI PCA.
- When any of the following conditions occur at other than Power Control Loop initialization:
  - Write Power Error
  - Read Power Error
  - Overwrite Error
  - Any fault condition (refer to Error/Fault Handling subsection)
  - Quad Sum Too High
  - Focus Error
  - Tracking Error
  - Track Miscompare Error
  - Wobble Error
  - Parity Error

  These conditions cause write power to be disabled until the ICI issues a Clear Errors command.
- At the end of the sector in which a fault occurs, write power is disabled until a Reset is issued.

CARR QUAD SUM

This signal is generated by the Carriage. It represents the sum of the voltages output by the four quadrants of the Quad Detector and therefore the total reflected light being received from the Media.

+OFF TRK STAT (Off Track Status)

This signal is generated by the Servo/Drive Control PCA. It indicates the status of the Fine Servo Motor. Off Track Status is high during a failure, low when an on-track condition exists, and toggles during Seeks or Jumpbacks. This signal is used in completing Seeks and in monitoring error conditions. When an off-track error is detected, the error is reported to the Servo/Drive Control PCA, then write power to the Laser Diode is disabled.

+READ HEADER

This signal is generated by the Modulator Demodulator Synchronizer PCA. It is active high once per sector, during the time the sector ID Field is read from the Media.

-SER WRT DATA (Serial Write Data)

This signal is generated by the Modulator Demodulator Synchronizer PCA. It carries TOON-encoded write data for the disk.

ENGY CNTL BITO, ENGY CNTL BIT1 (Energy Control Bits 0 and 1)

These signals are generated on the Servo/Drive Control PCA. They are used to control write pulse width. Write pulse width is varied to compensate for the increase in the physical length of the sectors as the continuous track spirals outward from the center of the disk. Track ranges and associated pulse widths, resulting from a given combination of Energy Control Bits, are as follows:

BIT 0	BIT 1	TRACK RANGE	WRITE PULSE WIDTH
0	0	0 - 12287	49.5 nanoseconds
0	1	12288 - 18431	52.0 nanoseconds
1	0	18432 - 24575	54.5 nanoseconds
1	1	24576 and up	57.0 nanoseconds

+CARR RD, -CARR RD (Carriage Read Data)

These differential pair signals are generated by the Carriage. They carry read data from the Media. Read data includes header and user data, write current readback, and disk clock signals.

+SECT MRK WIND (Sector Mark Window)

This signal is generated by the Modulator Demodulator Synchronizer PCA. On initialization of the LD 1200, it is active high until two consecutive Sector Marks have been read. Afterward, the signal is active high once per sector, during the time the Sector Mark is being read from the Media and decoded.

+LEFT PULSE

This signal is generated by the Modulator Demodulator Synchronizer PCA. It is a timing signal which, when active high, enables the Wobble Detection circuit to detect the peak level of a left wobble pulse from the Media.

+RIGHT PULSE

This signal is generated by the Modulator Demodulator Synchronizer PCA. It is a timing signal which, when active high, enables the Wobble Detection circuit to detect the peak level of a right wobble pulse from the Media.

+12V

This signal is an operating voltage provided by the power supply.

-12V

This signal is an operating voltage provided by the power supply.

+5V

This signal is an operating voltage provided by the power supply.

-5V

This signal is an operating voltage provided by the power supply.

+40V

This signal is an operating voltage provided by the power supply.

POSITION SUM

This signal is generated by the Carriage. It represents the sum of the voltages output by both diodes in the duodiode Position Sensor. POSITION SUM is used to generate supply voltage for the light source LED in the Position Sensor and to detect Position Sensor failures.

+RD PWR ER STAT (Read Power Error Status)

This signal is output to the Servo/Drive Control PCA. When high, it indicates the read power level, sensed at the Laser Diode, is not within required limits. This signal is not valid during PCL initialization.

+WRT PWR ERR STAT (Write Power Error Status)

This signal is output to the Servo/Drive Control PCA. When high, it indicates the write power level, sensed at the Laser Diode, is not within required limits.

I RD (Read Current)

This signal is output to the Carriage. It provides read current to the Laser Diode.

RD CURR LOW STAT (Read Current Low Status)

This signal is output to the Servo/Drive Control PCA. When high, it indicates there is no read current flowing through the Laser Diode or that the read current is too low.

LASE DYE STAT (Laser Dying Status)

This signal is output to the Servo/Drive Control PCA. When high, it indicates the Power Control Loop is reaching the maximum current limit and cannot go higher. This condition indicates Laser Diode performance is degrading to the point where read and write operation of the LD 1200 will be affected.

WRT CURR LOW STAT (Write Current Low Status)

This signal is output to the Servo/Drive Control PCA. When high, it indicates there is no write current flowing through the Laser Diode or that the write current is too low.

I WRT (Write Current)

This signal is output to the Carriage. It provides write current to the Laser Diode.

CARRIAGE +12V

This signal is an operating voltage output to the Carriage.

CARRIAGE -12V

This signal is an operating voltage output to the Carriage.

CARRIAGE +5V

This signal is an operating voltage output to the Carriage.

CARRIAGE -5V

This signal is an operating voltage output to the Carriage.

CARRIAGE +40V

This signal is an operating voltage output to the Carriage.

POS LED SUPLY (Position LED Supply)

This signal is output to the Carriage. It supplies the analog voltage to drive the LED which is the light source for the Position Sensor.

POS LED FAILURE (Position LED Failure)

This signal is output to the Servo/Drive Control PCA. When high, it indicates the output of the Position Sensor is too low.

+QUAD HI STAT (Quad Sum Too High Status)

This signal is output to the Servo/Drive Control PCA. When high, it indicates the Quad Sum voltage, representing the total output of the Quad Detector, has exceeded the upper limit.

+WRT DATA, -WRT DATA (Write Data)

These differential ECL signals are output to the Carriage. They carry TOON-encoded write data to be recorded in the Media.

SPS (Stop Sampling)

This signal is output to the Modulator Demodulator Synchronizer PCA. It is used to reset each sample signal after a TOON position is sampled for the presence of a monohole.

READ2 (Read Data)

This signal is output to the Modulator Demodulator Synchronizer PCA. It is an analog voltage representing TOON-encoded data read from the Media.

CLK (Clock)

This signal is output to the Modulator Demodulator Synchronizer PCA. It is a timing signal that is in phase with the zero-crossings of the clock read from the Media. CK goes high at the positive-going zero-crossings and low at the negative-going crossings.

2CLK (2 X Clock)

This signal is output to the Modulator Demodulator Synchronizer PCA. It is a timing signal that is twice the frequency of the CK signal.

HCLK (Half Clock)

This signal is output to the Modulator Demodulator Synchronizer PCA. It is a timing signal that is half the frequency of the CK signal.

PLL ERROR STAT (Phase-Locked Loop Error Status)

This signal is output to the Servo/Drive Control PCA. When high, it indicates the PLL phase error has exceeded 30 degrees. When a PLL Error is detected, write current to the Laser Diode is disabled, the error is reported to the ICI PCA, and (if enabled) a Rewrite is performed.

PLL ERROR STAT is deactivated at the beginning of each sector.

WOBBLE ERROR SIG (Wobble Error Signal)

This analog signal is output to the Error Signal Generator PCA. It indicates the relative shift of the laser beam from the center of the track in the Media.

3.10.2. Initialization Circuit

The Initialization Circuit is used to make the Power Control Loop operational following the Power-On or Reset of the LD 1200 (refer to figure 3-63). At the beginning of initialization, the Carriage is out of focus and in the retract position.

To initialize the Power Control Loop, the Servo/Drive Control PCA makes INIT PCL high, then makes +RD PWR DSBL and +WRT PWR DSBL low. INIT PCL high generates a low RESET signal, which initializes the Read and Write Power Control Circuits to a known (preset) value and inhibits the Laser Power Check Circuit.

After INIT PCL goes low again, the Initialization Circuit begins updating the read power circuit (using RPCK). At this time, RPCK is derived from an 84-kHz clock through the Initialization Switch. When RPOK (Read Power OK) goes high, updating switches to the write power circuit (using INIT WR DATA). INIT WR DATA is generated using the HCLK signal. RPCK simulates read power samples to initialize the Read Power Control Loop. INIT WR DATA simulates write data, which generates WPCK (Write Power Clock) to initialize the Write Power Control Loop.

During initialization, +RD PWR ERR STATUS is held continuously low. When write power reaches the required value, WPOK (Write Power OK) goes high. INIT WR DATA continues until a timeout occurs and INIT END (Initialization End) goes active. At this time +WRT PWR ERR STATUS goes low indicating that initialization has ended. The Initialization Switch then gates READ HEADER to the Read Power Control circuit (as RPCK), at the beginning of the next sector, to initiate a read power sample/update.

3.10.3. Initialization Switch

During initialization, this circuit switches an internal 84-kHz clock to the Read Power Control Circuit. (Refer to the Initialization Circuit subsection.) After initialization, READ HEADER (from the Modulator Demodulator Synchronizer PCA) is gated to the Read Power Control Circuit. The Initialization Switch is implemented in a field-programmable logic array (FPLA).

3.10.4. Laser Power Check Circuit

The Laser Power Check Circuit compares the read and write power outputs for the Laser Diode against four reference "windows" to determine whether the outputs are within acceptable limits. The difference between output power and the references produces digital adjustment (update) signals, which are stored in latches until clocked to the Read and Write Power Control Circuits.

SENSE DIODE RD, from the Carriage, is an analog voltage which represents the output power of the Laser Diode in the read mode. SNSE DIODE WRT, also from the Carriage, is an analog voltage representing the output power of the Laser Diode during the write mode. These signals are input to two quad comparators (one each for read and write power) in the Laser Power Check circuit. Each of these comparators checks for four windows (power thresholds):

- Read or write power is above the maximum power level allowed (RPAUL or WPAUL high)
- Read or write power is above the lower high power limit, but is within 10% of the nominal power value and is still a valid level (DUR high and ENR low or DUW high and ENW low)

- Read or write power is below the higher low power level, but is within 10% of the nominal power value and is still a valid level (DUR low and ENR low or DUW low and ENW low)

- Read or write power is below the minimum power level allowed (RPALL or WPALL low)

When either SNSE DIODE RD or SNSE DIODE WRT exceeds one of the middle windows, it indicates the associated power level is slightly too high or too low, but is still within the allowable 10% of nominal. The comparators generate signals which contain information to update the Laser Diode power levels (DUR, ENR, DUW, and ENW). These signals are stored in latches for input to the Read and Write Power Control Circuits. Read power levels are updated during initialization and at the beginning of each sector. Write power levels are updated during initialization, during the writing of the Write Power Check Byte in the sector, and while data is being written on the Media.

When read or write power exceeds either of the outer windows, an error status is generated to the Servo/Drive Control PCA (+RD PWR ER STAT or +WRT PWR ERR STAT) and Laser Diode power is then shut down by the Servo/Drive Control PCA. Only when RPAUL and/or WPAUL go high, are the Laser Diode currents turned off by the hardware.

3.10.5. Read Power Control Disable

This circuit disables the ENR (Enable Read Adjust) signal preventing the Read Power Control Circuit from updating the Laser Diode read power level. It is activated when the Read Power Control Circuit reaches maximum level, to prevent rolling over of the counters.

3.10.6. Read Power Control Circuit

The Read Power Control Circuit consists of a 10-bit up/down counter and a digital-to-analog converter (DAC). Read power level update signals (DUR and ENR), from the Laser Power Check Circuit, enable the counter to be clocked either up or down by RPCK. RPCK clocks the counter when the read power level is checked. The output of the counter is a 10-bit digital value, representing the new (updated) read power current value. The digital value is input to the DAC, which converts it to the new read power setting for the Read Power Current Source.

3.10.7. Read Power Switch

The Read Power Switch is used to turn off read current to the Laser Diode, when an unsafe condition has been detected:

- Laser Diode output power is too high

- Laser Diode output reflected from the Media (Quad Sum) is too high

- Servo/Drive Control PCA has detected a condition which requires that the Laser Diode be shut down.

Read power is turned off to prevent the destruction of the Laser Diode and to prevent writing in the Media with read power.

When Laser Diode read power exceeds the upper power level window, an associated error signal is sent to the Read Power Switch (RPAUL: read power has exceeded the upper power limit). This signal is input to the FPLA which comprises the Read Power Switch logic, generating RCS (Read Current Switch) high. RCS turns off a transistor switch which disables the Read Power Current Source.

The Quad Detector on the Carriage generates CARR QUAD SUM, which indicates the total laser energy being received from the Media. When the Quad Sum Too High detection circuit detects that the Laser Diode is producing too much energy, QSTHN (Quad Sum Too High Not) is input to the Read Power Switch FPLA. QSTHN generates RCS high, which turns off read power to the Laser Diode.

On detection of one of the following conditions, the Servo/Drive Control PCA activates +RD PWR DSBL to shut down read power to the Laser Diode:

- Carriage out of focus
- Fault condition detected
- Carriage at rest in the retract position

The +RD PWR DSBL high signal is inverted and input to the Read Power Switch FPLA. The FPLA generates RCS, which turns off the Read Power Current Source.

When a high Read Power Error Status is generated by the Read Current Detection circuit, read power is disabled by the Servo/Drive Control PCA.

3.10.8. Read Power Current Source

This circuit provides read current (I RD) to the Laser Driver on the Carriage. Read current is enabled by RCS low from the Read Power Switch.

3.10.9. Read Current Detection

The Read Current Detection circuit monitors read current from the Read Power Current Source for loss of current or a current level that is too low. When read current is zero or too low, RD CURR LOW STAT goes high. This status can be caused by a fault on the Read/Write Control PCA or an open circuit on the backplane.

The Read Power Current Source has a preset value, which is not controlled by the Read Power Control Circuit. The Read Current Detection circuit also checks read current for this preset value. When the preset value is too low, RD CURR LOW STAT goes high.

3.10.10. Write Power Control Disable

This circuit disables the ENW (Enable Write Adjust) signal, preventing the Write Power Control Circuit from updating the Laser Diode write power level. It is activated when the Write Power Control Circuit reaches maximum level, to prevent rolling over of the counters.

3.10.11. Write Power Control Circuit

The Write Power Control Circuit consists of a 10-bit up/down counter and a DAC. Write power level update signals (DUW and ENW), from the Laser Power Check Circuit, enable the counter to be clocked either up or down by WPCK. WPCK clocks the counter when the write power level is checked. One WPCK pulse is generated for every four write pulses, except during the beginning of a sector when +WRT FLAG WIND (Write Flag Window) is high. The output of the counter is a 10-bit digital value, representing the updated write power current value. The digital value is input to the DAC, which converts it to the new write power setting for the Write Power Current Source.

3.10.12. Write Power Switch

The Write Power Switch is used to turn off write current to the Laser Diode, when an unsafe condition has been detected. (Refer to the description of +WRT PWR DSBL in the subsection on Read/Write Control PCA Interface Signals.)

When Laser Diode write power exceeds the upper power level window, an associated error signal is generated to the Write Power Switch (WPAUL: write power has exceeded the upper power limit). This signal is input to the FPLA which comprises the Write Power Switch logic, generating WCS (Write Current Switch) high. WCS turns off a transistor switch which disables the Write Power Current Source.

The Quad Detector on the Carriage generates CARR QUAD SUM, which indicates the total laser energy being received from the Media. When the Quad Sum Too High Detection circuit detects that the Laser Diode is producing too much energy, QSTHN (Quad Sum Too High Not) is input to the Write Power Switch FPLA. QSTHN generates WCS high, which turns off write power to the Laser Diode.

When a condition is detected which requires that write current to the Laser Diode be turned off, the Servo/Drive Control PCA makes +WRT PWR DSBL high. This signal is inverted and input to the Write Power Switch FPLA. The FPLA generates WCS, which turns off the Write Power Current Source.

When a high Write Power Error Status is generated by the Write Current Detection circuit, write power is disabled by the Servo/Drive Control PCA.

3.10.13. Write Power Current Source

This circuit provides write current (I WRT) to the Laser Driver on the Carriage. This current source is enabled by WCS low from the Write Power Switch.

3.10.14. Write Current Detection

The Write Current Detection circuit monitors the write current control voltage from the Write Power Current Source for loss of current or a current level that is too low. When write current is zero or too low, WRT CURR LOW STAT goes high. This status can be caused by a fault on the Read/Write Control PCA or an open circuit on the backplane.

The Write Power Current Source has a preset value, which is not controlled by the Write Power Control Circuit. The Write Current Detection circuit also checks for this preset write current value. When the preset value is too low, WRT CURR LOW STAT high is generated.

3.10.15. Dying Status Circuit

This circuit monitors the output of the Read and Write Power Control Circuits for an indication that Laser Diode performance is degrading too much. When the outputs of the digital up/down counters indicate the Power Control Loop is reaching the maximum current value, and cannot go higher, LASE DYE STAT (Laser Dying Status) goes high. This status informs the Servo/Drive Control PCA that Laser Diode performance is approaching a point where read and write operation of the LD 1200 will be affected.

3.10.16. Quad Sum Too High Detection

This circuit provides additional protection against damage from Laser Diode power going too high. It provides another means of monitoring laser output power, should the Sense Diode in the Laser Pen stop working or degrade rapidly.

The Quad Detector on the Carriage generates CARR QUAD SUM, which indicates the total laser energy being received from the Media. When the Carriage is on track (+OFF TRK STAT is low) and is at the beginning of a sector (+READ HEADER is high), the Quad Sum Too High Detection circuit checks CARR QUAD SUM for an acceptable energy level. When the circuit detects that the Laser Diode is producing too much energy, it generates +QUAD HI STAT (Quad Sum Too High Status) high to the Servo/Drive Control PCA and QSTHN low to the Read and Write Power Switches. QSTHN causes these circuits to turn off power to the Laser Diode.

3.10.17. Logic

The Logic circuit generates SPS (Stop Sampling) for the Modulator Demodulator Synchronizer PCA. SPS is used in the sampling of TOON-encoded read data and write verify data from the Media.

During initialization or a Read operation, SPS is generated by 2CLK, which is selected through a multiplexer by +WRITE WINDOW low and -SER WRT DATA high. During a Write operation, write pulses from the DRDW Delay Setting circuit (-DRDW WRITE DATA) are input to a multiplexer in the Logic circuit. SPS is generated when -DRDW WRITE DATA is gated through the multiplexer by +WRITE WINDOW and -SER WRT DATA.

3.10.18. Write Pulse Delay Setting

The Write Pulse Delay Setting circuit synchronizes the pulse used to write a data monohole in the Media with the zero-crossing of disk clock. Serial write data (-SER WRT DATA) from the Modulator Demodulator Synchronizer PCA and 2CLK (which is in phase with the disk clock) are input to a NOR gate. The NOR gate synchronizes the write data to the zero-crossings of 2CLK. The write data is then converted to emitter-coupled logic (ECL) levels and input to a 100-nanosecond fixed delay line. The write data from the delay line is input to a 50-nonosecond selectable delay line. The delay produced by the second delay line is selected by jumper, allowing the time between the receipt of 2CLK and the output of write data to the Carriage (±WRT DATA) to be adjustable. The write data output from the second delay line is input to the Write Pulse Width Setting circuit.

3.10.19. Write Pulse Width Setting

When the disk is spinning at a fixed speed, more energy is required to write a hole in a track at the outer radius than to write the same size hole in a track at the inner radius. The Write Pulse Width Setting circuit varies the amount of energy used to write in the Media as the Carriage moves outward from the spindle (refer to figure 3-64).

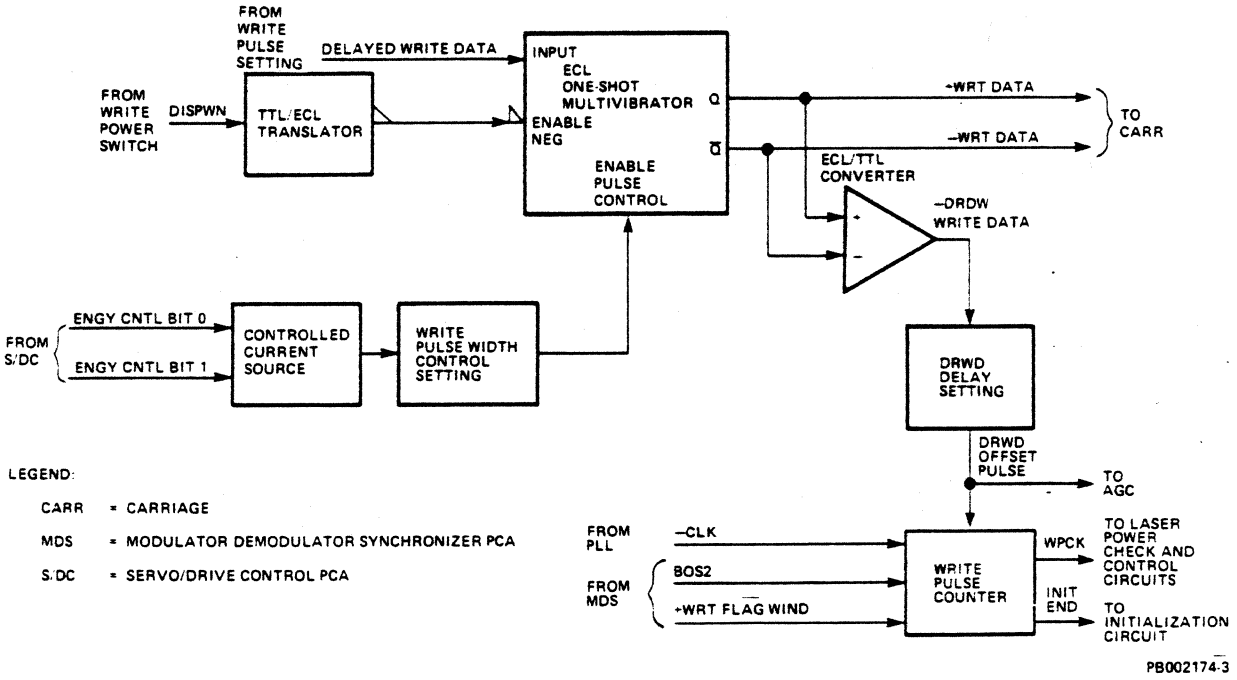


Figure 3-64. Write Pulse Width Setting Block Diagram

Write power level is specified by the Servo/Drive Control PCA using signals ENGY CNTL BIT0 and ENGY CNTL BIT1:

BIT 0	BIT 1	TRACK RANGE	WRITE PULSE WIDTH
0	0	0 - 12287	49.5 nanoseconds
0	1	12288 - 18431	52.0 nanoseconds
1	0	18432 - 24575	54.5 nanoseconds
1	1	24576 and up	57.0 nanoseconds

ENGY CNTL BIT0 and ENGY CNTL BIT1 are input to the Controlled Current Source. The states of these signals control the amount of current produced by the current source. The Write Pulse

Width Control Setting circuit draws current from the current source. The amount of current drawn by this circuit determines the write pulse width control setting. This control setting is applied to the enable pulse control input of the ECL one-shot multivibrator.

Serial Write Data pulses from the Write Pulse Delay Setting circuit are input to the ECL one-shot multivibrator. The multivibrator is enabled by DISWPN (write power is not disabled) from the Write Power Switch. The write data pulses cause the multivibrator to generate ±WRT DATA pulses with the pulse width specified by the write pulse width control setting. The ±WRT DATA pulses are output to the Carriage and are converted to TTL levels (-DRDW WRITE DATA) for input to the DRDW Delay Setting and thereby the Write Pulse Counter Circuit.

The DRDW OFFSET PULSE is input to a divide-by-four counter in the Write Pulse Counter Circuit. After four write pulses, the counter clocks a flip-flop which produces a Write Power Clock (WPCK). WPCK causes the Power Control Loop to take a write power sample.

3.10.20. DRDW Delay Setting

The DRDW Delay Setting circuit provides an adjustable delay for the SPS signal output to the Modulator Demodulator Synchronizer PCA and the DRDW OFFSET PULSE signal input to the read amplifier/current switch in the AGC. Write data from the Write Pulse Width Setting circuit is input to a 50-nanosecond selectable delay line. The delay is selected using jumpers. The output of the delay line is routed to the read amplifier/current switch in the AGC and the Logic circuit where it is used to generate SPS.

3.10.21. Automatic Gain Control

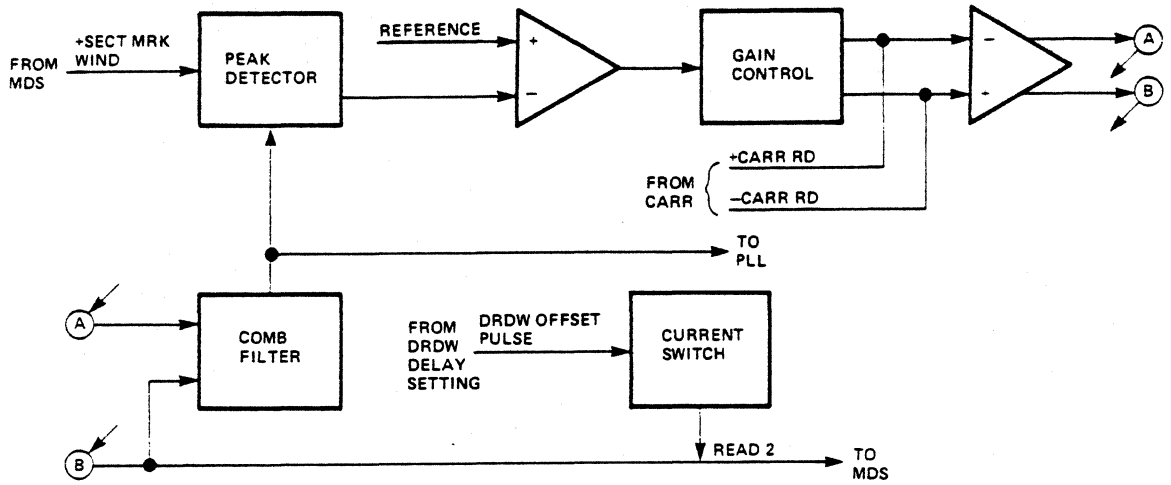
The Automatic Gain Control stabilizes the gain of the read signals received from the Read Preamplifier in the Carriage (refer to figure 3-65). From initialization of the LD 1200 until two consecutive Sector Marks have been read, the AGC continuously updates read data gain. After the second Sector Mark has been read, gain adjustment is performed once per sector, during the reading of the Sector Mark.

The differential read signal from the Carriage (±CARR RD) is ac coupled through input buffers to an operational amplifier. The gain of the operational amplifier is controlled by the Gain Control circuit. The positive output of the amplifier (READ2) is output to the Modulator Demodulator Synchronizer PCA. In addition, both outputs of the operational amplifier are input to the COMB Filter. The COMB Filter improves disk clock extraction from the overall read signal.

The output of the COMB Filter is routed to both the PLL and the Peak Detector. At the beginning of each sector, the Peak Detector is enabled by +SECT MRK WIND (Sector Mark Window), from the Modulator Demodulator Synchronizer PCA. It detects the peak value of the prerecorded Sector Mark which is being read from the Media. That value is compared against a reference voltage by an operational amplifier. The difference voltage is fed back to the Gain Control, which adjusts the gain of the operational amplifier supplying read signals to the Modulator Demodulator Synchronizer PCA and the PLL.

When +SECT MRK WIND goes low, the Peak Detector is disabled, preventing further gain adjustment. The fall of +SECT MRK WIND indicates the LD 1200 electronics have initialized to the point of synchronization with the disk or that the Sector Mark has been read.

Occasionally, Laser Diode write power can drop low enough that an amorphous (partially formed) hole is written in the Media. An amorphous hole is not fully formed and usually disappears in a few days, making the data unstable. To protect against amorphous writing, the DRDW OFFSET PULSE, from the DRDW Pulse Delay circuit, adds a negative offset to the read data. Because the PIP (write verification readback signal) from an amorphous hole is smaller than one from a properly formed hole, the offset cancels it out and the PIP is not as seen as read data by the Modulator Demodulator Synchronizer PCA.



LEGEND:

MDS = MODULATOR DEMODULATOR SYNCHRONIZER PCA

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Figure 3-65. Automatic Gain Control Block Diagram

3.10.22. Phase-Locked Loop and VCO Frequency Delay Setting

The PLL synchronizes the internal clock with the clock read from the Media and produces the clocks used for read and write timing:

- CLK (Clock) - This is a timing signal that is in phase with the zero-crossings of the clock prerecorded in the Media. CK goes high at the positive-going zero-crossings and low at the negative-going crossings.
- -CLK (Clock Not) - This signal is the inverse of CLK.
- 2CLK (2 X Clock) - This signal is twice the frequency of CLK. It is the major timing signal used in the Read/Write Channel.
- -2CLK (2 X Clock Not) - This signal is the inverse of 2CLK.

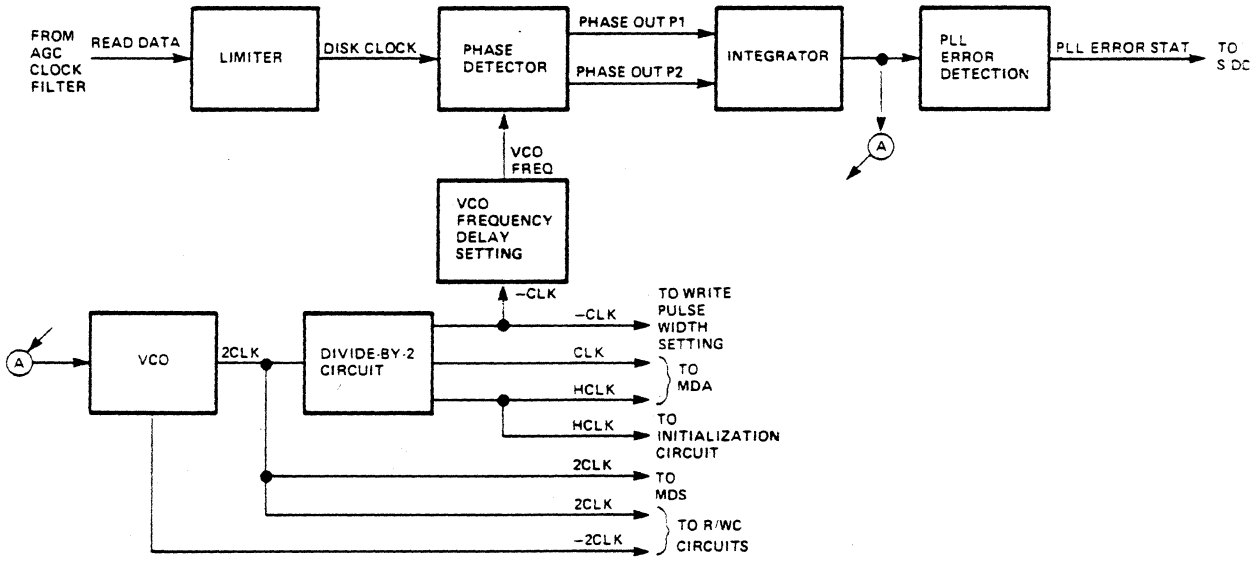
- HCLK (Half Clock) - This signal is half the frequency of CLK.

(Refer to figure 3-66.)

Read data from the Media is routed through the AGC circuit to the PLL. In the PLL, the read data is input to the Limiter, which clips the Read and Write data pulses, leaving the disk clock pulses intact. The disk clock is input to the Phase Detector along with VCO FREQ (VCO Frequency, the current frequency at which the PLL is running). The Phase Detector compares the frequencies of the two signals and produces a differential phase error signal, which defines the phase difference between them (PHASE OUT 1 and 2). The phase error signal is input to the Integrator, which produces a control voltage representing the adjustment that must be made to bring the VCO frequency in phase with the disk clock. This voltage is input to the VCO (Voltage Controlled Oscillator) and the PLL Error Detection circuit. The control voltage causes the VCO to adjust the VCO frequency to the phase of the disk clock, synchronizing the two signals.

The VCO runs at twice the frequency of the disk clock, producing 2CLK and -2CLK. The 2CLK output of the VCO is input to the Divide-By-2 circuit. This circuit produces the remainder of the timing signals required for read and write timing.

The -CLK output of the Divide-By-2 circuit is input to the VCO Frequency Delay Setting circuit. This signal is delayed by a selectable amount of time and output as VCO FREQ. The selectable delay allows adjustment of the phase of the internal clocks in relation to that of the disk clock. VCO FREQ is input to the Phase Detector for comparison with the disk clock.



LEGEND:

MDS = MODULATOR DEMODULATOR SYNCHRONIZER PCA

R/WC = READ/WRITE CONTROL PCA

S/DC = SERVO/DRIVE CONTROL PCA

PB002174-2

Figure 3-66. PLL and VCO Frequency Delay Setting Block Diagram

The ability of the PLL to maintain phase lock on the disk clock is monitored by the PLL Error Detection circuit. This circuit compares the phase error control voltage from the Integrator with a reference. When a phase error greater than 30 degrees is detected, PLL ERROR STAT (PLL Error Status) is sent to the Servo/Drive Control PCA.

The PLL includes two functions which are selected and installed at the factory: PLL offset and frequency. The PLL offset selection network is in the Integrator circuit. It is used to compensate for the offset introduced by the Phase Detector and the operational amplifiers in the Integrator. The PLL frequency selection network is in the VCO circuit. It is used to set the VCO frequency. Both networks are comprised of resistors which are selected and installed at the factory.

3.10.23. Wobble Detection

Wobble bytes (prerecorded in the Media) provide a low frequency tracking signal to supplement the Push-Pull Signal in keeping the laser beam following the center of the track. Wobble bytes are recorded off center, to the left and right of the nominal track center, as shown in figure 3-67. When the laser beam is centered in the nominal track, the left and right wobble byte signals cancel each other. Movement of the laser beam to the left or right increases the signal from the associated wobble byte.

Timing signals +LEFT PULSE and +RIGHT PULSE, from the Modulator Demodulator Synchronizer PCA, indicate whether a left or right wobble byte pulse is currently being read through the AGC. When a left wobble byte is being read, +LEFT PULSE enables the monohole pulses to a peak detector. The peak detector produces a level representing the peak amplitude of the wobble pulse. A level representing the peak of the left wobble byte is stored in a buffer. When the peak amplitude of the right wobble byte is detected, the right level is subtracted from the left to produce error signal WOBBLE ERROR SIG, which is sent to the Error Signal Generator PCA. This signal represents the difference between the two wobble signals, indicating how far from nominal track center the laser beam has moved and in what direction.

3.10.24. Carriage Power Supply Interconnect

The Carriage Power Supply Interconnect provides a path from the Power Supply to the Carriage for the following voltages: +12V, -12V, +5V, -5V, and +40V. With the exception of the +40-supply, voltages output to the Carriage are not filtered on the Read/Write Control PCA.

This circuit also provides supply voltage and error detection for the Position Sensor light source LED on the Carriage. POSITION SUM from the Carriage is used to generate POS LED SUPLY (Position LED Supply Voltage) and to check the output of the light source LED. When the output of the Position Sensor exceeds the limits of the reference, POS LED FAILURE (Position LED Failure) high is output to the Servo/Drive Control PCA.

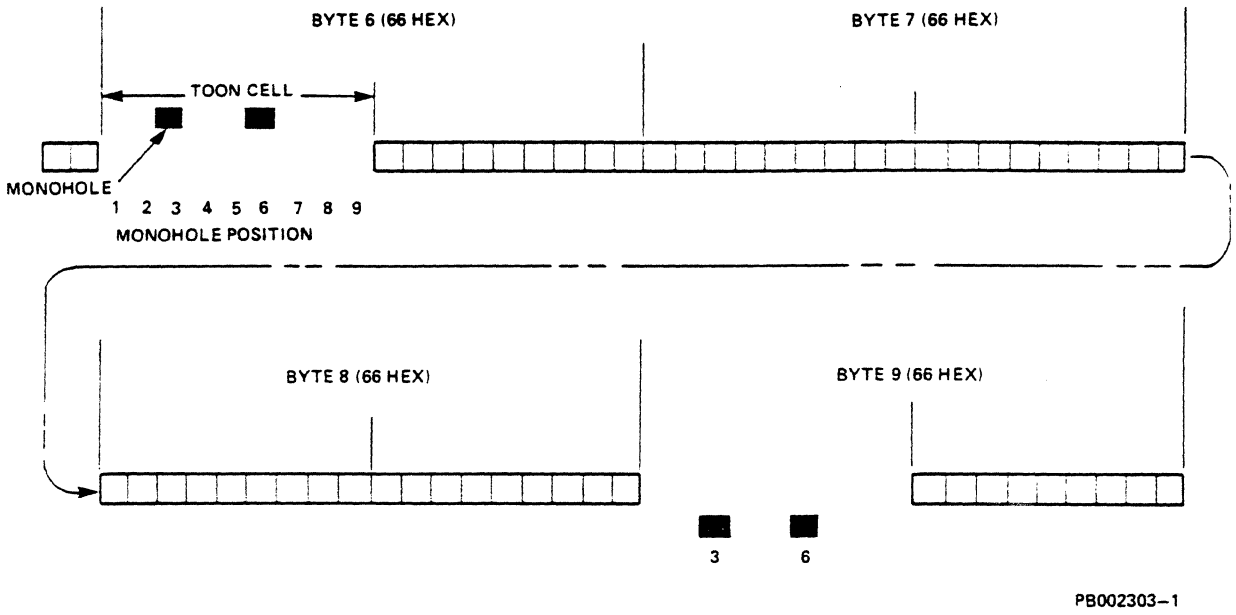


Figure 3-67. Wobble Bytes

3.11. MODULATOR DEMODULATOR SYNCHRONIZER PCA

The Modulator Demodulator Synchronizer (MDS) PCA performs basic data manipulation functions within the LD 1200, including:

- Sector Mark decoding
- Header identification (ID)
- Two-out-of-nine (TOON) modulation and demodulation
- Data serialization and deserialization
- Data interleaving and de-interleaving
- Write Verification
- Automatic rewrite operations
- Wobble byte verification

The MDS PCA decodes the Sector Header, Vector Address Field, Data Field, and Postfield (including all ECC codewords) from the Media and routes the decoded information to the appropriate destinations. Header information is sent via the SIA Bus to the Servo/Drive Control PCA. Vector address, user data, and Postfield information (including all ECC codewords) are sent

over the SIA Bus to the Common Memory in the Error Correction and COMEM Interface Unit (ECC) PCA.

The functional block diagram of the MDS PCA is shown in figure 3-68. Descriptions of the interface signals and functional blocks shown in the illustration are provided in the following subsections. Descriptions of the functions performed by the MDS PCA are provided in the LD 1200 Functions - Read/Write subsection.

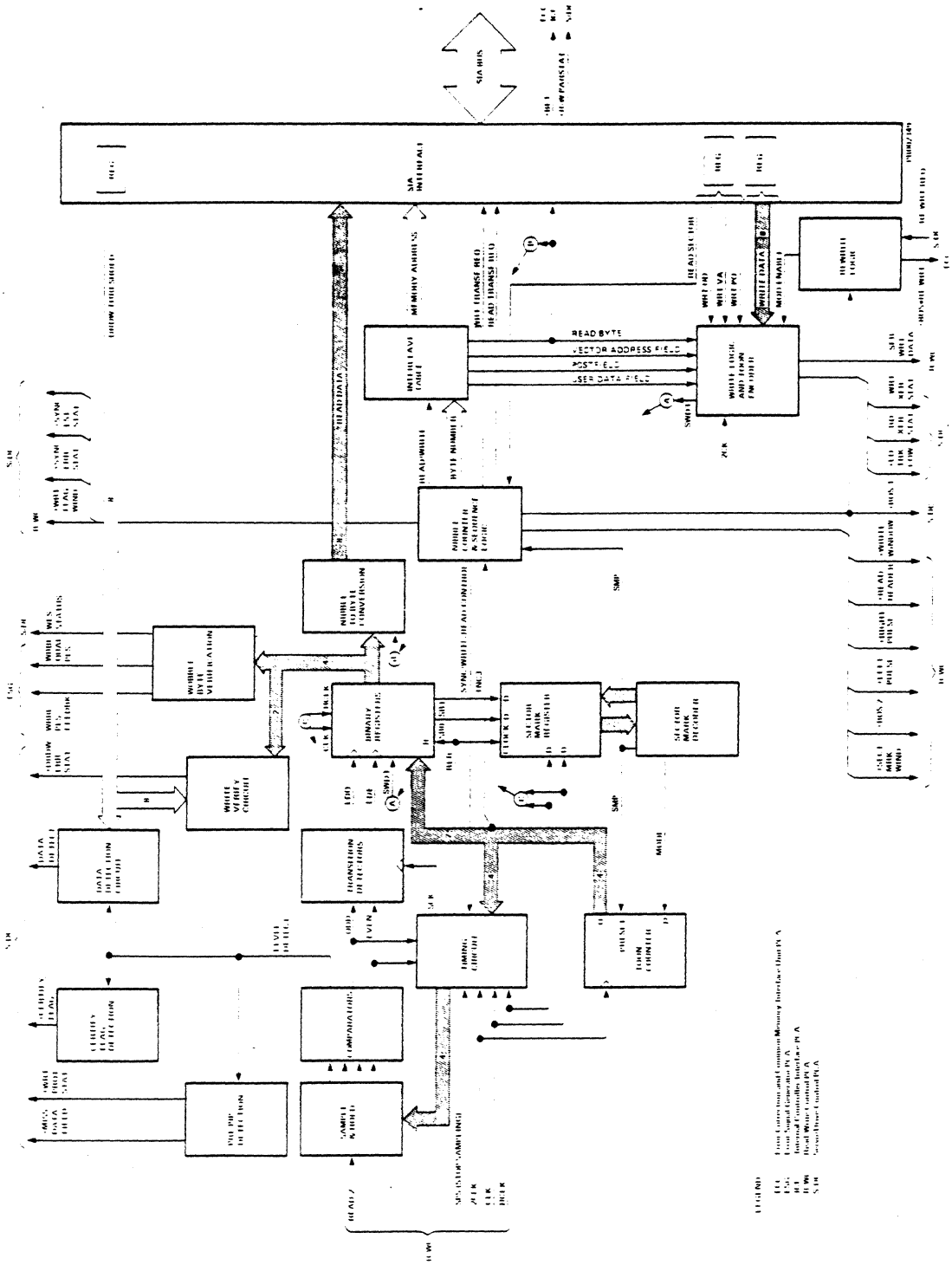


Figure 3 68 Modulator Demodulator Synchronizer PCA Block Diagram

3.11.1. Interface Signals

The MDS PCA communicates with the remainder of the LD 1200 using the following interface signals:

READ2 (Read Data)

This signal is generated by the Read/Write Control PCA. It is an analog voltage representing TOON (Two-Out-Of-Nine) encoded data read from the Media.

SPS (Stop Sampling)

This signal is generated by the Read/Write Control PCA. It is used to reset each sample signal after a TOON position is sampled for the presence of a monohole.

CLK (Clock)

This signal is generated by the Read/Write Control PCA. It is a timing signal that is in phase with the zero-crossings of the clock read from the Media. CLK goes high at the positive-going zero-crossings and low at the negative-going crossings.

2CLK (2 X Clock)

This signal is generated by the Read/Write Control PCA. It is a timing signal that is twice the frequency of the CLK signal.

HCLK (Half Clock)

This signal is generated by the Read/Write Control PCA. It is a timing signal that is half the frequency of the CLK signal.

-REWRT REQ (Rewrite Request)

This signal is generated by the Servo/Drive Control PCA. It is low when a Rewrite is to occur in the next sector. This signal can go low at any time during a sector and is cleared at the beginning of the next sector.

A Rewrite Request is enabled by the ICI PCA, via the Servo/Drive Control PCA, when any of the following conditions occur:

- PLL Error
- DRDW Error
- Sync Error

If any other errors also occur, the Rewrite Request is cancelled.

The ICI PCA then monitors Servo/Drive Control PCA status to determine when a Rewrite occurs and counts the number of Rewrites performed. When the maximum number of Rewrites allowed has been performed, or if none are to be performed, -REWRT REQ is disabled.

WBBL PLS FEEDBK (Wobble Pulse Feedback)

This signal is generated by the Error Signal Generator PCA. It toggles near the beginning of the sector, when a sample of the Wobble Error Signal is being taken. The Wobble Pulse Feedback signal is used by the MDS PCA to verify that the Error Signal Generator Sample and Hold circuitry is functioning properly.

+MISS DATA FIELD (Missing Data Field)

This signal is output to the Servo/Drive Control PCA. When high, it indicates an attempt was made to write in the Postfield of a sector in which no data has previously been written. When this occurs, the Servo/Drive Control PCA inhibits writing and reports the condition to the ICI PCA, which must clear the error before writing can be attempted again.

+WRT PROT STAT (Write Protect Status)

This signal is output to the Servo/Drive Control PCA. It goes high when a write operation has been attempted in a field where something has previously been written. On receipt of this signal, the Servo/Drive Control PCA disables the write power to the Laser Diode and the error is reported to the ICI PCA. The ICI PCA uses the DATA DETECT signal from the MDS PCA to determine what action is necessary in response to +WRT PROT STAT. If the sector contains data, DATA DETECT will be high. If DATA DETECT is low, there is no data written in the sector, which indicates there is probably a defect in the associated Write Protect Byte. The ICI PCA can enable a Rewrite operation (via the Servo/Drive Control PCA) in the next sector.

Write Protect Status is cleared at the beginning of each new sector.

+CERTIFY FLAG

This signal is output to the Servo/Drive Control PCA. It goes high when a Certify Flag byte is detected in the sector Header. This information is reported by the Servo/Drive Control PCA to the ICI PCA during the sector in which the flag is detected to prevent writing in that sector.

DATA DETECT

This signal is output to the Servo/Drive Control PCA. When high it indicates data was detected in the current sector. DATA DETECT remains low in a sector until a predetermined number of monoholes have been detected in the data fields.

The status of DATA DETECT is reported to the ICI PCA at the end of each sector, making it unnecessary for that PCA to perform a sector read operation to determine whether a sector contains data.

When an Overwrite status occurs, DATA DETECT can be used to determine whether the sector contains data or there is a defect in the Write Protect Flag field.

+DRDW ERR STAT (Direct Read During Write Error Status)

This signal is output to the Servo/Drive Control PCA. It goes high when a write error occurs during a Write operation. On receipt of this signal, the Servo/Drive Control PCA immediately disables write power to the Laser Diode, the error is reported to the ICI PCA, and, if enabled, a Rewrite is performed in the next sector. If data is detected in the sector during the Rewrite, it is cancelled and the Laser Diode is disabled until the error is cleared.

This error is cleared at the beginning of each new sector.

+WBBL QUAL PLS (Wobble Qualifier Pulse)

This signal is output to the Error Signal Generator PCA. It is used to initiate the sampling of the WOBBLE ERROR signal into the Sample and Hold circuit on the Error Signal Generator PCA. A pulse is generated only if all the wobble bytes are read correctly.

WES STATUS (Wobble Error Signal Status)

This signal is output to the Servo/Drive Control PCA. It goes high when the MDS PCA has difficulty reading the wobble bytes in the Sector Header. When the Servo/Drive Control PCA receives a high WES STATUS, all Write activity is immediately stopped, the error is reported to the ICI PCA, and error recovery procedures are initiated.

Error recovery consists of waiting 20 milliseconds at the current location for the error to go away. If the error still exists after that time, and no other errors have occurred, the Carriage is retracted to the Home position and WES STATUS is checked. If the Wobble Error persists, a Wobble Fault is declared.

+WRT FLAG WIND (Write Flag Window)

This signal is output to the Servo/Drive Control PCA and Read/Write Control PCA. It is high while the laser beam is moving through the Write Protect Flag field. It is used by the MDS PCA to determine whether a sector is write protected. On the Servo/Drive Control PCA, +WRT FLAG WIND is used to latch the current Write Power Disable status. This status is made available to the ICI PCA, which uses it to determine whether an error prevented writing on the Media before or after the Write operation was to start in the sector.

On the Read/Write control PCA, this signal is used to inhibit write power updates during the Write Protect Flag field.

+SYNC ERR STAT (Sync Error Status)

This signal is output to the Servo/Drive Control PCA. It goes high if a sync word is not decoded within a predefined window. On receipt of a Sync Error, the Servo/Drive Control PCA disables the write power to the Laser Diode, the error is reported to the ICI PCA, and, if enabled, a Rewrite is performed.

This signal is used for resynchronization at the end of a Seek. Once resynchronization is accomplished, the Servo Processor begins the Track Verify process.

Sync Error Status is cleared in the Servo/Drive Control PCA on the leading edge of the Beginning of Sector Pulse (+BOS2).

+SYNC LST STAT (Sync Lost Status)

This signal is output to the Servo/Drive Control PCA. It goes low when two Sector Marks are decoded exactly 2400 nibbles apart. Sync is lost, and this signal goes high, when Sector Marks are not decoded for four consecutive sectors.

Sync Lost Status is checked by the LD 1200 during the startup sequence after tracking has begun. The LD 1200 should be in sync within 10 milliseconds after tracking is established. If not, a Sync Fault is declared.

If sync is lost after the startup sequence, the write power to the Laser Diode is disabled and read data requests are stopped. The error is reported to the ICI PCA and statuses are checked. If no other higher priority errors have occurred, the servo loops are opened, the Carriage is retracted, and the startup procedure is reexecuted. If a higher priority error has occurred, appropriate error recovery procedures are performed.

Sync Lost Status is cleared at the beginning of each sector on the leading edge of the Beginning of Sector Pulse (-BOS).

+BE1 (Bus Enable Out)

This signal is output to the ICI and ECC PCAs. It is made low by the MDS PCA to take control of the SIA Bus. This PCA has the highest priority on the bus. When the MDS PCA makes +BE1 low, the next lower priority module on the SIA Bus generates Bus Enable Out low to the next module down the bus. Propagating Bus Out Enable low through all the lower priority modules on the SIA Bus inhibits them from bus access until the MDS PCA releases control of the bus by making +BE1 high. When the bus is released, any of the busmaster modules on it can take control of the bus by making Bus Enable Out low.

+R/W PAR STAT (Read/Write Parity Error Status)

This signal is output to the Servo/Drive Control PCA. It goes high when the MDS PCA detects a parity error on the SIA Data Bus. On receipt of this status, the Servo/Drive Control PCA immediately stops all Write activity and reports the status to the ICI PCA. +R/W PAR STAT is cleared at the beginning of each new sector.

+BOS ● $\overline{\text{REWRITE}}$ (Beginning of Sector AND Rewrite Not)

This signal is output to the ECC PCA at the beginning of a sector in which a Rewrite operation is to take place. The signal assures that the data for the Rewrite is taken from the same physical data buffer as that used for the original Write attempt.

-SER WRT DATA (Serial Write Data)

This signal is output to the Read/Write Control PCA. It carries TOON-encoded write data for the disk.

-WRT XFR STAT (Write Transfer Status)

This signal is output to the Servo/Drive Control PCA. It is low during a sector in which a Write operation is occurring. Write Transfer Status is activated or deactivated at the beginning of each sector. This signal is used in status reporting, Rewrite Request generation, and to prevent jumpbacks.

-RD XFR STAT (Read Transfer Status)

This signal is output to the Servo/Drive Control PCA. It is low during a sector in which a Read operation is occurring. Read Transfer Status is activated or deactivated at the beginning of each sector. This signal is used in status reporting and to prevent jumpbacks.

+LD TRK LOW (Load Track Low)

This signal is output to the Servo/Drive Control PCA. It is high when the Track Least-Significant Byte, read from the Header, is being transferred from the MDS PCA to the Servo/Drive Control PCA over the SIA Bus. During the transfer, the Servo/Drive Control PCA compares this information from the Header with the address stored in the Track LSB Compare Latch. The results of this comparison are clocked into a status latch on the trailing edge of +LD TRK LOW.

+BOS 1, +BOS 2 (Beginning of Sector Pulse)

These signals are output to the Servo/Drive Control PCA (+BOS 1) and the Read/Write Control PCA (+BOS 2). They are high during the first nibble of a sector (1.62 microseconds). The Beginning of Sector Pulses indicate the start of timing for each sector. It is used to latch the accumulated error count from the previous sector into the Servo/Drive Control PCA and generate a sector interrupt to the Drive Microprocessor, causing it to update previous sector status.

+WRITE WINDOW

This signal is output to the Read/Write Control PCA. It is high during the time writing is allowed in the Data Field of a sector.

+READ HEADER

This signal is output to the Read/Write Control PCA. It is high once per sector, during the time the sector ID Field is being read from the Media.

+RIGHT PULSE

This signal is output to the Read/Write Control PCA. It is a timing signal which, when high, enables the Wobble Detection circuit on the Read/Write Control PCA to detect the peak level of a right wobble pulse from the Media.

+LEFT PULSE

This signal is output to the Read/Write Control PCA. It is a timing signal which, when high, enables the Wobble Detection circuit on the Read/Write Control PCA to detect the peak level of a left wobble pulse read from the Media.

+SECT MRK WIND (Sector Mark Window)

This signal is output to the Read/Write Control PCA. On initialization of the LD 1200, it is high until two consecutive Sector Marks have been read. Afterward, the signal is high once per sector, during the time the Sector Mark is being read from the Media and decoded.

3.11.2. TOON Counter

This circuit counts the monohole positions in a TOON cell and generates an address for each monohole position. A TOON cell consists of nine consecutive monohole positions in a Media track (refer to figure 3-90 and table 3-18 in the subsection on Data Recording Format).

The TOON Counter is a four-bit up counter configured to provide counts of 0 through 8 in binary. It is initialized at the beginning of each sector by -SMP (Sector Mark Pulse) from the Sector Mark Decoder. The counter is initialized to a known value which is determined by the state of the MODE signal from the Sector Mark Register. It is clocked by 2CK from the Read/Write Control PCA, generating a count at outputs TNC0 through TNC3. The count represents the address of the current monohole position. After a count of eight is reached (TNC3 high), the next 2CK resets the TOON Counter. TNC3 increments the Nibble Counter, which keeps track of the TOON cells (nibbles) in a sector.

3.11.3. Nibble Counter and Sequence Logic

The Nibble Counter and Sequence Logic provides control signals to sequence the MDS PCA and Servo/Drive Control PCA through operations associated with the storage and retrieval of data (refer to figure 3-69). This logic also provides Read/Write status signals to the Servo/Drive Control PCA for inclusion in status information that is made available to the ICI PCA.

Read/Write operation sequencing is based on keeping track of data nibbles in relation to the beginning of each sector. This is done by the Nibble Counter in conjunction with the TOON Counter. The TOON and Nibble Counters are initialized at the beginning of each sector. The TOON Counter counts the monohole positions in each TOON cell (nibble). When nine positions have been counted, the TOON Counter generates TNC3 (TOON PULSE 0), which increments the nibble count by one. The nibble count is applied to the Interleave Table to steer data between the MDS PCA and Common Memory (on the ECC PCA), and to the FPLA in the sequence logic. The FPLA uses the nibble count and command signals from the MDS logic to produce sequencing signals for data manipulation operations (refer to figure 3-70):

- Input Signals:
  - NC0 through NC11 (Nibble Count) - These signals provide a count of the data nibbles that have passed through the MDS PCA logic during the current sector.
  - SYNC NIBBLE - This signal indicates the end of a Sector Mark.
  - LOCK - This signal goes low when the MDS PCA logic is in synchronization with the Media.
  - -WRT CMD (Write Command) - When low, this signal initiates a Write operation sequence. When high, it initiates a Read operation sequence.
  - -LONG WRAP TEST - When low, this signal initiates a Long Wrap diagnostic test. It is used during maintenance only.

- Output Signals:

  - -RNC (Reset Nibble Counter) - This signal resets the Nibble Counter at the end of a sector. It is combined with TOON PULSE 0 to generate the BEGINNING OF SECTOR PLS signal.

  - -LNC (Load Nibble Counter) - This signal initiates the Nibble Counter to a known state at the end of a Sector Mark.

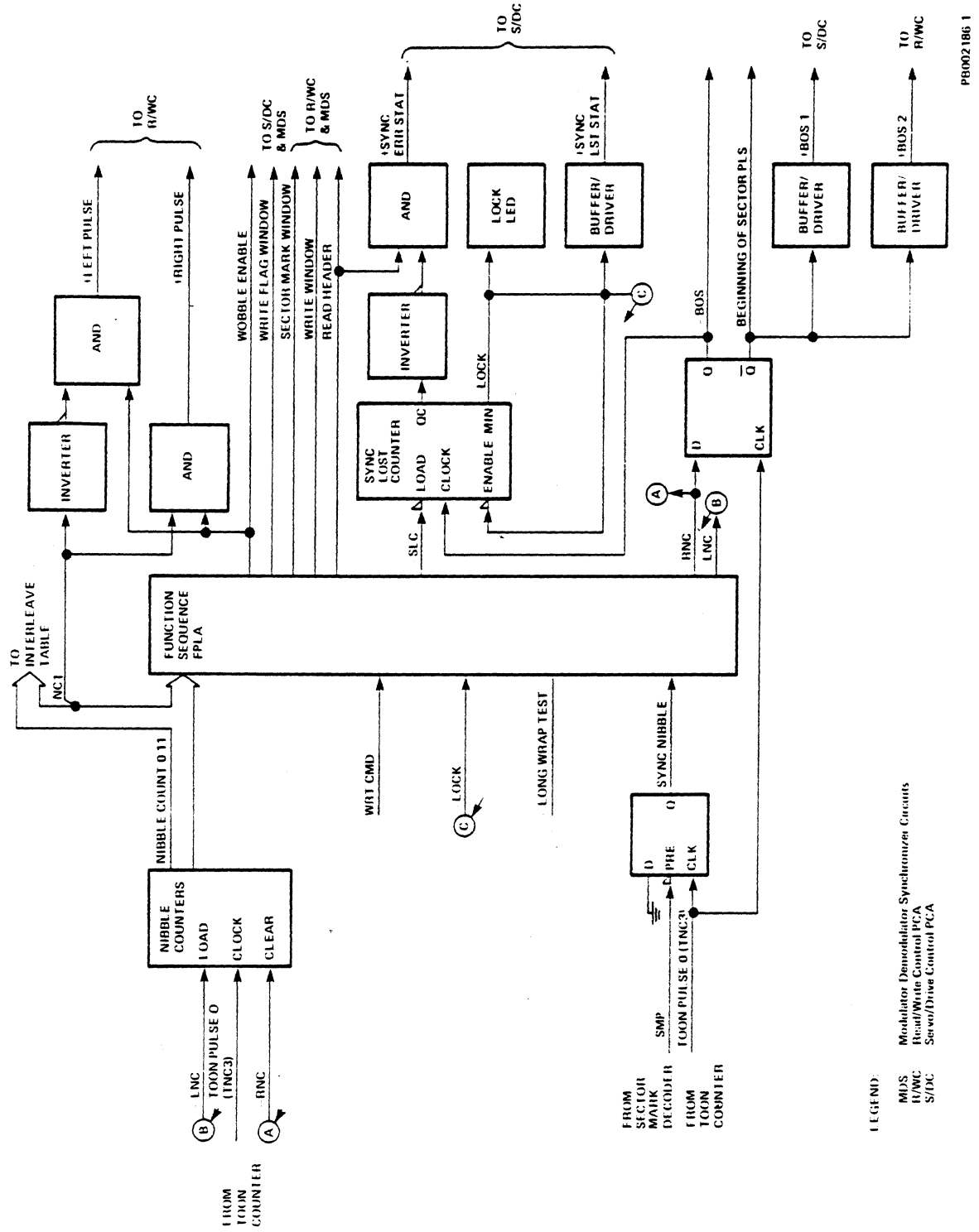


Figure 3-69. Simplified Nibble Counter and Sequence Logic

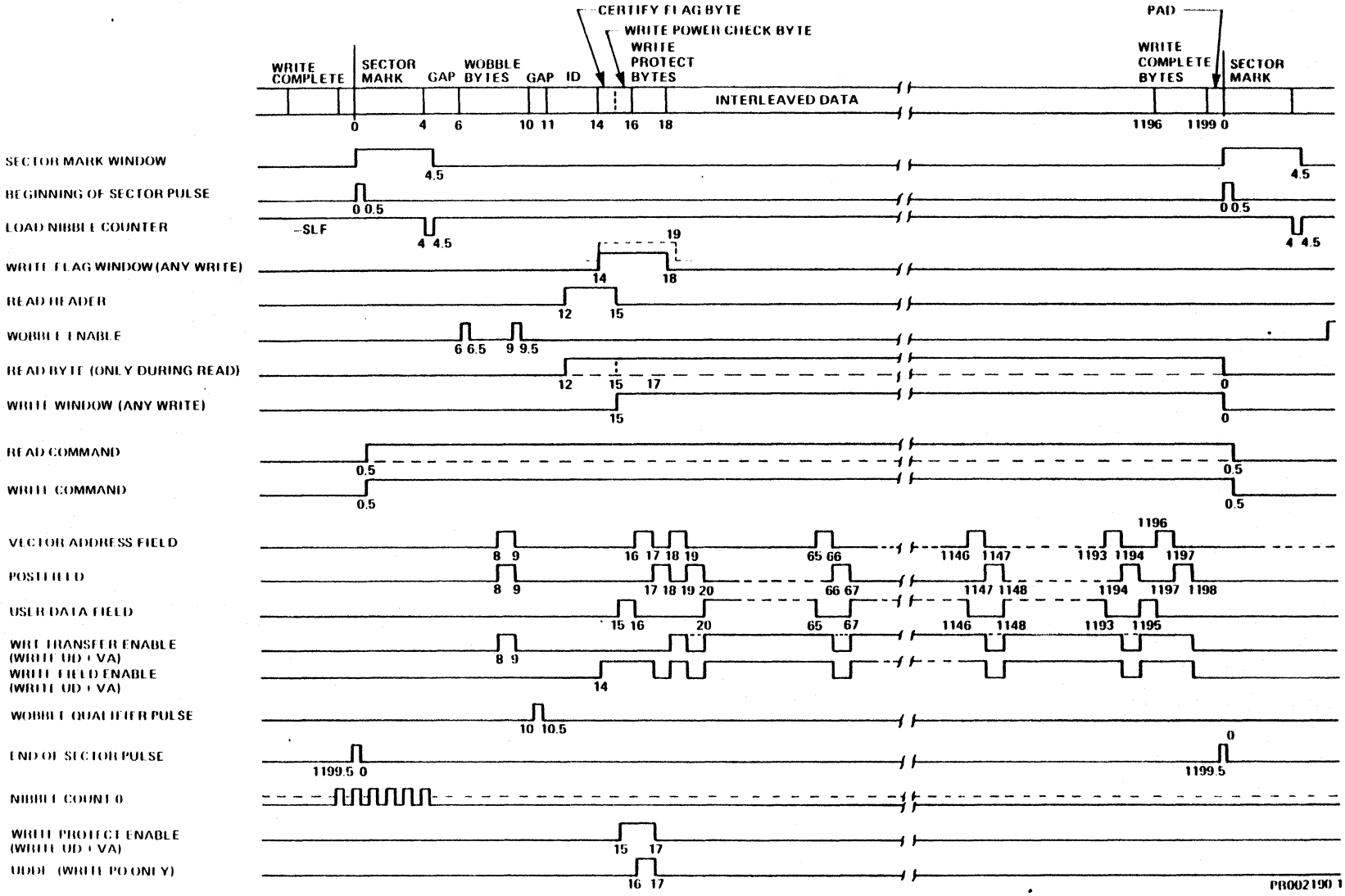


Figure 3-70. Sequence Signal Timing

- SECTOR MARK WINDOW - This signal goes high at the beginning of a Sector Mark and low following the end of the Sector Mark to define the duration of the Sector Mark. During this time, the MDS PCA logic is in the Sector Mark Search Mode.

- WOBBLE ENABLE - This signal goes high during the first wobble byte (Byte 6) and the last wobble byte (Byte 9). It enables the generation of +LEFT PULSE and +RIGHT PULSE to the Read/Write Control PCA.

- READ HEADER - This signal goes high at the beginning of the sector ID field and low following the Certify Flag Byte. It enables header information to be sent to the Servo/Drive Control PCA via the SIA Bus. READ HEADER is also used in generating the Sync Error Status, Load Track Low, and Certify Flag Signals to the Servo/Drive Control PCA.

- WRITE FLAG WINDOW - During a Read, this signal goes high before the first Write Protect Byte and low after the last. It is used to check the sector for write protection, by enabling a read of the Write Protect Byte, which precedes the data area.

  During a Write, this signal goes high at the beginning of the Certify Flag Byte and low following the last Write Protect Byte. It is used in the writing of the Certify Flag, Write Power Check, and Write Protect Bytes.

- WRITE WINDOW - This signal goes high before the Write Power Check Byte and low at the beginning of the next Sector Mark. It defines the period during which Laser Diode write power can be turned on for a Write operation.

- -SLC (Load Sync Lost Counter) - This signal loads a preset value into the Sync Lost Counter after the Sector Mark. It is used in the generation of Sync Error and Sync Lost Status to the Servo/Drive Control PCA.

WOBBLE ENABLE is ANDed with nibble count NC1 to generate +RIGHT PULSE. This signal enables the Wobble Detection Circuit on the Read/Write Control PCA to detect the peak of the right wobble pulses being read from the Media. NC1 is inverted and ANDed with WOBBLE ENABLE to generate +LEFT PULSE. This signal is used by the Read/Write Control PCA to detect the right wobble pulse peak.

When a Sector Mark is decoded, SYNC NIBBLE causes the FPLA to generate -SLC low. This pulse loads a preset value into the Sync Lost Counter, causing the Sync Error Status to go low (no Sync Error) and making the -LOCK signal low. The -LOCK signal turns on the LOCK LED and is buffered and output to the Servo/Drive Control PCA as Sync Lost Status low (Sync not lost). When READ HEADER goes high, Sync Error Status (which is low) is gated to the Servo/Drive Control PCA. At the beginning of the next sector -BOS clocks the counter, decrementing the count by one. This action makes the Sync Error Status line high. If a Sector Mark Pulse is generated at the end of the next Sector Mark, the counter is reloaded and the Sync Error Status line goes low. When READ HEADER goes high again, a good Sync Error Status is sent to the Servo/Drive Control PCA. If a Sector Mark Pulse is not generated, the counter is not reloaded. When READ HEADER goes high, the high Sync Error status (signifying synchronization is lost) is gated Servo/Drive Control PCA. If a Sector Mark Pulse is generated at the beginning of the next sector, the counter is reloaded and the Sync Error Status goes low again. Each time a Sector Mark is not generated, -BOS decrements the counter by one. When the counter has been decremented to zero, -LOCK goes high, disabling the counter, generating a high Sync Lost Status (signifying synchronization is lost), and turning off the LOCK LED.

3.11.4. Timing Circuit

This circuit provides timing sequences which enable the MDS PCA to sample and decode TOON-encoded data read from the Media. A unique timing sequence is provided for each of the following Read/Write Channel operations:

- Sector Mark detection
- Reading of data from the Media
- Verification of data holes as they are written through direct read during write (DRDW)

The majority of the Timing Circuit is implemented in a field-programmable logic array (FPLA).

3.11.4.1. Sector Mark Detection Timing

Signal 2CK from the Read/Write Control PCA is input to the Timing Circuit FPLA, which produces SCK (Sample Clock). It is the equivalent of 2CK inverted and delayed. This signal is used to clock the register which generates sample pulses S1 through S4. The SPS signal from the Read/Write Control PCA turns each of the sample pulses off, ending the sample periods.

On initialization of the LD 1200, or at the beginning of a new sector, the Sequence Logic makes +SECTOR MARK WINDOW high. This signal is input to the FPLA, placing the Timing Circuit in the Sector Mark Search Mode. In this mode:

- The sample signals are enabled by HCLK and CLK from the Read/Write Control PCA.
- Only sample signals S1 and S3 are generated, enabling the Odd Sample and Hold circuits, and disabling the Even circuits.
- Only OCK (Odd Clock) is generated, enabling the use of the Odd Comparator, Transition Detector, and Binary Register, and disabling the Even data path.

The phase relationship between HCLK and CLK is used to generate a sequence of addresses. Because these signals enable S1 and S3 during Sector Mark Search Mode, each sample taken is identified with an HCLK/CLK address.

On initialization of the LD 1200, HCLK can begin in either of two states (ONE or ZERO). Therefore, HCLK/CLK can produce two sets of addresses for the monoholes comprising the Sector Mark. To determine which of the sets of addresses to use, the logic monitors both sets until the first monohole is detected. If the first monohole is detected when HCLK/CLK specifies Address 2, HCLK is operating in Mode 0. The MODE signal from the Sector Mark Register goes low, and thereafter only addresses from the Mode-0 set are used to decode the Sector Mark. If the first monohole is detected at HCLK/CLK Address 0, the Sector Mark is decoded relative to the Mode-1 set of addresses.

At the beginning of each TOON cell in the Sector Mark, S1 is generated by HCLK/CLK to sample the first monohole position. At next monohole position in sequence, S3 is generated to sample the signal level. The signal levels of the two samples are compared by the Comparators. The result of the comparison generates signal ODD which is fed back to the Timing Circuit. If the S1 sample has the higher of the two signal levels, S3 is generated at the next HCLK/CLK address, thus saving the higher value in the S1 Sample and Hold circuit. If the S3 sample has the higher signal level of the two, S1 is the next sample signal generated. Sample pulses are generated in this manner for four monohole positions then the sampling sequence begins again with S1

When a higher sample signal level is detected (indicating the presence of a monohole), the output of the Odd Comparator changes state. This state change is clocked into the Odd Transition Detector by OCK (Odd Clock) from the FPLA in the Timing Circuit. OCK is equal to 2CLK during Sector Mark Search. In response to the comparator state change, the Odd Transition Detector generates LDO (Load Odd), which clocks the HCLK/CLK address of the detected monohole into the Odd Binary Register.

When the LD 1200 is initialized, two consecutive Sector Marks must be decoded successfully before the Read/Write Channel is synchronized with the Media.

3.11.4.2. Data Read Timing

Following the successful decoding of the Sector Mark, +SECTOR MARK WINDOW goes low, placing the Timing Circuit in the Data Read Mode. In this mode:

- The sample signals are enabled by the outputs of the TOON Counter and the Timing Circuit.
- All four sample signals are generated, enabling both the Odd and Even Sample and Hold circuits.
- Both OCK and ECK are generated, enabling both the Odd and Even data paths.

The states of the TOON Counter outputs, which are applied to the Timing Circuit, identify the address of the monohole position currently being read. The first position in a TOON cell (monohole position 1) has an odd address, therefore S1 is generated to sample it. The signal level sampled is stored in the Odd Sample and Hold circuit. The next position being even, S2 is generated to sample it. The signal level from the S2 sample is stored in the Even Sample and Hold circuit.

The next position in the TOON cell is sampled by S3. The signal level of the S3 sample is compared with that of the S1 sample. If the S1 sample has the higher signal level, that signal level and the associated address are retained as follows:

(1) At the next odd position, S3 is generated instead of S1, thereby leaving the S1 signal level unchanged.

(2) The address of the S1 sample is left unchanged in the Odd Binary Register.

If the S3 sample has the higher signal level, that signal level and associated address are retained as follows:

(1) At the next even position, S1 is generated, leaving the S3 signal level unchanged.

(2) The address of the S4 sample is left unchanged in the Odd Binary Register.

This self-adjusting sequence is continued through the sampling of the odd positions.

The next position in the TOON cell is even, therefore S4 is generated to sample it. As is done with the odd samples, the S2 and S4 signal levels are compared and the higher of the two is retained. This self-adjusting sequence also is continued throughout the sampling of the TOON cell. An example of a sample and hold timing sequence for a typical TOON cell is shown in figure 3-71.

NOTE

When a monohole is near the end of a TOON cell, the signal levels in associated sample and hold cells will be nearly equal until the monohole is reached. While the signal levels are so close, the output of the associated comparator is indeterminate, meaning either of the previous samples could be retained for comparison with the next sample taken.

Detection of a higher sample level indicates the presence of a monohole. When a higher odd sample is detected, the output of the Odd Comparator changes state. The state change is clocked to the Odd Transition Detector by OCK (Odd Clock) from the Timing Circuit. OCK is generated by S1 and S3. In response to the comparator state change, the Odd Transition Detector generates LDO (Load Odd), which clocks the address of the higher odd signal level (monohole) into the Odd Binary Register.

When a higher even sample level is detected, the state change of the Even Comparator is clocked to the Even Transition Detector by ECK. The change of state generates LDE (Load Even), which clocks the address of the higher even signal level into the Even Binary Register.

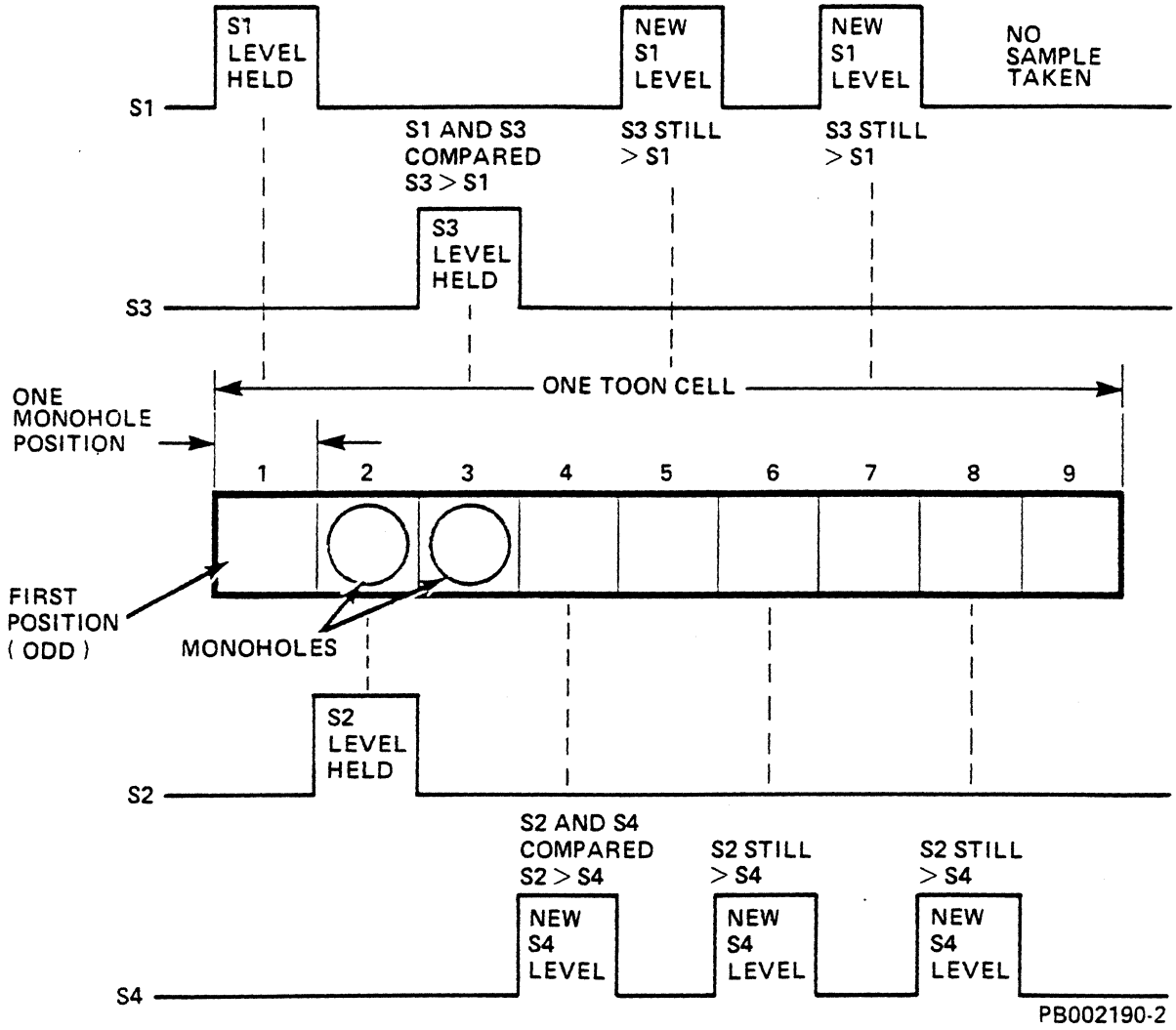


Figure 3-71. Sample and Hold Timing Sequence Example

3.11.4.3. Write Verify Timing

When data is written in the Media, the presence of a properly formed monohole is verified during the Write operation. Immediately after the write pulse that is used to burn the monohole is turned off, read power is turned on to sense the forming hole.

At the beginning of the Write operation, the Sequence Logic makes the +WRITE WINDOW signal high, placing the Timing Circuit in the Write Verify Mode. In this mode:

(1) The sample signals are enabled by the outputs of the TOON Counter and the Timing Circuit, and are turned off by the delayed SPS signal from the Read/Write Control PCA.

(2) All four sample signals are generated, enabling both the Odd and Even Sample and Hold circuits.

(3) Both OCK and ECK are generated, enabling both the Odd and Even data paths.

As described in the previous subsection (Data Read Timing), sample signals S1 through S4 are enabled by the outputs of the TOON Counter. In the Write Verify Mode, SPS extends the sample period into the trailing edge of the forming monohole by delaying the deactivation of the sample pulses. In this manner, the presence of a properly formed monohole can be detected during the Write operation (DRDW).

Each monohole position of the TOON cell is sampled in the same self-adjusting sequence as is used to read data. When a monohole is written, the associated Serial Write Data pulse from the Write Logic and TOON Encoder is delayed and fed back to the Binary Registers. Detection of a newly written monohole generates LDE or LDO, as applicable, which clocks the associated Binary Register. If a write data pulse was generated and no monohole is sensed, the delayed write data pulse is not clocked through the Binary Register indicating a DRDW error.

3.11.5. Sample and Hold

As the Media track is read by the laser beam, each position in a TOON cell is sampled for the presence of a monohole. These samples are taken by the Sample and Hold circuit, which consists of four cells: two for samples taken by odd sample signals S1 and S3, and two for those taken by S2 and S4 (refer to figure 3-72). A sample and hold cell consists of a field-effect transistor (FET) switch and a hold capacitor.

At the first monohole position in a TOON cell (odd position 1), the Timing Circuit generates S1 to sample READ2, representing the signal level read from the Media. S1 enables READ2 through the FET to the hold capacitor, where the signal level is stored. The signal level from the next position (even position 2) is sampled and stored by S2. At the next position (odd position 3), S3 samples and stores the associated signal level. The signal levels now in the S1 and S3 sample and hold cells are compared by the Odd Comparator. At the next odd position, the higher of the two signal levels is retained in the associated sample and hold cell. The cell containing the lower signal level is used to sample the next even monohole position (refer to figure 3-71). The same sample and comparison process is used for sampling even monohole positions: S2 followed by S4 followed by the even sample signal associated with the cell containing the lower signal level. This sampling sequence is followed throughout the TOON cell. At the beginning of the next TOON cell, the sequence begins again with S1 sampling the first monohole position.

Detection of a higher signal level indicates the presence of a monohole in the associated TOON-cell position. When a monohole is detected, the position address is copied into the associated Binary Register. The outputs of the Binary Registers are routed to the Sector Mark Register, Nibble-to-Byte Conversion, or Write Verify Circuit, as determined by the operation currently being performed (refer to subsections on Sector Mark Detection Timing, Data Read Timing, and Write Verify Timing).

3.11.6. Comparators

There is one Comparator circuit for each pair of sample and hold cells: odd and even (refer to figure 3-72). When an odd sample is taken, the Odd Comparator compares the current signal level with the previous signal level, stored in the other sample and hold cell. If the previous signal level is higher than the current sample, the output of the comparator remains unchanged. However, if the current sample has a higher signal level than the previous sample, the comparator goes high. The output of the comparator is clocked into a flip-flop by OCK from the Timing

Circuit. The ODD signal from the flip-flop is fed back to the Timing Circuit to alter the odd sample signal sequence (refer to the subsection on the Timing Circuit). OCK from the Timing Circuit inputs ODD to the Transition Detectors.

When an even sample is taken, the Even Comparator compares the previous and current samples and provides a high output when the current sample has the higher of the two signal levels. The state change of the comparator is latched into a flip-flop and made available to the Timing Circuit and Transition Detectors as the signal EVEN, as described for odd samples.

NOTE

When a monohole is near the end of a TOON cell, the signal levels in associated sample and hold cells will be nearly equal until the monohole is reached. While the signal levels are so close, the output of the associated comparator is indeterminate, meaning either of the previous samples could be retained for comparison with the next sample taken.

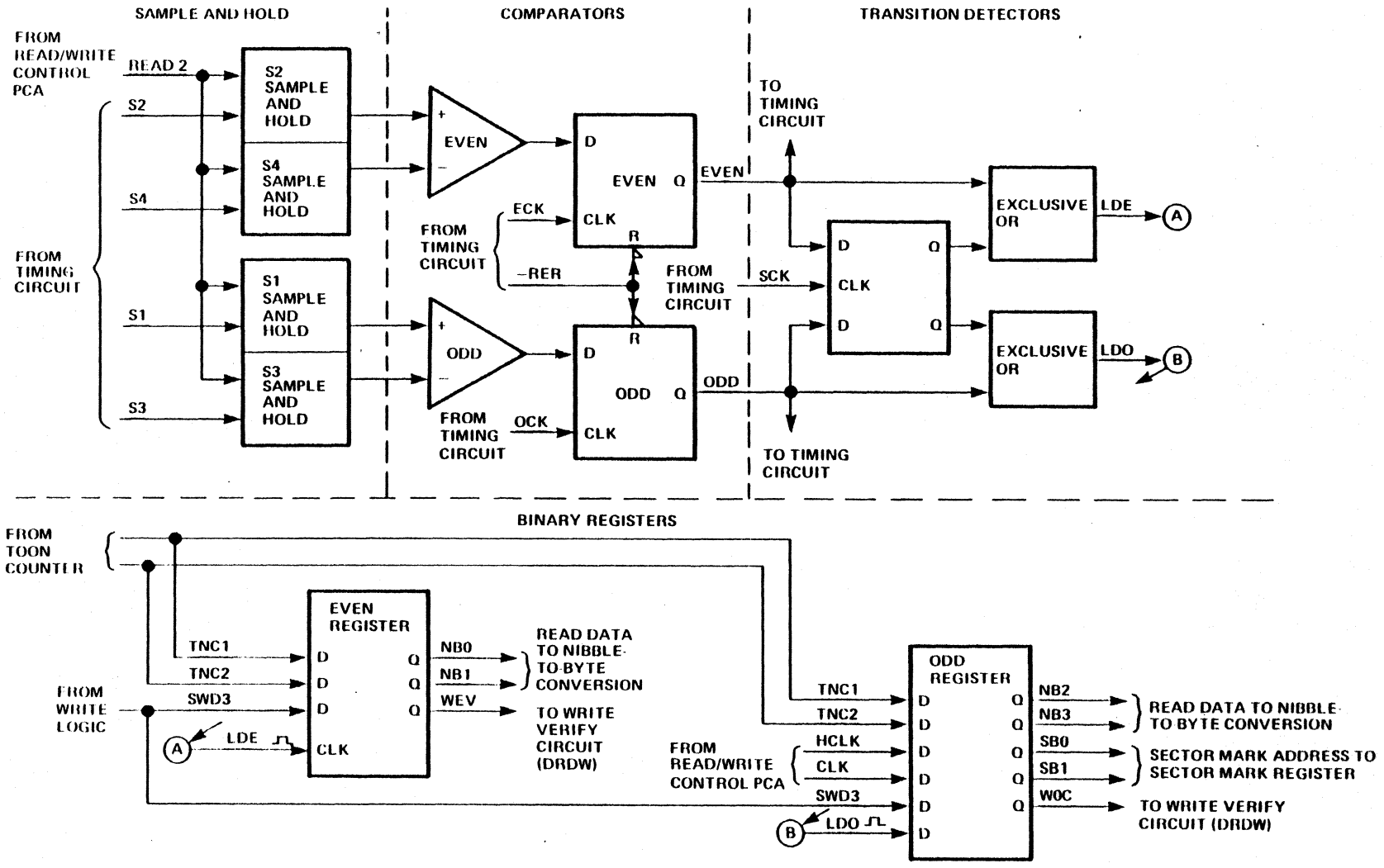


Figure 3-72 Data Path Simplified Logic

3.11.7. Transition Detectors

The Transition Detectors consist of a dual flip-flop to retain the last state change of the Odd and Even Comparators and an Exclusive-OR gate for each comparator to detect a transition from one state to another. The current state of the Comparators indicates a monohole has been detected at the associated TOON cell position.

Looking at the odd data path in figure 3-72, the detection of a monohole causes the Odd Comparator to make the ODD signal high. ODD is applied to the Exclusive-OR gate. The other input to the gate represents the previous state of the Odd Comparator. Because the inputs to the gate are different, the output is LDO high. Shortly thereafter, SCK clocks ODD into the dual flip-flop, making the output high. Now, both inputs to the gate are high, making output LDO go low. LDO is used to clock the address associated with the detected monohole into the Odd Binary Register, or to compare a delayed write data pulse with the resulting monohole indication during the Write Verify Mode.

As shown in figure 3-72, the detection of monoholes in even TOON cell positions is done in the same manner as described for odd monoholes.

3.11.8. Binary Registers

The Binary Registers are used as follows:

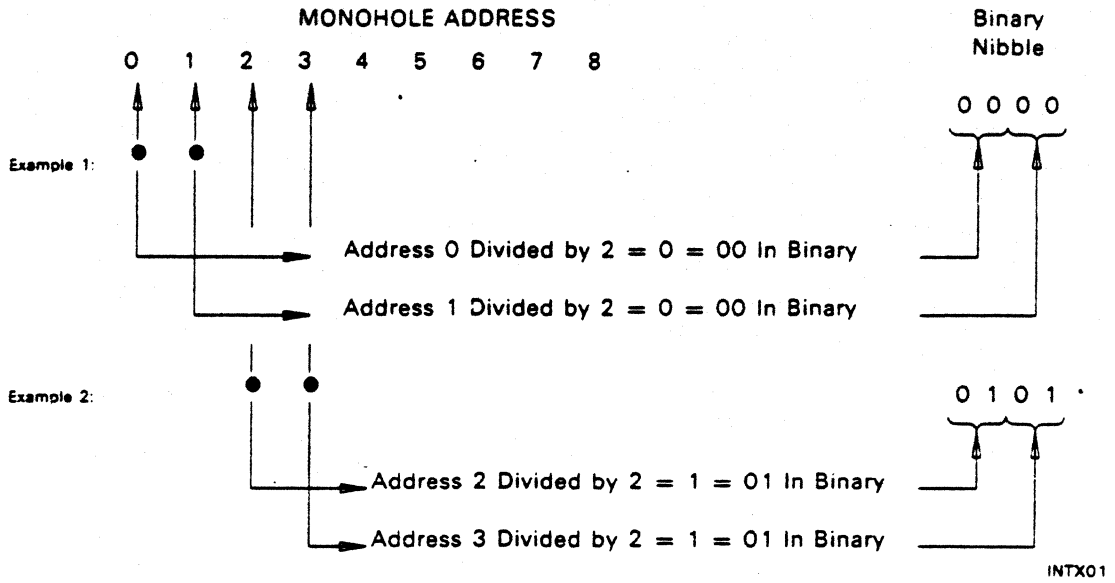
- During the Sector Mark Search Mode, to provide the address of a detected monohole to the Sector Mark Register
- During the Data Read Mode, to convert TOON-encoded data into a binary nibble (half a byte)
- During the Write Verify Mode, to compare a delayed write data pulse with the resulting monohole indication, to verify the proper formation of the hole in the Media

3.11.8.1. Sector Mark Search Mode

In this mode, the phase relationship between HCLK and CLK specifies the address of a detected monohole. The even data path is not used when the Sector Mark is being decoded. Therefore, when a monohole is detected, LDO clocks the associated address into the Odd Binary register. The monohole address (SB0 and SB1) is then output to the Sector Mark Register.

3.11.8.2. Data Read Mode

There is a systematic correspondence between the positions occupied by monoholes in a TOON cell and the binary address of the cell. As shown in table 3-18 (in the subsection on Data Recording Format), binary nibble 0000 is equivalent to a TOON cell with monoholes in positions 1 and 2 (monohole addresses 0 and 1 respectively). Dividing the even position address (0) by two, without regard to remainder, converts it to the two most-significant bits of the equivalent binary nibble. Dividing the odd position address (1) by two, without regard to remainder, converts it to the two least-significant bits of the nibble:



When a monohole is detected in an even position, LDE clocks associated address bits TNC1 and TNC2 from the TOON Counter into the Even Binary Register. The address appears at the output of the register as the two most-significant bits of the equivalent binary nibble (NB0 and NB1). The address of the odd monohole is clocked into the Odd Binary Register by LDO, providing the two least-significant bits of the nibble (NB2 and NB3).

3.11.8.3. Write Verify Mode

In this mode, the Binary Registers act as comparators to verify that a proper monohole has formed at a position where a Write operation was attempted. When a Write is attempted, the Write Logic and TOON Encoder provides a delayed Serial Write Data pulse (SWD3) to the D inputs of the Binary Registers. If a properly formed monohole is detected during DRDW of an even position, LDE clocks SWD3 into the Even Binary Register, generating WEV (Write Even Verified). This signal is input to the Write Verify Circuit, which uses it to generate a good DRDW Error Status. If the DRDW of an odd position results in the detection of a properly formed monohole, LDO clocks SWD3 through the Odd Binary Register as WOV (Write Odd Verified). WOV is also used by the Write Verify Circuit to generate a good DRDW Status.

3.11.9. Sector Mark Register and Decoder

The Sector Mark Register and Decoder decode a Sector Mark read from the Media to generate a Sector Mark Pulse (-SMP). This signal is used to initialize the TOON and Nibble Counters which provide counts to which monohole position and nibble boundaries are referenced.

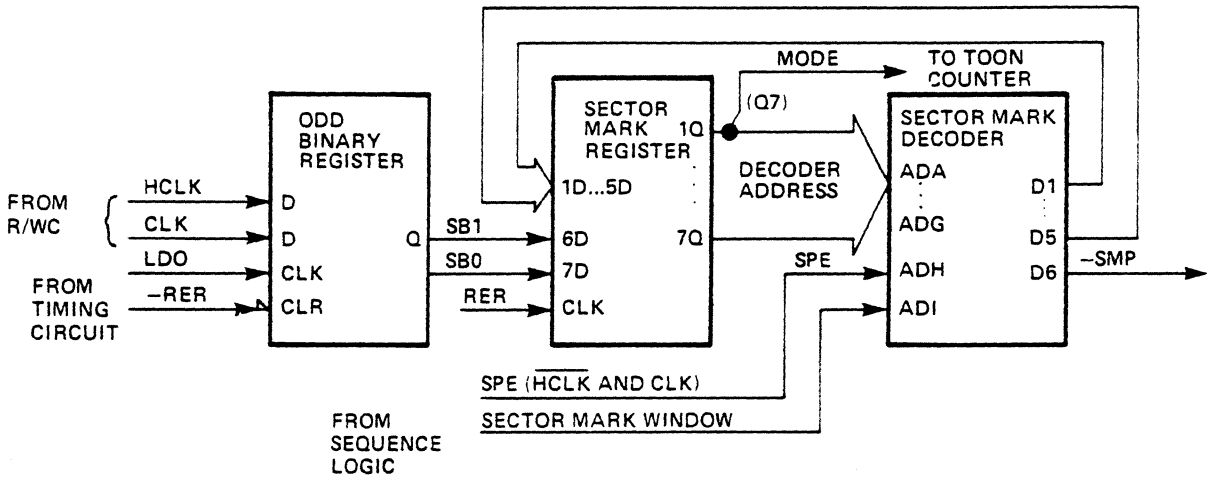
During Sector Mark decoding, the detection of a monohole in the Media generates LDO. This signal clocks the address of the monohole (specified by HCLK and CLK) into the Odd Binary Register (refer to figure 3-73). The -RER signal from the Timing Circuit clocks the address (now SB1 and SB0) into the Sector Mark Register. The monohole address is added to five outputs from the Sector Mark Decoder to form a new address for the decoder.

On initialization of the LD 1200, HCLK (which provides part of the monohole address) can begin in either of two states (ONE or ZERO). Therefore, HCLK/CLK can produce two different sets of addresses. To determine which of the sets of addresses to use, the Sector Mark Decoder monitors both sets until the first monohole is decoded. If the first monohole is detected at HCLK/CLK address 2, HCLK is operating in Mode 0. The MODE signal from the Sector Mark Register goes low and thereafter only addresses from the Mode-0 set are used to decode the Sector Mark. If the monohole address is 1, the Sector Mark is decoded relative to the Mode-1 set of addresses.

The Sector Mark Decoder looks for a specific series of 16 addresses:

- Mode 0: 2 2 2 2 1 1 1 1 ? 0 0 0 0 3 3 3 3
- Mode 1: 0 0 0 0 3 3 3 3 2 2 2 2 1 1 1 1

The question mark in the Mode-0 sequence represents a change in the uniform spacing between monoholes in the Sector Mark. This change results in an indeterminate state where a monohole should be. The Sector Mark Decoder is programmed to compensate for the indeterminate state and continue with the sequence. When the Sector Mark Decoder has recognized a complete sequence of addresses, a low Sector Mark Pulse is generated (-SMP).



LEGEND:

R/WC = Read/Write Control PCA

PB002186-2

Figure 3-73. Sector Mark Decode Simplified Logic

3.11.10. Nibble-to-Byte Conversion

Data read from the Media is encoded in TOON code. TOON code represents four bits of binary data (a nibble) as two monoholes in a 9-position TOON cell (refer to the Data Recording Format subsection).

The Binary Registers and Nibble-to-Byte Conversion circuit convert TOON-encoded data to binary data bytes (refer to figure 3-74). As described in the subsection on Data Read Mode, the address of an even monohole (TNC1 and TNC2) directly converts to the two most-significant bits of the equivalent binary nibble. Detection of an even monohole causes LDE to clock the current address through the Even Binary Register, producing the two most-significant bits of the nibble. The odd monohole address converts to the two least-significant bits of the nibble. Detection of an odd monohole causes LDO to clock the then current address through the Odd Binary Register, producing the two least-significant bits. These address are provided to the Binary Registers by the TOON Counter.

The first decoded nibble is gated into one of two four-bit registers in the Nibble-to-Byte Conversion circuit by NIBBLE COUNT 0 from the Nibble Counter. The Binary Registers are then cleared by -RER from the Timing Circuit. The next TOON cell is decoded in the same manner as the first, and is gated into the other register by -NIBBLE COUNT 0.

The two nibbles are gated by READ BYTE or -WRAP TEST and -TRANS ACKN from the registers to the SIA Interface. The first nibble is gated to the four least-significant bits of the bus, and the second to the four most-significant bits, forming a binary data byte. This data byte is then sent from the SIA Interface to Common Memory on the ECC PCA.

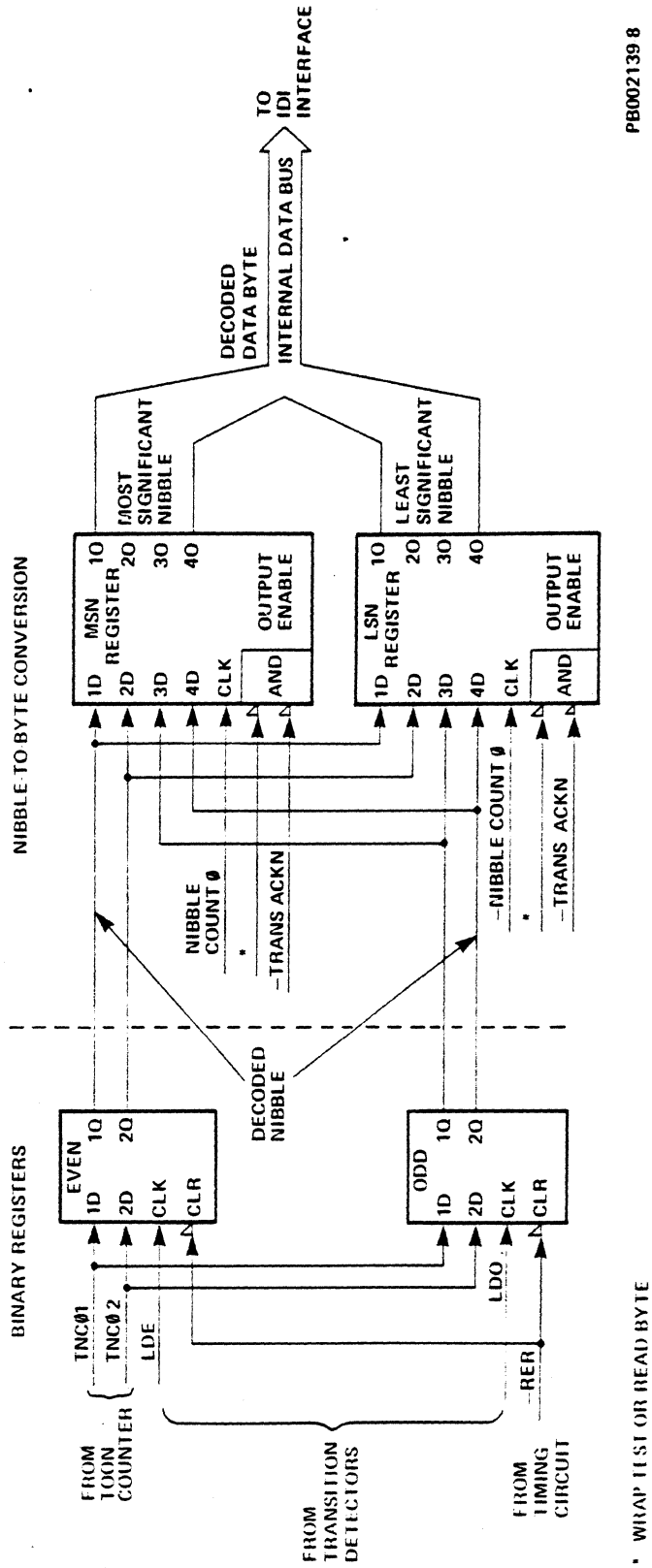


Figure 3-74. TOON Decode Simplified Logic

3.11.11. Interleave Table

The Interleave Table provides an address to the Common Memory (on the ECC PCA) that effectively interleaves data being written in the Media and "de-interleaves" data being read from the Media. Data written in the Media is fetched from a buffer area in Common Memory via the SIA Bus. Data read from the Media is stored in a similar buffer in Common Memory.

The MDS PCA does not include memory for data buffering. The data buffer is implemented in Common Memory.

The MDS PCA processes one sector of data at a time, regardless of buffer size in Common Memory. The LD 1200 uses an 11-bit address to access information within a physical sector. Where the data is stored (Read operation) or retrieved from (Write) in Common Memory is transparent to the LD 1200.

The Interleave Table provides addressing for a one-sector block of Common Memory into which data from the Media is stored or from which it is retrieved. The format used by the LD 1200 to address a one-sector block of Common Memory is shown in table 3-17.

The buffer format shown in table 3-17 provides storage for the User Data Field, Vector Address Field, Postfield, and all associated error correction code (ECC) codewords. Write Protect bytes are written in the Media immediately before the User Data Field. These bytes are used to prevent the Host from accidentally writing over a previously written sector.

Table 3-17. Common Memory Data Buffer Format (One Sector)

RELATIVE ADDRESS RANGE (HEX)	DESCRIPTION	NUMBER OF BYTES (DECIMAL)
0-31	Reserved for use by ICI PCA	5
32	Certify Flag (Diagnostics Only)	1
33-3C	Reserved for use by ICI PCA	10
3D	Write Power Check for Byte Writes (should be 66 hex)	1
3E	User Data Write Protect Byte read from Media	1
3F	Vector Address Write Protect Byte read from Media	1
40	Postfield Write Protect Byte read from Media	1
41	User Data Write Complete Byte read from Media	1
42	Vector Address Write Complete Byte read from Media	1
43	Postfield Write Complete Byte read from Media	1
44-49	Vector Address Field	6
4A-4F	Postfield	6
50-53	Reserved for use by the ICI PCA	4
54-454	User Data Field	1025
455	Reserved for use by ICI PCA	1
456-4B9	ECC for User Data Field	100
4BA-4CD	ECC for Vector Address	20
4CE-4E1	ECC for Postfield	20
500-7FF	Reserved for use by ICI PCA	768

TBL12

In addition to data storage, the buffer format provides 768 bytes per sector for ICI PCA use.

The LD 1200 does not write data in the Media in the same format as it is stored in the buffer. In the Media, data fields are interleaved during Write operations and de-interleaved during Read operations. Interleaving data reduces the possibility of any one Media flaw totally destroying a record or a field. The Vector Address Field and Postfield are most vulnerable to destruction because they are small (6 bytes each). Interleaving the contents of these fields with the contents of the User Data Field, (1025 bytes) spreads a Media flaw across the interleaved fields. In this way, a large flaw appears as a burst of small collectable flaws.

User information in each sector on the disk consists of:

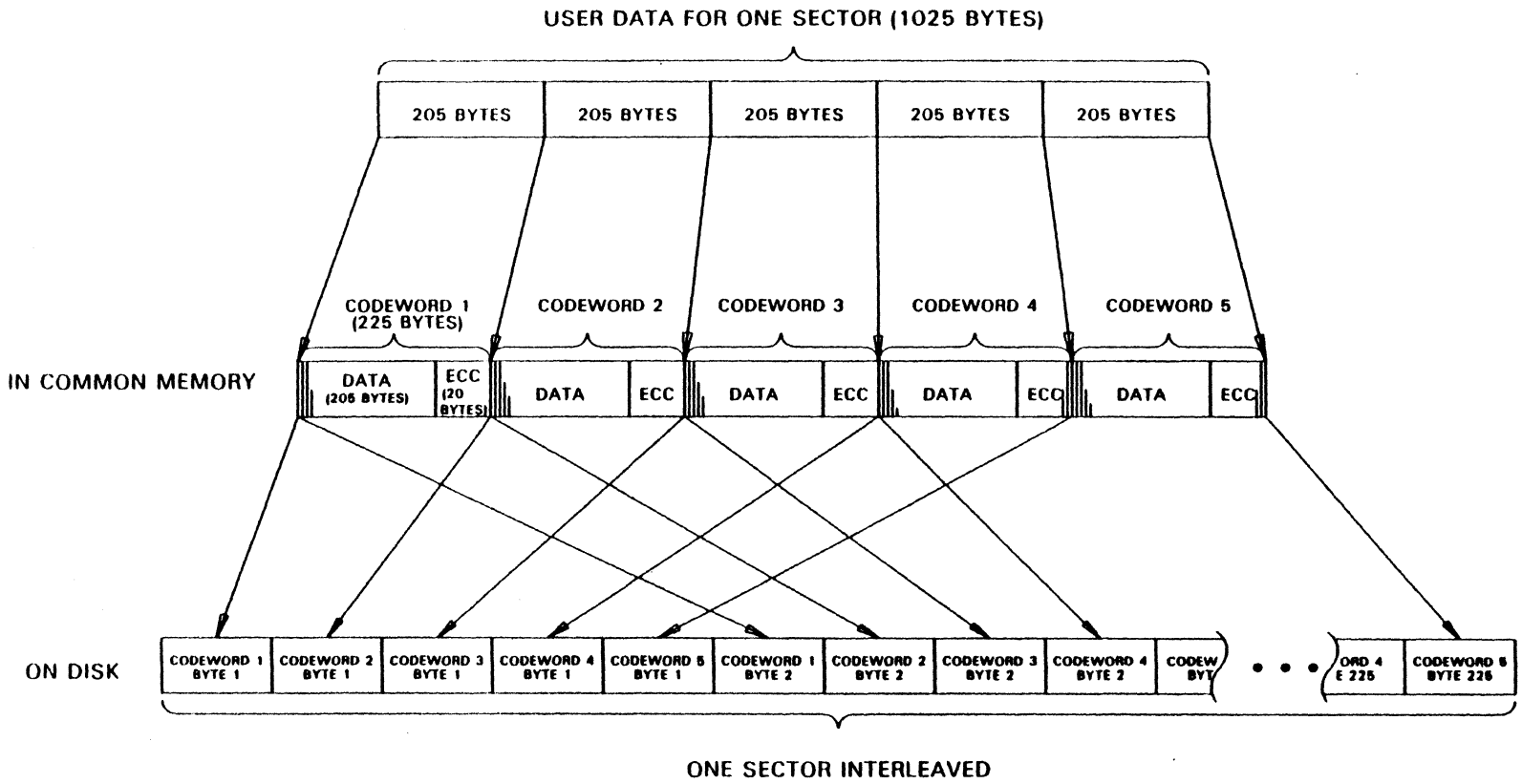
- 3 Write Protect Bytes
- 1025 User Data bytes
- 100 ECC bytes for the user data
- 6 Vector Address bytes
- 20 ECC bytes for the Vector Address
- 6 Postfield bytes
- 20 ECC bytes for the Postfield

The three Write Protect Bytes (one each for the User Data Field, Vector Address Field, and Postfield) are written at the beginning of the sector user data area. A Write Protect Byte indicates that something has been written in the associated field in that sector. The codes used for the Write Protect Bytes (normally 66 hex) are selected by the ICI PCA. If a Write Protect Byte is detected during a Write operation, the LD 1200 hardware immediately inhibits laser write power. If the Read/Write data detection circuitry fails to detect a Write Protect Byte during a Read operation, 00 hex is forced into the associated data buffer location. When data is detected at the Write Protect Byte location, the data buffer is loaded with the value read from the Media. Any nonzero byte value is interpreted as a Write Protect Byte by the ICI PCA. All fields associated with Write Protect Bytes containing all ZEROs are considered empty by the ICI PCA.

The method used to interleave sector data is illustrated in figure 3-75. The 1025 bytes of user data for a sector are divided into 5 equal groups of 205 bytes each. Associated with each group of 205 bytes are 20 bytes of ECC. The 20 ECC bytes are appended to the associated data group to form a 225-byte codeword (5 codewords per sector). The 5 codewords are stored in Common Memory in a group which comprises the 1125-byte data field for one sector. The Vector Address and Postfield fields are also stored in Common Memory with associated ECC bytes appended to them.

During a Write operation, the nibble count from the Nibble Counter is applied to the address inputs of the Interleave Table. The circuit output is the Common Memory address of the first byte to be written in the Media. This address is then routed to Common Memory, via the SIA Interface, and the data byte is transferred to the MDS PCA. In this manner, the data field is fetched from Common Memory and written in the Media in a sequence similar to that shown in figures 3-75 and 3-76. During a Read operation, data read from the Media is stored in Common Memory using the same addressing method, but in the reverse of the Write Interleave sequence (refer to figure 3-77).

The Interleave Table also provides control signals to the Write Logic and TOON Encoder (refer to figure 3-68). The signals POSTFIELD, USER DATA FIELD, and VECT. ADDR. FIELD enable the Write Logic and TOON Encoder to generate the appropriate Write command to write Postfield, User Data Field, or Vector Address Field information in the Media.



NOTES:

1. Not shown here are the Vector Address Field and Postfield, which are interleaved with user data and ECC.
2. Data bytes are not necessarily interleaved in the sequence shown.

ADP17

Figure 3-75. Interleave Theory

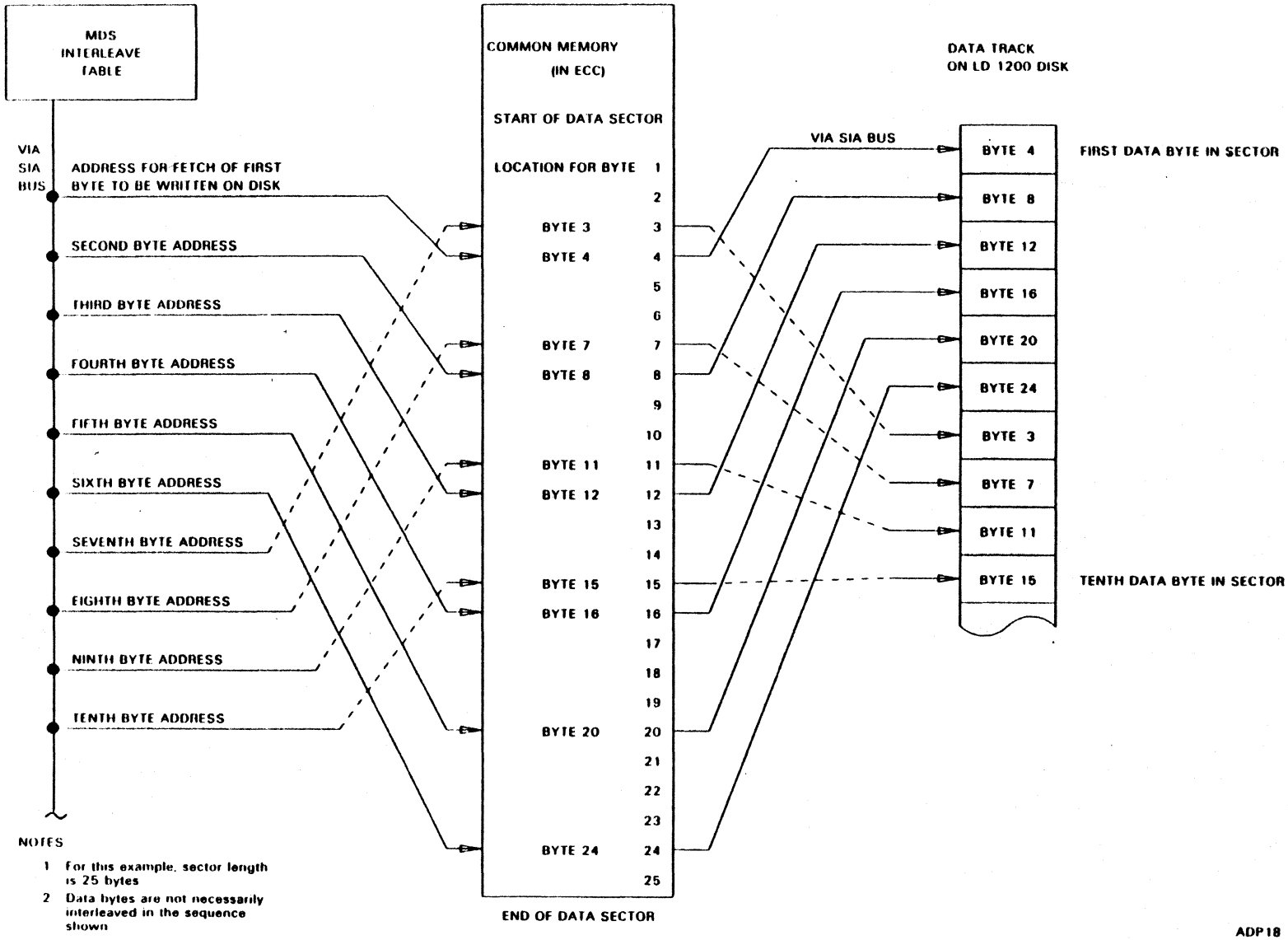


Figure 3-76. Write Interleave Process Example

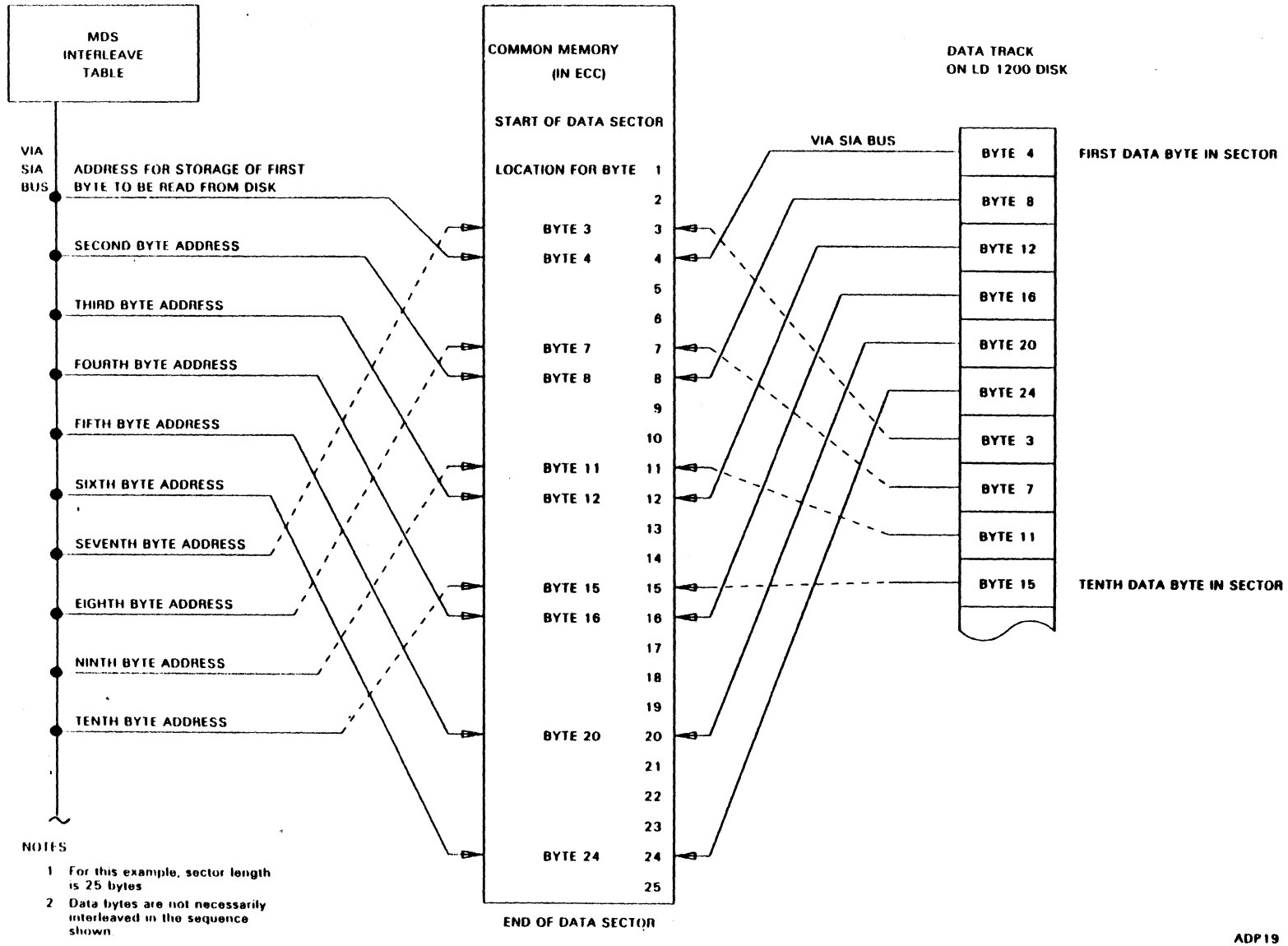


Figure 3-77. Read Interleave Process Example

3.11.12. Write Logic and TOON Encoder

The Write Logic uses commands from the ICI PCA to generate control signals for Read, Write, and Diagnostic operations. The TOON Encoder converts data received from Common Memory to serial write data for the Read/Write Control PCA. Refer to figure 3-78.

At the beginning of the sector, following a command transfer from ICI PCA to MDS PCA, the contents of the Read/Write Command Register in the SIA Interface is loaded into latches in the Write Logic.

NOTE

When a Rewrite operation is required, loading of the latches is inhibited.

Loading of the latches resets the Read/Write Command Register in preparation for the next command transfer from the ICI PCA. From the latches, the commands are input to the Command FPLA. This FPLA generates Read, Write, and Diagnostic control signals from the latched Read/Write Command Register bits. These signals are routed to the remainder of the MDS PCA to control its circuits during Read, Write, and Diagnostic operations.

Data to be written on the disk is received from Common Memory, one byte at a time in binary form (eight bits of data in parallel). The TOON Encoder converts each binary byte into two 9-position TOON cells.

During a Write operation, a byte of binary data is routed through the SIA Interface to a buffer (of flip-flops) in the TOON Encoder (refer to figure 3-78). The data is clocked into the buffer by -INT CLK 3 when TRANS ACKN and WRT XFR ENABLE are high.

The data byte is then input to a multiplexer. The least-significant nibble of the byte (bits 4 through 7) is selected for output from the multiplexer when NIBBLE COUNT 0 is low. The most-significant nibble (bits 0 through 3) is selected when NIBBLE COUNT 0 is high. NIBBLE COUNT 0 alternates between high and low at 9-clock intervals. The selected nibble is output to the encoders at the end of the current TOON cell time when the multiplexer is clocked by TOON PULSE 7. This signal, generated in the TOON Encoder, is a derivative of TNC3 from the TOON Counter. TNC3 is shifted through an eight-bit register by 2CLK. The eighth shift of the register makes TOON PULSE 7 high, defining the end of a TOON cell.

The data nibble from the multiplexer is converted to eight bits of TOON code by the encoders. The TOON code consists of a high bit in an odd bit position, a high bit in an even position, and six low bits.

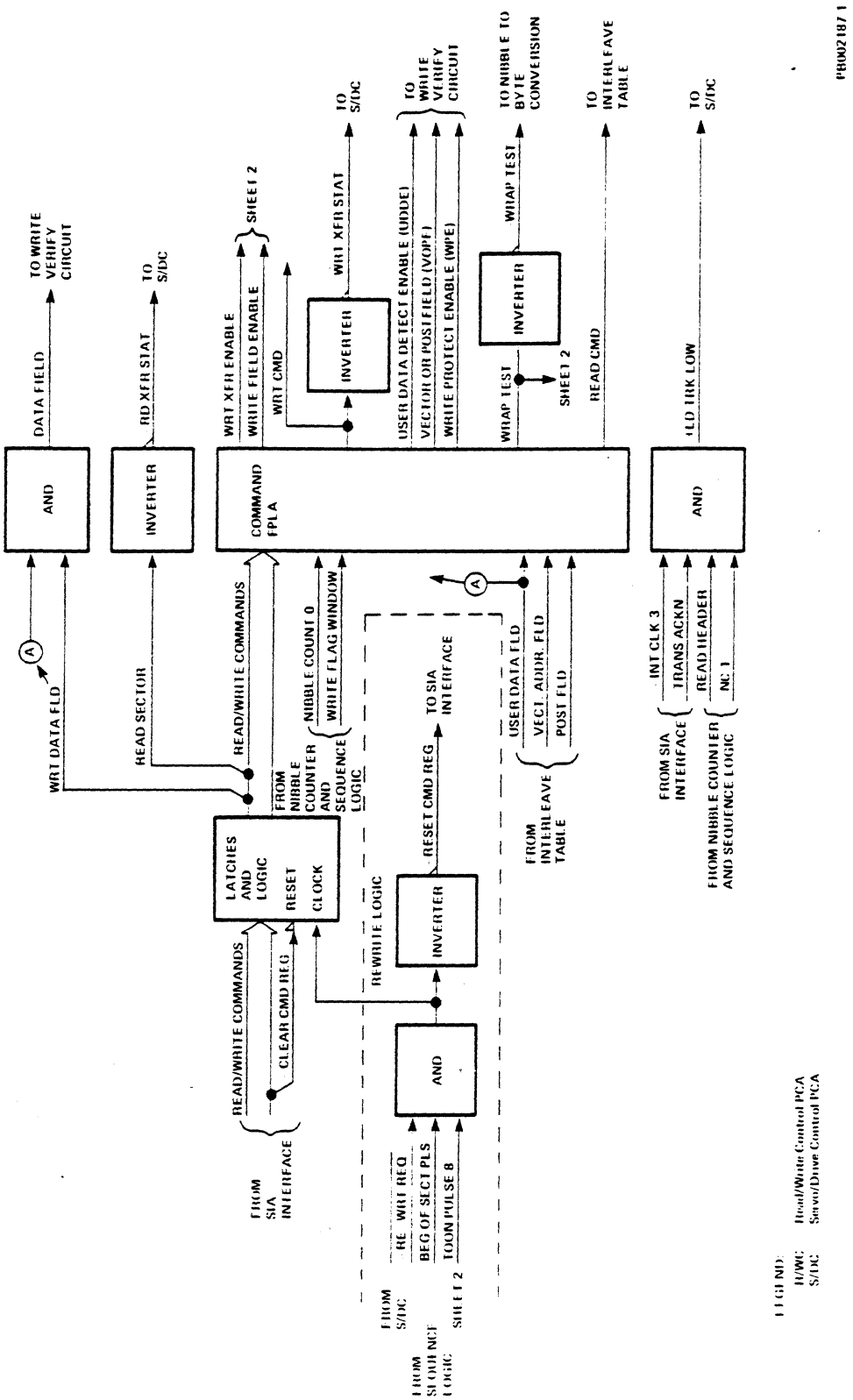


Figure 3-78 Simplified Write Logic and TOON Encoder (Sheet 1 of 2)

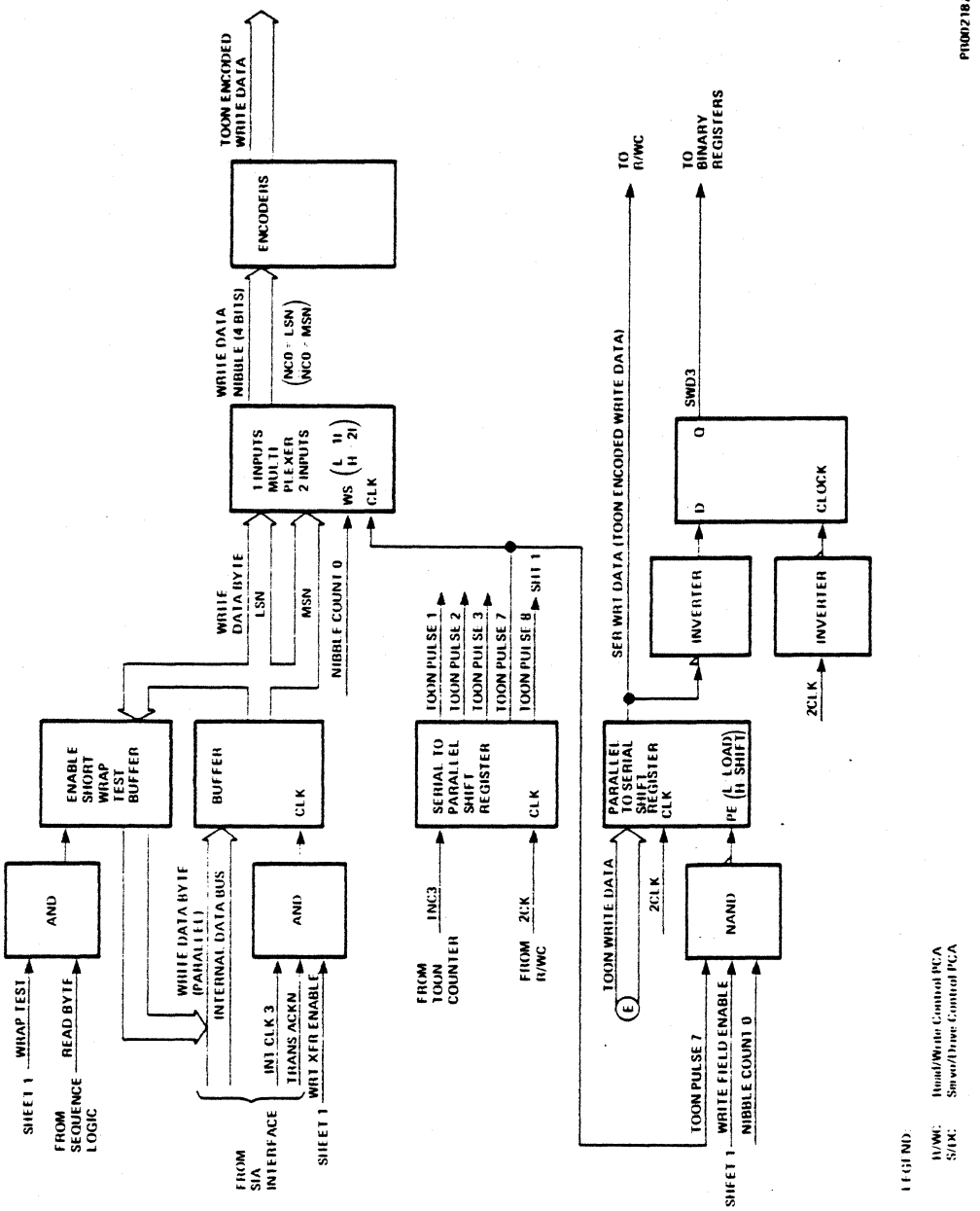


Figure 3-78. Simplified Write Logic and Toon Encoder Sheet 2 of 2)

The TOON encoded data is loaded, in parallel, into a parallel-to-serial shift register by TOON PULSE 7. The register is then enabled for shifting. Eight bits of TOON data, plus one low bit added by TNC3, are serially shifted from the register (as -SER WRT DATA) by -2CLK and are sent to the Read/Write Contrpl PCA. When the TOON cell has been completely shifted out, the register is enabled for the input of the next eight bits of TOON code.

Serial write data is also inverted and input to a flip-flop which is clocked by the complement of 2CLK. The output (SWD3) is delayed serial write data, which is input to the Binary Registers for DRDW.

3.11.13. Rewrite Logic

The Rewrite Logic causes the LD 1200 to attempt the current Write operation again in the next sector (refer to figure 3-78. Rewrite Request (-REWRT REQ) can go low at any time during the sector to request a Rewrite and is cleared at the beginning of the next sector. A Rewrite Request can be caused by any of the following occurrences:

- PLL Error
- DRDW Error
- Sync Error

The occurrence of any other errors cancels the Rewrite Request.

The activation of Rewrite Request prevents the BEG OF SECT PLS signal from clocking the new sector command into the command latches in the Write Logic. At the beginning of the next sector, +BOS ● REWRITE is output to the ECC PCA and the current Write command is attempted again. Rewrite Request also prevents the Read/Write Command Register in the SIA Interface from being cleared at the end of the current sector, thus retaining the command for the next sector after the Rewrite operation.

3.11.14. SIA Interface

The SIA Interface logic enables the MDS PCA to communicate with the SIA Bus. Refer to the Internal Device Interface subsection for a description of SIA signals and protocol.

During the latter two-thirds of each sector, the ICI PCA transfers commands for the next sector to the MDS PCA and reads status pertaining to both the previous and current sectors. A command transfer consists of loading one of two SIA Interface Registers:

- Read/Write Command Register, SIA Port 00 hex
- DRDW Threshold Register, SIA Port 02 hex

The address of the register to be loaded is used by the SIA Interface to route the data from the ICI PCA to the specified destination.

SIA clock, control signals, and Port Address from the ICI PCA are input to the SIA Interface via line receivers (refer to figure 3-79). These signals are routed to the SIA Interface FPLA. This FPLA uses SIA control signals and Port Address Bits 0 and 1 to generate clocks to select and load the Read/Write Command and DRDW Threshold registers.

Control information from the ICI PCA is loaded into SIA Interface Registers to control MDS PCA functions:

- Read/Write Command Register, SIA Port 00 hex – This register is used to specify the type of Read, Write, or Diagnostic operation that is to be performed in the next sector as follows:

SIA BUS BIT	FUNCTION
D0	Write Data Field (and Write Protect Byte)
D1	Write Vector Address Field (and Write Protect Byte)
D2	Write Postfield (and Write Protect Byte)
D3	Diagnostic Read/Write
D4	Read Sector
D5	Clear Read/Write Command
D6	Not Used
D7	Long Wrap Test

Bits 0 through 2 of the register enable the ICI PCA to specify which fields of the sector are to be written. The Postfield can be written only in a sector containing valid data.

Bit 3 enables the MDS hardware for a Short Wrap Test. When Nibble Count 0 is high, a byte of data is transferred from Common Memory to the TOON Encoder Buffer. When Nibble Count 0 goes low, the byte is transferred back to Common Memory. This process continues until the entire sector is shifted into Common Memory. Because Common Memory is addressed by the MDS PCA in an interleave pattern, the data appears scrambled in Common Memory. However, the intelligence in the Internal Controller is able to determine if the bus transfers have been successful.

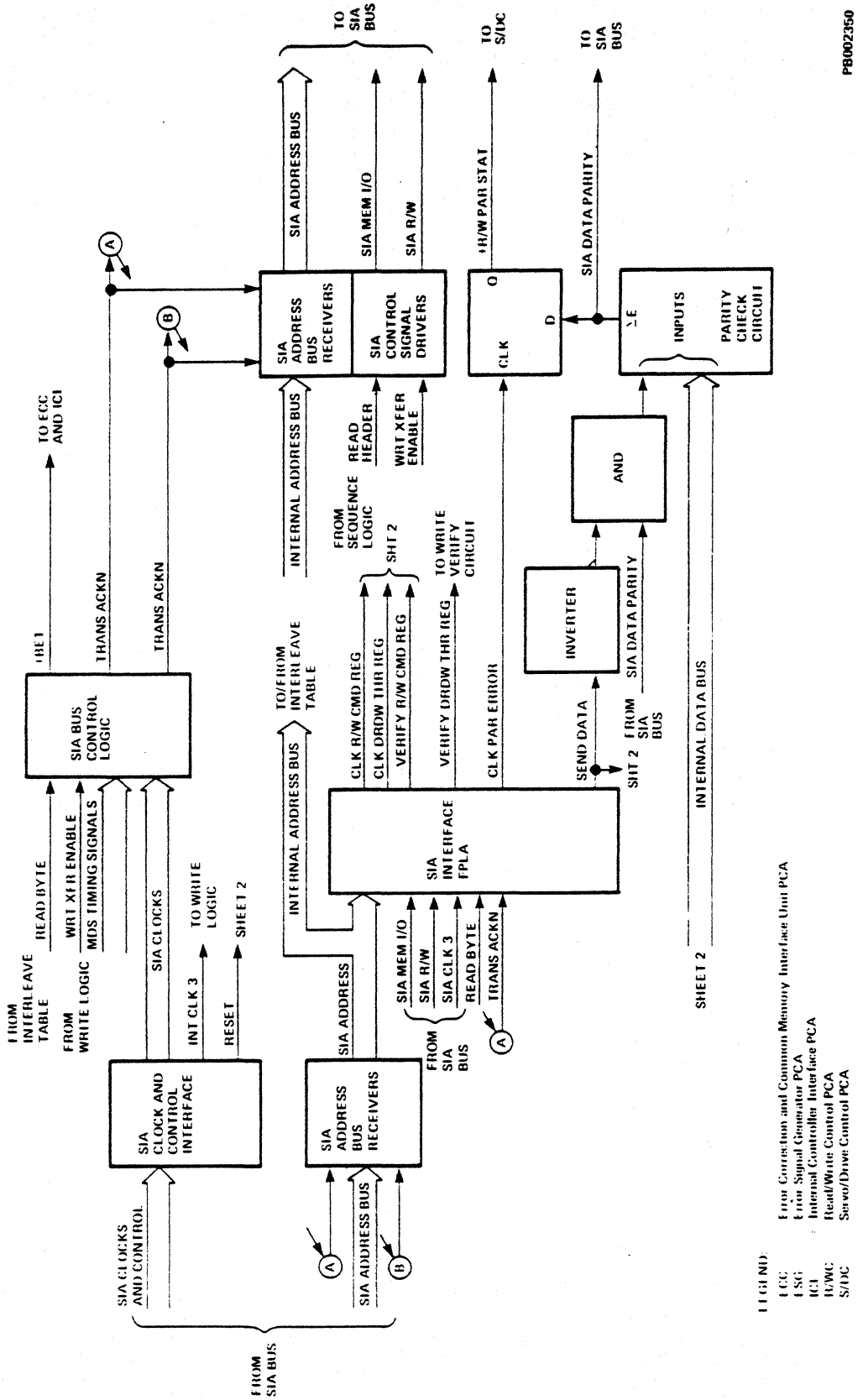
Bit 4 specifies a Read Operation, during which the MDS PCA reads the entire sector and distributes the contents to the Servo/Drive Control PCA and Common Memory. If the ICI PCA issues both a Read and Write command, the MDS PCA performs the Read operation and ignores the Write command.

When high, bit 5 aborts any Read or Write operation in progress, including pseudowrites. This bit should be made high before clearing errors that cause pseudowrites.

Bit 7 enables the MDS hardware for a Long Wrap Test. When a Long Wrap Test command sets Bit 7 high, write data from Common Memory is routed through the TOON Encoder, producing a modified version of serial write data (SWD3). The Long Wrap Test Relay disconnects READ2 (read data from the Media) from the Sample and Hold circuits and substitutes SWD3. The SWD3 pulses are decoded and transferred to Common Memory. As a result of the test, Common Memory should contain the original data plus properly decoded Write Protect Bytes, all in the correct locations. The data does not shift as in the Short Wrap Test.

The Long Wrap Test command is not cleared at the end of each sector. This command must be cleared by a Clear Read/Write Command.

Read/Write commands can be loaded or changed anytime during the Command/Status Window. Near the beginning of each sector (except during a Rewrite), the MDS PCA logs the command received during the previous sector, clears the Read/Write Command Register, and begins execution of the logged commands. The ICI PCA must issue the new commands for the next sector in the Command/Status Window at the end of the current sector. When a new command is not issued, the MDS PCA assumes an idle mode. Once the contents of the Read/Write Command Register are logged, the ICI PCA can not alter the command. When a Rewrite is requested, the contents of this register are not logged and can be changed by the ICI PCA.



LEGEND

ECC	Error Correction and Common Memory Interface Unit PCA
ESG	Error Signal Generator PCA
ICI	Internal Controller Interface PCA
R/WC	Read/Write Control PCA
S/DC	Servo/Drive Control PCA

Figure 3-79. SIA Interface Simplified Logic (Sheet 1 of 2)

- DRDW Threshold Register, SIA Port 02 hex - The ICI PCA loads this register with one plus the maximum number of Direct Read During Write (DRDW) errors that can be allowed to occur in each field (User Data, Vector Address, and Postfield) of a sector, during a Write operation, before the MDS PCA declares a DRDW error. This register is partitioned as follows:

SIA BUS BIT	FUNCTION
D3 through D0	User Data DRDW Threshold
D7 through D4	Postfield and Vector Address DRDW Threshold

When the MDS PCA detects more DRDW errors than are allowed, the Write operation is terminated and (if authorized) a Rewrite operation is attempted in the next sector.

A DRDW error is defined as a byte failure, which may involve as few as one or as many as four monoholes in a byte. A threshold value of zero prevents all writing. A threshold value of one indicates no errors are allowed.

The DRDW value is also used to determine whether a given sector is empty or has been written in previously. The MDS PCA declares the presence of data in a sector only when the number of properly decoded bytes from the Media equals or exceeds the DRDW threshold.

During a data transfer from the Media to Common Memory, the MDS PCA must have control of the SIA Bus when a byte is ready for transmission. To gain control, READ BYTE (from the Interleave Table) goes high. When SIA CLK 3 (from the SIA Bus) goes high, +BE1 (Bus Enable Out) goes low giving the MDS PCA control of the SIA Bus (refer to +BE1 description in the subsection on Interface Signals). At SIA CLK 2, TRANS ACKN (Transaction Acknowledged) goes high, enabling the SIA Address Bus drivers for the transfer of the Common Memory Address from the Interleave Table. READ BYTE and TRANS ACKN are applied to the SIA Interface FPLA, causing SEND DATA to be generated, enabling the SIA Data Bus drivers. As data is read from the Media, it is sent to Common Memory by these drivers.

During a Write operation, WRT XFR ENABLE goes high, giving the MDS PCA control of the SIA Bus, as previously described. TRANS ACKN enables the SIA Address Bus drivers to send the Common Memory Address to the ECC PCA. READ BYTE is low during a Write operation, making SEND DATA low. SEND DATA low enables the SIA Data Bus Receivers to accept a byte of data from Common Memory and route it to the TOON Encoder.

3.11.15. Pre-PIP Detection

This circuit generates Write Protect and Missing Data Field Statuses. During a Write operation, a Write Protect Byte for the type of field being written (User Data, Vector Address, or Postfield) is written before the Data Field (refer to figure 3-91 in the subsection on Data Recording Format). A hole burned in the Media at a specific monohole position spreads to include adjacent positions. Using differential detection, a monohole can actually be sensed before reaching the monohole position at which it was burned. Therefore, shortly before a write protect byte is written, Laser Diode read power is turned on. If there is already a Write Protect Byte in the field where one is

to be written, it is detected by the Sample and Hold circuitry and Level Detect signal -(S4>S2) is sent to the Pre-PIP Detection circuit. This circuit generates +WRT PROT STAT high to the Servo/Drive Control PCA, enabling it to shut down Laser Diode write power before the write protect byte can be overwritten.

When a Postfield is to be written, the sector must already contain user data, as indicated by the presence of a User Data Write Protect Byte. In this case, the Pre-PIP Detection circuit is allowed to look for a Data Level signal only during the User Data Write Protect Byte field (UDDE from the Write Logic goes high). If the Write Protect Byte is not detected, the Pre-PIP Detection circuit sends +MISS DATA FIELD high to the Servo/Drive Control PCA, enabling it to shut down Laser Diode Write power before the Postfield Write Protect Byte can be written.

3.11.16. Certify Flag Detection

When the presence of data is detected in the Certify Flag Byte (the LEVEL DETECT signal goes high) this circuit generates +CERTIFY FLAG high.

3.11.17. Data Detection Circuit

This circuit informs the Servo/Drive Control PCA when it is determined that there is data in a sector. A preset number of monoholes must be detected in a sector before it can be identified as containing data. This value is loaded into the DRDW Threshold Register by the ICI PCA (refer to the subsection on SIA Interface).

At the beginning of each sector, the value from the DRDW Threshold Register is preset into the Data Detect Threshold Counter. The counter is enabled during the User Data and Vector Address Fields. Each time a data monohole is detected, the counter is decremented by one. When the count reaches zero, DATA DETECT high is sent to the Servo/Drive Control PCA, indicating that data is contained in the sector. DATA DETECT is reported to the ICI PCA to enable it to determine whether a sector contains data without performing a Read operation.

3.11.18. Write Verify Circuit

The Write Verify Circuit generates a DRDW Error status when a properly formed monohole is not detected after an attempt has been made to write one.

There are two threshold counters in the Write Verify Circuit: User Data DRDW Threshold Counter and Vector Address or Postfield Threshold Counter. Data to initialize these counters is loaded from the ICI PCA into the DRDW Threshold Register (in the SIA Interface) before the end of the sector. At the beginning of the next sector, the threshold data is loaded into the threshold counters.

At the beginning of each byte written, one of the two threshold counters or the Write Protect DRDW Error AND gate is enabled by the associated enable signal from the Write Logic (refer to figure 3-80), as follows:

- When a write protect byte is written, WPE enables the Write Protect AND gate.
- When a user data byte is written, DATA FIELD enables the User Data DRDW Threshold Counter.
- When a Vector Address Field or Postfield byte is written, VOPE enables the Vector Address or Postfield DRDW Threshold Counter.

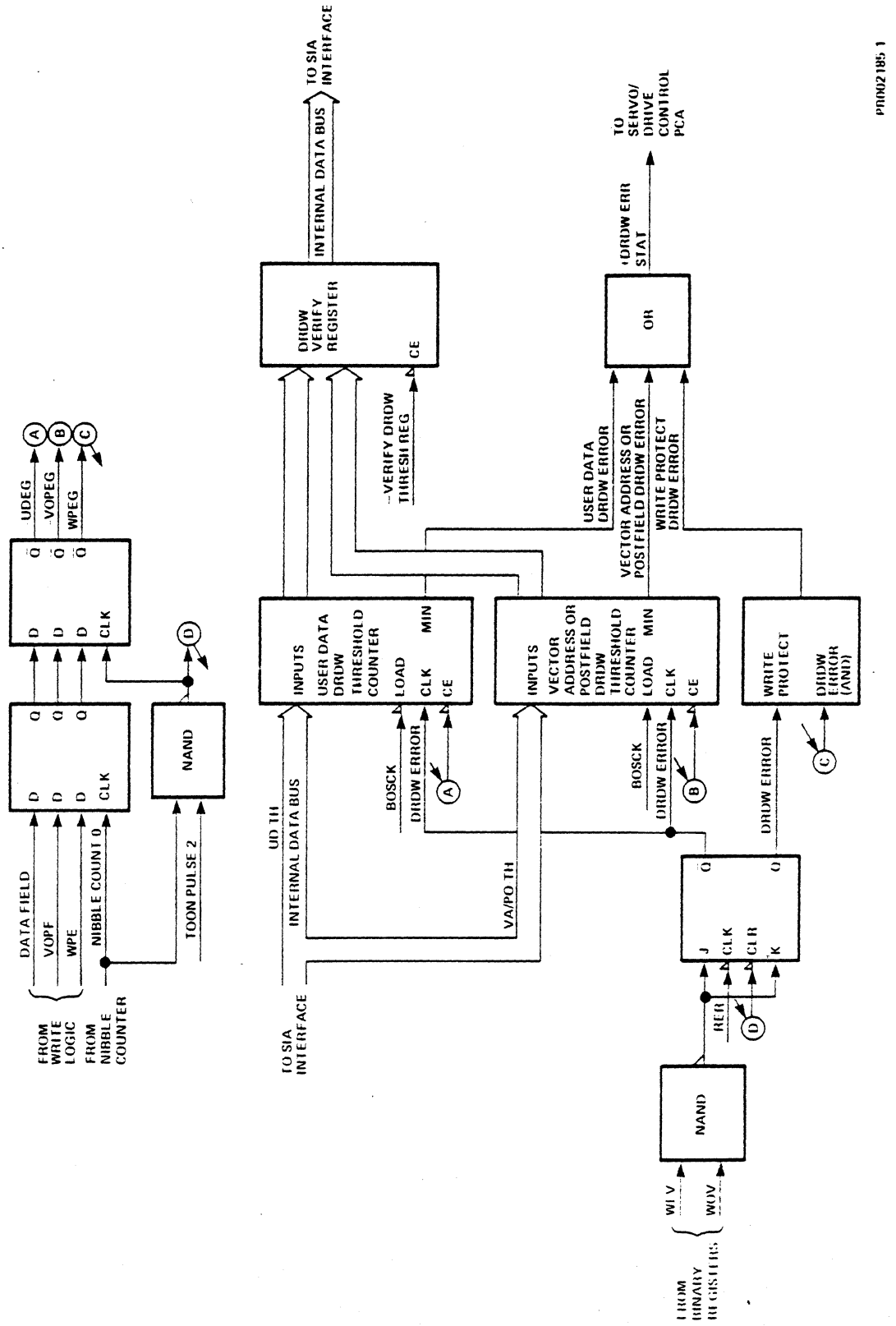


Figure 3-80 Write Verify Circuit Simplified Logic

WEV and WOV are applied to a NAND gate. If both the even and odd PIPs in a nibble are detected, the NAND gate disables the clock to the associated threshold counter, and the input to the Write Protect AND gate is low. If a PIP has not been detected, the associated signal (WEV or WOV) causes the output of the NAND gate to go high. This places a high level at both the J- and K- inputs of DRDW Error flip-flop. When the flip-flop is clocked by -RER at the beginning of the next nibble, the outputs toggle, generating a clock pulse to the enabled threshold counter and a high input to the Write Protect AND gate. Each time a User Data, Vector Address, or Postfield DRDW error is detected, the enabled counter is decremented by one. When the count reaches zero, +DRDW ERR STAT high is sent to the Servo/Drive Control PCA, indicating a Write error.

If the Write Protect AND gate is enabled, a missing PIP generates +DRDW ERR STAT high at the beginning of the next nibble. The DRDW Error flip-flop is cleared at the beginning of each byte.

3.11.19. Wobble Byte Verification

This circuit verifies that the wobble bytes have been properly read from the Media (refer to figure 3-81). As each nibble of the wobble bytes is decoded by the Binary Registers, it is input to the register in the Wobble Byte Verification circuit. WOBBLE ENABLE from the Sequence Logic is input to the register to verify that the wobble nibble has been decoded at the proper time. The register is clocked by TOON PULSE 0 at the beginning of the next nibble. The outputs of the register provide address inputs to a PROM. When eight properly decoded wobble nibbles have been recognized by the PROM, a high signal is sent to the Wobble Qualifier Flip-Flop. The flip-flop is clocked at the beginning of the next nibble, which sends +WBBL QUAL PLS (Wobble Qualifier Pulse) high to the Error Signal Generator PCA.

The Error Signal Generator PCA sends a Wobble Pulse Feedback (+WBBL PLS FEEDBK) to the Wobble Byte Verification circuit. This signal presets a down counter with a threshold value for the generation of a Wobble Error Status. This counter is clocked at the beginning of each sector. If it is not preset by the occurrence of a Wobble Pulse Feedback signal during each sector, the counter is decremented by -BOSCK (Beginning of Sector Clock) to zero. When the READ HEADER signal goes high, shortly after the wobble bytes are read, WES STATUS (Wobble Error Status) high is sent to the Servo/Drive Control PCA.

The complement of the Wobble Qualifier Pulse Signal is input to a flip-flop. The flip-flop is clocked by the complement of the Wobble Pulse Feedback signal. If the Wobble Qualifier Pulse and Wobble Pulse Feedback signals coincide, the output of the flip-flop keeps the Wobble Error Status signal low, indicating no Wobble Error. This circuit checks wobble pulse timing.

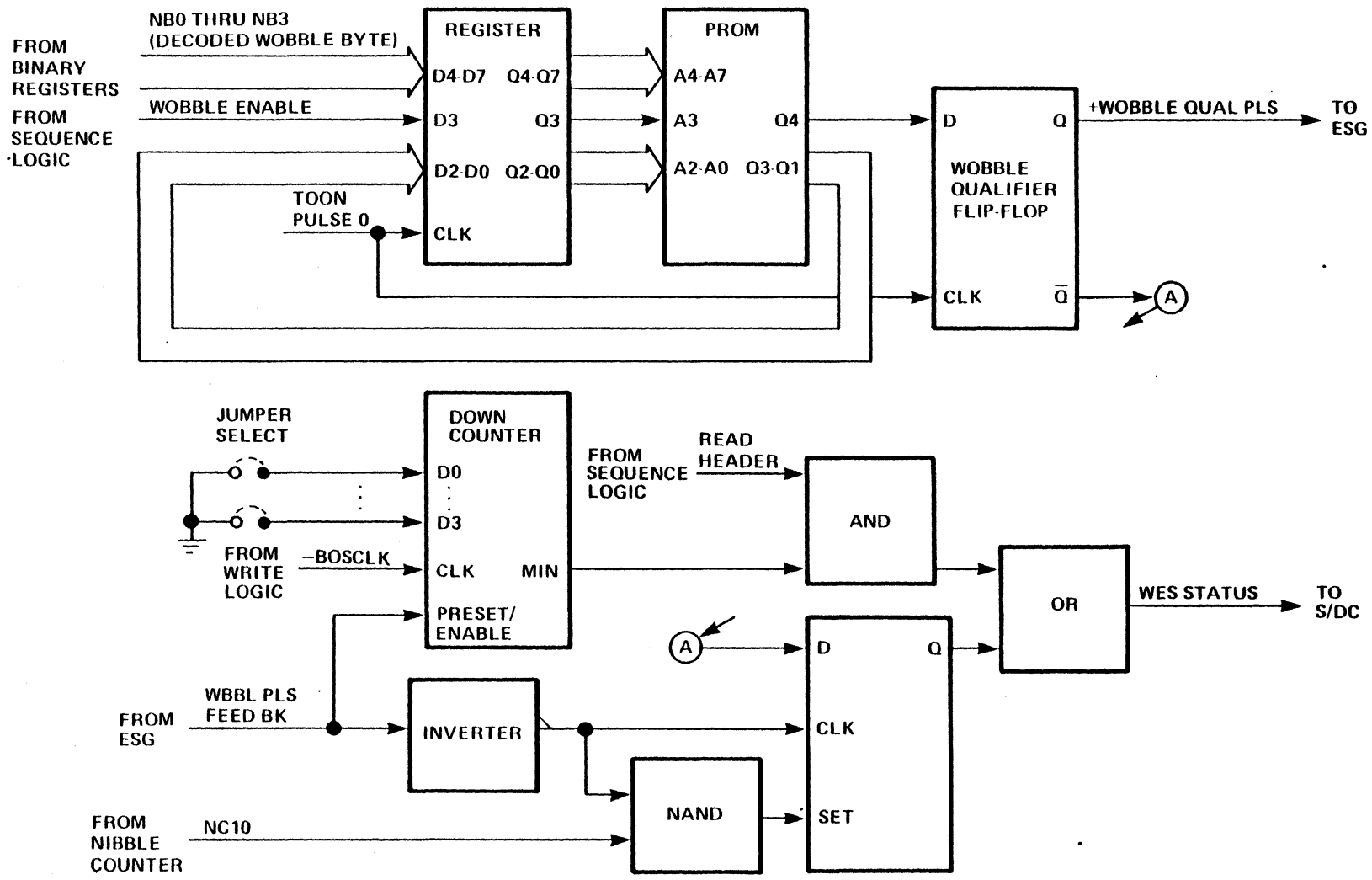


Figure 3-81. Wobble Byte Verification Simplified Logic

3.12. CARRIAGE

The Carriage is the largest moving mass in the servo system. In many ways, the Carriage is similar to the actuators in magnetic disk drives. As in these drives, the Carriage is capable of movement in only the radial direction, in relation to the Media disk, and is Driven electromagnetically by a voice-coil motor. It is through the actuation of the Carriage that long Seeks, from the inner to the outer tracks of the disk, are possible.

Physically, the Carriage consists of a Carriage Body, on which are mounted:

- Fine Servo Motor, the only other component of the LD 1200 capable of independent directed movement
- Position Sensor
- Quad Detector
- Carriage Electronics PCA
- Laser Pen
- Optics

Functionally, the Carriage consists of three interdependent systems: (refer to figure 3-82)

- Optical
- Carriage Electronics
- Electromechanical

These systems are described in the following subsections.

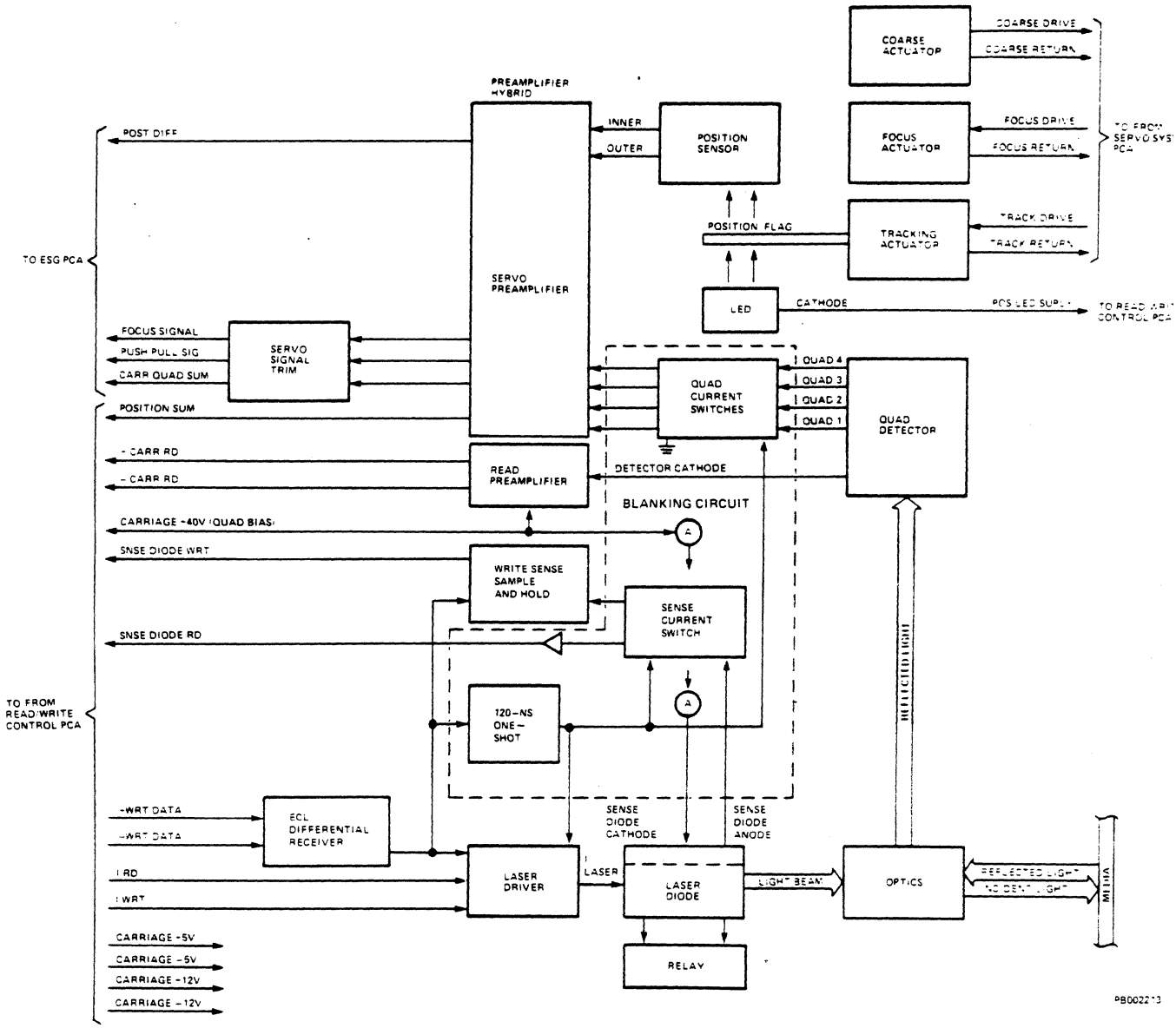


Figure 3-82. Carriage Block Diagram

3.12.1. Interface Signals

The Carriage interfaces with the remainder of the LD 1200 using the following signals (refer to figure 3-82):

POST DIFF (Position Difference)

This signal is output to the Error Signal Generator (ESG) PCA. It is generated by the Position Sensor on the Carriage. This signal indicates the relative position of the Fine Servo Motor (FSM) with respect to the Carriage Body, in a radial direction.

FOCUS SIGNAL

This signal is output to the ESG PCA. It is derived from the output of the Quad Detector on the Carriage. This signal indicates the distance between the actual and desired focus points. It is used to Drive the Focus Actuator to the point where the light beam from the Laser Diode is focussed on the sensitive layer of the Media.

PUSH PULL SIG (Push-Pull Signal)

This signal is output to the ESG PCA. It is an analog error signal derived from the output of the Quad Detector on the Carriage. This signal indicates the relative shift of the light beam with respect to a track center. It serves as the error signal to Drive the Tracking Actuator back to the center region.

CARR QUAD SUM (Carrier Quad Sum)

This signal is output to the Servo Systems, Read/Write Control and ESG PCAs. It is derived from the output of the Quad Detector on the Carriage. This signal indicates the total light intensity received at the Quad Detector. The Carriage Quad Sum signal is used for the following:

- Provide gain control voltage to the ESG PCA
- Provide Quad Low Status
- Provide Quad High Status to the Power Control Loop

POSITION SUM

This signal is output to the Read/Write Control (R/WC) PCA. It is generated by the Position Sensor on the Carriage. This signal indicates the total intensity of the light striking the split detector (duo-diode) in the Position Sensor. It is used to control the light intensity of the Position Sensor LED and thereby control the gain of the Position Difference signal.

+CARR RD and -CARR RD (Carriage Read Signals)

These differential signals are output to the R/WC PCA. They carry read data from the Media. Read data includes header and user data, write PIP readback (Write Verification signal), and disk clock signals.

CARRIAGE +40V (Quad Detector Bias)

This signal is generated by the Power Supply and distributed to the Carriage by the R/WC PCA. It provides the bias voltage for the Quad Detector.

SNSE DIODE RD (Sense Diode Read)

This signal is output to the R/WC PCA. It is a voltage which represents Laser Diode output power during the read mode.

SNSE DIODE WRT (Sense Diode Write)

This signal is output to the R/WC PCA. It is a sampled and held voltage which represents Laser Diode output power during the write mode.

I RD (Read Current)

This signal is generated by the R/WC PCA. It provides read current to the Laser Diode.

I WRT (Write Current)

This signal is generated by the R/WC PCA. It provides write current to the Laser Diode.

+WRT DATA and -WRT DATA (Write Data Signals)

These differential ECL signals are generated by the R/WC PCA. They carry TOON-encoded write data to be recorded in the Media.

CARRIAGE +5V

This signal is an operating voltage from the R/WC PCA.

CARRIAGE -5V

This signal is an operating voltage from the R/WC PCA.

CARRIAGE +12V

This signal is an operating voltage from the R/WC PCA.

CARRIAGE -12V

This signal is an operating voltage from the R/WC PCA.

COARSE DRIVE

This signal is generated by the power amplifier on the Servo Systems (SS) PCA. It provides Drive current for the Coarse Actuator.

COARSE RETURN

This signal is output to the SS PCA. It provides the return path for the Coarse Actuator, carrying current feedback to the Coarse Servo Loop.

FOCUS DRIVE

This signal is generated by the power amplifier on the SS PCA. It provides Drive current for the Focus Actuator function of the FSM.

FOCUS RETURN

This signal is output to the SS PCA. It provides the return path for the Focus Actuator, carrying current feedback to the Focus Servo Loop.

TRACK DRIVE (Tracking Drive)

This signal is generated by the power amplifier on the SS PCA. It provides Drive current for the Tracking Actuator function of the FSM.

TRACK RETURN (Tracking Return)

This signal is output to the SS PCA. It provides the return path for the Tracking Actuator, carrying current feedback to the Tracking Servo Loop.

POS LED SUPLY (Position LED Supply)

This signal is generated by the R/WC PCA. It supplies the analog voltage to Drive the LED which is the light source for the Position Sensor.

3.12.2. Optical System

The Carriage Optical System consists of the following components (refer to figure 3-83):

- Laser Pen (collimator pen), consisting of the following components:
  - Gain Guided semiconductor (Al Ga As) laser diode
  - Collimation objective
  - Cylindrical lens
  - Photodiode sensor

  The output of the Laser Pen is a collimated beam of light, which produces a maximum of 20 milliwatts of write power at a wavelength of from 800 to 840 nanometers. Collimation is within 0.3 milliradians. Radiation is linearly polarized light.

- 45 Degree Mirror – glass substrate with a multilayer coating optimized for an incident angle of 45 degrees.

- Polarizing Beamsplitter – reflects or transmits light, depending on the direction in which the light is polarized.

- Quarter-wave Retarder – changes linearly polarized light to circularly polarized light and circularly polarized light to linear.

- Objective Lens – three-element Rodenstock Lens that focuses the beam from the laser to a 1-micrometer spot. The Objective Lens has an F number of 0.96, which equals a numerical aperture of 0.52 and focal length of 4.13 millimeters. The lens system is mounted in the Fine Servo Motor.

- Bifocal Lens – this lens has two different radii. After passing through the lens, the light beam is astigmatized, producing two focal lines.

- Quad Detector - four-element quadrant detector, consisting of four light sensing semiconductor diodes. These diodes are used to detect focus, tracking, total laser power, read data, and clock signals.

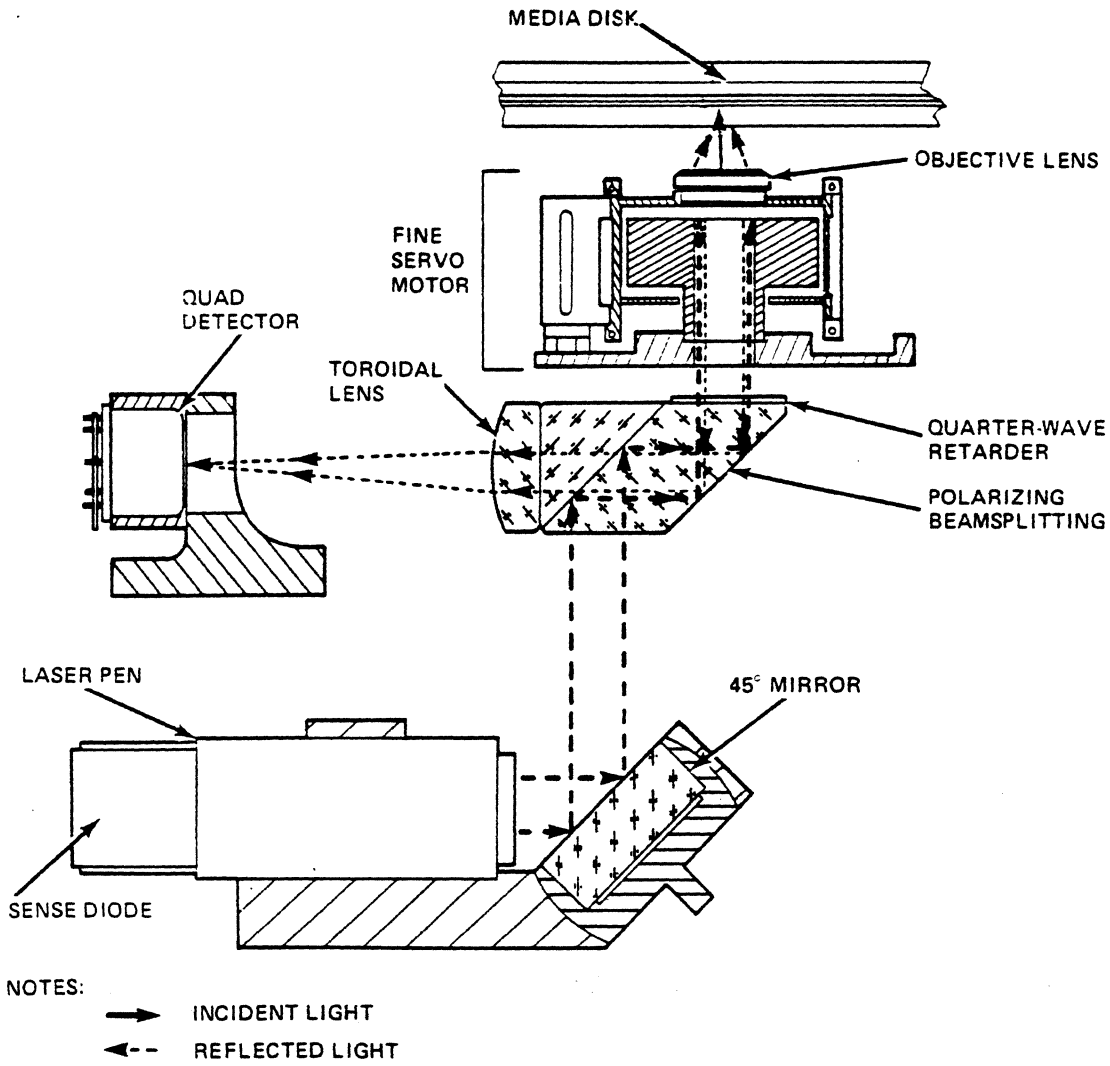


Figure 3-83. Carriage Optical System

The Laser Pen provides the light source beam to write data in and read data from the Media. Serial write data signals from the Read/Write Control PCA turn on laser write current, bringing the power of the laser beam up to the level where a hole can be melted in the sensitive layer of the Media. The polarized laser beam is collimated by the Laser Pen. This beam is transmitted to the Polarizing Beamsplitter, which deflects it 90° and transmits the light up through the Quarter-wave Retarder. The Quarter-wave Retarder converts the beam from linearly polarized light, to circularly polarized light which is rotated 45°. The circularly polarized light beam is projected up through the Objective Lens, which focuses it onto the sensitive layer of the Media.

When the beam is at the write power level, the light melts a hole in the sensitive layer of the Media.

When the laser beam is at the read power level, the light is reflected back from the sensitive layer of the Media, through the Objective Lens, to the Quarter-wave Retarder. The Quarter-wave Retarder rotates the polarization of the light another 45°, making it linear, but 90° out of phase with the incident light. This linearly polarized light is transmitted to the Polarizing Beamsplitter. Because of the orientation of the polarized light, the Polarizing Beamsplitter passes the beam through the Spacer and Bifocal Lens to the Quad Detector. The Quad Detector converts the reflected light into electrical signals which contain the information read from the Media.

3.12.3. Electronics System

The Carriage Electronics System consists of the following components (refer to figure 3-82):

- ECL Differential Receiver
- Laser Driver
- Laser Diode (part of both the Optical and Electronics Systems)
- Sense Diode
- Relay
- Blanking Circuit
- Quad Detector (part of both the Optical and Electronics Systems)
- Write Sense Sample and Hold
- Position Sensor, Position Flag, and LED
- Servo Preamplifier
- Servo Signal Trim
- Read Preamplifier

The Electronics System is implemented on the Carriage Electronics PCA, except for the Laser, Sense Diode, Quad Detector, Position Sensor, Position Flag, and associated LED.

3.12.3.1. ECL Differential Receiver

This circuit receives differential write data signals from the Read/Write Control PCA and routes write data to the Laser Driver, Write Sense Sample and Hold, and 120-ns One-Shot circuits.

3.12.3.2. Laser Driver

During a Write operation, this circuit modulates the output of the Laser Diode with write data. Write current, controlled by the Read/Write Control PCA, is enabled to the Laser Diode by serial Write Data pulses. The write current causes the laser to emit coherent light which melts a hole in the sensitive layer of the Media.

During a Read operation, read current, from the Read/Write Control PCA, is supplied to the Laser Diode. The read current causes the laser to emit coherent light at the read power level, which is reflected back through the Optical System carrying information read from the disk.

3.12.3.3. Laser Diode

During a Write operation, the Laser Diode is Driven by write current from the Laser Driver to emit coherent light of sufficient power to melt a hole in the sensitive layer of the Media. When the laser is not writing, it is Driven by read current from the Read/Write Control PCA to emit coherent light at the read power level, enabling data and servo information to be read from the Media.

3.12.3.4. Sense Diode

The Sense Diode is located in the Laser Pen behind the Laser Diode. This location enables the Sense Diode to monitor laser emissions which are proportional to those directed through the optical system to the Media. Light from the Laser Diode is converted to electrical signals, which indicate relative power output, by the Sense Diode. These signals (Sense Diode Read and Sense Diode Write) are sent via the Blanking Circuit to the R/WC PCA to control the Power Control Loop.

3.12.3.5. Relay

The relay is connected across the terminals of the LaserDiode to protect the laser from static when no power is applied to the Carriage.

3.12.3.6. Blanking Circuit

The Blanking Circuit eliminates the effect of far field shift on the Quad Detector during periods of high laser power (writing) and provides isolation for read and write sense currents. As shown in figure 3-82, this circuit is composed of the following:

120-ns One-Shot - During a Write operation, the retriggerable one-shot circuit provides a pulse to the Quad and Sense Current Switches which enables them to switch currents from the Quad Detector and Sense Diode to ground. The duration of the one-shot pulse is long enough to blank write pulse transients from the Quad Detector and Sense photodiodes before returning the current switches to the read mode.

Quad Current Switches - During a Write operation, these switches route the outputs of the Quad Detector photodiodes to ground, preventing write pulse transients from entering the Read Channel. This circuit also provides isolation to keep voltage changes on the photodiodes to a minimum and to prevent Blanking Circuit switching transients from entering the Read Channel.

Sense Current Switch - During a Write operation, this circuit routes sense diode current to the Write Sense Sample and Hold circuit for generation of the Sense Diode Write signal for the Read/Write Control PCA. The Sense Current Switch also isolates Blanking Circuit switching transients from the Sense Diode.

3.12.3.7. Quad Detector

The Quad Detector consists of four photodiodes arranged in a four-quadrant manner, as shown in figure 3-84. These diodes are used to derive the Focus Signal, Push-Pull Signal, Low-frequency Quad Sum Signal, and Read Signal (containing data and clock signals).

The LD 1200 focusing system is built around the Bifocal Lens. Light reflected from the Media is passed through the Objective and Bifocal Lenses, producing an astigmatic effect (refer to figure 3-84, part a). Rather than producing a single focal point, these lenses produce two focal lines. The focal lines are perpendicular to one another. Halfway between the focal lines, the lenses produce a nearly circular spot. When the Optical System is in focus, this spot is centered on the Quad Detector, producing equal outputs from all four diodes. As shown in figure 3-84, part a, the Focus Signal electronics produces an in-focus signal of zero. When the Objective Lens is too close to the Media to be in focus, a positive signal proportional to the deviation from focus is generated. A negative signal indicates the Objective Lens is too far from the Media to be in focus.

The tracking system is based on detecting the difference in intensity of the light falling on the two sides of the Quad Detector. As shown in figure 3-84, part b, the zero order defraction pattern created by the light reflected from the Media maintains the same intensity as tracks are crossed. The first order defraction pattern changes intensity from side to side as tracks are crossed. As a result, the intensity of light (zero order plus first order patterns) hitting each side of the Quad Detector changes as tracks are crossed, resulting in a tracking error signal.

Imperfections in the mechanical aspects of the LD 1200 cause the Media track to wander away from the on-track position of the Carriage. As the Media moves off-track, the intensity of the reflected light changes a proportional amount (refer to figure 3-84, part b). The change in intensity indicates the amount of deviation from track center. The detector quadrants detecting the change in intensity indicate the direction of the deviation from track center. This information is used to generate the Push-Pull signal which is sent to the ESG PCA via the Servo Signal Trim circuit. The ESG PCA generates a tracking error signal which is used by the Tracking Servo Loop to keep the Carriage on track.

NOTE

The spot of reflected light falling on the face of the Quad Detector does not move from the center position, except under the following conditions:

- The components of the Optical System or the Quad Detector are out of alignment.
- The FSM is extended (i.e., displaced) from its zero axis position relative to the Coarse Linear Actuator. For example, during a Seek operation, the FSM leads the Coarse Linear Actuator until the actuator catches up.

The read signal from the Media (containing data and clock information) is derived by detecting changes in Quad Detector bias current through monitoring of the +40-volt supply (refer to figure

3-84, part c). A monohole in the Media (representing data) causes a drop in the reflected light received by the Quad Detector. The resulting change in the current drawn by the Quad Detector is detected by the monitor in the Read Preamplifier, which generates the differential read signal for transmission to the R/WC PCA.

The outputs of all four Quad Detector diodes are summed to create the Quad Sum signal. This signal is used to normalize all other servo signals generated by the Quad Detector and to provide a "Laser-on" flag for the ESG PCA.

3.12.3.8. Write Sense Sample and Hold

Serial Write Data pulses from the ECL Differential Receiver enable this circuit to sample and hold sense diode current, which indicates Laser Diode power output. After four write pulses, the value held is sampled by the Read/Write Control PCA, which uses it to adjust laser write power.

3.12.3.9. Position Sensor, Position Flag, and LED

The Position Sensor indicates the position of the Fine Servo Motor relative to the Coarse Actuator. The sensor consists of a LED, Position Flag, and Sensor. As shown in figure 3-82, the LED and Sensor are mounted opposite each other on the Carriage Body. The flag is mounted between the LED and Sensor and is attached to the movable FSM actuator.

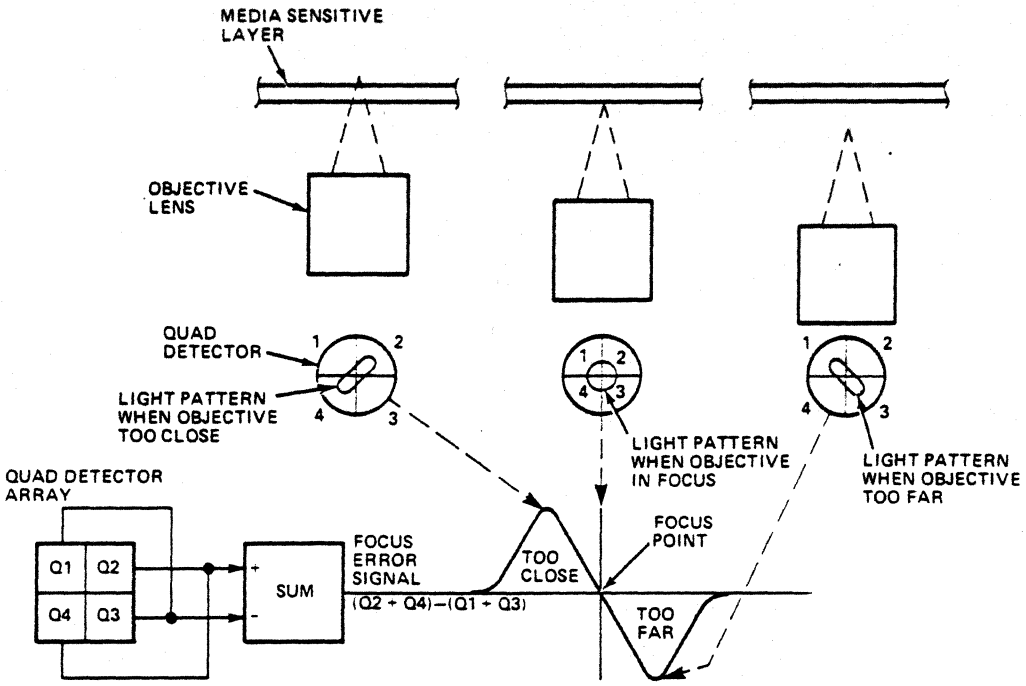
The LED is used as a light source. The Sensor is a dual photodiode, which is used to detect the light from the LED. When the FSM actuator is at the center (zero) position relative, to the Coarse Actuator, the light from the LED shines through the vertical slot in the Position Flag and illuminates equally both diodes of the Sensor. As the FSM actuator moves in either direction, the flag attached to it moves. The flag blocks the light from the LED allowing more light to fall on one of the two Sensor diodes. The difference in diode illumination generates an error signal which is proportional to the deviation of the FSM from the center position. This error signal causes the Coarse Linear Actuator to follow the movement of the FSM.

3.12.3.10. Servo Preamplifier

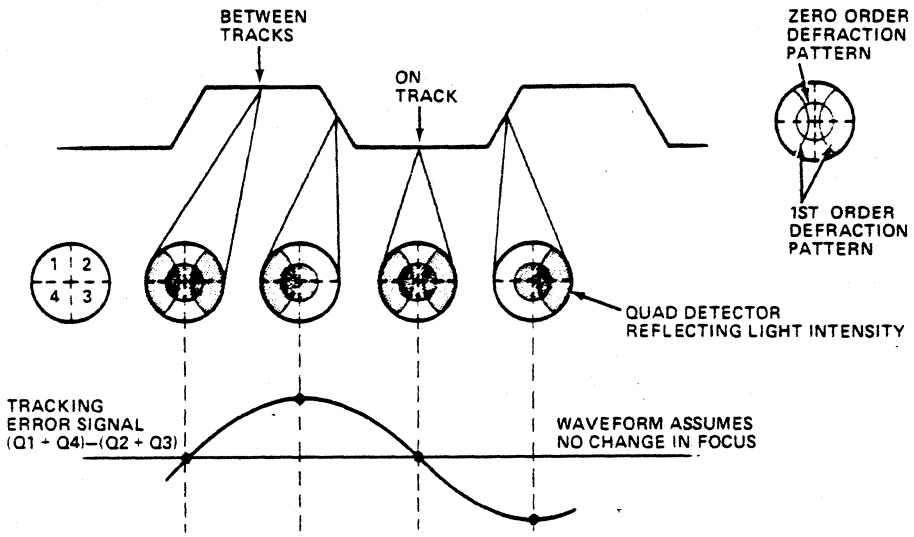
The Servo Preamplifier generates servo signals for the Focus, Fine, and Coarse Servo Loops from the outputs of the Quad Detector and Position Sensor. With the exception of the Position Sum signal, these signals are sent to the ESG PCA via the Servo Signals Trim circuit. The Position Sum signal is sent to the R/WC PCA.

3.12.3.11. Servo Signal Trim

The Servo Signal Trim circuit normalizes servo signals from the Servo Preamplifier for compatability with the servo loop circuits.



A. FOCUS ERROR SIGNAL DERIVATION



B. TRACKING ERROR SIGNAL DERIVATION

C. READ SIGNAL (DATA AND CLOCK) DERIVED FROM CHANGES IN BIAS CURRENT FOR Q1 - Q2 - Q3 - Q4

PB002210

Figure 3-84. Quad Detector Signals

3.12.3.12. Read Preamplifier

The Read Preamplifier buffers the read data output from the Quad Detector, amplifies the signals, and transmits them to the Read/Write Control PCA differentially over the flex lead.

3.12.4. Electromechanical System

Functionally, the Carriage Electromechanical System (refer to figures 3-82 and 3-85) consists of the Fine Servo Motor (FSM) and Coarse Actuator. Relative motions of these components are perpendicular to that of the spiral tracks on the spinning disk and parallel to each other.

The FSM (M2 in figure 3-85) is mounted on top of the Coarse Actuator (M1). The driving forces for the FSM and the Coarse Actuator are controlled independently. Two sets of error signals are generated to control these forces, X2 and X2-X1. Signal X2 is generated by the Optical System from preformatted servo information read from the disk. This error signal represents the spacing difference between the FSM and the track to be followed. Error signal X2-X1 is generated by the Position Sensor. This signal represents the relative spacing between the FSM and the Coarse Actuator.

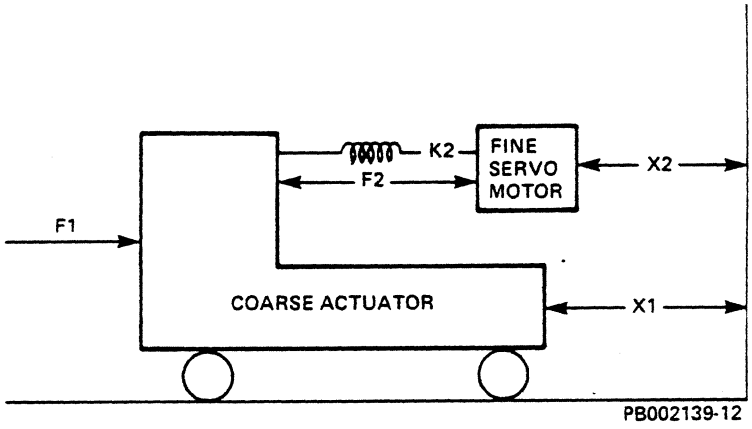


Figure 3-85. Electromechanical System Model

During a Seek operation, the FSM is moved toward the specified track, followed by the Coarse Actuator. The FSM is Driven by the 8031 Microprocessor on the Servo/Drive Control PCA. The Tracking Signal (refer to figure 3-84) from the Optical System is used to detect track crossings. The track crossing signals are input to the 8031 Microprocessor. The microprocessor measures the time between track crossings. The distance between tracks is known. The microprocessor calculates the average velocity of the FSM (change in distance divided by change in time). The number of tracks to be crossed before the desired track is also known. The number of tracks remaining to the target and the velocity trajectory are used to calculate the desired velocity. The difference between the average velocity and desired velocity is the velocity error. The 8031 Microprocessor outputs the velocity error to a digital-to-analog converter in the Tracking Servo Loop. In this loop, the error value is converted to Tracking Drive, which is applied to accelerate or decelerate the FSM to the desired velocity.

Long Seeks result in high velocities at long distances from the desired track which are continuously reduced in magnitude until the target track is reached. When the desired track is reached, the FSM enters the tracking mode. The microprocessor continues to monitor tracking error signal status to ensure Seek completion and that a stable tracking state exists.

During tracking, the Tracking Signal from the Optical System controls FSM movement. This signal is input to the Tracking Servo Loop which produces TRACKING DRIVE to keep the FSM on track. The Tracking Servo Loop is stabilized by a lead-lag network to prevent oscillation.

In the Tracking and Seek Modes, the Position Sensor is used to control the Coarse Actuator. When the FSM moves off the relative zero position of the Coarse Actuator, the Position Sensor sends an error signal to the Coarse Servo Loop. This loop provides COARSE DRIVE to the Coarse Actuator to reposition the Carriage. As a result, the Coarse Actuator follows the movement of the FSM. The Coarse Servo Loop is stabilized by a lead-lag network to prevent oscillation.

Although the components of the Electromechanical System are coupled, the effective loop bandwidth of the FSM is much larger than that of the Coarse Actuator. The resultant tracking system allows the FSM to follow large runouts up to relatively high frequencies (2.5 kHz). Whereas, the Coarse Actuator reacts to low frequency variations (200 Hz).

The FSM is also used to keep the Optical System in focus. The Focus Signal from the Optical System provides the focus error to the Focus Servo Loop. This loop provides FOCUS DRIVE to move the Objective Lens, mounted in the FSM, back into focus position. The Focus Servo Loop is stabilized by a lead-lag network to prevent oscillation.

3.13. MEDIA

The Media is the physical medium in which data is stored by the LD 1200. It consists of a 12-inch diameter glass sandwich disk contained in a protective enclosure (cartridge).

The Data Cartridge consists of a top and bottom half, which includes locks and optical access doors (refer to figure 3-86). When the cartridge is not installed in the LD 1200, it is in a closed position. In the closed position, the top and bottom halves form an enclosure with the recording Media disk (disk) inside. The locks at each corner of the cartridge keep it closed. The shape of the cartridge halves limits the movement of the disk and the hub attached to it.

When the cartridge is inserted into the LD 1200, the locks disengage, the optical access doors open, the cartridge halves separate to free the disk and hub assembly, and the disk is held to the spindle magnetically.

The cartridge includes a Write Protect Tab which enables a user to protect the cartridge from being written on, when desired (refer to figure 3-86).

The disk is a sandwich consisting of two 12-inch diameter glass disk substrates bonded to, and separated by, an inner and outer spacer ring (refer to figure 3-87). The sandwich construction of the disk protects recorded data against environmental exposure.

One side of the disk is usable for storing data. On this substrate, an intermediate polymer layer is deposited. A sensitive layer of Tellurium Alloy is deposited on the intermediate layer. Grooves, carrying prerecorded tracking, sector, and clock information, are impressed in the sensitive layer.

When the cartridge is inserted into the LD 1200, the disk attaches to the Drive Motor Spindle magnetically (refer to figure 3-87). The hub of the disk is aluminized, enabling the disk to be held in place on the Spindle by magnetic attraction.

3.13.1. Surface Format

The disk is preformatted with track, sector, and clock information in pregrooved continuous spiral tracks (refer to figure 3-88). The spiral tracks are logically segmented into circular tracks.

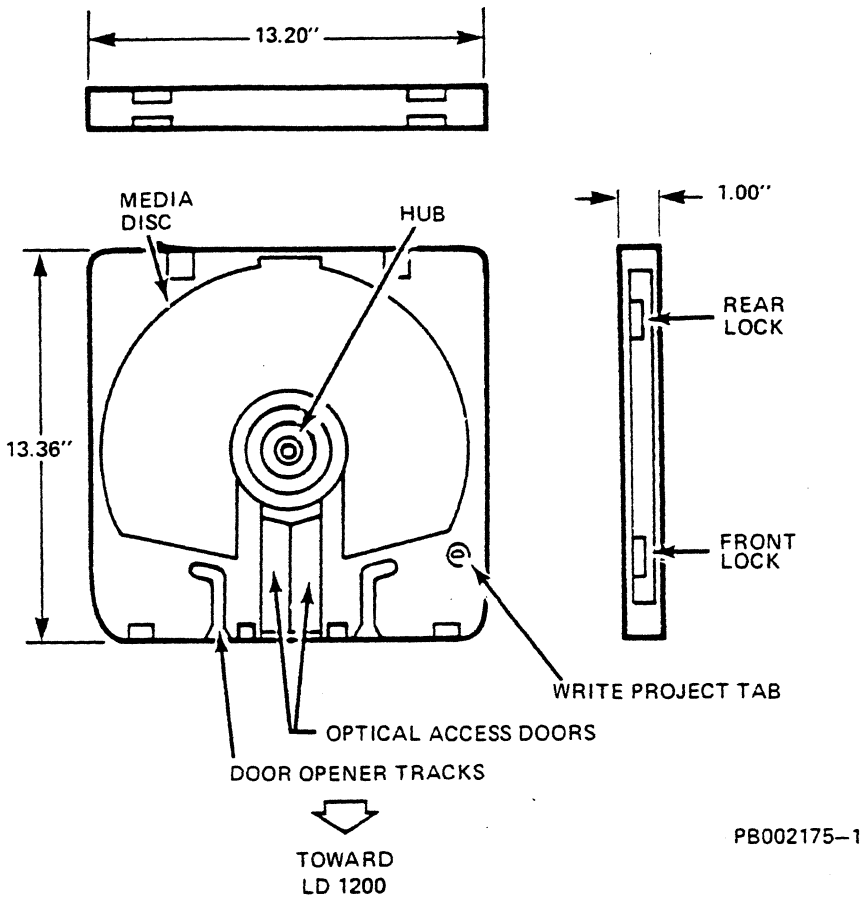
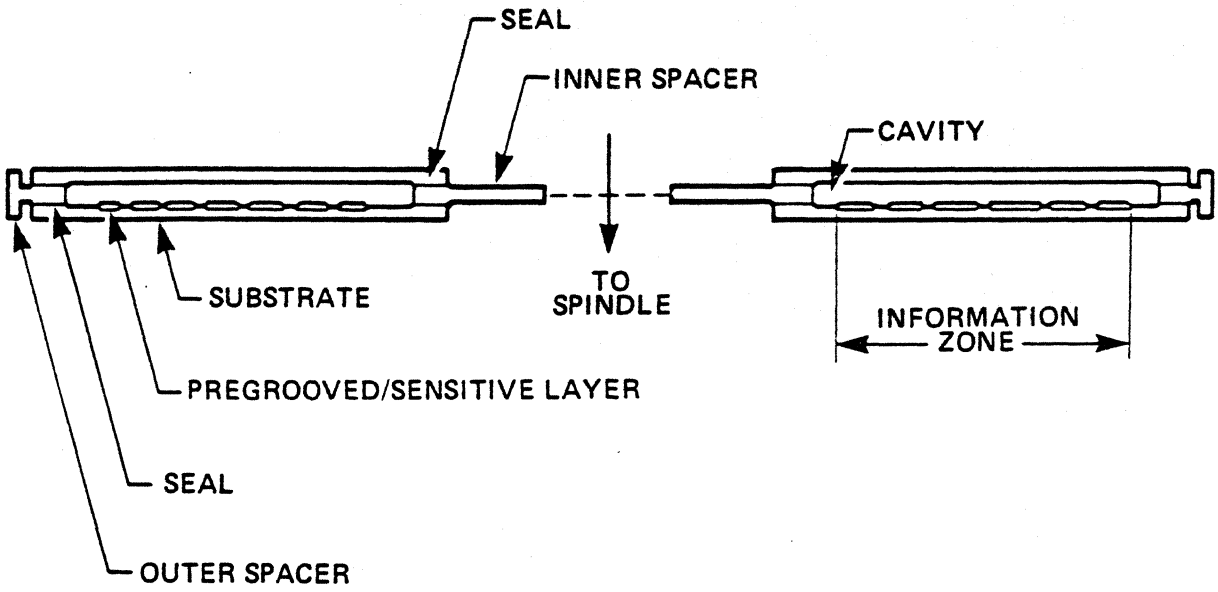
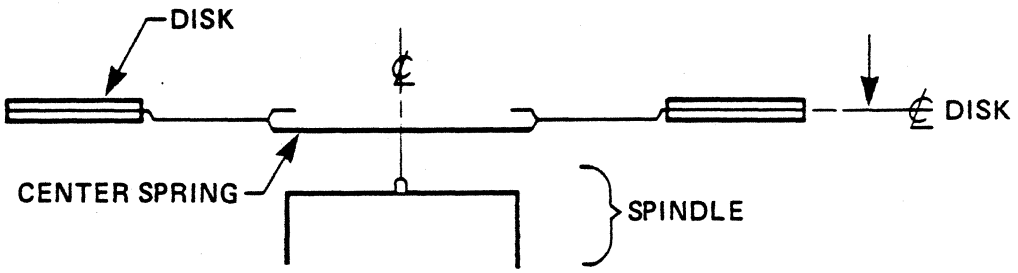


Figure 3-86. LD 1200 Data Cartridge



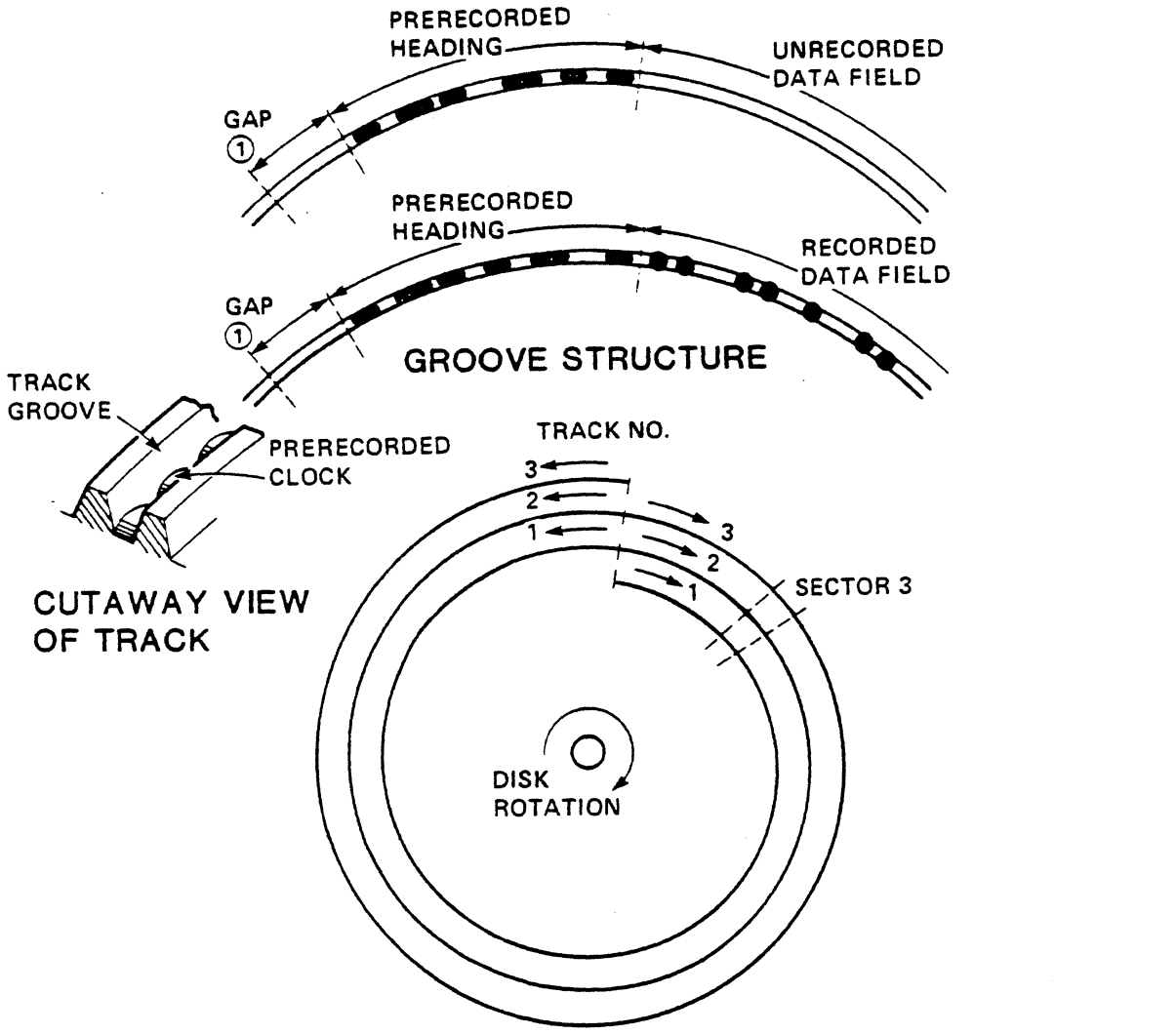
SANDWICH DISK CONSTRUCTION

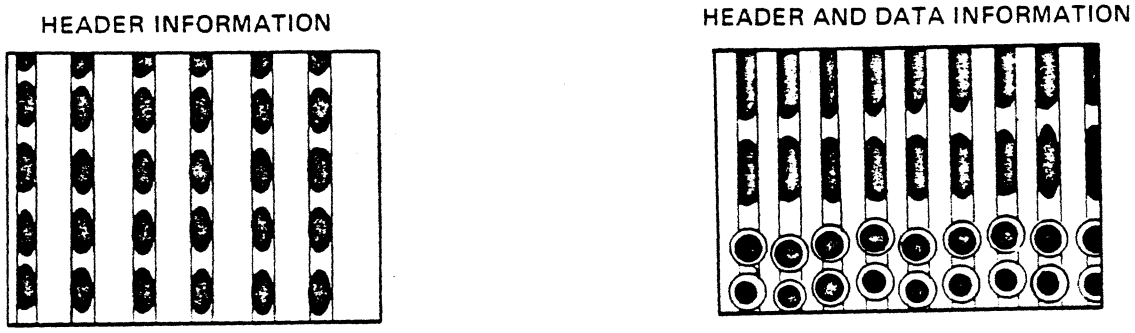


DISK TO DRIVE INTERFACE

PB002170-1

Figure 3-87 Disk Construction





NOTE:
① Gap contains clock information only.

PB002170-2

Figure 3-88 Recording Surface Format

The recording surface of the disk is divided into three areas: inner band, user band, and outer band.

NOTE

Inner and Outer bands are not accessable for user data, but are used by the Drive for initialization and diagnostics.

The three recording bands consist of groups of tracks, numbered as follows:

- Inner band (not for user data): Track -2350 (F6D2 hex), at radius 84.9 ±0.1 millimeters, through -1 (FFFF hex)
- User band: Track 0 (0000 hex) through 31,999 (7CFF hex)
- Outer band (not for user data): Begins at track 32,000 (7D00 hex), radius 142.6 ± 0.1 millimeters

With a clockwise rotation of the disk, the continuous track spirals outward from the inner radius. Beginning at the innermost logical track, track numbers increment by one, from -2350, with each revolution. Each logical track is divided into 32 sectors, numbered 0 through 31 (00 through 1F hex).

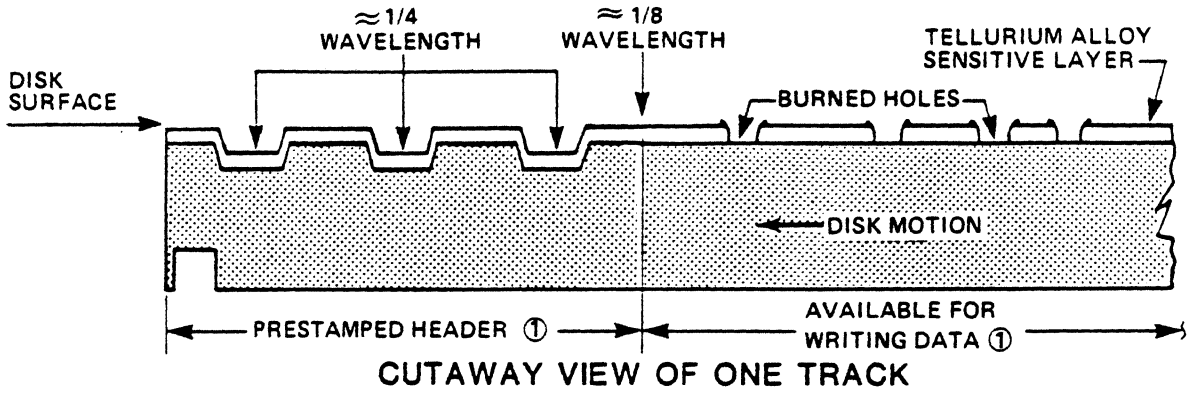
Each sector is identified in the Header by track number and sector number, which is prestamped in the track. A sector contains 1200 bytes of information, including a 15-byte Header followed by an 1185-byte Data Field. Track format is further described in the Data Recording Format subsection.

NOTE

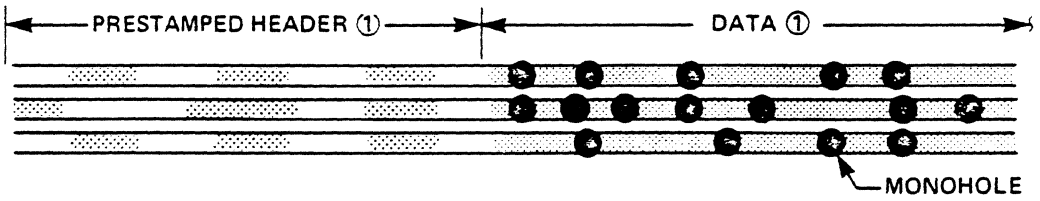
In the inner band, the data fields of Sector 0 are preformatted with TOON encoded data for visual reference.

Within the track groove, header information is prerecorded by forming a relief pattern, the depth of which is one quarter of the laser output wavelength (refer to figure 3-89). Disk clocks are preformatted in the bottom of the track groove, which is one eight wavelength in depth.

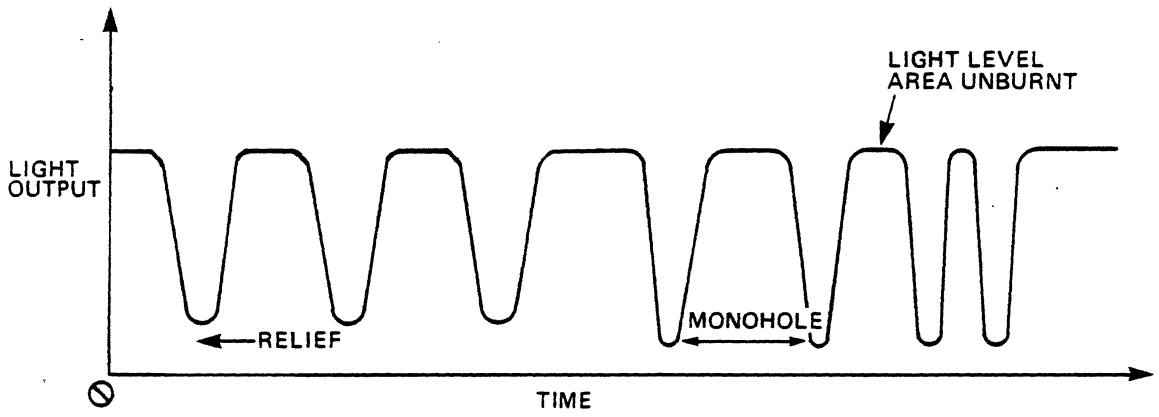
Data is written at the zero-crossings of the disk clock (refer to figure 3-90). When a data monohole is burned into the track, the resulting hole destroys approximately three clock zero-crossings. The remaining clocks in a TOON cell are sufficient to keep the Read/Write channel in synchronization with the disk.



CUTAWAY VIEW OF ONE TRACK



TOP VIEW OF THREE TRACKS



HEADER AND DATA AS REPRESENTED BY LIGHT REFLECTED FROM THE DISK

Note:
① Prestamped clock not shown.

PB002171-1

Figure 3-89. Media Track Structure

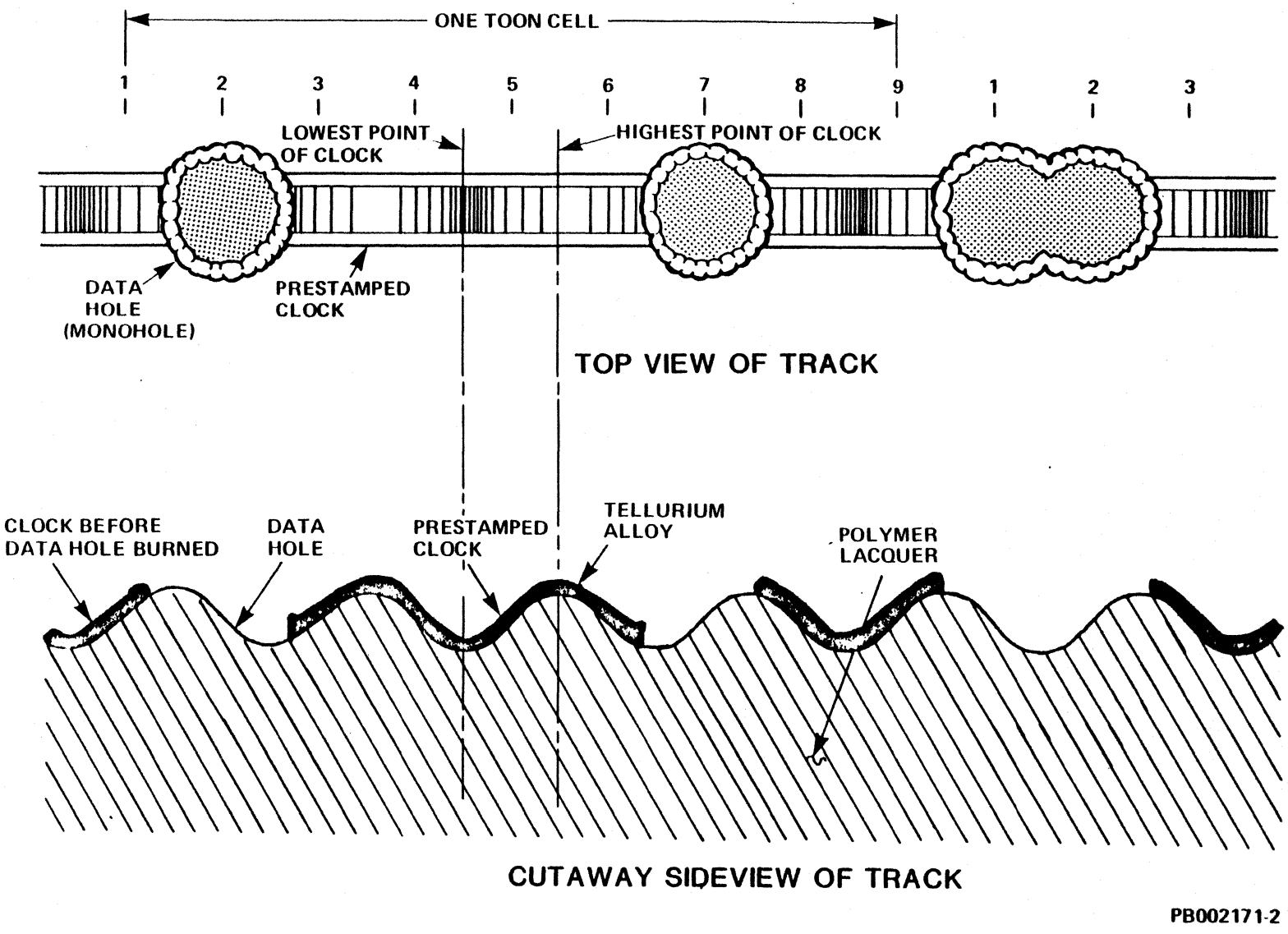


Figure 3-90. Data Representation in the Media

3.13.2. Data Recording Format

Header and user data is recorded in sectors, which are formatted as shown in figure 3-91. Each of the 32 sectors on a track includes the following fields:

HEADER

- Sector Mark (4 bytes) - used for bit and byte synchronization. The Sector Mark indicates the beginning of each sector, and is the point to which bit and nibble boundaries are referenced. The Read/Write channel resynchronizes the Read/Write circuitry to the beginning of each sector.

  The Sector Mark is prerecorded in a special TOON code to distinguish it from data (refer to figure 3-92). A Sector Mark TOON cell contains either two odd or two even monoholes, whereas a data TOON cell can contain only one odd and one even monohole.

- First Gap (2 bytes) - used for Phase-Locked Loop (PLL) resynchronization after a Sector Mark distortion. This field contains clock information only.

- Wobble Bytes (4 bytes) - used to synchronize the Tracking Servo Loop to the pregrooved track at the beginning of each sector. The prerecorded Wobble Bytes contain the TOON representation of 66 hex. The monoholes in the bytes are positioned off the center of the track, to the left then to the right, as shown in Figure 3-93. The arrangement of the monoholes provides a low-frequency tracking signal to supplement that provided during track following.

- Second Gap (1 byte) - used to maintain PLL synchronization. This field contains clock information only.

- ID (3 bytes) - contains sector identification, as follows:

  - Sector (1 byte) - contains the sector address

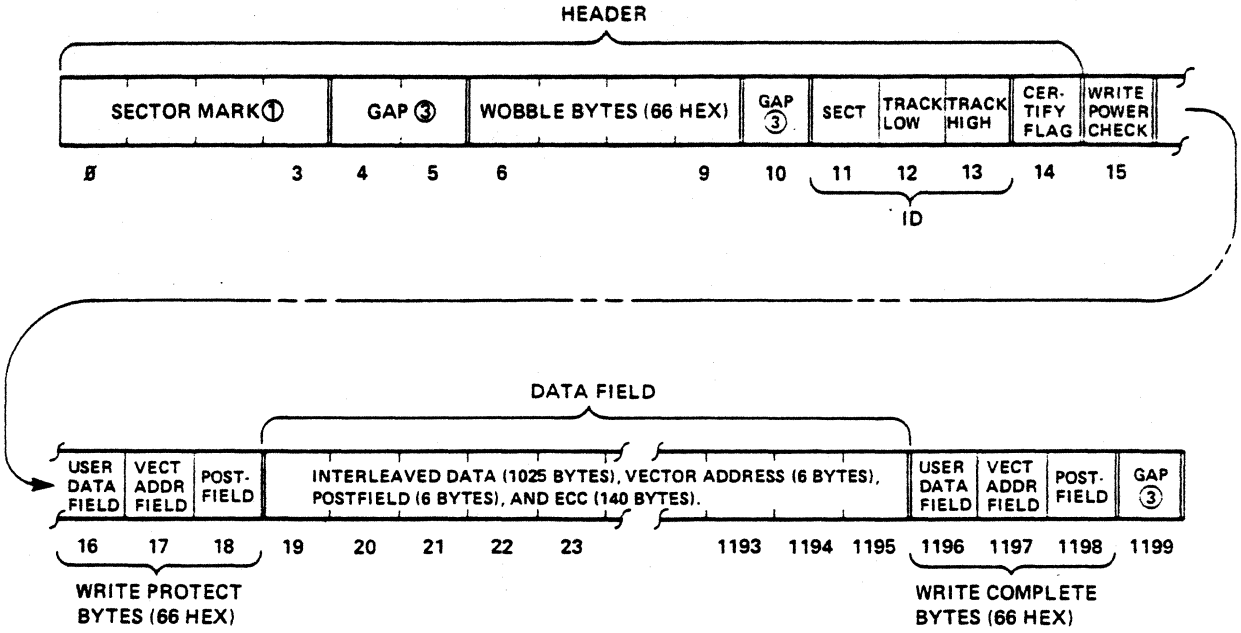
  - Track Low (1 byte) - contains the least-significant byte of the track address

  - Track High (1 byte) - contains the most-significant byte of the track address

- Certify Flag (1 byte) - 66 hex is written in this field when it is necessary to indicate there is a flaw in the next sector.

DATA

- Write-Power Check (1 byte) - 66 hex is written in this field every time a Write operation is attempted. Writing in this field enables the Power Control Loop to check laser write power before an attempt is made to write data. If write power is not within a predefined window when the check is made, the loop provides an error status which can result in reinitialization of the LD 1200.



Notes:

① Refer to Sector Mark Code Definition illustration.
2. Bytes 0 through 13 and 1199 are read-only areas. The remaining areas of the sector are for both writing and reading.
③ Gaps contain clock information only.
4. Refer to TOON Code Definition Table for code format used in Bytes 6 through 9 and 11 through 1198.
⑤ Refer to Wobble Bytes illustration.

PB002175-2

Figure 3-91. LD 1200 Sector Format (One Sector)

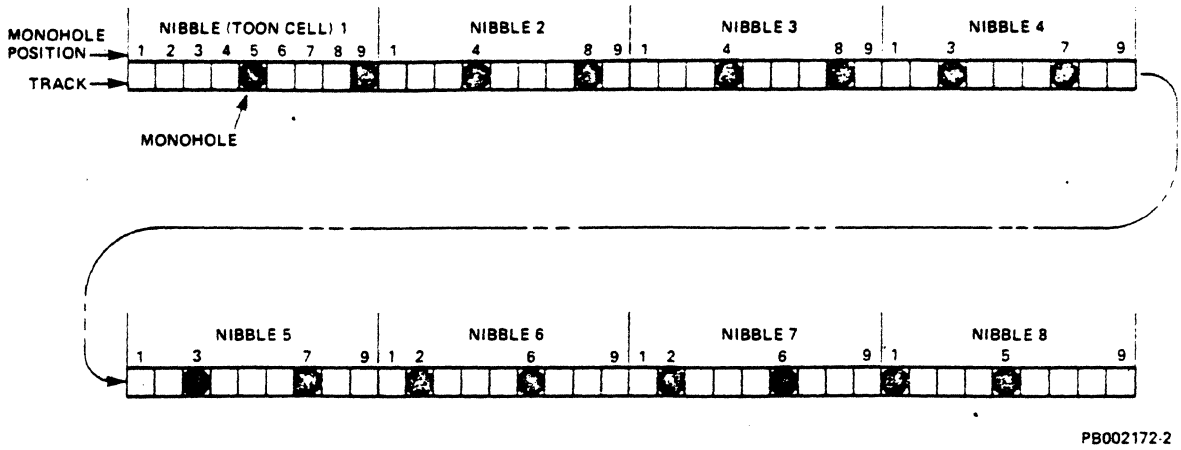


Figure 3-92. Sector Mark Code Definition

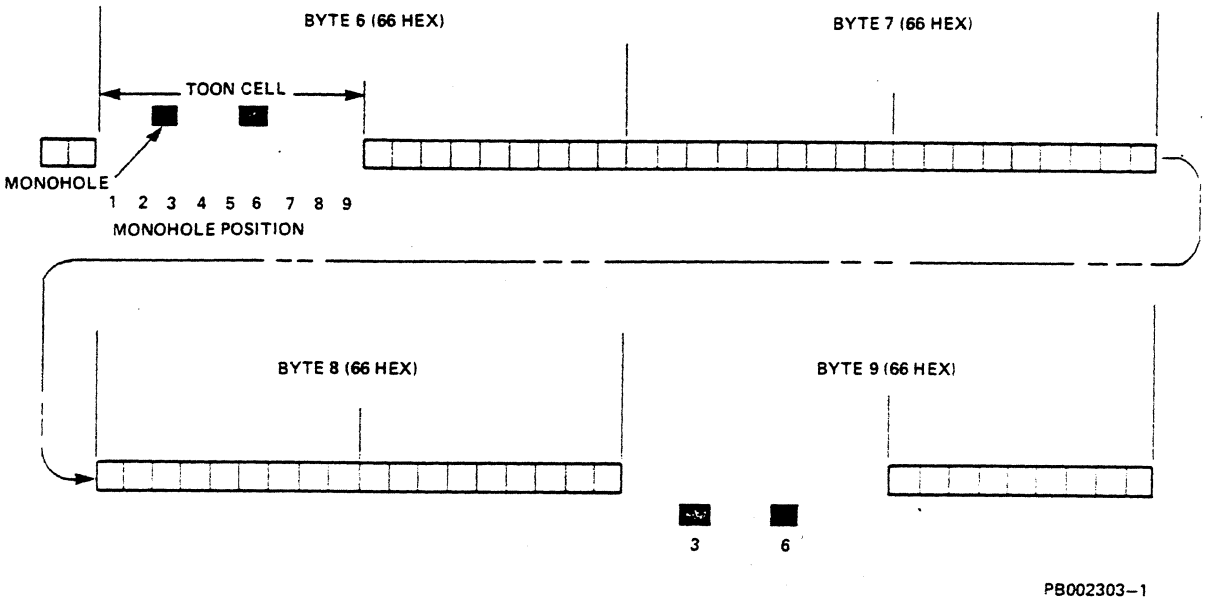


Figure 3-93. Wobble Bytes

- Write Protect Bytes (3 bytes) – there is one Write Protect Byte for each subfield of the Data Field, arranged in the following sequence:

  (1) User Data Field Write Protect Byte

  (2) Vector Address Field Write Protect Byte

(3) Postfield Write Protect Byte

When an attempt is made to write in a subfield of the Data Field, 66 hex is written in the associated Write Protect Byte. These bytes provide overwrite protection, which prevents data from being destroyed accidentally by an erroneous Write operation.

- Data Field (1177 bytes) - contains the following interleaved subfields:

  - User Data Field (1025 bytes) - user information stored in the LD 1200

  - User Data ECC (100 bytes) - error correction characters for the User Data Field

  - Vector Address Field (6 bytes) - used as a pointer to inform the ICI PCA whether or not to release the associated User Data Field to the Host as valid data. The LD 1200 writes information in the Vector Address Field as each sector is written. The information is then used during Read operations to monitor for sectors that were flagged as bad during a previous Write operation. The vector address for a given User Data Field is written in the sector following the one containing the user data.

  - Vector Address ECC (20 bytes) - error correction characters for the Vector Address Field

  - Postfield (6 bytes) - primarily used to enable the user to declare a particular sector, record, or file obsolete and to point to a new location for the current version of that information. The Postfield is written as a separate entity even though its contents are physically interleaved with the other subfields of the Data Field. Five bytes in the Postfield are defined by the user, and are not interpreted by the LD 1200. The remaining byte is used by the LD 1200 only when a sector has been flagged as bad. This byte is used in conjunction with the Vector Address to ensure that flawed sectors are not transferred to the Host during Read operations.

  - Postfield ECC (20 bytes) - error correction characters for the Postfield

  With the exception of the Sector Mark, data is written (and prerecorded) in the Media in TOON code. As shown in Table 3-18, a nibble (four bits) of binary information is encoded into a TOON cell using two monoholes. One monohole must be in an even position and one in an odd position. Monohole position 9 is never used in data encoding.

- Write Complete Bytes (3 bytes) - there is one Write Complete Byte for each subfield of the Data Field, arranged in the following sequence:

  (1) User Data Field Write Complete Byte

  (2) Vector Address Field Write Complete Byte

  (3) Postfield Write Complete Byte

  A 66 hex written in any of the Write Complete Bytes indicates that the associated subfield of the Data Field has been completely and successfully written. The Write Protect and Write Complete Bytes are used for data integrity and flawed sector detection.

- Third Gap (1 byte) - separates the Data Field and Header. This field contains clock information only.

Table 3-18. TOON Code Definition

BINARY NIBBLE MSB LSB	EQUIVALENT TOON CELL MONOHOLE POSITIONS 1	2	3	4	5	6	7	8	9
0000	●	●							
0001	●			●					
0010	●					●			
0011	●							●	
0100		●	●						
0101			●	●					
0110			●			●			
0111			●					●	
1000		●			●				
1001				●	●				
1010					●	●			
1011					●			●	
1100		●					●		
1101				●			●		
1110						●	●		
1111							●	●	

1. Data monoholes are never written in Position 9.

TBL13

3.14. BASEPLATE

The Baseplate provides the main supporting structure for the critical mechanical, electromechanical, and optomechanical components of the LD 1200.

3.14.1. Signal Descriptions

Signal descriptions for the Baseplate are as follows (refer to figure 3-94):

(1) CARRIAGE LOCK SOLENOID DC - This signal is generated by the Power Supply. It provides dc voltage to the Carriage Lock Solenoid, enabling the Carriage to lock in the home position.

(2) EJECT SOLENOID DC - This signal is generated by the Power Supply. It provides dc voltage to the Interlock Solenoid, preventing cartridge removal while the Spindle is spinning.

(3) SPINDLE MOTOR AC - This signal is generated by the Power Supply. It provides ac voltage to the Spindle Motor, enabling it to run.

(4) BRAKE SOLENOID DC - This signal is generated by the Power Supply. It provides dc voltage to the Spindle Brake Solenoid, applying direct braking to the Spindle pulley.

(5) +CART LD STAT - This signal is output to the Servo/Drive Control PCA. It goes high when a cartridge inserted, activating the Cartridge Sensor which senses that a cartridge is present and allows spin-up to occur.

(6) -CARR RTRCT ST - This signal is output to the Servo/Drive Control PCA. It goes low when the Carriage Latch Solenoid is deactivated, retaining the Carriage in the fully retracted position.

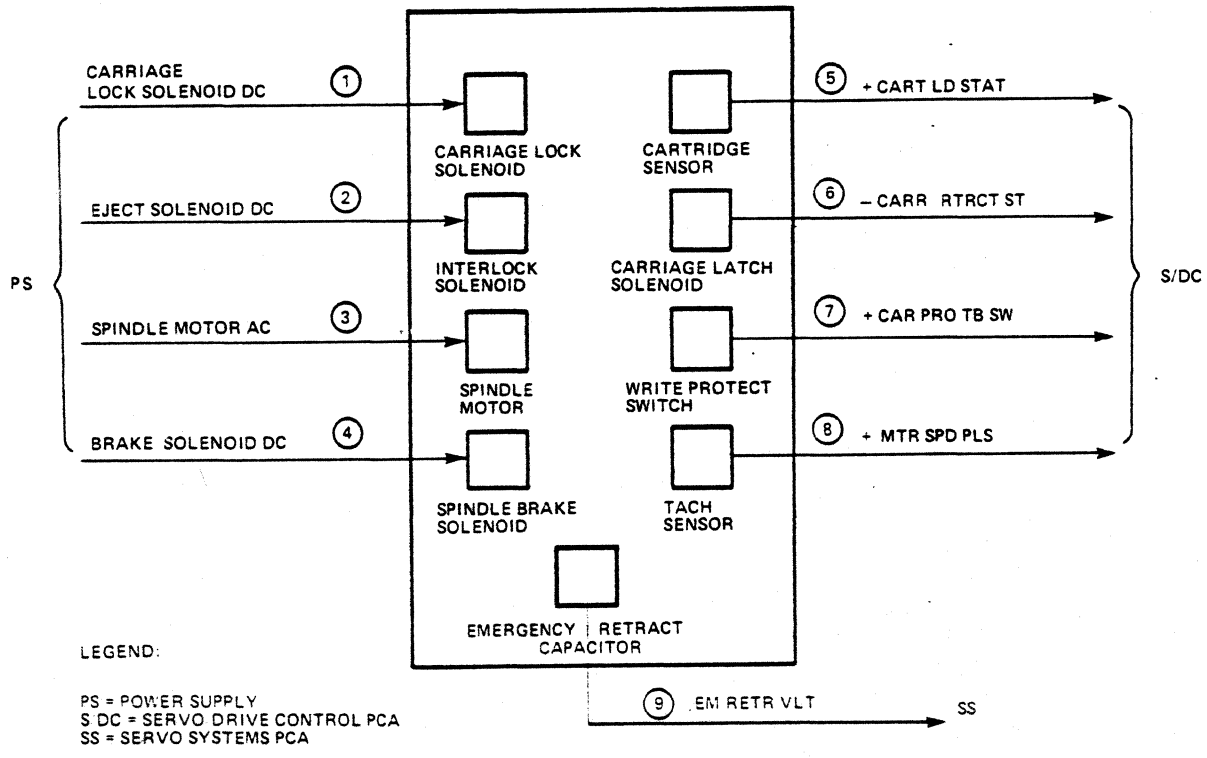
(7) +CAR PRO TB SW - This signal is output to the Servo/Drive Control PCA. It goes high when the Write Protect Switch is activated, indicating if a cartridge may be written upon.

(8) +MTR SPD PLS - This signal is output to the Servo/Drive Control PCA. It goes high when the Tachometer Sensor is active, indicating when the Spindle Motor is up-to-speed during spin-up and at rest during spin-down.

(9) EMERG RETRACT VOLT - This signal is output to the Servo/Systems PCA. It indicates when the Power Supply dc voltage is below an acceptable level, activating the Emergency Retract Capacitor to provide the +12 Vdc needed to initiate a Carriage retract.

(10) AC NEUTRAL - (Not shown on block diagram.) This signal line provides a neutral path for ac voltages output by the Power Supply.

(11) DC RETURN - (Not shown on block diagram.) This signal is generated by the Power Supply, providing a return path for dc output voltages.



PB002192-3

Figure 3-94 Baseplate Block Diagram

3.14.2. Functional Description

The Baseplate contains all the major components that allow data to be stored on and retrieved from the Data Cartridge. It contains the Cartridge Load/Eject Mechanism, the Spindle Assembly and Spindle Motor that rotate the disk, and the Carriage and Linear Actuator Motor that allow the Carriage Assembly to move between tracks. The Baseplate also contains carriage rails for reduced friction travel of the Carriage Assembly, and the actuating mechanism for the optical access doors which are opened by Data Cartridge insertion. Normally closed to protect the Media from the environment, they must be open to perform read/write operations.

Signals generated by the Power Supply provide power to lock the Carriage in the Home position, provide power to run the Spindle Motor, prevent Data Cartridge removal when the Spindle Assembly is rotating, and provide a means for braking the Spindle Assembly rotation.

Signals output to the Servo/Drive Control PCA and Servo Systems PCA retain the Carriage in the home position, allow Media write protection to occur, sense when the Spindle Motor is up-to-speed or at rest, and provide emergency power during a Power Supply malfunction to initiate a Carriage retract.

These functions are performed by the following components (refer to the General Description Section in this manual for their location):

Cartridge Guides - Properly align the Data Cartridge when inserted.

Cartridge Load/Eject Mechanism - Locks the Data Cartridge in place after insertion and opens the optical access doors. These doors are normally closed to protect the Media from the environment. The Media can only be accessed when they are open.

Spindle Motor and Motor Run Capacitor - Rotates the Spindle Assembly and provides centering for the disk. The Motor Run Capacitor enables the Spindle Motor to spin up smoothly.

Spindle Assembly - Holds the Data Cartridge in the proper position, brakes the Spindle to a stop during spin-down, and rotates the disk.

Motor Brake Assembly - Applies direct braking to the Spindle pulley.

Carriage Assembly - Provide the means to locate, read, and write data on the Media.

Positioner Motor Magnet - Interacts with the Carriage to form a voice coil motor, which moves the Carriage during Seek operations.

Shock Mounts - Reduce vibrational shock that could harm critical components and affect data access.

Tachometer Sensor - Senses the speed of the Spindle Motor.

Guardband Sensor - Indicates when the Carriage is retracted to the guardband area of the Media.

Data Cartridge Flag - Senses when a Data Cartridge is inserted.

Carriage Lock Solenoid Assembly - Allows the Carriage to lock in the fully retracted position during power-down and emergency retract.

Interlock Solenoid Assembly - Prevents Data Cartridge removal while the Spindle is spinning.

Write Protect Switch Assembly - Provides Media write protection when the Write Protect Tab on the Data Cartridge is in the write protect position. It is enabled by rotating 180 degrees in the counter-clockwise direction.

Spindle Grounding Brush - Provides Spindle ground to reduce electrostatic buildup.

Baseplate Terminator PCA (also known as Baseplate PCA) - Distributes logic signals from the Baseplate to the Card Rack. This PCA includes the Emergency Retract Capacitor, Write Protect Switch, and Data Cartridge Flag.

Carriage Rails - Provides the reduced-friction surface needed for Carriage movement.

Front and Rear Crash Stops - Stops the Carriage from further movement if the Drive circuitry malfunctions.

Emergency Retract Capacitor - Provides emergency voltage, causing the Carriage to retract if the Power Supply malfunctions and is unable to supply adequate power.

3.15. POWER SUPPLY

The Power Supply is a switch mode type unit, which includes a self-contained cooling fan for the LD 1200. For ease of maintenance, the Power Supply is a field-replacement unit (FRU).

The Power Supply provides:

- Five dc outputs with adequate current for the Drive and Internal Controller. Electronic margin control is provided for all the dc outputs except +40 Vdc.
- Logic controlled outputs for:
  - Spindle Motor
  - Cartridge Interlock Solenoid
  - Carriage Lock Solenoid
  - Spindle Brake Solenoid
- Power supply operative status
- Overtemperature status
- Line synchronization signal
- Circuitry for Power Supply external shutdown

3.15.1. Input Specifications

INPUT VOLTAGE

The Power Supply operates at any of the following line input voltages: 100, 110, 120, 200, 220, or 240 Vac, +6.7% -13.3%. Line input voltage is selected by means of a jumper provided on the Power Supply. The jumper is not easily accessible when the Power Supply is installed in the LD 1200. If it becomes necessary to change the jumper, the Power Supply top cover and the top printed circuit assembly (PCA) inside must be removed.

INPUT FREQUENCY: 47 to 66 Hz

INPUT POWER: 0.4 kVA

3.15.2. Output Specifications

The Power Supply provides the following output voltages:

NOMINAL OUTPUT VOLTAGE ±2%	LOAD RANGE	SWITCHED	PROGRAMMED MARGIN CONTROL
+5V	2 - 21A	N/A	±5%
-5V	0.1 -0.4A	N/A	±5%
+12V	0.3 - 3.9A	YES	±5%
-12V	0.2 - 3.5A	YES	±5%
+40V (Bias)	1A	N/A	N/A
115 Vac	0.75A	N/A	N/A
115 Vac	0.5A	YES	N/A

All dc outputs, except +40V, are protected against overvoltage and undervoltage conditions. Overcurrent and short circuit protection are provided for all ac and dc outputs except +40V. The +40-volt current is limited by the source impedance of the Power Supply.

3.15.3. Interface Signals

The following signals are used to interface the Power Supply with the remainder of the LD 1200 circuits (refer to figure 3-95):

AC NEUTRAL (not shown in Power Supply block diagram)

This is the neutral path for ac voltages output by the Power Supply.

+BRK MTR CNTL

This signal is generated by the Servo/Drive Control PCA. It controls the Spindle Motor ac output and Brake Solenoid +12-Vdc output as follows:

BRAKE/MOTOR CONTROL	SPINDLE MOTOR AC OUTPUT	BRAKE SOLENOID +12-VDC OUTPUT
Low	On (motor on)	On (brake off)
High	Off (motor off)	Off (brake on)
Open	Off (motor off)	Off (brake on)

+CARR LOCK CNTL

This signal is generated by the Servo/Drive Control PCA. It controls the Carriage Lock Solenoid, which locks the Carriage in the Home position when the LD 1200 is not running or is powered down. (Refer to CARRIAGE LOCK SOLENOID DC signal description.)

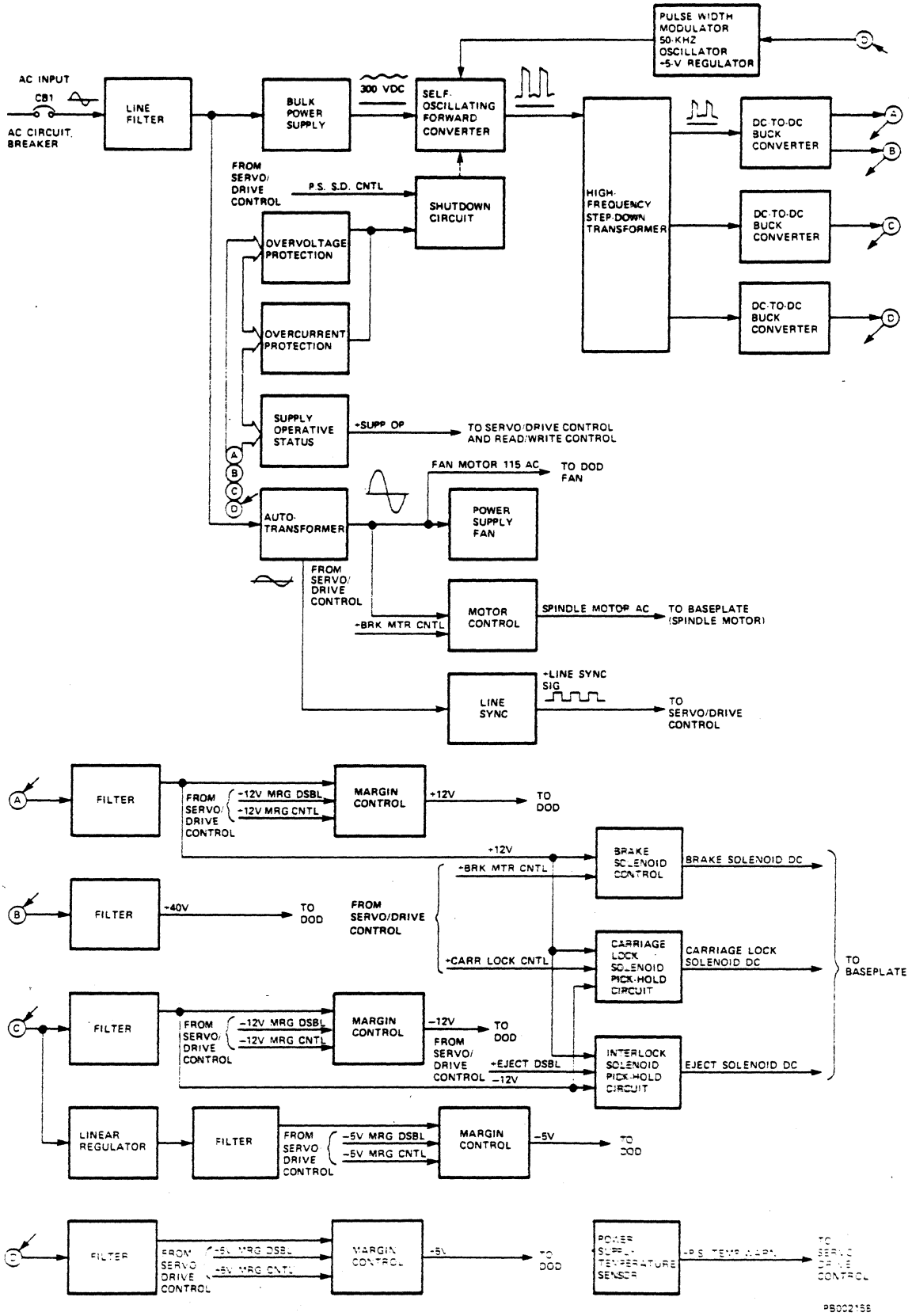


Figure 3-95. Power Supply Block Diagram

DC RETURN (not shown in Power Supply block diagram)

This is the return path for dc voltages output by the Power Supply.

+EJECT DSBL

This signal is generated by the Servo/Drive Control PCA. It controls the Interlock Solenoid, which locks the front door of the LD 1200 while the spindle is spinning, to prevent removal of the Data Cartridge. (Refer to EJECT SOLENOID DC signal description.)

P.S. S.D. CNTL (Power Supply Shutdown)

This signal is generated by the Servo/Drive Control PCA. It shuts down Power Supply outputs when the Servo/Drive Control logic detects an unsafe condition (such as overtemperature) in the LD 1200:

POWER SUPPLY SHUTDOWN	POWER SUPPLY OUTPUTS
Low	Off
High	On
Open	On

After the unsafe condition is removed, Power Supply operation can be restored by setting the ac circuit breaker (at the rear of the LD 1200) to OFF, then to ON.

MARGIN DISABLES (+5V MRG DSBL, -5V MRG DSBL, +12V MRG DSBL, -12V MRG DSBL)

These signals are generated by the Servo/Drive Control PCA. A margin disable enables the associated margin control line to force the pertinent output voltage up or down 5% from the nominal value:

MARGIN DISABLE LINE	ASSOCIATED MARGIN CONTROL LINE
Low	Enabled
High	Disabled (associated output nominal)
Open	Disabled (associated output nominal)

MARGIN CONTROLS (+5V MRG CNTL, -5V MRG CNTL, +12V MRG CNTL, -12V MRG CNTL)

These signals are generated by the Servo/Drive Control PCA. A margin control forces the associated Power Supply output voltage up or down by 5% when the associated margin disable line is enabled (low):

MARGIN DISABLE	MARGIN CONTROL	ASSOCIATED OUTPUT VOLTAGE
+5V low	+5V low	+5.355 Vdc ±2%
+5V low	+5V high or open	+4.847 Vdc ±2%
+5V high or open	+5V disabled	+5 Vdc (nominal)
-5V low	-5V low	-5.25 Vdc ±2%
-5V low	-5V high or open	-4.75 Vdc ±2%
-5V high or open	-5V disabled	-5 Vdc (nominal)
+12V low	+12V low	+12.6 Vdc ±2%
+12V low	+12V high or open	+11.4 Vdc ±2%
+12V high or open	+12V disabled	+12 Vdc (nominal)
-12V low	-12V low	-12.6 Vdc ±2%
-12V low	-12V high or open	-11.4 Vdc ±2%
-12V high or open	-12V disabled	-12 Vdc (nominal)

BRAKE SOLENOID DC

This signal is an output to the Baseplate. It provides switched +12 Vdc to the Spindle Brake Solenoid in order to apply braking action to the spindle. BRAKE SOLENOID DC is provided when the Brake/Motor Control line goes high. (Refer to Brake/Motor Control signal description.)

CARRIAGE LOCK SOLENOID DC

This signal is an output to the Baseplate. It provides switched pick-hold voltage to the Carriage Lock Solenoid to lock the Carriage in the Home position. CARRIAGE LOCK SOLENOID DC is controlled by the Carriage Lock Control and Supply Operative Status signals:

SUPPLY OPERATIVE STATUS	CARRIAGE LOCK CONTROL	CARRIAGE LOCK SOLENOID DC
Low (inactive)	Low (active)	Off (Carriage locked)
High (active)	Low (active)	On (Carriage unlocked)
High (active)	High (inactive)	Off (Carriage locked)
High (active)	Open	Off (Carriage locked)
Open	High (inactive)	Off (Carriage locked)

DC VOLTAGES

Refer to the Output Specifications subsection.

EJECT SOLENOID DC

This signal is a dc output to the Baseplate. It provides switched pick-hold voltage to the Interlock Solenoid to prevent removal of the Data Cartridge while the spindle is spinning:

EJECT DISABLE CONTROL	EJECT SOLENOID DC
Low	On (Cartridge removable)
High	Off (Cartridge not removable)
Open	Off (Cartridge not removable)

FAN MOTOR 115 AC

This signal is an ac output to the card cage fan. It provides power to operate the fan, which cools the LD 1200 card cage. This output is provided whenever the ac circuit breaker CB1 (at the rear of the LD 1200) is set to ON.

+LINE SYNC SIG

This signal is a TTL logic output to the Servo/Drive Control PCA. It indicates that the input voltage to the Power Supply is equal to or greater than the minimum range value required for reliable operation of the LD 1200. The duty cycle of + LINE SYNC SIG is from 45% to 55%. The frequency of the signal is the same as the ac input line.

+P.S. TEMP WARN (Power Supply Temperature Warning)

This signal is output to the Servo/Drive Control PCA. It is an early warning signal indicating the ambient temperature of the Power Supply has reached 65 ±3 degrees Centigrade. The Power Supply shuts down a minimum of 100 milliseconds after the low to high transition of this signal. Power supply operation can be restored after an overtemperature shutdown by setting the ac circuit breaker CB1 (at the rear of the LD 1200) to OFF, then ON.

SPINDLE MOTOR AC

This signal is an ac output to the Baseplate. It provides a switched ac voltage to run the Spindle Motor. SPINDLE MOTOR AC is controlled by the Brake/Motor Control signal. (Refer to Brake/Motor Control signal description.)

+SUPP OP (Supply Operative Status)

This signal is a TTL logic output to the Servo/Drive Control PCA. It goes high a minimum of 1 millisecond after all dc voltages are within operating range. It goes low within 5 microseconds after any of the dc voltages drops out of operating range. This signal is used by the Servo/Drive Control PCA to generate Power-On Reset for the Servo and Drive Control Microprocessors and the SIA bus.

+40V

This signal is a dc output to the Read/Write Control PCA. It provides power to the Sense Diode which provides the signal for the Power Control Loop that drives the Laser Diode. (Refer to the Output Specifications subsection.)

3.15.4. Block Diagram Description

Descriptions of the Power Supply functional blocks, shown in figure 3-95, are provided in the following subsections.

3.15.4.1. AC Circuit Breaker

The ac circuit breaker is the Power-On switch for the LD 1200. It trips to the OFF position, disconnecting the ac line input from the Power Supply, when an input current overload condition occurs.

3.15.4.2. Line Filter

The Line Filter suppresses noise on the ac input line.

3.15.4.3. Bulk Power Supply

The Bulk Power Supply provides approximately +300 Vdc to the Self-Oscillating Forward Converter.

3.15.4.4. Self-Oscillating Forward Converter

This circuit converts unregulated dc, from the Bulk Power Supply, to regulated high-frequency pulses which are applied to the Step-down Transformer. The amplitude of the converter output is controlled by feedback from the Pulse Width Modulator. Output frequency is produced by input from the 50-kHz Oscillator.

The Power Supply can be shut down by inhibiting the output of the Self-Oscillating Forward Converter. When an unsafe condition is detected by the LD 1200, the Shutdown Circuit produces a signal which inhibits converter operation.

3.15.4.5. Pulse Width Modulator, 50-kHz Oscillator, +5V Regulator

The Pulse Width Modulator and 50-kHz Oscillator provide a pulse modulated high-frequency signal to regulate and control the output of the Self-Oscillating Forward Converter.

3.15.4.6. High-Frequency Step-Down Transformer

This transformer steps down the voltage output of the Self-Oscillating Forward Converter to lower voltages for input to the DC-to-DC Buck Converters.

3.15.4.7. DC-to-DC Buck Converters

There are three DC-to-DC Buck Converters in the Power Supply, which produce the following output voltages:

- +12 Vdc and +40 Vdc
- -12 Vdc and -5 Vdc
- +5 Vdc

A DC-to-DC Buck Converter converts the stepped-down output from the Self-Oscillating Forward Converter to the dc output voltage(s) required by the LD 1200.

3.15.4.8. Filters

There is a filter on each of the Power Supply dc outputs: +5 Vdc, -5 Vdc, +12 Vdc, -12 Vdc, and +40 Vdc. The filter removes the ac component of the DC-to-DC Bulk Converter output. The output of a filter is the nominal output voltage required by the LD 1200.

3.15.4.9. Linear Regulator

The Linear Regulator provides the additional voltage regulation required for power supplied to LD 1200 logic circuits. It converts -12 volts from the Buck Converter to the -5 volt output.

3.15.4.10. Margin Controls

The Margin Control circuits enable the LD 1200 to vary a Power Supply output voltage ±5% of nominal under program control. Refer to the Margin Disables and Controls signal descriptions, in the Interface Signals subsection.

3.15.4.11. Overvoltage Protection

This circuit monitors the dc outputs of the Power Supply for an overvoltage condition. Detection of a voltage greater than 10% of the nominal value, for longer than 100 microseconds, causes the Shutdown Circuit to shut down all dc outputs.

After the unsafe condition is removed, Power Supply operation can be restored by setting the ac circuit breaker (at the rear of the LD 1200) to OFF, then to ON.

3.15.4.12. Undervoltage Protection

This circuit monitors the dc outputs of the Power Supply for an undervoltage condition. Detection of a voltage less than 10% of the nominal value, for longer than 100 microseconds, causes the Shutdown Circuit to shut down all dc outputs.

After the unsafe condition is removed, Power Supply operation can be restored by setting the ac circuit breaker CB1 (at the rear of the LD 1200) to OFF, then to ON.

3.15.4.13. Shutdown Circuit

When an unsafe condition in the LD 1200 or Power Supply is detected, this circuit inhibits the output of the Self-Oscillating Forward Converter, shutting down the dc outputs of the Power Supply.

3.15.4.14. Supply Operative Status

This circuit generates an error status signal to the Servo/Drive Control PCA when any of the dc outputs of the Power Supply drops out of the operating range. (Refer to the Supply Operative Status signal description in the Interface Signals subsection.)

3.15.4.15. Autotransformer

From filtered ac line input, the Autotransformer provides:

- 115 Vac to the fans in the Power Supply and LD 1200
- 115 Vac to the Motor Control for the Spindle Motor
- AC sense voltage to the Line Sync circuit

3.15.4.16. Power Supply Fan

The Power Supply Fan draws cooling air through the Power Supply, to maintain a safe operating temperature.

3.15.4.17. Motor Control

Depending on the state of the Brake/Motor Control signal, this circuit prevents or routes alternating current for the Spindle Motor to the Baseplate. (Refer to the Brake/Motor Control signal description in the Interface Signals subsection.)

3.15.4.18. Line Sync

When the input voltage to the Power Supply is equal to or greater than the minimum required, this circuit generates a sync signal to the Servo/Drive Control PCA. The signal has a 45% to 55% duty cycle and is at the same frequency as the ac input line.

3.15.4.19. Brake Solenoid Control

Depending on the state of the Brake/Motor Control signal, this circuit prevents or routes +12 Vdc for the Brake Solenoid to the Baseplate. (Refer to the Brake/Motor Control signal description in the Interface Signals subsection.)

3.15.4.20. Carriage Lock Solenoid Pick-Hold Circuit

Depending on the state of the Carriage Lock Control signal, this circuit prevents or routes +12 Vdc for the Carriage Lock Solenoid to the Baseplate. (Refer to the Carriage Lock Control signal description in the Interface Signals subsection.)

3.15.4.21. Interlock Solenoid Pick-Hold Circuit

Depending on the state of the Eject Disable signal, this circuit prevents or routes +12 Vdc for the Interlock Solenoid to the Baseplate. (Refer to the Eject Disable signal description in the Interface Signals subsection.)

3.15.4.22. Power Supply Temperature Sensor

This circuit monitors Power Supply ambient temperature. When the temperature reaches 65 degrees Centigrade, the circuit generates the Power Supply Temperature Warning signal to the Servo/Drive Control PCA as an early warning that Power Supply temperature is approaching the limit of safe operation.

3.16. OPERATOR PANEL

The functions of the Operator Panel are as follows:

- Display of diagnostic test results
- Indication of power-up
- Selection of Control Module and Slave Device addresses
- Control of Spindle Motor power-up and power-down
- Indication of LD 1200 ready state
- Write protection of Media

Signal descriptions of the Operator Panel are as follows (refer to figure 3-96):

(1) -WRT PROT SW - This signal is output to the Servo/Drive control PCA. It goes low when the WRITE PROTECT switch is depressed, causing the Media to be write protected.

(2) -STRT/STOP SW - This signal is output to the Servo/Drive Control PCA. It goes low when the START/STOP switch is depressed, allowing the Spindle Motor to power up or power down.

(3) +CM SW0, +CM SW1, and +CM SW2 - These three signals are output to the ICI PCA. Any of these signals goes high when the switch cap plug associated with that signal is present and inserted into the CONTROL MODULE ADDRESS receptacle socket associated with that signal. These signals specify the physical three bit address visually marked on the switch caps.

(4) +SLVE DEV SW0, +SLVE DEV SW1, and +SLVE DEV SW2 - These three signals are output to the ICI PCA. Any one or all three signals go high if the switch cap plug associated with that signal is present and inserted into the DRIVE ADDRESS receptacle socket associated with that signal. These signals specify the physical three bit address visually marked on the switch caps.

(5) +5V - This signal is generated by the Power Supply. It goes high when power is applied, causing the POWER indicator located with the CONTROL MODULE ADDRESS switch to illuminate. Illumination indicates that power is present in the LD 1200.

(6) -WRT PROT LED - This signal is generated by the Servo/Drive Control PCA. The WRITE PROTECT indicator is illuminated when this signal is low, indicating the Media has been write protected.

(7) -STRT/STOP LED - This signal is generated by the Servo/Drive Control PCA. The READY indicator is illuminated when this signal is low, indicating the ready state of the LD 1200.

(8) +5V - This signal is generated by the Power Supply. It goes high when power is applied, causing the POWER indicator located with the DRIVE ADDRESS switch to illuminate. Illumination indicates that power is present in the Drive.

(9) MSD - These four signals are generated by the ICI PCA. They can either be high or low, depending on the hexadecimal value to be displayed. They are used to represent the most significant digit on the hexadecimal display.

(10) LSD - These four signals are generated by the ICI PCA. They can either be high or low, depending on the hexadecimal value to be displayed. They are used to represent the least significant digit on the hexadecimal display.

(11) -ENBL OP DISP - This signal is generated by the ICI PCA. The hexadecimal display is enabled when this signal is low, allowing hexadecimal values to be displayed on the hexadecimal display.

Refer to the Operation section in this manual for further details on Operator Panel switch and indicator functions.

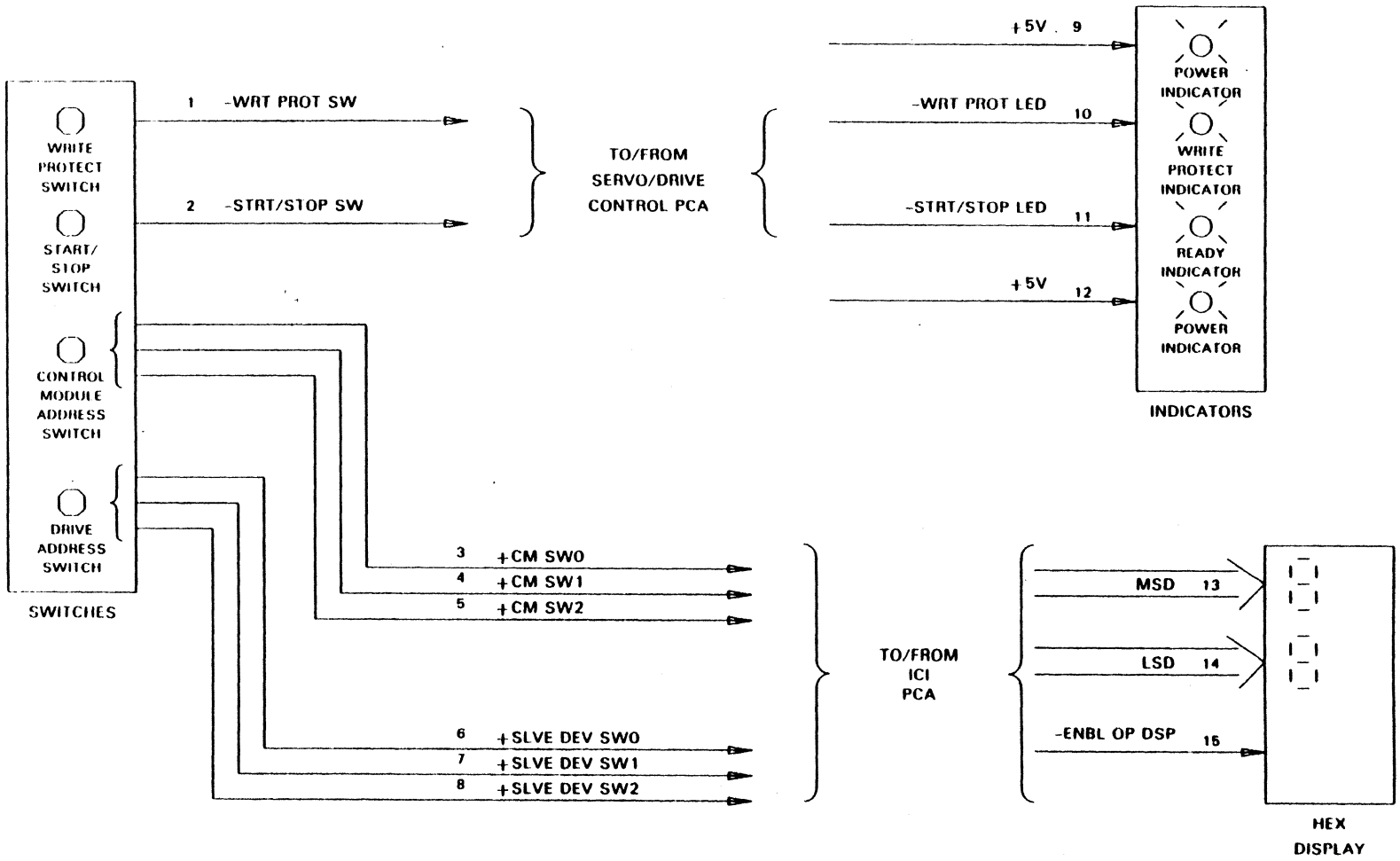


Figure 3-96. Operator Panel Block Diagram

Depressing the WRITE PROTECT or START/STOP switch sends a signal to the Servo/Drive Control PCA. In turn, the Servo/Drive Control PCA generates a signal illuminating the associated WRITE PROTECT or READY indicator. These indicators may be illuminated by other methods (refer to the Operation section for further details). During initial installation of the LD 1200, switch caps are press-fit onto the CONTROL MODULE ADDRESS and DRIVE ADDRESS receptacles. These caps are provided with up to three plugs that are inserted into up to three receptacle holes, causing signals to be sent to the ICI PCA. These signals specify the three bit address physically marked on the switch cap.

When a hexadecimal value such as a test result is to be displayed, a group of signals are generated by the ICI PCA. One signal enables the hexadecimal display. The others cause a physical representation of the hexadecimal value to be displayed.

When a test is run, the failure code that might result is sent to the data inputs of the Hexadecimal Display. During the running of the test, the display is disabled.

If a failure results, the Hexadecimal Display is enabled and the failure code is displayed. If a failure does not result, a successful completion code of "00" is displayed.

3.17. MAINTENANCE PANEL

The main purpose of the Maintenance Panel is to allow trained service personnel to run LD 1200 diagnostic tests without a Host CPU or external maintenance exerciser, facilitating field repair.

The Maintenance Panel can be divided into three main functional parts:

- Membrane Switch Panel
- Light Emitting Diodes (LEDs)
- Hexadecimal Display

These are shown in the Maintenance Panel Block Diagram (figure 3-97) included in this subsection.

Maintenance Panel signal descriptions are as follows (refer to the block diagram):

(1) -INCR MSD KEY - This signal is output to the ICI PCA. It goes low when the INCR MSD key is depressed, causing the most significant digit on the Hexadecimal Display to increment.

(2) -INCR LSD KEY - This signal is output to the ICI PCA. It goes low when the INCR LSD key is depressed, causing the least significant digit on the Hexadecimal Display to increment.

(3) -STRT STOP KEY - This signal is output to the ICI PCA. It goes low when the START STOP key is depressed, causing diagnostic test execution to start or stop. It is also used to increment a common memory address during display mode.

(4) -DISP MEM KEY - This signal is output to the ICI PCA. It goes low when the DISP MEM key is depressed, allowing entrance to or exit from display memory mode.

(5) -F1 KEY - This signal is output to the ICI PCA. It goes low when the F1 key is depressed, allowing diagnostic subfailure codes to be displayed on the Operator Panel Hexadecimal Display.

(6) -ENTER KEY - This signal is output to the ICI PCA. It goes low when the ENTER key is depressed, allowing the data byte currently displayed on the Hexadecimal Display to be saved.

(7) -CE MODE KEY - This signal is output to the ICI PCA. It goes low when the CE MODE key is depressed, causing entrance to or exit from CE mode.

(8) -SIA RESET - This signal is output to the ICI PCA. It goes low when the MASTER RESET key is depressed, causing a Power-On Reset test sequence to be executed.

(9) MSD - These four signals are operated by the ICI PCA. They can be either high or low, depending on the hexadecimal value to be displayed. They are used for physical representation of the most significant digit on the Hexadecimal Display.

(10) LSD - These four signals are generated by the ICI PCA. They can be either high or low, depending on the hexadecimal value to be displayed. They are used for physical representation of the least significant digit on the Hexadecimal Display.

(11) -ENBL MP DISP - This signal is generated by the ICI PCA. The Hexadecimal Display is enabled when this signal is low, allowing hexadecimal values to be displayed.

(12) -ENTER KEY LED - This signal is generated by the ICI PCA. The ENTER key LED is illuminated when this signal is low, indicating that the ENTER key has been depressed.

(13) -STRT/STOP KEY LED - This signal is generated by the ICI PCA. The START/STOP key LED is illuminated when this signal is low, indicating the START/STOP key has been depressed.

(14) -DISP MEM LED - This signal is generated by the ICI PCA. The DISP MEM key LED is illuminated when this signal is low, indicating that the DISP MEM key has been depressed.

(15) -CE MODE LED - This signal is generated by the ICI PCA. The CE MODE key LED is illuminated when this signal is low, indicating that the CE MODE key has been depressed.

(16) -F1 LED - This signal is generated by the ICI PCA. The F1 key LED is illuminated when this signal is low, indicating that the F1 key has been depressed.

(17) -MP PRESENT - This signal is output to the ICI PCA. When low, this signal indicates a Maintenance Panel is installed in the Drive and must be included in the normal polling process.

Refer to the Operation section in this manual for further details on Maintenance Panel switch and indicator functions.

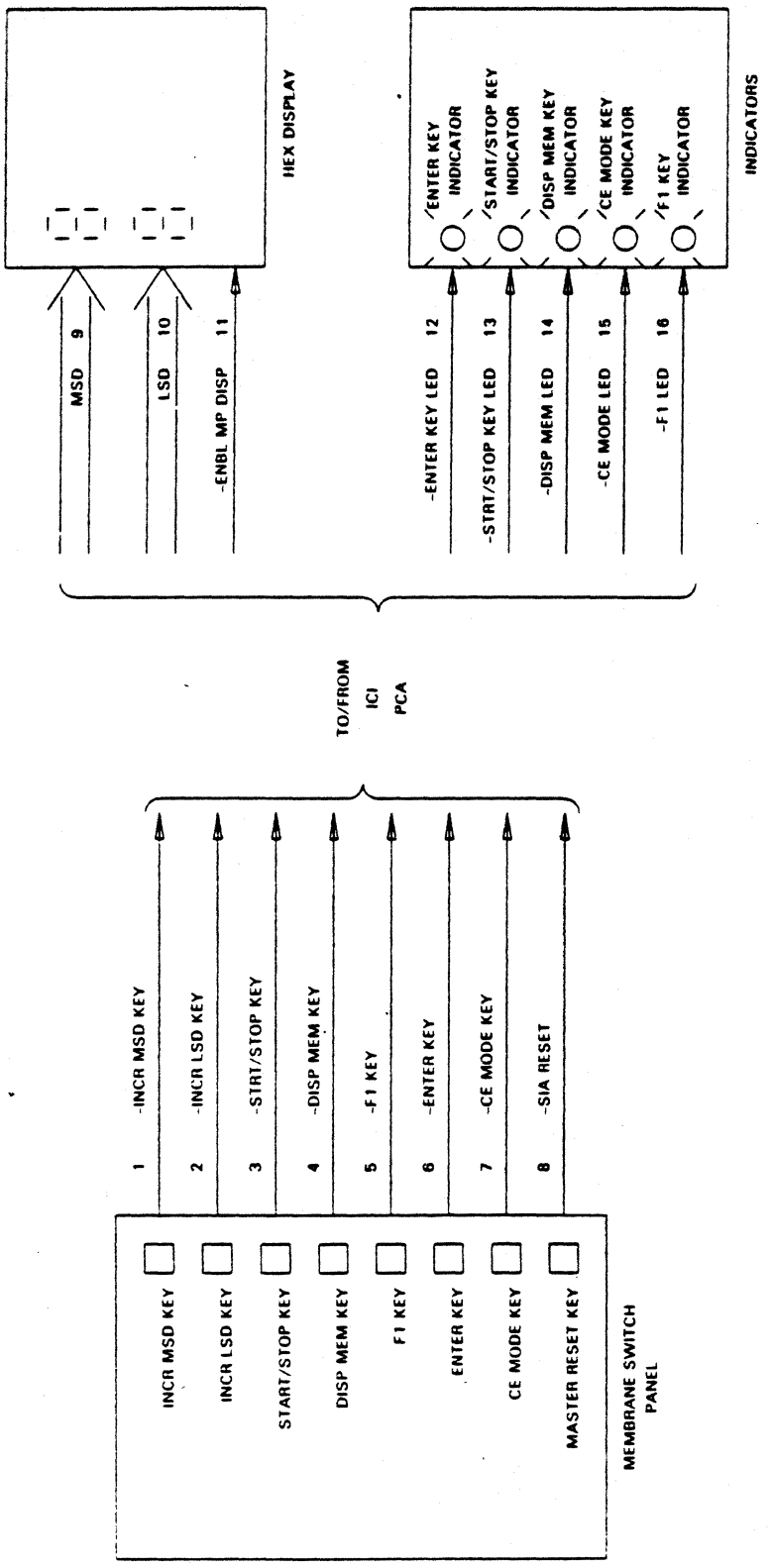


Figure 3-97. Maintenance Panel Block Diagram

Depressing any of the keys on the Membrane Switch Panel sends a signal to the ICI PCA. In turn, the ICI PCA generates a signal illuminating the associated LED.

When a hexadecimal value is to be displayed, the input value causes a signal to be sent to the ICI PCA. The ICI PCA, in turn, generates signals that are sent to the Hexadecimal Display. One signal enables the display, allowing it to illuminate. The others cause the physical representation of the input hexadecimal value to be displayed.

APPENDIX A. GLOSSARY

Absolute addressing	The ability to calculate where the laser beam should be positioned by subtracting or adding to the new address.
AC	Alternating Current (IPB only)
ac	Alternating Current (manuals)
AGC	Automatic Gain Control
AMP	Ampere(s) (IPB only)
AR	As required (IPB only)
ASSY	Assembly (IPB only)
Baseplate PCA	Baseplate Terminator PCA
Bus Master	SIA bus module capable of arbitrating for the SIA bus.
Bus Module	Circuitry which connects to and communicates via the SIA Bus.
Bus Slave	SIA bus module that cannot arbitrate for the SIA bus.
Byte	Eight bits of binary information; two nibbles; two TOON cells.
CAP	Capacitor (IPB only)
Carriage	The entire carriage assembly, including: ● Mechanical system: - Fine Servo Motor - Coarse actuator - Carriage Body ● Electronics system (Carriage Electronics PCA)

- Optical System:
  - Laser Pen
  - Quad Detector
  - Quarter Wave Retarder
  - Polarizing Beam Splitter
  - Fine Servo Motor and Three-Element Objective Lens

Carriage Body	Mechanical assembly on which the Carriage components are mounted.
Cartridge	The housing for the LD 1200 R/W Media.
CB	Circuit Breaker
CE	Customer Engineer
CHNL	Channel (IPB only)
CKT	Circuit (IPB only)
CM	Control Module
CMOS	Complimentary Metal Oxide Semiconductor
Coarse actuator	Also called Coarse Servo and Coarse Linear Actuator.
Command Descriptor Block	The structure used to communicate requests from an Initiator to a Target.
Common Memory	RAM data buffer on ECC PCA
Completion Status	One byte of information sent from the Target to the Initiator on completion of one command or a set of linked commands.
Connect	The function that occurs when an Initiator selects a Target to start an operation.
Control Module	Intelligent control logic that interfaces with the Host system via an external interface. Refers to the Internal Controller within the LD 1200.
Control Module ID	Control Module Identification
Control Store	ROM where COS and Diagnostic firmware reside.
COS	Command Operating System. The LD 1200 operational microcode.

Daisy-chained	Serial connection of multiple peripherals which requires termination of the last unit in the string.
DAC	Digital-to-Analog Converter
Data Buffer	The memory in the Internal Controller used for storage of all data transferred between the Host and the LD 1200 and between the Internal Controller and the Drive. This buffer allows the Internal Controller to conduct data transfers with the Host at a rate significantly faster than the Drive transfer rate.
Data Cartridge	Consists of a 12" diameter glass sandwich disk (Media) enclosed in a protective enclosure.
Data Field	The portion of the track from the Write Protect Bytes to the gap at the end of the sector.
DC	Direct Current (IPB only)
dc	Direct Current (manuals)
DES	Designator (IPB only)
DESCR	Description (IPB only)
Disconnect	The function that occurs when a Target releases control of the SCSI Bus, allowing the bus to go into the Bus Free phase.
Disk	The optical disk media
DP	Dual Port (IPB only)
Drive	That portion of the LD 1200 which controls and performs read, write, and control operations to the disk. It includes the following assemblies: ● Servo Drive Control PCA ● Modulator Demodulator Synchronizer PCA ● Read/Write Control PCA ● Error Signal Generator PCA ● Servo Systems PCA ● Carriage and associated electrical and mechanical assemblies
Drive Control Microprocessor	8039 microprocessor on the Servo/Drive Control PCA
Drive ID	Drive Identification
DRDW	Direct Read During Write. DRDW is the method used during the write cycle to verify that a data hole has been written in the

	Media as the result of a Write operation.
DMA	Direct Memory Access
ECC	Error correction code
ECC PCA	Error Correction and Common Memory Interface Unit PCA
ECL	Emitter–Coupled Logic
ECO	Engineering Change Order
ELEC	Electric(al) (IPB only)
EMA	Electromagnetic Assy (IPB only)
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EPROM	Erasable and Programmable Read–Only Memory
ESD	Electrostatic Discharge
ESG	Error Signal Generator
ESG PCA	Error Signal Generator PCA
Error	An abnormal condition, that can be corrected, which occurs during normal operation.
EXT	External
Failure Code	Two–character hexadecimal code displayed on the Operator Panel indicating a failure has occurred. Failure codes are described in the Structured Analysis Method Tables subsection of LD 1200 Hardware Maintenance Manual – Volume 1.
External Interface	The SCSI interface between the Host Adapter and LD 1200.
Fault	A malfunction from which the LD 1200 cannot recover.
FET	Field–Effect Transistor
FF	Flip–Flop
FIG.	Figure (IPB only)
Firmware	Control software residing in read–only memory (i.e., Command Operating System and Diagnostics)
Flag	Alterable bit used to signal a status condition that is set by hardware and interpreted by firmware.
Flaw	Media flaw information kept in the Flaw Table.

Focus actuator	A function of the Fine Servo Motor that controls the vertical position of the objective lens.
FPLA	Field Programmable Logic Array
FRU	Field replaceable unit
FSM	Fine Servo Motor used for focus and tracking purposes.
FT	Feet (IPB only)
FXD	Fixed (IPB only)
HD	Head (IPB only)
Header	Byte 0 to the first Write Protect Byte in the sector.
hex	Suffix used to denote hexadecimal values (e.g., 7F hex).
HEX HD	Hexagonal head, as on a screw (IPB only).
Host Adapter	The hardware and software required to interface the Host CPU with an external interface.
HZ	Hertz (IPB only)
Hz	Hertz (manuals): e.g., MHz, kHz, etc.
ICI PCA	Internal Controller Interface PCA (also known as LD 1200 SCSI Adapter PCA or SCSI PCA).
ID	Sector identification field in the Header.
ID	Inside Diameter (IPB only)
IDI	Internal Device Interface
INT	Internal (IPB only)
Internal Controller	This is the portion of the LD 1200 which consists of the ICI and ECC PCAs.
Internal Controller Interface PCA	Also known as LD 1200 SCSI Adapter PCA or SCSI PCA.
Initiator/Host	An SCSI Device (usually referred to as the Host) which requests an operation that is to be performed by another SCSI Device.
IPB	Illustrated Parts Breakdown
Jumpback	Controlled Seek during which the tracking actuator moves to the previous track at a specific sector, once per rotation, making the spiral track logically appear to be concentric circles.
Laser Diode	Laser (Light Amplified Stimulation of Electromagnetic Radiation)

Laser Pen	Assembly including Laser Diode and lenses.
LED	Light-emitting diode
LD 1200	OSI LaserDrive 1200 Intelligent Digital Optical Disk.
LKWSHER	Lockwasher (IPB only)
LOC	Location (IPB only)
Logical Unit	A physical or virtual device addressable through a Target.
Logical Unit Number	An encoded three-bit identifier for a Logical Unit.
LSB	Least-Significant Byte
LSD	Least-Significant Digit
MDS PCA	Modulator Demodulator Synchronizer PCA
Media	The physical medium in which data is stored by the optical disk.
Memory Map	Illustration showing the functional areas of memory and associated address ranges.
METR	Metric (IPB only)
Monohole	A hole prestamped or melted in the sensitive layer of the Media to represent recorded information.
Monohole Position	One of nine positions in a TOON cell in which a data hole can be melted (or prerecorded). Monohole positions are defined by zero-crossings of the disk clock.
MOS	Metal Oxide Semiconductor
MP	Maintenance Panel
MPU	Microprocessor. This refers to the microprocessor located on the SCSI PCA.
ms	Millisecond
MSB	Most-Significant Byte
MSD	Most-Significant Digit
MTBF	Mean Time Between Failure
MTTR	Mean Time To-Repair
NHA	Next Higher Assembly

Nibble	A four-bit binary pattern representing half a byte of information. For storage on the disk, a nibble is converted to a TOON cell (consisting of two monoholes within nine monohole positions).
NO.	Number (IPB only)
NM	Non metallic (IPB only)
ns	Nanosecond
OP	Operator Panel
Objective Lens	Three-element lens system used to focus the laser beam on the Media during the write cycle, and direct the reflected beam to the Quad Detector during the read cycle.
Operator Panel	The user-machine interface with the LD 1200 (not to be confused with the Maintenance Panel which is inaccessible to the operator).
Parity	Odd Parity: The sum of bits including parity is odd. Even Parity: The sum of bits including parity is even.
PC	Printed circuit (IPB only)
PCA	Printed circuit assembly
PCL	Power Control Loop
PIP	A PIP is the signal generated by the reflected light from a data hole that is forming.
PLA	Programmable Logic Array
PLL	Phase-Locked Loop, provides timing signals for the Read/Write Channel.
Ports	The addressable access to a device, e.g., IDI, SCSI, MPU ports.
Postfield	A field within the Data Field in a sector. It is used to flag obsolete data.
PROM	Programmable Read-Only Memory
Pseudowrite	LD 1200 attempts a write while laser power is disabled.
PWR	Power (IPB only)
Quad Detector	Converts data and servo information from the disk into electrical signals.
QTY	Quantity (IPB only)
RAM	Random Access Memory

Ramping	Sequence of increasing or decreasing steps in voltage with relation to Carriage movement (Carriage acceleration or deceleration).
Read/Write Channel	The paths taken by read and write data signals through the LD 1200 electronics. Refer to the LD 1200 Functions subsection of the Peripheral Equipment Reference Manual for more information.
Reconnect	The function that occurs when a Target selects an Initiator to continue an operation after a Disconnect.
REF	Reference (IPB only)
Rewrite	Also called Automatic Rewrite or Retry. When a Write operation is aborted, the operation is attempted again in the next sector, if authorized by the Host.
RFI	Radio frequency interference (IPB only)
RG	Ring (IPB only)
R/W	Read/Write
ROM	Read-Only Memory
RTZ	Return to Zero
R/WC PCA	Read/Write Control PCA
SAM	Structured Analysis Method. Troubleshooting information provided in LD 1200 Hardware Maintenance Manual - Volume 1 for fault isolation.
S/DC PCA	Servo/Drive Control PCA
SCR	Screw (IPB only)
SCSI	Small Computer System Interface
SCSI Address	The Octal representation of the unique address (0 through 7) assigned to an SCSI Device. This address is normally assigned and set in the SCSI Device during system installation (refer to the Initial Start-Up Procedures subsection in LD 1200 Hardware Maintenance Manual - Volume 1.
SCSI Device	A Host Adapter, peripheral controller, or intelligent peripheral, such as the LD 1200, which can be attached to the SCSI Bus.
SCSI ID	The bit-significant representation of the SCSI Address referring to one of signal lines DB7 through DB0.
SCSI Terminator Assembly	Electrical terminator required at the last unit on an SCSI Bus to terminate the bus. If the last unit on the bus is a LD 1200, two SCSI Terminator Assemblies are plugged into sockets on the SCSI PCA.

SCSI PCA	LD 1200 SCSI Adapter PCA (also known as Internal Controller Interface PCA or ICI PCA).
Sector Mark	The first four bytes in each sector.
Sector Mark Pulse	Denotes the beginning of a sector.
Servo Control	8031 microprocessor on the Servo/Drive
Microprocessor	Control PCA
SEQ	Sequence (IPB only)
SIA Bus	System Interface Assembly Bus
Signal Assertion	A signal driven to the true state by an SCSI Device.
Signal Negation	A signal either driven to the false state by an SCSI Device or biased to the false state by cable terminators.
Signal Release	A signal that is not driven to the false state by an SCSI Device, but that is biased to that state by cable terminators.
SPG	Spring (IPB only)
SPL	Split (IPB only)
SS PCA	Servo Systems PCA
Subfailure Code	Two-character hexadecimal code which can be displayed on the Operator Panel to provide additional information on a failure. Subfailure codes are described in the Structural Analysis Method (SAM) Tables subsection of LD 1200 Hardware Maintenance Manual - Volume 1.
SW	Switch (IPB only)
Sync	Synchronize
T	Tooth (IPB only)
Target	An SCSI Device (usually referred to as the LD 1200) that performs an operation requested by an Initiator.
THD	Thread (IPB only)
TOG	Toggle (IPB only)
TOON cell	Nine consecutive positions in a track on the disk, defined by nine consecutive zero crossings of the prerecorded disk clock, in which header information or data is encoded. Information is encoded as two monoholes in a TOON cell.
TOON code	Two-out-of-nine code used to physically record data in the Media.

TPG	Tapping (IPB only)
Tracking actuator	A function of the Fine Servo Motor that controls the radial, or horizontal, position of the objective lens.
TTL	Transistor-to-Transistor logic
V	Volts (IPB only)
Vector Address	A field within in the Data Field in a sector. It is used to ensure data integrity.
VCO	Voltage-controlled oscillator
WAIT State	Microprocessor halts, pending execution of the current command.
WSHR	Washer (IPB only)
Z80	Tradename for the microprocessor used in the ICI PCA.