DDP-24

INSTRUCTION MANUAL

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INSTRUCTION MANUAL
DDP-24 GENERAL
PURPOSE COMPUTER

August 1964

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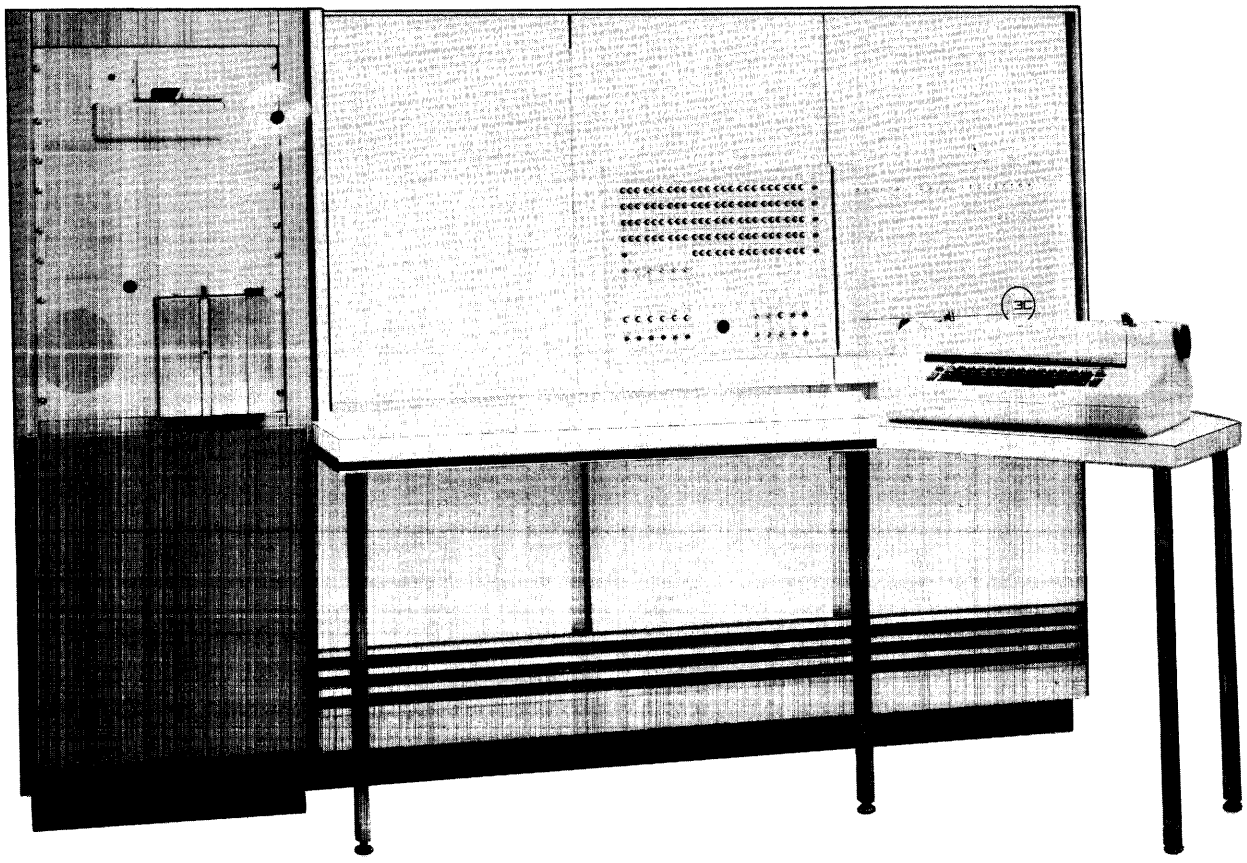
DDP-24 GENERAL PURPOSE COMPUTER



SECTION I
INTRODUCTION

1-1 GENERAL

This manual provides basic, comprehensive instruction for the DDP-24 General Purpose Digital Computer and its peripheral equipment, manufactured and assembled by Computer Control Company, Inc., Framingham, Massachusetts. The information includes a description of the system, installation procedures, operating instructions, detailed principles of operation and maintenance procedures.

1-2 GENERAL DESCRIPTION

The DDP-24 is a high-speed, solid-state, general-purpose digital computer for real-time, on-line, and scientific data processing.

The computer is completely transistorized, has a 24-bit word length, and has a sign magnitude code to represent positive or negative numbers. The expandable magnetic core memory stores both program instructions and data resulting from computer operations. Parallel logic, a fast memory cycle, and a comprehensive instruction repertoire make high-speed operation possible. The processor uses binary logic. The command format is single address and single operation with index and indirect addressing flags. The computer's capabilities are easily expanded by the addition of optional equipment or they may be adapted to special requirements. Typical options include additional input-output channels and interrupt lines, priority interrupt, and an increased memory capacity. Standard input-output capabilities consist of three input-output channels including a buffered character channel that can operate in either the input or the output mode; a parallel input channel, and a parallel output channel.

Other optional or peripheral devices include high- and low-speed magnetic tape units, medium- and high-speed line printers, adapters for IBM card input and output units, plotters, paper-tape spoolers, and remote input-output consoles. Other easily connected peripheral devices are oscilloscopes, disc memories, drum memories, data phones, analog-to-digital and digital-to-analog converters, multiplexers and distributors, teletype, and special instruments.

1-3 DETAILED DESCRIPTION

The DDP-24 Model 24-00, shown in Figures 1-1 through 1-3, contains all the parts of a standard computer in one 4-bay cabinet. The computer elements are distributed within the bays as indicated in Table 1-1.

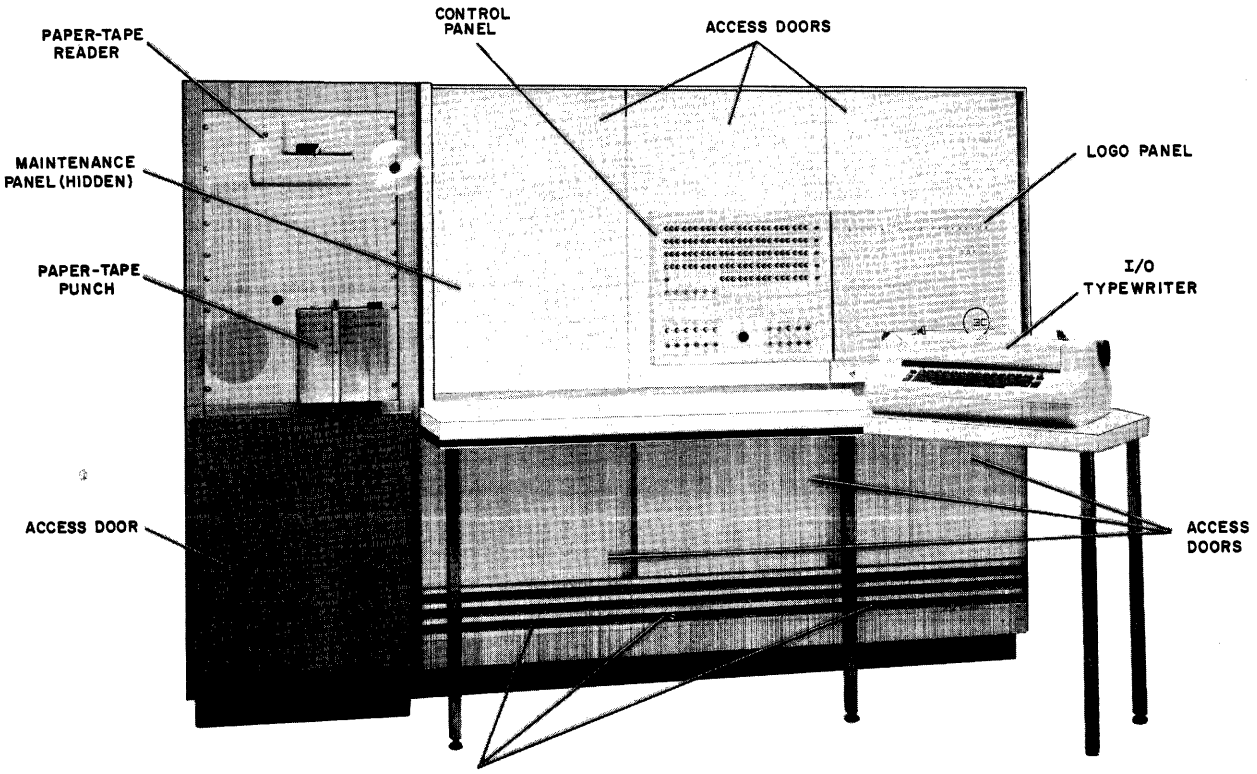


Figure 1-1. DDP-24 Front View with Access Doors Closed

TABLE 1-1
COMPUTER COMPONENT DISTRIBUTION

Bay 1	Bay 2	Bay 3	Bay 4
Tape Reader -2.5, -24, and -100 VDC Power Supplies Tape Punch TCM-32 Memory	RP-32 Power Supply AU S-BLOCs (7) Maintenance Panel Power Distribution Panel Blower	CU S-BLOCs (4) Control Panel Blower	RP-32 Power Supply I/O S-BLOCs (4) Connector Panel Blower

1-3.1 Bay 1

1-3.1.1 Tape Reader. — The tape reader is a unidirectional perforated-tape device which reads eight data channels (including parity) plus a sprocket hole channel at the rate of 30 inches per second (10 characters per inch or 300 characters per second). A pulsed mode is provided to allow for off-line operation of the tape reader with a typewriter and/or a paper tape punch. In the pulsed mode, the reader stops after every character and consequently reads at a much lower average speed.

The unit uses standard paper or mylar tapes (black paper recommended) 0.004 to 0.005 inches thick.

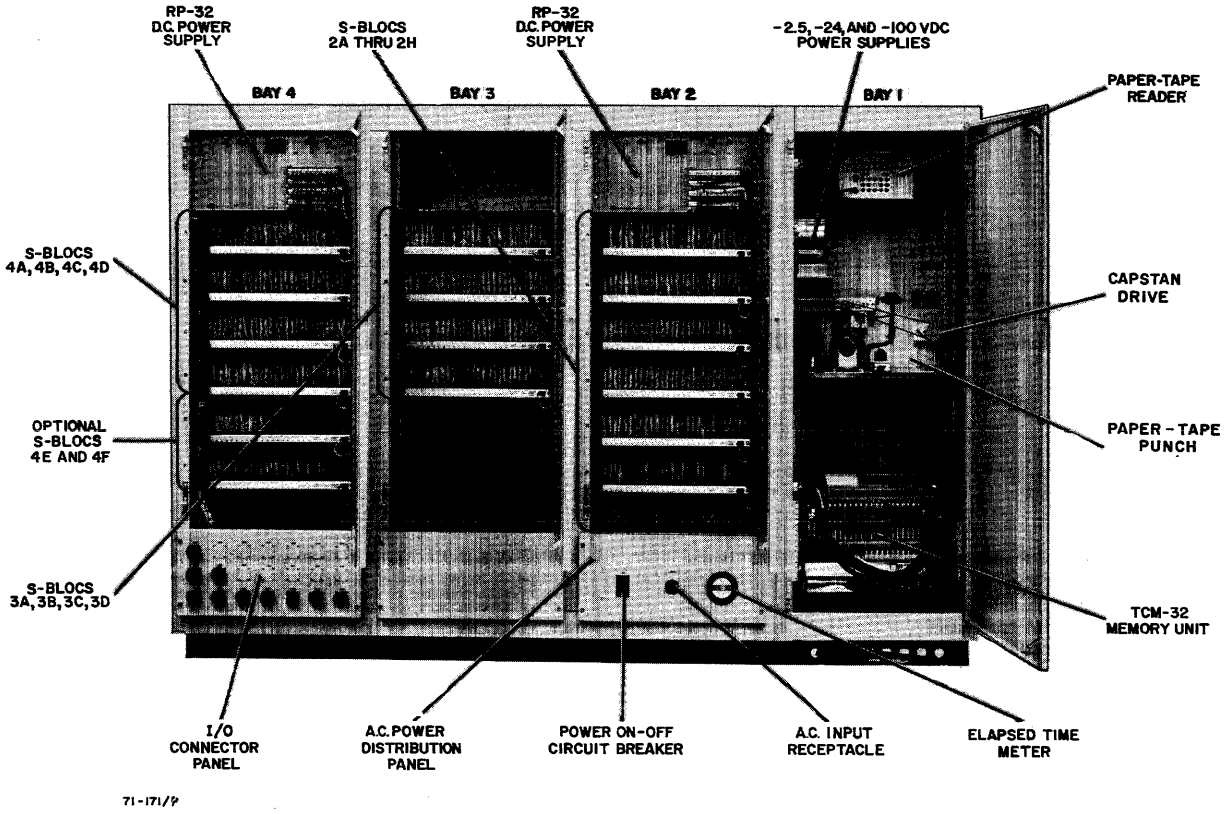


Figure 1-2. DDP-24 Rear View with Access Doors Open

1-3.1.2 Tape Punch. - This is a self-contained, high-speed unit capable of perforating 8-channel paper recording tape at rates up to 60 characters per second. The unit is asynchronous and can be operated at any speed below its maximum because the punching of each character is initiated by a separate, independent pulse. These pulses can be fed to the perforator at any rate provided the interval between characters is not less than 16-2/3 ms.

The 0.05-HP drive motor within the perforator requires a power source of 105 to 125 volts at 60 cps and 1.7 amperes. The escapement assemblies for the capstan drive and punch drive mechanisms require pulses of 4.5 ± 0.5 ms duration and -24 volts ±10 percent amplitude. One pulse must be supplied for each movement of the tape and one pulse is required for each character to be punched (the character pulse). Punch pulses for all eight channels are derived from the character pulse.

The paper take-up reel is rotated by a differential gear and clutch mechanism mounted on the back, center, left, of the bay-1 front panel and is driven by a belt from the capstan drive mechanism.

1-3.1.3 Memory. - Magnetic Core Memory TCM-32 (Figures 1-2 and 1-3), is a random access 4096-word memory, and is a standard product of Computer Control Company. It is housed in a tilt-drawer unit, a unique design for efficient and easy maintenance.

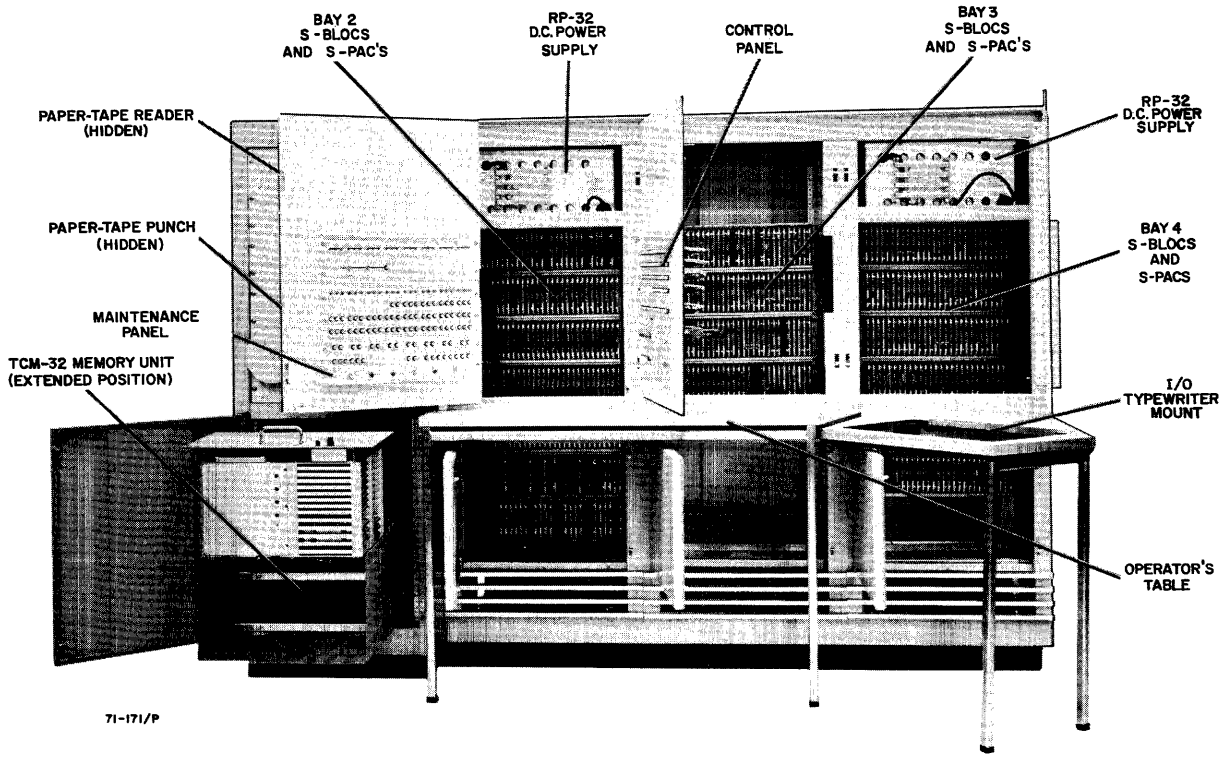


Figure 1-3. DDP-24 Front View with Access Doors Open

1-3.1.4 -100 VDC Power Supply. - This unit is located (Figure 1-2) on the same mounting as the -24 VDC power supply. It is compact (3-5/8 x 6-1/4 x 6-1/4 inches) and provides not only -100 VDC but also the -2.5-VDC bias voltage for the transistorized switch indicators used in the standard DDP-24.

1-3.1.5 -24 VDC Power Supply. - This unit is located (Figure 1-2) on the same mounting as the -100 VDC power supply and provides the -24 VDC to the power distribution relays.

1-3.2 AU Assembly, Bay 2

1-3.2.1 S-BLOCS (BL-33). - Seven S-BLOCS house the S-PACs used in the AU Assembly. Figures 1-2 and 1-3 show their location.

1-3.2.2 -18, -6, and +12 VDC Power Supply. - The location of the -18, -6, and +12 VDC power supply, Model RP-32, is shown in Figures 1-2 and 1-3. This subassembly provides the power required by the S-PACs.

1-3.2.3 Power Distribution Panel. - This panel contains an AC input receptacle, circuit breaker switches, relays, transformers and connectors to monitor and distribute 115 VAC to various sections of the DDP-24. An elapsed-time meter, Figure 1-2, provides visual monitoring of the total number of hours that the DDP-24 has been energized. Refer to the Maintenance Section (Section VI) of this manual for the electrical schematic of the panel.

1-3.2.4 Maintenance Panel. - This panel (Figures 1-1 and 3-2) provides switches, indicators, and switch-indicators to permit rapid isolation of faults. A detailed explanation of the panel is provided in Section VI. Refer to the Maintenance Section (Section VI) of this manual for the electrical schematic of the panel.

1-3.2.5 Blower Unit. - The Blower Unit is one of three used in the DDP-24. It provides filtered forced-air cooling to all of the subassemblies of the AU Assembly.

1-3.3 CU Assembly, Bay 3

1-3.3.1 S-BLOCS. - Four S-BLOCS, Model BL-33, (Figures 1-2 and 1-3) house the S-PACs used in the CU Assembly.

1-3.3.2 Control Panel. - This panel (Figures 1-1 and 3-1) provides switches, indicators, and switch-indicators to facilitate manual or automatic control of the DDP-24 functions. A detailed explanation of the panel is provided in paragraph 3-2. Refer to the Maintenance Section (Section VI) of this manual for the electrical schematic of the panel.

1-3.3.3 Blower Subassembly. - Refer to paragraph 1-3.2.5.

1-3.4 I/O Assembly, Bay 4

1-3.4.1 S-BLOCS. - Four S-BLOCS, Model BL-33, (Figures 1-2 and 1-3) house the S-PACs used in the I/O Assembly.

1-3.4.2 -18, -6, and +12 VDC Power Supply. - This power supply is similar to the AU power supply.

1-3.4.3 Connector Panel. - The connector panel (Figure 1-2) provides input and output routing of data to and from the peripheral equipment. Section II provides text and tabular data covering the connector panel.

1-3.4.4 I/O Typewriter. - A 15-character-per-second typewriter (IBM Series 73 Selectric) (Figure 1-4) is provided to communicate with the computer via the input-output character buffer. The typewriter is compact, light weight, binary-coded-decimal (BCD),

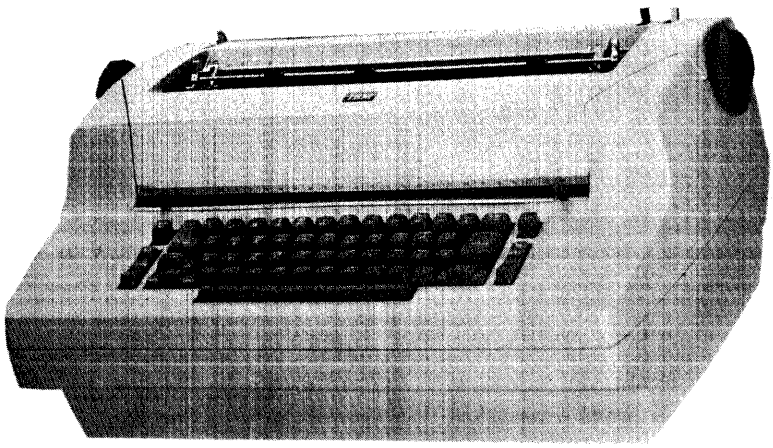


Figure 1-4. Input-Output Typewriter

and uses a type head and keyboard arrangement designed primarily for use with the computer. It has a 15-inch carriage with a 13-inch writing line; the ribbon mechanism has three ribbon lift positions and a stencil position. Both ribbon and spool are contained in a snap-in cartridge to allow rapid replacement.

A selection mechanism is used during input and output operations. When the typewriter is used as an output device, data flow is from computer to typewriter and the mechanism selects the character to be printed. During manually initiated input operations, data flow is from typewriter computer and contacts in the selection mechanism transmit pulses that define the character being printed. Magnets are used in the mechanism; impulsing a magnet causes a character to be selected and printed. The drive motor within the typewriter operates at 115 volts, 60 cps, at an operating current of 1.0 amperes.

1-4 REFERENCE DATA

Table 1-2 lists quick reference data for the standard DDP-24, Model 24-00.

Tables 1-3 through 1-6 list the specifications of the major options.

1-5 APPLICABLE PUBLICATIONS

The following documentation is supplied with the standard DDP-24 (Model 24-00). If optional peripheral equipment is obtained, adequate documentation will be provided.

DDP-24 Interface Manual
DDP-24 Systems Programs
DDP-24 Reference Manual
Service Manual
DIP/DAP Coding Forms
Interpretive Program (DIP)
Executive Control Program (DEP)
Fortran II Manual

DDP-24 Conversion Tables
DDP-24 Programmer's Reference Cards
DC Power Supply Instruction Manual
Tape Perforator Manual
Perforated Tape Reader Manual
Typewriter Instruction Manual
DDP-24 Test Tapes
Instruction Manual for Magnetic Core Memory TCM-32

Detailed description of operation and procedures for installation and maintenance of the Model TCM-32 Magnetic Core Memory are provided in the Instruction Manual for that unit. Depending upon the type of peripheral and/or optional equipment obtained, some or all of the following documents will be supplied.

Instruction Manual for S-PAC Digital Modules
Instruction Manual for 1-MC S-PAC Digital Modules
Instruction Manual for Perforated Tape Reader
Instruction Manual for Tape Perforator
Instruction Manual for Electric Typewriter
Maintenance Manuals for Magnetic Tape Transports

1-6 EQUIPMENT SUPPLIED

Table 1-7 lists the main and auxiliary equipment supplied with the standard DDP-24, Model 24-00.

Table 1-8 lists the PAC complement of the standard DDP-24, Model 24-00.

TABLE 1-2
DDP-24 MODEL 24-00 SPECIFICATIONS

Type: Parallel binary, solid state

Addressing: Single address with indexing and indirect addressing; hardware index register

Word Length: 24 bits

Machine Code: Sign-magnitude

Memory Type: Coincident current ferrite core; non-destructive storage

Memory Size: 4,096 words, expandable to 32,768 words, all directly addressable

Memory Cycle Time: 5 μsec

Memory Access Time: 3 μsec

Speed: Addition - 10 μsec
Multiplication - 31 μsec
I/O word transfer - 5 μsec
I/O block transfer - 166,000 words per second

Standard Peripheral Equipment: 300 CPS photoelectric paper-tape reader, with continuous and pulsed modes of operation; 60 CPS paper-tape punch; 15 CPS electric typewriter for input and output. Off-line paper-tape preparation and printout.

Input-Output Channels: Character buffer for both input and output, with parity, up to 6 bits. Parallel 24-bit input channel. Parallel 24 bit output channel. Additional character buffers and parallel channels with or without flip-flop register optional. Word-forming buffers, direct memory access channels and fully buffered channels optional.

Input-Output Modes: Program controlled input-output (Ready Mode), Automatic Interrupt. (Input-output channels can be connected to operate in either the Ready or Automatic Interrupt Mode)

TABLE 1-2 (Cont)

Block Transfer: Fill memory block command (FMB). Dump memory block command (DMB). Single line sense input and output control signals. Direct memory access channel optional. Fully buffered channel optional . Priority interrupt optional.

Circuitry: Standard one megacycle 3C S-PAC digital modules

Signal Levels: Zero volts for logical ZERO; -6 volts for logical ONE. All inputs are diode coupled/isolated. All output circuits are clamped.

Dimensions: 7 feet 8 inches x 3 feet 3 inches x 5 feet 1 inch high

Weight: 2,000 lbs

Power: 2,000 watts, single phase, 115 ± 10 volts, 58 to 62 CPS. Data is preserved in the event of power failure

TABLE 1-3
LINE PRINTER CHARACTERISTICS

Speed: 300 lines per minute

Physical Drum Speed: 360 rpm

Print Positions: 120 print positions per line. Number of print positions optional from 12 to 132 in twelve position increments

Ribbon: Conventional one inch horizontal tabulating ribbon

Paper Feed: Dual tractor paper feed. (1/2 inch hole centers)

Forms: Printer accepts standard forms up to 19 inches

Print Area: 12 inches width in center of 19-inch feed area

Character Per Inch: 10

Maximum Available Number of Characters Per Print Drum Revolution: 64

Paper Line Advance Time: 30 ms

Paper Shift Feed: 20 inches per second

Character Synchronization and Timing: Eight channel optical code disc

Line to Line Spacing: 0.167 ± 0.015 inch; 6 lines per inch

Paper Capabilities: Up to 6 parts, 12 lb. bond with "single shot" carbon, or tabulating card (0.007 inch) plus second record sheet

Character Type: Open Gothic or compatible font

Horizontal Character Spacing: 0.100 ± 0.010 inch between centers

Electrical Interface: Serial interface. A Soniline is used as a serial buffer.

Line Printer Interface: Connection to any 24 bit output channel (buffered or unbuffered), parallel output channel, DMA, or FBC.

TABLE 1-4
CARD READER CHARACTERISTICS

Serial Feed: Reads cards column by column

Speed: 200 cards per minute. Reads first column within 85 ms

Hopper Capacity: 500 cards

Information Signals: Ground and -12 volts DC (20 milliamperes). Information levels 300 μsec minimum duration. Strobe signals 80 per card, 15 μsec duration

Control Signals:

(a) Signals in

Start Card cycle
Binary/Alphanumeric
Reads Hollerith code from card and translates data to binary before entrance into the DDP-24 memory.
Binary/Upper-Lower
Signal (OCP) enters two binary characters per column (maximum of 160 binary characters per card) into memory.
Check For Validity

(b) Signals out

Ready Condition
Card Cycling
Read Check
Feed Check
End-of-File
Continue Level

Optical Reading: Precise read timing attained through the use of synchronized strobing of each column

Demand Feed: Immediate access clutching. Card read signal from external control source within 10 ms intervals causes no loss of speed

Validity Check Circuits: Check combination of holes in card columns for 64 valid codes

OCP Signals: With one OCP signal reads:
(a) Pulsed (one card at a time before deselected) or Continuous,
(b) Binary and/or Hollerith card

SKS Signals:
(a) CARD RDR BSY
(b) INVALID CODE or INTERNAL ERROR
(c) STOP CODE (End of File or Stop Code)

The card reader and its interface can be connected to every buffered channel: (character buffer (in), DMA, or FBC channels).

TABLE 1-5
45 IPS MAGNETIC TAPE UNIT CHARACTERISTICS

Tape:
- Width: 1/2 inch
- Reels: 10-1/2 inch
- File protect ring
- IBM compatible

Tape Speed:
- Forward: 45 inches per second
- Reverse: 45 inches per second
- Rewind: less than 3 minutes for complete tape
- Start Time: less than 5 ms
- Stop Time: 1.5 ms

Recording Density:
- Dual density
- High: 556 characters per inch
- Low: 200 characters per inch

Head:
- 7 tracks
- Separated Read and Write elements in same head
- Possible to read while writing (check back)
- Distance between read and write element 0.3 inch

Recording Format:
- IBM compatible
- NRZI: non return to zero, change on ONE
- 6 data tracks
- 1 track for parity bits
- Inter-record gap is 3/4 inch
- Loadpoint: beginning of tape: reflective spot (photo sense element)
- End of tape: reflective spot (photo sense element)

Control Signals From Computer:
- Read ONE record (forward) BINARY CODE
- Read ONE record (forward) BCD CODE
- Write ONE record (forward) BINARY CODE
- Write ONE record (forward) BCD CODE
- Forward one record - no information reading takes place
- Forward until file mark - no information reading takes place
- Backspace one record - no information reading takes place
- Backspace until file mark - no information reading takes place
- Rewind to loadpoint
- Write file mark

Note

The tape never stops in the middle of a record. A built-in gap detection circuit automatically stops the tape in a gap (or at a file mark).

Modes:
- Automatic: connected to computer (See control signals.)
- Manual: under pushbutton control
  - Rewind button
  - Reverse button
  - Forward button

The magnetic tape unit can be connected to a character buffer or to a WFB (word-forming buffer). A WFB can be connected to an I/O channel, DMA, or FBC channel.

TABLE 1-6
CARD PUNCH CHARACTERISTICS

Speed: 100 cards per minute

Feed: Row by row punching. Corner turning from column by column to row by row done by program.

OCP Signals: Start card cycle

SKS Signals:
CARD PUNCH BUSY (-6 volt for entire punching of one card)
ROW PRINT READY
CARD PUNCH ERROR

Punch prints row by row. Before every row punching, an 80-bit (serial input-parallel out) buffer has to be filled with information bits from the computer. The buffer is filled with 14 groups of six bits (most significant bit first). In the 14th group of 6 bits, the 4 least significant bits are ignored. The punch can be connected to any buffered channel of the DDP-24 (character buffer, DMA, or FBC).

TABLE 1-7
STANDARD DDP-24 UNITS

Quantity	Item	Mfg.	Model
1	3 bay enclosure	Electronic Enclosures	
1	1 bay enclosure	Electronic Enclosures	
15	S-Blocs	3C	BL-31
1	BS Unit	3C	TCM 32
2	Power Supply	3C	RP-32
1	Power Supply, +28-VDC	Dressen Barnes	21-103
1	Power Supply, -90-VDC	TEC	LPS 102 B
1	External Connector Panel	Electronic Enclosures	
1	Input Power Panel	Electronic Enclosures	
1	Control Panel	Electronic Enclosures	
1	Maintenance Panel	Electronic Enclosures	
1	Logo Panel (nameplate)	Electronic Enclosures	
1	Paper Tape Punch	Tally Corp.	420
1	Paper Tape Reader	Digitronics	2500
1	I/O typewriter	IBM	IBM 735
3	Blower units	Robbins and Myers Mfg.	703A
415	S-PACs	3C	(See Table 1-8)
1	Blank Panel	Electronic Enclosures	

TABLE 1-8
STANDARD DDP-24 PAC COMPLEMENT

Type	Description	Processor	Memory	Total
DI-30	NAND Type 2	98	4	102
DF-30	Parallel NAND Type 1	6	0	6
ST-30	Schmitt Trigger	2	0	2
DN-30	NAND Type 1	48	1	49
FA-30	Gated Flip-Flop	17	1	18
DL-30	NAND Type 3	26	0	26
DM-30	Delay Multivibrator	7	0	7
S-006-AD	Component Board	1	0	1
SD-30	Solenoid Driver	7	0	7
PN-30	Non-inverting Power Amp.	17	2	19
MV-30	Multivibrator Clock	1	0	1
DJ-30	Parallel NAND Type 2	60	0	60
DC-30	Diode PAC	7	0	7
OD-30	Octal/Decimal Decoder	7	0	7
UF-30	Universal Flip-Flop	12	0	12
SN-30	System Normalizer	1	0	1
MC-30	Master Clock	1	0	1
PA-30	Power Amplifier	5	0	5
MF-30	Multipurpose Flip-Flop	25	0	25
S-105	Adder PAC	23	0	23
FF-30	Basic Flip-Flop	0	3	3
TD-30	Timing Distributor	0	2	2
S-117	Address Decoder	0	4	4
S-139	Component Board	0	1	1
S-086	Bit Register	0	12	12
S-026	Selection Switch	0	8	8
S-091	Gate Driver	0	1	1
S-083	Dynamic Current Driver	0	2	2
S-087	Inhibit Driver	0	3	3
	TOTALS	371	44	415

SECTION II
INSTALLATION

2-1 INTRODUCTION

This section contains the necessary information for installation and initial testing of the DDP-24 General Purpose Computer and its major peripheral equipment. Included are installation dimensions, environmental data, power requirements and general installation information for the major optional equipment. Specific test and installation procedures for the optional devices are supplied with the device. Variation of these data may be necessary for the adaption of specific functions or equipment requirements.

2-2 EQUIPMENT SUPPLIED

2-2.1 Standard DDP-24 (Table 2-1)

Normally, all assemblies, except the I/O typewriter and table, are mounted and the internal connections are made before shipment. The I/O typewriter and table are packed separately to prevent damage during shipment. Refer to Figure 2-1, Standard DDP-24 Installation drawing for bay locations.

2-2.2 Auxiliary Cabinets

The physical dimensions of a single auxiliary equipment cabinet are shown in Figure 2-2. This cabinet is used to mount optional or additional equipment. Double auxiliary cabinets are supplied with some systems. The auxiliary cabinets may be physically connected to the standard computer or located separately and electrically connected by cable. The cable connectors are mounted on the rear panel of the unit. (See Figure 2-8.) A maximum of 21 connectors can be mounted on each unit.

TABLE 2-1
EQUIPMENT SUPPLIED

Quantity	Description	Mfg. Desig.	Dimensions	Weight
1	DDP-24 consisting of:		61-9/16 in. x 92 in. x 39 in.	2000 lb
1	3 Bay Enclosure			
1	1 Bay Enclosure			
15	S-BLOCs	BL-33		
1	Memory Unit	TCM-32		
2	Power Supply	RP-32		
1	Power Supply	Dressen Barnes Model 21-103		
1	Power Supply	Teclite 1390A		
1	Connector Panel (Bay 4)			
1	AC Connector Panel (Bay 2)			
1	Control Panel			
1	Maintenance Panel			
1	Paper Tape Perforator	Tally Model 420		
1	Paper Tape Reader	Digitronics Model 2500		
1	I/O Typewriter	IBM Series 73		
3	Blower Units			
1	AC Power Cable		15 ft.	

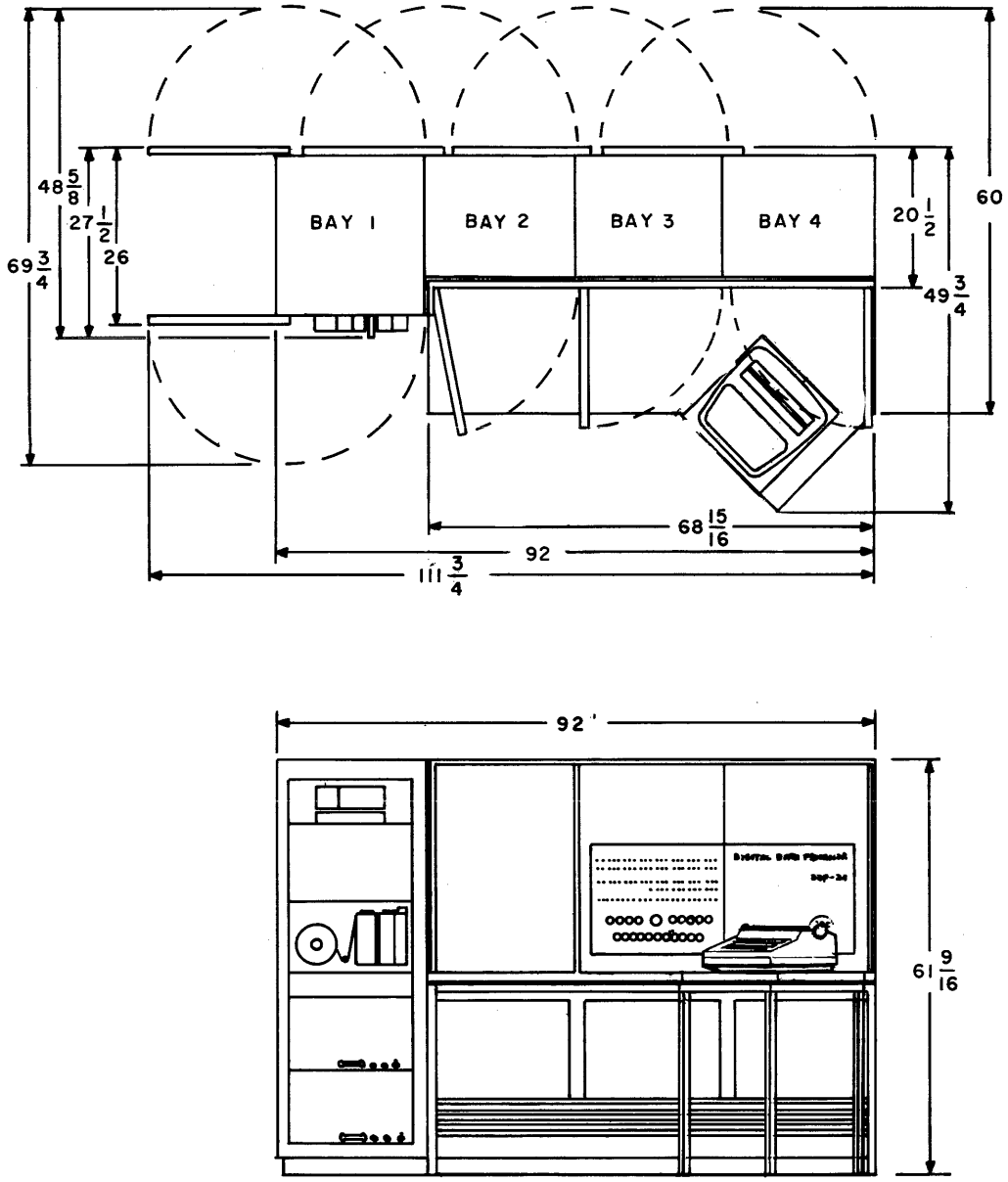


Figure 2-1. Standard DDP-24 Dimensions

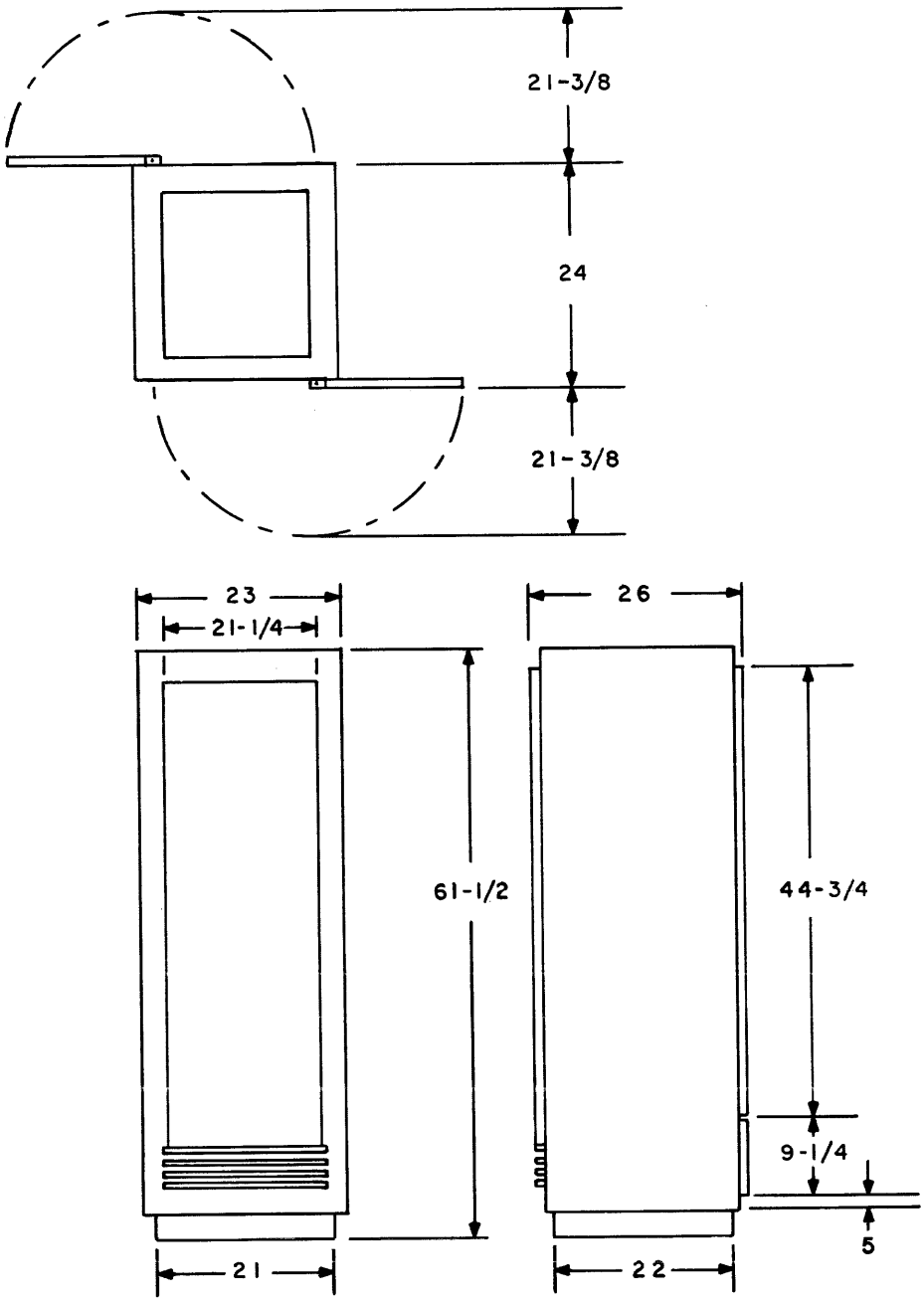


Figure 2-2. Auxiliary Equipment Cabinet Dimensions

2-2.3 Optional Peripheral Equipment

The standard DDP-24 can be complemented by several peripheral devices to extend its capabilities. These devices may be installed with or after the initial installation. Table 2-2 lists the physical characteristics and power requirements of the major peripheral devices, the outline dimensions of which are shown in Figure 2-3 through 2-6. Also available for use with the standard DDP-24 are a digital plotter, and a magnetic tape unit and transport with a speed of 75 inches/sec.

TABLE 2-2
MAJOR OPTIONAL PERIPHERAL EQUIPMENT

Unit	Dimensions			Weight	Power (Single-phase, 3-wire)	
	Height (inches)	Width (inches)	Depth (inches)	(pounds)	Type	(Watts)
Line Printer	40	39	21	400	115 ±10 V, 60 ±2 CPS	750
Card Reader	41	17-3/4	30	250	115 ±10 V, 60 ±2 CPS	345
Card Punch	53	44-1/2	28	1200	220 ±20 V, 60 ±2 CPS	2200
Magnetic Tape Unit (45 IPS)	72	26	25	Single = 900 Dual = 1500	115 ±10 V, 60 ±2 CPS	3000

CAUTION

In DDP-24 installations that include the Card Punch and Magnetic Tape Unit, the AC power distribution of the installation site should provide one input for the DDP-24 and a separate input for all peripheral equipment to prevent circuit overloading.

2-2.4 Maintenance Equipment

Table 2-3 lists the equipment needed for normal service of the DDP-24. Maintenance equipment required for an optional device is listed in the manual for that device.

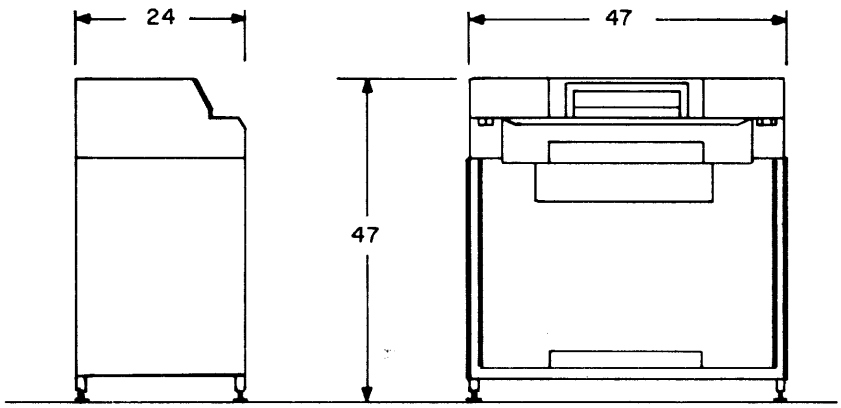


Figure 2-3. Line Printer Dimensions

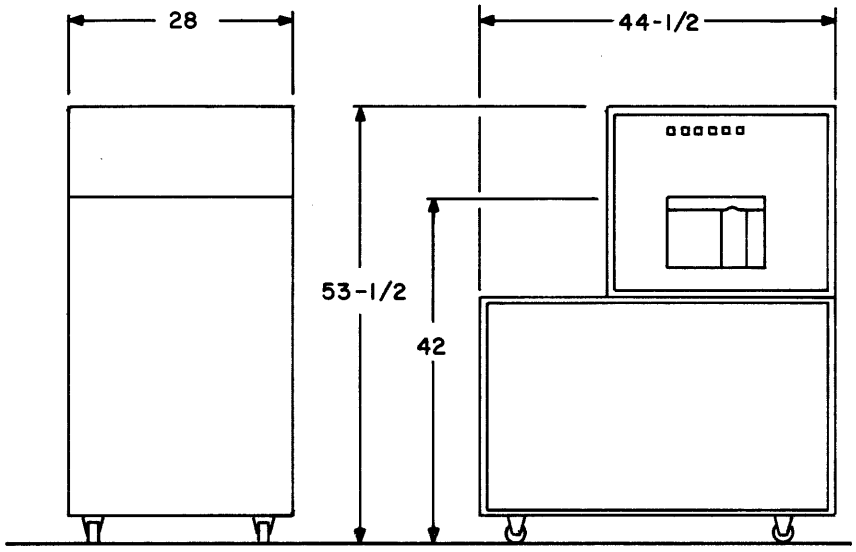


Figure 2-4. Card Punch Dimensions

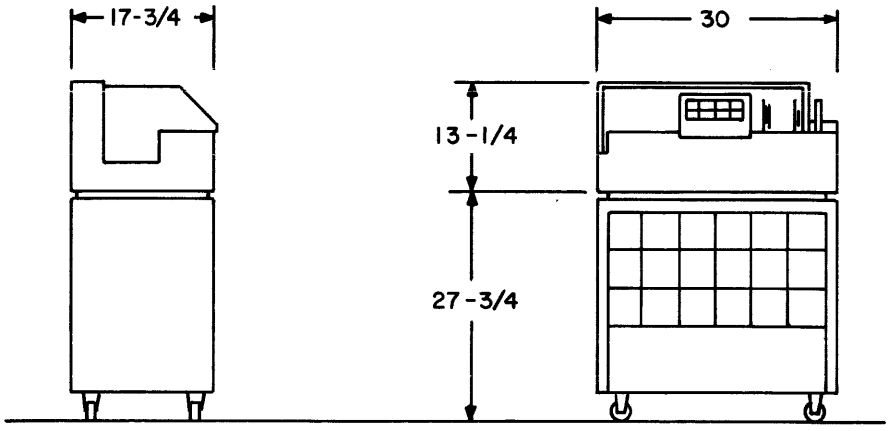


Figure 2-5. Card Reader Dimensions

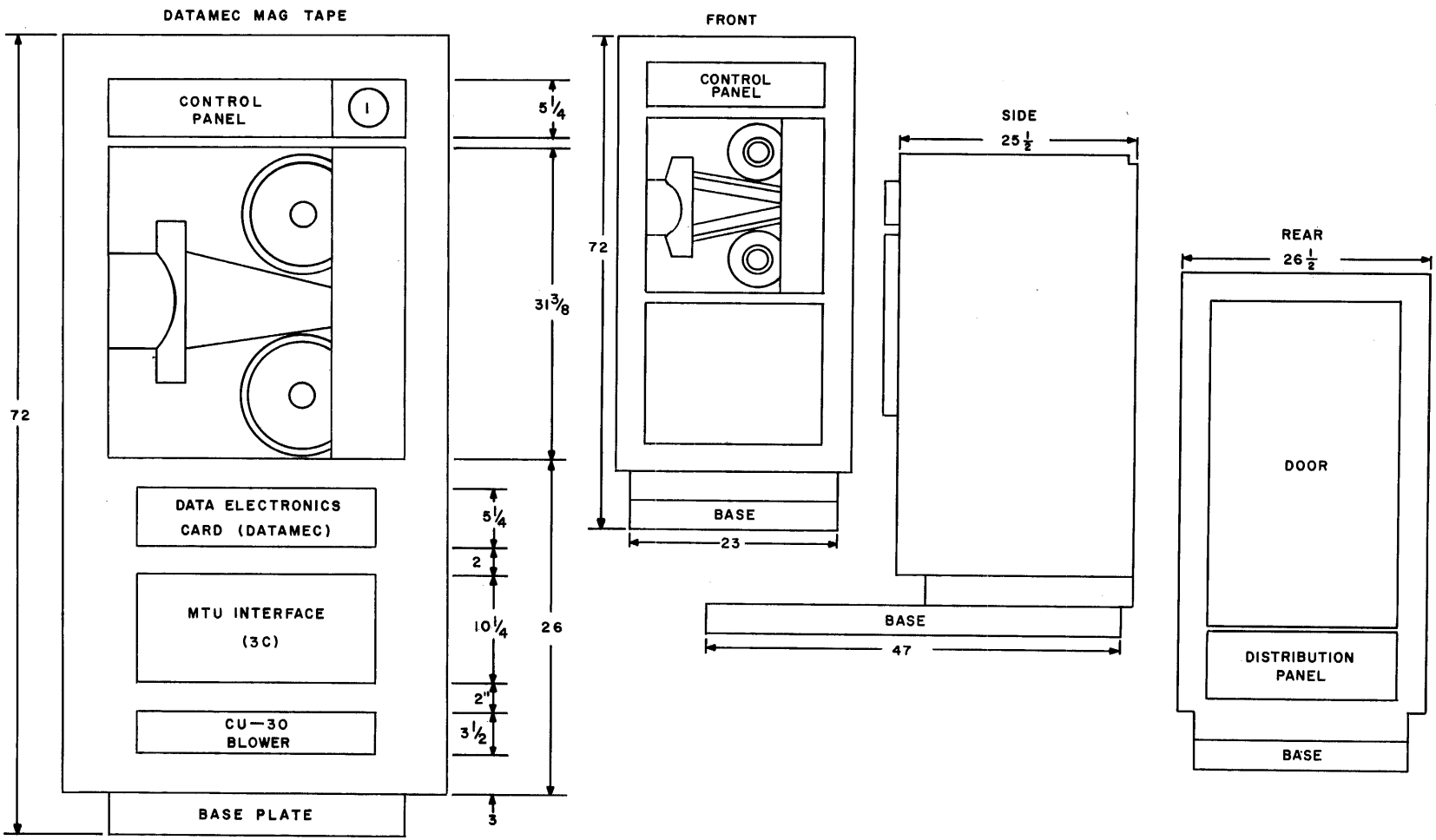


Figure 2-6. Tape Unit (45 ips) Dimensions

TABLE 2-3
MAINTENANCE EQUIPMENT REQUIRED

Quantity	Description	Mfg. or Part No.
1	Tektronix sweep delay oscilloscope	Model 545 or equivalent
1	Simpson multimeter	Model 260 or equivalent
1	Insertion tool	380306-2 (AMP Inc.)
1	Tip insertion tool	395005 (AMP Inc.)
1	Crimping tool(Type "F" 24-22 AMP Inc.)	48698*
1	Card extender PAC	XP-30*
* Computer Control Company		

2-3 ENVIRONMENTAL DATA

The standard DDP-24 requires approximately 109 sq ft of floor space for proper installation. This permits adequate room for the equipment and operating/maintenance personnel. The floor load limit should be in excess of 150 lb/sq ft. Ceiling height should be at least 10 ft to permit movement of equipment and to provide sufficient air space.

Table 2-4 lists the environmental tolerances for the standard DDP-24 and associated peripheral equipment.

2-4 POWER REQUIREMENTS

Input power for the standard DDP-24 installation is supplied from the normal commercial 3-wire, 115 ± 10 V, 60 ± 2 CPS, 1 phase, power. Power required is approximately 2000 W. A 15-foot input power cord is provided with the equipment.

The DDP-24 will, at the programmer's option, preserve the integrity of computation in the event of a power failure. If input power falls below a specified threshold, an interrupt is executed. The interrupt routine stores the contents of the arithmetic and control unit and executes a HALT (HLT) instruction. When power rises above the threshold, the interrupt may be initiated and the interrupt routine restores the registers and resumes operation.

Regulated power supplies are included in the DDP-24. No additional regulation is required if input power is within the stated specifications. Overall supply voltage variations, due to worst case combinations of the input line voltage changes, DC load regulation, dynamic load regulation, ripple, long term drift, etc., are less than 2 percent (and within the ±10 percent circuit tolerances).

TABLE 2-4
EQUIPMENT OPERATING ENVIRONMENT

Unit	Temperature °F	Relative Humidity (%)
DDP-24	32 113	0-90
Perforated Tape Reader	40 100	0-90
Paper Tape Perforator	40 100	20-90
Typewriter	40 100	0-90
Magnetic Tape Options		
75 IPS Model	32 122	40-60
45 IPS Model	55 110	40-60
Line Printer	32 113	0-90
Card Reader	32 113	0-90
Card Punch	32 113	0-90

A 230 ± 20 V, 60 ± 2 CPS, 1 phase, 3-wire power source input panel for the auxiliary cabinet power distribution box is optional. This panel may be mounted at the rear of either bay 3 or on one of the optional additional cabinets.

2-5 UNPACKING AND HANDLING

The standard DDP-24 is normally shipped uncrated in a padded moving van. The device is mounted on a wooden support to facilitate the use of lifts. If crating is required for shipment, special unpacking and handling instructions will be provided. The I/O typewriter, the table, cables, and accessories shipped separately in cartons. The auxiliary cabinets and peripheral equipment will be also mounted on wooden supports and shipped separately. Handle each unit with reasonable care to prevent excessive shock and vibration.

CAUTION

The standard computer, most of the peripheral devices, and auxiliary cabinets have a high center of gravity. Use caution when moving units.

Measure doorways and passage ways through which the equipment will pass and compare the measurements with the clearance dimensions shown in Figures 2-3 through 2-6. The exact floor locations of the various pieces of computer equipment should be marked to avoid unnecessary movement.

Move the separated components to their proper locations by the safest means available, and carefully remove the shipping material secured around each component. Visually inspect all units for physical damage. Carefully remove the wooden supports from all units. Locate the AC power cable and connect it from the main power source to the DDP-24.

2-6 INITIAL ENERGIZING AND TEST

It is mandatory that initial energizing and checkout of the DDP-24 equipment be satisfactorily completed before the installation of auxiliary cabinets or the connection of peripheral equipment. This will ensure proper system buildup and provide an immediate means for the detection faulty units.

After the DDP-24 system has been set up, ground connections have been properly made, and a visual check for faults has been made, perform the following sequential steps.

1. Position all DC circuit breaker switches to OFF.
2. Remove all AC plugs from the wire mold strips.
3. Install the 3-wire, AC power cord between the DDP-24 AC input receptacle and the site AC power source (115 ±10 V, 60 ±2 CPS 1 phase AC).
4. Turn the AC power switch to ON.
5. Monitor the AC input with an appropriate meter to insure that proper input power is applied.
6. Check all blowers for proper operation.
7. While monitoring the AC input, reconnect the plugs to the mold strips and immediately remove any inputs that place an excessive load on the input line. (This applies especially to the -24-V DC and -100 V DC power supplies.) When steps 1. through 8. have been satisfactorily completed, it can be assumed that the AC input circuits are operating properly.
8. Position the DC circuit breaker switch on the Power Supply RP-32 located in bay 2 to the ON and monitor the supply outputs with an appropriate meter.
9. Repeat step 8 with Power Supply RP-32 in Bay 4. If any abnormalities exist in any of the three supplies, turn the applicable power switch off and locate the fault. Refer to Figures 2-9 and 2-10 for power distribution. When steps 1.through 9. have been completed it can be assumed that the AC and DC lines are operating properly and that the DDP-24 is ready for checkout.

10. Insert the dummy connectors supplied with the DDP-24 in J152 and J153.

11. Program and run the diagnostic test listed in Table 2-5.

12. If an error is detected, correct the fault and rerun the diagnostic test until a satisfactory completion is obtained.

13. Install the auxiliary cabinets only after a satisfactory diagnostic test has been completed.

TABLE 2-5
DDP-24 DIAGNOSTIC TEST

1. Set SENSE SWITCHES on operation control panel as follows.

   (a) Switch 1 "up" to stop at end of test - Switch 1 down to repeat test.

   (b) Switch 2 "up" to delete type out on I/O typewriter - Switch 2 down to type instructions.

   (c) Switch 3 "up" to stop on error - Switch 3 down to continue in sequence after error.

2. Perform the diagnostic test in the following sequence.

   (a) Depress the OPERATIONAL CONTROLS, STOP button.

   (b) Depress the OPERATIONAL CONTROLS, MASTER CLEAR button.

   (c) Place the diagnostic test tape in the paper tape reader.

   (Refer to DIGITRONICS PERFORATED TAPE READER manual for loading instructions)

   (d) Set 00100 into the PROGRAM REGISTER switches.

   (e) Set the READER ON-OFF LINE switch to the ON LINE position.

   (f) Set the TYPE switch to ON LINE.

   (g) Set the READER, CONTIN-PULSE switch to the CONTIN position.

   (h) Depress the READER, FILL pushbutton. When the information on tape is read in, the tape will stop.

   (i) Depress the OPERATIONAL CONTROLS, MASTER CLEAR pushbutton.

   (j) Set 00100 into the PROGRAM REGISTER switches.

   (k) Depress the OPERATIONAL CONTROLS, START button.

3. If SENSE SWITCH 1 is placed in the "up" position, the computer will stop upon completion of the diagnostic tests. To repeat the test depress the OPERATIONAL CONTROLS, START pushbutton. If SENSE SWITCH 1 is placed in the "down" position, the diagnostic test will be repeated automatically.

4. If SENSE SWITCH 2 was placed in the "up" position, the typed result will only reveal existing errors and the end of pass. An example of this is shown below.

DIV Failing
LLS Failing
END OF PASS

TABLE 2-5 (Cont)

If at the completion a retest is desired, depress the OPERATIONAL CONTROLS, START pushbutton.

5. If SENSE SWITCH 2 was placed in the "down" position, the typed result will reveal all functions tested. An example of this is shown as follows.

```
XEC
STB
STC
STA
STD
ADD
SUB
SKG
SKN
ANA
ORA
ADM
SBM
LDB
LDA
JST
SMP
MPY
DIV FAILING
ARS
ALS
LRR
LLR
LRS
LLS FAILING
NRM
LGL
ADX
TAB
LDX
IAB
CRA
SKS
RND
TAX
SCR
SCL
STX
IRX
JPL
JZE
JIX
JOF
JXI
END OF PASS
```

6. If SENSE SWITCH 3 was placed in the "up" position and the test stopped on error (as commanded), the A, B, and index registers will retain information held at the time of the error detection. Press the OPERATIONAL CONTROLS START button to resume the test.

2-7 FIELD INSTALLATION OF AUXILIARY CABINET

If the installation of the auxiliary cabinets is essentially a reassembly task, use the predrilled holes and the hardware supplied to secure the auxiliary cabinet to bay 1 or bay 4. If the installation is a complete assembly task, proceed as follows.

Cut an access hole through the cabinet in the area adjacent to the taper pin connector located on the lower right side of bay 1. The diameter of the hole should be large enough to permit passage of interconnecting cables.

Note the manner in which bay 1 is mechanically bolted to bay 2. Drill corresponding bolt holes in the right-hand side of bay 1 and the left-hand side of the auxiliary cabinet. Secure the two cabinets together with hardware similar to that used to secure bay 1 to bay 2.

If interconnecting cables are not supplied with the auxiliary cabinets, use a breakaway type of connector to facilitate relocation of the equipment.

Fasten the typewriter table to the front of the standard computer with the hardware provided.

Install the input-output typewriter in its recessed position on the computer operator's table.

Install the peripheral equipment as near as possible to the DDP-24 main assembly. This prevents the necessity of long interconnecting cables, thereby reducing "cross-talk".

2-8. CABLING DATA

Interconnecting cables between the DDP-24 and peripheral equipment will vary in length according to placement of the units. The maximum recommended length of signal cables is 25 ft. If the cables are to be assembled at the installation site, mating plugs are provided for the receptacles on the connector panel.

The DDP-24 is equipped with a connector panel at the rear of the bay 4 cabinet (Figure 2-7). Figure 2-9 shows the connector panel itself. Besides the six connectors associated with the standard DDP-24, up to 15 additional connectors may be used for optional input/output signals. All necessary connectors are provided with the standard computer. More connectors can be accommodated, if required, by adding a connector panel at the rear bottom of bay 3.

Where an auxiliary cabinet is used, input power from the line may be applied directly to the cabinet by installing the optional A-C power distribution panel shown in Figure 2-8. The use of this panel is recommended when the auxiliary equipment cabinet requires more power than can be supplied from the main computer. Figure 2-8 shows the normal input wiring to the panel.

The 50-pin connector used on the panel is a Cannon KOA2-21-L-50S. The mating plug provided with each DDP-24 system is a Cannon KOA3-21-50P with a KA5-21-5/8 shell. (See Table 2-6 and 2-9 for polarization.)

Tables 2-6 and 2-7 show the designation of all standard DDP-24 connectors. Tables 2-8 through 2-13 provide the pin functions of the connectors for the various channels.

Figure 2-10 illustrates the system DC power cabling to BLOCs and memory. Routing of site cabling should coincide. If necessary, point-to-point checks can be made by referring to section 6 or the Instruction Manual for 1-MC S-PAC Modules.

Figure 2-11 shows the DDP-24 ground connections. Be sure the bay-to-bay ground connections are as indicated. This reduces transient inter-coupling between bays, circuits, and signal lines.

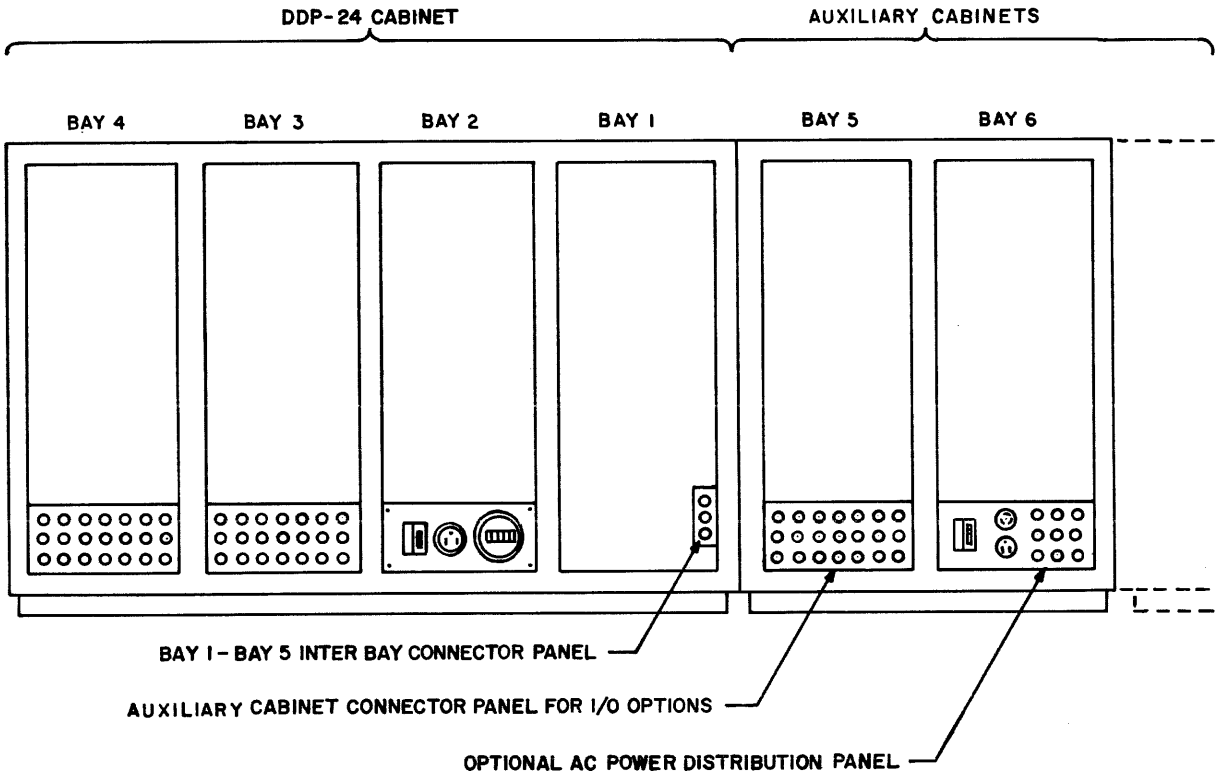


Figure 2-7. DDP-24 Complete System, Rear View (Typical)

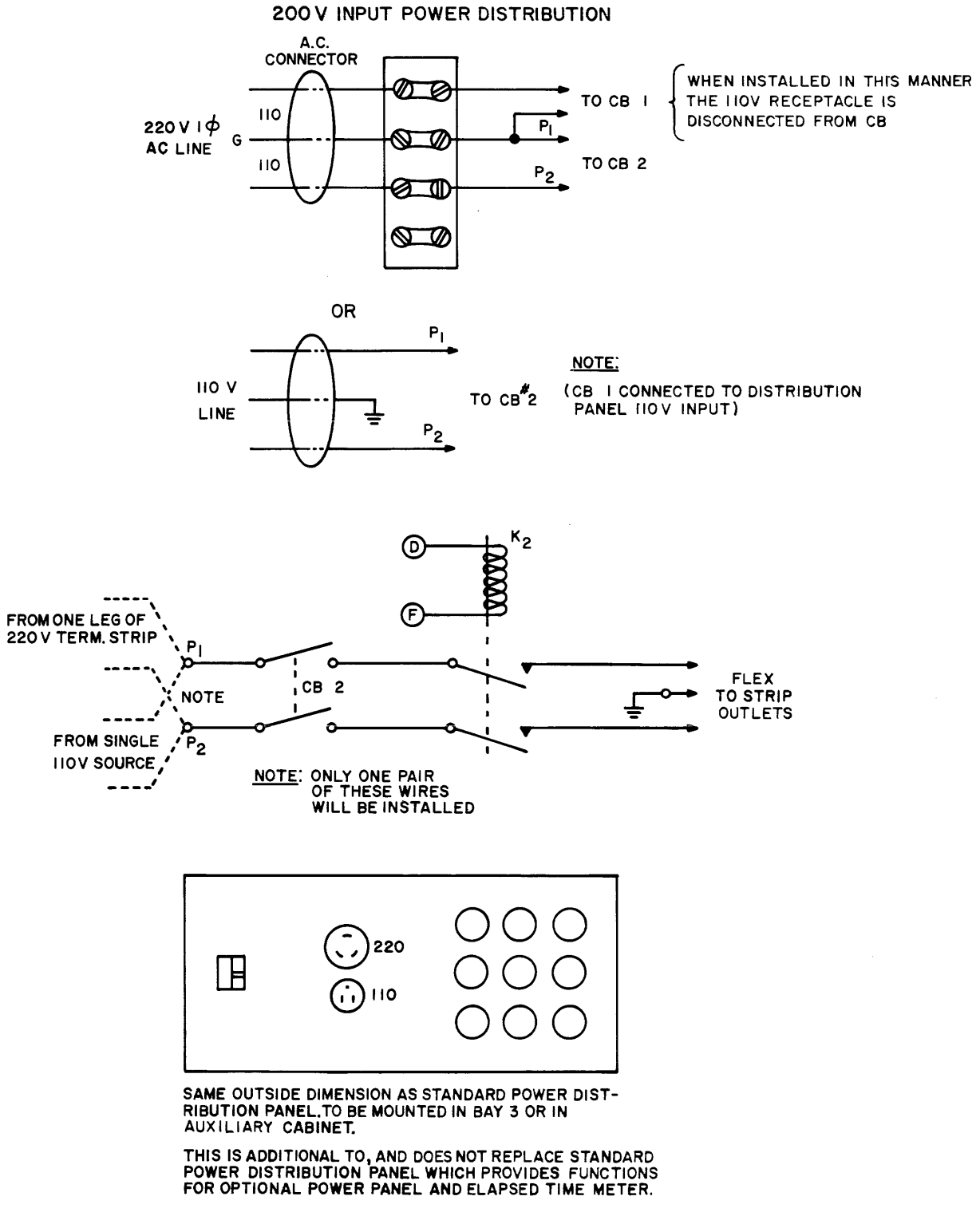
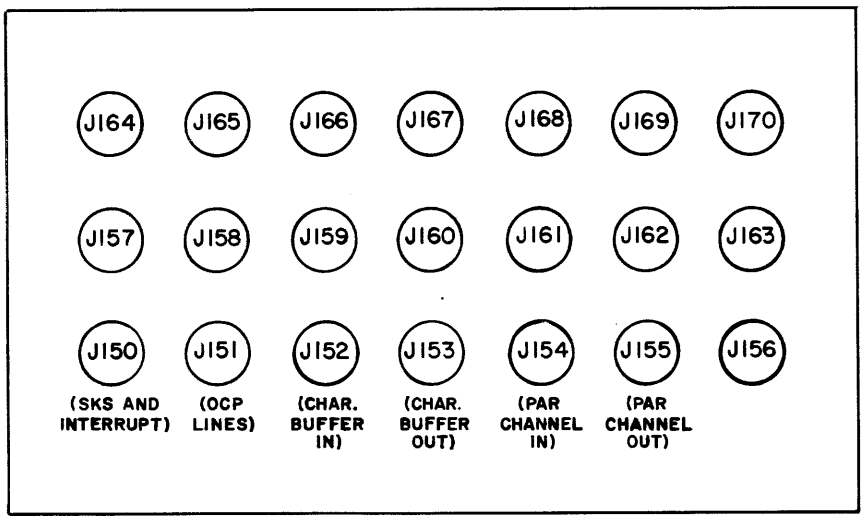
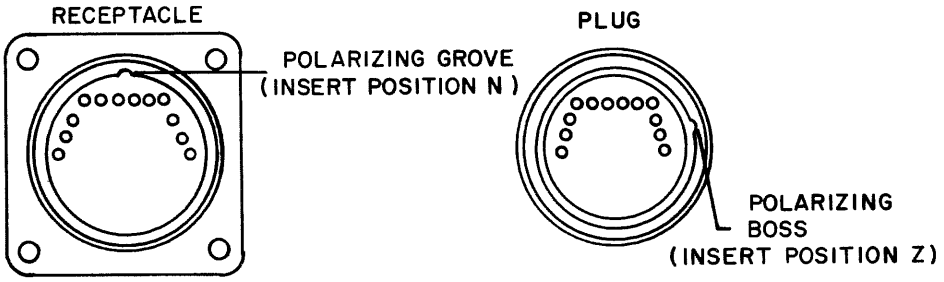


Figure 2-8. Optional AC Power Distribution Panel





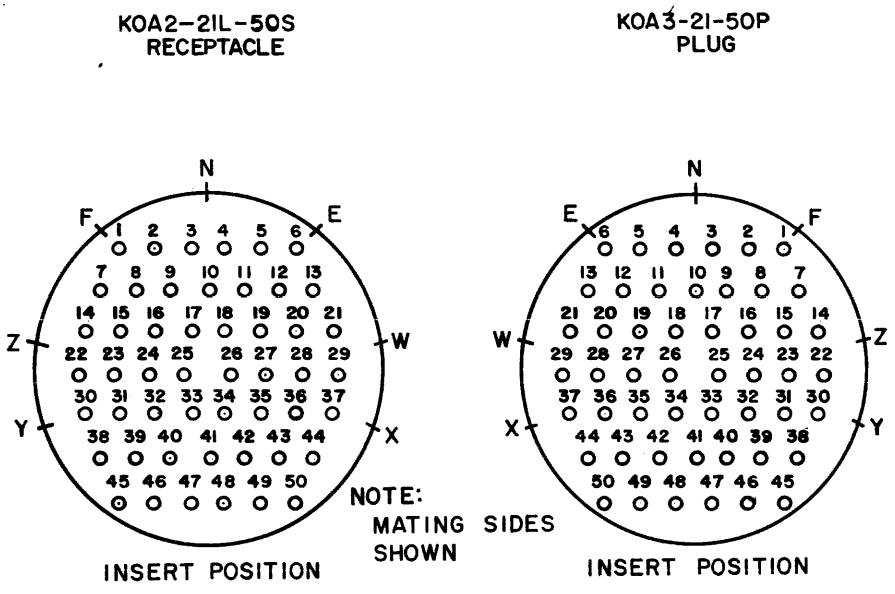


Figure 2-9. DDP-24 Connector Polarization

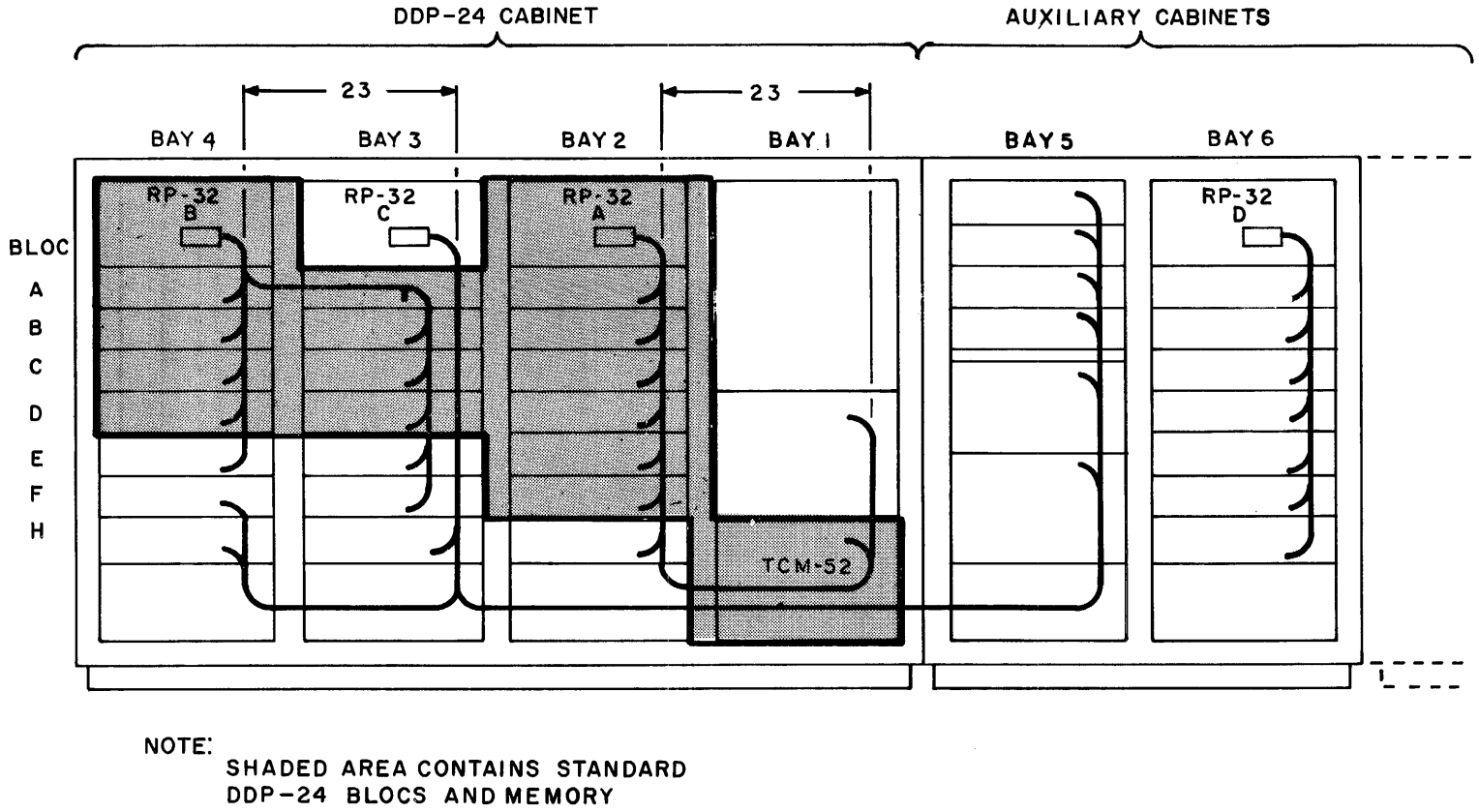


Figure 2-10. DDP-24 System DC Power Cabling to Block and Memory

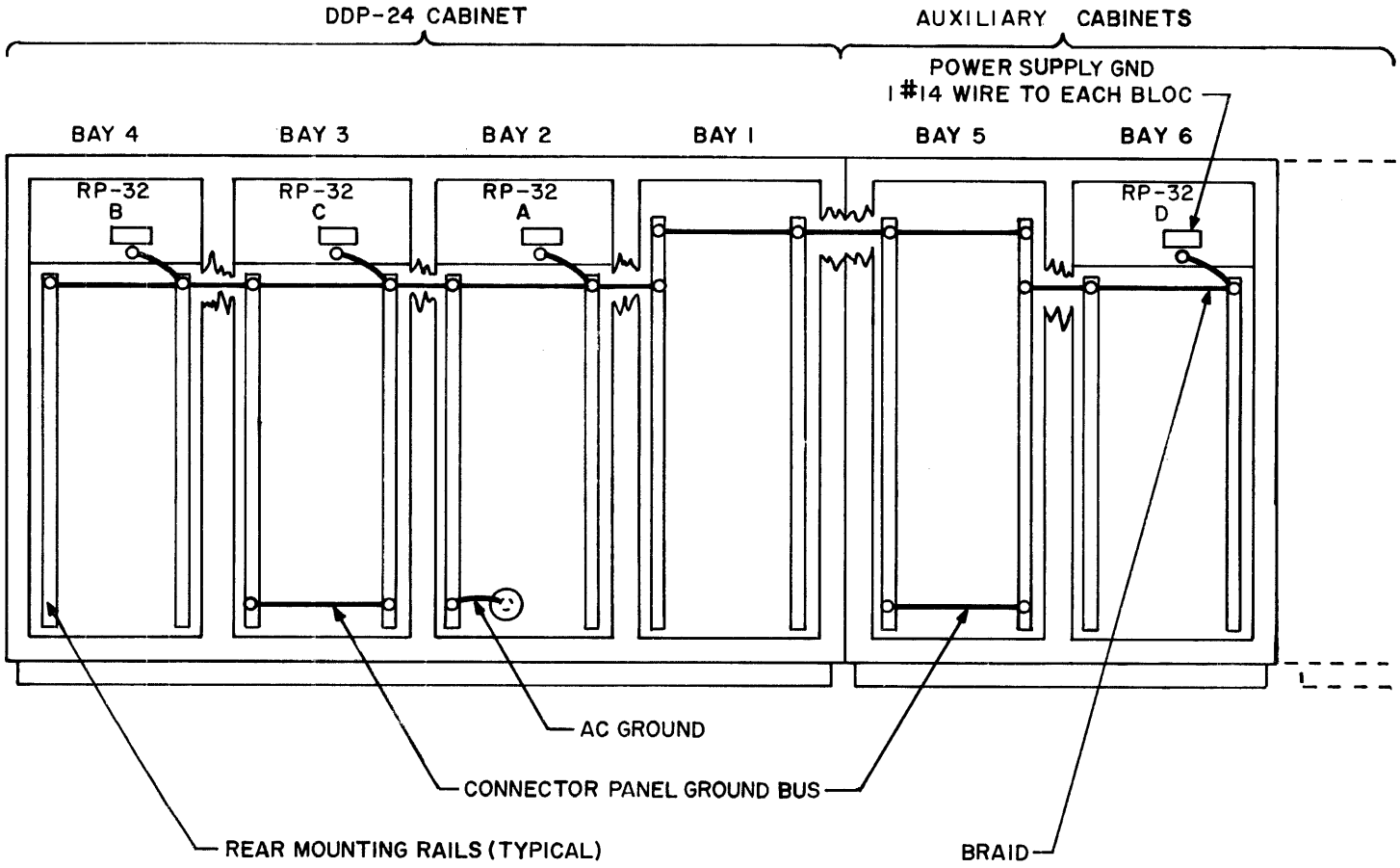


Figure 2-11. DDP-24 Details of Ground Connection

TABLE 2-6
INTERNAL DDP-24 CONNECTOR ASSIGNMENTS

Unit	Conn. No.	Major Function	J Type (Receipt)	P Type (Plug)	Mfg.
Memories	J100A-D	AC pwr, mem 1-4	P302-AB	S-302-CCT	Cinch Jones
	J101A-D	DC pwr, mem 1-4	P312-DB	S-312-DB	Cinch Jones
	J103A-D	Sig lines mem 1-4	DD50S	DD50P	Cannon
	J106A-D	Sig lines mem 1-4	DD50S	DD50P	Cannon
	J102A-B	Fully buffered mem 1-2	DD50S	DD50P	Cannon
	J105A-B	Fully buffered mem 1-2	DD50S	DD50P	Cannon
AC panel	J108	25 VAC to control panel	(126-198)	(126-195)	Amphenol
Power supply	J109	-24 VDC and ind voltages	NK-27-32S	NK-27-21C 1/2	Cannon
Control panel	J110	Indicator and switch signals	DD50P	DD50S	Cannon
Control panel	J111	Indicator and switch signals	DD50P	DD50S	Cannon
Control panel	J112	Indicator and switch signals	DD50P	DD50S	Cannon
Control panel	J113	Indicator and switch signals	DD50P	DD50S	Cannon
Paper tape perforator	J114	Voltages and signals		25034-16S	Continental
Typewriter	J115	Voltages and signals		MRA 50S+	Winchester
Perforated tape reader	J116	Voltages and signals		UPCC-F2HSL-23	US Components

TABLE 2-7
EXTERNAL DDP-24 CONNECTOR ASSIGNMENTS

Unit	Conn. No.	Major Function	J Type	P Type	Keyway
Standard DDP	J150	SKS and interrupt	KOA2-21L-50S	KOA3-21-50P	Key (N)
	J151	OCP lines	KOA2-21L-50S	KOA3-21-50P	Key (N)
	J152	Character buffer in	KOA2-21L-50S	KOA3-21-50P	Key (N)
	J153	Character buffer out	KOA2-21L-50S	KOA3-21-50P	Key (N)
	J154	Parallel chan in	KOA2-21L-50S	KOA3-21-50P	Key (N)
	J155	Parallel chan out	KOA2-21L-50S	KOA3-21-50P	Key (N)
Options	J156	Option	KOA2-21L-50S	KOA3-21-50P	Key
	J157	Option	KOA2-21L-50S	KOA3-21-50P	Key
	J158	Option	KOA2-21L-50S	KOA3-21-50P	Key

TABLE 2-8
PIN ASSIGNMENTS FOR J150-SKS AND INTERRUPT

Function	Pin	Function	Pin	Function	Pin
SKS20000	1	$\overline{\text{SKS30000}}$	18	L1	35
$\overline{\text{SKS20000}}$	2	SKS30001	19	L2	36
SKS20001	3	$\overline{\text{SKS30001}}$	20	L3	37
$\overline{\text{SKS20001}}$	4	SKS30002	21	RT1	38
SKS20002	5	$\overline{\text{SKS30002}}$	22		39
$\overline{\text{SKS20002}}$	6	SKS30003	23		40
SKS20003	7	$\overline{\text{SKS30003}}$	24	GRD	41
$\overline{\text{SKS20003}}$	8	SKS30004	25		42
SKS20004	9	$\overline{\text{SKS30004}}$	26		43
$\overline{\text{SKS20004}}$	10	SKS30005	27		44
SKS20005	11	$\overline{\text{SKS30005}}$	28		45
$\overline{\text{SKS20005}}$	12	SKS30006	29		46
SKS20006	13	$\overline{\text{SKS30006}}$	30	GRD	47
$\overline{\text{SKS20006}}$	14	SKS30007	31	GRD	48
SKS20007	15	$\overline{\text{SKS30007}}$	32		49
$\overline{\text{SKS20007}}$	16		33		50
SKS30000	17	LO	34		

TABLE 2-9
PIN ASSIGNMENTS FOR J151-OCP

Function	Pin	Function	Pin	Function	Pin
OCPx1010	1	OCPx1014	5	GRD	41
OCPx1011	2	OCPx1015	6	GRD	47
OCPx1012	3	OCPx1016	7	GRD	48
OCPx1013	4	OCPx1017	8		

TABLE 2-10
PIN ASSIGNMENTS FOR J152-CHARACTER BUFFER IN

Function	Pin No.
EXD 1: Least significant	24
EXD 2: Digit 2	23
EXD 3: Digit 3	22
EXD 4: Digit 4	21
EXD 5: Digit 5	20
EXD 6: Digit 6	19
EXD 7: Digit 7 (parity)	25
External parity error	26
Ground	41, 47, 48
Lateral parity strobe	27
Input device select	36
Input drop-in pulse	35
Character buffer busy	37
Stop signal	38

TABLE 2-11
PIN ASSIGNMENTS FOR J153-CHARACTER BUFFER OUT

Function	Pin No.
K1: Least significant	24
K2: Digit 2	23
K3: Digit 3	22
K4: Digit 4	21
K5: Digit 5	20
K6: Digit 6	19
K7: Digit 7 (parity)	25
External parity error	26
Ground	41, 47, 48
Output device select	36
Output busy (output drop-out pulse)	35
Character buffer busy	37
Stop signal	38

TABLE 2-12
PIN ASSIGNMENTS FOR J154-PARALLEL INPUT CHANNEL

Function	Pin No.
Data 1: Most significant bit	1
Data 2: 2nd bit	2
Data 3: 3rd bit	3
Data 4: 4th bit	4
Data 24: 24th bit	24
Ground	29
Input device select	31
Input drop-in pulse	30
Parallel IN channel busy	32
Stop signal	38

TABLE 2-13
PIN ASSIGNMENTS FOR J155-PARALLEL OUTPUT CHANNEL

Function	Pin No.
Data 1: Most significant bit	1
Data 2: 2nd bit	2
Data 24: 24th bit	24
Strobe gate line	28
Ground	29
Output device select	31
Output drop-out pulse	30
Parallel output channel busy	32
Stop signal	38

SECTION III
OPERATION

3-1 INTRODUCTION

This section contains detailed instructions in the use of operating controls and indicators on the DDP-24 control and maintenance panels. The description of each panel is in functional areas. The operating procedures contain the sequence of operation required to perform different modes of operation. Required adjustments, and precautions are included when applicable to proper operation.

3-2 OPERATING CONTROLS AND INDICATORS

3-2.1 Control Panel

The control panel (Figure 3-1) contains the switches and indicators required to operate the equipment. The contents of registers are displayed on panel indicators. Switches are provided for manual entry of data into the system. The control panel also provides sense switches for program branching, indicators and controls for input-output devices, and a power switch.

3-2.1.1 Register Display. - The binary contents of the registers are indicated on neon pushbutton indicators to facilitate a bit-by-bit entry of data into the system. A RESET button is provided to clear each register to all ZERO's. The RESET button for the OP-code register also clears the index bits and the indirect address bit. The following registers are displayed on the panel.

a. A-Register; one indicator for each of the 24 bits in the A register.
b. B-Register; one indicator for each of the 24 bits in the B register.
c. Z-Register; one indicator for each of the 24 bits in the Z register.
d. INDEX REGISTER; one indicator for each of the 15 bits in the index register.
e. PROGRAM REGISTER; one indicator for each of the 15 bits in the program register.
f. OP-CODE; one indicator for each of the 6 bits in the OP-code register.
g. INDEX; two indicators which denote the index register addressed.
h. INDIRECT ADDRESS BIT; one indicator which denotes status of the indirect address bit.

3-2.1.2 Operating Controls. - The following functions are performed by momentary-contact pushbutton switches on the Control Panel.

STOP: Sets the halt flip-flop and prevents execution of the program after the current instruction is processed.

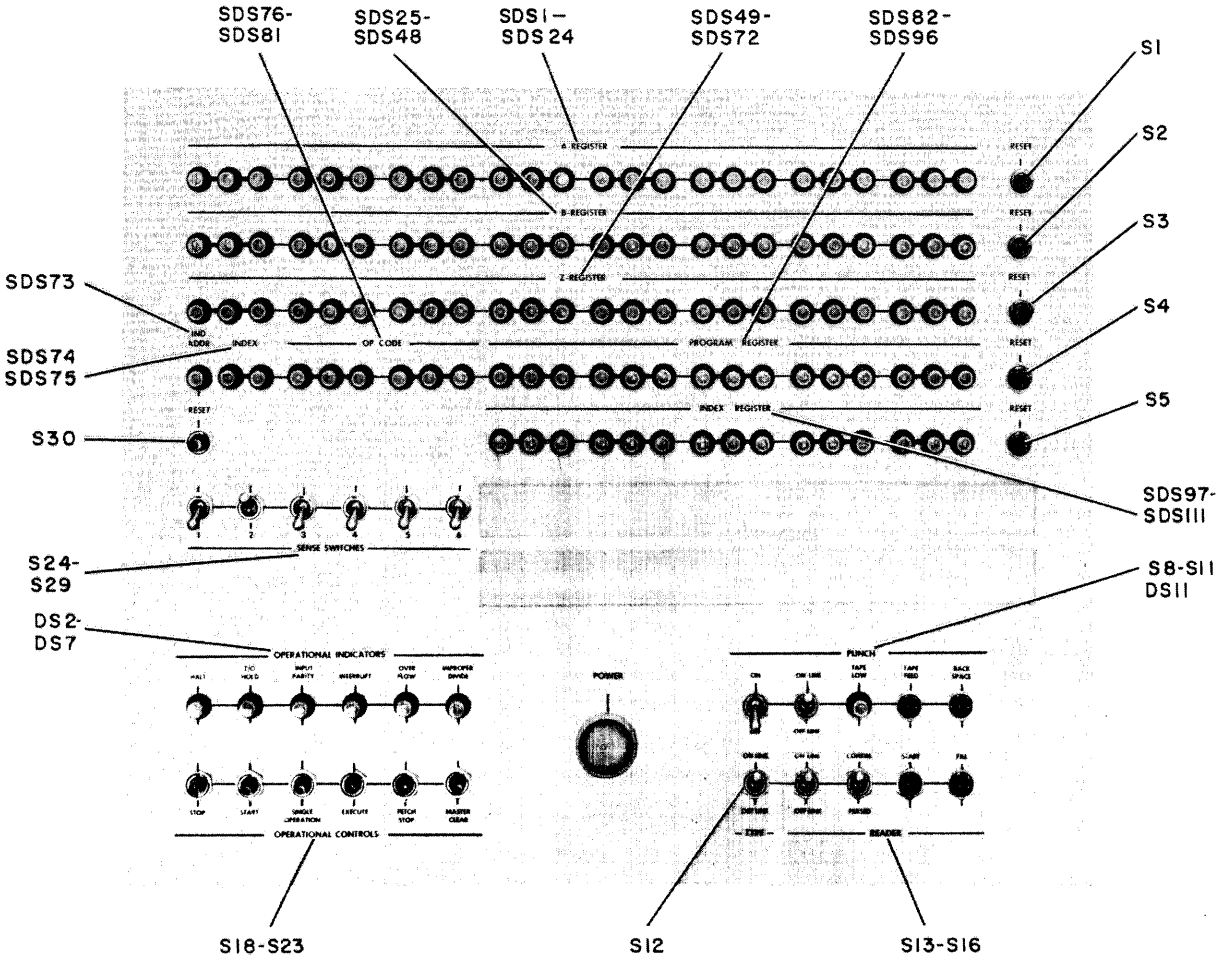


Figure 3-1. DDP-24 Control Panel

START: Resumes the execution of a program, beginning with the command stored in the memory location indicated by the program register.

SINGLE OPERATION: Same as START except the halt flip-flop is not reset. Computer operations stop after the execution of one command.

EXECUTE: Executes the OP-code in the OP-code register. When an operand address exists, it will correspond to the 15 least significant bits of the address portion of the Z register if no index is specified. If an index register is specified, the effective operand address is the sum of the address portion of the (Z) and the Index (X) registers.

FETCH-STOP: Stops command execution when a new fetch cycle is completed, and the Z register contains the contents of the memory location specified by the program counter.

MASTER CLEAR: Sets the halt flip-flop, resets all displayed registers, resets the index bits and the indirect address bit flip-flop, the control unit clock, the ready and enable flip-flops of all input-output channels, the interrupt enable, input parity, overflow, and improper-divide flip-flops. Stops the paper tape reader, and resets all control flip-flops of optional peripheral equipment.

3-2.1.3 Operating Indicators. - The following indications are displayed on the control panel.

HALT: The halt flip-flop is set and no operations can take place except the handling interrupts. Upon completion of the interrupt subroutine, the computer returns to the halt state with the same value in the program counter as before. The halt flip-flop is not reset by an interrupt procedure.

I/O HOLD: Indicates that one or more input or output devices is busy.

INPUT PARITY: Detection of an error while reading character information; corresponds to the state of the input parity flip-flop. Flip-flop can be reset with properly coded command.

INTERRUPT: Execution of an interrupt subroutine. Corresponds to the state of the interrupt flip-flop.

OVERFLOW: An overflow indicator for detection of arithmetic and scaling errors in the program. Overflow may occur during computer operations in the following cases.

a. Additions or subtractions which produce sums or differences surpassing the capacity of the A register. This is valid for both straight and absolute value additions or subtractions as well as for the rounding of A with the RND command. The overflow indicator is set by these conditions and remains set.

b. If a carry is produced by the addition or subtraction of the next lower order portion in multiple precision operations. The overflow flip-flop will be reset when a multiple precision operation step does not produce a carry, and therefore, it will be reset after the complete multiple precision addition or subtraction has been performed correctly.

c. During ALS, LLS, or SCL instructions, if a one is shifted out the A register (A2).

The overflow indicator may be reset by the JOF (Jump on Overflow) command and the SKS (Skip if Sense Line Not Set) command.

IMPROPER DIVIDE: The improper divide indicator is switched on in the following cases.

a. For division undertaken with a numerator larger than or equal to the denominator. The resulting quotient surpasses the capacity of the B register.

b. For the optional Binary to BCD command, if executed with a number which, upon conversion, results in a BCD number greater than 799,999. The improper divide indicator may be reset by the SKS (Skip if Sense Line Not Set) command.

POWER: This self-illuminating pushbutton turns computer power on and off. When power is switched on, system normalizers ensure that flip-flops are reset and the halt condition is set. This prevents undesirable runaway effects. No warm-up period is required.

SENSE SWITCHES: These 6 switches permit the operator or programmer to have manual control of program branching. The state of any or all six switches can be tested by properly coded SKS commands, after which branching may take place.

3-2.1.4 Input-Output Controls. - The following controls are used to interchange and control peripheral input-output equipment.

1. Reader

a. ON LINE/OFF-LINE switch. Permits characters to be entered in the character buffer for on-line operation. The reader is disconnected from the computer in the off-line mode. No outputs enter the character buffer while the tape reader is operating in the off-line condition.

b. CONTIN./PULSED switch. Permits either continuous or pulsed tape reader operation. In pulsed mode the reader stops after each character read, and the computer program must provide a pulse to read the next character.

c. START switch. Momentary pushbutton used to start movement of paper tape in the reader.

d. FILL switch. Momentary pushbutton switch used to enter data from paper tape or typewriter without the use of a stored program. Characters are built into words and words are stored in successive memory locations. The halt flip-flop is reset, no program execution can take place, and operation is terminated by the stop-code character.

2. Type

a. ON-LINE/OFF-LINE switch. Controls on-line or off-line operation of the input-output typewriter. Characters are entered in the character buffer for on-line

operation. Outputs from the computer to the typewriter are also handled through the buffer. During off-line operation, typewriter inputs and outputs are connected to the buffer, the keyboard lock is released, and the character buffer is disconnected from the computer.

3. Punch

a. ON/OFF switch controls the operation of the punch motor.

b. ON-LINE/OFF-LINE switch controls on-line or off-line paper tape punch operation. In both modes, the punch is connected to a standard character buffer. In the off-line mode, it can punch data from the typewriter or the tape reader.

c. TAPE LOW indicator light indicates that level of paper tape in punch has reached a predetermined low level.

d. TAPE FEED switch. Momentary-contact pushbutton switch which permits tape advance for sprocket hole punching.

e. BACKSPACE switch. Momentary-contact pushbutton switch which allows backspacing of paper tape by one sprocket hole for punching a delete code.

f. Table 3-1 lists the various On-Line/Off-Line combinations.

TABLE 3-1
ON-LINE/OFF-LINE COMBINATIONS

Reader	Type	Punch	On-Line Prog. Controlled	Off-Line Operation
On-line	On-line	On-line	Reader, type, punch; normal operation	None
On-line	On-line	Off-line	Reader, typewriter	None
On-line	Off-line	On-line	Reader, punch	Typewriter
On-line	Off-line	Off-line	None (reader must not be used)	Typewriter to punch, for paper tape preparation.
Off-line	On-line	On-line	Type, punch	None
Off-line	On-line	Off-line	None (typewriter must not be used)	Tape reader to punch, for paper tape duplication.
Off-line	Off-line	On-line	None	Reader to type-writer; for print-out of paper tape.
Off-line	Off-line	Off-line	None	Reader to type-writer and punch.

3-2.2 Maintenance Panel

A maintenance panel is provided for computer maintenance and troubleshooting (Figure 3-2). The panel is located behind the second bay (top panel) of the computer cabinet (Figure 1-2) and swings into full view for computer diagnostic tests. The panel indicators and controls permit rapid localization of system failures. For complete information on the controls and indicators refer to Section VI of this manual.

3-2.2.1 Indicators. - The following indications are displayed on the control panel.

MAR: A status indicator for each of the 12 bits in the memory address register.

AU BUS: A status indicator for each of the 24 bits from the AU bus.

TRANSFER BUS: A status indicator for each of the 24 bits from the transfer bus.

READY/ENABLE I/O CHANNELS: Two indicators are provided for each of the reader and enable flip-flops of the 8 input-output channels to indicate the status of each stage. Channel 1 is a parallel channel in; channel 2 is a character buffer, and channel 3 is a parallel channel out. Channels 4-8 are optional.

SHIFT COUNTER: A status indicator for each of the 6 shift counter flip-flops.

CONTROL CLOCK: Indicates fetch (Tf), transition (Tt), and operate clock signals (T01-8).

3-2.2.2 Controls. - The following functions are performed by the controls on the maintenance panel.

INTERRUPT ON-OFF switch. Disables automatic interrupt capability of all input-output channels.

CLOCK ON-OFF switch. Disables the computer one-megacycle clock when in the OFF position.

SINGLE-STEP switch. Produces a single clock pulse when depressed (with computer clock turned off).

REPEAT CYCLE ON-OFF switch. Provides repeated execution of the same command when in the ON position by preventing any change in the program counter (P register contents). The skip and jump commands do not apply to this command.

3-2.2.3 Paper Tape Format. - Paper tape coding is indicated in Figure 3-3. Punched holes in any of the eight paper tape channels correspond to ONE bits. Paper Tape Channel No. 1 corresponds to the least significant character bit. Paper tape must be loaded with channel 1 next to the computer front panel.

During paper tape fill, under control of the FILL button on the control panel, the bits in channels 4, 6, 7, and 8 must be ZERO. If any of these bits is a ONE, the associated character is ignored.

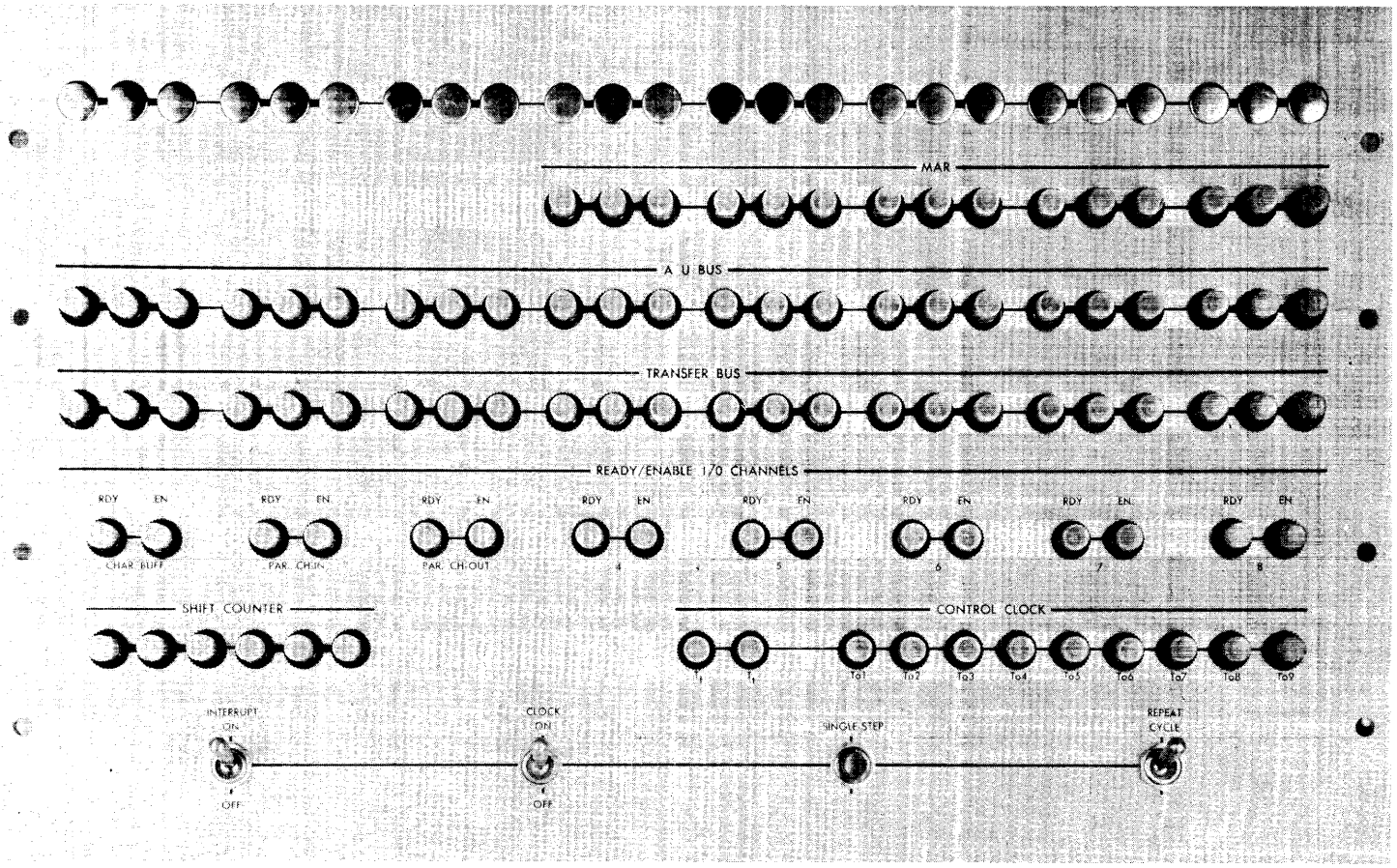


Figure 3-2. Maintenance Panel

The bits in channels 1, 2, 3, 4, 6, and 7 are read from the paper tape in normal operation. Any character with a ONE in all of these positions is ignored and corresponds to the DELETED character 011(p). 111.

The parity bit is automatically checked, either when it is read or punched, by the parity logic in the character buffer or word buffer. Odd parity is used.

If channel 8 contains a ONE bit (stop code) and channel 6 contains a ZERO (no punch), the paper tape reader is stopped. The contents of channels 1 through 7 are read by the computer, and the stop code flip-flop is set. If both channel 8 and channel 6 contain a ONE bit, the character is ignored (channels 1 through 5 and 7 are ignored) and the tape reader is not stopped.

THE BACKSPACE key is used to punch stop codes for off-line paper tape preparation with the punch unit under direct keyboard control. The stop code on the tape will appear as: 100(p)0.000, with (p) corresponding to the parity bit. A stop code can be punched for on-line tape punching after setting the stop code flip-flop with an OCP command.

The occurrence of a stop code from either the BACKSPACE key or the paper tape reader can be tested with an SKS command.

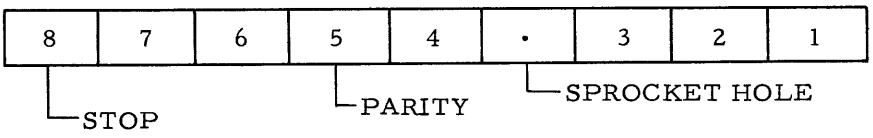


Figure 3-3. Paper Tape Format

3-2.3 Operating Procedures

3-2.3.1 Power Failure Protection. - Input power to the DDP-24 is monitored and if it falls below a specified threshold, an interrupt is initiated. The interrupt routine stores the contents of the arithmetic and control unit registers and executes a halt (HLT) instruction. When (after power failure) power rises above the threshold, a special interrupt may be initiated and an interrupt routine will restore the registers and resume operation.

3-2.3.2 Power On. - Depress the control panel POWER switch and the MASTER CLEAR button. The running time indicator and the system circuit breaker are located at the rear of the computer cabinet.

3-2.3.3 Paper Tape Reader Program Loading. - Complete the following steps to load a program from paper tape.

a. Depress the MASTER CLEAR button.

b. Set the paper tape reader controls to ON-LINE and CONTIN. Set the typewriter and the punch to ON-LINE, and turn on tape reader power.

c. Load the paper tape with the three-channel side next to the computer front panel.

Note

Black tape is recommended, but the reader can be adjusted to handle tapes of other colors.

d. Manually enter the memory address of the first paper-tape word to be stored into the program counter.

e. Depress the FILL button to start the tape moving through the reader.

Note

Do not use the READER START button during this procedure.

f. The reader will stop automatically when it reaches the stop code which is a ONE bit in the eighth paper tape channel.

During paper tape fill, the halt flip-flop will remain set. The characters are read from the tape, parity is checked, the characters are assembled into 24-bit computer words in the A register, and the words are entered in successive memory locations.

During fill, only the three least significant bits of each character are read from the three tape channels (on one side of the sprocket). These bits correspond to octal format. Eight octal formats form one 24-bit word. Bits 4, 6, 7, and 8 on the other side of the sprocket channel must be ZERO for the octal format. If any of these bits become ONE, the buffer ignores the entire associated character.

3-2.3.4 Typewriter Program Loading. - Complete the following steps to load a program from the typewriter.

a. Turn the tape reader off.

b. Set the typewriter, the reader, and the punch controls to ON-LINE.

c. Depress the MASTER CLEAR button, and set the OP-code register according to OCP command.

d. Enter octal 00002000 into the Z register (this corresponds to 02000 in the address portion of the OCP command).

e. Depress the EXECUTE button on the maintenance panel. This selects a typewriter input by executing instruction 05302000.

f. Depress the MASTER CLEAR button and manually enter the memory address for the first word from typewriter into the program counter.

g. Depress the FILL button.

h. Type in characters in octal form from the typewriter. Codes other than octal will be ignored. Eight characters are assembled into 24-bit computer words, starting

from the most significant end of the word. The assembled words are entered in successive memory locations under automatic control of the FILL system.

i. The FILL mode will stop automatically when the BACKSPACE key (stop code) is depressed.

3-2.3.5 Manual Program Loading. - Complete the following steps for manual program loading.

a. Depress the MASTER CLEAR button and enter the address information into the address portion of the Z register.

b. Set the A register according to the word to be entered in the computer.

c. Set the OP-code register according to the STA command (code 05) and depress the EXECUTE button located on the maintenance panel.

Note

This procedure loads only one word at a time. The effective address must be updated manually for consecutive words.

3-3 DDP-24 COMMAND LIST

The commands for the DDP-24 are listed in Table 3-2.

3-4 DDP-24 COMMAND REPERTOIRE

The command repertoire for the DDP-24 is listed in Table 3-3.

TABLE 3-2
COMMAND LIST

Op	Com-mand	Description	Execution Time
00	HLT	Halt	5 μsec
02	XEC	Execute	5 μsec +variable
03	STB	Store B	10 μsec
04	STC	Store command portion of A	10 μsec
05	STA	Store A	10 μsec
06	STD	Store address portion of A	10 μsec
07	INM	Input to memory	10 μsec
10	ADD	Add	10 μsec
11	SUB	Subtract	10 μsec
12	SKG	Skip if A greater	10 μsec
13	SKN	Skip if A not equal	10 μsec
15	ANA	AND to A	10 μsec
16	ORA	OR to A	10 μsec
17	ERA	Exclusive OR to A	10 μsec
20	ADM	Add Magnitude	10 μsec
21	SBM	Subtract Magnitude	10 μsec
22	OTM	Output from memory	10 μsec

TABLE 3-2 (Cont)
COMMAND LIST

Op	Com-mand	Description	Execution Time
23	LDB	Load B	10 μsec
24	LDA	Load A	10 μsec
25	JRT	Jump Return	10 μsec
27	JST	Jump and Store location	10 μsec
30	SMP	Step Multiple Precision	10 μsec
31	FMB	Fill Memory Block	variable
32	DMB	Dump Memory Block	variable
34	MPY	Multiply	31 μsec
35	DIV	Divide	33 μsec
36	BCD*	BCD to Binary Conversion	33 μsec
37	BIN*	Binary to BCD Conversion	33 μsec
40	ARS	A Right Shift	5+n μsec
41	ALS	A Left Shift	5+n μsec
42	LRR	Long Right Rotate	5+n μsec
43	LLR	Long Left Rotate	5+n μsec
44	LRS	Long Right Shift	5+n μsec
45	LLS	Long Left Shift	5+n μsec
46	NRM	Normalize	5+n μsec
47	LGL	Logical Left Shift	5+n μsec
50	OTA	Output from A	5 μsec
51	ITC	Interrupt Control	5 μsec
52	INA	Input to A	5 μsec
53	OCP	Output Control Pulse	5 μsec
54	ADX	Add to Index	5 μsec
55	TAB	Transfer A to B	5 μsec
56	LDX	Load Index	5 μsec
57	IAB	Interchange A and B	10 μsec
60	CRA	Clear A	5 μsec
61	SKS	Skip if Sense Line Not Set	5 μsec
62	RND	Round A	5 μsec
63	TAX	Transfer A to Index	5 μsec
64	SCR	Scale Right	5+n μsec
65	SCL	Scale Left	5+n μsec
66	STX	Store Index	10 μsec
67	IRX	Increment, Replace and Load Index	13 μsec
70	JPL	Jump if A Plus	5 μsec
71	JZE	Jump if A Zero	5 μsec
72	JIX	Jump on Index	5 μsec
73	JOF	Jump on Overflow	5 μsec
74	JMP	Unconditional Jump	5 μsec
75	JXI	Jump on Index Incremented	6 μsec
77	NOP	No Operation	5 μsec

*Optional commands

TABLE 3-3
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
		Load And Store Instructions	
03	STB	Store B The contents of B replace the contents of the memory word at the effective address. The contents of B are unchanged.	10 μsec
04	STC	Store Command Portion of A The contents of A, bits 1-9, replace the contents of the memory word, bits 1-9, at the effective address. The contents of A and the address portion of the memory word, bits 10-24, are unchanged.	10 μsec
05	STA	Store A The contents of A replace the contents of the memory word at the effective address. The contents of A are unchanged.	10 μsec
06	STD	Store Address Portion of A The contents of A, bits 10-24, replace the contents of the memory word, bits 10-24, at the effective address. The contents of A and the OP-code portion of the memory word, bits 1-9, are unchanged.	10 μsec
23	LDB	Load B The contents of the memory word at the effective address replace the contents of B. The contents of the memory word are unchanged.	10 μsec
24	LDA	Load A The contents of the memory word at the effective address replace the contents of A. The contents of the memory word are unchanged.	10 μsec
55	TAB	Transfer A to B The contents of A replace the contents of B. The contents of A are unchanged. The address portion and index bits of this instruction bits 10-24 and 2-3, are not interpreted.	5 μsec

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
57	IAB	Interchange A and B The contents of A and B are interchanged. The address portion and index bit of this instruction, bits 10-24 and 2-3, are not interpreted.	10 μsec
60	CRA	Clear A The contents of A, bits 1-24, are set to ZEROS. The address portion and index bits of this instruction, bits 10-24 and 2-3, are not interpreted.	5 μsec
		Arithmetic Instructions	
10	ADD	Add The contents of the memory word at the effective address are algebraically added to the contents of A, and the resultant sum replaces the contents of A. Overflow is possible and will set the overflow indicator. If the magnitude of the result is zero, the initial sign of A is unchanged. The contents of B and the memory word are unchanged.	10 μsec
11	SUB	Subtract The contents of the memory word at the effective address are algebraically subtracted from the contents of A, and the resultant difference replaces the contents of A. Overflow is possible and will set the overflow indicator. If the magnitude of the result is zero, the initial sign of A is unchanged. The contents of B and the memory word are unchanged.	10 μsec
20	ADM	Add Magnitude The magnitude of the contents of the memory word at the effective address are added to the contents of A, and the resultant sum replaces the contents of A. The sign of the memory word is ignored; if the sign of A is negative, a subtractive process will occur. Overflow is possible and will set the overflow indicator. If the magnitude of the result is zero, the initial sign of A is unchanged. The contents of B and the memory word are unchanged.	10 μsec

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
21	SBM	Subtract Magnitude The magnitude of the contents of the memory word at the effective address are subtracted from the contents of A, and the resultant difference replaces the contents of A. The sign of the memory word is ignored; if the sign of A is negative, an add will occur. Overflow is possible and will set the overflow indicator. If the magnitude of the result is zero, the initial sign of A is unchanged. The contents of B and the memory word are unchanged.	10 μsec
30	SMP	Step Multiple Precision The contents of the memory word at the effective address are added to or subtracted from A such that the result has the sign of the result of the overall multiple precision operation. This signal and the selection of either add or subtract is determined by the nearest previous ADD or SUB instruction executed prior to the SMP instruction. Normally, this will take place at the beginning of a multiple precision routine. The add or subtract operation is for initial set-up of the multiple precision routine only; the sum or difference is not to be used further. For a multiple precision add an ADD operation of the highest order portion of the two operands will be followed by SMP instructions which add all portions, starting with the lowest order and producing the same signs. For a multiple precision subtract, a SUB operation of the highest order portion of the two operands will be followed by SMP instructions which subtract all portions, starting with the lowest order and producing the same signs. Any carry (or borrow) produced by an SMP step will be properly added (or subtracted) at the following SMP. Overflow is set by the SMP command as in a normal ADD or SUB instruction. Overflow of a multiple precision addition or subtraction can be detected by checking the overflow indicator after completion of the operation (normally it would not be set after the last SMP operation).	10 μsec

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
34	MPY	Multiply The contents of B are multiplied by the contents of the memory word at the effective address. The 23 most significant bits of the 46-bit product replace the contents of A, bits 2-24; the least significant bits replace the contents of B, bits 2-24. The signs of A and B are set to the algebraic sign of the product. The contents of A are cleared at the start of this instruction. The contents of the memory word are unchanged. The B register must be loaded prior to the execution of the MPY instruction.	30 μsec
35	DIV	Divide The contents of the memory word at the effective address (the divisor) are divided into the contents of both A and B (the double-length dividend). The 23-bit quotient replaces the contents of B, bits 2-24; the 23-bit remainder replaces the contents of A, bits 2-24. The sign of B is set to the algebraic sign of the quotient; the sign of A is unchanged. If the initial magnitude of A is equal to or greater than the magnitude of the memory word, the improper divide indicator is set. The contents of the memory word are unchanged.	32 μsec
36	BCD*	BCD to Binary Conversion The contents of the memory word at the effective address are converted from BCD into binary; the result replaces the contents of A. The contents of B are destroyed; the contents of the memory word are unchanged. The maximum BCD number which can be converted with this instruction is decimal ±799, 999.	33 μsec
37	BIN*	Binary to BCD Conversion The contents of the memory word at the effective address are converted from binary to BCD code; the result replaces the contents of B. The conversion will be performed only on those bits of the memory word which will produce a	33 μsec

*Optional commands

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
		BCD code within the capacity of the B register (24 bits). The improper divide indicator will be set if the binary number to be converted is greater than octal 3,032,377, resulting in a BCD number greater than decimal 799,999. The original contents of A are destroyed; the contents of the memory word are unchanged.	
62	RND	Round A The contents of A are incremented by one if bit 2 in the B register is a ONE; the contents of A are unchanged if bit 2 (in B) is a ZERO. The address portion and index bits of this instruction, bits 10-24 and 2-3, are not interpreted. Overflow is possible and will set the overflow indicator. The contents of B remain unchanged.	5 μsec
		Logical Instructions	
15	ANA	AND to A This instruction forms the logical product of the contents of A, bits 1-24, and the contents of the memory word at the effective address and replaces the contents of A with the result. For each ZERO in the contents of the memory word, a ZERO is written into the corresponding bit in A; for each ONE in the memory word, the corresponding bit in A is unchanged. The contents of B and the memory word are unchanged.	10 μsec
16	ORA	OR to A This instruction forms the logical sum of the contents of A, bits 1-24, and the contents of the memory word at the effective address and replaces the contents of A with the result. For each ONE in the contents of the memory word, a ONE is written into the corresponding bit in A; for each ZERO in the memory word, the corresponding bit in A is unchanged. The contents of B and the memory word are unchanged.	10 μsec

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
17	ERA	Exclusive OR to A This instruction forms the logical exclusive sum of the contents of A, bits 1-24, and the contents of the memory word at the effective address and replaces the contents of A with the result. For each ONE in the contents of the memory word, the corresponding bit in A is complemented; for each ZERO in the memory word, the corresponding bit in A is unchanged. The contents of B and the memory word are unchanged.	10 μsec
		Shift Instructions	
40	ARS	A Right Shift The contents of A, bits 2-24, are shifted to the right the number of positions specified by the six least significant bits of the instruction, bits 19-24. The sign of A is not shifted and is unchanged. ZEROs are shifted into the vacated position next to the sign of A, bit 2; bits shifted out of the low-order position are lost. This instruction may be indexed, in which case the number of shift steps is the sum of the address portion of the instruction and the contents of the index register. The contents of B are unchanged.	5 + n μsec*
41	ALS	A Left Shift The contents of A, bits 2-24, are shifted to the left the number of positions specified by the six least significant bits of the instruction, bits 19-24. The sign of A is not shifted and is unchanged. ZEROs are shifted into the vacated low-order position next to the sign of A (bit 2) are lost. If a non-zero bit is shifted out of the position next to the sign of A, the overflow indicator is set. This instruction may be indexed, in which case the number of shift steps is the sum of the address portion of the instruction and the contents of the index register. The contents of B are unchanged.	5 + n μsec*

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
42	LRR	Long Right Rotate The contents of A, bits 1-24, and B, bits 1-24, are treated as a single 48-bit register and are rotated to the right (end around carry) the number of positions specified by the six least significant bits of the instruction, bits 19-24. The signs of A and B are also shifted. Bits shifted out of the low-order position of A enter the high-order position of B; bits shifted out of the low-order position of B enter the high-order position of A. This instruction may be indexed, in which case the number of shift steps is the sum of the address portion of the instruction and the contents of the index register.	5 +nμsec*
43	LLR	Long Left Rotate The contents of A, bits 1-24, and B, bits 1-24, are treated as a single 48-bit register and are rotated to the left (end around carry) the number of positions specified by the six least significant bits of the instruction, bits 19-24. The signs of A and B are also shifted. Bits shifted out of the high-order position of B enter the low-order position of A; bits shifted out of the high-order position of A enter the low-order position of B. The instruction may be indexed, in which case the number of shift steps is the sum of the address portion of the instruction and the contents of the index register.	5 +nμsec*
44	LRS	Long Right Shift The contents of A, bits 2-24, and B, bits 2-24, are treated as a single 46-bit register and are shifted to the right the number of positions specified by the six least significant bits of the instruction, bits 19-24. The signs of A and B are not shifted; however, the sign of B is made to agree with the sign of A. ZEROs are shifted into the vacated position next to the sign of A, bit 2; bits shifted out of the low-order position of A enter the position next to the sign of B, bit 2. Bits shifted out of the low-order position of B are lost. This instruction may be indexed, in	5 +nμsec*

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
		which case the number of shift steps is the sum of the address portion of the instruction and the contents of the index register.	
45	LLS	Long Left Shift The contents of A, bits 2-24, and B, bits 2-24, are treated as a single 46-bit register and are shifted to the left the number of positions specified by the six least significant bits of the instruction, bits 19-24. The signs of A and B are not shifted; however, the sign of A is made to agree with the sign of B. ZEROs are shifted into the vacated low-order position of B; bits shifted out of the position next to the sign of B, bit 2, enter the low-order position of A. Bits shifted out of the position next to the sign of A, bit 2, are lost. If a non-zero bit is shifted out of the position next to the sign of A, the overflow indicator is set. This instruction may be indexed, in which case the number of shift steps is the sum of the address portion of the instruction and the contents of the index register.	5 + n μsec*
46	NRM	Normalize The contents of A, bits 2-24, and B, bits 2-24, are treated as a single 46-bit register and are shifted left until a ONE is shifted into the position next to the sign of A, bit 2, or until A and B contain all ZEROs (46 steps). If an index register is specified, the number of shifts (N) required for normalization is subtracted from the index register. If no index register is specified, the index register is not affected by this instruction. ZEROs are shifted into the vacated low-order position of B; bits shifted out of the position next to the sign of B, bit 2, enter the low-order position of A. If a ONE is in the position next to the sign of A, bit 2, at the start of the operation (already normalized), the instruction will be treated as a NOP. The signs of A and B are not shifted and are unchanged.	5 + n μsec

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
47	LGL	Logical Left Shift The contents of A, bits 1-24, are shifted to the left the number of positions specified by the six least significant bits of the instruction bits 19-24. The sign of A is also shifted. ZEROs are shifted into the vacated low-order position of A; bits shifted out of the high-order position of A are lost. This instruction may be indexed, in which case the number of shift steps is the sum of the address portion of the instruction and the contents of the index register. The contents of B are unchanged.	5 + nμsec
64	SCR	Scale Right The contents of A, bits 2-24, and B, bits 2-24, are treated as a single 46-bit register and are shifted to the right the number of positions specified by the six least significant bits of the instruction, bits 19-24. If an index register is specified, the address portion of this instruction, bits 10-24, will be added to the contents of the index register. The signs of A and B are not shifted; however the sign of B is made to agree with the sign of A. ZEROs are shifted into the vacated position next to the sign of A, bit 2; bits shifted out of the low-order position of A enter the position next to the sign of B, bit 2. Bits shifted out of the low-order position of B are lost. If the index position, bit 3, is a ZERO, the SCR will operate as the LRS instruction (44).	5 + nμsec
65	SCL	Scale Left The contents of A, bits 2-24, and B, bits 2-24, are treated as a single 46-bit register and are shifted to the left the number of positions specified by the six least significant bits of the instruction, bits 19-24. If an index register is specified, the address portion of this instruction, bits 10-24, will be subtracted from the contents of the index register. The signs of A and B are not shifted; however, the sign of A is made to agree with the sign of B. ZEROs are shifted into the vacated low-order position of B; bits shifted out of the position	5 + nμsec

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
		next to the sign of B, bit 2, enter the low-order position of A. Bits shifted out of the position next to the sign of A, bit 2, are lost. If a non-zero bit is shifted out of the position next to the sign of A, the overflow indicator is set. If no index register is specified, the SCL will operate as the LLS instruction (45).	
		Jump Instructions	
12	SKG	Skip if A Greater The contents of A are algebraically compared to the contents of the memory word at the effective address. If the value in A is greater than the value in the memory word, the next instruction is skipped and the computer resumes at that point. If the value in A is equal to or less than the value in the memory word, the computer takes the next sequential instruction. The contents of A and the memory word are unchanged.	10 μsec
13	SKN	Skip if A Not Equal The contents of A, bits 1-24, are logically compared to the contents of the memory word at the effective address. If any of the bits in A is not equal to the corresponding bit in the memory word, the next instruction is skipped and the computer resumes at that point. If bits 1-24 in A are equal to the corresponding bits in the memory word, the computer takes the next sequential instruction. The contents of A and the memory word are unchanged.	10 μsec
25	JRT	Jump Return The JRT instruction is used to return program control to an interrupted program. The computer will take its next instruction from the location specified by the address portion of the memory word, bits 10-24, at the effective address. The contents of the memory word, bits 1-9, are used to restore certain internal flip-flops to their condition at the time the interrupt occurred. The	10 μsec

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
		JRT instruction must be the last instruction executed in an interrupt program. If the standard interrupt is used, this instruction will restore the capability of being interrupted. If priority interrupt (optional) is used, this instruction will return program control to the interrupted priority level. The contents of the memory word, bits 1-24, are not changed.	
27	JST	Jump and Store Location The location of the JST instruction plus one replaces the contents of the address portion of the memory word, bits 10-24, at the effective address. A jump is then executed to one location beyond the effective address. Bits 1-9 of the contents of the memory word are unchanged; the contents of A and B are unchanged. This instruction may be used for entering a subroutine.	10 μsec
70	JPL	Jump if A Plus If the sign of A, bit 1, is positive (ZERO), the computer takes its next instruction from the memory word at the effective address and continues from there. If the sign of A, bit 1, is negative (ONE), the computer takes the next sequential instruction. Thus, a jump for A negative could be accomplished by an unconditional jump instruction (JMP) immediately following the JPL instruction. The contents of A are unchanged.	5 μsec
71	JZE	Jump if A Zero If all of the magnitude positions in A, bits 2-24, are ZEROs, the computer takes its next instruction from the memory word at the effective address and continues from there. If any of the magnitude positions of A are ONEs, the computer takes the next sequential instruction. The sign of A, bit 1, is ignored. The contents of A are unchanged.	5 μsec
73	JOF	Jump on Overflow If the overflow indicator is set, it will be reset and the computer will take its next instruction from the memory word at the effective address and continue from there. If the overflow indicator is	5 μsec

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
		not set, the computer takes the next sequential instruction. To reset the overflow indicator without altering the normal sequence of instruction, the JOF instruction may be used with an effective address that is one location greater than the address of the JOF instruction.	
74	JMP	Unconditional Jump The computer takes its next instruction from the memory word at the effective address and continues from there. The JMP instruction with indirect addressing may be used for returning from subroutines which are not interrupt routines.	5 μsec
		Index Instructions	
54	ADX	Add to Index The contents of the address portion of this instruction, bits 10-24, are added to contents of the specified index register, and the resultant sum replaces the contents of the index register. Overflow of the index register is possible, but will be ignored. If the indirect address position of the instruction, bit 1 is a ONE, the contents of the address portion of the memory word, bits 11-24, at the effective address are added to the index register specified in the memory word. The contents of A and the memory word are unchanged. If no index register is specified, the ADX will be treated as a NOP.	5 μsec
56	LDX	Load Index The contents of the address portion of this instruction, bits 10-24, replace the contents of the specified index register. If the indirect address position of the instruction, bit 1, is a ONE, the contents of the address portion of the memory word, bits 10-24, at the effective address replace the contents of the index register specified in the memory word. The contents of A and the memory word are unchanged. If no index register is specified, the LDX will be treated as a NOP.	5 μsec

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
63	TAX	Transfer A to Index The address portion of A, bits 10-24, replace the contents of the specified index register. The contents of A are unchanged. If no index register is specified, the TAX will be treated as a NOP. The address portion of this instruction, bits 10-24, are not interpreted.	5 μsec
66	STX	Store Index The contents of the specified index register replace the contents of the address portion of the memory word, bits 10-24, at the effective address. The contents of A and the index are unchanged; bits 1-9 of the memory word are unchanged. If no index register is specified all ONEs are stored in the address portion of the memory word.	10 μsec
67	IRX	Increment, Replace, and Load Index The contents of the address portion of the memory word, bits 10-24, at the effective address are incremented by one. If an index register is specified the resulting sum replaces the contents of the address portion of the memory word and the index register. The contents of A are unchanged. Thus, it is possible to have many "index registers" in memory that can be incremented, saved, and made available for use in indexing operations, all with one instruction. If no index register is specified the address portion of the memory word will be incremented and this incremented value will replace the contents of the address portion of A and the memory word. In this case, the contents of the index register are unchanged. Any carry from bit 10 is ignored. Bits 1-9 of the memory word are unchanged; bits 1-9 of the A register are set to ZEROs.	13 μsec

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
72	JIX	Jump on Index If the contents of the specified index register are not ZERO, the computer takes its next instruction from the memory word at the effective address and continues from there. If the contents of the index register are ZERO, the computer takes the next sequential instruction. If no index register is specified the JIX will be treated as a NOP.	5 μsec
75	JXI	Jump on Index Incremented The contents of the specified index register are incremented by one and the resulting sum replaces the contents of the index register. If this resulting sum is not ZERO, the computer takes its next instruction from the memory word at the effective address and continues from there. If the sum is ZERO, the computer takes the next sequential instruction. If no index register is specified, the JXI will be treated as a NOP.	7 μsec
		Input-Output Instructions	
07	INM	Input to Memory The input word from a previously enabled input channel (refer to OCP) replaces the contents of the memory word at the effective address.	10 μsec
22	OTM	Output from Memory The contents of the memory word at the effective address are transferred as output to the previously enabled output channel (refer to OCP). The contents of the memory word are unchanged.	10 μsec
31	FMB	Fill Memory Block This instruction is used for high-speed input into the block of consecutive memory locations starting with the memory word at the effective address. Once started, the sequence continues	variable

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
		without interruption, controlled asynchronously by an external ready signal. The FMB instruction may operate with any input channel that has been previously enabled (refer to OCP). The contents of the specified index register are incremented by one for each word being stored, thereby increasing the effective address. Execution of this instruction may be terminated by either an external signal (e.g., a stop code) or upon the contents of the index register having become all ZEROs. If no index register is specified, the FMB will be treated as a NOP. The FMB instruction can process input data at a 166 KC word rate.	
32	DMB	Dump Memory Block This instruction is used for high-speed output from the block of consecutive memory locations starting with the memory word at the effective address. Once started, the sequency continues without interruption, controlled asynchronously by an external ready signal. The DMB instruction may operate with any output channel that has been previously enabled (refer to OCP). The contents of the specified index register are incremented by one for each output word being transferred, thereby increasing the effective address. Execution of this instruction may be terminated by either an external signal or upon the contents of the index register having become all ZEROs. If no index register is specified, the DMB will be treated as a NOP. The DMB instruction can process output data at a 166 KC word rate.	variable
50	OTA	Output from A The contents of the A register are transferred as output to the previously enabled output channel. If bit 10 of this instruction contains a ONE, bits 19-24 form a 6-bit mask. This provides a facility for flexible formatting of character outputs. For ZERO mask bits, there will be corresponding ZERO bits in the output; for ONE mask bits, the corresponding bits in A will be the output.	5 μsec

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
		If bit 10 contains a ZERO, 24-bit output words are transferred by this instruction. The index position of the instruction, bits 2-3, are not interpreted. The contents of A are unchanged.	
51	ITC	Interrupt Control Interrupt is enabled if bit 10 of this instruction contains a ONE; interrupt is inhibited if bit 10 contains a ZERO. The index position and the remaining positions of the address portion of the instruction, bits 2-3 and 11-24, are not interpreted.	5 μsec
52	INA	Input to A The input word from a previously enabled input channel (see OCP) replaces the contents of A. If bit 10 of this instruction contains a ONE, bits 19-24 form a 6-bit mask. This provides a facility for flexible formatting of character inputs. For ZERO mask bits, the corresponding bits in A are unchanged; for ONE mask bits, the corresponding input bits will replace the contents of A. If bit 10 contains a ZERO, 24-bit input words are transferred by this command. The index position of the instruction, bits 2-3, are not interpreted.	5 μsec
53	OCP	Output Control Pulse An output pulse is generated by this instruction for the control of input-output channels and external equipment. The address portion, bits 10-24, specifies the unit to be selected, the type of control, etc. (refer to Appendix C for the code assignments). The index position of the instruction, bits 2-3, are not interrupted.	5 μsec

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
61	SKS	Skip if Sense Line Not Set The sense line specified by the address portion of this instruction, bits 11-24, is interrogated. If the sense line is not set, the computer skips the next instruction and continues from there; if the sense line is set, the computer will take the next sequential instruction. The lines that may be tested include 10 internal sense lines (six sense switches, overflow indicator, improper divide indicator, input parity, and stop code), ready signals of input-output channels and external sense lines from peripheral equipment (busy status, parity errors, etc.). From one to ten of the internal sense lines may be tested simultaneously, in which case any or all of the tested sense lines may cause a skip. For the channel-ready sense lines, similar simultaneous testing is also possible. If the most significant address position of the instruction, bit 10, is a ONE, the flip-flop associated with the tested sense line is reset for certain assignments. Appendix D contains the sense line selection assignments. The index positions of the instruction, bits 2-3, are not interpreted.	5 μsec
		Control Instructions	
00	HLT	Halt The computer will halt until the START button is manually depressed (see description of operation), at which time execution will be resumed at the next sequential instruction. The index positions and address portion of this instruction, bits 2-3, and 10-24, are not interpreted.	5 μsec
02	XEC	Execute The instruction in the memory word at the effective address is executed. After execution of the specified instruction, the computer takes the next sequential instruction following the XEC instruction and continues from there. If the	5 μsec + variable

TABLE 3-3 (Cont)
COMMAND REPERTOIRE

Code	Mnemonic	Description	Execution Time
		executed instruction involves a jump, the computer takes its next instruction from the jump destination and continues from there; if the executed instruction involves a skip, the skip will be relative to the XEC instruction and not the instruction at the effective address.	
77	NOP	No Operation No operation is performed by this instruction. The computer will take the next sequential instruction and continue from there. The index positions and address portion of this instruction, bits 2-3 and 11-24, are not interpreted.	5 μsec

3-5 OCP ADDRESS CODES

Table 3-4 is a list of assigned codes to be used in the address portion of the OCP instruction to perform the specified functions. The codes are given in octal notation; x indicates number of unit.

TABLE 3-4
ENABLE I/O CHANNELS

00000	Standard character buffer, in and out
00001	Standard parallel input channel
00002	Standard parallel output channel
00003 thru 00075	Additional I/O channels
00076	FBC/DMA initial set up channel
00077	Disable all I/O channels
	Word Buffer
003mx	Word buffer control (8 possible)
	NOTE: m = number of characters per word x = word forming buffer MODE (in or out)
	Miscellaneous
01000	Enable stop code punch
01001 thru 01777	General purpose control pulses for external devices (01010 thru 01017 standard with DDP-24)
	Typewriter
0200x	Typewriter input select (keyboard enabled)
0201x	Typewriter output select (keyboard inhibited)
02070	Disconnect all three standard devices on standard I/O character buffer.
	Note Selection of a standard device on the standard I/O character buffer automatically disconnects any other standard device which is connected to it.
	Note x = 0 corresponds to standard typewriter
	Paper Tape Reader
0210x	Paper-Tape Reader Start and Select
	Note x = 0 corresponds to standard paper-tape reader
	Paper Tape Punch
0220x	Paper-Tape Punch Select
	Note x = 0 corresponds to standard paper-tape punch

TABLE 3-4 (Cont)
ENABLE I/O CHANNELS

	Line Printer
02300	Enable print buffer to accept 6-bit characters
02301	Enable print buffer to accept 24-bit words
02302	Print contents of buffer
02310	Advance carriage to punch in channel 1 of control tape (assigned to top of form)
02311	Advance carriage to punch in channel 2 of control tape
02312	Advance carriage to punch in channel 3 of control tape
02313	Advance carriage to punch in channel 4 of control tape
02314	Advance carriage to punch in channel 5 of control tape
02315	Advance carriage to punch in channel 6 of control tape
02316	Advance carriage to punch in channel 7 of control tape
02317	Advance carriage to punch in channel 8 of control tape (assigned to single space)
02304	Advance carriage one line (channel 8 of control tape)
	Card Reader
02400	Read one Hollerith card
02401	Read one binary card
02410	Read Hollerith cards continuously
02411	Read binary cards continuously
02420	Stop card reader
	Card Punch
02500	Card punch select
	Digital X-Y Plotter Control (2 possible)
026nn	Plotter No. 1
027nn	Plotter No. 2
nn	specifies function as follows: 01 Step - Y (carriage right) 02 Step + Y (carriage left) 04 Step - X (drum up) 05 Step - X, - Y 06 Step - X, + Y 10 Step + X (drum down) 11 Step + X, - Y 12 Step + X, + Y 20 Plotter pen down 40 Plotter pen up
	Magnetic Tape Control
200XY	Read (ODD PARITY)
202XY	Write (ODD PARITY)
204XY	Write End-of-File
203XY	Skip one file
304XY	Rewind
	IBM Compatibility
201XY	Read (EVEN PARITY)
203XY	Write (EVEN PARITY)

TABLE 3-4 (Cont)
ENABLE I/O CHANNELS

	Note
	X = master control unit number Y = slave unit number
	A-D and D-A Control
04000 thru 04377	A-D control (to be specified)
	Digital Resolver
05000	T mode with prescaling
05001	T mode without prescaling
05002	T* mode with prescaling
05003	T* mode without prescaling
05004	H mode with prescaling
05005	H mode without prescaling
05006	H* mode with prescaling
05007	H* mode without prescaling
05010	Sequential load of DR; start with Y
05011	Sequential load of DR; start with X
05012	Sequential load of DR; start with W
05013	Sequential DR output; start with Y
05014	Sequential DR output; start with X
05015	Sequential DR output; start with W

3-6 SENSE LINE CODES

The 14-bit address portion of the SKS command represents sense lines as follows.

3-6.1 Internal Sense Lines

The internal sense lines for possible simultaneous tests are illustrated in Figure 3-4.

3-6.2 External Sense Lines

Sixteen (16) sense lines are provided with the standard DDP-24. To test these lines, the address portion of the SKS command corresponds to 20000 through 20007 and 30000 through 30007. These are listed in Table 3-5.

TABLE 3-5
SENSE LINE CODES

Line Printer

22300 Printer busy
22301 Parity error
22302 Paper advancing

Card Reader

22400 Card reader busy
22401 Stop code*
22402 Not ready

Card Punch

22500 Punch busy
22501 Ready to punch next row
22502 Not ready

Magnetic Tape

310XO Master unit busy
311XY Slave unit rewinding
312XO End-of-tape encountered
313XO Beginning-of-tape encountered
314XO End-of-file encountered

Note

If bit 10 of the SKS command word is a ONE, the assigned flip-flops tested by the SKS command are also reset.

*Flip-flop tested can be reset by SKS command.

3-7 DDP-24 CHARACTER CODES

The character codes for the DDP-24 are listed in Table 3-6.

TABLE 3-6
DDP-24 CHARACTER CODE

OCTAL CODE	TYPEWRITER L/C	TYPEWRITER U/C	PAPER TAPE 8	7	6	P	4	S	3	2	1	
00	Ø	b				O		•				
01	1	■						•			O	
02	2	■						•		O		
03	3	■				O		•		O	O	
04	4	:						•	O			
05	5	@				O		•	O		O	
06	6	√				O		•	O	O		
07	7	>						•	O	O	O	
10	8	■					O	•				
11	9	■				O	O	•			O	
13	#	-					O	•		O	O	
20	*	¢			O			•				
21	/	■			O	O		•			O	
22	S	n			O	O		•		O		
23	T	■			O			•		O	O	
24	U	≡			O	O		•	O			
25	V	%			O			•	O		O	
26	W	"			O			•	O	O		
27	X	'			O	O		•	O	O	O	
30	Y	■			O	O	O	•				
31	Z	■			O		O	•			O	
33	'	■			O	O	O	•		O	O	
40	-	-		O				•				
41	J	■		O		O		•			O	
42	K	■		O		O		•		O		
43	L	■		O				•		O	O	
44	M	)		O		O		•	O			
45	N	*		O				•	O		O	
46	O	△		O				•	O	O		
47	P	;		O		O		•	O	O	O	
50	Q	■		O		O	O	•				
51	R	■		O			O	•			O	
52	tab			O			O	•		O		
53	$	■		O		O	O	•		O	O	
54	backspace*			O			O	•	O			**
56	space			O		O	O	•	O	O		
60	&	&		O	O	O		•				
61	A	¢		O	O			•			O	
62	B	■		O	O			•		O		
63	C	■		O	O	O		•		O	O	
64	D	(		O	O			•	O			
65	E	⌶		O	O	O		•	O		O	
66	F	‡		O	O	O		•	O	O		
67	G	<		O	O			•	O	O	O	
70	H	■		O	O		O	•				
71	I	■		O	O	O	O	•			O	
73	.	∨		O	O		O	•		O	O	
74	lower shift			O	O	O	O	•	O			
75	upper shift			O	O		O	•	O		O	
76	car. return			O	O		O	•	O	O		
77	line feed			O	O	O	O	•	O	O	O	
stop	backspace*		O	O		O	O	•	O			

NOTE: 1. The assembly program (DAP) will recognize the & (60_8) as a +
2. The assembly program (DAP) will recognize the line feed (77_8) as a delete

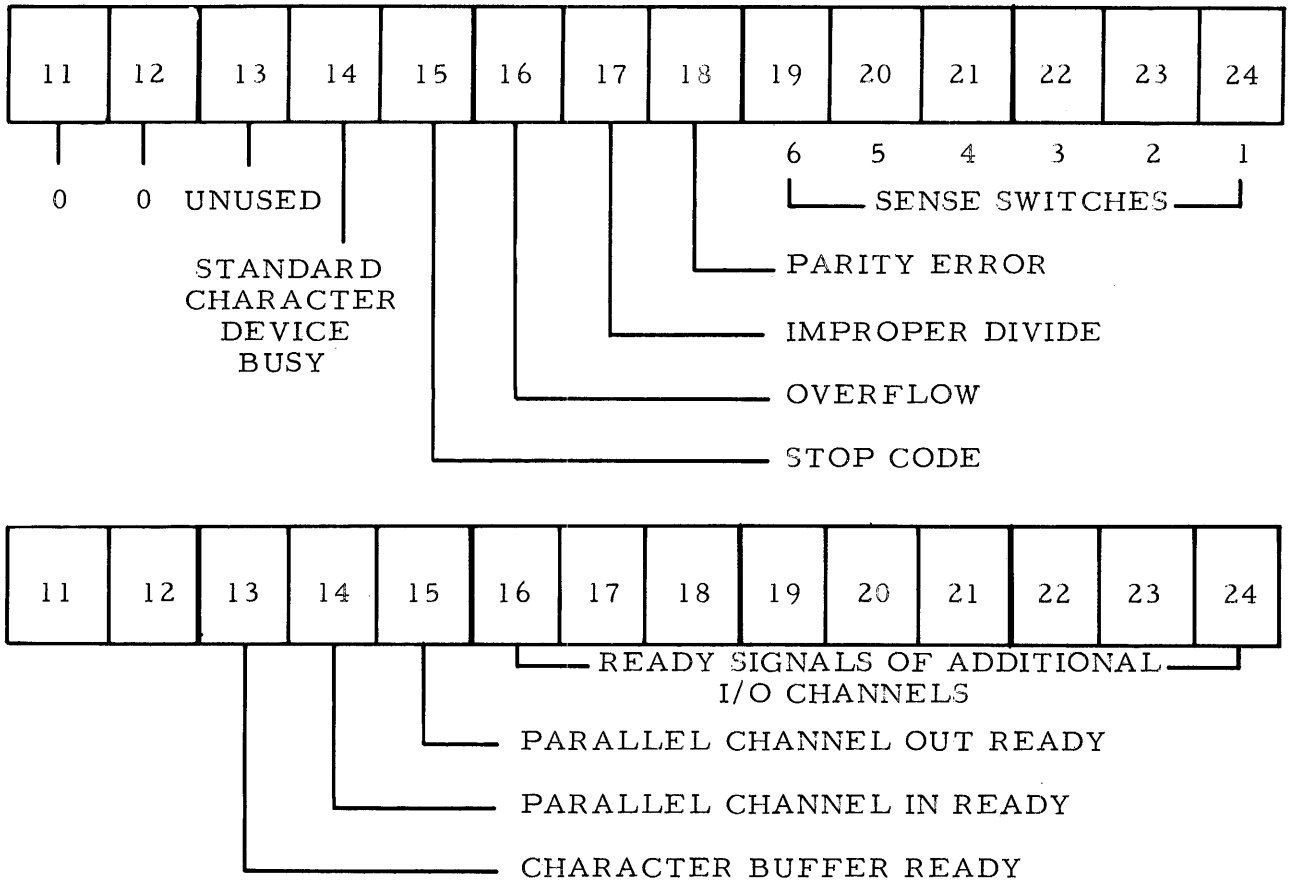


Figure 3-4. Internal Sense Lines (Simultaneous Test Possible)

SECTION IV
THEORY OF OPERATION

4-1 INTRODUCTION

A thorough understanding of the DDP-24 General Purpose Computer requires familiarity with the theory and application of the digital modules used in this system. Refer to Section V of the Instruction Manual for 1-MC S-PAC Digital Modules.

This section contains a complete functional description of the DDP-24 and a detailed theory of operation. Over-all block diagram explanations, detailed circuit analysis, and descriptions of the command instruction repertoire are included.

4-2 GENERAL SYSTEM OPERATION

Functionally, the DDP-24 consists of the arithmetic unit, the control unit, the input-output unit, and the memory units (Figure 4-1).

4-2.1 Arithmetic Unit

This unit contains the registers and the adder wherein the actual arithmetic operations take place during the computer program. The unit contains:

a. The A-Register – the main arithmetic 24-bit register,

b. The B-Register – the auxiliary arithmetic 24-bit register,

c. The Adder – the logic structure providing for sums or differences during computations, and

d. The Z-Register – a 24-bit register (considered a part of the arithmetic unit at certain times) that receives information from the memory. After a command fetch, the 15 least significant bits contain the address of the instruction, or the 15-bit operand in some cases. After an operand fetch, the Z-register contains the operand.

4-2.2 Control Unit

The timing of access to the memory for commands and operands, as called for by the program, is a function of the control unit. It also contains the execution of computer commands.

The control unit contains the program counter (P-register), the OP-code register (O-register), the transfer and AU buses, the control unit clock, and the clock matrix. The Z-register is sometimes considered a part of the control unit.

4.2.2.1 Program Counter (P-Register). - The memory location of the next instruction to be performed is contained in the P-register. Its contents are normally incremented

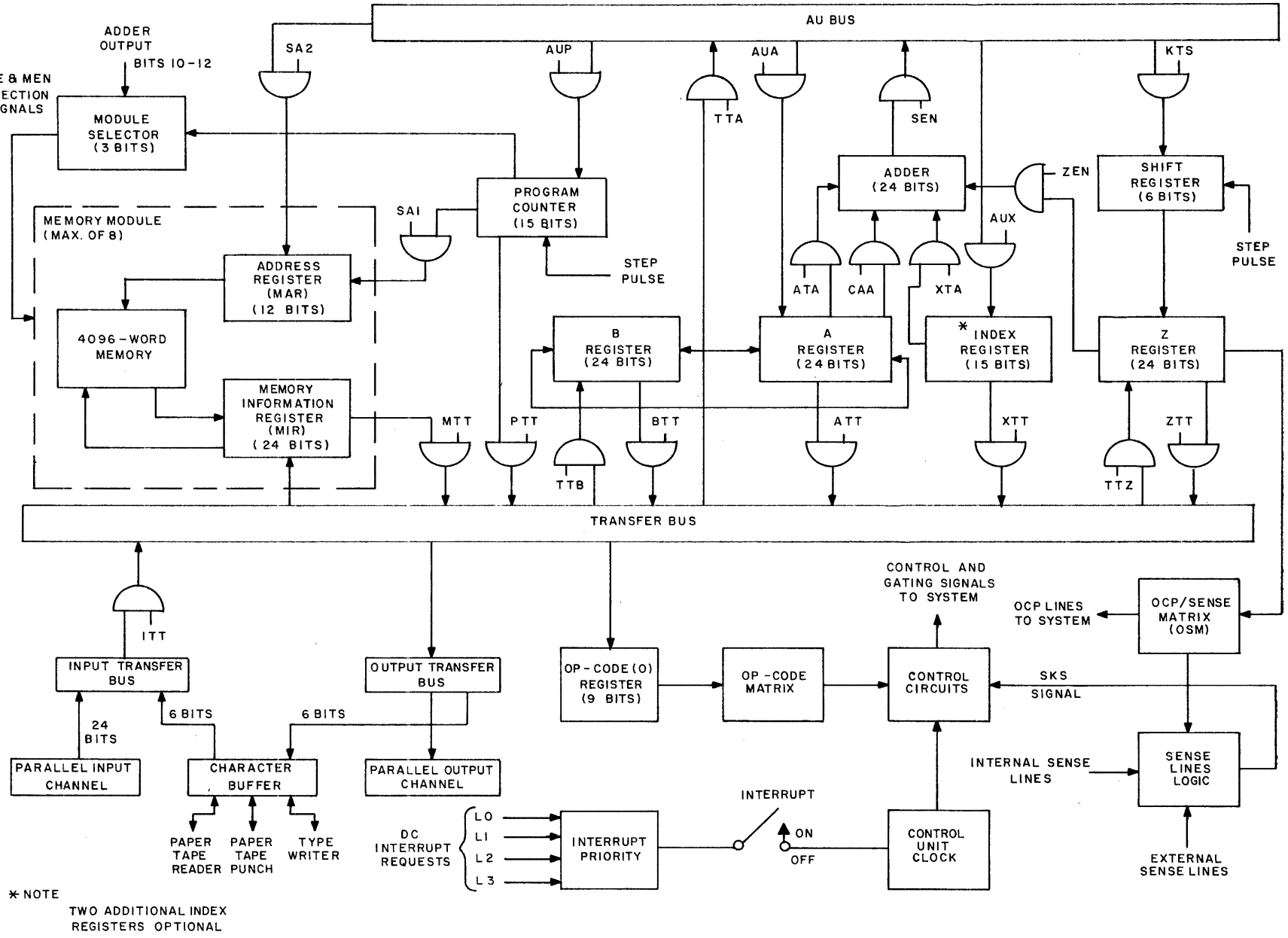


Figure 4-1. DDP-24 Simplified System Block Diagram

by one each time a new command is fetched from memory. In case of a jump, the program counter is loaded with the memory location to which the program is to jump. The P-register contains 15 bits.

4-2.2.2 OP-Code Register (O). - The 6-bit OP-code for the instruction being performed, the index bit, and the indirect address bit are contained in this register.

4-2.2.3 OP-Code Matrix (OCM). - This is a gating structure that decodes the 6-bit OP-code into different instruction controls.

4-2.2.4 Index Register (X). - When specified by an instruction, the contents of this register are added to the address of the instruction and the result becomes the effective address. There are a few instructions, such as scale and normalize, in which the 15-bit index register is used for control and counting.

4-2.2.5 Shift Counter (S). - Used with the shift instructions, the counter indicates the number of shift steps. The Shift counter contains 6 bits.

4-2.2.6 Transfer Bus and AU Bus. - These are two gating structures to which computer registers are connected as a source and as a destination. Transfer of information from one register to another takes place by the simultaneous gating of the proper paths from one register to the bus and from the bus to the other register. The transfer bus and AU bus allow simple interconnections between the many different computer registers and the adder. Easy monitoring of computer operations during troubleshooting is thus provided.

4-2.2.7 Control Unit Clock. - This component generates the timing pulses needed for the different operation sequences of the command executions.

4-2.2.8 Clock Matrix. - In this unit, the control unit clock signals are properly gated with the outputs from the OP-code matrix to supply the correct sequence of signals for each command to be executed.

4-2.3 Input-Output Unit

The input-output unit controls the transfer of data between the processor and the external system. It contains:

a. The input-output channels with their channel ready and channel enable signals,

b. The automatic interrupt that forces the computer program to be interrupted and jump to an interrupt destination in memory,

c. The decoding of the incoming sense signals for test by the SKS instruction (Skip if Sense Line not Set), and

d. The outgoing control signals of the OCP command (Output Control Pulse).

The transfer of input-output information takes place on a separate input-output transfer bus connected to the computer transfer bus. This allows maximum flexibility and expandability of DDP input-output capabilities. Input-output data transfer can take place directly to or from any memory locations or the A-register.

4-2.4 Memory Unit

The memory, a magnetic core unit of 4,096 twenty-four-bit words, contains its own 24-bit information register (MIR) and address register (MAR). The memory transfers data to and from other units of the DDP computer via the transfer bus. The memory of the DDP-24 can optionally be expanded to 32,768 words by adding identical 4,096-word memory modules. Each module has a MIR and a MAR that can be operated independently under the control unit of (optionally) fully buffered input-output channel.

4-2.5 Word Formats

The word length of the DDP-24 is 24 bits. (See Figure 4-2.) A computer word can be either a command or a data word; the only difference is the interpretation by the computer. A command word (an OP-code, which is a numeric code for the operation, and an address) specifies the command to be executed. This generally specifies the memory cell from which the operand is to be read. In addition to the OP-code and address fields, there are address modification bits – an index bit, which specifies that the index register will be used with the operation, and an indirect addressing bit, which indicates that the indirect address mode will be used (refer to ADDRESSING MODES).

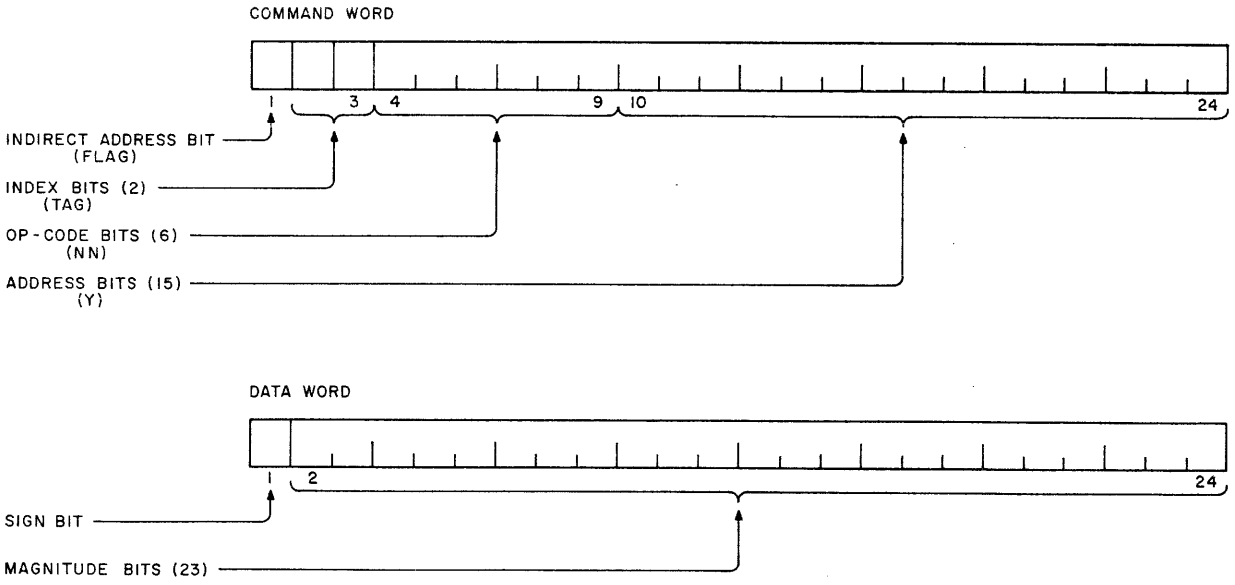


Figure 4-2. Word Formats

A data word is represented by a binary number. The sign bit when ZERO indicates a positive number and when ONE indicates a negative number. The remaining bits represent the numerical value. The DDP-24 uses sign-magnitude code, in which negative numbers differ only in sign from positive numbers. The magnitude portion represents the numerical value regardless of the sign.

The command word is also a binary number where the OP-code is given by bits 4 through 9, the address by bits 10 through 24. Bit 1 is for indirect address specification, bit 3 is the index bit, bit 2 (reserved for the addition of optional features,) is normally not interpreted by the command. In some cases the address portion carries information specifying additional operations, along with the OP-code bits. Shift commands are examples of this feature.

4-2.6 Addressing Modes

For commands involving an operand, an effective address in memory is to be specified for that operand. The following addressing modes are available.

a. Direct address: The address portion of the command word specifies the operand address; the 32,768 memory locations can be directly addressed.

b. Indexed address: The effective address is the sum of the address portion of the command word and the contents of the index register, specified by the index bit.

c. Indirect address: The effective address of the command word specifies a word stored in memory. The address portion of that word is the address of the operand. The indirect address mode is specified with an indirect address tag of ONE in the command word. Indirect addressing can be progressive e.g., if the address word stored in memory contains an indirect address bit of ONE itself, the operand address is to be found in the memory word specified by it, and so on.

Indexing takes precedence over indirect addressing. When the index bit and the indirect address bit are specified, the effective address containing the operand address is the sum of the address portion of the command word and the contents of the index register. In progressive indirect addressing, the effective address of each stage is determined by the indirect and index tags of the memory location from which it was fetched.

4-2.7 Fetch

There are four types of fetch cycles – normal fetch, XEC command fetch, indirect addressed command fetch, and an interrupt fetch. The first three types result in a memory read/restore cycle. The normal fetch cycle obtains a command word from the memory address specified by the program counter; the other two types read from the cell specified by the effective address. Figure 4-3 is a timing chart illustrating the machine functions generated for each of the four types of fetch cycles.

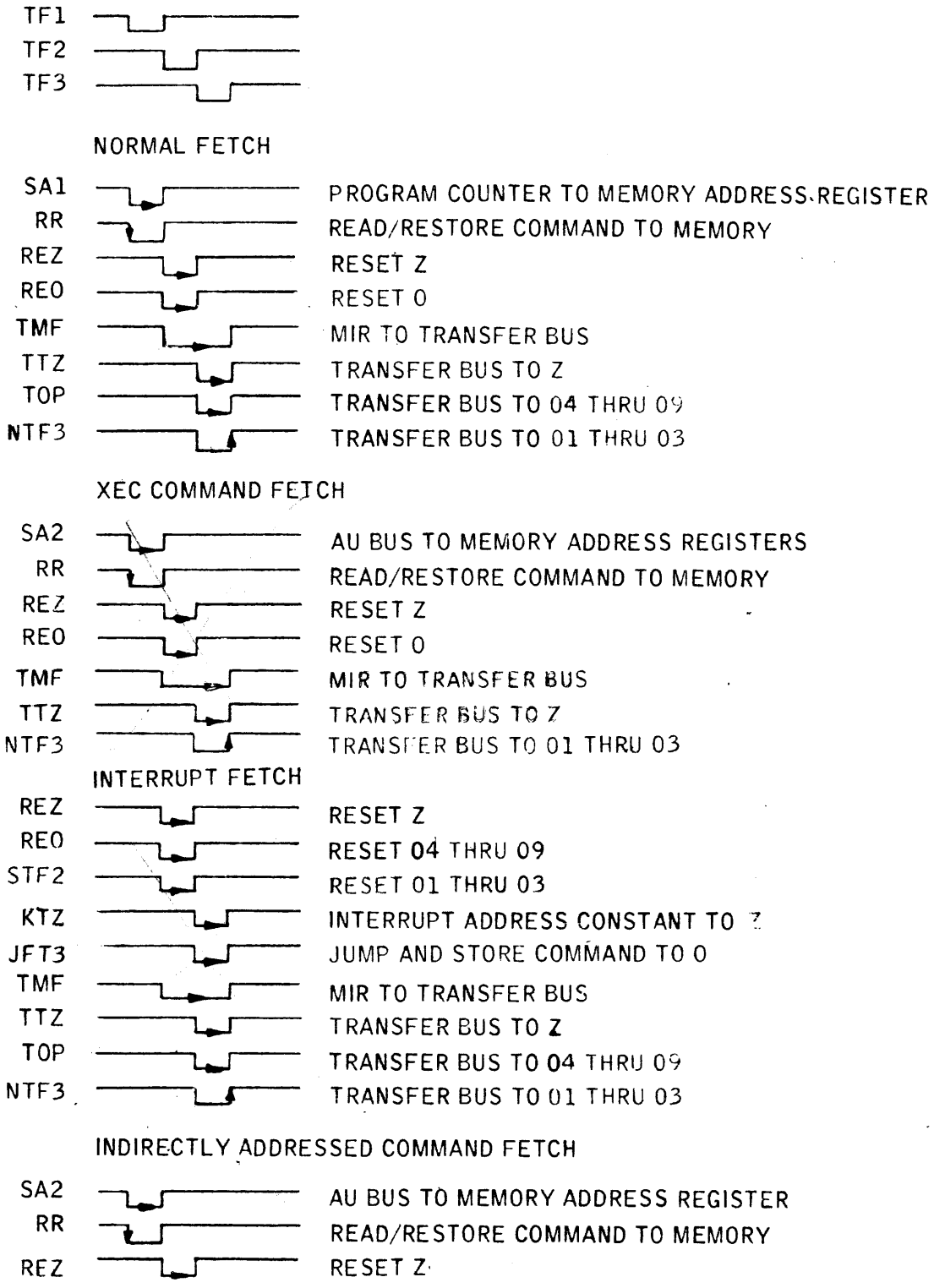


Figure 4-3. Fetch Cycles, Timing Chart

During the normal and XEC command fetch cycles the contents of the cell addressed replace the contents of the Z and O registers. The indirectly addressed command fetch cycle is similar, except that bits 4 through 9 of the O register remain undisturbed. The interrupt fetch cycle does not cause a memory access. During this cycle, the O register is set to the octal number 27, and bits 0 through 21 and bit 24 of the Z register are reset. The remaining bits (22 and 23) are selectively set or reset under control of the interrupt logic in the I/O unit.

4-2.8 Transition

The transition time (TT) is a test for entry into operate. Following the fetch cycle and if the indirect address bit is a ONE or the O register is loaded with 02_8 (XEC command), the operate domain will not be entered. Instead TT will initiate another fetch cycle using either the indirect address or the XEC command type. In these two instances, the period of TT is predictable (1 μsec).

Another case that causes TT to initiate a fetch cycle instead of an operate cycle is the normalizing shift when both A and B registers contain ZEROs. In this case, the period of TT may be 47 μsec.

The other functions that control the transition from fetch to operate do not preclude the entry into operate, but delay the action until certain conditions are met. The functions referred to are derivatives of the normalizing shift $(48)_8$ and the input-output group of commands. In the case of a normalized shift, the entry into operate is a function generated by the status of bit 2 in the A register. If A2 is a ZERO, the machine stays in transition time while the A and B registers are shifting. This status continues until a ONE is shifted into A2, at which time the operate domain is entered. The remaining condition that prolongs the transition from fetch to operate is when an attempt is made to process an input-output instruction when the channel is not ready. When this happens, the machine stays in transition time until ready status is achieved.

4-2.9 Operate

TO (operate time) is a function of the operation being executed and the time spent is variable. During TO the operate clock and the operation code matrix are combined to generate the active pulses and levels in the pertinent part of the machine. The operate clock is a one-shot pulse pattern generator normally triggered by TT. The operate clock pulse pattern along with the output of the operation code matrix determines the final pattern of pulses and levels to prevail during the execution of the command.

Figure 4-4 is a flow diagram of entry into operate. Five conditions can affect the entry into operate. Two cause reinitiation of a fetch cycle rather than entry into operate; two delay the starting of operate. The indirect address mode or the XEC command prevents entry into operate, while the normalized shift and input-output type commands delay the entry. Both delay functions are conditional. The normalized shift depends

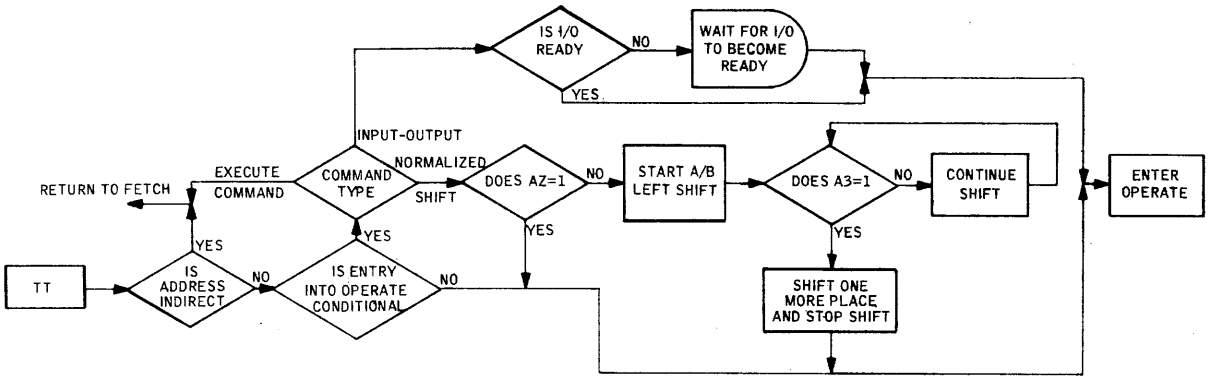


Figure 4-4. Entry Into Operate, Flow Diagram

on the status of the contents of A, and input-output depends on the ready status of the channel being processed. The fifth function that can delay the execution of an operation is a fully buffered/direct memory access channel. If the operation to be executed involves a memory access with the memory being used by the fully buffered/direct memory access channel, the operate clock is held in the initial position until the memory conflict disappears.

4-2.10 Fetch (Detailed)

A fetch cycle is normally 4 μsec in duration and consists of four sequential 1-μsec pulses (C8, TF1, TF2, and TF3) generated by shifting a ONE through a 4-stage shift register. Except for TF1, each stage of the counter is set by the preceding gating against the 1-MC clock. Each stage except TF3 is reset by the next sequential stage becoming set.

Stage TF1 was singled out as having different set logic than the other stages. In the case of TF1, the previous stage alone is not used as the set input. Instead, the previous stage (C8) is gated with a signal $\overline{\text{FDII}}$. While $\overline{\text{FDII}}$ is true, the setting of TF1 by C8 is initiated; if $\overline{\text{FDII}}$ is false, the C8 set input to TF1 is blocked. When $\overline{\text{FDII}}$ becomes true again, C8 sets TF1, causing C8 to extend in duration. The $\overline{\text{FDII}}$ signal is present only if the computer has a fully buffered channel and a memory module conflict exists, or if the computer has a direct memory access channel which is using memory at C8 time.

The reset logic of stage TF3 differs from that of the other stages because TF3 is reset by gating its output against the 1-MC clock. There are two reasons for the selected implementation of the reset of C8, TF1, and TF2. In the case of C8 the reason is that the $\overline{\text{FDII}}$ function controls the C8 to TF1 transfer. $\overline{\text{FDII}}$ may prevent C8 from transferring into TF1, thus the unsuccessful transfer into TF1 must be stored. C8 can store this fact if it is not reset until TF1 is set.

Because stages TF1 and TF2 are logically summed to form TMF, a 2-μsec pulse, it is desirable that the two have a time overlap. This overlap in time eliminates the presence of a narrow spike out of TMF during the TF1 to TF2 transition; the overlap is accomplished by holding TF1 set until TF2 is set.

The set input to C8 is enabled by an ENF signal following the execution of a command during an operate cycle and when the computer is cycling normally. If the computer is in a HALT condition, the active input to the set C8 logic is flip-flop C7. This flip-flop is set by one of four functions – three of them manual controls and one an interrupt function. The manual controls capable of setting C7, (and consequently initiating a fetch cycle) are START, FETCH-STOP, and SINGLE OPERATE. The interrupt function is the halt flip-flop (C1) gated with C22. C22 is an interrupt control flip-flop that stores the fact that an interrupt fetch cycle has been requested. The set-C8 signal is gated with a halt-interrupt function that disables the set input to C8 if the halt flip-flop (C1) is set and the interrupt line is false. Thus, the interrupt line is capable of overriding the effects of C1 on the set-C8 logic.

The leading edge of the 1-μsec pulse that gates against MCO1 to set C8 is used to set C23 if C22 is set. C23 is the interrupt cycle control flip-flop. The TF1, TF2, and TF3 flip-flops are gated with C23 to determine if the fetch cycle should be interpreted as an interrupt type.

4-2.11 Transition (Detailed)

Under normal conditions, transition time (TT) is a 1-μsec pulse used to test for entry into an operate cycle. During a normal machine cycle, TT is initiated by the last microsecond of fetch (TF3). TT may also be initiated by the execute flip-flop (C6) which is set by the EXECUTE button on the maintenance panel. Another manual control that influences the setting of TT is the FETCH-STOP switch.

4-2.12 Operate (Detailed)

The operate clock, used as a shift register, has nine flip-flop stages, TO1 through TO9. TO8 and TO9 are used only during the execution of one of the MUL, DIV, BIN, BCD or IRX instructions.

The normal duration of a TOX flip-flop is 1-μsec, but with two exceptions. TO1 can be prolonged during a program fill mode or during the FMB and DMB instructions when ready status (C4) is in a not-ready condition, TO8 is also prolonged during MUL, DIV, BIN or BCD instructions while the successive add-shift operations are being processed. All stages except TO7, TO8, and TO9 are reset by the set of the succeeding stage. This insures a time overlap between two successive stages. This overlap is desired in the OR gates used to generate 2 or 3 microsecond pulses.

The general concept of the operate clock is that a bit is inserted into stage TO1 and is shifted at a 1-MC rate through the successive stages; thus, a single bit travels

down the TO shift register. The output of each stage becomes a 1-μsec pulse. If two sequential stages are logically summed the result is a 2-μsec pulse.

This pattern of pulses generated by stages TO2 through TO7 is general and is not a function of the operation being performed. The only effect the operation being performed has on the pattern is its length. Figure 4-5 is a diagram of the pulse pattern developed by a bit starting in TO1 and shifting at the 1-MC rate through the nine stages of the operate clock. TO1 and TO8 can be prolonged under certain conditions, thus all functions of these stages are prolonged, i.e., for a TO1 of 10 μsec, T11 will be 10 μsec and T21 will be 11 μsec.

4-3 COMMAND EXECUTIONS

4-3.1 General

Simplified logical block diagrams will be used in this section to show the sequence of events during the execution of each instruction.

The next four paragraphs of this section are a discussion of the method used to access memory for an operand fetch or store. Previous to this access an effective address-used during T12 time by the memory-must be formed. During the first 2 μsec of operate, this address is normally present at the output of the adder. The value of the effective address will be (rZ bits 10-24) if no index bit is present in the OP register or (rZ bits 10-24 + specified index register) if an index bit is present. The output of the adder is normally the effective address because ZEN, which enables the rZ input to the adder, is a logical ONE except for a certain few operations that require the removal of ZEN for some special adder manipulation. These special cases appear in the timing sequences that accompany the logical block diagrams. The end-around carry is inhibited during effective addressing.

For operations requiring a memory access, the effective address is gated to the memory address register (MAR) by SEN and SA2 at T12 time. SEN gates the adder output to the AU bus while SA2 simultaneously gates the AU bus to the address register of the selected memory module.

During a read access, an RR signal is generated at T12 time to initiate a read cycle from the memory cores specified by MAR, into the memory information register (MIR). During T23 time and after a memory word has been read from the address specified by MAR into MIR, a signal MTT transfers the contents of MIR into the transfer bus, which will then be enabled to the appropriate destination.

During a write access, a CW signal is generated at T12 time to initiate a write cycle from MIR to the memory cores specified by MAR. During T23 time a signal will gate a register to the transfer bus which has its outputs enabled to the MIR.

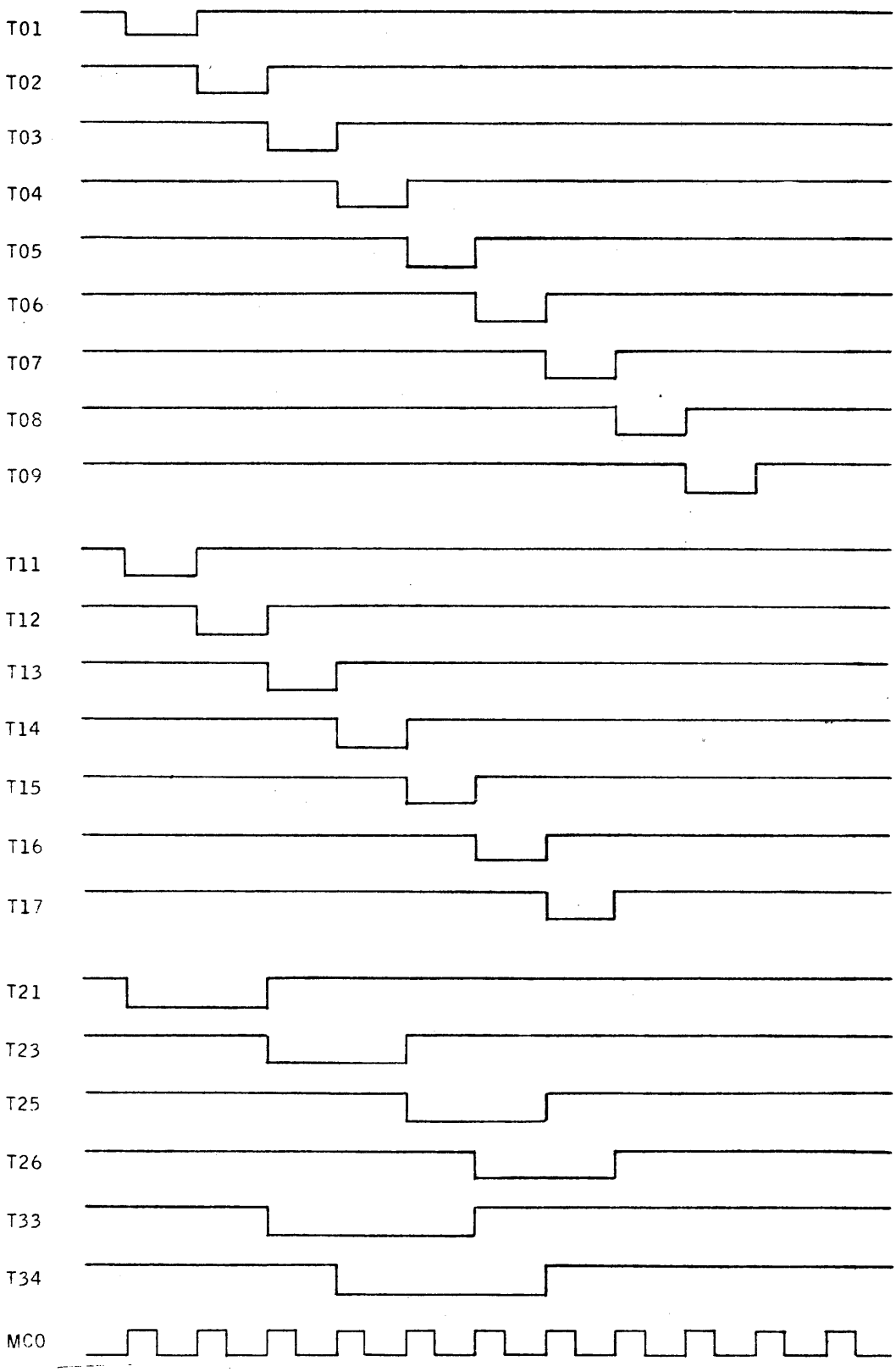


Figure 4-5. Operate Clock, Timing Chart

4-3.2 Command Executions

HALT (HLT) OPN00

The execution of a halt command must set halt flip-flop C1 and must not enable the start of the next fetch cycle. The halt flip-flop is set by the leading edge of T11 (Figure 4-6) during the execution of an HLT command. This will prevent the computer from entering another normal fetch cycle until the start switch is depressed.

EXECUTE (XEC) OPN02

The execution of this command does not involve an entry into the operate domain of the machine cycle; instead, a special fetch cycle is performed. The XEC command timing diagram is shown in Figure 4-7.

STORE CONTENTS OF rB (STB) OPN03

The command requires a memory access during which the contents of the B register are stored in the memory word at the effective address.

During T12 time, SEN, SA2, and a write memory access (CW) are generated. (Figure 4-8.) During T23 time, BTT is generated. This signal gates the contents of the B register to the transfer bus which has its outputs enabled to the MIR. At T15 time, an enable next fetch pulse (ENF) is generated to initiate the next fetch cycle.

STORE THE OP CODE OF rA (STC) OPN04

This command requires a memory access during which the contents of A1-A9 replace the corresponding bits in the memory word at the effective address.

The operate cycle is entered (Figure 4-9) and during T12 time, SEN, SA2, and a write memory access (CW) are generated. During T23 time, OP and ATT signals are generated. OP allows partial substitution of the OP code into a memory word; ATT gates

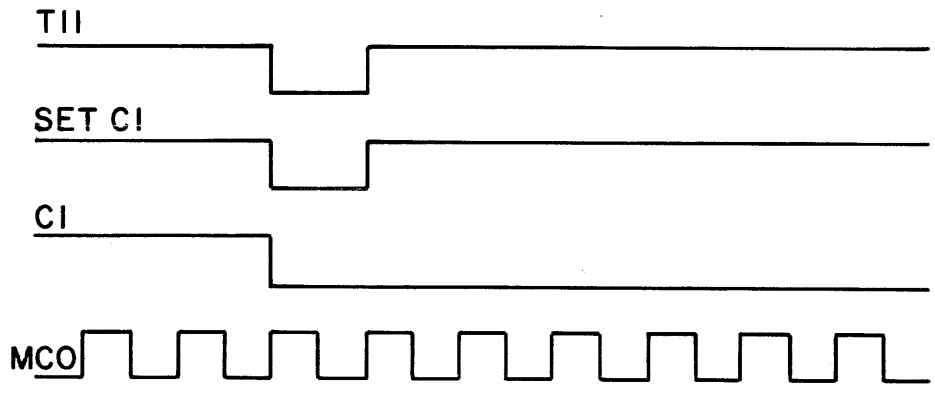
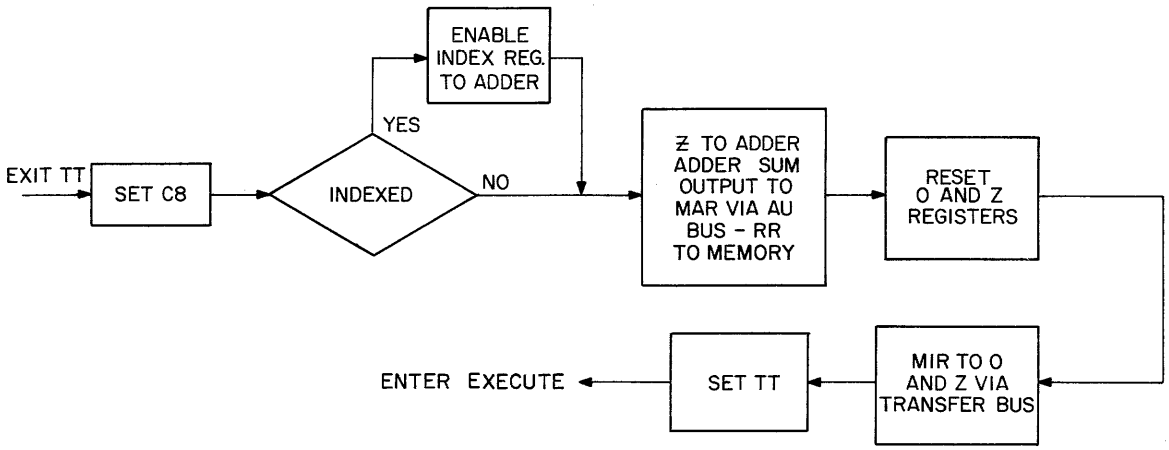


Figure 4-6. OPN 00 Halt, Flow Chart and Timing Diagram



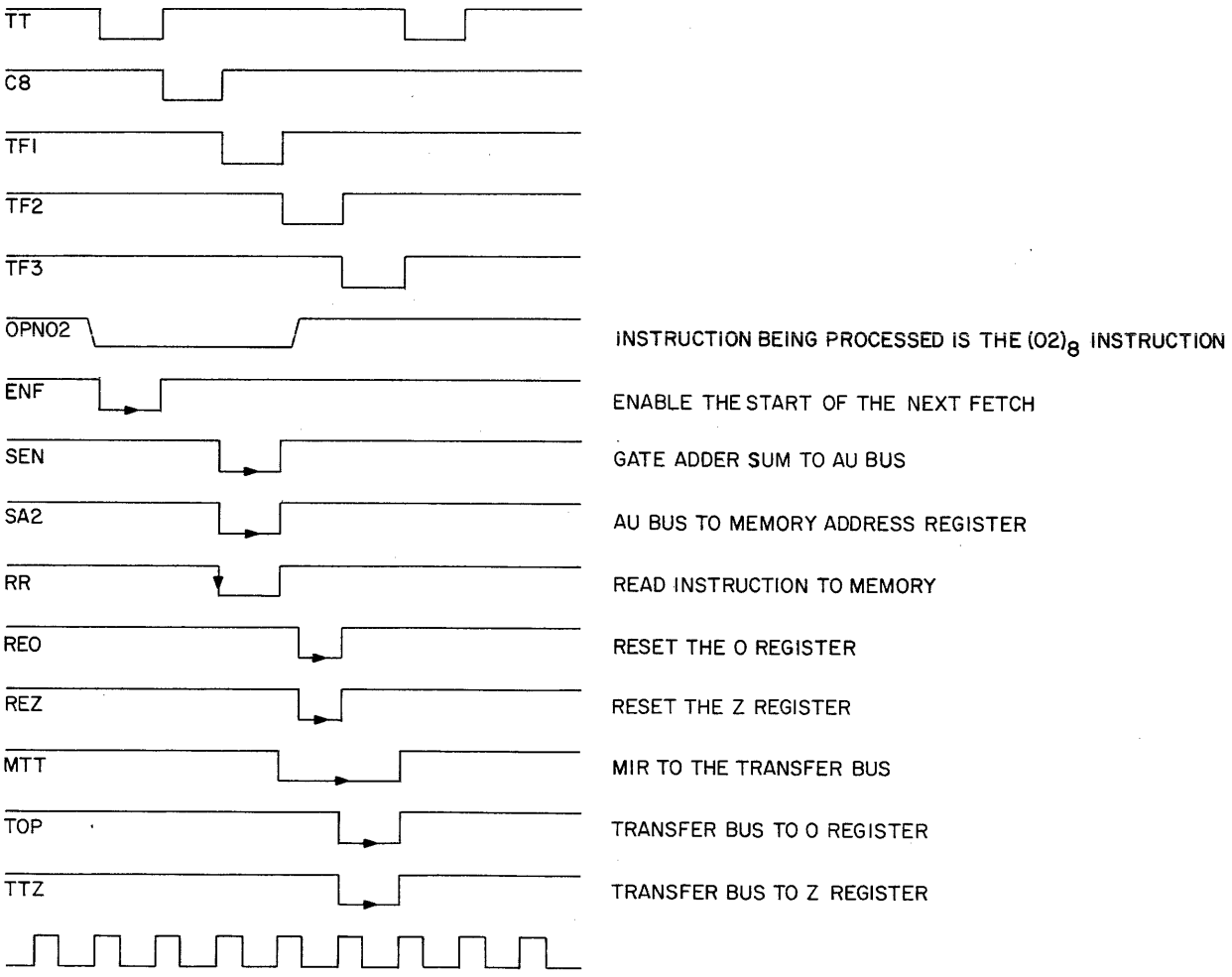
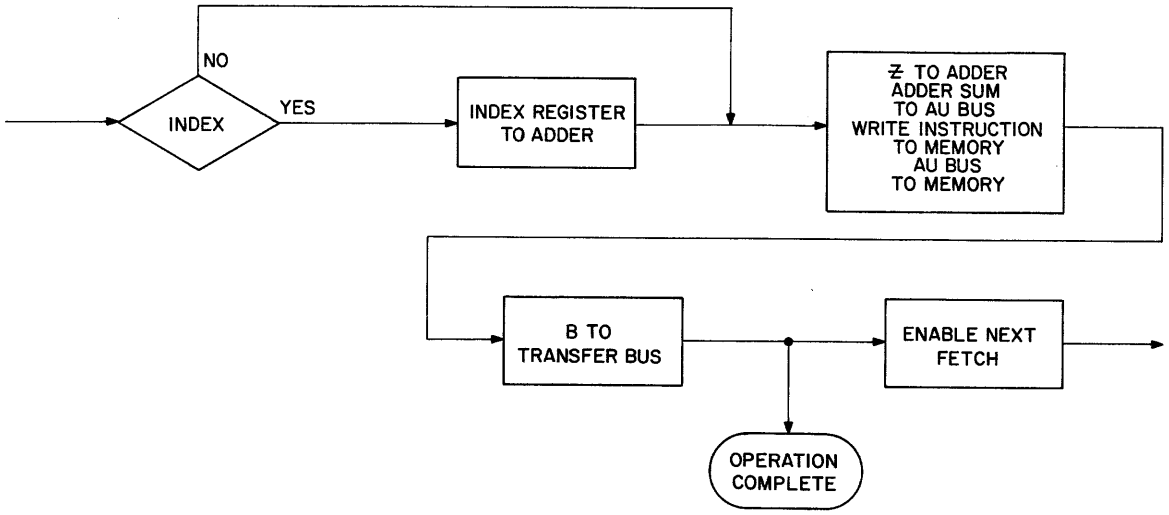


Figure 4-7. OPN 02 Execute, Flow Chart and Timing Diagram



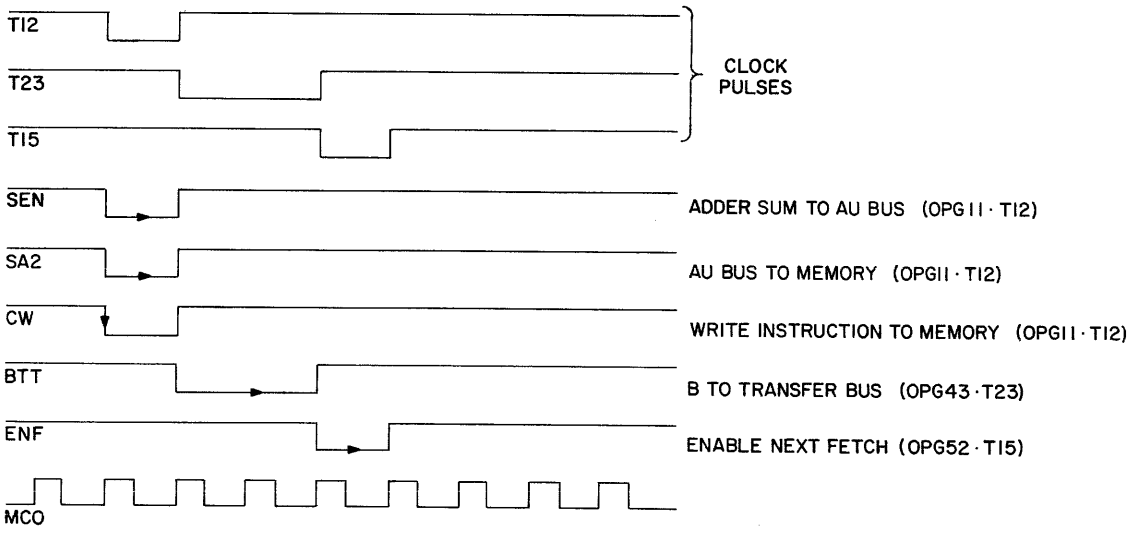


Figure 4-8. OPN 03 Store Contents of B, Flow Chart and Timing Diagram

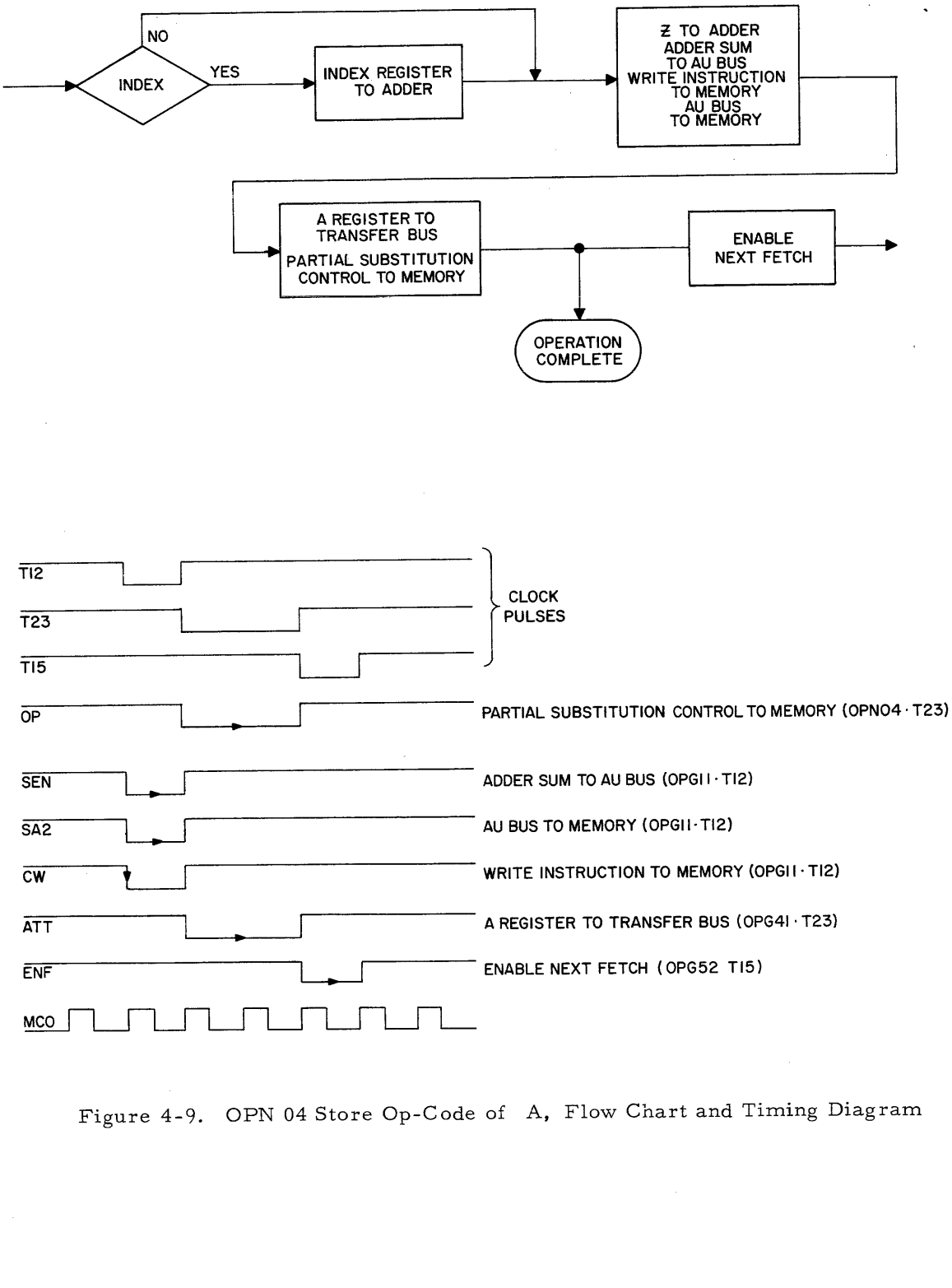


Figure 4-9. OPN 04 Store Op-Code of A, Flow Chart and Timing Diagram

the contents of the A register into the transfer bus, which has its outputs enabled to the MIR. At T15 time, an enable next fetch pulse (ENF) initiates the next fetch cycle. Bits 10-24 of the memory word at the effective address are unchanged.

STORE CONTENTS OF A (STA) OPN05

This command requires a memory access during which the contents of rA are stored in the memory word at the effective address.

During T12 time, SEN, SA2, and a write memory access (CW) are generated (Figure 4-10). During T23 time, an ATT signal is generated to gate the contents of the A register into the transfer bus which has its outputs enabled to the MIR. At T15 time, an enable next fetch pulse (ENF) initiates the next fetch cycle.

STORE ADDRESS OF A (STD) OPN06

The command requires a memory access during which the contents of A10-A24 replace the corresponding bits in the memory word at the effective address.

The operate cycle is entered (Figure 4-11) and during T12 time, SEN, SA2, and a write memory access (CW) are generated. During T23 time, AD and ATT signals are generated. AD allows partial substitution of the address field into a memory word and gates the contents of the A register into the transfer bus which has its outputs enabled to the MIR.

At T15 time, an enable next fetch pulse (ENF) initiates the next fetch cycle. Bits 1-9 of the memory word at the effective address are unchanged.

STORE INPUT IN MEMORY (INM) OPN07

INM is performed by executing one transfer from the input bus to the transfer bus and initiating a memory access that stores the input data in the memory cell specified by the effective address.

The transition from TT time to T11 time of the operate clock (Figure 4-12) is a function of input-output ready flip-flop C4. C4 is a synchronizing flip-flop set at the beginning of a clock cycle but after occurrence of the asynchronous input-output ready pulse (IOR). In this case, IOR indicates that the input channel is ready to transfer data to the computer. T12 time starts 1 μsec after C4 is set.

During T12 time, SEN, SA2, and a write memory access (CW) are generated. During T23 time, an ITT signal is generated to enable the input bus to the transfer bus, which has its outputs enabled to the MIR. During T14 time, an RRS signal is generated. The leading edge of this pulse resets IOR; 1 μsec later C4 is reset. At T15 time, an enable next fetch pulse (ENF) initiates the next fetch cycle.

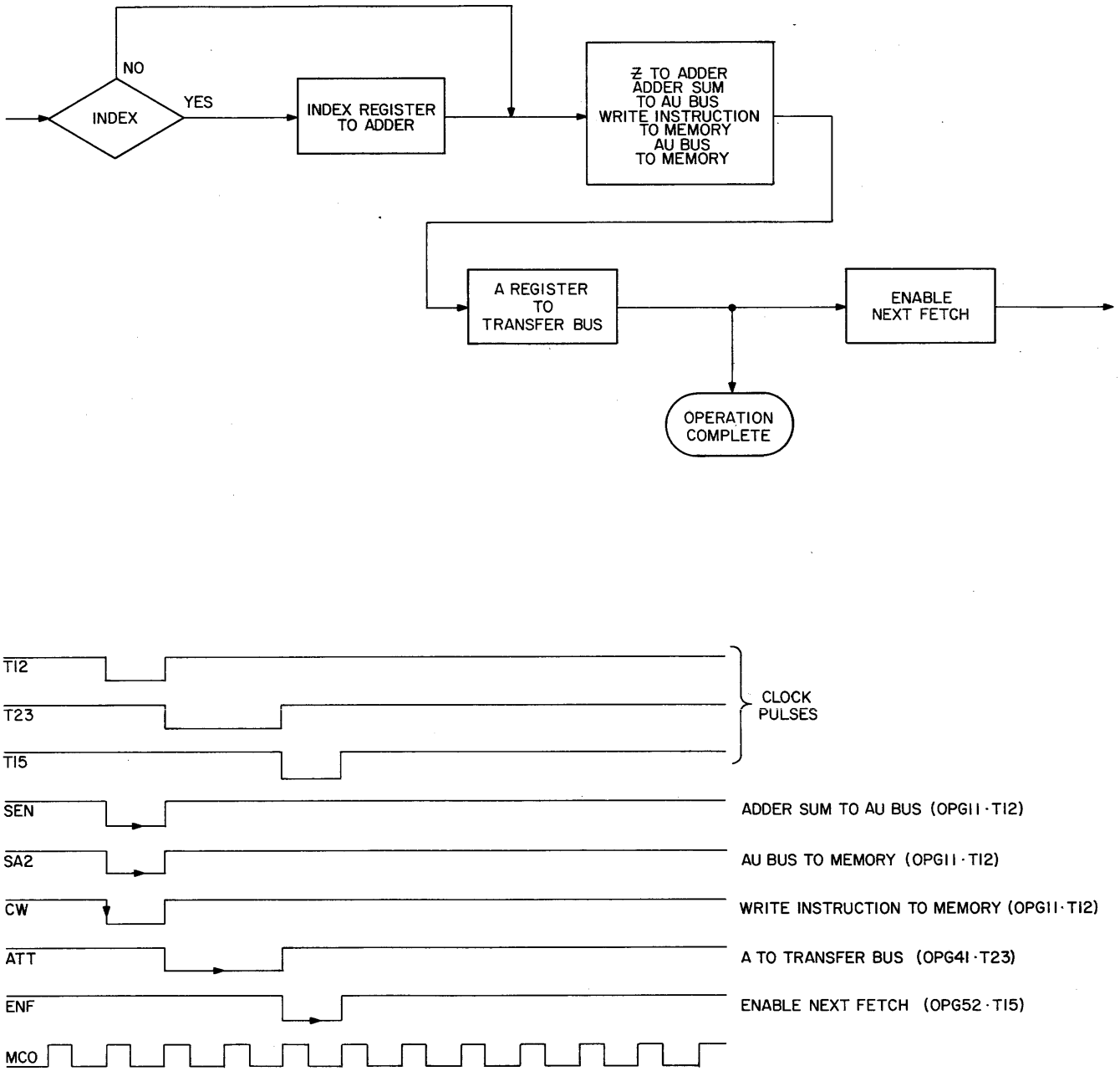


Figure 4-10. OPN 05 Store Contents of A, Flow Chart and Timing Diagram

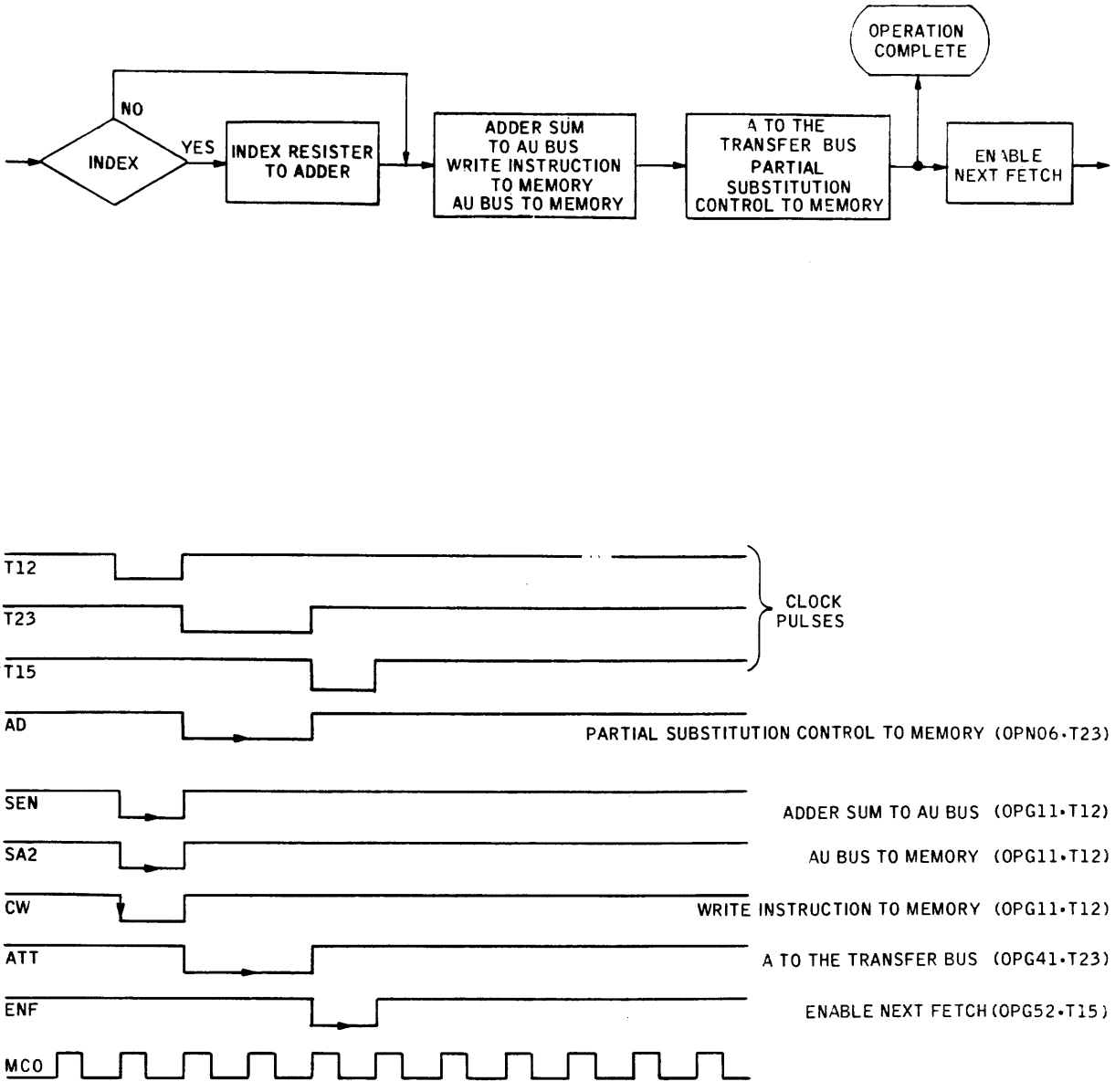


Figure 4-11. OPN 06 Store Address of A, Flow Chart and Timing Diagram

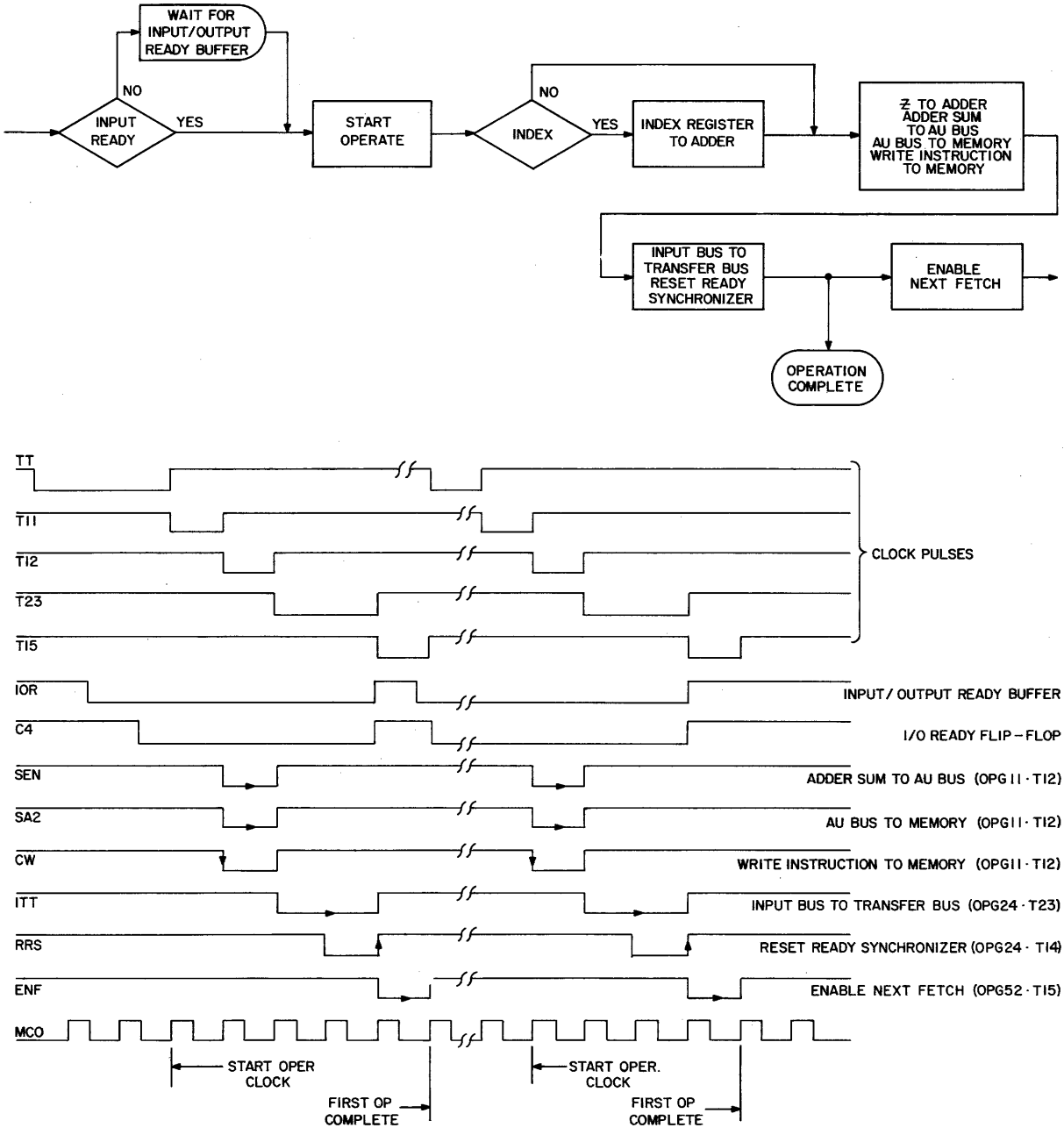


Figure 4-12. OPN 07 Store Input in Memory, Flow Chart and Timing Diagram

ADD MEMORY TO A (ADD) OPN10

In executing this command, the contents of the memory word at the effective address are algebraically added to the contents of rA, and the resulting sum replaces the contents of rA (Figure 4-13).

The algebraic addition occurring during this instruction consists of two parts, addition and correction. The addition is performed using ONE's complement arithmetic in which one of the two operands must be presented to the adder in complement form. In the DDP-24, this is accomplished by gating the complement side of the A register to the augend input of the adder.

The correction portion of an ADD is a function of A and Z sign comparison and a carry-out of the most significant magnitude column of the adder. Correction functions are sometimes generated at the same time as the addition. The possible corrections are overflow detection and sign change (which are simultaneous with the addition) and magnitude complementing (which is accomplished during the subsequent clock period).

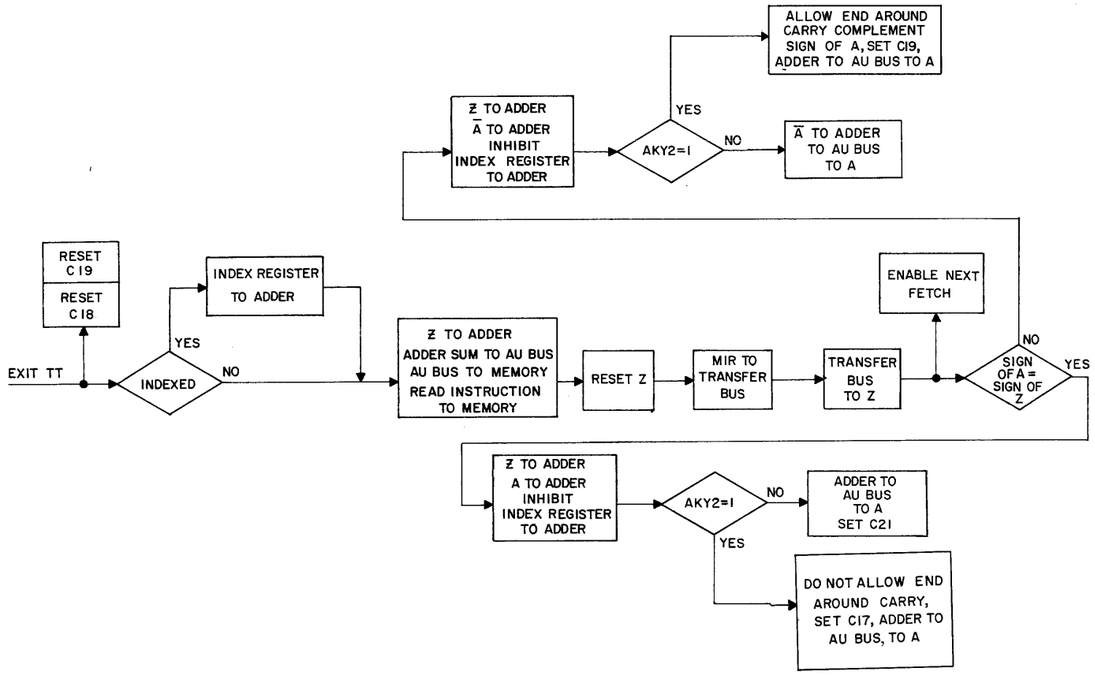
Each ADD instruction sets up certain control flip-flops for use if the ADD is an entry into a multiple precision program. These circuits, C18 and C19, are the ADD/SUB and the complement sign of the rA storage flip-flops. C18 is set by the trailing edge of TT. While C18 is set, any SMP command is treated as an add. C19 is initially reset at time T11 and will be set during the ADD if and when the sign of rA is complemented.

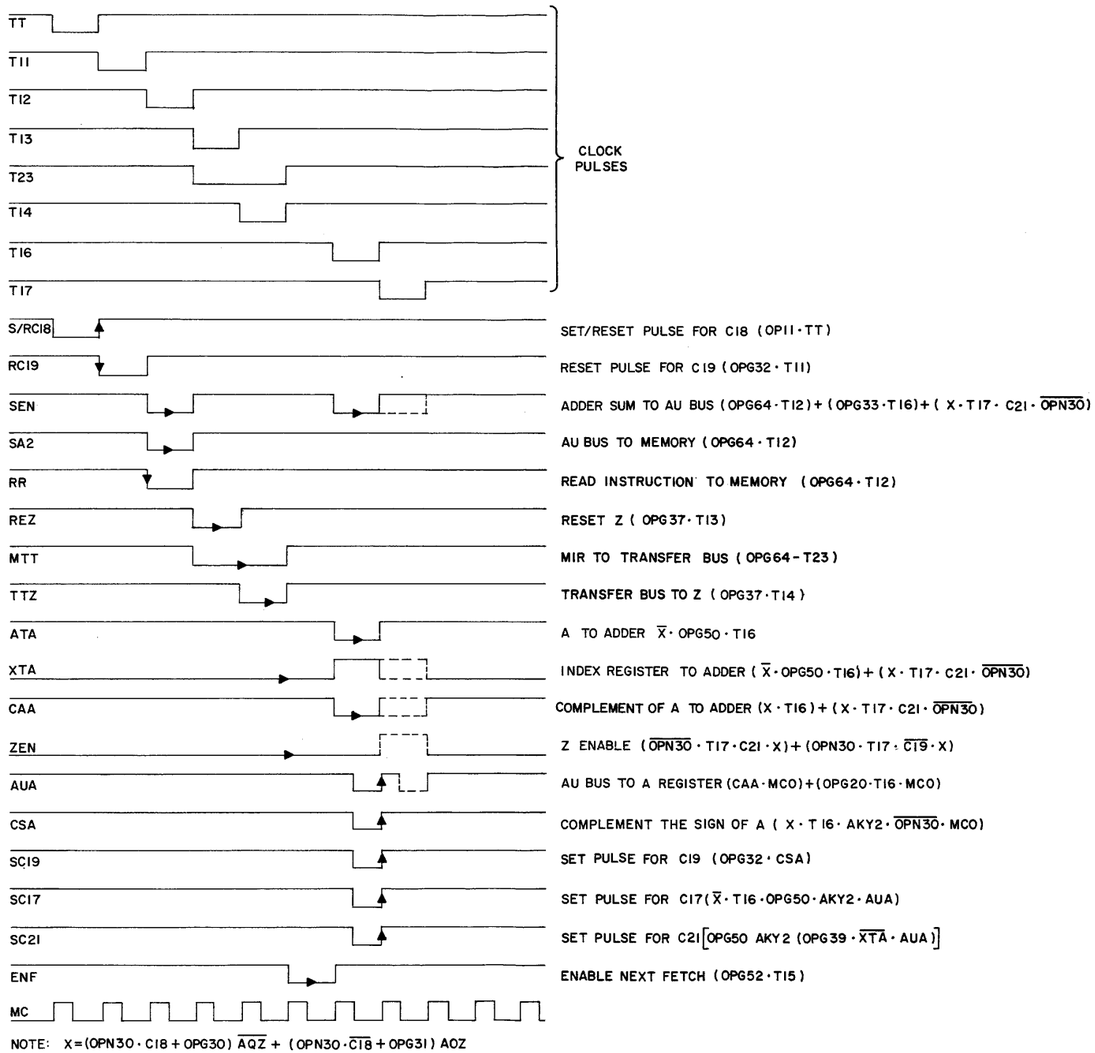
At T12 time, SEN, SA2, and RR are generated for the operand access. After rZ is loaded with the operand, the signs of rA and rZ are compared. If the signs are like, the set sides of the A register and the Z register are gated to the adder to form the sum (rA + rZ). For this case of like signs, a carry-out of column two represents an overflow and causes C17 to be set when the AUA transfers the adder sum output into rA, but this high-order carry, AKY2, is not allowed to propagate an end-around.

If rA and rZ signs are unlike, the reset or complement side of rA and the set side of rZ are gated to the adder to form the sum (-rA + rZ). If AKY2 is generated, it is allowed to propagate an end-around. The presence of AYK2 during the addition causes A1 to be complemented and C19 to be set.

If no AKY2 is formed during the unlike signs add, flip-flop C21 is set to store this fact. After the sum has been transferred back into rA, C21 is interrogated to see if the number in rZ is a complement number. If C21 is set (i.e., AKY2 = 0 during add) the complement side of rA is gated to the adder while the rA input (ZEN) is inhibited. The resulting sum is transferred into rA.

The signals that cause the sum to be formed are ATA or CAA. They select the set or reset side of rA as an augend to the adder while simultaneously removing the index inputs to the adder. This signal, SEN, gates the resulting sum output of the adder to the AU bus. Finally, AUA gates the AU bus into the A register. All of these signals are generated during T16 time. Each is a full 1-μsec pulse, except AUA which is 0.6 μsec





NOTE: X=(OPN30·C18+OPG30) $\overline{AQZ}$ + (OPN30·$\overline{C18}$+OPG31) AOZ

Figure 4-13. OPN 10 Add Memory to A, Flow Chart and Timing Diagram

during the last 0.6 μsec of T16. During AUA time, the carry AKY2 is interrogated for C17, C19, and C21.

During T17 time, C21 is used to make the complement rA decision. If rA is to be complemented, CAA and AUA will be generated. During this time rZ and rX are inhibited as adder inputs. The sum output of the adder is the complement of the A register and is transferred into rA.

At T15 time, an enable next fetch pulse (ENF) is generated to initiate the next fetch cycle.

SUBTRACT MEMORY FROM A (SUB) OPN11

In executing this command the contents of the memory word at the effective address are algebraically subtracted from the contents of rA, and the resulting difference replaces the contents of rA (Figure 4-14).

The algebraic subtraction which takes place during this instruction consists of two parts – addition and correction. The addition is performed using ONE's-complement arithmetic in which one of the two operands must be presented to the adder in complement form. In the DDP-24 this is accomplished by gating the complement side of the A register to the augend input of the adder.

The correction portion of a SUB is a function of rA and rZ sign comparison and carry-out of the most significant magnitude column of the adder. Correction functions are sometimes generated at the same time as the addition. The possible corrections are overflow detection and sign change, (which are simultaneous with the addition) and magnitude complementing (which is accomplished during the subsequent clock period).

Each SUB instruction sets up certain control flip-flops for use if the SUB is an entry into a multiple precision program. These circuits are C18, the ADD/SUB and C19, the complement sign of rA storage flip-flops. C18 is reset by the trailing edge of TT. While it is reset, any SMP command is treated as a subtract. C19 is initially reset at time T11 and will be set during the SUB if and when the sign of rA is complemented.

At T12 time SEN, SA2, and RR are generated for the operand access. After rZ is loaded with the operand, the signs of rA and rZ are compared. If the signs are unlike the set sides of the A register and the Z register are gated to the adder to form the sum (rA + rZ). For this case of unlike signs, a carry-out of column two represents an overflow and causes C17 to be set when AUA transfers the adder sum output into A, but this high-order carry, AKY2, is not allowed to propagate an end-around.

If rA and rZ signs are like, the reset or complement side of rA and the set side of rZ are gated to the adder to form the sum (-rA + rZ). If AKY2 is generated, it is allowed to propagate an end-around. The presence of AKY2 during the addition causes A1 to be complemented and C19 to be set.

If no AKY2 is formed during the like signs subtract, flip-flop C21 is set to store this fact. After the sum has been transferred back into rA, C21 is interrogated to see if the number in rA is a complement number. If C21 is set (i.e., AKY2 = 0 during add), the complement side of rA is gated to the adder while the rZ input (ZEN) is inhibited. The resulting sum is transferred into rA.

The signals that cause the sum to be formed are ATA or CAA. They select the set or reset side of rA as an augend to the adder while simultaneously removing the index inputs to the adder. The signal, SEN, gates the resulting sum output of the adder to the AU bus. Finally, AUA gates the AU bus to the A register. All of these signals are generated during T16 time. Each is a full 1-μsec pulse, except AUA which is 0.6 μsec during the last 0.6 μsec of T16. During AUA time, the carry AKY2 is interrogated for C17, C19 and C21.

During T17 time, C21 is used to make the complement rA decision. If rA is to be complemented, CAA and AUA will be generated. During this time rZ and rX are inhibited as adder inputs. The sum output of the adder is the complement of the A register and is transferred into rA.

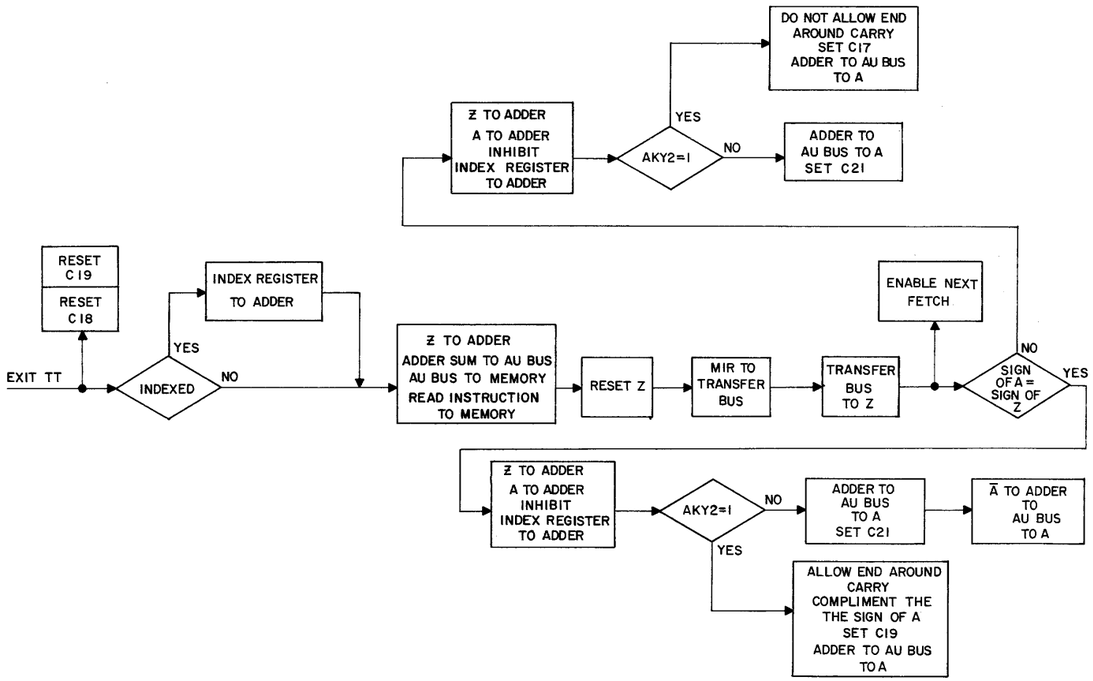
At T15 time, an enable next fetch pulse (ENF) is generated to initiate the next fetch cycle.

SKIP IF A GREATER THAN MEMORY (SKG) OPN12

The execution of this instruction places the memory word access in the Z-register. The sign bits of the A and Z register are then examined. Of the four possible sign-bit configurations for rA and rZ, only three produce a skip condition. They are $rA_1=rZ_1=0$, $rA_1=rZ_1=1$, and $rA_1=0$ when $rZ_1=1$ (Figure 4-15).

The three sign configurations investigated are: rA plus-rZ plus; rA minus-rZ minus; and rA plus-rZ minus. The rA plus-rZ minus case is of least concern. However, because a minus zero can exist, it creates a special case-rA zero and rZ zero-in which rA is plus zero and rZ is minus zero. Plus zero is not considered greater than minus zero; therefore the instruction should not result in a skip for this configuration. When the rA plus-rZ minus case is interrogated, the rA zero gate (C25) determines whether the plus zero-minus zero configuration exists. If the output of the A zero gate (C25) is not true, the decision is complete and the skip may be performed. However, if C25 is true, rA plus-rZ minus exists with rA being zero. Then, the end-carry must be investigated to determine if rZ is zero. The two remaining cases, like signs with both being positive or both being negative, are functions of end-carry.

At T12 time, SEN, SA2, and RR are generated for the operand access. At T15 time, when CAA gates the complement side of rA to the adder, XTA is blocked by T25. Thus the sum output of the adder is -rA + rZ. Simultaneously with the selection of the complement side of rA to the adder, an end-carry is inserted into the low-order column if the rA plus-rZ plus case is under investigation. With these inputs gated to the adder, the



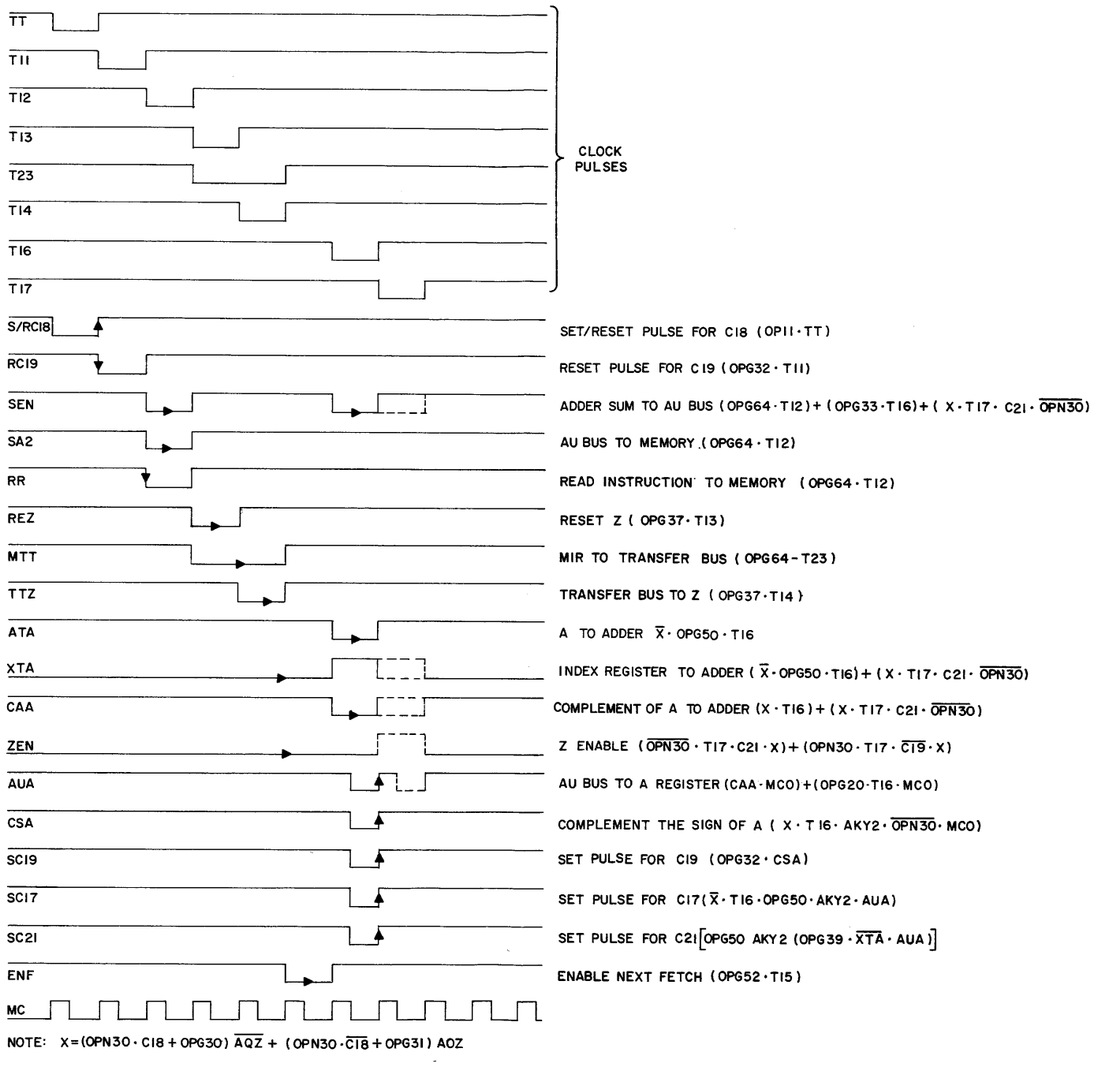


Figure 4-14. OPN 11 Subtract Memory from A, Flow Chart and Timing Diagram

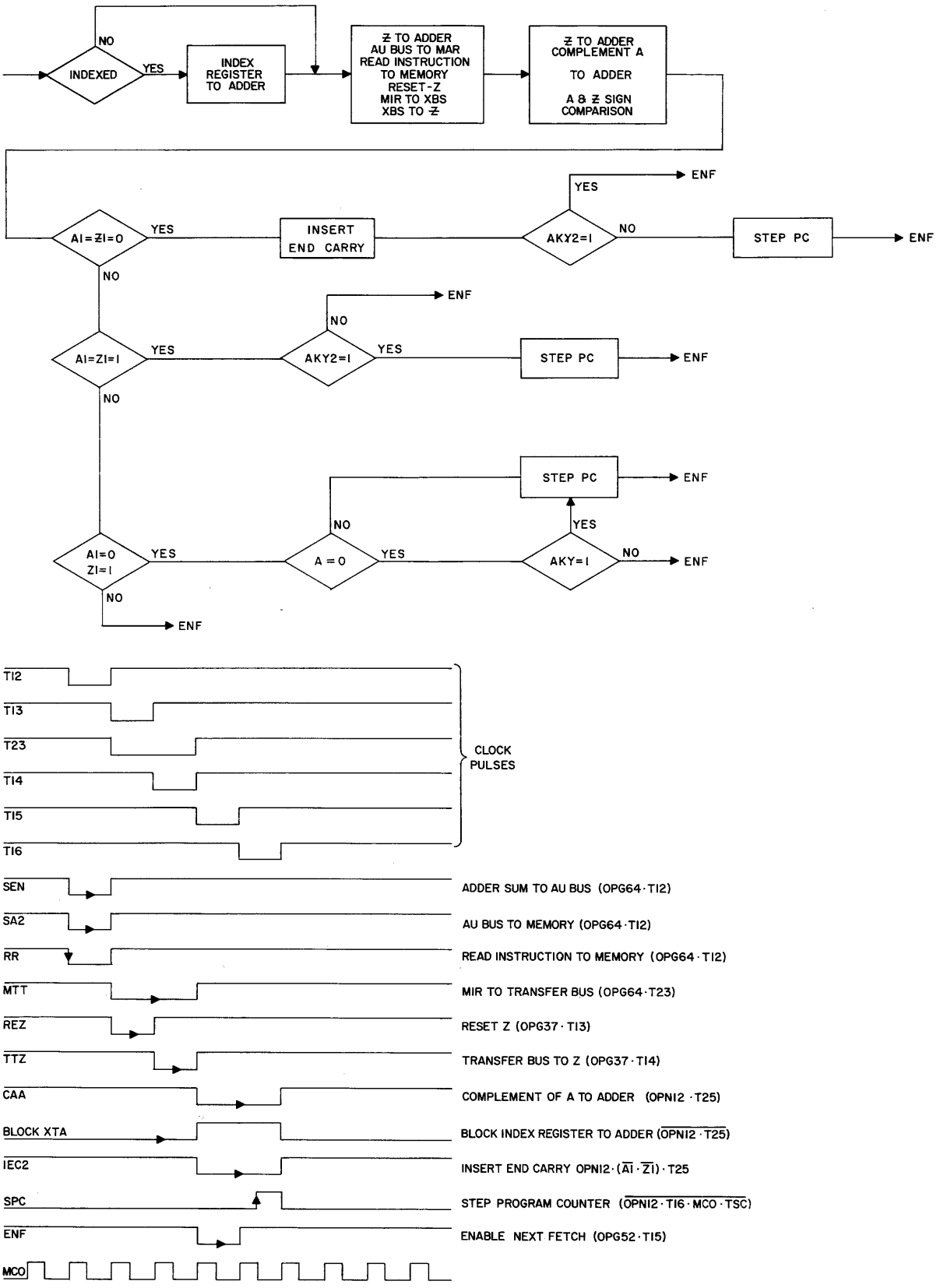


Figure 4-15. OPN 12 Skip If A Greater Than Memory, Flow Chart and Timing Diagram

carry-out of the high-order column is monitored. If a carry exists, the magnitude of rA was less than the magnitude of rZ and a skip pulse should not be furnished to the program counter. If no carry is present on the output of the adder, then the magnitude of rA was greater than the magnitude of rZ and the skip pulse should be supplied to the program counter. The carry is inserted into the lower column of the adder configuration of rA plus-rZ plus to eliminate the possibility of the equal's case.

If the case under investigation is that of like signs, both being negative, the complement side of rA is gated to the adder and the index input is removed, thus furnishing an output of -rA + rZ. No end carry is inserted in the lower column and the carry out of the higher column is investigated. In this case, a carry-out of the higher column represents a skip condition.

For the case of rA plus-rZ minus, the adder is set up in the same manner as the previous case of rA minus-rZ minus. Note that rA plus-rZ minus is a special case if A = 0. If, during this case, the output of the rA zero gate (C25) is false, stating that A does not equal zero, the decision is already made and the skip should be performed. If the output of the A zero gate (C26) is ture and A = zero, then the skip decision must be based on the existence of a carry-out of the high-order column of the adder. If a carry exists during the addition, a step pulse must be supplied to the program counter.

Note

At no time during the execution of this instruction was an AUA pulse generated which would drop the sum output of the adder into the A register. This instruction leaves the A register unmodified.

The final function to be performed in executing the OPN12 command, enabling the next fetch, is performed during T15 time while the skip investigation is being made. The timing sequence of this instruction shows a signal having the mnemonic SPC as the step input to the program counter. This is a leading-edge input. Furthermore, the program counter is implemented in the form of two individual 6-stage ripple counters. The inputs to the two counters are simultaneous because the skip instruction advances the program counter simultaneously with the enabling of the next fetch cycle. If the simultaneous count were not used in the program counter, the count would ripple through the program counter at the same time the fetch address was being selected.

SKIP IF A NOT EQUAL TO MEMORY (SKN) OPN13

During execution of the SKN instruction a memory access places the memory word in the Z register (Figure 4-16). Once rZ is loaded with a memory word, the adder is set up to generate an exclusive-OR function between rA and rZ. With the adder set up to generate the function A exclusive-OR Z, the skip decision is based on the adder output

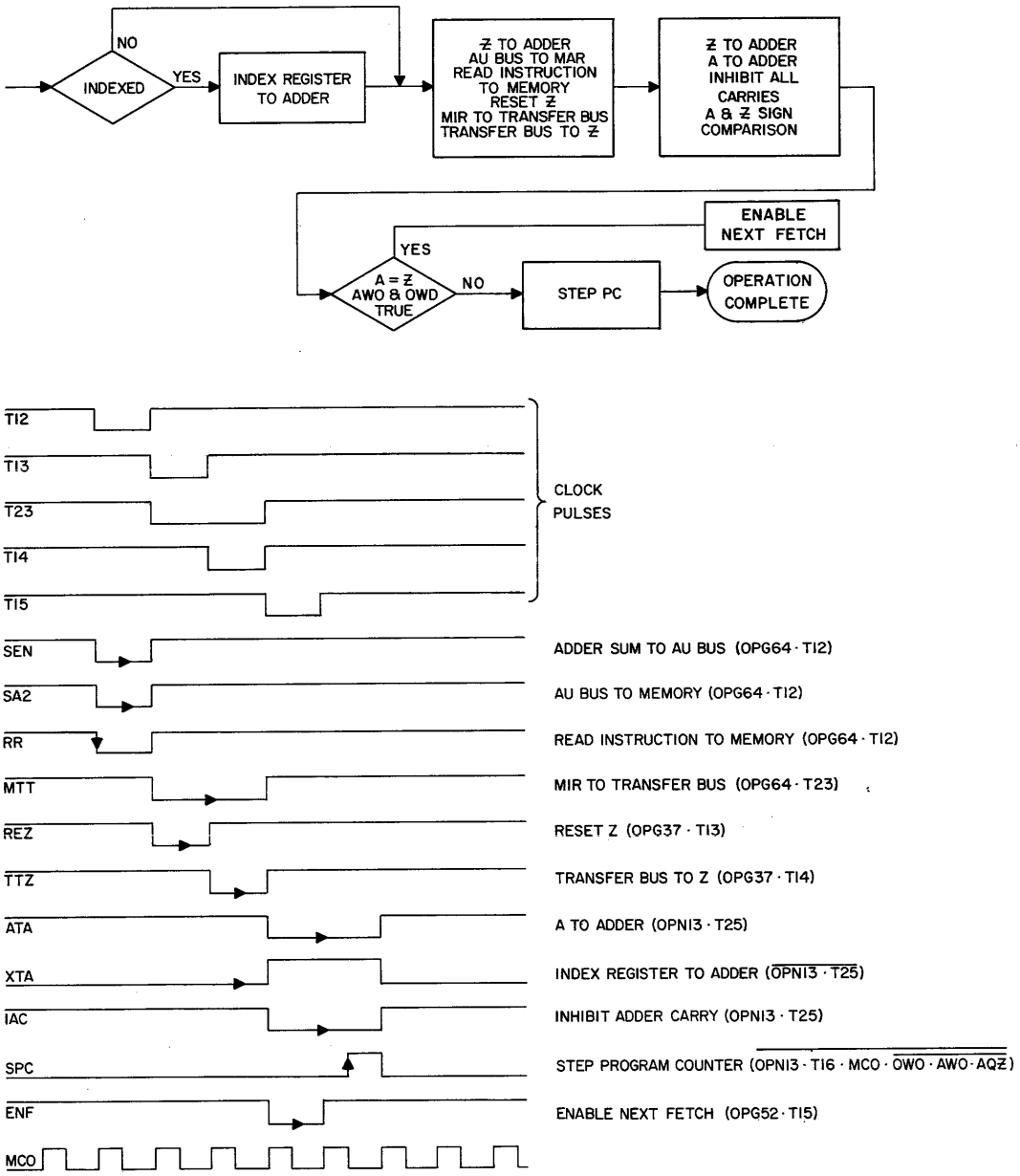


Figure 4-16. OPN 13 Skip If A Not Equal to Memory, Flow Chart and Timing Diagram

being equal to zero. In the case of unlike signs the adder output need not be gated because unlike signs are sufficient information upon which to base a skip decision.

The first function to be performed in the execution of the OPN13 instruction is that of a memory access to obtain a memory word and place it in the Z register. This memory access is the normal type previously described. At T15 time, ATA is generated to gate rA to the adder; IAC is generated to inhibit adder carry, and, at T25 time, XTA is inhibited. This adder configuration results in the sum output of the adder being an exclusive-OR of A and Z because IAC is generated. Bits 2 through 24 of the adder are gated to sense a zero output of the adder. This gating generates the signals AWO and OWO, both of which are generated by AND gating. AWO is an AND gating of all columns in the address portion of the computer word. OWO is an AND gating of all columns in the OP code portion. Recalling that since the adder output is the exclusive-OR of A and Z, AWO and OWO being logical zero implies that there is at least one column which has a discrepancy between A and Z. One such bit discrepancy is sufficient to generate a skip. Besides the functions AWO and OWO, there is a third function that can determine whether a skip pulse should be supplied to the program counter. This third input is the sign column information and a skip would be supplied if the signs of A and Z are unlike. Note that in the performance of this instruction, plus zero and minus zero are not considered equal.

In summary, there are three inputs to the test-for-skip position of the OPN13 instruction – AWO, OWO, and AQZ. AWO is the address portion of the computer word, OWO is the op-code portion of the computer word, and AQZ is a sign column function. These three conditions are logically ORed in the performance of the OPN13 instruction so that a skip will be processed if either AWO or OWO is not true or the signs are unlike. The remaining function to be performed during the OPN13 instruction is that of enabling the next fetch. This is accomplished by ENF at T15 time.

AND TO A (ANA) OPN15

This instruction forms the logical product of the contents of rA (bits 1-24) and the contents of the memory word at the effective address and replaces the contents of rA with the result (Figure 4-17).

If two sources are selected simultaneously as inputs to the transfer bus, the resulting state of each column is a logical AND of the corresponding inputs. During T12 time, a read memory access is initiated; during T13 time, an REZ pulse resets the Z register; and during T14 time, a TTZ pulse transfers the contents of the transfer bus into the Z register.

During T25 time, both the A register and the Z register are selected as inputs to the transfer bus by the pulses ZTT and ATT; during T16 time, the transfer bus is gated to the AU bus by TTA.

During the last 0.6 μsec of T16 time, an AUA pulse transfers the AU bus into the A register. During T15 time, an ENF pulse starts the next fetch cycle.

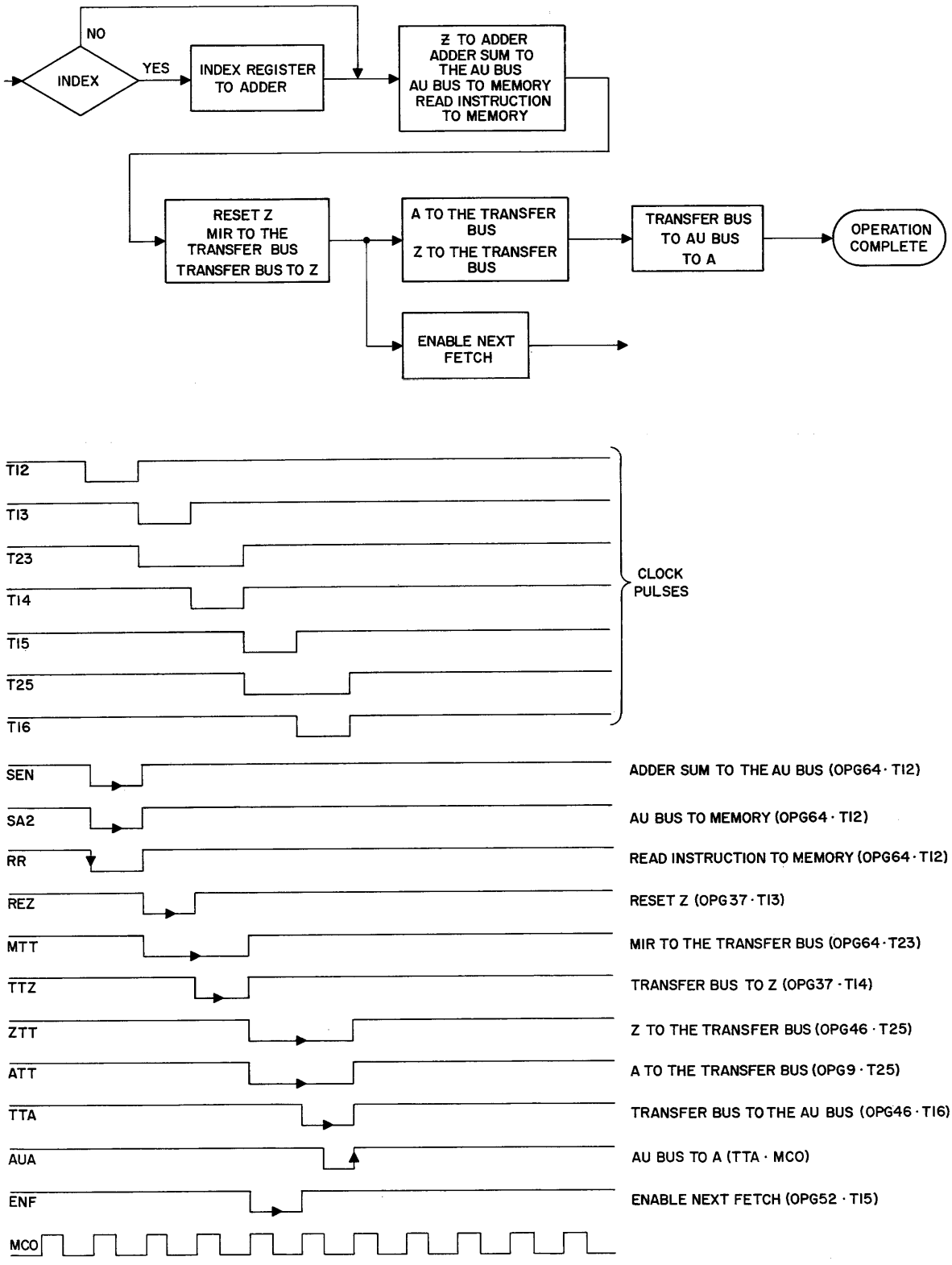


Figure 4-17. OPN 15 AND To A, Flow Chart and Timing Diagram

OR TO A (ORA) OPN16

This instruction forms the logical sum of the contents of the A register and the contents of the memory word at the effective address. The generation of the logical OR is accomplished by logically summing A· Z with A ⊕ Z (Figure 4-18).

During T12 time, a read-memory-access is initiated; during T13 time, an REZ pulse is generated to reset the contents of the Z register; and during T14 time, a TTZ pulse gates the transfer bus into the Z register. During T25 time, both the A register and the Z register are selected as inputs to the transfer bus by the pulses ZTT and ATT, causing the transfer bus to equal to A· Z.

During T16 time, the ATA pulse gates the A register to the adder while inhibiting XTA to disable the index register inputs to the adder. IAC is generated and inhibits the carry between the adder columns. Thus, the sum output of the adder is A ⊕ Z. SEN and TTA (at T16 time) gate the sum output of the adder (A ⊕ Z) and the transfer bus (A· Z) respectively into the AU bus. The AU bus logically sums the two inputs.

During the last 0.6 μsec of T16 time, an AUA pulse gates the AU bus into the A register. An ENF pulse generated during T15 time starts the next fetch cycle.

Note

The use of Inhibit Adder Carry (IAC) in effect results in the "exclusive OR" (⊕) condition.

EXCLUSIVE OR TO A (ERA) OPN17

This instruction forms the logical exclusive sum of the contents of rA and the memory word at the effective address and the contents of rA and replaced with the result (Figure 4-19).

During T12, time, a read memory access is initiated; during T13 time, an REZ pulse is generated to reset the contents of the Z register; and during T14 time, a TTZ pulse gates the transfer bus into rZ.

During T16 time, the ATA pulse gates the A register to the adder and inhibit XTA, thus disabling the index register inputs to the adder. An IAC pulse inhibits the carry between the adder columns and the sum output of the adder is A ⊕ Z. SEN enables the half-adder sum of the A register to the Z register to be gated into the AU bus.

During the last 0.6 μsec of T16 time, an AUA pulse gates the contents of the AU bus into the A register. The ENF pulse generated during T15 time starts the next fetch cycle.

ADD MAGNITUDE OF MEMORY TO A (ADM) OPN20

In executing this command, the magnitude of the contents of the memory word at the effective address is algebraically added to the contents of A. The resulting sum

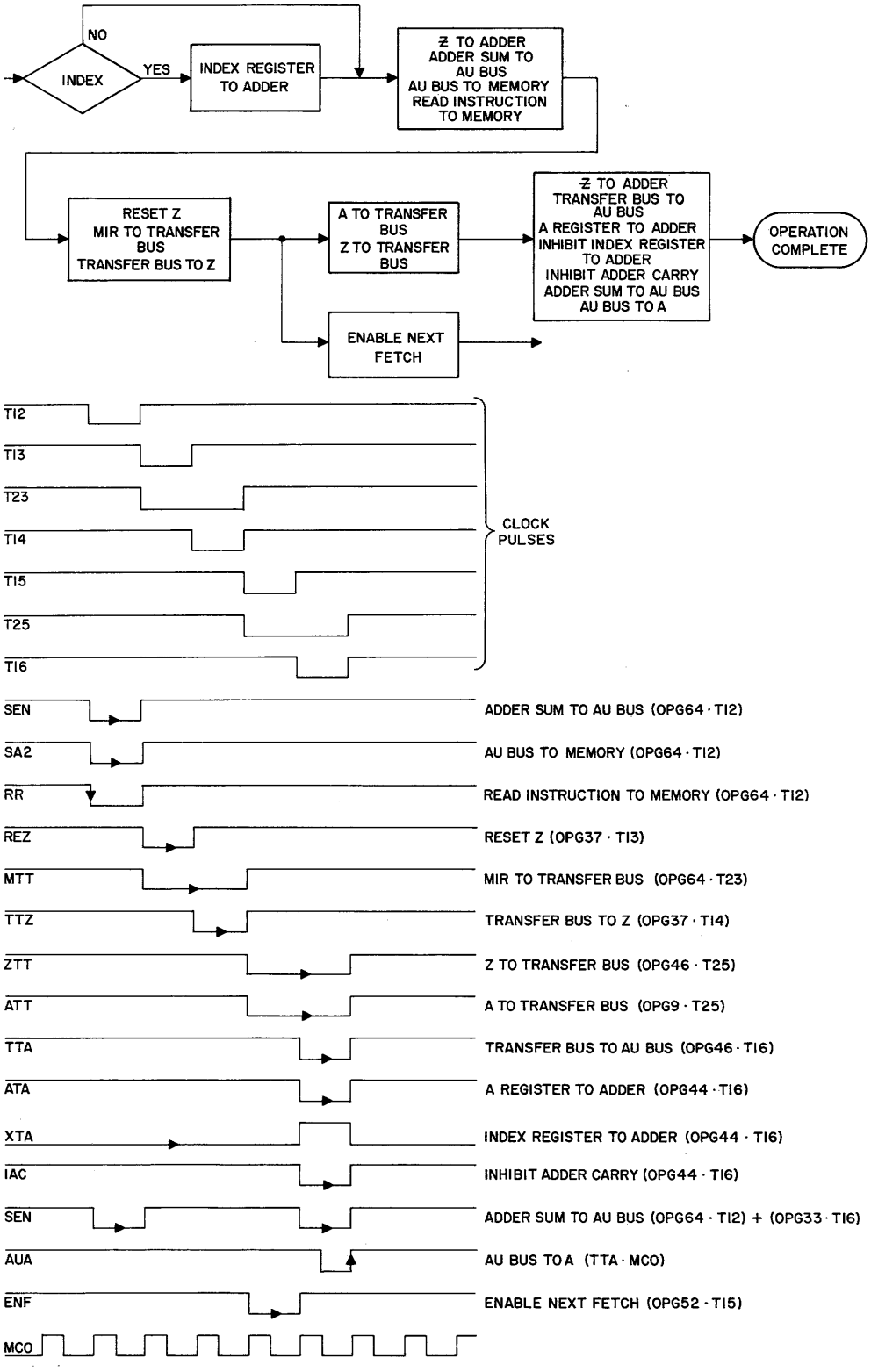


Figure 4-18. OPN 16 OR To A, Flow Chart and Timing Diagram

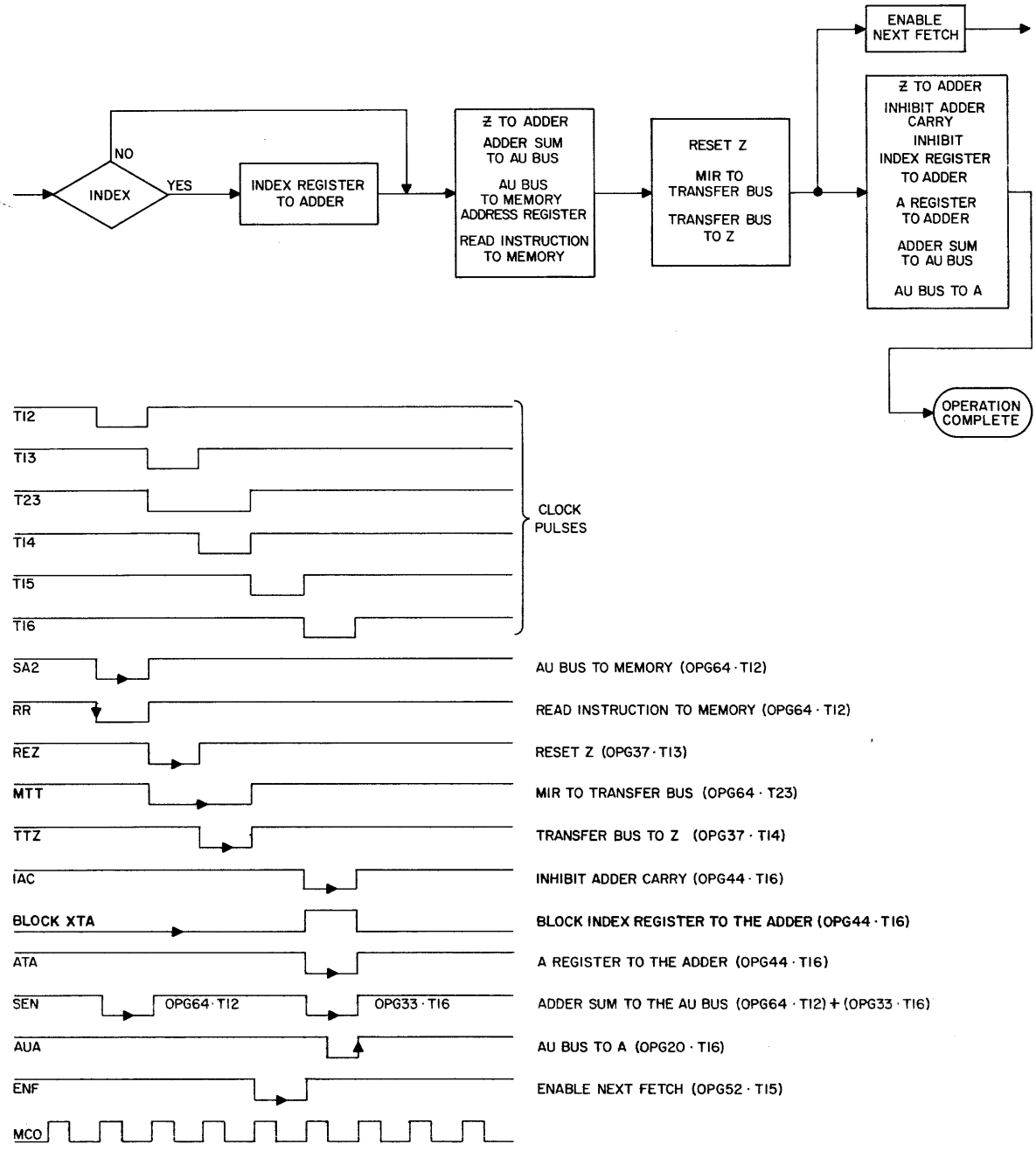


Figure 4-19. OPN 17 Exclusive OR to A, Flow Chart and Timing Diagram

replaces the contents of A. The execution of this instruction is identical to that of the ADD instruction except that when the contents of the effective address are brought into Z, the sign bit of Z is always made positive. This is done by the normal operand access reset of Z in conjunction with the deletion of a transfer bus to Z (TTZ) pulse as a function of operand access (Figure 4-20).

The algebraic addition taking place during this instruction consists of two parts – addition and correction. The addition can be performed using ONE's complement arithmetic. The correction portion of execution of an ADM is a function of A and Z sign comparison and a carry-out of the most significant magnitude column of the adder. In some cases, the correction functions are generated at the same time as the addition. The possible corrections are overflow detection, sign, change, and magnitude complementing. The first two are simultaneous with the addition while the last is accomplished during the following clock period.

At T12 time, SEN, SA2 and RR are generated for the operand access. After rZ is loaded with the operand, the signs of rA and rZ are compared. In this operand access, the sign of Z is always zero because column one of the transfer bus is not gated to Z1 for this instruction.

When the signs are like, the set sides of the A and Z registers are gated to the adder to form the sum (rA + rZ). For this case of like signs, a carry-out of column two represents an overflow and causes C17 to be set when AUA transfers the adder sum output into rA. This high-order carry AKY2 is not allowed to propagate end-around for this case of like signs. When rA and rZ signs are unlike, the reset or complement side of rA and the set side of rZ are gated to the adder to form the sum (-rA + rZ). If AKY2 is generated, it is allowed to propagate end-around. AKY2 present during the addition causes A1 to be complemented and C19 to be set.

If no AKY2 is formed during the unlike signs ADM, flip-flop C21 is set to store this fact. After the sum has been transferred back into rA, C21 is interrogated to see if the number in rA is a complement number. If C21 is set (i.e., AKY2 = 0 during add), the complement side of rA is gated to the adder while the rZ input (ZEN) is inhibited. The resulting sum is transferred into rA.

The signals causing the sum to be formed are ATA or CAA which select the set or reset side of A as an augend to the adder while simultaneously removing the index inputs to the adder. The signal, SEN, gates the resulting sum output of the adder into the AU bus. Finally AUA gates the AU bus into the A register. All these signals are generated during T16 and all are a full 1-μsec pulse except AUA which is a 0.6-μsec pulse during the last 0.6 μsec of T16. During AUA time, the carry AKY2 is interrogated for C17, C19 and C21.

During T17, time C21 makes the complement rA decision. If rA is to be complemented, CAA and AUA will be generated. During this time, rZ and rX are inhibited as

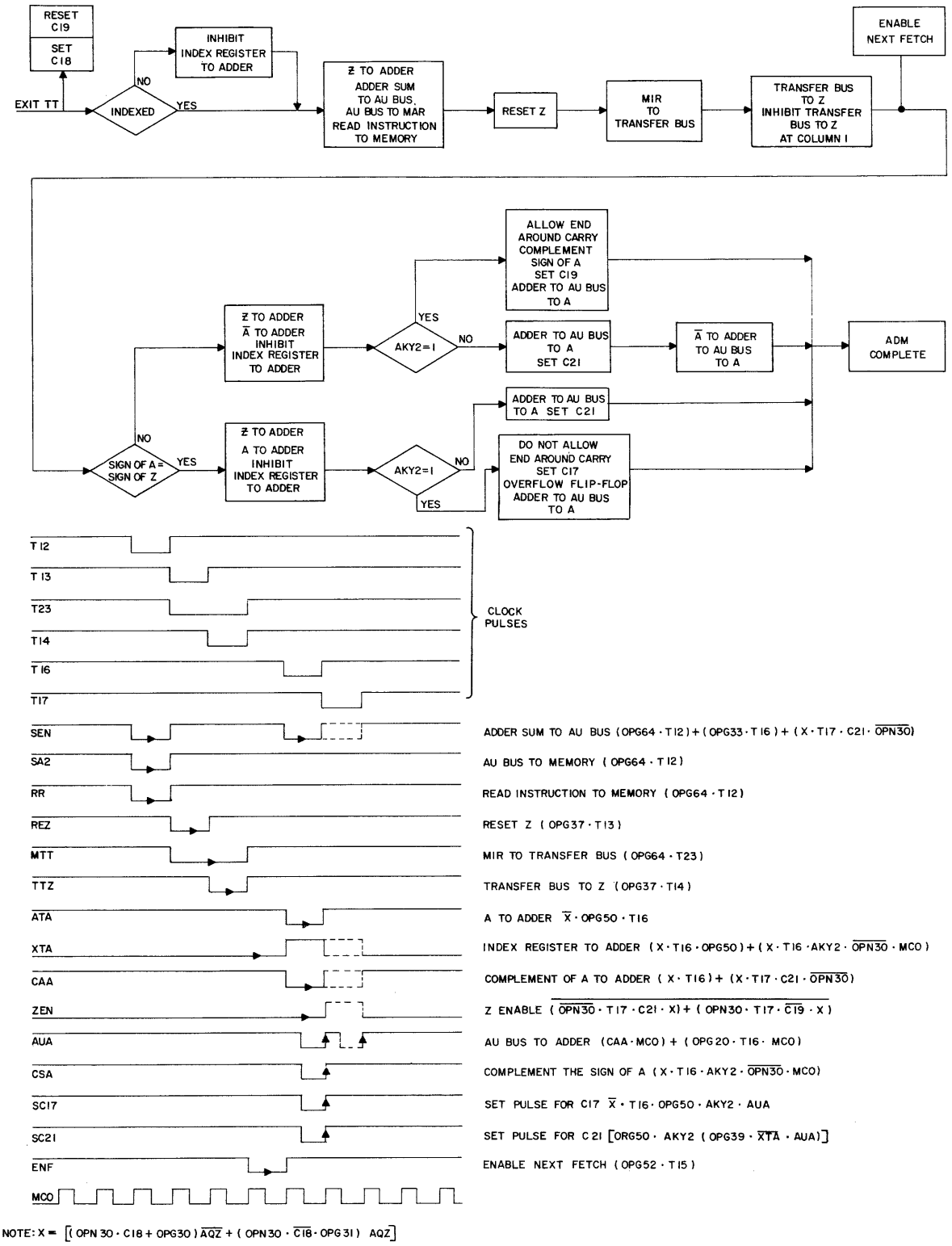


Figure 4-20. OPN 20 Add Magnitude of Memory to A, Flow Chart and Timing Diagram

adder inputs. The sum output of the adder will be the complement of the A register. AUA transfers this sum into rA.

At T15 time an enable next fetch pulse (ENF) is generated which will initiate the next fetch cycle.

SUBTRACT MAGNITUDE OF MEMORY FROM A (SBM) OPN21

In executing this command, the magnitude of the contents of the memory word at the effective address is algebraically subtracted from the contents of rA. The resulting difference replaces the contents of rA.

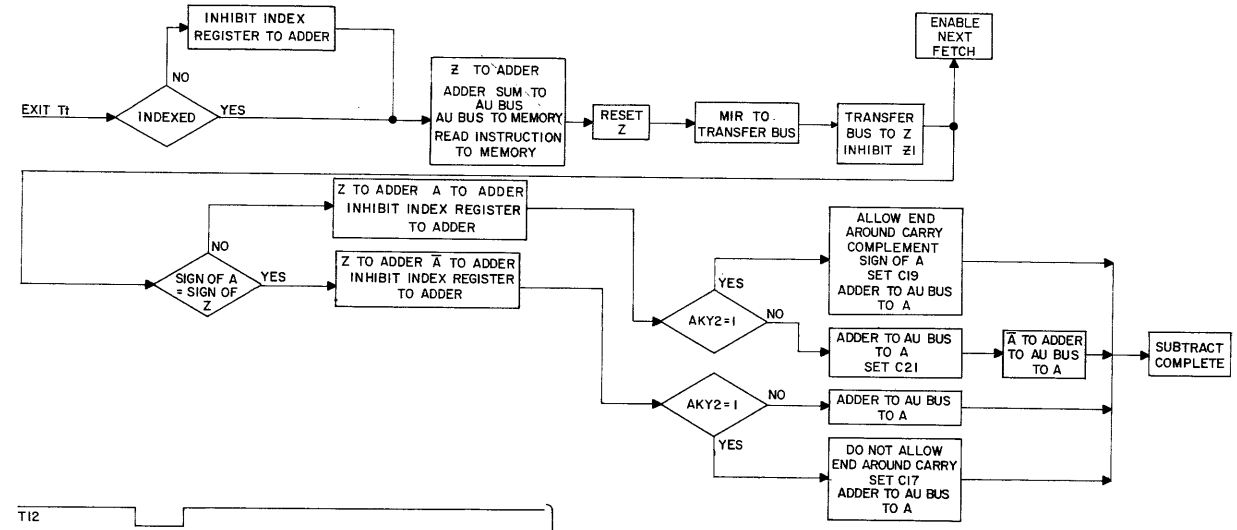
The execution of this instruction (Figure 4-21) is identical to that of the SUB instruction except that when the contents of the effective address are brought into Z, the sign bit of Z is always made positive. This is done by the normal operand access reset of Z in conjunction with the deletion of a transfer bus to Z pulse as a function of operand access.

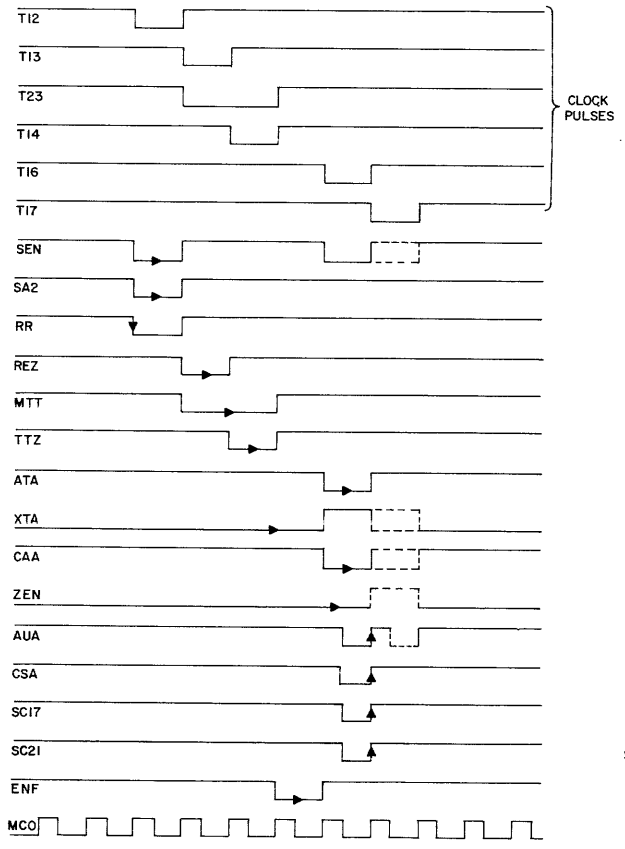
The algebraic subtraction taking place during this instruction consists of two parts — addition and correction. The addition itself is performed using ONE's complement arithmetic. The correction portion of execution of a SBM is a function of rA and rZ sign comparison and carry-out of the most significant magnitude column of the adder. In some cases, the correction functions are generated at the same time as the addition. The possible corrections are overflow detection, sign change, and magnitude complementing. The first two are simultaneous with the addition, while the last is accomplished during the following clock period.

At T12 time, SEN, SA2, and RR are generated for the operand access. After rZ is loaded with the operand, the signs of rA and rZ are compared. In this operand access, the sign of rZ is always zero since column 1 of the transfer bus is not gated into Z1 for this instruction. When the signs are unlike, the set sides of the A and Z resistors are gated to the adder to form the sum (rA + rZ). For this case of unlike signs, a carry out of column two, representing an overflow, causes C17 to be set when AUA transfers the adder sum output into rA. This high-order carry, AKY2, is not allowed to propagate end-around for this case of unlike signs.

When rA and rZ signs are like, the reset or complement side of rA and the set side of rZ are gated to the adder to form the sum (-rA + rZ). If AKY2 is generated, it is allowed to propagate end-around. AKY2 present during the addition causes A1 to be complemented and C19 to be set.

When no AKY2 is formed during the like signs SBM, C21 is set to store this fact. After the sum has been transferred back into rA, C21 is interrogated to see if the number in rA is a complement number. If C21 is set (i.e., AKY2 = 0 during add) the complement side of rA is gated to the adder while the rZ input (ZEN) is inhibited. The resulting sum is transferred into rA.





ADDER SUM TO AU BUS (OPG64 · T12) + (OPG33 · T16) + (X · T17 · C21 · $\overline{\text{OPN30}}$)

AU BUS TO MEMORY (OPG64 · T12)

READ INSTRUCTION TO MEMORY (OPG64 · T12)

RESET Z (OPG37 · T13)

MIR TO TRANSFER BUS (OPG64 · T23)

TRANSFER BUS TO Z (OPG37 · T14)

A TO ADDER ($\overline{\text{X}}$ · OPG50 · T16)

INDEX REGISTER TO ADDER ($\overline{\text{X}}$ · OPG50 · T16) + (X · T17 · C21 · $\overline{\text{OPN30}}$)

COMPLEMENT OF A TO ADDER (X · T16) + (X · T17 · C21 · $\overline{\text{OPN30}}$)

Z ENABLE ($\overline{\overline{\text{OPN30}} \cdot \text{T17} \cdot \text{C21} \cdot \text{X}}$) + ($\overline{\text{OPN30} \cdot \text{T17} \cdot \overline{\text{C19}} \cdot \text{X}}$)

AU BUS TO ADDER (CAA · MC0) + (OPG20 · T16 · MC0)

COMPLEMENT THE SIGN OF A (X · T16 · AKY2 · $\overline{\text{OPN30}}$ · MC0)

SET PULSE FOR C17 ($\overline{\text{X}}$ · T16 · OPG50 · AKY2 · AUA)

SET PULSE FOR C21 [OPG50 · $\overline{\text{AKY2}}$ (OPG39 · $\overline{\text{XTA}}$ · AUA)]

ENABLE NEXT FETCH (OPG52 · T15)

NOTE: X = [(OPN30 · C18 + OPG30) $\overline{\text{AQZ}}$ + [(OPN30 · $\overline{\text{C18}}$ · OPG31) AQZ]

Figure 4-21. OPN 21 Subtract Magnitude of Memory from A, Flow Chart and Timing Diagram

The signals causing the sum to be formed are ATA or CAA which select the set or reset side of rA as an augend to the adder while simultaneously removing the index inputs to the adder. The signal, SEN, gates the resulting sum output of the adder into the AU bus. Finally, AUA gates the AU bus into the A register. All of these signals are generated during T16 and all are a full 1-μsec pulse excepting the AUA which is a 0.6-μsec pulse during the last 0.6 μsec of T16. During AUA time, the carry AKY2 is interrogated for C17, C19, and C21.

During T17, time C21 is used to make the complement rA decision. If rA is to be complemented, CAA and AUA is generated. During time time rZ and rX are inhibited as adder inputs. The sum output of the adder will be the complement of the A register. AUA transfers this sum into rA.

At T15 time, an enable next fetch pulse (ENF) is generated which will initiate the next fetch cycle.

OUTPUT FROM MEMORY (OTM) OPN22

OTM is performed by executing one transfer with the transfer bus and a memory access which will transfer the memory word specified by the effective address to the output (Figure 4-22).

The transition from fetch to the operate cycle is a function of the input-output ready flip-flop (C4). C4 is a synchronizing flip-flop which is set at the beginning of a clock cycle after the asynchronous output ready pulse (IOR) occurs. One microsecond after C4 is set, the operate clock will start. During T12 time, a read memory cycle will be initiated.

During T13 time, an REZ pulse will be generated which will reset the Z register and at T14 time, a pulse TTZ will transfer the contents of the transfer bus to the Z register.

During T25 time, the signal ZTT will be generated which will transfer the contents of the Z register to the transfer bus. During T16 time, a TTO signal will be produced which will transfer the contents of the bus to the output. Also, during T16 time, a RRS signal will be generated and the leading edge of this pulse will reset IOR and one microsecond later C4 will be reset.

At T15 time, an enable next fetch signal (ENF) is generated, which will initiate the next fetch cycle.

LOAD B (LDB) OPN23

LDB is performed by executing two transfers with the transfer bus and a memory access (Figure 4-23).

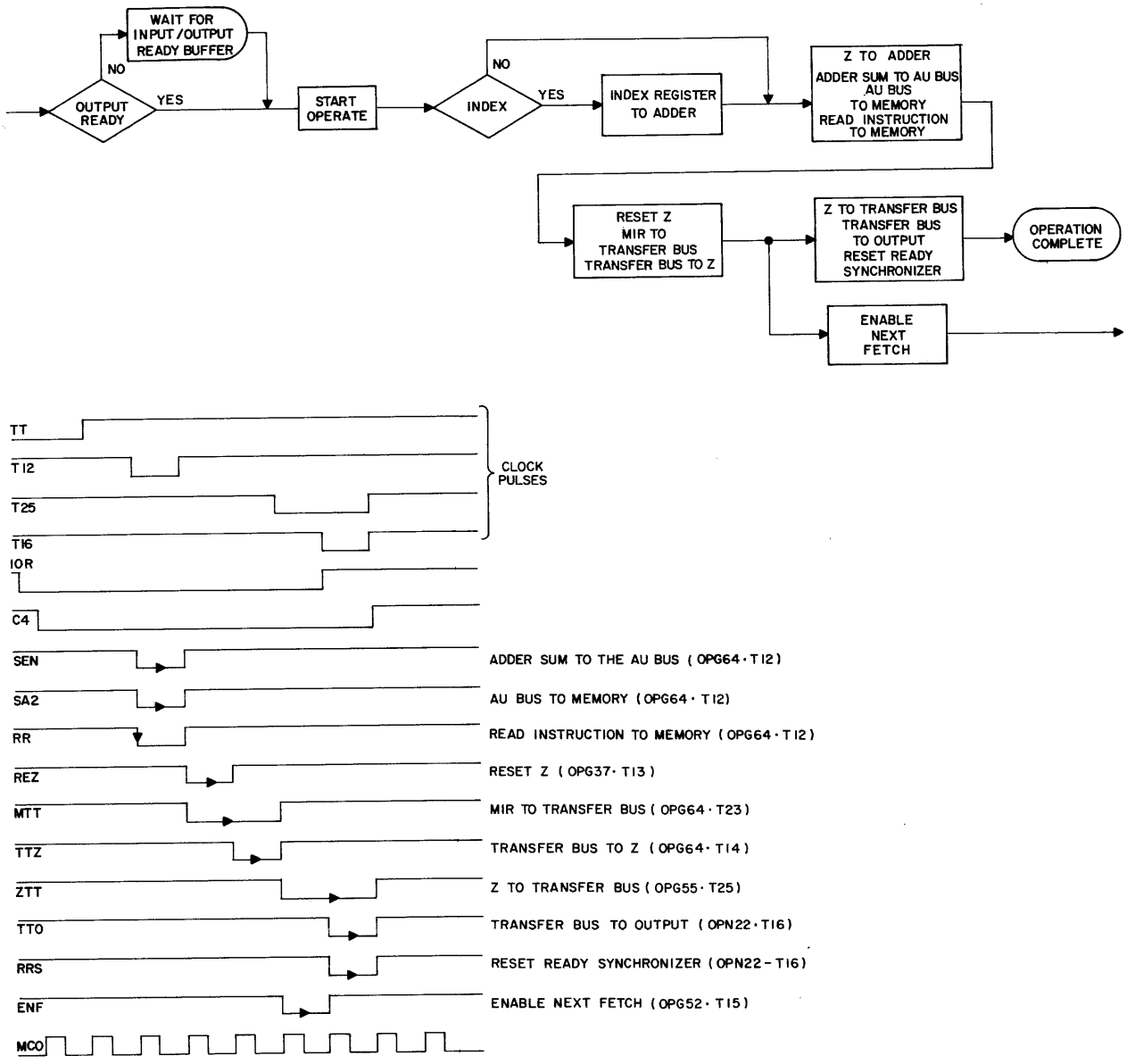


Figure 4-22. OPN 22 Output from Memory, Flow Chart and Timing Diagram

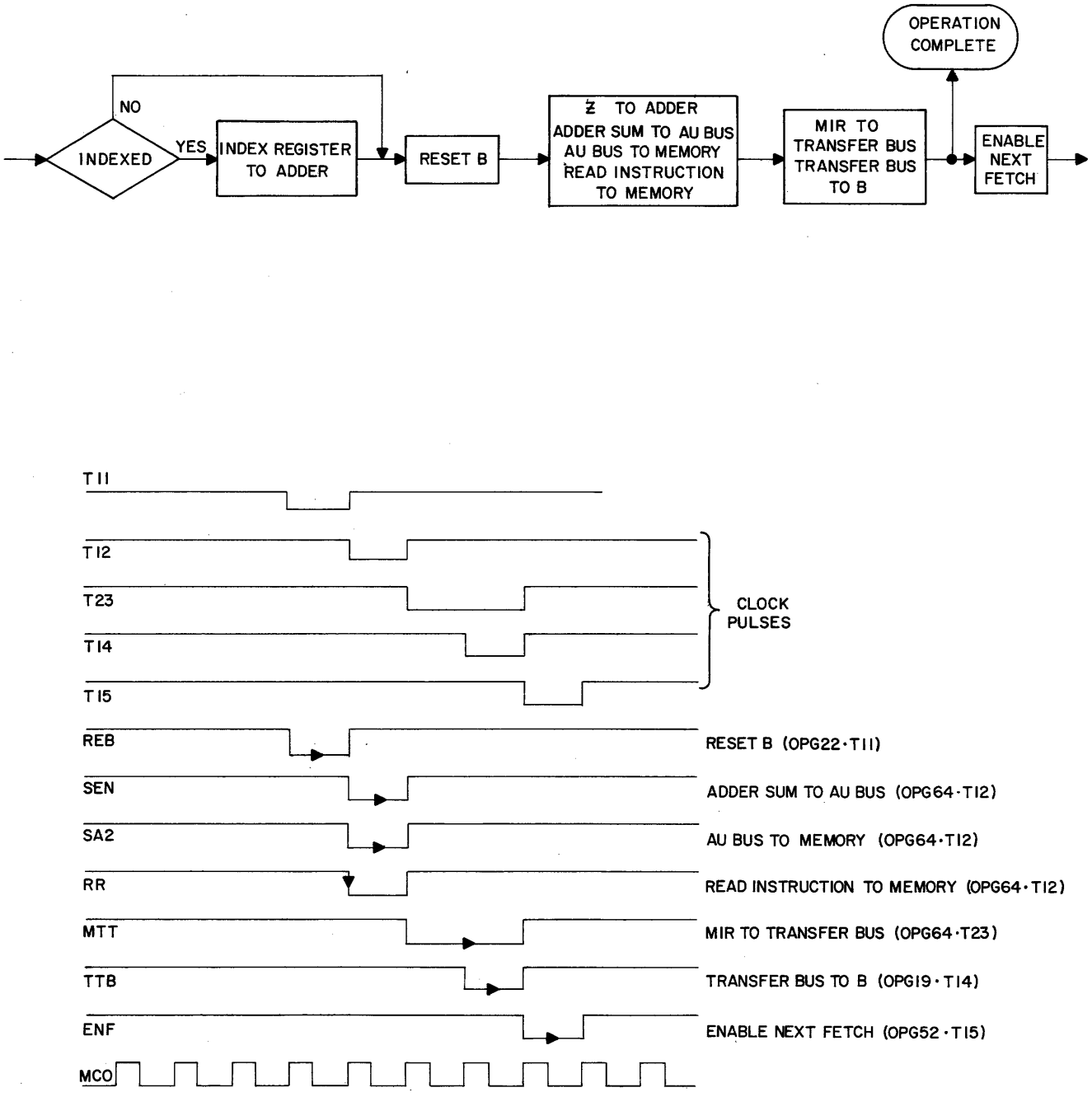


Figure 4-23. OPN 23 Load B, Flow Chart and Timing Diagram

The operate cycle is entered and during T12 time, a read memory access is initiated. At T11 time, an REB signal is generated which will reset the B register, and at T13 time, REZ is generated which will reset the Z register.

During T14 time TTB and TTZ signals are generated which will transfer the contents of the transfer bus into the B and Z registers.

At T15 time, an enable next fetch pulse (ENF) is generated which will initiate the next fetch cycle.

LOAD A (LDA) OPN24

LDA is performed by executing three transfers and a memory access; (two transfers involve the transfer bus and the other uses the AU bus) (Figure 4-24).

The operate cycle is entered, and during T12 time, a read memory access is initiated. During T13 time, an REZ pulse is generated which will reset the Z register. During T14 time, a TTZ signal is produced which will enable the transfer bus into the Z register.

During T25 time, the signal ZTT will gate the contents of the Z register to the transfer bus. A TTA signal generated during T16 time will gate the transfer bus to the AU bus and AUA (a 0.6 μsec pulse) will gate the AU bus to the A register.

At T15 time, an enable next fetch signal (ENF) is generated which will initiate the next fetch cycle.

JUMP RETURN (JRT) OPN25

This command requires a read memory cycle and two transfers, one with the transfer bus and the other with the AU bus (Figure 4-25).

The operate cycle is entered and during T12 time, a read memory access is initiated. During T13 time, an REZ pulse is generated which resets the Z register.

During T14 time, a TTZ pulse is generated which gates the contents of the transfer bus into the Z register. Also during T14 time, a TSR pulse is generated which will set a group of special registers according to the information stored in the nine high-order columns of the transfer bus. The add-subtract control flip-flop, C18, will be set by TSR if column one of the transfer bus is true. The complement sign of rA control flip-flop, C19, will be set by TSR if column two of the transfer bus is true. The A2 or AKY2 store flip-flop, C21, will be set by TSR if column three is true and an input-output channel enable flip-flop will be set by TSR according to the information stored in columns four through nine.

During T26, time the XTA-1 signal which gates the index register outputs to the adder is inhibited and SEN, a signal also produced during T17 time, will gate the sum output of the adder to the AU bus. Because ZEN is true while XTA, ATA, and CAA are not,

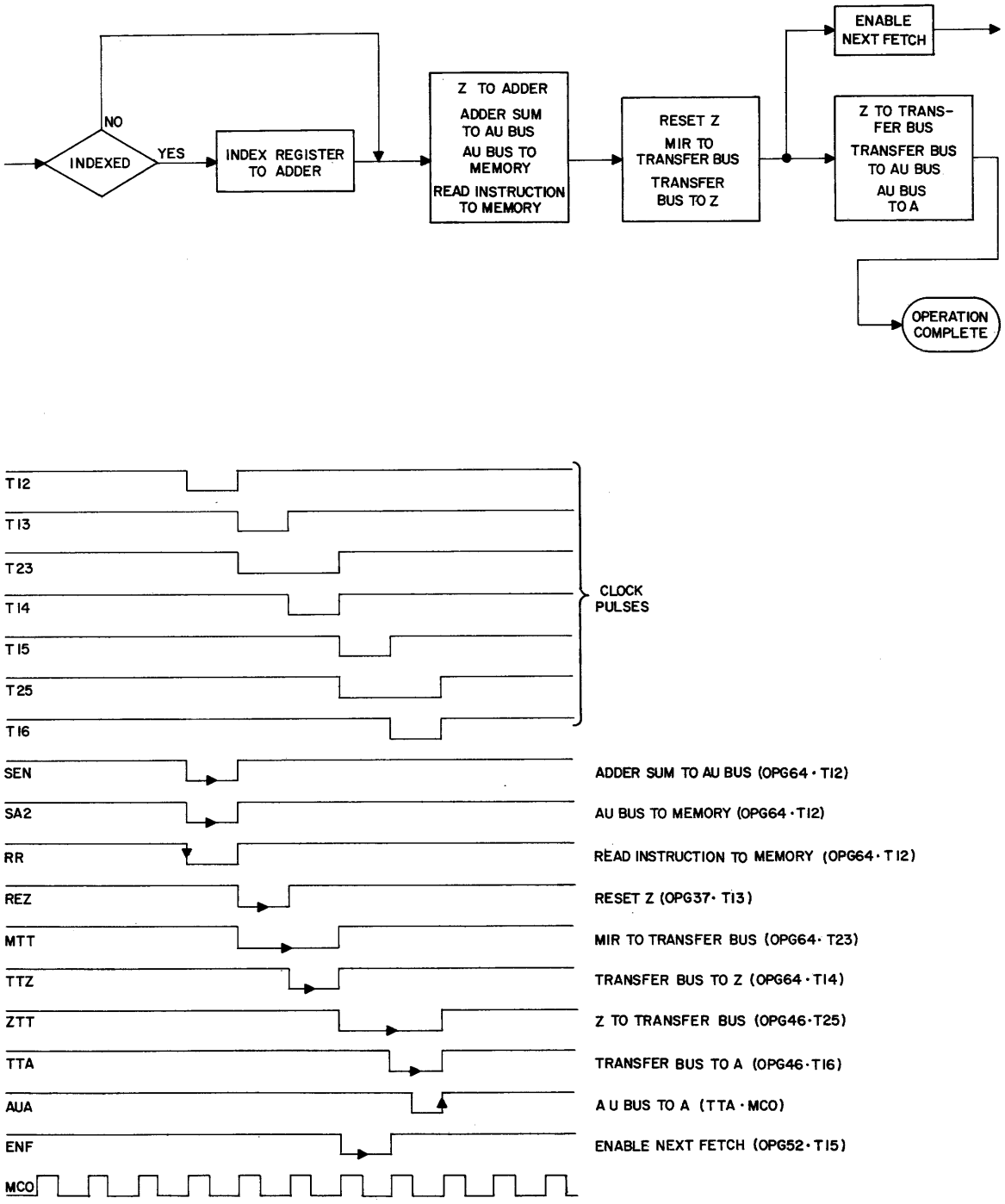


Figure 4-24. OPN 24 Load A, Flow Chart and Timing Diagram

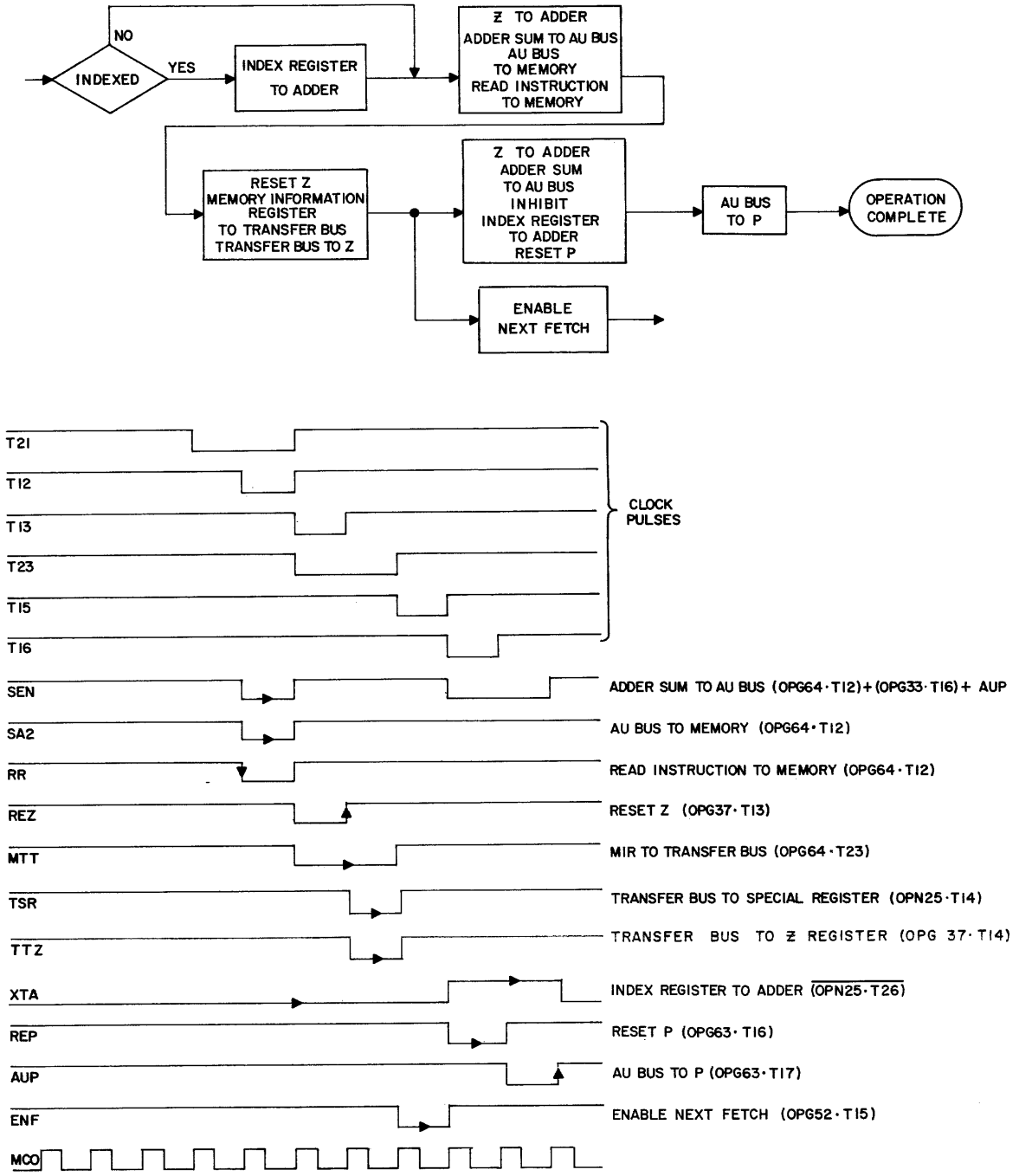


Figure 4-25. OPN 25 Jump Return, Flow Chart and Timing Diagram

the output of the adder at this time is equal to rZ. During T16 time, a REP signal is generated to reset the contents of the program counter and an AUP signal is generated during T17 time to transfer the contents of the AU bus into the program counter.

At T15 time, an enable next fetch (ENF) is generated which will initiate the next fetch cycle.

JUMP AND STORE WITHOUT INTERRUPT (JST) OPN27

The execution of a JST command, which takes place when C23 is reset, comprises a memory write cycle to store the contents of rP at the effective address and update rP with the effective address plus one (Figure 4-26).

The operate cycle is entered and during T12 time, a write-memory access is initiated. At T23 time, a PTT signal transfers the P register to the transfer bus, and an AD signal allows a partial substitution into the address field of the memory word specified by the effective address.

During T26 time, ZEN and IEC1 enable the adder with inputs rZ and a low-order twenty-four which is in the form of a carry into column twenty-four. During this addition, the end-around-carry input to the incoming carry logic of column 24 is disabled. The sum generated is the effective address incremented by one.

During T16 and T17 time, the SEN signal gates the above sum to the AU bus. During T16 time, an REP signal is generated to reset the P register, and during T17 time, an AUP signal is produced to gate the low order 15 bits of the AU bus into the program counter.

At T15 time an enable next fetch pulse (ENF) is generated to initiate a new fetch cycle.

JUMP AND STORE WITH INTERRUPT (JST) OPN27

The execution of JST during an interrupt cycle comprises a memory write cycle for storing the contents of P and the special registers at a predetermined address peculiar to the affected interrupt line. rP is updated with this predetermined address plus one (Figure 4-27).

The interrupt waiting-to-be-processed flip-flop (C22) will be set when an interrupt is to be processed. If C22 is set, the ENF pulse from the previous instruction will set the interrupt cycle flip-flop (C23) and will cause C22 to be reset.

During TF3 of the fetch cycle, KTZ jams the predetermined interrupt address into rZ and 27 will be jammed into the O register. At T12 time, a write-memory-access is initiated. During T23 time, the AD signal is inhibited since C23 is set, and a PTT signal transfers the program counter (P) to the low-order 15 bits of the transfer bus to MIR. Also during T23 time, an SRT signal gates the status of the following registers into the nine high-order columns of the transfer bus to MIR.

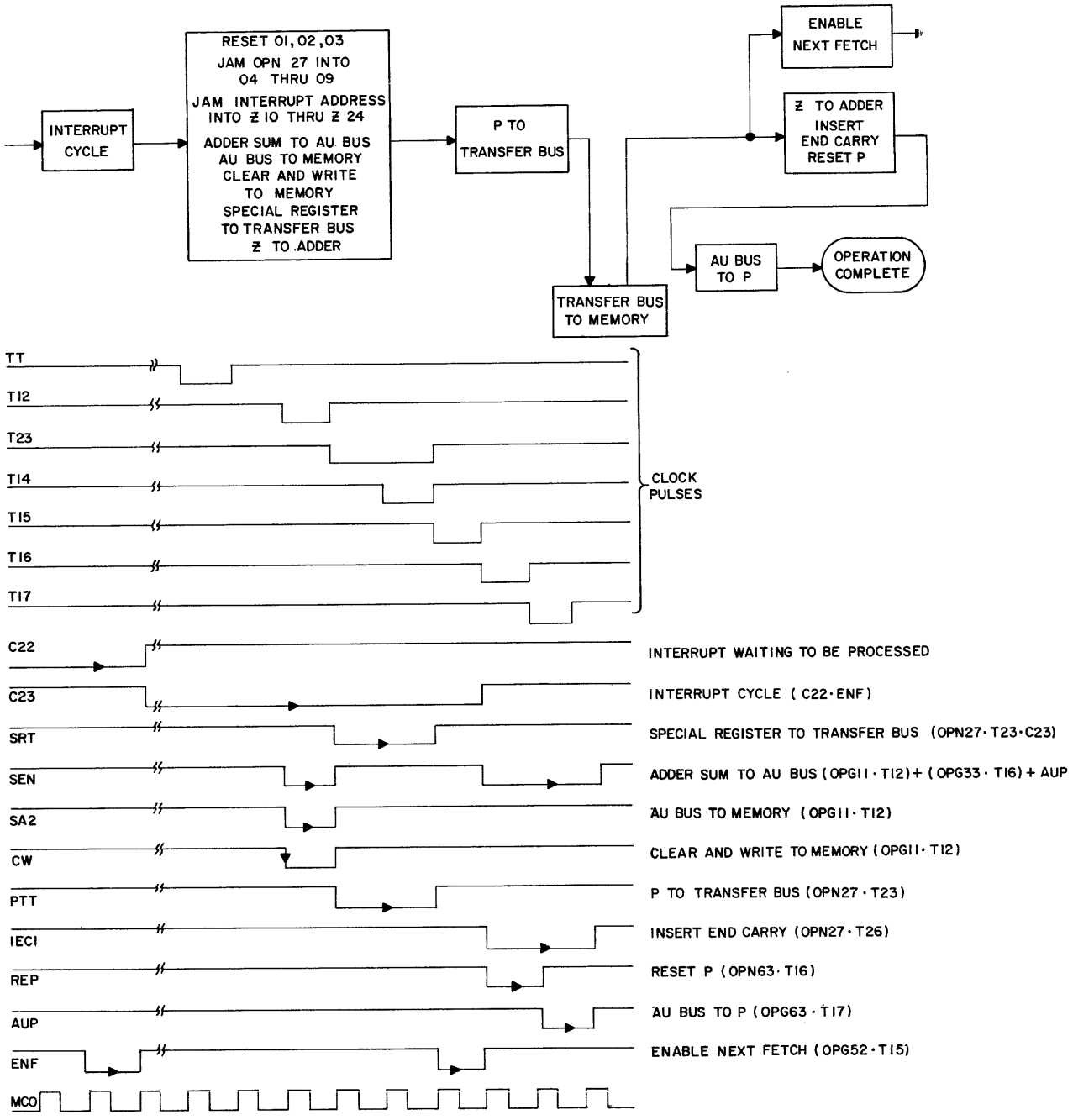
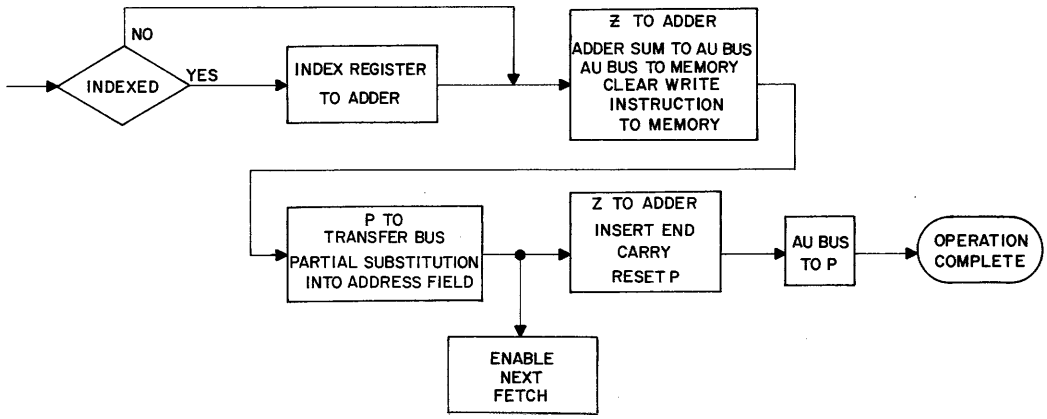


Figure 4-26. OPN 27 Jump and Store Without Interrupt, Flow Chart and Timing Diagram



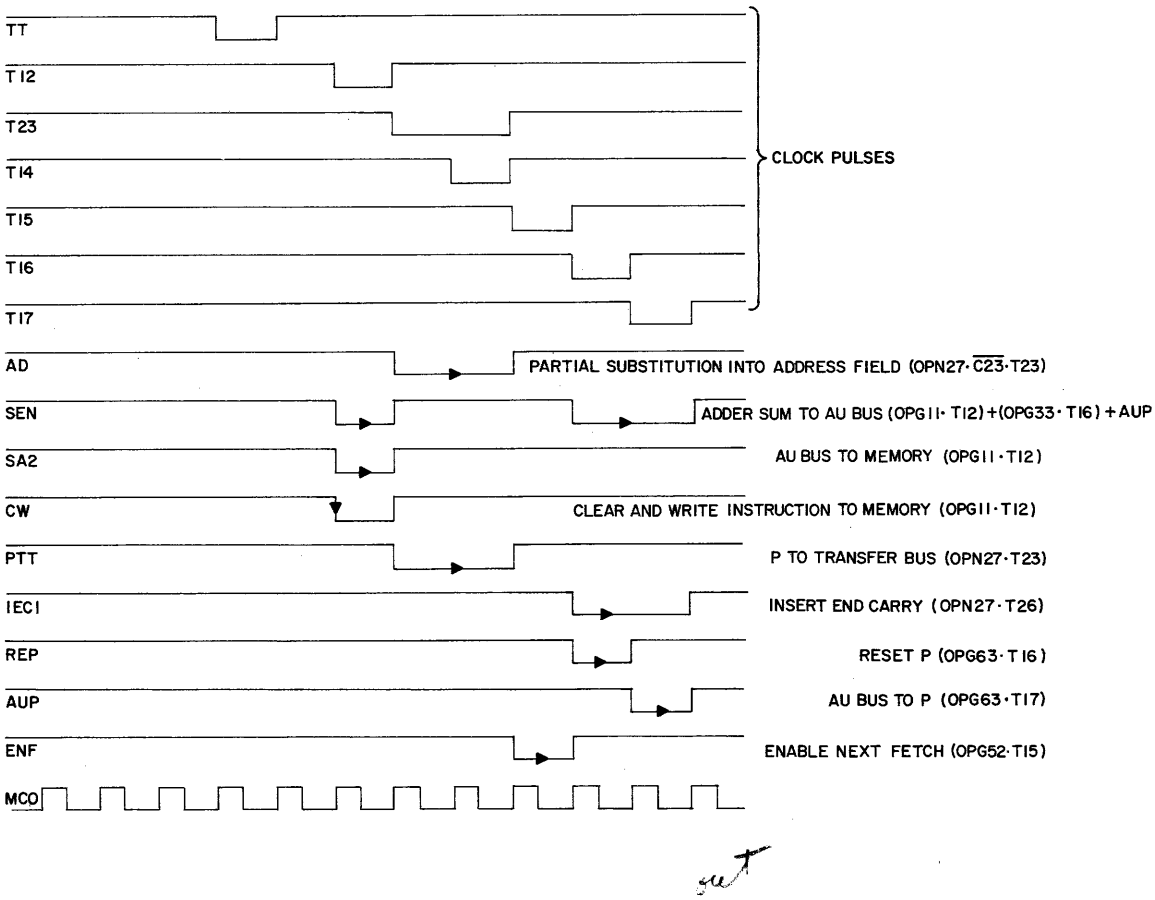


Figure 4-27. OPN 27 Jump and Store With Interrupt, Flow Chart and Timing Diagram

a. The add-sub control flip-flop, C18, into bit position 1.

b. The complement sign of A flip-flop, C19, into bit position 2.

c. The A2 or AKY2 store flip-flop, C21, into bit position 3.

d. Enabled I/O channel encoder outputs in bit positions 4-9.

During T26 time, an IEC1 signal inserts an end-carry into the low-order column (bit 24) of the adder, and ZEN enables rZ as an input to the adder. SEN, which enables the sum output of the adder to the AU bus, is generated during T16 and T17 time. AUP, which transfers the AU bus into P is generated at T17 time. REP is also generated during T16 time to reset the program counter. Thus, the predetermined address plus one is now loaded in the program counter.

At T15 time, an enable next fetch (ENF) is generated to initiate the next fetch cycle.

STEP MULTIPLE PRECISION (SMP) OPN30

Certain preliminary remarks concerning this instruction are required. Past history should have been recorded in certain flip-flops prior to entry into a multiple precision program. These flip-flops are C18, the add-subtract flip-flop; C19, the complement sign-of-A flip-flop, and C21 a carry-store flip-flop. When an add instruction is processed, C18 sets and remains set until a subtract instruction is processed, at which time it resets. Thus C18 stores the instructions (add or subtract) which occurred most recently. C19 stores the fact that during the last add or subtract instruction it was necessary to complement the sign of rA. C21 represents the fact that a carry was generated during the last add-type instruction. In the case of C21 this last add-type instruction could well have been another OPN30 instruction. C21 allows a carry to be propagated from one SMP instruction to the next in such a manner that starting with the low order of an SMP group, the carry-out of low order will be stored and added into the next higher order SMP group. Should a carry occur during that SMP, C21 again sets and supplies a carry into the following SMP. Thus the carry is propagated up the line until the high-order addition of the multiple precision word is reached. C18 is gated against the fact that an OPN30 instruction is being processed to allow the processor to treat the SMP as an add or subtract. Thus, the add algorithm is followed if C18 is set during the execution of an SMP instruction while a subtract algorithm will be followed if the C18 is reset during the execution of SMP instruction (Figure 4-28).

The SMP instruction requires a memory access to obtain the operand to be added or subtracted, as the case may be, to the A register. This memory access takes place at T12 time in the same manner as the memory access for an add command. Once the operand has been obtained from memory and placed in the Z register, the algorithm of the command follows the algorithm of either the add or subtract commands. The algorithm to be used is a function of C18. One thing peculiar to the SMP is the insertion of an end

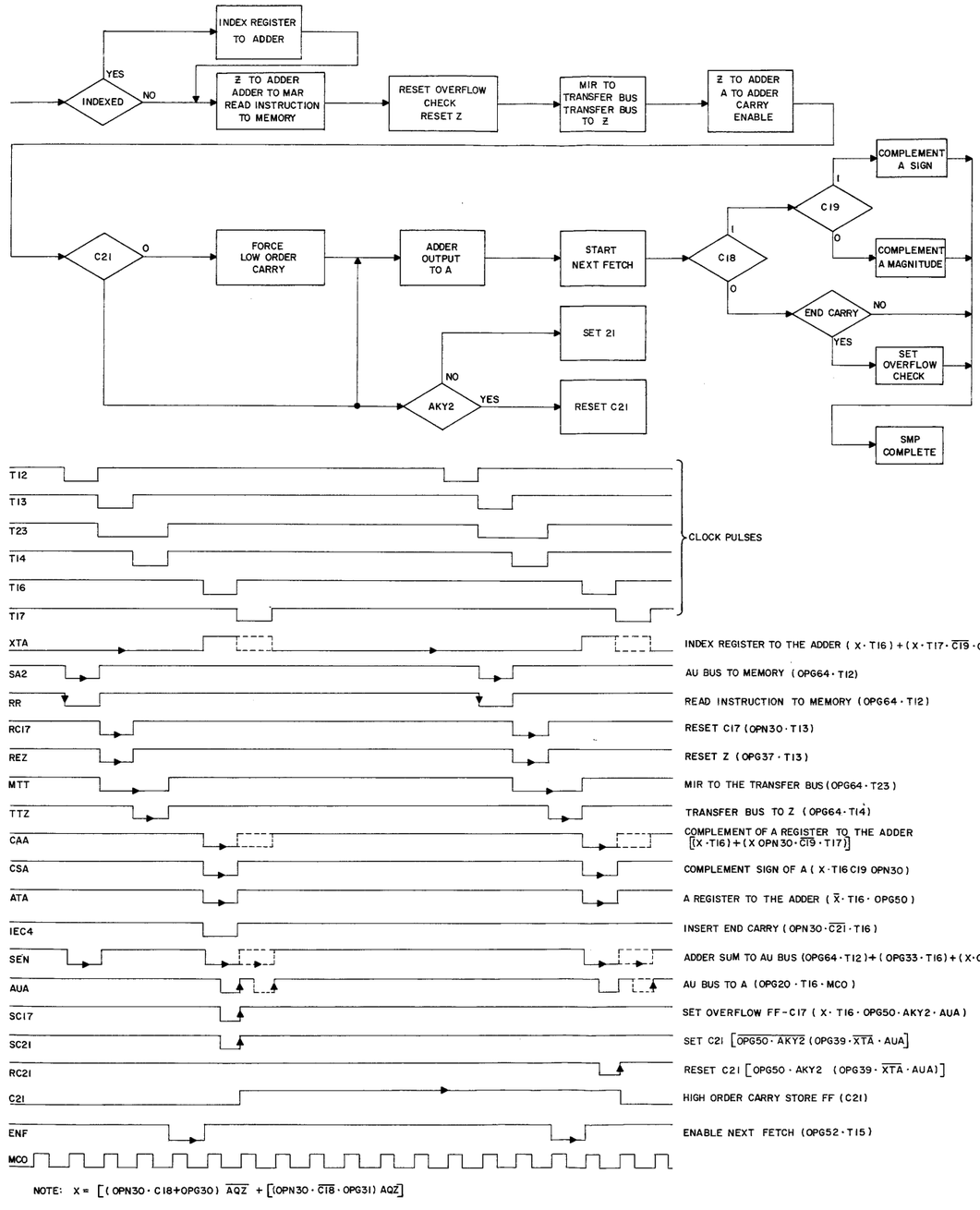


Figure 4-28. OPN 30 Step Multiple Precision, Flow Chart and Timing Diagram

carry-during the gating of the adder. If this SMP is an intermediate SMP and the carry originated in the prior SMP, an end carry will be inserted to carry into the new SMP.

The decision with respect to the complementing of the sign of rA is a function of C19 which stores the fact that in the last add or subtract command, (as the case may be) it was necessary to complement the sign of rA. In all probability this last add or subtract will have been the add or subtract used as the entry into the SMP program and will represent the addition or subtraction of the high-order words of the multiple precision words.

At T15 time, an enable next fetch (ENF) is generated to initiate the next fetch cycle.

FILL MEMORY BLOCK (FMB) OPN31

This is an input type instruction which causes a full interrupt of the machine cycle. As an input type instruction, it is subjected to the normal input ready interlock such that TT testing for operate interrogates the ready status. The central processor stays in TT time until the input device is ready for the first word to be transferred into the DDP. After the initial entry into operate, a recirculation path is set up such that the machine never leaves the operate cycle. For each operate cycle taking place during FMB, there is a clear-write memory access; during each operate cycle triggered by the FMB instruction, there is a count of one to the index register. Thus each operate cycle decrements the index register. The termination of an FMB comes by way of one of two functions — counting the index register to zero or supplying an external stop signal by the input device. During TT time, the FMB command input-output ready status is interrogated. If the ready flip-flop, C4, is not set, then the machine remains in transition time until ready is achieved. One microsecond after C4 is set, the machine cycle steps from transition time to the operate area and processes the first cycle of the FMB command (Figure 4-29).

A memory access is initiated at T12 time to store the input word into the memory. At T13 time, an end-carry is generated by IEC-6, the Z input to the adder (ZEN) is blocked, and one is added to the index register. (A one is added to the index register because the adder inputs are X and an end carry.) The resulting sum is then transferred back into the index register by an AUX pulse. During the write cycle, at T23 time, the ITT signal gates the INPUT TRANSFER BUS to the transfer bus. RRS, generated at T14 time, resets the ready flip-flop associated with the input channel.

When AUX transfers the newly incremented sum back into the index register, XZD is true if the sum transferred is not zero. This output XZD is used to determine whether another operate cycle should be initiated or the FMB command has reached the terminal point and the next fetch should be started. XZD is interrogated at T14 time, by RRS, and the next operate cycle is initiated by setting T01 if XZD is true. The next cycle occurs immediately after ready status has again been achieved. However, if the input device has not obtained the next word for transfer and is not ready, the computer now stalls at

T01 time while waiting for ready. When ready status is achieved, the operate clock cycles through to T14 repeating all the steps outlined in the previous operate cycle.

If, at T14 time, XZD was false (meaning the index register contained a zero), T01 would not be set to start a new execute cycle. Instead, the next fetch cycle would be initiated. It was previously pointed out that XZD or the external stop signal could be used to terminate the FMB. If the external stop occurs before the index register is counted to zero, this external stop signal is stored in C31. It will determine whether another operate cycle should be started or the next fetch initiated.

DUMP MEMORY BLOCK (DMB) OPN32

This instruction is almost identical to the previously described instruction, FMB. The exception is that during the operate cycle a read access rather than a write access is initiated (Figure 4-30).

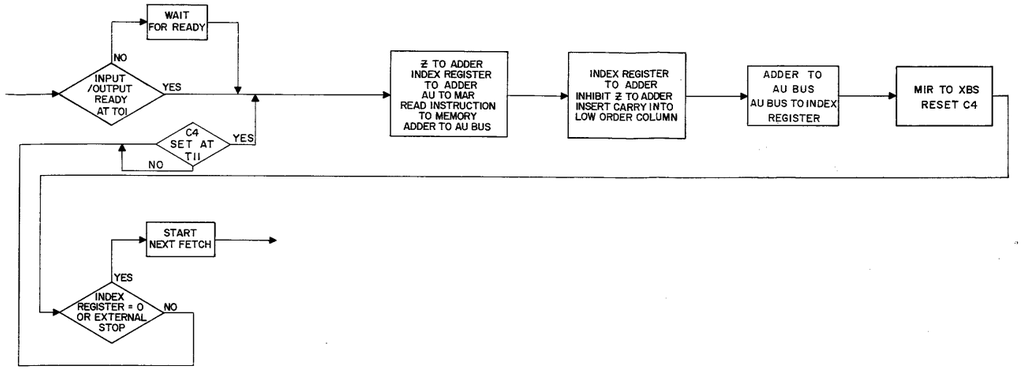
MULTIPLY (MPY) OPN34

The contents of the B and Z registers are multiplied and the resulting double length product (46 bits) replaces the contents of the A and B registers. The signs of both the A and B registers are the algebraic sign of the product (Figure 4-31).

A read memory access is initiated during T12 time to obtain the multiplier. (The multiplicand must have been left in the B register by some previous instruction.) The shift counter is set to a binary 24 count at T11 time. The Z register is reset by REZ at T13 time. During T14 time, a TTZ pulse transfers the contents of the transfer bus into the Z register. On the trailing edge of T14, T08 is set, which causes ATA and SER to become true. T08 will remain true for 23 μsec, during which time partial products are formed and the product is built up in the A and B registers. During T08 time, either the contents of the A register are shifted to the right or a shifted adder sum is strobed into the A register. (In either case, the contents of the B register shift to the right.) Which is done is determined by the least significant bit of the B register, stored in a special flip-flop, B24'. If B24' is true, ZEN is also true and the adder output is the sum of the contents of the A and Z registers (a partial product). If B24 is false, ZEN is false, and the adder output is the same as the contents of the A register. Thus, the AU bus output is either a shifted sum of the A and Z registers or just a shifted A register. The trailing edge of each AUA pulse transfers the AU bus into the A register. An SSC pulse decrements the shift counter during each microsecond of T08. The next fetch is enabled when the contents of the shift counter reach 4. If B1 and Z1 are unlike, the sign bit A1 is set, at T15 time, and A1 is copied into B1. When the shift counter reaches 1 the multiplication is complete.

DIVIDE (DIV) OPN35

The contents of the A and B registers are divided by the contents of the specified memory address, the quotient replaces the contents of the B register, and the remainder replaces the contents of the A register (Figure 4-32).



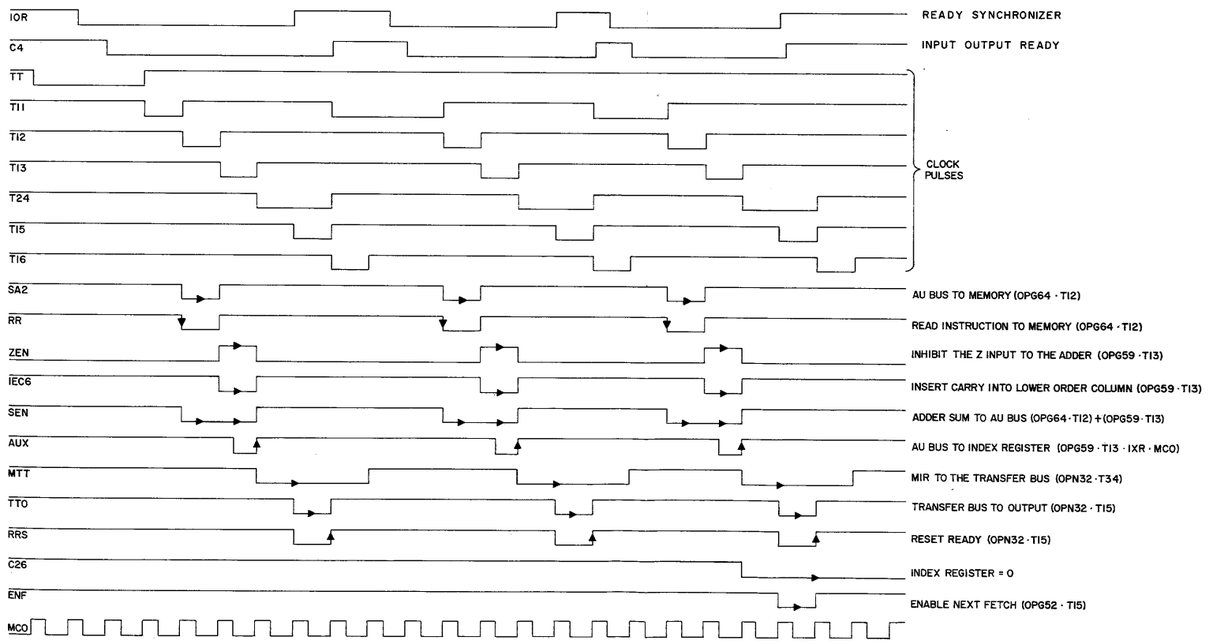
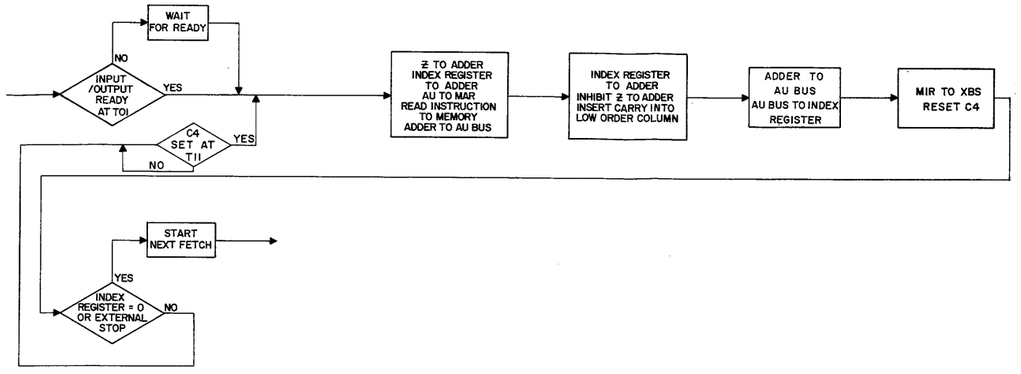


Figure 4-29. OPN 31 Fill Memory Block Flow Chart and Timing Diagram



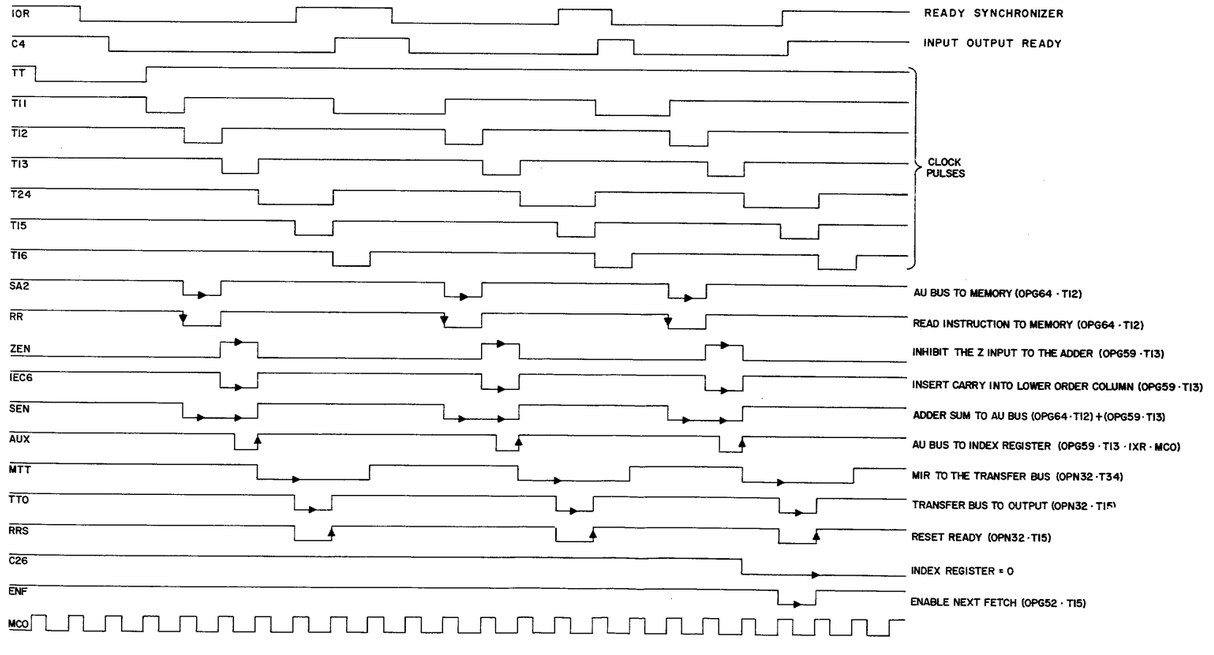
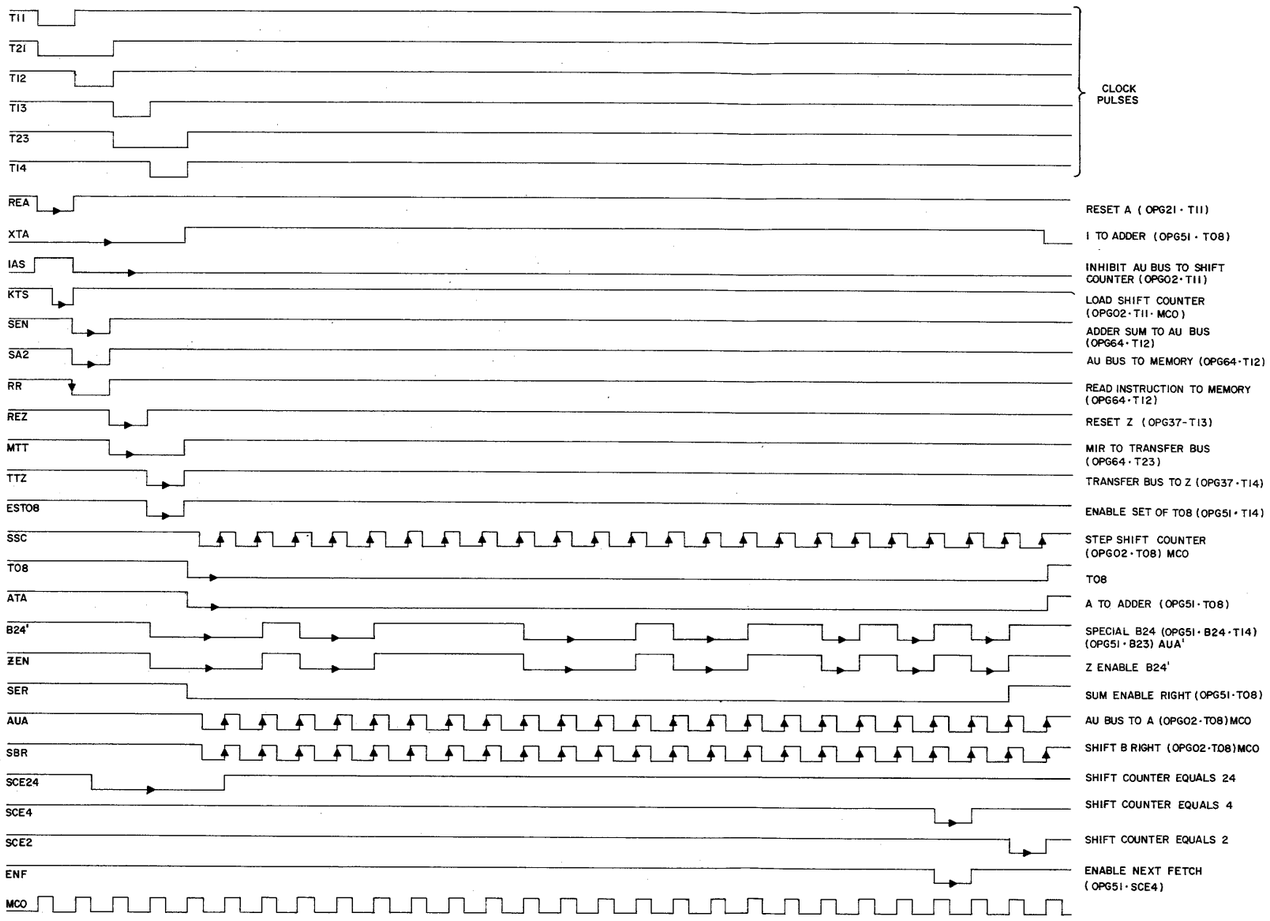


Figure 4-30. OPN 32 Dump Memory Block, Flow Chart and Timing Diagram



NOTE: 1. DURING AUA TIME, AKY2 IS TRANSFERED INTO A2

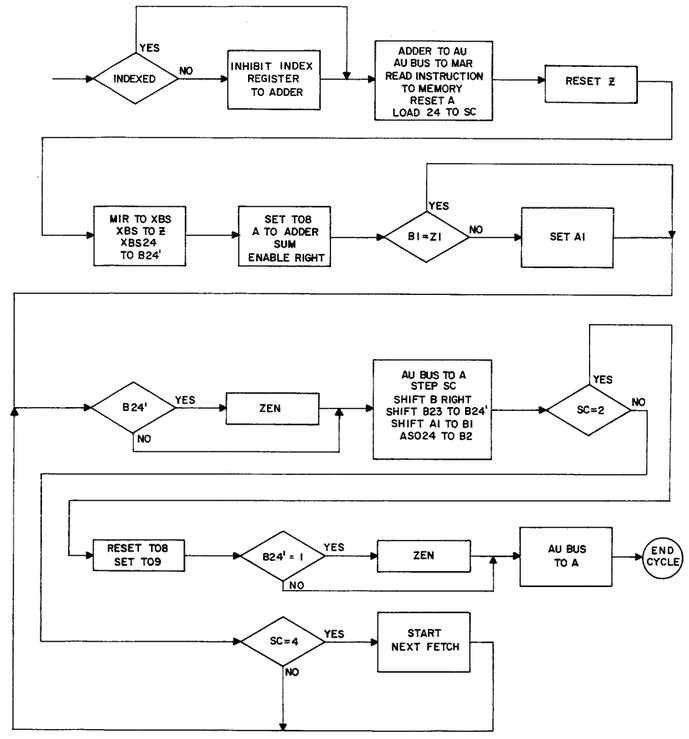


Figure 4-31. OPN 34 Multiply, Flow Chart and Timing Diagram

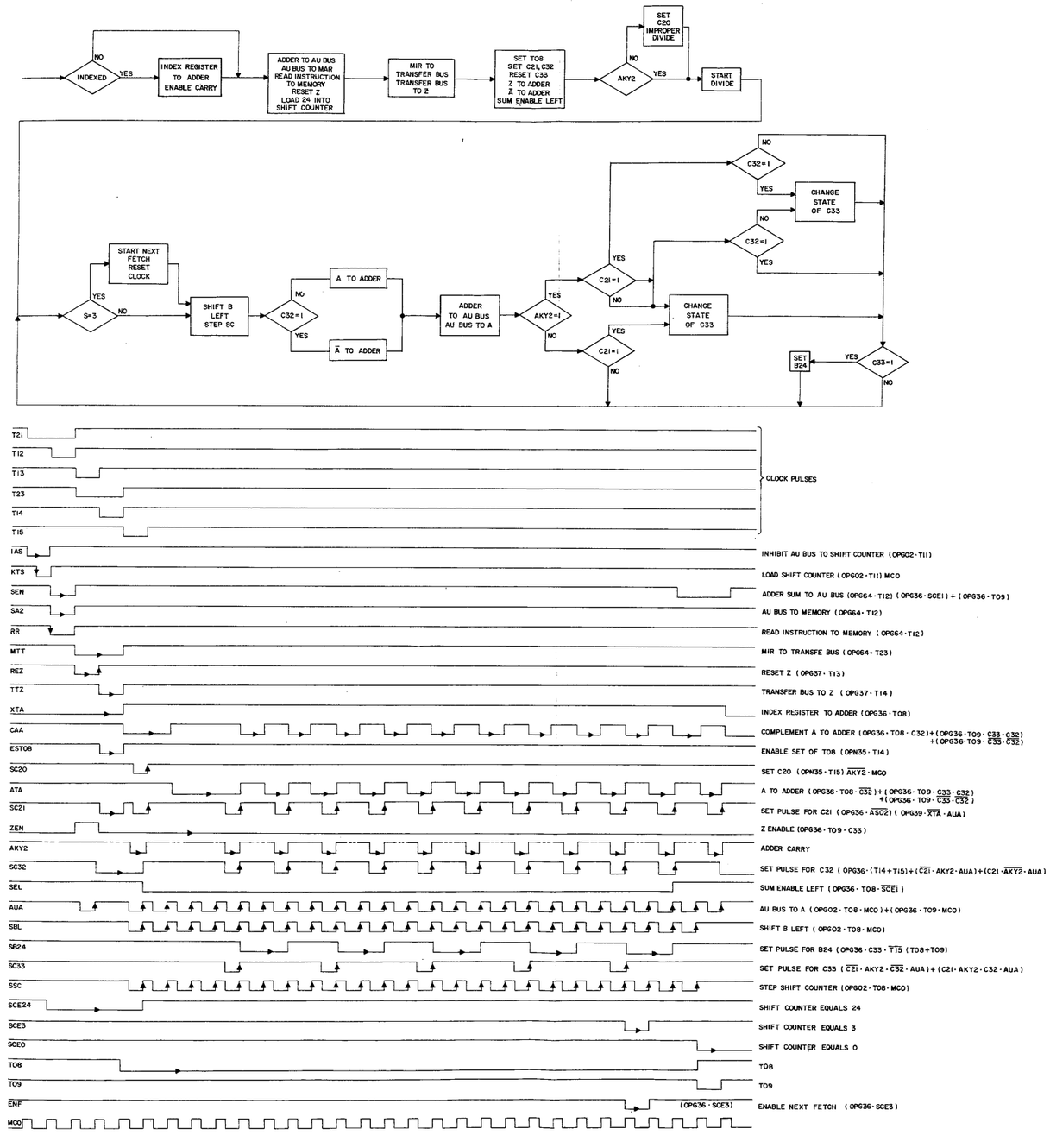


Figure 4-32. OPN 35 Divide, Flow Chart and Timing Diagram

A read memory access is initiated during T12 time to obtain the divisor and the contents of the shift counter are set to a binary 24. The Z register is reset by REZ at T13 time and during T14 time, a TTZ pulse transfers the contents of the transfer bus into the Z register. During T14 and T15, divide control flip-flop C32 is set and C33 is reset. Control flip-flop C21 is set at T14. TO8 is set at the trailing edge of T14 and will remain set until the shift counter has been decremented to zero. An improper division test is performed at T15 time while C32 generates CAA. If no carry exists out of the most significant magnitude bit column (AKY2 is false), an improper divide case exists and flip-flop C20 is set. Division proceeds if it is improper or not. The shift counter has been decremented at the trailing edge of T15 and will continue to be decremented at the trailing edge of each microsecond pulse during TO8. An AUA, occurring each microsecond of TO8, will transfer adder outputs into the A register and will also store the complement of the most significant magnitude bit sum in flip-flop C21. C32 controls addition and subtraction for non-restoring division by generating CAA if set and ATA if reset. The operation (add or subtract) for each division step is determined by the result of the previous step. If C21 and AKY2 are both true or both false at AUA time, C32 is unchanged and the same operation will be repeated. If C21 and AKY2 are unlike at AUA time, due to a zero crossover of the partial remainder, C32 will change stage to cause the alternate operation to be performed during the next step. Zero crossover is detected by C32 which, in turn, sets each bit of the quotient into the least significant bit of the B register. C32 also controls complementing of the contents of the B register as it is shifted into the A register (B? into A24). Zero crossover occurs during each division step when adding (C32 false) if a carry exists out of the most significant magnitude bit column (AKY2 true) and the most significant bit sum during the previous step was a one (C21 false). Zero crossover also occurs during each division step when subtracting (C32 true) if a carry exists out of the most significant magnitude bit column (AKY2 true) and the most significant bit sum during the previous step was a zero (C21 true), provided that a zero crossover had not occurred during the previous step. If it had occurred, the above conditions represent no zero crossover during TO8 time (except T15) if C32 is false, C21 is false, and AKY2 is true, or if C32 is true, C21 is true, and AKY2 is true, C33 will be set. If C32 is false, C21 false, and AKY2 true, or if C32 is true, C21 is true and AKY2 is true, C33 will be reset. SEL is true all during TO8 to allow transfer of shifted sum outputs from the adder into the A register. The B register is also shifted one place to the left each microsecond of TO8 by SBL. On the trailing edge of shift counter equals one (SCE1), TO8 is reset and TO9 is set. Remainder correction takes place during TO9. Three corrections are possible — addition, subtraction, or complementing. If both C32 and C33 are false, addition is performed. If C32 is false and C33 is true, complementing is performed, and if C32 is true and C33 is false, subtraction is performed. A fourth case, that of no change, is allowed for ease of implementing the other three cases by adding the contents of the A register to zero. The sign of the remainder (A1) is unchanged. The sign of the quotient (B1) is reset at T11 and set at TO9 if the signs of A and Z are unlike.

A RIGHT SHIFT (ARS) OPN40

This instruction will shift rA right the specified number of shifts as indicated by the six low-order bits of the effective address (Figure 4-33).

SEN is generated at T11 time and gates the adder sum to the AU bus. During the last 0.6 sec of T11, KTS loads the shift counter with the low-order six bits on the AU bus. If there is an index bit in the instruction word, XTA is enabled during T11 time, allowing the address portion of the instruction word to be equal to the sum of rZ plus the specified index register. On the trailing edge of T12, the shift enable flip-flop (C12) is set if the shift counter is not equal to zero. C12 disables ZEN and XTA and at the same time enables the A register to the adder (ATA), and the sum enable right (SER). C12 and the 1-MC clock generate SSC which steps the shift counter and gates the AU bus to rA (AUA). C12 is reset on the trailing edge of shift counter equals one (SCE1). The A register is shifted right one position for each shift count.

The sign bit of rA is not included in the shift and zeros are inserted into bit two position.

Enable next fetch (ENF) is generated at shift counter equals three (SCE3) and the next fetch is initiated on the trailing edge of SCE3. If a shift of 0, 1, or 2 bit positions is specified, ENF is generated at T12 time.

A LEFT SHIFT (ALS) OPN41

This instruction will shift rA left the specified number of shifts as indicated by the six low-order bits of the effective address (Figure 4-34).

SEN is generated at T11 time and gates the adder sum onto the AU bus. During the last 0.6 μsec of T11, KTS loads the shift counter with the low-order six bits on the AU bus. If there is an index bit in the instruction word, XTA is enabled during T11 time and allows the address portion of the instruction word to be equal to the sum of rZ plus the specified index register. On the trailing edge of T12, the shift enable flip-flop (C12) is set if the shift counter is not equal to zero. C12 disables ZEN and XTA and at the same time enables the A register to the adder (ATA) and the sum enable left (SEL). C12 and the 1-MC clock generate SSC which steps the shift counter once for each bit that A is shifted left and gates the AU bus to rA (AUA). C12 is reset on the trailing edge of shift-counter-equals-one pulse (SCE1). A register is shifted left except the sign bit and zeros are inserted into bit twenty-four position. If a one bit is shifted out of the position next to the sign of rA, the overflow indication is set.

Enable next fetch (ENF) is generated at shift counter equals three (SCE3) and the next fetch is initiated on the trailing edge of SCE3. If a shift of 0, 1, or 2 bit positions is specified, ENF is generated at T12 time.

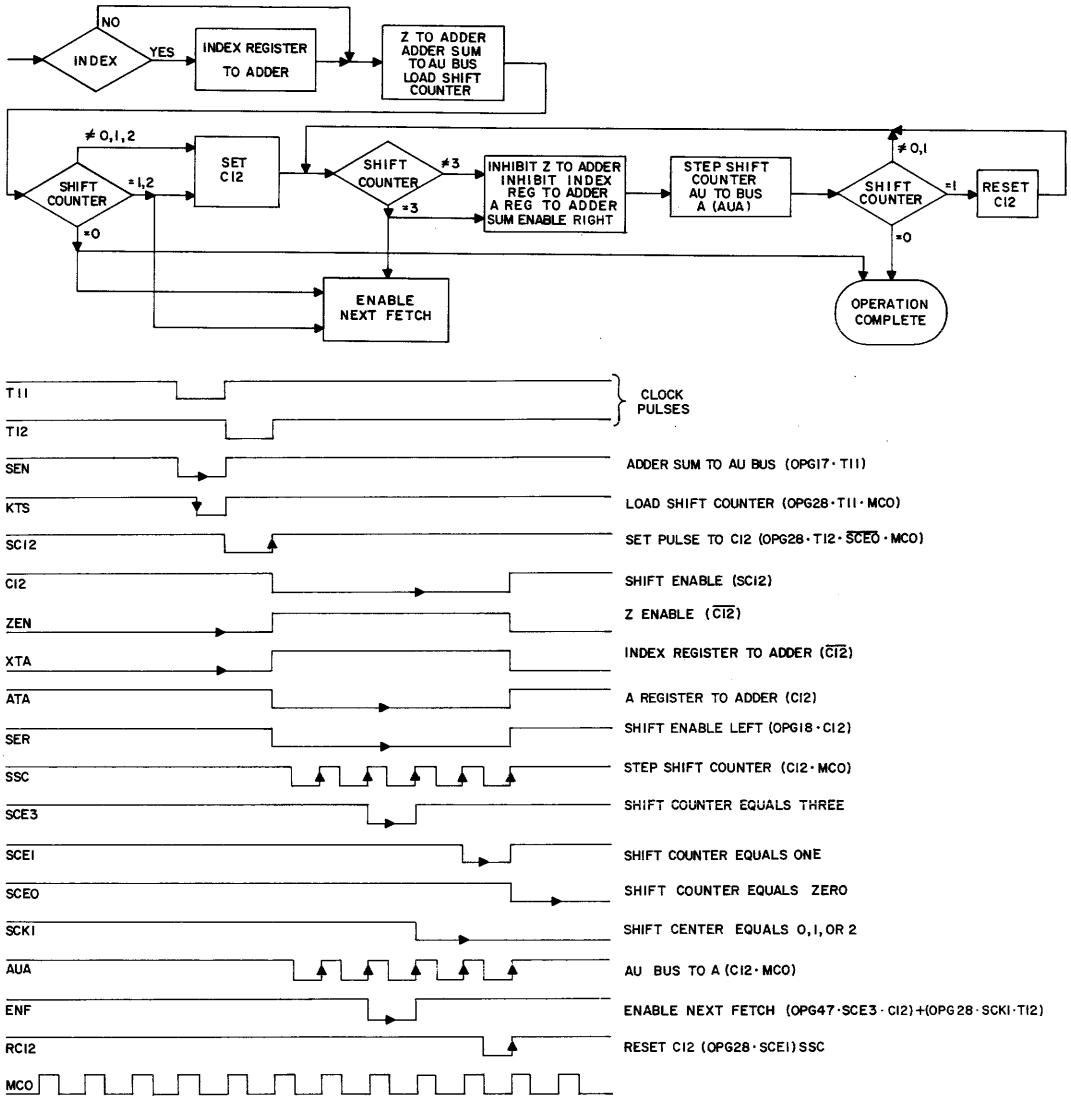


Figure 4-33. OPN 40 A Right Shift

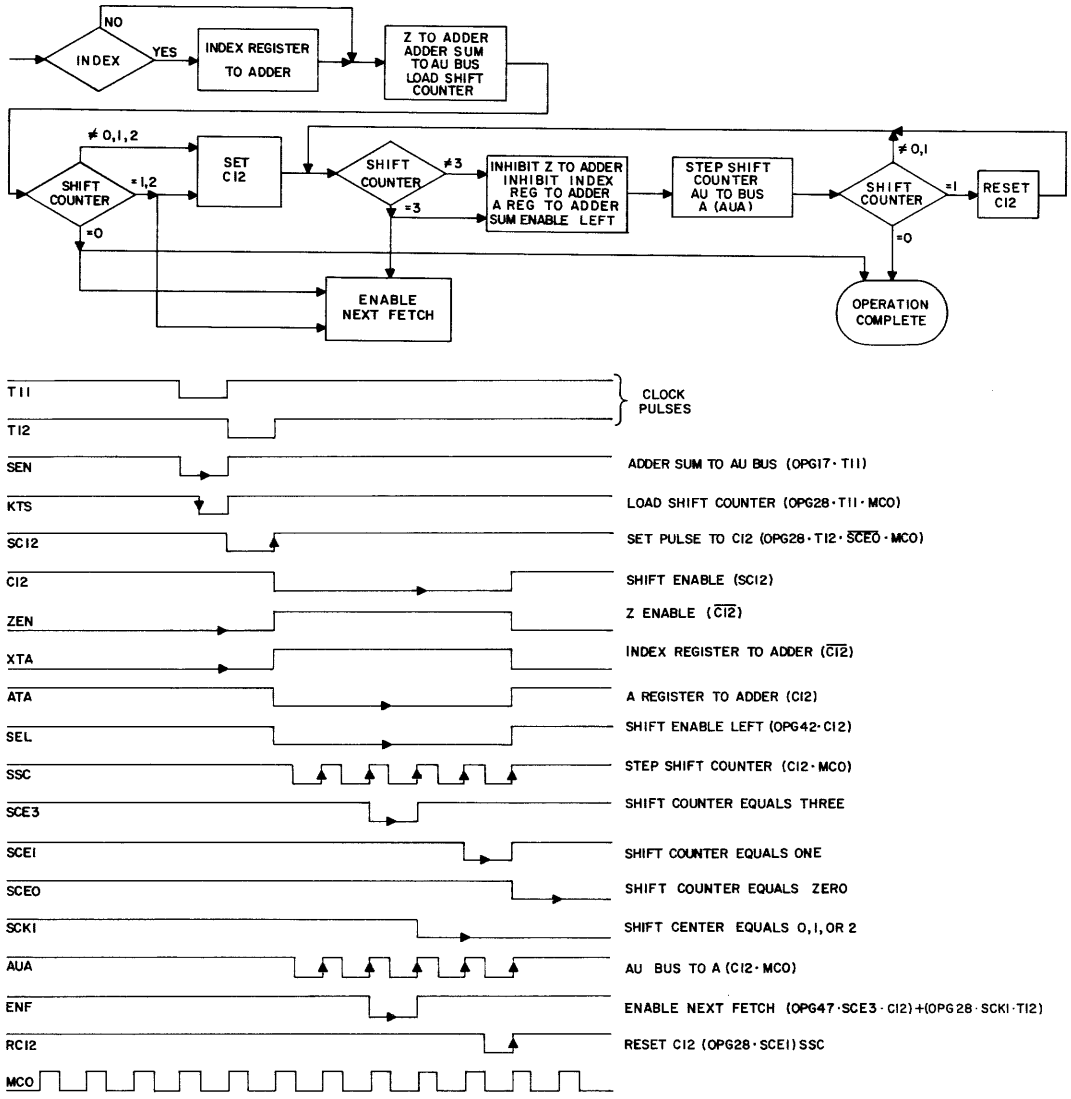


Figure 4-34. OPN 41 A Left Shift, Flow Chart and Timing Diagram

LONG RIGHT ROTATE (LRR) OPN42

This instruction will treat the A and B registers as one and shift right the number of shifts indicated by the six low-order bits of the effective address (Figure 4-35).

SEN is generated at T11 time and gates the adder sum to the AU bus. During the last 0.6 μsec of T11, KTS loads the shift counter with the low-order six bits on the AU bus. If there is an index bit in the instruction word, XTA is enabled during the forming of the effective address at T11 time and allows the address portion of the instruction word to be equal to the sum of rZ plus the specified index register. On the trailing edge of T12, the shift enable flip-flop (C12) is set if the shift counter is not equal to zero. C12 simultaneously disables ZEN and XTA and enables the A register to the adder (ATA), the sum enable right (SER), and shift rB right (SBR). C12 and the 1-MC clock generate SSC which steps the shift counter to zero and gates the AU bus to rA (AUA). C12 is reset on the trailing edge of shift counter equals one (SCE1). During each microsecond that C12 is set, rA and rB are shifted right one bit position including the sign bits, with the low-order bits of rA shifted into the high-order bit positions of rB and the low-order bits of rB entered in the high-order bit positions of rA. If a one bit is shifted out of the position next to the sign of rA, the overflow indicator is set.

Enable next fetch (ENF) is generated at shift counter equals three (SCE3), and the next fetch is initiated on the trailing edge of SCE3. If a shift of 0, 1, or 2 bit positions is specified, ENF is generated at T12 time.

LONG LEFT ROTATE (LLR) OPN43

This instruction will treat the A and B registers as one and shift left the number of shifts indicated by the six low-order bits of the effective address (Figure 4-36).

SEN is generated at T11 time and gates the adder sum to the AU bus. During the last 0.6 μsec of T11, KTS loads the shift counter with the low order six bits on the AU bus. If there is an index bit in the instruction word, XTA is enabled during the forming of the effective address at T11 time and allows the address portion of the instruction word to be equal to the sum of rZ plus the specified index register. On the trailing edge of T12, the shift enable flip-flop (C12) is set if the shift counter is not equal to zero. C12 disables ZEN and XTA and at the same time enables the A register to the adder (ATA), the sum enable left (SEL), and shift rB left (SBL). C12 and the one megacycle clock generate SSC which steps the shift counter to zero and gates the AU bus to rA (AUA). C12 is reset on the trailing edge of shift counter equals one (SCE1). During each microsecond that C12 is set, rA and rB are shifted left one bit position including the sign bits with the high-order bits of rB shifted into the low-order bit position of rA and the high-order bits of rA entered in the low-order bit positions of rB.

Enable next fetch (ENF) is generated at shift counter equals three (SCE3), and the next fetch is initiated on the trailing edge of SCE3. If a shift of 0, 1, or 2 bit positions is specified, ENF is generated at T12 time.

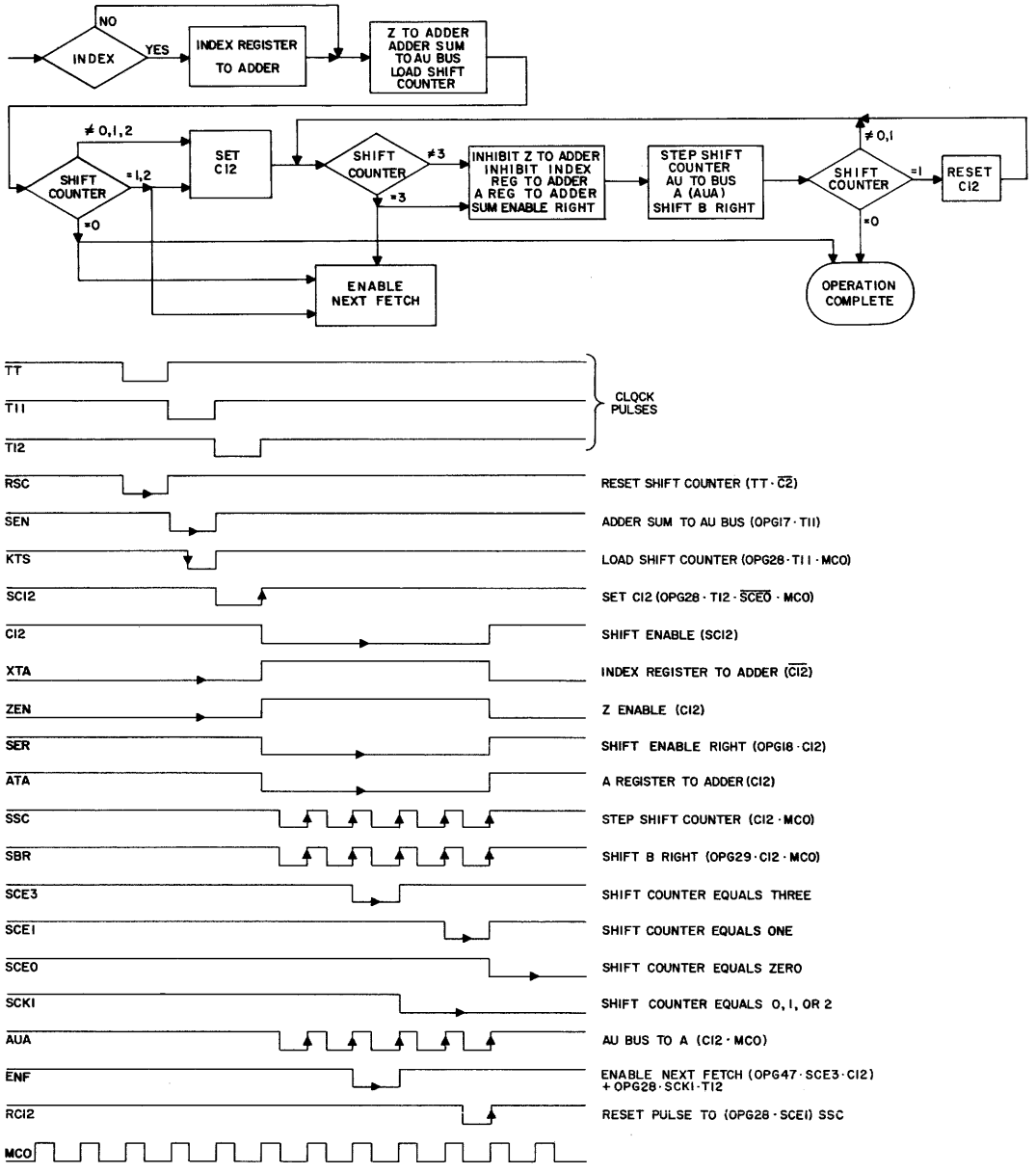


Figure 4-35. OPN 42 Long Right Rotate, Flow Chart and Timing Diagram

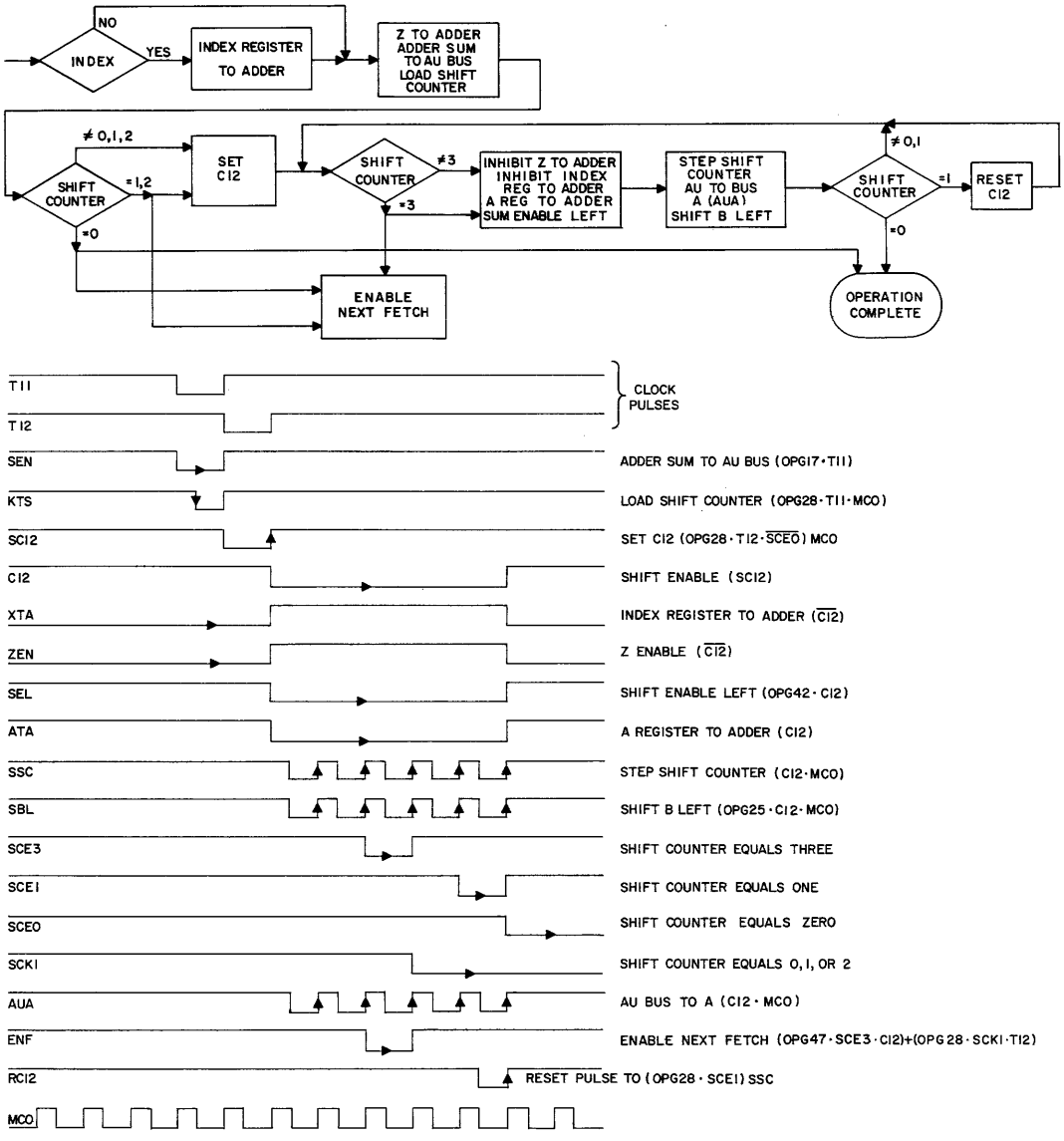


Figure 4-36. OPN 43 Long Left Rotate, Flow Chart and Timing Diagram

LONG RIGHT SHIFT (LRS) OPN44

This instruction will treat the A and B registers as one except for the sign bits and shift right the number of shifts indicated by the six low-order bits of the effective address (Figure 4-37).

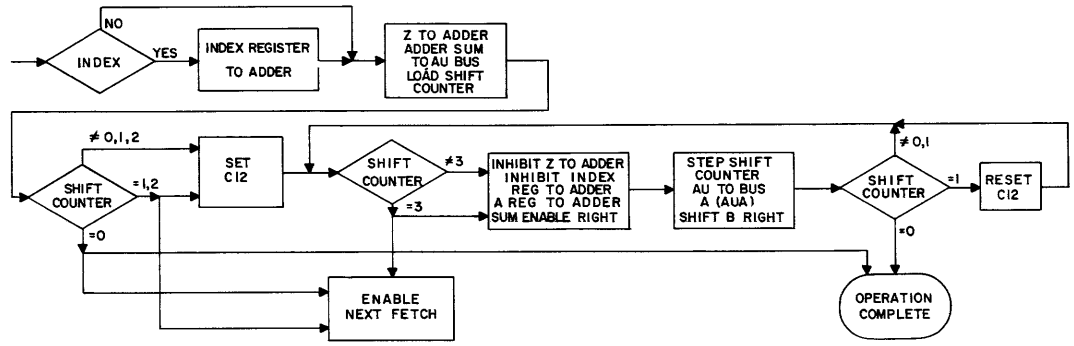
SEN, generated at T11 time, gates the adder sum onto the AU bus. During the last 0.6 μsec of T11, KTS loads the shift counter with the low-order six bits on the AU bus. If there is an index bit in the instruction word, XTA is enabled during the forming of the effective address at T11 time and allows the address portion of the instruction word to be equal to the sum of rZ plus the specified index register. On the trailing edge of T12, the shift enable flip-flop (C12) is set if the shift counter is not equal to zero. C12 disables ZEN and XTA and at the same time enables the A register to the adder (ATA), the sum enable right (SER), and shift rB right (SBR). C12 and the 1-MC clock generate SSC which steps the shift counter to zero and gates the AU bus to rA (AUA). C12 is reset on the trailing edge of shift counter equals one (SCE1). During each microsecond that C12 is set, rA and rB are shifted right one bit position except for the sign bits. The low-order bit of rA will be shifted into the high-order bit position of rB next to the sign bit, bit 2, and the sign of rB will be made to agree with the sign of rA. Zeros will be inseted into the high-order end of rA next to the sign bit of rA, and the low-order bits of rB will be lost.

Enable next fetch (ENF) is generated at shift counter equals three (SCE3), and the next fetch is initiated on the trailing edge of SCE3. If a shift of 0, 1, or 2 bit positions is specified, ENF is generated at T12 time.

LONG LEFT SHIFT (LLS) OPN45

This instruction will treat the A and B registers as one except for the sign bits and shift left the number of shifts indicated by the six low-order bits of the effective address (Figure 4-38).

SEN is generated at T11 time and gates the adder sum to the AU bus. During the last 0.6 μsec of T11, KTS loads the shift counter with the low-order six bits on the AU bus. If there is an index bit in the instruction word, XTA is enabled during the forming of the effective address at T11 time and allows the address portion of the instruction word to be equal to the sum of rZ plus the specified index register. On the trailing edge of T12, the shift enable flip-flop (C12) is set if the shift counter is not equal to zero. C12 simultaneously disables ZEN and XTA and enables the A register to the adder (ATA), sum enable left (SEL), and shift rB left (SBL). C12 and the 1-MC clock generate SSC which steps the shift counter to zero and gates the AU bus to rA (AUA). C12 is reset on the trailing edge of shift counter equals one (SCE1). During each microsecond that C12 is set, rA and rB are shifted left one bit position except for the sign bits. The high-order bit of rB next to the sign bit, is shifted into the low-order position, bit 24, of rA and the sign of rA is made



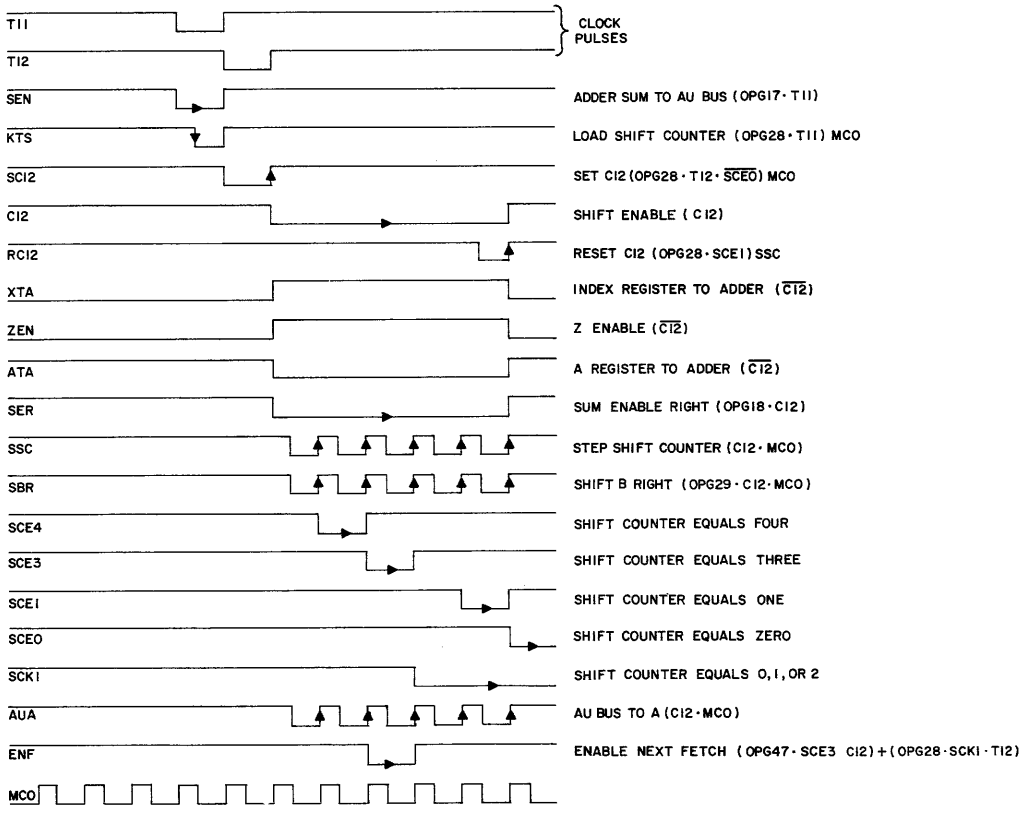
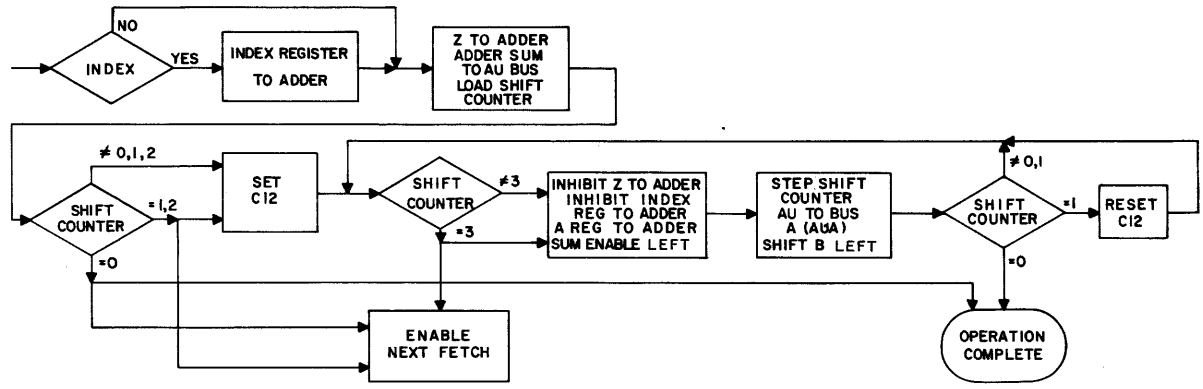


Figure 4-37. OPN 44 Long Right Shift, Flow Chart and Timing Diagram



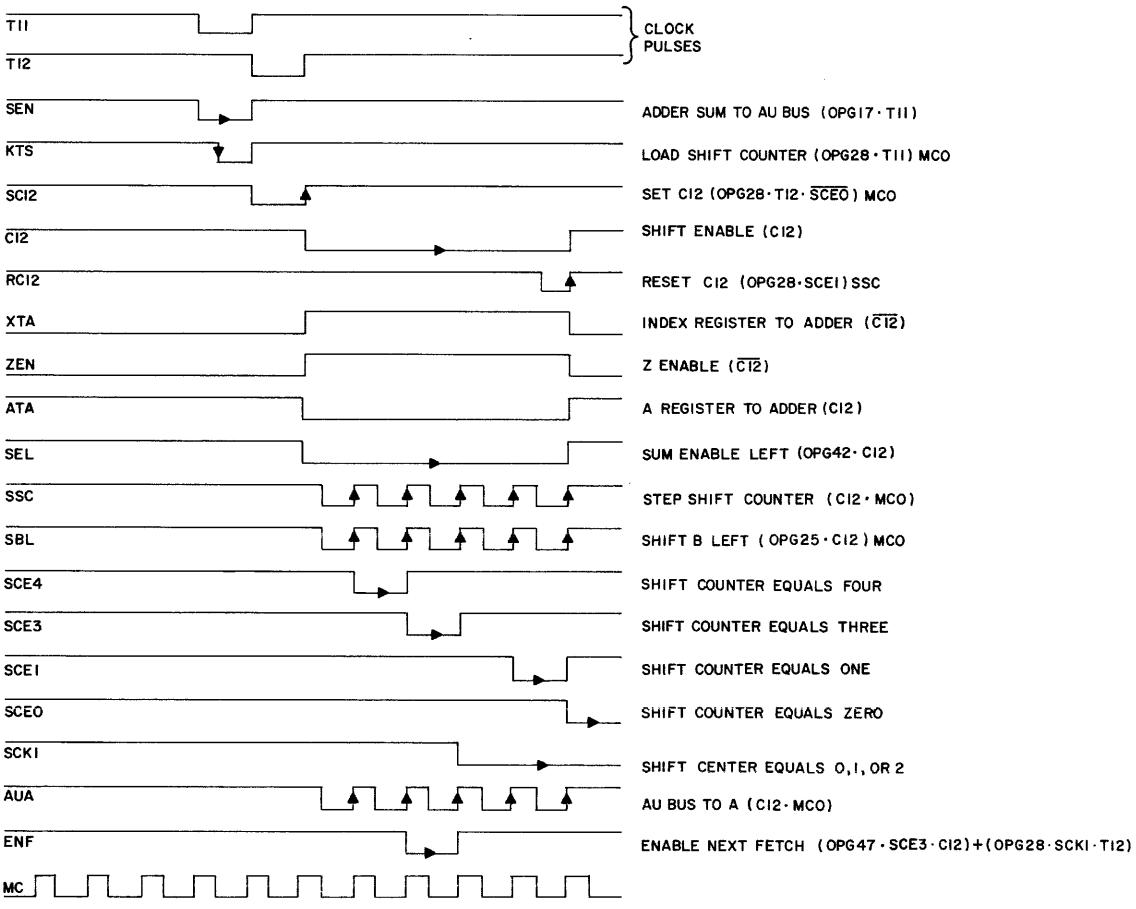


Figure 4-38. OPN 45 Long Left Shift, Flow Chart and Timing Diagram

to agree with the sign of rB. Zeros are inserted into the low-order bit position of rB and the high-order bits of rA are lost.

Enable next fetch (ENF) is generated at shift counter equals three (SCE3), and the next fetch is initiated on the trailing edge of SCE3. If a shift of 0, 1, or 2 bit positions are specified ENF is generated at T12 time.

NORMALIZE (NRM) OPN46

This instruction will treat the A and B registers as one except for the sign bits, and will shift them both left until a one bit is shifted into the position next to the sign of rA (A2), or until the low-order bit of register rB (B24) shifts into the high-order bit of register A (A2). If there is an index bit in the instruction word, the number of shifts required to normalize is subtracted from the index register (Figure 4-39).

At TT time the shift counter is cleared to all ONEs (RSC) and the shift enable flip-flop C12 is set if A2 is false (0 bit). The transition from TT to T11 is delayed until the shift operation is finished and C12 is reset. C12 being set disables ZEN and XTA, enables the A register to the adder (ATA), and sum enable left (SEL). C12 AND-gated with MCO clock pulses gate the AU bus to the A register (AUA), generate shift register B left (SBL), and decrements the shift counter (SSC). This shift cycle repeats at each clock pulse until C12 is reset by a one bit being shifted into A2 or the shift count equals a 46 (SCL) which indicates that there were no one bits in the A or B register. (B24 has been shifted through to A2).

Similar logic which resets C12 enables the clock to enter T11 time. T11 will reset rZ and will enable the loading of register Z (KTZ) with the effective complement (to subtract) of the shift count in the 6 least significant bit position of rZ. T12 will insert an end-carry pulse (IEC-5) to the adder (for correction) and will generate a sum enable (SEN) to the AU bus. Since C12 is now reset, ZEN and XTA (if indexed) have enabled register Z and the index register as inputs to the adder. During the last 0.6 μsec of T12, AUX enables the AU bus to the specified index register, which now contains the difference between the shift count and the initial setting of the index register.

T02 will enable next fetch (ENF).

LOGICAL LEFT SHIFT (LGL) OPN47

This instruction will shift rA, including the sign bit to the left, the specified number of shifts indicated by the six low-order bits of the effective address (Figure 4-40).

SEN is generated at T11 time and gates the adder sum onto the AU bus. During the last 0.6 μsec of T11, KTS loads the shift counter with the low-order six bits on the AU bus. If there is an index bit in the instruction word, XTA is enabled during the forming of the effective address at T11 time and allows the address portion of the instruction word to be equal to the sum of rZ plus the specified index register. On the trailing edge of T12,

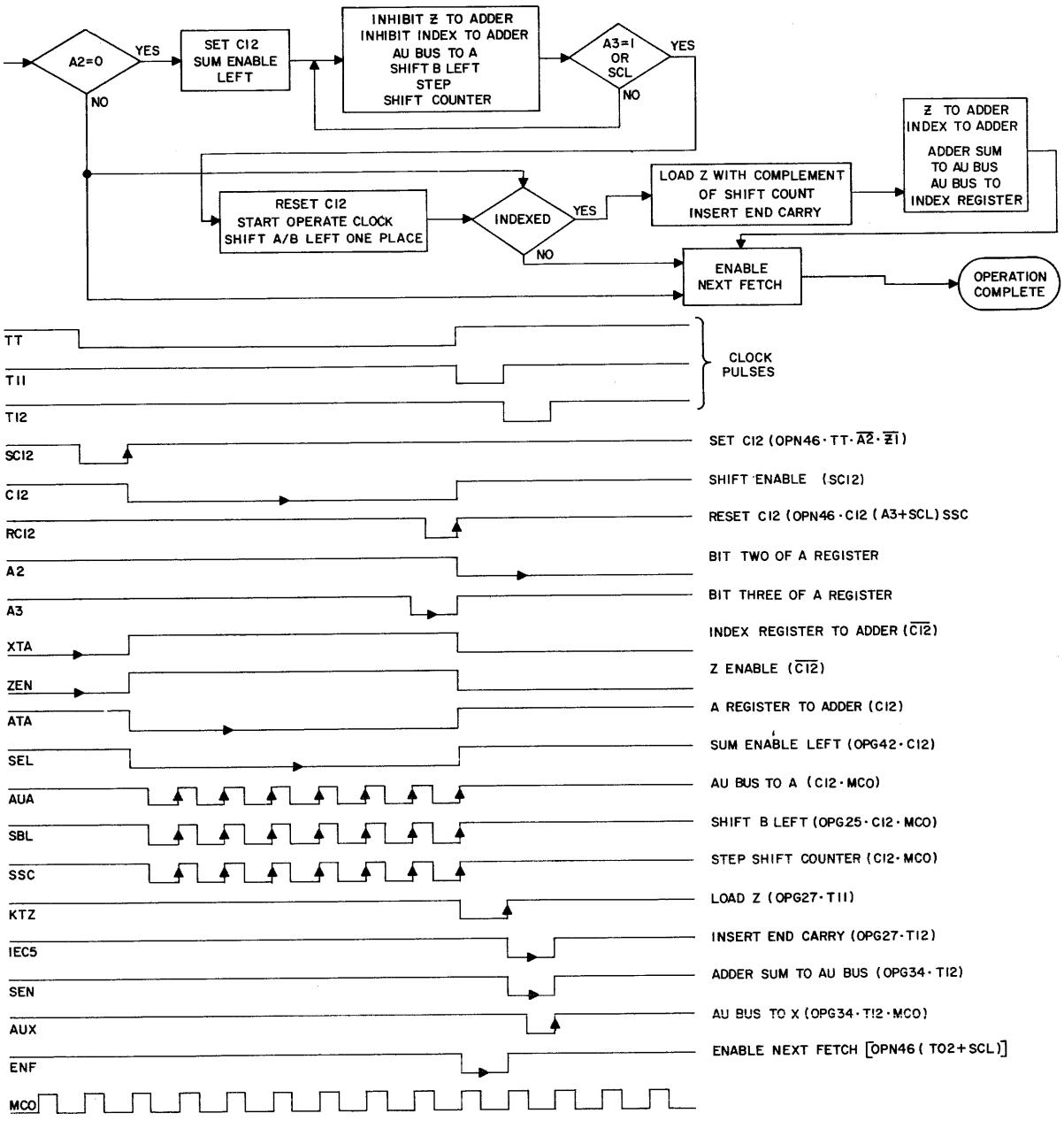


Figure 4-39. OPN 46 Normalize, Flow Chart and Timing Diagram

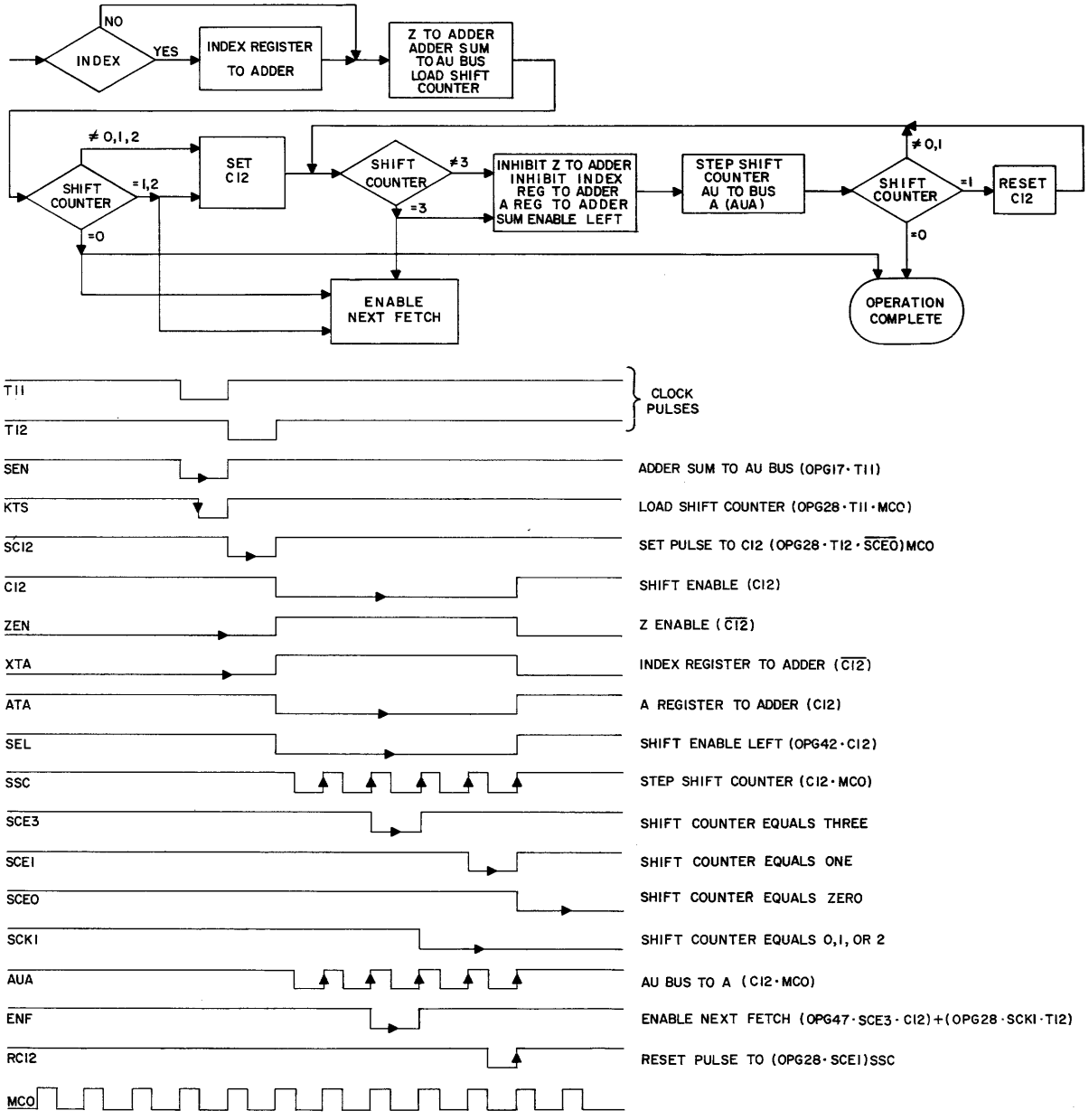


Figure 4-40. OPN 47 Logical Left Shift, Flow Chart and Timing Diagram

the shift enable flip-flop (C12) is set if the shift counter is not equal to zero. C12 simultaneously disables ZEN and XTA and enables the A register to the adder (ATA), sum enable left (SEL). C12 and the 1-MC clock generates SSC which steps the shift counter to zero and gates the AU bus to rA (AUA). C12 is reset on the trailing edge of shift counter equals one (SCE1). During each microsecond that C12 is set, rA is shifted left one bit position. Zeros are inserted into the low-order end of rA bit 24, and the high-order bits are lost as they are shifted out.

Enable next fetch (ENF) is generated at shift counter equals three (SCE3) and the next fetch is initiated on the trailing edge of SCE3. If a shift of 0, 1, or 2 bit positions is specified, ENF is generated at T12 time.

OUTPUT FROM rA (OTA) OPN50

OTA is performed by executing one transfer with the transfer bus. This transfers the contents of A register to the output transfer bus if bit 10 (Z10) of the instruction is a zero (24-bit word transfer), and transfers A19-24· Z19-24 to the output if bit 10 (Z10) is a one (6-bit mask) (Figure 4-41).

The transition from fetch to the operate cycle is a function of the input-output ready flip-flop (C4). C4, a synchronizing flip-flop, is set at the beginning of a clock cycle after the asynchronous input-output ready line (IOR) becomes true. One microsecond after C4 is set, the operate clock starts. OPG-45 and TT generate the enable next fetch (ENF) pulse which will start the next fetch cycle.

ATT is a 2-μsec pulse, generated during T21 time, which will transfer the contents of rA to the transfer bus. If bit 10 of the instruction was a one, ZTT (Z to the transfer bus) will also be generated and the output of the transfer bus will be the Boolean product of Z and A at T21 time.

At T12 time, the reset ready synchronizer pulse (RRS) is generated and the leading edge of this pulse resets IOR; 1-μsec later C4 resets. The output transfer bus is selected as the transfer bus destination by TTO which is generated during T12 time.

INTERRUPT CONTROL (ITC) OPN51

The operate portion of this instruction generates a 1-μsec pulse which is used to set or reset an interrupt enable flip-flop in the input-output section of the computer. Bit 10 (Z10) of this instruction must contain a one bit to enable interrupt (Figure 4-42).

At TT time, an enable next fetch pulse (ENF) is generated to start the next fetch cycle. The operate cycle (1-μsec long) generates a 1-μsec pulse T11. At T11 time, the interrupt control pulse (ITC) is generated.

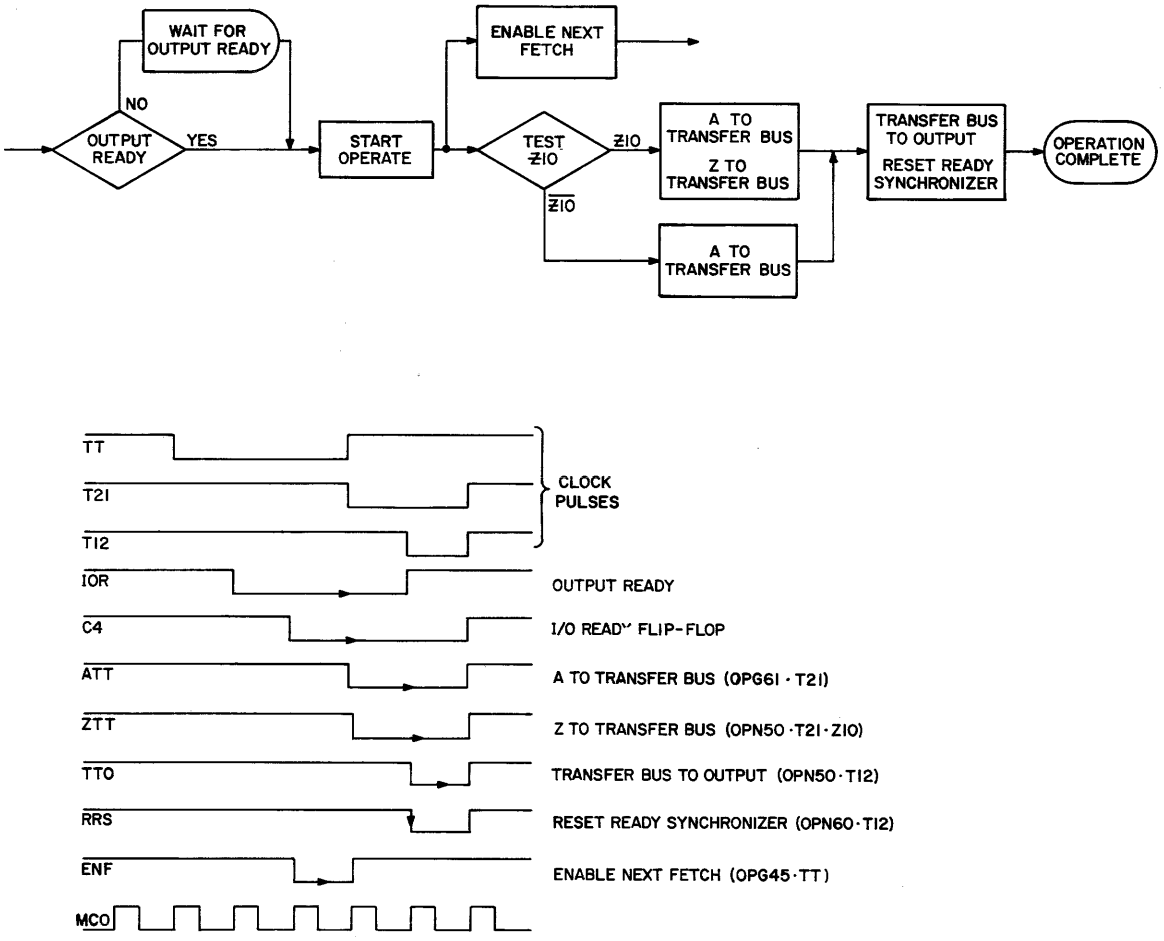


Figure 4-41. OPN 50 Output from rA, Flow Chart and Timing Diagram

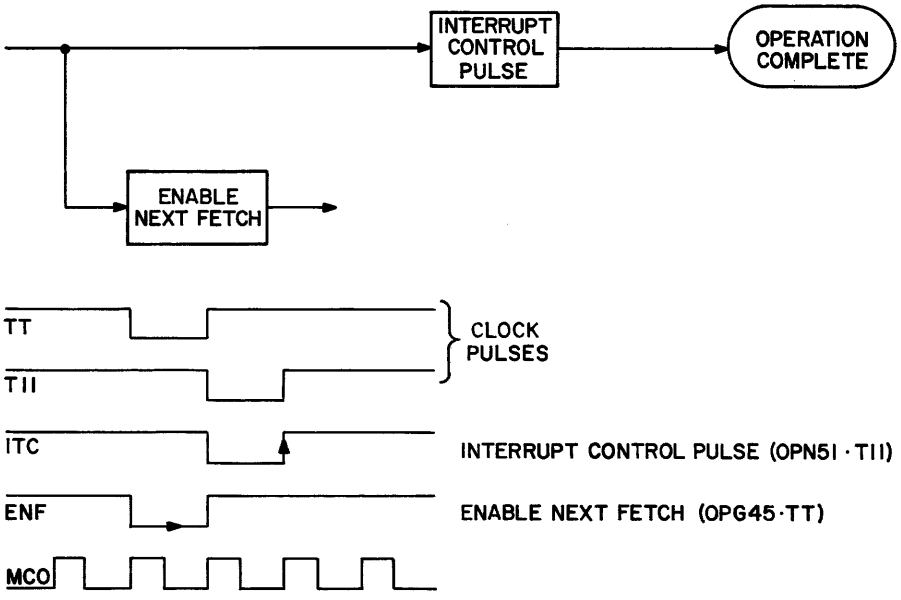


Figure 4-42. OPN 51 Interrupt Control, Flow Chart and Timing Diagram

STORE INPUT IN rA (INA) OPN52

INA is performed by executing three transfers; two involve the transfer bus and one uses the AU bus. These transfers are the input bus to the transfer bus and the transfer bus to the AU bus. The transfer of the AU bus into the A register is a 24-bit transfer of the input information if bit 10 (Z10) of the instruction is a zero. If bit 10 (Z10) is a one, IXB19-24 is transferred into A19-24 according to the 6-bit mask in bits 19-24 of the Z register (Figure 4-43).

The transition from fetch to the operate cycle is a function of the input-output ready flip-flop (C4). C4 is a synchronizing flip-flop which is set at the beginning of a clock cycle after the asynchronous input ready pulse (IOR) occurs. One microsecond after C4 is set, the operate clock starts. C4 will generate the enable next fetch (ENF) pulse which will start the next fetch cycle.

ITT is a 2-μsec pulse generated during T21 time which will transfer the input bus to the transfer bus. TTA is a 1-μsec pulse which transfers the transfer bus to the AU bus and is generated during T12 time. Also during T12 time, a reset ready synchronizer pulse (RRS) is generated, the leading edge of which resets IOR. One microsecond later, C4 resets.

If bit 10 of the Z register is zero, bits 1-18 of the A register are selected as the AU bus destination by AUA and AUA-2 which are generated during the last 0.6 μsec of TTA. The remaining bits of rA (19-24) have as their gating pulses AUA-S and AUA + FTA if Z10 is true. If bit 10 (Z10) is a ONE, AUA and AUA-2 are inhibited. MTA is generated instead to strobe in bits 19-24 of the A-reg. The MTA strobe is AND-gated with its Z-register negation bit to strobe the A-register so that if the Z register bit is zero, the strobe is inhibited and if ONE, the strobe is generated.

OUTPUT CONTROL PULSE (OCP) OPN53

The OCP operations are described in the input-output section of the manual. From a control unit point of view, all that is required is the generation of a 2-μsec pulse to be used by the input-output to perform various functions. The function performed depends on the address field of the instruction word which is stored in rZ during the performance of this instruction (Figure 4-44).

At TT time an enable next fetch pulse (ENF) is generated to start a new fetch cycle. The operate cycle (2 μsec long) generates a 2-μsec pulse (T21) which produces the output control pulse (OCP).

ADD ADDRESS PORTION OF COMMAND TO THE INDEX REGISTER (ADX) OPN54

For this instruction, the index register is the augend while the address field of rZ is the addend. The adder determines the sum and this sum replaces the value originally in the index register (Figure 4-45).

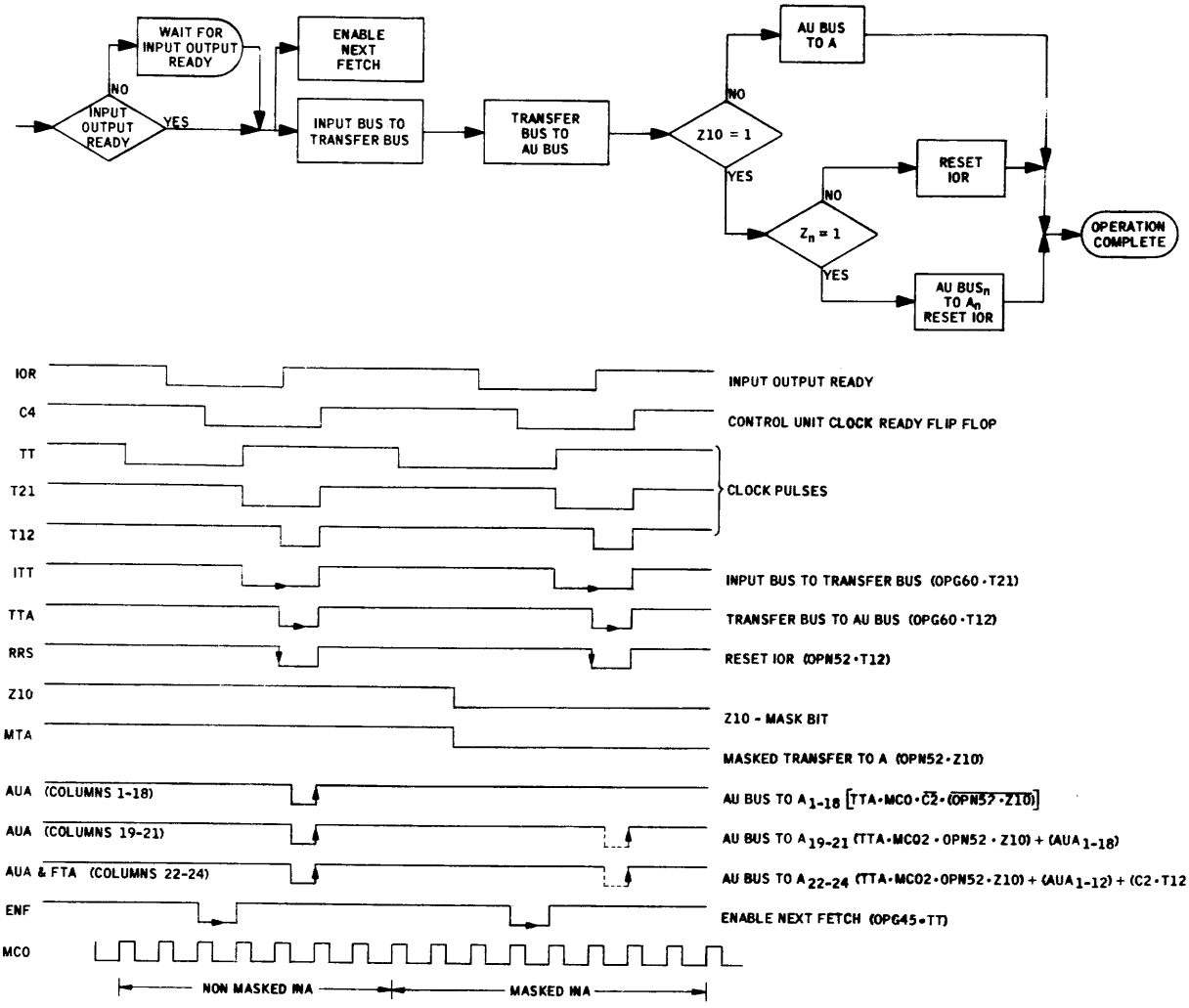


Figure 4-43. OPN 52 Store Input in A

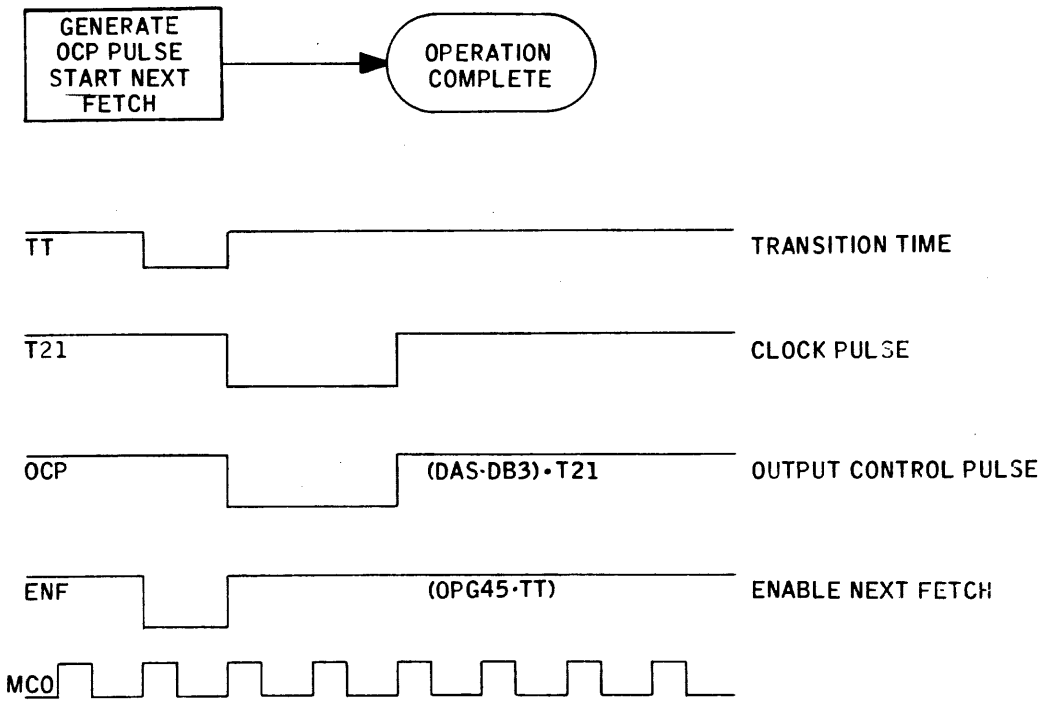


Figure 4-44. OPN 53 Output Control Pulse

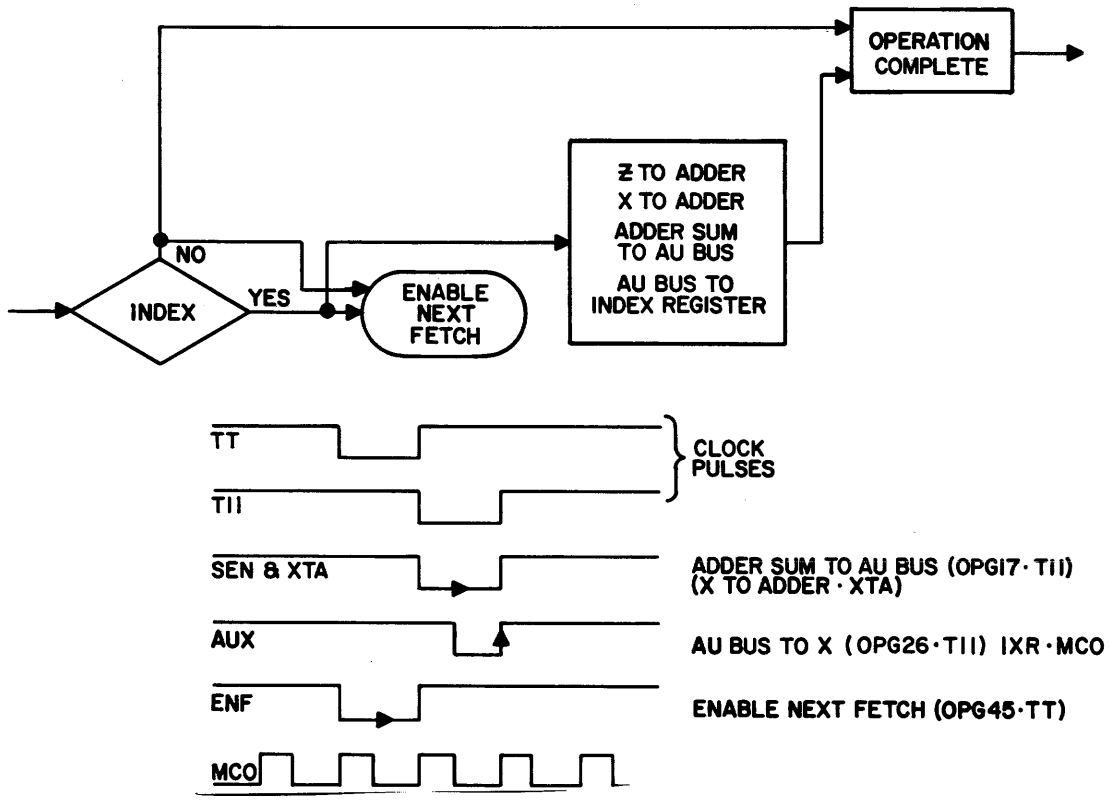


Figure 4-45. OPN 54 Add Address Portion of Command to the Index Register, Flow Chart and Timing Diagram

At TT time an enable next fetch pulse (ENF) is generated to start a new fetch cycle. The operate cycle (1 μsec long) generates a T11 pulse. SEN, generated during T11, gates the sum output of the adder to the AU bus. AUX, a pulse also generated during T11 time, transfers the low-order 15 bits of the AU bus into the index register. While the adder is enabled by ZEN and XTA for this sum, the end-around-carry is disabled to prevent a carry generated by the high-order columns from disturbing the low-order bits.

TRANSFER A TO B (TAB) OPN55

In this instruction the contents of the A register are transferred to the B register and the A register remains unchanged (Figure 4-46).

During TT time, an enable next fetch pulse (ENF) is produced and the operate cycle is entered at the trailing edge of TT. ATT, a 2-μsec pulse produced by T21, transfers the A register to the transfer bus. REB, a pulse produced at T11 time, resets the B register. TTB, a 1-μsec pulse produced at T12 time, transfers the transfer bus into the B register.

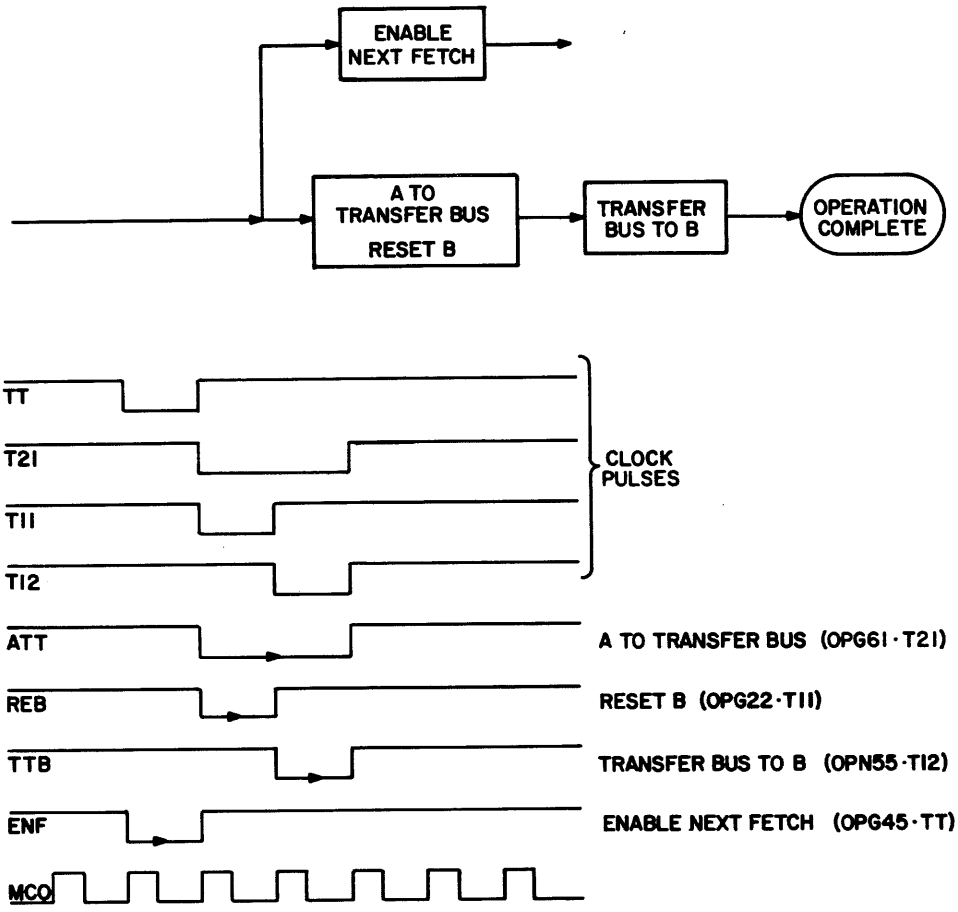


Figure 4-46. OPN 55 Transfer A to B, Flow Chart and Timing Diagram

LOAD INDEX REGISTER (LDX) OPN56

LDX is performed by adding the address field of rZ to zero and transferring the result into the index register (Figure 4-47).

During TT time, an enable next fetch pulse (ENF) is produced and the operate cycle is entered. During T12 time, the XTA signal is inhibited. Therefore, the only input to the adder is the Z register. SEN, produced during T12, enables the sum output of the adder to the AU bus. At this time the AU bus is transferred into the specified index register by AUX. The end-around-carry is disabled for this instruction.

INTERCHANGE A AND B (IAB) OPN57

In this instruction the contents of the A and B registers are interchanged (Figure 4-48).

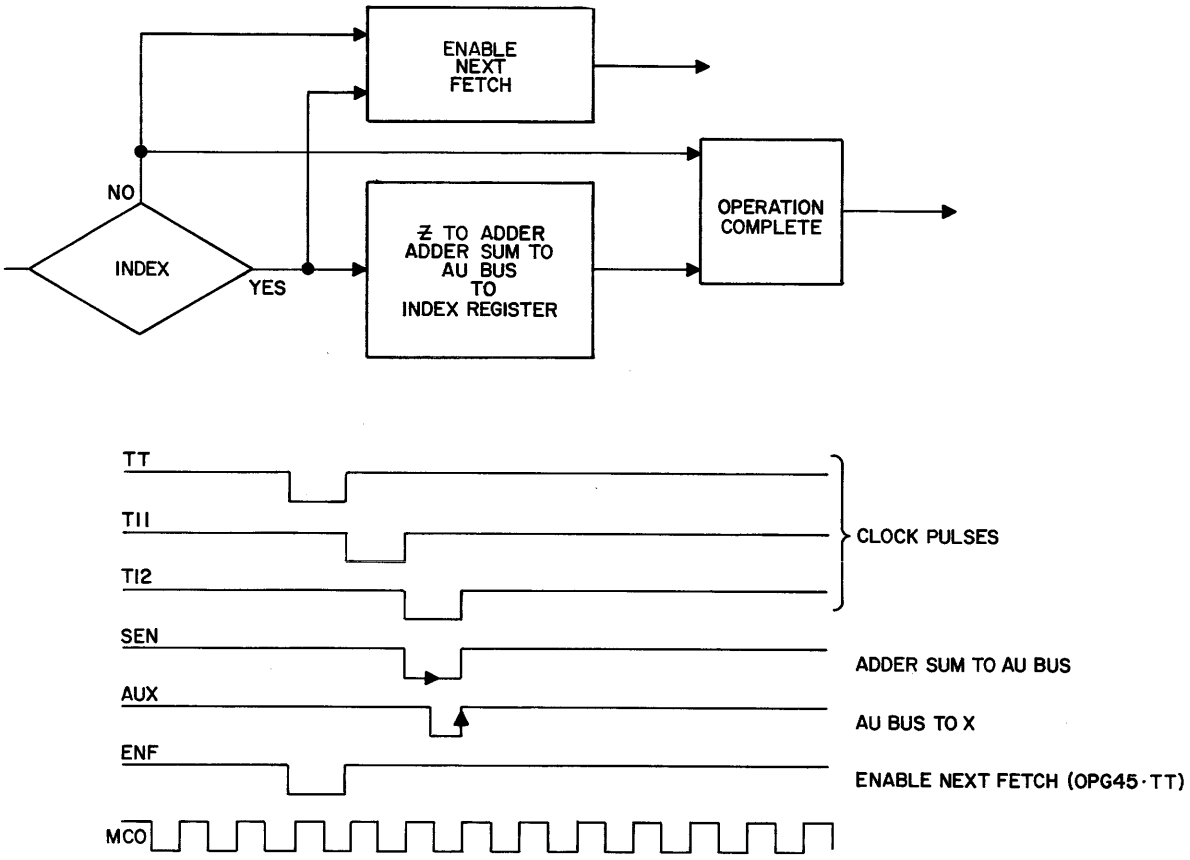


Figure 4-47. OPN 56 Load Index Register, Flow Chart and Timing Diagram

The operate cycle is entered and during T11, an REZ pulse resets the Z register. The A register is transferred to the transfer bus during T21 by the pulse ATT; during T12, a TTZ pulse gates the transfer bus into Z.

During T23 a BTT pulse transfers the B register into the transfer bus. During T14, a TTA pulse gates the transfer bus to the A register. AUA is generated by TTA and a clock pulse is used to gate the information into the A register. During T25 time, the Z register is transferred to the transfer bus by ZTT; during T15 time, an REB pulse resets the B register, and during T16 time, a TTB pulse gates the transfer bus into the B register.

During T15 time, an ENF pulse will start the next fetch cycle.

CLEAR A REGISTER (CRA) OPN60

CRA is performed by producing a 1 μsec pulse to reset the contents of the A register (Figure 4-49).

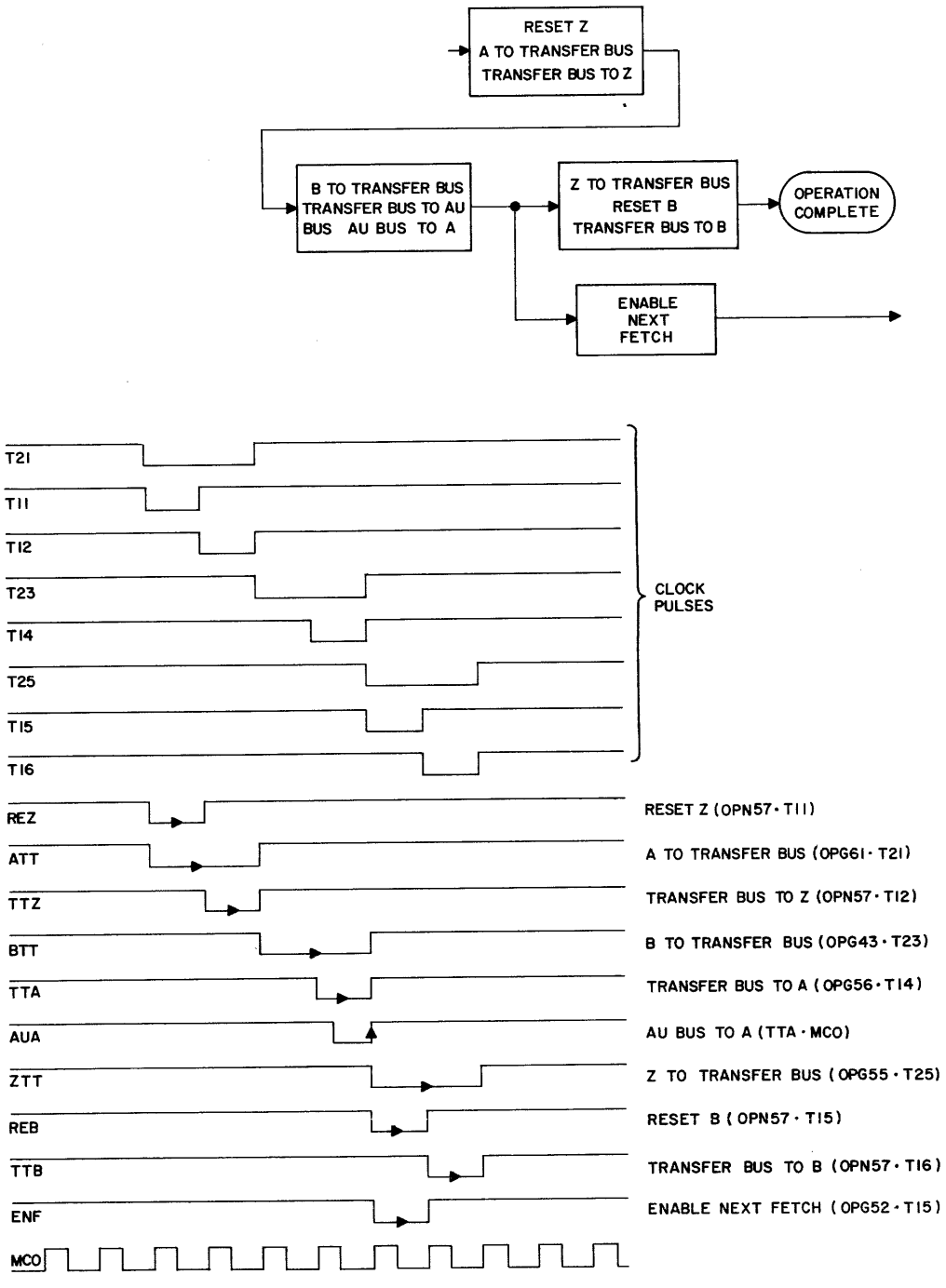


Figure 4-48. OPN 57 Interchange A and B, Flow Chart and Timing Diagram

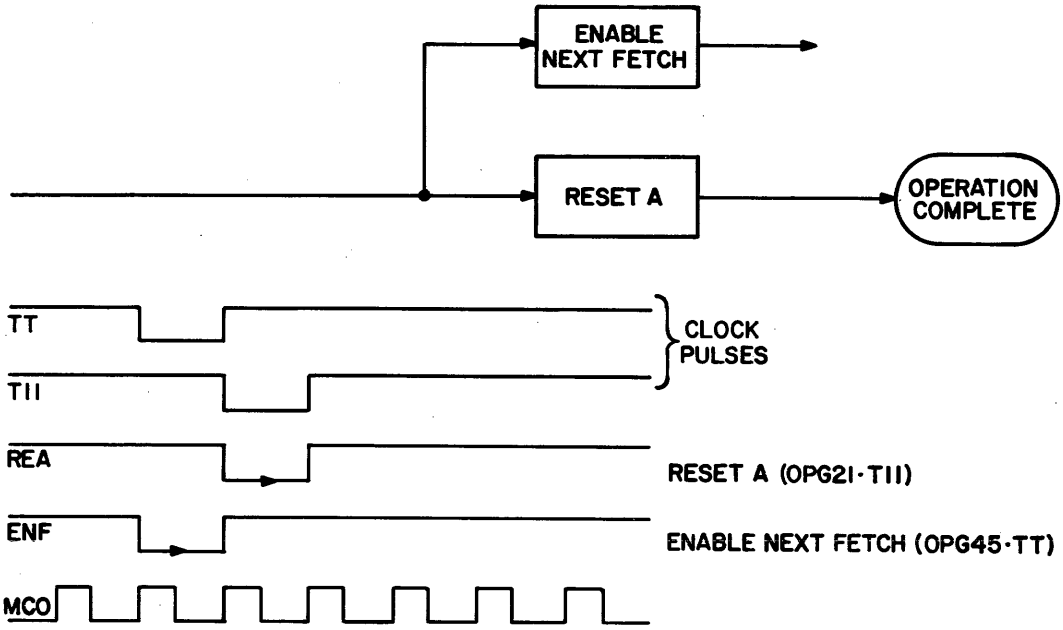


Figure 4-49. OPN 60 Clear A Register, Flow Chart and Timing Diagram

At TT time and enable next fetch is produced and the operate cycle is entered at the trailing edge of TT. At time T11, an REA signal is produced to reset the contents of the A register.

SKIP IF SENSE LINE NOT SET (SKS) OPN61

The SKS instruction selectively tests certain internal and external functions. If these functions are not equal to a logic one, an extra count is given to the program counter (P). The selection of functions to be tested is under control of the address field of the instruction word. When tested, certain functions (such as the overflow flip-flop) are reset if the instruction word contains a one in bit 10 (Z10) (Figure 4-50).

At TT time, an enable next fetch pulse is produced and the operate cycle will be entered at the trailing edge of TT. At T11 time, the selected functions are tested. If any one of the chosen functions is not set, the 0.6-μsec pulse, SPC, generated during T11 time, will step the program counter. If set when they are tested, certain functions are reset at T12 time by the 0.6-μsec pulse RTI(n) if the instruction has a one in bit 10 (Z10). Three RTI pulses are provided: RTI-1 is active during successful tests when the address field is (0XXXX)8; RTI-2 is active during successful tests when the address field is (2000X)8; and RTI-3 is active during successful tests when the address field is (3000X)8.

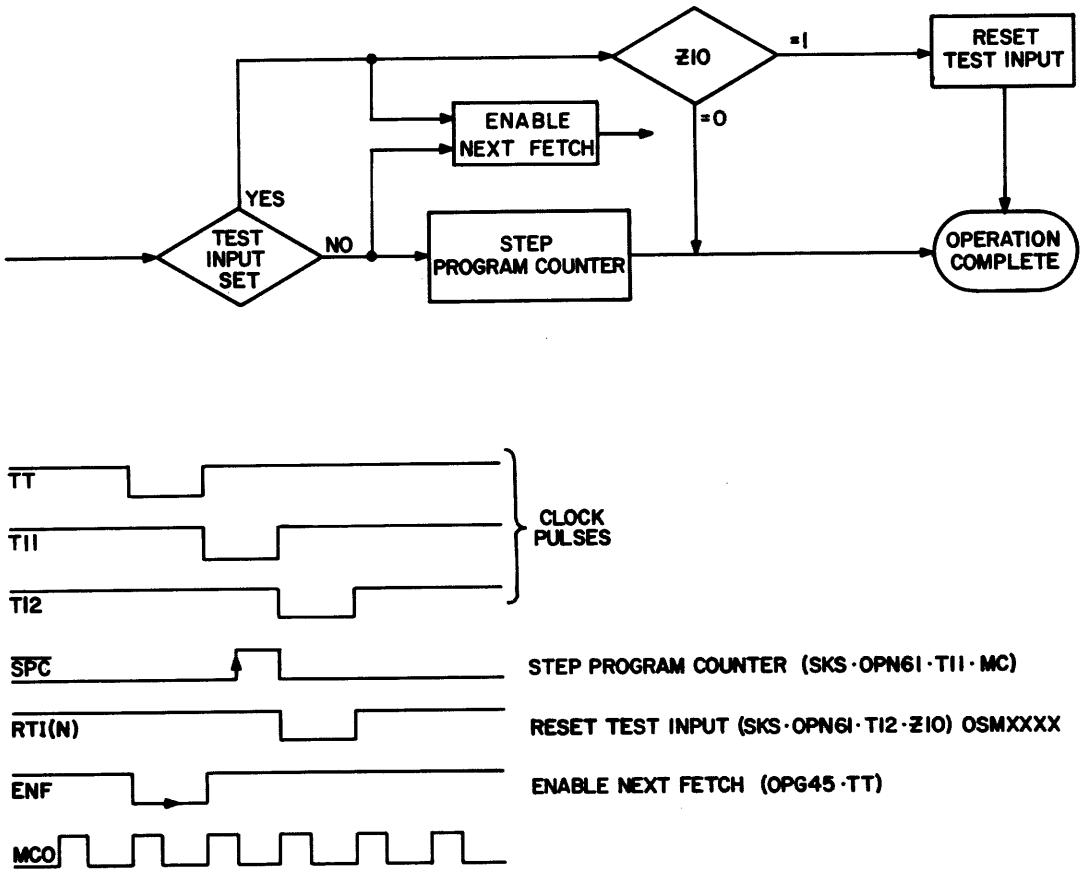


Figure 4-50. OPN 61 Skip if Sense Line not Set, Flow Chart and Timing Diagram

ROUND rA (RND) OPN62

The RND instruction increments the contents of rA by one if bit 2 in the B register is a one; the contents of rA are unchanged if this bit is zero. At TT time, an enable next fetch (ENF) pulse is generated and the operate cycle is entered at the trailing edge of TT (Figure 4-51).

The XTA signal (which enables the index register as an input to the adder) and the ZEN signal (which enables the Z register as an input to the adder) are inhibited during T11. XTA is inhibited by the ATA signal which enables the A register as an input to the adder. If bit 2 of the B register is a one, three signals are produced during T11 time. IEC7 inserts an end-carry bit into the first stage of the adder. SEN enables the sum of the adder to the AU bus; and AUA (a 0.6-μsec pulse) transfers the contents of the AU bus into the A register.

During this summation, the end-around-carry of the adder is disabled. A high-order carry output sets overflow flip-flop C17.

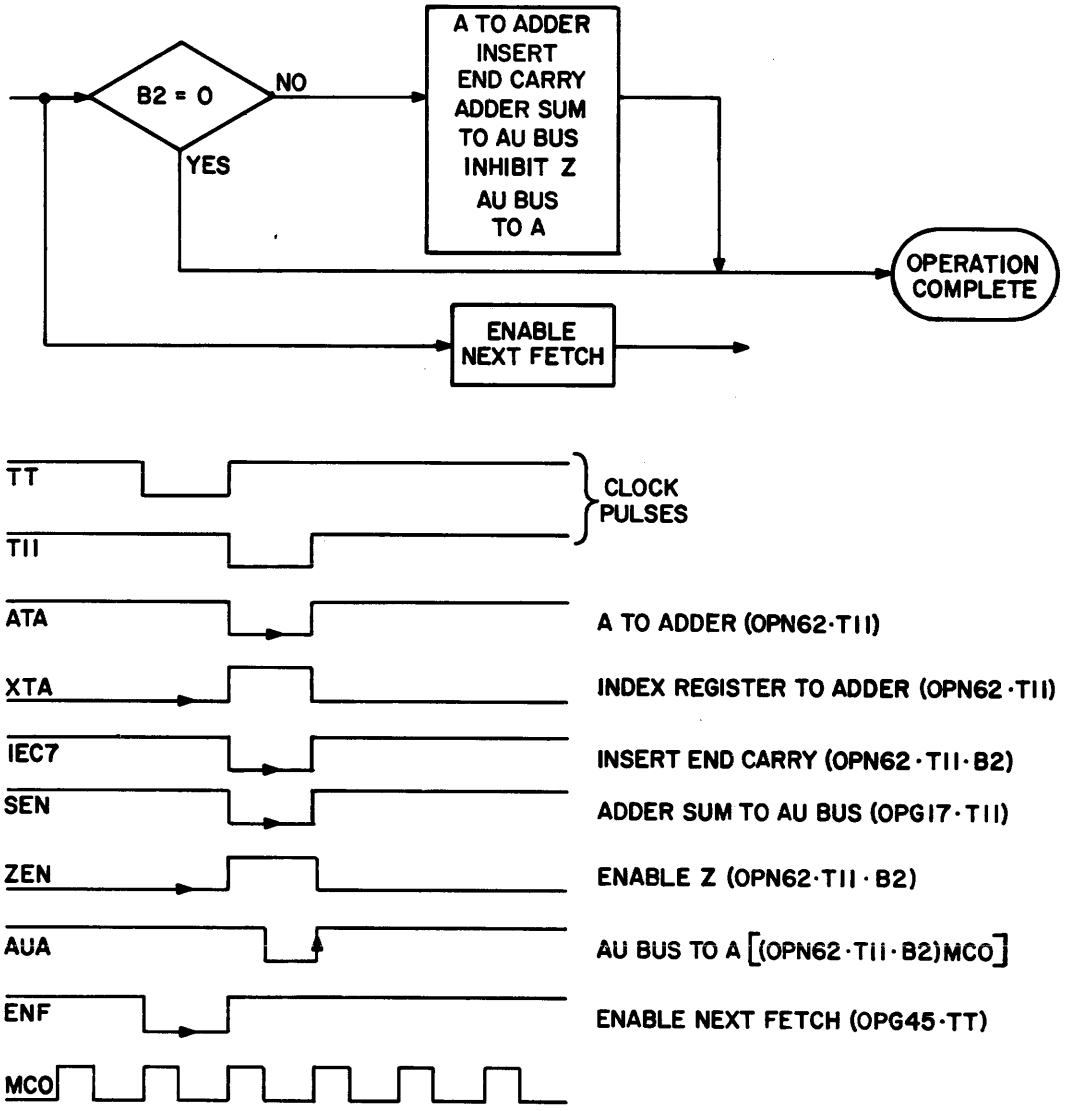


Figure 4-51. OPN 62 Round rA, Flow Chart and Timing Diagram

TRANSFER A TO THE INDEX REGISTER (TAX) OPN63

TAX is performed by adding the address field of rA to zero and transferring the result into the index register (Figure 4-52).

During TT, an enable next fetch signal (ENF) is produced and the operate cycle is entered at the trailing edge of TT. ATA (which selects A as an input to the adder during T12) inhibits the XTA signal, thereby blocking the index register as an input to the adder. The ZEN signal (which enables the Z register to the adder) is also inhibited durint T12. SEN, produced during T12, enables the sum output of the adder to the AU bus. The end around carry is disabled for this instruction.

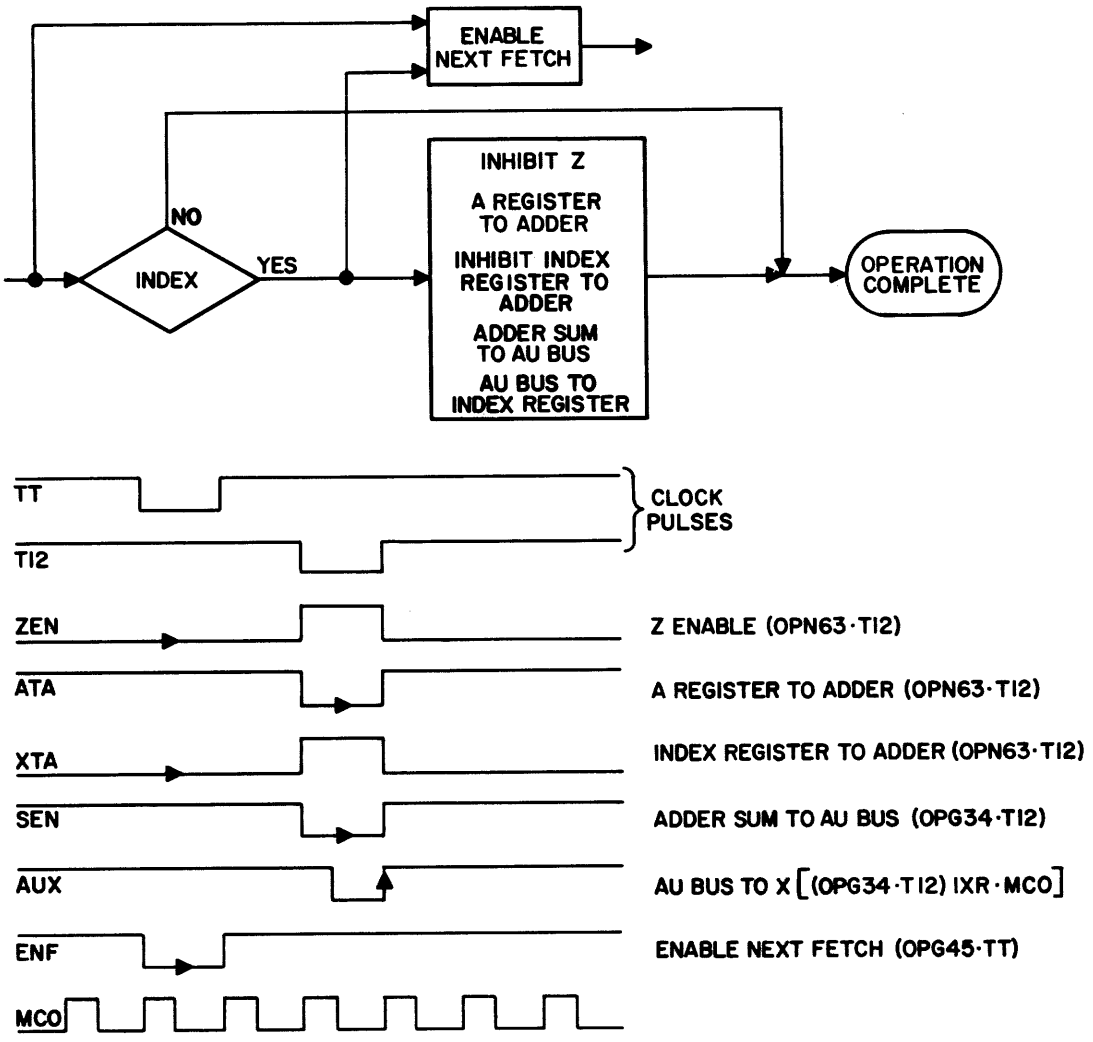


Figure 4-52. OPN 63 Transfer A to the Index Register, Flow Chart and Timing Diagram

At time T12 a 0.6-μsec pulse, AUX, transfers the 15 low-order bits of the AU bus into the index register.

SCALE RIGHT (SCR) OPN64

This command consists of three parts — loading the shift counter with the number specified by the six least significant bits of the command word; gating the Z register and the specified index register into the adder (the resulting sum then being transferred back into the index register), and shifting the A and B registers. (Note that after the second part of the command the shift counter has been loaded with the specified number of shift steps and the index register has been incremented by that number.) The A and B registers are shifted by setting C12 to generate a shift enable signal and gate shift lines to those

registers. If the number transferred into the shift counter is a zero, C12 will not be set, and therefore, no shifting will occur and the index register will not be modified (Figure 4-53).

The final phase of this command enabling the start of the next fetch cycle is accomplished by monitoring the count in the shift counter. For a scale right command involving a shift number of three or more, the next fetch is enabled when the shift counter reaches three. For a command of less than three, the next fetch is enabled when the shift counter reaches one, two, or three. For the special case of a shift of zero, the next fetch is enabled when the shift counter number equals zero.

SEN enables the sum output of the adder to the AU bus during T11. The sum being enabled (rZ plus zero, or rZ plus the number of steps to be shifted) is dropped into the shift counter by KTS which occurs during T11 time.

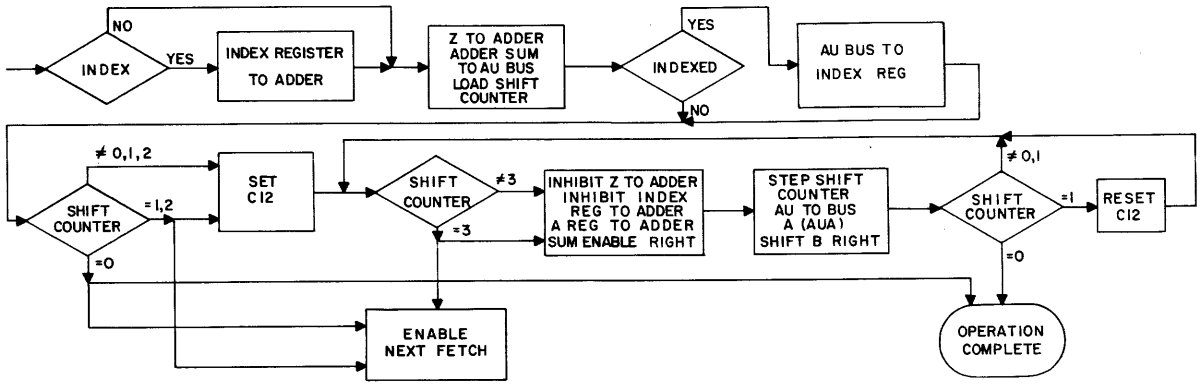
SEN again enables the sum output of the adder to the AU bus during T12 time. The Z register enable to the adder (ZEN) and the index register enable to the adder (XTA) are also true at this time if the instruction has been indexed. Since rZ contains the quantity originally transferred to the shift counter, its contents are now added to the contents of the index register. AUX then gates the AU bus into the appropriate index register.

Shift control flip-flop C12 is set at the end of T12 time if the contents of the shift counter are not equal to 0 (SCE-0). C12 simultaneously disables ZEN and XTA and enables the A register to the adder (ATA), the sum enable right (SER), and the shift rB right (SBR). C12 and the 1-MC clock generate SSC which steps the shift counter to 0 and gates the AU bus to rA (AUA). C12 is reset when the shift counter equals 0. During each microsecond that C12 is set, the A and B registers are shifted right one bit position, except for the sign bits. The signs of A and B are not shifted. However, the sign of rB is made to agree with the sign of rA. Zeros are shifted into the vacated position next to the sign of rA, bit 2. Bits shifted out of the low-order position of rA enter the position next to the sign of rB, bit 2. Bits shifted out of the low-order position rB are lost. If no index register is specified, the SCR instruction appears as an LRS instruction.

Enable next fetch (ENF) is generated at shift counter equals three (SCE-3) and the next fetch is initiated on the trailing edge of SCE-3. If a shift of 0, 1, or 2 bit positions is specified, ENF is generated at T12 time.

SCALE LEFT (SCL) OPN65

This command consists of three parts. First, the shift counter is loaded with the number specified by the 6 least significant bits of the command word. The Z register address field is then complemented and gated into the adder along with the specified index register; the resulting sum is the difference between the existing number in the index register and the number of shifts specified by the instruction. Thus far, the command has loaded the shift counter with a specified number of shift steps and decreased the index



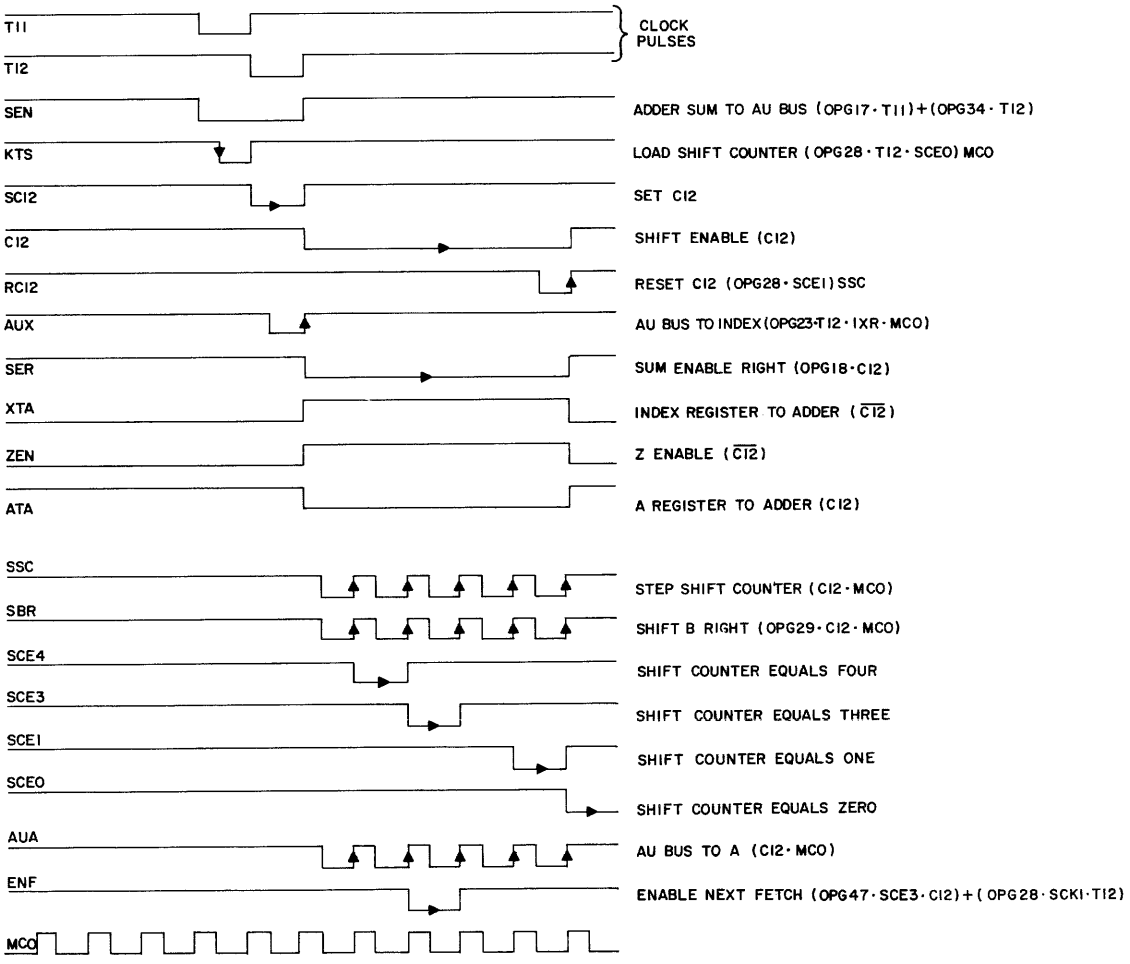


Figure 4-53. OPN 64 Scale Right, Flow Chart and Timing Diagram

register by that number. Having done these two parts the remaining function to be performed during scale left is the actual shifting of the A and B registers. This is accomplished by setting C12 to generate a shift enable signal and gate shift lines to the A and B registers. C12 will not be set if the number transferred into the shift counter is a zero. In this case, there is no shifting and the index register remains unmodified (Figure 4-54).

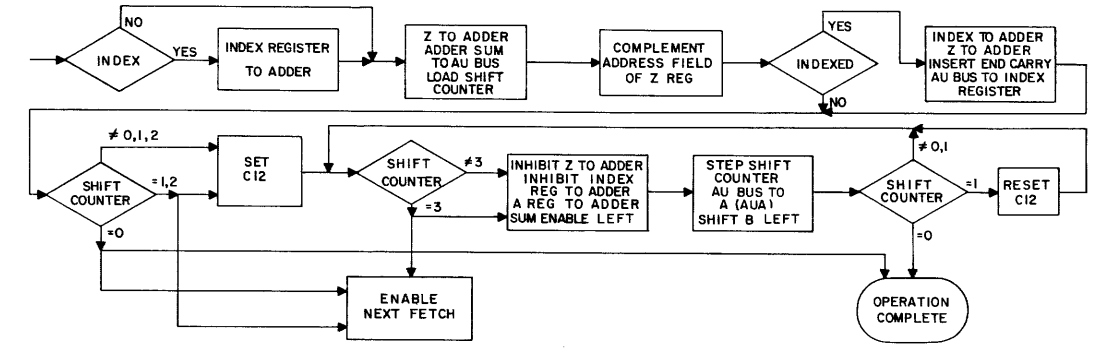
The final phase during the scale left instruction is that of enabling the start of the next fetch cycle by monitoring the count in the shift counter. For scale left instruction involving a shift number of three or more, the next fetch is enabled when the shift counter reaches a count of three. For an instruction in which the count is less than three, the next fetch is enabled when the shift counter equals 0, 1, or 2. For the shift of zero, the start of the next fetch is enabled when the shift counter equals zero.

SEN enables the sum output of the adder to the AU bus during T11. The enabled sum, rZ puls zero or rZ plus the number of steps to be shifted, is dropped into the shift counter by KTZ which occurs during T11 time. The Z register is also complemented during T11 by KTZ.

SEN again enables sum output of the adder to the AU bus during T12 time. The Z register enable (ZEN) and the index register enable (XTA) to the adder are also true at this time if the instruction has been indexed. Since rZ now contains the complement of the quantity originally transferred to the shift counter, its contents are now effectively subtracted from the contents of the index register. A correction factor (IEC-5) also occurs at this time to complete the subtraction process. AUX then gates the AU bus into the appropriate index register.

The shift control flip-flop (C12) will set at the end of T12 time if the contents of the shift counter are not equal to zero (SCE-0). C12 simultaneously disables ZEN and XTA and enables the A register to the adder (ATA), the sum enable left (SEL), and the shift B left (SBL). C12 and the 1-MC clock generate SSC which steps the shift counter to zero, and gates the AU bus to rA (AUA). C12 is reset when the shift counter equals zero. During each microsecond that C12 is set, registers A and B are shifted left one bit position except for the sign bits. The high-order bit of register B next to the sign bit (B2) is shifted into the low-order position, bit 24, of register A (A24) and the sign of rA is made to agree with the sign of rB. Zeros will be inserted into the low-order bit position of rB and the high-order bits of rA will be lost. If a one bit is shifted out of the position next to the sign of rA, the overflow indicator is set. If no index register is specified, the SCL appears as an LLS instruction.

Enable next fetch (ENF) is generated at shift counter equals 3 (SCE-3) and the next fetch is initiated on the trailing edge of SCE-3. If a shift of 0, 1, or 2 bit positions is specified ENF is generated at T12 time.



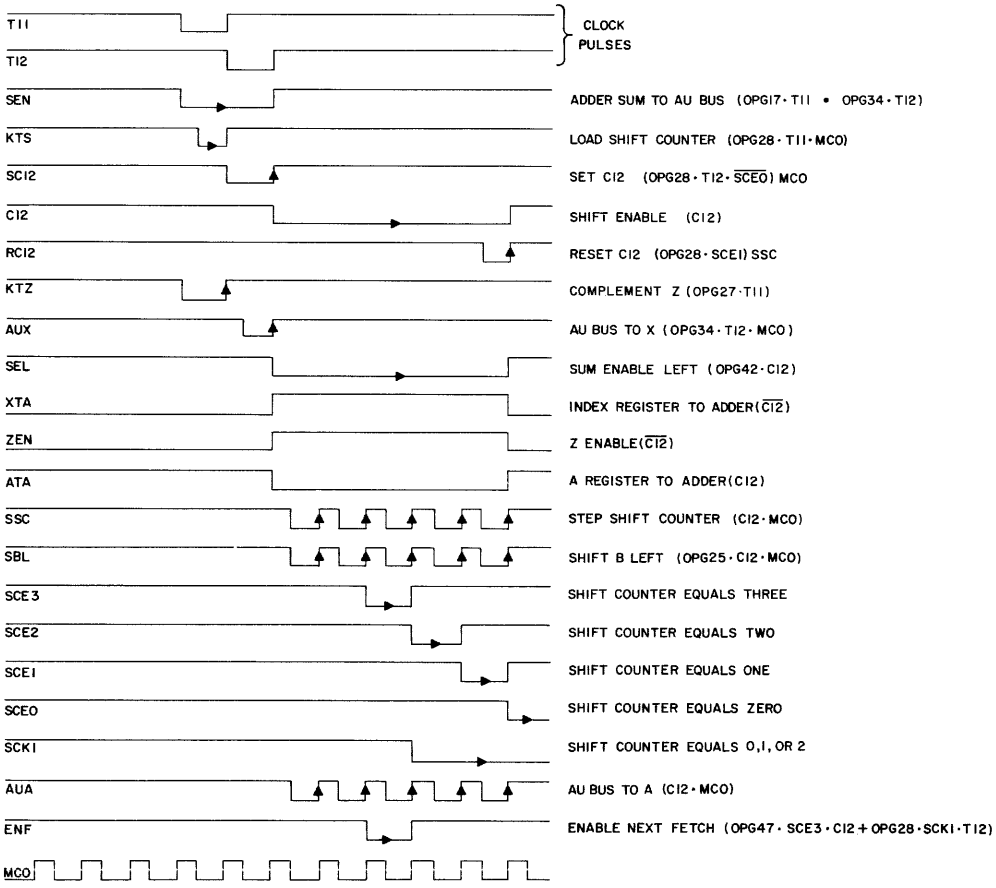


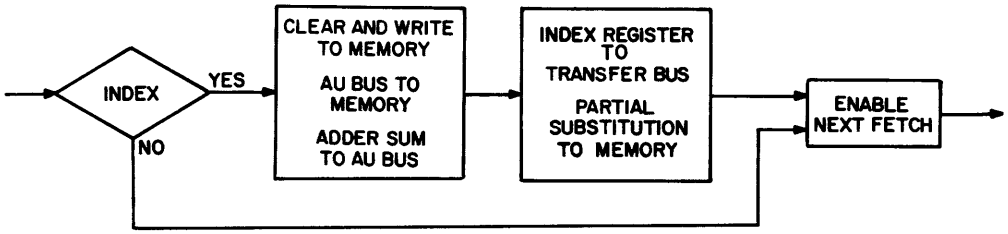
Figure 4-54. OPN 65 Scale Left, Flow Chart and Timing Diagram

STORE INDEX (STX) OPN66

In this instruction the contents of the index register replace the contents of the address portion of the memory word bits 10-24 at the effective address. The index register and bits 1-9 of the memory word are unchanged (Figure 4-55).

The operate cycle is entered and an AD signal is generated at T23 time to cause a partial substitution to memory. A write to memory access is done at T12 and a 2-μsec pulse XTT is generated during T23 time to transfer the specified index register onto the transfer bus. If no index register is specified all ones are on the transfer bus.

At T15 time an enable next fetch pulse (ENF) is generated to initiate the next fetch cycle.



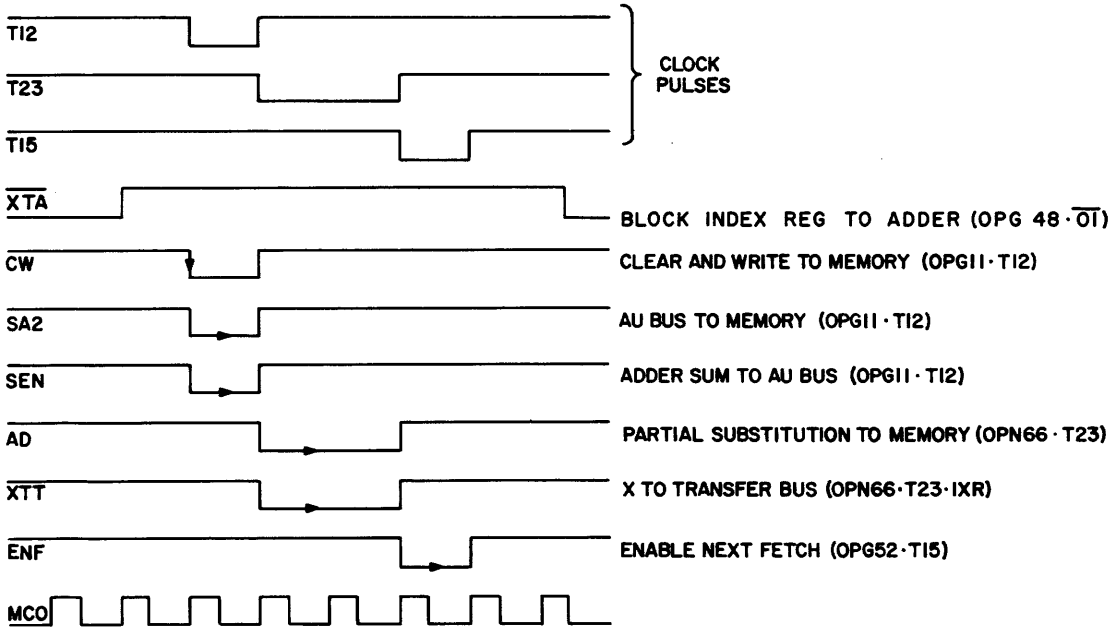


Figure 4-55. OPN 66 Store Index, Flow Chart and Timing Diagram

INCREMENT REPLACE AND LOAD INDEX (IRX) OPN67

This command accesses the memory in a special manner. It uses several of the memory interface logical controls. Memory is used in a split-cycle fashion as well as in a partial substitution mode. During this command a special external reset of the information register is supplied to the address portion of MIR (Figure 4-56).

IRX is started by making a memory access read and regenerate type at T12 time. A special consideration in this access is the fact that the index register does not modify the address field of the instruction word although an index bit may be in the instruction word. The index bit does not modify the address because its purpose is to specify whether the incremented word that results during the performance of this instruction is to be placed back in the specified index register or placed in the A register instead.

As in all other operand accesses, the memory access for this instruction is started at T12 time. However, during the memory access, a special control line to the memory (the write enable line) is forced to ground, thus inhibiting the second or regeneration portion of the read-regenerate cycle. Once the operand has been placed in the Z register, the address field is incremented by one by the removal of all register inputs to the adder with the exception of rZ. While the adder is set up with rZ alone as the input, an additional input in the form of a low-order carry is inserted into the adder, thus forming the sum of rZ + 1. During this addition, the adder-carry between the address field and the lowest order bit of the OP code field is inhibited. This special adder-carry inhibit prevents the incremented number from overflowing into the OP code portion of the word. If the IRX instruction is indexed, the resulting sum of the increment step is transferred into the specified index register. If no index register is specified, the resulting sum is transferred to the A register; in this case the A register is cleared prior to the forming of the new sum. Once the incremented number is transferred (into the A register or the index register) the register containing the number is gated onto the transfer bus and the second half of the memory cycle is started.

This second half of the memory cycle is started by the signal having the mnemonic start-write (SW). Prior to SW, RI is sent to memory and resets the address field of MIR. Note that in this special split-cycle mode of operation the address is not modified during the regeneration cycle; i.e., the original access, which was a read access in the early part of the command, selected a specified address which is left unmodified. The WE signal then prevents that read and regenerate cycle from performing a complete regeneration by inhibiting the regeneration portion of the cycle. Thus, halfway through the memory cycle the memory comes to a halt and no further processing is accomplished with the core memory system until the SW signal is emitted from the CPU. When the SW signal is emitted, the read flip-flop in the memory will have been reset by RI to the write configuration and the regeneration cycle goes on from there. (Note that the memory address register is not modified at the occurrence of the SW pulse from the central processor.)

An ENF pulse is then generated at T08 time to enable the next fetch.

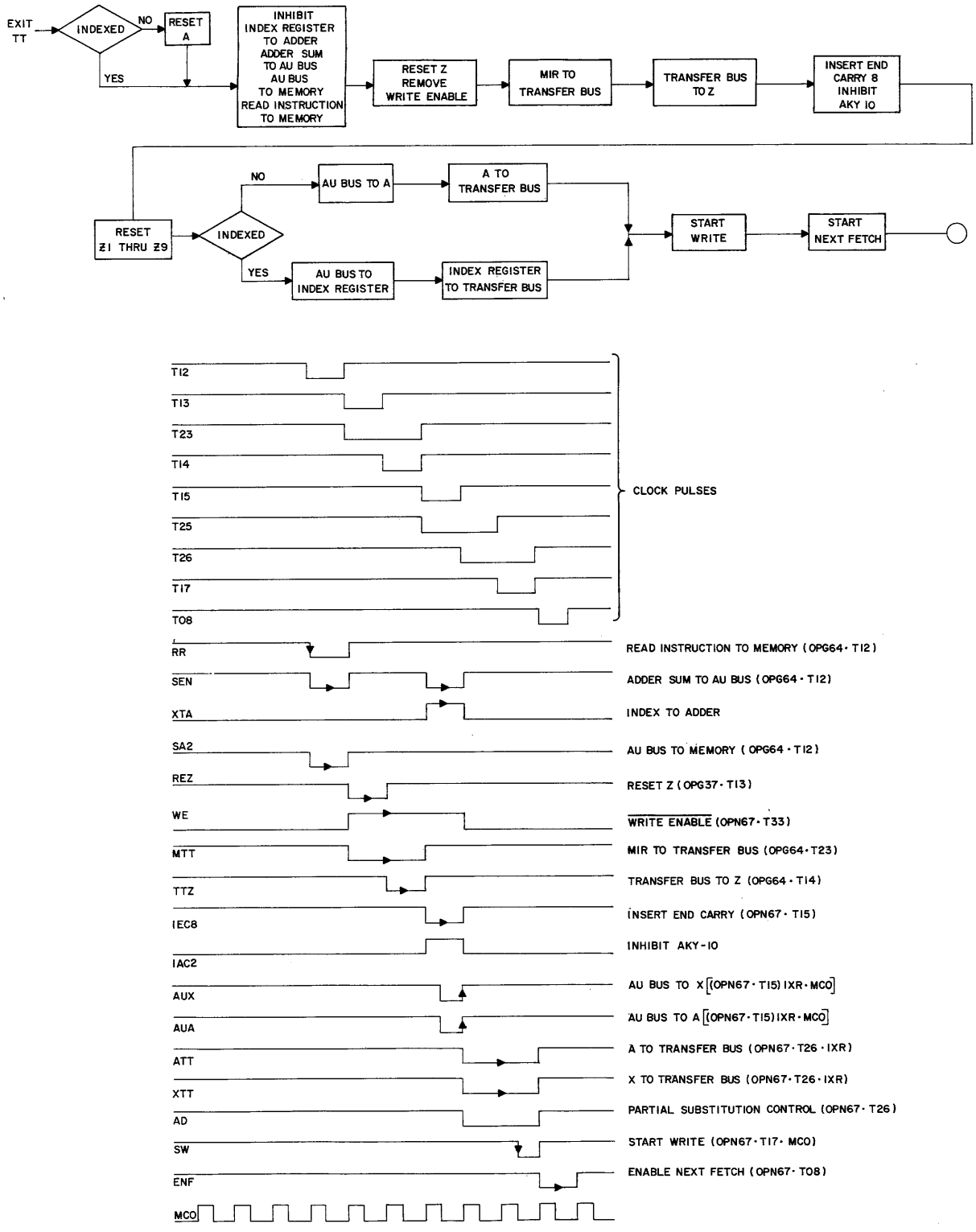


Figure 4-56. OPN 67 Increment Replace and Load Index, Flow Chart and Timing Diagram

JUMP IF rA IS POSITIVE (JPL) OPN70

If the sign of rA is positive (zero bit), the computer takes its next instruction from the memory word at the effective address and continues from there. If the sign of rA is negative (one bit), the computer takes the next sequential instruction (Figure 4-57).

During TT time an enable next fetch pulse (ENF) is generated and the next fetch cycle is initiated. At T11 and T12 time, a SEN signal is generated to gate the sum output of the adder onto the AU bus.

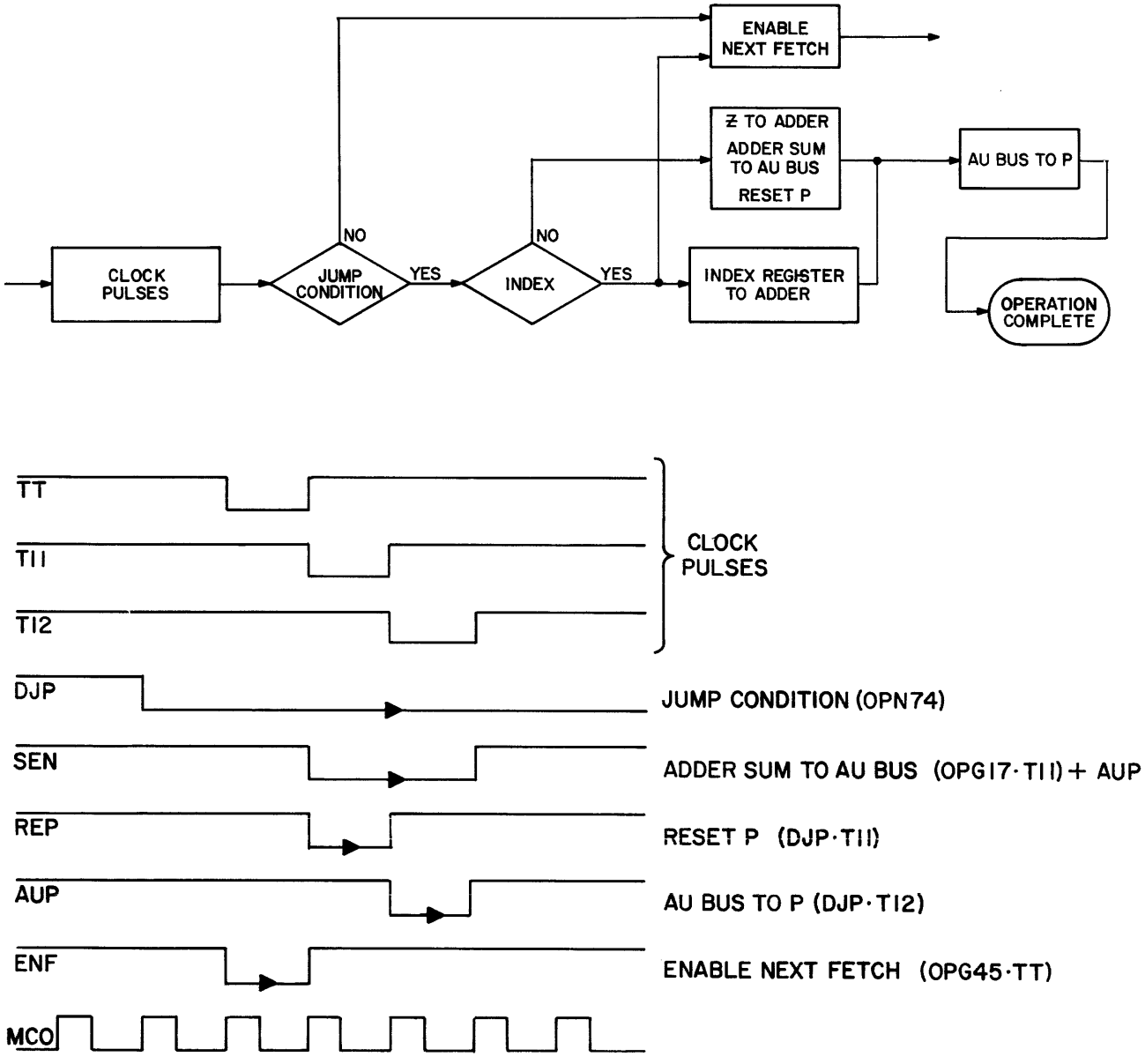


Figure 4-57. OPN 70 Jump If rA is Positive, Flow Chart and Timing Diagram

If the jump condition (A1 = 0) exists, a static gate DJP becomes true. Because DJP is true two signals are produced: REP generated during T11 time to reset the program counter (P) and AUP generated during T12 to gate the 15 low-order bits of the AU bus into P.

JUMP IF rA IS ZERO (JZE) OPN71

If the contents (excluding the sign) of rA are zero, the computer takes its next instruction from the memory word at the effective address and continues from there. If the rA contents (excluding the sign) are not equal to zero, the computer takes the next sequential instruction (Figure 4-58).

During TT time, an enable next fetch pulse (ENF) is generated to initiate the next fetch cycle. At T11 and T12 time, a SEN signal is generated to gate the sum output of the adder onto the AU bus.

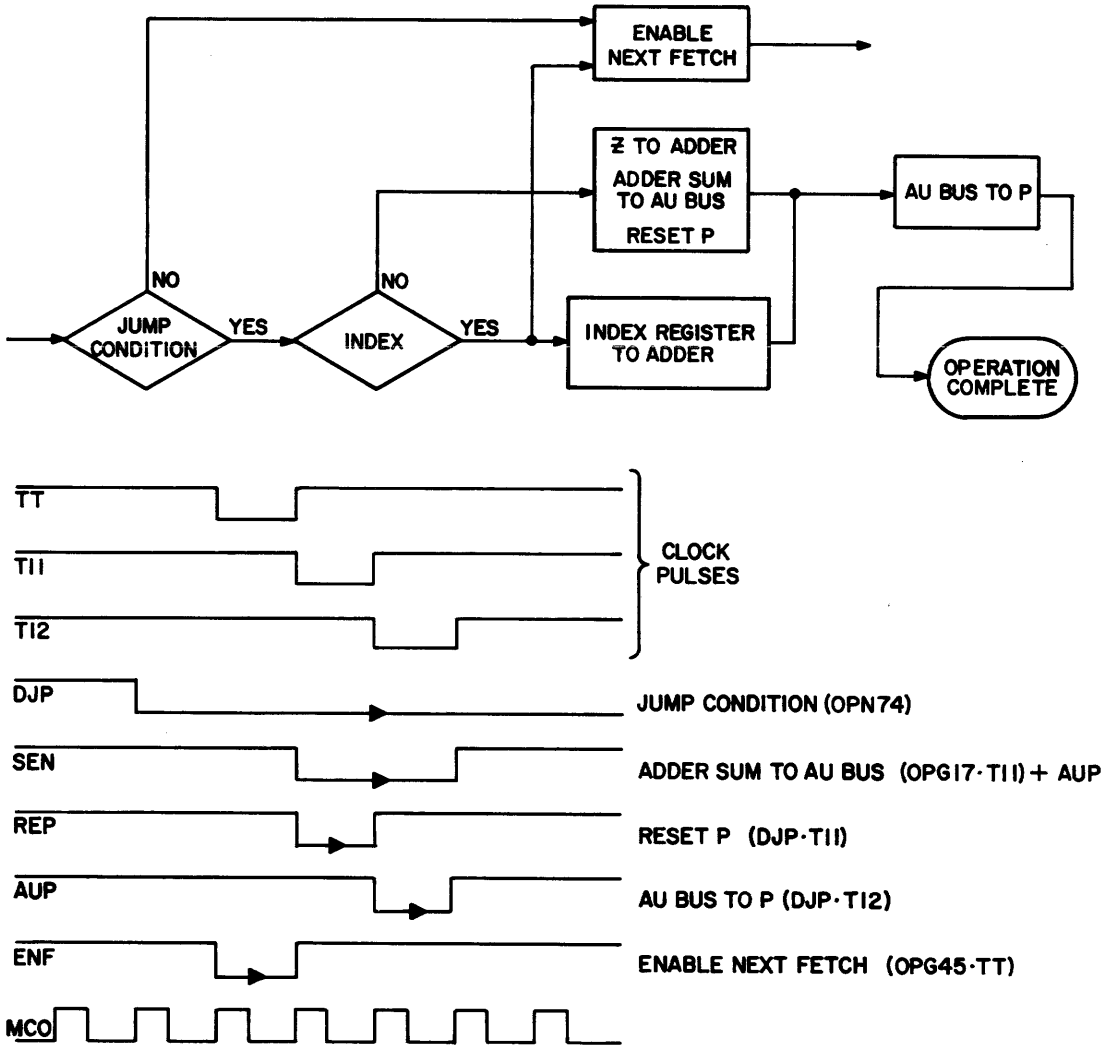


Figure 4-58. OPN 71 Jump If rA is Zero, Flow Chart and Timing Diagram

If the jump condition (the content of rA excluding sign equals zero) exists, a statis gate DJP becomes true, and, being true, produces two signals — REP, generated during T11, to reset the program counter (P) and AUP, generated during T12, to gate the 15 low-order bits of the AU bus into P.

JUMP ON INDEX (JIX) OPN72

If the contents of the index register are not zero, the computer will take its next instruction from the memory word at the address specified by the address field in rZ and continue from there. If the contents are equal to zero, the computer takes the next sequential instruction (Figure 4-59).

During TT time, an enable next fetch pulse (ENF) is generated to initiate the next fetch cycle. Line OPG 48 out of the operation code matrix disables the XTA signal during the execution of this instruction (after indirect addressing). At T11 and T12 time, a SEN signal is generated to gate the sum of rZ + 0 onto the AU bus.

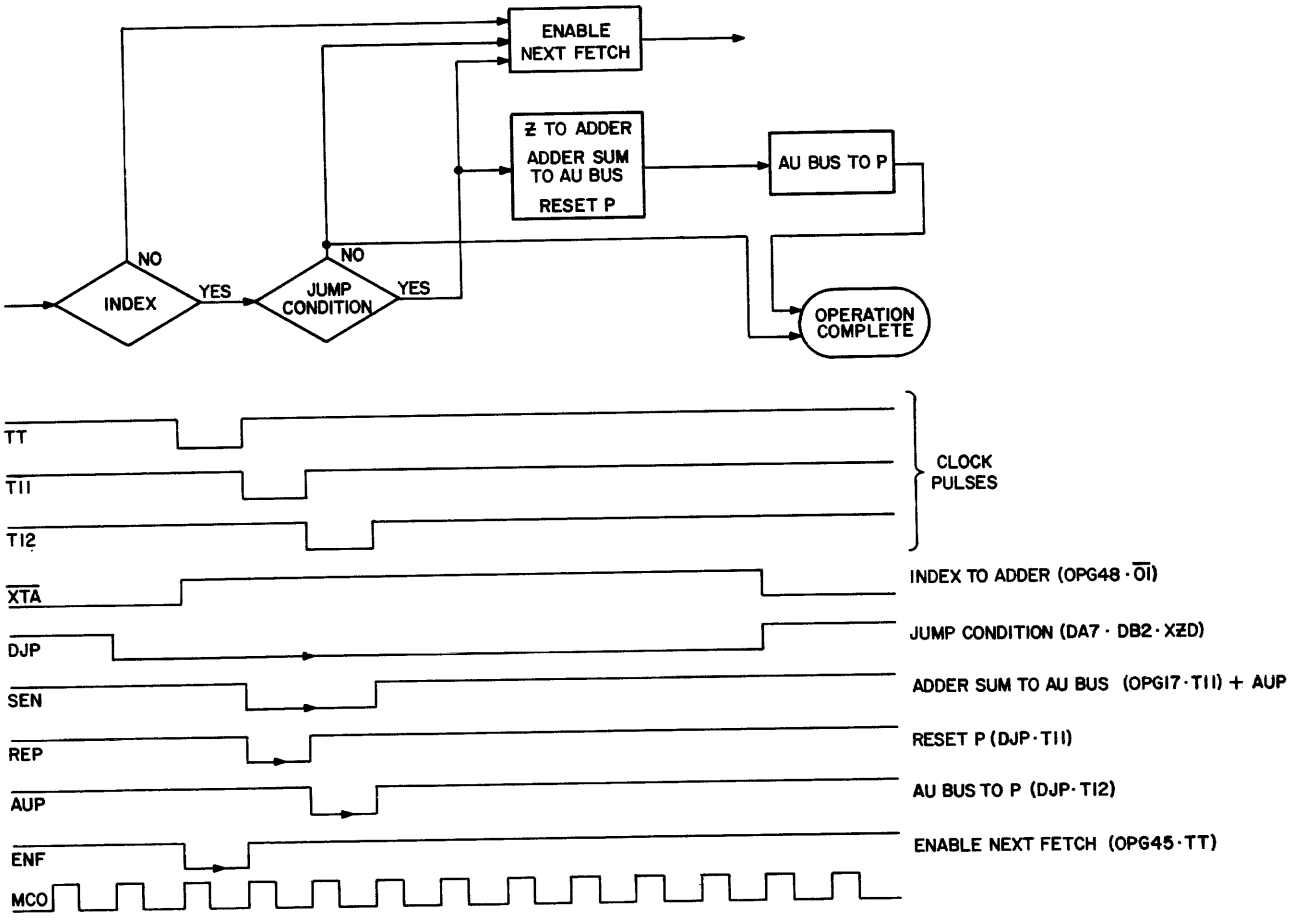


Figure 4-59. OPN 72 Jump on Index, Flow Chart and Timing Diagram

If the jump condition (index register ≠ 0) exists, a static gate DJP becomes true, and being true, produces two signals — REP, generated during T11 time, to reset the program counter (P) and AUP, generated during T12 time, to gate the 15 low-order bits of the AU bus into P.

JUMP ON OVERFLOW (JOF) OPN73

If the overflow indicator (C17) is set, it will reset and the computer will take its next instruction from the memory word at the effective address and continue from there. If the overflow indicator is not set the computer takes the next sequential instruction (Figure 4-60).

During TT time, an enable next fetch pulse (ENF) is generated to initiate the next fetch cycle. At T11 and T12 time, SEN is generated to gate the sum output of the adder onto the AU bus.

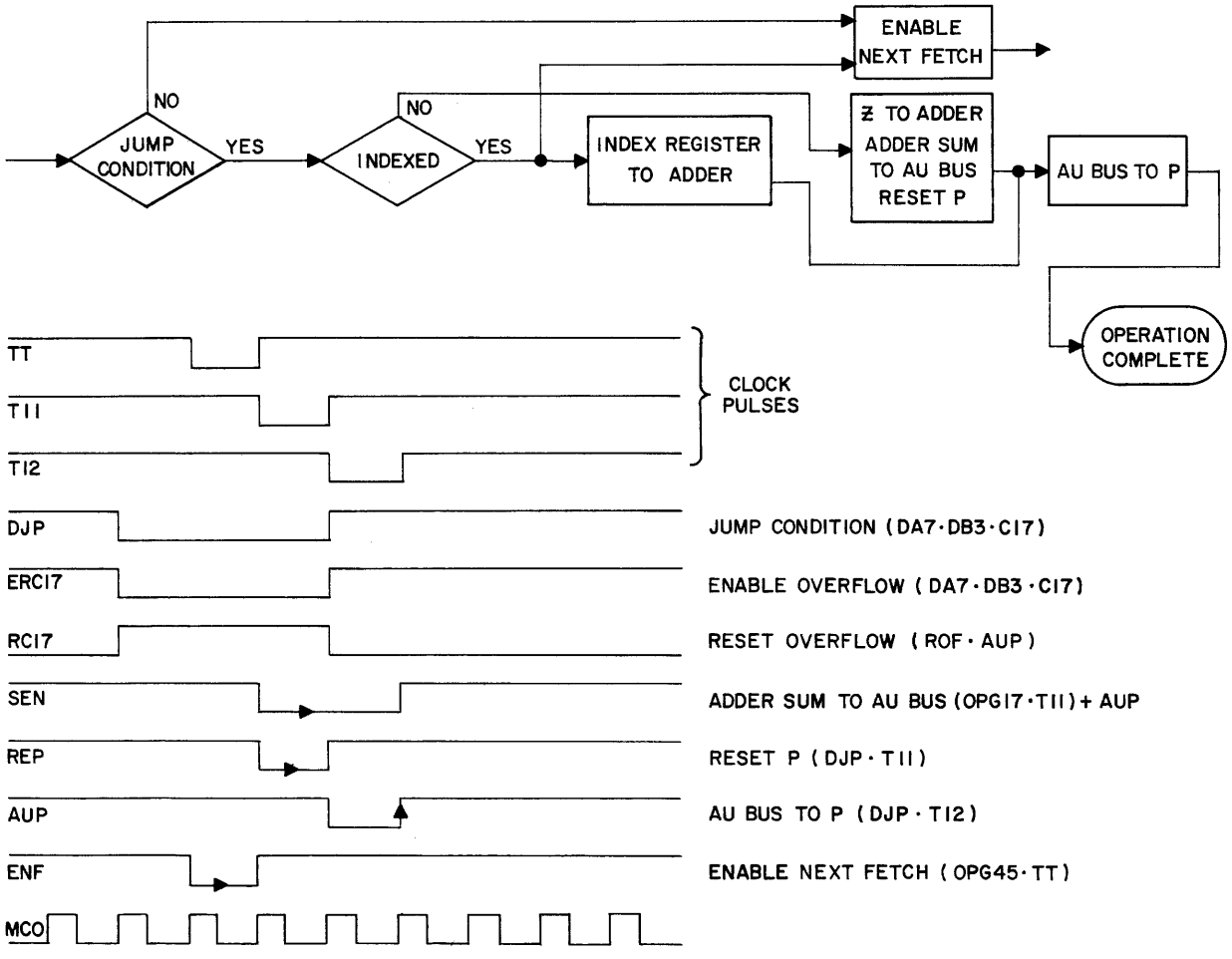


Figure 4-60. OPN 73 Jump on Overflow, Flow Chart and Timing Diagram

If the jump condition (C17 = 1) exists, a static gate DJP becomes true, and being true, C17 is reset. Since DJP is true, it produces two signals — REP, generated during T11 time, to reset the program counter (P) and AUP, generated during T12 time, to gate the 15 low-order bits of the AU bus into P.

UNCONDITIONAL JUMP (JMP) OPN74

In this instruction, the computer takes its next instruction from the memory word at the effective address and continues from there (Figure 4-61).

During TT time, an enable next fetch pulse (ENF) is generated to initiate the next fetch cycle. As soon as the OP code matrix contains the decoded OPN74, a static gate output (DJP) will become true. During T11 and T12 time, SEN is generated to gate the sum output of the adder onto the AU bus.

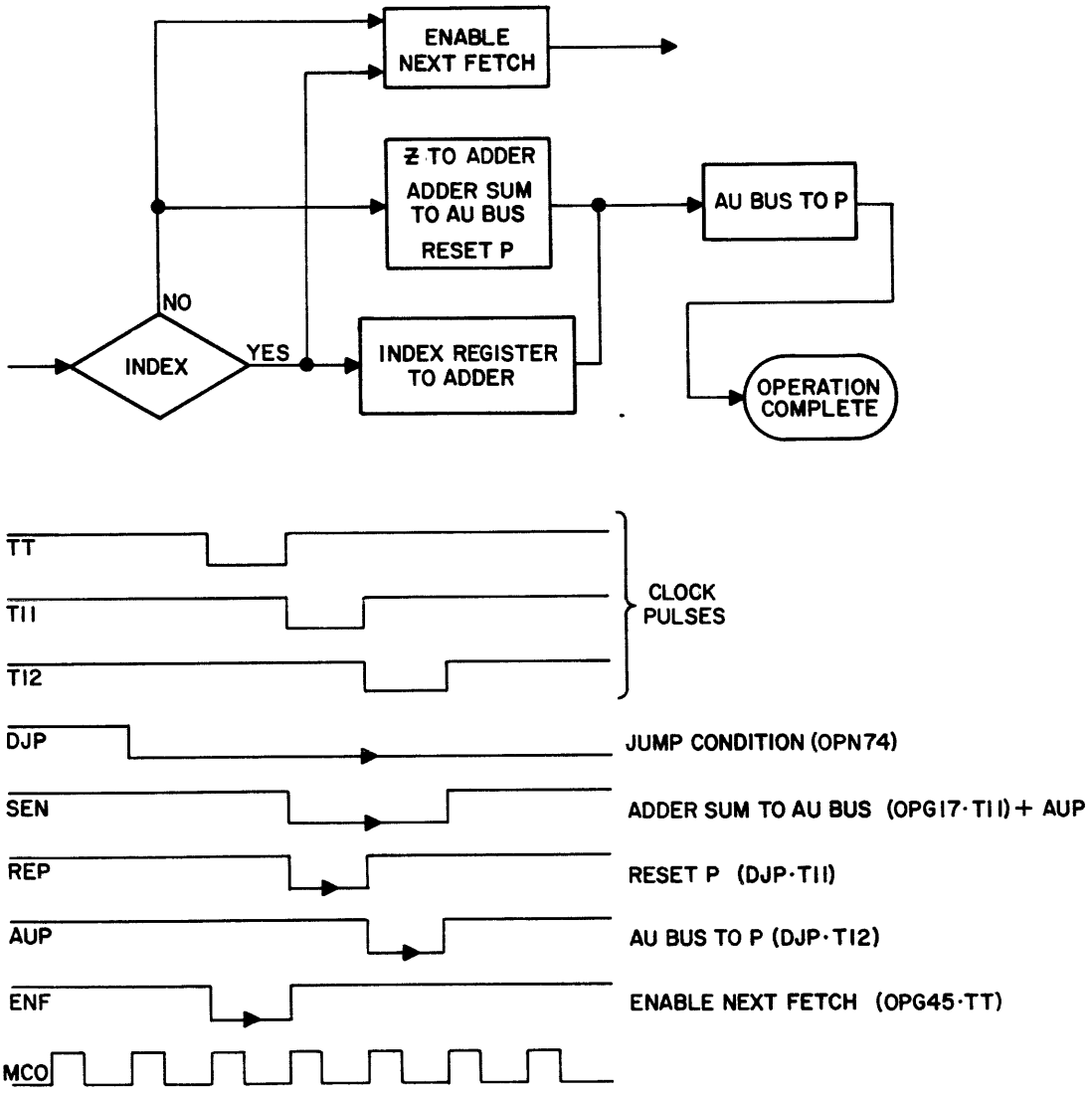


Figure 4-61. OPN 74 Unconditional Jump, Flow Chart and Timing Diagram

Since (DJP) is true it produces two signals — REP, generated during T11 time, to reset the program (P) and AUP, generated during T12 time, to gate the 15 low-order bits of the AU bus into P.

JUMP ON INDEX INCREMENTED (JXI) OPN75

In this instruction, the contents of the index register are incremented by one and the resulting sum replaces the contents of the index register. If this sum is not zero, the computer takes its next instruction from the memory word at the effective address and continues from there; if this sum is zero, the computer takes its next sequential instruction (Figure 4-62).

The operate cycle is entered and during T12 time, an enable next fetch pulse (ENF) is generated.

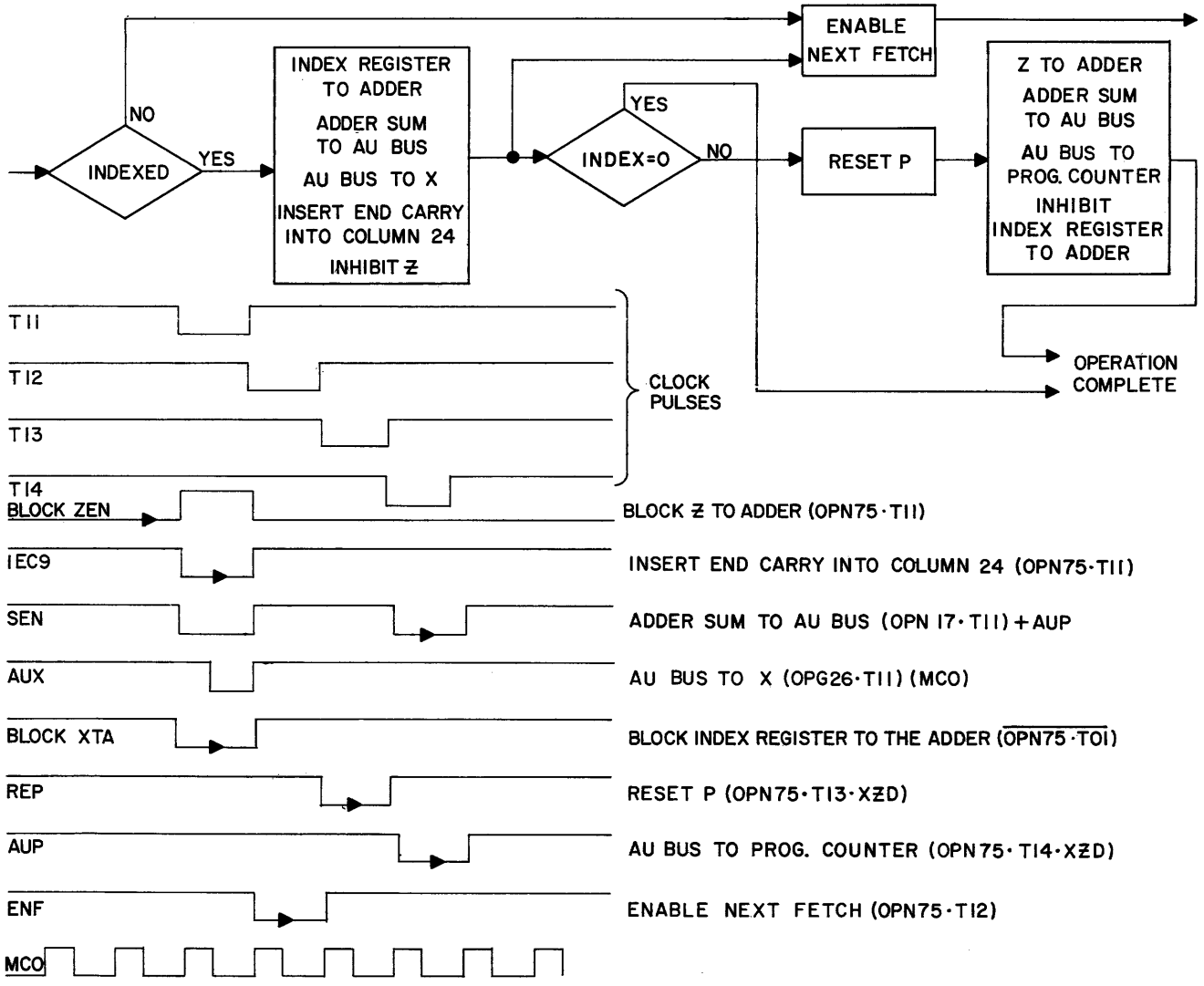


Figure 4-62. OPN 75 Jump on Index Incremented, Flow Chart and Timing Diagram

During T11 time, the ZEN signal (which enables rZ as an input to the adder) is inhibited, an IEC9 signal (which inserts an end-carry into the low-order column 24) is generated, and XTA (which enables the index register to the adder) is present. A SEN signal, generated during T11 time, enables the sum output of the adder onto the AU bus. Also, during T11 time, an AUX signal is generated to transfer the AU bus into the specified index register. If this result is zero, C26 will be true and the computer will take the next sequential instruction. If C26 is false, REP, generated during T13 time, will reset the program counter (P).

ZEN is present to enable rZ to the adder and XTA is blocked to inhibit rX from the adder. SEN is generated at T14 time to enable the adder to the AU bus and AUP is generated during T14 time to gate the 15 low-order bits of the AU bus into rP.

NO OPERATION (NOP) OPN77

No operation is performed by this instruction; the computer takes the next sequential instruction and continues from there. The only action occurs during TT time when an enable next fetch pulse (ENF) is generated to start the next fetch cycle (Figure 4-63).

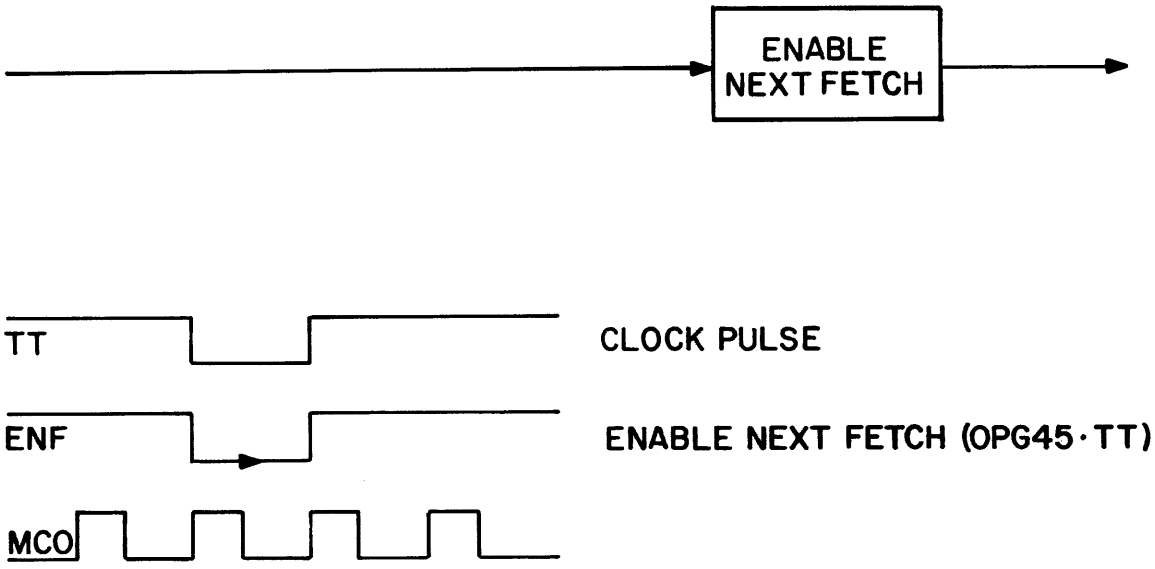


Figure 4-63. OPN 77 No Operation, Flow Chart and Timing Diagram

BIN/BCD INSTRUCTIONS (OPTIONAL)

The BIN instruction (OPN 37) will convert a binary number in memory to a binary-coded-decimal (BCD) number. This decimal number will be left in register B after the operation is completed. The location in memory of the binary number to be converted is specified by the address portion of the instruction. If the binary number is larger than 3,032,377 (BCD = 799,999), the improper-divide indicator will be set and the conversion will not take place.

The BCD instruction (OPN 36) will convert a binary-coded decimal number in memory to a binary number. The binary number will be left in register A after the operation is completed. The location in memory of the decimal number to be converted is specified by the address portion of the instruction.

Inclusion of the BIN/BCD instruction capabilities necessitate additional logic wiring throughout the standard DDP-24 control circuits. The explanations that follow make reference to various control and timing signals which are inherently part of the standard computer. All drawings affected by the inclusion of BIN/BCD logic have been revised in Volume 2 of the Service Manual for the DDP-24 General-Purpose Computer.

Operation of the BIN command is based on the shift left (multiply-by-2) of a decimal number through a binary register. The high-order bits of the binary number are shifted left into the low-order position of the binary register. After three shifts, the number in the binary register must be seven or less. This can be considered a BCD number. If the shift process continues, and it is necessary to maintain a BCD number in this register, certain operations in addition to shifting must be performed.

A BCD digit has 4 bits. The values of this digit are 0 to 9 inclusive. When this number is shifted left (in BCD mode), it is multiplied by 2. The BCD result of this shift is shown in Table 4-1.

TABLE 4-1.
BIN/BCD EQUIVALENTS

Dec. No.	BCD No.	BCD No. x 2
0	0000	0 0000
1	0001	0 0010
2	0010	0 0100
3	0011	0 0110
4	0100	0 1000
5	0101	1 0000
6	0110	1 0010
7	0111	1 0100
8	1000	1 0110
9	1001	1 1000

It can be seen that for 0, 1, 2, 3, and 4, a simple shift left will suffice to obtain the BCD equivalent of twice the original number. For 5, 6, 7, 8, and 9, a simple rule can be established to obtain the appropriate result. Table 4-2 illustrates this rule.

TABLE 4-2.
BIN/BCD EQUIVALENTS
(Multiply-by-2 Rule)

Dec. No.	BCD No.	(BCD No.) + 3	(BCD No.) + 3 shifted left
5	0101	1000	1 0000
6	0110	1001	1 0010
7	0111	1010	1 0100
8	1000	1011	1 0110
9	1001	1100	1 1000

Thus, the rule for BCD multiply by 2 is, before shifting left, add 3 to numbers greater than or equal to 5. This rule must be applied to each decimal digit (group of 4 bits) in the register. Since each one of these digits can be treated separately, the number in the register will always be a BCD number.

In the DDP-24, the binary number is placed in the B register, bits 2-24. It is shifted left from B2 into A24, and the BCD shift rule is applied to the A register. The decimal digits in register A will occupy bits 24-21, 20-17, 16-13, 12-9, 8-5, and 4-2. After 23 shifts, the whole binary number will have been transferred into A and the contents of A will be a BCD number equivalent to the initial binary number. To satisfy established programming requirements, the BCD number in A will be transferred into B.

The operation of the BCD command is based on the shift right in BCD mode (divide-by-2) of a BCD number through a binary register. This operation is the inverse of the BIN instruction BCD shift. The low-order bits of a BCD number can be shifted right once to become a binary number which is one-half the initial number. Thus, the low-order bit of the BCD number is shifted to the right out of the binary register and this process is repeated until the whole BCD number is converted to binary.

In order to shift a BCD number to the right in a binary register, certain operations must be performed on the number. Table 4-3 shows the desired result when a BCD number is divided by 2. The table also shows the result of shifting the BCD number one place to the right. It can be seen that by subtracting 3 from the shifted number, the desired result is obtained. Only the decimal numbers 10 to 19 are shown on the table. Decimal numbers

less than 10 can be treated as binary numbers for the purpose of dividing by 2. Numbers from 20 to 99 can be treated as two separate binary numbers in two different decimal digits, since there is no borrowing between decimal digits when dividing by 2.

The rule for BCD divide-by-2 is as follows: shift the number to the right one place; if the BCD digit is 8 or larger, subtract 3. This rule must be applied to each BCD digit (group 4 bits).

In the DDP-24, the BCD number is loaded into the A register. The A register can be used to add 3 to certain BCD digits. This feature must be used for the BIN command, and can also be used for the BCD command if the BCD number in the A register is complemented. The rule for BCD divide will then be as follows: shift the number to the right one place; if the BCD digit is less than 8, add 3.

TABLE 4-3.
BCD/BIN EQUIVALENTS

Dec. No.	BCD	BCD/2	BCD shifted right	(BCD shifted right) -3
10	1 0000	0101 0	1000 0	0101 0
11	1 0001	0101 1	1000 1	0101 1
12	1 0010	0110 0	1001 0	0110 0
13	1 0011	0110 1	1001 1	0110 1
14	1 0100	0111 0	1010 0	0111 0
15	1 0101	0111 1	1010 1	0111 1
16	1 0110	1000 0	1011 0	1000 0
17	1 0111	1000 1	1011 1	1000 1
18	1 1000	1001 0	1100 0	1001 0
19	1 1001	1001 1	1100 1	1001 1

With the new rule for BCD divide, the add -3 networks used for BIN can be used for BCD. The BCD digits occupy the same positions as for BIN: bit 24-21, 20-17, 16-13, 12-9, 8-5, and 4-2. The low-order bit of register A (A24) is shifted into the high-order bit of the B register (B2). After 23 shifts to the right, the binary conversion of the complemented BCD number will be in B. This number is then transferred back to A and complemented to obtain the binary number.

A read memory access is initiated during T12 time to obtain the binary number for memory. (Refer to timing sequence diagram, Figure 4-64, and flow chart, Figure 4-65.) The shift counter is set to 24 at this time. The number from memory is gated into the transfer bus (MTT) at T23, and is loaded into B (TTB) at T14. The sign of the number is loaded into A1 at T15.

At T14, a T08 pulse is generated. T08 enables ATA and ZEN is enabled for the whole instruction, except for T13 and T09. The shift counter is decremented every microsecond by SSC. The B register is shifted left by SBL, and the number enters A through A24. SEL is enabled during T08 allowing the number to be shifted and a 3 to be added to those BCD digits which are greater or equal to 5. AUA is pulsed during T08 and AUA-1 is inhibited in order to save the sign in A1.

When the shift counter equals 3 (SCE3 true), an ENF is generated to fetch the next instruction. When SCE2 is true, T09 is generated. During T09, the BCD number in A (including sign) is transferred into B. This is accomplished by ATT and TTB.

A read memory access is initiated during T12 to obtain the BCD number from memory. (Refer to timing sequence diagram, Figure 4-66, and flow chart, Figure 4-67.) The shift counter is set to 24 at this time. The number in memory is gated into the transfer bus (MTT) at T23, and is loaded into A (TTA and AUA) at T14. The sign is loaded into B1 at T14.

T14 generates T08 and T08 generates ATA, SER, and AUA to shift sum and load it into A register. Zen and KTZ are active during T08 to enable the addition of 3 to certain BCD digits. SSC will decrement the shift counter by one every microsecond. SBR shifts the number in B to the right. During the first microsecond of T08 (T15), CAA is enabled and ATA is inhibited. This complements the BCD number at the beginning of the shift.

When the shift counter equals 2 (SCE2), an ENF is generated to fetch the next instruction. SCE2 also ends T08 and starts T09. SSC and AUA are pulsed through T08 and T09. During the first microsecond of T09 (SCE1), BTT and TTA are TRUE. This loads B register into A register. During the second microsecond of T09 (SCE0), CAA and SEN are enabled, thus complementing the binary number in A. The sign is loaded in A1 by B1 OPN 36.

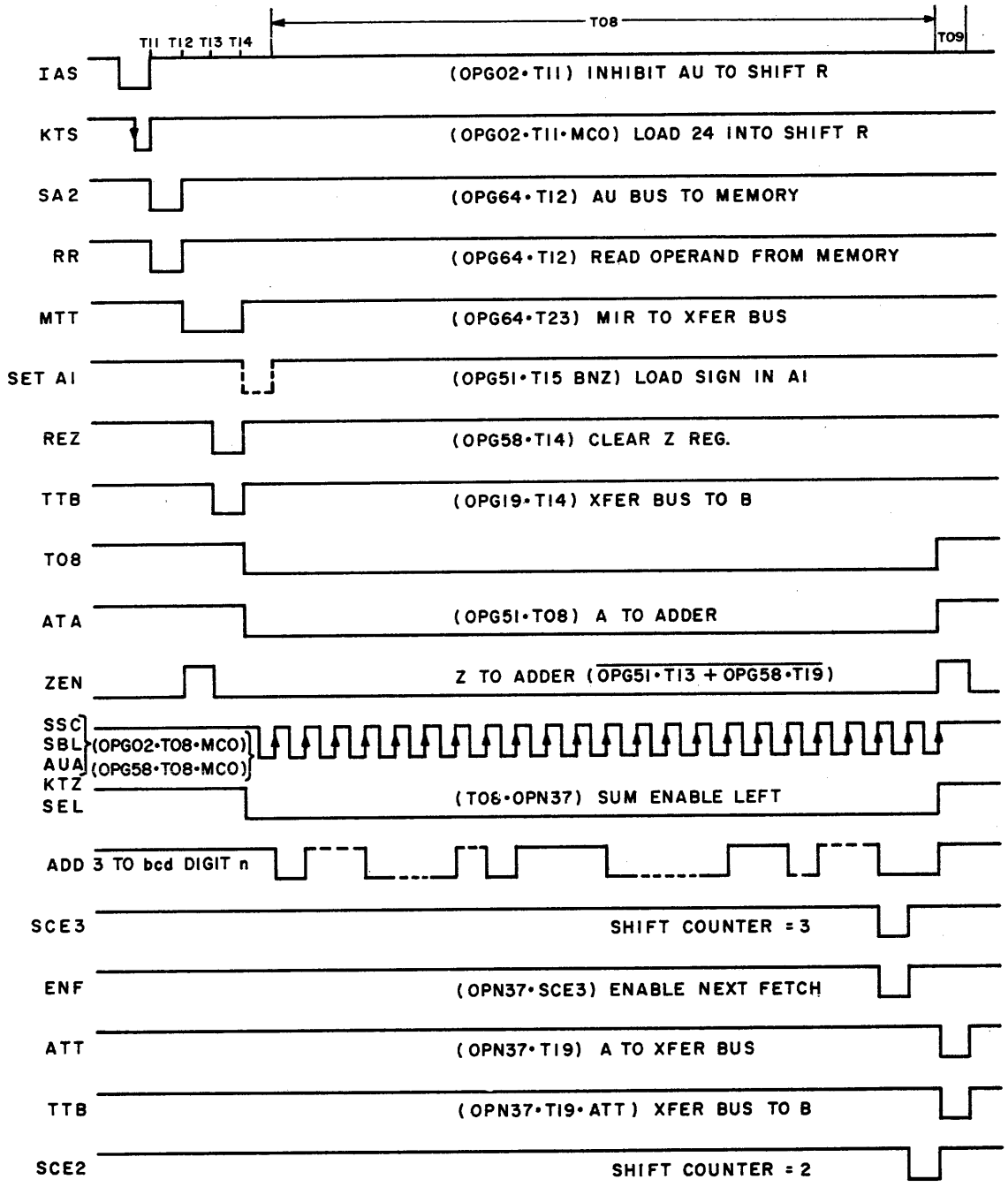


Figure 4-64. BIN Timing Sequence Diagram

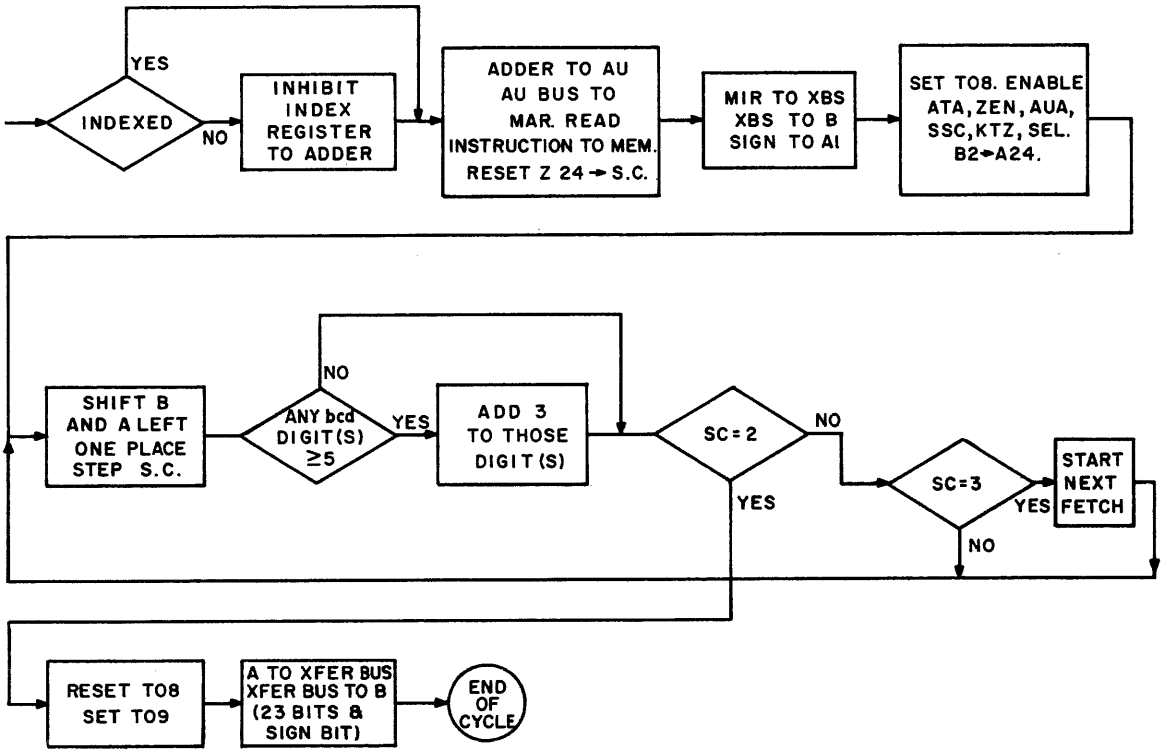


Figure 4-65. BIN Flow Chart

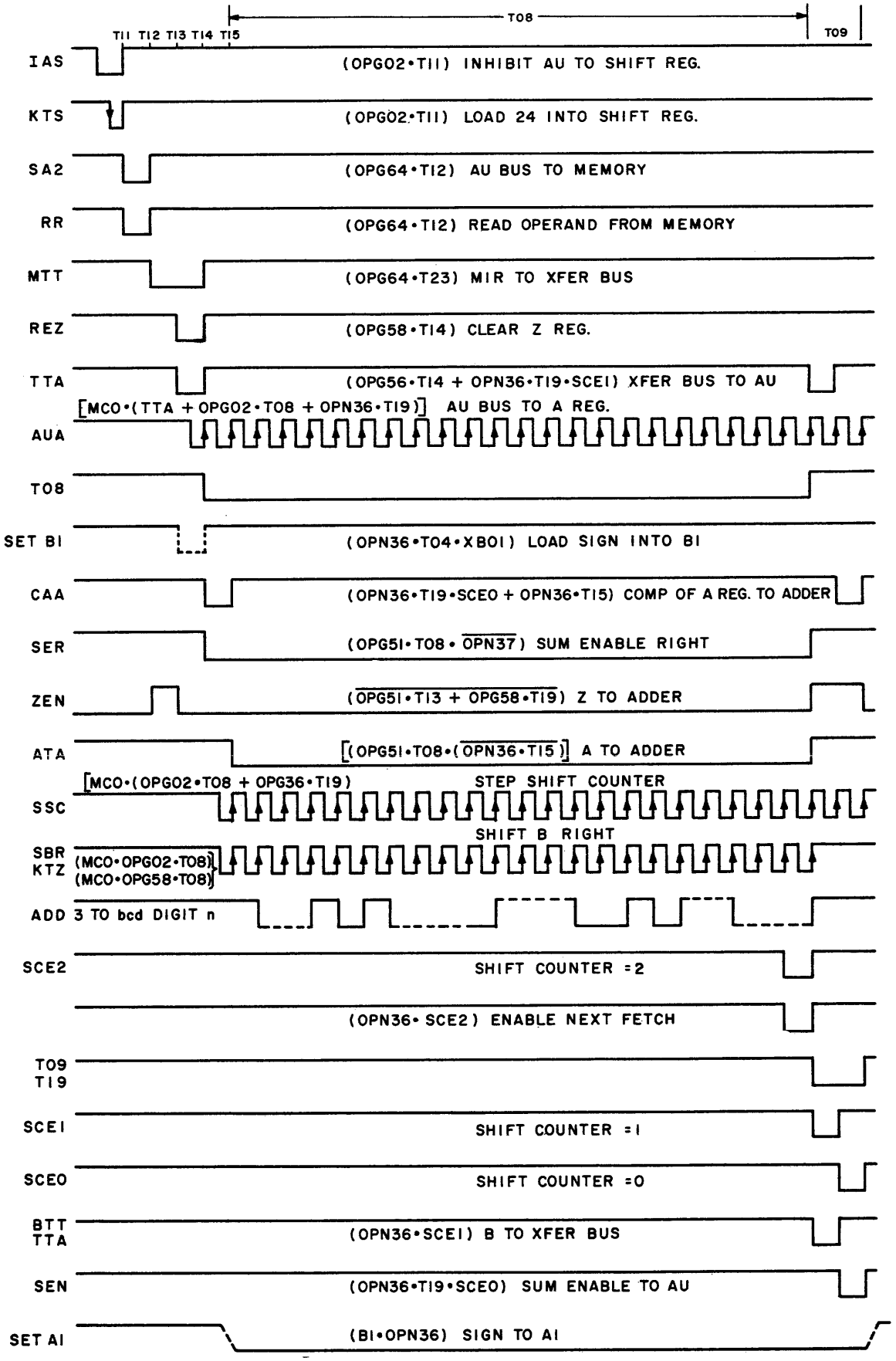


Figure 4-66. BCD Timing Sequence Diagram

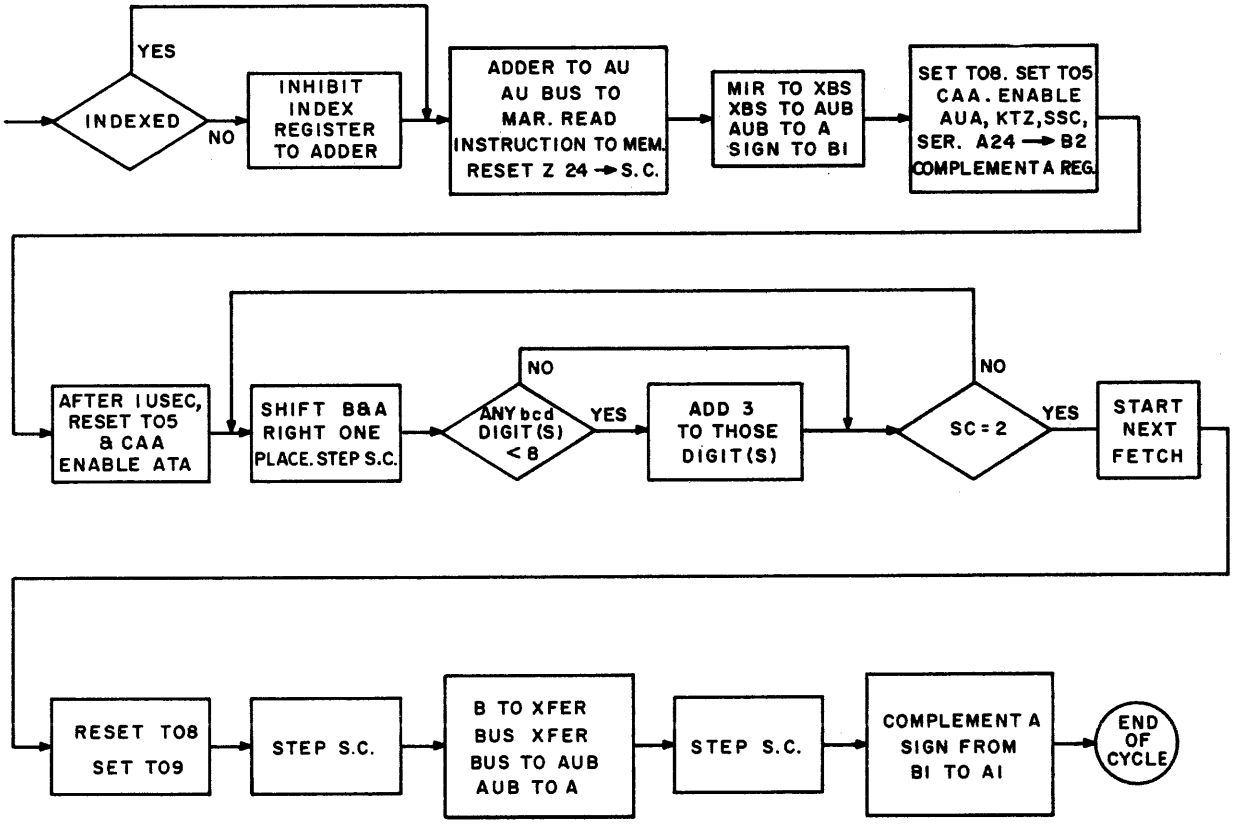


Figure 4-67. BCD Flow Chart

SECTION V
INPUT-OUTPUT (I/O) CHARACTERISTICS

5-1 GENERAL

Input/output devices for the DDP-24 include an electric typewriter, a photoelectric, paper-tape reader, and a paper tape punch. The typewriter has a 15-character-per-second rate and a program controlled keyboard lock. The lock permits data input from the typewriter without interfering with other peripheral equipment. When the paper tape reader is used, the keyboard is automatically locked; the lock may be released by the typewriter off-line switch.

The paper tape reader may be operated at a 300 character per second rate in the continuous mode or at a slower rate in the pulsed mode. In the pulsed mode, the paper tape reader stops after each character and the program must supply a signal when the next character can be read.

The paper tape punch may be operated at a rate of 60 characters per second.

Control panel switches select different on-line and off-line combinations of input/output devices. These include paper tape preparation from the keyboard; type-out of paper tape input; and paper tape duplication by punch out of paper tape input. The input-output diagram (Figure 5-1) illustrates the interconnection of the standard peripheral equipment, input-output channels, interrupt control, OCP, and the sense inputs.

5-2 SENSE LINES

A number of single lines from either external or internal sources can be tested by the SKS command 61 (skip if sense line not set). In the standard DDP-24, the following test inputs are provided.

a. Six sense switches on the control panel allow the programmer or operator manual control of program branching.

b. There are four internal computer flip-flops - overflow, improper divide, input parity, and stop code.

Note

All or several of the foregoing 10 test inputs can be tested simultaneously as controlled by the address portion of the SKS command. Any or all of the tested sense lines may cause a skip.

c. Of the four sense lines from the ready flip-flops of the four standard I/O channels, all or several can be tested simultaneously, controlled by the address portion of the SKS command. Ready signals of any optional additional I/O channels can also be tested simultaneously, up to a total of 12. Any or all of the tested channel ready sense lines may cause a skip.

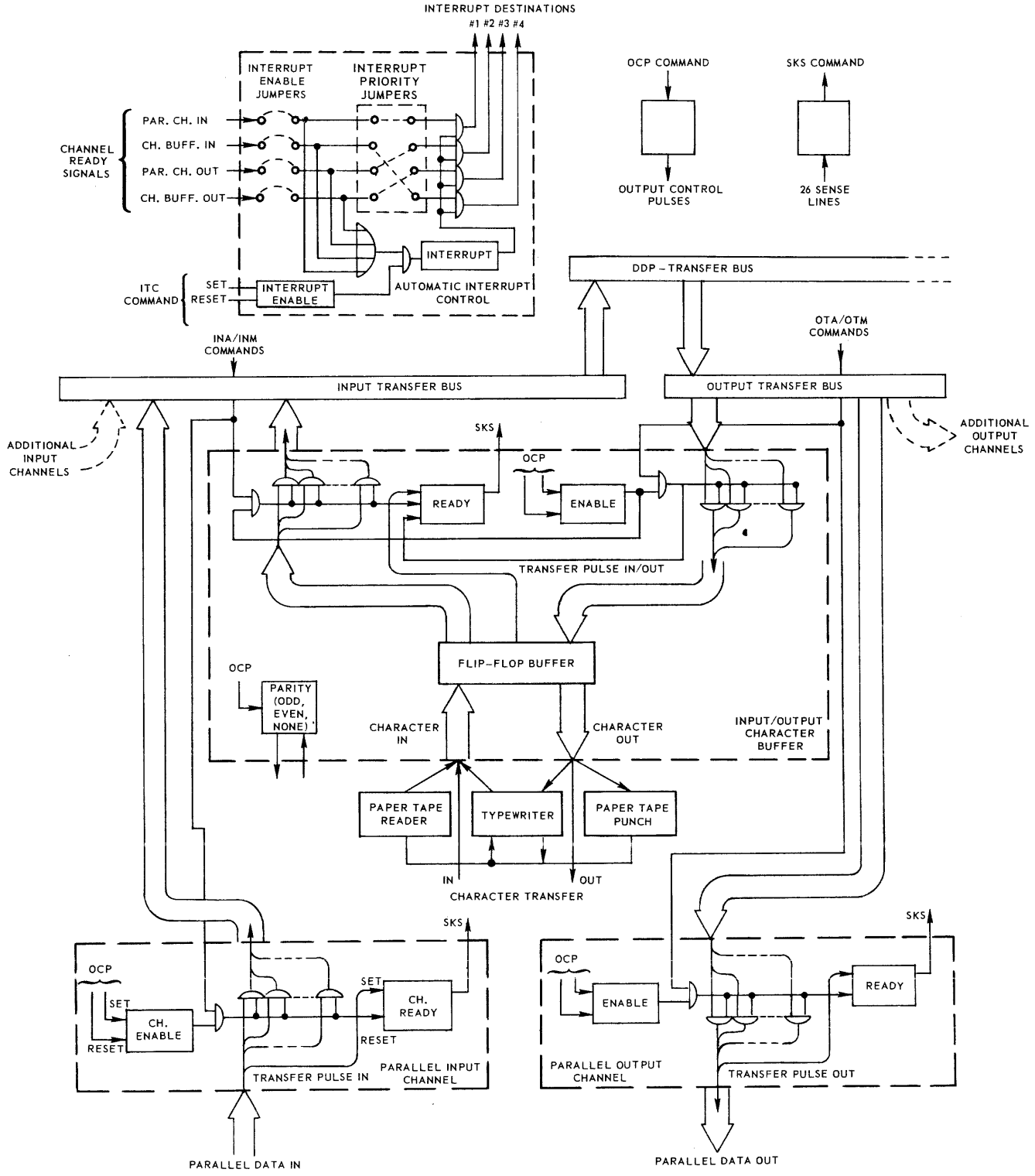


Figure 5-1. Input-Output Block Diagram

d. Of sixteen external sense lines from peripheral equipment, only one can be tested at a time. The number of test signals external to the computer can be expanded to over 2000.

The standard and optional general-purpose sense lines are tested with an SKS instruction selected according to its decoded address portion, bits 10 through 24. A 2-μsec select signal samples the sense line, then a 1-μsec test pulse steps the program counter if the sense input is not true. If bit 10 is ONE, the test pulse is returned as a reset signal upon execution of the SKS instruction. This can reset the test signal. For the proper decoding of the address portion of SKS, octave decoding is used. A decoding matrix of four octal decoders with eight outputs per octave is an integral part of the DDP-24. This matrix ensures simple and straightforward expansion. The 16 general-purpose sense lines (standard with the DDP-24) correspond to octal address portion codes 20000 through 30000 through 30007. A general diagram for one sense line input is shown in Figure 5-2. SKS signal characteristics are shown in Figure 5-3. The SKS signal specifications are as follows.

Sense Input Signals:

SET level:	-5 volts to -6.5 volts
NOT SET level:	0 volt to -1.5 volts
Input loading:	2.8 ma at 0 volt; 0 ma at -6 volts
Pulse RTI	

Reset Pulse RTI:

ONE level:	-6 volts
ZERO level:	0 volt
Output waveform width:	1 μsec
Rise time:	0.1 μsec (nominal)
Fall time:	0.15 μsec (nominal)
Output Loading:	100 ma and up to 2000 pf of stray capacitance.

5-3 OUTPUT CONTROL PULSES

The OCP command (output control pulse) provides control pulses for up to 4096 different lines to external equipment. Coding the address portion of this command selects the line; codes have been selected and others reserved for certain input-output control functions (such as start and stop devices) and enabling input-output control channels.

The OCP instruction generates a 2-μsec pulse, the destination of which is controlled by the address portion bits 10-24. The standard DDP includes certain OCP lines such as channel enable pulses for internal use. In addition, eight general-purpose OCP lines are provided for external use. This number can be expanded with either OCP pulse lines, output control DC signal lines, or output control DC signal lines with power drivers. (OCP lines required as part of optional equipment generally are included with the equipment.)

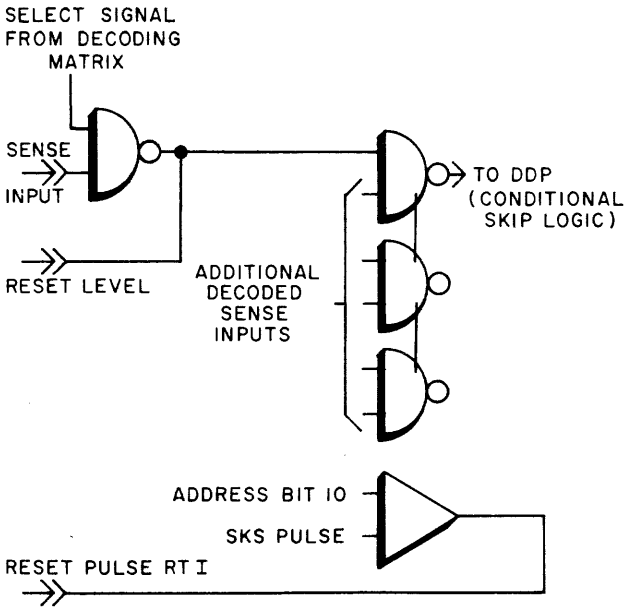


Figure 5-2. Typical Sense Line Input

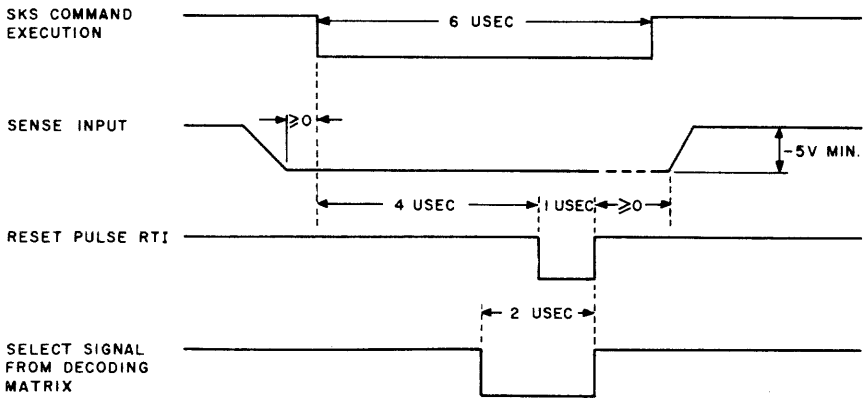


Figure 5-3. SKS Signal Characteristics

The address portion decoding of the OCP command makes use of the same integral decoding matrix as the SKS. The eight standard OCP lines of the DDP-24 correspond to octal address portion codes 01010 through 01017. Figure 5-4 shows a simplified diagram of the different types of OCP lines. Figure 5-5 shows the timing of the output control pulse. Specifications for the OCP signal are as follows.

Polarity:	Positive-going, between -6 volts and 0 volt
Width:	2 μsec
Rise time:	0.1 μsec (nominal)
Fall time:	0.15 μsec (nominal)
Output loading:	17 ma and up to 400 pf of stray capacitance.

Output Control DC Signal:

TRUE level:	-6 volts
FALSE level:	0 volt
Output loading:	17 ma and up to 400 pf of stray capacitance

Output Control DC Signal With Power Amplifier:

TRUE level:	-6 volts
FALSE level:	0 volt
Output loading:	100 ma and up to 2000 pf of stray capacitance

5-4 PARALLEL INPUT-OUTPUT CHANNELS

One parallel input channel and one parallel output channel are provided with the DDP-24. These allow full 24-bit parallel information transfer into or out of the computer. The two parallel channels handle inputs or pulse outputs. A ready signal indicates when the channel can transfer data; a channel-enable flip-flop enables the channel for subsequent information transfer into or out of the processor. The channel enable flip-flops are set by the computer with properly coded OCP commands. Parallel channels are used with parallel peripheral devices, such as A/D or D/A converters, printers, and digital resolvers. Additional parallel channels are optionally available - either for input or output, with or without a flip-flop buffer. The optional input-output expansion capabilities of the DDP-24 are shown in Figure 5-6.

All input signals are amplified by at least one NAND gate stage (Figure 5-7) is used as DC levels and by at least two NAND gate stages if the leading or trailing edge transitions are used. All output signals from the DDP-24 are NAND gate outputs. In general, TRUE, SET, or ONE signals correspond to -6 volts; FALSE, RESET, or ZERO signals to 0 volt. Consequently, all pulses are negative-going except the output control pulse which is positive-going.

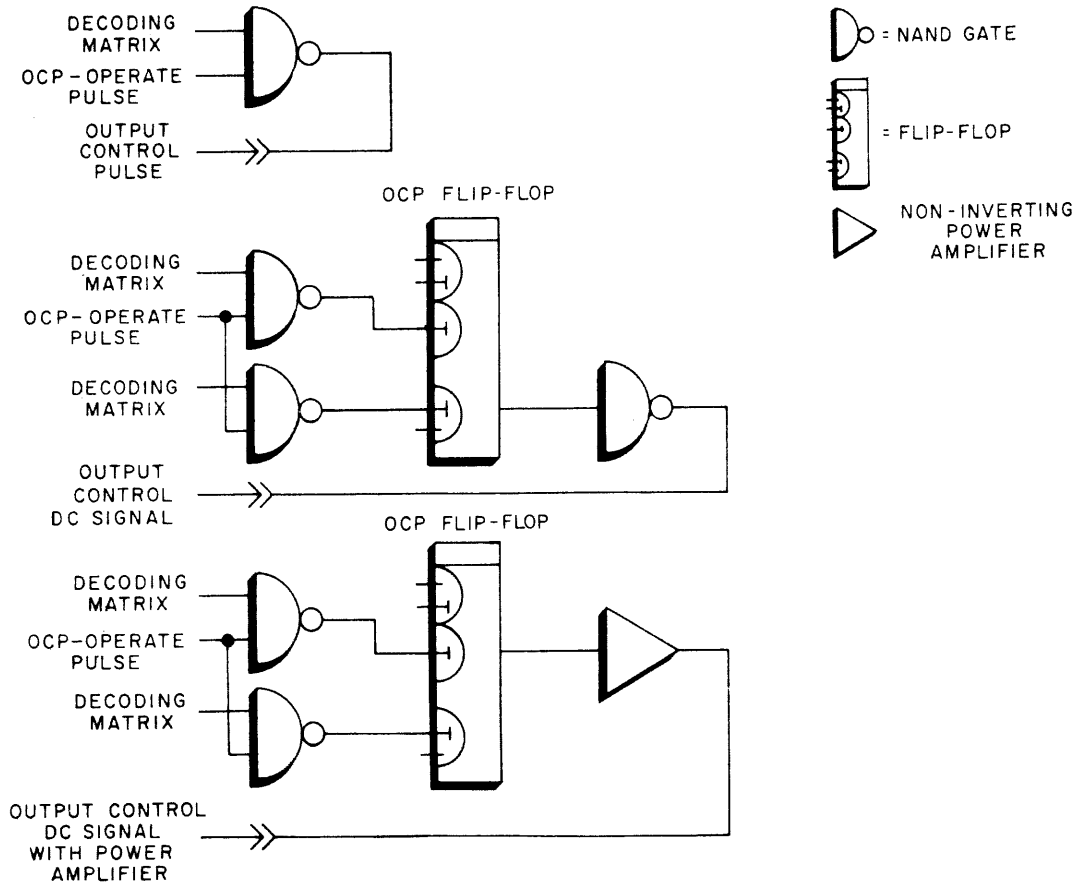


Figure 5-4. Output Control Pulse Lines, Block Diagram

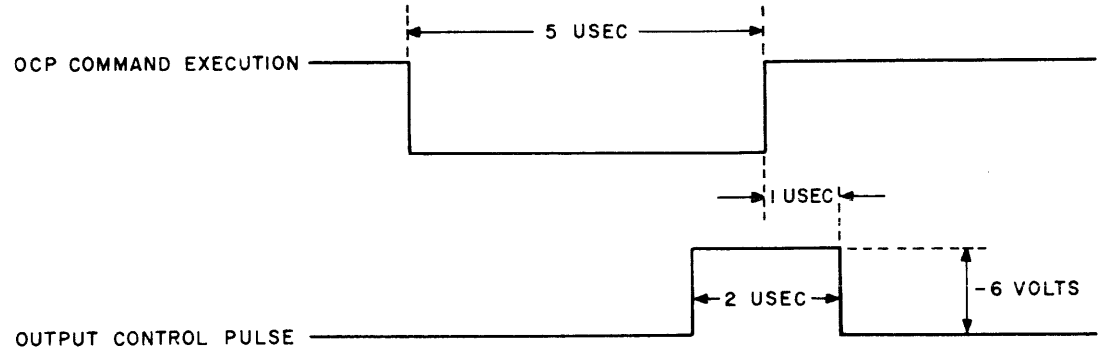


Figure 5-5. Timing Diagram of Output Control Pulses

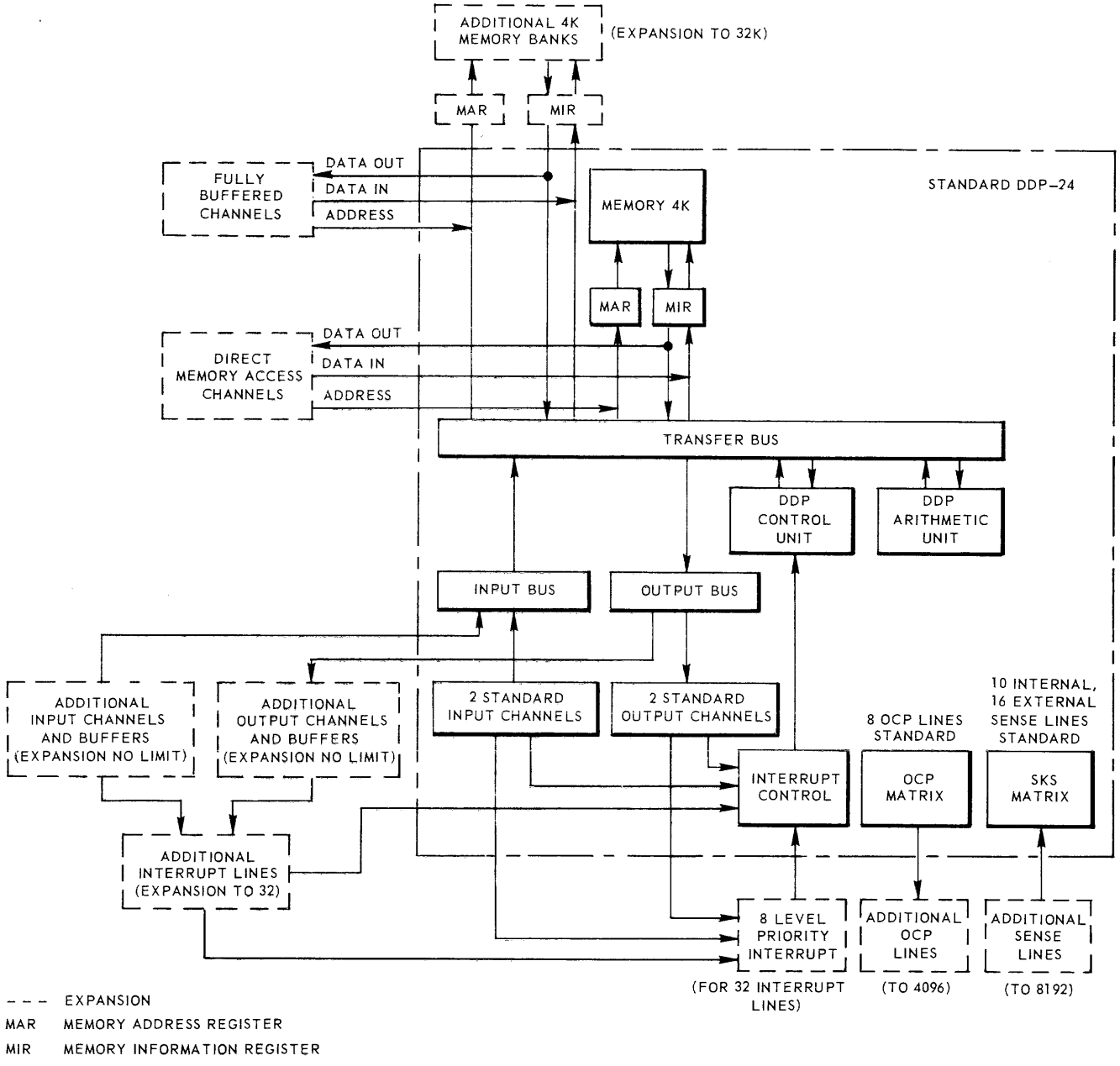


Figure 5-6. Input-Output Expansion Diagram

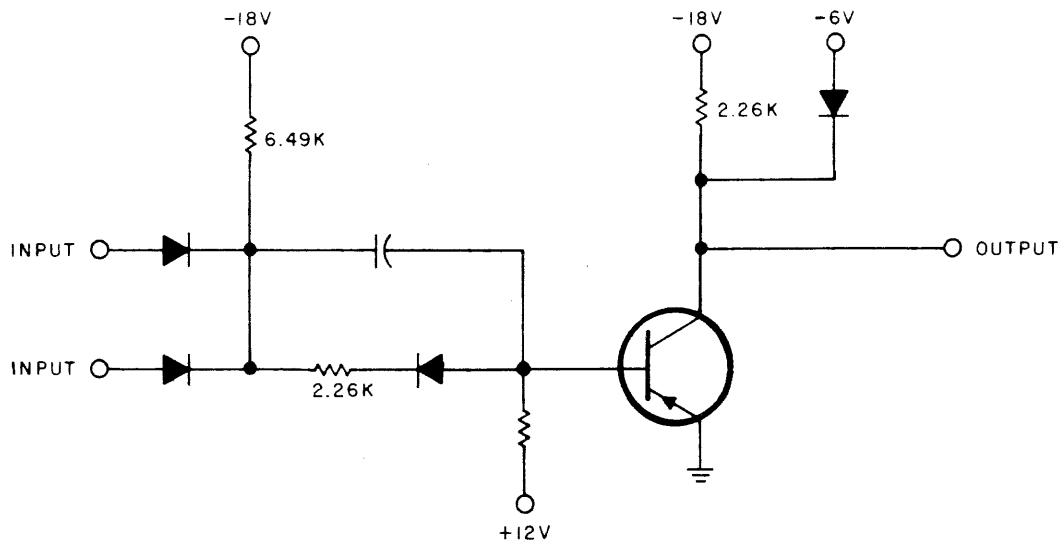


Figure 5-7. Basic NAND Gate Circuit

5-5 PARALLEL INPUT CHANNELS

Transfer of input data using a parallel input channel is illustrated by the block diagram of Figure 5-8. The internal logic shown has been slightly simplified for ease of explanation without affecting the characteristics of input and output signals. Data transfer of 24-bit words into the computer can take place under control of any of the DDP input commands INM, INA, or FMB.

Note

Descriptions of command mnemonics are provided in Table 3-3.

The input drop-in pulse sets the channel ready flip-flop with a positive transition. The channel ready signal is connected to the sense matrix where it can be tested by the SKS instruction. This signal can also be connected to an interrupt line to initiate an interrupt if the input channel is connected to operate in that mode.

The channel ready signal is also available through a NAND gate to the input device as a channel busy signal. The channel enable flip-flop is set with the execution of a properly coded OCP command if not already set.

An input device select signal can be provided by the input device to be gated with the channel ready and channel enable signal. This corresponds to the input ready signal which enables the DDP input commands FMB, INA, and INM. If no input device select signal is provided, this open input acts as a TRUE signal. The 24-bit parallel inputs are DC signals which must have attained their correct level not later than 3 μsec after the trailing edge of the input drop-in pulse. A ONE level corresponds to -6 volts; a ZERO level corresponds to 0 volt. The input data transfer pulse gates the 24-bit input data through the input transfer bus onto the DDP-24 transfer bus after the channel ready and channel enable flip-flops have been set. The input data transfer pulse is of 1-μsec duration

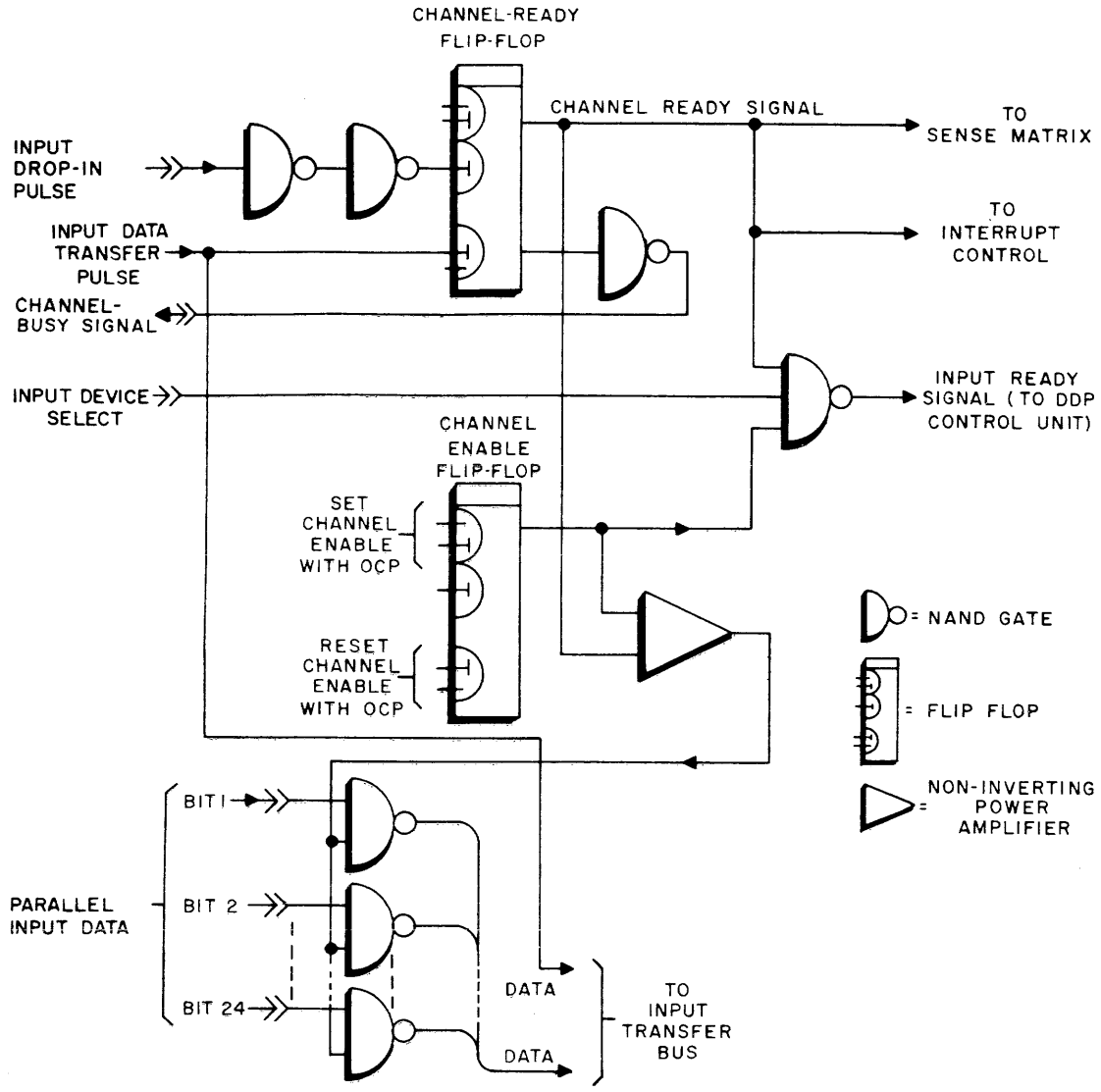


Figure 5-8. Parallel Input Channel

and is generated during the execution of either FMB, INA, or INM commands. The input levels can be removed immediately after the trailing edge of the data transfer pulse. Specifications for signals to and from parallel input channels are as follows.

Input Drop-in Pulse:

TRUE level:	-5.5 volts to -6.5 volts
FALSE level:	0 volt to -1.5 volts
Pulse specifications	5 μsec maximum rise time (90% to 10%): 0.6 μsec minimum width of the negative signal (measured from the 90% point on the falling edge to the 90% point on the rising edge); 0.25 μsec minimum width of applied logical ZERO (measured from the 10% point on the rising edge to the 10% point on the falling edge).

Input loading:	2.8 ma when driving source at 0 volt; 0 ma when driving source is at -6 volts.
Channel Busy Signal:	
ONE level:	-6 volts
ZERO level:	0 volt
Loading:	17 ma and up to 400 pf of stray capacitance
Rise time:	0.1 μsec (nominal)
Fall time:	0.15 μsec (nominal)
Input Device Select:	
TRUE level:	-5.5 volts to -6.5 volts
FALSE level:	0 volt to -1.5 volts
Input loading:	2.8 ma at 0 volt; 0 ma at -6 volts
Parallel Input Data:	
ONE level:	-5 volts to -6.5 volts
ZERO level:	0 volt to -1.5 volts
Input loading:	2.8 ma at 0 volts; 0 ma at -6 volts.

The channel ready signal is reset at the leading edge of the input data transfer pulse. The channel busy signal is reset at the trailing edge of the input data transfer pulse. This completes the input cycle and the input device can then remove the data signals from the input lines.

The channel enable flip-flop can be set at any time prior to the data transfer pulse. The data transfer pulse will be inhibited until the channel ready, channel enable, and input device select signals (if used) are set.

Timing of data inputs is illustrated in Figure 5-9. The positive transition of the input drop-in pulse sets the channel ready flip-flop; the negative transition may occur at any time, the only limitation being that it may be initiated before 0.25 μsec after completion of the positive transition and not later than 0.6 μsec before the next positive transition.

The rise time of the positive transition of the input drop-in pulse must be 5 μsec or faster. Input data are DC levels. Any level transition must be completed not later than 3 μsec after initiation of the positive transition of the input ready pulse.

5-6 PARALLAL OUTPUT CHANNELS

The block diagram of the parallel output channel, Figure 5-10, shows the output of parallel data. It is similar to the parallel input channel.

The output device places an AC positive transition on the output busy line which, in turn, sets the channel ready flip-flop. The channel ready signal is used similarly as in the parallel input channel. It is connected to the sense matrix and to the interrupt control (if operating in interrupt mode). The channel ready signal is also available to the output device as a channel busy signal.

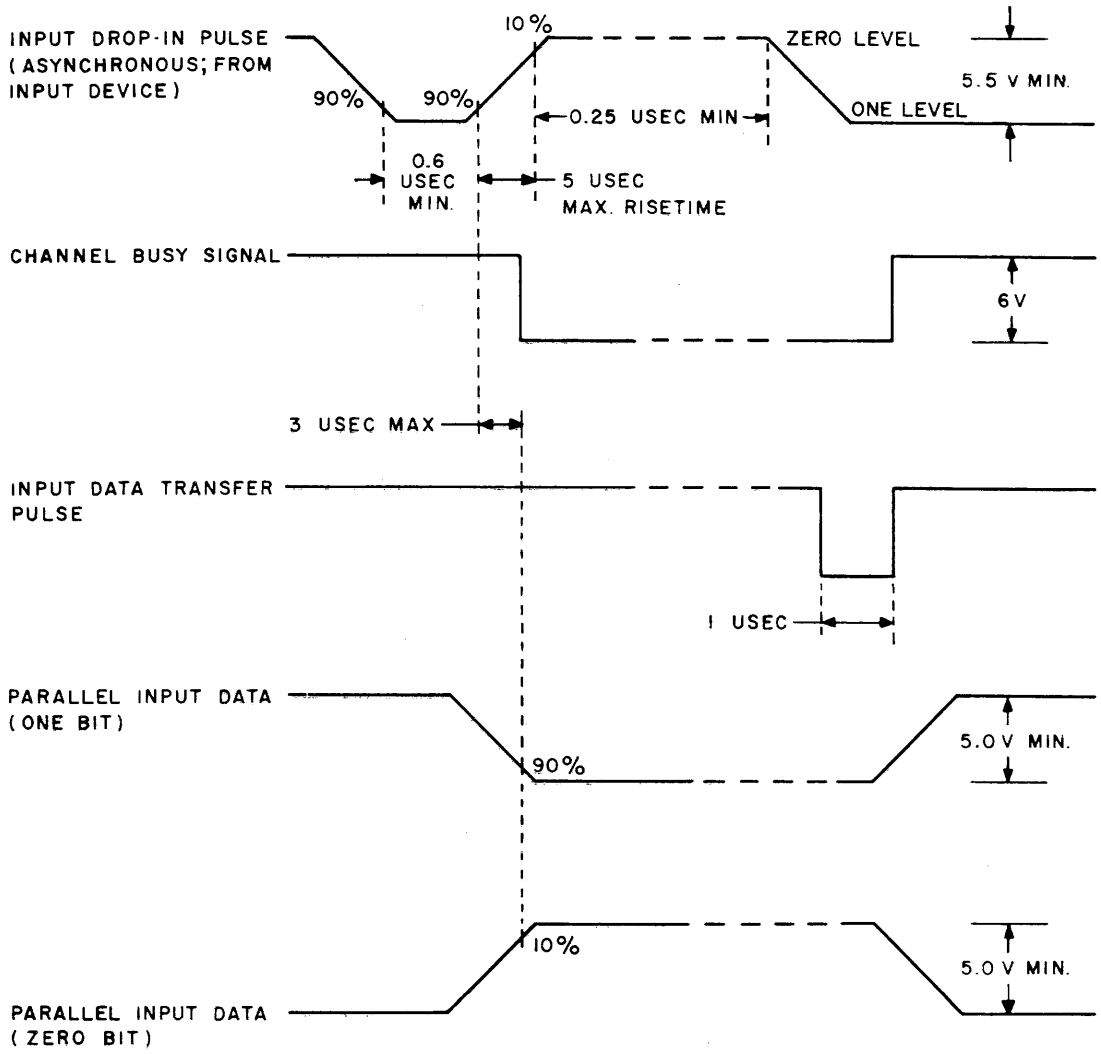


Figure 5-9. Parallel Input Channel Timing Chart

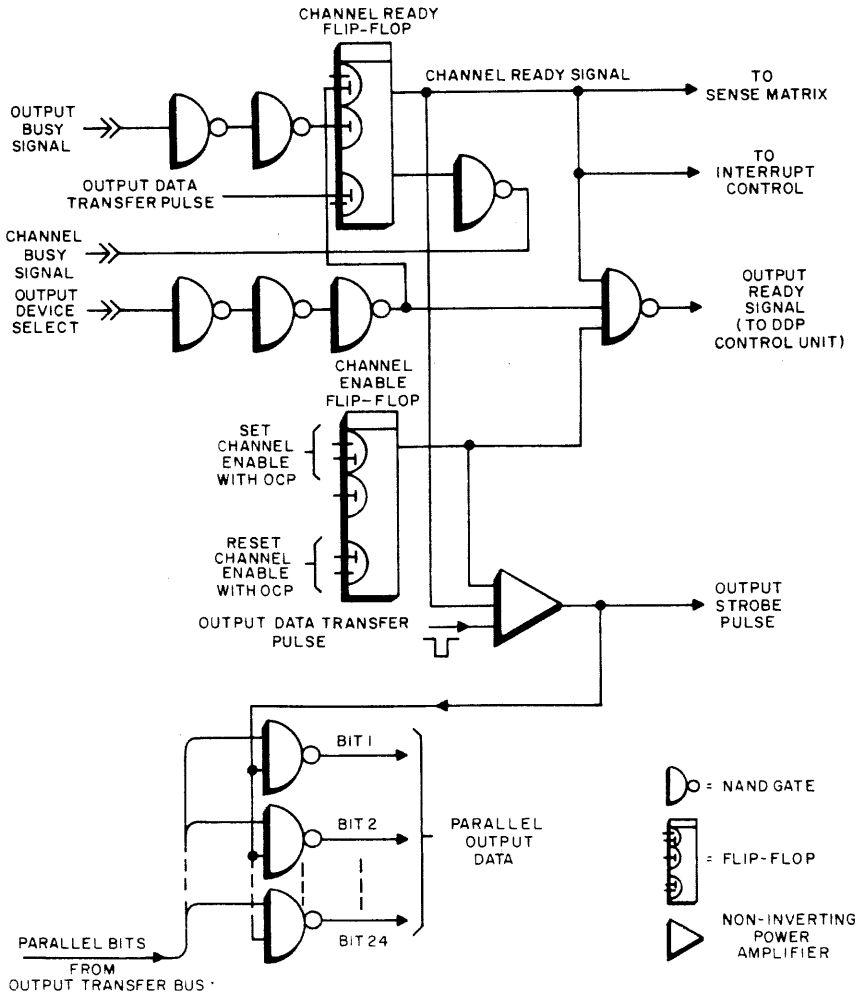


Figure 5-10. Parallel Output Channel, Block Diagram

The channel enable flip-flop, if not already set, is set with the execution of an OCP command. An output device select signal sets the channel ready flip-flop when it changes to the TRUE level and resets this flip-flop when it returns to the FALSE level (not shown in Figure 5-10). This feature is specifically required if the output channel operates in the interrupt mode. The data transfer pulse (1 μsec) is generated during the execution of an output command (DMB, OTA, or OTM) and is gated with the channel ready, channel enable, and device select signals. The output data transfer pulse is gated with the parallel bits from the output transfer bus. The output data consists of 1-μsec, positive-going pulses for ZERO bits, or -6-volt DC levels for ONE bits.

At the trailing edge of the output data transfer pulse, the channel ready flip-flop is reset, and the channel busy signal becomes false. (See Figure 5-11.) This action completes the output cycle.

The timing diagram for the parallel output channel, Figure 5-11, illustrates the timing relationships between the signals. After the output busy signal has enabled the setting of the channel ready flip-flop (and output channel busy signal), the output data pulses will take place at least 4 μsec later. This minimum interval will occur if the execution of the output command had been blocked by the reset channel ready signal.

The specifications for the signal parallel output channel are as follows.

Output Busy Signal:

TRUE level:	-5.5 volts to -6.5 volts
FALSE level:	0 volt to -1.5 volts
Pulse specifications:	5 μsec rise time (90% to 10%); at least 0.6 μsec width of the negative signal measured between 90% points on falling and rising edge;
	0.25 μsec width of applied logical ZERO, measured between 10% points on rising and falling edge.
Input Loading:	2.8 ma when driving source is at 0 volt; 0 ma when driving source is at -6 volts.

Output Channel Busy:

ONE level:	-6 volts
ZERO level:	0 volt
Loading:	17 ma and up to 400 pf of stray capacitance
Rise time:	0.1 μsec (nominal)
Fall time:	0.15 μsec (nominal)

Output Device Select:

TRUE level:	-5 volts to -6.5 volts
FALSE level:	0 volt to -1.5 volts
Rise time:	5 μsec max. (90% to 10%)
Input loading:	2.8 ma at 0 volt, 0 ma at -6 volts.

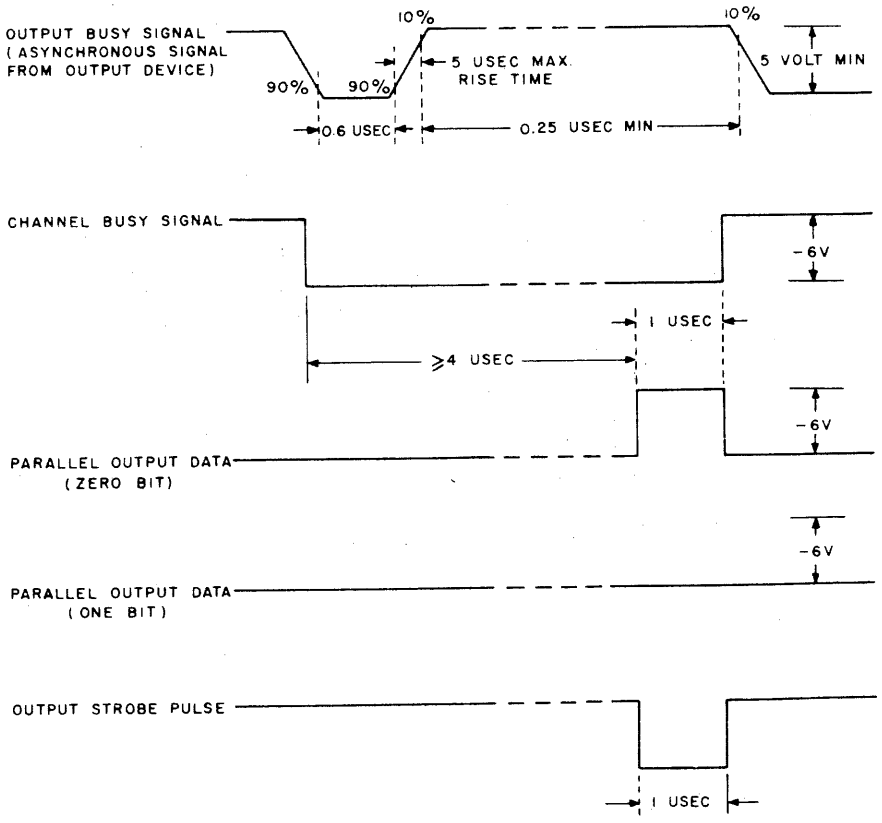


Figure 5-11. Timing Diagram for Parallel Output Channel

Output Strobe:

ONE level:	-6 volts
ZERO level:	0 volt
Waveform width:	1 μsec
Rise time:	0.1 μsec (nominal)
Fall time:	0.15 μsec (nominal)
Loading:	40 ma and up to 1500 pf of stray capacitance

Output Data:

ONE level:	-6 volts
ZERO level:	Positive pulse between -6 volts and 0 volt

Output Waveform:

Rise time:	0.1 μsec (nominal)
Fall time:	0.15 μsec (nominal)
Width:	1 μsec
Output loading:	17 ma and up to 400 pf of stray capacitance.

5-7 CHARACTER BUFFER

One 6-bit character buffer is provided for both input and output characters. The character buffer includes a 6-bit flip-flop register, an input channel and an output channel, parity detection for inputs, parity generation for outputs, a stop-code flip-flop, a character input-ready signal, a character output-ready signal, a character buffer input enable flip-flop, and a character buffer output enable flip-flop. Odd parity is used, except for the typewriter which does not have parity. The stop-code flip-flop is set either by a stop code from the paper tape or the typewriter keyboard and can be tested by the SKS command. The typewriter, paper-tape reader, and paper-tape punch are normally connected to the input-output character buffer.

Additional character buffers, to allow several character devices to operate simultaneously, are optional. These may be either for character inputs, character outputs, or both. An overall input parity signal is provided when additional input character buffers are used. The signal operates the control panel parity light.

5-8 BUFFERED INPUT-OUTPUT CHANNELS

Figure 5-12, the general block diagram of the buffered input-output channel, applies to either character buffers or optional buffered parallel channels for 24-bit input and/or output. The channel ready, channel enable and buffer flip-flops as well as the input and output gates are shown. Several input-output devices may be connected to the buffer, but only one device per buffer may be operating at a time. The buffer may be used for input or output, but not for both simultaneously. The drop-in pulse (for the input devices) or the output busy pulse (for output devices) sets the channel ready flip-flop with an AC positive transition. For output devices the channel ready signal should be turned on only when the device itself has been properly selected and enabled.

The channel-ready flip-flop is connected to the sense matrix, to the control unit of the DDP processor, and to the interrupt control (if wired in). The channel-ready flip-flop output is also made available to the input-output device(s) as a channel busy signal.

The channel-enable flip-flop is set by the execution of an OCP command if not already set; it is reset when another channel-enable flip-flop is set.

Data transfer pulses for either input or output are generated as in the parallel input or output channels and are gated with either one of the input or output commands. Input data is gated with the input device drop-in pulse and, in turn, sets the flip-flop buffer with its positive transition trailing edge. Output data is read from the buffer flip-flops through NAND gates.

The channel ready flip-flop is reset with the positive transition (trailing edge) of either one of the data transfer pulses.

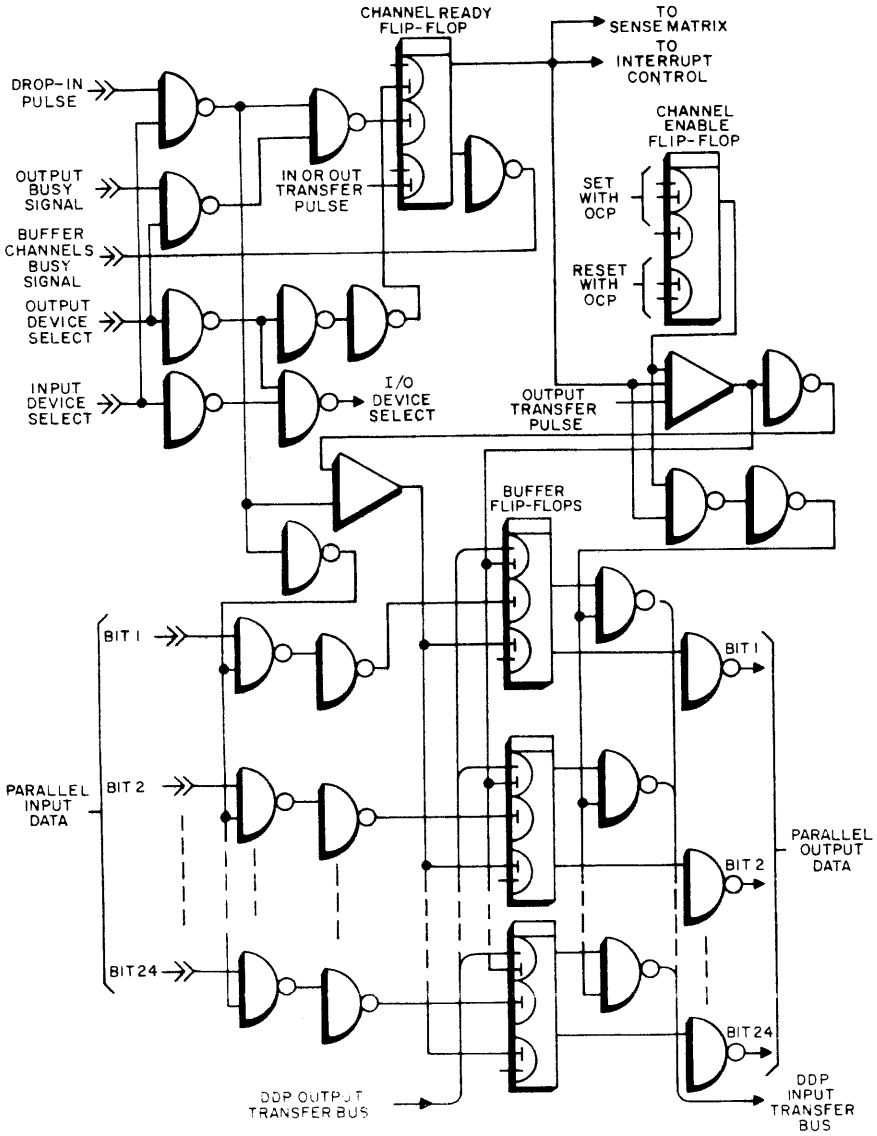


Figure 5-12. Buffered Input-Output Channel, Block Diagram

Only one device per buffer can be operating at one time. It is possible to select another device on a buffer and thereby switch off the one previously selected. To avoid losing any information that might have been stored in the buffer flip-flops, the switching off of an input-output device can take place only under certain conditions. An output device can be switched off only when the channel ready flip-flop is set; an input device can be switched off when the channel ready flip-flop is reset (the channel ready flip-flop corresponds to the input-output channel busy signal).

An interlock in the control logic for the standard input-output devices connected to the DDP-24 character buffer allows selecting and switching off of the devices only when permitted. The buffered channel-ready flip-flop is reset when an output device is switched off (not shown in Figure 5-12) and is set when an output device is selected. In general, the channel ready flip-flop can be connected to the interrupt control of the DDP-24, but with more than one character device on a buffer, it is also possible to connect proper signals from any of the devices to an interrupt line. This allows the operation of devices in both ready and interrupt modes on the same channel. (But still only one device per channel can operate at a time.)

The timing diagram, Figure 5-13, shows waveforms and timing specifications of the signals between buffered channels and input-output devices. Signal characteristics are similar to those of the nonbuffered input and output channels as follows.

Input Drop-In and Output Busy Signal:

TRUE level:	-5.5 volts to -6.5 volts
FALSE level:	0 volt to -1.5 volts
Pulse specifications:	5 μsec maximum reset time; 0.6 μsec minimum width of negative signal; 0.25 μsec minimum width of ZERO level.
Input loading:	2.8 ma at 0 volt and 0 ma at -6 volts

Buffer Channels Busy Signals:

ONE level:	-6 volts
ZERO level:	0 volt
Loading:	17 ma and up to 400 pf of stray capacitance
Rise time:	0.1 μsec (nominal)
Fall time:	0.15 μsec (nominal)

Input Device Select Signals:

TRUE level:	-5.5 volts to -6.5 volts
FALSE level:	0 volt to -1.5 volts
Input loading:	2.8 ma at 0 volt; 0 ma at -6 volts.

Input Data Signals:

ONE level:	-5 volts to -6.5 volts
ZERO level:	0 volt to -1.5 volts
Input loading:	2.8 ma at 0 volt; 0 ma at -6 volts.

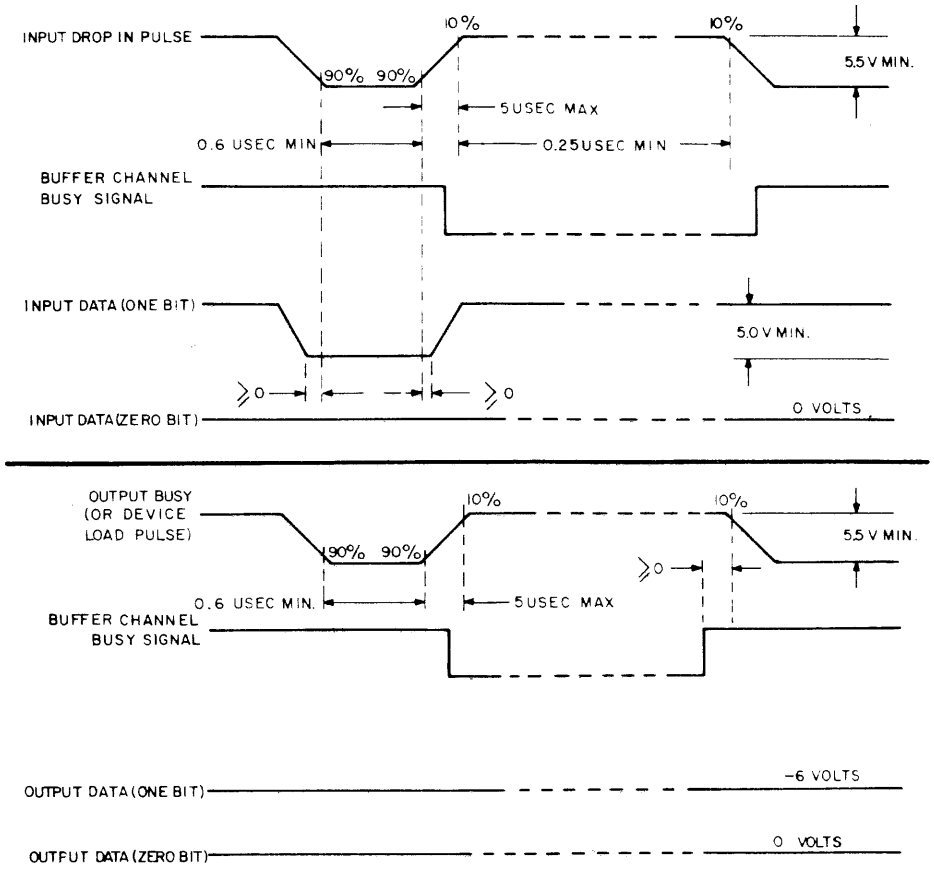


Figure 5-13. Timing Diagram For Signals Between Input-Output Devices And Buffered Channels

Output Device Select Signals:

TRUE level:	-5 volts to -6.5 volts
FALSE level:	0 volt to -1.5 volts
Rise time:	5 μsec maximum (90% to 10%)
Input loading:	2.8 ma at 0 volt; 0 ma at -6 volts.

Output Data Signals:

ONE level:	-6 volts DC
ZERO level:	0 volt
Output loading:	17 ma and up to 400 pf of stray capacitance.

In the character buffer, input-output data transfer takes place for six bits only. In addition, the character buffer provides odd parity detection for input characters and odd parity generation for output characters. It also provides stop code detection and generation. The characteristics of the single-bit parity signals and stop code signals for input or output are identical to those for the data bits.

5-9 AUTOMATIC INTERRUPT

Any standard parallel channel or character buffer is capable of operating either in the automatic interrupt or ready mode under control of a jumper in the input-output section.

In the interrupt mode, the computer program is automatically interrupted when a channel is ready to transfer data. Branching to the proper subroutine takes place automatically while the contents of the program counter at interrupt are stored. On completion of the interrupt subroutine, the main program resumes at the interrupted point. In the ready mode, the program tests for the channel-ready signal with periodic SKS commands. If the ready signal is not present, the computer program proceeds with the current routine and later repeats the test. The program may also branch into a test loop until the ready signal is available. If the test of the ready signal is successful, the program will transfer to the input or output subroutine.

The overflow flip-flop and the improper divide flip-flop can be connected to initiate an interrupt when set. The circuit for power failure protection will generate an interrupt if power falls below a threshold value.

The DDP-24 is equipped with four interrupt destinations. If an interrupt is initiated by either of the two parallel channels, character input or character output, an automatic program jump takes place to a different memory location, depending on the channel. The fourth interrupt destination is shared by the character buffer out, the overflow flip-flop, and the improper divide flip-flop. If several channels with different destinations cause an interrupt at the same time, a preassigned priority prevails. Interrupt from a channel with a high-order priority is recognized first.

Interrupt lines, each with a unique destination, can be added for additional I/O channels in the automatic interrupt mode. Up to 32 lines and destinations are standard options with the DDP-24.

In the standard processor, additional interrupts will be inhibited during the execution of an interrupt subroutine. A second interrupt is handled immediately after completion of the current subroutine. The interrupt inhibit flip-flop is reset by the execution of a JRT command. Any subroutine which may be part of an interrupt subroutine must not use a JRT command for subroutine return but must use an indirectly addressed JMP instruction.

An automatic priority control system can be added. This system permits assignment of up to 8 levels of priority to input-output channels and/or parts of the main program. An interrupt by an input or output channel will occur when its priority is higher than the program in progress. (Refer to paragraphs 5-15 and 5-16.)

If an interrupt occurs while the computer is in HALT condition, the interrupt subroutine will be executed as normal and, upon completion, the computer will return to HALT again with the same value in the program counter as before.

The transfer rate for channels operating in the interrupt mode depends on the length of the input-output subroutine. For a channel in the automatic interrupt mode, transfer rates over 25,000 words per second are possible. Interrupt lines can be provided to interrupt the computer program without the transfer of data, such as with an alarm condition. The interrupt capability of the DDP can be either enabled or inhibited by the TIC command while the master clear button on the control panel will disable the interrupt to prevent runaway conditions.

5-10 INPUT-OUTPUT DATA TRANSFER

The computer will operate with many peripheral devices connected to its standard input-output channels or to optionally added channels.

In general, more than one input or output device may be connected to an input or output channel. However, not more than one device per channel should be operating simultaneously. For simultaneous operation of several independent devices, a corresponding number of input or output channels should be provided; however, simultaneous output to the paper-tape punch and typewriter via the standard I/O character buffer is possible.

When an input-output device is ready for data transfer, it sets the ready flip-flop of the channel to which it is connected. If in ready mode, the computer may detect this condition with a periodic SKS instruction (Figure 5-14) as part of the main program. If in interrupt mode, this SKS instruction is not necessary unless more than one channel could cause an interrupt to the same destination. The input-output subroutine will enable the channel by setting the enable flip-flop with the properly coded OCP command.

The four functional groups of input-output data channels are input channels in ready mode, input channels in interrupt mode, output channels in ready mode, and output channels in interrupt mode. The enabling of a channel automatically resets any other enable flip-flop in the same group of channels.

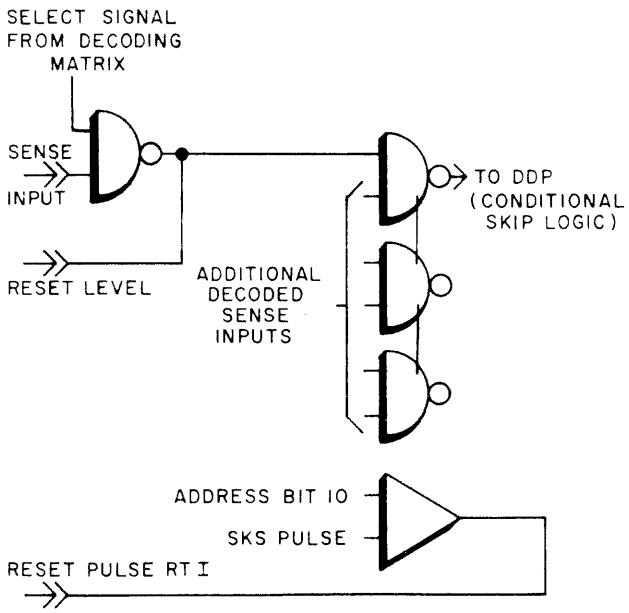


Figure 5-14. Typical Sense Line Input

After enabling the desired channel with an OCP command, the data transfer is accomplished with either INM (Input to Memory), INA (Input to A), OTM (Output from Memory), OTA (Output from A), FMB (Fill Memory Block) or DMB (Dump Memory).

These commands allow for direct input-output data transfer into or from any memory location, or into or from the A register. The latter is important if further handling of the input-output data is required.

The DDP program may command a data transfer with INA, INM, OTA, OTM, FMB or DMB without testing for the ready signal of the enabled channel. If the ready signal is not true, the command waits until it becomes true. These input-output commands reset the ready flip-flop of the enabled channel.

The address portion of the INA and OTA commands may be used as a mask for characters of up to 6 bits if the most significant bit of the address portion is a ONE. This provides for easy and flexible formatting. With the INA command, ZERO bits in the mask will leave the corresponding bits in A unchanged; a ONE mask bit will enter the corresponding input bits into A. With the OTA command, ZERO mask bits will produce corresponding ZERO bits in the output; for a ONE mask bit the corresponding bits in A appear as output bits.

The following is a typical subroutine for the input of a block of data from an input channel in the interrupt mode.

Location	OP-code	Address	Time (microseconds)
	Interrupt JST	00002	7
00003	JMP	a	5
a	INM	indexed address	10
a + 1	JXI	b	7
b	JRT	00002	10
			39 total

Upon interrupt, the contents of the program counter (P) are automatically stored, typically in memory location 00002 (octal notation), and the following command is executed from location 00003. The indicated execution time of 7 μsec for interrupt includes the automatic storing of (P). The INM command stores the input in the specified memory location. JXI increments the contents of the index register, and if not yet zero, a conditional jump will take place to the location where a JRT command is stored. This will effect the return to the main program where it had been broken by the interrupt. Total execution time of the interrupt subroutine is 39 μsec, corresponding to a data transfer rate of over 25,000 words per second. It has been assumed that only one input channel is operating in the interrupt mode. Therefore, the channel enable flip-flop can be set and remain set

beforehand. (This is not part of the subroutine.) In this example, the index register is used only for the input routine. If the index register contents have become ZERO, further inputs from the external device are to be prevented by proper commands. The JRT command will terminate the subroutine in the same way.

5-11 BLOCK TRANSFER

Block transfers are possible on any input or output channel with the standard commands FMB (Fill Memory Block) and DMB (Dump Memory Block). During execution, these commands enter or dump information in successive memory locations, directly and synchronously with the external device, until an external stop signal is given or a limit location is reached. No other instructions will be executed while an FMB or DMB is in process. The maximum transfer rate is 16,700 words per second.

The FMB or DMB commands can be used with any enabled input or output channel, and they are efficient for communicating with high-speed devices such as other computers, magnetic discs, drums, and others.

5-12 WORD-FORMING BUFFERS

Optional word-forming buffers for both input and output are available. These buffers permit the automatic building of a computer word from input characters, and the forming of output characters from a computer word.

The buffer, composed of a 6-bit character buffer, a 24-bit flip-flop register, and a buffer control, controls the following:

a. The number of characters per word (either 2, 3 or 4),

b. The shifting of information in the flip-flop register for the character output or input,

c. The buffer ready signal, and

d. The checking or generation of character parity.

In the interrupt mode, the possible character transfer rate is doubled and the I/O processing time is decreased by a factor of four. A word buffer may be connected to the DDP-24 with a parallel input channel and/or parallel output channel; a DMA channel, or an FBC channel.

5-13 FULLY BUFFERED CHANNEL (OPTIONAL)

The fully buffered channel (Figure 5-15) permits an external input-output device to communicate directly with up to two 4096-word memory modules for transfers of data at very high speed. Once set up and enabled by the computer program, the address of the sequential memory locations to be accessed is supplied by the FBC independent of the

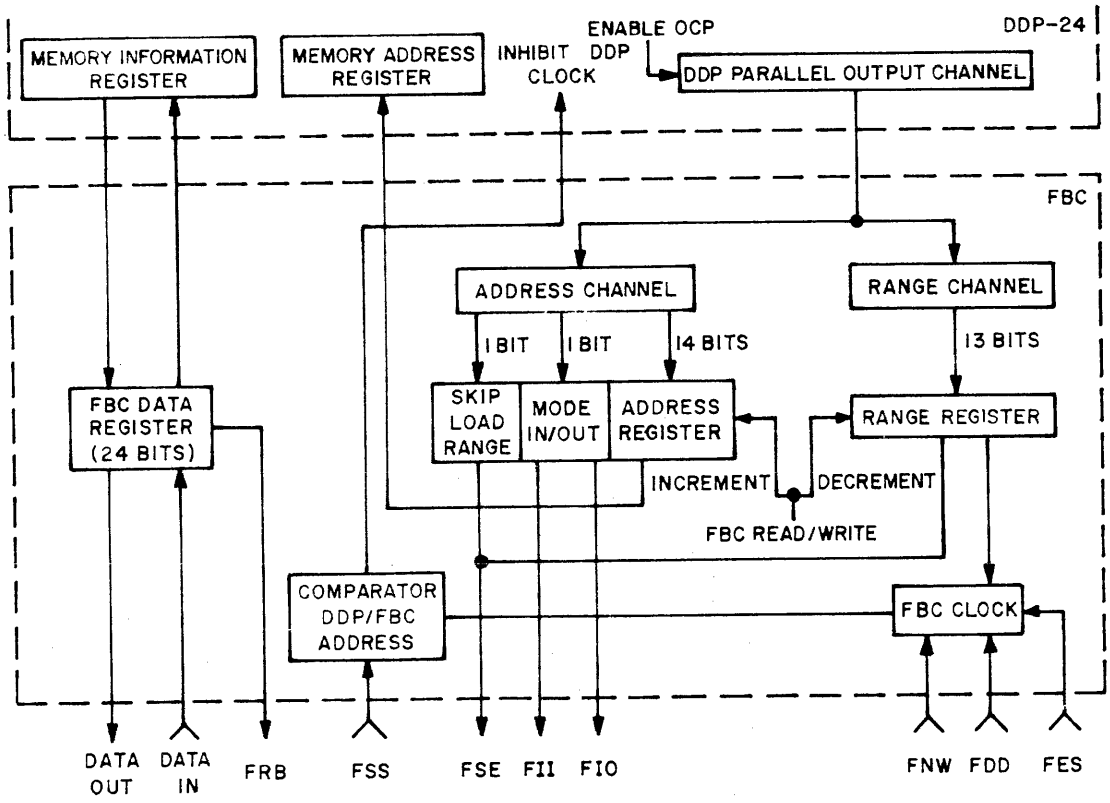


Figure 5-15. Fully Buffered Channel, Block Diagram

computer program. In case the fully buffered channel and the computer program both address the same memory module, the fully buffered channel operates in a direct memory access mode (memory cycle stealing).

The maximum transfer rate of the channel is 166 KC. When the channel operates in a DMA mode the computer program will be fully interrupted for rates higher than 83 KC. The FBC consists of a 24-bit data register for buffering of input-output data, a 14-bit address register controlling addressing of the memory, and a 13-bit range register providing a limit to the block transfer, an operational mode flip-flop, and the FBC clock. Included are various control circuits, some of which are used internally to the FBC and others used in the coupling of the FBC to the external device. The FBC is set up initially by the DDP-24 by way of a regular parallel output channel that can be either the standard or any optional parallel output channel. This channel is not included within the FBC proper.

Under program control, a parallel output channel for address and range setup is first enabled with an OCP command. The computer program then loads the FBC address register and operational mode flip-flop with an OTM command. (Bit 1, the signbit of this OTM word, specifies the input mode of operation if ZERO, and the output mode if ONE.) The range register is then loaded with a second OTM instruction. When bit 2 (the bit next to the sign) of the first OTM word transferred by the computer program is ONE, the

second OTM is not necessary, and the range register will be loaded with all ONEs. The start address is 14 bits, and the range register is 13 bits. Therefore the FBC can address up to 8192 memory cells starting with the initial address in the FBC address register. (Variations of the regular FBC allow addressing 12,288 and 16,384 memory cells.)

Note

The FBC will address memory modules sequentially and does not have a wrap-around capability.

The FBC address register is incremented with a ONE and the range register is decremented with a ONE after a memory read or write cycle is initiated. When the total number of words specified in the range register has been transferred from or to the FBC, the channel will be disabled, and no further words will be transferred. Any memory location within the two 4096-word memory modules addressable by the regular FBC can be the start address and the stop address for the block transfer. The start address must always be in a lower memory location. The FBC can be disabled with an external stop signal. A power failure in the DDP-24 system will also disable the fully buffered channel.

Eight control lines are used between the FBC channel and the external device. A short description of each is provided below.

FSE: This is the FBC start enable pulse generated by the FBC after the address and range registers have been properly loaded. Its trailing edge can be used to start a device. Signal specifications are: negative-going NAND gate output pulse between -6 volts and 0 volt; 1 μsec wide; rise time of 0.1 μsec (nominal); fall time of 0.15 μsec (nominal), and output loading of 17 ma with stray capacitance of 400 pf.

FII: A flip-flop level indicating that the FBC is in the input mode if TRUE (reading from the external device to the memory). The FII flip-flop is set when the range and address registers have been loaded if the sign bit of the first OTM word was a ZERO. The FII flip-flop is reset by a stop signal from the external device, by a power failure interrupt of the DDP-24, or upon reading the number of words specified by the range register. Signal specifications are: negative-going NAND gate output pulse with TRUE level of -6 volts and FALSE level of 0 volt, and output loading of 17 ma with stray capacitance of 400 pf.

FIO: A flip-flop level indicating that the FBC is in the output mode if TRUE. The FIO flip-flop is set after the address and range registers have been loaded if the sign bit of the first OTM word was a ONE. It is reset by a stop signal from the external device, by a power failure interrupt of the DDP-24, or upon reading the number of words specified by the range register. Signal specifications are the same as for FII.

FRB: This is the FBC data register busy flip-flop which is set in the output mode when the FBC initiates a read memory cycle, and in the input mode when the buffer register contains a new word from the external device. It is reset in the output mode as soon as the buffer register has been refilled with information or in the input mode after the contents of

the FBC register have been transferred into the memory. Signal specifications are the same as FII.

FNW: The read-next-word pulse from a device during the output mode. Its trailing edge sets the FBC demand flip-flop. Signal specifications are: negative-going pulse with TRUE level of -5.5 volts to -6.5 volts and FALSE level of 0 volt to -1.5 volts; 0.6 μsec minimum width and 3 μsec maximum width of the TRUE signal (between 90% points); 4 μsec minimum width of the FALSE signal (between 10% points); maximum rise and fall time of 5 μsec (between 10% and 90% points); input loading of 2.8 ma at 0 volt, and 0 current at -6 volts.

FDD: The drop-in pulse from a device during the input mode. It sets the FBC demand flip-flop and FRB flip-flop after information has been transferred into the FBC data register. FDD is a negative-going pulse with the same signal specifications as the FNW. In addition the drop-in pulse cannot be any wider than 1/5 of the cycle, in μsec, at maximum operate speed of the external device.

FES: The external stop signal given by a device that resets FIO or FII, thereby disabling the FBC data channel and preventing any further data transfer. FES is a negative-going pulse with the same signal specifications as the FNW and FDD signals.

FSS: A pulse generated by an input-output device during the fast input mode (speed of device greater than 83 KC), the trailing edge of which occurs at least 7 μsec before the first drop-in pulse. (Any delay greater than 7 μsec can interrupt the computer for the same amount of time.) This pulse enables a comparison circuit that checks that the FBC is in a DMA mode and ensures that the first word from the device will be transferred. FSS is a negative-going pulse with the same signal specifications as the FNW.

The FBC interrogates the address information contained in the program counter and in the effective address of the computer and inhibits the computer clock if both the FBC and the computer try to access the same memory module at the same time. The FBC operates then as in a direct memory access (DMA) mode. The computer clock will be inhibited if an operand access is to be processed or before an instruction is fetched while the FBC seeks access to the same memory module. The inhibit signal will be released after the FBC completes its memory access. The FBC in the DMA mode does not lock out the DDP-24 during the performance of the portion of a long operation cycle that does not require a memory access. A fast and a slow mode of operation are possible for the FBC in the DMA mode under the control of a jumper wire. The fast mode is required if transfer rates higher than 83 KC occur. During the fast mode of operation with transfer rates between 83 and 166 KC, the computer will not be able to gain access to the FBC memory module for 12 μsec after the last FBC demand, in which case the program will be fully interrupted. In the slow mode of operation (less than 83 KC) the computer program will only be inhibited for 5 μsec (FBC memory access).

The DDP program counter and effective address are compared for at least 10 μsec before the FBC address approaches the first location in the next sequential memory module. If the DDP tries to gain access to the module that the FBC will address, the computer clock will be fully interrupted for up to 10 μsec, and after this time the FBC will be in a DMA mode.

Any of the DC level signals may be tested by the computer with the SKS instruction using a regular sense line. (Sense lines not included with the FBC.)

If an interrupt occurs in the computer program after processing the first OTM or in the initial OCP during setup of the FBC, the parallel output channel of the computer will be disabled. The FBC will wait until the interrupt is completed and the channel has been returned to the enabled state. After the initial setup, an interrupt has no effect on the FBC.

5-14 DIRECT MEMORY ACCESS CHANNEL

The direct memory access (Figure 5-16) channel operates in the same way as the FBC when it addresses the same memory module as the DDP-24 program. The DMA channel always has priority access to memory over the DDP-24, but any current memory access by the computer (whether for command fetch or operand access) must be completed first. While the DMA has access to the memory, the DDP is inhibited if it requires memory access. This is independent of any different memory module addressing by DMA and DDP.

Two operation modes are possible for DMA under control of a jumper wire - a fast mode for data transfer rates of more than 83 KC in which each DMA memory access will inhibit DDP memory access for 12 μsec and a slow mode for data transfer rates below 83 KC in which each DMA memory access inhibits DDP memory operation for only 5 μsec.

The DMA channel is set up with address and range information exactly as the FBC. It contains a 24-bit buffered data register, a 14-bit address register, a 13-bit range register, an operational mode flip-flop, and the DMA clock. The DMA can address any of the 16,384 memory locations, and transfers of up to 8192 word blocks are possible. As with the FBC, no wrap around addressing is possible, except when 16,384 memory locations may be addressed. The control lines between DMA and the external device are quite similar to signals of the fully buffered channel as follows.

DSE DMA start enable pulse.
Signal specifications same as for FSE.

DII DMA input mode level.
Signal specifications same as for FII.

DIO DMA output mode level.
Signal specifications same as for FIO.

DRB DMA register busy level.
Signal specifications same as for FRB.

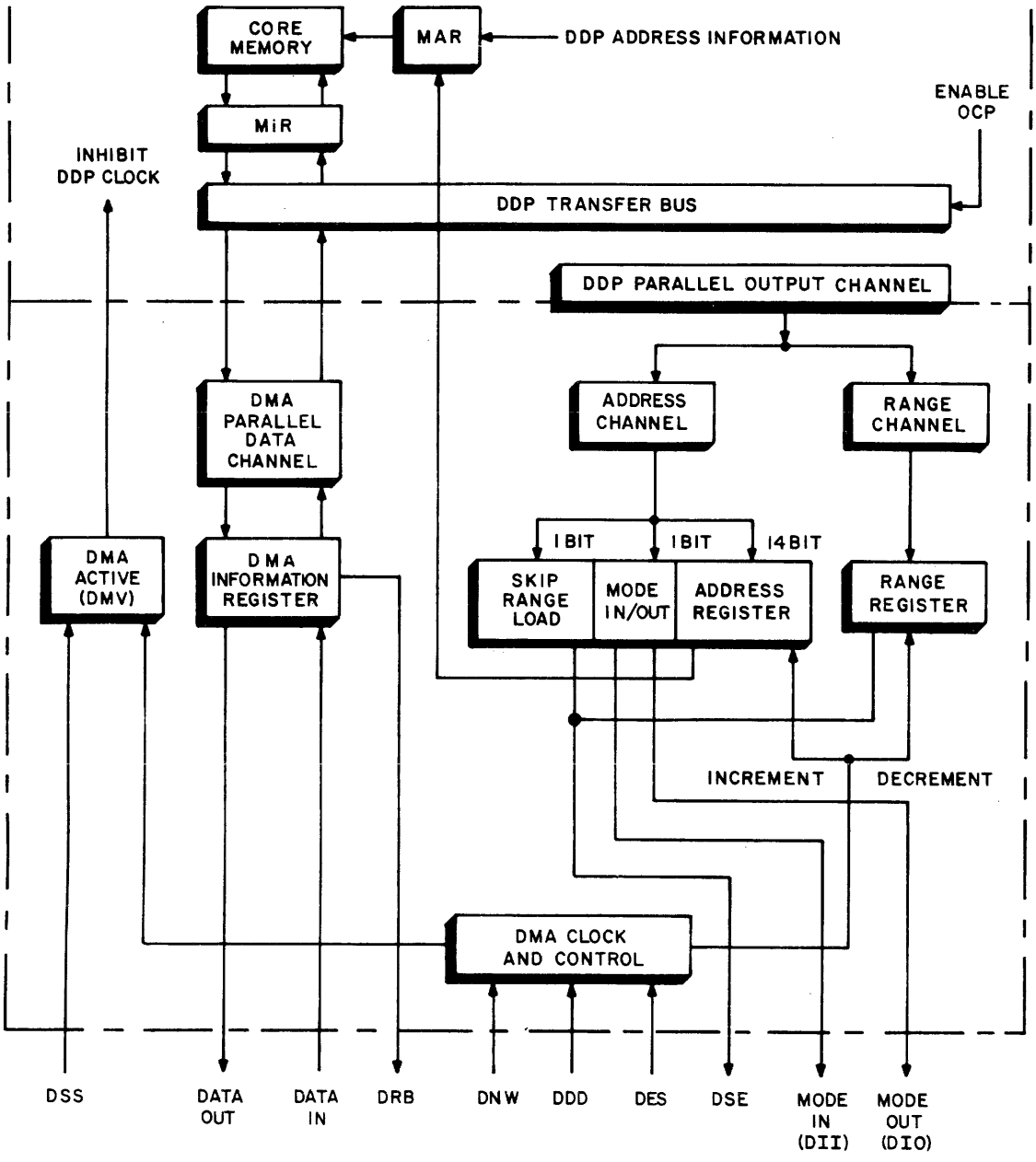


Figure 5-16. Direct Memory Access Channel, Block Diagram

DNW DMA read next word pulse.
Signal specifications same as for FNW.

DDD DMA drop-in pulse.
Signal specifications same as for FDD.

DES DMA external stop pulse.
Signal specifications same as for FES.

DSS DMA fast mode alert pulse.
Signal specifications same as for FSS.

5-15 PRIORITY INTERRUPT (OPTIONAL)

The optional priority interrupt system allows 8 levels of interrupt priority to be assigned to input-output channels and parts of the computer program itself. Any 4 of the 8 levels may be used for different sections of the program. Jumpers are used to assign levels of interrupt priority to I/O channels. The assignment of priority levels to parts of the main program is accomplished by properly coded OCP commands in that program. Several I/O channels or parts of the main program may have the same priority levels.

The Priority Interrupt System allows for automatic interrupts of the computer program or routine only if the requesting priority level of the I/O channel-ready for data transfer is higher than the current priority level of the I/O subroutine or main program. If a requesting priority level is lower than or equal to the current priority level, an interrupt must wait until the latter has returned to a lower level.

If an interrupt is allowed, a program transfer will be effected to a memory location unique to the interrupting I/O channel, as in the standard DDP-24. From there the proper interrupt subroutine will be executed. The end of the interrupt subroutine execution of the JRT-command effects automatic return to the priority level which existed before the interrupt occurred.

5-16 INTERRUPT LINES

Four interrupt lines are standard with the DDP-24. This number can be expanded optionally to 32. A TRUE DC signal on an interrupt line will cause an interrupt of the computer program if the interrupt enable flip-flop is set. Upon completion of any current DDP-24 command, a program jump is made to an interrupt destination which is unique to the interrupt line. The contents of the program counter, the coded number of any enabled input-output channel, and the state of certain internal flip-flops are stored in memory.

During interrupt subroutines no further interrupts can be made. Therefore, upon return from an interrupt subroutine several new interrupt requests may have accumulated. A lockout or priority-on-stacking feature is provided in the standard DDP-24 so that only one interrupt line will cause a new interrupt. The priority-on-stacking is set up according to a preassigned priority, rather than a priority in order of occurrence. The interrupt request signals on the interrupt signal must be DC levels, lasting at least until they are honored.

Four interrupt lines L_0, L_1, L_2, and L_3 are standard parts of the DDP-24 with respective interrupt jump locations 00001, 00003, 00005, 00007. The program counter contents and other information are automatically stored at 00000, 00002, 00004, and 00006, respectively. Interrupt line L_0 has the highest interlock priority; next highest is L_1, then L_2, and finally L_3.

The four interrupt lines of the standard DDP-24 are connected as follows.

a. Line L_0, interrupt destination 00000, power failure circuitry.

Note

The wiring is such that upon power restoration a start signal is provided which restores the register contents by program. If this feature is not desired, the wire should be removed.

b. Line L_1, interrupt destination 00002, character buffer

c. Line L_2, interrupt destination 00004, parallel channel in

d. Line L_3, interrupt destination 00006, parallel channel out

Note

To prevent the parallel output channel from initiating interrupt when no device is connected to it, the device selection signal for that channel is to be grounded with a jumper wire on connector J-155. (Refer to wiring charts for specific terminations.)

Any proper DC signal can be connected to an interrupt line. Typical possible connections are power failure detection, input-output channel ready flip-flops, overflow, improper divide, and parity flip-flops. Figure 5-17 shows the basic gating for the interrupt inputs. The interrupt input signal must be on for at least the time that it takes to start the interrupt subroutine, plus 3 μsec.

The interrupt routine must be terminated with a JRT command. This will not only restore the program counter to the location following the point of interrupt, but will also restore the channel enable and the other internal flip-flops and reset the interrupt flip-flop. The interrupt signal that caused the interrupt should be turned off by the end of the interrupt routine. Channel ready flip-flops that may cause interrupts are reset with the input or output command (either INA, INM, FMB, or OTA, OTM, DMB). Signals that are also connected to sense lines generally can be reset with the SKS command. The interrupt signal specifications are as follows.

TRUE level:	-5.5 volts to -6.5 volts
FALSE level:	0 volt to -1.5 volts
Waveform:	3 μsec maximum rise and fall time (between 10% and 90%)
Input loading:	2.8 ma at 0 volt; 0 ma at -6 volts.

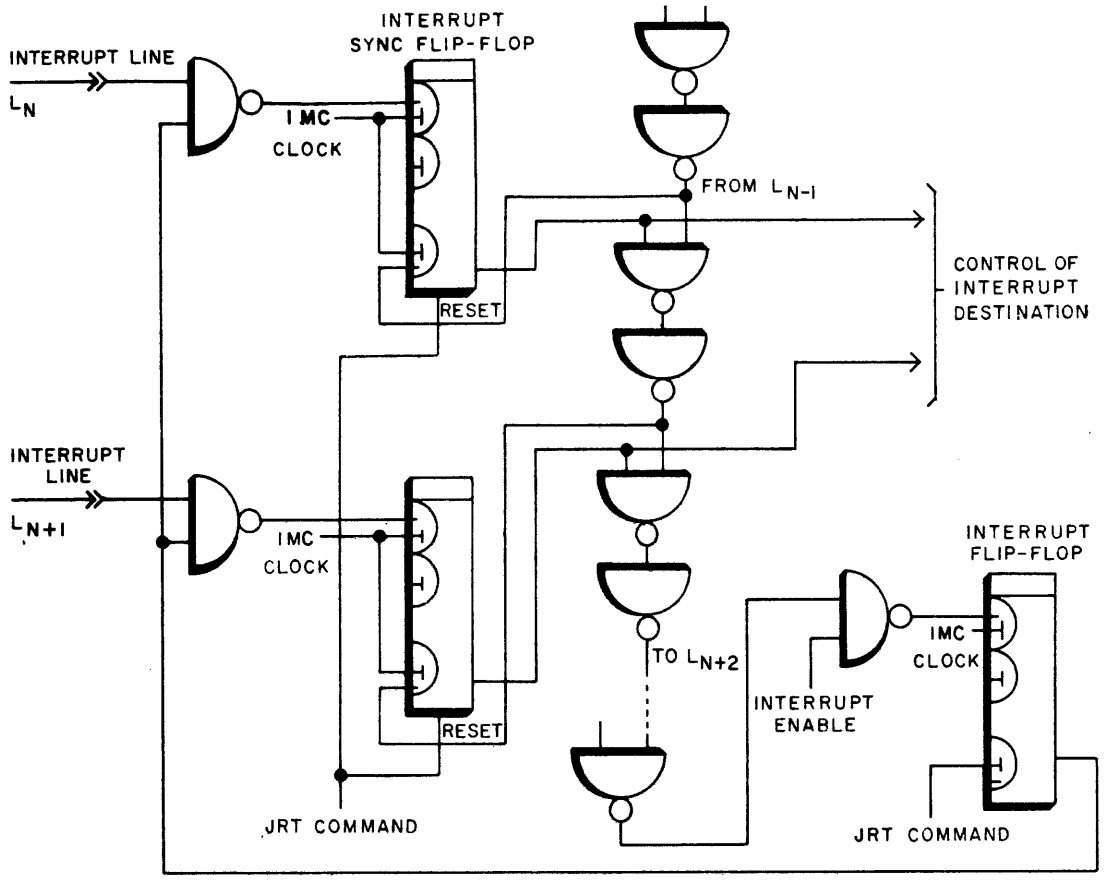


Figure 5-17. Interrupt Lines, Block Diagram

5-17 INPUT-OUTPUT TYPEWRITER

The DDP-24 input-output typewriter can be used as a regular typewriter or as an input-output device. The typewriter is compact, light-weight, and uses a new principle of printing. A spherical type head moves along the writing line while the carriage remains stationary. The typewriter will print 15 characters per second and can be used with the DDP-24 off-line as well as on-line.

The typewriter in the DDP-24 has four modes of operation.

a. OFF-LINE INPUT in which the typewriter and the punch are off-line, allowing paper tape preparation.

b. OFF-LINE OUTPUT in which the typewriter and the reader are off-line to produce a hard copy print out of the information on a paper tape.

c. ON-LINE INPUT in which information is transferred from the keyboard directly into the computer by means of the INM, INA, or FMB instructions.

d. ON-LINE OUTPUT in which information is transferred from the computer directly to the typewriter by means of the OTM, OTA, or DMB instructions to obtain hard copy print out.

These four modes are discussed separately in the following paragraphs. Signal outputs from the computer to the typewriter are provided by SD-30 PACs to pull in magnets. These signal outputs consist of the following.

a. WOC 1 thru WOC 7 are the print data lines, 6 data plus 1 parity.

b. Seven operational outputs include tab, space, backspace, carrier return, index, shift (upper case), and unshift (lower case).

c. Keyboard Lock is activated (keyboard locked) when the reader and punch are off-line for paper tape duplication or when the reader and typewriter are off-line for print out of paper tape.

Inputs from the typewriter to the computer are all contact closures activated by relays or cams.

In addition to the seven print data lines (WIC 1 through WIC 7) and the operational lines which correspond to those mentioned in b. above, the following inputs are provided by the typewriter.

a. Lower case and upper case modes to indicate the present status of the type head.

b. Parity check to indicate that the proper number of selection magnets have been pulled in.

c. Print data strobe (WDS), provided by CAM 1 to indicate the proper time to look at the selection contacts.

d. Cycle status (WCS) provided by CAM 2 for print data and CAMS 3, 4, 5 or 6 for operational functions and dependent on tab and carrier return interlock. This signal is timed in such a way that it indicates when magnets can be released and when a new machine cycle can start. The typewriter mode of operation is discussed in detail in the following paragraphs. Figures 5-18 through 5-21 show the timing and block diagrams of the I/O typewriter.

5-17.1 On-Line Input Mode (Figures 5-18 and 5-19)

The character buffer is first chosen by a channel select OCP and then the typewriter is chosen by a device select OCP. OCP 2000 sets typewriter input select (WIS) which enables typewriter input enable (WIE) if typewriter on-line select (WNS) is true. When a key is depressed the typewriter cycle starts. A typewriter output ready (WOR) pulse is generated at the leading edge of WCS. WOR sets the typewriter busy flip-flop (WBF) which makes character buffer device busy (KDB) true. At the same time, if a machine function key was depressed, a typewriter input pulse (WIP) resets the character buffer and a typewriter function strobe (WFS) gates the information, after conversion from IBM to DDP code, into the character buffer via typewriter input data lines WID 1 through WID 7. If an alphanumeric key was depressed, WIP and typewriter print strobe (WPS) are

generated on the leading edge of typewriter strobe synchronizer (WSZ), which sharpens up the incoming signal WDS, and operates on the character buffer as above. If the character buffer (K1 through K7) contains an even number of ones a parity error exists and is indicated on the control panel. The trailing edge of WCS produces typewriter-input ready (WIR) which sets character-buffer ready (Ro) and resets WBF, returning KDB to its original state. Ro enables input-output ready (IOR) to be sent to the DDP-24 control unit and when the contents of the character buffer are accepted into the computer via the input transfer bus, Ro is reset by input to transfer bus (ITT). Another character may now be typed into the computer. When typewriter output or another device is selected, WIS is reset and typewriter input delay (WIL) is set up to allow the last key depression to be processed.

5-17.2 On-Line Output Mode (Figures 5-20 and 5-21)

This mode is initiated by selecting the character buffer and then the typewriter. OCP 2010 sets typewriter output select (WOS) and Ro. A transfer bus to output (TTO) pulse is produced by the DDP control unit resetting Ro and generating an output transfer pulse OXP which gates the contents of the output transfer bus into the character buffer and sets typewriter output busy (WOB) if WNS is true. A typewriter output pulse (WOP) is generated from the leading edge of WOB if WBF is reset or on the trailing edge of WBF if the typewriter was busy when WOB was set. K1 through K6 are decoded into four categories — print code (WPC), function code (WFC), no operation (WNO) and shift code.

If K equals the print code, WOP sets typewriter data output (WDO). If K equals the function code, WOP sets typewriter function output (WFO). WOB will be reset by WOP if K equals no operation, or if K equals unshift when the typewriter is in lower case mode, or if K equals shift when the typewriter is in upper case mode. The trailing edge of WOB sets Ro, producing IOR.

A new character can be transferred into the character buffer if K equals shift when the typewriter is in lower case mode, or if K equals unshift when the typewriter is in upper case, mode WOB sets WFO. Because WCS is initially false before any motion of the typewriter shift takes place, WDO produces a typewriter data pulse (WDP) to pull in the appropriate selection magnets via WOC1 through WOC7 after converting the DDP code to the IBM code. Similarly, WFO would produce a typewriter function pulse (WFP) to pull in the correct operational magnet. Selection of the magnets initiates the typewriter cycle. As in the case of input operation, WOR is generated on the leading edge of WCS. WOR sets WBF, resets WDO or WFO, whichever was set, and resets WOB which sets Ro so that new data can be transferred to the character buffer. The trailing edge of WCS signifies that the typewriter cycle is complete and resets WBF, allowing WOP, if WOB had been set in the meantime. In the output mode, WSZ is used only to limit the time in which the typewriter internal parity check will be allowed to set the parity error flip-flop and indicate an error on the control panel. KDB becomes true when WOB is set and is held true until WBF is reset, unless WOB has again been set, in which case KDB remains true until WBF is reset for the last character to be typed out.

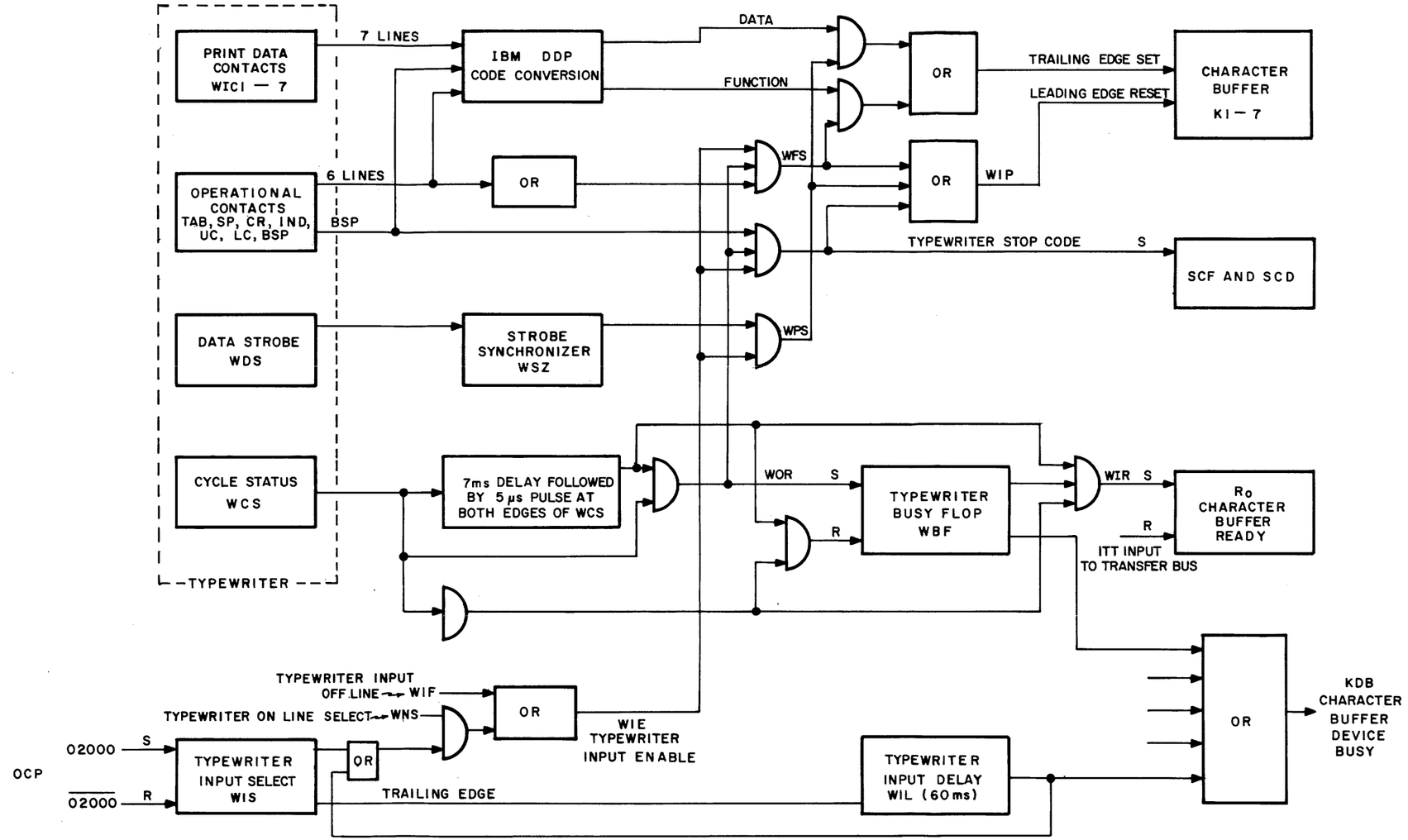


Figure 5-18. I/O Typewriter Input Block Diagram

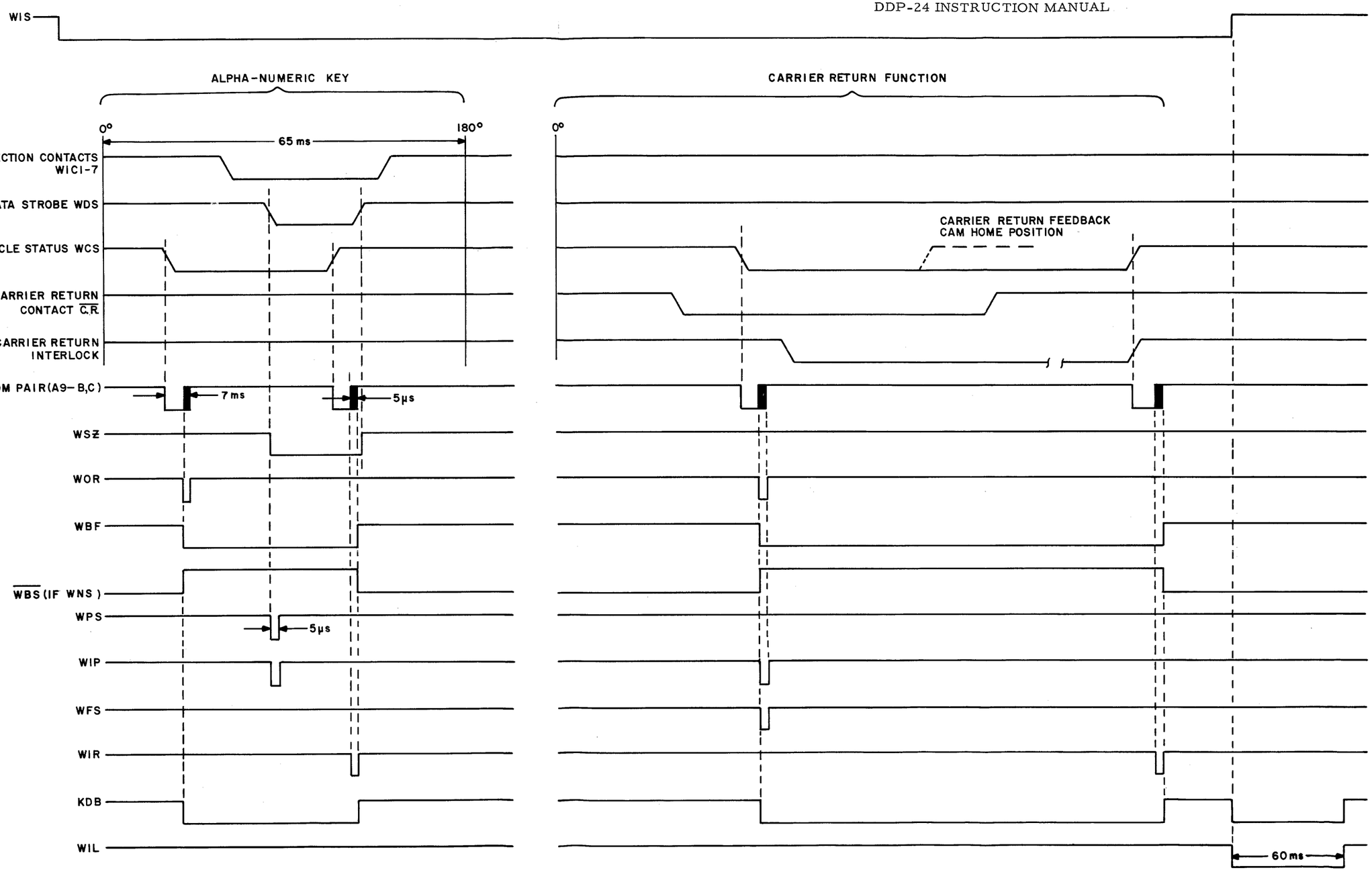


Figure 5-19. I/O Typewriter Input Timing Diagram

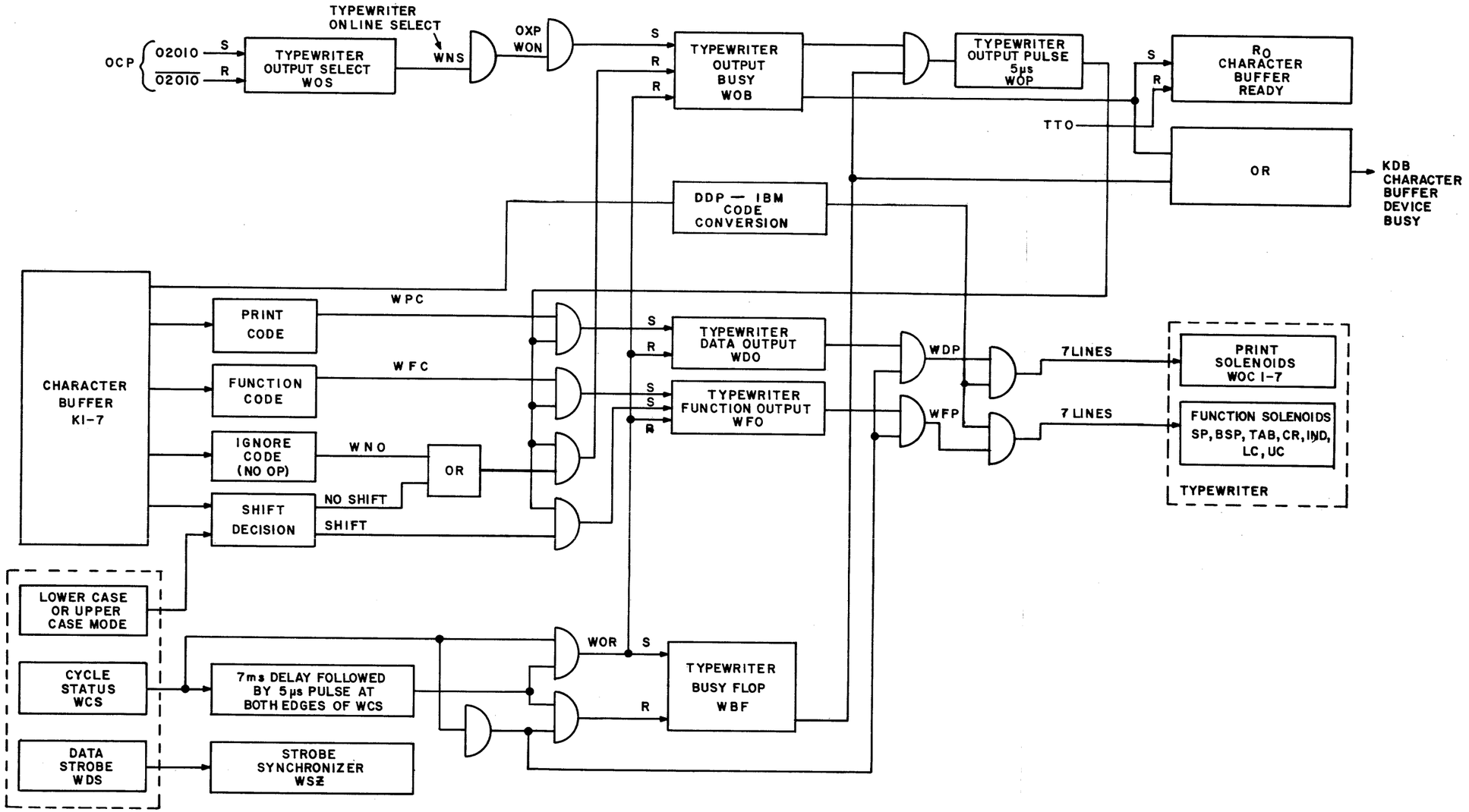


Figure 5-20. I/O Typewriter Output Block Diagram

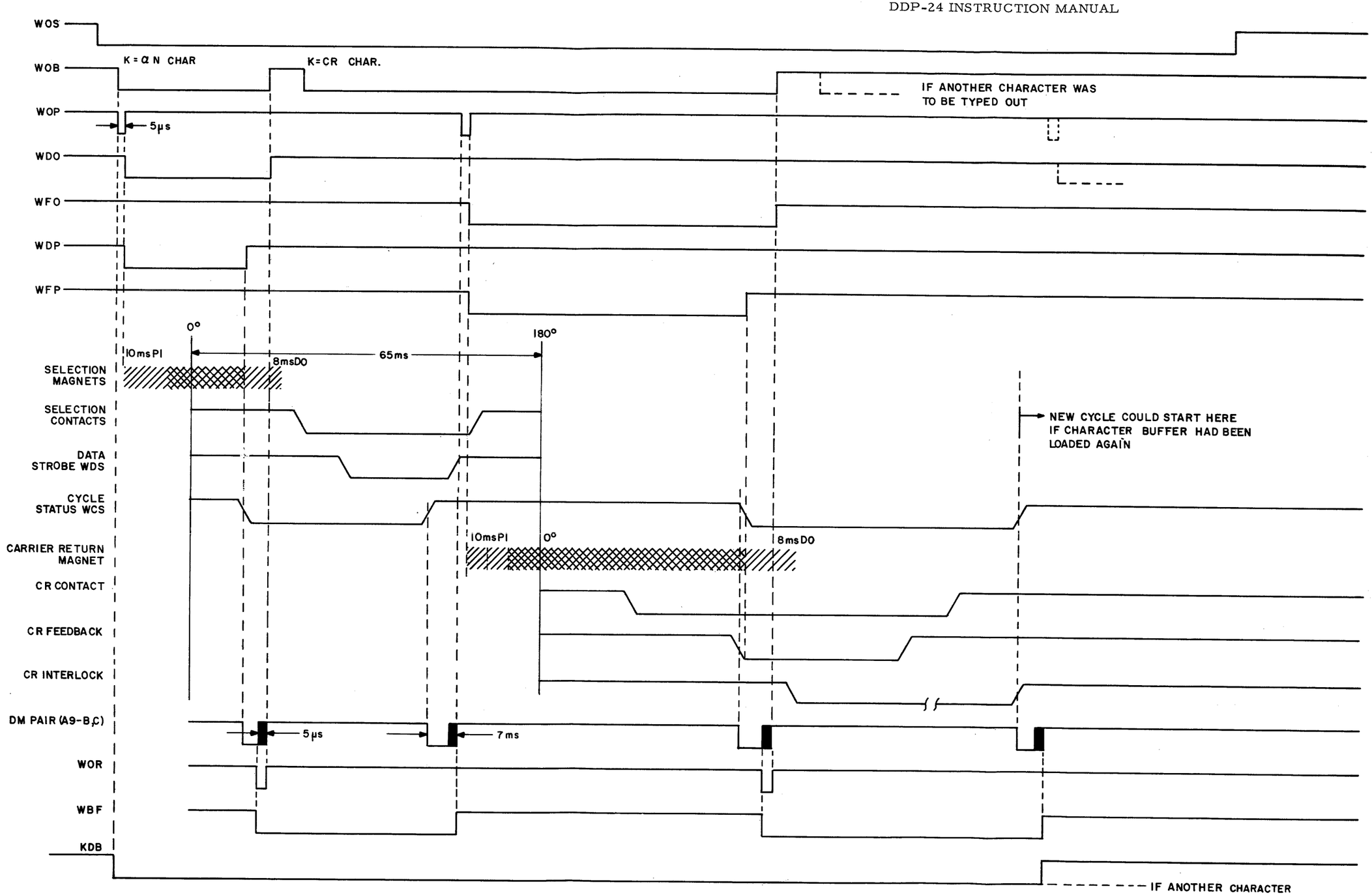


Figure 5-21. I/O Typewriter Output Timing Diagram

5-17.3 Off-Line Input Mode (Figure 5-21)

WIE is enabled by typewriter input off-line (WIF). The typewriter operation is the same as in the on-line mode, except that WIR will not set Ro. WIR produces punch start from typewriter (PSW) if K is not an ignore code and if punch off-line select (PFS) is true. PSW sets punch output busy (POB) which allows the contents of the character buffer to be transferred to the punch.

5-17.4 Off-Line Output Mode (Figure 5-21)

The off-line mode is the same as the on-line, except that WOB is set by typewriter start from reader (WSR) which is generated by reader input ready (RIR) if the typewriter output off-line (WOF) is true and K is not an ignore code. The reader is started initially by a pushbutton on the control panel. A character is read into the character buffer and typed out as before. When WOB is reset, the reader is again started for another character.

The following on-line/off-line typewriter operations are possible.

a. Input data to DDP-24 on-line.

b. Output data from DDP-24 on-line.

c. Typewriter to punch off-line.

d. Paper tape reader to typewriter off-line.

e. Paper tape reader to typewriter and punch off-line.

f. Program fill operations.

g. Operation as a standard secretarial typewriter, off-line.

5-17.4.1 Typewriter Input On-Line Operation. - The typewriter input on-line operation can be initiated by setting the typewriter ON-LINE switch to the ON-LINE position and at least one of the other two on-line switches to the ON-LINE position, and by initiating a typewriter input select OCP (OCP 02000) instruction. The OCP 02000 instruction will enable typewriter input select flip-flop (WIS) and will disable all other device select flip-flops. This OCP will also reset Ro by grounding the set output of the flip-flops. When WIS is set, typewriter output (WIN) and typewriter input enable (WIE) signals become true, permitting the input signals from the typewriter to transfer the character buffer when a typewriter key is operated. WIS also releases the typewriter keyboard lock by applying a -6 volt signal to the keyboard lock solenoid driver. (Refer to Figures 5-22 and 5-23.)

When a print key on the typewriter is operated, the typewriter selection cam shaft starts its rotation. A typewriter control signal (WOS) is generated by C2 print feedback cam and sets typewriter busy flip-flop (WBF). A typewriter data strobe signal (WDS), which is generated by C1 print feedback cam, generates a typewriter input pulse (WIP) to

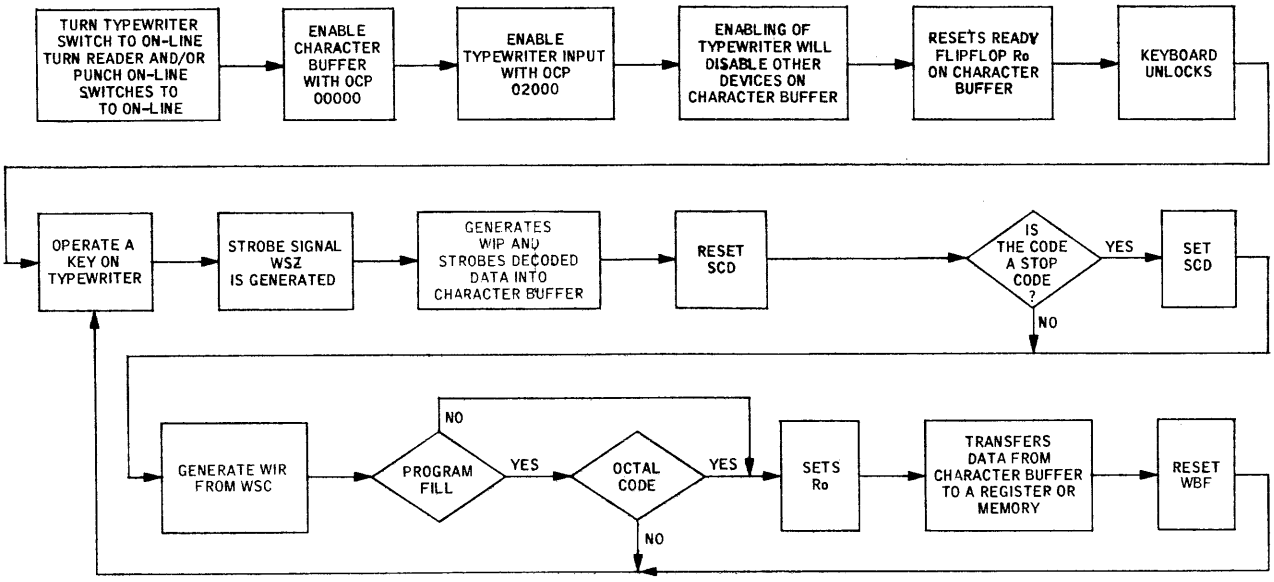


Figure 5-22. Typewriter Input On-Line, Flow Chart

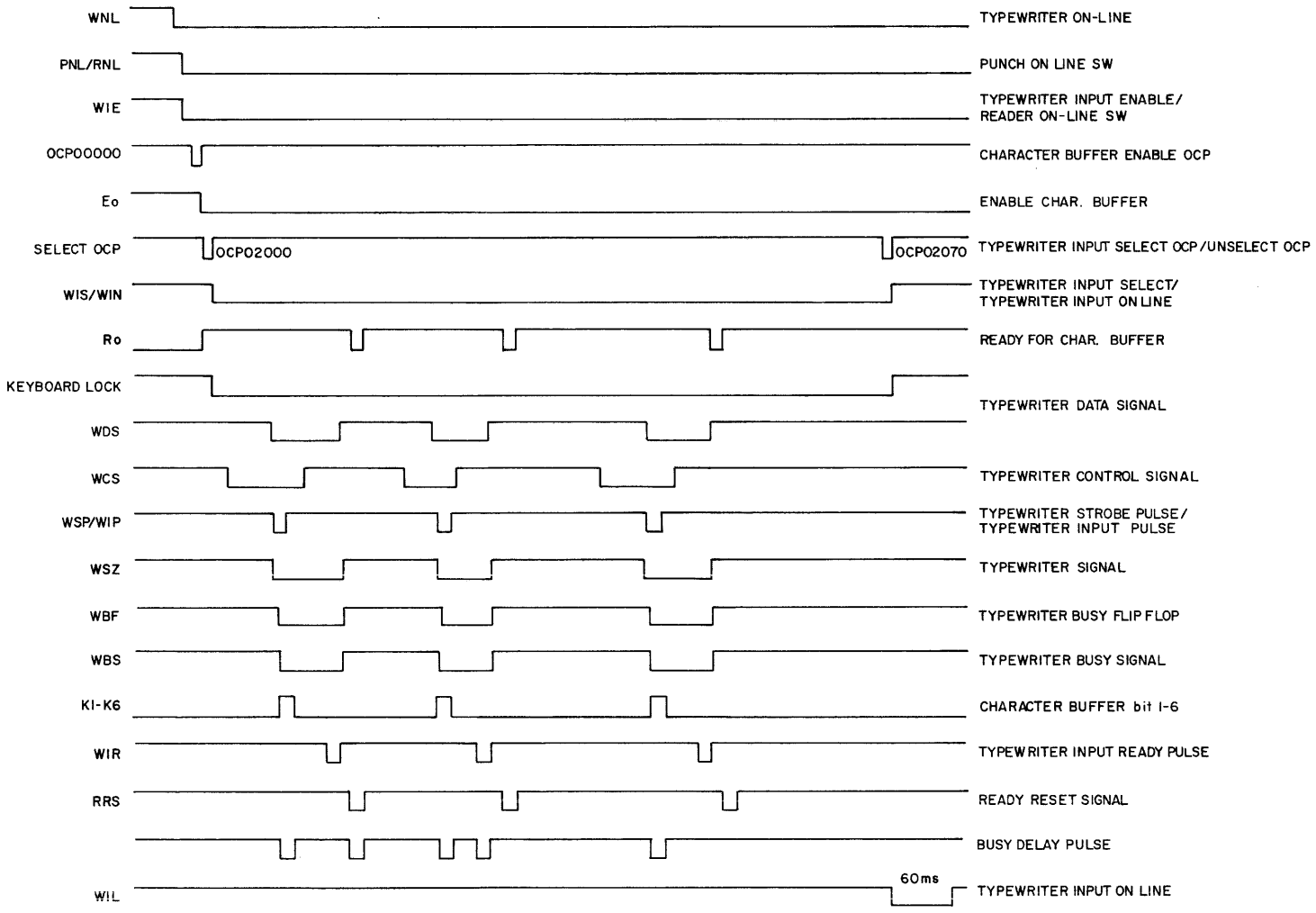


Figure 5-23. Typewriter Input On-Line, Timing Diagram

strobe decoded data signals into the character buffer flip-flops and insure that only one WIP is generated for a single operation. The decoding of data signals is shown in Table 5-1.

TABLE 5-1. IBM TO I/O DECODING

KEYBOARD	IBM CODE		I/O CODE	
0	110001	61	000000	00
1	111111	77	000001	01
2	111010	72	000010	02
3	111011	73	000011	03
4	111100	74	000100	04
5	111101	75	000101	05
6	111000	70	000110	06
7	111001	71	000111	07
8	110101	65	001000	10
9	110100	64	001001	11
#	110000	60	001011	13
	100001	41	010000	20
I	101111	57	010001	21
S	101010	52	010010	22
T	101011	53	010011	23
U	101100	54	010100	24
V	101101	55	010101	25
W	101000	50	010110	26
X	101001	51	010111	27
Y	100101	45	011000	30
Z	100100	44	011001	31
,	100000	40	011011	33
TAB	100011	43	011110	36
-	010001	21	100000	40
J	011111	37	100001	41
K	011010	32	100010	42
L	011011	33	100011	43
M	011100	34	100100	44
N	011101	35	100101	45
O	011000	30	100110	46
P	011001	31	100111	47
Q	010101	25	101000	50
R	010100	24	101001	51
$	010000	20	101011	53
B.S.	010111	27	101100	54
SP	010011	23	101110	56
&	000001	01	110000	60
A	001111	17	110001	61
B	001010	12	110010	62
C	001011	13	110011	63
D	001100	14	110100	64
E	001101	15	110101	65
F	001000	10	110110	66
G	001001	11	110111	67

TABLE 5-1. IBM TO I/O DECODING (cont)

KEYBOARD	IBM CODE		I/O CODE	
H	000101	05	111000	70
I	000100	04	111001	71
.	000000	00	111011	73
L.C.	000111	07	111100	74
U.C.	000110	06	111101	75
C.R.	000011	03	111110	76
IND.	000010	02	111111	77

When WCS is false, the typewriter busy flip-flop (WBF) is turned off, and the typewriter input ready signal (WIR) is generated. Because signal WCS has contact bounce, WBF is set 6.6 ms after WCS becomes true if WCS is still true after the delay. WBF is reset 6.6 ms after WCS becomes false if WCS is still false after the delay.

If WBS is true during an input operation, the character buffer device busy signal (KDB) will be true. This condition can be checked by SKS command. KDB also becomes true when the typewriter input delay signal (WIL) is true.

If the data in the character buffer is not an ignore code, the typewriter input ready signal (WIR) will set Ro. During program fill, the computer will accept only octal codes. When the typewriter input select signal (WIS) is reset, WIL is set and will reset after a 60 millisecond delay. As long as WIL is set, the character buffer device busy signal (KDB), the typewriter input (WIN), the typewriter input enable (WIE) and the input on-line enable (NIE) signals will be true and the transfer of inputs from the typewriter into the computer is allowed 60 milliseconds after WIS is reset. This permits the last information from the typewriter to be transferred after WIS is reset, since the keyboard delays before it locks.

When a function key is operated, the operational cam shaft rotates cams C3, C4, C5, or C6, depending on the operation, and generates a typewriter control signal (WCS) which sets the typewriter busy flip-flop (WBF). At the same time typewriter function strobe (WFS) is generated. The function is decoded into DDP I/O codes as shown in Table 5-1 and is strobed into the character buffer with the typewriter function strobe (WFS). WBF is reset when cams C3, C4, C5, and C6 close and is also reset after tab and carrier return interlock contacts release. A typewriter input-ready signal (WIR) is generated and Ro is set.

5-17.4.2 Typewriter Output On-Line Operation. - The typewriter output on-line operation is initiated by setting the typewriter ON-LINE switch to the ON-LINE position and at least one of the other two on-line switches to the ON-LINE position, and by initiating a typewriter output select OCP (OCP 02010) instruction. The OCP 02010 instruction will set the typewriter output select flip-flop (WOS) and reset all other select flip-flops. The OCP 02010 instruction will also set character buffer ready flip-flop (Ro). The setting of

of WOS will generate typewriter output on-line (WON) and on-line output enable (NOE) signals true and will lock the keyboard by grounding the input of the keyboard lock solenoid driver. (Refer to Figures 5-24 through 5-26.)

A character will be transferred into the character buffer by an OTA, OTM or DMB instruction which resets Ro and sets the typewriter output busy flip-flop (WOB). The setting of WOB will generate a 5 microsecond typewriter output pulse (WOP). The character in the character buffer is sorted into the typewriter print code (WPC); the typewriter function code (WFC), or a nontypewriter code (code that the typewriter cannot recognize) where WOB resets with typewriter output pulse (WOP) and no operation takes place. If the code is a print code, the typewriter data output flip-flop (WDO) sets with WOP. The typewriter control signal (WCS) will gate with WDO to create a data pulse (WDP) which energizes the typewriter data solenoids after the data in the character buffer is decoded. At the leading edge of WCS, the typewriter output ready (WOR) signal is generated and it resets WOB.

When a shift code is in the character buffer and the typewriter is already in upper case, the typewriter output pulse (WOP) will reset typewriter output busy flip-flop (WOB). When an un-shift code is in the character buffer and the typewriter is already in lower case, WOP will also reset WOB. In either case, no operation takes place and the codes will be ignored.

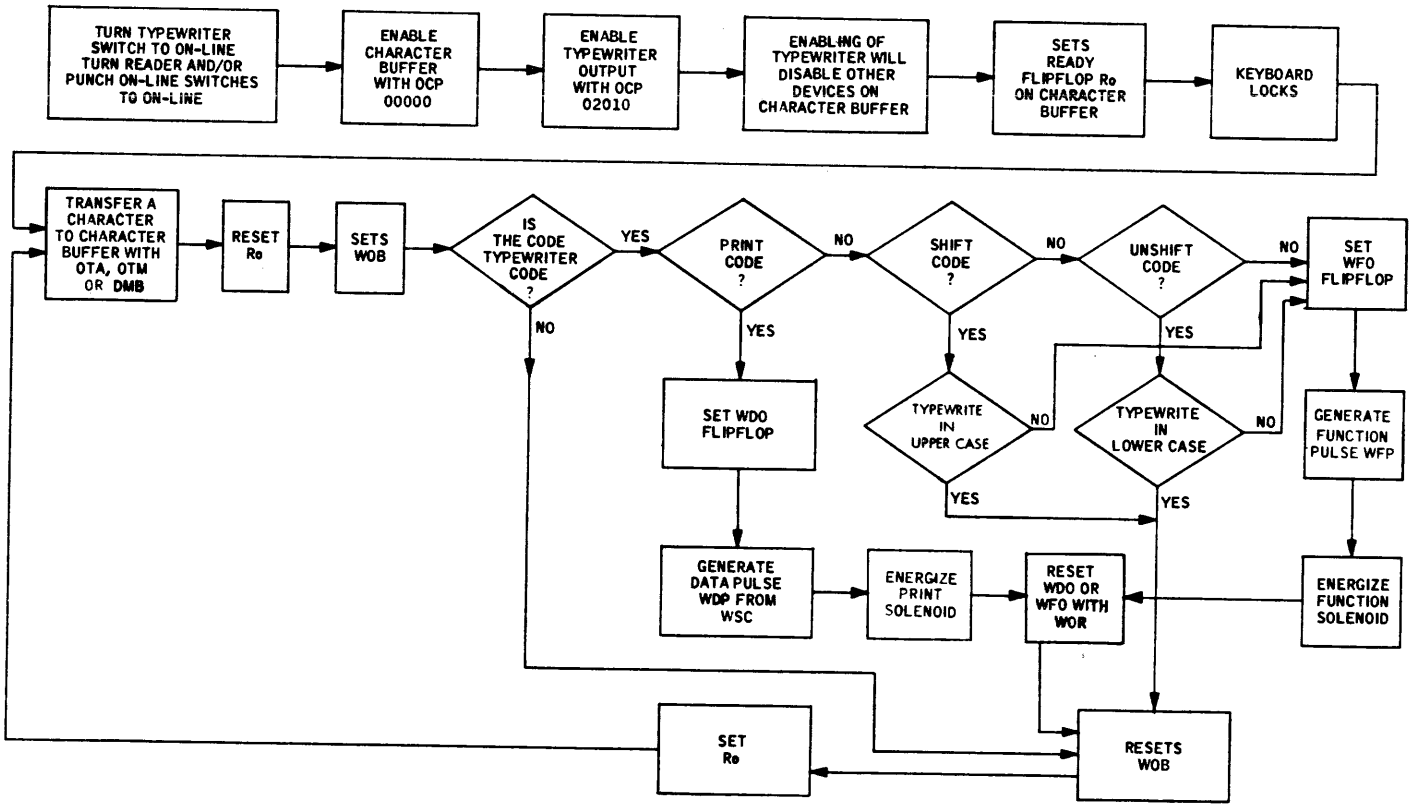


Figure 5-24. Typewriter Output On-Line, Flow Chart

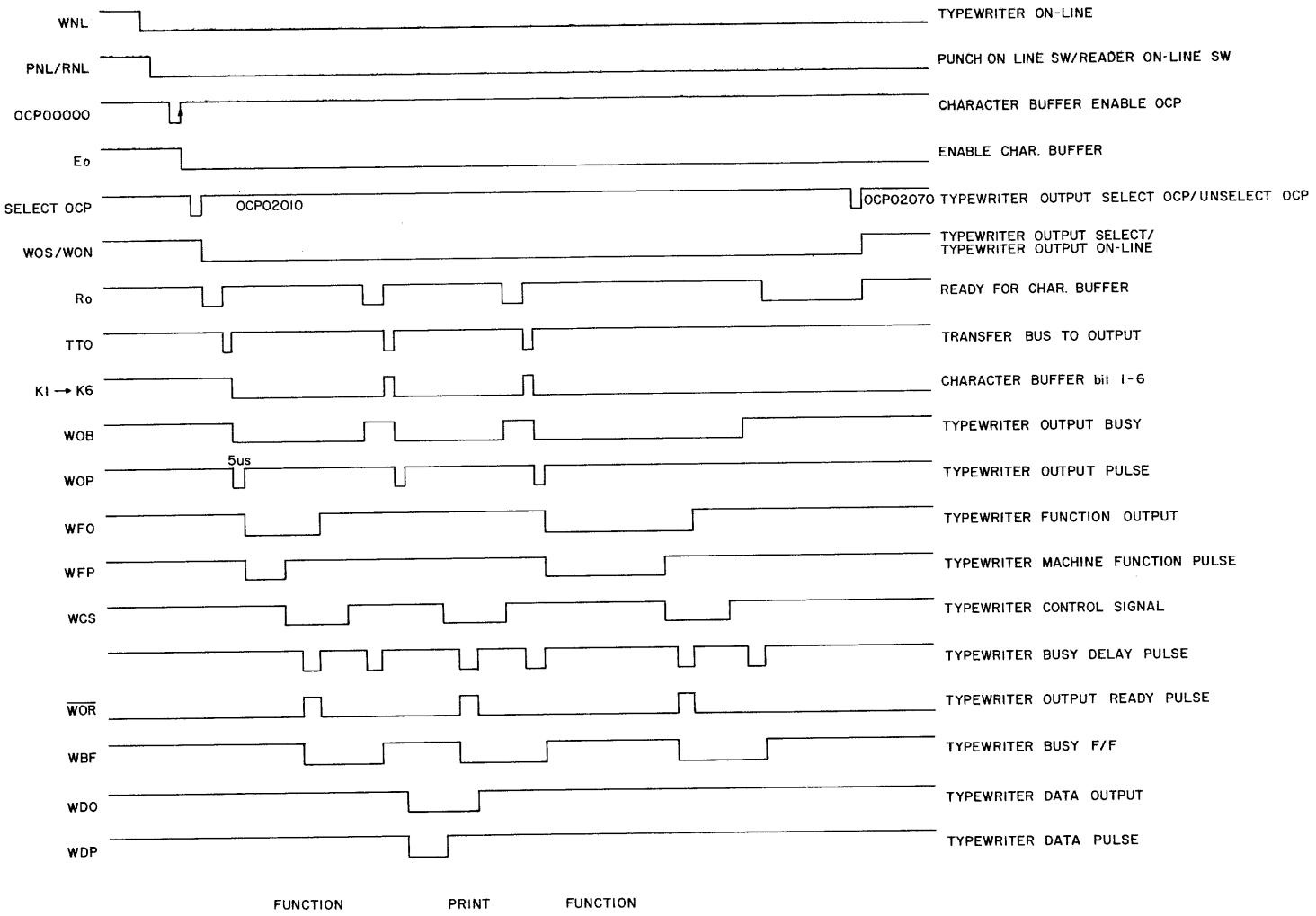


Figure 5-25. Typewriter Output On-Line, Timing Diagram

When the typewriter is in lower case and a shift code is in the character buffer, the typewriter output pulse (WOP) will set the typewriter output function flip-flop (WFO). The setting of WFO will generate a typewriter function pulse (WFP) until the typewriter control signal (WCS) becomes true. WFP will energize the typewriter shift solenoid and the typewriter will shift to upper case. At the end of the shift operation WCS becomes false, WBF is reset, and another WOP is allowed.

When an un-shift code is in the character buffer while the typewriter is in upper case, typewriter function output flip-flop (WFO) is set by the typewriter output pulse (WOP) and the typewriter busy flip-flop (WFP). These will energize the un-shift solenoid in the typewriter. When WCS becomes true, the typewriter output ready (WOR) signal is generated which resets typewriter output busy (WOB) and typewriter function (WFO).

If the code in the character buffer is a typewriter function code (WFC) such as space, back-space, tab, carrier return, or index, WOP will set WFO and WFP as before. The appropriate solenoid will be energized by a solenoid driver. At the end of the solenoid energizing, the WOR signal will reset WOB and WFO. The trailing edge of WOB will set Ro and another character is transferred into character buffer with an OTA, OTM or DMB instruction.

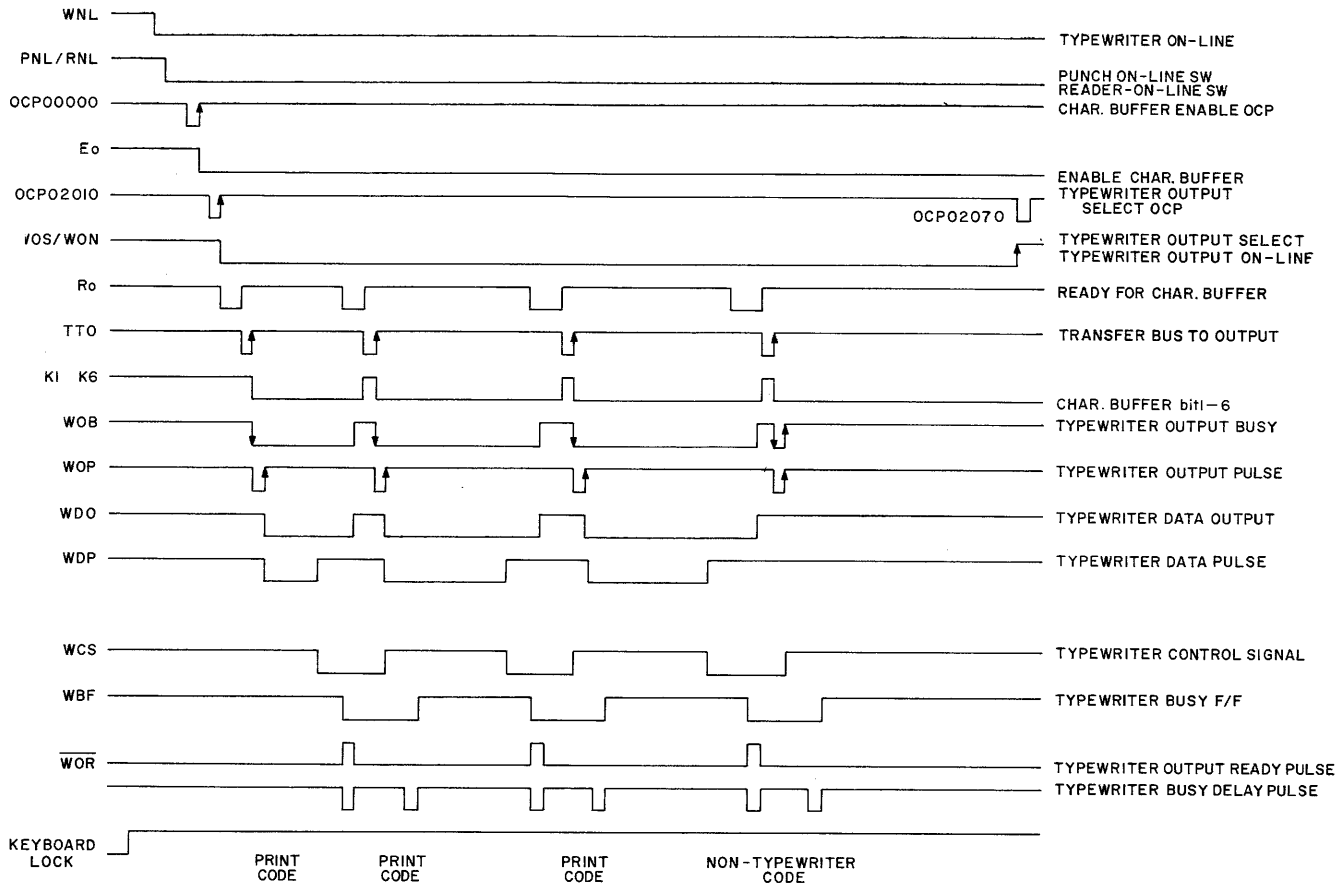


Figure 5-26. Typewriter Output On-Line Printing, Timing Diagram

During an output operation, typewriter busy (WBS) is true, and the channel buffer device signal (KDB) is true. As long as KDB is true, the typewriter output select (WOS) should remain unselected and the typewriter input select (WIS) should not be selected.

5-17.4.3 Typewriter Punch Off-Line Operation. - In order to perform this operation, the reader switch must be positioned to ON-LINE, and the typewriter and punch switches to their OFF-LINE positions. (Refer to Figures 5-27 through 5-30.)

Both the typewriter and the punch power switches should be positioned to ON. A key on the typewriter will generate a strobe typewriter input pulse (WIP). The strobe pulse is used to strobe data from the typewriter into the character buffer. Since typewriter code and DDP I/O code are not the same, decoding (Table 5-1) is performed before data is transferred into the character buffer. At the end of the operation, the typewriter input ready (WIR) is generated. This signal is used to determine if the information in the character buffer is an ignore code or not. If the information is not an ignore code, a punch start from typewriter (PSW) signal is generated. Signal PSW turns on the punch-output busy flip-flop (POB) which transfers information in the character buffer into the punch.

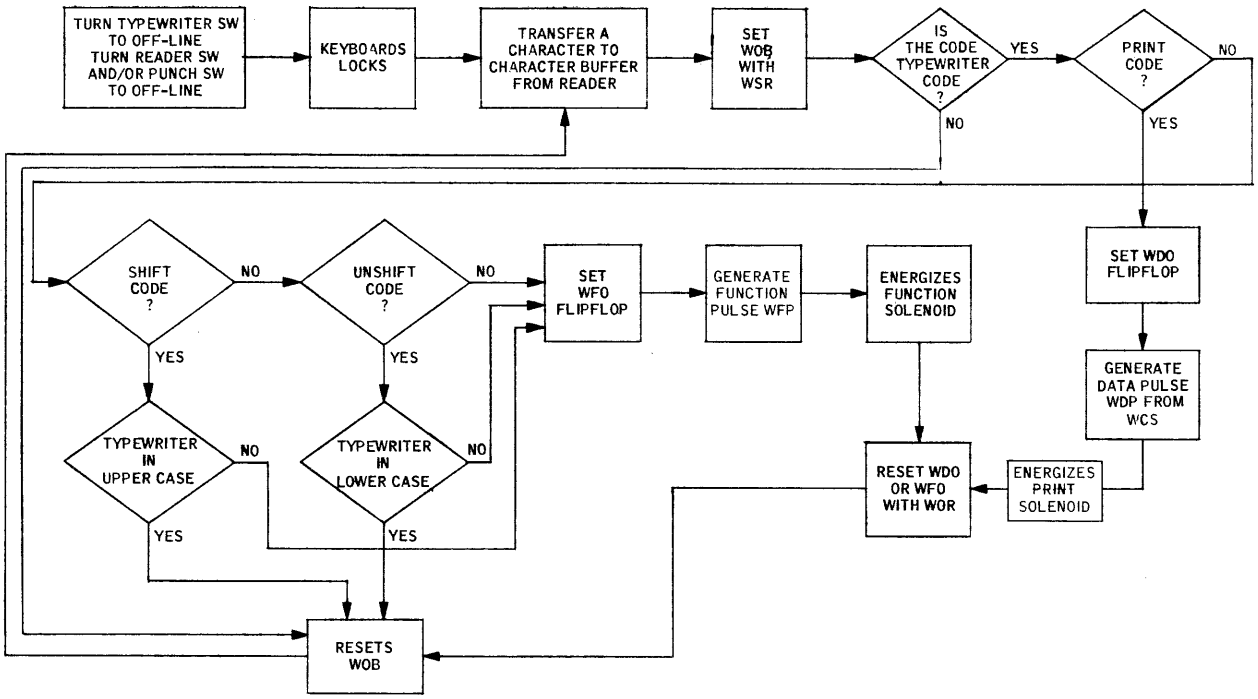


Figure 5-27. Typewriter Output Off-Line, Flow Chart

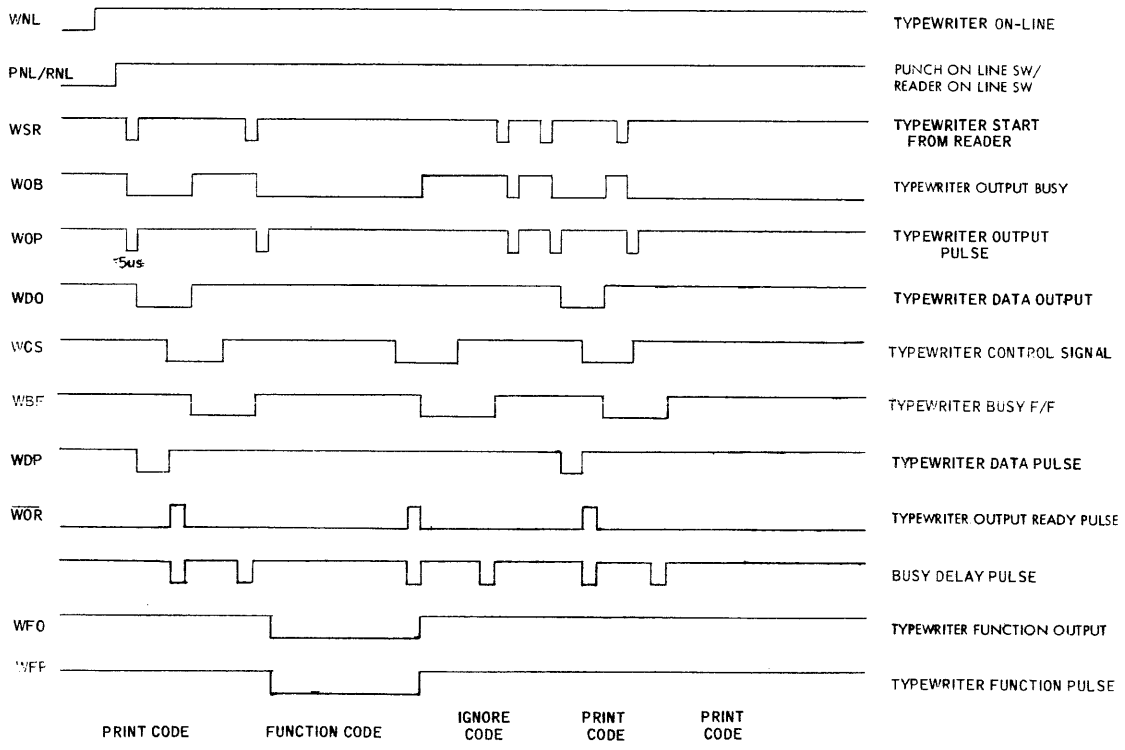


Figure 5-28. Typewriter Output Off-Line, Timing Diagram

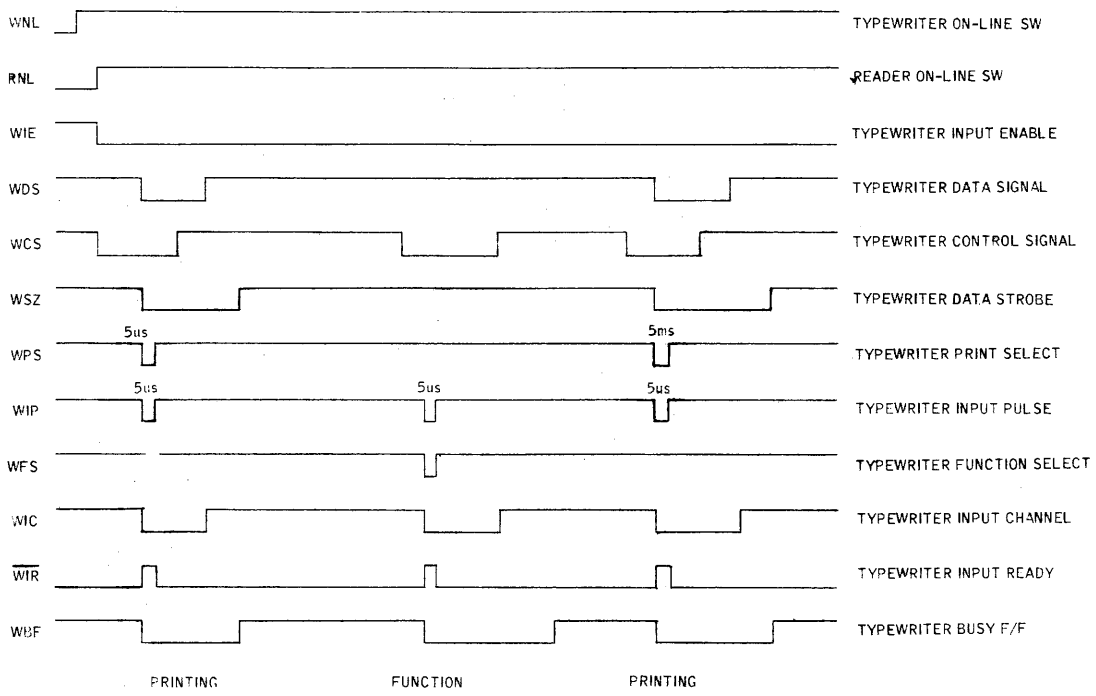


Figure 5-29. Typewriter Input Off-Line, Timing Diagram

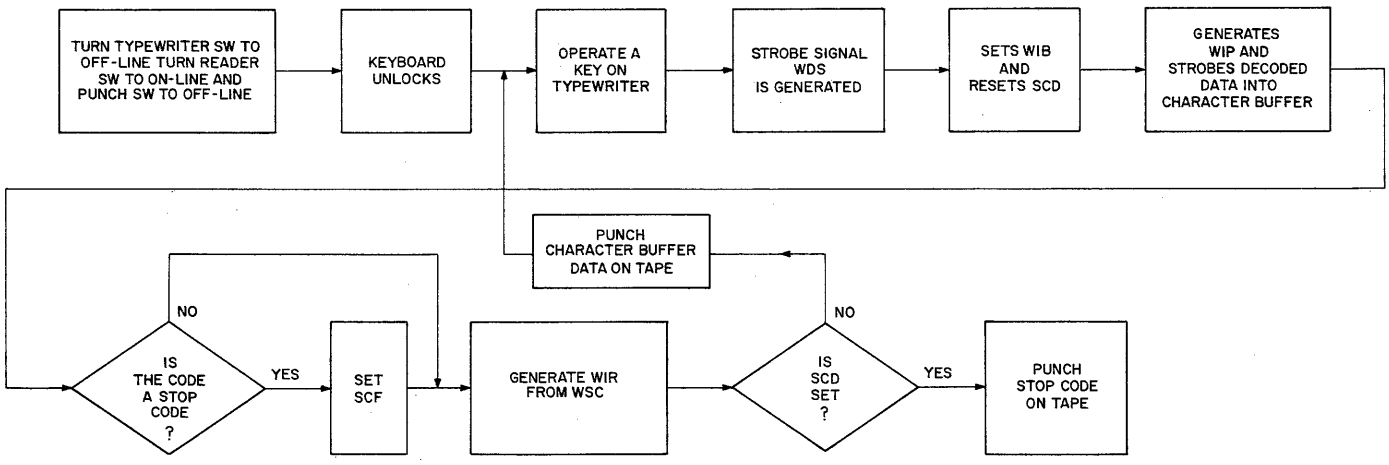


Figure 5-30. Typewriter Input Off-Line, Flow Chart

At the end of the punch output pulse (POP), POB will reset. Since the typewriter operates at a slower speed than the punch, the punch is ready to accept the new data before the typewriter.

When the typewriter backspace key is depressed, a stop code signal is generated which sets the stop code flip-flop (SCF) and causes a hole to be punched in column eight. This is accomplished by allowing the punch timing pulse (PTP) to set the punch output pulse (POP) as long as SCF is set. SCF will reset at the trailing edge of POP, allowing only one punch to be made in the tape.

5-17.4.4 Paper Tape Reader To Typewriter Off-Line Operation. - In order to list paper tape with the typewriter off-line operation, the paper tape reader switch and typewriter switch should be in the OFF-LINE position. The paper tape punch switch should be in the ON-LINE position and the paper tape reader must be pulsed. When the reader is started, a pulse is generated which sets reader start flip-flop (RST). Information on the tape will be transferred into the character buffer with the reader input pulse (RIP). Reader input ready pulse (RIR) is then operated after 5 μsec delay. At the same time parity checking is performed. If there is a parity error, parity error flip-flop (PEF) is set and the parity error light comes ON. However if the code is an ignore code, PEF will not set. If the data in the character buffer is not an ignore code, the typewriter start off-line (WSR) signal is generated with the typewriter input ready signal (WIR). WSR turns on the typewriter output busy (WOB) signal which starts the typewriter output operation. When WOB is set, a typewriter output pulse (WOP) is generated. Data in the character buffer is then examined to determine to which of the four categories it belongs. (Refer to Figures 5-27 through 5-30.)

a. Print codes

b. Function codes

c. Non-typewriter codes

d. Shift codes

If the data in the character buffer is a print code, the typewriter data output flip-flop (WDO) is set with the typewriter output pulse (WOP). This starts the typewriter in the print mode. After the data is decoded into IBM code, information in the character buffer is transferred to the data magnet in the typewriter through solenoid drivers. At the end of the typewriter control signal (WCS), the typewriter output ready (WOR) signal is generated in the typewriter. This signal turns off WDO and WOB. (WOR is generated before the actual printing occurs.) WOB is used to generate the reader start to typewriter (RSW) signal which starts the reader for another tape read cycle.

If the code in the character buffer is a function code, the typewriter function output flip-flop (WFO) is set. The typewriter function pulse (WFP) is used to operate the function magnets in the typewriter. When WCS becomes true, a typewriter output ready (WOR) signal is generated, resetting WOB and WFO.

If the data in the character buffer is not a typewriter code, the typewriter output pulse (WOP) turns off the typewriter output busy signal (WOB) and another reader start to typewriter (RSW) signal is initiated.

If the code in the character buffer is a shift code, the condition of the typewriter is examined before the shift operation occurs. If the shift code is in the character buffer when the typewriter is in lower case, the typewriter function output flip-flop (WFO) is set and the shift operation takes place as in the function operation. If the typewriter is in the shift operation, the typewriter output pulse (WOP) will turn off the typewriter output busy flip-flop (WOB) and another reader operation will start. If the character buffer contains an un-shift code and the typewriter is in upper case, the flip-flop (WFO) will set and the un-shift operation will take place. If the typewriter is in lower case, the WOB will reset with WOP and the tape will advance another character. During output operations, the keyboard is locked.

5-17.4.5 Paper Tape Reader to Typewriter and Punch Off-Line Operation. - In order to list tape with the typewriter and punch tape simultaneously, all switches should be in the OFF-LINE position. The tape reader should be in the pulsed mode. This operation is similar to the tape to punch or tape to typewriter operations. Because the typewriter is the slower of the two units, the tape start signal is always generated by the typewriter output busy (WOB) signal. (Refer to Figures 5-27 through 5-30.)

5-17.4.6 Program Fill Operation. - It is possible to fill a program into memory from the typewriter. To accomplish this, the typewriter input must be selected with an OCP 02000 instruction before the FILL button is depressed. Data from the typewriter will be transferred into the character buffer and examined for ignore codes. Codes other than octal will be considered ignore codes and will not set Ro. If the data is not an ignore code, Ro will set and data will be transferred into the A register. In the A register, a word is formed prior to transfer into memory. To perform this operation, the power switch on the paper tape reader must be in OFF position and the card reader should not be in ready status.

5-17.4.7 Standard Secretarial Typewriter Off-Line Operation. - If the reader and punch switches are in the ON-LINE position and typewriter switch is in the OFF-LINE position, the typewriter is disconnected from the DDP-24 and the keyboard is unlocked. The typewriter can now be used as an ordinary typewriter. (Refer to Figures 5-25 and 5-27 through 5-30.)

5-18 PAPER TAPE READER

The Digitronics Model 2500 Unidirectional paper tape reader is capable of reading 300 characters per second and can be stopped within a character length. The reader can be operated in a continuous mode when tape is fed without stopping or in a pulsed mode when the tape is stopped after each character. The reader uses photodiodes to read punched holes. When the reader POWER switch is turned ON, AC voltage is applied to the reader. However, power to the reader brake and pinch roller is inhibited until the tape guide lever is lowered.

Tape feed is initiated by a -6-volt run signal to the reader. While this signal is present, the brake is released and the pinch roller is energized. When the run signal becomes 0 volts, the pinch roller de-energizes and the brake is applied.

As tape is fed over the read heads, a negative going pulse is generated when a hole is sensed by the photodiode assembly. Since the photodiode assembly senses both data and sprocket holes (sprocket holes are smaller than data holes), the sprocket signal pulse turns on later and turns off earlier than the data pulse. As long as the read head is not covered by tape, the output will always be -6 volts. The reader operates in the following modes.

a. Tape reader on-line continuous mode

b. Tape reader on-line pulsed mode

c. Tape reader to punch off-line

d. Tape reader to typewriter off-line

To operate the tape reader in on-line continuous mode, the continuous mode switch must be positioned to CONTINUOUS, the reader ON-LINE/OFF-LINE switch must be placed in the ON-LINE position, and at least one of the other two on-line/off-line switches must be placed in the ON-LINE. When the reader input enable (RIE) and reader input pulse (RIN) become true, the reader is in the ON-LINE mode of operation. (Refer to Figures 5-31 and 5-32 and to the DDP-224 Service Manual, Volume II.)

To start the paper tape reader, initiate an OCP 02100 to set the reader start flip-flop (RST) and the reader operate flip-flop (ROP).

The character buffer ready (Ro) is reset by a grounding signal (from 4C11) the collector of which pulls the set side of the Ro flip-flop. The reader start (RST) signal starts the reader feed tape and the ROP signal resets the stop code flip-flop (SCD). When the sprocket signal becomes true, a 5 μsec-strobe reader-input-pulse (RIP) is generated. If the sprocket hole is sensed by the read head, the strobe pulse RIP is generated when RST is set. RIP strobes the data channels 1 through 8 into the character buffer, and a delayed reader pulse input ready (RIR) will set the ready flip-flop in the character buffer.

If the tape contains a stop code, the reader input pulse RIP will set the stop code flip-flop (SCD) and reset the ROP flip-flop.

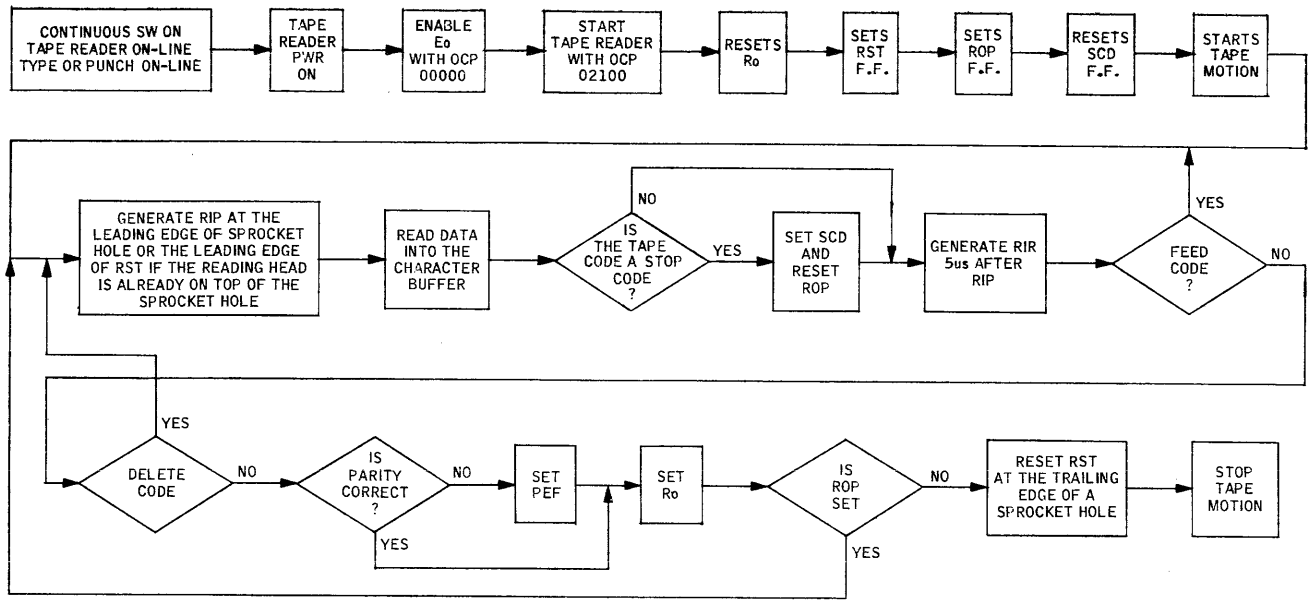


Figure 5-31. Paper Tape Reader On-Line Continuous Mode, Flow Chart

At the trailing edge of the sprocket hole, a 10 microsecond pulse is generated. If ROP is reset because of a stop code or by selecting an OCP other than the tape reader select, RST will reset and stop the tape from feeding.

For continuous operation of the reader, successive OCP's must be initiated within 1.3 milliseconds after ready Ro is set.

The paper tape reader pulsed mode operation is similar to the continuous mode operation, except the reader will halt after each character. (Refer to Figures 5-33 and 5-34.)

To duplicate a tape, the reader switches must be in the OFF-LINE and PULSED position and the typewriter switch must be in the ON-LINE position. The punch switch must be in the OFF-LINE position, and the punch power switch must be in the ON position. The reader off-line select (RFS) and punch off-line select (PFS) signals will be true. When the reader START pushbutton is depressed, the reader start flip-flop (RST) and the reader operation flip-flop (ROP) are set. When a sprocket hole appears over the reader read head, the reader strobe pulse one-shot (RSP) turns on and the tape data is transferred into the character buffer. Tape data is strobed with the signal RIP which is generated from RSP. This data is dropped into the character buffer. After a 5-μsec delay RIR is generated. With this pulse, the contents of the character buffer are examined to determine if the code which has just been read is an ignore code. If the code is not an ignore code, a punch start

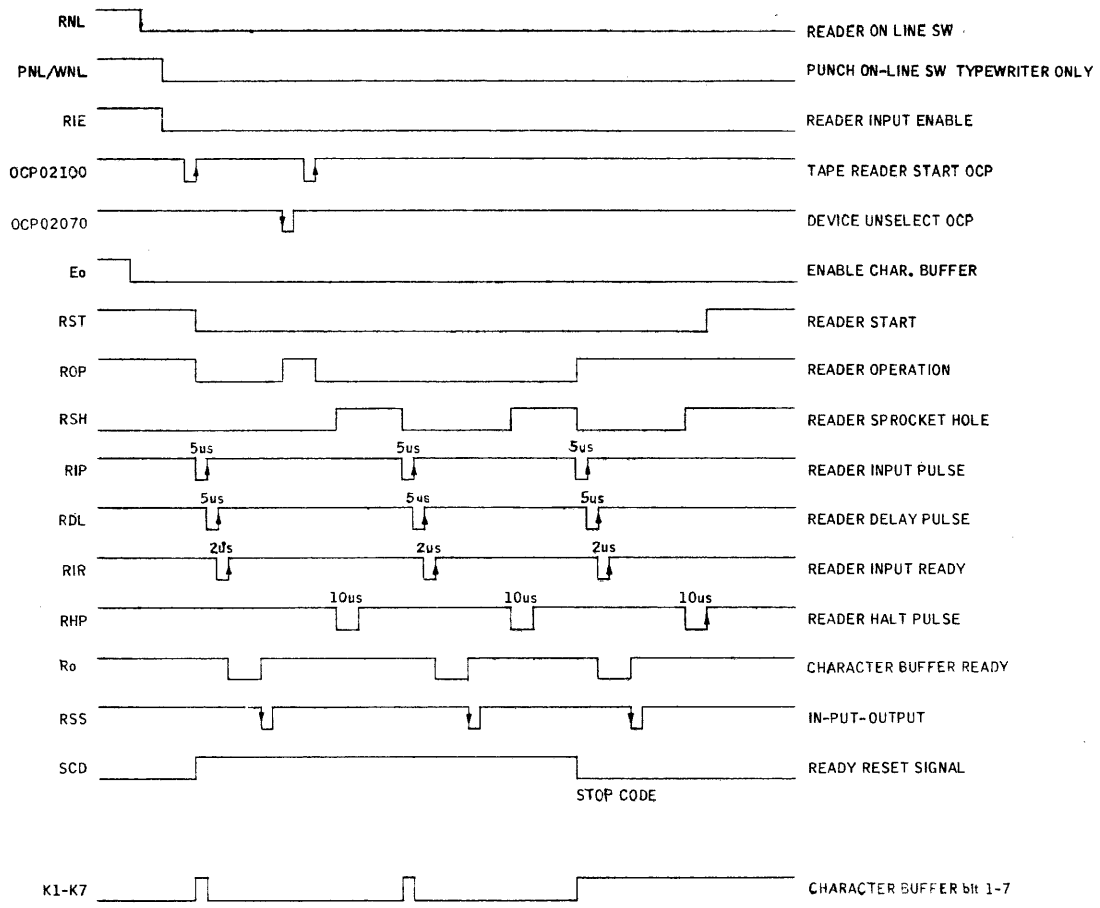


Figure 5-32. Paper Tape Reader On-Line Continuous Mode, Timing Diagram

pulse (PSR) is generated. This signal sets the punch output busy flip-flop (POB) which starts punch operation. Parity is checked with RIR and if a parity error exists, this pulse will set the parity error flip-flop (PEF) which turns on the control panel parity error light. Parity checking is not performed if an ignore code exists. (Refer to Figures 5-35 and 5-36.)

When the punch power switch is turned on, the punch timing pulse (PTP) is initiated. When punch output busy flip-flop (POB) is set the punch (PUB) signal is generated and triggers a 4.5 milliseconds one shot punch output pulse (POP). During POP, information is transferred from the character buffer to the punch with the signal PDP. The trailing edge of POP turns off POB.

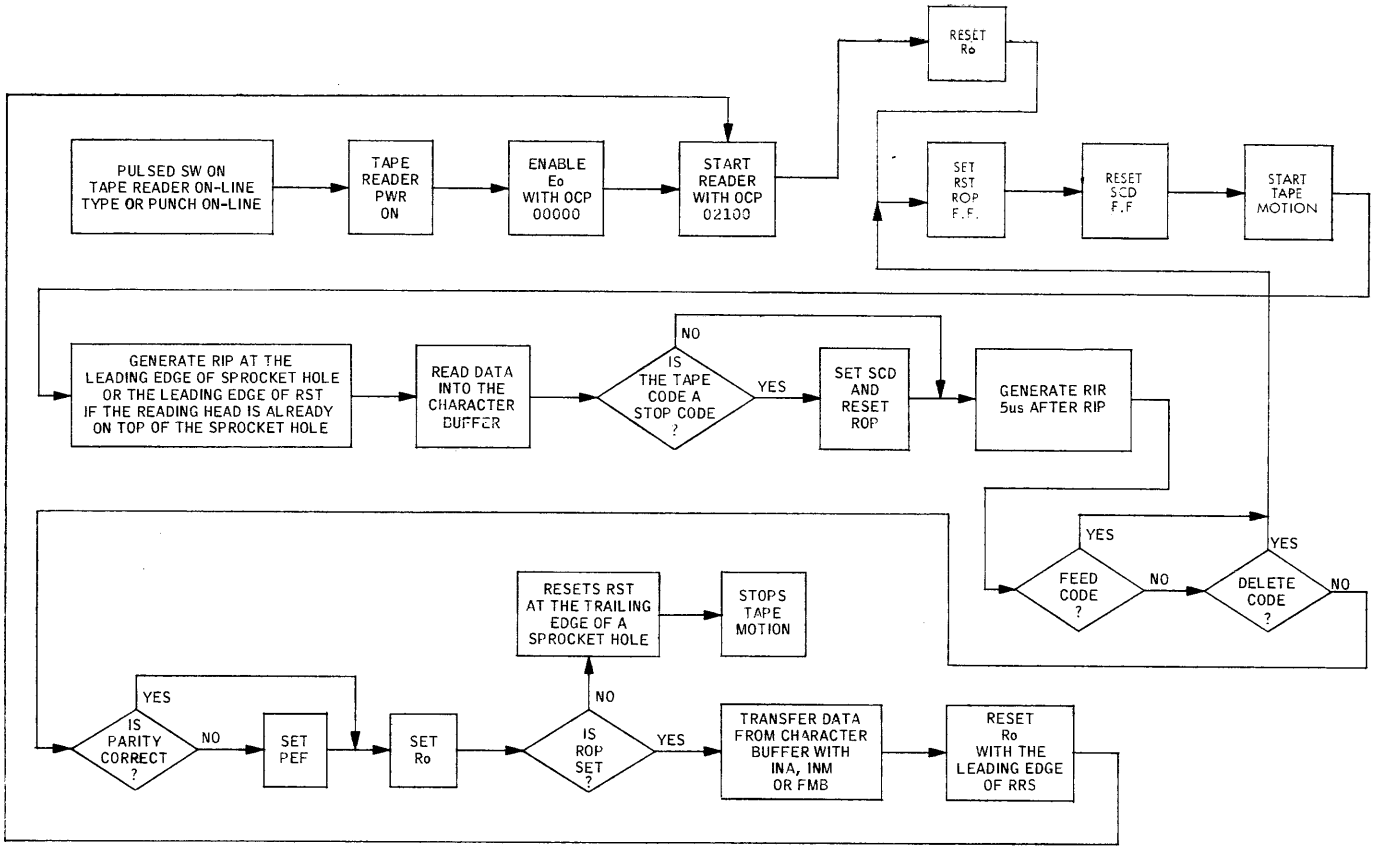


Figure 5-33. Paper Tape Reader On-Line Pulse Mode, Flow Chart

At the trailing edge of the sprocket hole, the reader halt pulse (RHP) is generated. Since the read output pulse (ROP) has already been reset, the RHP resets RST. When RST resets, the brake is applied to the tape reader. At the trailing edge of POP, the reader start pulse (RSP) is generated and RST is set to start the next cycle. This process will continue until the reader sees a stop code. When the stop code is read, flip-flop SCD is set as ROP resets. At the end of the sprocket hole, RHP will reset RST and the tape will halt. During off-line operation, the stop code will be ignored and the punch start signal (PSR) will be inhibited. When the tape contains an ignore code, information is transferred into the character buffer. During RIR time, the character buffer is examined to determine if an ignore code has been read (IGN). If an ignore code is read, signal IGN will inhibit RIR from resetting ROP. RST will not be reset by RHP, and a punch start signal will not be generated. Since the tape is still moving, it will come to the next sprocket hole and read in the next character.

When the fill button is depressed, flip-flop C15 is reset. This signal sets RST which starts the paper tape reader. Tape data is read into the character buffer and examined to determine if an ignore code exists. If the character is an ignore code, ready signal Ro will not set. During the program fill operation, all codes except the octal code

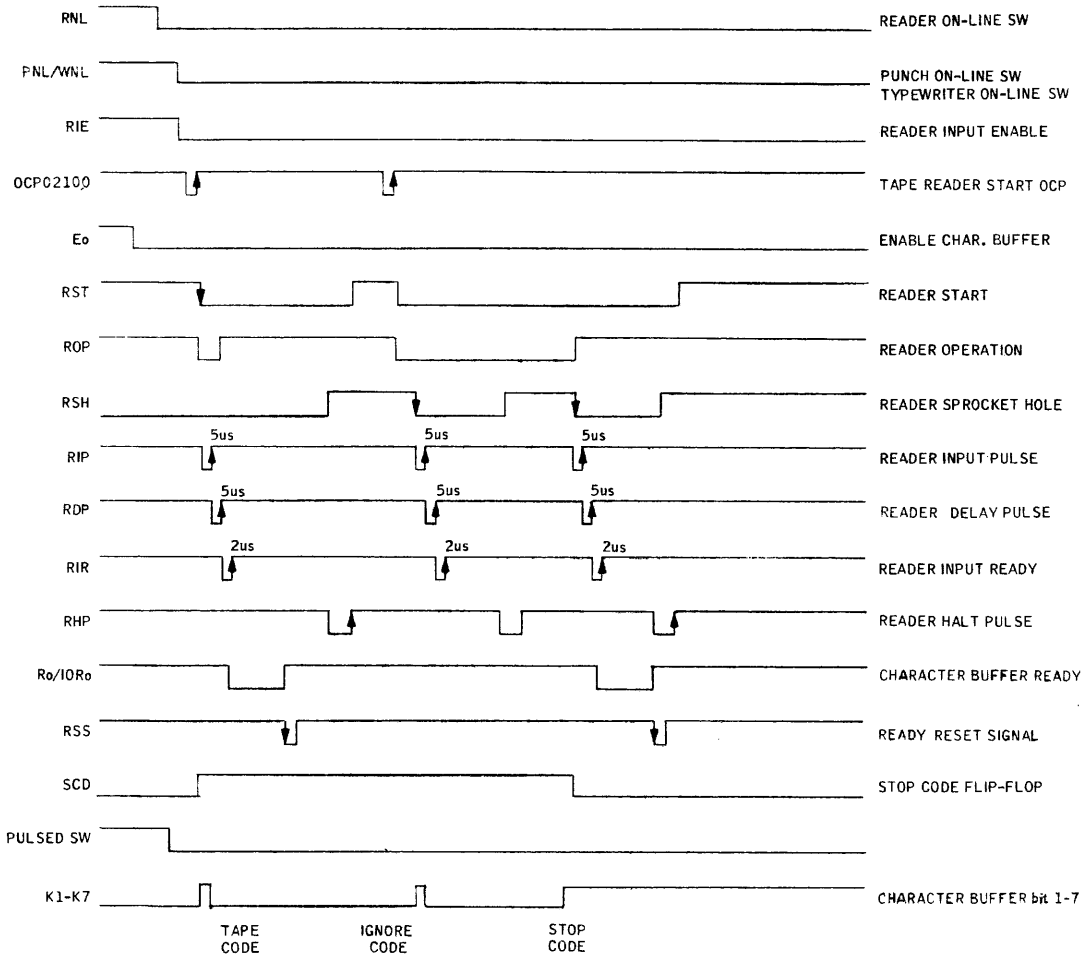


Figure 5-34. Paper Tape Reader On-Line Pulsed Mode, Timing Diagram

are recognized as ignore code. The tape is read when a stop code is sensed which halts the reader. Refer to Section II for detailed program fill information and to Figure 5-37.

5-19 PAPER TAPE PUNCH

The paper tape punch is capable of operating at rates up to 60 characters per second in either on-line or off-line operation. (Refer to Figures 5-37 through 4-50 and to the DDP-24 Service Manual, Volume II.)

Punch power is controlled from the control processor. Tape leader can be made by depressing the tape feed pushbutton on the control panel. A pushbutton on the punch is used for backspacing the punch one character.

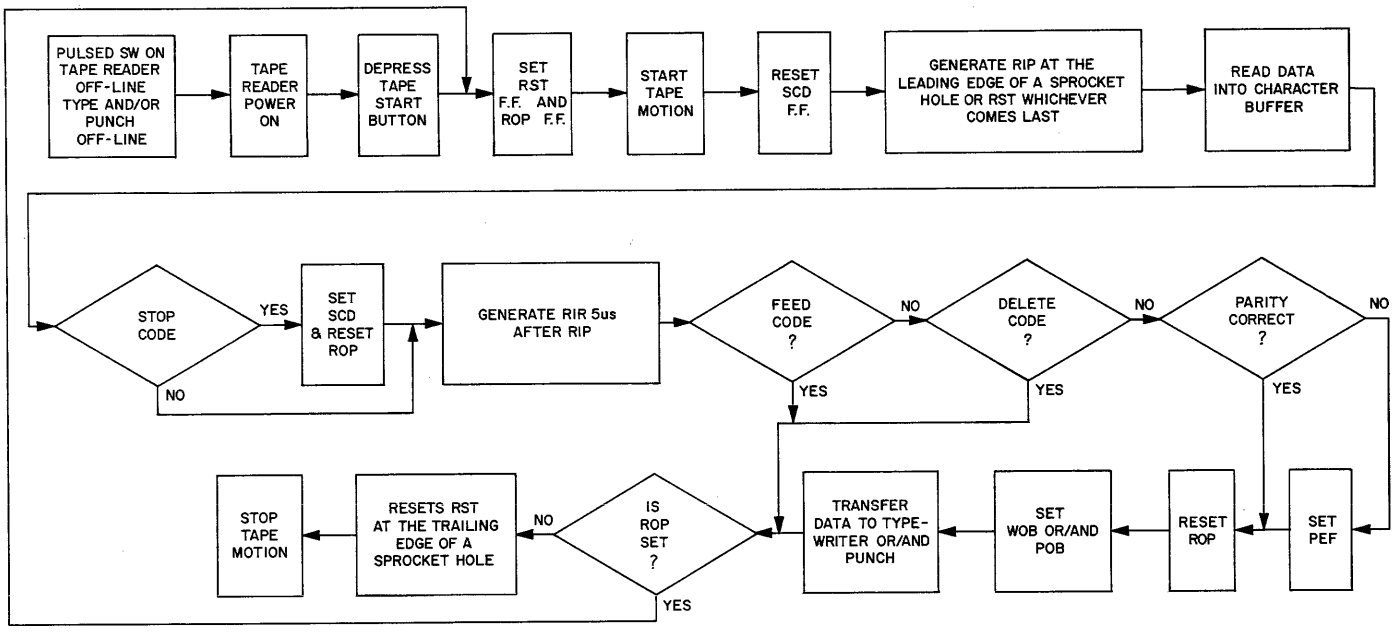


Figure 5-35. Paper Tape Reader Off-Line Pulsed Mode, Flow Chart

To operate the punch, the DDP-24 must generate signals which energize the punch and feed the magnets with a 4.5 ms pulse every 16.7 ms.

When the punch power switch on the control panel is turned on, power is applied to the punch motor and the punch timing pulse multivibrator (PTP) starts. The punch ON-LINE switch and at least one other on-line switch should be on. When an OCP02200 is initiated, the punch output select flip-flop (POS) will set while other select flip-flops will reset. With the punch in the on-line condition and with POS set, the punch on-line (PON) signal becomes true. This permits the busy flip-flop to set with the output transfer pulse (OXP). OXP strobes data into the character buffer. When POB is set, a 4.5-millisecond, one-shot, punch output pulse is triggered with PTP creating a punch drop-in pulse (PDP). According to the data in character buffer (K1 in channel 1, K2 in channel 2, K3 in channel 3, K4 in channel 4, parity bit in channel 5, K5 in channel 6, and K6 in channel 7), PDP will energize the punch magnets. At the trailing edge of PDP, POB is reset, blocking PTP from triggering the one-shot POP.

If an OCP 01000 is initiated, the stop code punch flip-flop (SCF) will set, and PUB becomes true. This permits PTP to set POP, but if POB is set, the punch is inhibited. When POB is reset, POP will energize the channel 8 punch magnet. The trailing edge of POP resets SCF and PUB becomes false, inhibiting PTP.

When the TAPE FEED pushbutton is depressed, PUB becomes true, enabling PTP which triggers POP every 16.7 milliseconds as long as the pushbutton is depressed. When the TAPE FEED pushbutton is depressed, only the tape feed punch magnet is energized. Refer to Figures 5-41 and 5-42.

When the punch backspace pushbutton is depressed, a pulse is generated which triggers the one-shot punch reverse pulse (PRP) which generates a 4.5 millisecond pulse energizing the backspace solenoid to reverse the punch feed one character. When punching, the punch backspace can be used to delete characters from the typewriter. (Refer to Figures 4-50 and 4-41.)

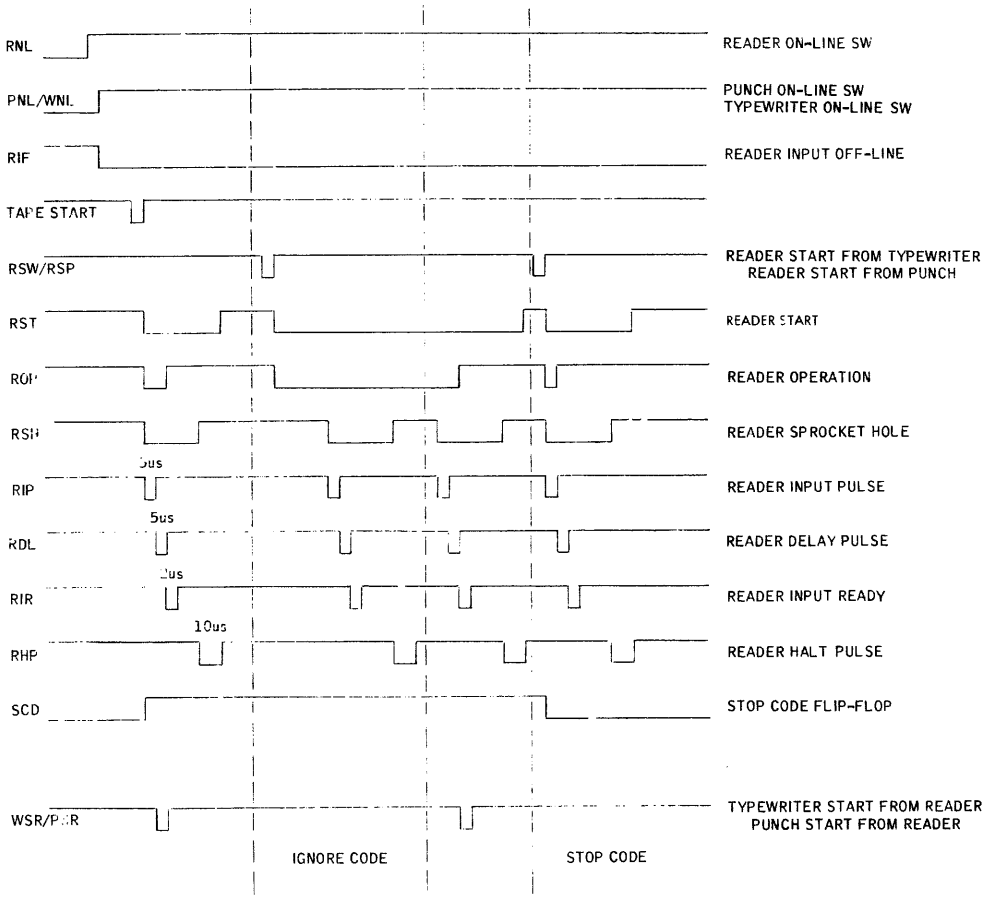


Figure 5-36. Paper Tape Reader Off-Line, Timing Diagram

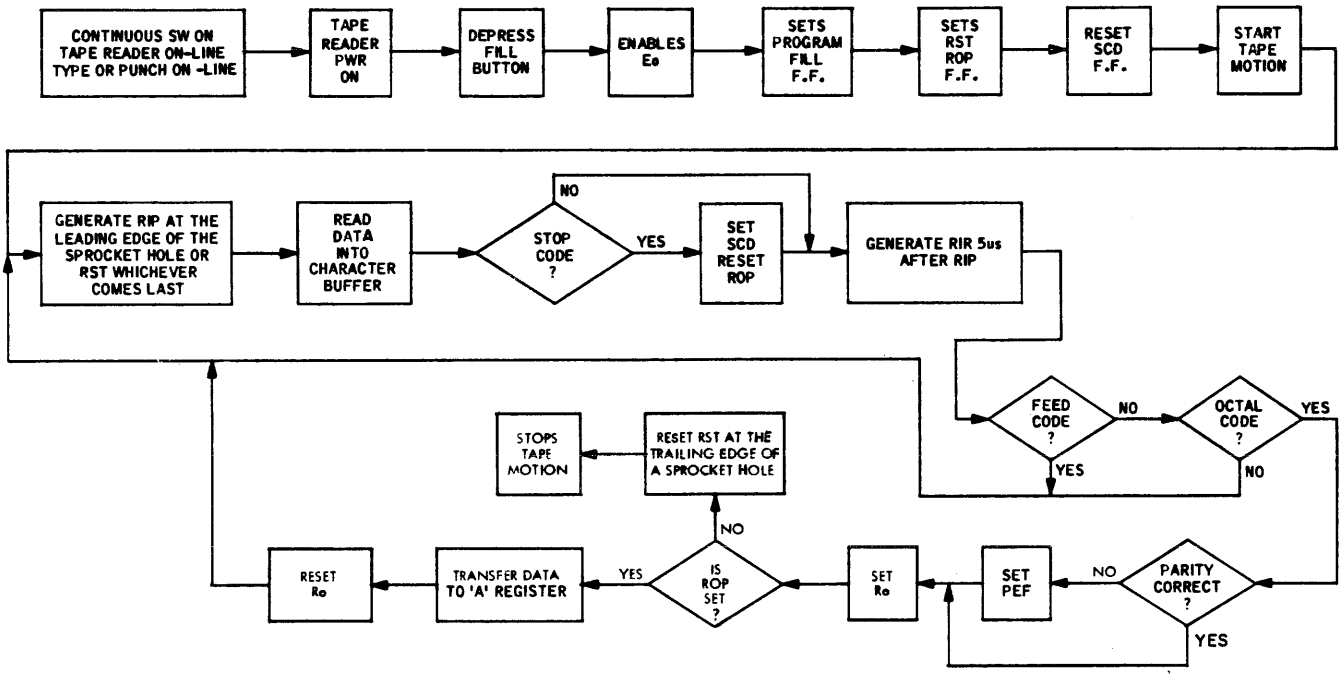


Figure 5-37. Paper Tape Reader Program Fill, Flow Chart

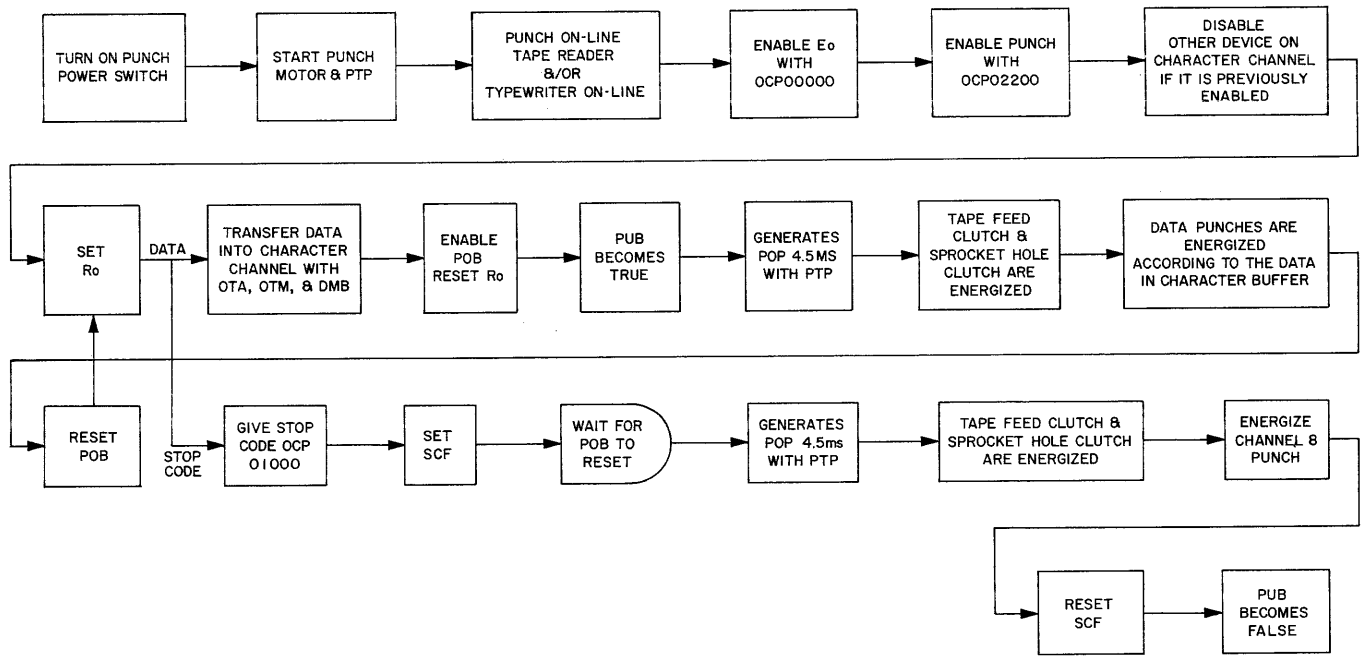


Figure 5-38. Paper Tape Punch On-Line, Flow Chart

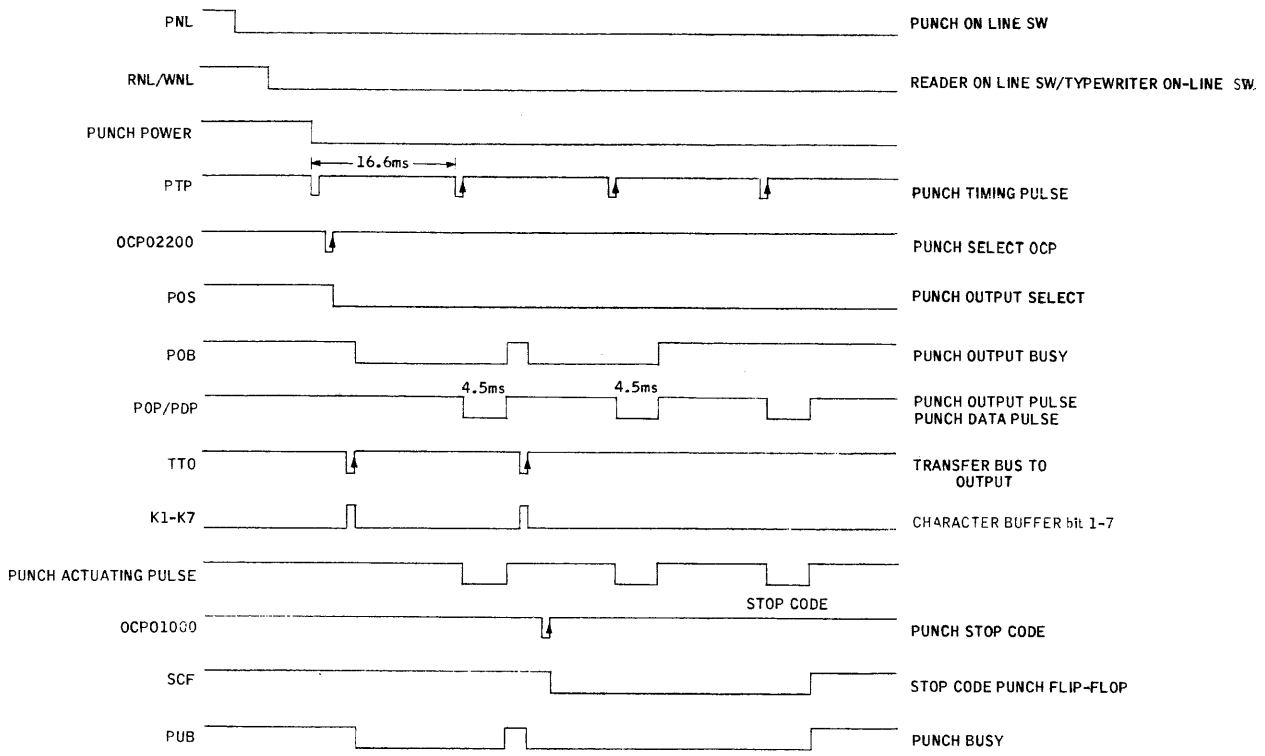


Figure 5-39. Paper Tape Punch On-Line, Timing Diagram

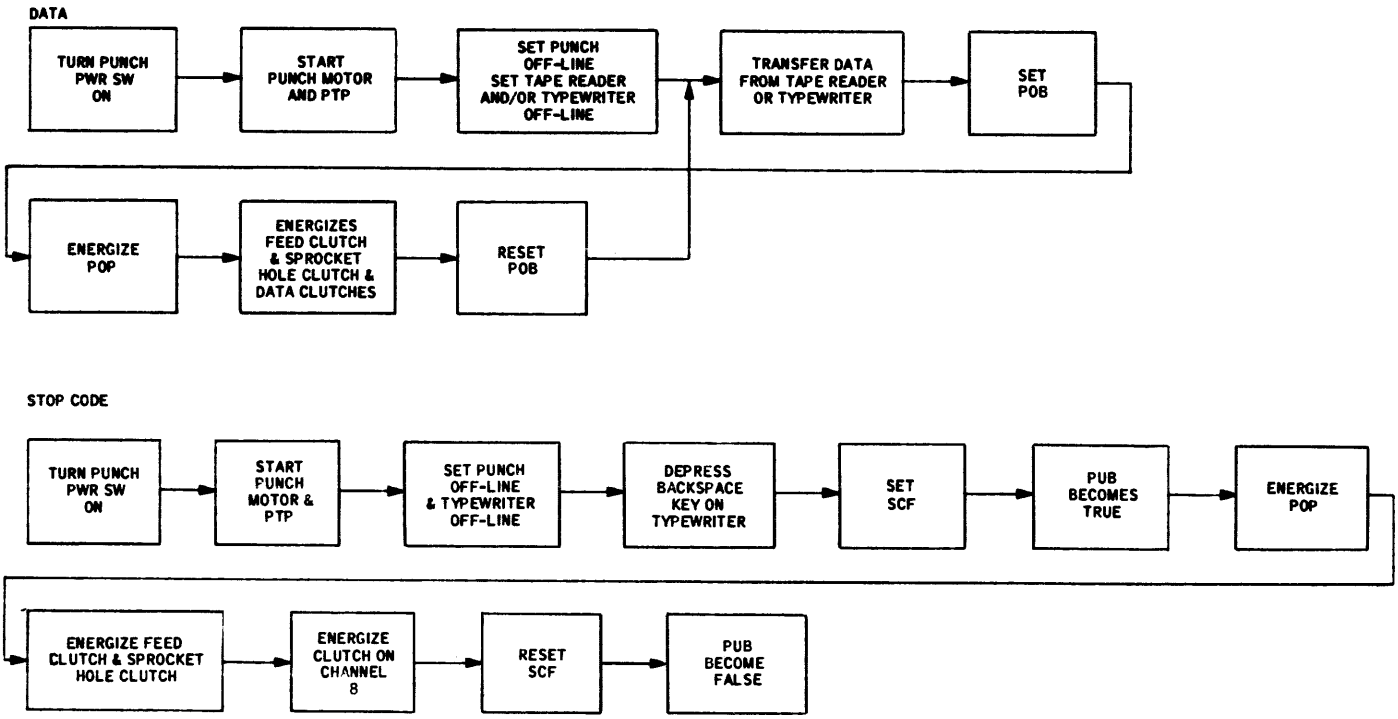


Figure 5-40. Paper Tape Punch Off-Line Data and Stop Code, Flow Chart

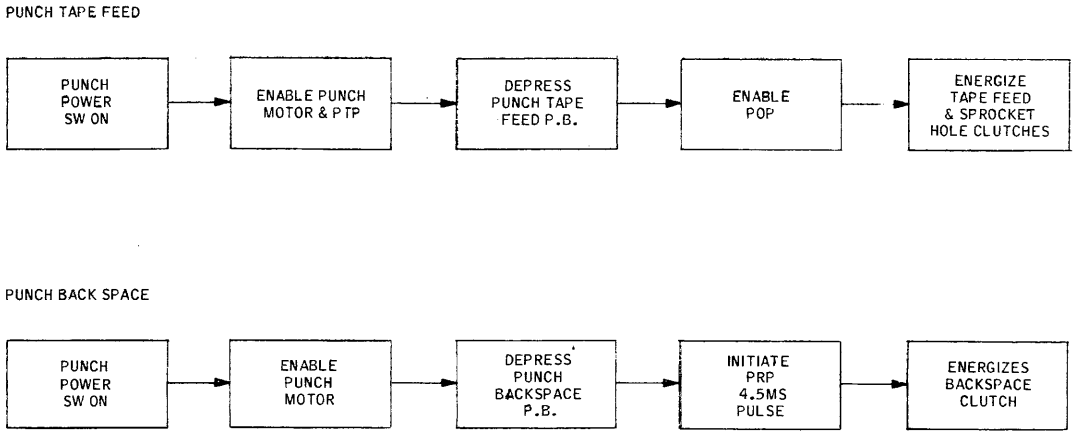


Figure 5-41. Paper Tape Punch Tape Feed and Backspace, Flow Chart

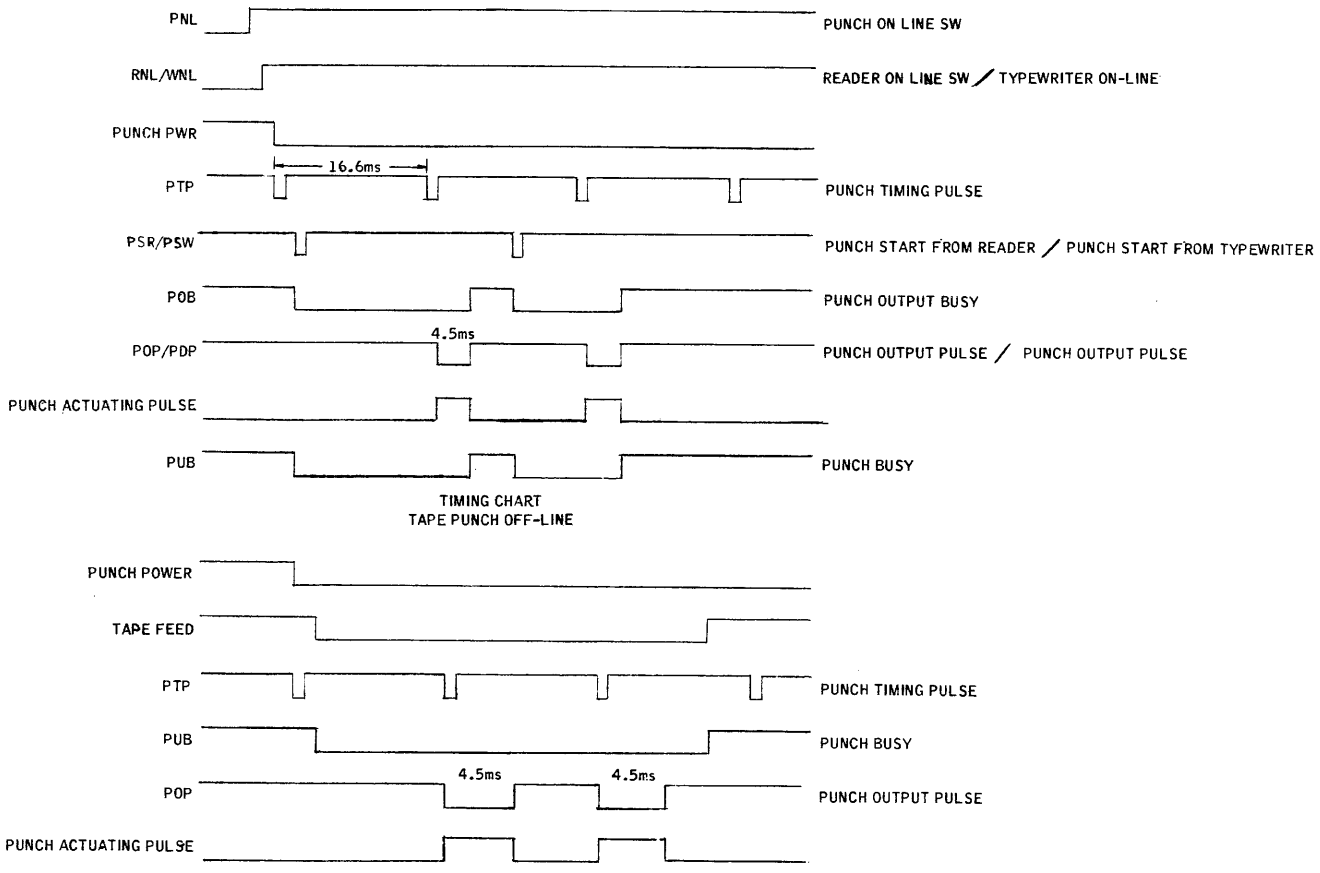


Figure 5-42. Paper Tape Punch Tape Feed, Timing Diagram

SECTION VI
MAINTENANCE

6-1 INTRODUCTION

The instructions and information provided in this section reflect the general maintenance procedures required to maintain the DDP-24 in proper operating condition. Specific and detailed troubleshooting procedures are contained in the DDP-24 Service Manual. Detailed information on the S-PAC digital modules, the S-BLOC assemblies and the RP-32 power supplies may be found located in the Instruction Manual for 1MC S-PAC Digital Modules. Information pertaining to the memory, tape perforator, tape reader and I/O typewriter is contained in the manual for the respective device. All other optional equipments will be supported by manuals supplied as required.

6-2 MAINTENANCE PANEL CONTROLS AND INDICATORS

Figure 6-1 shows the maintenance control panel, located behind the upper front panel in bay 2. The maintenance panel is used in conjunction with prescribed diagnostic routines to locate equipment malfunctions. The indications provided by the operating control panel in bay 3 are also used. Table 6-1 lists the location and the function of the switches and indicators on the maintenance panel.

6-3 POWER FAILURE

Adequate indicators and controls are provided on the standard computer to facilitate the localizing of power failures within the computer. Figure 6-2 shows the schematic diagram of the AC power distribution within the DDP-24 System. If an overload occurs on the AC line, circuit breaker, CB1 on the AC panel at the rear of bay 2 will open. To localize the trouble, remove all AC connectors from the wire mold strips and check the circuit breaker operation. If no trouble is evident, replace the AC plugs individually until the problem is localized.

Figures 6-3 and 6-4 show the DC power distribution from the two RP-32 power supplies located in bay 2 and bay 4. The RP-32 power supplies provide low voltage (-6V, -18V, and +12V) to the S-BLOC assemblies. Each power supply is equipped with a DC FAIL indicator which will light when any of the three output voltages fail. In addition, three circuit breakers prevent damage to the supply under overload conditions. An AC indicator and an input fuse on each supply monitors and protects the input AC voltage.

Two additional power supplies located in bay 1 provide low voltage to the control and maintenance panel. Figure 6-5 shows the schematic diagram of the power supply assembly. The -100 VDC supply furnishes -2.5 VDC and -90 VDC to the indicator-switch

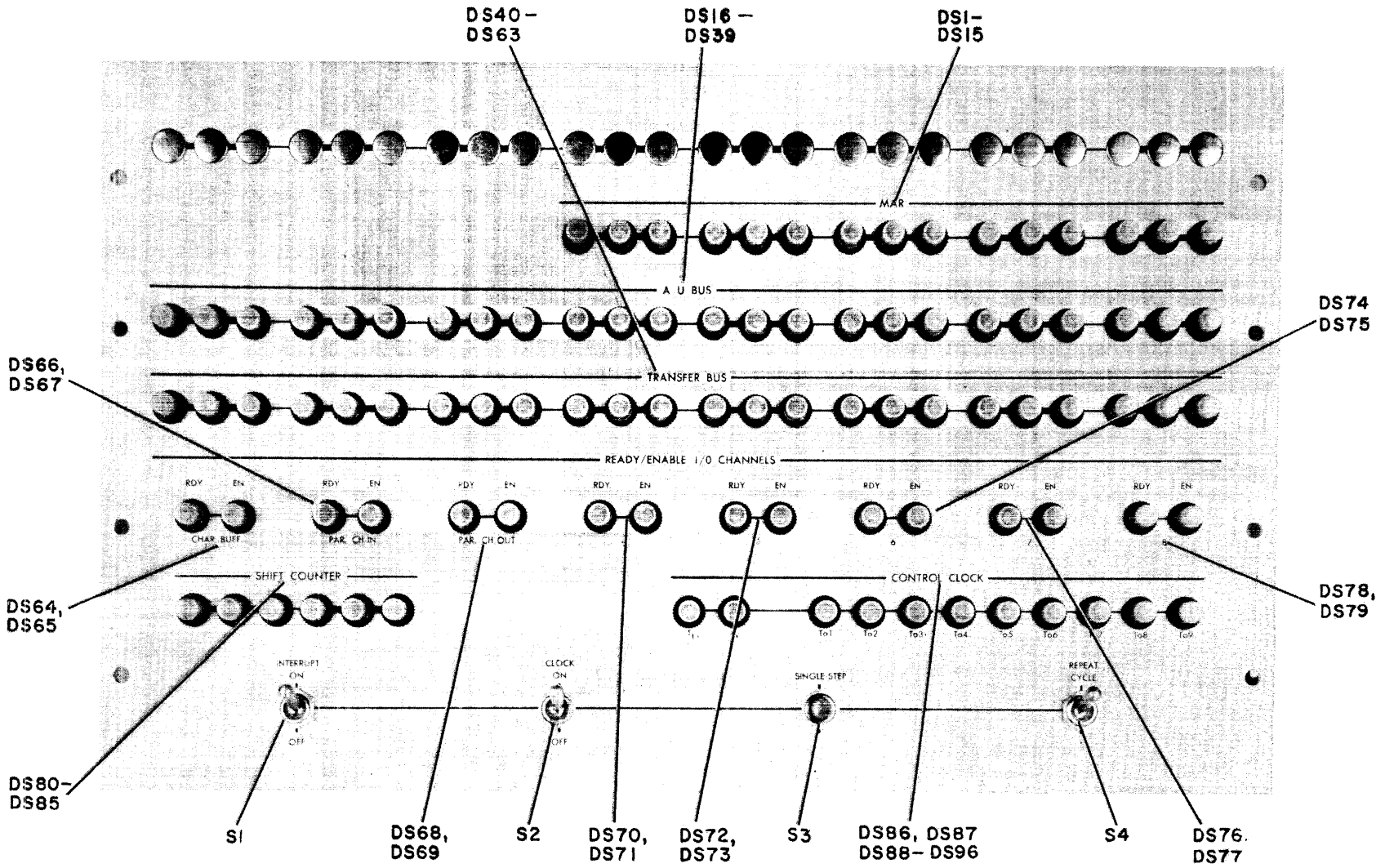


Figure 6-1. Maintenance Panel, Operating Controls and Indicators

lamps on the control and maintenance panel. The -24V supply provides low voltage to the SD-30 PACs located in S-Bloc (4A). A 10 amp fuse mounted on the chassis protects the -24 VDC supply against an overload condition.

The individual blower units in bay 2, 3, and 4 and the TCM-32 memory unit in bay 1 are equipped with fuses for power short circuit protection.

TABLE 6-1

MAINTENANCE PANEL CONTROLS AND INDICATORS

Switch or Indicator	Function
MAR DS 1 - DS 14	Indicates the binary content of the memory address register.
AU BUS DS 15 - DS 38	Indicates the status of the gates which comprise the AU bus.
TRANSFER BUS DS 39 - DS 62	Indicates the status of the gates which comprise the transfer bus.
READY/ENABLE I/O CHANNELS PAR CH IN RDY - DS 63 EN - DS 64	Indicates the status of the parallel channel input flip flops.
CH B IN RDY - DS 65 EN- DS 66	Indicates the status of character buffer input flip flops.
PAR CH OUT RDY - DS 67 EN - DS 68	Indicates the status of the parallel channel output flip flops.
CONTROL CLOCK T_f - DS 77 T_t - DS 78 T_o1 - T_o9 DS 79 - DS 87	Indicates the fetch portion of the computer cycle. Indicates the transition portion of the computer cycle. Indicates the timing of the operate portion of the computer cycle.
INTERRUPT S1	ON - Enables the automatic interrupt capabilities of the input-output channels.

TABLE 6-1 (Cont)

MAINTENANCE PANEL CONTROLS AND INDICATORS

Switch or Indicator	Function
CLOCK S2	OFF - Disables the computer one megacycle clock.
SINGLE STEP S3	Press to produce a single one megacycle clock pulse when the CLOCK switch (S1) is in the OFF position.
REPEAT CYCLE S4	UP position - provides repeated execution of the same command, excluding the skip and jump commands.
CH B OUT RDY - DS 69 EN - DS 70	Indicates the status of the character buffer output flip flops.
5 RDY - DS 71 EN - DS 72	Indicates the status of I/O channel 5 flip flops.
6 RDY - DS 73 EN - DS 74	Indicates the status of I/O channel 6 flip flops.
7 RDY - DS 75 EN - DS 76	Indicates the status of I/O channel 7 flip flops.
8 RDY - DS 77 EN - DS 78	Indicates the status of I/O channel 8 flip flops.
SHIFT COUNTER DS 71 - DS 76	Indicates the status of the six shift counter flip flops.

6-4 PREVENTIVE MAINTENANCE PROCEDURES

Under normal operating conditions, the standard DDP-24 requires a minimum of preventive maintenance. Extreme environmental conditions may necessitate that the following procedures be performed more often than the frequency indicated. For trouble-free operation, certain vital points should be inspected at periodic intervals and the

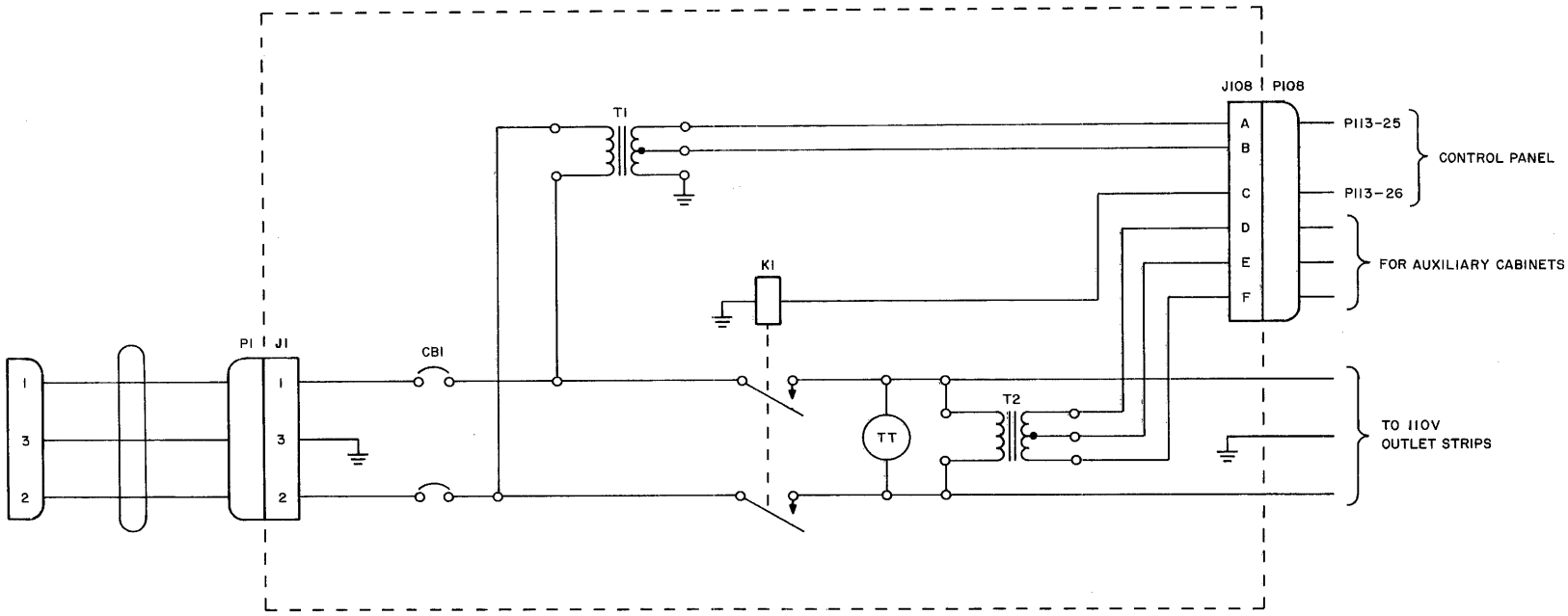


Figure 6-2. AC Power Distribution, Schematic Diagram

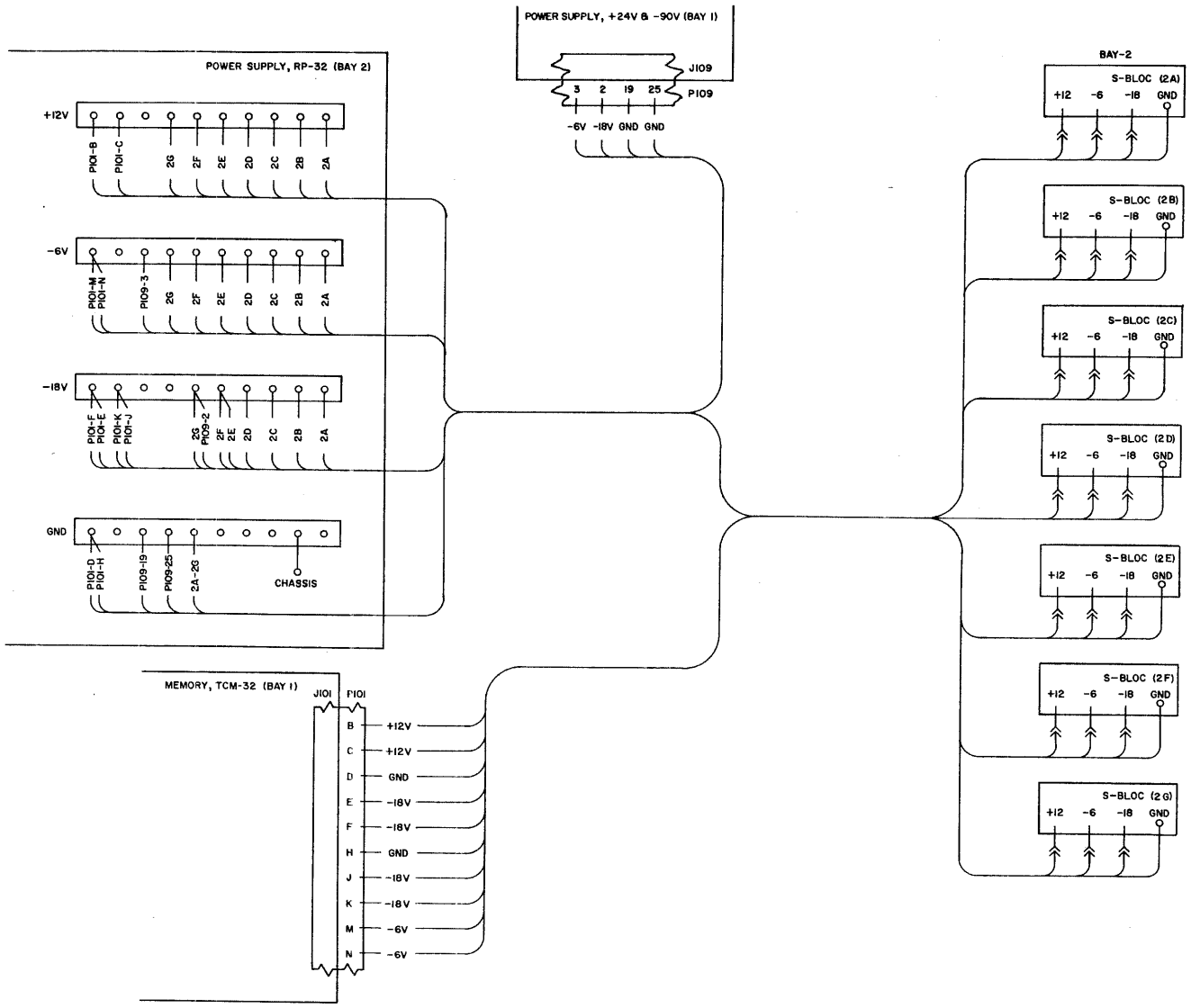


Figure 6-3. DC Power Distribution Diagram (RP-32, Bay 2)

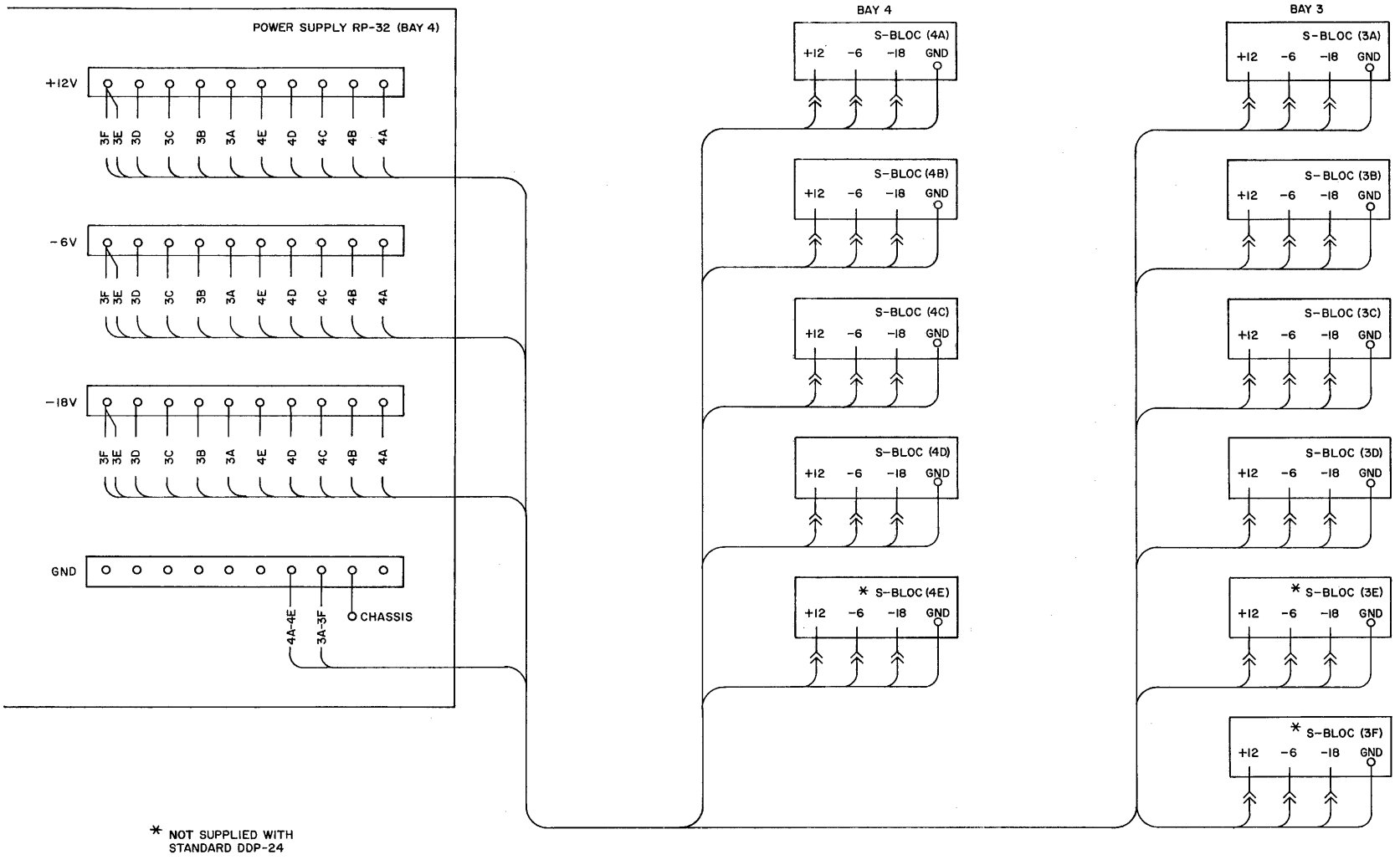


Figure 6-4. DC Power Distribution Diagram (RP-32, Bay 4)

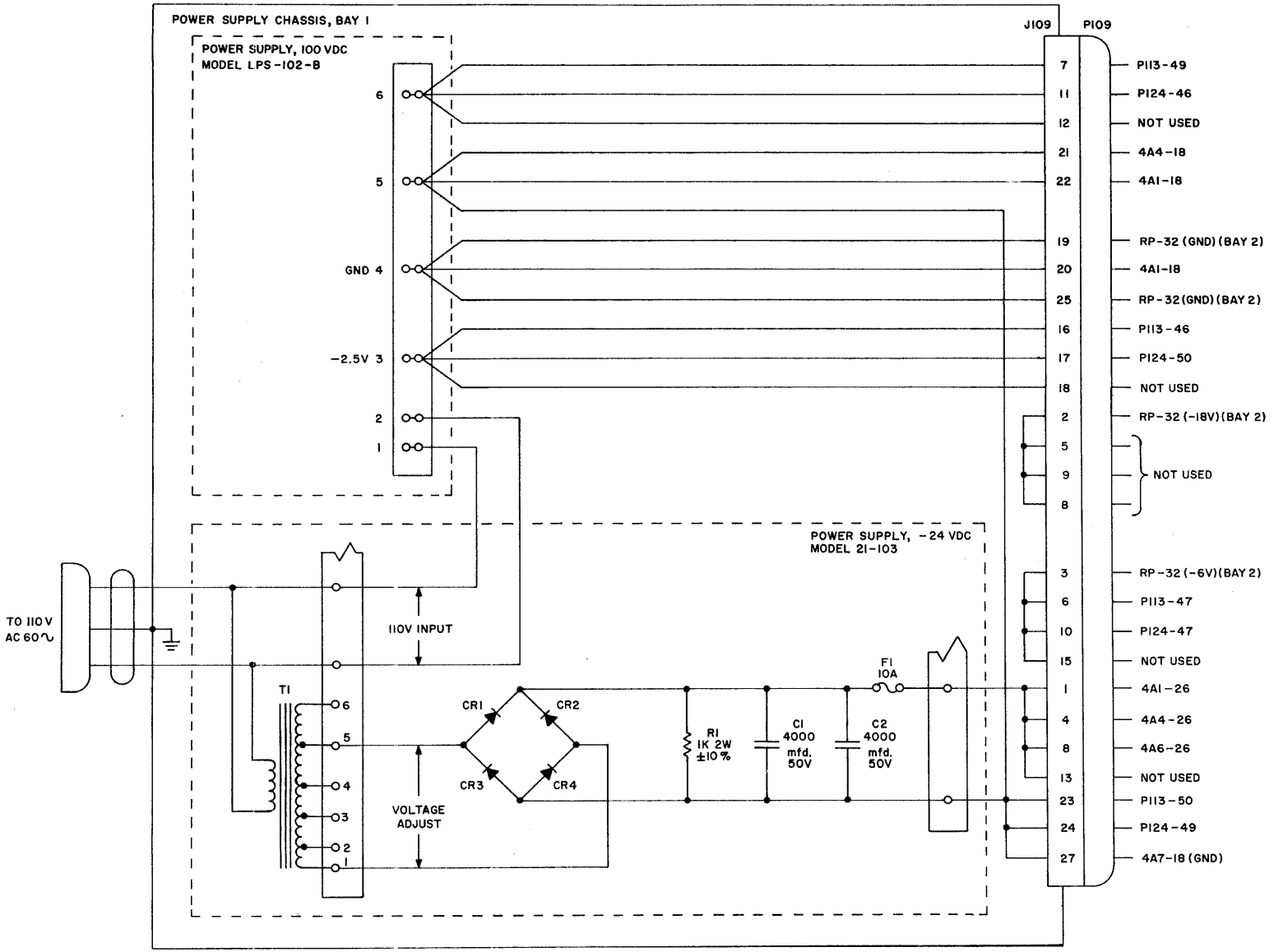


Figure 6-5. DC Power Distribution Diagram -100, -24 V Power Supply Assembly

necessary replacements made when trouble is discovered. While this equipment has been designed for reliable operation, a certain amount of wear and deterioration must be expected in an apparatus of this nature. If detected and corrected at an early stage, troubles from these causes can be held to a minimum. Preventive maintenance procedures not listed in this section for peripheral or for special devices supplied will be contained in an applicable manual supplied with the device.

6-4.1 Digitronics Tape Reader (Model 2500)

6-4.1.1 Periodic Inspection. – An over-all inspection of the equipment is recommended as a precautionary measure immediately before it is put into service, and at intervals of six to nine months, thereafter. Such an inspection involves a complete examination of electrical wiring and mechanical details in addition to inspection of the output signals and the proper functioning of the operating controls. The inspection table below was computed on the basis of a 40 hour week. When customer usage exceeds these limits, adjustments should be made to the table.

TABLE 6-2
PERIODIC INSPECTION

DAILY	MONTHLY	SEMI-ANUALLY
Read head, tape guide, pinch roller, capstan and brake. Clean all the above as required.	Inspect pinch roller and capstan gap, gearing in motor drive assembly.	Inspect all moving parts for wear, check data channel outputs, sprocket output and power supply voltages.

6-4.1.2 Lubrication. — With the exception of the motor assembly, the tape reader requires no lubrication. All bearings, excluding the motor bearings, are permanently lubricated and require no attention. Double shielded ball bearings are used throughout the tape transport system to prevent the entry of dust. Whenever a bearing shows any sign of sticking, it should be replaced. The only lubrication to be done is to the motor bearings. These should be lubricated monthly with ANDROL L456, Lehigh Chemical Co. (2 - 3 drops or until felt is saturated.)

6-4.1.3 Cleaning. — When it is determined by inspection that the components of the unit require cleaning, it is recommended that a cotton swab or lint-free cloth be used. Dampen the cloth with denatured alcohol and clean the dirty area.

6-4.2 IBM Typewriter

6-4.2.1 Lubrication and Maintenance. – For lubrication and preventive maintenance of the typewriter section, follow IBM Series 73 I/O Writer, Instruction Manual.

6-4.3 Tape Spooler 4566

6-4.3.1 Periodic Inspection. - An over-all inspection of the equipment is recommended as a precautionary measure immediately before it is put into service, and at intervals not to exceed 9 months depending upon the amount of use thereafter.

6-4.3.2 Routine Maintenance. - No mechanical parts of the equipment require lubrication at any time. All bearings are permanently lubricated and require no further lubrication. Double-shielded ball bearings are used throughout the tape transport system to prevent the entry of dust.

6-4.4 Tape Perforator, Model 420

6-4.4.1 Lubrication. - The tape punch drive gearing and escapement mechanisms are enclosed in a rectangular case consisting of an oil pan frame and front and top covers. A supply of oil in the oil pan is distributed as a mist throughout the mechanism by an oil lead gear partially submerged in the oil. The remainder of the tape punch mechanism is oiled at specific points, as noted below. Lubricate the unit as follows:

a. Punch Drive Mechanism. Keep the oil pan filled to a level between the two oil level marks on the outer bearing plate with light turbine oil, viscosity 160 SSU, Texaco Regal A R&O or equivalent. Remove the oil filter plug to add oil. The turbine oil should be changed when dirty; check every 200 hours of operation, as the change period varies with environmental dirt, temperature and perforator duty cycle. Oil level should be checked daily.

b. Capstan Drive. Lubricate both sides of each friction clutch with silicone oil (DC200, 350CS), inserting the tip of the oiling syringe 1/4 inch between the fiber friction washer and the black nylatron gear. To improve clutch run-in, relubrication should follow the first 20, 50, and 100 hours, and thereafter each 200 hours.

Lubricate input and output shaft bearings at each 200-hour period, using rust and oxidation inhibited oil, SAE20 grade.

Lubricate the escapement armature level fulcrum every 200 hours, using Tally pivot grease A, supplied in the lubrication kit. Wipe the mechanism clean of all excess lubricant.

c. Drive Motor. Lubricate the drive motor bearings twice yearly, using rust and oxidation inhibited oil, SAE20 grade.

d. Reel Drive. Lubricate the reel drive shaft bearings twice yearly with X SAE20 oil.

See Tally Tape Perforator Manual Model 420 - Page 19.

6-4.4.2 Cleaning. - After each spool of tape has been punched, empty the chad box and brush all loose chads from the tape guide. Failure to empty the chad box may result in jamming the transparent chad chute.

6-4.5 Blower Units

Blower units are installed at the bottom of bays 2, 3, and 4. The only maintenance required is that each filter be cleaned at periodic intervals to allow free movement of air into the computer. The filter is of the permanent type and can be cleaned by washing with warm water and a detergent to remove the accumulated dirt.

6-4.5.1 Removal and Replacement of Filters. - Remove and replace the filter as follows.

a. Locate the cabinet grillwork on the lower front of bay 2 and remove by pulling two levers which release it from the cabinet base.

b. Open the front access door of bay 2.

c. Locate the blower filter.

d. Slide the filter upward (approximately 1 inch) against the upper base of its encasement.

e. Pull the bottom of the filter forward (approximately 2 inches) and remove with a forward downward motion.

f. Procure the new replacement and install in the reverse order of removal outlined steps a. through e. The same procedure applies for filter removal from bay 3 and bay 4.

6-4.5.2 Memory Unit Filter Removal and Replacement. - The memory unit, model TCM-32 contains four separate filters which may be either the permanent or disposable type. Each filter should be inspected approximately every two weeks and cleaned or replaced as necessary. The permanent type filter should be washed in warm water with a detergent, and replaced. To remove the filters from the memory, perform the following procedures.

a. Open the TCM-32 tilt-drawer unit located at the lower front of bay 1.

b. Locate two filters seated in metal flanges.

c. Remove the two filters by sliding them upward against the base of the encasement.

d. To replace the filters, perform steps a. through d., in the reverse order.

e. Open the bay 1 access door.

f. Locate two filters seated in metal flanges mounted on the bottom of the bay 1 cabinet.

g. Remove the two filters by snapping them upward from their encasement.

h. Procure and make the necessary replacement. Installation is in the reverse order of removal outlined in steps a. through g.

6-5 UNIT REMOVAL AND REPLACEMENT INSTRUCTIONS

If it becomes necessary to remove and replace any of the following units mounted in the standard DDP-24, perform the applicable procedures.

6-5.1 Blower Unit

a. Disconnect the blower unit AC input power plug from the AC wiremold strip.

b. Remove the four bolts which secure the blower unit mounting brackets to the cabinet.

c. Remove the four bolts which secure the blower unit to the mounting brackets.

d. Locate the main power distribution panel at the rear of bay 2.

e. Remove the four bolts which secure the distribution panel to the cabinet.

f. Dismount the distribution panel to provide clearance for blower unit removal.

g. Hold the blower unit firmly and remove from the rear of the cabinet.

h. Installation of the unit is the reverse of the removal procedure outlined in steps a. through g.

Note

If bay 2 provides an optional H Bloc, loosen the four bolts which secure the Bloc to the cabinet and tilt it to provide clearance for blower removal.

i. To remove the blower units in bay 3 and in bay 4, follow dismantling steps a. through h. Lift the blower units up (approximately seven inches) and remove through the front of the cabinets.

6-5.2 Power Supply Assembly (-24-volt and -100-volt supplies)

a. Remove the AC input power plug from DDP-24 console rear before proceeding with dismantling instructions.

b. Open the bay 1 rear access door.

c. Locate the -24-volt and -100-volt power supplies, both mounted on a single frame.

d. Disconnect the AC input power plug from the AC wiremold strip.

e. Locate the DC output power plug, P109, mounted on the power supply frame and remove it from the output receptacle.

f. Hold the power supply unit firmly and remove the four bolts which secure the frame to the console.

g. Remove the frame with the power supply unit and withdraw it from the rear of the console.

h. To remove the -100 volt power supply from the frame, remove the four screws located beneath the supply.

i. Remove the cover plate located on the -100 volt power supply enclosure in order to gain access to components.

j. Install the power supply unit in the reverse of the order of removal outlined in steps d. through i.

k. Close the bay 1 rear access door and connect the AC input power plug to the rear of the console.

6-5.3 Tally Tape Perforator Model 420

a. Remove the AC input power plug from the DDP-24 console rear before proceeding with the dismantling instruction.

b. Open the bay 1 rear access door.

c. Locate the tape perforator.

d. Disconnect the tape perforator AC input power plug from the AC wiremold strip.

e. Disconnect the logic input plug, P114, from the receptacle located at rear of the tape perforator.

f. Hold the tape perforator unit firmly and remove the four bolts located on the front panel that secure the tape perforator to the bay chassis.

g. Remove the tape perforator from its mounting base and remove it from the front of console.

h. Install the tape perforator in the reverse of the order of removal outlined in steps a. through g.

i. Close the bay 1 rear access door and connect the AC input power plug to the rear of the console.

6-5.4 Tape Reader, Model 2500 Removal and Replacement

a. Remove the AC input power plug from the DDP-24 console rear before proceeding with dismantling instructions.

b. Open the bay 1 rear access door.

c. Locate the paper taper reader.

d. Disconnect the tape reader AC input power plug from the AC wiremold strip.

e. Disconnect the logic input plug, P116, from rear of the tape reader.

f. Hold the paper tape reader unit firmly and remove the four bolts located on the front panel that secure the tape reader to the bay chassis.

g. Remove the paper tape reader unit from its mounting base and remove it through the front of the console.

h. Procure and make the necessary replacements and install the tape reader in the reverse of the order of removal outlined in steps a. through g.

i. Close the bay 1 rear access door and connect the AC input power plug to the rear of the console.

6-6 MAINTENANCE

Figures 6-6 and 6-7 show the schematic diagrams of the maintenance and control panel respectively. Input signals and power for the indicators and switches are provided by the input connectors at the rear of each panel. These connectors may be removed when performing maintenance operations on the panel circuits or wiring.

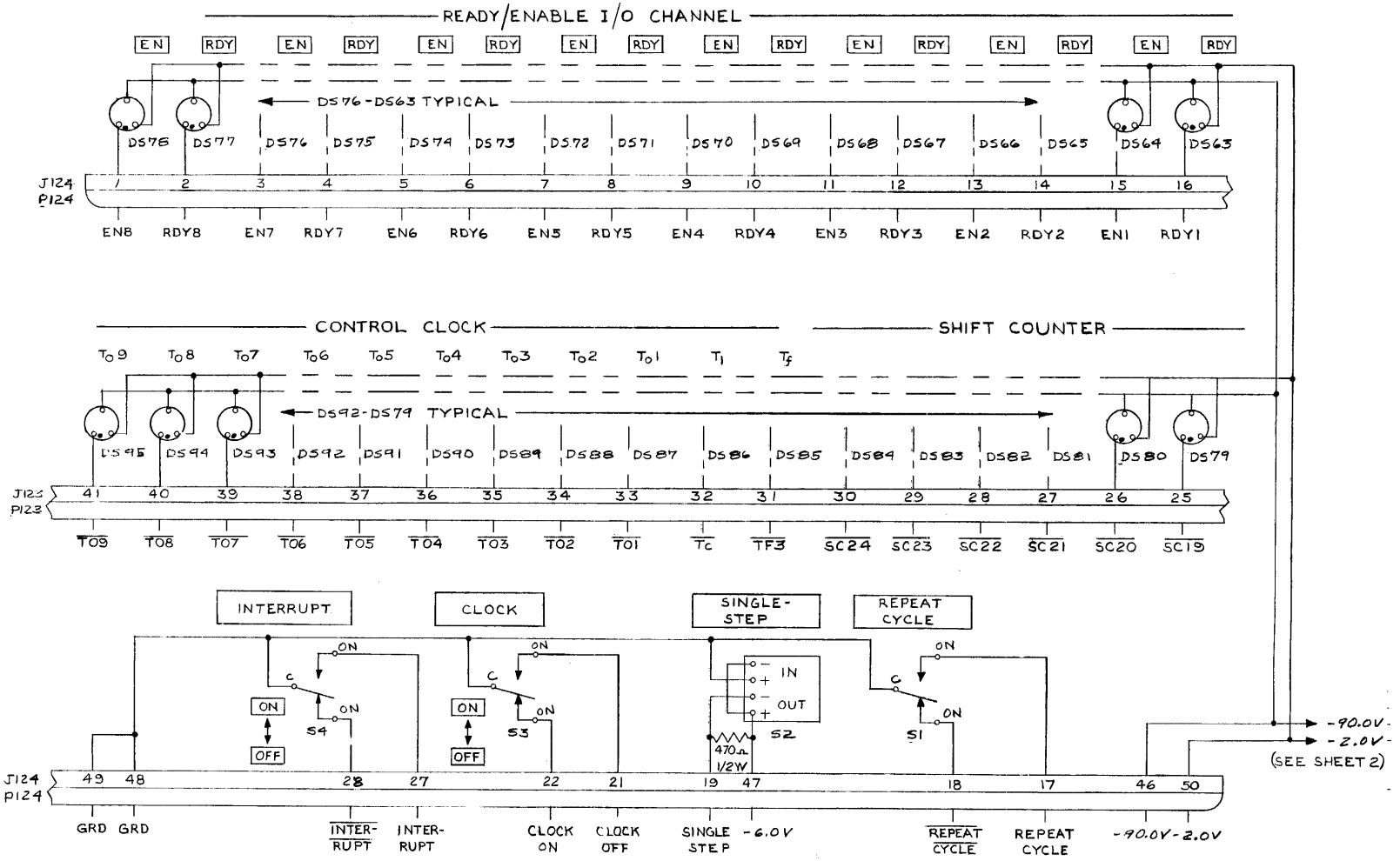


Figure 6-6. Maintenance Panel, Schematic Diagram
Page 1 of 2

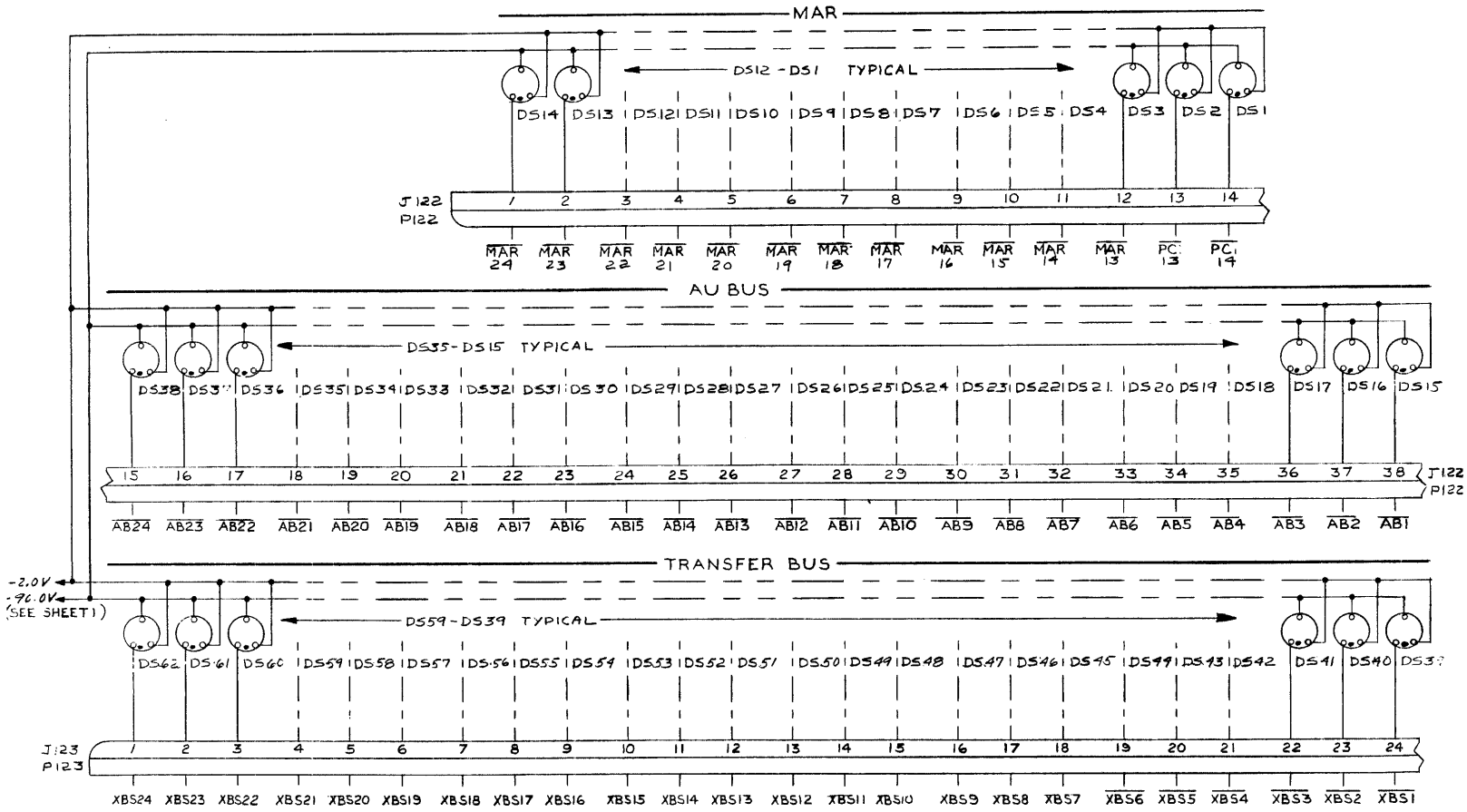


Figure 6-6. Maintenance Panel, Schematic Diagram
Page 2 of 2

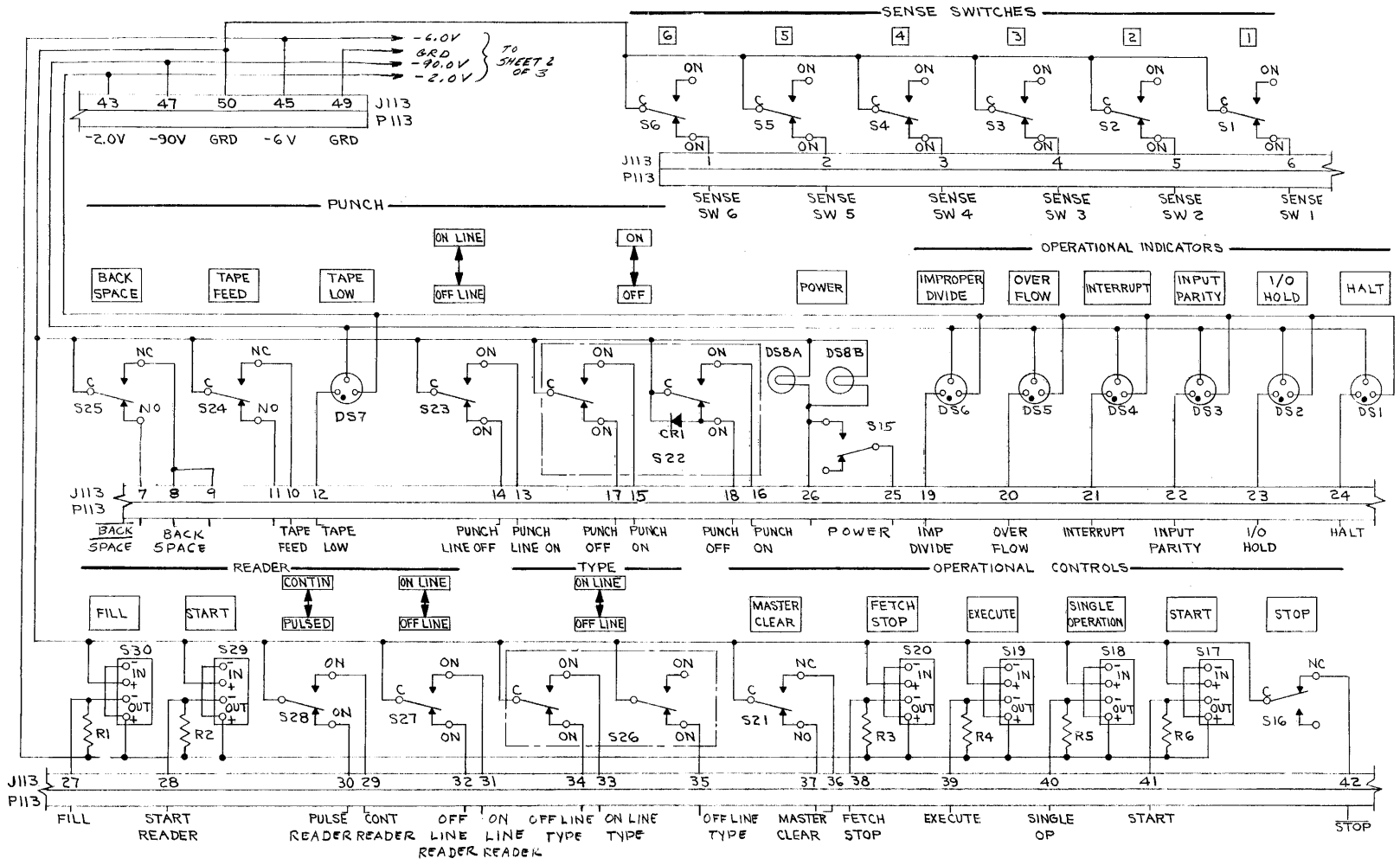


Figure 6-7. Control Panel, Schematic Diagram
Page 1 of 3

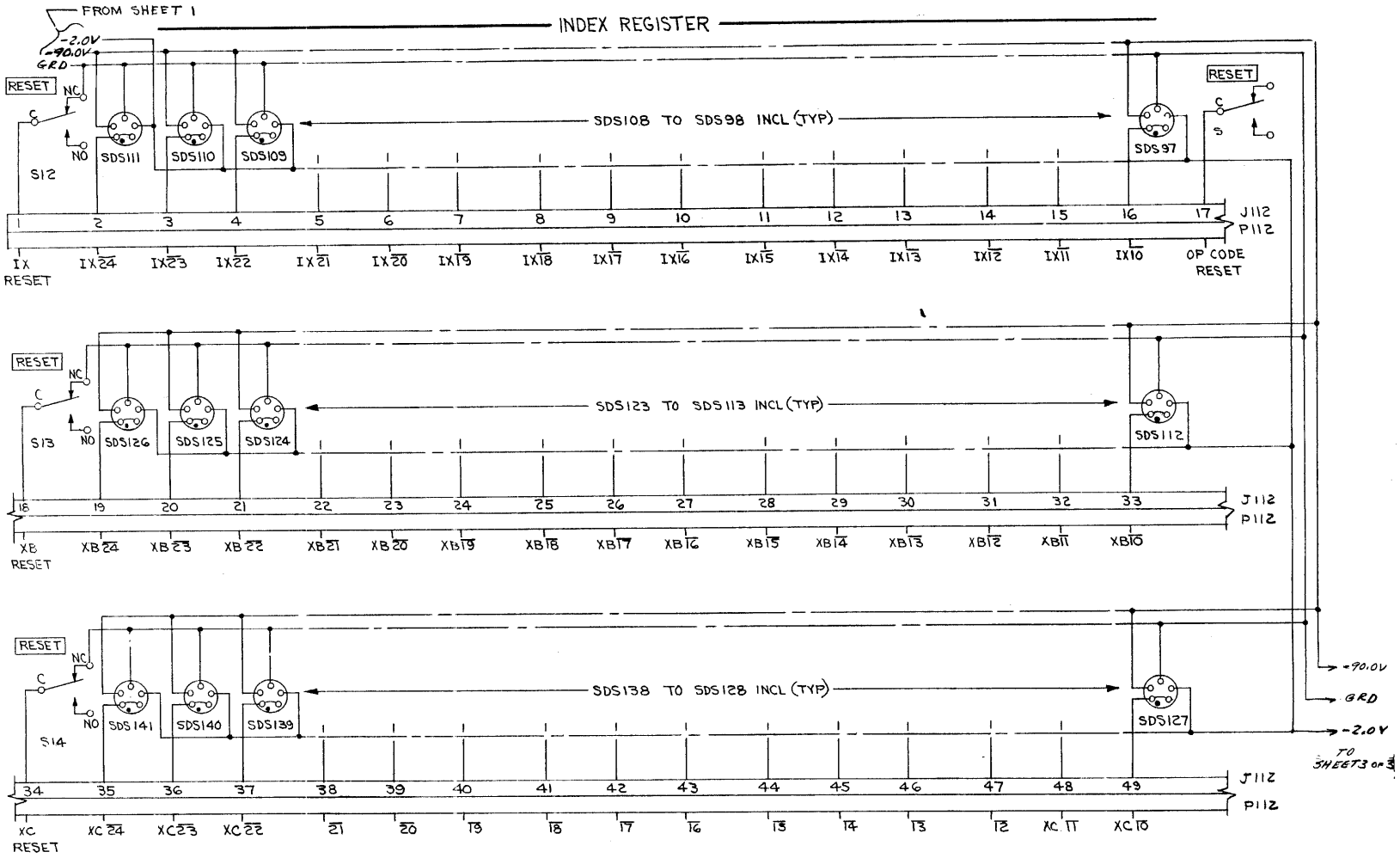


Figure 6-7. Control Panel, Schematic Diagram
Page 2 of 3

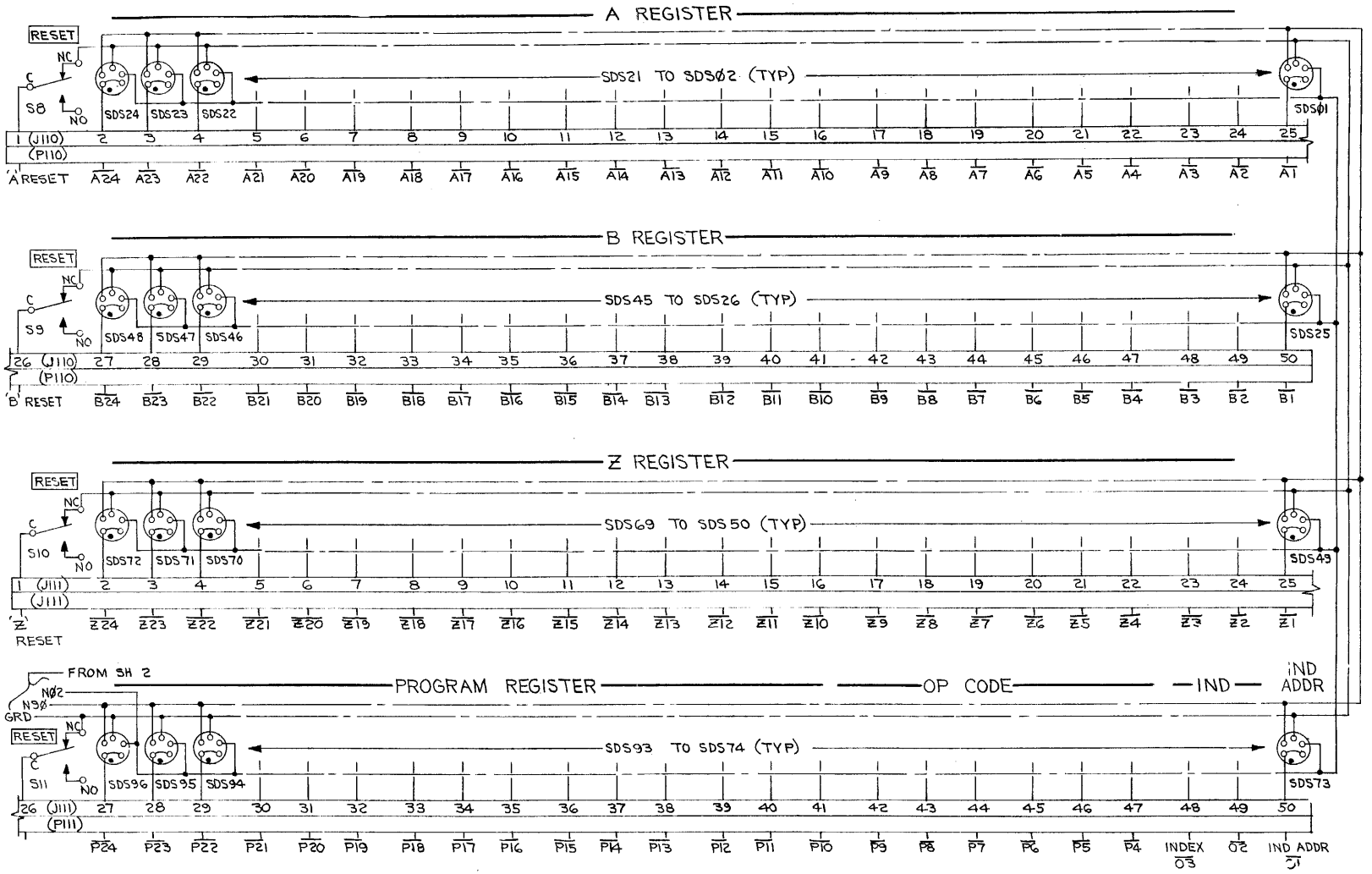


Figure 6-7. Control Panel, Schematic Diagram
Page 3 of 3

APPENDIX

DDP-24 OP CODE GROUPS

OP CODE GROUP	ANOTHER OP CODE GROUP	AND/OR	INDIVIDUAL OP CODE NUMBER OR CONTROL FLIP-FLOP	MNEMONIC
01			60	CRA
			61	SKS
			62	RND
			63	TAX
02			34	MPY
			35	DIV
			36*	BCD
			37*	BIN
03			20	ADM
			21	SBM
			22	OTM
			23	LDB
			24	LDA
			25	JRT
			26	SPARE
			27	JST
04			10	ADD
			11	SUB
			12	SKG
			13	SKN
			14	SPARE
			15	ANA
			16	ORA
			17	ERA
05			31	FMB
			32	DMB
			C2	
07			50	OTA
			51	ITC
			52	INA
			53	OCP
			54	ADX
			55	TAB
			56	LDX
			57	IAB
08			70	JPL
			71	JZE
			72	JIX
			73	JOF
			74	JMP
			75	JXI
			76	SPARE
			77	NOP
09			15	ANA
			16	ORA
10			41	ALS
			46	NRM

*BIN/BCD Code Groups

OP CODE GROUP	ANOTHER OP CODE GROUP	AND/OR	INDIVIDUAL OP CODE NUMBER OR CONTROL FLIP-FLOP	MNEMONIC
11			27	JST
			31	FMB
			66	STX
	12		00	HLT
			01	SPARE
			02	XEC
			03	STB
			04	STC
			05	STA
			06	STD
			07	INM
12			00	HLT
			01	SPARE
			02	XEC
			03	STB
			04	STC
			05	STA
			06	STD
			07	INM
13			30	SMP
			31	FMB
			32	DMB
			33	SPARE
			34	MPY
			35	DIV
			36*	BCD
			37*	BIN
14			20	ADM
			21	SBM
			22	OTM
			23	LDB
			24	LDA
			25	JRT
			26	SPARE
			27	JST
15			40	ARS
			41	ALS
			42	LRR
			43	LLR
			44	LRS
			45	LLS
			46	NRM
			47	LGL
16			70	JPL
			71	JZE
			72	JIX
			73	JOF
			74	JMP
			75	JXI
			76	SPARE
			77	NOP

*BIN/BCD Code Groups

OP CODE GROUP	ANOTHER OP CODE GROUP	AND/OR	INDIVIDUAL OP CODE NUMBER OR CONTROL FLIP-FLOP	MNEMONIC
17			54	ADX
			62	RND
			64	SCR
			65	SCL
	15		40	ARS
			41	ALS
			42	LRR
			43	LLR
			44	LRS
			45	LLS
			46	NRM
			47	LGL
	16		70	JPL
			71	JZE
			72	JIX
			73	JOF
			74	JMP
			75	JXI
			76	SPARE
			77	NOP
18			40	ARS
			42	LRR
			44	LRS
			64	SCR
19			23	LDB
			37*	BIN
20			10	ADD
			11	SUB
			16	ORA
			17	ERA
			20	ADM
			21	SBM
			30	SMP
21			34	MPY
			60	CRA
			37*	BIN
22			23	LDB
			55	TAB
	58		36*	BCD
			37*	BIN
23	30		10	ADD
			20	ADM
	31		11	SUB
			21	SBM
24			07	INM
			31	FMB

* BIN/BCD Code Groups

OP CODE GROUP	ANOTHER OP CODE GROUP	AND/OR	INDIVIDUAL OP CODE NUMBER OR CONTROL FLIP-FLOP	MNEMONIC
25			43	LLR
			45	LLS
			46	NRM
			65	SCL
26			54	ADX
			75	JXI
27			46	NRM
			65	SCL
28			64	SCR
			65	SCL
	15		40	ARS
			41	ALS
			42	LRR
			43	LLR
			44	LRS
			45	LLS
			46	NRM
			47	LGL
29			42	LRR
			44	LRS
			64	SCR
30			10	ADD
			20	ADM
31			11	SUB
			21	SBM
32			10	ADD
			11	SUB
33			25	JRT
			27	JST
			67	IRX
	20		10	ADD
			11	SUB
			16	ORA
			17	ERA
			20	ADM
			21	SBM
			30	SMP
34			46	NRM
			56	LDX
			64	SCR
			65	SCL
			63	TAX

OP CODE GROUP	ANOTHER OP CODE GROUP	AND/OR	INDIVIDUAL OP CODE NUMBER OR CONTROL FLIP-FLOP	MNEMONIC
35			07	INM
			22	OTM
			32	DMB
			50	OTA
			52	INA
			C2	
36			35	DIV
37			$\overline{36}$*	$\overline{\text{BCD}}$
			$\overline{37}$*	$\overline{\text{BIN}}$
			$\overline{32}$	$\overline{\text{DMB}}$
	64		67	IRX
	04		10	ADD
			11	SUB
			12	SKG
			13	SKN
			$\overline{14}$	$\overline{\text{SPARE}}$
			15	ANA
			16	ORA
			17	ERA
	13		30	SMP
			$\overline{31}$	$\overline{\text{FMB}}$
			32	DMB
			$\overline{33}$	$\overline{\text{SPARE}}$
			34	MPY
			35	DIV
			36*	BCD
			37*	BIN
	14		20	ADM
			21	SBM
			22	OTM
			23	LDB
			24	LDA
			25	JRT
			$\overline{26}$	$\overline{\text{SPARE}}$
			$\overline{27}$	$\overline{\text{JST}}$
38	Missing		12	SKG
			13	SKN
39	36		35	DIV
	50		$\overline{16}$	$\overline{\text{ORA}}$
			$\overline{17}$	$\overline{\text{ERA}}$
	20		10	ADD
			11	SUB
			16	ORA
			17	ERA
			20	ADM
			21	SBM
			30	SMP
40			45	LLS
			65	SCL

* BIN/BCD Code Groups

OP CODE GROUP	ANOTHER OP CODE GROUP	AND/OR	INDIVIDUAL OP CODE NUMBER OR CONTROL FLIP-FLOP	MNEMONIC
41			04	STC
			05	STA
			06	STD
42			41	ALS
			43	LLR
			45	LLS
			46	NRM
			47	LGL
			65	SCL
			$\overline{C2}$	
43			03	STB
			57	IAB
44			16	ORA
			17	ERA
45			C4-50	
			C4-52	
	01		60	CRA
			61	SKS
			62	RND
			63	TAX
	07		$\overline{50}$	$\overline{OTA}$
			51	ITC
			$\overline{52}$	$\overline{INA}$
			53	OCP
			54	ADX
			55	TAB
			56	LDX
			$\overline{57}$	$\overline{IAB}$
	08		70	JPL
			71	JZE
			72	JIX
			73	JOF
			74	JMP
			$\overline{75}$	$\overline{JXI}$
			$\overline{76}$	$\overline{SPARE}$
			77	NOP
46			15	ANA
			16	ORA
			24	LDA
47			35	DIV
			40	ARS
			41	ALS
			42	LRR
			43	LLR
			44	LRS
			45	LLS
			$\overline{46}$	$\overline{NRM}$
			47	LGL
			64	SCR
			65	SCL

OP CODE GROUP	ANOTHER OP CODE GROUP	AND/OR	INDIVIDUAL OP CODE NUMBER OR CONTROL FLIP-FLOP	MNEMONIC
48			56	LDX
			66	STX
			67	IRX
			72	JIX
49			40	ARS
	67		34	MPY
			36*	BCD
			44	LRS
			64	SCR
			37*	BIN
50			16	ORA
			17	ERA
	20		10	ADD
			11	SUB
			16	ORA
			17	ERA
			20	ADM
			21	SBM
			30	SMP
51			34	MPY
			36*	BCD
			37*	BIN
52			30	SMP
			57	IAB
			66	STX
	03		20	ADM
			21	SBM
			22	OTM
			23	LDB
			24	LDA
			25	JRT
			26	SPARE
			27	JST
	04		10	ADD
			11	SUB
			12	SKG
			13	SKN
			14	SPARE
			15	ANA
			16	CRA
			17	ERA
	12		00	HLT
			01	SPARE
			02	XEC
			03	STB
			04	STC
			05	STA
			06	STD
			07	INM

OPG59··XZD

*BIN/BCD Code Groups

OP CODE GROUP	ANOTHER OP CODE GROUP	AND/OR	INDIVIDUAL OP CODE NUMBER OR CONTROL FLIP-FLOP	MNEMONIC
53			31	FMB
	35		07	INM
			22	OTM
			32	DMB
			50	OTA
			52	INA
			C2	
55			22	OTM
			57	IAB
56			36*	BCD
			57	IAB
57	02		34	MPY
			35	DIV
			36*	BCD
			37*	BIN
			C2	
58	BIN-BCD OPTION		36*	BCD
			37*	BIN
59			31	FMB
			32	DMB
60			52	INA
			C2	
61			50	OTA
			55	TAB
			57	IAB
62			43	LLR
			47	LGL
			C2	
63			25	JRT
			27	JST
64			67	IRX
	04		10	ADD
			11	SUB
			12	SKG
			13	SKN
			14	SPARE
			15	ANA
			16	ORA
			17	ERA
	13		30	SMP
			31	FMB
			32	DMB
			33	SPARE
			34	MPY
			35	DIV
			36*	BCD
			37*	BIN

*BIN/BCD Code Groups

OP CODE GROUP	ANOTHER OP CODE GROUP	AND/OR	INDIVIDUAL OP CODE NUMBER OR CONTROL FLIP-FLOP	MNEMONIC
64 cont.	14		20	ADM
			21	SBM
			22	OTM
			23	LDB
			24	LDA
			25	JRT
			26	SPARE
			27	JST
65			45	LLS
	27		46	NRM
			65	SCL
66			45	LLS
	27		46	NRM
			65	SCL
	36		35	DIV
67			34	MPY
			36*	BCD
			44	LRS
			64	SCR
			37*	BIN
68*	11	Memory Expansion Option	27	JST
			31	FMB
			66	STX
	12		00	HLT
			01	SPARE
			02	XEC
			03	STB
			04	STC
			05	STA
			06	STD
			07	INM
	64		67	IRX
	04		10	ADD
			11	SUB
			12	SKG
			13	SKN
			14	SPARE
			15	ANA
			16	ORA
			17	ERA
	13		30	SMP
			31	FMB
			32	DMB
			33	SPARE
			34	MPY
			35	DIV
			36*	BCD
			37*	BIN

* BIN/BCD Code Groups

OP CODE GROUP	ANOTHER OP CODE GROUP	AND/OR	INDIVIDUAL OP CODE NUMBER OR CONTROL FLIP-FLOP	MNEMONIC
68* cont.	14		20	ADM
			21	SBM
			22	OTM
			23	LDB
			24	LDA
			25	JRT
			26	SPARE
			27	JST
69*			JME	
	68	Memory Expansion	27	JST
			31	FMB
	11	Option	66	STX
	12		00	HLT
			01	SPARE
			02	XEC
			03	STB
			04	STC
			05	STA
			06	STD
			07	INM