COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

APRIL 1977

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THE
MAGAZINE
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COMPUTER DESIGN

APRIL 1977 • VOLUME 16 • NUMBER 4

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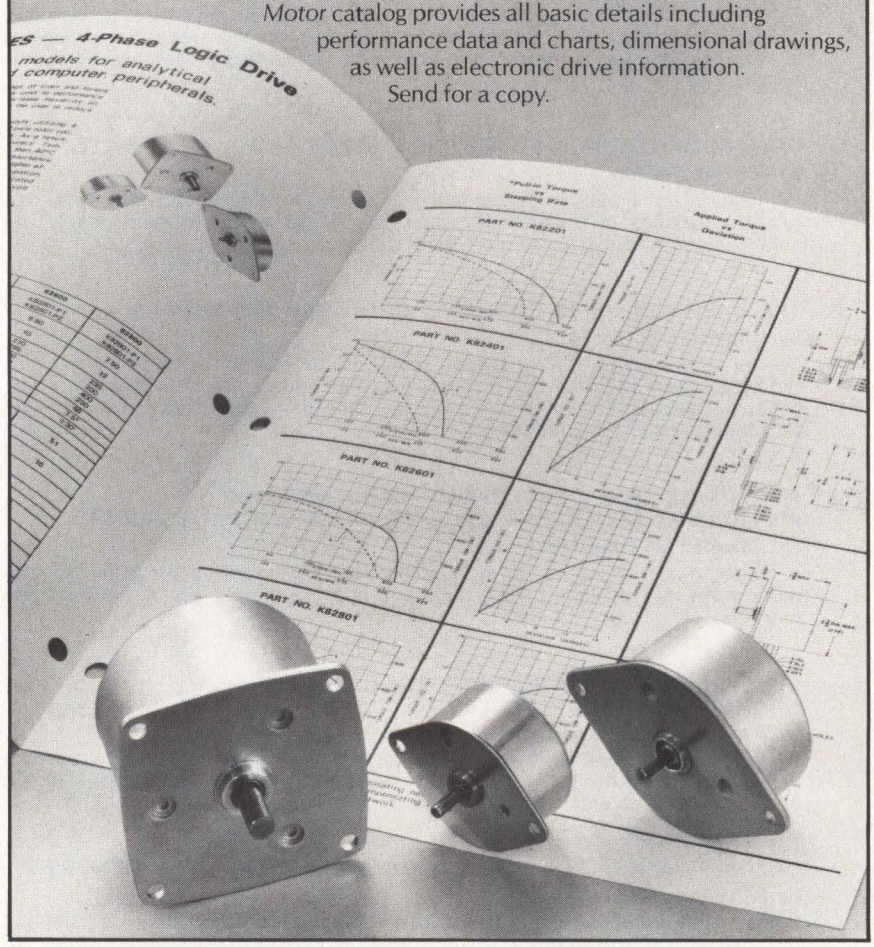

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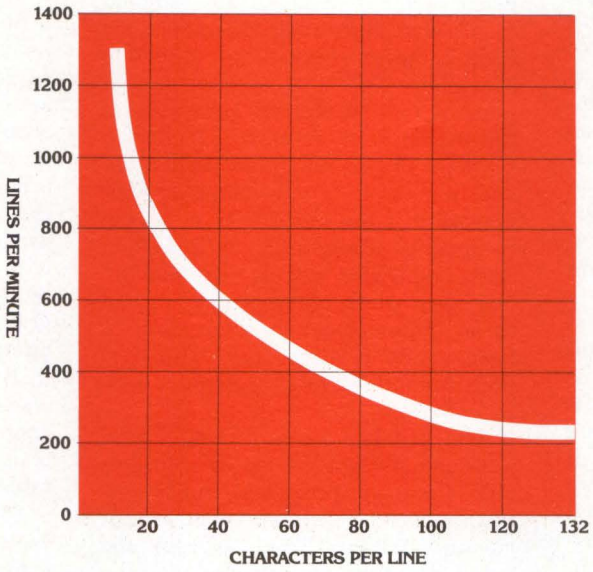
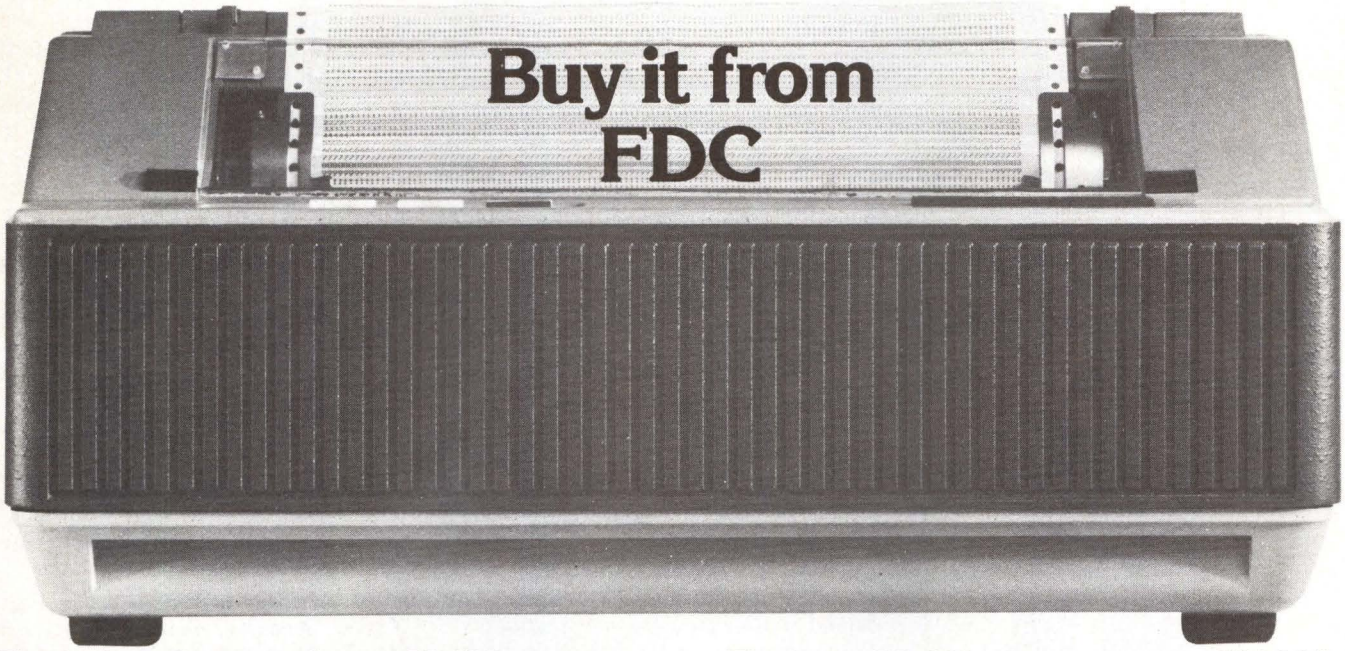
Line printer speed at serial printer prices





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LETTERS TO THE EDITOR

To the Editor:

In the Dec 1976 issue of *Computer Design,* "Letters to the Editor," pp 10-14, Mr A. J. M. Collins appears to question the statement that "No security (system) is inviolable." During World War II the German General Staff could never be convinced that their codes would someday be broken. The Allies broke the German code and took extraordinary measures to ensure that the German General Staff would continue to believe that it had never been broken.

Let us assume for the moment that a security system is used to transmit a letter. This system will format the letter for transmission such that the heading, address, greeting, etc are positioned somewhere in the body of the letter and restored to the proper format when the letter is printed at destination. Assume also that several codes are used for each consonant and numbers 0 through 9, and still a greater number of codes are reserved for vowels, space, null, and other frequently used characters. A 2-page letter would be difficult to "decode," but not impossible if sufficient repetition occurs. An unauthorized person, familiar with "decoding" procedures, can with the use of a computer break almost any coded message. (The words "decode" and "decoding" are synonymous with code breaking.)

"Decoding" is impossible if a sufficient number of codes are assigned to all characters such that the same code is never selected for repeating characters. This is true for a limited number of messages; however, as the number of messages increases, portions of the table are exhausted and repetition is unavoidable. Vulnerability ("decoding") of a system is directly proportional to repetition since repetition yields information. Nonlinear shift registers are viewed as an improvement in comparison to linear shift registers but offer less protection than small computer systems.

The problem of protecting coded information from attacks is considerable. Complete protection from crosstalk between telephone lines is not always realized. There is also the possibility that an intruder may be able to tap a line by means of capacitive or inductive coupling. Wire tapping, of course, needs no further discussion. Preparation of messages in clear codes (such as data on paper tape) could very well be a weak link in the system since it is possible to detect transients generated by characters that are being punched. Each character generates a slightly different transient (characters may be identified with an oscillograph record; however, a small computer can be programmed so as to readily identify characters if transients are digitized) that is reflected in the power line and can be detected by monitoring the power line with a wideband frequency selective voltmeter. Some protection can be realized with the use of saturable voltage regulators and complete protection has been obtained with the use of regulators that convert ac to dc and again back to ac. Isolation transformers, depending on the design, provide acceptable results.

In the writer's opinion the concept of absolute randomness is one that begs for a more precise definition, yet is frequently used to draw attention to the salient features of a security system. Some statisticians have expressed the opinion that the concept of absolute randomness cannot be defined with words but can only be exemplified by producing a table that is absolutely random and such a table would have to meet the following conditions. It must consist of the set of all integers; the set, after being arranged in a random sequence, cannot be formulated; the cross correlation between any two large subsets will produce identical results (or relatively small variations); and if the set is treated as a function of time, the results of a power spectrum would be identical to white noise.

Such a table cannot be produced because of the obvious limitation of an infinite set, but it is useful only as a concept that attempts to define absolute randomness by associating it with a table. Binary sequences originating from selected terms of the binomial formula have been used to produce pseudorandom tables with good results. Errors produced by the power spectral density program such as truncation, roundoff, filtering, and interpolation were found to be minimal. A loss in randomness was observed when numbers (binary) containing runs of three or more 0s and 1s were eliminated from the table.

The primary reason that accounts for the limited number of attacks on communication systems is believed to be the lack of technical competence of an attacker. There is also the problem of securing complex and expensive equipment that will, as a minimum requirement, detect and record serial data. Access to telephone lines where concealment is possible is difficult to find. The attack could come from an organization with the necessary resources and would have a high probability of success. One security failure is sufficient to destroy the confidence of users. For those who have the responsibility of maintaining security of communication systems, the advice given by the U.S. Navy to submarine crewmen is certainly worthwhile: "*Don't make the same mistake once!*"

Interested readers who would like additional information should consult the following references.

R. Krishnaiyer and J. C. Donovan, "Cyclic Sequence Generator Increases Security of Alarm Systems," *Computer Design,* July 1975, pp 73-77

R. Krishnaiyer and J. C. Donovan, "Shift Register Generation of Pseudorandom Binary Sequences," *Computer Design,* Apr 1973, pp 69-74

S. W. Golomb, *Shift Register Sequences,* Holden-Day, Inc, 1967

Carl H. Meyer, "Enciphering Data for Secure Transmission," *Computer Design,* Apr 1974, pp 129-134

F. Sellers, Jr, Mu-Yue Hsiao, and L. W. Bearnson, *Error Detecting Logic For Digital Computers,* McGraw-Hill Book Co, 1968

Roland M. Vayer
Consultant
Vergennes, Vt

NEW TECH EDITOR AT COMPUTER DESIGN—George V. Kotelly has joined the staff of *Computer Design* magazine as Technical Editor after a number of years of industrial technical communications experience. Most recently a senior technical writer at Analogic Corp, he previously held similar positions at USM Corp, Raytheon Co, and Honeywell. Prior to that he was a senior publications engineer at RCA. He holds a BSEE degree from Tufts University.

(*Continued on p* 10)

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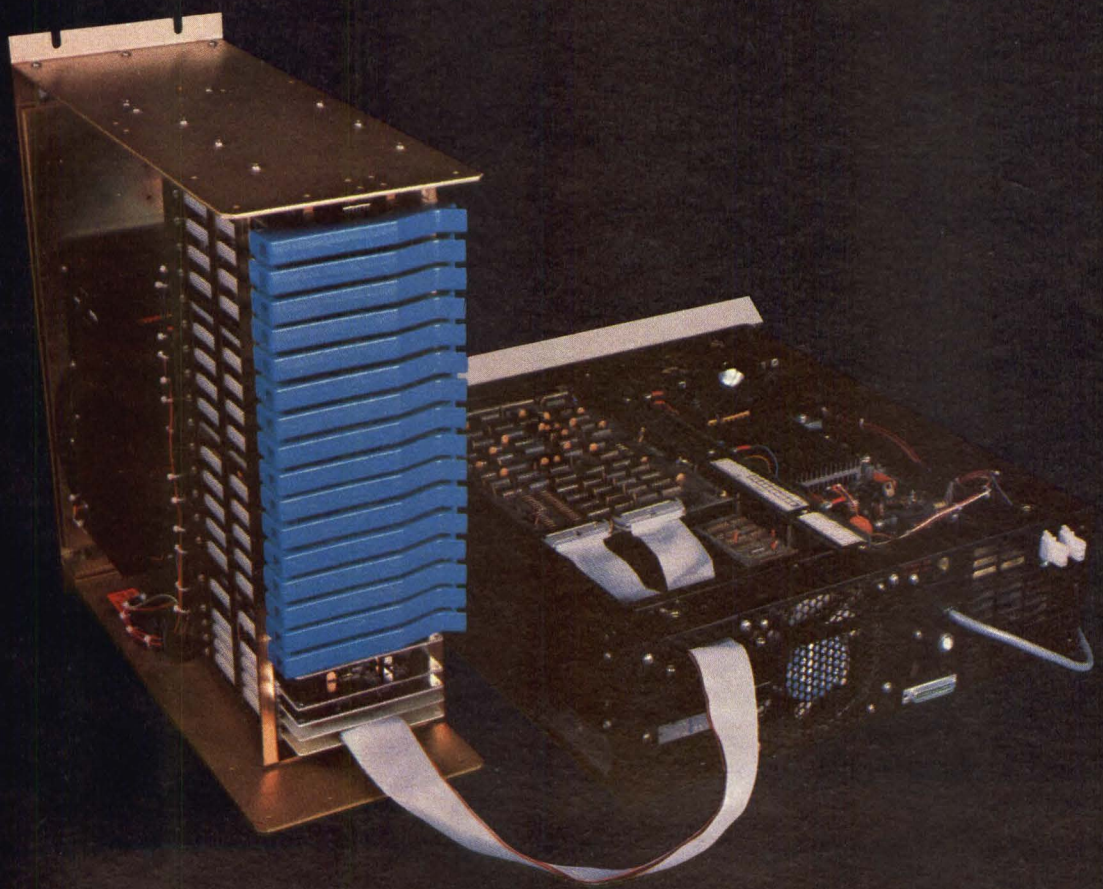

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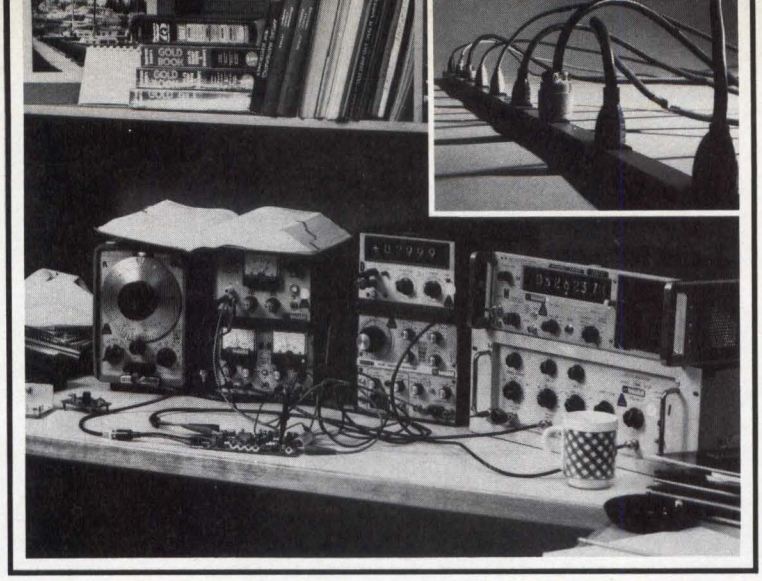

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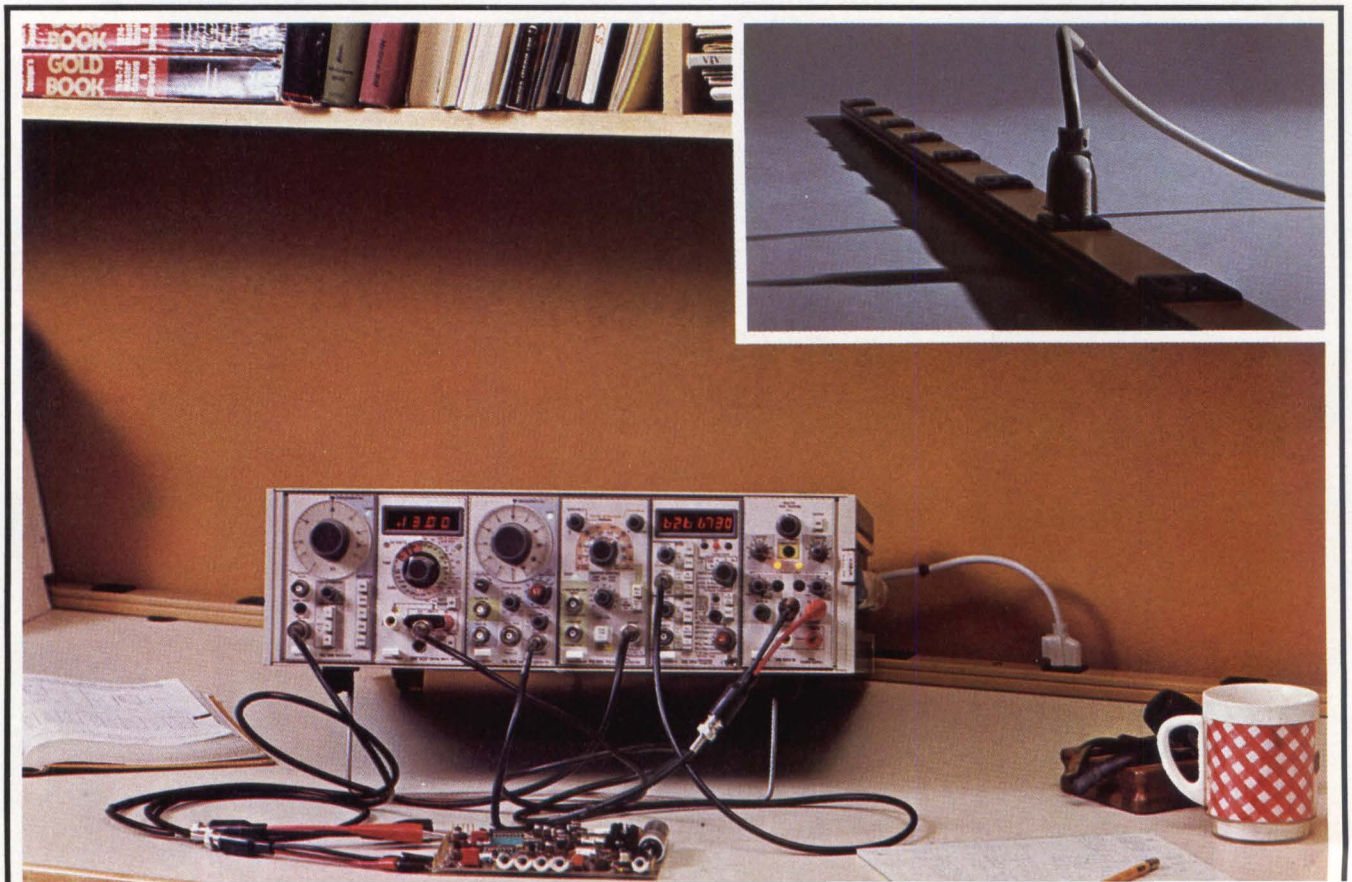

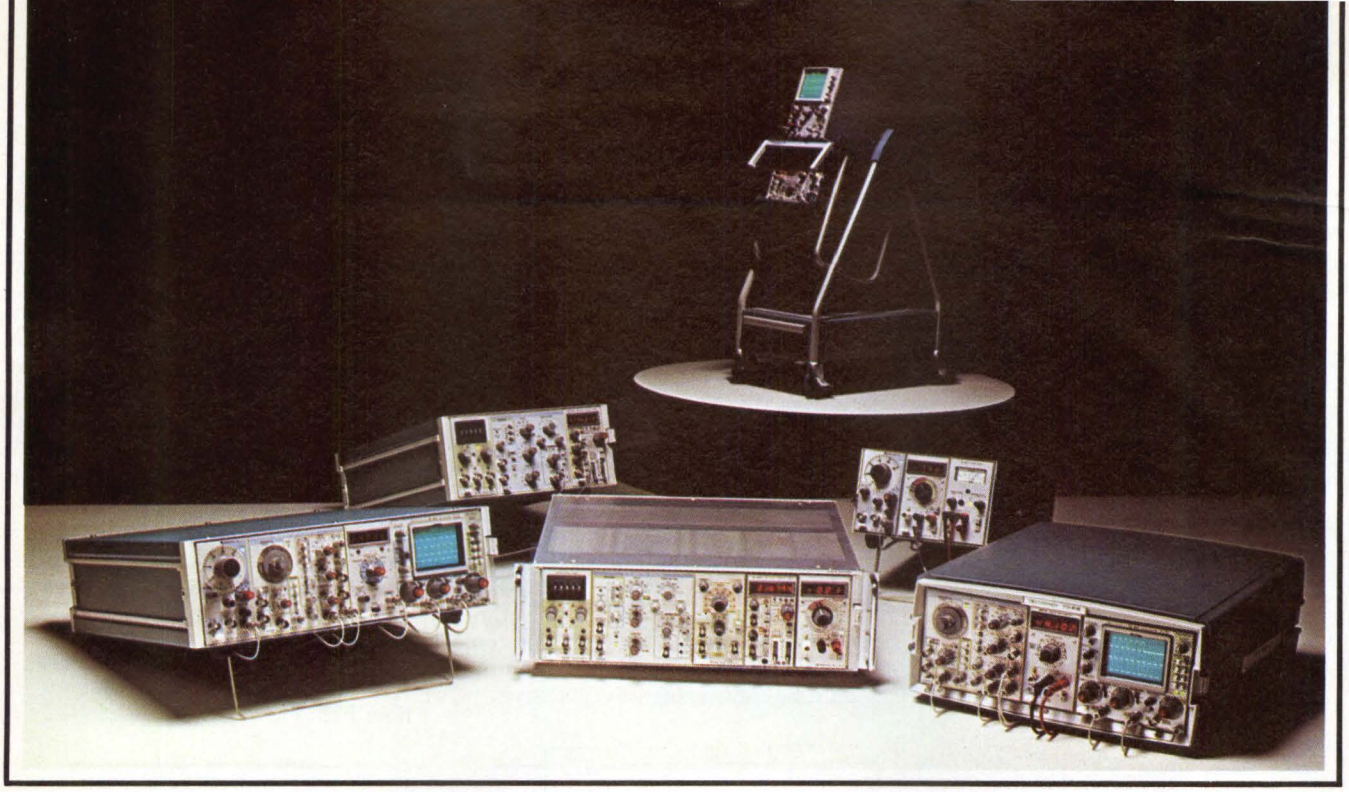

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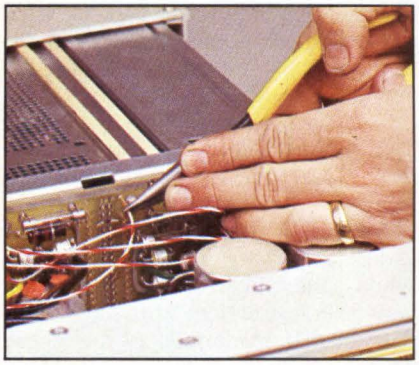

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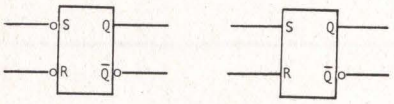
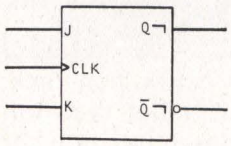
To the Editor:

I have just read the article "Documentation Standards Clarify Design," by J. F. Wakerly in the Feb 1977 issue of *Computer Design*, pp 75-85. Although the author recommends use of the "distinctive shapes" symbols of ANSI Y32.14-1973, certain of his illustrations do not reflect fully the requirements or capabilities of that standard.

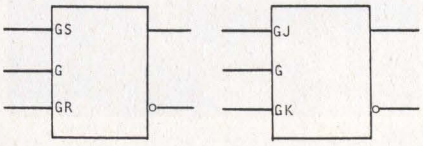
In particular, the symbology used for flip-flops in this article ignores the *essential* requirement of the ANSI standard that the outputs of the flip-flops are to be shown with the logic state or physical signal level that occurs when the flip-flop is set. Therefore when the author uses the negation indicator option, the flip-flops of Fig 5, for example, should be shown this way



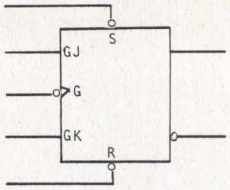
Again, in Fig 14, the author invents a doubled dynamic indicator symbol to designate that the flip-flop outputs change their state only after the clock signal disappears. The standard provides an output delay indicator symbol for this purpose. Thus the flip-flop in Fig 14 should appear as



In all of the above, I have ignored the internal labels on the input and output lines. In particular, the labels Q, $\overline{Q}$, CLK, PR, and CLR are not permitted in the standard. This is not a deficiency of the standard as it does provide a simple and unambiguous method of accurately reflecting the operations intended. For example, the "CLK" input to an S-R or J-K flip-flop is labeled G, and to show that the inputs are effective on the flip-flop only when the clock signal occurs, the symbols used are



Or, as in Fig 15, when some inputs are effective asynchronously, it would be shown as



The standard also addresses the question of symbology for more complex MSI or LSI symbols discussed briefly by the author. While the standard probably cannot represent many such devices in a simple single symbol, it does give examples covering the multiplexer of Fig 18(a).

My purpose here is simply to correct the impression conveyed by the article that the symbols adhere to the ANSI standard.

M. P. Chinitz
Sperry Univac Computer Systems
Blue Bell, Pa

To The Editor:

In the December 1976 issue of *Computer Design*, pp 112-114, the article titled "Microcomputer Interfacing: The Vectored Interrupt," by Jonathan A. Titus, Peter R. Rony, and David G. Larsen, briefly mentions that inputs to the 74148 priority encoder chip should be latched. The authors do not mention why or when to latch the interrupt inputs. The why is simple: the interrupt should be latched because an interrupt pulse may be missed by a busy processor. The interrupt latch should only be reset when the particular interrupt is answered by the processor.

Inputs to the 74148 priority encoder chip should be held stable while the interrupt acknowledge jams the instruction onto the 8080A data bus. If the inputs to the 74148 priority encoder chip are not held stable when the 8212 is being loaded, then the contents loaded into the 8212 are not predictable since the outputs of the 74148 may change.

Unpredictable contents loaded into the 8212 result in a bogus interrupt being recognized by the software. The results of software processing a bogus interrupt might be unpredictable.

William J. Gleeson
Honeywell Information Systems
Phoenix, Ariz

Letters to the Editor should be addressed:

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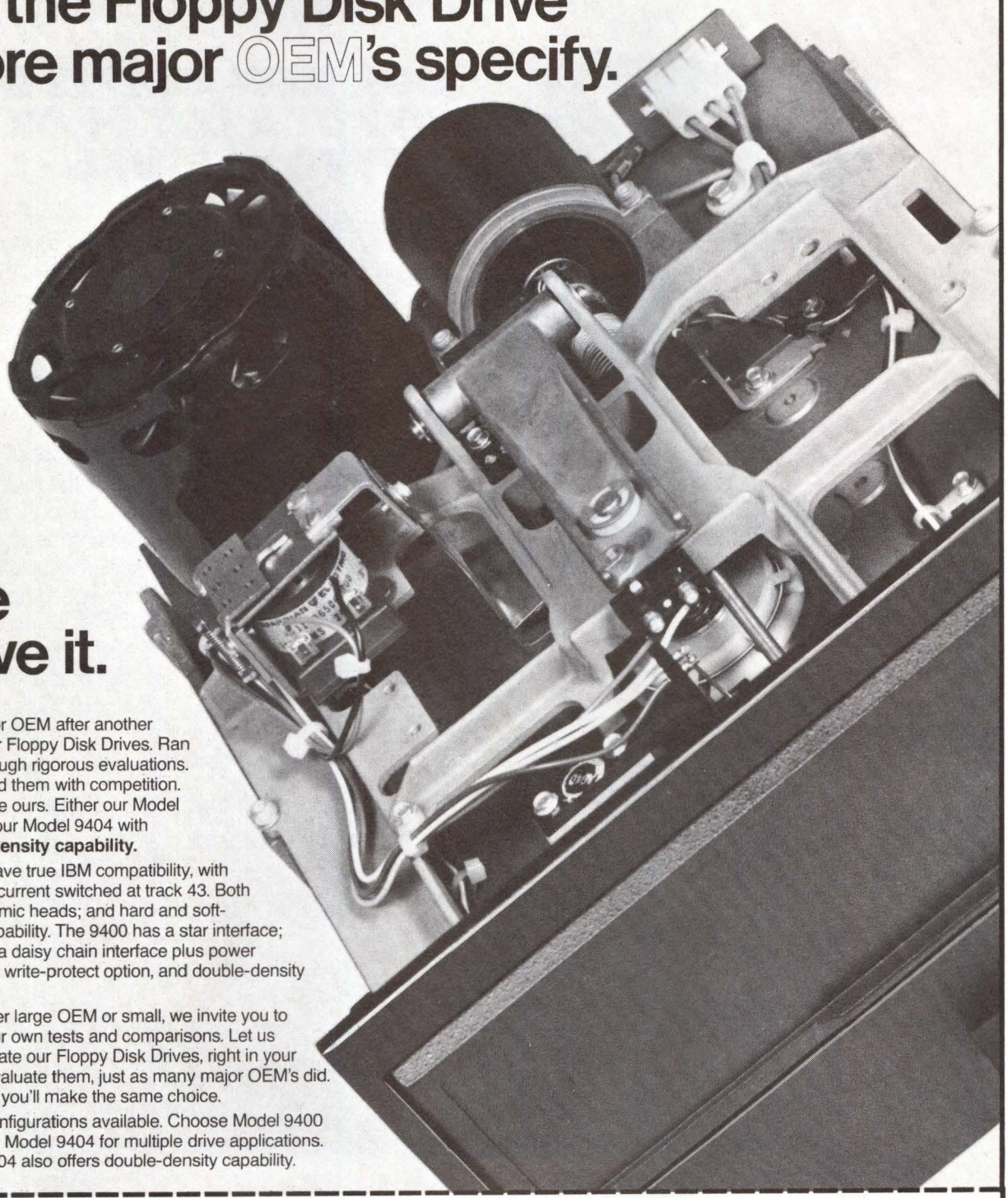

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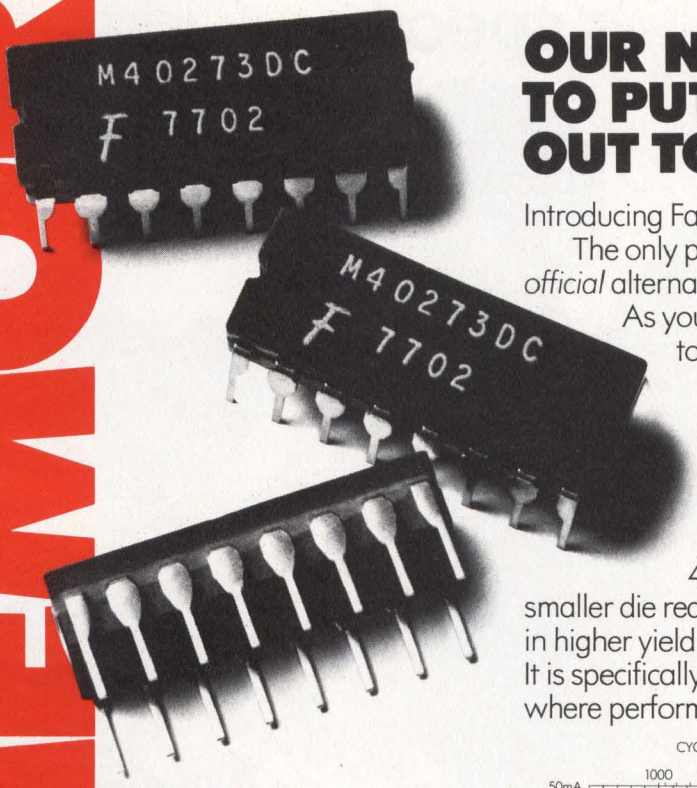
MOS MEMORY



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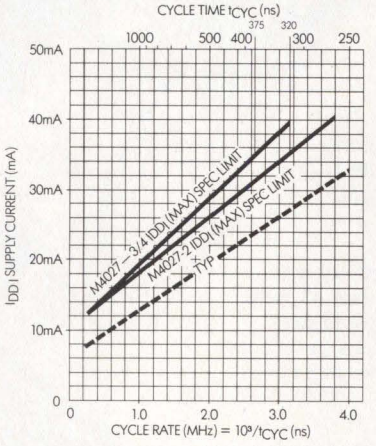

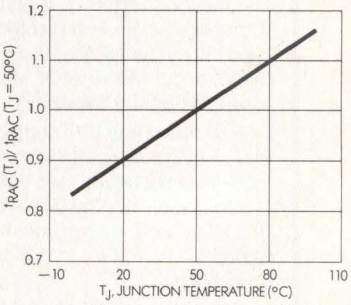

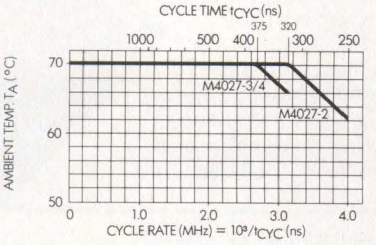

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Column-To-Row-Strobe Lead Time Range	−50 to +50 ns	$\overline{CAS}$ can stay LOW to end of cycle.		
Clock High Voltage Minimum	2.7 V	2.4 V	2.4 V	2.4 V
Input High Voltage Minimum (Except Clock)	2.4 V	2.2 V	2.2 V	2.2 V
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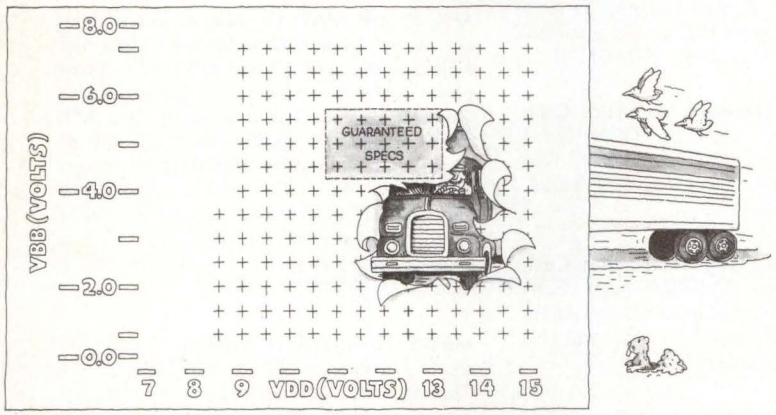

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CALENDAR

CONFERENCES

APR 26-27—The 25th Annual Nat'l Relay Conf, Oklahoma State U, Stillwater, Okla. INFORMATION: Dr D. D. Lingelbach, School of Electrical Engineering, 202 Engineering S, Oklahoma State U, Stillwater, OK 74074

APR 26 and 28—Invitational Computer Conf, Hempstead, NY and Philadelphia, Pa. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 204, Newport Beach, CA 92660. Tel: (714) 644-6037

APR 26-28, MAY 3-5, MAY 10-12, and MAY 24-26—Computer Caravan, Minneapolis/St Paul, Minn; Chicago, Ill; New York, NY; and Philadelphia, Pa. INFORMATION: John C. Forbes & Associates, One Hilltop Rd, Winchester, MA 01890. Tel: (617) 729-9244

MAY 2-5—ISA/77 Conf and Exhibit, Anaheim, Calif. INFORMATION: ISA/77, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

MAY 3-5—ECOMA-3 (European Computer Measurement Assoc), Hamburg, Germany. INFORMATION: Scott N. Yasler, ECOMA President, c/o Union Bank of Switzerland, Bahnhofstrasse 45, CH-8021 Zurich, Switzerland

MAY 3-6—EUROCON '77, Venice, Italy. INFORMATION: EUROCON '77, c/o AEI, Viale Monza 259, 1-20126 Milan, Italy

MAY 7-8 and JUNE 18-19—Personal Computing Show, Philadelphia, Pa and Boston, Mass. INFORMATION: Personal Computing, Conf and Exposition Mgmt Co, Box 844, Greenwich, CT 06830

MAY 10-14—Minicomputer, Peripheral, and Data Communications Exhibition, U. S. Trade Center, Milan, Italy. INFORMATION: Mike Springmann, Office of Internat'l Mktg, Rm 1014, U.S. Dept of Commerce, Washington, DC 20230. Tel: (202) 377-4270

MAY 16-18—27th Electronic Components Conf, Arlington, Va. INFORMATION: Eleanor Madden, Public Affairs Dept, Du Pont Co, Wilmington, DE 19898. Tel: (302) 774-2358

MAY 17-19—NEPCON '77 East (Nat'l Electronics Packaging and Production Conf), Philadelphia, Pa. INFORMATION: NEPCON '77 East, Industrial & Scientific Conf Mgmt, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

MAY 18-22—Hobby Electronics Fair, Philadelphia, Pa. INFORMATION: Aaron Kozlov, Project Mgr, ISCM, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

MAY 24-26—Sixth Annual Sym on Incremental Motion Control Systems and Devices, Urbana, Ill. INFORMATION: Dr B. C. Kuo, U of Illinois, Dept of Electrical Engineering, Urbana, IL 61801. Tel: (217) 333-4341

MAY 24-26—Internat'l Exposition of Mini/Microcomputers and Microprocessors, Palais de Exhibitions, Geneva, Switzerland. INFORMATION: Joseph C. Maurer, Industrial & Scientific Conf Mgmt, Inc, 222 W Adams St, Chicago, IL 60606. Tel: (312) 263-4866

MAY 24-27—PICA-77 (Power Industry Computer Application Conf), Toronto, Canada. INFORMATION: IEEE, 345 E 47th St, New York, NY 10017. Tel: (212) 752-6800

MAY 24-27—Seventh Internat'l Sym on Multiple-Valued Logic, Charlotte, NC. INFORMATION: Dr C. M. Allen, Sym Chm, Engineering Analysis and Design Dept, U of North Carolina at Charlotte, Charlotte, NC 28223. Tel: (704) 597-2302

JUNE 2—16th Annual Technical Sym, Nat'l Bureau of Stds, Gaithersburg, Md. INFORMATION: Dr Stuart Katzke, Rm A-265, Technology Bldg, National Bureau of Stds, Washington, DC 20234. Tel: (301) 921-3861

JUNE 6-8—Pattern Recognition and Image Processing, Rensselaer Polytechnic Institute, Troy, NY. INFORMATION: Gen'l Chm, Prof H. Freeman, Dept of Electrical and Systems Engineering, Rensselaer Polytechnic Institute, Troy, NY 12181. Tel: (518) 270-6311

JUNE 6-9—15th Internat'l Magnetics Conf, Los Angeles, Calif. INFORMATION: Gen'l Chm, Geoffrey Bate, GPD Laboratory, IBM Corp, PO Box 1900, Boulder, CO 80302. Tel: (303) 447-5634

JUNE 20-22—14th Design Automation Conf, New Orleans, La. INFORMATION: Gen'l Chm, Judith G. Brinsfield, Bell Laboratories, Rm 3B-323, Whippany Rd, Whippany, NJ 07981. Tel: (201) 386-3169

JUNE 20-22—IFAC/IFIP Real-Time Programming Workshop, Eindhoven, The Netherlands. INFORMATION: C. H. Smedema, Philips Research Laboratories, Eindhoven, The Netherlands

JUNE 22-24—Joint Automatic Control Conf, San Francisco, Calif. INFORMATION: Prof J. Meditch, Dept of Electrical Engineering, U of Washington, Seattle, WA 98195. Tel: (206) 543-2170

AUG 8-12—IFIP Congress 77 (Internat'l Federation for Information Processing), Toronto, Canada. INFORMATION: Robert C. Speiker, U.S. Committee for IFIP Congress 77, Registration and Accommodations, Western Electric Co, 222 Broadway, New York, NY 10038

SEMINARS

MAY 3-5, MAY 10-12, and JUNE 7-9—Designers' Forum: Designing Microprocessor Systems, Chicago, Ill; New York, NY; and Boston, Mass. INFORMATION: Computer Caravan, 797 Washington St, Newton, MA 02160

JUNE 6-8—Computer Science and Engineering Curricula Tutorial and Workshop, Williamsburg, Va. INFORMATION: CSE Workshop, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

JUNE 7-8—Digital Electronics for Automation Workshop, and JUNE 9-11—Microcomputer Interfacing Workshop, Virginia Polytechnic Institute and State U, Blacksburg, Va. INFORMATION: Dr Norris Bell, VPI & SU Continuing Education Ctr, Blacksburg, VA 24061 Tel: (703) 951-6328

SHORT COURSES

APR 25-28 and JUNE 13-16—Applications of the PACE Microprocessor; MAY 2-5 and JUNE 20-23—SC/MP Applications; MAY 9-12—Advanced Programming; and JUNE 6-9—Microprocessor Fundamentals, Santa Clara, Calif. INFORMATION: Local National Semiconductor Sales Offices, or National Semiconductor's Western Microprocessor Training Center, 1333 Lawrence Expwy, Santa Clara, CA 95051. Tel: (408) 247-7924

APR 26 and MAY 17—Microprocessor Project Mgmt: Design, Manufacturing, QA, and Field Service; APR 27 and MAY 18—Microprocessors/Microcomputers: A Comprehensive Technical Introduction and Survey; and APR 28-29 and MAY 19-20—Hands-On Microcomputer Programming Workshop, New York, NY (Apr) and Minneapolis/St Paul, Minn (May). INFORMATION: Enrollment Secretary, Integrated Computer Systems, Inc, 4445 Overland Ave, Culver City, CA 90230. Tel: (213) 559-9265

MAY 9-12—Computer Relaying, U of Missouri-Columbia. INFORMATION: W. J. Thomas, 1020 Engineering, College of Engineering, U of Missouri-Columbia, Columbia, MO 65201. Tel: (314) 882-3266

MAY 22-24—Microcomputer Basics and Programming; Successful Design/Project Management of Micro/Minicomputer Systems, and MAY 25-27—Microcomputer Architecture Interfaces and System Design; Micro/Minicomputer Software Development and Systems Diagnostics, St Charles, Ill. INFORMATION: NEC Registrar, 1211 W 22nd St, Oak Brook, IL 60521. Tel: (312) 325-5700

JUNE 13-17—Machine Vision, Automatic Assembly, and Productivity Technology, MIT, Cambridge, Mass. INFORMATION: Director of the Summer Session, Rm E19-356, Massachusetts Institute of Technology, Cambridge, MA 02139

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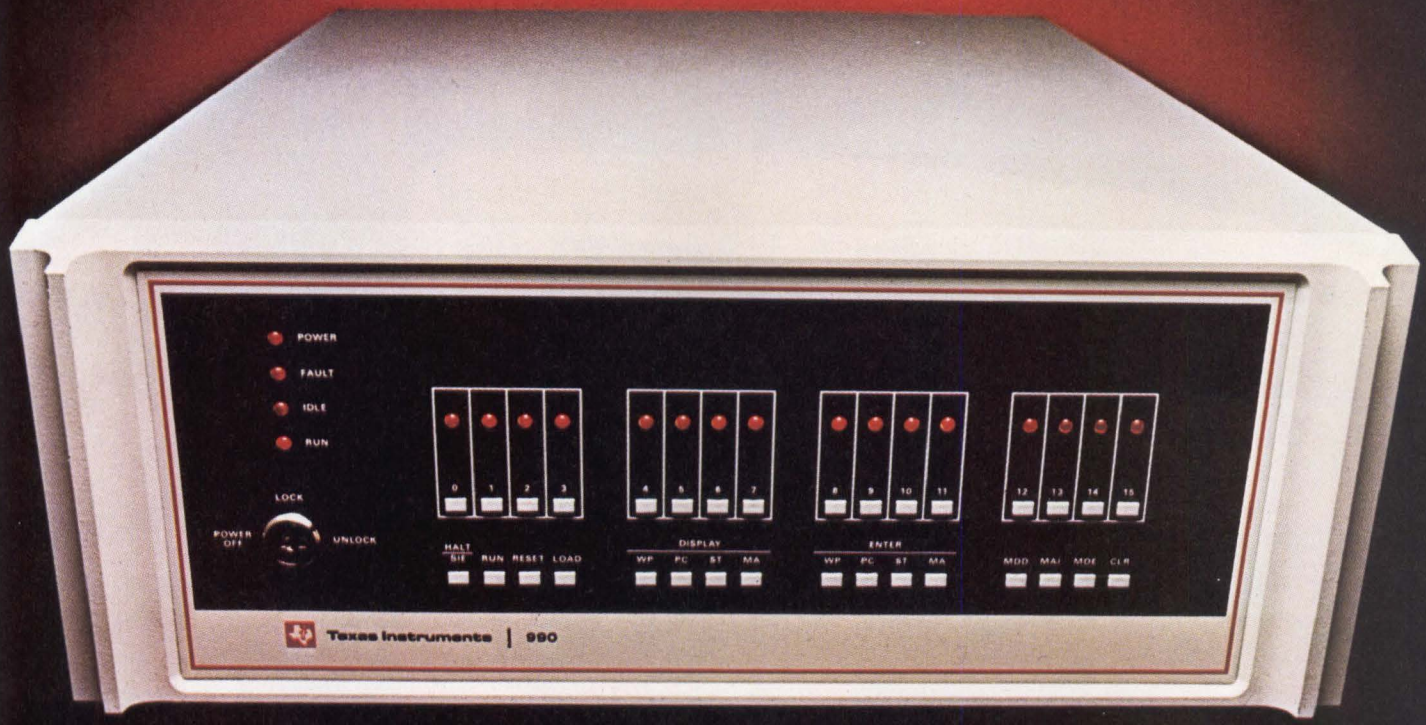

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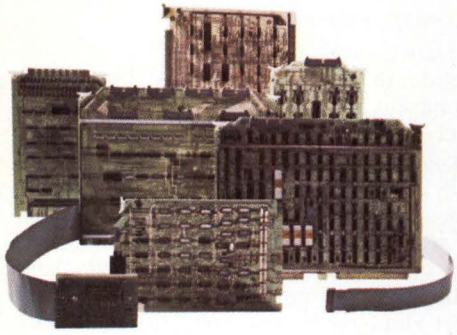

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CIRCLE 14 ON INQUIRY CARD

See Texas Instruments products at Computer Caravan.

by John E. Buckley
Telecommunications Management Corp
Cornwells Heights, Pa.

Computer-Aided Network Design

With the proliferation of remote data terminals and interactive data processing, the need to rapidly design optimum networks has experienced a parallel growth. Since these terminal applications tend to evolve rather than suddenly burst into full existence, the system designer must continually update and expand these networks. The majority of network requirements exhibit an order of magnitude and dynamics that defy manual design practices, making use of computer-aided techniques mandatory to proper configuration *and* management of today's data communications networks. This column addresses this requirement and discusses the parameters of a network design and management aid.

The first objective of such a network design program is to recognize that the computer's role is to reduce and structure the many terminal alternatives; it is not to "decide" on the optimum network configuration. Such a decision typically must reflect many factors that cannot be parameterized in a software program. Economic, operational, and even political considerations must be included in the final structuring of any data communications network. The computer merely presents the tangible parameters in a form such that the desirability or impact of these more subjective factors can be assessed properly.

Such a computer-aided network design program actually comprises a series of program modules that evolve the optimum network in a sequential manner. Each step of the evolution provides an output for evaluation and the ability to input changes or modifications to the progressing network model. These program modules typically consist of a hub assignment, hub configuration, multipoint configuration, and trunk circuit configuration; and they address the primary questions that the network designer must answer.

In order to take advantage of today's long distance leased line tariffs, the longer the continuous circuit mileage and/or the greater the number of circuits between the same points, the lower the cost per circuit unit. With this premise, it is advantageous to concentrate remote terminal lines into common remote hub locations. Long distance leased lines can then be installed from these hubs to the processing center or centers. Particularly with low speed (less than 300-bit/s) terminals or interactive multipoint terminals, the use of multiplexing or concentrating devices at remote hub points will result in major economic advantages.

Such a computer-aided network program must also accept and properly process the variety of data terminals that may be required in the resulting network applications. This variety encompasses the following considerations: terminal access lines, ie, dial, point-to-point leased, and multipoint leased; terminal types; terminal protocols; terminal data codes; and processing centers.

All of these must be accommodated within the network module. If there are two different computer processing centers which use the same type of terminals on multipoint lines for different applications, the computer-aided analysis must recognize that these same type terminals cannot share the same multipoint line from a hub if they are associated with different applications or processing centers.

The network designer must properly and in an isolated manner structure the various terminals' lines that are to use the composite network. Typically, the communications channel between terminals associated with the same hub is considered as a "segment." Segments are linked in such a manner as to form the lowest cost circuit among similar terminals with the same hub. These linked segments are referred to as "chains." Some chains may consist of a single segment that directly connects the terminal to the hub, due to the criterion for shortest distance to the hub; that particular terminal was closer to the hub than any other terminal associated with that hub.

In order to minimize the number of circuits that must be actually multiplexed or concentrated at a hub, these chains are then said to be bridged at the hub to other chains to form "lines." It is the actual lines that interface to the multiplexing or concentrating equipment. The determining factor for bridging these chains at a hub is the maximum number of terminals allowed on a multipoint line and/or the operational aspects, such as the resultant data volumes and response times.

These lines can now be combined into trunks which are the actual long distance leased lines to the processing centers. This combination typically is determined by the data rate capacity of the trunk circuit, ie, 9600 bits/s, and the composite data rate of all lines destined for the same processing center.

This circuit hierarchy is the key to the proper structuring of any composite data network. It is possible

to isolate and adjust any portion of the network development to reflect other more subjective considerations. Primary value of such a design tool is to enable quick, easy determination of the impact of those inevitable "what if" questions posed by fellow designers as well as management. In the past such rhetorical questions were ignored or dismissed with educated opinions based on some alleged years of experience. Too often the correct answers to such questions can significantly guide the network designer toward a truly optimum network.

The program modules are directed toward very specific objectives and are considered a particular part of the optimum data network objectives. The *hub assignment module* is intended initially to configure all possible remote data terminals to the nearest hub or concentrator location. This module would depend on the actual vertical and horizontal coordinates of each terminal and each hub to calculate the shortest airline mileage. In the United States and Canada, every telephone central office has been assigned a unique vertical and horizontal (V&H) coordinate. These coordinates have been assigned on a grid basis, and by using the Pythagorean theorem, the airline mileage between any two points can be accurately determined to one-tenth of a mile. While there are over 33,000 telephone central office designations in the United States and Canada, the V&H file can be obtained from a number of independent sources. This eliminates the need of the network designer's creating his own V&H coordinate table.

This module must also permit the network designer to force a terminal to any designated hub even though it is not necessarily the shortest distance. As discussed above, many operational and political considerations have to be factored into a network design in order to properly achieve the obtained network configuration.

The *hub configuration module* is intended to accept the completed output from the hub assignment module. The actual configuration of terminal lines that must be combined to form an initialized network are first structured within the hub configuration module. It is important to note that if a processing center which has associated remote data terminals is co-located with a particular hub, those terminals cannot be configured into the resulting inter-hub network. They must be eliminated from the hub configuration module output. For example, if a processing center is located in Chicago and there are 30 terminals in the Chicago area which communicate with that processing center, modifications must be made within the hub configuration module.

The first module is intended mainly to geographically associate terminals with minimum distance hubs. The second module is intended to structure those terminals associated with any hub that will be combined through multiplexing or concentrating techniques to common backbone trunks. The hub configuration module's output would now define the number of different type lines and data rates that must be interfaced at each hub to form a common backbone trunk circuit. This output in effect defines the type and configuration of local line interfaces that must be provided in the hub multiplexers or concentrator equipment.

The third module, *multipoint configuration*, is intended to focus on the structuring of local lines. A local line is a dial, point-to-point, or multipoint line that connects one or more terminals to its assigned hub location. It is suggested, in view of the intrastate

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tariff provisions in various states, that a minimum radius be defined for each hub specifying that any terminal located within that radius is always connected directly to the hub. Typically, an intrastate tariff for a communications channel specifies a fixed charge for any line that originates and terminates between any two points in the central office exchange or any contiguous exchange. Depending upon the individual cities involved, the tariff rate for such intra-exchange or intra-contiguous exchanges is in the order of magnitude of 15 to 20 dollars. Once the terminal is beyond the hub exchange or contiguous exchange, actual airline mileage charges apply. It is therefore recommended that for every hub, the network designer specify a radius which encompasses the hub exchange and contiguous exchange. Those lines would go directly from such a terminal to the hub at a low fixed cost per month. These direct connections are combined into a common line presenting a single interface to a multiplexer or concentrator at the hub by having the local phone company install the bridging equipment within the hub. One of the major advantages of having local terminals bridged at the hub is that operational personnel can easily test and associate any terminal for diagnostic and fault isolation activities without direct involvement of the local phone company.

Terminals beyond this radius would be assigned to the hub as a function of minimum distance. Line segments may properly be discussed in this context. The program algorithm cognizant of the maximum number of terminals or data volume per multipoint line would first select the terminal nearest to the hub. The next step in the algorithm is to select the next terminal nearest to the hub and to calculate the distance from that terminal to the previous terminal which has been connected to the hub. If the distance to the previous terminal is shorter than the distance to the hub, the program designates that terminal to be bridged from the previous terminal on the multipoint line. If the distance to the hub is shorter, the terminal is left in the file and the next nearest terminal is tested in the same manner.

Once the chain has been completed (the maximum number of terminals or data volume has been reached), the program stores the chain and returns to look for the next nearest in-file terminal to the hub, repeating the process. This process continues until all terminals destined from the same processing center with the same data rate and protocol have been configured into appropriate chains.

When all terminals have been assigned to chains and individual line segments defined, the multipoint configuration module must structure these chains into lines so there are a minimum number of line interfaces that must be connected to the multiplexing or concentration equipment to the hub. Again the primary criterion is the maximum number of terminals or data volume associated with a multipoint line. The program selects the chain with the largest number of terminals and attempts to combine it with the one with the lowest number of terminals to configure a single multipoint line which again requires bridging at the hub. When all the chains have been assigned to lines, the program has completed its multipoint configuration test for that hub.

At this point, it would be advantageous to have the individual inter- or intrastate tariffs stored within the computer system; the program could then calculate the cost of each line segment in each chain and easily present a total cost for the entire multipoint line. It must be remembered that in a large data communications network which utilizes the hub principal, the majority of line costs are incurred by local lines rather than between backbone trunk circuits which interconnect the hubs.

A provision must be available within this module to permit the network designer to redesign any of the multipoint line configurations. After examining the equipment, designers can decide whether to have a particular number of terminals interconnected on the same multipoint line. For example, if five terminals at a single location were assigned to the same multipoint line, the resulting network would present a value sensitivity for that location. A common value for that particular multipoint line would render all five terminals inoperative. It may be decided, therefore, that two or three of the terminals at that location should be forced to a different chain to provide a degree of backup in case of a single line failure. While this may not exhibit the optimum segment mileage distance, the backup operational factor may easily justify the small increase in local line cost by dividing the five terminals among two multipoint chains. The multipoint configuration module must provide this network design interaction.

Fourth module is the *trunk circuit configuration module*. This module would be based on the ability of the network designer to specify the capacity of each individual trunk circuit, which typically is expressed in the number of bits per second that a circuit can transmit. The voice grade trunk circuit, for example, can be expected to transmit up to 9600 bits/s. With this parameter established in the module, each of the local lines completed in the previous module would now be grouped by processing center destination into a common trunk. When the 9600-bit/s limit is reached or all available lines for that processing center have been accommodated, the module would designate the resulting trunk as being complete and would begin establishing the next trunk with the remaining lines.

The resulting output would list the local lines assigned to each trunk circuit. The network designer could then decide whether to combine in a common trunk local lines destined for different processing centers which require multiplexing at some intermediate point. Output of this fourth module would clearly specify the number of trunk circuits required, the available capacity for expansion in each trunk circuit, and the multiplexing or concentrator equipment configuration which would be required to combine local circuits into trunks.

These four different modules each address a specific point of the optimum data network objective, focusing on definite aspects that require human interaction and judgements. Only in this manner can the design and subsequent management of a data communications network be established and maintained. The computer performs those tasks within its domain and the human network designer retains control of the more subjective aspects. The following truism of this interaction is illustrated clearly in computer-aided network design: a computer is fast, logical, and unimaginative; man is slow, illogical, and imaginative. Don't attribute to one the attributes of the other. Too often computers are used in design problems in an attempt to relegate to them the role of finalizing judgements rather than merely delineating the input of the judgements.

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DR-121	1K x 10 2K x 8 2K x 10	900/350 ns 900/350 ns 900/350 ns	11.7" x 11.5" (297 mm x 292 mm)	+5V, −12V	25 Watts	Cambridge Memories' 1K x 9 Unicore
DR-104	4K x 9 8K x 9 16K x 9 32K x 9	750/350 ns 750/350 ns 750/300 ns 800/300 ns	13.5" x 8.3" (343 mm x 211 mm)	+5V, −12V	32 Watts	National Semiconductors' MOSRAM 104

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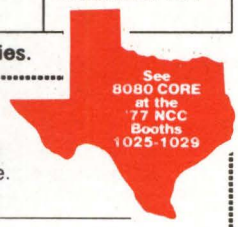

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CIRCLE 16 ON INQUIRY CARD

DP and Communications Users Favor Common Carrier Competition

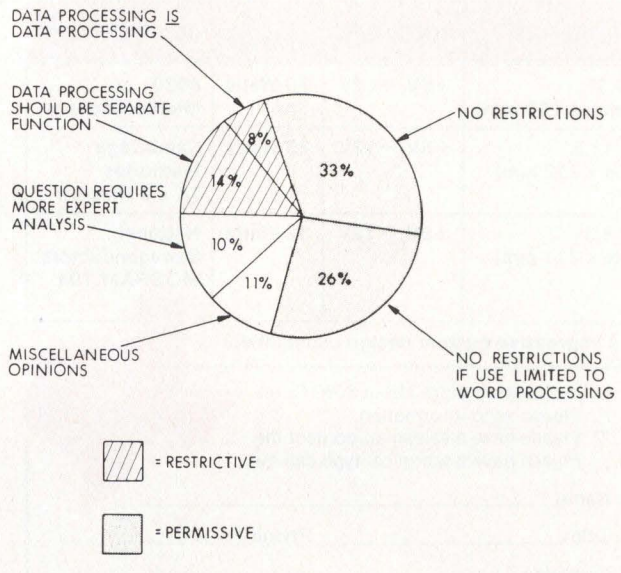
Based on an interpretation of the results received from its survey of the telecommunications industry, a research firm states that U.S. users of data processing and data communications "predominantly" favor permitting common carriers to compete in the data processing field. It found that, in spite of government rulings to the contrary, 59% of all users would allow the regulated communications carriers to provide computer-like processing as part of the communications package.

Of this "permissive" group, as shown in the pie chart, 33% felt there should be no restrictions on offering an integrated package, while 26% said that the user's primary application should not be classified as a data processing system if it is limited to word processing (formatting or editing) and data transmission functions (buffering or line protocol).

About 22% of all types of users, including government agencies, felt that there should be restrictions. Of these, 14% said that data processing is sufficiently unique to be considered a separate function. Therefore, it should not exist as a subsystem of any kind within the common carrier-provided data terminal equipment. The other 8% believed that the data terminal should be classified as a data processing device if it is used for any type of local data processing. Approximately 10% felt that the question was too complex and required further expert analysis to establish applicable definition, standards, and regulatory policy guidelines.

Center for Communications Management, Inc (CCMI), PO Box 324, Ramsey, NJ 07446 states that respondents to this survey represented companies in more than 50 cities in 31 states. Full copies of the report are available at $25 each ($35 for overseas points).

The research firm notes that final survey results essentially preceded the Jan 6 decision to reject its own Common Carrier Bureau ruling of Mar 1976. The Bureau, at that time, denied an AT&T application for marketing a new data service which would use computer technology to directly transmit digitalized data programs between remote terminal equipment.



Summary of results from CCMI survey of telecommunications industry. Research firm interpreted results to show that data processing and communications users favor common carrier competition in the DP field

Following the Bureau's rejection announcement, CCMI last July instituted the survey of industry attitudes toward increasing integration of data processing and data communications, pointing out that both terms were "a matter of definition." CCMI notified the FCC that it planned to present testimony on behalf of the user-industry at Commission hearings now postponed until May 1977.

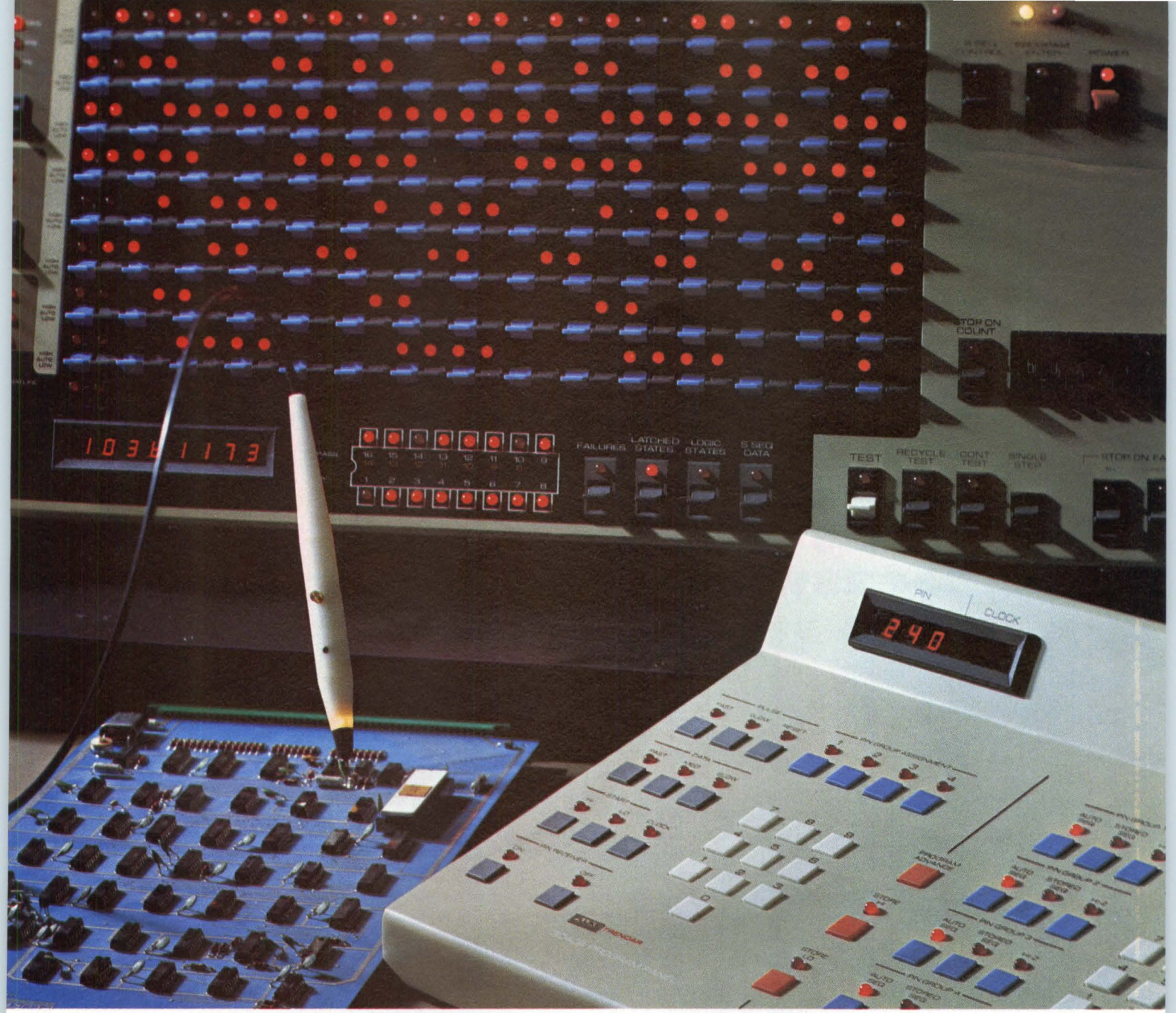
CCMI also noted that it is forwarding complete copies of the survey to key members of U.S. Senate and House committees, since they will shortly be holding hearings on a new Communications Act. Although more than 200 federal legislators introduced bills during the 1976 Congressional session, no formal action was taken. Several new bills have already been introduced in the 1977 Congress, all designed to modernize the original Communications Act of 1934. A limited 3-day hearing in the last session indicated that the new legislation may involve one of the longest and most controversial investigations.

Analysis Identifies Potential Market Tied To Satellite Service

According to an analysis performed by a California organization, FCC approval of the domestic satellite service to be offered by Satellite Business Systems will result in a major market for both existing and new products. SBS partners—IBM, COMSAT-General, and Aetna Casualty and Surety—have committed a minimum of $407 million for plant investment including satellites and earth stations.

ComQuest Corp of 1000 Elwell Court, Palo Alto, CA 94303 has prepared a 259-page analytical report covering proposed digital TDMA/DA techniques, 12/14-GHz equipment, regulatory implications, and implications for the telecommunications and computer industries, as well as for IBM. It also includes market forecasts for various categories of equipment and identifies new product needs.

The report indicates that hundreds, possibly thousands, of "roof-top" stations are planned to provide fully-integrated digital communications services via satellite to major business organizations. SBS projections of service demand indicate an estimated cumulative potential market through 1986 of $2.2 billion for ground sta-



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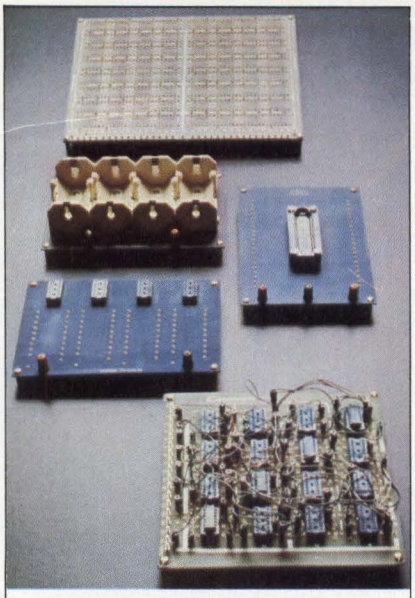

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tions. An estimated $945 million is for digital terminals, $310 million for antennas, and $945 million for equipment. Since most of the required equipment has yet to be developed, there are many opportunities for new products.

Report Issued On GOES Signal Problems

Laboratory tests that indicate how the performance of the geostationary operational environmental satellite (GOES) data collection platform interrogation link could be improved are described in a report issued by the U.S. Department of Commerce Office of Telecommunications. These tests showed that the received signal level was too low for reliable operation of the data buoy radio using its existing antenna. In addition, equipment was subject to severe interference from land mobile transmitters that have primary frequency allocation at 468.825 MHz.

Office researchers demonstrated that improved performance could be achieved through use of a higher gain antenna and with the insertion of a low noise amplifier. They also recommended the use of a 12.5-kHz offset to the interrogation frequency in order to minimize land mobile interference.

The 70-page report, "Evaluation of the GOES-Data Buoy Interrogation Link," OT Report 76-106, is available at $4.50 per copy from the National Technical Information Service, Springfield, VA 22161. Its accession number is PB-261-872/AS.

Stored Data Accessible Across Atlantic

As a result of a recent FCC authorization, computerized information stored in the U.S. and in the United Kingdom will soon be accessible to users across the Atlantic Ocean. Western Union International, Inc, 1 WUI Plaza, New York, NY 10004 will initially offer Database Service (DBS) access through Tymnet, Inc's domestic network. Later, additional domestic network interconnections are expected. DBS is compatible with data terminals operating at from 110 to 1200 bits/s. □

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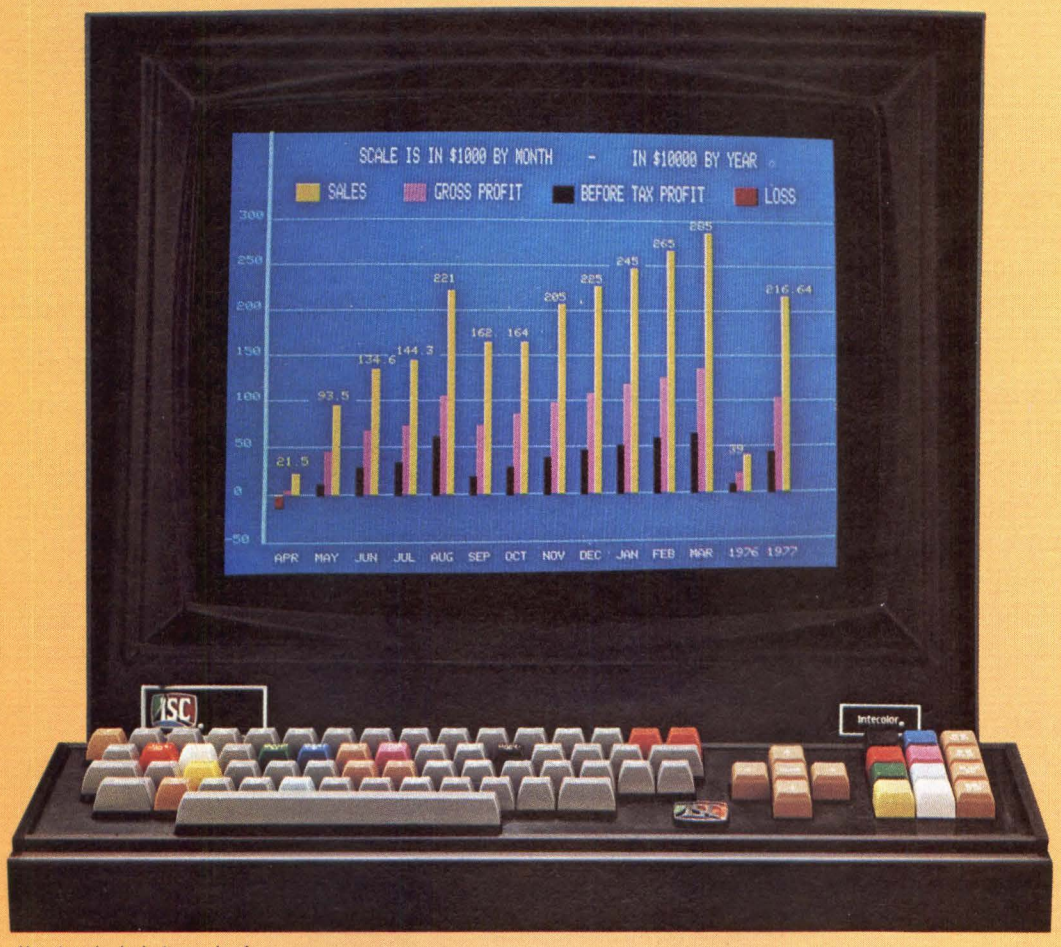

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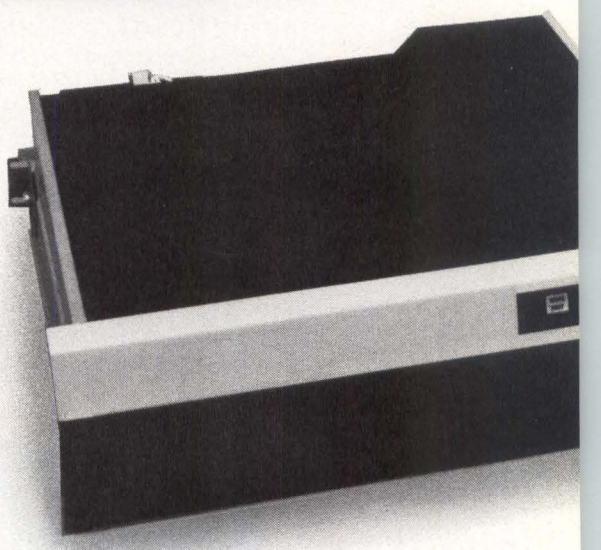

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	Compatibility	DEC RK05	DEC RK05	–	–	–	–
CAPACITY	PDP-11 (megabytes)	2.5	5	10	2.5	5	10
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CIRCLE 20 ON INQUIRY CARD

Mini-Diskette-Based Computer System Uses Support-Free Software

In introducing computer products that make use of technology to provide performance and low price, Wang Laboratories, Inc, One Industrial Ave, Lowell, MA 01851 emphasized the importance of increasing performance and power while reducing their cost and complexity through aggressive application of technology. Cited as examples were the PCS-II which is claimed to be the industry's first mini-diskette-based system, and extensive use of microprocessors—in some cases as many as four—in terminals, printers, diskette drives, and communications controllers.

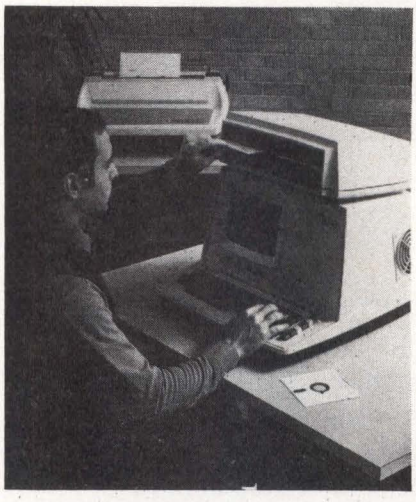
A second-generation personal computing system, the PCS-II is equipped with one or two mini-diskettes, high speed printer, large screen CRT/keyboard, and a high speed processor with 8k bytes of user available memory (expandable to 32k bytes). Addition of the Option 62B binary synchronous communications controller converts the computer to an intelligent terminal with total business computing capability.

System support is provided by the 2236 transaction terminal, a semi-intelligent device that changes personality when its microprocessor controller is reloaded; and the 2236 MXC mini-front-end which links multiple terminals to a single processor. The 2265 DMS permits concurrent multiuser sharing of the 2265 intelligent disc drive; printers range in speed from 15 char/s to 600 lines/min, and 2270A series diskette drives allow 2-way searching, reading, and writing between Wang and IBM 3740-compatible devices.

Software which operates on the PCS-II allows the Management Planning System to perform financial modeling and budgeting, statistical forecasting, business graphics, and other sophisticated functions. A mortgage management system includes a management control module that permits querying of files at any point in the process of mortgage preparation, automating all mortgage paperwork—by performing all necessary calculations and printing all related forms. The Time/Check system makes available accurate up-to-date management reports including an employee time report, employee analysis, analysis of billable and nonbillable time, and daily cash journal. A letter writing and editing option can produce personalized mass mailings for automatic client service.

Other applications software includes Lifeline, a fully automatic system that prepares insurance proposals for insurance carriers; Wang/Cash, an accounting package intended for small accounting firms and independent accounts; Patient Billing System, an automated patient billing and insurance processing system for doctors and dentists; and AUTO/MATE II, which provides fast processing time, random file searching, and information storage for automobile dealership financing and insurance applications.

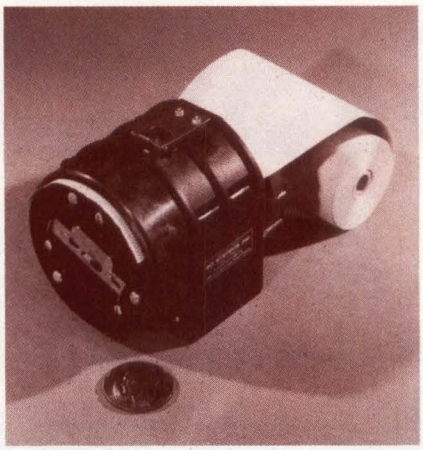
Circle 140 on Inquiry Card



PCS-II, a mini-diskette-based computer system from Wang Laboratories, provides random access to data and program storage in a low cost desktop unit. Standard are video display, alphanumeric BASIC keyword keyboard, and a single mini-disc drive. Expansion is accommodated with additional user-accessible memory, character and line printers, and another disc drive

Low Price, 2200-Char/s Rotary Printer Has Only Nine Moving Parts

Reportedly the first of its kind—using a totally different concept of printing mechanisms—the series 1100 rotary printer introduced by SCI Systems, Inc, 8600 S Memorial Parkway, Huntsville, AL 35802 prints at a nominal rate of 2200 char/s on 4-in (10.2-cm) wide, continuous roll electrosensitive paper. Including paper holder and electronics, the printer is only 4" wide by 5" high and 9" deep (10.2 x 12.71 x 22.9 cm) and weighs only 3 lb (1.35 kg). Yet it can print 136-column data with standard 10 char/in (3.9 char/cm) spacing —at a 70-dB noise level, which is about one-sixth that of an electric typewriter. A full CRT screen can be printed in less than 1 s; 24 lines of 136-column computer data can be printed in 1.5 s. Electronics are fully buffered.



Series 1100 rotary printer produces hardcopy at 2200 char/s on 4" wide electrosensitive paper. Full unit as shown is only 4" W x 5" H x 9" D (10.2 x 12.7 x 22.9 cm) and weighs about 3 lb (1.35 kg)

There are only three main elements: drive unit, printhead, and paper. Most wear items are concentrated within the cartridge type printhead which has an expected life of over 25 million characters and can be replaced in less than 10 s. Since user cost for the head will therefore be less than one dollar per million characters, the overall cost is much less than that of a typewriter ribbon. The drive unit, in comparison, has a rated life exceeding 8 billion characters.

Electrosensitive paper, equivalent to Nicolet type ESP-20, consists of three layers: a base paper coated with a black pigment and then a 10^{-6} thick, vacuum-deposited surface coating of aluminum. As print styli move across the paper, electrical pulses remove the surface layer and expose the black undercoat in a 5 x 7 dot matrix to form characters.

(Continued on p 30)

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CAN YOU AFFORD THE TIME REQUIRED TO DUMP YOUR CRT OR MINI USING SLOW THERMAL PRINTERS SUCH AS THE TI OR NCR 30 CPS UNITS???

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OEM prices go below $1200.00 in large quantities and lease terms are also available. ALL SERIES 200 printers are backed by warranty and nationwide service is available.

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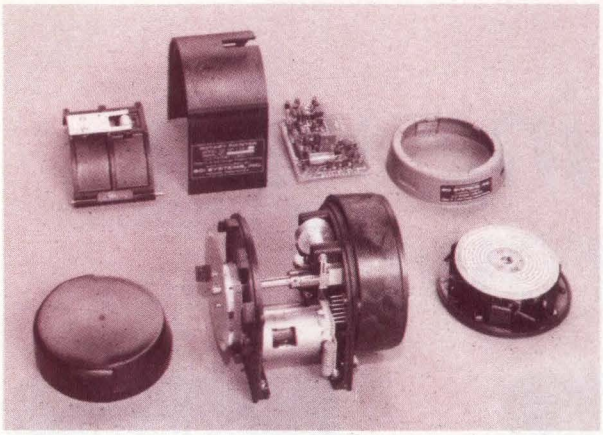
CIRCLE 21 ON INQUIRY CARD



Much of the SCI rotary printer is made up of plastic parts; most of remainder is stamped or machined metal. Small dc motor drives all elements

Only nine basic moving parts are involved and the printhead is the only replaceable element. There are three multiwire styli assemblies in the printhead, mounted 120-deg apart on a plastic rotor and protected by a molded cover. A slip ring disc, which forms the rear structure of the printhead is connected to the styli through flexible etched cables. Slip ring brushes connect printhead to drive electronics.

One small dc motor drives all elements of the printer. The central shaft, belt-driven by the motor, supports the printhead at the front and a code wheel at the rear of the drive unit. A single paper feed roller is driven from the shaft through a worm gear arrangement.

Paper is inserted through the writing platen and formed into a 120-deg arc by a snap down top cover. In operation, the drive roller continuously *pushes* the paper through the unit. Centrifugal force extends the styli wires through slots in the printhead cover and into contact with the platen and paper as the head rotates.

Writing pulses are timed directly from the central shaft code wheel so that constant size characters are formed regardless of motor speed. Each stylus assembly prints a column of characters as it sweeps over the paper (three columns per revolution.) Printed line length is unlimited but typically 40, 80, or 132 char/line. A maximum of 24 lines can be printed on the 4" (10.2 cm) paper.

Much of the unit consists of plastic parts. The housing, for instance, has plastic end plates, top and rear covers, and writing platen which surrounds the printhead. Of the relatively few metal parts, most are stamped or machined.

Nominal specifications for the 1100 rotary printer include: character set, 64 ASCII (96 optional); character spacing, 10/in (3.9/cm) horizontal, 7/in (2.8/cm) vertical; character structure, 5 x 7 dot matrix, 70-line/in (27/cm) resolution (7 x 9 matrix, 100-line/in (39/cm) option available in midyear); paper feed speed, 10 in/s (25.4 cm/s); rotor speed, 1800 rpm; and stylus speed, 350 in/s (889 cm/s).

Power is 55 W printing, 5 W standby. Temperature ranges are 0 to 55°C operating, −40 to 85°C storage (extended ranges optional), 10 to 95% humidity, noncondensing. Standard parallel and serial interfaces as well as custom interfaces are available.

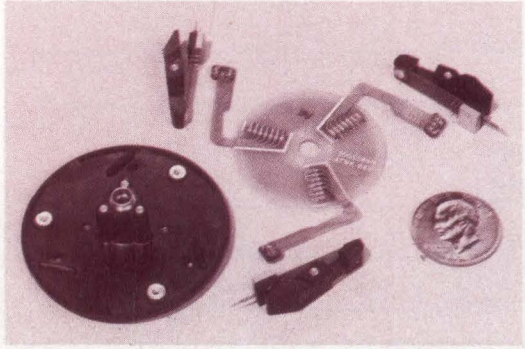
The printer is inherently resistant to shock and vibration. There are no levers, cams, hammers, solenoids, or reciprocating parts.

In its present 4" (10.2 cm) configuration, the rotary printer is quoted at about $300 in OEM quantities. For a single unit, sold to an end user through a distributor, the price would likely be less than $1000.

An 8.5" (21.5 cm) model, predicted for late 1977, will print 80 characters/line, 10 char/in (3.9/cm) at a rate of 4000 char/s. Letter size, legal size, and continuous roll paper lengths will be available. For 132 char/line at 16.5-char/in (6.4/cm) spacing the print speed will be 6600 char/s. As a column printer it will produce a 50-line by 132-column format with lines running the length of an 8.5 x 14" (21.6 x 35.6 cm) sheet, at 2500-chars/s throughput. Expected price for this unit is only 30% above that of the 4" model since much of the fabrication will be identical.

Plans for 1978 include a 200-line/in (78/cm) resolution printhead with 13 x 17 dot matrix characters. Future versions will include full graphics capability and an OEM facsimile mechanism with a compatible head for high speed facsimile scanning.

Circle 141 on Inquiry Card



Printhead, shown here in exploded view, is only replaceable element in rotary printer. Three multiwire styli assemblies are mounted 120 deg apart on plastic rotor

Disc Drive Offers Both Fixed and Moving Heads For Minimum Access Times

Intended to fill memory needs for a variety of minicomputers and medium-scale computer systems, 3300 series drives can be configured with one, two, three, or four nonremovable discs. Units incorporate moving heads and can include fixed heads to minimize access time to data.

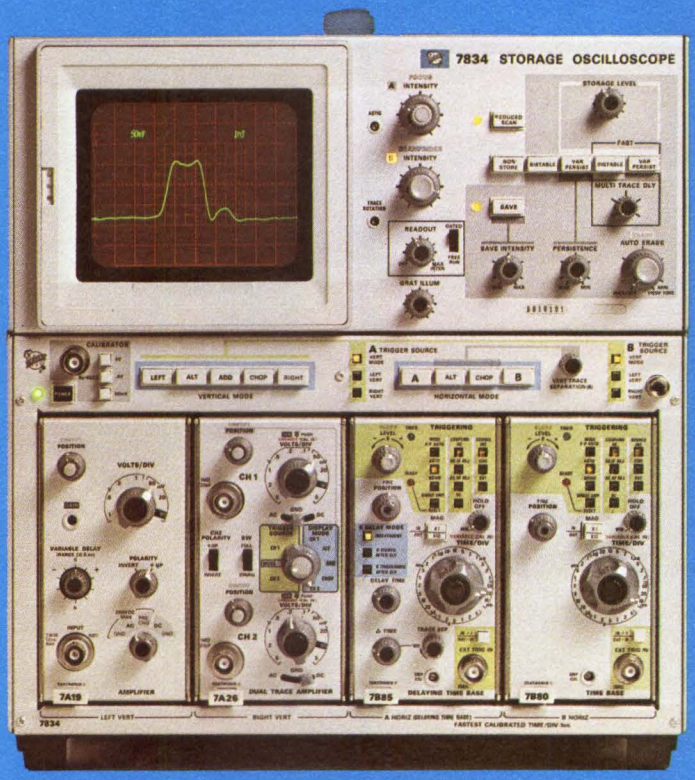
Eight models ranging from 12.4M to 74.4M bytes of moving head storage measure 7 x 23½ x 19" (17.8 x 59.7 x 48.3 cm) providing maximum capacity in a small package. Fixed heads with an average access time of 10.1 ms can be added to the same spindle up to 2.23M bytes in increments of 0.37M bytes. Overlapped seek enables read or write on fixed heads to occur while moving heads are undergoing a seek on the same drive.

Okidata Corp, Western Div, 849 Ward Dr, Santa Barbara, CA 93111 designed the positioner to take advantage of the fact that rotary inertia

Announcing a breakthrough in

FAST PULSE ANALYSIS

A storage oscilloscope that captures 1.4 ns rise time.



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Superior Performance. A stored writing speed of 2500 cm/μs, enabling you to capture single-shot rise times to 1.4 ns, 3.5 cm high, at full reduced scan amplitude (or 900 ps 2.25 cm high). System bandwidths from 160 to 400 MHz, depending on plug-ins selected. Four storage modes . . . bistable and variable persistence, FAST bistable and FAST variable persistence . . . to cover a wide range of storage applications. Autoerase for automatic display updating. A save control for 30 times longer viewing. Gated readout, which prevents the blooming that tends to occur between sweeps with nongated readout. Adjustable multitrace delay for varying the crt view time prior to storing the next sweep when using FAST transfer mode.

4-Compartment Flexibility. Perform more than one measurement at the same time without switching plug-ins. For example, store a single-shot event and simultaneously measure pulse width with a digital counter. Choose from over 30 7000-Series plug-ins for the combination your application requires. The selection includes the 7A19 for full system bandwidth, the 7D11 for digital delay, the 7L5 for spectrum analysis.

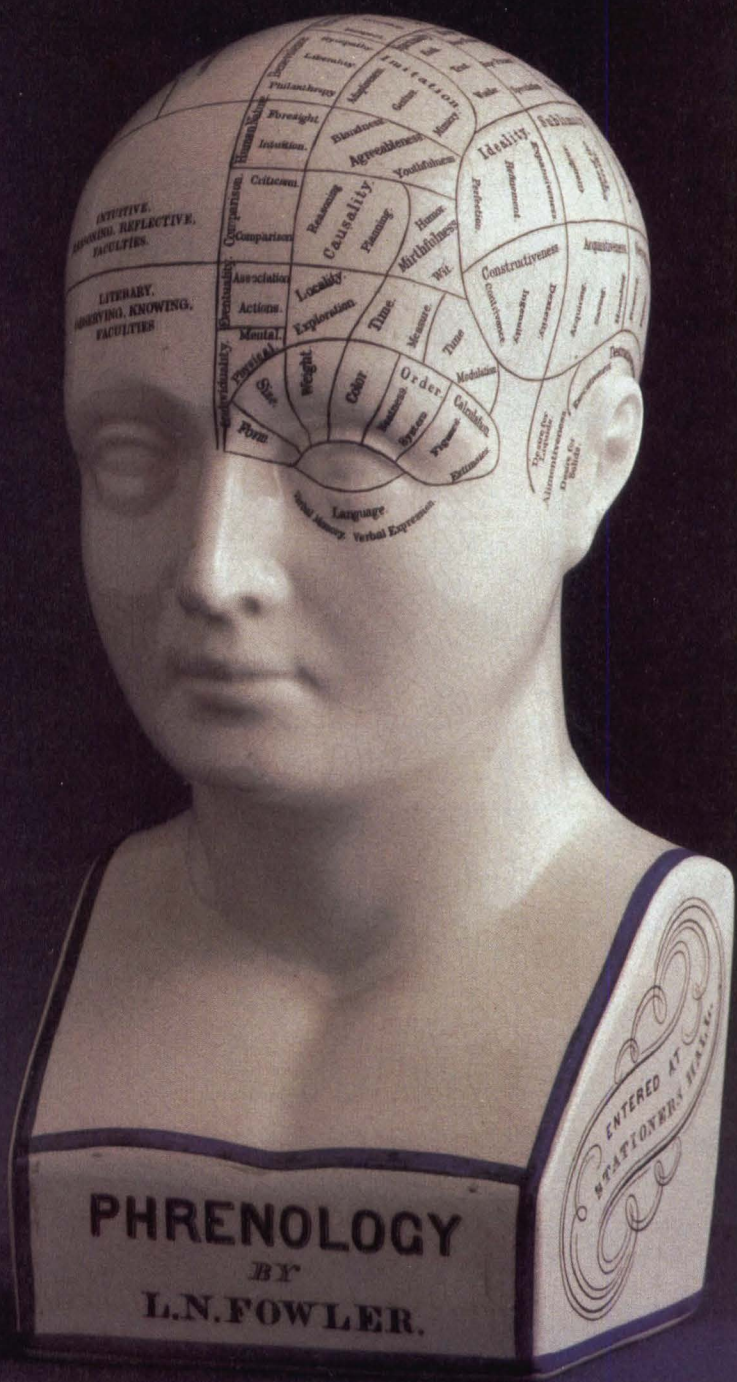
Future Expandability. The 7834 represents a breakthrough in oscilloscope technology. It follows the 7633 mainframe which introduced the then-highest stored writing speed of 1000 cm/μs. The 7B80 and 7B85 time bases, establishing a convenient delta delay measurement technique. The 7D01 Logic Analyzer and DF1 Formatter transforming the oscilloscope into a logic state—logic timing analyzer with a choice of 5 display modes.

The 7834. For fast pulse analysis in the laser fusion lab. For single-shot or low-rep-rate fast pulse analysis, glitch detection, or ECL logic analysis in digital design. For single-shot fast pulse analysis in destructive and nondestructive component testing When you buy into the 7000 Series, you're assured of technological advances that help set the pace for the oscilloscope world.

The 7000-Series . . . more than an oscilloscope

For a demonstration or more information, contact your local Field Engineer. Or write Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077. In Europe, write Tektronix Limited, P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

For technical data, circle 22 on Inquiry Card.
For a demonstration, circle 23 on Inquiry Card.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Verbal Expression
Causality
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Planning
Humor
Mirthfulness
Wit
Imitation
Agreeableness
Youthfulness
Ideality
Perfection
Constructiveness
Acquisitiveness

Introducing the SEL 32/75 System.

The Computer with a Subconscious.

Your eyes blink 25 times a minute. You don't realize it because this routine, like thousands of other vital routines, is handled by your subconscious.

That's important, because this parallel processing frees the conscious part of your mind for critical decisions.

This is also a good description of how the new SEL Regional Processing Units operate within the SEL 32/75 System. Working independently, these RPU's contain sufficient control and buffer storage areas to process an I/O region and transfer the resultant data directly to main memory. Computer system throughput is further enhanced by High-Speed Floating Point Hardware, Writable Control Storage, and flexible interleaving.

The SEL Memory MAP efficiently manages up to 16 million bytes of main memory, with no instruction overhead.

Sounds like a big system, doesn't it? SYSTEMS can link 20 CPU's, with hundreds of Regional Processing Units, into one multiprocessor network.

You see, the well-established SEL 32 computers fit the term "minicomputer" in price alone. Based on true 32-bit architecture, all are fast, powerful machines using functional, proven software. SYSTEMS computers are proving their worth in big jobs like seismic exploration, power plant operations, aircraft simulation, and scientific computation.

The SEL 32/75 System fits neatly as head of the SEL 32 family. It's more powerful, more flexible, more throughput-oriented than any computer we've ever built.

We'd like to help you explore how the SEL 32/75 System could simplify your computing requirements. Just circle our number on the Reader Service Card, and we'll send our brochure in the blink of an eye.

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CIRCLE 24 ON INQUIRY CARD

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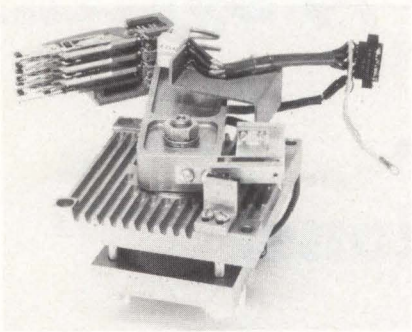


Small size and low cost are achieved in Okidata's series 3300 disc drives through use of a rotary head positioner. Heads are mounted directly on a rotating arm which moves across the disc surface much like a phonograph arm. This design does away with the typical head carriage and its mass, and eliminates precision rails and ball bearings

is the product of mass and radius squared. The positioner arm in the 3300 is mounted directly to the rotor of a high torque brushless dc motor. While the rotor has high mass, its effective radius in the system is small compared to the radius at which the heads are located; this results in minimum inertia and therefore minimum power dissipation.

The resulting positioner is compact. Only two bearings are involved in the entire system, and the motor can be removed from the drive without disturbing the arm or heads, which are located in a "clean" enclosure.

There are two data heads per surface. The track-following positioner servo system uses the bottom surface of the lower disc, which contains prewritten servo tracks used in positioning heads; this eliminates close tolerances and thermal problems common to drives which use devices in the positioner to derive track position information.

Optional fixed heads are mounted on a tray-like assembly containing head terminations and diodes. These assemblies can also be mounted to use a portion of the servo disc surface and also the entire top surface.

The interface is designed such that moving head drives may plug into a system intended to operate with the CDC 9760 storage module and operate to its specifications. Moving head and fixed head hybrid drives use a common interface. A single interface board contains all receivers, drivers, and electronics necessary to the standard interface and interface options.

The low cost units use Winchester 3340-type heads and media, and provide data separation; error recovery features such as early/late datastrobe; and track offset, direct track addressing, and index/sector lookahead. Both fixed and moving heads have 18,560 bytes/track and data transfer rates of 7.33M bits/s. Average access time is 38 ms. Expanded capacity and transfer rate will be accomplished using 3350 Winchester-type heads; maximum moving head capacity is expected to be 127M bytes in the same package.

Circle 142 on Inquiry Card

80M-Byte Disc Drive Incorporates Reliability, Maintainability Features

BD-80 is an IBM 3330-type disc drive which offers 80M bytes of online capacity and design features to improve both reliability and maintainability. When interfaced with the 3300 formatter the drive supports sophisticated file management techniques in real-time, suitable for multiterminal and batch processing systems requiring high speed, random access to mass storage.

In the drive, Ball Computer Products, Inc, 860 Arques Ave, Sunnyvale, CA 94086 has combined reliability and maintainability with features that include a 3330-type spindle interface, a track-following servo-system that requires no external references, a triple cooling system, a sealed-in actuator mechanism, and a constant-voltage power supply. The combination of features reduces common disc problems: dust accumulation on precision mechanisms, head crashes caused by contamination, hot spots in circuitry, and susceptibility to recording errors due to line power variations. Separate chassis for actuator and motor control mechanisms, power supply, and logic, and plug-in cards simplify maintenance as well as troubleshooting and repair. Operating problems are isolated by the system itself to power, interface, read, write, or head problem.

Basic disc drive contains dynamic braking, standard digital I/O, and an ac power cable and power supply. The BD-53 disc pack is based on IBM 3336-11 components; it contains five read/write surfaces with 815 cylinders/surface at 370 tracks/in. Recording densities are 6060 bits/in, 20,160 bytes/track or approximately 100M bytes/pack (unformatted). Start/stop times are 20 s. Average access time is 30 ms and data transfer occurs at 1.2M bytes/s.

The 3300 formatter offers large mainframe disc handling functions such as multiple drive capability. Features include seek overlap operation, multirecord transfers, IBM error correction codes, and high speed drive support. The unit supports variable size record formats, internal data encoding and decoding, error correction, and a sophisticated FIFO buffering technique that matches disc speed to minicomputer timing. It can accommodate up to eight spindles in a daisy chain arrangement. An internal microprocessor permits seek overlap operation.

Circle 143 on Inquiry Card

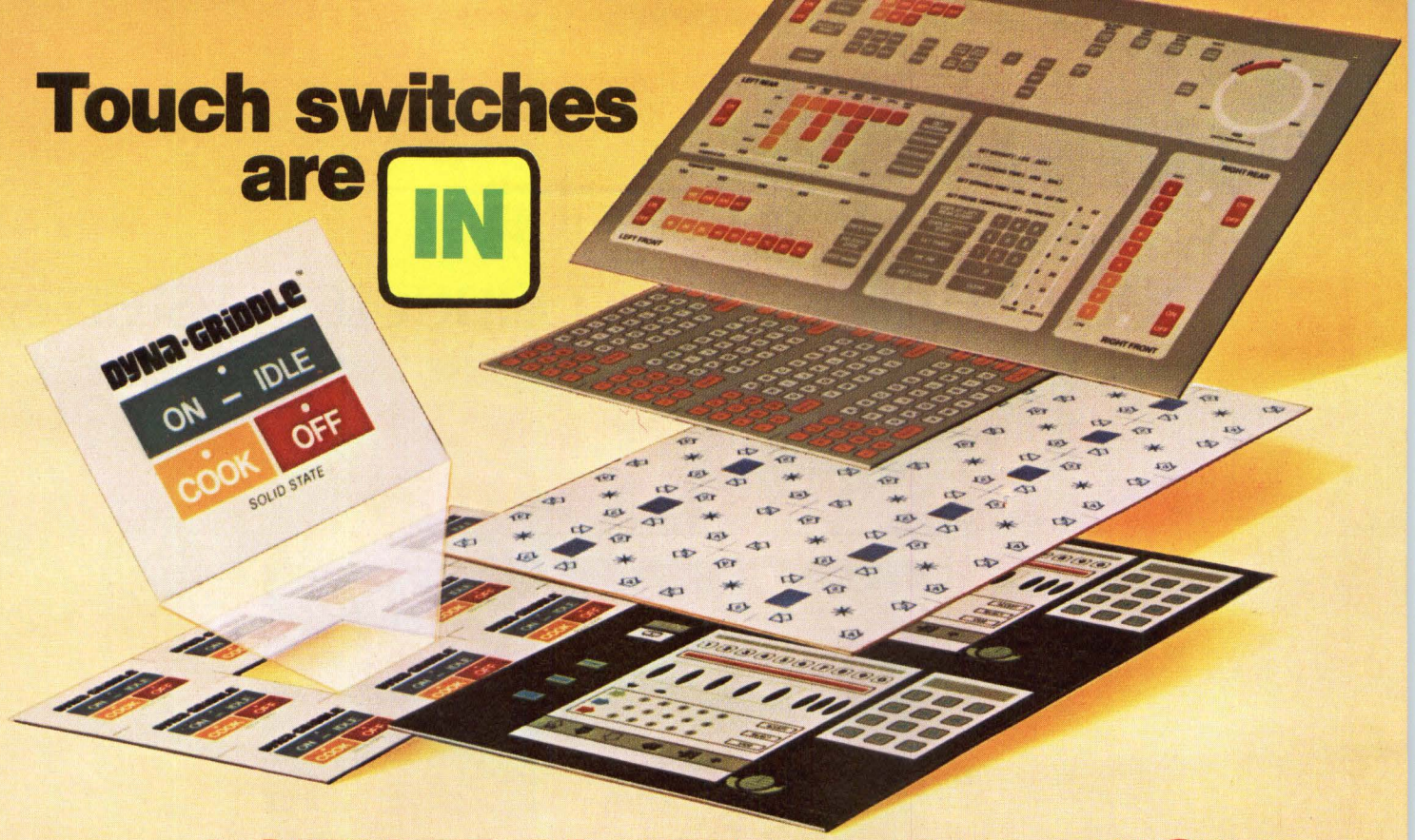
Battery-Powered Cassette Recorders Playback Directly on Terminals

ICT series write-only incremental digital cassette transports and recorder systems offer up to 2.2M bits of data capacity on a 300-ft cassette. Miniature transport uses a Philips data cassette, low power incremental stepping motor, and CMOS electronics, drawing just 700 mW from a 12-V battery when writing, to provide portable battery-powered data collection.

With the systems, Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021 offers a simplified approach to design by reducing data entry, retrieval, power-up, and power-down considerations to the point of providing and accepting logic levels at the required times. Circuit card modules are specified in terms familiar to circuit designers who know digital logic. In a complete system, design details of the transport's flux levels and motor drive are transparent to the designer, requiring only knowledge of ultimate word size, bit rate, and data capacity. However, full specification of transport and individual card modules allows customized systems to be created at any level.

Systems accept a variety of data formats ranging from full synchronous serial to 40-bit (five byte) parallel. Basic format is 8-bit bytes recorded at about 6 bytes/s; these bytes are externally coded as ASCII alphanumeric character bytes for direct playback on terminals. Optional analog inputs may be recorded by digitizing channels with low power A-D converters, to provide direct octal printout of A-D informa-

Touch switches are IN



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When Centralab introduces touch switches you can be sure they're "In". Backed by 40 years of switch know-how, and after years of intensive research and testing, Centralab is now delivering, in batch-process volume, a complete touch switch system. We call it MONOPANEL.

MONOPANEL is a thin, light, flat, front panel subassembly containing micro-motion touch switches already mounted and interconnected . . . with LED's, nomenclature, graphics and colors to meet your functional and aesthetic requirements.

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MONOPANELS are batch-processed as 11″ X 17″ master panels only .075″ thick, each containing up to 700 switches. Every Monopanel is a complete, 100% pre-tested subassembly containing switches, front panel and graphics.

60,000,000 Cycles Without Failure!

The basic MONOPANEL switch has been operated for sixty million switching cycles without mechanical or electrical failure. And MONOPANEL has been tested and proven against 22 separate mechanical, electrical and environmental standards.

Custom Designed For Your Application

On each 11″ X 17″ panel you can custom-design individual boards to meet your front panel needs. The illustration above shows just a few of the almost endless variations possible from each master panel.

Unlimited Graphics Available

The flat, smooth, front panel surface permits unlimited choice of graphics. Functions may be grouped by color, with 480 colors available. Thirty choices of type style and size. And whatever visual symbols meet your specific needs.

THIS IS MONOPANEL:

- A complete touch switch subassembly, ready to mount.
- All switches and graphics on a .075″ thin panel.
- Flat, spill-proof surface wipes clean.
- Noiseless.
- 100% tested.
- Choice of terminations.
- Operating voltage: 50 V max.
- Operating current: 100 mA max.
- Contact resistance: 0.2 ohms typical.

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CIRCLE 25 ON INQUIRY CARD

Reduce your vulnerability. Specify Amphenol® connector systems.

You'll get just the right connector.
Plus quality that makes you look good.

Waiting for the missing link in your product—the connectors—can be more than frustrating. A delay can leave you wide open to the perils of lost business and lost profits. So can less than top-notch quality.

Relax. There are thousands and thousands of famous Amphenol quality connector products. Many are available for prompt delivery from a close-to-you distributor. And even if you order a highly specialized connector, you won't have to wait long. Just long enough for us to give it quality worth waiting for.

You get that kind of prompt availability in quality connectors like those shown here. And a host of others for consumer and business products, data and word processing equipment, aerospace and military applications, nuclear power, telephony, and more.

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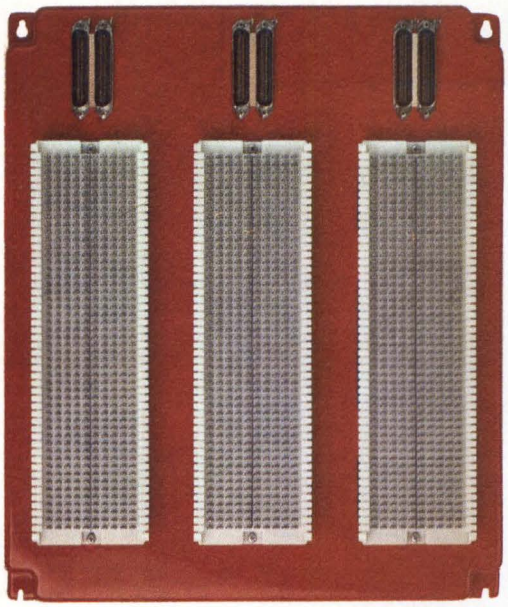
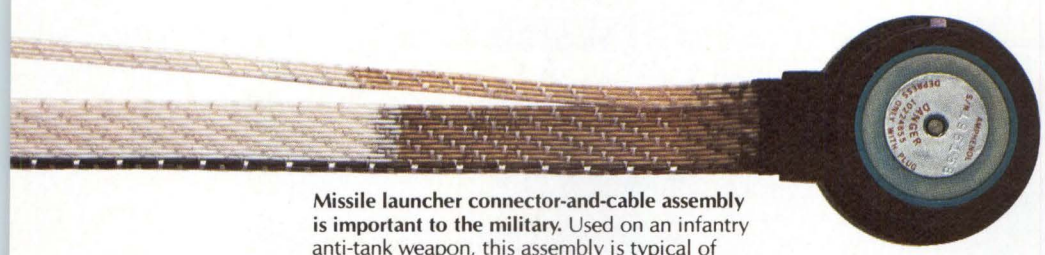


Cut telephone key-set installation costs in half. With System 66 connectorized red-field back panels. They're factory pre-wired.

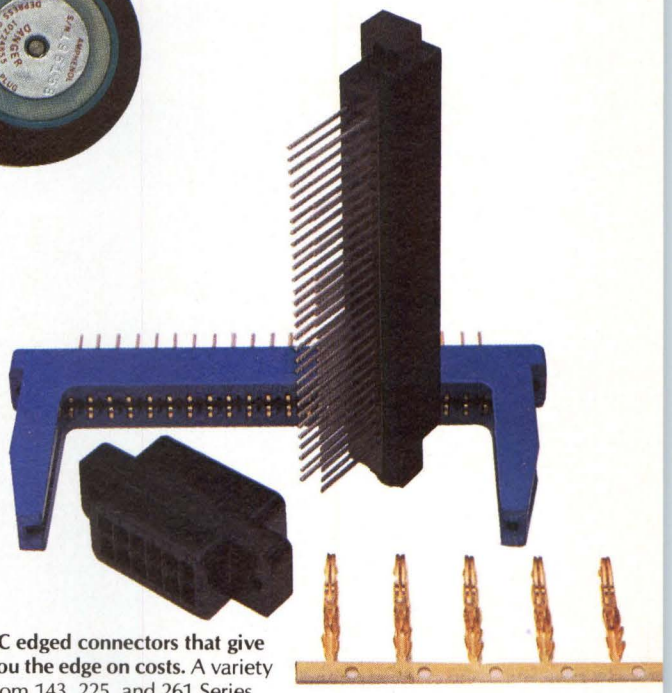
Microphone connectors that are quick to disconnect. Our QWIK-91 Series are efficient, easy to operate and an attractive complement to quality audio equipment.

The big name is SMA's. Amphenol, of course. Stainless steel or beryllium copper. Built-in quality ensures performance to your toughest design demands.



Missile launcher connector-and-cable assembly is important to the military. Used on an infantry anti-tank weapon, this assembly is typical of our total design capability.

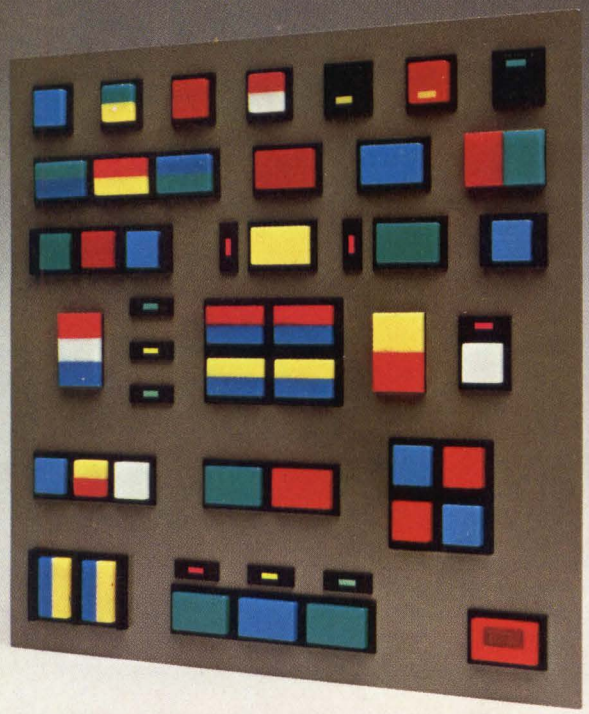
Radiation-resistant connectors for the nuclear power industry. Our 206 Series for containment rooms. Features stainless steel shells and crimp Poke-Home® contacts.

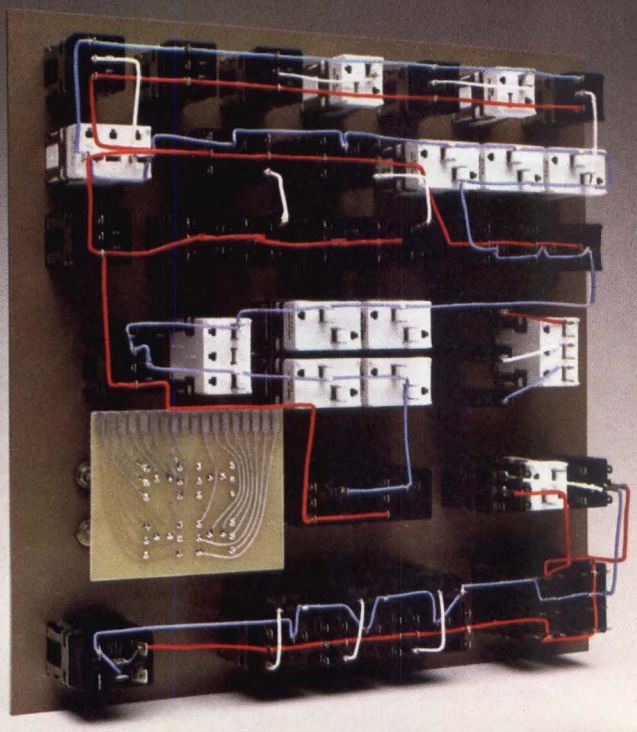


PC edged connectors that give you the edge on costs. A variety from 143, 225, and 261 Series. For solder, wire-wrap, and crimp snap applications.

The right idea at the right time.

AMPHENOL Connector Systems BUNKER RAMO®





The only pushbutton that gives flexibility to designers...

...without giving fits to the people who wire it.

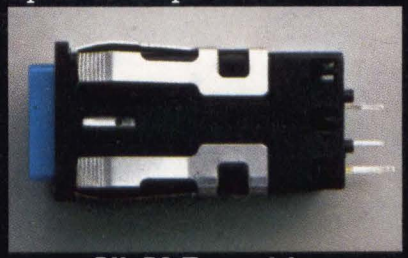
Until now, you wouldn't have counted on good-looking pushbuttons to look nearly as good when it's time to wire them.

But the AML (Advanced Manual Line) from MICRO SWITCH has changed all that.

AML devices combine button height, bezel size and compatibility of square and rectangular shapes to harmonize your panel. And the line is so broad, you won't need different-looking units to perform different functions.

Displays range from split screen and hidden color to a unique, three-segment lens cap indicator, all with transmitted or projected illumination, and a choice of lamps, including a T-1¾ wedge base lamp, neon and LED.

AML units also offer electrical flexibility, with features like three different electrically rated switches in the same size housing. Solid state pushbuttons that operate at 5V or 6-16V with a built-in regulator, sink (TTL) and source (CMOS). Electronic control from logic switching to 3 amps, 120 VAC. And power control up to 10 amps at 120 VAC.



All AML pushbuttons offer the same shallow depth for unique, single-level termination and easy wiring. You either snap them in place from the front, or subpanel mount them, using individual, strip or matrix mounting hardware.

And every AML device is designed to meet IEC, CEE24, UL and CSA standards.

Write for our "Control Panel Layout Design Guide." Contact your nearest MICRO SWITCH Branch Office or Authorized Distributor. Or call 815/235-6600.

Either way, you'll end up with a pushbutton that works as well as it looks.

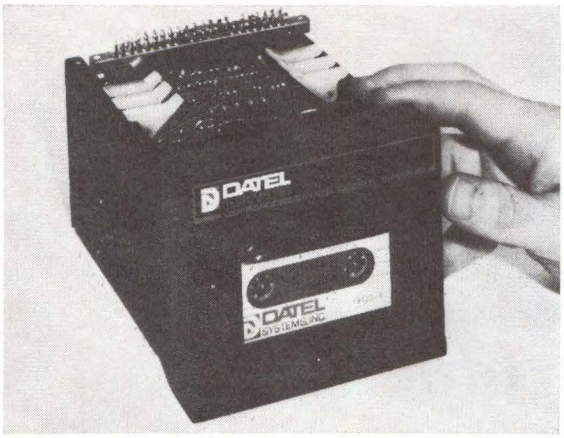
MICRO SWITCH

FREEPORT, ILLINOIS 61032

A DIVISION OF HONEYWELL

MICRO SWITCH products are available worldwide through Honeywell International.

Circle 27 for data.



Datel's ICT series miniature cassette transport uses CMOS circuitry and an incremental stepping motor to allow operation from a 12-V battery. Automatic block length termination and printer formatting control features permit data to be printed directly from the system on any ANSI-compatible terminal

tion on a display terminal or teleprinter.

Special features include automatic block length termination and printer formatting control using spaces, carriage returns, and line feeds generated by recorder electronics. This permits readable data to be printed with selected line lengths directly from ICT-WA systems to an ANSI-compatible terminal I/O device. A computer is needed only for arithmetic and to reformat the output.

Basic transport is a panel mounting assembly, which fits through a front panel cutout; it includes stepping motor, tape head, both hub assemblies, and optional EOT/BOT photodetector. All electronics are mounted in an optional 5-slot PC card cage which attaches to the rear of the transport. Transport and cards are available separately to allow complete customization of digital recording systems.

Circle 144 on Inquiry Card

Minicomputer Adapts to Freestanding Interactive or Distributed Processing

NCR 8250 is a general-purpose minicomputer system that offers up to 80M bytes of disc storage as well as a COBOL-oriented interactive multiprogramming operating system. It can be used as a communications-oriented processor or as a freestanding interactive multiprogramming system.

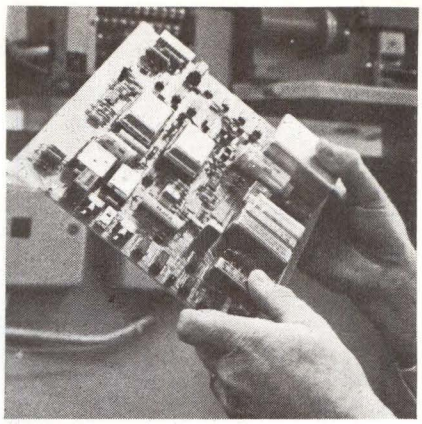
A 16-bit general-purpose minicomputer, which uses standard 19" rack-mounted plug-in circuit boards, the processor has from 48k to 128k bytes of MOS memory with automatic battery protection. In addition to processor and memory, the vertical cabinet can contain one or two disc storage units providing up to 19.6M bytes of storage, and one or two magnetic tape cassette handlers. The system is offered by NCR Corp, Dayton, OH 45479.

Operating software permits several applications operating at the same time to share common sections of coding from a single pool rather than duplicating coding for each application. Other features allow conversational question and answer procedures to simplify start of day procedures; three levels of security for each terminal, to prevent unauthorized use of certain system commands; and object code changes which reduce memory requirements and increase processing speed.

Circle 145 on Inquiry Card

Recorded Message Machine Is First Use of Magnetic Bubble Memory

A machine that stores and announces recorded messages is claimed to be the first to operate with a magnetic bubble memory and to be the first application of this technology. The machine was developed at Bell Telephone Laboratories, Mountain Ave, Murray Hill, NJ 07974, and is being tested in one of Michigan Bell Telephone Co's Detroit switching offices. Called the 13A announcement system, the machine is being used to record and announce standard repetitive 12- or 24-s "call assist" messages, each of which can be played back to as many as 500 telephone lines simultaneously.



Message board from Bell Lab's message announcement machine contains two magnetic bubble memory packages mounted one above the other in the center top half of the board. Four garnet chips in each package provide storage for 272,484 bits of digitized information

In this application, magnetic bubble technology provides the advantage of increased storage capacity in the same physical storage space, as well as low power consumption and nonvolatility. The bubble memory in the machine contains four garnet chips, each with a storage capacity of 68,121 bits—equivalent to about 12 s of digitized speech. Measuring 1.2 x 2.2 x 0.6" (3.05 x 5.59 x 1.52 cm), the package has 32 pins for external connection; a Permalloy outer case provides necessary shielding against possible external magnetic fields. Each board contains a maximum of two magnetic packages; one message is provided on each board. (Operation and details of a similar memory for use in a voice recorder are reported in *Computer Design*, Apr 1976, pp 38, 43.)

Instead of being recorded on a magnetic drum turned by a motor, messages are stored in digital format—in a code represented by the presence or absence of bubbles—in the machine's magnetic bubble memory. While messages stored on the drum deteriorated with use, messages processed by the 13A do not lose quality with repeated playing. About the same size as its predecessor, which handled one message, the 13A records and announces up to eight different messages.

Additional information on the technology of magnetic bubble memories can be found in "Magnetic Bubble Systems Approach Practical Use," by J. Egil Juliussen, *Computer Design*, Oct 1976, pp 81-91.

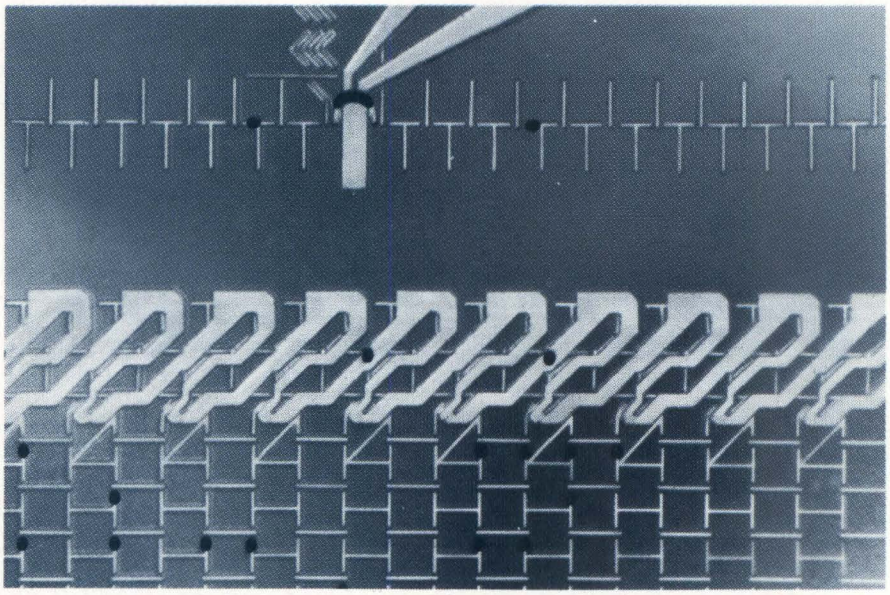
Circle 146 on Inquiry Card

Nine new memories

from the leader... Texas Instruments

Progress in memories comes quickly at Texas Instruments. Here are nine new memory devices. Spanning a wide range of technologies ... from NMOS to firsts in advanced processes – a magnetic bubble memory and a charge-coupled device memory.

There's higher performance, too. And broader choice. All reflecting memory leadership. Enabling you to explore new concepts. Upgrade existing designs. Achieve greater cost effectiveness. And improve system operation.



92K magnetic bubble memory

. . . doesn't forget to remember

The first commercially available bubble memory. TI's solid-state TBM 0103 . . . 92,304 bits.

Non-volatile, it remembers when the power is off. A natural for innovative applications requiring portability. Programmable calculators. Data loggers. Voice storage. Measurement and test equipment.

Use the TBM 0103 in intelligent terminals. Word processing. Controllers. As an alternative to disk and drum storage. And the new TBM 0103, with its microprocessor-compatible interface family, can handle your microprocessor mass memory function.

Data is written into and read out of a major loop, stored in minor loops. Result: Serial input I/O with random access to 641 pages 144 bits wide. Average access time: 4.0 milliseconds. Data rate: 50 kilobits per second.

Single-chip construction enhances reliability. A 1.02 by 1.1 by 0.4 inch 14-pin dual-in-line package contains the bubble chip and all necessary magnetics. Combines low initial price with system packaging flexibility and efficiency.

Prototype quantities are available now. Coming soon: new interface peripherals, including an N-channel MOS controller.

CIRCLE 121 ON INQUIRY CARD

65K CCD memory

. . . plugging a gap

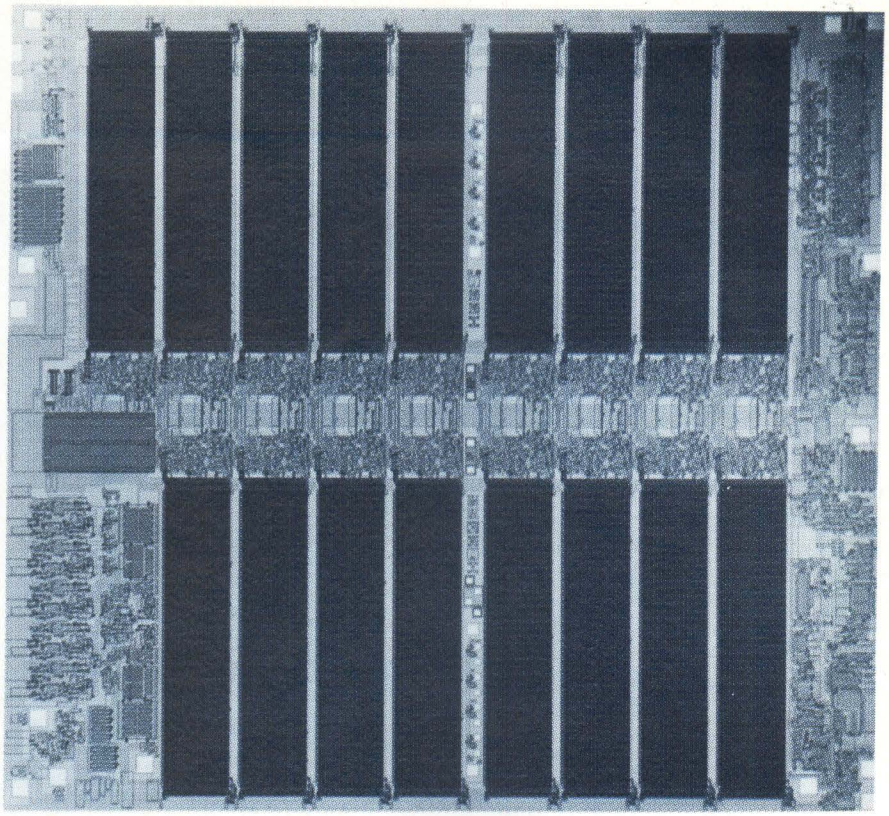
TI's new TMS 3064 is the first 65K charge-coupled device (CCD) memory on the market. Meets the need for a low-cost, high-performance memory between high-speed RAMs and low-speed, serial-access magnetic memories.

A new two-phase coplanar electrode CCD structure developed by TI, coupled with the standard double poly N-channel silicon gate process, is the key to the cost effectiveness of the TMS 3064.

Only two non-critical MOS-level clocks are required. Operating at 5 megabits per second, the TMS 3064 has a typical power dissipation of 300 mW.

In a 16-pin 400-mil ceramic DIP, the TMS 3064 will be available in May in sample quantities.

CIRCLE 122 ON INQUIRY CARD



4K static RAMs

. . . high performance and density

Your choice of NMOS 4K memories is substantially broader with TI's new static RAM family. Fully static design eliminates the need for clocks and reduces support circuitry.

These new 4K RAMs operate from single +5 volt supplies and are fully TTL compatible. A chip select and three-state output simplify memory expansion.

They come in four speeds: 450, 300, 200, and 150 ns maximum access times. And two organizations. The TMS 4044 and 4046 are organized as 4096 words of one bit; the 4045 and 4047 as 1024 words of four bits. Typical power dissipation at 200 ns is less than 325 mW.

All four new RAMs offer identical performance, with the TMS 4046 and 4047 series having the additional advantage of a unique power-down mode – less than 10 mW power consumption.

The TMS 4044 and 4045 come in a space-saving 18-pin ceramic or plastic package; the TMS 4046 and 4047 in a compatible 20-pin configuration. Sample quantities are available now.

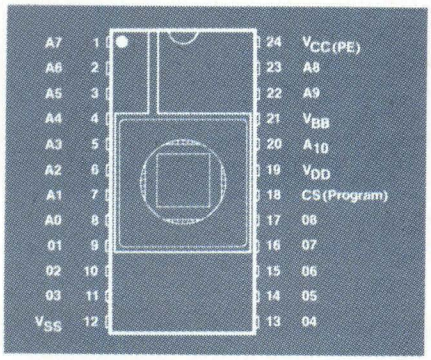
CIRCLE 123 ON INQUIRY CARD

16K EPROM

. . . a 2708 times two

TI's new TMS 2716 is a 16,384 bit device that plugs into existing 2708 sockets. You get twice the EPROM memory in the same space. So it's ideal for upgrading present designs. Same basic chip design and circuitry as the TMS 2708. Same production-proven N-channel process. Same power supplies. At 375 mW typical, the TMS 2716 dissipates less total power than most 2708s that have half the memory.

The TMS 2716 is a natural addition to TI's 8K EPROMs – the standard TMS 2708 and the low-power TMS 27L08. All are available now.



CIRCLE 124 ON INQUIRY CARD

16-pin 4K & 16K Dynamic RAMs

In addition to the industry standard 22 and 18-pin 4K RAMs from TI, a new high-performance 16-pin TMS 4027 is available in sample quantities.

A 16K dynamic RAM – the TMS 4070 (300 ns) – is available now. With an improved performance TMS 4071 (150, 200 and 250 ns) coming in the second quarter.

CIRCLE 125 ON INQUIRY CARD

For more information on any of these new memories, call your nearest authorized Texas Instruments distributor or TI field sales office. Or write Texas Instruments Incorporated, P.O. Box 1443, M/S 669, Houston, Texas 77001. Please identify the memory you are interested in by giving its TI part number.

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93113

Entry Level System Provides Floppy Discs For Cardless Computing

An entry level system for the series 90 family, the 90/25 offers integrated hardware and modular software for both new users and those wishing to upgrade their systems, and can be configured as a cardless system by using a diskette subsystem. Announced by Sperry Univac®, a div of Sperry Rand Corp, PO Box 500, Blue Bell, PA 19422, the 90/25 has as its nucleus a processor that is directed by microprogrammed instructions and is designed to perform random, sequential batch, communications, scientific, or inquiry/response information processing. Main memory can be expanded from 65k to 131k bytes.

Software consists of Operating System/3, which supports the simultaneously announced 8415 disc drive and 8413 diskette subsystem, other online peripherals, and communications; for terminals, CRT terminals, and intelligent terminal subsystems Job Control Language (JCL) is a set of descriptive control statements that define system requirements for each job and direct the operating system to assign necessary resources to execute it. OS/3 can support up to seven jobs running concurrently within three levels of priority. By means of multijobbing, steps from more than one job can be interleaved to increase throughput.

Integrated Communications Access Method (ICAM), an easy to implement system that includes a message control program to queue messages for delivery on demand, accommodates demands for communications capabilities. The IMS/90 Information Management System provides data file inquiry and update capability. Emulation of Univac 9200/9300 systems is accomplished using microprogram capability in the processor.

Peripherals for use with the system include the 8413 diskette, which provides cardless computing using IBM-compatible diskettes. It has a capacity of 242k bytes/disc and can read 128-byte records at 1500 records/min, and write at 850 records/min. The 8415 disc drive is a split-spindle fixed/removable device that permits on- and offline storage. It offers 24.8M bytes fixed storage; 8.3M bytes of removable storage. Also available are 300-line/min printer, 300-card/min reader, and communications terminals.

Circle 147 on Inquiry Card

Small Scale, Disc-Based Computers Offer Range of Growth and Performance

Small scale, disc-based computer systems added to the B 800 series have main processors operating at either 1 or 2 MHz with up to 131k bytes of main memory. A separate programmable data communications processor has up to four communications lines. Mass storage ranges from a low cost removable disc cartridge subsystem to a removable disc pack subsystem with up to 521.6 bytes of online storage. Burroughs Corp, Detroit, MI 48232 designed both the B 810 and B 820 around microprogrammed processors; multiple possible configurations of each adapt to particular operating environments.

Main memory for the 810 consists of 32k bytes of MOS memory with 500-ns access time for two bytes of data; the 820 has 16k bytes of MOS memory and 16k bytes of bipolar control memory with 70-ns access time for two bytes of data. Control memory takes advantage of the 820's 2-MHz speed, permitting faster execution of instructions. Both processors are expandable to up to 131k bytes of main memory.

Memory access is controlled by a separate microprocessor called a direct memory access controller (DMAC) which allows the disc I/O control and data communications processor to share memory cycles with the main system processor. The microprocessor controls the priority of access for the three sources and prohibits any one from preempting memory to the detriment of the other two.

Mass storage for the system is provided by an entry level removable disc cartridge subsystem which stores 4.6M, 9.2M, or 4.6M bytes with average access times of 80, 100, or 145 ms; a compact fixed disc subsystem with 9.4M, 18.8M, 28.2M, or 37.6M bytes/drive and average access time of 55 ms; and a removable disc pack subsystem with capacities of 65.2M and 130.4M bytes and an average access time of 33.3 ms.

The system may use a 10-MHz Data Communications Preprocessor (DCPP) which can service up to four communications lines in full- or half-duplex mode in a multipoint or point-to-point network. A microprocessor with standard memory of 6144 12-bit words, the DCPP operates concurrently with the main system processor, handling all processing associated with various line procedures and communications line management. The main system processor becomes involved only when a complete message has been assembled and is available for application processing.

System operation is supervised by a comprehensive executive system, the Master Control Program (MCP), which assigns memory, manages I/O, communicates with the operator, logs system use, loads programs, maintains a library of all files, and supervises other functions. MCP forms the key to virtual memory operation and multiprogramming, enabling the system to execute multiple programs that are larger than the main memory.

Circle 148 on Inquiry Card

Programmable Terminals and Controllers Collect Factory Data

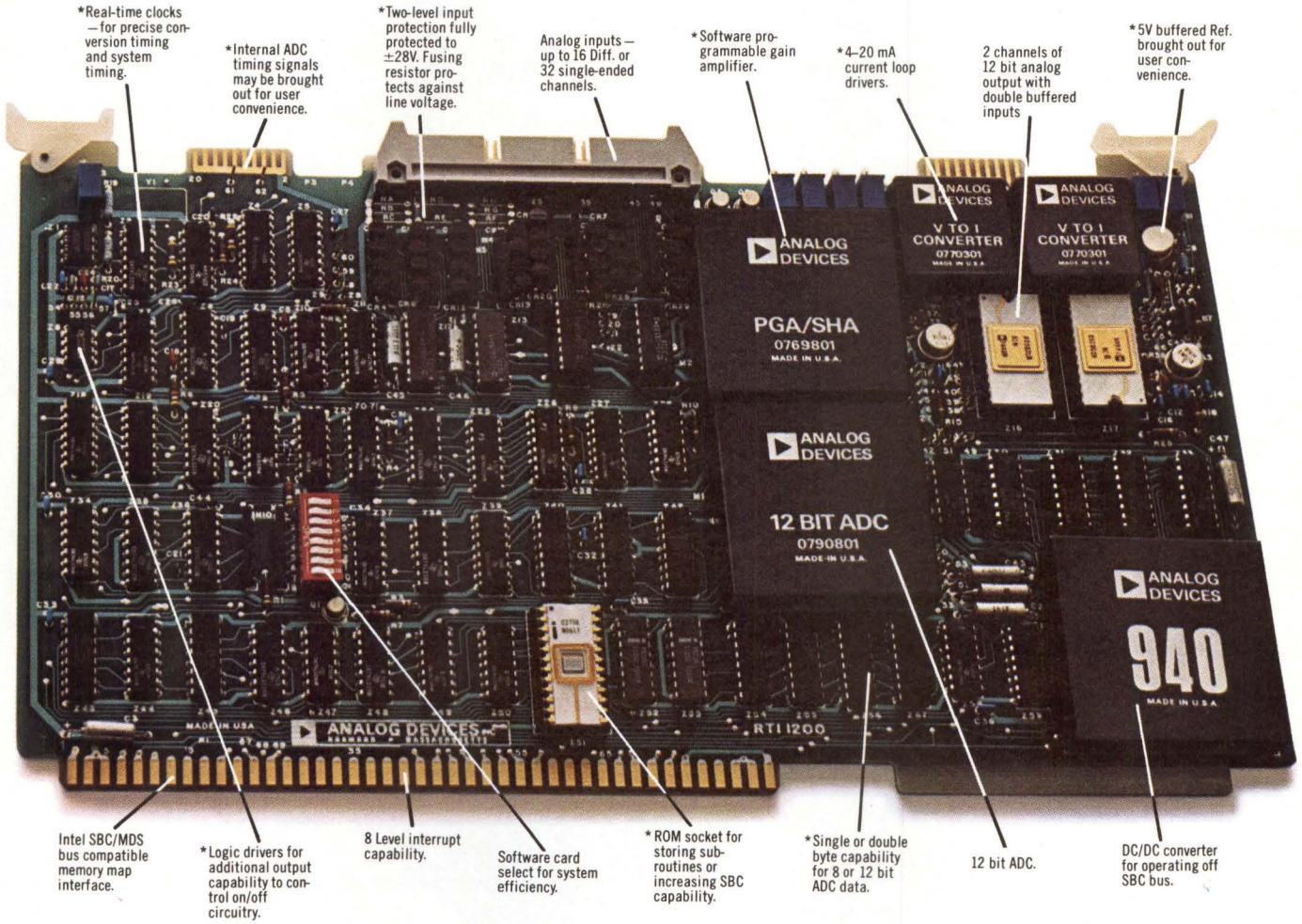
Compact, programmable data collection terminals and communications controllers, tested in conformity to MIL-STD-810, assure reliable operation in harsh environments. Introduced by Epic Data Corp, 12728 15th Pl NE, Bellevue, WA 98005, the terminals read punched badges, ANSI cards, or magnetic striped cards, while the controllers handle up to 100 terminals on four separate party lines.

An 8080 microprocessor-based terminal which electro-optically reads punched badges, displays time of day, and provides five LEDs for prompting, the 1647-1 converts data to ASCII format for storage in a transmit buffer before subsequent transmission via a built-in RS-232-C interface and/or differential line driver interface. Model 1647-2 incorporates features of the -1 and adds the ability to accept data from both punched badges and 80-column ANSI cards. It also incorporates 20 user-defined keys for inputting variable data. Information such as time and keyboard entries are displayed on a 10-digit numeric display. Combining all features of the -1 and -2, the model -3 also provides 40 user-defined keys and up to 10 LEDs for prompting.

(Continued on p 46)

Important news for Intel SBC 80 users:

The RTI-1200 solves your real-time analog I/O subsystem problems.



Now Intel SBC 80 users have the most complete, most versatile and easiest-to-use input card for the acquisition and control of analog signals.

What you don't see here are all the other significant RTI-1200 features that enhance its maximum convenience and versatility. One of the most impressive is our User's Guide. It doesn't just tell you how to hook up jumpers. It does tell you how to write programs that optimize throughput rates, how to use the 8080's instruction set to take advantage of the RTI-1200's capabilities and a whole lot more.

If you're looking for the solution to your analog I/O interface problems, the Analog Devices' RTI-1200 is it. Single prices range from $629 to $979 depending on options (quantity discounts are available). The Analog Devices' RTI-1200, the first in a family of analog subsystems from the market leaders in analog products for signal conditioning, converting and control.

Send for the complete RTI-1200 Technical Information Package.

ANALOG DEVICES

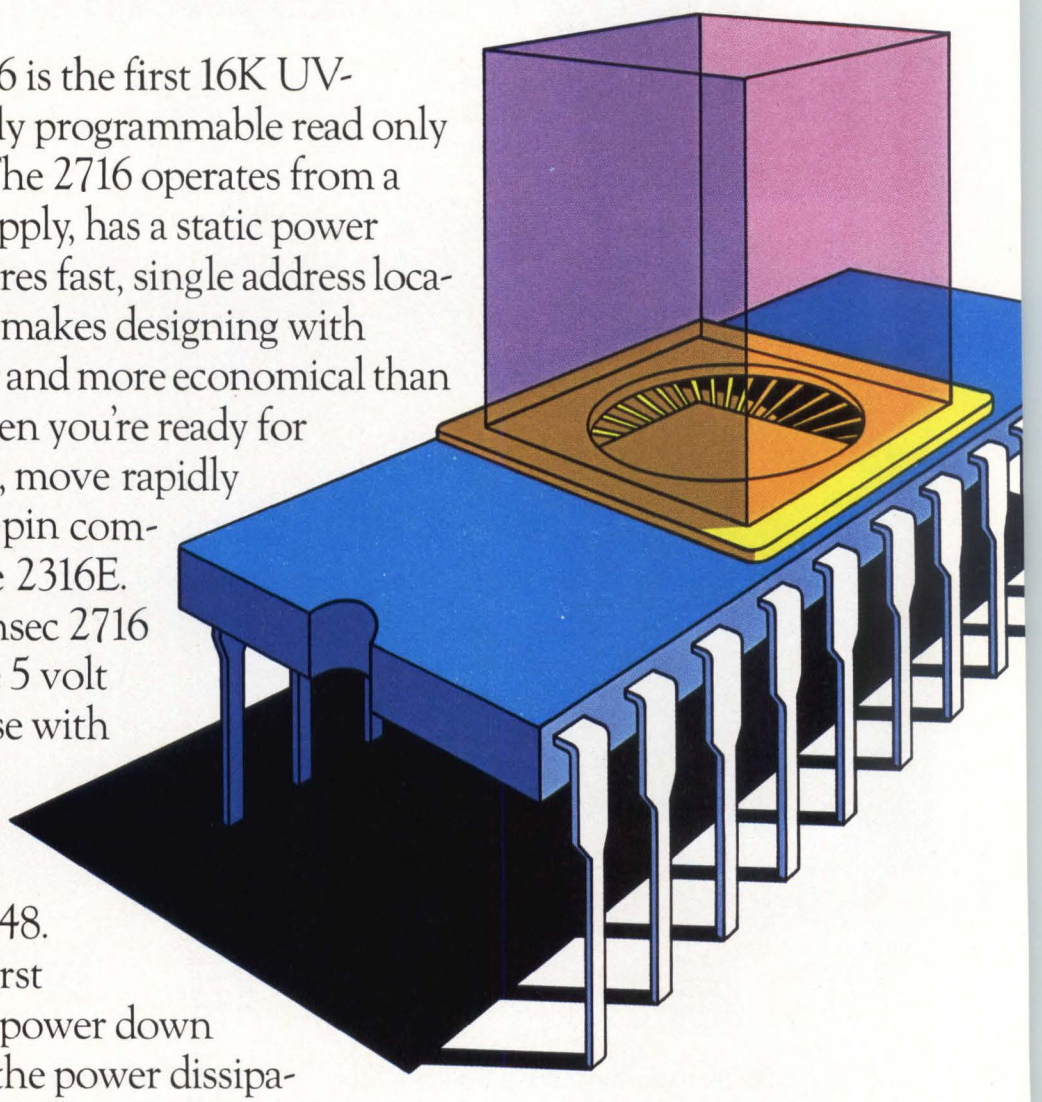
The real company in analog μperipherals

*Exclusive features of Analog Devices' RTI-1200.

Analog Devices, Inc., Box 280, Norwood, Massachusetts 02062 East Coast: (617) 329-4700, Midwest: (312) 894-3300, West Coast: (213) 595-1783, Texas: (214) 231-5094, Belgium: 031 38 27 07, Denmark: 02/84 58 00, England: 01/94 10 46 6, France: 686-77 60, Germany: 089/53 03 19, Japan: 03/26 36 82 6, Netherlands: 076 14 21 50, Switzerland: 022/319704 and representatives around the world.

CIRCLE 28 ON INQUIRY CARD

Intel delivers the first



The Intel® 2716 is the first 16K UV-erasable and electrically programmable read only memory (EPROM). The 2716 operates from a single 5 volt power supply, has a static power down mode and features fast, single address location programming. It makes designing with EPROMs faster, easier and more economical than ever before. Then, when you're ready for production quantities, move rapidly to Intel's new pin-for-pin compatible 16K ROM, the 2316E.

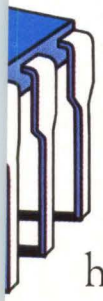
Since the 450 nsec 2716 operates from a single 5 volt supply it is ideal for use with the newer higher performance +5V microprocessors such as Intel's 8085 and 8048. The 2716 is also the first EPROM with a static power down mode which reduces the power dissipation without increasing access time. Active power dissipation is 525 mW while standby power is only 132 mW—a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs—single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Now you can program on-board, in the system, in the field. You can program any location at any time—either individually, sequentially or at random, with the 2716's single

5 volt 16K EPROM.

address location programming. Total programming time for all 16,384 bits is only 100 seconds.

The 2716 EPROM is pin compatible and directly interchangeable with Intel's new 420 nsec 2316E mask programmed ROM. Debug your systems using EPROM and when the pattern is firm, order the 2316E ROMs and plug them directly into the 2716 sockets. Turn around time on ROMs has been reduced to 6 weeks ARO. If you prefer, ship the first few products with 16K EPROM and switch to 16K ROM in the field. Either way you get the flexibility of EPROM and the economies of ROM. Both from Intel.



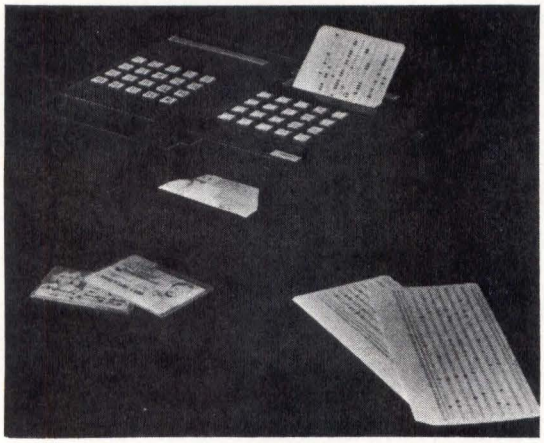
INTEL EPROM & INTERCHANGEABLE ROM FAMILY					
EPROM	Interchangeable ROM	Size	Organization	Power Supply	Max. Access Time
2716	2316E	16K	2K x 8	+5, only	450 nsec
2708	2308	8K	1K x 8	+12, ±5	450 nsec
1702A	1302	2K	256 x 8	+5, −9	1 μsec

Double the size of your program memory, improve performance, and get your product to market faster with Intel's reprogrammable 2716. And save money in production with the compatible high speed mask programmable 2316E ROM. The fastest way to get started is to order the new 2716 16K EPROM from your local Intel distributor. Contact: Almac/Stroum, Components Specialties, Cramer, Elmar, Hamilton/Avnet, Industrial Components, Liberty, Pioneer, Sheridan or L.A. Varah. And for quick turn around on the 16K mask programmable 2316E contact your local Intel sales office.

For technical information and a copy of "The New 16K EPROM" article reprint (AR-42) use the reader service card or write: Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.

intel® delivers.

Circle 29 for technical information.
Circle 30 for technical information and a demonstration.



Microprocessor-based data collection terminal reads punched badges or ANSI cards and allows variable data to be entered from the keyboard. The rugged unit from Epic Data provides operator prompting through user-defined LEDs, and stores ASCII coded data in RAM for subsequent transmission

For program storage the units have up to 2k bytes of ROM in 1k increments. 512 bytes of RAM allow data buffering during transmitting and receiving, and provide scratchpad memory. Architecture allows expansion to 16k bytes of ROM and up to 44k bytes of RAM.

System control units (SCUs) incorporate microcomputers which enable them to function as a flexible yet cost-effective method for controlling a network of terminals. They serve by polling each terminal to extract data being entered, analyzing received data to verify operation of the terminal, transmitting prompting information to lead terminal operators through data entry sequence, assembling received data into complete transactions, and transmitting data to a host processing system for analysis and report generation.

The model -1 can control up to 30 model 1647 terminals on one line. It incorporates 4k bytes of ROM or p/ROM (expandable to 16k), and uses 512 bytes of RAM for data buffering and scratchpad. The -2 has 8k ROM and accommodates from 4k to 44k bytes of RAM. It can control as many as 100 terminals on four separate party lines, and can assemble transactions and format data for simultaneous storage on one or two local storage devices.

Circle 149 on Inquiry Card

Low Priced Computer Stores Operating System in Main Memory

Model 20, an entry level member of the 1000 computer system family from Hewlett-Packard Co, 1501 Page Mill Rd, Palo Alto, CA 94304, is aimed at uses in manufacturing automation, automatic product testing, and multiterminal laboratory computing and control. Main distinction of the unit and primary reason for its low price is the multilingual, multiprogramming real-time executive operating system—RTE-M—which is implemented entirely within main memory.

Configured to include an HP 21MX-E series computer with 64k bytes of main semiconductor memory, a 2645A communications oriented CRT system console with two minicartridge drives, and a desk-style enclosure, the basic system operates under RTE-M, BASIC/1000M, and ISA FORTRAN. The operating system can be configured to manage main memory as large as 608k bytes, making the system useful where disc drives are inadmissible but where disc-sized capacity is needed, such as process control in harsh environments. Memory expansion is accomplished in 16k- or 32k-byte increments using plug-in boards.

The unit will support concurrent program execution and program development on four terminals or more, and will execute programs in BASIC, FORTRAN, or assembly language; its program development language is BASIC only. With an added flexible disc, it will handle any mixture of execution and program development at four stations or more, in any of the languages. Up to four flexible disc units can be added to provide up to 2M bytes of mass information storage. Flexible disc hardware is field retrofittable to systems. Drives have capacity for 512k bytes and are addressed by the same file manager calls as used by current real-time executive operating system software.

RTE-M, the memory resident real-time executive operating system, uses calls and file structures identical to those of RTE-II and RTE-III, making programs upward compatible. It also supports transfers to microcontrol store under program control. Expandable in modules, the system can implement memory mapping, enabling use with up to 608k bytes of memory.

Interconnection to local or remote process control equipment is accomplished through conventional screw terminal contacts on an available interface to the HP 9611R measurement and control station.

Circle 150 on Inquiry Card

Nonprocedural Language Simplifies Computer-User Communications

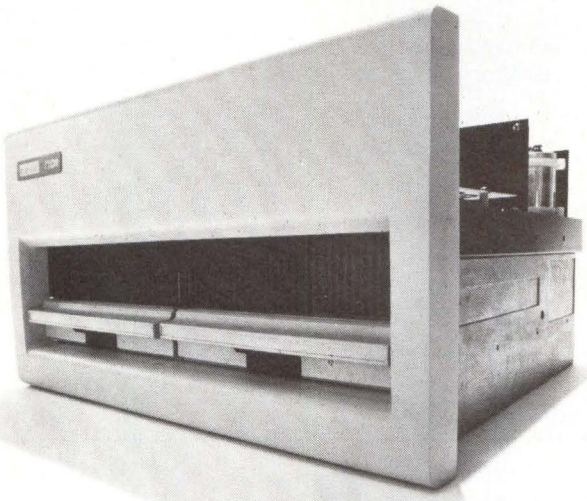
Integrating two separately evolving technologies—nonprocedural languages and data base management—the English-like RAMIS II (Rapid Access Management Information System) nonprocedural language simplifies communication between the user and computer by eliminating the need to translate to machine language. Users need not know how or where data are actually stored; the data storage structure can be changed without affecting existing applications.

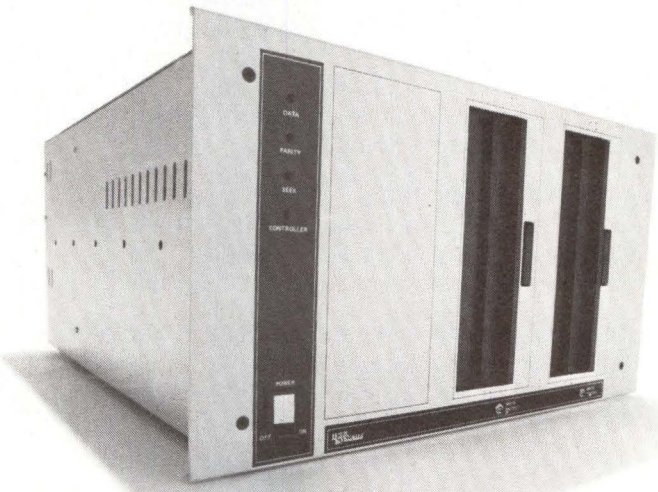
Evolved by Mathematica Products Group, Inc, PO Box 2392, 14 Washington Rd, Princeton, NJ 08540, the system runs on IBM System/360 and /370 with OS/VS, TSO, VM/370, and VP/CSS operating systems, providing security features, logging capabilities, and report formatting flexibility. Programs and routines can be developed without regard to access strategy, hardware limitations, or the storage structure of the data base. Access is automatic, but can be controlled at the user's option. Commands used in one environment are identical in all environments, minimizing the impact of different operating systems and devices on the user, and reducing problems in moving from one system to the next and

Now you have a choice of DEC®-compatible floppy disk systems.

The DEC RX01.
It costs $4,095.
You can wait months for it.

The DSD 210.
It costs $3,295.
You can have it in weeks.





YES	PDP®-8, PDP®-11, LSI-11 plug compatible	YES
YES	Software compatible with all DEC operating systems	YES
YES	IBM 3740 Format	YES
NO	Write protect switches	**YES**
YES	Automatic head unload	YES
YES	Ceramic read/write head	YES
YES	Holds 256,256 bytes per diskette	YES
NO	Diskette formatting capability	**YES**
1 OR 2	Drives per controller	**1, 2, OR 3**
NO	Interchangeable 50/60 Hz operation	**YES**
YES	Digital phase-lock-loop data separation circuit	YES
NO	Front panel activity LED lights	**YES**
NO	Front panel system status indicators	**YES**
PARTIAL	Modular construction	**COMPLETE**
MINIMAL	Self-testing microcode	**EXTENSIVE**
NO	Field-proven Shugart drives	**YES**

Our DSD 210 floppy disk system is 100% hardware, instruction set, and media compatible with all DEC PDP-8, PDP-11 and LSI-11 systems. It costs $800 less than DEC's RX01, has a far shorter delivery time, and has more useful features.

Data Systems

For an expanded comparison and complete technical details, phone or write Data Systems Design, Inc., 3130 Coronado Drive, Santa Clara, CA 95051, 408/249-9353.

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CIRCLE 31 ON INQUIRY CARD

Versatec challenges pen plotters to a "drawout."

Name your plot. Scientific graphics or business PERT charts. Maps or production drawings. Engineering simulations or circuit designs. Versatec will draw them faster, more reliably, and with far more expression than any other plotter.

Why wait minutes, even hours for pen plots? Versatec can produce a typical E-size drawing in less than sixty seconds.

Think what this speed could do for your own computer plotting. More throughput. Faster turnaround. Practical updates that give you visualizations now, not later.

Draw with more eloquence. High data density slows pen plotters to a crawl, but Versatec maintains constant speed. Produce subtle shading, toned patterns and variable line widths that are impractical, difficult, even impossible for pen plotters.

Print as you draw. Lettering is a problem for pen plotters, but not for Versatec. Display captions, legends and other alphanumeric data without losing a second. A simultaneous print/plot feature permits overlay of plot data and hardware generated print characters on the same scan line.

Enjoy troublefree plotting. Versatec electrostatics write without cranky mechanical arms and sputtering pens. No smears, skips or overshoots. Plot with fewer adjustments, less waste and less downtime.

Draw for less. With all these advantages, a Versatec electrostatic still costs about the same as a drum plotter system or about half as much as a comparable flatbed.

We've got you covered. Versatec has the paper width you need with formats of 22", 24", 36", 42" and 72". We've got controllers that link Versatec to all popular computers. We've got CalComp compatible software that gets you on-line quickly and easily.

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- ☐ Printer/plotters (Formats: 8½", 11", 20")
- ☐ Hard copy direct from CRT
- ☐ Versaplot software
- ☐ The 360/370 plotting system

Please send samples:

- ☐ Business graphics
- ☐ Computer aided design
- ☐ Mapping
- ☐ Scientific applications
- ☐ Production drawings

computer model and operating system

name telephone

organization

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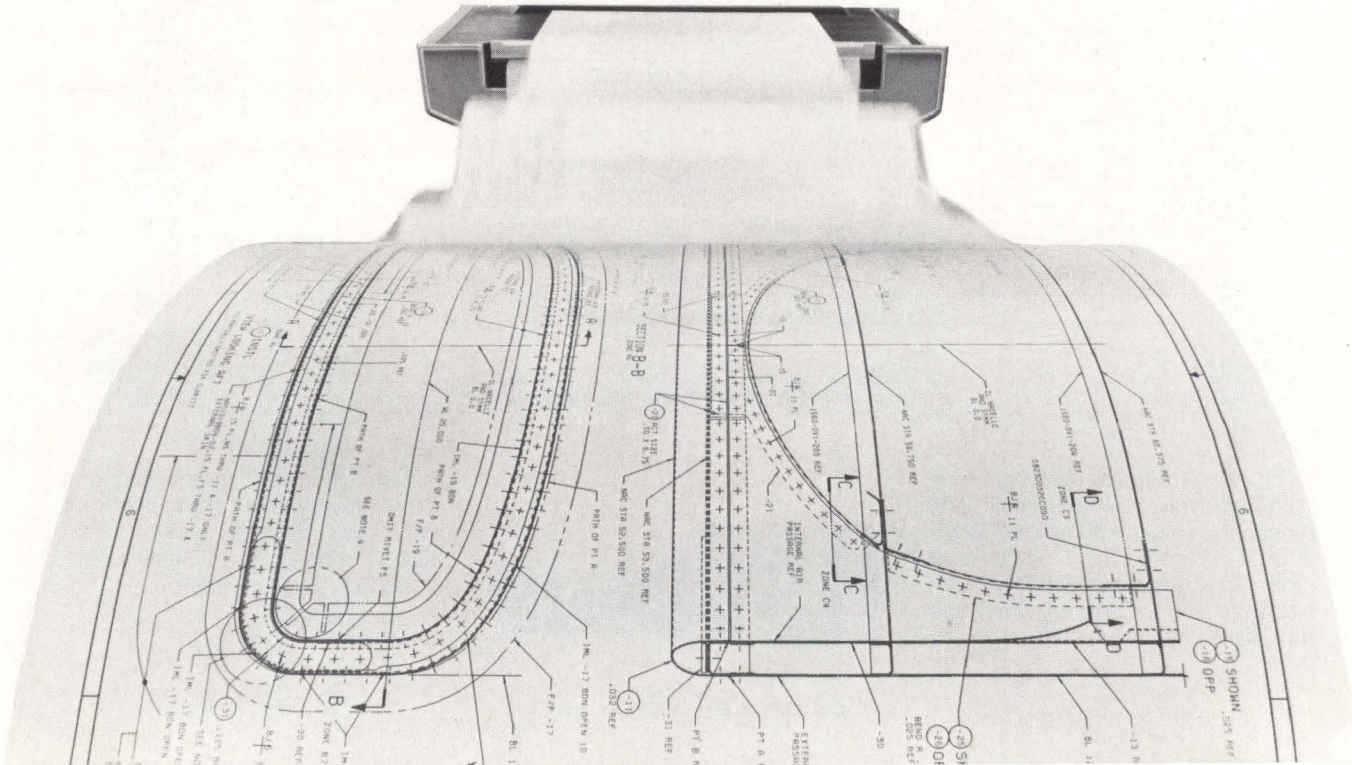
city, state and zip

Draw!

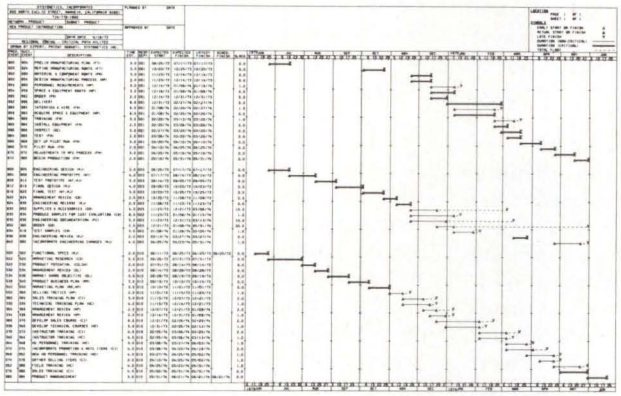


Versatec outdraws CalComp !

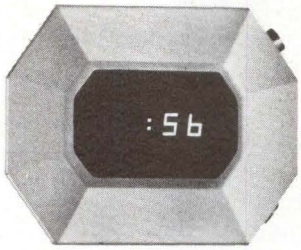
Plotting time

Versatec
Model 8136, operating off-line at half rated speed

CalComp™
Model 1036

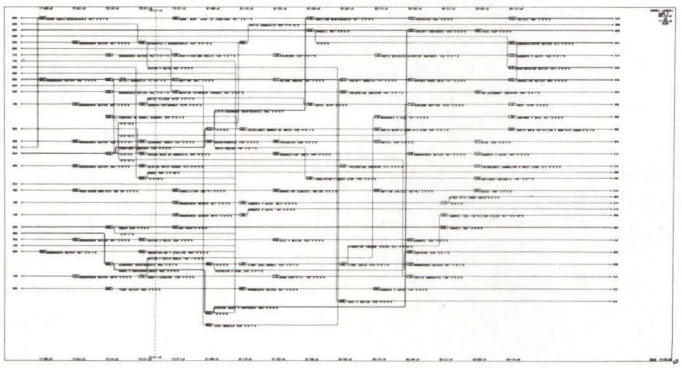


Plot size: 56" x 36" 33,000 vectors
CPU & I/O time for sort & rasterization:
9 seconds

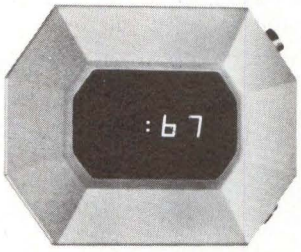


56 seconds

50 minutes

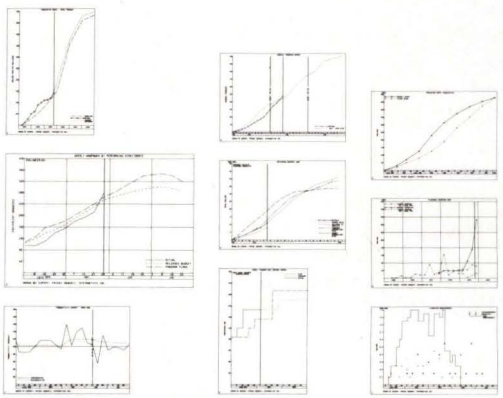


Plot size: 67" x 36" 16,000 vectors
CPU & I/O time for sort & rasterization:
8 seconds

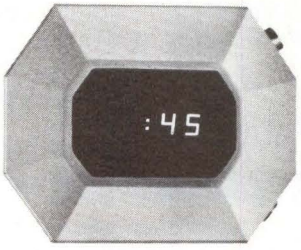


67 seconds

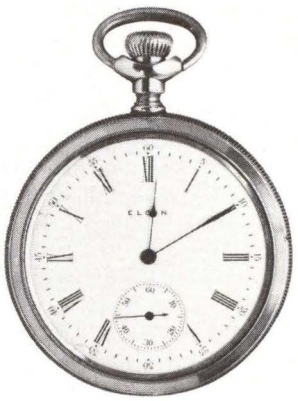
35 minutes



Plot size: 45" x 36" 15,000 vectors
CPU & I/O time for sort & rasterization:
6 seconds



45 seconds



10 minutes

Tests were performed with IBM 360/65 computer, OS/MVT operating system, EZPERT™ application software (Systonetics) and Versaplot™/Version 7 plotting software (Versatec). ™Trademarks: CalComp (California Computer Products), EZPERT (Systonetics), Versaplot (Versatec).

making the language easier to maintain.

System algorithms effectively utilize both static and dynamic storage for report preparation, records management, and network linking. Network linking can be controlled by specifying when files are to be linked and whether network pointers are to be recorded. This simplifies file reorganization by allowing pointers to be preserved throughout the reorganization procedure.

The type of direct access storage device on which the data base resides is automatically recognized by the system and is used according to its characteristics, assuring maximum efficiency for both online and batch systems. All system data base and data base management features are available for records management, report preparation, and the procedural language interface.

Syntax of the language is consistent with everyday English. Several formatting options can be indicated on one statement, both mathematical and relational operations are universally recognized, and character-string searches can determine which records do not match screening conditions. The only constraints in preparing output reports are hardware limitations such as insufficient memory or printer width.

Circle 151 on Inquiry Card

Voice Synthesizer Enables Computer to Tutor the Blind

A "talking computer" is being used to tutor the blind and visually handicapped in job skills in accounting and data processing. Called VOCAB, the project was made possible by a VOTRAX® voice synthesizer, developed by Vocal Interface, a div of Federal Screw Works, 500 Stephenson Hwy, Troy, MI 48084, which enables the computer to "speak," freeing the blind person from dependence on a reader. The project is being developed jointly by the Office of Research and Extension Services at North Carolina State University at Raleigh and the State of North Carolina, Dept of Human Resources, Div of Services for the Blind.

Students communicate with the instructional programs by means of a typewriter-like keyboard and receive messages from the computer-assisted program by synthesized voice response. Initially, four cassette tapes teach the student to use the keyboard and develop the typing skills necessary to communicate with the programs.

The student uses a telephone to contact the computer, and identify himself and the lesson he needs; the computer, by means of the voice synthesizer, reads a section of the lesson and asks the student a multiple choice question about the material. When the student responds by typing in the number of his answer, the computer transmits more information. Additional data is given to support correct answers and then new material is presented; if the answer is incorrect, supplementary information on the material is supplied and the question is asked again.

Circle 152 on Inquiry Card

Parallel Processors Operate as Standalone or Peripheral Units

Providing high performance, reliable, scientific computation for electrical and electronics engineering, research, and development, the EAI 2000 incorporates technological concepts that allow easy use and programming, facilitate digital connection, and improve user interaction with the problem. The parallel processor serves as a problem solving tool for designing analog and digital signal processing systems; developing filters, equalizers, oscillators, and adaptive circuits, investigating environmental requirements in electronic packaging, determining critical components or circuit tolerances; and designing and modeling circuit components.

Electronic Associates, Inc, West Long Branch, NJ 07764 designed the systems for use either as a digital computer or as an intelligent peripheral to a digital computer. Systems provide from 1.2M to 15M operations/s; the full set of mathematical computing blocks perform at repetitive speeds beyond 1000 solutions/s.

As a standalone mainframe parallel processor, the 2000 operates with I/O conducted through the associated alphanumeric terminal. This monitoring and control station (MACS), an integral part of every system, lets the user access the processor, improving user interactivity with the system for greater problem solving in less time with less effort. The system also includes a full complement of mathematical computing blocks which can be interconnected to model sets of higher mathematical equations.

As a peripheral, the 2000 is claimed to expand the capability of both systems by as much as 100 to 1 and to allow the user to do work not realistically possible with either system alone. Digital connection is accomplished through a built-in industry standard (RS-232 or CCITT) serial communications port; an optional parallel interface creates an independent path for high speed bi-directional data flow.

Circle 153 on Inquiry Card

Courses Emphasize Digital Signal Processing and Mini/Microcomputers

Two short courses which have been presented in several locations in Europe and the United States are scheduled to be held at the Marriott Motor Hotel, Dallas, Texas during June 1-8. "Digital Signal Processing: Fundamentals and Applications" (June 1-3) will be taught by Prof Alan V. Oppenheim, Dept of Electrical Engineering, MIT, Cambridge, Mass. Digital signal processing concepts form an integral part of systems in such areas as seismic data processing, communications, and speech and image processing. The course is designed to give an understanding of the fundamentals, applications, and future directions of the field.

"Microprocessors: Minicomputers/Microcomputers and their Applications" to be taught June 6-8 by Prof Hoo-min D. Toong, Dept of Electrical Engineering, MIT, provides a thorough understanding of minicomputers and microprocessors at all levels: software and hardware systems, and tradeoffs of successful applications. Intended for managers and engineers, it will use actual applications to illustrate techniques for utilizing mini/micro systems, as well as participant-supplied problems. Further information may be obtained from Digital Systems Associates, PO Box 295, MIT Branch, Cambridge, MA 02139.

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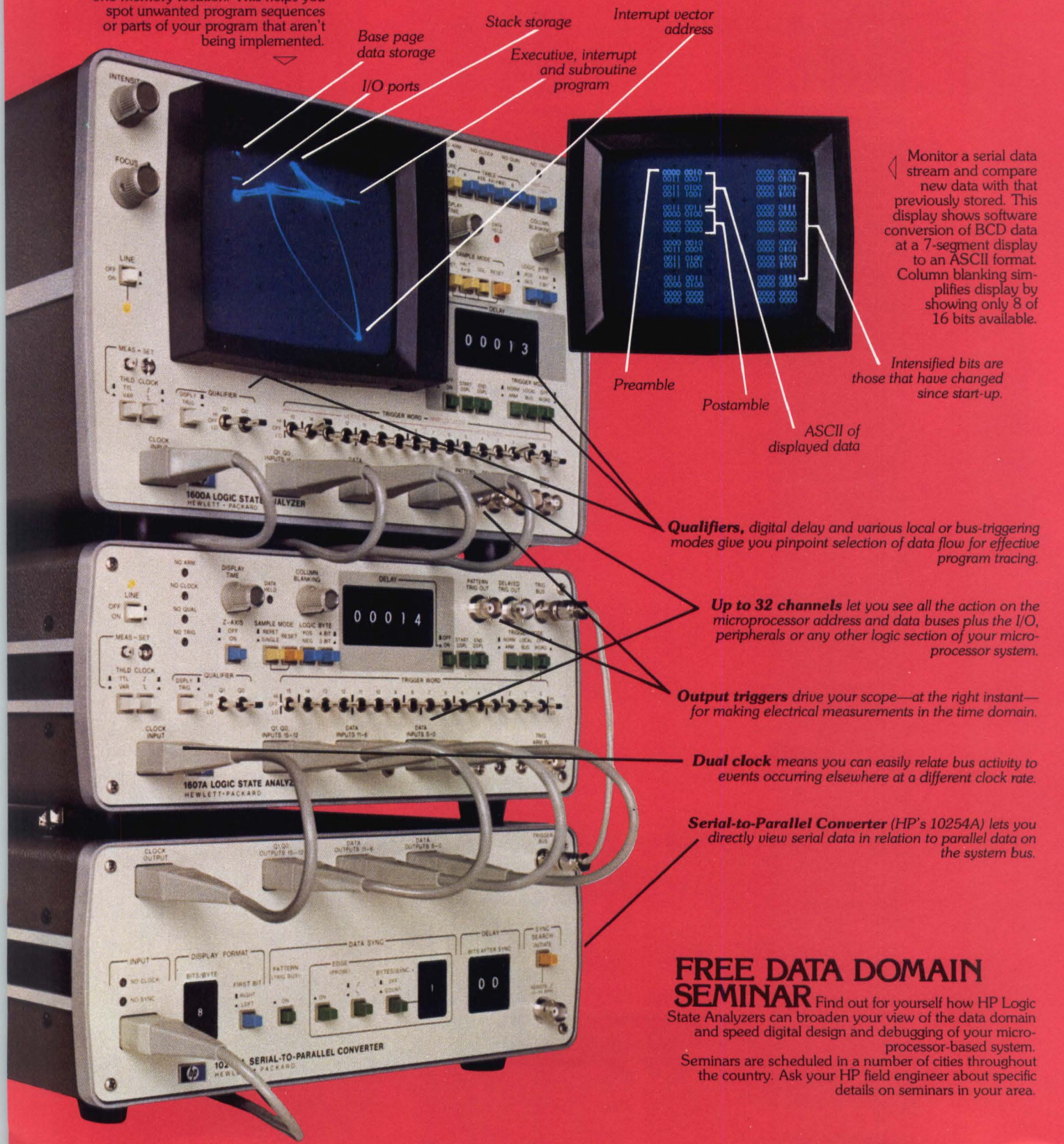
Designing microprocessor

Get a system overview with this memory map. The 1600S shows how your memory is being utilized in an operating program. Knowing how your memory is organized, you can see at a glance what your program is doing and the relative time being spent in any one memory location. This helps you spot unwanted program sequences or parts of your program that aren't being implemented.



Monitor a serial data stream and compare new data with that previously stored. This display shows software conversion of BCD data at a 7-segment display to an ASCII format. Column blanking simplifies display by showing only 8 of 16 bits available.

Qualifiers, *digital delay and various local or bus-triggering modes give you pinpoint selection of data flow for effective program tracing.*

Up to 32 channels *let you see all the action on the microprocessor address and data buses plus the I/O, peripherals or any other logic section of your microprocessor system.*

Output triggers *drive your scope—at the right instant—for making electrical measurements in the time domain.*

Dual clock *means you can easily relate bus activity to events occurring elsewhere at a different clock rate.*

Serial-to-Parallel Converter *(HP's 10254A) lets you directly view serial data in relation to parallel data on the system bus.*

FREE DATA DOMAIN SEMINAR

Find out for yourself how HP Logic State Analyzers can broaden your view of the data domain and speed digital design and debugging of your microprocessor-based system.
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based systems? You've discovered a new set of problems. Now discover HP's solutions.

HP's Logic State Analyzers give you a real-time view to help you spot and diagnose intermittent system operation. That can mean faster microprocessor system design and debugging.

The 1611A, priced at $5000*, can be tailored to either 6800 or 8080 microprocessors now. And more "Personality Modules" will be available soon. The 1611A lets you view bus activity and external events from the microprocessor's viewpoint. And, mnemonic decoding greatly simplifies interpretation.

The 1600S, with up to 32 input channels, dual clock capability and priced at $7100*, gives you a detailed real-time view of system activity from any vantage point, regardless of differences in clock rate. Add the 10254A Serial-to-Parallel Converter for $975* and you can simultaneously view serial data at peripherals.

One or more HP Logic State Analyzers give you greater insight for better understanding of your system's capabilities. That can mean earlier product introduction, lower development costs, a faster return on the development investment.

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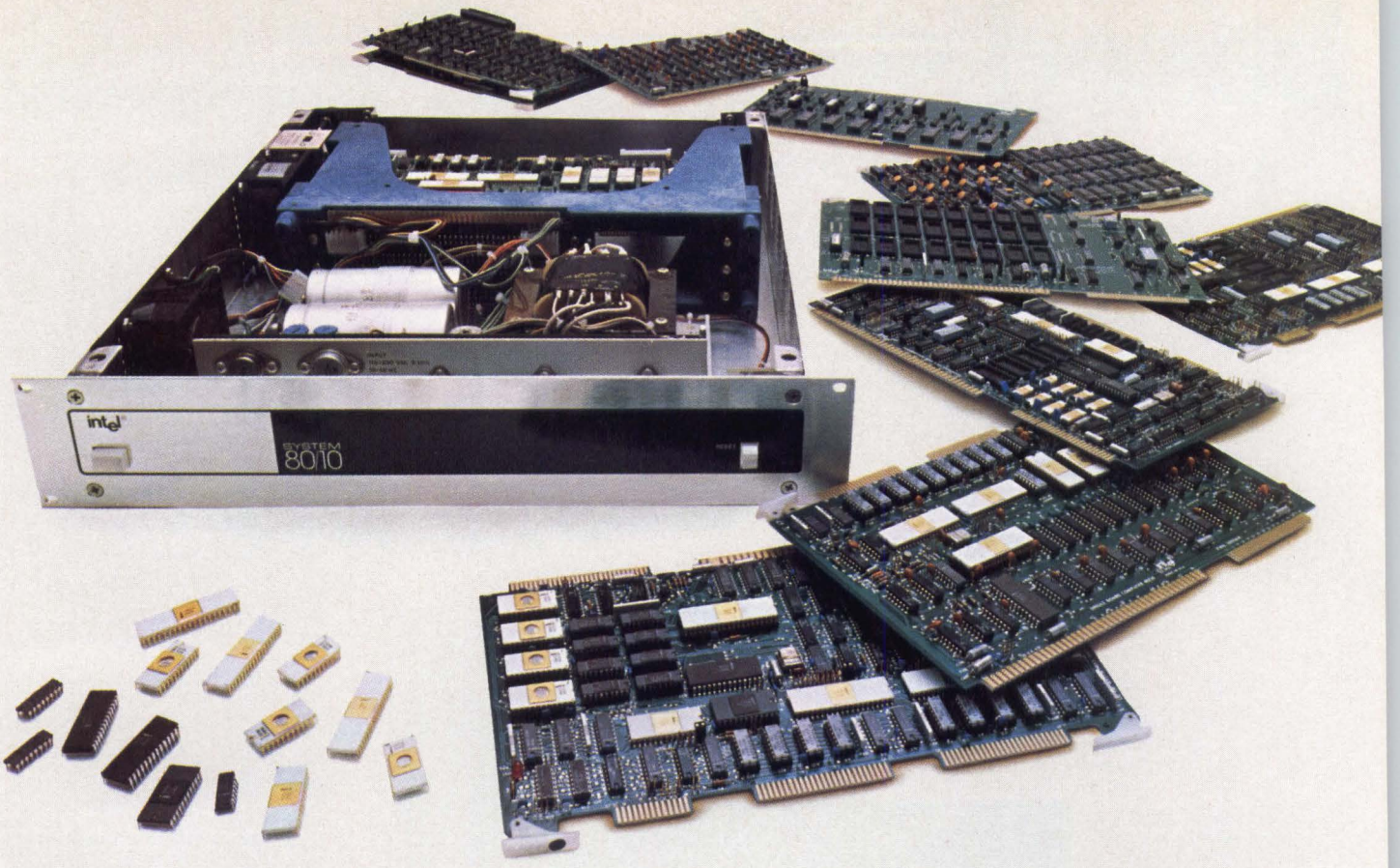
087/2

CIRCLE 34 ON INQUIRY CARD



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Circle 117 for technical information.
Circle 118 for technical information and a demonstration.

Medium-Scale Computer Emphasizes Need for Performance, Reliability

The medium-scale M-150 computer uses high performance LSI and MSI circuits, and incorporates high speed auxiliary storage, large volume files, communications control processors, and virtual storage features. Developed by Hitachi, Ltd, New Marunouchi Bldg, No. 5-1, 1-Chome, Marunouchi, Chiyoda-ku, Tokyo, Japan, the system provides online network, data base/data communications, and other capabilities.

System processor has up to 1M bytes of storage formed in 64k-, 128k-, or 256k-byte increments. Memory elements are 4k-bit n-MOS chips. Average instruction execution time is 8 ms. I/O transfers take place over byte and block multiplexer channels; total channel throughput is 4M bytes/s.

Peripheral equipment includes 100M-byte, 200M-byte, and 70M-byte disc drives which transfer at up to 885k bytes/s, as well as magnetic tape, line printers, and optical character recognition equipment. Software and I/O interfaces are compatible with other units in the series.

Circle 154 on Inquiry Card

Expanded Storage Extends Life of Xerox Computers

Expanded capabilities for Xerox computer users, announced by Honeywell Information Systems, PO Box 6000, Phoenix, AZ 85005, will both extend the life of the computers and assure users an orderly growth path and transition program. MOS memory subsystems for Sigma 6, 7, and 9; dual processor options for Sigma 6 and 7; virtual memory for Sigma 5; and removable disc storage and magnetic tape subsystems for Sigma and 500 series computers were included in the announcement.

A plug-compatible add-on alternative to the Sigma 9 core memory, the XPF 9850 MOS memory subsystem operates either with or as an alternative to the core system. Memory cycle time is 750 ns; capacities range from 128k to 512k. Two or 4-way interleaving is offered; however, core memory must be 4-way interleaved on mixed memories, requiring that core be configured in 64k increments only. The memory subsystem including a system controller, 128k words memory, and two ports will be available in third quarter 1977 at a price of $130,000. A similar unit for Sigma 6 and 7, model XPF 6850 includes an extended memory map, I/O processor upgrades, 128k word memory, and a memory interface unit. Price of this unit is $140,000; availability is planned for fourth quarter 1977.

Sharing common memory and I/O processors, the XPF 6851 dual processor option provides significant increases in computing power over single-processor Sigma 6 and 7. A single copy of Control Program-Five supports the configuration using one processor as the controlling unit and the other as the secondary or slave mode computing resource. The option will be available in fourth quarter 1977.

Model XPF 5850 virtual memory subsystem for the Sigma 5 is an architecture upgrade comprising memory management hardware, and from 32k to 128k words of Sigma core memory. Basic package, including 32k memory, is offered for purchase at $31,000; it is supported by the control program for real-time applications.

Magnetic media offerings are the XSP 9210 removable disc subsystem, which consists of microprogrammed mass storage processor and four disc units and provides formatted storage for 690M bytes; and the dual density 800- or 1600-bit/in magnetic tape subsystem model XTP 9310, which consists of magnetic tape processor and as many as 15 9-track tape units which operate using NRZI or PE.

Circle 155 on Inquiry Card

Low Cost Distributed Information Systems Offer Easy Start-Up

Distributed information systems 21/20 and 21/40, introduced by Mohawk Data Sciences Corp, 1599 Littleton Rd, Parsippany, NJ 07054, permit remote offices to perform customized data entry, application processing, and data communications. Basic configurations consist of an operator station with 1920-character CRT and keyboard, and a processor with one diskette drive.

System 21/20 is programmed for data entry and validation under control of user-supplied formats and is expandable to four operator stations. Fully programmable by the user via MOBOL (Mohawk Business Oriented Language), System 21/40 adapts to a range of distributed tasks, from extended data validation to full transaction processing from up to four terminals.

Users planning a distributed system can install a System 21/20 to replace keyboard devices at both local and remote locations. Addition of data validation routines programmed in MOBOL will add preprocessing power by upgrading the existing system to a 21/40; finally, transaction processing capabilities can be added at selected sites. Increasing work volumes are accommodated by expansion to four operator stations at each level.

A key factor in expandability is the 2-level software system. Formatted Data Entry Program (FDEP) enables users to convert existing data entry and media conversion formats from current equipment without procedural or programming changes. MOBOL language is a high level English-like language that is similar in structure and format to COBOL. Programs are supported by both a compiler and interpreter for rapid program generation. System software also provides media conversion, diskette labeling, and device control utility routines, and supports both BSC and SDLC communications protocols.

Circle 156 on Inquiry Card

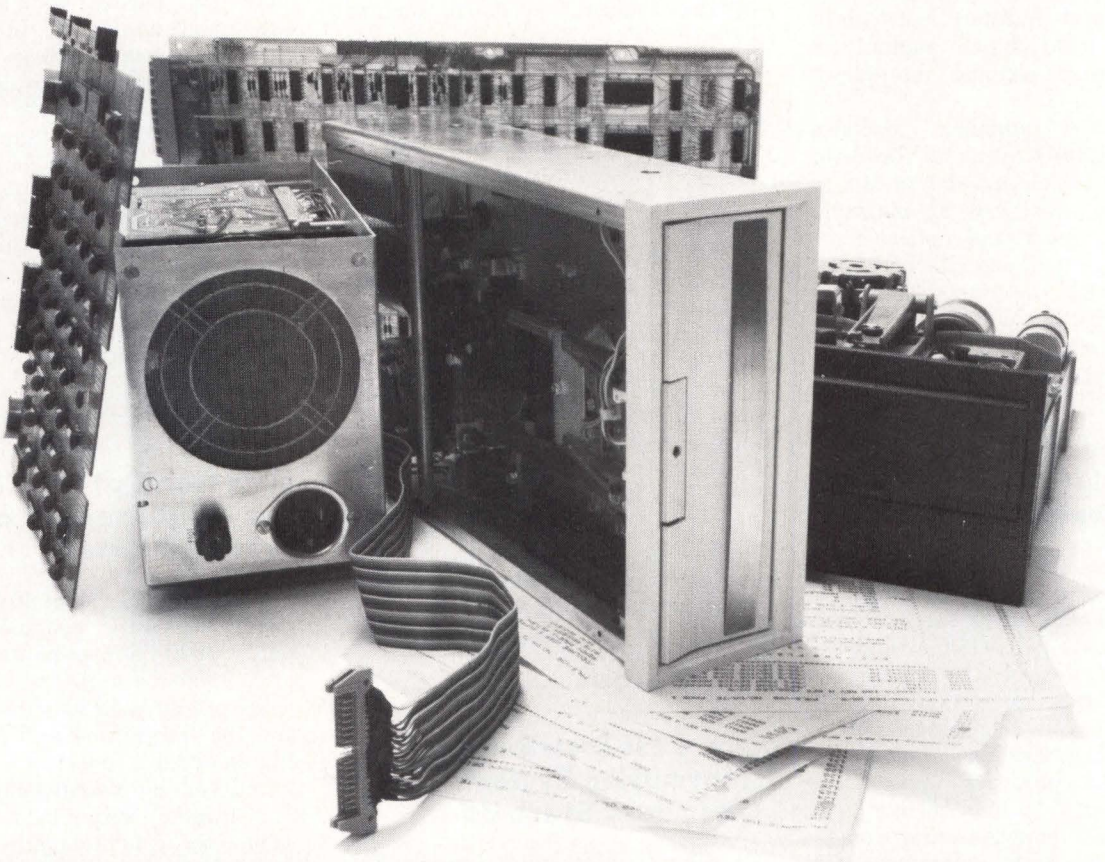
Emulator Option Allows Easy Replacement of Printer/Plotter

Emulator option model 40-340 allows users currently operating Gould series 5000 printer/plotters to replace them with the STATOS™ 4000 series printer/plotters without changing the software handler, application programs, interface, or cables. Introduced by Varian Graphics Div, 611 Hansen Way, Palo Alto, CA 94303, the emulator option supports the full speed capability of the printer/plotter in which it is installed.

Consisting of a single printed circuit board, which mounts in the printer/plotter's card cage and contains a combination of hardware additions and micro code changes, the emulator generates format control codes converted from the Gould discrete control line interface with hardware and uses the microcode changes to decode unique signals generated by the interface converter. □

Circle 157 on Inquiry Card

THEIR PARTS



An OEM flexible disk subsystem is more than the sum of its parts. Getting optimum performance at a low unit price requires design control to eliminate redundancy and volume production to reduce cost.

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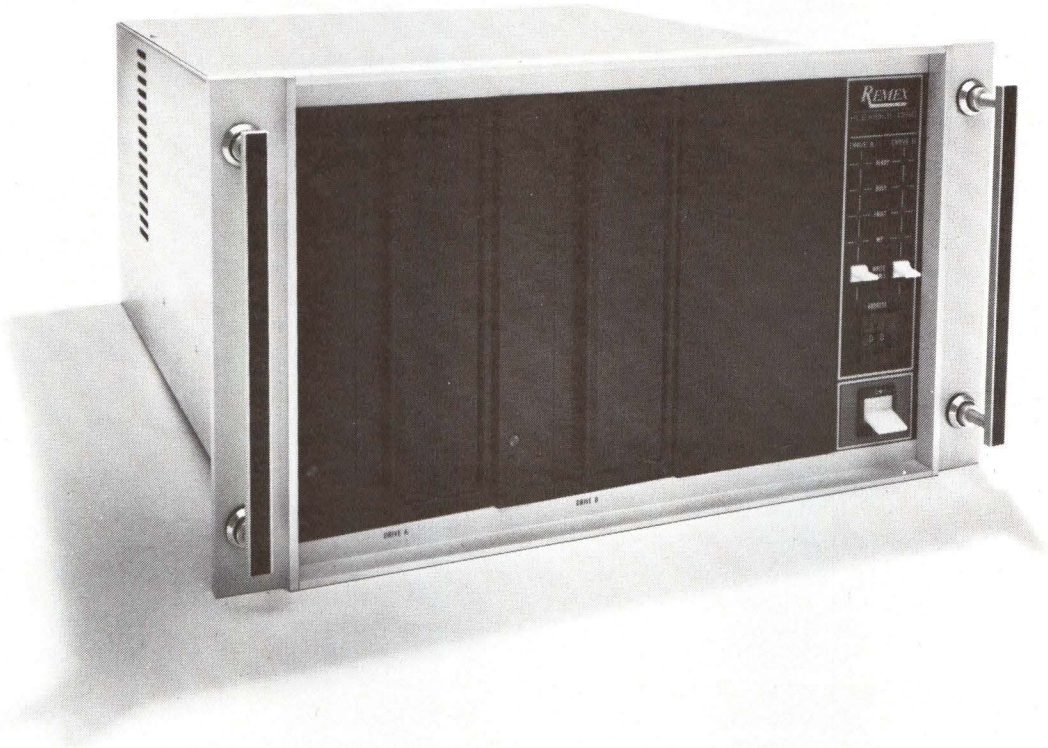
The RFS7500 is comprised of one to four RFD1000 Flexible Disk Drives, a microprocessor based controller/formatter, interface and software for most major minicomputers plus power supply cabling and rack mountable chassis. Because it is a fully integrated subsystem, the RFS7500:

☐ expands data capacity through implementation of IBM3740 format or a user selectable 1, 2, 4, 8, 16, 26 or 32

OUR PARTS



sector format. ☐ saves computer time by data block transfer of from one to 65K 2-byte words on a single command from the host. ☐ reduces core memory requirements due to automatic track and sector search and auto-initializing without software. ☐ simplifies operation and system integration by 8-command structure. ☐ saves space by housing interface card in the system chassis in some configurations. ☐ speeds access through 6 ms track to track speed plus unit select.

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CIRCLE 36 ON INQUIRY CARD

Automatic, Interactive Graphic Systems Maintain Pipeline Network Maps

Since the earliest time that man placed conduits underground to carry water for irrigation or to supply the various requirements of a city or village, there has been a problem in recording where those conduits were buried. Whether the conduits were pipe, tile, or hollowed logs, repairs eventually had to be made and the defective channels had to be located.

As likely as not—especially in past years—the location of each conduit was marked in someone's memory—probably the person who dug the channels and buried the conduit. Likely also, geographical markers were boulders, corners of buildings, or other objects that might be removed over a period of time. Rarely were accurate maps drawn that would allow the next generation of people to find the defective conduits without a great deal of digging and luck.

Often efforts were made to update maps but the projects were costly and time consuming. Records involving years of additions, replacements, and alterations had to be located, interpreted, and recorded on maps. Sometimes several changes might apply to the same conduit; determining what the present status was might be achieved only by digging holes and trenches.

Even in more recent times, when reasonably accurate and better defined maps were usually prepared, it became a major project to update those records every time conduits were replaced or repositioned or when systems were expanded. Forms were filled out and notes made but new maps might not be prepared except every few years or when old ones literally wore out. If a conduit broke or had to be located in an emergency, hours or even days—and many manhours of labor—might be expended before file records could be fully interpreted or the faulty channel found.

These not very efficient procedures might not cause much more than a serious nuisance for water supply systems. Hunting for a broken water main and not knowing exactly where to dig—or not knowing how to find the shut-off valve—might result in a few flooded basements and many wasted manhours of labor, but probably would not cost lives. In the case of a gas pipeline network, however, the situation is entirely different. Failure to find or know the exact location of a pipeline or valve could result in heavy property damage and serious injuries or even deaths.

Recently a number of organizations built up around pipeline networks have begun to update their maps. They often depend on aerial photography to set up basic maps with aboveground points on the networks as guides. Then the true locations and routings of all conduits are determined and recorded on the maps.

This, of course, results in sets of maps which are accurate—but only at the moment they are drawn. Any network changes result in either retrogression to a pile of addenda attached in file cabinets or the drawing of new maps. The first again results in the possibility of losing track of conduit locations; the second means sometimes prohibitive expenses.

Introduction of computer-automated management and control systems (*Computer Design*, Mar 1975, p 52) now appears to alleviate both of these problems. Such systems—built by Calma, 707 Kifer Rd, Sunnyvale, CA 94086—maintain complete files of information on every foot of conduit of all types—location, type, likely condition, inspection due date, predicted replacement—and automatically draw up-to-date maps including all data that are pertinent to the level of detail requested. They are applicable to the requirements of a number of different users.

Gas Distribution System

When Brooklyn Union Gas, which serves the New York City boroughs of Brooklyn and Queens, acquired the Staten Island territory in 1958, a major mapping problem developed. Schematics of pipeline routes were non-scaled and non-standard documentation had been used to describe and specify locations. Through the years the situation became too unwieldy—particularly as the piping system expanded.

Therefore, in 1973, Brooklyn Union initiated a complete and accurate pipeline inventory and mapping program. Raytheon Co was contracted for a 3-year period to prepare full maps based on aerial photography and a digital data base reconstruction of the pipeline.

Even this, however, brought about static presentations valid only at the moment they were drawn. As a result, work began in 1976 to tie in Calma Graphic Interactive (CGI) procedures and equipment with the Raytheon base material that would result in an automated mapping system.

Equipment includes a Data General Corp Eclipse™ S/200 minicomputer with 48k words of core memory, Century Data Systems 25M-byte model CD114 disc,

CIRCLE 37 ON INQUIRY CARD →

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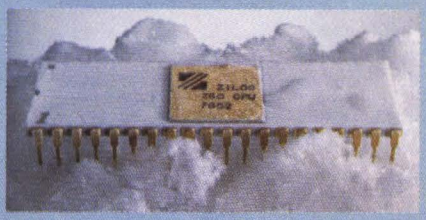
Deploy the Z80 peripheral devices:
Z80-PIO—Parallel I/O Interface Controller. Two (2) ports for fast I/O transfer under full interrupt control.

Z80-SIO—Serial I/O Interface Controller. Two (2) fully independent full duplex channels that can be programmed to operate in any asynchronous or synchronous modes including Bi-Sync and HDLC/SDLC.

Z80-CTC—Counter Timer Circuit. Four (4) independent channels that can be used to count external events or to generate interrupts at programmable intervals.

Z80-DMA—Direct Memory Access. Programmable circuit that transfers data between memory and peripheral devices at up to 1.2 megabytes per second. The DMA can operate in a transparent mode without slowing the CPU.

Deploy the Z80 software:
Resident Macro Assemblers. With cross-reference and conditional assembly, also relocatable assembler with linking loader.
PLZ Resident Compiler. Most powerful microcomputer compiler available today.
Text Editor and File Maintenance.
Basic Interpreter. For writing programs in Basic.
Cross Software. Available from NCSS.



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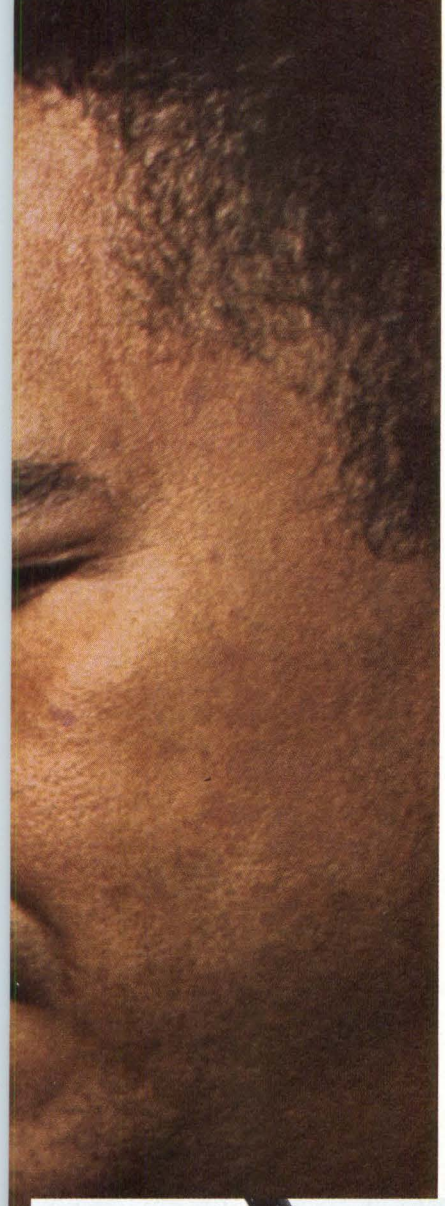

We designed them that way. Because a mass termination connector should help you save time and effort before, during and after assembly.

Their unique folded contact design, with dual camming and latching ears, assures you of four-point electrical contact and mechanical grip for each conductor. And that means superior overall reliability and protection. In addition, these fork-type contacts make it especially easy to visually inspect each termination before the cover is applied.

And even after the cover is on, each contact can still be visually checked for proper locking and latching. Because every AMP Latch cover has a built-in inspection port over each termination. This also permits electrical testing without cover removal, saving additional production time. And if repair ever is necessary, we've made that easier, too, by designing special hand and pen tools.

There are more reasons why you should choose AMP Latch connectors such as quick, easy terminating with the AMP shuttle tool, and the broad variety of pin headers and connectors. You also get AMP backup . . . expert design and production help that's yours for the asking from AMP connector engineers.

Why not contact Customer Service, at (717) 564-0100 for complete details on the AMP Latch connector line? Or write us direct. AMP Incorporated, Harrisburg, PA 17105.

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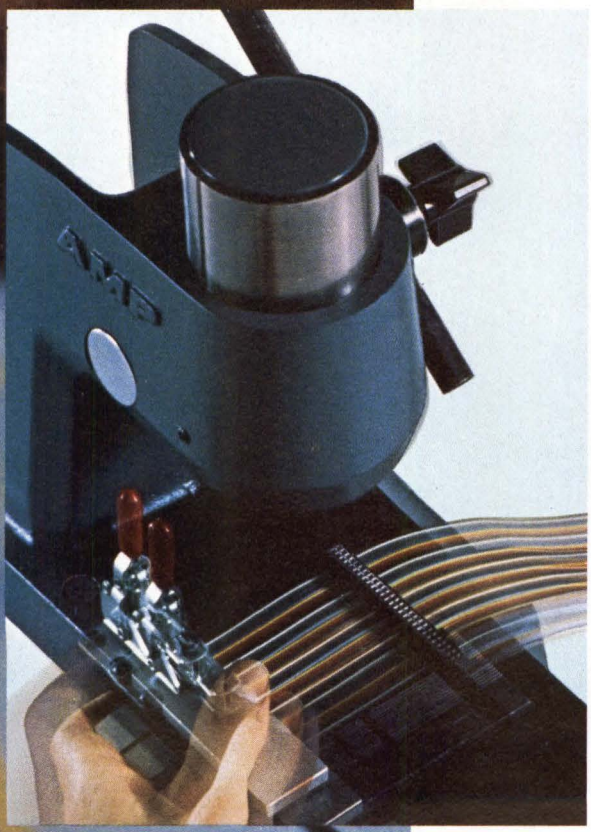

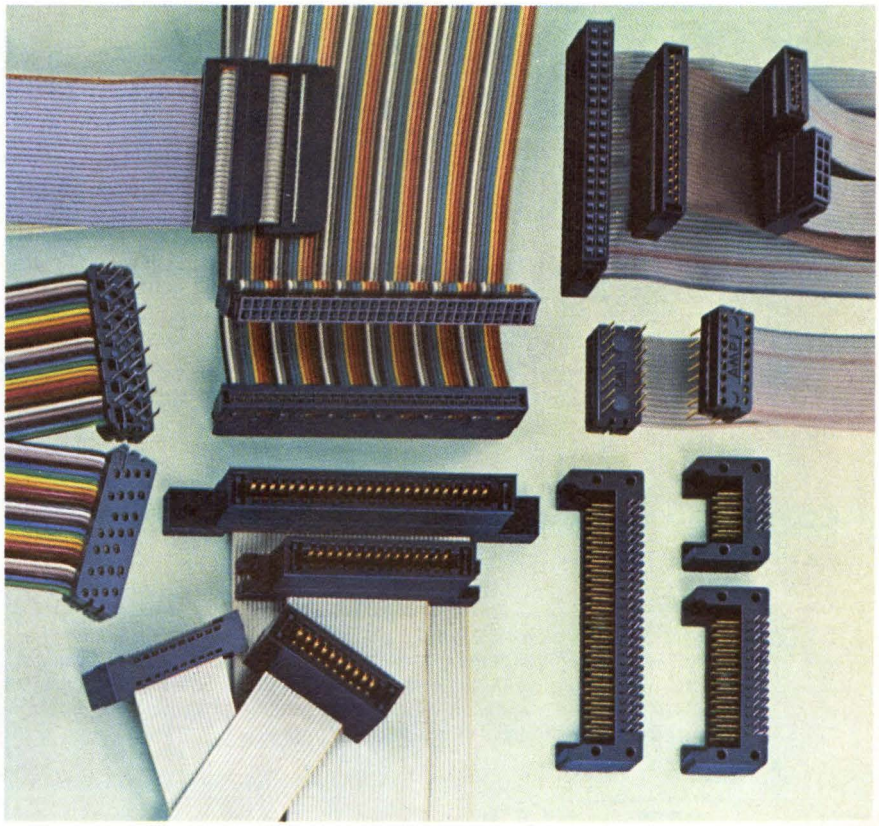

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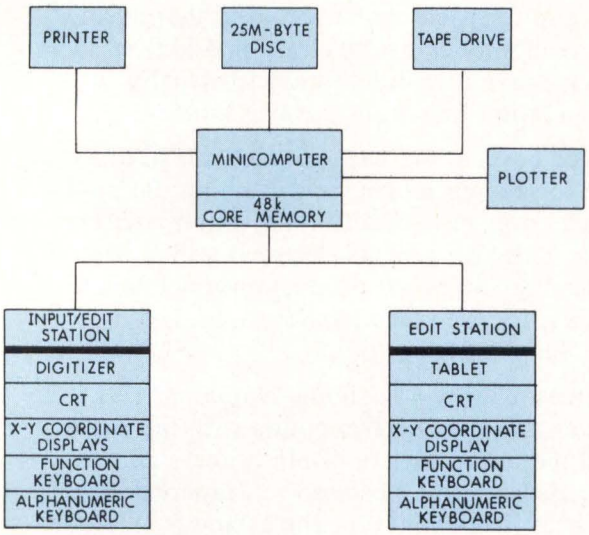
CIRCLE 38 ON INQUIRY CARD



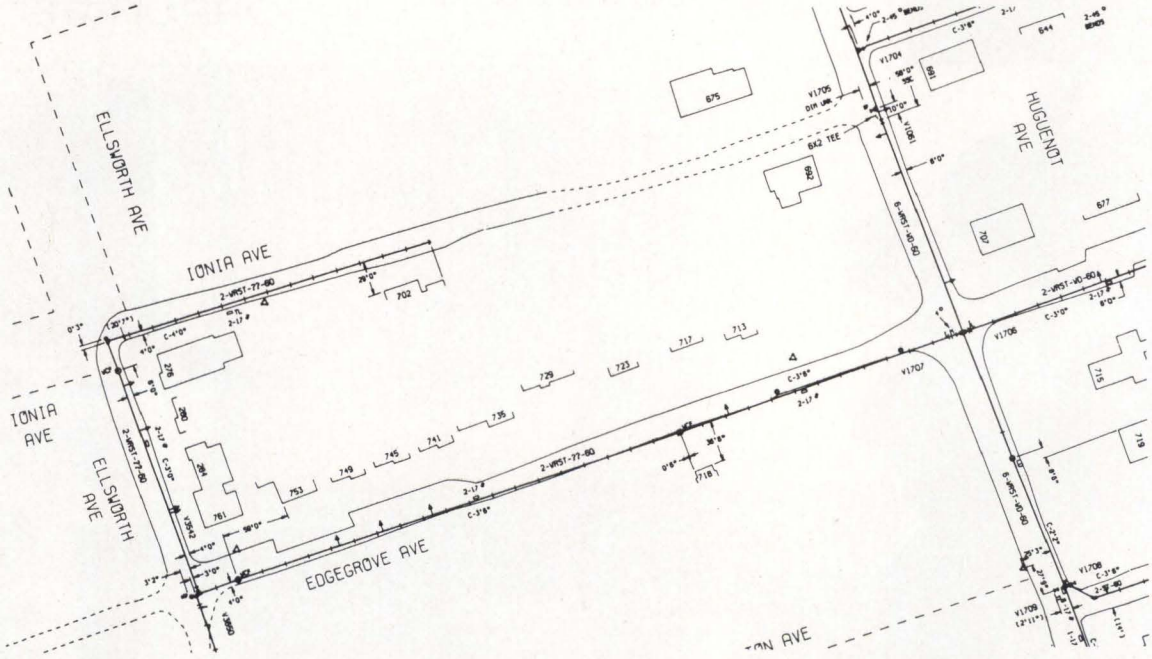
Calma Graphic Interactive (CGI) system used by Brooklyn Union Gas to automatically maintain maps of its Staten Island territory. Data General Eclipse S/200 minicomputer is controlling unit for system which digitizes information from workmen's sketches, stores and assimilates data, and draws up-to-date maps

Wangco tape drive, 48 x 60″ (121.9 x 152.4 cm) digitizing table, 11 x 11″ (27.9 x 27.9 cm) tablet editing station, California Computer Products model 960 high speed plotter with controller, DECwriter II printer, and two 19″ (48.3 cm) CRT terminals (one at each work station) with alphanumeric and 32-key function keyboards. To provide sufficient precision and avoid limitations, a 3-word format is used. This 48-bit floating-point configuration provides 32 bits of precision or 9.6 decimal bits. There are 32 bits to express the fraction and 16 bits for the exponent and sign.

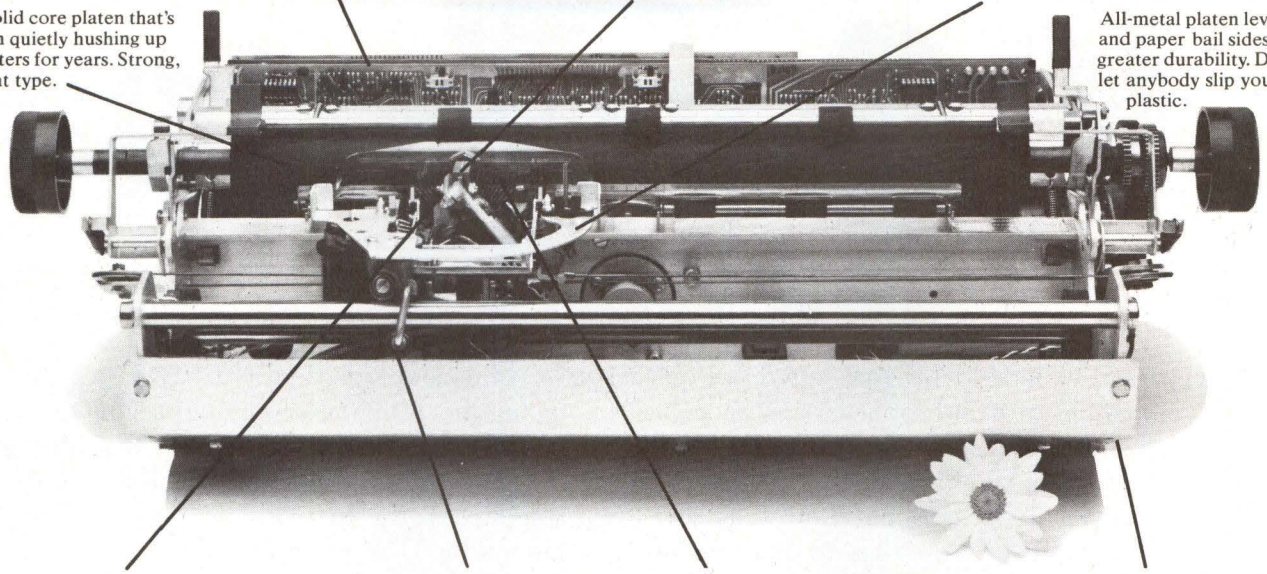
According to Calma, this configuration permits mapping of "any location on earth to within $\pm\frac{3}{32}$″ ($\pm$2.38 mm) and have the entire earth on the same coordinate system, and many smaller areas can be mapped to even higher accuracy." Even though that much precision is not required for this particular system, it is available for possible future use.

Rather than using 32 or 64 discrete levels for assigning descriptive data blocks for specific inspection or locations, the CGI system is designed around a tree structure. Data, therefore, can be partitioned into domains, each of which can be further subdivided into another level of domains. Up to 29 levels can be nested, with each level containing a virtually unlimited number of domains.

The data base will have geographic information on all gas company facilities including distribution network—pipes, valves, clamps, fittings, and textual data. In addition it will include all physical features visible in aerial photographs (curbs, manholes, hy-



Portion of typical CGI map showing gas pipelines, existing and planned streets, and frontages and/or full layouts of buildings. Code "6-WRST-WD-60" along Huguenot Ave indicates that pipeline there is 6″ mill wrap steel with welded joints and with normal pressure of 60. When pipeline is extended along planned streets such as incomplete section of Ionia Ave, information on all installations will be input from sketches for incorporation on new maps



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Call us old-fashioned.

Qume just believes continuity of product is everything. Savings in design, spares provisioning, training. So all Qume products are part of a continuing family. Not a designer-gone-berserk whim factory.

That's why the brand new 1976 Sprint Micro 3 pictured above is basically the same as the first Qume character printer we ever built. Each and every mechanical part is retrofittable, from the six-intensity hammer to the smooth-sailing carriage ball bearings.

So that any computer, terminal, or word processing system builder can buy Qume printers with the comforting knowledge that he'll face no printer-switching in midstream.

It's an interesting philosophy. (Made a big name for a small German car manufacturer a while back.)

And it's a sound philosophy we're committed to. Whether it's the industry's first true microprocessor-controlled character printer, our Sprint Micro 3. Or Qume's new WideTrack™—26 inches of bi-directional printing power.

All well and good, you might observe, but why buy Qume?

Because our unobsolescence philosophy is part of The Plan. A plan built on one simple rule: We don't compete with our customers. We don't make WP systems. We don't make terminals. We don't make computer systems. We have only one business—the printed word. And you get the best product we'll ever make.

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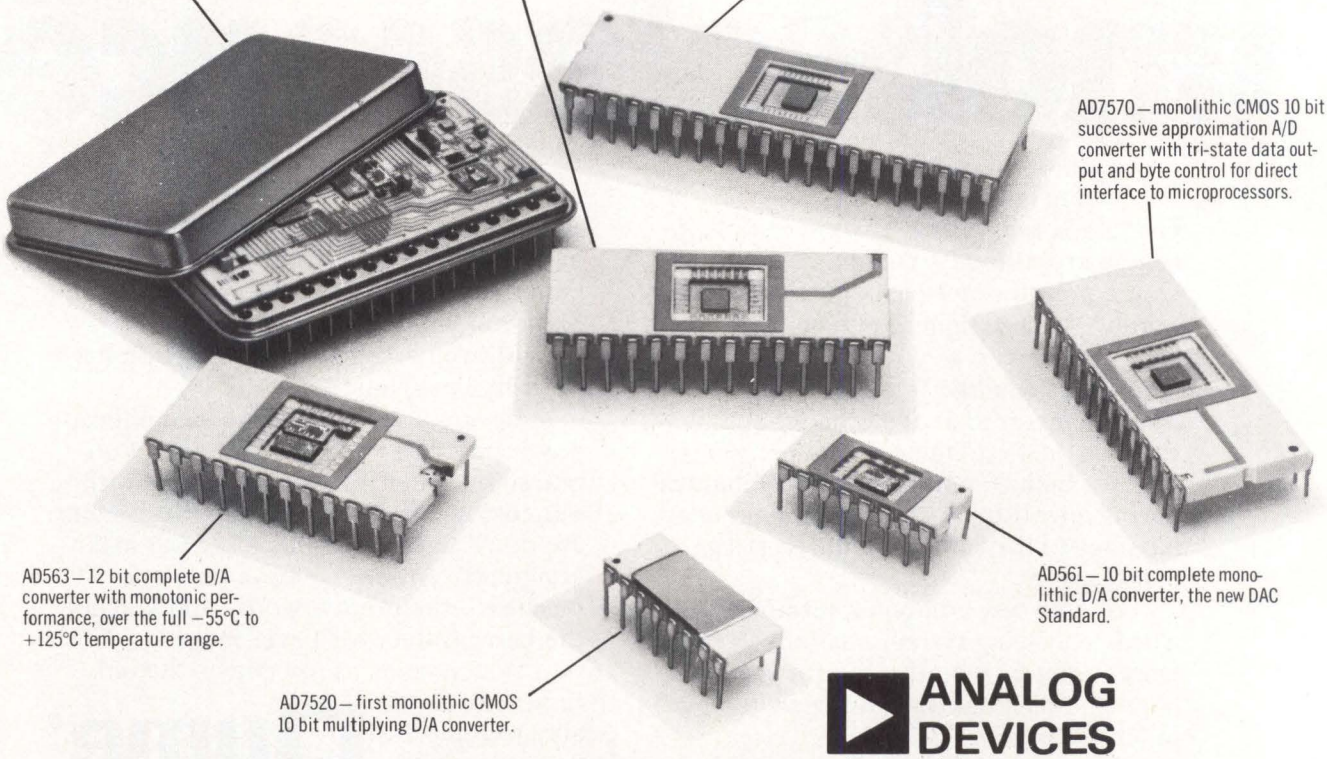
AD572—complete 12 bit successive approximation A/D converter can guarantee no missing codes over the full −55°C to +125°C temperature range.

AD7522—first monolithic CMOS 10 bit multiplying D/A converter with input buffer and holding register, allowing direct interface to microprocessors.

AD7550—13 bit monolithic CMOS integrating A/D converter using our revolutionary "Quad Slope" conversion technique for extremely high precision and stability. Tri-state data output and byte control for direct interface to microprocessors.



AD7570—monolithic CMOS 10 bit successive approximation A/D converter with tri-state data output and byte control for direct interface to microprocessors.

AD563—12 bit complete D/A converter with monotonic performance, over the full −55°C to +125°C temperature range.

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drants, house shapes or frontages, approved roads). It will also contain cartographic/cultural information such as house numbers, street names, and names of parks and cemeteries. This information is not available from photographs and not part of the gas company's facilities but valuable for identification. Once all data are converted and stored in the digital data base, the computer can recall any information needed.

As available maps are traced on the digitizing table, all data are automatically stored in memory. Numerical or text information can be added through the keyboard on a CRT terminal. Also, any section of the map can be altered by displaying it on the CRT display and ordering changes through either keyboard or light pen. Finished maps are drawn on the plotter.

When completed, the system will be able to generate a custom map of every 1000-ft^2 (90-m^2) area in the Staten Island service district—automatically—including up-to-date information, inexpensively and about four times faster than with other methods. A maintenance crew can determine exactly where a pipeline section is located and will know precisely where to dig to find a particular connection. In addition, the purchasing department will know when and what to order for portions of the network which must be replaced periodically.

Other available data will include the history of every pipe and fitting: manufacturer, material, and likelihood of problem based on the records of malfunctions that occurred in other pipe from the same batch. They will also provide a plan to show gas line peak load pressure if a particular tract were to be developed to maximum industrial potential, a perfected method of shutting down the system with minimum disruption of service in an emergency, and an economical method of meeting Federal corrosion inspection requirements.

The system will be able to assign diverse tasks such as draw all pipes of a certain size within a specific map section; compute the length of all such pipes within the section; draw only those pipes which are more than, for example, 20 years old and made of concrete, steel, cast iron, or some other material; display points at which pipes of different sizes meet; display all homes which would be affected if a rupture occurred at a certain point; and display the valve which should be closed to isolate that rupture.

Of particular interest is trace ability. For instance, if an operator wants to determine which part of a network is made up of a particular type of pipe, the system traces the entire network to locate and identify all sections using that kind of pipe. It will also be used in identifying cathodic protection section boundaries for corrosion control.

As additions or changes to the pipeline network occur, the information can be fed into the system daily either tabularly via keyboard or through the use of symbols on the CRTs. Types of fittings, certain forms, lengths of pipes, and other common or recurring items form a program "menu" that can be inserted by use of the cursor without the need to pencil plot or digitize data.

In practice, the draftsman first calls up a map page which brings to the screen a representation of a 1000-ft^2 (90-m^2) area. Using the cursor, the draftsman outlines the specific intersection where the work was done. That enlarged rectangle then appears on the screen and the draftsman keys in data on the keyboard or enters "menu" symbols via the cursor or a light pen.

When the draftsman inserts daily data from field documents or other sources, one change updates all maps and records. As data are entered, the computer verifies each bit of information by printing out confirming statements.

New maps containing fully revised data can be plotted at any time. However, in most cases, previously created maps are placed on the plotter and updated 10 to 15 times before being replaced.

Part of Brooklyn Union Gas mapping system. Input/edit station at left includes digitizing table and CRT display with function and alphanumeric keyboards; high speed plotter is shown at far right

(*Continued on p 70*)

Developed specifically to meet the increasingly stringent safety standards and regulations for electrical and electronic products, General Electric's LEXAN 940 resin provides a new level of performance in flame-retardant materials.

Based on a technological breakthrough, LEXAN 940 resin, both opaque or transparent, offers a UL 94 V-O* rating, an oxygen index of 35 and lower smoke emission. Yet, unlike ordinary flame-retardant plastics, it doesn't sacrifice processability. Melt strength, mold shrinkage and surface appearance are excellent. Forget streaked molded part surfaces.

What's more, new LEXAN 940 resin offers all the standard LEXAN resin properties, including lower finished part cost than metal, metal-like strengths, 110°C (with impact) UL continuous-use rating, high dielectric strength, clarity or molded-in color, and excellent dimensional stability, weatherability and gloss.

Best of all, it's been proven. For case histories and complete information, write: LEXAN Products Section 286, Plastics Division, General Electric Company, One Plastics Ave., Pittsfield, MA 01201.

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CIRCLE 41 ON INQUIRY CARD

Mostek breaks the 4K Static the most speed for the least

Mostek's new 4K × 1 static RAM is an important technology breakthrough in several areas—performance, circuit design and processing, reliability and ease-of-use. The 4104 is a static RAM yet it also offers the best characteristics of dynamic RAMs. Now, you can have the best of both worlds.

Features	Dynamic RAMs	Static RAMs	Mostek 4104
Density	X		X
Single power supply		X	X
Automatic standby	X		X
Low power dissipation	X		X
High performance speeds	X	X	X
Direct TTL compatibility		X	X
On chip latches	X		X
Minimal support circuitry		X	X
Battery back-up mode		X	X

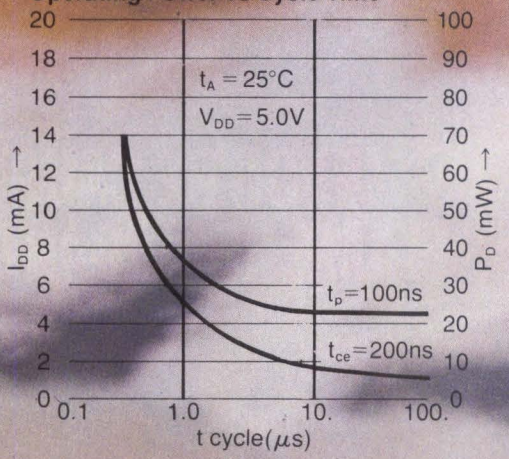
Industry's best speed/power product.

Mostek is introducing a complete family of 4K static RAMs. The high performance 4104-3 is rated at 200 ns access time, 310 ns cycle time, 165 mW active power dissipation and 27 mW standby power. All ratings are max. Other speed/power product ratings are available in the 4104 family to match your particular application requirements.

There's no sacrifice in system performance with the 4104. It's directly TTL-compatible with an input "one" level of 2.0 volts and a "zero" level of 0.8 volts. And the output will drive 4 TTL loads in addition to 100pf. The 4404, a 1K × 4 version that's ideal for microprocessor applications, will be introduced soon.

Automatic standby power, a feature you expect only in dynamic RAMs is now available in Mostek's new static RAM. This is achieved by forcing Chip Enable to an inactive state, thereby reducing standby power to just 27 mW max. An even further reduction of standby power occurs when the V_{cc} power supply is reduced.

Operating Power vs Cycle Time



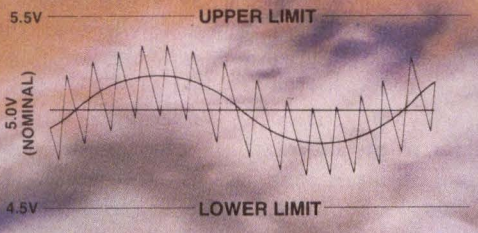
RAM technology barrier-power in the industry.

With this mode of operation, data retention is maintained at less than 0.3 μW/bit (typ.), allowing a true battery back-up static RAM system.

The 4104 represents a major breakthrough in memory design. With a 2.7 square mil cell size, Mostek's design reduces conventional chip area by 40%.

Easy to use with 5V-only supply.

The 5V power supply has a tolerance of ±10%, further increasing design flexibility. The 4104 is packaged in the industry-standard 18-pin configuration providing a compact board layout. With this pin-out, two-layer rather than four-layer printed circuit boards can be used for faster design cycles and reduced costs.



At Mostek, Power Supply Tolerance means that any combination of nominal DC level, low frequency ripple, and high frequency noise is acceptable so long as the sum of all noise does not go outside the specified plus and minus (±) envelope.

Now you can take advantage of the best features of both static and dynamic RAMS in one—the 4104.

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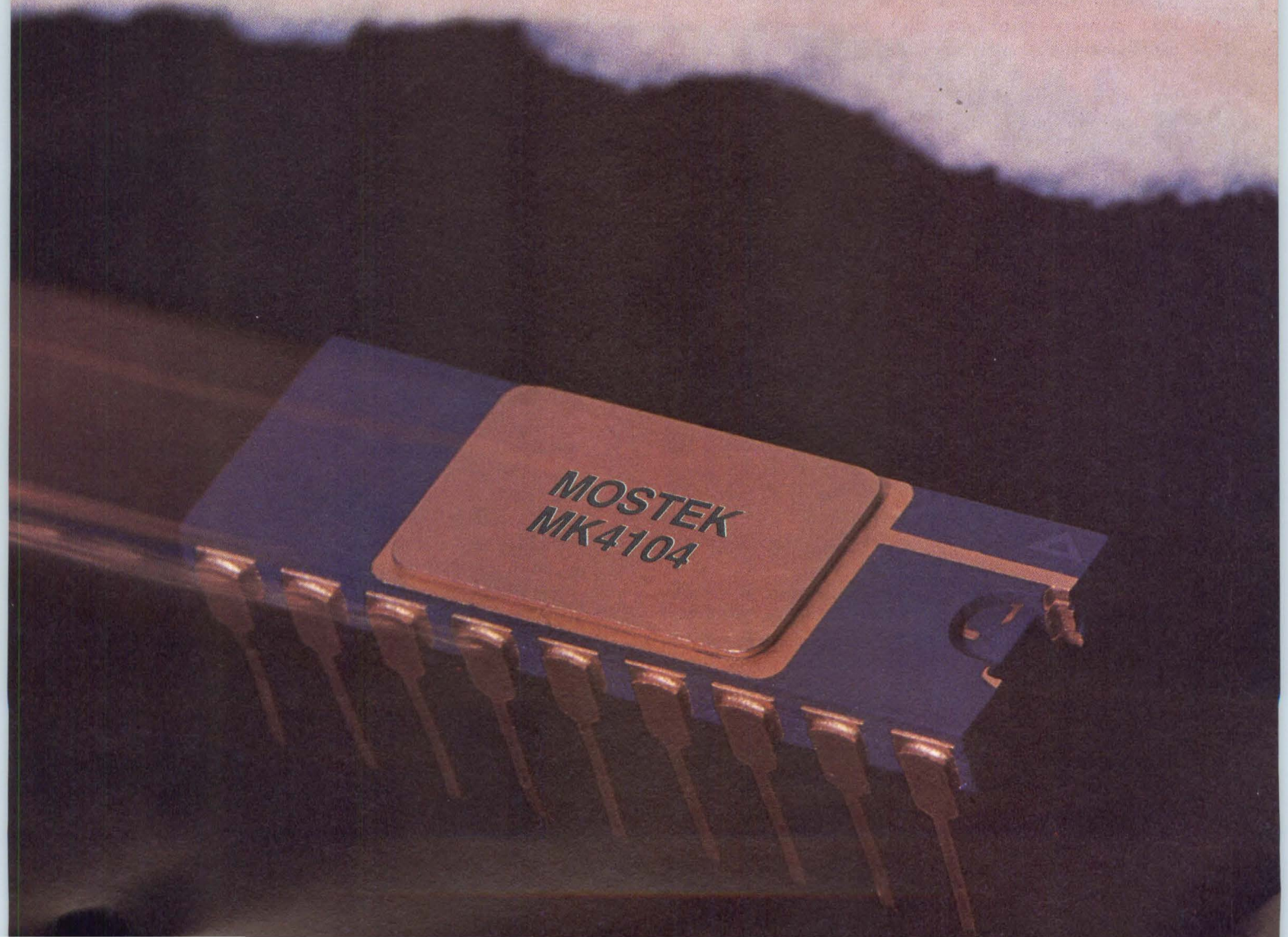


In one area alone—the digging of holes to locate damaged pipes—the mapping system offers large monetary savings. Each excavation costs about $300, and 40,000 such holes are currently being dug. Knowing just where to dig will result in far fewer excavations.

During 1977, Brooklyn Union will begin network analyses based on its prepared data base and will be able to run experiments and tests on hypothetical networks—and make alterations—before building them. Further advantages are expected in corrosion control programs, valve and regulator maintenance, emergency planning procedures, and tax and rate planning. However, a major possible opportunity lies far in the future: joint data banks operated by several utilities and government agencies so that each would know where all buried networks were located. This would eliminate much of the damage that now occurs from digging by crews of other agencies and would minimize repetitive digging and street repair.

Gas/Electric Utility

Another similar interactive, automated mapping system is in use by a major Western U.S. utility. The program models pressure and flow characteristics of sections of a gas distribution system. Analyses help solve existing low pressure problems and locate potential such areas as new customers are added.

A dedicated minicomputer—Data General Nova 2 with 32k words of memory—is included but there is also an interface to an IBM System/370. At present, a load profile based on peaks at various node points is being set up. Interfacing to the /370 memory enables automatic data collection and modification of drawings to include actual valves next to each node.

Then a range of street addresses is assigned to each node and another program assigns customers to nodes according to service address. Data on each customer's actual consumption is used to calculate peak load for that customer.

As in the Brooklyn Union system, automated mapping is a key feature. When various new area developers supply their maps, information from each is digitized automatically—no matter what scale was used by the original draftsman. As change reports are received, that information is also digitized. Then "as-built" drawings are automatically plotted. Source documents are 4 x 8 ft (1.22 x 2.44 m) wall maps that show locations of gas mains.

Predictions for the system include annual detailed analyses of 18% of the total pipeline network—opposed to 7% attainable in the past. It is also expected to reduce drafting manhours to a quarter of what has been spent.

Tax Maps

Another application of Calma's automated system is in maintaining current maps of cities or counties for tax assessment purposes. Often, such maps are as much as 10 years out of date.

Some counties in New York State and in Alabama are using the services of the Aero Service Div of Western Geophysical Co of America to maintain up-to-date maps based on aerial photography and the graphic interactive system. Under control of Data General Nova 2 or Eclipse S/200 minicomputers—with 32k or 48k words of memory, respectively—correction data are reduced to digital form. An operator moves a reticle over the manuscript or aerial photograph to indicate locations and shapes. Results are displayed on a CRT and then entered in memory when the operator is satisfied with the display.

Computer commands are entered in abbreviated English via keyboard or from a graphic "menu" on a digitizer table. Map scale, orientation, or sectioning can be selected or changed on command.

Use of this system eliminates the need for much of the manual work. Property lines and other information that make up 10 different overlays are maintained in computer memory. Each overlay can be plotted separately or all can be combined. All steps between digitizing of photos and plotting of maps are eliminated or automated.

Circle 160 on Inquiry Card

DC&AS BRIEFS

Computer Irrigates Remote Fields Automatically

Schedules determined and controlled by computer automatically trigger field irrigation units in a system developed and manufactured by Motorola Israel, Ltd, Tel Aviv, Israel, a subsidiary of Motorola Inc. Water, energy, and manpower can be conserved while cultivated land area and crop yields can be increased as a result.

Originally designed for border settlements to enable farmers to irrigate crops without walking in fields which had been mined in wartime, the MIR 1000 is equally applicable for peacetime use in remote farmlands which might not be regularly visited. It can be used for both sprinkler and drip irrigation networks and is designed for farms larger than 100 hectares (40 acres), up to 2000 hectares (800 acres) or even larger.

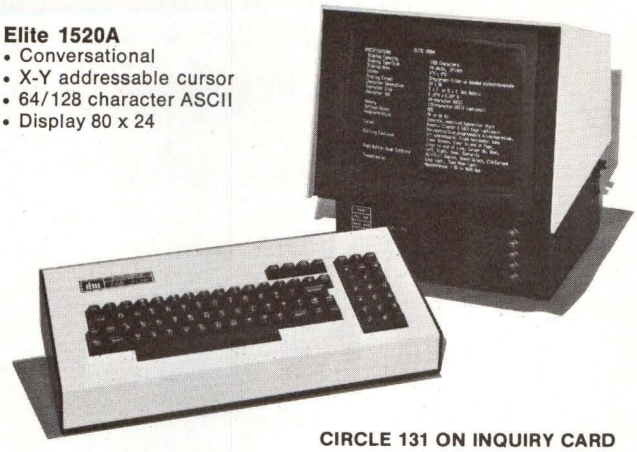
A basic system comprises a master control station and several field units located close to the irrigation network and control valves. Interconnection is ordinarily via a single 3-wire cable which carries both signals and power. When required for difficult to reach areas, field unit operating power can be supplied by small batteries and commands can be transmitted by radio.

(Continued on p 73)

See things your way

Elite 1500A
- Conversational
- Roll up
- 64 character ASCII
- Modular display (32 x 8 to 80 x 24)

CIRCLE 130 ON INQUIRY CARD



Elite 1520A
- Conversational
- X-Y addressable cursor
- 64/128 character ASCII
- Display 80 x 24

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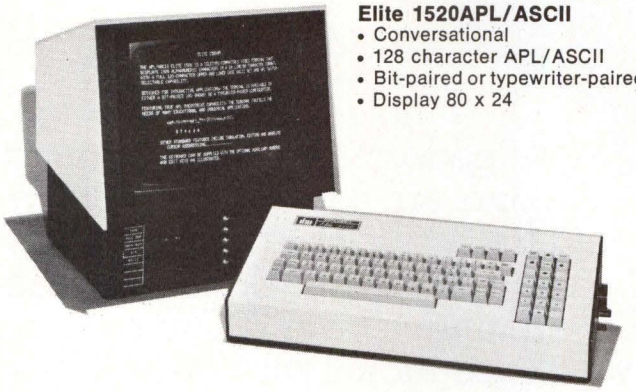
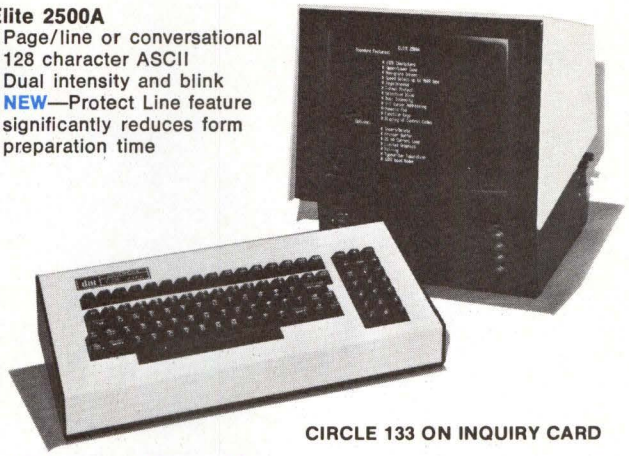


Elite 1520APL/ASCII
- Conversational
- 128 character APL/ASCII
- Bit-paired or typewriter-paired
- Display 80 x 24

CIRCLE 132 ON INQUIRY CARD



Elite 2500A
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- 128 character ASCII
- Dual intensity and blink
- **NEW**—Protect Line feature significantly reduces form preparation time

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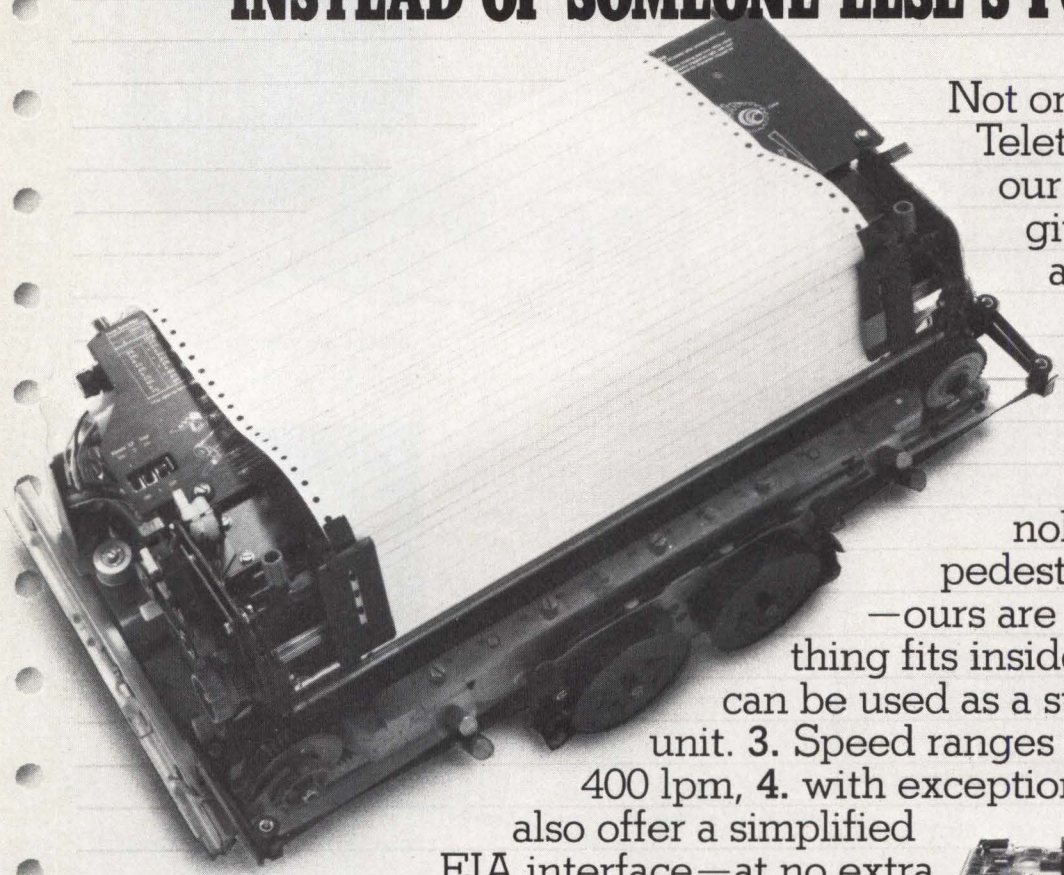

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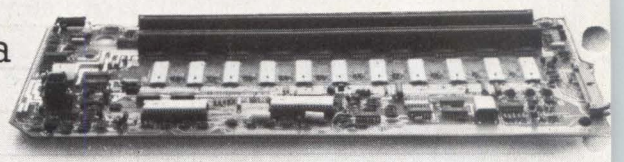

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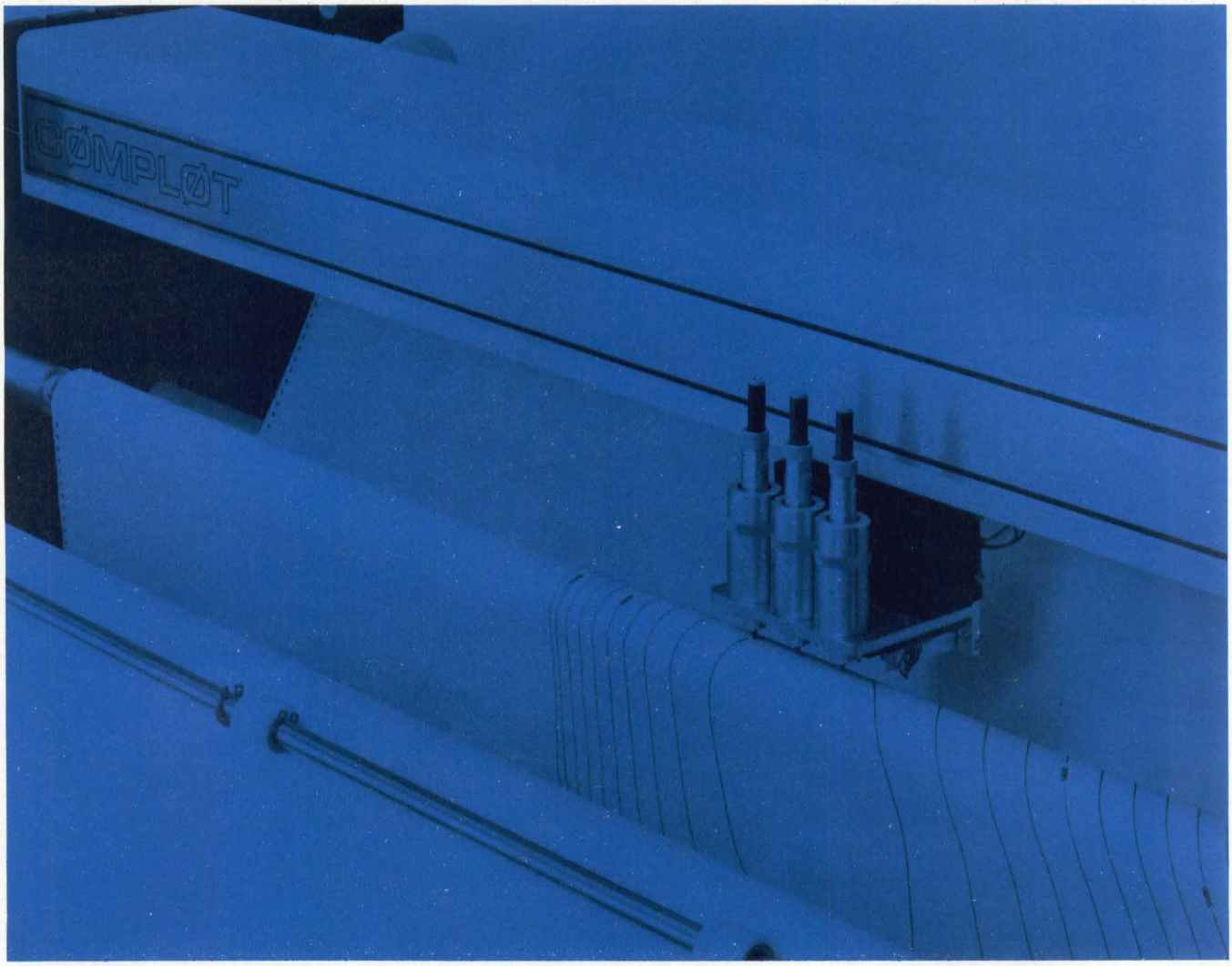

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Examination of lower cost, moderate-to-high performance solutions to the problem of implementing multiplication in microprocessors, rather than expensive, hardware intensive, all-parallel approaches, gives designers the facts necessary to make tradeoffs and achieve desired performance economically

Hardware Multiplication Techniques for Microprocessor Systems

Bala Parasuraman

Syscom, Incorporated
Santa Clara, California

High speed multiplication is not included in the instruction sets of presently available microprocessors, except in microprogrammable bipolar devices. Nevertheless, users may need it when they discover further applications for their microprocessor-based systems, or undertake system designs that grow out of existing designs. When this happens they are obliged either to write a program subroutine for multiplication, which is invariably slow, or to design a multiplication unit in add-on hardware. Either approach requires an analysis of numerous tradeoffs among the various alternatives.

When a hardware approach is elected, it is difficult to choose among several techniques to achieve medium-to-high performance at reasonable cost. Although a hardware-intensive, all-parallel approach will probably be too expensive, it is worth examining such implementations to obtain a basis for comparison. In general, multiplication algorithms that employ external hardware successively shift and add, with slight variations here and there to increase speed or reduce hardware. In the descriptions that follow, the treatment is limited to binary integer operands and results.

Multiplication Algorithms

Most multiplication algorithms are tailored for software execution on a sequential machine. Hardware techniques are generally adaptations of these software methods. The simplest multipliers, therefore, are direct implementations of shift and add algorithms.

Accumulation of partial products by repeated additions of the multiplicand under control of the multiplier bits is the basic principle underlying binary multiplication. Bit-by-bit examination of the multiplier bits determines whether or not an addition is to be performed. Significance is preserved by shifting after each step to align the intermediate partial products.

The first enhancement of the basic principle calls for shifting over 0s; its execution time depends on the number of additions required. A 0 bit in the multiplier causes the addition of a word of 0s to the partial product—or, equivalently, causes the addition to be omitted. As shifting is faster than addition, the overall execution time is decreased by shifting over strings of 0s.

If subtraction is available, a string of 1s in the multiplier, processed in order of increasing significance (or right to left), can be reduced to a subtraction for the first encountered 1, shifts for each subsequent 1, and then an addition when the first 0 is encountered beyond the string. For example:

$$\begin{aligned} 60_{10} = 111100 &= 2^5 + 2^4 + 2^3 + 2^2 \\ &= 2^6 - 2^2 \\ &= 1000000 - 100 \end{aligned}$$

Improved speed can be obtained by inspecting more than one multiplier bit at a time. However, this in-

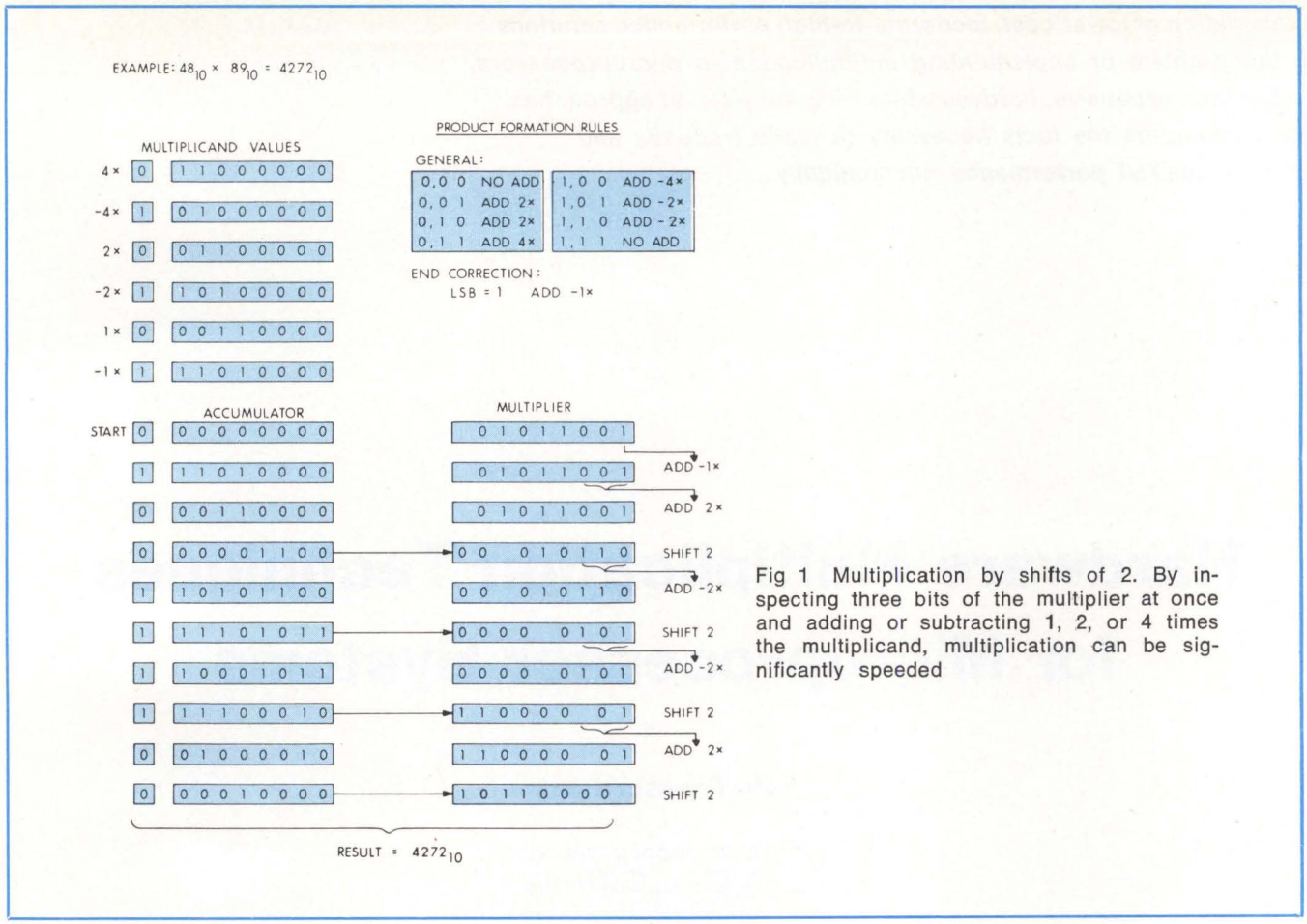

Fig 1 Multiplication by shifts of 2. By inspecting three bits of the multiplier at once and adding or subtracting 1, 2, or 4 times the multiplicand, multiplication can be significantly speeded

volves a few more types of operations, such as addition and subtraction of two times the multiplicand. For 2-bit inspection, the multiplication process follows these rules:

00 No addition
01 Add multiplicand
10 Add 2X multiplicand
11 Add 3X multiplicand

After each operation, the multiplier is shifted two positions.

A variation of this method shifts two positions but inspects three bits at a time; the less significant bit of each pair is inspected twice. Rules governing this method include a correction because each step can produce either the proper partial product, or one that is too large by 1X multiplicand (Fig 1).

These methods of bit grouping and examination are sometimes called multiplier recoding. They give rise to many different hardware implementations; one such implementation can be found in Advanced Micro Devices' AM 2505 iterative multiplier block, which uses Booth's algorithm (Fig 2). This algorithm examines two bits at a time, adds or subtracts, and shifts one position. It is fast with concatenated 1s and 0s, but slow when the multiplier has alternating 1s and 0s.

Multiplication Hardware

The simplest form of binary multiplier consists of a few shift registers and a parallel adder with some control logic (Fig 3). The result is accumulated partially in the multiplier register as the multiplier is shifted out. For a 16 x 16 multiply, a maximum of 16 shifts and 16 adds are necessary. Assuming equal time for shifts and adds, this requires 32 clock periods or, at 100 ns per period (an easily realizable rate), 3.2 μs for the entire multiplication.

A quasi-serial multiplier is an excellent example of the complexity-versus-speed tradeoff. This type of multiplication is based on the columnwise addition of bits in the partial product array of a multiplication table. For example, to find the product of two n-bit binary numbers X and Y, the partial products are arranged in a skewed rectangular array:

$$
\begin{array}{lccccccl}
 & Y_n \ldots & Y_3 & Y_2 & Y_1 & Y_0 & & \\
 & X_n \ldots & X_3 & X_2 & X_1 & X_0 & & \\
\hline
 & X_0Y_n \ldots & X_0Y_3 & X_0Y_2 & X_0Y_1 & X_0Y_0 & & \text{PP0} \\
X_1Y_n & \ldots & X_1Y_2 & X_1Y_1 & X_1Y_0 & & & \text{PP1} \\
X_2Y_n & \ldots & X_2Y_1 & X_2Y_0 & & & & \text{PP2} \\
\vdots & & & & & & & \\
X_nY_n & \ldots & & & & & & \text{PPn} \\
\hline
S_{2n-1} \ldots S_1 & \ldots & S_3 & S_2 & S_1 & S_0 & &
\end{array}
$$

To form the final product, these partial products are added together in one of at least three different ways: fully parallel addition of numbers of n bits

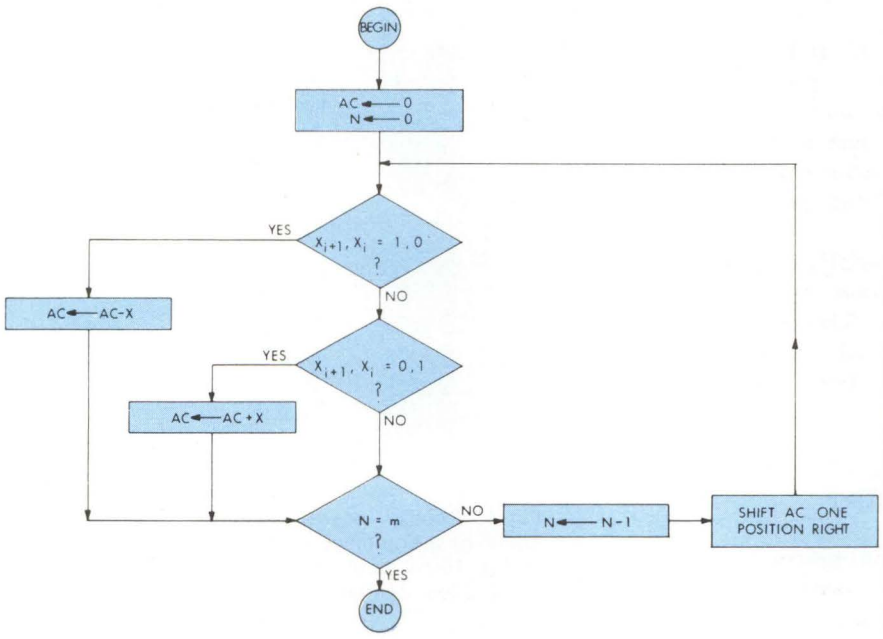

Fig 2 Booth's algorithm. Another recoding to speed multiplication, this process can be implemented in software or hardware. It calls for multiplier and multiplicand to have same number of bits and produces a product of twice that number of bits in the accumulator

each in a large array; addition of n-bit numbers two at a time; and addition by columns. Fully parallel addition, although prohibitively costly in terms of hardware, is the fastest of these three methods. Two-at-a-time addition is still fairly complex and moderately fast, while addition by columns is the least expensive and the slowest. However, column addition can be executed faster if a degree of parallelism is incorporated—for example, by using a combinatorial counter, which is the space-iterative version of a conventional time-sequential counter. It forms the binary sum of the number of 1s presented simultaneously to its inputs.

One possible implementation of such a counting circuit (Fig 4) is constructed with adder trees. A commercially available building block that implements much of this function is the SN74S275 7-input summing unit; this component is also useful in building high speed parallel multipliers. An alternative form uses half-adders (Fig 5).

With a combinatorial counter in a quasi-serial multiplier, parallelism is introduced by simultaneously adding column sums (Fig 6). The operation begins with the multiplicand left-justified in the double-length shift register, and the multiplier in the holding register. At the start of the multiplication cycle, if the least significant bits (LSBs) of both numbers are 1s, the AND gate and the counter generate a count of 1, which is added to the previous contents (all 0s at the start) of the add-and-shift register. The LSB of the count becomes the LSB of the product. The multiplicand

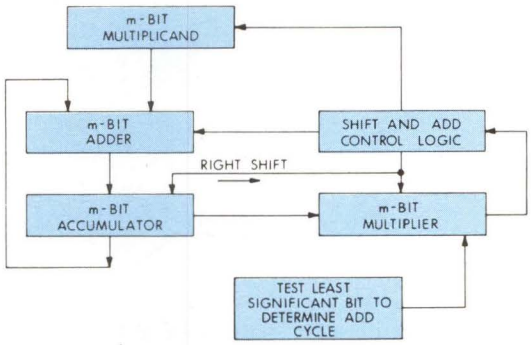

Fig 3 Shift-and-add multiplier. This is simplest and most straightforward technique

is then shifted right one position, and the process repeats. During the $(n - 1)$th cycle, the multiplicand is right-justified in the double-length register, and the most-significant bit (MSB) is in the place of the original MSB. During the $(2n - 1)$th cycle the MSB is the only original bit left.

For a 16 x 16 multiplier of this type, the interface to a microprocessor is simple. Multiplicand and multiplier are loaded into their respective registers directly from the microprocessor data bus, under control of a flag or address bit. Then, if the microprocessor is fast enough, results can be read back over the same bus at the end of the multiplication cycle. If the hardware multiplier unit uses a 10-MHz clock, results will be available after 3.2 μs. This time is comparable to that of a 16-bit ADD instruction with one memory reference in most metal-oxide semiconductor (MOS) microprocessors, so the hardware multiplier can be transparent to the processor.

Hardware costs for the quasi-serial multiplier are fairly low. A typical implementation uses six 8-bit shift registers, two 8-bit latches, a 5-bit adder block, a 5-bit shift register, and four quad gates. Optional hardware includes bus buffering from the microprocessor if required.

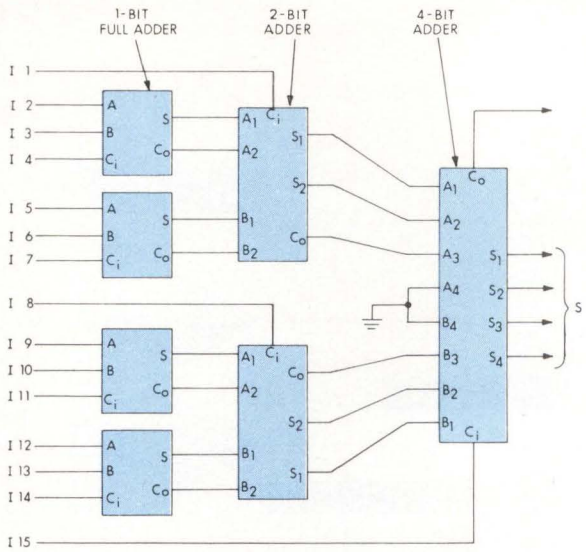

Fig 4 Parallel counter. Binary output at right is count of the number of 1s appearing simultaneously in the 15-bit input at left. It requires two dual full-adders, two 2-input adders, and one 4-bit adder

Sequential Iterative Multiplier

The symmetry of the multiplication process lends itself to other interesting iterative procedures. Just as the quasi-serial multiplier made use of the array nature of the partial products, another approach makes use of the space-iterative nature of bit-serial product formation (Fig 7).

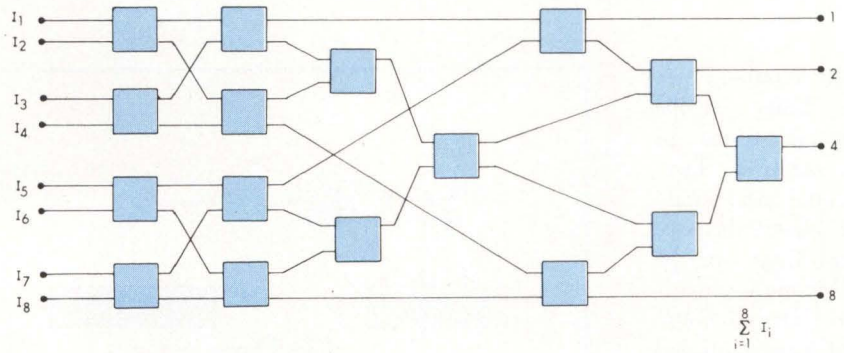

Fig 5 Parallel counter using half-adders. This network does not depend on ripple carry, but has six stages of propagation delay, compared to three in Fig 4

Multiplier and multiplicand are placed in a shift register with their bits alternating. Beginning with the LSB of the multiplier, every alternate bit position in the shift register is gated to a full adder by the bit at the low end of the shift register. Product bits are formed in an array of full adders with interstage signals appropriately delayed for proper synchronization. For an n-bit multiplication the result accumulates in 2n cycles. As with the quasi-serial method, the hardware for this approach is modest; a 16 x 16 multiplier may be implemented with four 8-bit shift-registers, four 8-bit latches, eight dual-gated full-adders, and optional data buffers to interface with a microprocessor.

Actual multiplication time for this scheme is 32 clock periods; however, setting up the operands requires overhead, which depends on the type of microprocessor. For example, as multiplier and multiplicand bits are arranged in alternating fashion, some shift sequence or special gating may be required to load the operands.

Table Look-Up Multipliers

Read-only memory (ROM) is fast becoming one of the least expensive resources in a microcomputer system. Its declining price per bit is causing a shift toward implementing more and more logic with ROM using table look-up techniques. However, for multiplication and other forms of function evaluation, a

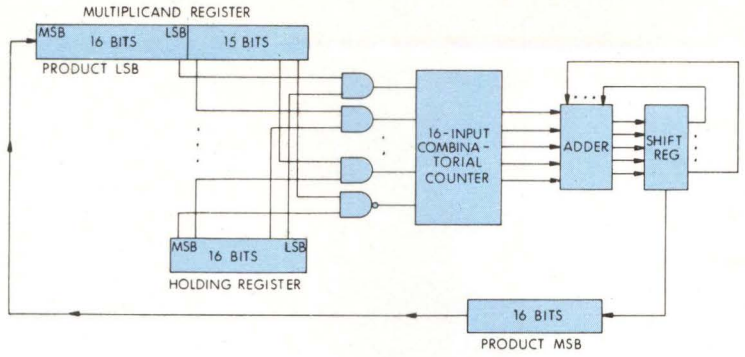

Fig 6 Quasi-serial multiplier. Combinational counter repeatedly gives count of bits shifted into the register; adder accumulates the count. For two 16-bit numbers, multiplier can be built with four quad 2-input ANDs, one 2-input NAND, two 8-bit latches, one 5-bit register, five 4-bit adders, two 2-bit adders, and six 8-bit shift registers; multiplication time is 16 clock periods

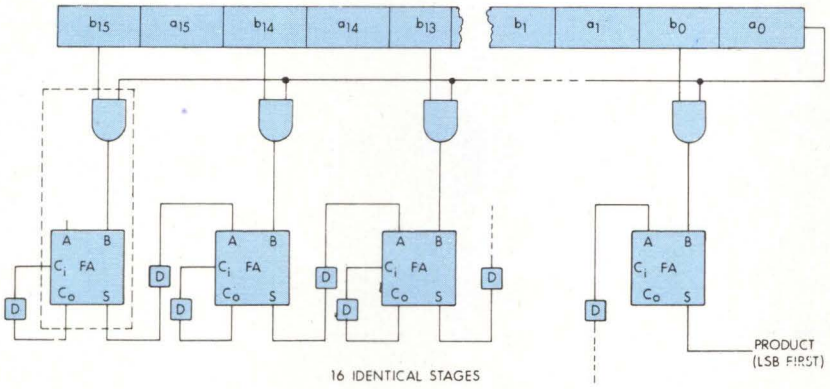

Fig 7 Sequential multiplier with iterative technique. This circuit generates product of two 16-bit numbers; if clock period is 100 ns, the multiplication time is 3.2 μs. It requires four 8-bit shift registers, four 8-bit latches, 16 gated full adders, and one oscillator (not shown)

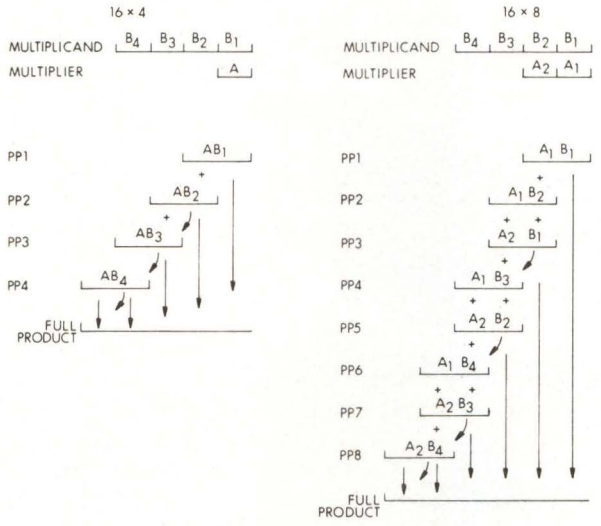

Fig 8 Partial product accumulation. Dividing multiplier and multiplicand into 4-bit parts and processing them separately can simplify multiplication under certain circumstances. Partial products, each eight bits wide, are arranged according to positional significance

prohibitively large number of bits is required for direct and total look-up; an effective compromise combines ROM tables of convenient sizes with adder blocks.

Examples of both a 16 x 4 and a 16 x 8 multiplication are shown in Fig 8. The multiplier (A) and the multiplicand (B) have been partitioned into 4-bit groups; the procedure looks up partial products of these groups in a ROM table at each step. For example, the least significant four bits of the multiplicand are multiplied by the least significant four bits of the multiplier to create the first partial product.

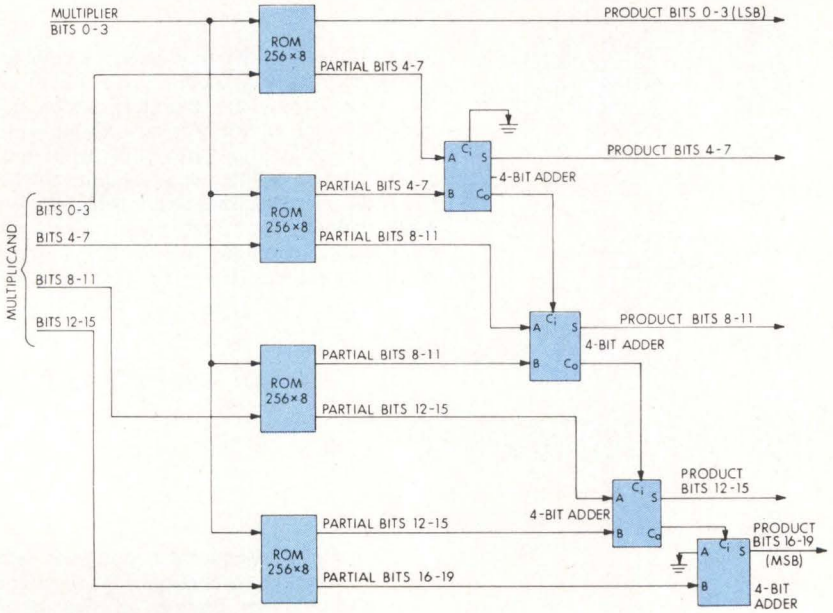

Fig 9 Table look-up. Technique of Fig 8 permits multiplication by ROMs and adders, an approach that is expensive for long operands

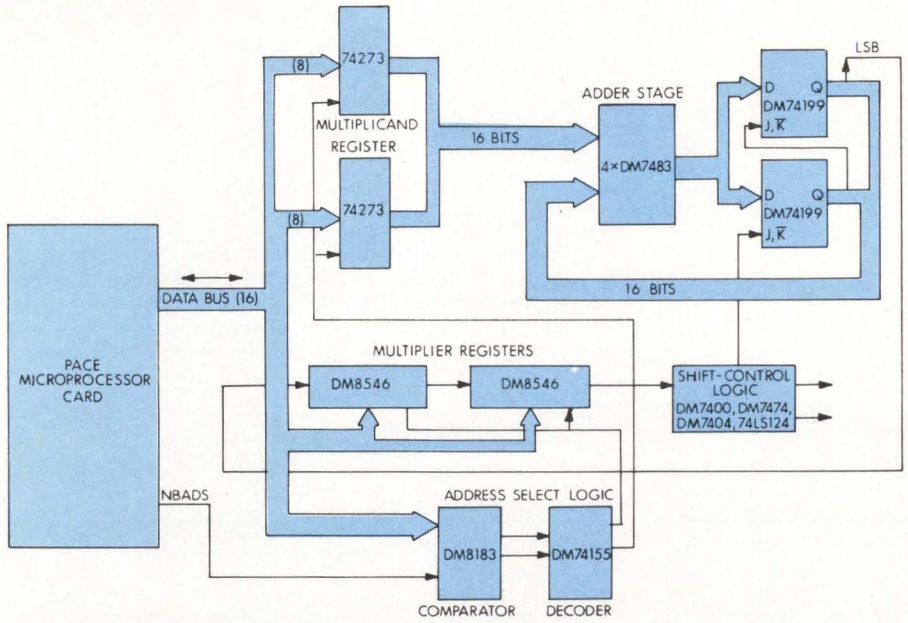

Fig 10 Low cost 16 x 16 multiplier. Although based on PACE and other National Semiconductor products, this design is generally applicable to other manufacturers' products as well

TABLE 1

Building Blocks for Hardware Multiplication

Description	Manufacturer	Part Number
4 x 4 Look-Up Multiplier	National Semiconductor	DM8875A, DM8875B
4 x 2 Iterative Array.	Fairchild	9344
4 x 2 Iterative Array	Advanced Micro Devices	25S05
4 x 4 Parallel Multiplier	Texas Instruments	SN74S274
8 x 1 Serial Multiplier	Advanced Micro Devices	25LS14
16 x 16 Parallel Multiplier	TRW	MPY-16
8-Bit Parallel Register With Sign Extend	Advanced Micro Devices	25LS22
7-Input Adder	Texas Instruments	SN74S275
8-Bit Universal Register	Texas Instruments	SN74S299
8-Bit Universal I/O Register	National Semiconductor	DM8546

The next partial product is produced by multiplying the next significant four bits of the multiplicand by the least significant four bits of the multiplier, and shifting four places to the left; and so on. For 4 x 4 multiplication, there are 256 possible results; hence the table must contain 256 entries of eight bits each. Such a table can be stored in a 256 x 8 ROM. Shifted partial products thus generated are added, as the diagram shows, in 4-bit 2-input adders connected to the ROM outputs (Fig 9). Operational speed for this circuit is determined by access time of the ROMs, speed of the 4-bit adders, and carry propagating time.

For longer operands, this table look-up approach is expensive in hardware. A 16 x 8 multiplier, for instance, would require eight ROMs and eleven 4-bit adders. Similarly, a 16 x 16 multiplier would need 16 ROMs and 28 adders.

A combination of creating partial products in parallel and adding them word-serially gives rise to an interesting variation. In this approach, the multiplicand is loaded in parallel into a holding register; the multiplier is then passed through serially by bit, generating product bits according to Booth's algorithm. A commercially available component that does this in 8-bit groups is the AM25LS14 2's-complement multiplier made by Advanced Micro Devices. It contains a cascading input that accepts longer multiplicands. The entire multiplication takes m + n shift cycles, where m and n are the bit lengths of the multiplicand and multiplier. The product is available serially, and must be converted to a parallel word in a shift register for transfer to a microprocessor.

Application Example

A typical low cost binary multiplier (Fig 10) makes use of a few universal shift registers and standard 4-bit adders, plus the control logic necessary to direct the operations. Interface signals for National Semiconductor's PACE microprocessor are shown, although any 16-bit central processor could communicate similarly.

The economy of this approach lies in the use of inexpensive standard components; clock frequencies can be low enough for standard transistor-transistor logic, yet the overall speed of multiplication is fast enough to be transparent to the calling program. For example, using the PACE instruction set, a 4-instruction sequence produces a 32-bit product:

```
(1)  ST   ϕ, MCAND      ; LOAD MCAND
(2)  ST   1, MPLIER     ; LOAD MPLIER, START MULT
(3)  LD   ϕ, RESULTLO   ; GET RESULTS
(4)  LD   1, RESULTHI   ;
```

MCAND is the address of the multiplicand register; MPLIER that of the multiplier register; ACϕ is the multiplicand, and AC1 the multiplier. The second store (ST) instruction initiates multiplication. In the time it takes for the first load (LD) instruction to set up for data acceptance, the multiplication can be completed (assuming a 4-MHz clock). This particular configuration uses two 8-bit latches (SN74273), two universal shift registers (DM8546), two parallel-in parallel-out shift registers (DM74199), four 4-bit

TABLE 2

16 x 16 Multiplication Techniques

Hardware Method	Basic Cost*	Time
Shift-and-Add	$ 15	3.2 μs
Quasi-Serial	15	3.2 μs
Serial Iterative	15	3.2 μs
Table Look-Up	120	0.8 μs
Parallel/Serial	50	1.6 μs
Parallel		
Iterative Array (AMD)	320	150 ns
Wallace Trees (TI)	550	120 ns
Single Chip (TRW)	250	300 ns
Software Method	**Storage (Bytes)**	**Time**
Booth's Algorithm on PACE Microprocessor	90	1100 μs
Booth's Algorithm on 6800 Microprocessor	110	600 μs
Shift-and-Add on PACE Microprocessor	20	1000 μs
Microprogrammed on IMP-16	4	150 μs

*Based on present 100-quantity pricing

adders (DM7483), and some address compare and decode logic, in about 16 standard packages.

Parallel Multipliers

A brief look at all-parallel multiplication techniques is interesting for the sake of comparison with more economical approaches. Parallel multiplication is based on the space-iterative nature of the partial product array. Instead of forming partial products for each bit of the multiplier, a combinatorial approach creates the simultaneous sum of several bits.

Terms in a partial product array are basically the AND functions of various bit combinations of the multiplier and multiplicand. These individual terms are summed in carry-save adder trees. Hardware for this technique is quite costly because it includes a large number of combinatorial gates. For example, using TI 74S274 and 74S275 multiplier blocks, a 16 x 16 parallel multiplier that operates in the 120 ns range can be built with 47 integrated circuits. Similarly, using the AMD 25S05 4 x 2 multiplier block, a 16 x 16 parallel array can be implemented with 32 larger devices and speeds in the 150 ns range. A recently announced product from TRW puts a complete 16 x 16 multiplier on a single chip. These are listed along with others in Table 1, which, although a representative list, does not necessarily cover all currently available products. Building blocks listed in the table may be used in several combinations to realize various implementations of binary multipliers.

Conclusions

Most of the schemes for binary multiplication surveyed in this article use variations of shift and add operations, because most microprocessors work well at the moderate execution speeds of these methods. These techniques and some of their software counterparts are compared in Table 2.

All figures in the table are merely estimates for the sake of comparison. Therefore, the ultimate choice depends on the particular cost/performance ratio desired. Several low cost solutions proposed in this article offer execution speeds that are high enough for many applications where expensive hardware cannot be justified.

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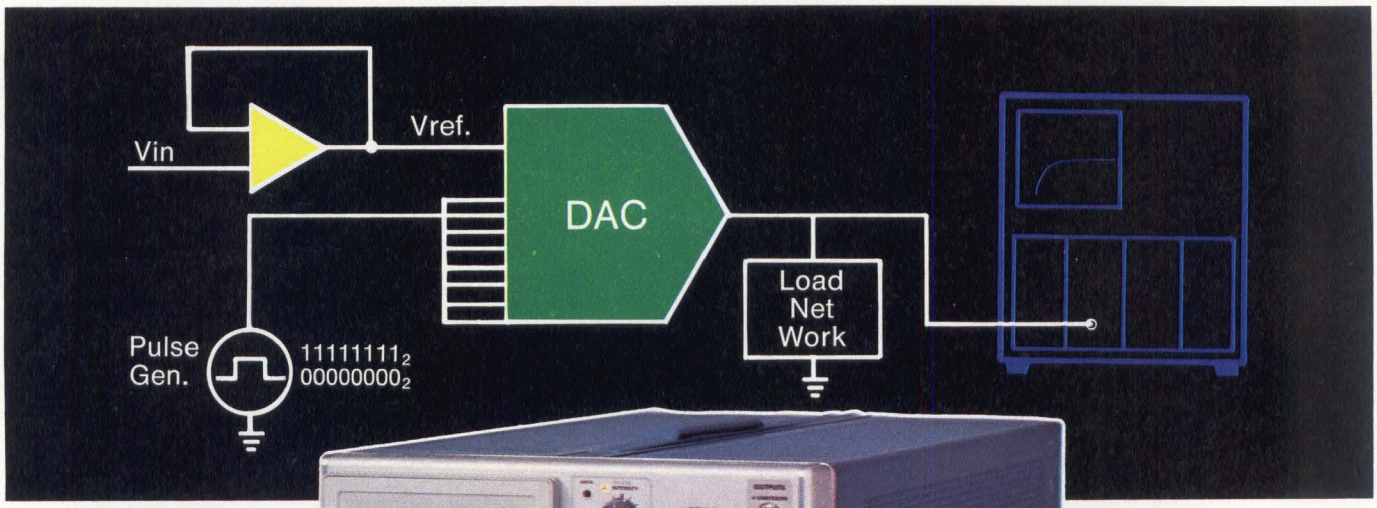

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When based on an algorithm that is constructed with the type of redundancy and characteristics of the data source in mind, compaction allows efficient reduction of redundancy in a data set to achieve savings in both transmission time and required storage space

Data Compaction in Computer Systems

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Compaction of data, ie, elimination of redundant bits in a data set, is well known and is particularly useful in data communication and storage systems. It is not uncommon to find that 50% or more of the bits in a data set are actually redundant as far as representation of information is concerned. Removing redundant bits achieves considerable savings in transmission time, storage space, or both. As the amount of data in computer systems and in communications between systems increase, compaction methods will become more and more significant.

Redundancy of data bits manifests itself in several ways. First, if each character is represented by a fixed number of bits and if some characters appear more frequently than others, representation of each character by the same number of bits will result in redundancy. Such is the case when characters of English text are represented by 8-bit bytes. Since characters do not occur with equal frequency in the English language (eg, the letter E is used more frequently than the letter Z), representing characters of English text with 8-bit bytes results in redundancy.

A second type of redundancy occurs in a string of identical characters. This redundancy is prominent in data sets representing graphic or analog information, and can also occur in text; eg, a fixed length record might be filled with blanks or zeros. A string of characters such as X X X X X provides two kinds of information: character type, X, and the number of repetitions beyond the first character, in this case four. Signaling the number of repetitions (four) with four 8-bit bytes is wasteful.

A third kind of redundancy results when the occurrence of one character implies the occurrence of one or more other characters. For example, the letter Q at the beginning of a word always implies that the letter U follows. This concept can be generalized to imply one group of characters by another group of characters.

Data redundancy may be desirable in noisy communication channels where it will enable lost or garbled information to be recovered. However, to make use of the redundant data bits, they must be structured in such a way that detection and correction of lost data are feasible. Examples of this structuring are parity bits, Hamming codes, or cyclic redundancy code bits. In all these cases, it should be noted that redundancy is added by the encoder before transmission or storage. In contrast, the three types of redundancy mentioned previously are inherent in the source of data. Since they do not lend themselves to improvement in data recovery, their elimination can result in savings of transmission time or storage medium.

Information Theory

A review of some information theory concepts will point to methods for eliminating redundancy and thus lead to ways of achieving economic savings. As with any scientific discipline, information theory seeks first to define information and to measure it quantitatively. Early research was motivated by an interest in increasing the rate of data transmission over telegraph lines. Claud

Shannon established the foundations of modern information theory in 1948.

The simplest type of information is a statement of "yes or no," "go/no-go," or "on/off." Information theory, however, is concerned also with the probability that an event will occur. For example, if you can see a train on the railroad crossing, you know that you cannot cross the tracks with your car; there is no need for the red warning light. However, when you cannot see the train, the warning light serves to resolve your uncertainty about the possibility that a train will come while you are driving across the tracks.

Therefore, an information source that can signal a "go/no-go" decision is the simplest type. The two choices presented can be represented by the binary numbers 1 and 0. The information theorist calls this "encoding the source of information"; the two binary numbers are termed "a code." In general, the source is capable of selecting and emitting a symbol from a finite alphabet of symbols. If it is known in advance what symbol the source emits, no information is generated. The greatest amount of information is obtained when there is total uncertainty about the symbol selection procedure performed by the source, ie, symbols are emitted at random. It is also possible that the source emits different symbols, with each symbol having a certain probability of being emitted. The measure of freedom that the source has in selecting the symbols and the amount of uncertainty that is involved in receiving them is called the "entropy" of the source.

Consider a source which can select symbols from an alphabet S which contains members $s_1, s_2, s_3, \ldots, s_n$. Let the probability of occurrence for each symbol be P_i. Then entropy is defined as

$$H = -\sum_{i=1}^{n} P_i \log_2 P_i \quad \text{bits/symbol}^*$$

The word entropy is a familiar term in thermodynamics, where it denotes the energy of a system which cannot be transformed into mechanical energy. Its mathematical expression is analogous to the expression above, from which it gets its name. In information theory, entropy indicates the average number of bits required to represent each symbol of the source alphabet.

Tossing a coin serves as a model for an information source. The two sides of the coin, tails (T) and heads (H), correspond to the source alphabet s_1, s_2. Tossing the coin corresponds to the source's process for selecting a symbol. On the average, either side (symbol) is equally likely to appear. Tossing two coins and encoding T = 0, H = 1, corresponds to a source of a 4-symbol alphabet, which is encoded

Outcome	Symbol	Probability	Code
T T	s_1	0.25	0 0
T H	s_2	0.25	0 1
H T	s_3	0.25	1 0
H H	s_4	0.25	1 1

The entropy of this source is calculated as

$$H = -\sum_{i=1}^{4} P_i \log_2 P_i = -4 \times 0.25 \log_2 0.25 = 2$$

Two binary symbols are needed to encode the alphabet of this source. However, if the coins were totally unfair, such that only T could occur, the only symbol selected would be s_1. There would be no need to do any coin tossing to determine the outcome, since it would be known in advance. A source such as this, which provides no information, has an entropy of 0.

However, if it is assumed that T occurs with each coin at a probability of 0.75, leaving a 0.25 chance for H, the table would look like

Outcome	Symbol	Probability	Code
T T	s_1	0.5625	0 0
T H	s_2	0.1875	0 1
H T	s_3	0.1875	1 0
H H	s_4	0.0625	1 1

This source has an entropy of

$$\begin{aligned} H = -\sum_{i=1}^{4} P_i \log_2 P_i &= -(0.5625 \log_2 0.5625 \\ &\quad + 2 \times 0.1875 \log_2 0.1875 \\ &\quad + 0.625 \log_2 0.0625) \\ &= 1.62 \text{ bits/symbol} \end{aligned}$$

By calculating the entropy it is found that about 1.62 bits are needed for every symbol, compared with the 2 bits/symbol which are used. This results in a savings of almost 20%. But, how does one provide fractions of a bit? Recall that the entropy indicates the *average* number of bits per symbol. If a short code is assigned for more frequently occurring symbols and a longer one for less frequently encountered symbols, then a long string of source symbols will have, on the average, fewer bits per symbol. In fact, by considering the source emitting blocks of symbols (combinations of a fixed number of symbols) and encoding these blocks, the number of bits per symbol required can approach the entropy as closely as desired.

Huffman Coding

The code for the 2-coin tossing experiment can be reassigned as

Outcome	Symbol	Probability	Code
T T	s_1	0.5625	0
T H	s_2	0.1875	10
H T	s_3	0.1875	110
H H	s_4	0.0625	111

The average number of bits per symbol is calculated by multiplying the code word lengths by their probabilities. This code uses

$$1 \times 0.5625 + 2 \times 0.1875 + 3(0.1875 + 0.0625)$$
$$= 1.63 \text{ bits/symbol}$$

While this result is not as good as that indicated by the entropy, it does approach it. Another property of this code is that it can be decoded instantaneously as the code words occur in a data stream. For example, the following

*The basic unit of information is defined by $-\log_2 P$ bits, where P is the probability of a 2-outcome event or decision such as go/no-go. If that probability is 0.5, then $-\log_2 0.5 = 1$ bit. A choice other than 2, say r, for the base of the logarithm would result in r-ary units. By summing up the amount of information times the probability of occurrence for each symbol, the average information contents of the source (H) can be obtained.

string, reading left to right, can be decoded immediately, without waiting for the end of the string.

Encoded Message: 0 1 0 0 0 1 1 1 0 1 1 0 1 0

Decoded Message: s_1 s_2 s_1 s_1 s_4 s_1 s_3 s_2

Codes such as this, which assign efficiently short code words to frequently occurring symbols and longer code words to less frequent symbols, are called Huffman codes. They can be formed by the tree method shown in Fig 1. The tree combines the two lowest probabilities, 0.09 and 0.04, of symbols s_5 and s_6, into a node which represents the combined probability of that pair, 0.13. Then the next pair of lowest probabilities, in this case those of

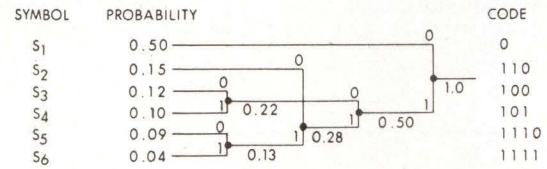


Fig 1 Tree method for constructing Huffman codes. After constructing the tree, by combining successive lowest probability pairs into nodes, 0 and 1 binary values are assigned to each branch. The code is derived by tracing from the 1.0 probability node to each source symbol, noting 1s and 0s as encountered

symbols s_3 and s_4, is combined into a node of 0.22. The next two lowest probability numbers are 0.13 (the combined s_5, s_6 nodes) and 0.15, the probability of s_2. This pair joins into a node with a combined probability of 0.28. The tree is then completed, by combining lowest probability node pairs, to a combined probability of 1. Next, 0 and 1 binary symbols are assigned to each branch of a node. The code can now be constructed by traveling from the 1.0 probability node to each symbol and writing down, left to right, the 0s and 1s encountered on the way.

In essence, this algorithm reduces the original source alphabet into "super symbols" of combined probability. At the 1.0 node, there are only two "super symbols"; the most trivial code for two such symbols is simply 0 and 1, respectively. By working backward, each "super symbol" is broken down and assigned 0s and 1s at each branch until the original source symbols are reached. The size (number of bits) of the shortest code word or that of any other code word depends on the particular probability distribution of the source symbols.

This method eliminates the redundancy that occurs when fixed length code words are assigned to symbols having unequal probabilities of occurrence. To construct the Huffman code, the probability distribution of the source alphabet must be known. From this, a tree can be formed to yield a Huffman code. The average number of bits per symbol of a Huffman code is within one bit of the average calculated by the entropy. The algorithm can be implemented either with software or hardware, or with a combination of the two. In either case, it usually requires that the source symbol be recognized, and that the code word (bits) be located in a table and then assembled into entities (bytes or words) with which the machine normally deals. The decoding process is slightly more complicated, since the boundaries (commas) between the (variable length) code words in the incoming bit stream are not initially known. One method of locating them is to look at the incoming bit stream through a "window" whose width is that of the shortest code word. Since the code is instantaneous, a search is made for a corresponding source symbol in the "window." If none can be found, the window is enlarged by one bit and the search is repeated; this process is repeated again until a window width is found which points to a source symbol. The decoded bits are then dropped from the data stream. The consideration of hardware or software methods usually implies a tradeoff between cost and time spent on the encoding/decoding process.

Unfortunately, the compaction of data is not entirely straightforward. First, different data blocks will compact into new data blocks of variable length which then must be reorganized. Second, in many cases, a data source contains information other than English text, making it necessary to know the probability distribution of all possible characters. Individual data sources can vary widely from these statistics and thus will not yield satisfactory results. It is possible to gather statistics on the particular data to be compacted and to construct a unique Huffman code. This code can then be affixed in front of the compacted data and transmitted uncompacted so that the decoder can use it to decompact the following blocks of compacted data. Of course, this implies additional cost, time, and storage space.

String Coding

The second type of redundancy consists of character strings, which are contiguous repetitions of the same character, eg, X X X X X. Often referred to as a run of characters, these strings occur frequently in graphic or analog information, and also in data sets which consist mainly of text. One simple way to compact such a string is to define a unique symbol within the source alphabet to mean "repeat" (designated RP). This symbol, followed by a count character, can be used to indicate a string more efficiently. For example, the above string would be encoded X RP 4. When dealing with 8-bit bytes, the string can be represented with $3 \times 8 = 24$ bits using the RP symbol and count character, compared with the $5 \times 8 = 40$ bits required initially. If Huffman codes are used, both string character X and repeat character RP are assigned variable length code words, according to their probabilities of occurrence.

This method is efficient only if the string is long. If Huffman compaction is not used, the method provides an advantage only if the string length is four or greater. The method does not compact strings of lengths of two or three. Since it has been shown statistically that shorter strings occur more frequently than longer strings and

because, in many cases, character strings occupy a significant portion of the total data, it is worthwhile to derive a more efficient method.

The following method, which efficiently encodes repeated character strings of length two, is also interesting because it does not break byte boundaries; this is significant both in implementing a compaction algorithm and in the management of storage space. The method consists of mapping the source alphabet, which might be an 8-bit EBCDIC code, into a mapped code alphabet whose code word length is that of the original code words. This mapping is done so that the first 50% of the most frequently occurring source symbols within the string all have the same most significant bit (MSB), say 0. Those symbols that occur least frequently have an MSB of 1. Thus two sets, A and B, distinguished by their MSBs, 0 and 1, respectively, are obtained. Fig 2 shows an example of this mapping into two sets. For brevity, an alphabet of only eight symbols is used.

Mapped code symbols are applied to an encoder which works in three states: A, B, and N (Neutral). In each state, the encoder makes an assumption about the type of symbols to be encoded. In states A and B, it assumes symbols from sets A and B, respectively; in state N, it assumes symbols for either set with equal likelihood (see Fig 3).

When the encoder is in state A, it emits single symbols (not belonging to a string) which are members of set A without further change. Note that all emitted symbols have an MSB of 0. If a repeated character string of length two is detected in the data stream, the encoder inverts the MSB of the first symbol to 1 and does not emit the second symbol. If the string is longer than two, a count character indicating the number of other characters in the string is appended to the symbol with the inverted MSB. This count character is recognizable because its MSB is also inverted, ie, the MSB is 1. Thus, a count character of length eight can indicate $2^7 - 1 = 127$ symbols in the string beyond the first two. If the string is longer than 127, a second count character can be added. Since the MSB of the second count character is also inverted, it is recognized as a count character. Fig 4 shows examples of this encoding procedure.

SOURCE ALPHABET	SOURCE CODE	PROBABILITY IN STRINGS	MAPPED CODE ALPHABET	SET
S_1	100	0.24	000	A
S_2	010	0.18	001	
S_3	001	0.14	010	
S_4	110	0.12	011	
S_5	000	0.10	100	B
S_6	011	0.10	101	
S_7	101	0.07	110	
S_8	111	0.05	111	

Fig 2 Mapping into two sets. Technique for encoding repeated character strings distinguishes between most-frequently occurring and least-frequently occurring symbols in a source alphabet by assigning MSBs of 0 and 1, respectively. Source alphabet is mapped into a code alphabet with code word length equal to that of the source code

In state B, encoding of single symbols or strings is performed identically as in state A, except that the inverted MSB is 0 instead of 1.

In state N, strings are not encoded—each symbol is emitted as mapped. Since state A represents characters that occur most frequently in strings and since a large percentage of the data set is assumed to consist of strings, the encoder will operate most frequently in state A.

Dividing source symbols into two sets basically implies the most significant bit. This bit is then used to signal the presence (if inverted) or absence (if not inverted) of a character string of length two or of a count character. When a source symbol from the other set is detected, a switch to state N is necessary where the MSB is not implied and each source symbol is encoded as mapped. From state N, the encoder can switch to either state A or B, depending on the type of characters that occur in the data stream. However, rules for switching from state to state must be defined.

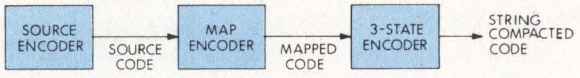
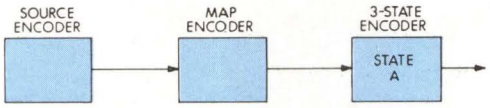


Fig 3 Information source, mapping, and compaction. Mapped code symbols are applied to a 3-state encoder. In states A and B, encoder assumes symbols from those sets, respectively; in state N, it assumes symbols from either set with equal likelihood



SEQUENCE NUMBER	SOURCE SYMBOL	SOURCE CODE	MAPPED CODE	COMPACTED CODE
1	S_1	100	000	000
2	S_2	010	001	001
3	S_1	100	000	100
4	S_1	100	000	
5	S_3	001	010	010
6	S_2	010	001	101
7	S_2	010	001	110
8	S_2	010	001	
9	S_2	010	001	
10	S_1	100	000	000

Fig 4 Encoding in state A. Symbols are emitted sequentially 1 to 10. 1, 2 are emitted by the 3-state encoder without further change (except as mapped); 3,4 constitute a string of length two. Compacted code for this string consists of the mapped code of s_3 with an inverted MSB. Symbols 6,7,8,9 constitute a 4-character string, with the first two characters indicated by an inverted MSB mapped code (101), to which is appended a 3-bit count field, also with an inverted MSB and contents of (10). Symbol 10, a single character, is emitted as mapped

At the start of the data stream, the encoder is in state N (as is the decoder). In this state, when k contiguous source symbols (k = a small number, eg, 3, 4, or 5), *all* belonging either to set A or to set B, are detected, the encoder correspondingly switches to state A or to state B. The decoder follows the same rule. In state A or B, single symbols or strings of the same symbol are encoded as described previously. When a source symbol of the other set appears in the data stream, the encoder switches to state N before encoding that symbol. This switching is indicated by emission of an "escape character," which serves to signal the decoder to switch to the Neutral state. The meaning "escape" is assigned to the character in the set that has the lowest probability of occurrence, and is thus part of the original source alphabet.

Since the "escape" character is part of the original source alphabet, it may appear in the source data stream. Therefore, to distinguish between its original meaning and its assigned "escape" meaning, it is emitted twice whenever it occurs as a single symbol in the source data stream. When it occurs in a string, the string is treated like any other string. Following this rule, the decoder discards a second "escape" character, and recognizes the first one as coming from the source data stream.

It is possible for source data to contain two adjacent strings, such as X X Y Y Y, both strings within the same set. In this case, the first symbol of the second string is encoded as a single symbol, to prevent it from being construed as a count character. The remainder of the second string is encoded as a single or string symbols, as the case may be. A comprehensive example, including switching, is given in Fig 5.

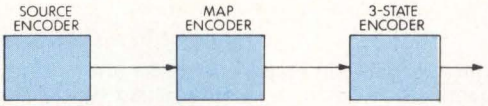
The example given in Fig 5 shows no compaction because of the particular sequence that was chosen for illustration. However, in a real environment, compaction ratios of approximately 2:1 have been observed with this algorithm. Also, it should be noted that, depending on the speed of the decoder, some buffering is required since the two code words may decode into a long string.

Implied Sequences

Data compaction can also be performed on a dependent information source. This source is also called an nth order Markov source, wherein the probability of occurrence of the next character is dependent on n previously occurring characters. English text is such a source, for each character's probability of occurrence depends, to some degree, on the previous characters. For example, it is highly likely that the character "E" will follow the characters "TH," while the probability that "Z" will follow is almost 0. Because an English text source is not free to emit characters in a random sequence, the entropy is correspondingly reduced. Shannon estimated the entropy of English text to be between 0.6 and 1.3 bits/symbol.

Better compaction can be achieved by taking dependency into account. One method is to consider English text emanating from a first-order Markov source and to provide a separate probability table of the character that will follow for each character. An alphabet of "m" characters would require m + 1 tables, one for each letter and another for the start of the text, where there is no previous character. If a Huffman code is generated for each probability table, the overall average number of bits per symbol will be less than if there were only one table and dependencies were not taken into account.

In practice, this technique requires m + 1 encoding and decoding tables, plus implementation of a switching algorithm. It would also incur a premium price. Good compaction can be achieved with considerable savings in encoding overhead by clustering together those probability tables which look similar. Thus, the number of Huffman codes would be reduced, yet the compaction



SEQUENCE NUMBER	SOURCE SYMBOL	SOURCE CODE	MAPPED CODE	STATE	COMPACTED CODE
				N	
1	S_1	100	000		000
2	S_2	010	001		001
3	S_1	100	000		000
				A	
4	S_1	100	000		000
5	S_2	010	001		101
6	S_2	010	001		
7	S_4	110	011		011
					011
8	S_1	100	000		000
9	S_4	110	011		111
10	S_4	110	011		
11	S_3	001	010		010
12	S_6	011	101		011
				N	101
13	S_1	100	000		000
14	S_8	111	111		111
15	S_5	000	100		100
16	S_5	000	100		100
				B	
17	S_5	000	100		000
18	S_5	000	100		
				N	
19	S_1	100	000		111
					000

Fig 5 Encoder state switching. Assuming an "inertia" constant k = 3, the 3-state encoder starts at N and stays in this state for three consecutive symbols, all from set A, then switches to state A. Symbol s_4, the escape symbol from state A, is encoded twice. Symbols 9, 10 constitute a string of the escape symbol but are treated like any other string (MSB inverted). Symbol 12, since it is from set B, is preceded by the escape symbol from set A (single occurrence), which causes the encoder to switch to state N. Three consecutive symbols from set B occur from symbols 14 on (including a string which is treated as single characters), and then the encoder switches to state B where it remains until it encounters symbol 19, again from set A and preceded by an escape character from set B

ratios would remain better than those achieved without taking dependency into account.

Summary

Describing the three types of redundancies and illustrating the encoding methods which can be used to minimize the amount of redundancy have shown how the number of bits required to transmit or store information can be reduced, thereby providing savings in transmission time and in storage space. Compaction ratios ranging from 2:1 to 4:1 are common using Huffman codes or string compaction methods, both of which are straightforward to implement. A compaction algorithm can be implemented with either hardware or software. Tradeoffs to be considered in choosing a method include the overall system complexity and the problems of organization of uncompacted and compacted data. Another consideration is that compaction methods are only as good as the statistics that have been previously collected about the data source, and that it is possible to have a unique collection of data for which a particular algorithm or code will fail, with the resulting "compacted" data containing more bits than the original.

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CIRCLE 49 ON INQUIRY CARD

Unexpected benefits can be derived from using memory components known to have defects. This approach permits manufacture of high density components with less penalty from low yield and provides users with cost savings, reliability improvements, and power savings and system size reductions

The Case For Using Partially-Good Memory Devices

Robert H. F. Lloyd*

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Techniques have been implemented that use memory components with known defects in the manufacture of memory systems, and have provided some unexpected benefits. However, to realize these benefits requires a change in the thinking of component manufacturers and users. Because the benefit is most obvious to the system manufacturer, the pressure for adopting this system must begin there.

The particular approach discussed in this article involves using partially good memory chips in which at least three-quarters of the memory array is known to be good. This approach is easy to implement and takes advantage of inherent cost savings. It divides components into five classes: one in which all bit positions are good, and four in which one of its four quadrants contains defects (Fig 1). These components are mounted on two types of memory cards: one with only all-good components, and one with a mixture of all-good and partially-good components. Both cards appear identical at the card connector.

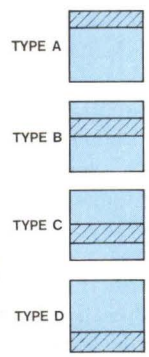

Fig 1 Partially-good memory components. The quadrant containing one or more defects defines four types of partially (three-quarters) good memory components

Cards of the second type are organized [Fig 2 (b)] so that they can accommodate any one of the four types of partially-good chips. Normally two address lines define any one quadrant of the chip. When partially-good components are used, a modified chip-select is derived from two of the address lines; it translates an address that would normally go to a defective portion of a chip to an all-good chip at the top of the card. Programming jumpers define the translation for the particular type of partial component, a, b, c, or d, and allow all cards to be interchangeable.

This concept makes sense immediately after the introduction of new high levels of large-scale integration, when yields are likely to be low. At that time it permits more of the devices produced to be used. Later, as yields improve, the concept is less advantageous—however, it can

*Mr Lloyd is currently serving as president of Conver Corp, San Jose, Calif.

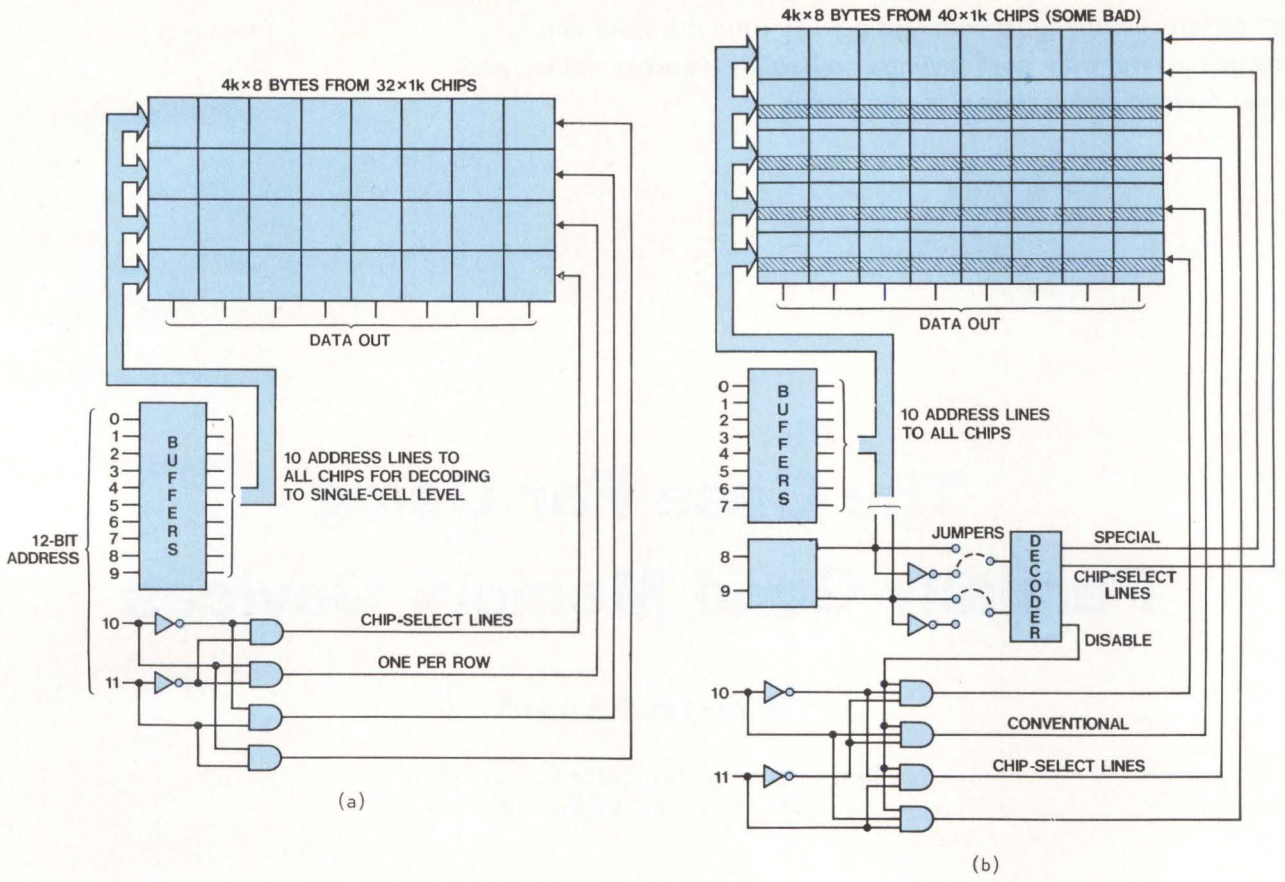

Fig 2 Partially-good vs conventional memory card. Jumpers in (b) allow the card using partially-good memory components to appear identical at the card connector to a conventional memory card (a) using all-good memory components

be applied reasonably for as much as 75% of a product's economic life. Toward the end, when production yield is high, most of the cards produced will carry only all-good components. Since the cards have been designed to carry either only all-good or a mixture of all-good and partially-good components, this end-of-life card production represents a penalty in packaging density. The beginning-of-life advantage, however, more than compensates for the penalty.

Today the partially-good concept might be profitably applied to memory systems using 16k-bit chips. Not too many years ago 1k chips were just making semiconductor memory systems economical; at that time the concept would have been profitable, but not today, as those chips are being phased out. Nevertheless, 1k chips will be used to illustrate how the concept works.

Ordinarily a memory card with a capacity of 4k bytes would consist of 32 of these 1k chips, logically and perhaps physically arranged in four rows of eight, plus supporting electronic circuits. Twelve address lines would come onto the card; 10 of these would go in parallel (except for buffering) to all 32 chips. The other two would be decoded into four chip-select lines that would go to the four rows. (Alternatively, chip-select decoding is sometimes on the chip, which has two chip-select inputs.) Collectively, therefore, the 12 address lines would select a single byte of data whose eight bits would come from eight chips in a row.

To make use of partially-good chips, the card would be redesigned to hold five rows of eight chips. If one lot of 32 all-good chips was obtainable, the chips would be inserted in the four lower rows, the top row would be left empty, and the card would operate the same way as the conventional design. Otherwise, 32 partially-good chips, all with defects in the same quadrant, would be used, together with eight all-good chips. The two high order address lines would be decoded as before to give four chip-select lines for the four rows of partially-good chips. The next two address lines, the highest order of those that conventionally go to all chips on the board, instead would go to the programming jumper terminals, by which the logic states of those two lines would be routed instead to a special decoder circuit.

When a cell in a good quadrant of the chips is addressed, operation is conventional; when a cell in the bad quadrant is addressed, the special decoder disables the main array of chips and enables one quadrant of the all-good cells at the top of the array (the fifth row

of chips). One of the four all-good quadrants corresponds to the defective quadrant in each of the four partially-good rows. Clearly, only minimal electronics overhead is required on the card to accommodate partial components—two convertors and the modified chip select decoder.

The basis for computing the yield improvement resulting from using partially good chips is the yield equation

$$p = e^{-ND_oFA}$$

where N = number of mask sets in the process
D_o = defect density of the process and mask
F = fatality factor (percentage of defects that make devices inoperative)
A = area for which yield is being computed, ie, area that must be free of defects
p = probability that a chip has no fatal defects

This equation predicts very well the yield to be expected for various die sizes using metal-oxide semiconductor (MOS) processing.

If a memory chip is divided into five areas (Fig 3), the yield (probability) can be expressed separately for each area; p_s is the yield of the support circuits, and p_a is the yield of one-quarter of the storage array. The yield for that chip is the product of the five yields, or probabilities: $p_s \times p_a^4$. Yield of the chip when one quadrant of the array contains a defect is the probability that the rest of the chip is good times the probability of one quadrant being bad, or $(1 - p_a)$. Since one quadrant of the chip can be bad four ways, combined yield for all four types of chips with one defective quadrant is $4\ p_s\ p_a^3 \times (1 - p_a)$.

Curves shown in Figs 4, 5, and 6 are calculated for a memory component design in which one bit-cell has an area of 4 square mils and the support circuits are collectively 8100 mils^2 plus 0.1 of the array area (for additional decoding and sensing in larger arrays). It is also assumed that 10 fatal defects are found per square inch. This is the product of $D_o \times F$, and represents the typical level of cleanliness and mask quality for MOS processing a year ago. These figures are used to compute the yield at wafer probe testing. Yield at final test of packaged parts was a constant 80%. This is typical of the industry and to a first-order approximation is independent of the number of bits per chip.

To measure the value of yield improvements, a preliminary study is required of the cost make-up of a memory system as represented by each component within

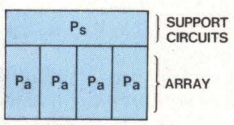

Fig 3 Calculating manufacturing yield. To determine manufacturing yield of three-quarters good memory components, the yield is computed separately for the area of the chip containing support circuits, p_s, and each quadrant of the memory cell array, p_a

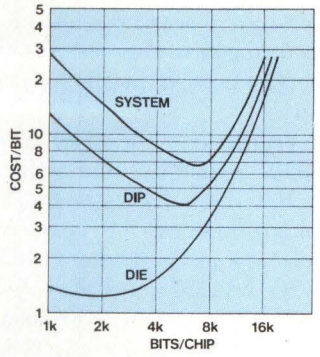

Fig 4 Cost per bit of memory. Relative cost per bit of memory at the die level, dual-in line package (DIP) level, and system level converge at high component capacities

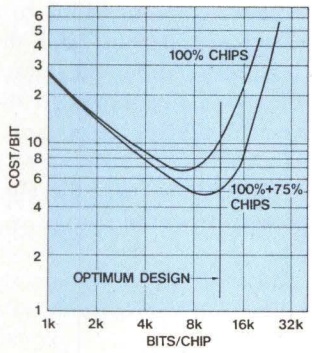

Fig 5 Cost advantages. At point of optimum design density, cost advantage at system level of using partially-good memory components is 2:1 over just using all-good components

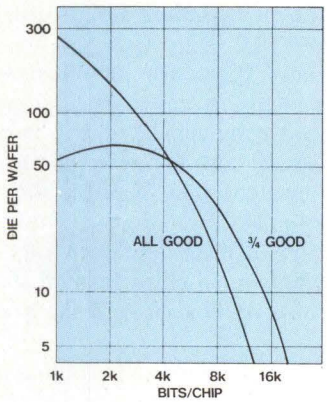

Fig 6 Die per wafer yields. At low chip capacities, yield or die per wafer of all-good components exceeds that of partially-good components because most available sites are used up by completely good components

that system. Normalized cost per bit at each of three levels—die, package, and system—shows a distinct minimum when plotted against chip capacity (Fig 4) for a given technology, a given set of design rules, and a given level of manufacturing art. However, as the number of bits per chip increases, other benefits accrue in addition to cost reduction.

Among these benefits are increases in density of the total system and in reliability, and reduction in power dissipation—the last since a large amount of the power in the system is required at the interface between the chip and the second-level packaging. Reliability, or its inverse, the failure rate, of integrated circuits (ICs) is nearly independent of the number of elements in the component because of the overriding effects of interconnection, manufacturing process, and packaging on the failure rate. In a memory with internal decoding, the number of input/output connections increases very slightly for very large increases in density. Therefore, increasing the density achieves dramatic improvements in reliability. The cost/capacity curve (Fig 4) shows the minimum cost per bit at the systems level for this particular example at approximately 6k bits/chip. Keeping in mind the previously mentioned benefits and the fact that as the technology matures and the manufacturing process improves the minimum point moves to the right on the graph, the optimum design point is more likely 10k to 12k bits/chip. At this level a very large portion of the total cost per bit is the die cost; therefore, a very significant improvement in overall system cost results from reducing die cost.

Using system cost built up from die cost, but reflecting the use of partially good components, as described previously, the combination (Fig 5) currently has a minimum point at 10k bits/chip, without waiting for a mature technology. Furthermore, at this density, the cost difference between the two approaches at the system level is almost 2 to 1. As the technology matures, this difference becomes less pronounced; eventually, there is no cost difference (as Fig 5 shows for a 2k-bit chip) at this manufacturing state of the art. Thus, the benefits of using partially-good components can be realized only when working at an optimum design density as defined by minimum cost.

Because the card types are interchangeable, the user is not constrained to use any particular mix of all-good and partially-good components or any particular mix of any certain type of partially-good components. This is an important consideration because the relative yield of three-quarter-good and all-good chips changes dramatically with the density level. At very low densities the yield of partially-good chips falls off sharply (Fig 6), because good chips occupy most of the available sites on the wafer.

This same diagram could also represent the relative yields of all-good and partially-good dice versus defect density for a particular bit density. As defect density decreases, yield of partially-good chips relative to all-good chips decreases. Since processing improves as time passes, causing the defect density to decrease, the diagram shows how yield changes with time, provided the horizontal (time) axis is read backward, from right to left.

Therefore, the mix of components at a certain density shifts with time from primarily partially-good to primarily all-good. Since the user can accommodate any mix of all-good or partially-good components, he should be able to order on a bit basis and accept any mix that is optimum for the manufacturer—who, in turn, can ship whatever distribution of parts reflects his manufacturing process. His risk of an occasional bad production run is therefore minimized. Also, as the product matures and the cost benefit of using partially-good chips diminishes, the supply of partially-good chips also diminishes.

The advantages of using partially-good chips include a cost saving of approximately 30%, reliability improvement of approximately 20%, and power savings and system size reduction of approximately 15% each. There is also an approximately 60% increase in wafer fabrication capacity. In addition to all this, the approach places no new burdens on component manufacturing or system manufacturing.

To achieve these benefits, both the semiconductor manufacturer and the user must change their ways. The manufacturer must agree to design a memory chip at a density level much higher than his previous ground rules would dictate; that is, he must design a memory component with an anticipated yield that would be unsatisfactory if only 100%-good chips were to be sold. The user, similarly, must be committed to use partially-good components; if he does not, when the parts are announced, the manufacturer may have nothing to sell.

The level of benefit achieved is also related to the size of the array relative to the size of the support circuits. The preceding example was based on the 3-transistor memory cell, no longer widely used. As the memory array size gets smaller, the manufacturer must build to higher densities to achieve the same advantage. Furthermore, in many cases, today's designs are close to the maximum power level that dual in-line packages can dissipate. Thus, to take full advantage of this approach, more emphasis must be placed on reducing power in memory components to allow the much higher densities to be achieved. These are not new requirements; they must be done anyway as memory density increases. However, to a certain extent they conflict with the goal of ease of use.

For example, using a differential current-sensing output with an external sense amplifier causes the memory array chip to dissipate much less power (and is also faster), but it is a little less convenient to use. To fully exploit the scheme at today's processing technology and circuit design level will probably require some compromises in speed to reduce the total power dissipation. However, the increase in density would reduce the signal delays in the interconnections at the second, third, and fourth levels of packaging—board, panel, and system, respectively—partially and perhaps fully compensating for the compromise in speed.

Robert H. F. Lloyd holds the BS degree in electrical engineering from Tufts University and has done post-graduate work in solid-state physics at Stevens Institute of Technology and at Syracuse University. Currently president of Conver Corp, his experience includes work in the areas of circuit design, semiconductor design, and in solid-state technology and computer electronics.

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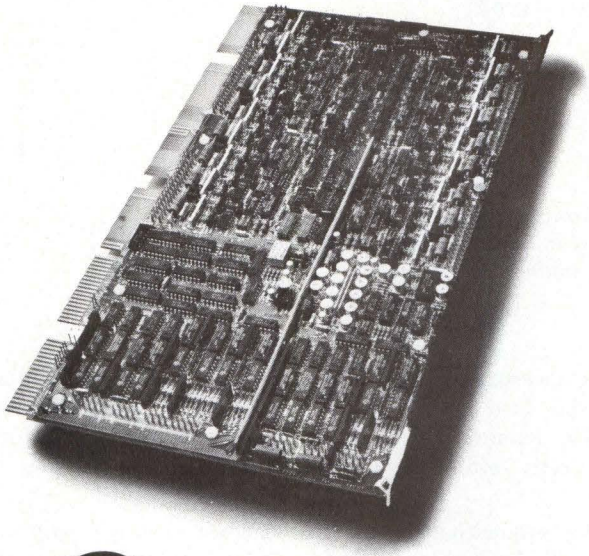

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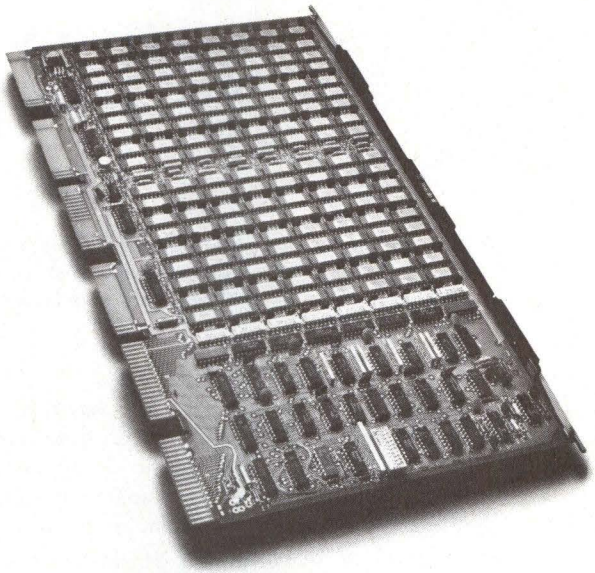

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CIRCLE 50 ON INQUIRY CARD

"Where Do We Go From Here"

MICROPROCESSOR/MICROCOMPUTER APPLICATIONS CONTEST WINNER

First Prize

Microprocessor Restroom Robot

Claude A. Wiatrowski

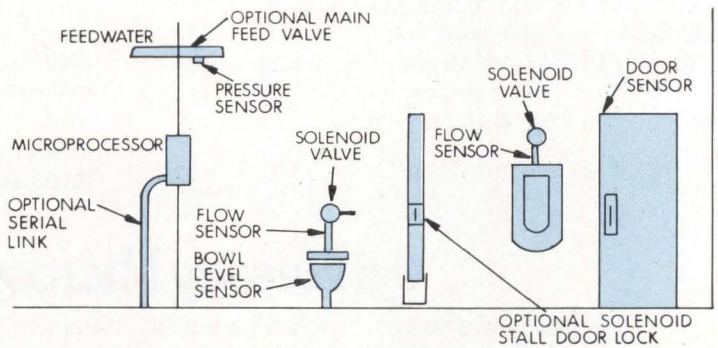
Colorado Springs, Colorado

Especially useful in large buildings, this microprocessor system saves both water and the energy needed for pumping it and treating waste, while also reducing construction costs and improving maintenance

Conservation of natural resources is of increasing importance and the microprocessor can assist in this goal in ways that are sometimes quite unusual. This application conserves water, the energy to pump it, and the energy to treat waste water. A microprocessor-implemented algorithm controls the commodes in a medium to large building to minimize the necessary water supply and resultant sewer loading. Considerable expense and increasingly scarce raw materials could be saved in new construction by the associated reduction in the size of pipes and pumps required. A maintenance monitoring feature is particularly useful in large buildings.

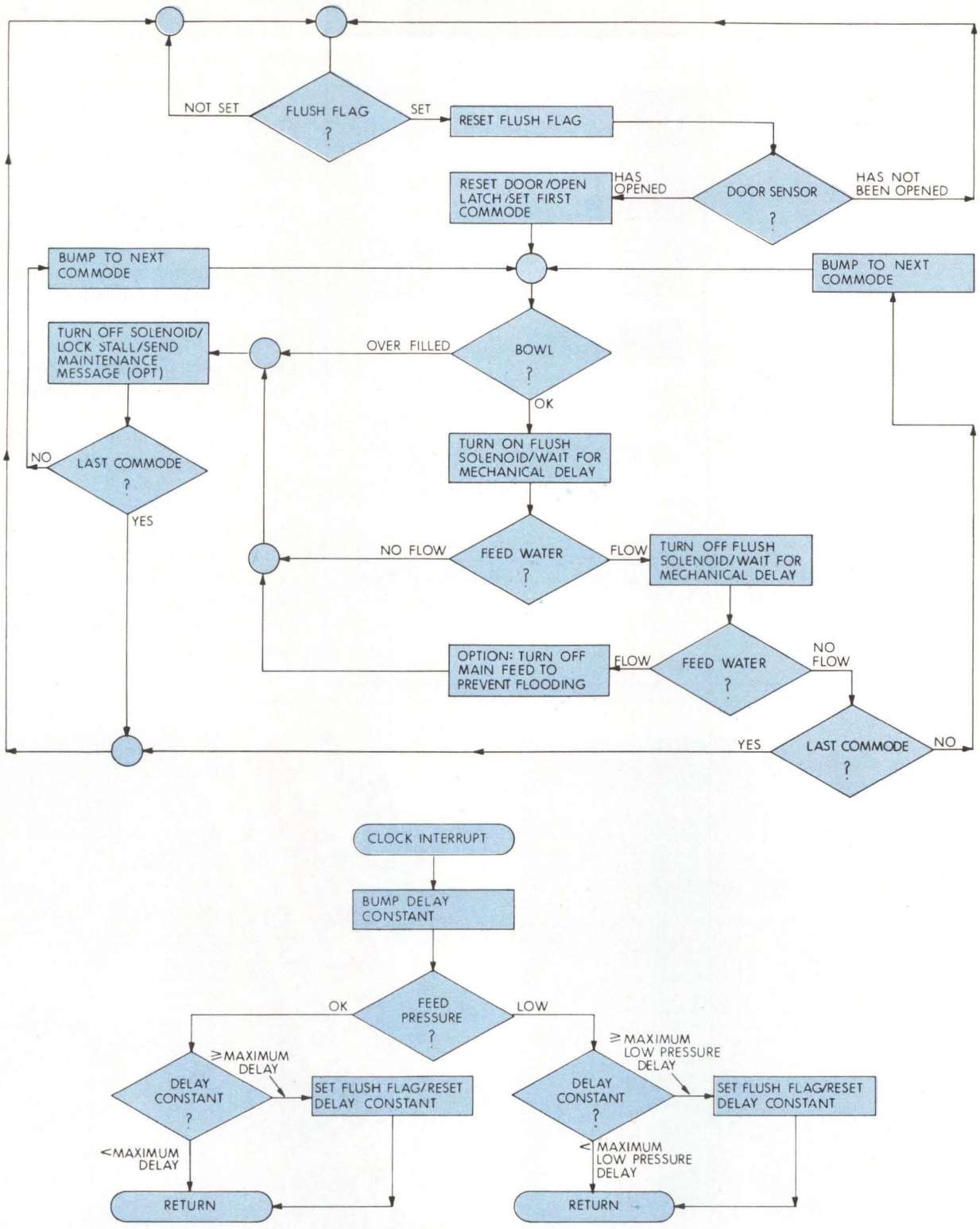
Most of us are familiar with the mechanical timers that flush urinals or commodes on a regular schedule. The microprocessor system, using one 4040 with 1k bytes of ROM per restroom, and one 8080 per building, improves on the mechanical timers by implementing a flushing schedule based on several inputs rather than just on elapsed time.

1. The microprocessor measures the elapsed time since the last automatic or manual flush, eliminating automatic flushing directly after a manual operation.
2. It flushes commodes sequentially to reduce loading on the feedwater supply and sewage system. Optionally, a multidrop serial link synchronizes several restrooms to further reduce loading on the building's systems.
3. The microprocessor lengthens the flushing cycle if feedwater pressure



Drawing illustrates various input sensors that microprocessor relies upon to provide improved maintenance and to implement a flushing schedule which conserves water and energy

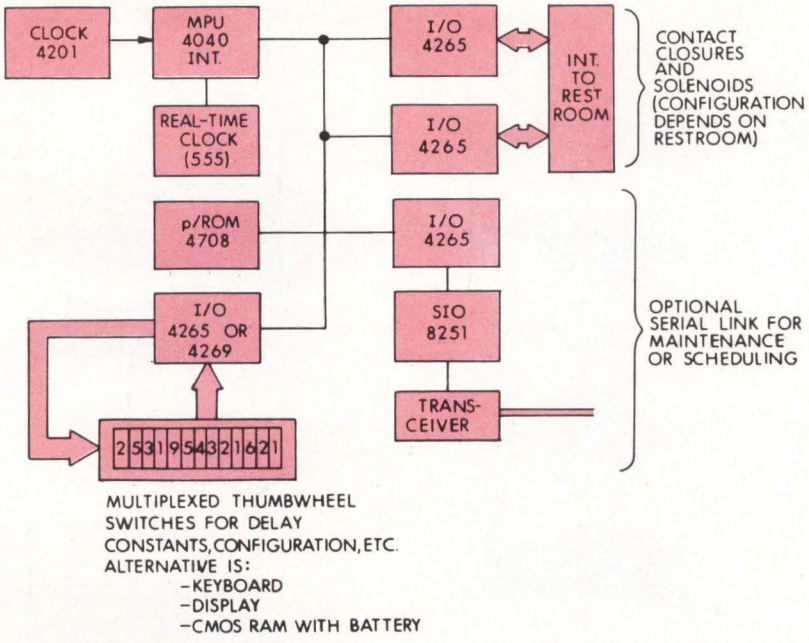
Flowchart



drops below a preset value due to excessive loading.

4. It will not flush a commode that has been flushed since the last opening of the restroom door as there is obviously no need.

5. Optionally, flushing delays could be modified by the time of day and unusual loading, such as a large meeting. This avoids flushing commodes at night in an empty office, while simultaneously allowing unusual loadings such as a John Denver concert in the ground-floor auditorium. A simple day/evening schedule might be appropriate for a small installation while a multidrop serial link could adjust delays dynamically



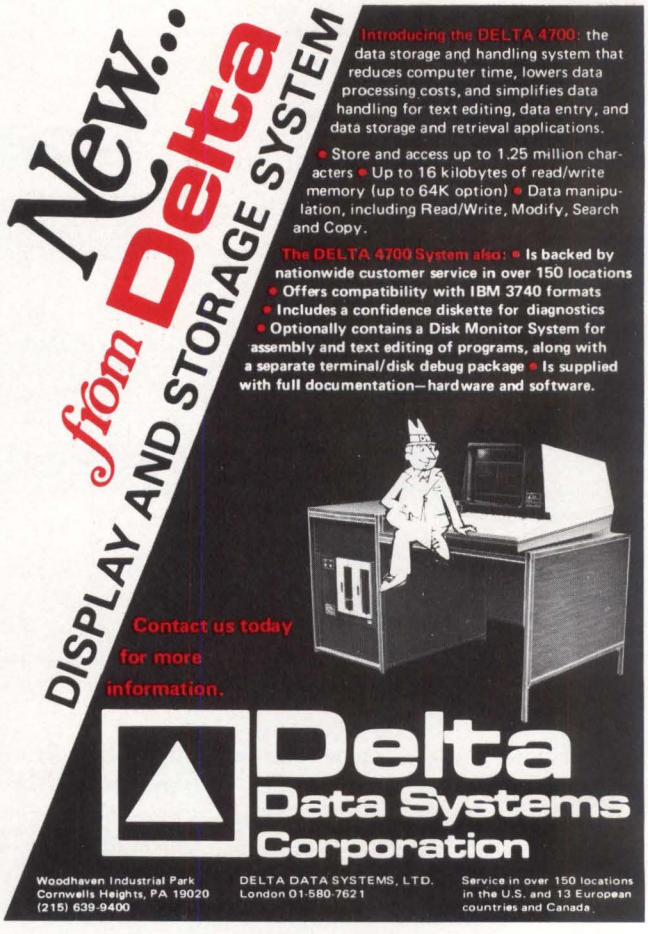
"Restroom robot," especially useful in large buildings, comprises a 4040 microprocessor for each restroom, and an 8080 for each building. Each 4040 uses 1k bytes of ROM

from a central microprocessor in a large building.

This same central microprocessor would also act as a maintenance monitor. Each feedwater pipe would be equipped with a simple flow/no flow sensor to verify proper valve action, while a bowl level sensor on commodes would detect clogged drains. Failure conditions could then be sent to the central microprocessor located in the maintenance office to be displayed on an alarm panel. Also, stall doors of malfunctioning commodes could be locked by solenoid and opened by a maintenance key (locked from the outside only, so that a computer cannot trap anyone inside with an overflowing commode).

Other additions are possible, such as routing the manual flush signals through the microprocessor to allow delaying manual commands when too many commodes would be flushed simultaneously. The above description contains many functions, some of which are duplicative. For clarity, the system detailed in the diagrams and flowcharts is a representative subset of these functions. □

CIRCLE 51 ON INQUIRY CARD



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Now, aren't you happy you didn't turn the page?

CIRCLE 53 ON INQUIRY CARD

APPLICATION NOTE

Synchronous Adapter Reduces Complexity of Floppy Disc Controller

Mark E. Eidson* and Larry A. Parker

Motorola Semiconductor Products, Incorporated
Phoenix, Arizona

Adapter for communication channels works just as well relaying data to and from a small peripheral device, and is especially suitable in a microcomputer system

Until recently, the task of designing an input/output controller for a microprocessor-based system was difficult, because development of the necessary signals required many integrated circuits. These took up much space on the printed circuit board (and cost much money).

Now, however, such controllers have been substantially simplified because of the availability of an integrated circuit (IC) designed primarily for interfaces with binary synchronous channels. Design of a typical controller for a flexible disc is outlined here. With small modifications, it may be applied to such devices as tape cassettes or cartridges, or other types of data communication channels than bi-sync. External hardware requirements for most applications are minimal, because the IC has two synchronizing signals, the function of which in other systems usually requires many additional ICs. The IC is a synchronous serial data adapter (SSDA) designated MC6852, part of the M6800 microprocessor family.

Among other advantages of the adapter are two 3-level first-in first-out (FIFO) registers, in the transmit and receive sections respectively, which allow double-byte transfer loops and faster data transfer while the microprocessor remains free for other tasks.

Basically, the adapter interchanges bit synchronous serial data in both directions with bus organized systems. Its bus interface includes select, enable, read/write, and interrupt logic, and it automatically inserts and deletes fill characters, and checks for errors. Its functional configuration is programmed from the data bus during system initialization. Programmable registers control variable word lengths, transmission, reception, synchronization, and interrupts. Status, timing, and control lines connect it to the peripheral device or modem.

Device Operation

At the bus interface, the adapter appears as two addressable memory locations. Internally, it contains seven registers (Fig 1): two for status and incoming data, two for sync code and outgoing data, and three control registers. Serial input/output (I/O) lines have independent clocks; there are also four peripheral/modem control lines.

Outgoing data are transferred directly from the data bus into the transmit data register, a 3-byte (FIFO) unit. Availability of the input to the FIFO is indicated by a bit in the status register; the first byte moves through the FIFO to the last empty location, and then is automatically transferred from the FIFO to the transmitting shift register as soon as the latter becomes available. If data are not available from the FIFO at this time (underflow con-

*Now with Courier Terminals, Incorporated, Phoenix, Arizona.

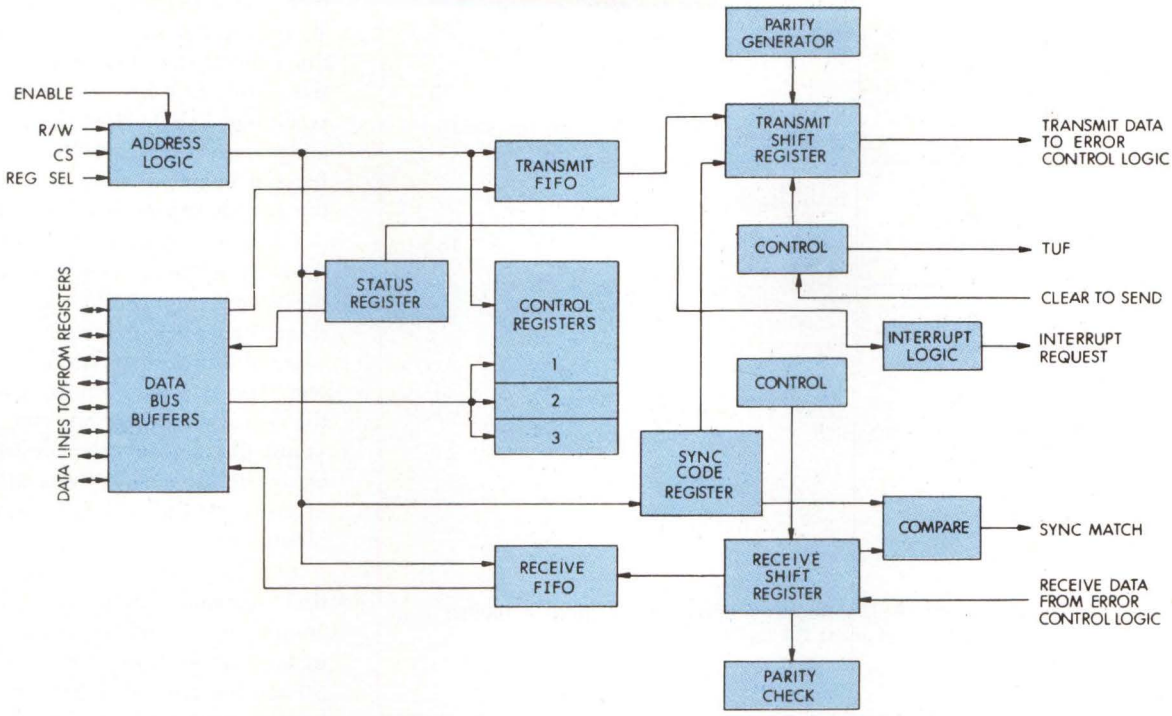

Fig 1 Synchronous adapter. This one IC, designed for use with communication lines, can also be principal element in peripheral controller for I/O equipment in a microcomputer system

dition), the shift register is automatically loaded either with a sync code or with 1s.

Incoming serial data are accumulated in the shift register under external or internal synchronization, parity is optionally checked, and data carried through the receiver FIFO to the last empty location. Availability of a word at the FIFO output is indicated by a bit in the status register, as is a parity error.

This circuit operation and status bits, in conjunction with such I/O lines as clear-to-send and data-carrier-detect, are ordinarily applied to data communication. They are also useful when the unit at the far end of the line is actually only a few feet away (in which case no data carrier is employed). However, two additional lines, called transmitter underflow (TUF) and sync match, permit the adapter to work with higher speed serial synchronous devices.

For example, its application to a controller for a floppy disc drive is economical because the drive and microcomputer are easily synchronized with the aid of these two lines (Fig 2). The controller design is completely flexible, defining all recording characteristics and the disc format in software. Double-density and minidisc formats can be made compatible by appropriately changing the system clocks, and data recovery and formatting circuits.

Recording Format

Format of the data recorded on a flexible disc is controlled by the host system. In one approach, compatible with the IBM 3740, data are recorded on the disc using double frequency encoding, in which each data bit, whether 1 or 0, is preceded by a clock bit, almost always 1. The system may record one long record or several shorter records in a single track. A physical index pulse and an index address mark start each track, and a unique recorded identifier, or address mark, precedes each record.

These address marks are the only places on the disc where clock bits are sometimes 0—namely, in bit cells 2 and 4 of the index address mark and in bit cells 2, 3, and 4 of the record identifier and data address marks.

Gaps separate the data records from their identifiers. The number of records per track and their lengths are established by the format prerecorded on the track, which can be altered by software. All tracks on a single disc have one track format (ie, record size and gap size), but different discs can have different track formats.

IBM compatibility requires data to be transferred most significant bit first, while standard data communication protocol transfers the least significant bit first. The adapter's design is compatible with the latter, but it can be rendered IBM-compatible by simply reversing the order of the data bus lines at the adapter. This also reverses the bit positions of the

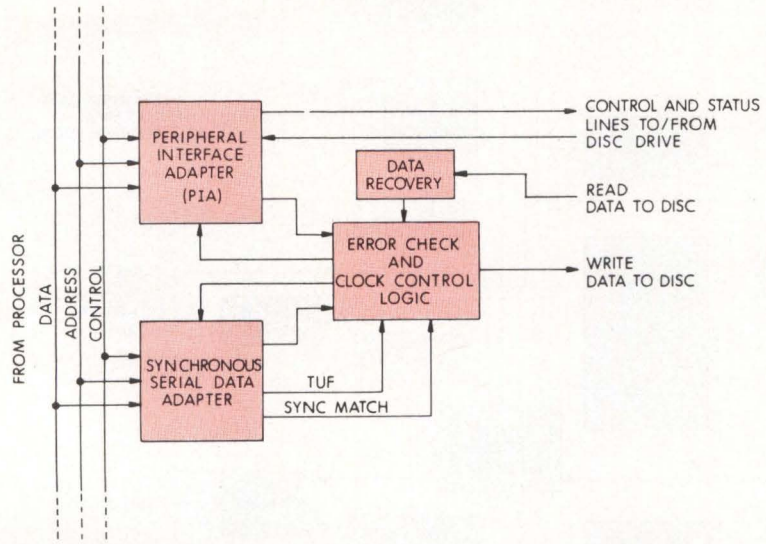

Fig 2 Small controller. SSDA requires minimum of other circuits in controller application—at most 30 to 35

data control and status registers of the adapter from those shown in the data sheet. Since parity bits are not used in flexible disc interfaces, the reversal creates no new problems; however, it must be used with caution in other systems requiring parity.

Data Recovery Circuit

Data recovery in the SSDA-based controller generates timing pulses at regular 2-μs intervals and separate data-only signals on a parallel line, also at a 2-μs rate. These rates are maintained regardless of small departures from the nominal 2-μs rate in the data being read from the flexible disc, which are inevitable in high density recording, while tracking larger, slower changes caused by failure of the revolving disc to maintain an absolutely constant speed. Recovery is governed by a voltage-controlled oscillator (VCO) with a nominal frequency of 8.0 MHz.

The circuit comprises, in addition to the VCO, four D flip-flops, two divide-by-16 counters, a detector and filter, and an 8-bit shift register. Flip-flops generate a clock signal derived from incoming data, stretch it into a pulse representing the data more accurately timed, and translate it into an NRZ format—which is also run through the shift register to delay it and thus permit synchronizing bytes to pass through the error-checking logic ahead of it. One of the counters, preset to 9 by every clock pulse, and counting VCO pulses from that point, generates a carry at count 16; the other counter, not present, generates a carry routinely after every 16 VCO pulses. The detector compares these two carries in frequency and phase; if they drift relative to one another, the detector and filter adjust the VCO frequency to compensate for the drift.

Read Operation

When the disc is spinning at its nominal speed, and when the seek operation has been completed and the head pressed down against the disc, a continuous stream of bits and clock pulses arrives at the controller, waiting to be recognized. A read command from the system places the first half-byte of the address mark in the sync code register, one of the seven registers in the adapter previously mentioned, and enables the receiver section. Contents of the sync code register are continuously compared with the bits in the data stream. Both data and clock bits are monitored, at a nominal rate of 500 kHz. When register bits match stream bits, the sync match line comes up, and the second half-byte is checked in the receiving FIFO. Both halves of the address must match before data transfer can begin; if they do not match, the search sequence is restarted.

Upon recognition of the full address byte, the external circuits switch the clock rate to 250 kHz so that thereafter only data pulses are recovered for transmission to the system. The external circuits also control the error-checking circuits, if any (most disc formats include two cyclic error-checking code bytes at the end of every data record and every record identifier).

External logic includes circuits that respond to the system's read command, a latch to store the sync match signal from the adapter, and a latch to gate either 250 or 500 kHz to the adapter. Control signals originate in the system peripheral interface adapter (PIA), also part of the external logic. Meanwhile, the data recovery circuit separates the read data and generates the 500-kHz clock pulses to the read data logic.

Recognition of the record identifier, as described previously, causes sync match to rise and read data to enter the receiving FIFO in the adapter. This record identifier comprises the bit pattern 1111 1110 plus the interspersed clock bits, which have not yet been switched out of the data path; the complete pattern is therefore 1111 0101 0111 1110, expressed in hexadecimal notation as F5 7E. This pattern includes the three 0 clock bits that are characteristic of the record identifier. Sync match rises when F5 has been recognized in the adapter, but eight more clock pulses arrive and store the pattern 7E in the FIFO before the clock rate switches to accept only data bits. These enter the FIFO; when its second and third locations are full, the status register bit indicating receiver data available is turned on, and data can be read by the system.

Write Operation

The TUF signal is generated once every eight clock pulses—that is, once

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every 16 μs—when the transmitting FIFO register and transmitter shift register are both empty. Upon receipt of a write command from the system, the gap pattern, both clock and data bits, is stored in the sync code register and the transmitter section is enabled. At this point, the SSDA begins to transmit the gap pattern and emit TUFs, which repeatedly reset a divide-by-16 counter also driven by the 500-kHz clock. About two-thirds of the way through the gap before the address mark, the write gate turns on, writing the six bytes of continuous gap prior to the address mark of the data record being updated. While TUFs are being generated, the clock is running at double frequency as at the start of the read operation—so 12 TUF pulses count off enough space in the gap to hold six bytes. At this point, the first half of the address mark is stored in the transmitting FIFO and moves into the shift register.

This stops the sequence of TUF signals, permitting the divide-by-16 counter to continue counting. Its output consists of four lines labeled Q_0 through Q_3, which count the input signal in binary—Q_0 at half the clock frequency, Q_1 at one-quarter, and so on. The lowest frequency line, Q_3, did not have a chance to rise as long as TUFs kept resetting the counter; but when the TUFs cease, Q_3 rises, enabling the error-checking logic, and via several logic stages directs the half-frequency clock (250 kHz) to the adapter. As this happens, the second half of the address mark enters the FIFO. Data to be written on the disc follow close behind, and are gated also to the CRC circuit, which generates the error-checking bytes to be written at the end of the record. Two dummy bytes are stored in the FIFO and are transmitted from the SSDA as the error-checking bytes are written.

Conclusion

Thus all necessary functions of a floppy disc controller can be implemented with about 30 to 35 ICs in addition to the basic synchronous adapter. All are conventional small- and medium-scale ICs available from many sources, and can be easily laid out on a single relatively small printed circuit board. □

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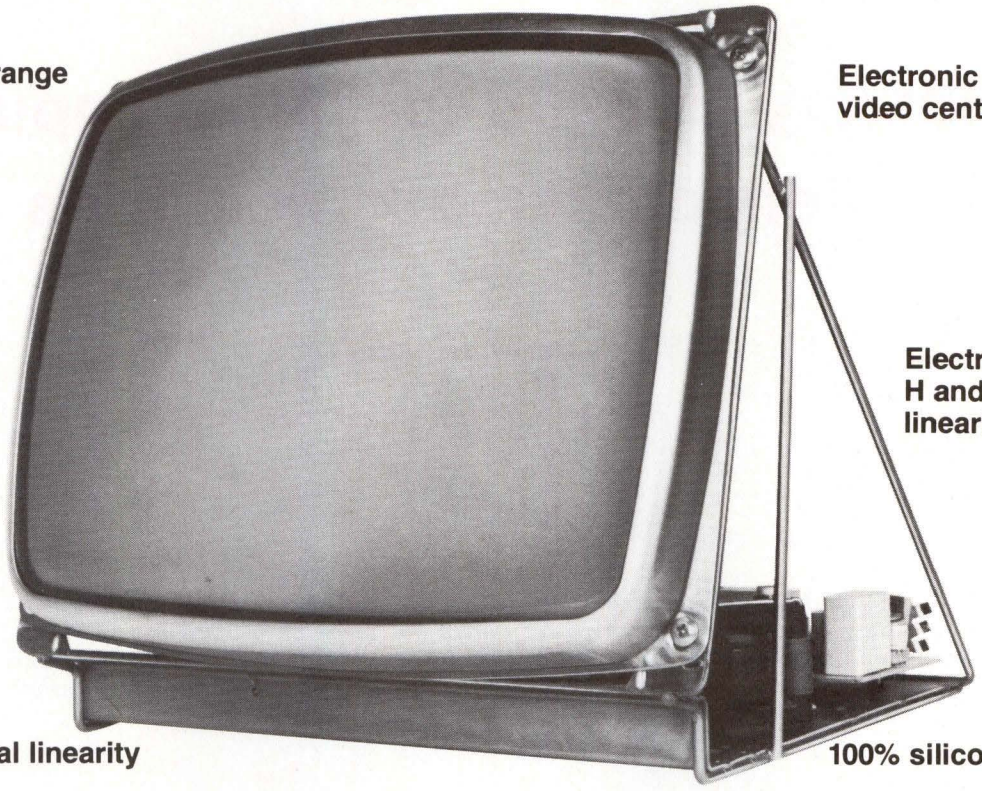

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CIRCLE 56 ON INQUIRY CARD

APPLICATION NOTE

Battery Backup for Minicomputer Semiconductor Memories

Jerry Washburn

Computer Automation, Incorporated
Irvine, California

Since data loss cannot be tolerated in most minicomputer applications, battery backup for primary power failure has taken on increasing significance with the advent of low cost, but nonretentive, semiconductor memories. Some decision-making guidelines are offered for matching memory retention needs to available battery types

Unlike magnetic core, semiconductor memories are volatile and have no data retention when power is interrupted or removed. In many cases, a power failure can be disastrous when operating in a real-time environment due to loss of intermediate results that cannot be regenerated without complete reruns from the last checkpoint. Solution to this memory retention problem is to provide battery backup capability in case primary system power is interrupted. However, while the battery backup solution seems simple enough, it often raises more questions than answers.

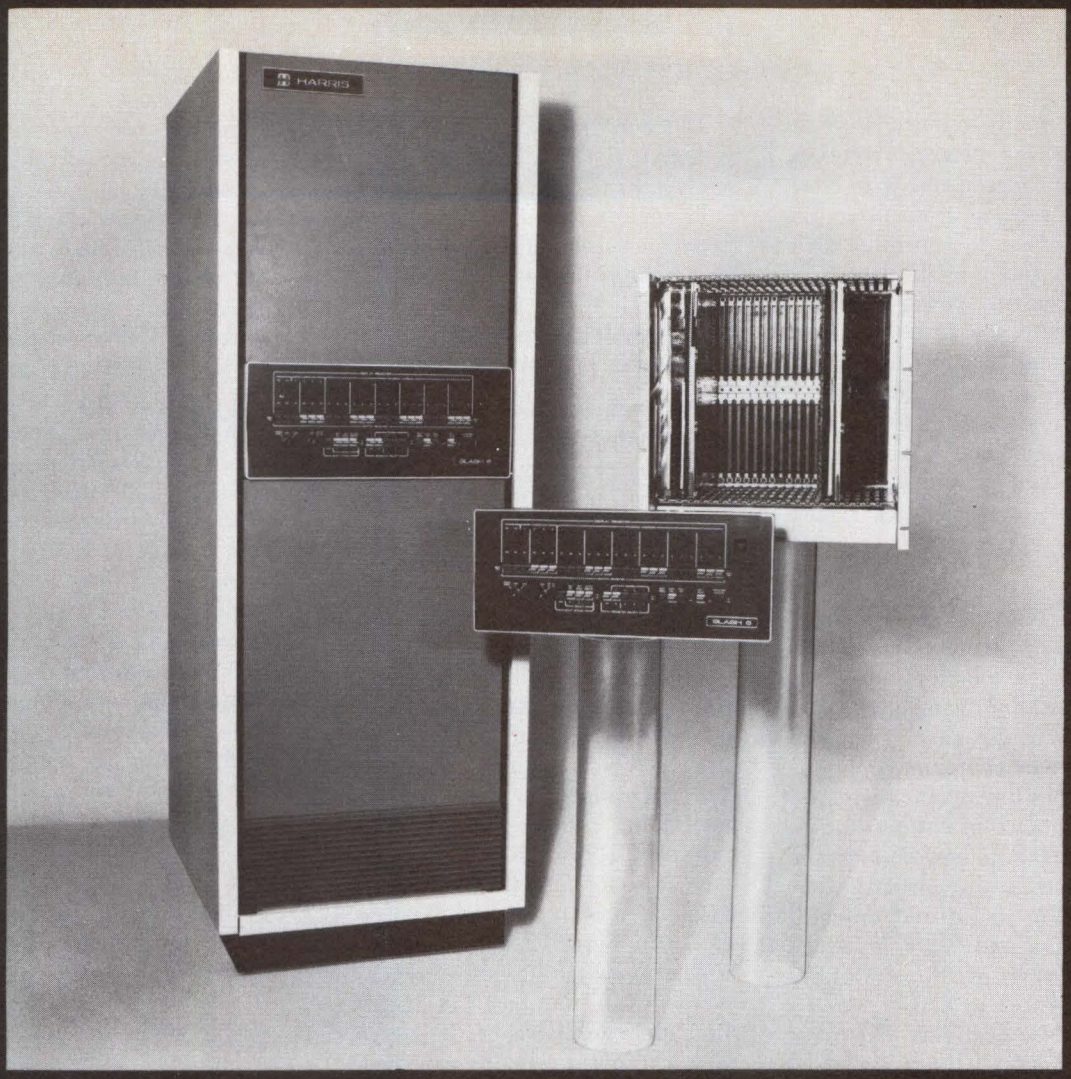
Many potential applications of semiconductor memory remain dormant due to the mystery and misunderstanding of battery backup. To clarify this situation, the user should ask the following questions about battery backup: What type of battery do I purchase; what voltage; what size; how long will it last; what type of battery charger is needed; is the battery protected, or is it switched automatically during a power failure; and what is the total cost?

Since minicomputer manufacturers are not primarily in the battery business, they cannot effectively cope with the many different electrical and packaging considerations that are dependent on the user's application. Most manufacturers provide auxiliary terminals on their memory products for connection to the user-supplied backup battery. A few manufacturers incorporate a small onboard battery to provide minimum retention power for certain types of semiconductor memory. While this is useful when system power is momentarily interrupted, it is not ideal for all applications. Each user must accurately define individual power backup requirements from power application, site, servicing, and environmental points of view to assure optimum backup battery selection.

Battery backup for semiconductor memory has been jokingly related to attaching several old car batteries, associated electronics, and cabinetry, and transporting the system to the local service station once a week for a checkup. However, in reality, a proper backup battery is effective, economical, and reliable. To assist the user in making the correct choice, brief descriptions are offered that cover semiconductor memories, battery types, battery charging, and additional support options.

Memory Types

Semiconductor memories are available in both static and dynamic MOS, and each type requires different backup battery considerations. Static



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memories normally require a single voltage source for memory retention, while dynamic memories are more complex and require up to three different voltages to operate their timing, logic, and refresh circuits.

Typical backup power requirements for an 8k by 16-bit dynamic memory module is approximately 5 W, while a typical 8k by 16-bit static memory module requires four times as much power. Some manufacturers provide onboard power-saving circuits for static memories that reduce power to the 4-W range.

Battery Types

Although many battery types are commercially available, such as LeClanche, alkaline manganese, mercuric oxide, zinc air, silver zinc, lead acid, and nickel cadmium, only the latter two types have gained wide industrial acceptance in uninterruptible power systems. Standard commercial lead acid batteries are rechargeable, are available in sealed and unsealed configurations, and have expected battery lifetimes of three to five years. Cost is $15 to $60 depending upon exact specifications. The most popular lead acid battery is sealed gelled electrolyte type, which requires no adding of liquid or checking of liquid levels. This type battery is small, compact, and mountable in any physical position, such as tilted or inverted. Most lead acid batteries are temperature tolerant, and usually exceed environmental requirements of the computer system. However, adequate ventilation must be considered for unsealed batteries during fast charging, as hydrogen and oxygen gases frequently are released and could cause an explosion if a spark is introduced. Also, lead acid batteries need undervoltage protection to prevent irreversible battery damage during excessive or deep discharge.

Nickel cadmium (Ni-Cd) batteries are effectively utilized where long battery life is required; they generally are small in size and have a battery lifetime of nine to 12 years. This battery is maintenance free, emits no gas during operation, and can be installed in any physical position without affecting its performance. However, the price of Ni-Cd batteries is much higher than that of conventional lead acid batteries.

The most popular backup battery voltage is 6 V, which is used in most semiconductor memory applications. Full environmental and application data can be obtained from most battery manufacturers.

Power Calculations and Battery Charging Methods

Ampere-hour rating of a battery can be determined for a specific requirement by multiplying the number of desired hours of memory retention life by the memory standby (or retention) current requirements in amperes; then, to provide a safety margin, the next larger commercially available size should be selected.

Small commercial battery chargers are available for as little as $12, if not supplied by the minicomputer manufacturer. However, commercial chargers cannot be used indiscriminately; for instance, a Ni-Cd battery requires a slow charge by a constant current source. A simple diode and resistor constant current source is shown in Fig 1. Proper charge rate is determined by dividing by 10 the current drain rate that will discharge the battery in one hour. This type of slow charger normally can be left connected to the battery for long periods of time without damage.

Faster charging is possible using a split-rate charge technique, as follows. The battery is initially charged at a fast rate. Then, at an appropriate time (generally when the battery goes into overcharge), charging is switched to a low rate. This low, or trickle, rate must be chosen so that the battery can withstand being charged indefinitely at this rate. The fast charge technique is ideal for applications requiring many partial or complete discharges per day.

Fastest and most efficient method for charging lead acid batteries is with a constant voltage source. Magnitude and current capabilities of this source dictate the period of time needed to charge the battery. A simple constant voltage source is diagrammed in Fig 2. Battery manufacturers usually supply application notes for all types of chargers, complete with schematics and parts lists. Commercially available automotive battery chargers should not be used because they do not include a voltage regulator and could cause severe memory damage or reduced battery life.

A typical example of a backup battery for a demanding application is a lead acid battery rated at 300 Ah. This battery would provide a 4k by 16-bit memory module with emergency power for five to six weeks, and would have sufficient capacity to withstand short power interruptions, as well as brownouts and blackouts.

Generally sufficient for most memory applications is a backup battery capacity of 6 Ah. This lead acid battery occupies less than 2 x 3 x 3″ (5.08 x 7.62 x 7.62 cm) and pro-

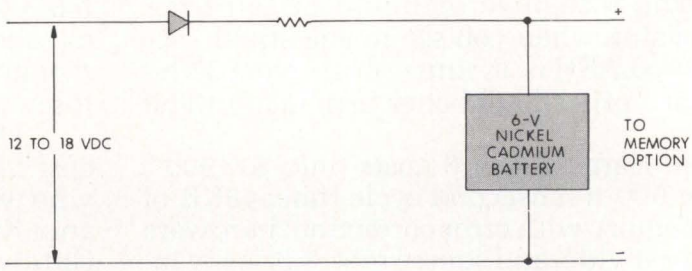

Fig 1 Schematic of simple resistor-diode constant current battery charger for a Ni-Cd battery. Value of resistor and dc source voltage determine charge current rate, and diode provides source isolation. For slow charging, charge rate is 1/10 of current drain rate that will discharge battery in 1 hour

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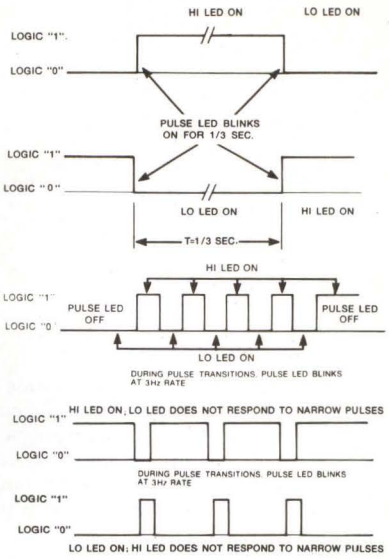
By setting the PULSE/MEMORY switch to MEMORY, single-shot events as well as low-rep-rate events can be stored indefinitely.

While high-frequency (5-10MHz) signals cause the "pulse" LED to blink at a 3Hz rate, there is an additional indication with unsymmetrical pulses: with duty cycles of less than 30%, the LO LED will light, while duty cycles over 70% will light the HI LED.

In all modes, high input impedance (100K) virtually eliminates loading problems, and impedance is constant for all states. LP-1 also features over-voltage and reverse-polarity protection. Housed in a rugged, high-impact plastic case with strain-relieved power cables, it's built to provide reliable day-in, day-out service for years to come.



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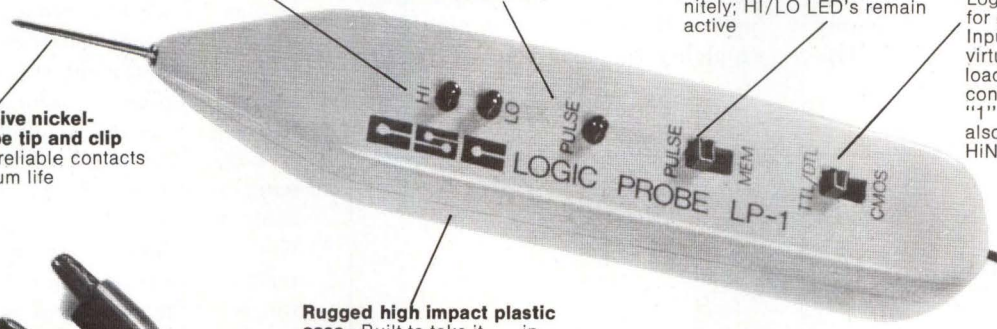

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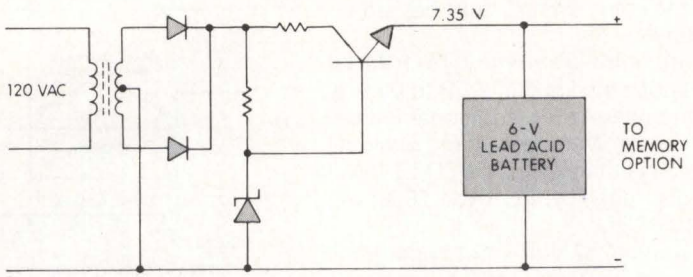


Fig 2 Schematic of simple constant voltage charger operating from 120-Vac source. Circuit can charge lead acid batteries. Rectification is accomplished using two diodes; transistor provides regulation with constant potential of 7.35 V. Regulator should provide charging current of six times current drain rate that will discharge battery in 1 hour

vides three to five hours of emergency service.

Battery Backup Options

Several minicomputer manufacturers now offer battery backup options to support their semiconductor memory products. A small Ni-Cd battery with automatic electronic switching and charging circuits is commonly mounted on the memory module. Onboard options may also contain circuits to detect and notify the minicomputer when the memory receives insufficient power from both primary and battery backup sources. Terminals are sometimes provided for external batteries when greater backup capabilities are required.

Multiple memory modules can be configured to operate from a single battery if the battery is capable of supplying the total current requirements. This battery option provides a minimum of two to 16 minutes of memory retention power and contains undervoltage protection and power-saving circuits. The latter circuits include a power oscillator to reduce backup power requirements. This is accomplished by a 10 to 20% duty cycle of pulsed power, which is sufficient to retain memory data while reducing normal power consumed by 80%. Using this technique, battery size and cost are both significantly reduced. This backup battery draws less than 0.5 A when primary power is off, and no current when primary power is available. Onboard battery backup capability can be expanded by connecting an external 6-V battery and charger. Ampere-hour rating of the external battery is determined by multiplying the number of backup or standby hours required by 0.5. External battery charging considerations are similar to those previously described.

Dynamic metal-oxide semiconductor random-access memories typically require three voltages for refresh cycle operation: 5, 12, and −5 V. To meet these increased demands, a dc-to-dc converter and regulator can be incorporated to reduce the number and type of batteries required. In this manner, a single common 6-V battery supplies all voltage and current requirements. An option of this type can be installed within the computer power supply to save costly equipment space. This option provides a minimum of three minutes of memory retention power for 16k words of memory and six minutes for 8k words of memory. It includes a small, internal Ni-Cd battery complete with charger, electronic switching, and external expansion capability. When it is desirable to utilize the external expansion capability, users can connect any size 6-V lead acid or Ni-Cd battery. To add rechargeability, a battery charger can be connected externally as shown in Fig 3.

It is recommended that backup battery options be utilized, even when an external battery and charger must be added to extend basic memory retention time. This is because power saving, voltage sensing, failure detection, and automatic switching are difficult to mechanize externally to semiconductor memory modules and related minicomputer equipment. □

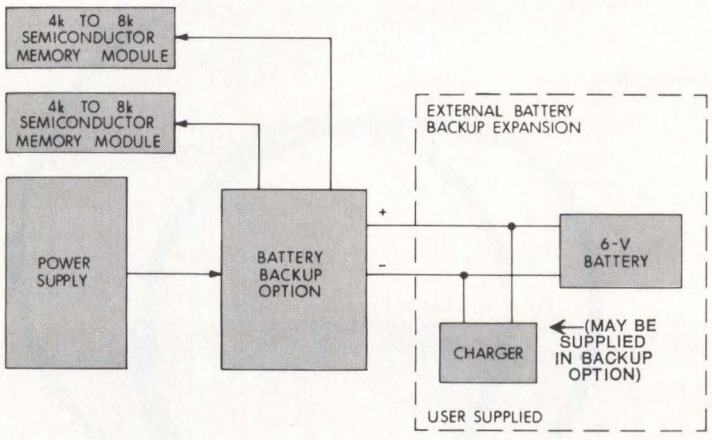
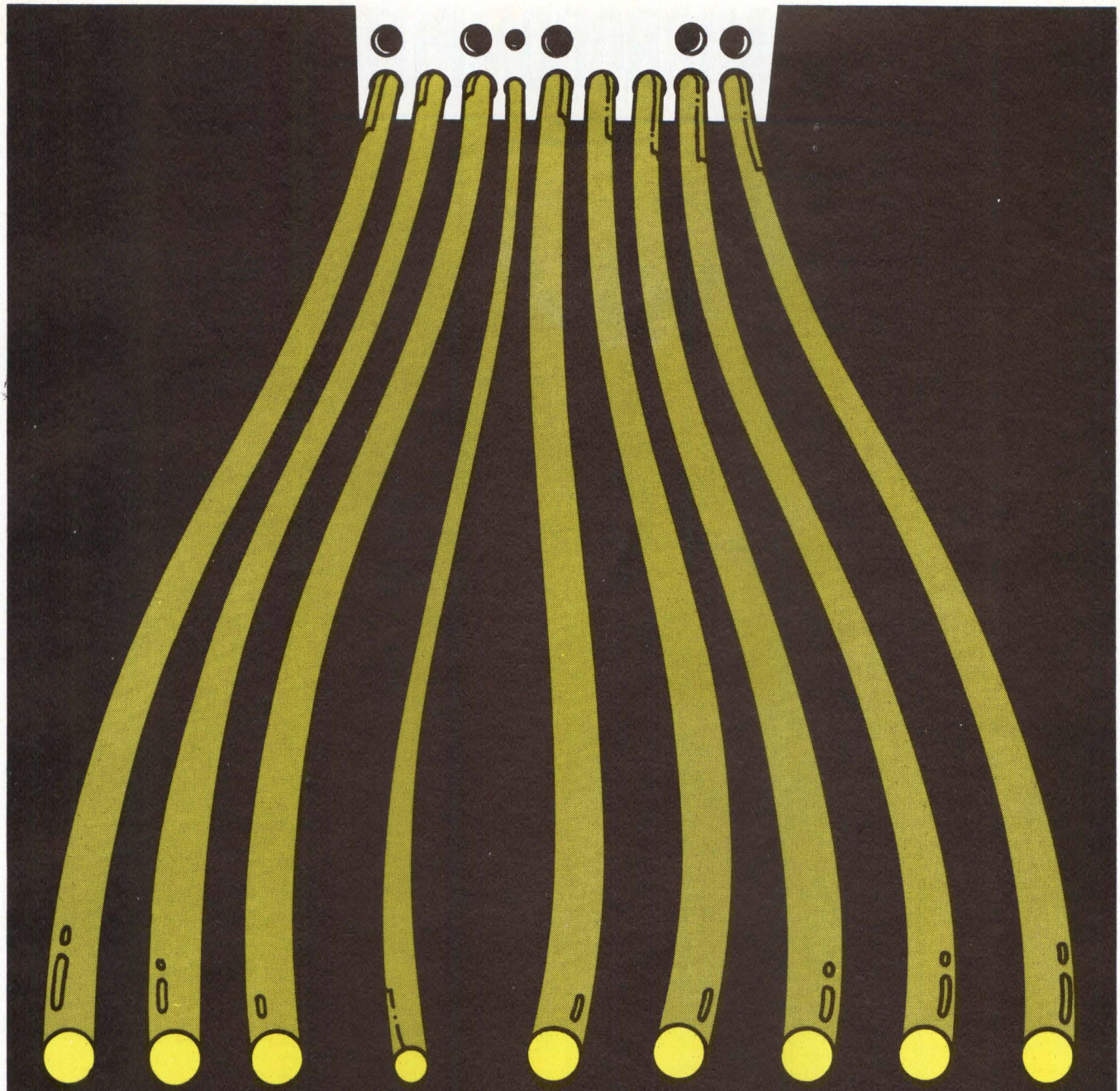


Fig 3 Block diagram of typical battery backup option for minicomputer dynamic semiconductor memories. Option usually provides several minutes of memory data retention when power is interrupted or removed. Backup capabilities can be expanded to increase desired memory retention time by adding external battery and charger



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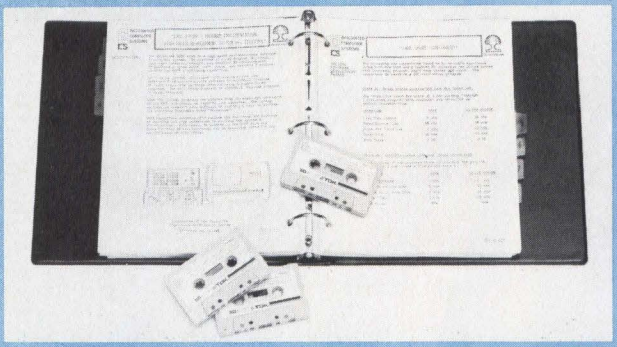

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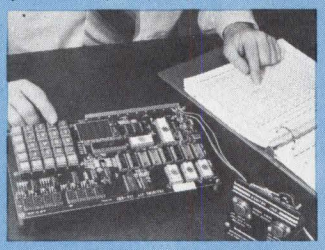

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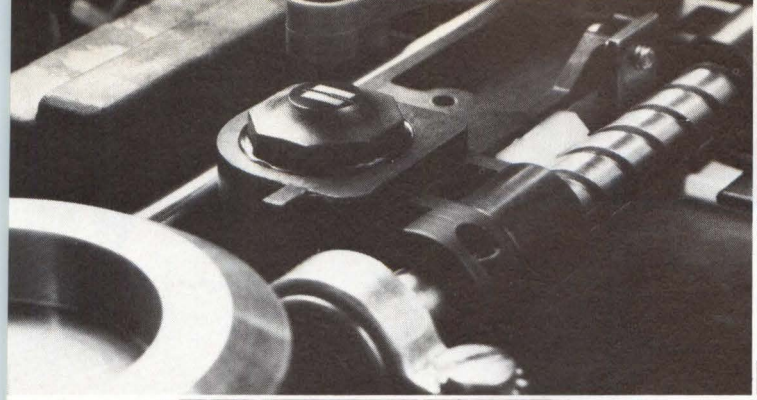

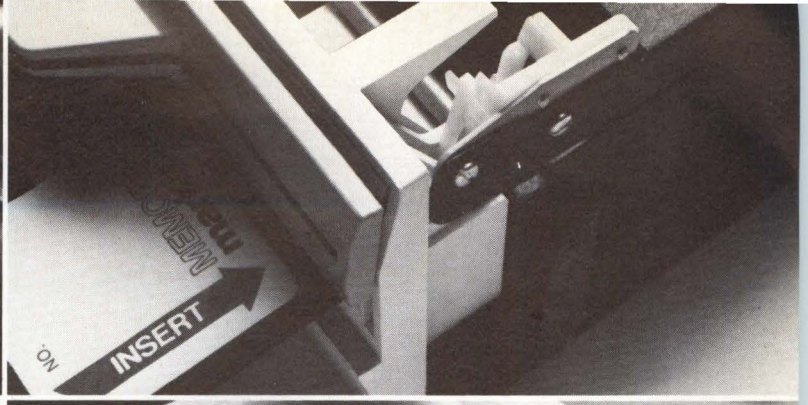

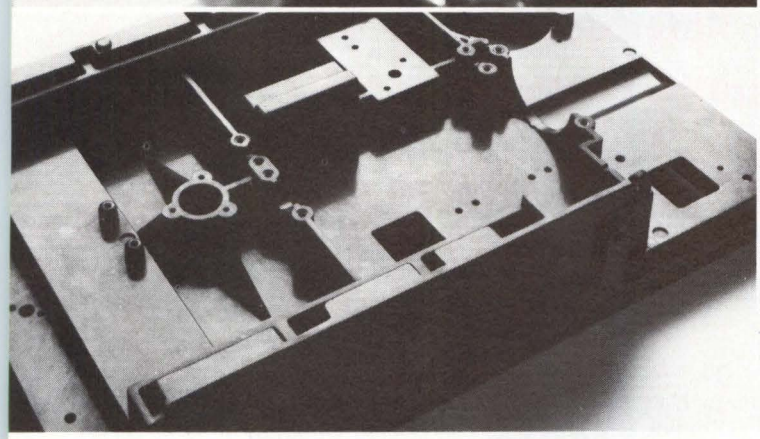

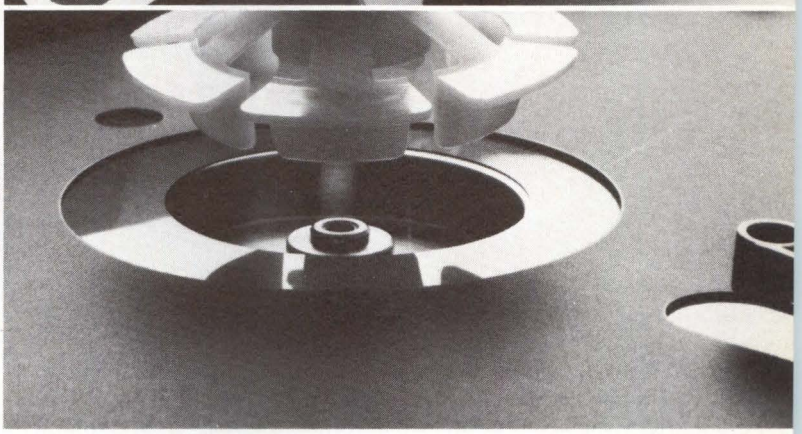

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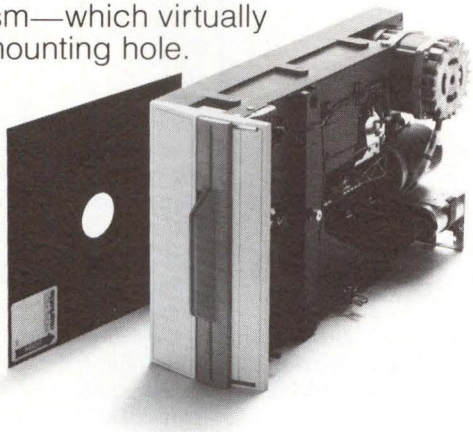

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CIRCLE 60 ON INQUIRY CARD

Microcomputer Interfacing: What Is a Logical Instruction?

Peter R. Rony
Virginia Polytechnic Institute & State University

David G. Larsen
Virginia Polytechnic Institute & State University

Jonathan A. Titus
Tychon, Inc

Most microcomputers manipulate information eight bits at a time. For example, the 8080A chip can move eight bits from internal register to internal register, from internal register to memory, and between the accumulator and an external I/O device. It can also perform arithmetic and logical operations, the former including add, subtract, and compare, and the latter including AND, OR, exclusive-OR, and complement. This month's column will cover logical operations.

Basic rules governing 1-bit logic operations are truth tables. A truth table can be defined as a tabulation that shows the relation of all output logic levels of a digital circuit to all possible combinations of input logic levels in such a way as to characterize the circuit functions completely.* Truth tables for the AND, OR, exclusive-OR, and complement operations are:

AND

B	A	Q
0	0	0
0	1	0
1	0	0
1	1	1

OR

B	A	Q
0	0	0
0	1	1
1	0	1
1	1	1

Exclusive-OR

B	A	Q
0	0	0
0	1	1
1	0	1
1	1	0

Complement

A	Q
0	1
1	0

These are 1-bit truth tables because the data words A and B each contain only a single bit.

It is useful to employ Boolean symbols when discussing logic instructions. Such symbols originate from the subject of Boolean algebra, which is the mathematics of logic systems. Alphabetic symbols such as A, B, C, . . . Q represent logical variables, and 1 and 0 represent logic states. Originated in England by George Boole in 1847, this particular form of mathematics did not become widely used until 1938, when Claude Shannon adapted it to analyze multicontact networks for telephone networks.

Basic Boolean symbols are used in Boolean algebra computations, and thus all digital logic. These symbols include:

- $+$ which means logical addition and is given the name OR
- $\cdot$ which means logical multiplication and is given the name AND
- $\oplus$ which is given the name exclusive-OR or XOR
- $\overline{A}$ which means negation and is given the name NOT

The negation symbol is a solid bar over a logical variable such as A, B, . . . Q. Thus, the Boolean statement for a 2-input AND gate is $Q = A \cdot B$, or simply $Q = AB$, where the equality symbol $(=)$ means that variables or groups of variables on either side of the $=$ symbol are the same, ie, both are in the same logical state. It is useful to summarize the symbol operations for the three gates under consideration:

AND	OR	Exclusive-OR	Complement
$0 \cdot 0 = 0$	$0 + 0 = 0$	$0 \oplus 0 = 0$	$\overline{0} = 1$
$0 \cdot 1 = 0$	$0 + 1 = 1$	$0 \oplus 1 = 1$	$\overline{1} = 0$
$1 \cdot 0 = 0$	$1 + 0 = 1$	$1 \oplus 0 = 1$	
$1 \cdot 1 = 1$	$1 + 1 = 1$	$1 \oplus 1 = 0$	

Multibit logic operations are treated as many 1-bit logic operations. No new principles of logic are involved. Corresponding bits of one binary word logically operate on corresponding bits of the second binary word to produce an overall multibit logic result. Length of binary words can be any number of bits: two, eight, 32, etc. Since the 8080A microprocessor performs multibit logic operations on 8-bit words, all of our examples will involve full bytes.

Consider the 8-bit logic variable A. Individual bits in this variable can be labeled as A7, A6, A5, A4, A3, A2, A1, and A0, with A0 being the least significant bit (LSB), the 2^0 bit, and A7 being the most significant bit (MSB), the 2^7 bit. Also consider the 8-bit logic variable B, with individual bits labeled B7, B6, B5, B4, B3, B2, B1, and B0. The logic operation, $A \cdot B = Q$, involves the following eight 1-bit logic operations:

$A0 \cdot B0 = Q0$
$A1 \cdot B1 = Q1$
$A2 \cdot B2 = Q2$
$A3 \cdot B3 = Q3$
$A4 \cdot B4 = Q4$
$A5 \cdot B5 = Q5$
$A6 \cdot B6 = Q6$
$A7 \cdot B7 = Q7$

The result of the logic operation is the logic variable Q, which has an LSB of Q0 and an MSB of Q7. In other words, multibit logic operations are performed bit by bit via a series of 1-bit logic operations. It is easier to perform multibit logic operations if the multibit binary words are

*R. F. Graf, *Modern Dictionary of Electronics*, Howard W. Sams & Co, Indianapolis, Ind, 1972

Listing of Logic Information for System of Eight Devices

Bit Position	Device	Logic State Information
Bit 0	Pressure sensor	1 = pressure above setpoint 0 = pressure at or below setpoint
Bit 1	Temperature sensor	1 = temperature above setpoint 0 = temperature at or below setpoint
Bit 2	Velocity sensor	1 = velocity above setpoint 0 = velocity at or below setpoint
Bit 3	Flow rate sensor	1 = flow rate above setpoint 0 = flow rate at or below setpoint
Bit 4	Concentration sensor	1 = concentration above setpoint 0 = concentration at or below setpoint
Bit 5	Valve A	1 = valve A open 0 = valve A closed
Bit 6	Valve B	1 = valve B open 0 = valve B closed
Bit 7	Power	1 = power on 0 = power off

placed one under the other. Thus, if A = 11011111_2 and B = 00100011_2, A • B is

$$\begin{array}{r} 11011111_2 \\ \bullet\ 00100011_2 \\ \hline 00000011_2 \end{array}$$

or Q = 00000011_2. We have performed a logical AND, and have used the relationships $0 \bullet 1 = 0$ and $1 \bullet 1 = 1$ in deriving the final result.

One of the more important uses for multibit logic operations is in situations in which the on/off state of external devices must be monitored. Consider the system of eight devices listed in the panel. The group of eight bits can be called the status byte for our system of eight devices. At any instant, the status byte will have a specific value. For example, status byte 11100010_2 signifies that pressure is at or below the setpoint, temperature is above the setpoint, velocity is at or below the setpoint, etc.

The importance of logical instructions in a digital computer is that they permit the user to determine the following characteristics about the external devices previously listed.

- Which devices are on, open, or above the setpoint?
- Which devices are off, closed, or at or below the setpoint?
- Since the last time we checked, which devices have gone from on to off, open to closed, or above the setpoint to at or below the setpoint?
- Since the last time we checked, which devices have gone from off to on, closed to open, or at or below the setpoint to above the setpoint?

In other words, by using logical instructions it is possible to determine not only the current state of the external devices, but also what changes have occurred since the last time that the devices were interrogated. Since it is not clear how this is done logically, we will discuss a specific example based upon the eight devices described above.

Assume that we have just interrogated all eight devices and have found the current status byte to be 11101010_2, where the LSB, bit 0, is on the far right. One second ago, the status byte was 11101001_2. We wish to know what the current state of each device is, which devices have changed state during the last second, and in which direction. Steps used to answer such questions are as follow.

Step 1 Examine the current status byte (CSB). Determine the status of each external device from the logic state of its status bit.

The CSB is 11101010_2. From this value, we conclude that pressure, velocity, and concentration sensors are all at or below their respective setpoints; temperature and flow rate sensors are above their respective setpoints; and valve A, valve B, and power are all on.

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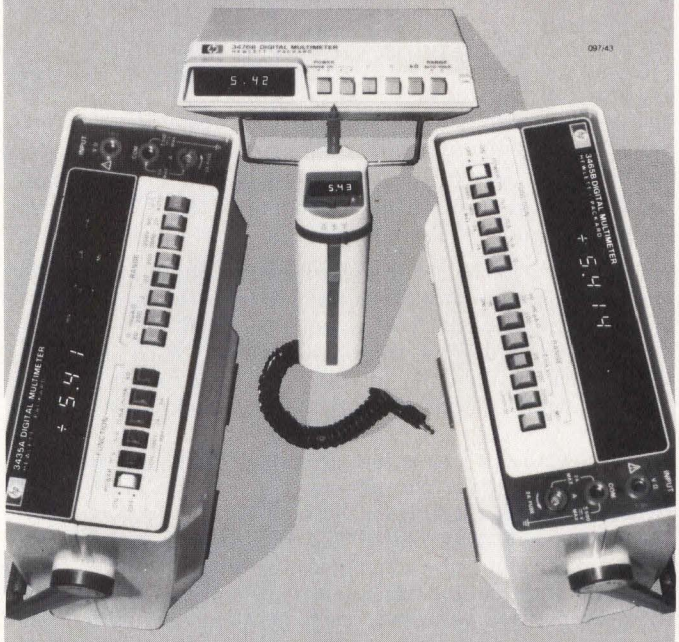

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Step 2 Perform an exclusive-OR operation between the prior status byte (PSB) and the CSB. A logic 1 in the result indicates that the logic state of that device has changed.

The logical operation to be performed is

$PSB \oplus CSB = Q1$

where $PSB = 11101001_2$, $CSB = 11101010_2$, and Q1 is the result of the exclusive-OR operation. Thus,

$$\begin{array}{ll} 11101001 & PSB \\ \oplus\ 11101010 & CSB \\ \hline 00000011 & Q1 \end{array}$$

and $Q1 = 00000011_2$. We conclude that only the pressure and temperature sensors have changed state.

Step 3 Perform an AND operation between Q1 and the PSB. A logic 1 in the result indicates a device that has changed state from logic 1 to logic 0.

The logical operation that we wish to perform is,

$PSB \cdot Q1 = Q2$

where $PSB = 11101001_2$, $Q1 = 00000011_2$, and Q2 is the result of the AND operation. We obtain,

$$\begin{array}{ll} 11101001 & PSB \\ \cdot\ 00000011 & Q1 \\ \hline 00000001 & Q2 \end{array}$$

and thus can conclude that the pressure sensor has changed from being above the setpoint to now being at or below the setpoint (logic 1 to logic 0 transition).

Step 4 Negate (or complement) Q2, then AND this complemented result with Q1. A logic 1 in the result indicates a device that has changed state from logic 0 to logic 1.

The logical operation that we now perform is,

$\overline{Q2} \cdot Q1 = Q3$

Since Q2 is 00000001_2, the complemented value of Q2 must be 11111110. The result of the AND operation is obtained as follows,

$$\begin{array}{ll} 11111110 & \overline{Q2} \\ \cdot\ 00000011 & Q1 \\ \hline 00000010 & Q3 \end{array}$$

The result, $Q3 = 00000010_2$, permits us to conclude that the temperature sensor has changed from at or below the setpoint to above the setpoint (logic 0 to logic 1 transition).

The reason for performing such a series of logical operations is to determine what type of corrective actions must be applied to the system if it is not operating properly. If the temperature is below its setpoint, we may have to turn on a heater. If the concentration of a reactant is too high, we may have to turn valve B off and temporarily halt the flow of reactant into the system. If the pressure is above the setpoint, we may have an emergency condition and must shut the power off to the entire system. With a properly interfaced microcomputer, all such decisions can be easily and quickly made under software control and the necessary corrective actions initiated. However, it must be realized that mechanical and electromechanical devices typically have response times that are much longer than the decision times for a microcomputer. These response times must be taken into account in software "design," and are important considerations in the field of digital controls. A discussion of response times is beyond the current scope of this column.

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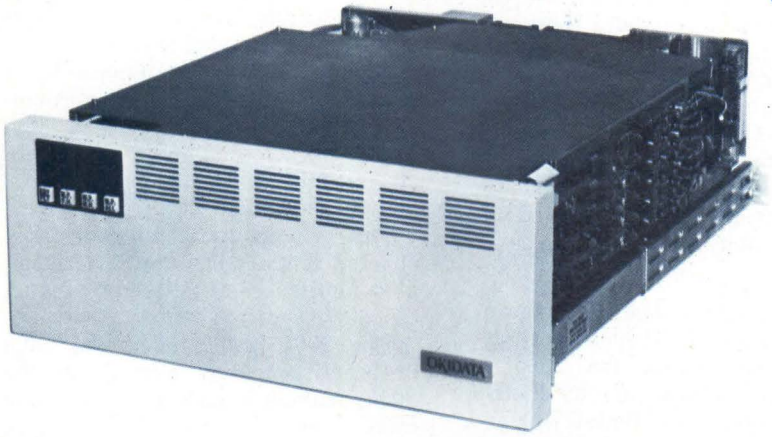

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CIRCLE 62 ON INQUIRY CARD

Microprocessor System Design Center Functions as General-Purpose Development and Integration Tool

Designed for use with several types of microprocessors, the 8001 and 8002 microprocessor development systems are general-purpose tools for supporting hardware emulation and debugging, and for facilitating development of control software. Tektronix, Inc, PO Box 500, Beaverton, OR 97077 has manufactured the units to fully support system development using the 8080 and 6800 microprocessors. Support for additional devices will follow, as will support of new microprocessors as they are developed. The user is therefore free to make use of the microprocessor best suited to his system requirements.

The 8002 serves as an active tool for developing control software for microprocessor-based systems and for quickly integrating software with the hardware prototype. Control programs are entered into the 8002's disc memory via a terminal; this includes interactive editing of the program. Source code is assembled into object code for the particular microprocessor, and the assembled program is run under debug control on a slave CPU which emulates the chosen microprocessor. Errors discovered during the debugging process can then be easily corrected. The program in both source and object codes is stored on a floppy disc.

In-circuit emulation of the microprocessor and control memory occurs via an in-circuit emulation cable between the 8002 and the microprocessor socket on the prototype hardware. This aids software/hardware integration and checking of each section (I/O, memory, microprocessor) of the prototype. Any errors in the I/O portion of the program are corrected in source code and those routines are reassembled. The satisfactory program is programmed into p/ROMs which are inserted into the prototype. Once the memory portion of the prototype is checked, the emulation cable is disconnected, the microprocessor chip is plugged in, and the prototype is run as a separate unit.

Optional built-in p/ROM programming capability is available to save time by eliminating the need of transferring the program to another piece of equipment. Both 1702 and 2704/2708 p/ROMs can be programmed.

The development system itself is a complete microcomputer. Basic elements include a main chassis housing CPU, 16k dynamic RAM master memory, 16k dynamic RAM common memory (expandable to 64k), control, and interface cards; 2-spindle floppy disc drive with 10-ms access time per track; and interactive terminal (either the company's CT-8100 video terminal or the user's RS-232-C compatible terminal). In addition, TTY terminal, paper tape reader/punch, modem, and line printers can be added as needed.

Containing a master memory card, CPU card, disc drive, and disc operating software, Tektronix 8002 is a complete software development aid which also integrates software with the hardware prototype. Both the 8002 and 8001—the in-circuit emulation portion of the system only—currently are designed for use with the 8080 and 6800 microprocessors

Master/slave architecture supplies flexibility to accommodate several microprocessor types. A master CPU controls previously mentioned operations through a disc operating system (TEKDOS). Up to three slave CPU cards can be plugged in at one time for emulating different microprocessor types, thus eliminating hardware reconfiguration when switching from one development project to another. Slave CPU cards can be swapped to accommodate additional microprocessor types. A separate CPU (also slaved to the master), used for program assembly, has an optimized design to shorten assembly time.

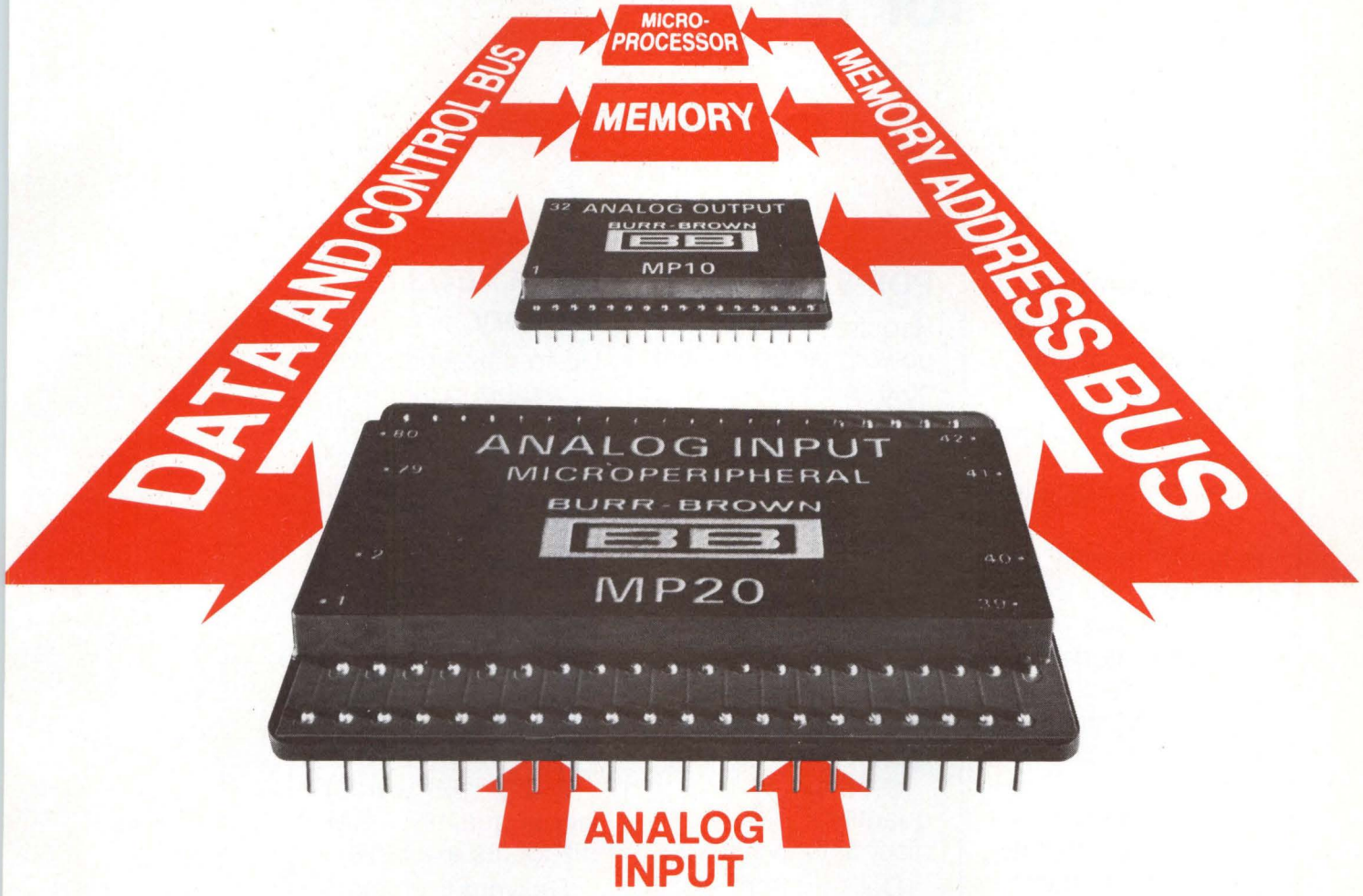
Software also is optimized. A table-driven relocatable macro assembler has two main features. A high degree of assembler commonality among microprocessor types is obtained; and when changes are made to the source code program, only affected routines have to be reassembled into object code, thereby saving time.

The 8001 system offers the same in-circuit emulation features as the 8002, without capabilities for source code entry and assembly of source to object code. This approach is valuable to established users who have facilities for program entry and assembly or to potential users who wish to minimize costs by renting time on a timesharing system. A ROM operating system replaces the disc. Common memory module is 16k dynamic RAM, expandable to 64k. Provision is made for entering object-coded programs directly into the emulator CPU's memory. With the addition of a master memory card, assembly CPU card, disc drive, and disc operating software, the 8001 can be upgraded at any time to an 8002.

Options available for both units include 8080, M6800, or Z80 slave CPU boards and slave CPU in-circuit emulation cables, which contain buffers and line drivers to isolate the slave CPU from the user's prototype hardware; 1702 or 2704/2708 EPROM programmer board with necessary logic and power supplies for programming; and 16k dynamic RAM expansion. Also available are a hardware trace board containing the P6451 logic probe and supporting hardware to provide real-time logic state display on the system peripherals selected by the operator, and maintenance front panel providing entry and display of addresses and data, as well as access to some internal bus controls.

Circle 170 on Inquiry Card

Analog input...analog output. Now they're both just this simple.



Meet the 16-channel MP20 and MP21 Analog Input Systems. They join our previously introduced MP10 and MP11 Analog Output Systems to give you a complete analog interface solution for your microprocessor based designs.

Now, instead of designing a complete data acquisition system, you simply plug in one of these units as if it were memory. That means big savings in design costs, and faster product introduction too.

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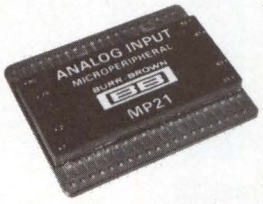
Since these systems are treated as memory by your CPU, software implementation is simple too. Just assign one 8-bit memory location per channel, and use any memory reference instruction to access data. For example, one LDA instruction will acquire a channel of information when used with the 8080A. Alternatively, the units can be interfaced as an I/O port or on an interrupt basis.



Both the MP20 and MP21 have resistor programmable input ranges of ±10mV to ±5V full scale allowing you to handle low-level signals directly. They provide 8-bit resolution and throughput accuracy better than ±0.4% of full scale on the ±5V range.

With a price of just $140 (100's), it just doesn't make sense to design your own analog input solution. For complete details, write or call Burr-Brown, International Airport Industrial Park, Tucson, Arizona 85734. Phone (602) 294-1431.

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2. Burst refresh mode. (DEC method)

One year warranty on parts and labor.

$1,195 single quantity. OEM discounts available.

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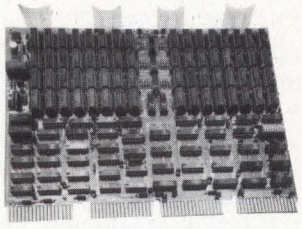

MSC 4501
January

PDP-8 Memory

Requires 75% less power than equivalent core memories (8K words requires only 0.6A at +5 volts DC).

Nonvolatile, 8K words fits in a single OMNIBUS® slot.

Totally PDP-8 A, E, F or M hardware and software compatible.

One year warranty on parts and labor.

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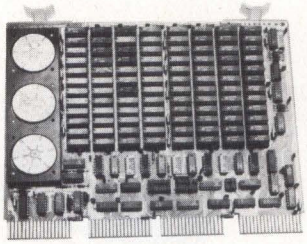

MSC 3201
February

PDP-11/04/34 Memory

Up to 64K words, with or without parity, in a hex wide "SPC" slot.

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Expandable in 4K increments to 16K words, and in 16K increments to 64K words.

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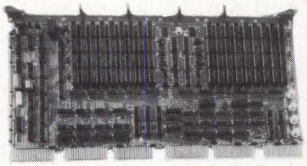

MSC 3501
March

CIRCLE 126 ON INQUIRY CARD CIRCLE 127 ON INQUIRY CARD CIRCLE 128 ON INQUIRY CARD

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Portable Microcomputers Contain Compiler and File Management System

A line of table-top 8080-based microcomputer systems, the Z//100 series, called "the personal FORTRAN machines," is comprised of three low cost models. Built around an 8080 CPU, all include 3k of p/ROM; a minimum of 33k bytes of RAM, expandable to 64k; and an IBM-compatible dual diskette drive, offering 512k bytes of online storage. A second dual drive can be mounted for a total 1M bytes of storage. Drives feature voice coil positioning and motorized loading and unloading of diskettes.

Announced by Realistic Controls Corp, 3530 Warrensville Center Rd, Cleveland, OH 44122, the complete systems contain a monitor; file management system; and FORT//80, an 8080 resident FORTRAN IV compiler (see *Computer Design*, Nov 1976, p 148). Z//100-1 is a timesharing replacement system, priced at $7995. It includes 36k bytes of RAM, dual diskette drive, and two EIA RS-232-C serial communications channels. One channel can be ordered with a 20-mA current loop interface.

The -2 includes 34k bytes of RAM, dual drive, 60-char/s bidirectional line printer (80-column friction feed standard, 132-column tractor feed optional), and keyboard. It costs $8995. Top-of-the-line -3, priced at $9795, includes 33k bytes of RAM, dual drive, keyboard/1920-char CRT display, and RS-232-C serial communication channel. An optional 300-line/min printer (either 80-column friction feed or 132-column tractor feed) is supported by this configuration.

Circle 171 on Inquiry Card

Complete Plug-In Floppy Disc Unit Boosts Personal Computing

Believed to be the first floppy disc system for 5¼" diskettes, the model FD 2411 Microfloppy™ includes flexible disc drive, power supply, cabinet, controller/interface card, power cord, fuse, and all cables. Pertec Computer Corp's iCOM Div, 6741 Variel Ave, Canoga Park, CA 91301 incorporates its FDOS-M software on diskette into the factory assembled and tested unit.

The system is 100% plug-compatible with the Altair 8800, Poly 88, Imsai 8080, and other microcomputers which use the Altair bus format. A controller/interface card, using advanced MOS LSI and low power Schottky technology, contains all necessary electronics to interface the disc to the microcomputer. The card incorporates an LSI controller chip; it also features onboard ROM and RAM. Phase-locked loop techniques are used to improve accuracy and performance.

FDOS-M software includes a macro assembler, string-oriented text editor, and diskette initializer. A single diskette stores up to 175 named files or programs (with files as small as 128 bytes or as large as the entire diskette capacity). The company's 8k disc BASIC-M software is compatible with FDOS-M, assembler, and editor, and is supplied on the same diskette.

Using the Shugart Minifloppy™ disc drive (see *Computer Design*, Sept 1976, p 134), the unit has an average access time of <0.5 s; transfer rate is 125k bits/s. The diskette has sectors containing 128 bytes and features "write protect." In formatted mode, a total of 70k bytes are available on a single diskette.

Circle 172 on Inquiry Card

Combination of Two Technologies in µProcessor Saves Power

As powerful as the CPU of a small computer, the MAC-8 is claimed to be the first microprocessor able to execute several hundred different electronic logic, or "thinking," functions while using 0.1 W of power. The device contains over 7k transistors fabricated on a single chip of silicon.

Using a combination of IC technologies known as CMOS and Pseudo n-MOS, Bell Telephone Laboratories, Research and Development Unit of the Bell System, Mountain Ave, Murray Hill, NJ 07974 designed the microprocessor to perform combinations of over 400 electronic instructions at a rate exceeding 100k per second, while using very little power. Portions of the unit's circuitry use CMOS technology, which has inherently low power requirements. Other portions use Pseudo n-MOS, which minimizes the size of the silicon chip by allowing designers to pack circuit elements close together. Power is conserved by switching the Pseudo n-MOS portions "on" only when their functions are needed. Combination of the two technologies allowed an extremely large number of circuit functions to be packed on a given chip area.

Memory capability is provided via a separate chip or chips designed to store instructions and hold intermediate results of computation. This "off-chip" memory provides potential for increased memory capacity and processing capability without additional circuit design.

Developed by Bell Labs engineers, an "address arithmetic unit" (AAU) on the processor chip, expedites communication between memory and the processor. The AAU is an electronic circuit that locates instructions and data in the off-chip memory while the processor simultaneously performs other tasks. Typical instructions are made up of eight bits, or basic units of "on-off" electronic information.

Processing functions are controlled by an extensive series of programs prepared by the company's system designers. As a result, off-chip memory units can be customized to enable the microprocessor to perform varied functions.

Singularly low power requirements and large instruction set make the device useful in telecommunications equipment and systems that are difficult to power or so compact that heat is a problem. It will form an integral part of Bell System equipment such as private branch exchanges and electronic switching systems.

Circle 173 on Inquiry Card

In-Memory Operating System Develops Microcomputer Programs

An exclusive software system, Quickrun is being offered by Microkit, Inc, 2180 Colorado Ave, Santa Monica, CA 90404 for their -8/16 universal microcomputer development system (see *Computer Design*, Sept 1975, p 114). As a memory resident microcomputer development concept for 8080 or 6800 microcomputers, the system runs in 32k bytes of memory

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which provides space for a 1000 statement source program, 4k-byte object area, and all system software. It consists of a monitor/debugger, editor, and assembler which are all co-resident in memory along with source and object code workspaces.

Program development is facilitated since changes are made directly in the source program; the user instantaneously switches from editing to assembling to debugging. Once software and source program are loaded, all subsequent processing is performed in memory, and virtually all I/O is eliminated.

Use of the microcomputer system's 8k RAM modules with write protection registers allows each 1k page of memory to be individually protected and unprotected under program control. Nonvolatile storage of debugged programs (source and object) is also provided by the microcomputer's cassette tape units.

Specific features of the software system include ultra high speed assembly and edit capability; user allocation of memory space as desired between source code, object code, and symbol table; symbolic debugging of object programs; and hardware memory protect which makes the system (source program) crash proof. Powerful screen-based interactive software—editor and monitor/debugger—is designed around a 20k-char/s CRT display. This allows the entire screen to be rewritten in 50 ms.

An in-circuit Microemulator option is also available. It provides in-circuit emulation, hardware breakpoints, single-step execution, trace execution, and 2708/2704 EPROM programming in addition to the software system's development tools.

Circle 174 on Inquiry Card

System Combines Data Storage Technology With µProcessor Flexibility

The standard MC-200 system, available from GNAT Computers, Inc, 7895 Convoy Ct, Unit 6, San Diego, CA 92111, provides RS-232 formatted I/O enabling any RS-232 device to plug directly to the DB25 connector on the system. Designed for applications such as data monitoring and

storage, process control, or communications, the system combines the reliable data storage technology of the 3M DCD-10 minicartridge tape drive with the flexibility of a microprocessor-based control system.

Features of the unit include hardware and software control of the tape drive plus optional parallel I/O for data monitoring and storage applications. Special control characters are designated as command words, and are duplicated on the control panel by control switches. A baud rate select switch, also located on the panel, allows selection from 75 to 9600 baud.

Available options include separate parallel I/O lines, expanded serial I/O, independent record and playback baud rates, file search capability, dual drives for increased data storage capability, and word length select. Programming and special applications requirements may be developed using the system's options or other microprocessor systems.

Circle 175 on Inquiry Card

Easy-To-Program Microprocessor System Controls Moisture

System 700, containing an Intel 8080 microprocessor, provides online process control and data logging using input data from high or low level analog sensors, contact closures, and speed indications for applications concerned with controlling moisture. Omega Controls Corp, 1542 Moulton Pkwy, Tustin, CA 92680 has provided the system with simple English language programming. A complete turnkey software package leaves the user only the task of entering process parameters via the computer-assisted entry/edit program.

Multi and varied inputs are accepted, manipulated, and output as either analog or digital signals for control purposes. The system can also serve as a data logger outputting raw or modified data via printer, mag tape, or disc.

Utilizing analog and digital multiplexing, the system interfaces with various types of input sensors, including the company's MM-600 moisture gauge and the 711A mass sensor. Standard I/O media are a CRT display and associated keyboard. Microprocessor-generated questions are displayed on the CRT to assist the user in inputting process control parameters. The CRT is also used to display monitored process results and derived data, such as process profiles. Other output devices include teletypewriter, floppy disc, IBM-compatible mag tape, and card reader.

Circle 176 on Inquiry Card

Expanded Single-Chip Family Replaces Custom Devices at Lower Cost

Six single-chip microcomputers have been added to the PPS-4/1 family which can be used to replace custom LSI TTL devices at lower cost to be the basic control system, and which also can be used as programmable peripheral controllers. Joining the MM77 microcomputer, which has 1344 x 8 ROM, 96 x 4 RAM, and uses a powerful 50-instruction set which allows more functions to be programmed in fewer ROM words, are the MM76 and MM78, both available immediately.

The -76 has a 640 x 8 ROM and 48 x 4 RAM, and contains slightly expanded instructions for special purposes; the -78, with a 2048 x 8 ROM and 128 x 4 RAM, also uses the 50-instruction set. All three have 31 I/O ports, many of which may be programmed for either input or output service. I/O options and two interrupt request input lines are the same as those of the original PPS-4/1 device.

Three other chips that Rockwell International, Microelectronic Device Div, 3310 Miraloma Ave, PO Box 3669, Anaheim, CA 92803 plans to produce as a part of the MM76 series are the -76C, -76D, and -76E. Each of these is identical to the -76, with certain additions.

Scheduled for the second quarter of 1977, the -76C contains a high speed counter (either one 16-bit or two 8-bit presettable up/down counters) with eight control lines. The -76D, with 12-bit ADC and six extra I/O lines added, will be available

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More to the point, Megastore keeps going long after a disk drive quits. Without motors, bearings, heads or platters, there's nothing to wear out, burn out or crash. No moving parts.

Megastore is the astonishing new fixed-head disk memory replacement from Ampex that uses reliable cores instead of rotating media. In the long run it saves a lot of money.

Megastore provides increased throughput, increased system availability, increased system uptime and reduced maintenance costs. A vastly better return on investment.

Unplug your disk and plug in Megastore. You'll get a half-million to four million bytes of capacity (in half-megabyte increments) that your existing software can't tell from the disk it was designed for. The only difference you'll see is a major improvement in throughput, because Megastore has a data access time that's anywhere from 1000 to 3000 times faster than the disk it replaces.

Megastore. Ready now as a software-transparent replacement for Novadisk (Megastore 1223) and DEC's RJSO3/RJSO4 Disk (Megastore 11). Also available as Megastore 4666 for users who wish to provide their own controller. Other versions on the way. Contact Ampex Memory Products Division, 200 North Nash Street, El Segundo, California 90245. Phone (213) 640-0150. Ask for Megastore. The disk that doesn't spin.

AMPEX

Novadisk is a trademark of Data General Corp.

during the third quarter of 1977. Containing an expanded ROM capability of 1024 x 8, the -76E is available 16 weeks ARO.

An economy single-chip computer, designated the MM75, is also planned for the second quarter. It has the same ROM and RAM capacity as the -76, but has only 22 I/O lines. It is packaged in a 28-pin DIP, while the other units come in 42- or 52-pin quad in-line packages.

All seven chips are compatible with other LSI devices and use the same system development aids. Shared features include provision of clocked, simultaneous serial I/O capabilities; and cascading of PPS-4/1 microcomputers. Other features are the same as those for the original PPS-4/1 member (see *Computer Design*, June 1976, pp 120, 122).

PPS-4/1 instruction sets are similar to those of the multichip PPS-4/2 and -4 systems. This permits upward and downward expansion of designs while using the most cost-effective microcomputer.

To facilitate production testing of programmed microcomputers, an on-chip design scheme enables complete testing of all functions, including user's ROM patterns. An "assemulator" system development tool is also available for converting assembler to machine language, and for editing.

Circle 177 on Inquiry Card

Floppy Disc System for 8080 Microcomputer Is Ready to Use

The FDS-2 floppy disc system designed for S-100 based 8080 microcomputers contains all hardware and software necessary for immediate use. Fully tested system comes with a customized diskette to meet the end user's specifications for I/O ports (if nonstandard) and machine.

Rugged IBM-compatible drives and controller of the iCOM Frugal Floppy™ which has an executive system, text editor, and assembler are combined synergically with the company's "executive handler" to form the system announced by Synetic Designs Co, PO Box 2627, Pomona, CA 91766. The executive handler provides for all I/O vector assignments, I/O device handlers, USART and CPU initialization, and program relocation requirements, all of which are done transparent to the operating system. A source copy of the handler allows the sophisticated user to build a more complex disc operating environment.

Diskettes can store up to 256k bytes of any number of files of any length containing program source, program object, or user generated data. One to four drives can be operated from the same controller for total online storage capacity of over 1M bytes. Motor shuts down on load and unload to protect the diskette, and disc head and pressure pad are retracted when not performing a read or write operation in order to increase media life.

Data format is IBM 3540 and 3740 compatible allowing future system expansion or multiprocessor correspondence. Aluminum cabinet, measuring 8.75 x 17 x 20" (22.23 x 43.18 x 50.8 cm), includes power supplies, RFI filter, fan, and all cables and connectors needed to support the floppy system which includes two disc drives, interface board and cable, and controller boards with cables.

Circle 178 on Inquiry Card

Z80-Based Single-Board Computer Offers 16k Bytes of RAM

A standalone microcomputer designed around the Z80 microprocessor family, the Software Development Board (SDB-80) is claimed by Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006 to contain more on-board firmware and RAM than any other single-board microcomputer. Offering the features of the Z80, the board uses the company's 16k dynamic RAM technology.

The board is available without firmware for OEM applications. For software development, it may be purchased with a complete package of system firmware in five 2k x 8 ROMs located on the board. This 10k-byte package enables the user to generate, edit, assemble, execute, and debug Z80 programs. RAM is therefore available for user's programs.

The development package also includes interface cables for EIA/RS-232 terminals and model 33 teletypewriters, documentation, and 4k or 16k bytes of RAM. System expansion is possible with optional add-on circuit boards. RAM-80 provides 16k bytes of additional RAM; AIM-80 (application interface module) adds in-circuit emulation; MKSX-80 permits Intel MDS systems to be interfaced with the SDB-80 on a port-to-port basis; and FLP-80, which includes software drivers, interfaces the SDB-80 to a dual floppy disc drive.

Single unit quantity price of the OEM configuration with 16k bytes of RAM is $995. Total package is priced at $1195 with 4k bytes of RAM, or $1395 with 16k bytes of RAM.

Circle 179 on Inquiry Card

Relocatable Software For Z80 μProcessor Is Powerful and Versatile

Inherent power of the Z80 microprocessor has been combined with outstanding design by Technical Design Labs, Inc, Research Park, Bldg H, 1101 State Rd, Princeton, NJ 08540 to create what is claimed to be the most powerful and versatile software developed for a microprocessor. Features of the Zapple™ line of software are that it is relocatable (ie, it may be loaded and run at any memory location), and all software (except for the macro assembler) may be placed in ROM and operated from ROM without first moving it into RAM.

Hardware independence is achieved because all I/O drivers for all of the software are contained only in the monitor program. Thus, once the monitor is configured for a certain hardware I/O configuration, all software is immediately compatible with that system.

Five software packages currently available are the monitor, text editor, relocating macro assembler, BASIC, and SCRIPT. Monitor occupies 2k of RAM and offers 27 instructions including full program debug capability, I/O handling, and modular

Could you simplify system design with 128K bytes, ECC, timing and control all on a single memory card? Intel has.

Introducing Intel's versatile new MOS-RAM memory card, mu-3000. It gives you your choice of 16K, 32K or 64K by 16 to 22 bits. That's up to 128K bytes on a single card. Plus the added advantages of on-board error correction coding, system interfaces, timing and control.

Imagine the design economies and efficiencies that makes possible. You can replace up to four conventional single board semiconductor and core memory cards with one mu-3000. And in addition to unprecedented density, Intel's semiconductor technology delivers improved speed and reduced power and cooling requirements.

The mu-3000 is compatibility-engineered to make it easy for you to use as the new best choice for mini and midi mainframe memory, add-on memory systems and specialized memory packages. Or use to upgrade existing single board semiconductor and core memory systems.

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ECC provides 10 to 25 times higher data reliability than typical memory systems. Six check bits are added to each word during write operations. Then, during read-out, single bit errors are detected and automatically corrected. And the host processor is notified of any multi-bit errors.

To accomplish longer word lengths and larger system capacity, up to four mu-3000 cards can be combined in a single 5¼" high system chassis. The chassis provides room for Intel's microprogrammable self test card and a custom interface card, too.

Clip the coupon to get detailed data on the mu-3000. Or, if you would like an Intel system specialist to show you how mu-3000 can improve your package, give us a call.

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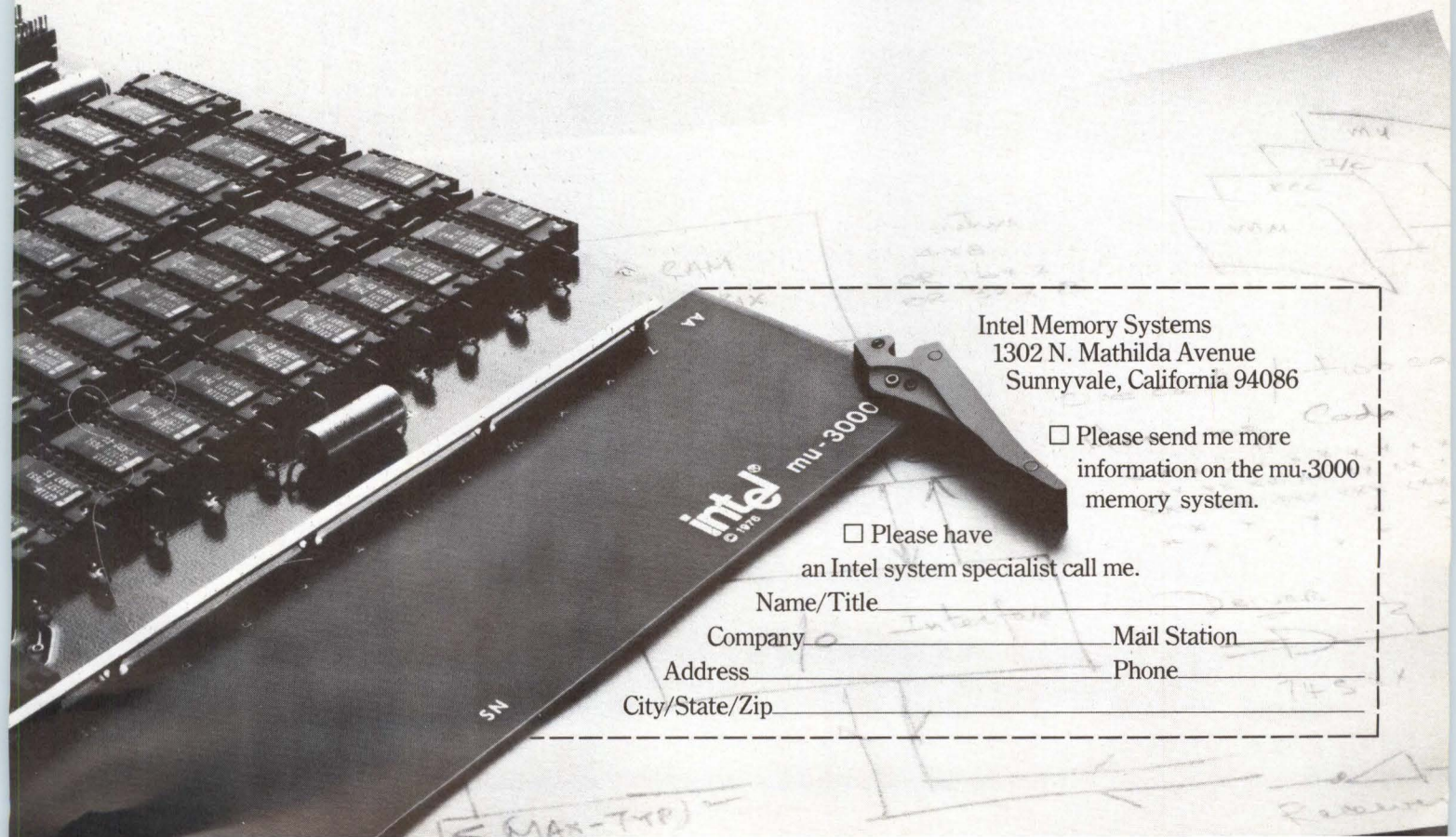

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☐ Please send me more information on the mu-3000 memory system.

☐ Please have an Intel system specialist call me.

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organization which allows simple expansion. Occupying 3k bytes of RAM, the editor is line-and-character-oriented for maximum manipulation of text and speed improvements of up to ten times those of similar 8080 editors.

The assembler, which occupies 8k of RAM, generates relocatable object code and allows infinite nesting of macros. A linking loader extension will be available in the first quarter of 1977.

In addition to "normal" requirements, BASIC includes complete editing facility, a List Variables statement, and Trace and Renumber commands. It uses 8k RAM. As a word processor occupying 3k RAM or ROM, SCRIPT allows complete word processing capability. User's manuals supply the software documentation; monitor documentation includes source code to enable full use of the hardware independence feature.

Circle 180 on Inquiry Card

Analog I/O Systems Provide Ready-Made Interface to µComputers

As a low cost solution to analog input and output interfacing requirements for both system development and production units, the 4216 (16-channel input board) and 4102 (2-channel output board) analog I/O systems are electrically and mechanically plug-compatible with Pro-Log 4- or 8-bit microcomputers. Interfacing involves plugging the single-board unit into the card file, wire-wrapping the card file bus connector, and making connection to analog inputs, outputs, and ±15-V supplies.

Systems which are treated as memory or I/O are easy to program. The boards from Burr-Brown, International Airport Industrial Park, Tucson, AZ 85734 can be treated as memory by the CPU, with each channel requiring one 8-bit memory location. The address block occupied by each board is strap selectable; thus they can be located anywhere in memory.

Intended primarily for industrial control or test equipment applications, each input board is a 16-channel differential-input system. Flexibility allows selection of input ranges between ±10 mV and ±10 V. Process current-loop input signals are handled by adding series dropping resistors.

Analog inputs are converted with 8-bit resolution and with throughput accuracy ranging from ±0.5% of full scale reading on the ±10-V range to ±0.7% on the ±10-mV range. Conversion time is 60 µs.

Output boards each contain two channels; they are jumpered at the factory for ±10-V operation (2's complement coding). Boards can be altered to provide 0- to 10-V operation (straight binary coding). Output resolution is 8-bit, with throughput accuracy of ±0.4% of full scale reading.

Circle 181 on Inquiry Card

Paper Tape Reader Loads Programs In Small µProcessor Applications

Microleru is a low cost, hand-driven paper tape loader which uses the Simser asynchronous serial link for an almost direct connection to most serial interface circuits (UART, ACIA, USART, etc). The Simser IEEE standard, suited to microprocessors, is similar to the 20-mA and EIA/RS-232 standards. Because the clock is transferred with the data, no precise, expensive clock is required at each end of the link. In applications other than those involving this paper tape reader, the clock line is under control of the receiver, providing a possible handshake between receiver and transmitter.

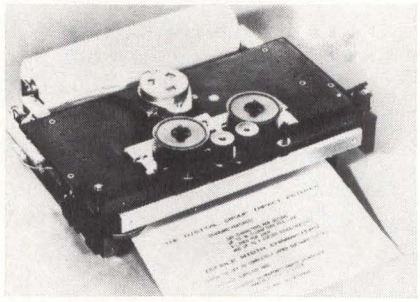
Stoppani Electronic, CH-2105 Travers, Switzerland has developed the small, high performance device to load programs in small microprocessor applications. Because of simple handling, programs smaller than 1k bytes are read as fast as with any other paper reader. With a 10k-baud transmission rate, the tape can be pulled as fast as the hand can move.

Measuring 70 x 60 x 20 mm, the unit features 4.6- to 5.3-V, 40-mA maximum V_{cc}; serial data out; and any length connecting wires with a maximum resistance of 4 Ω. Clock frequency is 16 times the data frequency (baud rate) with any phase shift between these two signals. For each character read on the paper tape, a start bit, eight data bits, and at least two stop bits are transferred.

Circle 182 on Inquiry Card

Inexpensive Impact Matrix Printer For Use With µComputers

A full size impact printer designed for use with microcomputers is being offered by the Digital Group, Inc, PO Box 6528, Denver, CO 80206.



Device prints 120 char/s, with 96 char/line, 12 char/in horizontal, and 6 lines/in, making up to four copies simultaneously. Character matrix is 5 x 7 and ribbon has built-in reinkers for life of 10M characters. Paper can be either standard 8½" roll, fanfold, or cut page.

Character set and pitch are variable under software control, allowing for double width characters, different width characters within the same line, etc. Printer interfaces to 8-bit parallel ports.

Circle 183 on Inquiry Card

µProcessor Power Supply Meets 8080 System Needs in Rugged Applications

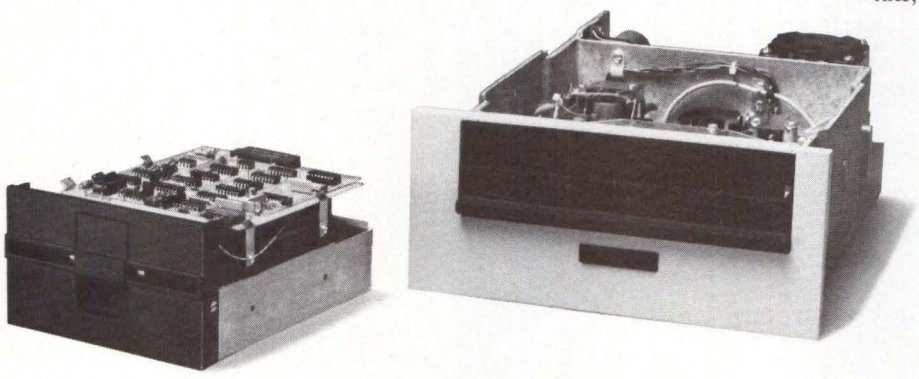
A miniature modular microprocessor power supply, model MPS-3000, is designed to meet power needs of small dedicated Intel 8080 microprocessor systems in rugged commer-

4 years, 17 patents, and 60,000 installations back every Shugart Floppy disk.

No wonder two out of three OEM's specify Shugart floppy disks. They get more exclusive features, more product support, and more responsive delivery schedules. So can you.

A SA800/801 diskette storage drive gives your system more salable features: ☐ Single density, or double density for the same price. ☐ A patented diskette clamping/registration design that prevents diskette damage from misregistration over 30,000 interchanges. ☐ A proprietary ceramic read/write head that extends media life to over 3.5 million passes per track with a head life exceeding 15,000 hours. ☐ Extras like patented pop-out diskette retrieval, drive activity indicator light, and die cast cartridge guide and base plate.

If your systems needs more data storage, you can easily convert from single to double density on the same drive. And you have a wide selection of product configurations—standard or compact "skinny" drive options, controller kits, and complete storage sub-systems.



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CIRCLE 67 ON INQUIRY CARD

cial and industrial applications where environmental protection is desired. In addition to meeting normal 5-, −5-, and 12-V requirements of the 8080 system, the supply provides 500 mA for other TTL components in the system.

Announced by Calex Manufacturing Co, Inc, 3305 Vincent Rd, Pleasant Hill, CA 94523, the supply has outputs of 5 V at 1.25 A, 12 V at 225 mA, and −5 V at 20 mA. Load regulation is ±0.02% and line regulation is ±0.05%. Output voltages are set to an accuracy of better than 1%, and output noise and ripple of all three outputs is <1 mV rms.

Supplies are protected against short circuits by foldback current limiting. Operating temperature range is 0 to 70°C. Packaged in a 1.56 x 2.5 x 3.5″ (3.96 x 6.35 x 8.89 cm) case with gold-plated pins for PC board mounting, the supply has two threaded 4-40 inserts in the cup to secure it to the board.

Circle 184 on Inquiry Card

Ruggedized μProcessor Combines 16-Bit Length With IIL Technology

Covering the full −55 to 125°C ambient temperature range, the SBP 9900 16-bit monolithic CPU is believed to be the first produced with bipolar integrated injection logic (IIL) technology. The 64-pin ceramic DIP microprocessor was developed by Texas Instruments, Inc, PO Box 5012, Dallas, TX 75222 to extend the performance capability of their 9900 family into severe operating environments.

Key features include parallel 16-bit word length; multiple 16-word register files residing in memory; seven addressing modes; and separate I/O, memory, and interrupt bus structures. Directly addressing up to 64k bytes (32k words) of memory, the unit has 16 prioritized hardware interrupts; word, byte, and bit data handling; 16 software interrupts (KOPS); and DMA capability.

Parallel I/O is achieved via separate data and address buses; serial I/O is via the communications register unit. The device is software compatible with other 9900 family members, and shares a common body of hardware/software with the 990 minicomputer family.

Speed versus power performance is variable, depending upon user-selection of the supply current. Typical clock frequency range is from dc to 3 MHz. IIL technology provides for fully static operation, a single noncritical dc power supply, and directly TTL-compatible I/O plus static logic implementation which eliminates the need for special clock and interface functions.

Benefits of faster execution times, savings in program coding, increased efficiency in interrupt handling, and reduction in memory bit requirements over 8-bit microprocessors are derived from a 16-bit instruction word and full 16-bit data precision, an advanced memory-to-memory architecture which supports multiple memory register files, and a full minicomputer instruction set which includes multiply and divide. □

Circle 185 on Inquiry Card

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The concept and design of the Printronix 300 Impact Matrix Line Printer/Plotter offers you several remarkable cost/performance advantages.

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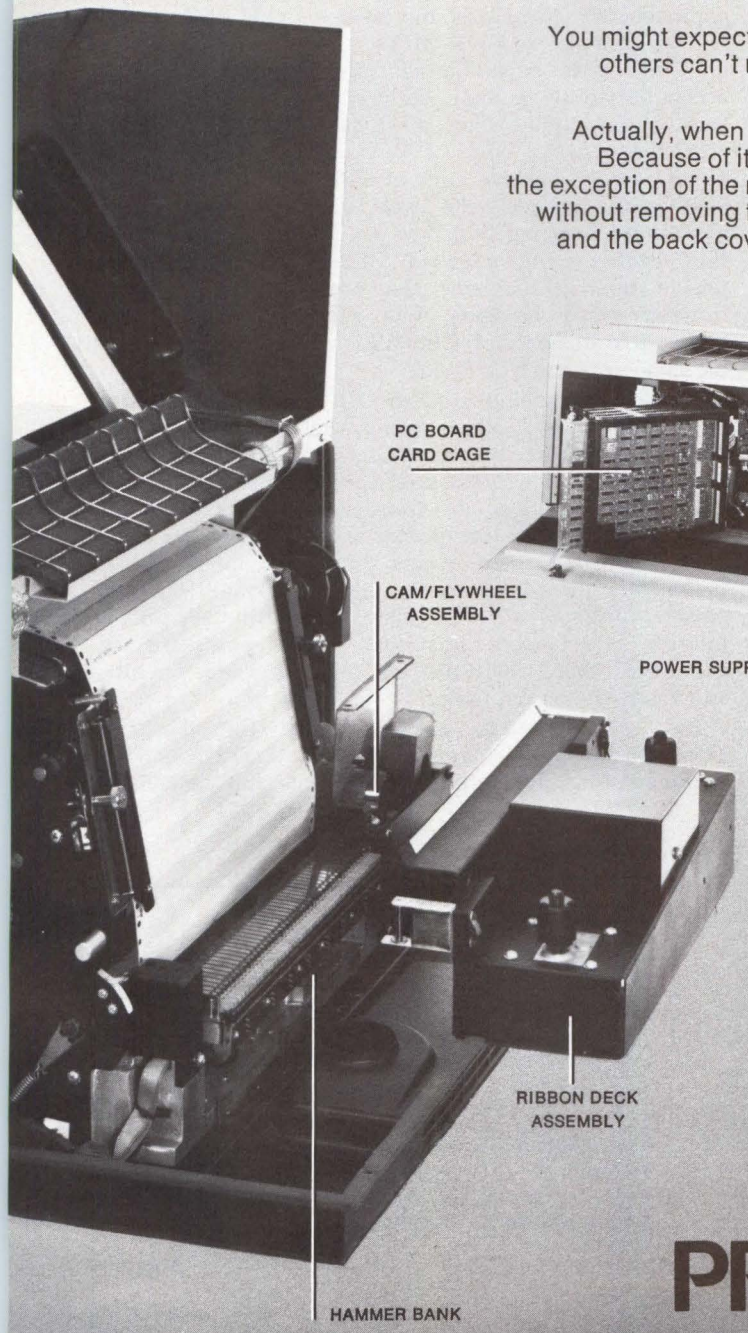
You might expect a precision 300 lpm line printer that produces print quality others can't match, and doubles as a plotter, to be a monster to service.

Actually, when compared to servicing other printers, it's easier and faster. Because of its modular design, the maximum MTTR is 30 minutes. With the exception of the main motor, all functional modules can be quickly removed without removing the shroud, as shown in the photos of the front cover raised and the back cover open. But that's only one reason why maintenance and service costs will be far lower than with other printers.



A Printronix 300 never requires character alignment or hammer flight time adjustment like other printers. Even the hammers and/or coils can be field replaced. And its mechanical simplicity extends MTBF so far that less servicing is required. That's why we've offered a one-year warranty from the beginning. Write for our brochure. You'll see why you'll have less downtime and fewer service calls. In short, a lower cost of ownership.

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CIRCLE 69 ON INQUIRY CARD

1977 ISSCC Review: Advances in Memory Circuitry

Much of the concentration at the 1977 IEEE International Solid-State Circuits Conference was on various facets of state-of-the-art semiconductor memory. Separate sessions covered MOS, high speed, and programmable read-only memories. Because of the scope involved, only a portion of the details can be reported here.

MOS Memories

One paper, for instance, described a static MOS RAM[1] which operates at 5 V, and has a typical access time of 150 ns and read/modify/write (R/M/W) cycle time of 260 ns. Operating power is 80 mW, and standby power is 8 mW.

This 4k device includes memory arrays, column decoders, internal clock circuitry, sense amplifier, and address and data I/O buffers on a 136 x 184 mil (3.45 x 4.67 mm) chip. Small chip size and the extremely low standby power are attributed to use of a new type of static cell in the matrix and dynamic circuit techniques in the clock generators, row and column decoders, and output buffers.

Fig 1 shows the typical timing requirements under nominal operating conditions for a chip having 150-ns access time. Each read, write, or R/M/W operation must be preceded by a minimum precharge time of 75 ns and is initiated by the negative-going edge of $\overline{CE}$. The input addresses must remain valid for only 70 ns past the negative edge of $\overline{CE}$. In the case of a read cycle (not shown), $\overline{CE}$ may be returned to a high level as soon as data out becomes valid or may be held low for as long as 100 μs. Data out goes open circuit approximately 25 ns past the positive-going edge of $\overline{CE}$. If the cycle is to be R/M/W, $\overline{CE}$ must be held low until the write operation is also complete. This is accomplished by holding both $\overline{WE}$ and $\overline{CE}$ low for at least 35 ns. Input data must be valid within 10 ns after the negative edge of $\overline{WE}$ and must remain valid 10 ns past the positive edge of either $\overline{WE}$ or $\overline{CE}$, whichever comes first. A write cycle (not shown) is accomplished by bringing $\overline{WE}$ low no later than 80 ns past the negative-going edge of $\overline{CE}$. Data out will then remain open throughout the entire cycle permitting straightforward common I/O memory systems. The timing requirements of $\overline{CE}$, $\overline{WE}$, and D_{in} are otherwise the same as in the R/M/W cycle.

The negative-going edge of $\overline{CE}$ triggers a sequence of internal clock edges which activate the address buffers, discharge the precharge clock, transfer true and complement address data to the inputs of the row and column decoders, and transfer the decoded row and column addresses to the proper word and column select lines. Following these events, the static input address buffers are turned off so that they no longer consume power. After a delay to allow time for the cell to transfer data to the differential output sense circuitry, additional clocks activate the output sense circuitry and finally the output buffer.

Positive-going edge of $\overline{CE}$ causes the precharge clocks to go high, discharging all other clocks, and open-circuiting the output. The entire chip remains in

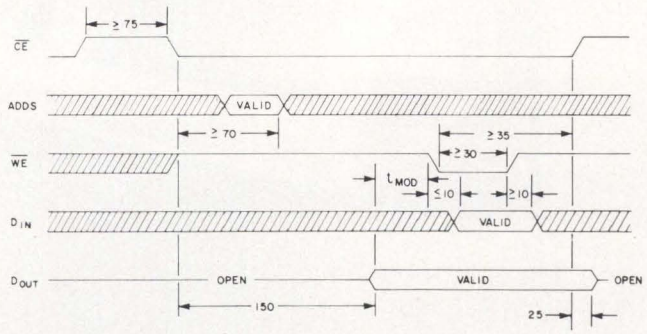
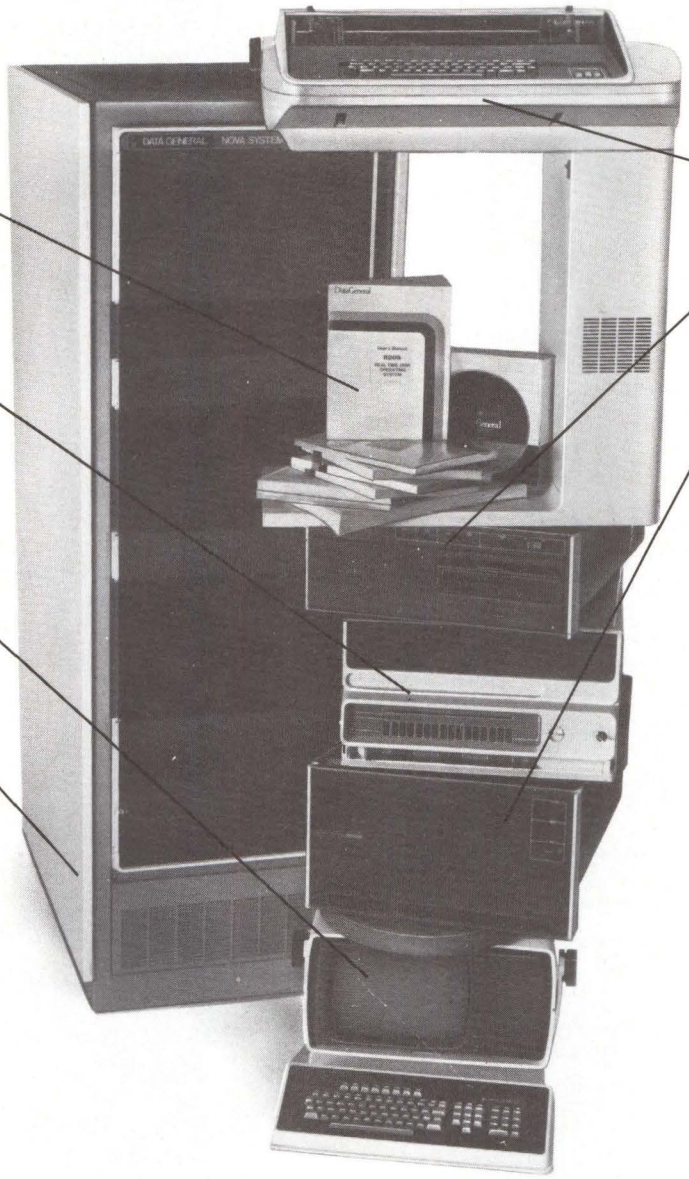


Fig 1 Read/modify/write timing diagram for 5-V, 4k static RAM.[1] Values (in nanoseconds) shown are for a 150-ns access time chip under nominal operating conditions

Here's how Data General's NOVA 3/D system stacks up against the competition.



Systems Software:
Multitasking real-time disc operating system, FORTRAN IV, Extended BASIC, ALGOL, SORT/MERGE, and Utilities.

NOVA 3/D Processor:
Hardware-protected dual partitions, 700-nanosecond arithmetic operations, 48K-word MOS memory with parity, RTC, and APL.

Video Display:
1920-character screen, upper/lower case characters, detached keyboard, numeric keypad, programmable function keys and character highlighting, display rotates on two axis.

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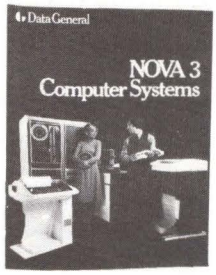

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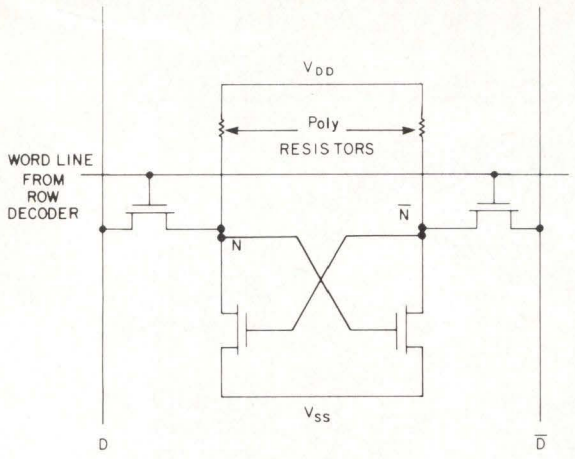


Fig 2 Schematic of static memory cell in 5-V, 4k static RAM

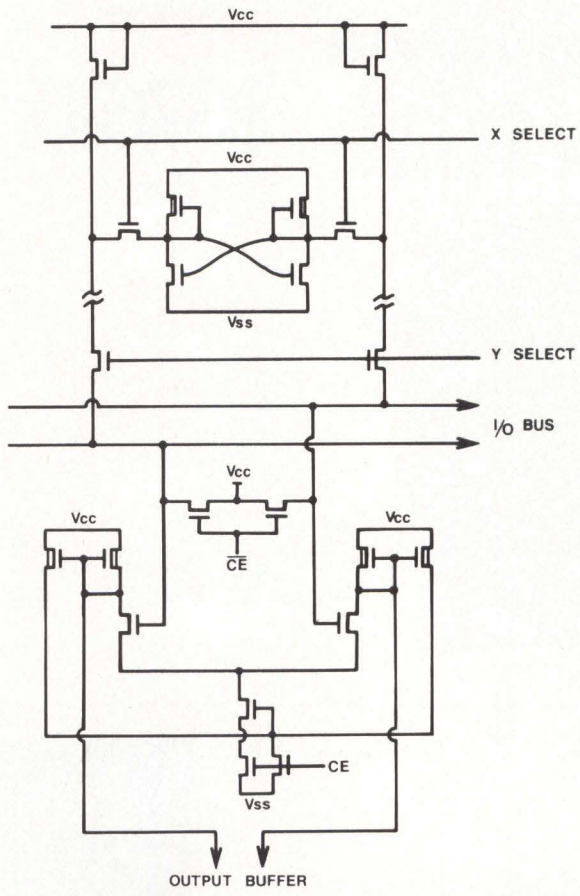


Fig 3 Partial schematic of static RAM cell,[2] column, and output sense amplifier circuitry

the precharge mode, which is also the low power standby mode, on a completely static basis. There is no maximum time limitation for $\overline{CE}$ to remain high.

The cell (Fig 2) consists of two high impedance polysilicon load resistors between V_{DD} and the two storage nodes. There is also a cross-coupled pair of transistors and a pair of address transistors with their gates connected to the poly word line.

In another application, a 5-V, 4k-bit static RAM[2] has 45-ns typical access time and 500-mW power dissipation. High performance of this n-channel MOS memory was achieved by combining MOS device scaling with on-chip substrate bias generation. Reducing the physical parameters of the MOS device by a fixed scaling factor enabled circuit density and performance to be increased while active circuit power decreased.

Memory element is a basic 6-transistor cross-coupled flip-flop. Internally, the cell, shown schematically in Fig 3, uses depletion load transistors to obtain full supply voltage while maintaining a typical cell current of 1 μA.

Low diffusion capacitance allows the memory cell to drive the output sense amplifier directly, without the aid of a column sense amplifier. The output sense circuit is a simple differential amplifier with dc feedback to provide for process and temperature compensation.

Powerdown mode is controlled by chip enable. During powerdown ($\overline{CE}$ high), the memory array is completely deselected and the column and I/O bus is reset to a threshold below supply voltage. By balancing the internal circuitry during powerdown, it is possible to overcome the additional chip enable powerup delay and obtain a powerup access time equal to the address access time. A summary of the device characteristics is given in Table 1.

TABLE 1

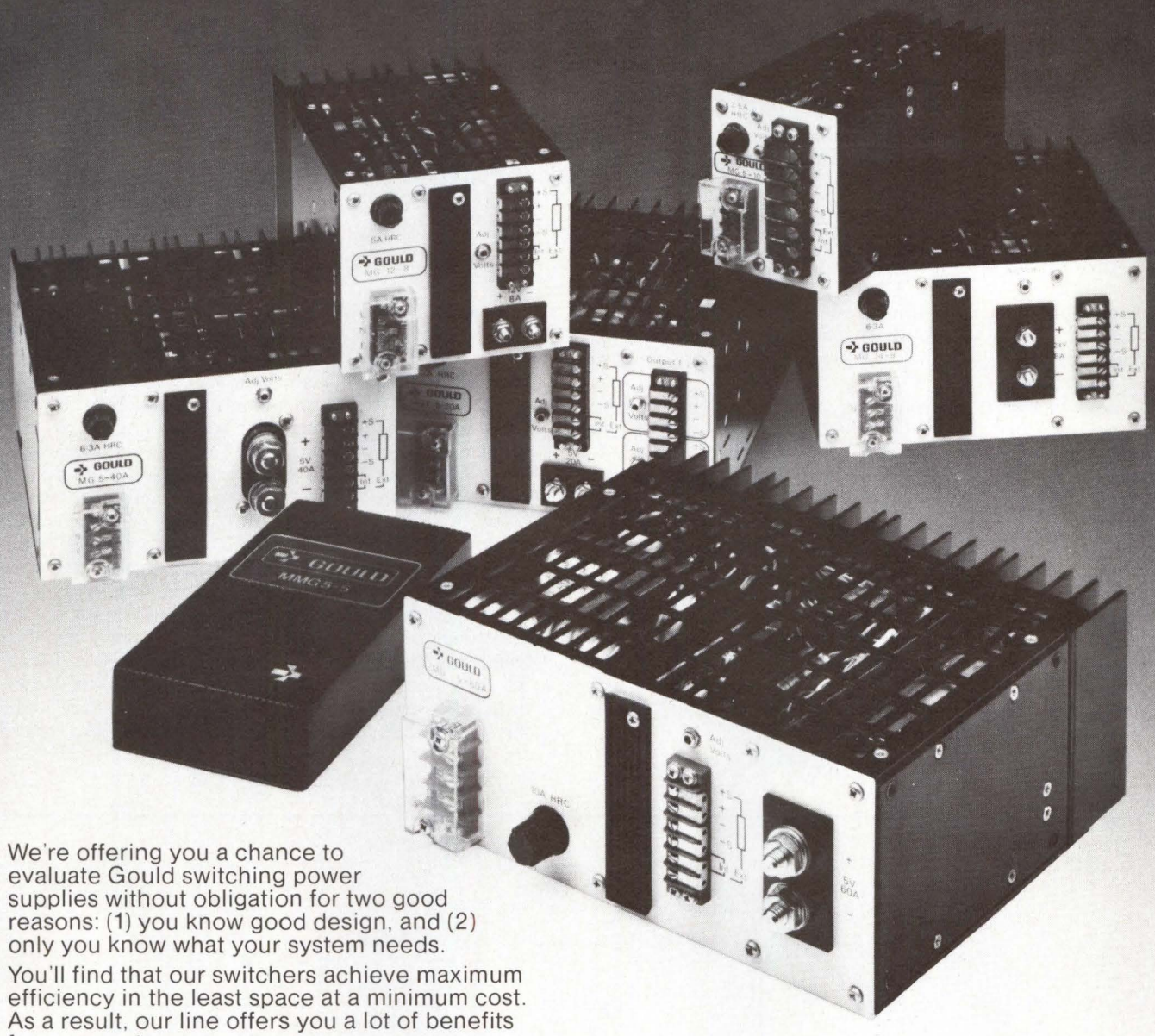
Summary of 4k Static RAM Characteristics[2]

DC	
Supply voltage	5 V
Active power dissipation	500 mW
Standby power dissipation	35 mW
I/O levels	TTL
Output sink current (V_o = 0.45 V)	25 mA
Output source current (V_o = 2.4 V)	15 mA
AC	
Address access time	45 ns
Chip select access time	45 ns
Powerdown time	30 ns
Read cycle time	45 ns
Write cycle time	30 ns
Write pulse width	7 ns

High Speed Memory

A bipolar 4k-word, fully static RAM[3] compares favorably with state-of-the-art MOS static RAM cell size. Chip size is 23,650 sq mils; memory cell size is only 3 sq mils/cell. Parasitic capacitances are reduced,

TRY ONE ON GOULD AND YOU DECIDE.



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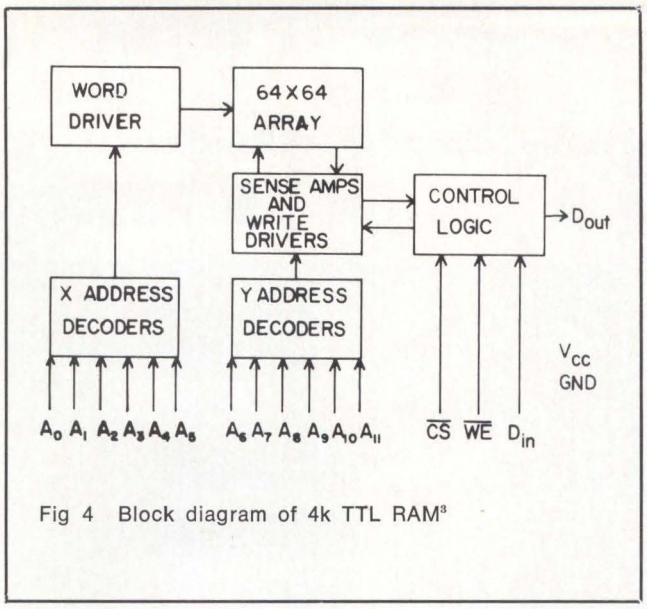

Fig 4 Block diagram of 4k TTL RAM[3]

TABLE 2

Summary of 4k RAM Power Allocation[3]

Memory array		64 mA
Address gates (12 each)		12 mA
X decode/driver		60 mA
Y decode/bit line current sink		14 mA
Output buffers		8 mA
$\overline{CE}$, D_{in}, $\overline{WE}$		3 mA
Others		24 mA
	Total	185 mA

improving memory performance. The cell has an emitter base capacitance of 0.05 pF, collector base capacitance of 0.09 pF, and collector substrate capacitance of 0.255 pF.

Architecture is conventional (Figs 4 and 5). A chip select input is provided for logic flexibility. Read and write operations are controlled by the state of the active low write enable, $\overline{WE}$. With $\overline{WE}$ held low and the chip selected, the data at D_{in} are written into the addressed location. To read, $\overline{WE}$ is held high and the chip selected. Data in the specified location are presented at the data output.

Word line discharge circuitry provides fast word line switching. Each bit line current sink is shared by 4-bit line pairs to reduce power. Performance of developmental samples manufactured to date shows typical address access of 35 ns, chip select access of 20 ns, minimum write pulse-width of 20 ns, and power of 185 mA (summarized in Table 2).

A 1k ECL RAM[4] described has typical address access time of 7.5 ns; write cycle time of 10 ns and write-enable pulse width of 3.5 ns are considered possible. Memory consists of four blocks, each 256 words x 1 bit, which can be independently selected by four block select terminals. It therefore may be used as either a 256 words x 4-bit or a 1024 words x 1-bit device.

The decoding circuit links a feedback loop from the collector circuit to the base of the multi-emitter transistor in each AND gate to equalize dc current distribution to these gates via a single current switch. Current mode operation, through driving of plural AND gates by condensed switching current, results in a very short delay time of 2.5 ns from address input to word driver output, according to computer simulation. Common-base-mode transistor switches connected between bit lines and sense circuits and cross-coupling between truth and complement in each sensing circuit reduce the undesirable effects of stray capacitances, resulting

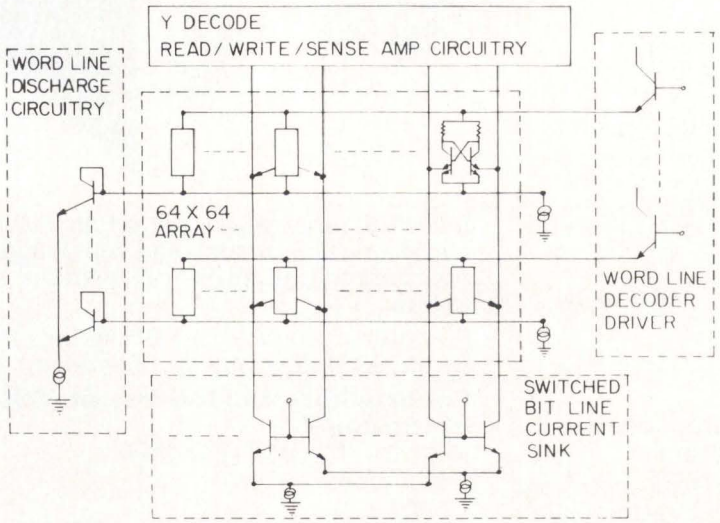

Fig 5 Schematic of 4k RAM[3]

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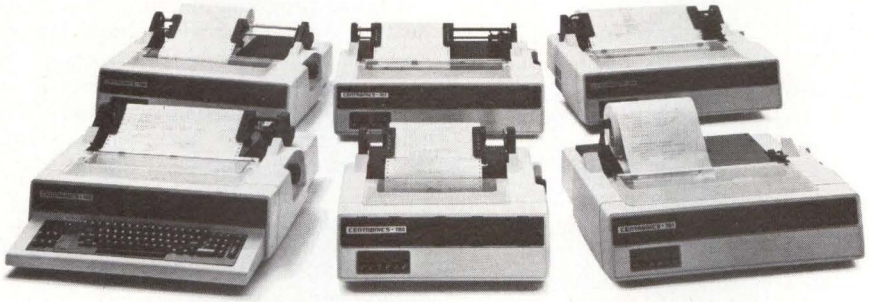
It's that simple.



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Now, the features that make our model 700 the best, lowest-priced serial printer are available in a *family of seven* models: uncomplicated modular construction; the reliability of fewer moving parts; high parts commonality; and low price. All of which means a lower cost of ownership.

The new 700 family covers a full range of serial printer requirements: 80- and 132-column format; 60 to 180 cps speed range; bi-directional and logic-seeking operations; and 110-300 baud KSR and RO teleprinters.

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in a high sensing speed. A bit line clamping circuit is effective in quick recovery of bit line potential.

Programmable Read-Only Memories

For the first time ISSCC devoted an entire session to p/ROMs. No radically new memory concepts were presented, but several proven approaches were expanded.

One word-alterable 4k p-channel ROM[5] can also be used as a block erasable p/ROM. Erase and write times are variable depending on the application and data retentivity required. All address, data, control, and clock lines are TTL compatible with pullup resistors to 5 V. Input address, data, and control lines are latched. Data outputs hold for the duration of the Chip Enable clock and then return to an open circuit condition for operation on a common data bus. Access time is 650 ns.

Four operating modes can be selected: read, write, word erase, and block erase. Circuits are provided to prevent writing or erasing of stored data during power supply application or failure.

A 336-bit MNOS EAROM[6], designed for 10-yr nonvolatile storage of data, is fully decoded and all voltages required for erasing, writing, and reading the MNOS transistors are totally controlled on chip in a manner that eliminates circuit threshold drops. All data input-output pads and all control pads are compatible with 15-V CMOS.

Memory is divided into two block-erasable banks, each containing 8 words by 21 bits. The flag is an additional MNOS nonvolatile flip-flop which selects one memory bank for reading and the other for erasing and writing. Data are entered serially to a shift register, transferred in parallel to a buffer, and then written to memory. The reverse order occurs during reading. In addition to control signals, −15 and −36 Vdc must be supplied to the chip.

Two MNOS transistors/bit are used with differential sensing. Both 2- and 3-level control circuitry are required to operate the chip.

An electrically erasable buried gate memory for moderate speed applications[7] is programmable at a much lower voltage than present p-channel floating gate memories because of the inclusion of an internal voltage multiplication technique which creates over 35 V at the selected bit for writing, but requires only a 25-V input voltage. This results in only 750-mW/chip power dissipation when programming at 1 ms/bit.

Erase time is typically 5 s at 60 V. The memory cell consists of a selection transistor, a bootstrap MOS varactor, and the memory transistor containing the buried gate.

A high performance 8k-bit erasable p/ROM[8] has been developed to meet requirements of second-generation microprocessors. Design goals of density and speed have been achieved through the development of an n-channel stacked-gate cell combined with novel peripheral circuits. Small cell size (1 mil^2) and fast memory access (450 ns max) extend EPROM performance beyond the levels established by the well-known p-channel approach.

The memory is organized 1024 x 8 bits and is fully decoded; all address and data lines are TTL compatible. Chip size is 134 x 189 mils. Within the memory array, the common-drain column lines perform the y-select function, and the top-gate lines act as x-select. Programming is accomplished by raising the selected column and the selected gate lines to a voltage of approximately 25 V. Program inhibit of unselected cells is insured by column pulldown circuits plus careful design of off levels delivered by the decoders.

One paper described an 8k-bit n-channel EAROM[9] featuring single transistor cell, standard operating voltages, and single high voltage pulse for programming and erasure, 24-pin package, TTL-compatible input/output for read and programming, static, no clock required, and low standby power. SIMOS (stacked-gate injection MOS) memory transistor accomplishes simultaneous erasure of all bits by Fowler-Nordheim emission (FNE) of electrons from the floating gate. To favor FNE instead of avalanche breakdown, a thin oxide at the erase overlap (50 nm) and a voltage ramp for erasure were used. Organization is 1024 x 8; the eight bits of a word are accessed in parallel.

A fused-link CMOS p/ROM[10] is claimed to overcome earlier limitations. Basic problem in the design is to provide the large currents needed to blow the fused-link while retaining reasonable speed for the read operation. The memory matrix and programming circuitry is p-channel, allowing the use of 30- to 35-V levels in the fuse path during programming. All other circuitry is CMOS for speed and low power.

During programming, the n-channel devices must be isolated from the high voltage levels in the fuse path. For the column lines, this requires one extra transistor per column. In the row drivers, the n-channel device is isolated by two p-channel devices when the row is not being programmed. When the row is being programmed, the n-channel device is turned on hard to limit the drain to source voltage. The source and substrate of the n-channel device can be pulled negative because they are tied to ground through a 5k resistor.

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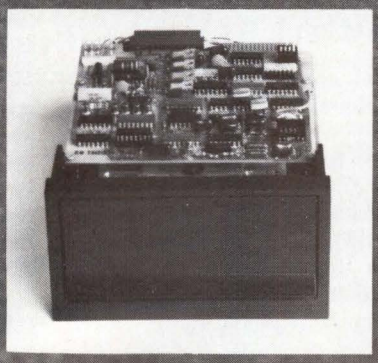


WANGCO

PERKIN ELMER DATA SYSTEMS

CIRCLE 73 ON INQUIRY CARD

4k Dynamic Bipolar RAM Offers High Performance, MOS-Competitive Price

A dynamic bipolar 4k-bit RAM using a single 5-V supply is available with maximum access time faster than the highest speed MOS 4k memories, at competitive prices. The part incorporates fast paging, controllable data latch, and two chip selects.

The standard version 93481, organized as 4096 x 1 bits, has maximum access time of 120 ns with 280-ns cycle time, both over the 0 to 70°C range with a 5-V ±5% supply. All pins meet standard TTL specifications. Power consumption is 350 mW active, 70 mW standby, and 500 mW in page mode at 5 V. A faster version, the 93481A has maximum access time of 100 ns with a 240-ns cycle time.

Page mode access and cycle times are 75 ns for the 93481 and 65 ns for the 93481A. The part provides seven addresses, ground and power, separate data-in and data-out, write enable, and a single timing control input.

Fairchild Camera and Instrument Corp, LSI Group, 464 Ellis St, Mountain View, CA 94042 uses their Isoplanar Integrated Injection Logic (I^3L) process in the design. It provides die size of 11,700 mil^2, using a single layer of metal.

A 16k-bit, 16-pin RAM with pin assignment identical to the 4k is expected to be available for prototyping in the last half of 1977. Users of the 4k RAM will not need to make board changes since both RAMs will work in the same sockets, thereby enabling a quadrupling of memory density at the board level. Speed and power for the 16k RAM will be within the range of the 4k RAM.

Available in standard 16-pin ceramic DIPs, the 93481 is priced at $24, and the 93481A is $31.20, in 100 quantities. Prices at 10k and 50k pieces for the 93481 are $8.78 and $7.64, respectively.

Circle 350 on Inquiry Card

EAROM Has 950-ns Access Time

Individual words on the ER3401, a 1024 x 4 EAROM, can be erased and rewritten without any effect on the rest of the memory. Designed with p-channel MNOS technology, the word-alterable device requires 10-ms erase and 1-ms write times and has access time of 950 ns. It is TTL-compatible with resistor pull-ups.

Unpowered, nonvolatile data storage is guaranteed for 10 years by the manufacturer, General Instrument Corp Microelectronics, 600 W John St, Hicksville, NY 11802. The device is available in a 22-pin ceramic package at $32 each in 100 quantities.

Circle 351 on Inquiry Card

Program Lowers Cost of Custom LSI Development

Six years of experience in developing more than 300 custom microcircuits is the basis for REACT (rapidly evaluate and apply custom technology). The low cost system enables development of custom LSI circuits in from three to six weeks and at a cost of $18k to $38k.

Based on a repertoire of optimized logic functions rather than a library of gate arrays, cells, or mask-programmable chips, the system is expected to help improve designs of microprocessor-based portable electronic equipment. Micro Power Systems, 3100 Alfred St, Santa Clara, CA 95050 states that its HD/CMOS process will be predominantly used in the program.

Although efficient, the system will not solve all problems. Some special requirements will still incur substantial development costs.

Circle 352 on Inquiry Card

ADC and Controller Form 2-Chip 12-Bit Data Acquisition System

Two announced IC chips—a monolithic analog-to-digital converter building block and a digital controller—which combine to form a low cost, high accuracy 12-bit (plus sign) binary data acquisition system are claimed to be industry firsts. The LF13300 ramp or integrating type A-D device is said to be the first to combine junction field effect and standard bipolar transistors on the same chip; and the ADB1200P controller is the first 12-bit converter in volume production using p-MOS metal gate processing. Both parts are available from National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051.

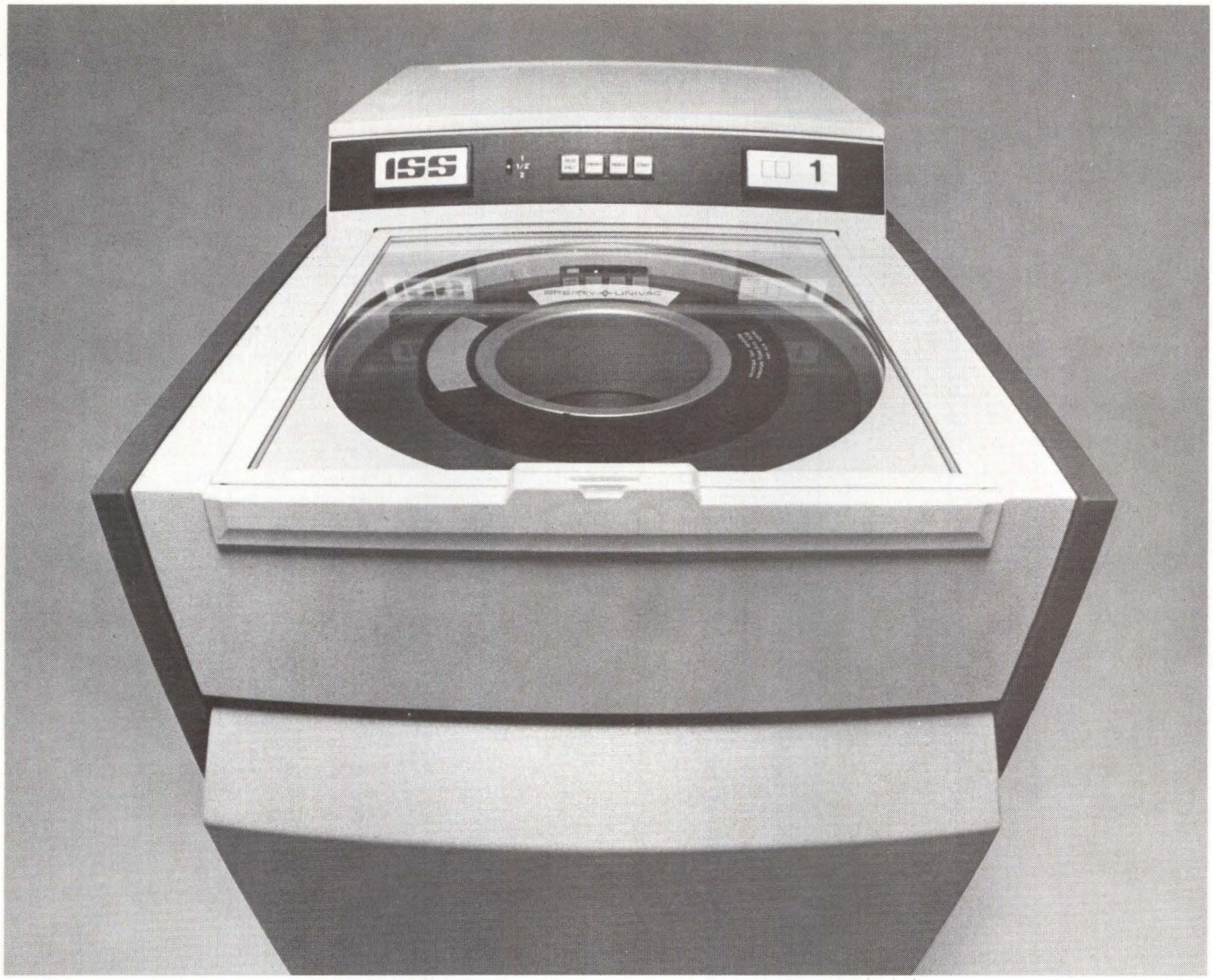
The analog chip, fabricated by the bi-FET process, combines bipolar op amps with j-FET input stages and j-FET analog switches with bipolar drivers to form high impedance unity gain buffer stage, integrator, and 9-element analog switching stages. It features 570-mW power dissipation, ±5- to ±18-V power supply range, ±11-V analog range with ±15-V power supplies, automatic offset correction, and compatibility with both CMOS and transistor-transistor logic. The 18-pin device includes automatic zeroing in its integrator, comparator, and buffer amplifiers, and provides an input impedance of >1000 MΩ. Slew rate of the on-chip op amp is 28 V/μs; bandwidth is 3 MHz, and open loop gain is 7 V/mV. Response time of the on-chip comparator is typically 2.5 μs.

The 110 x 110-mil digital controller building block, on a 28-pin DIP, provides all the necessary control functions plus such features as auto zeroing, polarity and overrange indication, and continuous conversion. Other features include either serial or Tri-State parallel outputs, TTL compatibility, and 100% overrange capability. It requires 5- and −15-V power supplies and is capable of operation at clock frequencies up to 500 kHz.

Together the devices operate at a conversion time in the 30 to 40 ms range on a clock frequency of 250 kHz. The 2-chip system has a nonlinearity of ±½ LSB max. Gain error drift is ±1 ppm/°C and zero reading drift is only ±0.5 ppm/°C.

Active Filter Modules Function With Low Speed IC Modems

Series 207C300 transmit and 207C400 receive active filter modules, when used with an appropriate modem, will provide all necessary filtering for originate only, answer only, or answer/originate operation. They may be employed with either user-



Our 100/200 megabyte OEM disk drives. Best for you. Best for your customers.

The new ISS 733-10/11 disk drives are the most advanced random access storage devices ever designed for the OEM market. With features that benefit you *and* your customers.

For example, exceptional speed in head positioning and start/stop times. Compactness. Quietness. Easy waist-high pack loading.

The big news, however, is their field-upgrade capabilities. The 100-megabyte 733-10 can be easily field-upgraded to 200 megabytes. Or you can have 200 megabytes immediately with ISS 733-11. And both can be ordered with, or field-upgraded to, dual port.

Advanced interface design
Our interface permits functional compatibility between ISS 733-10/11 and most current 40, 80, 100, 150, 200, and 300-megabyte drives. This means minimal controller modifications, if any.

Performance features
Integral power supply. Tolerates wide power variations, reduces susceptibility to cycle sags and brown-outs.

Module select plug. Permits flexibility in disk address assignments in multi-drive systems.

Data separation and write data precompensation. All data encoding/decoding is performed in the drive.

Absolute cylinder addressing. Disk addressing done in the drive, not the controller. Simplifies programming.

Industry standard media. 3336-1 and 3336-11 or equivalent disk packs.

Programmable sector mark. Allows user to select sector size to fit his application.

Rotational position sensing. Signals the system when the desired sector is approaching the read/write heads. Increases system throughput.

Daisy chaining. Greatly reduces cabling.

Important options
Dual port. ISS 733-10/11 can be upgraded from single to dual port in the field. Or dual port can be installed prior to delivery.

Address mark format. Permits variable record lengths.

Round-the-clock ISS support
ISS maintains a complete support facility. Not just spares, but also technical assistance is available round-the-clock. Just call.

We'll be glad to send more information about the ISS 733-10/11. Write or call ISS Marketing, 10435 N. Tantau Ave., Cupertino, CA 95014, (408) 257-6220. ISS is an operating unit of Sperry Univac.

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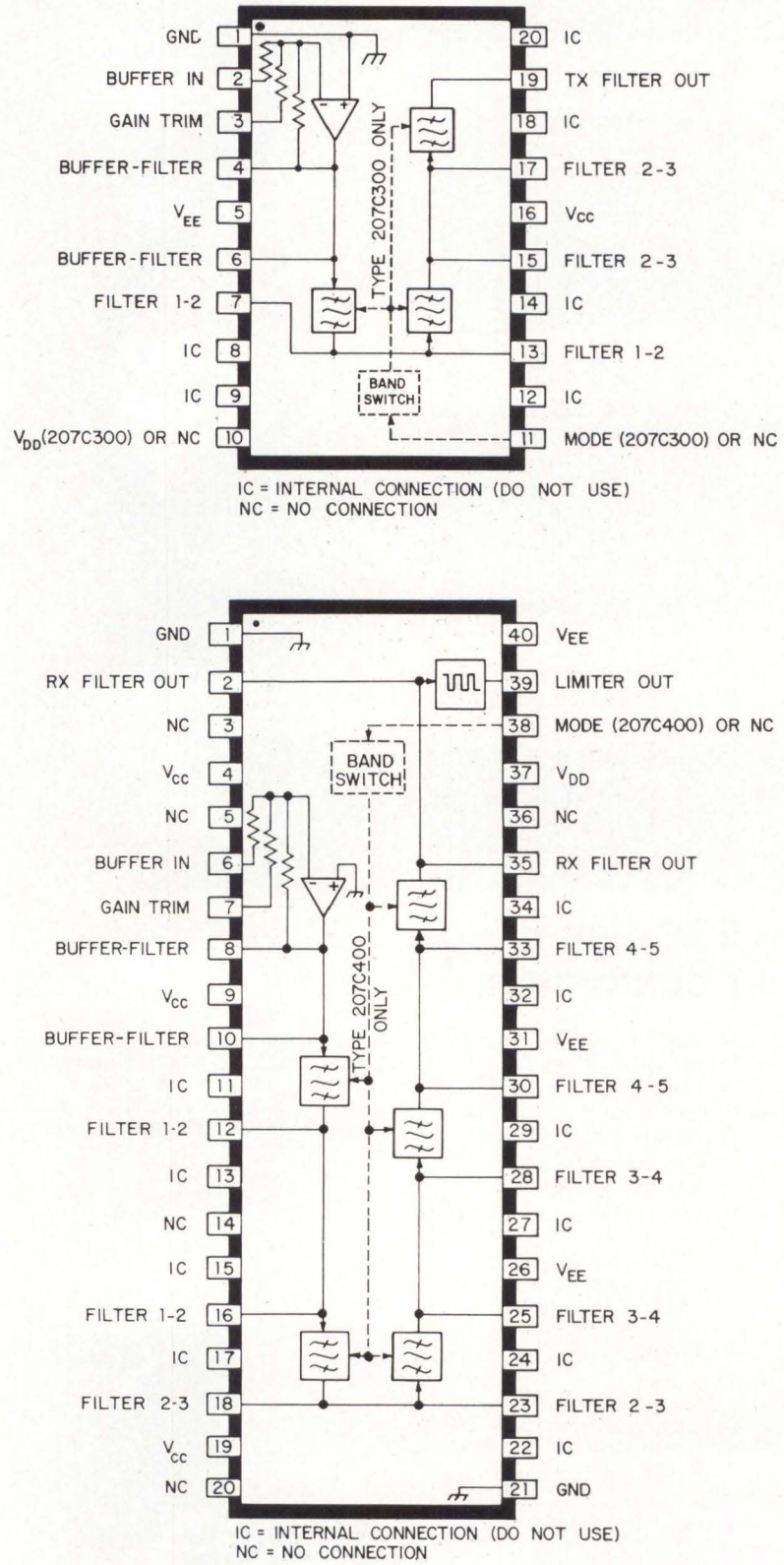

Sprague Electric series 207C300 transmit (top) and 207C400 receive active filter modules. Dotted lines in each diagram show answer/originate switching capability included in only two types of the 6-device series

built or commercially available IC modems.

Transmit modules include a 6-pole active filter to suppress output sidebands and to reduce harmonic distortion. Type 207C300 is switched between answer and originate modes by means of a mode signal which can be obtained from standard low level digital logic, 207C301 is a low band module designed for originate only applications, and 207C302 is a high band module designed for answer only applications. Each device has an input buffer amplifier with jumper-selected gains of 0 or 20 dB. Intermediate gains may be user-selected via an appropriate external resistor.

Receive modules include a 10-pole active filter to eliminate noise and local carrier signals. Type 207C400 also accomplishes answer/originate switching with a mode signal, 207C401 is a high band module designed for originate only applications, and 207C402 is a low band module for answer only applications. These devices also include the input buffer amplifier with selectable gains between 0 and 20 dB, and feature a symmetrical output limiter to provide equal half-cycle periods to the demodulator.

Absolute maximum ratings for the devices, manufactured by Sprague Electric Co, North Adams, MA 01247, include supply voltages of 18, −18, and 5.5 V (V_{CC}, V_{EE}, and V_{DD}, respectively); and temperature ranges of 0 to 70 and −40 to 125°C (operating and storage, respectively).

Circle 353 on Inquiry Card

Op Amp Has 3 Times Unity-Gain Bandwidth

Characteristics and package options of the MC4558/MC4558C dual operational amplifier are fully compatible with the "industry standard" MC1558/MC1458—and can be plugged directly into sockets of existing designs—but the newer device has three times as much unity-gain bandwidth. Features include 2.8-MHz guaranteed unity-gain bandwidth, internal compensation, short circuit protection, gain and phase match between amplifiers, and low power consumption.

Maximum ratings of the device from Motorola Semiconductor Prod-

INTRODUCING AN INNOVATION IN DISC CONTROLLER DESIGN

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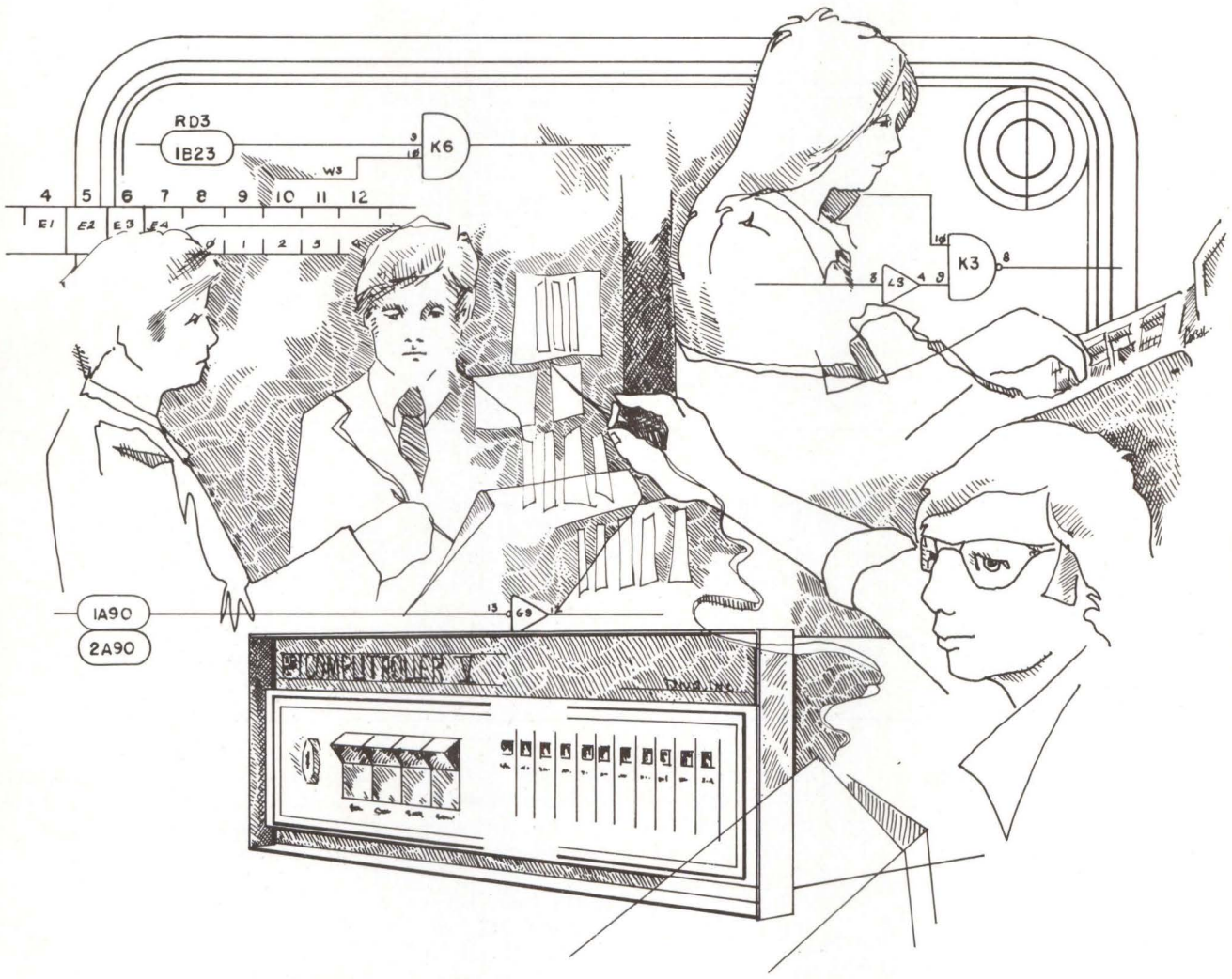

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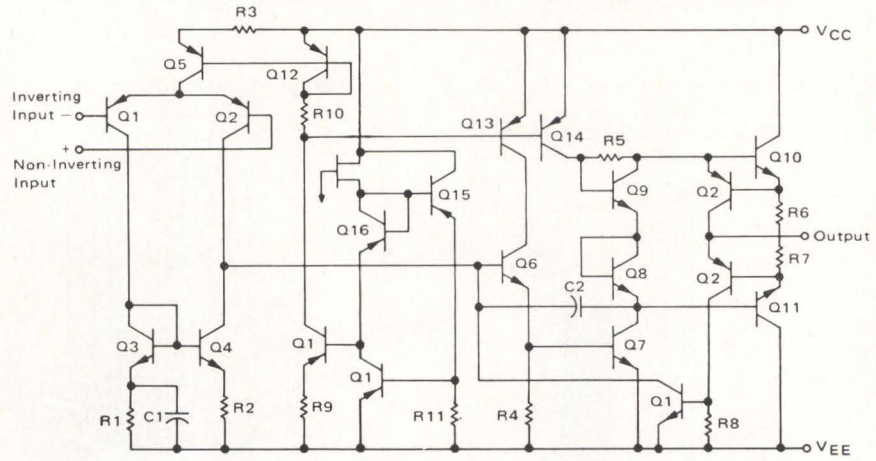
CIRCLE 75 ON INQUIRY CARD



Equivalent circuit schematic for Motorola Semiconductor MC4558/MC4558C dual operational amplifier

ucts Inc, PO Box 20912, Phoenix, AZ 85036 include power supply voltages (V_{cc} and V_{ee}) of + and − 22 Vdc (MC4558) and + and − 18 Vdc (MC4558C); input differential voltage (V_{ID}) of ±30V; input common mode voltage (V_{ICM}) of ±15 V; operating ambient temperature ranges of − 55 to 125°C (MC4558) and 0 to 70°C (MC4558C); and storage temperature ranges of −65 to 150°C for metal and flat ceramic packages and −55 to 125°C for flat plastic packages.

Prices of the MC4558 and MC 4558C, respectively, in 100 to 999 quantities are $2.20 and $ .90 for metal packages and $2.10 and $ .90 for ceramic. A plastic version of the MC4558C is available at $ .80.

Circle 354 on Inquiry Card

Schottky RAMs Provide Improved Speed vs Power Performance

Each of four low power Schottky RAMs features fully static operation, low current pnp inputs, industry standard pinouts, and fully static operation. SN74LS214 and -314 are, respectively, 3-state and open collector 1024 x 1 devices with 0.2-mW/bit power performance and 75-ns access time. 74LS200A and -300A, 3-state and open collector, respectively, are 256 x 1 devices with 1-mW/bit power performance and 35-ns access time.

In 16-pin plastic DIPs from Texas Instruments, Inc, PO Box 5012, Dallas, TX 75222, the 214/314N sell for $17.60 each in lots of 100 or more; the 200A/300AN sell for $3.60. All devices are available in ceramic packages.

Circle 355 on Inquiry Card

8-Bit D-A Converter Features Improved Performance

As a very high performance grade of the DAC-08 series 8-bit multiplying DAC, the DAC-08H from Precision Monolithics, Inc, 1500 Space Park Dr, Santa Clara, CA 95050 has a settling time of 135-ns max, nonlinearity of ±0.1% (±¼ LSB) max, and output current which is matched to the reference input current within ±1 LSB to eliminate the need for calibration. Complementary current outputs with −10- to 18-V compliance allow conversion to a voltage without an external op amp. Direct interface to TTL, DTL, n-MOS, CMOS, and MECL is accomplished using a voltage-programmed logic threshold control pin.

Specified over 0 to 70°C, the 16-pin hermetic DIP converter is useful in high speed ADCs, industrial control process current DAC designs, and in low power or battery-operated applications. Power consumption is 33 mW with ±5-V supplies and 135 mW with ±15-V supplies.

The DAC-08 has recently been second-sourced by four other IC manufacturers. This is claimed to establish the fast, low power, high compliance device as the first "industry-standard" DAC.

Circle 356 on Inquiry Card

1k and 2k Bipolar p/ROMs in Two Versions

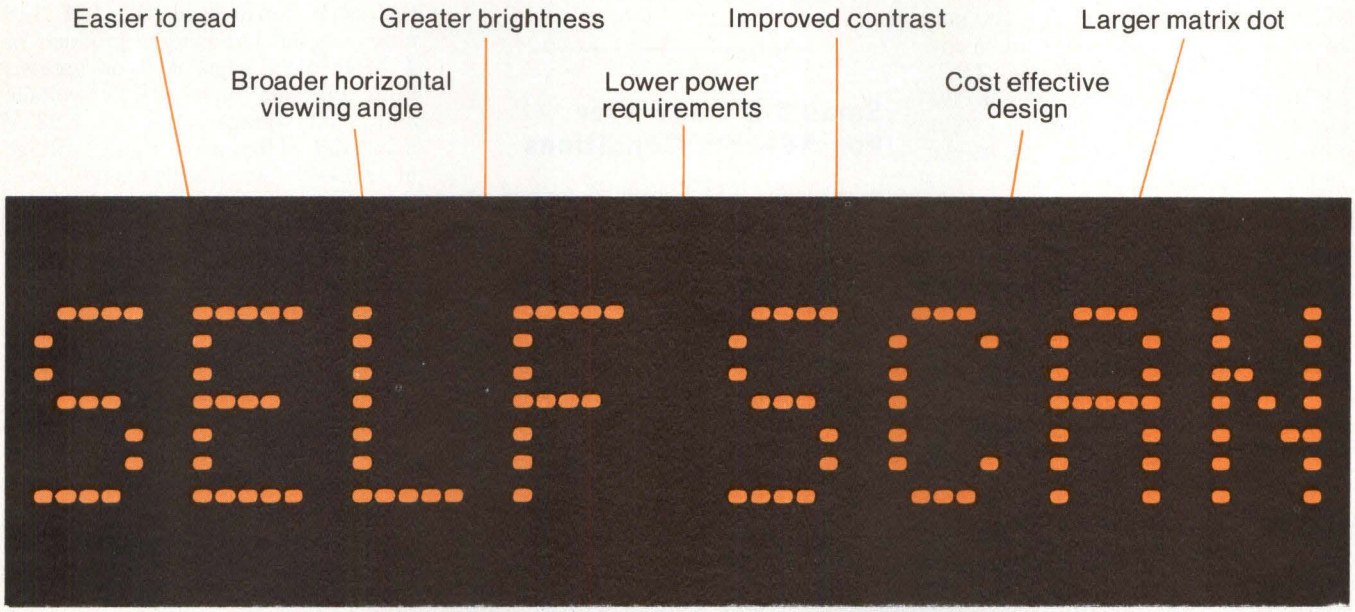
Industry standard bipolar 256 x 4 and 256 x 8 programmable read-only memories—the first available from this company—have been announced by Raytheon Semiconductor, 350 Ellis St, Mountain View, CA 94040. Both are designed with nichrome fuses.

The 1k device in a 24-pin configuration (designated 29660 and 29661 for open collector and 3-state versions, respectively) has access time of 70 ns for a 0 to 70°C range commercial version and 80 ns for a −55 to 125°C range military type. Power dissipation is 400 mW.

The 2k 29600 and 29601 (open collector and 3-state, respectively) have 70-ns access time at 25°C with 400-mW power dissipation. Both 20- and 24-pin versions are available.

Circle 357 on Inquiry Card

TAKE A CLOSE LOOK AT THESE BURROUGHS PLASMA DISPLAY BREAKTHROUGHS.

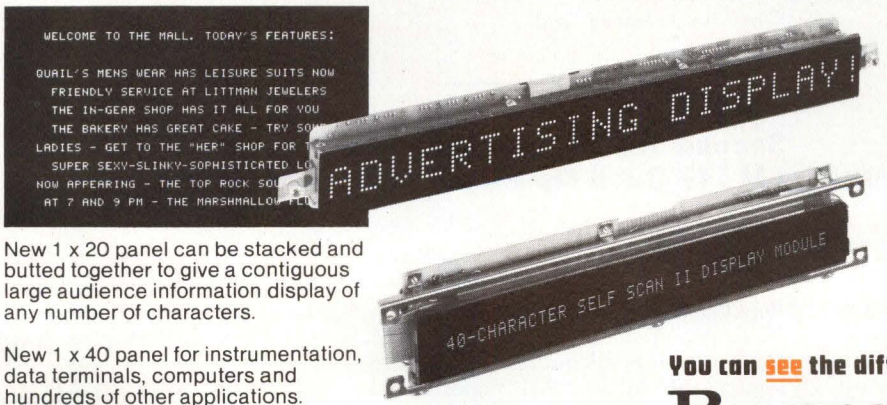


The new Burroughs SELF-SCAN® II single register gas plasma panels are breakthroughs in visibility and readability, making them ideal for all types of applications — from audience information displays to instrumentation applications. They are digitally addressed to interface easily with microprocessors and computers.

Only 15 connections are required. These new units complement Burroughs' standard line of single register 16 and 32 character plasma displays.

The Burroughs SELF-SCAN II 1 x 20 and 1 x 40 displays. Certainly worth looking into.

Burroughs Corporation, Electronic Components Division, P.O. Box 1226, Plainfield, New Jersey 07061. Telephone (201) 757-5000. SELF-SCAN displays are available nationwide through our distributors, Hamilton/Avnet and Cramer Electronics.



New 1 x 20 panel can be stacked and butted together to give a contiguous large audience information display of any number of characters.

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CIRCLE 76 ON INQUIRY CARD

RAM Useful for Systems With Battery Back-Up

SY5102, a 1k x 1 CMOS static RAM, is a pin-replacement for the industry standard SY2102. When not enabled, it remains in standby, dissipating only 1 mW at full 5-V power conditions and eliminating the need for expensive power-down circuitry. Even when operating, its power consumption is said to be low.

Because it will maintain memory at 2 V, it can be used for systems that have battery back-up for nonvolatility. A 16-pin ceramic DIP, SY5102-3, with an access time of 650 ns, is available from Synertek, 3050 Coronado Dr, Santa Clara, CA 95051 at $15.45 each for 100 pieces.

Circle 358 on Inquiry Card

Decoder-Driver Controls Large Area LCDs

A p-MOS BCD-to-7-segment decoder-driver with latch is claimed to enable an inexpensive technique for controlling and driving large area liquid crystal devices. The circuit, from Ashley-Butler, Inc, 208 U.S. Highway 206S, Somerville, NJ 08876, permits drive voltages of at least 50 V to be used with displays having digit sizes ranging from 1.5 to 6" (3.8 to 15 cm) or larger.

It will interface directly with CMOS and TTL and has the same pin assignment as the Motorola MC 14543. Limited alphanumeric capability is provided using the normally not allowed BCD codes.

Circle 359 on Inquiry Card

EPROM Prices Cut By More Than 50%

American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051 has reduced prices on three of its EPROM (erasable/reprogrammable read-only memory) by more than 50%. New 100 to 999 quantity prices are $9.95 for the S5204A and S6834-1 circuits and $10.95 for the S6834. According to the company, these prices provide cost-per-bit-of-memory storage at far less than for competitive devices.

The 512 x 8 AMI S6834 is TTL-compatible, has a 575-ns access time, and can be programmed in 42 s. Circuits are onboard programmable with R/W, CS, and V_{PROG} pins and are compatible with the company's 6800 microcomputer family. The S5204A, also a 512 x 8 device with onboard programmability, has 750-ns access time and 3-state data I/O. It operates with standard power supplies of 5 and −12 V.

Circle 360 on Inquiry Card

Small S-D Converter For Adverse Conditions

A thick-film LSI hybrid, described as the industry's smallest synchro-digital 14-bit converter, the HSDC-14 is designed for operation in environments in which conventional discrete converters cannot hold up. It has a dc velocity output signal and requires only a 15-V power supply in addition to a logic voltage. Power requirement is 750 mW.

The converter consists of two 0.8 x 1.9 x 0.21" (2 x 4.81 x 0.53 cm) 36-pin DIPs and is SEM-compatible, meeting MIL-STD-883 level C, with level B optionally available. Accuracy is ±4', ±0.9 LSB worst case error.

Separating the solid-state control transformer and error processor permits greater flexibility for such S-D functions as ECDX and 2-speed conversion. ILC Data Device Corp, Airport International Plaza, Bohemia, NY 11716 claims the unit is the ideal converter for remotely located, difficult-access equipment where high MTBF is required.

Circle 361 on Inquiry Card

Second Source For LM 148 Quad Op Amps

Said to be the first devices to provide identical functional characteristics, second source versions are being offered by Intersil, Inc, 10900 N Tantau Ave, Cupertino, CA 95014 for National Semiconductor's LM 148 family of quad 741 operational amplifiers. They can be substituted directly with no change in circuit performance.

The Intersil LM 148 is made up of four independent, high gain, internally-compensated, low power op amps, each of which has total supply current comparable to the supply current of a single 741-type op amp. Key specifications include 0.6-mA/amplifier supply current drain; 1-mV input offset voltage; 4-nA input offset current; 30-nA input bias current, and 120-dB isolation between amplifiers.

An available LM 149 version has the same features as the LM 148 plus a gain bandwidth product of 4 MHz at a gain of 5 or greater. Both versions have supply voltage and input voltage ratings of ±22 V max and differential input voltage of ±44 V max, and operate over the temperature range of −55 to 125°C.

Prices for 100 to 999 quantities range from $1.25 for the LM 348N/349N (commercial temperature range) in an epoxy DIP to $6.00 for the LM 148D/149D (military temperature range) in a ceramic DIP.

Circle 362 on Inquiry Card

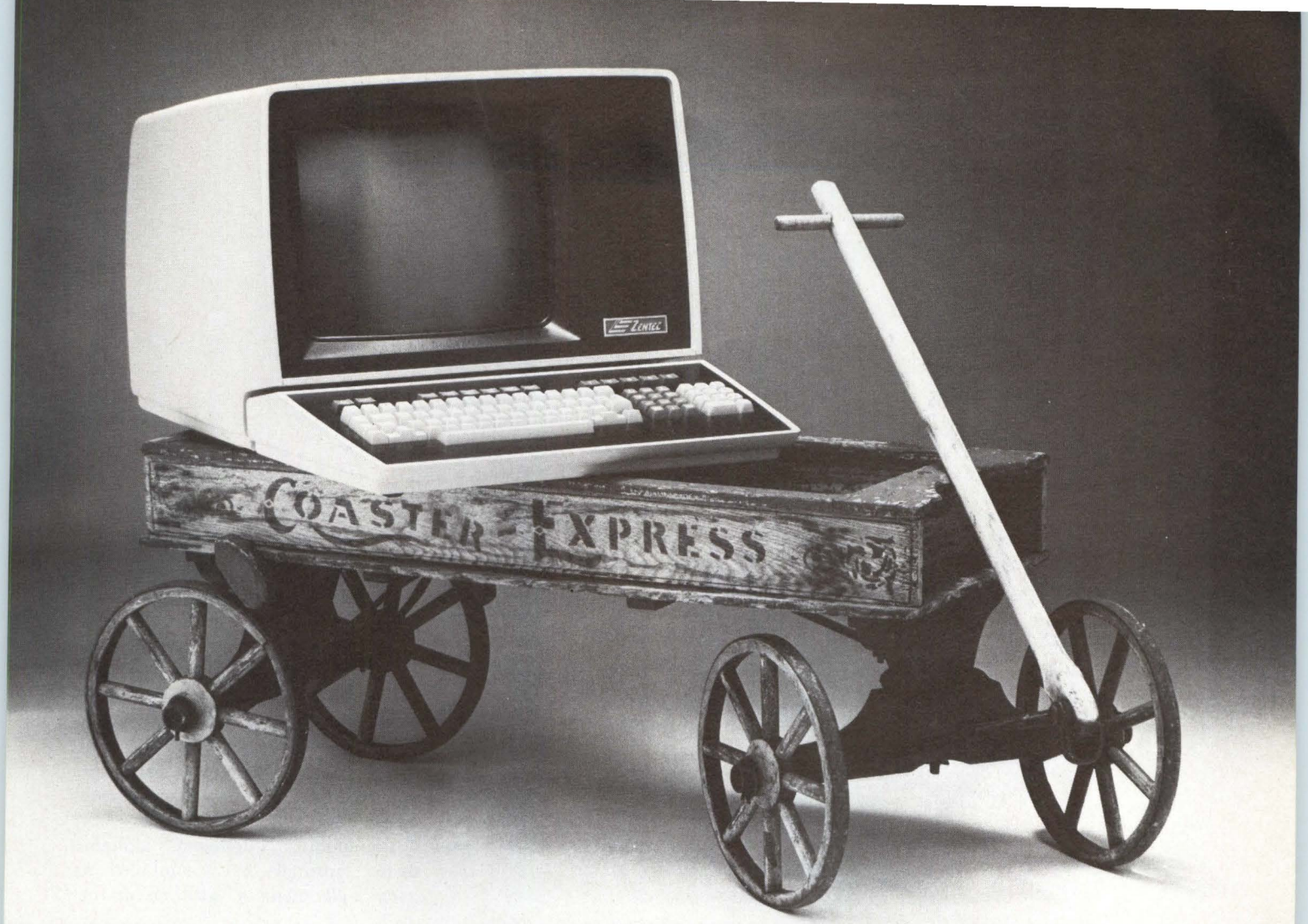
Multiplier and ADC Receive DoD Awards

A high speed multiplier and an analog-to-digital converter circuit have been selected by the Dept of Defense Advisory Group on Electron Devices as two of the ten most significant technical achievements of 1976. Both of these LSI circuits were developed by the TRW Defense and Space Systems Group's Microelectronics Center, 1 Space Park, Redondo Beach, CA 90278.

Just over 0.25" (0.64 cm) square, the 16-bit bipolar multiplier silicon chip contains more than 17,000 electronic components. It can multiply two 16-bit numbers to produce a 32-bit answer at better than 5M times/s. As a commercial device it is sold by the Electronic Systems Div for under $300.

The ADC is a higher performance, radiation-hardened version of a device that won a similar DoD prize for 1975. It samples and converts random analog changes at the rate of 10M/s. Commercial devices are expected to be marketed early this year. □

Circle 363 on Inquiry Card



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And the 9003's flexible bus architecture lets you add up to 64K bytes memory, telecommunications interfaces, our printer and flexible disk subsystem. Even your own customized interfaces. The Zentec 9003 Microcomputer keeps right on growing as you do.

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Philadelphia (215) 688-7325 • TWX 510-668-2995
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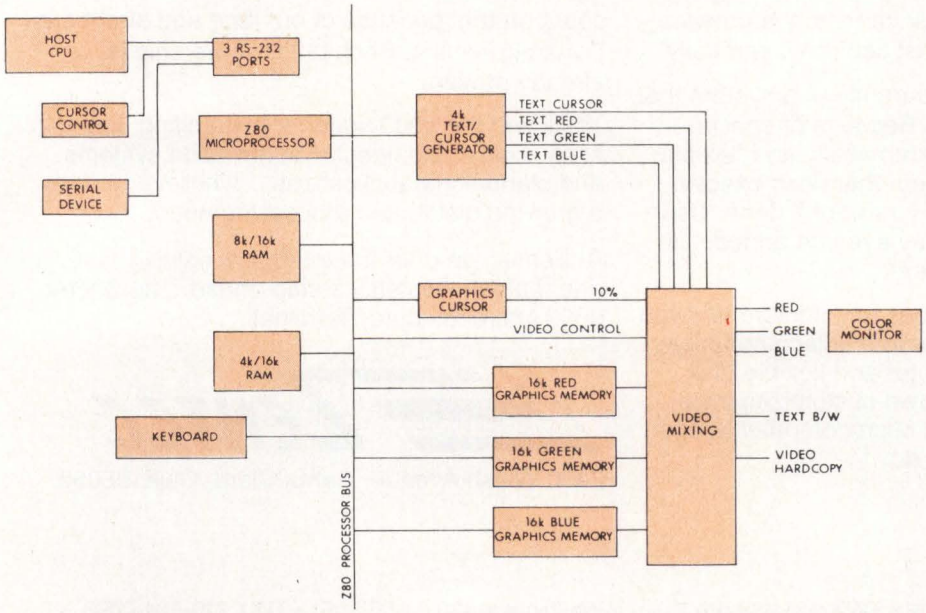
West Germany (0611) 590711 • TLX 841-413822
Austria 425451 or 421675 • TLX 847-74737
Switzerland 041-831043 • TLX 845-72231

PRODUCT FEATURE

Single Architecture Terminal Combines Graphic and Alphanumeric Capabilities

An intelligent terminal that not only combines alphanumeric and graphics display capabilities but also allows the user to choose between color and black and white in a single unit has now been introduced. The user can employ the same hardware/software set to solve both alphanumeric and graphics problems, thereby saving a considerable portion of software development costs.

Commonly, intelligent alphanumeric terminals have combined an ASCII byte memory with an on-the-



Block diagram of Ramtek Micrographic dual-capability terminal

fly character generator to drive a raster scan video display. Bit-per-element graphic display systems, on the other hand, have used a bit plane of memory in which each memory element corresponds to a raster scan display element. The Micrographic™ terminal introduced by Ramtek Corp combines both architectural approaches.

Functional Description

Internal operations of the terminal are completely controlled by a Z80 microprocessor which operates at a 2.8-MHz rate and activates or inhibits visual display of any of three graphic bit planes as well as the on-the-fly character generator. When the three 16k-byte graphic planes are not being displayed, they may be utilized as page buffer storage for the alphanumeric display, providing 24 pages of buffer memory to the display when used as an intelligent alphanumeric terminal.

Z80 software is contained in up to 16k bytes of p/ROM. Character input buffer and temporary program storage for the Z80 are supplied by 4k bytes of RAM (expandable to 16k bytes).

Two cursors are provided, one for control of alphanumeric entry and the other for use as a crosshair cursor in the graphics mode of operation. Three RS-232 serial ports for connection to the host computer, a cursor control mechanism, and other serial peripheral devices such as line printers are offered.

The keyboard is made up of a 61-key typewriter layout, a 12-key cursor/function pad, and a 12-key numeric/function pad. In addition, 16 special function keys may be assigned for optional features. Special N-key rollover and auto repeat features are provided.

Special video mixing logic combines the three graphics bit-per-element planes with the on-the-fly character generator. These mixing circuits allow the microprocessor to control which planes are displayed and to cause various colors to blink under software control.

Note on the block diagram that all of the terminal functions are on the Z80 processor bus. This microprocessor monitors the three RS-232 ports for transmissions from the host CPU and interprets the ASCII input for loading either the text/alphanumeric cursor generation memory or a combination of the three color graphics memories. Text and graphics memories form a part of the microprocessor address space.

Video mixing circuits mix text, color, alphanumeric characters, graphics cursor, and the three color graphics memory planes. These circuits provide the red, green, and blue drives to the color graphics monitor; the text black and white output, which can drive a black and white monitor; and a hardcopy output, to drive a video printer. Therefore, the color monitor within the case can be driven simultaneously with a separate black and white monitor and video hardcopy printer.

The microprocessor contains an instruction set for manipulation of 16-bit address quantities as well as instructions which assist in DMA transfers. It also provides the dynamic RAM refresh function which reduces the amount of logic required.

All internal functions of the terminal are either memory or peripherals to the microprocessor, facilitating generation of software self-test diagnostic capability which can isolate malfunctions down to the card level. A self-test indicator on the keyboard tells the operator that the terminal is operating when power is turned on.

Users can choose either the graphics interpreter language supplied by the terminal manufacturer or write specific software for the microprocessors in order to optimize the terminal for particular applications. The graphics interpreter language allows users to draw graphic entities such as boxes, vectors, and conics; and associated editing and debug features enable users to generate and modify complex graphic pictures. To minimize software development costs, packaged portions of the interpreter language can be used along with the specialized software.

Specifications

The bit-per-element graphics display memory comprises up to three planes of 256 lines by 512 elements (2000 bytes), while the on-the-fly alphanumeric display memory consists of 25 lines of 80 ASCII characters/line. Alphanumeric characters are in a 5 x 7 font (7 x 10 matrix including cursor control). Black and white screen size is 14″ while color is 13″ diagonal. Refresh rate is 60 Hz.

Cursors for alphanumeric and graphics have separate controls. Each alphanumeric character may have color specification, blink, visibility, and cursor.

Communications capabilities are synchronous or asynchronous, 110 to 9600 baud program selectable, full or half duplex, and character or block mode. Parity is odd, even, or none; characters are 10 or 11 bit; interface is RS-232-C; and three serial ports are provided.

The terminal can be provided either encased or as a stripped down rack-mounted chassis. Size is 20.75 x 17.5 x 32.5″ (52.7 x 44.5 x 82.55 cm) including detached keyboard.

Power requirements are 11/220 Vac ±10%, 50/60 Hz. Operating temperature range is 5 to 40°C, 10 to 90% relative humidity, noncondensing.

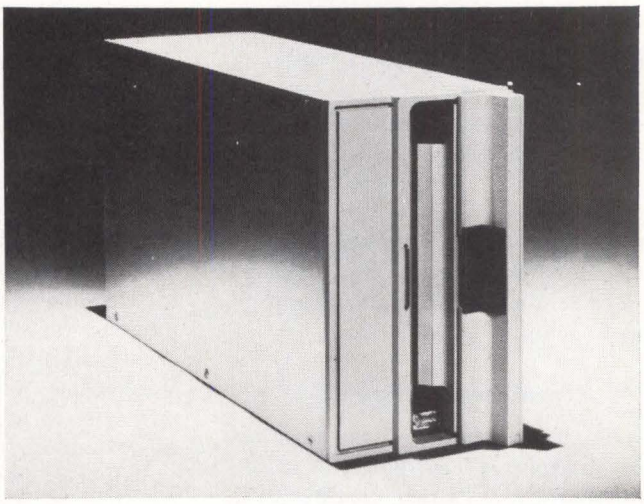
Price and Delivery

Basic Micrographic systems start at $5150 each for color and $4495 for black and white. OEM quantity discounts are available. Deliveries are scheduled to begin in July. Ramtek Corp, 585 N Mary Ave, Sunnyvale, CA 94086. Tel: (408) 735-8400.

For additional information circle 199 on inquiry card.

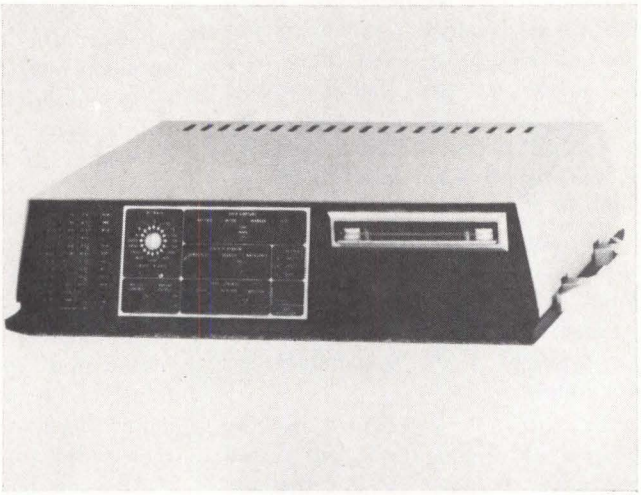
PRODUCTS

Multifunctional Floppy Disc Drive Provides Instant Switch Selection of Features



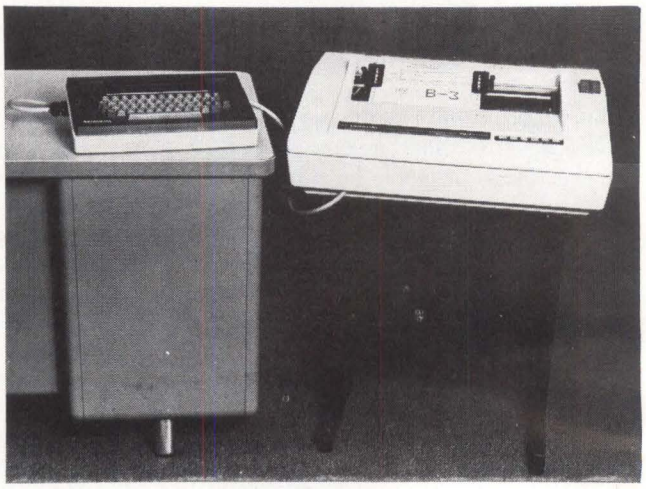
Affording flexibility in the selection of six built-in operational modes, the 142M floppy disc drive contains a 6-position rocker switch built into the drive's PC board. Selectable functions include hard or soft sectoring, gating of "write protect" or "ready" with select, stepper motor power control, and separation of data and clock. Enabling use of either IBM 3740 or user-selected formats, the unit performs as a single (243k bytes) or double (650k bytes) density drive requiring no additional control logic. LSI technology provides increased reliability. Plug-compatible with the firm's 140 (single density) and 142 (double density) floppy disc drives, this 6400-bit/in, 48-track/in unit has an access time of 6 ms track-to-track. Transfer rate is 500k bits/s. Other features include a range of power choices, signal line terminator connector in the drive, and an auxiliary power connector. **California Computer Products, Inc,** 2411 W La Palma Ave, Anaheim, CA 92801.
Circle 200 on Inquiry Card

Independent System for Digital Data Communications Networks Records in Real-Time



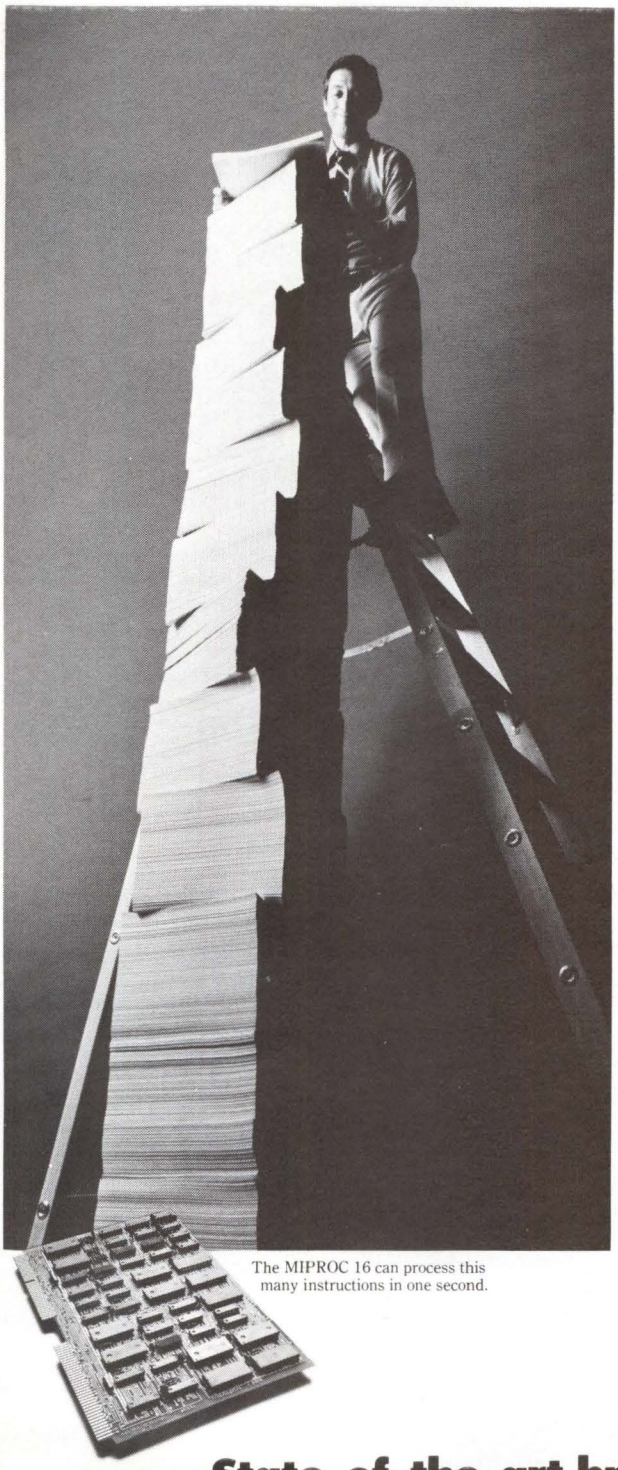
The DATATAPE recording system which records data in real-time at switch-selectable rates from 50 to 19,200 bits/s can accept ASCII, EBCDIC, SDLC, or any other async, bisync, unisync, or isosync line discipline. In the usual operating mode, the unit records full-duplex data and up to six control or status signals at up to 9600 bits/s. Signals, derived from a standard RS-232 interface, can be eliminated at higher data rates. Full tape cartridge capacity is 23M bits of unformatted data. Switch-selectable playback rate permits slow down or acceleration for analysis and troubleshooting operations. The portable instrument weighs 25 lb (11.25 kg) and measures 5 x 20 x 17.5" (12.7 x 50.8 x 44.45 cm). RS-232 plug-compatible with mainframe and terminal equipment, the unit can easily be installed in the system; other interface adapters and accessories are also available. Unit operates on either 110 or 220 Vac (±10%) at 47 to 63 Hz. **Epicom, Inc,** Altamonte Springs, FL 32701.
Circle 201 on Inquiry Card

Programmable Printer Combines With Keyboard/Display in Reconfigurable System



Dedicated to specific materials handling applications and easily reconfigured as requirements change or new applications develop, the IPS-7/KD programmable printing system combines a compact data input station with a 120-char/s printer configured around a microcomputer with 10k bytes of memory. Input station consists of a 32-char gas discharge display and 64-char ASCII-compatible keyboard. Linked to the printing system via a 5-ft cable, station permits direct communication with a central computer, data access via keyboard, or message receipt on the display. Station adds system backup potential and interactive communications capability to earlier IPS-7 versions. System has processing power to operate in a standalone mode, or in a local or remote mode within an online system. Double input and output buffering is a std feature which can increase printer throughput up to 50% when used in a serial communications mode. **Dataroyal, Inc,** Nashua, NH 03060.
Circle 202 on Inquiry Card

Introducing 4 MHz microcomputing



The MIPROC 16 can process this many instructions in one second.

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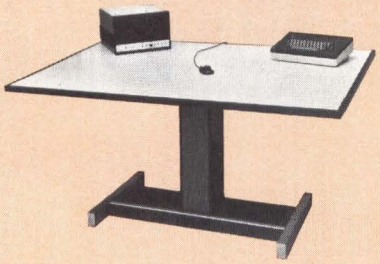
CIRCLE 78 ON INQUIRY CARD

? WHY A NEW DATA TABLET/GRID DIGITIZER...



. . . AND AT LOWER COST*

Because there are . . .

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No wire tension aging problems
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Because *NEW* means significant performance and cost benefits over other data tablets to the OEM or end user™ resulting from the unique DATATIZER design principle (patent pending).

Check out the advantages of GTCO's electromagnetic absolute coordinate approach. For simplicity, accuracy, stability, reliability and low cost it can't be beat.

The DATATIZER uses a free cursor/stylus to convert all types of maps, drawings, charts, graphic documents, etc., into digital form. X-Y coordinates are electronically generated many times each second allowing the cursor to be lifted and the work surface to be unobstructed for unrestricted operational freedom.

If you are using or plan to use a tablet or grid digitizer for any graphic data or interactive CAD application, you will appreciate the widest range of optional features now available and the flexibility of the all new GTCO DATATIZER.

Size:	11" x 11" to 42" x 60"
Resolution:	.010" or .001", inch or metric
Coding:	BCD or Binary
Cursor:	Crosswire or stylus
Origin:	Absolute or re-locatable
Design:	All electronic, no adjustments
Display:	X-Y plus sign
Mode:	Point, line and remote
Add Ons:	Keyboard, stand, format programming, calculations, special sizes
Interfaces:	Parallel, serial, RS232, keypunch mag tape, mini, calculator, paper tape, terminal, cassette, etc.
Construction:	Modular, printed circuit tablet, 4 basic plug-in boards for ease of repair, stand alone, includes all necessary power supplies and cables.
Power:	115-220V, 47-63 Hz

*Basic OEM unit, qty. 25-49 prices, 11" x 11" - $1600, 20" x 20" - $1900, 30" x 36" - $2800, 36" x 48" - $3100, and 42" x 60" - $4200.

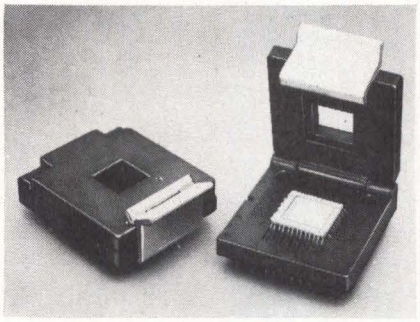
GTCO Corporation
1055 First Street
Rockville, Maryland 20850
(301) 279-9550, 424-7077

PRODUCTS

SOLID-STATE UPS MODULE

Compact, portable 910 module supplies a constant dc voltage for up to 2 h to any electronic instrument (within its power rating) that uses an offline switching-regulator power supply in the event of line-voltage deterioration or outright failure. Operating from a 100- to 130-Vac or 200- to 260-Vac, 47- to 450-Hz power line, the unit provides a dc voltage in the 120- to 170-V range at 0.2 A for 80% duty cycle, or 0.8 A for 20% duty cycle. **Dranetz Engineering Laboratories Inc,** 2385 S Clinton Ave, South Plainfield, NJ 07080.
Circle 203 on Inquiry Card

TEST SOCKET FOR LEADLESS ICs

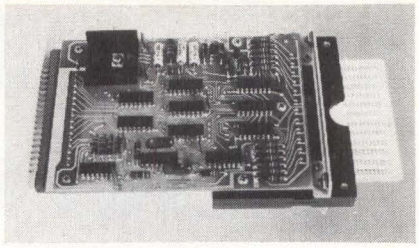


The R-N family of sockets permits testing of single ICs packaged in leadless ceramic substrates without soldering them to a motherboard. Zero force connections between IC contacts and solid pins occur when ICs are in place. Said to be the fastest way to test hermetically sealed ICs at temperatures up to 220°C, sockets are available with from 18 to 64 contacts. Beryllium copper contacts are mounted inside to prevent damage during repeated use. They handle packages ranging from 0.250 x 0.250" (0.635 x 0.635 cm) to 0.700 x 0.700" (1.778 x 1.778 cm) in size. **Robinson-Nugent,** 800 E 8th St, New Albany, IN 47150.
Circle 204 on Inquiry Card

SINGLE-, DUAL-, AND 3-OUTPUT POWER SUPPLIES

Series of g-p supplies offers single outputs for logic circuit application, dual tracking modules to power op amps, and 3-outputs for A-D-A conversion. Specs include input voltage of 105 to 125 Vac, 50 to 400 Hz; storage temp of −55 to 85°C; and input isolation of 100 MΩ in parallel with 100 pF. Units are accuracy adjustable via external pot, overvoltage protected, encapsulated, and plug-in. **SGR Corp,** Neponset Valley Industrial Park, PO Box 391, Canton, MA 02021.
Circle 205 on Inquiry Card

OPTICAL BADGE READER



A credit card/badge reader which meets personnel access-control requirements, model 4H10 is designed to avoid read-out errors caused by motion variables during insertion and withdrawal of badges. Incorporating a single PC board, device reads type IV badges [3.25 x 2.328" (8.26 x 5.91 cm)] containing up to 10 columns by 12 rows of punched holes. As the badge is removed, the holes are scanned optically and the resultant reading is produced digitally (character serial, bit parallel). **Taurus Corp,** Lambertville, NJ 08530.
Circle 206 on Inquiry Card

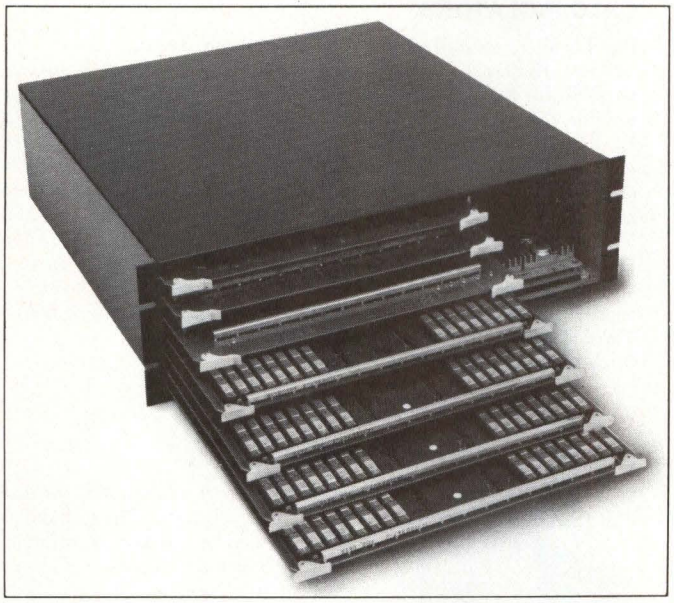
LED/PUSHBUTTON DIP-SIZE SWITCHES

Type 43 combines spst NO pushbutton switches with miniature T-1 size red LEDs in a PC size package, and can be used to clear individual bits and codes or as LED press to test. When used to program microprocessor systems the unit will indicate codes immediately. Available on standard IC terminal centers, the switch can be soldered directly to the PC board or installed in an 18-pin IC socket. Designs are available with four LEDs and five momentary switches. **Licon, Div of Illinois Tool Works, Inc,** 6615 W Irving Park Rd, Chicago, IL 60634.
Circle 207 on Inquiry Card

MULTIPLE OUTPUT SWITCHING POWER SUPPLIES

PM2675, and PM2676, and PM2677 with power levels of 375, 600, and 750 W, respectively, provide regulated output at full-rated load overvoltage ranges of 92 to 138 Vac for the 115-Vac input units, and 184 to 250 Vac for the 208/220-Vac input units. Operation continues for several minutes at inputs as low as 70 to 140 Vac; if input voltage fails entirely, the output voltage holds up for 30 ms min to allow orderly system shutdown. Output voltages range from 2 to 48 V. **Pioneer Magnetics, Inc,** 1745 Berkeley St, Santa Monica, CA 90404.
Circle 208 on Inquiry Card

Now, a memory system that doesn't forget the future.



Semiconductor technology changes as fast as greased lightning sliding down a buttered barber's pole. That's why we built our new NS-3 memory system with one eye on today and one eye on tomorrow.

NS-3 is a completely self-contained memory system built around four 32K x 22 bit memory cards.

It's fast (access times up to 270 nsec), inexpensive, and flexible (we can add more memory card capacity, options such as error correction, parity generation or double word control, and custom interface).

But we've also made room for some future improvements.

Unlike other memory systems, the NS-3 is designed to be compatible with future components technologies as they come along. For instance, we're now building NS-3 using 4K RAMs. But when we introduce 16K RAMs we'll build *them* into NS-3. Systems houses will be able to use the newer, advanced-technology NS-3s with no new interfaces to design, no changeover costs or hassles.

It's the memory system you could live happily ever after with.

CD-4

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Santa Clara, CA 95051

Gentlemen:
Please send me further information on your NS-3 memory system.

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COMPANY_____

ADDRESS_____

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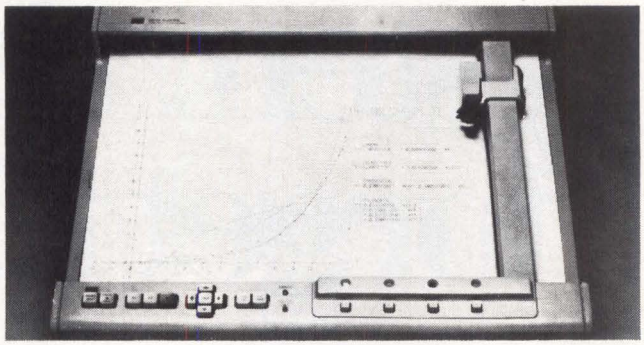
PRODUCTS

4-COLOR X-Y PLOTTER

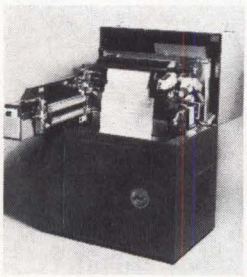


The 9872 microprocessor-based, A3-sized (11 x 17", 27.9 x 43.2 cm) plotter automatically, under program control, selects any of four different colored pens. Designed for use with the 9825 and 9831 desktop computers, the unit's 4-color plotting, seven dashed-line fonts, five built-in character fonts, user-defined characters, and symbol mode plotting combine to produce clear, easy to read plots in applications where curves and plots are difficult to distinguish. 38 instructions built into the microprocessor provide point digitizing, labeling, and character sizing directly through the plotter's HP-1B interface. Stepper motor drive system provides addressable moves as small as 0.0025 mm; resolution is 0.008 mm. Writing speed can be varied from 10 mm/s to 360 mm/s in 10-mm/s increments. **Hewlett-Packard Co,** 1501 Page Mill Rd, Palo Alto, CA 94304.
Circle 209 on Inquiry Card

OPTO-ISOLATORS

Developed to permit direct operation from an ac input, units use two IREDs (infrared emitting diodes) connected in inverse parallel in the input circuit to facilitate an ac input to the isolator. The inverse parallel connection constantly provides an IR light source in accordance with the input of the ac voltage wave. All four units have IREDs in the input circuits. CLI-25 and -26 use phototransistor outputs and provide a guaranteed min current transfer ratio (CTR) of 20 and 40% at 10 mA and 5 and 10% at 1 mA, respectively. CLI-27 and -28 use photo-Darlington outputs and deliver CTRs at 10-mA dc forward current of 400 and 600%, and of 50 and 100% at the 1-mA level, respectively. **Clairex Electronics, a div of Clairex Corp,** 560 S Third Ave, Mount Vernon, NY 10550.
Circle 210 on Inquiry Card

MILITARY-QUALIFIED LINE PRINTERS



Tempest 2200 series, designed for use in any data system which handles either classified or sensitive information, is packaged in rfi-tight enclosures to meet requirements of NACSEM 5100 and MIL-STD-461. The units provide full 136-col printing at speeds of 300 (model 2237), 600 (2267), or 900 (2297) lines/min. Servo-controlled ribbon and paper systems eliminate complicated mechanisms while achieving precise control with minimal maintenance. The hammer mechanism requires a single adjustment, and electronics consist of only five types of PC boards. MTTR is <45 min. Each printer is equipped with a std paper shelf to facilitate forms stacking, and a static eliminator to enhance forms handling under low humidity conditions. **Dataproducts Corp,** DeSoto Ave, Woodland Hills, CA 91364.
Circle 211 on Inquiry Card

epic data:
simple, practical, flexible terminals and network controllers for data collection applications.

The EPIC DATA Model 1647 data collection terminals and 1648 system control units (SCUs) are designed to help the OEM quickly provide systems for such data collection applications as *time and attendance recording, library circulation control, inventory reporting, access control, job costing and maintenance management.* And to allow the OEM to market systems at prices considerably below those of competitors.

simple. EPIC DATA terminals, with RS232C interface (ASCII), are simple to use and deploy. No computer knowledge is required. Maximum use of preformatted data reduces entry errors.

All models include an 8080 microprocessor; the user can program terminals to provide customized input, output and processing of data. In addition, programmability prompts the user through entry steps, validates data and enables off-line operation.

EPIC DATA terminals weigh only 8½ pounds. They can hang on a wall, sit on a desk, and are easily exchanged during maintenance.

practical. EPIC DATA terminals are designed with permanence in mind. Environmental tests conducted in conformity with MIL-STD-810 plus in-depth, on-site testing assure reliable operation over a broad spectrum of hostile, industrial environments. Simple design and rigorous testing have resulted in a demonstrated MTBF of 19,000 hours. MTTR is only 30 minutes.

flexible. Choose the terminal and options which best meet your application. EPIC DATA terminals can optically read punched badges and 80-column ANSI cards. User-defined keys are available for inputting variable data. Key entry data or time of day is displayed and LEDs are available for prompting.

Options. All terminals may optionally scan bar codes and magnetic stripes or accommodate through the RS232 ports other peripherals. Display options include additional numeric displays, up to 15 LEDs for prompting and a 32-character alpha/numeric display. A low-speed modem and serial asynchronous or synchronous communications ports with either RS232 or line driver I/O may be added. Both PROM and RAM memories are expandable.

SCUs. Each Series 1648 SCU polls up to 100 terminals, assembles transactions, formats data, appends time and date, and stores and forwards collected data to the host.

Let Epic Data help you penetrate the data collection market with simple, practical and flexible terminals and SCUs.

OEM quantity (100) prices start at $995. Contact your Epic Data representative today. Or write:

epic data corporation

12728 15th Place, N.E., Bellevue, Washington 98005.
Phone (206) 332-8724. Telex: 04-355701.

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CIRCLE 81 ON INQUIRY CARD

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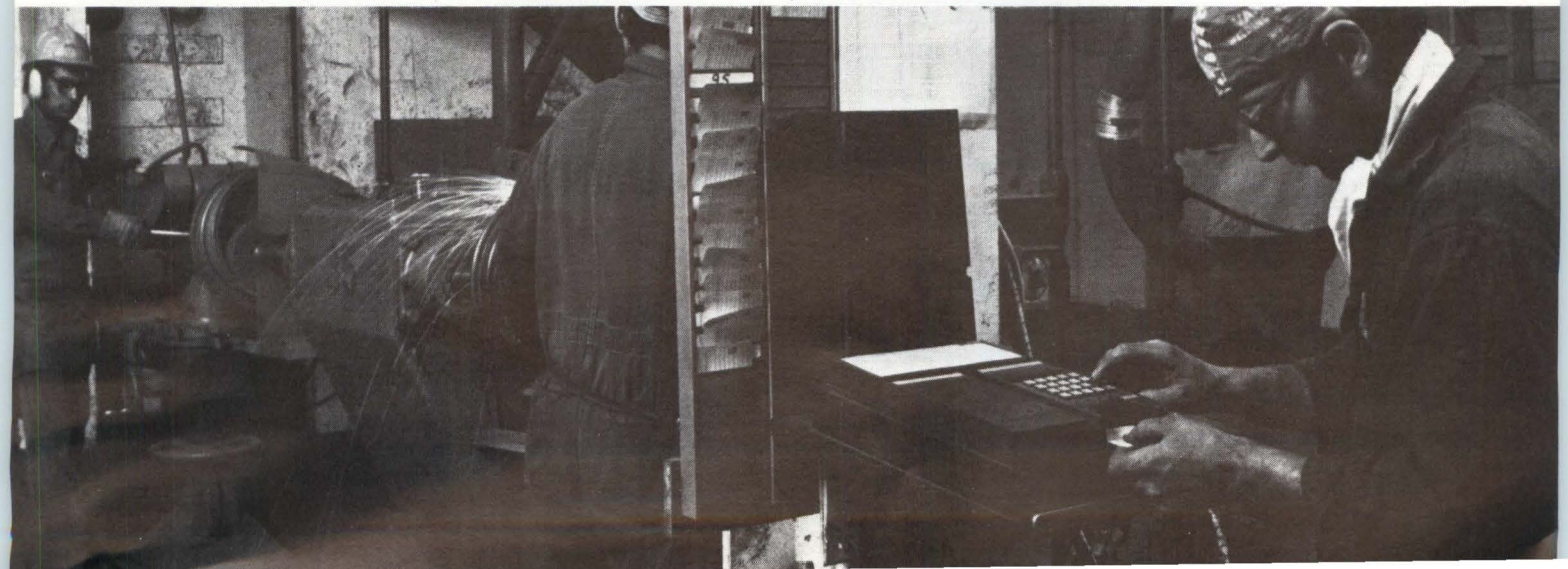
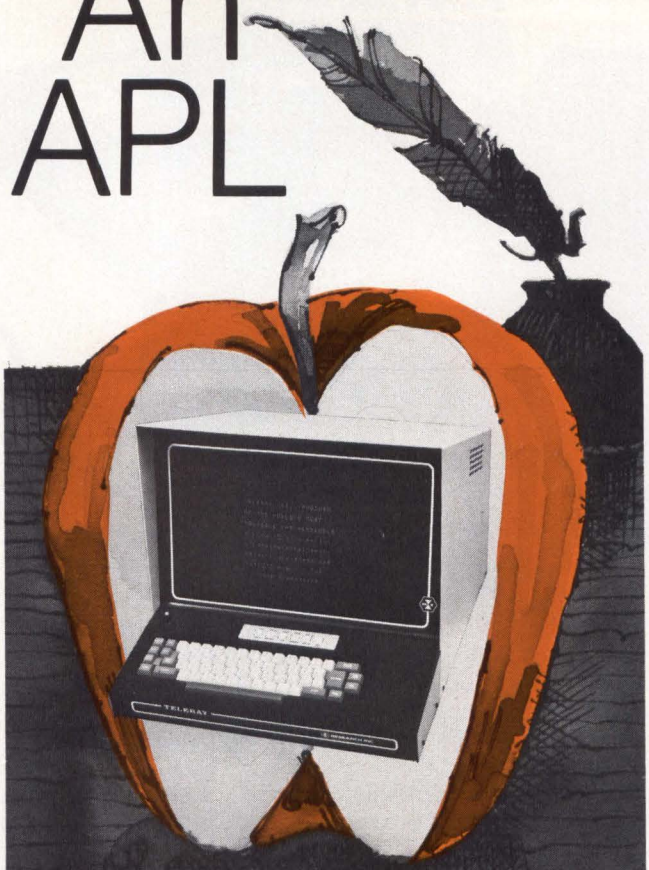


An APL



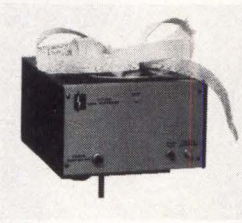
for 300 Teachers!
(and other nice folks)

Over 300 educational institutions and a few hundred other nice folks have good things to say about their TELERAYs. Our APL Model 3931 is really three terminals in one – APL, full ASCII, and upper-case TTY. The 3931 displays TRUE APL over-strike characters, on a big 15-inch high resolution monitor. Like all TELERAYS, it has plug-in assemblies and chips and no fan. And, the usual low TELERAY cost, the free one-year parts-exchange warranty, and easy-to-get field service make the Model 3931 another winner with money-conscious budgeters. Call collect for details! (612) 941-3300.

Teleray Division of
RESEARCH INC
BOX 24064 MINNEAPOLIS, MINNESOTA USA 55424

PRODUCTS

INSTRUMENT-TO-TELETYPEWRITER INTERFACE

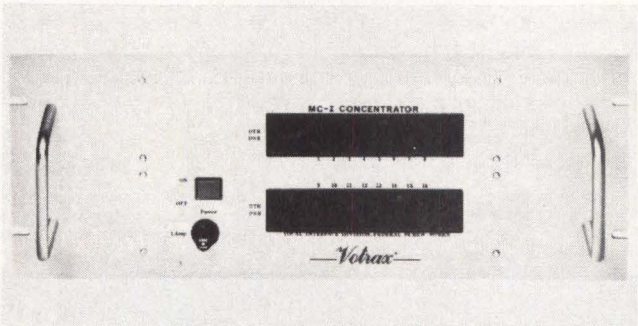


A permanent record of instrument readings can be generated automatically with the CC 1200 code converter, which accepts 10 digits of parallel BCD data from any digital instrument (spectrophotometers, position encoders, A-D converters) and transmits the reading in serial ASCII to teletypewriters, CRT terminals, or other data equipment. Data inputs are TTL/DTL compatible, buffered for up to 80-V logic (either negative or positive-true). When the log command button is pressed (or the remote control activated) the device strobes input data into memory and sends them out in serial ASCII. An isolated 20-mA loop output is std with selectable even or odd parity. After seven loggings, the unit automatically generates a carriage return, line feed, and rub-out. **Nationwide Electronic Systems, Inc,** 1536 Brandy Pkwy, Streamwood, IL 60103.
Circle 212 on Inquiry Card

DATA ACQUISITION MODULE

DT5702 acquires and digitizes signal levels from 10 mV to 10 V, allowing users to connect signals from transducers such as thermocouples, pressure sensors, or strain gauges directly to its input. Compatibility with the DATAX II series allows analog I/O system interface boards for DEC's LSI-11, Intel's SBC-80, Computer Automation's LSI series, and National Semiconductor's PACE series to measure and process 10-mV signals. Functional elements include 16-channel input multiplexer, instrumentation amp, high speed sample/hold amp, 12-bit high speed A-D converter with 3-state outputs for direct connection to microcomputer buses, and all control and programming logic. Instrumentation front end permits signal amplification gains of 1000 at throughput speeds of 3 kHz. Module has 12-bit resolution, $\pm\frac{1}{2}$ LSB linearity. **Data Translation Inc,** 23 Strathmore Rd, Natick, MA 01760.
Circle 213 on Inquiry Card

MICROPROCESSOR COMMUNICATIONS CONCENTRATOR



VOTRAX MC-1 is a compact, solid-state microprocessor-powered peripheral system which provides multiline Touch-Tone™ input handling capabilities for virtually any computer. The system can service up to 32 telephone lines, utilizing an on-board microprocessor to control all functions of the communications data sets and to decode and convert incoming Touch-Tone signals. It supports communications data sets including the Bell 407A, 407B, and several 403-type units, plus Bell Transaction* Telephone, automatic call distributor, and call director. System controller can simulate operation of an asynchronous terminal (RS-232-C) on the host computer's communications adapter. All transactions between controller and host computer are conducted using standard data formats. **Federal Screw Works, Vocal Interface Div,** 500 Stephenson Hwy, Troy, MI 48084.
Circle 214 on Inquiry Card

CIRCLE 82 ON INQUIRY CARD

MEET AT DEEC 77

DESIGN ENGINEERS' ELECTRONIC COMPONENTS SHOW MAY 16...18

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The DEEC Show 77 will be bigger and better than ever. It offers a unique opportunity for OEM Design Engineers to meet with engineers and technicians from leading component manufacturing companies.

It's the only Show created especially for a **one/on/one** discussion between design engineers and component technical people. It's your opportunity to meet the leaders of the component industry and to seek solutions to your specific design and application requirements.

Sponsored by the EIA Parts Division, the DEEC Show is held in conjunction with the Electronic Components Conference – the industry's most comprehensive technical forum on new concepts in active and passive components and electronic materials.

For advance registration information, fill out the coupon below and mail to: Tyler Nourse, Electronic Industries Association, 2001 Eye Street, N.W., Washington, D.C., 20006, (202) 457-4930.

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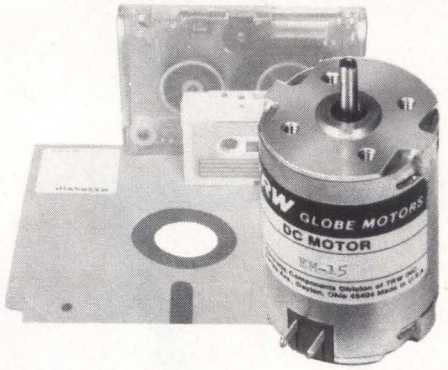
New 1½" servo motor for as little as $8.10



Clip your check, money order, or P.O. number to this ad, and we'll deliver this new **Econo-Mite 15** motor (designed for economy and high production) at our 1,000-lot price.

At 12 v.d.c., torque constant is 2.7 oz. in./amp and no load speed is 5200 rpm. Dimensions 1½" dia. by 2 9/64" max. Specify 6, 12, or 24 v.d.c.

Free technical data. TRW Globe Motors, 2275 Stanley Ave., Dayton OH 45404. See us in EEM.

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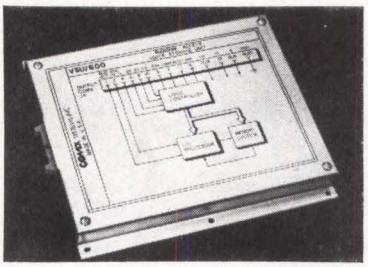
PRODUCTS

RANDOM-ACCESS, SOLID-STATE VOICE RECORD/PLAYBACK SYSTEM

A re-recordable random access voice playback system, using an all solid-state electronic memory system rather than a mechanical transport device, the VSU/600 uses a proprietary voice processing technique and allows individual parts or sectors of memory to be recorded and played back in any order. Each sector is 625 ms in length and can contain a word or phrase in any language. A single module contains 16 sectors (words or phrases), but several modules can be operated in parallel to increase vocabulary size. Packaged in a 7 x 8 x 7/8" (17.8 x 20.3 x 2.2 cm) emi and rfi shielded module, the unit interfaces with existing equipment. Connections are via a 20-pin ribbon type connector. Start, reset, record, and playback functions are controlled by CMOS-compatible logic signals. Individual sectors are addressed by 4-bit binary coding. **Comex Systems, Inc,** Executive Dr, Hudson, NH 03051.



Circle 215 on Inquiry Card

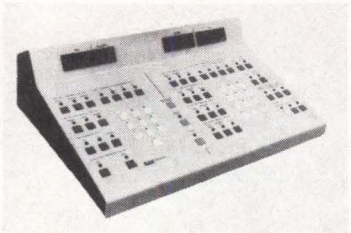
TERMINAL SERIALIZER SYSTEM

ASTRA-10 connects to the DECsystem-10 I/O bus, and supports up to 128 local (EIA or 20 mA) or dial-up terminals, providing an alternative to DEC's DC 76. Designed to use the ASTRA communications adapter, it requires no direct connection to host memory; all hardware and software are host compatible. Fully compatible with industry-standard terminals and modems at speeds from 110 to 9600 baud, the system provides automatic baud detection for 110- and 1200-baud terminals. Received and transmitted data characters are double buffered by the hardware. Each of 128 ports is separately programmable with various formats, and has a single LED indicator which shows ring, carrier, and data activity. Line connections for both EIA and 20-mA terminals are made to industry standard DB25S connectors. **Digital Communications Associates, Inc,** 135 Technology Pk/Atlanta, Norcross, GA 30071.

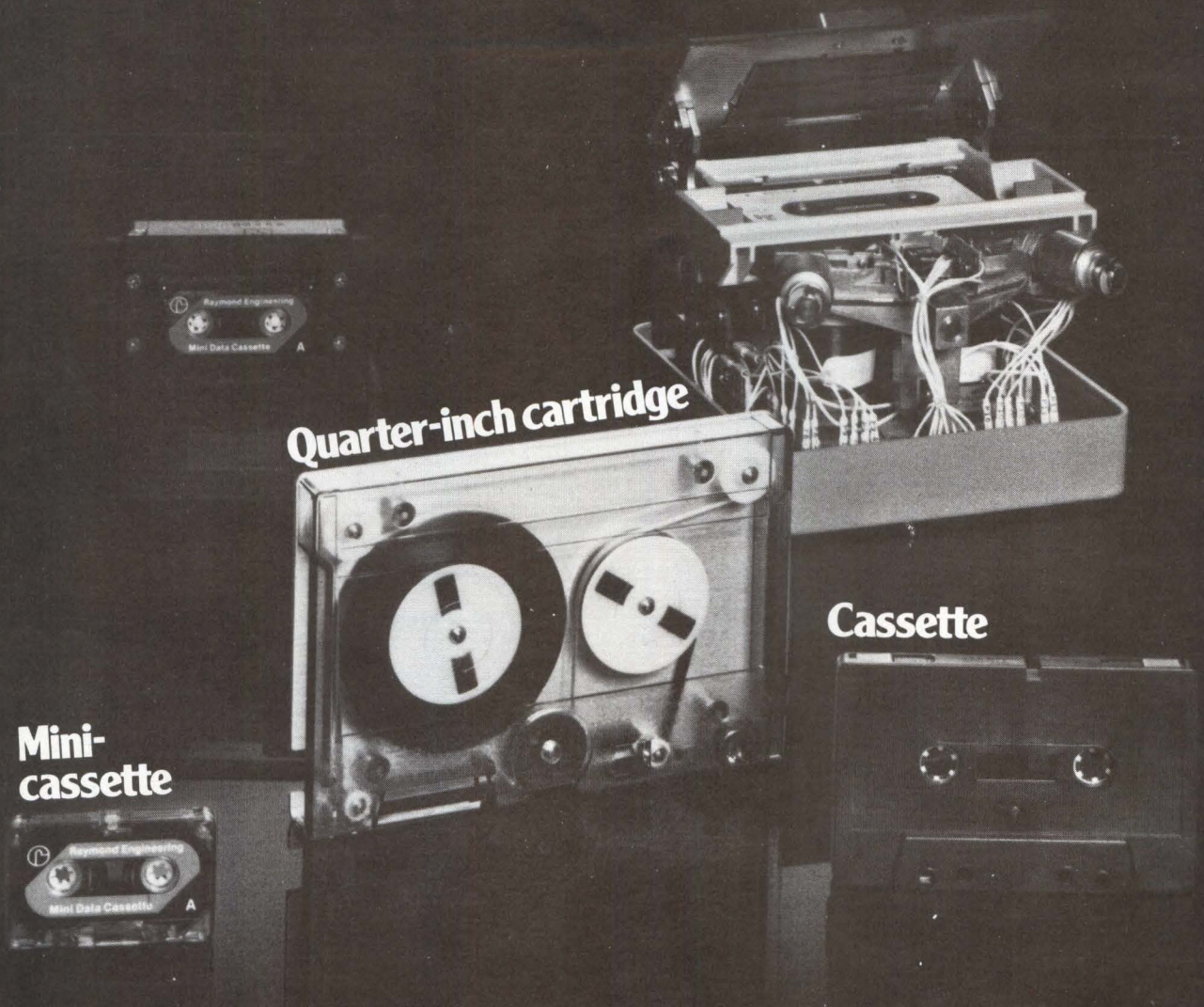
Circle 216 on Inquiry Card

μP BOARD LOGIC TESTER

The 3040 Logictester™ can apply user-defined test sequences at rates up to 1.5M input words/s, more than adequate to match the instruction execution speeds of available microcomputer boards and those not yet announced. Automatic sequences can be run at rates up to 5 MHz. Programmers can intermix both techniques, allowing a reduction in programming time and a higher test confidence. Interface and control capabilities for dynamic LSI logic include the ability to allow the unit-under-test to clock the tester and control the instant of test where appropriate. Sequence programs can be entered directly through a calculator-like program panel. Firmware editor/assembler is fully transparent to the test engineer. Program storage is on floppy discs, and the disc operating system is in firmware. **Fluke Trendar Corp,** 630 Clyde Ave, Mountain View, CA 94043.



Circle 217 on Inquiry Card



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You choose the media that best meets your cost/performance requirements, and Raymond has the Raycorder tape drive to fit. From the Mini Data Cassette storing 1 million bits at 2400 bits per second to the ¼" Data Cartridge storing 20 million bits at 48,000 bits per second, Raycorders will assure you of the consistent, reliable performance you demand.

You know that Raymond builds the world's leading digital cassette recorder, our Model 6406 Raycorder. By now you probably also know that our Model 6409 Mini-Raycorder was the first to use the new Mini Data Cassette. You probably don't know, however, that Raymond is one of the world's leading manufacturers of drives for the ¼" Data Cartridge. Surprised? Let us tell you about our Model 6413 Cartridge Raycorder. It's new to you, but it has a history thousands of units old.

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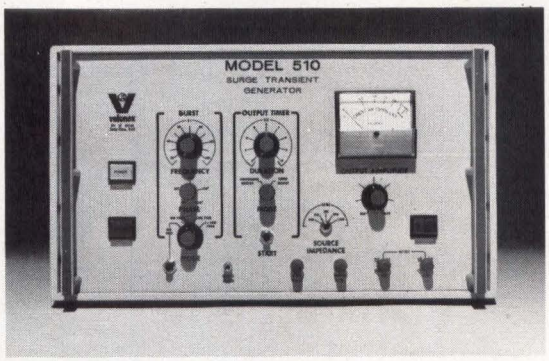

Our model **510 Surge Transient Generator** provides precise standardized repeatable test signals for determining capabilities of various equipment, components and systems for possible malfunction or damage caused by line transient surges. (Meets and exceeds IEEE Std. 472-1974/ANSI C37.90a 1974). Check our reader service card.

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Many possible variations in armature windings permit tailoring of outputs to a wide range of performance requirements.

GM 9413 Gearmotors ensure value and reliability at a moderate price. 123R-3

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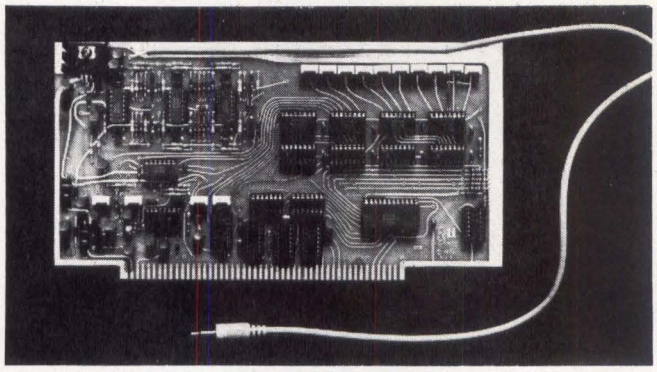
HARLEYSVILLE, PENNSYLVANIA 19438
Phone: (215) 256-6601 TWX: 510-661-8696

PRODUCTS

µP-CONTROLLED CASSETTE BUFFER

MSR 3141, a microprocessor-controlled cassette buffer programmed for ANSI protocol, when used on the company's EDT 33s provides error-detection and correction advantages of the ANSI control procedure (X3.28) for 1200-baud operation on the dial-up network. The device writes, reads, rewinds, and performs limited editing under microprocessor control at the operator's command. The operator issues commands directly from the terminal's keyboard in simple English language. Line disconnects are reported by a message to the buffer's printer, advising the operator of the number of messages and blocks satisfactorily sent and received during each line connection. Equipped with three ports, the buffer can be used in a variety of terminal configurations or transmission networks. It uses tape cassettes with a storage capacity of >50k char. **Western Union Data Services Co,** 70 McKee Dr, Mahwah, NJ 07430.
Circle 218 on Inquiry Card

SPEECH SYNTHESIZER



A hardwired analog of the human vocal tract, the model 1000 uses various portions of the circuit to simulate vocal cords, lungs, and variable-frequency resonant cavity of the mouth, tongue, lips, and teeth. All information necessary to produce speech sounds of American English is programmed into ROMs which reside on the synthesizer board. Unit accepts a string of ASCII characters (each character representing a particular phonetic sound or phoneme) in exactly the same fashion as a printing peripheral. New programming information is required only at the end of each completed phoneme. Max information transfer rate is about 50 bytes/s (25 bytes/s typ). The unit is directly compatible with the Altair/Imsai bus structure. **Ai Cybernetic Systems,** PO Box 4691, University Park, NM 88003.
Circle 219 on Inquiry Card

PRECISION ISOLATION AMPLIFIER

Featuring ±0.025% max nonlinearity, independent of gain, model 277 provides the versatility of a ±15-mA floating power output at ±15 V to permit transducers, front-end buffers, and auxiliary isolated circuits to be powered without the need for separate isolated dc-dc converters. A differential, uncommitted op amp input may be configured as inverting, noninverting, or differential. Both input and output stages can accommodate ±10 V of signal range. A pulse-width modulator/demodulator design within the device provides 160-dB min dc common-mode rejection between input and output stages as well as 120 dB min at 60 Hz. Isolation of ±5 kV pk (pulse) max is coupled with ±2.5-kV pk max continuous input-to-output CMV to facilitate reliable signal acquisition in harsh electrical environments. **Analog Devices, Inc,** PO Box 280, Rt 1 Industrial Pk, Norwood, MA 02062.
Circle 220 on Inquiry Card

CIRCLE 87 ON INQUIRY CARD

HP 9830A/B* USERS.

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By adding INFOTEK's field proven accessories, your 9830A/B will outperform any other general purpose desk top system.

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The cost is a fraction of what you'd pay for any other approach offering similar capabilities.

32,192-Byte Memory

Where more memory is important, the user area may be increased to 32K bytes with our EM-30... the first and only 16,096-word memory for the 9830A/B! Compared to newly introduced models equipped with commonly used ROM options, the 9830A/B with the EM-30 provides 8,192 bytes more user memory. A truly significant increase in capacity!

With the 9830A/B, the EM-30 provides 2,048 more bytes of memory, is priced right, and is fully warranted for a year.

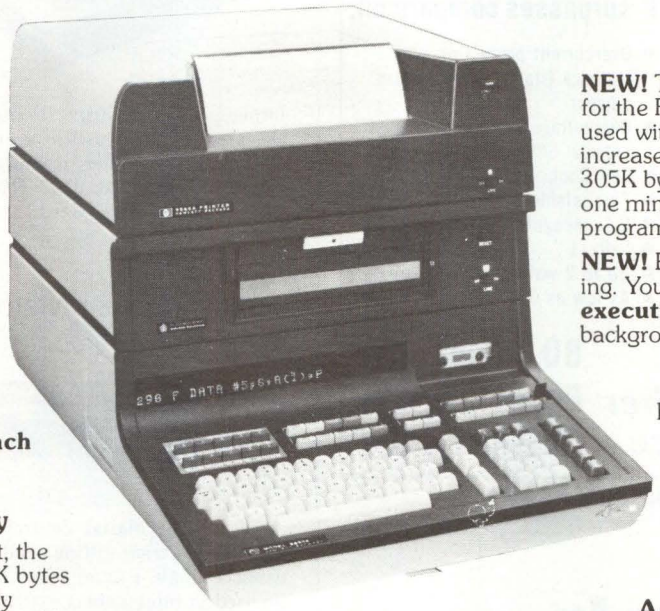
FAST BASIC ROMS

Infotek's FAST BASIC ROMS add to the machine instruction set where HP left off. These ROMS provide spectacular increases in the work throughput of your 9830A/B. For example, you can process arrays at speeds of 40,000 words per second, attain an I/O capability of 10,000 bytes per second, greatly increase the power of a 9880A/B disk system, and print from a buffer while computing.

By providing 46 additional functions, statements, and commands, the FAST BASIC ROMS give your 9830A/B the most powerful BASIC language repertoir short of $200,000 systems.

If you need FAST BASIC but don't have enough unused ROM slots, don't give up! You can install our FAST BASIC ROMS without losing any present capability. **Contact us, we'll show you!**

*A Product of Hewlett-Packard Company



HP 9830A/B with the Infotek FD-30 Mass Memory

Floppy Disk Memory System

The FD-30A provides 305K bytes of on-line data that can be searched 50 times faster than your present cassette system. Data throughput is actually four times faster than the 9880A/B Mass Memory. Best of all, no software modifications are required since the FD-30A obeys all cassette syntax.

The FD-30A is the optimum magnetic memory for the 9830A/B. It has the right capacity, speed, and price.

Prices that you'll appreciate

EM-30 Memory, 16K Words $4,600 / Less trade-in of HP 8K Words 1,100	net $3,500
FAST BASIC I ROM	675
FAST BASIC II ROM	525
FAST BASIC I & II as a set	1,050
FAST BASIC III ROM	525
FD-30A Mass Memory	3,895
FD-30S Slave Drive	1,780
FD-30D Dual Drive System	4,900
RS-30 High Speed RS 232C Interface	750
TC-30 Real Time Clock	825
LP-30 Heavy Duty Line Printer	6,850
CP-30 Character Printer	3,400
PS-30 Paper Tape Punch/Reader	3,850
BP-30 Interrupt Service Printer I/O	525
FI-30 10K Byte/Sec TTL I/O	395

All Prices Are U.S. Domestic

NEW! The FD-30S low cost Slave Drive for the FD-30A. Multiple slaves can be used with a single FD-30A so you can increase on-line capacity in blocks of 305K bytes. Also, the FD-30S provides one minute disk duplication under program control or stand-alone.

NEW! BP-30 automatic buffered printing. Your '30 will **continue program execution** while driving a printer as a background task under interrupt control.

Save $2,100

In our Word Processing Package you get the EM-30, FD-30A, FAST BASIC I and III ROMS, and the CP-30, including software, for a special package price of $10,850.

Other 9830A/B Accessory Equipment

RS-30 High Speed RS 232C Interface. Provides seven crystal controlled Baud rates from 150 to 9600/sec.

TC-30 Real Time Clock. Provides time in 10-millisecond increments, is set or read via the OUTPUT and ENTER statements.

LP-30 Heavy Duty Line Printer. A 200 line-per-minute, 132-column printer (128 character set is standard). Comparable in every way to the 9881A, except the LP-30 is lower in price.

CP-30 Correspondence-Quality Character Printer. Provides 14 easily changeable fonts including scientific symbols, UK, German, Scandia, and Cyrillic. Prints and plots at 45 cps.

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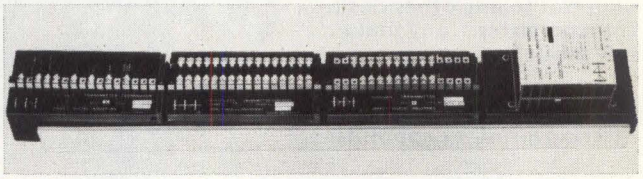
PRODUCTS

PORTABLE UNIVERSAL PROGRAMMER

A versatile, software-based p/ROM programmer in a compact lightweight package, model 9 has insert/delete data editing capabilities and is capable of programming, loading, and verifying 200 different p/ROM configurations. It can program entire generic p/ROM families using a single personality module. Hexadecimal keyboard and display and microprocessor-controlled operations result in simple operation. Software-based serial and parallel I/O interfaces allow for data communication in key-selectable data translation formats. Data polarity controls are provided, and built-in error checking routines assure accuracy of all data transfers. Integral 1k-byte RAM buffer memory expands to 4k bytes. **Data I/O Corp,** PO Box 308, 1297 NW Mall, Issaquah, WA 98027.

Circle 221 on Inquiry Card

MODULAR TIME-DIVISION MULTIPLEX SYSTEM

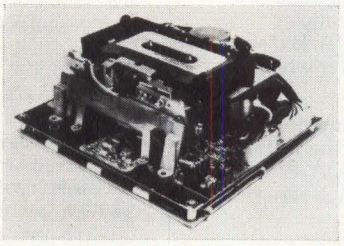


A multipoint digital control cable that provides an economical method of transmitting and receiving many points of control using a single pair of wires, the completely solid-state device can be used to interconnect systems separated by many miles. Circuitry is designed with an active memory built-in. If interconnecting wires should be cut, shorted, or stray voltages exceed the signal voltages, the receiver remembers the last valid signal. Essentially a terminal strip containing encapsulated solid-state circuitry, the device consists of four basic modular units: 8-point transmitter, 8-point receiver, 16-point transmitter, and 16-point receiver. System capacity is increased by plugging in additional modules and connecting the I/O devices. **Digicable, Inc,** 2151 Scranton Rd, Cleveland, OH 44113.

Circle 222 on Inquiry Card

DIGITAL CASSETTE RECORDER

STR^R-150 solves problems of interfacing to a microprocessor system, microcomputer, or minicomputer while providing high data reliability, by supplying complete interface electronics. Interfacing requires only supplying eight data-in lines with strobe, eight data-out lines with strobe, and a separate line for rewind. All lines are DTL/TTL compatible. To assure data reliability, the unit uses speed tolerant recording, a self-clocking technique which virtually eliminates effects of flutter, wow, and head misalignment and results in error rates of <1 in 10^7 (soft) and <1 in 10^8 (hard). Asynchronous 8-bit parallel inputs are accepted at rates to 125 char/s; data are output at the same rate. Up to 150k char can be stored on each side of a 450-ft (137-m) digital cassette tape. **Electronic Processors, Inc,** 1265 W Dartmouth Ave, Englewood, CO 80110.



Circle 223 on Inquiry Card

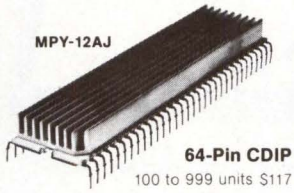
the Fastest Biggest Bipolar Multipliers you can buy

130 ns

40-Pin CDIP
100 to 999 units $70

8 by 8 Bits – Ideal for on-line multiply in micro and mini computers – operates directly on most data bus lines – consumes only 1.8 watts (typical)
Price $100 each in 1-9 quantities.

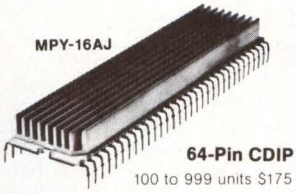
150 ns



64-Pin CDIP
100 to 999 units $117

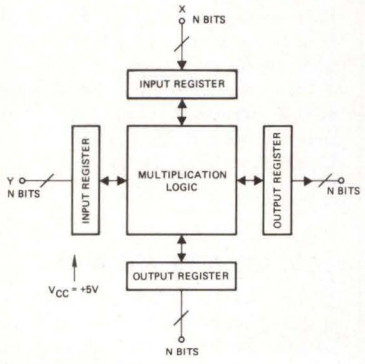
12 by 12 Bits – New size multiplier for data communications and Signal Processing – needs only 3-1/2 watts for room temperature operation – single TTL Clock – fully TTL compatible – Price $168 each in 1-9 quantities.

160 ns



64-Pin CDIP
100 to 999 units $175

16 by 16 Bits – Smaller chip improves performance – 64-pin DIP easy to use – dissipates 5 watts with built-in heat sink – perfect for micro/mini applications – signal processing – price $300 each in 1-9 quantities.



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- Two's Complement Multipliers
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- Single Chip Bipolar Design
- Asychronous Multiply
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- TTL Compatible Input/Output +5V

Operating Sequence Mini/Micro Computer Data Bus Operation

- Load Input Registers
- Wait Multiply Time
- Load Output Registers
- Read-Out

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Alternate Timebase Display

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●Forget MIXED-SWEEP limitations

The PM 3214 is the latest addition to the Philips oscilloscope family.
At 25 MHz and 2mV sensitivity, the PM 3214 incorporates all the triggering facilities found on the latest, most expensive oscilloscopes available: AC, DC, TV and an auto position that derives its trigger from the peak to peak signal input. Trigger selection from either channel, line and external sources as well as composite triggering for ASYNCHRONOUS signals.
Composite triggering in A-B display derives its source from the differential signal, allowing measurement of signals riding on high AC or DC components.
The 18.5 lb. portable is double insulated and even has an internal battery option. Supplied with two probes and a protective front cover, the PM 3214 is a money saving solution to many oscilloscope requirements.
If you don't need DELAYED TIMEBASE the economy priced PM 3212 has all the triggering and overall perfomance of the PM 3214 at only $ 1,155.00 *.

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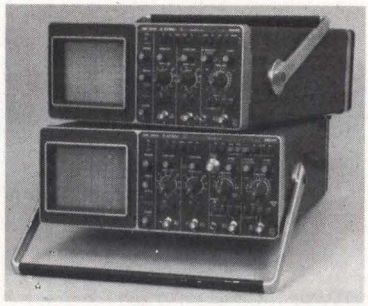
* U.S. Domestic Price Only

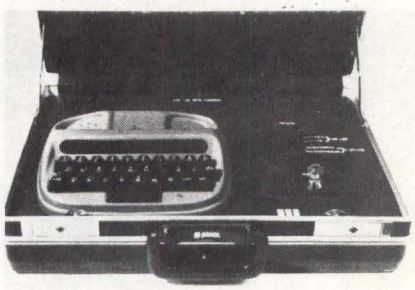


PHILIPS

PHILIPS

PRODUCTS

PORTABLE MESSAGE ENCRYPTION TERMINAL



DPD-100 encyphers messages for transmission by letter, TELEX, or to another -100 over the telephone lines, using a self-contained modem and acoustic coupler. The unit includes an alphanumeric keyboard and 32-position display, ac/battery power supply, and DPD-72A cryptographic system. More than 68 billion nonlinear codes are selectable by thumbwheel switches under a locked cover. On or offline operation is selected by a switch. The unit is packaged in a carrying case that measures 12 x 18 x 5" (30.5 x 45.7 x 12.7 cm) and weighs approx 10 lb (4.5 kg). **Technical Communications Corp,** 56 Winthrop St, PO Box 1070, Concord, MA 01742.
Circle 224 on Inquiry Card

BIDIRECTIONAL CODED SWITCHES

Mico series miniature switches mount in a 1.2" (3.05 cm) high opening, allowing a relatively large character size [0.315" (0.80 cm)] for better viewing distance. Available as decimal or coded 8421 BCD and BCD with complement, switches have heavy gold-plated contacts. Terminals are card-edge tabs for use with sockets but have holes for soldering. Extended PC tab board versions are available for component mounting. Features include snap-together assembly and mounting. **Alco Electronic Products, Inc,** 1551 Osgood St, North Andover, MA 01845.
Circle 225 on Inquiry Card

LOW COST KEYBOARD

Heart of the reliable keyboard and individual switches is a membrane molded of nonconductive silicon rubber, incorporating cup-shaped compartments with an integral disc fabricated of conductive silicon rubber. Keyboard is placed on top of a mating PC board. Pressure on the closed portion of the cup completes a circuit. Removing pressure returns it to the NO state. Positive snap action in both directions is insured. Keyboard is custom molded to specific numbers of keys and layout. **Current Industries, Inc,** 3359 Ocean Ave, Oceanside, NY 11572.
Circle 226 on Inquiry Card

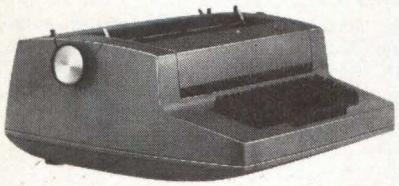
For immediate need, Circle 91 on Inquiry Card
For information only, Circle 92 on Inquiry Card

DISC STORAGE DRIVES

Storage options for S100 and S200 computers are the model 5540, a 150M-byte storage module and controller, and the 5550, a 300M-byte storage module and controller. Additional storage module drives may be added to each of the two basic models to increase storage capacities. Std features include a data transfer rate of 1.2M bytes/s; avg latency of 8.3 ms; avg access of 30 ms; and alternate error sector flag addressing. **Harris Corp, Computer Systems Div,** 1200 Gateway Dr, Fort Lauderdale, FL 33309.

Circle 227 on Inquiry Card

I/O TYPEWRITER

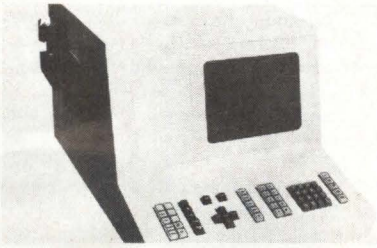


Heavy duty Rotary II can serve as an IBM 735 replacement. It has a single element printing system and prints at 15 char/s. Its electronic keyboard has true N-key rollover; a 3-char buffer assures data integrity, even when burst typing speeds are used. In addition to the std alphanumeric keyboard, four extra keys can be customized to perform specific functions or generate specific control signals to the output plug. Interface is readily modified to meet most specific needs, and is available with ASCII character set as well as RS-232 emulation. **CPT Corp,** 1001 S 2nd St, Hopkins, MN 55343.

Circle 228 on Inquiry Card

POSITIONING SYSTEM CONTROLLER

Anomatic™ automatic controllers use a microprocessor for positioning up to four axes for combinations of linear or circular motion. A 12-V CMOS bus interconnects the microprocessor to all I/O devices; all logic and controls are CMOS, and the microprocessor, p/ROM, and ROM are TTL. Noise immunity is 4.8 V throughout. System can be programmed from internal memory, paper tape, cassettes, or magnetic cards; it contains a built-in p/ROM programmer to provide nonvolatile memory. Unit has full editing capabilities for stored programs. **Anorad Corp,** 115 Plant Ave, Smithtown, NY 11787.



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DIGITAL COMPARATOR AND RATIO METER

Digital comparator compares parallel 3½-digit BCD input data to a setting preselected by thumbwheel switches. Comparison outputs include a change in logic level and a relay contact closure. Digital ratio meter computes the ratio of two 3-digit parallel BCD inputs. Three ranges—199:1, 19.9:1, and 1.99:1—are switch selectable and are displayed by a 2½-digit LED readout. Parallel 8421 BCD output is available. Both instruments operate on 115 Vac and are panel mounted. **Servo-Tek Products Co,** 1086 Goffle Rd, Hawthorne, NJ 07506.

Circle 230 on Inquiry Card

CARTRIDGE RECORDER/ 21MX INTERFACE

The 3011 interface occupies one card slot in the H-P 21MX computer and connects to the company's 3000 digital cartridge recorder over a 40-wire flat cable. Interface uses two select codes: the lower is the command channel and the higher is the data channel. Unit services one formatter, which can then service up to four 3000 drives. Operation is in either programmed-channel or DMA mode. Data transfer between the computer and interface is 16- or 8-bit parallel. **Tandberg Data, Inc,** 4901 Morena Blvd, Suite 407, San Diego, CA 92117.

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While they have some good reasons for calling theirs dumb, we've got good reasons for calling ours smart.

For instance, the IQ 120 gives you absolute cursor control. It also provides block mode so you can transmit a line or a page at a time.

Of the two, only IQ 120 has field protection to prevent inadvertent overtyping of designated information. What's more, the IQ 120 comes with 73 keys instead of 59, including a numeric pad.

Other than that, they're pretty evenly matched. Check our price and then see why the smart money is on IQ 120.

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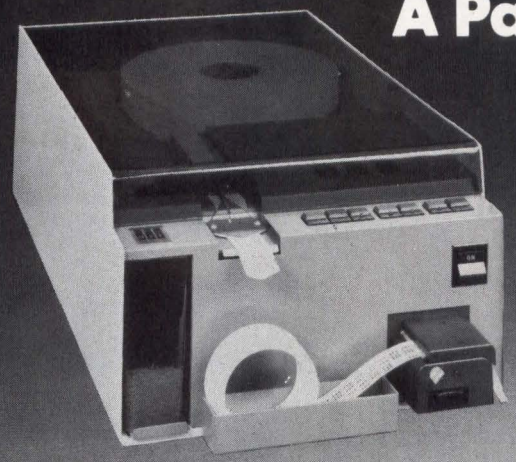
SOROC TECHNOLOGY, INC.

CIRCLE 94 ON INQUIRY CARD



A Paper Tape Combo for your Terminal

DATA SPECIALTIES' SRP-300 connects, without modification, to any 300 baud teleprinter or CRT terminal thru the RS-232 connector and provides all the features of a conventional ASR. In addition, the Combo may be used as a stand-alone computer peripheral. This whisper quiet (58 dB) unit is provided with full/half duplex, line/local, search/edit control, backspace, tape feed, remote control selection and switch selectable baud rates as standard features.

The Combo employs a photo electric/LED reader and the revolutionary MODUPERF™ tape punch mechanism. The unit will reliably read and punch without readjustment or modification paper, MYLAR, rolled or folded tapes.

DSI, 3455 Commercial, Northbrook, IL, 60062-Tel: (312) 564-1800

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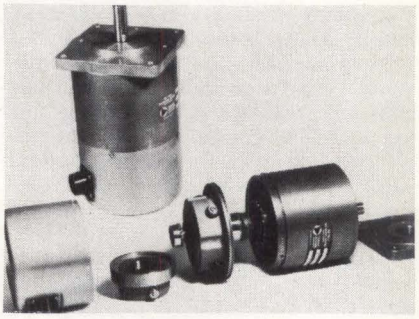
PRODUCTS

SINGLE BOARD INTERFACE CONTROLLER

Slot Saver™, a multicontroller interface board for Data General Nova™ and Eclipse™ computers, measures 15″ (38.1 cm) sq, and contains interface controllers for low speed peripheral devices commonly used with minicomputers. Max configuration consists of controllers for CRTs or TTYs, real-time clock, paper tape punch, and line printer. It requires one CPU slot. The device is fully compatible with instruction sets and operating systems software supplied by Data General for specific peripheral devices. **Custom Systems Inc,** 2415 Annapolis Lane, Minneapolis, MN 55441.

Circle 232 on Inquiry Card

SERVOMOTOR



5100 series 5″ (12.7 cm) dc permanent magnet servomotors and tachometers provide up to one-third better torque performance as a result of improved magnet design. The 5160 ¾-hp model can achieve up to 740 continuous torque (2400 oz-in, 16.8 N•m). Units range from ¼ to ¾ hp and can be used with the company's low tach ripple tachometer and/or an optical encoder. Both English and metric versions are available. **Torque Systems, Inc,** PO Box 588, 225 Crescent St, Waltham, MA 02154.

Circle 233 on Inquiry Card

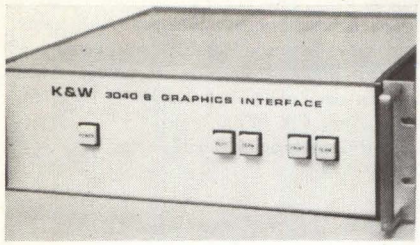
MINIATURE DC-DC CONVERTER

Measuring 0.33 cu in (5.4 cc) and weighing <0.2 oz (5.6 g), dc 500 series converters are available in four models: 12, −12, 15, and −15 V out. All four have 0.5% typ regulation for 3- to 7-V inputs, 300-mW drive capability, and 60 to 70% typ efficiency. Line can be used from 3- or 6-V battery power and features output regulation of 12 V ±0.6 Vdc, and 15 V ±0.7 Vdc. Full temp range is 0 to 50°C, derated to 70°C. **Elexon Power Systems, div of Elpac Electronics, Inc,** 3131 S Standard Ave, Santa Ana, CA 92705.

Circle 234 on Inquiry Card

CIRCLE 95 ON INQUIRY CARD

GRAPHIC INTERFACE FOR PROGRAMMABLE CALCULATORS



Using bistable storage CRT display units from Tektronix, 3040 series is hardware and software compatible with 9800 series calculators from Hewlett-Packard, and provides high speed simulation of HP-9862 plotter and -9866 printer. Designed to provide increased speed, versatility, and convenience to calculator users in plotting data output, program listing, and program generation, systems offer interactive capabilities that allow plots, graphs, or charts to be created, analyzed, or modified easily. **K & W Electronics, Ltd,** Vienna, VA 22180.

Circle 235 on Inquiry Card

FAST-SWITCHING INFRARED LEDS

High-output infrared LEDs, SE301A and SE302A, provide high radiated power (3 mW min) in a spectrally narrow band peaking at 9400 Å. Waveform is closely matched to silicon sensors. Small GaAs devices are mounted on TO-18 hermetically sealed headers with glass lens (-301), or on lead frame and mold with clear plastic lens (-302). Rugged LEDs are useful in optical switch sources, optical choppers, and sense-source applications. **NEC America, Inc, Electron Devices Div,** 3070 Lawrence Expwy, Santa Clara, CA 95051.

Circle 236 on Inquiry Card

FIXED-HEAD DISC MEMORIES

Model 980 head-per-track units for use with most minicomputers are available in storage capacities ranging from 0.5M to 2.0M bytes, with larger capacities achievable by daisy-chaining. All units use Disc Cell™, an interchangeable disc cartridge with self-contained spindle, Winchester-type media, and R/W head assemblies. Cartridge is packaged and sealed for reliable operation in severe environments. Other features are integral dc power supply, flexible I/O, constant data rate and access time regardless of power source (115 V/60 Hz or 230 V/50 Hz), and 10 kh MTBF. **Dataflux Corp,** 1195 E Arques Ave, Sunnyvale, CA 94086.

Circle 237 on Inquiry Card

PDP-11 PLUG-COMPATIBLE PRINTER

Through the use of a company controller, the family of printers can interface with DEC's PDP-11, Data General's Nova and Eclipse, Interdata, and Hewlett-Packard minicomputers. Speeds are 300, 425, 600, and 1000 lines/min with std 64-char set; 96-char sets are available. Using chain-train technology, printers are fully buffered to enable the CPU to perform other processing tasks between printer line settings. Device operates under standard systems software. **Business Systems Technology, Inc,** 3015 Daimler St, Santa Ana, CA 95705.

Circle 238 on Inquiry Card

CURRENT SENSOR

Adjustable relay response time allowing preset levels of known system inrush current, transient voltage immunity of up to 2500 V peak (short duration), and full rated output at operating temperatures of 0 to 55°C without forced air or heat-sinking are features of CSI-220 series ac current sensors. Accepting 0.1- to 100-A signals from the company's ac current transformers, they provide precision current sensing protection and/or process control. Input voltage is 90 to 125 Vac, 50 to 60 Hz. **Guardian Electric Manufacturing Co of Calif,** 4030 W Spencer St, Torrance, CA 90503.

Circle 239 on Inquiry Card

Without our software, we're just another flasher.

Let's face it. No microcomputer is worth a dime if you can't make it work. Even E&L's Mini-Microdesigner would be just a "light flasher" if it weren't for our software system.

But the fact is that our tutorial software is the best in the business. Not just a pathetic rehash of chip manufacturers' specifications. But a clearly written, step-by-step instruction that teaches you all about the microcomputer. How to program it, how to interface it, how to expand it.

The teaching material is written by Rony/Larsen/Titus (authors of the famous Bugbooks). It's called Bugbook V. And it teaches through experiments designed specifically to get you up to speed on our Mini-Microcomputer (MMD-1). *And you don't need any prior knowledge of digital electronics!*

The best news? E&L's MMD-1 costs $422.50* in kit form, including all software and teaching material. OEM and educational discounts available.

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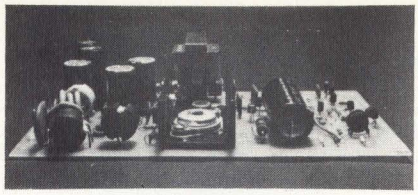
PRODUCTS

48-VDC TAPE TRANSPORT

A mag tape transport system which operates from 48-Vdc telephone system power sources, Mod 10/48 includes a tape transport, R/W head, R/W and control electronics, and a 48-Vdc power supply which is a dc-dc conversion system. Line filter protects power bus from tape unit generated noise. Based on the company's Mod 10 digital tape drive, the system has a 9-track read-after-write head and records 800 char/in NRZ and PE (IBM-ANSI compatible) at speeds of 12.5 or 25 in/s (31.75 or 63.5 cm/s). System functions by direct reel drive. **Wangco, Inc,** 5404 Jandy Pl, Los Angeles, CA 90066.
Circle 240 on Inquiry Card

MICROCOMPUTER POWER SUPPLY

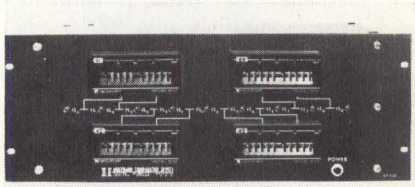


A 4-output switching power supply features outputs of 5 V at 6 A, ±12 V at 1 A, and −5 V at 1 A, with a maximum power of 50 W total. Input voltages are 90 to 130 V. Line regulation is 0.2%; load regulation is 0.5% for the 5-V output, and 5% for the other three outputs. Std features include overvoltage, overcurrent, and short-circuit protection. Switcher weighs 14 oz (392 g), and measures 7.85 x 4.6 x 2.25" (19.94 x 11.68 x 5.72 cm). **Boschert Associates,** 384 Santa Trinita, Sunnyvale, CA 94086.
Circle 241 on Inquiry Card

COMPUTER/COMMUNICATION INTERFACE BOARD

Combining four boards into one, the QuadrAsync™ interface gives PDP-11 users four asynchronous EIA series communications channels while presenting only one load to the Unibus®. Board, which is completely software compatible with DEC DL11B and DL11D boards, consists of one quad board and four DEC-compatible male Berg connectors. Operation is full duplex with both transmitter and receiver for each channel operating at the same baud rate; seven selectable baud rates per channel range from 150 to 9600. **Able Computer Technology,** 1616 S Lyon St, Santa Ana, CA 92705.
Circle 242 on Inquiry Card

MULTIBAND COMPARATOR



A universal multiband comparator with 9-band sorting is able to interface with any instrument having either 3½- or 4½-digit BCD output. SP3971 features a front panel indicator and open-collector logic level output for each of nine contiguous bands. Relay and solenoid outputs are also available. Option permits use with analog output instruments. Several limits can be set asymmetrically about the nominal. Designed with TTL logic, unit operates at 120 Vac. **Electro Scientific Industries, Inc,** 13900 NW Science Park Dr, Portland, OR 97229.
Circle 243 on Inquiry Card

MDB SYSTEMS presents... The LSI-11 Connection

GP Logic Modules · Peripheral Controllers · Communications Interfaces · Special Purpose Modules · Accessory Hardware
Plus: DEC's own LSI-11 Microprocessor Module.

Here are some MDB Systems connections to LSI-11 microprocessors:

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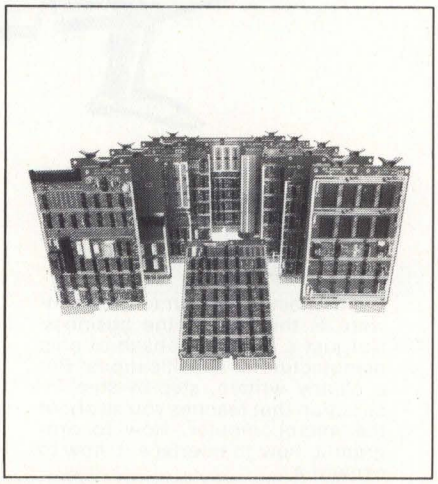
☐ Device Controllers for most major manufacturer's
Printers
Card equipment
Paper tape equipment
Plotters
☐ Communications/Terminal Modules
Asynchronous Serial Line
Synchronous Serial Line



☐ MDB Backplane/Card Guide Assembly (8 Quad slots)
Rack mount chassis 5¼" front panel.
☐ Special Purpose Modules and Accessories
System monitoring unit provides front panel switch addressing, power on/off sequencing; line frequency clock.
☐ Bus extenders/terminators.
E-PROM and PROM modules.
Bus connectors for backplane assemblies.

MDB Systems products always equal and usually exceed the host manufacturer's specifications and performance for a similar interface. MDB interfaces are software and diagnostic transparent to the host computer. MDB products are competitively priced; delivery is usually within 14 days ARO or sooner.

MDB also supplies interface modules for DEC PDP*-11 Data General NOVA* and Interdata minicomputers.

MDB
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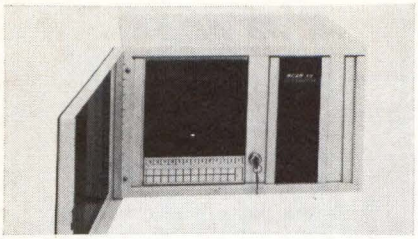
*TMs Digital Equipment Corp. & Data General Corp.

CIRCLE NO. 113 FOR LSI-11; 114 FOR PDP-11; 115 FOR NOVA; 116 FOR INTERDATA

VOICE RESPONSE SYSTEM



Providing multiline voice response output at low cost, the microcomputer-controlled 310 provides a simple interface to Touch-Tone® telephones, encoding incoming Touch-Tone signals to ASCII data characters for serial transmission to the host computer port. System's natural sounding synthetic voice is based on an analysis of real speech. Outputs are highly compressed digital codes which operate in conjunction with a 40 series communications processor. Communication with the system is by asynchronous and synchronous protocols. **Micom Systems, Inc,** 9551 Irondale Ave, Chatsworth, CA 91311.

Circle 244 on Inquiry Card

MINIATURE DRY REED RELAY

Available in monostable neutral and bistable polar versions with 1- or 2-make contacts, small size and standard 2.54-mm lead spacing of the relays makes them suitable for direct mounting on PC boards. Neutral, 1-contact relay has an operate time of <2 ms for an operate power of 100 mW; operate bounce time is 0.6 ms max and release bounce time is 0.1 ms max. Coupling capacitances between contact members of the open contact range from 1.7 to 4 pF. **Siemens AG,** Postfach 3240, D-8520 Erlangen 2, Federal Republic of Germany.

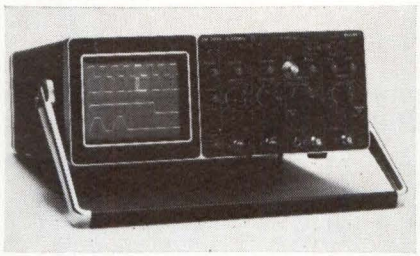
Circle 245 on Inquiry Card

20- AND 24-PIN SOCKETS

The 20-pin [on 0.300" (0.762 cm) centers] and 24-pin [on 0.400" (1.016 cm) centers] sockets have been added to the 500 series. The 20-pin socket is intended for microprocessors, interface circuits, and 4k RAM uses; the 24-pin socket is for use with Fairchild's TTL Macrologic™ devices. Both are available in wire-wrap or PC terminations, with gold-plated machined contacts, and gold- or tin-plated machined sleeves. **Augat Interconnection Products Div, Augat, Inc,** 33 Perry Ave, PO Box 779, Attleboro, MA 02703.

Circle 246 on Inquiry Card

DELAYED TIMEBASE OSCILLOSCOPE



A 25-MHz dual timebase portable oscilloscope, the PM 3214 features alternate timebase display, allowing full screen display of both main and delayed timebases for both channels simultaneously, resulting in four traces. Main timebase triggering modes are auto, ac, dc, TV line, or frame and source selection from Channel A or B, composite, external, and from the line. Delayed mode is also ac or dc coupled with full level control and source selection with calibrated delay, Channel A, B, composite, and external source. **Philips Test & Measuring Instruments, Inc,** 85 McKee Dr, Mahwah, NJ 07430.

Circle 247 on Inquiry Card

FLOPPY DISC TESTER

Measuring both starting and running torque of diskette cartridges within their protective envelopes, the model 200 is a readout and control instrument containing a floppy disc drive assembly which is used to make the required measurement. Torque is measured with the company's optical brushless torque transducer; running torque is displayed on a 4½-digit panel meter. 0- to 10-Vdc analog output for torque is provided for use in recorders and oscilloscopes. Displays present data either in ounce-inches or Newton-centimeters. **Vibrac Corp,** 11 Alpha Rd, Chelmsford, MA 01824.

Circle 248 on Inquiry Card

ILLUMINATED PUSHBUTTON SWITCHES

Series 88X and 86X "shorty" pushbutton switches, UL listed for power ratings of 6 A at 125 Vac or 3 A at 250 Vac, are also available with hard gold contacts for low level switching. Switching configurations are spst or dpst NO, momentary or alternate push on/off with positive latch down. Mountings are snap-in panel in 0.625 or 0.755" (1.58 or 1.92 cm) square cutout held by stainless steel retaining clips, or perpendicular to the PC board. **Compu-Lite Corp,** 711-F12 W 17th St, Costa Mesa, CA 92627.

Circle 249 on Inquiry Card

PDP-11, NOVA & ECLIPSE DISK STORAGE SYSTEMS USERS...

Phoenix Systems Offer Hardware, Software and Media Compatibility Plus...

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• FIELD PROVEN RELIABILITY • LOW COST • 30-DAY DELIVERY ARO

The Phoenix 45, for PDP-11 Users; and the Phoenix 35 and 40, for Nova and Eclipse Users; are microprocessor-based, embedded disk controllers featuring as standards:

● Write protect to the sector level ● Unique built-in self test
● 100% position verification ● Overlapped seek

Phoenix 45 is ☐ DEC RK11/RK05 compatible and ☐ Expandable up to 20 Mbytes in 2.5, 5 or 10 Mbyte increments.

Phoenix 35 and 40 are ☐ DG 4046 and 4234 compatible, and ☐ Expandable up to 40 Mbytes in 2.5, 5 or 10 Mbyte increments.

Phoenix 211 Mass Storage Controller for PDP-11 Users provides up to 1.2 ***billion*** characters: 40, 80, 200 or 300 Mbyte increments;
☐ software enables controller to be used as storage or system device for DOS/BATCH, RT11, RSX11M, RSX11D and IAS Operating Systems, and
☐ occupies one system unit (supplied) and one hex SPC I/O slot in computer or expansion box.

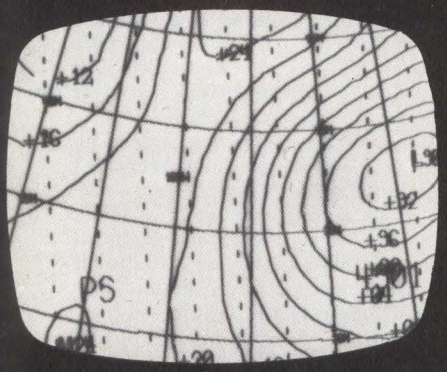
Phoenix 311 Mass Storage Controller for Nova and Eclipse Users provides up to 1.2 ***billion*** characters: 40, 80, 100 or 300 Mbyte increments;
☐ is compatible with 4231 Disk Subsystems when used with 100 or 200 Mbyte drives, and
☐ occupies one standard I/O slot in DG or equivalent computers.

For more complete details on Xylogics Phoenix Systems, telephone or TWX us TODAY!

Nova and Eclipse are trademarks of Data General Corp.

CIRCLE 98 ON INQUIRY CARD

From Genisco leaders in the resolution revolution...



1024 X 1024 digital raster displays for under $17K!

Genisco's GCT-1024 — the first high performance ultra-high resolution digital graphics display system available on a production-run basis — now takes the "stair step" appearance out of raster displays, to minimize distortion and give much greater density detail. What's more, it's the first system of such magnitude priced at less than $17,000* including a 21" monitor.

High Speed Graphics Manipulation A proprietary programmable microprocessor provides 51 mnemonic instructions — specifically designed for graphics manipulation — at 150ns cycle times. MOS/RAM refresh memories.

Field Proven Versatility Proven performance worthiness in a number of stringent-usage functions like: command and control process simulation, automatic data reduction, mapping, war gaming, crystallography, etc. And it is compatible with standard high-resolution monitors.

Expandable User-oriented options and accessories lets you go "on-line" at minimal cost and upgrade as needed. Included are: grey-scale video look-up tables, graphic tablets, keyboards, cursors and joysticks. You can even opt for systems with up to 16 grey scales.

So, when you want high resolution graphic displays at economically feasible costs, contact Genisco Computers, 17805-D Sky Park Circle Drive, Irvine, CA 92714, (714) 556-4916 . . . and ask for all the particulars.

*Price in volume production quantities

GENISCO COMPUTERS

A division of Genisco Technology Corp.

CIRCLE 99 ON INQUIRY CARD

PRODUCTS

HERMETICALLY SEALED ADC

Featuring hermetic DIL packaging, the ADC-80 12-bit A-D converter is pin-for-pin compatible with other ADC-80 converters. It provides ±½ LSB linearity, and multiple input ranges. Supplied complete with internal clock, reference, and comparator, the device is factory laser-trimmed. Conversion rates of 40k conversions/s are specified for 12-bit accuracy, and truncation may be employed to achieve rates of more than 160k conversions/s for applications requiring 8-bit resolution. **Micro Networks Corp,** 324 Clark St, Worcester, MA 01601.

Circle 250 on Inquiry Card

PRINTING DIGITAL VOLTMETER

Model 700 combines a presettable digital timer and a drum printer using ordinary office machine paper tape; print time is selected by means of a thumbwheel switch on the front panel and is variable from 1 to 99 min. Interfaced with the printer, the DVM has a 0.6" (15 mm) LED display which is convenient for remote and continuous observation. When used as an independent controller, timer initiates the measurement process, but the printer prints only when an external print-ready signal occurs. Std range is 1.999 V; 100 mV, 10 V, and 100 V ranges are optionally available. **Columbus Instruments International Corp,** 950 Hague Ave, Columbus, OH 43204.

Circle 251 on Inquiry Card

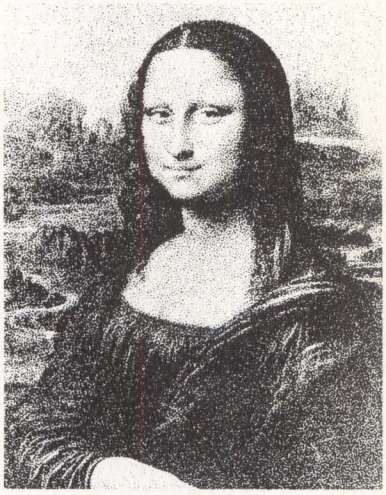
TIMESHARED OPERATING SYSTEM

Version 4B of the ETOS system for omnibus PDP-8 computers including -8/A permits any single user system to run in a timesharing environment, with up to 16 users. Multi-user OS/8 has simultaneous FORTRAN IV, assemblers, the company's extended BASIC, and COBOL/8. Timesharing, real-time tasks, and batch are provided simultaneously. OS/8 batch is also available. Features include printer and card reader spooling, support for detaching programs, private disc packs, and partial job accounting. **Educomp,** 196 Trumbull St, Hartford, CT 06103.

Circle 252 on Inquiry Card

DATUM ART VIGNETTES

Single Source? Not the Mona Lisa!



She smiles like that whenever they give her a lot of general data about only buying her peripherals from the mainframe manufacturer. But she's never decked by it because she knows about buying tape and disk systems. She knows that, at DATUM, she can get immediate delivery of controllers for a wider variety of peripherals . . . and save a lot of money, too.

Only DATUM has designed, built and installed over 7000 controllers and systems for so many different minicomputers to interface with such a variety of peripheral devices.

Check these tape-controller features: Triple-density NRZI formatting. Dual-density PE/NRZI formatting. 200 ips for all existing interfaces. Single-source responsibility for all major tape drives.

For that Mona Lisa smile, write DATUM now for specifications and prices.

Datum also manufactures cassette and rotating memories, data acquisition systems and timing instrumentation.

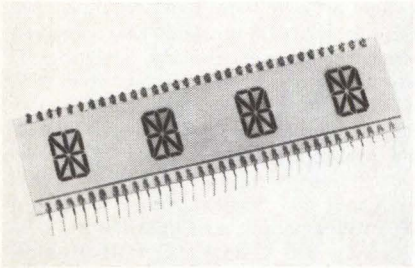
Peripheral Products Division
1363 S. State College Blvd., Anaheim, CA 92806 • 714/533-6333 EUROPE: Datum House, Cranford Lane, Harlington, Middlesex, UK • 01-897-0456

datum inc

CIRCLE 97 ON INQUIRY CARD

PRODUCTS

DIL ALPHANUMERIC LCD



A 16-segment design, the 3947 module includes 0.5″ (1.27 cm) high characters. Modules can be stacked side by side to make any alpha or numeric combination legend desired. Units are available in transmissive view mode with black characters on a clear background or with clear characters on a black background. Transflective and reflective modes have black characters on clear background. All LCDs are protected from humidity by a special coating; thermoplastic bonding provides max seal integrity. **Hamlin, Inc,** Lake & Grove Sts, Lake Mills, WI 53551.
Circle 253 on Inquiry Card

HEAD-PER-TRACK MEMORY SYSTEM

A fast, reliable random access rotating memory, the 4404 (4016) drum memory is functionally equivalent to the Data General 4019 Novadisc, occupies only 12¼″ (31.12 cm) of rack space, and provides up to 2M words of data storage. Compatibility includes the ability to run under RDOS. Controller occupies one card slot in the minicomputer CPU. Avg access time is 8.5 μs/word. Reliability and low data error rates are assured through use of automatic head retraction, conservative component derating, and power system monitoring. **Vermont Research Ltd,** Cleeve Rd, Leatherhead, Surrey KT 22 7NB, England.
Circle 254 on Inquiry Card

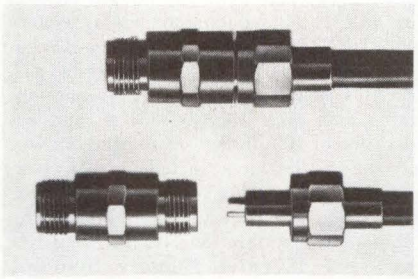
0.5″ HIGH LED DISPLAYS

Hercules series 1786 through 1789 consist of 0.5″ (12.70 mm) high, deep red characters, 0 to 9 with right hand decimal and ±1. LEDs are available in common cathode or anode configurations with typ 600 μcd/segment luminous intensity at 20 mA/1.7 V. Features include max current-to-brightness efficiency with high contrast ratio due to GaAsP emitting material, and wide-angle viewing. Ten horizontal in-line pin connections on 0.1″ (0.254-cm) spacing are adaptable to strip socket or PC board mounting. **Industrial Electronic Engineers, Inc,** 7740 Lemona Ave, Van Nuys, CA 91405.
Circle 255 on Inquiry Card

ZERO INSERTION FORCE SOCKET

Series 2944 24-position socket features self-ejection of LSI module, positive lock in loaded LSI position, and zero axial insertion force during loading cycle. Socket reduces danger of bending or breaking LSI leads during repeated insertions and withdrawals. The device accepts LSI lead spacing up to 0.650″ (1.651 cm) max, and 0.155 to 0.210″ (0.394 to 0.533 cm) lead lengths. 28-, 36-, and 40-position versions also are available. **Molex Inc,** 2222 Wellington Ct, Lisle, IL 60532.
Circle 256 on Inquiry Card

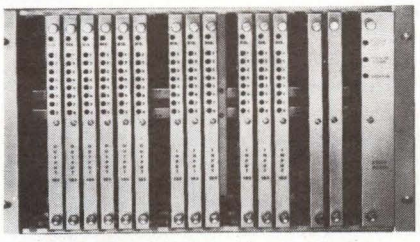
FIBER OPTIC CABLE-TO-CABLE CONNECTORS



"FiberheX" cable plugs and splicing sleeves for many fiber bundle sizes are precision machined for maximum coincidence of data carrying fibers at the interface, assuring lowest loss of signal. Fiber bundle is attached to the connector's bundle plug on the end of the cable. An interfacing threaded sleeve joins the two bundle plugs, aligning the interface. All parts of the connectors and interfacing sleeve are stainless steel to permit high torquing for mating the two fiber bundles. **Sealectro Corp, RF Components Div,** Mamaroneck, NY 10543.
Circle 257 on Inquiry Card

μ-PROCESSOR-BASED MULTIPLEXING SYSTEM

Transmission of control and feedback information between points up to 10,000 ft (3.04 km) apart is accomplished with the T-wire system that eliminates heavy conduit and field wiring. Operating in full- or half-duplex mode, basic system consists of two transmitter-receiver modules—one in the control area and one in the field area—connected by wire shielded cable or 3-wire cable (two for transmission, one for ground). I/O cards up to a maximum of 128 inputs and 128 outputs can be added. **Tenor Co, Inc,** 17020 W Rogers Dr, New Berlin, WI 53151.



Circle 258 on Inquiry Card

LSI-11 Micro-computer Data Acquisition System

The ADAC Model 600-LSI-11 is the first data acquisition system available for use with the DEC LSI-11/PDP-11/03 microcomputers.

Both software and hardware compatible, the Model 600-LSI-11 A/D system plugs directly into the bus of the LSI-11/PDP-11/03 systems.

Features include a 12 bit A/D converter, high speed sample and hold circuit, from 16 to 64 channels of MUX., DC/DC power converter and bus interfacing. A/D system throughput rate is 35 Khz.

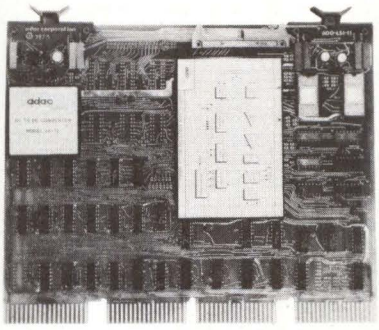
Optionally available are: one or two 12 bit D/As and programmable gain amplifier with auto zeroing circuit.

Basic system price in single quantity is $895.

Send for full technical data on the Model 600-LSI-11 and other ADAC minicomputer data acquisition and control systems and modules.

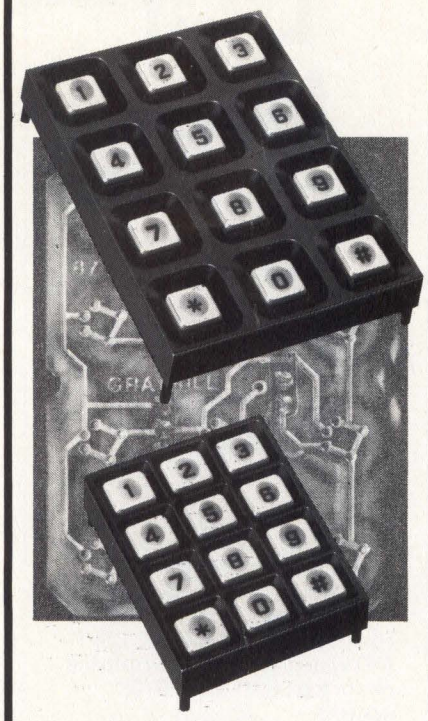
ADAC Corporation,
15 Cummings Park, Woburn,
MA 01801. (617) 935-6668.

GSA Contract Group 66.



adac corporation

A New Standard of Keyboard Quality



Grayhill 3x4 Keyboard Pads

for data input and telecommunications

2 out of 7 coded output—tested for millions of operations!

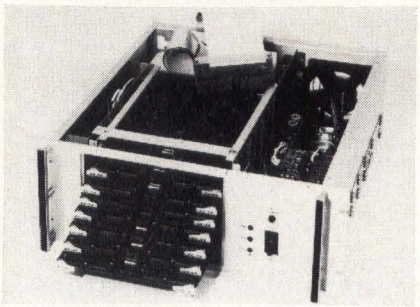
- **½″ or ¾″ button centers**
- **Excellent tactile and audio feedback**
- **Patented snap-action dome contact provides rugged, durable performance**

These new Grayhill low-profile, 12-button keyboard pads feature a 2 out of 7 coded output, standard mounting dimensions, and are ready for top-side or sub-panel mounting. The contact system is life-rated for 3,000,000 operations per button, and is readily interfaced with logic circuitry. The new Grayhill Series 87 modules offer excellent audio and tactile feedback characteristics with total button travel of only .015″. These durable keyboards are molded of tough ABS plastic; feature buttons with black on white molded-in legends as standard, and a variety of other legend options including clear snap-on caps for user legending. Complete specifications and truth table are provided in Bulletin #262, available free on request from Grayhill, Inc.
561 Hillgrove,
La Grange,
Illinois 60525
(312) 354-1040.

Grayhill INC.

PRODUCTS

ADD-ON MEMORY SYSTEM



The in-4011 semiconductor memory system for PDP-11 minicomputers stores 32k to 128k 18-bit words in a 7 x 19 x 17″ (17.78 x 48.26 x 43.18-cm) unit and operates with cycle time of 650 ns and access time of 500 ns. System expands in 16k increments. Features include parity generation and checking, integral parity registers, interface, and cabling. Interface is Unibus® compatible and includes parity error controls. **Intel Memory Systems,** 1302 N Mathilda Ave, Sunnyvale, CA 94086.
Circle 259 on Inquiry Card

μP-CONTROLLED TAPE-RECORDER/REPRODUCER

The Sabre X laboratory IRIG magnetic tape recorder/reproducer incorporates 10 electrically selectable tape speeds from 240 to $15\frac{5}{32}$ in/s (609.6 to 1.2 cm/s) for both record and reproduce, and dual functioning channel electronics. Other features include serial and/or parallel high density electronics, tape lifting from the R/R heads during a slew mode, and vacuum tape tensioning. A programmable microprocessor controls tape speeds, operating modes, monitor/alarm, and other diagnostic testing functions. **Sangamo Weston/Data Recorder Div,** PO Box 3347, Springfield, IL 62714.
Circle 260 on Inquiry Card

MODULAR PUSHBUTTON REED SWITCHES

Suited to interface with semiconductor circuits, precision-built 541 series switches have a reed element hermetically-sealed in a capsule to isolate contacts from contamination; impact and vibration-resistant glass-reinforced plastic housing; and welded internal connections. Electrical specs include 50-Vdc max switched voltage, resistive loading; 20-mA max switched current, resistive load; 1-GΩ min insulation resistance; and initial contact resistance of 0.5 Ω max rising to no more than 1.25 Ω at end of switch life. **Dialight, a North American Philips Co,** 203 Harrison Pl, Brooklyn, NY 11237.
Circle 261 on Inquiry Card

DC SERVOMOTOR CONTROLS

A line of solid-state four quadrant controls matched for use with the company's permanent magnet, pancake armature dc servomotors have peak outputs from 0.33 to 6.5 hp. Pulse-width and frequency modulated controls can supply 36 to 150 V and peak currents from 10 to 75 A. Frequency response is dc to 1 kHz with zero deadband and current form factors of 1.005. Gain stability and linearity are ±2% with max drift of 2 μV/°C. **PMI Motors, div of Kollmorgen Corp,** 31 Sea Cliff Ave, Glen Cove, NY 11542.
Circle 262 on Inquiry Card

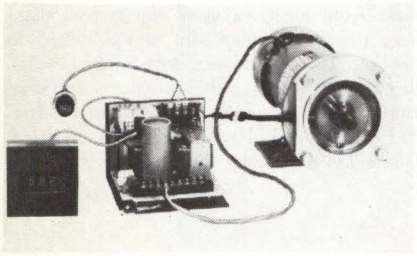
ELECTRONIC MAIL CAPABILITY

The electronic mail addition to the company's custom-tailored system 400 corporate message switching system provides rapid delivery of correspondence, with minimum handling, simplicity of originating messages, and access to the TWX and TELEX networks, meeting both domestic and international message requirements. Other features include least-cost routing, multiple priority levels, network accounting, security control, intercept capability, and capacity to support existing terminals and communications lines. **Norfield Electronics, Inc,** 3 Depot Pl, East Norwalk, CT 06855.
Circle 263 on Inquiry Card

MATRIX TELEPRINTER

Offering 30 char/s throughput, 94-char u/lc ASCII set, and 132-column format capability on 11″ (27.9 cm) wide fanfold paper, printer features a 9-wire impact printhead mechanism. Advanced MOS technology is used throughout the model 43 teleprinter. Portable desktop terminal weighs approx 30 lb (13.5 kg). Compatible with systems that support the company's model 33 terminals, it is available with an EIA or current loop interface. Controls are included for 10 or 30 char/s, half- or full-duplex operation, parity on/off, and printer test. **Teletype Corp,** 5555 Touhy Ave, Skokie, IL 60076.
Circle 264 on Inquiry Card

DIGITAL MOTOR SPEED CONTROL



Consisting of a chassis-mounting drive unit, panel-mounting potentiometer, and magnetic motor- or machine-speed sensor, the MC-141 is intended for dc motors up to ½ hp. A plug-in panel-mounting, 3- or 4-digit readout is optional for applications where speed monitoring is desired. Control accuracy is claimed to be 0.5%; the system automatically compensates for voltage and load variations. Max-min speed range is 20:1. System adapts to either single or multi-motor control. **Digital Systems Div, Detection Sciences Inc,** 14143-21st Ave N, Minneapolis, MN 55441.
Circle 265 on Inquiry Card

TRACKING TAPE

Outputs from the 0.5" (1.27 cm) magnetic tape allow instant verification of correct 7- or 9-channel head tracking (in forward and reverse directions), and indicate necessary mechanical adjustments. Tracking accuracy can be maintained within 0.0005" (0.00127 cm). A test in final Q.C. or field service could prevent a tape from overhanging both wear grooves either unevenly or excessively on one end, thereby causing tape flutter and end channel errors. The 600- or 1200-ft tape prevents premature head failures caused by this uneven wear. **Pericomp Corp,** 14 Huron Dr, Natick, MA 01760.
Circle 266 on Inquiry Card

µCOMPUTER-COMPATIBLE DATA ACQUISITION SYSTEM

Model 735 series is mounted on a single PC board that plugs directly into the same card cage as the Intel SBC-80/10 and /20 single board computers, and MDS-800 microcomputer development system. Bus interface includes a software choice of program control or program interrupt and a jumper choice of memory-mapped or isolated I/O. Basic system consists of 16 single-ended, or eight differential analog input channels, voltage or current inputs, 12-bit ADC, sample/hold, and bus interface. **Adac Corp,** 15 Cummings Pk, Woburn, MA 01801.
Circle 267 on Inquiry Card

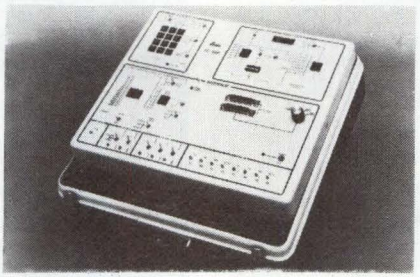
MINIATURE TOGGLE SWITCHES

Designed to meet demands for high quality, long life, and small size, toggle mechanism provides positive actuation and is easily mounted. Available in 1-, 2-, 3-, and 4-pole versions, the switches have contact resistance of 10 mΩ max initial at 2 to 4 Vdc, 0.1 A for both silver and gold contacts. Dielectric strength is 1 kV rms, and electrical life is 100,000 cycles make and break at full load for standard detent models. Contact ratings are 5 A, 120 Vac or 28 Vdc, 2 A, 250 Vac. **UID Electronics Div, AMF Inc,** 4105 Pembroke Rd, Hollywood, FL 33021.
Circle 268 on Inquiry Card

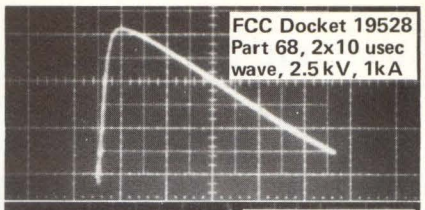
FLOPPY DISC DRIVE

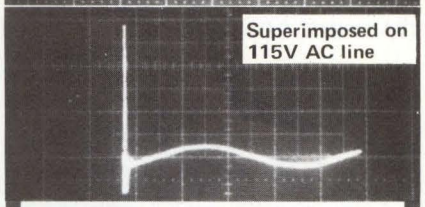
Providing formatter and interface on a single card which plugs directly into the processor small peripheral slot, the FD-11/L is a dual floppy disc add-on for the LSI-11. Features include total software compatibility with DEC's RX-11 instruction set, write protect and unit select switches, IBM 3740 format, p/ROM self-diagnostic, bootstrap loader, and microprocessor-based controller design. Access times are 6 ms track-to-track and 170 ms avg seek time. **Charles River Data Systems, Inc,** 235 Bear Hill Rd, Waltham, MA 02154.
Circle 269 on Inquiry Card

PORTABLE DATA COMMUNICATION TEST SET



The microprogrammed TC-100P performs a range of sophisticated diagnostic routines that traditionally have been difficult to perform during field testing. It can simulate and test all components of the data network including communication circuits, modems, terminals, and computer ports, and can handle both hardware and software. Keyboard entry, digital display, and clearly labeled controls provide operator convenience in performing a variety of tests. **Cooke Engineering Div, Dynatech Laboratories, Inc,** 900 Slaters Lane, Alexandria, VA 22314.
Circle 270 on Inquiry Card





Precision SURGE TESTING

FOR DESIGN AND QC CHECKS ON TELECOM CIRCUITS AND SYSTEMS

KeyTek's new Model 424 Surge Generator/Monitor is the first commercially - available, self-contained instrument for generating and measuring the peak values of classic transient pulse forms. Produces both oscillatory and impulse waves, such as the FCC-defined 2x10 at 2500V and 1kA. Includes built-in AC-line coupling/isolation as shown above. Other possible wave forms include 10x160, 10x560, 8x20, 1.2x50, etc. Test circuits, varistors, silicon avalanche devices, gas tubes and networks of all types. Ideal for engineering, QC and production.

Programmable Pulses: The versatile Model 424 can be programmed, by plug-in networks, to produce a wide variety of pulse shapes, with amplitudes to 6000 volts and currents to 2000 amperes.

Send for complete product data and new article on surge protection and testing . . . yours FREE

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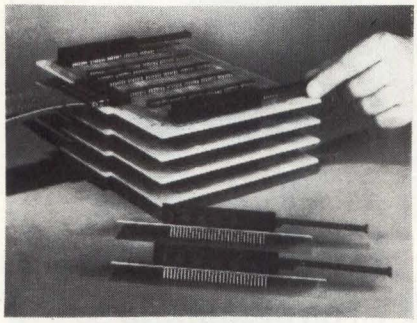
INSTRUMENT CORPORATION
220 GROVE STREET, BOX 109
WALTHAM, MASS. 02154
TEL. (617) 899-6200

PRODUCTS

ZERO INSERTION FORCE STACKING CONNECTOR



Designed to interconnect with backplane or motherboard in bus-oriented systems, connectors require only 0.500″ (12.7 mm) mounting width. Capable of stacking PC boards from 0.060 to 0.093″ (1.524 to 2.36 mm) thick on 0.600″ (15.24 mm) intervals, devices have post contacts on 0.100 x 0.100″ (2.54 x 2.54 mm) grid spacing to mate with each other or with several std varieties of connectors. Activating mechanism requires 0.420″ (10.66 mm) of linear travel to release the connectors or establish electrical contact. **AMP Inc,** Harrisburg, PA 17105.
Circle 271 on Inquiry Card

COMPUTER DISPLAY TERMINAL

The model 132A microprocessor-controlled interactive terminal, claimed to be the first to accommodate up to 132 columns, interfaces directly with std computer systems using 132-col output format. The terminal's Charactron® CRT instantly generates high quality alphanumeric characters and symbols. Basic unit with 8k buffer memory (16k optional) offers 96 u/lc ASCII char set, 60- or 120-line buffer, cursor control, multiple asynchronous transmission modes at 110 to 9600 bits/s in full- or half-duplex, and an RS-232-C output to 132-col serial printer. **DatagraphiX,** PO Box 82449, San Diego, CA 92138.
Circle 272 on Inquiry Card

FLOPPY DISC UNIT

A floppy disc unit for the ADAM business computer, disk/45 is a device which reads and writes IBM std diskettes. Integrated unit includes drive, power supply, and controller, which attaches to the computer as an "add-on" or as original equipment. Computer can read information from the diskette faster than an operator can type, and information is provided from the computer onto the disc for transfer to another computer system. Disc holds approx 250k char. **Logical Machine Corp,** 1294 Hammerwood Ave, Sunnyvale, CA 94086.
Circle 273 on Inquiry Card

HIGH DENSITY CONNECTORS

A series of low insertion force, 2-piece connectors meeting DIN standard 41612 are available in 16-, 32-, 48-, 64-, and 96-contact versions. Devices have different body widths but common length and mounting centers. Plug soldering directly to the PC board, connectors have an integral insulating shroud that protects contacts from electrical and mechanical damage. Plug and receptacle are polarized to prevent 180-deg mismating. Solder eyelet, dip solder, and solderless wrap terminations are available. **Vero Electronics, Inc,** 171 Bridge Rd, Hauppauge, NY 11787.
Circle 274 on Inquiry Card

S-D TRACKING CONVERTER

Operating from synchro reference voltages of either 26 or 115 V rms and from frequencies ranging from 50 to 400 Hz, the 14-bit 1651-24 automatically senses and responds to various input voltages and frequencies of synchro or resolver and converts angular information into 14 bits of binary data with no loss of tracking accuracy or resolution. This eliminates the need for separate conversion modules when changing voltage or frequency. Accuracy is ±4 arc min over the 0 to 70°C or −55 to 85°C temp range. **Transmagnetics, Inc,** 210 Adams Blvd, Farmingdale, NY 11735.
Circle 275 on Inquiry Card

Noise sensitivity problems go away- we guarantee it!

Topaz Ultra-Isolation Transformers provide an inexpensive and reliable way to supply clean, noise-free AC power to sensitive equipment such as computers, instrumentation, communication and process control equipment.

Ultra-Isolation Transformers offer the industry's best noise attenuation:

- Common-mode noise rejection greater than 145 dB.
- Transverse-mode noise rejection greater than 125 dB at 1 kHz.
- Standard models 125 VA to 130 kVA.
- Priced from $64.

Our guarantee: A Topaz Ultra-Isolation Transformer will solve your noise sensitivity problems to your complete satisfaction or we'll take it back— no questions asked.

TOPAZ ELECTRONICS — SOLUTIONS TO POWER PROBLEMS

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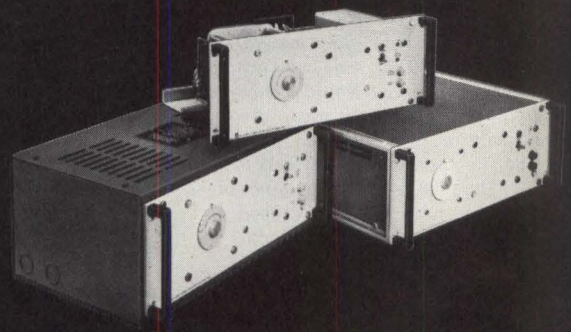
CIRCLE 103 ON INQUIRY CARD

Your answer to line-voltage problems



Variac® Automatic Voltage Regulators

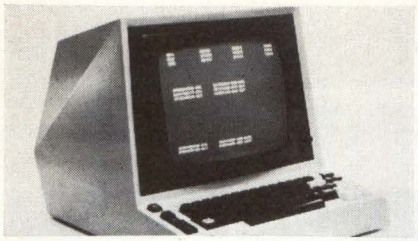
- Regulation to 0.2%
- Up to ±20% correction
- Models range from 8.7A to 85A
- Input: 50, 60 or 400 Hz; 120 or 240V

Contact your nearest GenRad sales office or write for descriptive catalog. 300 Baker Avenue, Concord, MA 01742, Telephone: (617)369-8770.

GenRad

CIRCLE 104 ON INQUIRY CARD

VIDEO DATA DISPLAY TERMINAL

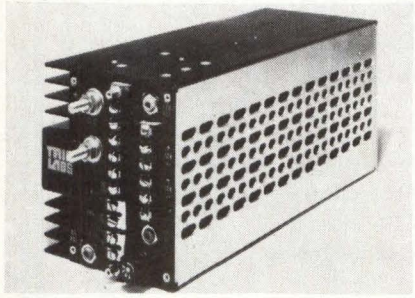


Std features of the Teletype™-compatible VC303A include serial asynchronous RS-232 interface, 1920-char display (24 lines x 80 char), eight switch-selectable data rates from 110 to 9600 baud, 12″ (30.48 cm) nonglare CRT, composite video output for slave monitors, and direct X-Y cursor addressing by computer or operator. The 64-char ASCII keyboard has easy to use cursor control key cluster, tactile feedback, and auto repeat. A detached 11-key numeric pad is optional. **Volker-Craig Ltd,** 266 Marsland Dr, Waterloo, Ontario N2J 3Z1, Canada.
Circle 276 on Inquiry Card

HIGH PERFORMANCE ADC

Meeting requirements of MIL-STD-883, Level B, ZAD3214 is a 14-bit ADC, capable of withstanding severe environments. Fully encapsulated and sealed in a rugged metal case measuring 2.12 x 4.0 x 0.45″ (5.38 x 10.16 x 1.14 cm), device features conversion time of 100 μs max, differential nonlinearity of ±½ LSB max, and input range of 0 to 10 V. Output coding is unipolar binary. Op temp range is −25 to 100°C; storage temp is −55 to 125°C. Unit is capable of withstanding peak shock of 350 G and vibration to 20 G. **Zeltex, Inc,** 940 Detroit Ave, Concord, CA 94518.
Circle 277 on Inquiry Card

3-OUTPUT SWITCHING POWER SUPPLY



The model 673 features a main output of 5 V at 20 A and two additional series-regulated outputs at either ±12, ±15, ±18, 12/5, 15/5, or 18/5 V; all at 2 A. The unit has an output on/off control, remote sense, ±10% output voltage adjust, overvoltage and overload protection, and MTBF of 40,000 h. Total output is 175 W. **Trio Labs, Inc,** 80 Dupont St, Plainview, NY 11803.
Circle 278 on Inquiry Card

POWER MODULE

Low cost ac to dc modular power supplies, series "B" NL units provide single outputs of 5 V/6 A, 12 V/3.5 A, 15 V/3 A, 24 V/2.4 A, and 28 V/12 A. Std input is 115 Vac, 47 to 440 Hz with 220 Vac available. Dual primaries may also be obtained. All units feature tight regulation, low ripple, and full load operation at 50°C ambient temperature with derating to 40% at 71°C. Case size is 5⅝ x 4⅞ x 2½″ (14.29 x 12.38 x 6.35 cm) with mounting on three surfaces. **Abbott Industrial Products Div, Abbott Transistor Laboratories, Inc,** 639 S Glenwood Pl, Burbank, CA 91506.
Circle 279 on Inquiry Card

MIL-SPEC ADC

An ADC interface module for the company's computers, model 3656 accepts bipolar (−2.5 to 2.5 V, −5 to 5 V, and −10 to 10 V) or unipolar (0 to 5 V and 0 to 10 V) differential analog input signals and performs a 12-bit conversion in 24 μs. Features include optional onboard multiplexing of up to 16 differential input channels with facilities for offboard multiplexing of up to 256 inputs, optional sample-and-hold logic, external triggering, and DMA capability. **Rolm Corp,** 4900 Old Ironsides Dr, Santa Clara, CA 95050.
Circle 280 on Inquiry Card

LOW LEVEL MULTIPLEXER

LLM series, which can be assembled in configurations including 2000 individual channels, is designed to provide a low level analog input system to the company's GM series A-D conversion system. High speed solid-state switching is combined with advanced low level transformer design. Specs include common mode rejection of >130 dB from dc to 60 Hz; pumpout current of $<10^{-9}$ A; and high speed multiplexing with data sampling rates up to 50 kHz. **Preston Scientific, Inc,** 805 E Cerritos Ave, Anaheim, CA 92805.
Circle 281 on Inquiry Card

MAGNETIC HEADS FOR FLOPPY DISC DRIVES

Magnetic heads (models 623100 and 623101) are intended for double-sided drives designed for media interchange with IBM model 43FD. Std assembly consists of ferrite/ceramic single-track mag head with a R/W and tunnel erase section, flexible PC lead-in cable, and load arm, all mounted on a flexure spring attached to a flexure support. In operation, two head assemblies face each other on opposite sides of the flexible disc. Max packing density is 3268 bits/in; radial density is 48 tracks/in. **Applied Magnetics Corp, Magnetic Head Div,** 75 Robin Hill Rd, Goleta, CA 93017.
Circle 282 on Inquiry Card

Give your PDP-11 a kick in the Fourier Transformation.

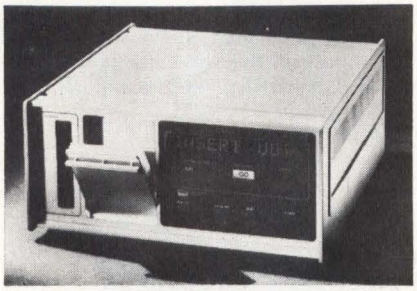
Your computer could do digital signal processing a lot faster. Just plug in our MFFT Array Processor and your PDP-11 will do Fast Fourier Transformations in 160 ms for 1024 real points. That's about 10 to 20 times faster than before.

No other hardware is needed. Just plug in the Elsytec MFFT. Standard program modules are furnished in Assembly or FORTRAN language for incorporation with your software. You'll also be able to speed up array computation for correlating, transfer function, PSD, and coherence.

The cost is $6900 for PDP-11 users, plus $300 if FORTRAN programming is required. Or we'll put together the whole system, including CPU, analog I/O, MFFT and software. There is also an MFFT model for Data General Nova or Eclipse users at $5900. Call or write for details: Elsytec, a Wavetek operation, 6150 Canoga Avenue, Suite 100, Woodland Hills, CA 91367. (213) 884-5200.

WAVETEK®

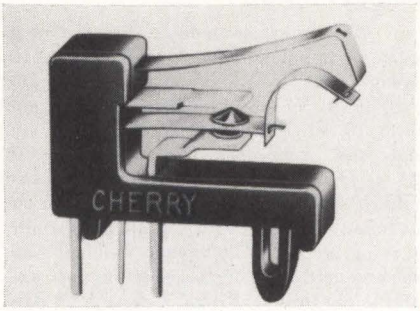
PORTABLE AUTOMATIC MODULE TESTER



Weighing approx 30 lb (13.5 kg), the unit provides the flexibility for "on-the-spot" testing of digital circuit cards or logic. Its interactive alphanumeric display system allows the operator to interact with the tester, in many cases eliminating the need for a separate test instruction manual. A microprocessor provides test sequence control. Test programs are stored on p/ROM cards which allow tests to be matched with modules prior to power turn-on. The unit automatically tests itself when turned on and can fault-isolate its own modules. **Bendix Corp, Test Systems Div,** Teterboro, NJ 07608.
Circle 283 on Inquiry Card

SUBMINIATURE PCB SWITCH

Snap-action S38-20H, designed for easy mounting and use with a PC board, has a flexible front mounting peg which allows the device to be simply plugged in. No additional hardware is necessary. Measuring 0.658 x 0.768 x 0.228″ (16.7 x 19.5 x 5.79 mm), the unit is suitable for space-limited applications. When mounted on a PC board, the top of the switch is <½″ (12.7 mm) above the board surface. Gold crosspoint contacts are optionally available for low energy applications. **Cherry Electrical Products Corp,** 3600 Sunset Ave, Waukegan, IL 60085.



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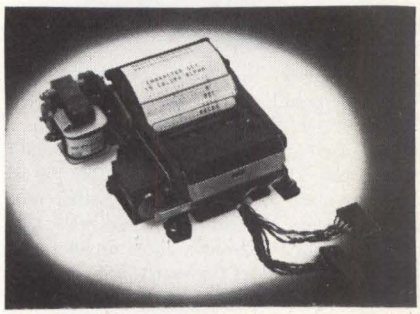
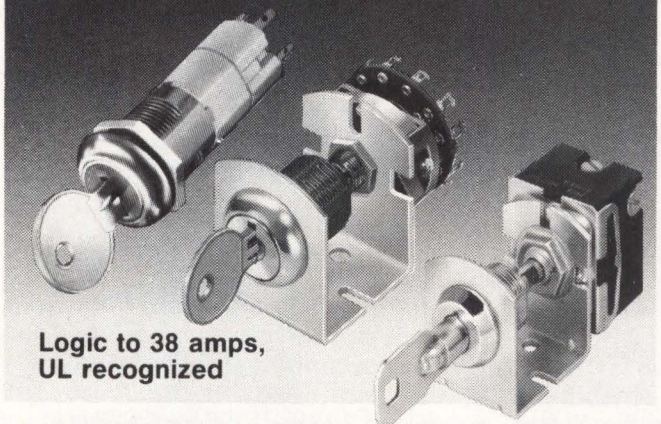
ALPHANUMERIC IMPACT PRINTER



Capable of printing up to 3 lines/s for numeric and 1.5 lines/s for alphanumeric, PR1500 printers offer full 54-char set and multicopy printing capabilities. Characters for every three of the 15 columns are formed by "spanning hammers." Device offers 500-ms start-up time with subsequent line feed of up to 10 lines/s. Drive motor power consumption is 11 W. Options include drum type fonts, 50-Hz operation, and vertical mounting. **Sheldon-Sodeco Div, Landis & Gyr, Inc,** 4 Westchester Plaza, Elmsford, NY 10523.
Circle 285 on Inquiry Card

Solve your security problems with OAK's complete line of KEYLOCK AND KEY SWITCHES



Logic to 38 amps, UL recognized

ANTI-STATIC keylock switches, logic level and rated to 4 amps, protect equipment against static discharges to 20,000 volts.

HIGH AND LOW POWER key and keylock switches are available from 2 to 12 positions in almost any switching combination or power requirement.

Many types are stocked by Oak distributors. Call or write for additional information.

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(513) 223-8161

For more information, Circle 106 on Inquiry Card.
Have a salesman call. Circle 107 on Inquiry Card.

CIRCLE 108 ON INQUIRY CARD

LITERATURE

Acoustic Couplers and Modems

Applications brochure outlines specs on products which allow data communications for remote computer access, TWX, and computer end send or receive devices. **Omnitec Data Corp,** Phoenix, Ariz.
Circle 300 on Inquiry Card

Precision Miniature Motors

Application factors and ac/dc motor performance are discussed in *Mini Motor Idea Index, Vol II* describing 21 motors which perform multiple functions in single units. **TRW Globe Motors, an Electronic Components Div of TRW Inc,** Dayton, Ohio.
Circle 301 on Inquiry Card

Multiplier Module

Features of the 602 4-quadrant multiplier module and mounting kit are provided in brochure, along with theory of operation, applications, specs, and accuracy information. **Calex Mfg Co, Inc,** Pleasant Hill, Calif.
Circle 302 on Inquiry Card

Keyboards and Switches

Bulletin furnishes specs, features, materials, layouts, dimensions, and diagrams on the Wild Rover® PCK series keyboards and switches for Touch-Tone® and business machine uses, or custom design. **Refac Electronics Corp,** Winsted, Calif.
Circle 303 on Inquiry Card

Cooling Systems

Illustrated catalog includes specs, options, RFI shielding information, mechanical drawings, and pressure charts for line of cooling systems ranging from 200 to 1200 ft^3/min. **Zero Corp,** Burbank, Calif.
Circle 304 on Inquiry Card

Switching Relay

Basics of the modified type D2A Multireed® relay for use in low level, multiple signal measurement applications are presented in technical bulletin. **Thermosen, Inc,** Stamford, Conn.
Circle 305 on Inquiry Card

Planar Interconnect Systems

Illustrated fold-out brochure briefly covers line of round and flat conductor planar laminated and bonded cables, and associated connectors. **Spectra-Strip,** Garden Grove, Calif.
Circle 306 on Inquiry Card

Education and Development Microcomputer

Descriptions, specs, accessories, and block diagrams of the 8080A 8-bit microprocessor-based MMD-1 Mini-Micro Designer are furnished in brochure. **E&L Instruments, Inc,** Derby, Conn.
Circle 307 on Inquiry Card

Electronic Packaging Hardware and Services

An overview of available hardware—wirewrap boards, cards, files, panels, and large assemblies—as well as optional wiring and documentation services is offered in illustrated brochures. **EECO,** Santa Ana, Calif.
Circle 308 on Inquiry Card

Uninterruptible Power Systems

Data sheets for line of UPS modules rated from 25 to 600 kVA feature information on electrical, physical, and environmental specs; standard features; options; and battery specs. **Teledyne Inet,** Gardena, Calif.
Circle 309 on Inquiry Card

Printers/Plotters

Brochure considers various techniques and applications of all printer/plotters, including drive and toning systems, microprocessors, output media, system configurations, and terminology. **Varian Graphics,** Palo Alto, Calif.
Circle 310 on Inquiry Card

IC Chips

Guaranteed electrical and mechanical specs of std line of linear ICs which are available in three electrical grades are listed in catalog. **Precision Monolithics, Inc,** Santa Clara, Calif.
Circle 311 on Inquiry Card

Data Communications Equipment

A 12-panel short-form folder provides details and photos of family of equipment and systems that monitor, control, and test data communications systems. **Spectron Corp,** Mt Laurel, NJ.
Circle 312 on Inquiry Card

Semiconductor Testers

Condensed specs highlight brochure featuring four discrete semiconductor test instruments, probe, and Dynapeak™ digital-pulse testing technique. **B&K-Precision,** Chicago, Ill.
Circle 313 on Inquiry Card

Microprocessor-Based Control System

Diagram and photos illustrate bulletin discussing key features of the 8000 ASCII computer interface and centralized control system, and information on the optional display and backup panel. **Beckman Instruments, Inc, Process Instruments Div,** Fullerton, Calif.
Circle 314 on Inquiry Card

Video RAM TV Controllers

Summarizing physical and electrical characteristics, brochure introduces family of VRAM controllers which provide an alphanumeric or graphic interface between a microprocessor and TV CRT. **Matrox Electronic Systems,** Montreal, Quebec, Canada.
Circle 315 on Inquiry Card

Miniaturized Momentary Action Pushbutton Switch

Product bulletin examines the Hi-D switch® with molded box construction and PC terminals, presenting diagrams, features, mounting and wiring information, and material specs. **Switchcraft, Inc,** Chicago, Ill.
Circle 316 on Inquiry Card

Mineral Insulated Thermocouples

General features and ordering information for 13 basic types of thermocouples are depicted in tables, drawings, and wire gauge charts contained in catalog. **Gulton Industries, Inc, Measurement and Control Systems Div,** East Greenwich, RI.
Circle 317 on Inquiry Card

Ceramic Capacitors

Complete with charts and graphs, catalog discusses monolithic and glass encapsulated capacitors offered with various dielectrics, voltages, temp ranges, and capacitance tolerances. **GTI Corp, Capacitor Div,** San Diego, Calif.
Circle 318 on Inquiry Card

Testing Instruments and Systems

Illustrations and technical data in summary catalog cover measuring and electrical instruments used for such measurements as high and low resistance, speed, and power factor. **James G. Biddle Co,** Plymouth Meeting, Pa.
Circle 319 on Inquiry Card

Tone Relaying Test Set

Complete with technical descriptions, specs, and applications, brochure provides an in-depth discussion of a concept in evaluation of tone transfer trip systems and FSK tones using the model 675 test set. **RFL Industries, Inc,** Boonton, NJ.
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