OCTOBER 1980

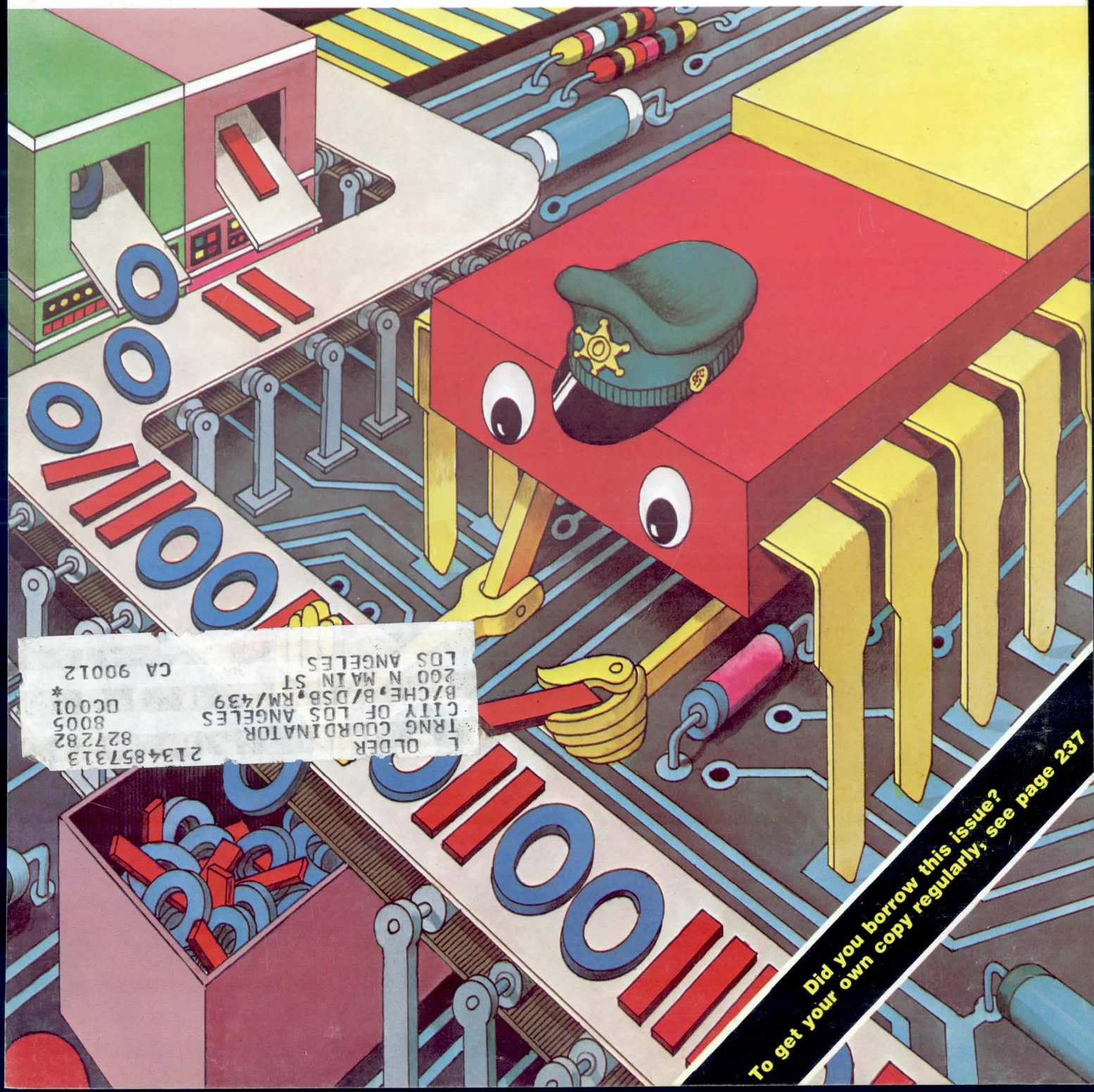
COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

ECC CHIP REDUCES ERROR RATE IN DYNAMIC RAMS

A BASIC TECHNIQUE FOR REALTIME SYSTEM DESIGN

IEEE 488 BUS TESTING PROBLEMS AND SOLUTIONS



Introducing the single board LSI-11* tape controller.

- Totally software transparent runs DEC operating and diagnostic software.
- Embeds in all LSI-11 series computers.
- Allows mixing 9-track, PE, NRZ or dual-density tape† units in any combination.
- 33-word data buffer allows automatic non-stop operation without special software.
- Integral LED self-test.
- 1-year warranty.
- 30-day delivery.

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Western Peripherals is the leading independent controller manufacturer. We're known throughout the industry for quality and reliability.

Our nationwide service and worldwide distributor service network provide support wherever you are.

For complete information on the TC-151 and our entire line of controllers, call or write Western Peripherals, 14321 Myford Road, Tustin, California 92680. (714) 730-6250 TWX: 910 595-1775 CABLE: WESPER

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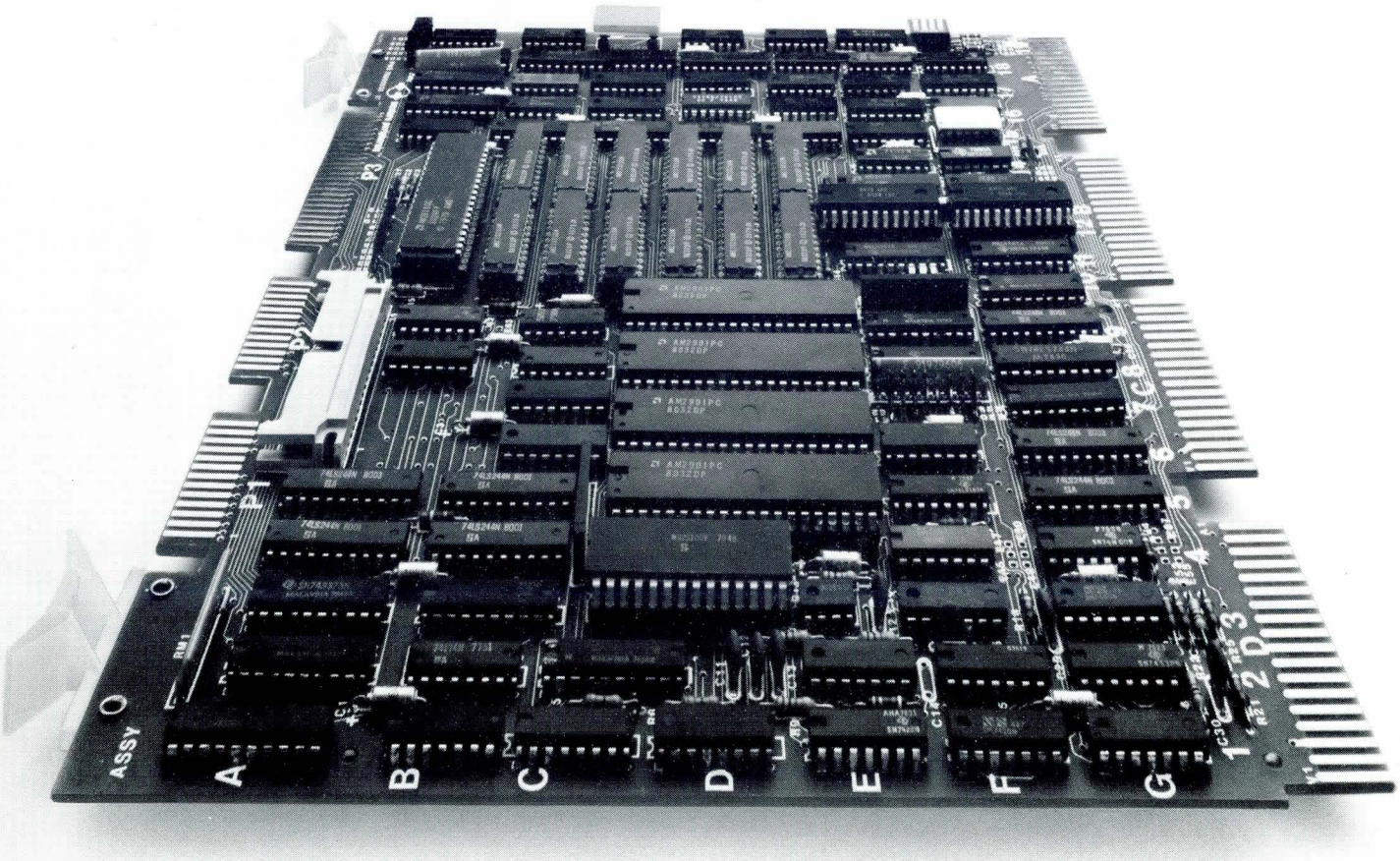

TC-151

†PE requires an additional half board
*Trade name of Digital Equipment Corporation

Number 1 in controllers.

CIRCLE 1 ON INQUIRY CARD

Fastest Data On Two Reels

The winners—Model 9300 (125 ips) and 9100 (75 ips) Vacuum Column Tape Transports. They're the fastest—and most dependable in their circuit.

Speed isn't their only advantage—they handle beautifully. Data densities of 200/556 cpi or 556/800 on the 7-track unit and 800 cpi, 1600 cpi or 800/1600 cpi on the 9-track. The format is NRZ1/PE.

They're fully equipped, with features such as capacitive tape-location detectors for improved tape life, hard coated read-after-write heads to reduce tape wear, crystal controlled timing, front-accessible test panel—all the features that make Kennedy tape transports the industry standard.

Just one thing—don't expect a deep-throated roar when you start up. Models 9100/9300 have the lowest noise levels in their class. Typically Kennedy—fast, reliable and quiet.

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(213) 357-8831 TWX 910-585-3249

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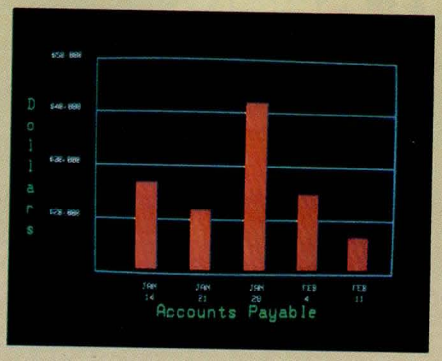
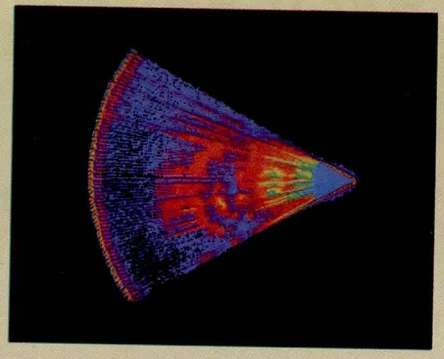
CIRCLE 2 ON INQUIRY CARD



Management Information Display



Ultrasonic heart sector scan

High-resolution display with alphanumerics

Get the professional color display that has BASIC/FORTRAN simplicity

LOW-PRICED, TOO

Here's a color display that has everything: professional-level resolution, enormous color range, easy software, NTSC conformance, and low price.

Basically, this new Cromemco Model SDI* is a two-board interface that plugs into any Cromemco computer.

The SDI then maps computer display memory content onto a convenient color monitor to give high-quality, high-resolution displays (756 H x 482 V pixels).

When we say the SDI results in a high-quality professional display, we mean **you can't get higher resolution than this system offers in an** NTSC-conforming display.

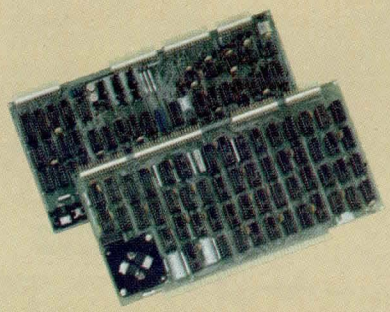
The resolution surpasses that of a color TV picture.

BASIC/FORTRAN programming

Besides its high resolution and low price, the new SDI lets you control with optional Cromemco software packages that use simple BASIC- and FORTRAN-like commands.

Pick any of 16 colors (from a 4096-color palette) with instructions like DEFCLR (c, R, G, B). Or obtain a circle of specified size, location, and color with XCIRC (x, y, r, c).

*U.S. Pat. No. 4121283



Model SDI High-Resolution Color Graphics Interface

HIGH RESOLUTION

The SDI's high resolution gives a professional-quality display that strictly meets NTSC requirements. You get 756 pixels on every visible line of the NTSC standard display of 482 image lines. Vertical line spacing is 1 pixel.

To achieve the high-quality display, a separate output signal is produced for each of the three component colors (red, green, blue). This yields a sharper image than is possible using an NTSC-composite video signal and color TV set. Full image quality is readily realized with our high-quality RGB Monitor or any conventional red/green/blue monitor common in TV work.

Model SDI plugs into Z-2H 11-megabyte hard disk computer or any Cromemco computer

DISPLAY MEMORY

Along with the SDI we also offer an optional fast and novel **two-port** memory that gives independent high-speed access to the computer memory. The two-port memory stores one full display, permitting fast computer operation even during display.

CONTACT YOUR REP NOW

The Model SDI has been used in scientific work, engineering, business, TV, color graphics, and other areas. It's a good example of how Cromemco keeps computers in the field up to date, since it turns any Cromemco computer into an up-to-date color display computer.

The SDI has still more features that you should be informed about. So contact your Cromemco representative now and see all that the SDI will do for you.

Cromemco
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Tomorrow's computers today

CIRCLE 3 ON INQUIRY CARD

COMPUTER DESIGN THE MAGAZINE OF COMPUTER BASED SYSTEMS

VOLUME 19, NUMBER 10 OCTOBER 1980

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FEATURES

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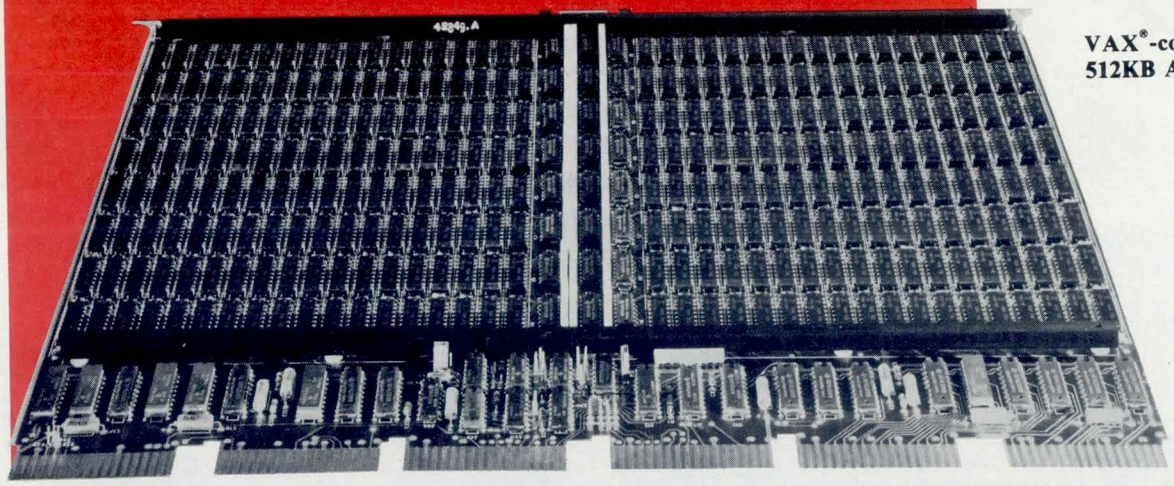
ADD-ON ADD-IN

MEMORY...FROM THE LEADER



VAX®-compatible 512KB ADD-IN

There's lots of good reasons to buy your ADD-ON/ADD-IN memory from the leader.

For starters, there's the wide range of core and semi mini-memories we offer. The industry's widest. In fact, Dataram is the only company in the world supplying minicomputer-compatible core and semiconductor main memory and disk emulation systems. The *only* company.

And Dataram ADD-ON/ADD-IN products do more. Like save money...as well as valuable space in your minicomputer. And they increase throughput and improve overall performance.

Just some of the reasons why Dataram is the leading supplier of ADD-ON/ADD-IN memory for the minicomputer industry...and shipping at an annual rate of $25 million.

Want more reasons? If you're using a minicomputer, and want to get more for your memory dollar, talk to us. We're very reason-able. Dataram.

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VARIAN	✓	
INTEL	✓	

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☐ Please send information.
☐ Please have a salesman contact me.

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Title _____ Phone _____

Company _____

Address _____

City _____ State _____ Zip _____

Canada: Ahearn & Soper Ltd., Alberta, British Columbia, Ontario, Quebec • **Finland:** Systek OY, 737-233; **France:** YREL, 956 81 42 • **Hungary/Poland/Rumania:** Unitronex Corporation, WARSAW 39 6218 • **Italy:** ESE s.r.l., 02/6073626 • **Netherlands:** Technitron b.v., 020-45 87 55 • **Sweden:** M. Stenhardt AB, (08) 739 00 50 • **Switzerland:** ADCOMP AG, 01/730 48 48 • **United Kingdom:** Sintrom Ellinor Ltd., (0734) 85464 • **West Germany:** O.E.M.-Elektronik GmbH, 07 11-79 80 47 • **Australia/New Zealand:** Anderson Digital Equipment, (03) 543 2077 • **India:** Industrial Electronic Instruments, 79281 • **Israel:** Minix Computers & Systems Ltd., 03-298783 • **Japan:** Matsushita Electric Trading Co., Ltd., 03 (435) 4501

CIRCLE 5 ON INQUIRY CARD

BIOMATION K100-D

Compare this general purpose logic analyzer with the currently accepted industry standard.

The K100-D wins over Hewlett-Packard's 1615A hands down!

Logic designers have made Gould's powerful Biomation K100-D our fastest selling logic analyzer

ever. You'll see why once you compare it to its nearest competitor, the 1615A from Hewlett-Packard.

Compare clocking speed.

With a 100 MHz clock rate, the K100-D gives you resolution to 10 ns—*five times better than the 1615A's.* Use the K100-D's latch mode to catch gliches as narrow as 4 ns. It gives you the most precise logic analysis for today's high speed minicomputer, mainframe and microprocessor systems. Best of all, you're already prepared for faster designs as they arrive.

Compare capacity.

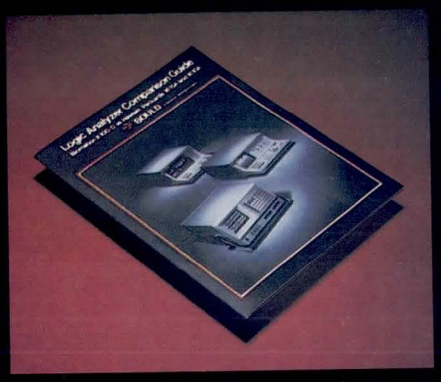
The K100-D's 1024 word memory is *four times as deep as the 1615A's.* This dramatically extends the length of data you can trap from your system at any one time. And that means faster, more accurate debugging. In addition, the K100-D's standard 16 channel format can be expanded to 32 channels for work on the new generation of 16-bit microprocessors.

Compare your productivity.

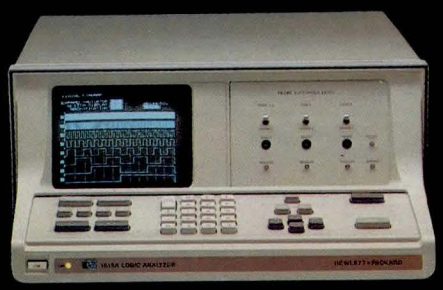
Finally, the K100-D makes designers more productive with convenience features superior to those of the 1615A. The K100-D has a larger keyboard, plus an interactive video display. Comprehensive status menu. Data domain readout in hexadecimal, octal, binary or ASCII. And the list goes on and on.

The final analysis.

To help you evaluate these two fine instruments before you buy, we've prepared a point-by-point *competitive comparison* of the two. If you're designing and debugging high-performance digital systems, you'll want to read this document carefully. To get your free copy, just use the reader service number or write Gould Inc., Biomation Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For faster response, call 408-988-6800.



Hewlett-Packard 1615A
A very good logic analyzer



Speed: to 20 MHz
Resolution: 50 ns
Memory: 256 words
Channels: 8 timing & 16 data, or 24 data

Biomation K100-D
The industry's finest logic analyzer

Speed: to 100 MHz
Resolution: 10 ns
Memory: 1024 words
Channels: 16 timing or 16 data, or 32 data

GOULD
An Electrical/Electronics Company

CIRCLE 6 ON INQUIRY CARD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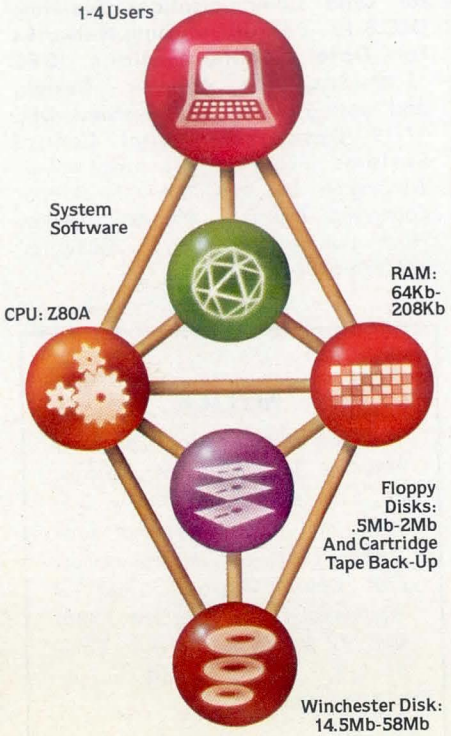
COMPUTER SYSTEMS
ALTOS
COMPUTER SYSTEMS
Built On Dependability
ALTOS
BRAND
QUALITY
RELIABILITY
DELIVERY
PROVEN VALUE
COMPUTER · SYSTEMS
PRODUCED IN THE HEART OF SILICON VALLEY, CALIFORNIA U.S.A.

FRESH IDEAS ARE GROWING AT ALTOS

Silicon Valley, California. At one time few places in the world were as abundant with orchards. Today, no other area is as technologically fertile. And nowhere on earth is the business climate as prolific with computer innovation.

Yet within this competitive environment, one microcomputer firm continues to grow above the rest. Altos Computer Systems. Recognized as a world leader in single board microcomputer technology, Altos flourishes on its ability to produce ideas and deliver them to the market while they're still fresh and packed with price performance value.



Fresh ideas like Altos' new ACS8000-6/MTU single board microcomputer system with a DEI ¼-inch cartridge tape back-up drive, and Shugart's 8-inch floppy and 14-inch Winchester hard disk drives, with total on-line capacities from 14.5 MBytes to 58 MBytes.

The ACS8000-6/MTU joins Altos' growing family of products that branch out to a multitude of single board system configurations to serve the OEM, the business sector, and many other end users. These systems range from the ACS8000-2 with its dual 8-inch floppy disk drives, to the powerful ACS8000-5, which is upgradable to any of Altos' hard disk and multi-user systems.

Altos supports three industry standard operating systems: single/multi-user CP/M*, OASIS,† and Altos' proprietary AMEX.™ Seven high level programming languages are offered which are CP/M or AMEX compatible.

Ideas aren't the only things growing at Altos. In three years over 4,000 field-proven microcomputer systems have been shipped worldwide to an ever-increasing customer base of over 300 companies. And recently a new facility has been acquired, expanding Altos' plot to over one-and-a-half acres of production facilities.

Weed through the microcomputer system alternatives. No matter what your application, you'll pick Altos.

For specific details about pricing or performance, call or write: Altos Computer Systems, 2360 Bering Drive, San Jose, CA, 95131, (408) 946-6700, Telex 171562 ALTOS SNJ.

Packed with Fresh Ideas

ALTOS
COMPUTER SYSTEMS

*CP/M is a registered trademark of Digital Research, Inc.
†OASIS is a registered trademark of Phase One Systems, Inc.

CIRCLE 7 ON INQUIRY CARD

CALENDAR

CONFERENCES

OCT 22 and NOV 18—Invitational Computer Conf, Breckenridge Inn at Frontenac, St Louis, Mo, and Hyatt Palo Alto, Palo Alto, Calif. INFORMATION: B. J. Johnson & Assoc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

NOV 4-6—MIDCON/80, Dallas Convention Ctr, Dallas, Tex. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

NOV 6-12—Electronica '80, Munich Fairgrounds, Munich, West Germany. INFORMATION: Franc D. Manzolillo, Rm 6015, U.S. Dept of Commerce, Washington, DC 20230. Tel: 202/377-2991

NOV 10-13—INTELCOM '80 (Internat'l Telecommunications and Computer Conf and Expo), Los Angeles Convention Ctr, Los Angeles, Calif. INFORMATION: Janet E. Schotta, Horizon House International, 610 Washington St, Dedham, MA 02026. Tel: 617/326-8220

NOV 11-13—Canadian Computer Show and Conf, Toronto, Ontario. INFORMATION: Canadian Information Processing Society, 243 College St, 5th Floor, Toronto, Ontario M5T 2Y1, Canada

NOV 11-14—Conf on Magnetism and Magnetic Materials, Dallas Hilton, Dallas, Tex. INFORMATION: D. C. Bullock, Texas Instruments, Inc, MS 974, Dallas, TX 75265

NOV 17-19—Asilomar Conf on Circuits, Systems, and Computers, Asilomar Conference Grounds, Pacific Grove, Calif. INFORMATION: A. M. Davis, Asilomar Conference, Dept of Electrical Engineering, San Jose State U, San Jose, CA 95192

NOV 19-21—GOMAC '80 (Government Microcircuit Applications Conf), Shamrock Hilton, Houston, Tex. INFORMATION: Larry W. Sumney, OUSDRE/E&PS, The Pentagon, Washington, DC 20301. Tel: 202/697-4198

NOV 19-21—COMDEX (Conf and Expo for Dealers, Distributors, and Reps), Las Vegas Convention Ctr, Las Vegas, Nev. INFORMATION: The Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 800/225-4620; in Mass, 617/879-4502

NOV 20-23—Northeast Computer Show, Hynes Auditorium/Prudential Ctr, Boston, Mass. INFORMATION: National Computer Shows, 824 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

NOV 30-DEC 4—NTC '80 (National Telecommunications Conf), Shamrock Hilton Hotel, Houston, Tex. INFORMATION: John R. Howell, Houston Lighting and Power Co, PO Box 1700, Houston, TX 77001. Tel: 713/228-9211, X3351

DEC 1-4—Internat'l Conf on Pattern Recognition, Konover Hotel, Miami Beach, Fla. INFORMATION: Harry Hayman, 5th Pattern Recognition, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

DEC 1-5—Symposium on Distributed Data Acquisition and Control, Miami Beach, Fla. INFORMATION: Dr Earl Swartzlander, Jr, TRW R3/2044, One Space Park, Redondo Beach, CA 90278

DEC 2-5—CMG XI (11th Internat'l Conf of the Computer Measurement Group), Sheraton-Boston Hotel, Boston, Mass. INFORMATION: Judith G. Abilock, Price Waterhouse and Co, Office of Government Services, 1801 K St, NW, Washington, DC 20006. Tel: 202/296-0800

DEC 4—California Computer Show, Hyatt-Palo Alto, Palo Alto, Calif. INFORMATION: Norm De Nardi, Norm De Nardi Enterprises, 95 Main St, Los Altos, CA 94022. Tel: 415/941-8440

DEC 8-10—Internat'l Electron Devices Meeting, Washington Hilton, Washington, DC. INFORMATION: Melissa Widerkehr, Courtesy Associates, 1629 K St, Washington, DC 20006. Tel: 202/296-8100

DEC 10-11—Computer Networking Symposium, Gaithersburg, Md. INFORMATION: Computer Networking, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

JAN 13-15—Communication Networks Conf and Expo, Albert Thomas Convention Center, Houston, Tex. INFORMATION: Terri Hamilton, The Conference Co, 60 Austin St, Newton, MA 02160. Tel: 617/964-4550

SEMINARS

OCT 1980-FEB 1981—Data Communications for Minicomputer Users, various U.S. cities. INFORMATION: Margaret Harveston, MICOM Systems, Inc, 9551 Irondale Ave, Chatsworth, CA 91311. Tel: 213/882-6890

NOV and DEC—Special Curricula on Data and Voice Technology, various dates and locations. INFORMATION: Systems Technology Forum, Inc, 8991 Cotswold Dr, Burke, VA 22015. Tel: 703/425-9441

NOV and DEC—Data Communications: Introduction to Concepts and Systems; Advanced Concepts and Systems; and Effective Network Design, various dates and sites. INFORMATION: Joe Menendez, Datapro Research Corp, Delran, NJ 08075. Tel: 609/764-0100

SHORT COURSES

OCT 1980-JAN 1981—Microprocessors: A General Introduction; Data Communications Concepts; and MCZ-2 Systems, various dates and locations. INFORMATION: Steve Blank, Zilog, 10340 Bubb Rd, Cupertino, CA 95014. Tel: 408/446-4666

NOV 17-19—Fundamentals of Data Communications (San Francisco, Calif) and Advanced Data Communications (New York, NY), INFORMATION: Ellen Sokol, American Management Associations, 135 W 50th St, New York, NY 10020. Tel: 212/586-8100

NOV 24-25—Protocols for Packet Switching: DEC 1-3—Software Design for Data Communications Systems; DEC 8-10—Packet Switching Networks for Data Communications; DEC 15-19—Structured Analysis, Design, and Testing of Computer Systems; DEC 17-19—Design of Digital Control Systems, George Washington U, Washington, DC. INFORMATION: Director Continuing Education Program, George Washington U, Washington, DC 20052. Tel: 202/676-6106

NOTICE

The Conference on Computer Graphics in CAD/CAM Systems, originally scheduled for Nov 3-5, 1980, has been postponed until Spring 1981. For details, contact Prof David Gossard, Dept of Mechanical Engineering, RM 3-445, MIT, 77 Massachusetts Ave, Cambridge, MA 02139. Tel: 617/253-4465

A NEW SERIAL PRINTER FROM THE LEADER IN MATRIX TECHNOLOGY

Mannesmann Tally sets the pace in price with the T1705.

From the Tally tradition of quality and reliability comes another dramatic advancement in lowered cost of ownership. A combination of low purchase price, low maintenance costs and low parts usage. A "no options" fully loaded printer that combines the latest in LSI electronics with precision mechanics. You get standard features that are extra cost options on other printers.

OEM's will select it because users will prefer it!

The T1705 is the quietest impact printer on the market. It has 160 cps optimized bi-directional printing with high speed 48 ips head slew for throughput speeds up to 200 lines per minute. Rugged reliability. No preventive maintenance requirements.

Standard features include a new operator changeable precision print head for long life and superb print quality. Dual tractors for positive paper positioning and control. Operator selectable 6 or 8 lpi spacing. Self test. Forms control. A convenient snap-in ribbon cartridge for clean, fast and easy ribbon changing. Double wide character printing. And a buffered serial interface.

A new serial printer. Competitively priced. 30 day delivery. Call your nearest Mannesmann Tally Sales outlet.

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Printers for the long run.

MANNESMANN TALLY

CIRCLE 8 ON INQUIRY CARD

Need advice on color graphics? Call ISC's toll-free hotline.

Make 1980 the year to improve your system with ISC's color graphics. You'll see the many advantages our terminals and desktop computers have over ordinary black-and-white models, because color conveys information faster and more effectively. ISC's color systems sell at black-and-white prices—starting at under $1,500. That's why ISC is the world's largest supplier of color graphics, with over 15,000 systems already in use.

If you're wondering how to update your system with color graphics, call **800-241-4310** and ask for Tom Landry, our System Support Manager. He'll give you the technical advice you need to make your conversion to color incredibly smooth. Or call your nearest ISC sales representative for a personal, "hands on" demonstration. Either way, you'll find out what our customers have known since 1973:

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Intecolor Drive ▪ 225 Technology Park/Atlanta ▪ Norcross, Georgia 30092 ▪ Telephone 404/449-5961 ▪ TWX 810-766-1581

Unretouched photos of screens.

LETTERS TO THE EDITOR

To the Editor:

I read with interest your article "Integer Base Conversion on Handheld Programmable Calculators" (May 1980, pp 202-207). I have used both the RPN and the AOS versions of the program in my school work. The RPN program performs as it should. However, the AOS program has an error that does not always affect the answer. Enter the AOS program and try the following:

	Enter	Press	Display	Comments
(1)	361100	A	0.	
(2)	8	B	10.	
(3)	16	C	114020316.	Wrong answer

The correct answer is 114020400.

Now edit the program as follows: GTO 36, LRN, 2nd INS, 2nd INS, 2nd INS, EE, INV, EE, LRN.

After editing the program, try the example above and you should get the correct answer. The three instructions that were inserted—EE, INV, EE—truncate the guard digits in the calculator. Since the TI-58/59 calculators use 13 digits to perform all calculations it is necessary to truncate the guard digits. TI-58/59 owners may consult pages C-1 and D-3 of their Personal Programming manual for a complete discussion of the guard digits and displayed results versus accuracy.

Congratulations on an excellent article, and an outstanding magazine.

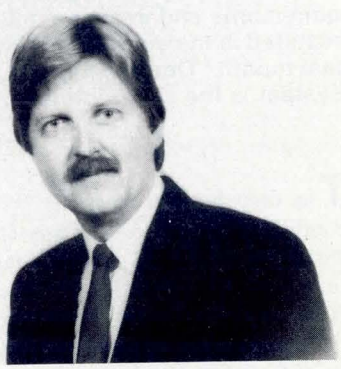
Ronny Horn
Meridian, Mississippi

To the Editor:

Douglas Raymond, in his otherwise excellent article on the testing of digital circuit boards (Apr 1980, pp 129-137), indicates in Fig 2 that 16 input combinations are required to test the 3- to 8-line encoder. Actually, however, only eight input combinations are required. Therefore, the output signature lengths can be cut in half, since half of the 16 states shown in the figure are redundant.

Richard I. Lewis
Lear Siegler, Inc
Santa Monica, Calif

***COMPUTER DESIGN* ADDS NEW FIELD EDITOR**—Douglas A. Eidsmore has joined *Computer Design* as a Field Editor for Northern California and the Northwestern states. A resident of San Jose, Doug has been associated with 'Peninsula' firms as a contract technical writer and editor. While with Serafini Associates and Info 3, he designed and wrote high technology training courses and promotional material for companies such as American Microsystems, TRW-Vidar, and Monolithic Memories, and edited an instructional course on software systems for Digital Equipment Corporation. Previously he worked as an engineer for FMC and McDonnell-Douglas, and he is the designer/inventor of several microcomputer based educational simulations. Doug received an MS degree in Cybernetic Systems from San Jose State University and a BS degree in Mechanical Engineering from California State University at Northridge. (Mike Chester now is Field Editor for Southern California and the Southwestern states.)



A DISTRIBUTED PROCESSING SYSTEM FOR MILITARY APPLICATIONS— PART 2: THE SERIAL DATA BUS

Ralph Mauriello

Litton Data Systems
8000 Woodley Ave, Van Nuys, CA 91409

An internal research and development study defined the requirements of a distributed processing system that would satisfy those types of U.S. military command, control, and communication systems designed and delivered by Litton Data Systems. Review of the requirements and implementation of a responsive design resulted in the distributed processing system described last month.[1] One key to the successful operation of this system is the serial interelement bus.

The distributed processing system serial interelement bus combines current technology in communications circuitry with a modified IBM synchronous data link control[2] protocol to provide a bus for militarized systems. It features 20M-bit/s serial data, dual loop redundancy, reassignable bus controller, multiple addressing modes, and automatic reconfiguration.

Objectives and Approach

Design considerations for the serial interelement bus (SIB) are given in the Panel, "Bus Architecture Considerations." Partitioning of system data processing and system data base is the key factor in determining the required speed for supporting data transfer needs. Several existing and proposed

Bus Architecture Considerations

Support Data Transfer Requirements
- Determine speed required
- Minimize overhead
- Guarantee access to all users
- Minimize bus access delays
- Minimize staleness

Fail-Safe Capability
- Bus controller capability at every node
- Distributed bus access logic
- Redundancy at card, node, and bus levels
- Alternate routing over multiple buses without requiring complex online routing algorithms

Bus Media Requirements
- Fiber optics (200 m max between each bus node pair)
- Coaxial cable (200 m max between each bus node pair)

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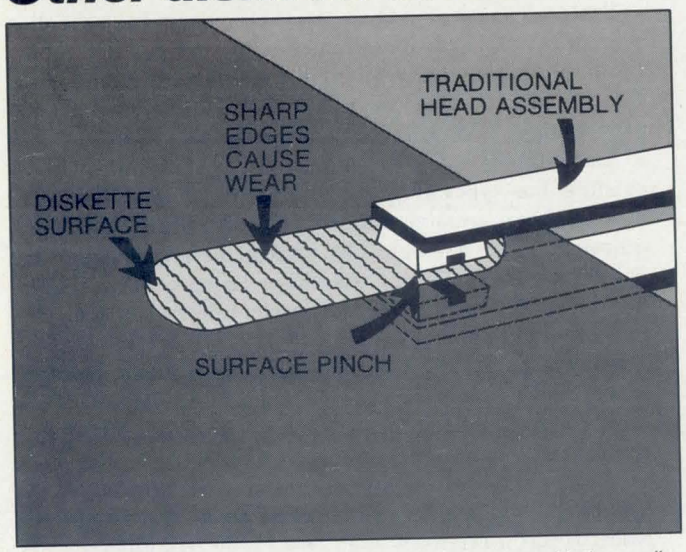
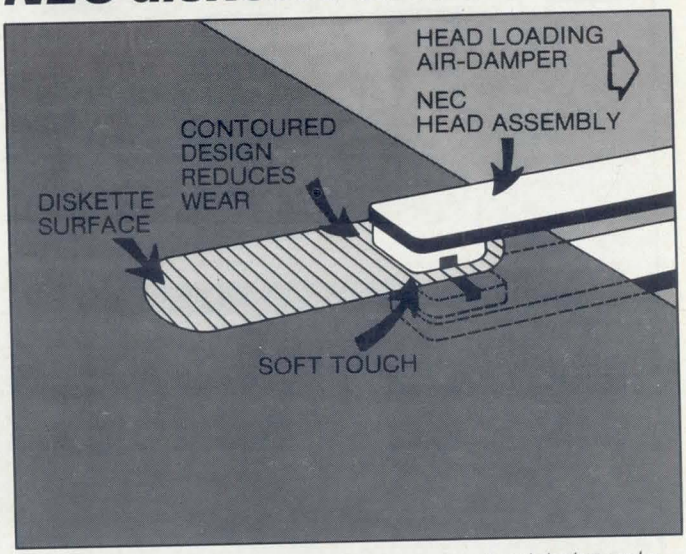
Other diskette drives



Dual-sided diskette drives require contact of both heads with the media to read or write. This causes head wear and a pinching action that deforms, mars and scratches the media surface, shortening head and media life.

NEC diskette drive



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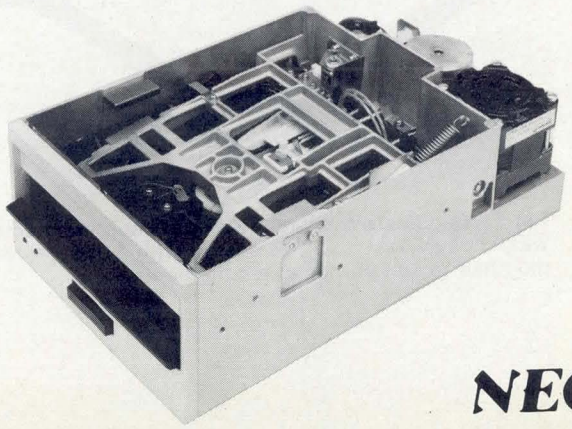

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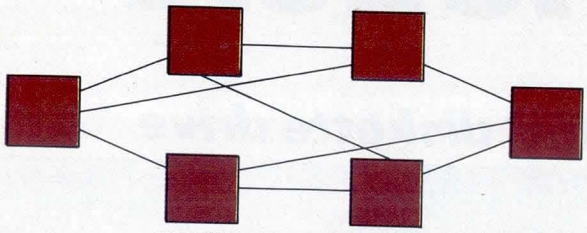
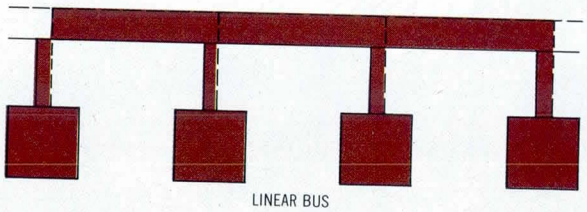
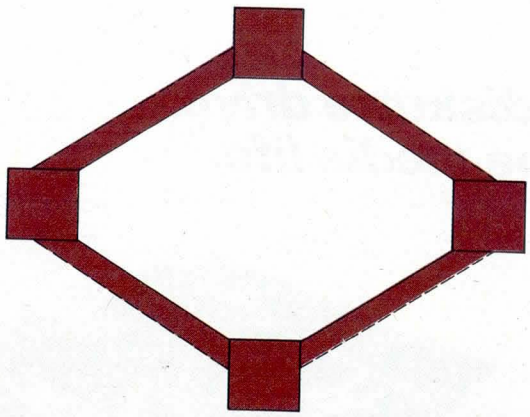


STORE AND FORWARD OR PACKET NETWORK



LINEAR BUS



RING OR LOOP

Fig 1 Candidate bus architectures. Loop architecture was chosen for basic SIB design with SDLC protocol modified to suit particular requirements

centralized systems were conceptually redesigned using distributed processing concepts. Expected traffic on the bus was then analyzed for these systems, one of which needed a 7.6M-bit/s rate. A 20M-bit rate was selected as the maximum that could be currently achieved consistent with conservative design and high integrity data transmission.

Prior to implementation, several existing bus approaches were evaluated. Criteria applied to the evaluation were maximum utilization of selected bandwidth, autonomous user access (no central polling), minimization of contention and guaranteed access by all users, continued operation following a variety of failure modes at system and subsystem level, and ability to isolate and test subsystems concurrent with continued system operation.

Protocol must maximize bus efficiency by providing minimum overhead. Requirements for survival dictate that bus operation be independent of a single master unit or station and that the bus system be redundant and self-healing after failures and/or battle damage.

Evaluation showed that none of the most promising of the existing bus types (Fig 1) satisfied all of the established criteria. Loop architecture came closest to fulfilling the requirements for a single bus system, and was, therefore, chosen as the basis for SIB. Very large systems require multiple buses; in these cases, a combination of loop and packet architecture is used.

However, even the best implementation of the loop bus synchronous data link control (SDLC) protocol has shortcomings. There is a fixed master-slave relationship based on a centralized control concept. A slave cannot transmit directly to another slave; all such messages must be relayed via the master, thus all slave to slave messages appear on the bus twice. It has a relatively high cost cyclic redundancy code, and there is no protection from single-point failures.

In design, the SDLC loop architecture has been modified to compensate for the deficiencies mentioned above. There is provision for distributed control by having reassignable bus controller capability at any node; there is direct point to point addressing for all nodes; a modulo 2^{16} checksum word is used; and there is dual loop redundancy for each bus.

Design Features of the SIB

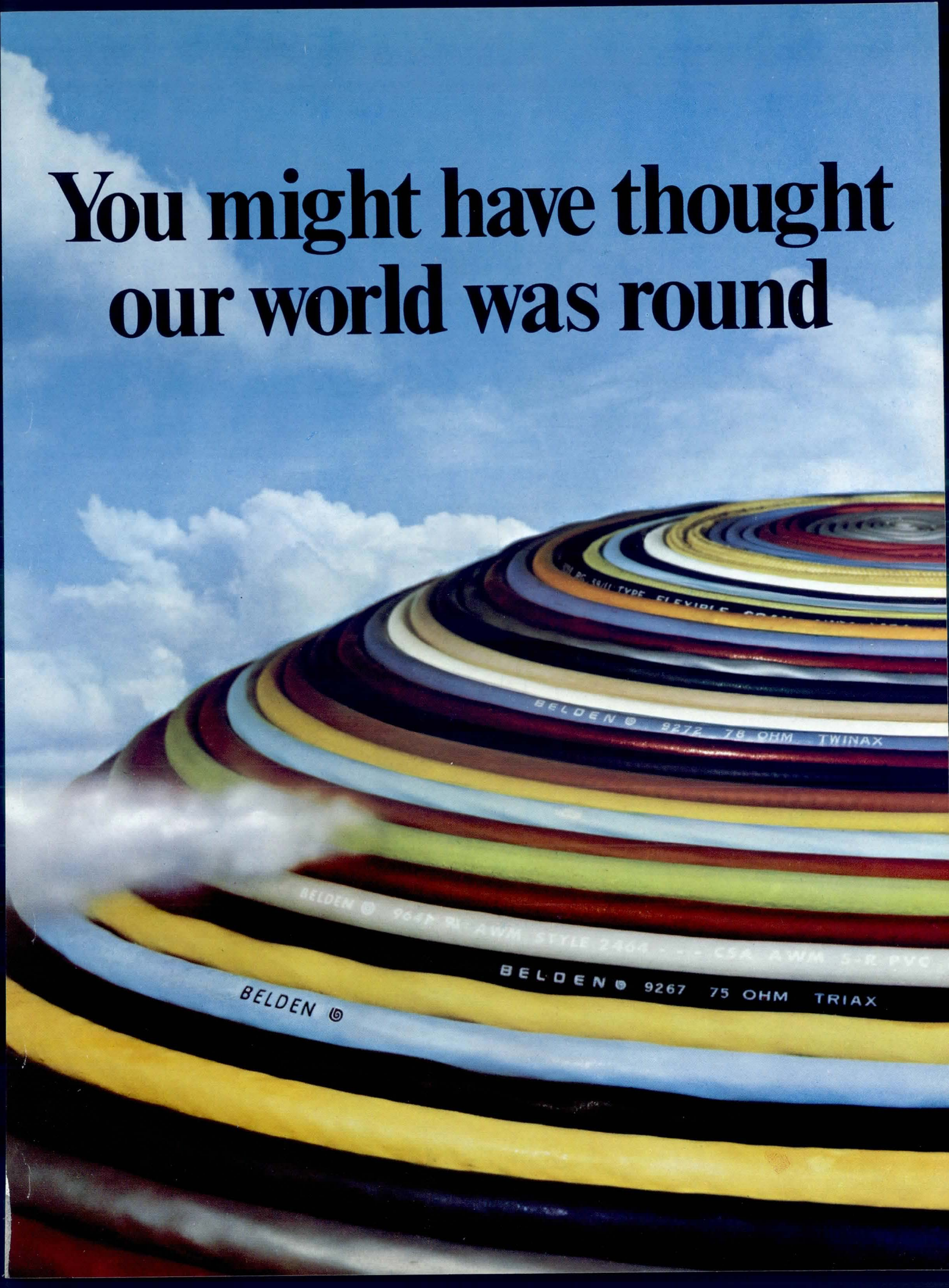
Key features of the Litton SIB design that optimize its use for command, control, and communications (C^3) distributed systems are the reassignable bus controller, dual loop redundancy, automatic reconfiguration, and distributed bus access logic. These attributes eliminate a system single-point failure.

A combination of hardware, firmware, and software implements the reassignable bus controller capability. The bus controller is initially assigned by software, determined by which node actually executes the system bootload function; any node having bootload media can do this. However, to ensure that a single node failure will not halt system operation, the bus controller function must be reassignable. Therefore, once the bus controller has been assigned, its first duty is to assign a backup controller that will take over this function should the primary fail or be removed from the system.

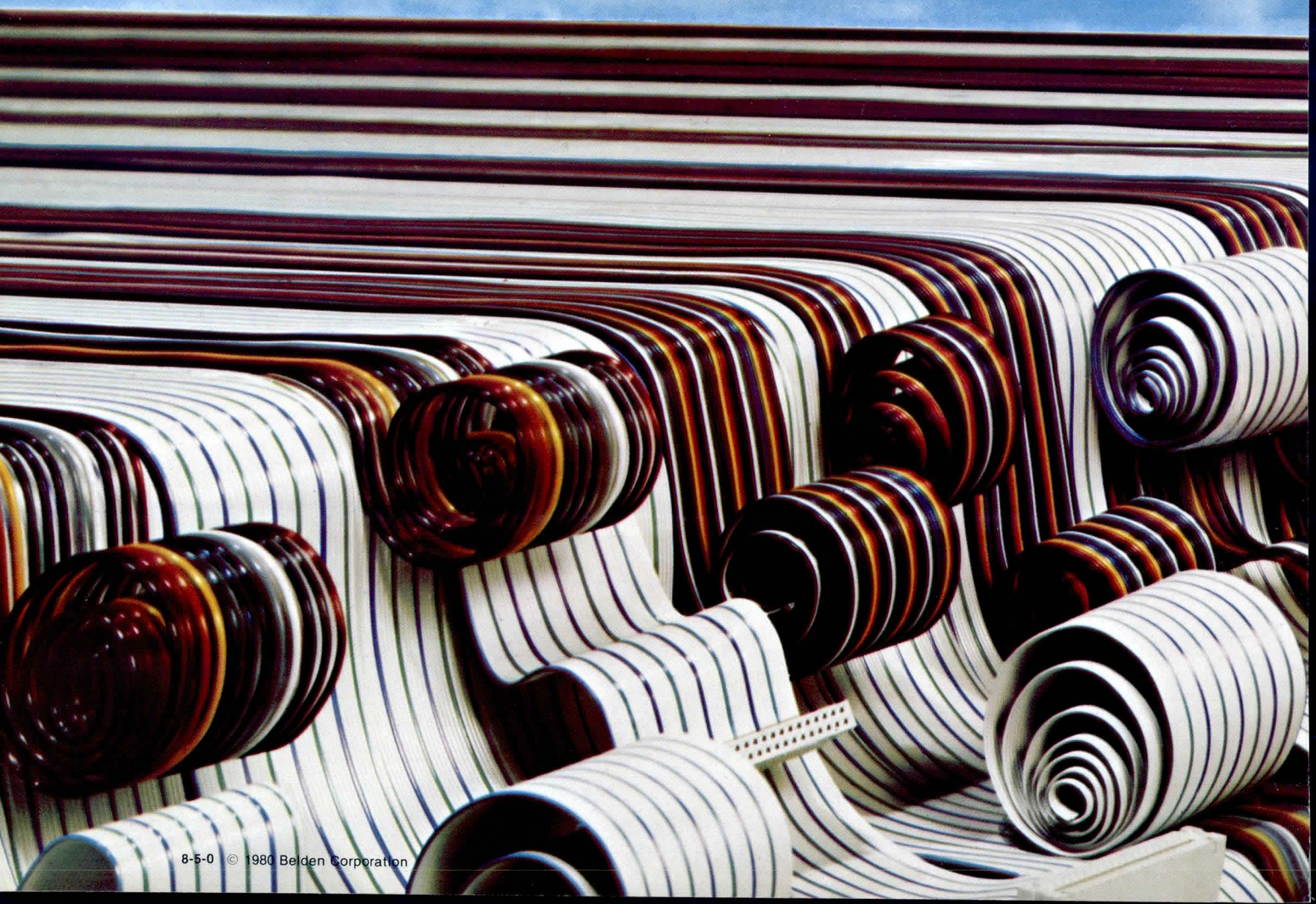
Failure of nodes not at the bus controller are easily detected, and those elements adjacent to failed elements

(continued on page 21)

You might have thought our world was round



Think again.



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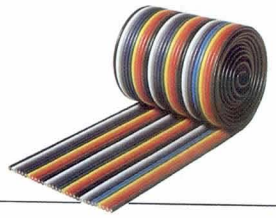

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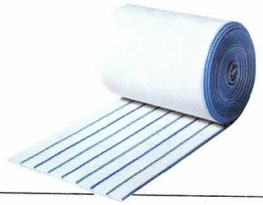

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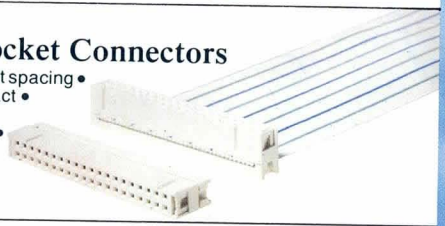
• .100" (2.54mm) contact spacing • Double-cantilever contact • Bottom-entry contact • Many diversifications (10 to 60 pins, closed-end/through-end) • Dual-beamed contacts • Polycarbonate strain relief

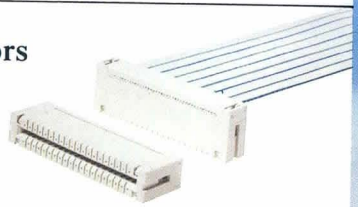
Low-profile Socket Connectors

• .100" (2.54mm) contact spacing • Double-cantilever contact • Bottom-entry contact • Dual-beamed contacts • Many diversifications (10 to 60 pins)



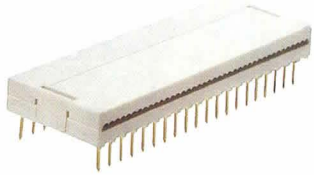
Card Edge Connectors

• .100" (2.54mm) contact spacing • Bifurcated contacts • Many diversifications (10 to 60 pins; with ears, half ears or without ears; and with or without strain relief)



D.I.P. Connectors

• Plugs into IC sockets or can be soldered for permanent connections • Low-profile installation on PC board • Many diversifications (10 to 60 pins)



P.C.B. Transition Connectors

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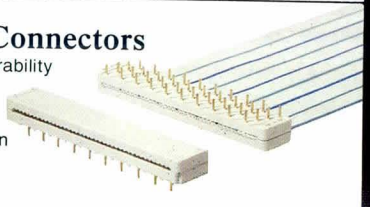

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automatically switch the failed node out of the link. Appropriate information is provided to the bus controller and to the system control operator.

Direct addressing of a message from one nonmaster node to another is also a feature requiring SDLC protocol modification because of the SDLC centralized control concept. In the Litton distributed processing system (DPS), all elements or nodes have processing capability; therefore, a bus design that enables efficient slave to slave transmission is required. The SIB protocol eliminates the double transmission store and forward approach characteristic of unmodified SDLC by permitting direct addressing by any node to any other node(s).

Design also provides four address categories that may be recognized by the nodes connected to the SIB.

Global—All nodes will accept the message (broadcast).

Device collective—All nodes of a given type (such as display nodes or antisubmarine warfare nodes) will accept the message. Six types have been defined, and one node may be specified as more than one type.

Unique—Only the addressed node will accept the message.

Bus controller—Only the active controller will accept the message.

This large set of address categories maximizes bus throughput. The global and device collective categories permit a single transmission of a message to multiple destinations, another major departure from SDLC protocol.

Two transmission media, fiber optics and coaxial cable, permit cost-effective implementation for a wide variety of applications. Design of the nodes allows implementation of the bus in any combination of the two media. Transmit/receive (T/R) assemblies of the node have been modularly designed to permit this choice at any location in the loop.

Finally, a true DPS requires system bootload and the capability for remote bootloading. System bootload permits programs to be automatically loaded and distributed to all system elements from a single mass storage device. Remote bootloading permits the bootloading of any node that is being added or reinserted into the system from one mass storage device. This eliminates the need for bootload media at every element.

SIB Transmission Format

While simultaneously providing four different addressing methods to maximize bus efficiency, the SIB transmission format makes excellent use of the available bandwidth by minimizing the number of overhead bits and characters required to accomplish data communication. Transmission format for the SIB is shown in Table 1. The go-ahead, start/stop flags, inserted zeros, and error control word are the only nondata bits required by the system, resulting in excellent bus efficiency.

Access to the SIB is provided by a go-ahead pattern, a zero followed by seven consecutive ones, that is initially issued by the current bus controller, and indicates that the bus is available for transmission. Each of the nodes determines bus availability for itself by sampling for the go-ahead pattern, thereby eliminating polling and distributing the bus access control logic. This makes it virtually immune to many possible SIB failures.

(continued on page 26)

TABLE 1

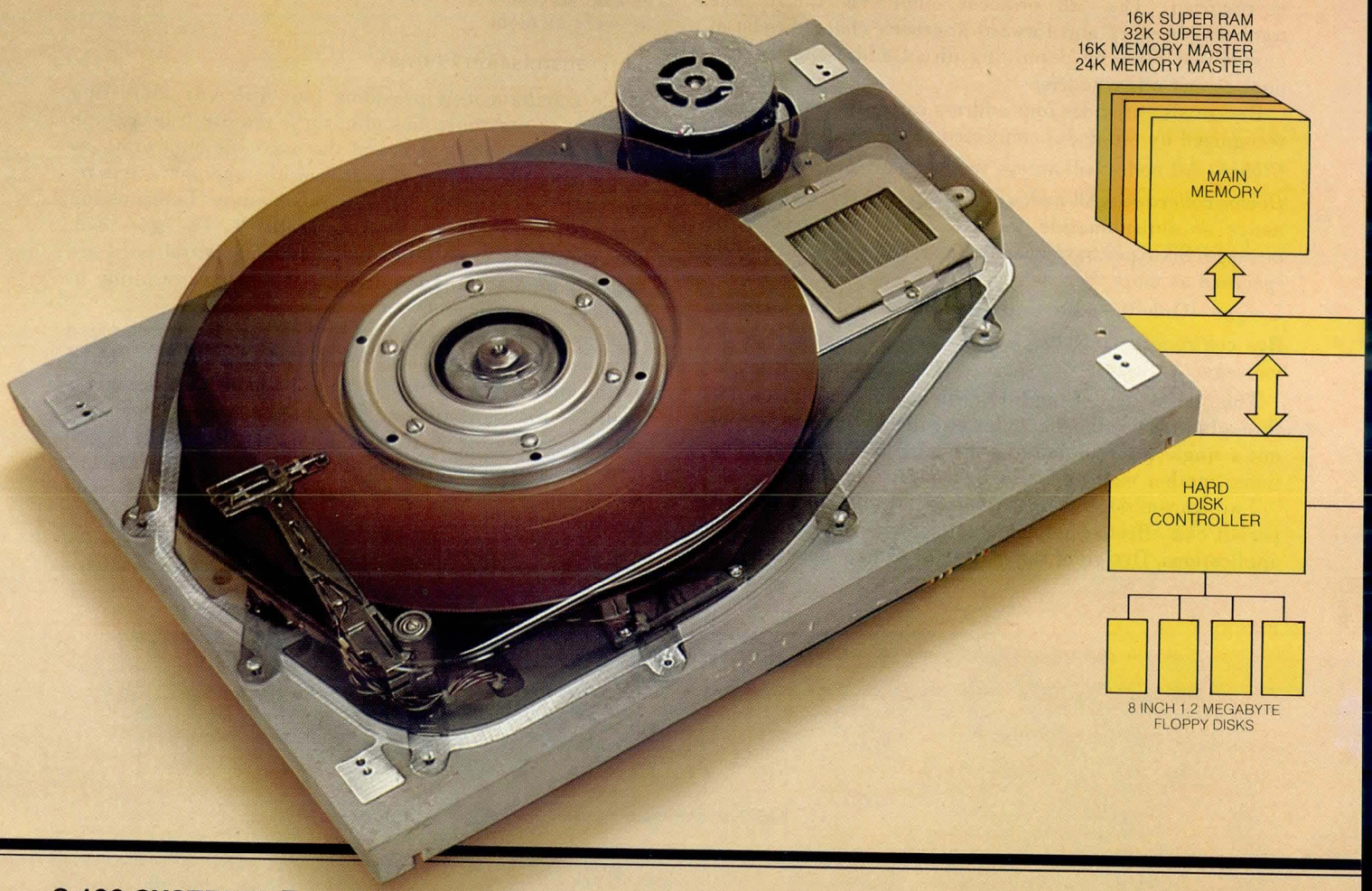
SIB Transmission Format

Go-ahead (Flag)*	Flag (F_O)	A_T	C_1	C_2	A_F	ML	Information	EC	Flag (F_E)

	Field	Length	Comments
	Go-ahead (flag)	8 bits	0 1 1 1 1 1 1 1
F_O	Opening flag	8 bits	0 1 1 1 1 1 1 0
A_T	Destination address	8 bits	See Address table (Table 2)
C_1	System control	8 bits	See Control table (Table 2)
C_2	User control	8 bits	System software
A_F	Source address	8 bits	See Address table
ML	Message length	16 bits	Number of words in message
I	Information	0 to 4092 words	No format restrictions on software
EC	Error check	16 bits	Module $2^{16} - 1$ sum of all words after F_O
F_E	Ending flag	8 bits	0 1 1 1 1 1 1 0

*Converted to flag pattern by SIB interface card

While they were thinking hardware and software, we were thinking



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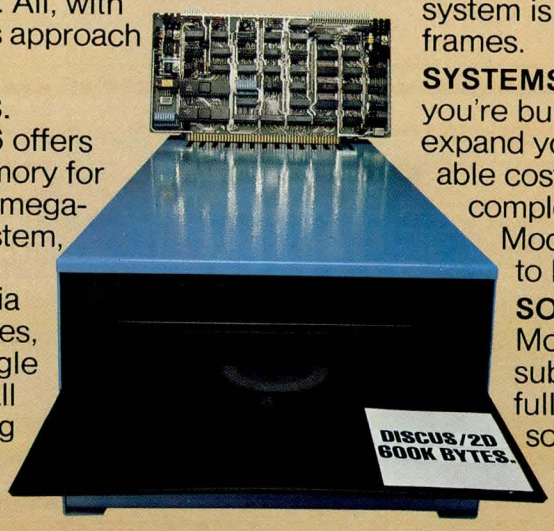

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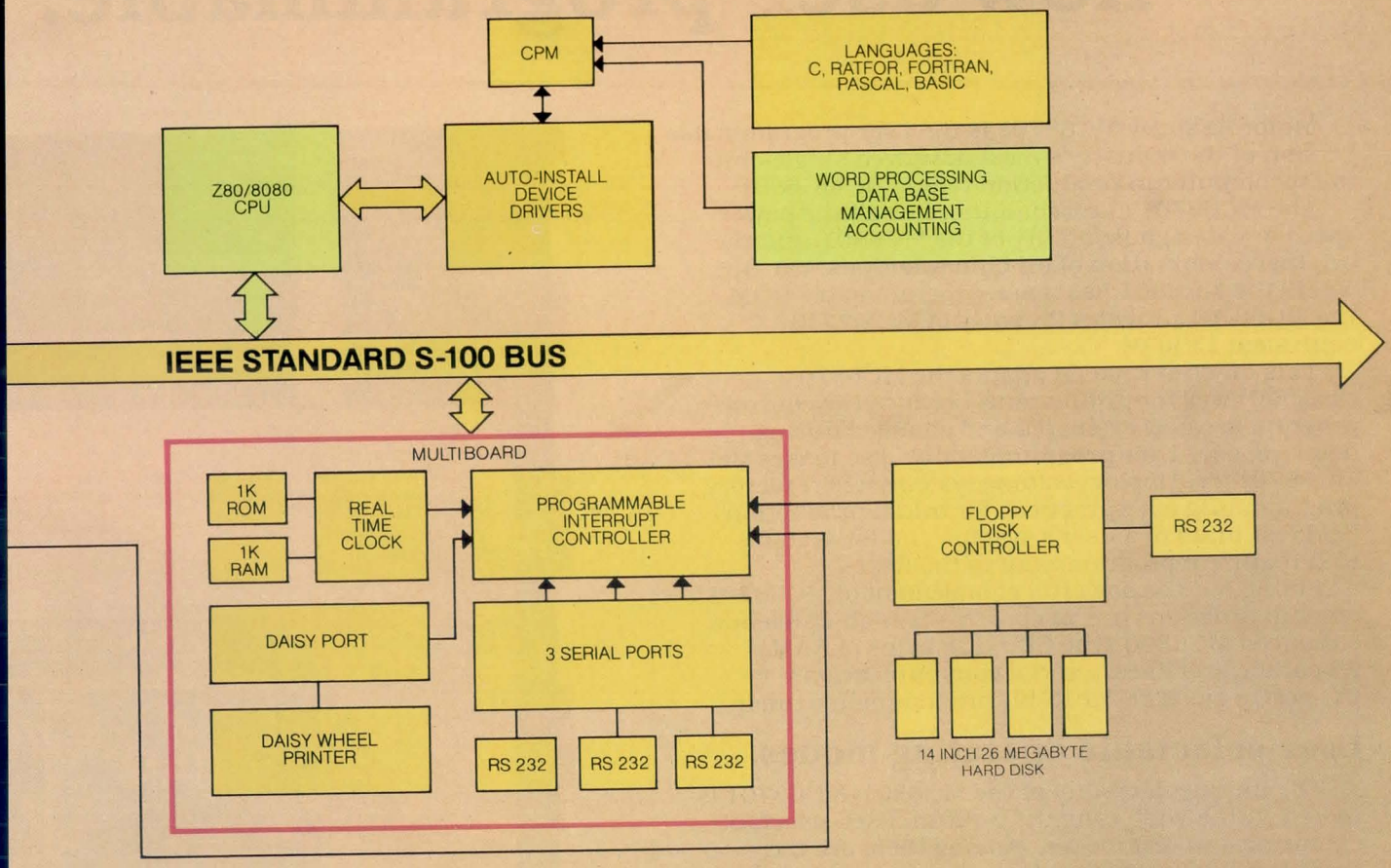

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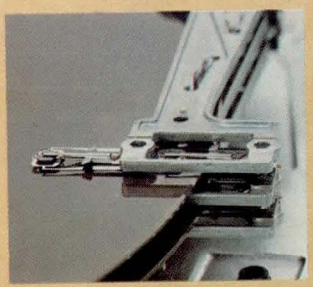

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Filling out the powerful complement of MC68701 on-chip functions are, of course, the high-efficiency, enhanced MC6800-type CPU, 128 bytes of RAM, 29 parallel I/O lines, a serial communications I/O port, a clock and a 16-bit programmable timer.

User-selectable operating modes.

The unique flexibility of the MC6801-MC68701 is rooted in the wide range of built-in, user-selectable operating and test modes. Among them are the three basic operating modes.

In the single-chip mode, all ports are configured for I/O-29 I/O and two control lines. The expanded multiplexed mode enables an impressive 64K-byte addressing capability. And, in the expanded non-multiplexed mode, no external logic is required to directly address 256 external locations, including any and all M6800 Family peripherals. Thirteen to 20 I/O lines are still available.

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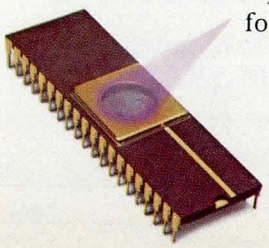
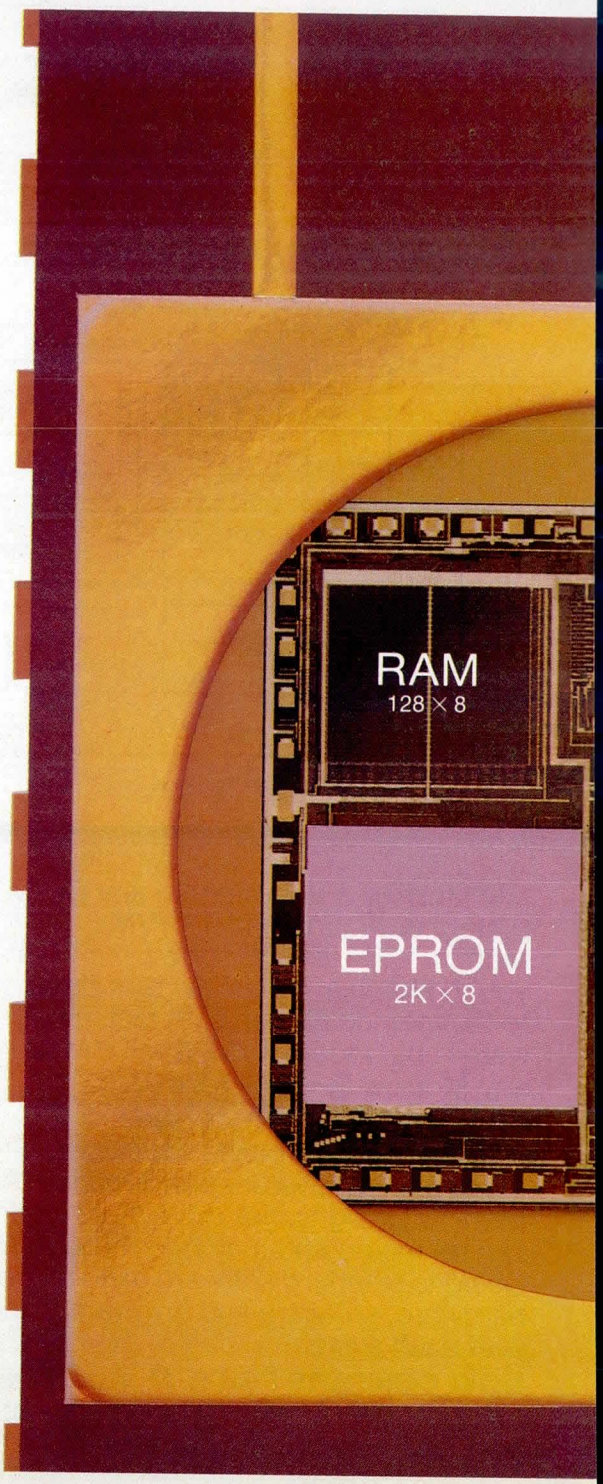
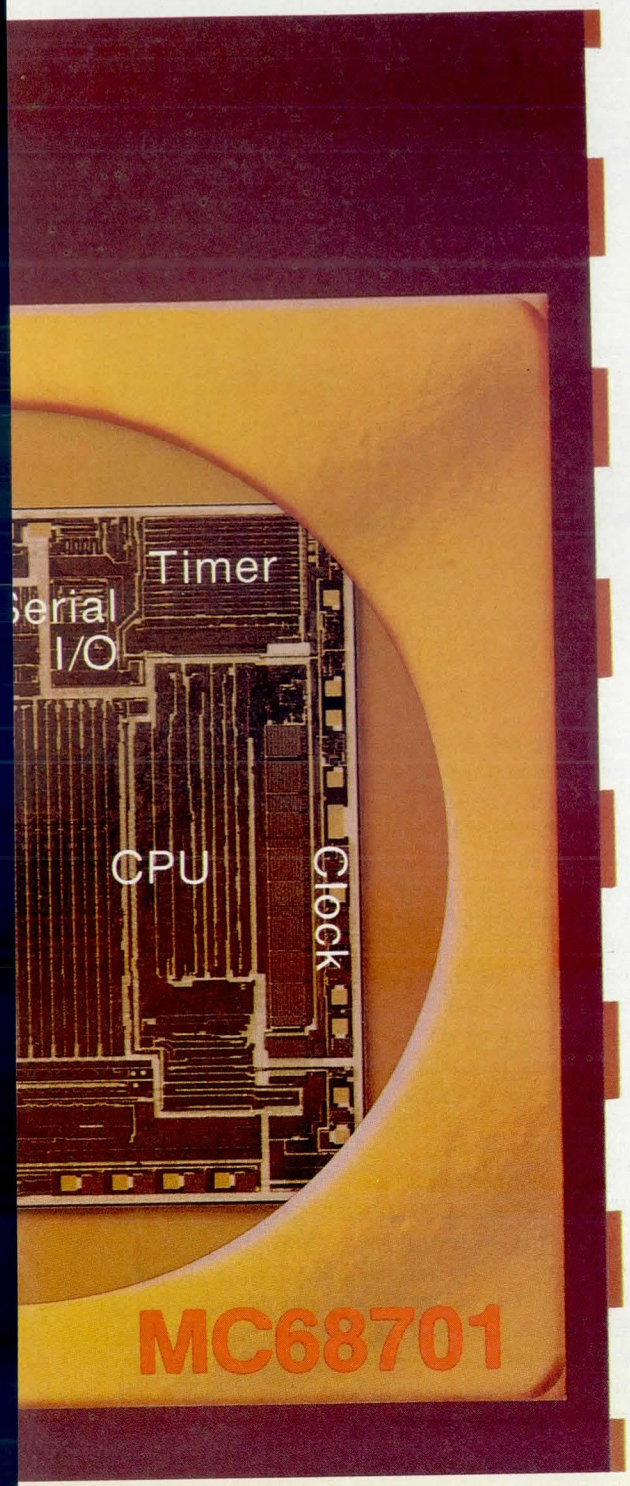




chip microcomputer is Motorola's MC68701.



The MC6801-MC68701 CPU is an enhancement of the highly-capable MC6800 which puts seven addressing modes at the designer's disposal. An MC6800 machine-code-compatible instruction set is expanded by 16-bit instructions, including a 10 μs hardware multiply. Execution time of most instructions has been reduced by reducing the instruction cycle count to increase throughput.

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TABLE 2

Address and Control Field Formats

Address Field

Bit		Definition
	7 6 5 4 3 2 1 0	
	x x x x x x x x	1 of 192 unique addresses selected from front panel Address Select switch where B_6 and B_7 may be any value but 1, 1
	1 1 x x x x x x	1 of 6 device collective addresses selected by backplane wiring
	1 1 0 0 0 0 0 0	Bus controller dedicated address

Control Field

Bit		7	6	
7, 6	Request/response codes as shown	1	1	Request from bus controller
		1	0	Request from non-bus controller
		0	1	Response to bus controller
		0	0	Response to non-bus controller
5	Long/short form: 1 = long, 0 = short			
4	Interim/final: 1 = interim, 0 = final			
3	With/without data: 1 = with, 0 = without			

2	1	0	
0	0	0	Message for firmware
0	0	1	Task request
0	1	0	Wilco
0	1	1	Unshunt
1	0	0	Cantco
1	0	1	Spare
1	1	0	Haveco
1	1	1	Spare

Bits 2, 1, 0: Coded as shown

When a message is available for transmission, hardware detects the go-ahead pattern and converts it to a flag. Therefore, each message has two 8-bit start flags and one 8-bit closing flag. In order to prevent these combinations from appearing within the message itself, the SIB interface card automatically inserts zero bits into the message following any string of five consecutive one bits. Zeros are automatically stripped out at the receiving SIB interface card.

Messages (data between the flags) may range in length from 4 to 4096 words depending on system requirements. The first 8 bits are always the TO address, the next 16 are control bytes, and the following 8 bits are a FROM address. Address field and control field formats are defined in Table 2. A 16-bit field message length (ML) defines the word count of the message which includes all words between beginning and ending flags (a word is 16 bits). A checksum follows the data and precedes the closing flag.

Under software control, the information field in the current design may range from zero to a maximum of 4092 words; however, system design considerations may dictate a shorter maximum length message. In addition, hardware in the SIB interface card limits the maximum message length to 4 ms in order to prevent software/hardware errors from surfeiting the bus with a continuous transmission.

Current software design permits up to 64-byte messages, which comprise the majority of messages, to be sent without requesting permission from the receiving node. With longer messages, a request must be sent first to assure that buffer space is available in the receiving node(s). The maximum length message is dependent upon system design requirements and should be established during the system design phase.

Acknowledgments for received messages, requests to send, permission to send, and several system control messages all make use of the control field in the message header to convey the required information. These dataless messages further serve to improve loop usage efficiency.

SIB Operating Characteristics

Bus controller functions. Because it is handling the program bootload for the system, the bus controller is responsible for establishing bus operations and resetting all nodes during start-up. The bus controller also periodically checks the status of all nodes on the bus. Major function of the bus controller is to provide clock synchronization for the loop, issue the initial go-ahead pattern, and ensure that a go-ahead is always present in the loop.

(continued on page 30)

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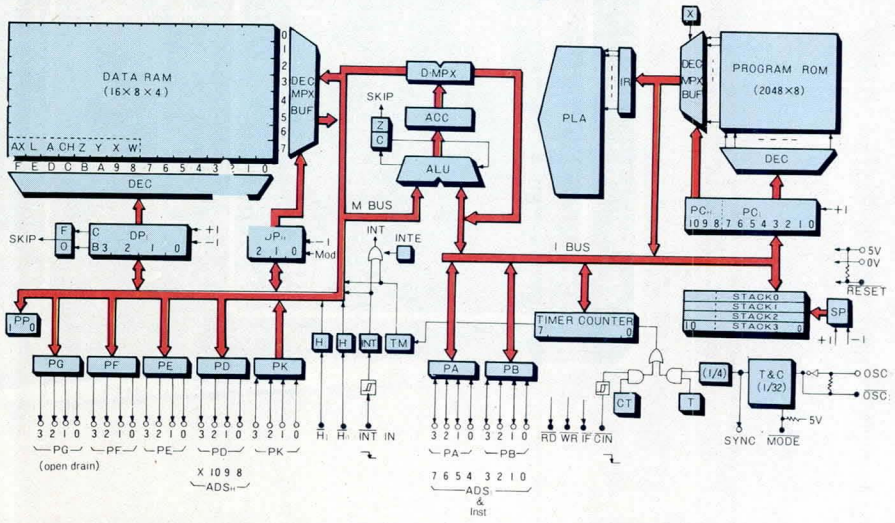

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MSM5845RS	MCU, 49 instructions, 1280x8 ROM, 64x4 RAM.
MSM58421GS	MCU, 52 instrcns, 1536x8 ROM, 40x4 RAM. 5-digit LCD driver.
MSM58423RS	MCU, 52 instrcns, 1280x8 ROM, 32x4 RAM, 12x12 matrix VF driver.
MOS EPROMS	
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MSM2732AS	4096x8 UV erasable, electrically programmable PROM.
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MSM5114RS	1Kx4 low power static RAM.
MSM5115RS	1Kx4 low power static RAM.
CMOS I/O PRODUCTS	
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MSM58281RS	Display driver, 4 digit VF.
MSM58282RS	Display driver, 4 digit VF/LED.
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MPB201	PC board emulator Series 40 MCU operation.
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MPB203	PC board provides MPB201 with EIA interface, 20MA loop interface or TTL compatible interface.
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SDP40-S	OKI Series 40 program dev pment package, stand-alone.
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MPSP-C	Evaluation boards, softwa. omplete User's Manuals — CP/M®.
MPSP-S	Eval. boards, software, complete User's Manuals — stand-alone.
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OLMS 42	MSM5842 Users Manual
OLMS 45	MSM5845 Users Manual
OLMS 421	MSM58421 Users Manual
OLMS 423	MSM58423 Users Manual
MPB 201/203	MPB201 & MPB203 Users Manual
MPB 202	MPB202 Users Manual
MPSP-I	SDP40-I Users Manual
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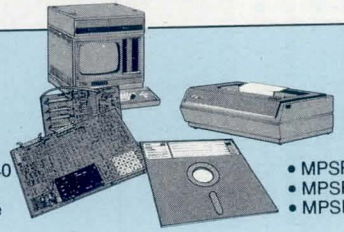

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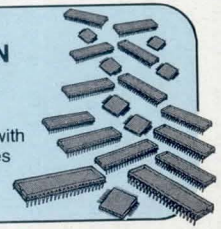

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CIRCLE 13 ON INQUIRY CARD

Transmission. Message transmission is achieved without intervention of the system bus controller. All messages sent by any node to any other node(s) are addressed directly and proceed directly to the addressees, and acknowledgments are sent directly to the addressors. As each node sees the go-ahead pattern go by, it has the opportunity to insert its message on the bus. When it does, it changes the go-ahead pattern to an opening flag, signaling the start of its message. At the end of its transmission, the node appends the closing flag and a go-ahead pattern to allow other nodes in the loop to transmit. Access to the bus is guaranteed to all nodes as each message proceeds around the bus. No node has the bus for transmission of more than one message at a time and the go-ahead pattern is constantly and automatically moving from one node to the next. There is no time lost for nodes that have no messages to place on the bus, as occurs in a time division multiplex system.

Reception. As messages move around the loop, each node looks for its unique, group, or global address to determine whether or not the message is for this node. The bus controller node also looks for the dedicated bus controller address. If the message is for the node, it is stored in memory at the node and a processor within the node is informed. In any event, the message continues around the loop until it is returned to the sending node, where it is stripped from the bus. Nodes in the loop, therefore, act as repeaters rather than as store and forward nodes.

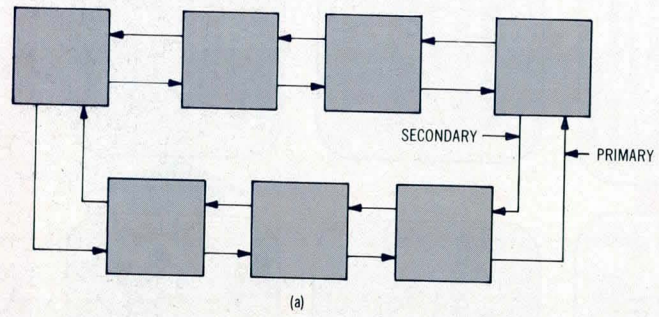
SIB Reconfiguration Characteristics

Automatic reconfigurability provides for a highly fault tolerant design. For a single bus, single failures are handled without loss of capability; continued operation at reduced capability is permitted with multiple failures. Multiple buses can sustain multiple failures without degradation.

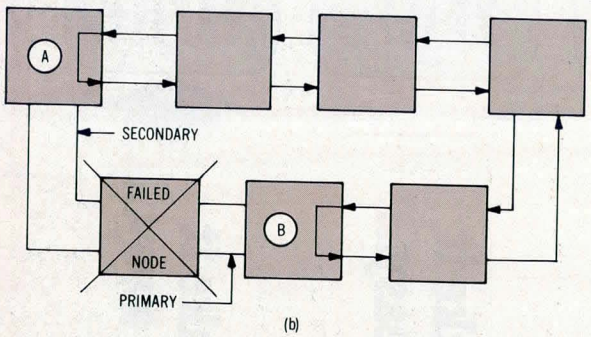
The SIB is implemented in a dual loop configuration as shown in Fig 2(a). Information transfer on the primary and secondary loops is in opposite directions and the loops are completely independent of each other. In normal operation, the primary loop is used for data transfer while the secondary loop carries a predefined idle pattern. This technique allows each node in the loop to constantly monitor the status of both primary and secondary loops. A failure of either loop (loss of signal/synchronization) will be detected and the bus automatically reconfigured as in Fig 2(b). There are two methods of reconfiguration control, hardware or software. If hardware, the appropriate paths are connected and software is notified of the action taken. If software, the loss of signal information is passed back to the processor for a software controlled reconfiguration.

In reconfiguring the bus as shown in Fig 2(b), both adjacent nodes detect the loss of incoming information. Node A loses the idle pattern and node B loses the data. Hardware or software within nodes A and B will close a path that connects the primary loop to the secondary. This causes data to

(continued on page 34)



(a)



(b)

Fig 2 Dual loop redundancy (a) and automatic reconfiguration (b). Both combine to prevent a single-point system failure

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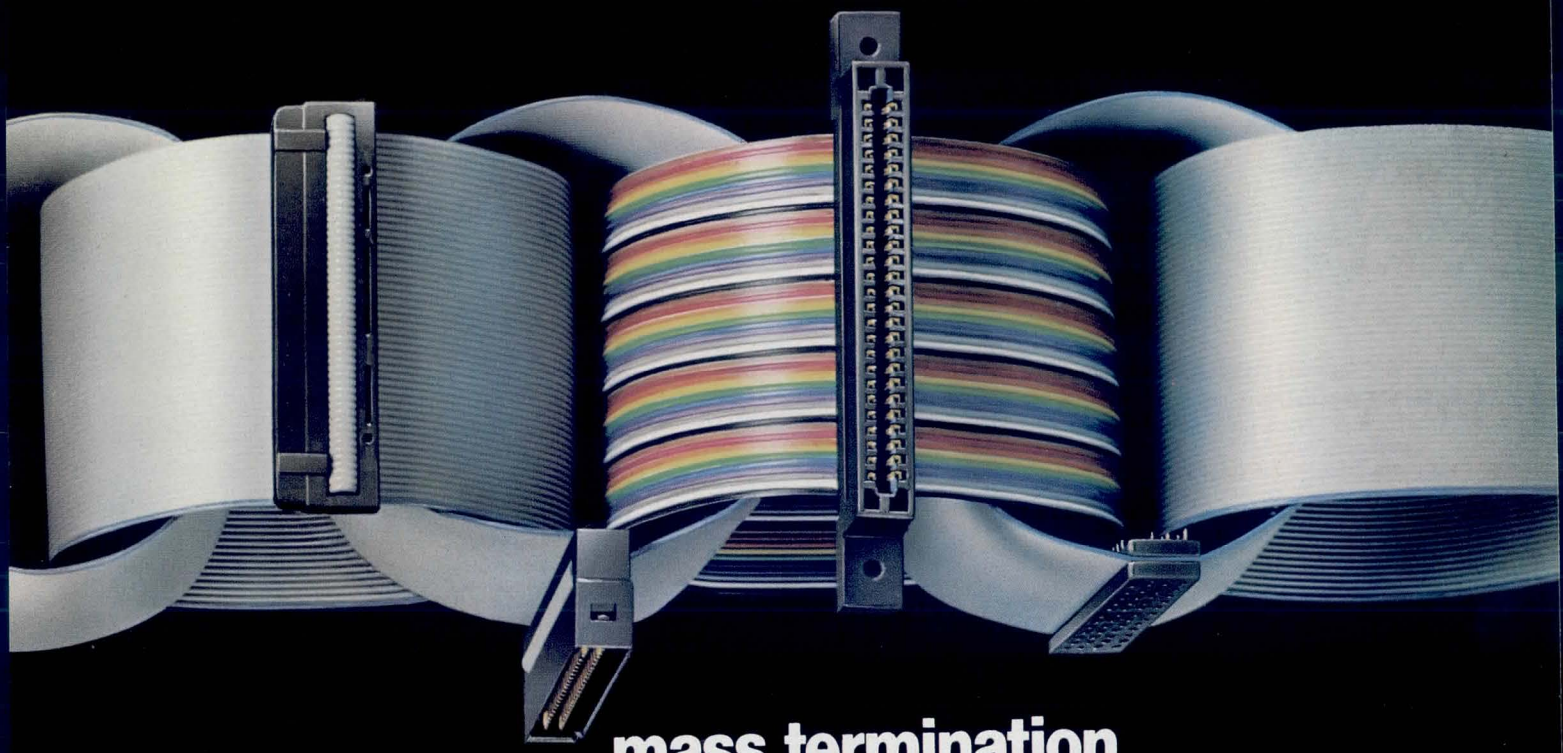

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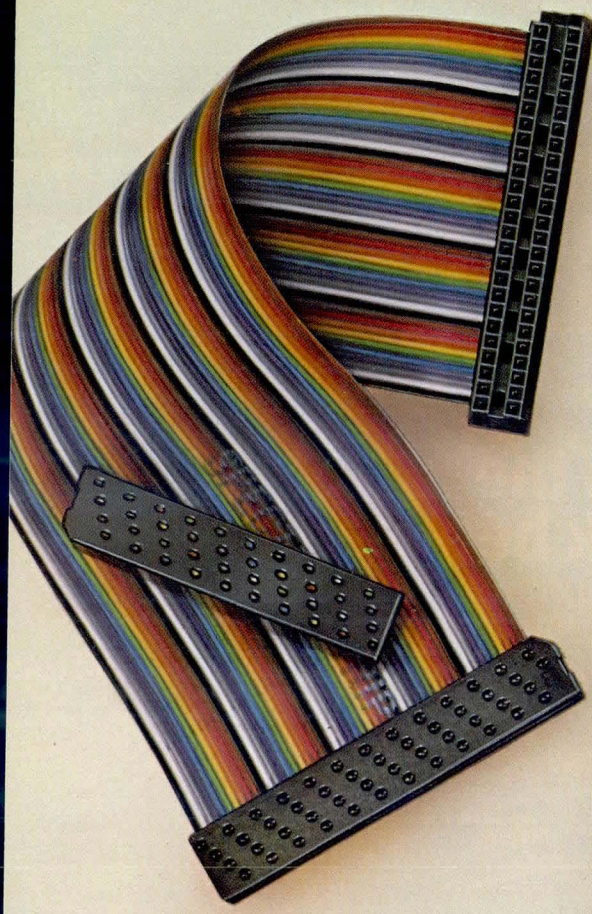

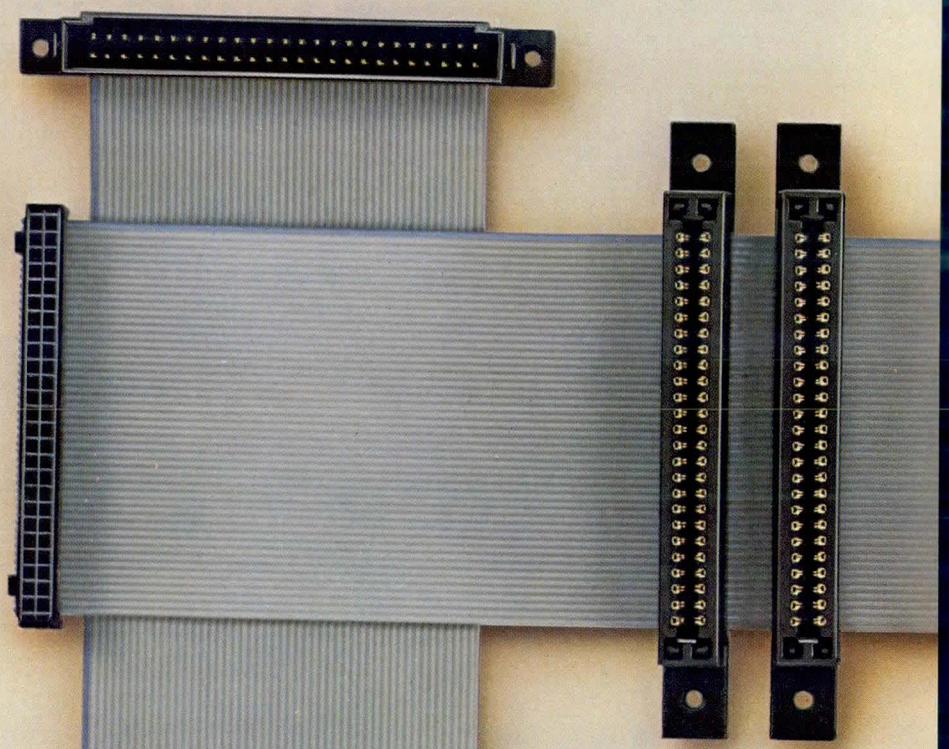

AMP Latch connectors.

Available in cable-to-cable, card edge, DIP and receptacle styles, each works with twisted pair, ribbon or bonded cables. And all are intermateable with a full range of headers, including right-angle, feed-through and barrier types. To complete a truly versatile, expandable system, they are compatible with discrete, flat flex, coaxial and transmission cable connectors.

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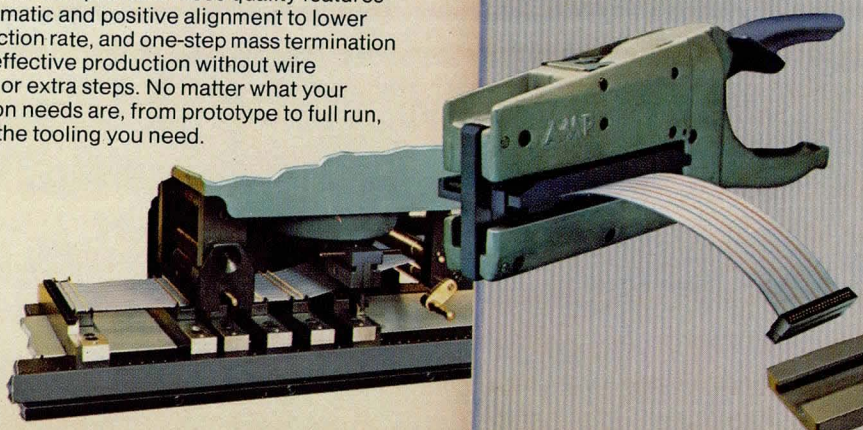

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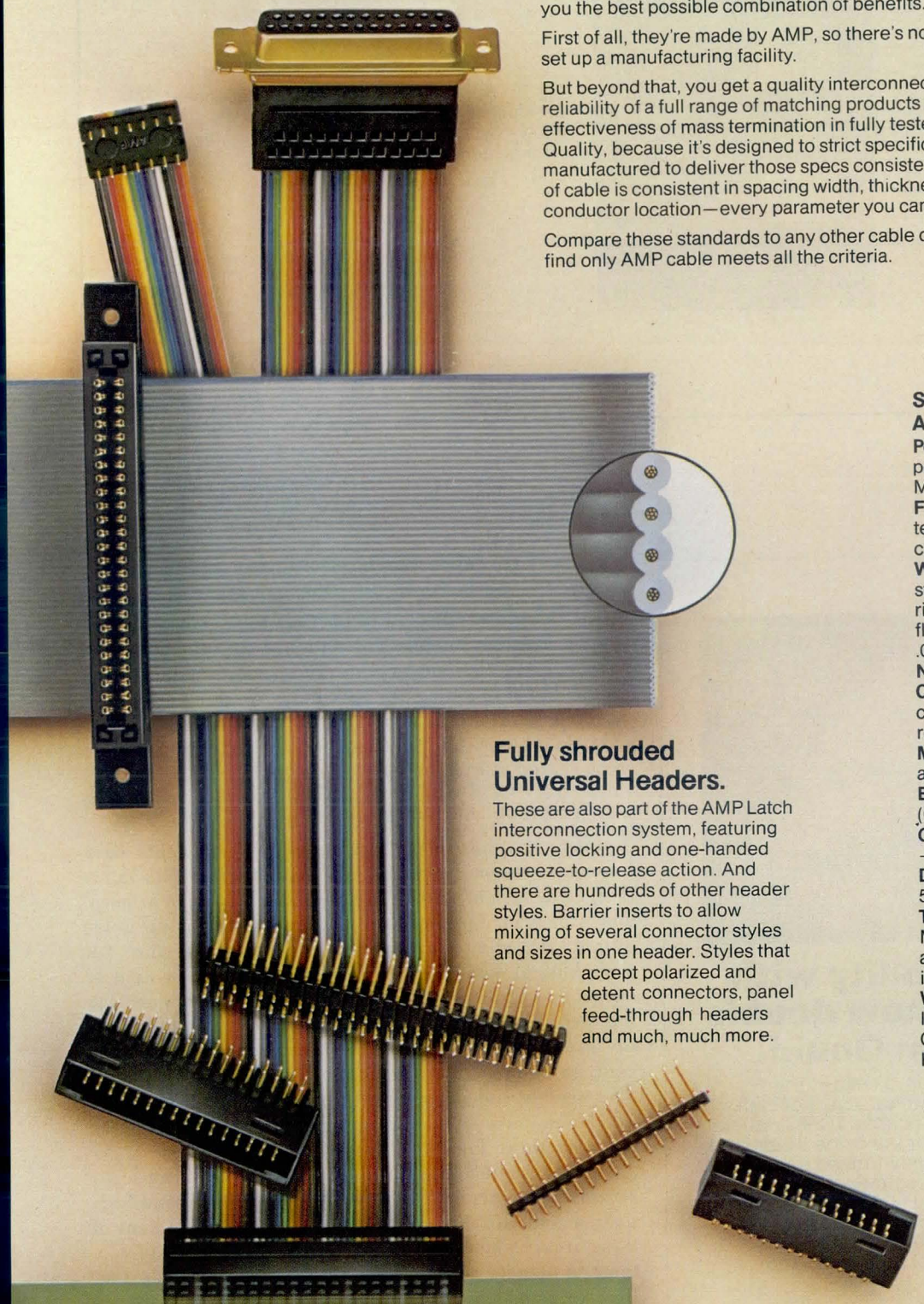

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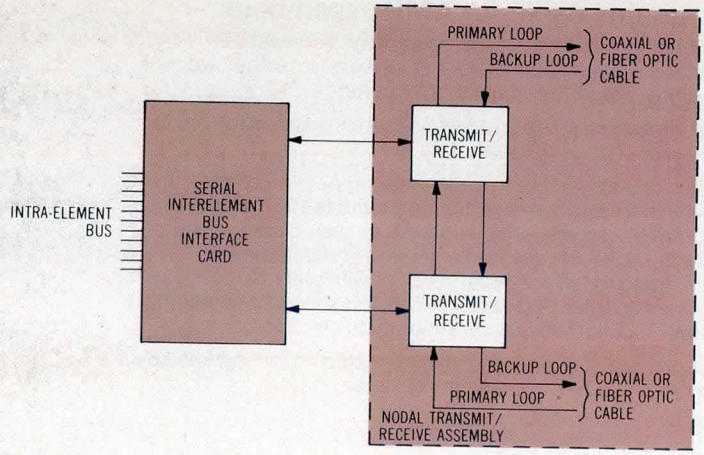

Fig 3 SIB interface hardware. Independent T/R assemblies enable bus reconfiguration and also allow hybrid (fiber optic/coaxial cable) loop arrangement

flow in both loops, keeps the bus intact, and isolates the failed node. In these circumstances, the failed node is dropped from the bus.

Should a loop (wire) fail, nodes on either side of the fault will reconfigure, preserving the bus and keeping all nodes active. Multiple failures, if not adjacent, will result in several isolated sub-buses determined by the points of failure. The technique used in this scheme maximizes the probability of retaining an active bus while it minimizes the required hardware as compared with systems using fully redundant buses. The SIB allows most of the hardware logic to be shared at each node.

Bus Interface Hardware

The data bus consists of three hardware components: data bus node, transmission link, and bus interface (SIB interface) card, each of which can handle two loops, the primary and a backup. Bus interface hardware partitioning is required to: allow independent operation of the T/R assemblies as data repeaters when the SIB interface card or element has failed; provide capability to reconfigure the bus; permit interchangeability of coaxial cable and fiber optic T/R assemblies; contain the SIB interface logic on a single card; and minimize the amount of redundant logic on the T/R assembly. Implementation of the bus interface hardware in relation to the node which is being provided access to the bus is shown in Fig 3.

The packaging approach physically and electrically separates T/R circuitry from the SIB interface card and from the remainder of the node. Should a failure occur in any of these areas, other than in the T/Rs, the full loop can continue to operate as a repeater with the failed node's T/Rs. Receive assemblies are internally connected and provide the capability to monitor the loop for signal absence/loss of synchronization for reconfiguration purposes.

Two independent T/R assemblies provide the capability to reconfigure the bus. The incoming signal from the primary

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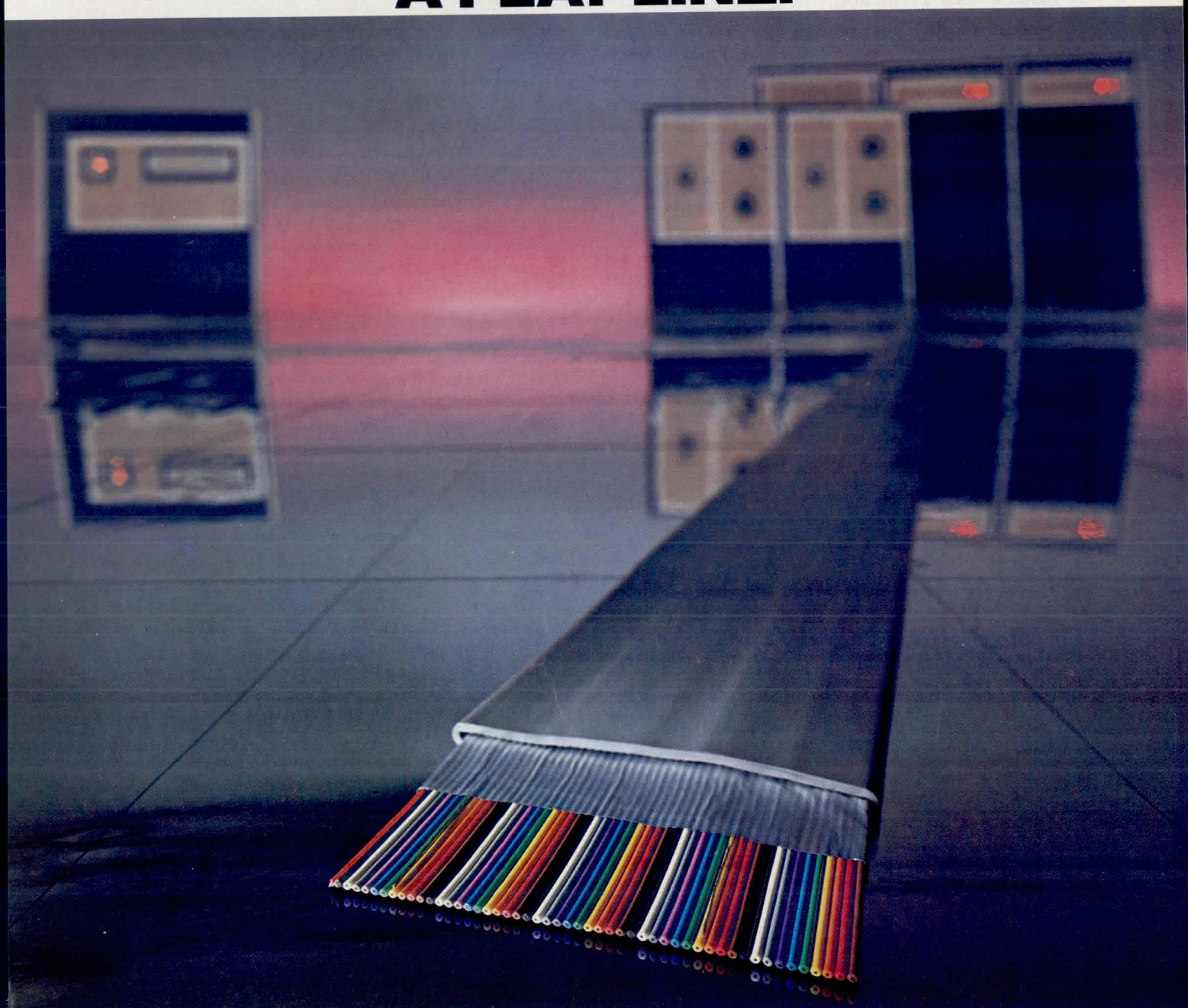

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CIRCLE 16 ON INQUIRY CARD

loop may be routed directly to the backup loop or vice versa as reconfiguration requirements dictate. A by-product of this approach is identification and isolation of the failed node/element.

Creation of a hybrid loop configuration also is possible with two independent T/R assemblies. Given this partitioning, an element can convert the transmission medium of the bus from fiber optic to coaxial cable and vice versa simply by replacing a T/R assembly. This feature allows the optimum transmission medium to be chosen for a given application. Fiber optic links, for example, should be selected for high noise or data security environments, while coaxial cable would be more cost-effective where elements are closely located in a relatively noise free environment.

SIB Performance Evaluation

Performance analysis determined the data throughput percentage and system response time for different length messages. These factors were chosen because system response time is critical to a military system, and because response time is highly dependent on what percentage of bus time is actually used for system data transfer.

Using the following assumptions, the analysis considers point to point and multidestination group address message transmissions. (1) Three message lengths are defined: short, 64 bits; medium, 32 bytes; and long, 4k bytes. (2) Message overhead includes all bits in a message frame that are not considered system-related information. SIB message overhead is 56 bits/message: 24 bits for flags, 16 bits for the message length word, and 16 bits for the error check word. (3) Response time is bus access delay plus the time to move the message from source processor memory to receiving processor memory. Bus access assumes that 50% of the data bus users are ahead in the go-ahead polling sequence and 10% wish to transmit. Bus access delay, therefore, would consist of 45% not using the go-ahead and 5% transmitting a message.

Results of the performance analysis are given in Table 3. Efficiency figures are for the node to node transmission. A review of the data indicates that the SIB provides a relatively efficient data transfer for short messages and improves as the message size increases. Together with an already efficient bus design, group addressing significantly increases the real data throughput by eliminating multiple transmissions, which would be required in a system without this capability.

TABLE 3

Performance Analysis

Evaluation Parameter	Percentage Bus Time For Data Transfer	Response Time, μs
Short message	50.3	38
Medium message	79.1	47
Long message	96.8	1634

TABLE 4

SIB Interbus Protocol

Field	Comment
F_O	Opening flag
A_T	Unique address of bus exit node
C	Control (16 bits)
A_C	Checksum on addresses and control
ML	Message length
I	First 8 bits: A_T unique address of receiver; second 8 bits: address of loop; remainder of I field: message
EC	Error check
F_E	Ending flag

Multiple Bus Operation

In a typical combat system installed on a destroyer, seven separate functionally organized buses provide for autonomous subsystem design, rapid response in the sensor to weapon chain, and enhanced survivability. One central command and control bus interfaces with six weapon subsystem buses. Two interconnections to the command and control bus are provided for each of the other buses to afford multiple redundant paths for fail-safe operation in case of battle damage. This configuration requires a protocol that permits efficient interbus communication. The design selected, a natural extension of the SIB protocol for single-bus communication permits continued use of the single-bus software without modification and minimizes the additional software needed to accommodate the additional capability. This approach has the advantage that no change is required to either hardware or firmware for implementation of the interbus communication.

Interconnection between the various buses is provided by multielement nodes (clusters). These may interconnect as many SIBs as the cluster has elements, ie, one bus interface per element. This cluster, called the bus exit node, performs a high speed, well-defined store and forward function.

Protocol for interbus communication is shown in Table 4. Header fields have no change in definition, permitting continued use of existing hardware and firmware. However, the first word of the I field has been reserved for special functions under software control. The first 8 bits of the I-field word are the unique address of the element to which the message is being transmitted, and the second 8 bits are the address of the loop containing the element addressed. These two fields are used by the bus exit node to route the message to the appropriate bus for eventual reception by the addressed element.

The data processing architecture of the distributed processing system will be described in a future issue.

References

1. R. Mauriello, "A Distributed Processing System for Military Applications—Part 1: System Overview," *Computer Design*, Sept 1980, pp 14-30
2. R. A. Donnan and J. R. Kersey, "Synchronous Data Link Control: A Perspective," *IBM Systems Journal*, No 2, 1974, pp 140-162

Add-in Reliability. Then Relax.

Our LSI-11* memory systems come with built-in ECC (Error Checking and Correction) circuitry. So you don't have to worry about expensive service calls, or strained relations with customers. Our 2,500 ECC systems in the field have a proven MTBF *in excess of 15 years.*

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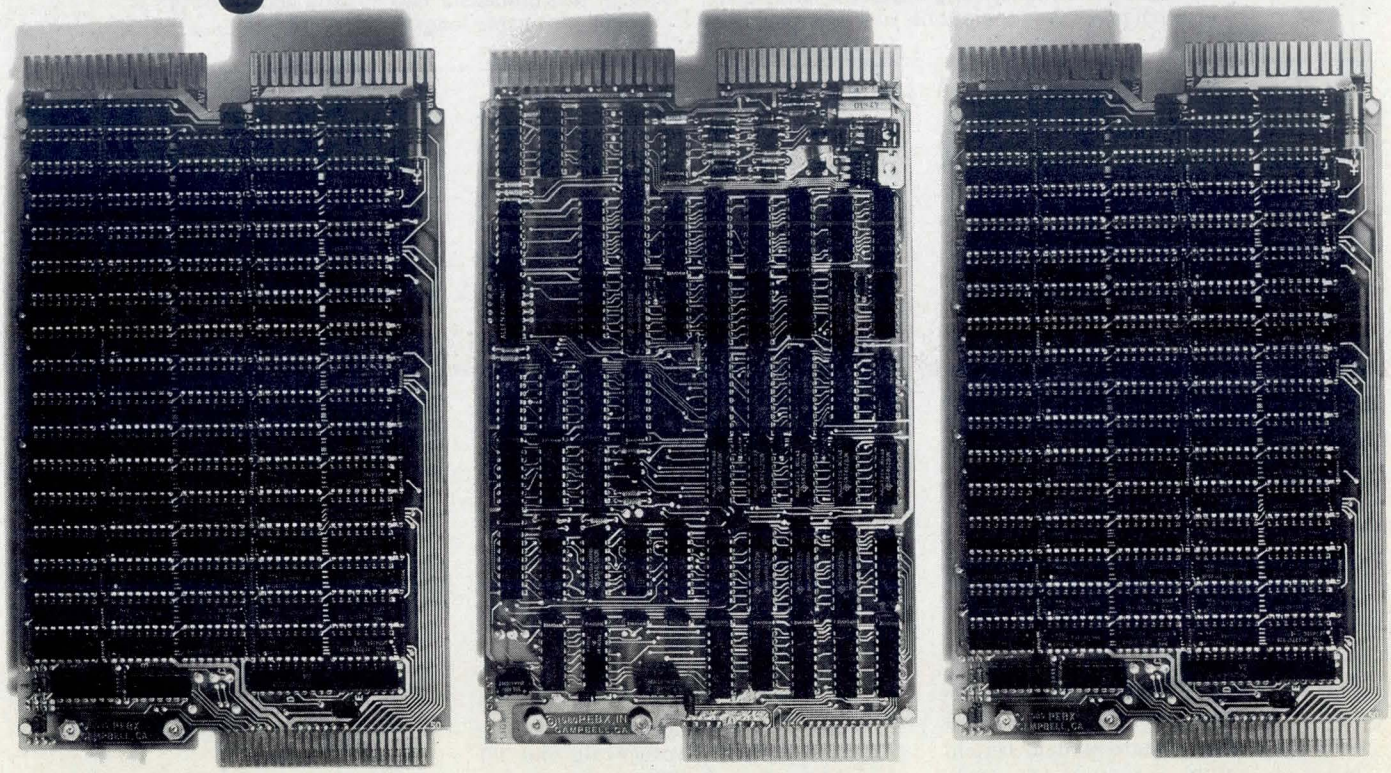

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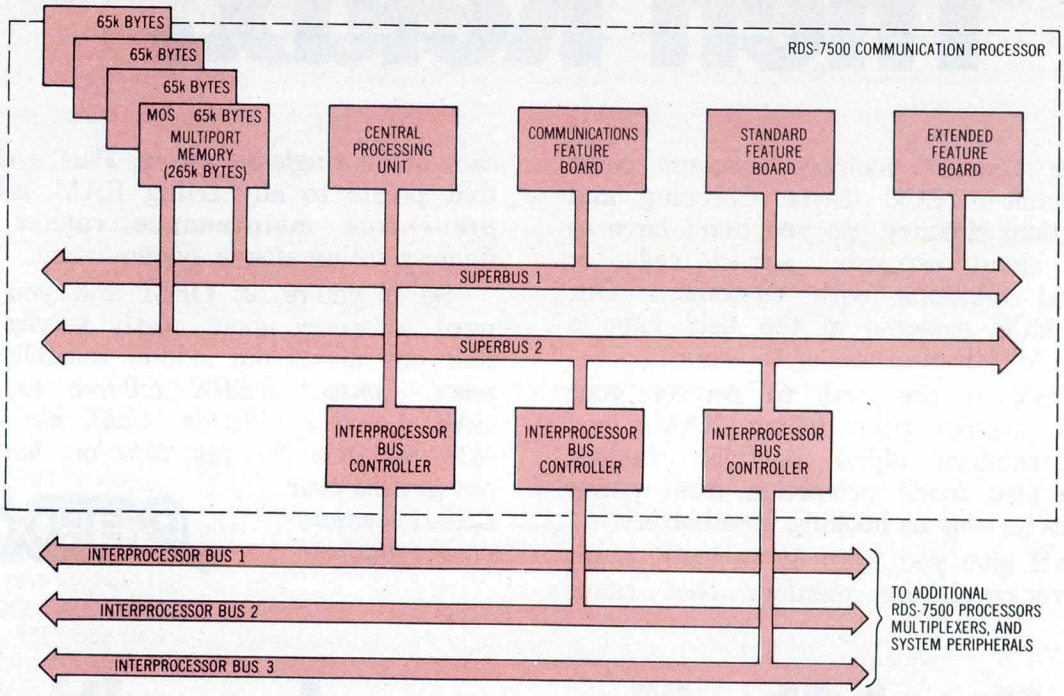
CIRCLE 17 ON INQUIRY CARD

Multiprocessor Hardware, Multitasking Software Combined in Data Network Enhancements



Bus architecture. Dual bus architecture reduces system contention problems and improves performance. One superbus handles internal processor operations, other handles IPB controllers that support additional processor, multiplexers, and system peripherals. RDS-7500 processor can directly access both buses. IPB cable length is 48 ft (14.6 m) max

RDS-7500 communications processor (CP) and preemptive communications operating system (PCOS), recently introduced by Raytheon Data Systems Co, Minicomputer/Communications Div, 360 Forbes Blvd, Mansfield, MA 02048, represent "Phase 2" in the company's evolving family of RAYNET systems. The processor unit provides access to multiple mainframes or applications without regard to differences in protocols used by either mainframes or terminals. PCOS includes multitasking control routines, application modules, and support for communication lines from both host processors and terminals.

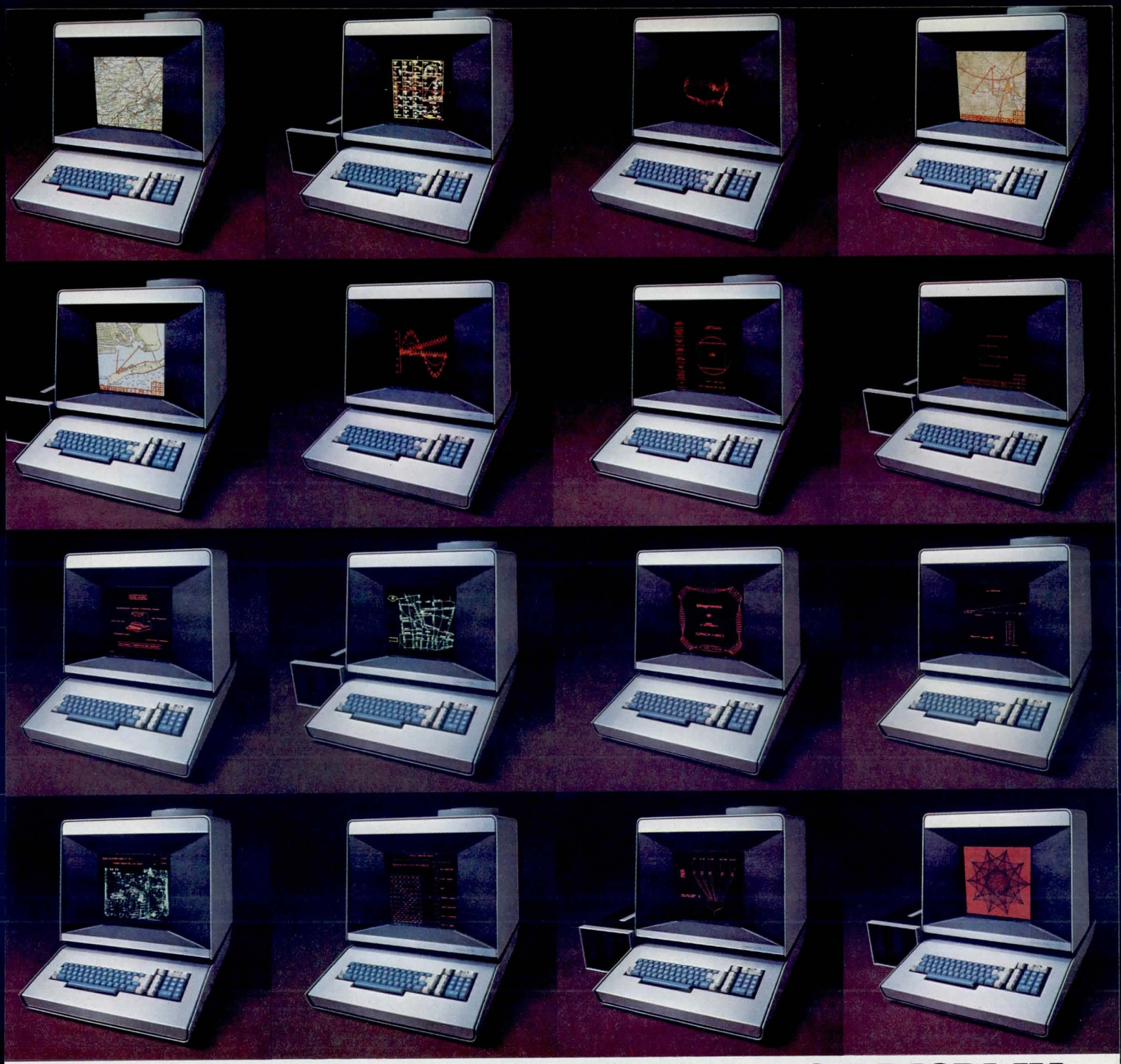
The CP features a multiple interprocessor bus (IPB) architecture (see Figure) that provides numerous ways to link processors for redundancy and reliability. A solid state modem switching device (MSD) replaces the formerly used electromechanical device. IPB architecture and the MSD allow fallback/recovery at the major component level for uninterrupted service even in event of a major component failure. The processor has up to 262k bytes of memory in 65k-byte modular increments with direct memory access (DMA), and a cycle time of 700 ns. The 22-bit word length consists of two 8-bit bytes plus 6 bits for ECC.

Buffer chaining increases throughput by enabling a network based processing routine to send multiple buffer messages, regardless of length, with a single command. Automatic handling of interrupts at the end of each buffer does not require software intervention to complete the processing task.

System software consists of PCOS, system initialization routines, and both debug and reconfiguration utilities. PCOS supports interprocessor and I/O control, and task, file, and memory management. It allows the processor to handle a virtually unlimited number of active tasks at the same time, based on as many as 256 user assigned priorities. Multiprocessor support ensures that the network will not go down because of a single component failure. The system also supports a variety of peripherals including the IPB, discs, cassettes, TTYs, communication lines, and printers. PCOS was designed specifically for communications control and not as a general purpose operating system; as a result, it requires a minimum amount of memory.

The RDS-7500 will replace RDS-500 processors within RAYNET system configurations and will be included in future shipments of all systems. Present users with currently installed systems will have the option of upgrading to the new processor level.

Circle 516 on Inquiry Card



WHEN IT COMES TO PUTTING IT ALL ON DISPLAY, THE ORION-60 STANDS ALONE.

A display terminal that won't stand alone can't be as versatile or as adaptable as the Orion-60, the modular plasma display system that stands by itself or interfaces with existing hardware to let you create your own programs.

To begin with, the Orion-60 is an easy touch: besides offering full alphanumeric, floppy disc and rear-projection capabilities, it lets you create displays and enter data simply by touching the screen with your finger.

That means you can project a slide onto the screen coordinates and plot your own course over it. You can program your own character sets. You can generate vectors of any length to absolute screen coordinates. In short, you'll have a flexible terminal that will keep up with your needs today—and grow with your operations tomorrow.

Of course, since Magnavox was a leader in the development of plasma terminals, you can be sure your Orion-60 will have a bright, high-contrast display free from jitter and distortion.

There's a lot more you should know about the ways this remarkable terminal can help you get more out of graphic displays. For a demonstration, call or write Tyler Hunt at Magnavox Display Systems, 2131 S. Coliseum Blvd., Ft. Wayne, IN 46803, (219) 482-4411.

Magnavox
DISPLAY SYSTEMS

CIRCLE 18 ON INQUIRY CARD


SIGNAL CONDITIONERS/ AMPLIFIERS
HI-5900
HI-5901
ANALOG MULTIPLEXER
SAMPLE AND HOLD
REF
D/A
REGISTER
ANALOG TO DIGITAL CONVERTER
HI-5712
μP

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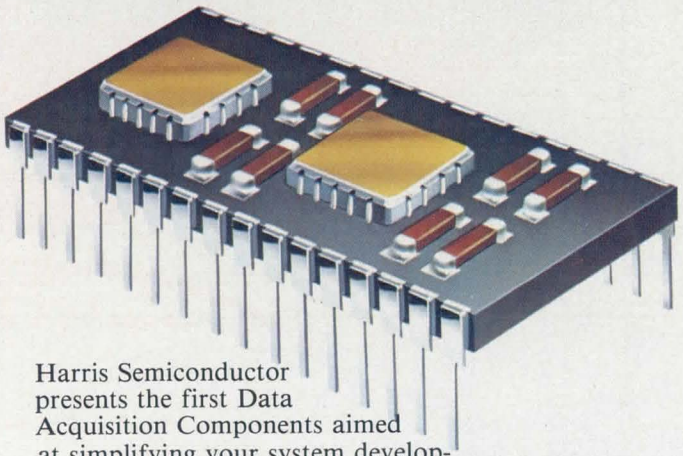
Harris unique LCC Hybrids simplify electronic system designs.



Harris Semiconductor presents the first Data Acquisition Components aimed at simplifying your system development tasks, while relaxing your design constraints.

Meet the HI-5900, the HI-5901 and the HI-5712—a new breed of products characterized by simplicity of application, accuracy, speed at low power consumption, versatility and reliability.

Simplicity of Application The HI-5900 (or the HI-5901) and the HI-5712 provide all the functions required to convert analog transducer outputs into a twelve-bit binary format suitable for microcomputer processing. No additional components are required. Moreover, they are offered in easy-to-use dual-in-line packages to minimize board size. Pin counts are 32, 32 and 40 respectively.

Accuracy An impressive list of product performance parameters minimizes inherent system errors:

- ☐ Common Mode Rejection—86 dB
- ☐ Feed Through—80 dB
- ☐ Sample-and-Hold Droop Rate—5 nV/μs
- ☐ Differential Linearity Error—¼ LSB
- ☐ Integral Linearity Error—¼ LSB
- ☐ Quantization Error—½ LSB

Speed and Power Consumption Minimum channel-to-channel throughput rate is 50 kHz. That includes 9 μs acquisition time for the HI-5900 or the HI-5901, and 8 μs conversion time for the HI-5712. Total power consumption is 1.4 watts.

Versatility and Reliability The HI-5900 delivers full performance when used in conjunction with *any* commercially available A/D converter.

It features software-controlled selection of:

- ☐ One (or none) of eight high-impedance differential input channels for time-multiplexed multisensor applications.
- ☐ One of four gain options (1, 2, 4 and 8) for increased dynamic range capability.
- ☐ Suitable track-and-hold cycle lengths.

Alternatively, the HI-5901 provides sixteen high-impedance input channels for single-ended applications. Both products offer serial/parallel MUX expansion terminals and external offset nulling capability. Their power consumption is only 255 mW.

The HI-5712 ADC features:

- ☐ Internal clock with external clock override option.
- ☐ Internal reference with external reference connection option.
- ☐ Software-controlled offset binary or two's complement output code selection.
- ☐ Tristate buffered parallel outputs, and NRZ serial output information for remote data transmission.
- ☐ Software-controllable conversion cycle lengths of 12, 10, 8 and 6 bits.
- ☐ External gain and offset adjustment capability.

The HI-5900, -5901 and -5712 are offered in four quality grades, grouped by operating temperature range:

Commercial/Industrial (0°C to +70°C)

1. Standard, Dash-5 code
2. High-reliability, Dash-7 code

Military (−55°C to +125°C)

3. Standard, Dash-2 code
4. MIL-STD-883 Class B, Dash-8 code

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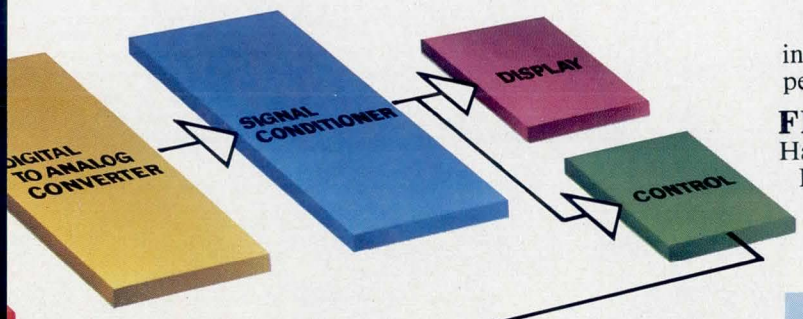

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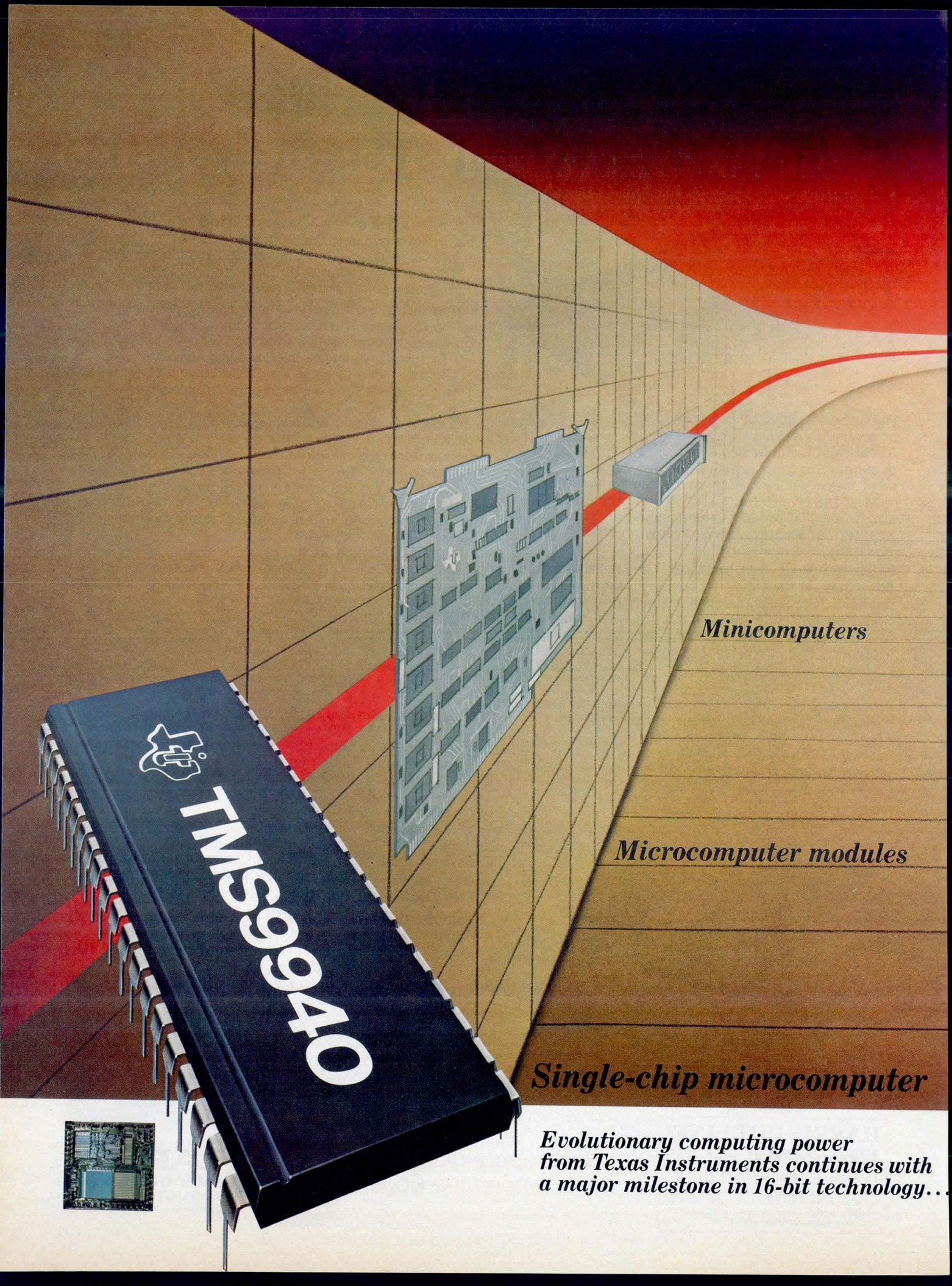

Evolutionary computing power from Texas Instruments continues with a major milestone in 16-bit technology...

TMS9940

16-bit single-chip microcomputer. World's first. Here. Now. Available.

With the TMS9940, Texas Instruments significantly advances its 16-bit leadership.

With the TMS9940, Texas Instruments expands on what is already by far the industry's most complete 16-bit family. The 9900 Family of microprocessors, microcomputers, peripherals, microcomputer modules and software and hardware development systems, offers a unique software compatibility. So you can move from one product level to another, confidently, protecting your development system and software investment with no need for translators, code convertors, etc.

TI's 9900 Family is the *only* family that maintains architectural and software compatibility from single-chips to multi-chips to modules to systems — all the way to the object code level.

With the TMS9940, Texas Instruments brings you high-volume, cost-effective solutions to tough system design problems, combining the computing power of a multi-chip 16-bit system with the reliability and compactness of a single-chip solution.

With its high-speed processing, bit I/O, and advanced memory-to-memory architecture, the TMS9940 offers computation power unequalled by any other single-chip product on the market, while retaining the programming ease of 16-bits.

High-speed number crunching and bit I/O

Powerful instructions — like BCD add, BCD subtract, 16-bit multiply with 32-bit results, and compatible divide — provide a number-crunching capability unsurpassed by any single-chip product.

Thirty-two on-chip, flexible, individually configurable input/output bits are addressable for manipulation by powerful bit I/O instructions.

I/O expansion modes permit up to 256 bits of external I/O to be added, allowing easy interface to 9900 Family peripherals and most industry peripherals.

Advanced memory-to-memory architecture

Advanced memory-to-memory architecture makes the TMS9940 ideal for interrupt-driven and extensive I/O applications.

This innovative architecture features multiple register files that provide ease of programming and unsurpassed interrupt response time.

The TMS9940 memory consists of 128 bytes of RAM and 2048 bytes of ROM. Other features include 4 levels of interrupts, plus an internal decrementer which can be programmed as a timer or event counter.

TMS9940 — Key Features

- 16-bit instruction word
- Instruction set includes 16-bit multiply and divide, BCD add and BCD subtract
- 128 bytes of RAM on chip
- 2048 bytes of ROM (or EPROM) on chip
- 64 general-purpose 16-bit registers
- Program execution from RAM or ROM
- 4 prioritized interrupts
- On-chip timer/event counter
- 32-bits integral general-purpose I/O bits — expandable to 256 external I/O bits
- 4 MHz crystal operation — up to 117,000 interrupts per second
- 5-volt MOS technology
- Offered in a 40-pin, 600-mil DIP

Here-and-now availability

Perhaps just as important as the unmatched capacity for design flexibility, the 9900 Family is here-and-now and readily available. It's the lowest cost 16-bit CPU family. And proven where it counts most. In the marketplace. The choice of hundreds of companies for a wide range of systems and end products.

Microcomputers mean high volume and TI has unequalled production capacity and experience. In fact, TI is the largest supplier of single-chip microcomputers and has shipped more than the next two suppliers — combined.

9900 Family development tools

Reliable, available, economical development systems designed to boost programmer efficiency and cut costs.

The AMPL* prototyping lab: A complete set of the software and hardware development tools for the TMS9940 as well as for other 9900 Family CPUs. The AMPL system provides a real-time TMS9940 emulator and a logic-analyzer function to solve complex programming and hardware debug problems.

TMS9940E: This EPROM version of the TMS9940 is the ultimate prototyping tool, allowing in-field system checkout, reducing turnaround time and expense for code revisions.

Leadership staying power

TI has paced the industry through generations of semiconductor innovation, pioneering the lion's share of major milestones.

The 9900 Family is an important part of that leadership tradition. The 9900 Family is a fact. A production-proven, available, deliverable fact.

The continuing introduction of new, advanced 9900 Family CPUs, with TI's state-of-the-art technology and proven production resources, demonstrates TI's total commitment to 16-bit leadership.

That's why you can design with the TMS9940, confident in a family that's a reality today. Confident that the family will grow with your needs to keep your systems competitive at the leading edge of tomorrow's technology.

For more information about the TMS9940, or any other 9900 Family member, contact the TI field sales office nearest you. For details and specifications, write to Texas Instruments Incorporated, P. O. Box 1443, M/S 6404, Houston, Texas 77001.

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CIRCLE 19 ON INQUIRY CARD

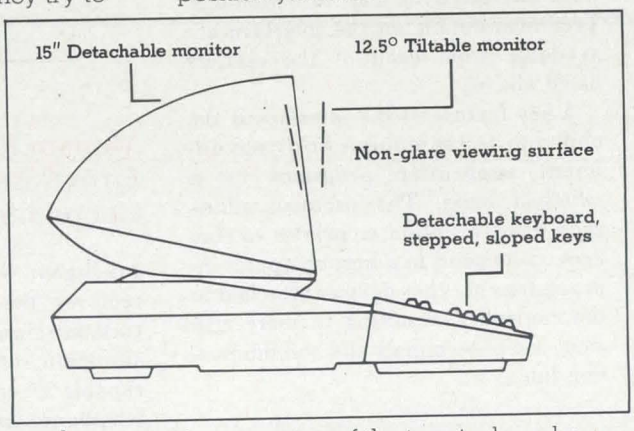
Introducing the terminal you've been crying out for.

Operators who use video display terminals all day know what a pain in the neck it can be.

They sometimes experience eyestrain, headaches, backaches, and irritability. Because they try to compensate for visual problems by assuming awkward body positions.

Meet the Ergonomic Terminal™ video display from Lear Siegler. The terminal that makes working conditions easier on the worker.

Ergonomics is the successful physical interaction between man and machine. It's the reason the Ergonomic Terminal was designed. For the most comfortable work environment possible and the convenience of the operator.



IT COMES APART TO KEEP YOU TOGETHER.

With the Ergonomic Terminal ADM-42, you get a large, non-glare 15" screen to cut down on sore eyes, tearing, and blurring. You get a high-resolution monitor (7 x 11 dot matrix characters) for the sharpest picture available. You even have separate contrast and brightness controls.

A tiltable monitor lets you reposition the Ergonomic Terminal, so you don't have to reposition yourself. You can separate the keyboard and video display and locate them in any position you like. And the control base portion of the terminal can be remotely positioned out of the way.

Farewell, eyestrain. So long, backaches. Good-bye, headaches.

BEAUTY *AND* BRAINS.

The ADM-42 isn't just another pretty face. It's the smartest terminal in its class with full editing capabilities, a full array of visual attributes, flexibility of format, security, interface, and transmission. Not to mention four-page display as standard equipment. With an optional extended memory capable of adding data space up to a maximum of 8 pages.

The Ergonomic Terminal has a bright, easy-to-read 1920 character display (24 x 80), 128 ASCII character set, and 16 function keys (optionally programmable) that store 32 or 64 characters each.

It also comes with a 25th line established and reserved for status indicators and messages of up to 78 characters.

As if all this isn't enough, the ADM-42 comes with options. Galore.

So if you think the terminal you're using now is a real eyesore, consider the Ergonomic ADM-42.

It just may put optometrists and aspirin makers out of business.

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DATA PRODUCTS DIVISION

The Ergonomic Terminal™ from LSI.

CIRCLE 20 ON INQUIRY CARD

Volume Lists Local Network Equipment Vendors

Over 100 pages listing information about more than 40 vendors of local network components and systems, including transceivers, modems, and communications software, comprise a volume available at $125/copy from 3Com Corp, 3000 Sand Hill Rd #1, Menlo Park, CA 94025. Vendors listed supply products that fit the loosely defined category of local computer networks: networks that connect computers within buildings at data rates above 100k bits/s. A few exceptions are included to extend the list in significant directions.

Included in the listing are such vendors as Amdax, Data Point, Digital Equipment Corp, Hewlett-Packard, General Electric, Intel, Interactive Systems/3M, Nestar, Sytek, Ungermann-Bass, Xerox, and Zilog. Each vendor listing is about a page long, with product descriptions, technical data and delivery schedules. The name of a key contact at each firm is included.

Carriers Adopt Standard Interface for Terminals, Access to Multiple Hosts

Three major data communications carriers in North America have agreed on a common communications protocol for interfacing IBM 3270 binary synchronous terminals to their public packet-switched networks. The carriers are: Tymnet, Inc, 20665 Valley Green Dr, Cupertino, CA 95014; GTE Telenet Communications Corp, 8330 Old Courthouse Rd, Vienna, VA 22180; and Bell Canada, Computer Communications Group, 160 Elgin St, Ottawa, Ontario K1G 3J4, Canada. The latter is the provider of the Datapac network in Canada.

Manufactured by IBM and other firms, 3270-type terminals are widely used for data entry, database inquiry, and other transaction processing applications. A typical application consists of up to 32 display stations or printers attached to a cluster controller. A leased line directly connects the controller to a host computer.

Agreement on the common protocol enables carriers to provide 3270 compatible data transmission service between networks on an international basis. The protocol specification is being made available to other carriers worldwide and also to manufacturers for developing compatible packet network interfaces for their 3270 products. Technical details on the interface are available from each of the carriers listed above.

A key feature of the interface is the ability to access multiple hosts and different application programs on a switched basis. The protocol allows each display station or printer to connect on demand to a host computer independent of other devices attached to the controller, resulting in more efficient use of terminals and communication lines.

Synchronous, Single-Line Interfaces Extend LSI/PDP Communications Abilities

Mounted on single quad boards, two communications interfaces are designed to operate with Q-bus™ and Unibus™ systems. Both synchronous single-line interfaces are functionally equivalent and software compatible with the DUP-11. They provide serial to parallel and parallel to serial data conversion, EIA level conversion, modem control for full- and half-duplex operation, protocol management, and bus interface.

The interfaces, according to MDB Systems, Inc, 1995 N Batavia St, Orange, CA 92665, offer increased flexibility in handling bit- and byte-oriented protocols. With data rates up to 500k bits/s, they will accommodate SDLC, ADCCP, and HDLC bit-oriented protocol (BOP), and Bisync and DDCMP in byte control protocol (BCP). Programmable character lengths of one to eight bits for BOP and five to eight bits for BCP are also provided.

Error control features include CRC-CCITT preset to 0s or 1s, CRC-16 preset to 0s, or VRC odd or even. Other features include sync or secondary station address comparison and idle transmission of sync-flag on mark. The units provide sync generation, detection, and stripping for BCP, automatic detection and generation of BOP control sequences, zero insertion and detection for BOP, and short character detection for last BOP character. For the Q-bus, all signal handling is confined to the A and B slots.

Circle 517 on Inquiry Card

Modem Provides Error Free Transmission on Unconditioned Lines

Intelligent modem series Micro5000 removes the problem of undetected transmission errors by providing automatic retransmission on error. It is capable of error free transmission on telephone lines having error rates greater than 1 in 10^4, through several seconds total line outage. Micom Systems, Inc, 9551 Irondale Ave, Chatsworth, CA 91311, has announced the devices, which are designed specifically for use with minicomputers and dumb terminals. The modems allow asynchronous terminals to operate at 2400, 4800, or 9600 bits/s on standard unconditioned lines, error free, without changes to existing hardware or software.

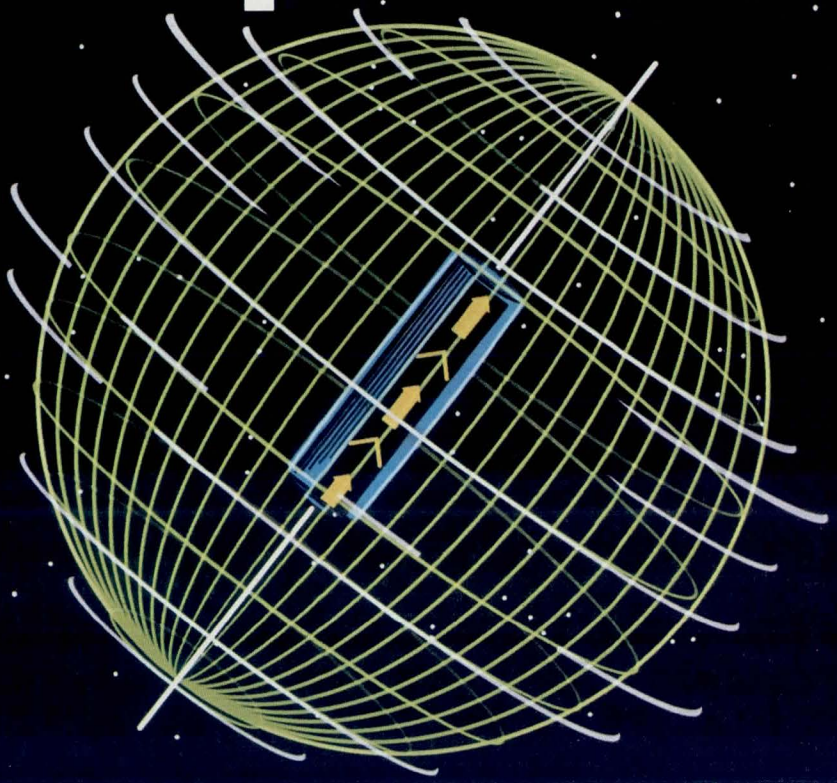
The units also provide automatic compensation for a variety of line problems and distortions. The line between modems must be a 4-wire point to point leased line. AT&T 3002 basic channels are adequate. The 2400-bit/s modem is compatible with Bell 201/CCITT V.26, the 4800 bit/s version with Bell 208A, and the 9600-bit/s unit with CCITT V.29.

Error control technique is full duplex, ARQ, go-back-N, with CRC, using a proprietary algorithm. Data compression is achieved by removing start and stop bits, and a 2600-character buffer storage is dynamically allocated to transmitted or received data as required. A MIL-STD-188C interface is selectable for military data terminals.

MOS/LSI design results in low component count; the 9600-bit/s modem is implemented on a single 10.5 x 11.5" (26.7- x 29.2-cm) card. Weight of a standalone unit is less than 10 lb (4.5 kg).

Circle 518 on Inquiry Card

Need high-reliability capacitors?



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Series Type	Capacitance Range (μF)	Voltage Range (V.DC)	Data Sheet
Low Leakage	0.1 ~ 100	6.3 to 100	LLU&E
Low ESR	1.0 ~ 1,000	6.3 to 200	PLU108
CS Low Profile	100 ~ 2,200	10, 16, 25, 35	CS040
PL-B, PL-BG High Ripple	47 ~ 2,200	160 to 450	PLB108
RD High Temperature	0.47 ~ 1,000	10 to 100	RD050
Bipolar	1.0 ~ 100	50, 63	BP376
Computer Grade Can	120 ~ 1,000,000	6.3 to 450	CG018

We're capacitor specialists. And that means we're delivering special application capacitors that meet the needs of the computer, computer peripheral, data terminal, telecommunications, high-frequency filter, power supply and audio equipment industries.

So, if special performance is what you need from a capacitor, go ahead and design with confidence. There's just no capacitor manufacturer anywhere ready to deliver more types of special application aluminum electrolytic, ceramic disc and film capacitors.

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CIRCLE 21 ON INQUIRY CARD

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A half-card 16-bit mini with half-cost economy. Four on-board distributed I/O channels, hardware multiply/divide and DMA are standard. Cost? Even less than many micro-computers.

The NM 4/30
A midrange beauty. Twice as fast as the 4/10 and with a larger instruction set. Double register shifts, multiple-word memory reference instructions, and more.

The NM 4/90
Twice as fast as the 4/30 and with a beefed up instruction set. With a hefty 128K byte's worth of direct addressing, it's an ideal choice for high-performance applications like industrial control and data communications systems.

The NM 4/95
Top of the line. Memory management unit for expansion to 8 megabytes. ECC RAM memory for reliability. High speed cache memory for faster throughput. And Page Protection to prevent destruction of another user's space.

The NM 4/04
SCOUT,™ the little fella that's had OEM's buzzing for months. Through the wizardry of ISOLITE,™ SCOUT can test himself every time he's turned on. And a 16-bit CPU, I/O, 32K byte RAM, and card cage costs less than $1,000.

ComputerAutomation has just what you need to cut a path through to your computer solutions.

You need compatibility? We've got it, with software compatibility from SCOUT through our 4/90. And I/O compatibility across the family, from the 4/10 through the 4/95. All with up to 128K Bytes of directly addressable memory. And up to 8 megabytes of physical memory for the 4/95.

You want software and development tools? We've got all the operating software to get you up and running. And our PROTOS system provides multi-user development support.

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Our famous Intelligent Cables offer low-cost interfaces for async and bisync communications, CRT's, line printers, magnetic tapes, IEEE-488 and 16- and 32-bit parallel I/O.

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The family never runs short of memories. Core, RAM, and E/PROM. Plus battery back-up and parity or error correction. From 8K bytes to 256K bytes per card.

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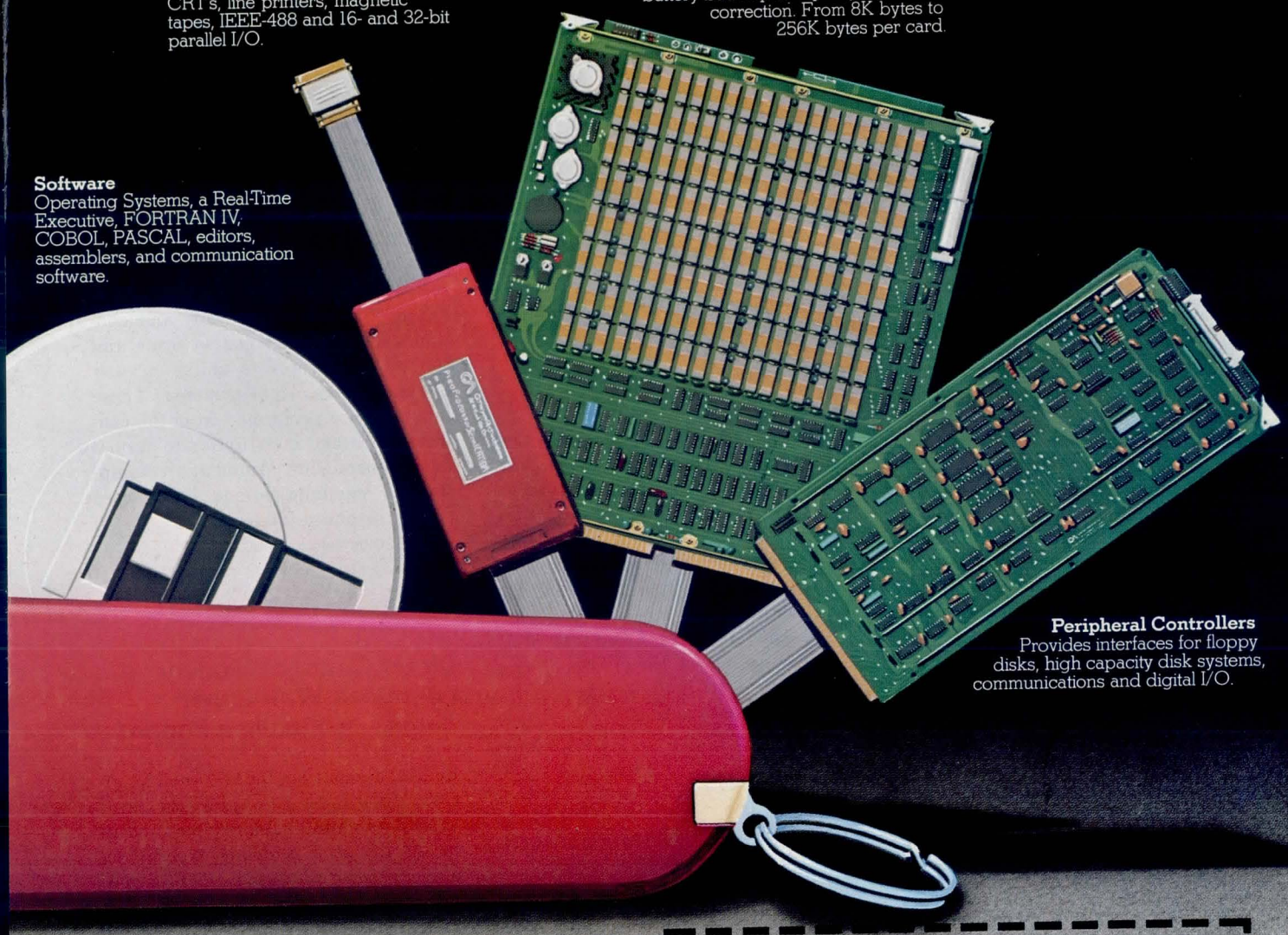

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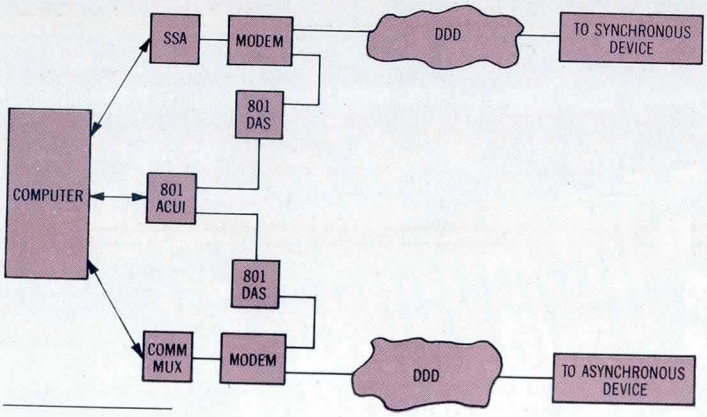
Automatic Calling Unit Interface Provides Dial Backup Capability



SSA: SINGLE SYNCHRONOUS ADAPTER
DAS: DATA AUXILIARY SET

Automatic calling unit interface. Features include onboard RS-232 interface and local loopback mode for online testing

The 801 automatic calling unit interface (ACUI) provides for the connection of up to two Bell 801 data auxiliary sets (DAS) to the company's family of computer systems. Using the ACUI, any number in the direct distance dial (DDD) network can be called to establish a data link. It is available from Perkin-Elmer, Computer Systems Div, 2 Crescent Pl, Oceanport, NJ 07757. The interface uses RS-232 voltage levels and conforms to RS-366 specifications. It connects to the DAS via a standard 25-pin plug and accommodates both Touch-Tone® and rotary dialing equipment.

A program call request to the DAS initiates the dialing process. The DAS then informs the program when each successive 4-bit digit of the called number should be transmitted. When the entire number has been dialed, the program waits either for a connection to be established or for a timeout. The latter condition may occur if the dialed number was either invalid or busy and the DAS will inform the program via the abandon call and retry signal.

The ACUI is fully digit buffered. Two independent ports allow concurrent dialing of two different numbers. The interface also provides complete program control over the 801 DAS.

Among the ACUI applications are dial network backup in event of failure of a leased line, and terminal connect with low traffic volume when leased line costs are not justified. When traffic increases, upgrade to a leased line can be achieved without impacting application programs.

The unit requires 5 Vdc at 3 A. Dimensions are 7 x 15″ (17.8 x 38 cm) and weight is 1.5 lb (0.68 kg).

Circle 519 on Inquiry Card

Diagnostic and Management System Serves Medium Scale Networks

Large system management techniques are now available for networks with up to 32 lines. CMS-1000 offers such medium scale network operators complete monitoring and test generating capabilities, and single operator directed automated monitoring, testing, control, restoration, and reconfiguration. This system is the latest addition to the communications management series (CMS) of Racal-Milgo, Inc, 8600 NW 41st St, Miami, FL 33166.

The 4-function system features a color display terminal with a color-keyed menu approach to ease operator understanding and response.

A 10M-byte hard disc stores significant information about modems and other network devices, as well as their physical location and interrelationships in the network. The basic system comes in a 16-line version, with an additional 16-line expansion as an option; the expanded 32-channel version supports 8160 managed units. System communication with the managed network is via interface processors, and each processor is capable of semi-independent handling of 16 channels of network equipment.

CMS network processors, used in conjunction with the diagnostic channel of the CMS modems, monitor and display alarm functions for no response, modem power failure, streaming, receive line failure, external customer alarm, normal mode not restored, and multiple alarms.

The system automatically and continuously scans designated units and reports inappropriate status or any unexpected incorrect response. These functions are performed from the central site without interruption to normal data transmission. Automatic resumption of communications is effected after a response failure.

Circle 520 on Inquiry Card

Direct Connect Modem Functions With Either Single- or Multiline Phones

Bell 103 compatible D-CAT™ modem offers full-duplex capability and voice/data monitor improvement of up to 20 dB over acoustic types. The modem incorporates hold function, privacy button, and self-test.

The device, from Novation, Inc, 18664 Oxnard St, Tarzana, CA 91356, is capable of working with a single- or 50-pin 6-line business phone at data rates to 300 bits/s. A mode switch permits user to monitor whether voice or data are being transmitted. The answer/originate direct connect device has FCC approval for handset jack connection with any modular phone. A separate ac power supply minimizes internal heat and voltage hazards.

Circle 521 on Inquiry Card

Instant Custom Keyboards!

Create Any Keyboard Array Your Way With Grayhill's System 87

1. Do-It-Yourself Prototypes. Choose the building block modules you need; the System 87 includes 1,2,3,4,5, or 6 button strip switches, plus 3x4 and 4x4 keyboard pads. Stack them as you want them; they maintain ½" button centers in any configuration. Single pole/common bus circuitry and matrix coding. We provide snap-on caps and self-stick legend sheet. You get a professional looking keyboard, laid out exactly the way you want it.

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CIRCLE 23 ON INQUIRY CARD

DON'T LET DRIVING YOUR MEMORY DRIVE YOU CRAZY.

You're trying to drive a large, high-performance memory array using 16K or 64K RAMs. And it's driving you nuts.

What with the undershoot, the skew problems, the large number of packages, the boss expecting a faster system than last year's—what's a designer to do?

Introducing the Am2964B: The Simple Solution.

Now Advanced Micro Devices has a bipolar dynamic memory controller for use with 16K and 64K RAMs. It's easy to use. It's flexible. And it takes care of all your $\overline{RAS}$, $\overline{CAS}$ and address problems on one chip.

The Am2964B replaces about a dozen high-speed, high-power Schottky parts. And it not only does the job faster, it uses less power.

But what about the interface to the RAM? We thought you'd never ask.

Meet our Am2965/66 RAM drivers.

The faster you drive your memory, the faster your system. And that's where our new Am2965/66 come in. Together with our Am2964B, they achieve maximum performance and completely eliminate undershoot.

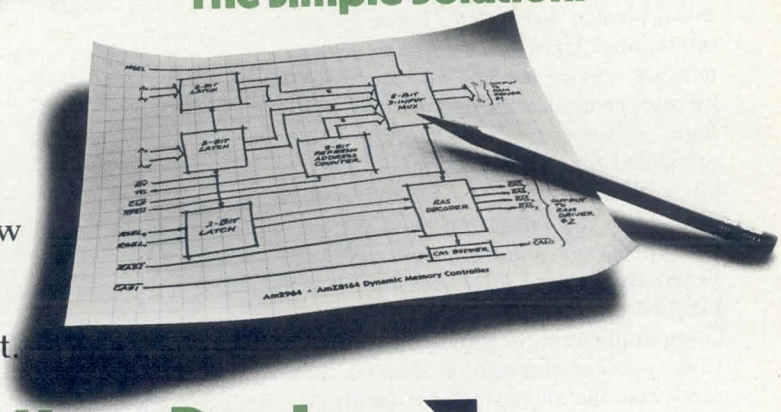
The speed is specified up to 500 pf. Min's and max's, too.

And if you need to upgrade your system, no problem. Our new RAM drivers have the same pin-outs as the S240 and 244, so it's easy to convert your existing system.

The Am2964B and Am2965/66 are the newest members of AMD's dynamic memory support family — the family that makes implementing dynamic RAM systems easier, cheaper, simpler, faster. Like all our parts, they're MIL-STD-883 for free, the highest quality parts you can buy.

Don't let driving your memory drive you up a wall. Send for all the facts on AMD's Dynamic Memory Support Family.

Bipolar LSI: The Simple Solution.



Advanced Micro Devices

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Right, from the start.

CIRCLE 24 ON INQUIRY CARD

Tariffs Filed for SBS Communications Services

Applications for a variety of communications services aimed at both large and small user markets have been filed with the Federal Communications Commission (FCC) by Satellite Business Systems (SBS), 8003 Westpark Dr, McLean, VA 22102.

The filings, submitted several months before the company's domestic satellite communications system is scheduled to begin commercial operations, involve three major areas: (1) an operational tariff for communications network service (CNS-A), an integrated private communications network for high volume traffic requirements, scheduled for availability Jan 1, 1981; (2) a description and informational tariff for CNS-B, a private network service for lower volume requirements. Based on shared use of facilities, it is planned for Jan 1982 availability; and (3) an application to provide interstate voice service through a network of earth stations and associated facilities connecting metropolitan calling areas in the U.S., also scheduled for Jan 1982.

CNS-A features all-digital integrated transmission using time division multiple access techniques and dedicated customer-premises earth stations. It provides each customer organization with a private network for nearly all intracompany communication needs, including telephone, computer to computer, high speed electronic document transfer, and video teleconferencing, integrated into a single network. CNS-A is provided through a minimum of three earth stations called network access centers (NACs). These facilities, owned and maintained by SBS, include relatively small rf terminals installed on customer premises to permit interconnection with customer facilities and terminal devices.

Charges for CNS-A are determined by the configuration of the user's network: the number of NACs, amount of satellite transmission capacity, and the number and types of network connection units (CAUs). CAUs provide the connection between such customer equipment as PBXs and computers and the NACs. Satellite transmission capacity is assigned in blocks called transmission units (TUs). One TU equals 224k-bit/s simplex capacity.

CNS-B, also a private network, offers many of the same services as CNS-A, the principle difference being that some CNS-B facilities will provide services to more than one customer. Each CNS-B network will have a minimum of three NACs, or two NACs plus at least one service point, which is an SBS facility located apart from customer premises. While service points initially will be limited to voice messages, they are planned at a later date to accommodate up to 56k-bit/s data transmission.

The third major element of the filing requests establishment of a company network of 20 earth stations and associated facilities to provide interstate voice service connecting up to 150 U.S. metropolitan calling areas.

Modem with Integral Diagnostic Features Controls Data Network

4800 DCM master site (left) and remote site modems. Master unit incorporates additional diagnostic circuitry, indicators, and controls needed for centralized network control and testing

Diagnostic controlled modem 4800 DCM provides data transmission at 4800 or 2400 bits/s and has integral diagnostic features for control of the entire network. The design incorporates a 110-bit/s secondary channel for test and control of remote site modems without interference to mainstream transmission. A single master modem can control or monitor up to 79 remote units. Analog, line, and digital loopback, plus antistreaming shutdown are included in the diagnostic capabilities.

The modem, from Penril Corp, Data Communications Division, 5520 Randolph Rd, Rockville, MD 20852, operates full-duplex over 4-wire point to point or multipoint leased lines, and half-duplex or simplex on 2-wire leased or general switched networks. Based on CCITT Recommendation V.27 bis/ter, 8-phase differential modulation at 4800 bits/s, and 4-phase differential modulation at 2400 bits/s are employed.

Standard features for the devices include LSI logic circuitry, automatic and adaptive equalization, loop tests between modems, and error bit checks. The equalization scheme allows the modem to be used without adjustment on leased lines having significant distortion or on switched lines having varying characteristics.

A basic configuration of the modems, essentially a remote site unit minus diagnostic capability, is also available. □

Circle 522 on Inquiry Card

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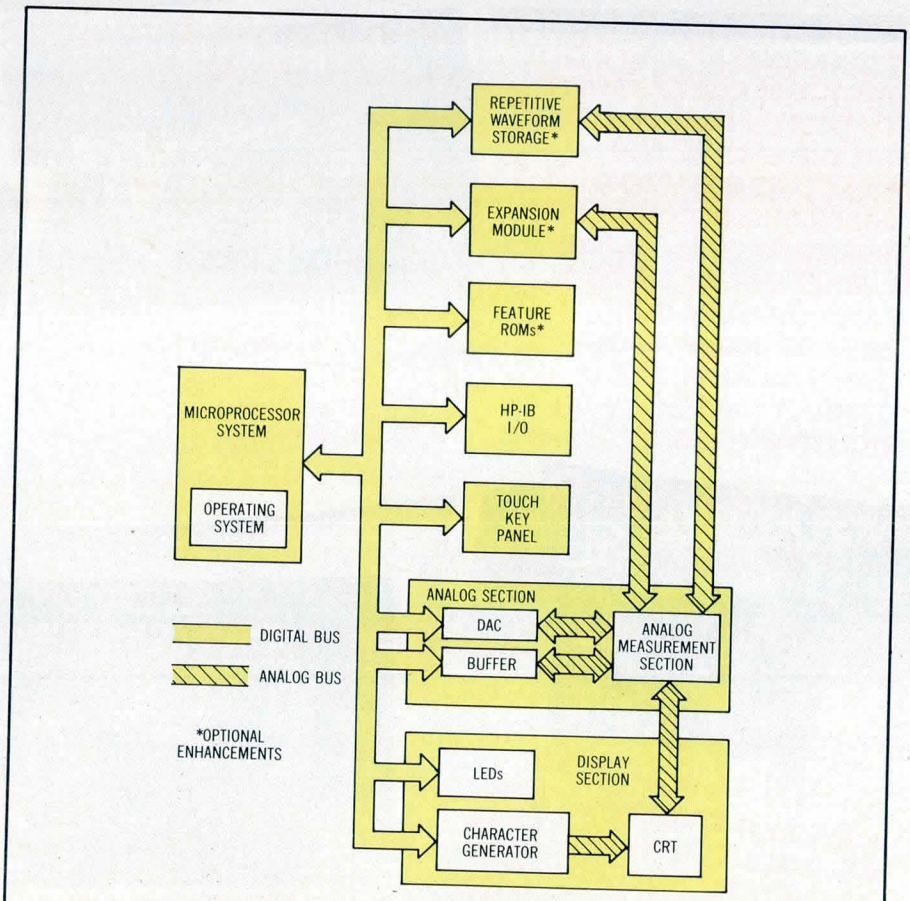
CIRCLE 25 ON INQUIRY CARD

Computer Architecture Makes Oscilloscope Into Measurement System

Using a computer architecture approach to design its 1980A/B measurement system, Hewlett-Packard Co, Colorado Springs Div, 1900 Garden of the Gods Rd, Colorado Springs, CO 80901, introduces a new concept in time domain analysis. Bearing little resemblance to traditional oscilloscopes, the 1980A/B system provides versatility in terms of measurement capability and potential applications, reduced downtime and faster setup and measurement times, and the opportunity to use production or R&D personnel more efficiently.

Patterned after computer systems with CPU operating systems, touch key panel, display, and I/O ports to communicate with peripherals, the basic configuration includes an 8085 based microcomputer with a 16-channel D-A converter, an analog input and measurement section, and LED display. The system is continuously calibrated and features a single rotary control and HP-IB port. Addition of front panel enhancement modules and internal feature ROMs allows future expansion of function and measurement capabilities. Each section in the architecture is a completely partitioned unit, communicating with each of the other units via an internal bus structure.

Another major difference between the system and today's plug-in oscilloscopes is that the basic configuration, without any enhancements, performs time domain measurements. It provides 2-mV sensitivity at 100-MHz bandwidth, independent main and delayed 5-ns/div direct sweep speeds, main or delayed trigger views, a large 10- x 12-cm CRT with a 10- x 10-div internal graticule, a dual (main and main intensified, and delayed) sweep mode, both delta time and voltage measurement capability, plus many features not on traditional oscilloscopes. In contrast, most plug-in designs require a partial or full complement of plug-in modules to provide even elementary measurements.



Simplified front panel, instead of complex array of knobs on traditional oscilloscopes, cuts setup time for HP 1980A/B by as much as factor of five. Touch keys are touch sensitive backlighted buttons, grouped in color coded, hierarchical display with basic operating modes at top, variable functions in center, and less frequently used setup functions for signal conditioning near bottom. Single digitally encoded rotary control adjusts all variable functions, depending on which touch key has been activated

Most significantly, the 1980A/B is capable of automated operation, which offers the user two important benefits: increased productivity and more efficient use of personnel. The system can be programmed by three different methods. First, through the HB-IB, the unit can communicate with and be controlled by an external computer for automatic or semiautomatic measurements. The second method of programming can be operator or computer controlled and consists of a series of nonvolatile registers that can save up to eight complete front panel

(continued on page 58)

DATA I/O INTRODUCES A UNIVERSAL MOS EPROM PROGRAMMER FOR PEOPLE WHO THINK AHEAD.

1982
1981
1980

System 19/MOS Pak programs all of today's EPROMs and offers plenty of room for future growth. MOS Pak lets you program all currently available EPROMs including the 2704, 2708, 2758, 2508, 2516, 2716, 2532, 2732, 2732A, 2564, 2764, 68764, and the new Hitachi 48016 EEPROM.

And what about the future? Simple software changes to the MOS Pak will enable you to program new devices as they're developed—even if you decide to design a 128K EPROM into your product.

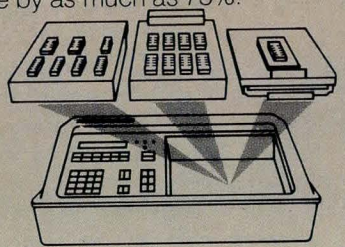
Semiconductor manufacturers' approval provides user security. System 19/MOS Pak is the first "MOS only" programmer to meet the high programming standards set by the semiconductor industry. Programming algorithms and waveforms have received written approval from all of the manufacturers.

APPROVED

Approval plus Data I/O's unique built-in calibration system assure you of high reliability and device yield.

System 19/MOS Pak is self-contained and easy to use. System 19/MOS Pak goes where you need it: engineering lab, service department or in the field. It requires only ten seconds to set up and begin programming. Simply key in a four digit code for the particular type of EPROM you want to program. A lighted LED on the MOS Pak will tell you which socket to use.

And the MOS Pak's new programming algorithm for 64K devices can shorten programming time by as much as 75%.



System 19's modular concept incorporates a mainframe and a variety of programming paks.

With the System 19/MOS Pak, Data I/O now offers three great ways to program MOS EPROMs.

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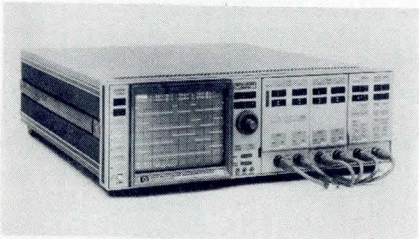
DATA I/O

CIRCLE 26 ON INQUIRY CARD

setups. Each can be recalled with just two keystrokes or one HP-IB command. The third programming method can be added to the architecture as needed through feature ROMs that expand resident firmware measurement capabilities.

Simplified operation was one of the main goals in the design of the instrument. Nontechnical personnel can now make complex production measurements, which previously required qualified technicians. Independent of a host computer, the unit contains several features that make it easy to use. In addition to the capabilities of the save/recall registers and the ROMs, an Autoscope key allows the user to rapidly obtain a display. One keystroke instructs the microcomputer to examine the input signals for vertical amplitude, horizontal sweep speed, and position, and to select settings on the instrument that produce an onscreen display—giving the user an immediate starting point. Selective Autoscope performs a similar function, but allows certain setup functions, such as input coupling and triggering to be preserved during the Autoscope sequence. This facilitates applications such as node probing where autoranging is desired by certain setup parameters that must remain constant.



Improved measurement capability of Hewlett-Packard's 1980A/B oscilloscope measurement system is achieved by incorporating computer architecture design with internal operation controlled by microprocessor and results in easy to use instrument with expandable measurement capabilities. Unit is partitioned into eight independent functional blocks that interface over internal bus. Extensive digital control permits physical separation of front panel and analog measurement circuits. Operating system is contained in 24k of ROM. 3.5k of nonvolatile RAM is used for storage of calibration factors and front panel setups

Software and firmware contributions to the simplification of the instrument are not the whole story. The front panel of the system consists of an array of color coded touch keys arranged in a logical hierarchy with the primary functions for setting basic operating conditions at the top, variable functions in the middle, and setup functions at the bottom. A series of soft keys to the left of the CRT is defined by software and used in conjunction with option menus to provide interaction between operator and installed firmware. A single rotary control is used to adjust all variable functions, depending on which variable function key is activated. Audible feedback is provided by a click when a key is activated.

There are no uncalibrated indicators on the unit because both vertical and horizontal axes are continuously calibrated, improving both timing and voltage measurements and making it impossible to make uncalibrated measurements. Continuously a variable vertical deflection factors from 2 mV/div to 10 V/div are available to 100 MHz. Sweep speeds are variable directly from 5 ns/div to 1 s/div in independent main and delayed sweeps. Continuous calibration not only increases measurement confidence and contributes to accuracy, but speeds and simplifies measurements.

Circle 400 on Inquiry Card

Word Processing Equipment Adds Operator Features, Extends Functions

Word processing—the creation, storage, and communication of words—may take many forms. Equipment typically falls into three categories: standalone hardcopy units, standalone display based units, and shared or distributed logic systems. While each suits a particular type of application, the trend seems to be toward the wide use of distributed logic systems, probably because of the fail-safe nature of such equipment. This trend has been promoted by the increasing degree of intelligence available within individual stations, the decreasing cost of equipment capable of rapidly processing information, and the availability of facilities for electronic communication of text between stations.

Among the benefits to be derived from recently introduced equipment are improved record keeping together with instantaneous retrieval capabilities. The steadily declining cost per byte of magnetic storage has promoted this facility within both standalone units storing data on flexible diskettes and shared or distributed logic systems with their larger capacity hard disc subsystems.

Essential to any user, the printing or hardcopy output function can be filled by a variety of mechanisms with oncoming developments in this area including electrostatic, ink jet, and laser printers. Other factors that play a role in the potential of future systems are communications facilities, access to computers, and the combination of arithmetic functions with word processing functions within a system.

Increasing in rapidity through the past years, announcements of products intended to automate business functions first focused principally on the job of creating multiple copies of standard text. Business automation spread into the creation of formatted and footlined print quality copy for reproduction, and reached the electronic mailbox and electronic filing system and functions for keeping track of executive appointments, messages, and reports. Most of these functions remained separate from the equally essential processing of the volumes of data that made all this communication necessary in the first place. However, each new surge of products has extended the function of the equipment and thus the attendant selection problems. Products providing a transition between the text manipulation functions of the word processor and the records processing power of the computer have increased the flexibility and growth potential of the field. A few, now rearing their heads, offer alluring clues about what the future will bring and when the office of the future will become reality.

Standalone Workstations

R II full-page and R III half-page display word processors function alone or in tandem to increase text throughput and operator productivity.

(continued on page 60)

The Idea:

To take the Digital VT100 and make it both graphical and economical for OEMs and end-users.

Digital Engineering, the pioneers in retro-fit graphics, has done it again. This time, we've turned DEC's VT100 alphanumerics terminal into a sophisticated graphics terminal that features multiple character sizes, dot-dash lines, point plotting, vector drawing and selective erase for quick, easy updating of the graphics display.

But complete emulation of Tektronix® 4010 Series terminals—and compatibility with most existing graphics software, including Tektronix Plot 10™ and ISSCO's® DISSPLA® and TELLAGRAF®—is just the beginning of the Retro-Graphics™ VT100 story. Graphics are displayed on a 12″ (diagonal) green-toned screen at 640 x 480 resolution. Refresh raster scan technology insures a bright, easy-to-read display. And all of the features that DEC's VT100 begins with remain intact, including 96 upper/lower case ASCII characters, up to 132 characters per line, numeric and function keypads, detachable keyboard and a wide variety of screen customizing features.

The Retro-Graphics VT100. Whether you are looking for continuity with existing DEC products, or for a high-quality graphics terminal at hundreds less than the competition, the Retro-Graphics VT100 is the right idea. An idea proven on thousands of Lear Siegler ADM-3A and 3A+ Dumb Terminals.® And an idea taken another step further, once again by Digital Engineering. For more information, write or call.

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CIRCLE 27 ON INQUIRY CARD

Two or three of these keyboard/display workstations, from Burroughs Office Automation Div, can share the same printer. Equipped with dual-hopper sheet feeder, the printer is used at full efficiency and operators can queue documents to it without leaving their workstations. A dual-diskette configuration permits communicating systems to receive incoming messages in background mode without tying up the word processor. Software features provide a forms mode that automates preparation and completion of forms and a math package that enables the system to do basic arithmetic operations and perform calculations within columns.

A dual-diskette configuration permits communicating systems to receive incoming messages in background mode while onscreen editing and formatting continues. Using telephone lines or public exchange networks, the processors transmit at up to 2400 bits/s, operating in either batch or interactive mode from diskette or keyboard.

DEXNET networking capability for electronic mail can be used to transmit typed or printed text, charts, graphic material, even handwritten information at speeds to 20 s/page. Core components of the network are digital facsimile equipment, analog facsimile (FAX) communicators, and operator attended analog FAX equipment. Compatibility between digital and analog equipment permits users to tailor a network to specific message traffic requirements.

Circle 401 on Inquiry Card

Other recent entries in this field are products from IBM, encompassing a standalone text processing system (Office Products Div), a distributed office system that allows word and data processing applications to operate concurrently on the 8100 information system (Data Processing Div), and enhancement to the 5520 administrative system that include file processing with arithmetic functions and additional communication capability (General Systems Div). In conjunction with these releases, IBM has issued a statement in which it outlines plans to provide communications support for filing

(continued on page 62)

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CIRCLE 29 ON INQUIRY CARD

and transmitting documents among the systems existing and those recently announced.

For instance, the Displaywriter communicates with other office systems over telephone lines. The distributed office system enables the 3732 text display station and 3736 printer—elements of the 3730 distributed office communication system—to attach to the 8100 information system. 5520 enhancements provide users with data sort and merge capabilities in addition to text and document distribution functions.

A modular desktop text processing system, the Displaywriter from the Office Products Div is one of the products offering communications capabilities that will become the key to the future. It also provides innovative features that make the system easy to use.

Guiding operators with messages in clear English on the CRT screen, it allows continuous data entry. Capabilities include dividing input into lines and pages and justifying line length. A spelling verification aid can be operator activated. Analyzing the structure of each word, the system compares text to words in a 50,000-word dictionary, highlighting unmatched words at machine speed for operator correction or verification. Users can add 500-word custom dictionaries to cover the vagaries of their specialized terminology.

Circle 402 on Inquiry Card

Permitting users to perform word processing functions concurrently with data processing functions, the distributed office system allows attachment of text display station and correspondence quality printer to the 8100 information system, and expands information processing capability to include word and text processing. Linked to an 8100, it provides users of the 3730 distributed office communication system with a path to increased storage capacity and performance.

Electronic document distribution capabilities combined with file processing and arithmetic functions added to the 5520 Administrative system allow users to blend administrative tasks with other functions. Communications enhancements add bisynchronous communications for document distribution between a 5520 and System/370 and support document interchange between 5520 and System/6, magnetic card equipment, and Displaywriter. Other vendors hoping to gain a share of the market have also placed emphasis on multilanguage capability, communications capabilities, modular problem solving software, and output flexibility, as well as redundant design for protection against system failures.

Circle 403 on Inquiry Card

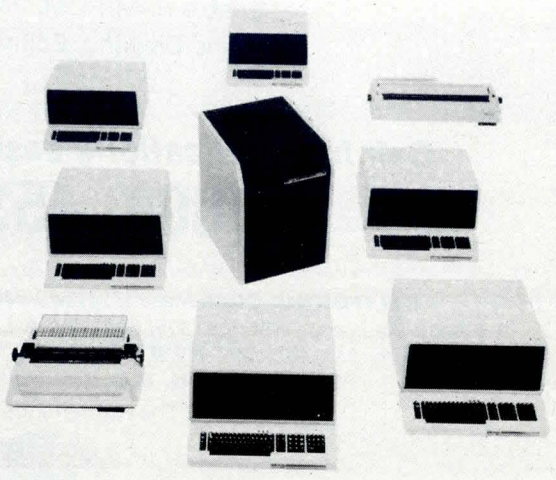
Shared Resource Systems

Enabling users to grow from a single standalone system into a network serving many locations with a common data base, Systems 8 and 64 (NBI Inc, 1695 38th St, Boulder, CO 80301) also maintain the integrity of the standalone systems functioning within the network. Both systems link office workstations and peripheral devices into clusters radiating from integrated control units (ICUs) that offer high speed document access while preserving independent workstation operations. Workstations on the System 8 or 64 may be either System 3000 standalones or the OASys model II workstations that were introduced concurrently. All have their own processors and memory to avoid system degradation. Thus, the systems provide both benefits of resource sharing and those inherent in standalone workstations.

System 8 uses an 8-port integrated control unit that supports combinations of up to 8 workstations and printers with up to 10M bytes of data storage, approximately 4000 pages of document storage, partitioned in up to 32 directories. Two systems can be linked to form a 14-device network sharing up to 20M bytes of storage. System 64 supports combinations of up to 64 workstations, printers, or peripheral devices with up to 70M bytes (28,000 pages) of document storage. System 8 ICUs can be plugged into a System 64 ICU enabling small system users to expand as necessary. Both systems use the low cost model II workstation and a high speed draft printer capable of 300 lines/min. File management capabilities include ability to divide the ICU storage area into up to 32 directories or individual work areas of any size up to full disc capacity. This allows all directories to be scanned quickly to find a given file and provides an efficient method of archiving long documents. The long document archiving command causes a document too long for storage on a single floppy disc to be broken up automatically and stored on several discs.

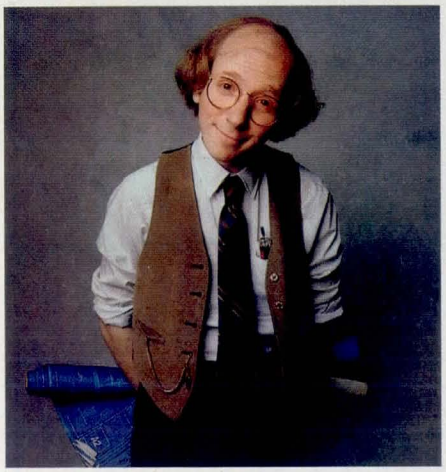
Circle 404 on Inquiry Card

(continued on page 66)



Users can integrate various devices based on NBI's System 8 Integrated Control Unit (center). Radiating from ICU are System 3000 workstations with integral disc storage that function independently as standalone units or as satellites to ICU; printers; and low cost Model II workstation (foreground) designed to function only as satellite processor

Every once in a while some designer finds a spot in a new machine for a sensor, a pushbutton or a keyboard, and none of the 50,000 devices we make will fit. It's always something.



Considering the number of products we make, you'd think we could satisfy all of the people who design machines like computers and copiers.

But no.

Every once in a while, someone still comes up with an idea that our products don't quite fit.

Naturally, we do everything we can to help. Which happens to be a lot considering the years of experience we have in the switching business.

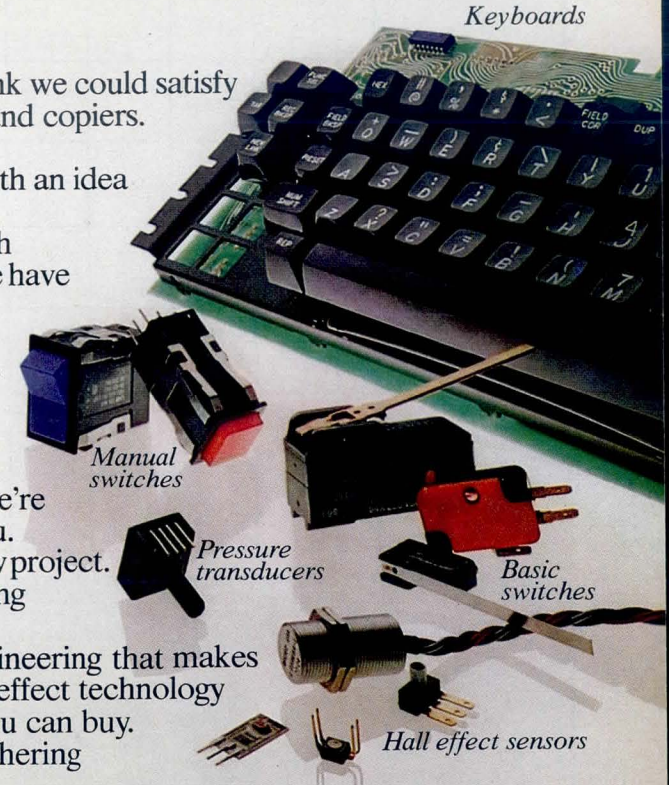
You see, one of the reasons we have so many sensors and manual controls in the first place is because people have always come to us with design problems. And they've usually resulted in new products. Which become part of our product line.

So when you come to us with some new idea, we're in a good position to modify an existing product for you.

Especially if you call us when you're starting a new project. That way, you get our nearly 50 years' experience helping customers solve design problems.

Experience that includes the human factors engineering that makes our pushbuttons easier for people to use. And the Hall effect technology that makes our solid state sensors the most accurate you can buy.

So, if you have a design problem that's been bothering you, call us at 815-235-6600. Or write MICRO SWITCH, The Sensor Consultants, Freeport, Illinois 61032.



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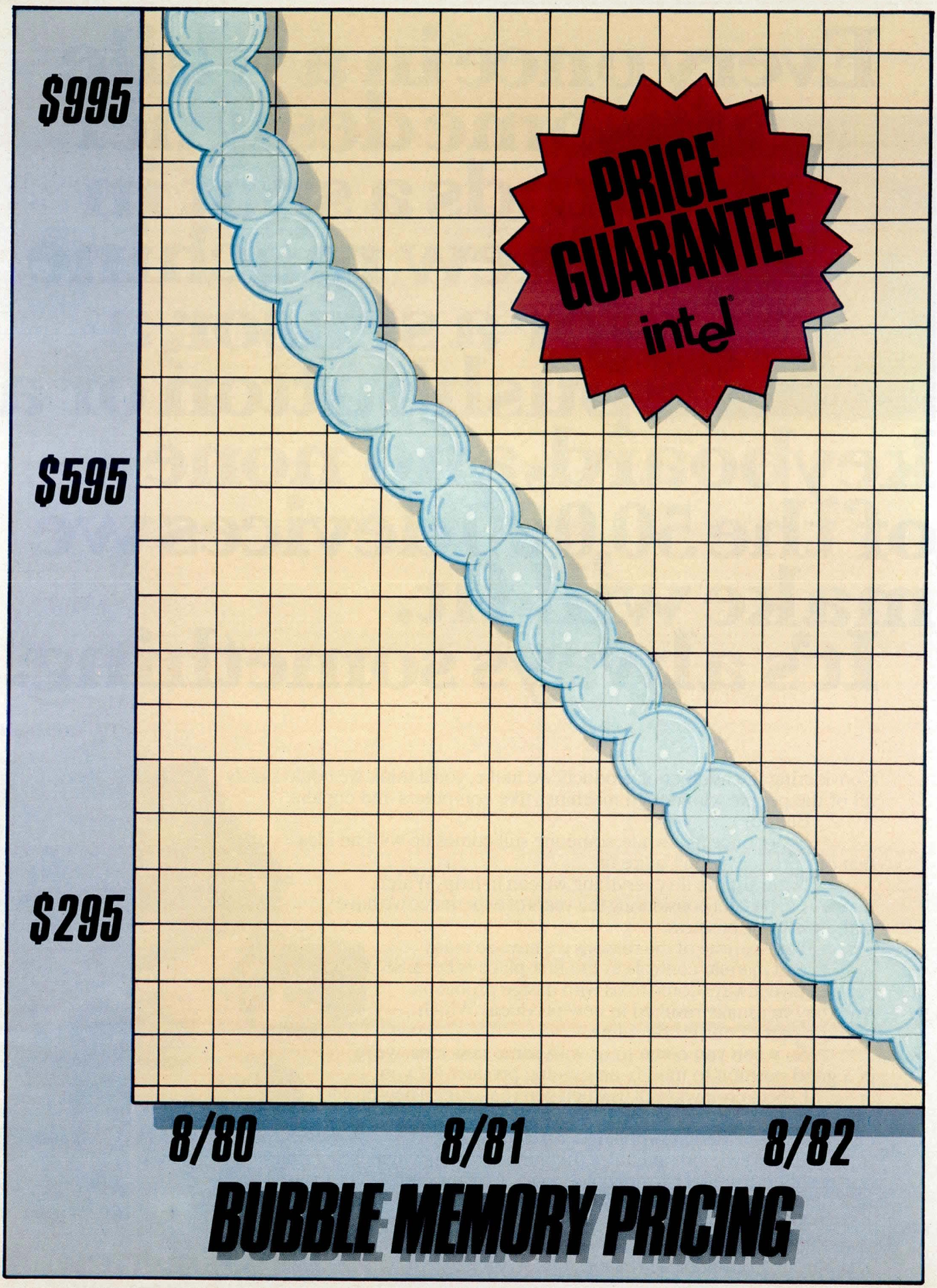
CIRCLE 30 ON INQUIRY CARD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BUBBLE MEMORY PRICING

Bubble Price Break

Intel reduces prototyping prices of 1-megabit bubble memories by 40% now. And guarantees a volume price of $595 for complete component sets by August 1981.

Fast-breaking bubble technology. You've been hearing about it for years. Now Intel announces the kind of break you've been waiting for: a price break.

On August 11th, Intel lowered its 100-unit price for the BPK72 Bubble Memory Kit by 40% to $995—less than 100 millicents per bit.

By August 1981, the price of megabit bubble memories ordered in 5,000-unit lots will be an unprecedented $595. That's 60 millicents per bit. Not "projected." Not "expected." *Guaranteed.*

One year later, for 25,000-piece orders, the unit price will be $295—cutting the per-bit price in half once more. Again, we guarantee it.

How can Intel guarantee such a sharp price reduction? Simple. Intel was the first to bring production 1-megabit bubble memories to market. We've been delivering them for over a year, for a wide range of applications, and now we're moving prices down the manufacturing learning curve.

Get more than bubbles

Intel's bubble memory is a complete set of bubble components for microprocessor-based applications. This set consists of six special support ICs: a controller, a formatter/sense amp., three packages for coil driving and a current pulse generator. It interfaces to Intel® and other microprocessor system buses via the controller, which handles up to eight bubble memory packages, and provides built-in power fail protection and error correction.

The bubble element and its small set of associated ICs can be treated as a peripheral subsystem. This allows designers to concentrate on higher level system objectives, instead of spending time learning the intimate details of bubble device interfacing. Thus minimizing expense in hardware and software development.

Add more value to your product

With Intel's solid-state bubble memory, all that moves is the information. That means high reliability and low maintenance for your products, even in harsh or unclean environments—the kind where disks and tapes won't go. And since the memory is completely nonvolatile, your data

remains secure when the power goes off. No battery backup or replacement is necessary.

Furthermore, Intel's bubble memory system is small, lightweight and silent. By packing over 1 million bits into less than 100 square centimeters of board space, it allows you to reduce the size, weight and power consumption of your products.

As the natural mass storage for LSI microprocessor-based systems, Intel's megabit bubble memory makes it practical to design more features into your equipment. So now you can build in programmability. Portability. Reduced service and repair costs. All with ensured data integrity, even in hostile environments. Consider what that means in your applications.

Start designing now

Everything you need to start designing your next generation product is included in our Bubble Memory Prototype Kit (BPK72), available now from distributor stock. It contains all the components necessary for a 1-megabit system, plus a printed circuit board and complete documentation.

To find out how bubble memories can give you that competitive edge in your next project—and to receive our bubble brochure, contact your local Intel sales office/distributor. Better yet, have one of our field sales engineers give you a firm quote based on exactly what you need for your next product. Write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call (408) 987-8080.

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CIRCLE 31 ON INQUIRY CARD

Focusing on resource sharing, Opus 80 from Hazeltine Corp, Greenlawn, NY 11740, features constant interaction between operator and workstation by means of audiovisual prompts that direct the operator to the correct procedural step and provide explanations when an error has been made. This dialog between operator and system avoids the need to memorize code sequences and thus speeds the learning process. The system's 15″ (38-cm) diagonal CRT provides a full representation of document text and format, displaying a full page of as many as 110 characters by 58 text lines or an enlarged character display of as many as 86 characters by 27 text lines. In addition, a 4-line reference area at the top of the screen constantly displays full status information.

Included in the system's capabilities are the choice of 10 or 12 pitch and proportional spacing, four varieties of underlining (including double), three types of bold print, and two levels of superscripting and subscripting (¼ and ½ line). A scratchpad glossary permits temporary or permanent storage of virtually unlimited capacity with up to 27 separate blocks of text and up to 10 different formats for each workstation; up to 50 scratch pads are stored on the central hard disc, and scratch pads can be archived on removable discs. Global search and replace permits up to 20 stacked text strings to be located.

Standard on this system is a rigid disc with capacity of 14.5M bytes (about 3000 pages), with 29M bytes available as an option. Each workstation contains 64k of memory and performs most of its own word processing functions using a 16-bit microprocessor. Initially up to six workstations and three printers may be connected to the CPU. Workstations and printers share disc storage, processing functions resident at the CPU, and floppy disc archiving. Planned enhancements to the system will include communications, list processing, sorting, math, and other applications packages, an equation writing mode, interfaces to other peripherals, including OCR and photocomposition, and a tape cartridge backup for the entire disc.

Circle 405 on Inquiry Card

In addition to a shared file system that serves up to eight workstations simultaneously, Micom Co, Montreal, Quebec, Canada, provides the 2001E text editor having 128k bytes of memory; the 2002 Twin which runs a pair of workstations from one 128k microprocessor; Micronet, a communications package which converts any of the company's text editors into an electronic mailbox; a software package that offers arithmetic capabilities on word processors; and the Executive Work Station 1, a text editor for executive use.

The 2001E features a Zilog Z80A microprocessor which provides the system with 128k bytes of memory, enough to permit integration of

(continued on page 70)

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There's lots of good reasons to buy your ADD-ON/ADD-IN memory from the leader.

For starters, there's the wide range of core and semi mini-memories we offer. The industry's widest. In fact, Dataram is the only company in the world supplying minicomputer-compatible core and semiconductor main memory and disk emulation systems. The *only* company.

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CIRCLE 33 ON INQUIRY CARD

We have a very simple philosophy about high performance 16-bit micros.

They shouldn't fail.

Since 1975, Digital Equipment Corporation has sold more 16-bit micros than any other company.

More than 100,000 of them.

And from the very beginning, our goal has been simple: to build failure-free microcomputer products.

To approach this goal, we use what we believe is the most comprehensive reliability program in the industry. In fact, we've adapted the same program we developed for our minicomputer and mainframe systems.

And it starts while a product is still on the drawing boards.

Reliability as a design goal.

We actually design reliability into Digital's micro products.

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Then before a component is qualified to go into one of our micros, it has to pass evaluations and tests lasting six months or more.

In production, we give every component a complete battery of functional and package tests. As the micro board moves through manufacturing, we test extensively at every important stage.

Even after a product is in the field, we continue to study its performance and failure rates so we can make design and manufacturing improvements.

All this effort has paid off in extremely high MTBFs. And an industry wide reputation for reliability.

The industry's most mature software.

Reliability is just as important for micro software as it is for hardware.

At Digital, we've been refining and enhancing the RT-11 family of development and application software for more than seven years.

RT-11 provides a wealth of high level languages and development aids. Plus you have the flexibility of using RT-11 with a wide range of LSI-11 hardware configurations.

RT-11 family capability ranges from multitasking, multiterminal support for larger configurations to a very small kernel for single-task applications. There's also a subset of RT-11 designed specifically for PROM applications. This subset, called SIMRT, is an integral part of FORTRAN IV.

And RT-11 development software is exactly the same as RT-11 target software, so you can debug your programs with complete confidence right on the development system.

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Reliable performance is just one of the ways we make micros easier to work with.

We also offer hundreds of hardware products to choose from—micro boards, boxes and development systems. Memory and interface boards. Terminals and printers.

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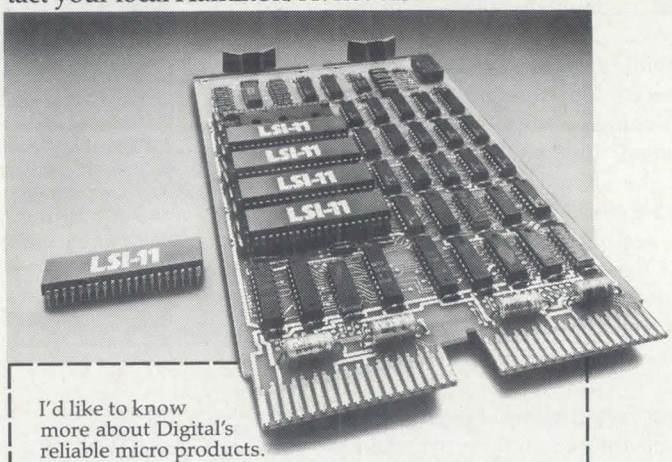

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CIRCLE 34 ON INQUIRY CARD

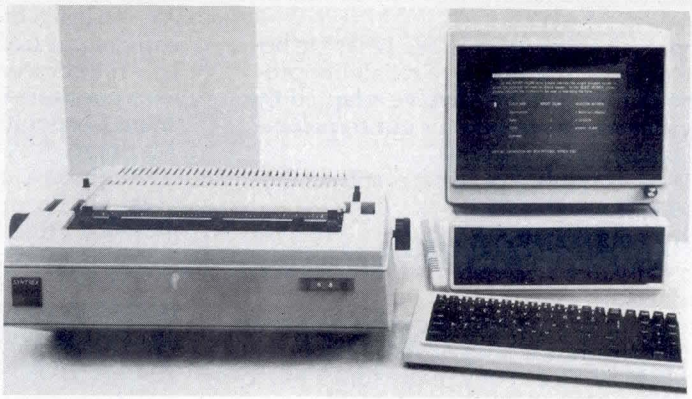
various software programs on one module diskette as well as development of special applications packages for specific working environments. A 128k-byte microprocessor is also used in the 2002 Twin. Two operator workstations share that controller, each with its own disc drive but with access to the other when necessary. Dual-disc capability combined with the 128k-byte memory gives operators advanced functions at a lower cost per terminal in multikeyboard configurations.

Combining large storage capacity and shared file capabilities of a terminal computer with simplicity and operational independence of standalones, the shared file system uses a removable cartridge with 16M bytes of storage and offers 16M, 48M, or 80M bytes of fixed hard disc storage. Up to eight units can use the system simultaneously, with each user able to access both a common and a private library.

Giving executive level personnel access to files stored on diskettes, the Executive Workstation 1 consists of a basic keyboard and CRT which can be plugged into a controller via an adapter. Running the Execupak application package, the system could provide an updated agenda of appointments, phone calls, and letters to be answered, and would organize and store incoming mail by subject and sender, and present a detailed status report of long term projects.

Circle 406 on Inquiry Card

Modular clustered systems that share data base, peripherals, and communications also offer an "Always Up™" redundant design developed by Syntrex Inc, 110 Centennial Ave, Piscataway, NJ 08854, to ensure continuous operation. A CRT based office automation workstation that combines advanced word processing capabilities with management support functions, the standalone Aquarius workstation includes two 160-page diskette drives and interfaces to an IBM Electronic Selectric® typewriter. Features aimed at administrative and management support personnel include natural language electronic filing system, automatic file searching, and optional communications functions. Word processing capability includes display of justified text, single- and double-underlines, footnote references, bold print, horizontal and vertical lines, and even forms. Screen information can be scrolled both vertically and horizontally.



Aquarius office automation workstation combines advanced word processing capabilities with management support functions. Unit includes 25-line tilt and swivel CRT screen and two 160-page diskette drives in standalone workstation for use with optional daisywheel printer and movable editing keyboard or electronic typewriter

Gemini integrates up to 14 Aquarius workstations into a clustered system and provides them with instant access to up to 60,000 pages of storage. Capricorn combines all of Gemini's capabilities with advanced office automation functions like automatic spelling checking, automatic keyword indexing, and electronic mail. Each system contains a built-in duplicate to ensure that office personnel never have to wait for a repair call. If one side of the redundant system detects a problem with the other, it automatically takes over all system functions. And because all incoming information is stored in both sides, the system eliminates the need for elaborate backup procedures and specially trained operators. A service approach, called the Service Genie™, uses the operational side of the system to automatically dial the service center and report any failure or malfunction.

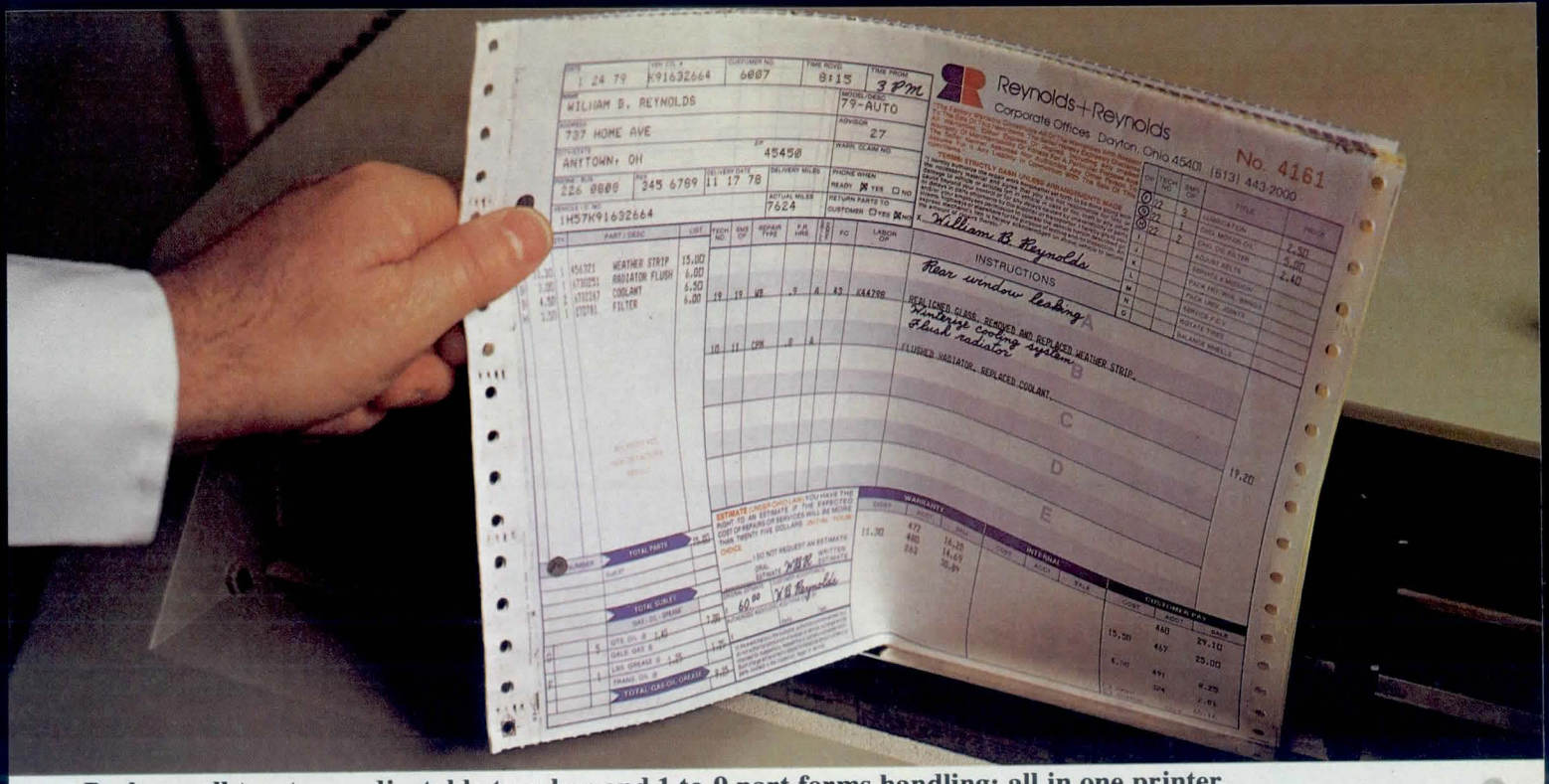
Circle 407 on Inquiry Card

Multifunction Systems

Extending capabilities to continue the multifunction evolution of their RayText systems, Lexitron Corp, a Raytheon Co, 9600 DeSoto Ave, Chatsworth, CA 91311, provides software enhancements that combine distributed data processing with word processing. Systems accept a software upgrade from the Intelligent Terminal Div of Raytheon Data Systems to expand into distributed data processing functions such as user programmability, database management, source data entry, and program development. PTS/1200 systems can accept RayText software and attach VT workstations to add word processing functions to the distributed data processing system.

Support for BASIC language on VT1202 and 1303 text processing systems adds another level of flexibility. Using BASIC capability, units can be transformed into multifunction information systems without additional equipment investment. Users can create their own programs; the system's interactive interpreter simplifies development and

(continued on page 74)



Push-n-pull tractors, adjustable tear bar and 1-to-9 part forms handling: all in one printer.

Finally, real-time forms access plus continuous forms output in one printer. Perfect for such applications as airline ticketing, invoicing, order preparation and more. And another example of the expanding TermiNet 200 printer family's application versatility.

No-waste, flexible forms control

One reason: an adjustable tear bar that lets you use standard forms with different header lengths. For precise alignment, no paper waste and clean paper tear. Every time.

More reasons: servo-driven tractors that allow infinite manual adjustment in both forward and reverse. A non-volatile electronic VFU that makes forms set-up easy and permits storage of up to 8 vertical formats. A down-line loading option enabling you to load formats directly from your data source. Plus straight-through paper path and push-n-pull tractors that give you perfect first-to-last-copy registration. As well as smoother paper handling for all types of forms, including single-part paper.

More features add up to more application versatility

With TermiNet 200 printers, you can also get a 9 x 9 printhead for exceptionally legible underlining and lower-case descenders. Two complete 96-character switchable print fonts for ASCII/APL use or your own special needs. A choice of Magnetic Tape or Edit Buffer Accessory. Plus a 100% duty cycle capability, excellent print quality at speeds up to 200 cps and low cost of ownership. All of which help make TermiNet 200 teleprinters and line printers the industry workhorses.

Immediate delivery instead of piecemeal allocation

Why wait months for other printers when TermiNet 200 printers are available now? When you need them. Mail the coupon today and find out how the expanding TermiNet 200 printer family can meet your range of application needs and generate real cost savings.

Great rip-offs: Just one way TermiNet® 200 printers give you no-waste forms access

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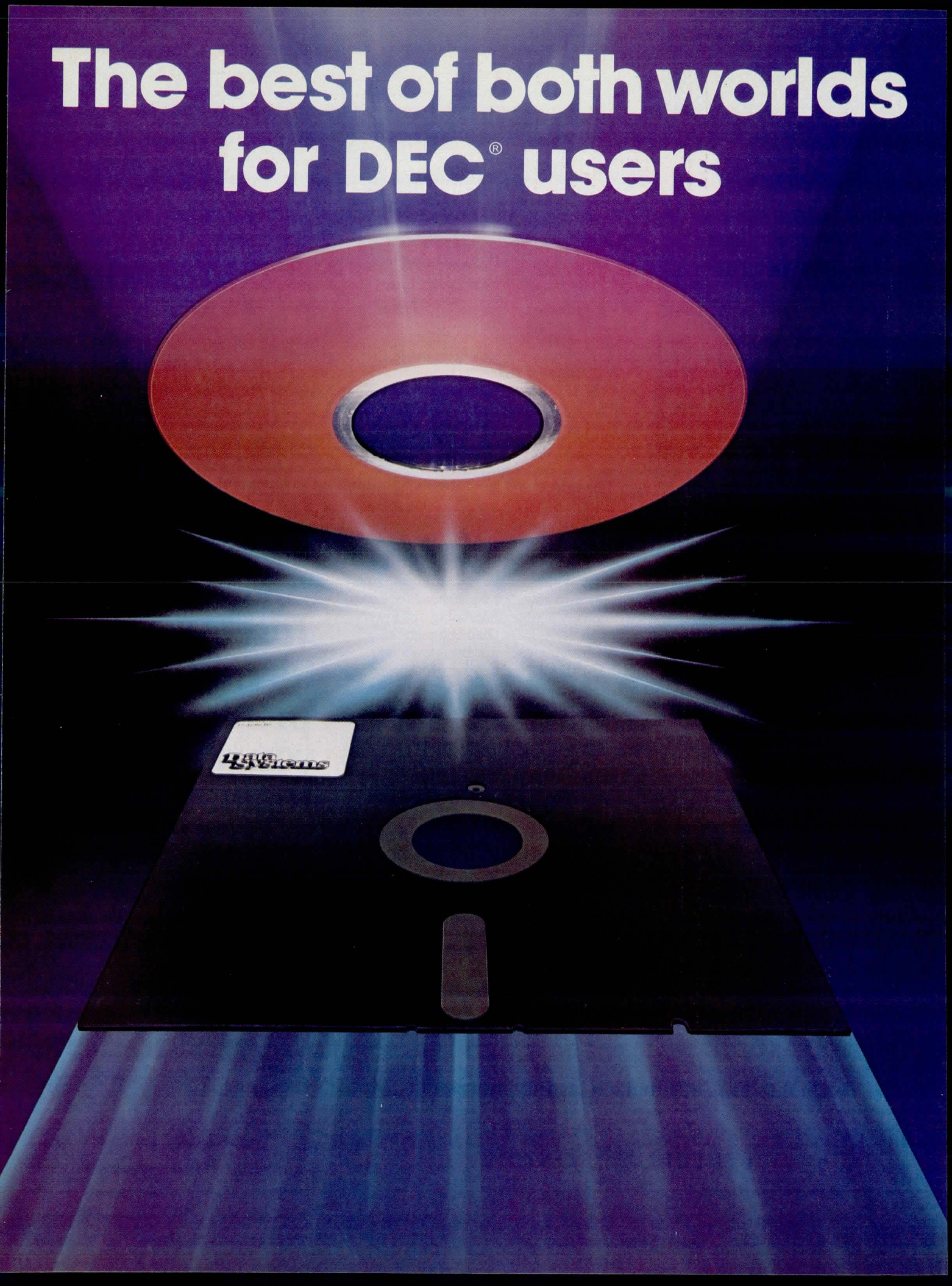

Data Systems Design's DSD 880

Introducing the DSD 880 — A DEC-compatible disk system combining eight-inch Winchester and flexible disks

For DEC users who need more capacity and performance than a dual RX02, the DSD 880 now offers a more cost effective alternative than a dual RL01. Consider these benefits offered by the DSD 880:

- significantly lower initial and total life-cycle costs
- the reliability of a Winchester, with 7.5 Mbytes, emulating RL01
- the removability of a flexible disk, with 1 Mbyte, emulating RX02
- valuable saving in rack space (5¼" vs. 21" for dual RL01)
- unique "hyperdiagnostics" enabling fast and easy trouble-shooting to the modular level
- built-in bootstrap eliminating the need for an expensive DEC bootstrap board and saving a backplane slot
- one half-quad backplane slot vs. two quad boards for the RLV11
- versatile interface card for easy integration with any LSI-11 backplane, unlike DEC's RLV11 interface that needs a special backplane and cannot be used with the VT 103 terminal

Compare for yourself and see why nothing compares to the DSD 880.

Data Systems

The Intelligent Alternative to DEC Disk Systems

To get more information on the DSD 880 call or write:

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VISIT US AT SAN FRANCISCO MINI-MICRO '80 BOOTH 203

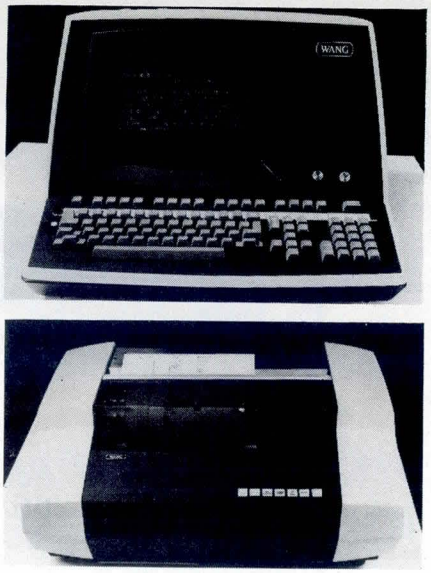
documentation and also permits the system to be used like a calculator.

Another step toward increasing economy and productivity of word processing systems, the VT1630 print multiplexer allows users to develop low cost clustered work groups, minimizes disc handling and printer setup time, and reduces overall cost per workstation. This makes it possible for users to invest in additional keyboards to take full advantage of the productivity benefits of electronic text editing. The multiplexer allows direct attachment of up to six VT workstations (any combination of VT1201, 1202, and 1303 text editors) with up to three standard, wide track, or twin track printers in any combination. Any workstation can select any printer, enabling users to send jobs for continous forms to one printer and other jobs to different printers. When used with VT1303 editors, print queuing is possible, permitting operators to work on other jobs while previous jobs wait to be printed.

Circle 408 on Inquiry Card

Low end additions to the OIS family further solidify the existing stature of Wang Laboratories, One Industrial Ave, Lowell, MA 01851, in the word processing field. OIS 105, designed for small office clusters, distributes function to the point of need and offers increased software performance and hard disc technology at a low price. OIS models 115-1 and 115-2 fill the needs of small to medium range clusters. All OIS systems upgrade easily to Integrated Information Systems (IIS) by incorporating the OFFICE-BASIC programming language, telecommunications, and high speed image printing capabilities, and MAILWAY electronic mail software. These systems combine word processing and data processing capabilities in one device.

The entry level 105 supports two workstations and one printer. User storage is provided through the use of a 2.5M-byte sealed disc. A 300k-byte diskette drive is packaged within the master for easy storage in an office environment. A telecommunications or



Ideographic word processing system from Wang Labs can create, edit, and print documents in Mandarin Chinese, Japanese, or English. Standard 10-key pad reproduces 10,000 characters using 3-corner coding method. Printer outputs in traditional columnar or contemporary horizontal style

phototypesetter connection is available as an option. All OIS software and peripherals, including high speed image printer, twin head daisy printer, and 5541Z phototypesetter are supported. Addition of text editing, hyphenation, and justification provides a complete photocomposition system.

The model 115-1 supports up to eight peripherals in any combination. The system is designed for users requiring systems larger than a standalone, but smaller than a large cluster, and may be expanded by simply adding peripherals. User storage is through a 4.2M-byte sealed disc. Like the 105, the 300k-char diskette drive is packaged within the master. Model 115-2 differs from the -1 only in disc storage capacity. This unit uses an 8.4M-byte sealed disc, and is geared to users requiring online accessibility to a large amount of data and documents.

Circle 409 on Inquiry Card

Foreign Language Units

Hoping to exploit the vast potential of the international market by providing foreign language capability, CPT 8000 and 6000 word processors have been designed to accept, display, and

(continued on page 78)

Tripppple Port

Qantex

RS-232 ~~DUAL PORT~~ TAPE TERMINAL FOR 3M DC100A DATA CARTRIDGE

The new Series 1000 Triple Port Tape Communications Terminal controls and monitors anv RS-232 host system.

Just plug it directly into CRT terminals, minicomputers or printers.

Or communicate via modems, acoustic couplers and telephone lines.

Two of its three I/O ports are bi-directional and independently baud rate selectable. The third port is dedicated for a printer.

Its versatile microprocessor controlled design permits the use of one or two Model 200 MINIDRIVES™ with up to 2.2 megabytes storage capacity.

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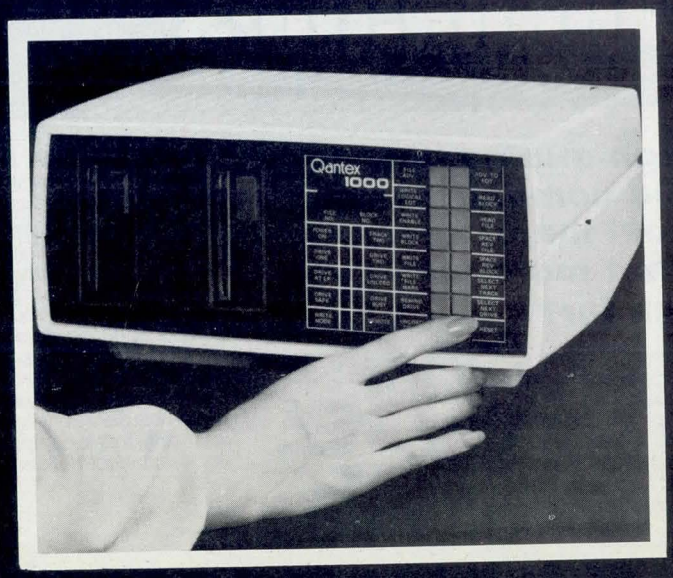


High quality, low cost, and compatible with most major systems. What more could you ask for?

Fujitsu 700 series connectors range from headers and sockets (including 4-sided headers), and polarized card edge types, to DIP plugs, and PCB transitions (staggered or .100″ x .100″ centers). All 700 series headers and sockets meet MIL-C-83503 for lock and eject hook, strain relief and, of course, polarization. And Fujitsu connectors offer three types of polarization: bump, header key or socket key. Truly a full line of flat-cable connectors with outstanding reliability.

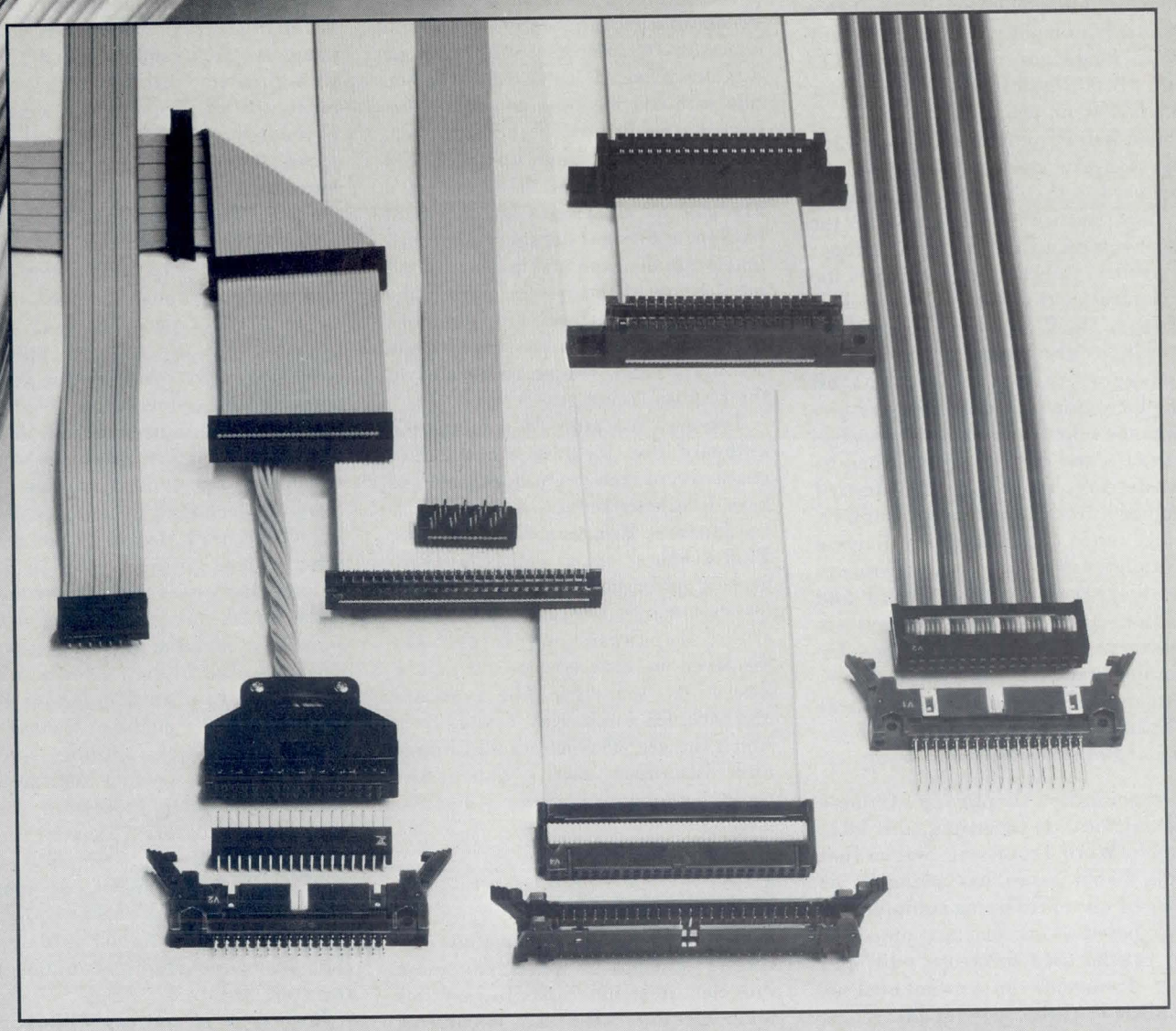
Some of the high reliability is, in fact, due to Fujitsu's unique IDC (insulation-displacement connection). It makes a firm, gas-tight connection between the U-contacts and the wire conductors. That means you have no problems during assembly or after you make your interconnections. Or in the field. And that means you save money. And speaking of saving money, you must look into our 720 series, which is a discrete wire connector, with crimped contacts, that is compatible with our 700 series lock and eject header.

All of the Fujitsu 700 series connectors are UL recognized (E-71597), all are flame retardant (UL 94) and solvent-resistant. The mating surfaces are selectively gold-plated and all PCB terminals are pre-tinned.

The quality is obviously there, the reliability is assured with the Fujitsu name. The cost is low because we are competitively priced. All in all, we feel you'll find our connectors and our service outstanding!

For your convenience, we have a complete stock of the 700 series in Chicago. And a national network of distributor/assemblers.

For complete details on the 700 series connectors, call or write Fujitsu today. It'll be the best connection you ever made.



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CIRCLE 39 ON INQUIRY CARD

FUJITSU

Fujitsu America, Inc., Component Sales Division
910 Sherwood Drive, Lake Bluff, Illinois 60044 Phone: 312-295-2610 Telex: 20-6196. TWX: 910-651-2259

output Spanish, German, Swedish, Danish, and Norwegian. Software necessary to modify the systems to any of 15 languages is supplied by CPT Corp, 8100 Mitchell Rd, Minneapolis, MN 55440, on two discs.

The WordType Table Configuration disc converts each keystroke on the keyboard to the designated characters of that particular language on the display screen, and with the proper printwheel inserted, it coordinates the keyboard with Rotary IV and V printers. The WordType Message Configuration disc converts the system messages into the designated language. Adapting the processor to a language other than English takes less than 60 s and can be accomplished by transferring tables of the desired language from one disc to another. Unlike other systems with multilingual capabilities, the systems can operate in one language for the keyboard and printer and another for system messages. For example, a Spanish operator may type and print letters in German while system messages appear in Spanish for the operator's use.

Circle 410 on Inquiry Card

Dramatically simplifying Chinese and Japanese keyboarding, the Ideographic Word Processing System that Wang Laboratories has added to its stable of word processing equipment is a disc based CRT display text processor that can be used to create, edit, and print documents in conventional or simplified Chinese, Japanese, or English. The system, according to the company, will have a strong impact on the ideographic character area since the standard 10-key pad can reproduce some 10,000 characters, which formerly required thousands of keys.

Extensive conventional Chinese, simplified Chinese, and Japanese dictionaries, each containing over 10,000 characters, have been developed for the system. Each Chinese and Japanese Kanji character has been given a 6-digit identification number. Based on the shape of the character, this coding, indexing, and retrieving system, called the Three Corner Coding Method, uses a standard keyboard layout, and eliminates the tedious means of coding characters and dependence on the recognition of radical Chinese characters.

Based on the Office Information System (OIS), the Ideographic WP System offers a range of standard word processing features in a modular system. Basic configuration consists of a master OIS processor with a single diskette drive, 5536-IWS CRT workstation with 64k memory, and 5531-IP impact matrix printer. Standard system disc storage can range up to 127.5M characters. Optional disc capacity, available on all systems for document backup, additional storage, and archiving, is equally expandable. Distributed intelligence of the system permits the workstation to perform these functions while other users on the same system are performing similar operations in the English language.

The system features a combination keyboard that includes the standard character, operations, and transactions keys. Character keys are used to access the Japanese Hiragana, Katakana, and English characters, as well as Japanese accent, pronunciation, and stylized question marks. The eight phonetically silent Japanese characters are displayed in reduced size through a 2-keystroke sequence. The keyboard also includes a numerical keypad from which the user may access all Chinese and Japanese Kanji characters through a unique character generation method.

Linking Electronic to Traditional Methods

A bottleneck in true information processing systems, in particular those with electronic mail capabilities, forms when operators must rekey documents arriving in traditional paper form for entry into the filing system. Eliminating this roadblock, OCR equipment introduced by Burroughs, OCR Systems, 9 Ray Ave, Burlington, MA 01803, operates online with a word processor scanning typewritten text and transmitting it automatically to the word processor, considerably increasing input and throughput, and providing a bridge or compatibility factor between traditional and electronic methods.

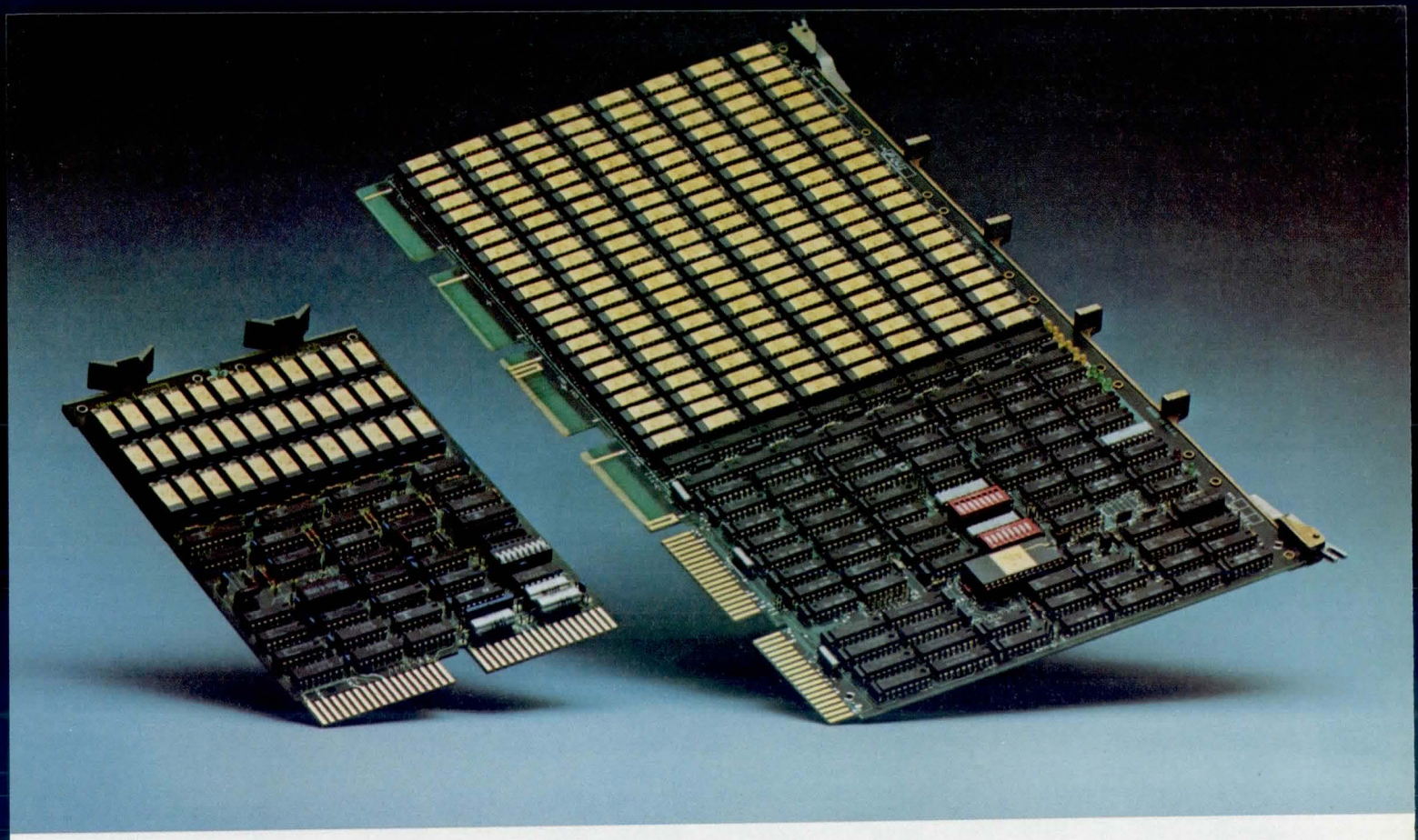
To become a core component in information processing in the office, OCR equipment must be able to read the Courier typeface, a font used extensively on typewriters, word processing, and other printers, and to format material for several manufacturers' word processors. The capacity for doing this—compatibility factor—is provided by the 1220 optical page reader, a low cost OCR scanner that can read and format information for as many as four different makes of word processors. By using the OCR reader in conjunction with currently installed office equipment, the user can reduce repetitive keyboarding, level out workloads, speed turnaround, and dramatically lower the overall cost of document production. The equipment scans copy faster and costs less than other OCR readers, reading up to 3000 words/min, and selling for under $20,000.

The unit accepts typed draft pages prepared on any Courier equipped typewriter, word processor, or printer, converts the information to digital form, and transmits it to text editing systems for further processing or to computers for central storage. The scanning technology employed is extremely accurate. Typically, less than 1 error is made for every 4 to 6 pages of ordinary copy—far fewer errors than a typist would make in rekeying similar amounts of material. As text is scanned it is converted to digital codes, which are recorded on word processor compatible magnetic media or transmitted to an online text editing system. Modems can be used to interface the scanner to remote processing equipment over ordinary communications lines. The scanner is compatible with most standalone, cluster, or shared word processors, and can be equipped with circuits to interface with more than one manufacturer's equipment in the same facility.

Regardless of the capabilities provided by the equipment, the question that will remain of the utmost importance over the long term is whether or not the system is easy to use. Some systems offer menu structures that facilitate their use by noncomputer personnel, while others require the memorization of complex codes or have functions with English labels that are used differently than in ordinary English. If these systems are ever to fulfill their enormous potential, designers must place greater stress on human engineering factors and make a serious commitment to winning general acceptance for the technology in both the office and the executive suite.

Circle 411 on Inquiry Card

(continued on page 82)



More memory on board and a custom-design capability. Memory systems from Texas Instruments.

Quality. Reliability. Compatibility. And more memory on board than anybody else can offer. These are just a few of the many user benefits inherent in TI's new add-in memory modules.
Here's more:

TMM20000 modules

This high-speed module is fully compatible with the DEC PDP-11 family of UNIBUS† computers. And, the TMM20000 offers enhanced system reliability through error detection and correction (EDAC) on board.

High-density, 256K x 16 bits organization *plus* 6 bits for EDAC, make TI's new TMM20000 the densest add-in module ever. Operation from a single 5-V supply with low power consumption is another big plus.

Programmable options include modified or extended UNIBUS, I/O page size, control status register address location, and error status register. Twenty-two address lines allow for expansion to 2M words.

TMM10000 modules

Two versions. Both Q-BUS† and Q-BUS PLUS† compatible. Q-BUS for LSI-11/2. Q-BUS PLUS for the newly announced LSI-11/23. The TMM10000-01 with parity. TMM10000-02, without. Both modules use 5-V only technology storage devices for high performance and low power.

These add-in modules, organized 64K x 16 bit words, with an additional 2 bits for parity (01 only) are the densest available on a standard DEC "dual" board. An optional feature allows extended addressing to 1 megabyte. Fast access and cycle times, too.

Basic storage unit

All TI-designed add-in memory systems employ a state-of-the-art 5-V memory technology. The basic storage unit makes possible such module features as increased board densities, lower power dissipation, improved performance and enhanced system reliability.

These same advantages will be available to users who require production of custom memory systems.

Custom capability

If you need custom memory systems in production quantities, be sure and talk to TI. We'll custom-design modules for specific applications with the same high quality, reliability and meticulous attention to cost-effectiveness that our standard modules offer.

For price and availability information, call your nearest TI Semiconductor sales office or authorized distributor. Or contact Texas Instruments, Box 1443, M/S 6958, Houston, Texas 77001. (713) 490-3746.

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CIRCLE 40 ON INQUIRY CARD

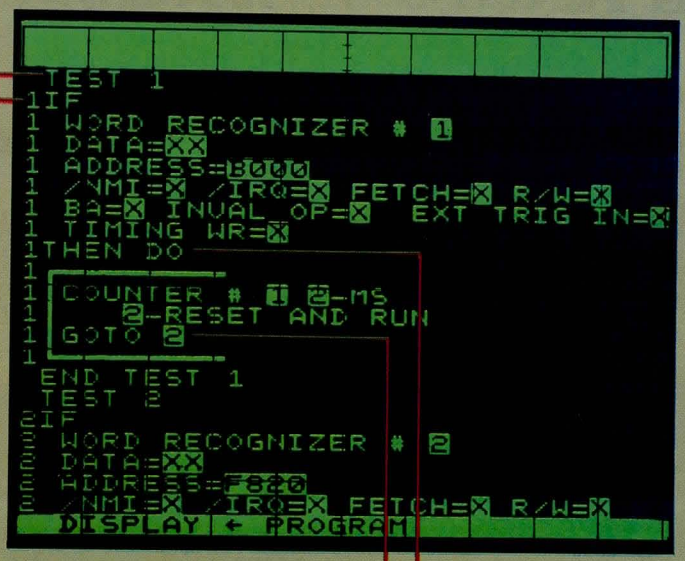
Tektronix' new 7D02. logic analyzer with the

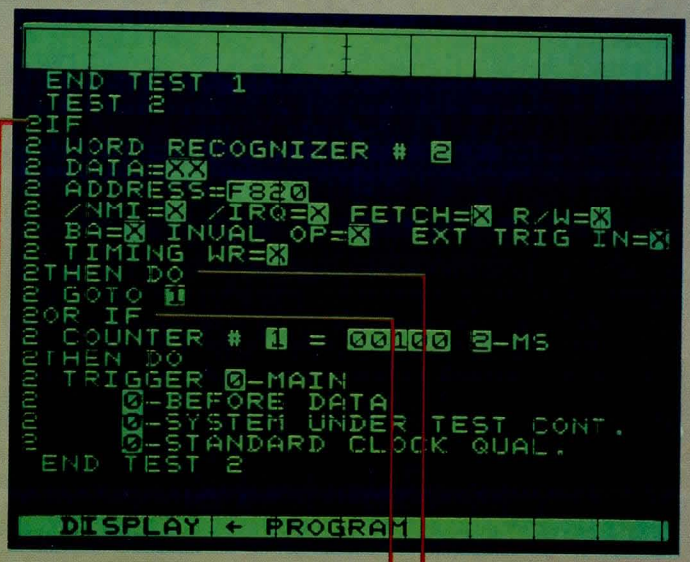
Now, a total solution to problems encountered either on or off the bus. Tektronix' new 7D02 Logic Analyzer. Featuring a unique user language that reduces even the most complex testing to a few simple statements. You supply the overview and the 7D02 does all the detail work for you. With a sophistication never before possible.

A simple, yet sophisticated user language. Writing a test program is no more complicated than responding to a few simple prompts. A handful of basic phrases let you configure the 7D02's resources into almost any combination needed to solve the problem at hand. Often you'll find the 7D02 has an intelligence equal to the software you're integrating into your prototype.

Individualized 8- and 16-bit mnemonics. Through a series of personality modules, the 7D02 can adapt to the characteristics of specific microprocessors. Familiar mnemonics let you work faster and more accurately. Support today extends to the 6800, 6802, 8085, 8086, Z80 and Z8002 with more to come. There's also a personality module available for general purpose logic analysis.

Up to 52 channels of information. Flexibility is the key. You start with the basic 28 channels used for state acquisition, then the expansion option increases this to 44. For timing applications or wider state acquisition, there's an additional synchronous or asynchronous 8-channel timing option complete with its own memory, word recognizer and glitch trigger.





All test parameters supplied by prompts.

IF clause defines a data stream event, which may be either single or compound.

THEN clause defines a response to the event. In this case, setting counter #1 to zero and then incrementing every millisecond.

At the same time the counter is set, branch to the second test. (bracketing allows simultaneous actions).

The 7D02 now monitors the data stream for an event to satisfy the second test's IF clause.

If the event occurs, then activate the trigger.

Or if counter #1 has reached 100 mS, then branch back to the first test and start the program over.

7D02 LOGIC ANALYZER

A user-programmable smartest triggering ever.

And there's more. The 7D02's user language takes advantage of four separate word recognizers, each up to 48 bits wide. Plus two counters usable in either the time or event mode. In addition to clock qualifications, there are two types of data qualification to provide selective data storage.

The Tektronix 7D02 Logic Analyzer can give you a whole new approach to μP-based design.

Locating an intermittent fault. The following program gives a limited demonstration of the simplicity and power behind the 7D02's user language. Here the object is to trigger when a second event on the bus occurs within 100 mS of a first event.

The 7D02 is a 3-wide plug-in for the popular Tektronix 7000 Series oscilloscope. Shown above is a Tek 7603 mainframe housing the 7D02 logic analyzer with a personality module supporting the 6802 microprocessor.

```
CTR1=00100 MS    TRIG LOC = 015
CTR2=00000 EVT   TRIG IN TEST 2
LOC   ADDRESS  OPERATION  /IRQ/NMI
010     F834    BNE   $F82C   11
011     F835     F6   READ    11
012     F82C    INC   $0006   11
013     F82D     00   READ    11
014     F82E     06   READ    11
015T    0006     02   READ    11
016     0006     03   WRITE   11
017     F82F    BEQ   $F865   11
018     F830     34   READ    11
019     F831    TST   $0004   11
020     F832     00   READ    11
021     F833     04   READ    11
022     0004     0F   READ    11
023     F834    BNE   $F82C   11
024     F835     F6   READ    11
025     F82C    INC   $0006   11
026     F82D     00   READ    11
DISPLAY ← ACQMEM 0-MAIN
  1=MNEMONIC
  0 ABSOLUTE
  1 MNEMONIC
```

By using the proper personality module, software flow can be displayed using the mnemonics of the chip under test, here the Motorola MC6802.

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COMMITTED TO EXCELLENCE

CIRCLE 41 ON INQUIRY CARD

For the address of your nearest Tektronix Field Office, contact:

U.S.A., Asia, Australia, Central & South America, Japan Tektronix, Inc., P.O. Box 1700, Beaverton, OR 97075, Phone: 800/547-1512. Oregon only 800/644-9051, 503/644-0161, Telex: 910-467-8708, Cable: TEKTRONIX

Europe, Africa, Middle East Tektronix International, Inc., European Marketing Centre, Postbox 827, 1180 AV Amstelveen, The Netherlands, Telex: 18312

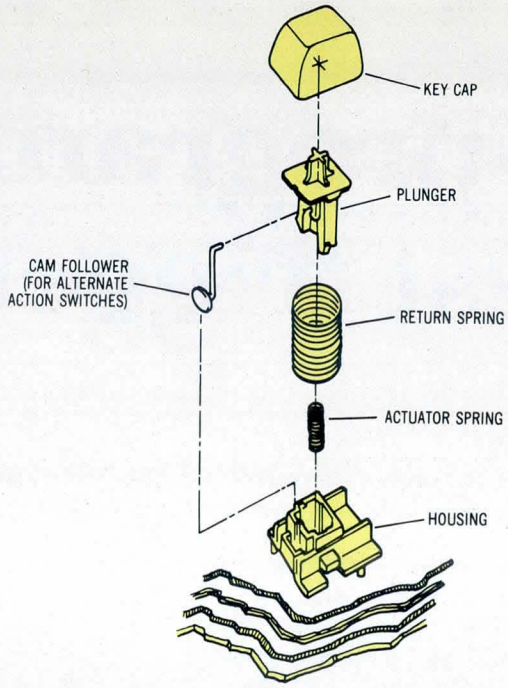
Canada Tektronix Canada Inc., P.O. Box 6500, Barrie, Ontario L4M 4V3, Phone 705/737-2700

Full Travel Keyboard Uses Membrane Technology For Low Cost/Reliability

Full travel membrane (FTM) keyboard, a basic matrix keyboard that combines standard human engineered feel and touch of a full travel key design with membrane switch technology, provides a price/performance mix that is claimed to be unmatched by any other type of keyboard currently available. Developed by Oak Technology Inc, Switch Div, 100 S Main St, Crystal Lake, IL 60014, the keyboard features a full travel (0.160" or 0.406-cm) key with industry standard feel and touch. The switch incorporates pretravel, overtravel, and hysteresis—important when it comes to operator ease and low fatigue considerations.

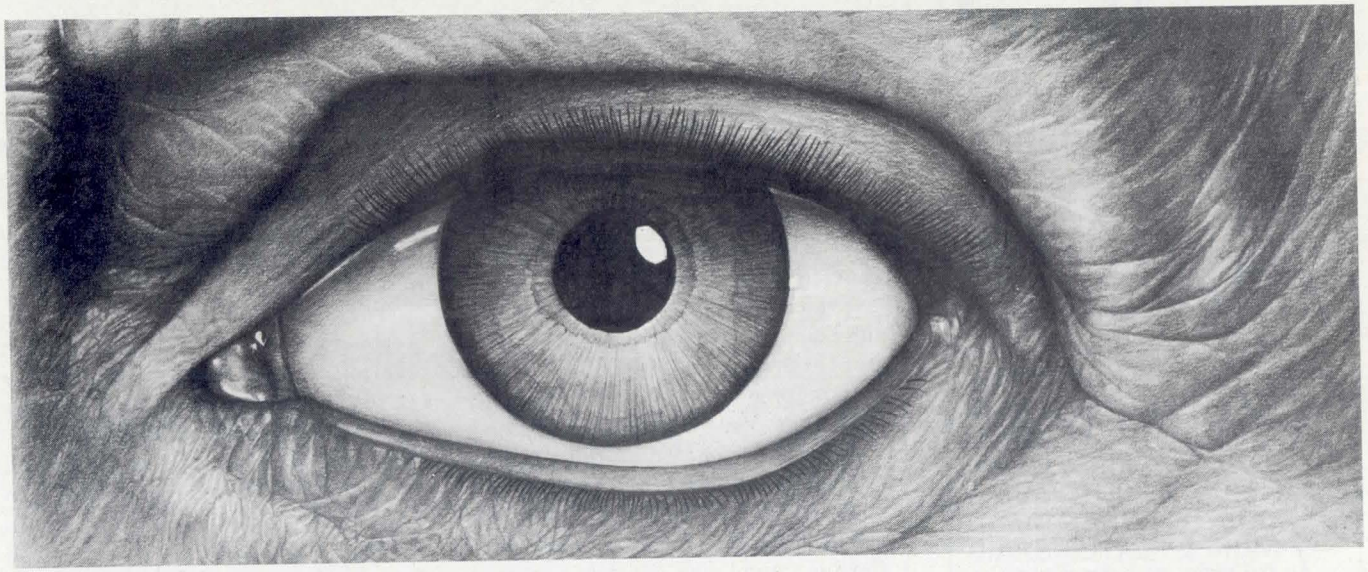
Basic design consists of a plastic housing, plunger, and spring attached to a prepunched metal plate and

(continued on page 84)



Oak Technology's FTM keyboard combines full travel plastic key parts with membrane technology. Basic design consists of plastic housing, plunger, and spring attached to prepunched metal plate and sandwich film base contact assembly

Foresight, foresight, foresight.



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You'll like what you see.

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CIRCLE 43 ON INQUIRY CARD

"sandwich" film base contact assembly. The design eliminates the double-sided, plated through hole printed circuit board and all the switch contacts and mounting terminal normally contained in the switch modules. In addition, it eliminates diodes and their mounting cost by using a software program in the microprocessor to provide N-key rollover.

Typically 5 x 13" (12.7 x 33.0 cm), the base mounting plate is made of a perforated 0.060" (0.152-cm) aluminum plate. The touch in panel (TIP) film contact sandwich and key modules are mounted on this plate by a plastic welding process. The polymer contact subassembly consists of substrate and membrane that have flexible conductive contacts screened on them, held together by an adhesive spacer with holes in it at each key switch position. The subassembly has perforations in it that correspond with the holes in the base mounting plate.

Attached to the mounting plate by a plastic welding process, the housing is a molded plastic part in which the plunger slides to provide a key travel motion. The plunger is held in the up position by the spring and has a key cap attached to its top. On one side of the plunger, a series of small ramps are molded in to provide alternate action. A small plastic part called a cam follower hook is added to any key module to convert it from momentary to alternate action. Pushing the key once causes it to stay down; pushing it again causes it to return to the full up position.

The standard key of an FTM keyboard is 4-mode: shift, unshift, shift control, and alphalock. Reliability is extremely high, with testing showing up to 100M cycles. In addition, the keyboard is front sealed to protect against spilled liquids and other contaminants. Automatic testing procedures assure high quality levels and long life for minimal field service.

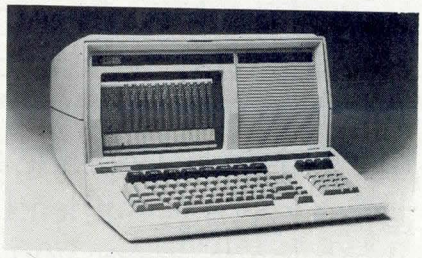
The keyboard can be configured to protect against emi, rfi, and static discharge. It is from 5 to 7 key positions deep and 27 positions long with 52 to 180 keys. Key height of 1.25" (3.175 cm) assures adaptability to low profile designs. The standard microprocessor based keyboard contains the ASCII code which can be modified to specific requirements.

Circle 412 on Inquiry Card

Video Display Terminal Configures Parameters From Keyboard

High performance and high resolution are provided by the software based VP 800/A video display terminal developed by Direct Inc, 1279 Lawrence Station Rd, Sunnyvale, CA 94086. The unit allows the operator or the host computer to configure all terminal parameters and is capable of emulating many other terminals. Its low profile and foldup keyboard adapt it to use in laboratory and office environments.

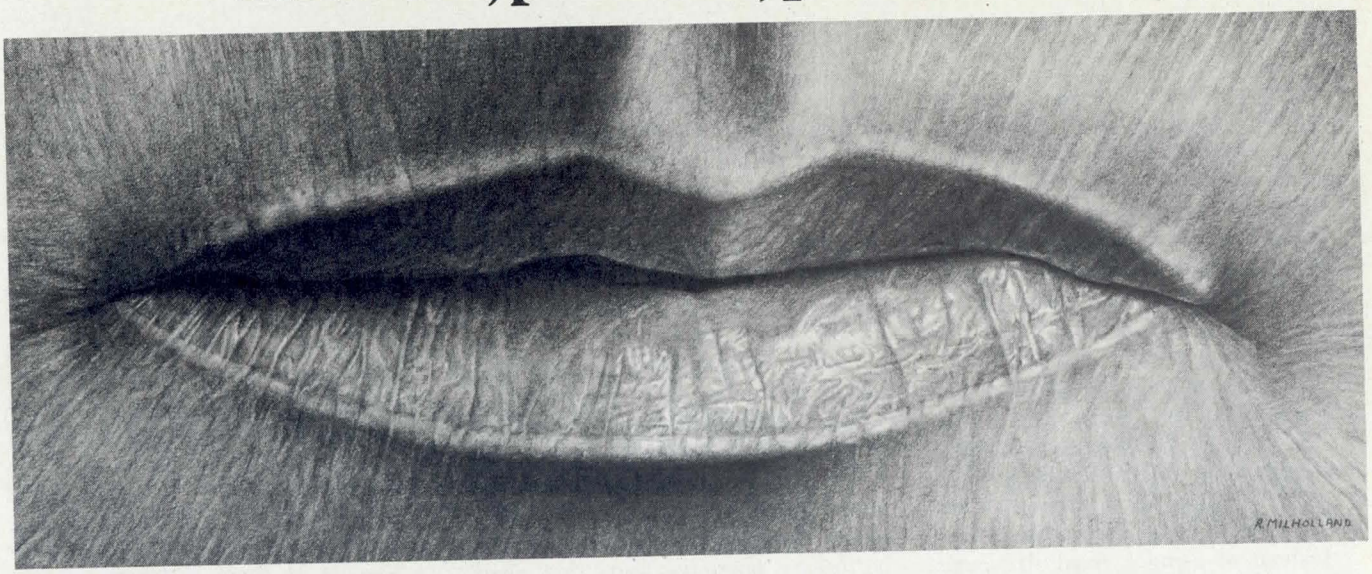
The table driven terminal incorporates those features proven popular in most of today's terminals as well as capabilities not customarily found. Standard machine features include multiple pages of memory, 80-char by 24-line or 132-char by 28-line display with an additional programmable status line, bidirectional smooth scroll at two distinct scrolling rates, and split screen. Full video attributes include double-high or double-wide characters.



Low profile, and foldup keyboard of Direct's VP 800/A video display terminal adapt it to laboratory or office environments. Unit can display 28 lines of 132 characters with an additional programmable status line

(continued on page 86)

Promises, promises, promises.



We've made over 80,000 promises. And we've delivered every one of them.

Pertec® has shipped more tape drives into the minicomputer market than any other independent manufacturer in the world. Tension arm models. Vacuum column models. Microformatters and mini-size drives. Tape drives that set the industry standards. Available in thousands of final feature and specification configurations.

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Four cursor control keys double as scroll keys allowing users to scroll or page backward and forward through memory. A printer port allows online attachment of any serial ASCII printer.

Packed memory manager software efficiently allocates and displays up to 32k of user accessible random access memory. A standard feature of the terminal, the manager provides the ability to use memory to maximize the amount of data that can be stored within the unit. The operator can then review resident data by scrolling either a line at a time (three distinct scroll rates are available) or a page at a time.

Instead of using a fixed size page scheme that saves entire lines, regardless of usage, the memory manager saves only that part of each line that is actually used. Since the average line length of a FORTRAN source program is 37 characters, a VP 800/A with 8k of RAM can save approximately 200 lines or 9 pages of information, while a fixed size page terminal would require over 16k of memory to store the same 200 lines. In addition to providing efficient local storage of information, the packed memory manager supports jump, smooth, and slow scroll rates, 80- or 132-column line width, a full complement of line and character video attributes, and all other machine features including optional buffered printer port and font definition packages.

The keyboard provides a layout similar to that of office typewriters, sculptured keys, and a 10-key numeric pad with user programmable function keys. The keyboard not only detaches from the unit but also has the ability to fold up in front of the display and latch to the terminal for additional space savings and portability.

All operator convenience features can be altered from the keyboard. This allows the operator to configure operating characteristics such as automatic key click, smooth or slow scroll, margin bells, tab stops, auto repeat keys, inverse video, or 80- or 132-char/line modes.

Options for the machine include from 8k to 32k of memory, a buffered printer port, and a font definition package. The font definition package includes variable width/proportionally spaced characters, and allows users to replace standard character fonts resident in the unit with user defined fonts downloaded from the host computer or other external peripheral device. One of the two 128-char fonts can use variable width or proportionally spaced characters that allow programmers to define characters with minimum width of 3 dots and maximum width of 10 dots. This flexibility is particularly useful in environments that require right and left justification and in foreign language fonts that need proportionally spaced characters.

Circle 413 on Inquiry Card

Signal Processing Systems Offer Automatic Waveform Characterization

Designed to provide quick and complete solutions to waveform characterization, three signal processing systems have been developed to fill needs for either extensive waveform processing requirements or fully automatic methods. Totally integrated, the systems, announced by Tektronix, Inc, PO Box 500, Beaverton, OR 97077, are based on the 7612D programmable digitizer.

The 7612D is two digitizers in one cabinet that offers high performance in capturing, digitizing, and storing single-shot or repetitive signals for subsequent computer processing. Sampling intervals are determined by a crystal-controlled clock and can range from 5 ns to 1 s. These intervals as well as all other functions can be selected independently for each channel.

Signals are converted to 8-bit words by an ADC before they are stored in memory. The converter achieves high speed conversion with extreme accuracy at high input signal frequencies. The unit's 2048-word memory capacity can be partitioned. Record length can be set at 2048 words/channel to capture complex signals, or at two records of 1024 words, four of 512, or eight of 256 words to capture fast successive signals such as those found in breakdown phenomena or in complex digital circuits. Within a record, sample rate can be changed at specified locations to provide increased resolution of fast waveform components or to skip portions of the waveform.

A desktop computer based system, the WP3110 signal processing system is composed of 7612D and 4052 graphic computing system. The 4052 is suited for waveform processing because of its extended BASIC language and graphic versatility. With two ROM packs, the system has the power to perform simple to complex waveform manipulations including fast Fourier transforms in a matter of seconds. This combination of waveform digitization, computation power, and graphics provides an interactive waveform graphics analysis system.

When acquisition of large quantities of data is necessary, the WP3200 and WP3201 minicomputer based signal processing systems provide required performance. WP3200, made up of the company's CP4165 DEC compatible minicomputer and 7612, has 34k-words memory while the 3201 with 64k words is comprised of DEC PDP-11/34A minicomputer and digitizer. Both are supported by SPS BASIC software.

Circle 414 on Inquiry Card

Microprogrammed CPU Offers Alternative to Timesharing Users

Model F2, a mainframe computer at a minicomputer price, offers high performance, large software library, range of peripherals, and advanced features such as extended addressing, user

(continued on page 90)

The Cook-able Computer

Configure Your Severe Environment System With Our SECS 80/10A Microcomputer And Support Modules

Buy a few cards or a complete system

Take our ruggedized SECS 80/10A Microcomputer, a functional counterpart of Intel's standard iSBC* single board computer, surround it with our equally ruggedized support modules, and you have the building blocks you need to design a system which will operate under the most severe environments.

This versatile SECS 80 System likes it cold — or hot. Meets Mil-E-5400, 4158, 16400- and more, making it perfect for space, missile and other military systems and tough industrial applications.

A multitude of modules

With these versatile modules, you'll save valuable time and development costs.

- **SECS 80/10A Microcomputer**
- **RAM, ROM & EPROM Memories**
- **Digital Tape Recorder & Controller**
- **1553 Serial I/O Board**
- **Digital Input/Output Board**
- **Analog To Digital Converter**
- **High Speed Arithmetic Unit**
- **Power Supplies**

System packaging

All system modules are mounted on 9″ by 6″ shock and vibration resistant boards. A 7.62″ by 4.88″ 12.62″ chassis (½ ATR) holds up to 6 boards.

Other EMM-SESCO products

We've got core and semiconductor memories for military and commercial use, a Digital Data Acquisition System for the 1553 bus, and a compact Digital Tape System with 23 megabit capacity.

Ask About Our New Low-Cost Industrial Version

*Trademark of Intel Corporation

EMM SESCO

A Subsidiary of Electronic Memories & Magnetics Corporation

20630 Plummer Street • P.O. Box 668 • Chatsworth, California 91311
Telephone: (213) 998-9090 • Telex: 69-1404

CIRCLE 46 ON INQUIRY CARD

Commitment.

It's one of those over-used words in danger of losing all meaning.

Not so for system houses and computer system manufacturers. To you, commitment is the difference between a supplier who leaves you in the lurch. And one who doesn't.

At Century Data, we understand that our success depends entirely on your success. And that broken shipment promises can mean a lot more to you than delayed drives.

Clearly we're in this together. You'll see that attitude reflected in everything we do.

Take our products. No one offers a broader selection of rotating disk drives. Our Trident has earned a reputation as the industry's most reliable removable-pack drive, in capacities from 25 to 600 MB.

Marksman is making a hit as the Winchester with built-in intelligence. It gets you to market quickly, without time wasted on controller development. It's available now—hard-tooled—in 10, 20 and 40 MB capacities, with or without built-in controller.

Hunter is gaining attention as the superior split-pack cartridge drive, combining 16 MB removable and up to 80 MB fixed. And the same reliability and maintainability proven in thousands of Tridents.

We've made the commitment to pump new life into Diablo cartridge drives. We couldn't be more delighted with Xerox's assignment to us of Diablo drive marketing. You can count on us as an eager, dependable source of supply.

The future looks even brighter as we listen to you. And the results are starting to show. The need for lower costs per megabyte led to development of this 600 MB Trident. Priorities have been made out of your need for more self-diagnostics and built-in intelligence. An intelligent Hunter is on the way. And more capacity for the Marksman.

Unlike few other disk drive manufacturers, we are able to draw on the resources of Xerox research to keep us—and you—on the leading edge of storage technologies as they develop.

Customers come to us for our products, then come back because we perform. With service. Support. Dependable delivery. And extra effort.

What it comes down to is this: Commitment may be just a word. We expect you to judge us on our actions. Then see if you can find a better word to describe our approach to this business.

Call or write Century Data Systems, A Xerox Company, 1270 North Kraemer Blvd., Anaheim, CA 92806. (714) 632-7500.

Century Data Systems
A Xerox Company

YOU CAN COUNT ON US FOR THE ENTIRE CENTURY.

CIRCLE 47 ON INQUIRY CARD

microprogramming, and high resolution graphics. The processor is a microprogrammed computing engine that emulates the DECsystem-10/20 computer family with a significant price/performance inprovement. The F2 is available from Foonly, Inc, 999 Independence Ave, Mountain View, CA 94043, as a completely integrated system or as processor and device controllers alone.

Most system functions are controlled by execution of a microprogram in the bipolar CPU. Instruction interpretation, software fault handling, and I/O device interrupt requests are all controlled by the microprogram. By modifying and adding to the standard microprogram, system characteristics can be adapted to special needs, such as efficient execution of inner loop software routines, control of custom devices, or emulation of other architectures. Under control of the standard microprogram, the system emulates the PDP-10 instruction set with an average execution speed about 25% of the DECsystem-2060.

The internal mass storage controller supports up to eight disc drives using industry standard SMD protocol; additional controllers are optional. 160M-byte Winchester drives are standard. Standard tape drives are medium performance 9-track units; controllers for 6250-bit/in, 125-in/s drives are optional. High resolution graphics support is offered as either bit mapped or vector drawing displays. Networking options include ARPAnet and PDP-11 compatible parallel interfaces. A packet stream network interface is planned. Micromachine assists and a flexible bus structure ease interfacing with new devices.

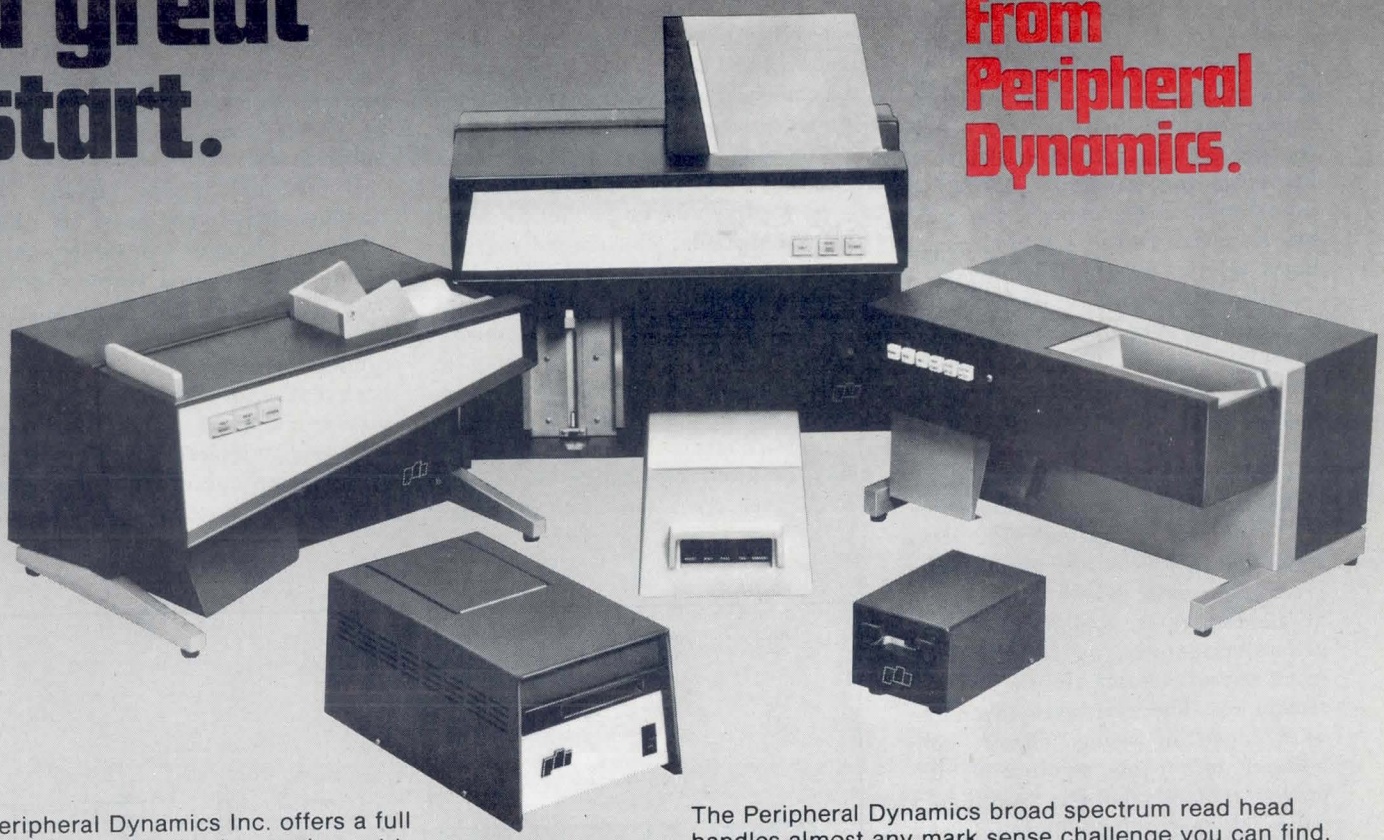
Under an enhanced version of the multiuser, virtual memory TENEX operating system, the system supports a library of software developed for the PDP-10 architecture. TENEX will run most TOPS-20 programs with few changes and includes a TOPS-10 compatibility package. Available languages include FORTRAN, LISP, Pascal, SAIL, BASIC, C, and SIMULA.

Circle 415 on Inquiry Card

Six cost-saving ways (and more!)

to give your data input needs a great start.

From Peripheral Dynamics.



Peripheral Dynamics Inc. offers a full range of data collection equipment to satisfy the most exacting data input applications. If your system requires the reading of punched cards, mark sense cards, badges, or special forms, start with these capabilities:

- Automatic Card Readers — up to 600 cards per minute.
- Manual Fed Readers — reciprocating and straight through.
- Punched hole and/or mark sense read capability models.
- Card/Badge Readers.
- Type 3 Badge Readers.
- All-Weather Badge Readers for hazardous locations.
- Special Forms Readers.
- Data communications interfaces for all equipment.

The Peripheral Dynamics broad spectrum read head handles almost any mark sense challenge you can find, and our forms readers can read everything from newsprint thinness to badge thickness, from 22 columns to 3½ feet, and on a range of colored stock that practically spans the rainbow.

We even have an outdoors, all-weather reader designed for hazardous environments that is unaffected by dirt on the user's badge — it only reads the badge!

With reading ability like that, it's no wonder we say that Peripheral Dynamics helps give you a great start on system performance...and profits.

Just like we've been doing — reliably and responsively — for OEMs and system houses for more than a decade.

pdi®

Peripheral Dynamics Inc.
Sales & Marketing Offices • Whitpain Campus
1730 Walton Road • Blue Bell, PA 19422
Telephone (215) 277-8484 • TWX 510-660-8028

CIRCLE 49 ON INQUIRY CARD

100-MHz Digital Signal Generator Outputs Timing Waveforms for IC Checkout

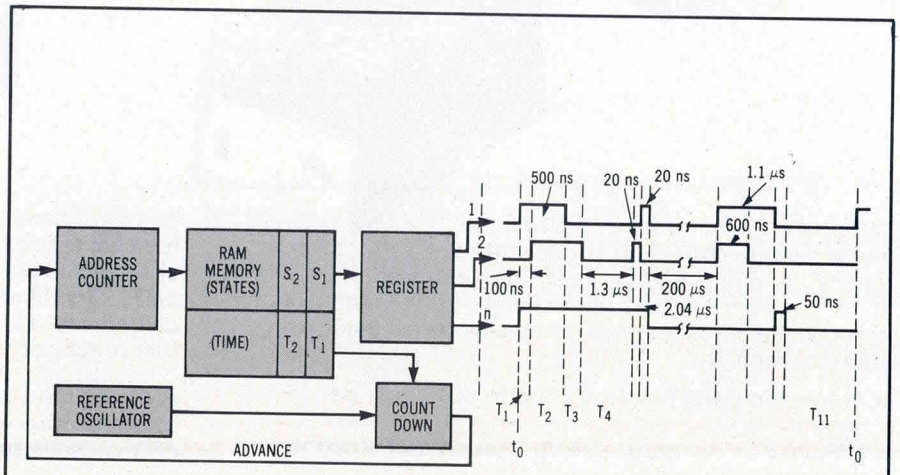
Addition of timing simulation capability to the process of digital word generation provides an added dimension for the test or design engineer, allowing creation of any arbitrary digital waveform needed for the simulation of any digital circuitry—from PC boards to ICs, charge coupled devices, hybrids, or memories. Providing this capability, the RS-680 from Interface Technology, 150 E Arrow Hwy, San Dimas, CA 91773, combines microprocessor intelligence, a built-in CRT, and a front panel keyboard to offer users the operating advantages of an intelligent terminal with the complex waveform generation capabilities of a digital word generator.

The instrument is a standalone, 8-channel parallel programmable timing generator operating with 10-ns resolution, a 16-channel parallel programmable data generator operating at 50-MHz rates, and a serial data generator operating at 100-MHz rates, using microprocessor and CRT control techniques. The unit takes advantage of a blend of semiconductor technologies to provide significantly improved tradeoffs between speed and power. It partitions ECL, MOS, and bipolar technologies such that the user gets the greatest benefits of each without the limitations. For example, an MOS microprocessor is used to reduce power requirements, while ECL in the timing simulator/data generator section provides high speed necessary for checkout of ICs or generation of test patterns.

To operate, the user communicates with the 6802 microprocessor via the keyboard, creating, verifying, and editing his desired signal patterns. The microprocessor and preprogrammed firmware offer prompts to guide him through the necessary setup and data preparation. The user need only select the data pattern and the physical connection to test signals. Once determined, this information is passed to the high speed digital generator which in turn processes and outputs the desired digital signals for stimulation of devices under test. The user can view test patterns as a contiguous table, and can visualize the complete test sequence instead of just one bit or word at a time. Using these known fixed programmed test signals, he can observe the output of the device under test and determine whether it is performing as intended. Finally, any arbitrary digital waveform can be generated by selecting either the word generator mode, which is suitable for synchronous serial or parallel data trains with clock rates of up to 100 MHz or the timing simulator mode, which is suitable for more complex waveforms with up to 10-ns resolution and less than 256 timing transitions.

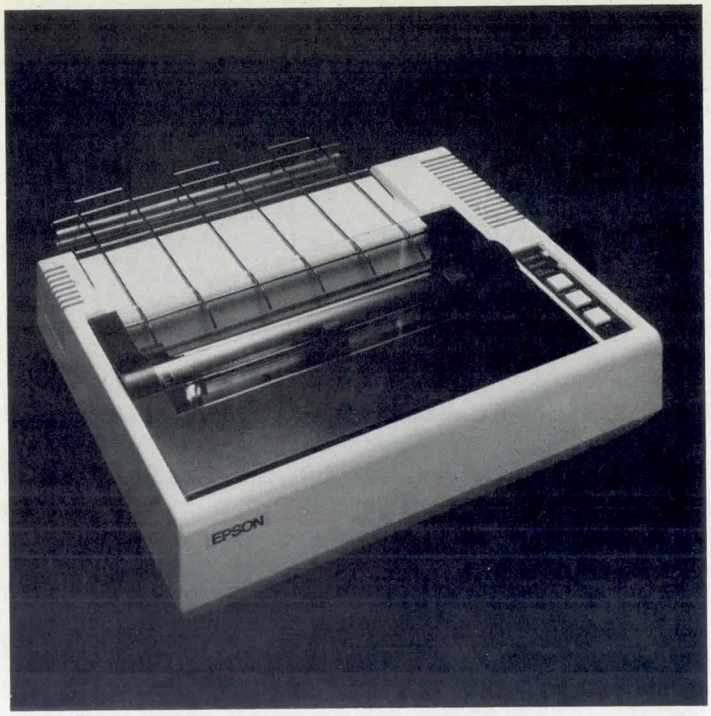
In word generator mode, the unit may be used for 1-, 2-, 4-, 8-, or 16-channel operations with a maximum of 4096 bits. It may be used with its own internal clock or with external clock timing ranging from dc to 100 MHz. In timing simulator mode, the instrument can provide up to 256 states on up to eight simultaneous channels with resolution as low as 10 ns for each state's period. This high level of resolution means that the edges of waveforms being generated can be controlled in increments as fine as 10 ns over periods as long as milliseconds.

Operational modes include continuous, single-cycle, burst, or single-word; triggering may be either manual or automatic external. Outputs include both first word and programmable word synchronization as well as free running synchronous clock output. Both ECL and TTL 50-Ω outputs are provided. Options include RS-232-C and IEEE 488-1978 remote control interfaces as well as an optional stored program EPROM card. Circle 416 on Inquiry Card



RS-680 from Interface Technology provides timing simulation through use of reference oscillator and separate timing memory in which variable clock transition states are stored. Memory access reaches both bits that create waveform and timing information that determines how low specific states stay in output register. Time information goes to countdown circuit which counts against reference oscillator and advances to each succeeding memory state in turn, changing waveform or not, as programmed

The MX-80. It not only does everything, it does everything well.



Epson.

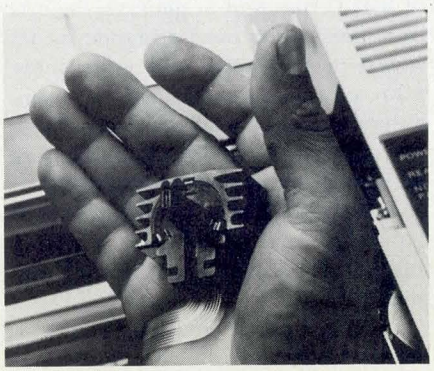
This is the new Epson MX-80 dot matrix printer. It does just about everything you could ask a printer to do. Quickly. Quietly. Reliably. In fact, for OEM installations, the MX-80 may be the single best, all-round printer you can buy. But that's not the best reason to buy it.

The MX-80 prints bidirectionally at 80 CPS in a user-defined choice of 40, 80, 66 or 132 columns. And if that's not fast enough, its logical seeking function minimizes print head travel time. The MX-80 prints 96 ASCII, 64 graphic and eight international characters with a tack-sharp 9x9 matrix. For a long time. Epson printers are known for reliability and the MX-80 is no exception. But that's not the best reason to buy it either.

The print head has a life expectancy of up to 100×10^6 characters, and when it wears out, just throw it away. A new one costs less than $30 and the only tool you need to change it is attached to the end of your arm. The MX-80 is compact, weighs only 12 lbs., and the whole unit, including the two stepper motors controlling carriage and paper feeding functions, is precisely controlled by an internal microprocessor. But even that isn't why you should specify the MX-80.

The best reason is this: because Epson makes more printers than anyone else in the world, we can afford to sell each one for a little less. So you can get one Epson MX-80 Printer for less than $650. And more than one for even less than that.

That's what we call a small price to pay for a printer that does everything well.



The world's first disposable print head. When it wears out, just throw it away. A new one costs less than $30, yet it's so simple, you can change it with one hand.

EPSON
EPSON AMERICA, INC.

Western: 23844 Hawthorne Boulevard, Torrance, California 90505 • (213) 378-2220 TWX: 910-344-7390
Eastern: 98 Cutter Mill Road, Rm. 350, Great Neck, New York 11021 • (516) 487-0660

CIRCLE 50 ON INQUIRY CARD

SOFTWARE

Pascal Packages Support Structured Programming

A Pascal compiler with a high level structured programming language for developing instructional and realtime applications programs and a FORTRAN compiler with Pascal based extensions for structured programming have been developed for use on System 32 series computers. Introduced by Systems Engineering Labs, 6901 W Sunrise Blvd, Fort Lauderdale, FL 33313, both compilers operate under the MPX-32 operating system. Pascal requires 192k bytes and FORTRAN-77+ requires approximately 80k bytes of memory for operation.

Pascal meets or exceeds the Jensen and Wirth standard language definition and FORTRAN-77+ meets the standards of ANSI X3.9-1978, MIL-STD-1753, and ISA S61.1 and S61.2. The ADDRESS function returns absolute memory locations of any variable. Also included are String Escape Characters to allow any 8-bit combination to be used in strings. Compiler directives such as INCLUDE and PAGEUP are supported as are hexadecimal constants. Through External procedures, separately compiled Pascal procedures can be cataloged with a main program. Monitor service access is provided in the form of a predeclared procedure SVC to permit access to all operating system services.

Pascal programs can call FORTRAN-66+ or FORTRAN-77+ or macro assembly subroutines. Any Scientific RTL routine can be called to provide facilities beyond those defined in Pascal, including operating system services, mathematical functions, data type conversions, and realtime I/O routines. Another useful feature is structured level indicators on the output listing.

Pascal based extensions for structured programming enhance the FORTRAN-77+ compiler. Included in the structured programming extensions are a CASE statement, DO WHILE, DO UNTIL, Internal Procedure, IF-THEN-ELSE, and BEGIN-END structures.

Circle 417 on Inquiry Card

Multipass COBOL-74 Compiler Written In Pascal Language

Implemented to ANSI Standard X3.23-1974, COBOL-74 Nucleus and nine functional modules (table handling, sequential I/O, relative I/O, indexed I/O, sort/merge, segmentation, library, debug, and interprogram communication) conform to full level 2 standard. The compiler, developed by Advanced Computer Techniques Corp, 437 Madison Ave, New York, NY 10022, also performs standard COBOL level checking in accordance with FIPS Pub 21-1.

Significant features are multipass structure and object code generation designed specifically for commonly used COBOL structures. These, coupled with Pascal implementation techniques, produce a COBOL compiler that is easy to maintain and enhance. The compiler is being implemented to allow late modifications when COBOL 80 is finalized.

Circle 418 on Inquiry Card

Data Maintenance Software Supports Variable Length Records

Designed to work with RMS-11 records management files, enhanced version of DataTRIEVE query, report, and data maintenance software is available on RSTS/E, RSX-11M, RSX-11M PLUS, and IAS operating systems for PDP-11 computers, and in compatibility mode for VAX-11/780 systems. Announced by Digital Equipment Corp, Maynard, MA 01754, the software enables users to locate, sort, and update information in RMS-11 files and to generate reports from files. It has been designed for inexperienced users as well as for those with extensive knowledge of computers, and has been extended through variable length record support, cross file views, and a revised and expanded documentation set. Cross file view capability enables a user to define logical records that are retrieved from multiple files.

Improved documentation includes a beginner's primer that explains basic system features and a revised reference manual. These documents are supplemented by Guide Mode, a software prompting aid that steps through a subset of commands. A help feature answers users' questions on the use and syntax of commands.

Circle 419 on Inquiry Card

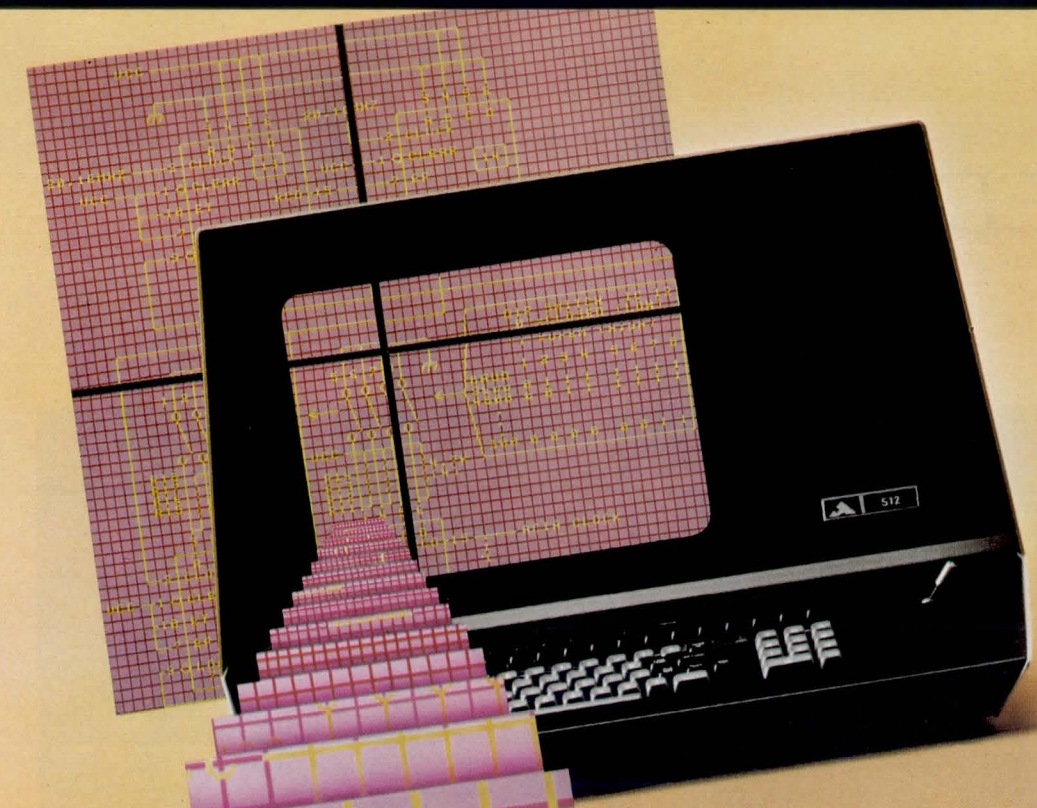
Query Language and Report Writer for Use On Minicomputers

Minicomputer version of the AZ7 query language and report writer facilitates information retrieval, report generation, and file maintenance on superminicomputer systems. AZ7 from Harris Corp, Computer Systems Div, 2101 W Cypress Creek Rd, Fort Lauderdale, FL 33309, interfaces with both the company's file system and TOTAL data bases.

Used with sequential and indexed sequential files, the software offers multifile coordination, data independence, and high level search functions. It enhances TOTAL database applications by providing an interactive query language and report writer with database updating, file extraction, output sorting, and data editing capabilities. Major benefits include significant time and cost reductions resulting from utilization of the program's special features.

The nonprocedural language allows the user to specify what to do rather than how to do it, permitting use by nonprogrammers and resulting in significantly reduced implementation time. It provides a free form, English-like language designed with emphasis on human engineering. Because it is easy to learn and remember, queries and reports can be generated by nonprogrammers. An integrated data dictionary provides for predefinition of information about files and data item characteristics. After one-time-only definition of file dictionaries, nonprogrammers can generate applications. A multiple reports feature allows up to 99 different reports to be generated in a single pass of the input file. Processing time can be significantly reduced when running applications with many reports from a common set of data. □

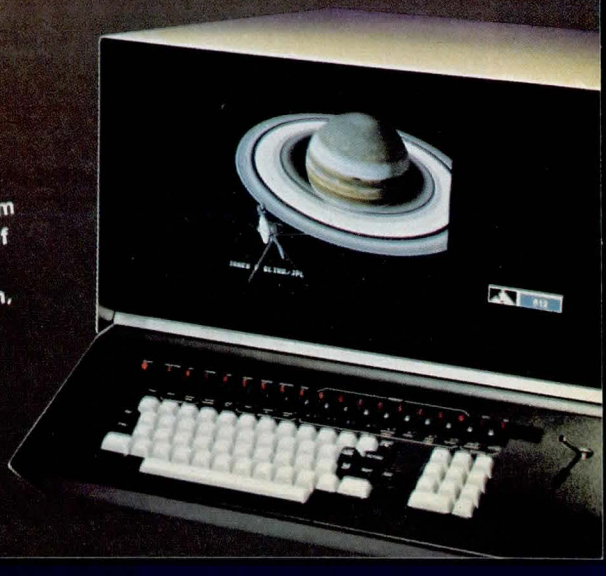
Circle 420 on Inquiry Card



The AED 512... graphics, imaging, Superoam™ and integer zoom in one desktop terminal!

At the Siggraph '79 Show, it was acclaimed as 'The Incredible Graphics Machine!' Since then, the AED512 full-color graphics and imaging terminal has more than lived up to its reputation among sophisticated users. Its ability to display 256 simultaneous colors (from a total palette of 16.8 million) on a 512 x 483 pixel screen; zoom at integer increments to x16; pan continuously via joystick; perform full-screen DMA transfer in 0.5 second; emulate Tektronix 4014 software; allow overlaying TV images with computerized graphics; permit animation by using read/write masks and colorblink make its under $20,000 price tag seem small. Add to this its unique ability to Superoam an expanded image of 1024 x 1024 pixels and you'll see why the '512 is way ahead of the competition. For information call Advanced Electronics Design, 440 Potrero Ave., Sunnyvale, CA 94086. Tel: 408-733-3555. Boston: 617-275-6400. LA: 213-705-0379.

TM Trademark of Advanced Electronics Design



CIRCLE 51 ON INQUIRY CARD

DRESSED FOR SUCCESS.

SUCCESSFUL FRONT PANELS DRESS IN DIALIGHT.

Even the most demanding industrial designer or design engineer will occasionally take switches, indicators and optoelectronics for granted. That's a mistake. Because they are often the first components people see and the ones they use most frequently.

That's why so many designers insist on Dialight standard products and custom designs. They know that precision Dialight products will give their computer, machine or instrument the look and feel of quality.

Choose from over 1,500,000 indicator lights.

Dialight is the world's largest manufacturer of incandescent, neon and LED indicator lights. For over 40 years we've introduced new sizes, styles and colors.

So there's a good chance our collection includes exactly the light you need. If it doesn't, we'll be happy to work with you on an original. After all, we didn't create over a million different designs by refusing special orders.

Rockers and toggles for panel and PC board mounting.

Dialight meets your needs for miniature switches with thousands of different designs in rockers, toggles and levers. All are 100% tested and made in the U.S.A.

Our rocker and toggle line contains a wide selection of actuators, terminations, mountings and contact ratings. Included are dozens of styles for mounting on front panels and sub-panels as well as styles for snap-in and printed circuit board applications.

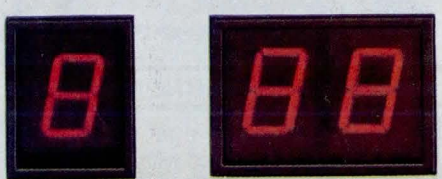
If our catalog doesn't show exactly the switch you need, we'll design and build it to order. All it takes is a call to our Applications Engineering department.

100% testing of every illuminated switch.

Dialight offers a complete line of computer-grade illuminated switches at reasonable cost. And to make sure they all work perfectly, we test every switch both electrically and mechanically before it's shipped.

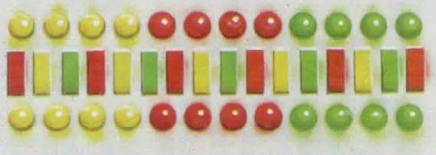
Other switch suppliers may settle for sample testing. That's like leaving reliability to chance. You don't take chances with your designs, and we never will with our illuminated switches.

Depend on Dialight to supply exactly the switch you need, either from our catalog or on special order. Since we manufacture the entire assembly ourselves, we can respond faster and still maintain complete quality control.

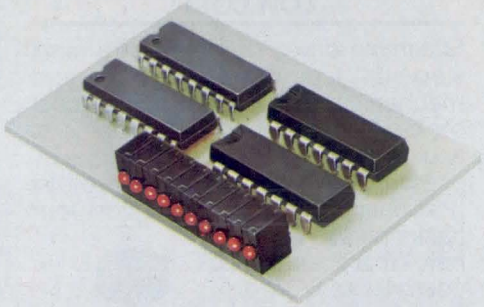


LEDs ready to mount on panels and printed circuit boards.

When it comes to optoelectronics, once again Dialight offers a wide selection plus many unique advantages. For example, we now package LED indicators singly and in arrays for mounting on PC boards. As soon as you insert them into the board, they're precisely positioned and ready for wave soldering. Installation is far faster. And production costs are dramatically reduced.



For front-panel LED readouts, we package 7-segment displays with their associated decoder-driver circuitry and mounting bezel. The entire assembly, with as many digits as you need, is ready for instant panel mounting.



Dress your products for success.

Your products never get a second chance to make a good first impression. So send them into the marketplace looking their best. Dress all your front panels and PC boards in quality indicator lights, rockers and toggles, illuminated switches and optoelectronics from Dialight.

Dialight, 203 Harrison Place, Brooklyn, New York 11237. Phone: (212) 497-7600.

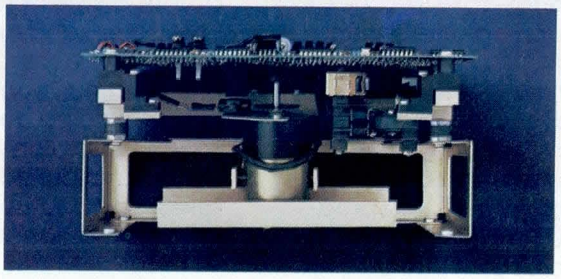
DESIGN IN **DIALIGHT**

A North American Philips company.

See us at Midcom Booth 113.

CIRCLE 52 ON INQUIRY CARD

There are many good reasons to backup Winchester Disks with Cartridge Tape. The Streamer is all of them.



20 MByte Streaming Cartridge Tape Drive.

Meet the Streamer, a product that makes sense every way you look at it. Designed specifically for Winchester disk backup, DEI's new 10 and 20 MByte high density, microprocessor controlled, ¼" streaming cartridge tape drives have impressive advantages over other backup methods.

LOW COST

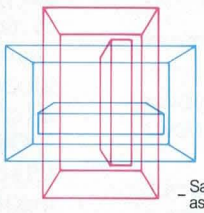
Streaming drives do not require rapid stop/start tape drive electronics and mechanics, resulting in a lower cost servo system, lower power requirements and lower heat dissipation. A unique bi-directional two track head with digital positioner that provides low cost four track operation is also new. What does this all cost? About 1/3rd the price of a Winchester disk for OEM's.

Digital magnetic tach and motor.

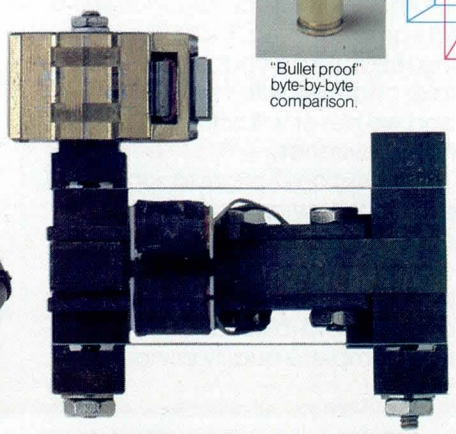
RELIABILITY AND INTEGRITY

The read-while-write capability allows for 'bullet proof' byte-by-byte comparison. Consequently error detection, correction and data resynchronization provides less than 1 error in 10^{10} bits. That boils down to about one error in three years of normal usage! In addition cartridge certification is built into the Streamer, because the data cartridge is calibrated during operation. The improvements don't end here. Our new digital magnetic tachometer increases mechanical reliability because it's operation is not susceptible to dust and dirt problems.

"Bullet proof" byte-by-byte comparison.



Same space requirement as diskette.



Unique 2-track head with digital positioner.

TAPE PROTECTION

The tape is protected against abuse, since it is totally contained within the cartridge. On insertion into the drive, a small door is opened which allows contact with the recording head.

EASE OF INSTALLATION

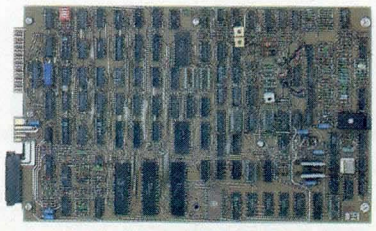
The Streamer is configured to fit the same size enclosure as a conventional 8 inch flexible disk drive. If you have a dual floppy system now, you can upgrade to a Winchester/Streamer 10 or 20 MByte system without additional space requirements.

TRANSFER RATE

The nominal rate is 5 MBytes per minute at a tape speed of 90 ips.

SIMPLE INTERFACING

The drive appears to the host as one of the most familiar interfaces in the industry, a FIFO memory chip.



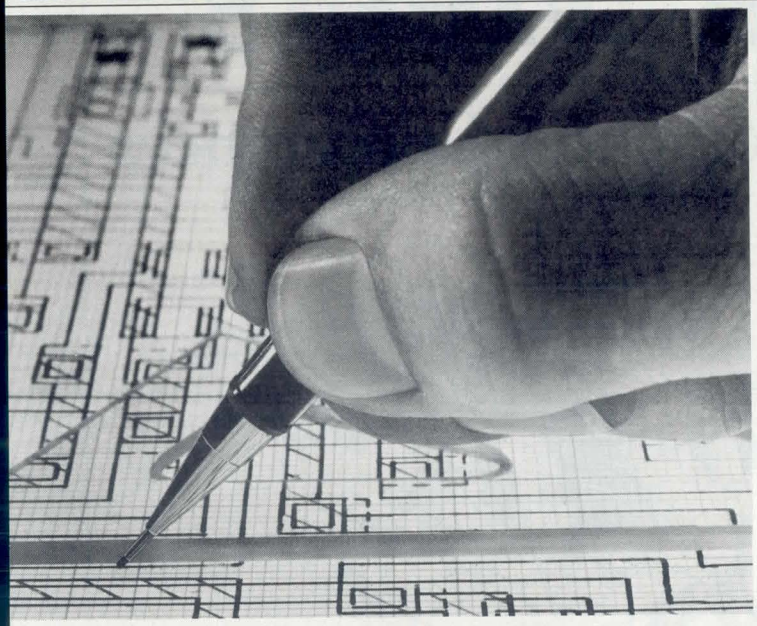
Streaming electronics.

We believe that the Streamer is easy to install, easy to interface, easy to use and easy to afford. Call Whitney Lynn and ask about the Streamer. You'll be in the mainstream of things to come.

DATA ELECTRONICS INC.

10150 Sorrento Valley Road
San Diego, California 92121
Call (714) 452-7840. Telex 69-7118

"Every time we ask a MOS/LSI company about their custom experience, they change the subject."



That's no surprise. Most MOS/LSI companies take on custom work only when market conditions force them to. And, no matter how big they may seem, they're usually only willing to handle a few limited jobs. So they really don't have much custom experience worth talking about.

AMI does. As the leader in the field, we have 14 years of successful custom work behind us. Since we opened for business in 1966, our engineers have designed over 1,300 LSI circuits. And for the entire period of time, custom has been the major—and most important part—of what we do.

We've designed circuits for appliance and consumer electronics companies, the telecommunications and EDP fields, the automotive industry and the military. In fact, we've created custom solutions for virtually every kind of company.

Which means that whatever business you're in, you can be just about certain that we'll understand your problems. And that we'll be able to offer you a MOS system solution tailored to the exact needs of your application.

We can design a MOS peripheral circuit for you that will interface with any standard microprocessor (ours or someone else's). Or we can offer you one of our own standard circuits customized to your specific requirements.

We've also designed complete systems on a chip with as many as 60,000 devices, and we're able to combine both linear and digital circuitry on the same piece of silicon. So if you need a chip with switched capacitor filters, A/D and D/A converters and other linear type circuits, we can give it to you.

What's more, our SIDS (Symbolic Interactive Design System) is the world's most advanced design system. It's the reason we've been able to cut design time while producing increasingly more complex circuits.

We're very flexible. AMI's engineers work in 14 variations of the three major MOS processes: the very mature P-channel, high speed, state-of-the-art N-channel and CMOS. So when the time comes for you to choose the process you want, unlike other companies, we have no limitations to impose on you.

But AMI's flexibility doesn't end there.

If you want to design your own LSI circuits, we make it easy for you to work with us. We can interface with you at any stage of chip development, and we have the industry's only group specially organized to handle customer designed circuits. In six years, they've managed the production of over 750 of these circuits.

You'll be in good company. AMI's list of satisfied customers includes some of Fortune 500's biggest companies. But we work for a lot of small and medium size companies, too. That's another part of our flexibility. We're set up so that we can provide cost-effective, state-of-the-art results for just about any size company—and just about any size job.

If what AMI has to offer sounds like what you've been looking for, mail in the coupon. We'll send you two books that will help you decide if custom MOS is right for your application and tell you everything you should know about AMI's custom capability.

It's really the quickest way for you to start taking advantage of our experience.

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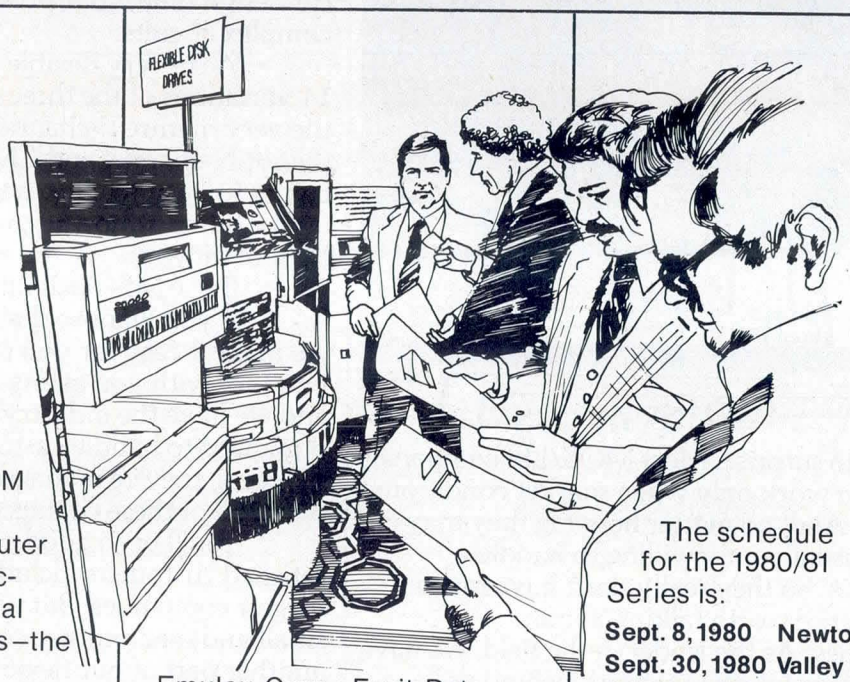
CD10/80

CIRCLE 53 ON INQUIRY CARD

OEM America Meets

At The Invitational Computer Conferences



In Boston
...in Ft. Lauderdale
...in Palo Alto and
seven other cities, OEM decision-makers meet the country's top computer and peripheral manufacturers at the Invitational Computer Conferences–the only seminar/displays designed specifically for the unique requirements of the quantity user.

In one day, at each 1980/81 ICC, guests will receive a concentrated, up-close view of the newest equipment and technology shaping our industry. Some of the companies which participated in the 1979/80 ICC Series were: ADDS; AVIV Corp; Applied Data Communications; BASF Systems; Cambridge Memories, Inc.; Centronics; Century Data Systems; Cipher Data Products; Compugraphic; Computer Devices; Control Data Corp.; Data Systems Design; Dataproducts Corp.; Dataram; Datasystems Corp.; Diablo Systems; Documation; Emulex Corp.; Facit Data Products; Florida Data; Hewlett-Packard; International Memories, Inc.; Kennedy Company; Lear Siegler; MDB Systems; MFE Corp.; Microdata; Monolithic Systems; Mostek; NEC Information Systems; National Semiconductor; Olivetti; Perkin-Elmer Memory Products; PerSci, Inc.; PCC/Pertec; Pioneer Magnetics; Plessey Peripherals; Powertec; Priam; Printronix; Remex; Rianda Electronics; Scientific Micro Systems; Shugart Associates; Siemens; Storage Technology; TEC; Tally Corp.; Teletype; Telex Computer Products; Texas Instruments; Trilog; Universal Data Systems; Versatec; Xylogics.

The schedule for the 1980/81 Series is:

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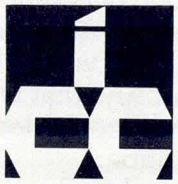
Sept. 30, 1980	**Valley Forge, PA**
Oct. 22, 1980	**St. Louis, MO**
Nov. 18, 1980	**Palo Alto, CA**
Jan. 13, 1981	**Orange County, CA**
Feb. 3, 1981	**Ft. Lauderdale, FL**
Feb. 5, 1981	**Atlanta, GA**
Mar. 3, 1981	**Dallas, TX**
Mar. 5, 1981	**Houston, TX**
Apr. 2, 1981	**Denver, CO**



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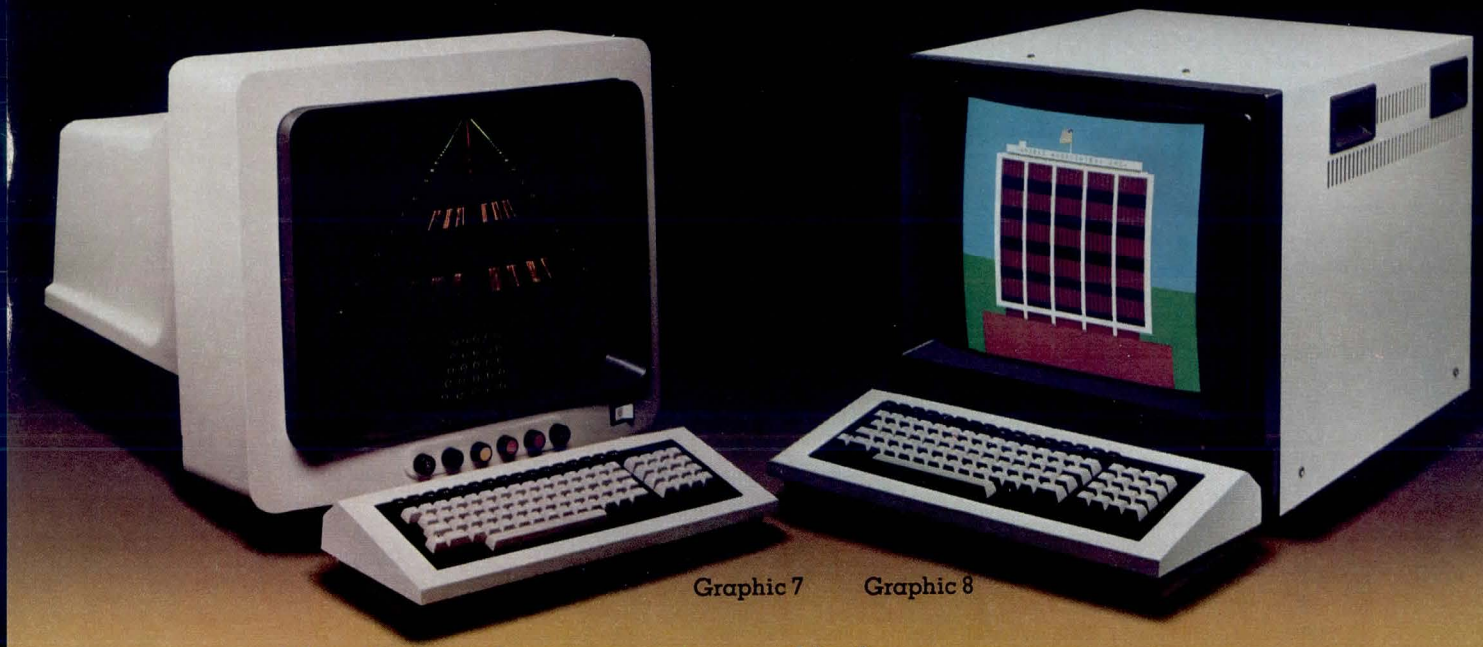

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Plus upward-instruction compatibility with the Sanders stroke refresh Graphic 7 and its color and 3D options.

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CIRCLE 155 ON INQUIRY CARD

Where ISOs meet their Makers.

Las Vegas is the place, COMDEX is the show, where thousands of ISOs (Independent Sales Organizations) will meet hundreds of exhibiting vendors. Purpose: Find new product lines to sell; learn some "survival tips" for the 1980's; see what the competition is showing. That's what COMDEX is all about.

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COMDEX is the unique conference and exposition that in its debut last year defined and brought together the explosively growing world of the ISO -- the key marketing channel for the computer industry in this decade. Dealers, distributors, commercial OEMs, systems houses, software packagers, turnkey vendors, manufacturers' reps, computer retailers and office machines/product dealers -- they came to Las Vegas in 1979; they'll be back in greater numbers in 1980.

More than 250 exhibitor companies will be there, all eager to expand their ISO marketing channels. They will be displaying and demonstrating small computer and word processing systems, peripherals, software packages, media, supplies, and many other products and services of interest to ISOs.

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And, once again, COMDEX will offer a comprehensive Conference program, 39 sessions in all. Geared to the special business interests of the ISO, more than 100 of the nation's leading experts will discuss how today's difficult business climate poses both challenge and opportunity.

Now you know why a leading industry publication last year called COMDEX the show that "had to happen." If it had to happen last year without you, make sure that this year it will happen with you!

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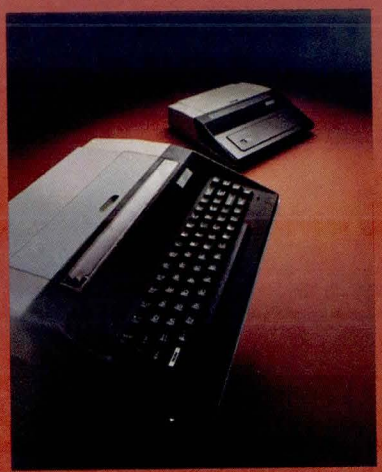

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CIRCLE 157 ON INQUIRY CARD

HOW TO COPY THE MICROPOLIS 8" RIGID DISK DRIVE.

It's bound to happen sooner or later. Someone will decide to copy our 8" rigid disk drive. It happens to all industry-standard products.

So we're going to save someone the trouble and tell exactly how we built our 8" drive. But we're not worried. Because, frankly, we don't think anyone else will want to go to the trouble we did to give you such a product.

First of all, our family of 8" rigid disk drives (9 to 45 megabytes) comes with features you simply can't find in the competition's products. Such as our low-cost intelligent controller board, designed to allow swift integration into your existing system.

In addition to low power dissipation and fastest access time, we also included a Quartz-locked, direct-drive, brushless DC motor. We gave our rigid disk a braking mechanism, too. It extends the life of the disk by not allowing the head to act as the brake. That's a longer disk life for you, and a higher MTBF in the critical clean area. Next, we included our balanced rotary voice coil positioner, which, together with the closed-loop servo, absolutely protects against unexpected jolts, bumps, and shocks during write operations which might otherwise result in off-track writing.

We enclosed the heads, platters, and positioner assembly in a sealed clean area. No other drive has all active components outside the clean area, for easy access and maintenance. So we can offer the longest drive warranty in the business.

All this adds up to unprecedented quality, reliability, and stability. And our 8" rigid disk fits into the exact same space as an 8" floppy drive—they even use the same screw holes.

So if you want the best 8" rigid disk drive, call us. We deliver.

If you want to try and copy it, good luck. You'll need it.

MICROPOLIS™

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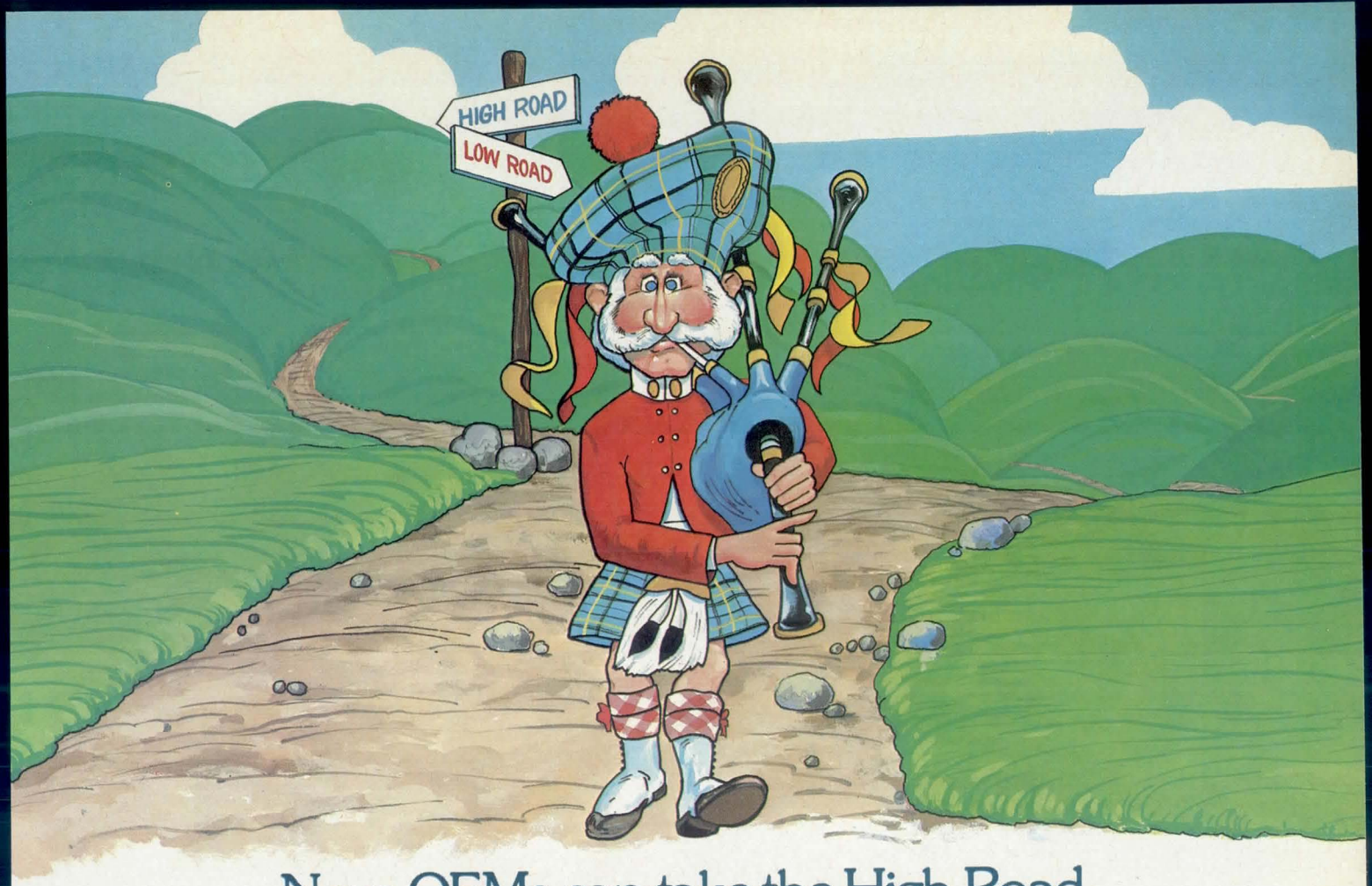
Chatsworth, California 91311
(213) 709-3300. Telex 651486

CIRCLE 158 ON INQUIRY CARD

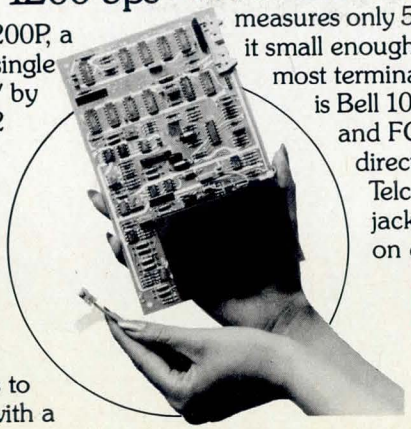


Now, OEMs can take the High Road or the Low Road with our Direct-Connect Modem Cards, small enough to mount inside Data Terminals.

As the auld Scottish tune suggests, Racal-Vadic now makes it easy for OEMs to take the high road (1200 bps) or the low road (300 bps), with low cost direct-connect "Modems-on-a-Card," small enough to mount inside CRT displays, teleprinters, POS devices, and other terminals and systems.

The High Road: 1200 bps

Meet the compact VS1200P, a complete modem on a single PC board measuring 5" by 8.35." That's a thrifty 42 square inches of space. It's fully compatible with Bell 202C and S modems. Only better, offering much more in performance, flexibility and test capability. It's registered for direct-connect, too. Connects to the switched network with a cable that plugs right into a Telco voice or data jack. Built-in 20 pin ribbon connector easily interfaces the VA1200P to your terminal. Price is right, too. Just $200 in quantities of 100.



The Low Road: 300 bps

The VS300P is a 300 bps full duplex, automatic originate/answer "Modem-on-a-Card." Like the VS1200P, it measures only 5" by 8.35," making it small enough to mount inside most terminals. The VS300P is Bell 103/113 compatible, and FCC Registered for direct connect via a Telco voice or data jack. Mounting holes on each corner make it a cinch to install. And the price would put a smile on the face of the thriftiest Scotsman. Just $200 in lots of 100.

Both Roads: The TI Story

Two of Texas Instruments new Silent 700* data terminals include Triple Modems custom made by Racal-Vadic. Although small enough to fit into TI's portable 17 pound terminal, this remarkable modem combines a Racal-Vadic VA3400, a Bell 212A, and a Bell 103. Imagine, a full originate/answer direct-connect modem with both 1200 bps full duplex and 300 bps full duplex in such a tiny package. And it can even be acoustically coupled.

We did it for TI, and we can do it for you. Phone or write today.

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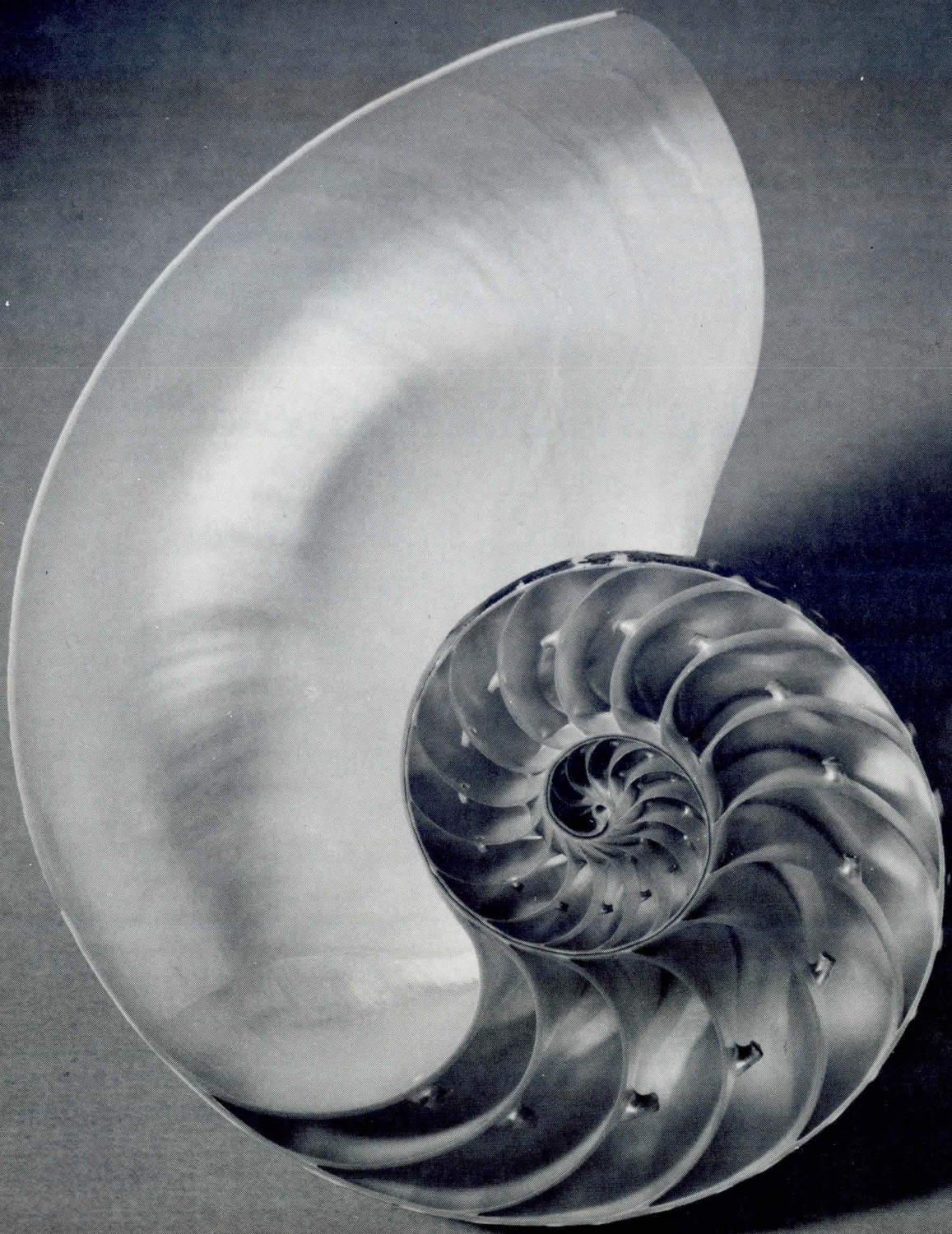
RACAL
The Electronics Group

CIRCLE 55 ON INQUIRY CARD

EXPAND YOUR DATABASE GRACEFULLY

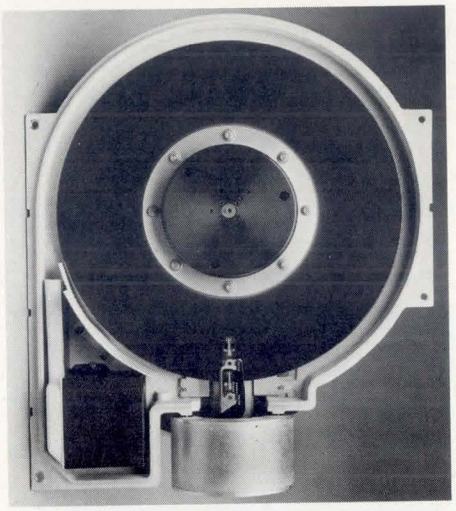


WITH PRĪAM'S DISKŌS 3350 DISC DRIVE

When the developing chambered nautilus requires more space, it simply expands its shell, moves into the new and larger chamber, and seals off the cavity it previously occupied. Expansion of your computer database capacity is even simpler and more efficient with PRIAM's DISKOS 3350 Winchester disc drives.

When the DISKOS 3350's capacity of 34 megabytes is outgrown, the DISKOS 6650, a second version, will store 68 megabytes of data. The DISKOS 15450 disc drive will have a capacity of 158 megabytes. Unlike the chambered nautilus, PRIAM's disc drives don't leave any empty chambers behind. The same basic mechanism and electronics are used in all three versions, making packaging, interfacing and field support easy and economical.

With an elegance of design similar to that of the nautilus, the DISKOS 3350 lowers disc data storage costs to levels that permit small business computers, word processing systems, low-cost computer systems of all kinds to take on new applications and bigger problems. Here are the important elements of this dramatic new approach to data storage.

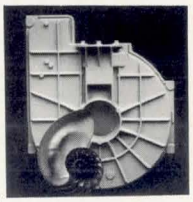


High Data Density

Using high level Winchester technology, PRIAM's DISKOS 3350 stores 34 megabytes (unformatted) of data on a single non-removable disc. Data is written and read at 480 tracks per inch and 6430 bits per inch. With its track-following positioner, PRIAM's DISKOS 3350 mechanism graduates naturally and economically to much higher capacities and still retains its high reliability.

Fully Servoed Linear Voice Coil Head Positioning

Only the PRIAM 3350, among low-cost Winchester disc drives, makes the advanced technology of track following, voice coil positioning available for graceful expansion of your database. PRIAM's linear positioner permits 34 megabytes to be stored economically on a single disc, using only four heads. Other low-cost drives use two discs and nine heads to store less data than the DISKOS 3350. And the precision and repeatability of PRIAM'S track-following, voice-coil head positioning provide unmatched reliability. Average positioning time is 45 milliseconds, and track-to-track takes only 8 milliseconds. Transfer rate is 1.04 megabytes per second.



Brushless, DC Spindle Motor, All DC Power

Reliability, efficiency and low cost are three benefits of the brushless DC motor that spins the disc in the DISKOS 3350. With a single shaft for the disc hub and the motor, there are no belts and pulleys to complicate the design. Result? Lower cost and greater reliability. PRIAM's brushless DC motor also eliminates the mechanical disc brake that prevents excessive rubbing contact between the heads and disc. Parts and cost are reduced and reliability is improved.

For telephone or other systems operating normally from DC, the DISKOS 3350 is an ideal component. No AC is required, and the power consumption of the drive is low.

Positive Pressure Air Filtering System

In the DISKOS 3350, a proprietary air system assures positive pressure throughout the head-disc cavity. This protects the drive from the danger of contamination. If a disc-head chamber or bearing seal leaks, air movement from the drive prevents foreign particles from entering and damaging the drive or reducing data reliability.

Compact Size, Light Weight

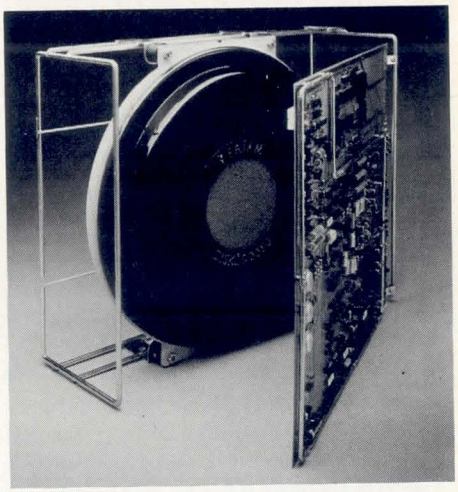
Economy, simplicity and lightness are combined in PRIAM's proprietary welded steel rod frame. This sturdy, open support for the DISKOS 3350 improves drive and system cooling. Total weight is only 34 pounds, so installation is easy and economical. PRIAM's optional power supply fits into the same 7" x 17.6" x 20" package with the DISKOS 3350, saving space and power supply installation cost.

SMART Interface Option

PRIAM's SMART Interface Adapter provides serialization and deserialization of data, disc formatting, sector buffer, polled or interrupt operation, defect mapping, overlapped commands, implied seek, selectable sector sizes and microdiagnostics. Up to four drives can be interfaced easily to the I/O bus at the byte level.

SMD Interface Option

An optional interface permits you to use PRIAM drives with existing controllers for CDC Storage Module Drives. You can stretch the life of your SMD controller or get on the air more quickly with the low-cost, high-capacity and splendid reliability of PRIAM Winchester disc drives.



The PRIAM 14-inch Line-Up

Model/Disc Size	Capacity	Transfer Rate
DISKOS 3350 (14")	34 Mbytes	1.04
DISKOS 6650 (14")	68 Mbytes	1.04
DISKOS 15450 (14")	158 Mbytes	1.04

Take a hint from the chambered nautilus. If limited capacity is cramping your system's marketability, provide for your future data storage needs now. Let us tell you how low-cost high-level disc drive technology can be. Call or write to: PRIAM, 3096 Orchard Drive, San Jose, CA 95134, Telephone (408) 946-4600, TWX 910-338-0293.

PRĪAM

Microcomputers Assist Residents in Home Management System

Joint control of home management functions—shared by the homeowner and five microcomputers—has been initiated in what is claimed to be "the most electronically-sophisticated dwelling ever built." Although the microcomputers aid the system in performing several important functions—energy conservation, electrical load switching, environmental control, security, and information storage and retrieval—they have no true control duties. The homeowner remains in full control, making all decisions which are then carried out by the microcomputer system.

This home management computer system was designed and built by the Semiconductor Group of Motorola Inc, 5005 E McDowell Rd, Phoenix, AZ 85062, and was installed in one house of a 2000-acre development being constructed south of the city. Known as the Ahwatukee House because of its location in the housing development with that Crow Indian name, this house was appropriately wired when it was built; the multifunction system could not easily be added to an existing home. Knowledge gained from this system, however, could result in the design of systems with more advanced components that might be used in older homes.

Special House Construction

Since the Ahwatukee House (Fig 1) and its management system were designed together, many features were built into the house in order to take advantage of the capabilities and benefits of the system. For instance, because of the intense sunlight common to the Arizona desert/mountain environment, solar collectors for heating the house and supplying hot water were made a part of the house. Special skylights enable the sun to light the house, and windows were minimized to conserve energy.

To overcome some of the disadvantages of desert summer temperatures, the house—roughly triangular in shape—was built of large masonry masses that absorb and release heat slowly during the wide temperature changes that occur daily. Earth was used for insulation and earth berms were piled against outside walls. In addition, some floors are 3′ (0.9 m) below ground level.

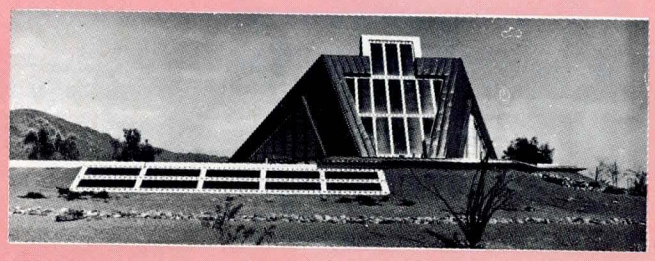


Fig 1 South elevation of Ahwatukee House. Solar collectors are used for heat and hot water, and earth berms piled against outside walls provide insulation. Windows have been eliminated wherever practicable, but special skylights permit use of sun for daytime lighting

Bedrooms, living room, and kitchen are arranged off a large central atrium to eliminate hallways and further conserve energy. A conversation pit is located in the middle of the atrium.

Heat is provided by three methods: solar, heat pump, and resistive electrical. There are also three ways to cool the

(continued on page 106)

A whole world. Because our parent company, C. Itoh Co., Ltd. (pronounced "C. Eetoe") is a multinational organization with resources and subsidiaries located in every corner of the globe.

As C. Itoh Electronics, Inc., we're fortunate to be part of this international network. It lets us seek out quality materials and technologies wherever they can be found. And for a company that specializes in computer peripherals for the OEM, that's just as important as price or the capability to deliver.

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A world of quality.

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CIRCLE 57 ON INQUIRY CARD

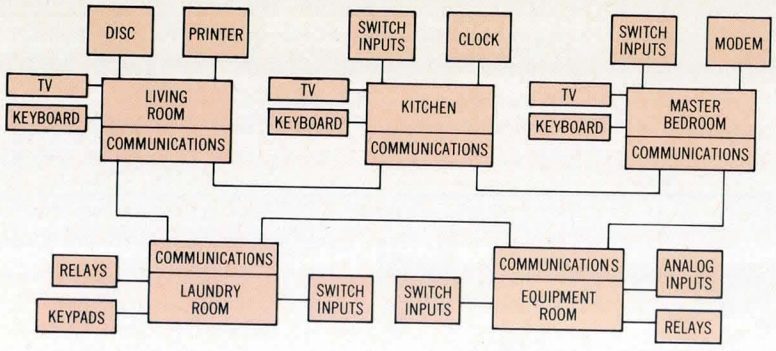

Fig 2 Five areas of house. Separate MC68000 microprocessor based nodes communicate via intelligent communications processor and advanced data link controller

house: evaporation, circulation of chilled water through a heat exchanger in the air ducts (water is chilled at night by refrigeration when electrical demands are low), and heat pump.

Multicomputer Management Network

Each of five areas of the house—living room, kitchen, master bedroom, laundry room, and equipment room—is maintained as a separate MC68000 microprocessor based unit called a node. These five nodes are connected together by an RS-422 communication link to form a multicomputer network (Fig 2).

The system is operator programmable, with the homeowner able to tailor it to individual needs. Instructions are entered through full American Standard Code for Information Exchange (ASCII) keyboards, and unused channels of standard television sets serve as the displays (Fig 3). (An MC6847 video display generator provides this capability.)

Once the system is programmed, operation is transparent to the homeowner. A method has been designed which leads homeowners without computer backgrounds through the steps of possible choices of action by interrogation and display. For most procedures, computer involvement is unobtrusive. When the homeowner closes his conventional appearing switches, there is no indication that the expected result is brought about by a programmed computer.

The electrical load switching capability also conserves energy by allowing the microcomputers to control lights, wall outlets, and electrical equipment, evening out use of electricity throughout the home. Time of day switching is based on the microcomputers' realtime clocks. Lights can also be programmed to turn on or off at various times during the day or night, and motion detectors can turn lights on when a person enters a room and off when the person leaves.

For environmental control, the house is divided into three zones, each maintained at different temperatures depending on time of day or day of the week. The computer system determines whether a zone requires heating or cooling, and then chooses the equipment that will bring about the desired effect with the least consumption of electric power. For instance, if one zone is too hot and the outside air is cooler, the system might automatically open certain doors and windows. If the outside air is too warm, the computer might turn on the evaporative cooler; however, if the air is too humid, the computer will turn on the air conditioning system.

Fig 3 Keyboard and display device. User inputs and programming are entered into system through ASCII keyboard. Unused channel of standard TV receiver displays information. Floppy disc unit at top stores all information for homeowner

Security control covers both fire and intrusion. Smoke and motion detectors sound alarms and turn on lights to alert the homeowners to fires or intruders; in the future, the computers will also automatically dial the police or fire

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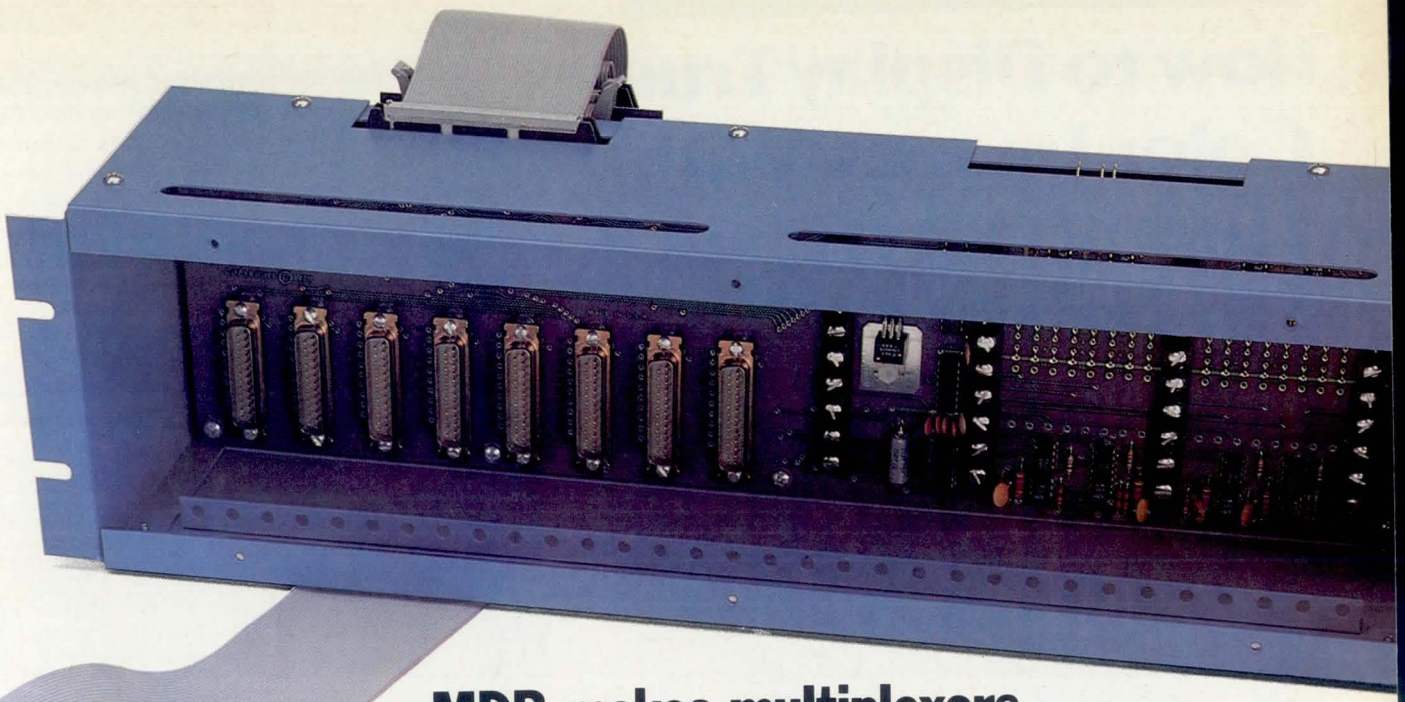
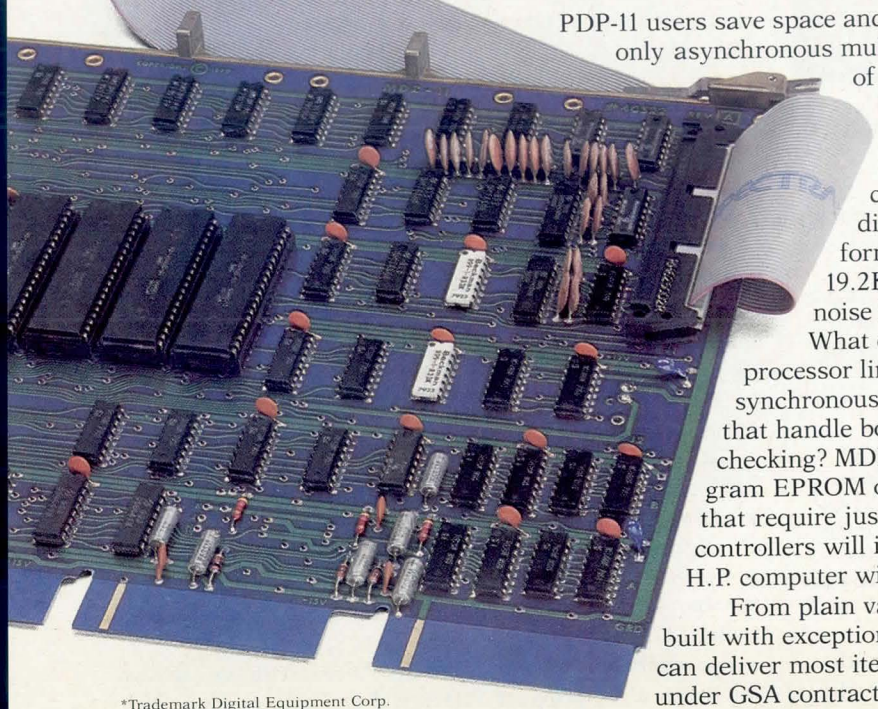


MDB makes multiplexors for the PDP*-11 that let you combine RS232 and current loop on one board.

Imagine what else we can do!



PDP-11 users save space and save money! MDB's DZ11AC is the first and only asynchronous multiplexor that lets you combine up to eight lines of RS232 and current loop in any configuration on a single hex board. No more doubling up on boards, distribution boxes, rack spaces or price. The MDB DZ11AC is fully compatible with DEC DZ-11 operating and diagnostic software and, at the same time, performs at 16 standard data rates from 50 to 19.2K baud with optical isolation for enhanced noise immunity.

What else can MDB do? Have you seen our interprocessor links for LSI*-11 as well as PDP-11? Or MDB's synchronous communications interfaces for Q-Bus* that handle both bit and byte oriented protocols and error checking? MDB makes PROM modules that let you program EPROM on the board and foundation modules that require just one card slot. Our famous line printer controllers will interface your DEC, DG, P-E, IBM Series/1 or H.P. computer with most of the major line printers in the world.

From plain vanilla to state-of-the-art, all MDB products are built with exceptional quality. We warranty them for one year, can deliver most items in 30 days or less and offer them under GSA contract #GS-00C-01960.

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Circle 58 for PDP-11, 59 for LSI-11, 60 for DG, 61 for P-E, 62 for IBM.

departments and deliver a prerecorded message. The computers can provide an explanatory display on the TV sets. If desired, they will automatically turn lights on and off to discourage intruders when the homeowners are away.

Electronic keypads (Fig 4) are used instead of the usual door keys. Doors will open only when a proper access code is entered on the keypad. Several codes can be placed in the computer system memory, each for certain uses. For example, service personnel can use an access code that is valid only during specific hours and days.

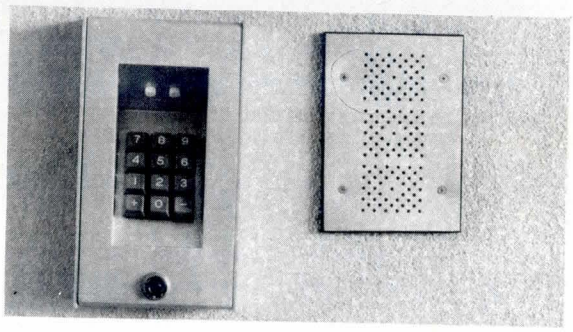

Fig 4 Door lock. Calculator style keypad placed near door is used to gain access. Homeowner can program system with individual code for each resident as well as with codes for service personnel that are valid only during specific hours and days. Voice synthesizer greets authorized persons by name

The computers have voice capability. When a member of the family enters the proper code on the keypad, the computer opens the door and greets the family member by name. This subsystem can announce the time of day when requested and can be tied into the security system for verbal warnings in case of fire or intrusion.

Using the same ASCII keyboards as for programming, the homeowner can set up an information storage and retrieval system. Income tax data, checkbook or savings account records, a calendar of events, menus, appointments, birthdays, and recipes can be entered for retrieval as desired.

System Hardware

Most of the hardware chosen for this system consists of standard micromodules; only a few modifications were necessary. Mass storage is provided by an EXORdisk II floppy disc unit.

Although most inputs are digital, some analog measurements—such as temperature and humidity—are required. These values are handled through a 32-channel analog to digital converter. Inputs from wall switches and motion detectors are sensed by contact closures connected through opto-isolators to the microcomputers. All outputs are contact closures. Reed relays drive power relays to handle the 120-Vac loads that make up most of those to be switched.

An intelligent communications board with an MC6800 microprocessor provides internodal communications. This communications processor and the system microcomputer share 2k bytes of memory. Although both processors are always in use, they are out of phase with one another to avoid memory access contention. A modified version of

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synchronous data link control (SDLC) protocol carries out the communications with an MC6845 advanced data link controller.

Future systems will undergo a drastic reduction in hardware. Input/output interface boards, which make up a large part of the system, could be replaced by a much smaller carrier current system that would also eliminate much of the extra wiring in the house. Switches throughout the house would communicate with the controller over the house's electrical wiring. In addition, the present 1300 integrated circuits and 750 discrete devices would be replaced by fewer than 200 semiconductors. Much of the necessary installation could be handled by the homeowner.

System Processes

A multitasking executive program, resident in each microcomputer, organizes the processes—Disc, Display, Load Manager, Switch Manager, Security, Energy Management, Environmental, Time, and Printer—for the five nodes. (See Fig 2.) Although each computer has several resident processes, some of which are duplicated among computers, no computer contains all processes.

The Disc process places and retrieves data on or from the floppy disc mass storage device. However, other processes also use the disc to store information. User interface to the system is the Display process. It is formatted to lead the user to choose from among possible actions whenever user action is necessary. The Load Manager process maintains a data base of information on electrical equipment, loading and causing switches to open or close as required.

A data base on various switches is maintained by the Switch Manager process. Whenever a change in switch state is noted, this process notifies other related processes. The Security process also maintains a data base. If a security switch or load change occurs, or if a programmed or time related event is due to occur, switches or loads are activated and the Display process is instructed to place certain information on the TV screens. Energy Management and Environment processes monitor energy consumption and methods of reduction. Data are sent to the Display process for access by the user.

All other processes can access and reference a 24-hour clock and a calendar maintained by the Time process. Battery backup is provided in case of power failure. The Printer process produces a hard copy of any text displayed on the TV screens. This permits printing of material or information that might be needed away from the house.

MPL, a Motorola developed high level language oriented to the MC6800 and similar to PL/1 or Pascal, was used for software development. All of the system processes were defined using finite state theory. Program flow is governed by a table of possible actions formed in a modular structure. Current state of a process and momentary input conditions determine the action to be taken.

Note: Information for this review is based in part on two Motorola Semiconductor Group publications: "The Ahwatukee House," by P. J. O'Malley; and "Microprocessor-Controlled Home Environment," by W. D. Pierce.

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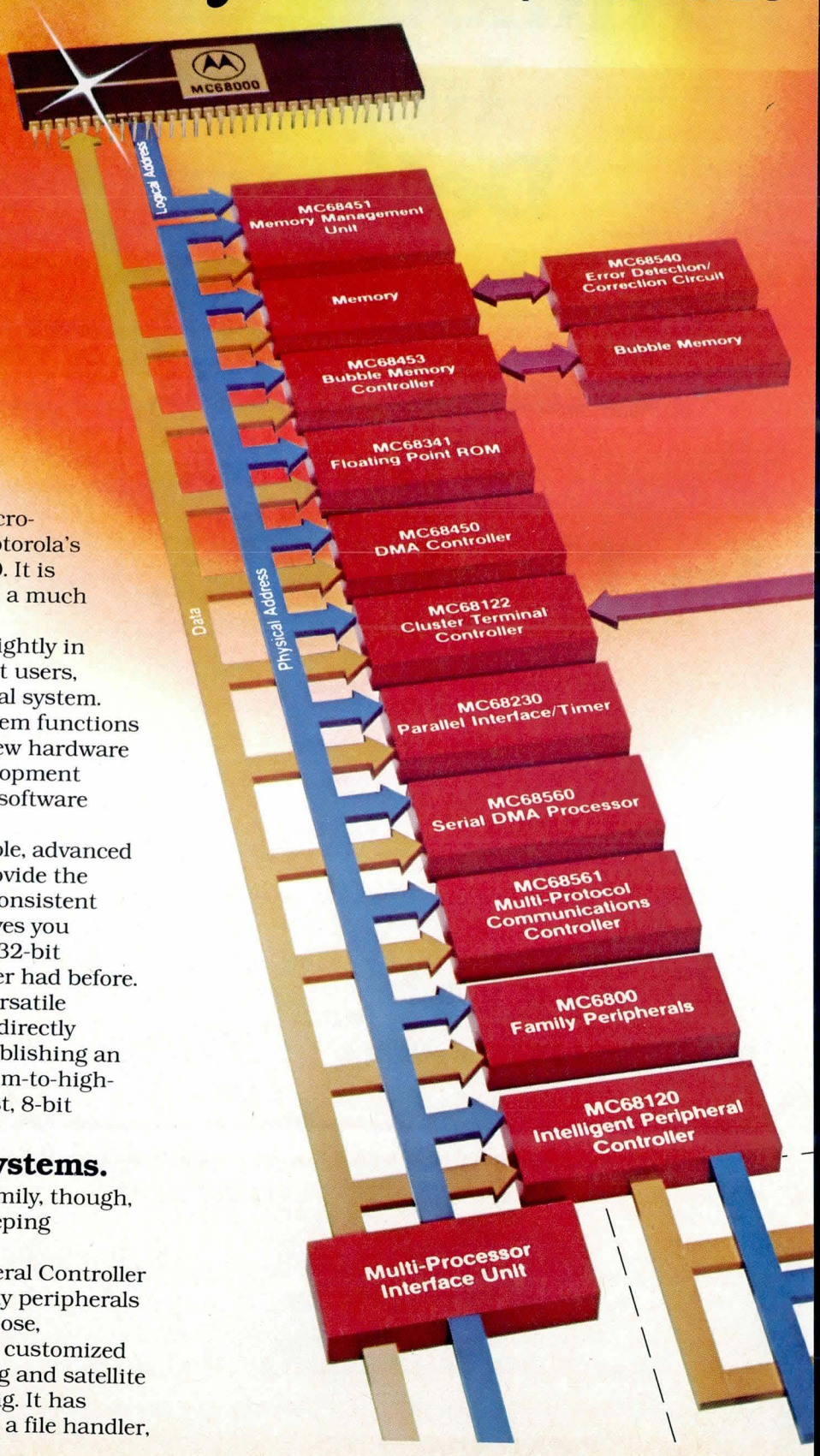
Technological leadership.

Motorola's M68000: family for 16-/32-bit



No high-performance 16-bit microprocessor gives you as much as Motorola's architecturally-advanced MC68000. It is demonstrably superior to others in a much broader range of systems.

The MC68000 shines just as brightly in the absolutely critical area, for most users, of support in implementing the total system.

Not one, but two families of system functions support the MC68000. Powerful new hardware implementation and software development support systems are available, and software is extensive.

The M68000 Family of compatible, advanced VLSI peripherals was defined to provide the optimum level of chip integration consistent with system design flexibility. It gives you design opportunities in 16-bit and 32-bit microcomputer systems you've never had before.

And more than a dozen of the versatile M6800 Family peripherals also are directly compatible with the MC68000, establishing an effective design approach for medium-to-high-performance systems where low-cost, 8-bit peripherals can be used.

Key to state-of-the-art systems.

It's the newer HMOS M68000 family, though, that offers you the capability for keeping systems state-of-the-art for years.

The MC68120 Intelligent Peripheral Controller was the first of these M68000 Family peripherals to be announced. It's a general-purpose, user-programmable unit for local or customized peripheral control, I/O preprocessing and satellite processing for distributed processing. It has many applications, including use as a file handler,

the most advanced VLSI microcomputer systems.

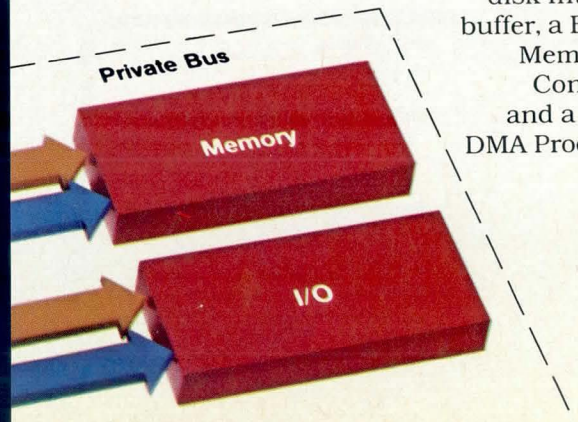
intelligent floppy or hard disk controller, data communications protocol controller, CRT driver and GPIA bus-management controller.

Also scheduled for imminent introduction are a Cluster Terminal Controller, the MC68122, and a compatible bipolar interface Error Detection and Correction circuit, the MC68540 (also numbered MC34040). The Cluster Terminal Controller will relieve the host processor of the coordinating task for communications between and among terminals, and the EDAC circuit performs the error check/correct function in 8-bit or 16-bit systems. It's directly expandable to 32-bit operation.

More HMOS VLSI.

Following these, availability is scheduled for the MC68451 Memory Management Unit, MC68450 DMA Controller, MC68230 Parallel Interface/Timer and the MC68341 Floating-Point ROM.

The MMU provides address translation and protection of the 16-megabyte MC68000 addressing space and can be accessed by any potential bus master. The DMAC offers the optimum in data transfer, and internal 32-bit registers ensure upward software compatibility with future M68000 Family processors. Still other M68000 Family peripherals now planned include a Multiprotocol Communications Controller, a Dual-Port RAM for multiprocessing systems or applications like CRT refresh and disk interface buffer, a Bubble Memory Controller and a serial DMA Processor.



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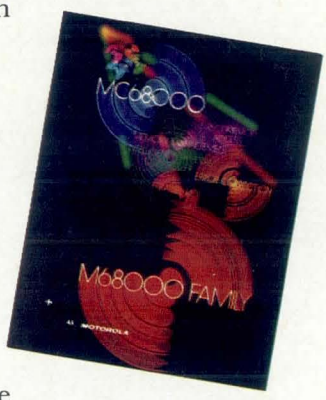

Just as Motorola set the pattern for the semiconductor industry back in 1973 with the total system approach of the M6800 Family, the M68000 Family raises the concept to a new level.

For more information, including an M68000 Family brochure, use the coupon provided below, or send a specific written request to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

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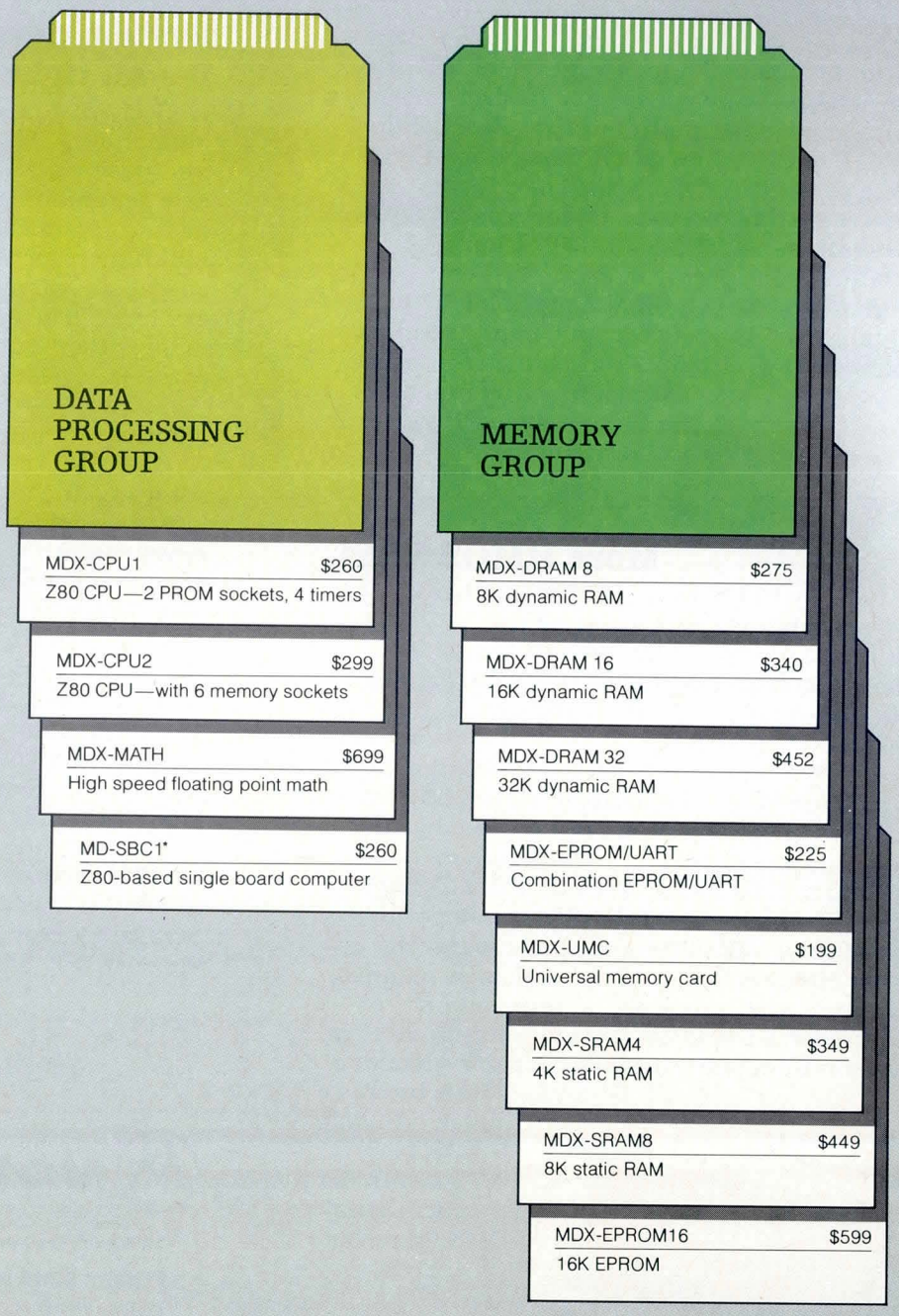

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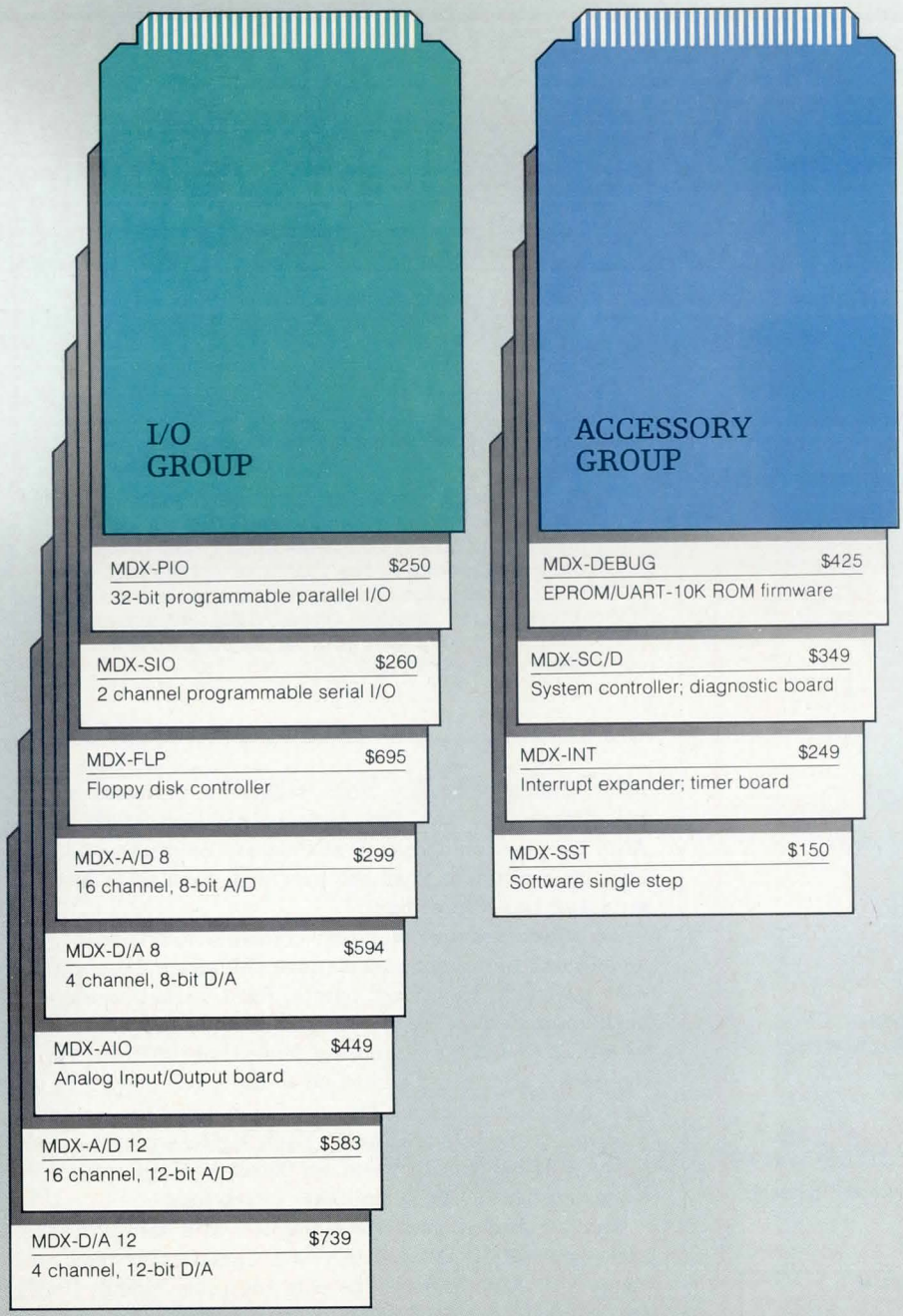

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CIRCLE 67 ON INQUIRY CARD

Distributed Multiplexing System Relays Messages in Power Plants

Intended primarily for application in the electric utilities market, the 1055/DMUX plant control system can contain up to 250 individual processing elements or nodes on a single logical loop. Any node can transmit messages unidirectionally to any other node at 1.54M bits/s, without need for a central transfer point. Message paths are not shared by more than two points in the system. Additional nodes can be inserted anywhere in the loop, without significant effect on message traffic, with the addition of a single path. Although this distributed multiplexer (DMUX) from Bailey Controls Co, Wickliffe, OH 44092, can operate as a standalone system, it functions at maximum capability when combined with a Modular Computer Systems IV-35 computer as central processing unit. Basic system architecture is a direct dedicated loop (DDL) structure.

Each node connects to two neighboring nodes. Redundant message paths are provided between active nodes to insure system reliability. Since redundant paths are active, the effective message rate between nodes is 3.08M bits/s. Also, because communications lines are unidirectional, and because redundant lines are provided, each node has two send and two receive lines.

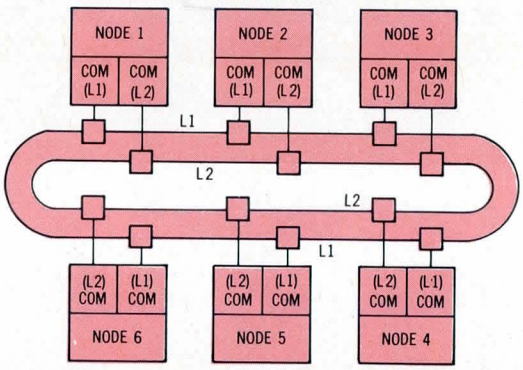

Fig 1 DMUX communication line organization. Each of up to 250 nodes is connected via redundant unidirectional communications lines to each of its neighboring nodes. COMs send, receive, and interpret message packets. If message received is intended for another node, COM retransmits packet to next node. Paths can be up to 1600 m of cable

To accommodate redundant communications paths, the nodes contain two communications modules (COMs), one for each path (Fig 1). A fixed length, fixed format message or packet is generated by the COM of one node and transmitted to the COM of the neighboring node. That COM interprets the packet and, if not addressed to its node, relays it to the next neighboring node. This continues until the packet is received at the intended node. Each logical packet is made up of a 32-bit 'header' and an 80-bit message, which includes an 8-bit cyclic redundancy check field.

An 8-bit single-board microcomputer with lk-byte random access memory (RAM) and lk-byte programmable read only memory (P/ROM) serves as the data controller module (DCM), the primary source of message traffic. Memory expansion modules (MEMs) provide an additional 11k bytes of RAM and 15k bytes of P/ROM. As many as seven DCM/MEM pairs can be provided in any node both for sharing the processing load and for redundancy. They all receive and/or transmit messages to/from the shared COMs.

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If a source node (Fig 2) does not receive an Acknowledge signal from the destination node on the first attempt, the message recirculates the loop up to seven more times; then, if the message is not received, the source node tries to recapture the message for another eight loop transits. If the message is neither received nor recaptured after 16 cycles, it is destroyed to prevent loop saturation.

Whenever a message is destroyed or returned to the source node as undeliverable, the sourcing DCM retransmits the message; up to three retransmissions are attempted over each loop path. A time delay is introduced between retransmissions to avoid loop saturation if the destination node is temporarily busy. Whenever the third retransmission over a communication path fails, the source node marks that path as bad, and does not attempt further normal transmission over the path. Periodically, loop monitor software in each DCM retries each bad path, and if a transmission is successful the path is marked as restored. Each time a path fails, a status message is sent to the DMUX, which serves as the loop master for error reporting.

Software in each DCM is subdivided into an operating system, a communication system, and application tasks. The operating system provides tasking, interrupt service, resource management, and general purpose services. Each application task performs one or more of these functions and is driven by the RAM contents.

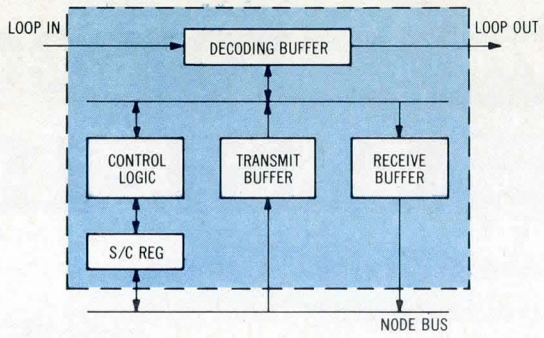


Fig 2 COM architecture. If not acknowledged by receiving node, message packet circulates on loop up to total of 16 times. If not recaptured by sending node, message is destroyed

Note: The plant computer system and distributed multiplexer is described in company publication TP79-5, "Distributed Multiplexing for Fossil/Nuclear Power Plants," by Michael S. Willey.
Circle 440 on Inquiry Card

Timeshared Management System Offers Energy Conservation Plus Reduced School Budgets

Energy conservation. Reducing educational costs. These two goals are at or near the top of the list of priorities in every U.S. city, town, or hamlet. When they are combined, interest level is more than doubled. Therefore, a claim that up to 27 million dollars in energy costs can be saved annually within a single state's elementary and secondary school system has to attract attention. That this saving can be gained *without increasing budgets* makes the subject irresistible.

Approximately 11% of all energy for space heating and cooling in the U.S. is consumed by elementary and secondary schools; heating and cooling alone account for 80% of the energy used in schools. However, most schools are overheated and overventilated because buildings and temperature control equipment are designed for the comfort and desires of individuals rather than for efficient energy consumption—even though comfort with efficiency can be easily attained. At present, in spite of conservation efforts, about 50% of the energy used by schools is wasted—a national total of almost one billion dollars.

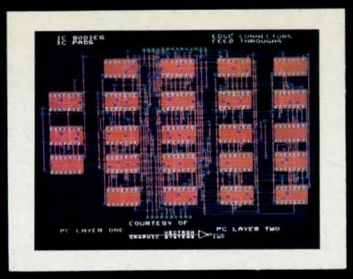
These claims result from a study prepared by the Energy Management Information Center of Honeywell Inc, Minneapolis, MN 55408. Entitled "Reducing Energy Costs in New Jersey Schools with Computerized Energy Management," the study is one of 20 similar state reviews based on data from the U.S. Department of Energy, state energy offices, the U.S. Bureau of the Census, the University of California's Lawrence Berkeley Laboratory, the American Association of School Administrators, and a report of the Harvard Business School Energy Project. Typical savings on annual energy expenses of 15 to 30% are promised by the use of a timeshared computer system to manage energy functions. Telephone lines link the computer to sensors attached to a school's boilers, chillers, motors, pumps, fans, and lights for automatic operation at peak efficiency with no decrease in comfort levels.

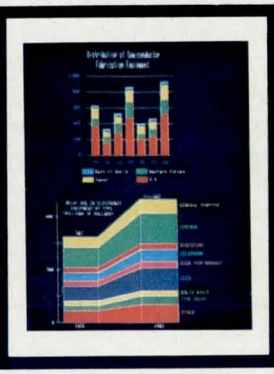
Timesharing Minimizes Capital Outlay

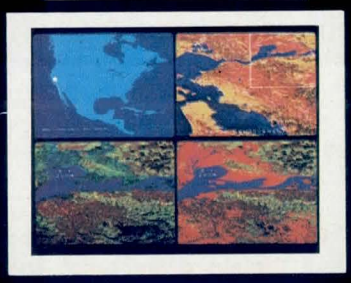
Emphasis of the studies is on timeshared computer systems because they require less capital expense and planning is more immediately cost-effective than it would be if separate computers were purchased. In addition, the report points out that the schools that most need to upgrade buildings and equipment are often least able to afford large capital investments. Since those schools, as well as many others, are often poorly maintained, they would not likely have personnel to keep computer equipment in working order.

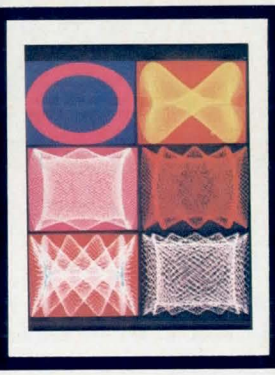
Failure to maintain energy conservation programs under ordinary circumstances is usually due to the human element. Teachers or maintenance personnel regulate room

(continued on page 120)









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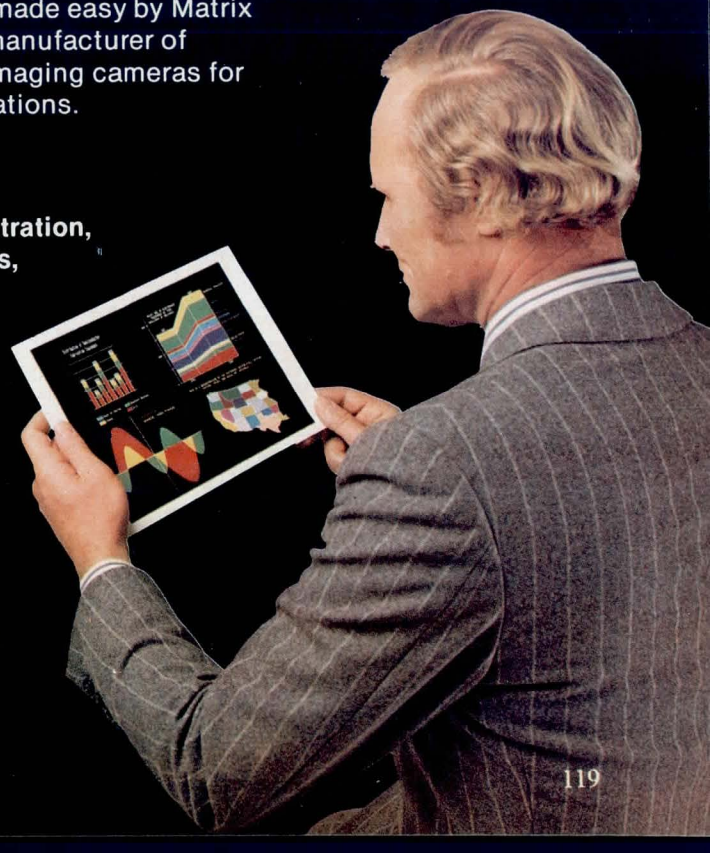
Color Graphics Hard Copy... Made Easy

The Matrix Color Graphic Camera System converts the output of any raster scan computer color terminal into brilliant, high resolution photographic hard copy. Both line and continuous tone images can be made with accurate, bright, saturated colors.

Our system does what no other instrument can do — it produces instant, on-the-spot results with Polaroid® 8 x 10 film, 8 x 10 color transparencies for backlit displays and overhead projection, 35mm color slides, 60 image color microfiche, and 16mm/35mm color animation films. All with one camera system. It also allows recording of multiple image formats. Related and sequential images can be recorded in orderly arrays, on a single sheet of 8 x 10 instant print film. The resultant ease of comparison and analysis is unmatched. The system is also fully modular and field upgradable. . . you purchase only the capability that you need now.

Microprocessor based electronics provide many automation, self-calibration, self-diagnosis and remote control functions. Color graphics hard copy made easy by Matrix Instruments, the leading manufacturer of precision electro-optical imaging cameras for diagnostic medical applications.

For more information, film samples, or a demonstration, contact Matrix Instruments, 230 Pegasus Avenue, Northvale, New Jersey 07647. Telephone (313) 439-8832. Or call toll-free: (800) 521-1596.



 # MATRIX INSTRUMENTS

CIRCLE 70 ON INQUIRY CARD

Hard copy shown reduced from original 8" x 10", slide, and microfiche films.
Multiple images recorded on a single sheet of film.
"Polaroid" is a registered trademark of the Polaroid Corporation.

temperatures according to whim; operators are not properly taught how to use equipment efficiently. Consequently, a building's entire heating or cooling system is often kept in operation for the comfort of a few employees who work after hours.

Full energy conservation can be negated by an overabundance of decision makers. Students, teachers, administrators, or maintenance staff are often permitted to change thermostat settings—without concern for increase in energy consumption since they do not feel the immediate responsibility for energy conservation. Even when responsibility and awareness are maintained, it is not cost-effective or practicable to have highly paid personnel take time away from other duties to make decisions about temperature settings when they cannot possibly know all of the factors involved for a proper determination.

Computerized energy management systems, however, whether based on timeshared or dedicated computers, monitor conditions on a 24-hour, 7 day/week basis. They depend on computer memory, not the cooperation of school building users. With computer control, unneeded heating equipment can be shut down when outside temperatures rise. Sensors can determine whether classrooms are full or only half full, and the computer can adjust the amount of energy necessary to maintain the proper comfort level.

With computerized control, equipment can be cycled so that units are not operated full time. Heating, cooling, and ventilating units can be shut off at night, on weekends, and in the period between day and evening classes. Power consumption can be reduced by shutting off units in unoccupied parts of the school and by operating other units at off-peak demand hours when possible. In addition, potential malfunctions can be located before the need for expensive repairs.

First-Year Savings Payback for System

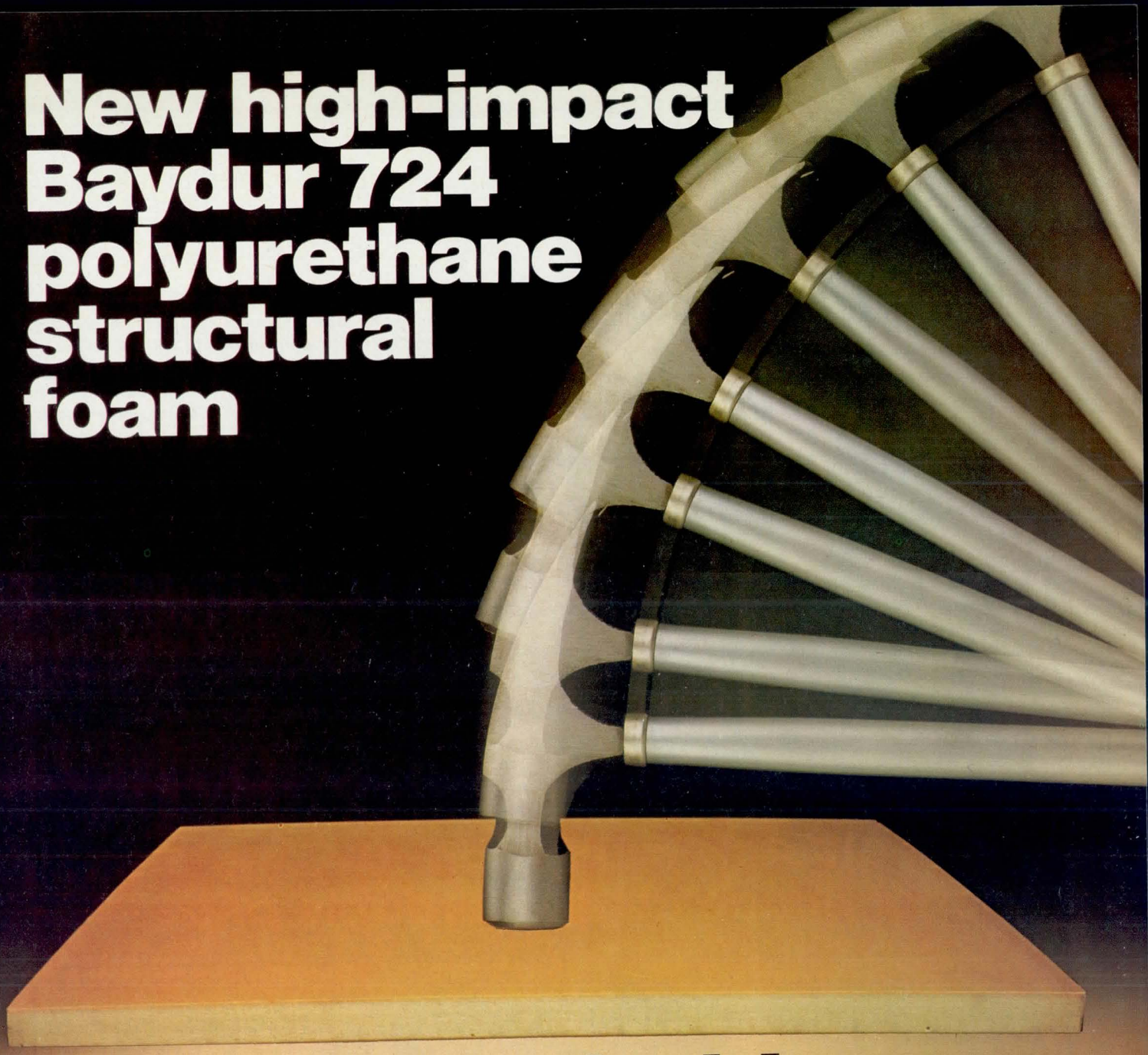
Energy costs, consumption, and potential savings vary, depending on several factors. The current report was based on costs for the 1978-79 school year, which are considerably lower than those for the 1980-81 period. Size and layout of buildings, type and efficiency of mechanical systems, hours of building use, climate, and existing conservation measures must all be considered. However, an estimated range of 13.5 to 27 million dollars of potential annual energy cost savings is estimated for all New Jersey schools. Individual schools could save from $2307 to $156,548, depending on size and location.

In one case study for timeshared computer control, an Atlanta, Ga, high school reported a savings of 18% ($18,447) in the consumption of electricity and 42% ($9053) for gas. The one-time cost of installing 22 sensors and linking them to the control computer was $18,812 and the first-year timesharing fee was $5844. Therefore the first-year costs were $2844 less than the savings for that period—and in future years the $18,812 cost will not be repeated.

For a second Atlanta high school, the installation cost was $22,256 and the timesharing fee was $5904. Electricity costs were lowered by $15,517 (16%) and gas expense dropped by $7387 (28%). In this case, the payback point occurred within the first 15 months; once again, the installation cost will not reoccur.

Circle 441 on Inquiry Card

New high-impact Baydur 724 polyurethane structural foam



can take it!

Impacts up to 140 ft-lbs Gardner or 11.2 ft-lbs/in^2 Charpy. That's real performance in a structural foam. And there are other properties that make new high-impact Baydur 724 an ideal material for computer and electronic equipment housings:

- Design freedom for complex, vari-dimensional shapes
- Smooth, swirl-free surfaces
- Better thermal insulating capability than other structural foams
- Dimensional stability
- Freedom from sink marks
- Ability to mold-in metal and wood reinforcements
- Excellent chemical and warp resistance.

In addition, reaction-injection-molded Baydur 724 has some special processing advantages:

- Single-shot molding of large-surface-area rigid parts
- Easier finishing than other structural foams
- Good flow characteristics
- Low energy consumption and low molding pressures.

UL testing is underway, but Mobay lab studies show that Baydur 724 is ideal for computer housings and other large-scale parts requiring V-0 and 5V ratings.

For complete information on new high-impact Baydur 724 structural foam, call Bill Daniels at 412-777-2636 today, or write:

Baydur 724
High-Impact Structural Foam

MOBAY

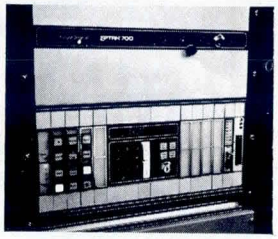
Mobay Chemical Corporation
Polyurethane Division
Pittsburgh, PA 15205

CIRCLE 72 ON INQUIRY CARD

DC & AS BRIEFS

Data Acquisition and Control Systems And Components

Microprocessor Based Programmable Controller



EPTAK 700 is claimed by Eagle Signal Industrial Systems, 736 Federal St, Davenport, IA 52803, to incorporate more efficient software, improved analog accuracy and resolution, better operator interface, and increased memory density—providing "more control per dollar while reducing both operational and system costs for users." Features of this programmable controller are comparable to those of more expensive process computers.

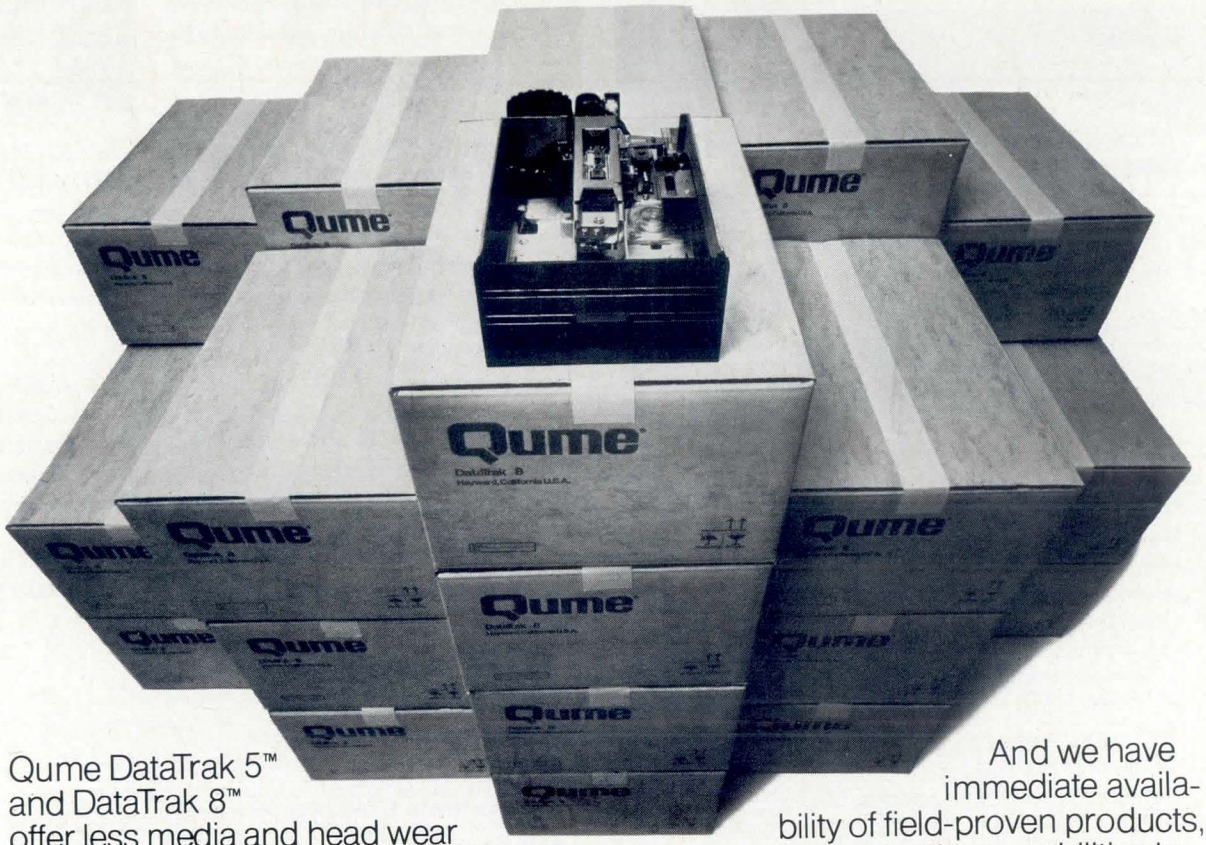
Executive D software incorporates computational capabilities of an arithmetic processing unit, three PID scan rates for response to critical analog loops, user defined algorithms for custom control schemes, and simplified operator interface in familiar terms. It also provides updating of the entire user program without recompiling, reduced compiling time necessary for program changes, reduced need for user support memory, doubled ranges (to 19999), timer freeze function that enables interrupts without effect on total time cycle, and compatibility with older EPTAK program modules. An ECL3 language instruction set has expanded and more comprehensive declare statements for analog control and operator interface.

Seven 12-bit analog modules consist of an ADC that supports up to 15 analog input modules, thermocouple input, 70-mV analog input, two 4- to 20-mA analog inputs, 4- to 20-mA analog output, and calibrator card. Standard input ranges are 4 to 20 and 10 to 50 mA; 0 to 5, 1 to 5, and 0 to 10 V; and 0 to 70 mV. Output ranges are 4 to 20 mA and 10 to 50 mA with simultaneous 0 to 5 V or 0 to 10 V.

Memory modules consist of 16k RAM, 16k UV P/ROM with 4k RAM, and 8k UV P/ROM with 8k RAM. By reducing the number of slots required for 48k maximum memory to three (16k modules rather than 4k), the remaining slots can be used for self-diagnostic or operator interface modules.

Circle 442 on Inquiry Card

More tap-tap on tap.



Qume DataTrak 5™ and DataTrak 8™ offer less media and head wear than any other double-sided floppy disk drive on the market. That means less service cost and more disk life.

Look how they stand up to the competition. Independent tests have shown a tenfold improvement in error rate over industry-standard specifications.

	Qume Performance	Standard Specifications
SOFT ERROR	1 in 10^{10}	1 in 10^{9}
HARD ERROR	1 in 10^{13}	1 in 10^{12}
SEEK ERROR	1 in 10^{7}	1 in 10^{6}

And we have immediate availability of field-proven products, with production capabilities to meet your needs. So you can order our double-density, double-sided floppy disk drives for delivery now.

So what's it all add up to? More tap-tap, better performance, immediate availability and prices that won't boggle your memory. For an evaluation unit, hurry and call today. **(415)783-6100.** Ask for Dept. M. Qume Corporation, Memory Products Division, 2323 Industrial Parkway West, Hayward, California 94545. TWX: 910-383-0710.

Qume®

Memory Products Division

CIRCLE 74 ON INQUIRY CARD

DIGITAL CONTROL AND AUTOMATION SYSTEMS

DC & AS BRIEFS

Cassette Based Standalone Control System

A user programmable data acquisition and control system, the CS430 includes microcomputer, memory, peripherals, Multibus compatible analog and digital I/O, and operator interface. BASIC-400, an extended interpreter language, permits logic program preparation and execution by unskilled operators. An autostart feature automatically loads and runs programs without operator involvement.

This unit, introduced by Burr-Brown, PO Box 11400, Tucson, AZ 85734, accommodates up to 8 I/O boards, and includes 130 differential or 248 single-ended high and low level analog inputs, up to 32 channels of analog outputs, and up to 576 channels of discrete input or discrete output. As many as 576 channels of TTL level I/O can also be handled. A variety of optional solid state relay modules provide discrete high voltage I/O. Modules offer 2500-Vac rms input to output isolation.

To meet severe environment requirements, both user programs and BASIC-400 are stored on dual minicassette tapes that rewind automatically whenever a tape operation is complete. A Centronics compatible port is provided for external printers. Options include an internally mounted 40-col printer, CRT, and full ASCII keyboard interfaced through an RS-232-C port. Dimensions of the basic unit are 17 x 12.5 x 24" (43.2 x 31.75 x 61 cm) and weight is 45 lb (20 kg). Op temp range is 5 to 35 °C.

Circle 443 on Inquiry Card

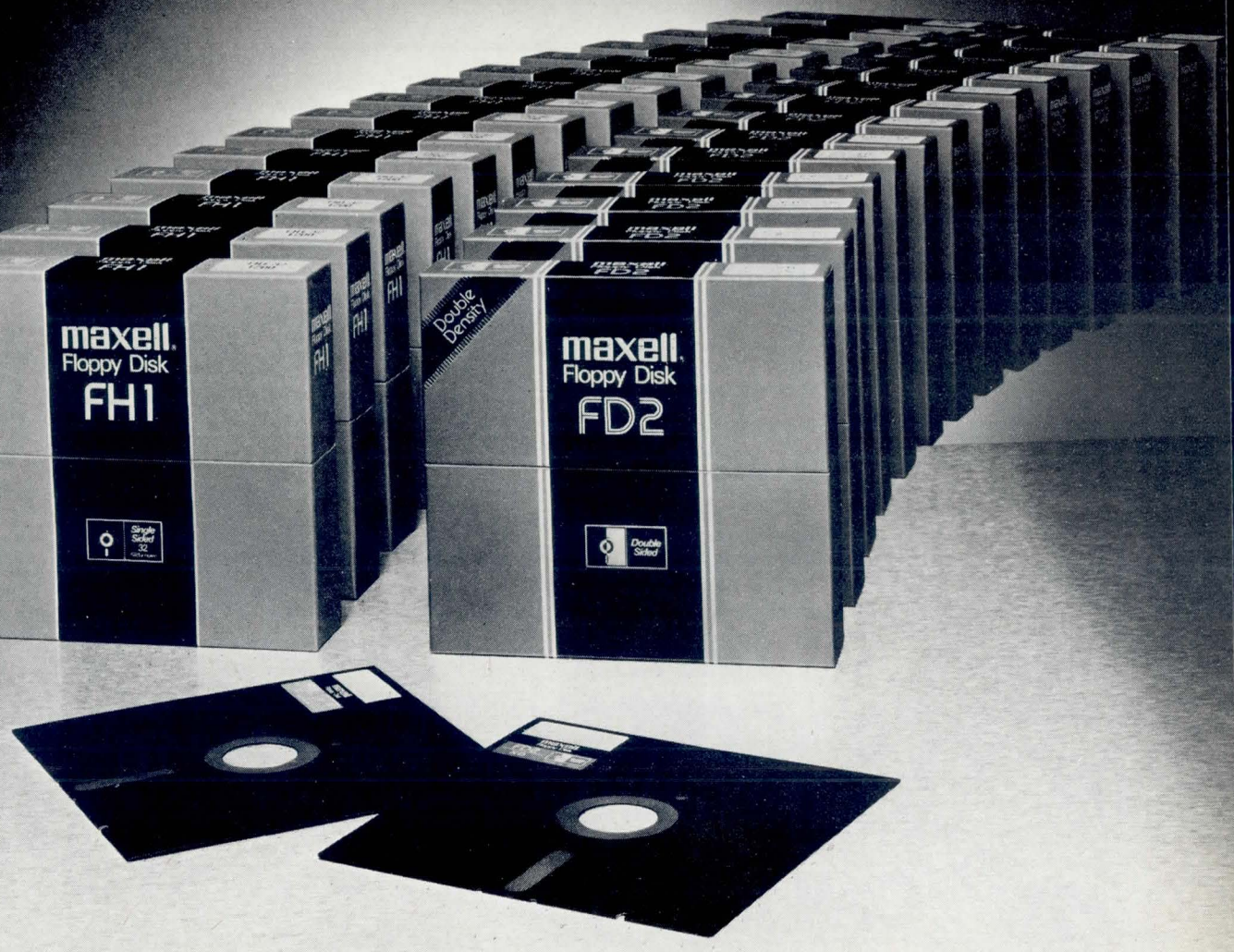
Factory Data Collection System

Accurate production, material, and labor data can be collected from areas such as the shop floor and processed by the model 5000 factory data collection system for management records. Introduced by Infolink Corp, 1925 Holste Rd, Northbrook, IL 60062, the system includes a 5100 controller that directs a network of data entry terminals, printers, and other peripherals. The controller can be configured from a series of 16-bit microprocessors and memory capacities from 256 to 32k bytes. Up to 128 terminals can be handled on multidropped lines at up to 10,000 ft (3 km) at 9600 baud. The network uses SDLC protocol and supports both batch and online communications to most computers through either EIA serial asynchronous or synchronous interface channels.

A 5040 data entry terminal can record up to 32 different transactions as they occur. Each terminal has a full alphanumeric keyboard and a 32-char alphanumeric display. Peripherals include 5600 printers and 5700 video display terminals.

Circle 444 on Inquiry Card

You don't have to take our word about Maxell Floppy Disk quality.



Ask the people who made your system.

Maxell Floppy Disks are either expressly specified or recommended by many major disk drive manufacturers. We're also relied upon by a growing number of 8" and 5¼" Floppy System owners. They find our Floppy Disks do everything possible to bring out the maximum performance of their systems. And they find our disks do this consistently.

Are we better than others? Will a box of ten Maxell Disks always contain ten disks that produce high performance results every time? We think so. We certify each one. We maintain extraordinary quality control. So they all meet or exceed the most critical industry standards.

But please ask the manufacturer of your system to double check our recommendation. See your computer products supplier. Or write to us for more information. We recommend dealers write to us about the opportunities Maxell Business Products offer.

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BUSINESS PRODUCTS DIVISION

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CIRCLE 76 ON INQUIRY CARD

DIGITAL CONTROL AND AUTOMATION SYSTEMS

DC & AS BRIEFS

Optically Coupled Interrupters

Dual channel side by side optically coupled interrupter assemblies contain pairs of GaAs near-IR LEDs coupled to a pair of Si phototransistors. Designed and built by Optron, Inc, 1201 Tappan Circle, Carrollton, TX 75006, the OPB822S and SD, respectively, have minimum current outputs of 250 and 100 μA. The S version contains a 10-mil (0.25-mm) aperture in front of each sensor; the SD has a similar aperture in front of both LEDs and sensors.

In addition, OPB825 and 825 A and B series each contain a near-IR LED coupled to a Si phototransistor mounted in a black plastic housing. LED and sensor are low cost plastic lateral discretes with molded prefocused lenses. The 825 has no mounting flange, A has a single flange on the sensor side, and B has a flange on both LED and sensor sides. All three devices have 500-μA min output with 20-mA LED drive and 100-nA max dark current with V_{CE} = 10 V and LED drive of zero.

Circle 445 on Inquiry Card

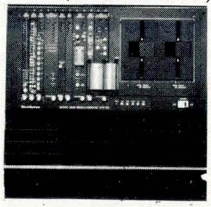
Analog to Digital Converter

Designed for operation with Pet, Apple, TRS-80, and Kim microcomputers, the AIM 16 is a 16-channel ADC that connects to a host computer through its 8-bit input and output ports or through a custom interface. Specifications for this device from Connecticut microComputer, Inc, 34 Del Mar Dr, Brookfield, CT 06804, include 0- to 5.12-V input range, 20-mV resolution with 0.5% ±1-bit accuracy, and conversion time of less than 100 μs/channel. All 16 channels can be scanned in less than 1.5 ms. Power required is 12 Vdc at 60 mA.

Circle 446 on Inquiry Card

CAMAC Standard Process Control System

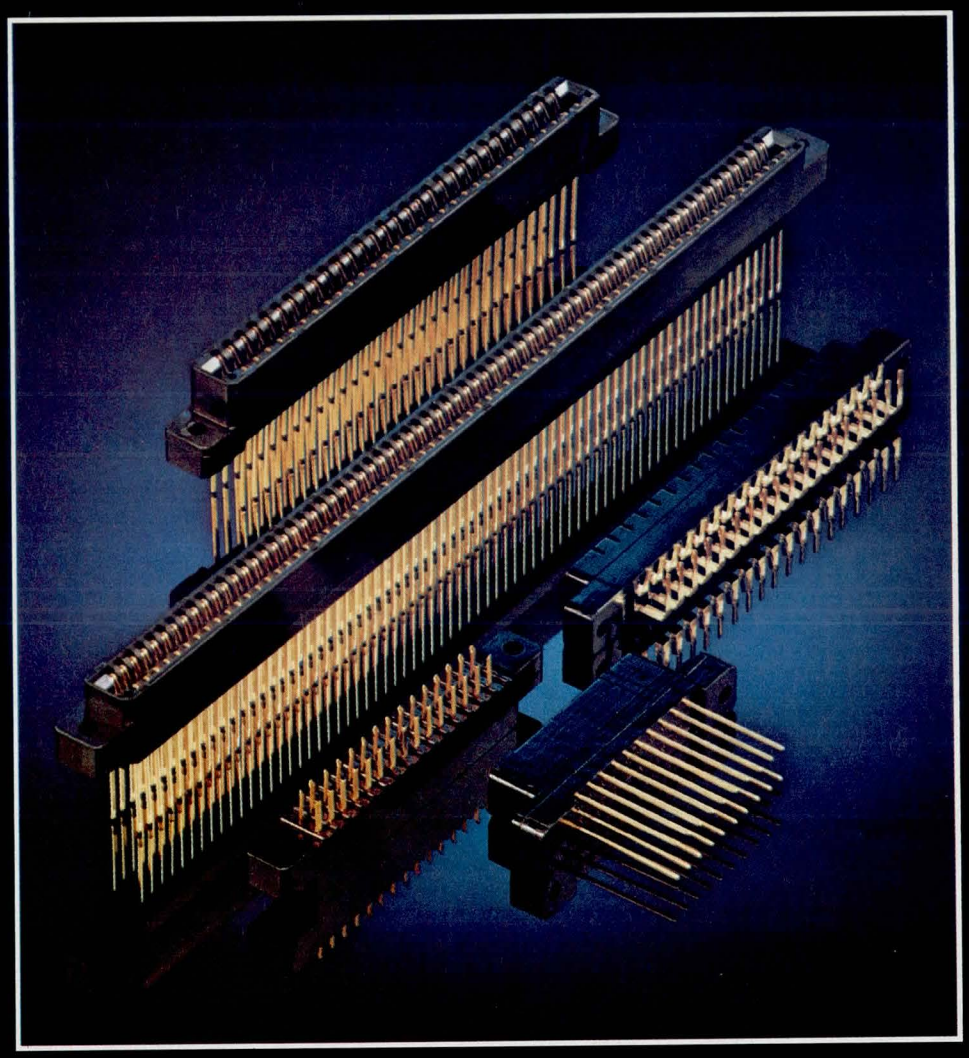
Requirements of a specific process industry can be met by a configuration of the 8030 Concept system offered by Kinetic Systems Corp, 11 Maryknoll Dr, Lockport, IL 60441. Hardware conforms to the international CAMAC (ANSI/IEEE-583) standard, and consists of a microcomputer module with 8085 processor, a microcomputer expansion module with additional memory and optional disc controller circuitry, a main or auxiliary crate controller, a 12- or 25-slot crate for housing, disc drives, and all interconnecting cables. Software packages are available for development of process control programs in FORTRAN, CAMAC*BASIC, CAMAC*Forth, or Pascal. I/O modules meet industrial or laboratory process interface requirements.



Circle 447 on Inquiry Card

Call one of our design engineers. They're idea men—the men who helped create what is now the largest and best line of P/C connectors around. That's a lot of connectors. More important, that's a lot of experience. And it's experience that's yours for the asking. Do ask.

How to make sure you've specified absolutely the best P/C connector.



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CONNECTORS

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CIRCLE 78 ON INQUIRY CARD

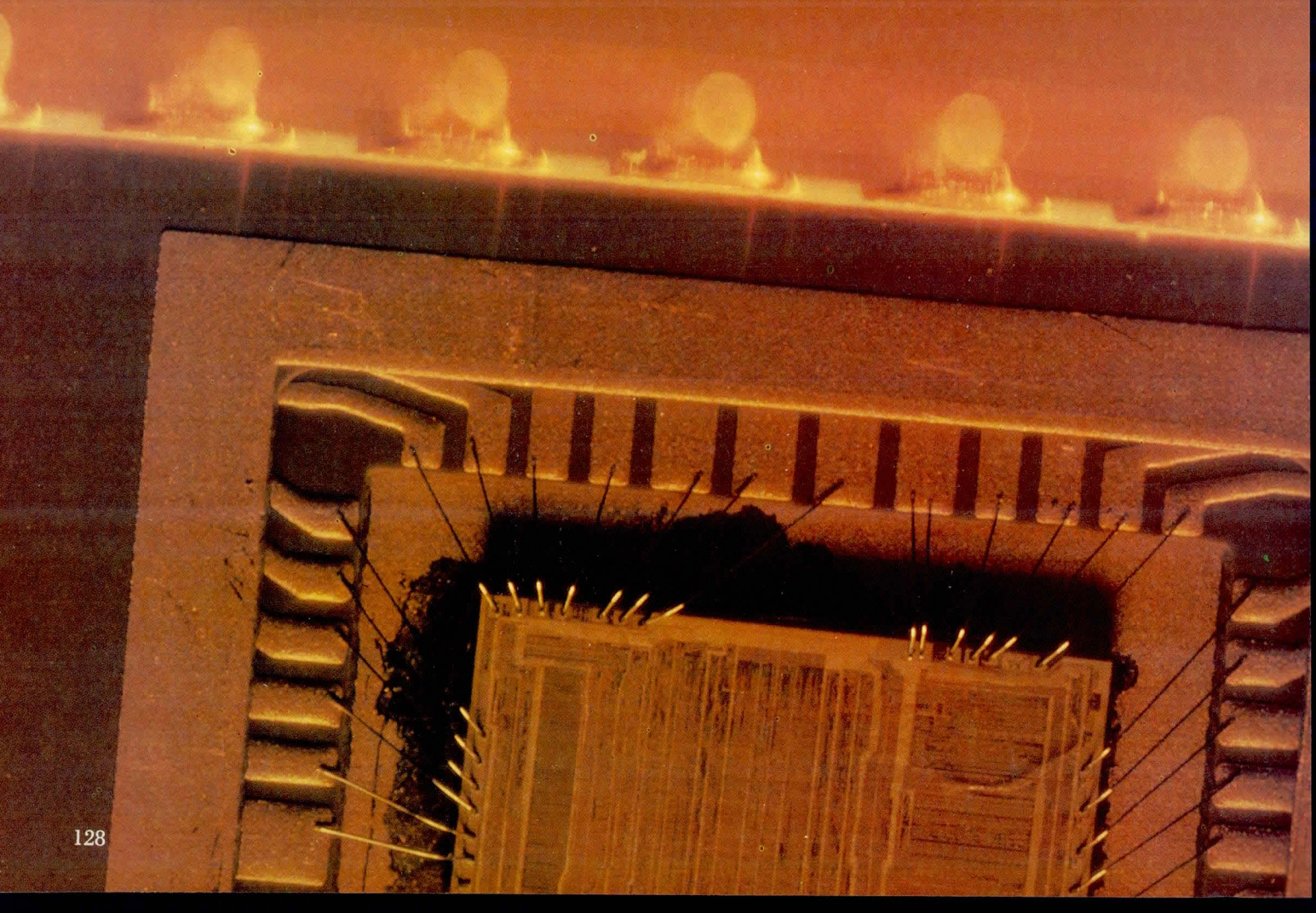
IMAGINE

As your ideas race into the future, you need products to match your stride. Today Zilog offers you the most advanced family of microprocessor products made: components, support devices, software, development systems. All available in production quantities with worldwide support.

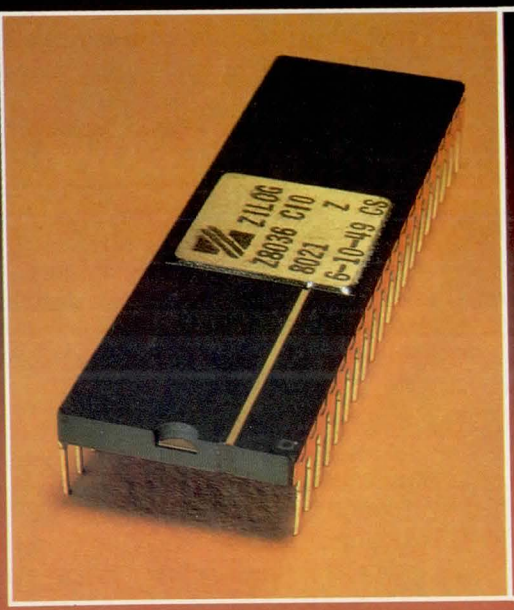
Elegant but soundly conservative scaled n-channel manufacturing processes combine with generation-ahead architecture to give Zilog products uncommon performance levels. The 8-bit Zilog Z80 revolutionized the microprocessor industry.

Today it's become the still more powerful Zilog Z80B. Its cousin, the Zilog Z8, packs an ingeniously flexible, complete 8-bit microcomputer onto a single chip. And, as you would expect, the incredible 16-bit Zilog Z8000 has set the microprocessor performance standards for the 1980's.

Give your imagination some of our hard, profitable facts to work with. Write: Zilog, Dept. E, 10460 Bubb Road, Cupertino, CA 95014. Or, call your nearby Zilog distributor.



THE POWER TO DESIGN THE MOST ADVANCED MICROPROCESSOR-BASED SYSTEMS IN THE WORLD. AT YOUR COMMAND TODAY. FROM ZILOG.



Meet the most versatile counter/timer and parallel I/O ever made. Zilog's Z8036 CIO.

Now there is an incredibly flexible way to time and count external events plus control peripheral I/O interfaces in real time. It's Zilog's new Z8036 CIO. The Z8036 offers the user 20 I/O lines with two fully programmable I/O ports with optional handshake signals (2 and 3 lines), and pattern recognition logic for each port. It also has three independent 16 bit counters/timers each with three external input lines and one counter output line with programmable duty cycle.

Zilog

An affiliate of EXXON ENTERPRISES INC.

CIRCLE 79 ON INQUIRY CARD

New iSBX™ Multimodule™ boards

Intel® introduces a whole new dimension in configuring single board computer systems.

Intel pioneered the concept of flexible microcomputer *system* design in 1976, with our family of iSBC™ single-board computers interfaced via the Multibus™ system bus—presently accepted as the industry standard.

Now we've extended this well-accepted concept to *board*-level design: A new generation of Multimodule boards interface to iSBCs via the new iSBX bus. So now you have a second design option. You can expand systems in large increments with Multibus boards. Or in smaller, more economical increments with Multimodules.

The key to configuration flexibility

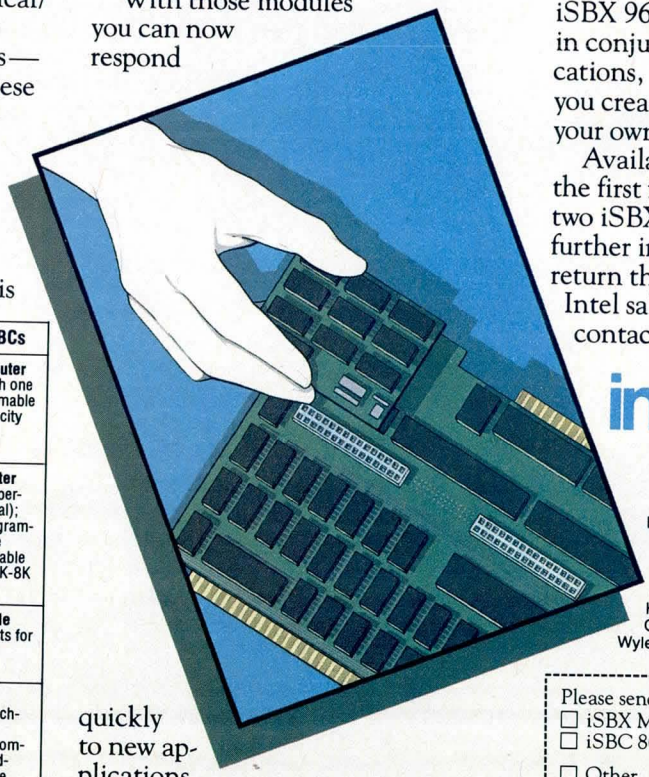
The iSBX bus—the first physical/electrical interface for direct on-board expansion of iSBC systems—assures compatibility between these systems and the emerging Multimodule product line.

Present on all future Intel single-board computers, the iSBX bus saves design time and space, and facilitates fast, easy upgrading. System performance is also improved because Multimodules tie directly to the iSBC internal bus. Connection to the iSBX bus is made with a set of rugged connectors—one on the iSBC board, the other on the Multimodule itself.

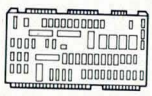
The new Multimodule family

Multimodules represent a whole new family of plug-in expansion boards. They allow you to add a variety of special performance features to your existing iSBC system. Currently available add-ons are shown below. Soon you'll also be able to add other Multimodules for D-to-A and A-to-D conversion, communications, peripheral interfaces—and more.

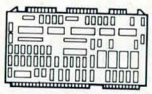
With those modules you can now respond quickly to new applications opportunities. Examples? Take data acquisition or industrial control: to add extensive I/O processing power, you simply plug in the iSBX 350 board. Or consider communications networks. Now there's no need to add entire USART boards; just use the iSBX 351 unit. In laboratory control applications, instead of an independent math processor, now you can choose the more economical iSBX 331 or 332 math modules.



New Multimodules and iSBX Bus-compatible iSBCs



iSBC 80/10B Single Board Computer
8080A-based microcomputer with one iSBX bus connector; 48 programmable I/O lines; one USART; timer; capacity for 1K-4K bytes RAM; up to 16K EPROM



iSBC 80/24 Single Board Computer
8085A-2 based microcomputer operating at 4.8 MHz (2.4 MHz optional); two iSBX bus connectors; 48 programmable I/O lines; one USART; three programmable timers; programmable interrupt controller; capacity for 4K-8K bytes RAM; up to 16K EPROM

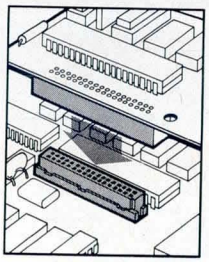
iSBX 350 Parallel I/O Multimodule
24 programmable I/O lines; sockets for inverting and noninverting transceivers

iSBX 351 Serial I/O Multimodule
Programmable synchronous/asynchronous communications channel; standard RS232C or RS449/422 compatibility; software-selectable baud-rate generation; two programmable 16-bit BCD or binary timers/event counters

iSBX 331 Fixed/Floating Point Math Multimodule
Fixed point single- (16-bit) and double- (32-bit) precision arithmetic; floating point single- (32-bit) precision functions; floating-to-fixed and fixed-to-floating point conversions; transcendental functions

iSBX 332 Floating Point Math Multimodule
Single- (32-bit) and double- (64-bit) precision arithmetic; compatible with proposed IEEE format and existing Intel floating point standard.

New Multimodule-compatible iSBC boards



iSBX 960-5 Connector

Intel's new 8-bit iSBC 80/10B and 80/24 single-board computers are the first of many iSBCs to offer iSBX Multimodule expansion capabilities. Both are improved versions of widely used iSBC boards. (See table).

Custom tailoring, too

For users who want to design their own Multimodule boards, Intel offers iSBX 960-5 connectors. When used in conjunction with the iSBX specifications, this set of connectors lets you create modular boards that meet your own unique requirements.

Available from Intel today are the first four iSBX Multimodules and two iSBX-compatible iSBCs. For further information, or to order, return this coupon or call your local Intel sales office or distributor. Or contact Intel at the address below.

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Please send information on:
☐ iSBX Multimodules ☐ iSBC 80/10B
☐ iSBC 80/24 ☐ Configuration Guide
☐ Other _____
☐ Please have a Sales Representative call.

Name _____

Title/Organization _____

Address _____

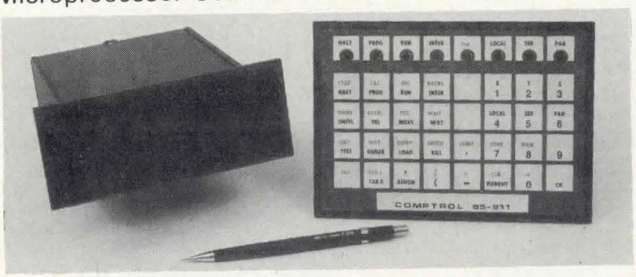
City/State/Zip _____

Phone _____

Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. Telephone (408) 987-8080.

Digital Panel Meters

Microprocessor Controlled Meter



The self-contained microprocessor controlled IMC 85-910 intelligent meter contains microprocessor, memory, interface, alphanumeric display, card rack, and power supply in a single NEMA enclosure. A plug-in keyboard assembly option mounts externally. Other options fit into the card rack. Containing all of the primary elements required for an industrial system, this meter is intended for industrial control and display applications. It has been introduced by Comptrol Inc, 9505 Midwest Ave, Cleveland, OH 44125, to increase display speed in small systems.

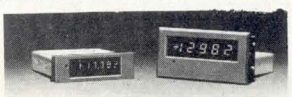
Features include an 8085A microprocessor with 3.072-MHz clock; 8-char red LED display with 0.54″ (1.37-cm) high characters; provision for 8k x 8 EPROM; 1.5k x 8 system RAM (including 1k CMOS); power fail monitor and memory protect; two programmable timers and a buffered 60-Hz input; four prioritized vectored interrupts; 40 general purpose I/O lines with 14 optically isolated inputs; differential quadrature tachometer interface; asynchronous serial I/O capability in RS-232-C, RS-422, or RS-423 formats; and software drivers for display, USART, and keyboard functions. Options include a 32-key (4 x 8) array, sealed keyboard assembly with 8 LED status lights, power supplies, and I/O system adapters. Other options are being developed.

Battery backup life for the CMOS RAM is 5 year min, 7 year typ. Power requirements for the meter are 5 Vdc at 650 mA and ±12 Vdc at 40 mA. Operating environment ranges are 0 to 55 °C at 0 to 90% RH noncondensing. Case size is 2 x 4.7 x 6.75″ (5.1 x 11.9 x 17.1 cm). Bezel size is 2.5 x 6.0 x 0.25″ (6.4 x 15.2 x 0.64 cm). Unit weight is 1.5 lb (0.7 kg).

Circle 448 on Inquiry Card

Process Control Meter

IMPAC™ 32A and 32B digital panel meters from Velonex, 560 Robert Ave, Santa Clara, CA 95050, replace analog control panel meters in process applications. LED readouts are 0.2″ (5 mm) or 0.33″ (8.4 mm). Auto zero of 5 times/s eliminates drift or offset error for a worst case instrument error of 0.4%. The meters accept 4- to 20-mA, 10- to 50-mA, and 1- to 5-Vdc inputs. In each case the readout is 000 at the lower limit and 100 at the upper. Front panel areas are 1.7 or 4.4 in² (11 or 28.4 cm²).



Circle 449 on Inquiry Card

Remember When We Had To Go To Different Stores for Math Processors, Industrial I/O and Sensor Conditioning.

Your challenges are too complex to depend on modules that come from different sources -- especially modules that were not designed for hostile plant environments. We now have a broad line of modules that covers virtually all industrial applications.

But modules are only part of our story. XYCOM offers a broad line of packages, modules and software designed specifically for industrial applications. We even have analog subsystems that interface directly to a broad range of primary sensors. Our growth in the highly specialized industrial microcomputer field has caused us to be referred to as 'The Hardhat Computer People'—and with good reason. The trend today is to put the control or target computer out on the plant floor with the operator. To do so, you've got to have equipment that is designed, built and tested specially for the hostile plant environment. Simply adapting general purpose hardware isn't the answer.

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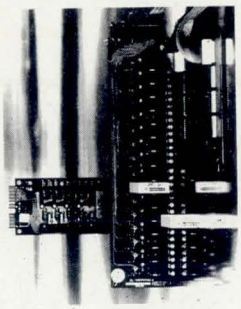
DC & AS BRIEFS

I/O Systems and Devices

Industrial I/O Interface

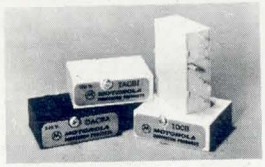


Direct microprocessor control of industrial ac and dc circuits in any mix can be attained with I/O interface modules announced by Wintek Corp, 1801 South St, Lafayette, IN 47904. The interface consists of a mounting board for 8 or 16 fully encapsulated plug-in I/O modules, and a cable assembly to a parallel I/O module. All inputs and outputs are optically isolated and fused, have an LED indicator light, and terminate with industrial barrier strip lug nuts.

Circle 450 on Inquiry Card

MOS Compatible I/O Modules

Built-in buffering in I/O modules capable of direct interface with all MOS logic, including CMOS, as well as microprocessor circuits and bipolar logic permits operation with input currents as low as 50 μA. Input impedance on various models is high, ranging from 20 to 200 kΩ, and noise immunity on some models meets the IEEE 472-1974 common mode specifications. The modules, introduced by Motorola Subsystem Products, PO Box 20923, Phoenix, AZ 85038, are completely interchangeable with the company's previously available (and other equivalent) I/O modules that require external components.



Models IACB and OACD are standard 120-Vac devices, IACBA and OACBA are standard 240-Vac devices, and IDCB and ODCB are standard dc devices. Models IACBI, OACBI, IACBAI, OACBAI, and IDCBI—comparable to models without the I-suffix—have the noise immunity feature. All models operate with logic systems ranging from 3.3 to 26.5 V. OACB series have zero voltage switching, and IDCB units provide logic to logic capability.

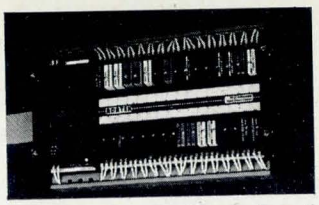
Circle 451 on Inquiry Card

Reed Relay Output Modules

Intended for control application requiring sealed contact interface, B592 and B596 500 series modules from Gould Inc, Modicon Div, 155 W Big Beaver Rd, Troy, MI 48084, can switch a wide range of ac and dc signals. Each mercury wetted relay output can handle 2 A at 300 Vac. A coil side LED indicator displays coil status. Each output is protected by a 3-A fuse and a filter network. Contact life is rated at 10M operations at rated load.

Circle 452 on Inquiry Card

Microcomputer I/O System



The RP32 acts as an interface for on/off control between microcomputer parallel I/O ports and industrial process loads and sensors. Transducers can be connected to any of 32 channels, each of which accepts a standard, optically isolated plug-in module. A 16-position thumbwheel switch allows addressing of up to 16 interfaces on one cable for possible expansion up to 512 I/O channels. Direct connection is possible to most common microcomputer boards; others are field strappable. All plug-in modules can be enabled/disabled simultaneously by computer command, allowing the microcomputer to conduct complete I/O system diagnostics while the process loads and sensors are unaffected. Introduced by Adatek, PO Box 1588, Sandpoint, ID 83864, the system operates at either 5 Vdc regulated or 8 to 12 Vdc unregulated. Current is 1 A.

Circle 453 on Inquiry Card

Interface Modules

Industrial control input modules announced by Opto 22, 15461 Springdale St, Huntington Beach, CA 92649, are available for both ac and dc inputs. They are intended for 5-V logic systems and fit on PC boards. The ac version is for 120- or 240-V input, the dc version for 10 to 32 V.

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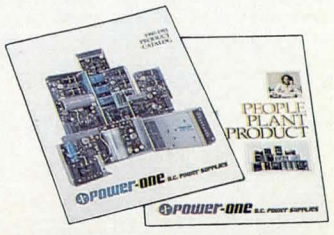

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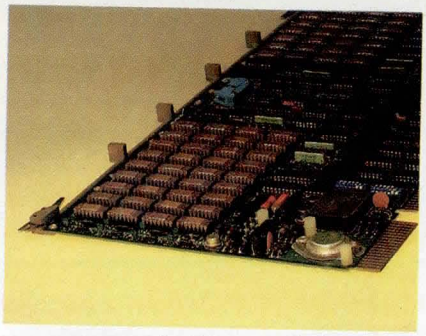

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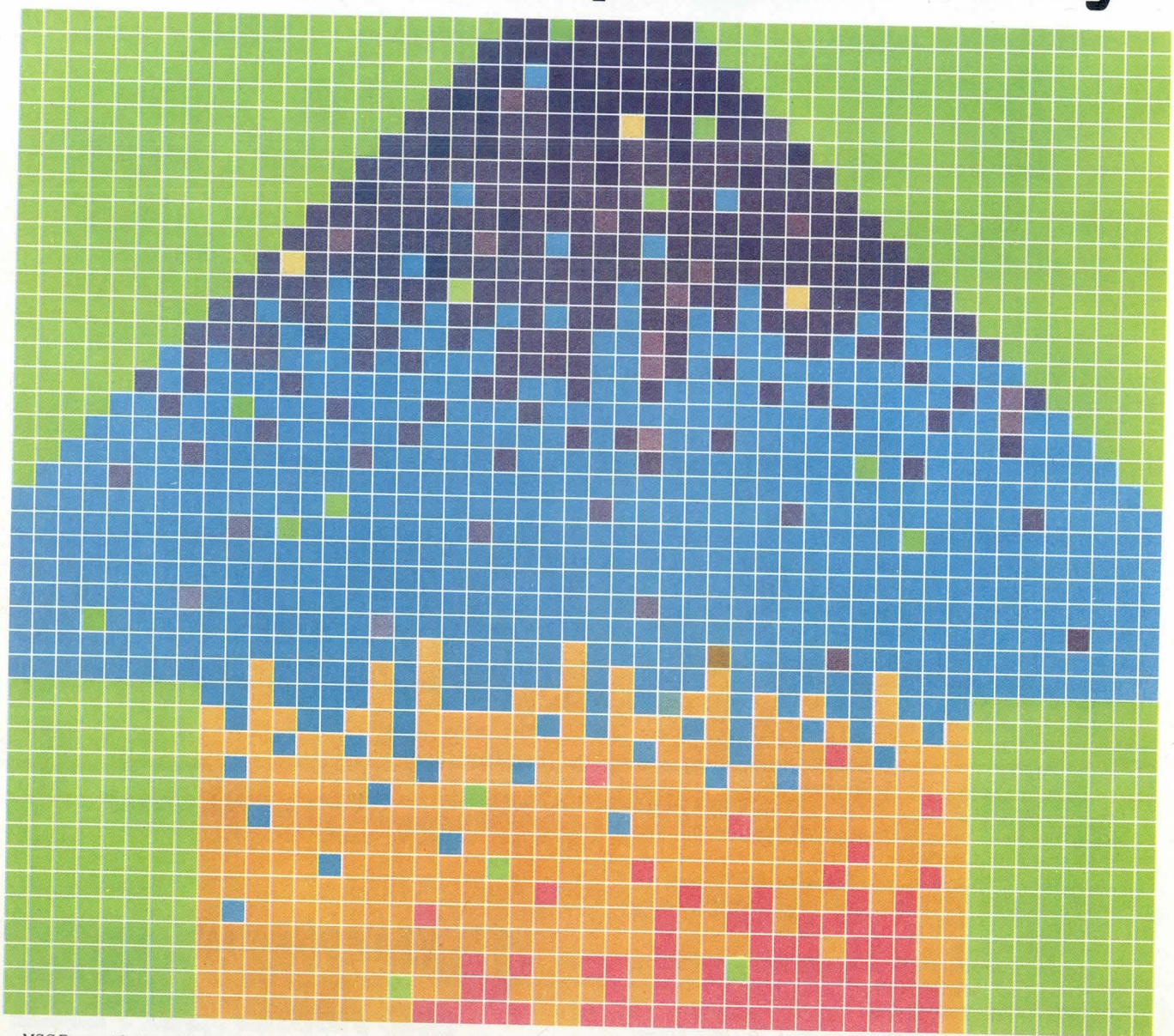

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ECC CHIP REDUCES ERROR RATE IN DYNAMIC RAMS

Integrated circuit offers single error correcting and double error detection to protect dynamic random access memory data in a wide variety of 8-, 16-, and 32-bit microprocessor and minicomputer applications

Dusty Morris

Motorola Semiconductor Products, Incorporated
5005 E McDowell Rd, Phoenix, AZ 85008

Richard W. Hamming published his first paper on error detection and correction 30 years ago. Yet, now the technique is applicable for error detection and correction chips that can be used with 8-, 16-, and 32-bit, or larger systems. In addition, the greater density and smaller geometries, with less stored charge, of 64k-bit dynamic random access memory chips make them increasingly susceptible to errors induced by alpha radiation. These characteristics make error detection and correction even more imperative.

Hamming Codes

Various error detecting and correcting schemes are in use. Parity circuits provide the simplest single error detection method, the counting of the number of binary 1s in each word. A single parity bit added to the data word records whether the number of 1s was odd or even, thus detecting single errors for any number of data bits. However, parity circuits will not determine the error location within the data.

By using more check bits, a code can be devised to determine the location of any number of bit errors and allow their correction. A Hamming parity check code with check bits generated from selected bits within the data word is such a code. The selection of data bits used to generate each of the check bits varies among error check and correct (ECC) chip designs. Certain arrangements offer such advantages as allowing 8-bit usage of a 16-bit ECC chip or easy expandability to larger word sizes. All Hamming code error correction circuits have two principles in common: the check bits are generated directly as a parity function of their associated data bits, without regard for other check bits generated from different data bits; and, the parity tree outputs produced during error checking, called syndromes, uniquely define the location of the error within the data word. Each individual error that might occur in either a data bit or a check bit has a unique syndrome used to identify the erroneous bit and correct it, by complementing its value, when required.

In addition, Hamming codes allow single-error correction (SEC). Adding one parity bit to a Hamming code SEC scheme upgrades the capability to SEC with double error detection (DED). However, as in the case of simple parity checks, only the fact of a double error is discovered, not its location. Also, adding DED to any SEC Hamming code increases the number of check bits by one.

As taken from information theory, the ratio of data bits to the total number of data and check bits, for an error detecting or correcting code, is called its rate. Another way to measure this relationship is overhead, the ratio of check bits to data bits. For SEC, it must be true that $2^m \geq n + 1$,

where m is the number of check bits and n is the total number of check bits and data bits. Adding one additional check bit for DED gives the maximum number of data bits protected by any number of check bits as $2^{(m-1)} - m - 1$.

Table 1 shows the number of data bits protected by various numbers of SEC, DED check bits. Table 2 gives the SEC, DED overhead for various data word sizes. For example, 16-bit data words require six check bits resulting in 37.5% overhead. Eight-bit data words require five check bits, accounting for 62.5% overhead, almost twice the figure for 16-bit words. Thus, in any implementation, ECC incurs a smaller relative cost penalty for 16-bit processors than for 8-bit machines.

TABLE 1

Data vs Check Bits

	5	6	7	8
Data Bits	4-10	11-25	26-56	57-119
Total Bits	9-15	17-31	33-63	65-127

TABLE 2

Overhead vs Data Word Size

	8	16	32	64
Check Bits	5	6	7	8
% Overhead	62.5	37.5	21.9	12.5

The ECC Chip

Features

ECC chips provide a link between microprocessors, minicomputers, and memories that detects and corrects memory data errors. The MC34040, a SEC, DED device for 16-bit data words specifically designed to allow processing of 8-bit data simply by supplying binary 0s for the unused bit positions and ignoring the sixth check bit, satisfies both 8- and 16-bit system requirements. However, because 8-bit operation incurs a much higher proportional overhead than 16-bit operation, the better way to implement an 8-bit ECC system would be to store and retrieve 16-bit memory data, using the least significant address line to select high or low order bytes. Of course, this would require a read-modify-write cycle to operate on two bytes of data at a time.

Most 32-bit systems require two MC34040 chips to accomplish error detection and correction in two stages. First, ECC is performed in parallel on each half of the data, with each chip passing partial syndrome information to the other; then the complete syndrome is assembled. However, in this particular ECC design, system expansion to 32 data bits requires no additional hardware.

In the instance of a catastrophic event such as accessing nonexistent memory, or a total memory failure, all 0s or all 1s may appear as data. These errors could go undetected, since it is not always possible to detect more than two simultaneous errors. The ECC chip ensures against such occurrences by detecting errors that produce all 0s or all 1s as data.

In addition to the Hamming code check bits, individual parity bits B0 and B1 allow parity testing of 8-bit data bytes. Data and check bits are latched into the input data register (IDR) for input and into the output data register (ODR) for output. The basic timing control signal, latch enable (LE), controls latching and the six syndrome out lines (S0 to S5) that supply the Hamming code syndrome generated during a read or correct cycle. When LE is high, the partial syndrome calculated from the input data and check bits is supplied. The total syndrome latch (TSL) latches the complete syndrome field when LE goes low, supplying the complete syndrome. If ECC were implemented in a 16-bit system without error logging, there would be no need to bring the syndrome off the ECC chip. Instead, it would be used only on the chip to correct the erroneous bit. The MC34040 makes the syndrome available off the ECC chip to allow error logging and to provide easy expandability to 32-bit applications.

Each of the 8-bit, output data bytes may be addressed independently through use of output byte control lines OB0 and OB1. These lines control the 3-state outputs, with OB0 handling D0 to D7 and OB1 handling D8 to D15. The two error flags are No Error (NE) and Multiple Error (ME). When a memory read is performed and the proper data and check bits have been latched in, NE will go high to indicate that no error exists. If one or more errors occur, this signal will be low. If it is in a generate or latch data register mode, NE will be low for an input parity error. In any event, it may be latched externally on the falling edge of LE. ME, in turn, will be high when two or more errors occur and low when no error or one error exists and may also be latched externally on the falling edge of LE.

Operating Modes

Three mode inputs, M0 to M2, shown in Table 3, select one of eight possible operating modes. In addition to the check (read without correct), check and correct (normal read), and generate (write) modes, the ECC chip provides an initialize to 0 generate mode and a variety of diagnostic modes using alternative input in conjunction with a diagnostic register. The check mode performs a normal read without correction and could be used by diagnostic software to recover memory data. Syndrome bits are calculated from the latched input data, in this mode, and error flags are valid once the complete syndrome becomes available. If enabled by OB0 and OB1, uncorrected data and check bits are supplied as output. The check and correct mode performs a normal read from memory with single-error correction by recovering memory data and correcting single-bit errors in either the data bits or

the check bits. Multiple errors are detected but no correction is performed. Corrected data and check bits are then supplied as output when enabled by OB0 and OB1.

There are two diagnostic modes that complement the two memory read modes just described. In one, the content of the diagnostic register is used for parity calculation in place of the check bits latched at the input, the error flags remaining active, in this mode, but with no correction performed. The other diagnostic mode substitutes the complete syndrome and the check bits for the IDR data latched into the ODR. Syndrome bits S0 to S6 supplant D0 to D6, in this mode of operation, while C0 to C5 replace D8 to D13. The check bits also appear on the check bit outputs. Single errors in the input data are corrected, and the central processing unit (CPU) can access syndrome and check bits generated for the input data word.

When data are written to memory, four generate modes calculate or otherwise provide check bits. The complete syndrome calculated for the input data appears at the check bit output drivers, in normal generate mode. OB0 and OB1 can enable the input data as output. A second generate mode performs memory initialization by setting all data output bits to 0 and producing the proper check bits for 0 data. Memory controllers might use this mode to initialize memory before attempting to read it for the first time, thus preventing errors that would almost certainly result from accessing random data.

In still another mode, diagnostic register content can be supplied at the check bit outputs, replacing the calculated check bits of the syndrome. The last mode of operation latches input data bits D0 to D5 into the diagnostic register. A write to memory should be performed in this mode to initialize the diagnostic register before any diagnostic mode is used.

TABLE 3

Mode Selection

Mode Inputs			
M0	M1	M2	Mode Description
0	0	0	Check (No correction)
0	0	1	Check and correct
0	1	0	Check, diagnostic register substituted for check bit inputs
0	1	1	Check and correct, syndromes and check bit inputs substituted for data out
1	0	0	Generate
1	0	1	Generate, force data out = 0, with proper check bits
1	1	0	Generate, diagnostic register substituted for check bit outputs
1	1	1	Latch diagnostic register

Functional Operation

When two MC34040 ECC chips are used in parallel to handle up to 32 bits of data directly, partial syndrome bits pass between the parallel devices. Each chip combines partial syndromes to form the complete syndrome without additional hardware. Parity trees calculate the partial syndromes from the input data and check bits to generate the total syndrome field. Each syndrome bit reflects the parity of its associated data bits, with partial syndrome bits 0, 2, 3, and 5 chosen as even parity bits and partial syndrome bits 1 and 4 as odd parity. This means that check bits C1 and C4 will be set to yield an odd number of 1s when combined with the designated data bits, and C0, C2, C3, and C5 will yield an even number of 1s, allowing detection of catastrophic errors, when all data and check bits are forced high or low.

In the generate mode, the complete syndrome appears at the output drivers as the check bits. In the check and correct modes, the complete syndrome is applied at the syndrome out pins and is used to detect and locate any errors. Information in the syndrome out lines can be latched for error logging and accessed by the CPU. The CPU rereads the same memory address after setting the mode of operation to substitute the syndrome and check bits for the output data.

The complete syndrome field is used to detect and correct errors. An all 0 syndrome field indicates that no errors exist. A single error asserts an odd number of syndrome bits, a double error asserts an even number, and some multiple errors generate unused syndrome codes. However, when a double error exists, ME is always asserted.

Read Cycle—LE latches data for a read cycle into the IDR. The parity trees generate a partial syndrome pattern from the input data and the check bits. When two ECC chips are used in parallel, these partial syndromes are combined with the partial syndrome input to form the complete syndrome field used to detect single and double errors and to correct single errors. In this case, the error flags become valid only after the complete syndrome has been generated. Single-bit errors are corrected before data are latched into the ODR when correction is enabled. Double errors are not corrected; instead, the IDR data are transferred into the ODR unaltered.

Write Cycle—Both read and write cycle data enter through the input registers. Partial syndromes are generated and passed between the two chips when they are used in parallel. Partials are again combined and latched to form the complete syndrome. Detection and correction are not performed, and the syndrome is applied directly to the check bit output drivers to be stored in the memory. Input data are also transferred to the ODR, ready for output under control of OB1 and OB2.

Tradeoffs

ECC chips currently available are in 28-pin packages. The MC34040 requires 48 pins, allowing more features. The 28-pin component handles a 16-bit data path, implements SEC, DED, and uses only two control inputs; however, it does not have diagnostic capability, 8-bit data handling, or expandability. The tradeoff between package size and functional capability suggests the use of the 48-pin component for diagnostics and in 8-, 16-, or 32-bit systems.

Like earlier components, the MC34040 has bidirectional ports. If bidirectional data paths with 3-state capability were not used, the ECC chip would have a data input and a data output port for both the data and the check bits. This would place the ECC chip in line, in the signal path, increasing the no-error data delay and requiring an additional 22 pins for data and check bits, which is undesirable. With the 3-state bidirectional data bus, memory data are already on the bus and a cycle can be considered complete when the NE flag shows valid data, thereby reducing cycle time. Only when the ECC chip makes a correction is it necessary to transfer data from the chip to the bus (with the resulting turn off and turn on delays). Even if an extra cycle is needed to correct the error, the delay seems a good tradeoff as errors occur so infrequently.

Interface

In Fig 1 a 0.5M-byte memory is interfaced to the MC68000 in a demonstration system using the basic ECC system. The ECC chip is installed on the 16-bit data bus between the memory and the CPU. Six check bits are bused between the memory and the ECC chip, with flags accessed by the CPU for error handling. Because the ECC chip lacks an address bus interface, it places no limit on the memory size other than the word size restriction. In this case, the system accesses a 0.5M-byte dynamic random access memory (RAM), 256k x 22, using the MC34040 for error correction.

All CPUs have control lines in addition to their data and address buses. The MC68000 uses Address Strobe ($\overline{AS}$) to signify valid address outputs. It uses Upper Data Strobe ($\overline{UDS}$) and Lower Data Strobe ($\overline{LDS}$) to signal that the data bus bytes are valid or ready for data. $\overline{UDS}$ and $\overline{LDS}$ allow separate access to bytes of bus data. Data Transfer Acknowledge ($\overline{DTACK}$) and Bus Error ($\overline{BERR}$) are handshake inputs. $\overline{DTACK}$ terminates a completed read or write cycle, and $\overline{BERR}$ informs the CPU of a problem with the current cycle. With the ECC chip interface, $\overline{BERR}$ can be used to invoke a multiple error recovery routine.

Row Address Select ($\overline{RAS}$) and Column Address Select ($\overline{CAS}$) time the address multiplexing required by dynamic RAMs. An MC3480 dynamic memory controller provides timing of the $\overline{RAS}$ and $\overline{CAS}$ signals, and the required refresh cycles, and handles the read/write signal to memory.

Timing inputs to the $\overline{RAS}$ and $\overline{CAS}$ signals and the refresh cycles are the refresh clock and five timing signals for the memory cycle, t_1 to t_5, in sequence. One shots, MPU signals, high frequency counters, shift registers, or delay lines can be used to generate the required timing signals. Delay lines are used in Fig 1 because high frequency signals were not available, and it was not considered desirable to adjust one shots. $\overline{AS}$ and a memory address residing on the dynamic RAM board begin a CPU memory cycle. Delay line timing generates signals from $\overline{UDS}$ or $\overline{LDS}$. Because of the variable length of a CPU word or byte read/write cycle, t_5, which terminates the memory cycle, is derived from the end of Data Strobe ($\overline{DS}$) rather than from the delay line signal. $\overline{DS}$, an internal systems signal, the logical OR of $\overline{LDS}$ and $\overline{UDS}$, is used in place of $\overline{AS}$ to permit the use of the MC68000 or any read-modify-write cycle instruction.

In this design, the RAM must be refreshed at a 64-kHz rate. If a refresh cycle is deferred too long, the memory could fail to retain data; so, when a decision between CPU access and refresh access must be made, refresh has to have priority. The CPU signals $\overline{AS}$, $\overline{UDS}$, and $\overline{LDS}$ remain stable indefinitely. The refresh cycle completed, the CPU can then access memory. When the system is asynchronous, it is conceivable that both the CPU access status flipflop and the refresh status flipflop could attempt to set simultaneously. Normally, the first flipflop to set will lock out the other until completion of the current cycle. However, owing to propagation delay in the flipflop output buffers and the input gating, the two flipflops could be set simultaneously without locking out the other. To prevent an erroneous cycle at this time, the refresh flipflop resets the CPU flipflop and resolves the contention problem.

Additionally, the refresh signal controls time delay signal multiplexing. As refresh has priority, timing errors do not occur in the sequence. Multiplexing is set for CPU access when the refresh cycle is inactive. To allow for variable length CPU cycles, $\overline{UDS}$ or $\overline{LDS}$ initiates the timing generation cycle with the delay lines with the end of $\overline{DS}$ initiating the end of the cycle. At the end of this cycle, 150 ns added before the status flipflops are reset provides precharge time for the dynamic RAM by holding off further access to memory long enough to satisfy memory timing requirements.

In Fig 2, data read from memory are valid 135 ns after $\overline{CAS}$ goes low. (All times are based on use of the MCM6664-20 memory parts with 200-ns access time.) Then, 50 ns after valid data are presented to the ECC chip, NE and ME become valid, LE having been asserted to latch the input data, and

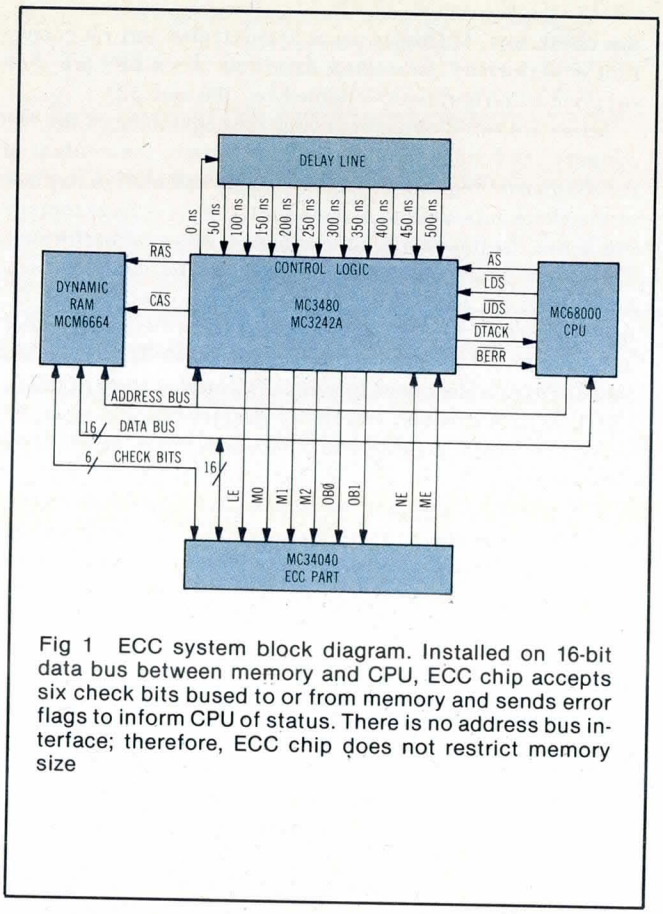

Fig 1 ECC system block diagram. Installed on 16-bit data bus between memory and CPU, ECC chip accepts six check bits bused to or from memory and sends error flags to inform CPU of status. There is no address bus interface; therefore, ECC chip does not restrict memory size

the interface logic having determined which of three conditions exists:

No errors (NE = 1, ME = 0— No correction is needed and the cycle is terminated by asserting $\overline{\text{DTACK}}$. When $\overline{\text{AS}}$ ends, $\overline{\text{DTACK}}$ is negated.)

One error (NE = 0, ME = 0— Correction is needed. OB0 and OB1 are asserted, removing data from the bus and substituting corrected data from the ECC chip onto the bus. Asserting $\overline{\text{DTACK}}$ terminates the cycle.)

Two or more errors (NE = 0, ME = 1— Uncorrectable errors exist. $\overline{\text{BERR}}$ is asserted to invoke an error handling routine. The end of $\overline{\text{AS}}$ negates $\overline{\text{BERR}}$.)

In all three cases, LE and t_5 change state when $\overline{\text{DS}}$ ends, and t_5 ends the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals. Thus, $\overline{\text{UDS}}$ or $\overline{\text{LDS}}$ starts the cycle, and $\overline{\text{DS}}$ ends it. Corrected data from the ECC chip are placed on the bus only when necessary.

In Fig 3, $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$ begin the word write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are initiated by t_1 and t_3; the read/write line, ($\overline{\text{W}}$), is output at t_4; LE is also asserted, to latch input data; and $\overline{\text{DTACK}}$ begins, indicating to the CPU that the write cycle can be ended. When $\overline{\text{DS}}$ ends, t_5 terminates $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{W}}$, $\overline{\text{DTACK}}$, and LE. Data from the CPU and check bits from the ECC chip have been written to memory by this time.

A read-modify-write cycle must execute in memory when a byte write cycle is selected (Fig 4). The ECC chip needs the full 16-bit word in order to generate the proper check bits when an 8-bit byte is written to memory. When performing a byte read, the upper and the lower bytes are read from memory but only the selected byte appears on the data bus. Fig 4 shows $\overline{\text{UDS}}$ active and OB1 asserted. If the lower data byte is selected, $\overline{\text{LDS}}$ is active and OB0 is asserted instead. Either $\overline{\text{UDS}}$ or $\overline{\text{LDS}}$ starts the cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ are asserted

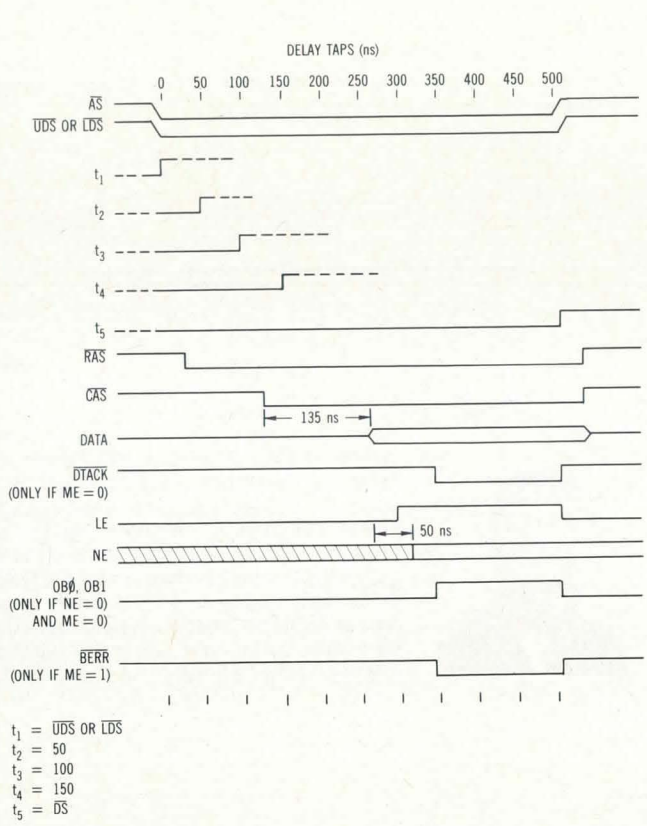

Fig 2 Read cycle timing diagram. Memory data are valid 135 ns after $\overline{\text{CAS}}$ goes low. NE and ME flags are valid 50 ns after ECC chip receives data; t_5 ends $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals that drive dynamic RAM. Corrected data are placed on bus only when necessary

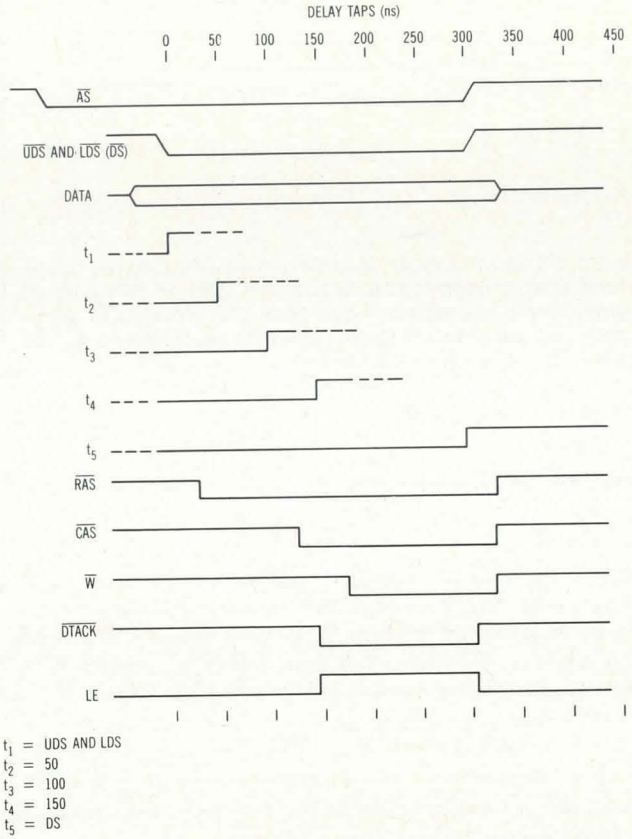

Fig 3 Word write cycle timing diagram. $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$ begin word write cycle. Then, t_1 initiates $\overline{\text{RAS}}$; t_3 initiates $\overline{\text{CAS}}$; and t_4 asserts LE, when read write line is available as output, to inform CPU that write cycle can be ended. Data and check bits have been written to memory before end of $\overline{\text{DS}}$

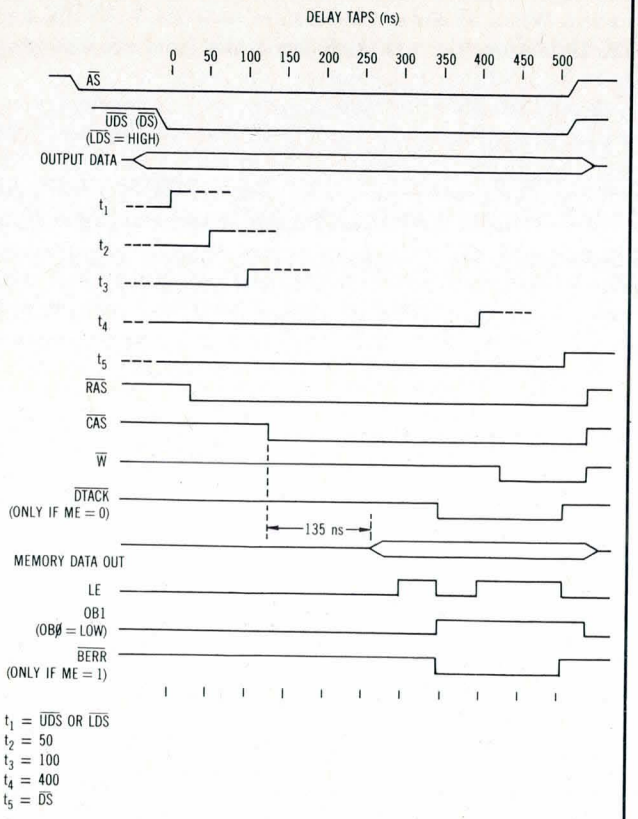

Fig 4 Byte write cycle timing diagram. $\overline{W}$ is delayed to perform a read-modify-write to memory. OB1 or OB0 outputs guarantee valid memory data. Diagram shows $\overline{UDS}$ active and OB1 asserted. If lower data byte were selected, $\overline{LDS}$ would be active with OB0 asserted

by t_1 and t_3, 135 ns after $\overline{CAS}$; valid data are read from the memory; LE then goes high to latch the input data. LE goes low 50 ns later and the error flags become valid. If no error or a single error exists at this time, $\overline{DTACK}$ is asserted. When multiple errors are present (ME = 1), $\overline{BERR}$ is asserted to abort the current cycle. LE again goes high 50 ns later, when t_4 occurs, and $\overline{W}$ drops to write. Data bits and check bits are written to memory as $\overline{DS}$ terminates the cycle. OB0 or OB1, whichever is used, remains active until $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ are negated, guaranteeing valid data to the memory.

Error Logging

In addition to the four banks (22 bits each) of 64k-byte dynamic RAM that make up the 0.5M-byte memory, memory that is accessible to the CPU at a separate address is used to log errors. When an error occurs, the memory address, syndrome, and parity bits are stored in the error logging memory which, in practice, should be a nonvolatile memory that makes error information available as a diagnostic tool even in the case of system failure or shut down.

Conclusion

Though by no means new techniques, error detection and correction have become desirable, economical, and — in many cases — necessary system capabilities. Working in conjunction with 64k dynamic RAMs, with their increased susceptability, the MC34040 ECC chip handles 8-, 16-, and 32-bit data, for any size memory, and offers full single-error correction with double-error detection. It affords convenient error rate reduction by using a proven method that is likely to become commonplace in the next generation of memory boards.

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As systems engineer in Computer/Federal Strategic Marketing at Motorola Semiconductor Products, Inc, Dusty Morris has designed a 6-language 64-key keyboard encoder using an MC3870 microprocessor, a fiber optic communication interface for a CRT terminal, and a Z80A to M6800 family interface with the MC6845 as the example. He has also been awarded two patents relating to FET circuits.

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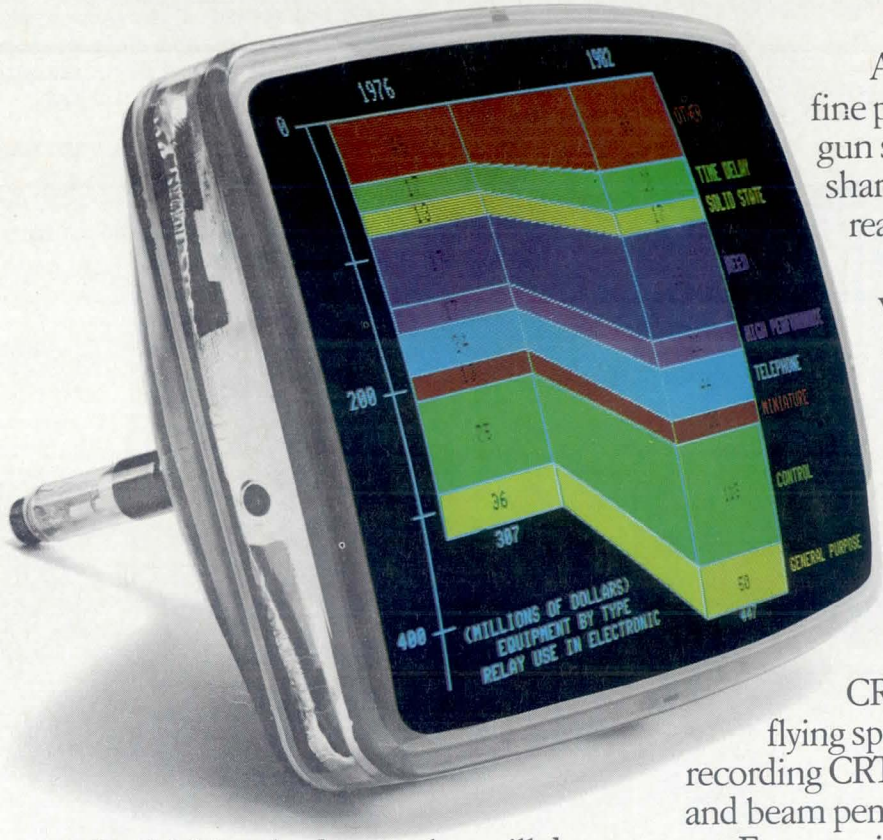

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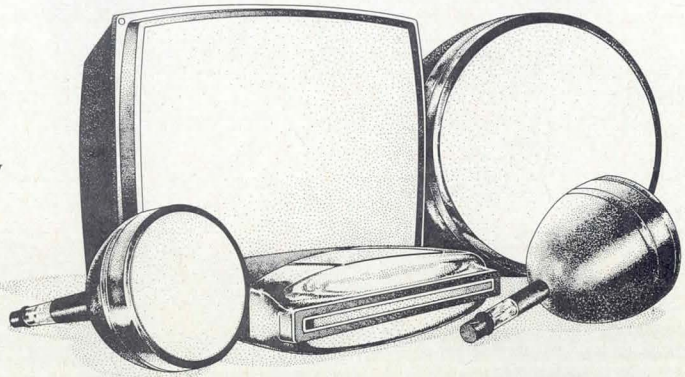

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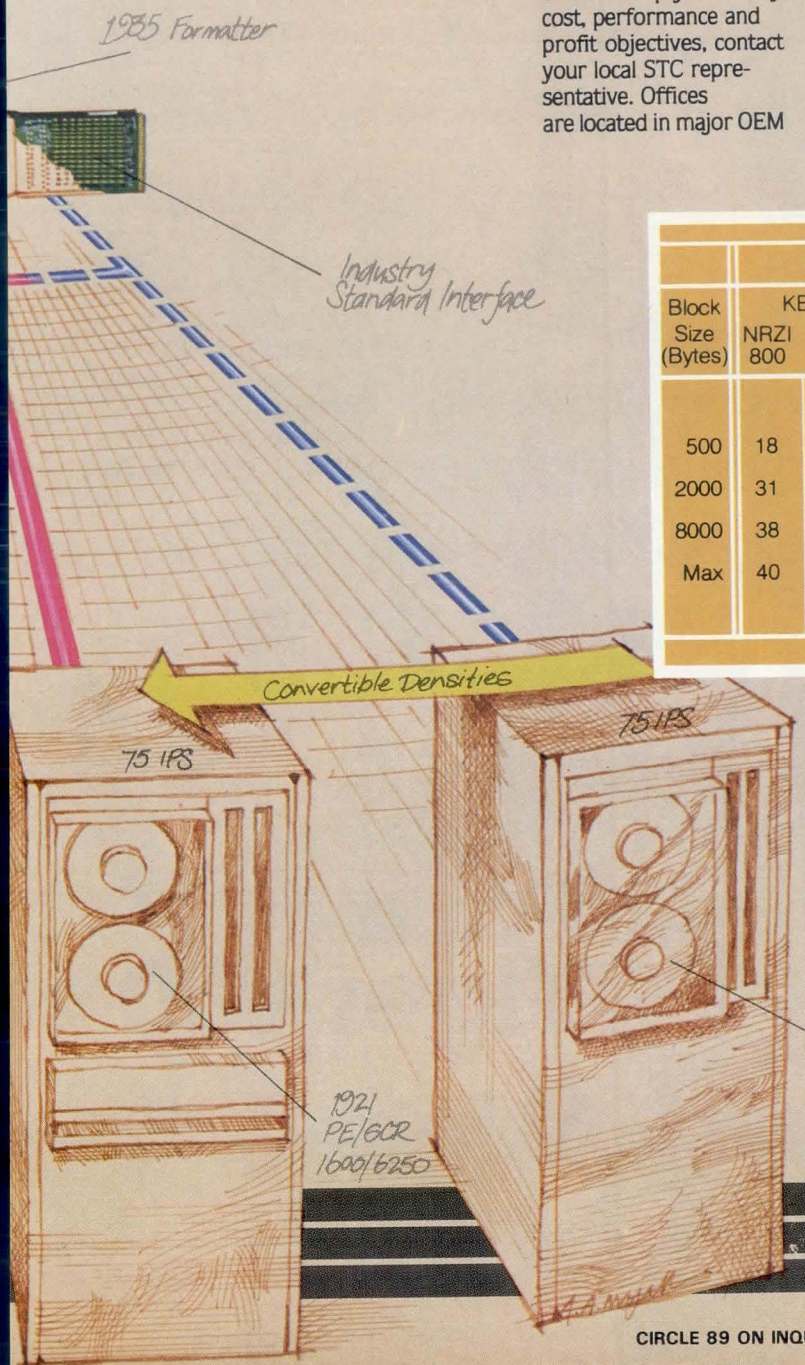
500	18	27	62	28	42	94	47	70	156
2000	31	52	156	46	78	235	77	130	390
8000	38	71	249	57	107	379	96	178	624
Max	40	80	312	60	120	470	100	200	780



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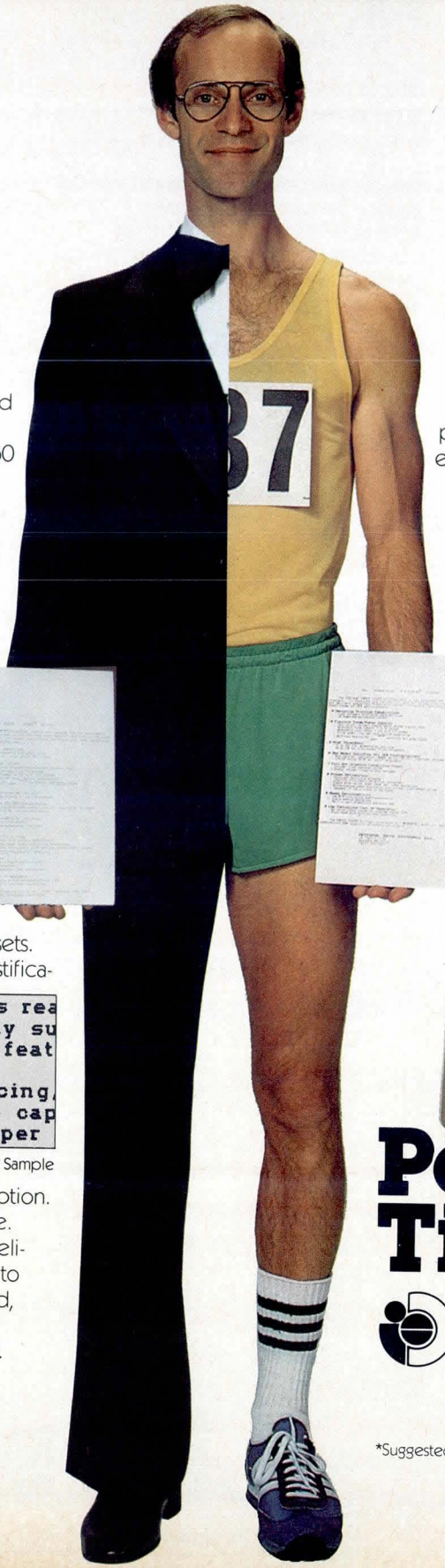

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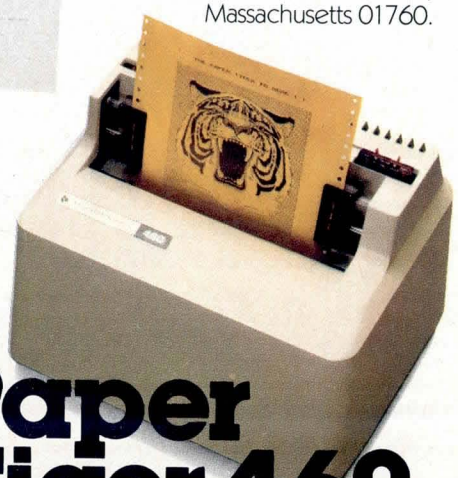

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CIRCLE 90 ON INQUIRY CARD

A BASIC TECHNIQUE FOR REALTIME SYSTEM DESIGN

A task scheduling program that requires no interrupts is an effective component of realtime system design. Hardware interface to the executive facilitates system debugging and realtime tuning

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Microprocessors have greatly simplified the design of data acquisition and process control systems by reducing hardware complexity and by providing inherently flexible software implementation. Through the use of microprocessors it is possible to integrate several distinct process functions into one control unit. In order to integrate multiple functions—each with distinct processing time requirements—into one microprocessor, it is essential that access to and management of central processing unit processing by each program be provided. Such an operation is often referred to as multitasking.

Independent programs which may be processed concurrently are called tasks (processes). Scheduling tasks for execution and transferring central processing unit (CPU) control from one task to another is the function of a special executive (supervisor) program, which manages the orderly running of system tasks so that control and data acquisition functions are performed within system design specifications. A system that performs all process functions within specified time constraints is a realtime system. Processing specifications to be met by a system in order to qualify as realtime are dependent on the individual process being monitored or controlled. Therefore, a system may provide realtime control for a slow process, yet not qualify as realtime when controlling a process calling for faster dynamics.

Most executive programs designed for microprocessors are based on concepts used for their predecessors, the minicomputers. In many instances the speed and capabilities of microprocessors are best served by utilizing a simpler technique for implementing realtime multitasking systems. Broadly speaking, executives may be characterized in terms of two parameters: the trigger mechanism used to switch processing among tasks and the manner in which tasks are scheduled for execution. Interrupt driven and task driven trigger mechanisms are most prevalent. In an interrupt driven executive, switching of execution from one task to another (context switching) is determined by the occurrence of a hardware or software originated program interrupt. In the task driven executive, context switching takes place as a result of a directive from the task being executed.

"Round-robin" and "priority" are two basic schemes for scheduling tasks for execution. In round-robin scheduling, tasks are run in fixed number sequence. Upon processing the task with the highest number, the executive transfers control to the task with the lowest number and continues the scheduling in circular fashion. In the priority scheme, each task is assigned a number based on priority, and the executive inspects the priorities of all tasks to be processed before switching from one task to the next. The task with the highest priority is given primary access to the CPU, and no other task will be run until this task terminates its

processing. Fig 1 illustrates the execution of three tasks by priority scheduling (a) and round-robin rotation (b).

Task driven executive realtime systems are easy to implement, simple to use, and, most importantly, easily adaptable to specific requirements of system functions. Design of dedicated systems with this executive is effective since special executive features required by a task can be implemented within the task. Size and flexibility of the executive are optimized by eliminating unused features of general purpose executives.

Real Time and Multitasking Concept

A realtime system is characterized by its ability to perform functions within time constraints that ensure satisfactory interaction with external process dynamics. In order to perform multiple process functions concurrently, it is essential that these functions be programmed as separate tasks. Consequently, one of the most important components of realtime system design is the selection or design of an executive program that maintains a realtime multitasking environment.

Response time—the period required by a system to perform a particular function—is a convenient parameter for the definition and evaluation of realtime operation. In interrupt driven executives, the response time is adjusted through selection of task priorities and context switching time. In a task driven executive, however, time does not play an explicit role in process scheduling, and cycle time is the variable that must be adjusted for achieving response time. Cycle time for a particular task is the interval between two consecutive executions of that task, and is a function of both the number of tasks scheduled for execution and the execution time of each task. When only one task is being processed, cycle time is minimal; it is maximal when all tasks are scheduled for execution and the longest segment of code in each task is being processed. Through proper task control it is possible to adjust the system cycle time and achieve the required response times.

Task Structure and Execution

Within the processing environment provided by a task driven executive, each task may assume one of four possible states: dormant, waiting, ready, or running (Fig 2). The task in current control of the CPU is said to be in the running state, and only one task may be in the running state at any one time. A running task releases control of the CPU voluntarily, either when it terminates its processing or when it does not require the immediate execution of a program segment. A task releases control of the CPU or invokes execution of another task through a service request to the executive. The executive is treated by each task as a coroutine and executive service is specified by the arguments of the coroutine call.

Dormant state characterizes a task which is not scheduled for execution. Tasks in the ready state gain control of the CPU (running state) whenever the task which is currently processing relinquishes control to the executive. A task goes into the waiting state when it must wait for an event that is

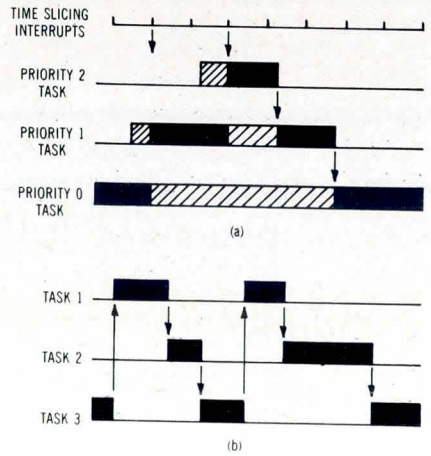

Fig 1 Priority versus round-robin scheduling. In interrupt driven system (a), bar shows time during which each task is runnable and solid portion indicates time during which task actually runs. When clock generates time slice interrupt, highest priority runnable task executes next. In task driven system (b), bar shows that each runnable task executes in sequence. When running task relinquishes CPU, next runnable task in sequence is next task to be scheduled

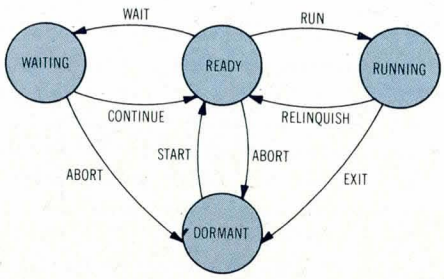

Fig 2 Task state diagram. Circles show states task may assume. Executive services on directed paths change task state. Only running task can request executive service. RELINQUISH and EXIT change state of running task that made request. Other services change state of another task. Every task must RELINQUISH or EXIT at some point

being monitored by another task to occur. Whenever that event occurs, the task with event monitoring responsibility will change the state of the waiting task into the ready state.

Executive routines available to a task can be grouped into two categories: those which affect the running task and those which affect other tasks. Among the procedures which affect the running task are EXIT and RELINQUISH. Procedures affecting other tasks are WAIT, CONTINUE, START, and ABORT.

Since control of execution proceeds under task control, it is imperative to have a task running at all times. In many systems, this running task may be an event monitor (such as a timer) that runs other tasks as a function of the time of day. Associated with the transition from the ready state to the running state, the RUN procedure itself is not an executive command; it is the automatic scheduling by the executive of a task for execution.

The simplest structure that a task may have is characterized by a program containing a single executive call. Fig 3 shows the format of such a task; tasks with this format 'execute to completion.' Once the execution of the cyclic segment is initiated, it will continue until the end, when the task releases use of the CPU through an executive program request.

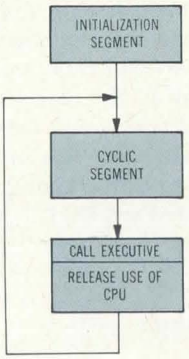

Fig 3 Basic task structure. Simplest possible task, shown here, has 2 program segments and makes 1 RELINQUISH or EXIT request. Initialization segment, normally processed only once, establishes parameters used in cyclic segment. Cyclic segment performs task functions and ends by requesting EXIT (if functions are required only once), or by requesting RELINQUISH (if functions are required periodically). Every task must contain at least 1 EXIT or RELINQUISH request

Specific procedures used to release the CPU are a function of the conditions under which the task should be reactivated in the future. RELINQUISH is used when the task requires processing during the next cycle of execution. WAIT is employed when a specific condition (event) must trigger further processing by the task, eg, the arrival of data from an input device. A task should assume the waiting state under control of another task responsible for monitoring the trigger event. Upon the occurrence of such a trigger event, the task responsible for monitoring that event should apply CONTINUE to make the waiting task ready. A task which must be processed only once uses EXIT to enter the dormant state upon completion of execution. Tasks which are infrequently used are normally maintained in the dormant state, and are scheduled for execution through the START executive routine. One task can initiate or terminate the execution of another task through a START or ABORT executive procedure. Typical use of START and ABORT is demonstrated in the emergency shutdown of a plant. Detection of shutdown conditions should cause all digital control processes to be aborted and a shutdown task to be started.

Whenever a task releases control through RELINQUISH, its execution upon return to the running state is resumed at the instruction immediately following the service call. In the basic structure shown in Fig 3, this instruction directs the transfer of program control to the beginning of the cyclic segment. When a dormant task becomes ready, its execution will start at the initialization segment.

Task Management

Grouping system functions into tasks is the initial step in task design. Typical examples of functional groupings are data acquisition, operator communication, and timekeeping. Once each system function has been assigned to a task, a classification of either critical or noncritical should be made for each. A critical task is one that must meet a specified response time, whereas a noncritical task may require prolonged execution. With this information, the design of tasks and the development of a strategy for managing execution should evolve such that response time specifications are met.

EXECUTIVE routines may be employed to eliminate CPU time wasted by waiting on a busy loop for an input/output (I/O) device (Fig 4). At the completion of a scheduling cycle, the task regains control and checks the device status. The loop to RELINQUISH on unmet condition enables a designer to specify one or more conditions for execution during the cyclic segment of a task.

WAIT plays an important role in synchronizing interdependent tasks. Consider two tasks, one performing data reduction and the other controlling the operation of a printer. Assume that the two tasks interact as follows: the data reduction task sets up a buffer with data to be printed and prepares a message for the printer task identifying the buffer location and the number of words it contains. Next, the data reduction task activates the printer task and releases use of the CPU. The data reduction task runs during every cycle, checking the status of the output task. If the printer task is active, the data reduction task relinquishes control. As long as the printer task is operational, it will output one character per scheduler cycle and relinquish control. This task control approach leads to the execution of a status check and a RELINQUISH request by both tasks for each printed character.

A more efficient utilization of the CPU may be achieved through use of the WAIT procedure. Once the printer becomes active, it calls WAIT to force the data reduction task into its waiting state. As a result, the data reduction task will not be scheduled for execution until the printer task outputs all data in the buffer, at which time a CONTINUE call is made to allow further processing by the data reduction task.

Noncritical tasks can be processed throughout several cycles by inserting RELINQUISH requests at specific points in the code in order to limit the maximum time of execution during any one cycle. An alternate technique, which can be

used to preempt processing by noncritical tasks when critical tasks need all CPU resources, forces noncritical tasks into the waiting state. When the execution of critical tasks is completed, CONTINUE procedure calls are made to restore the noncritical tasks to the ready state.

In round-robin task execution, an immediate action can be expected only of services affecting the running task (RELINQUISH and EXIT). START and CONTINUE do not result in an immediate transfer of execution to the object task; they simply cause the object task to become ready. Task execution occurs only when the task is next in line on the cyclic task list. Thus, it is important to assign contiguous numbers to tasks that must be processed sequentially with minimal delay.

Communication Among Tasks

Although tasks are independent programs, there is need for a mechanism that allows tasks to share or exchange data. Data exchange among tasks is normally implemented through the use of messages. Two data structures are used to transfer data among tasks—dynamic buffers and global common memory variables. In the dynamic buffer technique, one task sends a message to another task through EXECUTIVE routine request. EXECUTIVE selects a buffer (from a pool of unused buffers) to transfer the message, and informs the destination task of its location. The task receiving the message responds by returning an answer message to the task which generated the message. Such a technique provides efficient means for the transfer of information among tasks.

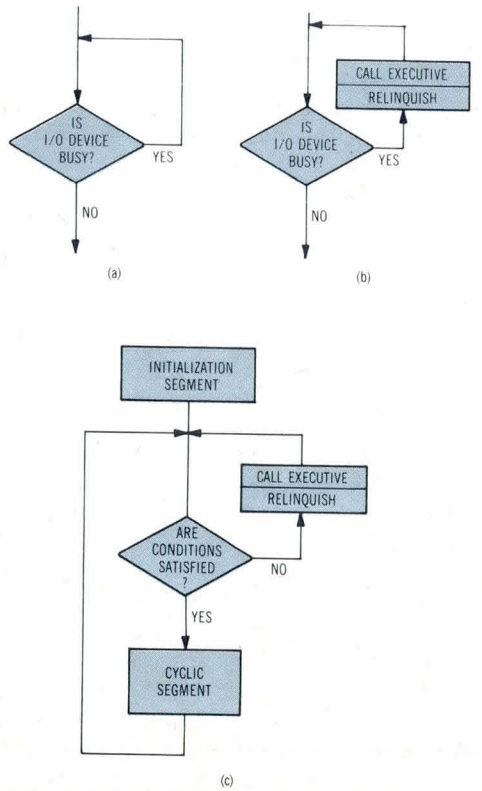

Fig 4 Executive services eliminate wait time. Conventional wait-on-busy loop (a) can be altered to RELINQUISH processor (b) and allow other tasks to run. Same technique can synchronize task with specified external conditions (c) by relinquishing processor until those conditions are met

In the global common memory technique, buffers are created in a common memory area accessible to all tasks for the purpose of intertask communication. Global common memory buffers for intertask message transfer have three basic areas: command, status, and data. Command area specifies the type of message being transferred; status area is where the receiving task indicates its action on the received message; and data area may contain data, pointers to data, or flags. Each buffer is used for the transfer of messages between a specific source task and a specific destination task. In this technique, the transfer of messages does not involve the EXECUTIVE; a handshake for the message transfer is part of the message buffer.

Due to the fixed assignment of a buffer to a pair of tasks, the global common memory technique may require more memory space than the dynamic buffer technique. However, it does not require implementation of special executive routines for allocating buffers or queuing messages to tasks. In fact, the use of global common memory for intertask message communication reduces the complexity of the executive.

Communication between the reduction task and the printer task can be implemented as follows. Whenever the data reduction task terminates processing, it sets up a message for the printer task requesting that a data buffer be printed. The command portion of the message specifies that while output is being performed the calling task be placed in a waiting state. The data section of the message contains the address and length of the data buffer. Upon receipt of the message, the printer task forces the calling task into the waiting state. When the output is complete, the printer task clears a flag in the command area of the buffer to indicate the completion of printing. A status word is then loaded into the status area to indicate the occurrence of errors or printer malfunction. Printed output involves substantial idle time between characters during which other ready tasks may run, but not the caller, which is waiting for message completion.

Design of the Executive Program

Architecture of the executive program is illustrated in Fig 5. The service dispatcher analyzes the validity of a service request and calls the appropriate executive routine to perform the procedure requested. When the service routine is completed, the scheduler is called to transfer CPU control to a task. Examining a flag set by the executive service routine, the scheduler will determine whether control of execution should return to the calling task or to the next ready task in the scheduling sequence. An executive program with the architecture shown in Fig 5 can be designed in a high level language as a subroutine.

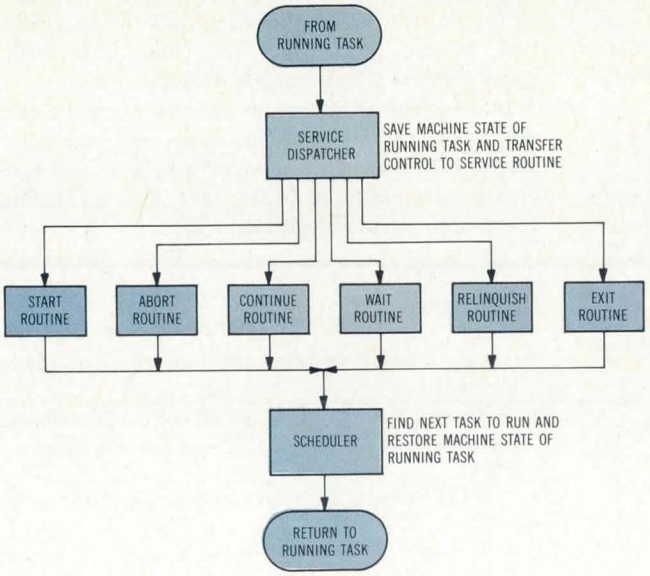

Fig 5 Realtime executive includes dispatcher and scheduler. Dispatcher verifies that request is valid in terms of Fig 2, then invokes appropriate executive procedure. Scheduler returns control to task that requested service or to next ready task in sequence, depending on procedure requested. Only RELINQUISH and EXIT suspend execution of task that requested service

Scheduling requires use of a task status table to store the state of each task. The executive service routines interact with the task status table and with the flag that specifies whether the running task retains execution or a new task must be scheduled. Each service routine must change the state of either the running task (to waiting or dormant) or the object task (to ready, waiting, or dormant) by writing the state code into the appropriate entry of the task status table. The scheduler monitors the flag to determine whether a new task must be scheduled. If it must, the task status table is searched for a ready task. This search starts at the entry in the task status table adjacent to that of the executing task.

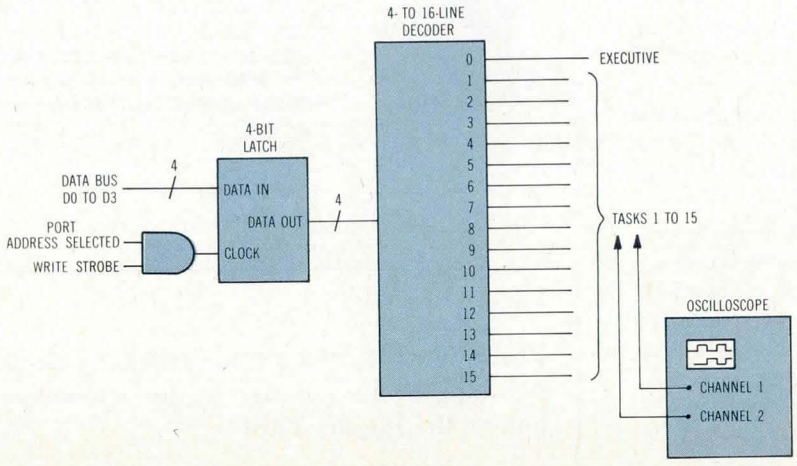

Fig 6 Hardware debugging aid. Device measures task execution time and executive overhead. Executive call sends binary zero to latch. When scheduler transfers control to task, binary task number is sent to latch. Demultiplexer decodes task number. Task cycle time is time between consecutive pulses on line that corresponds to task

Entry into the executive from a task is accomplished by calling the executive subroutine; upon service completion, the scheduler returns control to the scheduled task through a return from subroutine. Thus, in terms of the calls made to the executive and its return to the task, the executive is a subroutine. In view of the fact that the executive may return to a program (task) that is distinct from the calling program, however, it should be classified as a coroutine.

Design of the executive requires two routines which generally cannot be written in high level language. One of the subroutines is used by the service dispatcher to save the stack pointer of the running task. Each task requires a stack to store the machine state when a subroutine call is made. A similar routine is used by the scheduler to restore the program counter and stack pointer of the task scheduled to run. Both routines require access to machine registers which may not be supported by high level languages.

Debugging of a realtime system designed with this executive may be facilitated by use of the hardware accessory illustrated in Fig 6. Measurement of the execution time of tasks and the overhead of each executive procedure request is easily made with the aid of this hardware port, which identifies the current running task by electrical signals. After the executive is entered, a binary zero is sent to the output latch, and when the scheduler is ready to transfer control to a task, the binary number of this task is sent to the latch. A demultiplexer is used with the latch to decode the binary number into a 1-line signal. Activities of the executive are identified by pulses in line 0. By monitoring the line corresponding to a task (lines 1 through 15), one can determine the cycle time as the time between the start of consecutive pulses; duration of a pulse expresses execution time for the corresponding task. Providing task execution status without interfering with the system operation makes this device extremely effective in system debugging.

Design Extensions

In many situations, it is desirable to include tasks that facilitate system design as part of the system software. Typical among such tasks are the timer task and I/O tasks. A timer task provides the time of day, starts other tasks at specified times, and delays task execution for a specified time period. The timer task requires a hardware clock to provide the time of day.

Another useful system task is the I/O task, which provides a software interface between an application task and an I/O device. It also provides arbitration for an I/O device that must be shared among several tasks. Communication between an application task and a system task is implemented through messages. An additional feature that may be added to systems with fast I/O devices is the inclusion of interrupt routines, which perform the data transfer between a buffer and a device. The routine should be supervised by a task responsible for managing the device.

Summary

The design of realtime systems with an executive program that can be written in a high level language is simple and may be written by a programmer who has little experience in operating system design. Since the system designer knows exactly where context switching takes place, system debugging is extremely simple. By providing the executive with a hardware port that identifies the specific task being run, tuning the system for compliance with realtime specifications is accomplished easily.

In selecting an executive for management of a realtime multitask environment, one should carefully evaluate whether an interrupt driven or a task driven executive will provide adequate flexibility, easy implementation, and the necessary system integration support.

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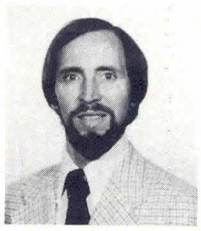

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IEEE 488 BUS TESTING PROBLEMS AND SOLUTIONS

Design, production, and maintenance problems call for an IEEE 488 bus testing device that can be programmed to exercise the full range of bus functions and solve the unique testing problems encountered at various stages of bus interface development

Stanley Kubota

Interface Technology
150 East Arrow Highway, San Dimas, CA 91773

Although IEEE Standard 488-1978 specifies the electrical, mechanical, and functional parameters for interfacing instrumentation on a common bus, it does not establish rigid specifications for the codes and formats of messages transmitted across the bus. This lack of standardization is intended to and does permit design flexibility, but it has also created compatibility problems. Each instrument designer can create a customized set of programming commands and data input/output formats that are not necessarily compatible with other designs; hence, each instrument and each controller designed for the bus implements its own subset of the standard bus functions.

Instrument manufacturers face the problem of handling unique testing requirements, as do instrument users, who must integrate the systems. Manufacturers encounter testing requirements at the design engineering stage, the production stage, the final test and calibration stage, and the service or repair stage. Applications engineers in the sales or marketing department may require further bus testing and stimulation.

Design engineers must physically connect their instrument to the bus and implement the 12 state diagrams specified in the standard. They must determine how to interrelate the state diagrams in an interface design so that the instrument function will interface properly with the bus. Although physical interface design is easier today because more integrated circuits are available to interpret state diagrams and provide the necessary bus interface, testing is more difficult. Engineers, often more concerned with the chip interconnections and bus signals than with the important message protocols, tend to take a general approach to interfacing problems. Consequently, they must bridge the gap between messages flowing across the bus and functions that these messages will cause the instrument to perform.

Testing Requirements

Because electrical states and chip characteristics are merely the mechanisms that allow communication to occur, the designer needs test tools capable of exercising a new instrument with the full set of IEEE bus transactions, which may range from discrete single-line setting or resetting through complete transmission and reception of whole messages. Required testing should enable the designer to test for anticipated functions as well as functions that the instrument is not expected to perform but that might be encountered in an end user environment.

Some designers find it necessary to test the various large scale integration chip sets they expect to use in their

designs. Among other things, testing determines which chip set is best suited to an application, and how fast a specific circuit responds to a Data Available transition or to an Interface Clear transition. Once the chips are integrated and assembled into the bus interface, further testing requirements dictate how to stimulate the overall instrument and interface design, how to emulate all of the various controllers available, and how to generate all of the combinations and character strings required to test the instrument. Test instrument programmability is likely to become a critical factor at this stage of the testing process. For example, it may become necessary to modify the sequences of characters being transmitted to the bus, or the order in which they are transmitted, or to repeat an abbreviated test sequence.

Different test problems develop when the completed design passes into production. Here, required test equipment should allow less highly skilled personnel to verify operation prior to shipping an instrument with an IEEE bus interface. This phase of testing requires a simple means of invoking a test program and a fixed procedure for verifying proper operation. In contrast to the debugging procedure used by design engineers, it involves a procedure for product validation.

Design efforts have been directed toward meeting all of these requirements to evolve a set of proven programs that verify operation of IEEE 488 bus interface designs. Using engineering test program inputs, production test personnel structured the test programs to allow a technician to invoke a specific test and, when problems occur, to modify the program by creating test loops that repeat specific operations so that signals can be traced and errors detected. The key to this capability is a test device that includes the entire set of IEEE bus functions. For example, a calculator/controller could be used during production testing; however it would be limited in that it could not perform the full range of IEEE bus functions, and those functions that it could perform would occur at a fixed speed.

Similar situations that arise during service and repair also require an easy way to verify proper bus operation. Moreover, service personnel may have to operate in a customer environment where the interface fails to work in an alien system. Good bus monitoring capability is extremely helpful in this situation. While a program is running on the system, test equipment can monitor all bus activity and also verify proper handshaking and timing protocol.

Equipment Survey

A review of available test equipment helped to identify these diverse requirements and showed that the spectrum of equipment presently used to test instruments for bus compatibility and proper bus operation ranges from simple, low cost controllers through monitor/analyzers to calculators and computers. At the low end of the capability scale, the single function test instruments allow execution of a function or a sequence but generally do not allow execution of a sequence of functions, although they may step through a multiline sequence or burst through a limited set of multiline messages. Toggle switches are used to operate these machines, which, to be effective, require a good understanding of the bus.

At the other end of the capability scale, a logic analyzer can record bus transactions for subsequent analysis. Some units encode transactions using standard IEEE mnemonics, which can be used to ascertain that transactions are occurring properly, provided the operator knows from the start what transaction sequences to expect. However, neither class of devices actually controls test sequences. They cannot send messages or commands to an instrument, retrieve the response data, make decisions based on these data, and simultaneously check the bus for proper uniline and multiline command message and data sequences. A general purpose computer or calculator achieves the control function but cannot test the interface because it cannot verify uniline message response or multiline message sequencing.

Design Integration

Each test device surveyed could handle part of the assigned task, but none could perform the complete test. Therefore, a multipurpose test instrument, the model 488, was designed so that all aspects of bus activity could be checked. Combining all of the required functions, the design admits of use as a bus monitor, a bus compatibility evaluator, a bus simulator, and even a bus controller. Composed of two primary functional subsystems, the unit includes a 6802-based input/output (I/O) processor and a 2909-based bus processor. The 6802 microprocessor, used for front panel operation and overall control, takes operator input and regulates the operator display feedback. It structures and

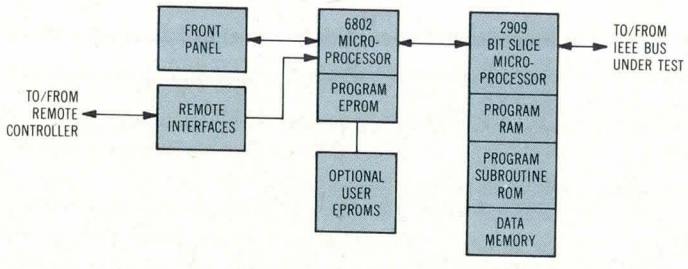

Fig 1 Functional block diagram. Blending two microprocessor technologies, design combines high speed operation, required to interact with IEEE 488 bus at various levels of detail, with complete control and status monitoring functions required for convenient operator interface

interacts with the 2909 bit slice microprocessor program, blending two microprocessor technologies to effect IEEE bus control and high speed test functions (Fig 1).

Providing the high speed execution required to test the bus, the 2909 executes most instructions at a 200-ns rate. It uses both a program memory and a data memory. Program memory, a 256 x 16-bit random access memory, stores the sequence of instructions executed to implement a desired bus function. It can be generated in any of three ways: at a stored program level, where the information is prepared in machine language form and loaded into erasable programmable read only memory; at the bus language level, where the information is programmed into the unit from the front panel using a specially developed macro level language; and at the machine language level, where programmed information is loaded from the front panel or from a remote control interface, such as the RS-232. Fig 2 depicts the software hierarchy and shows where an operator can enter instructions. Eventually, as shown, all program execution takes place at the machine language level. Data memory, which is essentially 511 x 8-bit, can contain three types of data: those to be transmitted across the bus to another device, data space to be loaded with information returned across the bus from a device, and comparison data used to test expected responses against actual responses from the device under test.

The 2909, indicated in Fig 1, contains a 256 x 16-bit subroutine read only memory that holds the fixed instruction sequences for the more common uniline and multiline commands. These are called by machine level instructions and are relatively important because they reflect an interpretation of the IEEE bus specification. The read only memory can be reprogrammed to accommodate any new protocol, format, or adaptation of the standard. This mixture of microprocessor capabilities achieves a full range of bus signal generation possibilities, as well as program execution at any level of detail necessary to test the bus, the bus functions, the instrument, or the controller. The table, Levels of Detail for Bus Interaction, describes these levels, ranging from discrete signal setting and resetting to the execution of complete test sequences.

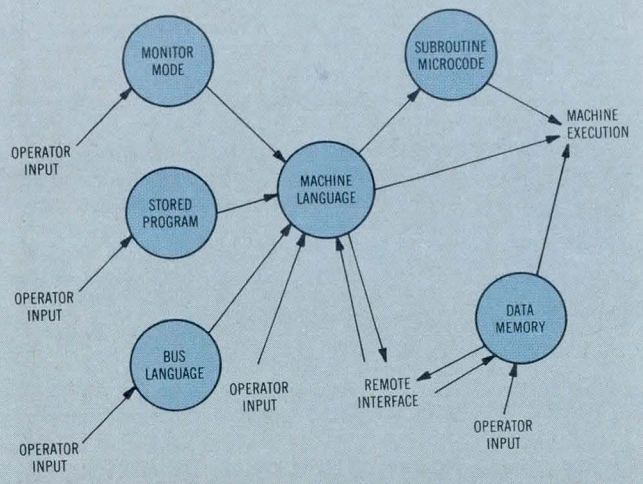

Fig 2 Software and firmware hierarchy. Programmed instructions can originate as input from front panel or remote control interface; as specially programmed, macro level statements in bus oriented language; or as stored program in machine language object code. Operator input is accepted at several stages before execution occurs at machine language level

Levels of Detail for Bus Interaction

Level 1: Discrete Bus Signal Transactions	Set or reset any bus line, test for true or false conditions of any bus line
Level 2: Command/Data or Message Transactions	2909 subroutines comprised of level 1 transactions to implement complete command transfer or data transfer, in essence a message transaction
Level 3: Control Transactions	Program sequences comprised of level 1 and level 2 transactions to implement complete control transactions such as read, write, and trigger transactions
Level 4: Program Transactions	Program sequences comprised of level 1, level 2, or level 3 transactions to implement complete programs such as measure and record voltage, set up, and calibrate instrument programs

Basic bus processor operations fetch an instruction from memory and load it into the instruction register. The instruction register content is used to generate control microcode which, in turn, directs the bit slice sequencer to define the next memory address. Apart from memory address sequencing, the microcode generates the necessary controls to carry out the instruction functions with respect to the bus control network. The bit slice sequencer provides four levels of subroutines, one of which is reserved for storage of the data memory address, leaving the remaining three levels available to the user.

The I/O processor controls all communication between the front panel switches and indicators, controller interfaces, and the bus processor. It loads the bus processor memory in accordance with user entries and then directs the bus processor to execute the program. While the bus processor is running, the I/O processor remains passive. When the bus processor either completes its program or detects an error, it generates an interrupt to request I/O processor intervention. The I/O processor can abort bus processor execution in response to a reset or stop command.

As shown in Fig 3, the I/O processor controls the bus processor by means of a programmable interface adapter. When the I/O processor takes control of the bus processor, it can then access bus processor memory and registers directly. Once the I/O processor relinquishes control and starts the bus processor, it can monitor only certain bus processor status registers until interrupted. This technique realizes fast bus operation and also supplies the control functions required for a convenient operator interface.

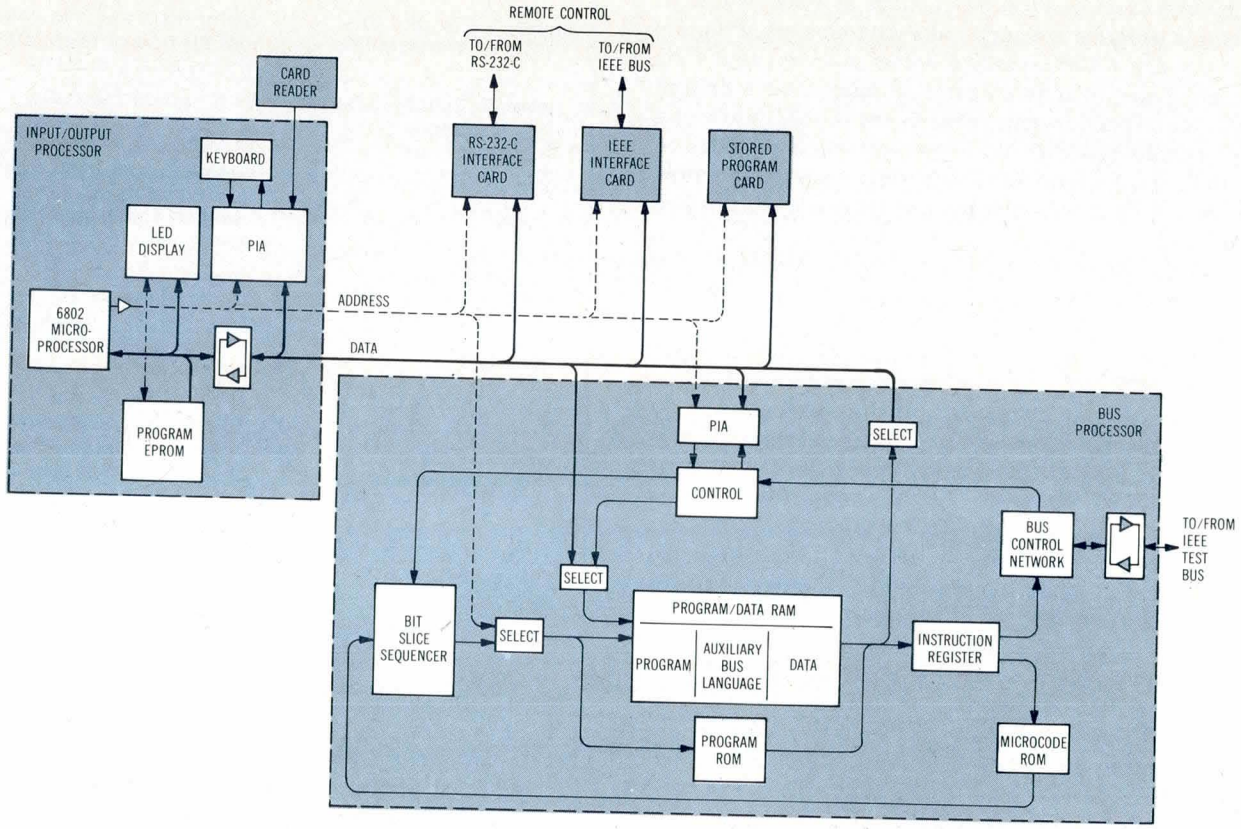

Fig 3 Subsystem block diagram. I/O processor at left handles front panel switches, indicators, and controller interface, using programmable interface adapter (PIA) to communicate with bus processor at right. While bus processor is executing instructions at 200-ns rate, I/O processor remains passive until interrupt signals that bus processor has completed operation or detected error

Summary

Testing requirements at different states in the product design cycle make widely varied demands on a test instrument. IEEE 488 bus interface testing can be especially demanding because the standard does not establish rigid specifications for message formats. The multipurpose test instrument discussed combines all functions required during product design, development, production, and field installation. It can be used as a bus monitor, a compatibility evaluator, a bus stimulator, and even a bus controller.

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As manager of sales and marketing at Interface Technology, Stanley Kubota is responsible for sales, applications engineering, and new product marketing. He specializes in IEEE bus related digital signal generators and testers, and holds a BSEE from the University of Hawaii.

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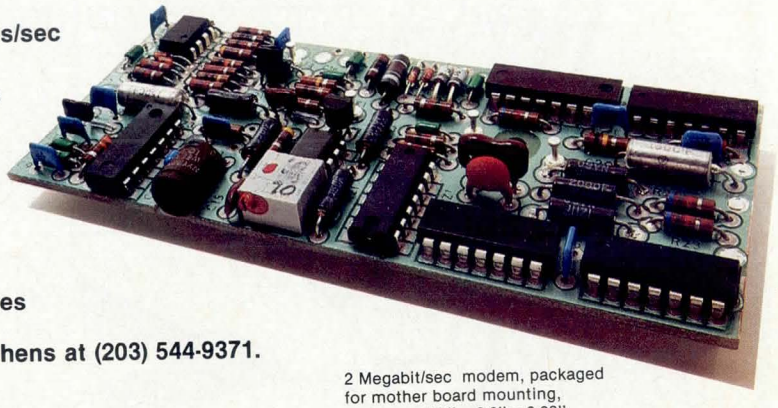

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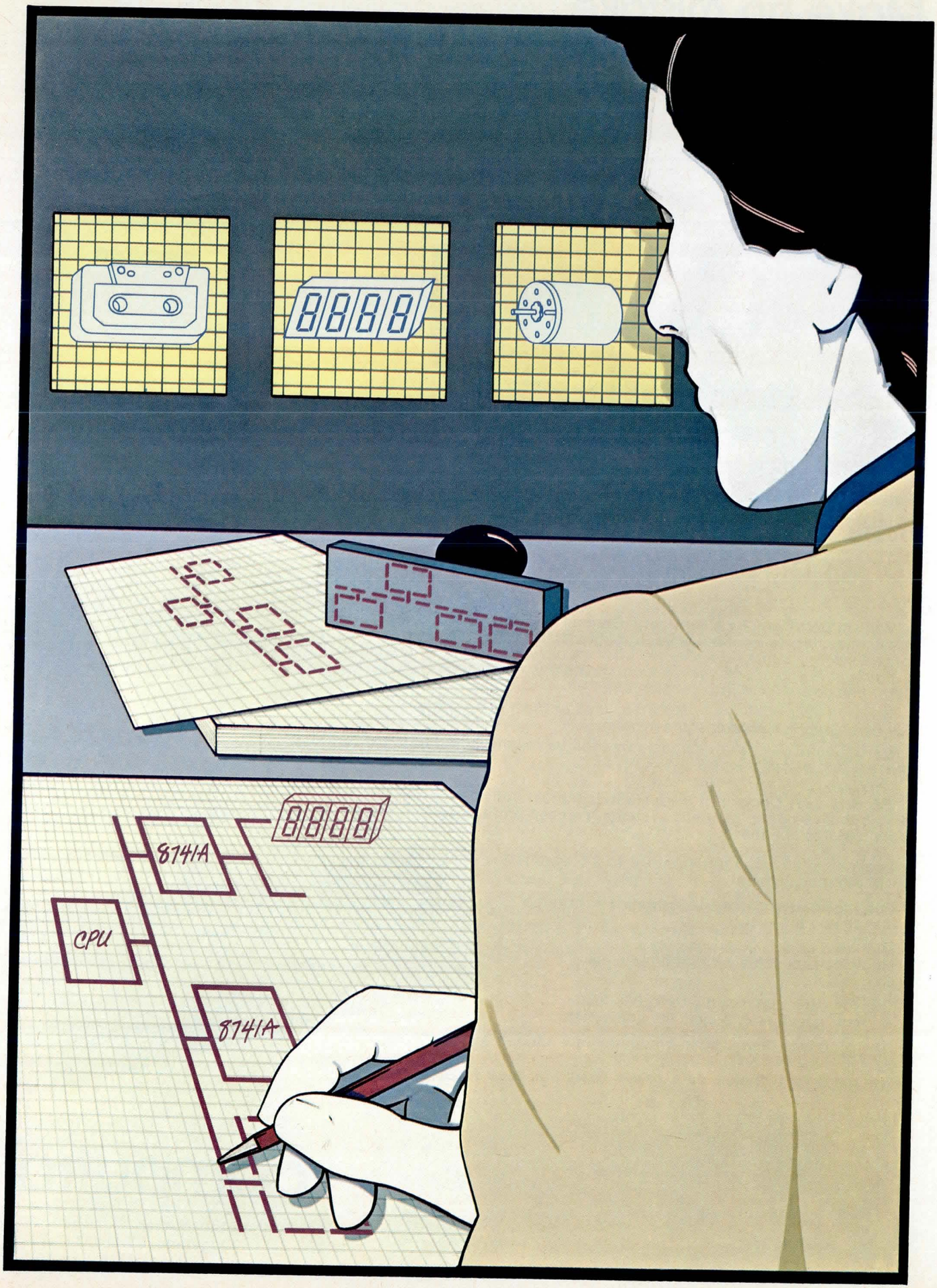
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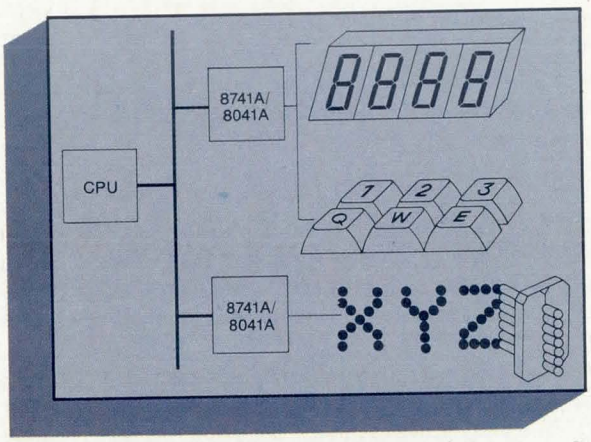

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CIRCLE 96 ON INQUIRY CARD

TECH NOTE

Selection Criteria Ease Choice Between 8- and 14-Inch Winchester Disc Drives

Analysis leading up to Winchester disc drive selection addresses cost, performance, compatibility, and size factors to identify the most effective candidate in a field marked by considerable overlap in device capabilities

Mike Kirby

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435 Oakmead Pkwy, Sunnyvale, CA 94086

To the wide range of disc drive alternatives can be added the 8-in Winchester fixed head disc drives. At first glance, these drives seem to fit into the hierarchy between 8-in floppy disc drives and 14-in Winchester drives; however, upon further consideration it appears that this is not necessarily true on a cost vs performance basis. For example, if a floppy disc system requires more storage capacity and is to be upgraded with a Winchester drive, there is no clear-cut candidate. The 8-in and 14-in Winchester products overlap in performance and cost; therefore such factors as cost per megabyte and function, size, performance, and other criteria influence the choice.

Winchester Technology

In general, Winchester disc drives are one of the most cost-effective and reliable mass storage peripherals available today. They use low mass heads that start and stop on a lubricated medium and have low load force. As the head assemblies contain fewer parts than those of prior technologies, head crashes are virtually eliminated. Simplicity of design and the absence of a load and unload mechanism offer substantial cost reduction. Winchester heads also operate a lower flying height than those of other rigid disc technologies, thereby increasing packing densities, and are enclosed in a hermetically sealed environment. Table 1 summarizes the differences between Winchester drives and older rigid disc technologies.

Eight-Inch Winchester Drives

Presently available 8-in Winchester devices fall into two categories: low cost per function and high performance. The low cost per function devices provide 5M- to 15M-byte capacities in a compact package no larger than a floppy disc unit and use a stepper motor band or capstan actuator, average access time for this technology being 60 to 70 ms. High performance products offer 20M bytes or more capacity and generally use closed loop servo actuators with 35 to 50 ms as typical access time. Where low cost is the most important goal, manufacturers have made minor tradeoffs to keep unit prices near $1200. Devices of higher performance and capacity are priced from $1500 to $2000.

Fourteen-Inch Winchester Drives

Standard 14-in Winchester disc drives, in production since 1975, fall into two general categories reflecting the same tradeoff between low cost and high

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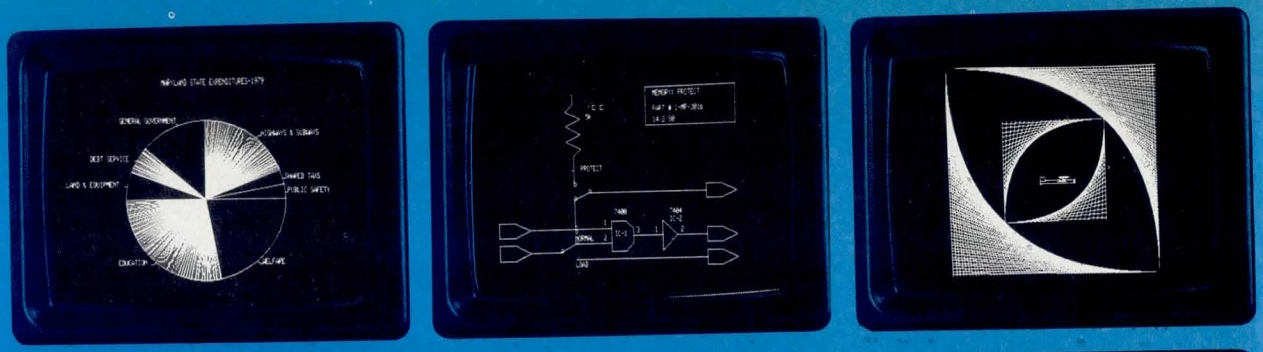

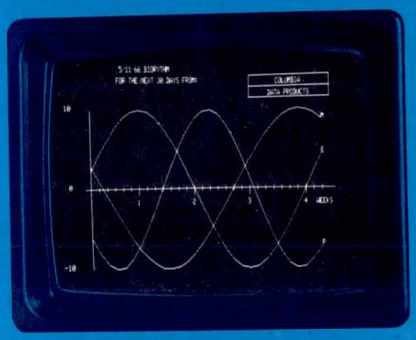

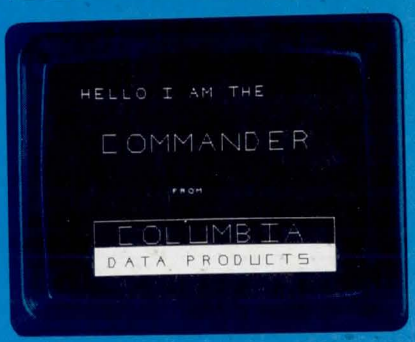

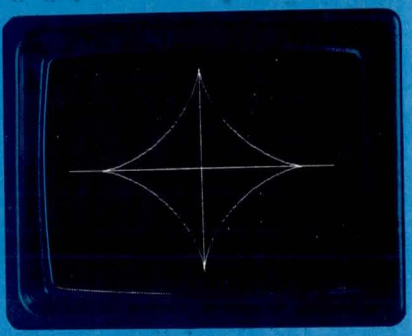

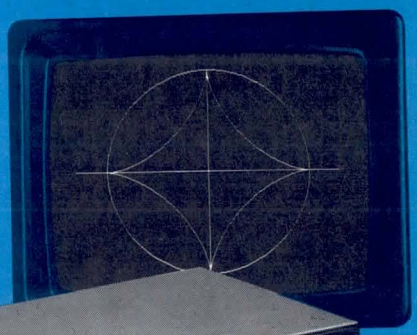

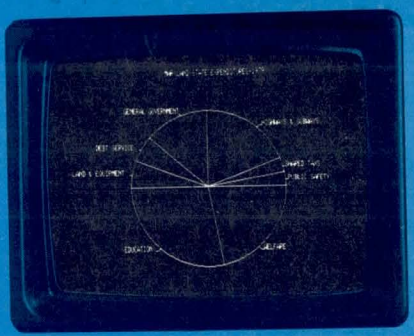

Model 900

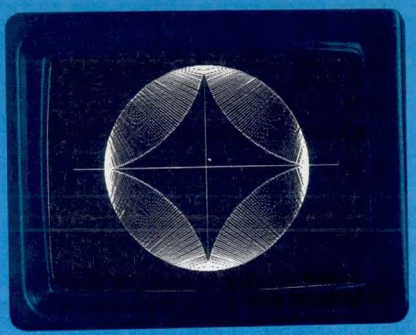

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TABLE 1

Typical Rigid Disc Drive Characteristics

Item	IBM 2314	IBM 3330	Winchester
Capacity — megabytes	1 to 100	25 to 300	12 to 300
Bits/in (bits/cm)	1k to 4k (394 to 1575)	4k to 6k (1575 to 2362)	5.6k to 6.2k (2205 to 2441)
Tracks/in (tracks/cm)	100 to 200 (39.4 to 78.7)	200 to 400 (78.7 to 157)	300 to 460 (118 to 181)
Average access time — ms	65 to 70	35 to 40	30 to 35
Heads			
Load — grams	350	350	10
Mass — grams	3.25	5	0.25
Flying height — μin (μm)	100 (2.54)	45 (1.14)	20 (0.5)
Core width — μin (μm)	7.3 to 5 (0.185 to 0.127)	5 to 2.5 (0.127 to 0.064)	2.6 to 1.8 (0.066 to 0.0461)
Media			
Oriented magnetics	No	No to Yes	Yes
Lubricated	No	No	Yes
Coating thickness — μin (μm)	100 (2.54)	50 to 35 (1.27 to 0.9)	30 (0.8)
Substrate — mils (mm)	50 (1.27)	75 (1.9)	75 (1.9)
Load/unload mechanism	Yes	Yes	Contract start/stop
Transfer rates — megabits/s	1.5 to 5	7 to 9	4 to 7
Error rates			
Soft read	10^{-10}	10^{-10}	10^{-10}
Hard read	10^{-12}	10^{-12}	10^{-12}
Seek errors	10^{-6}	10^{-6}	10^{-6}
Mean time between failure — hours	2500 to 5000	4000 to 6000	8000 to 12,000

capacity. Low cost 14-in units range in storage capacity from about 15M to 60M bytes, at a cost of from $1300 to $2500 in quantities. The higher cost units, near $4000, combine additional features with a storage capacity of from 20M to 150M bytes. Some devices originally designed for the mid or high range have spun off lower capacity models, making the low end 14-in drives the most competitive with the 8-in versions.

Selection Criteria

Selection analyses can be broken down into three basic areas of consideration: cost vs performance tradeoffs, size, and functional capability in the intended application. Across the board, 14-in Winchester drives offer a significantly lower cost per megabyte than their 8-in counterparts. Hence, when low cost per megabyte is critical, as in main storage for a clustered terminal, the 14-in products are almost always the better choice.

However, the compact size of some of the newer 8-in Winchester drives that can be exchanged for floppy disc drives is a key advantage. In systems where size is of the essence, their compactness alone may dictate a choice. If both high performance and compact size are critical, overlapping performance capabilities allow use of 14-in high performance in 8-in Winchesters that meet size constraints.

Because floppy disc compatibility was a prime reason for the evolution of low cost per function 8-in Winchester drives, it is relatively easy to interface these drives to a floppy disc system, as well as convenient to retrofit them in existing systems. This capability makes use of Winchester advantages with minimal design effort, while preparing for the next generation of equipment that will incorporate Winchester technology as an integral part of the design. Also, compatible command signals, pin assignments, track capacities, and voltage requirements allow 8-in Winchester drives and double-sided floppy disc drives to share a common controller.

In addition, Winchester disc drives are best suited to handling main system memory and fast access, high throughput mass storage requirements for online applications; however, they cannot replace floppy disc drives for data interchange and input/output (I/O). In many cases where designers are constrained by the need to achieve the lowest cost per function and must turn to very low cost memory peripherals, the opportunity to engineer cost factors out of the central processing unit and its main memory

(continued on page 166)

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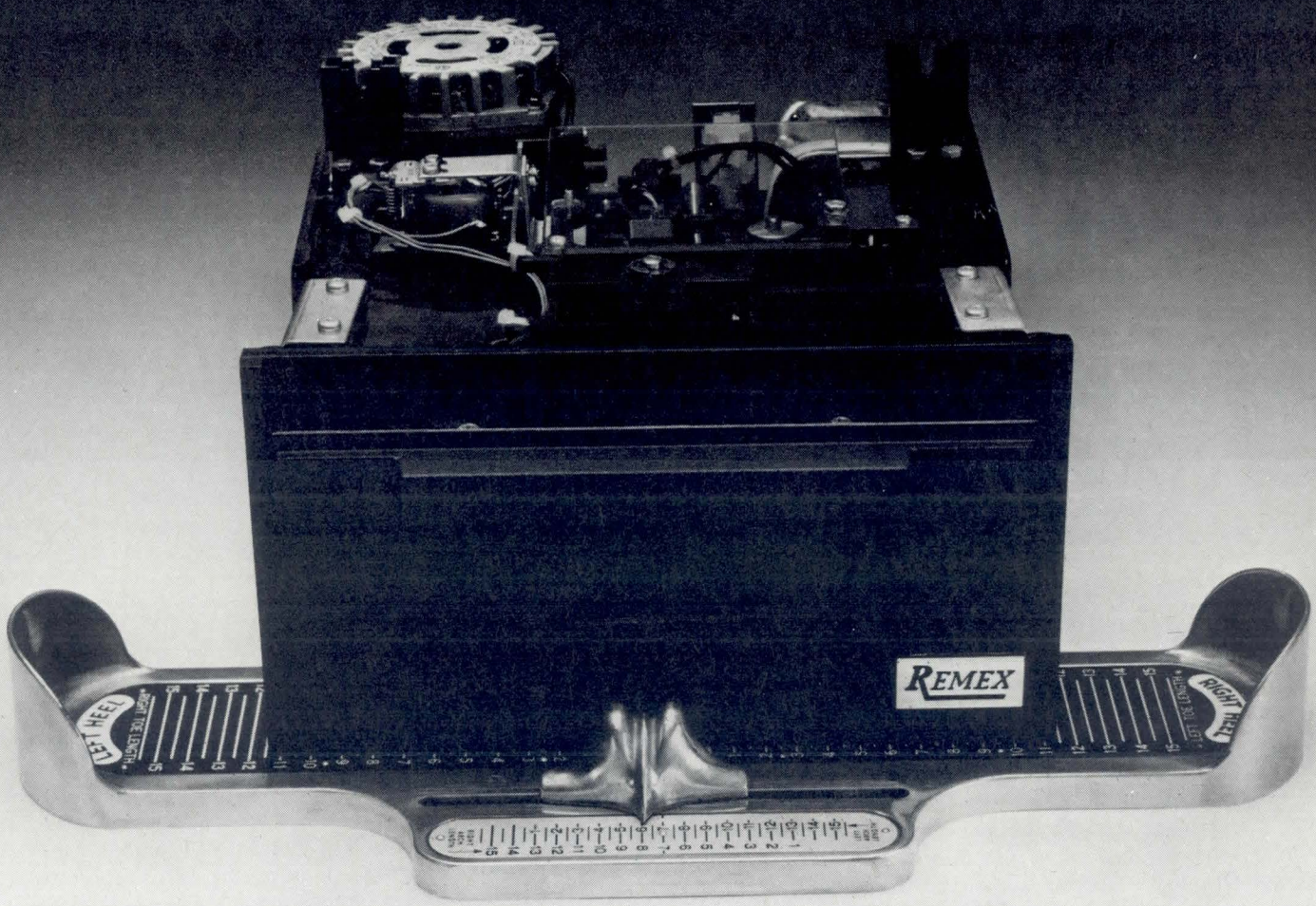

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TABLE 2

Small System Disc Drives

	8-in (20-cm) Floppy	8-in (20-cm) Winchester (low cost)	8-in (20-cm) Winchester (high performance)	14-in (36-cm) Winchester (low cost)	14-in (36-cm) Winchester (high performance)
Unformatted capacity/drive — megabytes	0.4 to 1.6	5 to 15	10 to 50	15 to 60	25 to 150
Average access time — ms	100 to 200	60 to 70	45 to 55	50 to 70	30 to 50
Average transfer time — megabits/s	0.25 to 0.5	4 to 6	5 to 8	7 to 9	8 to 10
Error rates					
Soft read	10^{-9}	10^{-10}	10^{-10}	10^{-10}	10^{-10}
Hard read	10^{-12}	10^{-12}	10^{-12}	10^{-12}	10^{-12}
Seek errors	10^{-6}	10^{-6}	10^{-6}	10^{-6}	10^{-6}
Recording density — bits/in (bits/cm)	3200 to 6400 (1260 to 2520)	5000 to 6000 (1968 to 2756)	5000 to 7000 (1968 to 2756)	5500 to 7500 (2165 to 2953)	6000 to 8000 (2362 to 3150)
Track density — bits/in (bits/cm)	48 to 96 (19 to 38)	170 to 300 (67 to 118)	300 to 450 (118 to 177)	170 to 300 (67 to 118)	350 to 600 (138 to 236)
Mean time between failure (power-on hours of typical usage)	5000 to 8000	8000 to 12,000	8000 to 12,000	8000 to 12,000	8000 to 12,000
OEM price range	$300 to $500	$1000 to $1500	$1500 to $2000	$1300 to $2500	$3000 to $5000

is almost totally lost because of the ready availability of very low cost microprocessors and semiconductor memories. Also, as software continues to increase in complexity and cost as the overall functional requirements of a system expand, designers find it more and more difficult to make a choice other than the low cost Winchester disc drive.

As the floppy disc provides the absolute lowest cost per function, teaming an 8-in Winchester disc with a floppy disc for data interchange and backup achieves the lowest cost per function for a total auxiliary memory subsystem. A total cost of about $2000 puts it well within reach. It is impossible to explore and make specific recommendations as to which type of Winchester drive should be considered for each of the myriad of applications. However, examples within each category illustrate possible recommendations based on individual system requirements.

In a word processing application, such as a shared processor system in which a central processor controls several work stations, adding the capacity of one or more 14-in Winchester disc drives makes sense at the host site. On the other hand, for individual work stations, an 8-in Winchester can provide improved performance and capacity without affecting the work station size by substituting for a floppy disc drive.

A 5M-byte, 8-in Winchester drive upgrades the systems representing the strong trend in the personal computer market toward small business applications by affording a substantial increase in storage capacity and performance. Here, again, the most cost-effective approach might team 8-in Winchesters with floppy disc units and assign to each an appropriate portion of the overall system storage requirements. The mass market for 8-in Winchester drives will probably center around those with the storage capacity of from under 10M to 20M bytes. Small desktop business systems that need performance enhancements without size increase can benefit from these drives. In networks that use minicomputers or microcomputers at remote sites, the 8-in drives are, again, natural candidates. An additional key application involves the melding of data processing systems with word processing systems. Here, the requirement for additional storage while maintaining a small desktop system is very apparent. Once again, the 8-in drive is a logical choice.

Summary

At the bottom line, system designers must compare and decide which criteria for disc drive selection are most important in a particular system. (See Table 2.) If capacity is more important than size, a 14-in Winchester drive will usually be the most cost-effective solution. If, however, the physical size of the disc is the key factor, an 8-in Winchester is probably the answer. Happily, the variety of disc drive options being made available to system designers can only continue to expand. Presently, 14-in Winchester drive development seems to center around the 75M-byte capability; 8-in drives will use the same technological advances as their 14-in counterparts. However, as 8-in Winchester disc capacity has already reached 66.7M bytes, and the range capacities and capabilities are overlapping to a larger extent, criteria for selection become increasingly important.

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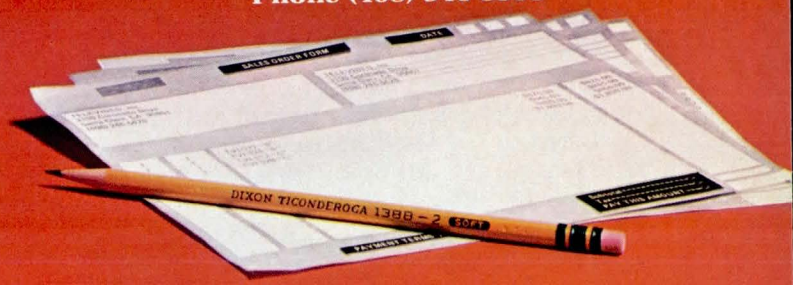

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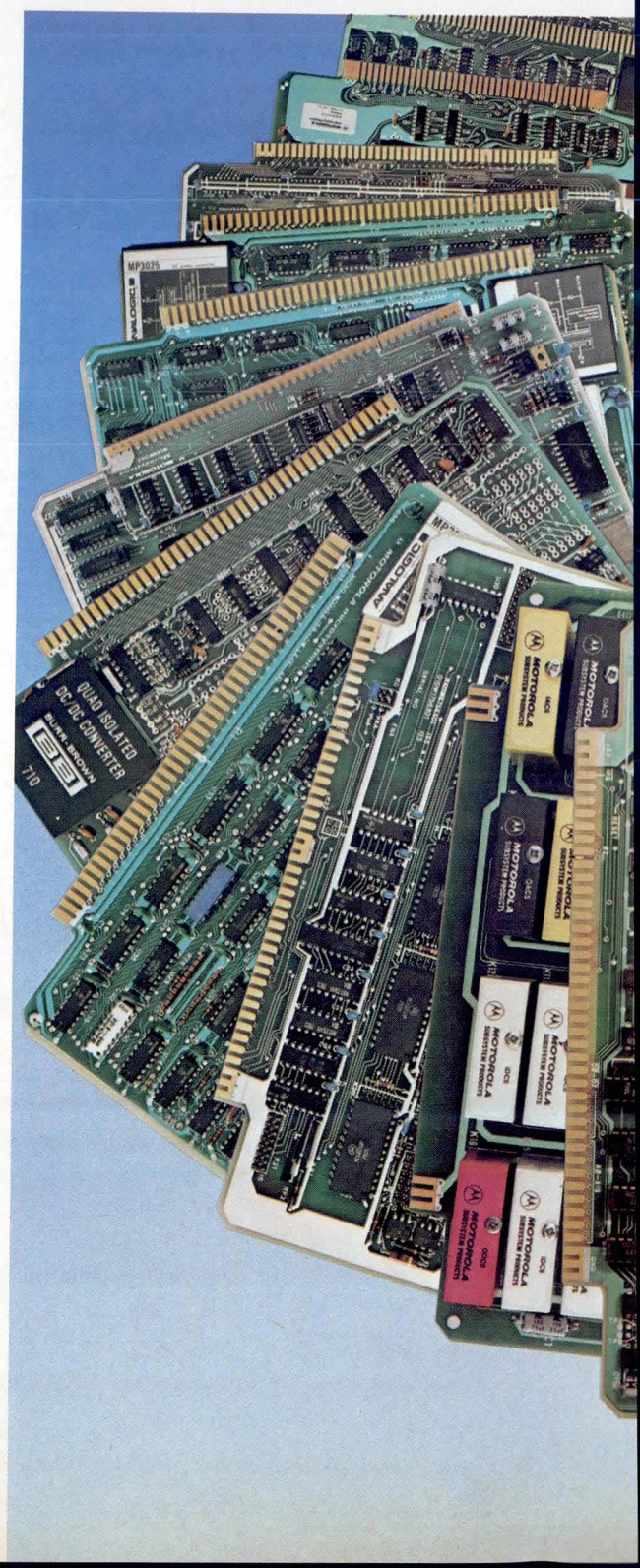

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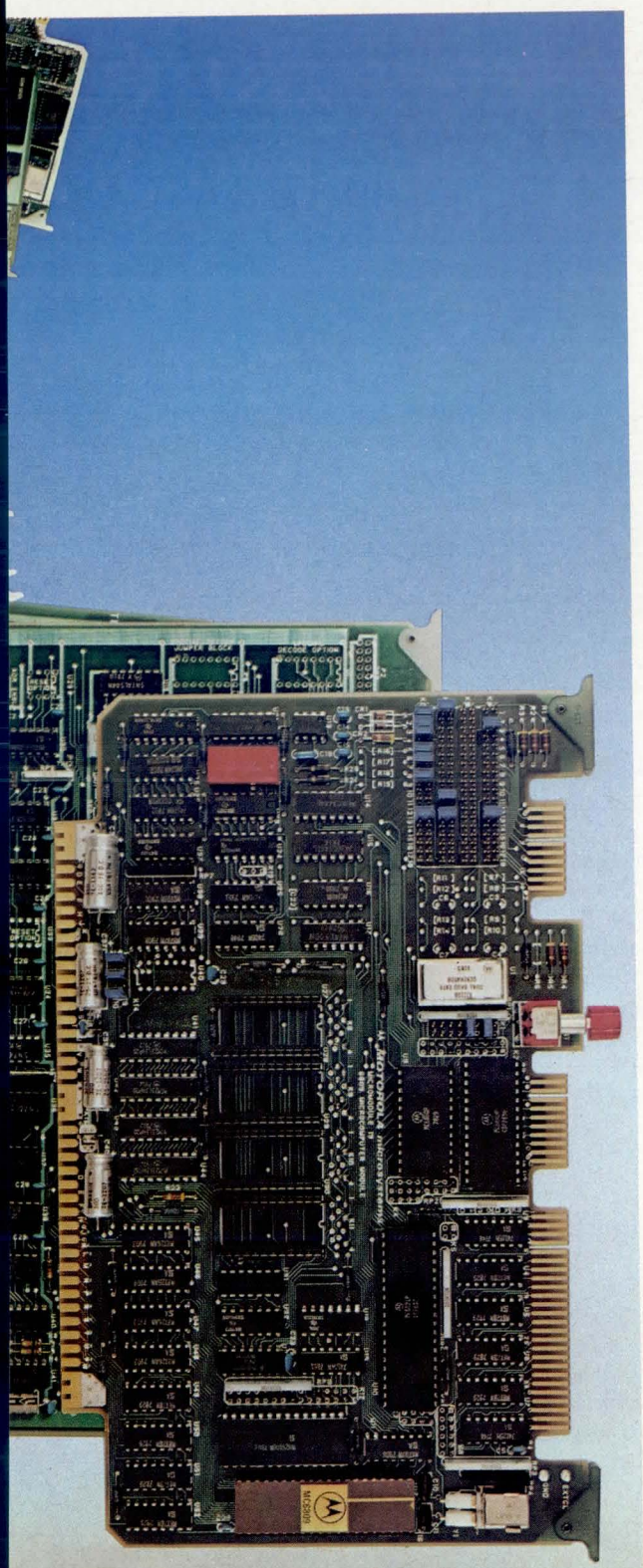

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CIRCLE 100 ON INQUIRY CARD

DESIGN NOTE

7-Track Data Recording on a 4-Track Digital Tape Cartridge

Increasing the number of tracks on a standard ANSI 0.25-in digital tape cartridge from four to seven achieves a 34M-byte storage capacity without sacrificing speed, reliability, or compatibility with 4-track drives

William Valliant

Data Electronics, Incorporated
10150 Sorrento Valley Rd, San Diego, CA 92121

Present high density tape cartridges achieve a fourfold improvement in capacity by increasing linear data density to 6400 bits/in (2520/cm), while maintaining the 4-track format used in early 1600-bits/in (630/cm) drives. Further improvements in tape storage capability require other methods of increasing capacity while maintaining the design margins of current high density tape drives. Increasing the number of tracks from four to seven and increasing the linear density to 7200 bits/in (2835/cm) achieves an unformatted data capacity of 34M bytes.

Why Seven Tracks?

Recording head design, available track width, and track positioning are among the major factors to consider when selecting the number of tracks; these and other design decisions must be balanced in order to achieve optimum results.

In view of constraints on usable tape width and practical limits on track width enforced by today's head technology, use of seven tracks to read data that were written by conventional 4-track drives reflects an optimal selection—the three additional tracks are interleaved between the original four tracks. Thus, four tracks occupy the same position as tracks on American National Standards Institute (ANSI) standard cartridges, which dictates the four track locations as well as the same read track width that conventional high density drives use. An important feature of this approach is the much larger percentage of data residing near the center of the tape, increasing data reliability.

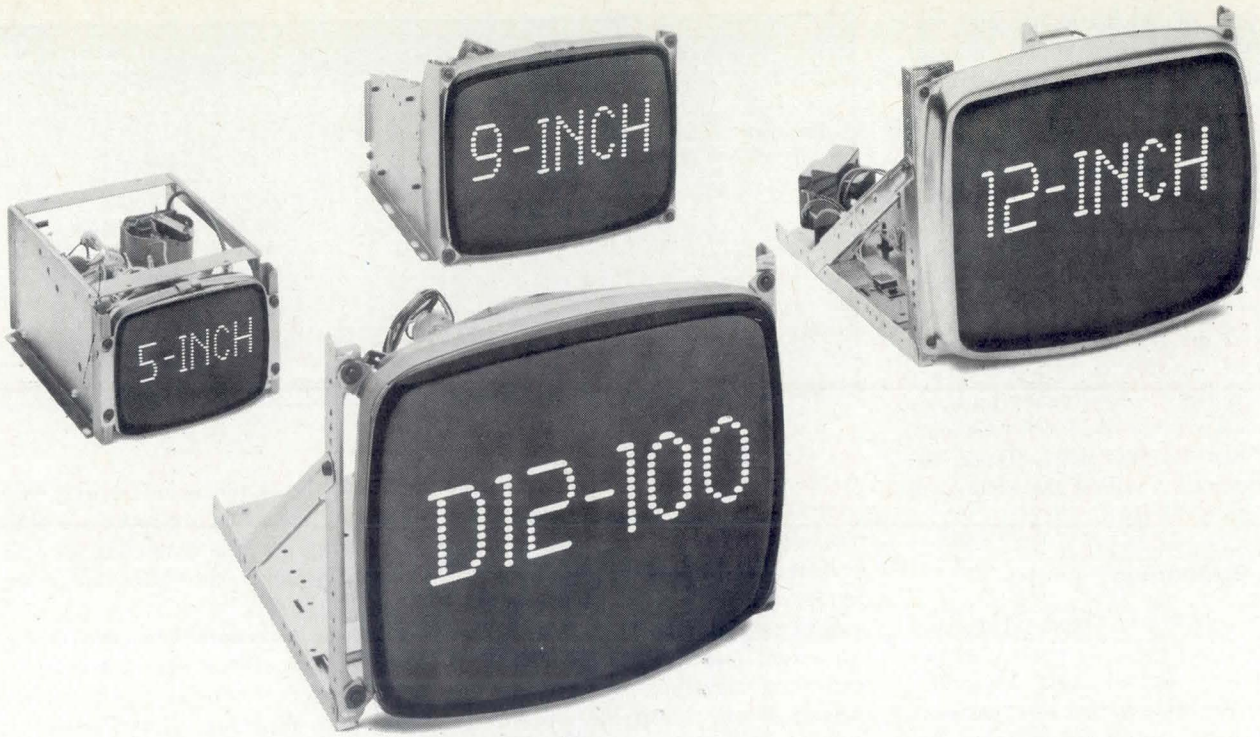
Recording Head Design

Currently available 4-track high density heads employ 10-mil (0.25-mm) read track widths. Field results with thousands of drives show that this track width achieves good data reliability. Seven-track design uses the same well-established head technology. Head contours are chosen to provide the necessary head to tape pressure at high densities, even with the low, varying tape tensions found in tape cartridges. When the head to tape pressure is too low, physical separation between head and tape results in loss of recovered signal. The table, Recovered Signal versus Separation at 6400 Bits/in, shows the effect of head and tape separation on recovered signal strength.

Practical Track Width

Track width must compensate for any indeterminancy of tape position in the cartridge. Drive tolerances also contribute to variations in the lateral position of the tape as it crosses the head. Because of the fit between the tape width and the maximum size guide posts, tape guiding assures tape position only within 4 mils (0.1 mm). Furthermore, when establishing tape edge position, the 2-mil (0.05-mm) tolerance in the lower tape guide thickness also must be included. This factor does not affect track position because the guide

(continued on page 172)



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is a part of the cartridge and tape system; it must be included, however, to determine tape wear gutter dimensions.

Dimensional tolerances in the drive can be minimized by establishing a flat reference surface and ±0.0005-in (±0.0127-mm) accuracy between the cartridge rails and the head, achieving a ±0.001-in (±0.0254-mm) tolerance between the cartridge reference surface and the position of the number one track for the write head. Taken together, the total tolerance build up requires a write head 14 mils (0.36 mm) wider than the read head. Hence, the effective track width of the write head is 24 mils (0.61 mm).

Recovered Signal versus Separation at 6400 Bits/in

Separation Distance (inches x 10^{-6})	Percent of Remaining Signal	Comments
25	60	Flying height of disc head
31	53	Size of smoke particle
50	37	Read gap thickness
150	5	Thickness of fingerprint
200	2	Thickness of oxide coating
250	1	Size of dust particle
312	0.2	Diameter of human hair = 0.1 in

Track Positioning

Physical geometry, tape wear, and head wear combine to make the outside tracks of all tape recording systems less reliable. For this reason, it is best to maximize the distance between the outside track and the edge of the tape. Interleaving three new tracks between the standard four tracks preserves the standard edge dimension while assuring the compatibility with existing 4-track cartridges that allows for upgrades to existing systems. New track locations permit normal recording in the reverse direction, which eliminates time-consuming rewind operations and preserves the desirable read-while-writing check feature. Reading or writing alternate tracks, first forward and then reverse, reduces the track to track switching time to less than 1 s. Fig 1 shows the resulting serpentine format, achieving low cost drive design by using a single data channel with a head switch to multiplex the various tracks.

Track 1 occupies the same location as on conventional 4-track drives. Data are recorded on track 1 in the normal forward direction. Inner tracks are filled first for maximum reliability on partially filled tapes using only the first few tracks. New track 2 resides

(continued on page 174)

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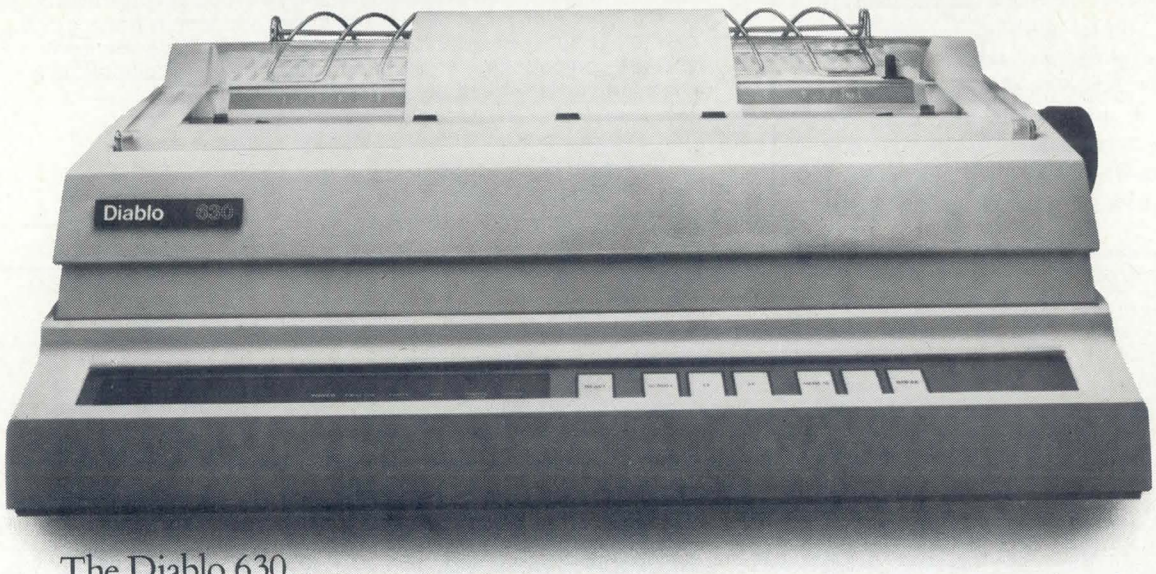

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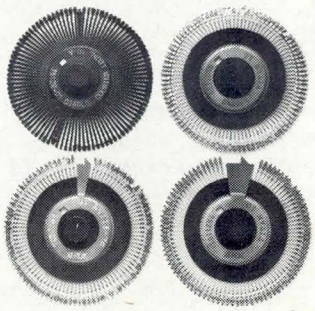

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CIRCLE 102 ON INQUIRY CARD

between conventional track 1 and conventional track 2, but is recorded in the reverse direction. New track 3 has the same position and recording direction as the original track 2. New tracks 4 and 5 extend this convention, but track 6 requires a different procedure. ANSI standard data cartridges have early warning holes and load point holes punched directly in the path of the new sixth track (Fig 2). Since the drive senses these holes optically, they must be dealt with in a special way.

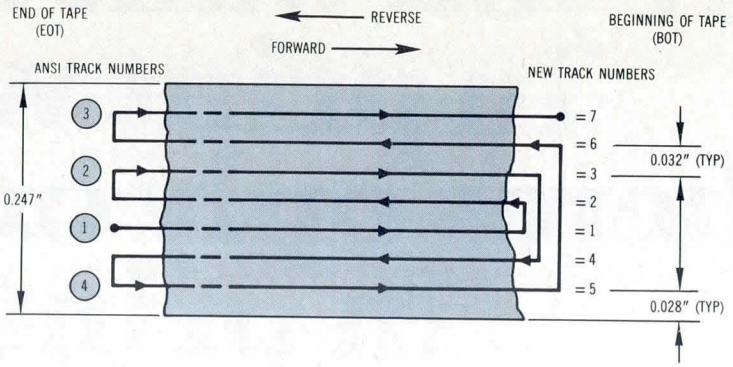

Fig 1 Track position and direction. Arrows indicate tape motion past record/reproduce head: head is stationary and tape is moving. Placing new tracks between old tracks preserves standard edge dimension and assures compatibility. Track numbering scheme positions data near center of partially filled tape

Dealing With Holes

On any track, the block being recorded is finished when either the early warning hole or the load point hole is sensed; then, adding a magnetic marker at the end of the block further identifies the logical end of record. Recording does not resume until the hole has been passed in the opposite direction. On the sixth track, where the hole occupies a position in the center of the data area, it is treated simply as a magnetic anomaly, and reflects a maximum potential loss of 160 data bits. Implementing both the turnaround algorithm and its error correction capability, the controller handles this 160-bit maximum data loss as it would handle any other dropout.

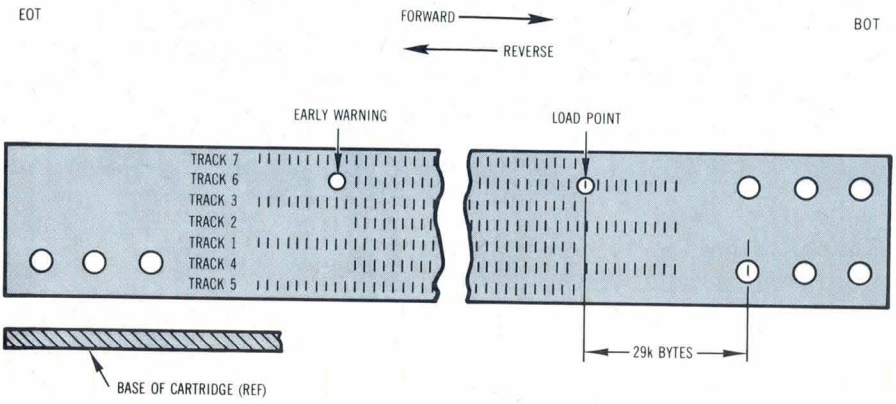

Fig 2 EOT, BOT, early warning, and load point holes. Optically sensed load point hole falls directly in path of data track 6. By treating hole as 160-bit magnetic anomaly, error correction circuitry in controller handles problem as for any routine dropout

Summary

Applying 7-track technology to conventional 4-track digital tape cartridges increases capacity to more than 34M bytes without sacrificing reliability. Seven-track design is capable of reading the 0.25-in (0.64-cm) ANSI standard cartridges recorded on earlier, 4-track equipment. Selection of both the number of tracks and their location on the tape reflects careful consideration of several factors that could influence reliability. A fail-safe turnaround algorithm allows bidirectional access, without rewind, and error correction circuitry in the controller deals with the special problem of early warning and load point holes.

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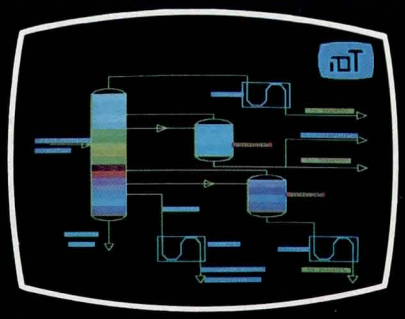

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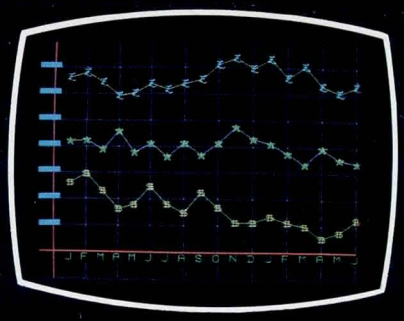

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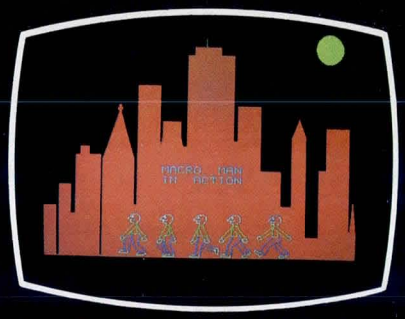

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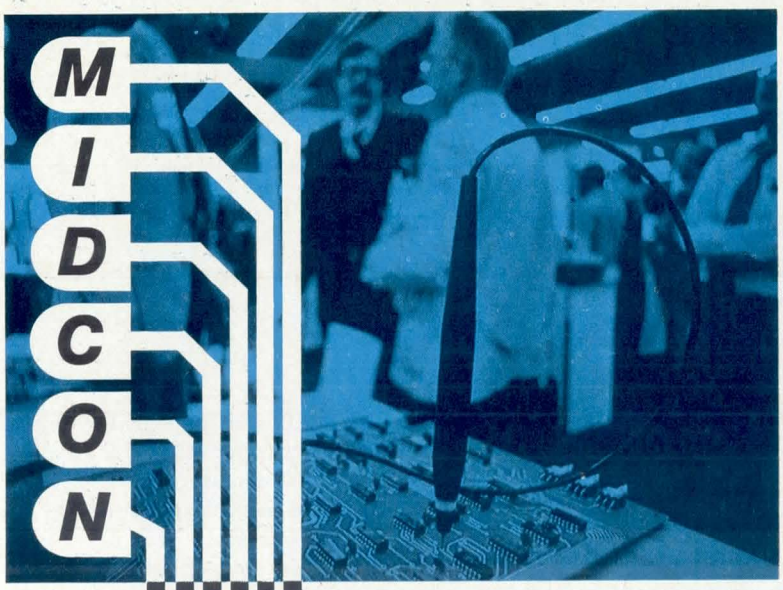

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TECH BRIEF

Video Compression Scheme

Diagonal picture elements are transmitted serially, stored, and then reconstructed at the receiver

The channel bandwidth requirements for transmitting video pictures are reduced by a scheme that divides the picture into blocks containing a checkerboard pattern of picture elements. Elements are sampled along diagonal rows, converted to digital signals, and transmitted serially to the receiving station where they are stored in a video frame memory. Memory contents are continuously updated as new picture elements are received. Standard bandwidth of 8.064 MHz for transmitting a 525-row x 512-column picture is reduced by factors of 4, 8, 16, or higher by the scheme.

The picture to be transmitted is imagined to be partitioned into blocks, each containing n x n picture elements. Thus, 512/n blocks span the horizontal width of the picture. Elements are transmitted by the circuit shown in Fig 1. A crystal oscillator in the transmitter is the origin of all synchronizing and sampling signals. Its output is divided to 15.75 kHz to develop horizontal and vertical synchronizing pulses and to 8.064 MHz to furnish the fundamental video sampling signal. This 8.064-MHz signal clocks an n-bit recirculating shift register (in the clock generator) to produce n clock phases, all at 1/n of the fundamental frequency and all equally shifted in phase from each other (n is typically 4, 8, or 16).

During each line scan, the combination of horizontal line counter, binary to one of n decoder, and clock selector routes one of the n clock phases to the storage command input of the analog to digital converter (ADC). For a typical scan, the nth picture element of each block on the line is transmitted. On the following line scan, the next clock phase is selected, and the (n + 1)th picture element in each block is transmitted. In this way, all picture elements along corresponding diagonals in the blocks are transmitted.

Fig 2 shows one 8 x 8 picture element block, with the shaded squares in color indicating those that are sampled during a typical scan of all 8 lines. Since the 525 lines of the video frame are not an even multiple of 8, the diagonals will be displaced in each successive frame until every picture element is covered once.

(continued on page 181)

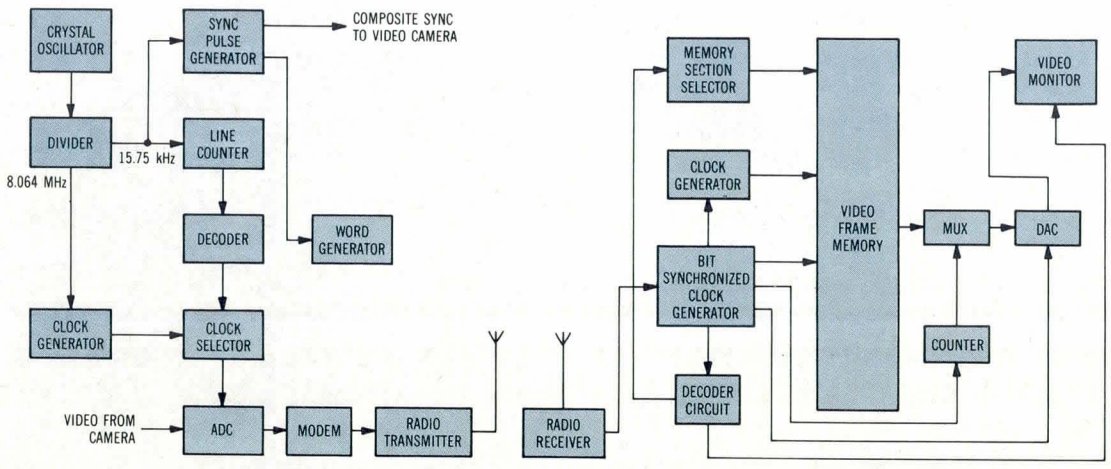

Fig 1 Video compression circuit. Circuit divides picture into elements that are transmitted at reduced data rate. By sampling elements along diagonals in n x n picture element blocks, system gives picture quality comparable to that of standard television and superior to most pseudorandom sampling schemes

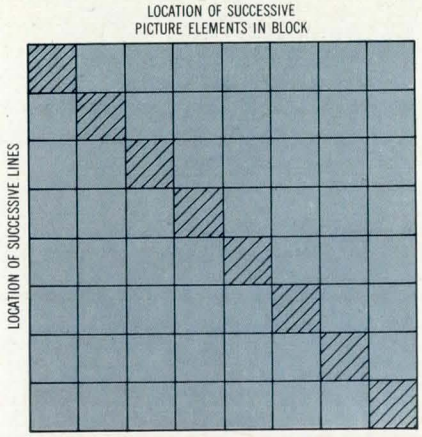

Fig 2 Typical picture element block. Shown after one frame scan, shaded elements represent those that have been transmitted. Corresponding diagonals in other blocks have also been transmitted

Picture elements are transmitted to the receiving station where they are placed in the video frame memory. In the receiver, a bit synchronized clock generator develops the 15.75-kHz synchronizing signal at the video line frequency and the 8.064-MHz video information rate signal. The decoder circuit and memory section selector route each incoming image element into a section of the video frame memory. The memory has as many sections as the largest useful number of blocks (for example, 16). If n is chosen to be equal to this maximum number, each block goes into one section; if n is less than the maximum, the picture elements of each block are distributed in more than one section. At the memory output, multiplexing circuitry selects consecutive sections of memory and transmits the picture elements in the proper temporal sequence to a digital to analog converter (DAC). The DAC feeds the analog video to the monitor and reconstructs the picture.

Note

This work was done by Henry Lum, Jr, and Yutaka Matsumoto of Ames Research Center.

INTERFACING FUNDAMENTALS: TIME LINES

Peter R. Rony Virginia Polytechnic Institute and State University
Blacksburg, VA 24061

Time lines, which depict the intervals required by individual steps or tasks in a sequential process, can be used to demonstrate how source and acceptor perform their data processing tasks in a conditional input/output system. Fig 1 provides a general flowchart for conditional input/output using a semaphore. For the specific situation in which acceptor processing time is much greater than source processing time, there is a corresponding set of time lines as shown in Fig 2.

From these illustrations it can be seen that the source outputs data to the acceptor, sets the semaphore, and then repeatedly tests the semaphore for the reset condition.[1,2] The acceptor repeatedly tests the semaphore for the set condition; when such a condition is met, the acceptor inputs the data, resets the semaphore, and proceeds to the processing of the input data.

After the source detects the reset condition of the semaphore, it proceeds to its own processing tasks, which can be as simple as retrieving new data from memory and incrementing the memory pointer.[2] Dotted arrows in Figs 1 and 2 represent the communication of the one bit of semaphore information between source and acceptor.

A time line representation can be a valuable pedagogical tool in answering questions associated with the choice of input/output (I/O) technique. Typical questions such as the following must be answered. Is a flag or semaphore needed? If a flag is needed, should the source or acceptor test the flag output? Does the source or acceptor spend too much time in a test loop? Can the use of interrupts improve performance by releasing the source or acceptor to perform other tasks?

For example, in Fig 2, the source sets the semaphore considerably before—not during—the acceptor test loop. Consequently, only a single pass is made through the acceptor test loop, and it can be eliminated. Removal of this loop converts the semaphore into a flag that is tested by the

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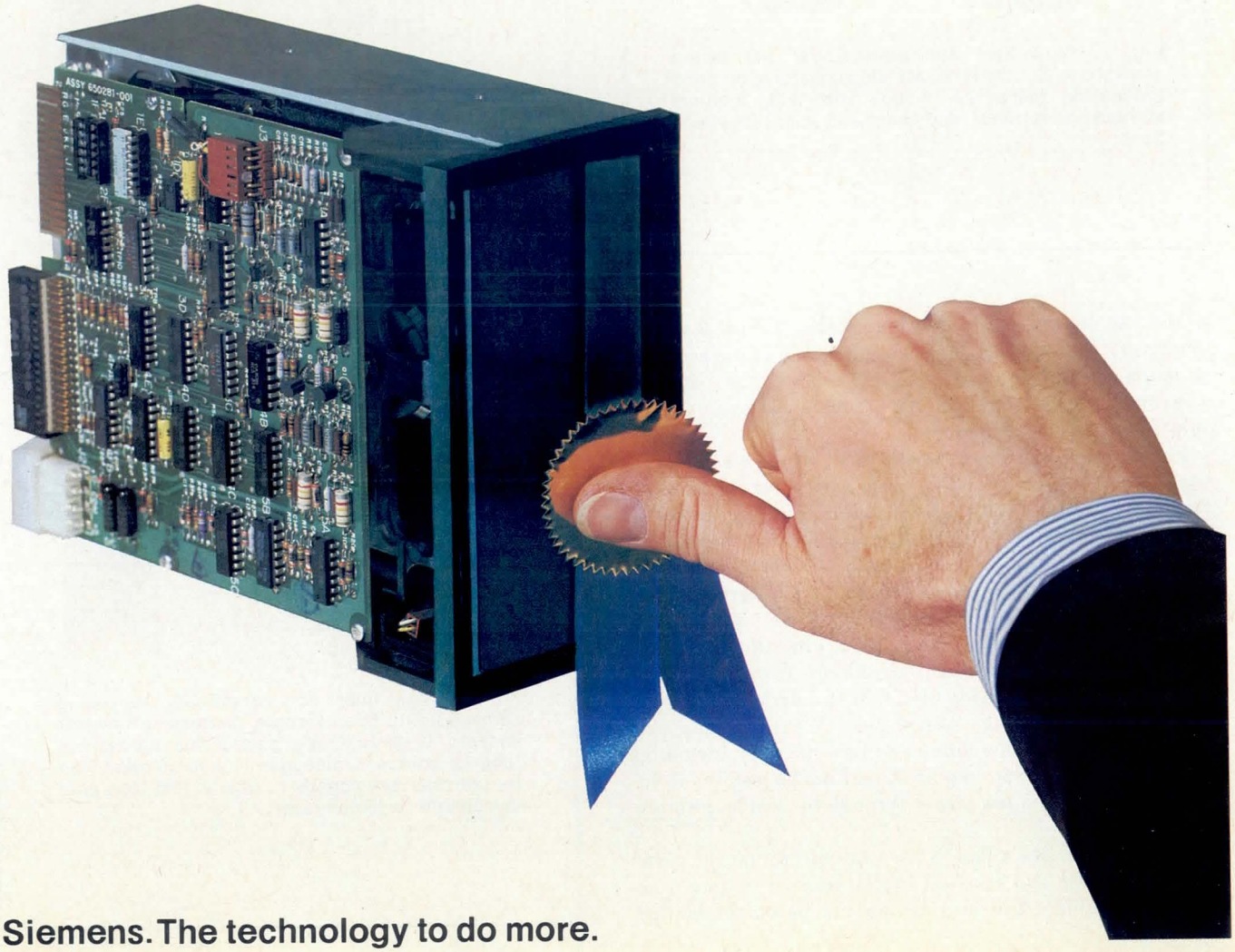

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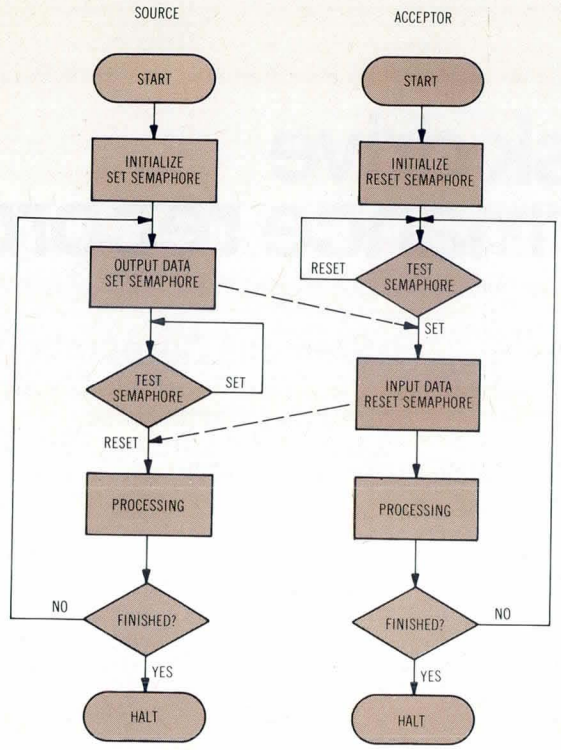

Fig 1 Flowchart for conditional I/O using semaphore. Source is on left and acceptor is on right. Processing tasks can include arithmetic, memory storage and retrieval, and command word test operations

source, as shown in Fig 3. Comparison of Figs 2 and 3 demonstrates that when the processing time of the acceptor is much greater than that of the source, the acceptor semaphore test loop can be eliminated and a flag substituted for the semaphore.

Furthermore, the source wastes time testing for the reset condition of the flag. (See Fig 3.) An alternative choice of I/O technique would employ an interrupt. By using an interrupt, the source test loop would be eliminated, the source would be diverted to processing tasks associated with other acceptors, and the flag would generate the interrupt signal whenever the acceptor required service. For 8080A based microcomputers operating at 2 MHz, interrupt overhead, the time associated with stack operations that do not contribute to a data processing task, falls within the range of 25 to 50 μs, whereas a single pass through a test flag loop consumes about 14 μs. Therefore, use of an interrupt, including the additional hardware required, may not be justified if the source makes only a few passes through the test loop shown in Fig 1.

A semaphore, like a flag, is used to synchronize the asynchronous source and acceptor for the transfer of data from one to the other. Use of a semaphore becomes justified when processing times of source and acceptor are comparable, or are both comparable and variable, as shown in Fig 4. It can be seen from Figs 1 and 4 that the basic software principle behind the synchronization process is the test semaphore loop.

For example, time lines in Fig 4 depict source and acceptor initially to be performing their respective processing tasks. Then the source outputs data, sets the semaphore, and proceeds to test the semaphore for the reset condition. At about the same time, the acceptor tests the semaphore for the set condition, detects the condition, inputs data, resets the semaphore, and proceeds to process the input data. The subsequent acceptor processing time is shown to be short, so the acceptor spends considerable time in its test loop awaiting the source to output new data and set the semaphore once again. The acceptor test loop can be viewed as the means whereby the acceptor resynchronizes itself to the source and, in a similar fashion, the source test loop can be viewed as the means whereby the source resynchronizes itself to the acceptor.

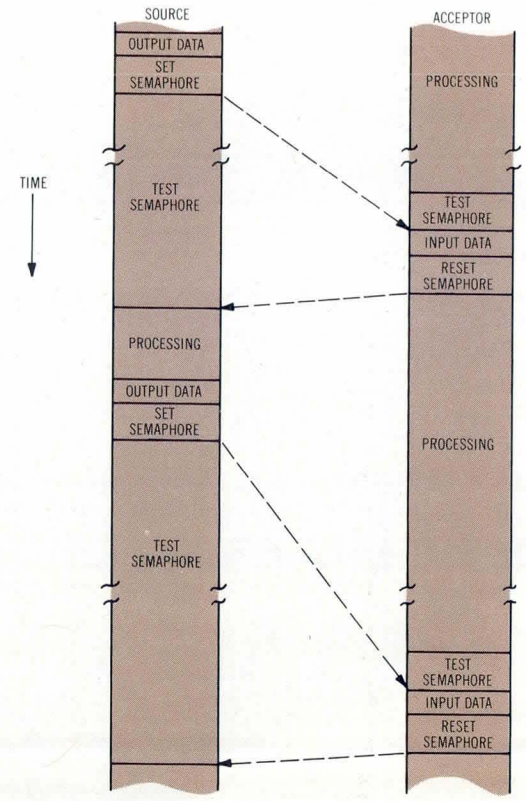

Fig 2 Time lines for conditional I/O using semaphore. In this example, processing time for acceptor is considerably greater than processing time for source. Consequently, source must wait for considerable periods of time in test loop until semaphore becomes reset

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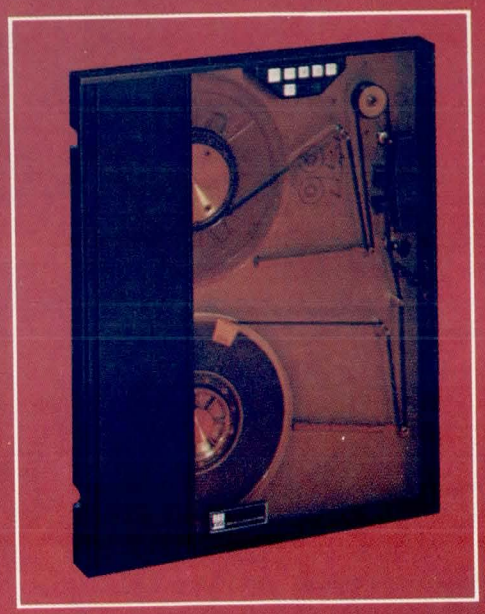

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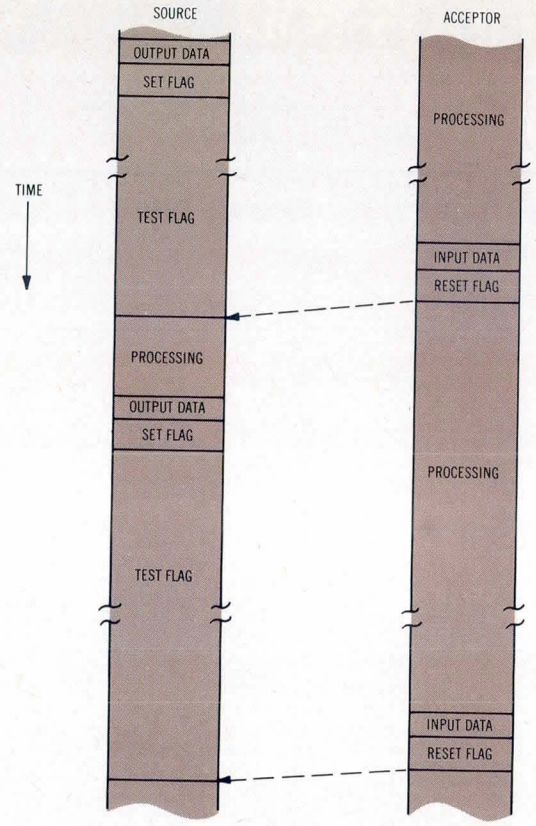

Fig 3 Time lines for conditional I/O using flag. This is essentially same diagram as Fig 2, with test semaphore task removed from acceptor time line. Elimination of test semaphore loop (software) and semaphore connection (hardware) to acceptor converts semaphore to flag

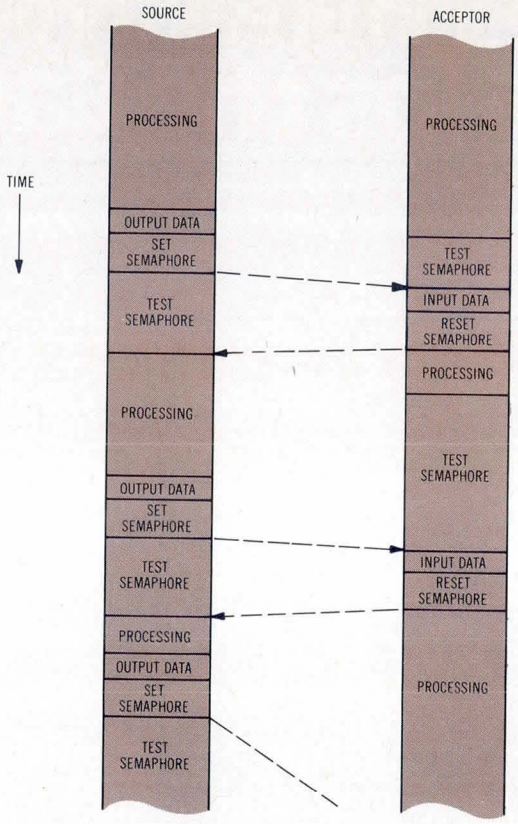

Fig 4 Specific case of time lines for conditional I/O using semaphore. Source and acceptor processing times are comparable and variable; either can be greater than other. Situation is excellent candidate for use of hardware semaphore

Use of semaphores currently appears to be more common in software than in hardware. In fact, semaphore as a term itself is rarely mentioned in hardware textbooks or specification sheets. An excellent example of the use of a pair of semaphores is the Mode 2, 8080- to 8080-interface circuit described in the *Intel Peripheral Design Handbook*[3]. The OBF and IBF semaphores associated with the 8255 programmable peripheral interface chip synchronize bidirectional transfer of data between the two microcomputers. This example will be discussed in greater detail in future columns.

The trend in hardware continues to move toward distribution of processing tasks—to peripheral chips such as I/O, math, fast Fourier transform (FFT), and firmware data processors, and stepper motor controllers. Given the increase in sophistication of microprocessors, it appears that hardware semaphore use will become more prevalent.

References

1. P. R. Rony, "Interfacing Fundamentals: Conditional I/O Using a Semaphore," *Computer Design,* Apr 1980, pp 166-167
2. P. R. Rony, "Interfacing Fundamentals: Conditional I/O Using Two Microcomputers," *Computer Design,* Aug 1980, pp 136-138
3. *Intel Peripheral Design Handbook,* Intel Corp, Santa Clara, Calif, 1979, pp 2-135

Note: The following statement was omitted from the Aug 1980 article (*Computer Design,* pp 136-138): "The author respectfully acknowledges contributions to this article from Neil J. Bungard."

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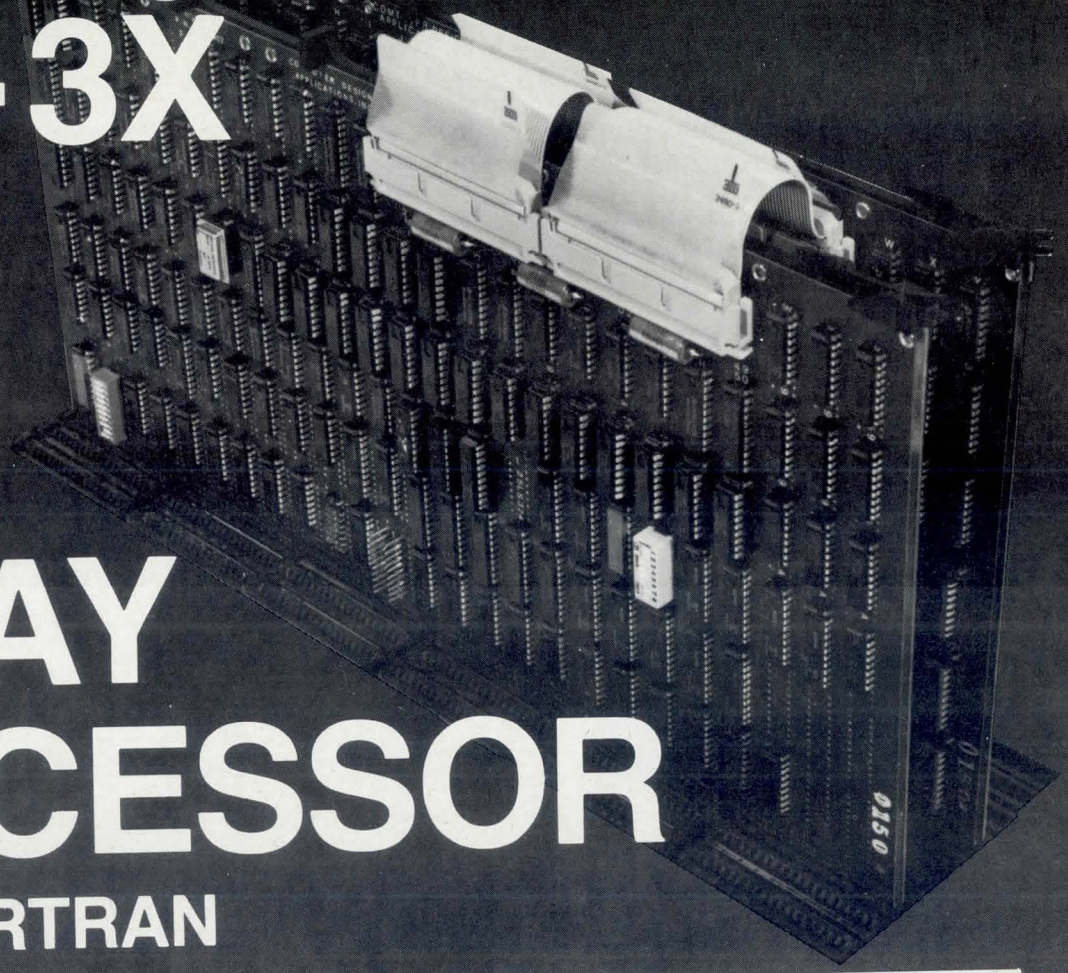

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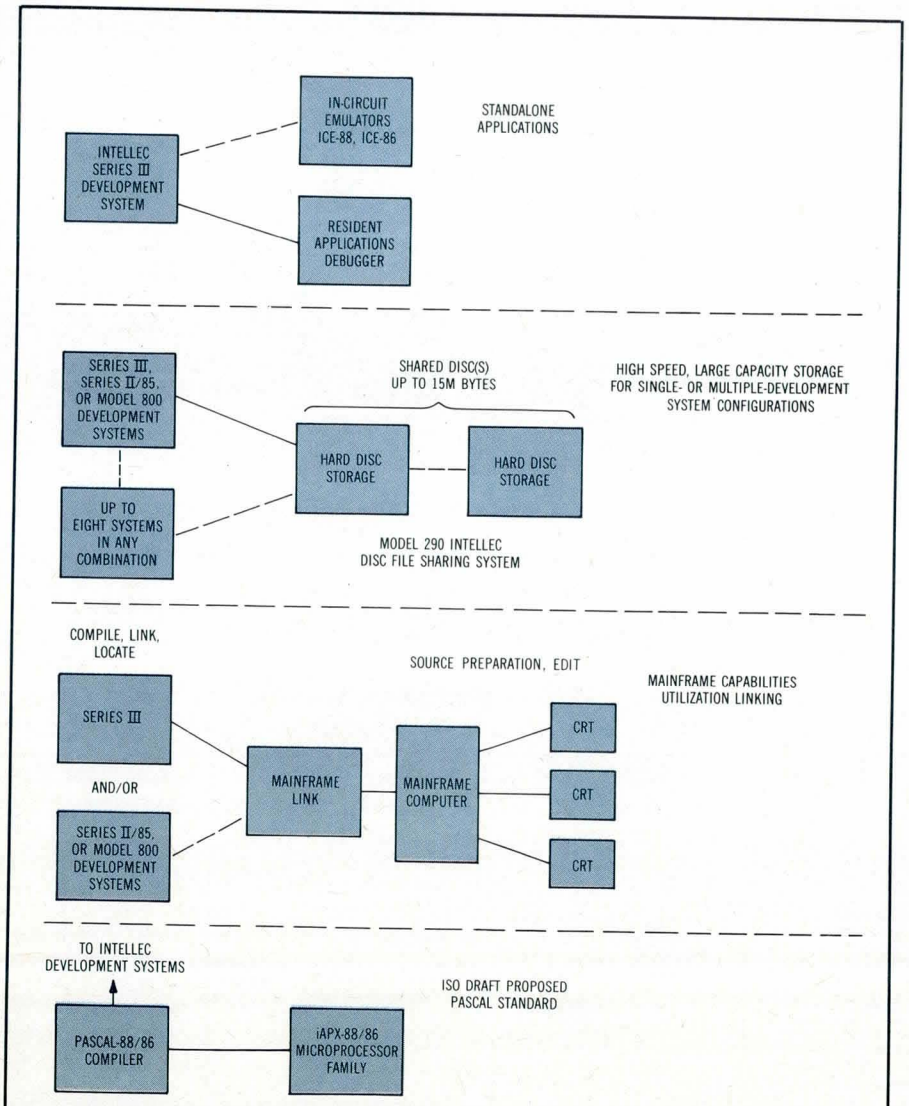
CIRCLE 107 ON INQUIRY CARD

Development System Functions Alone or In Distributed Software Development Network

A flexible, comprehensive approach to system software development can be undertaken through use of an Intellec[R] Series III microcomputer development system. Tailored for the iAPX-88/86 (8088 and 8086) 8- and 16-bit family of microcomputers, the system supports high level languages and multiuser, multiple microprocessor distributed development configurations and includes two host CPUs and 1M-byte address capability. The system, from Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, consists of a CRT monitor with detached keyboard and integral floppy disc drive that can function alone or in conjunction with other development tools. Available to operate with the Series III are a high speed disc file sharing system, mainframe link, and Pascal-86 compiler.



Intellec[R] Series III development system. System operates alone or linked with shared disc storage system or mainframe. Linking permits utilization of capabilities of high speed storage and multiple operator approach for distributed development system network

Two CPUs (8085 and 8086) provide a dual execution environment enabling running of 8-bit applications and translators resident in the 8085 execution environment, and 16-bit applications and translators resident in the iAPX-86 execution environment. The full 16-bit environment ensures faster translation speed for the iAPX-88/86 applications. While developing 16-bit applications programs, the 8085 functions as an intelligent input/output (I/O) controller. Up to 1M byte of system memory increases symbol table and user program space potential and allows high level language compilers to run faster than those with smaller memories (64k).

PL/M, FORTRAN, Pascal, and an iAPX-88/86 resident assembler operate with the system, and codes generated by each compiler can be linked together by the system. Included with PL/M-88/86 is a high speed syntax checking option that increases efficiency of source code debugging.

For iAPX-88/86 systems with multiprocessor design projects, in-circuit emulators and a resident applications debugger permit debugging of software controlling interaction between processors and the system bus, as well as individual software for each processor. The emulators include software oriented debug features such as English-like commands and conditional and macro commands. Breakpoints, single-step functions, register, memory, and I/O references, symbolic debug, disassembly, compound commands, and code execution functions are available through use of the applications debugger.

Older development system models such as the model 800 and 8085 based Series II can be upgraded to System III capability with a model 556 upgrade package.

Disc File Sharing System

Up to eight development systems can share files on one or two hard disc drives providing storage of up to 15M bytes. A multiuser distributed program development system utilizing Series III, II/85, or model 800 systems is

(continued on page 190)

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configured by interconnect boards and cables linking individual development work stations to form a model 290 Intellec® disc file sharing system (DFSS). Both private and public files can be generated at each work station. The work stations can be located up to 20 ft (6.1 m) apart.

Mainframe Link

Purpose of the mainframe link is to combine capabilities of a large mainframe system and one or more development systems and apply them to large microcomputer development projects. Multiple CRT terminals and use of hard disc storage permit a number of write and edit source program files to be produced simultaneously.

When the source programs are complete, they can be downloaded through the link to a development system. There, the programs can be compiled into object modules, linked together, and located. The linked binary file can be transmitted to the mainframe for storage for later use with in-circuit emulator modules for system debugging.

Pascal-88/86 Compiler

Complementing the iAPX-88/86 family and Series III development systems is the Pascal-88/86 compiler. Relocatable object code is produced directly from the English-like source code and can be linked with other Pascal-88/86, PL/M-88/86, or ASM86 object files. The compiler conforms to and implements the ISO draft proposed Pascal standard with extensions.

To permit portability of Pascal programs, the number of extensions is restricted to those that are required for most microcomputer applications, and all extensions are separable from standard features. A compile time option can have the compiler flag the end use of an extension, thus, in one compilation, parts of the program that are not portable are identified.

In addition to the compiler module linking extension, direct port I/O in Pascal and compilation of a procedure for execution at an interrupt are the major extensions. Compiler options are provided that direct the software to produce either extra code and information to assist debugging process, or to produce minimal object code to prepare a debugged system for production.

Runtime support system is structured to simplify execution of Pascal-86/88 programs outside the development system. Compiled programs can be run on any 8086/8087/8088/8089 system provided that the operating system entry points required by the runtime system are linked in. These entries are part of the Series III operating system and the RMX-86 realtime executive.

Circle 465 on Inquiry Card

Development System Gains Effectiveness by Use of Target Hardware

Use of the DS22 microcomputer development system with its CRT, printer, and mass storage provides advantages in the software development, hardware debug, and system integration to be performed on a hardware system. Produced by Micro/sys, Inc, 1353 Foothill Blvd, La Canada, CA 91011, the system is said to be exceptionally cost-effective.

Based on the STD BUS interconnect system, the tabletop system contains Z80 or 8085 CPU, 32k to 64k of RAM, dual floppy disc drives with controller, two RS-232-C serial ports, 20-slot card cage, power, fans, and internal cabling. Full access is provided to the card cage from the front, allowing prototype STD BUS systems to be assembled into the card cage, cabling to be connected from input/output cards to external devices, and system development to proceed with all of the utilities and features of a disc operating system. In-circuit emulation is not required, as the target system hardware is being used directly for development and test.

For realtime systems that require hardware trace capabilities, an external emulation device such as a Millenium uSE can be connected to the system. Once programs are downloaded for test, the two units can operate independently.

Version 2.2 of the CP/M disc operating system includes complete assembly language development capabilities, with editor, assembler, utilities, and dynamic debugger, featuring breakpoint, single-step, and traced execution operation. Macro assemblers and languages such as BASIC, FORTRAN, Pascal, C, and PL/1 are available options.

Languages generating P/ROMable code allow a dedicated P/ROM based control system to be developed in a higher level language on the system. As an example, using the features and utilities of the disc operating system, control applications can be written in FORTRAN and tested in the system's RAM.

When completely verified, the FORTRAN source file can be used to create a P/ROM version of the same program, with P/ROM/RAM addressing modified to operate on a dedicated system. The development system then can be coupled to a P/ROM programmer for P/ROM replication.

Circle 466 on Inquiry Card

16k-Byte CMOS RAM Board Includes Onboard Battery Backup

Onboard batteries and battery charger with short circuit and overcharge protection provide a minimum of 168 hours of memory retention for the BP-0200 memory board after removal of 5-Vdc bus power. Multibus compatible, the board is produced by NEC Microcomputers, Inc, 173 Worcester St, Wellesley, MA 02181, and utilizes the company's μPD444 CMOS RAMs for both 8-bit bytes and 16-bit data words.

Measuring 12 x 6.75 x 0.5" (30.48 x 17.15 x 1.27 cm), the board features software controlled 8- or 16-bit word size and supports 16- or 20-bit addressing; memory inhibit allows paging of two or more boards to the same address block. Address selection is jumper selectable along 16k-byte blocks. Read access time is 450 ns max, while read cycle time is 600 ns max.

Intended for data logging, process control, medical instrumentation, and small business systems, the board uses three type AAA NiCd cells, providing a 3.6-V, 180-mAh power source.

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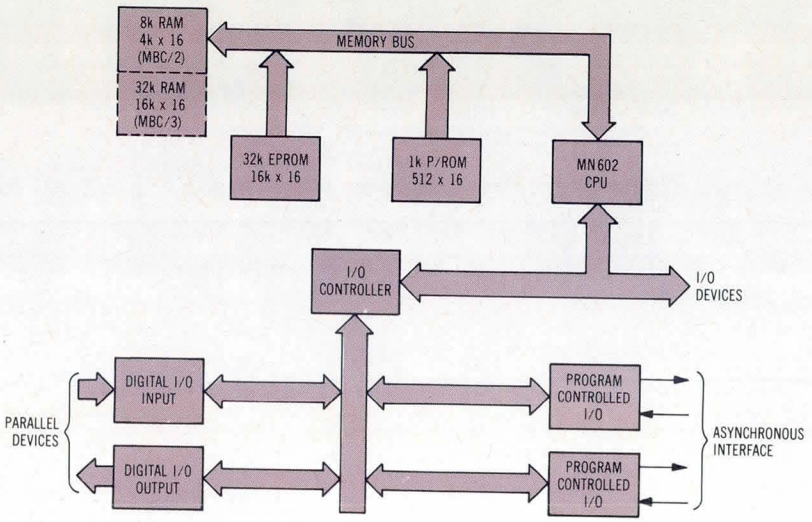
CIRCLE 109 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

Single-Board Computer Products Increase Systems Capabilities

Two single-board computers, a central processor based debugging aid, and input/output (I/O) expansion interface are compatible with the microNOVA™ board computer (MBC) family from Data General Corp, Rte 9, Westboro, MA 01581. The MBC/2 and MBC/3 computers include a central processor, three types of memory, and serial and parallel I/O on a single 7.5 x 9.5" (19 x 24-cm) board. The MBC/SDX board is combined with an MP/100 or MP/200 central processor to provide (I/O) interface for the system, permitting use of microNOVA hardware and software in MBC debugging applications. All I/O features of the MBC/2 board are included on the MBC/SDX.



16-bit processor based single-board computer. Intended for realtime applications in instrumentation, communications, data acquisition, and control, the board can stand alone or utilize resources of microNOVA system. MBC/SDX board consists of I/O bus structure of single-board computer and functions as a debugging aid or expansion interface

Both MBC/2 and MBC/3 are based on the microNOVA MN602 central processor unit, which provides full NOVA architecture, hardware stack and frame pointer, 16-bit hardware multiply and divide, realtime clock, and 16-level priority interrupts. The boards differ only in RAM capability, with 8k and 32k bytes for the MBC/2 and MBC/3, respectively.

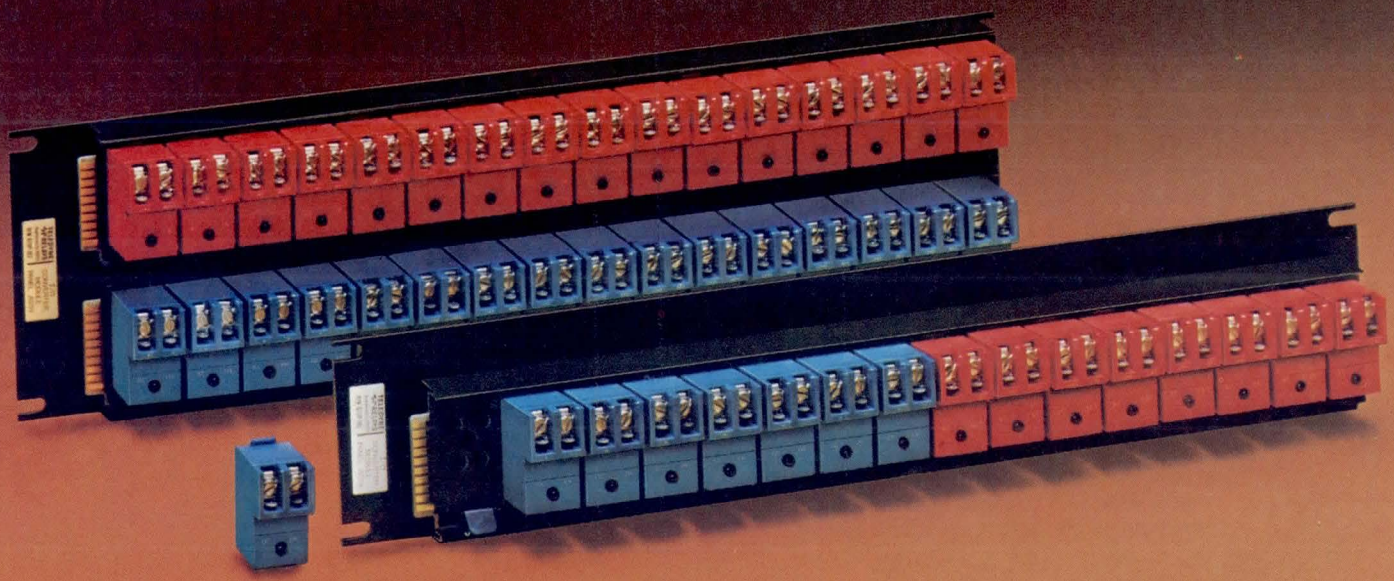
Sockets for up to 1k bytes of P/ROM and for up to 32k bytes of EPROM are provided. The boards also have 2 independently programmable asynchronous/synchronous communication interfaces, 16 lines of digital input, and 16 lines of digital output.

Configurable in a 4-slot card frame, as well as an 8-slot MP/100 or MP/200 chassis, runtime support for the computer boards is provided by the MP/OS operating system. Application programs using Pascal, FORTRAN, or assembly languages on NOVA or microNOVA based systems under MP/OS, or on ECLIPSE computers under AOS can be developed. The MP/OS operating system, along with MP/Pascal and MP/FORTRAN IV, is designed to support ROM based applications using the EPROM facilities of the MBC/2 and 3.

Circle 468 on Inquiry Card

SSR UPDATE

We put a generation of know-how into this industrial I/O system



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If you want the best in I/O systems compatible with today's microprocessor-based single board computers, call on the folks who started it all – Teledyne Relays.

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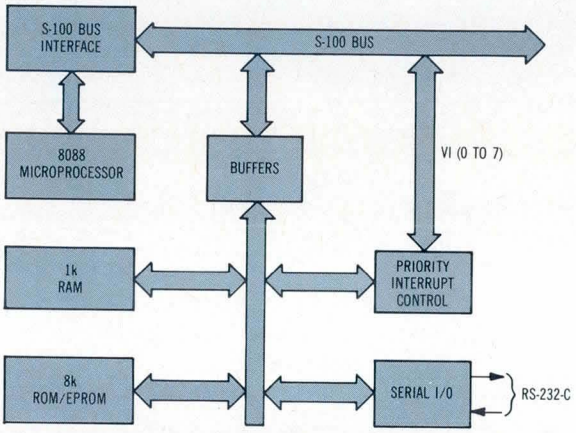
CIRCLE 111 ON INQUIRY CARD

CPU Board Increases Performance of S-100 Bus Systems



S-100 CPU board interfaces 8088 processor to S-100 bus. 16-bit data paths are used internally through an 8-bit interface, enabling use of many current S-100 system boards. 4-byte fetch ahead queue permits throughput approaching 16-bit data bus in some applications

Advantages of 16-bit internal data paths and 8-bit external interface can be realized on S-100 bus systems with the LDP88 CPU board. The instruction set is fully 8086 compatible, and the 8-bit 8088 enables use of S-100 bus boards with memory and peripheral controllers that are 8-bit oriented. The board includes 8088 processor, serial interface port controlled by an 8251A, two ROM/EPROM sockets (2716 or 2732) for a maximum of 8k bytes, and 1k bytes of RAM. A product of Lomas Data Products, 11 Cross St, Westborough, MA 01581, the board is a complete processor and can stand alone.

Eight levels of vectored interrupts and a serial RS-232-C port are included. 8088 software is compatible with the 8086 and offers significant performance improvement over 8-bit processors. Memory address range is extended to 1M bytes.

Circle 469 on Inquiry Card

Disc Drive Family Extends HP-85 Memory Capacity

Up to 1.08M bytes of storage for the HP-85 personal/professional computer can be provided by the HP 82900 series of drives. The drive family includes single and dual double-sided, double-density 5.25" (13.34-cm) discs with capacities of 270k to 1.08M bytes and can be configured in master/slave arrangements as memory requirements increase.

Interface between the HP-85 and the disc drives is through the HP-85 mass storage ROM, also a product of Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304. With the mass storage ROM plugged into the HP-85, the disc operating system is ready to function when power is applied, and disc memory is totally integrated into the HP-85 system, requiring no bootstrapping.

Included in the ROM are 30 additional BASIC commands, many of which are programmable. Other features of the ROM are a Translate command that automatically upgrades previously written tape based programs for use on the disc drives, the ability to store and retrieve the graphics display on the CRT, and automatic default to the disc drive so that the drive is subject to mass storage commands at application of power.

Single drives include the HP 82902M single master drive (270k bytes) and HP 82902S single add-on drive, producing a total of 540k bytes. Dual drive configurations available are the HP 82901M dual master drive with 540k-byte capacity and HP 82901S dual add-on drive that doubles the total storage.

Circle 470 on Inquiry Card

Single-Board Assembly Provides IEEE-488/S-100 Systems Interface

A universal interface for general purpose interface bus (GPIB) and S-100 systems complies fully with the IEEE-488 GPIB standard and proposed IEEE-696 (S-100) standard. The model 1020A communicates with a microprocessor by means of input/output ports and can be configured for polled or interrupt driven input/output functions. All data and address lines are fully buffered from the S-100 bus.

From Dylon Corp, 3670 Ruffin Rd, San Diego, CA 92123, the interface handles all IEEE-488 functions, such as talker, listener, and controller, with system control and pass control capabilities. Other functions include service request, parallel or serial poll, device clear and trigger functions, automatic source and acceptor handshakes, and remote or local options with local lockout capabilities.

(continued on page 196)

Now available in plain or fancy.

Yes, Virginia, now there really are two Dumb Terminal® video displays. And they're available for immediate delivery.

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CIRCLE 112 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

Addressing modes are single and dual, with secondary addressing capabilities.

Functioning as a controller, the interface is capable of managing communications over the GPIB such as addressing and sending commands. Capabilities include operation as a system controller or a controller that can pass control to another controller. All bus commands can be transmitted to devices on the GPIB, service request functions are available, and complete serial and parallel poll functions are included. S-100 based systems can use the interface to take advantage of the IEEE-488's capacity for integration of multiple instruments and devices for data acquisition, automatic testing, and general purpose lab use.

Circle 471 on Inquiry Cards

Microprocessors and Ancillary Products Meet MIL-STD-833

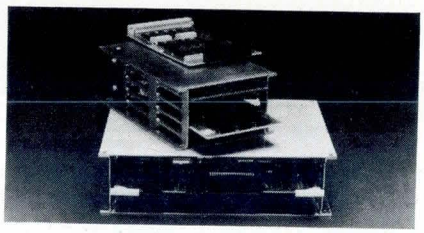
Operable over a −55 to 125 °C range and meeting MIL-STD-833, method 5004, ten 6800 family microprocessors and accessories are available from American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051. The company offers three standard screening options in classes B and C.

Class B to the current official version of method 5004 requires temperature extreme electrical testing both on a 100% and on a group A sampling basis. Class B method 5004.0 requires temperature extreme electrical testing only on a group A sampling basis.

Products available are S6800 8-bit microprocessor, S6802 8-bit microprocessor with clock, S6810 1k-bit (128 x 8) static read/write memory, S6821 peripheral interface adapter, S6840 programmable timer, S6852 synchronous serial data adapter, S6831B 16k-bit (2048 x 8) static NMOS ROM, S5101 1k-bit (256 x 4) static CMOS RAM, and S6508 1k-bit (1024 x 1) static CMOS RAM.

Circle 472 on Inquiry Card

Backplane Bus Structure Is Applications Oriented



Z-bus backplane interconnect structure. Designed to work with the Zilog ZCM family of single- and double-size microcomputer boards, the system operates with Z8, Z80, and Z8000 and memory expansion, I/O, and peripherals

Designed to work with the Z-Bus component interconnect (ZCI) and Zilog computer module family (ZCM), the Z-Bus backplane interconnect structure (ZBI) from Zilog, 10340 Bubb Rd, Cupertino, CA 95014, handles 8-, 16-, and 32-bit processors. The bus is suitable for single processor controllers or advanced multiprocessing tasks utilizing the company's Z8, Z80, and Z8000 microprocessors.

Features of the ZBI structure include parity lines, ground lines distributed between signals for noise reduction, and terminated bus lines. A total of 32 address/data lines and 28 control lines provide the capability to accommodate future 32-bit microprocessors.

Address and data information share the same lines, permitting extended word sizes and minimizing the number of bus lines and buffers, and backplane connector size. Word size of each transaction is defined by a combination of two separate signals, enabling 8-, 16-, and 32-bit devices to communicate on the same bus within a single system. The ZBI bus structure is supported by ZCM products, including a Z8 based single-chip microcomputer and Z8000 based microprocessor board.

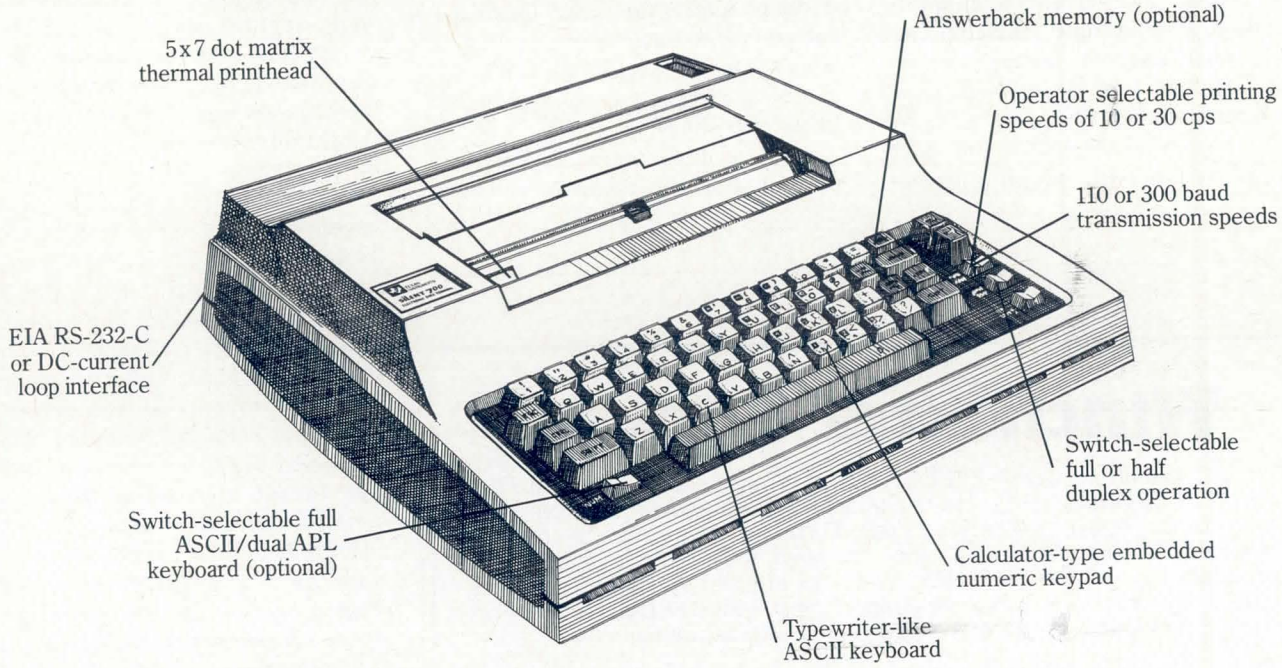
Circle 473 on Inquiry Card

IMMEDIATE DELIVERY

The Silent Commander.

743 KSR

Keyboard Send-Receive Data Terminal



TI's *Silent 700** Model 743 KSR Data Terminal can help you take command of your data entry application needs today. The compact 743 offers a variety of easy-to-use standard features and options, and is an ideal input/output console. And with virtually silent thermal printing, the low-cost 743 leads the way for efficiency and reliability. The field-proven 743 is also available as a Receive-Only model.

With either 743, you can depend on high-quality *Silent 700* performance.

TI is dedicated to producing quality, innovative products like the 743 KSR Data Terminal. TI's hundreds of thousands of data terminals shipped worldwide are backed by the technology and reliability that come from 50 years of experience, and are supported by our worldwide organization of factory-trained sales and service representatives.

For more information on the 743 terminals, contact the TI sales office nearest you or write Texas Instruments Incorporated, P.O. Box 1444, M/S 7784, Houston, Texas 77001, or phone (713) 937-2016. In Europe, write Texas Instruments Incorporated, M/S 74, B.P. 5, Villeneuve-Loubet, 06270, France.

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CIRCLE 114 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

In-Circuit Emulation Support Available For M68000 and Z8002

For use with 2300 series single-user and 2301 development network configurations using floppy or hard disc storage, the 2300 slave emulator accomplishes program execution and emulation. User microprocessor resources are not used for debugging purposes with the emulator from GenRad/futuredata, 5730 Buckingham Pkwy, Culver City, CA 90230. The emulator supports simultaneous, multiple emulation for up to eight different microprocessors and includes breakpoint and logic analyzer features.

All features of the M68000 and Z8002 are fully supported, including execution speed, control lines, interrupts, and address space. Programs are executed at full processor speed using either an internal or a prototype clock without wait states or other timing constraints.

Full symbolic debugging is available, allowing program labels to be used in place of absolute addresses in all commands. Auto command completion allows entering of only an abbreviated command syntax from the keyboard while having the full command appear on the display. A Help display describes function and options for the command.

Four complex breakpoints are used to control program execution and logic analysis. Breakpoints may be set to contents of address and data buses, status of control lines, and four external probes. A timer measures time in microseconds or cycles between breakpoints. Logic analyzer capture is 256 traces of 64 lines.

Software development support consists of file management and text editing for program entry, relocatable macro assembler and linkage editor for program development, and interface software to the emulator for program execution and emulation.

Circle 474 on Inquiry Card

μComputer Development System Operates in Industrial Environment

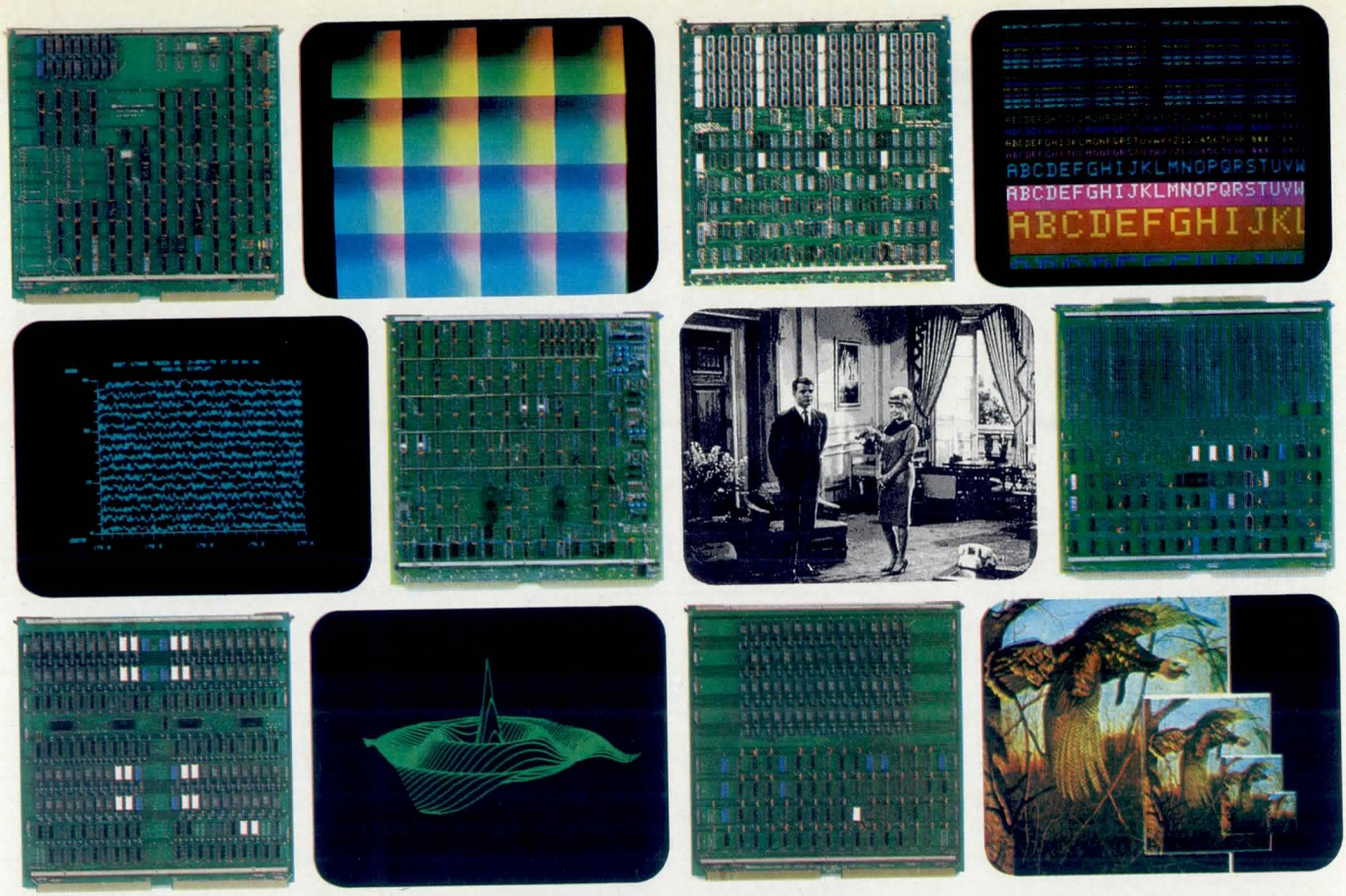
Intended for software development and distributed microcomputer network applications in industrial environments, the standalone, floppy disc based 3805A microhost/development system has an ambient operating temperature range of 5 to 35 °C, 20 to 80% RH.

Based on a Z80A, the system measures 17 x 22 x 15.5″ (43.2 x 55.9 x 39.4 cm), weighs 62 lbs (28.1 kg), and is a product of Xycom, Inc, PO Box 984, Ann Arbor, MI 48106. The system includes 96k bytes of RAM with no wait states, and bank switched memory management, parallel and serial input/output (I/O), free-standing 93-key intelligent keyboard and built-in IBM 3740 format compatible floppy disc drive providing 250k bytes of storage, and a tabletop line printer. Options include an EPROM programmer and a single-, dual-, or triple-disc drive floppy subassembly realizing up to 1M byte of storage.

TTL-compatible serial I/O signals can be converted to 20-mA current loop, RS-232-C, -422A, or -423A specifications through the use of available communication adapters. One channel is provided with a 20-mA adapter, and three serial I/O channels are available for user configuration.

System software is tailored to ease development of realtime control industrial applications programs for the company's 180+, 180, 280, 380, and 390 based microcomputer systems. Host/development system software package includes three independent software systems: Industrial Pascal, BASIC, and SPDS. SPDS supports FORTRAN (FORTRAN compiler and runtime libraries).

Circle 475 on Inquiry Card



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GENISCO COMPUTERS

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CIRCLE 116 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

Error Correcting Dynamic RAM Board Operates With S-100 Bus Standard

Capable of addressing up to 16M bytes and of being configured for 8- or 16-bit processors, Supermem 3 is a high speed dynamic RAM memory board that automatically detects and corrects all single-bit errors before they reach the CPU. Double-bit errors and component failures are reported by the board from Piiceon, Inc, 2350 Bering Dr, San Jose, CA 95112.

Measuring 9 x 10″ (22.9 x 25.4 cm), the double-height board contains 64k bytes and operates at 3 MHz either in 8- or 16-bit systems. Access time is 330 ns max, with a cycle time of 400 ns. Single- and double-bit error reporting is controlled by software; an error status register is available for interpreting syndrome bits into a failing memory location. Memory refresh is totally transparent to the processor.

Circle 476 on Inquiry Card

Z80 CPU Board Includes S-100 Front Panel Compatibility

S-100 systems can use the speed and instruction set of the Z80 by implementing the 2810 CPU board from California Computer Systems, 250 Caribbean Dr, Sunnyvale, CA 94086. The board supports front panel operations and is fully compatible with Altair and Imsai computers, as well as a majority of S-100 systems without front panels.

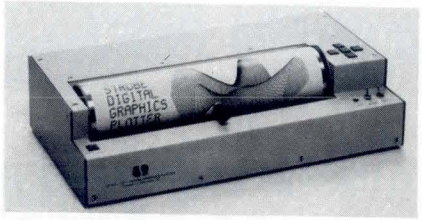
Standard features for the board include a jumper enabled 2k ROM containing monitor firmware and monitor with auto baud select, allowing the serial port to match any baud rate from 2 to 56k set at the console. Phantom overlay of the ROM's memory space, Refresh, Nonmaskable Interrupt (NMI), and MREQ can be enabled.

A switch allows 2- or 4-MHz clock rate selection and LEDs indicate Halt state, ROM Enabled, and Interrupt Enabled. The board also features CPU and baud rate ICs with separate crystal controls.

Options include an RS-232-C serial input/output (I/O) port which can be used for a console interface and software selectable bits/word, parity, number of stop bits, and baud rate. Other options include I/O address mirroring, power-on jump to any location in 64k, and M1 wait states with optional wait state generation.

Circle 477 on Inquiry Card

Digital Graphics Plotter Offers High Resolution



High resolution drum type plotter. Software package includes flexible alphanumeric generation, variable character sizes, horizontal and vertical character strings, 90° character rotations, axis generation, and vector plotting

Utilizing 4ϕ stepping motors for drum and pen motion, the model 100 graphics plotter can provide X-Y axis control in 0.004″ (0.01-cm) increments. The drum is designed to accept 8.5 x 11″ (21.6 x 27.9-cm) paper, and the pen holder can accommodate a variety of pens. The plotter uses an interactive digitizing mode of operation for entering X-Y coordinate data corresponding to pen location directly into a computer.

Assembly language vector software support for 8080/8085, Z80, and 6502 microprocessors is provided. Source listings and flowcharts are included. Also offered is a plot applications software package that runs with most versions of BASIC and FORTRAN. Computer interface is through two parallel 8-bit output ports and one 8-bit input port. Optional interfaces for TRS-80, Apple, PET, and S-100 bus computers also are available.

Specifications for the unit include 8 x 10″ (20.3 x 25.4-cm) plotting area, 3″ (7.6-cm)/s max pen or drum velocity, and parallel TTL input/output of nine bits from output port and six bits to input port. Overall dimensions of the plotter from Strobe, Inc, 897 Independence Ave, Mountain View, CA 94043, are 3.5 x 15.5 x 8.5″ (8.9 x 39.4 x 21.6 cm).

Circle 478 on Inquiry Card

Low Cost Single-Board Computer Utilizes Z80 Microprocessor

A Z80 CPU, sockets for 2k or 4k bytes of P/ROM, up to 2.1k bytes of RAM, 16 input/output lines, system clock, and 12 decoded address strobes are included in the M-80 microcomputer from Miller Technology, 16930 Sheldon Rd, Los Gatos, CA 95030. The board also has a drilled breadboard area for additional user circuitry.

Two software packages are available. A monitor contained in a single ROM enables users to dump or enter data into memory, set breakpoints, control input/output (I/O) lines, or download programs from another computer. An integer BASIC provides 30 functions and commands, and permits calling machine language routines. Both monitor and BASIC use serial I/O for communications. Baud rates of 110, 300, and 1200 are available.

Designed for test equipment, smart peripheral controllers, and dedicated control and processing applications, the 4.5 x 6.5″ (11.4 x 16.5-cm) board can be mounted in a card cage or by using standoffs.

Each of the 16 I/O bits can be individually selected as either an output or an input. As outputs, the bits can be individually set, reset, or tested for current output state; as inputs, the bits can be read individually. Alternatively, the 16 bits can operate as two separate I/O ports on an 8-bit wide basis; or one of the 8-bit ports can be defined either as a strobed input port, or a strobed output port with full handshaking. Unit prices are $28.50 for the bare board, $69 for the kit, and $185 for an assembled and tested board.

Circle 479 on Inquiry Card

The new VISUAL 200 terminal has the features of competitive terminals and will code-for-code emulate them as well. A flick of a switch on the rear panel programs the VISUAL 200 for compatibility with a Hazeltine 1500, ADDS 520, Lear Siegler ADM-3A or DEC VT-52. This allows you to standardize on the new, reliable VISUAL 200 for virtually all of your TTY compatible video terminal applications, with no change in the software you've written for the older, less powerful terminals. And you're not limited to mere emulation; you can outperform them at the same time by taking advantage of the additional features and human engineering of the VISUAL 200, such as:

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- Tilt Screen (10° to 15°)
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FEATURE COMPARISON CHART

FEATURE	Visual 200	Hazeltine 1500	Hazeltine 1420	Lear Siegler ADM-3A	Digital VT-52	ADDS 520	ADDS Regent 20	ADDS Regent 40
24 x 80 Screen Format	STD	STD	STD	STD	STD	STD	STD	STD
7 x 9 Dot Matrix	STD	STD	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**
Background/Foreground	STD	STD	STD	**NO**	**NO**	**NO**	**NO**	STD
Insert/Delete Line	STD	STD	**NO**	**NO**	**NO**	**NO**	**NO**	STD
Insert/Delete Character	STD	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**
Clear End Line/Field/Page	STD	STD	**NO**	**NO**	STD	**NO**	**NO**	**NO**
Blink	STD	**NO**	STD	**NO**	**NO**	**NO**	**NO**	STD
Security Mode	STD	**NO**	STD	**NO**	**NO**	**NO**	**NO**	STD
Columnar and Field Tab	STD	**NO**	STD	**NO**	**NO**	**NO**	**NO**	STD
Line Drawing	STD	**NO**	**NO**	**NO**	STD	**NO**	**NO**	STD
Upper/Lower Case	STD	STD	STD	**OPT**	STD	**NO**	STD	STD
Numeric Pad	STD	STD	STD	**OPT**	STD	**NO**	**NO**	STD
Composite Video	STD	**NO**	**NO**	**NO**	**NO**	STD	**NO**	**NO**
Current Loop	STD	STD	**NO**	**OPT**	**OPT**	STD	STD	STD
Serial Copy Port	STD	STD	**OPT**	STD	**OPT**	**NO**	STD	STD
Hold Screen	STD	**NO**	**NO**	**NO**	STD	**NO**	**NO**	**NO**
Detachable Keyboard	STD	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**
Solid State Keyboard	STD	**NO**	**NO**	**NO**	**NO**	**NO**	STD	STD
Typamatic Keys	STD	STD	STD	**NO**	**NO**	**NO**	STD	STD
Cursor Addressing	STD	STD	STD	STD	STD	STD	STD	STD
Read Cursor Address	STD	STD	STD	**NO**	**NO**	**NO**	**NO**	STD
Cursor Control Keys	STD	**NO**	STD	**NO**	STD	**NO**	**NO**	STD
Secondary Channel	STD	**NO**	**NO**	STD	**NO**	STD	**NO**	**NO**
Self Test	STD	**NO**	STD	**NO**	**NO**	**NO**	**NO**	STD
Baud Rate to 19,200	STD	STD	**NO**	STD	**NO**	**NO**	**NO**	**NO**
Smooth Scroll	STD	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**
Microprocessor	STD	STD	STD	**NO**	STD	**NO**	STD	STD
Tilt Screen	STD	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**
Switchable Emulations	STD	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**	**NO**

The new VISUAL 200 obsoletes competitive terminals without obsoleting the software.

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CIRCLE 117 ON INQUIRY CARD

DS BRIEFS

Dynamic Memory Board Operates at 1.2-MHz Clock Rate—Intended to operate with 6502 based systems, the 6502DM board is available from Beta Computer Devices, 1230 W Collins Ave, Orange, CA 92668, in board only, and in 16k- and 32k-byte arrangements organized in 4k-byte blocks. Each block is independently addressable on any 4k address within the 64k address space. Circle 484 on Inquiry Card

A-D Conversion Module Is S-100 Compatible—Designed for direct conversion of voltages from thermocouples, level sensors, and other low level signals, the AIM-12 board features onboard resistor programmable instrumentation amplifier and 25-μs conversion time. From Dual Systems Control Corp, 1825 Eastshore Hwy, Berkeley, CA 94710, the board uses BASIC or assembly language instructions. Circle 485 on Inquiry Card

Field Upgrade Memory System Is Available—A 14″ (35.6-cm) hard disc/controller system available from Digital Microsystems, Inc, 4448 Piedmont Ave, Oakland, CA 94611, can be added to the company's DSC-2 or other Z80 based computers. Providing up to 27.4M bytes, the HD0-4000 includes intelligent controller, cables, and power supply. Interface is via an 8-bit parallel port. Circle 486 on Inquiry Card

Dynamic RAM Module Can Use External Battery Backup System—A product of Adaptive Science Corp, 4700 San Pablo Ave, Emeryville, CA 94608, Module 1560 is a 32k-byte dynamic RAM board featurin refresh that is automatic anc transparent to system programs. Up to eight boards can be combined to provide 256k bytes of capacity. Circle 487 on Inquiry Card

Database Management System Enhances Apple II File Management—Composed of four Apple-soft programs, Filemaster II, from Rainbow Computing, Inc, 9719 Reseda Blvd, Northridge, CA 91324, facilitates storing, classifying, manipulating, and retrieving data for the Apple II microcomputer. Special input routines, menu driven programs, error trapping, and full documentation are included. Circle 488 on Inquiry Card

Wirewrap Board Operates With EXORciser Family Bus Structure—The 4-6800 board is pre-pinned with screw machined socket pins configured to provide maximum density of ICs and discrete components. Other family products from Hybricon Corp, 410 Great Rd, Littleton, MA 01460, include the 2-6800 (pre-pinned V_{CC}, ground, and I/O), 6800ET extender card, and 6800 DOC K documentation kit. Circle 489 on Inquiry Card

Networking Module Allows Shared Discs and Printer—NOS.2, a disc based operating system from Cambridge Development Laboratory, 36 Pleasant St, Watertown, MA 02172, is upwardly compatible with CP/M 1.4 and can run on the Z80 and 8080 family of microprocessors. Discs and printer can be shared by large number of microcomputers; master system software requires 64k and satellites need 32k. Circle 490 on Inquiry Card

Cross-Assembler and Linker for M68000 Runs on PDP-11—Using Motorola-compatible mnemonics and instruction formats, the cross-assembler from Ruben Engineering Corp, 60 Aberdeen Ave, Cambridge, MA 02138, features full expressions with Add, Subtract, Multiply, Divide, And, Or, and Shift operators. The linker's object file is suitable for M68000 downloading. The system runs on RSX-11M, UNIX, and VAX operating systems. Circle 491 on Inquiry Card □

SOFTWARE

Interactive Compiler Includes Realtime Monitoring Capability

Designed for systems using the M6809 microprocessor or monoboard computer, the resident M6809 BASIC-M™ interactive compiler is a high level programming language with particular emphasis on realtime, process control, and business related applications problem solving. A product of Motorola Semiconductor Products, Inc, PO Box 20912, Phoenix, AZ 85036, the compiler produces position independent object programs. Target programs may be executed in an M6809 system and are not limited to development system environment.

Minimum configuration for BASIC-M compilation includes M6809 EXORciser with EXORdisc II/III, EXORciser compatible terminal, and M6809 MDOS; or M6809 EXORterm with EXORdisc II/III and M6809 MDOS; or EXORset with XDOS. Each configuration requires 48k bytes of RAM.

Realtime monitoring functions allow easy monitoring of external events or conditions and permit execution of service routines when specified events or conditions occur. Monitoring functions remain effective until a new condition occurs or Never statements halt the monitoring of events or conditions.

Circle 480 on Inquiry Card

Network Operating System Uses Hardware Independent Approach

Portability of CP/NET, a software system which allows independent microcomputer access to common facilities such as peripherals, data bases, and programs, is provided by separating the logical operating system from the hardware environment. All hardware dependent code is placed in one input/output module, making CP/NET network independent.

The system, a product of Digital Research, Inc, PO Box 579, Pacific Grove, CA 93950, operates with the company's CP/M™ operating system and MP/M™ multiuser operating system. The network consists of one or more masters running MP/M and one or more slaves running CP/M or MP/M. A network may be constructed with any combination of shared memory, serial links, or parallel input/output with any protocol, such as X.25, BISYNC or SDLC.

Circle 481 on Inquiry Card

Signal Processing Package Exhibits Speed and Flexibility

Comprehensive data acquisition, preprocessing, and signal processing library functions, including a complex FFT function, are provided by Sigpak, a signal processing package from Plessey Microsystems, 19546 Clubhouse Rd, Gaithersburg, MD 20760. Designed to operate with the company's MIPROC-16 microcomputer, the package is said to promote efficient implementation of signal processing systems for special applications in realtime processing.

Data acquisition on up to 64 analog channels is supported by the package, which can be used to process optical, audio, or other time-variate data without using array processing.

Software resident in P/ROM on an applications memory module can be divided into four parts: user interface, analog acquisition and preprocessing, spectral analysis, and bivariate analysis. The analog acquisition utility reads raw data from the analog input channels, performs realtime transformations, and saves the data for future analysis. Features supported are up to 64 single-ended inputs with sample rate selectable, formation of up to 64 synthetic channels, and calculation of minimum, maximum, mean, rms, and standard deviation. Also included are formation of minima and maxima histograms and array production for spectral or bivariate analysis.

The FFT analysis utility provides 1024 real point input and 512 complex frequency output with frequency response and resolution, power spectrum, and spectra averaging. Block floating point format and fractional binary 2's complement arithmetic are utilized. Bivariate analysis utilizes a 2-axis histogramming technique in which two 1024-point arrays are processed to form one 256-word, 2-dimensional array.

Circle 482 on Inquiry Card

Computer Utility Permits Multiple Use of Data

Available for TRS-80, Level II BASIC/disc BASIC applications, VARKEEP is a disc resident machine language utility that allows users to save, restore, and manipulate one set of data that may be common to two or more programs. The utility, available from Percom Data Co, 211 N Kirby, Garland, TX 75042, operates with the company's OS-80™ or TRSDOS disc operating systems.

Four BASIC commands (Name Save, Name Restore, Name Delete, and Name Clear) are added by the utility to protect values of variables from erasure, restore program variables used in another program, delete variables no longer needed, and change the amount of string space available. Name Restore also provides the means to simulate the Chain command found in other BASICs.

Circle 483 on Inquiry Card

DIGITAL SIGNAL PROCESSING SYSTEMS MOVE TO FLOATING POINT ARITHMETIC— PART 3: VLSI ADDITION

Louis Schirm IV

TRW LSI Products

2525 E El Segundo Blvd, El Segundo, CA 90245

Addition in floating point is more complex than multiplication because action on the mantissa is dependent on exponent values, causing a floating point adder chip to require about 50% more circuitry than a floating point multiplier. This discussion of the basic design considerations for a high speed floating point adder very large scale integration chip considers the general concepts of floating point arithmetic as presented in Part 1 (*Computer Design*, Aug 1980, pp 156-160) and the hardware details for implementing floating point multiplication (Part 2, *Computer Design*, Sept 1980, pp 188-193).

Implementing the Adder

A floating point adder's level of complexity is indicated by the necessary operations shown in Fig 1. The sequence starts by comparing the exponents to determine which is larger and by how much. Then, the mantissa with the smaller exponent is downshifted to normalize the two numbers relative to each other. For example, if one number is 0.1719×10^{14} and the other is 0.9421×10^{12}, the second

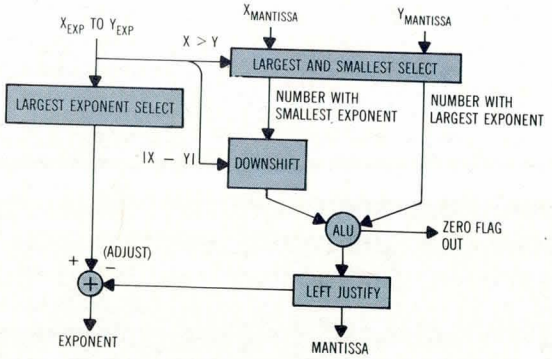

Fig 1 Floating point adder operations. Complexity results from adjustment of mantissas required when inputs have different exponents

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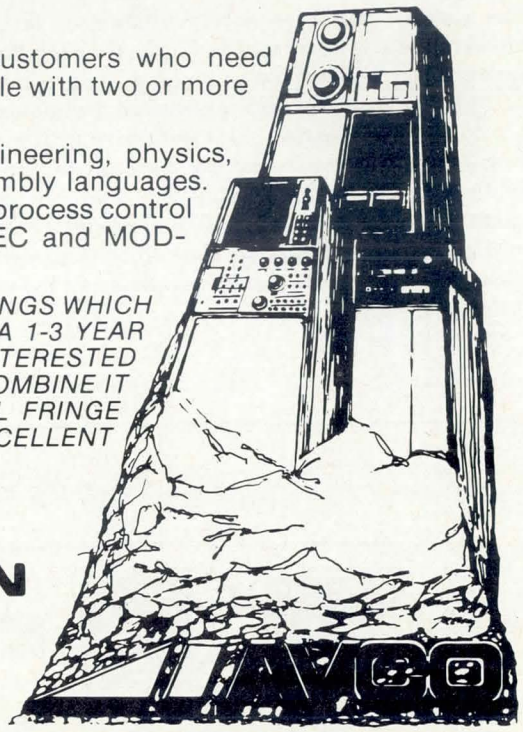

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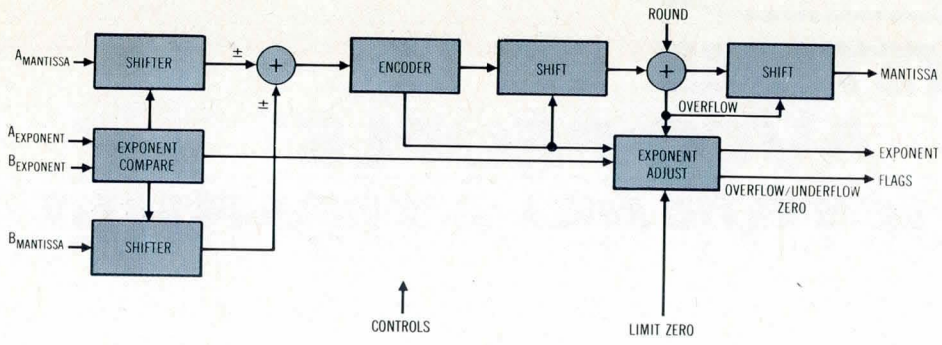

Fig 2 Floating point adder architecture. Feeding output exponent and mantissa back to inputs would provide accumulator function

number must be changed to 0.0094 x 10^{14} before the addition is performed. After the addition, the resultant mantissa is examined to determine how many leading zeros there are. The mantissa is upshifted in enough places to normalize it (left justification), and then the exponent is decremented. If the mantissa answer exceeds 1.0, it must be downshifted and rounded to single precision. Flags are generated if the exponent goes out of range or if the answer is zero.

One possible hardware implementation of the floating point adder chip is illustrated in Fig 2. Although the chip is complex, it can be designed and built using present state of the art bipolar semiconductor processing techniques. When this is done, use of floating point arithmetic in digital signal processing systems will increase because of the system simplification. Such a circuit might include an accumulate function to facilitate the summation of products in the standard digital signal processing algorithms. This can be implemented by feeding the output mantissa and the exponent back into the inputs.

The fundamental architecture shown in Fig 2 points out that, unlike the multiplier (which has a very regular organization for the mantissa), the adder is a series of subsections with interconnecting buses. Therefore, it does not easily lend itself to a cellular layout structure as in the multiplier.

Package Interconnections

Another problem with the design of a floating point adder chip is packaged interconnection. The largest commercially available package has 64 pins, which puts an upper limit on the word lengths that may be accommodated if parallel buses are used.

A 64-pin arrangement is adequate for a 12-bit mantissa and a 4-bit exponent, providing separate A and B 16-bit inputs, and allowing a 3-bus system. This arrangement, shown in Fig 3, offers the flexibility and speed required in many signal processing systems. However, for those applications

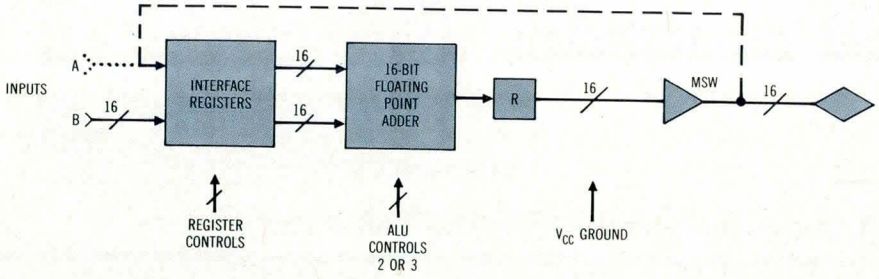

Fig 3 Packaging configuration for floating point adder with 12-bit mantissa and 4-bit exponent. Separate 16-bit A (dotted line) and B inputs result in 64-pin, 3-bus system. Dashed line indicates 48-pin, 2-bus option, with one bus multiplexing between input and output functions

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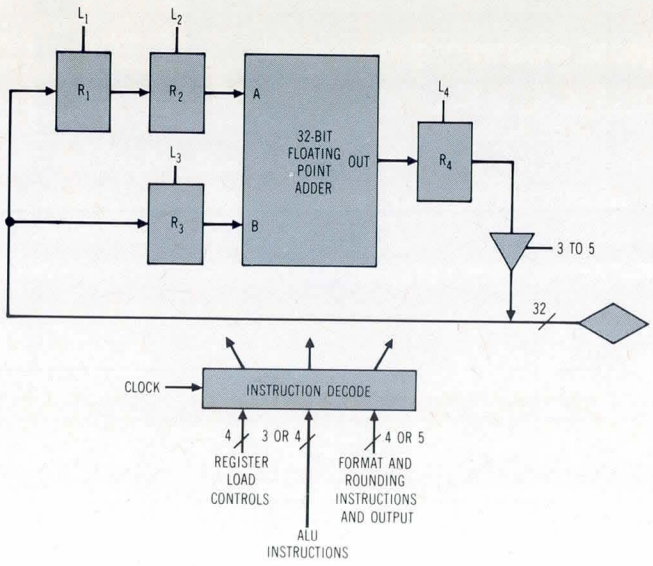
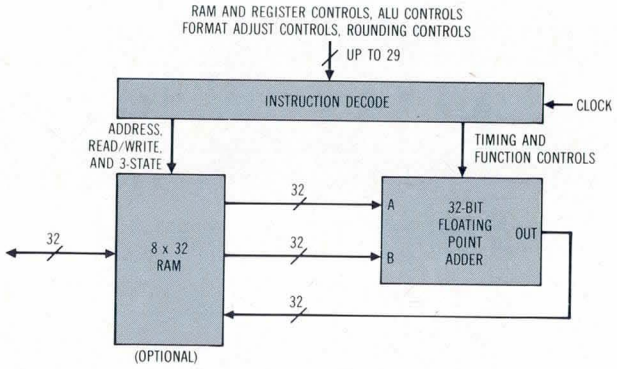


Fig 4 Single-bus options utilize 48 pins (a) or 64 pins (b). Simplification and lower cost result, but operation is less flexible, offering single precision only



where speed is not as important and smaller package size is desirable, the 48-pin, 2-bus option of Fig 3 can be used.

If the user requires the full dynamic range offered by the 32-bit format, there is no alternative to the single bus. The choices shown in Fig 4 offer chip simplicity (lower cost) and ease of usage, but single precision only, versus greater flexibility and multiprecision capability.

Additional Factors

There are also some tradeoffs on speed. The speeds of these adders could be in the range of 100 to 200 ns using relatively standard cells. Input/output registers on the single bus chips could be made fast enough to support this computation speed. To improve speed, lower impedances could be used in the critical delay path areas (dissipating more power), or pipeline registers could be used. However, pipelining increases chip size and complicates the user's programming task.

Standardization is the final issue yet to be resolved in the design of the adder. In floating point multiplication, the mantissa operator is essentially free from standard format constraints. This is not true for addition, since the designer is forced to adopt specific methods for handling such cases as rounding, overflow, and underflow. Numerous incompatible "standards" now exist. However, a subcommittee of the Institute of Electrical and Electronic Engineers has been meeting for over a year in an effort to resolve the problem.

Summary

Digital signal processing systems are now implementing floating point arithmetic to a greater extent. Reducing the size of the floating point multiplier is the first step in applying the power of very large scale integration (VLSI) to floating point, and floating point addition, using VLSI, is the next step. Finally, the format of the adder design must be standardized before fixed point arithmetic can give way fully to floating point arithmetic and, consequently, its wider dynamic range.

Hybrid Data Acquisition System Offers 12-Bit Resolution in Single Package

Designed for military and aerospace applications, the MN7140 from Micro Networks Corp, 324 Clark St, Worcester, MA 01606, is said to be the industry's first complete single-package, 12-bit, hybrid data acquisition system (DAS). This device includes an 8-channel input multiplexer, instrumentation amplifier, track/hold amplifier (T/H) with internal hold capacitor, 12-bit successive approximation analog to digital converter with internal clock and reference, and all the timing to control logic necessary to operate the system from a single trigger pulse.

The standard system has 8 single-ended inputs and can easily be expanded to 16 single-ended or 8 differential inputs with the addition of a single external multiplexer. Operating temperature ranges offered are: 0 to 70 °C, −25 to 85 °C, and −55 to 125 °C. Total time from channel addressing to valid digital output is 59 μs max, a minimum throughput rate of 17,000 channels/s. Only simple address decoding and 3-state buffers are necessary for microprocessor interfacing, and external multiplexers may be added for channel expansion and/or differential operation. Power consumption is 1365 mW max, and all digital inputs and outputs are TTL compatible.

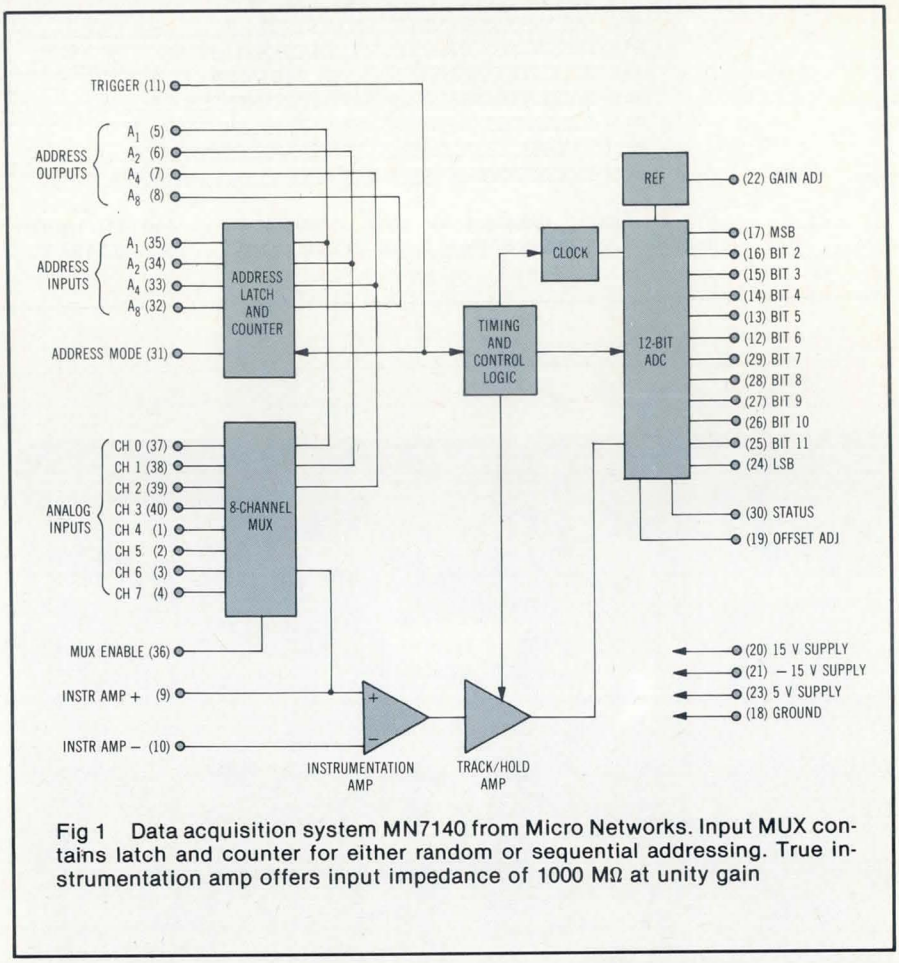


Fig 1 Data acquisition system MN7140 from Micro Networks. Input MUX contains latch and counter for either random or sequential addressing. True instrumentation amp offers input impedance of 1000 MΩ at unity gain

At 25 °C, system linearity is guaranteed to be better than ±0.012% FSR, and system absolute accuracy (without adjustment) is guaranteed to be better than ±0.1% FSR. Over the full operating temperature range, these two parameters are ±0.024% FSR and ±0.4% FSR, respectively. This accuracy results from functional laser trimming of completed devices and would be unachieveable using discrete DAS components without external adjusting potentiometers.

Operation commences as the rising edge of a trigger pulse loads the MUX channel address and initiates a data acquisition and conversion cycle. If sequential addressing is being used, the next channel will be accessed. When random addressing is being used, the channel whose address has been applied to the channel address inputs will be accessed. The rising edge of the trigger pulse simultaneously fires an internal one-shot (10-μs pulse duration) whose output disables the internal clock. After 10 μs, the falling edge of the one-shot drives the T/H into the

(continued on page 210)

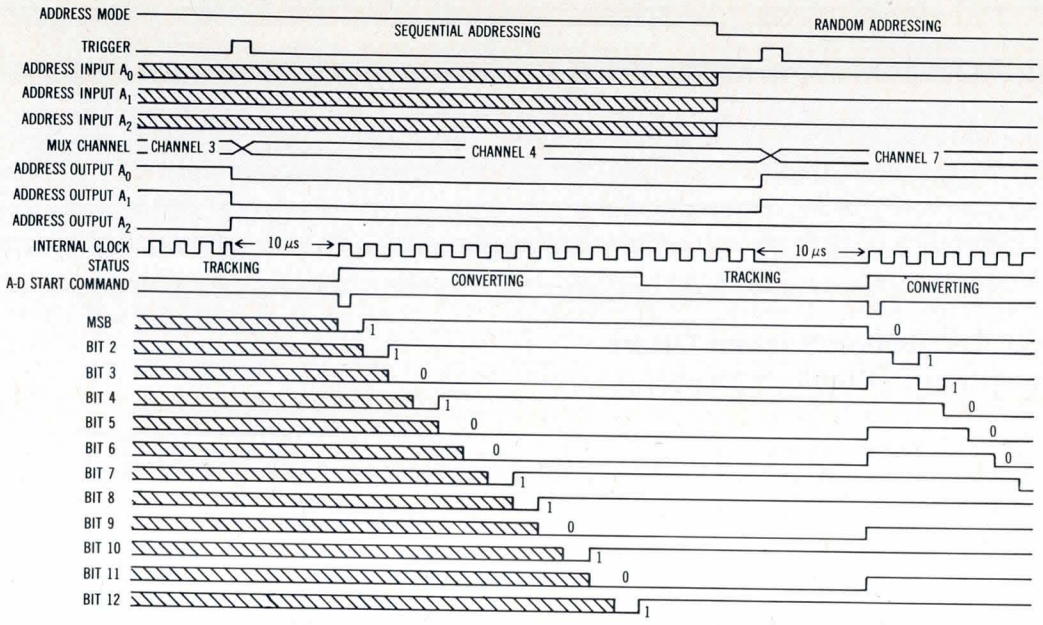


Fig 2 Timing diagram for data acquisition system. Operation shown is for digital word 1101 0011 0101, corresponding to analog input of −6.5137 V

hold mode, gates on the clock, generates a start convert signal for the 12-bit ADC, and drives the status output to a logic 1. Gating off the clock during the time the MUX is settling into its new channel and the T/H is acquiring a new signal reduces noise errors.

When the conversion is complete (approximately 40 μs later), the status output returns to a logic 0, indicating that the conversion is complete, that the digital output is valid, and that the T/H has returned to the tracking mode. The unit is now ready to be triggered for the acquisition and conversion of the next channel.

Absolute maximum ratings limit positive and negative power supplies to ranges between ±0.5 and ±18 V, respectively. The logic supply must stay between −0.5 and 16 V, with digital inputs staying between −0.5 V and the logic supply voltage. Analog inputs are to remain within a ±15-V range. Storage temperature must stay between −65 and 150 °C.

All units are available fully screened and qualified to the requirements of MIL-STD-883, Method 5008. Packaging is provided in a standard ceramic 40-pin, hermetically sealed DIP.

Circle 501 on Inquiry Card

CMOS Hybrid MDAC Serves as Replacement For Monolithic Types

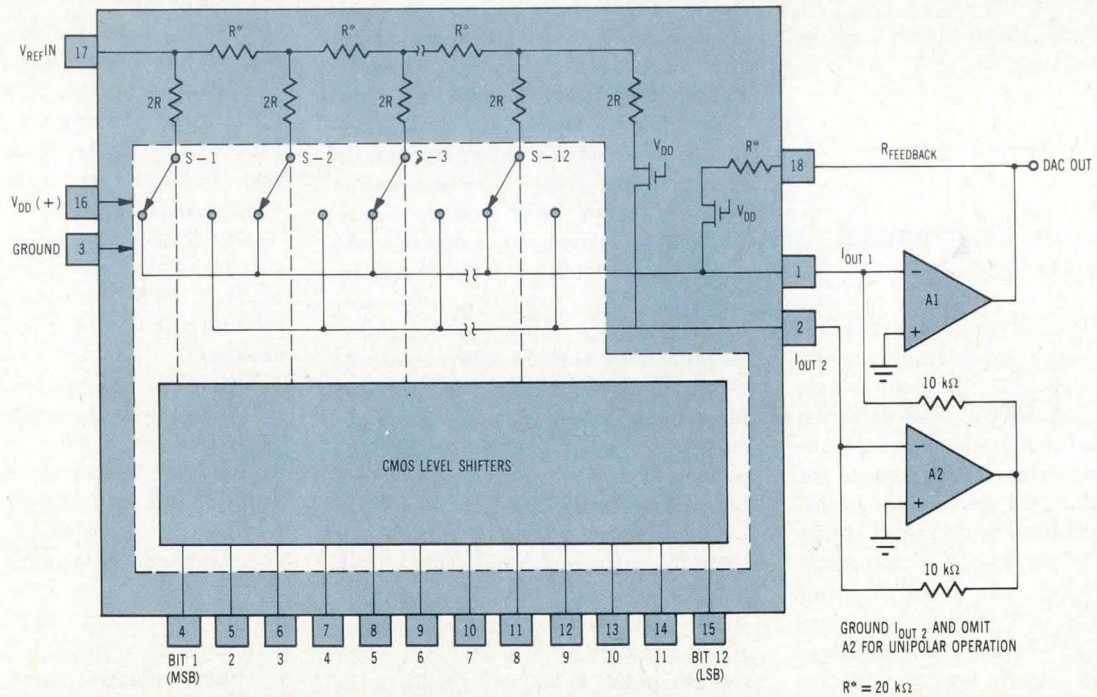
A 12-bit multiplying DAC, the 7541 from Beckman Instruments, Inc, 2500 Harbor Blvd, Fullerton, CA 92634, consists of a CMOS integrated circuit and a nichrome thin film ladder resistor network. Providing a pin for pin replacement for lesser performance 7521 and 7541 monolithic designs, the converter operates from 5- to 15-V supplies and can be driven directly by TTL or CMOS logic.

Characteristics include true 12-bit accuracy, ±5% absolute ladder R tolerance, ±0.002% FSR/%V guaranteed supply rejection, and linearity guaranteed to ±½ LSB over the entire operating temperature range of 0 to 70 °C (commercial model) or ¹55 to 125 °C (military model). Also guaranteed over the temperature range are monotonicity and ±1 LSB gain, after zeroing at 25 °C. Power consumption is 20 mW, typ, making the device appropriate for portable instrumentation or airborne equipment. This DAC incorporates FET switch compensation for the R-2R network, termination resistor, and feedback gain resistor, providing power supply rejection and gain tempco superior to uncompensated monolithic versions.

The CMOS IC provides 12 parallel inputs with level shifters, 2 compensation transistors, and 12 current steering switches. As shown in the figure, each 2R leg of an inverted R-2R ladder is connected to a pair of n-channel transistors. These transistors switch the binary weighted currents that flow in each 2R leg to either the $I_{OUT\ 1}$ bus (logic high input) or to the $I_{OUT\ 2}$ bus (logic low input). Normal operation maintains $I_{OUT\ 1}$ and $I_{OUT\ 2}$ at ground or virtual ground.

Absolute maximum ratings limit V_{DD} to ±17 V and V_{REF} to ±25 V. The digital input voltage must remain between V_{DD} and ground. Storage temperature is restricted to a range from −65 to 150 °C. The device is packaged in a standard 18-pin sidebrazed ceramic DIP, available with a polymer seal for industrial applications and a hermetic solder seal with MIL-STD-883 Class B visual inspection for military applications.

Circle 502 on Inquiry Card



Multiplying DAC, 7541 from Beckman Instruments includes CMOS IC and R-2R ladder network. Converter provides 12-bit resolution and accuracy, as well as ± ½ LSB linearity

8k P/ROM Operates At High Speed

An 8192-bit programmable read only memory (P/ROM), the HM-7681A, provides a 50-ns max access time, a 1k x 8 organization, and 3-state outputs. Produced by Harris Semiconductor Products Division, PO Box 883, Melbourne, FL 32901, the bipolar P/ROM is contained in a 24-pin ceramic or epoxy dual inline package.

The memory is a fully decoded, high speed, Schottky TTL device. Manufactured, utilizing nichrome fuse technology, with all bits storing a logical 1, it features selective programming that can subsequently store a 0 in any 1-bit position.

This P/ROM contains test rows and columns in addition to the storage array, designed to assure high programmability and to guarantee parametric and ac performance. The fuses in these test rows and columns are blown prior to shipment. There are four chip enable inputs on the device. CE_1, CE_2 low and CE_3, CE_4 high enable the chip.

Circle 503 on Inquiry Card

ICs Generate Polynomials For Error Detection

Two polynomial generator/checker (PGC) circuits have been announced by Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086. One of these, the 9401, is a functionally identical, pin for pin compatible second source for the like numbered device from Fairchild Camera and Instrument. Like its counterpart, this circuit is programmable, operates at 12 MHz, and generates any one of the eight commonly used polynomials that calculate the cyclic redundancy check characters (CRCC) for error detection in serial data streams.

The second part to be introduced, the 8X01A, original with this manufacturer, does exactly the same PGC function but adds synchronous data link control (SDLC) protocol capability. For those users involved with SDLC, it provides a more efficient and less costly method of dealing with this bit oriented protocol, since it eliminates the extra circuits needed to implement SDLC with SSI/MSI devices.

Each of these circuits uses an identical error detection scheme, in which the remainder generated is added to a serial binary message. This checksum, or CRCC, is regenerated at the receiving point and compared with the CRCC appended to the message. Any difference indicates a transmission error.

Typical applications would be in word processing systems, terminals, floppy and rigid disc controllers, data concentrators and multiplexers, and communications controllers. Both of the devices provide TTL compatibility, operation from a single 5-V power supply, and packaging in a 14-pin DIP.

Circle 504 on Inquiry Card

Peripheral Circuits Provide Assortment Of Drivers and Switches

Fifteen peripheral linear integrated circuits from Texas Instruments Inc, PO Box 225012, Dallas, TX 75265, offer a wide variety of capabilities. These ICs include low power dual peripheral drivers, a low power quadruple NAND gate peripheral driver, quadruple high current drivers, and quadruple high voltage, high current darlington transistor switches.

The SN75446, SN75447, SN75448, and SN75449 are AND, NAND, OR, and NOR drivers, respectively and are low power dual peripheral drivers designed for use in systems requiring high current, high voltage, and fast switching times. They feature very low power requirements and low input current, offering 35-mW (typ) power dissipation from a single 5-V power supply. Capable of driving up to 400 mA, the drivers can switch up to 50 V and include PNP input gates to provide very low (1 μA, typ) input current. Additionally, they contain internal output clamp diodes, making them suitable for driving inductive loads. These circuits are available in either an 8-pin plastic (P-suffix) DIP or an 8-pin ceramic (JG-suffix) DIP.

Capable of switching up to 35 V, the SN75437 is a low power quadruple NAND gate peripheral driver. A unique single-saturated transistor output allows it to drive up to 700 mA, while standby power is 200 mW, typ. It contains internal output clamp diodes for driving inductive loads and features PNP input gates for a 1-μA typ input current. This circuit is available in a 2-W copper leadframe 16-pin plastic (NE-suffix) DIP.

The other ten circuits are second sources for circuits from Sprague Electric Co. Designed for such applications as dc motor drivers, discharge printers, and relay drivers, the UDN2841 and UDN2845 are quadruple high current drivers. Output collector current is 1.5 A, max. These ICs feature low input current and inputs compatible with TTL, DTL, and 5-V CMOS. Internal PNP level shifting allows use with negative load voltages. The UDN2481 sinks from a negative power supply, while the /45 has two sinks and two sources. Both devices are available in a 2-W copper leadframe 16-pin plastic (NE-suffix) DIP.

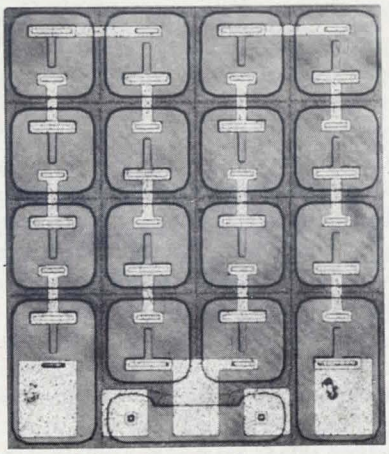
Finding applications in relay drivers, hammer drivers, lamp drivers, display drivers, line drivers, and logic buffers, the ULN2064, ULN2065, ULN2066, ULN2067, ULN2068, ULN2069, ULN2074, and ULN2075 are quadruple high voltage, high current (1.5 A, max) darlington transistor switches. This family can be divided into devices consisting of four NPN darlington pairs and others consisting of four NPN cascaded switches.

With regard to input characteristics, the family includes a subfamily using TTL, DTL, and 5-V MOS logic, another to be used with PMOS and CMOS logic, and a third used with TTL and 5-V CMOS. Additionally, two of the circuits feature uncommitted outputs for sink or source applications. All of the others feature high voltage outputs with common cathode output clamp diodes for switching inductive loads, using 35 to 50 V. Outputs and inputs may be paralleled for higher current capability. These devices are available in a copper leadframe 16-pin plastic (NE-suffix) DIP.

Circle 505 on Inquiry Card

Photovoltaic Chip Outputs 8 V

Using a dielectric isolation technique to fabricate a monolithic circuit, Dionics, Inc, 65 Rushmore St, Westbury, NY 11590, has developed a light sensitive diode array package with an output up to 8 V. Applications will include automatic test equipment, telephone switching equipment, data acquisition systems, industrial production systems, and a wide variety of computer controlled equipment in industry and telecommunications, areas where electromechanical and functionally limited solid state devices have been used for relay and switching circuits.



Photovoltaic generator IC chip, DI-16V8 from Dionics. Array consists of 16 diodes on 35- by 40-mil chip

One version of the diode array chip is incorporated in a solid state relay that is presently on the market. The chip is the DI-16V8, a 16-diode array photovoltaic generator chip measuring 35 x 40 mils. When illuminated by an LED, it delivers an output up to 8 V and 3 μA, controlling the gate of a MOSFET device and providing a center tap point which makes up to 4 V available.

With an LED chip, this microcircuit is an opto-isolated double diffused VMOS solid state relay, said to be the first of its kind.

The manufacturer notes that electronic control system designers have long needed a small inexpensive device that could respond rapidly to very low signals, yet produce sufficient voltages to operate switches and relays. However, it is believed that previous single IC chips comparable in size to the chip described above have been limited to a max output of approximately 0.5 V. Attempted solutions have failed to meet the goal for a variety of reasons, including insufficient response speed, multiple-chip designs that did not satisfy size requirements, and excessive costs.

Flexibility in circuit assembly of the photovoltaic chip arises from various factors. Since the bottom of the chip is dielectrically isolated, it can be placed on a common metallized area with other chips without danger of interaction, which is not true of other chips employing junction isolation. Also, the output voltage of the device is determined simply by the number of diodes connected in series on the chip. If it were needed, a center point pickoff could be included so that, as an example, a 16-V chip could have an 8-V pickoff or ± 8 V from a center point. Masks have been made for similar diode array chips that will offer increased voltage and current outputs.

Circle 506 on Inquiry Card

Integrated Circuit Varies Phase Control For Power Switching

An IC from Siemens Corp, 186 Wood Ave South, Iselin, NJ 08830, provides variable phase control for power switching devices as used in switch mode power supplies. This universally applicable circuit, TDA 4700, comprises digital and analog functions necessary for the design of high quality, blocking, single-ended and push-pull converters in normal, half-bridge, and full bridge circuits. In addition, this IC can also be used for capacitive voltage multipliers and speed controlled motors.

Operational amplifiers, which are integrated in the component, can detect errors in the electrical operation and initiate protective measures. Other features include component count reduction, ac line hum suppression, symmetric inputs for push-pull converters, dynamic output current limitation, output overvoltage protection, input undervoltage protection, and soft start capability. The two outputs are transistors with an open collector and work in a push-pull mode and are low active, featuring a typical output current of 15 mA. Oscillator frequency range is up to 250 kHz.

Circcle 507 on Inquiry Card

Line Receivers Meet Interface Specs

A family of monolithic 7- and 8-channel line receivers designed to meet I/O interface specifications for the IBM System 360 and 370 series CPUs has been announced by National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051. The 8-channel line receivers use a common strobe for each group of four receivers. One of these, DS75128, has an active high strobe, while the other, DS75129, has an active low strobe. The 7-channel devices are designated DS75125 and DS75127.

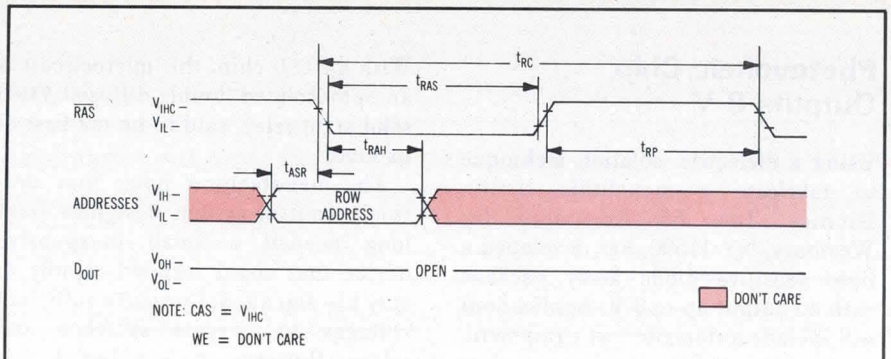
All of the receivers are built with a special low power design, utilizing Schottky diode clamped transistors. This results in low supply current requirements from a single 5-V supply, while maintaining fast switching speeds with TTL/74LS compatible outputs. Input resistance ranges from 7 to 20 kΩ.

128k Dynamic RAM Offers High Reliability

A row access time of 150 ns (max) and a failure rate of 0.3%/1000 h in the field characterize a 131,072-bit dynamic RAM from the Microproducts Division of General Automation, 14405 N Scottsdale Rd, Scottsdale, AZ 85254. This module, designated HMM 128KD, has served as the basis for the company's HYPAK high density minicomputer RAMs for the past two years. It is said to provide the highest system bit densities obtained by semiconductor technology.

Multiplexed address inputs and the use of multiple $\overline{RAS}$ inputs permit the memory to be packaged in a 28-pin dual inline configuration with an industry standard footprint. The provision of a separate $\overline{RAS}$ input for each pair of 16k RAM chips makes possible the external wiring option to obtain 32k x 4 or 64k x 2 configurations.

Additional features include a 320-ns max cycle time, internally connected power supply decoupling capacitors, and 10% tolerance on 12- and ±5-V supplies. Power dissipation, when the device is active, is 924 mW max for the 64k x 2 organization and 1848 mW max for the 32k x 4 organization. On standby, max dissipation is 160 mW.



Refresh cycle for General Automation's HMM 128KD dynamic RAM. Any operation in which $\overline{RAS}$ transits accomplishes refresh. Max refresh interval is 2 ms

The output buffer is 3-state TTL compatible with a fanout of two standard TTL loads. Data out is the same polarity as data in. The buffer can be powered via V_{CC} from the supply voltage (normally 5 V) to which the memory is interfaced. In standby operation, V_{CC} may be removed without affecting refresh. Thus, standby power is conserved because all the power supplies for peripheral circuitry with the exception of $\overline{RAS}$ timing and refresh addresses, are turned off.

Refresh of the dynamic RAM cells is accomplished by performing a memory cycle at each of the 128 row addresses at least every 2 ms. Any operation in which $\overline{RAS}$ transits accomplishes refresh; $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 128 row addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Maximum ratings require that voltage on any pin relative to V_{BB} remain between −0.5 and 20 V, and that voltage on V_{DD} and V_{CC} supplies relative to V_{SS} remain between −0.5 and 15 V. Power dissipation must not exceed 2.5 W.

Circle 508 on Inquiry Card

IC Provides Both Op Amp and Booster Operation

A thick film hybrid microcircuit device from Modular Devices, Inc, 50 Orville Dr, Airport International Plaza, Bohemia, NY 11716, combines the low input characteristics of an FET input operational amplifier and the high output capability of a booster or buffer amplifier. Input offset current to the model 2392 is 25 pA (typ), and the min rated output is ±10 V at 50 mA.

The device has a voltage gain of 100 dB, a small signal bandwidth of 10 mHz, and a full power bandwidth of 800 kHz. Other performance features include a slew rate of 40 V/μs (typ), internally trimmed offset voltage of 1 mV max at 25 °C, and a max voltage drift coefficient with temperature of 10 μV/°C.

This circuit finds use in such applications as accurate buffers, high speed integrators, current to voltage converters, sample/hold, and bridge circuits. It is provided in a 14-pin DIP and operates off a standard ±15-Vdc bipolar power supply.

Circle 509 on Inquiry Card

3-State 16k P/ROM And Power Saving SPROM Offer Fast Access Times

Two fast bipolar memories from Raytheon Semiconductor, 350 Ellis St, Mountain View, CA 94040, provide 16k of memory each, organized as 2k x 8. One of these, the 29681ADC, a 3-state P/ROM, has a max access time of 50 ns and an enable access time of 35 ns over the full commercial temperature range.

The other device is a 3-state SPROM, 29683ADC, offering a power savings of up to 70% when used in place of a conventional P/ROM. This type of programmable read only memory, evolved by this manufacturer, utilizes onchip power switches, which turn off most of the internal circuitry for an unselected device. Max access time for this circuit is 50 ns and enable time is 65 ns over the commercial temperature range.

Circle 510 on Inquiry Card

Monolithic Controller Accepts Wide Range Of Floppy Disc Drives

The HD46503 is a floppy disc controller designed to provide the interface between a microprocessor system and a floppy disc transport. Offered by Hitachi America, Ltd, 707 W Algonquin Rd, Arlington Heights, IL 60005, the chip is IBM 3740 compatible.

This controller's flexible hardware design enables it to be used in any microprocessor environment and is adaptable to a wide variety of disc drives. It uses ten macrocommands to control all head movements and read/write functions and features programmable seek and settling times, read/write operation of consecutive sectors by a single command, and both program controlled and DMA data transfer modes.

There are four read only registers on the chip, seven write only registers, and one read/write register. Data transfer speed is 4 μs/bit (32 μs/byte). Seek time is programmable from 1 to 15 ms and settling time from 4 to 60 ms. The device is implemented in n-channel, silicon gate, enhancement/depletion MOS technology, operates from a single 5-V power supply, and is packaged in a 40-pin DIP. As a member of the HMCS8600 family, it provides direct bus connection to elements of that family. □

Circle 511 on Inquiry Card

PRODUCT FEATURE

Dual Acoustic Coupler Provides Both 1200- and 0- to 300-Bit/s Full-Duplex Operation

Fully compatible with VA3400 and 103/113 type modems, the VA3413 is said to be the world's first dual acoustic coupler to provide both 1200- and 0- to 300-bit/s full-duplex asynchronous operation. Almost all originate applications for full-duplex data transmission at those baud rates over 2-wire switched networks can be satisfied by this portable unit from Racal-Vadic. Remote terminal users are now able to operate in Bell 103/113 mode (0 to 300 bits/s) but instantly step up to 1200 bits/s full-duplex using the same Bell 103 protocol.

Design Features

Under microprocessor control, this acoustic coupler simplifies operation by a scheme for automatic detection of the called modem. It is unnecessary for the user to manually select either VA3400 or 103 mode. Automatic 9- or 10-bit character length recognition in VA3400 mode allows the user to communicate with either IBM 9-bit or other 10-bit systems without physical changes to the modem.

Double-flange seals on the acoustic cups improve noise isolation. In addition, handset to microphone coupling virtually eliminates vibration problems

and assures performance with very low data error rates.

The unit includes microprocessor based CMOS components and crystal controlled oscillators. User diagnostics and displays with analog loopback, digital loopback, and transmit reversal are built in.

Specifications

Input data format is serial, binary, synchronous or asynchronous. Synchronous data rate is 1200 bits/s (3400 mode only). Asynchronous rate is 0 to 300 bits/s in 103 mode; and 1800 to 1205 or 1196 to 1219 bits/s and any standard data rates at 300 bits/s or below in 3400 mode.

Character length is 9 or 10 bits, automatic selection, in 3400 mode. Modulation is quadrature am (4-level PSK) in 3400 mode, binary phase coherent FSK in 103 mode.

Transmitter carrier frequencies are 2250 Hz in 3400 mode and 1270 Hz Mark, 1070 Hz Space in 103 mode. Line data rates are 1200, 1206.3, or 1220.12 bits/s, switch selectable, in 3400 mode, and equal to the transmit data input in 103 mode. Transmit level is −16 dBm. Receiver carrier frequencies are 1150 Hz in 3400 mode, 2225 Hz Mark and 2025 Hz Space in 103 mode.

Power requirements are 117 Vac ±10%, 47 to 63 Hz, 12 W max. Temperature ranges are 0 to 50 °C operating and −20 to 70 °C storage at 90% maximum relative humidity, without condensation. Dimensions are 4.25″ H x 8.5″ W x 14″ D (10.8 x 21.6 x 35.6 cm). Weight is 1 lb (454 g).

Price and Delivery

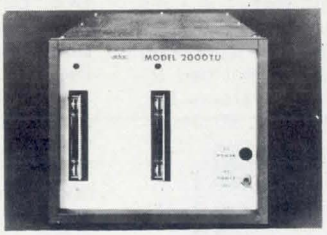
Single-unit price for the VA3413 dual acoustic coupler is $895; OEM discounts are available. Units are available through distributors. Racal-Vadic, 222 Caspian Dr, Sunnyvale, CA 94086. Telephone: 408/744-0810.

For additional information circle 199 on Inquiry Card.

PRODUCTS

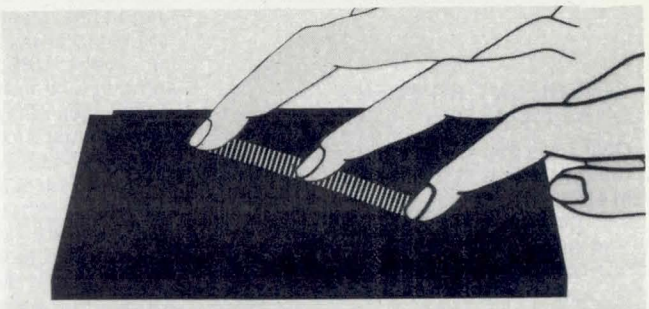
Cartridge Tape Drive Communicates with Computer via RS-232-C/-423 Serial Ports

Packaged in a chassis with an interface/control card and power supply, the model 2000TU tape drive is available in either 1- or 2-cartridge configuration. Communication between controller and host computer is accomplished via an RS-232-C/-422/-423 compatible serial I/O port in radial serial protocol format. Command and data byte sequences or packets have protocol information in specific locations in the byte sequence. The fixed length block, random access, mass storage system uses preformatted tape cartridges that store 262k bytes of data in two 256-block tracks. Receipt of a block number and word count from the host causes the controller to go directly to the specified block and start transferring data. Search speed is 60 in (152 cm)/s; R/W is 30 in (76 cm)/s. Typ access time is 9.3 s; max is 28 s. The interface operates on full-duplex, asynchronous, 4-wire lines at jumper selectable rates from 150 to 38.4k baud. An 8085 microprocessor is supported by firmware in a 2k-byte ROM and by scratchpad and data buffer in a 256-byte RAM. Drive motors are powered by servo-regulated speed and direction circuits that are controlled by the processor. The device is supported by the DEC TU58 handler and is available for all DEC supported hardware. **Adac Corp,** 70 Tower Office Park, Woburn, MA 01801.



Circle 200 on Inquiry Card

Finger Movement of Operator Over Surface of X-Y Controller Produces Positioning Signals

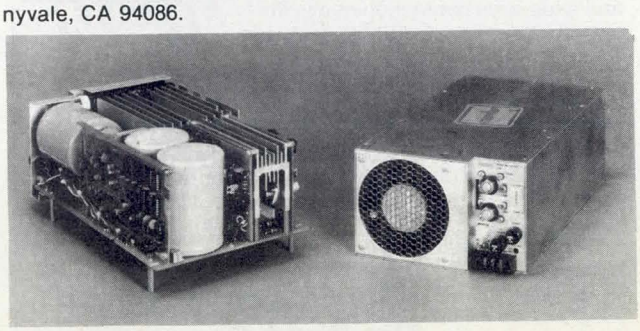


Motion of a fingertip on the surface of the Touch Graphic™ controller produces a train of pulses that serve as X-Y positioning signals. Seemingly a smooth surface across which the operator slides a fingertip in the direction in which positioning is desired, the device accepts movements at up to 60″ (152 cm)/s without loss of resolution. A simple software algorithm can be used to make the device rate sensitive so that a rapid finger motion will give large or coarse control while a slow motion will produce fine control. The 4 x 4″ (10- x 10-cm) positioner is made up of multilaminates and is rugged and chemically resistant. Since a strobe output signal indicates presence of a fingertip on the pad surface, when finger travel stops, the output signals also stop and the finger can be removed. Hybrid VLSI circuits and 3600 sensors activate in less than 1 ms. During fingertip motion, sensor circuits produce X-right and -left and Y-up and -down outputs. A solid state alternative to trackballs, thumbwheels, lightpens, and joysticks, this positioner can also be used as a controller for freehand graphics. It has no moving parts, is environmentally sealed, and is said to use 70% less space and provide up to 70% cost reduction (in OEM quantities) over other types of devices. **Touch Activated Switch Arrays, Inc,** 2346 Walsh Ave, Santa Clara, CA 95051.

Circle 201 on Inquiry Card

1.5-kW Switching Power Supply Is Housed in Standard 5 x 8″ Package

Model HL 1500, a 1.5-kW switching power supply, provides a higher power replacement for 750- and 1000-W supplies without need for extra space. The 5-V, 300-A unit fits into the same 5 x 8″ (12.7- x 20.3-cm) cabinet or rack slot as used by the lower powered packages, or two 750-W supplies can be replaced by one 1.5-kW supply, freeing a slot for other equipment. Power density is 2.5 W/in³ (0.15 W/cm³) at the nom 5 V and over 2.8 W/in³ (0.17 W/cm³) at 5.75 V (when needed to compensate for voltage drops in cables for remote operation). Efficiency is 82% at full load. Output voltage is controlled within 1% during a 25% load change and recovers to a flat output in 0.5 ms. Typ line regulation is 0.2%, load regulation is 0.3%. A 30-ms holdup masks ac line interruptions and brownout tolerance accepts line variations from 167 to 250 V. When supplies are paralleled, they automatically share load current within 5%, without user intervention. Up to 4 supplies linked by a control cable will share up to 1.2 kA automatically, for a 6-kW total power output. The supply operates with an air temperature rise of only 18 °C from intake to exhaust and can function safely at full output at ambient temperatures of 50 °C or at 1.2 kW at 70 °C. **Boschert, Inc,** 384 Santa Trinita Ave, Sunnyvale, CA 94086.



Circle 202 on Inquiry Card

PRODUCTS

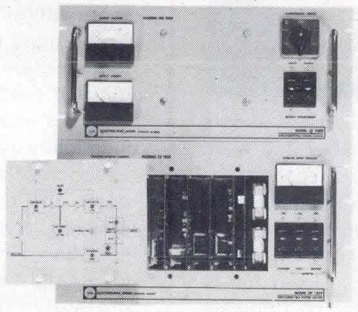
SEVERE ENVIRONMENT CORE MEMORY

Q25/MP, a 65k x 18 memory system, has full cycle time of 900 ns and is available in std planar package of 9.0 or 9.7 x 6.0 x 1.4″ (22.8 or 24.6 x 15.2 x 3.55 cm). It is also offered in a 130k x 9-bit configuration. Data guard, read-modify-write, and module decode options are offered. Fully compatible and interchangeable with the company's Q32/MP (32k x 18) and Q9/MP (16k x 18) it meets requirements of MIL-E-5400 Class 2 and is qualified to MIL-E-16400. Core storage array consists of 18 matrix arrays wired in a 3D, 3-wire configuration. Each matrix of 65,536 lithium ferrite (14-mil OD) cores is bonded to the aluminum plane to provide mechanical support and direct thermal conduction from cores to support structure. Half of bit arrays are mounted on each side of plane with continuous X- and Y-axis wiring through each. Max power consumption at −55 °C is 87.75 W, 72.6 W at 85 °C under normal 5-, −12-, and 15-V supply conditions. **Quadri Corp,** 1725 W Seventeenth St, Tempe, AZ 85282.

Circle 203 on Inquiry Card

120-Vac UPS

UP-100 MINI UPS provides 1 kVA of regulated, clean, uninterrupted 120-Vac power to critical loads. System consists of main UPS, bypass, and battery modules, mounted behind a 19″ (48-cm) relay rack panel. Front panel of unit shows operation of each subsystem by means of 8 LEDs. Removable front panel permits servicing of electronic components without removing unit from rack. Battery module provides 15 to 20 min of emergency operation at full load. Static switch automatically senses low UPS output voltage and transfers critical load to reserve line with less than 4 ms interruption; 3-position manual bypass switch provides means for bypassing UPS without interrupting critical load. **Instrumentation and Control Systems, Inc,** 520 Interstate Rd, Addison, IL 60101.



Circle 204 on Inquiry Card

MULTIPURPOSE NETWORK ANALYZER

Model 3100 is a portable microprocessor controlled complex vector computer that offers precise determination of each of two periodic waveforms and the characteristics of one to the other. Digital FFT analysis techniques used in the instrument provide high speed measurement response of the fundamental, total, and each harmonic to the 14th. A frequency range of 1 Hz to 500 kHz, and 12 voltage ranges from 1 mV to 300 V FS with accuracies of up to 0.1% and 0.03 deg are std. Twelve preprogrammed algorithms provide measurements of impedance, admittance, phase angle, real and imaginary quantities, pulsed phase, total, fundamental, harmonics, and harmonic power from CW, pulse, and burst mode inputs. **Dranetz Engineering Laboratories, Inc,** 2385 S Clinton Ave, South Plainfield, NJ 07080.

Circle 205 on Inquiry Card

16-BIT D-S CONVERTER

Converter DSC5116 is pin programmable for either 14- or 16-bit resolution with a ±0.05% transformation ratio. Accuracy is ±4 arc-min and output is 2 VA with power supply requirement of ±15 V. Short circuit and thermal overload protection are incorporated. Input is DTL/TTL/MOS compatible and transformer isolated output is compatible with any 3-wire synchro or 4-wire resolver. Available in commercial, military, and high reliability versions, unit's reference input can be either 26 Vrms or 115 Vrms at 60 or 400 Hz. **Natel Engineering Co, Inc,** 8954 Mason Ave, Canoga Park, CA 91306.

Circle 206 on Inquiry Card

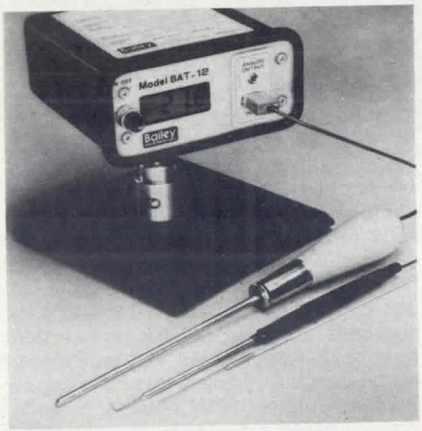
TAPE DRIVE EMBEDDED FORMATTER

TDX series II magnetic tape drives can use an embedded microprocessor based formatter to provide capacities of 800 bits/in NRZ, 1600 bits/in PE, or 800/1600-bit/in dual-density formats. Though designed for the 75-in/s TDX drive, interfaces for drive and computer are compatible with industry standards. Software also utilizes standard command structure. **TDX Peripherals,** 150 New York Ave, Halesite, NY 11743.

Circle 207 on Inquiry Card

HIGH STABILITY LABORATORY THERMOMETER

BAT-12 laboratory digital thermometer offers 0.1 °C resolution and accuracy of 0.08% ±1 digit over a −100 to 200 °C temp range. Negligible change in calibration is claimed for wide ambient temperature fluctuation. A 9-V battery typically provides several hundred hours of use for the device. Supplied with a camera-style carrying case for portable use, the unit can be used with optional tabletop stand, which provides an adjustable viewing angle. **Bailey Instruments, Inc,** 515 Victor St, Saddle Brook, NJ 07662.



Circle 208 on Inquiry Card

INTELLIGENT CONTROLLER FOR PRINTER

Magnum™-3400 permits the IBM 5256 printer on System/34 and /38 computers to be emulated by Printronix 150-, 300-, and 600-line/min printer/plotters. Two microcomputer systems on a single card fit into the controller slot inside the printer. Enhanced firmware on the controller generates variable size letters, 0.1 to 10″ (0.254 to 25.4 cm), and bar codes. Enhanced print capabilities include reverse imaging, variable aspect ratios, label repeat, and horizontal and vertical tabbing. **Quality Micro Systems, Inc,** PO Box 1644, Mobile, AL 36601.

Circle 209 on Inquiry Card

HIGH BRIGHTNESS LED INDICATOR

Using double-chip LED in an all metal threaded body, 2L702 indicator light produces typical ambient light viewing of 80 mcd at 100 mA. Transparent or translucent lens provides 180° visibility. Designed to operate at 5 V, lamps have 20-yr half life continuous operation. Termination is by wire leads or wirewrap posts suitable for soldering. Lamps are available in red, green, and amber. **The Sloan Co,** PO Box 367, 7704 San Fernando Rd, Sun Valley, CA 91352.

Circle 210 on Inquiry Card

PRODUCTS

PROGRAMMING STATION FOR MEMORY BOARD TESTER

Standalone station MD-247, used with the MD-207/11 memory board tester, allows offline program development concurrent with production work. Test control language (TECOL) executive, TECOL editor, DEC RT-11 operating system, and utilities are included in the LSI-11 based system. The station consists of the microcomputer, with 32k bytes of memory and a VT-100 CRT terminal. Options include dual cassette tape transports and TI Model 810 150-char/s printer. **Eaton Macrodata,** 21135 Erwin St, Woodland Hills, CA 91365.
Circle 211 on Inquiry Card

HIGH SPEED PDP-11/70 MASS MEMORY SYSTEM

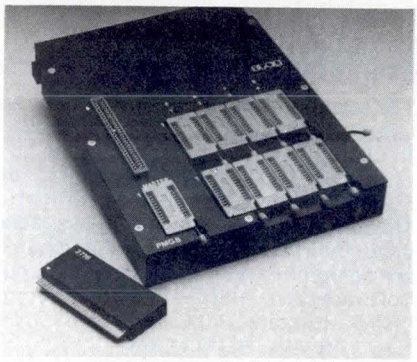
Attached directly to the cache bus of PDP-11/70 computers, Maxiram-11/70HS solid state nonrotating equivalent of RS04/RS03 fixed head disc drives is said to achieve up to 50% throughput increase while reducing traffic on the Unibus. The system comprises a high speed controller placed in one of the RH70 locations in the processor plus a 19″ (48.3-cm) rackmounted chassis containing the solid state RAM. Capacities from 512k to 8M bytes can be attached to the controller. **Imperial Technology, Inc,** 831 S Douglas St, El Segundo, CA 90245.
Circle 212 on Inquiry Card

BRUSHLESS DC MOTOR

Continuous duty 173-W output at 3600 r/min is provided by a brushless dc motor utilizing printed circuit stator winding and 8-pole ferrite magnet rotor. Features include rapid acceleration to a set speed, dynamic braking, and speed regulation of ±1% from 500 to 5000 r/min. Start/stop command capability and digital velocity signal for feedback purposes are available for remote control applications. NEMA 42C face mount is standard; an 80-V, 8-A dc power supply is also available. **PMI Motors,** 5 Aerial Way, Syosset, NY 11791.
Circle 213 on Inquiry Card

8-POSITION EPROM PROGRAMMER

Gang programmer PMG-8 will operate with any company programmer mainframe, PPX, PP-19, and PP-17 and program most popular EPROM devices by plugging in the appropriate unit to characterize the programmer and module for any of these devices. Built-in display and keyboard provide editing capability. Data can be downloaded via paper tape reader or RS-232-C interface and output to paper tape punch or printer. Self-test allows checking for faulty or improperly inserted devices. Special empty check tests parts for proper erasure. **Stag Systems Inc,** Palo Alto Industrial Park, 1120 San Antonio Rd, Palo Alto, CA 94303.



Circle 214 on Inquiry Card

THICK FILM CHIP RESISTORS

IMS-7 thick film chip resistors replace resistors in the 0.030 to 0.040″ (0.076 to 0.10-cm) range and offer resistances from 1 Ω to megohms with ±1% tolerances. The 0.025 x 0.030″ (0.064 x 0.076-cm) devices have a free air dissipation of 30 mW at 25 °C. Sixteen other chip sizes can be provided. Elongated gold terminations permit multiple wire bonds to a single device. Produced on a 0.010″ (0.0254-cm) 96% alumina substrate, the passivated devices also are available with backside metallization. **International Manufacturing Services, Inc,** 50 Schoolhouse Ln, Portsmouth, RI 02871.

Circle 215 on Inquiry Card

2.54-mm FLAT CABLE

Introduction of 2.54-mm cable extends the Jet Flecs™ flat cable line that also includes 1.27- and 3.96-mm types. Available in AWG 22 and 28 stranded and AWG 26 solid, the cables are UL listed at 105 °C and 300 V max and are rated FR-1 for flammability. Designed to mate with the IDT™ header connector system and compatible insulation displacement systems, the gray cable contains a first circuit color key marker and can be separated by zipping. **Molex, Inc,** 2222 Wellington Ct, Lisle, IL 60532.

Circle 216 on Inquiry Card

BLACK BOX INTELLIGENCE FOR DUMB TERMINALS

A self-contained Smarts Box™ computer based on DEC's LSI-11/2 processor provides intelligence for nonintelligent terminals. The 5.5 x 8 x 11.75″ (13.9 x 20.3 x 29.8-cm) unit weighs only 8 lb (3.6 kg) and can be provided with mounting hardware for tabletop or fixed position use. Alternatively, the portable unit can be moved from job to job. All power supplies, cooling fans, interface, and memory for standalone operation are included in the device along with LSI-11/2 processor board, two independent RS-232-C interfaces, 8k bytes of RAM (optionally expandable to 32k bytes), space for 8k bytes of ROM, 60-Hz crystal clock, and 2 vacant Q-bus compatible card slots to accommodate specialized cards. **North Atlantic Industries, Inc,** 60 Plant Ave, Hauppauge, NY 11787.

Circle 217 on Inquiry Card

SMALL 12-V GEL-TYPE BATTERY

Maintenance free and usable in any position, PS-1212 sealed rechargeable gel-type battery has a capacity of 1.2 Ah. It weighs 1.25 lb (0.56 kg), has an op temp range of −4 to 140 °F (−20 to 60 °C), and allows discharge currents of up to 40 A. Life expectancy is up to 5 yr. The battery was designed for such standby applications as electronic memory protection, UPS and telecommunications systems, and portable power. **Power-Sonic Corp,** PO Box 5242, 3106 Spring St, Redwood City, CA 94063.

Circle 218 on Inquiry Card

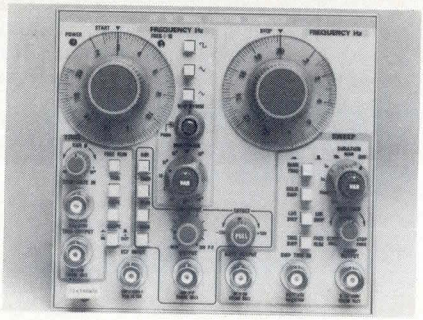
125-VA D-S CONVERTERS

Suited to driving heavy torque receiver loads or control transformers, 192A650 series D-S converters feature automatic disabling or outputs on overloads of more than 3 s and automatic recovery when overload is removed. Locked rotor caused by 180° input steps is prevented, and thermal shutdown is provided. 12-bit natural binary angle data stored in input registers are converted into 3-wire synchro information. Worst case accuracy is ±21 min of arc for torque receiver, and ±10 min for control transformer loads. **Control Sciences, Inc,** 8399 Topanga Canyon Blvd, Canoga Park, CA 91304.

Circle 219 on Inquiry Card

2-MHz FUNCTION GENERATORS

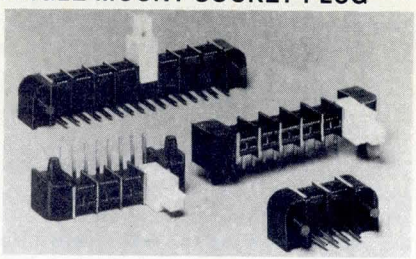
Log and linear sweep capabilities of FG 507 sweeping function generator adapt the TM 500 plug-in to use in applications requiring low distortion and versatile



sweep capabilities. Log sweep is mathematically derived and allows accurate frequency plots when using log scales, log paper, or a storage oscilloscope. Separate start and stop frequency dials make settings easy to set and interpret. A third frequency control allows manual sweep between preset start and stop frequencies. The FG 501A function generator has no sweep. Replacing the FG 501, the unit features increased frequency, output voltage, and offset as well as output step attenuator, variable symmetry, and trigger mode. Both units provide low distortion outputs from 0.002 Hz to 2 MHz and are capable of generating sine, square, triangle, ramp, and pulse waveforms. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.

Circle 220 on Inquiry Card

LOW PROFILE RIGHT ANGLE MOUNT SOCKET PLUG



Considerable cost savings over DIP switch utilization is said to be realized through use of switches consisting of an SWS switch socket and SWP switch plug. Where it is intended that a desired signal pass through a circuit, whether programming or on/off functions, a plug is inserted into the socket; circuit changes are made by changing plug locations within each socket. **Robinson-Nugent, Inc,** 800 E 8th St, New Albany, IN 47150.

Circle 221 on Inquiry Card

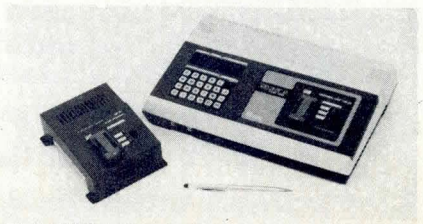
128k x 21-BIT NOVA ADD-IN MEMORY

Single-card add-in memory MK8018 for Data General's NOVA 4 computer has onboard error correction and 8-LED error log for onboard RAM level troubleshooting. The card implements 4-way interleaved timing compatible with NOVA 4/X or 4/S and can be used alone or with other memory cards in either 5- or 16-slot chassis. Capacity is 128k 16- or 21-bit words. Write access is 200 ns and read cycle 400 ns. Dimensions are 15 x 15 x 0.56″ (38 x 38 x 1.4 cm). **Mostek Corp,** 1215 W Crosby Rd, Carrollton, TX 75006.

Circle 235 on Inquiry Card

PORTABLE UNIVERSAL P/ROM PROGRAMMER

Universal programmer PKW-7000, developed by Toyo Telesonics Co, Ltd, incorporates 8085 CPU, RAM capacity expandable from 2.25k bytes and is suited to programming 4k- to 64k-bit EPROMs, bipolars, CMOS, 1-chip CPUs, as well as future devices. Unit is mainframe with several universal pluggable modules depending on types to be programmed. Design features include voltage margin, data sum, and self- and error-checks. Dimensions are 290 x 190 x 65 mm and weight is 1.8 kg. It is marketed worldwide outside Japan by **Intertek, Inc,** 7-2-8, Nishi-Shinjuku, Shinjuku-ku, Tokyo, 160, Japan.



Circle 223 on Inquiry Card

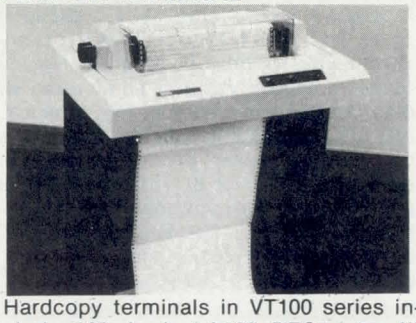
PRODUCTS

SINGLE-BOARD TAPE CONTROLLER

Encoded and NRZ formats are combined on a single PC board in the TC-131 universal magnetic tape controller designed for use with Digital Equipment Corp's PDP-11 series computers. Contained on a single hex-size PC board that plugs into a standard SPC slot in the computer, the controller requires no special backplane board. In addition to the convenience of both PE and NRZ formats, the unit can mix 9-track NRZ, PE, or dual-density tape units in any combination of up to 8 units. All filtering is switch-selectable, and a built-in self-test LED indicates when an error is present. Other features include a 33-word buffer and automatic nonstop operation when doing consecutive read/write operations. Available separately or as a complete system, the unit allows full size 2400′ (731 m) tape reels to be handled and can accommodate IBM and DEC byte packing and VRC, LRC, and CRC checking. It allows users to edit previously recorded records. **Western Peripherals, Div of Wespercorp,** 14321 Myford Rd, Tustin, CA 92680.

Circle 224 on Inquiry Card

BIDIRECTIONAL RECEIVE-ONLY PRINTER TERMINAL



Hardcopy terminals in VT100 series include 180-char/s LA120 DECprinter III and enhanced version of LA34 DECwriter IV. A receive-only version of the LA120, DECprinter III is a bidirectional printing terminal with logic moving printhead to margin closest to its position after it completes a line. It prints 180-char/s, with each character formed from a 7 x 7 dot matrix. It has a 1k-char buffer and logic that permits it to skip over areas not requiring printing, and it accepts data at rates to 9600 baud. LA34-AA is a 30-char/s terminal that prints characters from 9 x 7 dot matrix and has a 160-char buffer. Character sizes are adjustable from 5 to 16.5/in (1.9 to 6.5/cm). The unit incorporates keyboard selectable local echo, parity, and last character visible features. **Digital Equipment Corp,** Maynard, MA 01754.

Circle 225 on Inquiry Card

BAR CODE INTERFACE FOR SYSTEM/34 AND /38

Intermec 9230 interface unit allows a bar code reader to connect directly to an IBM System/34 or /38 through a 5251 terminal. The interface, installed between the 5251 CRT display and its keyboard, receives data from a bar code reader or other asynchronous serial ASCII device via RS-232-C leads at switch selectable rates from 150 to 9600 baud. A 1k-char internal buffer is provided. Data are output to the 5251 at an avg rate of 20 char/s and appear to the computer as keystroke data from the terminal. **Interface Mechanisms, Inc,** PO Box N, Lynnwood, WA 98036.

Circle 226 on Inquiry Card

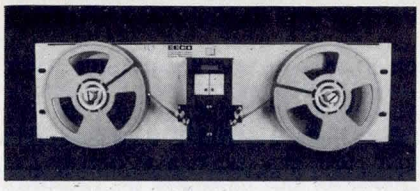
FACE WIPE SOCKET

707 series face wipe sockets available in 8- to 40-pin sizes incorporate CA-725 alloy contacts with either gold or tin inlay on contact area. They are provided in packaging compatible with major automatic insertion equipment. Sockets are oriented by polarization identification and have tapered leads. Tapered entry holes facilitate IC insertion and alignment of IC leads to socket contacts. Series meets or exceeds all EIA RS-415 stds. **Scanbe Div Zero Corp,** 3445 Fletcher Ave, El Monte, CA 91731.

Circle 227 on Inquiry Card

PRODUCTS

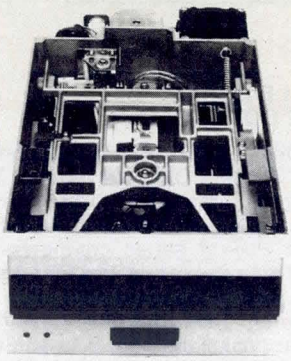
200/300-CHAR/s TAPE READER



Said to be the first tape reader with this performance capability, the dual-speed Model 80 is available at a 200-char/s price. Designed for rugged industrial environments, reliability is improved by fewer moving parts and elimination of electrical and mechanical adjustments. It is fully compatible with the company's commercial tape products and is available in 5.25 or 8″ (13.3 or 20.3-cm) panel heights with optional RS-232 interface. **EECO Inc,** 1601 E Chestnut Ave, Santa Ana, CA 92701.

Circle 228 on Inquiry Card

DOUBLE-SIDED, DOUBLE-DENSITY FLEXIBLE DISC DRIVE

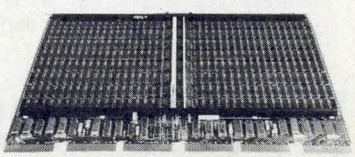


Air damped head loading system of 8″ (20.3-cm) FD1160 Soft Touch drive increases media life to more than 6M passes. Design of the drive results in MTBF rating of 15,000 power-on hours. The double-sided, double-density drive has formatted capacity of 1.2M bytes and unformatted capacity of up to 1.6M bytes with max track to track access time of 5 ms and is electronically and dimensionally compatible with industry std single- and dual-density 8″ drives. Steel band carriage driven by stepper motor provides accurate head positioning and rapid seek time. Other features include front panel ready and busy indicators, write protect detection, and mechanical interlock that ensures proper disc insertion. **NEC Information Systems, Inc,** 5 Militia Dr, Lexington, MA 02173.

Circle 229 on Inquiry Card

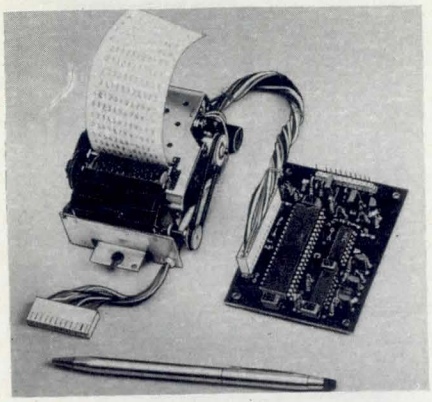
512k-BYTE SEMICONDUCTOR ADD-IN MEMORY FOR VAX

Single-board DR-178S offers twice the storage capacity of DEC's compatible 256k-byte M8210. Using 16k dynamic RAMs, the memory is internally organized as 64k x 72. The 72-bit word consists of two 32-bit words plus 8 bits of error correcting code. Timing is governed by the M8213 memory controller in the VAX-11/780. Typ access and cycle times in read mode are 250 ns and 530 ns, respectively. Operating from the host's 5-, −5-, and 12-Vdc power supplies, max current drains are 0.58, 0.02, and 1.45 A, respectively. A DIP switch allows the board to be isolated from the bus during troubleshooting. Two LED indicators mount at the rear edge; one indicates that memory is being accessed, the other whether or not the memory is switch disabled. **Dataram Corp,** Princeton-Hightstown Rd, Cranbury, NJ 08512.



Circle 230 on Inquiry Card

SMALL DIRECT IMPACT DIGITAL PRINTERS



Intended for applications with severe space restrictions, the series MP-2000 printers measure 1.5 x 2.75 x 3.94″ (3.81 x 6.96 x 10.0 cm) and provide numerical print capability at 2 lines/s, 13 char/line, in a 12-column configuration. Char size is 0.10 x 0.05″ (0.254 x 0.127 cm) and paper is 1.5″ (3.81 cm) wide. Complete interface PCB is 1.2 x 2.8 x 4.4″ (3.05 x 7.11 x 11.8 cm) and data input signal requirements are 4-bit BCD positive parallel logic code at TTL level. **International Technology Resources Corp,** One World Trade Center, Suite 3451, New York, NY 10048.

Circle 231 on Inquiry Card

CERAMIC TRIMMER CAPACITORS

Available in substrate mounting and PCB mounting variations, the capacitors range in size from 5 mm in dia and 2 mm thick to 3 mm in dia and 1.5 mm thick and are suited for hybrid circuit applications. Capacitance ranges are from 0.5 to 2.0 pF up to 5.0 to 35.0 pF. High Q designs can be used in UHF and GHz configurations. **Sprague-Goodman Electronics, Inc,** 134 Fulton Ave, Garden City Pk, NY 11040.

Circle 232 on Inquiry Card

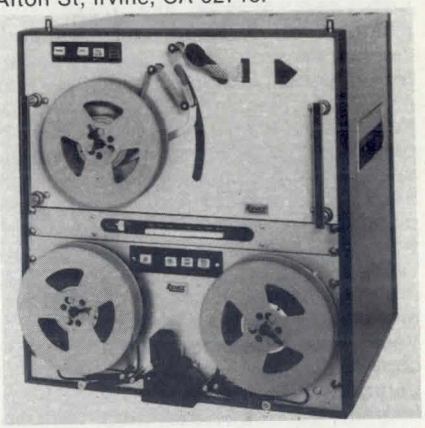
DUAL-TRACK FLOPPY DISC HEAD

Intended for use on 5.25″ (13.34-cm) diskettes, the head provides a max write density of 2768 bits/in with resolution of 125 kHz/62.5 kHz, 95% max, 45% min. Write track radii are 57.15 mm (track 00) and 36.5 mm (track 39). Resonant frequency for read/write is 500 kHz min; read/write inductance is 1.4 ±0.4 mH; erase is 25 μH max. Dc resistance read/write is 16 Ω max, erase 3 Ω max. Write current is 8 mA pk-pk and read output is 13 mV pk-pk max and 2 mV pk-pk min, while tunnel erase current is 80 mA dc. **Canon USA, Inc, Electronic Components Div,** 10 Nevada Dr, Lake Success, NY 11042.

Circle 233 on Inquiry Card

PROGRAM GENERATION STATION

Systems designers can use RMA0026 enclosure kit to configure a compact program generation station in such applications as numerical control and computer programming. High speed reader/spooler, punch, and RS-232-C or duplicator interface can be integrated into a single package which can be mounted on a rolling station for manufacturing floor use. Kit accepts either 6000 or 7000 series readers. Perforators for the station are available in 120- or 75-char/s models for 5- and 8-level paper or mylar tape. **Remex,** PO Box C-19533, 1733 Alton St, Irvine, CA 92713.



Circle 234 on Inquiry Card

PRODUCTS

GRAPHICS CAPABILITY FOR VT-100 TERMINALS

Graphics-100, an add-in for DEC VT-100 or VT-103 terminals, offers X-Y graphics display capability. The PCB fits into the terminals' option slot and provides 1220 x 240-dot resolution on the 8 x 4.5″ (20.3 x 11.4-cm) screen. Normal terminal functions are separate and remain unchanged. The board provides a separate display memory along with extensive text and graph labeling capabilities. Text includes 4 character sets, 3 text rotations for labeling, and 3 type fonts. A built-in vector generator allows users to specify line endpoints anywhere in the 64k x 64k addressable area. The unit then computes the line and displays that section which lies within the designated viewing window. The viewing window may be moved programmatically anywhere within the addressable space. Vectors may also be magnified. Hardcopy is available from the DECwriter II using the company's Graphics II upgrade feature. **Selanar Corp,** 2403 De La Cruz Blvd, Santa Clara, CA 95050.
Circle 236 on Inquiry Card

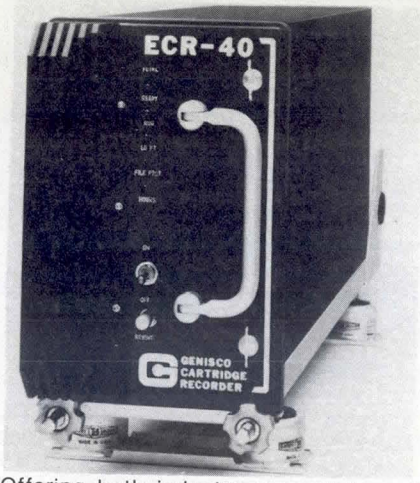
STANDALONE SPEECH OUTPUT TERMINAL

Designed specifically for use by the blind, Orator interfaces to any RS-232-C port and enables a host computer to speak with full word or spelled speech capabilities. Synthesized speech offers unlimited vocabulary and special commands permit specification of speech parameters for individual tasks. User options included are choice of aural punctuation and/or capitalization and input or output speech monitoring. **Arts Computer Products, Inc,** 80 Boylston St, Suite 1260, Boston, MA 02116.
Circle 237 on Inquiry Card

INTELLIGENT DAISYWHEEL PRINTER INTERFACE

Daisy Brain DB2000 features include proportional spacing, high resolution graphic plotting, automatic justification, and bold char printing. Z80 microprocessor and 3k-byte memory reduce CPU overhead. The intelligent RS-232-C interface installs into all major daisywheel printers with no additional power supply required. Communication speeds are up to 9600 baud. Interface is compatible with any host or terminal with an asynchronous RS-232-C serial port. **Wilker, Inc,** 3459 La Mesa Dr, Hayward, CA 94542.
Circle 238 on Inquiry Card

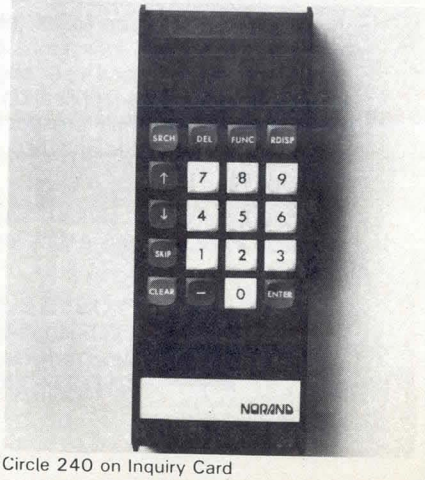
MILITARY CARTRIDGE TAPE RECORDER



Offering both industry compatible and airborne 1553 interface, ECR-40 environmentalized military recorder uses ruggedized 0.5″ (1.27-cm) cartridge for full emulation of 125″ (49.2-cm)/s reel to reel recorders. It uses 9-track parallel phase encoded data at 6400 bytes/in (2520 bytes/cm). Data rate is 200k bytes/s; shuttle speeds are up to 240 in/s (95 cm/s) with a single cartridge capacity of 48M bytes. Dimensions are 5 x 8 x 19″ (12.7 x 20.3 x 48.3 cm), and weight is under 40 lb (18 kg). Power requirement is 85 W nom. **Genisco Technology, Systems Div,** 18435 Susana Rd, Compton, CA 90221. Circle 239 on Inquiry Card

PORTABLE TERMINAL WITH 16k x 8-BIT MEMORY

Measuring 1.5 x 3.3 x 8.75″ (3.81 x 8.38 x 22.22 cm) and weighing 1.75 lb (0.79 kg), the 101XL™ terminal is used to telecommunicate data it acquires to a mainframe computer. Complementing 64k bytes of data storage, the original 12k bytes of program storage has been increased to 16k bytes, permitting larger applications programs. Featuring an alphanumeric display, the terminal records data, counts items, and performs calculations and can be used for inventory processing. **Norand Corp,** 550 Second St, SE, Cedar Rapids, IA 52401.



Circle 240 on Inquiry Card

HIGH SPEED MAGNETIC TAPE PROCESSOR

Major feature of tape processor subsystem is ability to support 125-in (317-cm)/s tri-density magnetic tape drives with 800-, 1600-, and 6250-bit/in (314, 629, and 2460/cm) recording in NRZI, PE, and GCR formats. Command and data chaining and error correction are also std features. In GCR format 1 or 2 track errors are corrected. Autoload provides self load of tape by touch of button after tape is mounted; density selection permits operator to choose tape density by means of switches; and mix 'n match allows up to 4 tape drives to be supported by either the tri- or dual-density subsystem. Although the formatter provided with the dual-density subsystem can support only dual-density drives, the formatter supplied with the tri-density subsystem can support both dual- and tri-density tape drives. **Systems Engineering Labs,** 6901 W Sunrise Blvd, Fort Lauderdale, FL 33313.

Circle 241 on Inquiry Card

POCKET SIZED MICROCOMPUTER

TRS-80 pocket computer has 24-char LCD display, English language prompting, and BASIC programming. A 1.9k RAM retains data for the 300-h life of the internal batteries. Computer weighs 6 oz (168 g) and is less than 7″ (17.8 cm) long. Preprogrammed tapes include real estate, civil engineering, personal finance, aviation, math drill, and a games pack. Unit can also be used as a calculator; numbers may be edited, stored, reviewed, and placed in equations with up to 15 levels of parentheses. **Tandy Corp/Radio Shack,** 1800 One Tandy Ctr, Forth Worth, TX 76102.

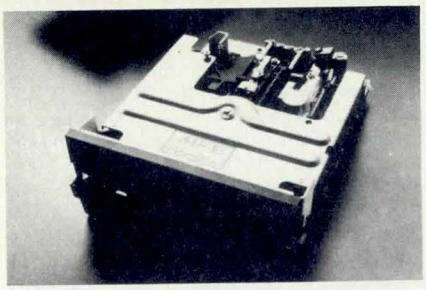
Circle 242 on Inquiry Card

TOUCH SENSITIVE CRT TERMINAL

Divided into multiple transparent capacitor touch pads that eliminate need of a keyboard, the Public Access Terminal is designed for unattended use. All switches, adjustments, and cable connections are inaccessible; power and maintenance modes are key operated. The Z80 based terminal uses a 15″ (38.1-cm) CRT and 10 x 14 dot matrix with full u/lc ASCII char set and user specified fonts of up to 240 chars. Keyboards and bar code scanners are optional. **Interaction Systems, Inc,** 24 Munroe St, Newtonville, MA 02160.

Circle 243 on Inquiry Card

SINGLE-SIDED FLEXIBLE DISC UNIT



Circle 244 on Inquiry Card

Heliband™ head positioning system guarantees 3-ms track to track access time for the 500 series drive. Weighing less than 10 lb (4.54 kg), the drive includes a reduction in head load force for longer media wear. A special mechanism prevents diskette damage produced by improper insertion. Said to be the smallest and most compact drive with standard industry compatible mountings, the drive includes a wide range of factory or user installed options and employs double-sided technology features. **MFE Corp,** Keewaydin Dr, Salem, NH 03079.

PRODUCTS

675M-BYTE OEM DISC MODULE

Fixed module drive (FMD) model 9775 offers data interface compatibility with the company's industry standard storage module drives and provides more than twice the max data storage capacity previously available in a single SMD drive. It operates at a 1.2M-byte/s data transfer rate. Its microprocessor controlled servo system reduces product cost and increases reliability. Drive unit includes a fixed sealed data module head disc assembly, drive motor and brake, and filtered air circulation system. A logic chassis provides all electronics for read/write, I/O, and drive operations, including servo electronics. A second microprocessor provides self-test and diagnostics. Data are recorded at density of 6495 bits/in (2557/cm) with density of 662 tracks/in (260/cm). Avg access time is 25 ms. Optional features include 1.9M bytes of fixed head/track storage for fast access, and a dual-channel capability that provides 2-controller access to the drive unit. **Control Data Corp,** Box O, Minneapolis, MN 55440.

Circle 245 on Inquiry Card

FLAT CABLE CONNECTORS

No stripping is required with FCN 750 miniature DIP series flat cable connectors. Designed to connect flat cable to PCBs by dip soldering, the series replaces headers without PCB redesign, using construction similar to PCB transition connectors (paddle card) but having the same footprint as a 0.1 x 0.1″ (0.254 x 0.254-cm) header. Mass termination is provided for AWG 28 stranded and AWG 30 solid flat cable. The connectors are part of the FCN 700 series. **Fujitsu America, Inc, Component Sales Div,** 910 Sherwood Dr-23, Lake Bluff, IL 60044.

Circle 246 on Inquiry Card

UNIVERSAL COMMUNICATIONS INTERFACE

Supporting a wide selection of communications protocols, the MCS-40 microprocessor based controller also includes Centronics or Dataproducts parallel interface. Designed for the Teletype model 40 printer mechanism, the board efficiently utilizes a large buffer memory to increase performance. Power-on and operator initiated diagnostics isolate printer failures to print position and controller errors to chip level. Total hardware and software transparency is provided. **Innovative Electronics, Inc,** 15200 NW 60 Ave, Miami Lakes, FL 33014.

Circle 247 on Inquiry Card

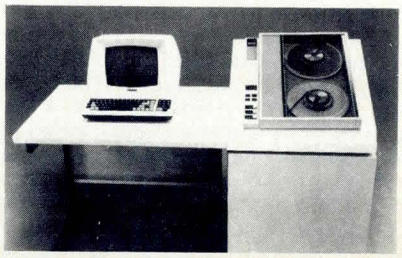
PORTABLE INSTRUMENTATION RECORDER

Lightweight model 6300 increases tape handling convenience, versatility, and reliability by providing pushbutton control of functions. A 4-digit LED display presents either tape speed or tape used counts in English or metric. The 0.25″ (0.635-cm) unit offers 16 h of continuous recording in either 4- or 8-track configurations with ac or dc power. Plug-in function modules provide a variety of recording modes and speeds. Decade speeds of 92.25, 9.525, and 0.925 cm/s and 7 IRIG speeds from 76.2 through 1.1906 cm/s are provided. Capstans and capstan servo control systems provide precise tape handling with significantly reduced mechanical component noise. Improved noise suppression permits more accurate reproduction of critical signals in the FM record/reproduce mode. **Precision Data, Inc,** 2370 Charleston Rd, Mountain View, CA 94043.

Circle 248 on Inquiry Card

PLOTTING WORK STATION

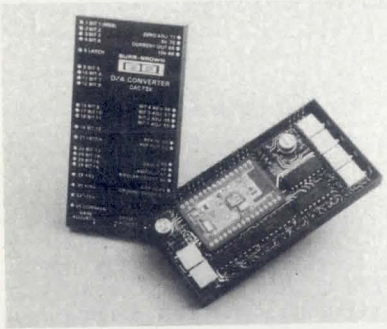
Work station 430, working directly from unsorted CalComp 921/925 mag tapes, sorts, rasterizes, and controls electrostatic plotting for a claimed throughput improvement of 10 to 1. Components include microprocessor with 64k-byte memory, 24.8M-byte Winchester disc, CRT display, dual-density mag tape drive with imbedded formatter, and bipolar algorithmic processor for sorting and vector to raster conversion. System drives two plotters, which need not be of same width, in plotting widths from 11 to 72″ (6 to 183 cm). **Versatec, a Xerox Co,** 2805 Bowers Ave, Santa Clara, CA 95051.



Circle 249 on Inquiry Card

±0.00075% FSR, 16-BIT DAC

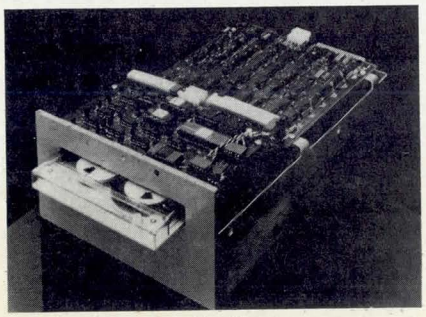
DAC 73 delivers performance and resolution (1:65,536) required for ultraprecision, wide dynamic range instrumentation. Design concepts reduce total component count by 50% compared to traditional 16-bit DACs. Critical components including current steering switches, temperature compensated zener reference, and laser trimmed thin-film resistor network are contained in single ceramic hybrid IC package mounted inside the module. Also included in the 2 x 4 x 0.4″ (50.8 x 101.6 x 10.16 mm) package are potentiometers for gain, offset, and linearity calibration; high accuracy output amplifier; and input storage register. Output ranges of 0 to 10, ±5, and ±10 V can be selected and ground sense output pin provides 16-bit accuracy at load. **Burr-Brown, Data Conversion Products,** PO Box 11400, Tucson, AZ 85734.



Circle 250 on Inquiry Card

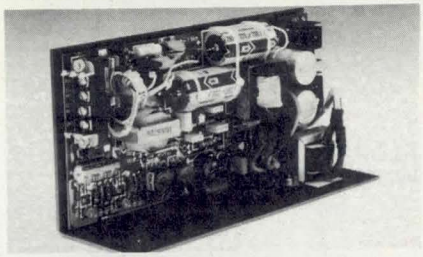
STREAMING 0.25″ CARTRIDGE TAPE DRIVES

Sidewinder family of streaming 0.25″ (0.64-cm) drives have 8k-bit/in (3150-bit/cm) recording density and speeds of 30 and 90 in/s (76 and 229 cm/s). Designed for Winchester drive backup, the drives use ANSI std 450-ft (137-m) cartridge and come in either Basic or Intelligent configuration with 10M- or 20M-byte capacities. Erase-write-read head operates in 2- or 4-track format, recording serially one track at a time using serpentine technique. Precision stepper motor positions head accurately on proper track. **Archive Corp,** 3540 Cadillac Ave, Cost Mesa, CA 92626.



Circle 251 on Inquiry Card

150-W SWITCHING POWER SUPPLIES

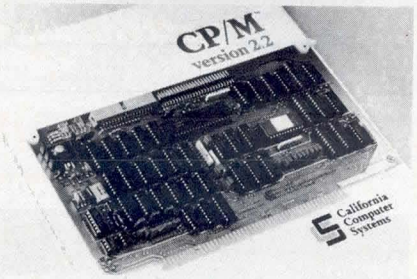


Single-output switching regulated dc power supply series SWS 150 comes in 5 models rated at 150 W that provide 5 V at 30 A, 12 V at 12.5 A, 15 V at 10 A, 24 V at 6.5 A, and 28 V at 5.5 A. Open frame series offers continuous operation, 115/230-Vac single phase input, and 75% efficiency. Features include overvoltage protection, logic shutdown and/or inhibit, power fail alarms, and factory burn-in. **Standard Power, Inc,** 1400 S Village Way, Santa Ana, CA 92705.

Circle 252 on Inquiry Card

PRODUCTS

FLOPPY DISC CONTROLLER WITH CP/M SOFTWARE



Both 5.25 and 8" (13.33 and 20.3 cm) single- or double-sided drives in any combination of up to 4 drives are supported by the 2422 controller for S-100 systems. Based on Western Digital's 1793 disc controller chip, it supports both IBM 3740 single-density and IBM System/34 double-density soft sectored diskette formats. An onboard 2k EPROM supplies monitor firmware and a bootstrap ladder for loading CP/M from disc. Autoboot gives users a choice of having CP/M loaded on power-on and reset or under the monitor boot command. The bootstrap loader and monitor are disabled when CP/M is loaded, and LED indicates whether they are enabled or disabled. Additional features include software enabled auto wait on either data register or board status register. **California Computer Systems,** 250 Caribbean Dr, Sunnyvale, CA 94086.

Circle 253 on Inquiry Card

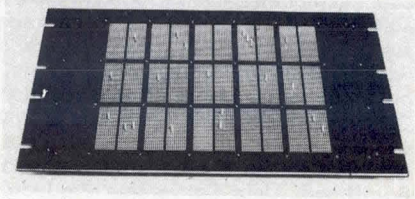
DIGITAL IC LOGIC PROBES

Model 3300A has 50-ns min pulse width detection, 10-MHz frequency response, and switch selectable threshold level (DDT/TTL and HTL/CMOS). Pulse stretchers can detect single or multiple pulses (active 0.33 s). Input impedance is 150 kΩ with input overload and probe power protection. Universal logic probe DPL-1 has 1.5-MHz frequency response and 300 kΩ input impedance. Thresholds are logic 1 (hi-LED) 70% V_{CC}; logic 0 (lo-LED), 30% V_{CC}. Detectable pulse width is 300 ns min. Both devices require 5 V at 30 mA/15 V at 40 mA. **Energy Electronic Products Corp,** 6060 Manchester Ave, Los Angeles, CA 90045.

Circle 254 on Inquiry Card

9000-POINT MATRIX BOARD

Matrix board is arranged in a 90 x 100 format, subdivided into 30, 30 x 10 configurations, and provides 9000 programming cross points in a standard 21.2 x 19" (53.9 x 48.5-cm) rack panel. Part number 072-879-2603-990 has two decks, and programming holes are on 0.1" (0.254-cm) centers. Both shortening pins and diode pins can be accommodated for interconnecting or sequential test programming. **Sealectro Corp,** 225 Hoyt St, Mamaroneck, NY 10543.



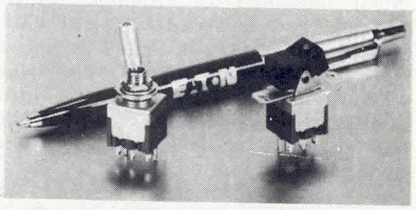
Circle 255 on Inquiry Card

RFI POWER LINE FILTERS

Available in 2- and 6-A configurations, these filters, made by Feller AG in Switzerland, are designed for use with instrumentation, communications equipment, industrial controls, computers, and peripherals. They provide attenuation of 40 dB min from 1 to 100 MHz. Connections are with combination solder/0.25" (0.64 cm) quick disconnects. Filters satisfy both European and North American test agencies and can be used interchangeably in equipment made for domestic or export markets. **Panel Components Corp,** 335 Tesconi Circle, PO Box 6626, Santa Rosa, CA 95406.

Circle 256 on Inquiry Card

MINIATURE SWITCHES WITH BUILT-IN LEDs



Rated at 125 Vac, 6 A, or 250 Vac, 3 A, in spdt configurations, both toggle and rocker style switches have integral LED and utilize solder lug terminals that are epoxy sealed to prevent flux contamination. Toggle switches are designed for single-hole panel mounting while rocker switches use subpanel mounting with flat style frame. Said to consume minimal power, have long service life, and not generate heat, the switches permit circuit switching and indication in a single unit. **Eaton Corp, Commercial Controls Div,** 4201 N 27th St, Milwaukee, WI 53216.

Circle 257 on Inquiry Card

PRODUCTS

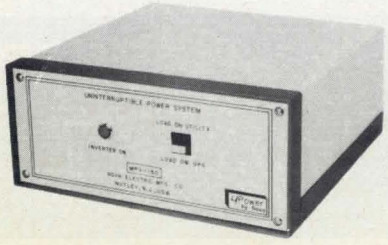
64-CHANNEL LOGIC ANALYZER

With 100-MHz sampling on 64 channels and 400-MHz effective sampling on 8 special channels, model D132 is controlled from a simple folddown keyboard. Self-prompting menu displays are used to establish trigger, sample, and display specs. Eight different setup procedures can be stored internally, each with 8 levels of sequential triggering. Calling up the desired procedures requires one key to select all controls for data acquisition. Basic 32-channel instrument expands to 48 or 64 channels for use with wide bus architectures. Multiple clocking operations allow access to bus structures operating either in synchronous or asynchronous modes. Additional systems features include glitch time trigger, dual memory compare, transitional clocking, and pre- and post-trigger repeat modes. **Intech, Inc, BP Instruments Div,** 282 Brokaw Rd, Santa Clara, CA 95050.

Circle 258 on Inquiry Card

SMALL INSTRUMENT POWER FAILURE PROTECTION

Switching at 50 kHz, MicroPower™ MPU-150 standby power system provides 200 W of 115 Vac power for 30 min. High switching rate permits what is said to be the smallest [8 x 11 x 4.625″ (20.3 x 27.9 x 11.7 cm)] and lightest [15 lb (6.8 kg) including rechargeable battery] 200-W system available. When utility power drops below 105 Vac, power is transferred within 25 ms. When utility power is restored, the load is reconnected to it and the battery begins charging. Rectangular waveform output voltage regulation is maintained within ±2%. **Nova Electric Manufacturing Co,** 263 Hillside Ave, Nutley, NJ 07110.



Circle 259 on Inquiry Card

PRODUCTS

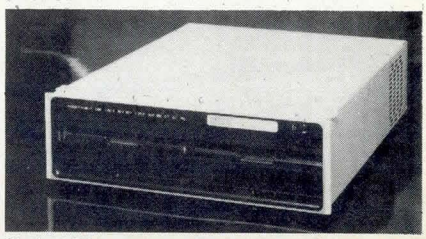
UNIVERSAL P/ROM PROGRAMMER

A 256k-bit RAM option for the company's IM1010 programmer allows loading multiple P/ROM images into programmer memory and programming complete sets of P/ROMs. With the programmer connected to a microprocessor development system, the user can load the IM1010 with a 32k x 8 P/ROM object file. When the data are in the programmer RAM, edit commands can be applied or multiple P/ROM sets can be programmed. The unit programs bipolar P/ROMs, EPROMs, single chip microcomputers, FPLAs, and can emulate P/ROMs using a ROM simulator module. **International Microsystems, Inc,** 11554 C Ave, Auburn, CA 95603.

Circle 260 on Inquiry Card

FLOPPY DISC DRIVE WITH RS-232-C INTERFACE

FT0227I provides up to 2M bytes of IBM compatible storage using dual-head drives to store 1M byte of IBM double-density formatted data on a single diskette. The unit includes two independent disc drives and convenient front panel controls for formatting, copy, and diagnostic functions. Two std RS-232-C interface ports insure easy connection to terminal or host computer. Modem controls provided by the unit support remote site usage in data collection applications. Data transfers up to 19.2k baud are supported. Data transfers of up to 65k bytes occur continuously with automatic seek to successive tracks without host interruption. Front panel controls allow the user to execute self-test and diagnostics independent of the host. **Scientific Micro Systems, Inc,** 777 E Middlefield Rd, Mountain View, CA 94043.



Circle 261 on Inquiry Card

LITERATURE

Power Sources

Illustrated engineering guide details electrical and mechanical specs and design considerations for available ac-dc and dc-dc power sources, switchers, and uninterruptible power supply systems. **Semiconductor Circuits, Inc,** Haverhill, Mass.
Circle 300 on Inquiry Card

Graphics for Control Systems

Booklet describes uses of interactive computer graphics display systems in control applications, highlighting raster scan technology and capabilities and applications of 9400 series imaging display systems. **Ramtek Corp,** Santa Clara, Calif.
Circle 301 on Inquiry Card

Strip Chart Recorders

Lists of features and photos for lab and portable models, input range adapters, and accessories for temperature and millivolt recording applications are included in 4-p bulletin. **Omega Engineering, Inc,** Stamford, Conn.
Circle 302 on Inquiry Card

RAM Test System

Illustrated brochure detailing features of J389 for production testing and device characterization includes discussion of computer controlled time domain reflectometry technique and Pascal-T. **Teradyne, Inc,** Woodland Hills, Calif.
Circle 303 on Inquiry Card

Data Concentrator

Applications, principles of operation, system hardware, troubleshooting functions, technical and functional specs, and configuration options for Micro800 are discussed in illustrated buyer's guide. **Micom Systems, Inc,** Chatsworth, Calif.
Circle 304 on Inquiry Card

Data Communications Equipment

Features of line of network control and restoral equipment, modems, and tech control products are provided in catalog also describing data communications network and diagnostics equipment. **Intertel, Inc,** Burlington, Mass.
Circle 305 on Inquiry Card

Miniature and Subminiature Switches

Photos, line drawings, specs, and engineering data for slide, pushbutton, wave-solderable, rotary, and illuminated and non-illuminated rocker and paddle switches are presented in catalog. **Chicago Switch Inc,** Chicago, Ill.
Circle 306 on Inquiry Card

Rocker, Toggle, and Lever Switches

Catalog illustrated with photos and mounting and wiring diagrams includes mechanical, electrical, and materials specs along with associated hardware, accessories, and cross-reference guide. **Dialight,** Brooklyn, NY.
Circle 307 on Inquiry Card

PCB and I/O Connectors

Found in catalog with photos and drawings are materials and finishes, mechanical and electrical data, UBS and UBC series crimp contact and unshrouded header specs, and tooling/component and special assembly information. **ITT Cannon Electric,** Santa Ana, Calif.
Circle 308 on Inquiry Card

Step and Synchronous Inductor Motors

Performance curves, electrical and mechanical specs, connection diagrams, drive circuit characteristics, and summary of features are provided for 1.8° step and 72 r/min motors. **Globe Motor Div, TRW Inc,** Dayton, Ohio.
Circle 309 on Inquiry Card

Precision Measurement And Control

Specs for data conversion and signal conditioning products, temperature instrumentation, digital panel instruments, and computational circuits and list of related publications are contained in short form guide. **Analog Devices,** Norwood, Mass.
Circle 310 on Inquiry Card

Statistical Multiplexers

Diagrams, charts, and summary of specs are included in handbook explaining use of series II to improve or create data communications network. Write Bill Arnold, **Timeplex, Inc,** One Communications Plaza, Rochelle Park, NJ 07662.

Industrial Microcomputer Devices

Catalog describes and lists options for modules, desktop and RacPac system packages, peripherals, compilers, interpreters, and line of multifunction modules designed to operate in harsh environments. **Xycom, Inc,** Ann Arbor, Mich.
Circle 311 on Inquiry Card

IC Sockets

Included in illustrated catalog and design engineering guide are descriptions of DIP and low profile sockets, solder-tab and Wrapost[R] very low profile socket configurations, and mechanical specs for 6- to 64-pin position sizes. **Cambion,** Cambridge, Mass.
Circle 312 on Inquiry Card

MIL-STD Switches

Product guide with photos presents basic data on sealed, QPL, and general purpose thumbwheel, pushbutton, lever actuated, and rotary switches along with features and options for each model. **Digitran Co,** Pasadena, Calif.
Circle 313 on Inquiry Card

Voice Synthesis Technology

Brochure describes linear predictive coding technology and vocabulary development and discusses solid state voice synthesis processors, memories, and speech modules. **Texas Instruments Inc,** Dallas, Tex.
Circle 314 on Inquiry Card

EMI/RFI Ceramic Filters

Catalog describes line of C-, L-, Pi-, and T-style lowpass filters, ac filters, eyelet style subminiature capacitors, and 8-32 bolt style filters and includes photos, dimensional drawings, installation guide, and applications notes. **Viclan, Inc,** San Diego, Calif.
Circle 315 on Inquiry Card

LITERATURE

Membrane Keyboards

Tactile and non-tactile etched copper/flex circuit combination and screened conductor thin polyester substrate keyboards and their applications and technology are cited in booklet with photos. **Rogers Corp, Flex Circuits Div,** Chandler, Ariz.
Circle 316 on Inquiry Card

Subminiature Switch Assemblies

Design features, material specs, and terminations for 10- and 15-mm subminiature Tini DW Multi-Switch[R] switches are detailed in brochure also covering available push buttons and options for non-illuminated versions. **Switchcraft, Inc,** Chicago Ill. Circle 317 on Inquiry Card

Hybrid Video Sample/Hold Amplifier

Specs, features, applications, and mechanical outline drawings and pin connection table for SH-8518 module in 24-pin double DIP metal package are supplied in 4-p bulletin. ILC **Data Device Corp,** Bohemia, NY. Circle 318 on Inquiry Card

Process Control Instruments

Booklet provides functional descriptions and photos of electronic and pneumatic controllers, sensors, and transmitters for temp, level, flow, and pressure, gas analyzers, valves, and digital computer systems. **Taylor Instrument Co, Div of Sybron Corp,** Rochester, NY.
Circle 319 on Inquiry Card

Computer EMI/RFI Shielding

Bulletin outlines shielding requirements of UL, FCC, FDA, and VDE and illustrates and describes conductive silicone elastomer strips, gasketing, conductive coatings, and cable shielding. **Metex Corp, Electronic Products Div,** Edison, NJ.
Circle 320 on Inquiry Card

Video Display Terminals

Specs, including display, keyboard function, switch selectable transmission modes, and options, for line of ADM-3A and -3A+, full- or half-duplex dumb terminals are listed in 4-p brochure. **Lear Siegler, Inc,** Anaheim, Calif.
Circle 321 on Inquiry Card

Harsh Environment Power Supplies

Military quality, partially and fully encapsulated, open frame, and switching units are detailed in catalog, along with overvoltage protection, rackmount, and thermal data for base rated models. **Technipower, Inc,** Danbury, Conn.
Circle 322 on Inquiry Card

Teleprocessing Network Loop Modems

Direct interface to IBM 360X controller bipolar port, permitting teleprocessing network enhancement, optional diagnostic secondary channel, and network diagrams for LSI 24L are covered in brochure. **Paradyne Corp,** Largo, Fla.
Circle 323 on Inquiry Card

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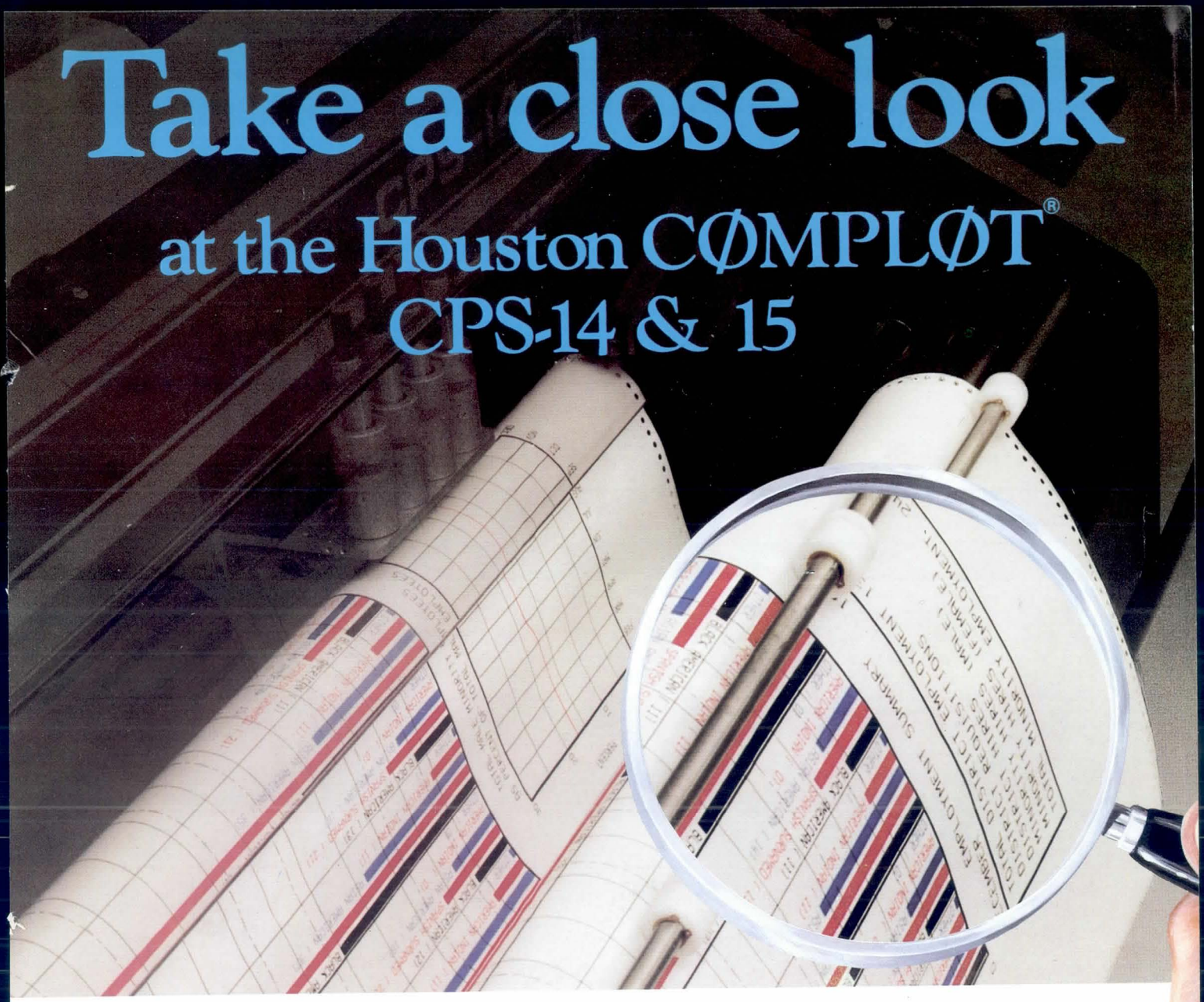

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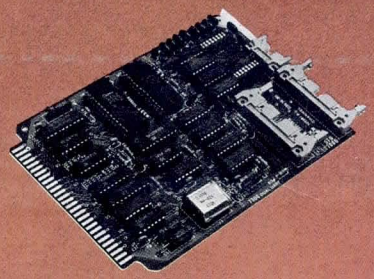

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