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# COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED SYSTEMS

JANUARY 1984

## SPECIAL REPORT: DESIGN TOOLS

# It's just not fair to claim that TEMPLATE® is the best graphics software available. Our competition's already discouraged.

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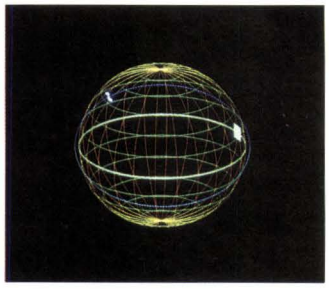

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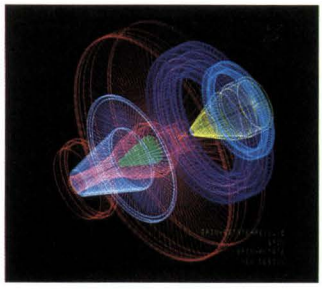

But let's be fair. If you're looking for graphics software, call our competitors first. Find out what they have to say about theirs. Then call us, and find out why TEMPLATE really has no competition.

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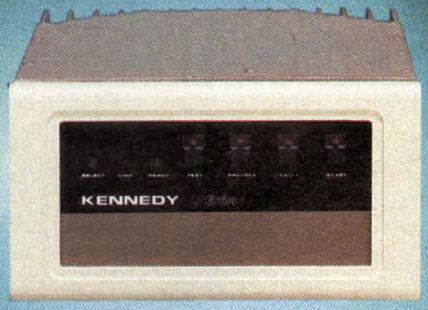


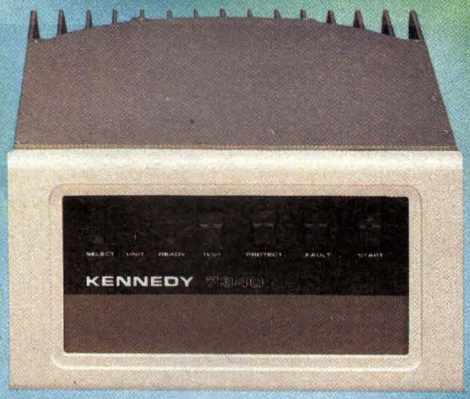


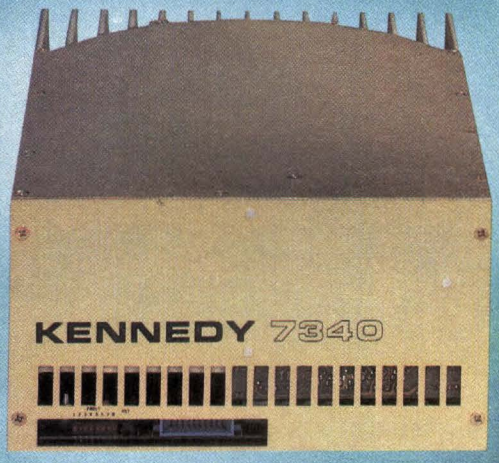


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CIRCLE 3

# UP FRONT

## IBM exits Josephson work

IBM has reluctantly admitted that its research activity into the fast-speed, low power Josephson technology has been heavily curtailed. The company attributed the decision to both the slow progress on developing a cryogenic processor as the next generation computer, and to the faster development in alternative technologies such as gallium arsenide. Work in Josephson circuits has also been severely limited in other laboratories such as Bell Labs and Sperry R & D Labs. Meanwhile, Hypres Inc, a new company formed by former IBM employees, has announced that it is proceeding at full speed to develop what the company labels a commercially viable "quiteron." This device is similar to a Josephson junction circuit and also operates at cryogenic temperatures. Hypres operates out of Elmsford, NY and has obtained license from IBM to develop a quiteron-based ultrafast signal processor. The company's founder is F. Faris, who developed the quiteron while employed at IBM. Wafer production of the devices is expected to start this month.

## MUMS the word

Marking Seagate's (Scotts Valley, Calif) move into the 8-in. arena, the multi-user memory system (MUMS) combines a half-height, 100-Mbyte Winchester drive with a controller capable of handling a second drive as well as secondary storage devices. To fit the needs of supermicro systems, the ST8100 drive has cut access time down to 30 ms using a proprietary voice coil linear actuator design. Transfer rate is 10 Mbits/s.

A key component of a memory system for multiple users is the ST9100 controller. Designed around the ST412HP interface at the drive level, the controller supports the SCSI interface standard at the system level to sustain the high throughput rates demanded. When packaged with a single drive, half-high, quarter-inch tape cartridge drive, and power supply, controller fits in a cabinet measuring 16 x 16 x 3.5 in. (41 x 41 x 8.9 cm).

## Microprocessor extends capabilities of 6502

Removing the limitations that restricted the 6502 from many applications, a 16-bit design executed by Western Design Center (Mesa, Ariz), is hardware and software compatible with that popular chip. The 16-bit 65816 microprocessor, developed in CMOS, runs 6502 software in emulation mode without revisions. This plug-in replacement for the 6502 switches to 16-bit mode under program control. Architecturally, the chip provides an 8-bit external bus and a 16-bit internal bus to speed internal movement of data and instructions. The hybrid 8- and 16-bit processor accommodates the object code of its 8-bit predecessor as a subset.

## Digital finally talks

DECtalk, a voice synthesis box that transforms ASCII text to quality speech, has been introduced by Digital Equipment Corp (Maynard, Mass). The device takes any computer output and transforms the ASCII characters into any one of several voices from an older male, to a female, to a young child. The device has an unlimited vocabulary and features speaking rates of from 120 to 350 words/min as well as pronunciation and intonation controls. DEC expects the device to find wide application in telephone access to computer data bases where the push buttons can be used as prompts for gaining information on a variety of subjects. The device also has educational potential in helping handicapped people. DEC engineers attribute the high voice quality to the development of a sophisticated computer model that almost perfectly simulates the human vocal tract. Demonstrated without fanfare in several applications at DECtown in late Aug 1983, the device will be available in quantity in March at an expected price of $4000.

# UP FRONT

## Transportable personal computer sports versatility

A nationwide introduction of the M3000 by MicroStandard Technologies Inc (New Lebanon, Ohio), at the recent Comdex show was hailed as being the most flexible and expandable personal computer for industrial/military applications. The ruggedized unit is water-resistant and dustproof and occupies a little more than 1 cubic-foot area. The personal computer comes with a choice of Z80A, 8088, 8086, or 68000A processors and allows the user to choose from one of three optional card cages to interface with other peripherals. The three card cage types hold four STD bus, two VME bus, or two S-100 bus boards. In addition, besides the standard 64 Kbytes of internal RAM, an optional 512-Kbyte RAM board can be inserted into one of the STD bus card slots. The color monitor is a full RGB unit with a monochrome version offered as an option. Storage capacity includes one 376-Kbyte 5¼-in. floppy disk with options that include either double-capacity floppies or one floppy and a 10-Mbyte, 5¼-in. Winchester hard disk. Based on the configuration, prices range from $1645 to $2895.

## Sun shines for engineers

Powerful workstations for software development, document preparation, and CAD/CAM work have been introduced by Sun Microsystems, Inc (Mountain View, Calif). The Sun-2 family of desktop and rackmountable stations is based on a 10-MHz 68010 microprocessor with a 1-Mbyte internal memory that can display bit-mapped graphics of 1152- x 900-dot resolution. A demand-page virtual memory allows for simultaneous display of multiple windows. The machines have been embedded with an advanced version of the Berkeley Unix 4.2 operating system that runs C, Pascal, and Fortran compilers; and the MC68010 assembler. Included in the basic $16,900 price is an Ethernet interface card and a 9-slot IEEE 796 (Multibus) card cage.

## Computer security gets a break

A copyright insurance technique enables software vendors to sell their services over telephone lines without fear that their copyright interests will be violated. Telelok from the Vault Corp (Los Angeles, Calif) allows modem-to-modem communications of programs stored on floppy diskettes in a way that ensures that the receiving party is the only authorized agent for the transmission. A proprietary manufacturing process etches an identifying scribe into the oxide surface of diskettes. The vendors retain a master diskette while the receiving community is given an encrypted version of the program. When this version is played back on the fingerprinted diskette it only permits the receiver to read the program's contents. This two-key encryption method requires the creation of only one master disk, and that backup copies be generated without compromising the security. The Telelok system is transparent to legitimate users and does not require special hardware. The current version is available for MS-DOS-based machines.

## Fast chip compares data strings

A special IC that can rapidly search a data base for matching or approximately matching strings has been produced by Proximity Devices Corp (Fort Lauderdale, Fla). The PF474 compares strings up to 127 bytes long to a query string and computes a degree of similarity for each comparison. It also maintains a list of the 16 best matches and provides users with the ability to set the desired degree or proximity. Using its DMA facility, the PF474 can perform 49,600 comparisons and rankings of 8 character strings/s.

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CIRCLE 4

# COMPUTER DESIGN®

## System technology


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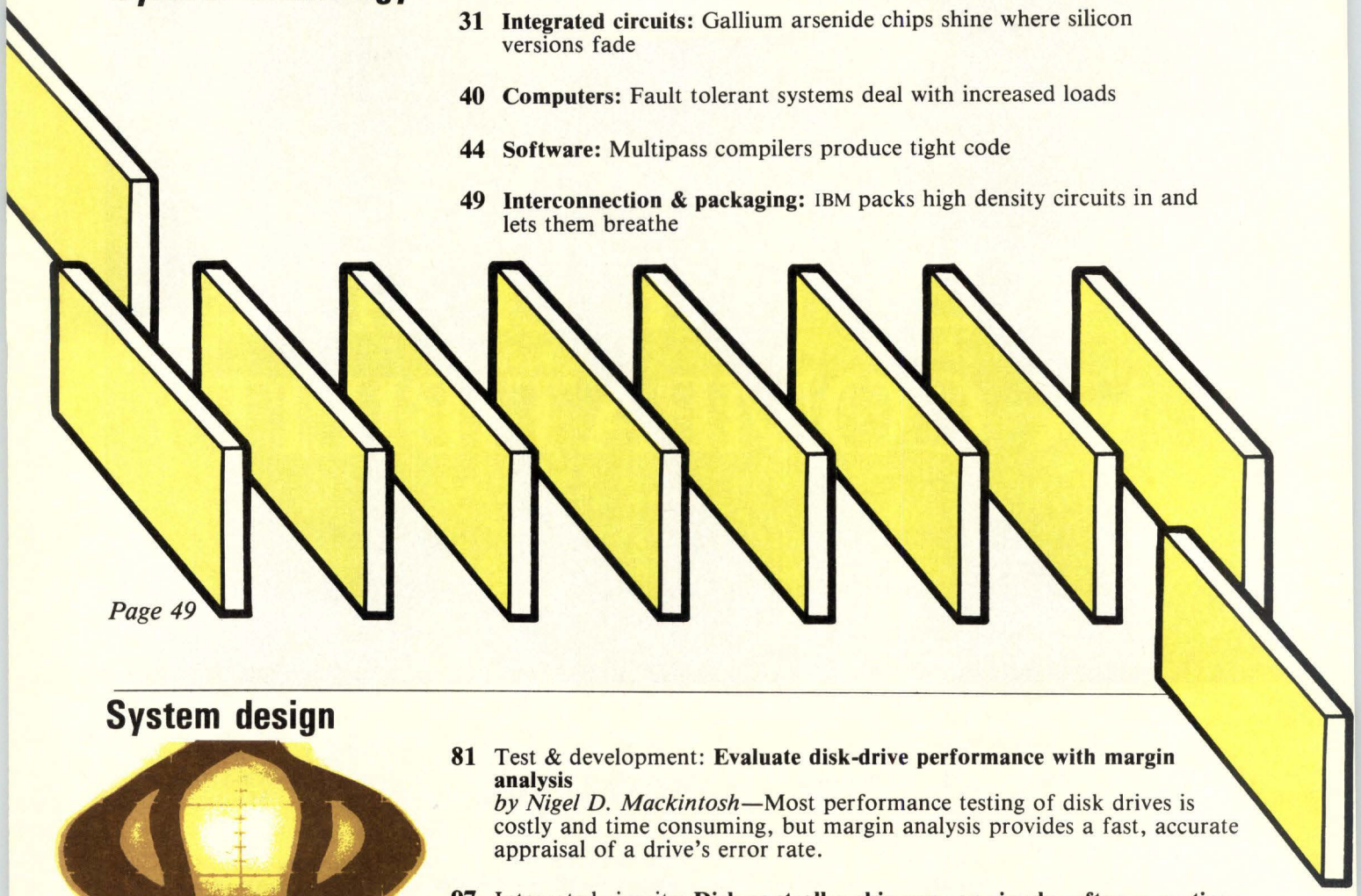

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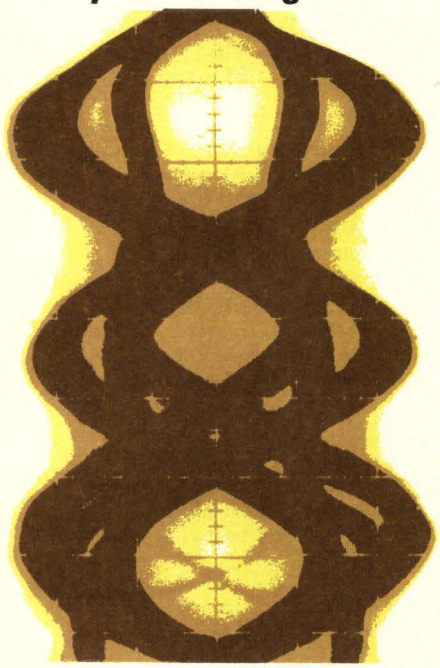
## System design



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*by Nigel D. Mackintosh*—Most performance testing of disk drives is costly and time consuming, but margin analysis provides a fast, accurate appraisal of a drive's error rate.

**97** Integrated circuits: **Disk controller chip runs on simple software routines**
*by David Davidian*—Successful integration of programmable controllers into computer systems requires devices whose command set unburdens both the host processor and the system designer.

**113** Software: **A second look at computer piracy**
*by Estella S. Gold*—The case of Apple versus Franklin may give copyright protection to software, but the guidelines are not clear. The decision can be better understood in the context of a cultural collision between the technical and legal professions.

**127** Software: **Language-based architecture eases system design—III**
*by B. Jane Curry*—Occam channels are implemented on a multiprocessor Z80 system, using the only computer language designed for multiple processors and true parallel processing.


## ISSCC '84


**61** Next month's International Solid State Circuits Conference in San Francisco will amass a trove of digital and analog circuits to whet the appetites of computer system designers. Among the newcomers are more 1-Mbit memory chips, 20-ns static 64-K RAMs, and faster access EPROMs.

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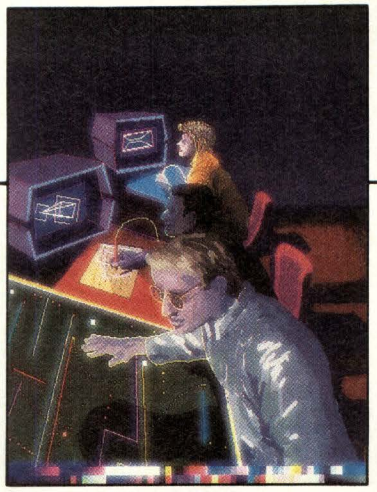
Jan 1984



*This month's cover was created and designed by Mark Lindquist on the Digital Effects Video Palette III and D-48 high resolution camera system.*

## Special report on design tools

**145** The meteoric growth in complexity of 16- and 32-bit microprocessors places new demands on software developers, who must now work with processor and system functions in terms of high level languages. With the vast number of designs appearing in embedded and realtime control systems, the programmer must nonetheless continue correlating events in software with exactly timed events in the hardware system. Manufacturers of the new generation of microprocessor development systems are rising to these challenges not only with high level programming languages, but also with realtime debugging tools, user interfaces, and communication and management systems to tie the team development effort together.

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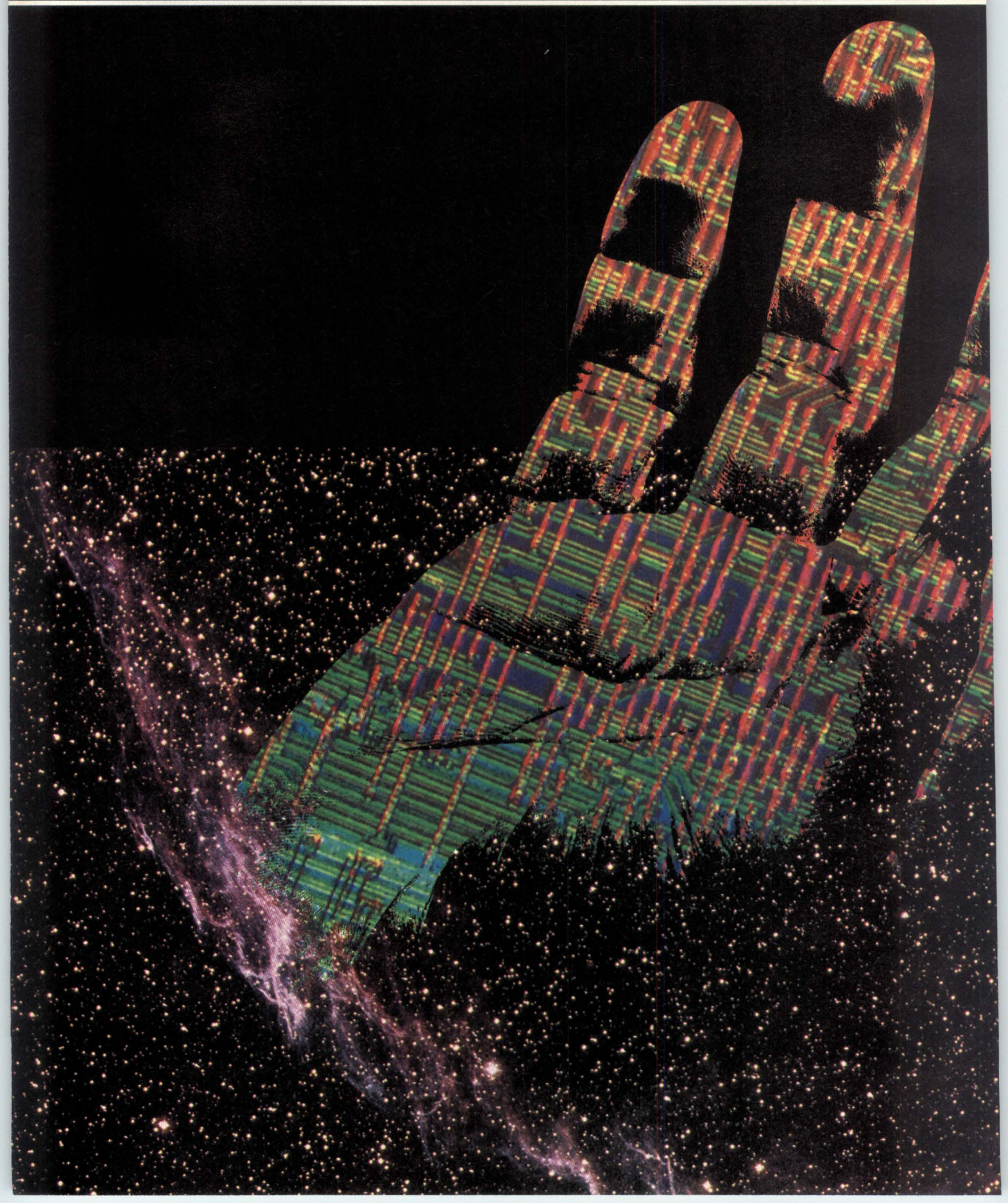
# *Where in the Microworld*



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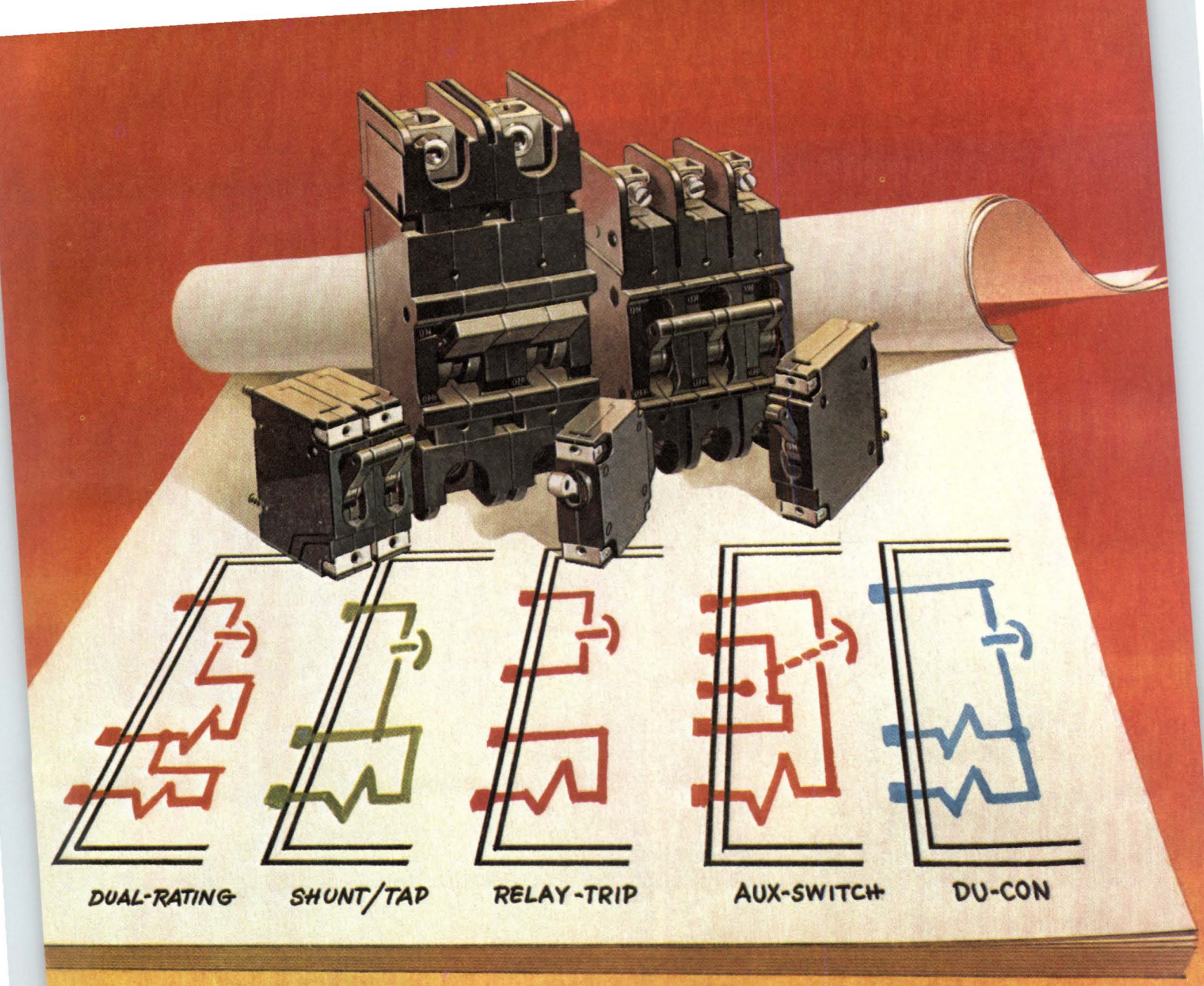
CIRCLE 137

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CIRCLE 7

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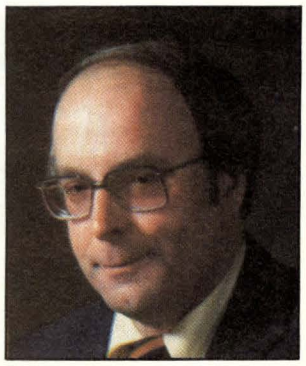
# WHEN THE CHIPS ARE DOWN



All too frequently in the computer industry, conventional wisdom proves unwise. For example, just a few short years ago, it was often said that most semiconductor companies would willingly give away microprocessor chips if they could be assured of getting the subsequent orders for memory chips to go with them. Yet, today we find that some personal computer manufacturers may go out of business because they cannot get enough of the popular microprocessor chips, such as the Intel 8088 or 80186. Also, some processor chips (eg, the 8051) are in such tight supply that they go for as much as $200 each in the clandestine "gray market."

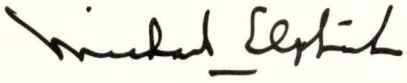
Commenting on the present situation, Jack Scanlon, a vice president of AT&T Western Electric, joked in his keynote address at the recent Comdex Fall '83 exposition in Las Vegas, "This is the last place on earth where chips are not only in ample supply, but seem to maintain the same price for longer than 24 hours." Obviously, something not so funny happened on the way from yesterday's market projections to today's reality. Actually, several things happened—some predictable and some quite unpredictable.

The first problem with the early market projections was that they were extrapolated from a mainframe computer experience in which each CPU worked with enormous amounts of memory. Shorter wordlength microprocessors, however, were able to directly address much less memory. Also, bit densities of memory chips climbed rapidly in accordance with "Moore's Rule." Thus, fewer chips were needed for a given amount of storage capacity. Furthermore, Japanese semiconductor manufacturers (perhaps spurred by the bullish market projections) decided to target the RAM chip market, and glutted the world with inexpensive memory chips.

On the processor side, the problem was caused primarily by IBM. That company's use of Intel processor chips in its personal computers, coupled with its equity investment in the chip supplier, made the 8088 a *de facto* standard almost overnight—competing computer manufacturers rushed to share the market dominance promised by the IBM PC. There were few alternative sources for the Intel chips because other semiconductor manufacturers were either promoting their own designs or could not afford the required capital investment in the midst of a semiconductor industry slowdown. After the surge in demand for the 8088, other Intel processors also became scarce—the 80186 because it offered higher performance in personal computers, and the 8051 because it was made on the same fabrication lines as the 8088.

Of course, Intel will be expanding its output while other suppliers, such as Advanced Micro Devices, will offer alternative sources and expand their production capacity. Yet, the inevitable correction of the supply/demand imbalance may come too late to save many of the companies now jostling for the limited number of positions on the computer store shelves.

It would appear, therefore, that—in an industry where the stakes have become so high—there is an urgent need for better market research. No longer can research merely state the obvious or extrapolate from past experience; rather, it must explore various scenarios. To put it another way, Murphy's Law may not always prevail, but that is probably the way to bet.



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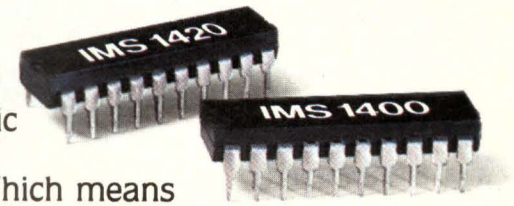
# In 16K static RAMs, INMOS choices...starting

# means high-performance with 35ns access times




**When you're looking for top memory performance in your system, look to today's leading supplier of high-speed static RAMs...INMOS. Because INMOS gives you a choice of speeds, organizations, power dissipation and packaging. Which means you can optimize your designs, without compromising on cost or performance.**

**High speed.** The INMOS family of fast static RAMs deliver access times of 35, 45, and 55ns. Perfect for high-performance tasks such as buffer memories, graphics, and main-store memory. And they give you a low-cost alternative to expensive 35ns ECL parts. Choose our by-1 organization for deep memory. Or the by-4, which also offers versions with 30 and 40ns chip-select access times, for writeable control store and cache memory. Most versions are available in plastic DIPs, ceramic DIPs, and chip carriers.

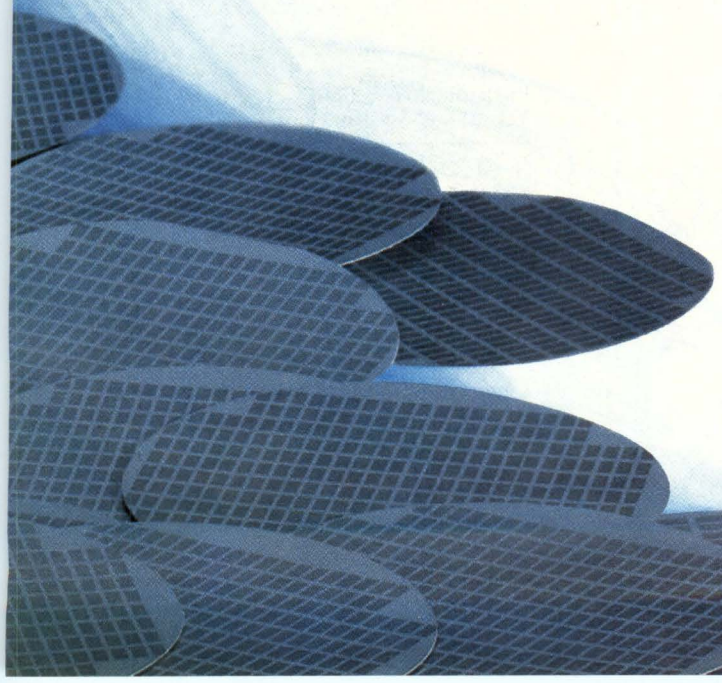
**Low power.** For high performance combined with low power, INMOS offers plastic packaged SRAMs with 70 and 100ns chip-enable access times in by-1 and by-4 organizations. Both have maximum power dissipation of 495 mW active, 83 mW standby. The by-4 organization is also a better alternative to 2Kx8 SRAMs in many high-speed applications. Best of all, they're both low cost. Here's your answer for fast systems that are power critical and price conscious.

**Military versions.** When you need fast RAMs you can trust in hostile environments, INMOS can supply 55 and 70ns parts with specs guaranteed over the full military temperature range of -55°C to 125°C. These parts, available in side-brazed ceramic DIPs, chip carriers, and flat-paks, conform to MIL-STD 883B processing, including screening to class B Method 5004 and quality conformance to Method 5005.

**Check the chart.** With all these choices, its easy to see why INMOS is the leading high-speed RAM supplier. Look for the part you need, then call an INMOS distributor for complete details.

| Organization | Speed (ns) | Power (mW) Active | Standby | Part No. |
|---|---|---|---|---|
| 16Kx1 | 35 | 660 | 110 | IMS1400-35 |
| | 45 | 660 | 110 | IMS1400-45 |
| | 55 | 660 | 110 | IMS1400-55 |
| | 70 | 495 | 83 | IMS1400-70L |
| | 100 | 495 | 83 | IMS1400-10L |
| 4Kx4 | 45 | 605 | 165 | IMS1420-45 |
| | 55 | 605 | 165 | IMS1420-55 |
| | 70 | 495 | 83 | IMS1420-70L |
| | 100 | 495 | 83 | IMS1420-10L |

**INMOS Distributors:**
Anthem Electronics, Arrow Electronics, Future Electronics, Lionex Corp., RAE



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**CIRCLE 8**

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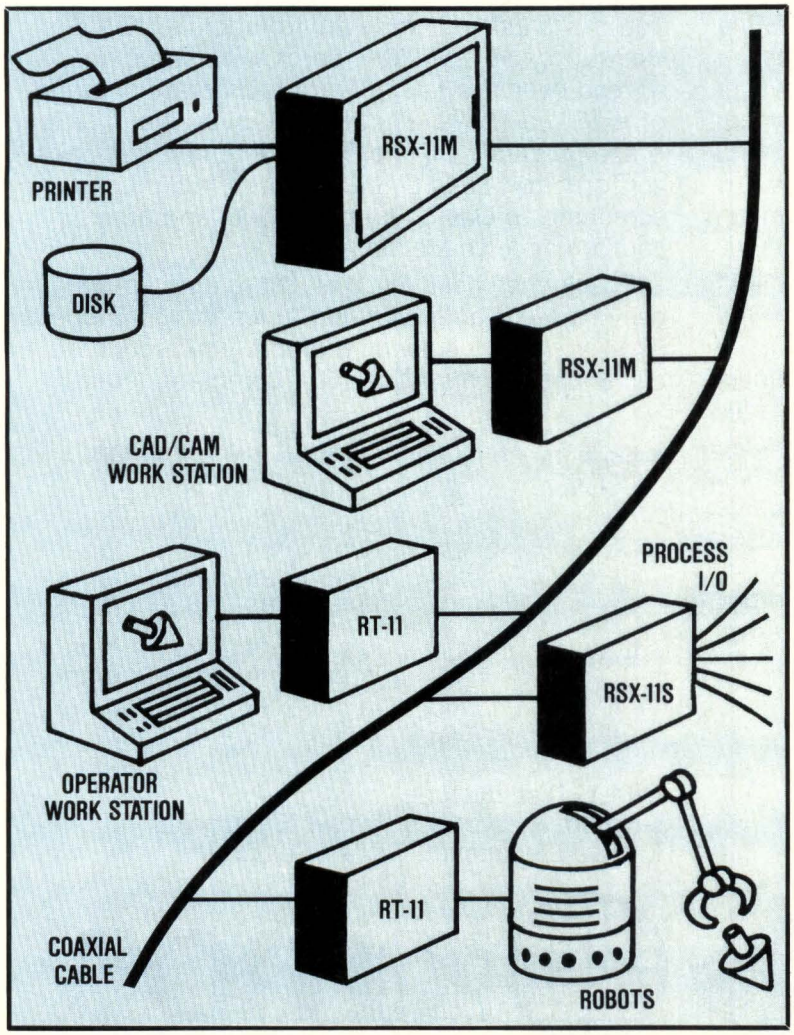


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- 256Kb main memory (expandable 4Mb)
- Expansion space for 15 dual height modules.
- LSI-11/23 16 bit CPU with memory management.
- 4 Serial ports.
- Advanced disk controller with ECC, flaw management, bootstrap, error retry and non-interleaved data transfer.
- PDP-11* architecture compatible with RT-11, RSX-11M and UNIX** software.
- 17.8Mb, 35.6Mb or 71.2Mb Winchester disk.
- Self test with LED display of system faults.
- Start/stop tape supports file operations.
- Compact 3M Cartridge.

TAPE CONTROLLER ONLY AVAILABLE FOR VOLUME REQUIREMENTS.

* Trademark of Digital Equipment Corporation. ** Trademark of Western Electric.

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**CIRCLE 147**

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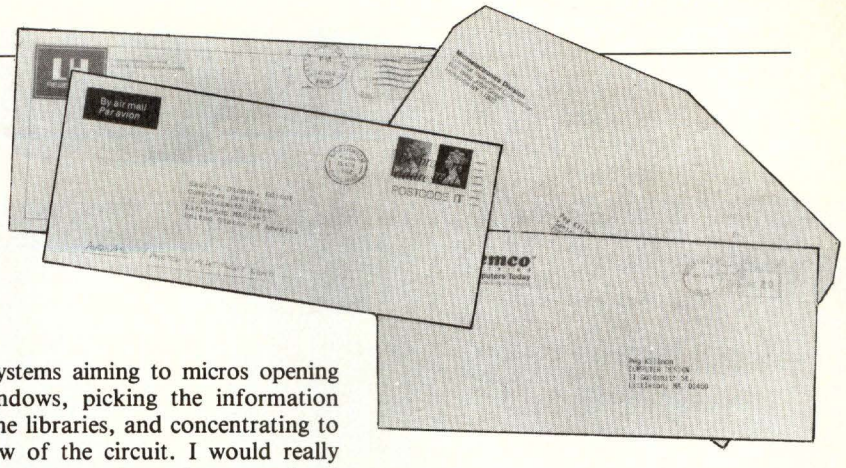
CIRCLE 11

# LETTERS TO THE EDITOR




## More on CAE workstations

*In his May 1983* Computer Design *editorial, "We've Seen the CAD—Now Let's See the CAE," Saul Dinman (then Editor in Chief) asked users and prospective users of engineering workstations for comments and relevant experiences. Here are some of the answers:*

I want it all! Schematic capture, digital and analog simulation, local floppies (1 Mbyte), network capability, mail, remote files, plotters, printers, high speed, color graphics, PC layout, and gate array packages.

R. B. O'Hara
Fairchild Space & Electronics
Germantown, Md

Amen! We have purchased systems and software for design purposes and have been both pleased and disappointed with the products. Now we are looking for a CAD/CAM system for drafting, schematic design, and the ability to lay our PC boards onto clear Mylar for direct production.

Barry Larsen
Gemco Electric
Clawson, Mich

Working on system engineering of complex systems requires very frequent preparation of system diagrams and brief notes or explanations. The diagrams get changed frequently, but ultimately the products are briefings, memos, and technical reports. An engineering workstation that has easy-to-use graphics and word processing capability would be very useful. The engineering workstation would be accessible by other engineers, secretaries, and graphics personnel to convert draft material into final form. Workstation access to current and predicted project cost data would also be useful. Some of these techniques are now being used.

J. H. Selander
Mitre
McLean, Va

Only the logic simulation is of help to the engineer. The rest of the features are just a means of automating the data documentation. If the test pattern generation or the running of the simulation is inconvenient, the CAE station will not be used. "Using a computer should be easier than not using a computer."

S. Young
Interstate Electronics
Anaheim, Calif

We are following, with very high interest, the CAE development and market. We read all the details about hardware, software, and prices. I also dream about low price systems aiming to micros opening the windows, picking the information from the libraries, and concentrating to the flow of the circuit. I would really buy the components one by one and put the system together. How can I get the software? Help.

Dezso Fokos
Hughes Aircraft Co
Irvine, Calif

Any workstation should be able to access the data base created by the drafting function. This base should include schematics, PC layouts, bills of material, weldments, assemblies, etc. Using this base, the engineer can perform analyses of circuits, structures, and temperatures without having to reenter basic information on the design of the subsystem. The workstation operator should only be required to know about 25 commands to operate the system on the existing design data base.

Frank Luteran
Weston Controls
Archbald, Pa

I work with a university research environment—designing research computers. However, the greatest problem faced is that of design documentation. The greatest boost to my productivity would be a high resolution graphics personal workstation to provide editing functions on both word and drawing documents. I believe my productivity would increase by at least 100 percent with even modest CAD software tools.

Prof D.M. Koch
Monash University
Clayton, Australia

Here we have a small number of workstations due to the "closed market" in our country that prohibits the importation of such equipment, or reduces it. In our factory, we have a Gerber CAD and we're using it for mechanical and drawing design. We're still in the beginning with printed circuits due to missed information. I personally use a TRS-80-like micro in my home technical affairs. We need more knowledge in the CAE area to get to use such stations.

Enrique Ferri
Industrias Villares SA
Sao Paolo, Brazil

What bothers me most, and the reason for not buying a microcomputer yet, is the lack of support for a Fortran compiler with which quick enough response can be obtained. Key application is mostly scientific data processing and simulations, and I have to limit myself to mainframe or large minicomputer systems.

Mario Y. Atias
Aerotec Consultants
Petah Tikua, Israel

More details of other companies' experiences/benefits will be needed before certain companies ever consider the "workstation/engineer" approach. A great number of functions will be covered by a good graphics and scientific S/W system.

N. J. Tebble
Marconi Avionics Ltd
Welwyn Garden City, England

I was very much impressed by a recent announcement that Simulation Sciences will place its PROCESS—Process Simulation Package (Steady State)—on an HP 9000 desktop minicomputer. Our engineers have used this package for years—on various IBM machines in a time-sharing mode (TSO, etc). This has been less than satisfactory from the user's point of view due to delays in logon, slow turnaround, etc. However, the PROCESS package is useful so they persisted in using it. The point of all this is that engineers will be delighted to use an engineering workstation as long as it is sufficiently large enough to accommodate software that is useful to them. With the HP 9000 desktop, this breakthrough has been achieved.

George A. J. Homolka
Arabian American Oil
Ran Tanura via Dhahran, Saudi Arabia

There is a need [in CAE] for microcomputer software (IBM PC, Apple) that combines text editing, graphics, circuit simulation (digital and analog), etc, in the realm of electrical engineering.

*(continued on page 22)*

# STAY OUT OF THE

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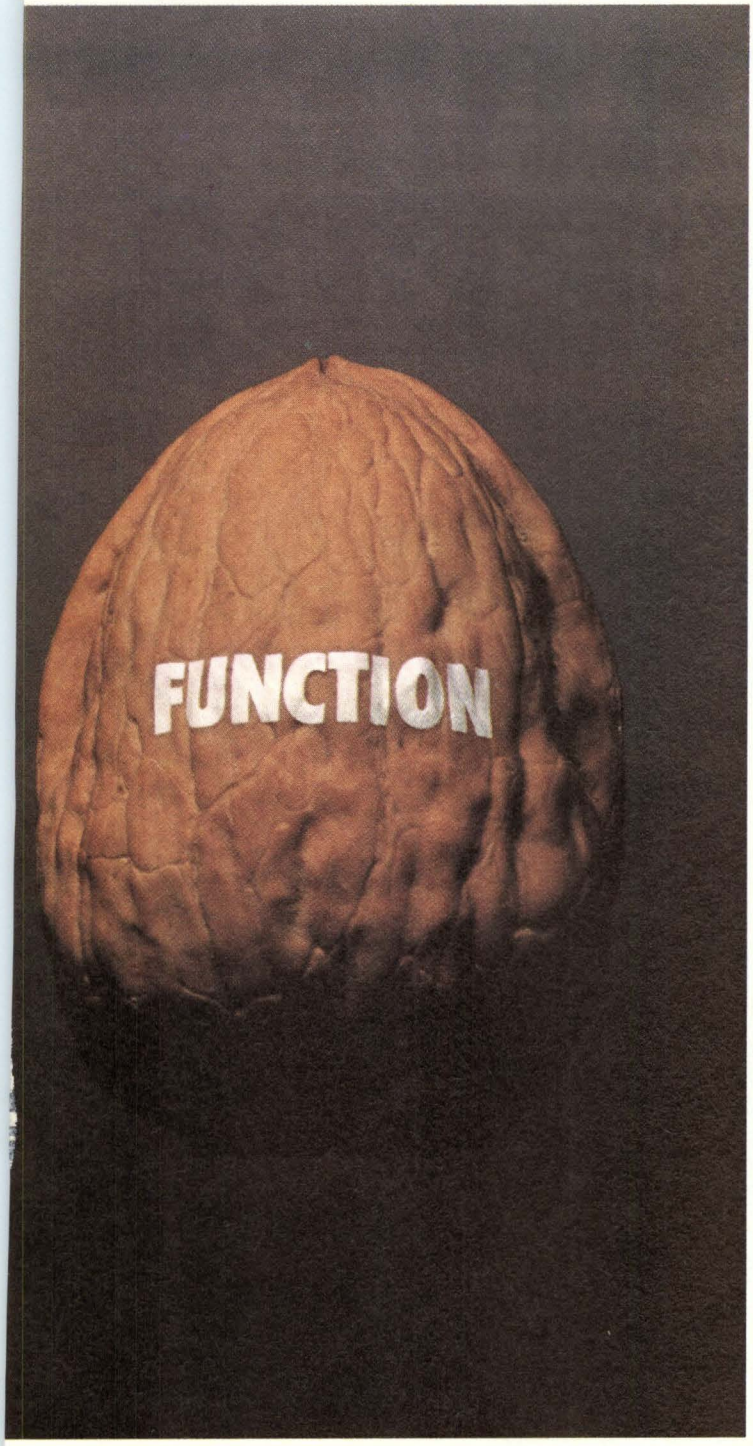
# GUARANTEE GAME.




It's easy to spot the "now-you-see-it, now-you-don't" guarantee.

It guarantees function, but not at speed. Or speed and function, but not at temperature. While you're looking at one part of the guarantee, another part moves, changes, vanishes.

And that can be a very expensive game.

Better talk to Advanced Micro Devices. We're the folks with the long suit in quality and the short guarantee.

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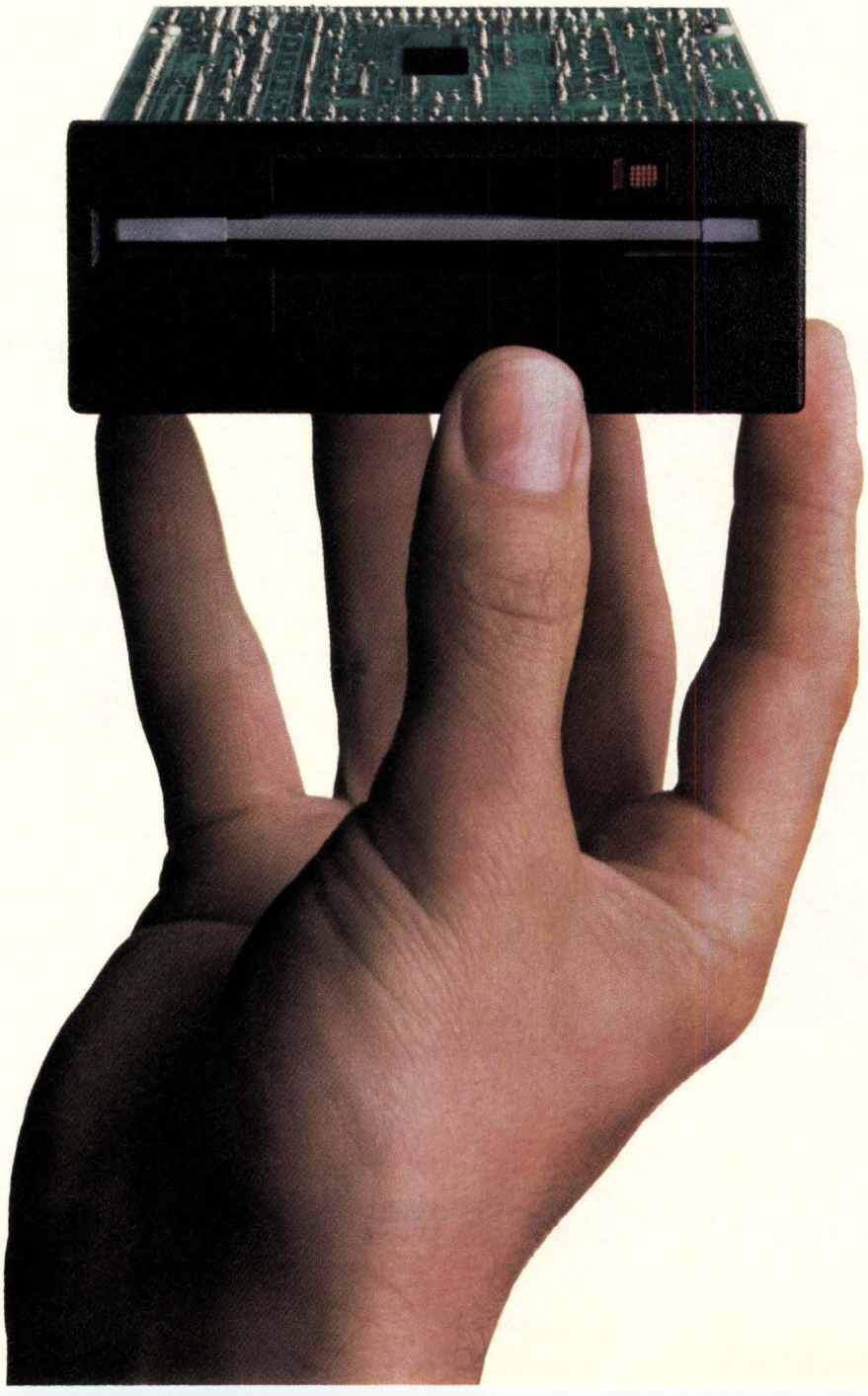
CIRCLE 12

# DO YOU HAVE THE DRIVE TO SUCCEED?



You do?

Good. So do we.

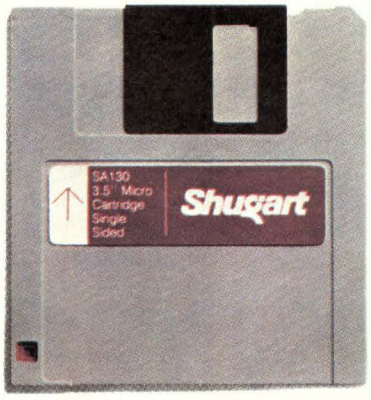
Shugart's 3.5" microfloppy drive. The SA300 by name.

And, considering where the personal/home/portable computer market is headed (betterfastercheapersmallerwithmorestorage), it's not a moment too soon.

It's also quite an achievement. One that allows you to engineer a wealth of advantages into smaller, more competitive systems.

Take the most obvious advantage, for instance.

Size. With the SA300 you can make your personal and home systems less imposing, more, well, personal. Our microfloppy takes up 75% less room than a standard sized Minifloppy.™




*The 3.5" Micro-Cartridge provides maximum media protection.*

And it weighs just a tad over a pound. So your portable system can be more, you guessed it, portable, even with two drives in it.

Yet the SA300 still delivers 500 Kbytes in the single-sided version (1 Mbyte in the double-sided version) and uses less power, worst case, than an 8-watt night-light.

It's also so quiet, you can't hear it running unless you put your ear right down on top of it.

And with an MTBF of over 10,000 power-on hours, it should run for quite some time.

Then, of course, there's the not-so-small matter of the industry standard 3.5" microfloppy diskette.

Which offers a few important advantages of its own.

Like Minifloppy compatibility.

A track density that allows room for a generous upgrade path to more capacity.

And a hard shell plastic media cartridge for protection against the rigors of pocket and purse, with an automatic head access shutter as a last line of defense against little computer users who eat a lot of peanut butter and jelly.

Want to learn more?

We'll do a private Microfloppy Workshop right in your office. And you'll have the chance to talk with media manufacturers and our own applications engineers about your plans for a big design win.

Call your local Shugart Sales Office to set it up. But do it soon.

You'd be amazed at what you can do with a little drive.

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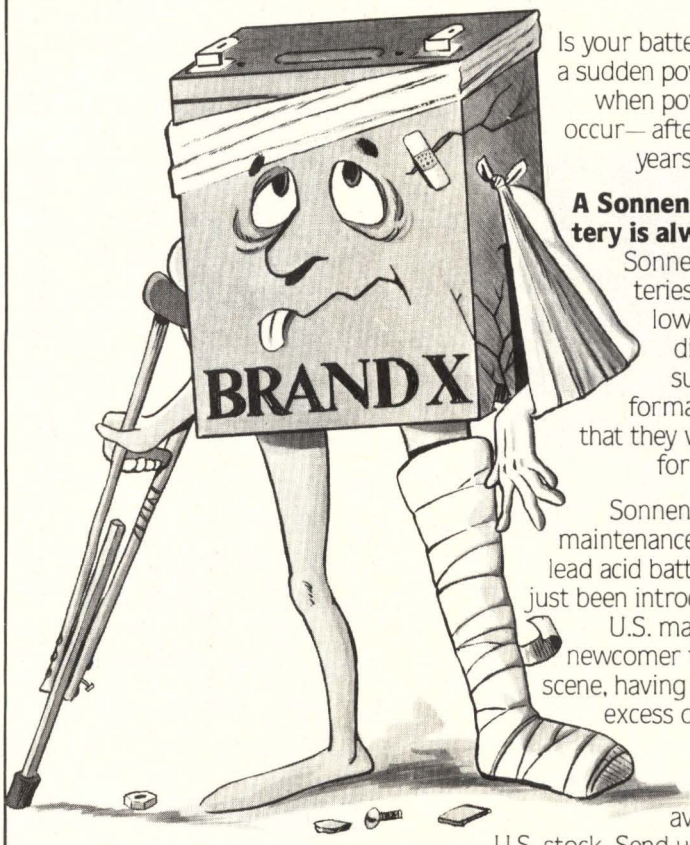
**CIRCLE 13**

# Assault & Battery.

**(The costs could cripple you.)**

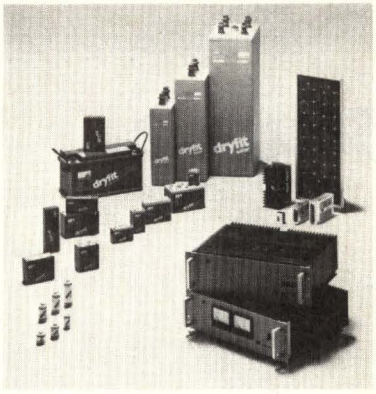



Is your battery ready for a sudden power demand when power outages occur—after 3, 5, 7, 10 years on the job?

**A Sonnenschein battery is always ready!** Sonnenschein batteries have such a low rate of self-discharge and such high performance on float that they will be ready for any assault!

Sonnenschein is the maintenance-free sealed lead acid battery that has just been introduced to the U.S. market. It is no newcomer to the world scene, having produced in excess of 20 million batteries.

All models available from U.S. stock. Send us your application and see what a Sonnenschein will do for you. 1Ah-1350Ah. 2-12 V.



Write for our 24 page dryfit Brochure with all the details.

**Sonnenschein**

**Sonnenschein Batteries Inc.**
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Please send me your DRYFIT Brochure.

**Name** _____

**Address** _____

**City** _____ **State** _____ **Zip** _____

**Application** _____

Meets NATO Military specifications.


# LETTERS TO THE EDITOR

*(continued from page 17)*

Unfortunately, most of the match software does not have the ability to conveniently deal with complex numbers, if at all. I need to develop models, store them, combine them, excite them, and display the resulting steady state and/or response, etc.

Phillip Cutter
Orange Coast College
Costa Mesa, Calif

### Bubble memories do have benefits

Deb Highberger's Fall 1983 article, "Sizing Up 16-bit Portable Computers," included a lot of good information in this exciting new product area. However, I must comment on Mr Mitchell's statement, "I think that [CMOS SRAM] is going to win out over bubble and everything else," found on p. 56.

Bubble memories operate at a fraction of the power requirements for floppy disks or Winchesters. And, with proper techniques, bubbles aproach the power consumption of CMOS RAM, with standby current below 20 mW. This certainly makes bubbles suitable for battery-operated portables. Add to that bubble memory's high density, solid state reliability, and lower cost per bit than CMOS RAM both today and for the foreseeable future, and it is clear that bubbles have an important future in portable computers.

In fact, *Computer Design* could do its readers an important service by further educating them in the significant features bubble memory can bring to a microcomputer system.

Michael W. Eisele
Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051

### Another 32-bit chip set

In Sam Bassett's article, "Microprocessors: Speed Up, Price Down, and CMOS Everywhere," (Oct 1983) there was an erroneous statement. On p 186 under the subhead "On the horizon," Mr Bassett claims that "The only 32-bit chip set currently on the market is Intel's three-chip 432 architecture."

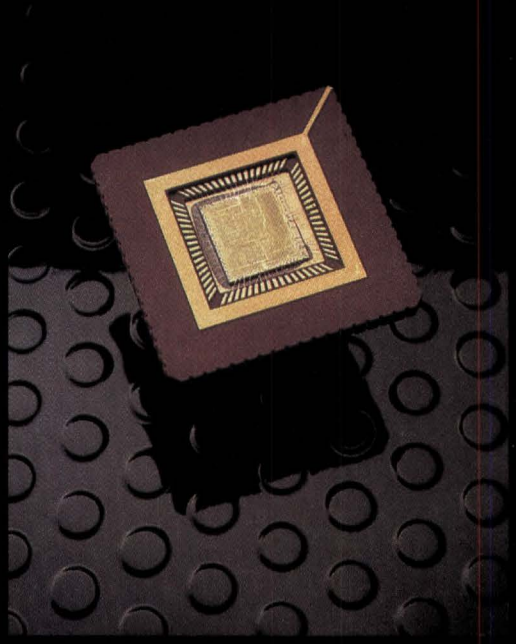
NCR Corp's Microelectronics Div is producing, and has been sampling since July 1983, a full 32-bit chip set—the NCR/32 microprocessor family. The NCR/32 provides new VLSI mechanisms for offchip microcoding, instruction-set partitioning, and microcode primitives.

Mary Anne Ryan
NCR Corp
1635 Aeroplaza Dr
Colorado Springs, CO 80916

 CIRCLE 14

# NS32032

## The First True 32-Bit Microprocessor to Become Reality.



## NS32032

*The first commercially available microprocessor to feature:*

1. *Full 32-bit architecture*
2. *Full 32-bit internal implementation*
3. *Full 32-bit data bus to memory*

**The industry's consensus: with the introduction of the NS32032, the NS16000™ microprocessor family has become the foundation for the next generation of high-performance, low-cost computers.**

Any software developed for the 32-bit NS32032 will run just as well on the 16-bit NS16032 or the 8-bit NS08032, and vice-versa. And it will also run on future NS16000 32-bit CPUs. Consider this absolute *downward-upward* object code compatibility in contrast to the *upward-only* compatibility of other microprocessor families, which will make their 16-bit processors obsolete when they add 32-bit processors to their product line.

The NS16000 microprocessor family already includes peripherals compatible with its CPUs, and each is in full production: the *NS16201* Timing Control Unit (TCU), the *NS16202* Interrupt Control Unit (ICU), the *NS16081* Floating Point Unit (FPU), and the *NS16082* Memory Management Unit (MMU). Since the FPU and MMU interfaces are almost entirely invisible to NS16000 programs, the decision to include or omit floating point or memory management hardware (for cost/performance reasons) will not affect NS16000-based systems' software compatibility.

The billions of bytes of existing mainframe software can now be easily ported to run on NS16000-based systems. The NS16000 family's mainframe-in-silicon architecture (designed specifically to support high level language programming), its full high-speed floating point arithmetic capability, its integral support for Demand Paged Virtual Memory, and the NS32032's 32-bit data bus to memory combine to make this possible for the first time.

Elegance, you see, is everything.

Think about it.

# The only limits on NS16000-based applications are those of the imagination.

**The full 32-bit architecture of the NS32032 (shared by all NS16000-family CPUs) sets no bounds to programmers' productivity or creativity.**

No other processor family—micro, mini, *or* mainframe—has an architecture designed to fully support the use of high level languages, with a structure and behavior corresponding directly to the objects and operations of HLLs.

Its powerful features:

- —A compactly encoded, completely symmetrical, two-address instruction set.
- —Thirteen addressing modes (many not found in other microprocessors) designed for the kinds of accesses compilers generate.
- —Indexing automatically scaled to argument size (1, 2, 4, or 8 bytes), applicable to any addressing mode.
- —Instructions to implement high level language constructs such as case statements, loops, and calls, as well as bit-field and string manipulation.
- —A fully integrated floating point instruction set, supported by hardware.

**The 32-bit architecture of the NS32032 (like that of the other NS16000 CPUs) is fully implemented, without exception or restriction.**

Simply stated, physical limitations in processing or packaging technology have not constrained internal implementation. All NS16000 CPUs have a full 32-bit Arithmetic Logic Unit (ALU), a full 32-bit register set, and a full 32-bit internal data bus to the input/output control block.

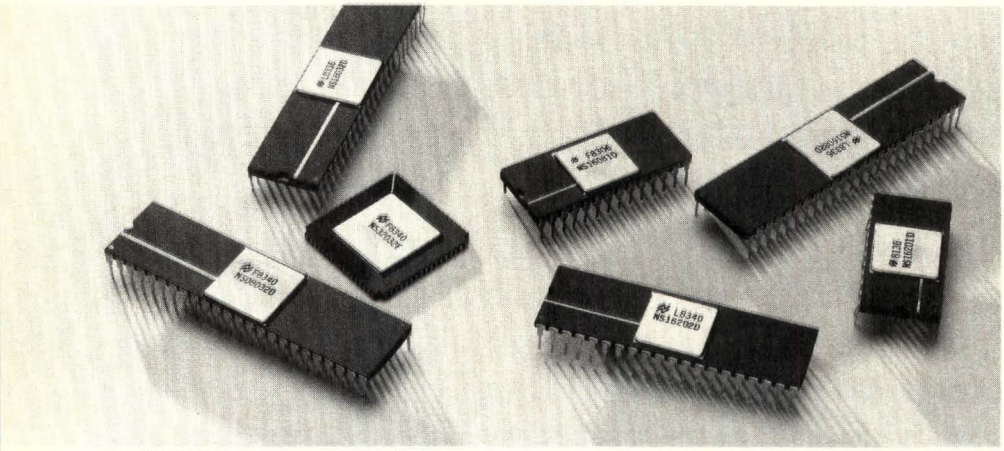
The value of such elegant implementation? An example: competitive microprocessors take eight to twenty internal steps to execute the expression evaluation "A = A * X + Ai," commonly used in high-performance technical and scientific applications.

The NS32032 takes four.

**The NS32032's full 32-bit data bus to memory increases memory bus bandwidth—and thus the speed at which data can be transferred.**

In simple systems (CPU and memory), the NS32032's ability to access a full 32 bits of external data dramatically increases the rate at which instructions and data are processed, while leaving bus time available for system peripherals.

Because it requires less than 50% of the available bus bandwidth in standard applications, the NS32032 is also ideally suited to complex *multi*-processor systems, DMA transfers, and high-speed graphics.



The NS16000 microprocessor family.

**In the NS16000 family of CPUs, the primary feature that distinguishes one processor from another is the width of the data bus to memory.**

The fact that the NS08032 and the NS16032, with their 8-bit and 16-bit data buses, share identical 32-bit architecture and 32-bit implementation with the NS32032 means that it is now possible to develop 8- and 16-bit systems with all the benefits of 32-bit software performance. The same software can now be implemented on all the systems within a product family; an enormous benefit to programmers and systems designers.

Future 32-bit CPUs planned for the NS16000 family will feature improved performance—bettering the NS32032's 1 MIPS tenfold by 1988—yet these future CPUs will also be compatible. This clear migration path guarantees the preservation of your initial software investment while providing for significant enhancement in your product line.

No other family of microprocessors shows such forethought or foresight.

TYPICAL EXECUTION TIMES (in μs at 10MHz)

| | Register-to Register | Memory-to-Memory | | |
|---|---|---|---|---|
| Instruction | NS08032 NS16032 NS32032 | NS08032 | NS16032 | NS32032 |
| Mov Byte | 0.3 | 1.7 | 1.7 | 1.7 |
| Word | 0.3 | 2.5 | 1.7 | 1.7 |
| Dbl.word | 0.3 | 4.2 | 2.6 | 1.7 |
| Add Byte | 0.4 | 2.0 | 2.0 | 2.0 |
| Word | 0.4 | 3.2 | 2.0 | 2.0 |
| Dbl.word | 0.4 | 4.7 | 2.3 | 2.0 |
| Mul Byte | 3.8 | 4.3 | 4.3 | 4.3 |
| Word | 5.4 | 7.0 | 5.8 | 5.8 |
| Dbl.word | 8.6 | 12.0 | 9.6 | 8.4 |

**Additional reasons why the NS16000 family now leads in microprocessor design-wins:**

1. *Hardware development can begin immediately.* All three CPUs are available right now. So are all the necessary peripherals in the family.

2. *Software development can begin immediately.* Appropriate evaluation tools, and both resident- and cross-support packages, are available now, as is an extensive list of third-party software.

Our *SYS16*™ – a multi-user, multi-tasking development system—incorporates the *complete* family of NS16000 chips (CPU, TCU, ICU, FPU, and MMU), and therefore gives up to eight programmers a true, native environment to work in.

GENIX,™ a product of our software engineering group, is the first microprocessor operating system capable of implementing Demand Paged Virtual Memory.

Adapted from the Berkeley 4.1 bsd version of UNIX,™ it has been elegantly tailored to optimize the NS16000 architecture. (We also offer source code under license for GENIX and its utilities.) Together, the SYS16 and GENIX demonstrate that the NS16000 microprocessor family makes the best "UNIX engine" on the market today.

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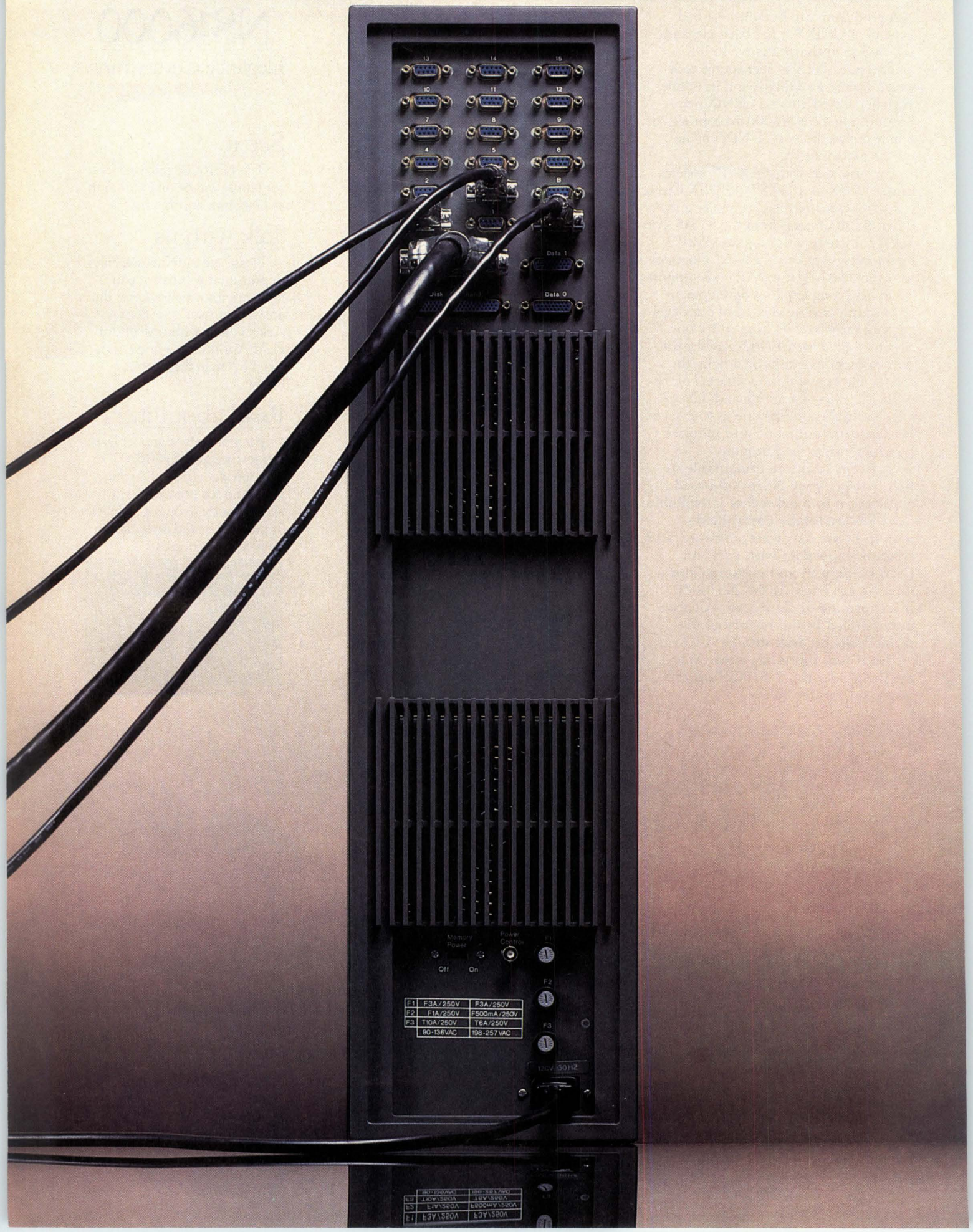
**National Semiconductor Corporation**

MICROCOMPUTER SYSTEMS DIVISION

**CIRCLE 17**


13
14
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9
4
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2
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Data 1
Disk
Data 0
Memory Power
Power Control
Off
On
F1
F2
F3
F1 F3A/250V F3A/250V
F2 F1A/250V F500mA/250V
F3 T10A/250V T6A/250V
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120V 50HZ

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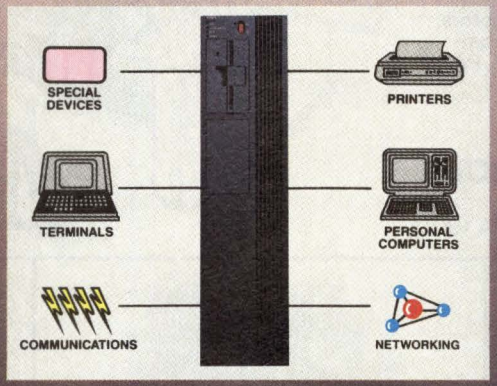


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CIRCLE 18

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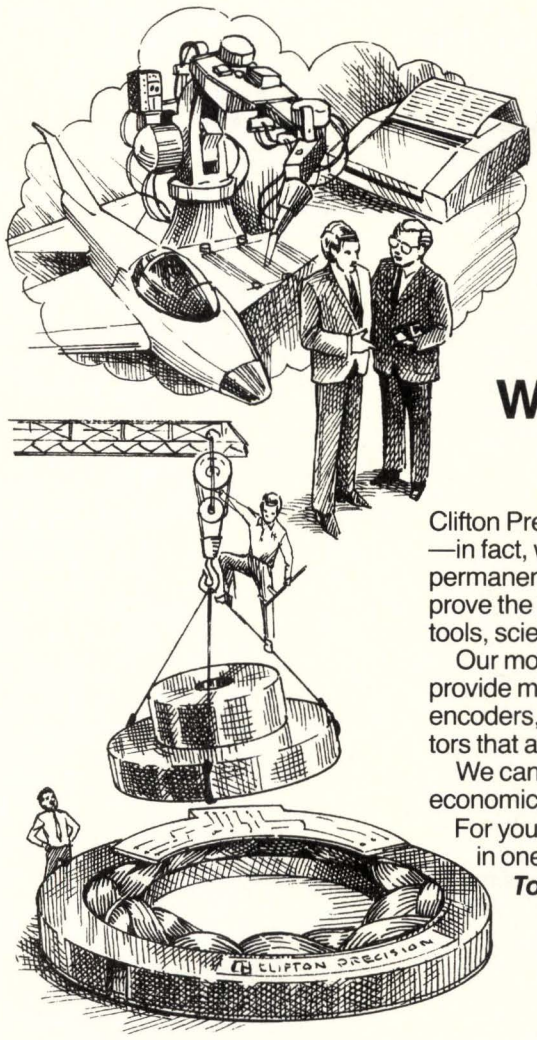


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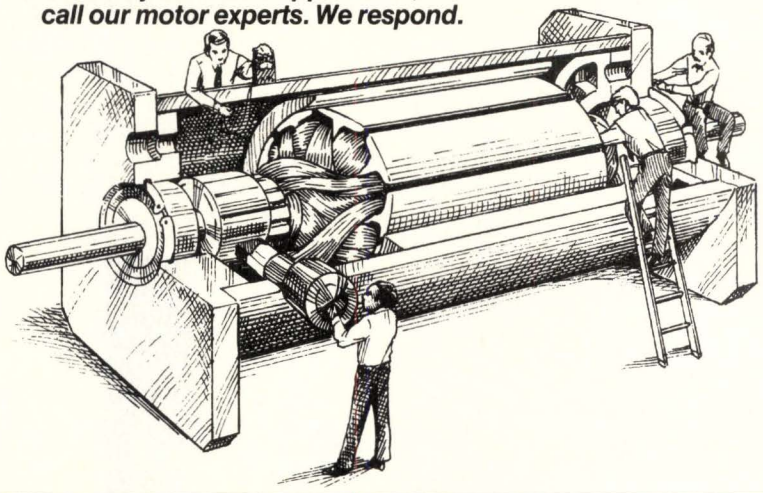

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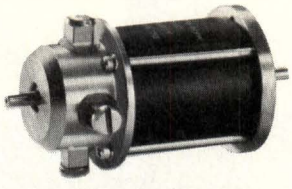

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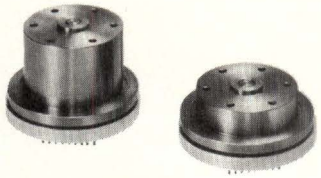

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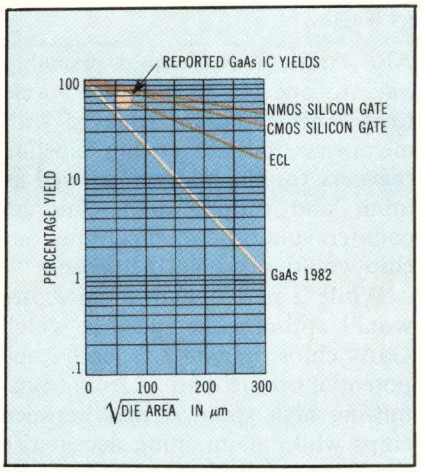
CIRCLE 148 CIRCLE 149 CIRCLE 150

For General Information Circle 151

# Gallium arsenide chips shine where silicon versions fade

Plainly put—the world is running out of quicksand. That is, the chemical compound silicon, found in sand and currently the bedrock of ICs, is reaching its physical limits. Silicon cannot switch digital logic signals at ultrahigh speeds without evaporating from the resultant generated heat.

While silicon diehards are squeezing every nanosecond out of new IC designs, proponents of another IC material—gallium arsenide—are reaching cruising speeds in the picosecond range. In addition, researchers




**In comparing wafer probe test yields versus die size for various IC processes, GaAs yields for a small die size have been reported matching those of bipolar ECL.**

are achieving these switching speeds with a smaller increase in power consumption than that of silicon-based circuits. As a result, prototype GaAs chips exhibit a smaller speed-power product than their commercially available silicon counterparts.

Until recently, the higher performance level of GaAs ICs could only be produced in insignificant wafer yields unacceptable for large-volume commercial production. Thus, applications for these chips were relegated to laboratory experimentation or very specific projects. Chips were being designed in areas where high speed was crucial for the operation of unique, sophisticated systems such as microwave-rf satellite receivers, military signal processors, or medical image processors—all analog applications.

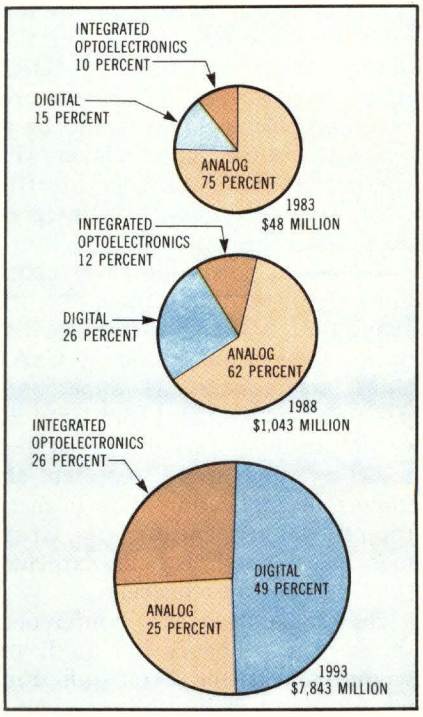
Recently, however, developments in GaAs technology have brought the technology to the forefront as a legitimate candidate for high speed digital applications such as supercomputers. Two major factors make this possible: modern silicon wafer production techniques are being used to dramatically increase GaAs wafer yields; and system engineers are concentrating their designs on applications for which GaAs digital chips are best suited. For the latter, second-generation high electron-mobility transistor (HEMT) technology will be instrumental in developing a GaAs VLSI computer that operates at ultrahigh speed and dissipates low power.

Reproducibility of good GaAs ICs is, of course, crucial to developing a supercomputer that exclusively uses GaAs circuits. To that end, one industry observer optimistically predicts wafer yields will approach those of silicon by 1993, or perhaps sooner. George Avery, of Technology Insight Consultants (San Jose, Calif), recently claimed that the same factors contributing to almost defect-free silicon chips will also play a key role in attaining better yields for GaAs ICs. Avery said this will happen at a faster rate than that achieved by silicon producers because "there is going to be a wealth of shared experience that will fall out of the silicon IC world in terms of equipment and techniques that can be applied directly to the gallium arsenide industry."

### Matching ECL yields

At a recent GaAs symposium in Phoenix, Ariz, Avery pointed out four reasons why silicon houses are now able to obtain consistent yields in the 80 to 90 percent range. These include improved contamination control, modern lithography equipment, defect-free masks, and dry processing. Applying the same methods to GaAs production will yield similar results, said Avery. To back that assertion, Avery pointed to the results of one GaAs company that has matched the yields of bipolar ECL wafers with similar-sized dies.

Based on these preliminary showings, Avery sees the three current market segments shifting dramatically in the next 10 years.




**The world market shares of GaAs will change dramatically in the next 10 years. While the majority of circuits today are analog, by 1993 integrated optoelectronics will grow to a 26 percent share and digital circuits will dominate with an almost 50 percent share.**

Analog applications, today a dominant market with a 75 percent share, will shrink to 25 percent by 1993, meanwhile digital applications, currently holding a 15 percent share, will expand to almost 50 percent, according to Avery. He makes these projections based on several assumptions. He expects resumed real GNP growth and GaAs market growth that will be demand-driven and supplier-limited. Avery claimed that the GaAs market will be independent from the silicon IC market. "Gallium arsenide ICs, I believe, are going to create their own very large

*(continued on page 32)*

### GaAs chips shine

*(continued from page 31)*

niche," said Avery. Barry Gilbert of the Mayo Foundation (Rochester, Minn) agreed by stating, "The two technologies are complementary and should not be competing against one another directly."

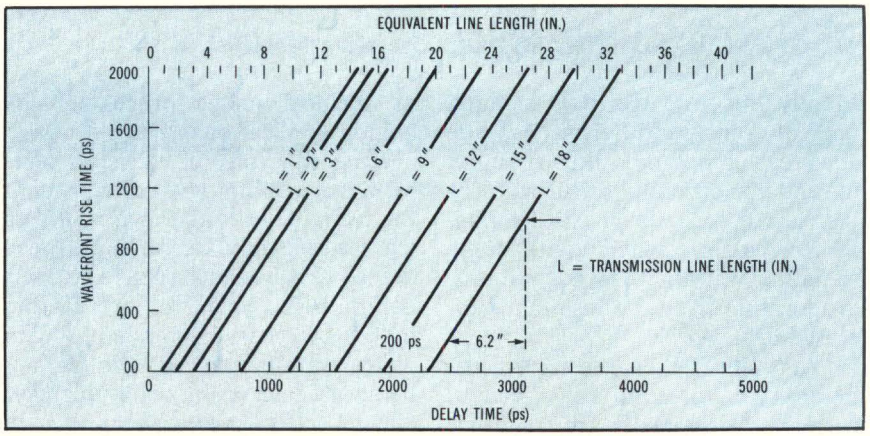
In fact, Gilbert said, designers should be striving at both ends of the speed/integration spectrum to maximize the potential of both technologies. He advocates that silicon producers push integration to the hilt while GaAs designers exploit the natural speed advantage of GaAs rather than try to integrate more functions onchip. This would be a defeatist course, since silicon will continue to have the edge in efficient, single-chip function integration for some time.

Gilbert called on the GaAs community to take advantage of its strengths, which automatically opens applications as far as GaAs chips are concerned. Supercomputers like the Cray 1 and Cray 2, which use many MSI chips in parallel to achieve high speed, represent an important application area. In fact, the next generation of Cray machines, Cray 3, is being targeted for GaAs chips exclusively.

Gilbert and other conference speakers at Phoenix put faith in second-generation heterojunction technology to realize the supercomputer goal. Currently, gate speeds of first-generation GaAs devices suitable for volume production are in the 100- to 350-ps region. This is two to five times faster than the fastest commercial bipolar ECL devices.

Second-generation devices whose development is proceeding at a feverish pace both in the U.S. and Japan are exhibiting propagation delays of 10 to 50 ps. To take full advantage of these speeds, according to Gilbert, processor onchip architecture must have a radically different orientation. The number of gate delays on each chip must be maximized to reduce system performance loss caused by interchip connections.

Gilbert addressed a specific set of problems encountered at the Mayo Foundation. "We have been looking at signal processors where data rates are at least 100 Mbytes," said Gilbert, "the clock rates in these processors are at least as fast as the data rates and, sometimes, 10 to 20 times faster. This is because a few microcycles of the engine are needed to capture and dispose each data byte as it enters and before accepting the next data byte." Thus, Gilbert's processor requires a clock rate that is sometimes 20 times higher than the data rate. "This is clearly a case where silicon VLSI is going to have trouble giving us the kind of performance we want, particularly toward the higher end," concluded Gilbert.




**While deliberate degradation of offchip rise times can alleviate interconnection problems, overall system performance is also reduced. Computer simulations performed in the Mayo laboratories on the trade-offs between wire delays and rise time effects indicate that rise times as low as 100 to 200 ps result in substantial reduction in effective interconnect length.**

### Serial solution

To solve this problem, according to Gilbert, there are two solutions. One is to have many coprocessors operating on the problem in parallel. This would be what the silicon VLSI community or the Department of Defense's Very High Speed Integrated Circuits program would opt for. The other approach would be to have a smaller number of processors connected in serial but operating at a much higher system clock rate—the GaAs solution.

For such a processor, logic and arithmetic algorithms would have to be written along the lines of recursive algorithmic forms. Systolic arrays would have to be implemented where the operands are not processed as full operands but are divided, and individual parts are screened through individual nodes. Also, static RAMs would probably have to operate at 1- to 4-ns cycle time. This could be achieved with memories that use onchip pipeline registers for the address, as well as input and output data. Address counters and other control lines onchip would also help the process.

While a new onchip architecture would optimize the speed at which GaAs chips operate efficiently, one potential problem arises from transmitting high speed signals between chips while maintaining decent rise times and fall times. Skin effect, series inductance, and signal noise all come into play. Gilbert said that the correlation existing between a signal's rise time and the interconnect length between chips should be used wisely to maintain fast rise times and also sustain system performance.

Using computer simulations and based on a board dielectric constant of about 2.3, Gilbert showed that if the signal rise time is decreased from around 1000 to 200 ps, it is equivalent to saving 6.2 in. of interconnect length between any two chips on the board. This observation, according to Gilbert, can be interpreted in two different ways: "Either the chips could be spread apart by an average of 6.2 in. using this faster rise time and throughput and system performance would remain the same, or the system could be packed as densely as possible and

*(continued on page 34)*

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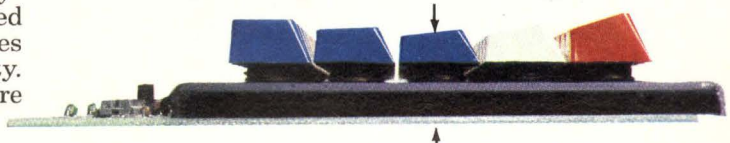

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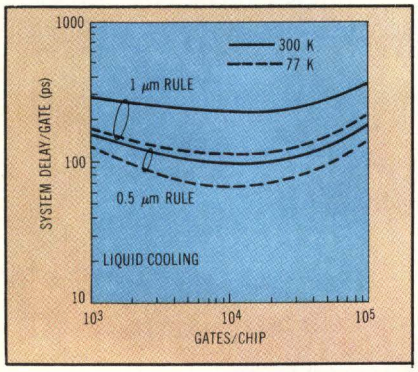
CIRCLE 20

**GaAs chips shine**

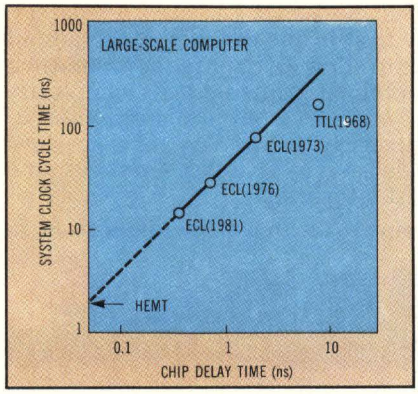
*(continued from page 32)*




**LSI complexity depends on system delay/gate. Fujitsu engineers were able to achieve an optimum system delay of 70 ps at a 10,000-gate integration level where the chip delay is 40 ps.**

thereby gain in performance." Thus, the advantage of maintaining rise times should not preclude designers from solving problems associated with ultrafast switching.

Several computer manufacturers have large research programs to design supercomputers with GaAs circuits. Fujitsu, Ltd, (Tokyo, Japan) used the Phoenix conference to describe its efforts to design a general purpose computer with HEMT technology operating at a system clock cycle of 2 ns and exhibiting 120 million instructions per second performance. The company has achieved switching speeds of 12.8 ps for a ring oscillator using HEMT technology, while its 1-Kbit static RAM using first-generation metal semiconductor field effect transistor (MESFET) technology has an access time of 3.6 ns. If replaced by an HEMT-based RAM, access time would be less than 1 ns. Impressive to say the least. In general, the switching speed of HEMT is roughly three times as fast as GaAs MESFET technology, according to Fujitsu.




**Fujitsu engineers were also able to improve system clock cycle time an order of magnitude over the best ECL technology by achieving a cycle time of 2 ns and by using HEMT second-generation GaAs chips.**

For evaluating desirable system performance of future high speed computers, Fujitsu engineers took into consideration the components that cause overall system delay. System delay results mainly from chip delay on the LSI chip and external wiring delay between chips. Usually, the chip delay time is calculated by summing the intrinsic gate delay, logic layout delay according to the fan-out capability, and the delay caused by the wiring on the chip. Fujitsu engineers calculated the delays based on experimental data for the HEMT devices with both a 1 $\mu$m gate length and a 0.5 $\mu$m gate length. The calculations were made for both 300K and 77K temperatures. Using 0.5 $\mu$m rule technology and liquid nitrogen cooling, an optimum system delay of 70 ps was achieved. This was done on a chip that had an integration level complexity of 10,000 gates, and the chip delay was 40 ps. This translates into a system clock time of 2 ns which is an order of magnitude improvement over the use of silicon-based ECL technology for such a computer.

Besides Fujitsu's efforts, serious work is being conducted at Toshiba, Mitsubishi, and Hitachi as well as a number of U.S. computer companies such as IBM, Honeywell, Hewlett-Packard, Harris, and instrument giant Tektronix. In fact, IBM can be expected to devote even more energy to this technology since the company decided to back off from extensive research into Josephson junction technology—until recently the leading contender to GaAs for high speed, low power design. Judging by all this interest, an objective observer might remark that, after many years, GaAs has come into its own to claim a place beside silicon for design of next-generation computers.

*—Nic Mokhoff, Senior Editor*

**SYSTEM TECHNOLOGY**

*(continued on page 40)*

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**Up to 500 Kbytes storage capacity.** Single or double side, single or double density models. 48 TPI track density. Head load time 35 millisec. FM (single density) or MFM (double density) recording method.

**Automatic disk eject.** Media removal is fast, smooth and easy.

**Simple design, high reliability.** High precision ultra-thin stepper motor is combined with a unique hub collet configuration in a simple, reliable design for improved accuracy in head positioning and media clamp centering.

**Improved disk life.** A ceramic based magnetic head protects the media from excess wear and provides increased accuracy of data readout.

**World-wide acceptance.** Many thousands of Series 2000 drives have been delivered to OEM manufacturers throughout the world. You can easily learn what they already know about The Alps Advantage—just write or call today.

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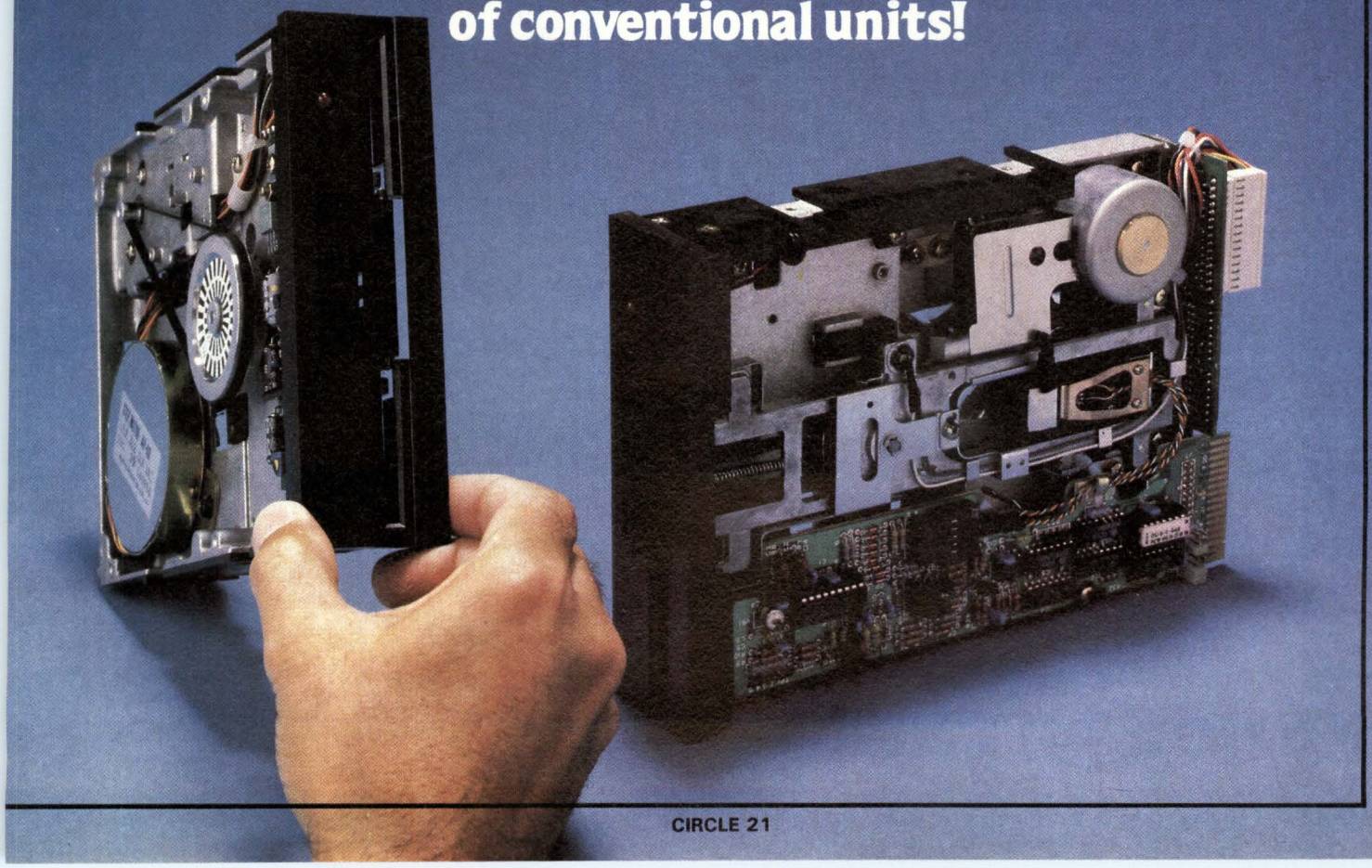
## Low profile Series 2000. Only 1.61" thick– half the size of conventional units!



CIRCLE 21

# If you don't find the logic you probably don't need

Meet the logic analyzer family that spans a wide spectrum in design. It's a family you can rely on in hardware design, software test and debug and even system performance analysis. One that's equally at home testing and troubleshooting low-cost single processor designs or sophisticated multiprocessor systems.

You can choose from a wide selection of different logic analyzer configurations with HP. And when you do, you'll have an analysis solution that can help accelerate your design cycles...and speed your products to market.

## The 1630A and 1630D...for confidence in tackling the day-to-day logic problems.

Choose one of these logic analyzers and you'll have the combined power of timing, state, and software performance analysis in one convenient, low-cost instrument. At just $8,600*, the 1630A gives you 35 channels of state/performance analysis (to 25 MHz), or 8 channels of timing (to 100 MHz). In the interactive measurement mode, it delivers 27 channels of state and 8 timing.

For $10,630*, the 1630D offers 43 channels of state/performance analysis or 16 timing. In the interactive mode, you have a choice of 35 state and 8 timing or 27 state and 16 timing.

As your primary tool in hardware test and debug, the 1630 provides new triggering power to help you isolate the source of timing errors. This includes pattern triggering ANDed with a transition or glitch, edge or glitch triggering, and time qualification of pattern triggering. This is the capability that helps you quickly solve difficult hardware problems such as timing errors, transient effects and handshake malfunctions.

Use the 1630 in software development and integration phases and you have sequencing, triggering, store qualification, and sequence restart power to isolate targeted areas of code and view just the measurement information you desire.

To optimize your system performance, the 1630 gives you a nonintrusive view of system software in action. One that lets you analyze system activity at the level of procedures and tasks instead of the instruction level. Histogram displays make it easy to spot software bottlenecks and inefficiencies. The result can be improved system performance, and a more competitive product...with minimal additional design effort.

The 1630 also gives you interactive measurement capability for greatly enhanced analysis power. The ability to cross arm and trigger between state and timing analyzers helps you get to the problem source quickly when the difficulty could be either a hardware or software malfunction.

Throughout the development cycle, you'll find the 1630 easy to use. That's because menus simplify operation. Label assignments let you view results in your system's terminology. And inverse assembly, via low-cost peripherals, displays listings in familiar target microprocessor mnemonics.

## The 64110A...a configurable analyzer that can handle those complex problems found in multiprocessor environments.

This logic analyzer is, in reality, a number of different analyzers, depending on how you configure it. For example, it can be a standalone timing analyzer with 8 or 16 channels.

It can also be a standalone state analyzer with up to 120 channels. You can combine timing and state with performance overview. Or, combine multiple state or timing analyzers in the same station.

Price for the 64110A,

# analyzer you need here... a logic analyzer.

including a 60 channel state analyzer subsystem with performance overview is $21,870*.

Put the 64110A to work in the hardware test and debug phase and you can allocate high speed timing resources. For example, you might choose sampling speeds to 400 MHz. The resulting 2.5 ns resolution lets you make high-resolution measurements to resolve timing margin problems.

In addition, the timing analyzer provides new triggering capability. The dual threshold mode lets you trigger on marginal signal levels, which helps you spot excessive fan-out, bus loading problems, and slow transition times. Other trigger modes include time qualification of pattern triggering, sequential triggering, pattern triggering ANDed with a transition or glitch, glitch triggering, plus other modes that simplify the analysis of handshake problems.

In software test and debug, the 64110A gives you unequalled tracing, triggering, and store qualification power. With its master enable function, 16-level sequencer plus 8 user-definable terms for trigger, store qualification and count functions, you'll have little trouble locating the specific portion of code you want and displaying only the information of interest...even in the most complex multiprocessor software.

For system performance analysis, the 64110A gives you a nonintrusive view of software in action in the form of histogram and graph displays. The histogram modes provide a fast way to locate system bottlenecks and identify inefficient portions of software. These display modes help you identify a processor stuck in a loop, see where software went into the weeds, or spot activity occurring in a forbidden area. A graph mode shows software performance data in chronological order.

Interactive measurements between all analyzer subsystems multiplies the power of the 64110A far beyond the capability of other logic analyzers. Cross arming and triggering between any of the analyzer subsystems helps identify the source of difficult hardware/software interaction problems, and resolves hardware/software fingerpointing issues.

In any phase, the 64110A is a pleasure to use. Directed syntax softkeys guide you through setups and measurements with a minimum of keyboard entries. Symbolic tracing means you interface with the analyzer using terminology you're familiar with. And preprocessors with inverse assemblers let you view measurement results in familiar processor mnemonics. All of which lets you concentrate on the problem you're trying to solve...not the analyzer.

## Choose both and you'll have your analysis needs covered.

When you combine both of these analyzers in your lab, you have a cost-effective solution to the day-to-day test and debug tasks, plus the power to deal efficiently with those complex troubleshooting jobs.

So before you buy any logic analyzer, be sure you explore the individual power of HP's standalone analyzers...and the synergistic effect of a combination of instruments.

For complete details, call your local HP sales office listed in the telephone directory white pages. Ask for an HP field engineer in the electronic instruments department.

*U.S.A. list price only.

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CIRCLE 22

D201304

# HOW TO CHOOSE A DISK DRIVE, PART II:

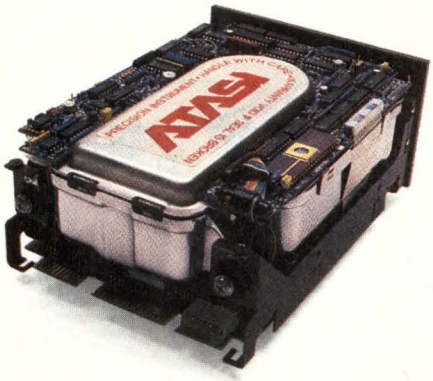
# Your new computer system may be in for a cool reception.

Here's a cold, hard fact that should influence your selection of a disk drive for multi-user computer systems or local area networks: In today's energy-conscious offices, temperatures can vary enough during the day to affect the performance of a disk drive. We made the operating range of ATASI drives up to 25% greater than most competitive drives because poor performance under thermal stress can result in system downtime and even lost data. Here's how it happens.

In most drives, the bottom of the bowl serves as the base-plate where the carriage and spindle assemblies are

# STRESS

mounted. There is no thermal isolation. Heat from the motor, PC boards or a power supply can result in differential expansion of the baseplate, so that it temporarily warps. This can change the alignment of the carriage and spindle, which in turn affects the drive's ability to find data reliably.



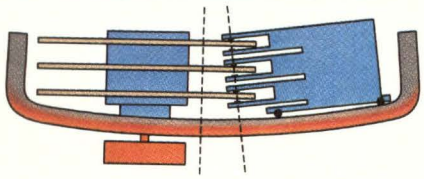
*ATASI's 46 Mbyte, 5¼-inch Winchester disk drives are available in production quantities immediately.*

### Alignment problems

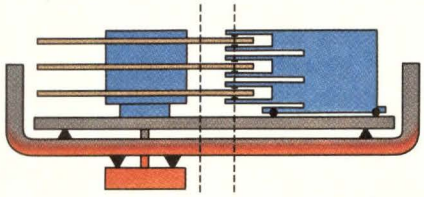
In high-performance, closed-loop drives, servo information carried on the bottom surface of the disk stack is used to position the data heads on all other surfaces. Assume that data is recorded when the drive is "cold." If the carriage and spindle go out of alignment when the drive gets "hot," the servo system cannot properly position the read/write heads to recover the data. This may mean that data written in the morning won't be accessible the same afternoon!

### Thermal isolation

To prevent this from happening with ATASI's 5¼-inch Winchester disk drives, the ATASI design incorporates a baseplate which is separate and thermally isolated from



*Heat can temporarily warp a drive's baseplate, causing alignment problems between carriage and spindle.*



*Thermal isolation in ATASI's proprietary design eliminates the problem.*

the lower half of the bowl. The baseplate is therefore protected from external sources of localized heat. Even if the drive heats up, it does so uniformly, with no resultant deformation of the baseplate, and no alignment problems.

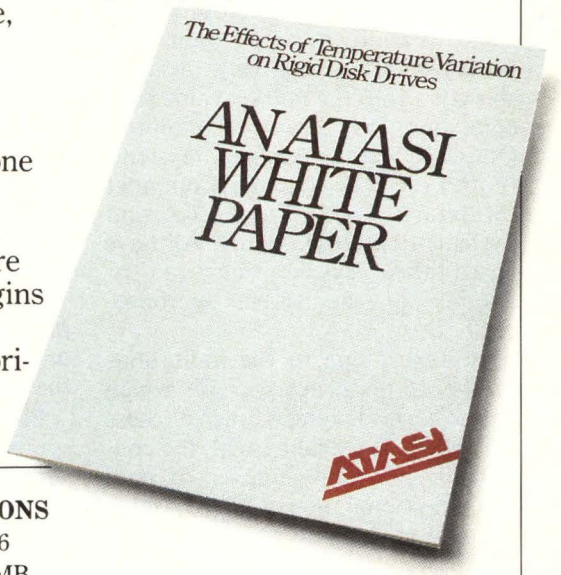
### Extra margins

Thermally isolating key mechanical components is one way we improve the performance of ATASI drives, but not the only one. Everywhere in the design there are margins of safety other drives don't offer. For example, our proprietary spindle motor design provides substantially greater dissipation of heat away from the disk module than competitive drives.

### The ATASI White Paper

At ATASI, we are proud of the quality we build into every drive we make, and we encourage clients to test our products rigorously. To help, we have prepared a White Paper on thermal testing which discusses test methods and interpretation of test data in detail.

If you are a systems integrator, contact ATASI Corporation now to receive your ATASI White Paper. Corporate headquarters: 2075 Zanker Road, San Jose, CA 95131, (408) 995-0335; Eastern region: (617) 890-3890; Southwest region: (714) 432-0757.




**PERFORMANCE SPECIFICATIONS**

| MODEL NO. | 3033 | 3046 |
|---|---|---|
| CAPACITY | 33 MB | 46 MB |
| ACCESS TIME (AVG.) | 30 ms | 30 ms |
| DATA RATE | 5 Mbits | 5 Mbits |
| INTERFACE | ST 506 | ST 506 |

Available in high volume today.

| MODEL NO. | 3065 | 3075 |
|---|---|---|
| CAPACITY | 65 MB | 75 MB |
| ACCESS TIME (AVG.) | 24 ms | 24 ms |
| DATA RATE | 5 Mbits | 5 Mbits |
| INTERFACE | ST 506 | ST 506 |

Available second quarter, 1984.

ATASI

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# Fault tolerant systems deal with increased loads

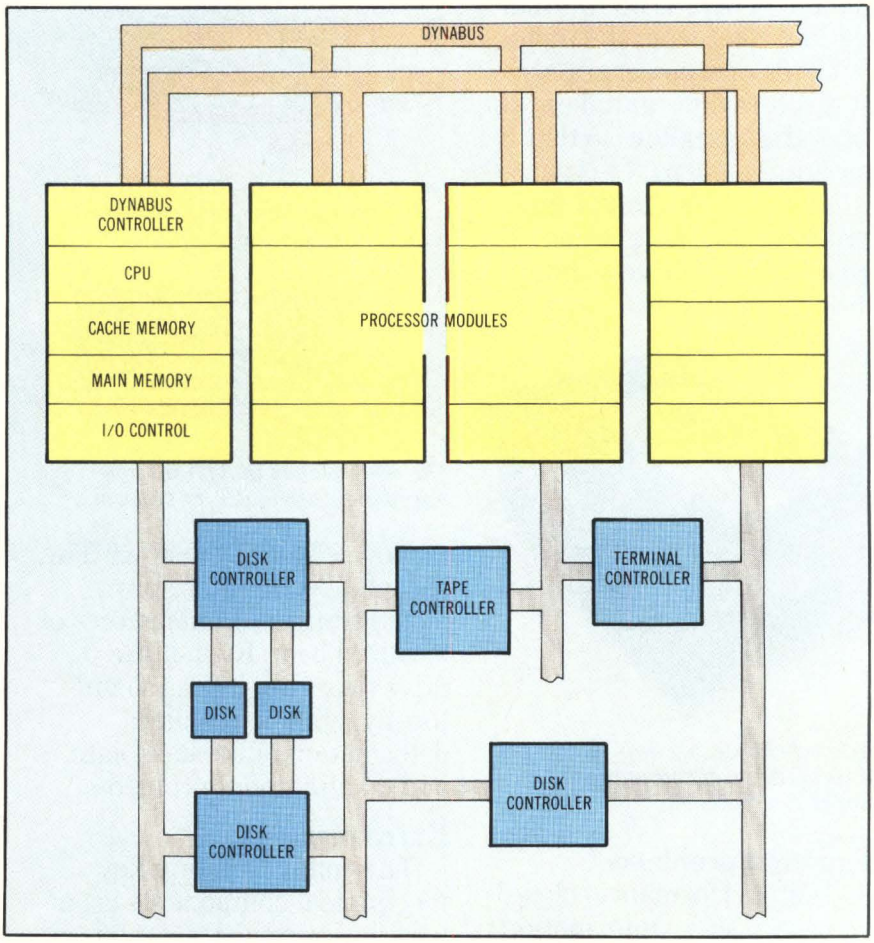
Moving away from batch processing central computer systems, the transaction processing market has grown by leaps and bounds. In the move, these systems have become distributed. Remote sites continually transmit data to one another or to the central site. To ensure continued operation of both the systems and the links, fault tolerant systems came into being.

Tandem Computers (Cupertino, Calif), was not only the first to recognize these needs—and supply a method of preventing a single failure from stopping the system—but the fastest in responding to increased demands. The company's entry into this field, the NonStop system, was based on redundant 16-bit processors. As the demands for such reliable systems grew, additional vendors moved in to fill their need for increased distributed systems and the growing work load.

With the 16-bit microprocessor came the ability to supply redundant processors at a relatively inexpensive cost. Into the market came such companies as Stratus Computers (Natick, Mass), Auragen Systems (Fort Lee, NJ), Synapse Computer (Milpitas, Calif), and Tolerant Systems (San Jose, Calif). All have based their systems on one or another of the 16-bit microprocessors.

However, due to the limitations of the 16-bit processors on which they are based, systems such as these have difficulty dealing with the continually expanding masses of data and additional users, all of which demand reasonable response times. Tandem's recent upgrade, the NonStop TXP, builds on 32-bit minicomputer technology to answer these needs. Tandem's architecture depends on total redundancy. Multiple processors, dual-bus communications, dual-ported controllers, and multiple power supplies are inherent.

All processors independently process different applications, instructions, and I/O operations in parallel. However, if a module or data path fails, its counterpart automatically takes over to complete work in progress. The faulty part can be replaced or repaired without shutting down the system.




**Tandem's NonStop TXP eliminates single points of failure through total duality. If any module or data path fails, its corresponding device or alternative data path automatically takes over to complete the function.**

Each processor module is a 32-bit computer with a 32-bit native addressing mode and a 64-bit path to main memory. Each processor has its own 64-Kbyte hardware cache memory, and each can address 1 Gbyte of virtual memory.

Using three levels of instruction overlap achieves computational performance. This allows the processor to fetch one instruction and preprocess a second while executing a third. The CPU cycle time is 83 ns. Based on a 98-percent cache hit rate, effective memory access time is 116 ns.

From 2 to 16 processors are accommodated in a single system. From 2 to 14 systems are linked through a 4-Mbyte/s fault tolerant fiber optic interface to form a local network. Geographic dispersion is handled through networking software.

The system's 64/32/dual 16-bit design allows application programs written for any NonStop system to run on the TXP. Transfer requires no changes in code and results in two to three times greater throughput.

### Gaining data integrity

Each CPU supports one to four 2-Mbyte memory boards. Control signals between the CPU and memory are continually checked. Single-bit error correction (SEC) and double-bit error detection (DED) are performed on data; single-bit error detection (SED) occurs on addresses.

Among the system's data integrity safeguards are validation checks that are performed by operating system

*(continued on page 43)*

# Fill in your IBM micro/mainframe communications picture.

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AST keeps pace with your ever-changing applications requirements with reliable, high quality, cost effective communications products. AST products provide support for Bisync and SNA/SDLC communications protocols as well as networking multiple PC's for sharing resources.

CIRCLE 24

## Choose AST products — by the numbers.

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3. **AST-PCOX™** allows your PC to connect to an IBM 3274/3276 cluster controller via coax cable and emulates a 3278 or 3279 display terminal.
4. **AST-3780™** emulates 2770, 2780, 3741, and 3780 RJE workstations using Bisync protocol.
5. **AST-5251™** emulates a 5251 Model 12 remote workstation connected to an IBM System 34, 36 or 38.
6. **PCnet™** is the first Local Area Network designed specifically for the IBM PC or XT and the PC-DOS 1.1 or 2.0 operating system.
7. **CC-232™** is a user-programmable dual-port card capable of communicating in Async, Bisync, SDLC, or HDLC protocols.

Discover how well AST can fill in your micro/mainframe communications picture. For descriptive data sheets, write or call: AST Research Inc., 2121 Alton Ave., Irvine, CA 92714. (714) 863-1333. TWX: 295370ASTRUR

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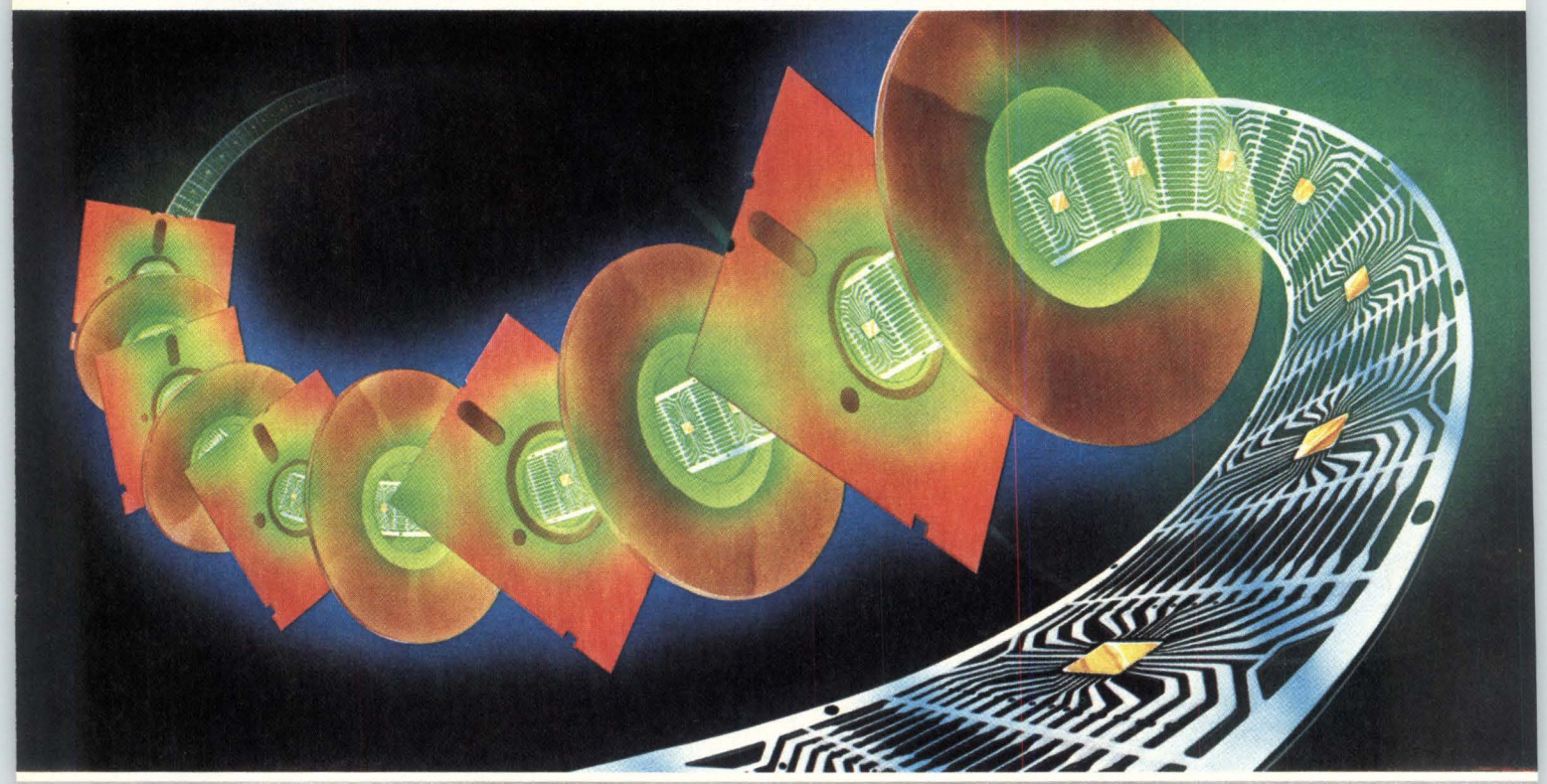
# SSi–INNOVATORS IN DISK DRIVE INTEGRATION



**We've delivered more read/write IC's than everyone else combined, but we're not satisfied.**

Everyone knows that Silicon Systems dominates the market with read/write IC's for 14", 8", 5-1/4", and smaller Winchester disk drives. What they may not know is that we're not satisfied to stop there. Although our present line of rotating memory circuits includes much more than read/write IC's, we won't be satisfied until we completely integrate Winchester disk drive electronics. And we are continuing to expand the industry's most complete line of "Applications Specific" IC's for Winchesters, Floppies, and Tape Drives.

**We're also the leading innovators in custom IC's for use with mass storage systems.**

In addition to our broad line of standard circuits, we have developed a host of innovative custom IC's for use with a variety of mass storage systems. We have produced custom IC's for read/write electronics, spindle motor control, analog data processing, digital bus interface, and servo control functions.

For rigid and floppy disk drives, or tape back-up systems—if the circuit you want isn't in our standard line, we have the capability to produce it for you. We have the analog and digital design capability, the Bipolar and CMOS process technology, and the rotating memory IC experience to make the exact custom chip your system needs.

For more information on our standard products and custom capabilities, send for our "Rotating Memory Integrated Circuits" brochure.

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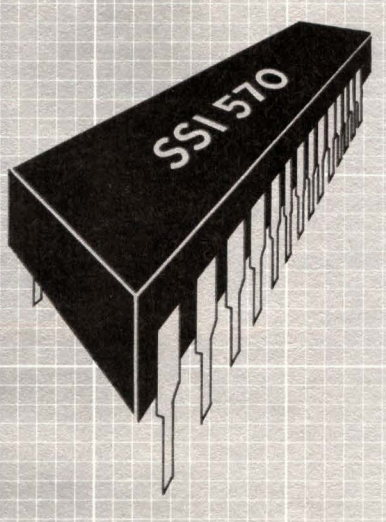
INNOVATORS IN INTEGRATION

CIRCLE 154

NEW
HI-PERFORMANCE
FLOPPY DISK
CIRCUIT




Silicon Systems' latest innovation in disk drive integration is the SSI 570. This creative design by Silicon Systems engineers integrates both the read and write data processing functions on one, 2-channel, monolithic IC. The circuit is designed for use with 8", 5-1/4", and 3-1/4" double-sided floppy disk drives.

The write data circuitry includes the erase head drive with programmable delay and hold times, and the read data circuitry includes low noise amplifiers for each channel. This TTL compatible circuit operates on +5 and +12 volts and is provided in a 28-pin plastic DIP package.

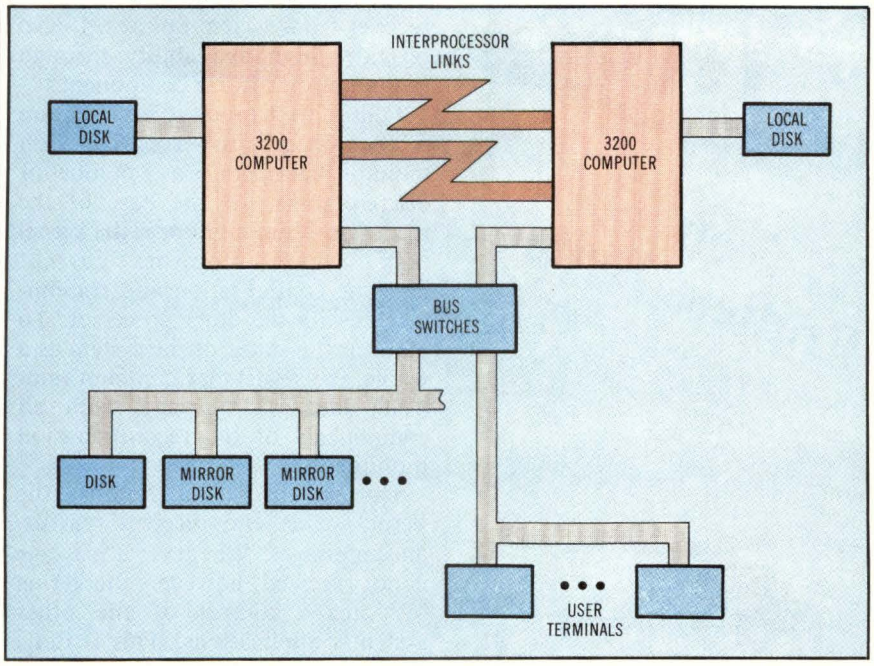
For more information on this new advanced product from the leader in disk drive integration, contact: **Silicon Systems,** 14351 Myford Road, Tustin, CA 92680, **(714) 731-7110** Ext. 575.

silicon systems
INNOVATORS IN INTEGRATION

CIRCLE 155

**Fault tolerant systems**

*(continued from page 40)*




**Perkin-Elmer's Resilient system combines redundant hardware components with reconfiguration monitor software. In addition, it allows independent operation of processors while providing either with the capability to take total control if necessary.**

software on data transfers. System-level safeguards include parity checking on data paths, checksums on bus transfers, and SEC/DED on data in memory. End-to-end checking ensures that messages are transmitted correctly.

To this end, the CPU includes parity prediction algorithms for a program counter, an interval timer counter, and a microcode address incrementer. Parity checking occurs on critical data paths. Buried in microcode is a function that freezes the CPU when a hardware fault is detected.

### Success breeds competition

Traditional minicomputer vendors have also recognized the potential to expand into this market. Mid-1983 found Digital Equipment Corp (Maynard, Mass) entering the arena with its VAXcluster. Using multiple VAX processors and intelligent storage subsystems connected through a star coupler, the concept enables all components to function as a single system. Serving as the basis for the system, the star coupler connects eight nodes through computer interconnect bus cables. To provide redundant 70-Mbps data paths, each bus consists of two transmit and two receive cables.

Processors connect to the bus through intelligent controllers. The interface uses whatever path is available. This enables high throughput to be achieved when both are available. It also allows one path to handle all traffic if one becomes unavailable. All traffic is automatically shifted to the available path when one is unavailable.

Integral to cluster operation, VAX VMS operating system software versions 3.3 and 3.4 have provisions for dual-ported disks between storage controllers. Other releases take advantage of the hardware's data protection and fault tolerance potential, thus enabling the system to survive and reconfigure around failed components.

Attempting to outgun Tandem, Perkin-Elmer's Data System's group (Tinton Falls, NJ) has put its 3200 series machines together with database software to form what it calls the Resilient system. The system combines existing 3200 series superminicomputers with software designed to automatically sense and

*(continued on page 44)*

Full Story:

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12



### Fault tolerant systems

*(continued from page 43)*

recover from system failures. It also provides high availability through redundant hardware components.

Central to the fault tolerant nature of the system is the reconfiguration monitor that operates as a number of discrete tasks. At the base of the reconfiguration monitor is the kernel task, which monitors current machine configuration and communicates with the other processor. To monitor the status of the system as a whole, the kernel task communicates using intertask messages with all components of the reconfiguration monitor.

During normal operations, the kernel sends and receives reassurance messages. Whenever a message is not received, however, the kernel task takes control of the other system's applications. This is done by running command substitution system (CSS) files to acquire necessary peripherals and then running other CSS files to load and start the application.

The monitor runs in both computers. On detection of a failure in the other system, the monitor activates bus switches to take over peripherals from the failed system and performs actions to load and restart the failed application or system. The monitor can act on operator commands to reconfigure the system for normal engineering maintenance.

These systems have eliminated the necessity for maintaining a "hot standby" to protect transactions. By allowing each processor to handle tasks independently, throughput remains high until a problem develops. Meanwhile, these systems offer assurance that all transactions can be completed and that the integrity of the data base will be maintained should a component within the system fail.

*—Peg Killmon, Senior Editor*

## SOFTWARE

# Multipass compilers produce tight code

Compilers generally go through two stages to produce tight object code. In the first stage, a front end processes a text file that contains source code. Its output is in an intermediate language (IL) not specific to any given CPU architecture. Often as part of the compiling process, a global optimizer processes the IL. This process examines the whole program to identify parts of the code that can be combined or eliminated.

The optimized IL is then passed to a back end that generates object code for a specific CPU. The object code is then scanned by a peephole optimizer. This optimizer, in turn, scans small chunks of code (typically 6 to 12 instructions) to speed up loops, and make the best use of the CPU registers.

Optimizers and optimizing compilers have been available in the academic and scientific world for a number of years. They were mainly written in-house and aimed at specific processors, such as the CDC Cyber Series and the Illiac parallel processor. However, these tools were not easily available to outside designers, nor were they adaptable for use with other CPUs.

### Optimizers add speed to applications

Block-structured languages (principally C, Pascal, and Ada) have by and large taken over from Fortran and Assembler in scientific and engineering applications. At the same time, compiler writing technology has become much more sophisticated, and users are demanding and getting more efficient tools from language vendors. Memory space is no longer a critical issue in microprocessor development, but speed is, and an optimizer can speed up an application program significantly.

In the mainframe and supermini world, several semiconductor houses, including Intel (Santa Clara, Calif) are using Mainsail, a block-structured language and operating system from Xidak, Inc (Menlo Park, Calif), as the underlying language for their computer aided

*(continued on page 46)*

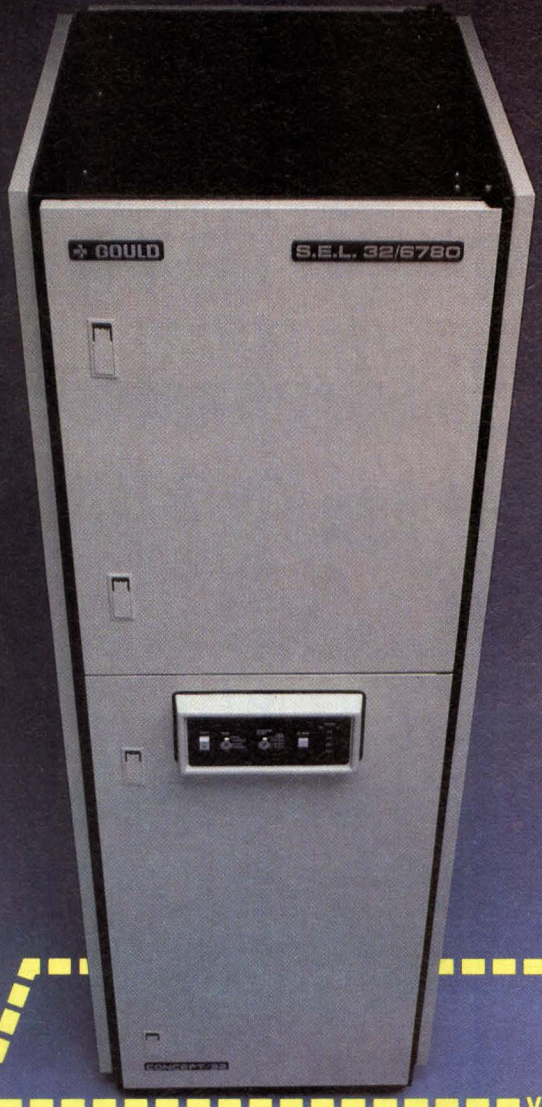
*Gould...Innovation and Quality in Computers*

# We just gave the computer industry something to reach for. A new standard... performance/footprint.

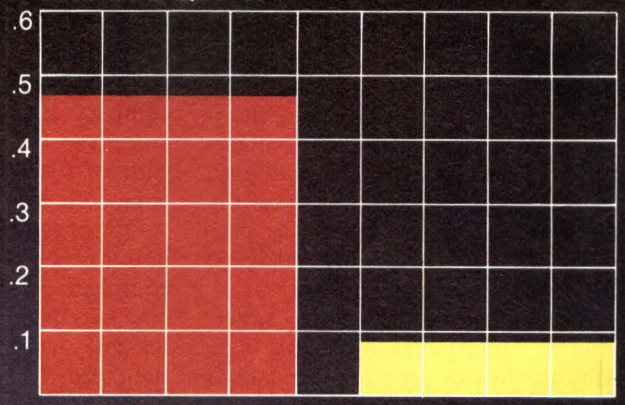
**Introducing the Gould CONCEPT 32/67. Performance in a size as accommodating as its price.**

From the 32-bit performance leader comes yet another minicomputer product line other suppliers can only hope to duplicate. The 2-MIPS-class, cost and space-saving CONCEPT 32/67.

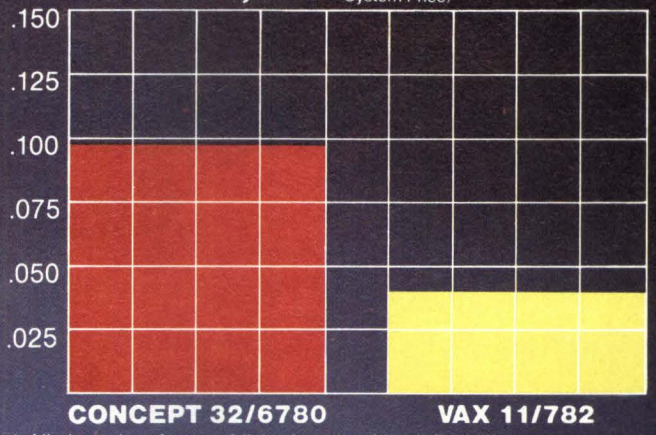
We scrimped on size, but that's all. The 32/67 gives you top computational power in 1/5 to 1/3 the floor space of the competition. And it's packed with features. Performance up to 2.6 MIPS. Largest cache in a mini ... 32K byte two-way set associative with separate 16K banks for data and instructions. And, 16M byte task addressing in a base register mode. All at a price that matches its size.



**MIPS/SQ. FT.***




**MIPS/$10,000** *(Equivalent System Price)




* All chart data from published competitive information.

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*Electronics*

CIRCLE 27

**Multipass compilers**

*(continued from page 44)*

design/computer aided manufacturing applications. The language runs on the IBM 370 architecture (machines from IBM, Amdahl, and others), as well as on superminis from Digital Equipment Corp (Maynard, Mass), Apolio Computer (Chelmsford, Mass), Sun Microsystems, Inc (Mountain View, Calif), and Ridge Computers (Santa Clara, Calif).

An optimized IL file produced on any one of these machines can be transported to any of the others, converted to object code, and run without change. Since it deals with only one source language, the Mainsail IL optimizer is not particularly general. According to the company, however, the IL itself was carefully designed to be as versatile as possible, so that code could easily go from one machine to another.

On minicomputers and supermicros, Intermetrics (Cambridge, Mass) provides separate front ends to compile its Pascal and C languages to an optimized IL. The front ends also provide back ends to generate object code for the Motorola 68000 or the Intel 8086 family CPUs.

In describing a source-level debugging system that Intermetrics developed in conjunction with Gould Inc, SEL Computer Systems Div (Fort Lauderdale, Fla) to run on a microprocessor development system (see this month's staff report by Tom Williams, p 149), Ron Kole, president of the Software Products Div at Intermetrics, points out that it is possible to do too much optimization. Multipass optimizers that compact and speed up code by any given factor are well within the state of the art of modern software engineering.

Optimizers slow down the compilation process. They also change the compiled code, so that debugging, whether by hand or automatically, becomes harder. Unless special data structures for ports and toggles are built into the compiler, memory references that signal the hardware to do something may be eliminated by the optimizer when it finds that the data is not used anywhere in the program.

For this reason, a balance must be struck between doing too much and too little. Eliminating dead code and common subexpressions (ie, doing the same address calculation several times at different places in the program), doing only as much calculation as absolutely necessary to evaluate Boolean expressions, and doing constant arithmetic at compile time all speed up a program. Doing too much can distort the program structure to the point where it no longer does the job for which it was designed. Both the compiler writer and the end user have to use good judgment in deciding how much or how little optimization to do on any given program.

TeleSoft (San Diego, Calif) also uses an IL in the Ada compiler it offers for various microprocessor


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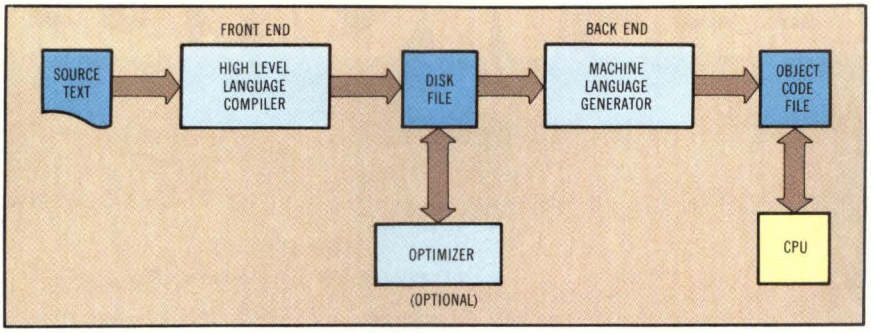
CIRCLE 145




**Intermediate language (IL) representations of high level language programs make them more general and more transportable. Optimizers for the IL and object code, working with the back end, tailor the program for a variety of CPUs.**

architectures. According to Tom Dent, the company's president, this was seen as the only practical and cost-effective way to support the large number of machines that would be running Ada.

It is also seen as a way to maintain flexibility for future growth in directions other than Ada. While declining to talk about any specific future products, Dent stated that TeleSoft is not exclusively committed to Ada, and would consider supporting other languages and applications in the future. New architectures (32-bits and up) are also being developed, so separating high level language parsing from the generation of machine specific object code is a necessity.

### Is a standard IL impossible?

All intermediate languages are individual. There is no "standard intermediate language," just as there is no "standard computer architecture." One school of thought in computer science maintains that a standard is impossible—that in order to generate efficient code, there must be a correspondence between the IL and the architecture of the machine on which it will run.

Others maintain that if enough information on both the language and the ultimate machine architecture is provided to the compiler and the optimizer, that satisfactory (and even excellent) code can be generated for any program in any language on any machine. Neither point of view can be shown to be absolutely correct, but widespread use of both IL and optimizers can be expected to increase dramatically in the future.

*—Sam Bassett, Field Editor*

**SYSTEM TECHNOLOGY**

*(continued on page 49)*


# World-Class Components Update:

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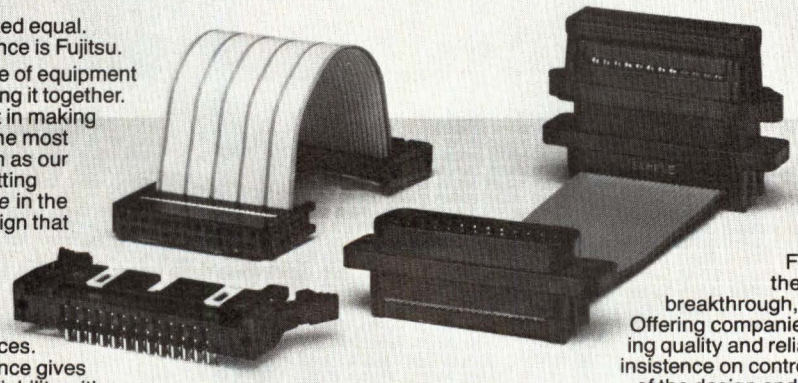

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CIRCLE 146

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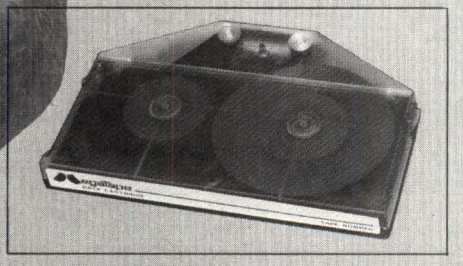

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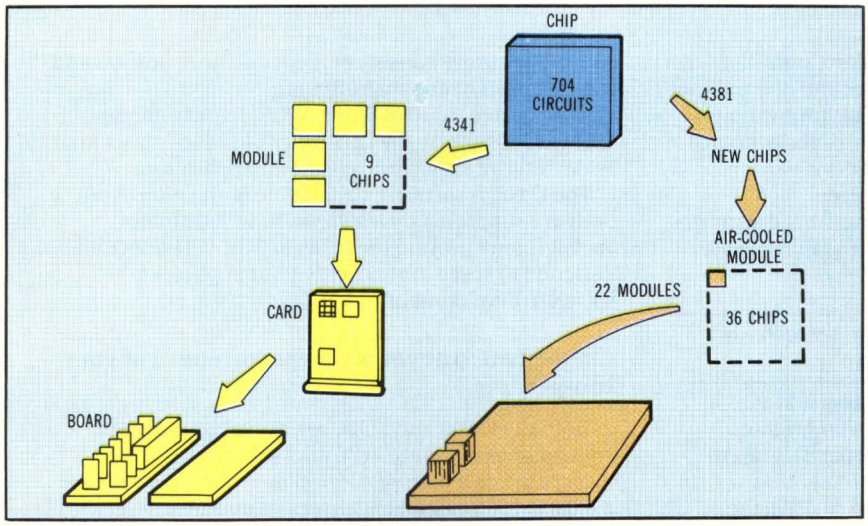
# IBM packs high density circuits in and lets them breathe

Packaging plays a critical role in the computational performance of IBM's mid-range 4381 processor. As a result, the new computer provides up to three times the performance of its predecessor—the IBM 4341—while not requiring air conditioning for cooling. The company uses an air-impingement cooling technique that yields twice the million instructions per second (MIPS) per kilowatt of power that was obtained from the 4341 machine. As a result, the individual power densities at the component level increased fivefold.



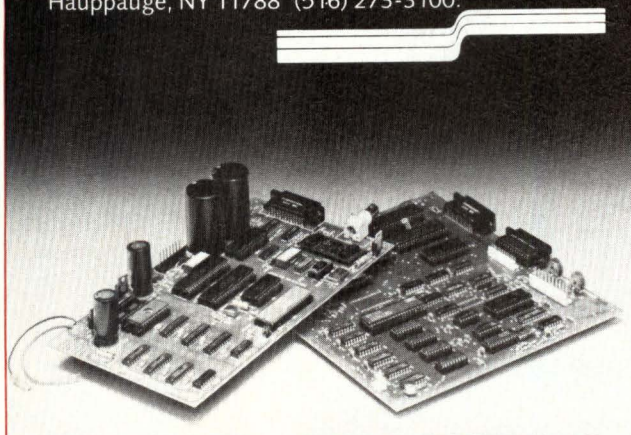

**By implementing a novel packaging technique, IBM engineers were able to eliminate the card, which is still part of the 4341 computer package. More than 200,000 circuits are interconnected on the 4381 board. This is twice the number that was wired on the 4341 board.**

The densely packed circuits eliminated the need for an entire level of packaging. As opposed to the chip-on-module-on-card-on-board hierarchy used in the 4341, the 4381 has the chip mounted in modules. These modules are in turn stacked on a single board, thereby eliminating the card entirely. To top it off, the 4381 has twice the number of circuits in each module that the 4341 had on a card. More than 200,000 circuits are interconnected in 22 air-cooled modules. Three major components make up each module: a cooling assembly, the substrate chip carrier, and up to 36 chips containing about 700 circuits. .

*(continued on page 51)*

OUTSTANDING STAND-ALONE BOARDS.

SMC's Stand-Alone boards stand out in the crowd. Our **HAWK I** Video Terminal Board provides all the circuitry to build a "SMART" CRT Terminal, featuring enhanced video attributes and screen editing capabilities. Our **ARCNET-LINK** Board connects any computer with an RS-232 port to a high-performance ARCNET® local area network. For complete details, contact Standard Microsystems Corporation, 35 Marcus Boulevard, Hauppauge, NY 11788 (516) 273-3100.



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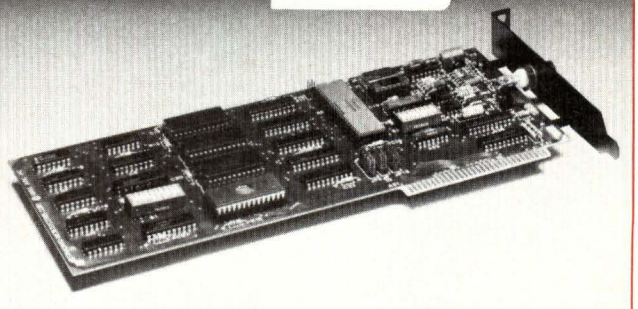

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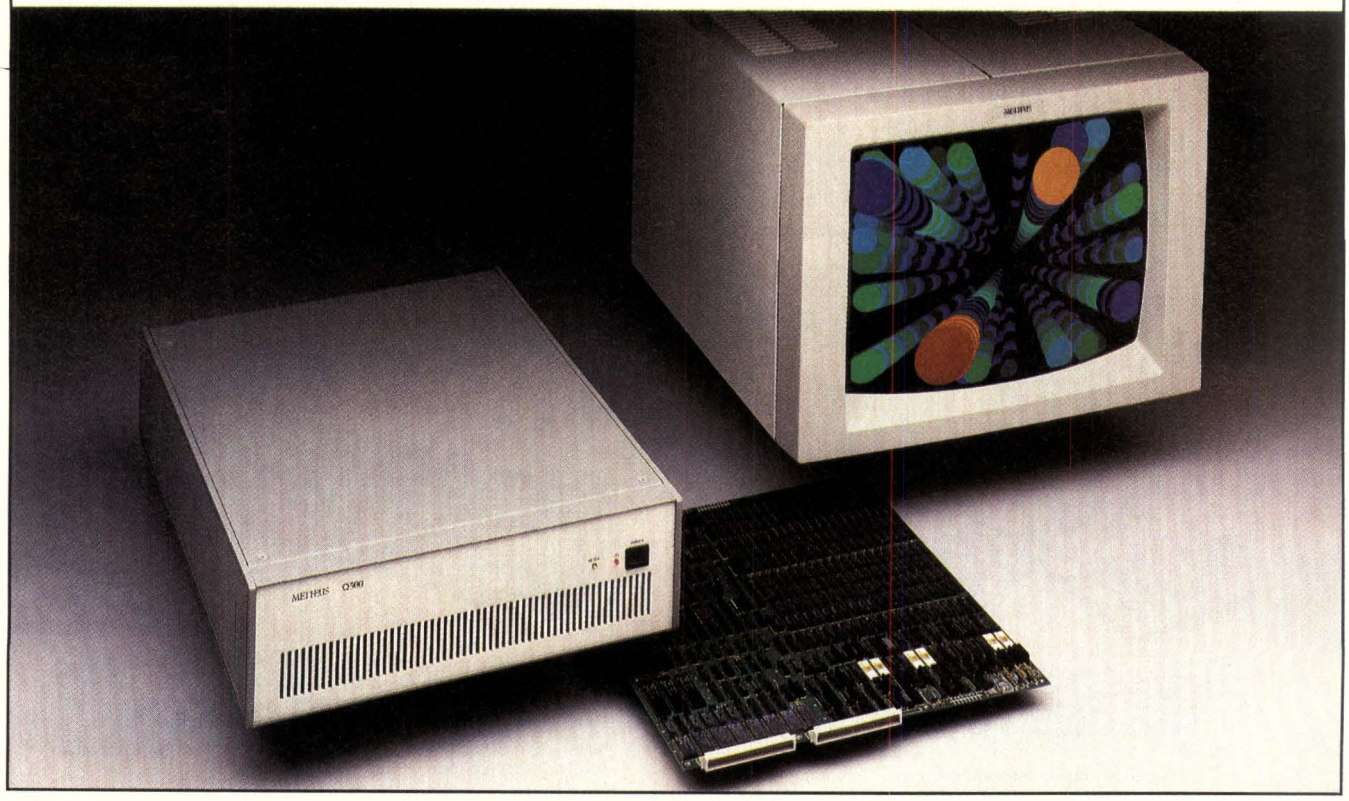
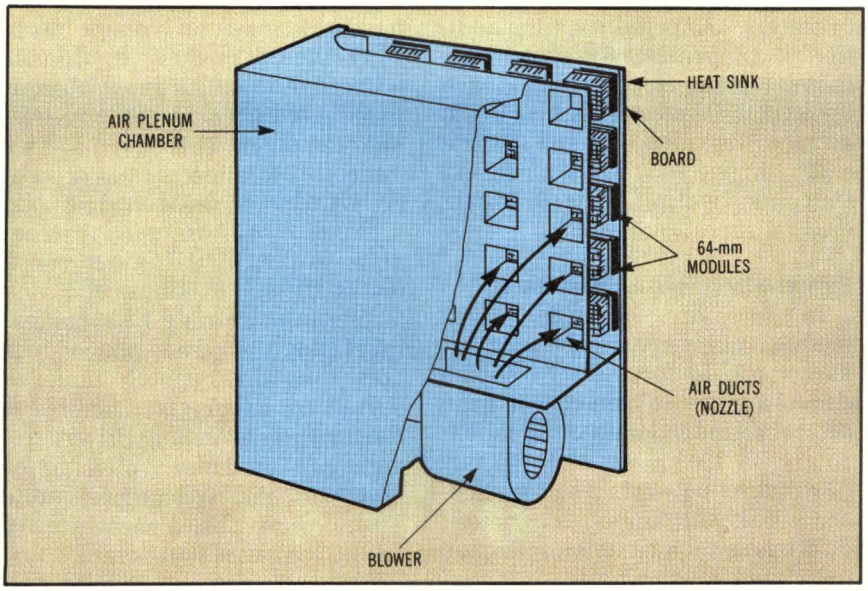



CIRCLE 31

**High density circuits**

*(continued from page 49)*




**Cooling this compact mass is an air impingement mechanism with a blower that directs air simultaneously through nozzles. The air hits the circuit board in a perpendicular direction.**

To cool these circuits, a blower supplies room air to a plenum chamber and directs the air simultaneously through nozzles (arranged in parallel rows) to all the modules plugged on the circuit board. Air impinges on the modules in a direction perpendicular to the circuit board at velocities over 10 m/s. It then exits near the base of each heat sink at the low velocity of 1.5 m/s into channels that lead to the periphery of the computer console. There are two primary advantages that parallel impingement has over serial cooling, according to IBM engineers. First, each module receives fresh air without having been heated by adjacent modules. Second, no air conditioning is required.

Specially designed heat sinks further enhance the external cooling of the modules. In turn, chips in each module are cooled again in parallel with direct heat pads provided by the thermal paste placed between each chip and the module cap. The 4381 module can accommodate up to 36 chips in a 6 x 6 arrangement on a 64-mm ceramic substrate. High powered chips are judiciously placed on the substrate based on thermal considerations. It is then solder-sealed against a ceramic cap that is fitted with an aluminum heat sink.

*(continued on page 52)*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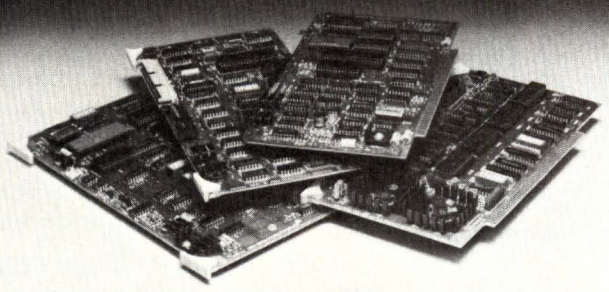

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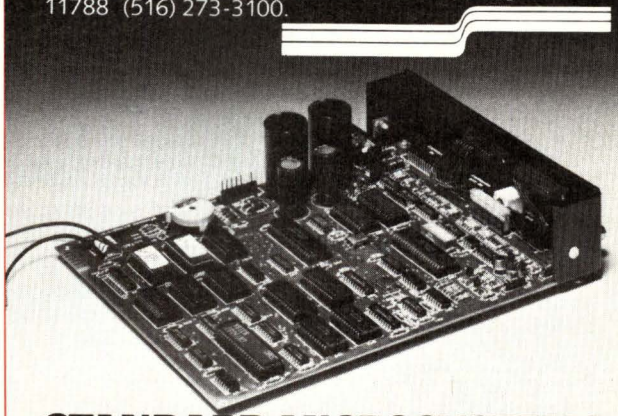

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CIRCLE 163

### High density circuits

*(continued from page 51)*

IBM engineers say that they owe much of the success of the 4381's heat dissipation to computer modeling that was done during the design stages. The modeling helped engineers decide how to partition and place the chips—to remain below maximum allowable junction temperatures, and above the specified minimum temperature. In the 4381, some chips are qualified to 90 °C, others to 85 °C, and all are specified not to operate below 25 °C.

For this type of configuration, high powered chips are designed for placement on the module's periphery to take advantage of the proximity to the cap walls. These walls provide additional cooling paths to the heat sink. In the same manner, chips are allocated according to computed specifications to minimize temperature differences between them. This also reduces electrical noise.

The thermal model was verified against measurements made on actual modules. It can predict beginning-of-life and end-of-life operating temperatures. In addition, it compensates for appropriate thermal parameters as determined by several different tests performed on many test modules. The tests include impact, vibration, shock, thermal cycling, mechanical/thermal shock, and others.

### High density means minimum noise

In such a highly integrated module, noise control becomes of paramount importance. Noise can come from several sources, and can act either individually or simultaneously, in the power or the signal distribution network. The IBM engineers dealt with four types of noises: dc drops, switching noise, reflection noise, and coupled noise.

In general, circuits must be able to tolerate dc drops in the power distribution network in addition to any ac noise generated in the package. Efficient placement of power pins optimizes dc drops. In the 4381 module, each chip site is supported by exactly seven power pins and all have the same dc voltage drops. Thus, the 4381 module's dc drops are 44 percent less than those observed in the predecessor module in IBM's 308X computer. This advantage was traded off to allow greater drops in PC board and more on-module noise.

Driver transistors cause a second noise source in the power supply that is difficult to control and could in this instance only be minimized by placing the power pins at locations that would cancel mutual inductances. Keeping the number of concurrently switching drivers to a minimum can limit the effect of this noise on the system-level noise. This, however, has a negative effect on the computer's MIPS rate.

Both reflection and coupled noise are a result of a poor signal-distribution network. Reflection noise was greatly reduced by the package's sheer density. In terms of reflection noise exposure, the 4381 is a vast improvement over the 4341. This is due, in part, to the increased number of circuits on a first-level package. Couple that with no cards and just one board, and the result is fewer transmission line-type problems.

Mutual capacitances and inductances of nearby conductors cause coupled noise. In turn, active lines coupling into a quiet line can cause false switching. IBM claims that rules have been written for its design automation system to limit coupled noise. Power switching noise and coupled noise can occur simultaneously. But, in terms of system noise tolerance, if the sum of the four noise sources remains below the individual circuits' noise tolerances (but not so low that it causes the machine to operate below its potential), then the computer is said to be working at its highest efficiency.

In general, as computers become more integrated and clever packaging techniques are found (eg, the 4381 system) engineers must pay very close attention to noise allocation from the inception of their design.

*—Nic Mokhoff, Senior Editor*

**February Preview**
*Special Report on Data Communications*


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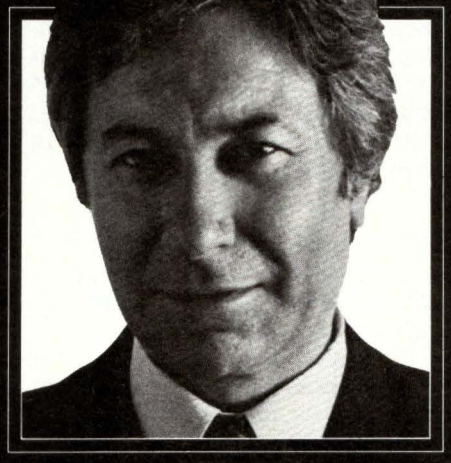

*– Napoleone Cavlan*
*Director of New Product Development,*
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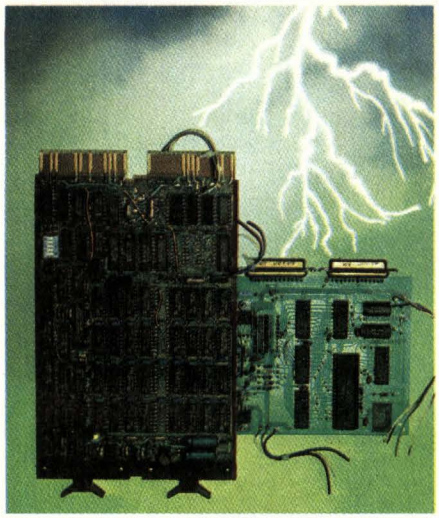

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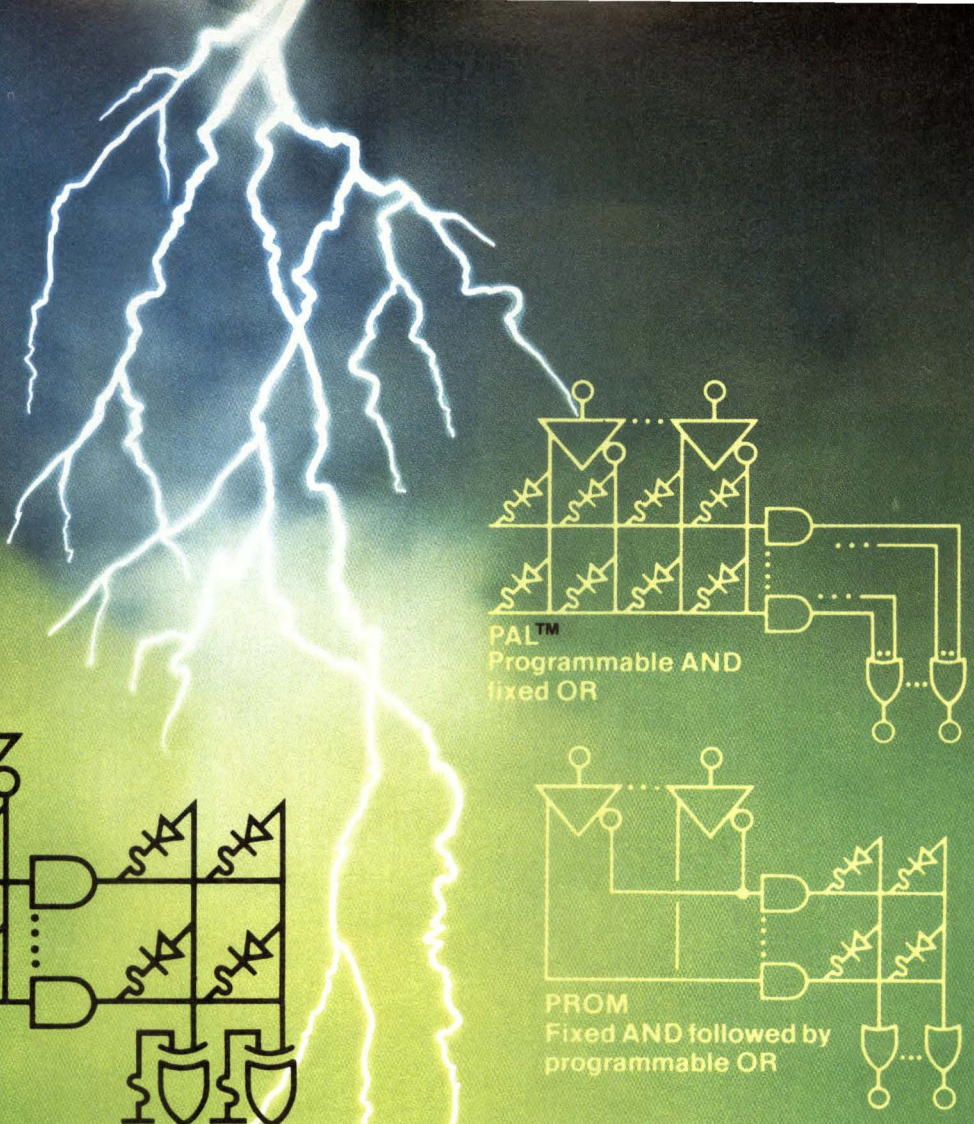


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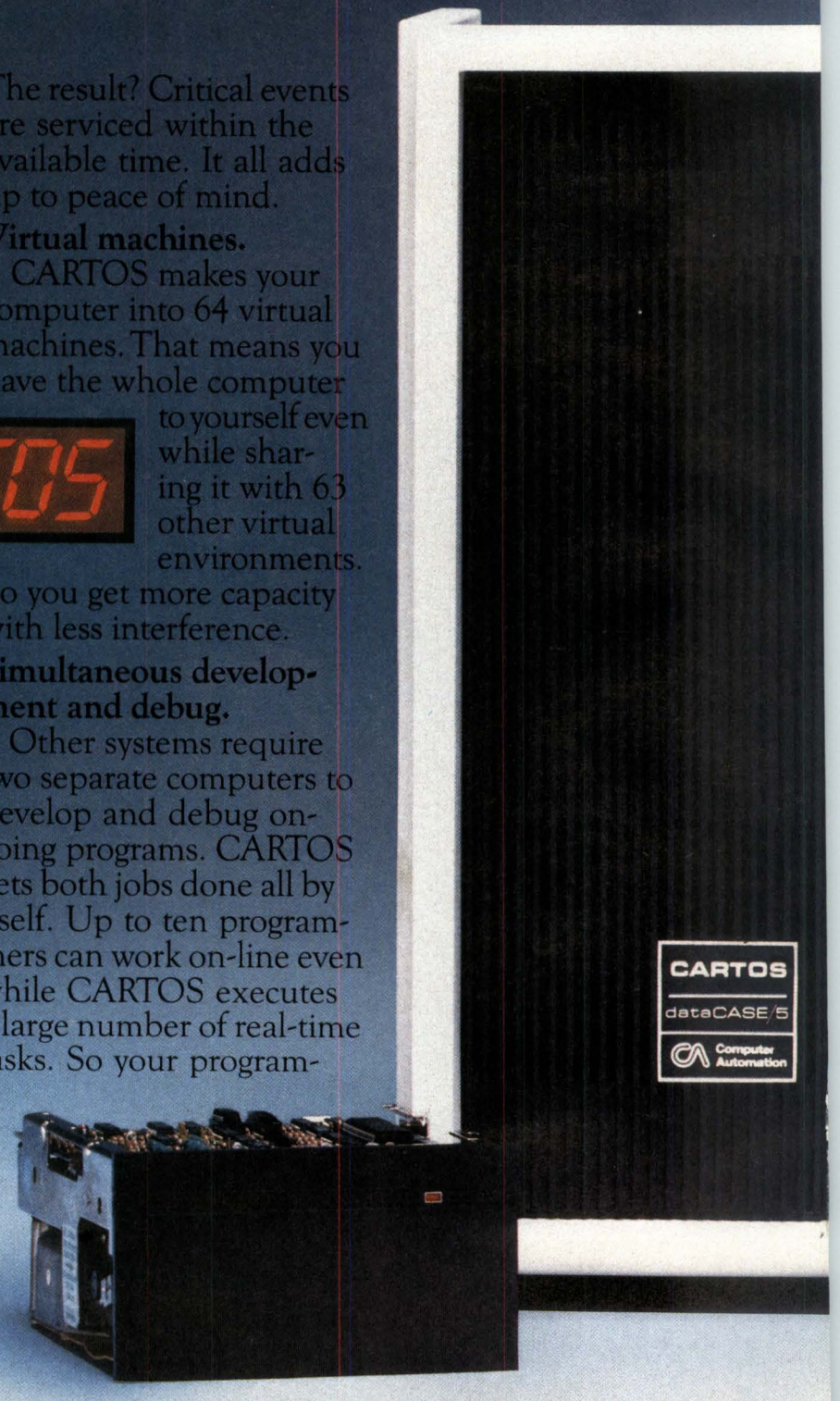

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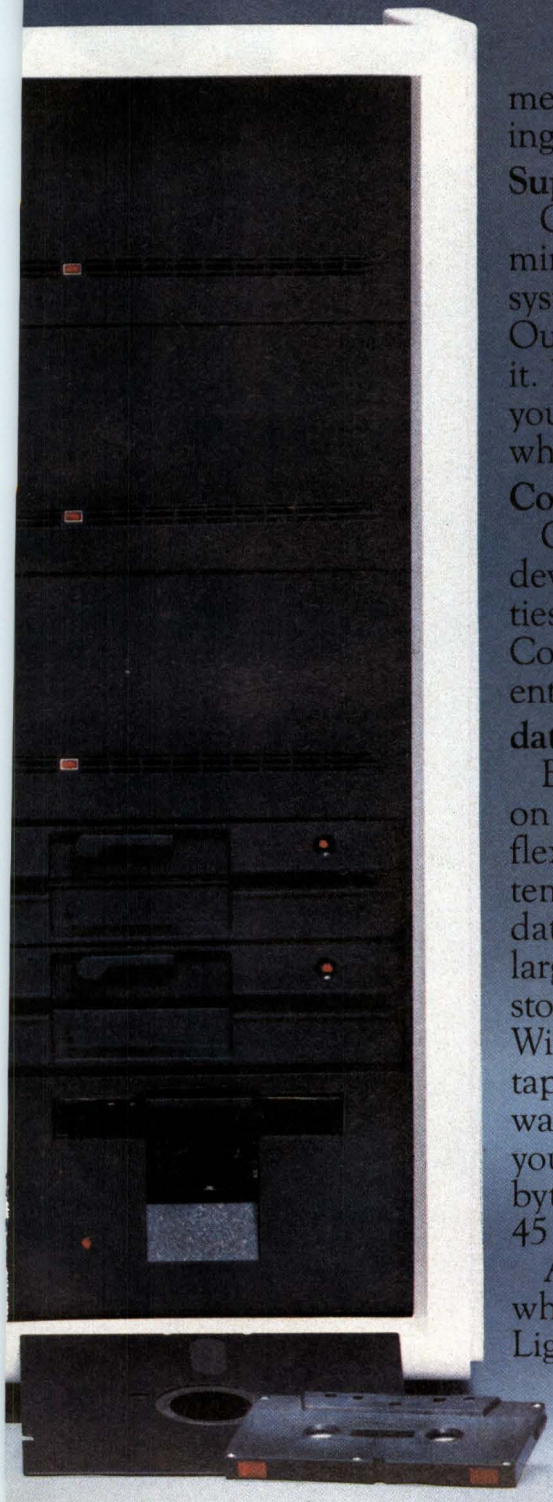

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CIRCLE 36

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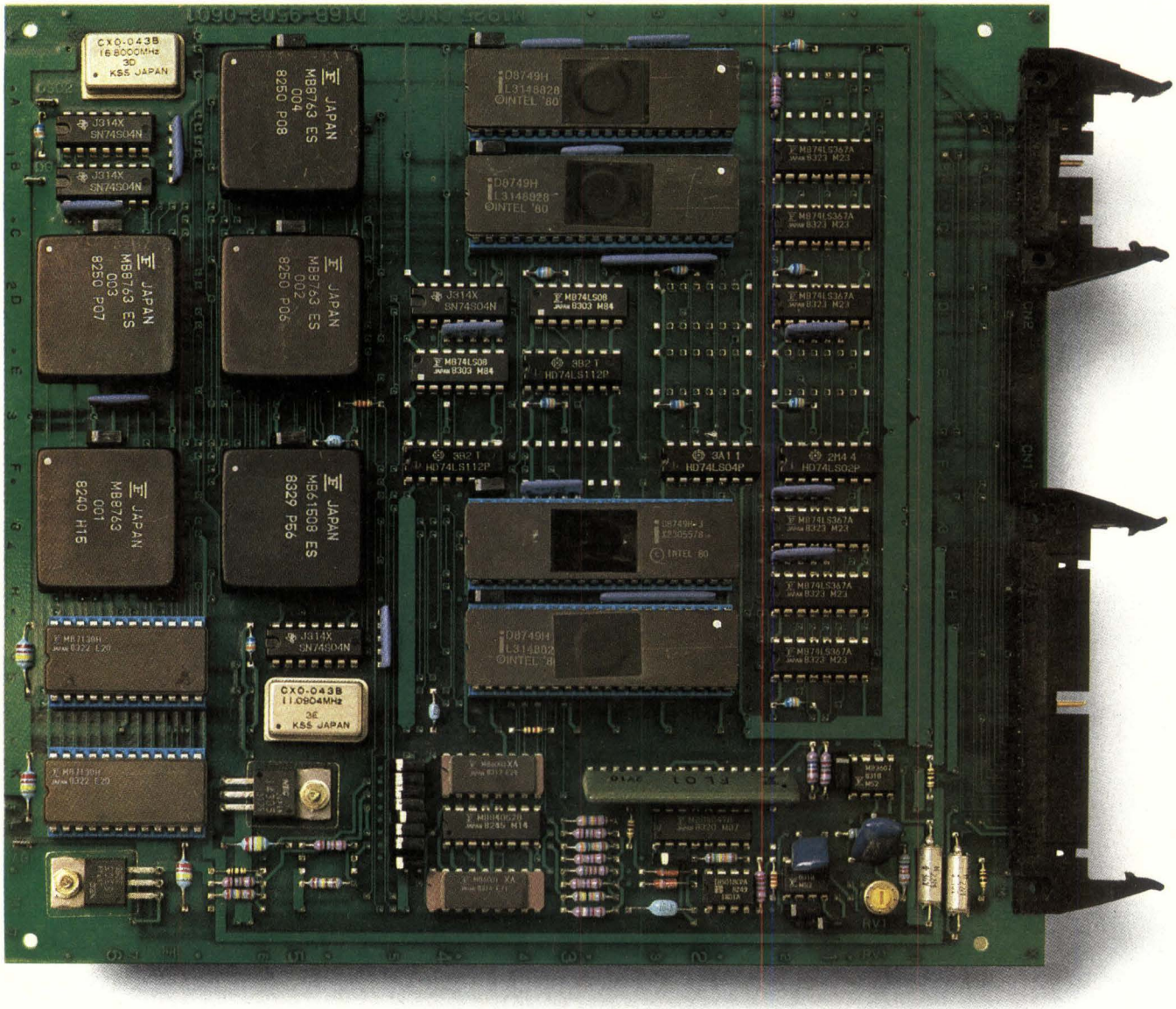


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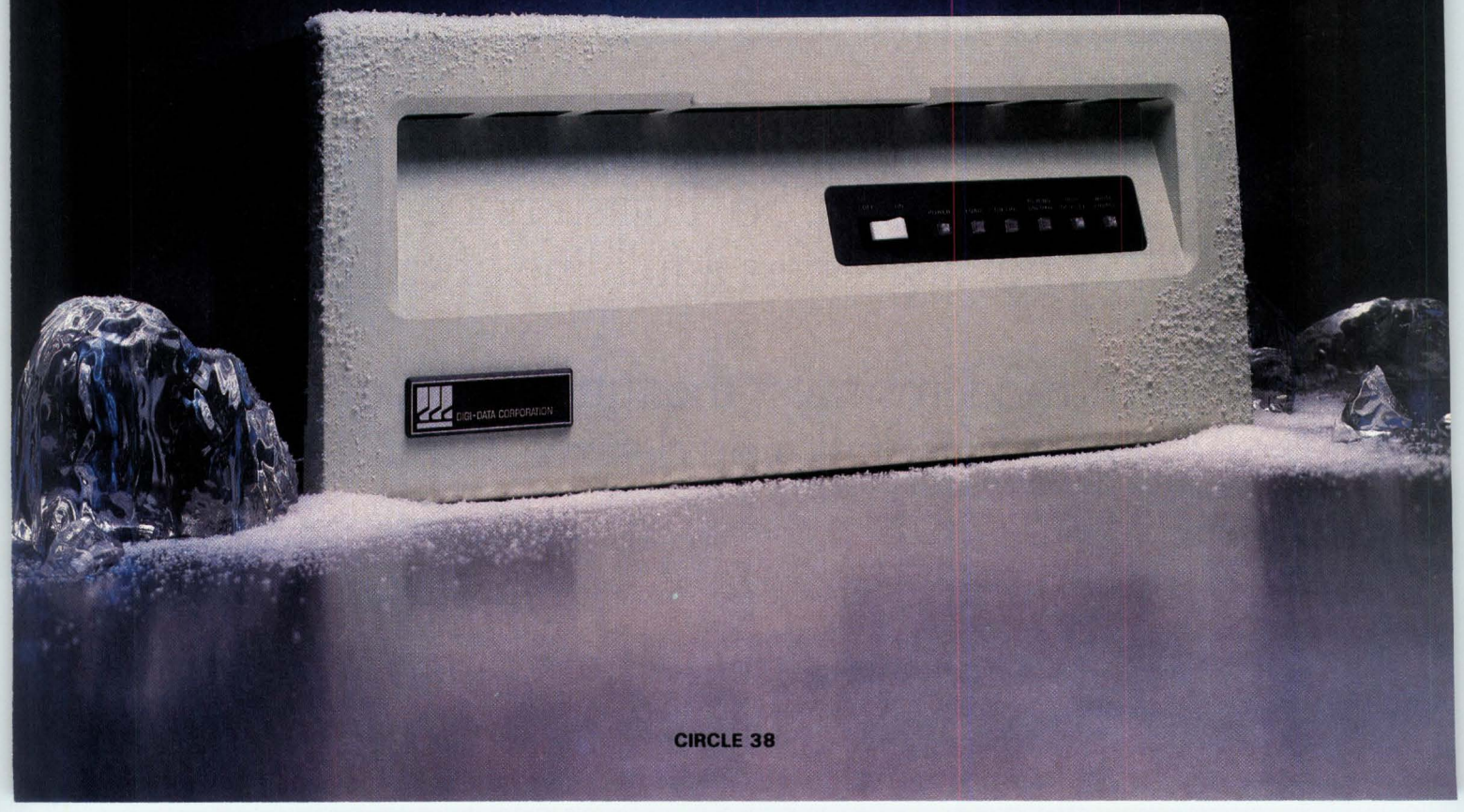
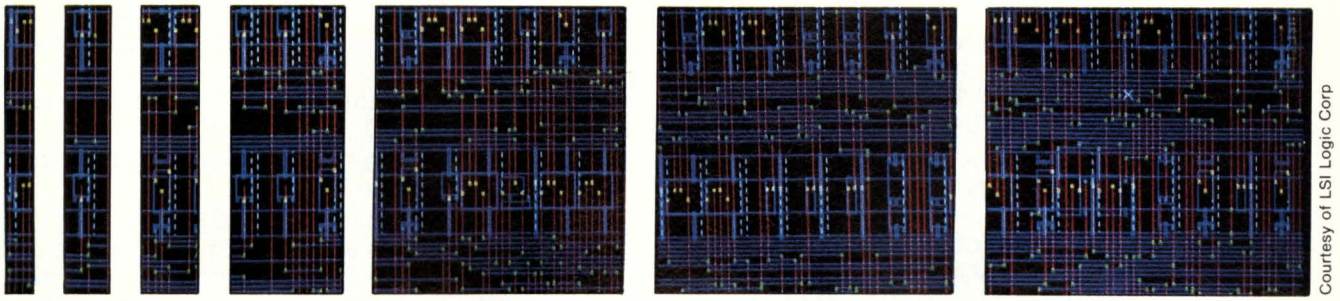



CIRCLE 38

# ISSCC '84
# International Solid State Circuits Conference

**San Francisco Hilton Hotel, San Francisco, California February 22 to 24, 1984**



Courtesy of LSI Logic Corp

Next month's International Solid State Circuits Conference will plumb advanced prototypes in bipolar, MOS, and GaAs technologies. Capitalizing on design rules as low as 1 $\mu$m, memory chips with ultrafast access times reach densities of 1 Mbit. Moreover, growing ranks of 256-Kbit dynamic RAMs clock access around 80 ns, while 64-Kbit static RAMs are closing in on 20 ns. Other chips to watch for are a 32-bit VLSI superminicomputer CPU with 1,220,500 transistors and faster, higher capacity erasable PROMs.

Submicrometer design rules, picosecond gate delays, and three-dimensional architecture remain for the most part in theoretical discussions. Meanwhile, CMOS continues to solidify its posture alongside NMOS as a high performance technology, and GaAs is coming into sharper focus as a potential player in high speed digital circuits.

Circuit integrators who are puzzling over reliable ways to scale semiconductor technology further are about to get a boost. This year, standard power supply voltages for ICs are expected to drop from 5 to 3.3 V, $\pm$0.3 V. Based on impending JEDEC approval of this lower power standard, many designers are already planning in earnest for the next round of integration. At its lower limit, the proposed standard matches high performance CMOS; at its upper limit, established 5-V technologies.

Inevitably, memory technology is in the vanguard of semiconductor development because of its device regularity and testability. Right now, researchers from Stanford University (Stanford, Calif) project a 16-Mbit density ceiling for VLSI DRAMs. From the performance standpoint, the Stanford group will present an analytic model representing estimated limits of NMOS and CMOS devices. Minimum channel lengths of 0.14 and 0.40 $\mu$m, corresponding to logic gate delays of 19 ps for CMOS and 103 ps for NMOS, are predicted.

Shrinking linear dimensions by 36 percent, Intel Corp (Santa Clara, Calif) scientists have scaled a CMOS chip down to 1.5 $\mu$m. They did this by integrating existing NMOS devices with an n-well CMOS approach. Bulk p-substrates replace p– epitaxy on p+ substrates to reduce latchup susceptibility. In this way, an 8-bit microcomputer is said to achieve minimum gate delays of 190 ps.

The Hitachi Central Research Laboratory (Tokyo, Japan) will analyze how it integrates 84-ps ECL with 320-ps $I^2L$ technology. A side wall base contact structure is used to make the ECL and $I^2L$ circuits, whose gate areas measure 3500 and 112 $\mu m^2$. Members of the Institut fur Theoretische Elektrotechnik (Aachen, Germany) form nonsaturating and merged current mode logic using up/down transistors. The chip displays a power-delay product of 0.1 pJ for power dissipation less than 50 $\mu$W/gate, and a minimum delay of 1.6 ns at 200 $\mu$W/gate.

**Dense DRAMs speed up, SRAMs go CMOS**

Over the last 10 years, DRAM design rules shrank from 10 to under 2 $\mu$m while designers grappled with speed/density trade-offs. Today, the 256-Kbit plus league is filling up with CMOS and NMOS DRAMs, and putting access times under 100 ns into the contract. In due course, this increased density may force the familiar x 1 address-multiplexed configuration to yield ground to x 4 and x 8 organizations.

Auxiliary onchip functions also distinguish newcomer 256-Kbit RAMs. Staff from Siemens AG (Munich, Germany) will describe a double poly $TaSi_2$-gate 256-Kbit DRAM with 20-ns nibble mode and automatic descrambled testing. Colleagues from IBM Deutschland (Boeblingen, Germany) will present an 80-ns, 256-Kbit n-channel metal-gate DRAM with four selectable data I/O buffers. This chip configures 64-K x 4, 128-K x 2, or 256-K x 1, with parallel or serial 20-ns data transfer rate.

Intel Corp (Aloha, Ore) will present a sub-100-ns 256-Kbit DRAM constructed from CMOS III technology with a 1-$\mu$m channel length. The chip dissipates 25 $\mu$W standby power and offers 25-MHz ripple mode and static column mode. Beyond that, Hitachi, Ltd (Tokyo, Japan) will highlight an externally clocked 32-K x 9 pseudostatic RAM. The 288-Kbit chip uses a 6.8- x 13.6-$\mu$m n-channel dynamic transistor cell, with 5.58- x 9.86-mm die size.

An experimental 1-Mbit DRAM with an onchip voltage limiter will be the subject of another Hitachi report. The 5-V NMOS chip has a 21-$\mu m^2$

cell; typical access time is 90 ns, cycle time is 260 ns, and power dissipation is 300 mW.

Demand for cooler, portable high performance systems is driving CMOS SRAM developers hard. The big news this year is Toshiba Corp's (Kawasaki, Japan) 46-ns, 256-Kbit chip. The 59.2-mm$^2$, 32-K x 8 CMOS SRAM is made from double-metal, double poly 1.2-$\mu$m p-well technology. It displays 10-mW operating power at 1 MHz and 30-$\mu$W standby power. Toshiba will present a second CMOS SRAM made with 1.2-$\mu$m design rules. This one features bipolar sense amplifiers, and uses both CMOS and bipolar devices with double poly MoSi processing. The 64-K chip typically accesses in 28 ns and has a 20-nA standby mode.

The fastest 64-Kbit CMOS SRAM at the conference ticks off 20 ns during a typical address access. Hitachi, Ltd's 19.0-mm$^2$ chip uses 1.3-$\mu$m gate MOS transistors, a pulsed-word-line technique, and p-well/bipolar technology. Power dissipation is typically 70 mW, given a 1-MHz cycle time.

Two 64-Kbit SRAMs follow 1.5-$\mu$m design rules. A 25-ns, 30.9-mm$^2$ chip from NEC Corp (Kanagawa, Japan) is based on p-well CMOS technology featuring a double-metal poly load four-transistor memory cell. Fairchild Research Center's (Palo Alto, Calif) SRAM is a poly load 28.0-mm$^2$ chip using 1.5-$\mu$m double TaSi p-well CMOS technology.

Inmos Corp (Colorado Springs, Colo) researchers will present a 30-ns, 64-Kbit CMOS SRAM using analog circuit techniques. This chip also features multistage decoding and a single polysilicon memory cell with buried $V_{SS}$ line.

The other 20-ns access, 64-Kbit SRAM, made by IBM Research Center (Yorktown Heights, NY), is an NMOS chip configured 4-K x 16. Made with 1.7-$\mu$m lines and single-level polycide, it features a four-transistor dynamic refresh memory cell and a 30-ns cycle time.

**Nonvolatile memories diversify**

The CMOS revolution is transforming nonvolatile memory as well as dynamic and static RAM techniques. EPROMs and ROMs are improving speed and density, but the many technologies used to implement electrically erasable PROMs may create a standardization problem.

This year's EPROMs range from 1 Mbit down to 256 Kbits, with corresponding access times of 200 to 125 ns. The densest, from NEC Corp (Sagamihara, Japan) is a fully static design using 1.2-$\mu$m design rules. The chip's organization can be either 64-K x 16 or 128-K x 8, and programming voltage is about 13 V.

Advanced Micro Devices (Sunnyvale, Calif) will be showing its 150-ns, 512-Kbit NMOS EPROM. Double polysilicon floating gate technology is realizing the densities of 64 to 512 Kbits; 1.7-$\mu$m design rules allow a cell size of 36.6 $\mu$m$^2$.

Seeq Technology, Inc's (San Jose, Calif) 125-ns, 256-Kbit EPROM is made from 1.5-$\mu$m n-well CMOS on epitaxy. This results in a cell size of 37.5 $\mu$m$^2$ and a die size of 180 mils square. The chip features 12- to 16-V programming and a 50-mW active power dissipation.

Exel Microelectronics, Inc's (San Jose, Calif) 4-K x 8 CMOS EEPROM achieves 55-ns access time through the memory array by using two memory cells per bit. Generating a differential signal on complementary bit lines reduces the voltage swing necessary for sensing.

Another Seeq chip using 1.5-$\mu$m$^2$ n-well CMOS on epitaxy is a 5-V only 64-Kbit EEROM. The device features an 85-$\mu$m$^2$ two-transistor cell and 33,100-mil$^2$ die area. Address edge detection circuits result in a 100-ns typical access time with 50-mW active power dissipation.

Megabit capacity in an 80-ns PROM will be examined by Toshiba Corp (Kawasaki, Japan) designers. Their chip incorporates a through-hole programmed mask ROM cell and a fully static CMOS sense amplifier. Using double polysilicon p-well CMOS technology, the ROM achieves a cell size of 33 $\mu$m$^2$.

**Microprocessors and microcontrollers rev up**

Without a doubt, 32-bit architecture is creating the framework for future advanced processor developments. At the same time, sophisticated 8- and 16-bit processors and controllers are dedicating powerful intelligence with onchip memory to myriad ancillary operations.

Researchers from the University of California, Berkeley, will analyze the characteristics of two scaled versions of their 32-bit, reduced instruction set computer. The 58-mm$^2$, 4-$\mu$m version of this NMOS microprocessor runs at 8 MHz within 5 percent of expected speed and consumes 1.25 W. The 3-$\mu$m, 32-mm$^2$ version operates at 12 MHz using 1.8 W.

Digital Equipment Corp (Hudson, Mass) will make three presentations to whet the appetites of 32-bit architects: a VLSI superminicomputer CPU, a microprocessor with onchip virtual memory management, and a bus interface chip. The superminicomputer processor consists of a five-chip set implementing 304 instructions. Design encompasses 1,220,500 transistors and a 220-ns microcycle. In addition, DEC will unveil a 140,000-transistor, 32-bit single-chip microprocessor that carries out 304 superminicomputer instructions. The chip measures 8.5 x 8.0 mm, and dissipates 3 W. The bus interface provides 600-ns data access, 13-Mbit bandwidth, and error detection. This 265- x 265-mil chip mounts on a 132-pin ceramic grid array and dissipates 3.5 W.

*(continued on page 64)*

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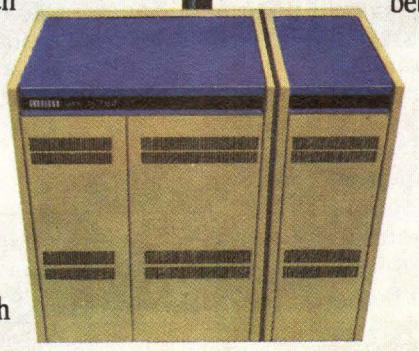

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CIRCLE 39

*(continued from page 62)*

In addition, scientists from SGS-ATES (Milan, Italy) will detail their 8-bit, 5-V only single-chip microcomputer implemented in 4-$\mu$m double poly floating gate technology. The computer carries 32 Kbits of ROM, 512 Kbits of RAM, and 512 Kbits of nonvolatile SRAM. Texas Instruments, Inc (Houston, Tex) researchers will examine a 16-bit digital communication controller with 2816 bytes of RAM. The chip features instruction fault detection, I/O parity check/generation, and special test modes.

**Digital GaAs circuits progress**

Presently, GaAs technology imposes speed-versus-function trade-offs that make its feasibility questionable in many computer system applications. Despite such concerns, gigahertz clock rates inspire designers to work around the functional limitation and capitalize on short gate delays for high speed digital applications.

A fourfold density improvement characterizes this year's GaAs SRAMs over those from last year. Fujitsu Laboratories, Ltd (Atsugi, Japan) will show a 3-ns, 4-K x 1 chip. Researchers will describe the tungsten-silicide gate, self-aligned technology responsible for this 700-mW SRAM. It features 1.5-$\mu$m gates, E/D direct coupled FET logic, and 2-$\mu$m line-width metallization. In addition, NTT Atsugi Electrical Communication Laboratory (Kanagawa, Japan) will present its own 4-K x 1 SRAM, with direct coupled FET logic. The 5-ns chip uses self-aligned implantation for the n+ layer. It also dissipates 700 mW.

Two GaAs gate arrays demonstrate present levels of functional complexity. TI (Dallas, Tex) will report on the design, fabrication, and performance of its 1-K heterojunction bipolar array. The $I^2L$ gate array has a base bar size of 3.55 x 3.80 $mm^2$, and contains 1024 internal gates, 64 programmable I/O buffers, and 8 power supply pads. Also, Toshiba Corp will highlight a 1050-gate array connected as a 6 x 6-bit parallel multiplier. The 350-mW chip performs 10.6-ns multiplies.

IBM General Technology Div (Essex Junction, Vt) researchers will compare gate array, mixed gate array, and custom integrated circuit design methods used to create a full-custom, 32-bit NMOS microprocessor. Onchip 5- and 3.4-V supply voltages and automated gate array design in parts of the chip achieve 230-ns speed and 2.8-W power dissipation. The IBM group will also present a CMOS logic circuit using 10,880 NMOS differential pairs. This approach generates performance comparable to conventional CMOS, and is suited to automated logic minimization and placement and routing techniques.

In semicustom array prototypes, as elsewhere, CMOS looms large. A 12,000-gate CMOS array with 10 Kbits of flexible memory will be detailed by Hitachi, Ltd spokesmen; the 2-$\mu$m CMOS gate distributes transistors throughout the wiring region. In addition, Hitachi will cover a 16-ns array with 16-word x 8-bit RAM, and a 16-word x 10-bit first-in, first-out memory.

Toshiba Corp will be touting its 8370-gate, subnanosecond CMOS/SOS array, made using a 2-$\mu$m Si-gate process. Typical propagation delay for the two-input NAND gate is 0.87 ns; the gate has a fanout of 3 and 2-mm metal interconnect loading.

The development of a 2-$\mu$m poly gate CMOS array that combines digital gate array design with stacked-layout analog capability will be detailed by Stanford University researchers. The analog part contains up to 10 sections of a biquadratic switched-capacitor filter.

A team from TRW Defense Systems Group (Redondo Beach, Calif) and AT&T Bell Laboratories (Allentown, Pa) will present a VLSI delay commutator for fast Fourier transform processors. Made using 2.5-$\mu$m CMOS standard cell technique, the 108,000-transistor circuit realizes data rates to 40 MHz. It has 12,288 shift register stages and about 2000 logic gates.

A 4-ns ECL field programmable logic array will be outlined by Fairchild Research Center and Fairchild Advanced Bipolar Div (Mountain View, Calif). The array configures 16 x 24 x (8 + $\overline{8}$) with true and complement outputs. Features include programmable vertical junction fuses and built-in test.

**Spotlight on communications**

Although ISSCC '84 will be a bit early to take the wraps off many telecommunication circuits now in development, several presentations may give a glimpse of what is coming. Among them, Seeq Technology, Inc will show its 10-MHz Ethernet serial interface chip made using 2-$\mu$m n-well CMOS. The 99- x 115-mil Manchester encoder/decoder consumes 150 mW and uses a phase locked loop to decode data having 18-ns jitter. The transmitter drives a 78-$\Omega$ transceiver cable directly with less than 0.5-ns skew. Also, a cooperative effort between TI (Houston, Tex) and Racal-Vadic (Milpitas, Calif) has resulted in a 1200-bit/s quadrature phase shift keyed full-duplex modem chip. The 55,700-$mil^2$ die houses all Bell 212 and CCITT V.21, V.22, and V.23 functions.

*—Deb Highberger, Senior Associate Editor*

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*(ISSCC coverage continued on page 66)*

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(continued from page 64)

## Technical Program Excerpts*

### Session 1: Custom and Semicustom Design Techniques

**Wed 9 am to 12:15 pm, Continental 1-4**

Chair: A. R. Newton, University of California, Berkeley

1/1 "An Integrated Modular and Standard Cell IC Design Method"
R. Kasai, K-n. Fukami, K. Tansho, H. Kitazawa, N. Miyaho, and S. Horiguchi, NTT Atsugi Electrical Communication Laboratory, Kanagawa, Japan

1/2 "A Comparison of Mixed Gate Array and Custom IC Design Methods"
W. K. Hoffman, R. A. Bechade, C. K. Erdelyl, and M. P. Concannon, IBM General Technology Div, Essex Junction, Vt

1/3 "Cascode Voltage Switch Logic: A Differential CMOS Logic Family"
L. G. Heller and W. R. Griffin, IBM General Technology Div, Essex Junction, Vt; and J. W. Davis and N. G. Thoma, IBM System Products Div, Boca Raton, Fla

1/4 "A Synthesis Program for Operational Amplifiers"
M. G. Degrauwe, Centre Electronique Horloger, Neuchatel, Switzerland; and W. M. C. Sansen, Catholic University/Leuven, Heverlee, Belgium

1/5 "Computer Generation of Digital Filter Banks"
P. A. Ruetz, S. P. Pope, B. Solberg, and R. W. Brodersen, University of California, Berkeley

1/6 "The Use of E-Beam for Random Access Read and Write of Digital Test Signals"
J. Jensen and K. Martin, University of California, Los Angeles

### Session 2: Image Sensors

**Wed 9 am to 12:15 pm, Continental 5**

Chair: R. P. Khosla, Eastman Kodak Research, Rochester, NY

2/1 "MOS Imaging with Random Noise Suppression"
S. Ohba, M. Nakai, H. Ando, T. Ozaki, N. Ozawa, T. Imaide, S. Ikeda, T. Suzuki, I. Takemoto, and T. Masuhara, Hitachi Central Research Laboratory, Tokyo, Japan

2/2 "A Line Transfer Color Image Sensor with 576 x 462 Pixels"
J. L. Berger, L. Brissot, Y. Cazaux, and P. Descure, Thomson-CSF Electronic Tube Div, Cedex, France

2/3 "A 488 x 430 Interline Imager with Integral Exposure Control"
Y. T. Chan, O. R. Barrett, C. W. Chen, Y. Abendini, and D. D. Wen, Fairchild Camera and Instrument Corp, Palo Alto, Calif

2/4 "An Interline Transfer CCD Imager with a Half-inch Format"
Y. Matsunaga and N. Suzuki, Toshiba Corp, Kawasaki, Japan

2/5 "A 3456-Element CCD Sensor with Serpentine Shift Registers"
D. D. Wen, D. Reaves, S. Onishi, and J. Pendleton, Fairchild Camera and Instrument Corp, Palo Alto, Calif

2/6 "A 5732-Element 1.2-in. Linear CCD Imager"
N. Kadekodi, A. Claproth, A. Anyiwo, L. Sheu, J. Tandon, and A. Ibrahim, Xerox Microelectronics Center, El Segundo, Calif

### Session 3: Digital GaAs Circuits

**Wed 9 am to 12:15 pm, Continental 6-9**

Chair: A. Podell, Podell Assocs, Palo Alto, Calif

3/1 "A 1-K Gate GaAs Gate Array"
Y. Ikawa, N. Toyoda, M. Mochizuki, T. Terada, K. Kanazawa, M. Hirose, T. Mizoguchi, and A. Hojo, Toshiba Corp, Kawasaki, Japan

3/2 "GaAs Heterojunction Bipolar 1-K Gate Array"
H. T. Yuan, W. V. McLevige, H. D. Shih, and A. S. Hearn, Texas Instruments, Inc, Dallas, Tex

3/3 "A 3-ns GaAs 4-K x 1-bit SRAM"
N. Yokoyama, H. Onodera, T. Shinoki, H. Ohnishi, H. Nishi, and A. Shibatomi, Fujitsu Laboratories, Ltd, Atsugi, Japan

3/4 "A GaAs 4-Kbit SRAM with Direct Coupled FET Logic"
M. Hirayama, M. Ino, Y. Matsuoka, and M. Suzuki, NTT Atsugi Electrical Communication Laboratory, Kanagawa, Japan

### Session 4: Data Acquisition Circuits

**Wed 9 am to 12:15 pm, Imperial**

Chair: R. A. Blauschild, Linear Design, Inc, Los Altos, Calif

4/1 "A Bulk CMOS 20-MS/s, 7-bit Flash A-D Converter"
Y. Fujita, E. Masuda, S. Sakamoto, T. Sakaue, and Y. Sato, Toshiba Corp, Kawasaki, Japan

4/2 "An 8-bit, 100-MS/s Flash A-D Converter"
Y. Yoshii, K. Asano, M. Nakamura, and C. Yamada, Sony Corp, Kanagawa, Japan

4/3 "A Multi-Step Parallel 10-bit 1.5-$\mu$s A-D Converter"
M. Kolluri, Signetics Corp, Sunnyvale, Calif

4/4 "A Ratio-Independent Algorithmic A-D Conversion Technique"
P. W. Li, M. Chin, P. R. Gray, and R. Castello, University of California, Berkeley

4/5 "A Self-Calibrating 12-bit, 12-$\mu$s CMOS A-D Converter"
H-S. Lee, D. A. Hodges, and P. R. Gray, University of California, Berkeley

4/6 "A Trimless, 16-bit Digital Potentiometer"
P. Holloway, Analog Devices, Wilmington, Mass

(continued on page 68)

*Program sessions are subject to last-minute changes.

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CIRCLE 41

*(continued from page 66)*

## Session 6: Keynote Address
**Wed 2:15 to 2:45 pm, Continental**

Chair: P.W.J. Verhofstadt, Fairchild Microprocess Div, Mountain View, Calif

"A Positive Program for World Cooperation"
G. Madland, Integrated Circuit Engineering Corp, Scottsdale, Ariz

## Session 7: High Speed Analog Circuits
**Wed 3:15 to 6 pm, Continental 1-4**

Chair: H. J. Boll, AT&T Bell Laboratories, Murray Hill, NJ

7/1 "A GaAs Monolithic Voltage Controlled Oscillator"
B. N. Scott, M. Wurtele, and B. B. Cregger, Texas Instruments, Inc, Dallas, Tex

7/2 "Fine Line NMOS Transresistance Amplifiers"
A. A. Abidi and R. A. Kushner, AT&T Bell Laboratories, Murray Hill, NJ; and B. L. Kasper, AT&T Bell Laboratories, Holmdel, NJ

7/3 "Distributed Cascode Amplifier and Noise Figure Modeling of an Arbitrary Amplifier Configuration"
D. E. Dawson, M. L. Salib, and L. E. Dickens, Westinghouse Electric Co, Baltimore, Md

7/4 "Computer-Aided Design of Nonlinear Microwave ICs"
M. I. Sobhy and A. K. Jastrzebski, University of Kent, Kent, United Kingdom

## Session 8: Data Processing Circuits
**Wed 3:15 to 6 pm, Continental 5-6**

Chair: E. Swartzlander, TRW Defense Systems Group, Redondo Beach, Calif

8/1 "A 45-ns, 16 x 16 CMOS Multiplier"
Y. Kaji, N. Sugiyama, S. Ohya, Y. Kitamura, and M. Kikuchi, NEC Corp, Kanagawa, Japan

8/2 "A 25/50-MHz, Dual-Mode Parallel Multiplier/Accumulator"
F. Welten and J. Lohstroh, Philips Research Laboratories, Eindhoven, The Netherlands; and A. Linssen, RTC, Caen, France

8/3 "A 16-ns, 2-K x 8-bit CMOS SRAM"
N. Okazaki, T. Komatsu, N. Hoshi, K. Tsuboi, and T. Shimada, Sony Corp, Kanagawa, Japan

8/4 "A Dual-Port RAM with Internal Contention Resolution for Asynchronous Operation"
F. E. Barber, G. A. Ingram, and M. S. Strauss, AT&T Bell Laboratories, Allentown, Pa

## Session 9: Dedicated Signal Processors
**Wed 3:15 to 6 pm, Imperial**

Chair: R. W. Brodersen, University of California, Berkeley

9/1 "A CCD Matrix-Matrix Product Parallel Processor"
A. M. Chiang, R. W. Mountain, D. J. Silversmith, and B. J. Felton, MIT Lincoln Laboratory, Lexington, Mass

9/2 "A Single-Chip, 20-Channel Speech Spectrum Analyzer"
Y. Kuraishi, K. Nakayama, and K. Miyadera, NEC Corp, Kawasaki, Japan

9/3 "An Integrated Phoneme Speech Synthesizer"
D. G. Maeding, C. C. Austin, P. J. Maimone, Silicon Systems, Inc, Tustin, Calif

9/4 "A Monolithic Programmable Speech Synthesizer with Voice Recognition"
T. Takamizawa, T. Yoshino, S. Abiko, M. Hashizume, K. Katoh, K. Chin, and A. Henderson, Texas Instruments Japan Ltd, Tokyo, Japan

## Panel 1: Wafer Scale Integration
**Wed 8 pm, Continental 1-4**

Moderator: H. G. Gragon, Texas Instruments, Inc, Dallas, Tex

Panelists: D. Fussel, University of Texas, Austin; E. Harari, Wafer Scale Integration, Inc, Santa Clara, Calif; R. Headrick, Hewlett-Packard, Cupertino, Calif; D. L. Peltzer, Trilogy Systems Corp, Cupertino, Calif; J. Raffel, MIT Lincoln Laboratory, Lexington, Mass; and R. R. Johnson, Mosaic Systems, Troy, Mich

## Panel 2: Testing Methodology for VLSI
**Wed 8 pm, Continental 5**

Moderator: R. W. Dutton, Stanford University, Stanford, Calif

Panelists: J. Beyers, Hewlett-Packard, Fort Collins, Colo; P. Bottorff, IBM Corp, Endicott, NY; E. McCluskey, Stanford University, Stanford, Calif; M. Nagamine, Fujitsu, Ltd, Kawasaki, Japan; R. Young, Intel Corp, Aloha, Ore; and J. Zasio, STC Research Corp, Santa Clara, Calif

## Panel 3: System Requirements for GaAs Digital ICs
**Wed 8 pm, Continental 6**

Moderator: P. T. Greiling, Hughes Research Laboratories, Malibu, Calif

Panelists: R. Buchanan, RADC, Hanscom Air Force Base, Bedford, Mass; N. T. Linh, Thomson-CSF, Cedex, France; S. E. Nelson, Cray Research, Inc, Chippewa Falls, Wis; K. J. Sleger, Naval Research Laboratory, Washington, DC; and K. Suyama, Fujitsu, Ltd, Kawasaki, Japan

## Panel 4: High Speed A-D Conversion
**Wed 8 pm, Continental 7-9**

Moderator: R. J. van de Plassche, Philips Research Laboratories, Sunnyvale, Calif

Panelists: A. Dingwall, RCA Solid-State Technology Center, Somerville, NJ; K. de Graaf, TRW Systems Group, Redondo Beach, Calif; T. van Kessel, Philips Research Laboratories, Eindhoven, The Netherlands; T. Matsushita, Sony Corp, Kanagawa, Japan; G. L. Schaffer, Telmos, Inc, Sunnyvale, Calif; and S. S. Taylor, Tektronix, Inc, Beaverton, Ore

*(continued on page 70)*

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**CIRCLE 42**

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## Panel 5: 1-Mbit DRAM Alternatives

**Wed 8 pm, Imperial**

Moderator: H. C. Kirsch, AT&T Bell Laboratories, Allentown, Pa

Panelists: S. Chou, Intel Corp, Aloha, Ore; M. Czekalski, Digital Equipment Corp, Maynard, Mass; C. J. Grohowski, IBM, Essex Junction, Vt; K. Miyasaka, Fujitsu, Ltd, Kawasaki, Japan; K. Itoh, Hitachi Central Research Laboratory, Tokyo, Japan; H. Penzel, Siemens AG, Munich, Germany; D. Segers, Mostek, Carrollton, Tex

## Session 10: Nonvolatile Memories

**Thurs 9 am to 12:15 pm, Continental 1-4**

Chair: P. J. Salsbury, Seeq Technology, Inc, San Jose, Calif

10/1 "512-Kbit EPROMS"
D. Rinerson, M. Ahrens, M. Briner, J. Lien, B. Venkatesh, T. Lin, P. Song, S. Longcor, L. Shen, and D. Rogers, Advanced Micro Devices, Sunnyvale, Calif

10/2 "A 256-Kbit CMOS EPROM"
W. Ip, T-L. Chiu, T-C. Wu, and G. Perlegos, Seeq Technology, Inc, San Jose, Calif

10/3 "A 1-Mbit EPROM"
K. Okumura, S. Oya, M. Yamamoto, T. Watanabe, Y. Shimamura, and M. Kikuchi, NEC Corp, Sagamihara, Japan

10/4 "A 64-Kbit CMOS EEROM"
S. Mehrotra, T-C. Wu, T-L. Chiu, and G. Perlegos, Seeq Technology, Inc, San Jose, Calif

10/5 "A 55-ns CMOS EEPROM"
R. Zeman, C. Ho, and T. Chang, Exel Microelectronics, Inc, San Jose, Calif

10/6 "An 80-ns 1-Mbit ROM"
F. Masuoka, S. Ariizumi, T. Iwase, M. Ono, and N. Endo, Toshiba Corp, Kawasaki, Japan

## Session 11: Scaling and Performance Aspects of Technology

**Thurs 9 am to 12:15 pm, Continental 5**

Chair: P. Cottrell, IBM General Technology Div, Essex Junction, Vt

11/1 "Integrated 84-ps ECL with $I^2L$"
T. Nakamura, K. Nakazato, T. Miyazaki, T. Okabe, and M. Nagata, Hitachi Central Research Laboratory, Tokyo, Japan

11/2 "Merged Current Mode Logic"
P. J. Zdebel and W. L. Engl, Institut fur Theoretische Elektrotechnik, Aachen, Germany

11/3 "A 1.5-$\mu$m Scaled CMOS Technology Chip"
S. S. Liu, G. E. Atwood, E. Y. So, B. Wu, R. Leftwich, K. Hasserjian, and B. Jones, Intel Corp, Santa Clara, Calif

11/4 "Performance Limits of NMOS and CMOS"
J. R. Pfiester, J. D. Shott, and J. D. Meindl, Stanford University, Stanford, Calif

11/5 "Physical Limits of VLSI DRAMS"
L. L. Lewyn and J. D. Meindl, Stanford University, Stanford, Calif

11/6 "Stability and Soft Error Rate Analysis of SRAM Cells"
B. Chappell, S. Schuster, and G. Sai-Halasz, IBM Research Center, Yorktown Heights, NY

## Session 12: Microprocessors and Microcontrollers

**Thurs 9 am to 12:15 pm, Continental 6-9**

Chair: D. Seccombe, Hewlett-Packard, Fort Collins, Colo

12/1 "A 32-bit NMOS Microprocessor with a Large Register File"
R. W. Sherburne, Jr, M. G. H. Katevenis, D. A. Patterson, and C. H. Sequin, University of California, Berkeley

12/2 "A 5-V-Only Single-Chip Microcomputer with Nonvolatile SRAM"
P. Rosini, R. Finaurini, and M. Gaibotti, SGS-ATES, Milan, Italy

12/3 "A VLSI Communication Processor Designed for Testability"
S. Sacarisen, M. Stambaugh, P. Lou, A. Khosrovi, and R. Chang, Texas Instruments, Inc, Houston, Tex

12/4 "A VLSI Superminicomputer CPU"
W. N. Johnson, Digital Equipment Corp, Hudson, Mass

12/5 "A 32-bit Bus Interface Chip"
R. Schumann and W. Parker, Digital Equipment Corp, Hudson, Mass

12/6 "A 32-bit Microprocessor with Onchip Virtual Memory Management"
J. Beck, D. Dobberpuhl, M. J. Doherty, E. Dorenkamp, R. Grondalski, D. Grondalski, K. Henry, M. Miller, R. Supnik, S. Thierauf, and R. Witek, Digital Equipment Corp, Hudson, Mass

## Session 13: Modems

**Thurs 9 am to 12:15 pm, Imperial**

Chair: M. S. Foster, Mitel Corp, Kanata, Canada

13/1 "A CMOS Ethernet Serial Interface Chip"
H-M. Haung, D. Banatao, G. Perlegos, T-C. Wu, T-L. Chiu, Seeq Technology, Inc, San Jose, Calif

13/2 "Signaling Pickoff Filter for FDM"
K. Fukahori and T. Glad, Silicon Systems, Inc, Nevada City, Calif; and L. Engh, Farinon Div/Harris Corp, San Carlos, Calif

13/3 "A 300-baud FSK Modem"
A. Takla and Y. A. Haque, American Microsystems, Inc, Santa Clara, Calif

13/4 "An Asynchronous FSK Modem"
K. Yamamoto, S. Fujii, and K. Matsuoka, Oki Electric Industry Co, Inc, Tokyo, Japan

13/5 "A 1200-baud FSK CMOS Modem"
C. A. Laber and P. Lemaitre, National Semiconductor Corp, Santa Clara, Calif

*(continued on page 72)*

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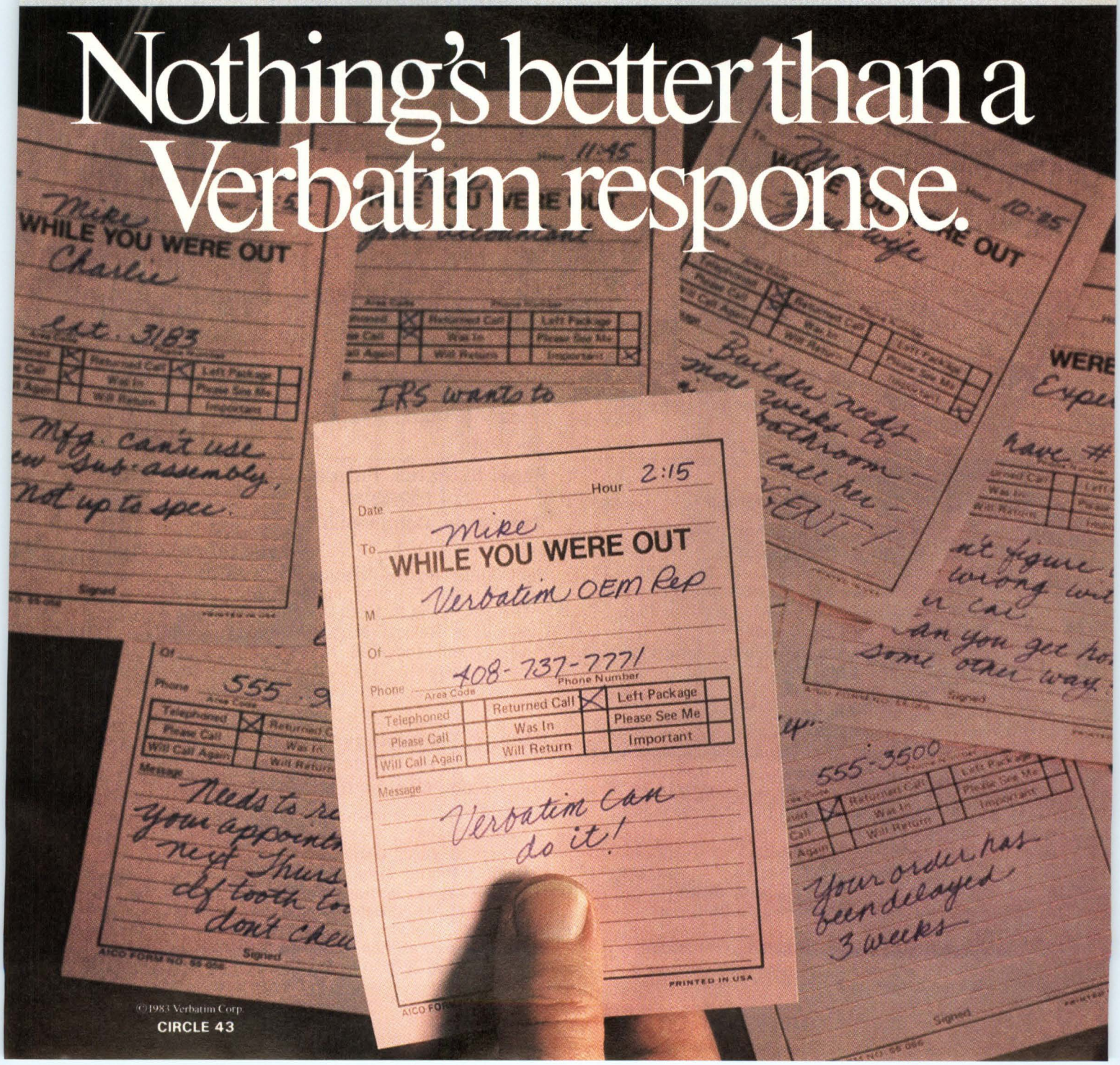


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CIRCLE 43

*(continued from page 70)*

13/6 "A 1200-bit/s QPSK Full-Duplex Modem"
E. Hanson, W. Severin, D. Richardson, E. Klinkovsky, and J. Hochschild, Texas Instruments, Inc, Houston, Tex; and J. Bingham, Racal-Vadic, Milpitas, Calif

## Session 14: Signal Processing

**Thurs 1:30 to 5 pm, Continental 1-4**

Chair: R. Baertsch, General Electric Corporate R & D, Schenectady, NY

14/1 "A CCD TV Signal Processor"
S-i. Imai, T. Sakaue, and H. Moriyama, Toshiba Corp, Kawasaki, Japan

14/2 "An Integrated CMOS-CCD TV Ghost Canceler"
S. Matsumoto, K. Kondo, T. Murata, S. Matsuura, and M. Kazumi, Hitachi Research, Yokohama, Japan; and I. Kobayashi and N. Horino, Hitachi Musashi Works, Tokyo, Japan

14/3 "Facsimile Shading Corrector"
M. Togashi, S. Sato, and S. Ohsima, Matsushita Graphic Communications Systems, Inc, Tokyo, Japan; and K. Aruga and T. Nakamura, Matsushita Electronics Corp, Kawasaki, Japan

14/4 "A 40-MHz, 308-Kbit CCD Video Memory"
H. J. M. Veendrick, L. C. Pfennings, M. J. J. C. Annegarn, H. A. Harwig, M. J. M. Pelgrom, H. J. F. Peuscher, J. G. Raven, A. Slob, and J. W. Slotboom, Philips Research Laboratories, Eindhoven, The Netherlands

14/5 "A VLSI Image Pipeline Processor"
T. Nukiyama, T. Kusano, K. Matsumoto, H. Kurokawa, T. Hoshi, H. Goto, T. Temma, NEC Corp, Kawasaki, Japan

14/6 "A Digital Radio Control Link for Implantable Biotelemetry Applications"
S. J. Gross and J. D. Meindl, Stanford University, Stanford, Calif

## Session 15: Static RAM

**Thurs 1:30 to 5 pm, Continental 5-9**

Chair: R. Pashley, Intel Corp, Santa Clara, Calif

15/1 "A 46-ns, 256-Kbit CMOS SRAM"
M. Isobe, J. Matsunaga, T. Sakurai, T. Ohtani, K. Sawada, H. Nozawa, T. Iizuka, and S. Kohyama, Toshiba Corp, Kawasaki, Japan

15/2 "A 30-ns, 64-Kbit CMOS SRAM"
K. Hardee, M. Griffus, and R. Galvas, Inmos Corp, Colorado Springs, Colo

15/3 "A 25-ns, 64-Kbit SRAM"
H. Ito, S. Koshimaru, O. Kudo, T. Ozawa, T. Yamanaka, N. Yasuoka, H. Asai, N. Harashima, and S. Kikuchi, NEC Corp, Kanagawa, Japan

15/4 "A 35-ns, 64-Kbit CMOS SRAM"
A. Au, N-H. Tsai, P. Chen, M. Hsue, M. Barry, T. Reifsteck, and M. Osman, Fairchild Research Center, Palo Alto, Calif

15/5 "A 20-ns, 64-Kbit CMOS SRAM"
O. Minato, T. Masuhara, T. Sasaki, Y. Sakai, and T. Hayashida, Hitachi, Ltd, Tokyo, Japan

15/6 "A 28-ns, 64-Kbit CMOS SRAM with Bipolar Sense Amplifiers"
J. Miyamoto, S. Saitoh, T. Iizuka, H. Momose, H. Shibata, and K. Kanzaki, Toshiba Corp, Kawasaki, Japan

15/7 "A 20-ns, 64-Kbit NMOS RAM"
S. Schuster, B. Chappell, V. DiLonardo, and P. Britton, IBM Research Center, Yorktown Heights, NY

## Session 16: Telecommunication System ICs

**Thurs 1:30 to 5 pm, Imperial**

Chair: J. M. Huggins, Silicon Systems, Inc, Nevada City, Calif

16/1 "A Single-Chip, High-Voltage Shallow-Junction BORSHT LSI"
T. Ohno, T. Sakurai, Y. Inabe, and T. Koinuma, NTT Atsugi and Musashino Communication Laboratories, Kanagawa and Tokyo, Japan

16/2 "A Programmable CMOS Dual-Channel Line Circuit"
B. K. Ahuja and W. M. Baxter, Intel Corp, Chandler, Ariz; and P. R. Gray, University of California, Berkeley

16/3 "A 150-mW Subscriber Line Board Controller"
P. P. Guebels, F. Van Simaeys, and M. C. Rahier, Bell Telephone Manufacturing Co, Antwerp, Belgium

16/4 "A 200-Kbit/s Burst Mode Transceiver with Two-Bridge Tap Equalizer"
A. Komori, M. Furukawa, T. Sato, and T. Komazaki, Oki Electric Industry Co Ltd, Tokyo, Japan

16/5 "A Burst-Mode LSI Equalizer with Analog-Digital Building Blocks"
Y. Hino, T. Chujo, N. Ueno, and K. Fujita, Fujitsu, Ltd, Kawasaki, Japan

16/6 "A Regenerator Chip Set for High Speed Digital Transmission"
D. G. Ross, R. M. Paski, and D. G. Ehrenberg, AT&T Bell Laboratories, Holmdel, NJ; and W. H. Eckton, Jr and S. F. Moyer, AT&T Bell Laboratories, Reading, Pa

## Panel 6: Status, Future, and Standardization of EEPROMs

**Thurs 8 pm, Continental 1-4**

Moderator: R. W. Pryor, Pitney Bowes, Norwalk, Conn

Panelists: T. Ihzuka, Toshiba R & D Center, Kawasaki City, Japan; F. Jones, Inmos Corp, Colorado Springs, Colo; D. McCranie, Seeq Technology, Inc, San Jose, Calif; J. Skupnjak, Intel Corp, Santa Clara, Calif; and W. E. Tchon, Xicor Corp, Milpitas, Calif

## Panel 7: Technology for Data Transport in an Office Environment

**Thurs 8 pm, Continental 5**

Moderator: H. E. Mussman, AT&T Bell Laboratories, Naperville, Ind

Panelists: C. Bass, Ungermann-Bass, Inc, Santa Clara, Calif; P. Beirne, Mitel Corp, Kanata, Canada; M. Patrick, Texas Instruments, Inc, Houston, Tex; R. Snyder, Wang Laboratories, Lowell, Mass; L. Lerach, Siemens AG, Munich, Germany; T. Tsuda, Fujitsu Laboratories, Ltd, Kawasaki, Japan; and H. Wurzburg, Motorola Semiconductor, Austin, Tex

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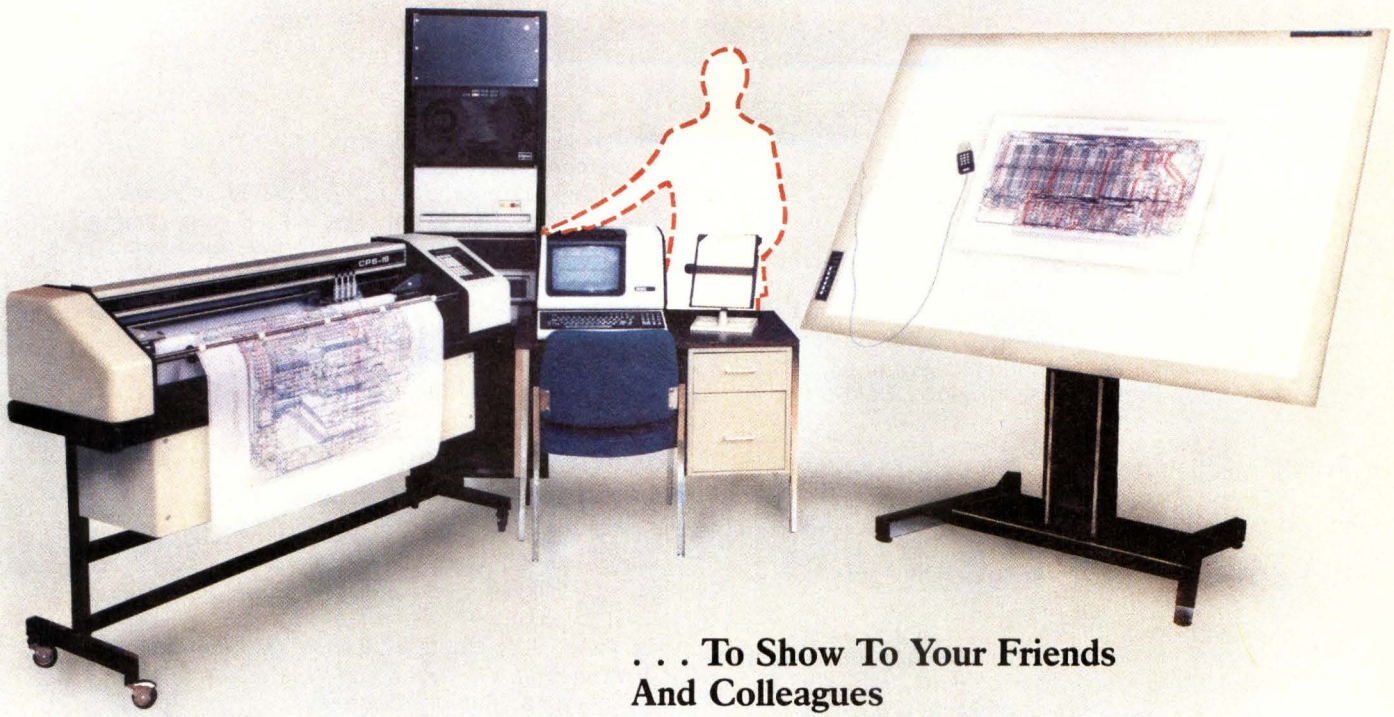

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**CIRCLE 44**

*(continued from page 72)*

## Panel 8: High Speed Analog ICs

**Thurs 8 pm, Continental 6**

Moderator: R. van Tuyl, Hewlett-Packard, Santa Rosa, Calif

Panelists: J. Addis, Tektronix, Inc, Beaverton, Ore; D. Fraser, Bell Laboratories, Murray Hill, NJ; D. Hornbuckle, Hewlett-Packard, Santa Rosa, Calif; N. Kitagawa, Nippon Electric Corp, Kanagawa, Japan; M. Morishita, Mitsubishi Electric, Hyogo, Japan; and A. Podell, Podell Assocs, Palo Alto, Calif

## Panel 9: Semicustom Analog LSI Design Trends and Directions

**Thurs 8 pm, Continental 7-9**

Moderator: A. R. Grebene, Micro-Linear Corp, Saratoga, Calif

Panelists: D. Bray, Interdesign, Inc, Scotts Valley, Calif; G. Kelson, Silicon Systems, Inc, Tustin, Calif; G. McGlinchey, Analog Devices, Inc, Palo Alto, Calif; P. Nance, Telmos Corp, Sunnyvale, Calif; E. Swanson, AT&T Bell Laboratories, Reading, Pa; and H. Yamada, Toshiba R & D Center, Kawasaki, Japan

## Panel 10: Ultrahigh Speed Static RAMs

**Thurs 8 pm, Imperial**

Moderator: W. H. Herndon, Fairchild Advanced Research Center, Palo Alto, Calif

Panelists: R. Eden, Gigabit, Newbury Park, Calif; F. R. Janisch, Sperry, Roseville, Minn; H. Mayumi, NEC Corp, Kawasaki City, Japan; K. O'Connor, AT&T Bell Laboratories, Allentown, Pa; S. L. Smith, Intel Corp, Santa Clara, Calif; S. K. Wiedmann, IBM Laboratories, Boeblingen, Germany; and N. Yokoyama, Fujitsu Laboratories, Atsugi, Japan

## Session 17: Semicustom Arrays

**Fri 9 am to 12:15 pm, Continental 1-4**

Chair: H. Borkan, U.S. Army Electronics Technology and Devices Laboratory, Fort Monmouth, NJ

17/1 "A CMOS 12-K Gate Array with Flexible 10-Kbit Memory"
M. Takechi, K. Ikuzaki, T. Itoh, M. Fujita, M. Asano, A. Masaki, and T. Matsunaga, Hitachi, Ltd, Tokyo, Japan

17/2 "A Subnanosecond 8-K Gate CMOS/SOS Gate Array"
S. Tanaka, K. Nakata, J. Iwamura, J. Ohno, and K. Maeguchi, Toshiba Corp, Kawasaki, Japan

17/3 "A 2-$\mu$m Poly-Gate CMOS Analog-Digital Array"
J. B. Kuo, O-H. Kwan, D. C. Galbraith, F-C. Shone, J. D. Shott, J. T. Walker, R. W. Dutton, and J. D. Meindl, Stanford University, Stanford, Calif

17/4 "An ECL Field Programmable Logic Array"
C. Schmitz and H. Hingarh, Fairchild Research Center, Palo Alto, Calif; and M. Brown, H. Kwan, and J. Vithayathil, Fairchild Advanced Bipolar Div, Mountain View, Calif

17/5 "A VLSI Delay Commutator for FFT Implementation"
E. E. Swartzlander, Jr and W. K. W. Young, TRW Defense Systems Group, Redondo Beach, Calif; and S. J. Joseph, AT&T Bell Laboratories, Allentown, Pa

17/6 "An EEPROM for Microprocessors and Custom Logic"
R. Cuppens, C. D. Hartgring, J. F. Verwey, and H. L. Peek, Philips Research Laboratories, Eindhoven, The Netherlands

## Session 18: 256-Kbit DRAM and Beyond

**Fri 9 am to 12:15 pm, Continental 5-9**

Chair: K. Hoffmann, Bundeswehr University/Siemens Corp, Munich, Germany

18/1 "A 256-Kbit DRAM with Descrambled Redundancy Test Capability"
D. Kantz, J. R. Goetz, R. Bender, M. Baehring, J. Wawersig, W. Meyer, and W. Mueller, Siemens AG, Munich, Germany

18/2 "A 256-Kbit DRAM"
E. Baier, H. Barsuhn, R. Clemen, and W. Haug, IBM Deutschland, Boeblingen, Germany

18/3 "A 288-Kbit CMOS Pseudo SRAM"
K. Kawamoto, Y. Yamaguchi, S. Shimizu, K. Oishi, N. Taninura, and T. Yasui, Hitachi Ltd, Tokyo, Japan

18/4 "A Sub 100-ns 256-Kbit DRAM in CMOS III Technology"
R. Kung, A. Mohsen, J. Shutz, P. Madland, C. Webb, E. Hamdy, C. Simonsen, R. Guo, K. Yu, and S. Chou, Intel Corp, Aloha, Ore

18/5 "Shared Word Line DRAM-Cell"
R. E. Scheuerlein, W. W. Walker, D. C. Morency, W. Noble, P. Bakeman, and D. Critchlow, IBM General Technology Div, Essex Junction, Vt

18/6 "An Experimental 1-Mbit DRAM with Onchip Voltage Limiter"
K. Itoh, R. Hori, J. Etoh, S. Asai, N. Hashimoto, K. Yagi, and H. Sunami, Hitachi Ltd, Tokyo, Japan

## Session 19: General Purpose Analog Circuits

**Fri 9 am to 12:15 pm, Imperial**

Chair: E. A. Vittoz, Centre Electronique Horloger, Neuchatel, Switzerland

19/1 "An Analog Array Processor"
B. Gilbert, Analog Devices, Forest Grove, Ore

19/2 "A Monolithic p-Channel JFET Quad Operational Amplifier"
W. F. Davis and R. L. Vyne, Motorola Semiconductor, Tempe, Ariz

19/3 "A Power BiMOS with Integral High Current pnp Transistor"
D. Cave, B. Bynum, and T. Houk, Motorola, Inc, Tempe, Ariz

19/4 "A Fahrenheit Temperature Sensor"
R. A. Pease, National Semiconductor Corp, Santa Clara, Calif

□

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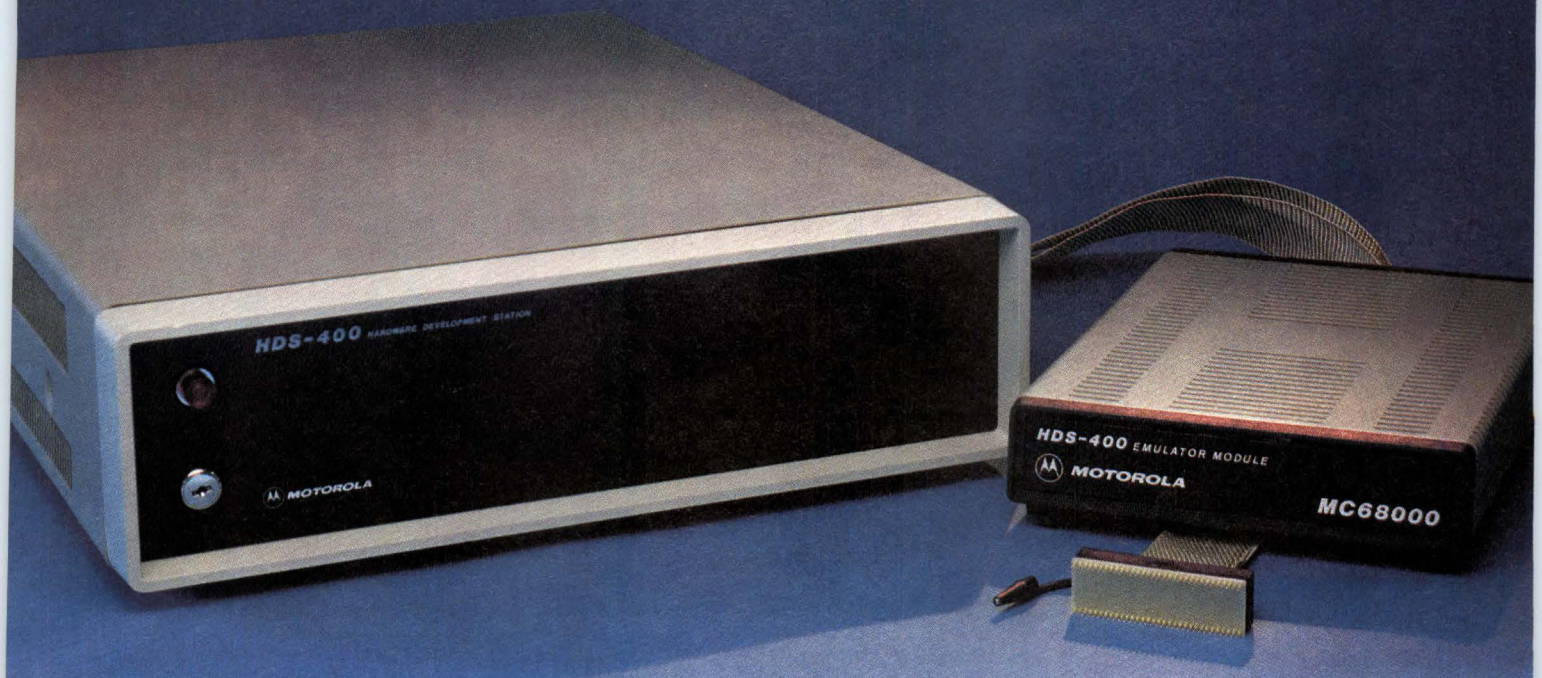


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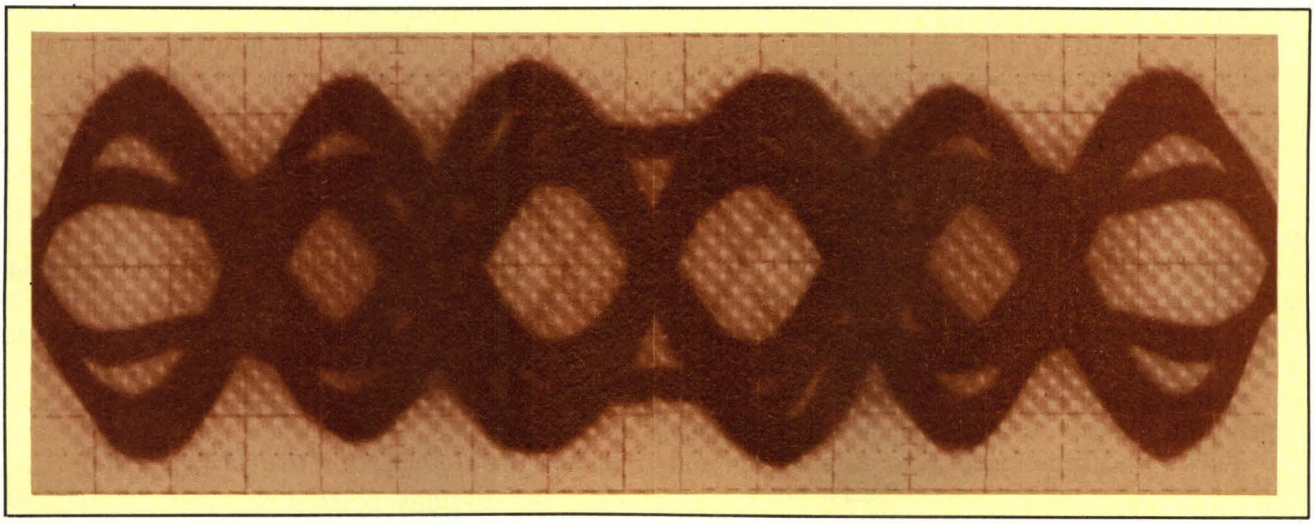
**CIRCLE 48**

# EVALUATE DISK-DRIVE PERFORMANCE WITH MARGIN ANALYSIS

**Most performance testing of disk drives is costly and time consuming, but margin analysis provides a fast, accurate appraisal of a drive's error rate.**



**by Nigel D. Mackintosh**

Disk drives offer one of the most popular and convenient means for storing large amounts of data. But problems can crop up if the recovered information fails to match what was originally put on the disk. Both users and manufacturers of disk drives realize that these machines will occasionally produce errors, and that a method is needed for evaluating the so-called soft-error rate of a drive. Indeed, error-checking methods are available. However, most are so time consuming that a user might be occupied for days or weeks before obtaining meaningful results.

To reduce the time required to check drive performance, the technique of margin analysis is used to examine the inner workings of the read/write circuitry. Margin analysis actually involves a number of techniques, some of which permit data evaluation from the disk with just an oscilloscope. Another type of analysis requires the construction of a special decoder board, but this can be expensive and complex, depending on the number of drives to be tested and the frequency of testing. Although even simple margin analysis testing gives very useful information about disk drive operation, more elaborate tests can provide some of the most useful tools available to both drive designer and manufacturer.

A drive's performance is determined by testing it against its rated specifications. However, not every specification needs to be tested, and some characteristics are not relevant to margin analysis. Therefore, a starting point for margin analysis begins with knowing which drive parameters are important, and which can be safely neglected.

Key specifications for the Century Data Systems Advanced Marksman disk drive (AMS 315), a 315-Mbyte machine, are listed in the Table. The first item—capacity—should be checked initially. But once verified, it need not be rechecked in drives of the same type since it is fixed by many

*Nigel D. Mackintosh is director of storage technology at Century Data Systems, PO Box 3056, Anaheim, CA 92803. He holds a BS in computer science and a PhD in magnetic recording from the University of Manchester, England.*

| AMS 315 Drive Specifications | |
|---|---|
| Capacity (unformatted) | 315.2 Mbytes |
| Data rate | 1.209 Mbytes/s |
| Access time—track-to-track | 6 ms |
| average | 25 ms |
| Latency (average) | 8.3 ms |
| Rotational speed | 3600 rpm |
| Lineal recording density | 6050 bits/in. |
| Track density | 712 tracks/in. |
| Number of cylinders | 845 |
| Recording method | MFM |
| Seek-error rate | 1 in $10^6$ seeks |
| Bit-error rate (soft) | 1 in $10^{10}$ bits |

other well-defined parameters. This also holds for the data rate. After initially verifying this specification, it is highly unlikely to change in the same model drive from the same vendor.

Access time is another story. It is highly dependent on both electrical and mechanical drive components, and should be checked for each drive. Track-to-track access time may be about 6 ms and average access time only 25 ms. The most lengthy tests are for average access time measurement, but to run 1000 of these still only takes 25 s.

Latency is a reasonably stable parameter that depends on the drive's rotational speed. It is easily and quickly checked. Lineal recording density and track density are on most spec sheets, but for the user, they are irrelevant as long as the error rates are acceptable. The number of cylinders is critical for proper mapping of information, but once checked and verified, it will not vary from drive to drive. Likewise, the recording method is not of significance to a user since most experts agree that the differences between the various codes are quite small.

A good seek-error rate is typically defined as less than one seek error in $10^6$ seeks. To perform $10^6$ random seeks can take several hours, and the test should be repeated several times to obtain a good average. However, experience shows that most causes of seek errors have catastrophic rather than continuous effects. Thus, a drive either fails the specification test miserably or exceeds it comfortably. In practice, therefore, a short test for this parameter is usually sufficient.

Finally, there is a bit-error rate—sometimes called raw or soft-error rate—typically specified as less than one error in $10^{10}$ bits. A quick calculation shows how long it can take to test for the parameter. Assume an average access time of 25 ms, and an average block of data to be 256 bytes. This gives an average transfer rate during random seeks of 256 × 8 bits every 25 ms, or a rate of 80 kbits/s. To check for an error rate of 1 bit in $10^{10}$, statistics mandate that the check should be for 10 times that many errors, and then averaged. In other words, the test should be for 10 errors in $10^{11}$ bits transferred. But to transfer $10^{11}$ bits takes [$10^{11}$/80k] seconds, or approximately $10^6$ seconds, which is 15 days.

Obviously, testing the bit-error rate puts a tremendous burden on manufacturers who must potentially check hundreds or thousands of units. Fortunately, there are various techniques for getting around the problem of fully testing the soft-error rate specification on a disk drive. But first, a designer must understand what occurs when there is an error in received data.

### Recovering disk data

In a typical read/write circuit, incoming nonreturn to zero (NRZ) data and the write clock pass through an encoder and the write driver. They then go to the write head for the appropriate flux transitions to be written on the disk (Fig 1). During data recovery, flux transitions excite the read head and the resulting voltage passes through a preamplifier, filter, differentiator, and a zero crossover detector to form the data transitions. At this point, the data splits. One part goes into a phase lock loop (PLL), which creates a data window. This is used to clock the data transitions into a decoder to permit recovering NRZ data and to send it with a read clock to the controller.

*A good seek-error rate is typically defined as less than one seek error in $10^6$ seeks.*

The typical waveforms of this operation are illustrated in Fig 2. Five data bits are defined, representing the pattern 00101. The top trace is the write current according to modified frequency modulation (MFM) rules. MFM is a very common recording code defined such that a logic 1 data bit causes a change in the write current in the center of the bit cell. Logic 0 data does not cause a change in the write current except when two 0s occur in succession. This produces a change in the write current (see the top waveform) causing a change in the direction of magnetization of the disk. Note that these changes in magnetization direction coincide with the peaks of the pulses in the readback voltage.

The objective is to detect these peaks since they define the original data. The best way to detect peaks is by differentiating the signal and finding where the value equals zero. Note that the zero value of the differentiated signal corresponds to the peak value of the data signal. Next, the differentiated wave is squared to allow the recovery of

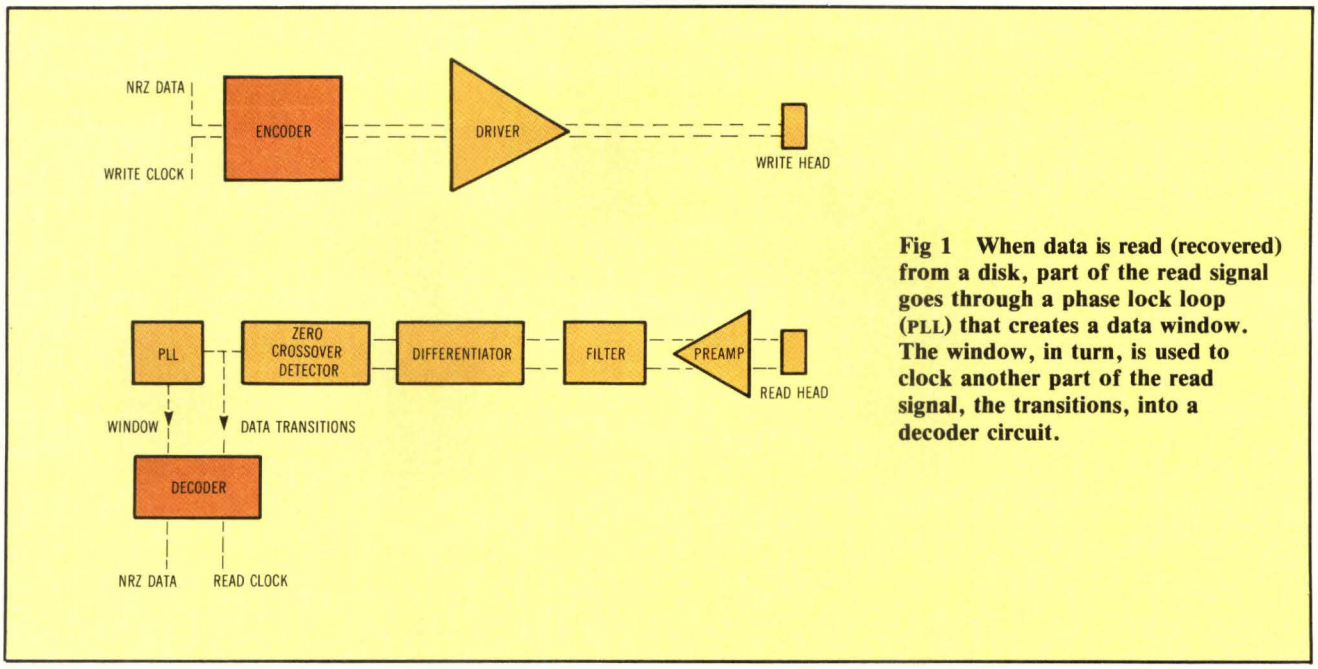



**Fig 1 When data is read (recovered) from a disk, part of the read signal goes through a phase lock loop (PLL) that creates a data window. The window, in turn, is used to clock another part of the read signal, the transitions, into a decoder circuit.**

the original write current. From this, one can deduce the original data pattern.

First, it must be determined whether the data transitions occur in the center of a bit cell or on the junction of two bit cells. This indicates whether the transition represents a logic 1 or a pair of logic 0s. The function of the PLL is to provide a signal that delineates the center of a bit cell from the edges. This waveform, called the data window, is shown at the bottom of Fig 2. The high portion in each cell is known as the "ones window" because if a transition occurs in the readback in this window, a logic 1 must have been recorded. It is common practice to look only for the logic 1s transitions since the absence of a 1 transition automatically means the bit was a logic 0.

Unfortunately, the real world is not as well defined as the waveshapes of Fig 2 indicate. In practice, recovered transitions are not perfectly located in the center or at the edges of the bit cells. This results from noise picked up from the disk and noise introduced by the preamplifier. Interference of the readback pulses also causes the waveform to distort and introduce so-called peak shift. Moreover, the PLL generates some timing jitter, and the delay through the read amplifier is not constant at all frequencies, causing additional distortion. Finally, interference results from previous data incompletely overwritten or from data on adjacent tracks of the disk.

## Analyzing disk data

A distribution can be plotted to show the results of various types of noise introduced to data on a disk [Fig 3(a)]. The horizontal scale represents the data window of a drive with a 100-ns wide bit cell and using MFM code. The width of the data window is half that of the bit cell, or 50 ns. On the vertical scale is the probability density of a given transition occurring at any point within the data window. According to this all ones pattern curve, the vast majority of transitions fall perfectly in the middle of the data window.

In fact, the curve is basically a Gaussian, or normal, distribution because Gaussian noise introduced by the disk and preamplifier is usually the dominant cause of timing errors. From the curve, it appears that there is little chance of a transition falling outside the data window. Theoretically then, there is little chance of misreading the data. The problem with the curve however, is that the error-rate specification is just one error in $10^{10}$ bits (a probability of $10^{-10}$) and this is not easily seen on a linear scale.

A better representation of the data in Fig 3(a) is provided by using a curve with a logarithmic vertical scale as shown in Fig 3(b). The distribution of

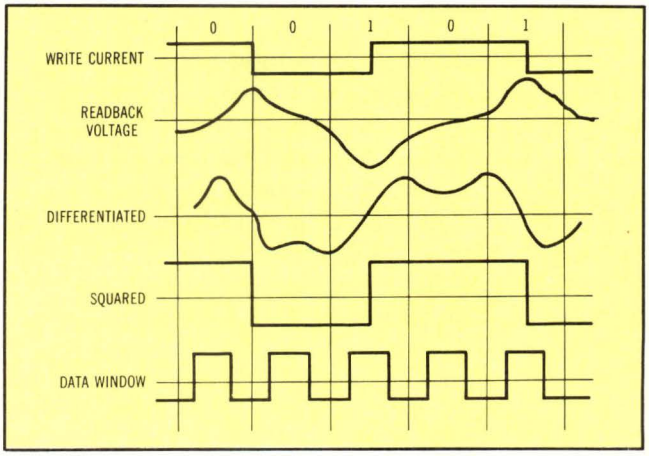



**Fig 2 The read/write waveforms from the disk circuitry are shown here. Data window pulses serve to define the center of a bit cell. Data transitions must occur correctly in a bit cell, otherwise an error will be recorded.**

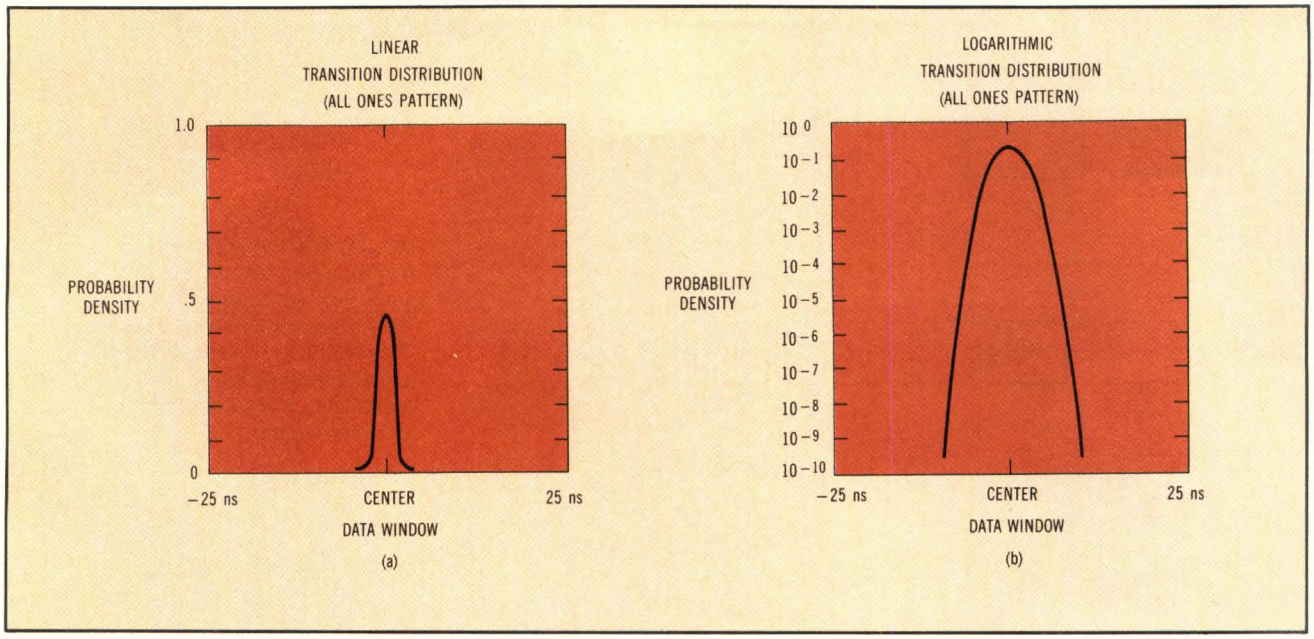



**Fig 3 A linear transition distribution plot shows where in the bit cells recovered data falls. In plot (a), all recovered logic 1 data bits appear to fall very near the center of the 50-ns wide window. A more accurate determination of data distribution is provided by a logarithmic distribution plot (b). Only one transition in $10^{10}$ bits occurs as much as 10 ns away from the center of the data window.**

both curves is the same, but Fig 3(b) shows more clearly that once in every $10^{10}$ bits, a transition will occur 10 ns away from the center of the window on each side. But this still leaves a 15-ns margin on each side before an error will occur.

A distribution for a "peak shift" pattern—an MFM 110110 repeating pattern—is graphed in Fig 4. Here, the two transitions in the pair oppose each other and push apart. This produces a fixed shift in the two peaks, one to the left and one to the right of center. The curve results from the transfer of a huge number of bits (approximately $10^{11}$) and each one has been examined to determine exactly where in the data window it fell. The curve shows that many of the bits fell 7 ns to the left of center and equally as many fell 7 ns to the right. This represents the amount of peak shift introduced into the curve.

A normal Gaussian distribution around each of the two nominal peaks is graphed. In effect, it is a bimodal distribution that clearly shows the amount of peak shift, as well as the signal-to-noise ratio as shown by the slope of the curve.

Ideally, all recovered data transitions should fall in the middle of the data window, but this is not a practical, absolute necessity. That is, transitions can move around inside the window as long as they do not jump out, since that would cause an error. Transitions should stay away from the window edges, giving a greater degree of noise margin.

## Using margin analysis techniques

Information derived from various types of distributions can be used to estimate the normal error rate without having to wait days or weeks for an answer. The first and simplest margin analysis method is called the eye pattern.

In the eye pattern method, an oscilloscope is used to examine the differentiated readback signal. The scope is triggered from one zero crossing to permit examination of subsequent zero crossings as shown in Fig 5. Three different data patterns are superimposed here to show the effects of random data transfers. On a drive having good noise margins, transitions occur fairly accurately and consistently. The "eyes" or loops will therefore be very large. In the bad margin case, shown to the left of the Fig 5,

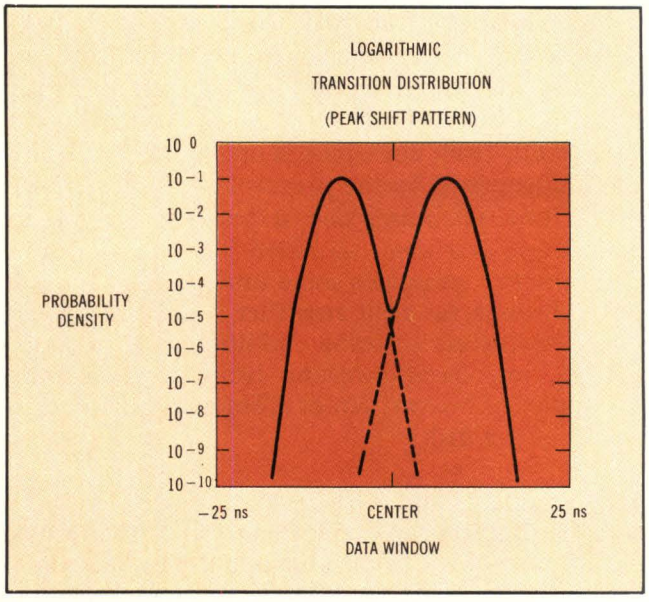



**Fig 4 This logarithmic distribution plot results from distortion introduced on the read signal by components of the readback system.**

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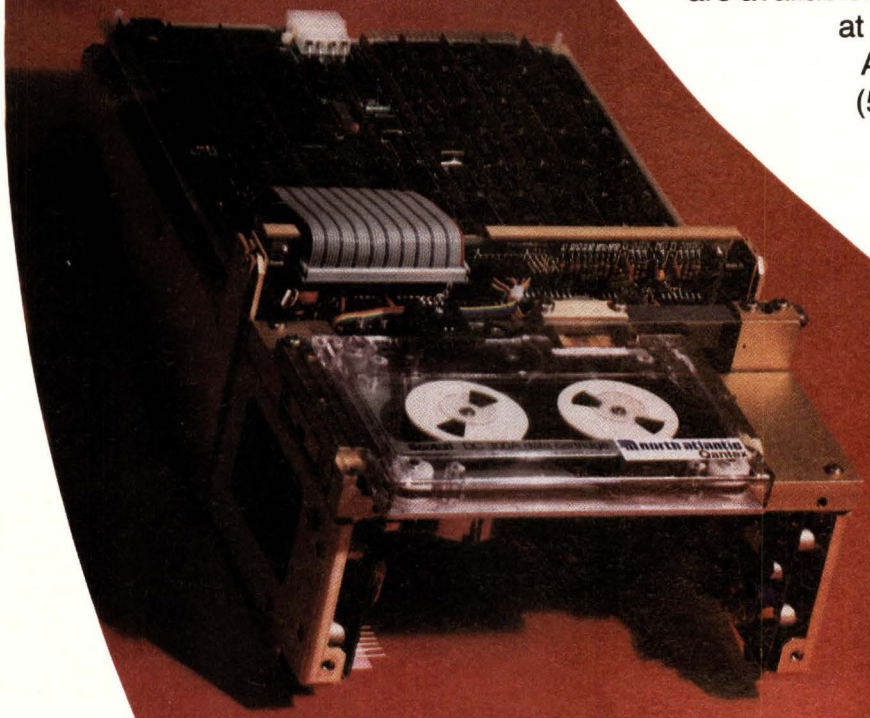

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succeeding zero crossings occur at different points in time. Thus the eyes appear small or almost closed. The advantage of the eye pattern is that it requires very simple equipment and is the fastest method for analyzing a drive's performance.

A second margin analysis technique, window sliding, can also be performed with an oscilloscope. Fig 6 shows the relationship between the data window and data transitions, as well as a typical distribution plot for a peak-shift pattern. The number of transitions that occurs at the edges of the window is virtually nil; that is, the probability of a transition falling on either edge of the data window is far less than 1 in $10^{10}$. (If $10^{10}$ bits were transferred, not one would be expected to fall outside the data window.) But what happens if everything remains the same, and the data window is slid slightly to the right, as shown in Fig 6?

If the data window is moved 15 ns to the right, it is apparent that many transitions will fall outside the left-hand edge of the window. In fact, the probability from the plot is roughly $10^2$. For every 100 bits transferred, on average, one would fall outside the data window. Therefore, window sliding provides a method for artificially increasing the error rate of a disk drive.

Window sliding is used in the following manner. If the data window position is easily alterable on the drive (perhaps by a potentiometer), set the drive to transfer data continually and adjust the potentiometer to slide the window until a fairly large number of errors occurs (eg, about one error per second). Depending on the particular test used, it is possible to be on a track transferring data, or seeking between tracks and transferring data. This might represent an error of 1 in $10^6$ or $10^7$. By measuring how far the window has been shifted with the scope's time base, the amount of margin for a particular error rate is determined.

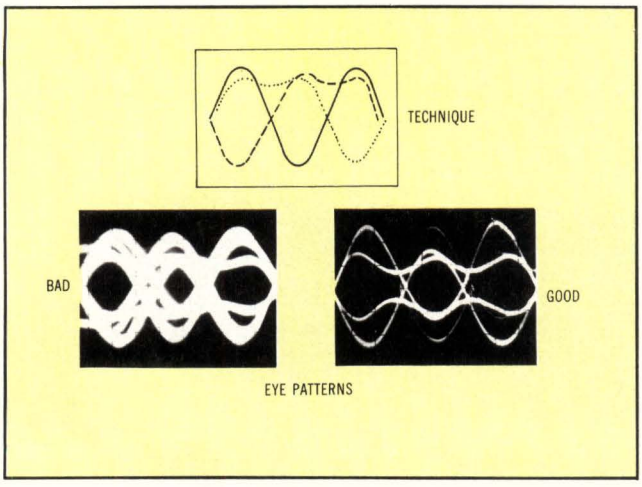


**Fig 5 Eye pattern analysis is the simplest, fastest method for judging the error-rate performance of a disk drive. An "open eyes" pattern (on the right) indicates that data transitions occur at consistent points in time. Thus, the drive has adequate error margins.**

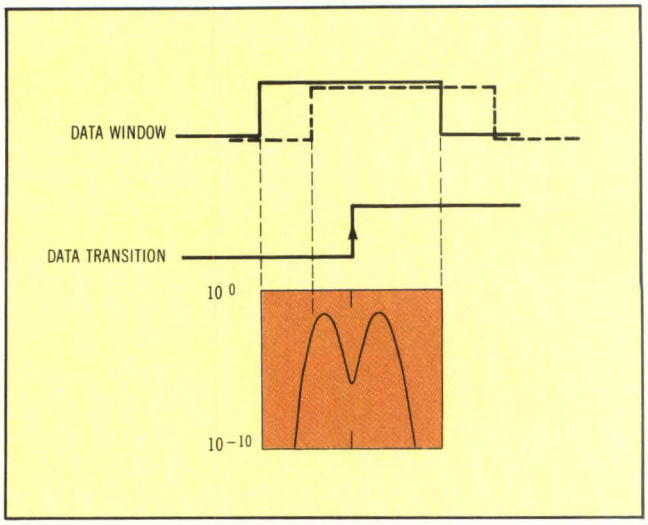


**Fig 6 A window sliding technique provides a quantitative measure of a drive's error-rate performance. By moving the data window (sliding it in time), it is possible to determine the number of transitions that will fall outside the window. This technique is much more accurate than eye patterns since the error rate can be calculated numerically.**

For example, assume that it is possible to slide the window 10 ns on the left-hand side at an error rate of $10^7$. By consulting the typical slope of the transition distribution curve, it can be extrapolated that at the $10^{10}$ error rate the drive has about an 8-ns noise margin. Sliding the window in the opposite direction produces a similar result for the other side.

Although window sliding is more sophisticated than eye patterns and gives a quantitative measure of the margins, it is not always possible to slide the window in a drive. Even if sliding is possible, it is difficult to know if the drive's operation is disturbed by such sliding. It is possible to interfere with the normal operation of the phase lock loop by artificially changing the relationship of data transitions in the window. This can invalidate the data.

Despite these drawbacks, window sliding is a useful technique. By moving the data window in increments, a transition distribution plot similar to the one in Fig 6 can be produced. However, better methods exist, and these are best performed with a dedicated decoder board.

It has been shown how the data window and data transition signals both feed into the decoder. If both signals can be brought offboard, a dedicated variable window decoder can be built specifically for margin analysis. Since this decoder board will be used to test all disk drives, it can be built as complex as is required to do the job.

The controller in charge of the testing ignores the read data and read clock sent from the drive's normal read channel. Instead, it takes these signals from the variable window decoder. The entire process can be automated in the controller so that it slides the window in increments and measures the error rate for each increment. This method ensures that all drives meet acceptable margins.

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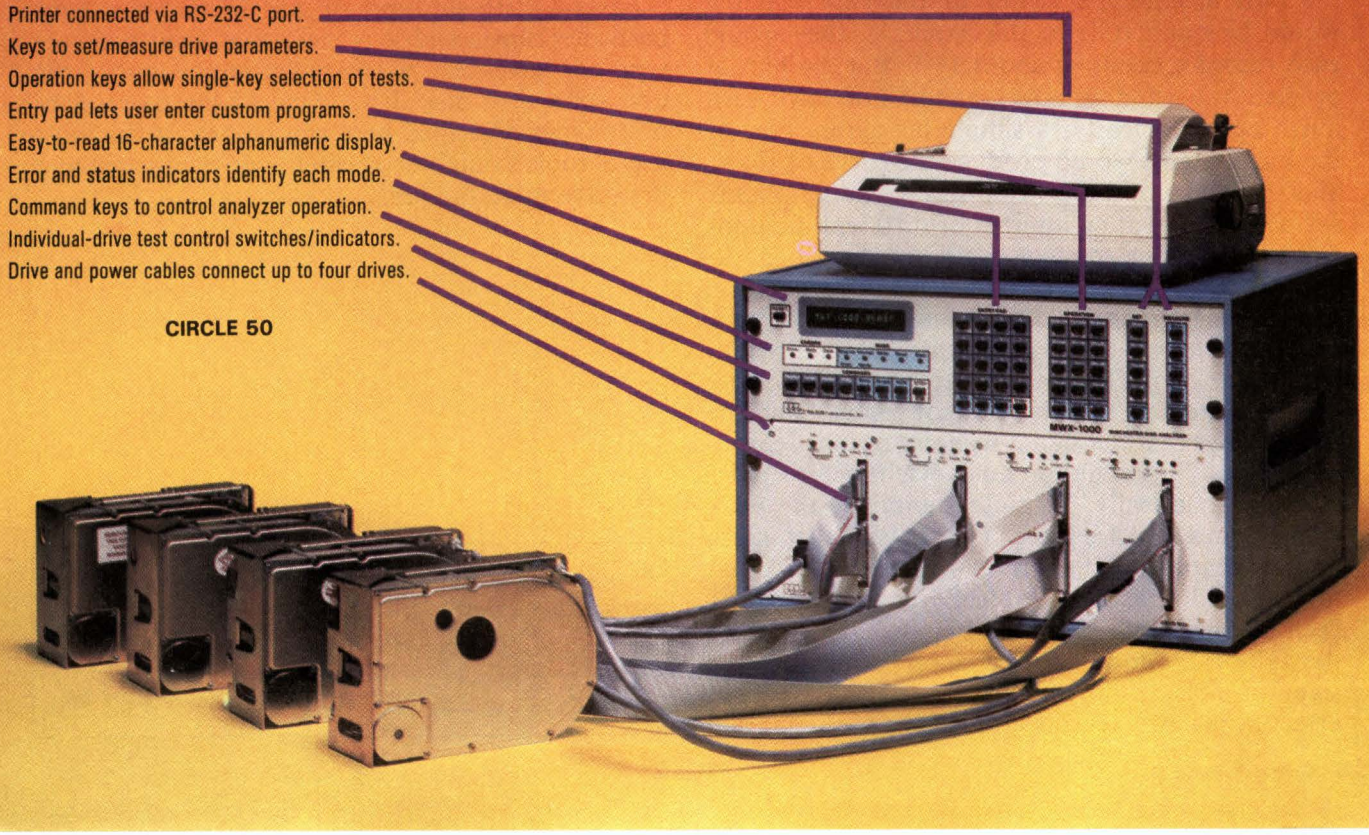


CIRCLE 50

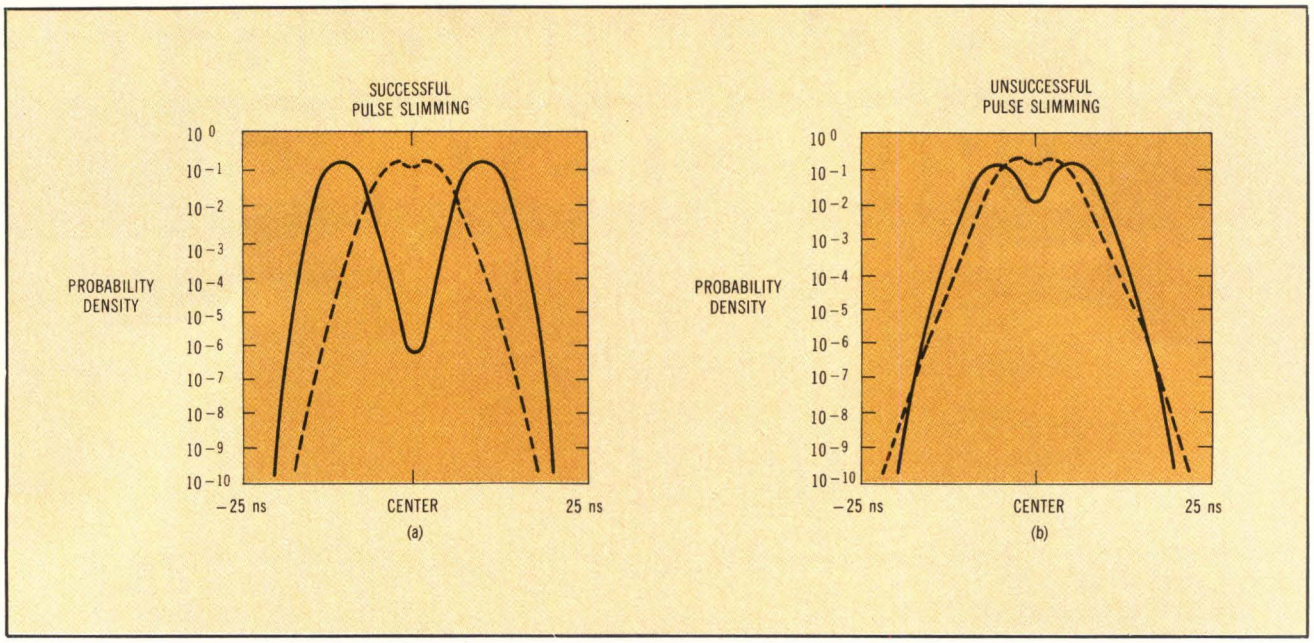


**Fig 7 Pulse slimming is a trade-off technique whereby peak shift is reduced but signal-to-noise ratio is degraded. Plot (a) shows that successful slimming improves the margin. Plot (b) is not a good candidate for pulse slimming since the margin gets worse after slimming is applied.**

One other margin analysis technique exists. The objective is to gather data to generate a typical transition distribution plot such as that shown in Fig 4. Assume that the data window is divided in 1-ns increments—50 increments as shown in the time base of Fig 4. Consider these increments to be 50 buckets or bins. Assume further that $10^{11}$ data bits are transferred, and on each transition, the occurrence is stored in its appropriate bin. For each transition that goes into a particular bin, the numerical count of that bin is increased by one.

At the test's conclusion, it would be likely that the bins around the center of the data window would be quite full. In this example, they would each record a count of about $10^{10}$. But the bins at or near the window edges would not have seen much action. Clearly, a simple histogram plot of the bin contents would produce the curve of Fig 4, and the peaks in the distribution would be plainly revealed. There are a number of different methods for implementing the technique just described.

### Applying margin analysis to disk drive design

Fig 7(a) illustrates a normal peak-shift distribution (solid line). The peak shift is well defined—approximately 10 ns either side of center—and the slope shows that the signal-to-noise ratio is reasonably good. This situation lends itself well to pulse slimming. Basically, in pulse slimming, the peak shift is improved (reduced) but the signal-to-noise ratio is degraded. The dashed-line plot shows that the peak shift has been reduced to about 2.5 ns on each side by pulse slimming but that the slope of the fall-off is now less steep, indicating that the signal-to-noise ratio has been degraded. The net effect at the $10^{10}$ level is an increase in the margin from 5 to 8 ns on each side, so the technique is judged to be successful.

By contrast, the plot of Fig 7(b) shows an unsuccessful application of pulse slimming. The solid line curve here starts out with just 5 ns of peak shift on either side of center and a fairly poor signal-to-noise ratio. This gives the same result as in Fig 7(a), namely that the margin at the $10^{10}$ level is 5 ns on each side. However, pulse slimming reduces the peak shift from 5 to 2 ns, and again degrades the signal-to-noise ratio. But the overall result is a loss in margin at the $10^{10}$ level from 5 to 3 ns.

Several different types of margin analyzers have been described, and it is clear that even a simple type can give very useful information about the operation of a disk drive. One of the more elaborate types described here can be one of the most useful tools available to both the drive designer and the drive manufacturer.

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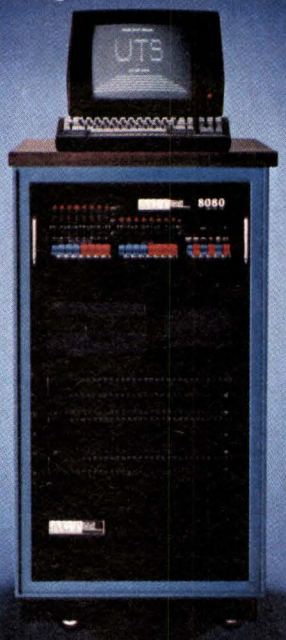


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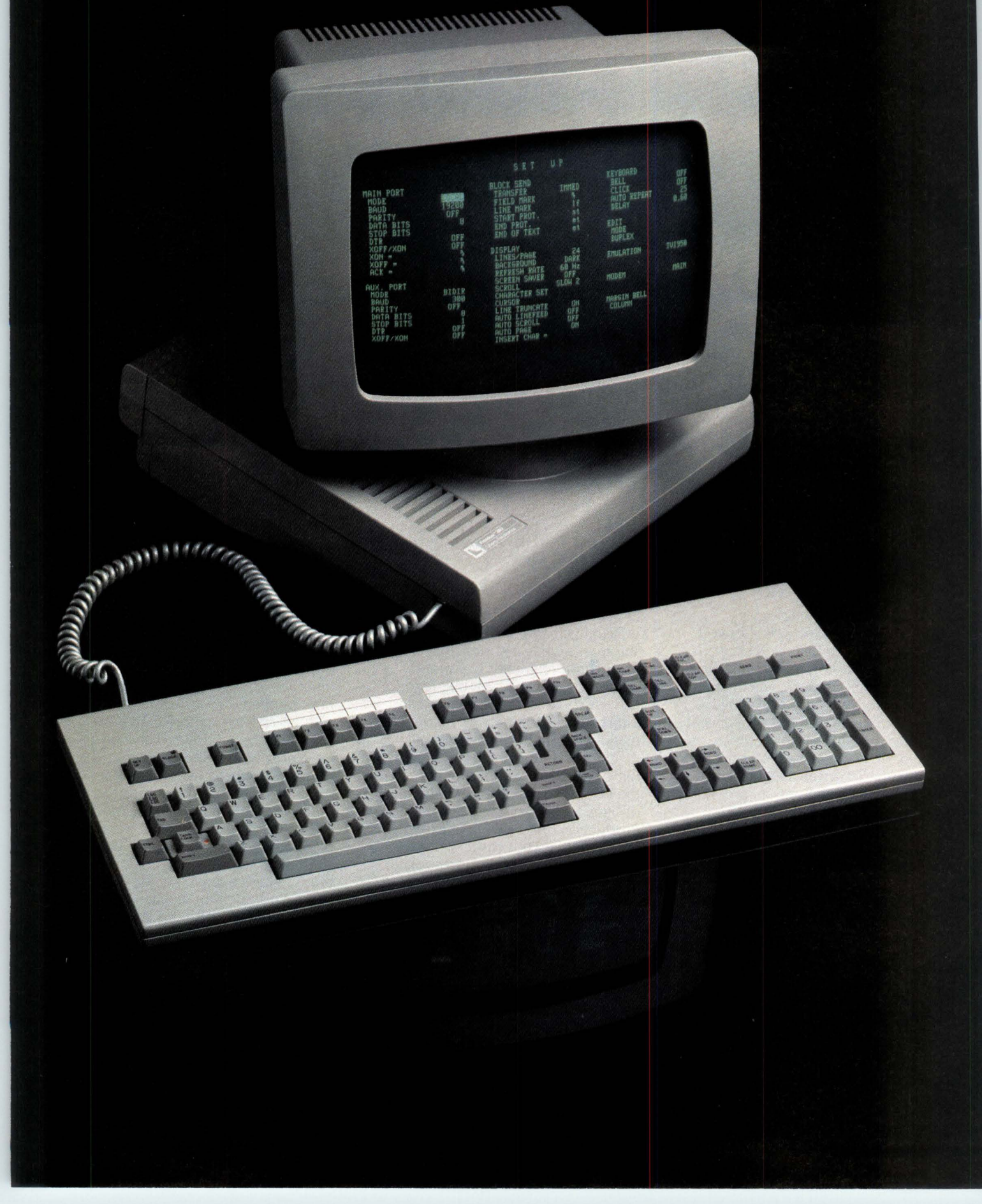
SET UP
MAIN PORT
MODE
BAUD
PARITY
DATA BITS
STOP BITS
DTR
XOFF/XON
XON =
XOFF =
ACK =
AUX. PORT
MODE
BAUD
PARITY
DATA BITS
STOP BITS
DTR
XOFF/XON
BLOCK SEND
TRANSFER
FIELD MARK
LINE MARK
START PROT.
END PROT.
END OF TEXT
DISPLAY
LINES/PAGE
BACKGROUND
REFRESH RATE
SCREEN SAVER
SCROLL
CHARACTER SET
CURSOR
LINE TRUNCATE
AUTO LINEFEED
AUTO SCROLL
AUTO PAGE
INSERT CHAR =
IMMED
24
DARK
60 Hz
OFF
SLOW 2
ON
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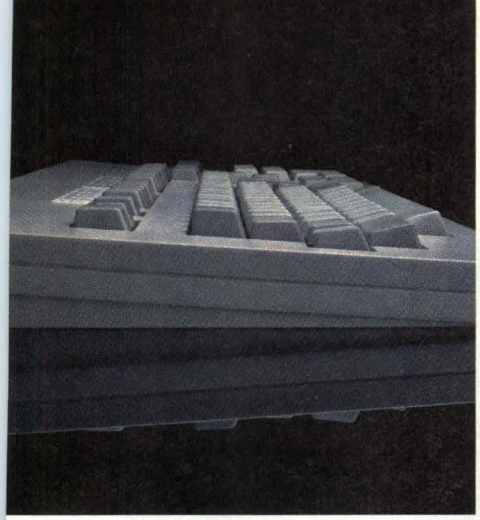

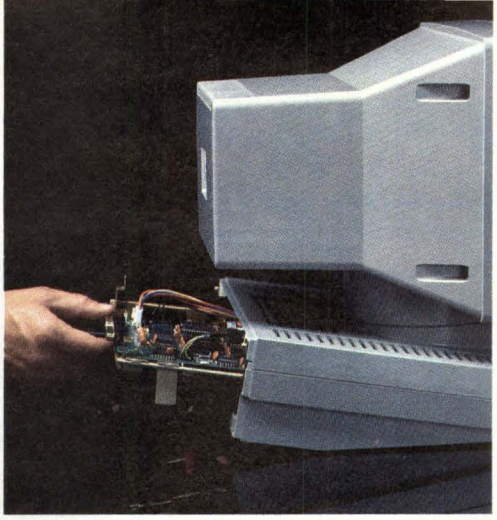

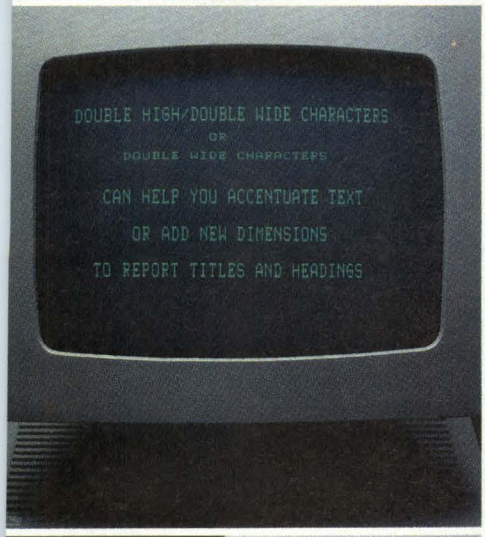

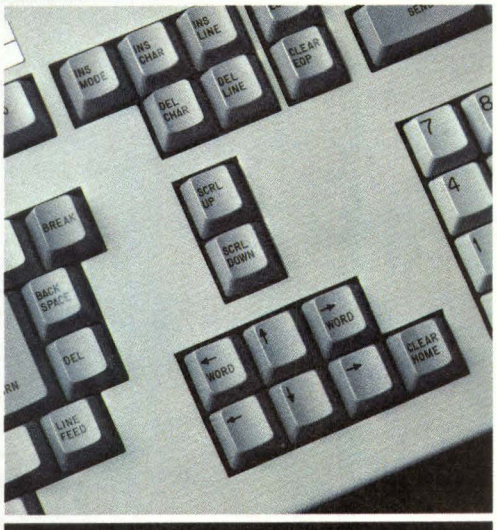


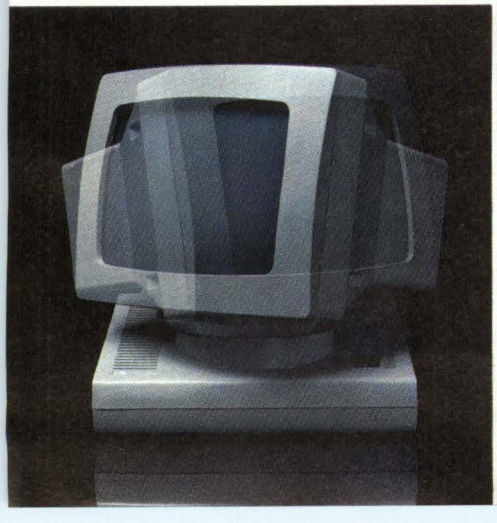

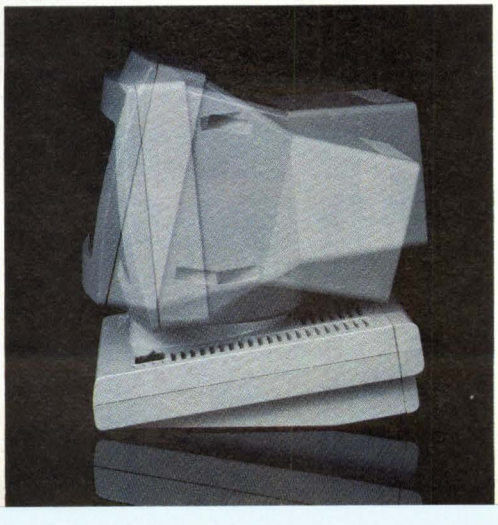

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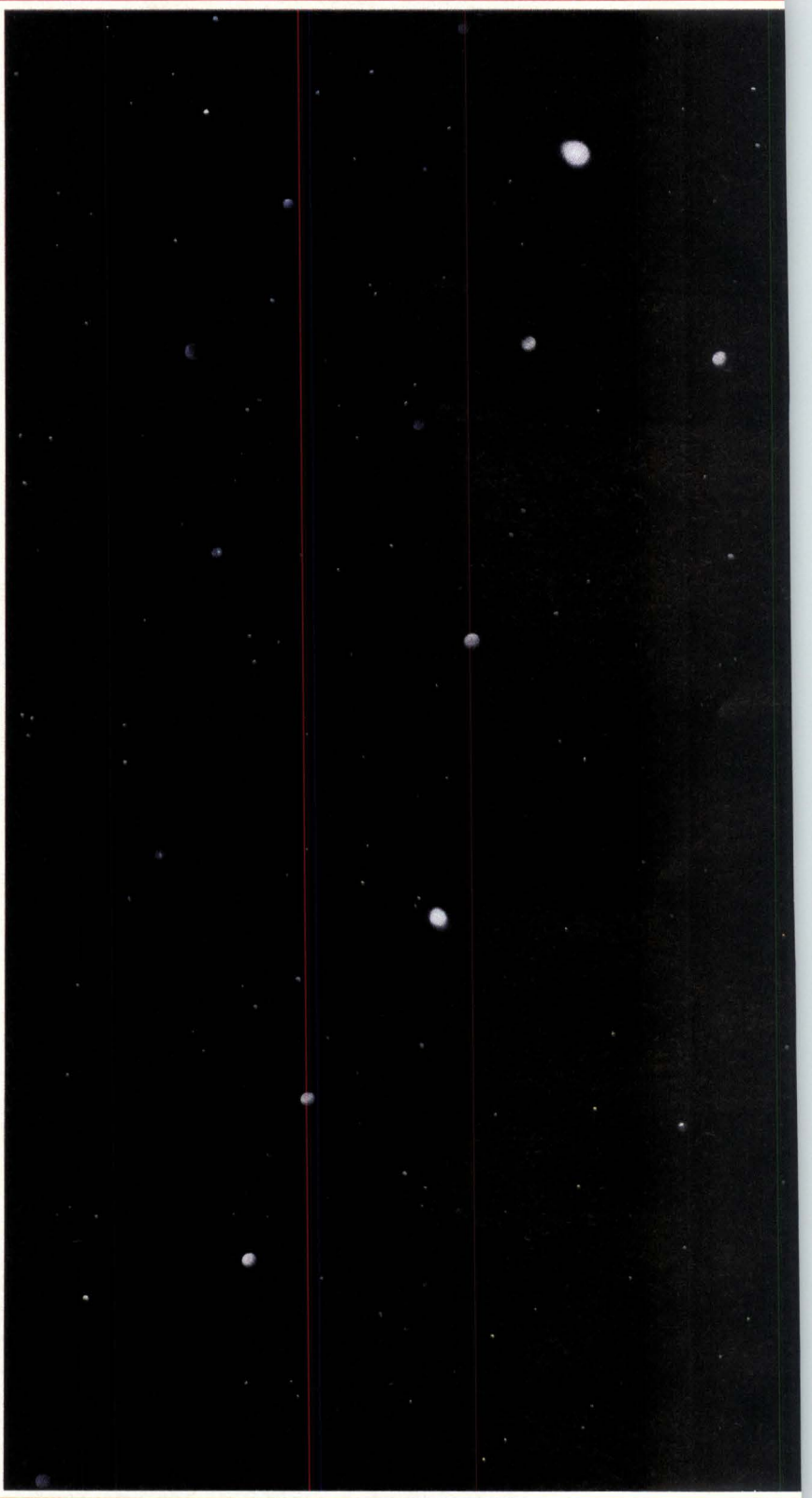

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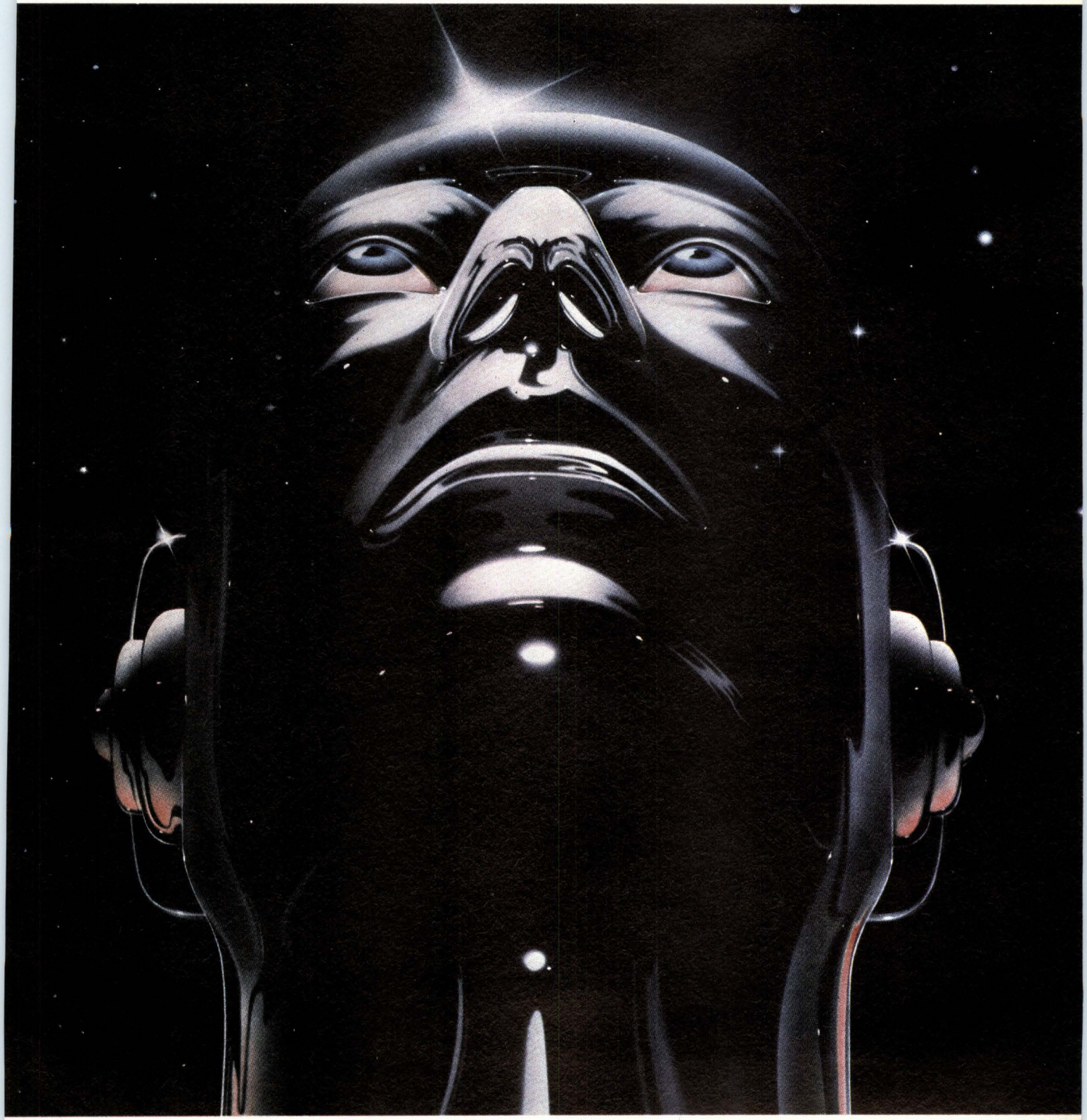

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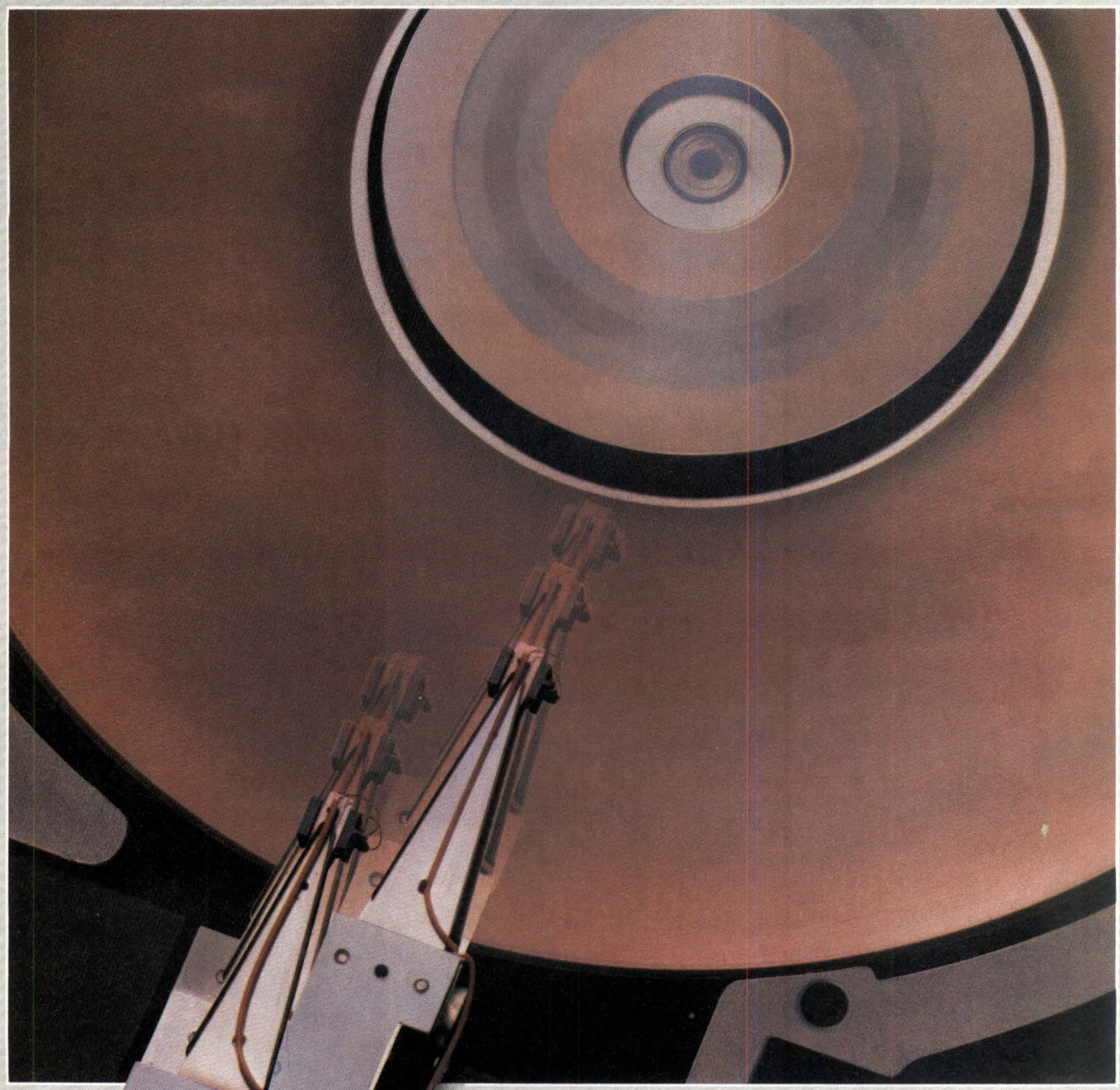

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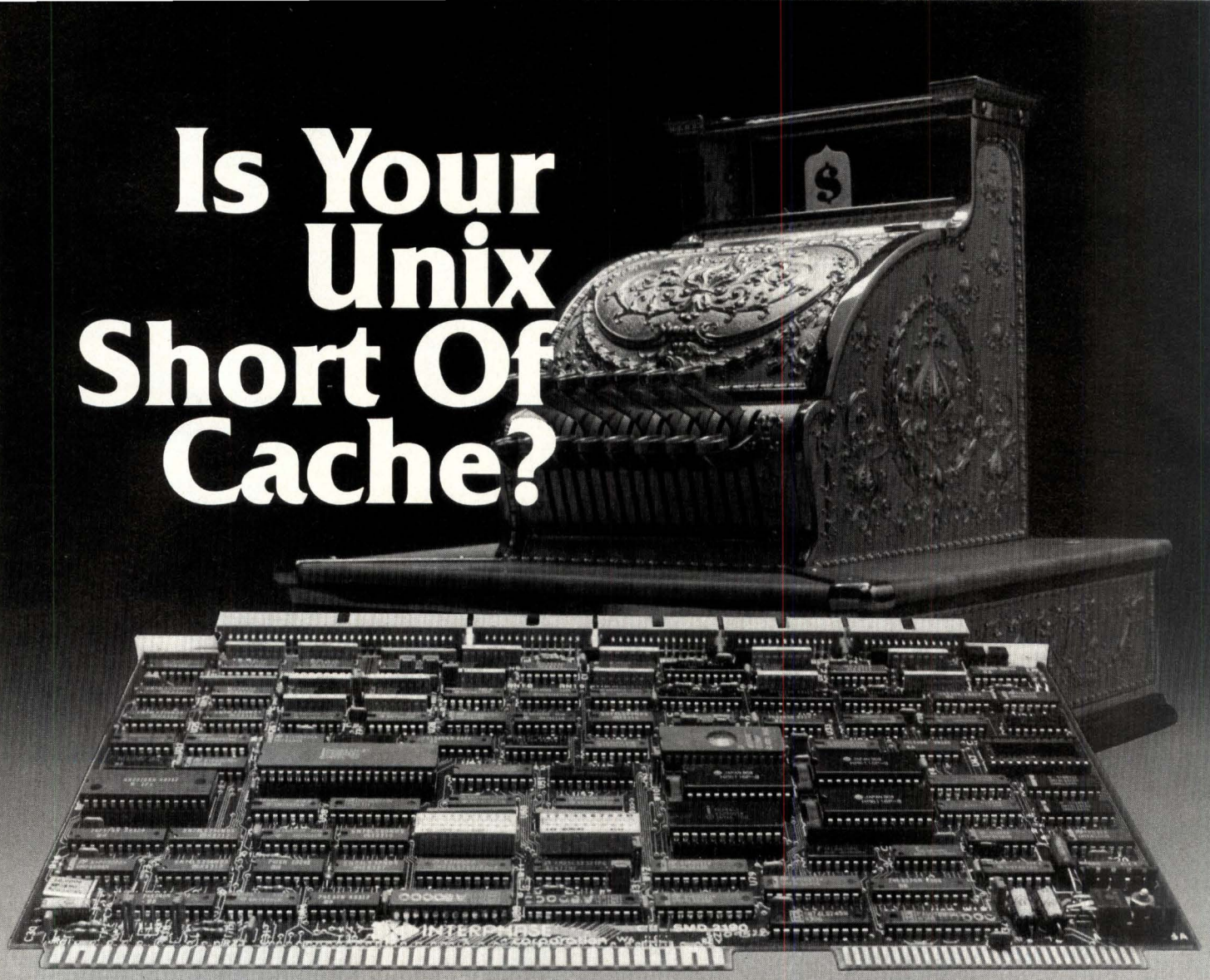

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CIRCLE 55

# DISK CONTROLLER CHIP RUNS ON SIMPLE SOFTWARE ROUTINES

## Successful integration of programmable controllers into computer systems requires devices whose command set unburdens both the host processor and the system designer.

by David Davidian

As hard disk drives become the chief mass storage media for small and medium computer systems, a number of dedicated hard disk control ICs have emerged to offload the host processor's task in controlling hard disk drive operation. One of the latest ICs of this type is NEC's μPD7261 hard disk controller (HDC). The chip is designed to control disk drives that support either a hard- or soft-sectored disk format. In addition, the HDC provides all control signals for interfacing a processor to a hard disk drive with a storage module device (SMD) interface, or to the popular floppy-like hard disk interface drives manufactured by Seagate Corp (ST506).

Programmable peripheral chips such as the 7261 have evolved to the point that the system integrator's task is concerned more with software rather than hardware aspects. Thus, designers must rely on the chips to offer sophisticated instruction sets that minimize both chip and processor overhead. Such software is provided in the 7261. For example, all data transfers to and from the disk are handled by the 7261 together with a DMA controller such as the NEC μPD8237.

Features of the 7261 include user-programmable track format and the ability to control up to eight hard disk drives with SMD interfaces, or up to four hard disk drives with a floppy-like interface. It offers parallel-seek capability, and multisector or multitrack data transfers. Data recording formats include modified frequency modulation (MFM) in the floppy-like disk mode and nonreturn-to-zero (NRZ) in the SMD mode. In the floppy-like mode, the maximum data transfer rate is 6 MHz, while in SMD mode, the rate is 12 MHz. Error diagnostic capabilities are either cyclic redundancy check (CRC) or error checking and correction (ECC).

As shown in the 7261 block diagram (Fig 1), the chip is partitioned into three major logical units: the command processor (processing unit), a format controller, and an external interface (port control). The command processor is an 8-bit microprocessor having its own RAM, ROM, and I/O interface. Its key

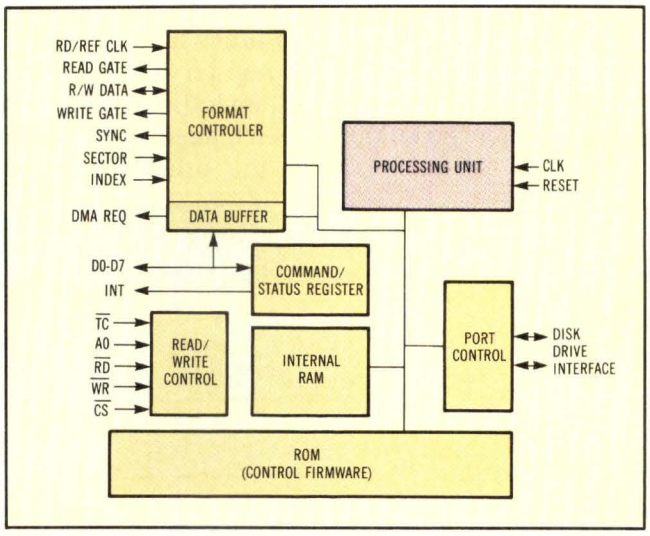


**Fig 1 The architecture of the μPD7261 HDC is centered around its processing unit, external interface and format controller. Disk data I/O operations are handled by the format controller, which executes instructions sent in by the host processor.**

*David Davidian is a software engineer at NEC Electronics USA, Inc, Microcomputer Div, One Natick Executive Park, Natick, MA 01760, where he is responsible for software integration of complex peripheral devices. He holds a BS in nuclear engineering from the University of Lowell.*

functions are to decode commands received from the host CPU, to execute seek and recalibrate commands, to monitor drive status and the interface, and to load the format controller with information appropriate for executing read/write data commands.

The command processor remains idle until it receives a command from the host. The format controller, a hardwired logic processor, executes high speed instructions sent in from the host—one instruction/clock cycle. This processor also handles a variety of tasks including serial-to-parallel and parallel-to-serial conversions from disk accesses, CRC and ECC generation and correction, MFM data encoding and decoding, write precompensation, address mark detection and generation, soft-sector identification (ID) field search and generation, and DMA transfer control.

Interfacing to the 7261 is handled on an I/O-port basis to the host processor. An onchip buffer/register is an 8-byte first-in, first-out (FIFO) type for command parameter loading and command end-result status reading. During DMA operations, the FIFO serves as a data buffer. Two other special registers are provided: the command register is a write-only type into which hard-disk operation codes are entered after the FIFO has been loaded with specific command parameters. On the other hand, the status register is a read-only type that indicates the HDC's status at any time.

### Talking to the HDC

Issuing commands to a μPD7261 is a relatively straightforward operation. Assume, for example, that an input/output parameter block (IOPB), consisting of a command byte followed by command parameters, is previously stored in memory. To get this information into the HDC, the FIFO is loaded first (with the command parameters) and this is followed by the command byte.

The flowchart in Fig 2 illustrates the command loading sequence. First the user may want to set an "Interrupt Completion Flag." This allows the software to detect the completion of the command interrupt servicing. In essence, this indicates that the HDC has executed the command sent, irrespective of any errors. The next step is to issue an auxiliary command, such as the halt sense interrupt status request, to eliminate the possibility of interrupt servicing during command loading. Before the HDC will accept a new command (with the exception of auxiliary commands), bit 7 of the status register, called controller busy, must be low. This is indicated by the first decision block in Fig 2.

If the HDC can accept commands, parameters such as sector and head (for a read-data command)

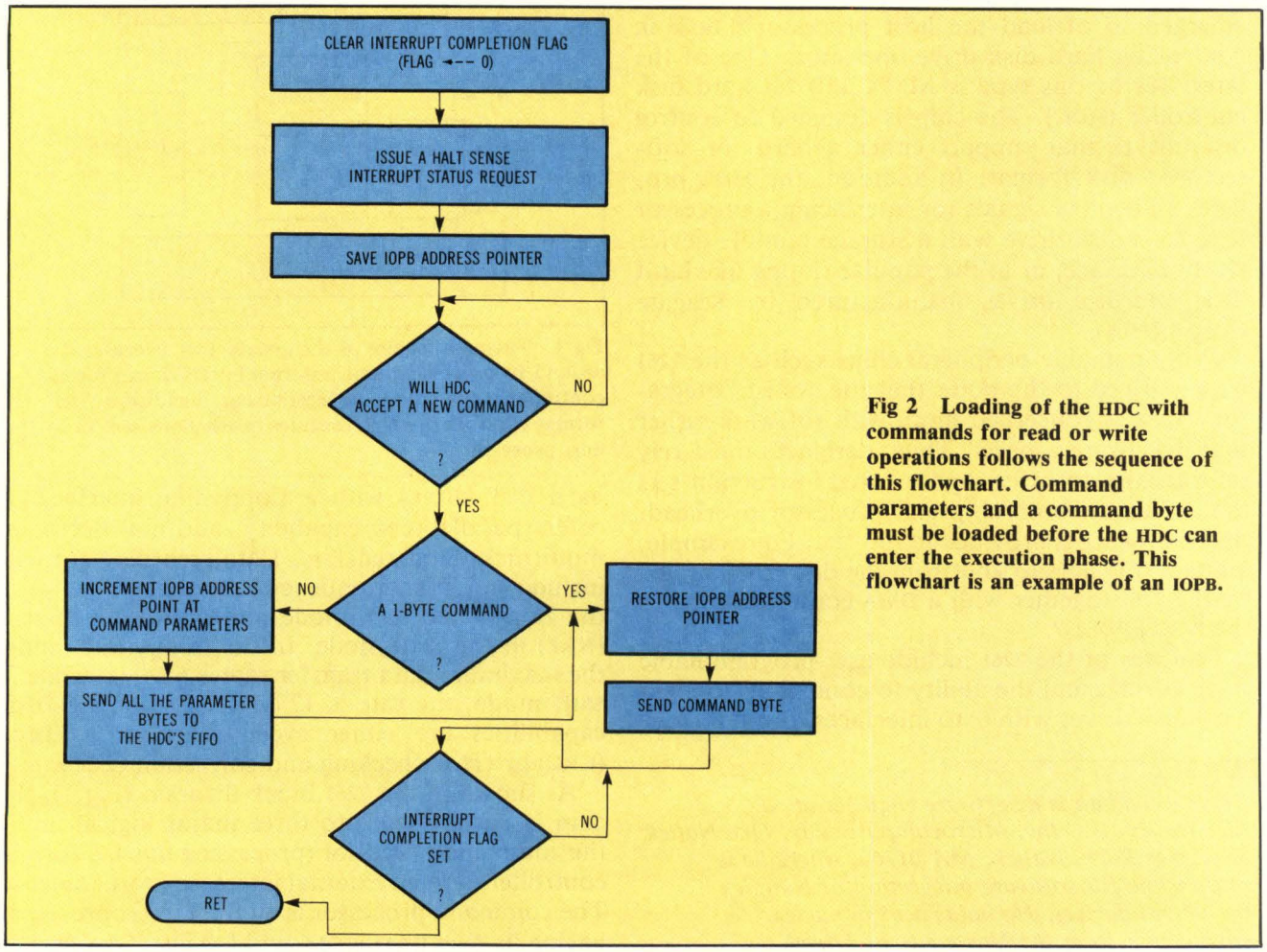


**Fig 2 Loading of the HDC with commands for read or write operations follows the sequence of this flowchart. Command parameters and a command byte must be loaded before the HDC can enter the execution phase. This flowchart is an example of an IOPB.**

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CONTROL DATA

CIRCLE 56

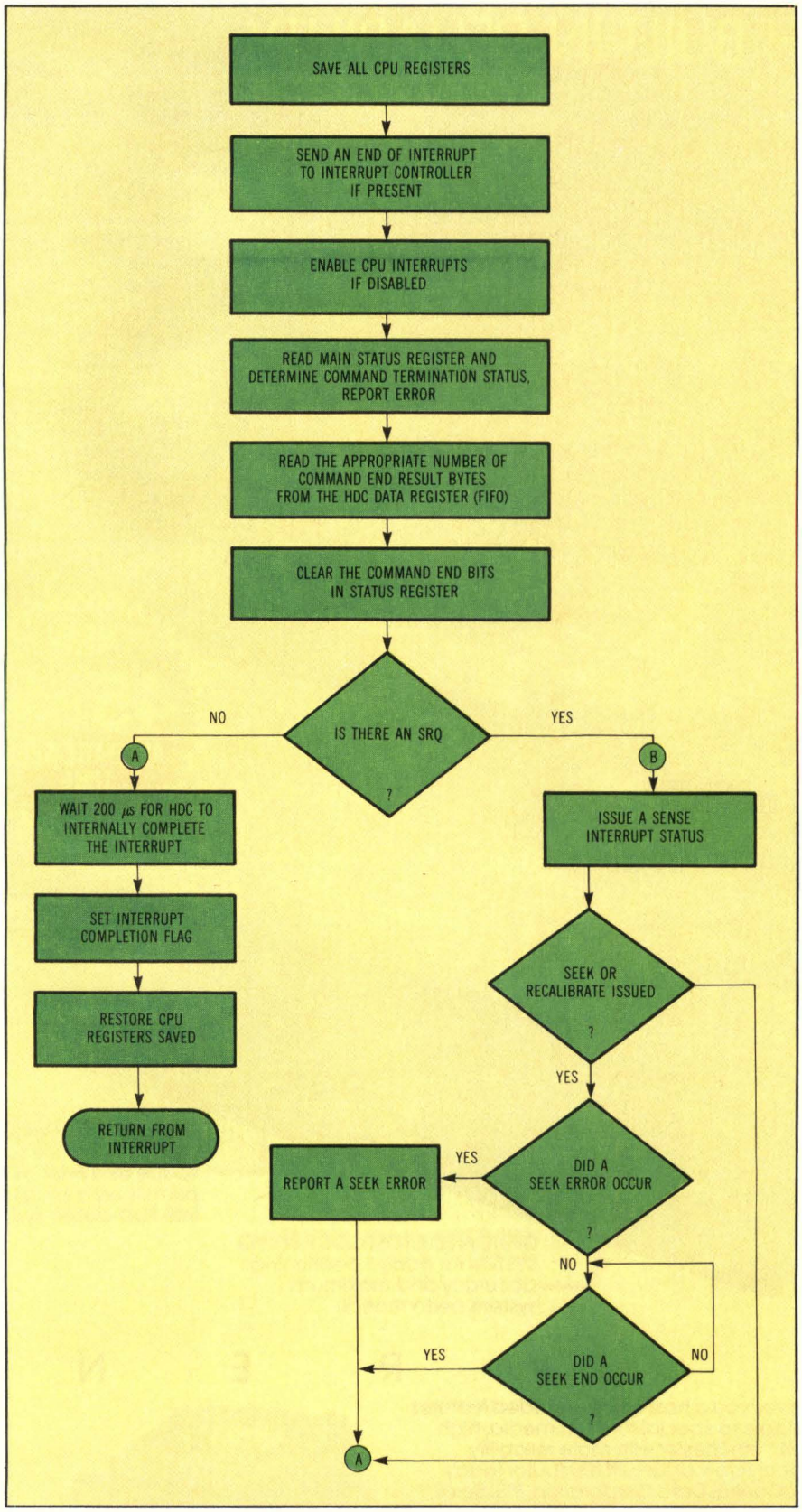



**Fig 3 The HDC's interrupt service routine allows access to the controller's status at command completion. At command-end, the main status register indicates a normal or errored command execution and the need for an SRQ. Result bytes can be used to further describe any errors that occur. The proper interpretation of an SRQ completion is vital to the internals of the HDC.**

are loaded into the FIFO. At completion, the command is loaded into the command register. This concludes the command phase of instruction execution and the 7261 proceeds to the execution phase.

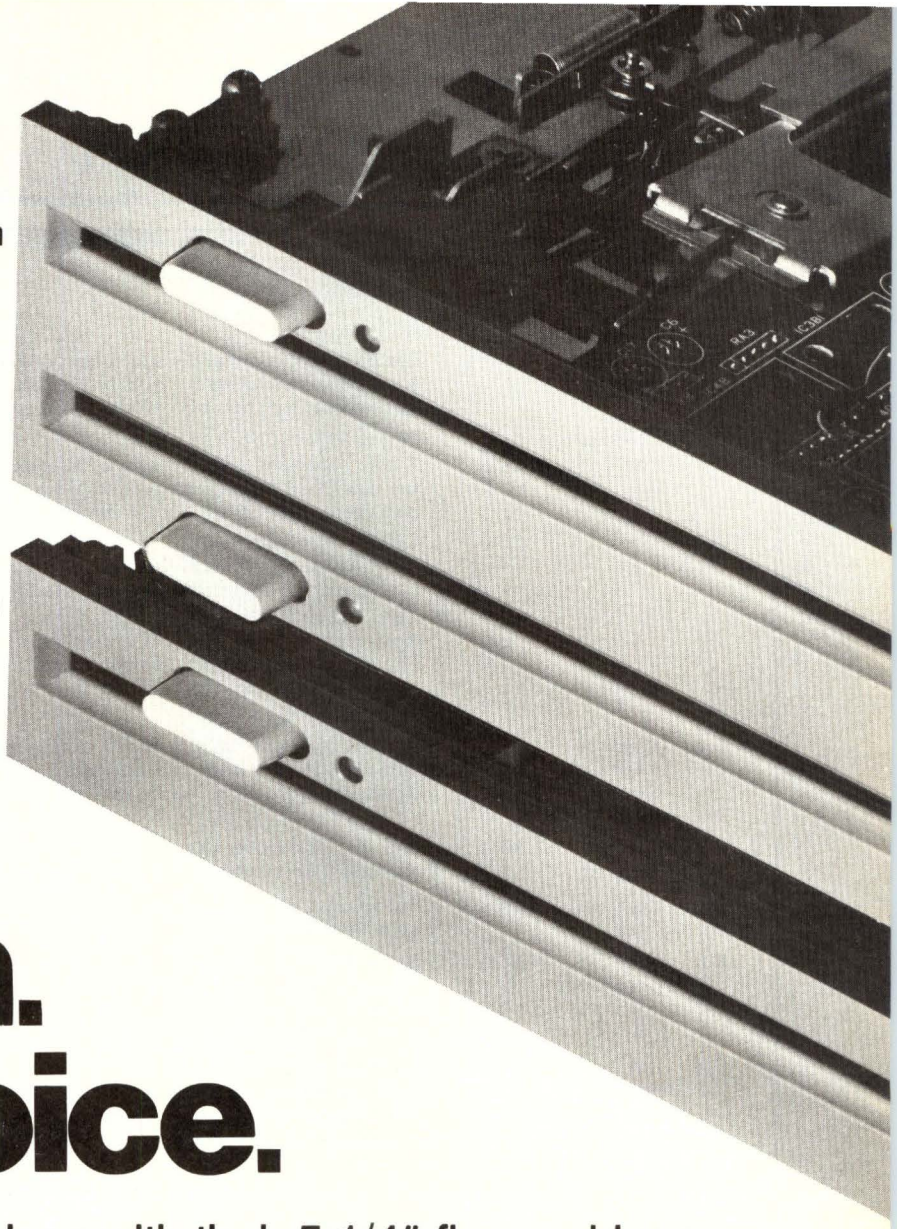
The execution phase is verified by again referring to bit 7 of the status register. After execution, this phase is ended with either a normal or abnormal termination. An abnormal termination results from either a read or write error or a drive status change. A normal termination results from a correctly completed command. Command termination status is determined by reading the appropriate status register bits when directed by an HDC interrupt.

At the end of the execution phase, the HDC enters the result phase. Now the host can read various result parameters from the FIFO. These information bytes are useful for determining the cause of an interrupt and verifying command parameters initially sent with the command. Result-byte handling is a process usually performed at the interrupt level.

## How to handle interrupts

Servicing command-end interrupts from the 7261 is the most important role of any software I/O driver set. At this time, the command's end status is determined. During this service routine, all error detection and correction, error reporting, and controller status information are available.

The flowchart in (Fig 3) shows that most of the interrupt process takes place after the appropriate registers are saved. If a priority interrupt controller chip such as the μPD8259A is in the system, an end of interrupt (EOI) byte is issued to the chip. If the host processor disables interrupts during interrupt servicing (8086/88 microprocessors do this) then interrupts must be enabled to allow their nesting.

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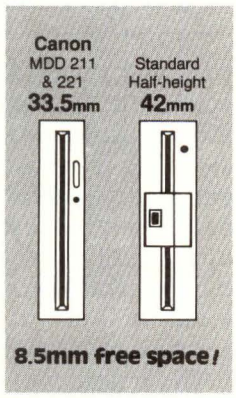


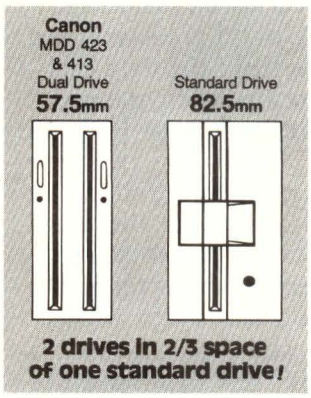


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CIRCLE 57

**TABLE 1**

**Contents of HDC Main Status Register**

| Bit No. | Name | Symbol | Description |
|---|---|---|---|
| D7 | Controller Busy | CB | Set by a disk command issue. Cleared when the command is completed. (This bit is also set by an external reset signal or an RST command, but will be cleared at the completion of the reset function.) When this bit is set, a new disk command will not be accepted. |
| D6<br>D5 | Command End | CEH<br>CEL | CEH = 0 and CEL = 0<br>A disk command is in process, or no disk command is issued after the last reset signal or the last CLCE auxiliary command. Both the CEH and CEL bits are cleared by a disk command, a CLCE auxiliary command, or a reset signal.<br>CEH = 0 and CEL = 1<br>Abnormal termination of a disk command.<br>Execution of a disk command was started, but was not successfully completed.<br>CEH = 1 and CEL = 0<br>Normal termination of a disk command.<br>The execution of a disk command was completed and properly executed.<br>CEH = 1 and CEL = 1<br>Invalid command issue. |
| D4 | Sense Interrupt Status Request | SRQ | When a seek end, an equipment check condition, or a ready signal state change is detected, this bit is set requesting a sense interrupt status command be issued to take the detailed information. This bit is cleared by an issue of that command or by a reset signal. |
| D3 | Reset Request | RRQ | Set when controller has lost control of the format controller (missing address mark, for example). An auxiliary RST command or another disk command will clear this bit. |
| D2 | ID Error | IER | Set when a CRC error is detected in the ID field. An auxiliary RST or another disk command will reset this bit. |
| D1 | Not Coincident | NCI | Set if the controller cannot find a sector on the cylinder which meets the comparison condition during the execution of a scan command. This bit is also set if data from the disk does not coincide with the data from the system during a verify ID or a verify data command. This bit is cleared by a disk command or a reset signal. |
| D0 | Data Request | DRQ | During execution of write ID, verify ID, scan, verify data, or a write data command, this bit is set to request that data be written into the data buffer.<br>During execution of read ID, read diagnostic, or read data command, this bit is set to request that data be read from the data buffer. |

Determining the command termination status requires that the HDC's main status register be read to check for the appropriate bit setting. Table 1 lists the 8 bits of the main status register and their functions. Note that bits D5 and D6 are associated with the command end interrupts.

At this point, the command end bits must be cleared so they can be set by the next command. Further investigation on the cause of an interrupt—whether an error condition or a normal interrupt—can be carried out by reading out a predetermined number of result status bytes from the data register. Table 2 gives a complete listing of the result bytes and the number of bytes that must be read, depending on the command. The status register's condition, together with the result byte, allow the interrupt service routine to determine the exact cause of an error and the action that must be taken.

To determine if a sense interrupt status request is necessary, the SRQ bit in the main status register must be checked. If set, the result byte generated is the interrupt status. Typically, this byte indicates the successful termination of a seek or recalibrate. This allows the next command to be issued to a particular disk drive. Usually, the command is a data transfer such as a read or write data.

Because of HDC processing requirements and the initialization necessary for the completion of a specify command, a special command-end sequence is used. Immediately after the issuing of a specify command, and within the first several polling cycles, up to nine interrupts can be generated. These must be processed by both the host and the 7261. One interrupt is for the command end, and four others establish the present drive status. Setting the SRQ bit can cause up to four additional interrupts, and this requires a sense interrupt status bit to be generated for each drive that is not ready. A certain amount of time is required between each interrupt to allow for 7261 servicing.

*Interfacing to the 7261 is handled on an I/O-port basis to the host processor.*

The amount of delay necessary for the 7261 to catch up on its interrupt servicing depends on the type of host processor used and its clock rate. The

**TABLE 2**
**Command and Result Bytes of the HDC**

| Disk command | Command code | Preset Parameters/Result Status 1st | 2nd | 3rd | 4th | 5th | 6th | 7th | 8th |
|---|---|---|---|---|---|---|---|---|---|
| DETECT ERROR | 0100X | EADH | EADL | EPT1 | EPT2 | EPT3 | | | |
| RECALI-BRATE | 0101[B] | IST* | | | | | | | |
| SEEK | 0110[B] | PCNH<br>IST* | PCNL | | | | | | |
| FORMAT WRITE | 0111(S) | PHN<br>EST | (PSN)<br>SCNT | SCNT | DPAT | GPL1 | [GPL3] | | |
| VERIFY ID | 1000(S) | PHN<br>EST | (PSN)<br>SCNT | SCNT | | | | | |
| READ ID | 1001(S) | PHN<br>EST | (PSN)<br>SCNT | SCNT | | | | | |
| (READ DIAG-NOSTIC) | 1010X | PHN<br>EST | PSN | | | | | | |
| READ DATA | 1011X | PHN<br>EST | (FLAG)<br>PHN | LCNH<br>(FLAG) | LCNL<br>LCNH | LHN<br>LCNL | LSN<br>LHN | SCNT<br>LSN | <br>SCNT |
| CHECK | 1100X | PHN<br>EST | (FLAG)<br>PHN | LCNH<br>(FLAG) | LCNL<br>LCNH | LHN<br>LCNL | LSN<br>LHN | SCNT<br>LSN | <br>SCNT |
| SCAN | 1101X | PHN<br>EST | (FLAG)<br>PHN | LCNH<br>(FLAG) | LCNL<br>LCNH | LHN<br>LCNL | LSN<br>LHN | SCNT<br>LSN | <br>SCNT |
| VERIFY DATA | 1110X | PHN<br>EST | (FLAG)<br>PHN | LCNH<br>(FLAG) | LCNL<br>LCNH | LHN<br>LCNL | LSN<br>LHN | SCNT<br>LSN | <br>SCNT |
| WRITE DATA | 1111X | PHN<br>EST | (FLAG)<br>PHN | LCNH<br>(FLAG) | LCNL<br>LCNH | LHN<br>LCNL | LSN<br>LHN | SCNT<br>LSN | <br>SCNT |
| SENSE INTERRUPT STATUS | 0001X | IST | | | | | | | |
| SPECIFY | 0010X | MODE | DTLH | DTLL | ETN | ESN | GPL2 | [MGPL1]<br>[RWCH] | [RWCL] |
| SENSE UNIT STATUS | 0011X | UST | | | | | | | |

(a)

Definitions

| | |
|---|---|
| EADH | Error Address, High Byte |
| EADL | Error Address, Low Byte |
| EPT1 | Error Pattern, Byte One |
| EPT2 | Error Pattern, Byte Two |
| EPT3 | Error Pattern, Byte Three |
| PCNH | Physical Cylinder Number, High Byte |
| PCNL | Physical Cylinder Number, Low Byte |
| PHN | Physical Head Number |
| PSN | Physical Sector Number |
| SCNT | Sector Count |
| DPAT | Data Pattern |

(b)

Auxiliary Command

| Bit name | Operation |
|---|---|
| CLCE | Clears the CE bits of the status register, inactivating the interrupt request output caused by Command End condition. This is used when no disk commands are going to be issued and it is desired to clear the interrupt. |
| HSRQ | Deactivates the interrupt request output caused by Sense Interrupt Status Request condition until a Command End occurs. However, this command has no effect on the SRQ bit of the status register. |
| CLB | Clears the data buffer. |
| RST | This has the same effect as a reset signal on the Reset input. This function is used whenever the RRQ bit in the status register is set (indicating the format controller is hung up), or when a software reset is needed. |

(c)

**Note:** ( ): These are omitted for soft-sector disks.
[ ]: These are omitted for hard-sector disks.
*: IST available as a result byte only when in nonpolling mode.
B: Indicates buffered mode when set.
S: Indicates skewed mode (SMD only) when set.
X: Indicates don't care.

program (Table 3) shows that an Intel 8086 microprocessor operating at a 5-MHz clock rate imposes a 200-$\mu$s delay between 7261 interrupts. The faster the host executes code, the greater the delay time between interrupts. A 5-MHz 8088 microprocessor, for example, imposes no delay on the 7261 because its execution time is longer than the 8086's interrupt servicing time. In general, there is no significant reduction in performance by inserting delays during interrupt servicing.

**TABLE 3**

**The HDC Interrupt Service Routine**

```
INTRPT:
        PUSH    AX      ;SAVE
        PUSH    BX      ;ALL
        PUSH    CX      ;THE
        PUSH    DX      ;REGS
        PUSH    BP      ;THAT
        PUSH    SI      ;MAY
        PUSH    DI      ;GET
        PUSH    ES      ;KILLED
        PUSH    DS
        CALL    SEND_EOI_TO_8259
        STI     ;ENABLE INTRS FOR S_I_S'S DURING INTRS
        CALL    READ_MAIN STATUS_REPORT_ERRORS_CLEAR_COM_END
        CALL    READ_RESULTS        ;FROM FIFO
        TEST    MAIN_STATUS_STORAGE,10H ;CHK for AN SRQ
        JZ      END_INTR ;IF NO RQS AND SINCE WE HAVE READ FIFI-EXIT
        CALL    ISSUE_SENSE_INTR_STATUS ;IF RQS SET DO A S_I_S
        CALL    CHK_FOR_SEEK_END
END_INTR:
        CALL    WAIT_FOR_HDC_INTERNALS
        MOV     INTR_COMPLETION_FLAG,1 ;SET THE INTR DONE FLAG
        POP     DS      ;RESTORE
        POP     ES      ;REGS
        POP     DI      ;SAVED
        POP     SI
        POP     BP
        POP     DX
        POP     CX
        POP     BX
        POP     AX
        IRET
```

At this point, interrupt servicing in the HDC is complete. The restoration of the CPU registers and a return from interrupt signal indicate the completion of interrupt servicing.

### Initializing the HDC

The specifying or initializing of the 7261 depends largely on hard disk media specifications, interface type, and operating system requirements. An 8-byte parameter set is sent to the HDC with the specifying command. Of these, the most important is the mode byte.

Bit 7 of the mode byte is always a logic 1, while bit 6 selects either CRC or ECC error-correction. Bit 5 determines the generating polynomial for ECC operation. The remaining 5 bits set the head servo's stepping rate.

The typical track formatting arrangement for both hard- and soft-sectored disks is shown in Fig 4. Within the data length high (DTLH) byte, the polling (POL) bit determines whether the 7261 is in polling or nonpolling mode—a logic 0 indicates polling. In polling mode, the ready status of each drive is continually queried and updated. Drives are polled for status information when the 7261 is idle and in between step pulses. A change in the status of any drive is reported immediately through an interrupt—the SRQ bit is set. In the nonpolling mode, the selected drive is first polled and then accessed. Also in this mode, the seek and recalibrate commands have the interrupt status byte available to them as a result byte. Normally, the result byte is available only as a result of a sense interrupt status signal.

The data length low (DTLL) byte together with the lower 4 bits of the DTLH byte constitute a 12-bit value that represents the number of bytes/sector on the disk. For example, if DTLL is 0 and DTLH bit-8 is set high, the number of bytes/sector is 256.

Data transfers to and from the disk must be supported by high speed logic external to the 7261. The most accepted technique is the use of a DMA controller such as the $\mu$PD8237. Data transfer rates for floppy-like interfaces are 1.6 $\mu$s/byte, and 0.9 $\mu$s/byte for SMD interfaces. Conventional NMOS microprocessors cannot handle such high data rates, thus requiring the assistance of a DMA controller or another form of high speed logic.

### A "seek and read" operation

One way to illustrate HDC operation is by reading a data sector from the disk and transferring it to user memory. A read-data operation involves setting up the DMA controller, issuing a seek to a track, and issuing the read-data command.

As shown in Table 3, the 8237 DMA controller is sent a master internal reset initially, and this is followed by the clearing of the mask register. A number of assumptions must be made to describe the read operation, and these may vary if a different type of HDC/DMA hardware implementation is used.

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| ZU-1402 | ISO2 (ABA) |
| ZU-1420 | ISO1/ISO2 |
| ZU-1601E | ISO1 (IATA) |
| ZU-1602E | ISO2 (ABA) |
| ZU-1601 | ISO1 (IATA) |
| ZU-1602 | ISO2 (ABA) |
| **Magnetic Encoders** | |
| ZU-2401 | ISO1 (IATA) |
| ZU-2402 | ISO2 (ABA) |
| **Automatic Magnetic** | |
| ZU-1507 | ISO2 (ABA) |
| ZU-1521 | ISO1 (IATA) |
| **Horizontal Optical Reader** | |
| ZU-XXXHR* | Type II, III |
| **Vertical Optical Reader** | |
| ZU-XXXVR* | Type II, III, IV, V |

*XXX indicates number of bits

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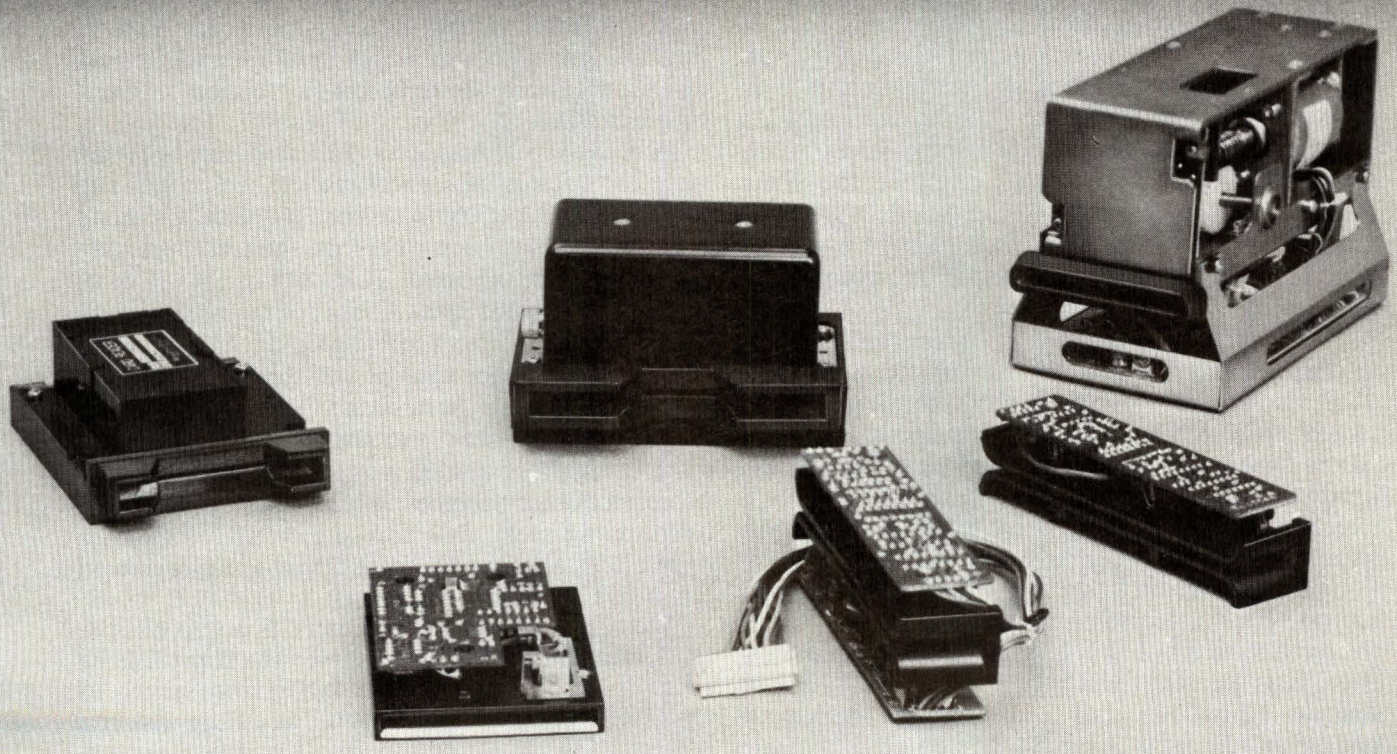

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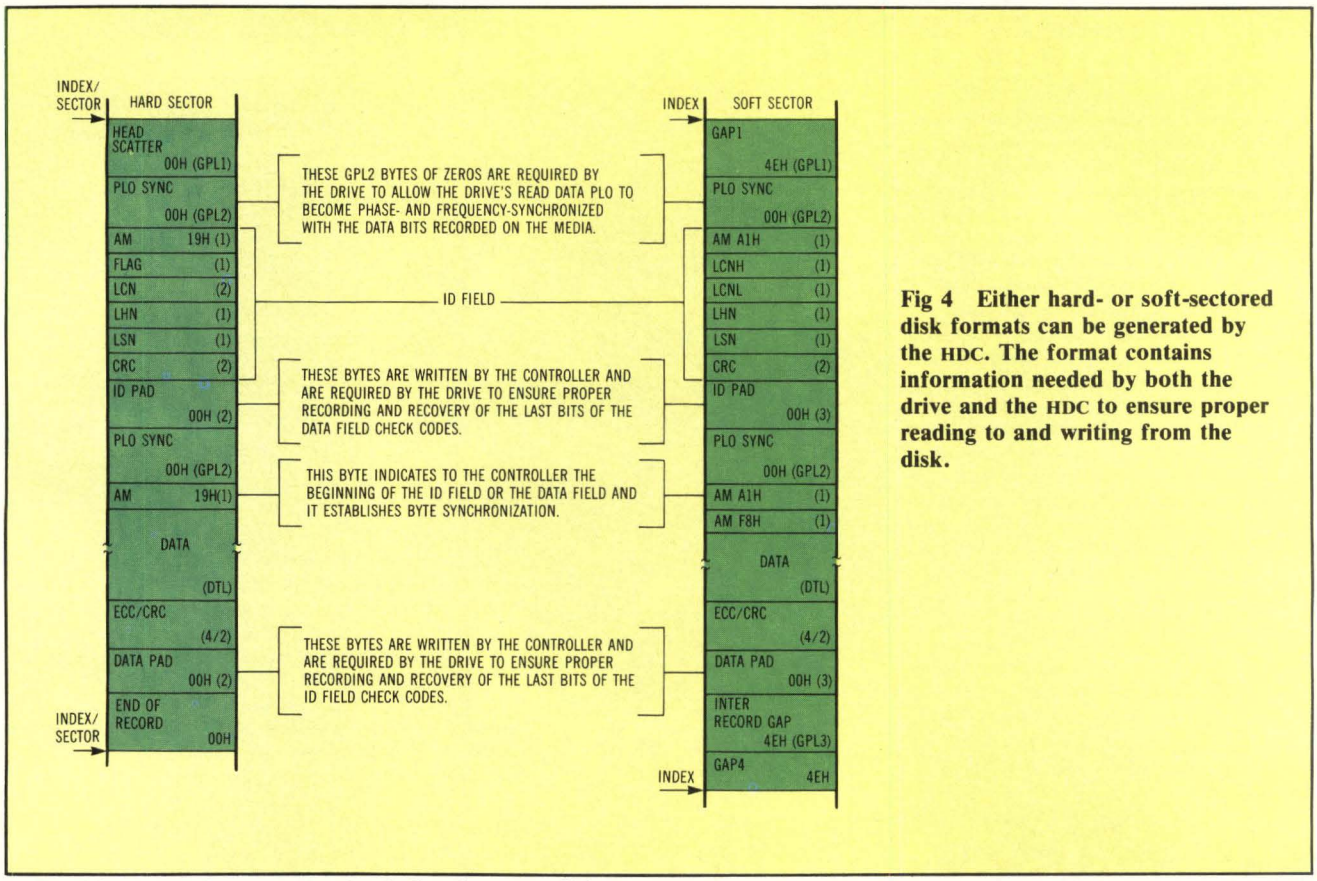


**Fig 4 Either hard- or soft-sectored disk formats can be generated by the HDC. The format contains information needed by both the drive and the HDC to ensure proper reading to and writing from the disk.**

In this example, assume the following conditions: an extended write operation is required, the data acknowledge (DACK) line is active low, data request (DREQ) is active high, the memory-to-memory transfer is disabled, channel-0 hold is disabled and channel 3 of the 8237 will be used. The command byte required is 20 hex. And the channel-3 mask position bit in the all-mask register must be cleared. Next, the channel-3 terminal count is sent to the 8237's channel-3 terminal count register. This is the number of bytes to be transferred minus 1 byte. For this example, the terminal count is actually the number of bytes/sector minus 1.

The channel-3 base address register then receives the base address of the memory to which the disk data will be transferred. Finally, the mode byte is issued to the 8237, and based on channel use and the HDC's characteristics, the mode byte is 07 hex. As hardware handshaking proceeds, the 8237/7261 will transfer data from the disk to the memory location specified by the base address.

Using subroutine HDC_COM, the seek command's parameters are loaded into the 7261's FIFO. Then the command byte is loaded into the command register. Assume that the object is to seek to physical cylinder 1 (track 1). This means that the IOPB must consist of the seek command byte and 2 address bytes for the physical cylinder. The HDC_COM routine requires the address of the IOPB with respect to the present data segment, and the number of bytes required for the command—three in this case.

Once the command and its parameters are loaded in the HDC, the required number of step pulses and their direction are issued to bring the head to the specified track. When the head arrives at track 1, the HDC sends out a seek-end interrupt and the host will service this as described in the section on interrupt handling.

Now the actual read-data command can be issued since the DMA is initialized and the seek command is complete. HDC_COM loads the FIFO with command parameters describing where on the track the data to be accessed is located. Then HDC_COM will issue the read-command byte. A return to the calling routine occurs only after a software handshake between the interrupt service routine and the interrupt completion flag. This handshake, together with the seek issued and seek end flags prevents the HDC from being programmed while a seek is in progress. More elaborate schemes can be used for multiple overlapping seeks, but for single-disk, single-user operations, the use of these flags is the preferred technique.

When the read-data command is accepted, the HDC immediately begins to survey the track for the specific sector address or ID bytes from which to read data. If after two revolutions of the disk the correct ID is not found, an error condition occurs, followed by an interrupt to the host. If the correct sector is found, data begins to flow into the FIFO and DMA transfers take over the data transfer operation. Data transfers then continue until the read

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*Data transfers to and from the disk must be supported by high speed logic external to the 7261.*

operation is terminated by a terminal count interrupt from the DMA controller, or until an error condition occurs as indicated by the error status byte. If no errors occur, disk data has been transferred via the DMA controller to the user's memory.

### Simplifying system integration

The overwhelming majority of commands issued to the HDC in a system environment are read data, write data, and seek. Thus, in a single-user system, the HDC/DMA read/write data buffer can occupy one location in memory. If the same buffer serves both to read from and write to the disk, the only difference between a read-data and write-data command is the DMA transfer's direction. This is controlled by the direction bit in the mode register, and the read/write data command at the top of the IOPB. This assumes that a seek to a specified track is not necessary.

Obviously, the HDC must be able to access any track and sector on a disk. This can be accomplished by embedding all seeks to tracks in a common read/write routine. From a system standpoint, the only variables subject to change on a disk access—read or write data—are the head number, track number, starting sector and the number of sectors to be accessed sequentially.

From these variables, a call to a Common_Read_Write_Module establishes a specific IOPB based on the specified parameters. The DMA terminal count and direction of data transfer—read or write—are established as passed parameters for setting up the DMA controller. The track to be accessed is used as the parameter to be passed to an embedded seek to track. This seek is transparent to the user. The user's IOPB is then copied to the_HDC COM's IOPB location and the HDC_COM loads the seven read or write data command parameters and the command byte into the HDC.

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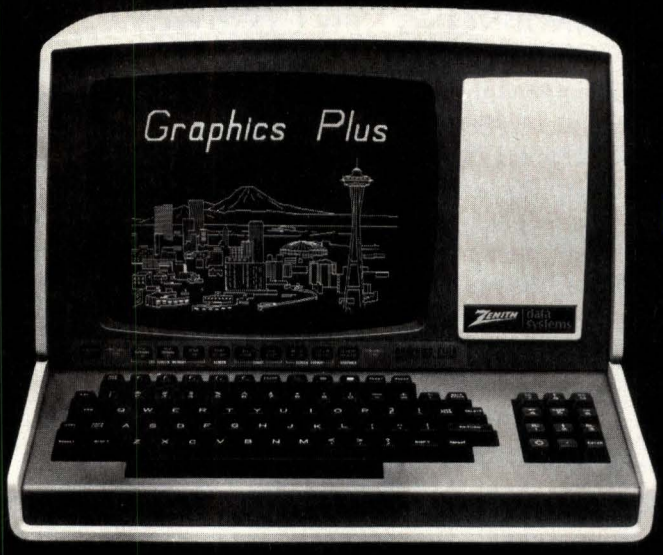


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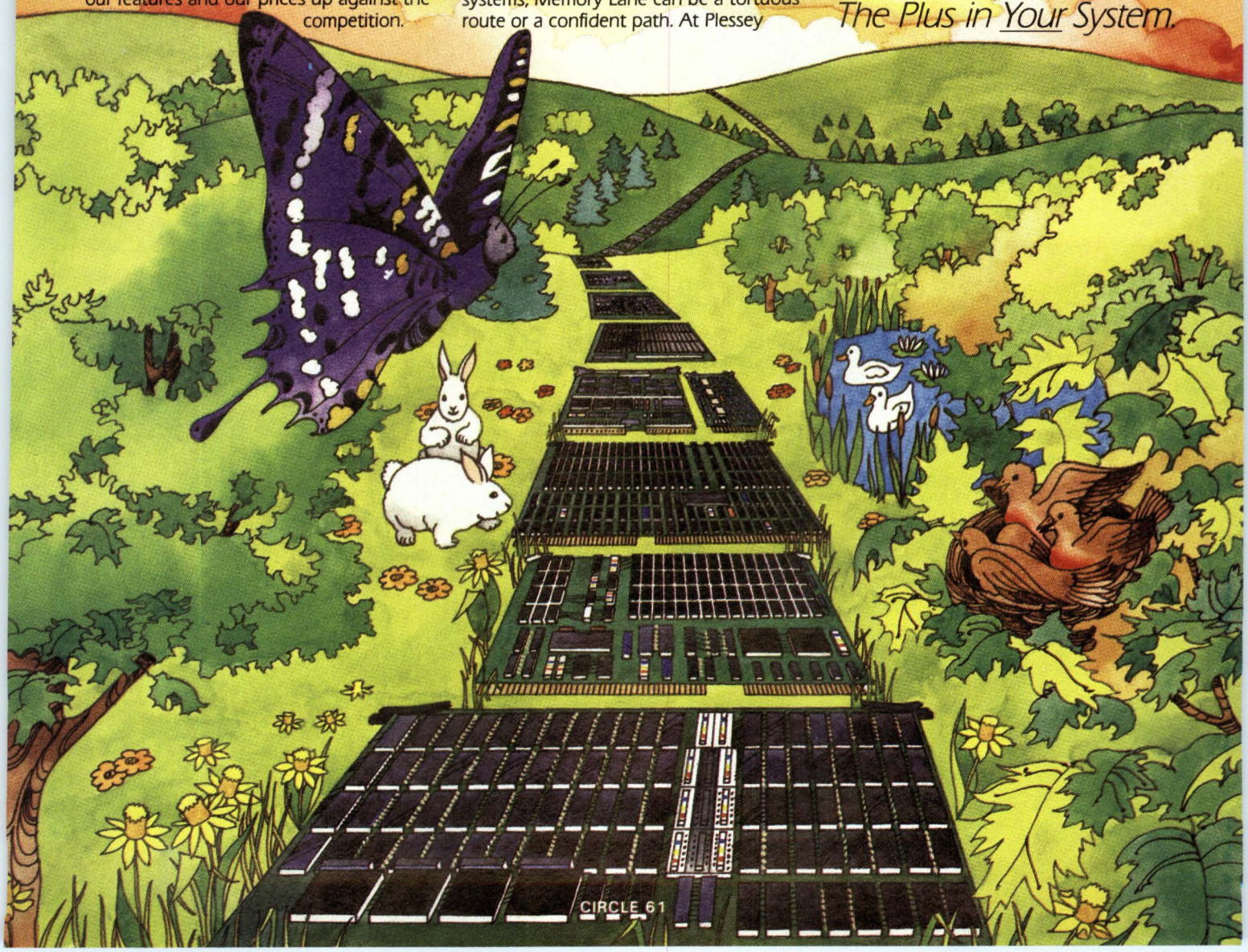

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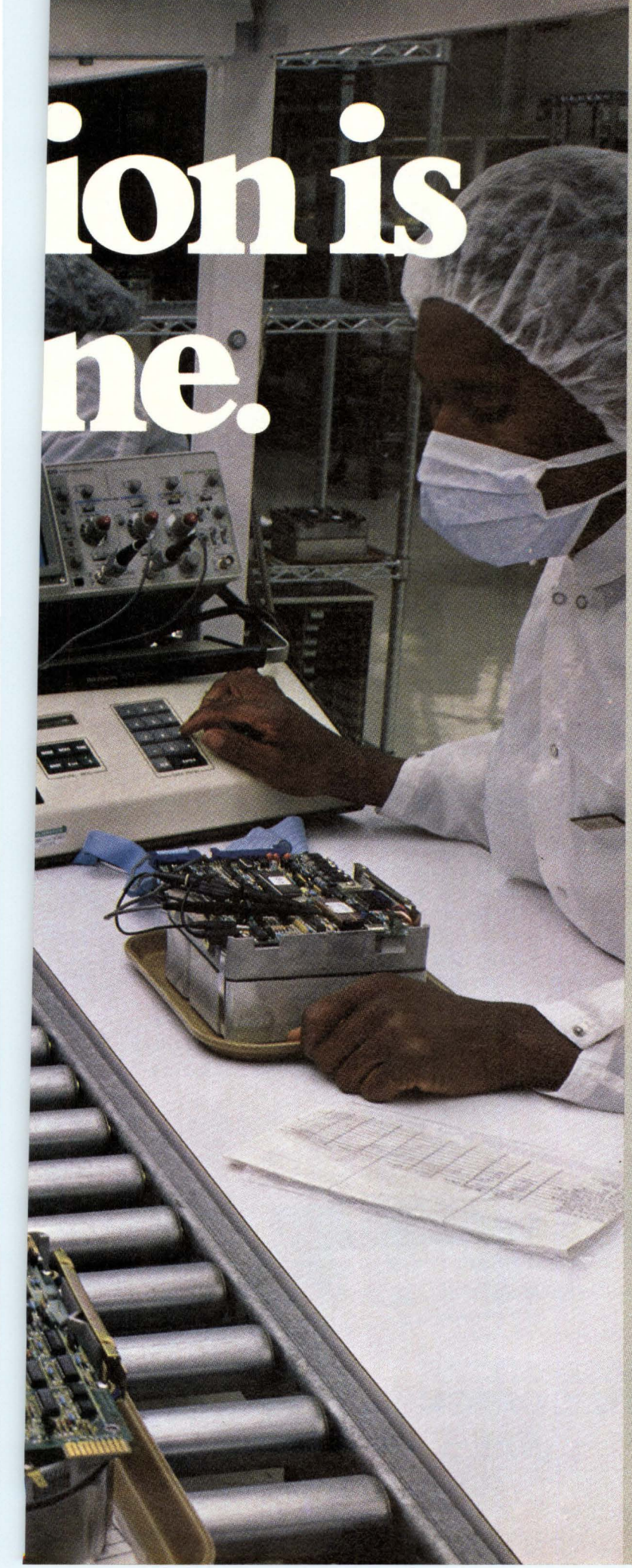

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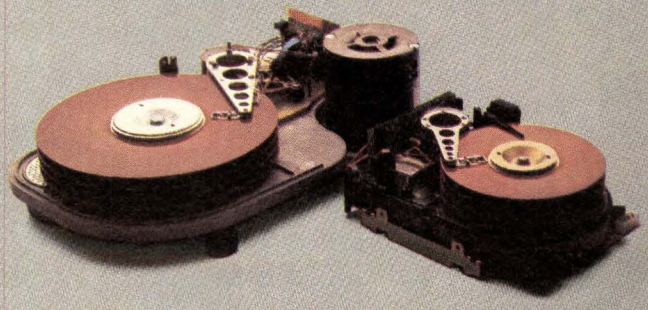

CIRCLE 62

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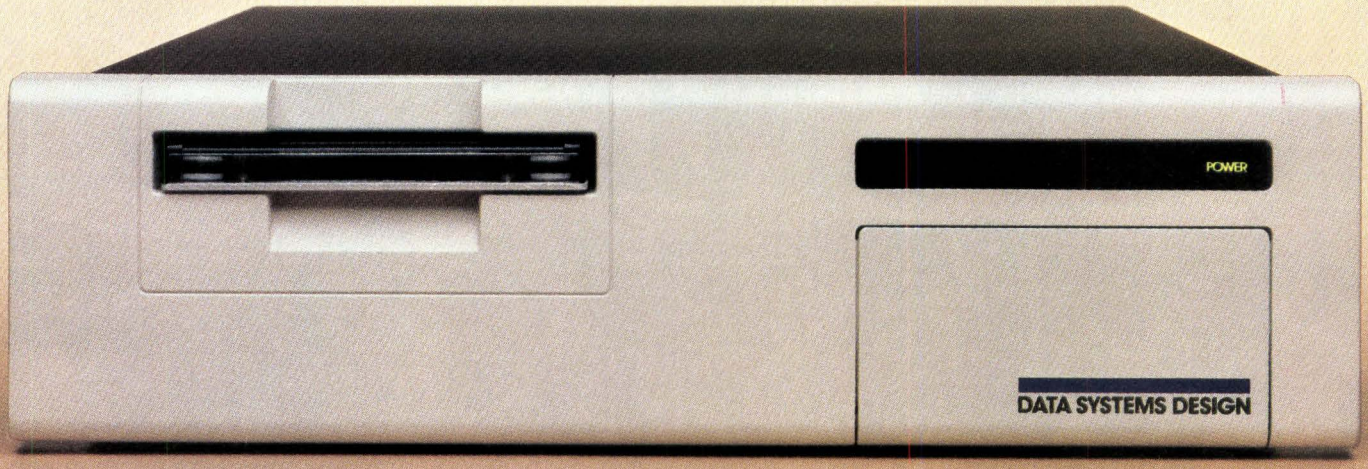


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CIRCLE 63

# A SECOND LOOK AT COMPUTER PIRACY

## The case of Apple versus Franklin may give copyright protection to software, but the guidelines are not clear. The decision can be better understood in the context of a cultural collision between the technical and legal professions.

by Estella S. Gold

*The appeals court decision—Apple versus Franklin—has received a lot of press coverage. Unfortunately, some of it was too superficial to be helpful. The editors of* Computer Design *feel that software protection is important enough to our readers for us to depart from our usual format. Therefore, we are running this in-depth article on the significance of the Apple decision.*

On Aug 30, 1983, the United States Court of Appeals for the Third Circuit handed down a definitive decision that computer software, even in object code or ROM form, may be afforded copyright protection. This ruling reversed the trial court's denial of Apple Computer Inc's application for a preliminary injunction against Franklin Computer Corp (for simplicity called *Apple I*). The news shook the computer industry and its lawyers, offering legal remedies against piracy. As the court openly admitted, this was a case of "first impression." Franklin is now appealing.

Based upon this appellate decision (for simplicity called *Apple II*), the computer industry and the news media may rightfully expect that their legal counsel can now establish clear guidelines on how to adequately protect their products. Not so.

### What the courts did not decide

On May 12, 1982, Apple sued Franklin for copyright infringement, patent infringement, unfair competition, and misappropriation due to Franklin's manufacture and marketing of the Ace 100. Fourteen operating system programs are at issue, among them Applesoft and DOS 3.3. Apple's procedures in filing these programs with the U.S. Copyright Office were inconsistent—some were submitted in source-code form, some in object-code form, some on diskette, and some on ROMs. Franklin defended, asking the court to determine that each of the copyrights claimed is invalid, and counterclaiming that Apple attempted to monopolize its technology in violation of antitrust laws.

The *Apple I* case is limited to Apple's request for a preliminary injunction against Franklin. On Aug 2, 1982, Judge Clarence C. Newcomer in the District Court, for the Eastern District of Pennsylvania denied Apple's preliminary injunction request. *Apple II* is the appeal from that denial. *Apple II*, like *Apple I*, does not address patent infringement, unfair competition, misappropriation, or Franklin's antitrust claim. The focus of *Apple II* is the correctness of the district court's denial of the preliminary injunction. The reversal decision remanded the case to the lower court for further decision on the validity of Apple's procedure in obtaining the copyrights.

A preliminary injunction, commonly referred to as a temporary restraining order or TRO, is the court order requiring the supposedly offending party to stop the objectionable activity until an actual trial on the issue. Failure to obey could result in contempt.

The court's decision is usually made well in advance of the trial and the amount of evidence available upon which the judge bases a decision is often limited. Under these circumstances, parties to the lawsuit applying for the injunction must show the court that they have a reasonable probability of success at trial and that, without the injunction, they would suffer irreparable harm. The standards for granting preliminary injunction

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are intentionally high in an effort to be fair to the party whose freedom will be restricted until the day of trial. For example, in a dispute over ownership of land, a preliminary injunction to stop the cutting of trees until the trial date would be a typical scenario.

### Franklin admitted copying

Apple applied to the court for a preliminary injunction to restrain Franklin from using, copying, selling, or infringing upon Apple's copyrights on 14 programs. Apple presented evidence that the Ace 100 programs were virtually identical to the Apple programs except for the deletion of the Apple name and its copyright notice. In one program, the word "Applesoft" and the programmer's name still were embedded in the Franklin code. (One cannot help but marvel at how human foibles become valuable evidence at trials.)

Franklin witnesses testified that they had studied the feasibility of independently developing the programs and decided that the attempt was impractical. Franklin employees openly admitted copying. They outlined the technical difficulties of interfacing with the Apple software, which had a multitude of entry points. The court did not address this last testimony, and one cannot help but suspect that possibly only the programmers present understood the problem Franklin raised.

Given Franklin's admitted copying, the company's only defense to Apple's probable success at trial would be that the programs were not "copyrightable," or failed to meet the requirements of registration. For unexplained reasons, the *Apple I* court focused its discussions almost exclusively on the copyright of the software on ROMs, ignoring the source-code and object-code submissions.

Without question, based upon earlier cases, source code could be copyrighted. However, object code has been treated with some hesitation. When submitted to the U.S. Copyright Office in object form, the applicant receives a "letter of doubt" which reads in part:

> "The Copyright Office generally requires the best representation of the authorship for which copyright is being claimed. Because copyright examiners are not skilled computer programmers, they have extreme difficulty in examining computer programs in other than source code format to determine whether the deposit contains copyrightable authorship. Deposit copies of works registered for copyright are available only for inspection in the Copyright Office by members of the public and may not be 'copied.'
>
> . . . Where however, the applicant is unable or unwilling to deposit a printout in source format, we will proceed with registration under our 'rule of doubt' upon receipt of a letter from the applicant assuring us that the work as deposited contains copyrightable authorship."

This letter of doubt is not a refusal of copyright status. Although the letter would appear to be a refusal of enforceable copyright status, it actually leaves the applicant in limbo. The applicant may provide the requested letter of assurance but never know if those rights are enforceable until the applicant sues an infringer and receives a favorable court decision.

The programs on the ROM presented the most difficult problems to both the *Apple I and II* courts because the ROM is a physical device. Prior court decisions determined that videogame ROMs were copyrightable. Franklin argued that the Apple ROMs produced no humanly readable product and that the ROM chips are part of the electromechanical process of the computer. Such processes can sometimes be patented, but heretofore not copyrighted. The *Apple I* case did not decide that ROMs could not be copyrighted—the court simply expressed "doubt" regarding ROMs. Since Apple had to prove "likelihood of success at trial" to be awarded the preliminary injunction, the court's "doubt" meant certain defeat.

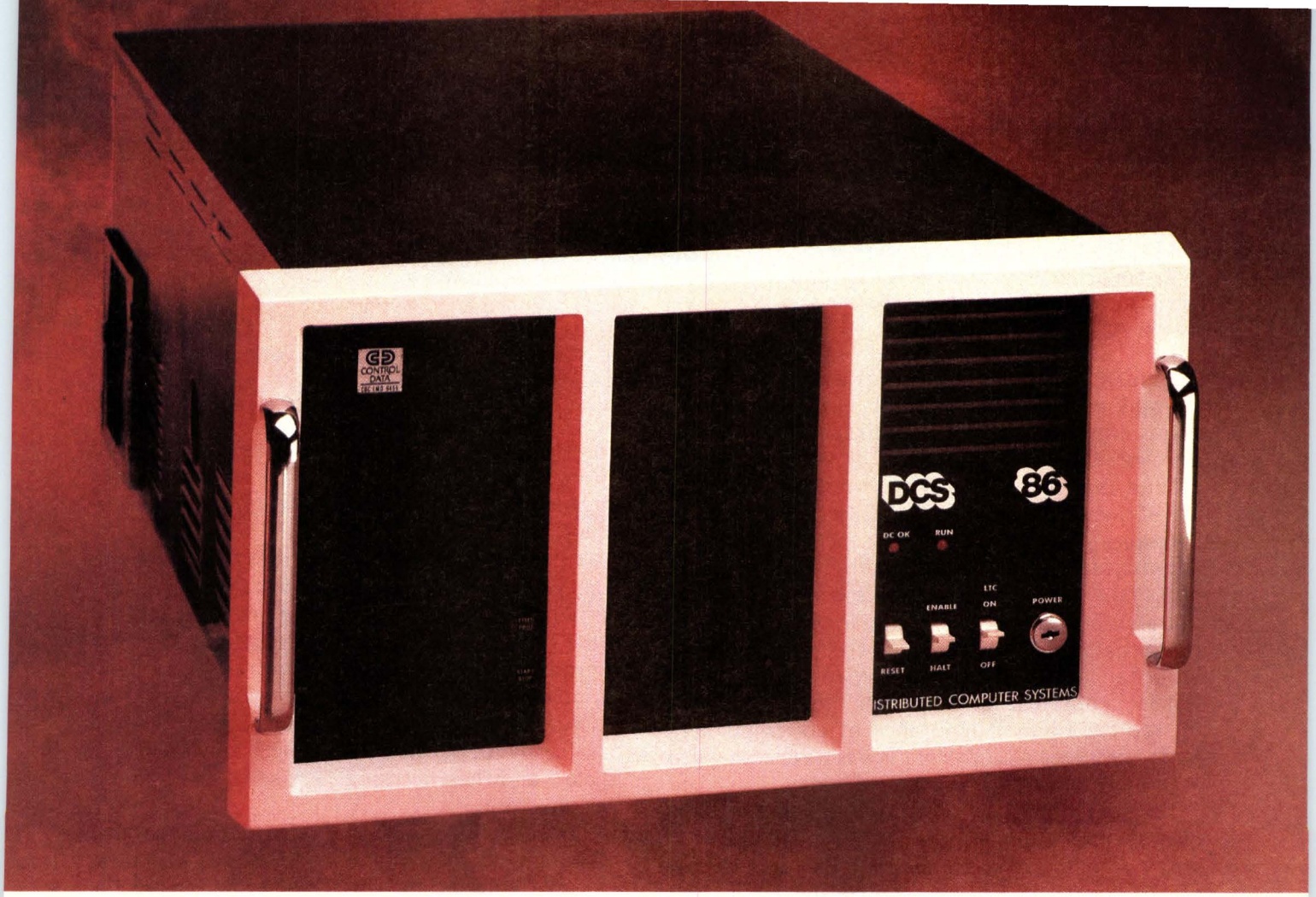
*"The first thing we do, let's kill all the lawyers"*—King Henry VI

### The communication barrier

Anyone reading the testimony, briefs of counsel, and court opinion cannot help but conclude that at last the lawyers have met their match when confronted with EDP's love of technical terms and jargon. But my comparison is an unfair one. Both lawyers and litigants know that "real time," "interface," and "software" are technical terms. Yet, how many of the EDP witnesses know that "expression," "concept," and "ideas" are technical terms of such difficulty in copyright law that even in current opinions, judges spend pages of explanation on each point?

The lawyer's use of ordinary language as "terms of art" may remind many frustrated clients and witnesses of a line from Shakespeare's *King Henry VI:* "The first thing we do, let's kill all the lawyers." For example, in *Apple I,* there was testimony from Apple's systems programmer describing an operating system that manages files: "It is a general sort of concept that many applications may require." In its brief, Franklin argued that "concepts" under Section 102(b) of the copyright law are excluded from protection. Section 102(b) reads as follows:

> "In no case does copyright protection for an original work of authorship extend to any *idea*, procedure, process, system, method of operation, *concept*, principle or discovery . . ." (emphasis supplied).

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The court in *Apple II* then recognized and addressed the problem:

"The witnesses undoubtedly had the not uncommon difficulty of finding the precisely correct words of description in this field. It would be both unreasonable and arbitrary to consider the statements of non-lawyer witnesses without experience in using the statutory language as words of art to be binding admissions against Apple."

Obviously, the programmer was using English.

Franklin now appeals on this point (only one of many arguments Franklin makes): "[The court] dismisses the testimony of Apple witnesses on the ground that the witnesses were not trained in the use of the technical language of Section 102(b). But how does [the court] know that fact? [the fact that the programmer was using English rather than statutory language] It is not in the record." Following this argument to its extreme and logical conclusion, this programmer, in order to competently testify on behalf of Apple, would have to pass a literacy test in "copyright language" or otherwise profess on the record total ignorance of copyright laws. Such ignorance of copyright law is rare among programmers and EDP management today.

Franklin's counsel cannot be faulted for acting like lawyers. Simply put, the appellate court in *Apple II* may reverse the earlier ruling only because of errors of law, and not change the facts as the *Apple I* court found them. The programmer's use of the English word "concept" as compared with the word "concept" in copyright language is a question of fact and not subject matter for the appeal. This issue was but a minor point in the reversal of *Apple I*, but it illustrates communication difficulties between the EDP and legal communities.

### What the Apple II court did decide

In reversing, the *Apple II* court makes absolutely clear that all forms of program expression in issue—source code, object code, and programs embedded in ROMs—are within the protection of the copyright laws. In addition, *Apple II* specifically decides that operating system programs are entitled to the same status as application programs for copyright protection.

The *Apple II* court found sufficient reason to rule that Apple had the requisite probability of success to satisfy that first criterion for the preliminary injunction. But what of the second—irreparable harm? The *Apple I* court addressed the question with but two sentences:

"It is also clear that Apple is better suited to withstand whatever injury it might sustain during litigation than is Franklin to withstand the effects of a preliminary injunction. While I am not prepared to find that the injunction sought by Apple would force Franklin out of business, it would certainly have a devastating effect."

This was the *Apple II* court's response:

"Nor can we accept the district court's explanation which stressed the 'devastating effect' of a preliminary injunction on Franklin's business. If that were the correct standard, then a knowing infringer would be permitted to construct its business around its infringement, a result we cannot condone . . . (citations omitted) the size of the infringer should not be determinative of the copyright holder's ability to get prompt judicial redress."

These "moral" considerations aside, the *Apple II* court also ruled that a fair showing of copyright infringement carries with it a presumption of irreparable harm.

As the fictional Mr Dooley said, "An appeal is when ye ask wan court to show its contempt for another court." One cannot help but wonder if the *Apple II* court's outrage over the admitted piracy of programs costing over $740,000 to develop, in conjunction with the trial judge's sympathy for the underdog, has caused the court to decide more than the issues before it. Such decisions are called "dicta" and then need not necessarily be followed in future cases.

If the *Apple II* court has ruled definitively that software in source-, object- and ROM-storage forms are copyrightable, then why did they remand the case to the district court for a decision on Apple's application for a preliminary injunction on the Copyright Office's rule of doubt? After *Apple II*, the rule of doubt should no longer exist. The appellate court has decided object code is copyrightable and such a decision is binding. Sending the case back to the lower court on the rule of doubt causes confusion because the rule of doubt is based on the idea that object code may or may not be copyrightable. With this ambiguity, it is likely that the *Apple II* decision, hailed by the industry, will be before future courts for interpretation. Apple faces other issues on remand to the district court, such as proper notice and misuse of the copyright, which must be overcome before a preliminary injunction will be issued.

### Antipiracy solutions

Will Rogers once said, "The minute you read something you can't understand, you can almost be sure it was drawn up by a lawyer." As a lawyer, I am commonly faced with the difficulty of explaining what is copyrightable material. "Expression" is protectable. "Ideas," "concepts," and "methods" are not. The explanations inevitably leave clients confused and lawyers must often use analogies, (often humorous) in an effort to explain. For example, the idea of a chocolate cake is not protected. People who follow recipes are not

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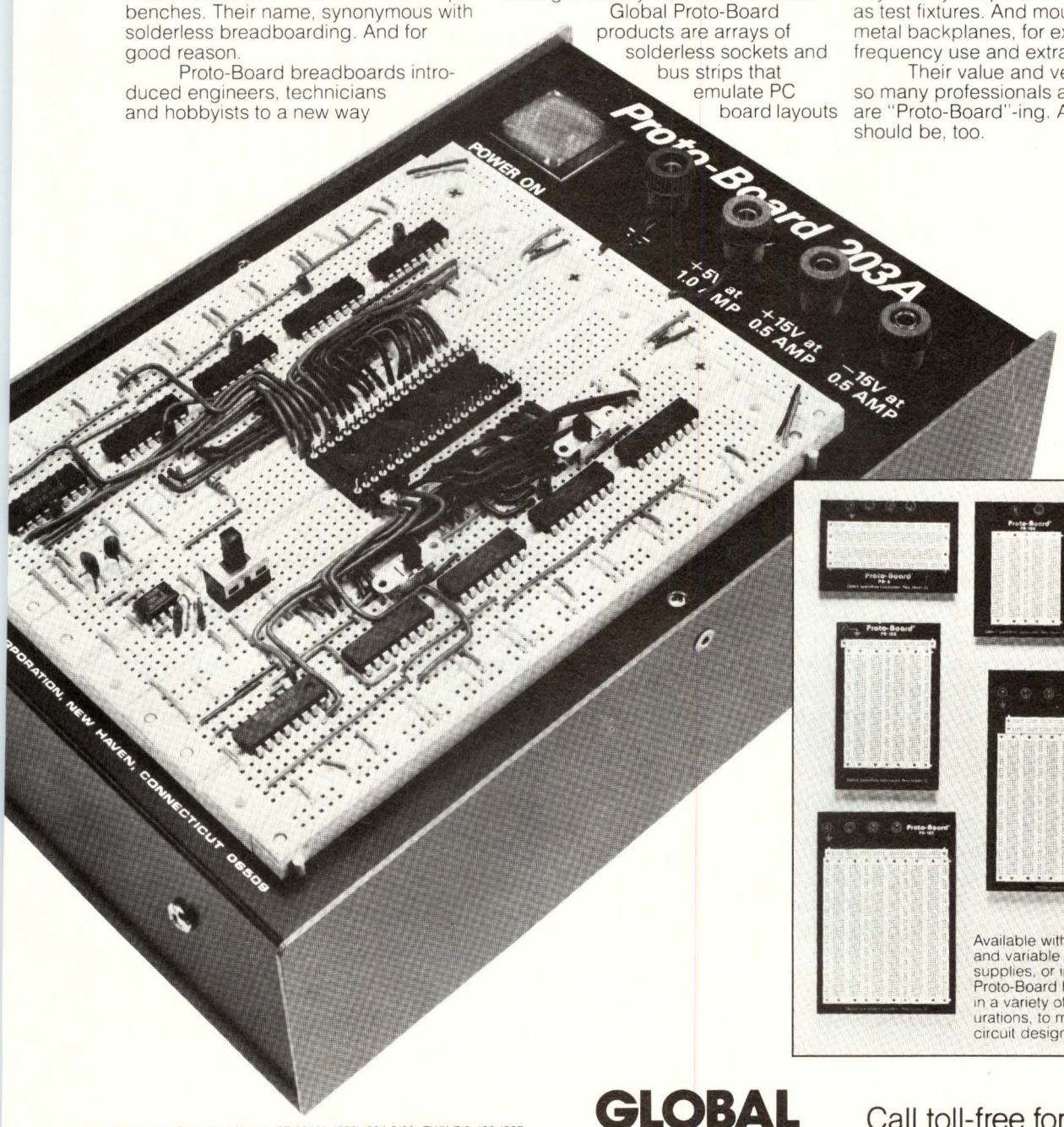


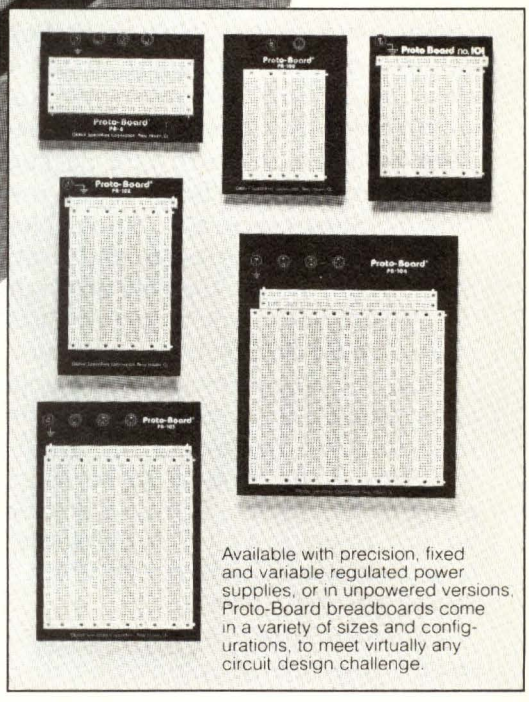

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infringers. They may even sell the resulting cake without obligation to the recipe writer. But, they may not copy or sell the recipe.

These simple explanations assist the public in understanding copyright protection. Nevertheless, the difficulty remains in fitting the expanding complexity of computer technology into the restrictive girdle of an existing legal framework.

Copyright offers many advantages. It is easy and inexpensive to obtain—only requiring notice of copyright and registration with the U.S. Copyright Office. Once obtained, the copyright holder has exclusive rights to the work including enhancements and corrections incorporated in new versions of the software. Copyright duration is remarkable: the author's life plus 50 years, or, if the program is a "work made for hire," 75 years from first publication or 100 years from creation, whichever is shorter.

The copyright law is grounded in the U.S. Constitution and will be enforced nationwide against infringers. An infringement suit requires registration with the U.S. Copyright Office. Therefore, a "letter of doubt" on registration becomes critical in an infringement suit. If the copyright holder is successful in an infringement suit, recovery may include money damages for lost profits, counsel fees, court orders to prevent the making of additional copies, and court orders to seize and destroy illegal copies.

Detection of infringers is a problem plaguing the computer industry. On this issue the law provides no assistance. Copyright notices embedded in coding, and devices such as useless entry points deliberately inserted, assist in the courtroom to show intentional infringement. Rapid advances throughout the industry in the development of both hardware and software packages to prevent copying or to make illegal copies useless may provide the most practical solution. Nevertheless, the enormous cost of software and firmware development, as opposed to the high profitability of the industry, provides tremendous financial incentive to pirates intent on breaking codes and protections.

Since the processing time for patent protection is approximately three years, it is not worth addressing this protective method in any detail for software. Not only is the product to be patented probably going to be obsolete before protected, but patents do not tolerate with flexibility the constant enhancements and updates for which the computer industry is well known.

Although little has been written about trade secret protection in comparison to copyright and patents, it is probably the most widely used legal protection for software. When firms opt for trade secret protection, they take a course very different from that of the copyright applicant. Both patent and copyright laws are premised upon public disclosure, requiring registration in Washington. The theory is that publication of a new development will provide the foundation for further advances in the industry. Until the *Apple II* case, the administrative copyright office and courts have opposed the deposit of coding that cannot be readily deciphered.

### Enforcing trade secret protection

In contrast to copyrights and patents, the essential element in trade secret protection is secrecy. Legal secrecy in mass marketed software is hard to achieve, requiring aggressive procedures and assistance of counsel. Affirmative steps must be taken both in-house and in distribution to prevent dissemination of software contents. Contracts and marketing procedures must be planned carefully to maintain trade secret status, such as the use of licensing rather than sales agreements. A sale may be considered a loss of ownership rights that leaves the originator with no claim of secrecy. Consultation with legal counsel is essential to establish the appropriate steps to take. Other possible steps include prohibitions on copying for other than backup purposes with the customer, nondisclosure agreements, limitation of use to a single CPU, and restrictions on processing of third party data.

The deposit of object code and ROMs (by nature indecipherable to layman and lawyer) is an attempt to preserve both copyright protection and trade secret protection simultaneously. The courts have not yet fully resolved whether such deposit destroys trade secret status.

Legal enforcement will depend upon detection and the effort expended by the software producer in adequately following the legal guidelines. Legal remedies for trade secret infringement vary from state to state, unlike the copyright and patent laws.

In conclusion, it is apparent that the legal system is slowly addressing the problems raised by a new technology. The court decision of *Apple II* has brought to the computer industry new hope of legal protection against piracy.

The growth of computer literacy among the public will surely filter upward from schoolchildren to lawyers and judges. However, the ability of the legal system to explain in simple terms the laws of copyright, patent, and trade secret to the public is sorely lacking. Surely the English/copyright language problem for witnesses in *Apple I* and *II* will recur. Nevertheless, the first steps have now been taken to ensure that the innovators in the computer industry will more adequately profit by their endeavors.

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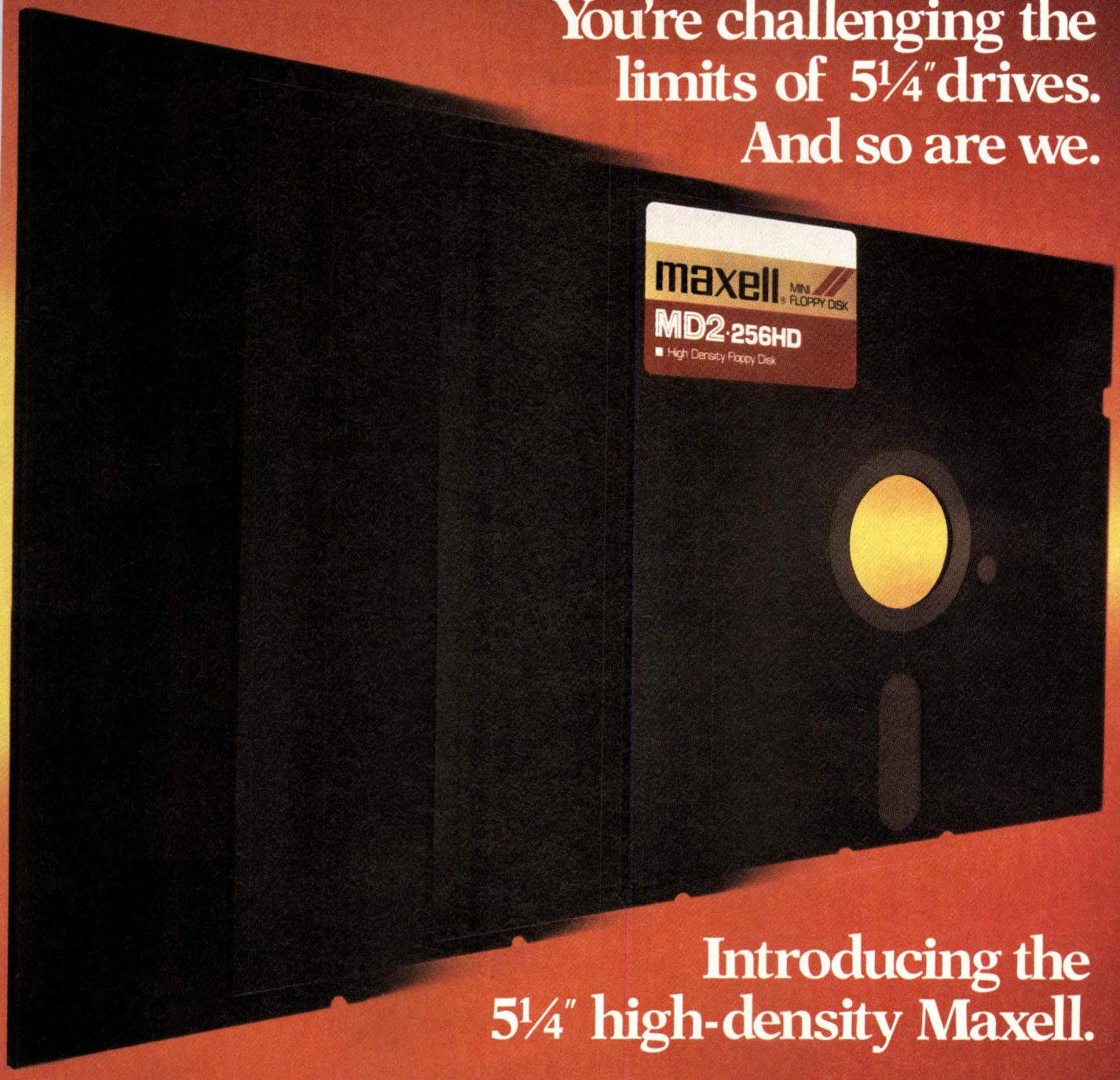


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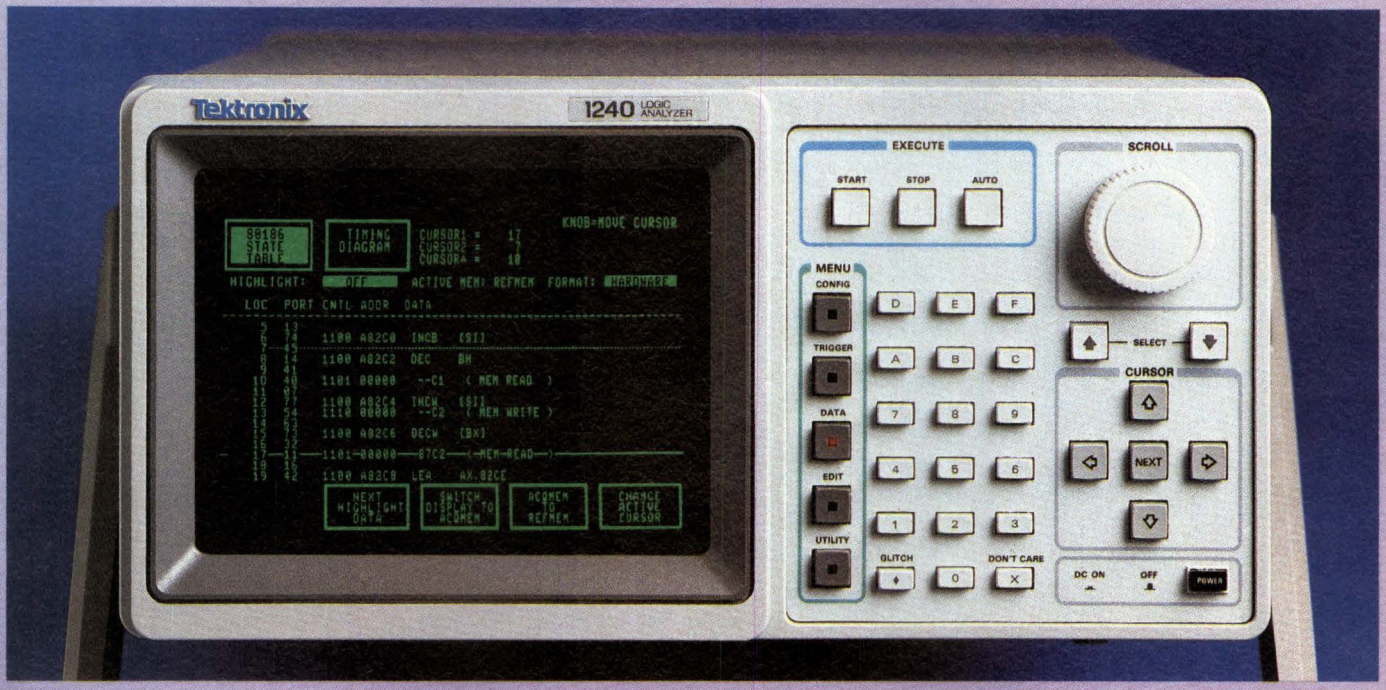


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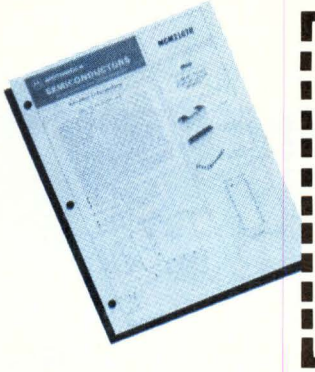
| 2K x 8 | 45,55,70<br>45,55,70<br>45,55,70 | MCM2016HY<br>MCM2016HL<br>MCM2016HP | 300 Mil Ceramic DIP<br>600 Mil Ceramic DIP<br>600 Mil Plastic DIP | 120 mA<br>120 mA<br>120 mA | 20 mA<br>20 mA<br>20 mA | HMOS<br>HMOS<br>HMOS |
| 2K x 8 | 120,150,200<br>120,150,200 | MCM6116P<br>MCM61L16P | 600 Mil Plastic DIP<br>600 Mil Plastic DIP | 55 mA<br>55 mA | 2000 uA<br>100 uA | CMOS<br>CMOS |
| 4K x 1 | 55,70<br>55,70 | MCM6147P<br>MCM61L47P | 300 Mil Plastic DIP<br>300 Mil Plastic DIP | 35 mA<br>35 mA | 800 uA<br>100 uA | CMOS<br>CMOS |



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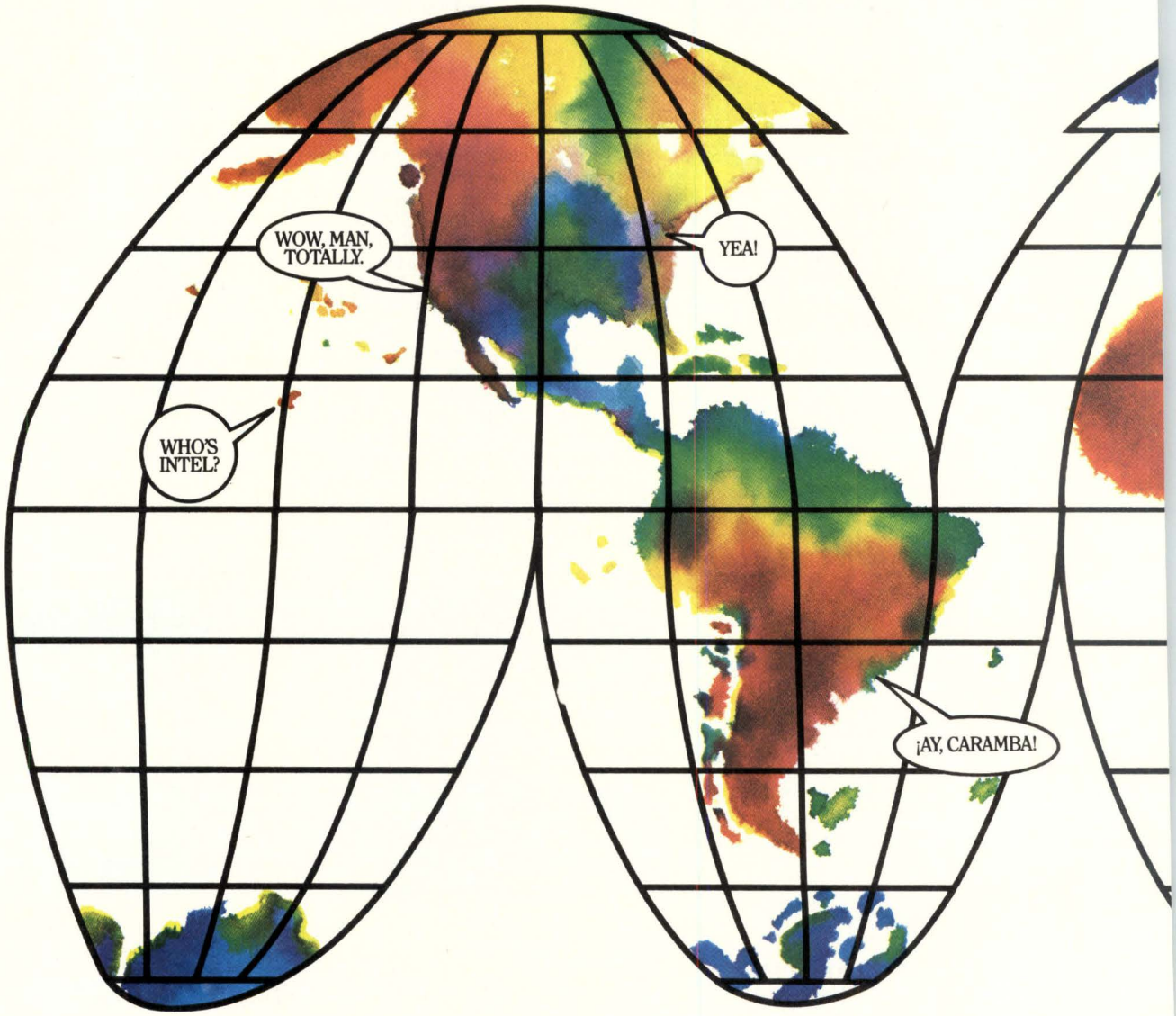


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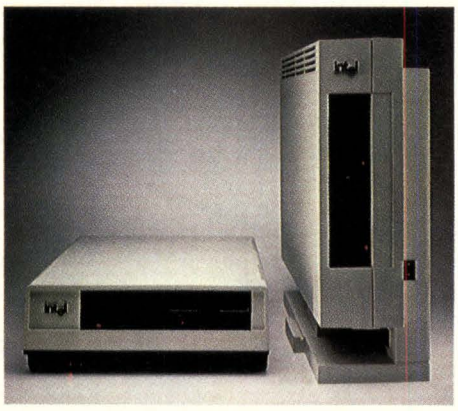

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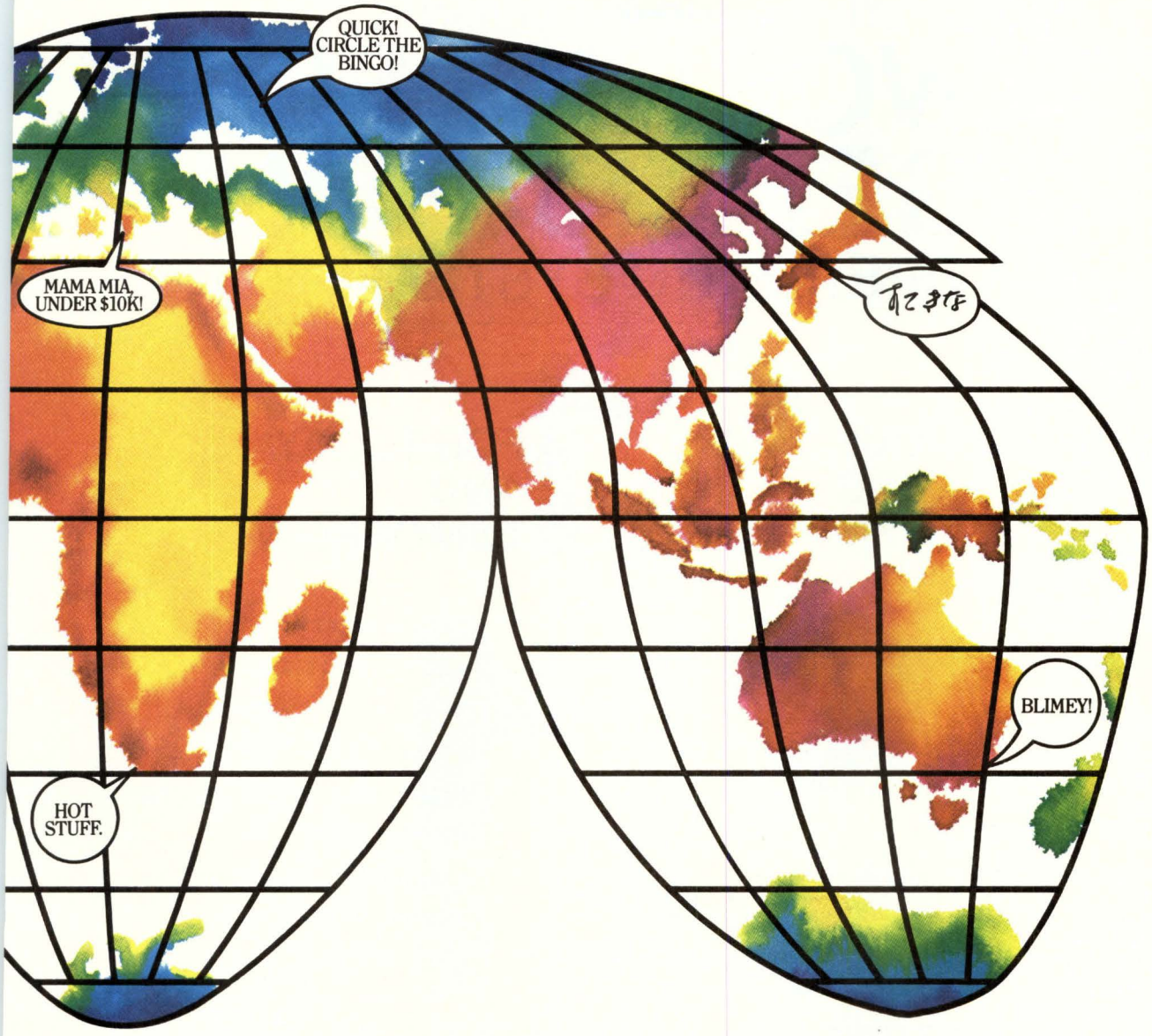


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# LANGUAGE-BASED ARCHITECTURE EASES SYSTEM DESIGN—III

**Occam channels are implemented on a multiprocessor Z80 system, using the only computer language designed for multiple processors and true parallel processing.**

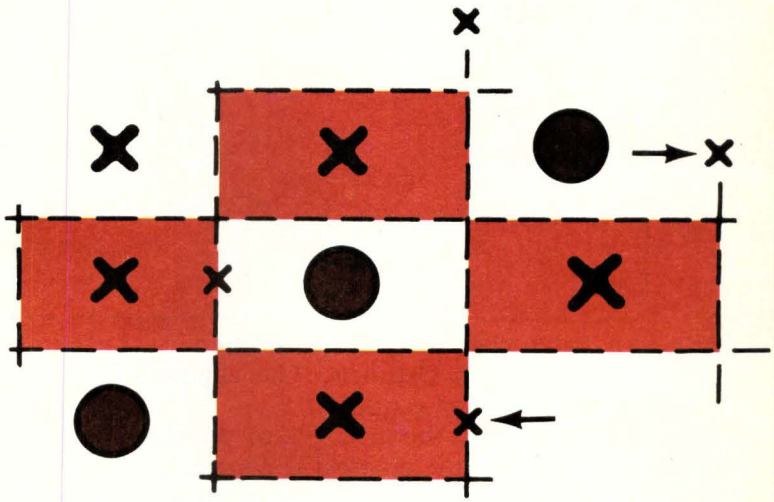
**by B. Jane Curry**

*This is the third in a series of articles on the Occam language. (See* Computer Design, *Nov 1983, pp 107-115 for Part I, and Dec 1983, pp 109-120 for Part II.)*

Occam was designed to provide a simple solution to concurrent processing problems. The language provides sequential and parallel constructs directly, thus removing the need for software to sequentially handle parallelism. Although Occam can be run on a single processor, with concurrency managed by calls to a multitasking runtime system, the obvious use for the language is in a multiprocessor environment where true concurrency can be shared between several processing elements. Occam embraces concepts in programming beyond conventional languages. Moreover, its instruction set is very small, compact, and system oriented.

An Occam program consists of one or more processes joined by constructors. There are three basic types of Occam constructors: sequential (SEQ), where program elements are executed in sequence; parallel (PAR), where program elements are executed in parallel; and alternative (ALT), in which one program element is selected from a set. The conventional 'WHILE' statement achieves repetitive execution of a process. Communications between processes take place through a channel, the fundamental communication element in Occam.

Besides channels and processes, arithmetic, Boolean, relational, or bit operation expressions are the remaining fundamentals of Occam. The basic data type in an Occam program is the 'word,' which can be used to represent numbers, characters, or Boolean values. Variables must be declared before use, preceded by the reserved word VAR. Similarly, CHAN precedes declared channels.



Occam's simplicity is demonstrated by its three fundamental processes: assignment (variable := expression); output (channel ! expression); and input (channel ? variable). All other processes are built from these three basic elements with the constructors SEQ, PAR, and ALT, and the arithmetic and repetitive functions. Contiguous lines of code, indented at the same level, share the same context. Each concurrent process has its own variables, which cannot be shared by any other process unless passed by way of a channel. Thus, programs can be devised in a modular fashion, with a well-defined interface between separate processes.

The channel, a one-way communication medium between two concurrent processes, is key to Occam's concurrency power. Communication is synchronized such that output cannot take place unless the channel is free, and input cannot take place unless the channel is supplying a value. Thus, both the input and output processes must be ready before transfer

*B. Jane Curry is microprocessor development officer at Chelsea College, University of London, Pulton Place, London SW6 5P, England. She holds a BS in computer science from the University of Reading.*

```
CHAN in,procin,procout,out              [declare channels]
PAR
  WHILE TRUE                            [continuously]
    VAR x:                              [local variable x]
    SEQ                                 [INPUT PROCESS]
      in ? x                            [input from in to variable x]
      ALT
        x < 0:                          [if value negative]
          procin ! -x                   [then output -x to procin]
        x > = 0:                        [else]
          procin ! x                    [output x to channel procin]
  WHILE TRUE                            [MEANWHILE, continuously]
    VAR X:                              [a different local variable]
    SEQ                                 [ARITHMETIC PROCESS]
      procin ? x                        [input from procin to x]
      x:=x+x                            [double x]
      procout ! x                       [output x to channel procout]
  WHILE TRUE                            [MEANWHILE, continuously]
    VAR x:                              [another local variable x]
    SEQ                                 [OUTPUT PROCESS]
      procout ? x                       [input from procout to x]
      out ! x                           [output x to channel out]
```

**Fig 1 This simple Occam program demonstrates the language's basic constructs. Its three-process system consists of an input process, an arithmetic process, and an output process. All three processes can run in parallel while data is available.**

can take place. There is no implicit buffering associated with channels. The channel operators are input (?) and output(!).

For the user, the principle of the channel is the same whether the channel is connecting processes on one or many processors, even though the implementation obviously differs.

A simple Occam program (Fig 1) demonstrates most of the language's basic concepts. The degree of obtainable parallelism is diagrammed in Fig 2. In the most efficient situation, all three processes run simultaneously: the input process accepts data from the in channel, the arithmetic process performs calculations, and the output process sends data to the out channel.

Occam is available on the VAX and 8086. Inmos Transputer and 68000 versions are being developed. While an evaluation kit is available to run under the University of California at San Diego (UCSD) p-System, it is a single-processor compiler and thus does not fully exploit Occam's potential. To demonstrate further the principles of processes and channels, a dual-processor system has been constructed based on the Z80 CPU (Fig 3). Each system is independent, but the two can be connected via the parallel interfaces (PIAs) using a ribbon cable.

In the manner of channels, both halves of the PIA are used as single-direction communication links. Thus, the lines PA0 through PA7 are input lines, and PB0 through PB7 are output lines. A full

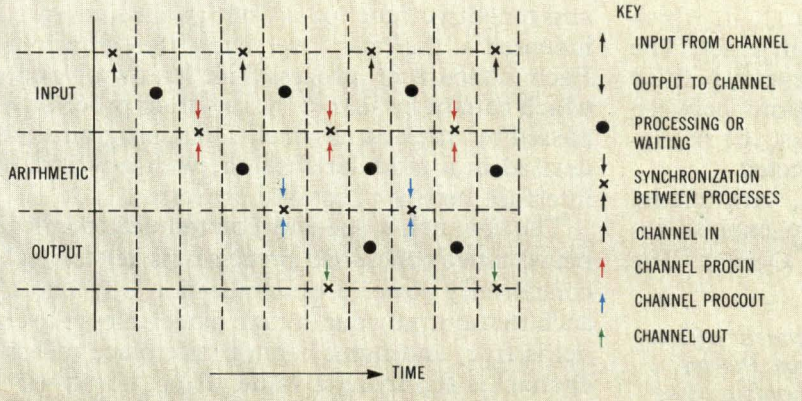



**Fig 2 In this diagram of the three concurrent processes shown in Fig 1, maximum possible parallelism is achieved when all processes are executing simultaneously.**

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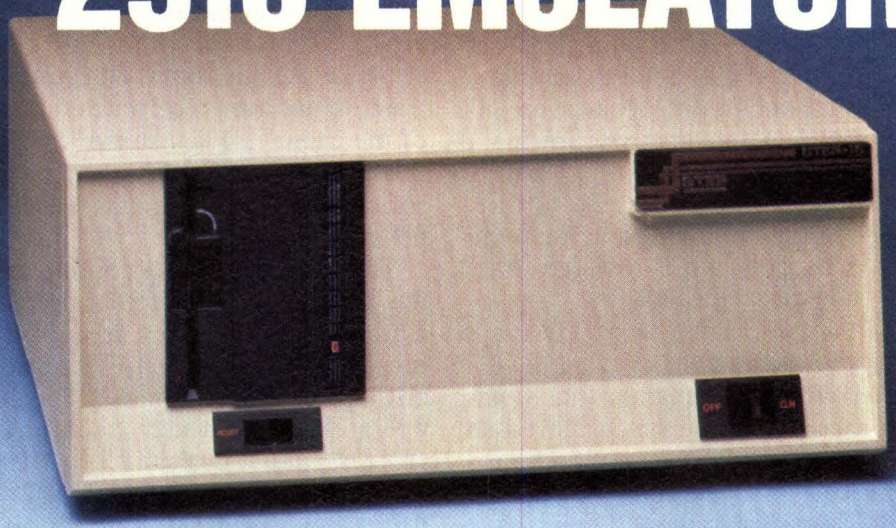

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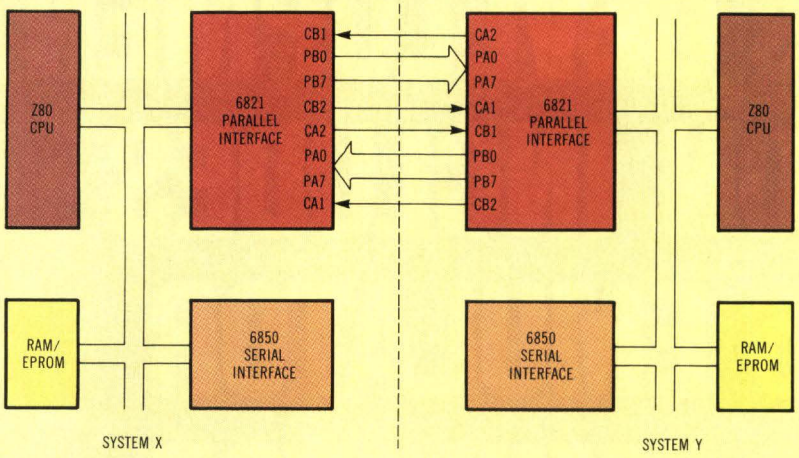


**Fig 3 The dual-processor Z80 target system's schematic demonstrates the Occam language. Each system, X and Y, can be independent of the other. However, the two can be linked, as shown, using a ribbon cable.**

hardware handshake is established between the two PIAs using the interrupt control lines CA1, CB1, CA2, and CB2. These lines can be programmed to act such that the falling edges of CA1 and CB1 set interrupt flags within the PIA and initiate a hardware interrupt. CA2 is driven low immediately following a read from the A data register (data input) and is returned to the high state on the rising edge of CA1. Similarly, CB2 is driven low following a write to the B data register (data output) and is restored to its high state on the rising edge of CB1.

## Hardware/software implementation

Occam's channel concept demands that communication along the channel be synchronized so that data transfer will not take place until both processes involved are ready. This situation can be paralleled in the hardware using the PIA handshake lines, as described above, and a very small amount of Z80 code.

When a byte is written to a PIA, its CB2 line is driven low. This drives the CA1 line on the receiving PIA low and causes an interrupt. When this interrupt is processed, the receiving PIA executes a read instruction, thereby sending its CA2 line low. This drives the transmitting PIA's CB1 line low, causing an interrupt. This interrupt restores the transmitter's CB2 line to its high state and signifies that the byte has been received and read at the other end of the channel. Fig 4 shows the timing diagram for this procedure. To complement the hardware, the software in Fig 5 is implemented to complete channel synchronization.

The interrupt service routine tests both halves of the PIA. If a character is present it is read and stored; if the interrupt is an output acknowledgment, a flag (OUTFLG) is reset to signify that the channel is no longer in use. The PIA output routine operates on a sense status basis, which tests OUTFLG until it is zero. When this condition is true, output takes place and OUTFLG is set to one, thus preventing further output until an acknowledgment is received from the other end. To avoid discrepancies, the flag setting must be made an indivisible operation with the output instruction.

As a result of the interrupt strategy, a process cannot receive input from a channel unless the interrupt service routine has received a byte.

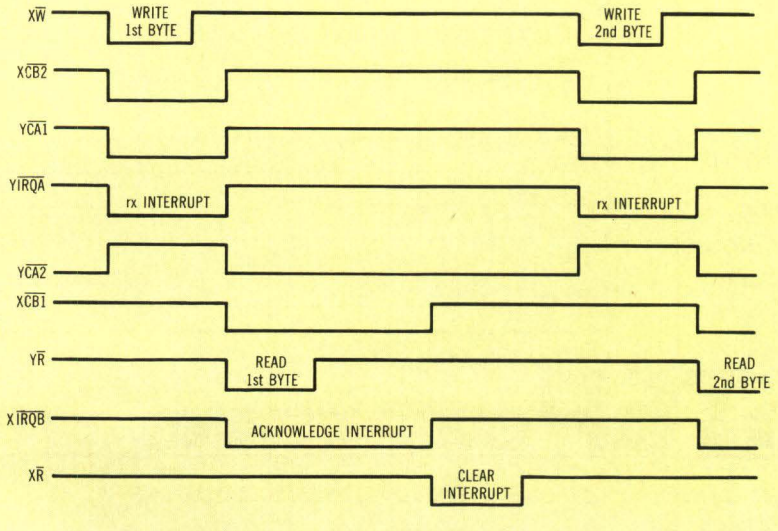


**Fig 4 In this timing diagram for hardware channel synchronization, system X is transmitting a byte to system Y. When system Y reads the byte, the YIRQA interrupt is cleared and the acknowledge interrupt for system X is initiated. Receiving this interrupt, system X must perform a read to clear its interrupt flag.**

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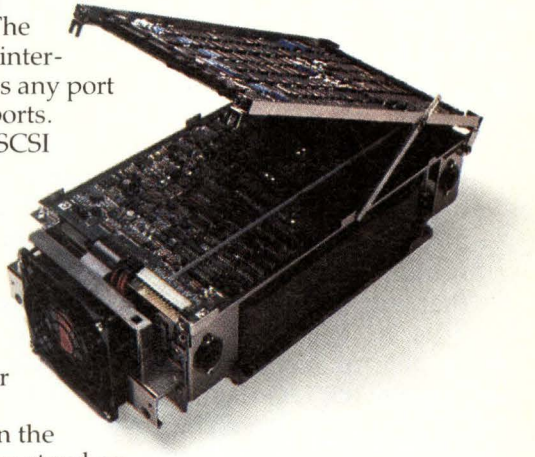

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```
ISR     IN A,[PIACRA]           ;test PIA control register A
        BIT 7,A                 ;if byte present
            JR Z,NEXT1          ;then
            IN  A,[PIAIN]       ;    read byte from input port
            store byte
    NEXT1   IN A,[PIACRB]       ;test PIA control register B
            BIT 7,A             ;if output acknowledgment
            JR Z,ENDISR         ;then
            IN A,[PIAPRB]       ;   read byte to reset int. flag
            LD A,0
            LD [OUTFLG],A       ;   reset OUTFLG
     ENDISR EI                  ;enable interrupts
            RETI

     OUTPUT LD A,[OUTFLG]       ;repeat
            CP 0                ;    test output flag
            JR NZ,OUTPUT        ;until flag is zero
            get byte in A
            DI                  ;disable interrupts
            OUT [PIAPRB],A      ;output byte to output port
            LD A,1
            LD [OUTFLG],A       ;set OUTFLG
            EI                  ;enable interrupts
            RET
```

**Fig 5 There is no implicit buffering in either the interrupt service routine or the sense status output routine for driving Occam channels with synchronization.**

Similarly, output to a channel cannot take place until the previous character has been sent and an acknowledgment received. This schema does not exactly parallel the Occam channel principle since the synchronization is between an Occam process and system software rather than between Occam processes directly. For practical purposes, however, the analogy is sufficient.

### The multitasking environment

Having established very low level system software to service channels, further software layers are required to handle the queueing and dequeueing of processes, as well as their interaction with system routines. With a dual-processor system, it is unlikely that any processor will have a single, dedicated process. Therefore, each processing element must be able to manage multitasking requirements. In implementing Occam channels, there are two categories to consider. The first is where communication is desired between two processes on the same processor; the second case occurs where a channel links processes on separate processing elements.

To run a multitasking environment, a small runtime system has been designed around the data structures shown in Fig 6. The channel and the process are the system's basic building blocks. A channel is represented by 9 bytes of information, containing the channel identifier (1 byte); the next channel in the list (2 bytes); the channel status byte (1 byte); a 1-byte buffer (1 byte); the donor process (2 bytes); and an accepter process (2 bytes).

The channel identifier is a single byte with the MSB set to zero, making the maximum possible number of channels 64. The MSB of this field will be used later in the multiprocessor implementation. The donor process field is a pointer to the process supplying data to the channel; the accepter field is a pointer to the process receiving data from the channel. If either of these pointer fields are null, it signifies a process external to this processor.

The status byte has the following significance: bit 0 (0 = buffer empty, 1 = buffer full); bit 1 (0 = donor not queued, 1 = donor queued); and bit 2 (0 = accepter not queued, 1 = accepter queued). The data structure representing the process has 5 bytes: the status byte (runnable or unrunnable) has 1 byte, the next process in the list has 2 bytes, and the pointer to process stack has 2 bytes.

*With a dual-processor system, it is unlikely that any processor will have a single, dedicated process.*

Fig 6 demonstrates the configuration necessary to implement the small Occam program in Fig 1. Along with the program's input, arithmetic, and output processes, there are two extra processes. A serial, sense status output process sends data bytes

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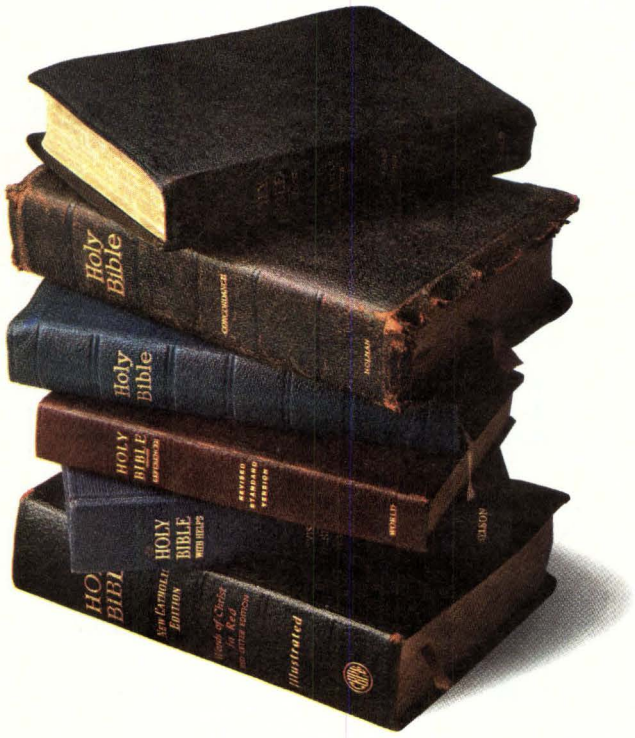


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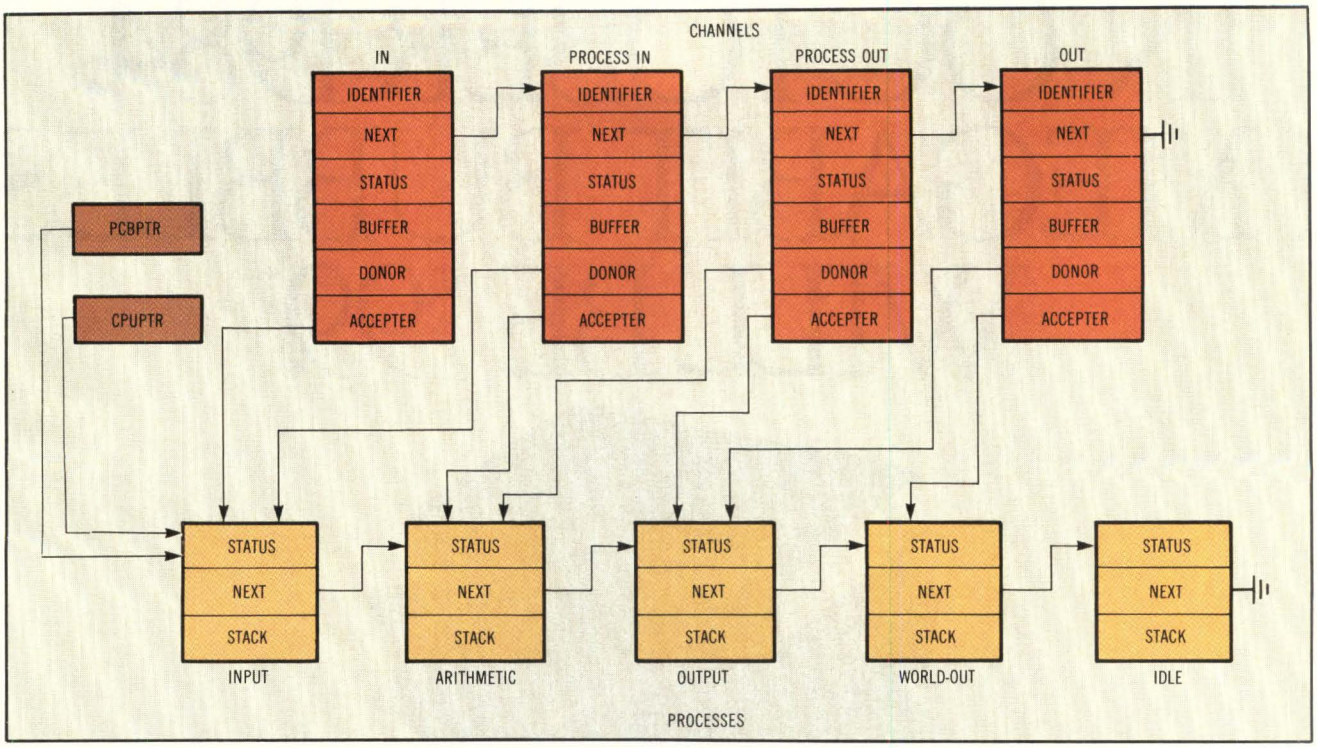


**Fig 6 Multitasking environment data structures show both channels and processes organized as linked lists, with each element in the list containing a pointer to the next element. The structures shown implement the program in Fig 1. Two pointers, PCBPTR and CPUPTR, point respectively to the head of the list of processes and the process currently running.**

to the outside world via the serial interface; an idle process is the end of the process queue and performs an endless loop until interrupted. The head of the process queue is pointed to by the variable PCBPTR. Similarly, the process currently running is pointed to by CPUPTR.

Extremely basic, the scheduling algorithm merely inspects the queue of processes and selects the first one that is able to be run. This process resumes operation one instruction beyond where it was interrupted. Each process has its own stack: when a process is suspended, its registers and program counter are pushed on to its stack. The stack pointer is stored in the third field of the process data structure. On resumption, these registers are restored with the program counter and the stack once again becomes the working stack.

The channel management routines must handle the buffer manipulation, as well as process queueing and dequeueing. Algorithmic outlines (Fig 7) implement the Occam channel operators ? (input) and ! (output).

Queueing a process takes the following form: mark the process as queued in the channel status byte; mark the process as unrunnable in the process status byte; suspend the process; and call the scheduler. Dequeueing is simpler, as there is no need to suspend the process currently running. The dequeue routine will mark the process as dequeued in the channel status byte, mark the process as runnable in the process status byte, and continue with the current process.

These algorithmic outlines implement Occam channels on a single-processor system. For a multiprocessor system, another level of complexity is introduced.

```
chan_in:  test channel status byte
          IF buffer contains a byte
          THEN
label1:       pick up byte
              mark buffer empty in channel status byte
              IF donor process queued
              THEN dequeue donor process
          ELSE
               queue this process
               on resumption, return to label1
chan_out:  test channel status byte
           IF buffer is free
           THEN
label2:         put byte in buffer
                mark buffer full in channel status byte
                IF accepter process queued
                THEN dequeue accepter process


           ELSE
                queue this process
                on resumption, return to label2
```

**Fig 7 Pictured are the algorithmic outlines implementing the ? (input) and ! (output) Occam channel operations.**

# Welcome the newest member of the Panasonic non-impact printer family.

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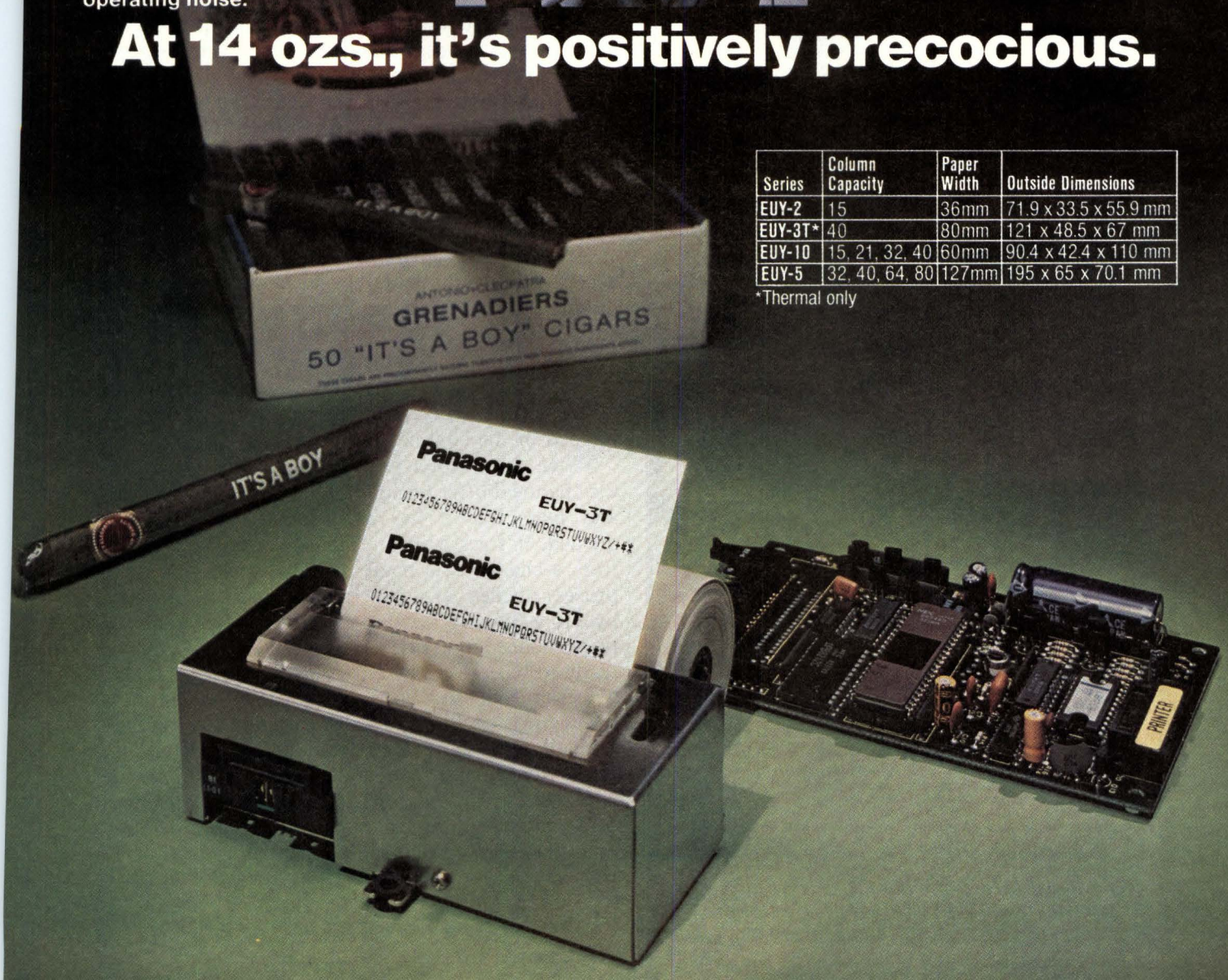


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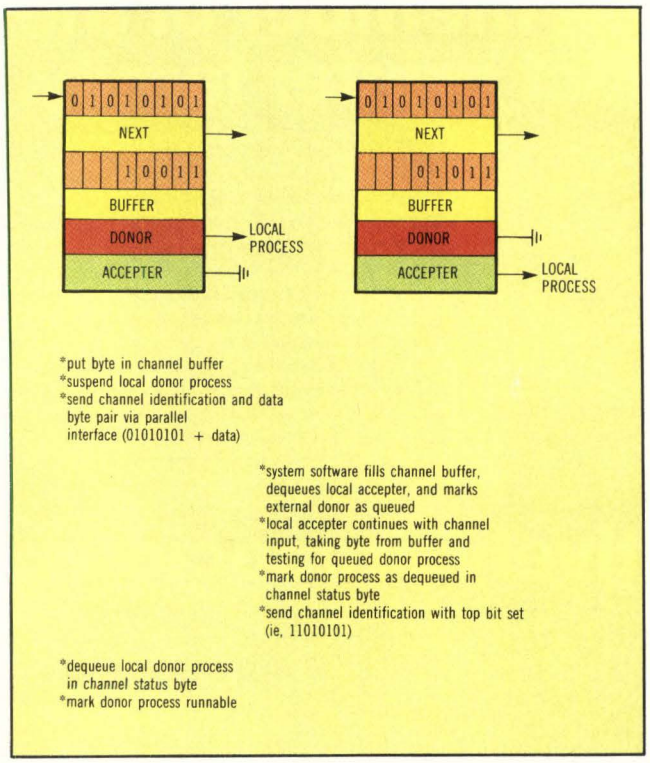


**Fig 8 Synchronization for channel buffers require that PIA transmits channel identification and data bytes to an external accepter process. A byte containing channel identification with the top bit set is sent to suspend the donor process.**

When a system consists of more than one processing element, changes must be made so that a process can be recognized as being local or external to a processor. To this end, two more bits of the channel status byte are used: bit 3 (0 = donor local, 1 = donor external); and bit 4 (0 = accepter local, 1 = accepter external).

### Channel implementation for multiprocessors

If a channel donor process is external, the channel input routine must have some conception of how to dequeue an external process. To do this, a message is sent via the PIA to the other processor, containing the channel identifier with the most significant bit set. On receiving this message, the processor can inspect the relevant channel, determine which process is in question, and proceed to dequeue this process, making it able to be run.

Synchronization along the channel will be maintained on a byte level by the hardware handshake and simple assembler routines in Fig 5. On a higher level, data must be passed by the parallel interface in byte pairs: the first byte will give the channel destination; the second byte will be the actual data. To prevent overflow of the channel buffer, the process that donates a byte to a channel for an external accepter must immediately suspend itself having donated the byte to the channel buffer. The system software handles data coming in from the parallel port and must place the data byte in the correct channel buffer, dequeue the local accepter process (if queued), and mark the external donor process as queued in the channel status byte.

When the accepter process removes the byte from the channel buffer (using the channel input operator) and finds that it has an external donor process queued, it frees it in the manner discussed. Therefore, a channel will never have an external accepter process queued. If a process is allowed to output a byte to a channel (because the process is runnable), it is guaranteed that the external accepter process is ready to receive the byte (see Fig 8).

Occam is the first language of a new generation. It is designed specifically for concurrency and parallelism, as opposed to a conventional, sequential language that must have added features to provide parallelism. This extremely simple yet powerful tool offers programming techniques that were previously unavailable in a multiprocessing environment.


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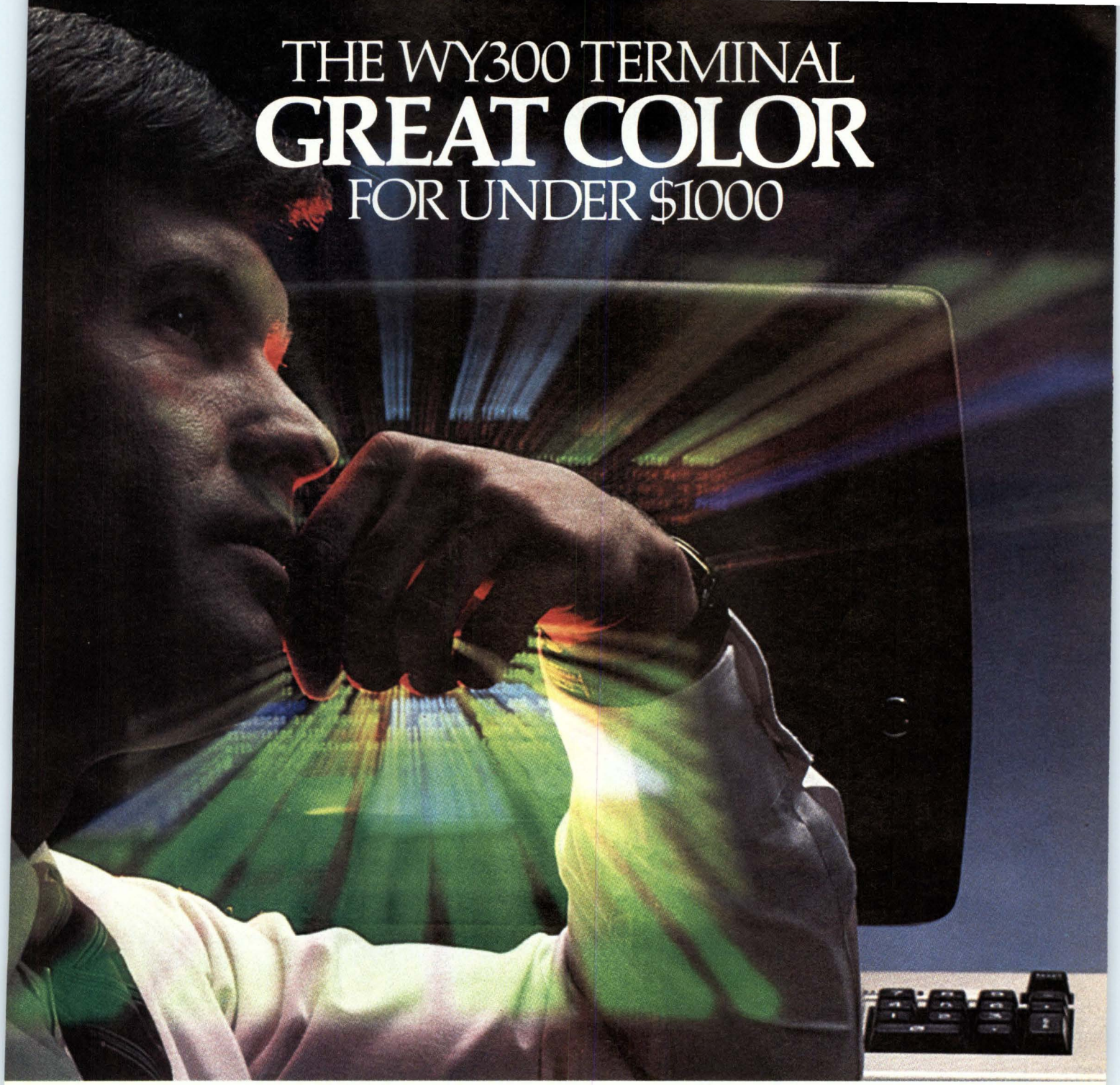

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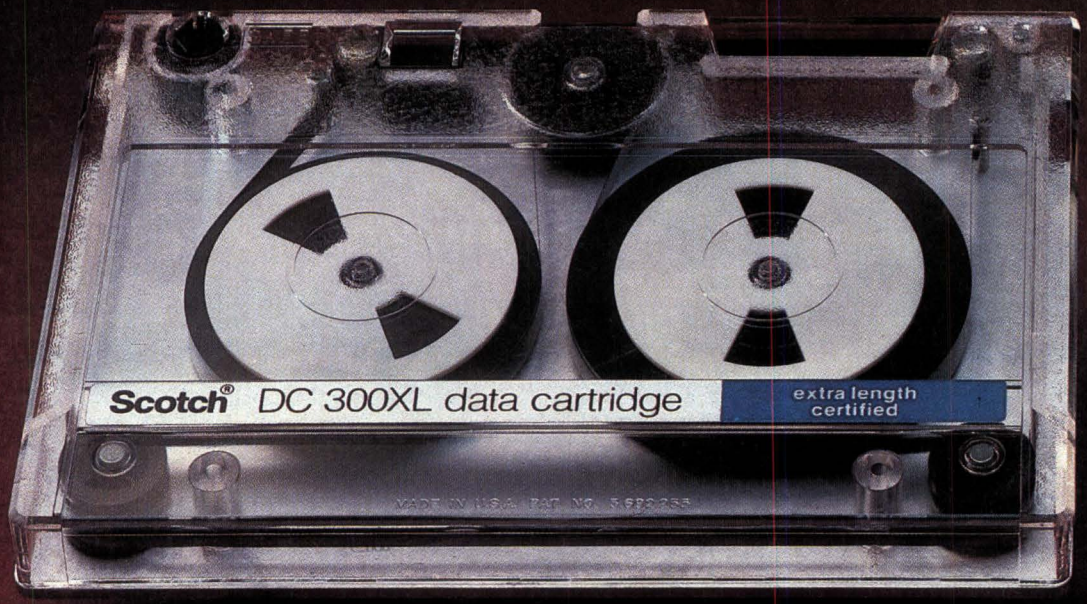


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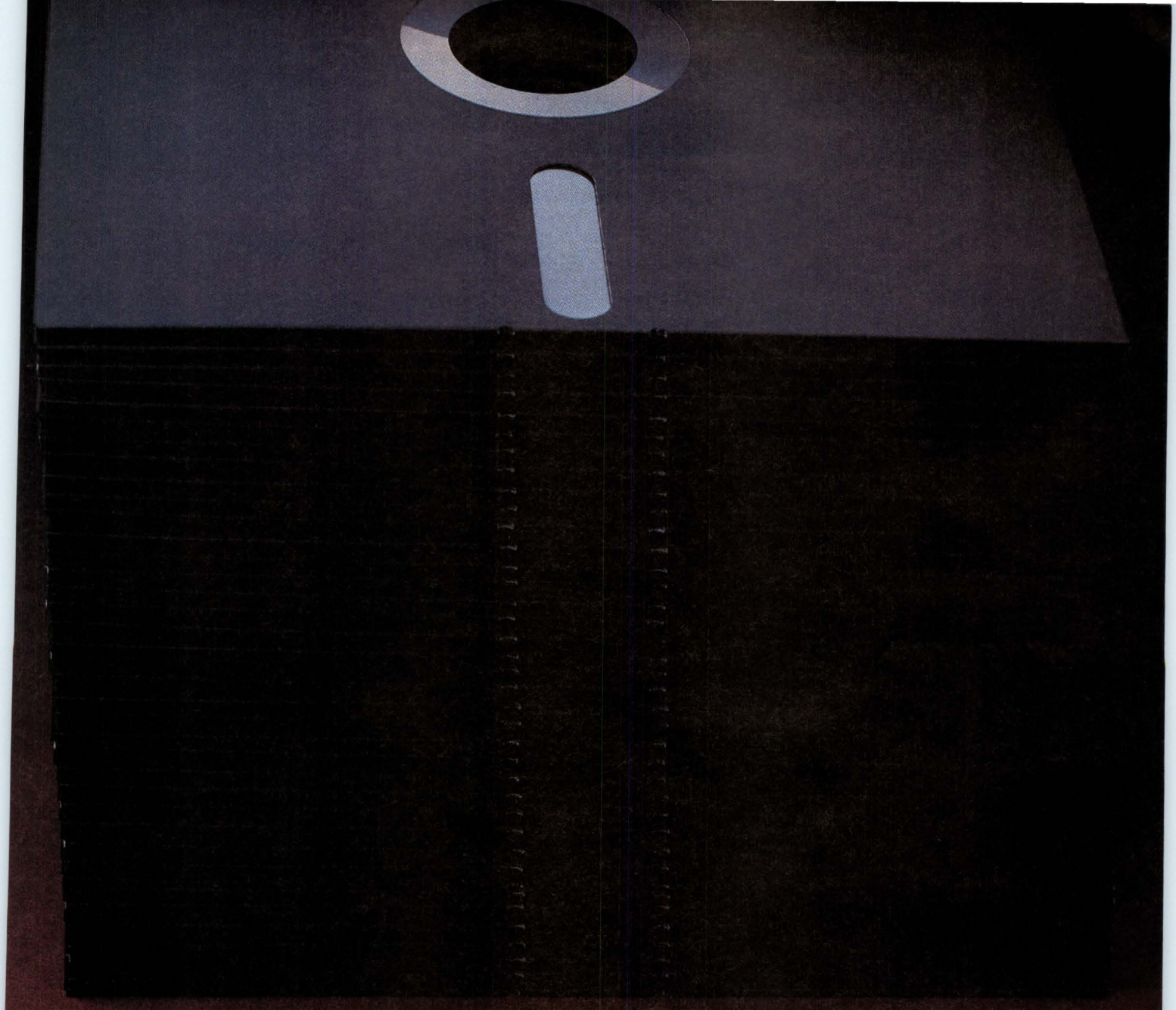

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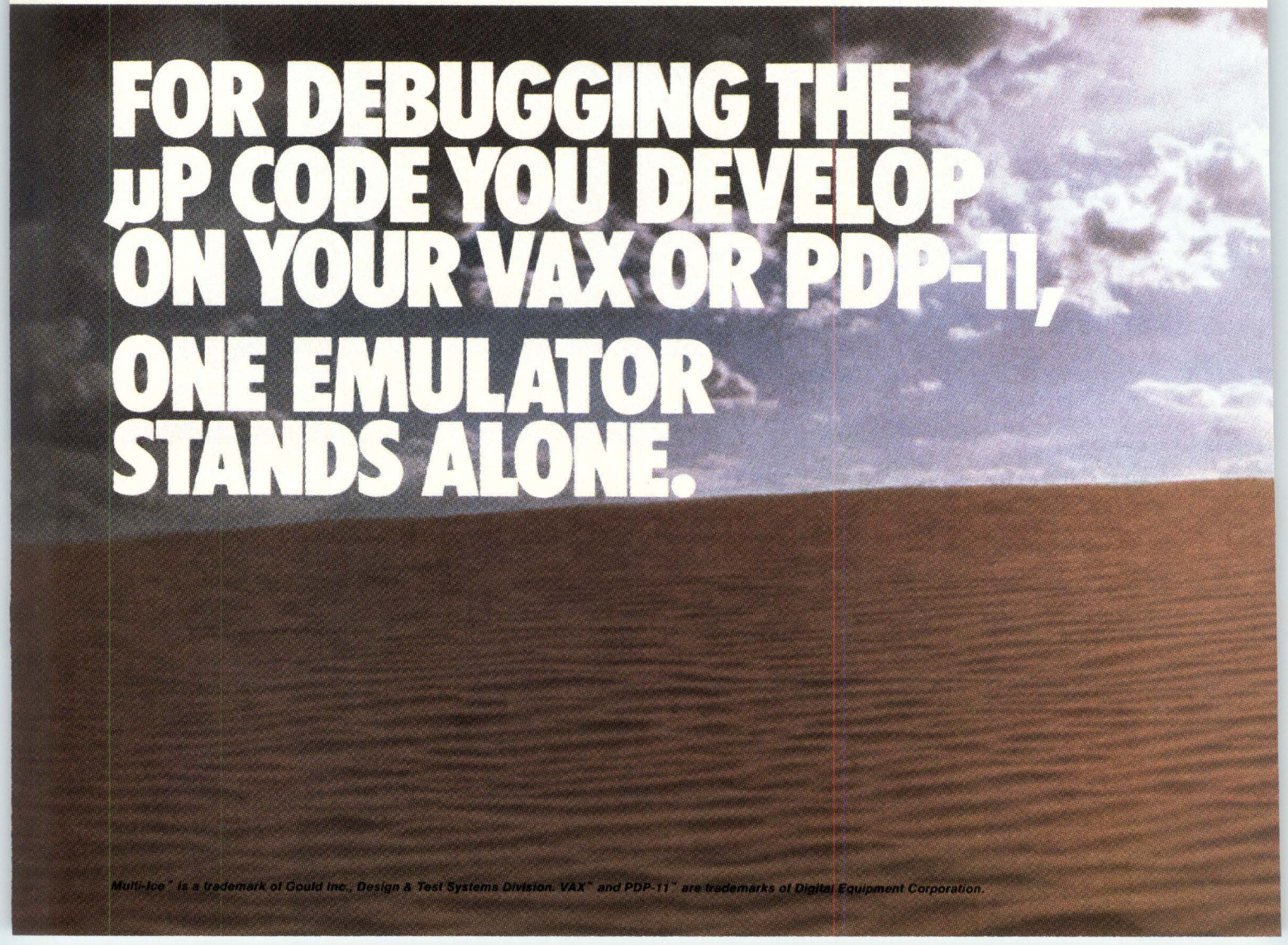


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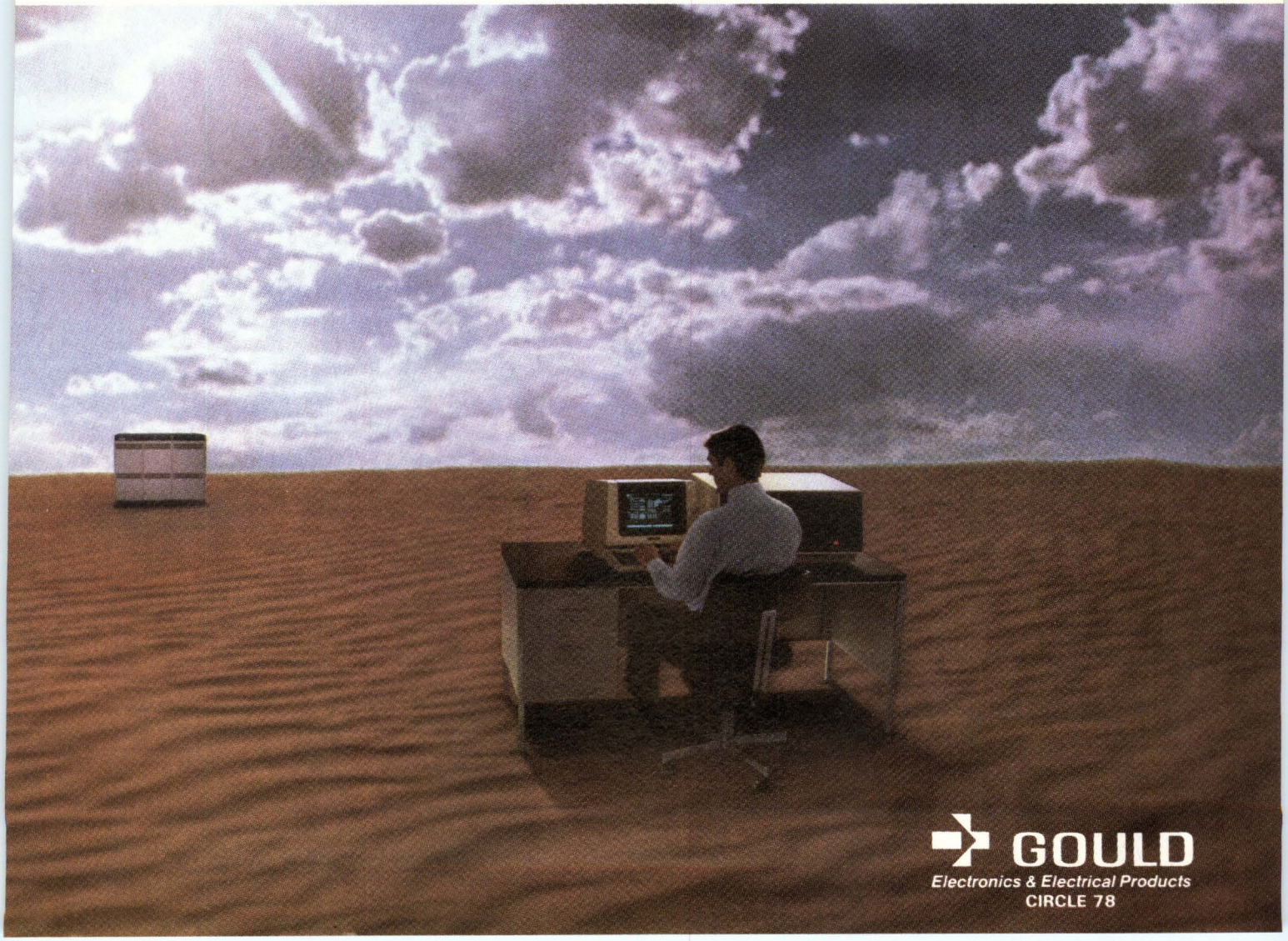

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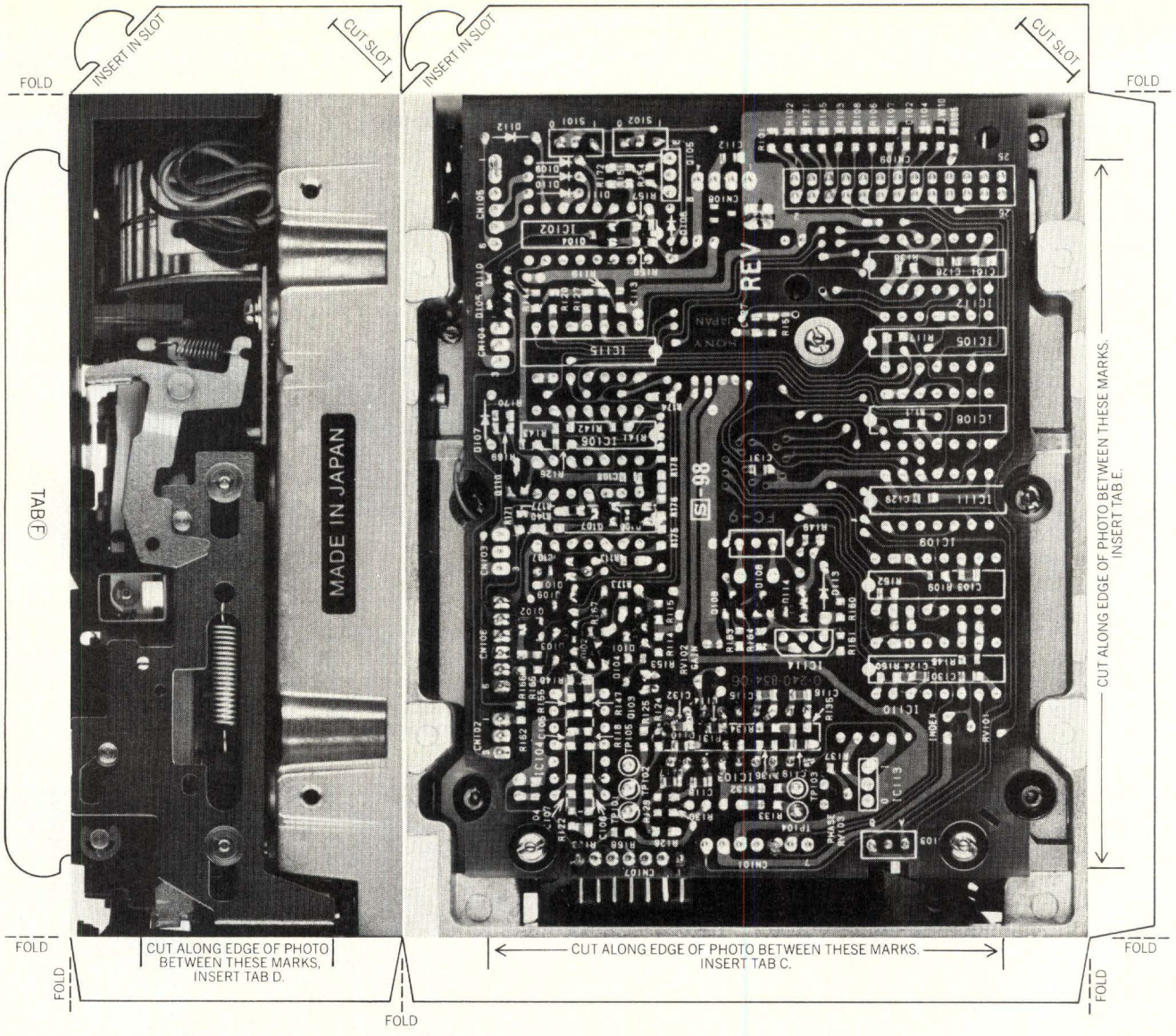


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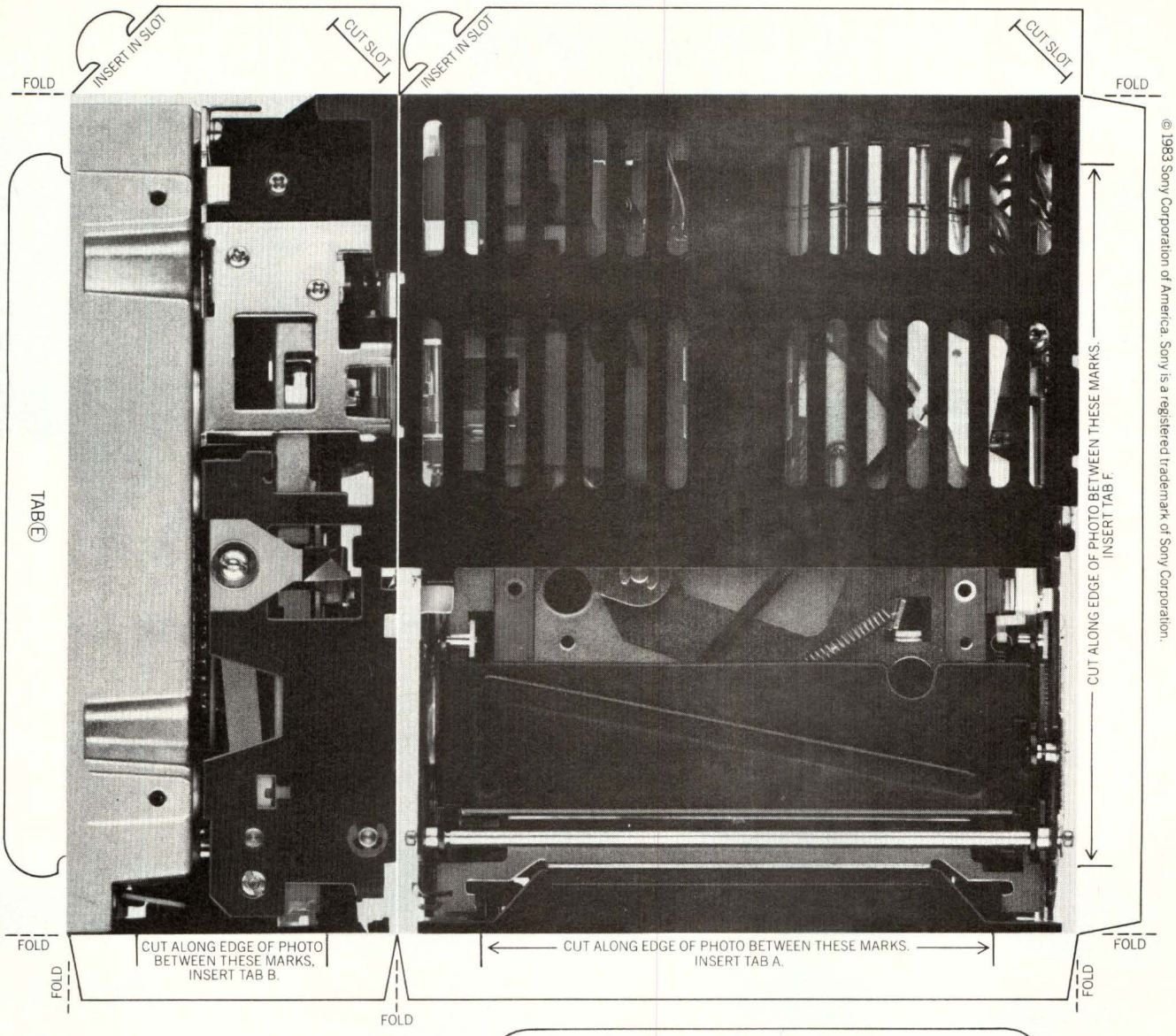


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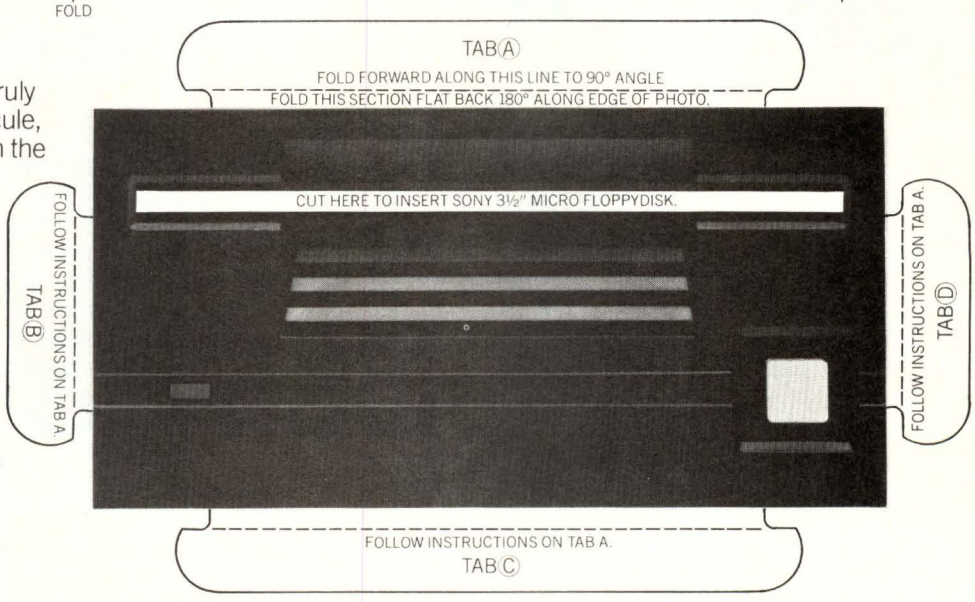


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## SPECIAL REPORT ON

# DESIGN TOOLS

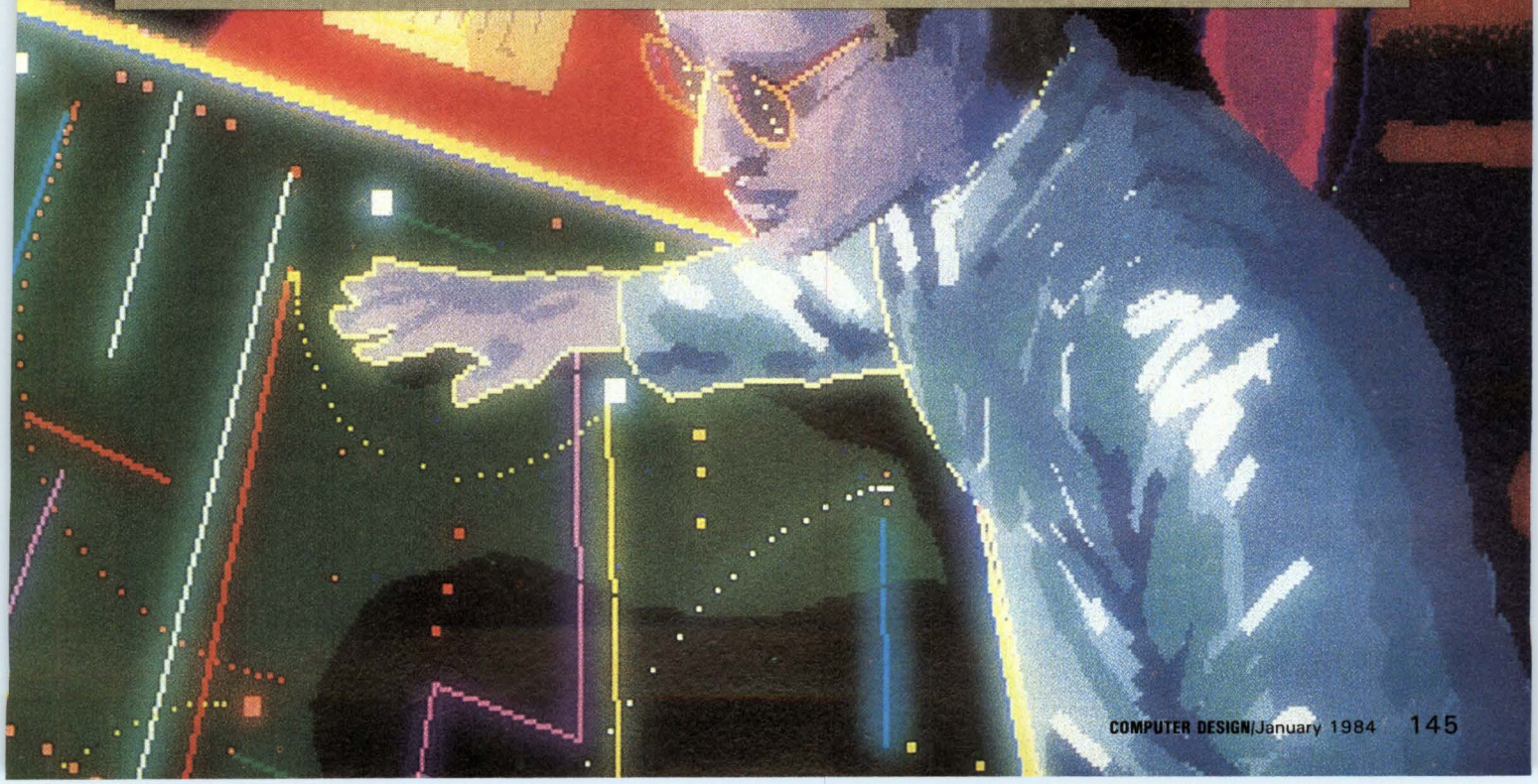
The pace of innovation in systems that incorporate embedded microprocessors and, in increasing numbers, bit-slice processors has become a blur. Both the complexity of the processors themselves and the sheer size of the applications that they support have created a demand for a whole new generation of hardware instrumentation and software tools. Of primary importance these days is the development team—a group of hardware and software specialists who spend an increasing amount of time in activities that partially overlap.

Thus, a means is needed to tie together the jobs of team members and allow them to speak a common language. The level of communication occurs in terms of the system functions and cannot be expressed in a meaningful way to all team members as either processor instructions or circuit nuances. The common tongue they are finding is the high level programming language (ie, C, Pascal, or Fortran). It is in terms of these languages that the team members are able to rise above the Babel of their specialties and communicate across the hardware/software range of the system they are developing.

This, of course, places a large burden on the development and test equipment. Not only must development systems be able to communicate with logic analyzers and emulators with data bases, but high level software must be able to select and present the vast volume of data in ways that a human can interpret. Thus, compilers and debugging software need additions and interfaces to analyze tools and graphics display systems—all of which must let the user control the lowest levels of hardware in terms of symbols rather than the ultimate details. However, the circuit must at the same time be accessible, in its smallest detail, from the high level language.

Beyond the integration of functions among design team members, today's development tools must provide ways for management to maintain control of the development effort. This means that version control, electronic mail, word processing, and many other functions usually associated with the normal office, must be linked to the technical design environment. The challenge of the new world of engineering has just begun, and as the industry progresses, more and more of the most sophisticated products yet known will be designed on the basis of *what* they are supposed to do rather than on specifically *how* they are supposed to do it.

Tom Williams
West Coast Managing Editor



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# Special report on design tools


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*by Tom Williams and Joseph Aseo*—High level development languages, multi-user networks, and powerful software debugging and analysis tools are rising to the challenge of 16- and 32-bit processors.

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**205 New tools build microsystems**
*by Larry Badagliacca*—Designing modern 16-bit computer systems requires a new set of tools. Modularity and a variety of realtime tools increase productivity.

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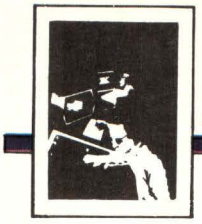
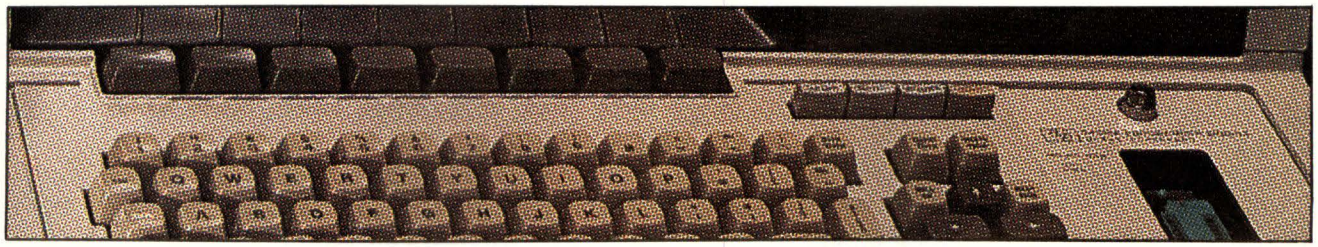




# DEVELOPMENT SYSTEMS: BIG CHIPS REQUIRE HIGH LEVEL TOOLS

**High level development languages, multi-user networks, and powerful software debugging and analysis tools are rising to the challenge of 16- and 32-bit processors.**



**by Tom Williams,**
**West Coast Managing Editor and**
**Joseph Aseo, Field Editor**

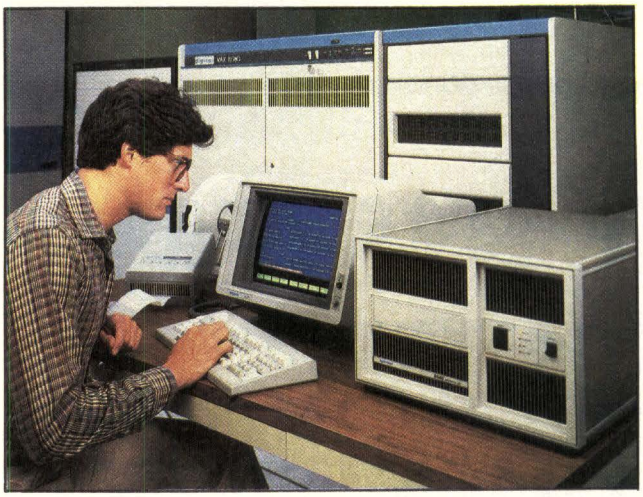
Microprocessors have outstripped the ability of humans to program them without automated assistance. Instruction set complexity, and the vast address ranges available with 16- and 32-bit processors, have catapulted the demands on development systems far beyond assemblers and editors. They require teams of programmers working with both personal and shared resources, and tools to manage and coordinate the activities of both humans and machines. Microprocessors need interfaces to protect existing investments in software and equipment, and to economically incorporate new tools into the design environment. Above all, they demand software machinery to let people get into the processors and make them do work.

High level debuggers, project data bases, source-directed editors, and code optimizers are all part of the manufacturers' push to automate the design process and increase engineering productivity. Unix, and its derivatives, with a hierarchical file structure and an extensive set of programming tools, is becoming the operating system of choice for managing the advanced development environment. Development systems for custom microprogrammed applications are starting to appear. While they are not yet as technically sophisticated as the microprocessor systems, they will ultimately provide designers with even more flexibility in optimizing systems. Each of these tools makes the design process faster and more cost effective by automating functions that were previously done "by hand."

Engineers and programmers tend to write the same number of lines of code per day, whatever the programming language they are using. This rule of thumb is the chief reason to insist on using high level languages for any software development projects, including those for controllers and embedded applications. With the present price of memory, hardware costs no longer dominate design decisions, but software (labor) costs do. Sixteen-bit CPUs, with expanded address space, have led to larger and more complex control programs. These programs would be prohibitive to build with assembly language, and without software design tools.

### Controlling complex projects

Intel (Santa Clara, Calif), in talking about its new Intellec Series IV Microcomputer Development



**The Integration Control System from Tektronix automates the specification of the hardware/software interface through the use of a menu-driven display.**

System (MDS) and Ethernet-based Network Development System (NDS-II), estimates that about 25 percent of development time is spent on writing software, an equal 25 percent on administration and project management, and fully one half on debugging and integrating the code into the product. Automating these functions is an obvious step, but the pieces must work together smoothly to get the most out of them. A uniform user interface from beginning to end, and careful thought to program compatibility, are what the company sees as the main strengths of the Series IV/NDS system.

Fortran, C, and Pascal are the most widely used development languages, and Intel offers these (with systems programming extensions, in the case of Pascal) as part of the system. It also offers its own language, PL/M, and macro assemblers.

The Series IV has a set of tools to handle the two main problems associated with creating the large applications for 16- and 32-bit processors. These include tracking the status of the project and its individual parts, and putting those parts together to make a working whole. One tool, the Source Version Control System (SVCS), is a data base that holds copies of different software module versions, as well as documentation and notes about each. The second, iMAKE, automatically compiles and links the latest versions of the modules to make up a system. iMAKE recompiles and links only in those modules that have been changed. This reduces the need for exhaustive recompilations to incorporate minor changes.

Once the software is written, it is debugged offline (in the MDS or DEC minicomputer) using Intel's PSCOPE, an interactive high level debugger. This allows the designer to step through the high level source code program, examining and changing variables and source code as necessary. This avoids searching through hardcopy listings or memory dumps, and speeds the development process.

When the target hardware is finally available, the debugged code can be integrated, using the Integrated Instrumentation and In-circuit Emulator ($I^2$ICE). This instrument supports emulation and high level debugging using symbol information supplied by the compiler and stored separately from program code. The symbol information also supports logic analysis, and logic timing analyzer display. The interface back to PSCOPE allows programmers to correlate events in hardware with high level source code.

Much like Unix, the Series IV/NDS operating system, iNDX, features a hierarchical file system, foreground/background processing (one task in each), and a screen-oriented text editor. The iMAKE and iSVCS utilities are also very similar to the Source Code Control System (SCCS) utility offered with Unix.

Tektronix (Beaverton, Ore) provides essentially the same set of functions in the TEK 8500 Series Microcomputer Development Lab (MDL). These include high level languages (Pascal for all emulated processors, and C for the 68000), standalone or DEC minicomputer processing, a smart emulator with a hardware interface for a logic analyzer, and source code debugging. Based explicitly on Unix (TEK's implementation is called Tnix), the MDL system has all of the software tools (eg, SCCS, the Unix "vi" editor, and database managers) which come with it. It also has two additional features, a language-oriented editor, and a code optimizer.

A language-oriented, or syntax-directed, editor "knows" the language it is used with—in effect, it has "keys" which generate typical statements in the language, and can catch and correct typographical errors before the compiler is run. This saves both typing time and frustration. The most common programming error in Pascal, for instance, is a missing semicolon at the end of a statement. The compiler will choke on this error, and the programmer generally feels like choking the computer.

Code optimization is something of a mixed blessing. While an optimizer can do an excellent job of compressing and speeding up compiled code, care must be taken to preserve both debugging information and the program's structure. If too much optimization occurs, the result will bear little resemblance to the source, and critical timing loops may suffer.

### Unix on the march

Standard development environments (ie, Unix) provide the common link between Gould Design and Test Systems (Santa Clara, Calif), Kontron Electronics (Culver City, Calif), Motorola Semiconductor (Tempe, Ariz) and National Semiconductor (Santa Clara, Calif). All offer standard languages as well, with Pascal and C being the most popular. Prime differences between these

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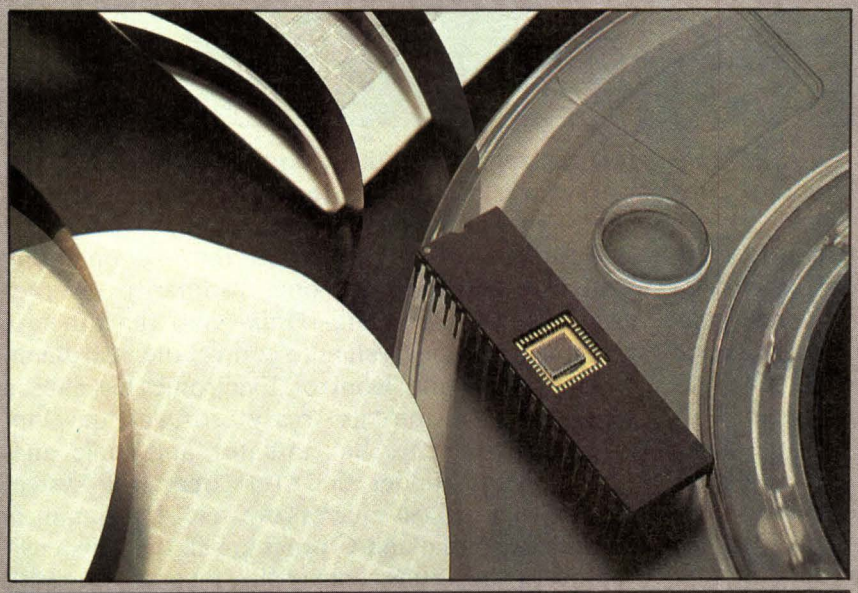
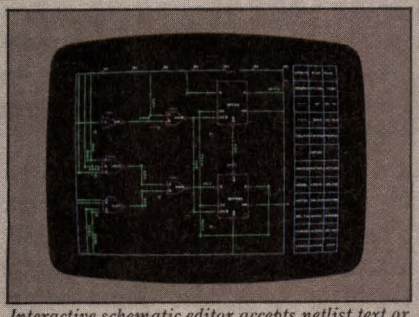
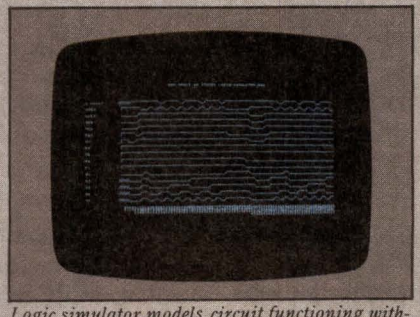
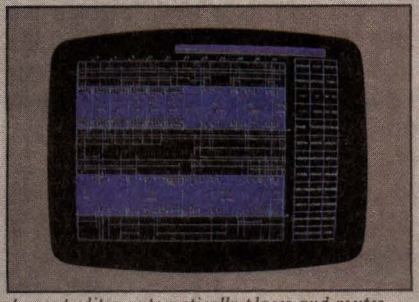




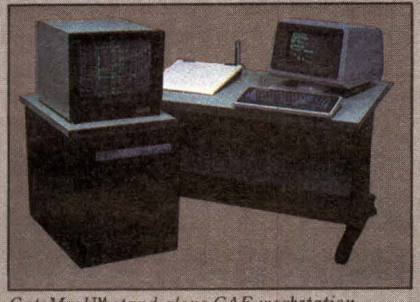
*Interactive schematic editor accepts netlist text or logic input.*



*Logic simulator models circuit functioning without actual breadboarding.*



*Layout editor automatically places and routes structured cells from our library.*



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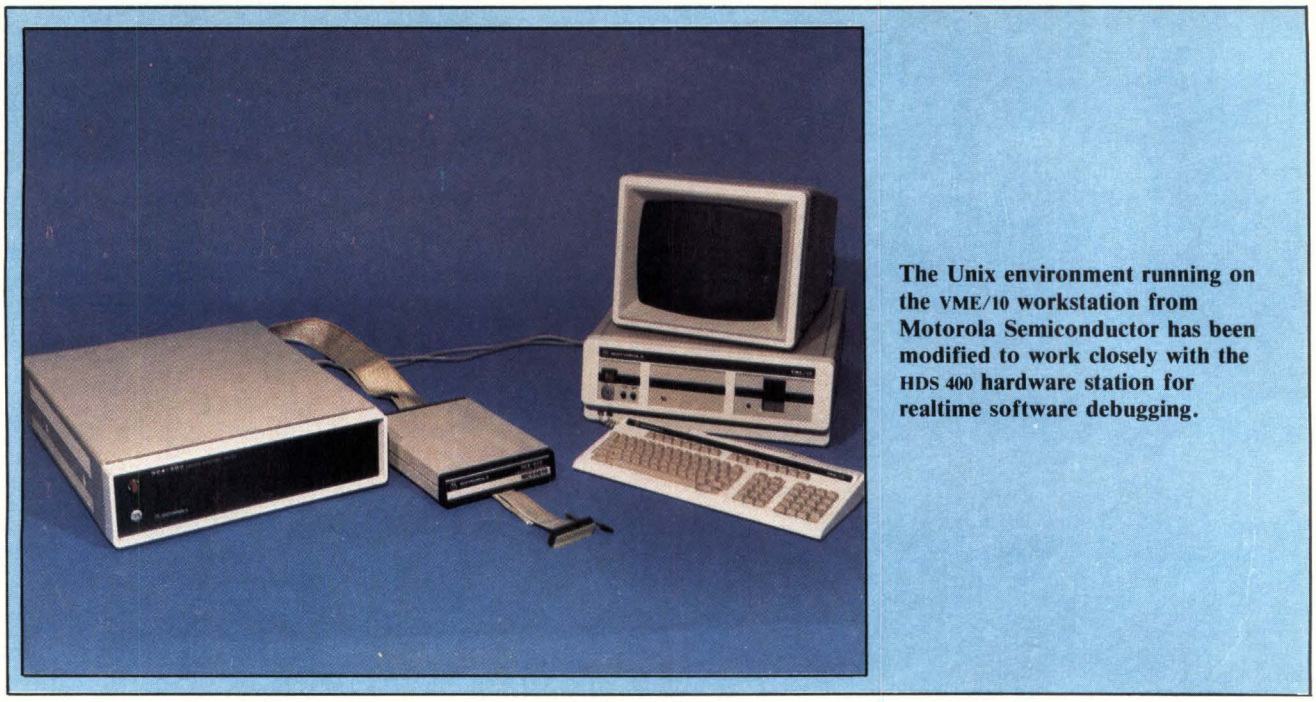

**The Unix environment running on the VME/10 workstation from Motorola Semiconductor has been modified to work closely with the HDS 400 hardware station for realtime software debugging.**

vendors' offerings focus on specific hardware configurations as well as the particular brand of Unix spoken.

Motorola has chosen Unix System V as the development environment for its ExorMACS multiuser system as well as its VME/10 standalone workstation. Bundled with this version is the source code debugger (SDB) high level language debugger familiar to users of the Unix operating system. This debugger displays high level language source statements concurrently with the disassembled object code and can provide a history of calling procedures so that errors can be traced back to the original calling routine. Users can set software breakpoints so that high level statements are executed one by one or as a range of statements. Enhancements to the original version also allow the HDS-400 in-circuit emulator to be used. As a result, the debugger can perform strictly as a software monitor like PSCOPE, or as a realtime debugger with hardware breakpoints.

Meanwhile, the other vendors have chosen to forsake the SDB and develop proprietary symbolic debuggers that are closely coupled to their in-circuit emulators. For example, Gould Design and Test Systems provides a C-based command interpreter on its 9516/9516S integration workstations. This symbolic debugger offers the same capabilities found on other realtime systems. It can link memory locations and registers with their source code counterparts, and complex breakpoints with several conditional trigger events. Its extensive program tracing monitors jumps and interrupts. The command interpreter lets users define macros with local and global variable declarations, and create compound and conditional functions. Users have full control over not only the target hardware (eg, internal registers and memory), but also the 9516/9516S workstation, since the command language includes emulator specific commands as well.

Gould points out the need for two operating system environments: one, primarily a programming environment—Unix—and the other, a realtime operating system to control the instrumentation. Meanwhile, Kontron Electronics has chosen to use Unix Version 7 as strictly a software development environment. Its emulator and logic analyzers operate under the CP/M operating system running on a Z80 microprocessor. Programmers developing Pascal and C programs in the Unix environment (which runs concurrently on a separate 68000 microprocessor) access instrumentation resources by invoking a command that calls in the CP/M operating system. Thus, the KDS968 workstation can support two users doing software development on separate terminals while another user performs hardware development on the KDS968 itself.

The Genix version of Berkeley Unix 4.1 by National Semiconductor supports two-phase debugging. One phase enables Genix to be brought up on any target system for cross development. The debugging tools mainly involve bringing up the Genix kernel in the native machine code. Its NSX16 symbolic debugger handles cross development for targets with prototype hardware as well as with the DB16000 evaluation board and in-circuit emulators. To support large memory addresses, the symbolic debugger can insert breakpoints that trigger on either logical or absolute addresses. The debugger can also do program tracing whether segments reside in physical memory or ondisk. To handle virtual addressing, a microprocessor development system must have the ability to tell where the physical addresses end and logical addresses begin. Thus, the 16081 memory

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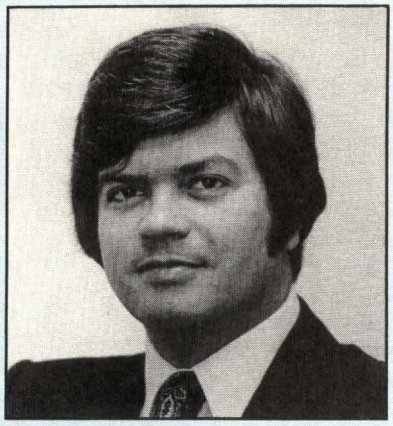
## Integrating tools at Gould

According to Dave West, vice president of marketing for Gould Electronics, multiple processors (mostly of the 16- and 32-bit variety) are driving the development environment to networks of engineering workstations. "The biggest trend that we're starting to witness is multiprocessors," says West. Single-user development systems are being linked into networks while the minicomputer VAX-type environment is increasingly being used as a high powered node in such networks. While the mini can be used as a database manager, it also serves as a programming environment. In a network, the ability to port software tools from mini to workstations also becomes an issue.



Dave West of Gould Electronics

In addition, the nature of the high level language compilers such as Pascal and C used in development and debugging goes beyond what would be required. "Most of the microprocessor-based systems that are being designed now are embedded systems," notes West. Among other things, the compiler must generate more information in terms of symbols and labels that can be used in a debug environment, and the final code should be ROMable to fit with embedded systems.

To accommodate the trend toward multiple processors—often with quite different architectures and instruction sets—Gould believes that the same high level source code should be able to produce object code for a variety of processors. To accomplish this, the company has implemented machine-specific back ends to its compilers. "The front end is so that you can move from language to language, the back end is so that you can move from processor to processor," says West.

For the total development environment, Gould sees the need for two kinds of operating systems: one for programming and project management (ie, Unix), and another for realtime control of the instrumentation. But even at the instrumentation level, there is need for a high level user interface and command languages. At this level, the language of choice is C, which is used not only to control high speed multiprocessor operation, but also to monitor that data and then convert it into information that can be analyzed by the user.

With all the asynchronous events that happen among multiple processors in the target system, the processors must be tightly coupled over the instrument's emulation bus. The realtime operating system must then be able to vertically couple control and monitoring to the higher level languages. Gould does not see its role as providing specific analysis programs, a task which is best left to the user. But the tools to produce them are provided in the form of the human interface program (HIP) and the C command language which allows control of all hardware functions in the 9516 workstation. "It happens to be an emulation computer, but it's a computer," West notes. "That general purpose power is needed for capturing, controlling, and analyzing data."

"You must be able to collect that data and control in real time, but also take that data and convert it into information the user can absorb. We went beyond the user's ability to absorb all of that data when we went from 8 to 16 bits," says West. Therefore, although the interaction between multiple processors takes place down at the hardware level, the software tools need to deal with it symbolically.

The development environment, then, has a vast task. It must preserve previous investments in tools and incorporate new ones, along with providing high level interfaces—from the minicomputer world to the detailed interaction between multiple processors. The processors in the target system may be tightly or loosely coupled. It is imperative, however, that their instrumentation be tightly coupled in a horizontal sense (among one another), and also in a vertical sense. This is to ensure that the data they generate can be manipulated and analyzed to increase the productivity of system development.

management unit includes registers designed to store breakpoint information and to support program traces.

Zilog Inc's (Campbell, Calif) Z-Lab 8000 uses the company's Zeus implementation of Unix as its operating system, and therefore has all of the popular programming languages available, as well as the Unix utilities. It does not yet have a source code debugging facility. The central processor is based on the Z8000, and will support up to 16 users working concurrently on software development or documentation. It can also communicate with other Zilog systems via the company's Z-Net implementation of Ethernet.

The company provides a line of standalone emulators for the chips it builds, which communicate with a host computer via an RS-232 link. These provide information on CPU registers, and the address bus state. They also disassemble object code as necessary and provide access for a logic analyzer.

### One source, several objects

Cross assemblers, which run on minicomputers, have been available for many years from both development system makers and independent software houses. In the minicomputer field, Whitesmiths, Ltd (Concord, Mass) has a relatively complete line. Avocet Systems, Inc (Dover, Del) supports most popular microprocessors with cross assemblers that run under CP/M and CP/M-86.

More recently, cross compilers that generate object code for almost any microcomputer have

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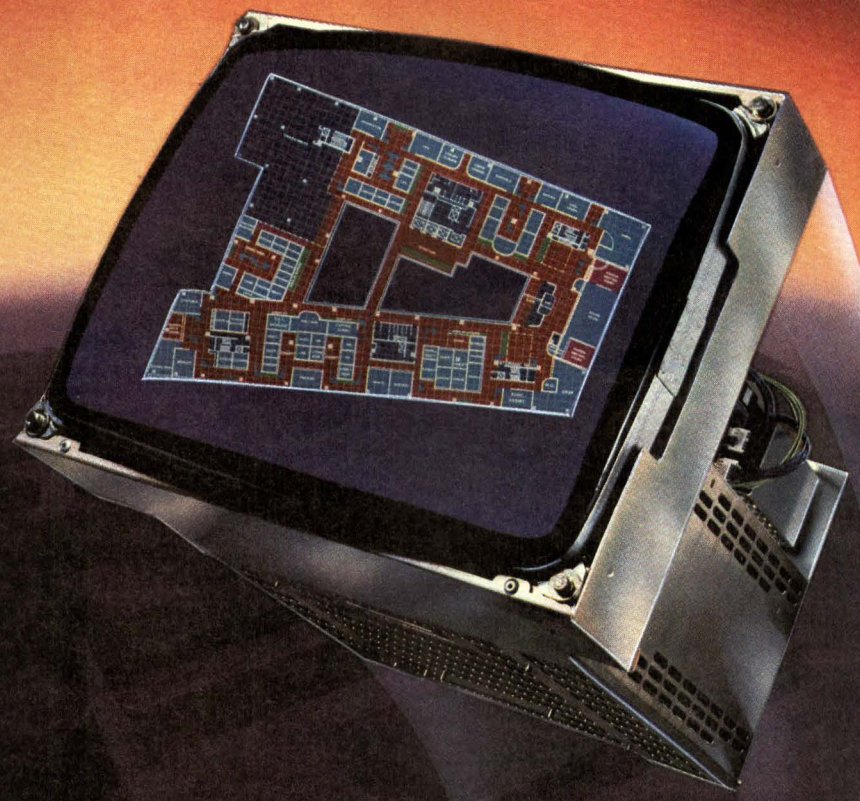

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CIRCLE 85

**The 64000 workstation from Hewlett-Packard uses a dedicated internal bus to handle peripherals, such as emulators and analyzers, while the control processor and memory reside on a separate bus. This results in increased throughput and realtime measurements.**

become common. While these tools speed the programming process, they do not address the problem of debugging the system being developed. Few programs run right the first time, and hardware design changes can start the whole cycle over again.

Simulation on minicomputers or mainframes, such as the package available from Systems & Software, Inc (Costa Mesa, Calif), is a powerful tool for analyzing a circuit before it is built. Its usefulness, however, depends on how accurately it models the real circuit. Small variations from nominal parameters on individual chips can add up to major problems in an actual design. Without a careful check of the program in an actual circuit (which takes more setup and analysis time), simulation is not a sure-fire development technique.

A high level debugger saves information from the high level source code compiler, and associates it with particular locations in the object code. These are available from all of the major development system manufacturers such as Intel, Hewlett-Packard (Palo Alto, Calif), Tektronix, and Gould, as well as from independent software vendors, such as Intermetrics (Cambridge, Mass), Boston Systems Office (Waltham, Mass), and Concurrent Sciences, Inc (Moscow, Id). A particular location in memory will contain a variable, for instance, which is part of a particular procedure in the source. If there is a problem, the designer can then examine the source code and the contents of the defined variables at the time of the difficulty, and thus find errors in logic or hardware problems more easily.

To make this approach work, the compiler must save the symbol table, containing the names of the procedures and variables that it creates while processing the source. It must then pass this information on, so that the debugger can associate the names with memory locations, and retrieve the source when necessary. The two must be written together, and be smart enough to know the type of hardware being tested. In addition, the debugger must know about the development system's resources, and the system, in turn, should be built to make the debugger's job easier. Intermetrics and Gould/Millennium (Cupertino, Calif), have jointly developed such a system, each company applying its expertise to one section of the problem.

These tools almost require the power and storage of a medium to large minicomputer, and most of the complete systems offered run on DEC or vendor-supplied machines. Tektronix and Digital Equipment Corp (Maynard, Mass), for instance, have cooperated to offer a system which runs on the VAX and controls the system under test through a Tektronix emulator. Softscope, from Concurrent Sciences, runs under VMS on the VAX or under VM/CMS on IBM machines. The announcement of the IBM PC/370, which uses the latter operating system, indicates that many more sophisticated tools, which would otherwise require a mainframe, will be available to the designer at a reasonable cost relatively soon.

Forth and Forth-like development systems, such as those available from Forth, Inc (Hermosa Beach, Calif), Infosphere (Portland, Ore) (see Evan Solley's article, "Simplify programming of realtime systems," p 193), and Inner Access (Belmont, Calif) are a curious cross between high and low level languages. The language has been described as a structured assembler for a virtual machine. It contains the control structures and the

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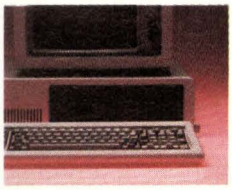

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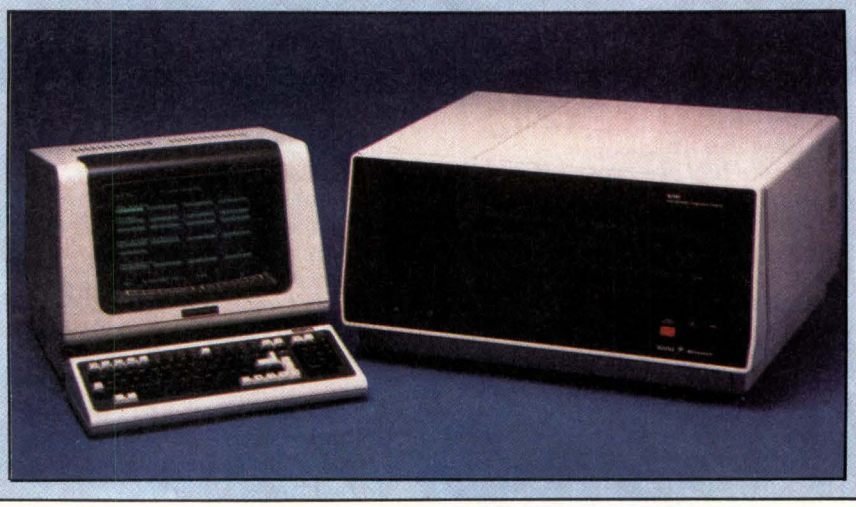

**The 9516S microsystem integration station from Gould Design and Test Systems includes a C-based command interpreter. This allows users to supplement menu functions with their own defined macro commands.**

ability to create block structures (procedures and functions) typical of modern languages such as Pascal, yet it allows direct manipulation of memory and peripherals. Its greatest advantage is compactness. Most of the code consists of 16-bit pointers, and the primitive code sections can be relatively small. In addition, once the code has been debugged at the highest level, utilities exist to strip out names and header information and produce code that can be put into ROM.

Two companies, Hilevel Technology, Inc (Irvine, Calif) (see "Microprogramming versus microprocessors," by Bjorn Dahlberg and Wendy Kane Wanderman, p 171), and Step Engineering (Sunnyvale, Calif), provide systems for developing microprogrammed processors using TTL or ECL bit-slice devices. Both companies provide the equivalent of an assembler and a software emulator, to relieve the designer of the tedious job of hand coding that custom bit-slice designs had previously demanded.

Microprogramming has been common in the development of large systems, where high labor costs could be justified on the basis of the very high final system cost. Embedded systems and controllers are very cost sensitive, however, and it has heretofore been more practical to use standard chips and software for most applications.

Technology and tools for microprogramming are still five or so years behind those available for microprocessor development, but they are progressing along the normal curve for the industry. Their future development, along with the advances expected in chip fabrication and VLSI design (eg, the "Silicon Compiler") will give the designer new capabilities and the power to build powerful, cost-effective products "on demand."

## Performance analysis

Programmers now have the tools to increase performance by recoding with high level languages as well as assembly language. As with high level symbolic debuggers, the latest generation of hardware development tools display statement numbers and labels from the original source code statements in addition to the contents at the physical addresses. Furthermore, such tools can examine execution times of individual source code statements as well as compare procedures against each other. Development system vendors active in this area include Gould Design and Test Systems, Hewlett-Packard, Intel, Motorola Semiconductor, National Semiconductor, and Tektronix.

The importance of measuring high level source code performance increases as application programs for 16- and 32- bit microprocessors move away from assembly language and toward languages like Pascal and C. No longer will there be a one-to-one relationship between source code and resultant object code as was the case with assembly language programming for 8-bit microprocessors. High level language compilers generate many lines of object code for each source code statement, making automated analysis tools mandatory.

Past efforts at performance analysis involved manually sifting through symbol maps and code listings to translate physical locations along with the original source code variables. This approach proves inadequate, however, for large application programs developed for 16- and 32-bit microprocessors that can easily exceed 100,000 lines of code. Furthermore, the complex instruction sets for 16- and 32-bit microprocessors make it more difficult to increase performance by programming in assembly language. Programmers must match instructions with the correct addressing scheme and word format (eg, integer, real, and floating point) with different combinations yielding different performance levels.

On the other hand, high level language compilers have reached a point where the performance penalty between compiled code and the assembly equivalent is small. For example, the PL/M compiler for Intel processors typically produces code 40 percent larger than the assembled equivalent, according to an experienced PL/M programmer. Optimizing compilers take advantage of special instructions and

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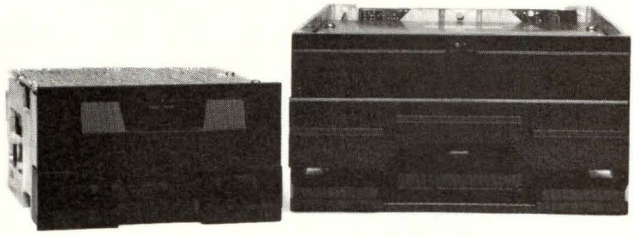

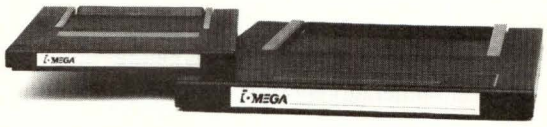


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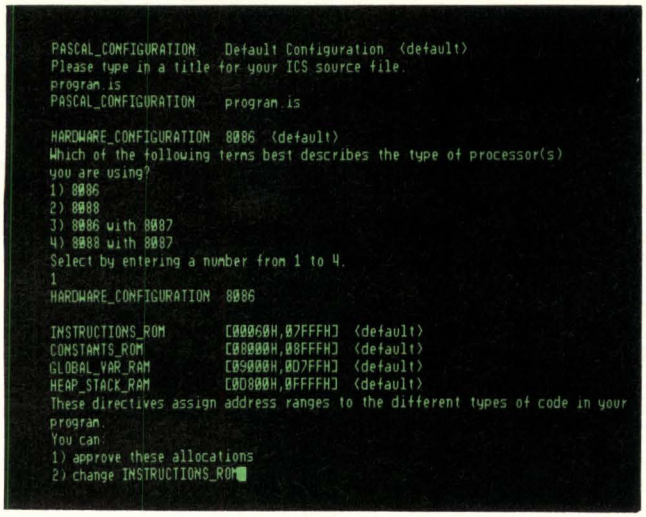


**The Language Oriented Development System (LANDS) from Tektronix supports high level language development and debugging on DEC VAX-11 computers or their own 8540/8560 development systems.**

addressing schemes that speed up execution while avoiding possible exceptions.

Performance analysis reduces potential penalties even further by highlighting which source code procedures take the longest to execute. This approach follows the programming truism stating that "80 percent of the execution time involves only 20 percent of the code." Identifying performance bottlenecks such as I/O processing or interrupt handling gives programmers the option of recoding these portions in assembly language for faster execution; this leaves the remainder of the compiled code unchanged. Programmers were often faced with the choice of either all assembly languages or all high level languages for the entire project prior to the availability of these tools which pinpoint inefficient code.

The latest generation of development tools can examine compiled code one source code statement at a time, or an entire range of statements. In addition, execution times of several procedures can be compared to detect possible trends. On most systems, programmers can view the source code statement and the resultant object code simultaneously. This enables users to manipulate either the contents of physical locations or the original source code variables and constants.

The tools required for high level language performance analysis are remarkably similar to those used for assembly programming: in-circuit emulators, state analyzers, and timing analyzers. Rather than displaying the contents stored at physical addresses, however, state analyzers now show source code variables and constants. Instead of single-stepping through object code one machine cycle at a time, timing analyzers now step through high level language programs one statement at a time, or through an entire procedure. Rather than setting breakpoints and triggers on fixed addresses and actual values, in-circuit emulators now use statement numbers and variable names.

Software monitors like PSCOPE also perform many of the same functions as their hardware siblings, but are limited in performance since they rely on software breakpoints embedded in the object code. Once triggered, control of the program returns to the host operating system for further action. In contrast, in-circuit emulators employ hardware breakpoints to monitor activity without affecting the object code execution. This becomes important in systems where even minimal delays of a few microseconds can affect the overall performance of the system under test.

Prime examples of this class of tools are the 64620S software/state analyzer and 64310A software performance analyzer from Hewlett-Packard. The software/state analyzer shows relative execution times by user-assigned events or a state distribution of different program blocks. It also provides extensive program tracing capability for either high level language or assembly language programs. Going beyond one-shot execution measurements, the software performance analyzer makes long-term measurements to detect possible trends in program execution. This analyzer is also able to measure the number of accesses to a specified code segment, the number of transfers between code segments, and memory accesses by several code segments. The 9516/9516S workstation from Gould Design and Test Systems matches closely the same hardware scheme. Motorola provides similar functionality with its combination of an HCD 400 emulator with the state bus analyzer. Tektronix takes a similar tack with its 85610 integration station with trigger trace analyzer.

Particularly useful during the debugging process, the HP64620S software/state analyzer can gauge execution speeds once individual code segments have been compiled and linked. The analyzer is most useful when coupled with an in-circuit emulator for interactive measurements. As many as 120 input channels (or as few as 20) are used to collect all logic states, or selected states within a range of narrowly defined data types. Realtime counting, either by event or time, adds another analysis dimension.

Controlling these functions is a complex triggering scheme that allows up to eight patterns connected by logical OR operations. The trigger patterns can include values, ranges, "don't care" terms and NOT terms. These trigger terms can always be enabled, either by a 15-term sequencer, or in conjunction with another analyzer or emulation module for use in multiple processor systems.

Especially useful for tracking glitches that occur infrequently, the sequencer specifies a state sequence that must occur before it can trigger, count, or store events—much in the manner of a hardware

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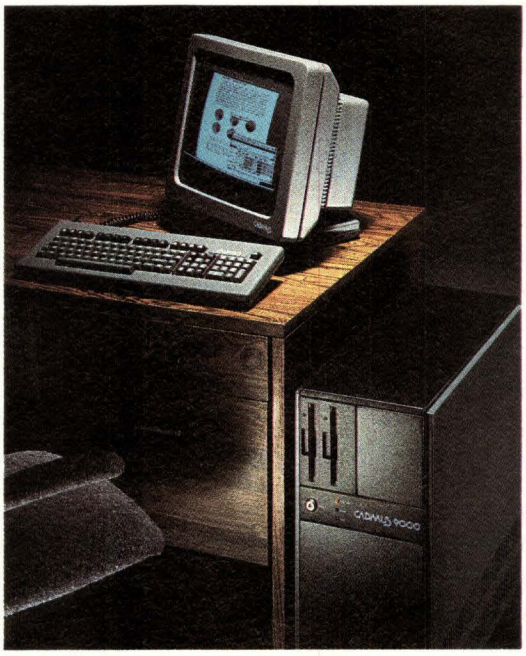

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logic analyzer. These sequences can be set to trigger after one specified state follows another, or after a state occurs a specified number of times. Up to 15 such events can be monitored with ranges or values corresponding to program addresses or other information stored in the symbol maps. Graphics display of the acquired data takes the form of either a histogram that measures the percentage of execution time used by each of the events, or a frequency distribution of events that displays the sequence of their occurrence.

Histograms and tables play a major role in the 64310A performance analyzer's display of activity among several object code modules. The histogram gives programmers an easy-to-interpret bar graph representation of program or memory activity, while tables show the actual data that serves as a basis for the histogram. In addition, users can switch from absolute to relative measurements to compare time and occurrence measurements between several object modules or against the entire program.

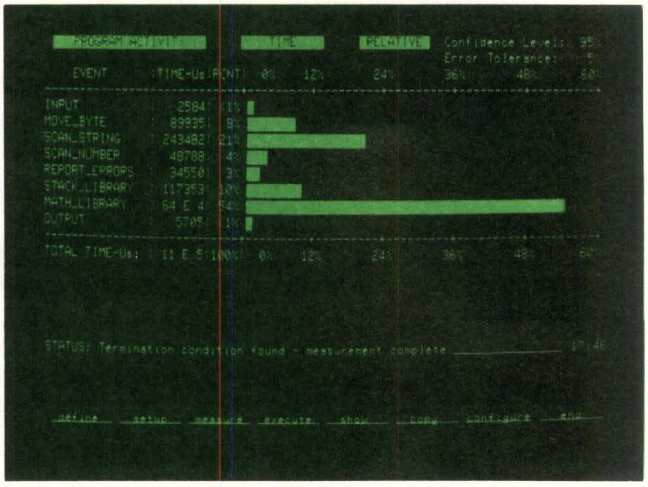
Data is continuously accumulated and displayed in the histogram format. In fact, this information can be used for further processing. For example, users can glean such statistical information as means, standard deviations, and confidence levels to gauge the accuracy of the activity measurements.

## The bigger picture

Going beyond merely measuring one-time execution of selected object code modules, the software performance analyzer allows programmers to monitor the time distribution of executing object modules to see if they are performing within expected bounds. For example, the analyzer can tell a user that module A takes 50 to 60 $\mu$s to execute 36 percent of the time. Furthermore, users can include (or exclude) in the measurements the time involved interacting with other code segments or external inputs to spot best-case and worst-case conditions.

If programmers are concerned with the interaction between two object modules, time interval measurements can measure the activity between them (eg, the time interval between module A and module B ranges between 6.5 and 6.6 $\mu$s). Likewise, users measure the interval between the time a selected code segment is exited and the time it is entered again to judge the intensity of demand. Overall software traffic patterns are detected by measuring the number of transfers between selected code segments.

Other vendors also plan on using graphic displays to highlight performance measurements. For example, Gould Design and Test Systems provides an application package to display program activity comparisons as well as memory activity. Motorola provides histogram displays as part of its state bus analyzer module. Often linked with its HCD 400 in-




**Histogram displays are part of the software analysis package offered on Hewlett-Packard's 64000 development system. The program activity measurements display actual execution times for several modules as well as their relative performance against each other.**

circuit emulator, the analyzer displays relative performance for both program and memory activity.

More important than vendor-defined measurement routines is the ability for users to write their own measurement and display routines. Gould Design and Test Systems takes the attitude that vendors cannot conceive of all possible measurements that users might need to accurately gauge the performance of their products. Extensive command languages provided with the development systems give users the tools needed to design custom measurement routines as well as displays.

Customers could quickly develop such packages since the development systems already have command languages that control the hardware. As an illustration, Gould includes a C-based command language for its 9516S emulation system. This language has the hooks needed to acquire such information as memory transfers from the emulators, monitor state, or timing analyzers, and to display the results on the CRT screen. Tektronix includes such capabilities for its 8500 development workstations through its Pascal Debug package. Motorola operates a Unix-based environment with enhanced C-shell to offer similar capabilities on its ExorMACS and VME/10 systems.

Perhaps it is not important to provide such detailed information since the state of software management is such that specifications cannot be drawn to such minute detail. Robert Freund, software manager for National Semiconductor, believes that such measurements as relative performance comparisons give a global view, but do not provide any added insights to pinpoint problems within the code itself. Software management tools have yet to reach the point where specific code segments have an expected execution time, so measurements focused on comparing the two are, then, often subject to wide interpretation, according to Freund.

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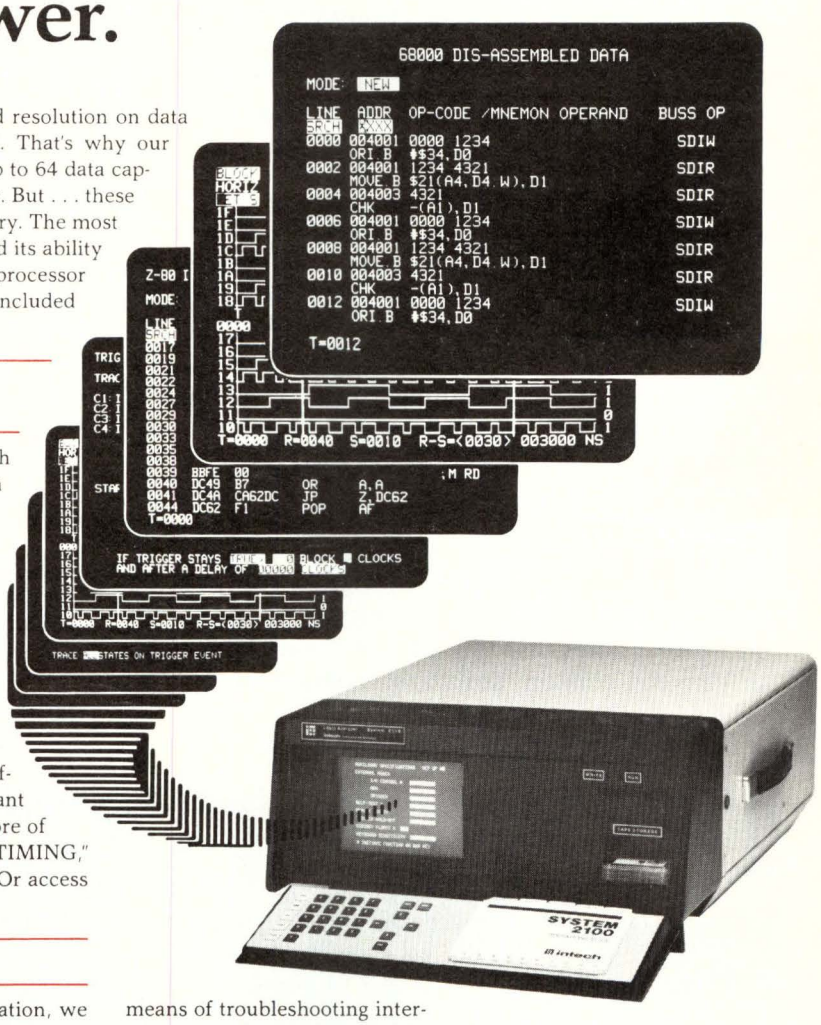


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Whatever the detail of the measurements provided, users will still need to have the option of modifying programs at the object code level or the original high level language source. All vendors also provide the ability to insert high level patch files for debugging with the option to replace them when production begins. This issue is not so much a programmer's dilemma, but an engineering management decision concerning standards.

### Where to optimize

Of critical importance is the ability to document changes during a product's life cycle. Tools such as the Source Code Control System on Unix-based development systems usually track revisions to source code only. Object-code patches to speed execution or fix problems often fall between the cracks in such an environment. They fail to get documented during the revision process, and knowledge of such fixes vanishes when the engineer leaves the company.

Many vendors recommend that customers implement standards for their respective projects, emphasizing changes to source programs only. Mike Haggerty, software development manager with Motorola, notes that this may be the only means to effectively contain software maintenance costs, which usually comprise almost 80 percent of the effort during a project's typical five-year life cycle.

Meanwhile, assembly language runtime libraries offer a compromise between the needs for documentation and increased system performance. Previously used to handle common realtime routines (eg, I/O processing), such libraries can easily be created as part of software performance analysis. In fact, Tektronix provides an Integration Control System that can link runtime libraries at the same time that such hardware parameters as memory ranges and interrupt handling are specified.

Such tools will be especially effective for designers using off-the-shelf single-board computers and peripherals. With the hardware architecture already specified, designers can only increase performance by ensuring that the software has few bottlenecks. The ability to closely monitor compiled object code and make necessary changes at the source code, or with assembly language routines, makes software performance analysis a key tool for the future.

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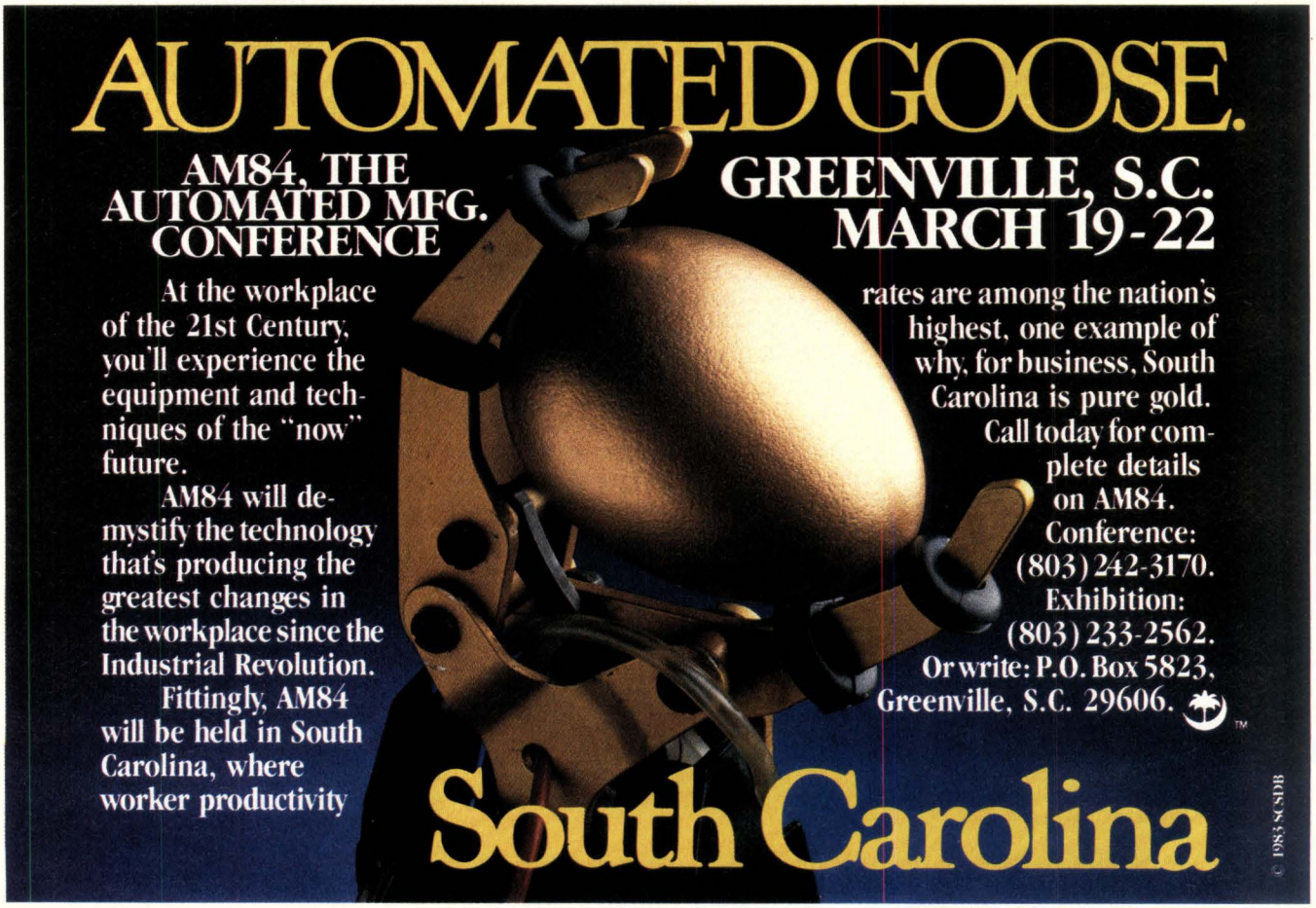





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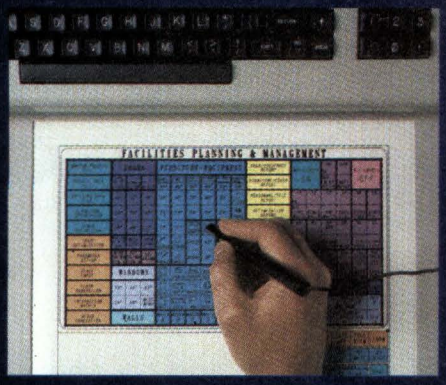

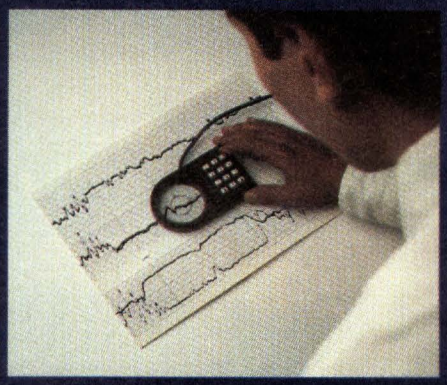

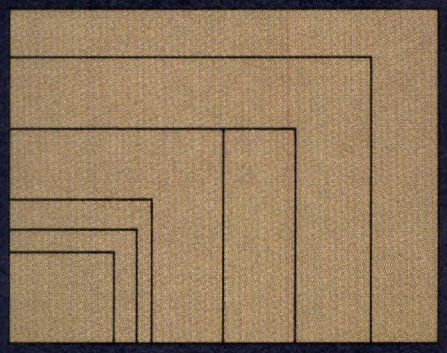

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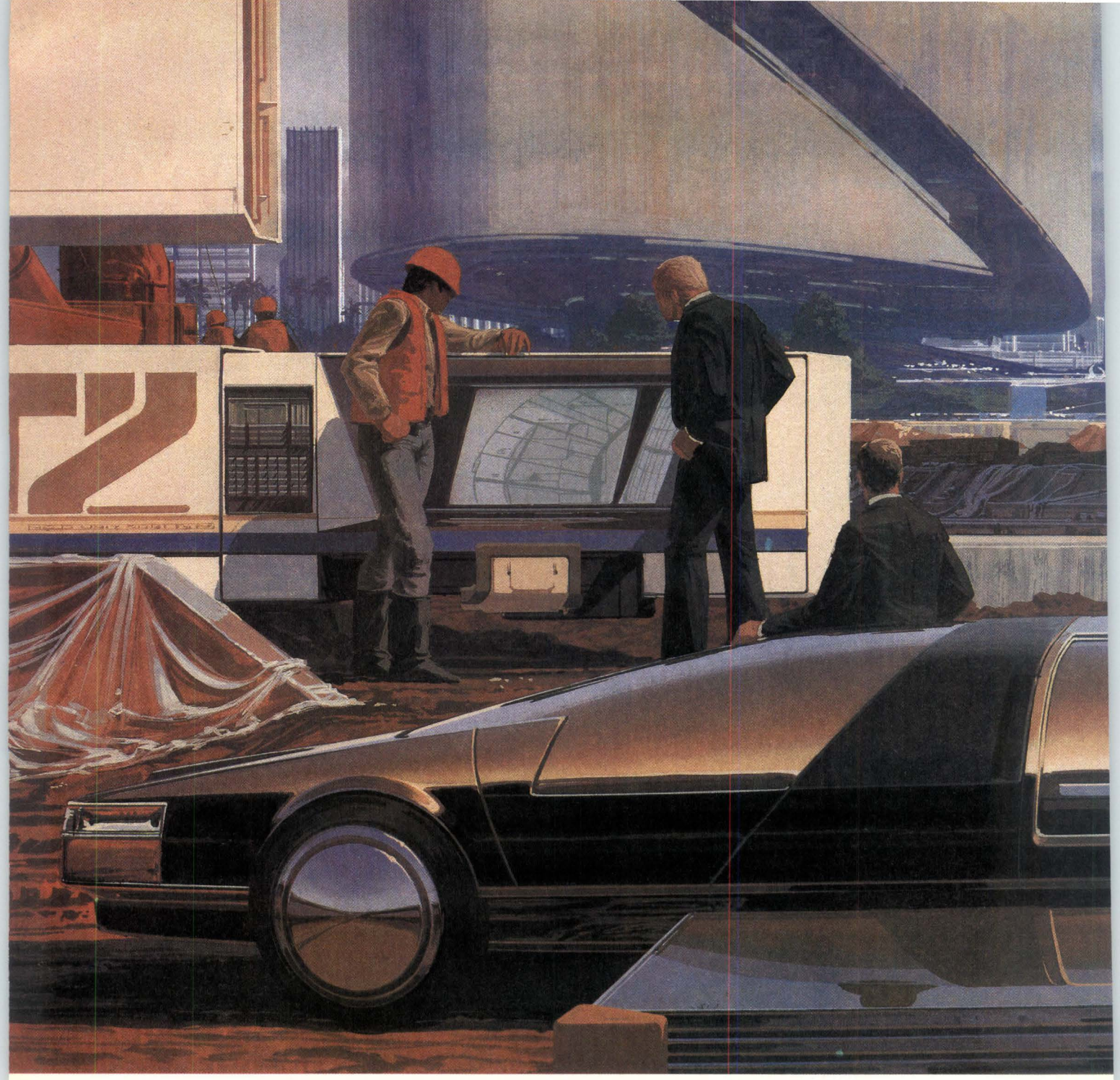

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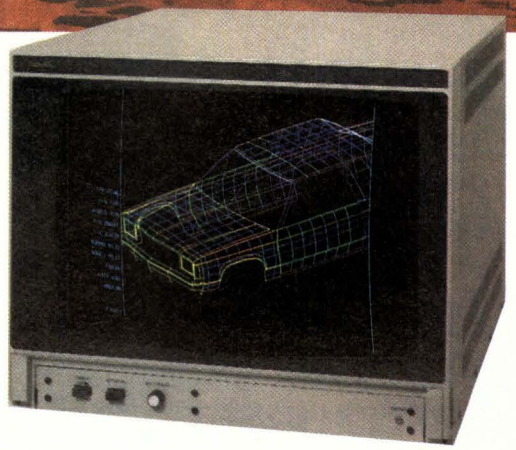

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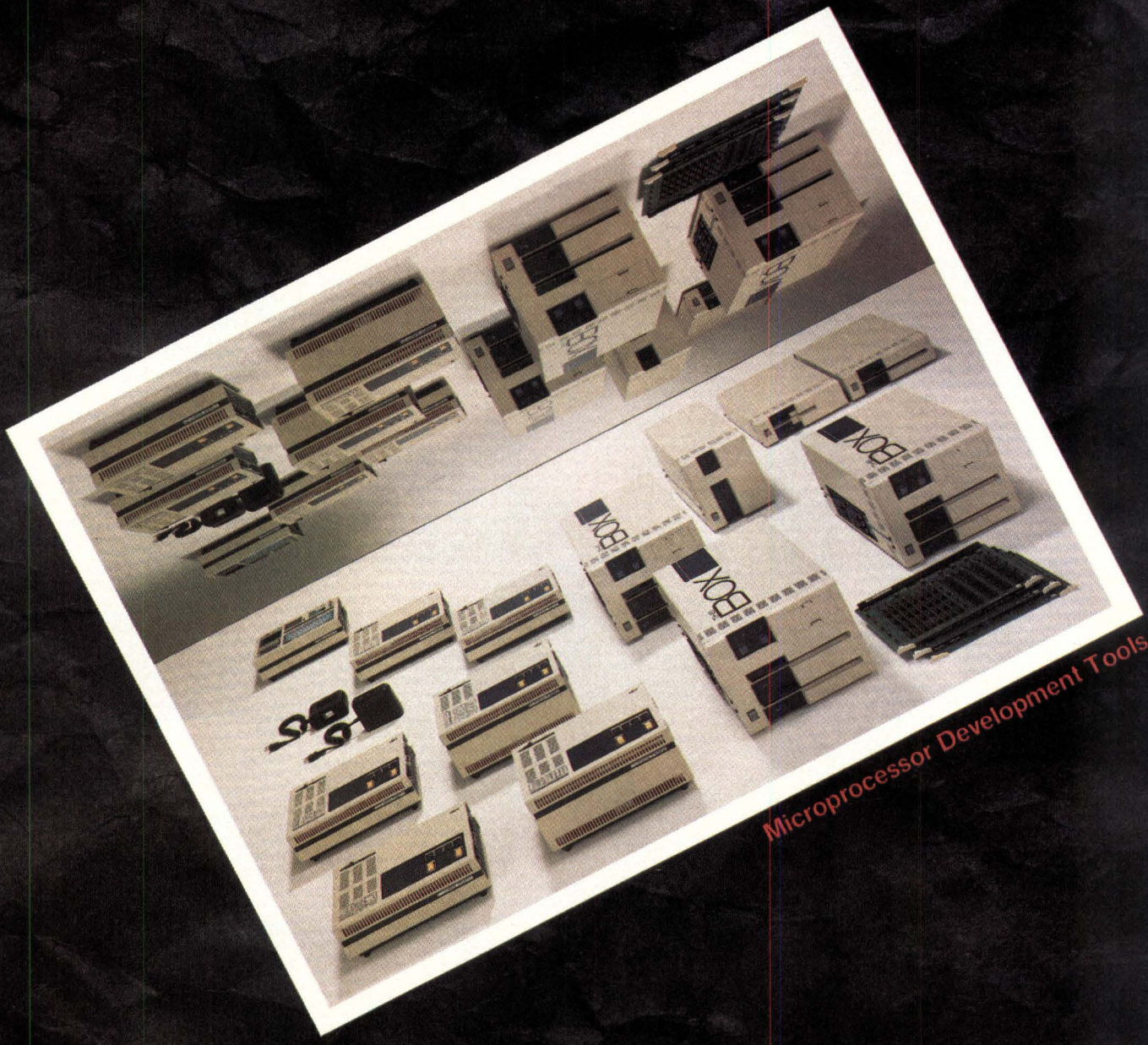


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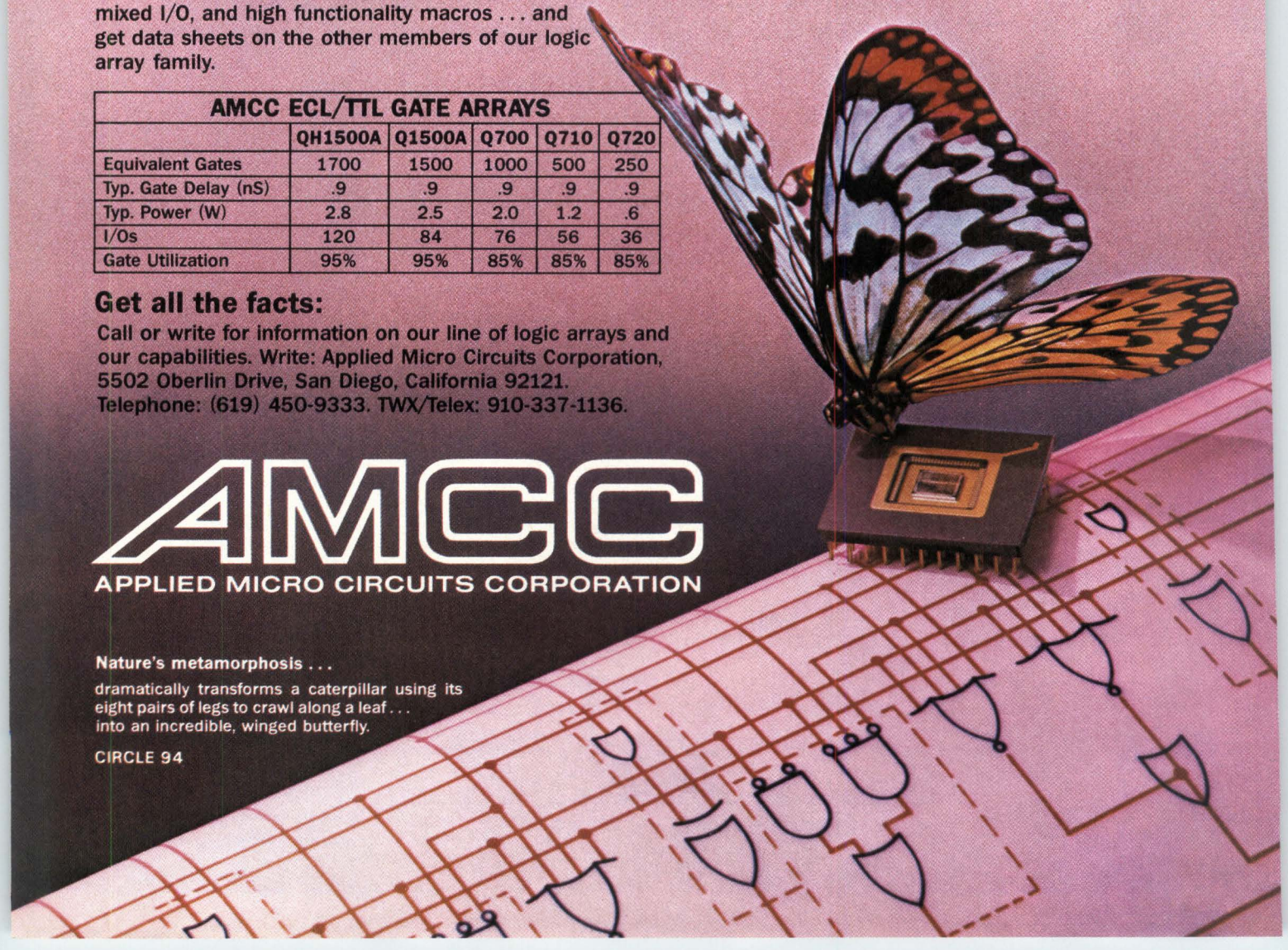

**Nature's metamorphosis . . .**

dramatically transforms a caterpillar using its eight pairs of legs to crawl along a leaf . . . into an incredible, winged butterfly.

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# MICROPROGRAMMING VERSUS MICROPROCESSORS

**Designers who choose a standard microprocessor chip may quickly discover that semicustom and custom variations have boxed them out of the market, and that microprogramming is indeed the wave of the future.**

**by Bjorn Dahlberg and Wendy Kane Wanderman**

Despite tremendous growth in the use of standard microprocessor chips, these off-the-shelf devices are inadequate in many design situations. Using them can often hinder a clean, top-down design approach, and stifle designer creativity. In some cases, too many support chips are required to achieve the desired control and performance. This raises system cost dramatically. In other cases, the software needed to make these chips perform as desired becomes enormously complex, raising real costs excessively. This software, which accounts for 60 percent or more of the total effort, is relatively unprotected; that is, it is easily copied. This leaves the designer at the mercy of competitors. Furthermore, since commonly available chips are used extensively, the capabilities and limitations of the selected chips tend to define, and can limit, overall system performance.

Microprogramming is reemerging as an alternative to this dilemma. Microprogrammed bit-slice processors, custom VLSI, and other nonstandard forms offer designers the chance to achieve superior system performance, and to implement more functions in less time. Microprogrammed designs can also be more secure while offering more flexible upgrade paths. These advantages can help designers meet critical market windows and extend product life cycles. A microprogrammed design by itself offers better proprietary protection than a design based on off-the-shelf microprocessors. In addition, this protection is further magnified when the design is embedded in a custom or semicustom VLSI chip.

The concept of microprogramming originated in the 1950s and although overshadowed later by random-logic design, it has made steady inroads. With increased interest over the last decade (that parallels the industry's accelerated interest in semicustom and custom chips) a new wave of use is underway. This activity is still limited by

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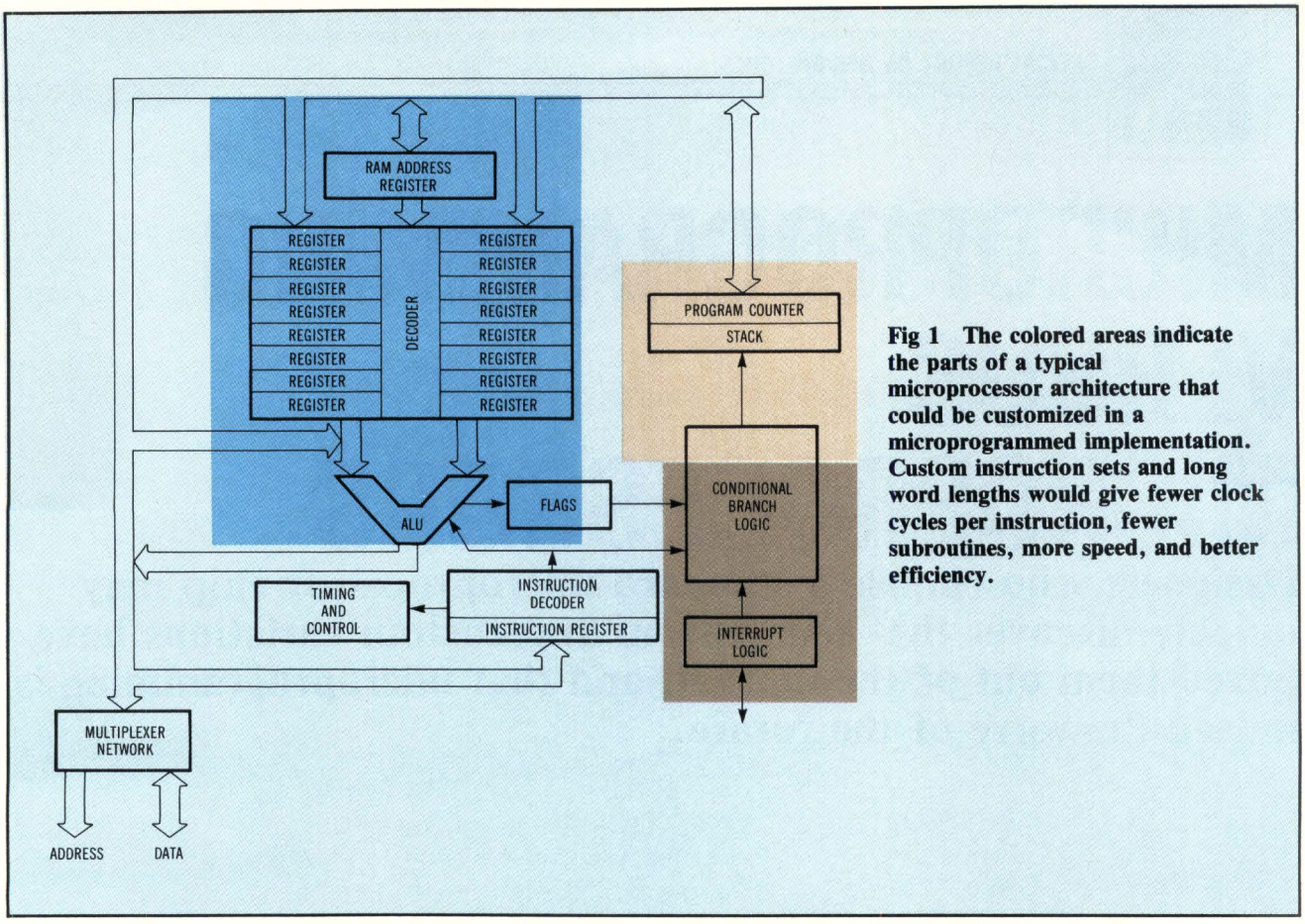


**Fig 1 The colored areas indicate the parts of a typical microprocessor architecture that could be customized in a microprogrammed implementation. Custom instruction sets and long word lengths would give fewer clock cycles per instruction, fewer subroutines, more speed, and better efficiency.**

misunderstandings that have obscured the validity of the microprogrammed approach. Some designers still believe that microprogramming is outdated, uneconomical, overly complex, or poorly supported by development tools and instruments. Many automatically turn to the off-the-shelf solution—chips that have essentially become minicomputers on silicon, with fixed architectures and instruction sets. These Von Neumann-based architectures are familiar and easy to use. Even when in ROM, the program and data reside in the same logical memory. Since these devices are so well (and permanently) defined, support software, hardware tools, application notes, and supply sources are readily available. The temptation to use them is great, requiring little or no justification to associates or management. But, it also suppresses designer creativity and can mean loss of the competitive edge, which in turn affects the bottom line.

On the other hand, microprogrammable elements actually place fewer constraints on the designer (Fig 1). The designer is free to create the instruction set that makes overall operation most efficient. The architecture (data path width) can be matched to the application (number crunching capability). When compared to a microprocessor software solution, this is not much more complex, and support tools are now readily available to make the task easier than ever. A design team with a good mixture of hardware and software expertise—working closely together from concept to project completion—can greatly reduce the problems that normally occur in integrating hardware and software. For these reasons, an examination of some popularly held beliefs (and misconceptions) about microprogramming is in order.

## Microprocessors are not always cheaper

Microprocessors are poorly structured for high speed I/O. I/O operations generally take several instructions. Each instruction takes several clock cycles, and fetching data and instructions consumes memory bandwidth. I/O also frequently calls for time-critical handshaking, something microprocessors are ill suited to handle. The microprocessor itself may be capable of handling only the simplest I/O (ie, terminals and printers). To overcome these limitations, designers often turn to special I/O processors with their own memory, to DMA, and to special interrupt handling hardware and software. Such solutions are costly, and require more logic, power, memory, and software. They are also more complex, both in hardware and software (which is likely to be excessive), making the solution inefficient as well.

Microprogrammed designs generally have enough bandwidth to allow I/O processing on demand. The I/O handler can be microcoded, for the most part, resulting in faster interrupt and I/O processing. Code and data reside in separate, high speed

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# SUPER. MICRO.

CIRCLE 95

## A short history of microprogramming

The word microprogram was first coined by M.V. Wilkes, in his paper, "The Best Way to Design a Calculating Machine." At the same time, a battle for prominence among computer thinkers was being waged between two distinguished schools: Harvard and Princeton. The winner was Princeton with the Princeton or Von Neumann machine. The Harvard machine, however, had an architecture that possessed all the elements of a microprogrammed structure. There was no clear association between the Harvard design and Wilkes's idea, but ironically, what he was suggesting would eventually allow the Princeton machine to be driven by a Harvard machine.

Microprogramming gained considerable prominence when IBM used the technique in some mid-size and small models of the 360 series mainframes, such as the 360/55. The memories used were capacitive Mylar memories, too slow for the largest mainframes. With introduction of bipolar ROMs in the 1960s and field programmable ROMS/PROMS in the early 1970s, the microprogramming technique was embraced by many of the emerging minicomputer manufacturers. Microdata Corp (Irvine, Calif) was one such pioneer. Microdata's *Microprogramming Handbook* (Microdata Corp, Santa Ana, Calif, 1971) contained what is thought to be the first reference to firmware—a term that originally meant microprogram, not microprocessor program stored in ROM or PROM.

Microprogramming became exceedingly popular in the 1970s. Random logic designs were replaced by structured and well-organized microprogram designs. During that time, some designers contended that microprogramming was slower than random logic. To some extent that was true. Microprogramming, however, offered the opportunity to incorporate higher level instruction such as string search and floating point multiply as basic machine instructions at little cost. These operations were often executed by software routines. The speed advantage of incorporating these operations in the basic instruction set was immense.

Smart controllers were a direct result of incorporating microprogramming into the I/O. Many CPU functions were offloaded by this approach, and a host of diagnostic features were added. Then, the true viable microprocessor (ie, small processor) emerged. The 8080 was crude, but it succeeded beyond almost everyone's expectations. It was random logic, but in silicon. The 8080 represented a gigantic step to those needing an affordable processor, but in a sense, it also represented a step backward in the advancement of computer science. The emergence of higher level machine instructions was abruptly halted by a crudeness which belonged in the previous decade. Its success is history, however, and the 8080 no doubt expanded computer usage.

Since the 8080, many more powerful microprocessors have emerged—the micro applies to the processor's physical size rather than to its processing power. With that, an interesting phenomenon occurred. The microprocessors became microprogrammed. The microprogram, however, resides inside the chip. And is the conceptual difference inside a chip or a PC board? Perhaps, the most significant difference is how to test and debug the board or the chip.

Custom chip design is a booming business today. Whole companies are dedicated to transforming existing boards into a single chip or implementing a new design in silicon. The emergence of custom chips as a commonplace alternative is evident. As complexity on the silicon increases, it seems only natural that most of these designs would be microprogrammed. Microprogramming offers designers the freedom to choose the optimum architecture for their applications while maintaining an orderly design structure.

memories and are fetched simultaneously. Programmable pulses and levels (pulse and level orders) can be matched to the I/O requirements, and can be handled without resorting to complicated microprocessor software. Interrupt driven, burst I/O is handled especially well by the microprogrammed or bit-slice approach.

As an example, a simple routine to send data to a universal asynchronous receiver/transmitter (UART) takes 6.6 $\mu$s (exclusive of wait loops) when coded for a 10-MHz 8086. A microprogrammed implementation for a bit-slice architecture would typically take 600 ns, given an equivalent clock rate. The speed-up (almost a full order of magnitude) has obvious advantages in time-critical applications.

Special interfaces pose similar problems because the designer usually must develop a random logic interface, matching the I/O to the chip's architecture, and much of this is done in software. The hardware interface requires more devices and more power, conflicting with modular microprocessor-based design goals and advantages. Software routines must be written in assembly language, complicating software development. The software often requires excessive overhead, which is usually solved by adding yet another microprocessor to drive the interface. This, of course, requires additional software and defeats the primary design goal of keeping things simple. Again, microprogramming is an excellent alternative. The flexibility of the microprogrammed or bit-slice solution generally leads to a smaller, simpler, and cheaper design when special interfaces are involved.

Beware of special processing, too. Microprocessor implementations usually involve development of assembly language function routines, the design of special hardware, or the introduction of coprocessors. All of these can introduce latency and slow the system down, by requiring additional registers, scratchpad RAM, etc. Microprogramming, of course, can avoid these problems.

Microprocessor designs are not always easier to implement. This is especially true if multiple processors are used to solve a problem that could be

solved by a single bit-slice processor. It is also true when the chip's instruction set does not match the task (eg, doing a fast Fourier transform with an 8086) or when special random logic must be developed. When using a microprocessor, the designer must rely on sophisticated in-circuit emulators and software tools. The tools may not be readily available, may never become available, may be limited in capability, may not operate in a general environment, and may not run in real time.

### Eliminating random logic

The microprogrammed approach is actually simpler, because the components employed are more general and more pliable. Register file structures and pulse/level order design can be closely tied to the microcode, eliminating random logic and simplifying the design. The microcode can be tailored to the architecture. New firmware development tools now give the designer all the capability (PROM emulation and sophisticated logic analysis) needed to develop the hardware and software.

Microprocessor implementations are not necessarily more advanced. LSI, state-of-the-art components are available in both microprogrammable and off-the-shelf forms. Furthermore, many popular chips were, in fact, developed with microprogramming techniques. But these standard devices are often not well suited to handle I/O processing or string processing, multiprocessing and heavy arithmetic applications. State-of-the-art chips with more sophisticated instructions and special architectures, such as stack implementations, do offer more capability, but still do not match the capability of a custom bit-slice implementation on a PC board, or in a custom VLSI device. The ability to map hardware to architecture through microcode is a great advantage, and the code resides in the densest of components, the PROM.

*Off-the-shelf solutions often grow quite complex when elements are added that require truly random logic.*

Microprogramming eliminates random logic. While it is true that part counts for such designs may be higher than a simple microprocessor-based design, random logic requirements may be no more extensive. Off-the-shelf solutions often grow quite complex when elements are added that require truly random logic to hold the system components, processors, and interfaces together. But even when the microprogrammed approach requires more components, these often function as blocks instead of as random gates. The microprogrammed approach more readily supports a top-down design methodology, yielding a cleaner solution.

Microprocessors are often selected for the more complex applications. Using a completely self-contained intelligent chip is alluring. But, now that effective development tools exist for microprogrammed devices, they should also be considered for complex applications. With the right tools, designers can microprogram a new and better generation of processors.

Microprogramming use has grown slowly but steadily since its inception. In the 1960s, for example, most computer systems were built with hardwired random logic, but by the 1970s mainframes and minicomputers were taking advantage of microprogramming's flexibility. Many of today's most popular microprocessor chips were developed with microprogramming and some, such as the TI7000, are microprogrammable to match user requirements. The industry's current hot topic is the integration of complete systems onto single silicon chips. The process of putting PC boards into silicon is taking microprogramming out of the backroom.

### Microprogramming: an old idea but not outdated

Microprogramming no longer means "computer monks," quill pens, and volumes of hand-assembled code. Today's microprogramming recruits are third-generation chip users who have witnessed several performance revolutions. They have worked with the early (primitive) chips and support tools, as well as with sophisticated development systems and computer aided engineering workstations. They have come to expect more capability in their software and hardware development tools, and if it is not available off-the-shelf, they will build their own solutions. Many already have.

This new generation of microprogrammers also has expertise that crosses two disciplines: hardware and software development. While this hybrid designer has traditionally been a rare breed, the number of engineers thoroughly familiar with both disciplines is increasing. This trend will also accelerate, as will applications for VLSI, gate-arrays, and standard cells.

Microprogramming uncomplicates things because, contrary to popular belief, it is fundamentally simple, and with the right tools, it is far easier to use than assembly language (Fig 2). If good microcode assemblers had been available 8 or 10 years ago, microprogramming would have been far more popular. Early assemblers that accompanied development systems supporting the first bit-slice products were indeed primitive. Today's macro assembler is highly structured and allows the programmer to define macros to speed up program development. Custom assemblers that allow arithmetic syntax in a way similar to that of a Fortran compiler, (with constructs that resemble those found in Pascal) can be (and have been) developed rather easily to accommodate specific tasks. It

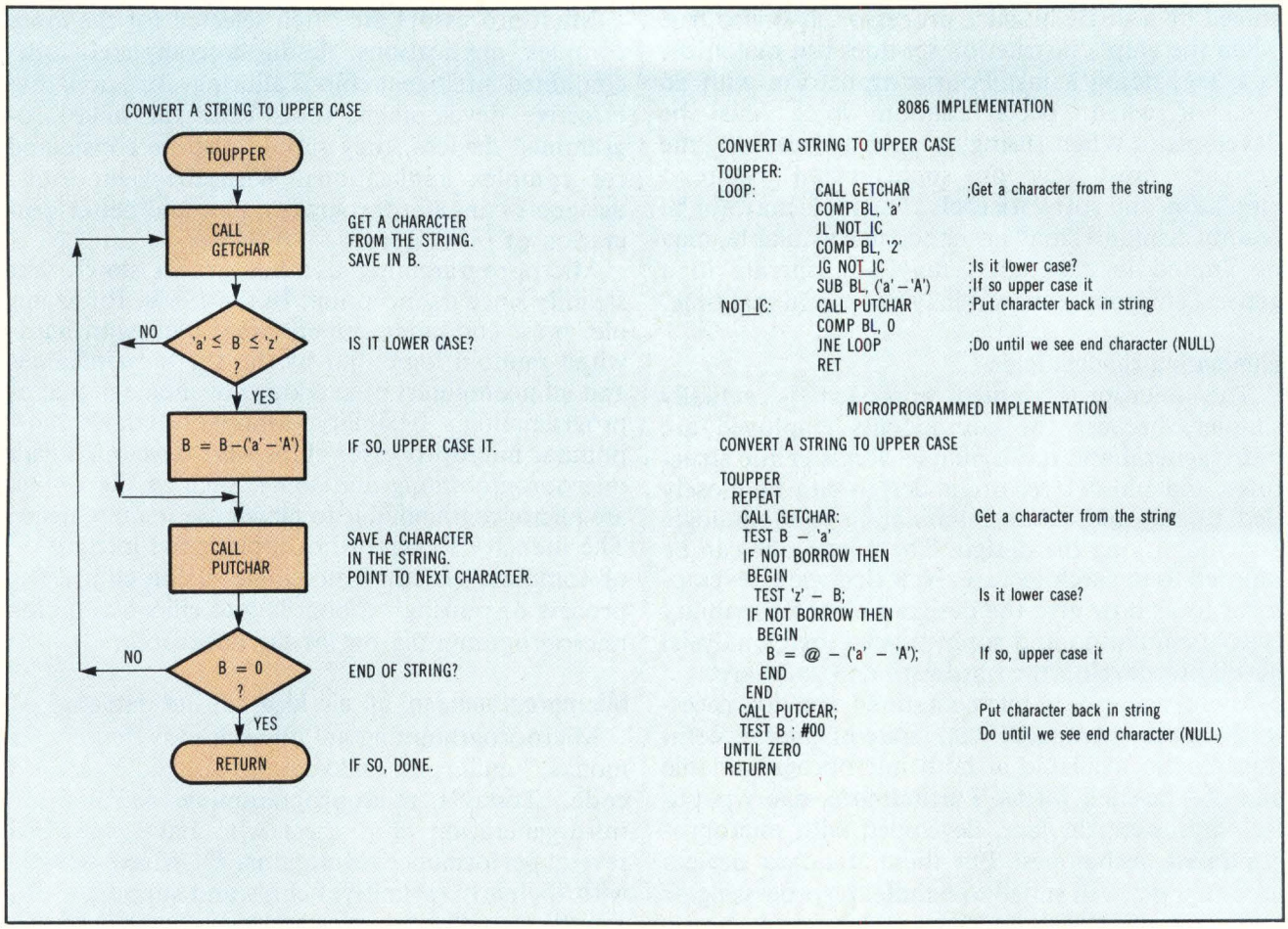


**Fig 2 Pictured is the program implementation with 8086 versus microcode. Compilers and assemblers available today take the complexity out of microprogramming. The high level like language and ability to structure the program will make it easier to follow and debug in the future.**

takes skill and creativity to design a microprogrammed structure that is powerful and yet easy to use. On the other hand, it is easy to fall into the trap of designing a structure that executes fast but takes forever to program.

## Today's firmware tools pave the way

The current crop of firmware development tools is amazingly productive and advanced. PROM emulation (writable control store) and third-generation logic analysis capabilities are combined. The incorporated features rival or exceed those available in development systems designed to support standard microprocessors. For example, a performance analysis capability is available that allows the designer to detect potential design problems, software traffic jams, and architectural inefficiencies early in the development cycle. With this feature the designer can make hardware and software trade-off decisions, and avoid costly redesign.

Multilevel triggering, up to 16 levels with 8 qualifiers each, is available in some systems, along with selective trace and selective snapshot facilities. These features allow the user to define complex patterns and events, and allow the capture of data that simple development systems might never see. Unwanted data must be filtered out, so that only meaningful information is captured for review. User-defined instruction mnemonics and alphanumeric labels are provided, to identify traced events at a glance. Parameter cross-checking minimizes errors. Histograms display buffer utilization and simplify trigger program refinements. Comprehensive display prompting, help files, and other user-accommodating features are available.

More advanced firmware development tools are on the drawing board and new entrants expected in this field will give the user an even broader range of selection in choosing support tools.

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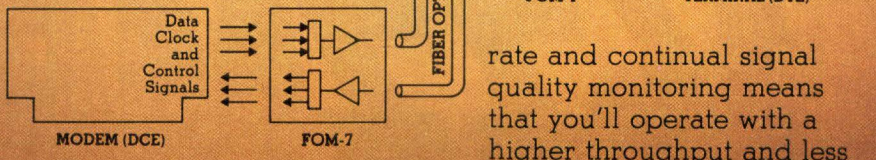


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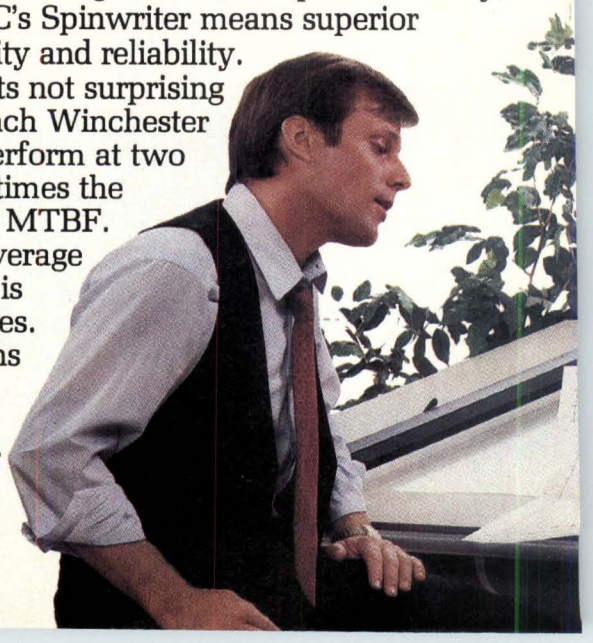

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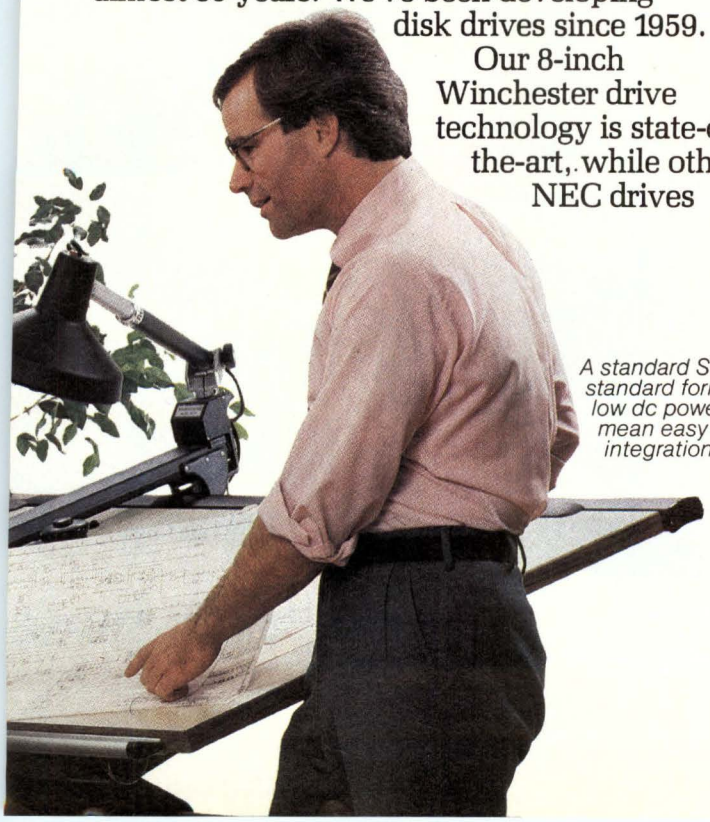

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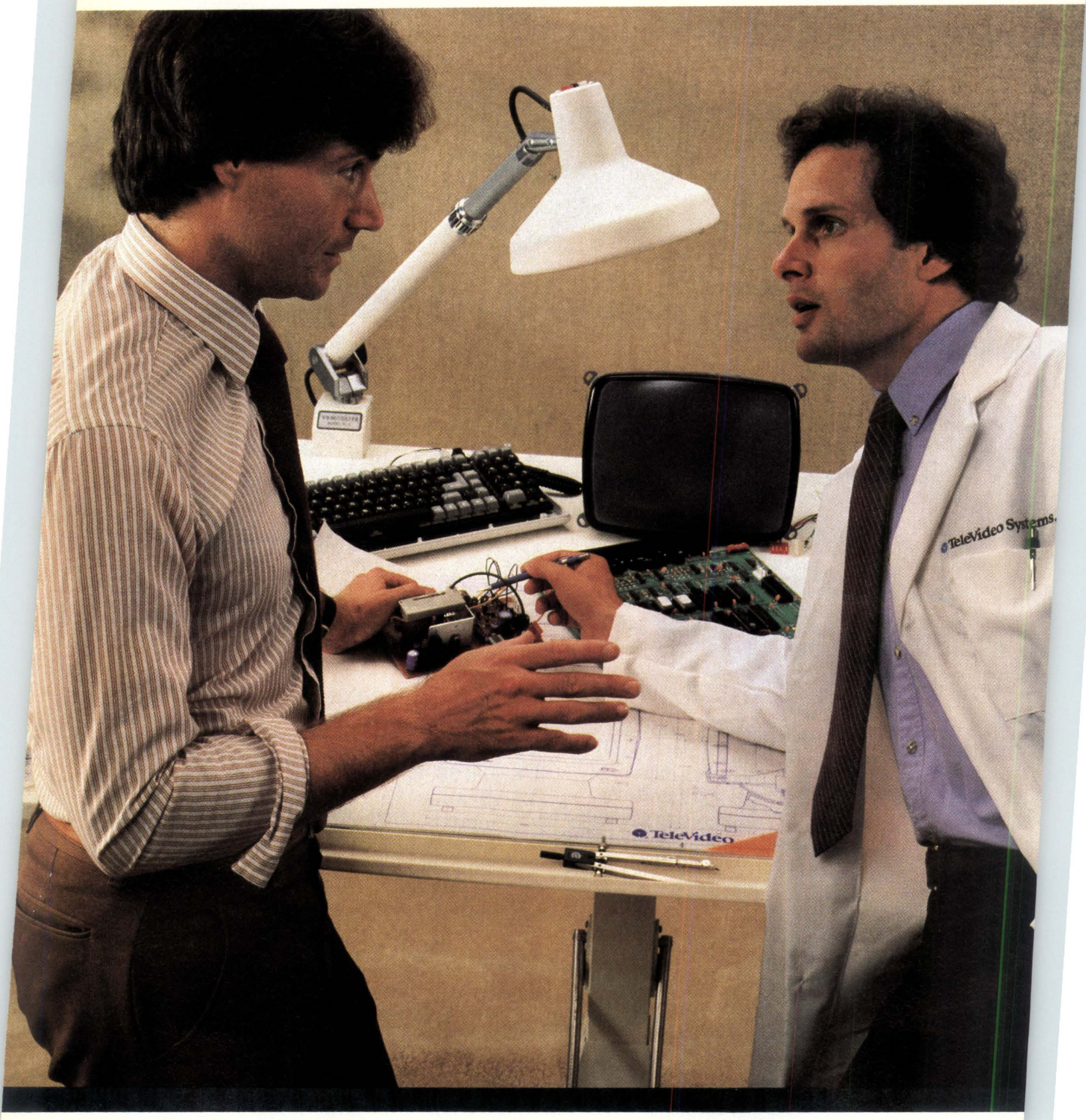
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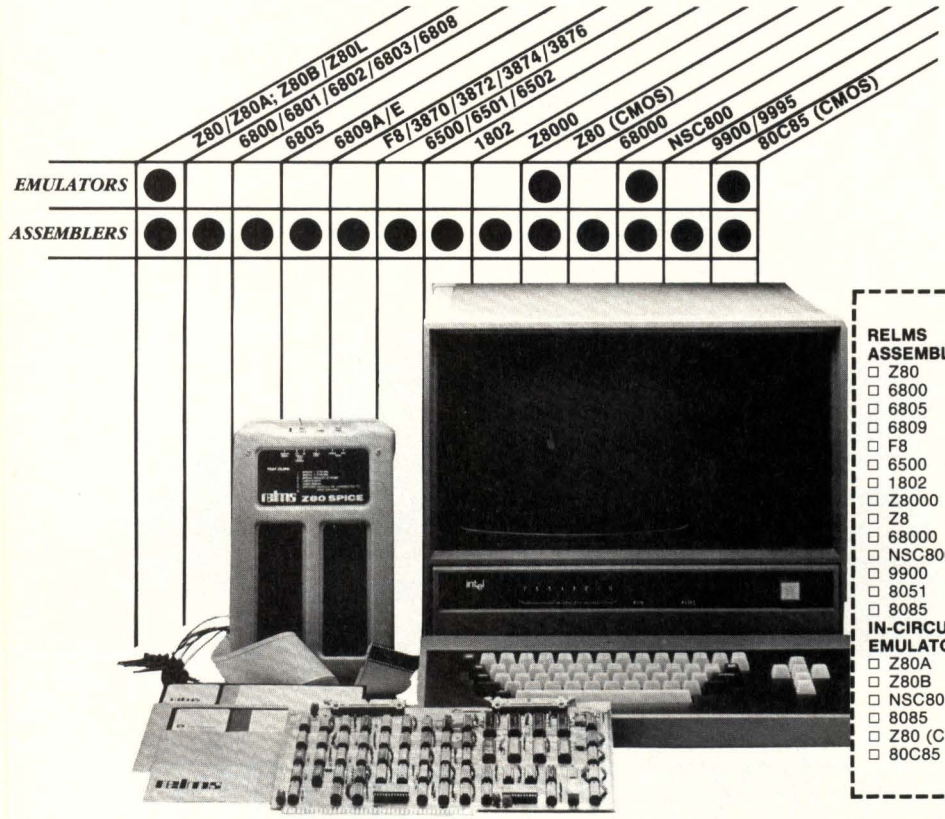


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**CIRCLE 99**

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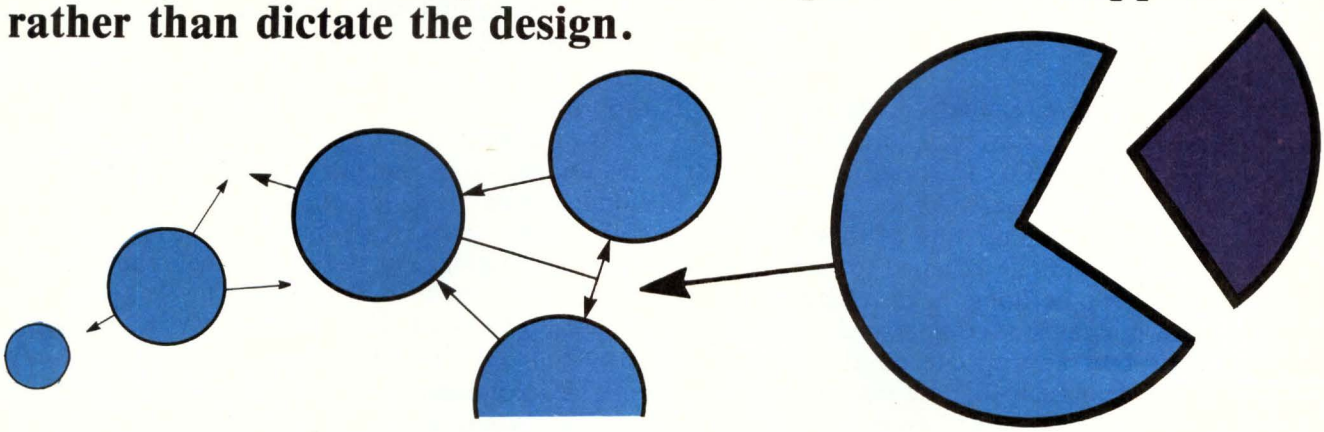

by John R. Adam

Almost no design of a microprocessor-based product takes place today without the support of a development system or the equivalent capability. Two major trends must be considered when evaluating microprocessor development methods. First, the growing number of competing systems and instruments that can be used in the design process is becoming overwhelming. Second, the use of gate arrays, standard cells and custom LSI, and the ever-increasing amount of software that needs to be developed has placed new demands on the development environment.

Beginning in the early 1970s with the Intel MDS-800, development systems have provided the software and hardware development tools to support microprocessor-based design. As development requirements have changed, so have development systems. For example, multi-user systems have kept pace with the growth in the size of development teams and powerful, universal in-circuit emulation and logic analysis have matched the requirements of the fastest 8- and 16-bit chips. High level languages have been developed to support the growing software development task.

In the last three years, the development environment has radically changed. These changes include the size and organization of the development team, significant new development procedures, and documentation and control requirements. Data bases have mushroomed, and new security methods have been installed. Traditional development systems consisting of basic desktop microcomputers and software tools with emulation and logic analysis attached, only address a subset of today's development environments. For example, the design team with responsibility for hundreds of thousands lines of code which must be written, debugged, and mated to hardware has significantly different needs from a single designer who is writing a videogame or small application program. To address the needs of the full user community,

*John R. Adam is marketing manager of Kontron Electronics, 5730 Buckingham Pkwy, Culver City, CA 90230, where he is responsible for digital instrumentation. Dr Adam holds a BS, an MS, and a PhD in electrical engineering from the University of Illinois.*

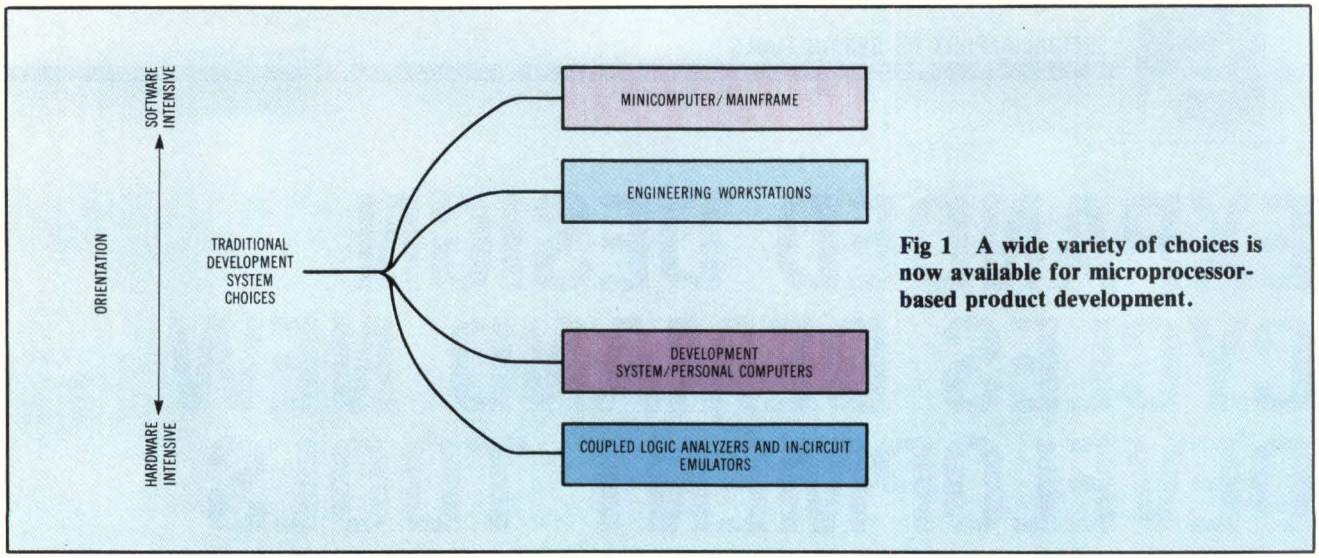


**Fig 1 A wide variety of choices is now available for microprocessor-based product development.**

development system manufacturers have therefore had to broaden their product offerings.

## Development choices

The range of development choices is shown in Fig 1. The alternatives are categorized by the size of the total effort and by the relative size of software and hardware tasks. Although all product development is really a mixture of these tasks, the time spent or individuals assigned to each effort is a key parameter in defining the development environment. For purposes of comparison, the assumption is made that appropriate development tools exist in all environments. These include languages for software development, in-circuit emulation, logic analysis, and PROM programming for hardware debugging and software/hardware integration. Furthermore, these tools must exist for the particular microprocessor being used. This is the case today for most popular 8- and 16-bit microprocessors. However, all of the required support tools may not be available from one vendor. This can create a compatibility problem that must be closely examined before a development system choice is made.

In large software-intensive projects with several simultaneous users, the development system must provide each user access to a large data base that can be partitioned by subtask. The data base must support the security and backup procedures the team adopts or the organization dictates. Since multiple program compile and assembly operations must be executed simultaneously, a large computing resource is needed. In this environment, a high performance minicomputer is the appropriate choice. While the initial investment is high, the cost per user is typically less than for a collection of individual development systems.

The demand for tools in this environment has been filled, to a large extent. This is especially true for DEC PDP-11 and VAX users. Several software suppliers, including Language Resources and Boston Systems Office, offer cross compilers and assemblers for microprocessor software development in the DEC environment. For the first approach (hardware development and hardware/software integration), two choices exist: interface a traditional development system to the minicomputer (most development system manufacturers offer utility packages for this purpose), or eliminate the development system and mate the in-circuit emulator directly to the mini. This lets any user access an emulator directly from a VT102 terminal. Kontron and Tektronix offer such systems.

The second approach is development of an engineering workstation. Workstations provide gate array, standard cell, custom LSI, and PC board computer aided design (CAD); microprocessor-oriented software and hardware features; word processing; and when networked, electronic mail project control, and documentation capability. Still in its infancy, the workstation approach is intended to provide a full turnkey solution to the development effort. The adoption of standard operating systems, such as Bell Labs' Unix, and networking schemes will relieve the user from matching incompatible systems and tools.

The third approach is a collection of individual, traditional development systems. Such a configuration is directed toward projects with an equal mix of software and hardware tasks. Since development systems have integrated software and hardware development tools, individual users can switch between them readily. This environment is appropriate for a group of contributors or for a project that can be partitioned into clearly defined subtasks. While most development systems support some form of networking scheme, they do not provide the software management functions associated with minicomputers or workstations.

An offshoot of this third approach is to substitute an inexpensive personal computer for the

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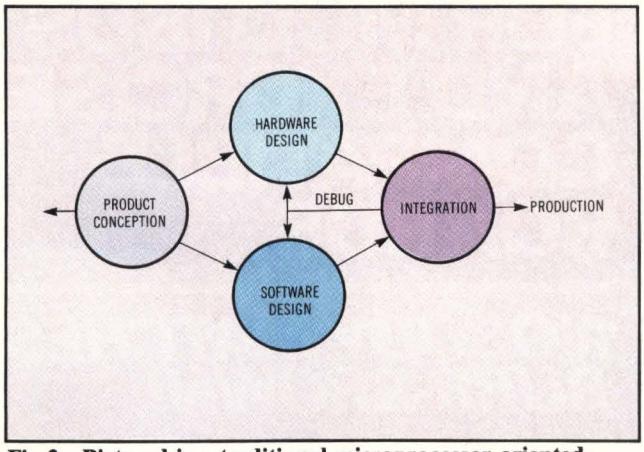


**Fig 2 Pictured is a traditional microprocessor-oriented design cycle with separate hardware and software functions.**

microcomputer used in traditional development systems. This approach is attractive because of the low cost, adequate performance, and availability of personal computers; and the wide range of non-development software available, such as word processing packages that support the development effort. Complete sets of professional quality microprocessor-oriented development tools for personal computers have yet to emerge. Some tools are available, such as software development tools from RTCS Corp, logic analysis packages from Northwest Instruments, and semicustom design software from FutureNet.

The fourth choice, coupled instrumentation, is most useful in hardware-intensive environments with limited software development requirements such as hardware development labs, prototype or limited production operations, or repair centers. This approach is based on closely coupled logic analysis and in-circuit emulation. The in-circuit emulator is used to control data capture by the logic analyzer. The results of the data capture are then wed to control program execution. The Dolch Atlas and Kontron Laser systems are examples of this type of system.

## Changing design cycles

The design process of the last 10 years can be represented by the cycle shown in Fig 2. In the product conception phase, features and capabilities are determined and enumerated in a specification. The features are then partitioned into hardware and software tasks. Individual tasks in each area are defined and completed independently. When the tasks are completed, they are integrated to produce the final result. If problems are discovered, the software and hardware are modified and the integration continued until a functional prototype is obtained.

As the typical design has become more complex, the development cycle has expanded to that shown in Fig 3. In the concept phase, along with the functional ability of the product, a detailed analysis of the available software and hardware development approaches can be made.

It is assumed that a standard microprocessor is at the heart of these designs. In the foreseeable future, microprocessors will be the major controlling element in the design cycle. This will hold true due to the mass of software currently available and the ease of writing new software. Indeed, the trend is toward multiple microprocessors with tasks partitioned among them.

Developers must answer hard questions. Can the software be partitioned into a kernel that handles all of the hardware-dependent functions? Should this

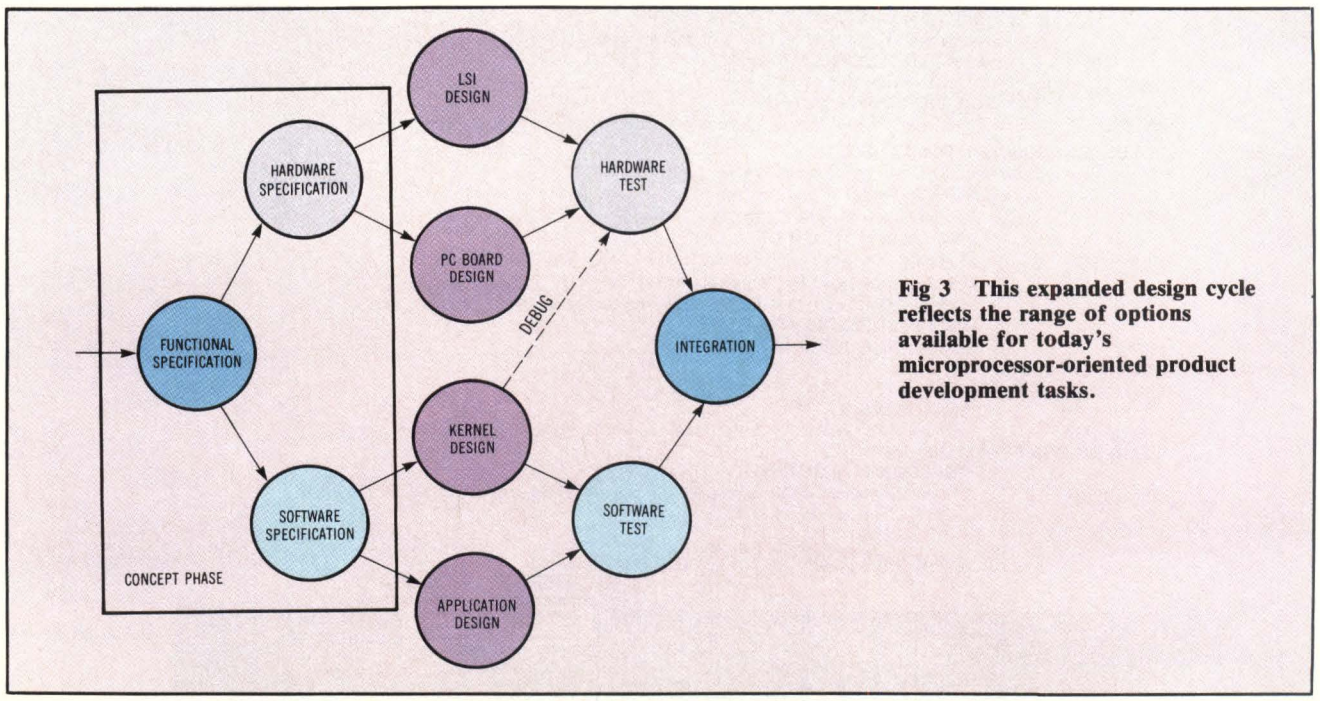


**Fig 3 This expanded design cycle reflects the range of options available for today's microprocessor-oriented product development tasks.**

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**Fig 4 Kontron's team workstation combines microprocessor software and hardware development with PC board layout and gate array design.**

be a standard operating system kernel? Can the application software, which controls the product's functional ability, be separated? If it can, this relieves the design engineer from the task of knowing the hardware implementation details, since calls to the kernel handle this task. Separation also allows the application to be written in a high level language. The application can be debugged independent of the hardware and easily modified to produce multiple versions customized to specific uses or markets.

At the hardware concept level, similar issues exist. For speed, product protection, or other reasons, there is a question as to whether or not custom components should be used. There are a wide range of choices including gate arrays, standard cells, and semi- or custom-LSI. The PC board must be designed and laid out. The combination of the custom LSI, the PC board, and the operating software kernel must be tested. The combination of the completed software and hardware are then integrated to produce a complete prototype. As an auxiliary output from the design process, manufacturing and service documentation and test procedures are also to be generated.

This design cycle expansion demands a new generation of electronic design workstations. They must incorporate the software and hardware development capabilities and instrumentation associated with traditional development systems plus the graphics handling, auto-routing, and layout capabilities of CAD systems.

The first product to address this new design cycle is the Kontron KDS 980 team workstation shown in Fig 4. This system offers both microprocessor-oriented software and hardware development tools and CAD features in one distributed processing, multi-user configuration. This arrangement, in addition to supporting the major design cycle elements, provides a large shared data base and features such as electronic mail.

Simulation is the one major element missing in this design cycle. Rudimentary simulation of a gate array or PC board can be performed today. The goal however, is to be able to simulate a complete product. This includes not only the hardware portion but the hardware-dependent software kernel. This type of simulation will, if not eliminate, at least drastically reduce troubleshooting during the prototype phase. Such simulation capability should be available on development workstations in the near future.

The design environment, type and size of tasks, changing technology, and organizational characteristics all play a role in determining the type of microprocessor-oriented development tools that are most appropriate. The choices range from minicomputer-based systems to standalone instruments. To determine which is most appropriate for individual design needs, all of these factors must be considered.

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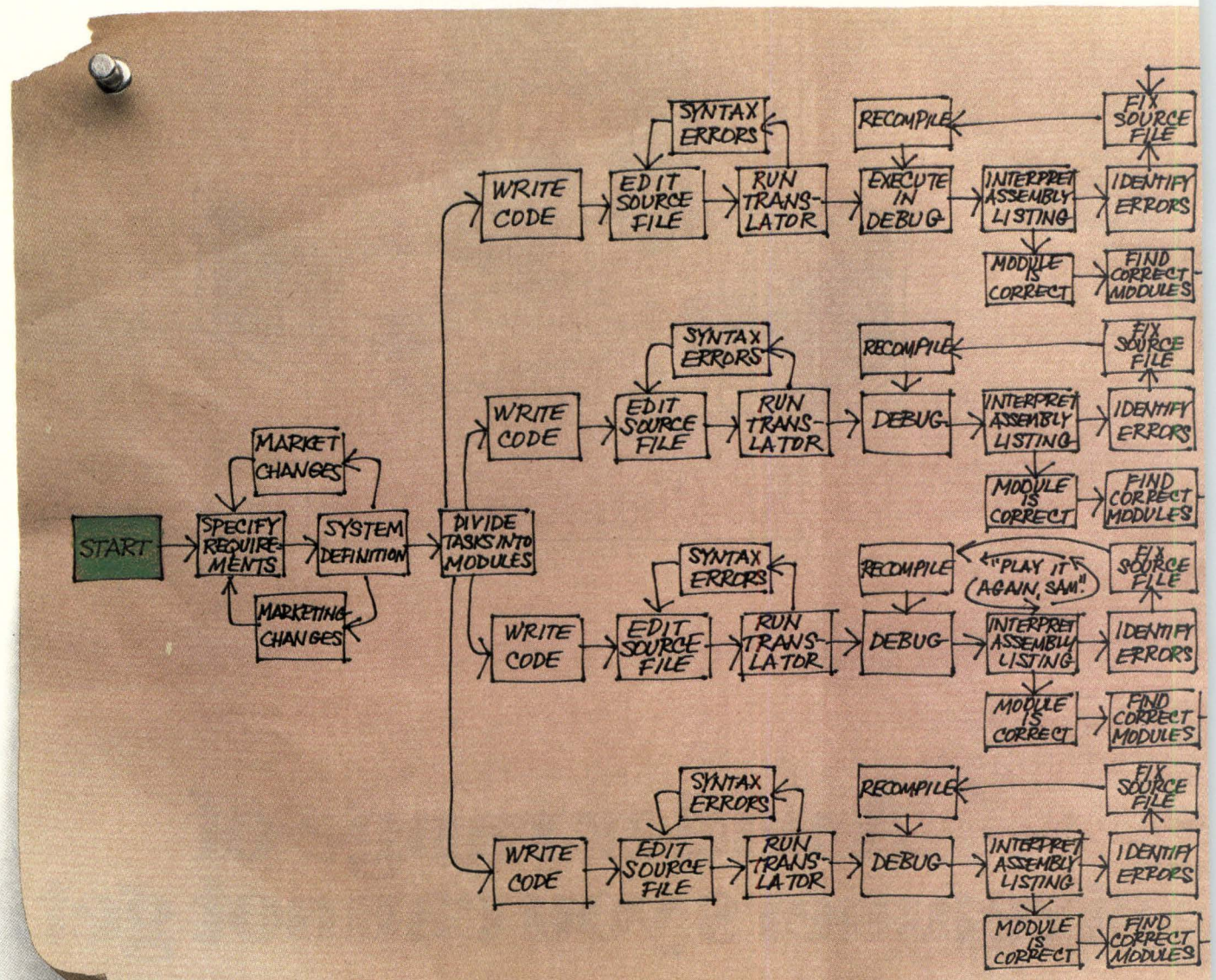


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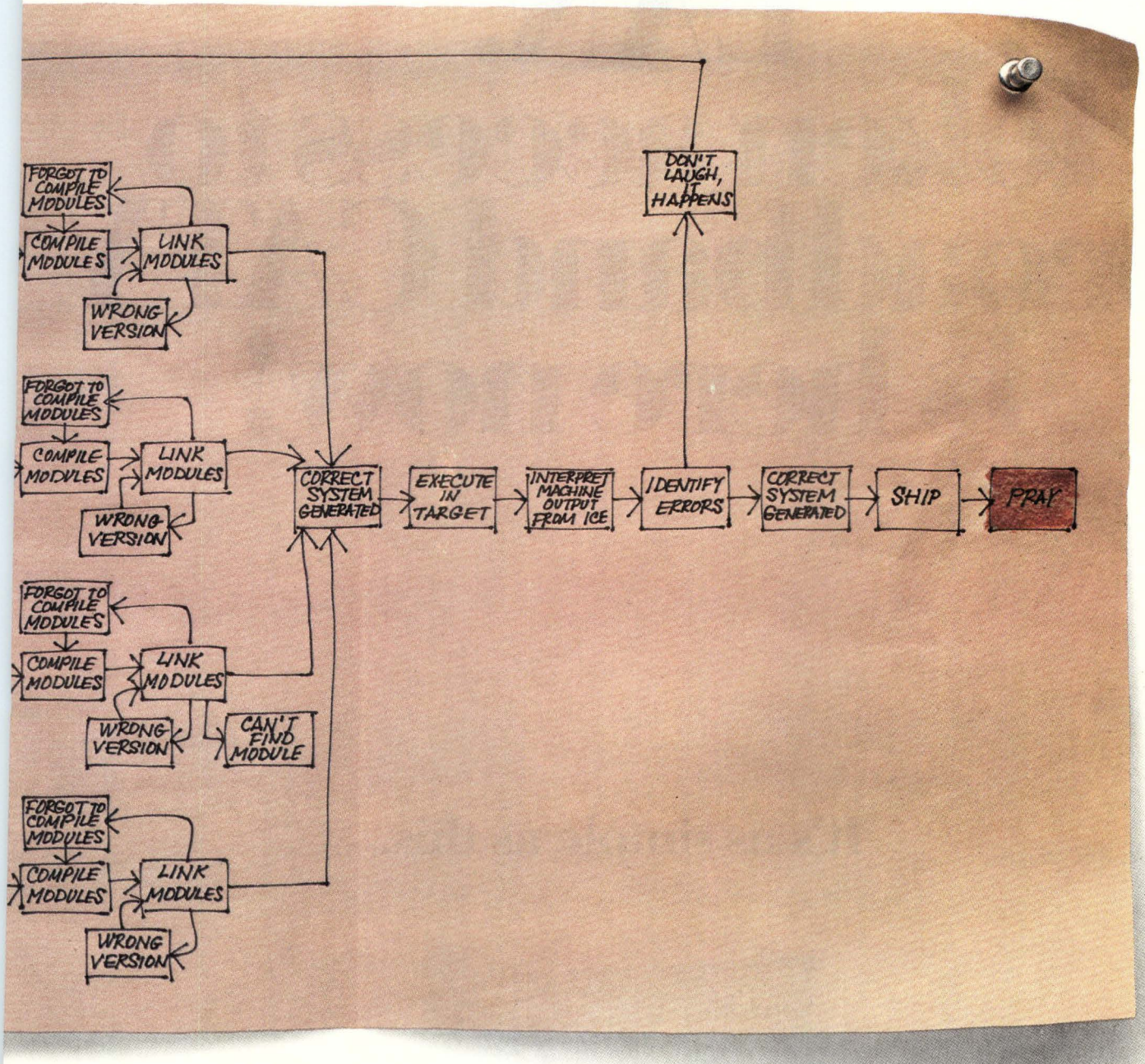


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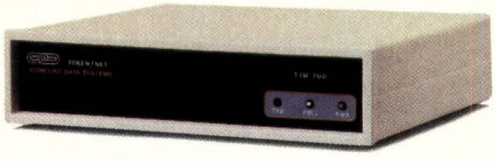

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**CIRCLE 104**

# SIMPLIFY PROGRAMMING OF REALTIME SYSTEMS

**Designers need development tools to test and interactively refine realtime applications. A tool for testing a routine in a high level language and then compiling it into a compact ROMable form is very valuable.**

**by Evan Solley**

Realtime programs have a unique set of requirements and constraints that set them apart from other software engineering tasks. Producing error-free code is difficult for two reasons: the need to deal explicitly with time constraints, and the need to deal with hardware at a very primitive level. Moreover, most standard programming languages offer little help in these areas. Realtime facilities are usually extensions to a language provided by either a specific vendor or the application engineer.

A tool for building realtime programs should be a complete programming environment designed specifically for microprocessor-based realtime applications. It must combine features usually distributed among high and low level language translators, realtime operating systems, and support tools such as editors, linkers, and debuggers. It must also produce fast-executing compiled code when testing is complete. In addition, when the software is developed and tested on the target system, there can be no discrepancies, as with cross-development techniques, between the development and the target environments.

*Evan L. Solley is president of Infosphere, Inc, 4730 SW Macadam Ave, Portland, OR 97201. He has studied design and organization science at Roger Williams College, and has participated in the system science program at Portland State University.*

Timing dependencies, imposed by external hardware or physical processes, present a major challenge in realtime programs. The need for raw speed is one example. A realtime program gets input from a device or process, and generates a controlling response. The program must be fast enough to perform calculations and make decisions in time to guarantee stability, which may be only a few milliseconds.

To ensure the necessary response, Infosphere's programming tool, Sphere, is a threaded-code language similar to Forth. Complex functions are built up from the predefined primitives provided in the Sphere nucleus. Primitives are coded in assembly language, while composite (user-defined) operators are compiled as address lists that point directly to the component primitives. The result is a compact code that executes at compiler speeds, while providing a mechanism for interactivity. The system can also operate in an interpretive mode in which new definitions are added to a dictionary and incrementally compiled. Once defined, the target system can immediately execute the new operators to run at full compiled speed.

In addition to Forth's speed, the programming system provides the clarity of Pascal with the classic block control structures: IF-THEN-ELSE, REPEAT-UNTIL, CASE, and DO-LOOPs. Table 1 is an example of how to define and use operators. The system uses postfix (reverse polish) notation, to simplify the language syntax and minimize the complexity of token parsing. Arguments are passed on a dedicated parameter stack, making all

**TABLE 1**

**Sphere Code Example**

```
  > % Sphere code:                    Pseudocode comments:
  > HEX                               % set hexadecimal radix
  > 1        'ENABLE  CONST           % define constants
  > 0        'DISABLE CONST           %
  > OFFFF    'POS     CONST           %
  > 0        'NEG     CONST           %
  >                                   %
  >                                   %
  > 'START   :                        % start motor:
1 >     ENABLE DRIVE !                % drive  := enable
1 >     10 1 DO                       % for i=1 to 10 do
2 >         I 30 * OUTPUT !           %   output := 30*i
2 >         2 SLEEP                   %   delay 2 system ticks
2 >     LOOP ;                        % end
  >                                   %
  >                                   %
  > 'STOP    :                        % stop motor:
1 >     10 1 DO                       % for i=1 to 10 do
2 >         10 I - 30 * OUTPUT !      %   output := (10-i)*30
2 >         2 SLEEP                   % delay 2 system ticks
2 >     LOOP                          % end
1 >     DISABLE DRIVE ! ;             % drive := disable
  >                                   %
  >                                   %
  > 'SET SPEED   :                    % set speed:
1 >     MOTION @                      % get MOTION value
1 >     CASE                          % case MOTION of
2 >         -1 { STOP }               %   -1: stop
2 >          0 { }                    %    0: do nothing
2 >          1 { START }              %    1: start
2 >     END ;                         % end
  >                                   %
  >                                   %
  > 'SET DIRECTION   :                % set motor direction:
1 >     MOTOR @ GTZ                   % test MOTOR
1 >     IFT                           % if  0
2 >         DIRECTION POS !           %   direction  := pos
2 >     ELSE                          % else
2 >         DIRECTION NEG !           %   direction  := neg
2 >     ENDIF ;                       % end
  >                                   %
  >                                   %
  > 'MOTOR_CONTROL   :                % main operator:
1 >     REPEAT                        % repeat
2 >         SET_DIRECTION             %   set direction
2 >         SET_ SPEED                %   set speed
2 >     FOREVER ;                     % forever
  >                                   %
```

operators reentrant. This is important in a multitasking environment, where several concurrent tasks may use a given operator.

In Table 1, several operators are defined using primitives. The system indicates the nesting level within definitions and block structures to the left of the prompt character (>). First, the START operator enables a motor drive, then outputs a set of 10 values—one every two system clock ticks—to control motor speed. The effect is to ramp the motor up to speed.

The STOP operator does just the reverse. Based on the value of a variable called MOTION, the SET_SPEED operator determines whether to call START or STOP (or do nothing). The SET_DIRECTION operator tests a variable called MOTOR to determine what to write to the motor direction control register. Finally, MOTOR_CONTROL, the main operator and an infinite loop, calls the other operators to control motor direction and speed.

Two other aspects of timing dependencies are closely related: responding to asynchronous external events and multitasking. Realtime problems require a program to respond quickly to external events, which are essentially random with respect to the program sequence. Event-driven programs take their action cues from the external system.

A program can sense external events through polling, but most systems use hardware interrupts to alert the program about an event, and to pass control directly to an associated routine. Facilities deal with interrupts directly in high level language, and the context is saved and restored automatically. The programmer does not need assembly code interrupt service routines or special software interfaces to incorporate interrupts into the application. This saves time, and enhances program portability, since no processor-specific code is required.

## Multitasking facilities

The problem of maintaining the logical flow of program segments that deal with various external events becomes manageable if it can be broken into independent tasks that focus on various components of the problem. These tasks execute concurrently on the target processor, corresponding to the multiple physical (or electrical) processes that the program must deal with. However, multiple tasks require a special routine, called a multitasking executive, to handle execution of the tasks. This allows tasks to communicate in a coordinated manner, and gives them access to the processor and other resources.

Traditionally, the programmer had two ways to provide multitasking in an application: to incorporate a large multitasking operating system into the target; or to write a special purpose multitasking executive. An integral multitasking executive is part of the sphere runtime nucleus that allows the programmer to create and run as many tasks as needed. Since the entire runtime system fits into 16 Kbytes (two 64-K or one 128-K ROM), the memory required to support multitasking is minimal.

The scheduler manages processor resources according to a preemptive scheduling algorithm that has been assigned a priority. When an interrupt or a signal from another task occurs, the scheduler searches a list of ready tasks and starts the one with the highest priority. It will even replace the previously running task if necessary. If all eligible tasks have the same priority, the scheduler defaults to a round robin order. Tasks can be defined, started, stopped, and their priority can be modified dynamically through task control operators that are directly accessible from high level constructs.

Communication or synchronization between tasks is also done directly in high level language with a formal signaling mechanism called a significant event. Tasks send and receive information through this memory location. While operators

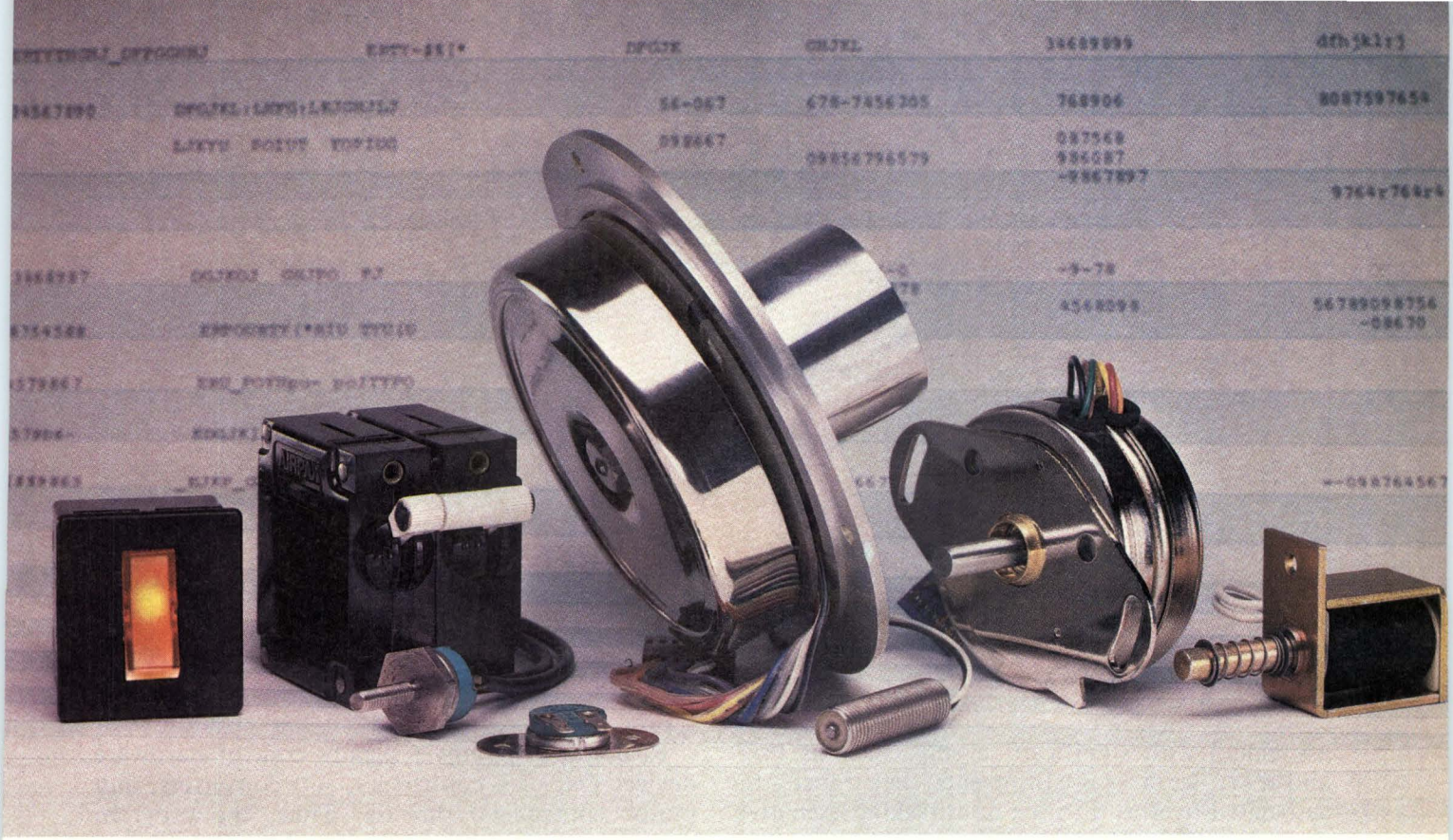

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**TABLE 2**

**ISRs and Significant Events**

```
  > % ADC Interrupt Service Routine
  > 'READ_ADC :                                  % define ISR operator
1 >       ADC_Loc @ ADC_EVENT !                  % read ADC, store in event cell
1 >       ADC_EVENT POST                         % POST event
1 >       ;                                      % end definition READ_ADC
  >                                              %
  >                                              %
  > 'READ_ADC 'ADC_ISR ISR                       % declare ISR called AC_ISR
  >                                              %
  >                                              %
  > %Display Task                                %
  >                                              %
  >                                              %
  > 'DISPLAY :                                   % define task operator
1 >       REPEAT                                 % repeat
2 >           0 ADC_EVENT WAIT =                 %       wait, display
2 >           ADC_EVENT 0!                       %       clear event
2 >       FOREVER                                % forever
1 >       ;                                      % end definition DISPLAY
  >                                              %
  >                                              %
  > 10. 20. 20. 'DISPLAY D_TASK TASK             % define display task
  >                                              %
```

associated with significant events, such as POST and WAIT, let tasks use the events, they transfer the associated overhead to the multitasking executive. A task waiting for a specified event to occur is suspended and imposes no load on the system.

Another task or interrupt service routine can signal an event (receipt of a character, end of a sector search, closing of a solenoid, etc) with the POST operator. POST causes a search of the list of WAITing tasks, to see if any are waiting for that event. If so, they are activated when they have the highest priority. Table 2 shows an interrupt service routine and a task communicating, using significant events. The interrupt routine operator, READ ADC, gets a value from an A-D converter channel, stores it in a significant event cell, and then posts the event. The display task, D TASK, is suspended while it waits for the event to occur. When ADC EVENT is posted, D TASK awakens, displays the ADC value, and clears the event cell.

Realtime programs typically control hardware devices (eg, disk controllers, A-D converters, and motor controllers) directly. Thus, the program must be able to address hardware ports and interpret and manipulate individual bits in a device control word. Bits can be tested, modified, shifted, and rotated directly in high level language. Hardware ports at explicit locations can be given symbolic names for convenience. Special operators control initialization, the enabling and disabling of interrupts, and interfacing a system clock.

## Realtime data structures

Common predefined data types include constants, scalars (both static and dynamic), and vectors. Realtime programmers find certain complex data types useful because they occur in many realtime applications. However, programmers must spend a great deal of time coding and debugging, using the basic constructs of a language. In Sphere, these

**TABLE 3**

**FIFOs and LIFOs**

```
> ADV                                  % invoke ADV vocabulary
> HEX                                  % set hexadecimal radix
> 64 'INBUFFER FIFO                    % defines a 64 element FIFO buffer
> 25 TO INBUFFER = 64                  % 64 cells left, value 25 to FIFO
> 50 TO INBUFFER = 63                  % 63 cells left, value 50 to FIFO
> 75 TO INBUFFER = 62                  % 62 cells left, value 75 to FIFO
> INBUFFER = = 3 25                    % 3 cells occupied, get value 25
> INBUFFER = = 2 50                    % 2 cells occupied, get value 50
> INBUFFER = = 1 75                    % 1 cell occupied, get value 75
> INBUFFER = 0                         % no cells occupied
>                                      %
>                                      %
> 24 'TEMPSTACK LIFO                   % defines stack 24 cells deep
> 10 TO TEMPSTACK = 24                 % 24 cells left, 10 on LIFO
> 20 TO TEMPSTACK = 23                 % 23 cells left, 20 on LIFO
> TEMPSTACK = 2 20                     % 2 cells remaining, returns 20
> TEMPSTACK = 1 10                     % 1 cell remaining, returns 10
```

structures—first in, first outs (FIFOs), last in, first outs (LIFOs), and logic device emulators—are predefined. Thus, the programmer has a ready-made set of data objects that fit the realtime environment.

FIFO queues are useful for I/O data buffering, especially between interrupt service routines and modules receiving data (Table 3). They can isolate the timing dependencies between device drivers and high program layers. LIFO stacks are used within modules to provide a local, dynamically allocated data structure for temporary storage workspace. This is an effective way to allocate additional working space, because routines remain reentrant and are therefore available to multiple concurrent tasks. Space allocation and pointer manipulation are managed transparently through associated operators.

Logic device emulator operators allow programmable logic arrays (PLAs) and programmable logic sequencers (PLSs)—finite state machines—to be emulated in software. This is useful for coding algorithms expressed in state machine notation, such as device controllers. Conversion to code is straightforward and results in a compact table driven procedure. Fig 1(a) shows a very simple PLS for a motor controller. The input to the controller is a 2-bit field, where D0 is a STOP (0) or a GO (1) command, and D1 is a phase lock (1 = locked) indicator. The state diagram shows the transitions for the controller based on the input bits. The controller is phase locked when the motor is at a constant velocity, but loses lock when the speed changes. Controller hardware requires a unique

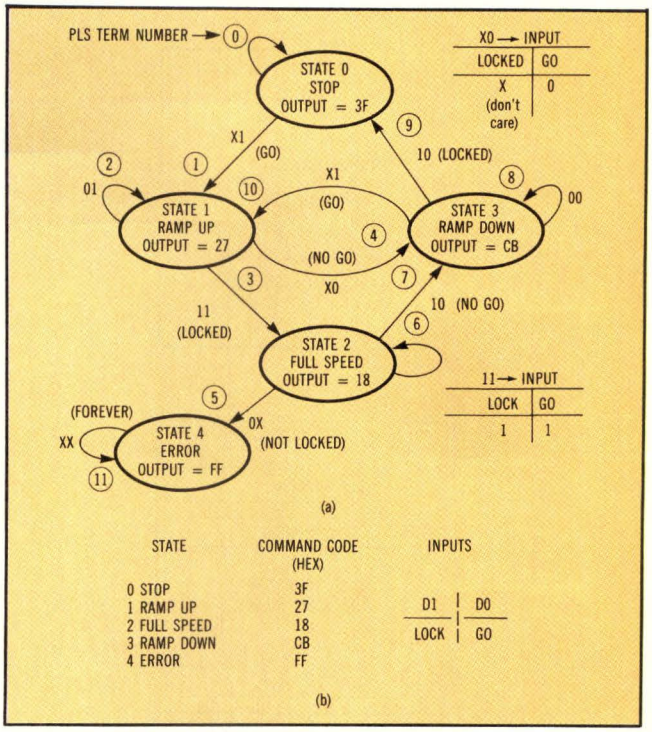


**Fig 1 This state diagram (a) describes the possible actions of a software motor controller and the possible inputs (b) that control the changes of the state.**

**TABLE 4**

**State Programmable Logic Sequence**

```
> % Argument order for PLS:
> %   S1 term number (top of stack)
> %   S2 input mask
> %   S3 input pattern
> %   S4 state mask
> %   S5 state pattern
> %   S6 next state
> %   S7 output
> ADV                          % invoke ADV vocabulary
> HEX                          % set hex radix
> 11. 'CONTROL PLS             % define PLS
> %
>  % Output  Next  State  Smask  Input  Imask  Term    TO PLS
>     3F      0      0     0FF     0      1     0.     TO CONTROL
>     3F      1      0     0FF     1      1     1.     TO CONTROL
>     27      1      1     0FF     1      3     2.     TO CONTROL
>     27      2      1     0FF     3      3     3.     TO CONTROL
>     27      3      1     0FF     0      1     4.     TO CONTROL
>     18      4      2     0FF     0      2     5.     TO CONTROL
>     18      2      2     0FF     3      3     6.     TO CONTROL
>     18      3      2     0FF     2      3     7.     TO CONTROL
>     0CB     3      3     0FF     0      3     8.     TO CONTROL
>     0CB     0      3     0FF     2      3     9.     TO CONTROL
>     0CB     1      3     0FF     1      1     10.    TO CONTROL
>     0FF     4      4     0FF     0      0     11.    TO CONTROL
>
>
>   'EXECUTE:
>       REPEAT                                        % repeat
>           STATUS @ CONTROL CREG !                   %     CREG := CONTROL (STATUS)
>       FOREVER                                       % forever
>           ;
```

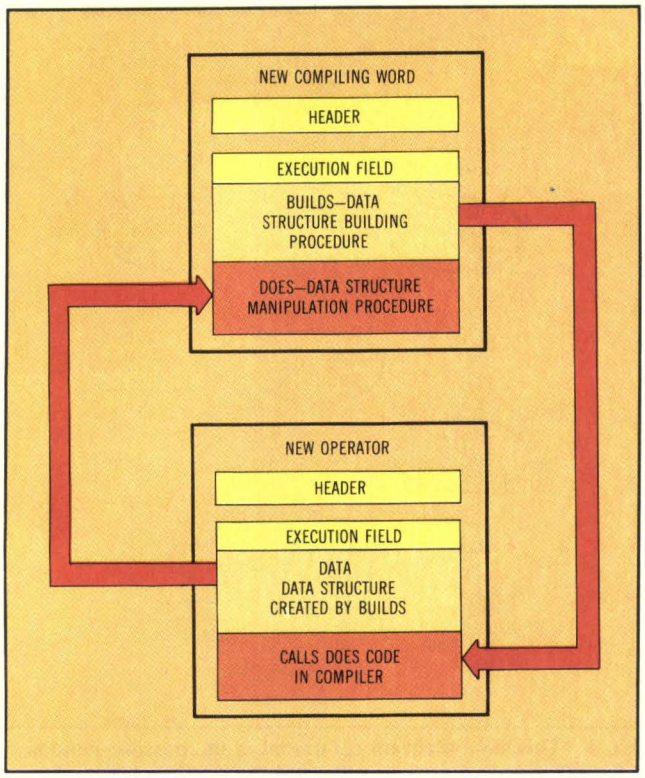


**Fig 2 In building a new type of operator, a new compiling word is created using the BUILDS . . . DOES primitive. When an instance of the new operator is created, it calls the BUILDS part of the compiling word to define data structures. When it is executed, it calls the DOES part to manipulate the data.**

command code for each possible state. An error occurs if the controller loses phase lock at an inappropriate time.

In Table 4, the contents of the PLS, named CONTROL, are listed as the following: the term number, an input mask, the current input, a state mask, the current state, the next state, and the current output. The CONTROL PLS is used in the EXECUTE operator of Table 4. The motor status is read from a variable, STATUS, and becomes the input to CONTROL. The PLS searches the definition table for a matching input (after applying the input mask) and current state. When a match is found, the corresponding output is returned, and the PLS steps to the corresponding next state in the table.

## Extensibility through meta-compiling

As previously mentioned, new operators and data structures are added by using the defining operators. Another level of extensibility that allows an operator to define entirely new classes of objects beyond those provided with the basic system is also available. This is possible because, unlike most languages that use a single compiler with a predefined feature set, Sphere is composed of a large number of very small, special purpose compilers (compiling words). There is one for each data type, in addition to the construct that defines new operators.

Some languages, Pascal and PL/I in particular, allow new data types to be added to make the language better fit the application. As with other procedures, these procedures associated with the new data structures are coded and distinct from the data structures. Sphere extends the notion by encapsulating both the data structure and managing procedures within a data object. Once created (by defining a new compiling word), new instances of the data object can be created at will, with the internal details completely hidden from the calling modules. The only access to the data structure is through the defined object interface.

New compiling words (and therefore new data objects) are created with the BUILDS...DOES

**TABLE 5**

**Defining the Bitset Data Object**

```
> 'BITSET : BUILDS                                  % builds data structure
>                 2 VAR+                            % allocates one cell (2 bytes)
>                   D                               % places address in dictionary
>       DOES                                        % execution behavior
>           @ MODE @                                % celladdr mode
>       CASE                                        % mode = ?
>           4 {  1 ROT ROTATE NOT SWAP ANDW  }      % clear bit
>           5 {  1 ROT ROTATE SWAP ORW  }           % set bit
>           6 {  RADIX @ SWAP BIN ? RADIX !  }      % display cell
>           7 {  1 ROT ROTATE SWAP @ AND            % test bit and
>              NEZ                                  % print
>              IFT "  TRUE"                         %  "true" or
>              ELSE "  FALSE"                       %  "false"
>              ENDIF  }                             %
>         END MODE 0!       ;                       % reset mode
>                                                   % and exit
> % Defining an Instance of BITSET
>
> 'FLAG BITSET                          %  create a bitset called FLAG
> 'SET          : 5 MODE ! ;            %  assign modes as operators
> 'CLEAR        : 4 MODE ! ;
> 'EXAM         : 6 MODE ! ;
> 'TEST         : 7 MODE ! ;
```

construct (Fig 2). This defines a new compiling word in two parts. The first part, BUILDS, defines the characteristics of the data structure(s) created each time the new compiling word is invoked. Since BUILDS is actually a compiled operator that executes separately, it can receive arguments that modify the characteristics of data structure instance. For example, an argument of a new compiling word that creates a two-dimensional vector can specify the number of elements in the new vector.

**TABLE 6**

**Using the Flag Bitset**

```
> ET 7 FLAG SET 2 FLAG SET 4 FLAG      % set bits 7, 2 and 4
> EXAM FLAG 10010100                   % examine FLAG
> CLEAR 4 FLAG EXAM FLAG 10000100      % clear bit 4, examine
> TEST 4 FLAG FALSE                    % test bit 4
> TEST 7 FLAG TRUE                     % test bit 7
>                                      %
>                                      %
> 3 'DRIVENB CONST                     % define constants
> 5 'DIRSENS CONST                     %
>                                      %
>                                      %
> SET DRIVENB FLAG                     % set drive enable bit
> TEST DIRSENS FLAG FALSE              % test direction sense
```

The DOES part of the structure specifies actions performed by the objects that are created by the new compiling word. This is the procedural part of the data object. For example, a two-dimensional vector so created might return the address (or contents) of element (i,j) when the arguments i and j are provided. The DOES part of the compiler definition specifies the procedure that uses i and j to look up the appropriate matrix element. DOES specification procedures can incorporate elaborate features (out-of-bounds checking, scalar, or matrix multiplication, etc). As a result, the programmer can customize the system to create an application-specific language.

### Meta-compilers build complex data objects

A common data structure in realtime programs is the 1-bit flag. There are usually many in a program to keep track of various operating states, or to control external devices through control registers. Although a single-bit (instead of a byte or word) requires more overhead, it is preferred in small applications because RAM space is very precious (eg, in single-chip controllers like the 8051).

To use single-bit flags, the programmer must either deal with locations and bit masks explicitly, or create a special routine to manipulate flags and a data structure to associate locations and masks with each symbolic flag reference. The first approach is awkward and prone to error. The second requires constant maintenance of the flag definition data structure as the various flags are added, deleted, or moved.

Meta-compiling allows the programmer to define a new compiling word that automatically creates and manipulates bit flags. Table 5 shows a new compiling word that creates a data object called BITSET. The BITSET data object is one cell (2 bytes) containing 16 flags. Each flag can be set, cleared, tested, or examined by setting the appropriate mode before accessing the BITSET and indicating the desired bit position (BITSET 0-15). BITSETs are referred to symbolically. Space for each new BITSET is automatically allocated when it is created.

The BUILDS part of the definition allocates space for a new BITSET and places its address in the dictionary for later reference. The DOES part performs one of four actions (set, clear, test, or display), depending on the value of the variable MODE. The desired bit position is specified as part of a call to the newly created BITSET operator. Four operators that set the state of MODE are also defined for convenience. For example, a new BITSET, called FLAG, is created (Table 6). In this example, bits 7, 4, and 2 of FLAG are set, and then FLAG is examined. Bit 4 is then cleared and FLAG is examined again, showing the result. Bits 4 and 7 are then tested showing the results FALSE and TRUE, respectively. By creating symbolic constants (DRIVENB, DIRSENS), FLAG manipulation can be done entirely with symbols.

Realtime software developers have traditionally written their code in assembly language because of the need for performance and hardware control. They expect to rewrite code for each target system with a different processor or hardware interface. Realtime applications can be made portable across processor and systems by supplying all the required functions as high level language constructs, independent of the underlying processor instruction set. The programming system also includes a generalized interface to character I/O and mass storage, for added portability. By providing compatible environments for the major processor families, it allows high performance realtime programs to be moved at will among target systems. This means that system development can begin even before the target processor is selected. Upgraded systems can also incorporate new processors without software redevelopment.

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# Leapfrog

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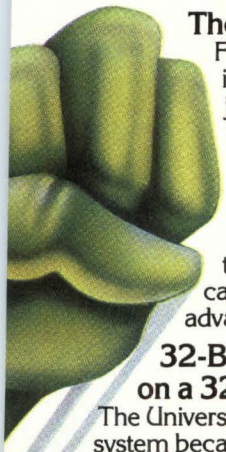

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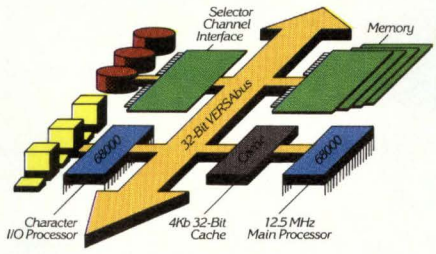


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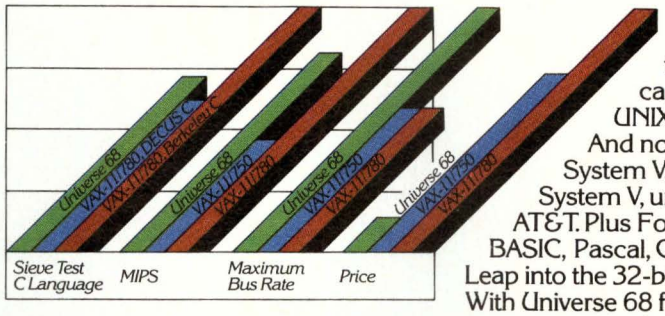


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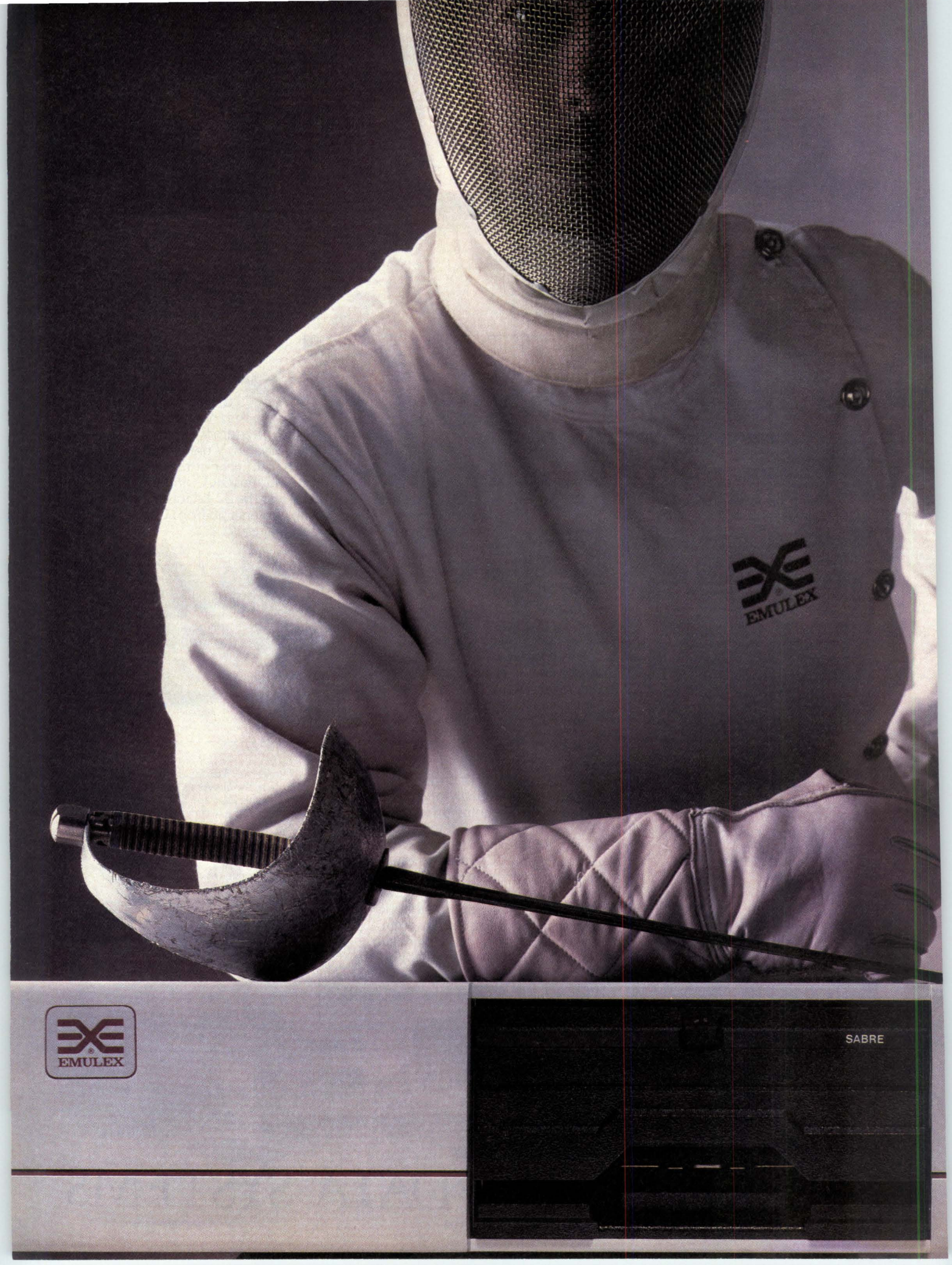
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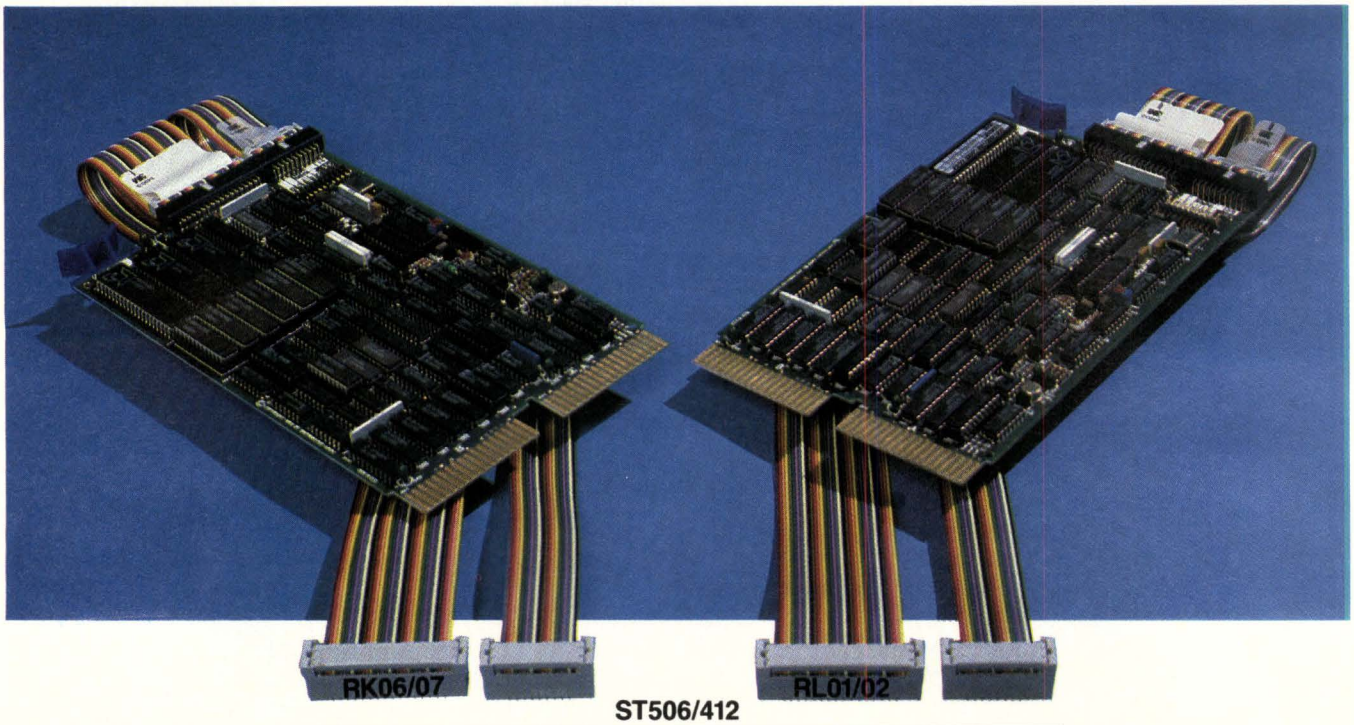


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**CIRCLE 108**

# NEW TOOLS BUILD MICROSYSTEMS

## Designing modern 16-bit computer systems requires a new set of tools. Modularity and a variety of realtime tools increase productivity.

by Larry Badagliacca

A highly structured, controlled environment leaves little or no room for individual instruments jury-rigged to run more or less together. It does involve a mini or mainframe computer for software development, surrounded by multiple, integrated workstations (eg, Dolch's ATLAS system) as nodes. In-circuit emulators, stimulus instruments (such as pattern generators), and logic analyzers may all be linked in a consistent, realtime way that defines their interactions according to the controls available and the events sensed. A common data base is provided for all development team members, and file and display formats are standardized for ease of use by any team member, regardless of the data origin.

Such an approach provides for tight project management and control. It is in direct contrast to today's team effort in which the various team members may each have private copies of data and programs, with little or no consistency among the various copies.

### The modern development process

Microprocessor-based systems apply the modern development process to larger and more complicated problems. System resources now include multiple 8- and 16-bit microprocessors, larger memories, and more special function chips such as math and floating point processors, communication processors, and text processing chips.

Even though the computational power of 8-bit microprocessors is frequently adequate, these devices today are playing a transitional role, by paving the way for 16-bit devices. In some cases, the 8-bit processors are still used because of the large software base available, or because of the great variety of specialized peripheral chips available. On the other hand, the demand for more memory has created an equivalent demand for processors that can address the required memory directly.

One significant consequence of the new systems' complexity is that it is no longer efficient for one person to design and implement a complete system—the scope of the system is too large and the interactions are too complex. Instead, several people—a team—now work together to develop a system.

Another consequence of this complexity is that the use of the larger memories means that more code is being generated. For this reason, efficient code generation is needed to keep the development process short and economical. Both factors—team effort and the need for efficient code generation—result in a need for modularity as well as hardware and software standards. Modularity and standards allow development team members to concentrate on the piece of the job for which they are responsible, and ensure that the finished pieces can be successfully integrated into a common whole.

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At the hardware level, the new systems need standard bus structures and interfaces to the system under test, and other standards (protocols) that define the logical interactions, timing, logic levels, etc. At the software level, there is a need for structured programs in which a dedicated module performs each function. There must be standard methods of passing parameters and data structures from module to module, a common data base on which all the modules operate, and software tools to optimize system memory use and execution speed.

Developers also need to generate small amounts of dedicated, throwaway code—code written to test small portions of the system that will not become part of the higher level, total test program. Older, smaller systems could be developed by one person able to optimize system performance. In contrast, the newer, larger systems prevent any one person—except perhaps the project manager—from seeing a clear picture of the whole. This means that the systems being developed must be broken down into separate modules, which until integration into the whole, remain as quasi-independent functions to be developed by themselves. This same modular approach also makes debugging easier.

As a result, the payoffs and problems are now much larger. The early systems were applied to simpler, less consequential uses such as controlling a single motor. On the other hand, the new systems are applied to far more complex uses, such as controlling an entire production line.

### Linked development tool functions

Many times, hardware and software modules must be tested before the interfaces are available. This requires a stimulus source to simulate the inputs to the controller. Physical modularity also creates a need to link together various tools (ie, in-circuit emulators, and logic analyzers) to monitor the various modules and their interactions. There may be several interacting processes at work among the modules being investigated, so the designer may need to look at the processes and their interactions both simultaneously and individually, to identify and correct problems. Multiple logic analyzers connected to the development system make this possible.

Multiple instruments, in turn, have created a need for new kinds of instrument interaction and linking. First, the software development environment (on a mini or mainframe) must communicate with the actual target system via the test/debug instrumentation. Such communications now make use of traditional methods, essentially the RS-232-C serial interface. But such methods are not designed for distributed networks, do not permit realtime interaction, and typically give only a point-to-point type of communication. Information flows to and from the host to a single emulator, or to a single logic analyzer. Besides being limited to communications between two devices, this type of interface, the RS-232-C in particular, is painfully slow when large amounts of code must be transferred.

The most significant new requirement is that there be realtime interaction among all the various test-support units such as analyzers, emulators, stimulators, etc. This is a serious problem, since parts are not usually available from a single vendor, and it is not easy to make the instruments work together.

### Integrating the workstation

In software development, the integrated workstation functions, first of all, as a terminal interfacing the host—a minicomputer or mainframe—on which the software is developed. Users operating this "terminal" have a direct connection to the software development environment for editing, assembling, compiling, checking syntax, etc.

Another mode lets the designer download the developed software into the workstation or an emulator, via communication tools ranging from a simple RS-232-C interface to a high performance local area network (LAN). Once in the target system's code debugging environment, the workstation allows the various tools to be tied together in a consistent, realtime way.

Dolch's adaptive test and logic analysis system (ATLAS) is a family of instrumentation front ends combined into a single, integrated, digital workstation. The ATLAS mainframe itself combines a general purpose microcomputer, the MP/M operating system, and a high speed interface (the link bus) into a system in which the plug-in modules operate as intelligent multi-users. The modules can interact among themselves, with the target system under development/test in real time, and also with the mainframe controller and other systems on the development network. A double-wide CRT screen provides split-screen displays that simultaneously show data or timing diagrams, with menus, comments, or test results. (See Fig 1.)

*The integrated workstation allows event detection capabilities to be combined in a variety of ways.*

The ATLAS system does this using its link bus, which allows each plug-in instrument to sense realtime events detected in other instruments, and to combine them in logical ways. Historically, such realtime events have been called by different names in different instruments. In in-circuit emulators, they have been called breakpoints, because their most common use was to stop or start the emulation process. In logic analyzers, these same events

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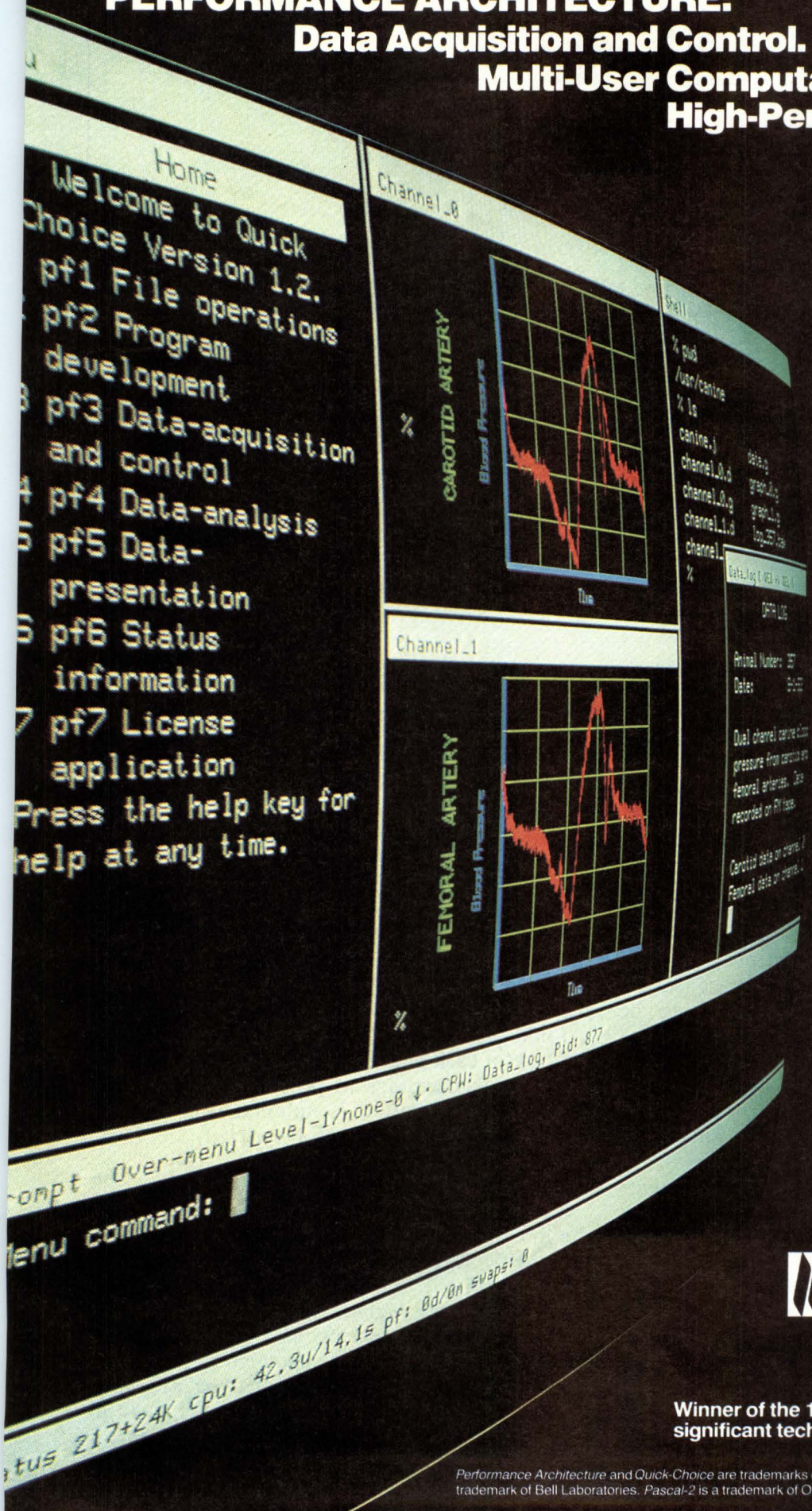


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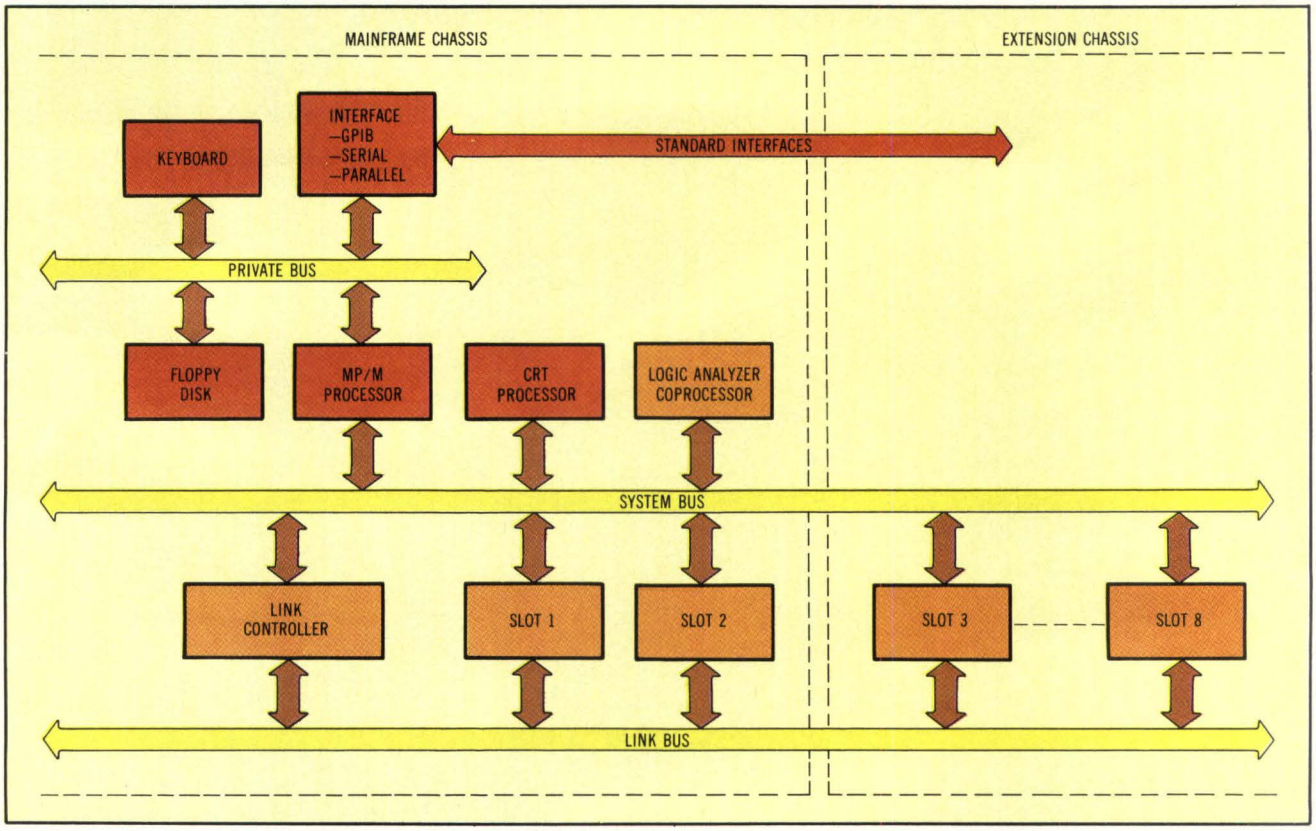


**Fig 1 The ATLAS system consists of an extension chassis with six expansion slots for instruments, and a mainframe chassis with three microprocessors for MP/M, CRT, and logic analysis processing and control. The private bus handles interfacing tasks to computer peripherals (disk drives, etc). The system bus controls the communications between the two chassis and ties together all the plug-ins, the three microprocessors, the link controller, and its associated link bus.**

are called triggers. These are semantic differences, however. What is important is the ability to detect all such events in a realtime hardware system, even though they may assume myriad forms.

Furthermore, each instrument within the integrated workstation detects events at a level of complexity appropriate to that instrument. It may be capable of multiple trigger levels, pass counts within levels, sequencing of the events to be detected, or whatever function is needed.

Finally, the integrated workstation allows all these event detection capabilities to be combined in a variety of ways. This lets the workstation link those events to the various test system units that need the information.

If the various plug-ins and other instruments must influence each other in real time, ATLAS users can use the system's link function. This function detects events from the instruments attached to ATLAS to determine the start and stop sequences for all involved. Thus, events that occur in one plug-in (eg, a logic analyzer's triggers) can influence the process in another plug-in such as an emulator.

The link function may be best compared with the sequential trigger of a logic analyzer. In a sequential trigger, the time interval between starting and stopping the analyzer is divided into steps called trigger levels, and an advance from one level to another is signalled by trigger events.

Analogously, in ATLAS the interval between the initialization of all plug-ins and the time they finish their tasks is divided into steps called link levels. A link event occurring in a plug-in causes an advance to the next link level, and other plug-ins can be signalled to begin a specific action called a link reaction. Figs 2 and 3 depict this process.

Link events and link reactions are separately defined for each plug-in, and each plug-in stores the information necessary to program the link function. The information is automatically accessed whenever ATLAS' link menu is selected.

## The integrated workstation

Two examples will demonstrate the concept of the integrated workstation. Both examples are of tasks difficult for today's typical instrumentations. The first example is of a relatively simple stimulus interaction; the second, much more complex, shows how several elements may be viewed simultaneously in a logic analyzer/emulator interaction.

In the first example, a logic analyzer plug-in is set to trigger at the occurrence of an I/O request to an external device. When it detects this event, it supplies an input signal to ATLAS' link bus. Using the system's link menu, the users have also

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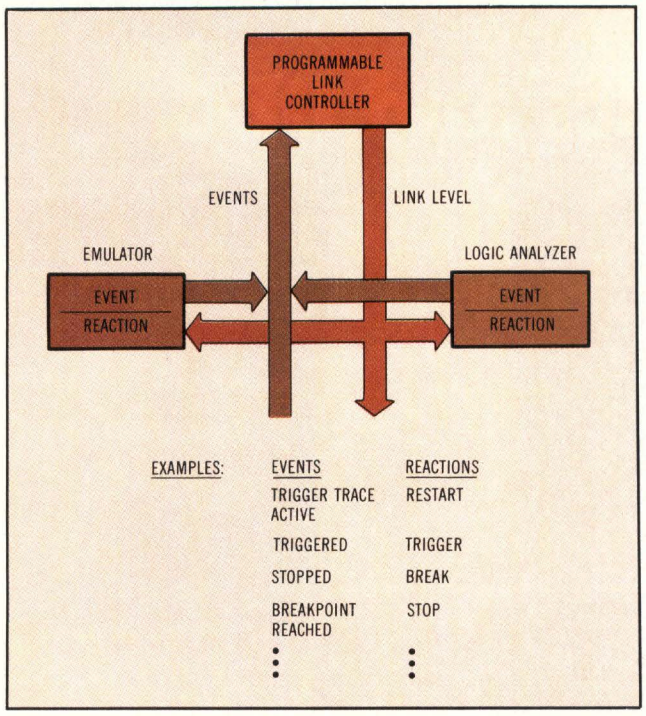


**Fig 2 The link bus offers realtime interaction between instruments. Through it, an event occurring at one instrument causes a reaction at another. The logic analyzer can be told to start recording immediately after the emulator has reached a specified breakpoint. Programmed through a separate menu, the link controller can await specified events and trigger reactions elsewhere.**

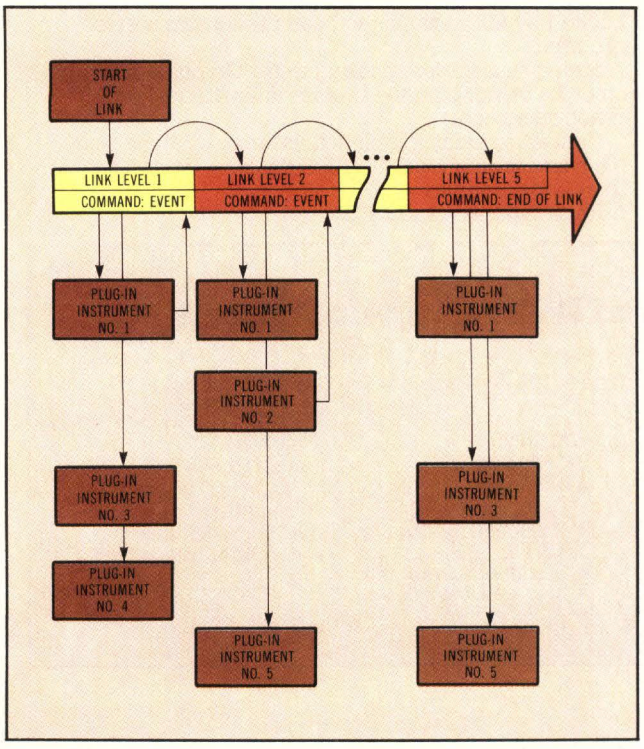


**Fig 3 The link process is a sequential one. An event must occur, then a reaction, then a moving-on to the next link level. The start of the link process causes a command to be sent to a group of plug-in instruments. When an event occurs, the system goes to the next level, and so on, up to five link levels.**

programmed the pattern generator plug-in to trigger on the occurrence of the event. This trigger then causes the pattern generator to simulate the external device, the desired result.

As a second example, consider a system based on multiple 8- and 16-bit microprocessors, in which the processors communicate with each other across a common bus. Suppose, too, that a problem exists in transferring data from two 8-bit processors to a 16-bit processor.

The test set up is as follows: each 8-bit processor has been connected to a logic analyzer plug-in on the ATLAS system; each analyzer has been set to trigger when a bus transfer is generated by the processor connected to it. A third logic analyzer plug-in, connected to the target systems' internal microprocessor bus, has been set to trigger on the occurrence of an event on the link bus—in particular, the 8-bit transfers in question.

The 8-bit transfers are detected by the plug-in logic analyzers connected to the respective processors, and passed to the ATLAS link bus. These link bus events can be subsequently combined and qualified using conditions local to the analyzer connected to the processor bus to check the bus activity by pass counting, adding bus control signals and/or data patterns, etc.

## Look-alikes in the integrated workstation

The power and versatility of the integrated workstations are based in part on file and display format standardization. Standardization allows data transfer among all plug-ins. Standard timing diagrams, data lists, disassemblies, etc permit varied data to be handled in similar ways, and afford the operators a standard way of dealing with the system.

Standardization also allows the systems to display and manipulate realtime events in nonreal time. A pattern can be captured, then used as a stimulus for debugging when the original pattern source may no longer be available. It can even be saved for use in the production test environment. Examination of events in nonreal time also allows multiple sample averaging, generation of histograms for analysis of memory use, determination of the dominant instruction mix, finding where and how the program spends its time, etc.

An individual interface to a shared system, as the integrated workstation affords, brings with it all the advantages of a true individual station, but adds the benefits of multilevel standardization. The software used is guaranteed to be the correct version (through library management and control). The data used is up-to-date (from a shared data base). Compatible file formats provide easy file exchanges. All modules share compatible displays, and all instruments look alike with operating modes that are consistent from one to the other.

In effect, this new approach extends the concept of the laboratory notebook. It offers a common site for the recording of system observations, test results, design notes, manual inputs, etc. The integrated workstation's common data base makes these things possible.

In the new systems, the level of hardware/software complexity already requires multiple instruments to be linked in real time for development and debug. Yet such linking, using even advanced techniques, becomes an extremely complicated process if there is no logical and easily understandable interaction between instruments and functions.

### Workstations become more versatile

Software options permit ATLAS to operate as an instrumentation terminal for minicomputers or mainframes. For example, ATLAS can emulate a VT-100 terminal for a VAX or PDP-11 computer, providing a transparent interface between the target system and the computer.

Programs generated on the larger computer can be downloaded to ATLAS for debugging of the target system and integration of its hardware and software. In this fashion, ATLAS can operate on a LAN with other ATLAS systems and/or Dolch logic analyzers, or on a larger central computer host network via RS-232-C or the IEEE 488 bus.

Available for ATLAS are logic analyzers, in-circuit emulators, digital word generators, a serial data analyzer, and a PROM programmer. Each plug-in is supplied with its software on diskette, an operating manual, and its keyboard flip chart. The ATLAS concept and its documentation allow anyone—not just Dolch alone—to design and supply plug-ins.

Using the system's proprietary link bus, only a 10-ns delay is required for one module, such as a logic analyzer, to recognize an event and trigger another module, such as an in-circuit emulator, to trace or control the CPU.

The modular flexibility of the ATLAS system includes logic analysis with 48 channels (at 10 and 20 MHz), 32 channels (at 100 MHz), or 16 channels (at 300 MHz); in-circuit emulation (support of 8- and 16-bit microprocessors); word generation (20 and 100 MHz); PROM programming; and serial data analysis. Finally, the ATLAS mainframe will accept two plug-ins, with six more in an expansion chassis.

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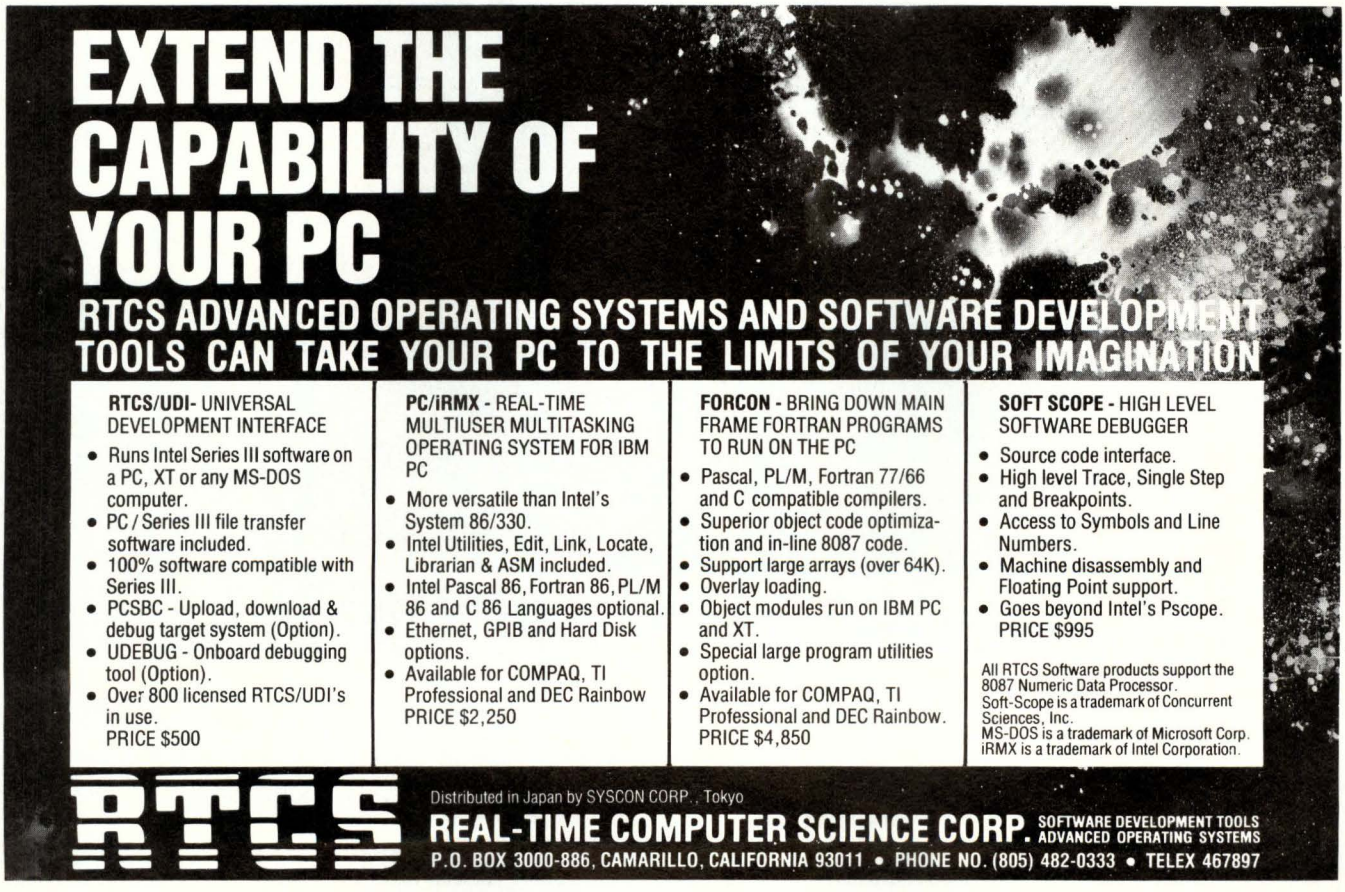

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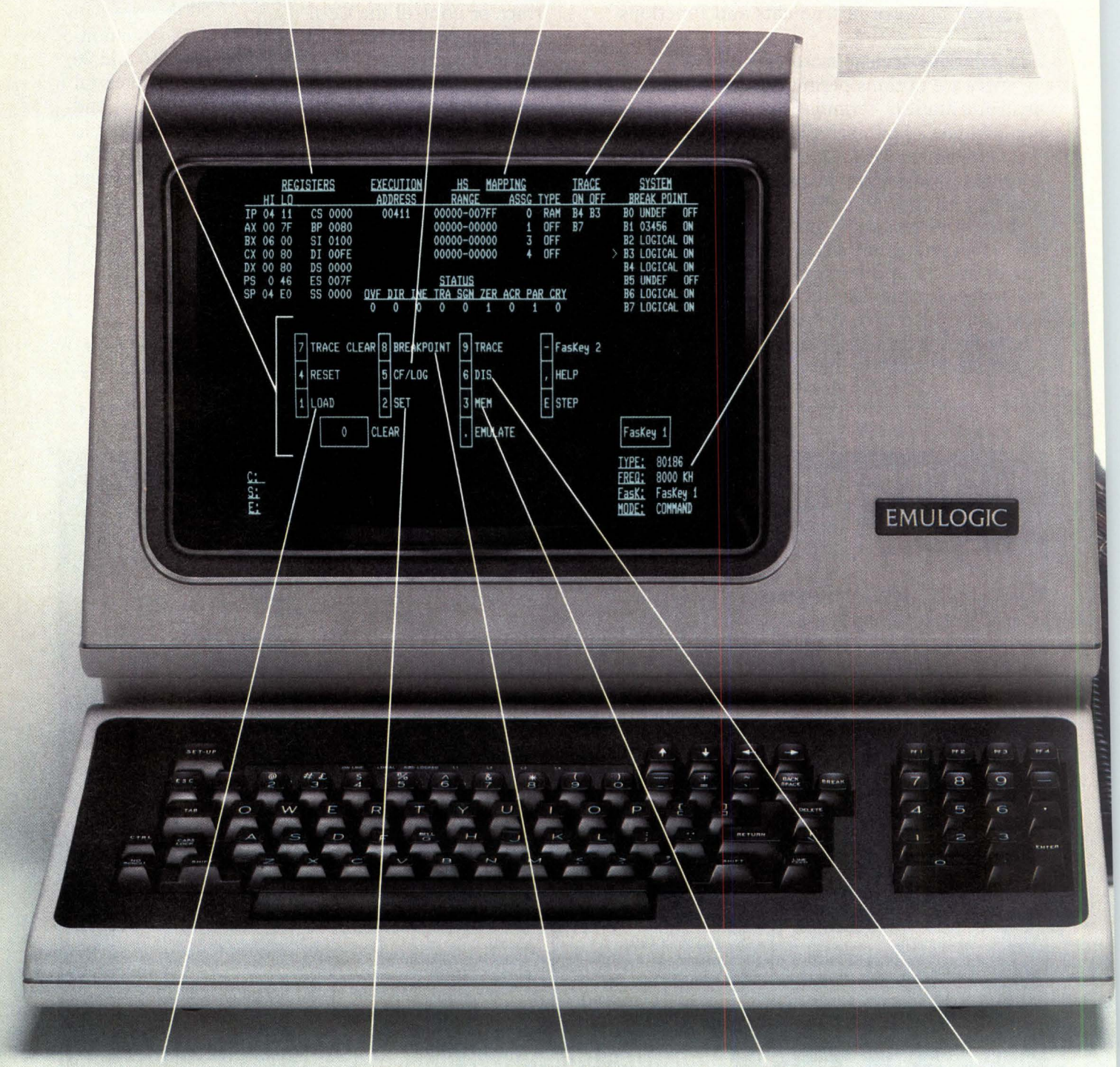


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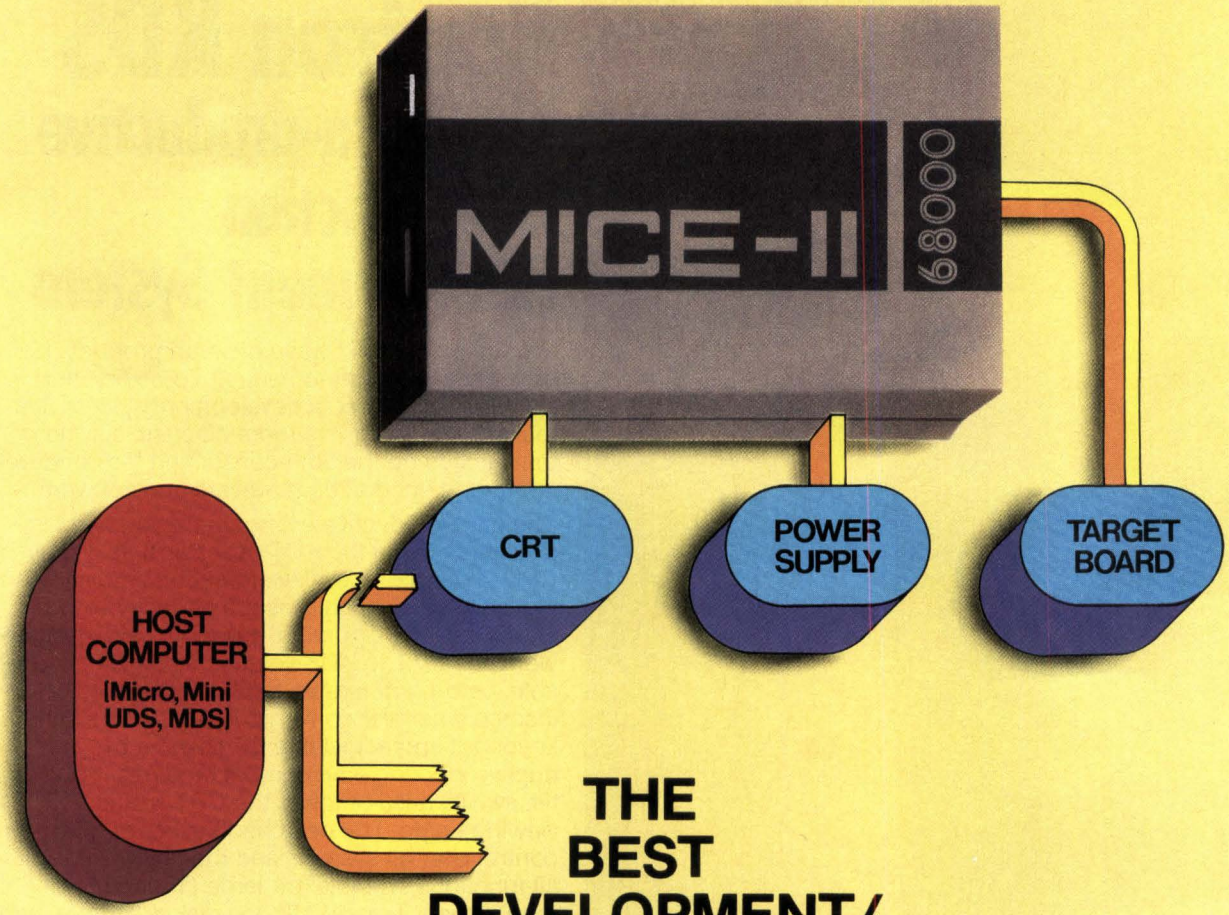


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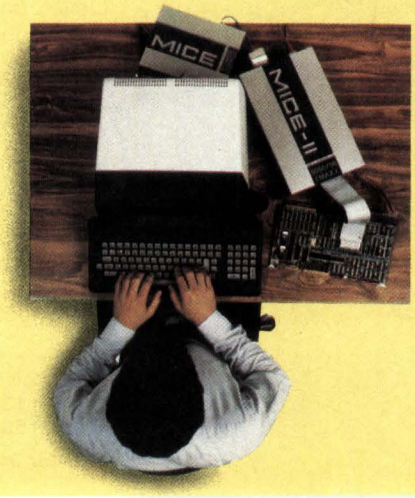


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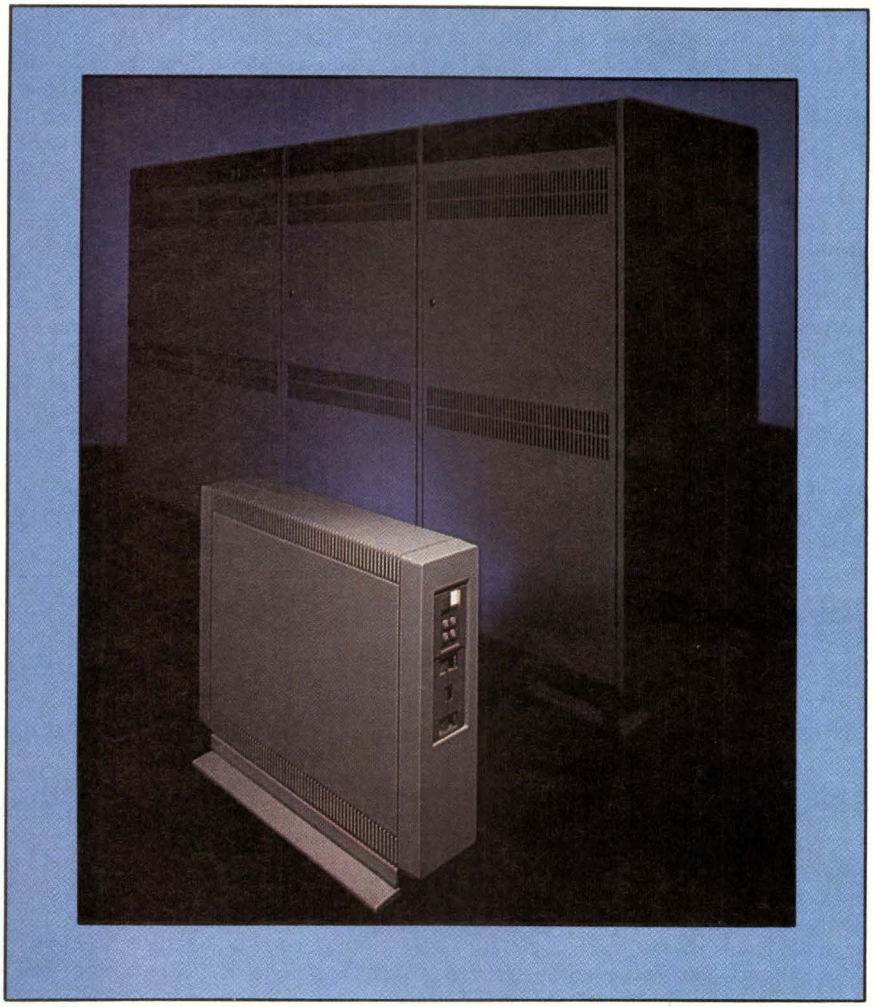
Implementing a subset of the VAX architecture, the microcomputer retains all the key family elements. These include virtual memory management with address capability of more than 4 billion bytes, sixteen 32-bit general registers, and 32 hardware and software interrupt priority levels. In addition, all native-mode instructions are provided for byte, word, long-word, quad-word, and single- and double-precision floating point data types. Full memory management performs virtual to physical address translation and page protection. The system supports emulation for the full VBAX instruction set excluding the PDP-11 compatibility mode.

Some instructions that are hardware-assisted in other VAX systems are implemented in software. They include both D and H floating point instructions, decimal strings, some character strings, and compatibility mode instructions. The central processor resides on two quad-height modules occupying adjacent slots in the Q22 backplane. One module contains a 32-bit data path, a microsequencer, and control store. The second module contains both memory management and cache. It also provides the interface logic for the Q-bus connection to the internal VAX architecture. The system uses standard Q-bus memory modules and performs all data transfers in block mode.

Storage options include a 5¼-in., 10-Mbyte RD51 Winchester disk subsystem, and the RX50 dual-floppy diskette drive with a total storage of 800 Kbytes. A 28-Mbyte Winchester disk is also available. The system uses the same compact enclosure as the Micro/PDP-11 computer.

Software packages offer VAX compatibility in development and production environments. VAXElan software, a compatible subsystem to the VMS operating system, allows application development for realtime control and distributed computing. It consists of development utilities



for creating target applications, and a runtime kernel of device drivers and service code that becomes a part of each application. Applications are written in an optimizing native-mode version of Pascal, which can be downline-loaded across network (local or wide area) links, or transferred to target systems by disk or tape. Finished programs are entirely memory resident.

The MicroVMS operating system is a VMS system version for the MicroVAX. Specially packaged, it still provides the same runtime environment as larger VAX computers. In modular form it allows support for configurations with small secondary storage capacity and reduces the overall system cost. A base system provides application execution. One or more system options tailor operations to specific environments, such as networking, program development, and multi-user authorization and accounting.

ULTRIX is based on the Berkeley VM Unix system, which takes advantage of the VAX virtual memory architecture. It offers vendor independence and portability. Applications are in nonrealtime design and analysis, and in value-added systems requiring a generic software base.

Supported VAXElan development licenses begin at $8200 with a runtime license at $100. Prices for the MicroVAX I begin at $9995 for a diskless, rack-mountable unit with 512 Kbytes of memory for dedicated, memory-resident applications. With RX50 diskette and RD51 Winchester disk drives in a floor-standing unit, the price is $13,880. Initial deliveries are set for Mar 1984. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754. **Circle 260**

## Two-part array couples memory and logic and adds testing

As a member of the bipolar Macrocell array family, the MCA1500M uses the Macrocell array logic concept and high speed RAM to form an LSI circuit. The logic part of the array uses the MCA2500 macro library (with performance equal to the MCA2500), while the memory part configures 1280 bits in various user selectable modes.

The array consists of 112 logic cells and eight memory blocks. Of the 112 logic cells, 63 are major cells and 49 are output cells. Arranged in a 7 x 9 array, the major cells take up the largest die area. The output cells are along the top and bottom edge of the die. Five output cells double as memory test outputs; they therefore have a restricted options.

Memory portion of the die has eight equal blocks of 32 x 5 bits located on the right one third of the die. This positioning allows convenient routing to and from the logic portion, yet does not disrupt interlogic routing.

The selection of predesigned memory macros customizes memory configuration. These macros store interconnect information for various configurations within a CAD system. Ten basic macros come in any combination within the 1280-bit constraint. In addition, the memory has a dual-port mode design. The six dual-port macros allow the same data to be written into two memory files simultaneously with each file having independent address selection. While in the read mode, an independent address accesses each file.

A memory test circuit is a fixed part of RAM. The testing is the same, independent of user-selected memory configurations. Each block tests as a 32 x 5 RAM with block selection by three higher order memory test addresses. There are some restrictions on option die ports during test access. For example, a test enable input (TE) determines memory mode so that its port is restricted.

Test memory input buffers operate in parallel with the option input ports. An option may or may not use the 15 inputs that are in a fixed location. When the memory is operational, the input buffers disable. Thus they present little influence on option input ports.

Five output cells take in the test outputs from the memory. Fixed to five ports via a CAD system, these cells and ports face restrictions (as outputs) only when used by options. The TE signal selects between memory test and option output on the five ports.

TTL interface provisions allow any device port to assign a TTL compatibility using macro selection at the design stage. TTL-to-ECL translation on input ports and ECL-to-TTL translation on output ports reduces total system package count while enhancing system performance. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051. **Circle 261**

## Computerized engineering index: a boon to components research

An IBM PC compatible software index that keeps track of some 400,000 products and services from roughly 5000 suppliers is updated every 60 days. By giving design engineers desktop, library-style support without intermediaries, Micro-Index can dramatically reduce the time a staff spends researching prospective system elements.

Product/service descriptions and supplier names in the index reference a companion microfiche data base—Tech-Doc. The data base contains complete specifications, test data, application notes, catalogs, and pricing information for items listed in the index. Source material is reproduced from the supplier's documentation, without editing or abridgement. A detailed contents page outlines key elements in each major database category.

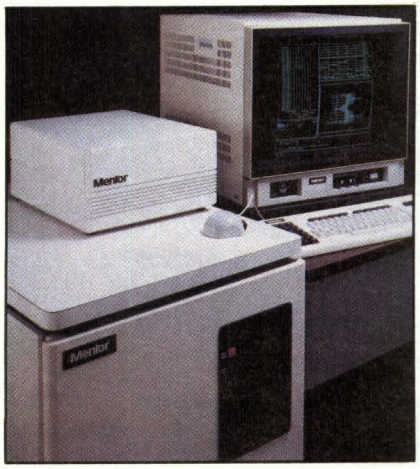
The disk-based index provides company name, address, contact, phone number, telex, and specific page reference to desired document. A search by product description leads to supplier names, addresses, communication numbers, and location of the source data. Search by supplier name locates addresses, communication numbers, full product line description, and location of the firm's complete data on microfiche.

Structured around an engineering "thesaurus," the index addresses entries by either formal nomenclature or common descriptions. Spelling algorithms branch to a new menu for each "correct" item selected. A partial product description or company name will call up a menu of related records.

Eighteen product/service categories constitute the index and data base. These include electrical and electronic components, computers, communications, and instruments and controls. Indexing software comes on 5¼-in. double-sided, double-density floppies or a 10-Mbyte hard disk, and runs on 256-Kbit microcomputers using the MS-DOS version 2.0 operating system. Future releases will port Micro-Index to the CP/M operating system and Digital Equipment Corp minicomputers and mainframes.

Apart from the indexing software and microcomputer, a complete workstation includes microfiche cards and reader. Annual database subscription for any one component category ranges from $105 to $945; a partial component index costs 57 percent of the component order. Total component index is $2850. **Inacom International,** 4380 S Syracuse St, Denver, CO 80237.
**Circle 262**

## Workstation integrates test and measurement with CAE




With a complete logic analysis system and tools from the Idea 1000, the Midas 7000 supports the entire digital hardware design cycle. The system covers not only schematic capture, simulation, and physical layout, but also verification and test of the final hardware.

Data acquisition and clock probes connect the 7000 to the hardware under test. Realtime acquisition results go to the workstation's main memory. Once there, a disk drive on the network stores the data, or the workstation can process it.

To analyze software performance, a user-written program (anywhere on the network) acquires and processes realtime software execution. In histogram form, the CRT displays subroutine call frequencies that are automatically sorted. Through the use of command macro files and programmable keys, only a single keystroke will accomplish the software analysis.

A triggering system is the basis for state acquisition. Its 60-word recognizers trace software data flow. The recognizers organize into 15 states for either triggering or data qualification. A programmed trigger sequence can jump between states, branch to other states, or branch within a state to trace recursive software flow.

The sample clock uses five clock lines defined in terms of logic or transition edge, then they are ORed together for synthesis of bus-cycle clocks for microcomputer systems. Two hold clocks demultiplex buses without double probing.

To make the most of its 4-Kbyte/channel data storage memory, the timing analyzer uses several acquisition modes to increase the time window for acquiring data. The transition mode stores data only when a transition occurs on one of the acquisition channels. A counter provides realtime representation of timing activity on the display. The counter keeps track of the number of samples between transitions.

A multitrigger mode breaks data acquisition up into subgroups of 16 samples. The same user-specified trigger event is at the center of each subgroup. During acquisition, an additional subgroup is stored for each trigger event. In this way, up to 32 stored subgroups can give the user a record of triggering occurrences.

Available in the first quarter of 1984, the Midas 7000 is priced at $14,900. **Mentor Graphics Corp,** 10200 SW Nimbus Ave, Portland, OR 97223.
**Circle 263**

## Development system turns any microcomputer into workstation

Using a personal computer as its control console, the Universal Development Laboratory integrates an analyzer, an emulator, a programmer, and an input stimulus generator in a single pod-sized box. A control program running on the host coordinates system resources. When emulating a target ROM, the laboratory becomes a development system for any target processor.

The 48-channel bus state analyzer triggers if a program goes outside its normal address range. In addition, the trace buffer stores 170 bus cycles that can be used for debugging. Trigger setups and traces of good systems can be saved on disk, then automatically compared to later test traces. A filtered trace allows only writes to a particular memory location together with a following cycle (which contains the next instruction). Four-step sequential triggering specifies up to three events that must occur before triggering becomes possible.

To search for the trigger, the system uses high speed RAM truth-tables instead of comparator circuits. This allows any 8-bit function to be specified on each of the 6 input bytes.

Universal at both ends, the system interfaces to the host through an RS-232 port and to the target system through a standard ROM socket. Because the bus state analyzer can debug any processor, target processor emulation is unnecessary. Most target bus signals connect at the ROM socket, so a complete view of bus operation takes only about 12 additional analyzer inputs. The signals connect by plugging probe wires into a 40-pin DIP clip on the target processor.

Since the target processor stays in its socket, operation is transparent. Moreover, maximum 195-ns access time makes ROM emulation fast enough for full-speed operation with next generation processors. A single wire connects both the analyzer and the emulator to target system signals, minimizing loading.

The ROM emulator and EPROM programmer share the same memory, so EPROMs can be burned directly from the target program image used for emulation. This target program can be loaded several ways: read from hexadecimal or binary disk files, received serially in hexadecimal format, or from a ROM in the programming socket.

The system sells for $2395 with 64 Kbits of emulation memory. **Orion Instruments,** 172 Otis Ave, Woodside, CA 94062. **Circle 264**

## Ergonomic VDT's calling cards are programmable features and low cost

The Freedom 200 offers a long list of features in one package. Consisting of a 12-in. display and a detachable keyboard, the terminal's points of interest range from a nonglare screen to setup modes and programmable functions keys.

The CRT uses a 24 x 80 display format. The 25th line is user accessible for status or other information. A full tilt (+15-degrees, −5-degrees) and swivel (70-degrees) console houses the etched green phosphor screen.

In native mode, display memory is one page with the second page optional. In emulation mode, memory reaches two pages with additional pages optional. The unit emulates both TeleVideo 950 and Lear Siegler ADM 31 terminals.

Advanced video features include nonembedded character attributes. In visual mode these are normal, reverse, half intensity, underline, blink, and blank. In data entry mode they include protected, alphanumeric, alpha only, numeric only, and extended numeric.

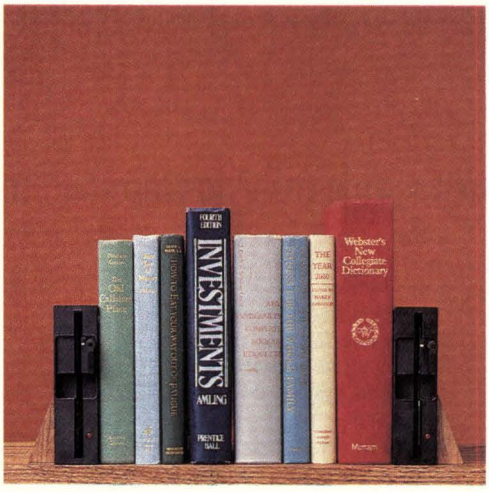
Jump or smooth scroll is available. Smooth scroll is programmable with rates of 2.5, 5, and 10 lines/s. The user can elect to scroll only parts of the screen by defining a scrolling region.

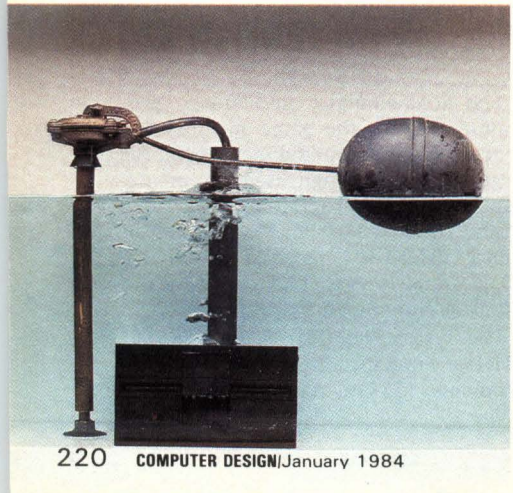
Four communication modes are provided: block, conversation, monitor, and local. Block can be immediate or deferred and sent from command. Conversation mode transmits half and full duplex. Monitor mode displays control codes in programming applications, while local mode operates standalone.

The detached, low profile keyboard clusters 106 sculptured keys into functional groups. Twenty programmable function keys (using the shift) produce up to 256 Kbytes of code sequences. These keys can also send 20 preprogrammed default sequences. The 11 cursor control keys assume an inverted "T" format. In addition, there are nine editing keys and 12 functional command keys.

Handshaking protocol is X-on/X-off with programmable characters and DTR. Fifteen transmission rate selections range from 50 to 19.2k baud. Parity choices are even, odd, or none, with word structure at 7 or 8 data bits with 1 or 2 stop bits. Interface is via EIA RS-232-C.

The terminal is priced at $745 for quantities of one to nine; $670 for 25 to 99 units. **Liberty Electronics,** 625 Third St, San Francisco, CA 94107.
**Circle 265**





### Small size industrial computer

Indy is a portable computer designed for a rugged multitasking environment. It emphasizes software flexibility by offering CP/M-86 and RMX-86 operating systems; Fortran, Pascal, Basic, and C compilers; and various utility programs. Based on a Multibus architecture, the computer consists of 16-bit 80186, 512 Kbytes of parity RAM, 9-in. CRT, dual 3.5-in. floppy drives, and parallel serial ports. Basic computer configuration containing only the CRT controller board costs $1975. **Monolithic Systems Corp,** 84 Inverness Circle East, Englewood, CO 80112. **Circle 266**

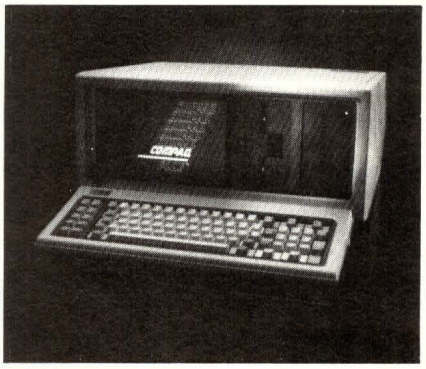
### Supermicro computer family

Decentralized hardware and software are features of the Multex I and II. Hardware includes dedicated processor buses and multi-ported processors that share a common system bus to provide 6.3 Mbytes of RAM for up to 32 users. Running on software with a standard Unix programmer interface and built-in DBMS, the processor performs many operations without application software. The Multex I has a 157-Mbyte Winchester, while the Multex II combines a 315-Mbyte disk with a 16-channel 1200-baud full-duplex modem. This provides a total network capacity of 1024 users. The two systems are priced from $25,000. **NuVec Laboratories, Inc,** 429 Marrett Rd, Lexington, MA 02173.
**Circle 267**

### Mini-compatible color workstation

The 4180 is a color raster addition to general purpose minis. The workstation's 19-in. monitor displays 16 colors with 1024 x 1024 resolution. A 20-MHz (50-ns) pixel writing rate generates image updates. It offers both 2-D and 3-D local processing and display/communication speeds of 3.088 Mbaud at a distance of 1.5 miles. In a typical configuration, the per-workstation price is less than $43,000. **Adage, Inc,** 1 Fortune Dr, Billerica, MA 01821.
**Circle 268**

### Portable with fixed disk



With 16 bits and a 10-Mbyte fixed drive, the Compaq Plus is capable of running all software developed for the IBM PC XT. The unit contains 128 Kbytes of RAM, a 9-in. video display, two PC-compatible hardware expansion slots, MS-DOS 2.0, and Basic. The portable uses a shock isolation system to protect the fixed disk and ensure its reliability. Price is $4995. **Compaq Computer Corp,** 20333FM 149, Houston, TX 77070.
**Circle 269**


# Six things you can do with your obsolete floppies.

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The DMA 360 gives you hard-disk reliability. Floppies don't.

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In fact, anything you can do with a floppy, you can do even better with a DMA 360. That's why we call it the floppy replacement.

For more information on what you can do with your obsolete floppies, write DMA Systems, 601 Pine Avenue, Goleta, CA 93117. Or call us at (805) 683-3811, Telex 658341.

**Introducing the floppy replacement: DMA Systems' new half-height removable 5¼" Winchester.**

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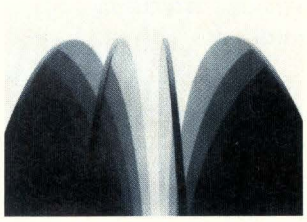
**The Removable Winchester Company.**

CIRCLE 165

### Micro with built-in hard disk

The TRS-80 256-Kbyte micro comes with a self-contained 1.25-Mbyte 8-in. floppy drive and a 15-Mbyte hard disk drive. It accesses 15 million characters on hard disk, and interfaces to an additional 12-Mbyte drive for about 9000 pages of storage. The computer comes with the TRS-Xenix multi-user operating system, which allows up to three users simultaneously without loss of performance. The dual-processor design features Z80A and 68000 16/32-bit micros for high operating speeds. It is available for $6999. **Tandy Corp/Radio Shack,** 1800 One Tandy Ctr, Fort Worth, TX 76102. **Circle 270**


**Step up to a new standard in disk drive performance**
**12 megabyte/sec transfer rate**



Now, you can have data transfer rates in a large-scale disk storage system unequalled in today's OEM disk drive market. This is a real-world solution for designers of graphics, image and other high performance data processing systems. It improves your system's performance while giving your customers the large-scale data storage, higher data transfer rates and added system throughput demanded by today's applications. IBIS provides 1.4 gigabytes of data storage on a single 14-inch Winchester disk drive. The data transfer rate is 12 megabytes per second with average access time of 16 milliseconds thus giving you the fastest disk drive in the industry. Plus, the "designed-in" reliability assures your system's performance.

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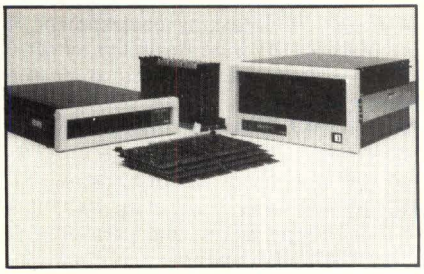
CIRCLE 116


### Array processor memory options



Consisting of a 375-ns, 256-Kbyte memory board, Mini-MAP 211 complements the existing 111 series. For both series, a 375-ns, 1-Mbyte board is available. Designed to meet the needs of large directly addressable memory, tight packaging, and economical pricing, the options target applications including medical imaging, CAD/CAM, and simulation. Burdensome algorithms can be offloaded from the host to the array processor, which can perform floating point calculations one or two times faster than minis or superminis. The 1-Mbyte memory option costs $4160 in quantity 50, while the 211 processor is $13,175 quantity 50. **CSP Inc,** 40 Linnell Circle, Billerica, MA 01821. **Circle 271**

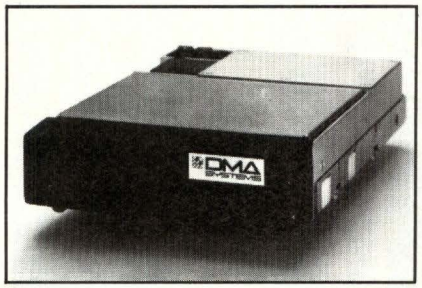
### Supermicro systems

System 286/310 and 286/380 combine iAPX 286 micro and 80287 numeric coprocessor with an enhanced Multibus architecture and system software. The basic package includes chassis, power supply, disk storage, single-board computer, operating system software, and languages. Operating system is available for real-time applications and is object-code compatible with iRMX 86. The Xenix 286 is also available. Prices range from $9900 to $29,860. **Intel Corp,** 5200 NE Elam Young Pkwy, Hillsboro, OR 97123. **Circle 272**

### Computer compatible with IBM PC

The 16-bit TS 1605 comes with 128 Kbytes of memory standard, with optional expansion to 256 Kbytes. Based on the 8088, it offers high resolution (640- x 200-pixel) graphics on a 14-in. green phosphor display. The computer has two half-height 5¼-in. floppy drives, each providing 368.6 Kbytes of formatted storage. Ports include one RS-232 async serial port and one IBM-like DB-25S parallel printer port. **TeleVideo Systems Inc,** 1170 Morse Ave, Sunnyvale, CA 94086. **Circle 273**

### Removable Winchester drive



A half-high, 5¼-in. drive features 98-ms access time and improved transfer rates over floppy disk drives. Extensive air filtration and a 30-s purge cycle ensure safe operation. Fully retracted heads load dynamically to avoid head and media damage. Moreover, onboard firmware lets the user format a blank cartridge after it is inserted into the drive. This eliminates the need to write servo data on the disk surface. The DMA 360 is priced at $500 in quantity. **DMA Systems Corp,** 601 Pine Ave, Goleta, CA 93117.
**Circle 274**

### Battery-backed RAM

The 1822CMOS RAM board features 128 Kbytes of storage on one half-quad size board. Organized to support 32-, 64-, 96-, and 128-Kbyte RAMs, it uses a 2-K x 8 chip for the 32-Kbyte board and a 8-K x 8 chip for the other models. Self-charging NiCad batteries provide data retention for one month. The board supports 16-, 18-, and 22-bit addressing with up to 2 Kwords from the 4-Kbyte I/O for additional space. Applications include nonvolatile program store, data logging, and auto-restart after power failure. **Adac Corp,** 70 Tower Office Pk, Woburn, MA 01801.
**Circle 275**

### Slimline 8-in. floppy drive

With an unformatted storage capacity of 9.6 Mbytes, the FDD-441 uses a 5¼-in. disk controller compatible interface. The drive has a data transfer rate of 1.5 Mbit/s and an average access time of 168 ms, with a track-to-track access time of 3 ms. Track density is 96 tracks/in. It employs a micro-controlled stepper motor, capable of accurately positioning the magnetic head. Rotational speed is 360 rpm, latency is 83 ms, and data transfer encoding method is modified frequency modulation. **Hitachi America, Ltd,** 1800 Bering Dr, San Jose, CA 95112.
**Circle 276**

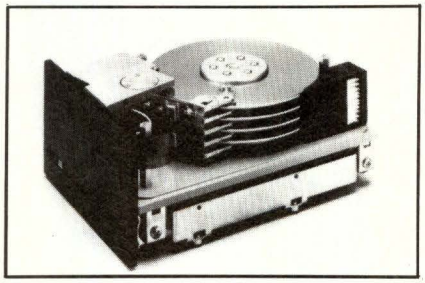
### Dynamic parity Versabus RAM

The PSM 1VP offers 1 Mbyte on a single board. It features a 32-bit structure and a choice of 512 and 256 Kbyte versions. By meeting full requirements of the Versabus spec, these memories support data transfers of byte, word, and long-word width for future compatibility. The RAM provides error status reporting, user-definable mode response, fast access time, and single-bit error detection. A bus parity function ensures high immunity from system failures. **Plessey Microsystems, Inc,** 451 Hungerford Dr, Rockville, MD 20850.
**Circle 277**

### Disk drive subsystem

The 5360 series provides 406 Mbytes of user accessible storage (formatted). It features 1.9-Mbyte/s data transfer and an average seek time of 18 ms. Physically, the drive consists of a single spindle drive motor, power supply, operational electronics, front panel, and sealed module containing the spindle media, rotary actuator, and read/write heads. The 10.5-in. fixed media consists of six platters with one servo and ten data recording surfaces. Drives cost $19,000 per unit. **Harris Corp, Computer Systems Div,** 2101 W Cypress Creek Rd, Fort Lauderdale, FL 33309.
**Circle 278**

### Winchester drive at 100 Mbytes



Using thin-film media exclusively, the V2100 offers a 25-ms average access time. The 5¼-in. drive meets the ST412HP interface standard with a 10-Mbit data transfer rate. Features include a dual-frequency, closed-loop servo system that allows continuous sampling and correction of head-to-track positioning as disks rotate. Track density is 960 tracks/in. An automatic actuator lock and dedicated landing zone counter potential shock and vibration damage. **Vertex Peripherals, Inc,** 2148 Bering Dr, San Jose, CA 95131.
**Circle 279**

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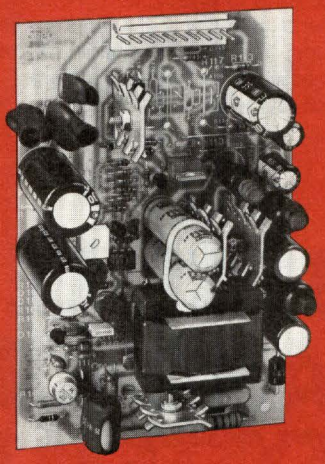

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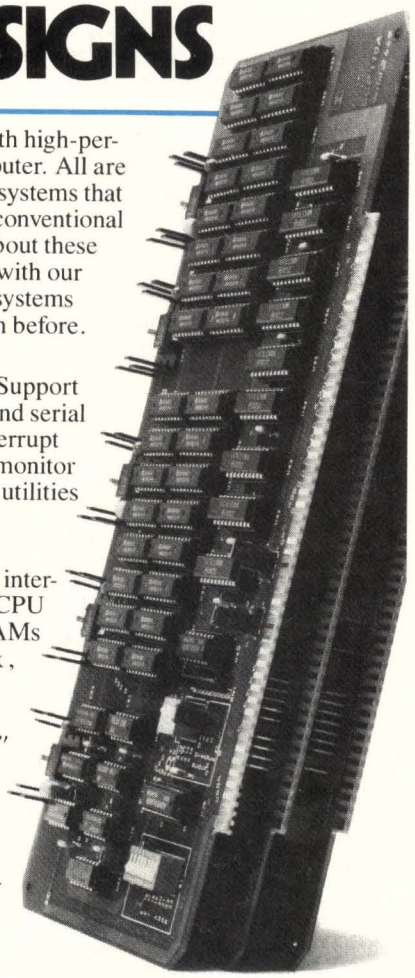
### Static CMOS RAM card

The CBC 512/24 features three-year minimum data retention, 8- or 16-bit CPU compatibility, 24 address lines, Multibus interface, and 800-mW typical operating power. There are three options for battery backup: onboard rechargeable NiCad battery, nonrechargeable lithium battery, or external battery. The starting address is selectable on 64-Kbyte boundaries in a 16-Mbyte memory space. Access time is 300 ns and memory cycles range from 470 to 570 ns for read and from 475 to 575 ns for write. Prices are $1989 to $3978. **Diversified Technology, Inc,** PO Box 748, Ridgeland, MS 39157.
**Circle 280**


# SEATTLE GIVES YOU AN EDGE IN S-100 SYSTEM DESIGNS



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Seattle, WA 98188


### Half-wide streamer

The MT-1220 has a 330-Mbyte capacity and uses the industry standard Pertec micro formatter interface. The drive employs a 24-track, bit-serial, serpentine format with a packing density of 9600 bits/in. It operates in 200- or 50-in./s streaming mode or a 50-in./s start-stop mode. Data is encoded into a 4/5 GCR format, with all encoding and decoding done by the integral formatter. A unique head-stepping feature permits access to any record stored in the cartridge within an average of 30 s. Drives are $4950 each and data cartridges are $100 each. **MegaTape Corp,** 1041 Hamilton Rd, PO Box 317, Duarte, CA 91010.
**Circle 281**

### Cartridge drive with 600 Kbytes

This flexible 3-in. drive is compatible with standard 5¼-in. drives. The MFD-80 records double-density, double-sided on the standard 3-in. disk cartridge at 100 tracks/in. It permits the use of all 48 tracks on each side of the disk. The basic unit is 3.54 in. (90 mm) by 1.58 in. (40 mm), including electronics. A cam controls the read/write head carriage assembly for improved reliability. The drive's rotation speed is 300 rpm and transfer rates are 250 kbits/s. Average track-to-track access time is 10 ms. MTBF is estimated at 8,000 h. **Janome, Ltd,** 1-1 Kyobashi 3-Chome, Chuo-Ku, Tokyo, Japan.
**Circle 282**

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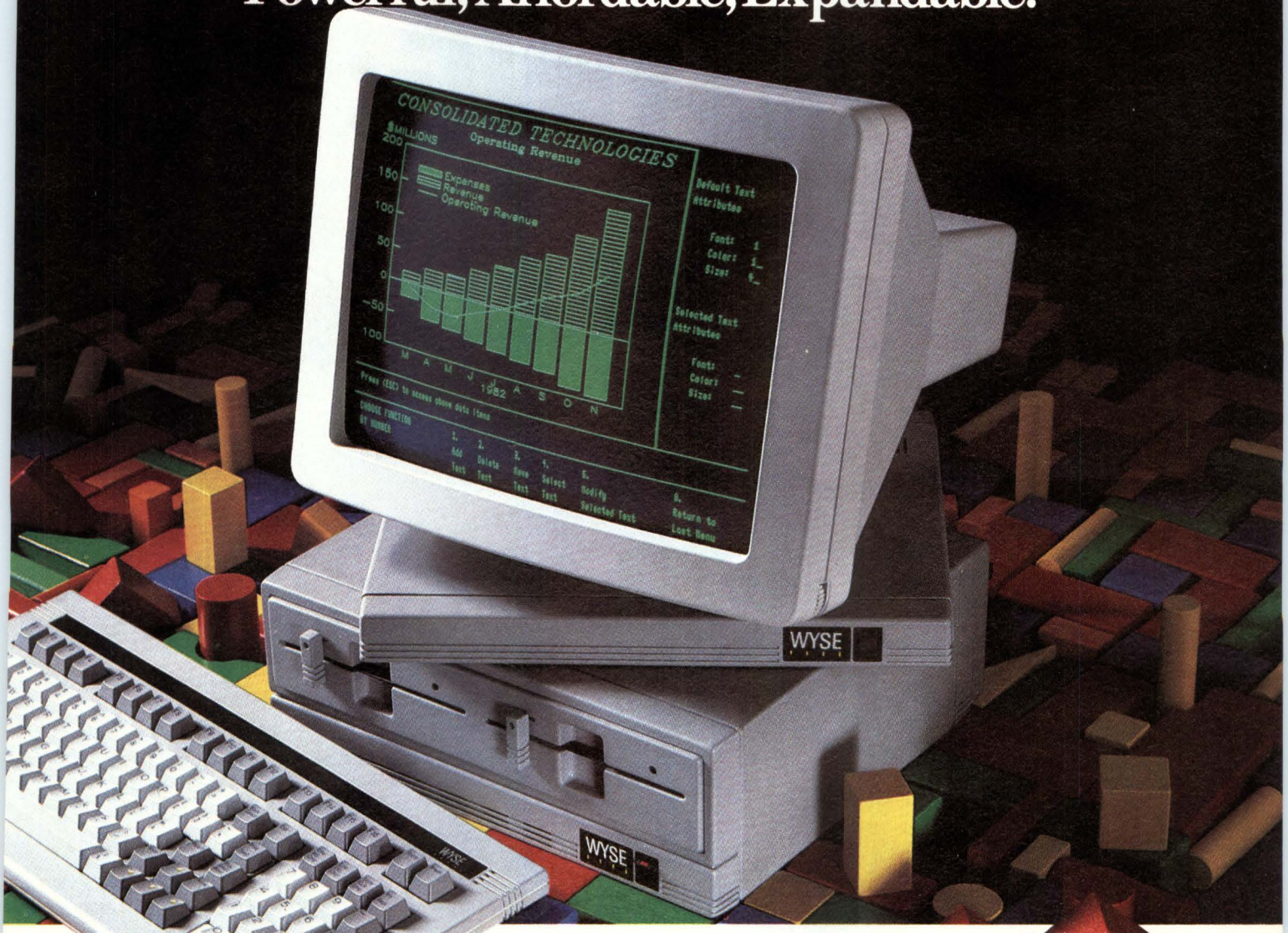
# The New WY1000 Microcomputer

# BUILDING BLOCKS

## Powerful, Affordable, Expandable.




The WY1000 stacks up to be a lot of machine from a few simple pieces. By adding the WY1000 microcomputer to the good-looking, ergonomic WY50 display terminal, we created the most exciting concept in desktop workstations on the market today.

We also added sophisticated high resolution graphics, suitable for the most demanding applications.

Plus, we added color capability, when used with our color terminal.

And on top of that, we added a Winchester Disk Drive option providing an additional 10 megabytes of storage.

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- **80186 16 Bit 8 MHz Processor**
- **128KB to 768KB RAM Memory**
- **Two Floppy Disk Drives (725 KB)**
- **Optional 10 MB Winchester Drive**
- **RS232 & RS422 Serial Ports**
- **Optional Graphics/Color Graphics**
- **Networking Capability**
- **CP/M™, MS-DOS™ Compatible**
- **Priced from only $1995**

Best of all, we priced the WY1000 from only $1995. It all adds up to a system builder's dream.

For a complete brochure on the WY1000 contact Wyse Technology toll free at 800/421-1058.

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**WYSE TECHNOLOGY** *3040 N. First St., San Jose, CA 95134, 408/946-3075, TLX 910-338-2251, Outside CA call toll-free, 800/421-1058, in So. CA 213/340-2013.*

**CIRCLE 139**

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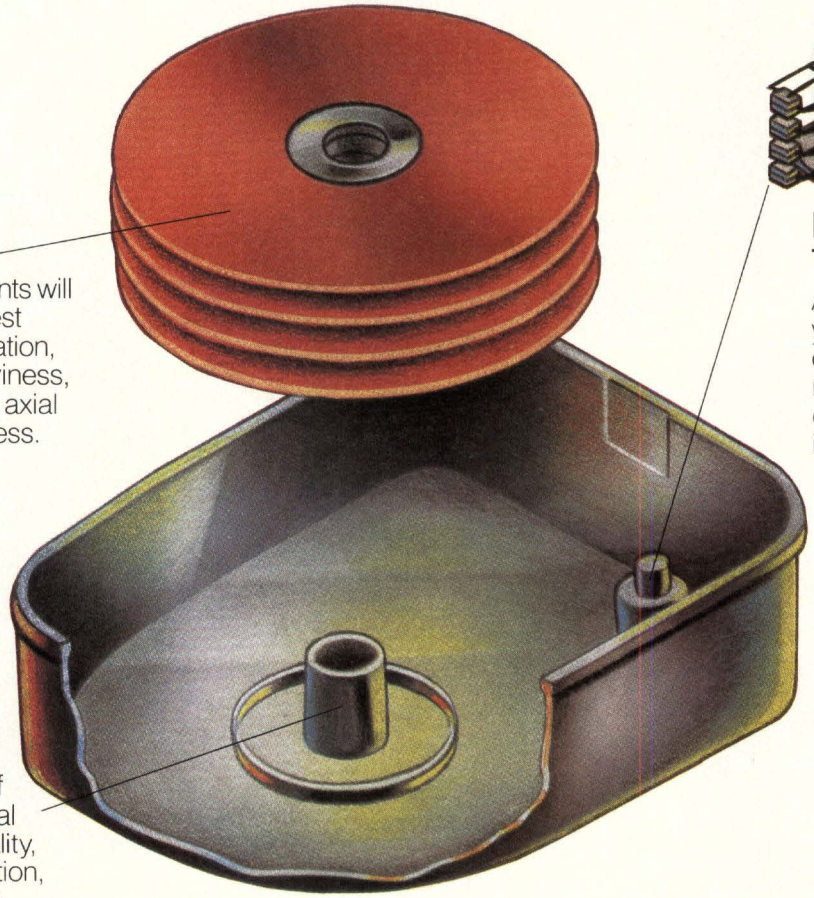
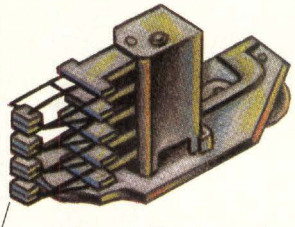
# A CRASH COURSE IN DISK AND DRIVE TESTING:





### Disk Testing

ADE RVA instruments will show you how to test excessive acceleration, flatness, radial waviness, datum positioning, axial run-out and thickness.

### Head/Assembly Testing

ADE RVA instruments give you advanced instruction on head positioning accuracy, head motion studies, dynamic flight characteristics, pitching and rolling.

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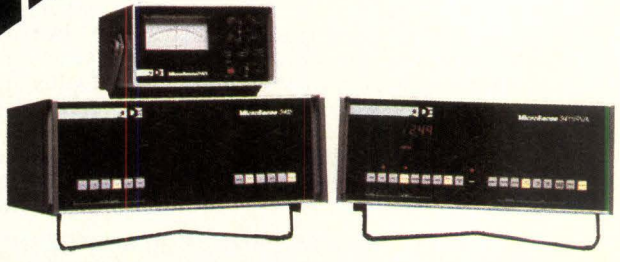
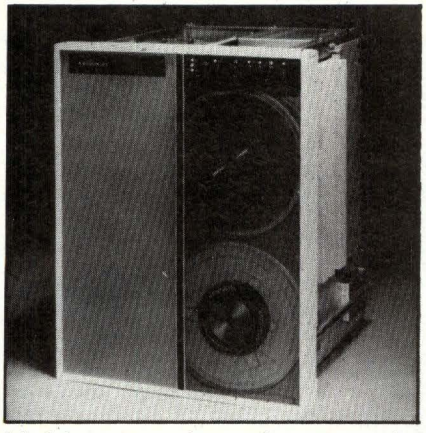



ADE Corporation
77 Rowe Street
Newton, MA 02166
Telephone: (617) 969-0600
Telex: 922415


CIRCLE 142

### Tri-density tape transport



Model 9400 uses nine-track, group-code-recording and provides high speed backup for minicomputer systems. It has a 6250-bit/in. data density for an unformatted capacity of 180 Mbytes on a 10.5-in. reel. The unit will also operate at 1600 bits/in. using phase encoding and at 800 bits/in. using nonreturn to zero encoding. Diagnostics allow onsite troubleshooting in the field or remote diagnostics via a modem. A bipolar bit-slice processor handles digital write functions. In 1000s, the price is $7500 each. **Kennedy Co,** 1600 Shamrock Ave, Monrovia, CA 91016. **Circle 283**

### Add-in memory board for VAX

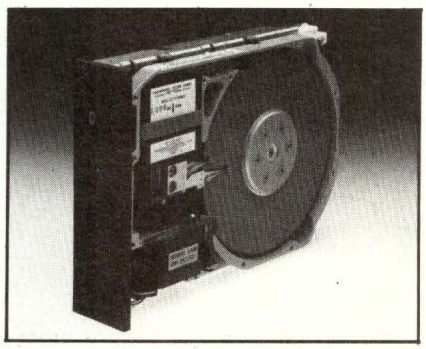
The MK8076 is a direct replacement for the DEC M8750 memory board and features a 1-Mbyte storage capacity. It uses 64-Kbyte dynamic RAMs (5-V only) that are upgradable with 256-Kbyte DRAMs. Other features include a data transfer rate of 39 bits (32 data and 7 ECC), an on/off-line switch, and three LEDs. The board also supports battery backup operation. Single quantity price is $2450. **Mostek Corp, sub of United Technologies Corp,** 1215 W Crosby Rd, Carrollton, TX 75006. **Circle 284**

### Disk cache PC system

Containing RAM that ranges from 128 Kbytes to 1 Mbytes, Quick Disk is an external add-on memory device. It operates 120 times faster than a Winchester and 190 times faster than a floppy when performing common data transfers. It also features dynamic error correction and can be used independently as an additional data storage unit or in combination with a floppy or Winchester as a disk cache. Five models are available that range in price from $2795 (128-Kbyte version) to $8585 (1-Mbyte version). **Santa Clara Systems,** 1860 Hartog Dr, San Jose, CA 95131. **Circle 285**

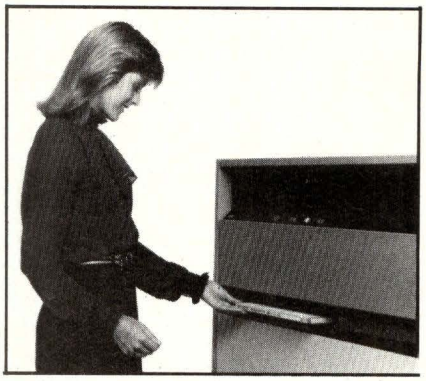
### Half-high 5¼-in. Winchester

The 12-Mbyte ST212 drive improves shock protection with low mass mini-slider ferrite R/W heads. It is fully compatible with the standard-height counterpart. Average access time is 65 ms. Track densities are 550 tracks/in. The drive has a total of 612 tracks per surface, divided into two 306-cylinder bands. It is configured with one oxide-coated disk and four R/W heads (two per surface), each of which addresses 306 cylinders. Price is $690 in lots of 1000. **Seagate Technology,** 920 Disc Dr, Scotts Valley, CA 95066.



**Circle 286**

### Optical storage subsystem



The 7600 is particularly suited for applications requiring large amounts of accessible data. It stores 4 Gbytes of data on the surface of a single optical platter. Data transfer rate between host computer and storage unit is 3 Mbytes/s. The subsystem consists of optical storage unit, media unit, storage control unit, and optical storage access software. It is compatible with IBM 370, 4300, 30XX, and others running under MVS/SP 1.3. **Storage Technology Corp,** 2270 S 88th St, Louisville, CO 80028.

**Circle 287**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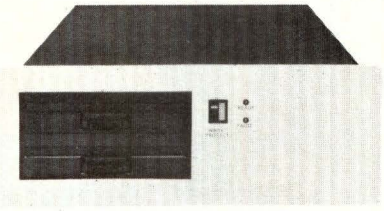
DEC USERS



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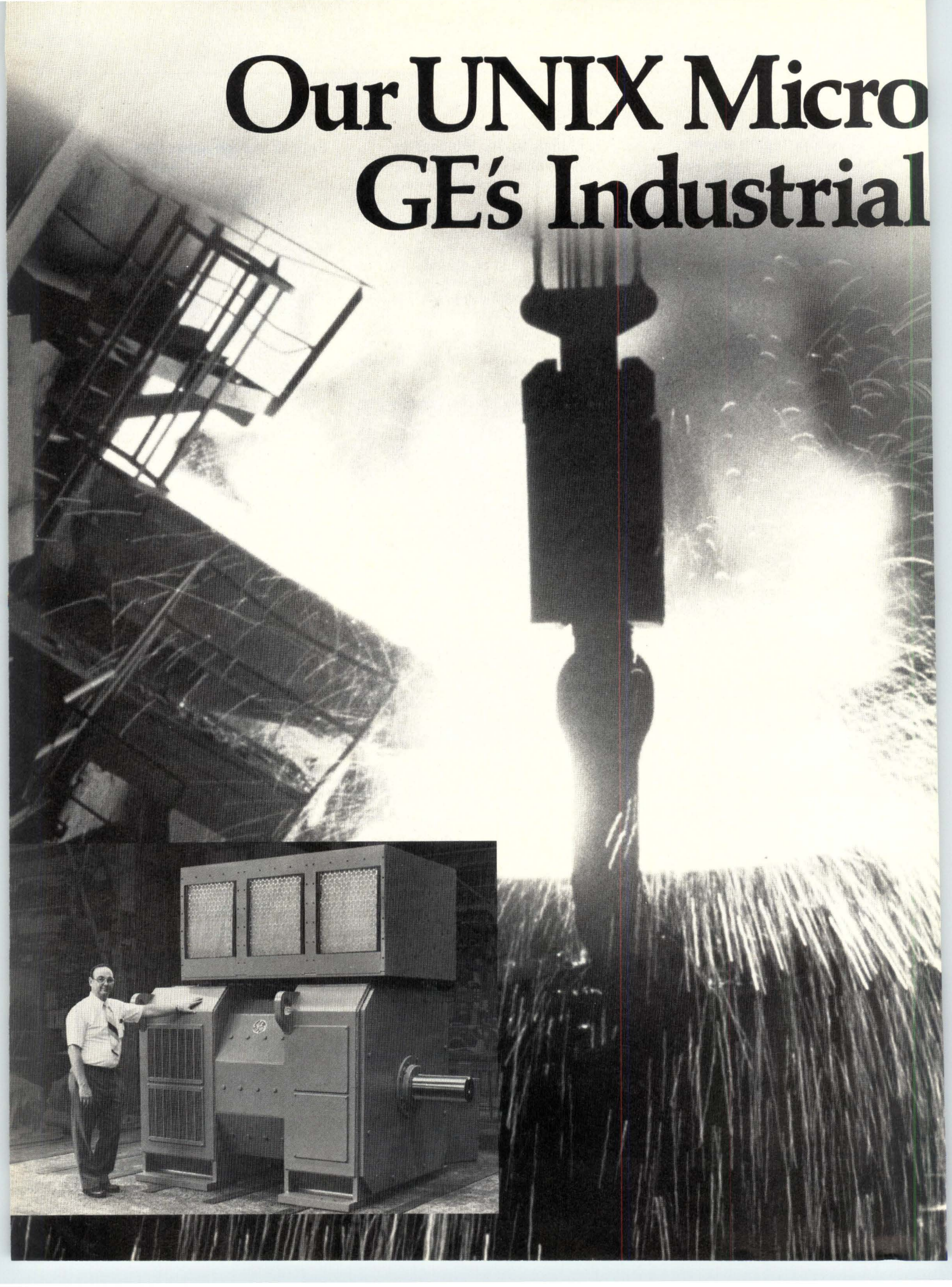
# Our UNIX Micro
# GE's Industrial



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And for three years we've been delivering 68000-based systems, full UNIX* Version 7 with Berkeley enhancements, and IEEE-696/S-100 bus conformance. That's longer than anyone else.

Which brings us to our newest high-performance micro, the 83/80. Featuring the full UNIX capabilities of Version 7 or System III, the 83/80 can handle up to twelve users and provides a standard 512 KB of dynamic RAM with parity that's expandable to 3.25 MB.

And we've backed it with a full one-year warranty.

Our 83/80 incorporates a high-throughput SMD controller and an 80 megabyte Winchester disk drive with 20-25 milliseconds average seek time. And our backup memory is well worth remembering — it consists of an 8" floppy disk with 1 MB of storage.

In addition, you'll find our 83/80 delivers increased performance through its Dual ported full-track disk buffer and proprietary controller circuiting. More users can access with better response time.

It's also very well-educated. Our 83/80 can read or write up to an entire track of data in a single disk rotation, regardless of where the disk-head settles on a given track.

That's smart.

The C programming language comes standard with UNIX, of course. Other optional languages include FORTRAN-77, PASCAL, RM/COBOL®, LISP and BASIC. And that's just for starters.

Optional software includes data base and administrative packages like INGRES and UNIFY.

And the sticker price? Quantity 10 at $14,693.

For further information, please write or telephone our Marketing Department at 415/549-3854.

We'll be glad to tell you about one powerful microsystem that's revved up and ready-to-go.

DUAL

Dual Systems Corporation
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Berkeley, CA 94702

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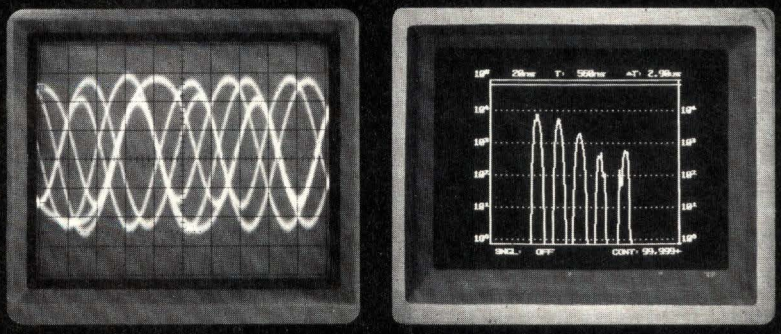
CIRCLE 67

### Dual-port RAM board

Multibus and Sam-Bus compatible, the Sam-DPRAM allows simultaneous access of the memory bank through either bus. It has a typical access time of 250 ns and a maximum cycle time of 350 ns. Memory capacity can range from 128 Kbytes to 2 Mbytes. Parity checking detects any single-bit errors, then the CPU reads input ports to determine the physical address of the error. Both buses provide a 24-bit addressing range for 16 Mbytes of addressing capability. The board costs $2400. **SGS USA,** 1000 E Bell Rd, Phoenix, AZ 85022.
**Circle 288**


Frustrated with eye patterns?
Time interval analysis advances from



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Bringing science to time interval analysis.


## INTERFACE

### Cluster controller

The 4970 enables ASCII graphics terminals to operate in IBM environments. Together with communication software, the controller connects Tektronix terminals to the SNA as if they were IBM 3270 type terminals. It supports up to four async devices on a single polled sync line with transmission rates up to 9.6 kbits/s. Software provides terminal to host communications with SNA network compatibility and SDLC protocol. Other features include error-free transmission with auto error recovery. Price is $6200. **Tektronix, Inc,** PO Box 500, Beaverton, OR 97077.
**Circle 289**

### Parallel interface card

Designed for the STD bus, the DSTD-408 is compatible with the QIC-2 ¼-in. tape interface protocol. A Z80 DMA controller chip gains transfer speeds up to 88 Kbytes/s required for the 90-in./s streaming tape drives. It features an 8-bit data bus with a 9th parity bit. Seven control signals plus two handshake signals are supported. Both 2.5- and 4-MHz versions are available. Pricing is $225 in quantities of 100 or more. **Dy-4 Systems Inc,** 888 Lady Ellen Pl, Ottawa, Ontario, Canada K1Z 5M1.
**Circle 290**

### Controller for STD bus

Model M/E200 features two RS-232 serial ports with software selectable independent baud rates. It has true EIA levels on transmit data, receive data, clear to send, and data terminal ready. Three 28-pin byte-wide memory sockets provide space for onboard EPROM and RAM. Memory can switched out in software for boot-up to RAM-based disk based operating system. DIP switch selects GPIB address and options. Interface board costs $390. **Mitchell Electronics,** Rte 4, PO Box 39, Athens, OH 45701.
**Circle 291**

### Network software

Liaison family includes an operating system, device servers, and development tools. Features include hardware independence, sharing of programs and data, as well as disks and printers. Networks are peer to peer and each workstation functions as an independent self-contained node. The software provides various services: locator, to find nodes in the network and establish connections; channel, to handle two-way, point-to-point communication; and socket, to provide best-effort transmission. **SofTech Microsystems, Inc,** 16885 W Bernardo Dr, San Diego, CA 92127.
**Circle 292**

### Software for 68000

Designed to support applications development on the 16-bit 68000, Microbench software includes a relocating assembler, linking loader, librarian, and object file formatter. Assembler is source compatible with 68000 assembly language, supports macro and conditional assembly capabilities, cross-reference listings, and a macro library. Object-file formatter produces binaries in compatible formats to use with PROM programmers and emulation systems. Perpetual license fees start at $2200 including documentation. **Virtual Systems, Inc,** 1500 Newell Ave, Walnut Creek, CA 94596.
**Circle 293**

### Language for scientific computing

DEQSOL stands for differential equation solver language, designed for numerical simulation applications. It uses array processors, a DEQSOL translator, and a Fortran translator program. The software reduces the number of lines in a program and decreases the computing time required by array processors. The language consists of 20 parameter instruction commands. The translator is written in Pascal and is about 25,000 lines long. **Hitachi America, Ltd,** 1800 Bering Dr, San Jose, CA 95112.
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Version 4.0 increases virtual address space, improves user security, and introduces DEC RT-11 compatibility. The operating system creates a multi-user, multitasking RT-11 environment. It addresses up to 4 Mbytes of main memory on PDP-11 systems that have either the extended Unibus or the 22-bit Q-bus together with the PDP-11/23 CPU. Software supports up to eight logical disks per user, and each user has eight distinct files arranged either hierarchically or in parallel. TSX-PLUS costs $2000; an annual $500 fee buys support and the option to order upgrades. **S&H Computer Systems, Inc,** 1027 17th Ave S, Nashville, TN 37212.
**Circle 295**

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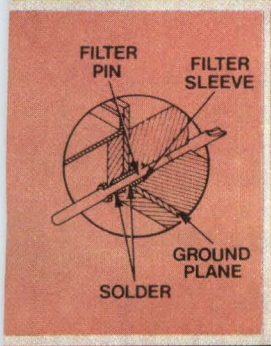


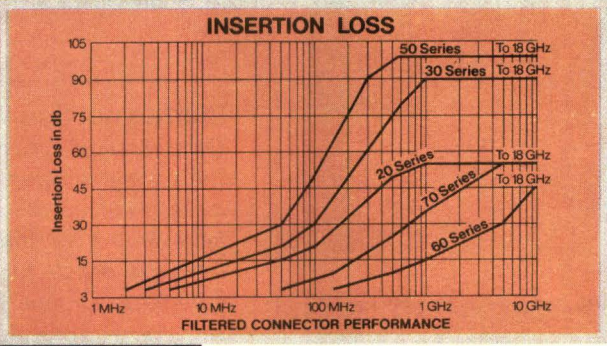


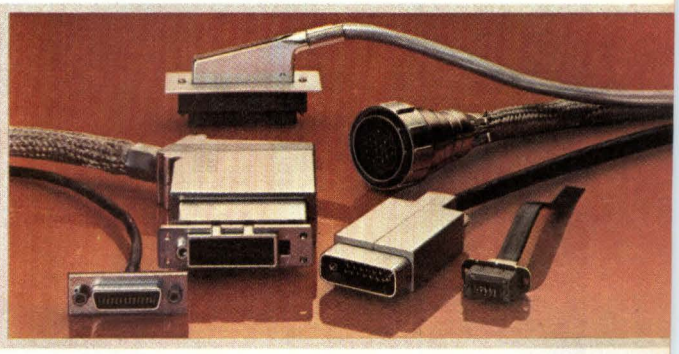

You can choose the insertion-loss vs. frequency characteristics you need.

CIRCLE NUMBER 10

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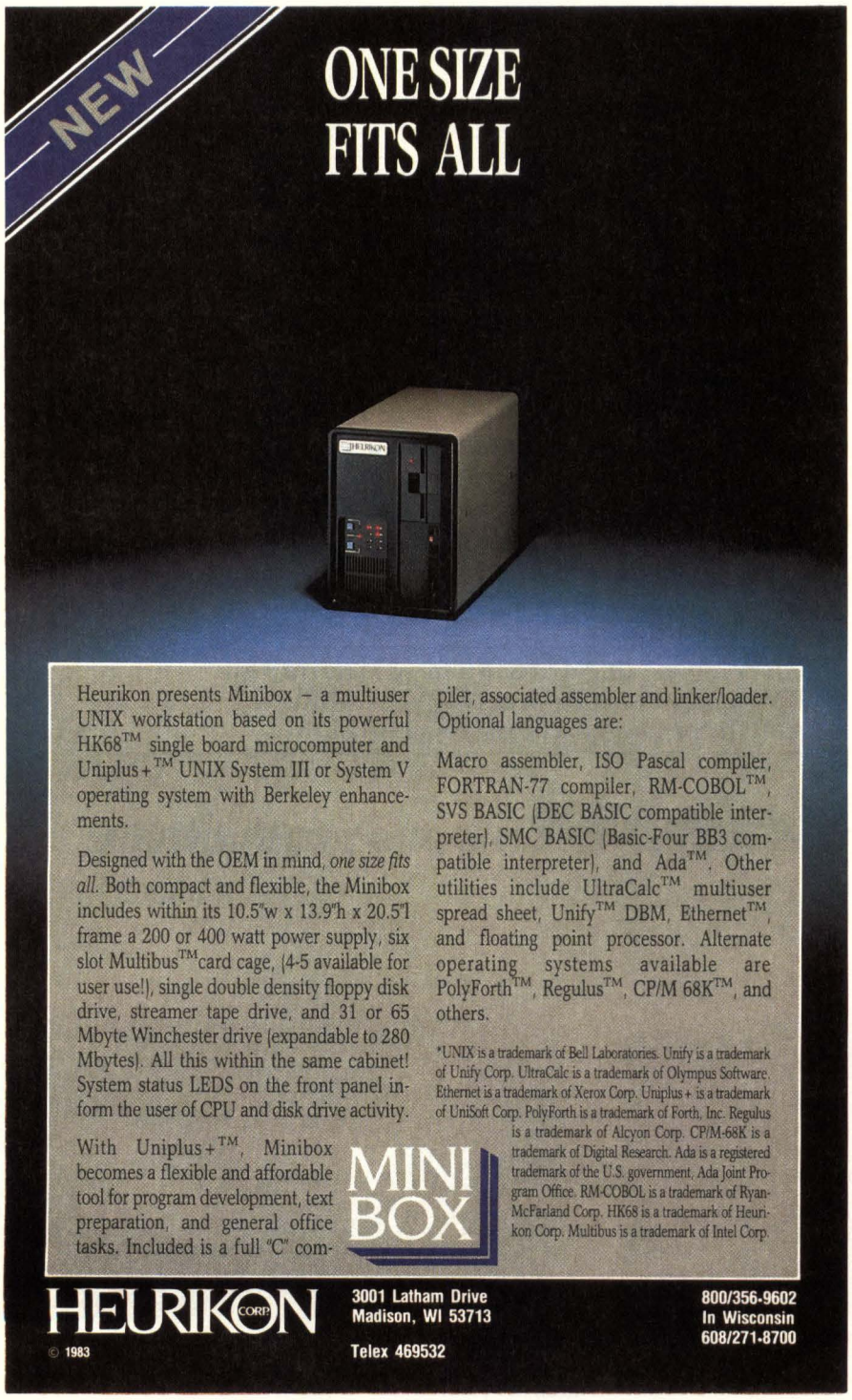
### Micro/mainframe software link

Solving the problems of overloaded IBM mainframes, slow terminal response time, and mainframe downtime, the m3278/SPF combines mainframe communication with local computing power. Communication occurs with the PCOX communication board and CXI software. It emulates the 3278 and implements the complete micro/SPF software. This software provides a full-screen text editor. A parameter specification option redefines program function keys and a browse option allows full scroll in all directions. **Phaser Systems, Inc,** 24 California St, San Francisco, CA 94111. **Circle 296**



### Expanded graphics capabilities

Subroutines and utilities for developing hardware-independent microcomputer graphics applications make up the GSS-toolkit. A kernel system following the GKS syntactical protocol addresses lower level graphics primitives. When used with GSS-drivers software, the system can be graphic-ported across machines running the MS-DOS operating system. A plotting system helps to create charts, and a window manager helps develop multiple viewports. **Graphic Software Systems, Inc,** 25117 SW Parkway, Wilsonville, OR 97070.
**Circle 297**

### Transportable compilers

Fortran and C compilers are fully transportable from workstation to supermini. The Fortran VII for edition VII workbench is source-coded compatible with all OS/32 Fortran system compilers. It is possible to develop and test programs in a realtime environment for optimum runtime performance. The C version is an optimizing compiler that takes advantage of the Series 3200 architecture for fast application processing. C version is priced from $3400 to $7000, while the Fortran version is $3400. **Perkin-Elmer Corp, Data Systems Group,** 2 Crescent Pl, Oceanport, NJ 07757.
**Circle 298**

### Cross compiler in C

Hosted on the VAX under Unix, the compiler targets the 68000 CPU. The package includes 68000 compiler, assembler, linker, and full runtime library. It features a C processor, 32-bit pointers, data intitialization, absolute load maps, and global symbols listing. For realtime applications, it features tightly generated ROMable code. The compiler makes five passes, yet is time competitive with other compilers. **The Destek Group,** 830 E Evelyn, Sunnyvale, CA 94086.
**Circle 299**

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*Other system designers face the same problems you've already solved. You could help them by writing a technical article for Computer Design. For a free copy of our Author's Guide, circle* **500** *on the Reader Inquiry Card.*

### Transferring files PC to mainframe

When used with protocol converters, FileLynx/3278 makes the IBM PC or PC compatibles emulate an IBM 3278-2 terminal. All function and cursor keys are supported. Users can transfer an entire file to or from the mainframe automatically and a variable number of lines per screen can be transferred. A user-friendly configuraton mode stores all parameters. Software supports several auto-dialing modems. It requires a minimum of one serial card, 64 Kbytes of memory, and any PC-DOS version. Price is $200. **Local Data,** 2701 Toledo St, Torrance, CA 90503.

**Circle 300**

### Micro program for system design

Tutsim is a block diagram oriented simulation program for continuous dynamic systems. Users can build models from engineering equations or describe their system with approximately 40 types of program block elements. To enter the program block, users specify parameters in line format. The program then does a model simulation. Output is graphic or numerical, and most parameters can be changed by one or two line commands. Micro versions range from $475 to $574. **Applied i,** 200 California Ave, Palo Alto, CA 94306.

**Circle 301**

### Software debugger for 68000

Probug allows the user to print and alter memory and registers; copy, fill, and search memory; assemble and disassemble instructions; and control program execution. The debugger/monitor downloads programs from and writes programs to a host computer, and boots a disk operating system. The user can set observation points to halt program execution when a specified memory location changes. A user manual comes with the 16 Kbytes of firmware. Price is $250. **SBE, Inc,** 4700 San Pablo Ave, Emeryville, CA 94608.

**Circle 302**

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# Mouse Controls
## Cursor Control The Easy Way

They operate on any surface. They're easy to use. And they're durable.

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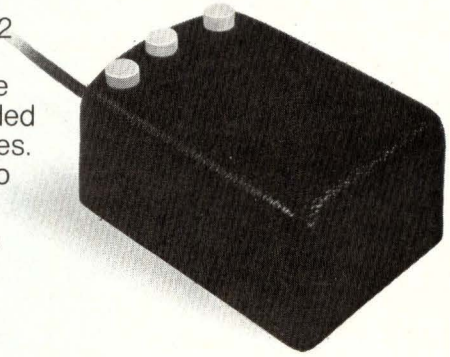
Once you've seen these controls in action, you'll be a confirmed mouseketeer, too. Contact us for more information.



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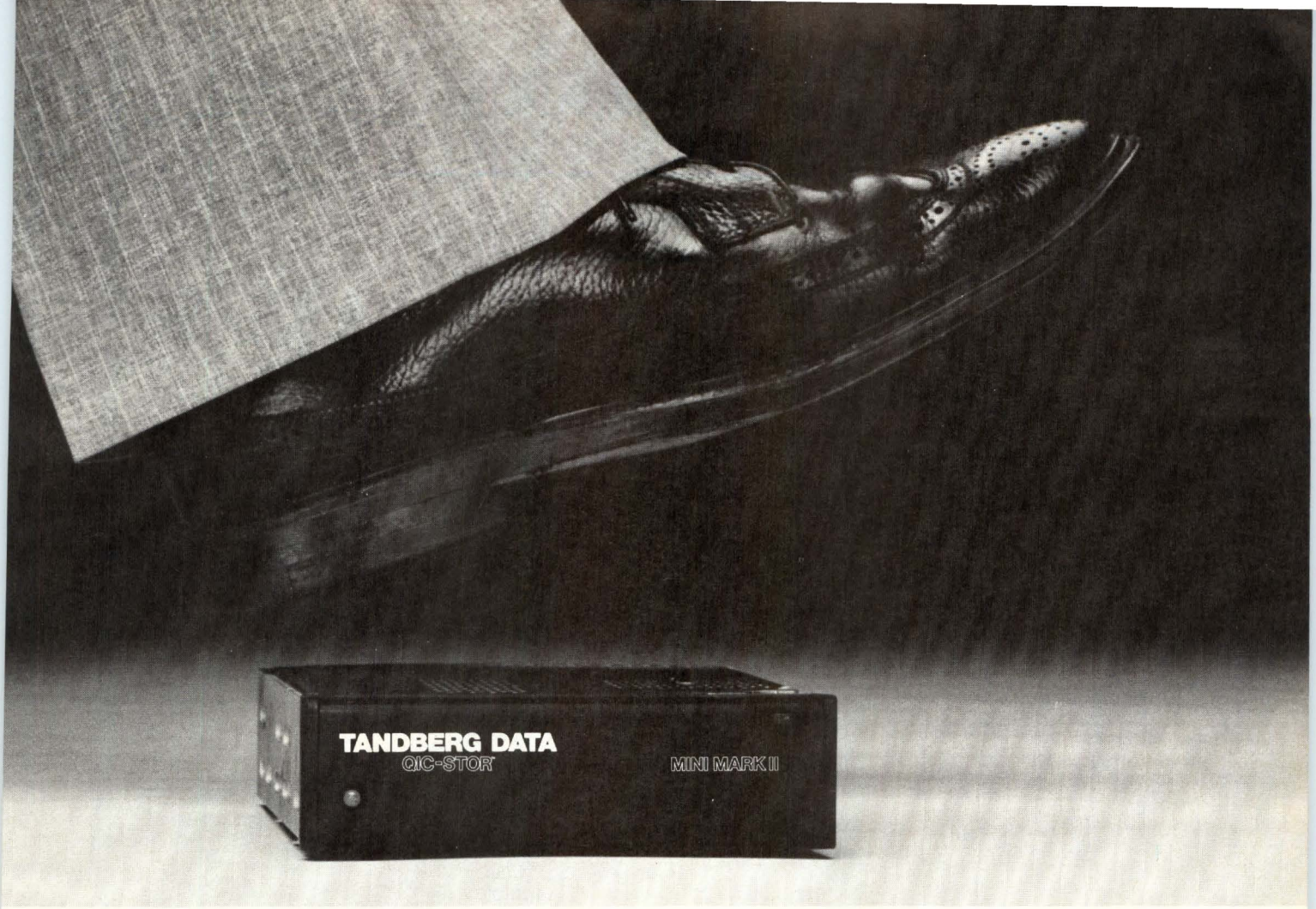
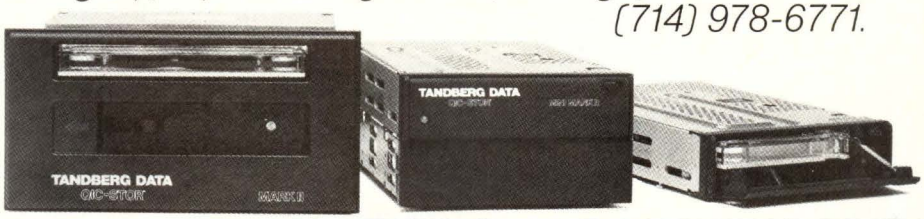
# TANDBERG DATA TAKES THE NEXT STEP.




*The first step, if you remember, was the introduction of our QIC-02 8," four- and nine-track tape drive. This ¼" streamer set new standards for data integrity and accuracy. (You can actually stand on one.)*

*Our next step, the QIC-STOR™ Series, finally brings 100% QIC-compatibility to the ¼" streamer market. And now with QIC-02 and QIC-24, our newly announced Mini-Mark II™ packs incredible performance and reliability into a half-high 5¼" form factor. It has all the best features of our new 8" Mark II,™ including precise track locating and rugged cartridge locking/loading to totally eliminate the machine interchangeability problems that have plagued the industry. You get all this, plus capacities of up to 60 megabytes on a single ¼" tape cartridge!*

*We've stepped up our facilities and capabilities too, just to keep up with demand. But that's another story. If you'd like the full story on our growing lineup of QIC-STOR streamers, you'll have to take the next step and contact Tandberg Data, Inc., DATA STORAGE DIVISION, 571 North Poplar, Suite H, Orange, CA 92668. (714) 978-6771.*



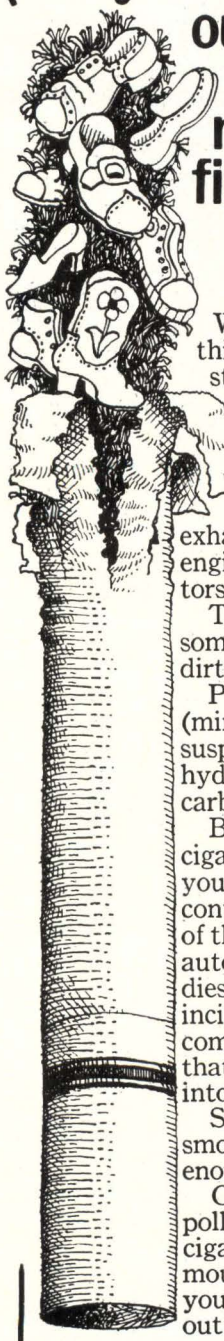

**TANDBERG DATA**

*QUALITY IN EVERY BIT.*

CIRCLE 138

# If you're going to gripe about the quality of the air you breathe,

# at least take your cigarette (and your foot) out of your mouth first.



When you think of the stuff that makes air dirty, you think of auto exhaust, diesel engines, incinerators; right?

They contain some pretty bad dirt-makers like: Particulates (minute solids suspended in air); hydrocarbons; carbon monoxide.

But the cigarette smoke you inhale contains more of this stuff than auto exhaust, diesel engines and incinerators combined. And that's straight into your lungs.

So you see, smoking is dumb enough.

Griping about pollution with a cigarette in your mouth can get you laughed out of town.

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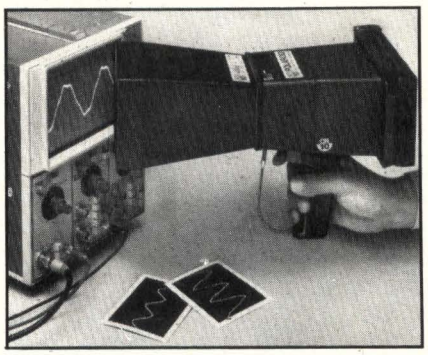
## Instant camera for CRTs



A versatile, handheld camera takes pictures of displays in industrial, scientific, and security applications. The CR-10 model 33-30 shoots 3¼-in. x 4¼-in. instant film, black and white, or color. Interchangeable hoods size images from various scopes and CRT screens. A built-in supplementary lens in each hood matches image magnification to film size. The camera costs $349; hoods are $49 each. **Polaroid,** 575 Technology Sq, Cambridge, MA 02139. **Circle 303**

## Advanced ASCII terminals

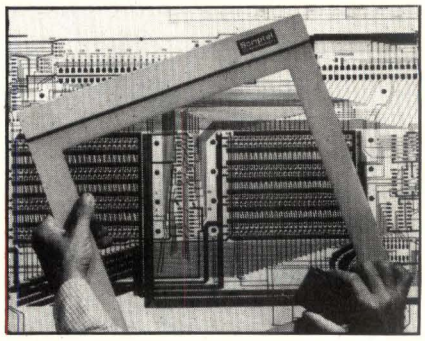
The VT200 family offers three models that will have full VT100 emulation capabilities. The VT220 is a two-piece monochrome text unit. The VT240 has all the text features of the 220 plus bit-mapped graphics. The VT241 has all the features of the 240 and, in addition, a color display. This version offers an optional integrated modem that features auto-dial and auto-answer. Monitors include reverse video and character highlighting, and function keys are programmable. Prices range from $1295 to $3195 depending on model. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754.
**Circle 304**

## Band printers

Estimated mean time between failure for the M304X series is 4000 hours at 1200 lines/min and 6000 hours at 600 lines/min. Forty-eight-character models print 390, 750, 1090, or 1300 lines/min, while 64-character models print 300, 900, or 1200 lines/min. Standard features include type-band exchange and auto-identification of four print bands. The operator's panel indicates errors detected automatically. Each model comes with a Centronics, Dataproducts, or RS-232-C interface. In quantity, the 1200-line/min model costs below $8000. **Fujitsu America, Inc,** 3075 Oakmead Village Dr, Santa Clara, CA 95051.
**Circle 305**

## Graphics tablet

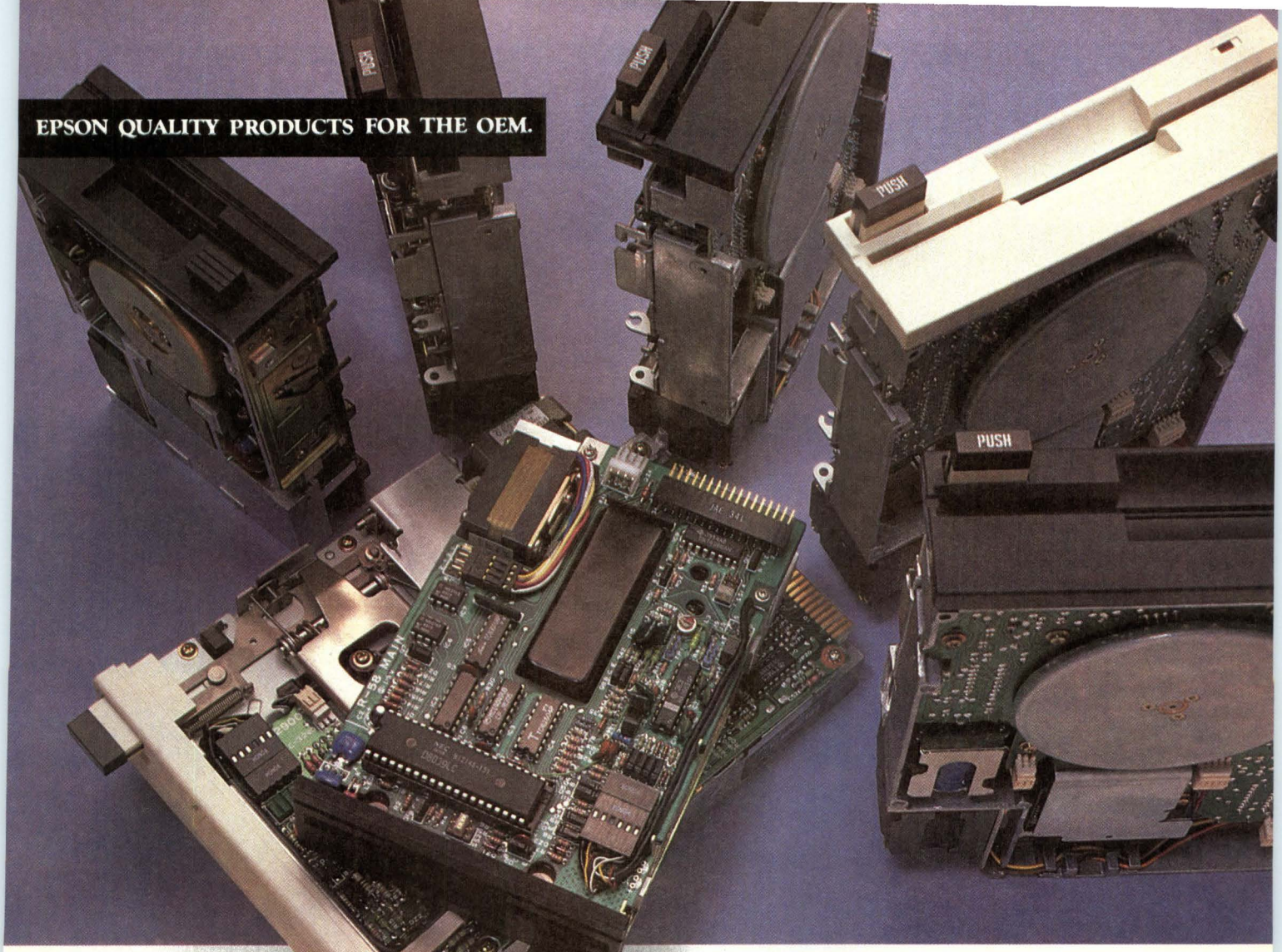
The Pen Pal has a 100 percent transparent writing surface so ther user can place menus, artwork, and drawings under the digitizer. Sizes range from 6 x 6 in. to 24 x 36 in. and are accurate to better than 1 percent, with resolution better than one mil. Speeds can be obtained to 1000 coordinate pairs/s. It is unaffected by stray emi or rfi fields and never requires magnetic biasing. Low power operation allows the use of cordless pens and cursors. **Scriptel Corp,** 3660 Parkway Ln, Hilliard, OH 43026.
**Circle 306**



## Enhanced display terminal

The ET 100B emulates the VT100 series, including advance video option, identical keyboard layout, and printer port. None of the features require software changes. In addition, the terminal provides 16 user programmable function keys, easy to use menu setup mode, and audio signal that indicates data received. DIN standard as well as other international keyboards are available. **TEC, Inc,** 2727 N Fairview, PO Box 5646, Tucson, AZ 85703.

**Circle 307**

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|---|---|---|---|---|---|---|
| MEDIA SIZE | 3½" | | 5¼" (1/2 High) | | | 5¼" (1/3 High) |
| | 4" x 1.57" x 5.98" | | 5.75" x 1.6" x 7.68" | | | 5.75" x 11" x 9.27" |
| Max. Capacity (2 Sides) (Unformatted) | 500 KB | 1000 KB | 500 KB | 1000 KB | 1604 KB | 500 KB |
| Drive Motor Speed | 300 RPM | 300 RPM | 300 RPM | 300 RPM | 360 RPM | 300 RPM |
| Track Density | 67.5 TPI | 135 TPI | 48 TPI | 96 TPI | 96 TPI | 48 TPI |
| Access Time | 6 msec | 3 msec | 6 msec | 3 msec | 3 msec | 15 msec |

Extraordinary is the best word we could find to describe the new Epson family of 3½" and 5¼" floppy disk drives. Because there is nothing ordinary about them.

The 3½" drives, for instance, feature two-sided capacities up to 1MB. And some draw so little power they can operate on batteries.

The half-height 5¼" drives offer capacities from 500KB to 1.6MB and access times down to 3 msec. And the one-third height 5¼" drive is the industry's slimmest.

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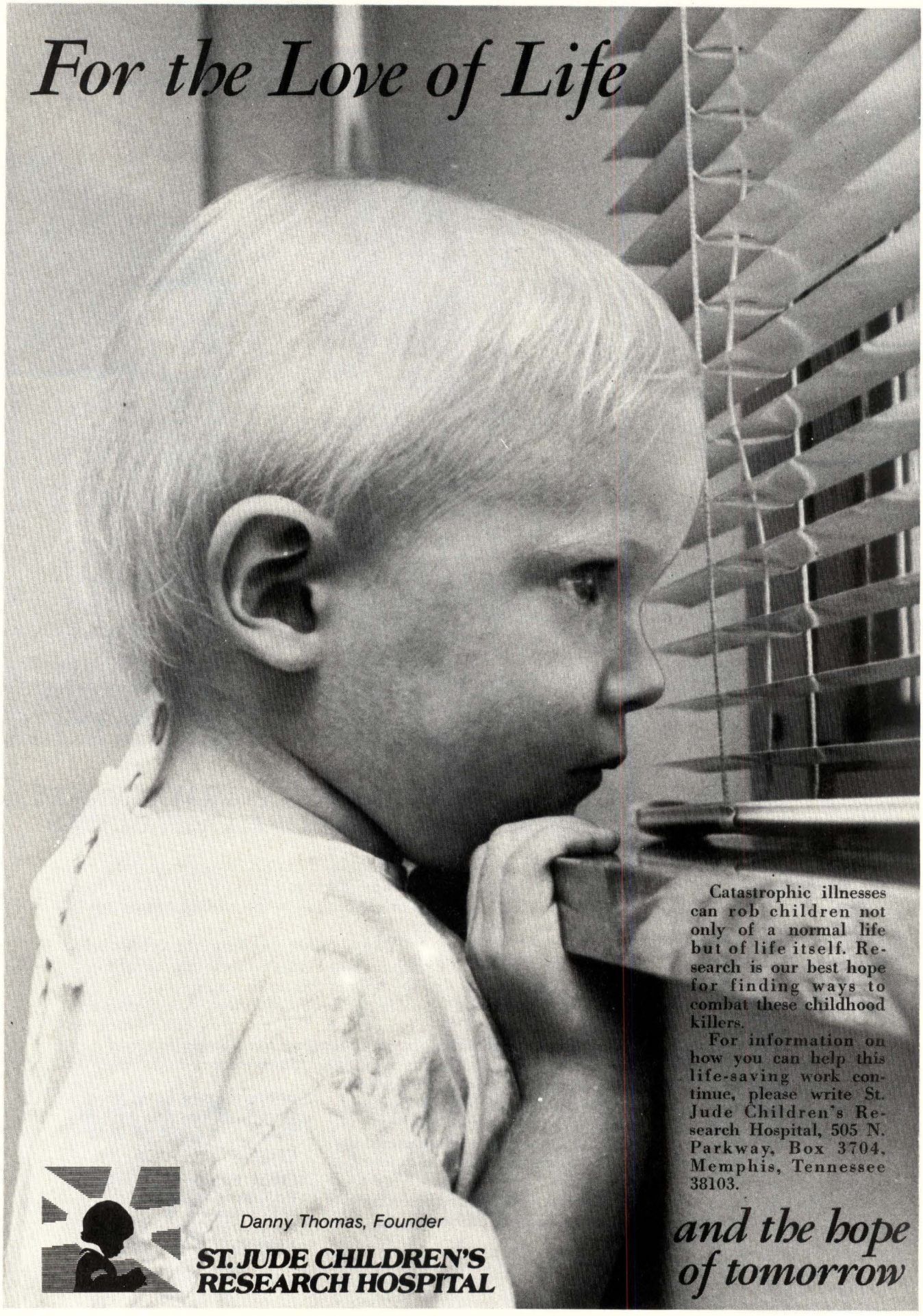
CIRCLE 127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### Plotters and hardcopy unit

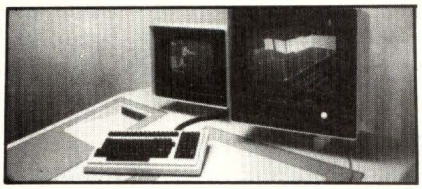
The online electrostatic plotter produces an E-sized, full-color plot in 8 min. Sixty-four line codes and fill patterns create 256 color patterns in four colors. A color pen plotter features a high speed writing system for graphics. Fiber tip or liquid ink draft pens plot up to 24 in. of graphic data/s. The color hard copier produces A-sized copies directly from design stations without host support. Copies are made with oil-based ink in a thermal ink transfer process. It makes 99 copies unattended, and downloads screen images from a video device in about 0.5 s. **Calma Co,** 2901 Tasman Dr, Santa Clara, CA 95050. **Circle 308**

### Color graphics terminal

The 6411 comes with a desk-side console, a 19-in. monitor, and a keyboard. In the basic configuration, it has four refresh memory planes, and allows simultaneous display of 16 colors chosen from a palette of 4096. With the addition of four optional refresh memory planes, 256 colors from a palette of 16 million can be displayed, as well as shadows and dimension, in solid objects on the screen. Display resolution is 1280 x 1024 pixels, and can be zoomed in integer steps between 1:1 and 16:1. The system costs $14,995. **Ramtek Corp,** 2211 Lawson Ln, Santa Clara, CA 95050. **Circle 309**

## DEVELOPMENT SYSTEMS

### Low price CAD system



Based on Data General's Desktop Generation, ICON features software to create, preview, edit, store, and recall graphics. Available in single- and dual-user configurations, each workstation has an integral digitizer with menu and two tilt and swivel monitors. The display measures 19 in. with 1280 x 1024 resolution. Complete application packages include programs for PC board design, mechanical and electrical design, and word processing. Price per station in a four-workstation configuration is $37,250. **Summagraphics Corp,** 35 Brentwood Ave, PO Box 781, Fairfield, CT 06430. **Circle 310**

### Custom RAM/ROM cells

A standard-cell technique creates custom VLSI circuits with onchip RAM and/or ROM tailored to specific requirements. Designers enter only macro definitions of memory size and organization. The zyP system automatically generates both the artwork and the simulation model. Construction occurs by assembling body, control, and end-cap cells. Each cell type comes in 32-, 64-, and 128-bit deep configurations for RAM, and 512-, 1024-, and 2048-bit configurations for ROM. **Zymos Corp,** 477 N Mathilda Ave, PO Box 62379, Sunnyvale, CA 94088. **Circle 311**

### Monochrome graphics terminals

The IGT-1000M series features a 15-in. raster scan screen with P-39 green phosphor and 1024- x 780-pixel resolution. The terminal emulates Tektronix 4010 series with Plot 10 software compatibility plus commands to draw rectangle, arc, and circle. Images can be selectively erased or blinked, and a closed polygon filled. Options include 17-in. and 20-in. monitors, 1024 x 1024 resolution, tablet and lightpen input for high speed menu selection, and cursor control. Unit price is $3995. **Infocom Systems Inc,** 6001 Gulf Fwy, Houston, TX 77023. **Circle 312**

### Mid-range graphics system

The 19-in. color raster Whizzard 3355 offers 2-D graphics, 1024- x 1024-pixel resolution, and realtime dynamic transforms. A 12-bit (4096 x 4096) virtual addressing system accesses the memory mapped display pixel by pixel. Architecture is based on a dual-bus graphics engine with host computer interface, 32-bit graphics processor, and local processor. The system is $22,500. **Megatek Corp,** 9605 Scranton Rd, San Diego, CA 92121. **Circle 313**

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**CIRCLE 121**

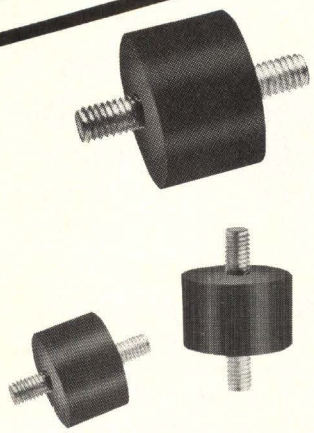
### In-circuit emulator

The Mice-II line's 68008 model program development/debugging system operates standalone or together with a computer system. Its 68008 micro lets the user run the target 68008 micro system transparently in realtime with no wait states and using no memory space. It features two hardware breakpoints, resident assembler/disassembler, realtime forward/backward trace up to 2048 cycles, and a 32-Kbyte emulation memory expandable in 32-Kbyte segments. Unit is $3995. **MicroTek Lab, Inc,** 17221 S Western Ave, Gardena, CA 90247. **Circle 314**

### Realtime 8086/88 development

Sphere ROM-based software system combines the functions of operating system, multitasking executive, high level language, native assembler, and development tools in one package. Using only 16 Kbytes of ROM, 2 Kbytes of RAM, and a terminal port, it provides complete tools for designing, coding, testing, and implementing realtime applications. Time critical routines can be written in the native assembler of the target micro, then mixed with HLL code for maximum realtime performance. Prices start at less than $3000. **Infosphere, Inc,** 4730 SW Macadam Ave, Portland, OR 97201. **Circle 315**

VIBRATION ISOLATORS



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CIRCLE 119



### Data acquisition of PC

Sample and hold system DT2818 provides simultaneous analog I/O capabilities as well as digital I/O and clock functions. Analog input throughput rate is up to 27,500 samples/s. The user can take a snapshot of up to four high-level analog input channels, freezing their values instantaneously within ±5 ns. Also included are two 12-bit D-A converters, two 8-line digital I/O ports, and an onboard programmable clock for scanning inputs or for multiple output conversion. Single unit price is $1585. **Data Translation,** 100 Locke Dr, Marlboro, MA 01752. **Circle 316**

### Digital dc servo controller

Micro-based FPC-1800 interfaces to any computer, micro, or standard bus protocol. Controller/computer link consists of 8 bidirectional bus lines, plus read, write, and chip select control. Point-to-point positioning and damping are both programmable. Instruction set commands control accurate system positioning within ±8 million counts from a home reference, stepping a programmed number of counts, moving at a constant velocity, and moving to home or seeking a limit switch. Unit is $735 in 100-piece quantities. **Finell Systems, Inc,** 1190-S Mountain View-Alviso Rd, Sunnyvale, CA 94089. **Circle 317**

### Measurement and control system

With micro, realtime software package, Fortran or Pascal high level language, and networking capabilities, the Control/1000 is designed for industrial automation. Applications include process control, machine automation, and control with a medium to high sensor point count. The micro has a 1-MIPS CPU and 512 Kbytes of memory. Software reduces much of the protocol needed to communicate with function cards. Prices range from $25,000 to $150,000 depending on point count. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303. **Circle 318**

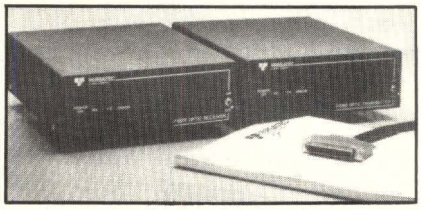
**February Preview**
*Watch for a special article on microprocessors*

### Chip program for scanning

A Basic program on a PROM, Autoscan is designed for automatic stop-flow peak scanning, absorbance ratio determinations, and time-programmable wavelength changes. It is intended for use with a variable wavelength detector together with an HPLC system and a computing integrator. The firmware-based system eliminates loading programs from auxiliary storage devices. Applications include confirming the indentity and purity of chromatographic components and determining the optimum monitoring wavelength for an analysis. **Spectra-Physics,** 3333 N First St, San Jose, CA 95134. **Circle 319**

## DATA COMMUNICATIONS

### Fiber optic modems



Modems enable online electrostatic plotting up to 2 miles (3 km) from a host computer without repeaters. Model 410 fiber optic system (one transmitting and one receiving modem) is compatible with all Versatec controllers. No special software or protocols are required. Cables must be terminated with SMA 905/906 metallic connectors. Transmission rates exceed 132 kbytes/s and support all Versatec printer/plotters. The system costs $6000. **Versatec, a Xerox Co,** 2710 Walsh Ave, Santa Clara, CA 95051. **Circle 320**

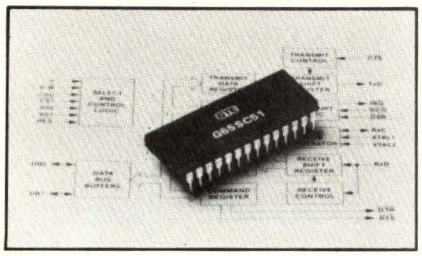
### Small computer LAN

An intelligent Ethernet compatible network interface unit allows PC users to share information and resources. The plug-in board features SNA gateways allowing access to mainframe-based application programs. It also features a shared disk and print servers. The disk server manages the shared access to all files and application programs stored on one or more Winchesters at the server station. Diskshare software provides multilevel password protection. The $850 unit includes MS-DOS networking commands on a 5¼-in. diskette. **Ungermann-Bass, Inc,** 2560 Mission College Blvd, Santa Clara, CA 95050. **Circle 321**

### Programmable logic sequencer

By directly replacing the 16R8 PAL, the 82S159 can replace more than two dozen small and medium TTL circuits. The chip is organized as 16 x 45 x 12 with 16 inputs, 45 product terms, and eight registered plus-four combinatorial outputs. Nickel-chromium fuse links on AND/OR gate arrays allow field programming sum-of-products logic. Eight onchip registers permit dedicated or program-controllable flipflop configuration to either T, JK, or D operation. In plastic, the IC costs $11.95 (100 to 999); in ceramic, $13.25. **Signetics Corp,** 811 E Arques Ave, PO Box 409, Sunnyvale, CA 94086. **Circle 322**

### Communication interface adapter



An onchip baud rate generator in the G65SC51 allows 15 programmable rates from 50 to 19.2k baud. A single standard 1.8432 MHz external crystal achieves this performance; an external clock input handles higher baud rates. The chip has programmable interrupt and status registers, full-duplex or half-duplex operating modes, and selectable 5-, 6-, 7-, 8-, or 9-bit transmission rates. Power consumption is 11 mW at 1 MHz and 11 $\mu$W standby. Packaging options include 28-pin plastic, ceramic, or cerDIP at 1 and 2 MHz. Plastic, in 100 or more, costs $7.90. **GTE Microcircuits,** 2000 W 14th St, Tempe, AZ 85281. **Circle 323**

### Skinny static RAM

The hermetic-packaged 2-K x 8 CMOS chip offers savings in circuit board space compared with the standard-packaged 6116. The IDT6116 T DIP is a packaging alternative that features a 300-mil wide, 24-pin package. Because of circuit board space savings, the chip is useful for airborne applications. It is available in four speeds: 70, 90, 120, and 150 ns. In addition, there are two power options: standard at 200 mW and low at 20 mW. Prices are $18.20 each in 100s. **Integrated Device Technology, Inc,** 3236 Scott Blvd, Santa Clara, CA 95051. **Circle 324**

### High speed static RAM

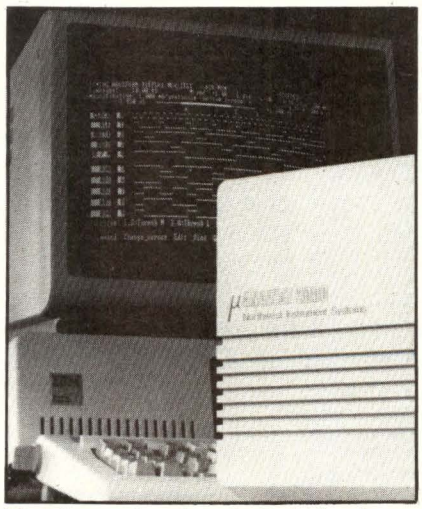
Organized as 16 Kbits x 1, the Am2167 is available in 35-, 45-, 55-, and 70-ns versions. It draws 660 mW power (active) and when deselected by a chip enable, it automatically enters a power down mode. The architecture allows applications in mainframe memories, image processing, and signal processing. All interface signal levels are identical to TTL specs. Packaged in 300-mil, 20-pin plastic, the device is $25 in 100s. **Advanced Micro Devices Inc,** 901 Thompson Pl, Sunnyvale, CA 94086. **Circle 325**

## TEST & MEASUREMENT

### Test system for VLSI

A tester-per-pin architecture makes all the test system's resources available at each pin. The MegaOne offers data rates to 80 MHz at each of 256 pins. Each pin has a timing generator, wave formatter, 1 million elements of vector memory, pin driver and comparator, programmable current load, and parametric test unit. In addition, the tester includes a computer system built around multiple 680010 processors and runs Unix Version 4.2 software. **Megatest Corp,** 2900 Patrick Henry Dr, Santa Clara, CA 95050. **Circle 326**

### Interactive timing analyzer



Model 2200 pinpoints faults in hardware during design of micro-based systems. Controlled by the IBM PC, it has 16 timing input channels with a maximum 100-MHz sample rate that uses a transitional timing mode. Trigger modes include triggering on setup and hold time violations. Transitional timing acquisition mode stores data only when a transition occurs on a specified input line or lines; counter measures the time between transitions. Virtual memory scheme permits a 128-Kbyte memory depth. The two-card set plus probes is $2995. **Northwest Instruments Systems, Inc,** PO Box 1309, Beaverton, OR 97075. **Circle 327**

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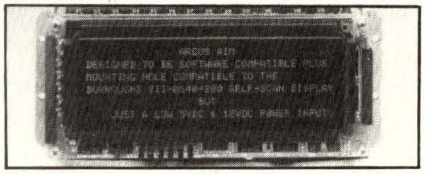
## SYSTEM ELEMENTS

### Character module



Model 3402-04-320N is a 8-line x 40-character display that requires only 5 Vdc for logic and 11 to 29 Vdc for internal power. The neon-orange characters are formed with a 5 x 7 dot matrix and the entire 96-character ASCII set is displayed. The modules have a micro-based controller that accepts parallel ASCII data from the host. Panel dimensions are 279.4 x 128.3 x 52.2 mm. Total power required is typically 16 W. Price is $624 in 100s. **Industrial Electronic Engineers, Inc,** 7740 Lemona Ave, Van Nuys, CA 91405. **Circle 328**

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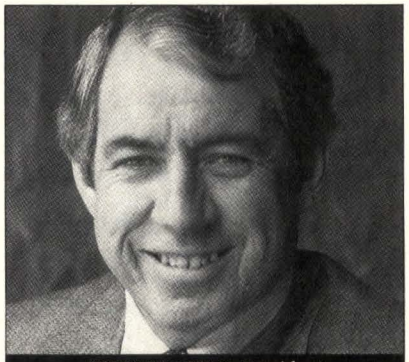

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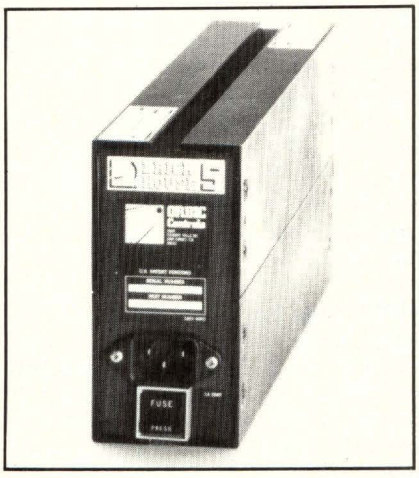
CIRCLE 129

### Multisystem timer

Timing five independent system, K-series microprocessor-based clock can be set/reset from the external system in 12 field selectable formats. Other features include four-day to six-month battery backup, 0.1-s time reads, and realtime or up/down operation. Bidirectional RS-232, RS-422, and RS-423 ports have parallel and byte-serial output. Time base can be line frequency (50 or 60 Hz) or one of several internal crystal oscillators as well as an external frequency input. **Chrono-Log Corp,** 2 W Park Rd, Havertown, PA 19083. **Circle 329**

## POWER SOURCES & PROTECTION

### Battery power at board level



Offering complete independence from line power, BrickHouse 5 provides highly regulated, uninterrupted 5-Vdc power to computers that use all-CMOS digital circuits. Circuitry allows the computer to operate normally through line-power variation, with complete protection against data loss in process or in the memory. The supply works with CMOS on STD bus, Cimbus, and COSMAC systems. Input is 90 to 135 Vac, 60 Hz; 100 to 120 Vac, 50 Hz; or 100 to 140 Vac, 400 Hz. Output current range is 1 to 5 A maximum. Prices range from $250 to $750. **Orbic Controls,** 5625 Kearny Villa Rd, San Diego, CA 92123. **Circle 330**

### Low power switchers

Using MOSFET circuitry, this line has 130 standard models ranging from one to eight outputs in three basic configurations (enclosed, base-mounted, and PC board). The International-MITE series meets safety requirements of IEC 380, VDE 0806, UL 1012, and CSA 22.2. Termination choices include AMP, Molex, barrier strip, and edge card compatible. Output voltages are 5, 9, 12, 15, and 24 V with output current at 25 A maximum. Pricing for single-output supplies at 50 W is $84. **LH Research, Inc,** 14402 Franklin Ave, Tustin, CA 92680. **Circle 331**

## MICROPROCESSORS/ MICROCOMPUTERS

### True 32-bit microprocessor

Monolithic NS32032 CPU is designed for systems that manipulate large data bases at high speeds. Features include full 32-bit internal and external architecture and high level language support, advanced operating systems, and demand paged virtual memory. The external data bus offers increased bandwidth, 32-bit registers, ALU, 32-bit internal data paths, and 32-bit displacements, The initial, 6-MHz version has a 1 MIPS rate and costs $220 each in 100s. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051. **Circle 332**

### Processor with 12-Kbyte ROM

The 8-bit TMS70120 chip stores a 12-Kbyte applications program without external ROMs, buffers, or latches. Onchip memory frees up 20 or more of the chip's individual I/O lines for flexible interfacing. In addition, the processor has 128 bytes of RAM and 64 Kbytes of address space. Other features include three prioritized interrupts, an 8-bit timer with programmable 5-bit prescaler, and a stack for control and data storage. Packaged in a 40-pin plastic DIL, the chip is $11.05 in 10,000s. **Texas Instruments, Semiconductor Group,** PO Box 401560, Dallas, TX 75240. **Circle 333**

### Single-board computers at 8 MHz

The master board (SBC 100/8M) and the slave board (SBC 100/8S) offer high throughput via the IEEE 696/S-100 bus. Each board contains a Z80H central processor with 64 to 512 Kbytes of RAM, bank selectable in 8-Kbyte segments. Support chips include DART for two serial ports, 4 to 32 Kbytes of EPROM, and an optional math coprocessor. The slave features a 4-Kbyte static RAM buffer for high speed 8- or 16-bit bus transfers. Standard boards (128-Kbyte RAM) are priced at $995 for the master and at $895 for the slave. **Sierra Data Sciences, Inc,** 25700 First St, Westlake, OH 44145. **Circle 334**

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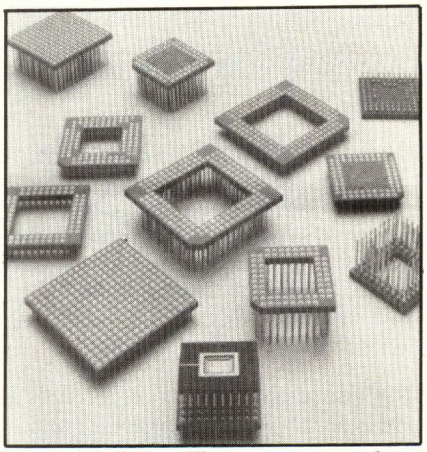
CIRCLE 120

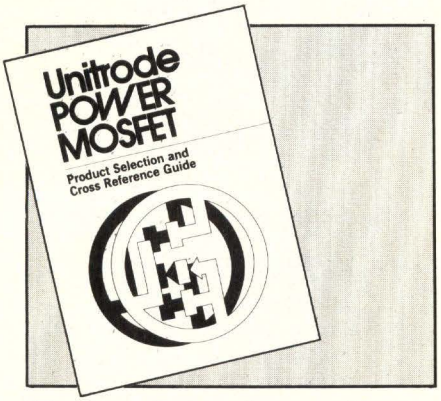
## INTERCONNECTION & PACKAGING

### Grid array sockets



Beat-treated beryllium copper sockets with gold plate come in 25 configurations, solid or open. Outer sleeves are screw machined brass with tin or gold plate. Terminations accept printed circuit or two- or three-level wirewrap. Precision-machined inner contact features four-finger wiping action and low insertion force (80 g per IC pin). Glass-reinforced body is molded thermoplastic polyester. **Mupac Corp,** 10 Mupac Dr, Brockton, MA 02401. **Circle 335**

### Power MOSFETs




Selection and cross-reference guide separates devices by package, voltage, current rating, and $R_{DS(ON)}$ to expedite match of product to application; over 700 power MOSFETs are listed. **Unitrode Corp,** Lexington, Mass. **Circle 410**

### Applying rms-to-dc theory

Fifty-six page manual considers design and applications of rms-to-dc conversion, examines several circuits, and discusses testing methods for critical parameters. **Analog Devices,** Norwood, Mass.
**Circle 411**

### Local area networks

Twenty-page booklet reviews the status of different network architectures, technologies, and standards; it also summarizes market characteristics and forecasts growth. **Harris Corp,** Melbourne, Fla.
**Circle 412**

### Advanced technology video courses

Brochure describes courses in microprocessors, software engineering, CAD/CAM, and electronic design for engineers, technical managers, and computer professionals. **Integrated Computer Systems,** Santa Monica, Calif.
**Circle 413**

### Array processors

Individual brochures give précis of Mini-MAP and MAP-6410, touching on applications, system architecture, performance, software, configuration, and support. **CSP Inc,** Billerica, Mass.
**Circle 414**

### Diodes and rectifiers

Data book has 232 pages of information, applications, and cross-reference guide on complete line, plus acquired Siemens diode products. **Microsemi Corp,** Santa Ana, Calif.
**Circle 415**

### International electrical specs

"World Electricity Supplies and Connectors" tabulates industrial and commercial voltages, as well as plug configurations and types, frequencies, voltage tolerances, and phase distribution diagrams, for most industrial countries; document comes in bound hard copy or floppy disk, or over computer data link. **Pulver Laboratories Inc,** Boise, Id.
**Circle 416**

### Linear circuits

Catalog and cross-reference of military ICs, voltage references, dual transistors, op amps, and D-A converters lists second sources for Analog Devices, PMI, Hybrid Systems, Siliconix, Harris, Intersil, Burr-Brown, and National Semiconductor. **Micro Power Systems, Inc,** Santa Clara, Calif.
**Circle 417**

### Chip carrier resistors

Product bulletin details TaNFilm LCC network for high density surface mounting in precision industrial or military/aerospace applications; specs, performance and test data, ratings, and ordering information, as well as dimensional drawings and schematics, are included. **TRW Electronic Components Group,** Corpus Christi, Tex. **Circle 418**

### Telecommunications trends

Proceedings of the EIA's 1983 telecommunications conference present an overview of market restructuring, and directions in fiber optics, data communications, and subscriber equipment. Request on company letterhead ($20 postpaid) from: **EIA Telecommunications Group,** 2001 Eye St NW, Washington, DC 20006.

### Sockets and terminal carriers

Twenty-page catalog gives specs, footprints, and dimensional cross sections of LIF pin grid arrays, low profile DIPs, high density LSI sockets, DIP adapters, and Peel-a-Way terminal carriers. **Advanced Interconnections,** Warwick, RI.
**Circle 419**

### Cable-shielding performance

Selection guide defines interference problems, explains FCC regulations on emi, and discusses trade-offs of different cable shield types; 24-page brochure also specifies how well each testing method performs for various types of interference. **Belden,** Geneva, Ill.
**Circle 420**

### Electronic connectors

Flex-Com IDC system is examined in 65-page guide, which includes complete electrical specs and dimensional drawings for mil-spec headers and sockets, shielded D-subminiatures, and telecommunication-type connectors. **Winchester Electronics,** Oakville, Conn.
**Circle 421**

### Programmable controller links

Technical report discusses communication between industrial programmable controllers, and suggests alternatives to communication networks; performance criteria are analyzed, and interface to "foreign" devices on a network are discussed. **Reliance Electric Co,** Stone Mountain, Ga.
**Circle 422**

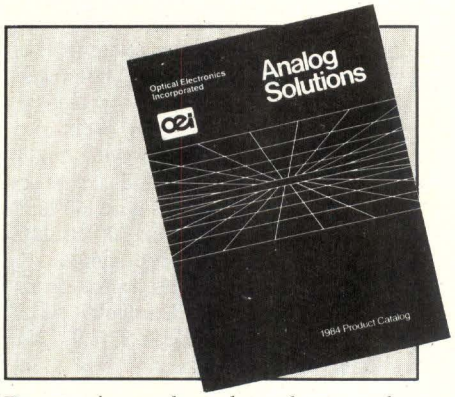
### Enhanced position sensing

Four-page application note outlines critical design considerations for a synchro position indicator with built-in microprocessor; five figures illustrate circuits described in text. **ILC Data Device Corp,** Bohemia, NY.
**Circle 423**

### Miniaturized switching power

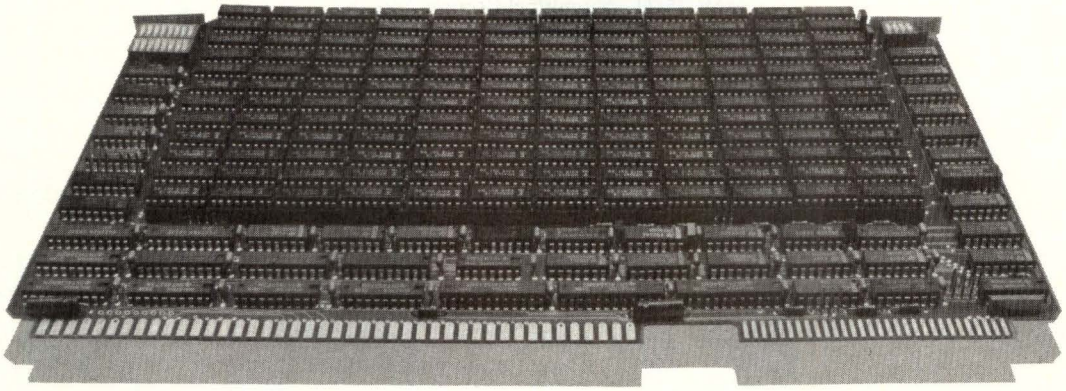
Electrical and environmental specs cover over 50 mil-std encapsulated packages that have ac or dc input modules, with 1 to 10 dc output modules up to 400 W. **Arnold Magnetics Corp,** Culver City, Calif. **Circle 424**

### Analog components




Twenty-six product data sheets and a reference section on the definition and testing of analog specs profile low noise FET amps, fast settling op amps, wideband op amps, log amps, peak sense and hold modules, and other function modules. **Optical Electronics Inc,** Tucson, Ariz.
**Circle 425**

# THE MULTIBUS*-
# MEGABYTE CONNECTION



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|---|---|---|
| MM-8086E | 512K-128KB | DRAM, EDC |
| MM-8086D | 512K-32KB | DRAM |
| MM-8000C | 128K-64KB | CMOS |

| PART NO. | CAPACITY | TYPE |
|---|---|---|
| ★MM-8500D | 256KB | CMOS, Calendar/Clock |
| MM-8086C | 64K-16KB | CMOS, Calendar/Clock |
| MM-8086 | 32KB | Core |

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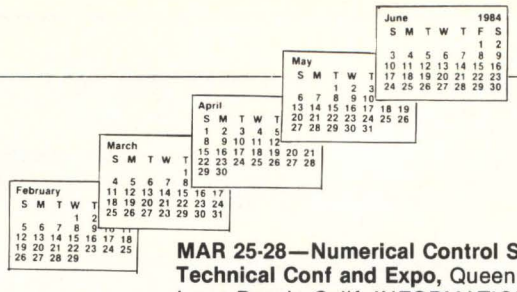
# CALENDAR




## CONFERENCES

**FEB 14-17—Computer Science Conf and SIGCSE Symposium,** Franklin Plaza Hotel, Philadelphia, Pa. INFORMATION: Richard Austing, Dept of Computer Science, Univ of Maryland, College Park, MD 20742. Tel: 301/454-2024

**FEB 20-22—Office Automation Conf,** Los Angeles, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**FEB 21-23—Softcon,** Superdome, New Orleans, La. INFORMATION: Peggy Kilburn, Northeast Expositions, 822 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000; 800/343-2222 (outside Mass)

**FEB 22-24—ISSCC (IEEE Internat'l Solid State Circuits Conf),** San Francisco, Calif. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

**FEB 22-28—Imprinta (Internat'l Congress and Exhibition for Communications Techniques),** Dusseldorf, West Germany. INFORMATION: Borman/Williams Inc, 222 Park Ave S, New York, NY 10003. Tel: 212/254-5400

**FEB 27-29—Nonimpact Printing Technologies: Database Access Meetings,** Sheraton at Fisherman's Wharf, San Francisco, Calif. INFORMATION: Jack Jordan, Advanced Technology Resources Corp, 6256 Pleasant Valley Rd, El Dorado, CA 95623. Tel: 916/626-4104

**FEB 28-MAR 1—Compcon/Spring,** Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**MAR 12-15—Interface,** Las Vegas Convention Ctr, Las Vegas, Nev. INFORMATION: Richard Katzeff, The Interface Group, Inc, 300 First Ave, Needham, MA 02194. Tel: 617/449-6600; 800/325-3330 (outside Mass)

**MAR 12-16—Internat'l Conf on Robotics,** Atlanta Hilton, Atlanta, Ga. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**MAR 19-21—Phoenix Conf on Computers and Communications,** Phoenix Hilton, Phoenix, Ariz. INFORMATION: David Gretton, Digital Equipment Corp, 2500 W Union Hills Dr, Phoenix, AZ 85027. Tel: 602/869-5273

**MAR 25-28—Numerical Control Society Technical Conf and Expo,** Queen Mary, Long Beach, Calif. INFORMATION: Lisa Schultz, Numerical Control Society, 111 E Wacker Dr, Suite 600, Chicago, IL 60601. Tel: 312/644-6610

**MAR 26-30—Internat'l Conf on Software Engineering,** Orlando, Fla. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**APR 2-5—Test & Measurement World Expo,** Brooks Hall, San Francisco, Calif. INFORMATION: Meg Bowen, Interfield Publishing Co, 215 Brighton Ave, Boston, MA 02134. Tel: 617/254-1445

**APR 3-5—Internat'l Reliability Physics Symposium,** Caesars Palace, Las Vegas, Nev. INFORMATION: George Ebel, Singer Co, 150 Totowa Rd, Wayne, NJ 07470. Tel: 201/785-6656

**APR 4-11—Hannover Fair,** Hannover, West Germany. INFORMATION: Delia Assocs, PO Box 338, Whitehouse, NJ 08888. Tel: 201/534-9044; 800/526-5978 (outside NJ)

**APR 10-12—Infocom,** Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**APR 18-20—Optical Data Storage,** Monterey Convention Ctr, Monterey, Calif. INFORMATION: Optical Society of America, 1816 Jefferson Pl NW, Washington, DC 20036. Tel: 202/223-8130

**APR 24-27—Compdec (Internat'l Conf on Data Engineering),** Bonaventure Hotel, Los Angeles, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**APR 30-MAY 2—Workshop on Computer Vision,** Hilton Hotel, Annapolis, Md. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**Announcements intended for publication in this department of *Computer Design* must be received at least three months prior to the date of the event. To ensure proper timely coverage of major events, material should be received six months in advance. Programs and dates are subject to last minute changes.**

**MAY 13-17—Computer Graphics,** Anaheim Convention Ctr, Anaheim, Calif. INFORMATION: National Computer Graphics Assoc, 8401 Arlington Blvd, Fairfax, VA 22031. Tel: 703/698-9600

**MAY 14-17—Internat'l Conf on Communications,** Congresscentrum Rai, Amsterdam, The Netherlands. INFORMATION: K. Teer, Philips Research Lab, 5600 MD Eindhoven, The Netherlands.

**MAY 14-17—Internat'l Conf on Distributed Computing,** Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**MAY 15-17—Electro,** Bayside Exposition Ctr and Hynes Auditorium, Boston, Mass. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

**MAY 15-17—Mini/Micro-Northeast,** Hynes Auditorium, Boston, Mass. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

**JUNE 4-8—SID (Society for Information Display Internat'l Symposium),** San Francisco Hilton, San Francisco, Calif. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

**JUNE 5-7—Internat'l Symposium on Computer Architecture,** Rackham Building, Ann Arbor, Mich. INFORMATION: Keki Irani, ECE Dept, Univ of Michigan, Ann Arbor, MI 48109. Tel: 313/764-8517

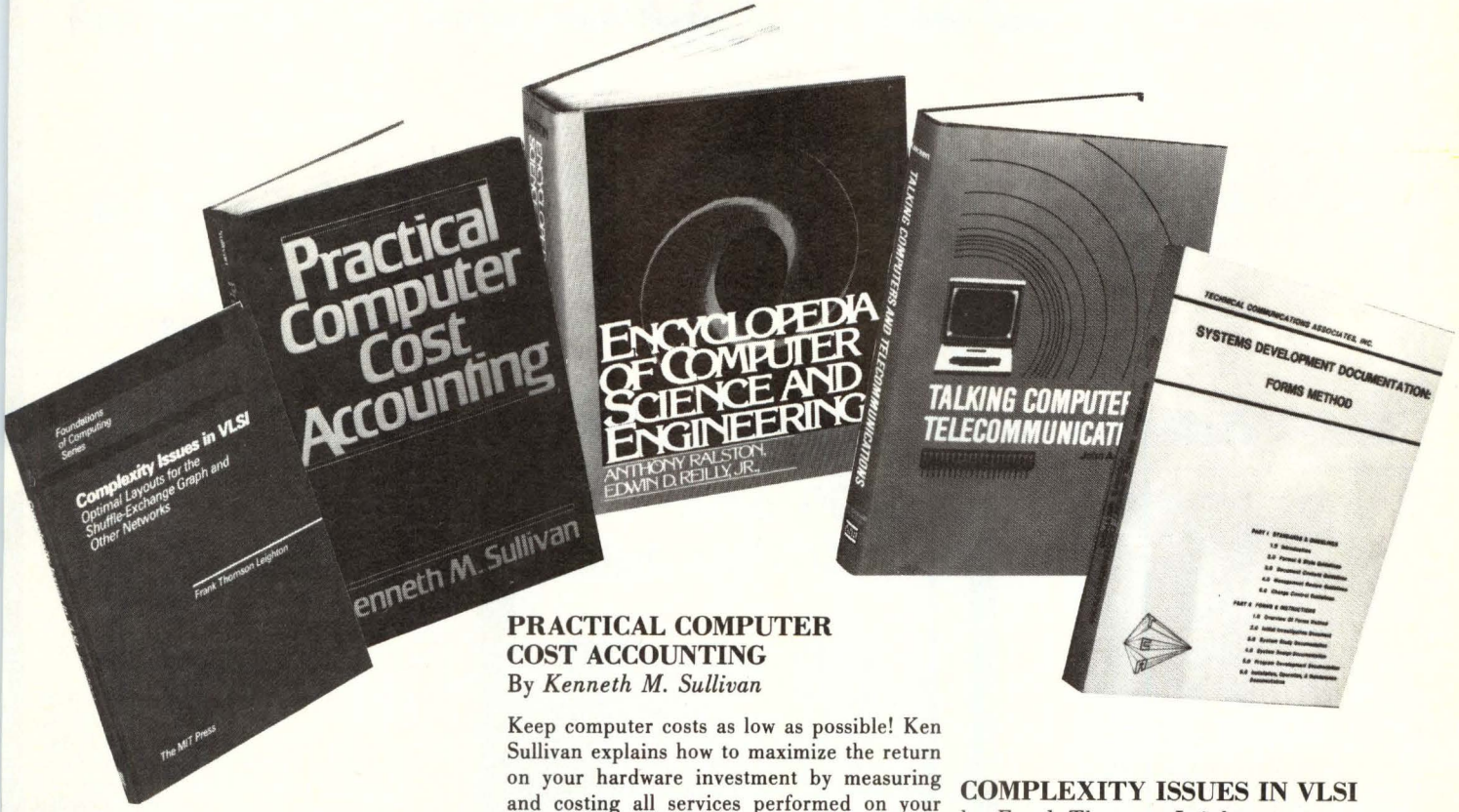
**JUNE 5-7—Symposium on Mass Storage Systems,** Marriott Mark Resort, Vail, Colo. INFORMATION: Bernard O'Lear, NCAR, PO Box 3000, Boulder, CO 80307. Tel: 303/494-5151

**JUNE 6-8—Communications Architectures and Protocols,** Montreal, Canada. INFORMATION: Rebecca Hutchings, Honeywell/FSD, 7900 Westpark Dr, McLean, VA 22102. Tel: 703/827-3982

**JUNE 19-22—Internat'l Symposium on Fault Tolerant Computing,** Hyatt Orlando, Orlando, Fla. INFORMATION: Richard Sedmak, Sperry Univac, PO Box 500, MS C1SW12, Blue Bell, PA 19404. Tel: 215/542-3638

**JUNE 24-27—Design Automation Conf,** Albuquerque Convention Ctr, Albuquerque, NM. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

# Designer's Bookcase

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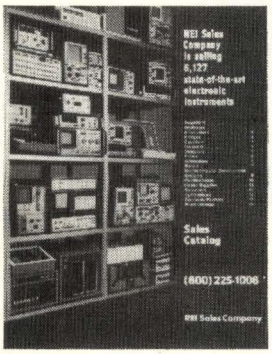


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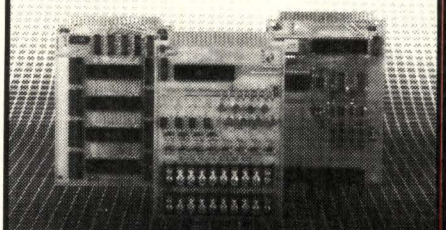
**CIRCLE 476**

## 6800/6809 Micro Modules



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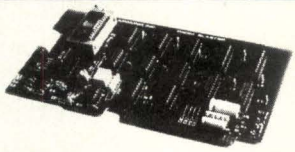

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Apparat's Prom Blasting system (A.P.B.) will program most 24-pin EPROM's including the Motorola 64K device (68764). The package comes complete with interface card, a complete set of personality modules, software on disk and a detailed instruction manual. The cost of the A.P.B. system is $119 ($129 for the IBM). TRS-80 versions may require the Apparat Bus-Extender at $69.95, or a user-supplied power supply and cable.

For details on the A.P.B. system, contact **APPARAT, INC.** located at 4401 S Tamarac Parkway, Denver, Colorado 80237, or call Apparat's technical/service department at 303-741-1778.

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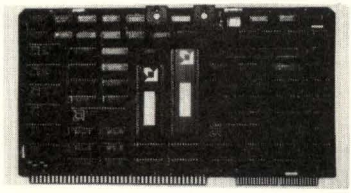

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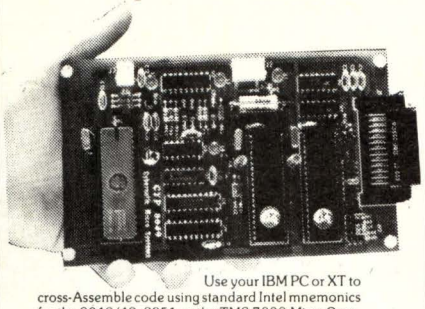

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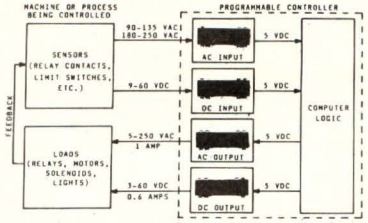


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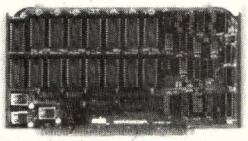

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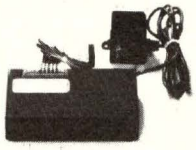

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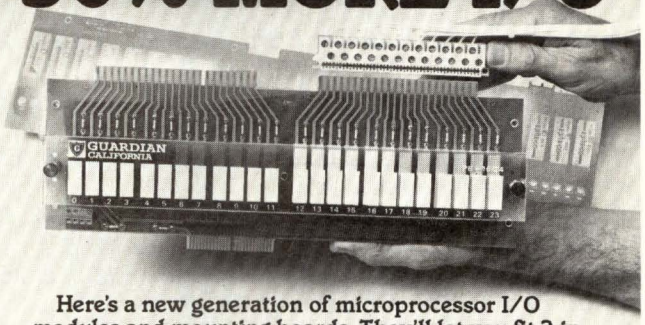


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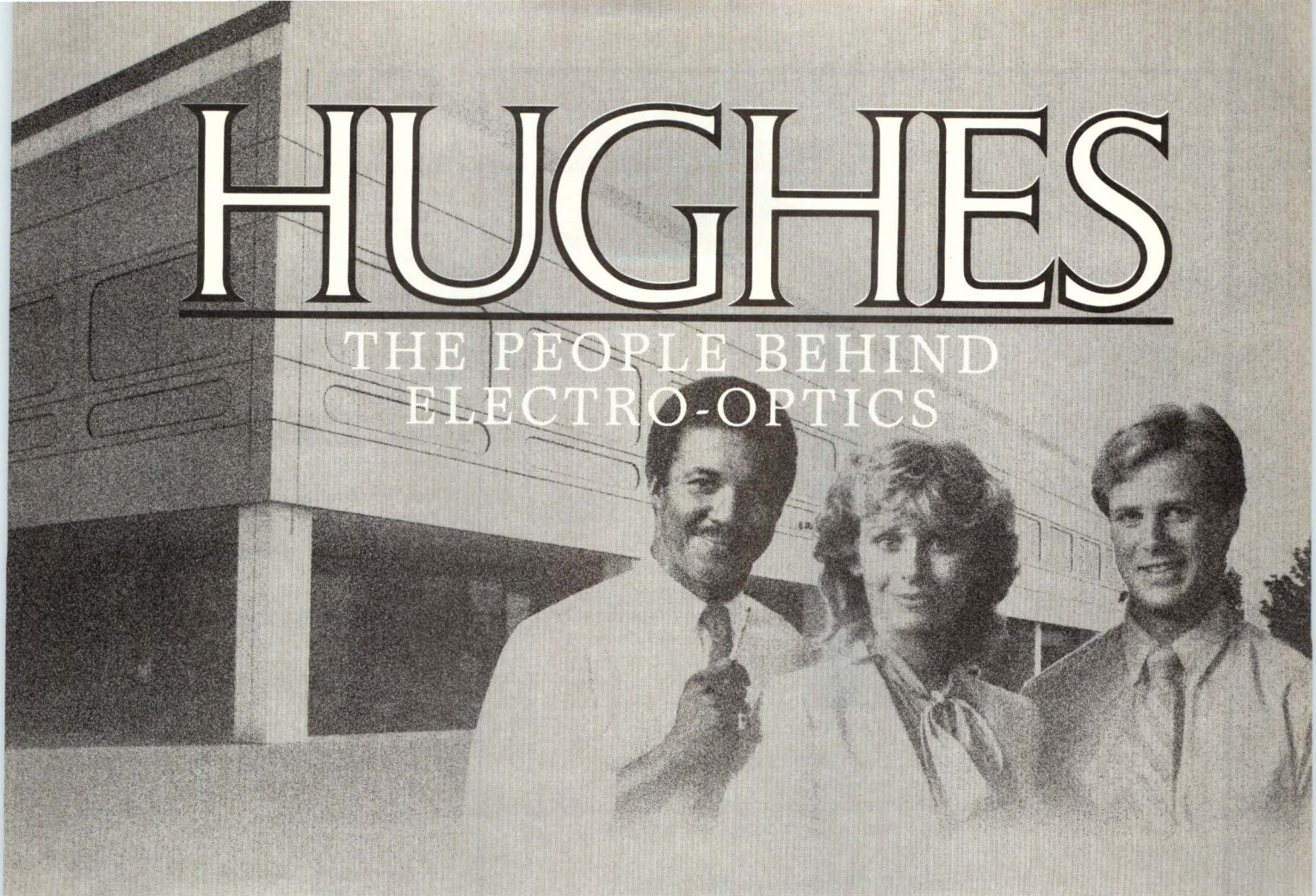

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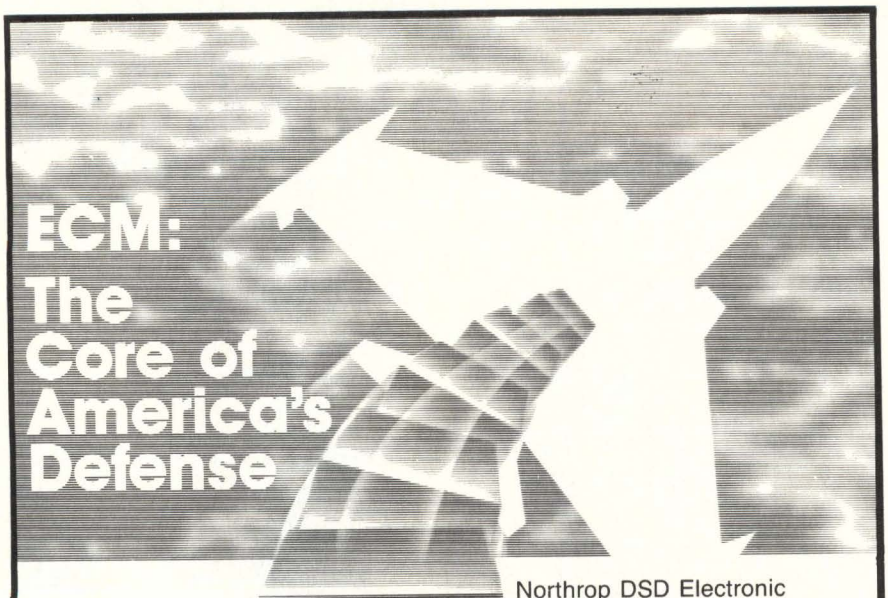


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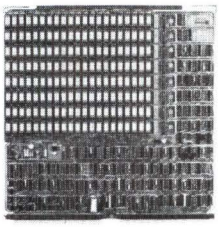

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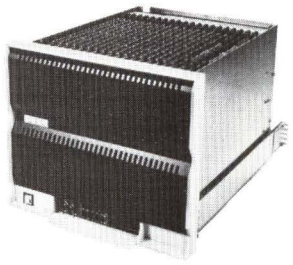
| DR-1200 (core) | 32 KB | NOVA 1200 |

**ADDING MORE THAN MEMORY.** And we don't stop with ADD-IN memory products — we can expand the capability of your Data General mini with a family of BULK MEMORY systems. Performance-proven systems that emulate Data General fixed head disc systems — but add the important advantages of solid-state speed and reliability. Making it ideal for disc swapping and more.



**MORE THAN COMPATIBLE.** Many of Dataram's products incorporate enhancements not available from comparable Data General products. For example, our 1.0 MB NOVA 4 compatible ADD-IN provides an extra ECC bit (giving you 6 ECC, rather than Data General's 5 ECC bits), transparent to the host mini, which allows full double-bit error detection.

**AND FOR LESS COST THAN YOU'D EXPECT** for highly reliable, proven memory products.

Any way you look at it, Dataram can do a lot in general to meet your requirements for Data General memory. But be specific — give us a call today to discuss your requirement.

| DATARAM BULK MEMORY | EMULATION | MAXIMUM CAPACITY |
|---|---|---|
| BS-303 (semi) | 6063/6065 (AOS compatible) | 8.0 MB |
| BC-303 (core) | 6063/6065 | 2.0 MB |
| BS-301 (semi) | NOVADISC | 4.0 MB |
| BC-301 (core) | NOVADISC | 2.0 MB |

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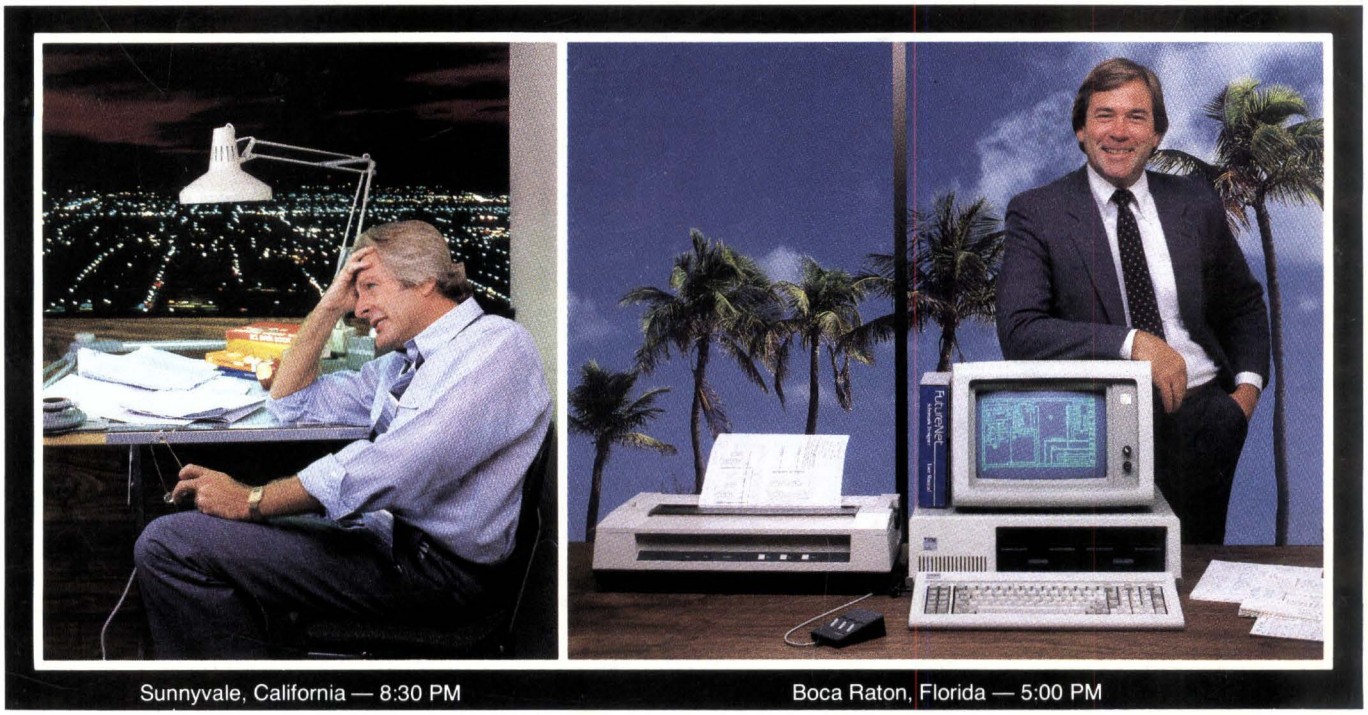
**DATARAM**

**Dataram Corporation** □ Princeton Road □ Cranbury, New Jersey 08512 □ (609) 799-0071 □ TWX: 510-685-2542

CIRCLE 135

# A TALE of TWO CITIES



Sunnyvale, California — 8:30 PM

Boca Raton, Florida — 5:00 PM

## How FutureNet's DASH-1™ Has Revolutionized Schematic Design and Documentation!

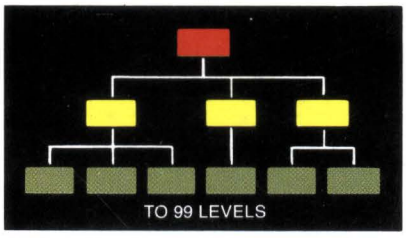
### Increased Schematic Design Efficiency

Obviously the engineer in Boca Raton has a big edge over his counterpart in Sunnyvale. The reason is simple. He uses FutureNet's DASH-1 Schematic Designer to create perfect schematics on his IBM PC... in a fraction of the time it takes others who still struggle with manual methods.

Besides producing top-quality schematics, the DASH-1 can automatically generate Net Lists, Lists of Materials, Design Check Reports and other critical support documents. All in all, DASH-1 increases your efficiency as a designer about five-fold... forget those long, wearisome hours slaving over routine documentation.

### Extensive Parts Library Included

At the heart of the amazing DASH-1 is a comprehensive symbol library (easily expandable, of course). It includes hundreds of TTL, microprocessor, memory/support chips, as well as discrete components, all with pinouts and pin functions. Call symbols instantly to your screen, move and connect them effortlessly to create your desired schematic while your DASH-1 automatically captures all the intelligence of your design. An optional plotter even allows you to produce a finished pen and ink drawing in minutes. Should you need it, the DASH-1 has full compatibility with most large CAD systems, as well.




### Now... Another Stride Forward!

An exciting new option, STRIDES™ (Structured Interactive Design System), lets you set up a complete "drawing tree" under DASH-1 control. Basically it works like this. When any drawing is updated, all related Pin Lists, Net Lists, Lists of Materials can also be updated automatically, at one time. And with STRIDES incredible power, up to 99 subordinated levels of drawings, net lists, etc., can be related to each other. Previously, if you could even find this capability on another system, it would cost you 10 to 20 times more than DASH-1.

### Productivity of the Future...Today!

In just a few short months, legions of designers throughout the world have discovered the new levels of design productivity and convenience DASH-1 provides. Four out of the top five electronics companies in the USA use DASH-1. At $5,980 for an add-on package to fit your IBM PC, nothing compares to it for value. Complete turn-key systems are also available at prices starting at $12,960.

So, no matter which city, state, or country you work in, let DASH-1 give you that efficiency edge.

Give us a call, today!

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(818) 700-0691

Productivity of the Future... today.

**CIRCLE 164**