# CP2034/
# CP2064

## Product Manual

CONNER

# Conner Peripherals, Inc.

# CP2034/CP2064
# Intelligent Disk Drive

# Product Manual

Revision I.4

March, 1991

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## CP2034/CP2064 Revision History

| Revision | Date | Change |
|---|---|---|
| I.4 | March 1991 | Initial Release |

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13.0 Command Register

# 1.0 Introduction

The CP2034 and CP2064 are a family of high performance 2.5 inch low-profile disk drives with formatted capacities of 32 and 64 megabytes respectively. Both drives have 19 ms average seek time and are designed to operate on IBM PC/AT or equivalent computers. The drives feature a low 5V power requirement and high shock resistance, enabling battery operation in a portable environment.

## 1.1 Scope

This specification describes the key features, specification summary, physical characteristics, environmental characteristics, functional description, electrical interface, recommended mounting configuration, timing requirements, host address decoding, command description, operations description, and error reporting for the Conner Peripherals models CP2034 and CP2064.

# 2.0 Key Features

- 2.5" Form factor
- Single 5 Volt supply
- Low power requirements
- 7 oz. unit weight
- High performance rotary voice coil actuator with embedded servo system.
- Single connector for power & interface
- Run length limited code (one of seven or two of seven)
- High shock resistance.
- Internal air filtration system
- Sealed HDA
- Automatic actuator latch over data free landing zone during standby mode or power down.
- Microprocessor-controlled diagnostic routines that are automatically executed at start-up.
- Automatic error correction and retries.
- Block size 512 bytes.
- PC AT interface
- 1:1 sector interleave

- Automatic read look ahead
- 32K Buffer
- Master/Slave

# 3.0 Specification Summary

## 3.1 Formatted Capacity

| | CP2034 | CP2064 |
|---|---|---|
| Formatted Mbytes | 32.0 Mbytes | 64.0 Mbytes |

## 3.2 Physical Configuration

| | CP2034 | CP2064 |
|---|---|---|
| Actuator Type | Rotary Voice-Coil | Rotary Voice-Coil |
| Number of Disks | 1 | 2 |
| Data Surfaces | 2 | 4 |
| Data Heads | 2 | 4 |
| Servo | Embedded | Embedded |
| Tracks per Surface | 823 | 823 |
| Track Density (TPI) | 2,100 TPI | 2,100 TPI |
| Formatted Track Capacity (bytes) | 19,456 user | 19,456 user |
| Bytes per Block | 512 | 512 |
| Blocks per Drive | 62,548 user | 125,096 user |
| Sectors per Track: user | 38 | 38 |
| Recording Density at ID (FCI) | 39,222 | 39,222 |
| Flux Density at ID, 1 of 7 (FCI) | 29,416 | 29,416 |
| Flux Density at ID, 2 of 7 (FCI) | 26,148 | 26,148 |
| Translate[1] | Universal | Universal |

[1] *see page 50 for Universal Translate definition.*

## 3.3 Performance

| | |
|---|---|
| Seek Times (nominal D.C. voltage and operating temperature)[1] | |
| Physical track to track | 5 ms (maximum) |
| Logical (translated) track to track | 10 ms (maximum) |
| Average access | 19 ms (maximum)[2] |
| Maximum stroke | 40 ms (maximum) |
| Average Latency (1/2 rev. after seek complete) | 8.7 ms |
| Rotation Speed (+0.5%) | 3486 RPM |
| Controller Overhead | 1.0 ms |
| Data Transfer Rate (to/from Media) | 1.5 Mbyte/second |
| Data Transfer Rate (to/from Buffer) | 4.5 Mbyte/second |
| Start Time | |
| (0 RPM - Ready) | typical: 10 seconds<br>maximum: 20 seconds[3] |
| Stop Time (Power Down) | typical: 3 seconds<br>maximum: 5 seconds |
| Start/Stop cycles | 40,000 minimum |
| Interleave | 1:1 |
| Buffer Size | 32K |

[1] *The timing is measured through the interface with the drive operating at nominal DC input voltages. The timing also assumes that:*
- *BIOS and PC system hardware dependency have been subtracted from timing measurements.*
- *The drive is operated using its native drive parameters.*

[2] *The average seek time is determined by averaging the seek time for a minimum of 1000 seeks of random length over the surface of the disk.*

[3] *These numbers assume spin recovery is not invoked. If spin recovery is invoked, the maximum time could be up to 60 seconds. Briefly removing power can lead to spin recovery being invoked.*

## 3.4 Power Requirements (Typical)

| | | Power | |
|---|---|---|---|
| | +5V DC ± 5% | Typical | Maximum |
| **Read/Write/Seek Mode** | 560 ma | 2.80 W | 3.00 W |
| **Idle Mode** | 260 ma | 1.30 W | 1.50 W |
| **Standby Mode** | 80 ma | 0.40 W | 0.50 W |
| **Sleep Mode** | 60 ma | 0.30 W | 0.40 W |
| **Spin-up Mode** | 1110 mA (5 sec) | n/a | n/a |

**Read/Write/Seek Mode:** occurs when data is being read from or written to the disk, or when the access mechanism is in motion.

**Idle Mode:** occurs when the drive is not reading, writing or seeking. The motor is up to speed and DRIVE READY condition exists. Actuator is residing on last accessed track.

**Standby Mode:** occurs when the motor is stopped and actuator is parked. STANDBY MODE will occur after a programmable time-out since last host access occurs. The drive will leave STANDBY MODE upon receipt of a command which requires disk access or upon receipt of a spin up command.

**Sleep Mode:** occurs when all electronics are disabled. Requires Host to reset to exit the SLEEP MODE.

Maximum noise allowed (DC to 1 MHZ, with equivalent resistive load): +5V DC: 3%.

# 4.0 Physical Characteristics

| | |
|---|---|
| Outline Dimensions ± .010" | 75" max. x 2.75" x 4.00" |
| Weight | 7.0 ounces |

# 5.0 Environmental Characteristics

## Temperature

| | |
|---|---|
| Operating | 5°C to 55°C |
| Non-operating | -40°C to 60°C |
| Thermal Gradient | 20°C per hour maximum |

## Humidity

| | |
|---|---|
| Operating | 8% to 80% non-condensing |
| Non-operating | 8% to 80% non-condensing |
| Maximum Wet Bulb | 26°C per hour |

## Altitude (relative to sea level)

| | |
|---|---|
| Operating | -200 to 10,000 feet |
| Non-operating (maximum) | 40,000 feet |

## 5.1 Reliability and Maintenance

| | |
|---|---|
| MTBF | 100,000 hours (POH)[1] |
| MTTR | 10 minutes typical |
| Preventive Maintenance | None |
| Component Design Life | 5 years |
| Data Reliablity | <1 non-recoverable error in $10^{13}$ bits read |

[1] *population is minimum of 100 units*

## 5.2 Shock and Vibration

| | |
|---|---|
| Shock | measured without shock isolation |
| Non-operating shock | 100G's, 11 ms, 1/2 sine wave |
| Operating Shock | 10 G's, 11 ms, 1/2 sine wave |
| Non-operating vibration | |
| 5-32 HZ (1/2 oct/min) | 0.010 inch displacement (double amplitude) |
| 33-500 Hz (1/2 oct/min) | 5 G's peak |
| Operating Vibration | |
| 5-10 Hz (1/2 oct/min) | 0.010 inch displacement (double amplitude) |
| 11-500 Hz (1/2 oct/min) | .5 G's peak |

## 5.3 Magnetic Field

The externally induced magnetic flux density may not exceed 6 gauss (DC - 700KHz) or 1.0 gauss (700KHZ - 1.5MHz) as measured at the drive surface.

## 5.4 Acoustic Sound Emission

Pressure: 34 dB(A) max at 1 meter.

## 5.5 Safety Standards

The CP2034 and CP2064 disk drives are designed to comply with relevant product safety standards such as:

- UL 478, 5th edition, Standard for Safety of Information Processing and Business Equipment, and

  UL 1950, Standard for Safety of Information Technology Equipment

- CSA 22.2 #154, Data Processing Equipment and
  CSA 22.2 #220, Information Processing and Business Equipment.

- IEC 435 Safety Requirements for Data Processing Equipment,
  IEC 380, Safety of Electrically Energized Office Machines, and
  IEC 950, Safety of Information Technology Equipment Including Electrical Business Equipment.

- VDE 0805 Equivalent to IEC 435,
  VDE 0805 TIEL 100, Equivalent to IEC 950, and
  VDE 0806, Equivalent to IEC 380.

# 6.0 Functional Description

The CP2034 and CP2064 contains all necessary mechanical and electronic parts to interpret control signals, position the recording heads over the desired track, read and write data, and provide a contaminant free environment for the heads and disks.

## 6.1 Read/Write and Control Electronics

One integrated circuit is mounted within the sealed enclosure in close proximity to the read/write heads. Its function is to provide head selection, read preamplification, and write data circuitry.

The single microprocessor controlled circuit card provides the remaining electronic functions which include:

- Read/Write Circuitry
- Rotary Actuator Control
- Interface Control
- Spin Speed Control
- Dynamic Braking
- Power Management

At power down or the start of STANDBY MODE or SLEEP MODE the heads are automatically retracted to the inner diameter of the disk and are latched and parked on a landing zone that is inside the data tracks.

## 6.2 Drive Mechanism

A brushless DC direct drive motor rotates the spindle at 3486 RPMs. The motor/spindle assembly is balanced to provide minimal mechanical runout to the disks and to reduce vibration of the HDA. A dynamic brake is used to provide a fast stop to the spindle motor when power is removed, or upon initiation of STANDBY MODE.

## 6.3 Air Filtration System

Within the sealed enclosure, a .3 micron filter provides a clean environment to the heads and disks.

## 6.4 Head Positioning Mechanism

The read/write heads for the CP2034 and CP2064 are supported by a mechanism coupled to the voice coil actuator.

## 6.5 Read/Write Heads and Disks

Data is recorded on 65mm diameter thin film disks through micro-miniature thin film or MIG heads.

## 6.6 Error Correction

The CP2034 and CP2064 use a Reed-Solomon code to perform error detection and correction. The error correction polynomial is capable of correcting one error burst with a maximum of 22 bits or 2 error bursts of up to 11 bits each, per 512 byte block. Single bursts of 11 bits or less are corrected with no performance degradation.

## 6.7 Master/Slave Configuration

The CP2034 and CP2064 drives are designed to operate either as a Master drive (C Drive) or a Slave Drive (D Drive). This feature is dependent on two drive settings; the status of hardware Jumper E1 and the firmware setting of a feature bit. When (E1) is closed, and the feature bit is set, the drive will assume the role of a Master Drive. When (E1) is open, and the feature bit reset, the drive will act as the Slave. In single drive configurations E1 must remain in the closed position. For the location of E1 refer to Figure 1. Information on the feature bit setting will be found in section 13 of this manual.

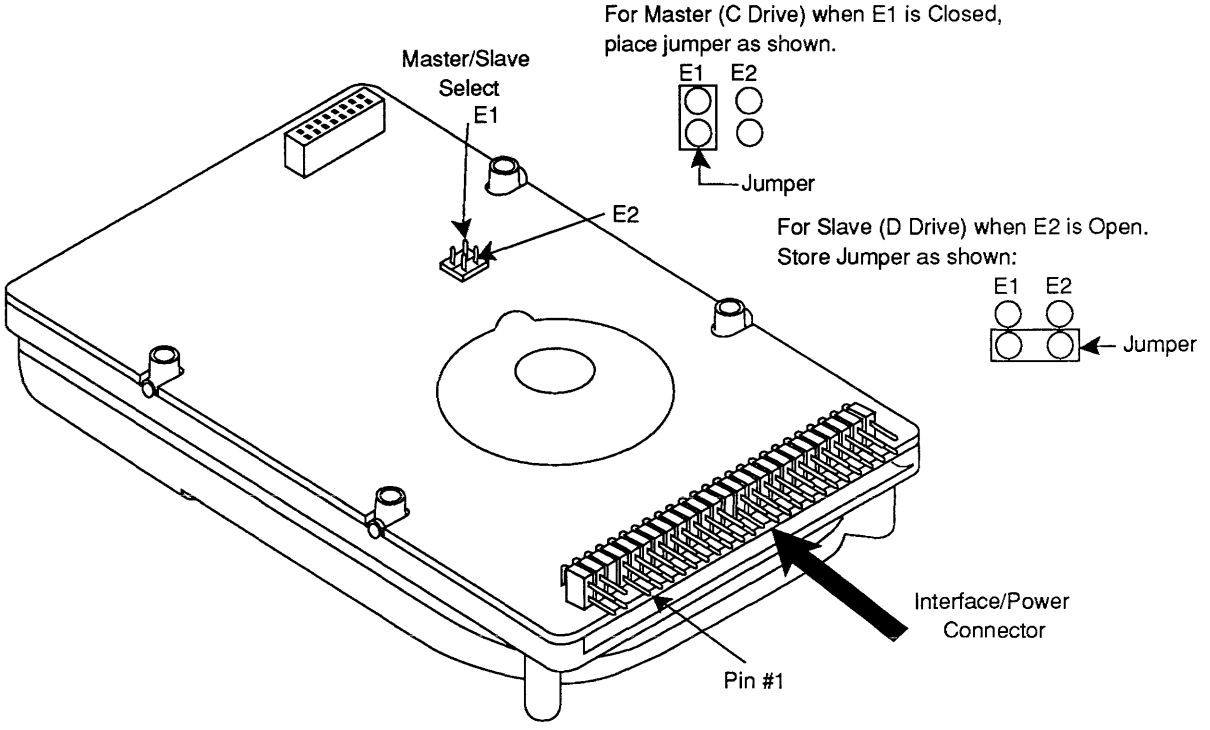


Figure 1. Master/Slave Jumper Configuration

# 7.0 Interface Connector

The CP2034 and CP2064 drives have a 44 pin right angle interface/power connector mounted on the PCB. The recommended mating connector is DuPont part number 69764-044 or equivalent (Refer to TAB 90-007). The maximum cable length is two feet. For location of the interface connector, see Figure 1 (DWG# 22589-001).

## 7.1 Diagnostic Routines

The microprocessor performs diagnostics upon application of power. If an error is detected the drive will not come ready.

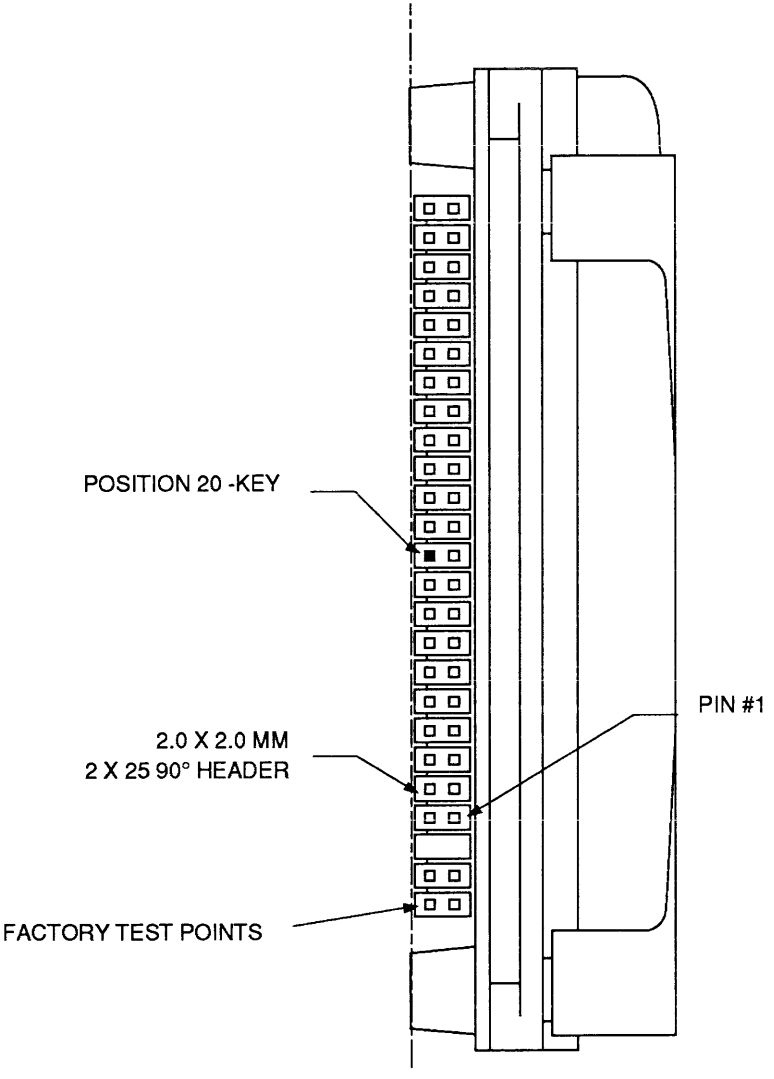


Figure 2. Connector

## 8.0 Recommended Mounting Configuration

The CP2034 and CP2064 drives are designed to be used in applications where the unit may experience shock and vibrations at greater levels than larger and heavier disk drives.

The design features which allow greater shock tolerance are the use of rugged heads and media, a dedicated landing zone, closed loop servo positioning and specially designed motor and actuator assemblies.

Four (4) side mounting points and four (4) bottom mounting points are provided to the customer. The drive is mounted using 3mm x 0.5mm thread screw. The screw insertion depth should not exceed 4mm into the mounting holes. The system integrator should allow ventilation to the drive to ensure reliable drive operation over the operating temperature range. The drive may be mounted in any attitude. See Figure 3.

For additional vibration isolation, an external suspension system may be used.

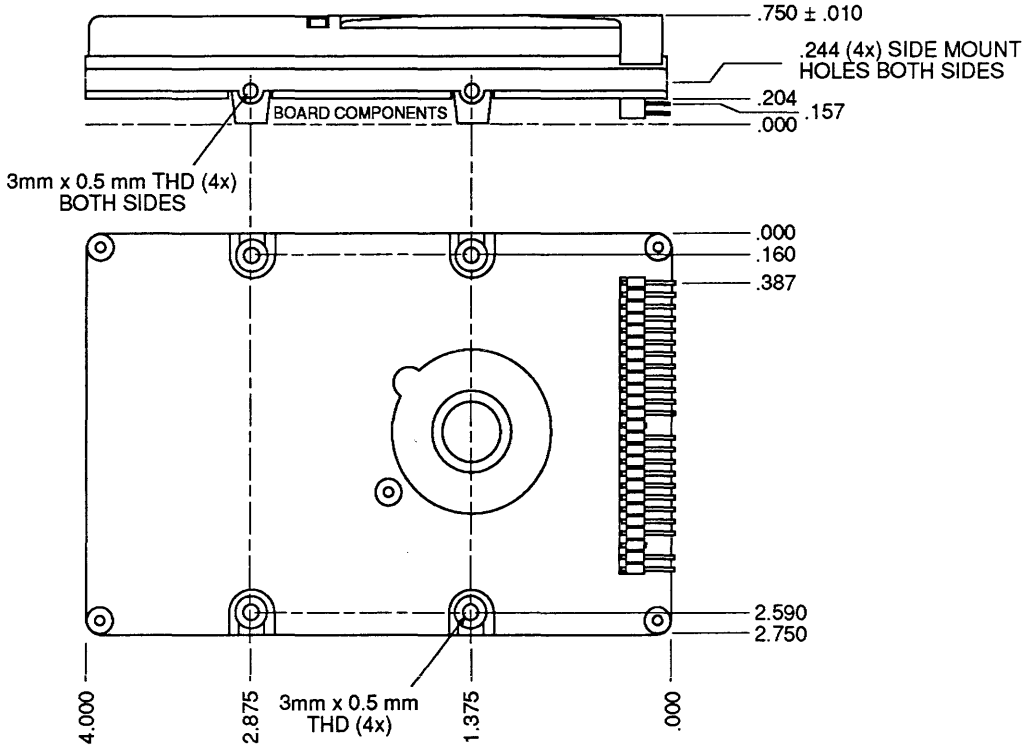


Figure 3. Mounting Configuration

# 9.0 Electrical Description

## 9.1 Signal Levels

All signal levels are TTL compatible. A logic "1" is > 2.0 Volts. A logic "0" is from 0.00 Volts to .70 Volts. The drive capability of each of the inbound signals is described below.

## 9.2 Conner Compatible Pin Descriptions

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 01 | –RESET | 02 | GND |
| 03 | +DATA 7 | 04 | +DATA 8 |
| 05 | +DATA 6 | 06 | +DATA 9 |
| 07 | +DATA 5 | 08 | +DATA 10 |
| 09 | +DATA 4 | 10 | +DATA 11 |
| 11 | +DATA 3 | 12 | +DATA 12 |
| 13 | +DATA 2 | 14 | +DATA 13 |
| 15 | +DATA 1 | 16 | +DATA 14 |
| 17 | +DATA 0 | 18 | +DATA 15 |
| 19 | GND | 20 | KEY |
| 21 | RESERVED | 22 | GND |
| 23 | –IOW | 24 | GND |
| 25 | –IOR | 26 | GND |
| 27 | IOCHRDY | 28 | RESERVED |
| 29 | RESERVED | 30 | GND |
| 31 | +IRQ | 32 | –IO16 |
| 33 | +ADDR 1 | 34 | –PDIAG |
| 35 | +ADDR 0 | 36 | +ADDR 2 |
| 37 | –CS0 | 38 | –CS1 |
| 39 | –ACTIVE | 40 | GND |
| 41 | 5 VOLTS (LOGIC) | 42 | 5 VOLTS (MOTOR) |
| 43 | GND | 44 | RESERVED |

| Signal Name | Dir | Pin | Description |
|---|---|---|---|
| -RESET | O | 1 | Reset signal from the Host system which is active low during power up and inactive thereafter. |
| GND | O | 2,19, 22, 24, 26, 30, 40, 43 | Ground between the drive and the Host. |
| +DATA 0-15 | I/O | 3-18 | 16 bit bi-directional data bus between the host and the drive. The lower 8 bits, HDO-HD7, are used for register & ECC access. All 16 bits are used for data transfers. These are tri-state lines with 10 mA drive capability. |
| KEY | N/C | 20 | An unused pin clipped on the drive and plugged on the cable. Used to guarantee correct orientation of the cable. |
| RESERVED | O | 21, 29, 28, 44 | Reserved |
| -IOW | O | 23 | Write strobe, the rising edge of which clocks data from the host data bus into a register or the data register of the drive. |
| -IOR | O | 25 | Read strobe, which when low enables data from a register or the data register of the drive onto the host data bus.The rising edge of IOR latches data from the drive at the host. |
| IOCHRDY* | O | 27 | Used to extend I/O cycles in fast transfer environment. |

** Not used by Conner.*

| Signal Name | Dir | Pin | Description |
|---|---|---|---|
| +IRQ | I | 31 | Interrupt to the Host system. This signal is enabled only when the drive is selected, and the host activates the -IEN bit in the Digital Output Register.<br><br>When the -IEN bit is inactive, or the drive is not selected, this output in a high impedance state, regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a Host read of the Status register or a write to the command register. This signal is a tri-state line with 10 mA drive capacity. |
| -IO16 | I | 32 | Indication to the Host system that the 16 bit data register has been addressed and that the drive is prepared to send or receive a 16 bit data word. This line is tri-state line with 20 mA drive capacity. |
| -PDIAG | I/O | 34 | At POR -PDIAG will be activated by the slave within 1 ms. If the master doesn't see -PDIAG active after 4 ms it will assume no slave is present. -PDIAG will remain active until the slave is ready to go not busy or 14.0 seconds on a power on reset. The master will wait 14.5 seconds or until the slave deactivates -PDIAG on power on reset before it goes not busy. The slave will de-activate -PDIAG and go not busy, if it is not ready after the 14.0 seconds. Neither drive will set ready or seek complete until they have reached full spin speed and are ready to read/write. |

| Signal Name | Dir | Pin | Description |
|---|---|---|---|
| | | | During a software reset, -PDIAG will be activated by the slave within 1 ms. If the master doesn't see -PDIAG active after 4 ms it will assume no slave is present. The slave will not de-activate -PDIAG until it is ready to go not busy or 400 ms. The master will only wait 450 milliseconds or until the slave deactivates -PDIAG before it goes not busy. The slave will only wait 450 milliseconds before it activates -PDIAG and goes not busy. The slave will not set ready or seek complete until those states are achieved.<br><br>After reset, -PDIAG will be used for the diagnostic command in the following manner. It is output by the drive if it is the slave drive, input to the drive if it is the master drive. This low true signal indicates to a master that the slave has passed its internal diagnostic command. This line is only inactive high during execution of the diagnostic command. |
| +AO,A1,A2 | O | 35,33,36 | Bit binary coded addresses used to select the individual registers in the drive. |
| -CS0 | O | 37 | Chip select decoded from the host address bus. Used to select some of the Host accessible registers. NOTE: This signal should be disabled by the Host when data transfers are in progress. |
| -CS1 | O | 38 | Chip select decoded from the Host address bus. Used to select three of the registers in the Task File. |

| Signal Name | Dir | Pin | Description |
|---|---|---|---|
| -ACTIVE | I | 39 | This pin provides for connection of an external LED to indicate "Drive Active" status. It is capable of sinking 24 ma. |
| +5V (Logic) | O | 41 | 5 volt ±5% supply to drive circuitry. |
| +5V (Motor) | O | 42 | 5 volt ±5% supply to drive motors. |

## 9.3 Cam Compatible Pin Descriptions

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 01 | –RESET | 02 | GND |
| 03 | +DATA 7 | 04 | +DATA 8 |
| 05 | +DATA 6 | 06 | +DATA 9 |
| 07 | +DATA 5 | 08 | +DATA 10 |
| 09 | +DATA 4 | 10 | +DATA 11 |
| 11 | +DATA 3 | 12 | +DATA 12 |
| 13 | +DATA 2 | 14 | +DATA 13 |
| 15 | +DATA 1 | 16 | +DATA 14 |
| 17 | +DATA 0 | 18 | +DATA 15 |
| 19 | GND | 20 | KEY PIN |
| 21 | DMARQ | 22 | GND |
| 23 | –DIOW | 24 | GND |
| 25 | –DIOR | 26 | GND |
| 27 | IOCHRDY | 28 | SPSYNC |
| 29 | DMACK | 30 | GND |
| 31 | UNTRQ | 32 | IOCS16 |
| 33 | DA1 | 34 | –PDIAG |
| 35 | DA0 | 36 | DAZ |
| 37 | CS1FX | 38 | CS3FX |
| 39 | DASP | 40 | GND |

**Feature Bit 1 must be set by Conner.*
*Feature Bit cannot be set by User.*

| Signal Name | Dir | Pin | Description |
|---|---|---|---|
| -RESET | O | 1 | Reset signal from the Host system which is active low during power up and inactive thereafter. |
| GND | O | 2,19, 22, 24, 26, 30, 40, 43 | Ground between the drive and the Host. |
| +DATA 0-15 | I/O | 3-18 | 16 bit bi-directional data bus between the host and the drive. The lower 8 bits, HDO-HD7, are used for register & ECC access. All 16 bits are used for data transfers. These are tri-state lines with 10 mA drive capability. |
| KEY | N/C | 20 | An unused pin clipped on the drive and plugged on the cable. Used to guarantee correct orientation of the cable. |
| DMARQ | O | 21 | This signal, used for DMA data transfers between host and drive, shall be asserted by the drive when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in a handshake manner with DMACK- i.e. the drive shall wait until the host asserts DMACK- before negating DMARQ, and re-asserting DMARQ if there is more data to transfer. |
| DMACK | O | 29 | This signal shall be used by the host in response to DMARQ to either acknowledge that data has been accepted, or that data is available. |

| Signal Name | Dir | Pin | Description |
|---|---|---|---|
| SPSYNC | O | 28 | This signal received by a drive is used as the synchronization signal to lock the spindles in step. The time to achieve synchronization varies, and is indicated by the drive setting DRDY i.e. if the drive does not achieve synchronization following power on or a reset, it shall not set DRDY. |
| RESERVED | O | 44 | Reserved |
| -IOW | O | 23 | Write strobe, the rising edge of which clocks data from the host data bus into a register or the data register of the drive. |
| -IOR | O | 25 | Read strobe, which when low enables data from a register or the data register of the drive onto the host data bus.The rising edge of IOR latches data from the drive at the host. |
| IOCHRDY* | O | 27 | Used to extend I/O cycles in fast transfer environment. |

** Not used by Conner.*

| Signal Name | Dir | Pin | Description |
|---|---|---|---|
| +IRQ | I | 31 | Interrupt to the Host system. This signal is enabled only when the drive is selected, and the host activates the -IEN bit in the Digital Output Register.<br><br>When the -IEN bit is inactive, or the drive is not selected, this output in a high impedance state, regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero by a Host read of the Status register or a write to the command register. This signal is a tri-state line with 10 mA drive capacity. |
| -IO16 | I | 32 | Indication to the Host system that the 16 bit data register has been addressed and that the drive is prepared to send or receive a 16 bit data word. This line is tri-state line with 20 mA drive capacity. |
| -PDIAG | I/O | 34 | At POR -PDIAG will be activated by the slave within 1 ms. If the master doesn't see -PDIAG active after 4 ms it will assume no slave is present. -PDIAG will remain active until the slave is ready to go not busy or 14.0 seconds on a power on reset. The master will wait 14.5 seconds or until the slave deactivates -PDIAG on power on reset before it goes not busy. The slave will de-activate -PDIAG and go not busy, if it is not ready after the 14.0 seconds. Neither drive will set ready or seek complete until they have reached full spin speed and are ready to read/write. |

| Signal Name | Dir | Pin | Description |
|---|---|---|---|
| | | | During a software reset, -PDIAG will be activated by the slave within 1 ms. If the master doesn't see -PDIAG active after 4 ms it will assume no slave is present. The slave will not de-activate -PDIAG until it is ready to go not busy or 400 ms. The master will only wait 450 milliseconds or until the slave deactivates -PDIAG before it goes not busy. The slave will only wait 450 milliseconds before it activates -PDIAG and goes not busy. The slave will not set ready or seek complete until those states are achieved.<br><br>After reset, -PDIAG will be used for the diagnostic command in the following manner. It is output by the drive if it is the slave drive, input to the drive if it is the master drive. This low true signal indicates to a master that the slave has passed its internal diagnostic command. This line is only inactive high during execution of the diagnostic command. |
| +AO,A1,A2 | O | 35,33,36 | Bit binary coded addresses used to select the individual registers in the drive. |
| -CS0 | O | 37 | Chip select decoded from the host address bus. Used to select some of the Host accessible registers. NOTE: This signal should be disabled by the Host when data transfers are in progress. |
| -CS1 | O | 38 | Chip select decoded from the Host address bus. Used to select three of the registers in the Task File. |

| Signal Name | Dir | Pin | Description |
|---|---|---|---|
| DASP | I | 39 | This is a time-multiplexed signal which indicates that a drive is active, or that Drive 1 is present. This signal shall be an open collector output and each drive shall have a 10K pull-up resistor. During power on initialization or after RESET- is negated, DASP- shall be asserted by Drive 1 within 400 msec to indicate that Drive 1 is present. Drive 0 shall allow up to 450 msec for Drive 1 to assert DASP-. If Drive 1 is not present, Drive 0 may assert DASP- to drive activity LED. DASP- shall be negated following acceptance of the first valid command by Drive 1 or after 31 seconds, whichever comes first. Any time after negation of DASP-, either drive may assert DASP- to indicate that a drive is active. (See Note below). |
| +5V (Logic) | O | 41 | 5 volt ±5% supply to drive circuitry. |
| +5V (Motor) | O | 42 | 5 volt ±5% supply to drive motors. |

*Note: Prior to the development of this standard, products were introduced which did not time multiplex DASP-. Some used two jumpers to indicate to Drive 0 whether Drive 1 was present. If such a drive is jumpered to indicate Drive 1 is present it should work successfully with a Drive 1 which complies with this standard. If installed as Drive 1, such a drive may not work successfully because it may not assert DASP- for a long enough period to be recognized. However, it would assert DASP- to indicate that the drive is active.*

# 10.0 Timing Requirements

Host PC Programmed I/O Timing Parameters

The following timings are operating under the assumption that all outputs will drive 24 milliampre load in parallel with 300 pF and all inputs are at TTL level. The MIN and MAX timings are conforming to the operating ranges of power supply voltage of 5V +/- 10% and ambient temperature of 0C to 70C.

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| CS16L | HCS0* & A0:2 low, HCS1* high to IOCS16* low | | 30 | ns |
| ADRSET | Address setup to IOR*/IOW* low | 30 | | ns |
| ADRHLD | Address hold from IOR*/IOW* low | 30 | | ns |
| RDTA | IOR* low to HDB[0:15] valid | | 50 | ns |
| RDHLD | IOR* high to HDB[0:15] invalid | 0 | | ns |
| RDTRI | IOR* HIGH TO HDB[0:15] tri-state | | 40 | ns |
| WDS | HDB[0:15] setup to IOW* high | 10 | | ns |
| WDHLD | HDB[0:15] hold from IOW* high | 10 | | ns |
| RWPULSE | IOR*/IOW* pulse width | 80 | | ns |

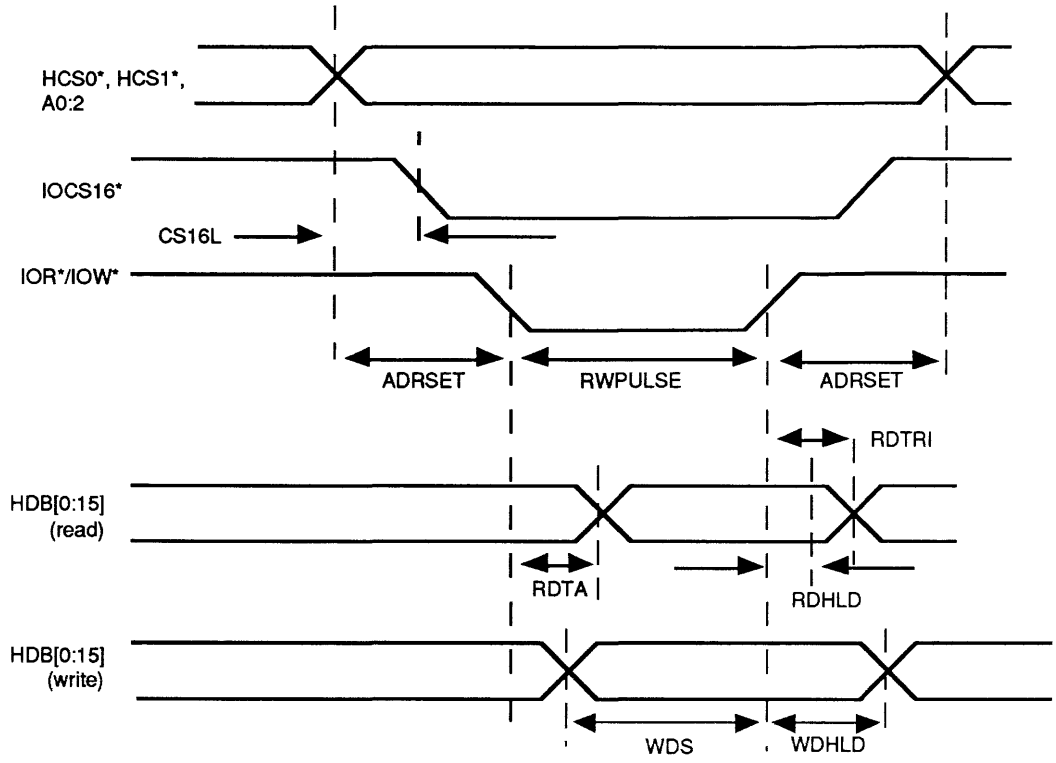


Figure 4. Timing Diagram

# 11.0 Host Address Decoding

The Host addresses the drive using programmed I/O. This method requires that the desired register address be placed on the three address lines A2 - A0, a proper drive chip select is asserted and a read or write strobe (-IOR/-IOW) is given to the chip.

The Host generates two independent chip selects on the interface. The high order chip select, -CS1, is used to access register 3F6 or 3F7. The low order chip select, -CSO, is used to address registers 1F0 - 1F7.

The Host data bus 15-8 is only enabled when IO16 enable is active and the Host is addressing the data register for transferring data and not the ECC bytes which are only transferred if the operation is a read or a write long.

The following I/O map defines all of the register addresses and functions for these I/O locations. A description of each register follows.

| Addr[1] | –CS0 | –CS1 | HA2 | HA1 | HA0 | Read Function | Write Function |
|---|---|---|---|---|---|---|---|
| | 1 | 1 | x | x | x | No operation | No Operation |
| | 0 | 0 | x | x | x | Invalid address | Invalid address |
| | 1 | 0 | 0 | x | x | High Impedance | Not used |
| | 1 | 0 | 1 | 0 | x | High Impedance | Not used |
| 1F0 | 0 | 1 | 0 | 0 | 0 | Data Register | Data Register |
| 1F1 | 0 | 1 | 0 | 0 | 1 | Error Register | Write Precomp Reg. |
| 1F2 | 0 | 1 | 0 | 1 | 0 | Sector Count | Sector Count |
| 1F3 | 0 | 1 | 0 | 1 | 1 | Sector Number | Sector Number |
| 1F4 | 0 | 1 | 1 | 0 | 0 | Cylinder Low | Cylinder Low |
| 1F5 | 0 | 1 | 1 | 0 | 1 | Cylinder High | Cylinder High |
| 1F6 | 0 | 1 | 1 | 1 | 0 | SDH Register | SDH Register |
| 1F7 | 0 | 1 | 1 | 1 | 1 | Status Register | Command Reg. |
| 3F6 | 1 | 0 | 1 | 1 | 0 | Alternate Status Reg. | Digital Output Reg. |
| 3F7 | 1 | 0 | 1 | 1 | 1 | Drive Address Reg. | Not used |

x = don't care

# 12.0 Register Description

In the following register descriptions, unused write bits are treated as "don't cares", and unused read bits are read as zeroes.

## 12.1 Data Register

(-CS0, address 0, R/W). The data register is the register through which all data is passed on read and write commands. It is also the register to which the sector table is transferred during format commands and the data associated with the identify command is transferred. All transfers are high speed 16 bit I/O operations except for ECC bytes transferred during R/W long commands, which are slower 8 bit operations that occur after the transfer of the data.

Data is stored on the disk with the Least Significant Byte first, then the Most significant byte for each word. This is important to remember when testing the ECC circuitry.

## 12.2 Error Register

(-CS0, address 1, read only). This error register contains status from the last command executed by the drive. The contents of this register are only valid when the error bit (ER) is set in the Status register, unless the drive has just powered up or completed execution of its internal diagnostic, in which case the register contains a status code. The error bits in the register are defined below. The status codes are discussed later in the description of the DIAGNOSTIC Command.

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| BBK | UNC | – | IDNF | – | ABRT | TKO | – |

where:

**BBK** indicates that a bad block mark was detected in the requested sector's ID field. A bad block is not created in the factory, but only when requested in the format command.

**UNC** indicates that a non-correctable data error has been encountered.

**IDNF** indicates that the requested sector's ID field could not be found.

**ABRT** indicates that the requested command has been aborted due to a drive status error (not ready, write fault, etc.) or because the command code is invalid.

**TK0** indicates that track 0 has not been found during a recalibrate command.

-- not used. These bits are reset to zero.

### 12.3 Write Precomp Register

(-CS0, address 1 write only). A register previously used to set write precompensation, now is used only for enabling or disabling LOOK AHEAD READs or to activate extended commands.

### 12.4 Sector Count

(-CS0, address 2, R/W). The sector count defines the number of sectors of data to be read or written. If the value in this register is zero, a count of 256 sectors is specified. This count is decremented as each sector is read such that the register contains the number of sectors left to access in the event of an error in a multi-sector operation.

The contents of this register define the number of sectors per track when executing an Initialize Drive Parameters command. This register is also used in the power commands to provide the power down time-out parameter and status.

## 12.5 Sector Number

(-CS0, address 3, R/W). This register contains the starting sector number for any disk access. At the completion of each sector, and at the end of the command this register is updated to reflect the last sector read correctly, or the sector on which an error occurred. During multiple sector transfers, this register is updated to point at the next sector to be read/written if the previous sector's operation was successful.

## 12.6 Cylinder Low

(-CS0, address 4, R/W). The cylinder low register contains the low order 8 bits of the starting cylinder number for any disk access. At the completion of each sector, and at the end of the command, this register is updated to reflect the current cylinder number.

## 12.7 Cylinder High

(-CS0, address 5, R/W). The cylinder high register contains the two high order bits of the starting cylinder number for any disk access. At the completion of each sector, and at the end of the command, this register is updated to reflect the current cylinder number.

## 12.8 SDH Register

(-CS0, address 6, R/W). This register contains the drive and head numbers, as defined below:

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| RSVD | 0 | 1 | DRV | HEAD | | | |

where:

**DRV** is the binary encoded drive select number. When this bit is reset, the master drive is selected, and when this bit is set, the slave drive is selected.

**HEAD** is the four bit binary encoded head select number.

**RSVD** this bit is used by the Host.

At the completion of each sector, and at the end of the command, this register is updated to reflect the currently selected head.

## 12.9 Status Register

(-CS0, address 7 read only). This register contains the drive/controller status. The contents of this register are updated at the completion of each command. If the busy bit is active, no other bits are valid. The Host reading this register when an interrupt is pending is considered to be the interrupt acknowledge, and any pending interrupt is therefore cleared whenever this register is read.

The bits in this register are defined below:

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| BSY | DRDY | DWF | DSC | DRQ | CORR | IDX | ERR |

where:

**BSY** is the busy bit, which is activated whenever the drive has access to the Task File registers, and the Host is locked out from accessing the Task File. This bit is activated under the following circumstances:

1) At activation of the HOST RESET pin in the interface, or at activation of the software bit in the digital output register.

2) Immediately upon Host write of the command register with a read, read long, read buffer, seek, recall, initialize drive parameters, read verify,identify, or diagnostic command.

3) Immediately following transfer of: A) 512 bytes of data after Host write of the command register with a write, format track, or write buffer command, or B) 512 bytes of data and the four ECC bytes after a Host write of the Command register with a write long command. When BSY is active, any Host read of a Task File register is inhibited and the Status register is read instead.

**DRDY** is the drive ready indication. When there is an error, this bit is not changed until the Status register is read by the Host, at which time the bit again indicates the current readiness of the drive. This bit will be inactive at power up and remain inactive until the drive is up to speed and ready to accept a command.

**DSC** is the drive seek complete line. It is an indication that the actuator is on track. When there is an error, this bit is not changed until the Status register is read by the Host, at which time the bit again indicates the current readiness of the drive. This bit will be inactive at power up and remain inactive until the drive is up to speed and ready to accept a command.

**DWF** is the drive write fault bit. When there is an error, this bit is not changed until the Status register is read by the Host, at which time the bit again indicates the current write fault status.

**DRQ** is the data request bit, which indicates that the drive is ready for transfer of a word or a byte of data between the Host and the Data register.

**CORR** is the corrected data bit, which is active when a correctable data error has been encountered and the data has been corrected by an ECC operation that required processor intervention. On-the-fly hardware ECC correction will not post the CORR bit.

If for diagnostic purposes it is necessary to have the CORR bit set in all cases the on-the-fly capability should first be disabled via the retry control command (op code F3H). This condition will not terminate a multi-sector read operation.

**IDX** is the index bit which is active once per disk revolution.

**ERR** is the error bit, which indicates that the previous command ended in some type of error. The other bits in the Status register, and the bits in the error register will have additional information as to the cause of the error.

## 12.10 Command Register

(-CS0, address 7, write only). The eight bit code written to this register passes the drive the command from the Host. Command execution begins immediately after this register is written. A list of executable commands with the command codes and necessary parameters for each command follows:

| Command Name | Command Code | | | | | | | | Parameters Used | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | SC | SN | C | SDH |
| Recalibrate | 0 | 0 | 0 | 1 | x | x | x | x | n | n | n | d |
| Read Sector(s) | 0 | 0 | 1 | 0 | 0 | 0 | L | r | y | y | y | y |
| Write Sector(s) | 0 | 0 | 1 | 1 | 0 | 0 | L | r | y | y | y | y |
| Read Verify Sector(s) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | r | y | y | y | y |
| Format Track | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | n | n | y | y |
| Seek | 0 | 1 | 1 | 1 | x | x | x | x | n | n | y | y |
| Execute Drive Diag. | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | n | n | n | d |
| Initiate Drive Parms | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | y | n | n | y |
| Power Command | 1 | 1 | 1 | 0 | p | p | p | p | y | n | n | d |
| Read Multiple | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | y | y | y | y |
| Write Multiple | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | y | y | y | y |
| Set Multiple Mode | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | y | n | n | d |
| Read Sector Buffer | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | n | n | n | d |
| Write Sector Buffer | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | n | n | n | d |
| Identify Drive | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | n | n | n | d |

where:

**L** is the long bit, if 1, R/W long commands are executed, if 0, normal R/W commands are performed.

**r** is the retry bit; = 0, retries are enabled, = 1, retries are disabled. Retries that may be enabled/disabled are those on ECC and data errors. When retries are disabled at the start of a command, they are always automatically enabled at the end of the command.

**SC** is the sector count register.

**SN** is the sector number register.

**CY** is the cylinder registers.

**SDH** is the drive/head register.

**PR** is the precomp register.

**y** means the register contains a valid parameter for this command. For the drive/head register, y means that both the drive and head parameters are used.

**n** means the register does not contain a valid parameter for this command.

**d** means only the drive parameter is valid and not the head parameter.

**p** indicates commands codes E0, E1, E2, E3, E5 and E6.

x = don't care.

## 12.11 Alternate Status Register

(-CS1, address 6, read only). This register contains the same information as the Status register in the Task File. The only difference being that reading this register does not imply interrupt acknowledge to reset a pending interrupt.

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| BSY | DRDY | DWF | DSC | DRQ | CORR | IDX | ERR |

See the description of the Status register for definitions of the bits in this register.

## 12.12 Digital Output Register

(-CS1, address 6, write only). This register contains two control bits as follows:

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| – | – | – | – | – | SRST | -IEN | – |

where:

**-IEN** is the enable bit for this disk drive interrupt to the Host. When this bit is active, and the drive is selected, the Host interrupt, +IRQ, is enabled, through a tri-state buffer, to the Host. When this bit is inactive, or the drive is not selected the +IRQ pin will be in a high impedance state, regardless of the presence or absence of a pending interrupt.

**SRST** is the Host software reset bit. The drive is held reset when this bit is active, and enabled when this bit is inactive.

-- these bits are not used.

## 12.13 Drive Address Register

(-CS1, address 7, read only). This register loops back the drive select and head select addresses of the currently selected drive. The bits in this register are as follows:

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| RSVD | -WTG | -HS3 | -HS2 | -HS1 | -HS0 | -DS1 | -DS0 |

where:

**RSVD** is reserved and undriven by the drive. When the Host reads the drive address register, this bit must be in a high impedance state.

**-WTG** is the write gate bit, which is active when writing to the disk drive is in progress.

**-HS3 through -HS0** are the one's complement of the binary coded address of the currently selected head. For example, if HS3- through HS0- are 1 1 0 0, respectively, head 3 is selected.

**-DS1** is the drive select bit for drive 1, and should be active when drive 1 is selected and active. -DS0 is the drive select bit for drive 0, and should be active when drive 0 is selected and active. It is important to note that Bit 7 is not driven for compatibility with the floppy drive address space. If your system is different, you may have to drive this bit when this register is read.

# 13.0 Command Register

All commands are decoded from the COMMAND Register. The Host interface shall be programmed by the Host computer to perform commands and will return status to the Host at command completion.

To issue a command load the pertinent registers in the Task File activate the interrupt enable bit, -IEN in the digital output register, and then write the command code to the command register. Execution begins as soon as the command register is written.

Also see the section on retries.

## 13.1 Recalibrate (Hex 1X)

This command will move the R/W heads from anywhere on the disk to cylinder 0. Upon receipt of the command, the drive sets BSY and executes a seek to cylinder zero. The drive then waits for the seek to complete before updating status, resetting BSY and generating an interrupt. If the drive cannot reach cylinder 0, the error bit is set in the Status register and the track 0 bit set in the error register. An aborted command response will be given if the drive is not spinning or is not on track. Upon successful completion of the command, the Task File registers will be as follows:

| | |
|---|---|
| Error Register | 00 |
| Sector Count | Unchanged |
| Sector Number | Unchanged |
| Cylinder Low | 00 |
| Cylinder High | 00 |
| SDH | Unchanged |

## 13.2 Read Sector(s)

| | |
|---|---|
| $20_H$ = | Read with Retries |
| $21_H$ = | Read without Retries |
| $22_H$ = | Read Long with Retries |
| $23_H$ = | Read Long without Retries |

This command will read from 1 to 256 sectors as specified in the Task File (sector count equal to 0 requests 256 sectors), beginning at the specified sector. As soon as the command register is written, the drive sets the BSY bit and begins execution of the command. An aborted command is set if bits 2 & 3 are not equal to zero. An ID not found error is returned if incorrect task file parameters are passed. If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, the drive begins searching for the appropriate ID field. If the ID is read correctly, the data field is read into the sector buffer, error bits are set if an error was encountered, the DRQ bit is set and an interrupt is generated. The DRQ bit is always set regardless of presence or absence of an error condition at the end of the sector. Upon command completion, the Task File registers contain the cylinder, head, and sector number of the last sector read. The sector count is zero after successful execution of the command.

A read long may be executed by setting the long bit in command code. The read long command returns the data and the ECC bytes contained in the data field of the desired sector. During a read long, the drive does not check the ECC bytes to determine there has been any type of data error. Data bytes are 16 bit transfers and ECC bytes are 8 bit transfers. During read long transfers only 4 bytes are transferred although 11 bytes of ECC are generated. The other 7 bytes of ECC are stored in the drives buffer. Therefore only single block Read longs are permitted and a read long must be performed before a write long.

## 13.3 Write Sector(s)

| | |
|---|---|
| $30_H$ = | Write with Retries |
| $31_H$ = | Write without Retries |
| $32_H$ = | Write Long with Retries |
| $33_H$ = | Write Long without Retries |

This command will write from 1 to 256 sectors as specified in the Task File (sector count equal to 0 requests 256 sectors), beginning at the specified sector. As soon as the command register is written, the drive waits for the Host to fill the sector buffer with the data to be written. No interrupt is generated to start the first buffer fill operation. Once the first buffer is full, the drive sets BSY and begins command execution. An ID not found error is returned if incorrect task file parameters are passed. If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, the drive begins searching for the appropriate ID field. If the ID is read correctly, the data loaded in the buffer is written to the data field of the sector, followed by the ECC bytes. Upon command completion, the Task File registers contain the cylinder, head, and sector number of the last sector written. The sector count is zero after successful execution of the command.

A write long may be executed by setting the long bit in the command code. The write long command writes the data and the ECC bytes directly from the sector buffer; the drive will not generate the ECC bytes itself for the write long command. Data byte transfers are 16 bits, ECC bytes are 8 bit transfers. During write long transfers only 4 bytes of ECC are transferred although the drive uses 11 bytes. In order to prevent an ECC error a read long must be performed on the sector first to save away the other 7 bytes of ECC. Only single block transfers are allowed.

## 13.4 Verify Sectors

| | |
|---|---|
| $40_H$ = | Read Verify with Retries |
| $41_H$ = | Read Verify without Retries |

This command functions similarly to the read sectors command except that no data is transferred to the host and at completion of the command the CORD bit is set if software ECC correction was required.

## 13.5 Format Track (Hex 50)

This command formats the track specified in the Task File. As soon as the command register is written, the drive waits for the Host to fill the buffer with the format data. When the buffer is full, the drive resets DRQ, sets BSY and begins command execution. If the drive is not already on the desired track, an implied seek is performed. Once at the desired track, formatting begins using the data in the sector buffer. Media defects may be marked bad on a sector level. At the completion of the track, the drive resets BSY and generates an interrupt.

The format information is made up of two bytes per sector on the track. The least significant byte is 00 if the sector is to be formatted normally, or $80_H$ if the sector is to be formatted bad. The most significant byte is the sector number. After writing the information for all the sectors on the logical track, the remaining bytes of the sector should be filled with zeroes. It should be noted that the data is written into the sector buffer with the least significant byte followed by the most significant byte. The sectors may be arranged in any order but they must contain two bytes per sector as previously described and they must be transmitted as the first "n" bytes ("n" = 2 x number of sectors per track) to the sector buffer.

If a zero sector or sector number greater than the maximum for the mode is transmitted, be it native or logical, an ID Not Found error will be set. If there are multiple bad sector numbers, the smallest illegal sector number will be stored in the sector number register in the Task File.

However, all legal sectors will be formatted according to the second byte before the error is posted.

If a sector that was previously formatted bad is requested to be formatted good, an attempt will be made to format it good.

A descriptor byte of 40H will cause the drive to logically assign the sector to an alternate sector in its set of spares. A descriptor byte of 20H will cause the drive to logically unassign the spare sector and recover the primary sector. This provides the capability to replace a bad sector. The spare sector is recovered.

### 13.6 Seek (Hex 7x)

This command initiates a seek to the track and selects the head specified in the Task File. The drive need not be formatted for a seek to execute properly. When the command is issued, the drive sets BSY in the Status register, initiates the seek, resets BSY, and generates an interrupt. Only the cylinder register and drive head register are valid for this command.

The drive does not wait for the seek to complete before returning the interrupt. Seek complete will be set upon completion of the command. If a new command is issued to a drive while a seek is being executed, the drive will wait, with BSY active, for the seek to complete before executing the new command. No checks are made on the validity of the Sector number in the Task File. The Error bit in the Status register and the ID Not Found bit in the Error register of the Task File will be set if an illegal cylinder number is passed.

## 13.7 Execute Drive Diagnostic (Hex 90)

This command performs the internal diagnostic tests implemented by the drive. The diagnostic tests shall only be executed upon receipt of this command. The drive sets BSY immediately upon receipt of the command.

If unsuccessful, it sets its error register as described below. The master drive resets BSY, and generates an interrupt. The value in the error register should be viewed as a unique 8 bit code and not as the single bit flags defined previously. The interface registers are set to initial values except for the error register if error.

The table below details the codes in the error register and a corresponding explanation:

| Error Code | Description |
|---|---|
| 01 | no error detected |
| 02 | formatter device error |
| 03 | sector buffer error |

Additional codes may be implemented at the manufacturer's option.

## 13.8 Initialize Drive Parameters (Hex 91)

This command enables the drive to operate as any logical drive type. By setting the Sector Count Register and Drive Head Register, this command allows the host to alter the drive's logical configuration. Subsequently, the drive operates or emulates any drive type of equal capacity.

When this command is executed, the drive reads the Sector Counter Register to determine the number of logical sectors per track and also reads the Drive Head Register to determine the number of logical heads per cylinder. Based on these two parameters and the drive capacity (number of sectors per drive), the number of logical cylinders is calculated by:

$$\#\ \text{cylinders} = \frac{\text{Drive Capacity (Sectors)}}{(\#\ \text{logical heads/cylinder})\ (\#\ \text{sectors/track})}$$

Upon receipt of the command, the drive sets BSY, saves the parameters, resets BSY, and generates an interrupt. To specify maximum heads, write 1 less than the maximum (e.g. write 4 for a 5 head drive). To specify maximum sectors, specify the actual number of sectors (e.g. 17 for a maximum of 17 sectors/track).

The cylinder value in the Task File is not checked for validity by this command. Therefore, if it is invalid, no error will be reported until an illegal access is made by some other command.

## Universal Translate Mode (Definition)

Conner has established a Universal Translate Mode which enables the user to configure the drive in an AT environment to any cylinder, head, and sector configuration desired. The translate configuration is limited only by the maximum capacity of the drive. Upon initial power up of the drive it will default to a predetermined configuration shown below:

| | No. of Cylinders | No. of Heads | No. of Sectors |
|---|---|---|---|
| **CP-2034** | 411 | 4 | 38 |
| **CP-2064** | 823 | 4 | 38 |

After the drive is ready, the host system may issue INIT DRIVE PARMS COMMAND (command code 91H) to alter the translate configuration (number of heads and number of sectors per track). The drive parameters will then be saved in EEPROM for subsequent drive operations.

## 13.9 Power Commands

Commands EO through E3 and E5-E6 constitute the power commands. The following table describes these commands:

| Command | Drive Action |
|---|---|
| EO | The drive enters STANDBY MODE immediately. |
| E1 | The drive enters IDLE MODE immediately. |
| E2 | The drive enters STANDBY MODE immediately. If the Sector Count register is non-zero then the Auto Power-Down feature is enabled and will take effect when the drive returns to IDLE MODE. If the Sector Count register is zero then the Auto Power-Down feature is disabled. |
| E3 | The drive enters the IDLE MODE immediately. If Sector Count register is non-zero then the Auto Power-Down feature is enabled and will take effect immediately. If the Sector Count register is zero, then the Auto Power-Down feature is disabled. |

E5 Puts $FF_H$ in Sector Count register if drive is in the IDLE MODE. Puts $00_H$ in Sector Count register if drive is in, going to, or recovering from the STANDBY MODE. Puts a $BB_H$ in the sector count register if power lock is enabled.

E6 The drive enters the SLEEP MODE. A reset is required to bring the drive out of sleep mode.

*Note: Minimum power off/on cycle time should be no less than 3 seconds.*

All of the power commands except command E6 will execute immediately and return the ending interrupt after the spin up/down sequence is initiated.

Note that if the drive is already spinning (IDLE MODE) and a spin up command is issued from the host, the spin up sequence is not initiated.

Similarly, if the drive is in the STANDBY MODE and the host issues a spin down command, the spin down sequence is not initiated. Return of the ending interrupt does not mean that the drive has fully transitioned to the desired operating mode. The sleep command is the exception. In command E6, the drive is spun down and when it is stopped, the drive returns the ending interrupt and the SLEEP MODE begins.

When enabling the Auto Power-down feature, the value in the Sector Count register specifies the number of 5 second increments for the time-out value. If the drive does not receive a command within the specified time, the drive will enter the STANDBY MODE. The minimum time-out value is 60 seconds which means the smallest value for the Sector Count register is 12 when enabling the Auto Power-down feature.

If a number between 1 and 11 inclusive is specified in the Sector Count register, a value of 12 is used. This prevents overheating of the drive during spin up/down sequences.

The maximum allowable time-out value is 1000 seconds, or 16.6 minutes, resulting in a maximum Sector Count register value of 200. If a number greater than 200 is specified, a value of 200 is used.

Assertion of Host Reset will only affect the current state of the SLEEP MODE. If the drive is in SLEEP MODE and Host Reset is asserted, the drive wakes up into STANDBY MODE. Note that the drive will not return to the state it was in when the host issued the sleep command. The default power-on condition of the drive is IDLE MODE.

### 13.10 Read Multiple Command (Hex C4)

The read multiple command performs similarly to the read sectors command except that data transfers are multiple sector blocks and the long bit is not valid. Command execution is identical to the read sectors operation but with several sectors transferred to the Host as a block without intervening interrupts and only requiring DRQ qualification of the transfer at the start of the block count on each sector. The block size, which is the number of sectors to be transferred as a block, is programmed by the set multiple mode command which must be executed prior to the read multiple command. When the read multiple command is issued, the sector count register will contain the number of sectors (not the number of blocks or the block count) requested. If this sector count is not evenly divisible by the block size, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer will be for N sectors, where:

N = (sector count) module (block size)

If the read multiple command is attempted before the set multiple mode command has been executed or when read multiple commands are disabled, the read multiple operation will be rejected with an aborted command error.

Disk error encountered during read multiple commands will be reported at the beginning of the block or partial block transfer, but DRQ will still be set and the transfer will take place as it normally would, including transfer of corrupt data, if any. Subsequent blocks or partial blocks will only be transferred if the error was a correctable data error.

All other errors will cause the command to stop after transfer of the block which contained the error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

### 13.11 Write Multiple Command (Hex C5)

The write multiple command performs similarly to the write sectors command except that the controller sets BSY immediately upon receipt of the command, data transfers are multiple sector blocks, and the long bit is not valid.

Command execution is identical to write sectors operation but with several sectors transferred to the host as a block without intervening interrupts and only requiring DRQ qualification of the transfer at the start of block, not on each sector. The block size, which is the number of sectors to be transferred as a block, is programmed by the set multiple command. When the write multiple command is issued, the sector count register will contain the number of sectors (not the number of blocks or the block count) requested. If this sector count is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer will be for N sectors, where

N = (sector count) module (block size)

If the write multiple command is attempted before the set multiple mode command has been executed or when write multiple commands are disabled, the write multiple operation will be rejected with an aborted command error.

All disk error encountered during write multiple commands will be reported after the attempted disk write of the block or partial block transferred. The write operation will end with the sector in error, even if it was in the middle of a block. Subsequent blocks will not be transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block (exception: no interrupt is generated prior to the first block transferred).

## 13.12 Set Multiple Mode (Hex C6)

This command enables the controller to perform read and write multiple operations and establishes the block size for these commands. Prior to command issuance, the sector count register should be loaded with the number of sectors per block. The controller supports block sizes of 2, 4, 8, 16, 32, and 64 sectors. Upon receipt of the command, the controller sets BSY and looks at the sector count register contents. If the register contents are a valid and supported block size, that value is loaded for all subsequent read and write multiple commands and execution of those commands is enabled. Any unsupported block size in the register will result in an aborted command error and read and write multiple commands being disabled.

If the sector count register contains 0 when the command is issued, read and write multiple commands will be disabled. Once the appropriate action has been taken, the controller reads BSY and generated an interrupt. At power up the default mode is to have read and write multiple disabled.

## 13.13 Read Buffer (Hex E4)

The read buffer command allows the Host to read the current contents of the drive's sector buffer. Only the command register is valid for this command. When this command is issued, the drive will set BSY, set up the sector buffer for a read operation, set DRQ, reset BSY, and generate an interrupt. The Host may then read up to 512 bytes of data from the buffer. If the cylinder high and low registers are loaded with $599A_H$ then a count may be specified from 1 to the maximum number of blocks available. If the count is valid, then that many blocks will be read into the buffer. If the number of blocks requested is greater than the buffer size, an aborted command will be returned.

## 13.14 Write Buffer (Hex E8)

The write buffer command allows the Host to overwrite the contents of the drive's sector buffer with any data pattern desired. Only the command register is valid for this command. When this command is issued, the drive will set BSY, set up the sector buffer for a write operation, set DRQ, reset BSY, and generate an interrupt. The Host may then write up to 512 bytes of data to the buffer. If the cylinder high and low registers are loaded with $599A_H$, then a count may be specified from 1 to the maximum number of blocks available. If the count is valid, then that many blocks may be written to the buffer. If the count is not valid, an aborted command will be returned.

## 13.15 Identify Drive (Hex EC)

The identify command allows the Host to receive parameter information from the drive. When the command is issued, the drive sets BSY, stores the required parameter information in the sector buffer, sets the DRQ bit, and generates an interrupt. The Host may then read the information out of the sector buffer. The parameter words in the buffer are arranged as follows, all reserved bits or words should be zeroes.

All numbers are given in hexadecimal format right justified. All reserved words are zero.

| | | |
|---|---|---|
| Word 00 | - | A constant 0A5A |
| Word 01 | - | Current logical # of cylinders |
| Word 02 | - | Number of removable cylinders |
| Word 03 | - | Current logical # of heads |
| Word 04 | - | Number of unformatted bytes/physical track |
| Word 05 | - | Number of unformatted bytes/sector. |
| Word 06 | - | Current logical # of sectors/track |
| Word 07 | - | Number of bytes in the inter-sector gaps |
| Word 08 | - | Number of bytes in the sync fields |
| Word 09 | - | 0000 |
| Word 10-19 | - | Serial number |
| Word 20 | - | Controller type<br>0003 dual ported multiple sector buffer with LOOK AHEAD READs. |
| Word 21 | - | Controller buffer size in 512 byte increments |
| Word 22 | - | Number of ECC bytes passed on read/write long commands |
| Word 23-26 | - | Controller firmware revision |
| Word 27-46 | - | Model number |
| Word 47 | - | Number of sectors/interrupt (0 = does not support >1) |
| Word 48 | - | Double word transfer flag (0 = not capable, 1 = capable) |
| Word 49 | - | Assign Alternate (0 = not capable, 1 = capable, See Format Description) |
| Word 50 | - | Mode for PIO |
| Word 51 | - | Mode for DMA |
| Word 52-127 | - | Reserved |
| Word 128 | - | Native number of cylinders |
| Word 129 | - | Native number of heads, sectors |
| Word 130 | - | Default logical number of cylinders |
| Word 131 | - | Default logical number of heads, sectors |
| Word 132 | - | Interface flag, Drive Feature bytes. |

bit F - Unused
bit E - Lookaheads enabled when set
bit D - Format bad request detected
bit C - Translate mode active when set
bit B - Disable multiple block r/w/v
bit A - Reserved
bit 9 - Reserved
bit 8 - Reserved
bit 7 - Reserved
bit 6 - Reserved
bit 5 - Special reset mode
bit 4 - Reserved
bit 3 - Reserved
bit 2 - Reserved
bit 1 - 1 if 15 sec min auto time-out
bit 0 - 0 to enable the power commands

Word 133 - FFFF if power commands supported
Word 134 bits F-2 - RSVD
bit 1 - CAM Compliant
bit 0 - Universal Translate
Word 135 MSB-Age LSB-Program
Word 136-255 - Reserved

### 13.16 Set Buffer Mode (Hex EF)

This command provides capability to enable or disable the LOOK AHEAD READ capability. "$AA_H$" in the write precomp register enables LOOK AHEAD READs. Any other value in the write precomp register will result in an aborted command error. The default state on power up or reset is LOOK AHEAD READ enabled. "$55_H$" disables LOOK AHEAD READs.

## 13.17 Translate Command (Hex F1)

The command uses parameters passed to the drive in the cylinder high, cylinder low, head drive, and sector number registers. These values are then translated into the physical location on the drive and values are passed back through their respective registers and a interrupt is sent. An $AA_H$ must be loaded in the precomp register or an aborted command will result.

## 13.18 Physical Seek (Hex F2)

The command uses parameters passed to the drive in the cylinder high, cylinder low, and drive head registers. The parameters are checked for validity and if correct a seek is performed to that physical location on the drive. An interrupt will be sent at the start of the seek and busy cleared. When the seek is complete the seek complete bit in the status register will be set. Valid cylinder parameters will be 5 to max. cyl. (from ID command word 128) if the sector count register contains any value other than $FF_H$. If the sector count register contains $FF_H$ then an offset of 8 will be added to the value in the Cylinder Registers. Valid head parameter will be from 0 to max head - 1 (from ID command word 129 most significant byte). An $AA_H$ must be loaded in the precomp register or an aborted command will result.

## 13.19 Defect List (Hex F5)

The command returns three Factory Defect List in 6 blocks. The first 4 blocks being the skip list and the last 2 blocks being the alternate list. The drive will set the sector count register to 6 at the start of the command and is the only register altered as the data is read. Defect information is returned with a 4 byte header followed by 7 byte defect descriptors. The format of the Data is as follows:

Byte 0 - error log #
Byte 1 - error log type 0 or 2
Byte 2, 3 - reserved

Seven byte defect descriptors follow in the following format:

Byte 0 - Error Code
Byte 1 - Cylinder High
Byte 2 - Cylinder Low
Byte 3 - Head
Byte 4 - Sector
Byte 5 - Sense
Byte 6 - Count

Each of the logs are 2 blocks long. The error log #'s will be 2A and 2B for skip logs and 2C for alternate logs. The error code is $50_H$ for the skip list and $51_H$ for the alternate list. An $AA_H$ must be loaded in the precomp register or an aborted command will result.

If the precomp register is loaded with a $BB_H$ then a scan ID will be performed. The drive will take the physical, not logical, parameters from the cylinder high, cylinder low and drive head registers and scan that track's ID for alternates. The results will be returned in two 512 byte blocks in the same format as used for the factory defect list.

## 13.20 Enable Index (Hex F6)

This command enables an index pulse to be generated by the drive. This pulse is located physically in the same spot across the entire disk. This command will degrade performance of the drive so should only be used for diagnostic purposes. An $AA_H$ must be loaded in the precomp register or an aborted command will result.