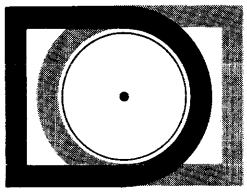
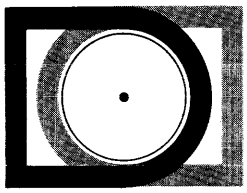


DATA DISC
INCORPORATED

F Series Disc Memory
ELECTRONICS MANUAL



DATA DISC
INCORPORATED

F Series Disc Memory
ELECTRONICS MANUAL

This manual should be used with the Data Disc F Series Input/Output Manual and F Series Application Notes. These items provide all necessary information for understanding and operating the Data Disc F-Series Memory System.

DATA DISC, INC. • 1275 California Ave. • Palo Alto, California 94304 • (415) 326-7602

WARRANTY

Data Disc F Series equipment is warranted against defects in workmanship and materials, and to meet the summary functional specifications quoted in the F Series Input/Output Manual supplied at the time of purchase, for a period of one year from date of shipment to the original purchaser.

The warranty obligation is limited to replacing or repairing parts not subjected to misuse, neglect, non-factory repair, alteration, or accident which prevent specifications from being met, using only equipment operated normally and properly within specified application and environmental conditions, following proper installation and adjustment in accordance with the instruction manual furnished with the equipment.

This warranty does not cover, nor shall Data Disc be liable for, any contingent damages such as, but not limited to, accidental loss of stored data, damage to other equipment used in conjunction with Data Disc equipment, etc., arising out of the sale or use of defective equipment, whether used properly or not, and is in lieu of all other warranties expressed, implied, or statutory.

Data Disc is not obligated to retrofit earlier models of equipment in the field with features not available at the time of shipment. These earlier models, for a negotiated charge, can be updated to include later improvements, optional features, and accessories.

The purchaser must obtain prior approval from Data Disc to return equipment to be repaired at the factory in Palo Alto, California. Return shipment shall be at the expense of the purchaser. Data Disc shall have the final right of determination as to the existence or cause of a defect, the need for and the time required for warranty repair at the factory or in the field, and its liability for expenses incurred in warranty investigation, replacement, or repair.

Printed in U. S. A. 200 7-67

Table of Contents

List of Figures

continued...

List of Drawings

NOTE: Where applicable, the component location drawing is printed on the back of the schematic drawing.

This page purposely left blank.

Section 1
Installation Instructions

1.1 UNPACKING

Each F Series system is shipped in a custom-built shipping case designed to provide maximum protection.

WARNING

Exercise the utmost care during unpacking to ensure that the equipment is not damaged. All electronic and mechanical components are mounted in their operating positions in the rack-mounting tray when the unit is shipped.

Check the contents carefully against the enclosed packing list for loss or damage which may have occurred during shipment. Despite the use of carefully engineered packaging materials, there is a possibility that the equipment may have been damaged in transit. If such has occurred, immediately notify the responsible carrier and the local Data Disc representative.

NOTE: DO NOT OPERATE THE F-UNIT WITH THE DUST COVER REMOVED.

1.2 SYSTEM PLANNING CONSIDERATIONS

1.2.1 Location

F Series units are designed for location where the ambient temperatures and humidity do not exceed the limits defined in the specifications. Rackmounting places disc rotation in a horizontal plane. The F Series is not designed for mobile use and any shock and vibration must not exceed the specification.

1.2.2 Input/Output Lines

The F Unit communicates with a controller through two Input/Output cables. One cable carries 25 control and data lines, the other carries three control lines and dc power for the F-Unit. The signal lines are terminated as shown in the drawings and tables in Section 2 of the F-Series Input/Output Manual. Connector-pin assignments for the two Input/Output cables are also shown in Section 2.

NOTE: Cable lengths should be kept to 5 ft. maximum. Excessive cable length can cause deterioration of system performance.

1.3 INSTALLATION

1.3.1 Outline Dimensions

Figure 1-1 shows the outline for the F Series recorder in its standard rackmounting configuration.

1.3.2 Rackmount Installation

The F Series is designed for installation into standard 19-inch-wide equipment racks or cabinets, with the disc rotation in a horizontal plane. Installation requires bolting the front panel to the rigid mounting frame of the rack or cabinet with four 10-24 x 5/8" screws. The tray may also be mounted with most standard chassis-slide sets.

1.3.3 Electrical Connections

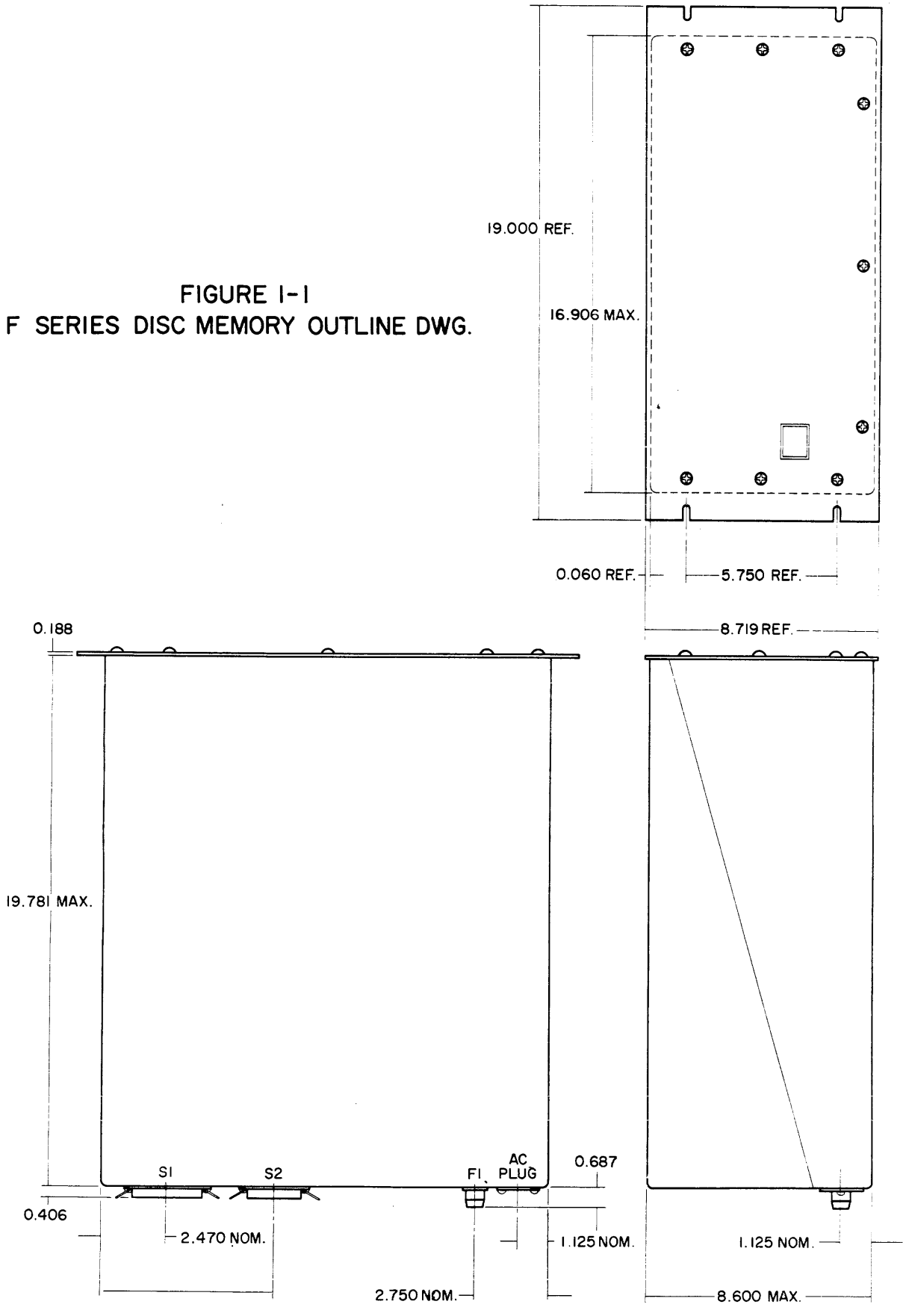
Electrical connection to a source of 120 volt, 60 cycle, single-phase ac is through a grounding-type connector at the back of the tray. An 8-foot-long cord with mating connectors is supplied.

Signal- and dc-power connections to the back of the tray are made to two Amphenol connectors, Nos. 57-40500, and 57-40360. The mating connectors 57-30500 and 57-30360, respectively are supplied. Connections are detailed in Tables 3 and 4 of the F Series I/O Manual.

Specifications

DISC SPEED	1,800 RPM $^{+1.3\%}_{-3.0\%}$
DATA RATE	3.0 mbps $^{+1.3\%}_{-3.0\%}$
DATA CAPACITY	100,000 data bit cells per track
TEMPERATURE	
Operating	50°F to 105°F, less than 20°F change per hour
Non-operating	-20°F to $+130^{\circ}$F
HUMIDITY	
Operating	20% to 80% R.H. without condensation
Non-operating	To 90% R.H. without condensation
ATMOSPHERE	Corrosive atmospheres such as those present in steel and chemical plants are not considered normal.
VIBRATION	Floor vibration of 0.15 g's maximum in the frequency range of 10 to 65 Hz (cps).
SHOCK	The disc package shall withstand a maximum shock of 5 g's in any direction without damage under operating and non-operating conditions.
A-C POWER (Apply D-C with or before A-C)	120V±10%, $60^{+0.5}_{-1.5}$ Hz (cps), single phase. 8.2A starting, 1.6A running. A-C ground connects to front panel, rackmount tray, and cover. A-C ground and D-C ground are isolated.
D-C POWER (Apply D-C with or before A-C)	+3.6V @0.8 Amps. ±1% +10V @0.4 Amps. ±1% -10V @0.8 Amps. ±1% +20V @0.2 Amps. ±1% 100 mv ripple allowable on all D-C supplies. D-C ground connects circuit ground and the entire shock-mounted assembly within the case. D-C ground and A-C ground are isolated.
SIZE & WEIGHT	8.7 X 19 X 19.8 inches, 62 pounds

FIGURE 1-1
F SERIES DISC MEMORY OUTLINE DWG.



This page purposely left blank.

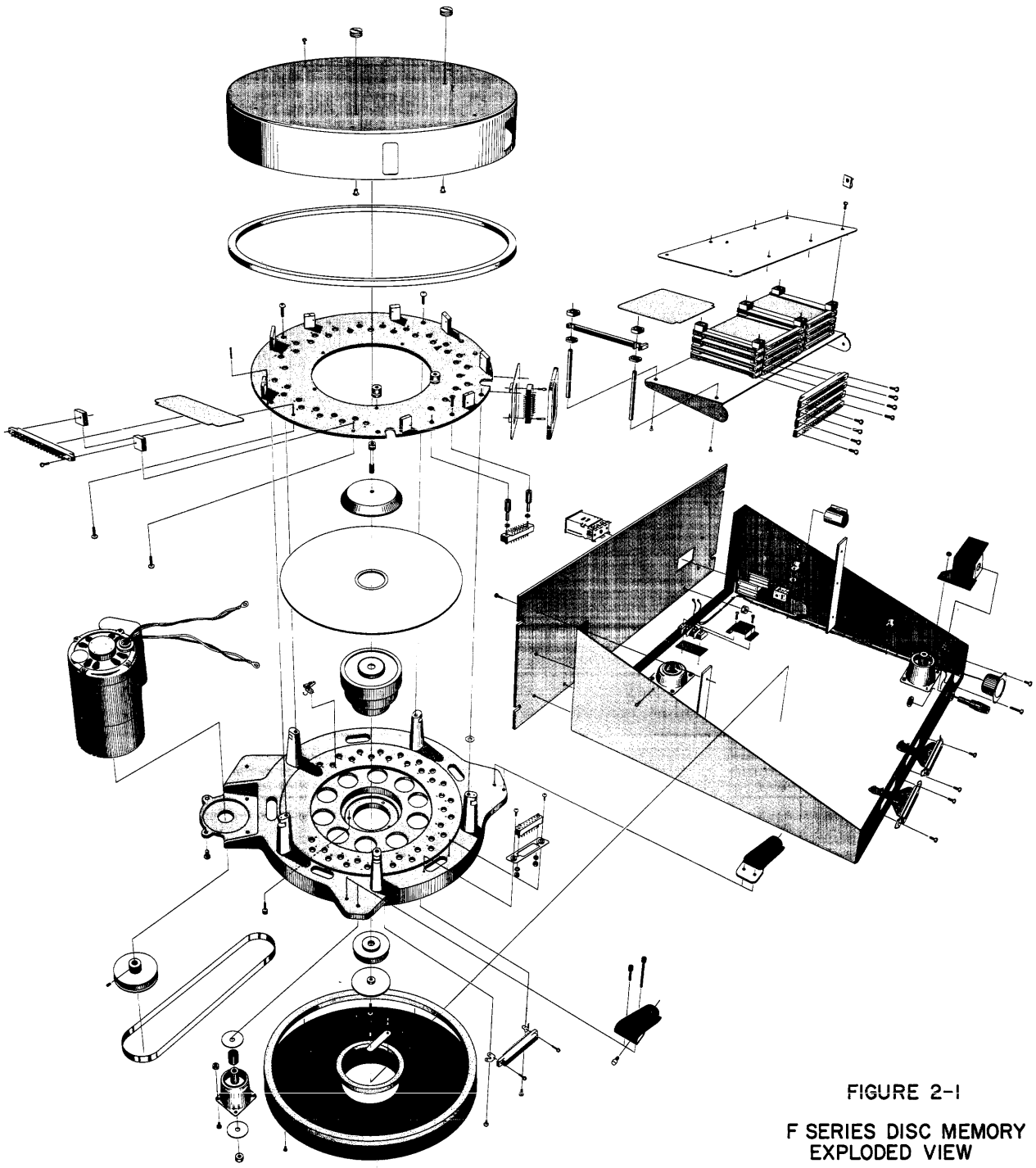


FIGURE 2-1

F SERIES DISC MEMORY
EXPLODED VIEW

This page purposely left blank.

Section 2
Introductory Description

2.1 GENERAL DESCRIPTION

The F Series Disc Memory System is a random-access memory module for interface with digital computers and/or other digital devices.

The F Series Disc Memory System accepts a serial digital input, records it by saturation magnetic recording at up to 3300 bits per inch, and delivers a clocked serial digital output of the memory content on command.

For example, the F3 Model provides 3.2 million bits of storage on 32 data tracks on a single 12-inch disc. The disc-rotation rate of 1800 RPM provides an average access time of 16.7 milliseconds and a data transfer rate of three million bits per second.

2.2 MECHANICAL PACKAGE

The complete memory module with electronics (as shown in the exploded view Figure 2-1) is housed in a rackmountable assembly measuring 8-3/4 x 19 x 19-3/4 inches. The disc rotates in a horizontal plane with 32 fixed data heads located to provide 16 discrete tracks on each side of the disc in an annulus about 1-1/2 inches wide near its perimeter. A minimum of six spare heads which can electrically replace any data head are provided with each unit. Two clock heads are located on the top surface of the disc.

2.3 DISC AND HEADS

The 12-inch aluminum disc used in the F Series has a plated magnetic-recording medium. Magnetic heads used in the Data Disc F Series Memory Systems have been specially developed for high-density contact recording and reproducing.

The contact plane of each head is determined by three points, the transducer and two bearing points carried on the gimballed transducer-support platform. This lightly loaded three-point contact provides for stability, compliance, and long service life. Tracks recorded by the heads are 24.5-mils wide with a 5.5-mil guard band between each track.

2.4 ELECTRONICS

The electronic system contains a single read amplifier for the data heads. Data are written onto or read from only one data track at a time. An electronic head-switching matrix provides interconnection between the read and write amplifiers and any one of the data heads. Each clock track has its own read amplifier. The bit-clock track is used as a timing source for writing data. The sector-clock track divides the data tracks into conveniently sized sectors. The sector clock track is not pre-formatted, so the user can format the disc to fit his application. The electronics

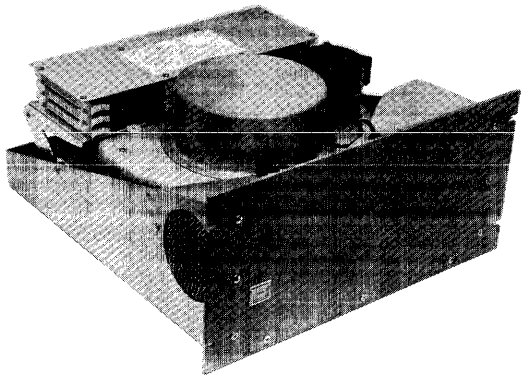


Figure 2-2 Front view

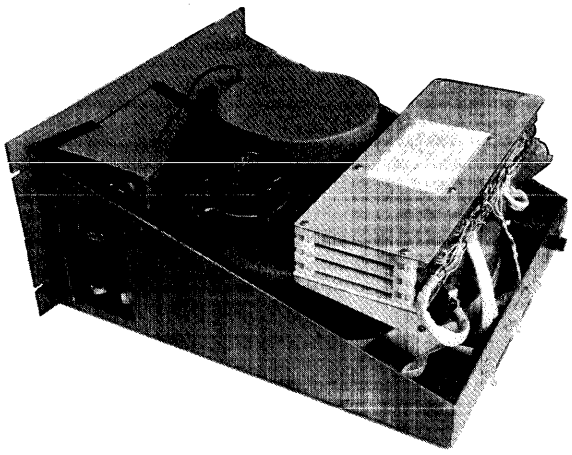


Figure 2-3 Rear view

system also includes read/write control circuitry, an encoder for translating dc-level binary input data into a self-clocking, modified NRZ data for writing, a decoder for retranslating from modified NRZ to dc-level binary data output, and read-clock derivation circuits.

2.5 INTRODUCTION TO OPERATIONS

2.5.1 Head Selection and Writing

The data heads are arranged electrically into a two-dimensional selection matrix where a particular head may be selected by defining the two coordinates of the head. In Figure 2-4, four heads are shown arranged in a 2 x 2 matrix. The X_1 Y_1 head has been selected by turning on transistor Y_1 and the two X_1 transistors. A small amount of current (about 1 milliampere) flows along the indicated path to establish electrical connection between the X_1 Y_1 head, the read-amplifier and the write-amplifier.

During write, the write-amplifier switches current (100 milliamperes) alternately between the two halves of the selected head. In the drawing, when write current flows through the top half of the X_1 Y_1 head, a magnetic

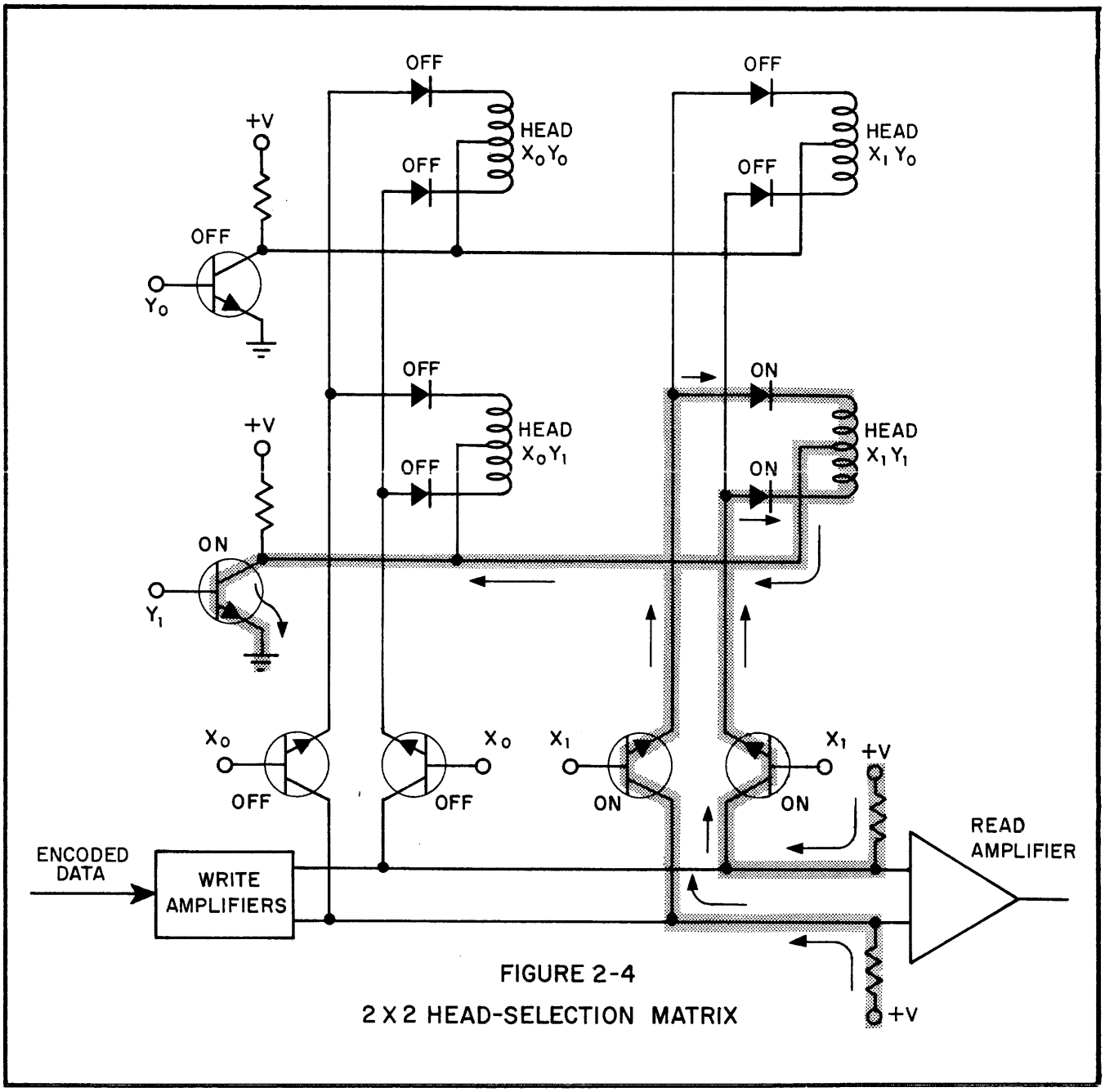


FIGURE 2-4
2 X 2 HEAD-SELECTION MATRIX

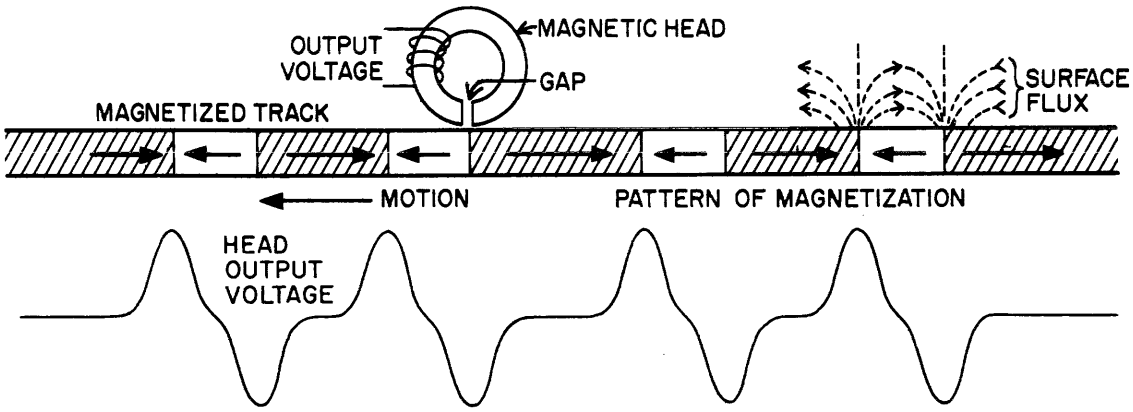


FIGURE 2-5
MAGNETIC RECORDING DETAILS

field is created by the transducer causing the portion of the track passing under the head at that time to be magnetized to saturation in one direction. When the write current flows through the bottom half of the X_1 Y_1 head, a magnetic field of the opposite polarity is created by the transducer causing the portion of the track passing under the head at that time to be magnetized to saturation in the opposite direction.

The change in the direction of magnetization, as shown in Figure 2-5, is a change in the magnetic flux direction, a term which can be abbreviated to a flux transition or simply a transition.

Saturation recording automatically removes data previously written on the track as new data are written over it.

In the F Series Disc Memory System, the matrix is expanded as more heads are used. For example, an eight-head system has an 8 x 1 matrix; a 16-head system has an 8 x 2 matrix; and a 32-head system has an 8 x 4 matrix.

2.5.2 Head Selection and Reading

As shown in Figure 2-5, a voltage pulse is generated in the magnetic read windings by a change of flux direction in the head caused by the change of surface magnetization passing through the gap in the magnetic head.

The minute currents associated with these millivolt pulses are differentially applied to the read amplifier through the path established, as shown in Figure 2-4.

2.5.3 Data Encoding & Decoding

Data are written serially upon the selected track by encoding the input data into a self-clocking code, using the bit clock track for timing.

The bit clock track delivers write clocks in synchronism with the instantaneous rotation rate of the disc memory. Writing timing errors due to speed variations are thereby eliminated.

Figure 2-6 shows data encoded into the modified non-return-to-zero (M-NRZ) code by the following rules:

a. The sync bit, a binary one, is inserted before the first data bit of a sector to provide a reference for encoding and decoding the first data bit.
b. A binary one causes a flux transition at the end of the bit cell.
c. A binary zero which was preceded by a binary one causes no flux transition in the bit cell.
d. A binary zero which was preceded by a binary zero causes a flux transition in the middle of the bit cell.

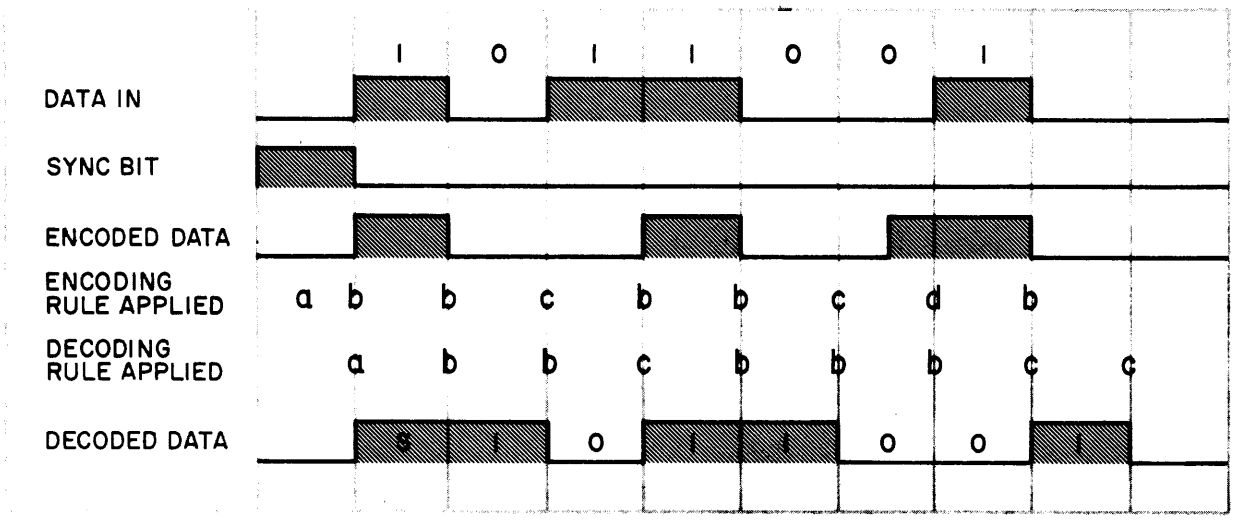


FIGURE 2-6

M-NRZ ENCODING/DECODING

Decoding rules for translating from the Modified NRZ data to the dc-level binary data output are:

a. The first transition of a sector is a binary one transition which occurs at the end of the sync bit cell.

b. If the previous bit cell was a binary one, the present bit cell is a binary one if and only if a transition occurs at the end of the bit cell $\pm 1/4$ bit cell (otherwise the present bit cell is a binary zero).

c. If the previous bit cell was a binary zero, the present bit cell is a binary zero if and only if a transition occurs in the middle of the bit cell $\pm 1/4$ bit cell. (Otherwise the present bit cell is a binary one designated by a transition at the end of the bit cell $\pm 1/4$ bit cell).

d. The decoded sync bit is removed from the data stream before the data are output.

2.5.4 Read Clock Derivation

At the high densities used for recording in the F-Series system, small mechanical variations which would be insignificant at lower densities contribute to timing deviations of up to a half bit cell between heads. These timing deviations, called "jitter," prevent use of the pre-recorded clock track for reading. A clock derived from the data itself is therefore necessary in order to achieve a synchronous clock.

A double-frequency (two cycles per bit cell) read clock is derived from the data by starting a voltage-controlled oscillator at the beginning of each sector and correcting the phase of the oscillator at each data transition.

2.5.5 Bit Level Error Detection

The modified NRZ coding guarantees a flux transition every one, one and one-half or two bit cells. Because flux transitions cannot be closer together than one bit cell nor farther apart than two bit cells, a simple check provides an effective bit-level error detection. This check detects over 50% of all possible errors occurring in random data.

Section 3
General Operation & Servicing

3. 1 GENERAL OPERATION

The F Series Disc Memory Unit interacts with a computer through an O. E. M. -supplied external controller as shown in Figure 3-1. The F Unit is connected to the Controller via the INTERFACE connectors. Refer to Application Note 004 on F-Series Controller Design.

The Functional Block Diagram Drawing 10683 shows inputs and outputs to the controller on the INTERFACE. The external controller directs the functions of Head Selection and Change, Data Reading, and Data Writing. The F-Unit provides timing information in the form of Track Origins, Sector Clocks and Read/Write (R/W) Clocks and status information such as Disc Ready, Read Error, and Read Inhibit.

The I/O Manual should be referenced for a general treatment of the Input/Output details.

3. 1. 1 Head Selection (ref: Drawing 10416)

The head-selection-matrix drawing shows the cards involved in head selection. The section of the text where their operation is explained is given below:

X-Drivers Card	(4. 7)
X-Selection and Input Network Card	(4. 8)
Y-Drivers & Write Amplifiers Card	(4. 9)

A head is selected by furnishing a ground to the center tap of the head through the Y driver and establishing a path for current flow through the input network, through the X-selection switches, and through the two diodes to the head. The X-selection switch is turned on by an X-driver.

3. 1. 2 Data Writing (ref: Drawing 10683)

When a head has been selected, it may be used to write data on its track. The head-selection-matrix drawing shows how the write-amplifiers (paragraph 4. 9) are connected to the selected head. The other cards involved in Write operation and the paragraphs explaining their operation are:

Write Control Card	(4. 10)
Bit Clock Read Amp Card	(4. 11)
Multipurpose Card	(4. 6)

The Bit-Clock Read-Amplifier Card provides the basic timing, the Write Control Card controls all Write operations and encodes the data. The Multipurpose card helps provide data protection by inhibiting write during turn-on and turn-off.

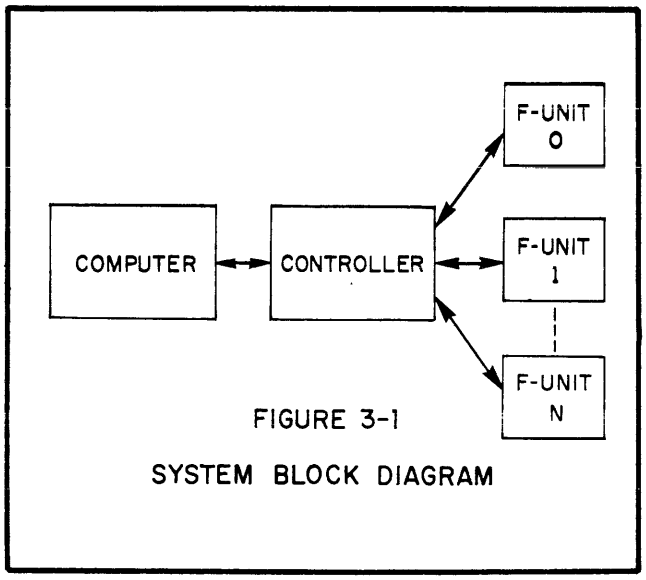


FIGURE 3-1

SYSTEM BLOCK DIAGRAM

3. 1. 3 Data Protection

Power to the F-Unit may be cycled ON or OFF in any manner with no danger of erasing data on the disc. The total design concept of the head-selection matrix, the Write amplifiers and Write-Turn-On circuits provides complete protection of data. Only three voltages (of the four supplied) are connected with the writing of data (1) +20 volts (2) +3. 6 volts and (3) -10 volts. Because write current is supplied by the +20 volt source, no data may be written while the +20 volts is OFF.

The following table shows how data protection is provided in all voltage conditions other than the operate condition, assuming that the +20 volts is ON.

DATA PROTECTION CONDITIONS (assumes +20v ON)		
+3.6 volts	-10 volts	Data Protection
OFF	OFF	Yes - No Y Selection.
OFF	ON	Yes - Write amplifier held off by -10 volts on base.
ON	OFF	Yes - WTO* line will be positive.

3.1.4 Data Reading (ref: Drawing 10683)

When a head has been selected, it may be used to read the data from its track. The head-selection-matrix drawing shows how the Read Amplifier (paragraph 4.11) is coupled through the input network (paragraph 4.8) to the selected head. Other cards involved in the read operation are:

Write Control Card	(4.10)
Read Control Card	(4.12)
VCO and Control Card	(4.13)

The Write Control Card provides the interface connection for the Read* line. The Read Control Card controls all read operations and decodes the data. A VCO and Control Card derives a double-frequency clock from the data transitions to provide basic timing for the read operation.

3.1.5 Clock Derivation & Timing (ref: Drawing 10683)

The clock used for synchronous encoding and writing of data is read from the Bit Clock Read Amplifier Card (paragraph 4.11). The clock used for decoding data is derived from the asynchronous data by the VCO and Control Card. A Sector Clock Read-Amplifier provides sector clocks as written by the user. The R/W Clock* output of the F Unit is either the bit-rate clock used for writing or the bit-rate clock derived during reading. Track Origin* is an output of the Multipurpose Card, created by sensing a gap in the bit clock track. Output circuits for the Clock Track (CT) signal and the Sector Clock* signal are also located on the Multipurpose Card.

As explained in Section 2.5.4, "jitter" can occur between any two heads. When worst-case timing deviations between the sector clock head and a data head are considered, it can be shown that if data are written under worst-case conditions (+ one-half bit relative jitter) and read under the opposite worst-case conditions (-one-half bit relative jitter), the total timing variation of the data head with respect to the sector clock head can amount to 1 bit cell.

An erase of at least one-half bit cell precedes the first transition to eliminate "previous-history-information" which, under worst-case "jitter" conditions, could remain to cause start-of-read timing errors.

The start of read, in a specific sector, is specified as beginning one bit cell (0.3 microseconds) after the start of write instead of at the same time, to compensate for read delays.

3.2 GENERAL SERVICE INFORMATION

Electronics components of the F Series are of conservative solid-state design and utilize proved integrated monolithic circuitry for logic functions.

Every plug-in module is a printed-circuit card. With the exception of the X-Select and Input Network and the diode cards, all cards are housed in the electronics card cage attached to the disc drive assembly. Cards are inserted into the cage with the component side up. Cards are secured in the cage by their connectors. When unlatched, the cage swings up for card installation, removal, or for mounting a card onto an extender card Accessory Part No. 10300 for troubleshooting or servicing. Note Figure 3-2.

The rear-view card and connector location guide, Figure 3-3, is provided on the card cage. Connections to the cards are by insertable contacts which are accessible for test measurements at the back of the card cage. Documentation Standards explaining pin numbering, symbols, and interconnection information are in the Appendix.

An asterisk is used in this manual to signify the logical inversion of a term. i.e., A is the same as the more conventional $\overline{A}$, read as not-A or A-not. As a general rule, an asterisk also signifies that the signal line is normally high and becomes low when active.

3.2.1 Electronic Servicing

Servicing of the F Unit is predicated first on modular replacement and secondly on component replacement. Each F Unit is supplied with spare Read/Write heads which may be electrically connected into the matrix in place of any other head. No adjustments to the F Unit electronics should be necessary unless a card containing an adjustable resistor is changed. There are four such cards in the F Unit. Three are read amplifiers and the fourth is the VCO and Control Card.

3.2.2 Mechanical Servicing

Mechanical servicing described in this Manual is limited to changing the motor, drive belt, and ground brush. Information contained in this Manual is not sufficiently detailed to permit safe mechanical disassembly or assembly. Mechanical servicing problems should be referred to the factory or to a factory-trained service representative.

WARNING

Do not operate the F-Unit with the dust covers removed. If it is necessary to replace any cards within the dust covers, the covers should be reinstalled prior to turning the machine on.

3.2.3 Head Location

The magnetic-recording heads have electrical addresses which are relatively independent of the heads' physical locations. Figures 3-4 and 3-5 give the mechanical head mounting hole numbers and location of diode cards and connectors.

Heads which have their black and white leads connected into Diode Board X0 (S6) will have "0" for the X portion of the XY selection address.

Head-selection lines for F3 units are Y0, 1, 4, 5 and X0, 1, 2, 3, 4, 5, 6, 7. Heads with X-selection lines 0, 1, 2, 3 will always be located on the base casting (bottom plate). Heads with X-selection lines 4, 5, 6, 7 will always be located on the top plate.

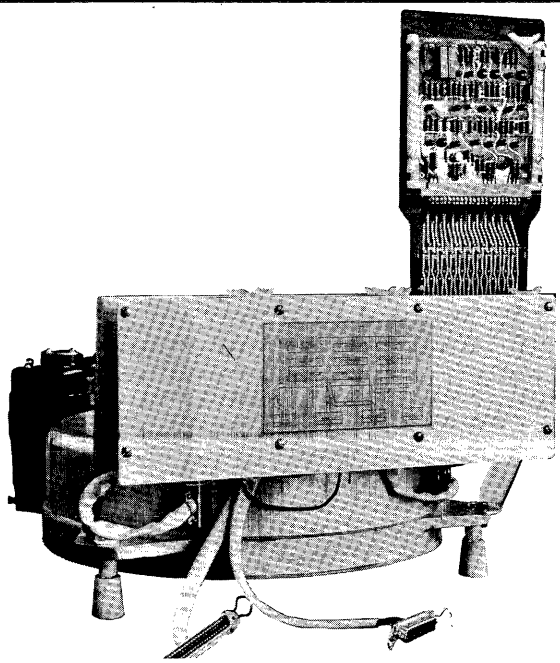


Figure 3-2 Card cage in servicing position, with one card on extender

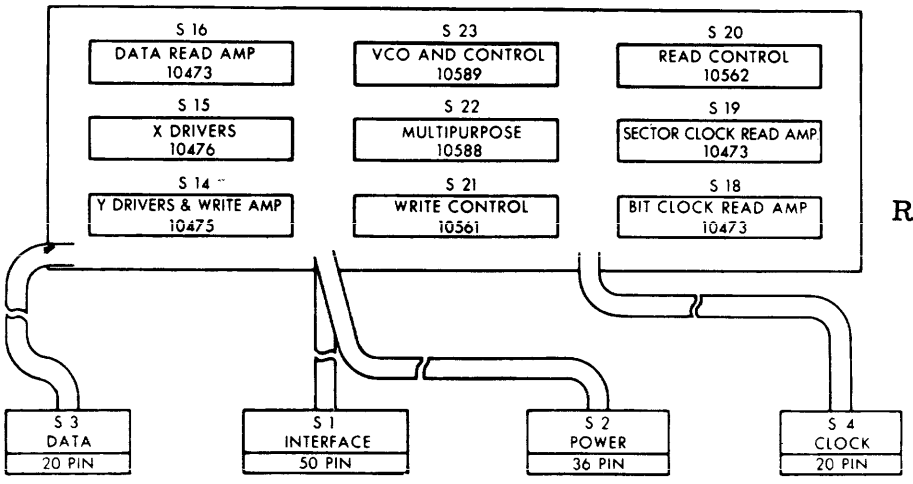


Figure 3-3 Card and connector location guide

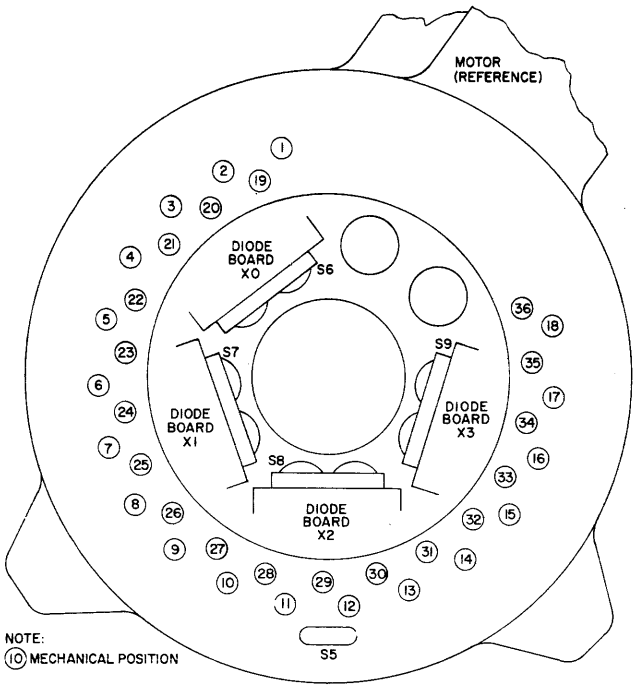


FIGURE 3-4

LOWER PLATE HEAD ASSEMBLY

MECHANICAL HEAD LOCATIONS

UNDERSIDE VIEW

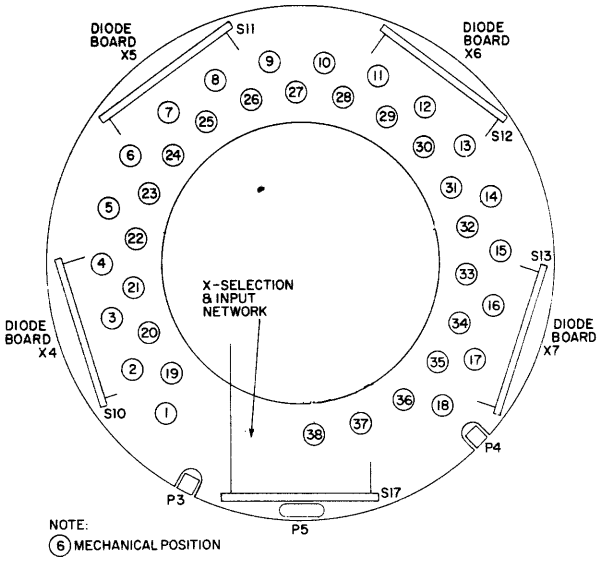
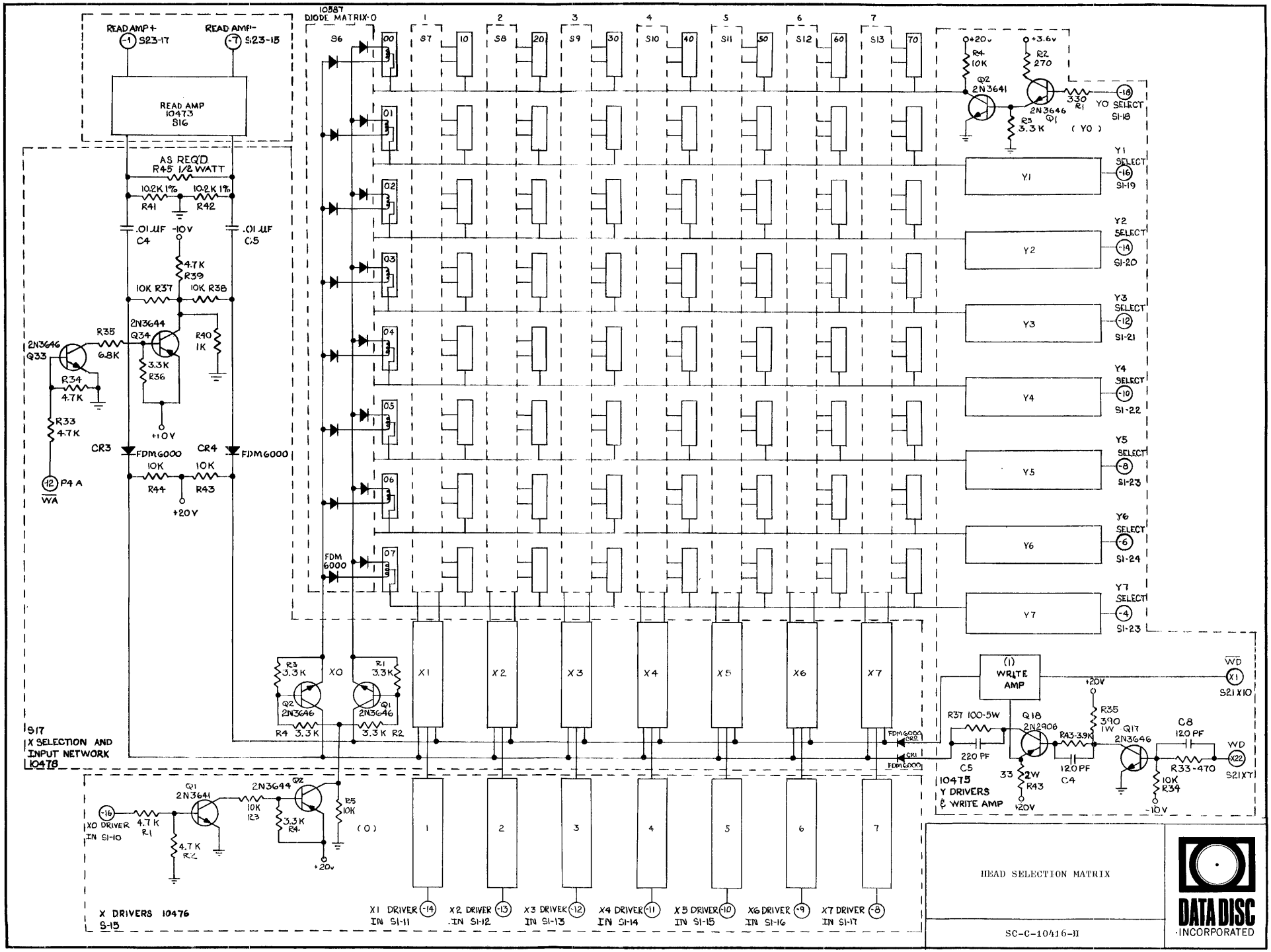


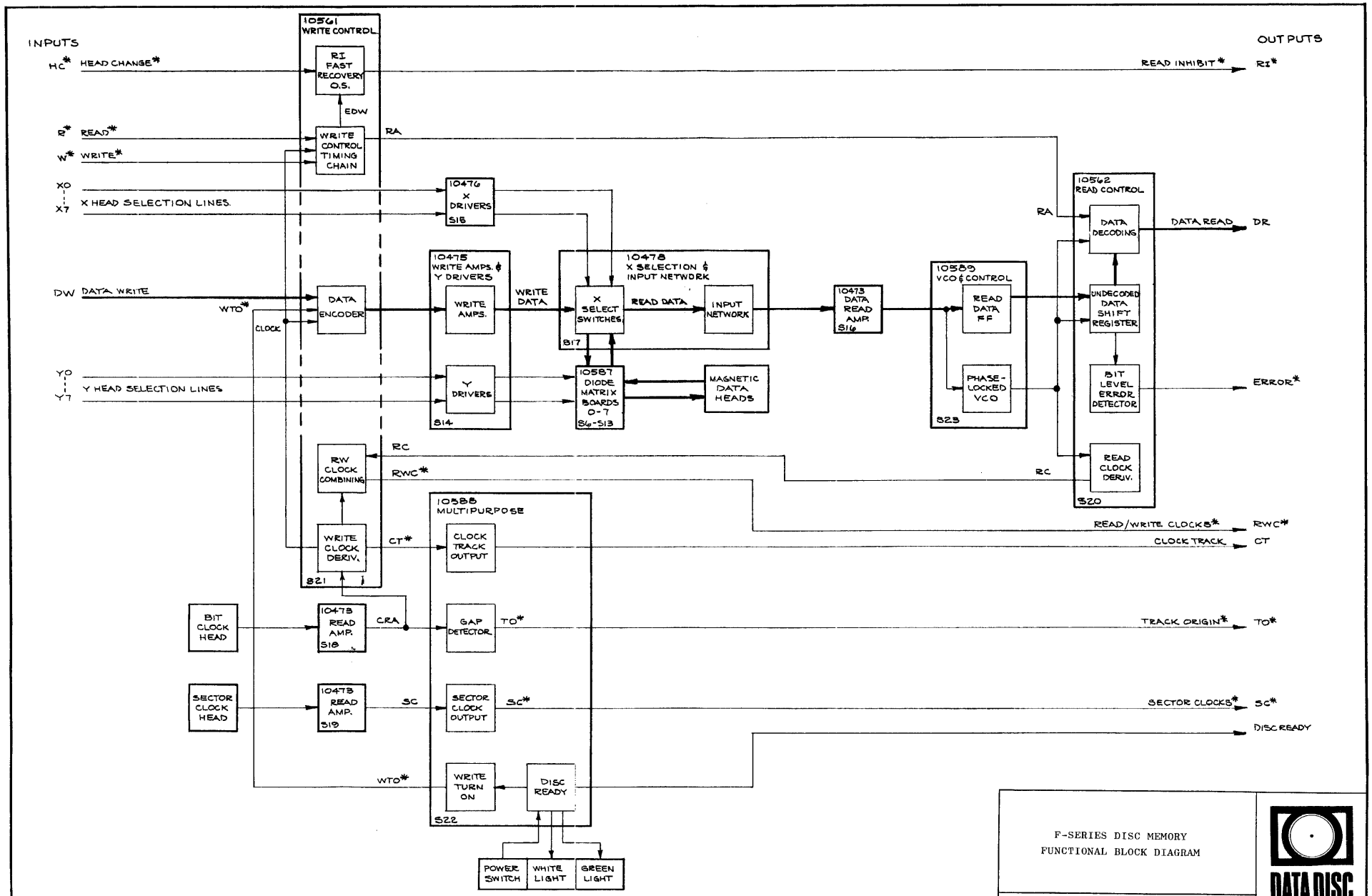
FIGURE 3-5

TOP PLATE HEAD ASSEMBLY

MECHANICAL HEAD LOCATIONS

TOP VIEW


READ AMP+
S23-17
READ AMP-
S23-18
READ AMP
10473
S16
10587
DIODE MATRIX-0
AS REQ'D
R45 1/2 WATT
10.2K 1%
R41
10.2K 1%
R42
.01 µF
C4
-10V
.01 µF
C5
4.7K
R39
10K R37
10K R38
2N3644
Q34
R35
6.8K
R40
1K
3.3K
R36
2N3646
Q33
R34
4.7K
R33
4.7K
+10V
CR3
FDM6000
CR4
FDM6000
10K
R44
10K
R43
P4 A
WA
+20V
FDM
6000
S6
S7
S8
S9
S10
S11
S12
S13
00
01
02
03
04
05
06
07
10
20
30
40
50
60
70
1
2
3
4
5
6
7
+20v
R4
10K
Q2
2N3641
+3.6v
R2
270
2N3646
Q1
330
R1
YO SELECT
SI-18
R3
3.3K
(YO)
Y1
SELECT
-16
SI-19
Y2
SELECT
-14
SI-20
Y3
SELECT
-12
SI-21
Y4
SELECT
-10
SI-22
Y5
SELECT
-8
SI-23
Y6
SELECT
-6
SI-24
Y7
SELECT
-4
SI-23
Y1
Y2
Y3
Y4
Y5
Y6
Y7
R3
3.3K
XO
R1
3.3K
X1
X2
X3
X4
X5
X6
X7
Q2
2N3646
Q1
2N3646
R4 3.3K
3.3K R2
FDM6000
CR2
CR1
FDM6000
(1)
WRITE
AMP
WD
X1
S21X10
+20V
R37 100-5W
Q18
2N2906
R35
390
1W
Q17
2N3646
C8
120 PF
WD
X22
S21XT
220 PF
C5
R43-3.9K
120 PF
C4
R33-470
10K
R34
33
2W
R43
+20V
-10V
10475
Y DRIVERS
& WRITE AMP
917
X SELECTION AND
INPUT NETWORK
10478
Q1
2N3641
2N3644
Q2
10K
R3
R5
10K
XO DRIVER
IN SI-10
-16
4.7 K
R1
4.7 K
R2
3.3K
R4
+20v
(O)
X DRIVERS 10476
S-15
X1 DRIVER -14 IN SI-11
X2 DRIVER -13 IN SI-12
X3 DRIVER -12 IN SI-13
X4 DRIVER -11 IN SI-14
X5 DRIVER -10 IN SI-15
X6 DRIVER -9 IN SI-16
X7 DRIVER -8 IN SI-17
HEAD SELECTION MATRIX
SC-C-10416-H
DATA DISC
INCORPORATED


INPUTS
OUTPUTS
10561
WRITE CONTROL
HC* HEAD CHANGE*
RI FAST RECOVERY O.S.
READ INHIBIT*
RI*
EDW
R* READ*
W* WRITE*
WRITE CONTROL TIMING CHAIN
RA
X0
X7
X HEAD SELECTION LINES.
10476
X DRIVERS
S16
10562
READ CONTROL
RA
DATA DECODING
DATA READ
DR
10475
WRITE AMPS. & Y DRIVERS
10478
X SELECTION & INPUT NETWORK
DW DATA WRITE
WTO*
CLOCK
DATA ENCODER
WRITE AMPS.
WRITE DATA
X SELECT SWITCHES
READ DATA
INPUT NETWORK
B17
10473
DATA READ AMP
S16
10589
VCO & CONTROL
READ DATA FF
UNDECODED DATA SHIFT REGISTER
Y0
Y7
Y HEAD SELECTION LINES
Y DRIVERS
10587
DIODE MATRIX BOARDS 0-7
S6-S13
MAGNETIC DATA HEADS
PHASE-LOCKED VCO
BIT LEVEL ERROR DETECTOR
ERROR*
S14
S23
RC
RW CLOCK COMBINING
RWC*
RC
READ CLOCK DERIV.
S20
10588
MULTIPURPOSE
READ/WRITE CLOCKS*
RWC*
WRITE CLOCK DERIV.
CT*
CLOCK TRACK OUTPUT
CLOCK TRACK
CT
S21
BIT CLOCK HEAD
10473
READ AMP.
S18
CRA
GAP DETECTOR
TO*
TRACK ORIGIN*
TO*
SECTOR CLOCK HEAD
10473
READ AMP.
S19
SC
SECTOR CLOCK OUTPUT
SC*
SECTOR CLOCKS*
SC*
DISC READY
WTO*
WRITE TURN ON
DISC READY
S22
POWER SWITCH
WHITE LIGHT
GREEN LIGHT
F-SERIES DISC MEMORY
FUNCTIONAL BLOCK DIAGRAM
BD-C-10683-A
DATA DISC
INCORPORATED

Section 4
Detailed Operation & Servicing

4.1 POWER SWITCH AND FUSE (Ref. Drawing 10651)

4.1.1 General Description

The unit is turned ON and OFF with a push-type switch, the illuminated POWER button on the left side of the front panel. The unit operates from 120-volts ac, supplied through the ac-input plug on the left side of the back of the chassis. A 6-1/4A Slo-Blo line fuse is located next to the input plug. The power switch also connects operating power to the Multipurpose Card (10588) and receives ground from the card for lighting the power switch lamps.

4.1.2 Functional Description

The unit is turned ON by pushing the POWER button on the front panel. The next time the POWER button is pushed, the unit is turned OFF.

When the unit is turned ON, 120 volts ac operates the drive motor and minus 10 volts dc operates the time delay and lamp drivers on the Multipurpose Card. Initially, the POWER button is illuminated by the WHITE lamps in the switch, indicating that the unit is NOT READY because the disc has not yet reached operating speed. After a 10-second delay, the POWER button is illuminated by the GREEN lamps in the switch, indicating that the disc is up to speed and the unit is READY for operation. There will be a 10-second delay every time the unit is turned ON, even if it has been OFF for only a moment and the disc has not slowed down an appreciable amount.

The power line is connected to the drive motor at terminal board TB-1.

4.1.3 Servicing

If the fuse blows, replace it with a 2A-SLO-BLO fuse.

If an indicator light in the POWER button goes out, replace it as follows:

a. Holding the plastic POWER button with your finger nails in the notches on either side, pull it out until it stops (approximately one inch).
b. Rotate the button one-quarter turn to either side (so that "POWER" is vertical), and push it in gently to disengage the catch.
c. Pull the button out as far as it will come, then tilt it down. This exposes the bases of the four lamps. The lamps may be pulled out of their sockets by their bases. Replace them with GE330 miniature flange base bulbs.
d. Insert the assembly back in the switch, and push the POWER button in as far as it will go.
e. While gently pushing the POWER button in, rotate it back one-quarter turn and push it all the way back into the switch.

4.2 CABLES AND CABLE ASSEMBLIES

4.2.1 General Description

There are five cables in the F unit--the shelf-wiring cable and the cables ending in connectors S1, S2, S3 and S4 (which will be referred to as cable S1, cable S2, etc.).

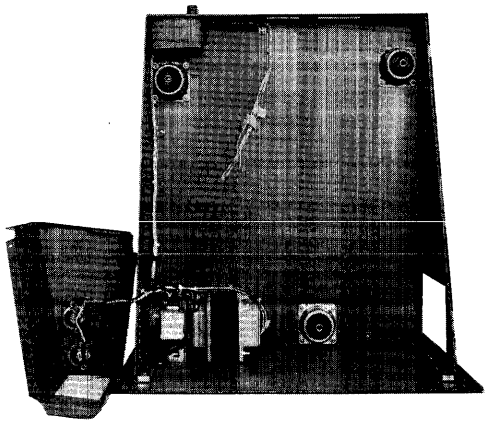


Figure 4-1 Shelf-wiring cable, disc unit removed

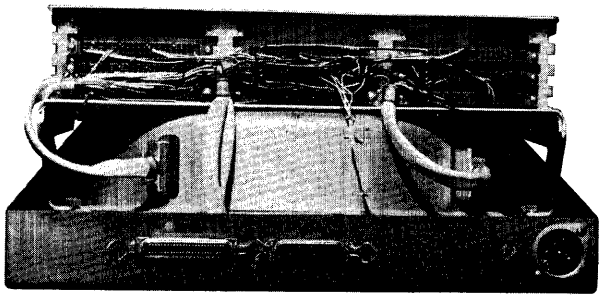


Figure 4-2 Rear view

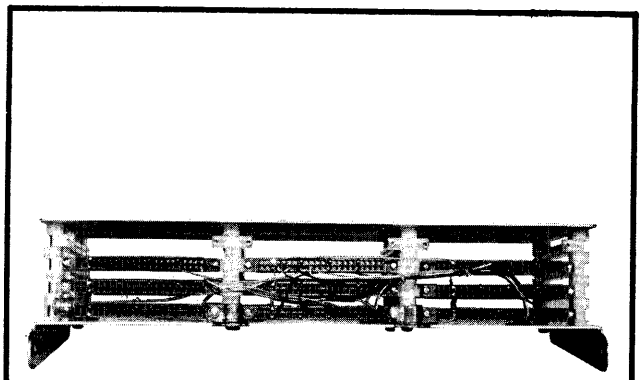


Figure 4-3 Card-cage interconnection wiring with Cables S1, S2, S3 and S4 removed

The shelf-wiring cable is laid out along the left inside edge of the chassis, from the ac plug to the power switch and drive motor as shown in Figure 4-1. Cables S1, S2, S3 and S4 are shown attached to the card-cage interconnection wiring in Figure 4-2.

There are three cable assemblies in the F unit—the card-cage interconnection wiring, the top-plate wiring harness, and the bottom-plate wiring harness.

The card-cage interconnection wiring shown in Figure 4-3 is the system of wires on the back of the card-cage which connects the printed-circuit cards with one another.

The top-plate wiring harness is strung around the periphery of the top-plate as shown in Figure 4-4.

The bit-clock head and sector-clock head are connected to 20-pin connector P4 with three-wire shielded cables. Each data head is connected to its diode-card connector by a twisted assembly consisting of a red, a white and a black wire attached to the connector as shown in Figure 4-5.

The bottom-plate wiring harness is strung around the center of the bottom-plate as shown in Figure 4-6.

Drawing #10651 details the cables and interconnections.

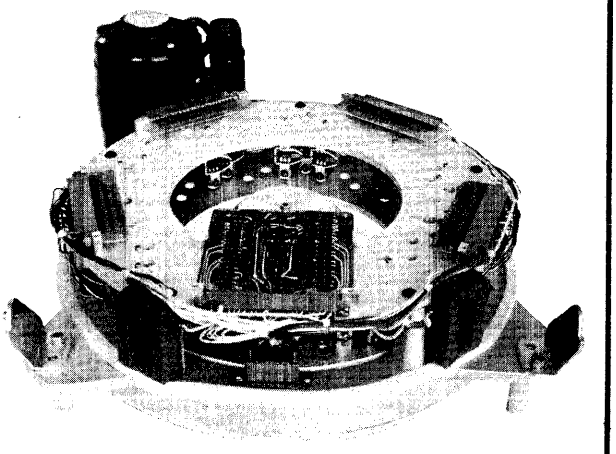


Figure 4-4 Top-plate wiring harness

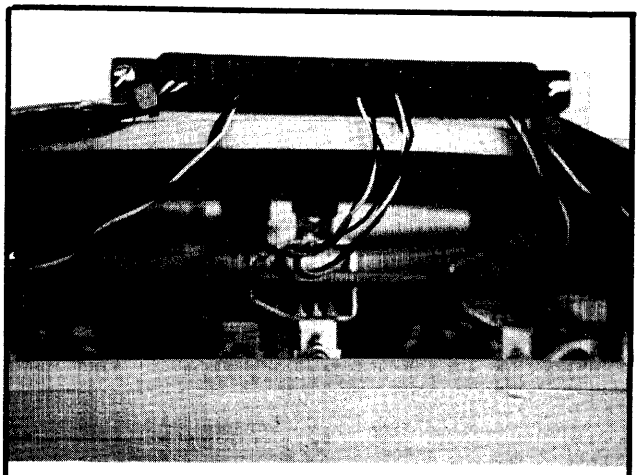


Figure 4-5 Data head/diode card connector wiring

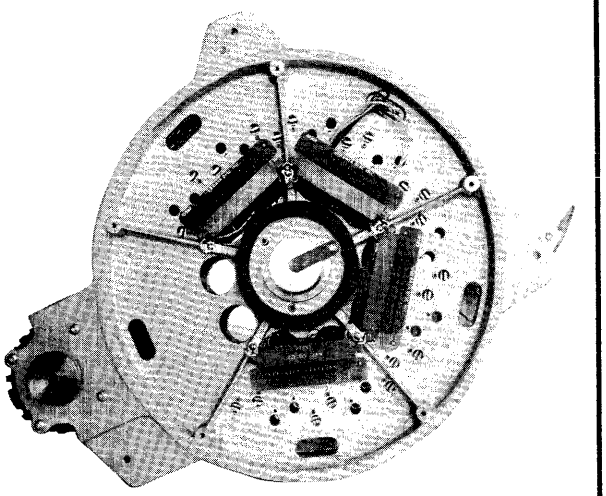


Figure 4-6 Bottom-plate wiring harness

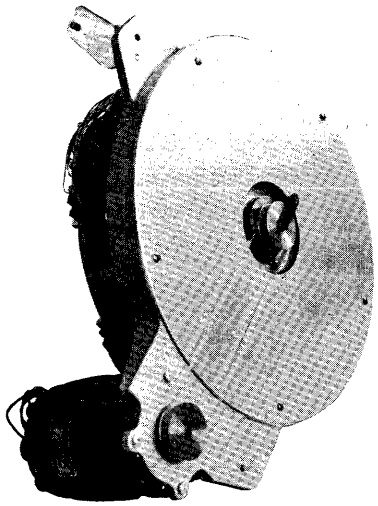


Figure 4-7 Disc-drive assembly in vertical position for servicing

4.2.2 Service

Spare cables and cable assemblies are available for replacement purposes.

In replacing or repairing any wiring in the unit, make sure that twisted pairs are replaced with twisted pairs, and that shielded connections are replaced with shielded connections.

4.3 MOTOR, DRIVE BELT & GROUNDING BRUSH

4.3.1 General Description

The disc is mounted on a precision spindle which is driven by a hysteresis-synchronous motor through a seamless mylar belt. A spring-loaded carbon brush provides a ground connection from the rotating assembly to the outer casting.

4.3.2 Servicing

To replace the motor, the drive-belt, or the grounding brush, the disc-drive assembly must be removed from the rack-mounting tray. This is accomplished as follows:

a. Disconnect power by detaching the ac plug from the unit, and remove the perforated outer cover.

b. Disconnect the two 20-pin connectors, S3 and S4, from the disc-drive assembly.

c. Detach the card-cage from the assembly by removing one of the sockethead screw hinge-pins, which hold it in place on its brackets.

d. Disconnect the two leads to the motor from terminal board TB-1.

e. Detach the disc-drive assembly from the rackmounting tray by removing the three 1/4-20 nuts which attach the base plate to the shockmounts (one is located at the front of the unit next to the motor, and the other two are at the rear with the card-cage mounting brackets). The snubbing washers will remain inside the shockmounts.

f. Carefully lift the assembly from the unit and remove it to a clean work area.

4.3.3 Grounding-Brush Replacement

a. Tip the assembly into a vertical position with the motor at the base as shown in Figure 4-7. The unit will be stable in this position.

b. Loosen the binding-head screw which attaches the ground-brush contact arm to the contact spacer. (See Figure 4-8)

c. Swing the arm clear to one side of the disc-spindle pulley and retighten the binding-head screw to secure it out of the way.

d. Gently pull the carbon grounding-brush contact from the center opening in the disc-spindle pulley screw, taking care not to lose the spring.

e. Insert the spring (Part #70045) in the pulley screw, replace the carbon grounding-brush with (Part #70044) and reverse the above procedures to reposition the contact arm and tighten the binding-head screw.

4.3.4 Belt Replacement

a. Swing the grounding brush contact arm clear by repeating 4.3.3 a, b, c, and d.
b. Take off the lower flange on the disc-spindle pulley by removing the spindle-pulley screw which houses the grounding-brush and spring. (Figure 4-8) The belt may now be removed. Clean the pulley with organic solvent such as Methyl Ethyl Ketone (MEK) or detergent and water.
c. Position the replacement belt (Part # 71014-4) over the motor pulley, then turn the motor pulley by hand as the belt is guided onto the disc-spindle pulley.
d. Reinstall the disc-spindle pulley flange. Turn the motor pulley by hand and observe belt-tracking. It should track in the center of the face of each pulley. If it does not track properly, loosen the motor pulley setscrew and adjust the motor pulley up or down until proper tracking is obtained.
e. Replace the grounding-brush and spring, and reposition the contact arm and tighten the binder-head screw.

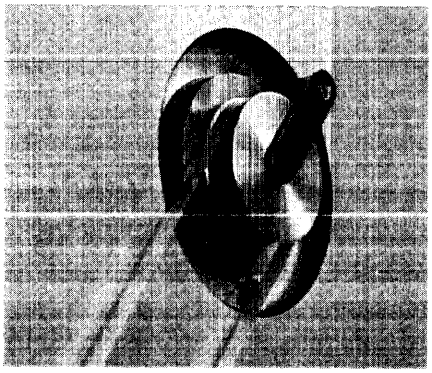


Figure 4-8 Disc-spindle pulley with grounding brush

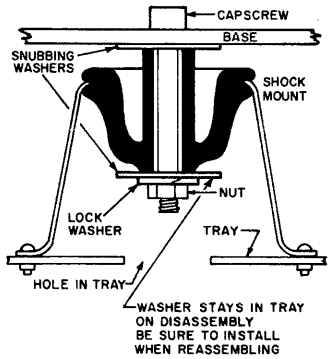


Figure 4-9 Shockmount construction details

4.3.5 Motor Replacement

a. Remove the motor pulley by loosening the single 6-32 socket-head setscrew which fastens it to the shaft. This also frees the belt for removal.
b. Take out the motor by removing the four screws which attach it to the base-plate casting.
c. Install the replacement motor (Part #2024) by locating in the counter bore of the base-plate casting, and replacing the mounting screws.
d. Reinstall the belt as described in Belt Replacement.

4.3.6 Reinstallation of Disc-Drive Assembly

a. Attach the assembly to the three shock mounts with 1/4-20 nuts. Be sure to install the snubbing-washers in the shockmounts.
b. Connect the two motor leads to terminal board TB-1.
c. Install the card cage onto its brackets and insert the socket-head screw hinge-pin.
d. Connect the two 20-pin connectors, S3 and S4.
e. Attach the perforated outer cover.
f. Reconnect the ac power plug at the back of the unit.

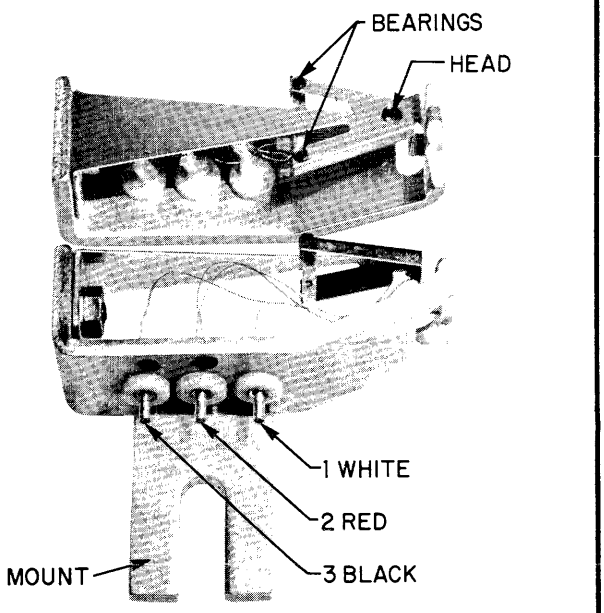


Figure 4-11 Data Disc Magnetic Head

4.4 MAGNETIC HEADS

4.4.1 General

Magnetic heads used in the Data Disc F Series Memory Systems have been specially developed for high-density contact recording and reproducing. Each head is in constant contact with the disc surface, in a contact plane determined by the head's transducer element and two bearing points carried on the gimballed transducer-support platform. Lightly loaded three-point contact is thus provided for stability, good surface compliance, and long service life. Uniquely designed mountings and adjustments provide simple alignment of the heads on the disc. The same heads are used for clocks and data, but clock heads are selected for better resolution. Replacement heads totaling 10% of original components are included with each unit.

4.4.2 Functional

The head has a center-tapped bifilar winding. Both sides of the winding (1-3) are used for reading, alternate sides (1-2 and 3-2) are used for writing, with one side causing magnetic saturation of the disc in one direction and the other side causing saturation in the opposite direction. Color-coded dots on the head frame assembly identify the connections. Connection 1 is white, 2 is red, and 3 is black. 1-3 are the total head winding and 2 is the center tap. (See Figure 4-11).

Heads are electrically identical, within allowable tolerance. Nominal resistance of the head winding is 18 ohms, or 9 ohms per side. Inductance is 12 microhenries. Heads of identical construction are used for all data tracks. Heads with superior resolution are used for double-frequency clock tracks. The unshielded construction of F Series heads requires the use of a differential read amplifier which provides at least 60 db common-mode noise rejection.

WARNING

Do NOT check head resistance with a standard ohmmeter. Current flowing through the head can change the state of the disc's magnetic coating. The track may be erased if the disc is rotating, or, if the disc is stationary, a single transition may be erased or written. When measuring heads on tracks which contain valuable data, use an ohmmeter which will cause less than one milliampere to flow through the windings.

4.4.3 Servicing

Head servicing described in this manual is limited to electrical replacement of the head by one of the spare heads provided with each unit. It is not permissable to mechanically position a spare head over the track which has a failed head, nor is it permissable to mechanically replace the failed head with one of the spare heads. Data which was written by the failed head is generally NOT recoverable.

4.4.4 Testing the Head

Compare the suspected head with other heads that are known to be good. The transducer and the two bearing points should be making contact with the disc surface. The mounting bracket should be about 0.014 inch from the disc surface across the tail of the arrow and at the point.

4.4.5 Electrical

Excessive noise from one individual head is sometimes caused by a high-resistance short circuit from the windings to ground. Disconnect the head from the assembly by removing the diode card into which it is connected. Refer to Interconnection Drawing 10651. Check the resistance between the head-winding terminations on the diode-card connector and ground. Impedance should be greater than 10 megohms when measured at 30 volts dc.

4.4.6 Use of Spare Heads

Spare heads may be used for electrical replacement of a failed head. F3 unit spare heads are connected to the Y7 select line so that all spare heads may be selected by external control lines for testing. (F3's with serials 109 and lower have spare heads connected to the Y8 select line terminating at pin B of P3).

Before using a spare head, test its quality by writing and reading data with the head. Use the Y7 selection line and the appropriate X-selection line (first choice is the line with the same number as the failed head). If head X1Y4 has failed, check spare X1Y7 first as it has the correct X-selection line connected: only the Y-select line will have to be changed. If X1Y7 is not satisfactory (or not present), use X0Y7, X2Y7, or X3Y7 as these are also on the bottom plate (casting). Spares on the upper plate assembly cannot be wired into the X1 diode board on the bottom plate.

The X-selection number locates the diode card to which the heads are connected. Figures 3-4 and 3-5 provide connector and diode-card locations on the top and bottom plates. The full complement of Y-address lines (0-7) is available on each diode board for terminating the red center-tap lead of the head.

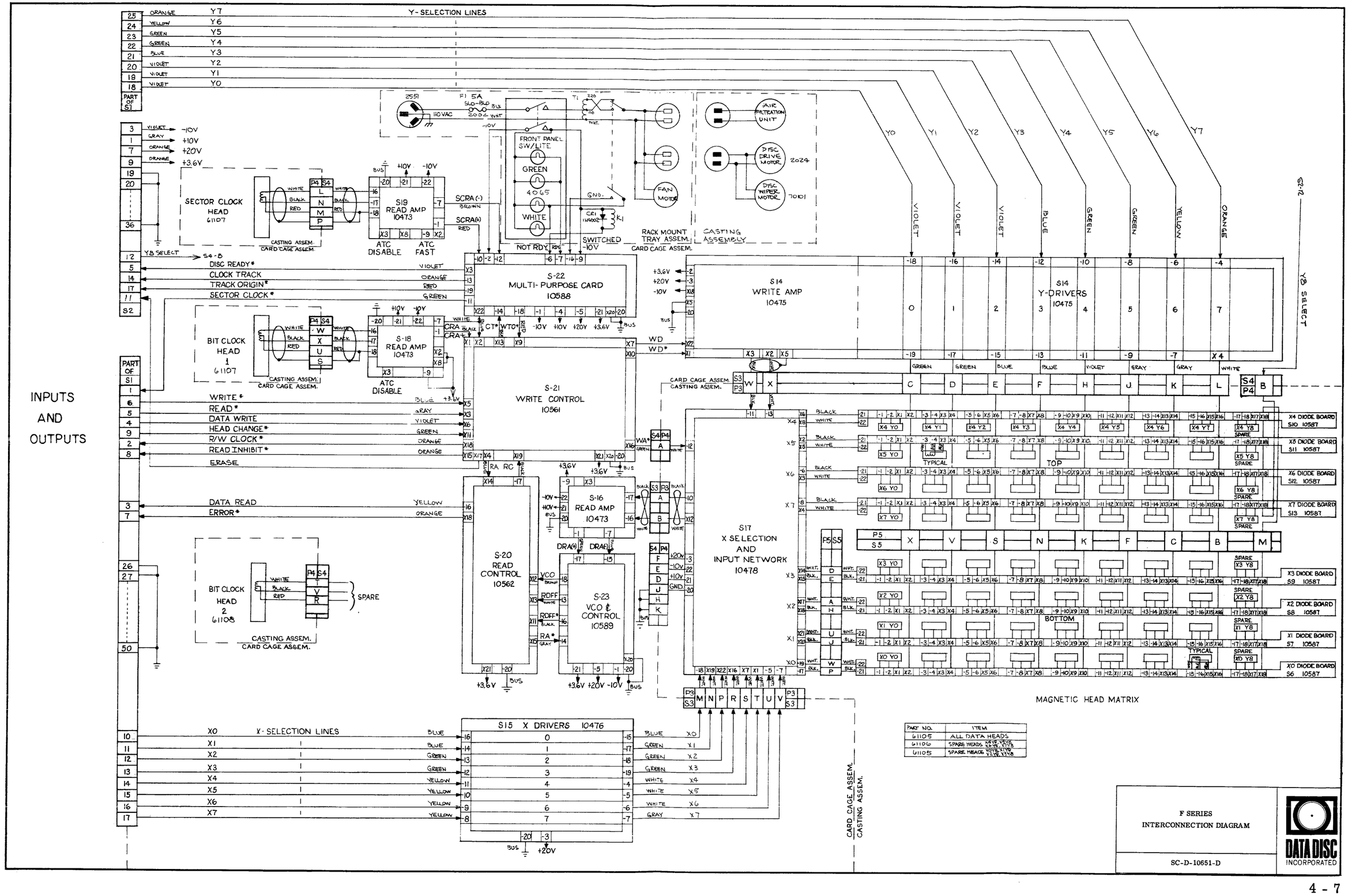
Interconnection Drawing 10651 shows head connections to the diode boards for a full head complement. F3 units use Y-selection lines Y0, Y1, Y4, and Y5. The spares line is Y7.

4.4.7 Connecting Spare Head With Same X Selection Number as Failed Head

a. Locate red center-tap lead of failed head by pin number and remove the inserted connector with AMP pin-removal tool 465195.
b. Locate red center-tap lead of spare head by pin number and remove its connector with the AMP tool.
c. Insert pins removed in steps a and b so that each pin is inserted in the other's previous location.

4.4.8 Connecting Spare Head With Different X-Selection Number Than Failed Head
Refer to Figure 4-12

a. Select spare head physically closest to the failed head. Remove wires and connector pin from X16 with AMP pin removal tool 465195 and insert in blank position -19.
b. Remove white-wire connector pin from -15 and insert in X19.
c. Remove black-wire connector pin from -16 and insert in X21.
d. Use three-wire jumper cable (spare parts No. 10685) to connect spare-head diode card connector (A) to failed-head diode card connector (B).
At (A): Insert red-wire connector pin at X16; insert white-wire connector pin at X20; and insert black-wire connector pin at X22.
e. Run other end of jumper cable to (B).
At (B): Remove failed-head red-wire connector pin and replace with jumper cable red-wire connector pin; remove failed-head white-wire connector pin and replace with jumper cable white-wire connector pin; and, remove failed head black-wire connector pin and replace with jumper cable black-wire connector pin.
f. Leave failed head in place. Lace jumper cable and the three wires from the failed head to the wiring harness.



PART NO.	ITEM
61105	ALL DATA HEADS
61106	SPARE HEADS X4Y8, X5Y8, X6Y8, X7Y8
61105	SPARE HEADS X0Y8, X1Y8, X2Y8, X3Y8

F SERIES
INTERCONNECTION DIAGRAM

SC-D-10651-D

DATA DISC INCORPORATED

This page purposely left blank.

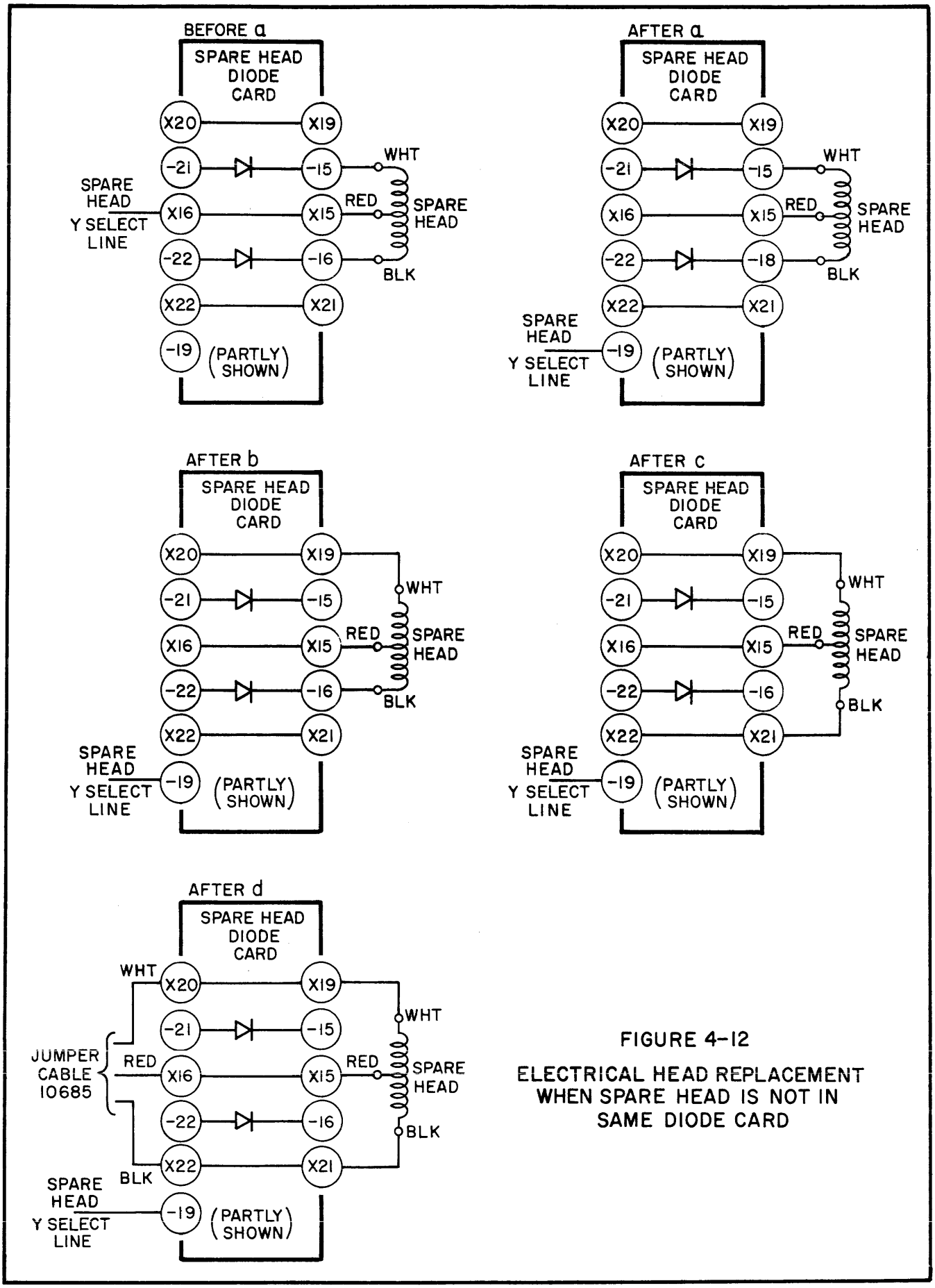


FIGURE 4-12

ELECTRICAL HEAD REPLACEMENT WHEN SPARE HEAD IS NOT IN SAME DIODE CARD

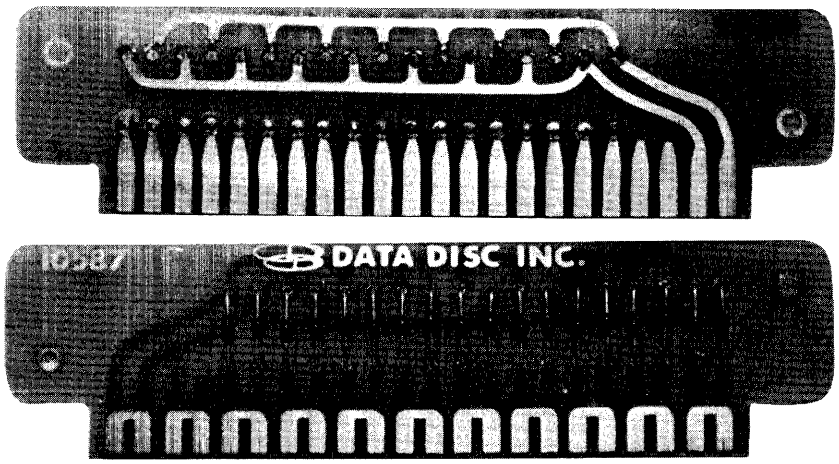


Figure 4-13 Diode Card

4.5 DIODE CARDS (10587)

4.5.1 General Description

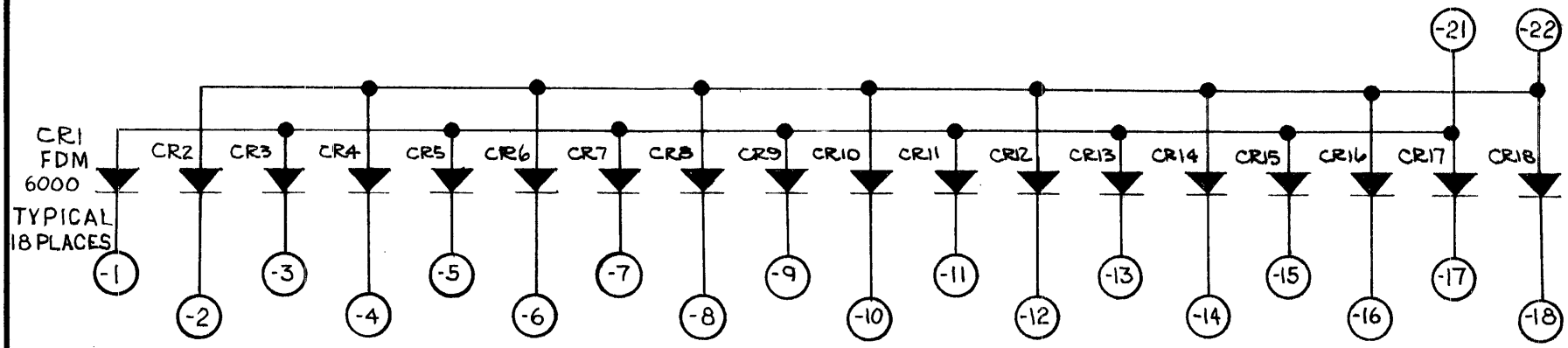
The Diode Cards contain the diodes which comprise part of the head-selection matrix. There are up to eight electrically identical Diode Cards in each unit. Four can be mounted in connectors on the metal plate above the disc, and four can be mounted in connectors on the casting below it (see Drawings 10496 and 10497). The plug-in printed circuit cards are held in their mountings by their own connectors.

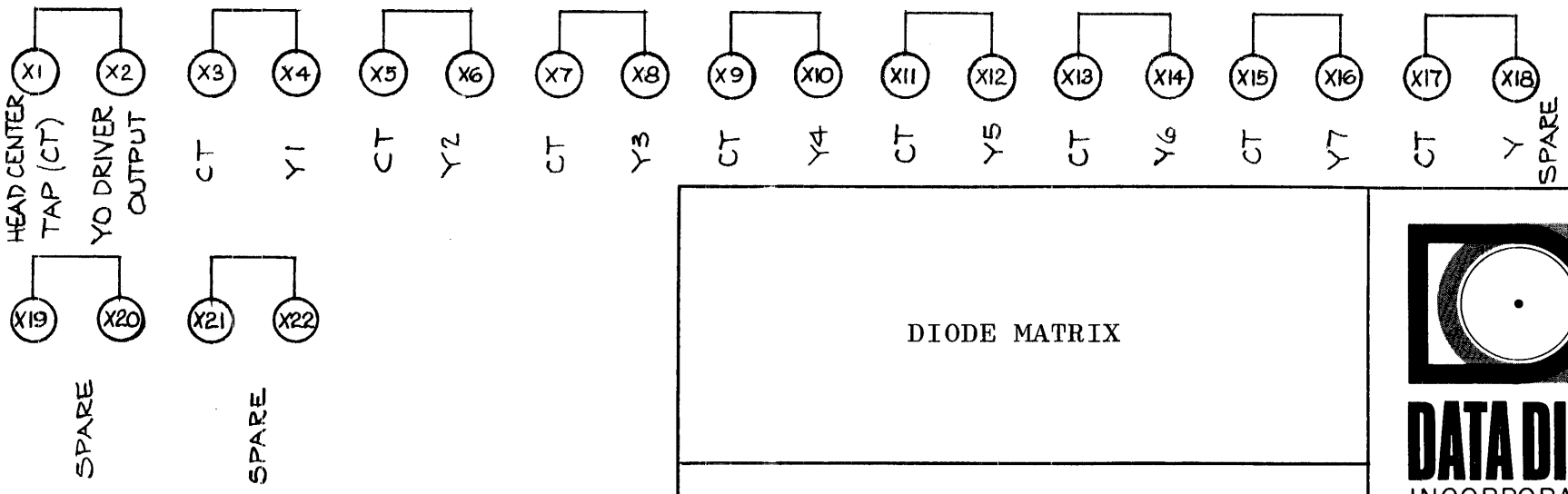
There are 18 diodes on each card, two for each of the heads connected to it, plus two for the spare head. All Diode Cards are electrically connected to the X-Selection and Input Network card, and to the head windings as shown in Drawings 10416 and 10651.

4.5.2 Functional Description

The Diode Cards constitute the X co-ordinates of the electrical head-selection matrix. The Diode Cards are designated X-0 through X-7, and the Y-selectors are designate Y-0 through Y-7. A typical F3 unit with 32 heads uses only a 4 x 8 matrix of the 8 x 8 matrix capability afforded by the eight cards. Thus, by defining the X and Y co-ordinates, any one of the 32 heads may be selected for reading or writing data on the disc. Table 3-2 identifies the X and Y selection lines used to select heads on F3 units.

Schematic Diagram 10416 shows in detail the selection of head 00 (X-0, Y-0). Y-0 transistor Q1 and X-0 transistors Q1 and Q2 are turned ON. The two X-0 transistors allow current to flow through Diode Card X-0, and the Y-0 transistor provides a ground return connection for head current. The other diodes on card X-0 are back-biased by a +20 volt potential on their cathodes and a low anode potential because the 00 set of diodes is conducting. Thus, an electrical path is established for current to flow only through head 00.

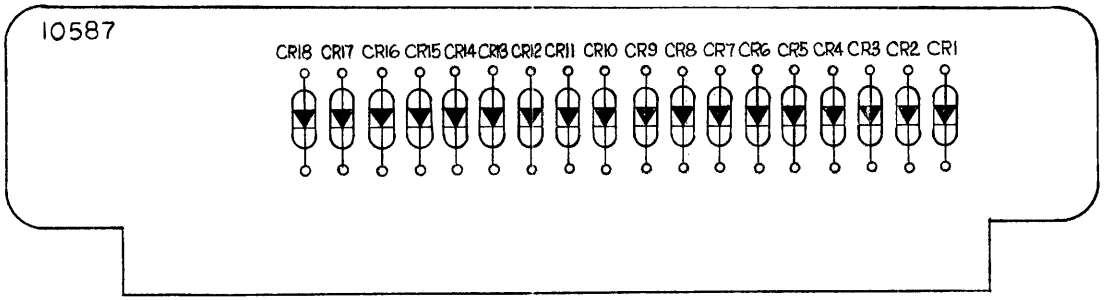




DIODE MATRIX

SC-A-10587-C

DATA DISC
INCORPORATED



QUAN.	DESCRIPTION & MANUFACTURER	
1	SCHEMATIC DWG. DATA DISC#	10587 B
1	P.C. BOARD # 10587	DATA DISC
10	FDM 6000 DIODES	FAIRCHILD

DIODE MATRIX

AD-B-10587-C

DATA DISC INCORPORATED

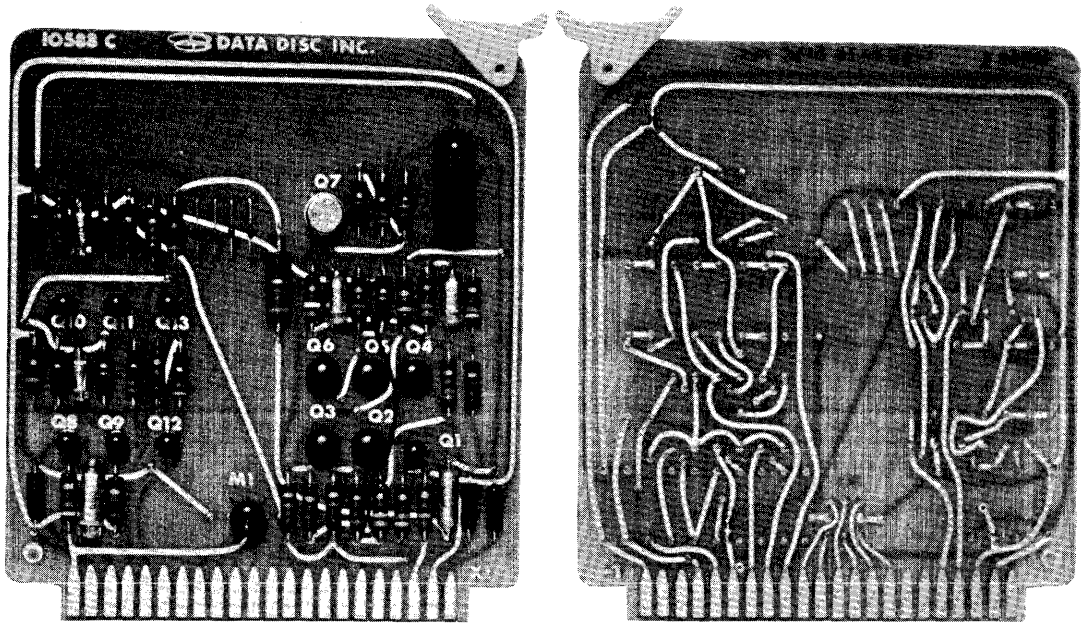


Figure 4-14 Multipurpose Card

4.6 MULTIPURPOSE CARD (10588)

4.6.1 General Description

The Multipurpose Card, located at S22, in the card-cage contains three discrete-component circuits and two micrologic NOR gates.

A Disc-Ready circuit supplies a Disc Ready* signal to the INTERFACE, lights the white portion of the power switch during disc acceleration and lights the green portion of the power switch when the disc is at operating speed. This circuit has a 20-second time delay, which is sufficient time for the disc to reach operating speed after the power has been turned ON.

The Write Turn-On (WTO) circuit protects against false writing. It uses the time delay built into the Disc-Ready circuit to allow time for the disc to attain its normal speed before permitting writing.

A Gap Detector circuit generates a Track Origin* signal from the gap in the clock track signal. The pulse is approximately two-microseconds long, and is generated once per disc revolution and sent to the INTERFACE to mark the beginning of each data track. See Figure 4-15.

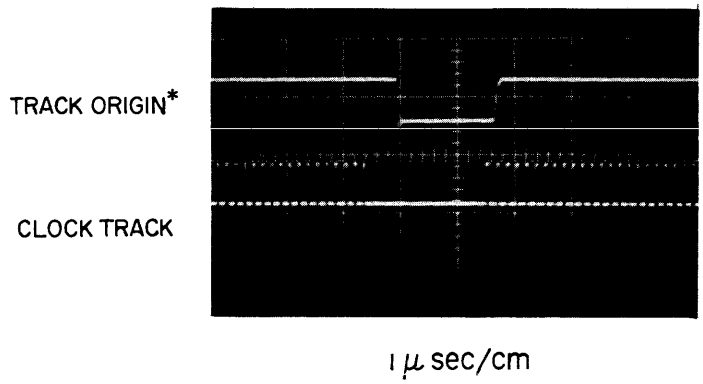


Figure 4-15 Relationship of Track Origin* to Clock Track

4.6.2 Functional Description

4.6.2.1 Disc-Ready. On Drawing 10588, pin -9 receives minus 10 volts from the front-panel switch, turning the circuit ON. The capacitor, C7, then begins charging through resistor, R16. Q5 and Q6 and their associated components comprise a Schmitt Trigger circuit (S/T). When the voltage on the base of Q6 attains the level required to trigger the S/T, Q6 turns ON and Q5 turns OFF. Q4 inverts the signal from Q5. Q1 provides the Disc Ready* signal for the INTERFACE at Pin X3, and the ground supplied by Q2 through pin -6 lights the white lamps on the power switch. Q3 inverts the signal from Q2 (Q3 turns ON as Q2 turns OFF). The ground supplied by Q3 through pin -7 turns the power switch "green" lights ON as the white lights are turned OFF.

When power is turned OFF, Q7 dumps voltage from C7 through R17, and the circuit is reset. Another Disc Ready signal cannot be obtained until 20 seconds have elapsed, even though power may be turned ON immediately after it has been turned OFF, and even though the disc has not been allowed to slow perceptibly.

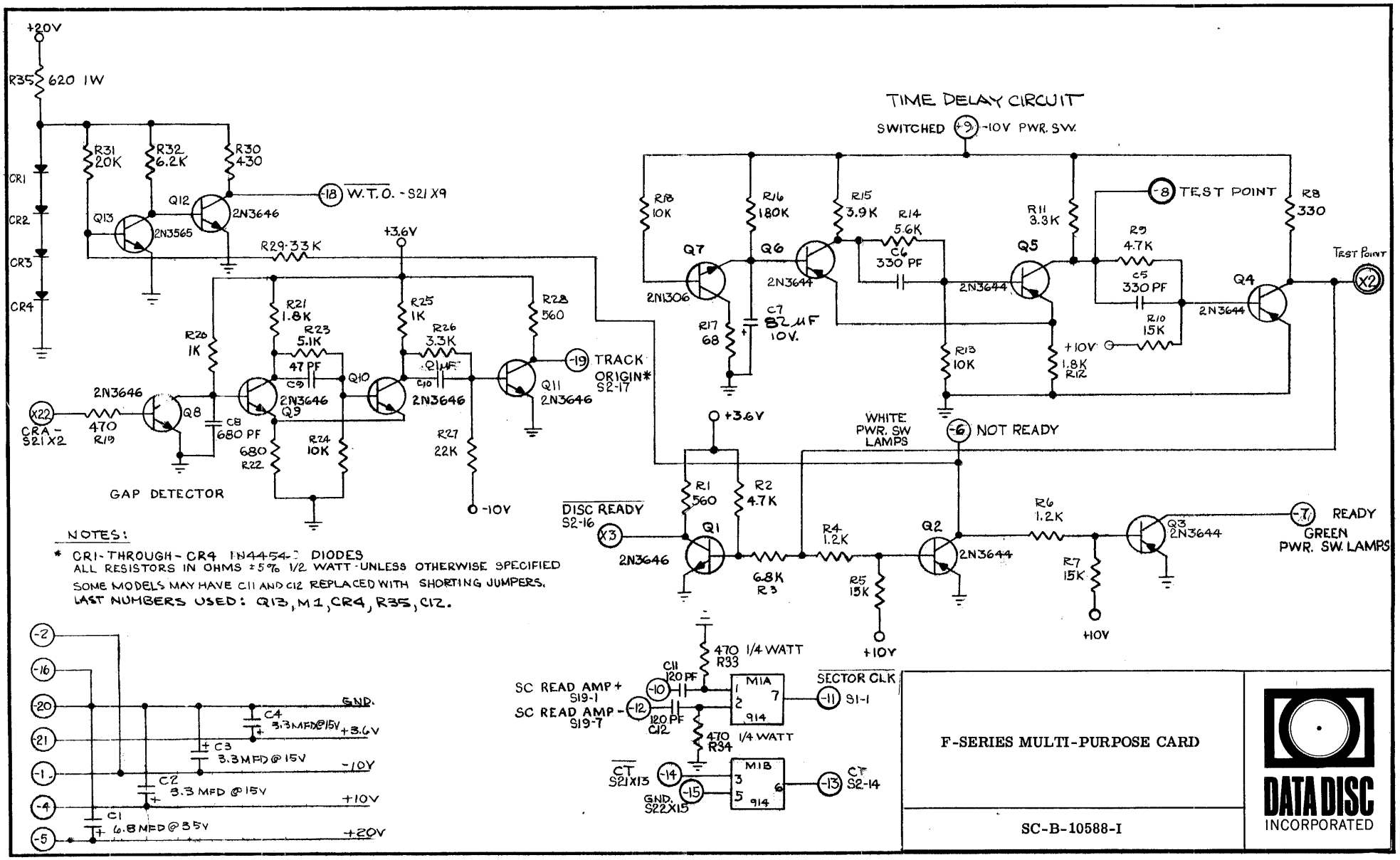
4.6.2.2 Write Turn-On. This circuit protects against false writing by keeping WTO* (pin -18) positive until the Disc Ready time-delay circuit allows the test point, pin -8, to go negative. Q13 will turn OFF, turning Q12 ON, and WTO* goes to ground to permit writing.

The WTO circuit is powered by voltage developed across CR1 to CR4 from the +20 volt supply to insure that data protection is maintained whenever the +20 volt supply is ON. See Section 3.1.3 on Data Protection.

4.6.2.3 Gap Detector. One of the clock track read-amplifier outputs (CRA-) is applied to pin X22 of the Multipurpose Card. Transistor Q8 inverts the signal, and capacitor C8 is kept discharged by the clock pulses. This capacitor charges when a gap occurs, turning ON Q9 and turning Q10 of the S/T OFF. Q11 therefore turns ON during the gap time (as shown in Figure 4-15) to provide the Track Origin* pulse at pin -19.

4.6.2.4 Sector Clock. Sector-Clock* output at pin -11 is a NOR of the Sector-Clock read-amplifier positive pulse outputs which appear as inputs on pins -10 and -12.

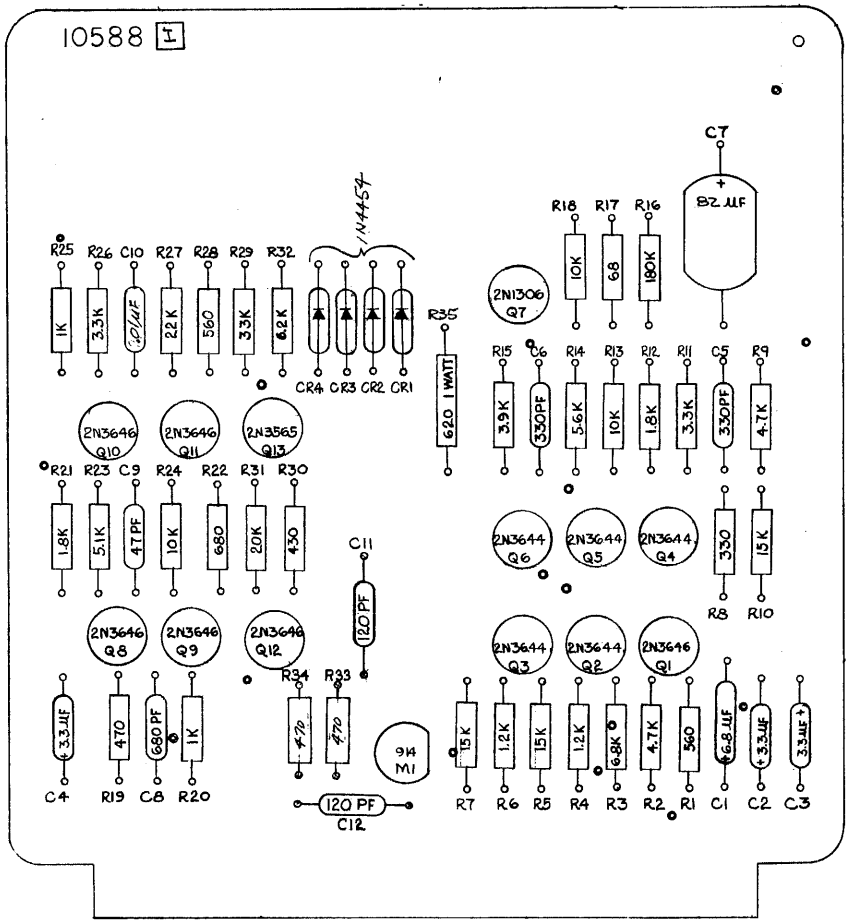
4.6.2.5 Clock Track Inverter. Clock Track (CT) output on pin -13 is an inversion of the CT* input on pin -14.



F-SERIES MULTI-PURPOSE CARD

SC-B-10588-I

DATA DISC INCORPORATED



ITEM	COMP. DESIG.	QUAN.	DESCRIPTION AND MANUFACTURER	
43	Sc-C-10588 I	1	SCHEMATIC	
42	8013-I	1	REVISION TAG	BRADY
41				
40	C11 & C12	2	120 PF CAPACITOR	CENTRA LAB
39	EJECTOR	1	CARD EJECTOR #9202	SCANBE
38	R11-R26	1	33 K 1/2 WATT 5% RESISTOR	G H
37	M1	1	914 µ LOGIC CAN	FAIRCHILD
36	10588 F	1	PRINTED CIRCUIT BOARD	
35	Q7	1	TRANSISTOR SPACERS	
34	Q7	1	2N1306 TRANSISTOR	TEXAS INST.
33	Q13	1	2N3565 TRANSISTOR	FAIRCHILD
32	Q2-THROUGH-Q6	5	2N3644 TRANSISTORS	FAIRCHILD
31	Q1-Q8-Q9-Q10-Q11-Q12	6	2N3646 TRANSISTORS	FAIRCHILD
30	CR1-THROUGH-CR4	4	1N4454 DIODES	G.E.
29	C2-C3	3	3.3 µF @ 15V CAPACITOR	KEMET
28	C1	1	6.8 µF @ 35V CAPACITOR	SPRAGUE
27	C7	1	82 µF CAPACITOR 10V	KEMET
26	C9	1	47 PF CAPACITOR	CENTRA LAB
25	C10	1	.001 MF CAPACITOR	CENTRA LAB
24	C5-C6	2	330 PF CAPACITOR	CENTRA LAB
23	C8	1	680 PF CAPACITOR	CENTRA LAB
22	R35	1	620 1 WATT 5% RESISTOR	G H
21	R17	1	68 1/2 WATT 5% RESISTOR	G H
20	R8	1	330 1/2 WATT 5% RESISTOR	G H
19	R30	1	430 1/2 WATT 5% RESISTOR	G H
18	R19, R33, R34	3	470 1/2 WATT 5% RESISTOR	G H
17	R1-R28	2	560 1/2 WATT 5% RESISTOR	G H
16	R22	1	680 1/2 WATT 5% RESISTOR	G H
15	R20-R25	2	1K 1/2 WATT 5% RESISTOR	G H
14	R12-R21	2	1.8K 1/2 WATT 5% RESISTOR	G H
13	R11-R26	2	3.3K 1/2 WATT 5% RESISTOR	G H
12	R15	1	3.9K 1/2 WATT 5% RESISTOR	G H
11	R2-R9	2	4.7K 1/2 WATT 5% RESISTOR	G H
10	R23	1	5.1K 1/2 WATT 5% RESISTOR	G H
9	R14	1	56K 1/2 WATT 5% RESISTOR	G H
8	R32	1	6.2K 1/2 WATT 5% RESISTOR	G H
7	R3	1	6.8K 1/2 WATT 5% RESISTOR	G H
6	R13-R18-R24	3	10K 1/2 WATT 5% RESISTOR	G H
5	R5-R7-R10	3	15K 1/2 WATT 5% RESISTOR	G H
4	R31	1	20K 1/2 WATT 5% RESISTOR	G H
3	R27	1	22K 1/2 WATT 5% RESISTOR	G H
2	R4-R6	2	12K 1/2 WATT 5% RESISTOR	G H
1	R16	1	180K 1/2 WATT 5% RESISTOR	G H

F-SERIES MULTI-PURPOSE CARD

AD-C-10588-G

DATA DISC INCORPORATED

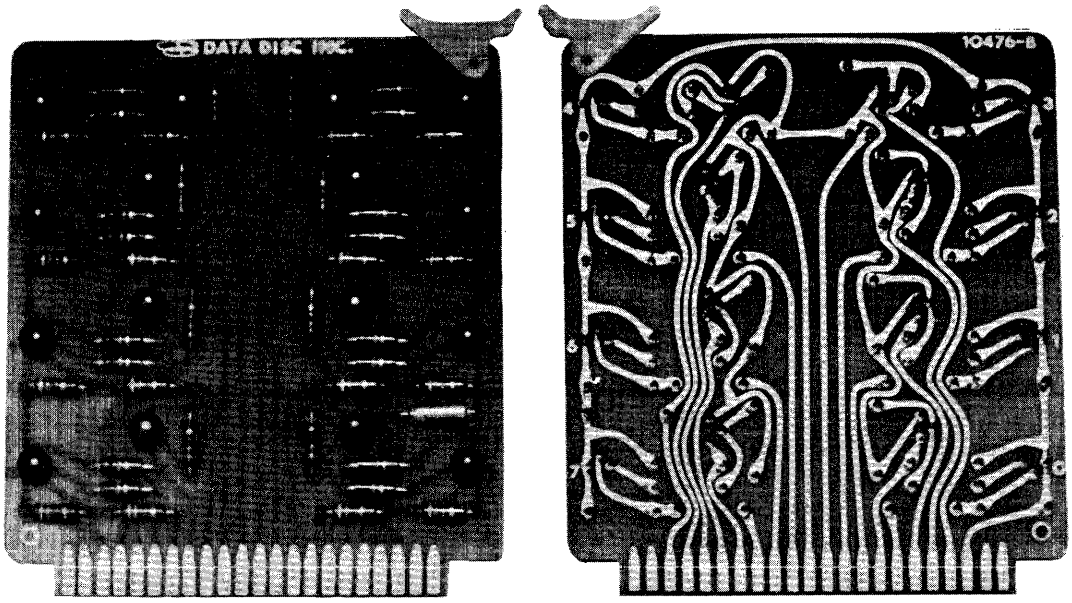


Figure 4-16 X Drivers Card

4.7 X DRIVERS (10476)

4.7.1 General Description

The X Drivers furnish drive power to the X Selection Switches on the X Selection and Input Network. The X Selection Switches, in conjunction with the Y Drivers, connect the desired magnetic head to either the read or the write amplifiers. There are eight identical X Drivers, X-0 to X-7, on the card. The X-Driver Card is mounted in the electronics card cage at connector S15, and is connected to the INTERFACE through connector S2.

4.7.2 Functional Description

In X-0 selection, the application of a voltage greater than 1.7 volts to pin -16 of the X-0 driver from the INTERFACE turns on X-0 driver transistors Q1 and Q2, which enables turn ON of transistor Q1 or Q2 on the X-0 X-Select switch. This applies 20 volts to the diode matrix for the X-0 heads. The head which has a ground at its center tap provides a conduction path for the diodes to select that head. The center tap is grounded by a Y Driver.

4.8 X-SELECTION & INPUT NETWORK (10478)

4.8.1 General Description

The X-Selection and Input Network operates in conjunction with the X Drivers, the Y Drivers and the diode matrix to connect the desired magnetic head to either the read or the write amplifier. There are eight identical X selection switches on the card, numbered 0 through 7. The Input Network is used to provide improved read-amplifier input, and to block dc offset voltages caused by semiconductor junction drops between the head and the read-amplifier input.

The X-Selection and Input Network Card is mounted inside the disc-drive assembly on the upper head-support plate in connector S17, and is made accessible by removing the top dust cover of the disc-drive assembly.

WARNING

Do not operate the F-Unit with dust cover removed.

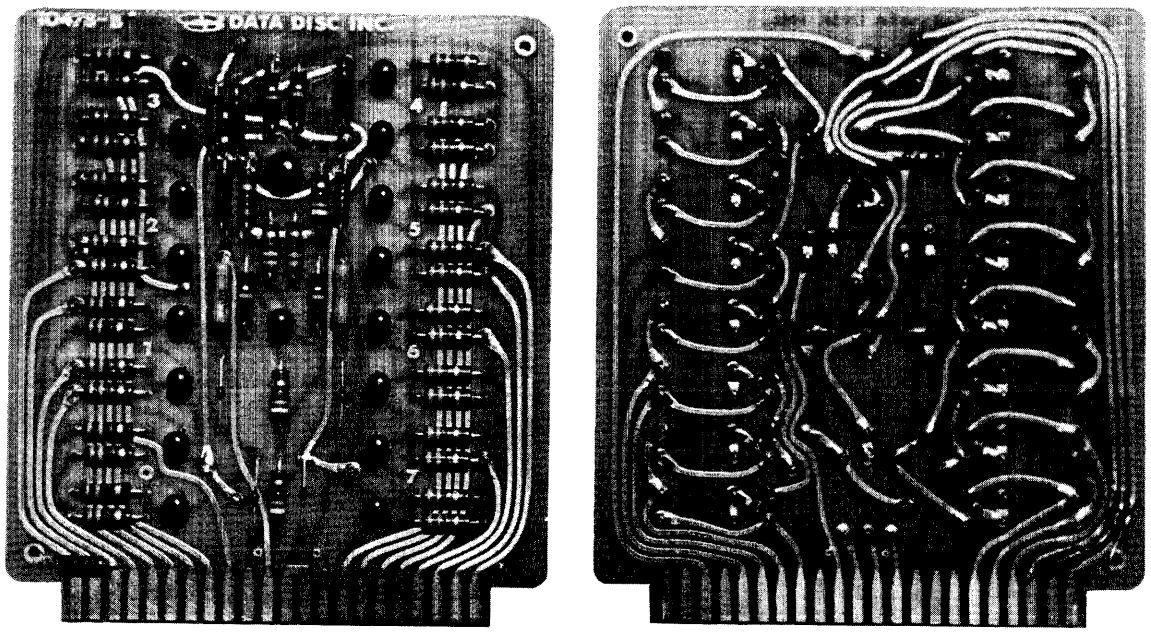


Figure 4-17 X Selection and Input Network Card

4.8.2 Functional Description, X-Selection Switch

An X-Selection Switch is turned ON when its respective X-Driver is turned ON. For example, in X-0 selection, +20 volts is applied to pin -18 of the X-Selection Switch 0 from the X Driver Card output of the X-0 Driver.

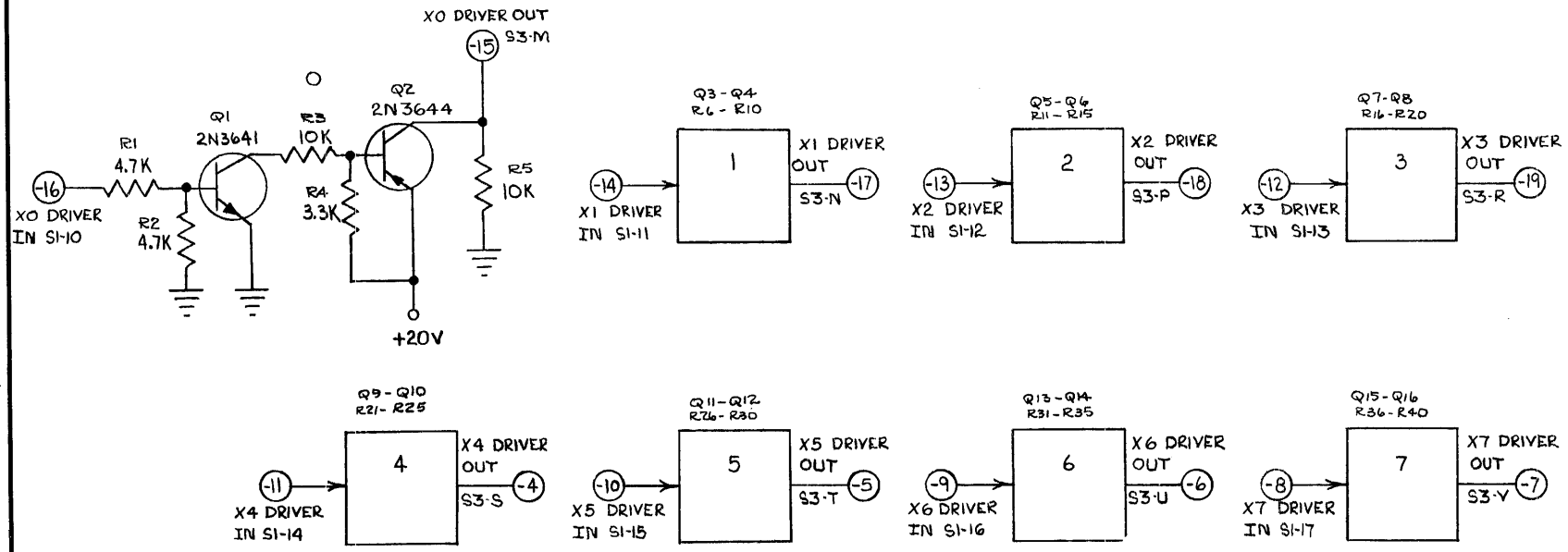
Q1 or Q2 is thereby enabled to turn ON to connect one of the X-0 heads, i.e., 00, 01, 02, 03, 04, 05, 06, or 07, as determined by Y-Driver Selection to the Input Network. The Input Network switches the head to connect with either the read or the write amplifier as determined by the signal at pin -12.

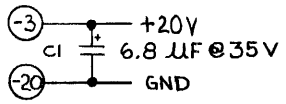
4.8.3 Writing

The WA* signal, a ground on pin -12, turns transistors Q17 and Q18 OFF, causing the collector of Q18 to assume a negative potential. This action back-biases diodes CR3 and CR4, preventing the saturation-level write-amplifier signals flowing through CR1 and CR2 from entering the read-amplifier. Write signals from the write-amplifiers are applied alternately through pins -11 and -13, through diodes CR1 and CR2, and through the selected X selection switches to the selected head windings.

4.8.4 Reading

In reading, the potential of pin -12 (WA*) is raised toward 3.6 volts, turning transistors Q33 and Q34 ON. Diodes CR3 and CR4 are forward-biased by the +10 volt potential at the junction of R37, 38, 39, 40 and the collector of Q18. Read-current pulses from the selected head flow through the established path to the read-amplifier input at pins -10 and X12. Blocking-capacitors C4 and C5 prevent any differential D-C voltages originating from diode drops in the switching matrix from reaching the read-amplifiers.



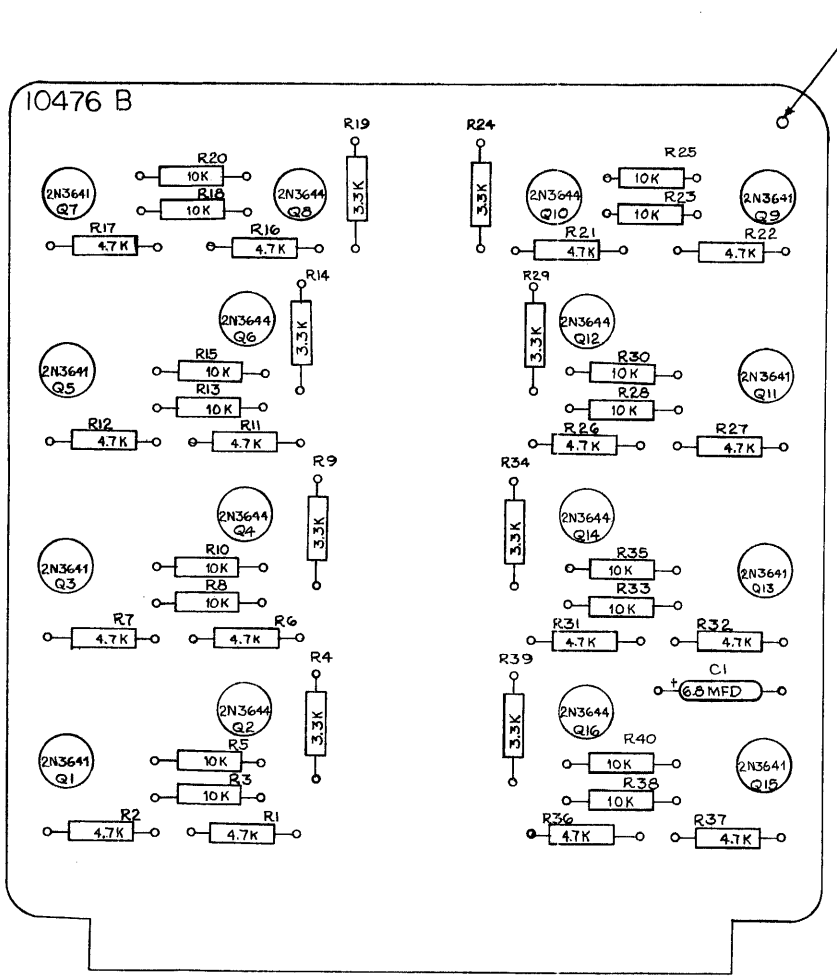


UNLESS OTHERWISE SPECIFIED; ALL RESISTORS IN OHMS ± 5%, ½ WATT.

X DRIVERS

SC-B-10476-G

DATA DISC INCORPORATED

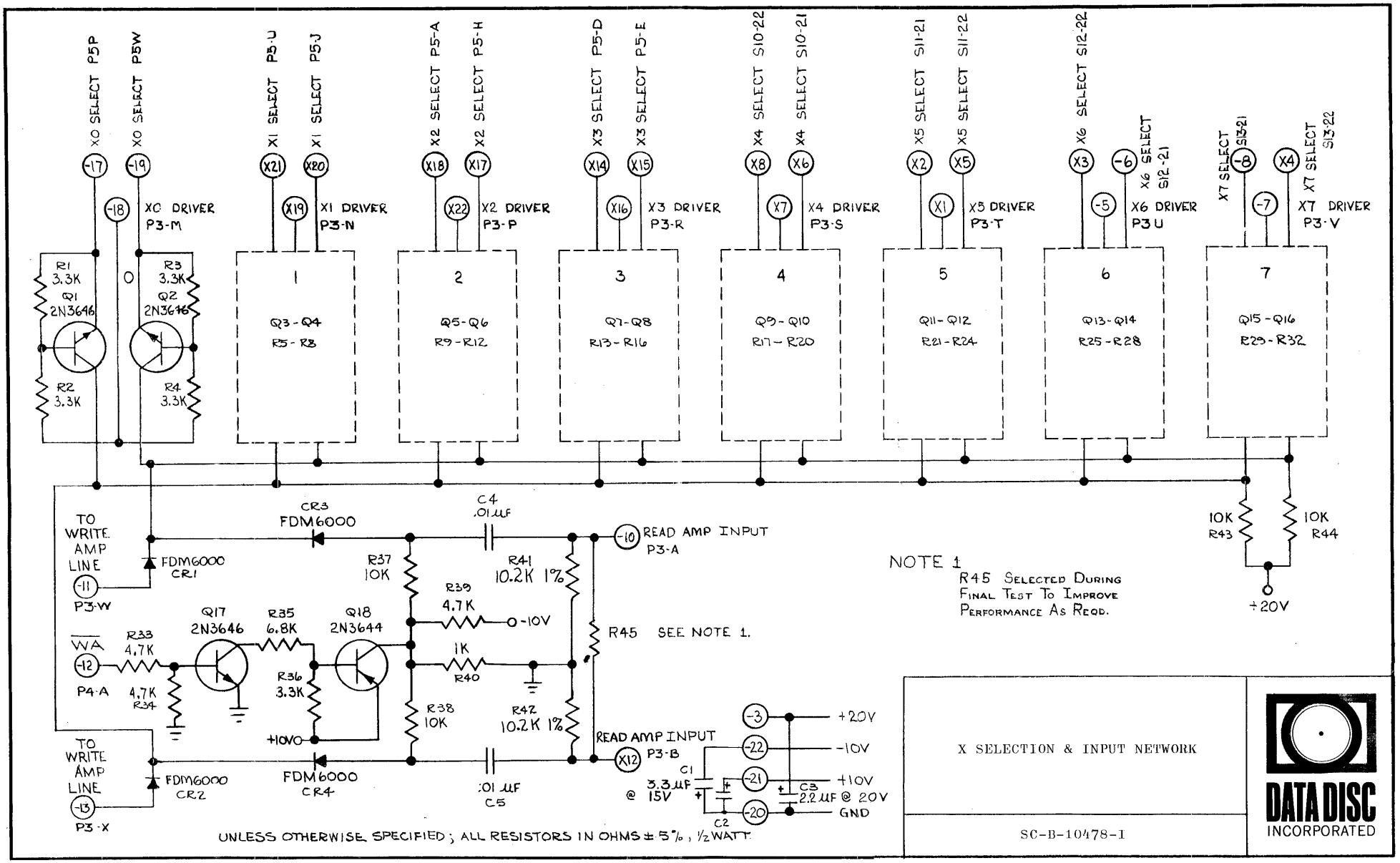


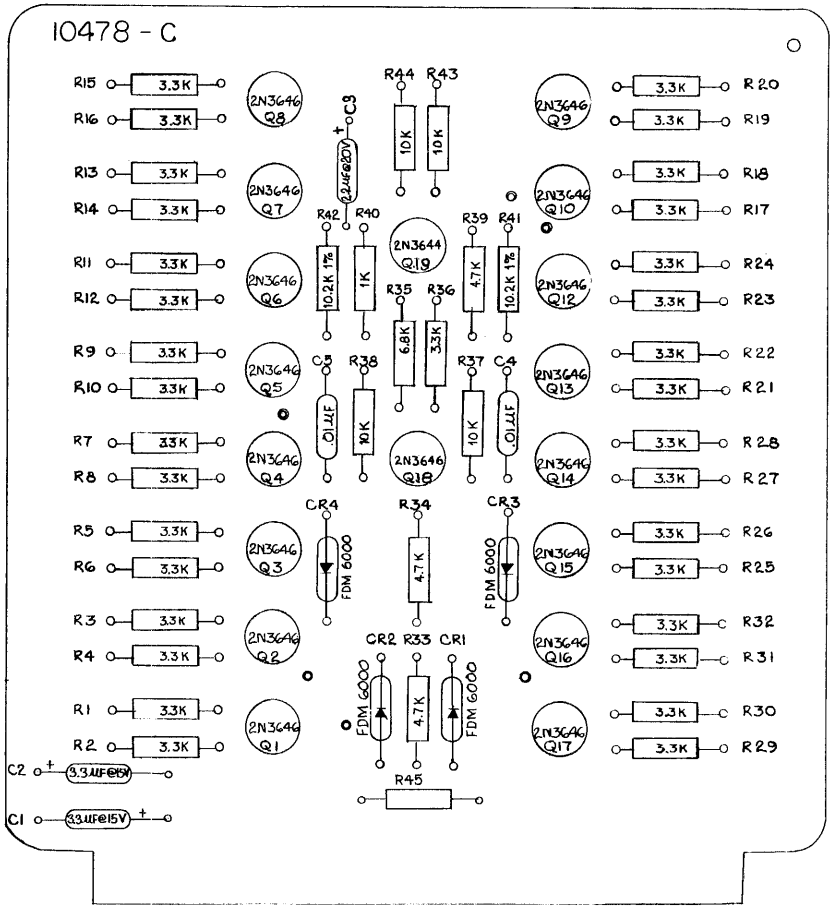
ITEM	COMP. DESIGNATION	QUAN.	DESCRIPTION	
9	SC-10476 G	1	SCHEMATIC DWG. DATA DISC #	10476 G
8	EJECTOR	1	CARD EJECTOR S202	SCANBE
7	C1	1	6.8 MFD @ 35 V CAPACITOR	SPRAGUE
6	10476-B	1	P.C. BOARD #10476-B	DATA DISC
5	Q2-Q4-Q6-Q8-Q10-Q12-Q14-Q16	8	2N3644 TRANSISTOR	FAIRCHILD
4	Q1-Q3-Q5-Q7-Q9-Q11-Q13-Q15	8	2N3641 TRANSISTOR	FAIRCHILD
3	R4-R9-R24-R14-R19-R29-R34-R39	8	3.3K 1/2 WATT 5%	GH
2	R1-R2-R6-R7-R11-R12-R16-R17 R20-R18-R24-R21-R19-R22-R25 R23-R26-R10-R13-R15-R18-R28 R23-R25-R28-R30-R33-R35-R38-R40	16	4.7K 1/2 WATT 5%	GH
1		16	10K 1/2 WATT 5%	GH

X DRIVERS

AD-C-10476-E

DATA DISC INCORPORATED


X0 SELECT P5P
X0 SELECT P5W
X1 SELECT P5-U
X1 SELECT P5J
X2 SELECT P5-A
X2 SELECT P5-H
X3 SELECT P5-D
X3 SELECT P5-E
X4 SELECT S10-22
X4 SELECT S10-21
X5 SELECT S11-21
X5 SELECT S11-22
X6 SELECT S12-22
X6 SELECT S12-21
X7 SELECT S13-21
X7 SELECT S13-22
X0 DRIVER P3-M
X1 DRIVER P3-N
X2 DRIVER P3-P
X3 DRIVER P3-R
X4 DRIVER P3-S
X5 DRIVER P3-T
X6 DRIVER P3 U
X7 DRIVER P3-V
R1 3.3K
Q1 2N3646
R2 3.3K
R3 3.3K
Q2 2N3646
R4 3.3K
1
Q3 - Q4
R5 - R8
2
Q5 - Q6
R9 - R12
3
Q7 - Q8
R13 - R16
4
Q9 - Q10
R17 - R20
5
Q11 - Q12
R21 - R24
6
Q13 - Q14
R25 - R28
7
Q15 - Q16
R29 - R32
10K R43
10K R44
+20V
TO WRITE AMP LINE
P3-W
FDM6000 CR1
CR3 FDM6000
C4 .01 µF
READ AMP INPUT P3-A
R37 10K
R41 10.2K 1%
R39 4.7K
0 -10V
R45 SEE NOTE 1.
Q17 2N3646
R35 6.8K
Q18 2N3644
R33 4.7K
WA
P4-A
4.7K R34
R36 3.3K
1K R40
R38 10K
R42 10.2K 1%
+10V
TO WRITE AMP LINE
P3-X
FDM6000 CR2
FDM6000 CR4
.01 µF C5
READ AMP INPUT P3-B
C1 3.3 µF @ 15V
C2
C3 2.2 µF @ 20V
+20V
-10V
+10V
GND
NOTE 1
R45 SELECTED DURING FINAL TEST TO IMPROVE PERFORMANCE AS REQD.
UNLESS OTHERWISE SPECIFIED; ALL RESISTORS IN OHMS ± 5%, ½ WATT
X SELECTION & INPUT NETWORK
SC-B-10478-I
DATA DISC INCORPORATED



ITEM	COMP. DESIG.	QUAN.	DESCRIPTION	
14	10478-I	1	SCHEMATIC DWG. DATA DISC #	10478 I
13	C1-C2	2	3.3 µF @ 15V CAPACITOR	KEMET
12	10478 C	1	P.C. BOARD # 10478-C	DATA DISC
11	Q1 THROUGH Q18	18	2N3646 TRANSISTOR	FAIRCHILD
10	Q18	1	2N3644 TRANSISTOR	FAIRCHILD
9	C3	1	2.2 µF CAPACITOR @ 20V	KEMET
8	C4-C5	2	.01µF CAPACITOR	SPRAGUE
7	CR1 THROUGH CR4	4	FDM 6000 DIODE	FAIRCHILD
6	R41-R42	2	10.2K 1/2 WATT 1%	GH
5	R35	1	6.8K 1/2 WATT 5%	GH
4	R40	1	1K 1/2 WATT 5%	GH
3	R33-R34-R39	3	4.7K 1/2 WATT 5%	GH
2	R37-R38-R43-R44	4	10K 1/2 WATT 5%	GH
1	R1 THROUGH R32, R36	33	3.3K 1/2 WATT 5%	GH

NOTES
1. SOLDER ALL TOP-BOTTOM CONNECTIONS, ON BOTH SIDES OF BOARD
2. R45 ADDED DURING FINAL CHECKOUT AS NECESSARY

X SELECTION & INPUT NETWORK

AD-C-10478-G

DATA DISC INCORPORATED

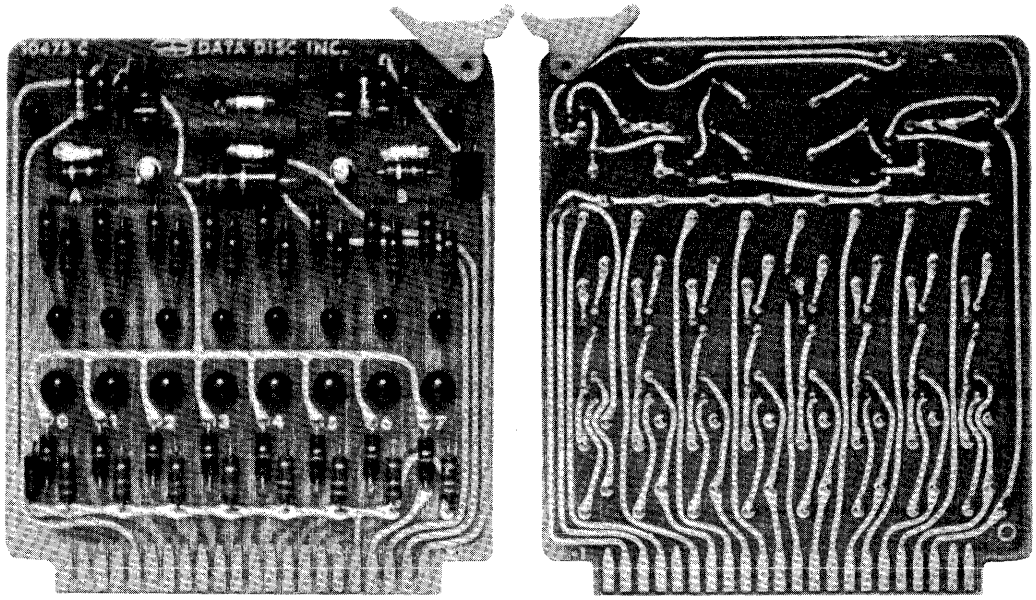


Figure 4-18 Y Drivers and Write Amplifier Card

4.9 Y DRIVERS & WRITE AMPLIFIERS CARD (10475)

4.9.1 General Description - Y Drivers

Each Y Driver converts a Y-Selection signal from the INTERFACE to ground the center-tap of a set of eight heads in the head selection matrix. The Y Drivers operate in conjunction with the X Drivers and the X-Selection and Input Network to connect the specified magnetic head to either the read or write amplifiers. There are eight Y Drivers, numbered 0 through 7 on the card. The Y Driver and Write-Amplifiers Card is mounted in the electronics card cage at connector S14, and is connected to the Write Control Card and the INTERFACE.

Write-Amplifiers. The write-amplifiers provide currents to the selected magnetic head to switch the magnetic coating of the disc to either positive or negative saturation.

4.9.2 Functional Description

Y Drivers. When the Y-0 select-line, pin -18, is between -4.0 and +1.0 volts, it is not selected. Under these conditions, transistors Q1 and Q2 are OFF, and the 20 volts applied through the collector-resistor R4 at Q2 back-biases the diodes on the diode cards of the eight heads on the Y-0 line, i.e., heads 00, 10, 20, 30, 40, 50, 60, and 70. When a voltage greater than 1.7 volts is applied to pin -18, transistors Q1 and Q2 are turned ON, grounding the Y-0 line. This grounds the center taps of all Y-0 line heads such that the one head which has positive voltage from the X-Driver applied to its selection diodes (therefore causing those diodes to conduct), will be selected for reading or writing. The other Y-select lines (Y-1, Y-2, etc.), work in a similar manner.

Write Amplifiers. There are two write-amplifiers on the card, each consisting of two transistors. Operation of one of the amplifiers is as follows: when Write Data (WD) goes high at pin X22, Q17 is turned ON, lowering its collector to turn Q18 ON, and thereby providing a Write signal of approximately 100 milliamperes from the +20-volt supply through R43 and R37. This signal goes out pin X2 and through the windings of one side of the magnetic head to the ground at the center tap provided by the selected Y driver.

The other write amplifier operates in a similar fashion. The voltage drop across R43 helps to turn OFF one write amplifier rapidly when the other turns ON.

Together, the two write-amplifiers provide 100 ma of current which is switched between the two halves of the magnetic head to cause a magnetic field in the head of first one polarity and then the other, in turn causing the magnetic flux of the disc coating to switch between positive and negative saturation. Figure 4-18 shows the path write current follows from the write-amplifier through the various components of the head-selection matrix to the ground supplied by the Y Driver.

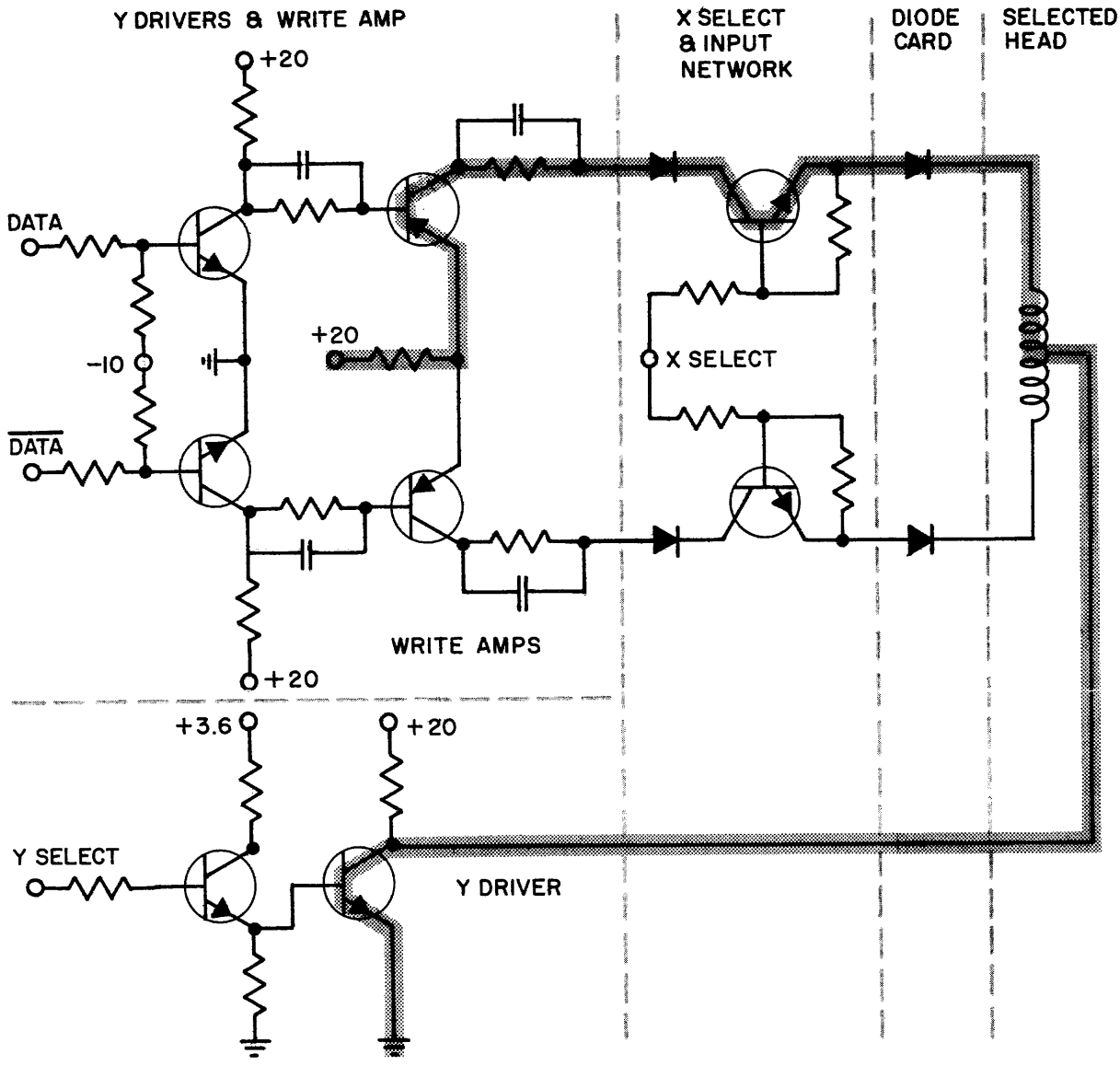
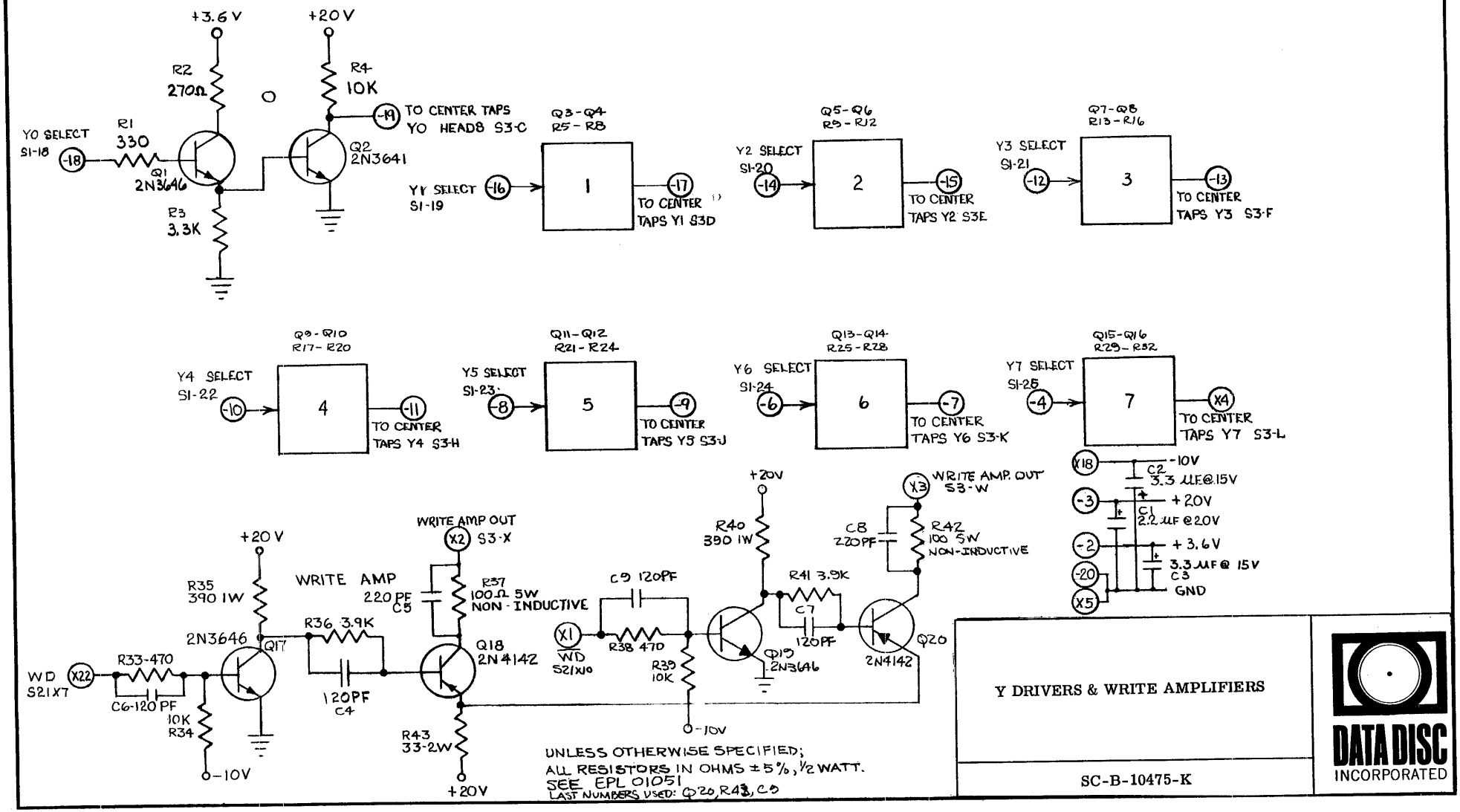
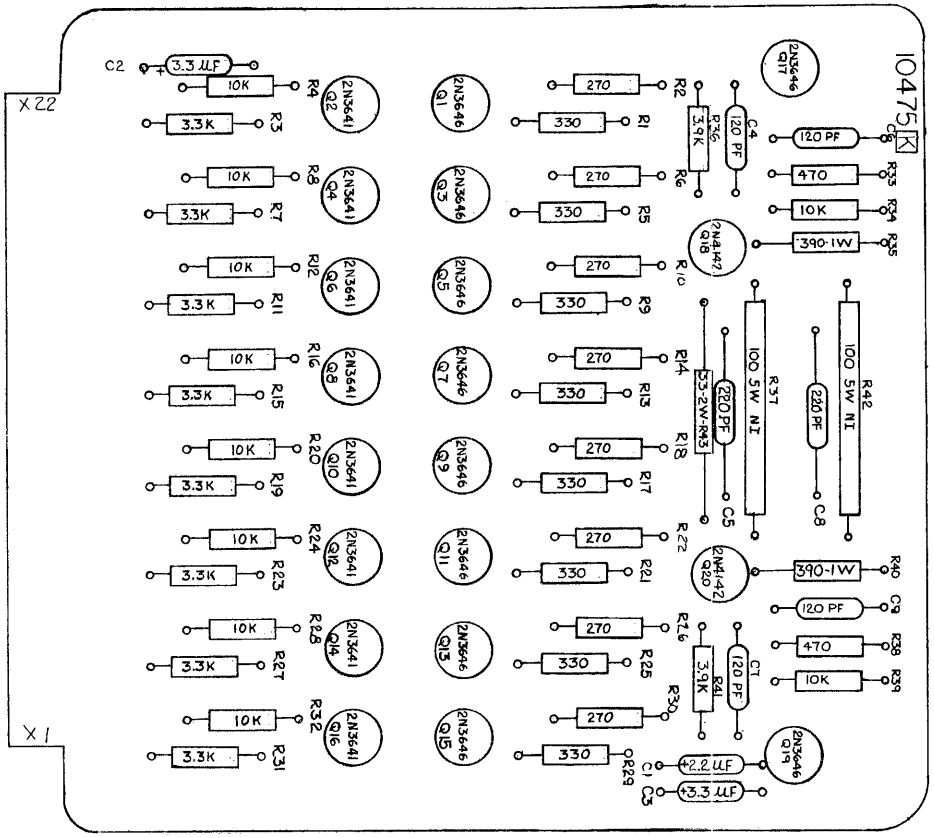


FIGURE 4-19

WRITE CURRENT PATH


+3.6 V
+20 V
R2
270Ω
R4
10K
TO CENTER TAPS
Y0 HEAD8 S3-C
Y0 SELECT
S1-18
R1
330
Q1
2N3646
Q2
2N3641
B3
3.3K
Q3-Q4
R5-R8
Y1 SELECT
S1-19
TO CENTER
TAPS Y1 S3D
Q5-Q6
R9-R12
Y2 SELECT
S1-20
TO CENTER
TAPS Y2 S3E
Q7-Q8
R13-R16
Y3 SELECT
S1-21
TO CENTER
TAPS Y3 S3-F
Q9-Q10
R17-R20
Y4 SELECT
S1-22
TO CENTER
TAPS Y4 S3-H
Q11-Q12
R21-R24
Y5 SELECT
S1-23
TO CENTER
TAPS Y5 S3-J
Q13-Q14
R25-R28
Y6 SELECT
S1-24
TO CENTER
TAPS Y6 S3-K
Q15-Q16
R29-R32
Y7 SELECT
S1-25
TO CENTER
TAPS Y7 S3-L
-10V
C2
3.3 μF@15V
+20V
C1
2.2 μF @20V
+3.6 V
3.3 μF @ 15V
C3
GND
WRITE AMP OUT
S3-X
WRITE AMP
R35
390 1W
220 PF
C5
R37
100Ω 5W
NON-INDUCTIVE
R36 3.9K
2N3646
Q17
WD
S21X7
R33-470
C6-120 PF
10K
R34
120PF
C4
Q18
2N4142
R43
33-2W
C9 120PF
WD
S21X10
R38 470
R39
10K
R40
390 1W
Q19
2N3646
R41 3.9K
C7
120PF
C8
220PF
R42
100 5W
NON-INDUCTIVE
WRITE AMP. OUT
S3-W
Q20
2N4142
UNLESS OTHERWISE SPECIFIED;
ALL RESISTORS IN OHMS ±5%, ½ WATT.
SEE EPL 01051
LAST NUMBERS USED: Q20, R43, C9
Y DRIVERS & WRITE AMPLIFIERS
SC-B-10475-K
DATA DISC
INCORPORATED



Component Designation	Qty.	DD P/N	Description	Mfr.
SC-B-10475-K	1		Schematic	
10475-C	1		P.C. Board	
Q2,4,6,8,10, 12,14,16	8	3107	2N3641 Transistor,NPN	Fairchild
Q1,3,5,7,9,11, 13,15,17,19	10	3109	2N3646 Transistor,NPN	Fairchild
Q18,20	2	3112	2N4142 Transistor,PNP	G.I.
R43	1	1003	33 ohm Resistor, 2w, 5%	G.H.
R37,42	2	1032	100 ohm Resistor, 5w,5%, N.I.	Sprague
R2,6,10,14,18, 22,26,30	8	1001	270 ohm Resistor, ¼w,5%	G.H.
R1,5,9,13,17, 21,25,29	8	1001	330 ohm " " " "	
R35,40	2	1002	390 ohm Resistor, 1w,5%	G.H.
R33,38	2	1001	470 ohm Resistor, ¼w,5%	G.H.
R3,7,11,15,19,23, 27,31	8	1001	3.3K Resistor, ¼w, 5%	G.H.
R36,41	2	1001	3.9K Resistor, ¼w, 5%	G.H.
R4,8,12,16,20,24, 28,32,34,39	10	1001	10K Resistor, ¼w, 5%	G.H.
C4,6,7,9	4	1100	120 pf Capacitor, Poly-styrene	CRL
C5,8	2	1100	220 pf " "	"
C1	1	1102	2.2 uf, 20V Capacitor, Tantalum	Kemet
C2,3	2	1102	3.3 uf, 15V Capacitor, Tantalum	Kemet
Ejector	1	5083	Card Ejector #S202	Scanbe
8013-K	1	8013	Revision Tag	Brady

Y DRIVERS & WRITE AMPLIFIERS

AD-B-10475-E

DATA DISC INCORPORATED

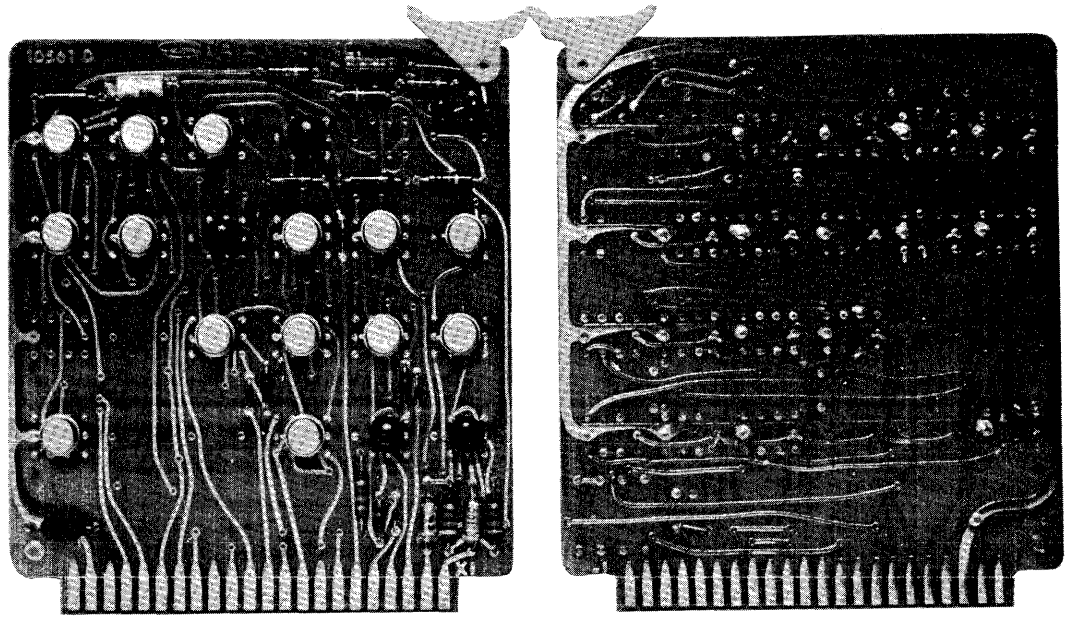


Figure 4-20 Write Control Card

4.10 WRITE CONTROL CARD (10561)

4.10.1 General Description

The Write Control Card controls the start and stop of the write operation internal to the F-Unit, and encodes data received from the INTERFACE before they are recorded onto the disc by the Write-amplifiers and magnetic heads. The Read Inhibit* (RI*) pulse is generated by the Write Control Card at the end of a write operation or when a Head Change* (HC*) pulse is received.

Data encoding permits generation of self-clocking data when the data are read back from the disc. A Modified Non-Return-to-Zero (M-NRZ) code is used to allow self-clocking without an increase in the number of flux transitions required per data bit. For random data, this coding guarantees an average of one flux transition for every 1.5 data bits. Data encoding rules are given in section 2.5.3.

The Write Control Card is inserted in the electronics card cage at connector S21, and is interconnected with the Read Control, the Bit Clock Read-Amplifier, the Write-Amplifiers and Y-Selection, and the Multipurpose Cards, and to the INTERFACE.

4.10.2 Functional Description - Initialization

When 3.6-volt power is first applied to the F-Unit, an initializer circuit (C4, R4 and D2A) operates. Capacitor C4 is charged through R4, and when C4 reaches the 0.8 volt threshold of D2A, the D2A output changes from high to low. The high output resets FF's WA-1, WA-2, and WA-3 (B3, C2 and B2). The WA-2 output of (C2) is low after being reset. This output is inverted by D3C to reset FF's DW-1, DW-2 and EDFF (D1, E1 and C3). Note Figure 4-21.

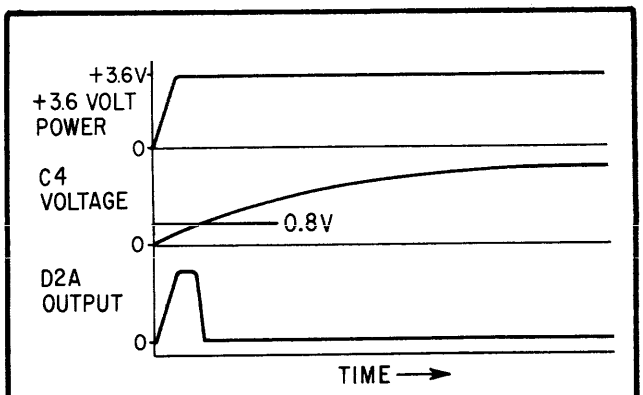


FIGURE 4-21

INITIALIZATION PULSE GENERATION

Control - The control section of the Write Control Logic consists of the following elements:

Control lock-out FF-B4A/B4B
Write control timing chain FF's-B3, C2, B2
Initializing inverter D2A
Write Enable (WE*) gate D2B
End of Write (EOW) gate A4B
1.2 usec One Shot F1B/B1A
200 usec, Read Inhibit Fast-recovery One-Shot Q1 and Q2 with output inverter B1B
Inverters D3A, D3B, D3C, D3D

The Write Timing Diagram, Figure 4-23, will be of assistance in understanding the control and encoding operation of the Write Control Logic.

The W* input on X5 is the WRITE* control line from the INTERFACE. When W* is low, writing is requested; when W* is high, writing is not requested.

The R* input on X3 is the READ* control line from the INTERFACE. When R* is low, reading is requested; when R* is high, reading is not requested. When both W* and R* are high, WA (the output of B4A) and RA (the output of B4B) are low. WA is inverted by the inverter D3B to give WA* high.

While WA is low, WA-3 is also low as a result of the initialization reset. These two low signals are applied to NOR gate D2B, making its WE* output high. WE* high is fed to the dc preset pin of FF A3 where it forces A3's 1G* output high. WE* high is also applied to NOR gates C4A and C4B to keep their WD* and WD outputs low. The WD* and WD outputs leave the PC card and connect to the inputs of the two write amplifiers. A write amplifier is OFF when its input is low. Therefore, before the start of write when both WD* and WD are low, head current is zero, as shown in the actual waveform photograph, Figure 4-22. After writing starts WD* and WD are high alternately so that the write amplifiers operate in push-pull, causing head current to flow first one way and then the other.

The control lock-out FF (B4A/B4B) is so named because when either of the control inputs (W* or R*) becomes low, the FF assumes a latched state which the other control input cannot alter. For example, when W* becomes low, WA becomes high, guaranteeing that the RA output of B4B will remain low even if R* becomes low.

The Write Control timing chain FF's (B3, C2 and B2) are a shift register which controls turn-on and turn-off events at the beginning and end of a Write operation. The Write operation starts when WA becomes high. The instant WA becomes high, WA-1 also becomes high through the dc-set input to pin 1 on B3. WA-2 becomes high on the first negative transition of the O-G* clock, and WA-3 becomes high on the second negative transition of the O-G* clock.

When WA becomes low at the end of a Write operation, WA-1 becomes low at the next negative transition of the O-G* clock, WA-2 becomes low at the next following negative transition, and WA-3 becomes low at the next negative transition of the O-G* clock after that. The Write operation internal to

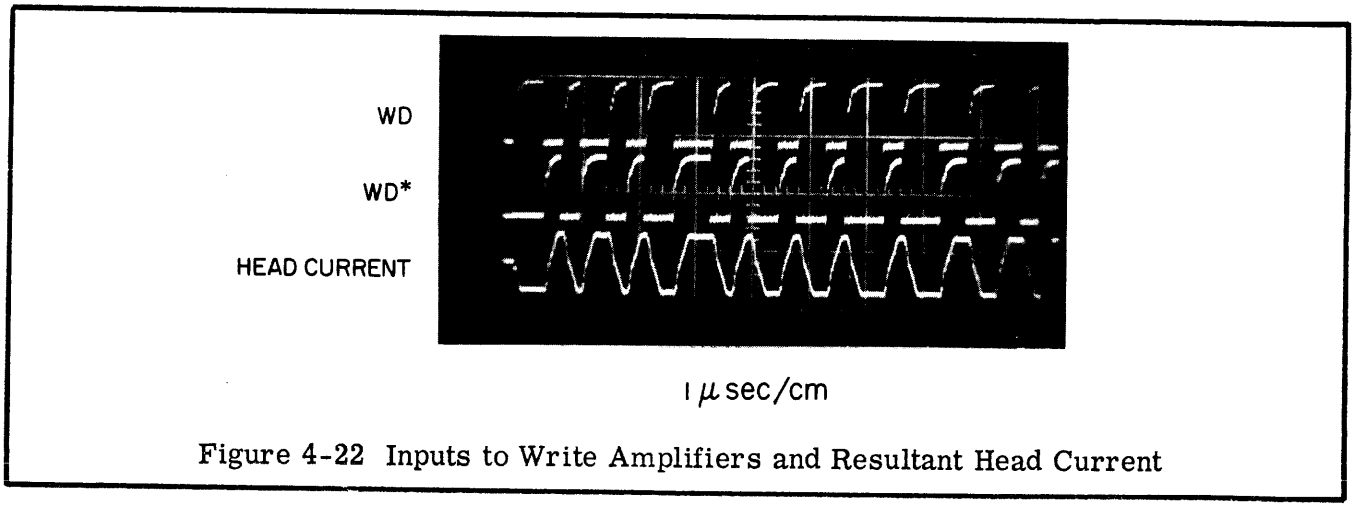


Figure 4-22 Inputs to Write Amplifiers and Resultant Head Current

the unit ceases when WA-3 becomes low.

The WE* gate D2B becomes low at the start of a write operation when WA becomes high, and becomes high again when WA is low and WA-3 becomes low at the end of the write operation. While WE* is low, the 1-gate* (1-G*) and O-gate* (O-G*) bit rate clocks are generated by FF A3. The Write Data (WD and WD*) gates C4A and C4B are partially enabled when WE* is low. The WTO* input to C4A and C4B will be low after the 20-second disc-turn-on time delay has expired.

The EOW gate A4B becomes high for one bit-time at the end of write, the last bit-time before WE* becomes high. On the Write Timing Diagram EOW becomes high at the time when WA-2* is high and WA-3* is low.

The 1.2-microsecond one-shot F1B/B1A will fire either when EOW becomes high or upon receipt of a negative pulse on the HC* line from the INTERFACE. A 1.2-usec positive pulse is generated at B1A pin 7 which drives the base of Q1. Q1 conducts, and discharges C6. Q2, which was conducting while C6 was charged, now ceases conducting until the charge on C6 becomes positive enough to turn Q2 ON again. The time required for this is approximately 200 microseconds. Q1 and Q2 form a fast-recovery one-shot which can be recycled immediately after firing or restarted in the middle of firing.

Clock Derivation - The clock derivation section consists of the following elements:

- Differentiators C2/R1 and C3/R2
- Clock Track* (CT*), gate A4A
- One-Gate* (1-G*) FF A3
- Zero-Gate* (O-G*) inverter A2
- Write Clock (WC) gate F4A
- Read/Write Clock* (RWC*) combining-gate F4B

Differentiators C2/R1 and C3/R2 on input pins X1 and X2 differentiate the clock read-amplifier outputs CRA^{+} and CRA^{-}. Gate A4A combines the pulses to form Clock Track* (CT*). WE* becomes low to remove the dc preset, and CT is divided by the 1-G* FF A3. 1-G* is inverted by A2 to form O-G*. 1-G* is used for encoding binary ones in the data write (DW) input. O-G* is used for encoding binary zeroes in the DW signal, and also is passed through NOR gates F4A and F4B to form the Read/Write Clock* (RWC*) going to the INTERFACE via pin X18. The negative transitions of the O-G* signal are used to clock FF's B3, C2, B2, D1 and E1.

Data Write Encoding - The encoding section consists of the following elements:

- DW input gates C1A and C1B
- DW two-bit shift register D1 and E1
- Encoding gates E2B, F2A, F2B, F1A and E2A
- Encoded Data FF C3
- Write Data output gates C4A and C4B

As shown in the timing diagram, Figure 4-23, the first data bit is not shifted into the DW-1 FF until the sync bit is generated by the Encoder Sync (ES) gate E2B. The ES pulse dc sets a binary one into DW-1 and enables the Encoded Data FF (EDFF) to change state at the end of the sync bit cell. The CT* transition which caused the EDFF to change state and every second CT* transition which follows can be considered as a "ones"transition of the CT* clock. The next CT* transition would be an "even" transition. This even transition and every second one which follows can be considered as a "zeroes" transition of the CT* clock. The sync bit cell is the cell ahead of the first data bit cell. The sync bit level in DW-1 is shifted into DW-2 by the O-G* negative transition as the first data bit is shifted into DW-1. Now and hereafter DW-1 contains the data bit being encoded and DW-2 contains the previous data bit.

A one-pulse (1-P) is generated by gate F1A to enable the EDFF input whenever the DW-1 FF contains a binary one. A zero-pulse (O-P) is generated by gates F2A and F2B to enable the EDFF input when, and only when, both DW-1 and DW-2 contain a binary zero. The 1-G* signal causes the 1-P signal to be high at the end of a bit cell in order to select the "ones" transition of the CT* signal. The O-G* signal causes the O-P signal to be high in the middle of a bit cell in order to select the "zeroes" transition of the CT* signal.

The Write Data output gates C4A and C4B turn ON either the WD or WD* output to the Write Amplifiers as directed by the ED and ED* outputs of FF C3. When WE* becomes high at the end of Write, gates C4A and C4B turn OFF outputs WD and WD*.

This page purposely left blank.

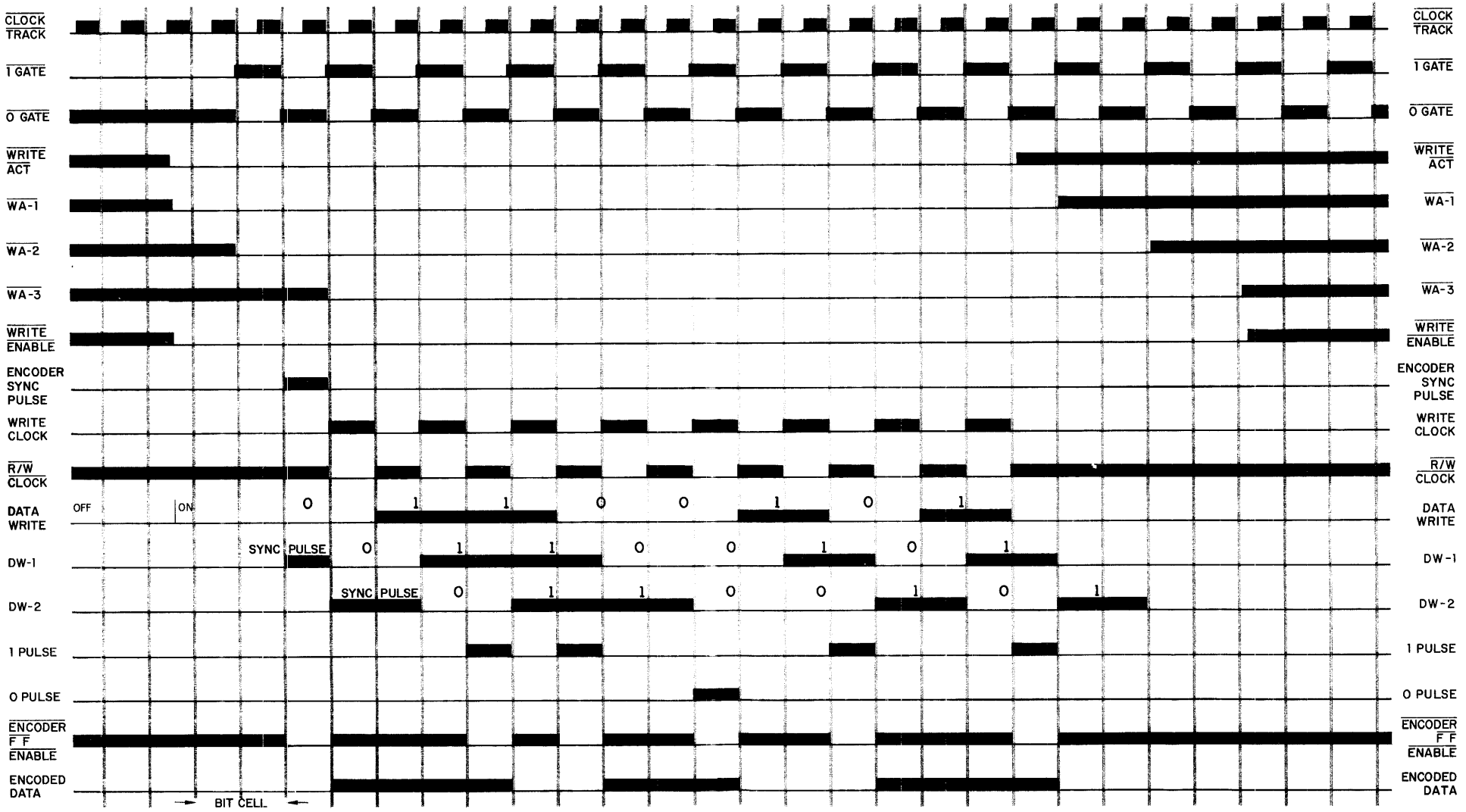
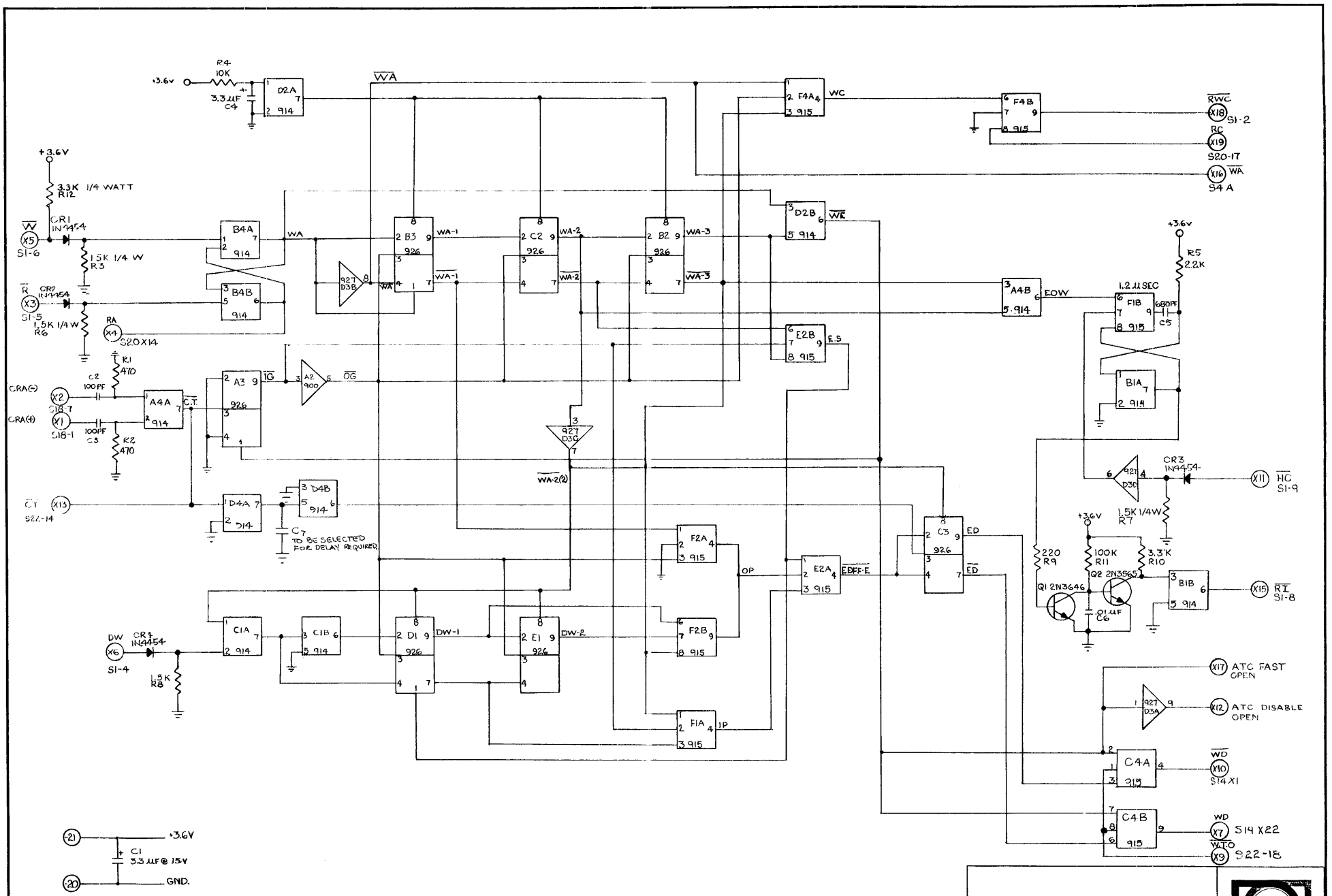
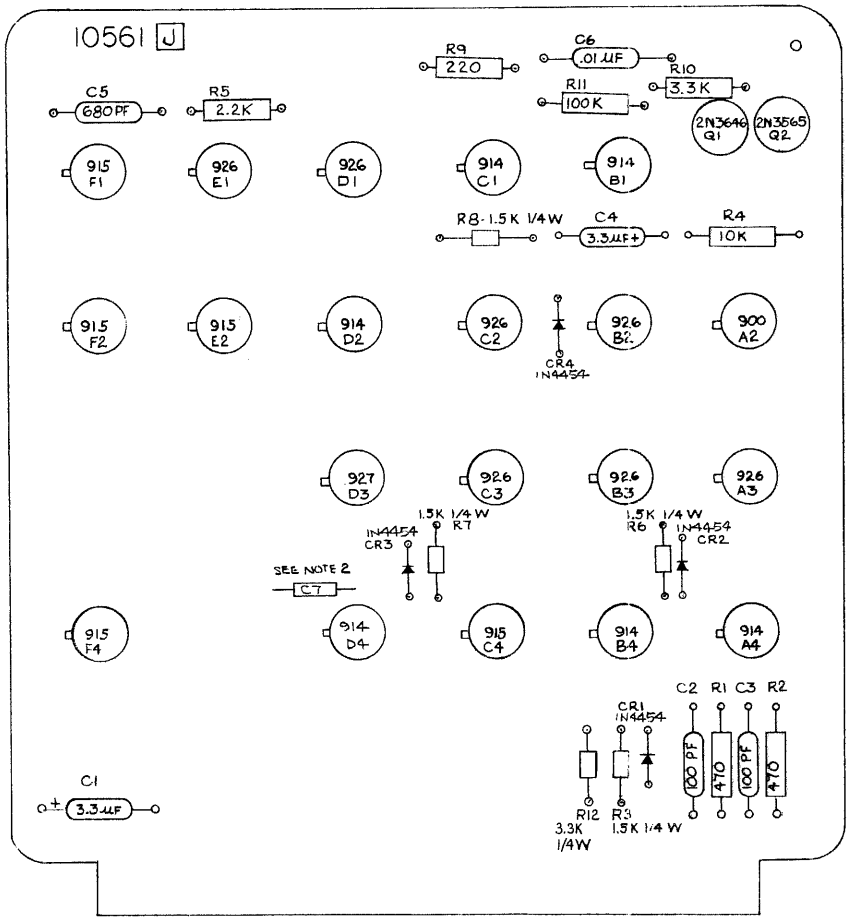


FIGURE 4-23
WRITE DATA TIMING DIAGRAM

This page purposely left blank.


WRITE CONTROL
SC-C-10561-G
DATA DISC INCORPORATED



ITEM	COMP. DESIG.	QUAN.	DESCRIPTION & MANUFACTURER	
25	SC-C-10561-J	1	SCHEMATIC	
24	8613-J	1	REVISION TAG	BRADY
23	C7	1	SELECT FOR PROPER DELAY	CRL
22	EJECTOR	1	CARD EJECTOR # S202	SCANBE
21	Q2	1	2N3565 TRANSISTOR	FAIRCHILD
20	Q1	1	2N3646 TRANSISTOR	FAIRCHILD
19	CR4-CR3-CR2-CR1	4	1N4454 DIODE	G.E.
18	C5	1	680 PF CAPACITOR	CENTRA-LAB
17	R9	1	220 1/2 WATT RESISTOR	G.H.
16	C6	1	.01 µF CAPACITOR	SPRAGUE
15	C2-C3	2	100 PF CAPACITORS	CENTRA LAB
14	R1-R2	2	470 1/2 WATT 5% RESISTOR	G.H.
13	10561-F	1	P.C. BOARD # 10561-F	DATA DISC
12	R11	1	100K 1/2 WATT 5% RESISTOR	G.H.
11	R10	1	3.3K 1/2 WATT 5% RESISTOR	G.H.
10	R8-R7-R6-R3	4	1.5K 1/4 WATT 5% RESISTOR	G.H.
9	R12	1	3.3K 1/4 WATT 5% RESISTOR	G.H.
8	R4	1	10 K 1/2 WATT 5% RESISTOR	G.H.
7	C1-C4	2	3.3 µF @ 15V CAPACITORS	KEMET
6	R5	1	2.2K 1/2 WATT 5% RESISTOR	G.H.
5	A2	1	900 MICROLOGIC CAN	FAIRCHILD
4	D3	1	927 MICROLOGIC CAN	FAIRCHILD
3	C1,D2,A4,B4,B1,D4	6	914 MICROLOGIC CANS	FAIRCHILD
2	F1-F2-E2-F4-C4	5	915 MICROLOGIC CANS	FAIRCHILD
1	E1-D1-C2-B2-C3-B3-A3	7	926 MICROLOGIC CANS	FAIRCHILD

NOTES:

1. ALL NUMERALS WITH "X" FOLLOWING MEANS + VOLTAGE PIN NOT CONNECTED.
2. C7 ADDED DURING CHECKOUT FOR PROPER DELAY IF NECESSARY.

WRITE CONTROL

AD-C-10561-J

DATA DISC INCORPORATED

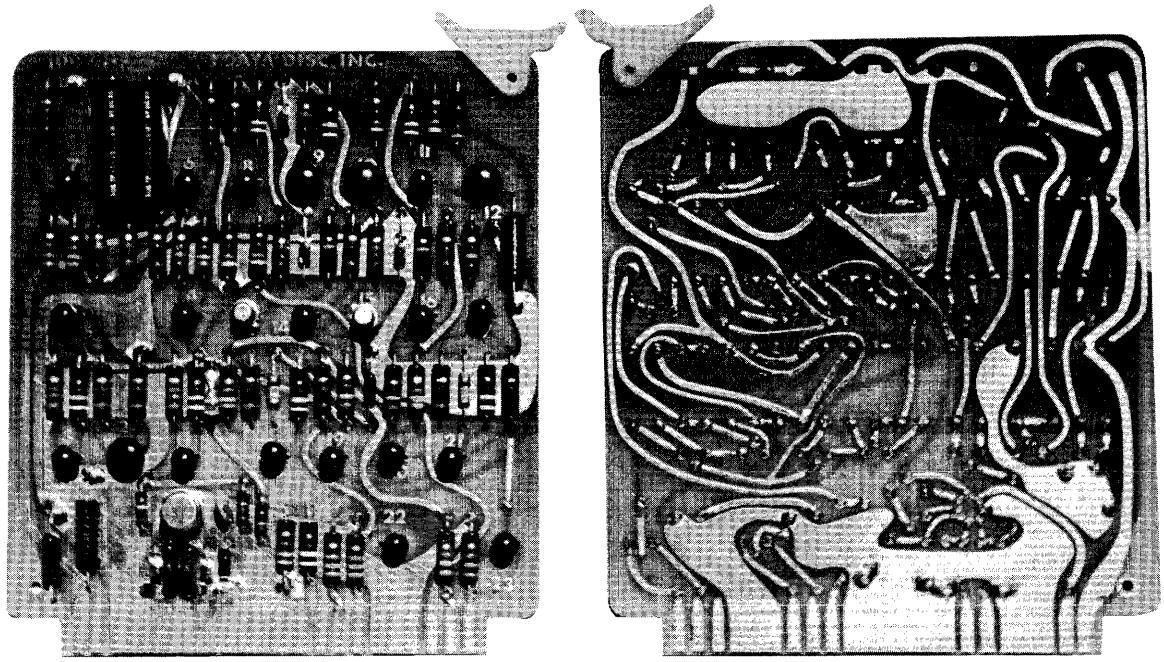


Figure 4-24 Read Amplifier Card

4.11 READ AMPLIFIERS (10473)

4.11.1 General Description

Three read amplifiers are used in the F Series electronics system, all basically the same unit. Each is a high-gain, wideband, dc-coupled differential amplifier with peak-detection circuitry. Two threshold stages are used to minimize noise problems, one before peak detection and one after. The Data Read-Amplifier and Bit Clock Read-Amplifier employ fast envelope-following Automatic Threshold Control (ATC) in the predetection section which functions over a peak-to-peak signal range from five to 50 millivolts. The Sector Clock Read-Amplifier uses a slow ATC in the peak detection section. All three read amplifiers use fixed threshold control in the post-detection section.

Read-Amplifier output is suitable for driving micrologic. Signal rates of up to five-million bits/second are accommodated by the amplifiers. All of the read amplifiers are housed in the electronics card cage, the Data Read-Amplifier Card at S16, the Bit Clock Read-Amplifier Card at S18, and the Sector Clock Read-Amplifier at S19. The Bit Clock Read-Amplifier Card is connected to the Write Control Card. The Sector Clock Read Amplifier Card is connected to the Multipurpose Card. The Data Read Amplifier Card is connected to the VCO and Control Card.

4.11.2 Functional Description

Figure 4-25 is a block diagram of the Wideband Read Amplifier. An explanation of the functional blocks follows, with reference to components as shown on Drawing 10473. Actual waveforms taken from a typical read amplifier are shown in Figure 4-26.

Preamplifier - The preamplifier is a monolithic differential amplifier with a nominal voltage gain of 100 and a bandpass of dc to 7MHz. Because the head assembly is relatively unshielded, a differential amplifier is required to provide common-mode noise rejection greater than 60 db. Drawing 10473 shows C7 across the input leads on pins -16 and -17. The bit-clock read amplifier uses this capacitor to "tune the head," thereby increasing the amplitude of the high-density clock. C6 and R56 are not used on the F Series systems. R1 and R2 provide input impedance of 2K ohms. The Input Network may shunt this impedance with R45 to provide correct head termination. A feedback loop is used to set the gain. Two limiting diodes CR1 and

CR2 limit positive pulses to protect the preamplifier.

NOTE: R3 is selected to optimize amplifier gain to fit the application of the card as a Data or Clock Read Amplifier. Because the gain is higher on the Clock Read Amplifiers, the Read Amplifier cards cannot be interchanged (as in substitution procedures during trouble shooting) unless R3 is changed accordingly.

Phase-Inverter Amplifier - The phase inverter converts the preamplifier's single-ended output to two signals which are 180 degrees out of phase. Q1 and Q3 are inverters which split the signal from the differential amplifier. The signal at the collector of Q3 is equal and opposite the signal at the collector of Q1. Both Q4 and Q5 invert and double the amplitude of the signal supplied and apply it to emitter followers Q6 and Q7. Test Points A and B are essentially opposite in phase. With the signals (at Test Points A and B) balanced and their offset adjusted as described in the Alignment Section which follows, both waveforms swing about zero (approximately). The negative portion is clipped by diodes CR4 and CR5 to protect the threshold transistors. Signals at the Test Points are illustrated in Figure 4-26.

Automatic Threshold Control (ATC) - The Automatic Threshold Control delivers a dc signal proportional to the peak amplitude of the phase-inverter-amplifier output. R57 is 470 ohms to provide a 30% reference level. Resistors R25 and R57 divide the signal, and diode CR6 clips the negative portion to provide a positive signal. C4 is the ATC capacitor which is kept charged as long as there is a signal on Q9.

Q9 is normally conducting and Q10 is cut off by the ATC voltage on its base. When the positive pulses on the base of Q9 exceed the

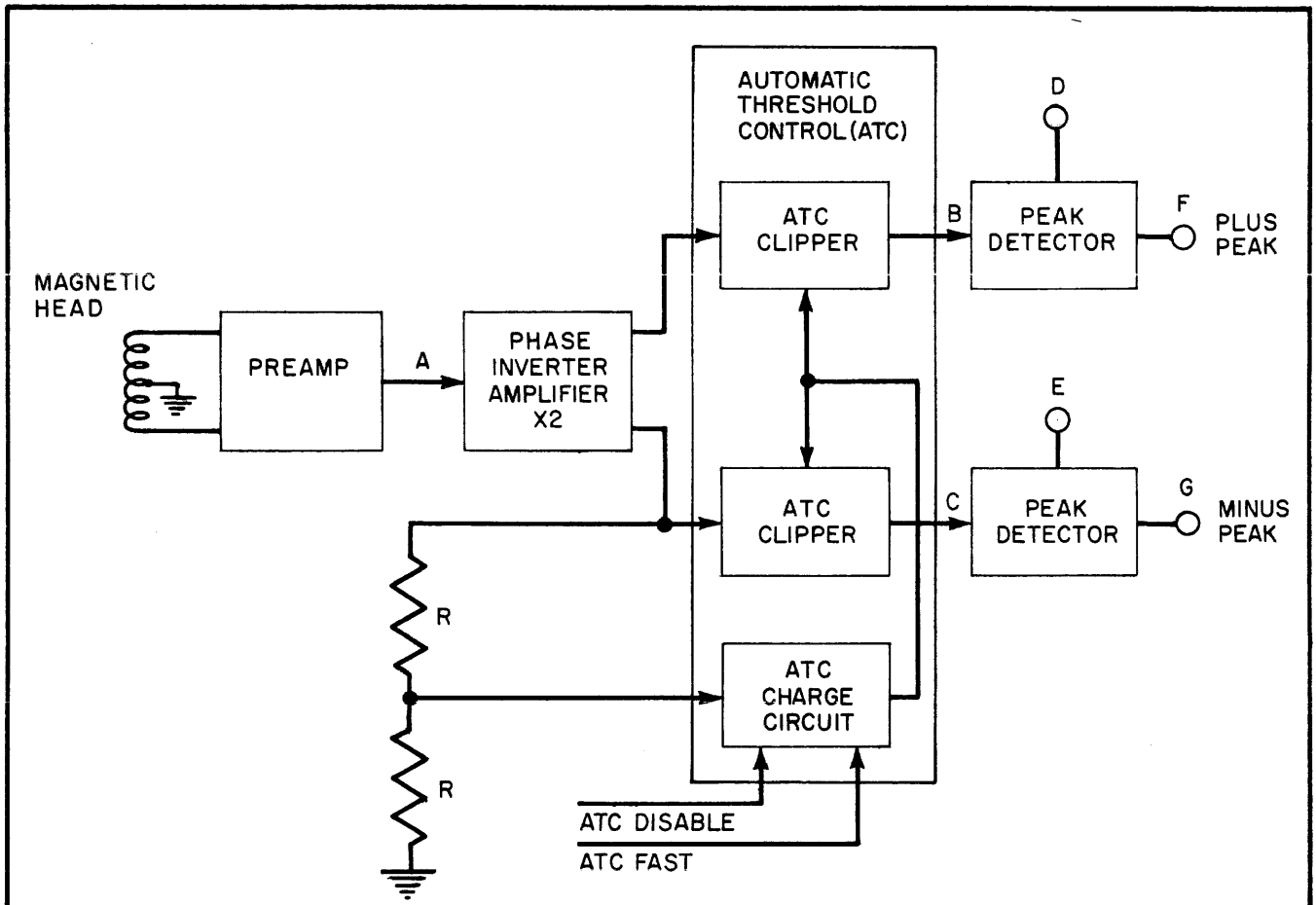


FIGURE 4-25
WIDEBAND DATA READ AMPLIFIER

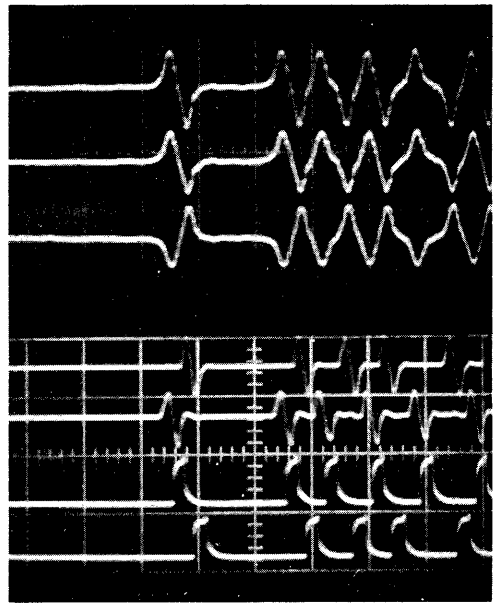


Figure 4-26 Actual representative waveforms from the high-density read amplifier

positive ATC voltage on the base of Q10, Q9 is cut off and Q10 conducts. The collector of Q11 becomes more negative, turning on Q12 to add charge to the ATC capacitor C4. C4 is thus kept charged to the peak value of the 30% reference level when Q17 is OFF.

When Q17 is ON, C4 discharges rapidly through R37 and Q17 to provide the envelope-following characteristics as shown in Figure 4-27. When Q17 is OFF, as in the case of the Sector Clock Read Amplifier, C4 discharges slowly through the base impedances of Q10, Q14, and Q16.

ATC Fast - When envelope following is employed in the Clock Read Amplifiers, ATC Fast provides a rapid discharge path for ATC capacitor C4 as previously noted. The envelope-following characteristic of the read amplifier is evident in Figure 4-27.

ATC Disable - This circuit is not used on F Series units. The input is disabled (open).

ATC Clipper - Transistors Q14 and Q16 are emitter followers which isolate the ATC capacitor C4 from the bases of Q13 and Q15. The ATC voltage on the bases of Q13 and Q15 determines that portion of the signal on the emitter of each transistor which will reach the collector. These transistors perform the threshold noise limiting prior to peak detection.

Peak Detector - The peak detector differentiates the clipped signal, Figure 4-28 lines B and C, and converts the signal into a

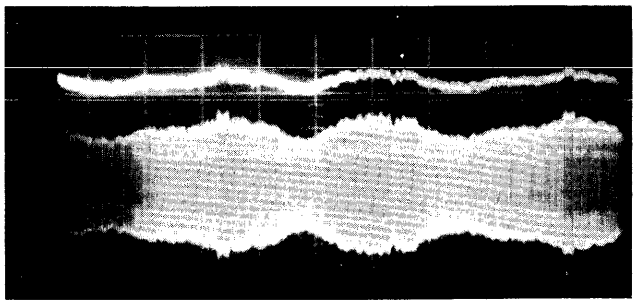


Figure 4-27 Envelope-following capability of ATC voltage

doublet as shown in lines D and E. The zero crossing of the differentiated signal corresponds to the peak, or zero slope of the input signal. Passing the signal through a clipping stage and squaring up the negative part of the doublet gives a signal whose leading edge corresponds to the head-signal peak. There are two of these circuits, one each to detect positive and negative head read signal peaks (line A). Inductors L1 and L2, and resistors R42 and R43 provide L/R differentiation of the signals at the collectors of Q13 and Q15. The signal applied to the emitter of Q13 is the half of the head signal which is related to the negative-pulse inputs to the read amplifier. The signal applied to the emitter of Q15 is the half of the head signal which is related to the positive-pulse inputs to the read amplifier.

The 6.3-volt dc level on the collectors of Q13 and Q15 is set by Zener diode CR7. A dropping resistor R44 provides the post-detection threshold level by biasing the bases of Q19 and Q21. Q20 and Q21, and Q18 and Q19 are emitter-coupled amplifiers. Q20's threshold-limited differentiated signal appears inverted at the collector of Q21, and the same is true for Q18 and Q19. Output transistors Q22 and Q23 invert the signal and provide voltage-level changing to match the signal requirements of the micrologic circuits which follow in the system.

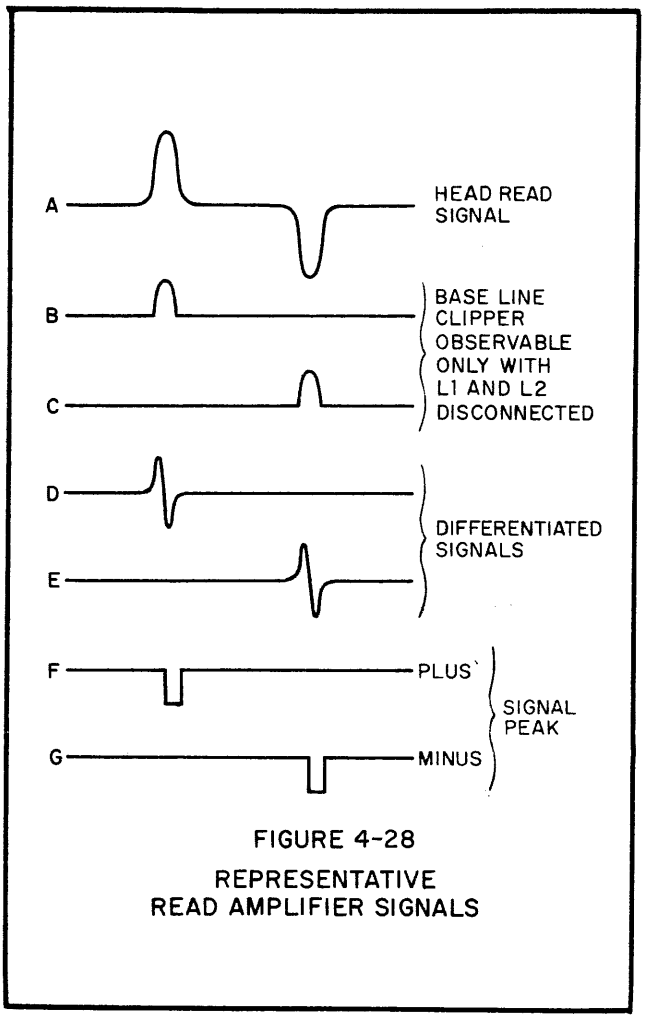


FIGURE 4-28
REPRESENTATIVE
READ AMPLIFIER SIGNALS

4.11.3 Alignment of Read Amplifier

A dc voltmeter with 10,000 ohms/volt impedance and 0.25-volt full-scale capability is recommended for this alignment.

Making the Balance Adjustment - Balance adjustment may be required when components in the front end of the amplifier (ahead of Test Points A and B) have been replaced. The gain of the two sides of the differential amplifier (Q1, Q4, and Q6 vs. Q3, Q5, and Q7) must be balanced as follows.

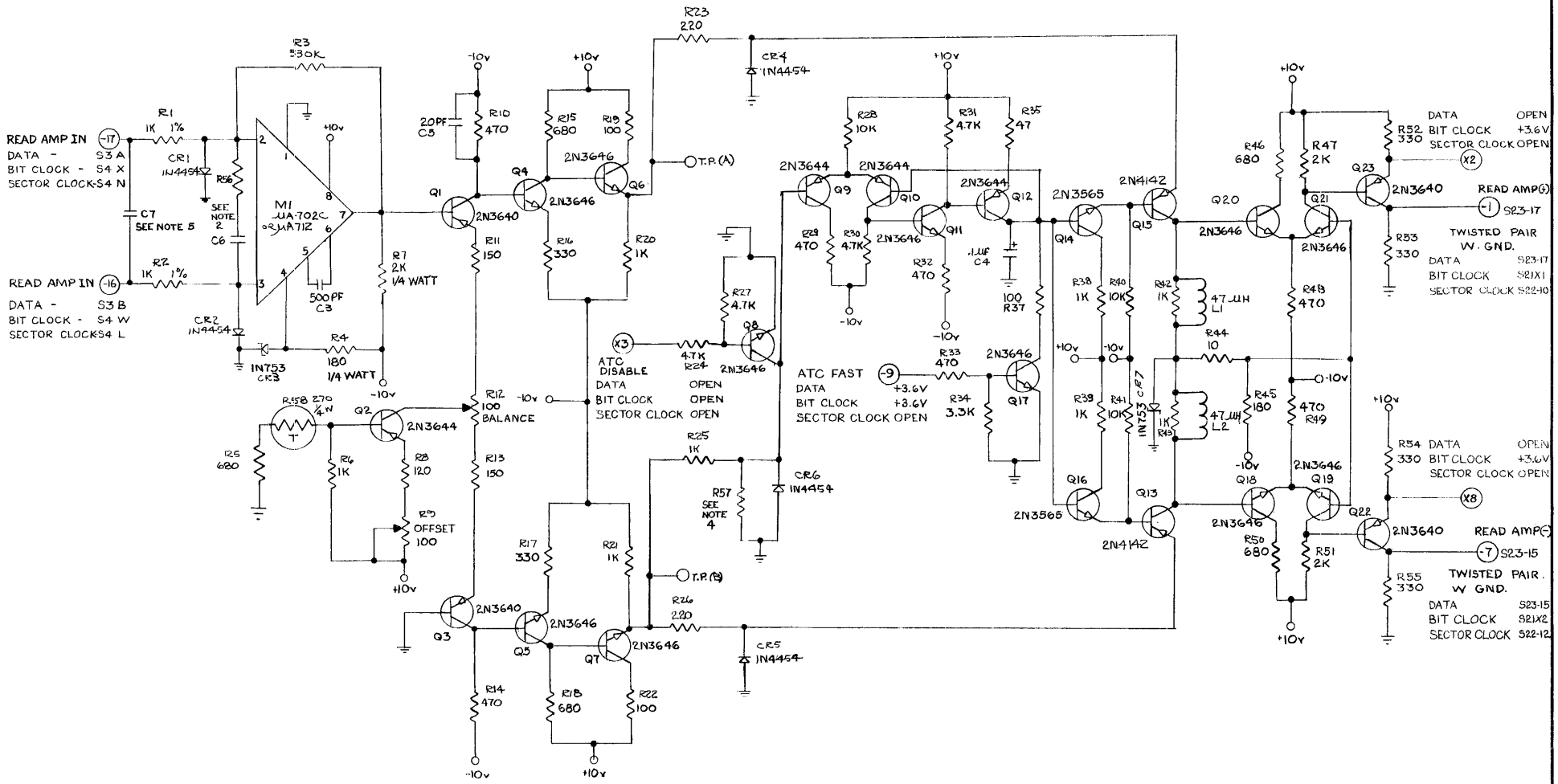
Place one voltmeter probe on TP - A, and the other on TP - B. Adjust balance trimpot "B" (R12) to zero volts on the 0.25-volt scale.

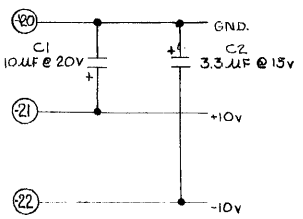
Making the Offset Adjustment - Connect one voltmeter probe to ground and adjust trimpot "O" (R9) so that the dc voltages read at TP - A on each read amplifier are as shown in the table below.

The clock read-amplifier amplitude should be between 3 and 5 volts at TP - A.

READ AMPLIFIER	OFFSET
Sector Clock	-0.4v
Clock	0
Data	-0.2

This completes the read-amplifier alignment.



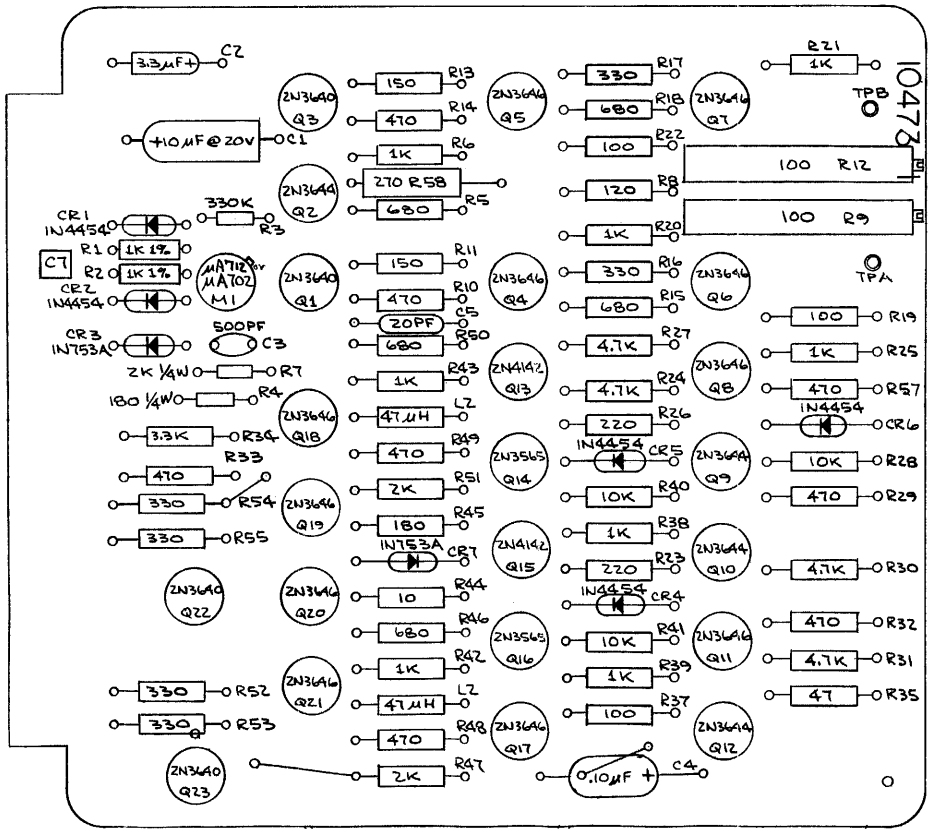


NOTE: 1. UNLESS OTHERWISE SPECIFIED; ALL RESISTORS IN OHMS ± 5%, ½ WATT.
ALL CAPACITORS IN PF.
2. R56, C6 SELECTED TO ROLL OFF AMPLIFIER FREQUENCY RESPONSE. IN LOW BIT RATE APPLICATIONS
3.
4. R57 ADJUSTS THRESHOLD, MAY RANGE FROM 120 Ω TO 1.2K, DEPENDING ON APPLICATION
5. C7 SELECTED TO TUNE BIT CLOCK READ AMPS IN HIGH FREQUENCY APPLICATIONS.
6. LAST NUMBERS USED: M1, Q23, CR7, R58, C7, L2

HIGH-DENSITY READ AMPLIFIER

SC-C-10473-H

DATA DISC INCORPORATED



Component Designation	Qty.	DD P/N	Description	Mfr.
SC-C-10473-H			Schematic	
10473-I			P.C. Board	
M1	1	3232	*μA712 Integrated Circuit	Fairchild
Q14,16	2	3105	2N3565 Transistor	Fairchild
Q1,3,22,23	4	3106	2N3640 Transistor	Fairchild
Q2,9,10,12	4	3108	2N3644 Transistor	Fairchild
Q4,5,6,7,8,11, 17,18,19,20,21	11	3109	2N3646 Transistor	Fairchild
Q13,15	2	3112	2N4142 Transistor	G.I.
CR1,2,4,5,6	5	3008	1N4454 Diode	G.E.
CR3,7	2	3003	1N753A Diode	Fairchild
R44	1	1001	10 ohm, ¼w, 5% Resistor	G.H.
R35	1	1001	47 ohm, ¼w, 5% "	G.H.
R19,22,37	3	1001	100 ohm, ¼w, 5% "	G.H.
R8	1	1001	120 ohm, ¼w, 5% "	G.H.
R11,13	2	1001	150 ohm, ¼w, 5% "	G.H.
R4	1	1000	180 ohm, ¼w, 5% "	G.H.
R45	1	1001	180 ohm, ¼w, 5% "	G.H.
R23,26	2	1001	220 ohm, ¼w, 5% "	G.H.
R16,17,52,53,54 55	6	1001	330 ohm, ¼w, 5% "	G.H.
R10,14,29,32,33 48,49,57	8	1001	470 ohm, ¼w, 5% "	G.H.
R15,18,46,50	4	1001	680 ohm, ¼w, 5% "	G.H.
R1,2	2	1010	1K ohm, 1/8w, 1% "	Ward-Leonard
R5,6,20,21,25, 38,39,42,43	9	1001	1K ohm, ¼w, 5% "	G.H.
R7	1	1000	2K ohm, ¼w, 5% "	G.H.
R47,51	2	1001	2K ohm, ¼w, 5% "	G.H.
R34	1	1001	3.3K ohm, ¼w, 5% "	G.H.
R24,27,30,31	4	1001	4.7K ohm, ¼w, 5% "	G.H.
R28,40,41	3	1001	10K ohm, ¼w, 5% "	G.H.
R3	1	1000	330K, ¼w, 5% "	G.H.
R9,12	2	1053	100 ohm Potentiometer	Beckman
R58	1	1070	270 ohm, ¼w, Sensistor	T.I.
C5	1	1104	20 pf Capacitor	Centralab
C3	1	1104	500 pf Capacitor 500J	Centralab
C4	1	1101	.1 μf 200V DC Capacitor	Sprague
C2	1	1102	3.3 μf, 15V Capacitor	Kemet
C1	1	1102	10 μf, 20V Capacitor	Kemet
L1,2	2	1130	47 μh Inductor	Nytronics
	1	5080	Card Ejector S202	Scanbe
	2	4018	Terminals #13408-1	Useco
*Alternate:		3231	uA702C Amplifier	Fairchild

HIGH-DENSITY READ AMPLIFIERS

AD-B-10473-D

DATA DISC INCORPORATED

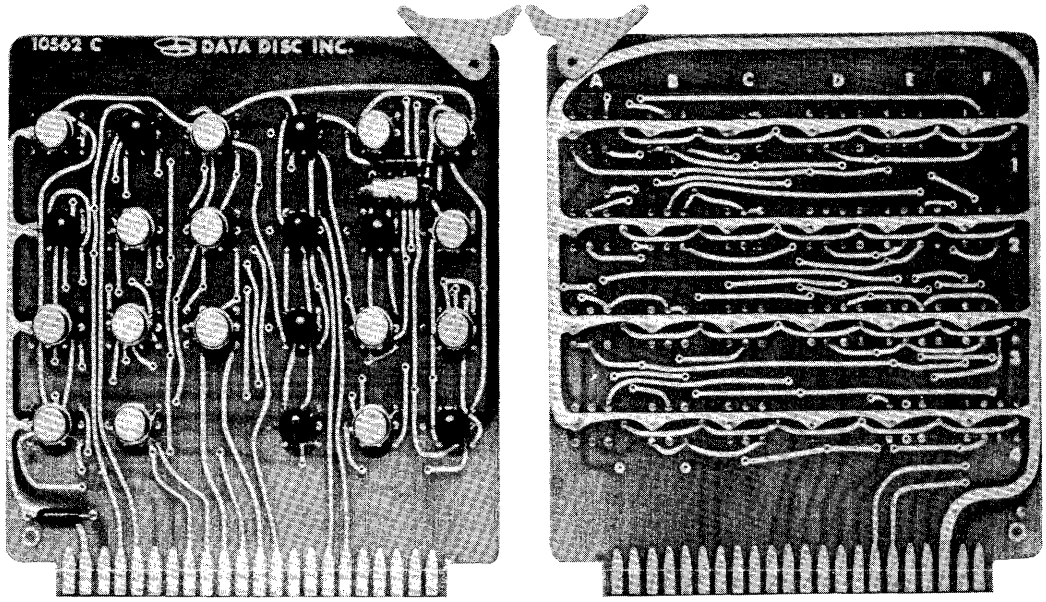


Figure 4-29 Read Control Card

4.12 READ CONTROL (10562)

4.12.1 General Description

The Read Control Card decodes data which are read off of the disc, and supplies these data to the INTERFACE, along with a bit clock which is synchronized with the data. A bit-level error check provides a bit-by-bit check for code violations. This check will detect at least 50% of all possible read errors occurring in random data. The Read Control Card is located at S20 in the card cage and is interconnected with the Read-Amplifier, the VCO and Control, and the Write Control Cards, and to the INTERFACE.

4.12.2 Functional Description

The description following pertains to the operations of the Read Control logic and Read Data Timing. The Read Data Timing Diagram, Figure 4-30, shows idealized signals from a hypothetical eight-bit data sector.

Initialization - The Read Control logic is initialized whenever the Read Act (RA) input on pin X14 is low. The six FF's, D1, D2, D3, E3, F1, and F3 are preset by RA* to bring pin 9 of each FF low. The VCO input on pin X12 is low while RA is high. The Data Read (DR) output on pin -16 and the Read Clock (RC) output on pin -17 are low. The bit-level-error detection output ERROR* on pin X18 is high.

Control - The control section of the Read Control Card is composed of the following elements:

- Read Act buffer/inverter E4
- Sync bit detector gate E1B
- Read Control timing chain E3, and F3
- Timing chain input gates F2A and F2B

The control section operates as follows: Data from the RDFF enters the undecoded data-storage register after the RA line becomes high. The sync bit, which precedes the data, is shifted by the VCO clock into FF D3 and then to FF D2 where it is detected by the sync-bit detector gate E1B. E1B's output becomes high which presets the Data Read FF E2 and switches gates F2A and F2B so that read control timing-chain FF's E3 and F3 become set and latch-up on the two VCO clocks which follow. The one-bit delay thus created is used to mask out the sync bit from the DR output, and to prevent Read Clocks from being output until the first data bit cell.

Decoding Logic - The decoding logic of the Read Control card is composed of the following elements:

Undecoded data storage register: D3, D2, D1
Data Decoding gates: B3A, B3B, A3A, A3B, B1A, A1A, A4A, A4B, B4A, A1B, A2A, A2B, B1B, B4B
Error Decoding gates: C3A, C3B, C4A, C4B, C1A, C1B, C2A, C2B
Error Pulse generator: B2A, B2B and E1A
Data Read FF: E2
Data Output gate: F4A

The decoding logic transforms the modified-NRZ code read from the disc to binary data. The transformation is performed by synchronous demodulation logic which makes the transformation-decision based on examination of the previously decoded data bit stored in the Data Read FF (DRFF) and the undecoded data stored in the undecoded data-storage register D1, D2, and D3. Synchronous bit level error detection is performed by the error decoding gates which check for invalid states in the undecoded data contained in FF's D1, D2, and D3.

DRFF E2 will change state on the negative transition of the VCO clock if and only if Data Read Input (DRI*) (which is present at input pins 2 and 4 of E2) is low. Elements B3A, B3B and A3A form gate W through collector coupling of the NOR gates. Gates X, Y and Z are similarly constructed. If the output of gates W, X, Y or Z becomes high, DRI* becomes low. The timing diagram shows low sections of the DRI* waveform labeled with W, X, Y and Z caused by gates W, X, Y and Z, respectively. The logic equations for W, X, Y and Z are:

W = (NOFF1 + DRFF + A + B* + C* + CG*)*
X = (NOFF1 + DRFF + A* + B + C + CG*)*
Y = (NOFF1 + DRFF* + A* + B* + CG*)*
Z = (NOFF1 + DRFF* + A + B + CG*)*

If the data written were the regular pattern 0101..., the firing order of the W, X, Y and Z gates during decoding would be: X, Z, W, Y, X, Z, W... One and only one gate will fire for each transition of the DRFF.

If the data written were the regular pattern 001001..., the firing order of the W, X, Y and Z gates during decoding would be: W, Y, W, Y, W...

When all zeroes or all ones are written, none of W, X, Y or Z gates will fire once the initial state of the DRFF has been set.

Clock Derivation - The clock derivation for the Read Control consists of a clock divider FF-F1, and the read clock output gate F4B. FF-F1 is preset to the proper phase output by the RA* term. The RC output on pin -17 is operative as long as RA* is low and the timing chain FF No. 2 is set.

Bit-Level Error Check - The error detector examines the contents of the undecoded data storage register D3, D2 and D1 at every half-bit-time to determine whether the pattern 101 or 010 is present. These are invalid patterns which signify an error. Application Note 005 F-Series Bit-Level Error Detection presents an analysis which substantiates the detection of 50% of all possible read errors.

NOTE: * An asterisk is used in this manual to signify the logical inversion of a term, i.e., A* is the same as the more-conventional $\overline{A}$, read as not-A or A-not. As a general rule, an asterisk also signifies that the signal line is normally high and becomes low when active.

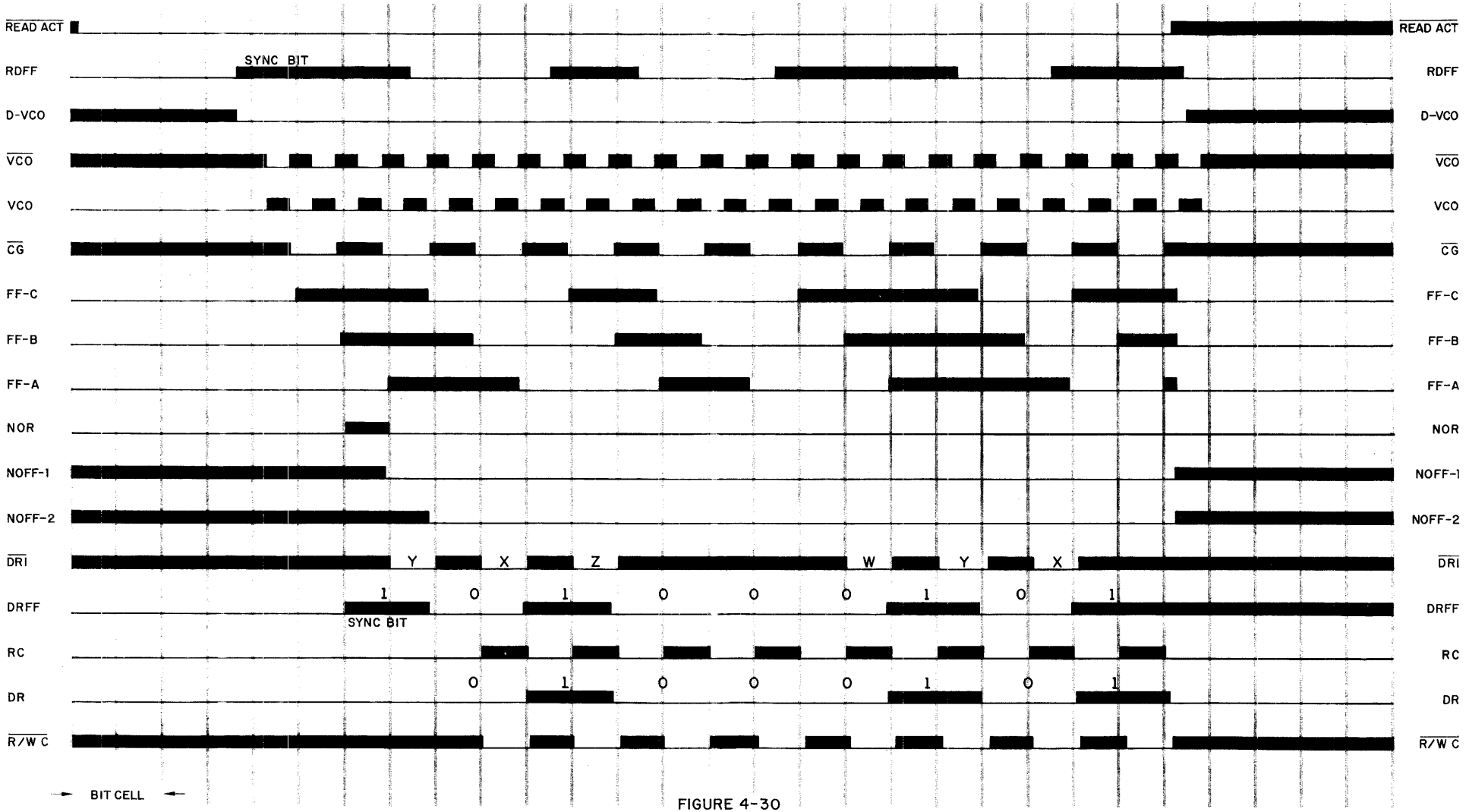
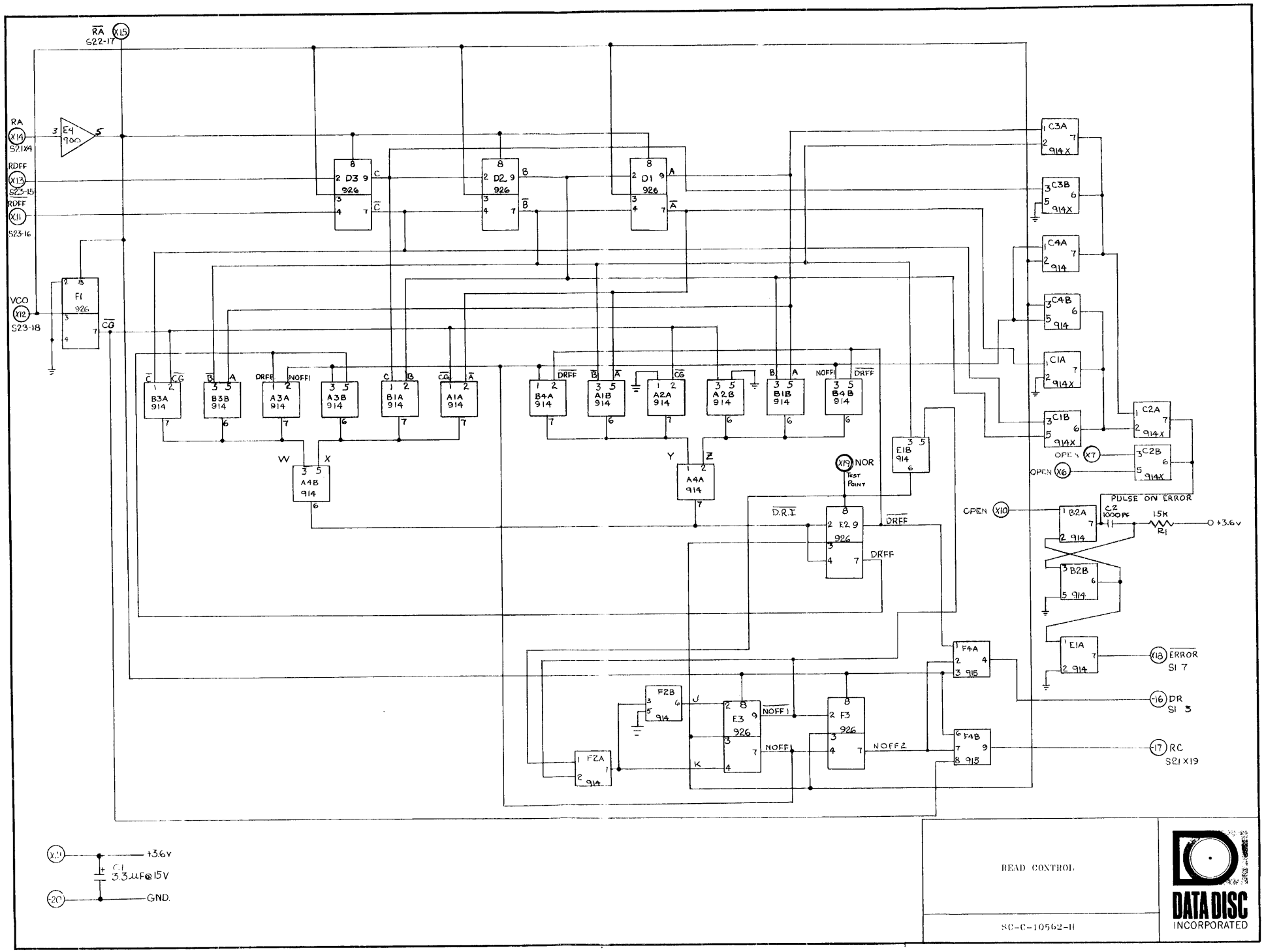
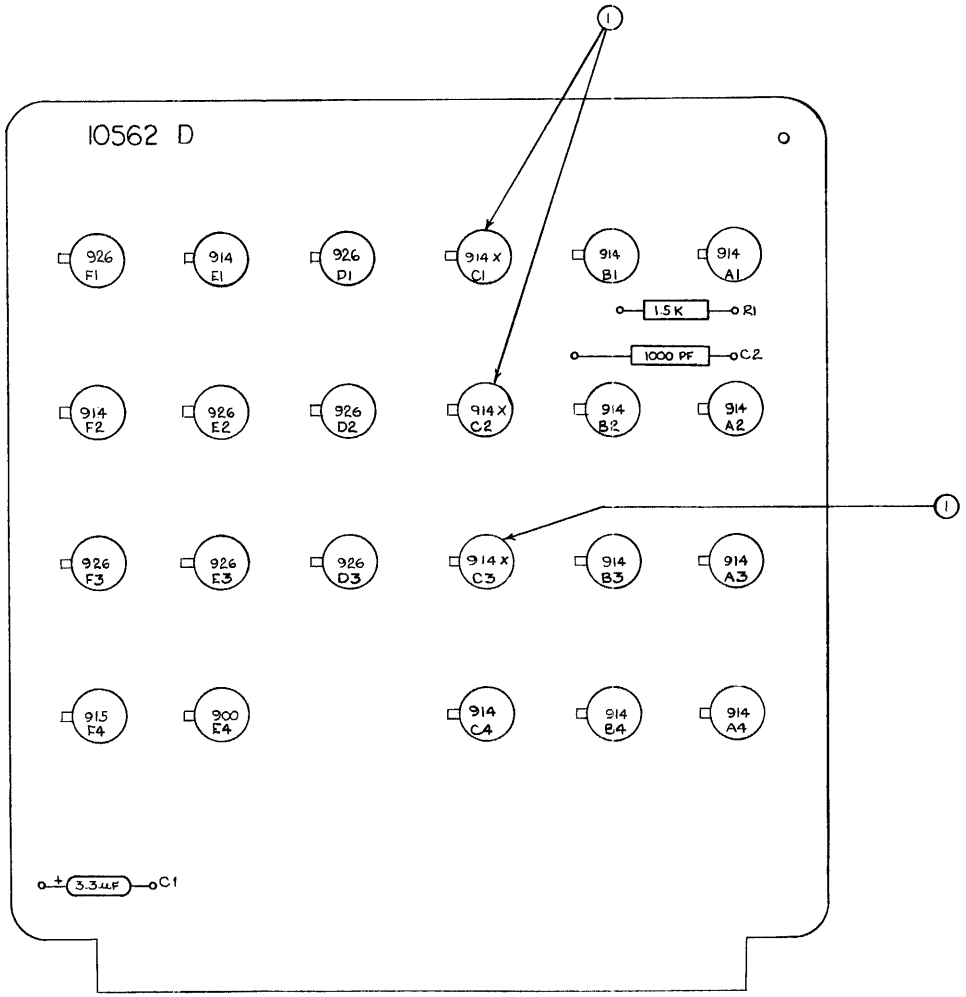


FIGURE 4-30
READ DATA TIMING DIAGRAM

This page purposely left blank.


READ CONTROL
SC-C-10562-H
DATA DISC INCORPORATED
RA
S22-17
RA
X14
S21X4
RDFF
X13
S23-15
RDFF
X11
S23-16
VCO
X12
S23-18
E4
900
F1
926
D3
D2
D1
926
B3A
B3B
A3A
A3B
B1A
A1A
B4A
A1B
A2A
A2B
B1B
B4B
914
A4B
A4A
E1B
X19
NOR
TEST POINT
D.R.I
E2
F2B
F2A
E3
F3
F4A
F4B
915
C3A
C3B
C4A
C4B
C1A
C1B
C2A
C2B
914X
914
OPEN
X7
X6
X10
B2A
B2B
E1A
PULSE ON ERROR
C2
1000 PF
1.5K
R1
+3.6v
X18
ERROR
SI 7
-16
DR
SI 3
-17
RC
S21 X19
X21
+3.6v
C1
3.3 µF @ 15V
-20
GND.



ITEM	COMP. DESIGNATION	QUAN	DESCRIPTION & MANUFACTURER	
10	SC 10562-H	1	SCHEMATIC DWG. DATA DISC# 10562-H	
9	EJECTOR	1	CARD EJECTOR # S202	SCANBE
8	10562-D	1	P.C. BOARD #10562-D	DATA DISC
7	C1	1	3.3 uF @ 15v CAPACITOR	KEMET
6	C2	1	1000 PF CAPACITOR	CENTRALAB
5	R1	1	1.5K 1/2 WATT 5% RESISTOR	CH
4	E4	1	900 MICROLOGIC CAN	FAIRCHILD
3	F4	1	915 MICROLOGIC CAN	FAIRCHILD
2	A1-A2-A3-B1-B3-B4-E1 C1-B2-C2-F2-C3-A4-C4	14	914 MICROLOGIC CANS	FAIRCHILD
1	D1-F1-D2-E2-D3-E3-F3	7	926 MICROLOGIC CANS	FAIRCHILD

NOTES:
1. ALL NUMERALS WITH "X" FOLLOWING, MEANS + VOLTAGE PIN, NOT CONNECTED

READ CONTROL

AD-C-10562-F

DATA DISC INCORPORATED

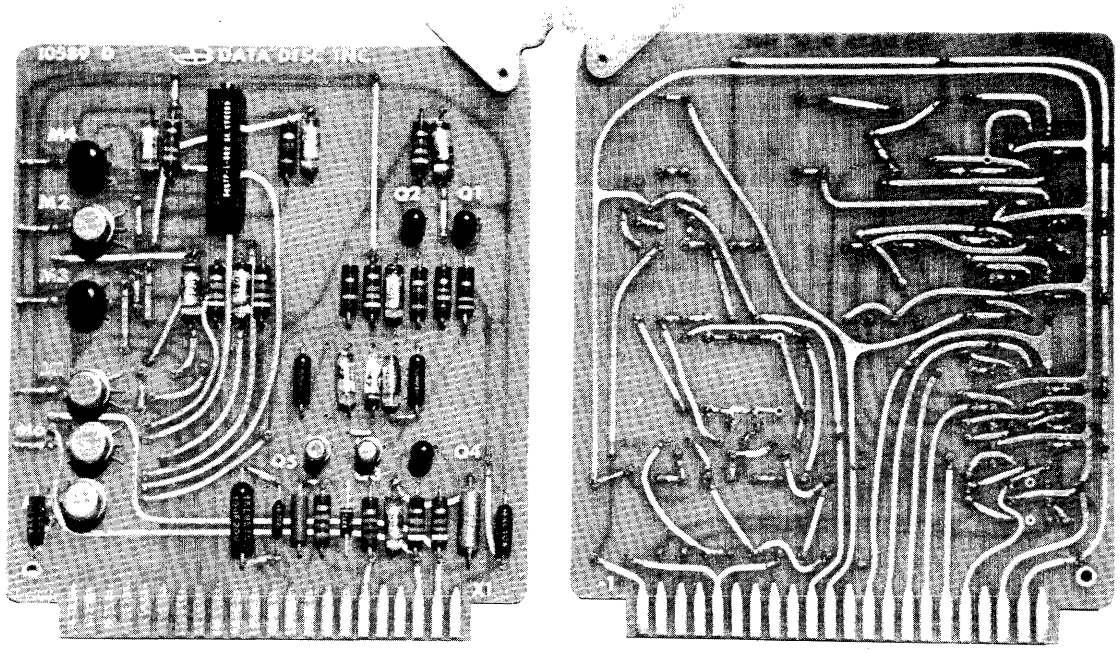


Figure 4-31 VCO and Control Card

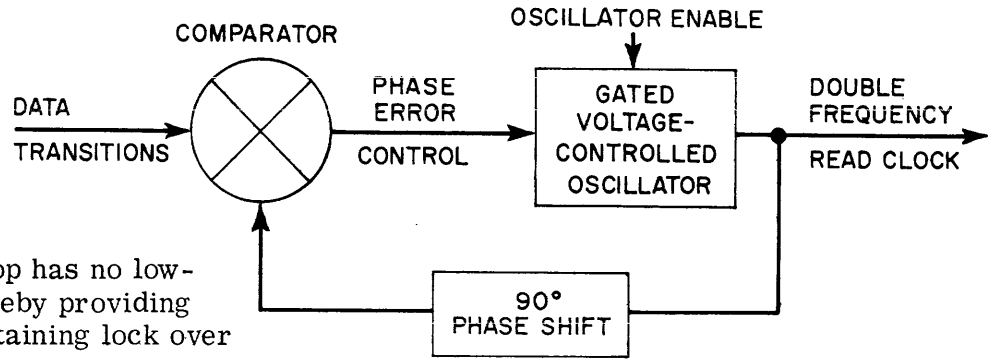
4.13 VCO & CONTROL (10589)

4.13.1 General Description

The Voltage-Controlled Oscillator (VCO) provides a clock which is derived from and is synchronous with the data which is read from the selected data track. In reading, a clock is developed in the correct phase relationship to the data. The VCO is started in phase with the data and continuous phase corrections are made to maintain phase-lock and to achieve frequency-lock. The card contains the VCO, a comparator circuit, and a circuit which provides the optimum phase relationship between the data and the derived clock. The card is located in the card cage at connector S23.

4.13.2 Functional Description

VCO Turn-On. The VCO is started in phase with the data, as shown in Figure 4-33, by the following sequence: with RA* pin -14 at ground and pins -15 and -17 (read-amplifier) at zero, occurrence of the sync pulse at pin -17 sets RDFF* low and RDFF high. The high output at pin -13 (RDFF) sets the D-VCO flip-flop M3A/M3B low at pin -11. This causes transistor Q1 to stop conducting and the VCO starts oscillating within one-half cycle of its natural frequency. The natural frequency of the VCO clock is twice the bit clock rate.



This phase-locked loop has no low-frequency filter, thereby providing fast lock-in and maintaining lock over a wide tracking range.

Figure 4-32 Wideband phase-locked loop

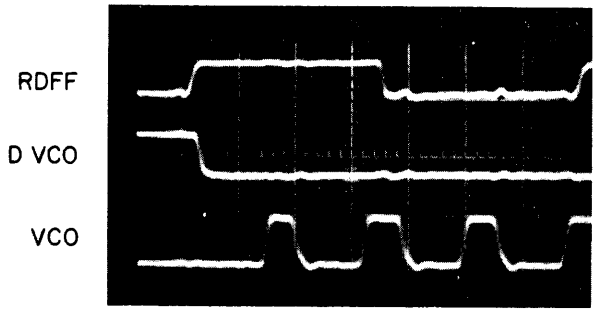


Figure 4-33 VCO Turn On

VCO Control. VCO* signal at pin -10 is inverted by M5, and is fed out at pin -18 as VCO and applied to the VCO inverter M6A. VCO output at pin -18 is used to clock the data, and is applied at pin X12 of the Read Control Card, S20. The VCO (2)* signal at pin X3 is used as an input to the comparator section (R7, R8 and Q4) of the VCO. The comparator compares the output of the Data One Shot from M6B DATA O. S. (2)* with the VCO output from M6A on a bit-by-bit basis, shifting the VCO frequency to maintain its output in phase with the Data One-Shot. The shift of frequency is accomplished by pulse-width modulation of the VCO control voltage to cause instantaneous deviation of the VCO frequency in an attempt to maintain the VCO output transitions 90^{o} out of phase with the data transitions. As shown in Figure 4-34, the DATA O. S. (2)* negative-going transitions are ideally centered in the zero-volt level of the VCO (2)* signal. Q4 is therefore normally ON and is turned OFF only when both comparator inputs are low.

The 20pf capacitor C9 across Q4 in the comparator provides noise filtering in this wide-band phase-locked loop.

The emitter-coupled multivibrator formed by transistors Q3 and Q5 operates at a frequency set by capacitors C12 through C15 and resistors R14 and R16 in the emitters. When transistor Q4 is ON and Q5 is ON, a low-impedance current path is established from the collector of Q5 through R15 and Q4 to ground. The operating threshold point for Q3 to turn ON is thus shifted proportionally with the duty cycle of Q4. When Q4 is OFF and Q5 is ON, a high-frequency path through C9 is provided. When Q1 turns ON, the multivibrator is turned OFF. A positive signal at pin -11 disables the VCO. The signal from the collector of Q3 is converted by Q2 to the 3. 6-volt level required by M5.

A Zener supply, R18 and CR3, is used to render the entire circuit insensitive to fluctuations in the 20-volt power supply. The operating voltage on the base of Q5 is maintained by the Zener supply R17 and CR2 with additional filtering of high frequency variations furnished by C10.

Data pulses from the read-amplifier at pins -15 and -17 are differentiated by the capacitors C4 and C5 in each line, and OR'd at the input to M2A, the delay one-shot multivibrator. C11 is factory-selected, and the 5K-ohm potentiometer is adjusted, to provide the optimum phase relationship between the data and the derived clock.

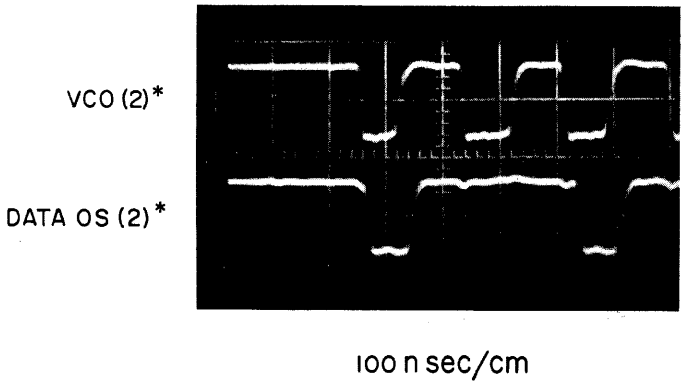


Figure 4-34 VCO Comparator Inputs

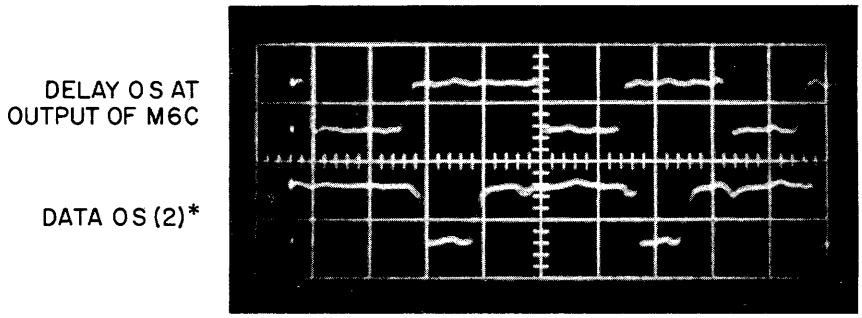


Figure 4-35 VCO Control One-Shots

The pulse from the delay one-shot M2A/M2B is inverted by M6C and applied to M4A/M4B, a strobe one-shot. The output of the strobe one-shot is inverted by M6B and is available at pin X2, the DATA O. S. (2)* output. Resistor R19 is factory-selected for proper width of the strobe. The photo shows the time duration of these one-shots in a correctly adjusted system.

M1A/M1B are two NOR gates used as a Reset /Set flip-flop. M1A restores the pulse outputs of the read-amplifier to a dc level binary signal and applies it to the decoder in the Read Control through pins -13 and -16. The D-VCO signal is positive when flip-flop M3A/ M3B is reset by a positive RA* signal on pin -14.

4. 13. 3 VCO Adjustment Procedure (R3)

The frequency-determining elements are factory adjusted, and are not to be altered in the field. The VCO's free-running frequency may be roughly checked by grounding TP X6 and TP -11. By using this method which does not simulate actual conditions, properly operating VCO's should produce frequencies from 6. 0 to 6. 5 MHz.

The following procedure describes how to adjust potentiometer R3 in the delay one-shot to generate the correct phase relationship between clock and data pulses.

a. Select a track with data written on it by applying a +3. 6v signal to the proper X and Y select lines.

b. Select a continuous read operation by grounding the Read* (R*) line.

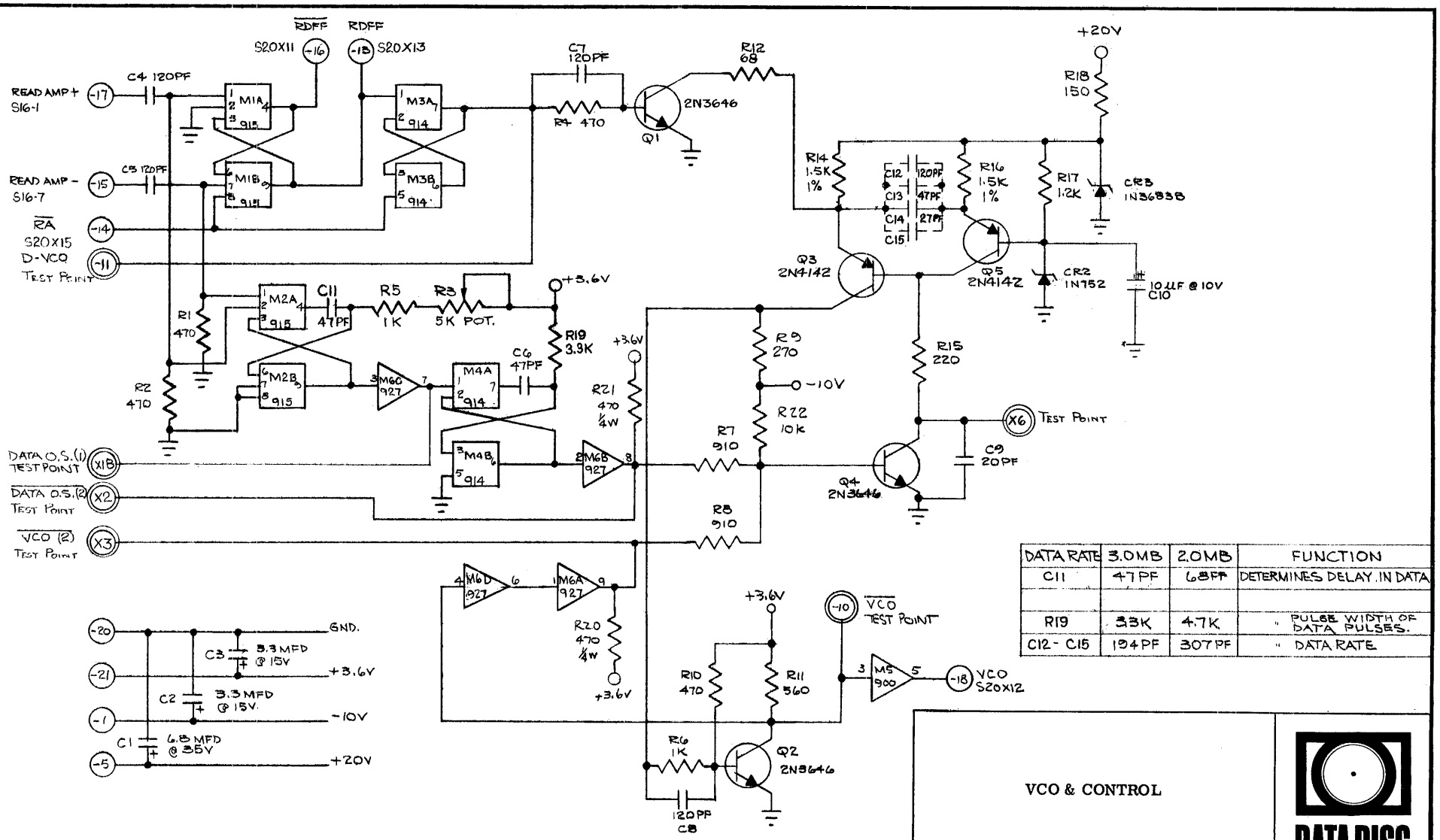
c. Turn potentiometer R3 fully counterclockwise (CCW) and monitor the Error (E*) line with an oscilloscope.

d. Slowly turn R3 clockwise (CW) until the E* pulses just disappear and then count the number of CW turns until the pulses appear again.

NOTE: When the E* pulses disappear, it may be helpful to put the scope in the "single-sweep" trigger mode. It should take 5 to 10 turns of R3 to cover the area without E* pulses.

e. Adjust R3 to the midpoint of the area without E* pulses by turning R3 CCW one-half the number of turns counted in Step (d). This is the best setting.

This page purposely left blank.



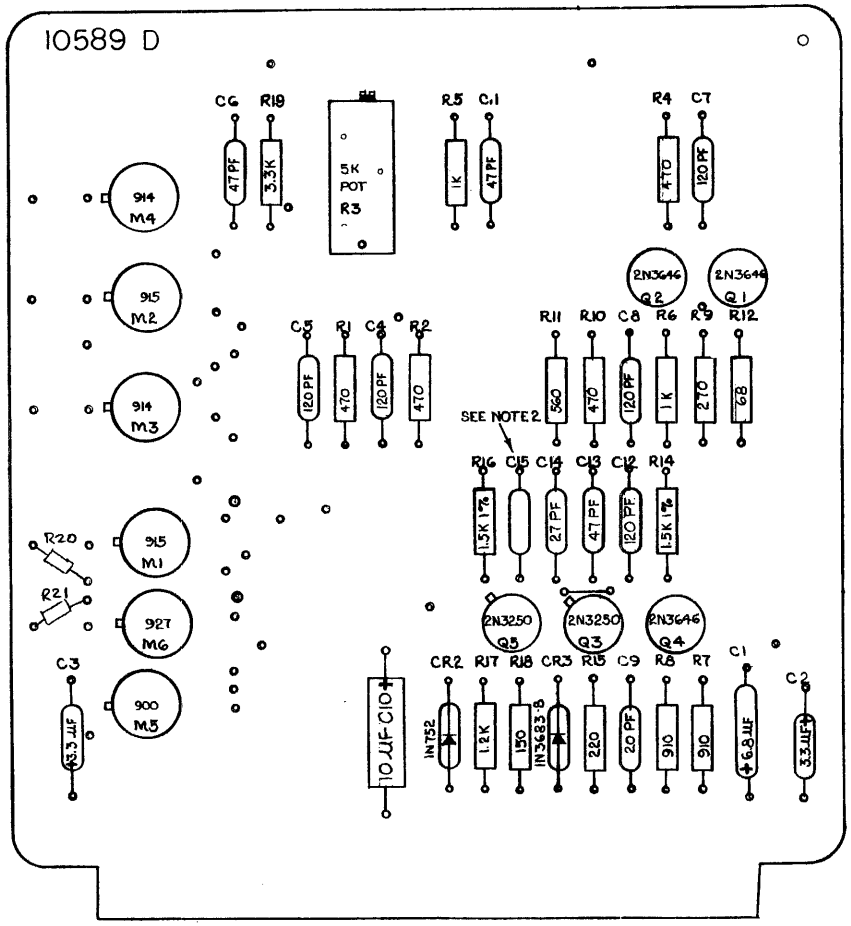
DATA RATE	3.0MB	2.0MB	FUNCTION
C11	47 PF	68PF	DETERMINES DELAY IN DATA
R19	3.3K	4.7K	" PULSE WIDTH OF DATA PULSES.
C12 - C15	194 PF	307 PF	" DATA RATE.

UNLESS OTHERWISE SPECIFIED; ALL RESISTORS IN OHMS ± 5%; ½ WATT.
LAST NUMBERS USED M6, Q5, CR3, R22, C15

VCO & CONTROL

SC-B-10589-G

DATA DISC INCORPORATED



ITEM	COMP. DESIG.	QUAN.	DESCRIPTION & MANUFACTURER	
32	EJECTOR	1.	CARD EJECTOR - # 9202	SCANBE
31	C9	1	20 PF CAPACITOR	CENTRA-LAB
30	10589-D	1	PRINTED CIRCUIT BOARD DATA DISC # 10589-D	
29	M5	1	900 MICROLOGIC CAN	FAIRCHILD
28	M3-M4	2	914 MICROLOGIC CAN	FAIRCHILD
27	M1-M2	2	915 MICROLOGIC CAN	FAIRCHILD
26	M6	1	927 MICROLOGIC CAN	FAIRCHILD
25	Q3-Q5	2	2N3250 TRANSISTOR	FAIRCHILD
24	10589 E	1	SCHEMATIC DWG. DATA DISC #	10589-E
23	Q1-Q2-Q4	3	2N3646 TRANSISTOR	FAIRCHILD
22	CR2	1	IN752 DIODE	MOTOROLA
21	CR3	1	IN3683-B DIODE	MOTOROLA
20	R20, R21	2	470 1/4 WATT 5% RESISTOR	GH
19	R3	1	5K POTENTIOMETER	BOURNS
18	C2-C3	2	3.3 µF @ 15 V CAPACITOR	KEMET
17	C1	1	6.8 µF @ 35V CAPACITOR	SPRAGUE
16	C6-C11-C13	2	47 PF CAPACITOR	CENTRA LAB
15	C4-C5-C7-C8-C12	4	120 PF CAPACITOR	CENTRA LAB
14	R14-R16	2	1.5K 1/2 WATT 1% RESISTOR	MEPCO
13	R12	1	68 1/2 WATT 5% RESISTOR	GH
12	R18	1	150 1/2 WATT 5% RESISTOR	GH
11	R15	1	220! 1/2 WATT 5% RESISTOR	GH
10	R9	1	270 1/2 WATT 5% RESISTOR	GH
9	R1-R2-R4-R10	4	470 1/2 WATT 5% RESISTOR	GH
8	R11	1	560 1/2 WATT 5% RESISTOR	GH
7	R7-R8	2	910 1/2 WATT 5% RESISTOR	GH
6	R5-R6	2	1.0K 1/2 WATT 5% RESISTOR	GH
5	R17	1	1.2K 1/2 WATT 5% RESISTOR	GH
4	C14	1	27 PF CAPACITOR	CENTRA-LAB
3		1	JUMPER # 26 WIRE	
2	C10	1	10 µF @ 20V CAPACITOR	KEMET
1	R19	1	3.3K 1/2 WATT 5% RESISTOR	GH

VCO & CONTROL

AD-C-10589-E

DATA DISC INCORPORATED

Appendix
Documentation Standards

1.1 Component Designation

Accepted industrial symbols are used for all conventional components. Three simple outlines shown in Figure A-1 are used for logic element symbols. The three-digit number within an outline designates the three digits from the Fairchild Industrial Micrologic part code. Example: A 926 JK Flip Flop corresponds to Fairchild Code UX 5992629X (digits underlined for clarity).

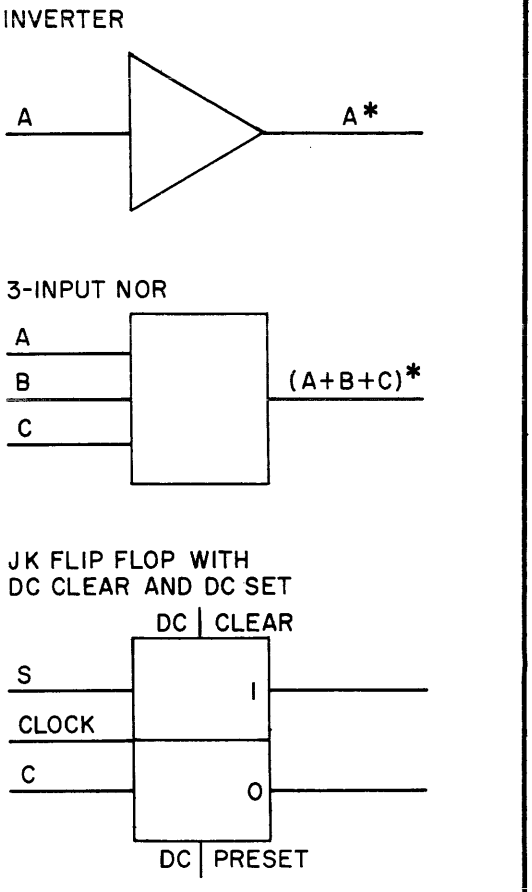


FIGURE A-1
LOGIC ELEMENT SYMBOLS

Micrologic input and output pins are numbered in accordance with the manufacturer's standard. Viewed from the top, pins are numbered counter-clockwise starting at the first pin to the left of the tab on the element. (Fig. A-2)

Each card has its own sequence of component numbers starting at 1 for each type of component. The usual prefixes R, C, CR, Q and L are used. Example: resistor 1 is R1.

The alpha-numeric symbol within a logic-element outline is its component number. The symbol also provides positional information. For example, logic element D4A is the micrologic element in column D, row 4 on the card, and is part A of a multiple-part element. Single micrologic elements, such as 926 JK Flip Flops, have a designation such as B3. Logic elements with an M as the first letter are located on boards containing primarily discrete components. M numbers are used as micrologic component numbers and give no positional information.

1.2 Connector Numbering

Double-sided printed-circuit cards with two-sided printed-circuit connectors are used throughout the F Series Unit. Each side of the printed-circuit cards has 22 gold-plated contact tabs. Pins on the component side of the board are numbered X1 to X22 starting at the board ejector edge; pins on the back side are numbered -1 to -22 starting at the ejector edge of the board. A 44-pin AMP connector with insertable pins provides connection to the intercard wiring. Small numbers and letters impressed in the plastic connector are NOT used. Every fifth pin is marked on the connector body to aid in locating pins. Assignment of "S" (socket) numbers to the connectors is shown on Drawing 10651 and Figure 3-3.

1.3 Interconnecting Wires

The interconnection drawing 10651, supplies all interconnection information for the various cards and the I/O connectors. As an additional aid, schematics have notations written near the card pin number circle to provide most intercard connection information. For example: S21X7 or S17-15 written next to a pin number circle means the pin is wired to socket 21, pin X7 or to socket 17, pin -15.

2.1 Abbreviations Used in This Manual

The following abbreviations appear on drawings or in the text of this manual to designate functions or signals:

ATC - Automatic Threshold Control
CG - Clock Gate
CT - Clock Track
DR - Data Read
DRI - Data Read Input
DW - Data Write
ED - Encoded Data
EOW - End of Write
ES - Encoder Sync
FF - Flip-Flop
HC - Head Change
IP - Input
NRZ - Non-Return to Zero
R - Read
RA - Read Act
RC - Read Clock
RI - Read Inhibit
R/W - Read/Write
RWC - Read/Write Clock
S/T - Schmitt Trigger
VCO - Voltage-Controlled Oscillator
W - Write
WA - Write Act
WC - Write Clock
WD - Write Data
WE - Write Enable
WTO - Write Turn-On
1-G - 1-Gate (One-Gate)
0-G - 0-Gate (Zero-Gate)
1-P - 1-Pulse (One-Pulse)
0-P - 0-Pulse (Zero-Pulse)

An asterisk is used in this manual to signify the logical inversion of a term. i. e., A is the same as the more conventional $\overline{A}$, read as not-A or A-not. As a general rule, an asterisk also signifies that the signal line is normally high and becomes low when active.

The following abbreviations are used to designate components:

C - capacitor
CR - diode
L - inductor
M - micrologic unit
Q - transistor
R - resistor

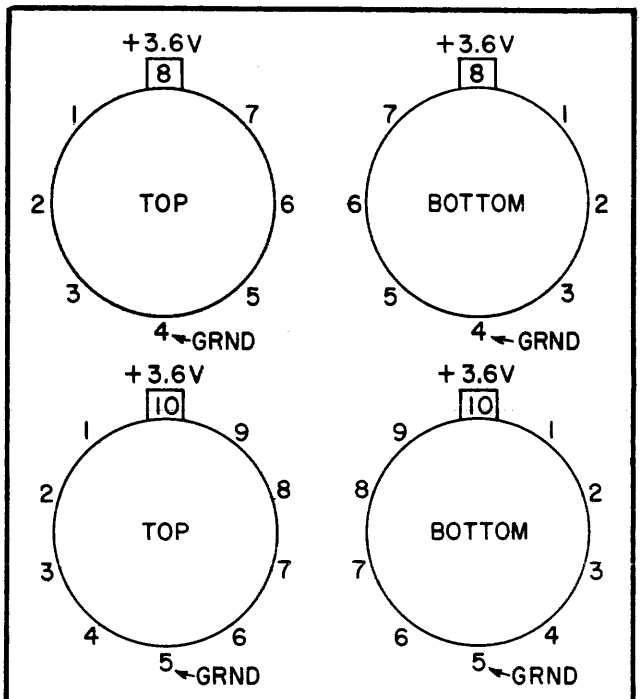


FIGURE A-2
MICROLOGIC PIN-NUMBERING CONVENTIONS

DATA DISC, INC. • 1275 California Ave. • Palo Alto, California 94304 • (415) 326-7602