DATA TRANSLATION INC
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ENGINEERING SPECIFICATION

MODEL DT1761/62/63/64 SERIES

DATAX ANALOG I/O INTERFACE

BOARD FOR DIGITAL EQUIPMENT CORP.

LSI-11 MICROCOMPUTERS

Data Translation, Inc. (DTI) has prepared this guide for use by DTI personnel and customers as an explanation to the proper use, operation and calibration of DTI DATAX equipment. The drawings and specifications contained herein are the property of DTI and shall neither be reproduced in whole or in part without DTI prior written approval nor be implied to grant any license to make, use, or sell DATAX equipment manufactured in accordance herewith.

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USER NOTE FOR DT1761 & DT1762

The manual for the DT1761 and the DT1762 is the same. Therefore, all references made in the manual to the DT1761 apply also to the DT1762, accept that all references to Analog output given in the manual do not apply to the DT1762.

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User Note for Operation of any DT1761 series
Analog I/O Systems with DMA option.

The LSI-11 board must have installed ECO #10 from DEC. This ECO corrects a number of problems on the LSI-11 associated with DMA operation.

ENGINEERING SPECIFICATION

1.0 General

The DT1761 is a complete ANALOG I/O system plug compatable with the DEC LSI-11 series microcomputer. The system consists of 16 channels (8 differential) and two channels of 12 bit D/A outputs plus scope control logic. The analog input front end also includes a sample and hold amplifier and a 12-bit A/D converter. Available acquisition times are 10, 20 and 40 USEC.

2.0 Analog Input Specification

The DT1761 utilizes standard data acquisition modules manufactured by Data Translation, Inc. The standard unit utilizing the DT5701 contains input multiplexer, a high input impedance instrumentation amplifier, sample and hold and 12-bit A/D converter. An optional switch gain amplifier is available with ranges of 1, 2, 4, 8.

2.1 Multiplexer

The multiplexer consists of C-MOS switches and is available as 16 channels in the single ended configuration. In the differential configuration 8 channels are available.

2.1.1 Input Protection

Multiplexer is guaranteed to break-before-make on new channel selection. Overvoltage protection is also included on the MUX inputs. In the event of an overvoltage, current limiting on the multiplexer input occurs. Thus the protection is non-destructive. Inputs are protected to $\pm$ 35 volts.

2.1.2 Configuration

The input multiplexer can be configurated up to 16 channels single ended or 8 differential.

2.1.3 Input Impedence

100 Mohm in "off" or "on" position of multiplexer

2.2 Analog Input Specifications

Resolution - 12 bits unipolar or offset binary
11 bits + sign (2's complement) bipolar

2.2.2 Linearity - $\pm$ ½ LSB

2.2.3 Inherent Quantizing Error - $\pm$ ½ LSB

2.3 System Parameters

The analog input system consists of MUX, differential amp. S+H and A/D converter.

2.3.1 Accuracy $\pm$ 0.03% FSR

(FSR = full scale range, i.e. for a $\pm$ 10V range the full scale range is 20V

2.3.2 Stability - Temp. Co. = $\pm$ 25 ppm/^{o}C FSR

2.3.3 Throughput

The standard DT1761 has a throughput specification of 25KHz. Throughputs of 50KHz and 100KHz are available utilizing the DT5720 and DT5710 respectively.

2.4 Connection of Analog Signals

Analog signal connection is via the top connector on the DT1761. This connector is a 50 pin 3M type connector Part #3433.

3.0 Analog Output Specifications

The DT1761 utilizes a standard DATAX D/A module to implement Analog Output. The DT212 Point Plotter and Dual D/A Converter contains Z axis control, selectable set up delay, timing functions, x and y axis D/A converter with power amplifier output, and mode control.

3.1 Resolution - 12 Bits

3.2 Linearity - ±½ LSB

3.3 Range - ± 10V, 0 → 10 V; @ 25 ma minimum current output, all jumper selectable.

3.4 Relative Accuracy - ±0.025%

3.5 Full Scale Settling - 0.1% - 1 usec, 0.01% - 3usec; into 50ft coaxial cable terminated with 470 ohm

3.6 Temperature Coefficient - 25 ppm/^{o}C

3.7 Z Axis Control

The DT1761 contains all the control circuitry for Z axis and scope control mode bits.

3.7.1 Z Output (Intensity) - LO (0.8V) to HI (2.4V) TTL compatible into 50 ohm termination

3.7.1.1 Z Risetime - 100 nsec into 50 ft of COAXterminated

3.7.1.2 Z Pulse Width - Jumper Selectable

a. 0.5 usec
b. 5 usec
c. external R.C. 1 usec to 0.5 msec

3.8 Mode Bits

Four mode bits are provided and can be used for various control parameters. For example; store, non-store, cursor, and erase are typical functions required when dealing with a storage scope. The mode bits are Lo true and can drive up to 10 TTL loads.

4.0 PROGRAMMING

Data Translation interfaces are designed to meet the requirements of standard DEC interfaces. As such they are structured around a Control & Status register for complete program control of the interface. DMA operation is also available to provide high throughput and low software overhead.

4.1 Modes of Operation - The DT1761 can operate in a number of operating modes, as follows.

4.1.1 Program I/O - In this mode standard LSI-11 instructions can access and control the A/D and D/A components on the interface. Start A/D conversion can be accomplished by the following means:

1. LOAD MUX ADDR in ADCSR
2. Set A/D START (BIT0) in ADCSR
3. Enable external triggers or Real Time clock inputs in ADCSR.

The D/A can be updated by accessing the DACDBR D/A converter data buffer register.

4.1.2 Interrupt Operation - In many real time applications the program does not want to dedicate itself to taking analog measurements. Then the Interrupt on A/D done bit is utilized. In this case an interrupt is produced on either A/D done or Error. (See Error bit description in the ADCSR.)

4.1.3 DMA (Direct Memory Access) - The DT1761 has as an option the capability to provide data transfers directly to LSI-11 memory. Transfers are only on A/D data to memory. All set up of channel or trigger select should be done via standard Programmed I/O transfers. The user will set up a word count and memory address on the interface. Then choose a trigger mode in the ADCSR i.e., External or RTC. If no trigger mode is selected the A/D will run at its own highest throughput. As soon as data is taken from ADDBR a new conversion is initiated and another NPR cycle requested.

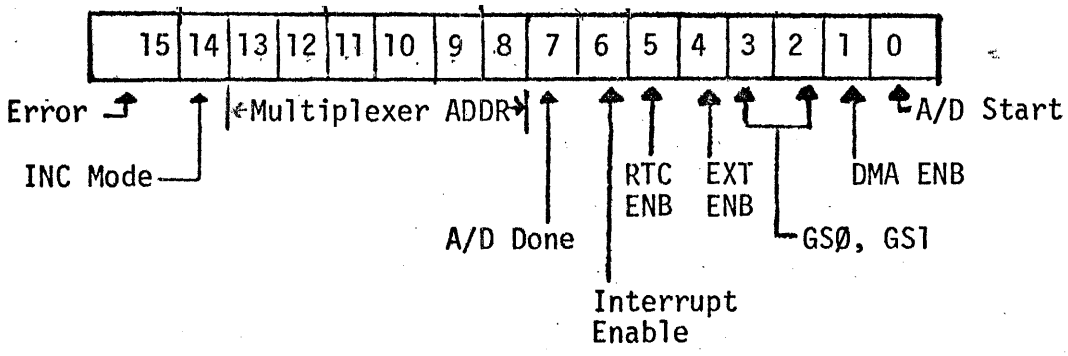
4.2 Device Address - The DT1761 device address is selectable via a dip switch. Device address may be assigned between 170000_8 and 177774_8.

The order of address is as follows, once a base address has been set in the switch:

A/D Control and Status Register (ADCSR) - Base
A/D Data Buffer Register (ADDBR) - Base + 2 (Read Only)
D/A Data Buffer Register (DADBR) - Base + 2 (Write Only)
DMA Word Count Register (DMWCR) - Base + 4
DMA Current Address Register (DMCAR) - Base + 6

4.3 Interrupt Vector Address - The vector address is also set by a dip switch pack. They are selectable in increments of 10_8. The A/D done and Error interrupts will produce the same interrupt vector. The DMA end of range condition will produce a vector which is four locations higher.

4.4 Control and Status Register



4.4.1 Programming the DT1760 Series

Programming of the DT1760 is straight forward. However, there are certain sequences of instructions that should be followed to properly utilize the various operational modes.

Programmed I/O

All program I/O operation of the A/D converter is controlled in the Control and Status Register (ADCSR). This register is byte addressable. A start conversion is accomplished in a variety of ways as follows:

A. Setting Bit ØØ A/D start of ADCSR

B. Loading Mux channel address (upper byte)

C. RTC IN or EXT Trig IN when enabled.

Sequential Mode Operation

The DT1760 series will automatically increment through the Mux when Bit 14 INC Mode is set in the ADCSR. However, since the INC Mode bit is located in the upper byte of the ADCSR a start conversion is initiated when the bit is set. Thus, the programming sequence for INC Mode is as follows:

```
MOV #40000,@ #ADCSR :    Set INC mode + start conversion on
                         Channel 1.

A  TST B @ #ADCSR :      Test A/D Done
   BMI B
   JMP A

B  MOV @ #ADDBR, (R) +: Store Data
   INC @ #ADCSR:        Start next conversion and INC. Channel
   JMP A
```

This program will increment through all A/D channels and store the data into memory. It should be noted that the initial instruction which sets the INC Mode bit also contains a channel address. The address that is loaded is one less than the channel the conversion is taken on. Thus if it is required to start on channel 3, channel address 2 should be loaded with Bit 14 the INC Mode bit.

Interrupt Operation

The DT1760 series interface modules provide an interrupt to the LSI-11 processor if the Interrupt Enable, bit 6, ADCSR is set. The condition for interrupt is A/D done bit 7, ADCSR is set. Thus, for every A/D done an interrupt will occur. The module provides a vector address which is completely dip-switch selectable.

DMA Operation

A unique option for the DT1760 series interfaces is the DMA or Direct Memory Access option. Programming for this option requires proper sequencing but it is very straight forward.

Initiating Conversions under DMA

Conversions can be initiated a variety of ways in DMA mode as follows:

1. Normal operation is that every time the A/D done flag is set a DMA request is made. When the interface becomes master and sends the data to memory the A/D done flag is reset. Upon reset, the next conversion is initiated. Thus the data rate is dependent upon the speed of the Data Acquistion Module and the time required to do the transfer.

2. If the RTC or EXT Trig enable bits are set conversions will be initiated from these sources. Operation will follow the same as explained in the preceeding section.

3. Increment Mode - Whether conversions are run as in normal operation or externally the Increment Mode can be utilized. This mode must be set up before DMA operation is enabled.

Note: Due to the restriction of the LSI-11 refresh memory. This device is not designed to hog the bus. The DT1760 series interfaces relinquish bus mastership after each transfer thus allowing LSI-11 memory refresh to occur.

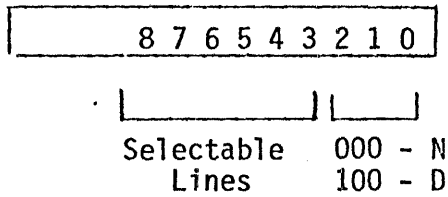
The Operation of DMA is as follows

1. Load Word Count Register with the complement of the number of words to be transferred.

2. Load the address register with the starting memory address of the block.

3. Load the ADCSR with the DMA Enable bit and the A/D start bit.

4. When transfer is complete an interrupt will occur. The vector for this interrupt is the selected vector for the module + 4.



5. This interrupt is automatically cleared by the interface so the user software need not worry about clearing it out.

A programming example is as follows:

```
MOV # WC, @ #DMWCR :      Set up word count

MOV #ADR, @ #DMCAR:       Set up current address

MOV #3 @ #ADCSR:          Set DMA ENB and A/D Start.

WAIT:                     Wait for EOR Interrupt after block
                          has been transferred.
```

4.4.2. Programming the DT1762 with the calibration and test routine:

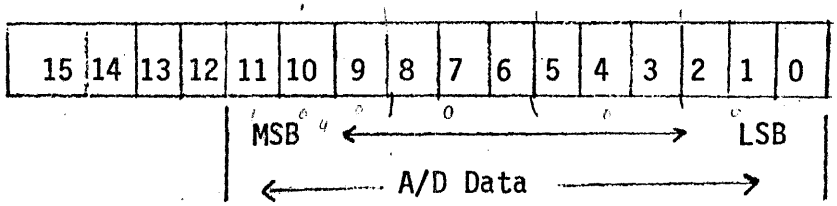
In order to provide a channel scan for all channels on the DT1762 a constant should be changed in the calibration and test routine. This constant will allow a channel scan routine to scan all of the channels implimented. The constant is located at location 1426 octal. The constant should be set for the number of channels in octal. required for the scan. For example, if there are 32 channels the number 40 octal should be set in that location.

CSR BIT DESCRIPTIONS: Note: All bits cleared by processor INITIALIZE

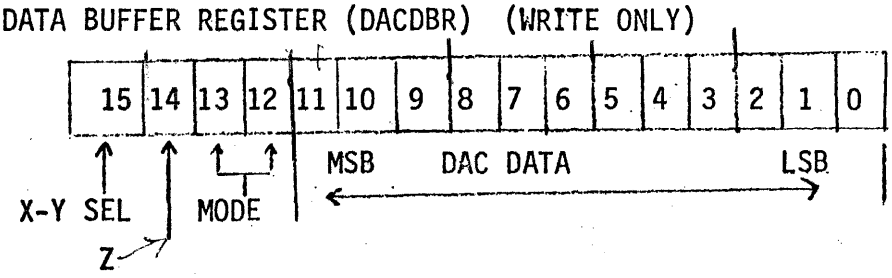
BIT #	NAME	DESCRIPTION
15	ERROR	READ/WRITE - Indicates an error condition with following parameter: 1. Attempting an external start or clock start during MUX settling. 2. Attempting a start while conversion in process. 3. Doing a read data during A/D busy.
14	INC MODE	READ/WRITE - When set the MUX channel address will increment on every start convert.
13 - 8	MULTIPLEXER ADDRESS	READ/WRITE - Six MUX channel address bits for addressing up to 64 channels.
7	A/D DONE	READ ONLY - Set by end of conversion reset by read A/D data.
6	INTERRUPT	READ/WRITE - When set will enable interrupts from A/D done or A/D error bits
5	RTC ENB	READ/WRITE - Real time clock enable when set this bit allows start conversion from the real time clock.
4	EXTTRIG ENB	READ/WRITE - When set this bit allows start conversion from an external trigger source.
3 - 2	GAIN SELECT	READ/WRITE - These bits provide the gain select information BIT 3 (GS1) | 2 (GSØ) | GAIN 0 | 0 | 1 0 | 1 | 2 1 | 0 | 4 1 | 1 | 8
1	DMA ENB	READ/WRITE - This bit when set allows the transfer of data via direct memory access.
Ø	A/D START	READ/WRITE - Initiates a conversion when set cleared by end of conversion signal.

4.5 A/D DATA BUFFER REGISTER (ADDBR) (READ ONLY)

This location contains the A/D data format is as follows:



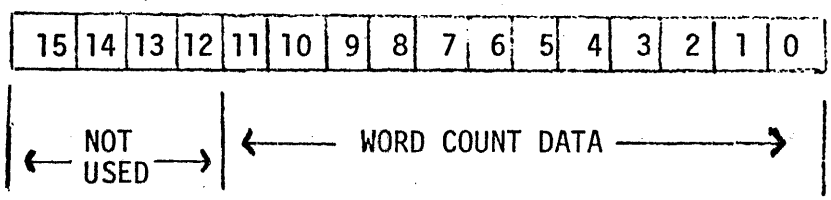
4.6 DAC DATA BUFFER REGISTER (DACDBR) (WRITE ONLY)



BIT #	NAME	DESCRIPTIONS
15	X/Y SEL	WRITE - When set this bit selects X-DAC, when reset selects Y DAC.
14	$\overline{Z}$	WRITE - When set will cause Z output.
13 - 12	MODE	WRITE - These bits are decoded to produce four DAC mode bits for erase as digital control points.
11 - 0	DAC DATA	WRITE ONLY - 12 bits DAC data.

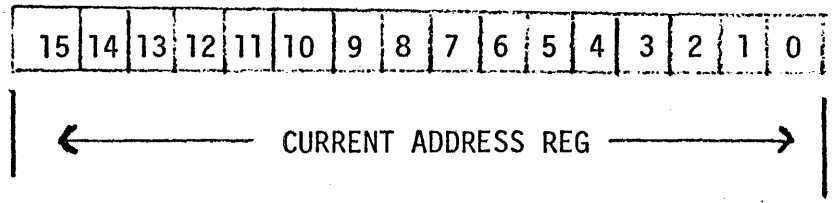
4.7 DMA REGISTERS

4.7.1 DMA WORD COUNT (DMWCR)



The word count register is a 12 bit counter/register which determines the number of transfers that will occur. The register is loaded with the two's compliment of the desired word count. An interrupt is generated on overflow signifying the end of range in data transfers.

4.7.2 DMA CURRENT ADDRESS REGISTER (DMCAR)



The current address register is used to supply the actual memory location where data is transferred. This register is incremented after each transfer.

5.0 External Trigger and Real Time Clock Inputs

There are two external inputs brought out to the user connections. One is utilized for external trigger inputs, the other for real time clock input. In normal mode this input switches the sample and hold to hold mode directly. Thus, the user must allow ample time for the input to be settled if a new channel is selected. These inputs can also be run in increment mode. That is, the channels will be incremented on every trigger pulse.

5.1 Electrical Characteristics

The External Trigger and Real Time Clock Inputs are TTL compatible and present one unit load.

6.0 Mechanical

The DT1761 is contained on a single quad size PC Board for LSI-11 compatibility.

7.0 Power Requirements

The DT1761 contains an on card DC-DC connector for generation of all analog voltages, thus, +5V @ 2A MAX is all that is required.

APPENDIX A

USER CONNECTION SUMMARY

PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	CH Ø	26	A GND
2	A GND	27	CH14/RET6
3	CH8/RETØ	28	A GND
4	A GND	29	CH7
5	CH 1	30	A GND
6	A GND	31	CH15/RET7
7	CH9/RET1	32	A GND
8	A GND	33	YDAC OUT
9	1 CH2	34	A GND
10	A GND	35	XDAC OUT
11	CH10/RET2	36	A GND
12	A GND	37	RTC IN
13	CH3	38	D GND
14	A GND	39	EXT TRIG IN
15	CH11/RET3	40	D GND
16	A GND	41	Z OUT
17	CH4	42	D GND
18	A GND	43	DAC MDO
19	CH12/RET4	44	D GND
20	A GND	45	DACMD1
21	CH5	46	D GND
22	A GND	47	DACMD2
23	CH13/RET5	48	D GND
24	A GND	49	DACMD3
25	CH6	50	D GND

DT1762 Analog Input System - User Connections

Differential Input Configuration

CONNECTOR J1				CONNECTOR J2			
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	CHØ	26	A. GND	1	RET8	26	CH20
2	A. GND	27	RET6	2	CH8	27	RET21
3	RETØ	28	A. GND	3	RET9	28	CH21
4	A. GND	29	CH7	4	CH9	29	RET22
5	CH1	30	A. GND	5	RET10	30	CH22
6	A. GND	31	RET7	6	CH10	31	RET23
7	RET1	32	A. GND	7	RET11	32	CH23
8	A. GND			8	CH11	33	RET24
9	CH2			9	RET12	34	CH24
10	A. GND	37	RTC IN	10	CH12	35	RET25
11	RET2	38	D. GND	11	RET13	36	CH25
12	A. GND	39	EXT TRIG IN	12	CH13	37	RET26
13	CH3	40	D. GND	13	RET14	38	CH26
14	A. GND			14	CH14	39	RET27
15	RET3			15	RET15	40	CH27
16	A. GND			16	CH15	41	RET28
17	CH4			17	RET16	42	CH28
18	A. GND			18	CH16	43	RET29
19	RET4			19	RET17	44	CH29
20	A. GND			20	CH17	45	RET30
21	CH5			21	RET18	46	CH30
22	A. GND			22	CH18	47	RET31
23	RET5			23	RET19	48	CH31
24	A. GND			24	CH19	49	A. GND
25	CH6	50		25	RET20	50	A. GND

DT1762 Analog Input System - User Connections

Single-Ended Connections

CONNECTOR J1				CONNECTOR J2			
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGN
1	CHØ	26	A. GND	1	CH24	26	CH36
2	A. GND	27	CH14	2	CH16	27	CH45
3	CH8	28	A. GND	3	CH25	28	CH37
4	A. GND	29	CH7	4	CH17	29	CH46
5	CH1	30	A. GND	5	CH26	30	CH38
6	A. GND	31	CH15	6	CH18	31	CH47
7	CH9	32	A. GND	7	CH27	32	CH39
8	A. GND			8	CH19	33	CH56
9	CH2			9	CH28	34	CH48
10	A. GND			10	CH20	35	CH57
11	CH10	37	RTC IN	11	CH29	36	CH49
12	A. GND	38	D. GND	12	CH21	37	CH58
13	CH3	39	EXT TRIG IN	13	CH30	38	CH50
14	A. GND	40	D. GND	14	CH22	39	CH59
15	CH11			15	CH31	40	CH51
16	A. GND			16	CH23	41	CH60
17	CH4			17	CH40	42	CH52
18	A. GND			18	CH32	43	CH61
19	CH12			19	CH41	44	CH53
20	A. GND			20	CH33	45	CH62
21	CH5			21	CH42	46	CH54
22	A. GND			22	CH34	47	CH63
23	CH13			23	CH43	48	CH55
24	A. GND			24	CH35	49	A. GN
25	CH6	50		25	CH44	50	A. GN

DT1761 Configuration

The DT1761 module has a number of configurations for user selection. Explanations are as follows:

A. Device Address Selection: The device address is completely dip switch selectable. Selection is accomplished by a compare between the dip switch and the actual address. The dip switch open position will compare to a "one" of the address bit.

Switch \ Address Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B8				5	7	4	2	1	3	6	8					
B11												3	2			

Bits 15 through 13 always look like a 1 for the address decode.

Bits 2 to 0 decode the following address: 176770

Address Bits	2	1	0	Register
	0	0	0	ADCSR LO BYTE
	0	0	1	ADCSR HI BYTE
	0	1	0	DATA BUFFER *
	0	1	1	DATA BUFFER *
	1	0	0	DMWCR *
	1	0	1	DMWCR *
	1	1	0	DMAR *
	1	1	1	DMAR *

* NOT BYTE ADDRESSABLE

B. Vector Address Selection: The vector address is also dip switch selectable. An open of the switch is equivalent to a one in the vector address. The vector address is selectable from bits 7 through 3 as follows: 130

Switch \ Address Bit	7	6	5	4	3	2	1	0
B11	4	1	6	7	8	*	*	*

* Bits 2, 1, 0 are utilized as follows: Bit 2 - Set by DMA EOR interrupt.
Bit 1, 0 - Always Ø.

PR = 4

C. A/D Input Range Selection: A/D Ranges are selected via jumpers on the module.

0 - 10V	R3 - R4,	S3, S1	
±10V	R2, R4	S3, S1	Offset Binary
	R2, R4	S2, S1	2's complement

NOTE: P2-P3 Always connected.

D. DAC Range Selection:

	YDAC	XDAC	OFFSET BINARY	2's Complement
±5V	Y1-Y2 Y3-Y4	X1-X2 X3-X4	M2-M3	M1-M3
±10V	Y1-Y2	X1-X2	M2-M3	M1-M3
0 - 10V	Y3-Y4	X3-X4	M2-M3	N/A

E. DAC Intensify Timing:

Set Up Delay	3 usec	20 usec	1 usec-0.5 sec
	D-D1	D-D2	D-D3 (C EXT)
	0.5 usec	5 usec	.2 usec-100 usec
Z Pulse Width	I-I2	I-I3	I-I1 (C EXT)

$PW \cong 0.5796\ C_p$

$C_p > 1000pF$

F. Operation with Calibration and Test Routine - The calibration and test routine SP-006 provides the user with a means for verifying operation of the module and calibration of the unit. Each test is started at its proper starting address as indicated on the listing supplied. The software requires that the device address and vector address be configured to the following address:

Base device address 177000:

Vector address 130:

Switch Configuration:

B8-1	C
B8-2	O
B8-3	C
B8-4	O
B8-5	O
B8-6	C
B8-7	O
B8-8	C
B11-1	O
B11-2	C
B11-3	C
B11-4	C
B11-5	C
B11-6	C
B11-7	O
B11-8	O

C=Close

O=Open

Shipment configuration: The unit is shipped in the following configuration:

Base Device Address:	177000
Vector Address:	130
A/D Range	±10V, 2's complement
D/A Range	±10V, Offset Binary
Z pulse width	0.5 us
Z delay	3 us

All numbers, unless otherwise stated, are in octal notation.

Note to RT-11 users:

Due to the RT-11 KMON use of interrupts on the keyboard/printer, this software will not run properly. To run this software, load SP-006 into memory. Halt the processor to return to the ODT micro-code routine. Deposit Ø into locations 177562 and 177564. This disables interrupts from the keyboard/printer. RT-11 is now prevented from interfering with the I/O routines. To run the tests in this software, use the ODT go instruction (see LSI-11 Processor Handbook for information on the ODT program).

Calibration of Analog Input Portion

The board must be configured for two's complement operation on the A/D section.

1. Load SP-006,
2. Connect voltage standard to channel Ø input.
3. Set voltage standard to -2.4mV.
4. Start program at location 1000. The program will now output. continuous A/D data. Data is output as a 4 digit octal number.
5. Adjust the A/D offset control (see DT1761 Series Adjustment Locations) so that the printout ranges between 7777 and 0000 (i.e. there is no printout of any value other than these two values). Try to adjust the offset so that there is an equal predominance of the two values listed.
6. Set voltage standard to +9.9927V and adjust the A/D range control so that the printout ranges between 3776 and 3777 in a manner similar to that described in (5) above.

The following steps need only be followed if the module is equipped with the programmable switch gain amplifier option.

7. Stop the program. Set the gain to 8 (this is accomplished by depositing 1100 in location 1006).
8. Set voltage standard to -600uV.
9. Start the program at location 1000.
1Ø. Adjust the switch gain offset pot until the printout ranges between 7777 and 0000 (follow the procedure described in Step 5 for adjustment).

This completes the calibration of the analog input section.

Channel Scan Routine

This routine allows the user to check the operation of the MUX on different channels. To run this routine, load SP-006 and start the program at location 126Ø. The routine will now cycle through all the channels, outputting a line of information on each channel. The output is in the form "CH <8 conversions output as 4 digit octal numbers> <channel number>" The routine will cycle through the channels continuously.

MODE TESTS

These tests allow the user to verify operation of the module in various modes of operation.

Increment Modes

This routine will set the increment mode enable bit on the module, and output the value of ADCSR as a 16 bit, 6 digit octal number followed by the 12 bit, 4 digit value of the A/D data. Every time a conversion is completed, the MUX address is incremented. The user should check the MUX address bits output in the ADCSR printout to insure that the multiplexer is operating properly in this mode.

External Clock/Real Time Clock Mode

This routine will enable EXT CLK/RTC mode on the module. The routine will now continuously output "NO D" until a conversion is initiated by an external clock. When this conversion is completed, the contents of ADCSR is output followed by the actual A/D data. If an error occurs, "ER".

Interrupt Test

This routine enables interrupt mode and waits for an interrupt to be received. When an interrupt occurs, the contents of ADCSR is output followed by the actual A/D data.

Calibration of Analog Output Portion

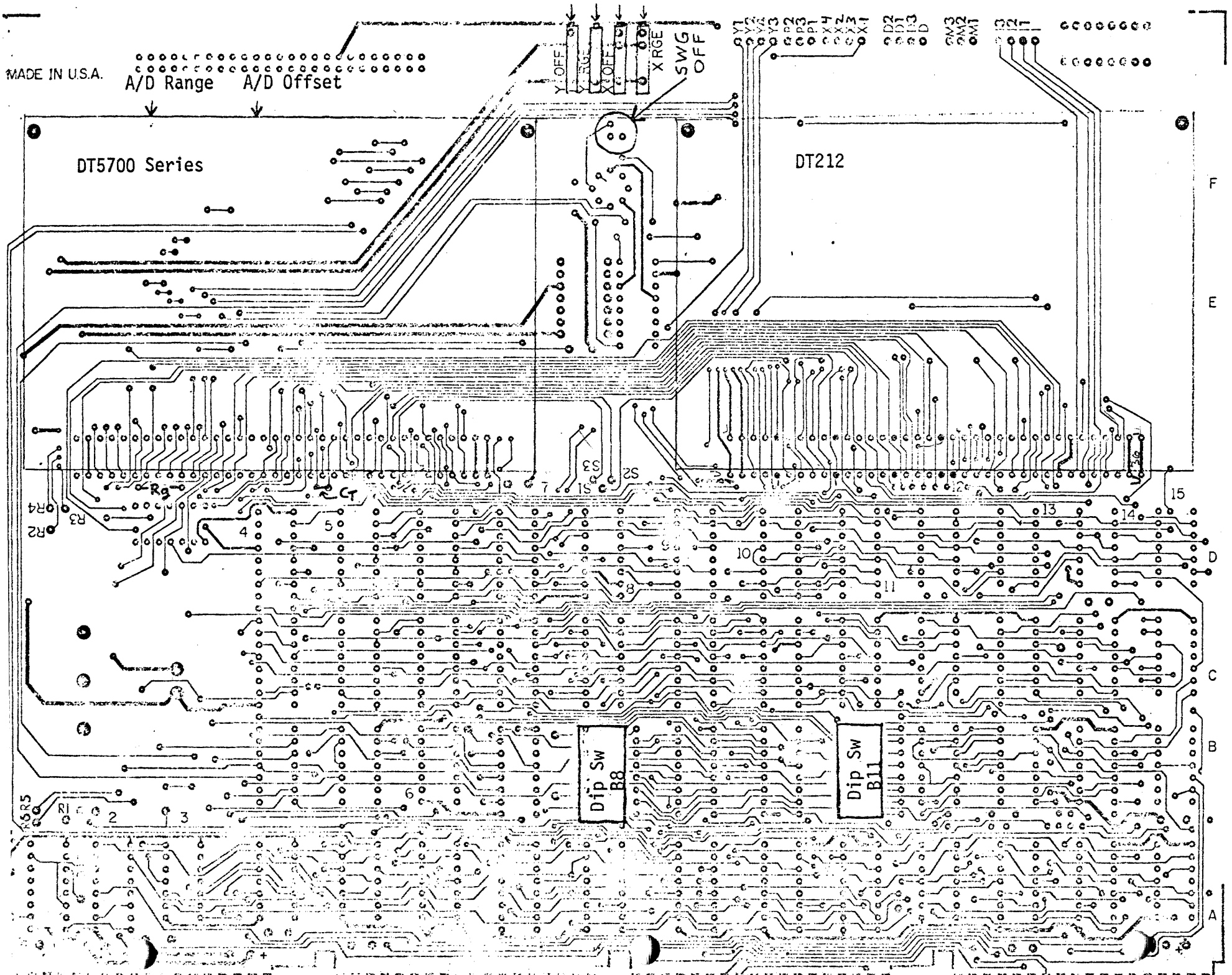
The moduel must be configured for offset binary on the D/A section. To run this test, load SP-006 and start the program at location 2132. The instructions for calibration are as follows.

1. Connect DVM to Y DAC out.
2. Adjust Y offset pot for DVM reading of -10.000V.
3. Type "N".
4. Adjust Y range pot for DVM reading of +9.9951V.
5. Type "N".
6. Connect DVM to X DAC out.
7. Adjust X offset pot for DVM reading of -10.000V.
8. Type "N".
9. Adjust X range pot for DVM reading of +9.9951V.
1Ø. Type "N". Routine is now in mode to start at Step 1.

This completes the calibration of the analog output portion.

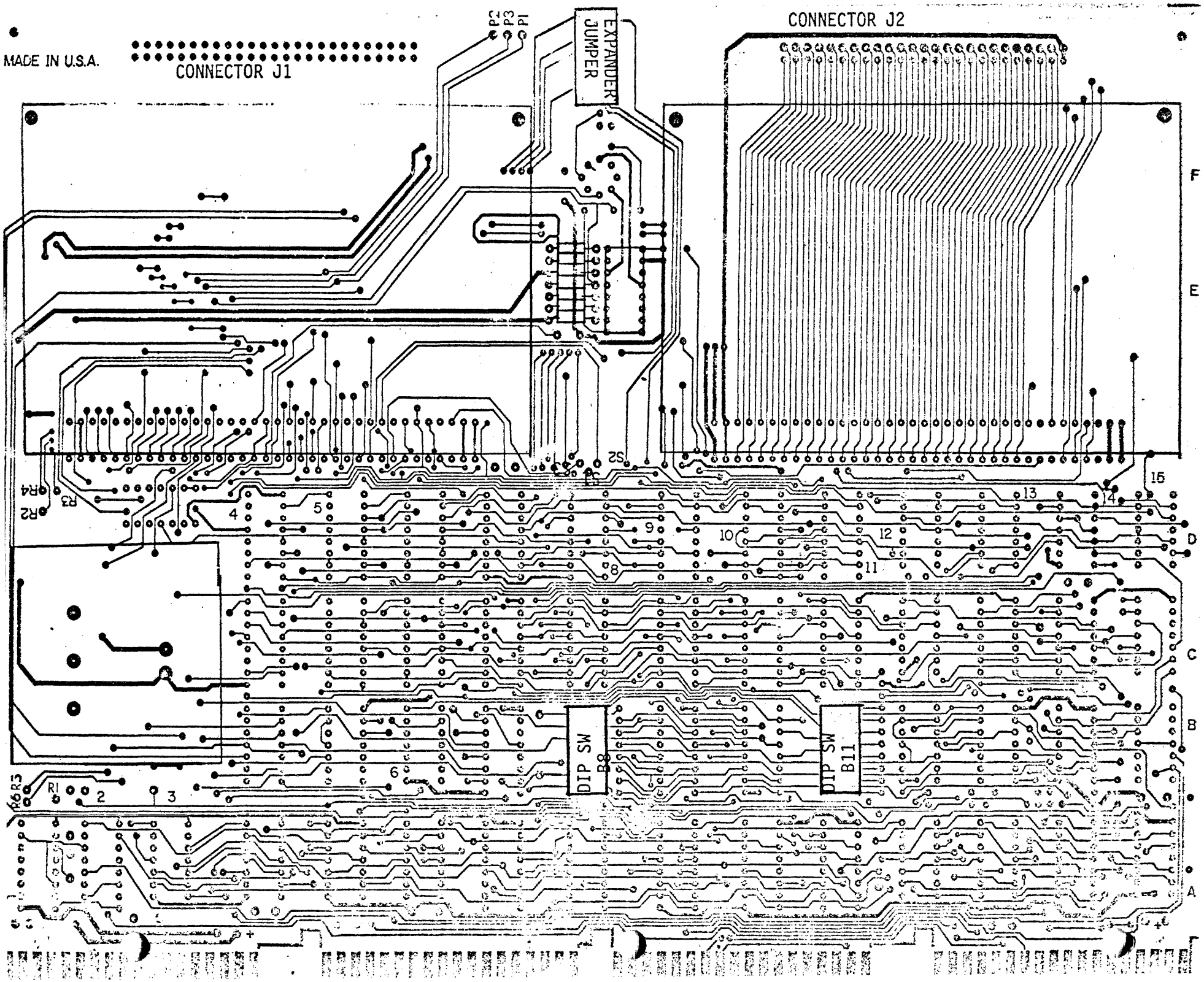
D/A Square Wave Routine

This routine generates square waves on both DACs simultaneously. To run this routine, load SP-006 and start the program at location 2076.



DT1761 Jumper and Adjustment Locations

SHEET 25 of 26 SHEETS



DT1762 jumper locations

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Data Translation, Inc.
Software Products

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We are interested in hearing of any problems encountered in the use of our software and calibration manuals. Please fill out this postage paid form and return it to us if you have any comments or suggestions regarding this release.

Title of manual/release: _____

Did you find any errors in this release? If so, please describe.

_____
_____
_____
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Did you find this manual understandable, usable, and well-organized? Please make suggestions for improvement.

_____
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_____
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Is there sufficient documentation on the software, regarding both system requirements and usage? If not, what material is missing and where should it be placed?

_____
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Please indicate the type of user/reader that you most nearly represent.

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Name _____ Date _____

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City _____ State _____ Zip Code _____

If you require a written reply, please check here. ☐

```
                                                00010   ;DT1760 SERIES CALIBRATION AND TEST RTNS
                                                00020   ;*
                                                00030   ;*
                                                00040   ;***CALIBRATION ROUTINE
                                                00050   ;*
          000000                                00060   .ASECT
          001000                                00070   .=1000
          177000                                00080   ADCSR=177000
          177002                                00090   DATDBR=177002
          177004                                00100   DMWCR=177004
          177006                                00110   DMCAR=177006
001000    012704    000012                      00140   CAL1: MOV   #12,%4
001004    012737    000000    177000            00150   CALT: MOV   #0,@#ADCSR
001012    004767    000740                      00160         JSR   %7,ADN
001016    013702    177002                      00170         MOV   @#DATDBR,%2
001022    004767    000034                      00180         JSR   %7,PRT1
001026    005304                                00190         DEC   %4
001030    001402                                00200         BEQ   C1
001032    000167    177746                      00210         JMP   CALT
001036    012700    000015                      00220   C1:   MOV   #15,%0
001042    004767    000154                      00230         JSR   %7,TTO
001046    012700    000012                      00240         MOV   #12,%0
001052    004767    000144                      00250         JSR   %7,TTO
001056    000167    177716                      00260         JMP   CAL1
                                                00270   ;*
                                                00280   ;*
                                                00290   ;12 BIT BINARY TO 4 DIGIT OCTAL TYPEOUT
                                                00300   ;*
001062    010203                              00310   PRT1: MOV   %2,%3
001064    042703    170777                    00320         BIC   #170777,%3
001070    006003                              00330         ROR   %3
001072    000303                              00340         SWAB  %3
001074    052703    000060                    00350         BIS   #60,%3
001100    010300                              00360         MOV   %3,%0
001102    004767    000114                    00370         JSR   %7,TTO
001106    010203                              00380         MOV   %2,%3
001110    042703    177077                    00390         BIC   #177077,%3
001114    006003                              00400         ROR   %3
001116    006003                              00410         ROR   %3
001120    006003                              00420         ROR   %3
001122    006003                              00430         ROR   %3
001124    006003                              00440         ROR   %3
001126    006003                              00450         ROR   %3
001130    052703    000060                    00460         BIS   #60,%3
001134    010300                              00470         MOV   %3,%0
001136    004767    000060                    00480         JSR   %7,TTO
001142    010203                              00490         MOV   %2,%3
001144    042703    177707                    00500         BIC   #177707,%3
001150    006003                              00510         ROR   %3
001152    006003                              00520         ROR   %3
001154    006003                              00530         ROR   %3
001156    052703    000060                    00540         BIS   #60,%3
001162    010300                              00550         MOV   %3,%0
001164    004767    000032                    00560         JSR   %7,TTO
```

```
001170  010203                  00570          MOV   %2,%3
001172  042703  177770          00580          BIC   #177770,%3
001176  052703  000060          00590          BIS   #60,%3
001202  010300                  00600          MOV   %3,%0
001204  004767  000012          00610          JSR  %7,TTO
001210  012700  000040          00620          MOV   #40,%0
001214  004767  000002          00630          JSR   %7,TTO
001220  000207                  00640          RTS   %7
                                00650
                                00660  ;*
                                00670  ;*
                                00680  ;TTY OUTPUT
                                00690  ;*
001222  105737  177564          00700  TTO:  TSTB  @#177564
001226  100375                  00710          BPL   .-4
001230  010037  177566          00720          MOV   %0,@#177566
001234  000207                  00730          RTS   %7
001236  012700  000015          00731  CRF:  MOV   #15,%0
001242  004767  177754          00732          JSR   %7,TTO
001246  012700  000012          00733          MOV   #12,%0
001252  004767  177744          00734          JSR   %7,TTO
001256  000207                  00735          RTS   %7
                                00740  ;*
                                00750  ;*
                                00760  ;*
                                00770  ;*
                                00780  ;CHANNEL SCAN ROUTINE-THIS PROGRAM WILL PROVIDE
                                00790  ;A TABLE OF VALUES WITH THE FOLLOWING FORMATS.
                                00800  ;******CHANNEL NUMBER-AS PUT OUT BY PROGRAM
                                00810  ;******8 CONVERSIONS ON THAT CHANNEL
                                00820  ;******CHANNEL NUMBER AS READ BACK FROM INTERFACE
                                00830  ;
                                00840  ;
001260  012700  000015          00850          MOV   #15,%0
001264  004767  177732          00860          JSR   %7,TTO
001270  012700  000012          00870           MOV  #12,%0
001274  004767  177722          00880          JSR   %7,TTO
001300  012705  000000          00890  CHS:    MOV   #0,%5            ;R5=MUX REG
001304  012700  000103          00900  CH:     MOV   #103,%0
001310  004767  177706          00910          JSR   %7,TTO           ;PRINT "C"
001314  012700  000110          00920          MOV   #110,%0
001320  004767  177676          00930          JSR   %7,TTO           ;PRINT "H"
001324  012700  000040          00940          MOV   #40,%0
001330  004767  177666          00950          JSR   %7,TTO           ;PRINT SPACE
001334  010502                  00960          MOV   %5,%2
001336  004767  000074240       00970    NOP   JSR   %7,PCH
001342  012700  000040          00980          MOV   #40,%0
001346  004767  177650          00990          JSR   %7,TTO
001352  012704  000010          01000          MOV   #10,%4           ;R4=CONV CNTR
001356  110537  177000          01010  CHB:    MOVB  %5,@#ADCSR       ;LOAD CHAN AND START CONV
001362  004767  000370          01020          JSR   %7,ADN
001366  013702  177002          01030          MOV   @#DATDBR,%2      ;INPUT A/D DATA
001372  004767  177464          01040          JSR   %7,PRT1          ;PRINT DATA
001376  005304                  01050          DEC   %4               ;DEC CONV CNTR (R4)
```

```
001400  001402                  01060          BEQ    CHA
001402  000167  177750          01070          JMP    CHB
001406  013702  177000          01080   CHA:   MOV    @#ADCSR,%2       ;INPUT ADCSR TO R2
001412  004767  000020          01090          JSR    %7,PCH
001416  004767  177614          01100          JSR    %7,CRF
001422  105205                  01110          INCB   %5
001424  120527  000017          01120          CMPB   %5,#17
001430  001723                  01130          BEQ    CHS
001432  000167  177646          01140          JMP    CH
001436  010203                  01150   PCH:   MOV    %2,%3
001440  000303                  01160          SWAB   %3
001442  042703  177707          01170          BIC    #177707,%3
001446  006003                  01180          ROR    %3
001450  006003                  01190          ROR    %3
001452  006003                  01200          ROR    %3
001454  052703  000060          01210          BIS    #60,%3
001460  010300                  01220          MOV    %3,%0
001462  004767  177534          01230          JSR    %7,TTO
001466  010203                  01240          MOV    %2,%3
001470  000303                  01250          SWAB   %3
001472  042703  177770          01260          BIC    #177770,%3
001476  052703  000060          01270          BIS    #60,%3
001502  010300                  01280          MOV    %3,%0
001504  004767  177512          01290          JSR    %7,TTO
001510  000207                  01300          RTS    %7
                                01310  ;
                                01320  ;
                                01330  ;
                                01340  ;MODES TEST-THIS ROUTINE ALLOWS TESTING OF ALL MODES
                                01341  ;OF THE ANALOG INPUT PORTION OF THE INTERFACE BY
                                01342  ;STARTING THE PROGRAM AT THE PROPER STARTING
                                01343  ;LOCATION.THE PROGRAM WILL LOOK FOR
                                01344  ;AN A/D DONE AND PRINT THE ADCSR AND A/D DATA.
                                01345  ;
                                01346  ;
                                01390  ;
                                01400  ;
                                01401  ;INCREMENT MODE TEST
                                01402  ;
                                01403  ;
001512  012737  040000  177000  01404          MOV    #40000,@#ADCSR
001520  004767  000232          01405   IA:    JSR    %7,ADN
001524  004767  000060          01406          JSR    %7,PCD
001530  012737  000001  177000  01407          MOVB   #1,@#ADCSR
001536  000167  177756          01408          JMP    IA
                                01409  ;
                                01410  ;EXT CLK/RTC CLK TEST
                                01411  ;
001542  012737  000200  177000  01412          MOV    #200,@#ADCSR
001550  004767  000202          01413   EA:    JSR    %7,ADN
001554  004767  000030          01414          JSR    %7,PCD
001560  000167  177764          01415          JMP    EA
                                01416  ;
                                01417  ;INTERRUPT TEST(INT VECT=130)
```

```
                                        01418   ;
001564  012737  000100  177000          01419   IT:   MOV   #100,@#ADCSR
001572  000240                         01420   ITA:  NOP
001574  000167  177772                 01421         JMP   ITA
001600  004767  000004                 01422   ITB:  JSR   %7,PCD
001604  000167  177754                 01423         JMP   IT
001610  013704  177000                 01430   PCD:  MOV   @#ADCSR,%4
001614  010403                         01440         MOV   %4,%3
001616  042703  077777                 01450         BIC   #077777,%3
001622  000303                         01460         SWAB  %3
001624  006003                         01470         ROR   %3
001626  006003                         01480         ROR   %3
001630  006003                         01490         ROR   %3
001632  006003                         01500         ROR   %3
001634  006003                         01510         ROR   %3
001636  006003                         01520         ROR   %3
001640  006003                         01530         ROR   %3
001642  052703  000060                 01540         BIS   #60,%3
001646  010300                         01550         MOV   %3,%0
001650  004767  177346                 01560         JSR   %7,TTO
001654  010403                         01570         MOV   %4,%3
001656  042703  107777                 01580         BIC   #107777,%3
001662  000303                         01590         SWAB  %3
001664  006003                         01600         ROR   %3
001666  006003                         01610         ROR   %3
001670  006003                         01620         ROR   %3
001672  006003                         01630         ROR   %3
001674  052703  000060                 01640         BIS   #60,%3
001700  010300                         01650         MOV   %3,%0
001702  004767  177314                 01660         JSR   %7,TTO
001706  010402                         01670         MOV   %4,%2
001710  004767  177146                 01680         JSR   %7,PRT1
001714  012700  000040                 01690         MOV   #40,%0
001720  004767  177276                 01700         JSR   %7,TTO
001724  013702  177002                 01710         MOV   @#DATDBR,%2
001730  004767  177126                 01720         JSR   %7,PRT1
001734  012700  000015                 01730         MOV   #15,%0
001740  004767  177256                 01740         JSR   %7,TTO
001744  012700  000012                 01750         MOV   #12,%0
001750  004767  177246                 01760         JSR   %7,TTO
001754  000207                         01770         RTS   %7
                                        01780   ;
                                        01790   ;
                                        01800   ;A/D DONE TEST-THIS TEST FIRST LOOKS FOR THE
                                        01810   ;ERROR BIT AND WILL PRINT "ERROR" ON THE
                                        01820   ;CONSOLE IF IT IS SET IT WILL THEN LOOK
                                        01830   ;FOR THE DONE BIT IF IT IS SET IT WILL RETURN
                                        01840   ;TO THE CALLING PROGRAM,IF NOT IT WILL LOOP
                                        01850   ;FOR 4096 TIMES TESTING DONE IF DONE NEVER SETS
                                        01860   ;IT WILL PRINT "NO DONE" ON THE CONSOLE AND
                                        01870   ;RETURN TO THE CALLING TEST
                                        01880   ;
001756  012701  170000                 01890   ADN:   MOV   #170000,%1
001762  005737  177000                 01900   ADNA:  TST   @#ADCSR
```

```
                                                01910          BMI    ERR
                                                01920          TSTB   @#ADCSR                  ;TEST DONE
                                                01930          BMI    DNE
                                                01940          INC    %1
                                                01950          BEQ    NDN
                                                01960          JMP    ADNA
                                                01970  DNE:    RTS    %7
                                                01980  ERR:    MOV    #3000,%1
                                                01990  ERRA:   MOV    (%1)+,%0
                                                02000          JSR    %7,TTO
                                                02010          CMP    %1,#3004
                                                02020          BNE    ERRA
                                                02030          RTS    %7
                                                02031
                                                02040  NDN:    MOV    #3005,%1
                                                02050  NDNA:   MOV    (%1)+,%0
                                                02060          JSR    %7,TTO
                                                02070          CMP    #3013,%1
                                                02080          BNE    NDNA
                                                02090          MOV    #15,%0
                                                02100          JSR    %7,TTO
                                                02110          MOV    #12,%0
                                                02120          JSR    %7,TTO
                                                02130          JMP DNE
                                                02140  ;
                                                02150
                                                02160  ;D/A CONVERTER TESTS-THE FOLLOWING ROUTINES ARE
                                                02170  ;PROVIDED TO TEST AND CALIBRATE THE ANALOG
                                                02180  ;OUTPUT SECTION OF THE INTERFACE
                                                02190  ;
                                                02200  ;
                                                02210  ;FULL SCALE SQUARE WAVE TEST-THIS TEST PROVIDES
                                                02220  ;A SQUARE WAVE OUTPUT ON BOTH X&Y D/A'S FOR
                                                02230  ;SETTLING TIMES AND RISE TIME MEASUREMENTS.
                                                02240  ;
                                                02250  ;
002076  012737  000000  177002                  02260  DASQ: MOV    #0,@#DATDBR
002104  012737  050000  177002                  02270        MOV    #050000,@#DATDBR
002112  012737  027777  177002                  02280        MOV    #027777,@#DATDBR
002120  012737  177777  177002                  02290        MOV    #177777,@#DATDBR
002126  000167  177744                          02300        JMP    DASQ
                                                02310  ;
                                                02320  ;
                                                02330  ;
                                                02340  ;D/A CALIBRATE ROUTINE-THIS ROUTINE WILL ALLOW
                                                02350  ;THE USER TO CALIBRATE THE DACS.THE ROUTINE ASSUMES
                                                02360  ;THE DACS ARE CONFIGURED EITHER STRAIGHT BINARY
                                                02370  ;OR OFFSET BINARY.THE USER STARTS THE PROGRAM
                                                02380  ;AT THE SPECIFIED PLACE AND DAC Y IS SET TO 0000
                                                02390  ;WHEN AN "N" IS TYPED AT THE KEYBOARD INPUT
                                                02400  ;DAC Y IS SET TO 7777.AT THE NEXT "N" DAC X=0000
                                                02410  ;AT THE NEXT "N" DAC X=7777.THE TEST WILL REPEAT
                                                02420  ;AS "N" IS TYPED.
                                                02430  ;
```

```
 271                                            02440   ;
 272  002132  012737  000000  177002            02450   DACA: MOV   #0,@#DATDBR
 273  002140  004767  000106                    02460         JSR   %7,IKB
 274  002144  022700  000116                    02470         CMP   #116,%0
 275  002150  001402                            02480         BEQ   DACB
 276  002152  000167  177754                    02490         JMP   DACA
 277  002156  012737  077777  177002            02500   DACB: MOV   #077777,@#DATDBR
 278  002164  004767  000062                    02510         JSR   %7,IKB
 279  002170  022700  000116                    02520         CMP   #116,%0
 280  002174  001402                            02530         BEQ   DACC
 281  002176  000167  177754                    02540         JMP   DACB
 282  002202  012737  100000  177002            02550   DACC: MOV   #100000,@#DATDBR
 283  002210  004767  000036                    02560         JSR   %7,IKB
 284  002214  022700  000116                    02570         CMP   #116,%0
 285  002220  001402                            02580         BEQ   DACD
 286  002222  000167  177754                    02590         JMP   DACC
 287  002226  012737  177777  177002            02600   DACD: MOV   #177777,@#DATDBR
 288  002234  004767  000012                    02610         JSR   %7,IKB
 289  002240  022700  000116                    02620         CMP   #116,%0
 290  002244  001732                            02630         BEQ   DACA
 291  002246  000167  177754                    02640         JMP   DACD
 292                                            02650   ;
 293                                            02660   ;
 294  002252  105737  177560                    02670   IKB:  TSTB  @#177560
 295  002256  100375                            02680         BPL   IKB
 296  002260  013700  177562                    02690         MOV   @#177562,%0
 297  002264  042700  000200                    02691         BIC   #200,%0
 298  002270  000207                            02700         RTS   %7
 299                                            02701   ;
 300                                            02702   ;
 301          002272                            02703   .ASECT
 302          003200                            02704   .=3200
 303                                            02705   ;
 304                                            02706   ;INTR HANDLER
 305  003200  004767  176552                    02707   IH:   JSR   %7,ADN
 306  003204  000002                            02708         RTI
 307                                            02709
 308          003000                            02710   .=3000
 309  003000  051105  047522     122            02711   .ASCII /ERROR/
 310  003005     116  020117  047504            02712   .ASCII /NO DONE/
      003012  042516
 311          000130                            02713   .=130
 312  000130  003200  000000                    02714   .WORD 003200,0
 313                                            02717   ;
 314          000001                            02718   .END
```

```
ADCSR  = 177000          ADN     001756          ADNA    001762          CALT    001004
CAL1     001000          CH      001304          CHA     001406          CHB     001356
CHS      001300          CRF     001236          C1      001036          DACA    002132
DACB     002156          DACC    002202          DACD    002226          DASQ    002076
DATDBR = 177002          DMCAR  = 177006          DMWCR  = 177004          DNE     002006
EA       001550          ERR     002010          ERRA    002014          IA      001520
IH       003200          IKB     002252          IT      001564          ITA     001572
ITB      001600          NDN     002032          NDNA    002036          PCD     001610
PCH      001436          PRT1    001062          TTO     001222          .      = 000134

         000000
```

ERRORS DETECTED: 0