DATAMATION

64

April

Spring Joint Computer Conference

Washington D.C. April 21-23

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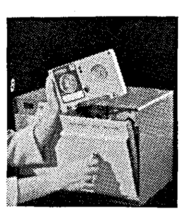
Save it for parades. Now Ampex magnetic tape is faster, more accurate and costs less.

And it's more efficient. One small Ampex CDR-1 tape cartridge stores as much data as 7000 feet of paper. And can be erased and used again. Paper tape systems are slow. The CDR-1—an incremental digital recorder—records 2400 bits of information per second. Plays back up to 3840 bits per second. Paper tape systems need operators. The CDR-1 is automatic. Paper tape systems make mistakes. With the CDR-1 mistakes are less than 1 in 10,000,000. And mistakes are spotted—the CDR-1 automatically verifies every



AMPEX

bit of data it records. In short: Ampex has made all the benefits of magnetic tape available to manufacturers of systems incorporating other input/output devices. The CDR-1 is comparably priced, incomparably better. And available now for evaluation by manufacturers of systems designed for communications, factory data acquisition, data logging, machine tool control, computer input/output devices, and many other applications. For full details on the CDR-1, write Ampex Corporation, Redwood City, California.

CIRCLE 1 ON READER CARD

HOW DO YOU BECOME AN ELDER STATESMAN IN JUST 10 YEARS?

By imitating us ▪ Back when C-E-I-R began operations in 1954, the computer industry was in its infancy. Operations research and mathematical modelling, like most of the powerful conceptual resources of management science, were largely untapped. ▪ Then C-E-I-R arrived on the scene to meet the growing need of business, science, and government for precise problem solving through resources of human intellect amplified by electronic logic. By the standards of that time, it was a bold undertaking. But even the boldest of visions have been surpassed by the accelerating pace of technological progress. ▪ In these past ten years, improvements in computing hardware have come in abundance... larger systems capacity, faster operating cycles, superior command structures. These developments have been accompanied by software innovations . . . automatic programming, translators, simulators, compilers, common languages. ▪ These extensions in hardware and software have been facilitated largely through contributions made by C-E-I-R in "brainware"—a term which covers our many accomplishments in computer services, management science and analytical research. Ten years old, C-E-I-R takes pride in its position as an elder statesman of the industry. ▪ Some of the major achievements of our first decade: * C-E-I-R established a network of computing centers, bristling with 30 million dollars worth of advanced hardware, spanning the United States, and stretching beyond to London, Paris, and Mexico City. * C-E-I-R organized a distinguished professional team of hundreds of mathematicians, statisticians, economists, computer programmers, engineers, physicists, and other scientists, of whom many are internationally acclaimed authorities in their respective fields. * C-E-I-R created unique proprietary software systems for linear programming (LP90/94), resources allocation and multi-project scheduling (RAMPS), electric utility applications (C-EUA), advertising media-cost programming (MEDIAMETRICS), and other optimized man-machine decision systems. * C-E-I-R implemented state-of-the-art programming projects for the industry at large, including advanced compilers of compilers, interpreters, simulators, and other specialized linguistic systems blanketing three generations of main frames. * C-E-I-R advanced new concepts to improve profit; minimize risk; streamline business strategy and policy making; forecast trends; simulate decision environments; optimize information storage and retrieval; improve communications and control; and extract maximum efficiencies from man-machine systems. * C-E-I-R implemented and extended the repertory of problem solving techniques to optimize interfunctional performance in marketing, advertising, finance, production, inventory, quality assurance, reliability analysis, experimental design, research and development. * C-E-I-R developed national, sub-national, and supra-national models and industrial development techniques without parallel in the history of government planning. ▪ Today C-E-I-R credentials are unmatched. C-E-I-R is the world's oldest, largest, best-equipped, and most experienced computer service and problem solving organization, assisting large and small clients alike, at home and abroad, in business, science and government. If you would like to discover how this legacy of analytical and machine strength can amplify profit and performance in your organization, write or call:

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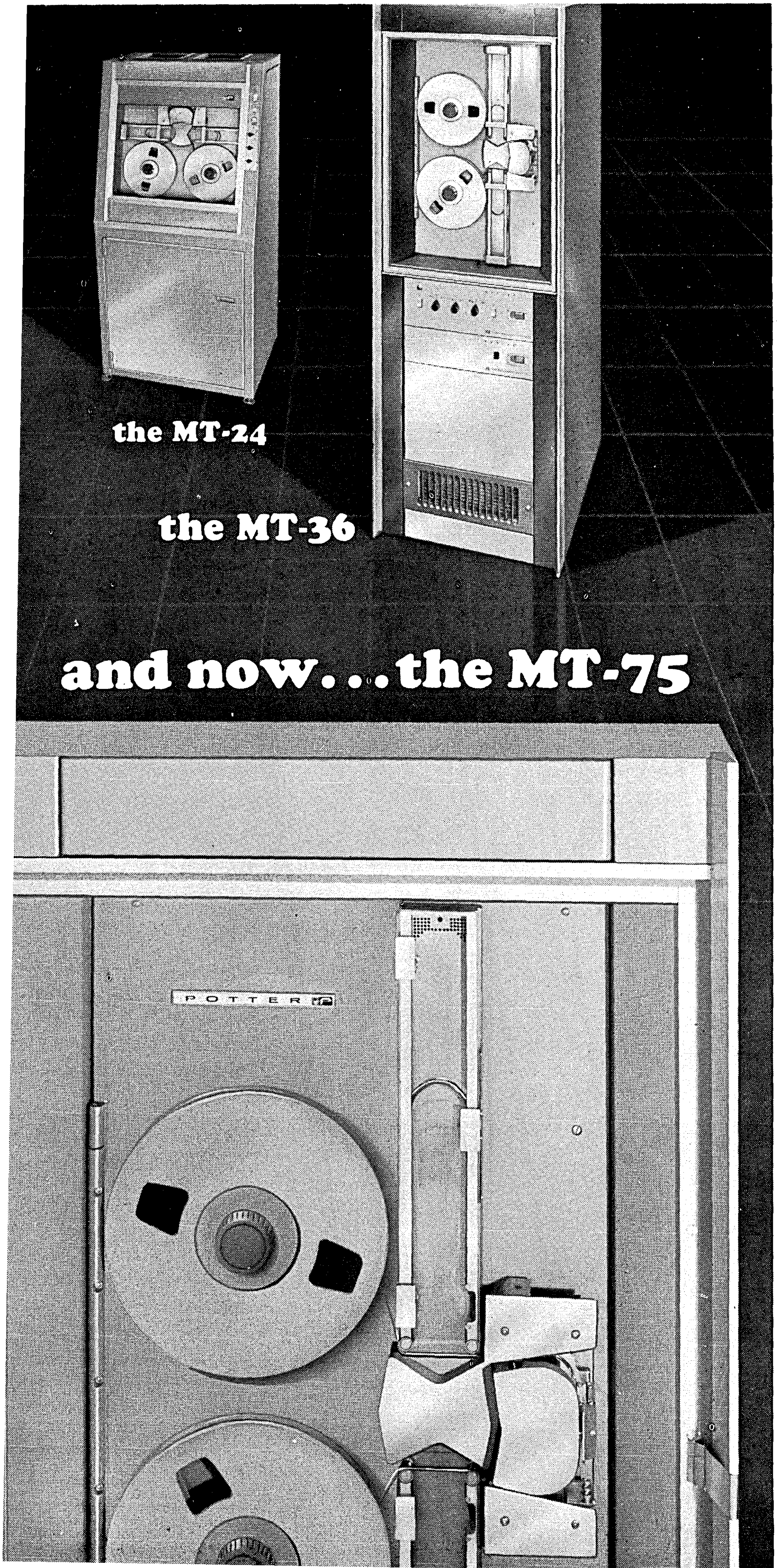
CIRCLE 5 ON READER CARD



Small cost... BIG PERFORMANCE

Now, with the introduction of the new MT-75, Potter offers a complete family of high-performance, vacuum-column magnetic tape transports, featuring packing densities to

800 b.p.i.

These new Potter transports, the MT-24, the MT-36, and the MT-75, have been thoroughly value-engineered for the highest possible reliability at minimum cost. They cover a tape speed range of 1 to 75 ips; provide data transfer rates to 60kc. All are IBM-compatible. Here are the facts:

MT-24: 1–36 ips — data transfer to 28.8kc, 200 commands per sec.

MT-36: 1–50 ips — data transfer to 40kc, 200 commands per sec.

and the NEW MT-75: 1–75 ips — data transfer to 60kc, 200 commands per sec.

Interested? Complete data is available on these, as well as many other Potter models for speeds to 150 ips and packing densities to 1200 b.p.i. For information on the broadest line of digital transports available anywhere, just write to Sales Manager.

POTTER®
INSTRUMENT CO., INC.
151 Sunnyside Boulevard, Plainview, New York

®

CIRCLE 6 ON READER CARD

DATAMATION 64

the automatic handling of information

volume 10 number 4

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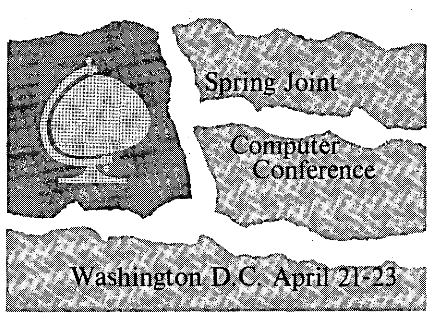
Cover

DATAMATION 64 April



Strike up the band, raise the flag. Getting ready to unfurl is the '64 SJCC, previews of which begin on p. 59. Adapted for this month's cover, Old Glory symbolizes the locale of the conference, Washington, D.C. Cover design is by Art Director Cleve Boutell.

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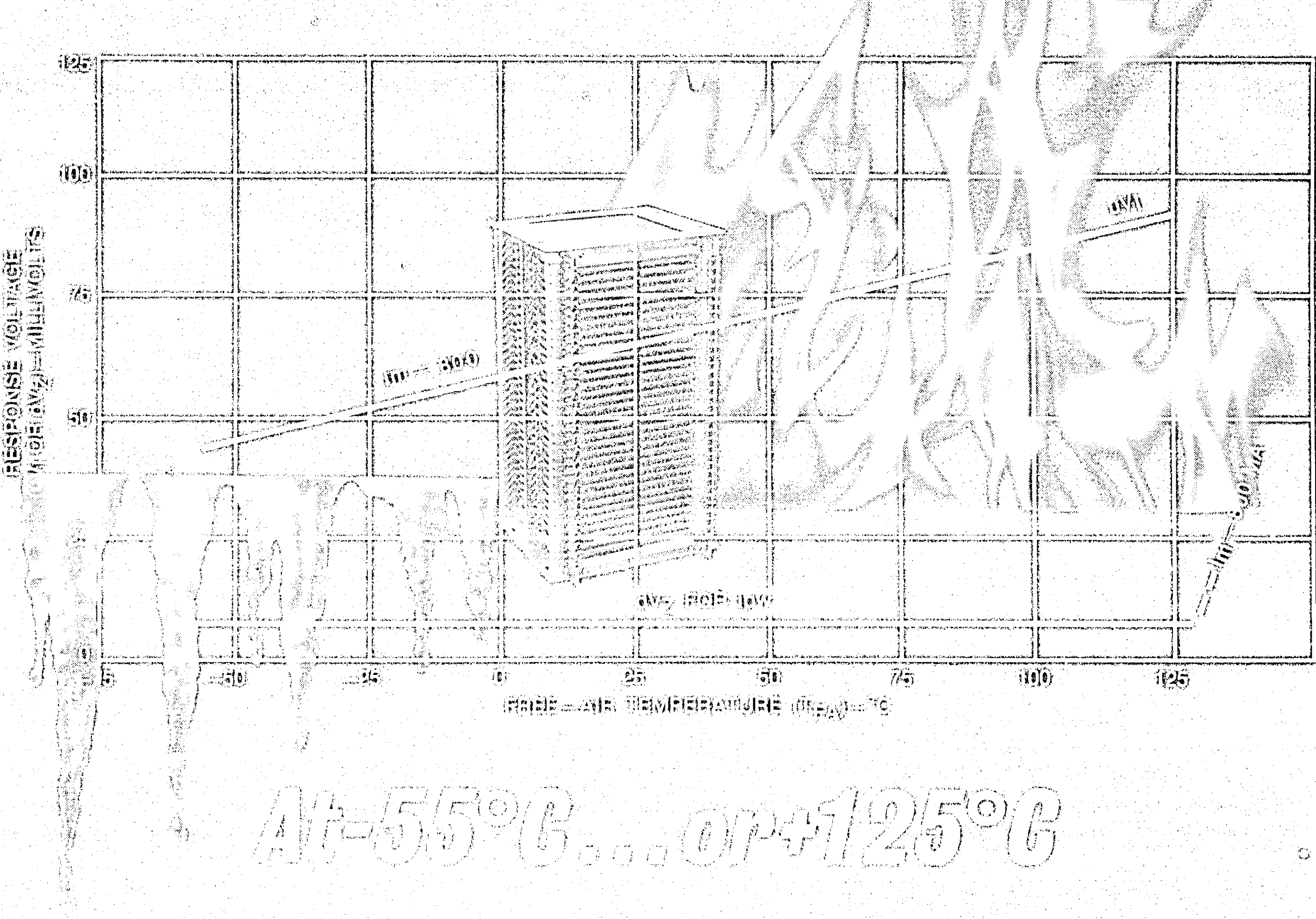
NOW YOU CAN ELIMINATE TEMPERATURE CONTROLS FROM FERRITE MEMORIES...

EVEN FROM 2 μSEC HIGH-SPEED SYSTEMS



RCA high-speed, wide-temperature-range ferrite memory planes and stacks operate without temperature controls or current compensation over any 100 centigrade degree range between the limits of -55°C and +125°C.

Memory planes and stacks using RCA 0146M5 ferrite cores provide high-speed operation over the full temperature range with less than 180 ma partial-write current. At full driving current of 800 ma, these temperature-stable cores have a switching time of approximately 0.5 μsec, making them particularly suitable for memory systems with 2 μsec operating cycles.

RCA wide-temperature-range cores are also available for low drive operation at slower speeds.

The full line of RCA cores, planes and stacks offers a wide variety of types for coincident-current, word-address, and switching applications at speeds to 250 nsec. Complete RCA memory systems range in size from 256 words x 8 bits to 16,384 words x 20 bits and offer speeds to 250 nsec.

Whatever your memory requirements, call your RCA Representative for a coordinated application service for RCA memory components and devices, ranging from cores and transistors to complete memory systems. For technical data, write: RCA Electronic Components and Devices, Memory Products Operation, Section F-D-4 , 64 "A" Street, Needham Heights 94, Mass.

The Most Trusted Name in Electronics

See RCA High-Speed Cores and Microferrites at SJCC... Booths 21-22

What makes ASI's 2100 today's outstanding computer buy?

ASI's new 2100 is designed to satisfy both small and medium scale computer needs, combining high operational speed, expanded input/output capabilities and low cost-to-answer ratios in a convenient to use, compact unit. Check just a few of the 2100's features:

MEMORY—2 microsecond total memory cycle time . . . 21 bit word . . . 4096 word core memory expandable in modules of 2,048 words.

ARITHMETIC AND CONTROL—Three index registers . . . double precision hardware . . . fast indirect addressing . . . convenient subroutine access . . . instructions to facilitate floating point operation . . . rapid instruction execution.

Add— 4 usec.
Multiply—30 usec.
Double Add—12 usec.
Unconditional Transfer— 2 usec.

INPUT/OUTPUT—Up to eight complete, buffered, bidirectional input-output channels . . . 500 KC total word input-output rate . . . channels will accept information in 6 to 48 bit fields as specified by the program . . . any channel may be connected to as many as 32 external devices . . . each external device has its own unique interrupt address to which program can be automatically transferred . . . multiple priority interrupts, each with its own order of priority . . . external device operations require program attention for initiation only . . . central processor may communicate directly with external devices without using buffered channels.

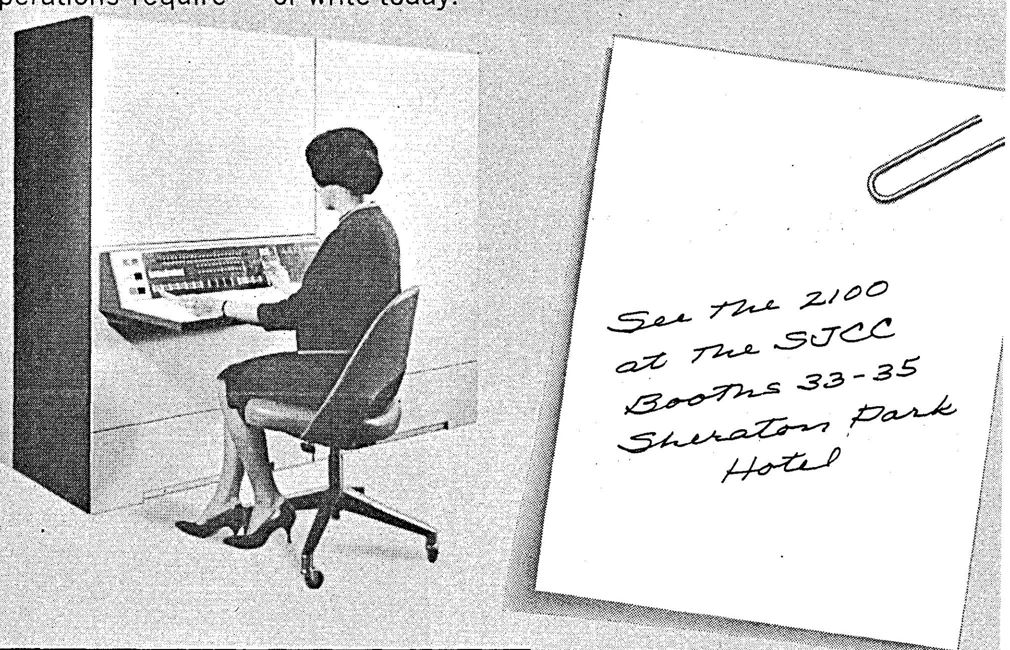
SIZE AND POWER REQUIREMENTS—A single upright cabinet includes all electronics power supply and operator control and display panel . . . over-all height 67 inches, depth 25.5 inches, width 72 inches; power consumption is less than 1.8KW . . . standard 110/120 volt 60 cycle AC. No special temperature or humidity controls required.

PERIPHERAL EQUIPMENT—Available with the 2100 is a complete line of proven peripheral equipment . . . high and low density magnetic tape units . . . 800, 200 and 100 cpm card reader . . . 250 and 100 card punches . . . incremental plotter systems . . . 500 character per second paper tape reader . . . 100 character per second paper tape punch . . . input/output typewriter . . . 400 and 200 lpm line printers . . . A-to-D and D-to-A conversion units.

SOFTWARE—A complete package of programs, compilers and routines . . . field tested FORTRAN II . . . symbolic assembler . . . mathematical subroutines . . . available at delivery of 2100 system.

PRICE AND DELIVERY—The prices of the 2100 begin at $87,800 . . . monthly lease price $2,590 . . . first deliveries in December 1963.

For complete descriptive data on ASI's 2100, call or write today.



ASI | 2100

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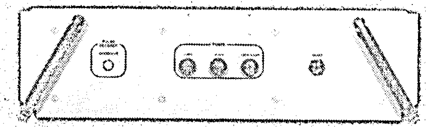

Motorola's TP3000 non-impact electronic teleprinter has been selected for more than 500 critical military and scientific readouts. Reasons: *RELIABLE*... offers higher MTBF predictions than any comparable equipment. *FAST*... up to 3000 WPM or 2400 bits per second with standard 8½" or 72-column page width. *QUIET*... inaudible under normal room environment. *VERSATILE* ...translator can selectively drive 30 or more remote printers. *FLEXIBLE*... accepts up to 8 level codes, generates up to 64 characters, symbols or figures. Typical applications: NASA—at McDonnell Aircraft Corp. as AGE monitor and readout on Gemini program, and at JPL for space flight data systems. ARMY—at Ft. Huachuca as readout for BASIPAC and MOBIDIC. NAVY—as readout for an experimental missile control system aboard the Navy electronics test ship, USS Norton Sound. AIR FORCE—as readout for numerous Air Force "L" systems, assigned official USAF nomenclature—Electrographic Teleprinter TT-352 and Pulse Decoder KY-417. Please call or write for technical information package that includes data sheets, printing samples and teleprinter rate calculator.

MOTOROLA TP3000 HIGH-SPEED TELEPRINTERS SERVE NASA IN GEMINI CHECKOUT

Today, at McDonnell's St. Louis facility and at the Cape Kennedy launch site, Motorola TP3000's are furnishing real-time records of digital command stimuli and the response of spacecraft command equipment. Also, they are providing hard copy readout of fault detection and location data, and displays of preprogrammed maintenance instructions.

Military Electronics Division MOTOROLA

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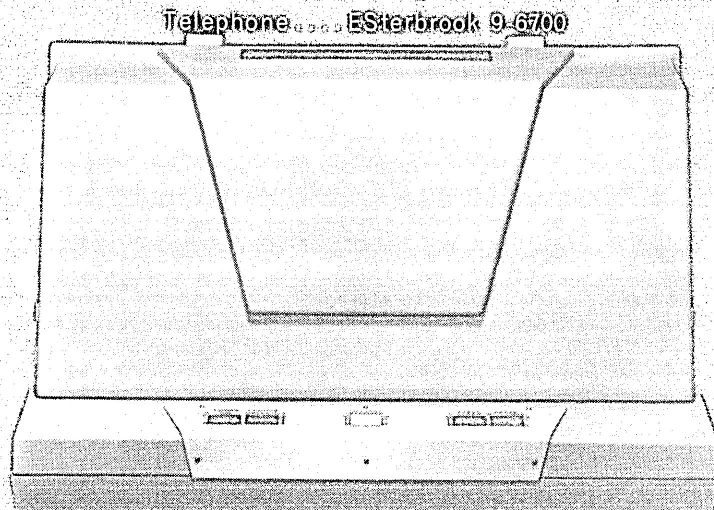
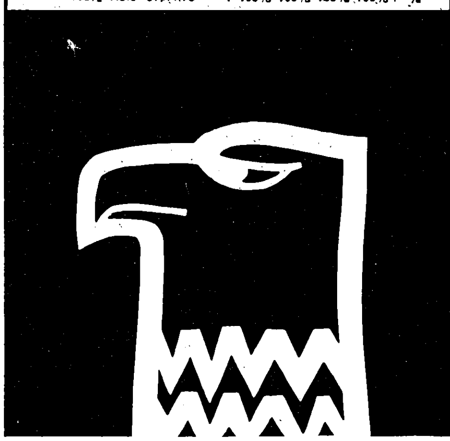


CIRCLE 9 ON READER CARD

When you think EDP, now think NCR. They did.

30¼	18⅝	HoudIn 1.20a	14	30¼	30⅜	30⅛	30⅜	+ ¼
46	40⅜	Houd pf 2.25	4	45	45	45	45	+ ½
61⅜	45½	House F 1.50	13	51⅜	52½	51⅜	51⅞	+ ¾
92½	87	Hous F pf 4	z10	91	91	91	91	+1
49⅞	42	HoustLP .72	18	48¾	48¾	47¾	47¾	— ¾
55¾	39⅝	HowJohn .88f	12	51⅛	51⅛	51	51	....
25¼	20	Haw Tel .70	12	21⅞	21⅞	21¾	21¾	— ⅛
14	9⅞	Howe Sd .40	8	10¾	10¾	10⅝	10⅝	— ⅛
59¼	47⅜	Hud Bay 3a	6	57⅞	58	57¾	58	+ ¼
36½	26⅛	HuntFds .50b	25	27⅛	27⅛	26⅝	26⅞	— ⅛
103¼	98¼	HuntF pfA 5	z20	100	100	100	100	— ½
103	98½	HuntF pfB 5	z10	100	100	100	10	+1
9⅛	6½	Hupp Cp .31t	33	7⅝	7¾	7⅝	7¾	+ ⅛
40½	31	Inspirat 1 20h	22	39	39½	38¾	38¾	— ¼
42½	30⅝	Interch 1 40	29	43¼	43½	42¾	43	+ ½
27½	23½	Interlak 1.60	13	27⅜	27⅜	27⅛	27⅜	+ ¼
567	384¼	IntBusMch 5	93	558	559	553	553	—2½
63⅛	49½	IntlHarv 2 40	29	60	60⅛	59¾	60	— ¼
175	157⅛	IntlHarv pf7	z80	165	165¾	165	165¼	+ ¼
71⅞	40¼	InMiner 1.80a	111	71¾	71⅞	71	71⅛	— ⅜
11¼	7	Int Mng .30g	5	7¾	8	7¾	8	+ ⅜
74¼	56⅝	IntNick 2.20a	69	72	73	71¾	72⅝	— ½
20¾	12⅞	Int Pack 1	16	15⅜	15⅞	15⅜	15⅜	— ⅜
36¼	26⅛	IntPap 1.05b	x103	31½	32	31¼	32	+ ½
35¼	20⅞	IntPipeCer 1	4	22¼	22¼	22¼	22¼	+ ⅛
114¼	101	Int Pipe pf5	2	104	104	104	104	.....
10⅝	6	Int Rectif	30	6⅞	6⅞	6⅝	6⅞	— ⅛
29⅜	16	IntResis .40a	23	16¼	16⅝	16⅛	16½	.....
89	71	Int Salt 4	1	88½	88½	88½	88½	— ½
28¼	24	IntlShoe 1.20	26	25⅞	26¼	25⅞	26¼	+ ⅜
42¾	34	IntSilv 1.20b	14	41⅜	41½	40¾	41½	— ½
57¾	41¾	Int T&T 1	178	55	55¾	55	55½	+ ⅜
109½	101	IntT&T pfC4	z10	108¼	108¼	108¼	108¼	..
109½	100½	IntT&T pfD4	z230	107¾	108½	107¾	108½	+ ½
25⅜	20	IntUtil .80	15	22	22⅛	22	22⅛	+ ⅜
52	42½	Int Util pf 2	1	44⅜	44⅜	44⅜	44⅜	+ ⅛
52¾	28¼	InterDS .70b	35	44	45½	43½	45½	+1½
27½	20⅝	IntMotFrt .80	17	21⅝	21⅞	21½	21⅝	...
28¼	23⅞	InterPw 1.05	9	26½	26⅝	26¼	26⅜	— ⅜
31⅞	27⅝	IowaElLP 1	1	28½	28½	28½	28½	+ ⅜
58⅞	49	Iowalll GE 2	1	59¼	59¼	59¼	59¼	+ ⅜
34½	19¾	IslCrkCl 1.50	18	33	33	32¾	32¾	...
20⅞	13⅞	ITE Ckt .15g	24	20⅜	20¾	20⅛	20⅛	— ¼
13¾	10	JaegerM .60	17	11⅛	11⅞	11⅛	11⅞	+ ¾
		Japan Fd fn .33g	1	8⅜	8⅜	8⅜	8⅜	.....
9½	8	JapanFd .18e	8	8⅝	8⅝	8½	8½	....
19¼	12	Jeff Lak S	38	18¼	19	18¼	18¾	+ ⅝
90	84¼	JerCPL pf 4	z30	86½	86½	86¼	86¼	— ½
61¼	47⅝	Jewel T 1.60	26	53	53⅜	52	52	— ¾
55¾	42	JohnsManv 2	60	55⅜	56	55⅜	55¾	+ ¼
124½	73½	JohnJ 1a	16	112	112	111	111½	— ¾
21¼	14¼	JonLogan .70	21	19⅜	19⅜	18⅞	18⅞	— ½
71	47½	Jones&L 2.50	39	68¼	68¼	67⅝	67¾	— ¼
105¾	100½	Jones&L pf5	z120	105	105	105	105	.....
16	13½	Jorgens .80	3	15⅞	15⅞	15⅞	15⅞	+ ¼
29¾	19⅝	Joy Mfg 1	30	28¾	29	28½	29	+ ⅛
[redacted]								
42⅛	31⅛	KaiserAl .90	40	36½	37	36½	36⅞	+ ⅛
[redacted]								
110	102½	Kais 59pf4.75	1	103⅝	103⅝	103⅝	103⅝	+ ⅜
100¼	90	Kais pf 4.12	1	90¼	90¼	90¼	90¼	....
52¼	50	Kais ncpf2.37	1	51	51	51	51	.....
44½	37½	KanCPL 1.32	10	44	44	43¾	43¾	
48¾	38¼	KCSoln 2.50g	9	43	43⅛	43	43⅛	+ ⅜
21¾	19⅝	KC Sou pf 1	3	20¼	20½	20¼	20½	+ ¼
35½	27⅜	Kan GE 1 04	13	33¾	33¾	33½	33½	— ¼
55	47½	KanPL 1 60	21	54¼	54¼	53½	53½	— ¾
24¾	16½	KaysrR .40a	25	22	22¼	21¾	21¾	— ¼
44¾	36	Kellogg .80a	7	42¼	42⅝	42⅛	42⅛	+ ⅛
42	33	KelseyHay 2	6	38	38⅛	37¾	37¾	— ¼
47	30	Kendall 1.20	11	45¼	45¾	44¾	45	— ⅝
80⅜	66¼	Kennecott 4	111	80	80½	79¾	80	— ¼
		Ky Util 1	35	31¾	32	31⅝	31⅝	..
78¾	60¾	KernCL 2.40	22	63¼	63⅝	63⅛	63⅛	+ ⅛
42¾	34⅜	KerrMcG 1	24	37	37⅛	36½	36½	— ½
72¾	52⅜	KimbClark 2	9	64⅞	65	64¼	64½	— ¼
50	32⅛	KingS 1.60	58	42¾	42¾	42¼	42⅜	— ⅛
25	15⅛	KirkNat .40	77	20⅞	20⅞	20¼	20¼	— ⅝
		KLM Airl fn	8	18⅛	18⅝	18⅛	18⅝	.....
43⅞	39¼	Koppers 2	17	40	40½	40	40⅛	+ ⅛
93	84½	Koppers pf 4	z10	00¾	90¾	90¾	90¾	— ¾
40½	25	Korvette	48	32⅞	33⅛	32⅝	32¾	.....
30	21½	Kresge 1.20	27	28⅞	29¼	28¾	29⅛	+ ¼
20	13¼	Kroehler .20g	67	19⅞	21¼	19⅞	20⅞	+1⅛
31⅜	23¾	Kroger 1.10	42	27	27⅞	27	27⅜	+ ¼
34¾	27⅜	KVPSu 1.40a	5	30⅝	30¾	30½	30½	.....
15⅞	6⅞	Lab Electron	26	7	7	6⅞	7	+ ⅛
35⅜	25	LacGas 1.05b	14	25½	25¾	25⅛	25½	.....
29⅜	22½	Lane Bry 1	2	25⅞	25⅞	25⅝	25⅝	— ¼
17⅜	15⅝	Lanv Ritz	15	16	16⅛	15⅞	16	— ⅛
18¾	13⅛	LearS .40b	16	13¼	13½	13¼	13½	+ ⅜
24	13⅞	Lee Rubber	10	23¾	23¾	23¼	23½	...
44¼	21	Leesona .50	6	37⅞	37⅞	37½	37½	— ¾
20¼	14¼	Leh Port 1	17	15⅛	15¼	15⅛	15¼	+ ⅛
1¾	1⅛	Leh Val Ind	259	1⅝	1¾	1⅝	1⅝	— ⅛
23	21	LVInd pf1.50	1	23¼	23¼	23¼	23¼	+ ⅜
32	26¾	Lehman 1.34e	21	29⅛	29¼	29	29⅛	— ⅛
39½	27½	Lehn&Fink 1	12	29½	29½	28⅞	28⅞	— ⅞
12½	9⅜	LeonardR .60	13	10½	10¾	10½	10¾	+ ⅛
56⅞	50⅞	LOFGls 2 60	x64	54	54⅛	53⅜	53¾	+ ⅛
17⅜	12⅛	Lib McN .16t	32	16½	16⅝	16⅜	16⅜	— ¼
83⅞	66½	Liggett&M 5	40	76⅝	77	76⅜	76¾	— ⅞
159½	150	Ligg&My pf7	y10	152⅛	152⅛	152⅛	152⅛	+ ¾
47⅛	33¼	Lily Tulip 1	16	37⅛	37⅜	37⅛	37⅛	..
20¼	13½	Ling TV .12g	127	19⅜	19⅜	18½	18½	— ¾
59⅜	46½	LinkBlt 2.40a	7	59⅛	59⅜	59	59⅜	+ ½
[redacted]								
44	32¾	LockAirc 1.60	x79	36⅜	36⅝	36⅛	36½	+ ⅜
[redacted]								
24½	22	Lone S Gas 1x	100	23	23	22⅝	22¾	— ⅜
34½	29½	LongIslLt .86	68	31	31⅜	30⅞	31⅛	+ ¼
18⅜	7¼	Loral Electr	44	8⅛	8¼	8	8	— ⅛
54⅞	40⅛	Lorillard 2.50	103	44⅛	45	44⅛	45	+ ⅞
154	142¾	Lorillard pf7	z100	149	149	149	149	+ ¾
39	32	LouisGE .98	2	36½	36½	36⅛	36⅛	— ⅝
94¾	59¾	Lou Nash 3a	8	85	85	85	85	+ ½
13⅞	9⅜	Lowenstein	15	12⅞	12⅞	12½	12½	— ⅛
22⅛	19⅝	LuckySt .80b	4	19¾	20	19¾	19⅞	+ ¼
49⅞	38	LukensSt 1.40	5	41½	41⅝	41½	41½	+ ⅛
23	15½	Lykes SS .80	4	19¾	19¾	19⅝	19⅝	....
[redacted]								
80¼	56	MacyRH 2.20	13	77½	78⅞	77½	78⅞	+2⅛
[redacted]								
9¾	8	MadSG pf.60	4	8	8	8	8	...
38¾	25	MagmaC .25e	10	37	37	36⅝	37	— ⅜
48¼	35½	Magnavx .90	226	39¼	39⅞	38	38	—1⅛
33¼	28¾	Mallory 1.20	21	30⅜	30½	30	30⅜	+ ⅜
33½	21	MnShirt .70b	6	22½	22½	22	22	— ¼
27¾	21½	Manning 1.40	12	27½	27½	27⅛	27⅛	— ⅛
9⅜	5⅜	Marac Oil	2	9⅛	9⅛	9⅛	9⅛	....
59⅝	43½	Marathon 2b	33	58⅝	58⅝	58⅛	58¼	— ⅜
35	19¾	Maremont 1	13	24⅛	24½	24⅛	24⅛	— ¼
35¼	26¾	MarMid 1.15	67	31⅞	32¼	31⅞	31⅞	— ⅛
36¼	24⅜	MarlRk 1.40	58	35⅛	35¼	35	35⅛	— ⅛
15⅝	9½	Marquar .25e	3	9¾	9¾	9¾	9¾	...
40⅝	30¼	Marq C 1.80	20	34⅜	34⅞	34⅛	34⅞	+ ⅝
40⅝	32	MarshFd 1.60	11	38½	39⅞	38½	39⅞	+1¼
22⅝	18	Martin M 1	83	20	20	19⅞	20	+ ⅛
48⅞	36¼	Masonit 1.20b	18	47¾	48⅜	47¾	48⅛	+ ½
61	35½	Mattel .40	74	39	40⅛	39	40⅛	+1⅞
75	53	MayDSt 2.20	27	73	73½	72¾	73½	+ ½
19⅝	14⅞	MaysJW .80	11	15¾	15¾	15⅝	15⅝	...
39⅞	29½	Maytag 1.40a	11	35⅛	35½	34⅞	35½	+ ½
68¾	48	MCA Inc	188	56¼	56⅝	56¼	56¼	.....
39¼	34¼	MCA pf1.50	3	35⅝	35⅝	35½	35½	— ⅛
23⅞	21½	McCall .40	4	23⅝	23⅝	23¼	23¼	— ¼
23⅞	20⅝	McCord 1.20	6	22½	22½	22½	22½	+ ⅛
17¾	9⅞	McCrory .80	46	11⅜	11½	11⅜	11½	+ ⅛
89	70⅛	McCro pf3.50	z50	72	72½	71½	71½	+ ½
73¼	52⅜	McCro pf4.50	z190	60⅜	61¾	60¾	61¾	+ ¼
94	77	McCro 6pf6	z120	84¼	84¾	84¼	84¾	+1¼
31½	21⅛	McDerm .80a	55	22¾	23⅜	22⅝	23⅜	+ ⅝
60¼	47	McDonAir 1b	15	55⅞	55⅞	55⅝	55⅝	+ ⅛
40⅝	34½	McGEd 1.40a	38	36¾	36⅞	36½	36¾	
33¾	23⅜	McGHill .60a	46	33½	34	33½	34	+ ⅝
18⅞	15½	McGreg A 1	1	15¾	15¾	15¾	15¾	+ ⅛
53½	40	McIntyr 1.60	2	51⅜	51⅜	51⅛	51⅛	— ½
19	10⅞	McKee 1	4	18⅜	18⅜	18⅛	18⅜	+ ⅛
51⅜	39¼	McKess 1.50	7	44⅝	44⅝	44	44	— ¼
12	9⅞	McLean .40a	12	10¾	11	10¾	11	+ ⅛
56	46	McLouth 1.40	19	50	50⅜	49¾	49¾	— ⅛
29⅝	20⅝	McNeilM 1b	11	21⅞	21⅞	21⅝	21⅝	— ⅜
23⅜	19½	McQuay 1a	5	20⅞	20⅞	20½	20⅝	— ⅛
47⅜	37⅜	MeadCp 1.70	10	43⅞	44¼	43⅞	44	+ ¼
27⅞	16¼	MelvShoe .80	26	16¾	17	16⅝	17	+ ⅛
27⅝	20¼	Merc St 1	x2	26⅜	26⅝	26⅜	26⅝	+ ¼
120½	77½	Merck 2a	9	115⅞	116¼	115¼	115¼	—1⅜
13⅜	11½	MerrCh .30g	30	11¾	12	11¾	12	....
15⅜	11¾	Mesabi .14e	16	14¾	14⅞	14⅝	14¾	— ⅛
37⅞	27	MestaM 1	6	32	32	31¾	31¾	....
37¼	26½	MGM 1.50	18	29½	29¾	29	29	— ⅝
38⅜	15	Metrom .40a	21	30	30¼	29½	29½	— ⅜
89	84½	MetEd pf3.85	z180	85½	86	85½	86	+1
41½	34¾	Mid SU 1.16	44	40	40¼	40	40¼	— ⅛
72	49⅜	MidlRoss 3.20	6	70	70¼	69⅞	69⅞	+ ⅛
80¼	60¼	MidOil 1.80b	2	70¼	70¾	70¼	70¾	+ ¼
33¾	24¼	Miles .70a	3	32⅛	32⅛	32	32	— ⅛
24⅝	18⅜	MinerCh .70	20	19⅞	20	19⅞	20	+ ⅛
150¼	84½	Mpl Hon 2	x34	133⅞	135	133¼	134⅞	+1⅞
96	79¾	Mpl Hon pf3	3	94¾	94¾	94¼	94¼	....
73¼	52½	MinnMngM 1	x147	69	70	69	69⅝	+1⅜



NCR may not be the first name that comes to mind as a maker of electronic data processing systems. Yet why have the U.S. government and so many leading companies throughout America invested in NCR systems? Like the U.S. Air Force who uses 174 NCR 390's. Like Lockheed. Like Kaiser Jeep. Or R. H. Macy's.

The answer, we feel, lies in NCR's unique position as a long-time manufacturer of the input side of EDP. We've been making cash registers and other business equipment for 80 years. We have a practical, businessman's point of view and an outstanding ability to create a total system. We have 7500 highly trained servicemen in the field. We've been able to put NCR EDP installations into effect with a speed that others would find hard to equal. For detailed information on how NCR equipment can be applied to your firm's operations, call your local NCR representative or write today to: The National Cash Register Company, Dayton 9, Ohio.

NCR

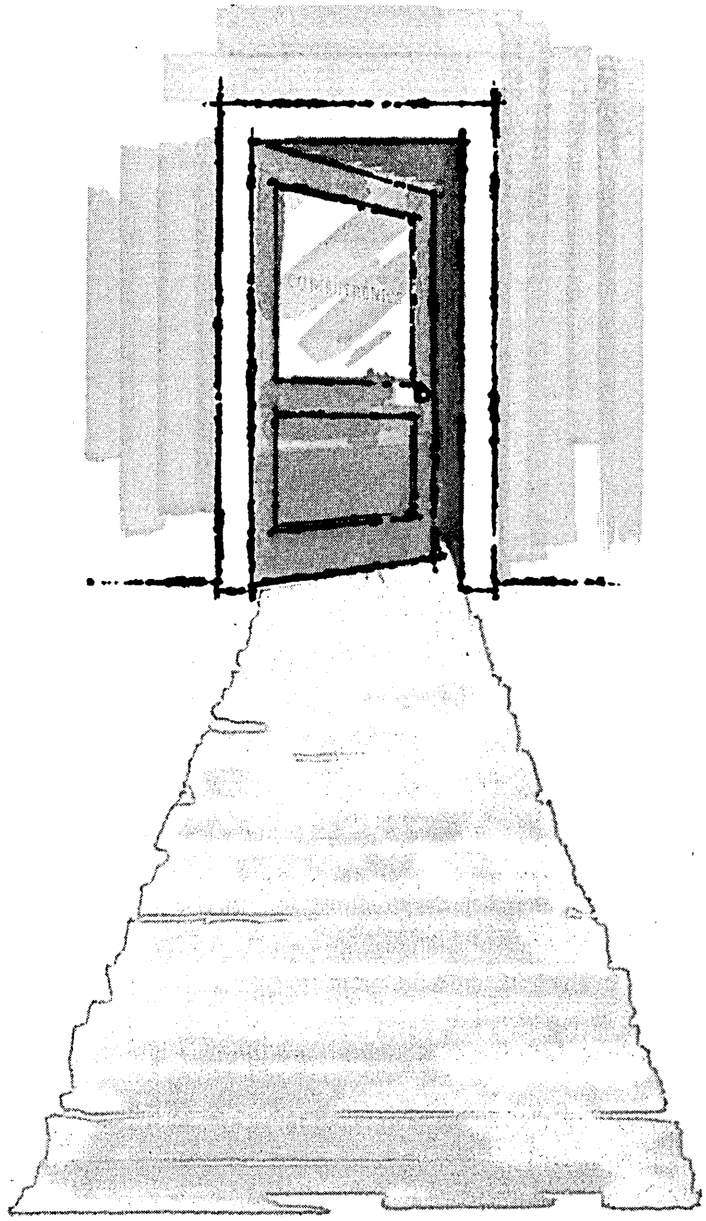
BE SURE TO VISIT THE NCR PAVILION AT THE N.Y. WORLD'S FAIR

THE NATIONAL CASH REGISTER COMPANY ®

CIRCLE 10 ON READER CARD

DATAMATION calendar

- The annual conference of the Industrial Communications Assn. will be held at the Williamsburg Lodge Conference Center in Williamsburg, Va., May 3-6.
- GUIDE International (large scale IBM edp machine users group) will hold its next meeting at the El Cortez Hotel, San Diego, May 5-8.
- The fourth national conference of the Computing and Data Processing Society of Canada will be held on May 11-12 at the Univ. of Ottawa.
- The 1964 Spring Meeting of the Society for Industrial and Applied Mathematics will be held on May 11-14 at the Hotel Shoreham, Washington, D.C.
- The ninth annual Data Processing Conference will be held at the Hotel Stafford, Tuscaloosa, Ala., May 12-13. Sponsors include DPMA, National Accountants Assn., U. of Alabama, and Certified Public Accountants.
- The 1964 Western Systems Conference, sponsored by the Systems & Procedures Assn., will be held at the Statler Hilton Hotel, Los Angeles, on May 14. Conference theme is Management Information Crises.
- The next ADAPSO symposium will be held in Portland, Ore., May 14-15.
- A two-day course on digital data transmission and its application in business and industry will be presented by the Engineering and Sciences Extension, Univ. of California, San Francisco, May 21-22.
- UCLA Physical Sciences Extension-Engineering Extension will offer a course on Information Systems for Executive Planning and Control, one week, 30 hours of lecture, May 25-29. The instructor will be Prof. Lionello A. Lombardi of MIT.
- The International Instruments, Electronics and Automation Exhibition will be held at Olympia, London, England, May 25-30. Some 700 international firms will present their equipment.



the red carpet's out for you at Decision Systems, inc.

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If you're the special kind of man we seek for Computronics, we will roll out the red carpet to welcome you. We are anxious to meet with qualified engineering and scientific personnel who will welcome the stimulating environment in this rapidly expanding company. Our projects, including a major space program, are long-range and diversified. Computronics has no complicated organizational chart to inhibit your progress as you grow in your job. This is a young company on the move and we wish to talk to men on the move. Please send your resume.

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CIRCLE 99 ON READER CARD

letters

selective non-service

Sir:

Lou Fein's provocative style (Jan., p. 35) compels me to contribute this palatable solution to the delicate problem of determining how and who might be compensated for not working. Let's have none of this nonsense of the two-day week. If we're to do the job, let us do it right—by taking a leaf from the book of academe: the sabbatical.

The idea would be realized in the form of an annual lottery (not unlike that associated with the birth of the military selective service program). Each year, from among all those eligible to participate, names would be drawn, the number of them according to some economic index that would forecast how much people-effort would be required during the forthcoming year. Those fortunate enough to be selected would be paid a sum of money, the amount determined by their regular earnings according to formula; such pay could be accepted only on condition that the recipient retire from the labor force for the entire year for which the grant was made.

ROBERT M. GORDON
Anaheim, California

delayed escalation

Sir:

I was disturbed by the adverse reader comments in the February issue, stemming from the December editorial, "Prayer of a Computer Specialist." We live constantly under a sword, suspended by a thread; I am amazed that many people are insensitive to the frailty of that thread. Human designs of equipment are never 100% foolproof, and neither are the humans involved in the decision-making process.

The possibility of attack by intent, accident, or confusion following President Kennedy's assassination was very real. Who knows how many close calls we may have already had at other times?

By the grace of God, the thread has not broken.

I feel the editorial was in good taste and appropriate. A scientific journal should not have to exclude all reference to God.

DONALD R. NEWMEYER
Norristown, Pennsylvania

Sir:

[The editorial] did not need comment other than a note of passing thanks that some persons are still concerned with the significance of events outside their peculiar business interests. The factor which must be remarked was the letter response.

I fear we have developed a large group of technically trained, uneducated, deliberately unimaginative people who believe that nothing can happen except when properly arranged through "channels" . . .

Our capability for survival depends on flexible independent thinking which responds to facts and situations, rather than organizational doctrines and assessments. May intelligence and Heaven combine to protect us from the people who say, "This cannot be, it isn't in The Plan."

DONALD BAKER MOORE
Stanford Research Institute
Menlo Park, California

with one stone

Sir:

Your December editorial was in bad taste. However, I did not take time to voice my opinion on that matter. But now you subject your readers to "The Language's Prayer" (Feb., p. 79) which causes your at-one-time-excellent periodical to sink to a new low.

MILTON T. AUSTIN JR.
Mauchly Associates Inc.
Fort Washington, Pennsylvania

pirates & thinkers

Sir:

Congratulations on your Feb. editorial, "Wanted: Super-Specialists." This echo, in a trade journal, of the concerns of leading American educators over our excessive emphasis on practical training in the schools, is gratifying indeed.

Perhaps in part because of our relatively recent frontier history, Americans have always taken a particular, almost nationalistic, pride in our international reputation for technical "know-how" or competence in practical endeavors. While we are justified in this pride, too often we have allowed it to deteriorate into smug, at times militant, complacency. This anti-intellectual attitude has frequently reflected itself in the curricula and faculties of American schools at all levels. And a very large part of the American business community has contributed, through their anachronistic hiring policies, to the perpetuation of this unfortunate situation.

Ironically, the business community itself is now awakening to the weaknesses of our largely craft-oriented educational establishment, and the influence of powerful business interests may provide the impetus for long overdue modifications in the schooling of the nation's youth. At least we can hope so. Perhaps such re-orientation will, in decades to come, relieve us of the embarrassment occasioned us by the growing concern of European nations over the pirating of their thinking class by American enterprises.

GARY R. MARTIN
The Bunker-Ramo Corporation
Canoga Park, California

fadac production

Sir:

We have read with interest your article on "The FADAC" (Feb., p. 61). Of particular interest is the statement that Teledyne Systems Corp. of Hawthorne, Calif., was selected by U.S. Army Ordnance in 1961 to manufacture FADAC's and, since, has been the exclusive quantity producer.

We wish to advise you that on April 11, 1963, The Magnavox Co., Urbana, Ill., was awarded a contract by AMC, Frankford Arsenal for a large production quantity of FADAC's. On June 28, 1963, we received an award for a large quantity of memory devices for the FADAC. On Aug. 15, 1963, we received an award for an additional production quantity of FADAC's.

H. A. EMMETT
The Magnavox Company
Urbana, Illinois

Thanks for setting the record straight.

recording of dates

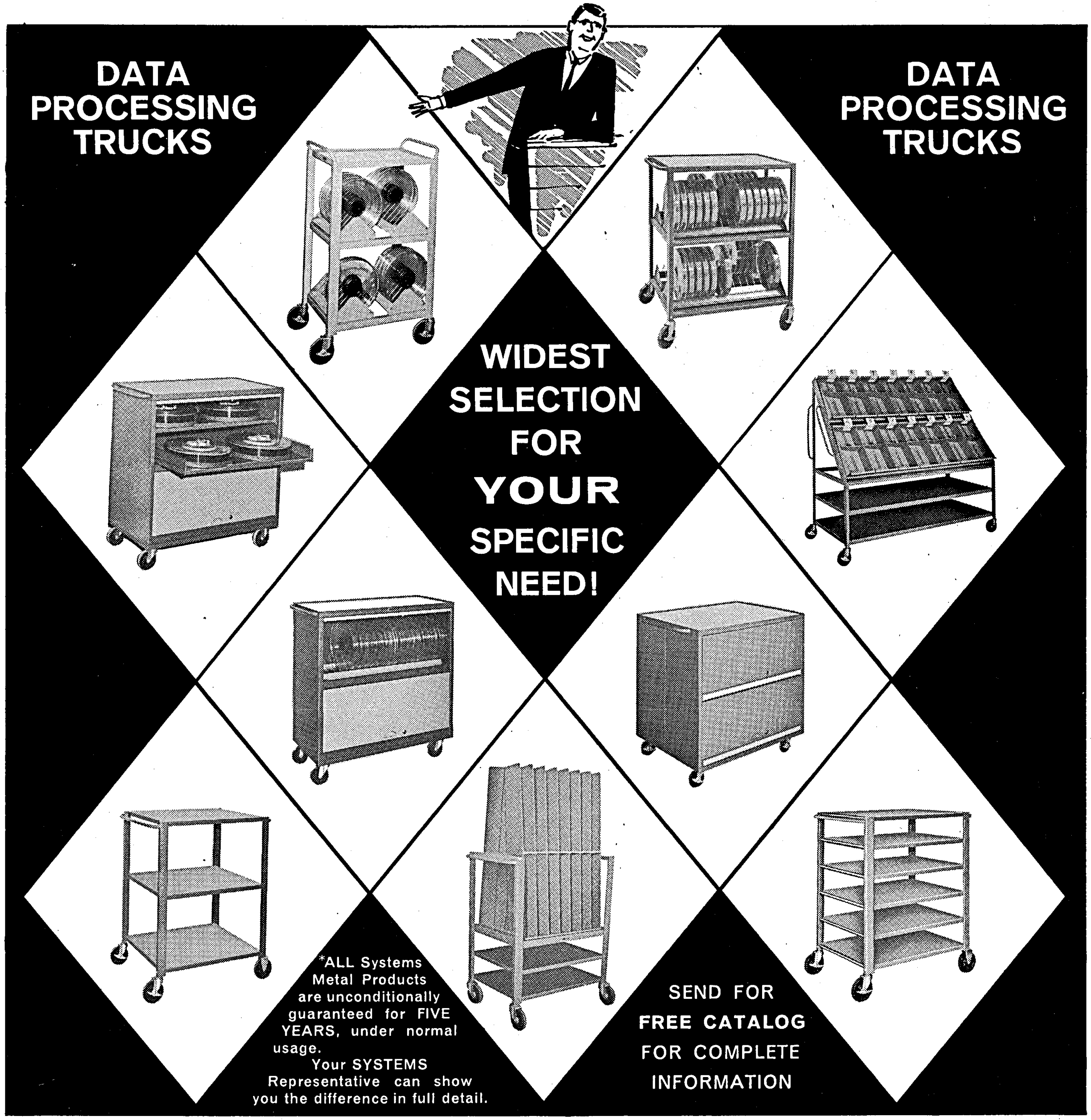
Sir:

Re: Mr. Page's proposal (Feb. letters) to standardize on a sequence of date recording, giving year, month and day (in that order) in a six-digit form, we have been following such a standard on our Personnel Automated Records system for nearly a year.

C. M. GRAVES
American Machine & Foundry Company
New York, New York

DESIGN

makes the difference*



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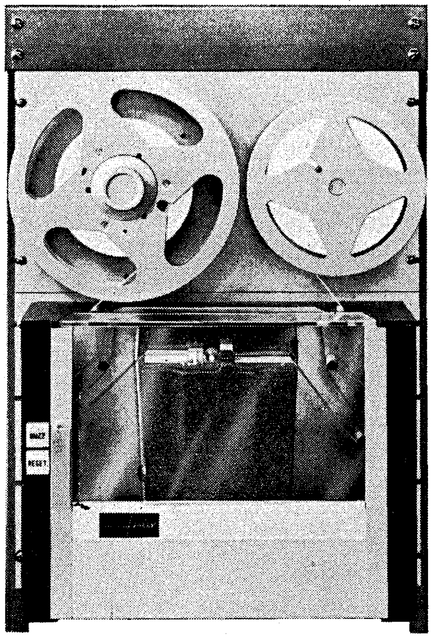
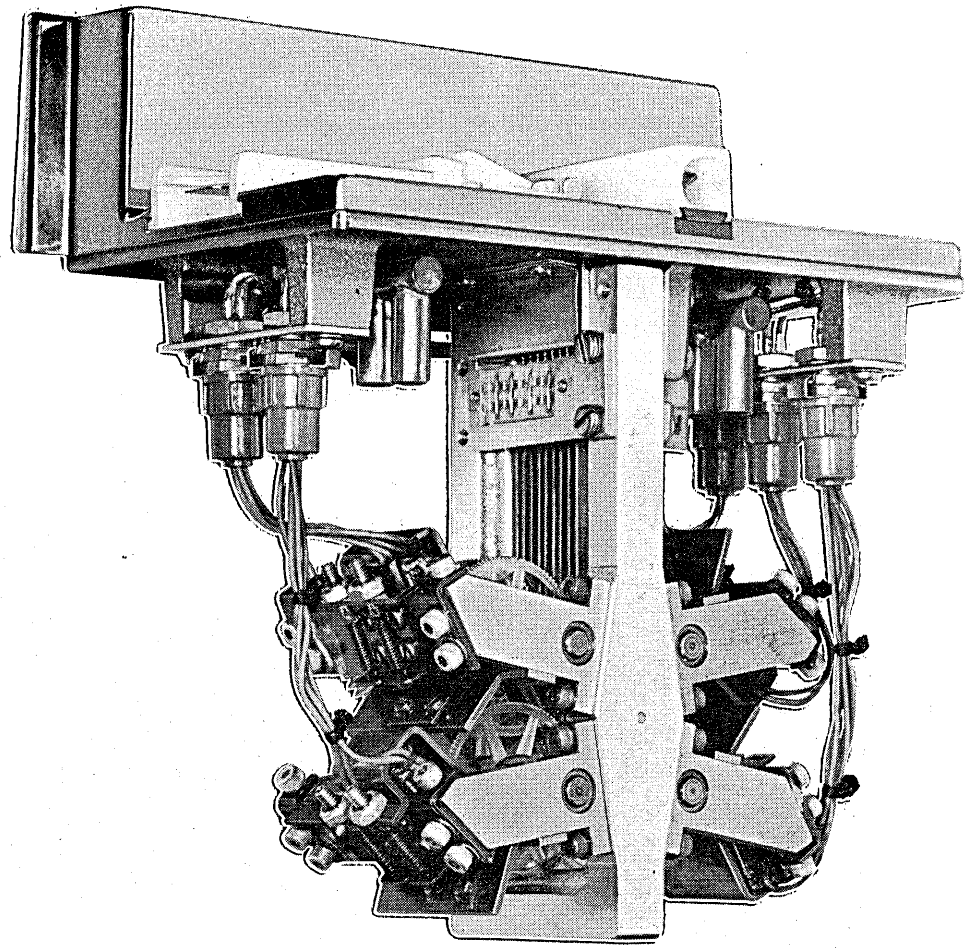
Finest Quality Data Processing Accessories Since 1945

CIRCLE 15 ON READER CARD





You can trust the P-150; it corrects its own mistakes

All of Tally's perforators (over 3,000) have made mistakes. We haven't built a perfect machine and neither has anyone else.

But Tally has built the next best thing—a perforator that can tell when it makes a mistake and can correct it—all at 150 characters per second.

Tally calls this new perforator the P-150. Even before we added the self-correction feature, it was a dependable machine. Now it's by far the industry's most trustworthy high speed perforator.

How You Can Use It

Computer and machine tool programming, photo composing, and many data logging applications demand accurate paper tapes. With the P-150, you don't need to design a system which includes post reading the tape for error or going through a cleanup routine which takes time and more equipment. Instead, you can design around the perforator's accuracy. Tally gives your system these lines to communicate with the perforator: (1) 8 data lines and a sprocket line; (2) a line to introduce the parity test signal; (3) two lines to check parity condition, one odd and one even; (4) a line for advancing tape; (5) a line for reversing tape.

With the P-150 your system can produce clean tape in less time, with less equipment, and at lower cost.

The Price is Right

The cost of the industry's most trustworthy perforator is: mechanism, $2,850; drive electronics, $1,400; tape handler (1,000-foot), $450.

For additional details on how Tally's P-150 perforator can solve your design problem, please write to Tally Corporation, 1310 Mercer Street, Seattle, Washington 98109.

See it at SJCC, #116

TALLY®

CIRCLE 16 ON READER CARD

Until now, there were three ways to break the digital computer speed/cost barrier:

Designation	Add (fixed point)	Multiply (fixed point)	Addressable Memory Size	Price
SDS 910	16 μsec.	248 μsec.	to 16,384 words	$41,000
SDS 920	16 μsec.	32 μsec.	to 16,384 words	$83,000
SDS 9300	1.75 μsec.	7 μsec.	to 32,768 words	$215,000

The new SDS 930 makes four

SDS 930	4 μsec.	8 μsec.	to 32,768 words	$108,000

The SDS 930 is the newest addition to Scientific Data Systems' line of high speed, general purpose computers. It has complete program compatibility with the SDS 910 and 920 (which are now operational in more than seventy-five installations). The 930 instruction list is identical to the 920's. The remarkable 930 speed includes 2 μsec. cycle time and 20 μsec. divide time.

The SDS 930 has one standard and seven optional buffered input/output channels and all I/O channels can operate simultaneously with computation. All SDS 900 Series Computers share these features: all-silicon semi-conductors, buffered input/output, comprehensive software including FORTRAN II and floating point and multi-precision operation. For all the facts about the 930, write . . .

SDS 930

SCIENTIFIC DATA SYSTEMS 1649 Seventeenth St., Santa Monica, Calif.

CIRCLE 17 ON READER CARD

BUSINESS & SCIENCE

45-BANK ON-LINE SYSTEM IS UP FOR GRABS

Several edp manufacturers are breathlessly awaiting the word on a big, several-megabuck on-line savings accounting system for the Savings Banks Trust Co., NYC. Controlled by 126 member banks in NY state, the company has received proposals from several firms for three system configurations. The basic configuration would include 45 banks -- with 2,700,000 savings accounts and 141,000 mortgages -- who have indicated an interest in participating in the system. Other configurations involve larger and lesser numbers of banks (and teller stations).

A recommendation on the proposals is expected this month from consultant John Diebold; a final decision is due this summer. If the member banks go along with the proposed system, it would be in operation within two years. So far, only three U.S. savings banks have on-line systems -- all developed by Teleregister.

FORTRAN VI POPS UP; SHOVED BACK DOWN

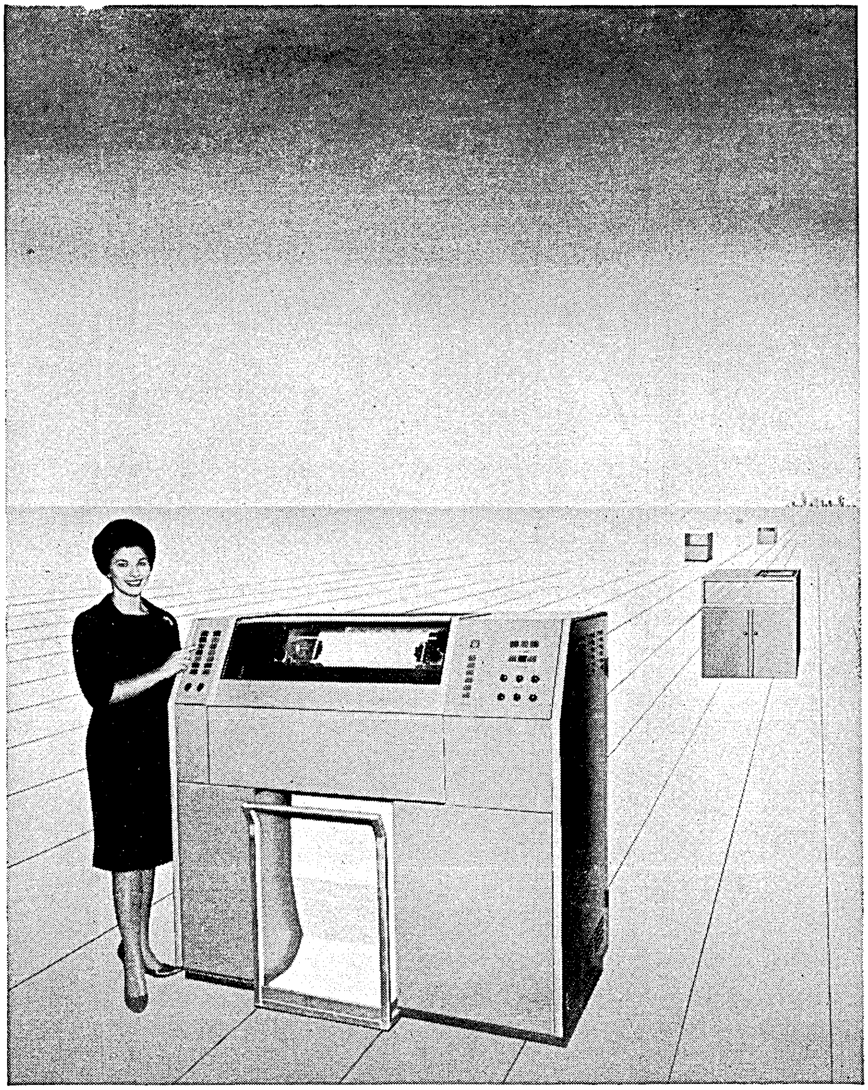
That new programming language which came out of a six-man IBM/SHARE committee and announced at the recent SHARE meeting seems to have been less than a resounding success. Called variously "Sundial" (changes very minute), FOALBOL (combines FORTRAN, ALGOL and COBOL), FORTRAN VI, the new language is said to contain everything but the kitchen sink . . . is supposed to solve the problems of scientific, business, command and control users . . . you name it. It was probably developed as the language for IBM's new product line.

One reviewer described it as "a professional programmer's language developed by people who haven't seen an applied program for five years. I'd love to use it, but I run an open shop. Several hundred jobs a day keeps me from being too academic." The language was described as too far from FORTRAN IV to be teachable, too close to be new.

Evidently sharing some of these doubts, SHARE reportedly sent the language back to IBM with the recommendation that it be implemented, tested . . . "and then we'll see."

75-100 MEGABUCK INVESTMENT GENERATES 2 ON-LINE DISPLAYS

After 10 years and an investment of $75-100 million in automated displays, only two are operating, DOD official Dr. Ruth M. Davis told the Society for Information Display in San Diego in February. And she commented on the tendency to allow one effort to duplicate the mistakes of others . . . while not



allowing any one contracting company to duplicate its own errors.

Of the eight major efforts, one is being removed, two have been completely re-oriented. Characterizing the display field as "challenging, rapidly growing, and relatively ineffective . . . perhaps 10 years behind the computer field, . . ." Dr. Davis stressed the need for improved computer-to-display techniques and hardware . . . the importance of viewing the display as the core of an information system, not as a computer peripheral.

The two-day conference drew over 600 registrants, 50 new members and 25 exhibiting companies. Next symposium is scheduled for Washington, D.C., Oct. 1-2.

RCA LOSES RACE

RCA's new random access mass memory has lost its original acronym, RACE. It seems another firm uses that for a piece of obsolete test gear, wants $100K for rights. RCA officials reportedly turned down field appeals to substitute MARS, allegedly the acronym of a new IBM mass memory.

CSC DEVELOPS PARALLEL STORED LOGIC COMPUTER

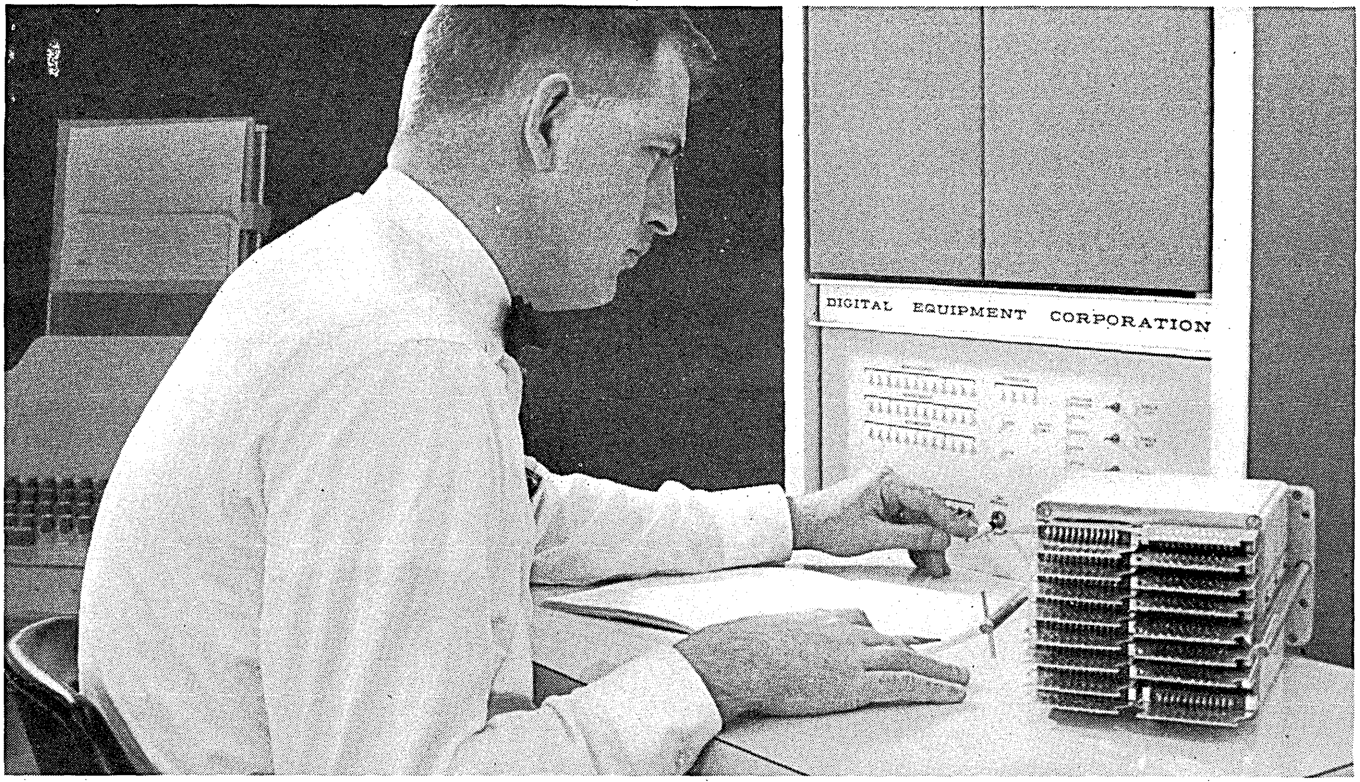
Consolidated Systems Corp., L.A.-area subsidiary of Allis-Chalmers and Bell & Howell, has come up with a new all-parallel microprogrammed computer. The new machine features a 1024-word (32 bits) fixed store of ferrite slugs with a ½-usec cycle time. Working core memory is 4096 words with a cycle time of six usec and access time of two usec. The first unit is scheduled for a satellite tracking system, but the company feels it will serve well as a process control computer. The computer is reportedly competitive with machines in the SDS 920 class.

LIVERMORE'S 6600 DELIVERY DELAYED 'TIL MAY

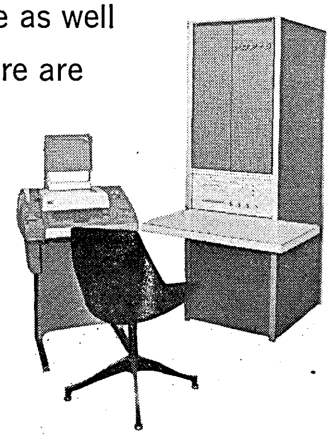
That 6600 scheduled for February for the Lawrence Radiation Lab in Livermore, Calif., is now due to be installed in May. The system configuration has been upped from 64-128K of one-usec cycle memory, and three Bryant discs (total capacity: 24-million characters), instead of two. Meanwhile, we understand that another 6600 has been ordered by CERN, the European nuclear research institution.

RUMORS AND RAW RANDOM DATA

We hear that Philco will be coming out with a new scientific machine -- the 9000 series -- this summer . . . Burroughs will be getting into the election prediction business this year. CEIR is supposed to handle the ugly details on a B 5000 out of NYC . . . Fine-Kettle-of-Fish Dept.: As of early March, only one major manufacturer had signed up for space at the '64 ACM conference . . .Is it true that the 465L, SAC's command & control system, has been written off as a failure? . . . ASA's X3 has approved for publication proposed American standards for paper tape code, one-inch paper tape, mag tape and punched card (physical), as well as two EIA (Electronic Industries Assn.) standards relating to the use of paper tape for numerically controlled machine tools . . . ACM membership, evidently not seriously hurt by the recent dues hike, stood at 8,080 in mid-February, less than 1,000 drop from last year at this time . . . An Eastern firm, Computer Clearinghouse, currently lists for sale the equivalent computing power of the entire U.S. in '56. They're early Univacs, 650's, etc.



You can own the PDP-5 computer for what a core memory alone used to cost: $27,000. This general purpose computer is ideal for scientific computations, system and process control, and data collection and reduction. Don't let the low price fool you. The PDP-5 has features and capabilities many higher priced computers wish they had. A six-microsecond memory cycle and fully parallel processing, for example, permit a 55,555 additions-per-second computation rate as well as real-time data compilation and processing or recording. Then there are the 4096-word random access magnetic core memory (or 1024-word memory for $3,000 less), 12-bit word length, and 24-bit arithmetic. Add to these a two-megacycle bit input via built-in data channel, program interrupt for input-output devices, and a complete software package—including FORTRAN. Price includes keyboard-printer, paper tape reader, and punch. Impressed? Then let's get together soon and talk computers.



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CIRCLE 19 ON READER CARD

WASHINGTON REPORT

<u>NEW EDP SURVEY IN THE WORKS</u>

BuBudget is preparing its fourth annual report on computers in government agencies. Expected to be available in 30-60 days, this year's report will, for the first time, list information on different applications of the government computer corps. Quickest way to get a copy will likely be through the House Post Office & Civil Service committee, which has become the prime source of most statistical information on government edp equipment.

<u>COMPUTER MAKERS GO SCHIZOID OVER H.R. 9548</u>

H.R. 9548, the bill sponsored by Rep. Multer (Dem., N.Y.) which would prevent banks from offering computing services to non-banking clients, has fanned a two-sided controversy in which computer makers find themselves somewhat painfully with a foot in both camps.

Low-cost machine time offered on bank-operated hardware has cut into the potential market for new computers in many locales, it's admitted <u>sotto voce</u> by most manufacturers. Their reaction varies from academic concern to strident alarm. "Bank competition is playing havoc with us right now in any city of consequence," claims one computer sales executive. Others see bank time-sales as potentially dangerous, but not yet so.

The other side of the coin is that banks have been, and continue to be, among the most open-pursed of computer customers. (Indeed, sales to banks have often been cinched by the argument that excess machine time can readily be resold outside). Fear of damaging these delicate sales sensibilities was one reason computer manufacturers were conspicuous by their absence at two days of hearings on the Multer bill, recently concluded by a House Banking and Currency subcommittee.

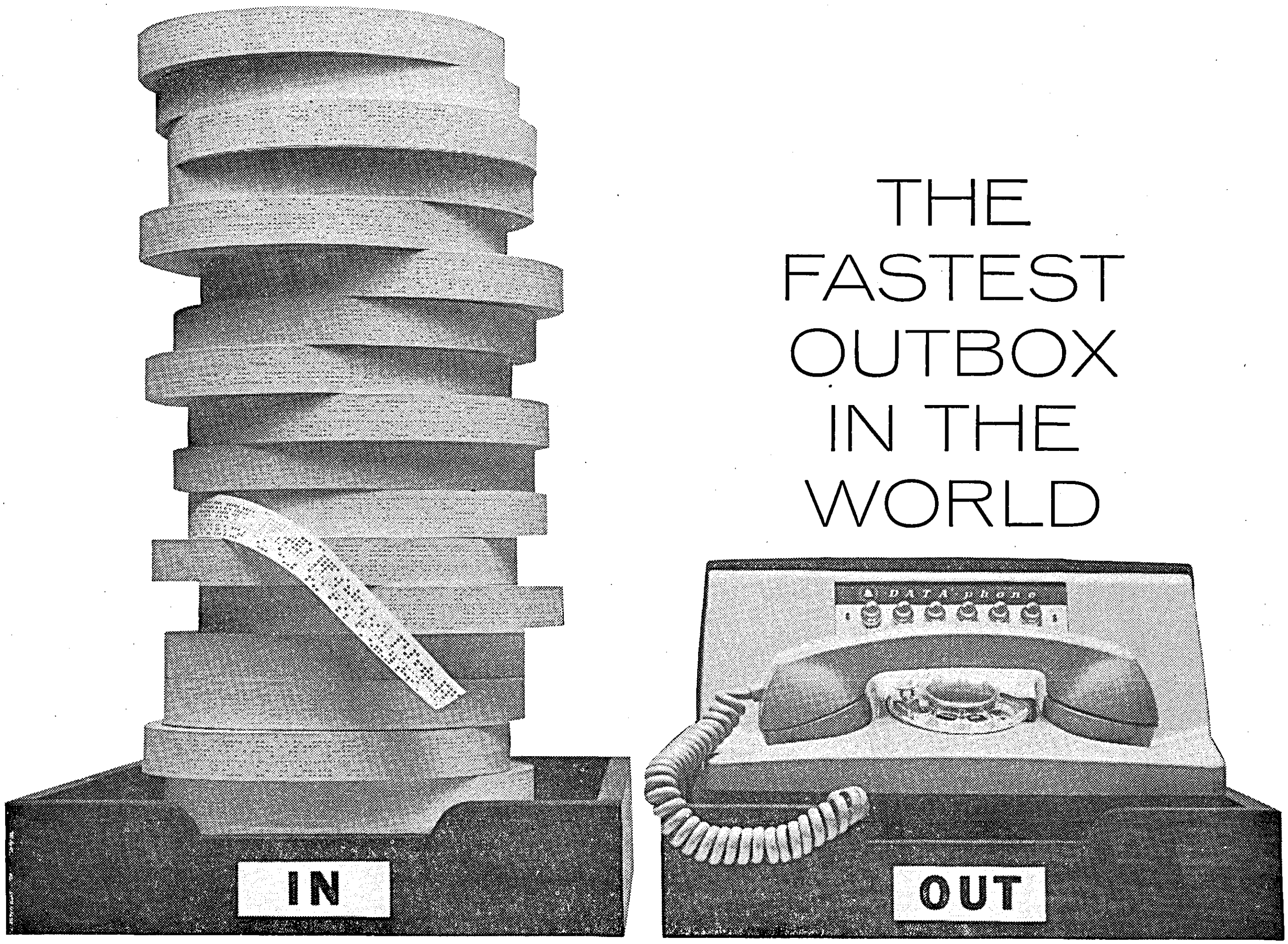
At the hearings banking representatives argued H.R. 9548 would prevent small and medium banks from enjoying the fruit of automation, that it interdicted competition unnecessarily and that edp services were a legitimate extension of normal banking services.

Witnesses for the bill, who included an independent banker, an accountant and a spokesman for independent service bureaus, raised cries of unfair, unnecessary and illegal competition. The large banks, they argued, can in effect blackjack smaller banks and commercial clients into tying into their computing systems through their control of capital funds. It was also claimed that the banks were illegally risking depositer funds in such a risky venture as establishment of an edp center, and that any bank could automate to meet its own needs from the size spread of equipment presently available.

Interrogation by committee members was generally

Continued on page 135

THE FASTEST OUTBOX IN THE WORLD



Bell System DATA-PHONE service can tie your organization together efficiently and economically with a communications system that's thousands of times faster than the mail—and 16 times faster than people can talk.

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CIRCLE 20 ON READER CARD

EDITOR'S READOUT

COMPETITION AND SELF-RELIANCE

They laughed when the tinny piano began tinkling out its ricky-ticky tunes, while the boys in the sincere suits sang along, "Pack up your troubles in your old kit bag, T. J. Watson's on his way."

Today, they're dancing to that tune, the score of one of the biggest hits on the American commercial scene.

We're talking, of course, about IBM and its astonishing rise to almost overwhelming predominance in an industry which has been often labeled as "fiercely competitive."

Some people forget that IBM didn't start out on top in the computer game. The man-in-the-street's first name for computers was "UNIVAC." But the company that couldn't decide at first whether to manufacture two or three of its first commercial machines has made up for that momentary indecisiveness. Today it controls what is generally estimated as 80% of the commercial market . . . perhaps even more of the fat federal government market (for '64, an estimated $704-million, excluding "military operational and classified uses)."

Even more important, the general term for computers is now "IBM machine." People learn "IBM." They become not tab operators, but IBM operators.

"Where did all them blankety-blank Injuns come from?"

So how did all this happen? A lot of people would like to know. The easiest explanation: "They got there the firstest with the mostest." This appears to be a bit over-simplified in view of the comment by one widely recognized computer expert who says, "IBM always has the second best computer."

Another answer, equally general and dissatisfying, says simply "Marketing." Pinned down a little, it offers more insight, however, than the first phrase.

Students of the computer scene point, first of all, to a dedication and a drive which has sometimes been compared to that of the Marine Corps. This was coupled with a confidence in marketing prowess expressed by the belief that the company could swap product lines with Univac and still maintain its edge. Then they point out the expert IBM exploitation of its solid punched card market, most of whom have graduated into computer customers. This after several years of close ties with IBM, which has often helped its customers get their jobs. And, points out one old-timer, "IBM nearly always knew more about the tab equipment and the job than their customers."

This certainly helps to account for the loyalty and allegiance which has made IBM an almost automatic choice amongst prospects, many of whom simply don't bother to look any place else.

When computers came along, and IBM no longer knew more than its customers, they went out and hired a pack of Ph.D.'s, called them applied science representatives, and turned them loose on the customers.

Another factor is the manner in which IBM has won friends and influenced people among the influential – the *top* top management people, who are given extensive tours of impressive facilities. Emphasized are training, large staffs of support personnel . . . plus a casual glimpse of an assembly line in passing. Hardware is disdained, capabilities subtly underlined. "That's the way to market," says one observer.

The facts of life

But whatever the reasons, the IBM domination is an established fact of life. The big questions are: 1) Does this domination constitute a healthy situation for the industry? 2) If not, what can be done about it? First things first. Despite the anguished howls of the competition, there is no clear-cut agreement in the industry at large that the domination is unhealthy. And the most objective look at the "problem" indicates that it offers both benefit and bane.

One positive result lies in the land of languages. If IBM announces and implements a new language – say FORTRAN – for its whole family . . . one which is widely used by the IBM customer, a *de facto* standard is created. The emulation of the standard language by the competition is done without the equivalent design costs or risk of failure. The predominant usage of one size tape, one packing density, one punched card width, etc., etc., obviously helps to force standards.

Whether the standards are the best may be beside the point, in light of the natural sloth-like progress of standards work without such artificial stimulus.

On the dark side of the picture, the domination can mean the slowing of major technological advances: why bring out something newer and better when what is currently in the production pipe (with unit costs falling as volume rises), is still drawing the customers and dollars? More subtly, attempts by the minority to announce something truly dramatic or different are discouraged . . . it doesn't have a chance unless it fits the pre-fabricated mold. (It might be added that some people still haven't made proper use of their first generation machines. An increased rate of obsolescence – like that in automobiles – is of dubious value).

Some people feel that the man who buys IBM blindly – or out of allegiance – is denying his allegiance to his company by not making available to his firm the complete range of alternatives. They point to the plain old-fashioned common sense of having more than one source of supply.

The happy mixer

The sophisticated user likes to feel that he doesn't have to depend upon IBM, or on any one manufacturer. One user who mixes equipment feels he can afford to because he's developed a staff which can handle the mix – design and specify converters, develop necessary software. "Why should I buy a 1401 if a buffered Burroughs computer will do the job better?" he asks.

Another IBM customer says, "IBM domination a problem? Not as long as we dominate them." He says that the service has been good, and adds, "There's nothing wrong with superiority."

Others point out that not all IBM customers are in a position to wangle all of the support goodies and services which can be made available. One user complains that IBM's standard lease agreement makes no room for acceptance tests, "and they won't accept any suggested modifications. They tell *us* when rental starts." Encouraged by his top management to open the doors to the competition, this man is now running acceptance tests on a non-IBM computer.

The fact remains, however, that – for most people, including consultants – IBM remains the "easy" buy. If a non-IBM installation fails, there's hell to pay, because top management could have told them they went to the wrong supplier in the first place. It seems to boil down to a question of the level of competence and confidence in its own skills and abilities on the part of dp management.

As we suggested earlier, there seems to be no nice, black-and-white answer to the question of whether or not IBM domination constitutes a problem. But assuming for the moment that – for the customer and the industry as a whole – the harmful results outweigh the healthy, what can be done?

Open the door, Richard

One suggested solution: making competitive manufacturers solve benchmark problems. Others want to see hardware, software and post-sales services priced separately. This, they say, will prevent give-away services smaller manufacturers can't afford. IBM, the argument goes, could no more afford to cut prices here than it can in hardware, where a slash might make them dominant to the exclusion of everybody (Major competitors, anonymously off-the-record, agree that IBM could wipe them out if it wanted to).

Competitors agree that IBM has earned its spot at the top of the heap. But the point is not so much whether IBM deserves its domination, whether it's good or bad . . . but whether a customer committed to one supplier isn't handcuffing himself, weakening his position to negotiate for the best.

By straightening his own house . . . by developing documentation, establishing ways to measure an installation's performance, and through programmer discipline . . . the user can develop the self-reliance which permits him to look a manufacturer right in the eye and insist on more than average performance. He can demand the kind of compatibility which will permit him to change suppliers if the next step up or next generation doesn't meet his needs.

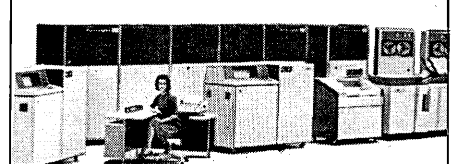
This isn't going to change overnight the competitive complexion of the industry. It doesn't mean that three companies will split 90% of the market. But it will foster the kind of hungry, healthy competition which can help accelerate the advancement of the computer profession . . . and remove the handcuffs from an awful lot of users.

We think it will happen. As customers mature, as the IBM competition gets more savvy, as standardization and compatibility and programming languages develop, the domination will dwindle. And if IBM welcomes competition as a healthy impetus, who can argue?

Multi-Processing

they're starting to copy us

It seems that in proving to business and government that multi-processing really works, we convinced the competition too! They used to knock us. Now they're knocking themselves out trying to develop multi-processors of their own. But remember this: only the Burroughs B 200, B 5000 and D 825 are right now routinely running production programs for their users, utilizing effective multi-processing. The proof is yours for the asking.



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CIRCLE 21 ON READER CARD

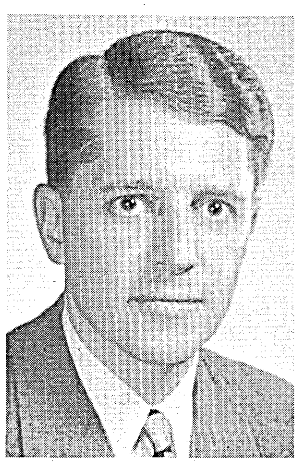
COMPUTERS AND FALSE ECONOMICS

diminishing costs, rising salaries

by MARK HALPERN

The quality of fantasy that pervades most discussions of computer costs is due largely to one vestigial habit of mind that most programmers have not yet thrown off—an exaggerated respect for computer time. The writer is enough of an old-timer to remember when one approached a computer with something close to awe, and only after having done at one's desk everything that could possibly save a second of machine time. A pair of us, green beginners just out of a two-week course on SAP language, were running our first program on an early 704, and got carried away when answers began appearing at the on-line printer. Forgetting our plan to take just a few lines on the printer and then switch to outputting on tape, we stood transfixed at the printer for more than 20 minutes while the results of perhaps 40 seconds' worth of computation were slowly doled out by that miserable old clunker, the 716. When the bill reached our boss (one R. W. Bemer), he took our heads, one to a hand, and brought them smartly together—the act, we decided, of a mind unhinged by grief. The ringing in our ears subsided; the idea that computer time costs money remained. Such was programmer-training in the Old Days, and we survived, with a slight loss of response to tones above 15,000 cycles that would have come in the course of nature anyway.

We venture on this personal note not only for its pastoral charm, but to make the point that we have been taught a proper respect for money. It is, in fact, this very respect that prompted the assertion that most programmers have an exaggerated respect for computer time. For computer time, though still not free, has greatly diminished in cost, while other expenditures involved in computer usage have risen almost as sharply as it has dropped. Nevertheless, measurements of computer-usage costs, whether relative ("High School Girl Develops Compiler 3.26 Times Faster than FORTRAN!") or absolute ("New Machine Brings



Mr. Halpern leads a group currently engaged in developing a meta-language processor at Lockheed Missiles & Space Co., Palo Alto, Calif. He entered the computer field with IBM's Programming Research and Programming Systems departments. He is a member of the ASA X3.4.2 language standards subcommittee, and is writing a book, "The Craft of Programming." He holds degrees from City College of New York and Columbia Univ.

Costs Down to Millibuck per Megastatement!"), are almost always confined to machine-time cost. The temptation to shut out reality here is the usual one—it's so ugly. Once on the machine, we can time a program to the microsecond, if necessary, and compute its machine-time cost to the fraction of a mill. The question of cost outside the machine room is just such a messy one as we got into programming hoping to avoid. Unlogical, unquantifiable, subjective—like life, hopelessly unscientific. So we retreat to a world safe for the programming temperament where (when we are not spending our hours quarrelling with the Computer Center over an apparent 30-second overcharge on our last run) we write papers showing how a compiler given input on Moebius strips, algebraic statements in Runic notation, and arrays stored boustrophedon could shave a millisecond off average compiling time.

All this while machine costs have gone down by more than an order of magnitude since 704 days, and weren't very high even then. The idea that machine time is the great cost in computer usage springs from several roots, among them the fact that it is—or was until quite recently—so awkwardly packaged and distributed. The smallest unit it could be bought in was the computer-full. Few single users might want more than five dollar's worth of computing at a time but we were all very much aware of how much the machine cost per hour, month, and year, and treated it with these national-debt-size figures in mind. It was as if every customer of a supermarket had to know and care about the financing behind the store when he came in to shop, and felt he had to sprint down the aisles while gathering the goods, out of respect for a six-figure mortgage. Even then we knew better, as witness this excerpt from the classic paper that introduced FORTRAN to the world:

> . . . it was known that about two-thirds of the cost of solving most scientific and engineering problems on large computers was that of problem preparation. [1]

The system announced in that paper, and a few others since, have helped to cut down on the time formerly spent on problem preparation, certainly, but even the most enthusiastic champions of these compilers would hardly claim that they have had as great an effect in that area as hardware progress has had on machine-time cost. Further, those doing programming today, like almost all scientific/technical people, are higher paid than their counterparts of 10 years ago. In short, the *relative* economic unimportance of machine time stands out even more vividly today than it did to the authors of FORTRAN back in 1954.

In a round-about way, however, FORTRAN may bear a share of responsibility for the inordinate stress on computer-time economics that is still a major theme in our technical literature. For some very special reasons, the authors of FORTRAN were deeply interested in the optimization of the coding they compiled. The first was the widespread skepticism about compilers they saw around them—and not only outside IBM. The few compilers that had been turned out before 1954 produced coding that was seldom good, often very bad; many tight-coding virtuosos (and practically all programmers, of necessity, were such) took one pained look and swore they'd never use one. To establish the compiler's right to exist, the FORTRAN group had to show, at any cost, that a compiler *could* produce tight coding. As to whether a compiler *should* go all out to compile the best possible object program, they didn't say; the one comment on the subject in the paper at hand sounds rather negative:

> The generality and complexity of some of the techniques employed [by FORTRAN] to achieve efficient output programs may often be superfluous in many common applications. However, the use of such techniques should enable the FORTRAN system to produce efficient programs for important problems which involve complex and unusual procedures.[2]

A second reason for making the FORTRAN compiler as sophisticated as it is was simply that its authors are superb craftsmen who delight in exercising their powers, as they freely admit:

> In any case the intellectual satisfaction of having formulated and solved some difficult problems of translation and the knowledge and experience acquired in the process are themselves almost a sufficient reward for the long effort expended on the FORTRAN project.[3]

Whatever the reasons, they did show that a compiler could produce good coding. In doing so, they set up a target for various marksmen. As the fastest gun in the west, beating them became the dream of every kid programmer in the country—later, the world. (Also, and this must have given them a few wry laughs, many of the previous skeptics passed over their achievement as if they had always known a compiler could produce good coding, and turned to complaining about compiling time). In one way, the kids have succeeded in taking the crown away from FORTRAN. They have, for one thing, turned out algebraic compilers that compile any program, and execute some, faster than FORTRAN—the former due largely to their invariable omission of the bulk of FORTRAN's optimization, the latter due largely to their restriction of test programs to those that offer little for FORTRAN's optimization routines to get their teeth into. The kids have also beaten FORTRAN in the publicity race.

The FORTRAN authors—how many of the 13 can you name?[4]—have been so little interested in the hurly-burly of conventions, committees and getting into print that, for most of them, the paper in which they announced FORTRAN represent the only occasion on which their name appears in print. (This may be a world record for saying nothing unless you have something to say). One would hardly remember them at all, were it not that the compiler they produced is the most important ever written, and the workhorse of the programming world.

The question left unanswered by the authors of FORTRAN, concerning the desirability of applying its full optimization machinery to every FORTRAN source program, remains open, though. The writer, following the hint from FORTRAN's authors quoted just above, believes that it is not advisable. Reflect that the justification for spending the compiling time necessary to make FORTRAN's object-time optimization will depend on:

(1) The size of the source program;

(2) The asymmetry of flow of the source problem; i.e., the existence of paths of flow of such relative frequency that substantial savings can be made by systematically shifting index-register storing and loading instructions from them to other paths; and

(3) The value of the expression $\frac{N_C P_C}{N_E S_E}$, where N_C =

[1]J. W. Backus *et al.*, "The FORTRAN Automatic Coding System," *Proceedings of the Western Joint Computer Conference*, Feb. 1957. Quotations in this article are taken from the reprinting in *IBM Customer Engineering Manual of Instruction: FORTRAN I, II, and 709*, dated 1959. The quotation to which this note is appended is on p. 51.

[2]Ibid., p. 61.

[3]Ibid., p. 61.

[4]J. W. Backus, R. J. Beeber, S. Best, R. Goldberg, L. M. Haibt, H. L. Herrick, R. A. Nelson, D. Sayre, P. B. Sheridan, H. Stern, I. Ziller, R. A. Hughes, R. Nutt.

the number of compilations required, on the average, before a satisfactory object program is produced; P_C = the price paid at each such compilation for optimizing the object program; N_E = the number of times FORTRAN object programs are executed, on the average; and S_E = the savings realized at each such execution because the program has been optimized.

For each of these three dimensions there is clearly some critical value below which the optimization process will not be worth its price. What these values are we do not know, and for (1) and (2) it may be so difficult to give even an approximate answer as to make them useless as practical guides. For (3) it may be worthwhile to spend some time gathering statistics. The importance of establishing realistic values for the terms N_C and N_E is to be stressed; the latter is, we believe, commonly overestimated, while the former is often ignored altogether. It is a commonplace in formulas for measuring the effectiveness of programming systems to start recording time and cost with the first wholly successful compilation of a test program. This may spring from a feeling that a compilation failure due to programmer error, as most are, cannot in fairness be charged against the compiler. This is magnanimous, but silly; we are not assigning guilt, but keeping books. Money thrown out on optimizing an object program that cannot be used—for whatever reason—is a cost properly chargeable to the optimization process. N_C, commonly taken as 1, is actually greater, we suggest; somewhere between 2 and 3 seems right to us. Guesses are neither here nor there; what matters is that statistics could very easily be gathered toward evaluating it to any usable precision. N_E, on the other hand, we believe to be commonly over-valued. The pitfall causing this error, it seems, is that programmers don't always regard a re-compilation made for the purpose of cleaning up an already running program as a "real" compilation; they regard it as much like the loading of an SOS SQUOZE deck with a few alter cards, or a FAP update-reassembly—a kind of trivial revision of an existing assembly that can be done practically at tape speed. But FORTRAN knows nothing of "trivial" re-compilation; it gives every job its all. If this fact is kept in mind, we think, N_E will take on a rather lower value than one tends to give it at first thought.

We said earlier that some of the skeptics who began by denying that compilers could produce good coding quickly became interested in compiling time above all things, and had at FORTRAN on that count. These admirably versatile critics are not much heard from any more. What has gotten them off FORTRAN's back is neither an onset of wisdom on their part, nor any change of heart on FORTRAN's. The peacemaker has been the 32K core memory and the two usec cycle time. The great speeding up of the compiler due to its accommodation in core memory, particularly, with consequent liberation from the notorious "ping-ponging" of tables from drum to core and back again, has practically ended all interest in the question. This is to be regretted because the question is not really settled. The proportion of compiling time devoted by FORTRAN to optimization is unchanged, even though the absolute times involved have dropped so greatly since 704 days. And if, as the FORTRAN authors themselves seem prepared to discover, much or most of that optimization is uncompensated for by savings realized later during execution, then the proportion of compilation time now wasted is just as great, though not so important to any one FORTRAN user.

But we were speaking of the relative unimportance of machine time. Not only has the price of computer time gone down from approximately \$4.50 per million instructions (704) to approximately 30 cents per million (7094),[5] and not only have programmers' salaries gone up by something like 40% in the period bounded by those two machines, but—and this I believe to be most important of all—the kind of value to be placed on computer output has changed sharply. Whole industries are already dependent on regular and accurate computer output for their day-to-day survival; chains of events we seldom bother to trace from first link to last are contingent on such output.

This has long been the case in the aerospace industry, where the writer is employed; it has become true of banking and oil-refining; it is in process of becoming true of many other sectors of our lives. As the computer is accepted, it becomes a necessity; vast systems are radically revamped to permit the computer to work efficiently, and thereupon it becomes impossible to do the job the old way, or any other way. The programmer becomes a necessary part of every group, and computer turn-around-time the pacing factor in many projects. The writer has often observed the following scene, with slightly varying details: a programmer losing his temper on the phone, trying to discover what's become of last night's input; behind him the engineer or physicist who needs the output to complete a report; behind *him* (at least figuratively) a project leader or department manager who needs the report to back up a proposal to one of the armed services. The output is late, or lost, because a slight breakdown has occurred in the elaborate procedure set up to ensure that the machine is approached only by its professional handlers, and thus used with maximum efficiency. The points of potential breakdown are so numerous that it is hard to account for the successful runs: dropped decks, misunderstood instructions, wrong program-stops recorded by operators trying to convert binary to octal after six hours of graveyard-shift, wrong tapes mounted, master files scratched—any programmer could fill up this page and the next. Miraculously, though, most runs are successful.

Even without the normal proportion of unsuccessful runs, the near-universal acceptance of the rule that computer utilization efficiency always comes first and customer service (practically synonymous with minimum turn-around time) a poor second, is a piece of economic folly. A distinction must be made, certainly, between routine production programs whose output must be ready at 9:00 every morning but will make no-one richer or happier by being ready a minute earlier, and the program in check-out or in support of R and D work. What is being urged here is that this latter class of effort is generally one in which the machine-time costs are trivial compared to the aggregate salaries of the men waiting for output, to say nothing of the value of the project they are on. To give such jobs the handling they deserve would cause the computer to be used less efficiently, no question; and rightly so. It is not reasonable that a \$5-a-shot machine be permitted to waste the time of \$40-a-day men. If the computer had heads, it might be time to clap a pair of them together. ■

[5]The average instruction = 2 cycles = 24 $\mu s \cong$ 40,000 instructions/second; price at \$600/hour $\cong$ 17¢/second $\cong$ \$4.50/million instructions. The 7094 average instruction = 1.5 cycles = 3 μs = 333,333 instructions/second; price at \$360/hour = 10¢/second = 30¢/million instructions.

CONDENSED COMPUTER CHARACTERISTICS

by CHARLES W. ADAMS

Four years ago, when Adams Associates first compiled its Computer Characteristics Chart, it contained information on only 43 general-purpose computers, all that were then commercially available in the United States. But each year the number increased and the volume mounted. And each year, with our permission, *Datamation* faithfully reproduced the then-current issue of the Computer Characteristics Quarterly, devoting more and more pages to it as the 28 solid-state systems reprinted in November 1960—the other 15 were vacuum-tube machines—swelled to 75 by November 1963.

About that time it became apparent to ourselves and *Datamation* Editor Bob Forest that reproducing this mushrooming volume of data was a problem that had to be faced. We finally decided on what is perhaps the most feasible solution—to reprint every three months in *Datamation* the characteristics of the new solid-state general-purpose computers added to Section I of each issue of the Quarterly, along with any remarks about them that appear to be warranted.

Meanwhile, those who have followed the steady growth of the number of competitive computers produced in this country and abroad will be interested in knowing that the Adams Associates Computer Characteristics Quarterly for March 1964 contains information not only on the four computers listed below but also on an additional 81 solid-state general-purpose systems, 19 intended for process control and other specialized applications, 43 developed for military purposes, 76 foreign-built computers, and 16 vacuum-tube machines, most of them obsolescent but still in service. Thus, 239 computers are catalogued in the current issue of the Quarterly.

The many *Datamation* readers who have looked forward to the annual reprinting of Section I each November and of Sections II, III and IV each May can take consolation from the fact that *new* machines will now appear more currently in *Datamation*, and that for the modest sum of $10 a year they can receive every three months, in a choice of two convenient formats, a fully updated compilation which will keep them abreast of changes in the design and manufacture of computing equipment throughout the free world. ■

	Monthly Rental Typical Range	*First Delivery* Month and Year	*Processor Speed* Complete Add Time in Microseconds	Storage Cycle Time in Microseconds	*Internal Storage* Capacity in Words	Type	*Logic* Word Size Instr. Addresses	*Magnetic Tape* Thousands of Characters per Second	Buffering	Maximum Units Attachable	*Random Access File* Capacity	Access Time in Milliseconds	*Peripheral Devices* Cards per Minute In — Out	Paper Tape Characters per Second In — Out	Printer Lines per Minute	Off-line Equipment	*Other Features* Program Interrupt	Index Registers	Indirect Addressing	Floating-point Arith.	Console Typewriter	*Software* Algebraic Compiler	Business Compiler
GENERAL ELECTRIC 435	$11,500 (8-25)	12/64	8.8	2.7	32K	core	24b —[G]	15-83	MRWC	56	94M[L]	199	900 100	500 150	1200	—	√	√[T]	√	—	I/O	√[X]	√[Y]
GENERAL ELECTRIC 425	$9,500 (6-20)	6/64	16	5.1	32K	core	24b —[G]	15-83	MRWC	56	194M[L]	199	900 100	500 150	1200	—	√	√[T]	√	—	I/O	√[X]	√[Y]
HONEYWELL 200	$5,000[A] (3-10)	7/64	44[C]	2[D]	2-32K	core	1a[F] 2	20-90[H]	MRWC	64	806M[L]	110	800 250	500 110	1260	same	√	6	√	—	I/O	3/65	3/65
SCIENTIFIC DATA SDS 930	$4,320[A] (3.2-8)	6/64	3.85	1.93	4-32K 16-96K	core drum	— 24b 1	15-96[H]	MRWC	32	— —		250[N] 125	300 60	300	910	√	1	√	—	I/O	6/64[X]	—

GENERAL ELECTRIC 435: G. Binary, decimal, single, double, triple and quadruple arithmetic instructions included. L. Up to 28 disc storage units with 23.5 million characters each available. T. Each word of memory can be used as an index register. X. FORTRAN. Y. COBOL.

GENERAL ELECTRIC 425: G. Binary, decimal, single, double, triple and quadruple arithmetic instructions. L. Up to 28 disc storage units with 23.5 million characters each available. T. Each word of memory can be used as an index register. X. FORTRAN. Y. COBOL.

HONEYWELL 200: A. Monthly rental for card system is $3,160. C. Add time assumes two five-character fields. D. Control memory access time of .25 microseconds. F. Variable-length instructions operate on variable-length data fields. H. One-half and three-quarter inch tape units available. L. Up to 64 random access drums, each with 2.6M character capacity and 25 microseconds average access time also available.

SCIENTIFIC DATA SDS 930: A. Rental price includes magnetic tapes. H. Magnetic tape units are IBM compatible. N. Graph plotters and analog conversion equipment are available. X. FORTRAN II. Note. System is directly program compatible with SDS 920.

THE BURROUGHS D 825

by JAMES P. ANDERSON

Modularity has meant many things to many people in the past. Where computer systems are concerned, Burroughs Corporation has defined the word by example. One such example is the B5000, which, of course, is well-known in the commercial arena; the other is the D825, a military computer system oriented toward the command/control problem. The *functional,* as well as *physical,* modularity of these systems permits a comprehensive building-block approach to applications design. For example, a D825 system can consist of as little as one processor (computer) module, one memory module, one I/O control module, and various peripheral devices, the whole responsive to a broad interrupt system and controlled by an executive program stored in memory. In its fully expanded state, the D825 can consist of four processor modules, 16 memory modules, 10 I/O control modules, and as many as 64 peripheral devices. Processor modules share access to the executive program, to each other, and to all memory and I/O. The first system, designated AN/GYK-3(V), was delivered to the U.S. Navy in July 1962; 37 systems for other government agencies are presently in use or on order.

design rationale

The Burroughs D825 Modular Data Processing System is based upon an advanced systems organization of relatively conventional hardware. Numerous technological

As manager of the Advanced SystemsTechnology Dept., Paoli Research Lab, in Burroughs' Defense and Space Group, Mr. Anderson is responsible for automation studies, research in computer systems design, and feasibility development. He conceived and developed the multicomputer system organization and operating program which led to the D825. Before joining the firm in 1959, he was with Univac. He holds a BS from Penn State Univ.

innovations were necessary in hardware design, but the scheme conceived for organization and control is of more fundamental importance. The concept which led directly to the D825 was formulated in the late 1950's as a result of Burroughs studies of command/control requirements. The studies conducted by the original design team established a number of criteria that would have to be met by computer systems used in command/control applications. The problems to be encountered required highly reliable systems operating continuously in a real-time environment—systems that could be expanded (or contracted) as the demands of the problem required, with no reprogramming necessary to adapt to changes in system configuration. The studies also indicated that the command/control situation calls for all of those functions typical of data processing, as well as several generated by the need to react in real-time.

In the eyes of the Burroughs design team working on the project, the obvious needs of command/control systems were simply not attainable by adapting commercial equipment, the approach generally taken at the time. Growth criteria suggested the need for a building-block approach to building a system. Reliability criteria required organization, control, and construction such that failure of a single element would not propagate through the system. Availability criteria specified for many command systems called for extremes in the ability to operate continuously. (As an example, one application employing a D825 called for no more than four *hours* of downtime in a 10-year period).

Extraordinary requirements such as these led to the concept of functionally independent modules, each module operable independently of the others but free to communicate with any of them, so that the failure of a single module could not down the system. The three module types which communicate in this manner are the processor (or computer) module, with 128-word, integral, thin-film register stack, the 4,096-word core memory module, and the I/O control module, a small processor with access to all I/O devices, which effects data transfers between I/O and main memory.

Although the individual modules of the system enjoy the usual high reliability of solid-state devices, the environment in which they were to be employed would not tolerate loss of the system as a result of damage or failure to individual modules. Therefore, it was decided to permit more than one module of each type to function in a system. Further, it was decided that a control doctrine should be employed that would permit on-line self-reconfiguration of the system.

By making the design such that additional modules of each type could be easily added to existing D825 systems, the requirement for orderly and economical growth was also met.

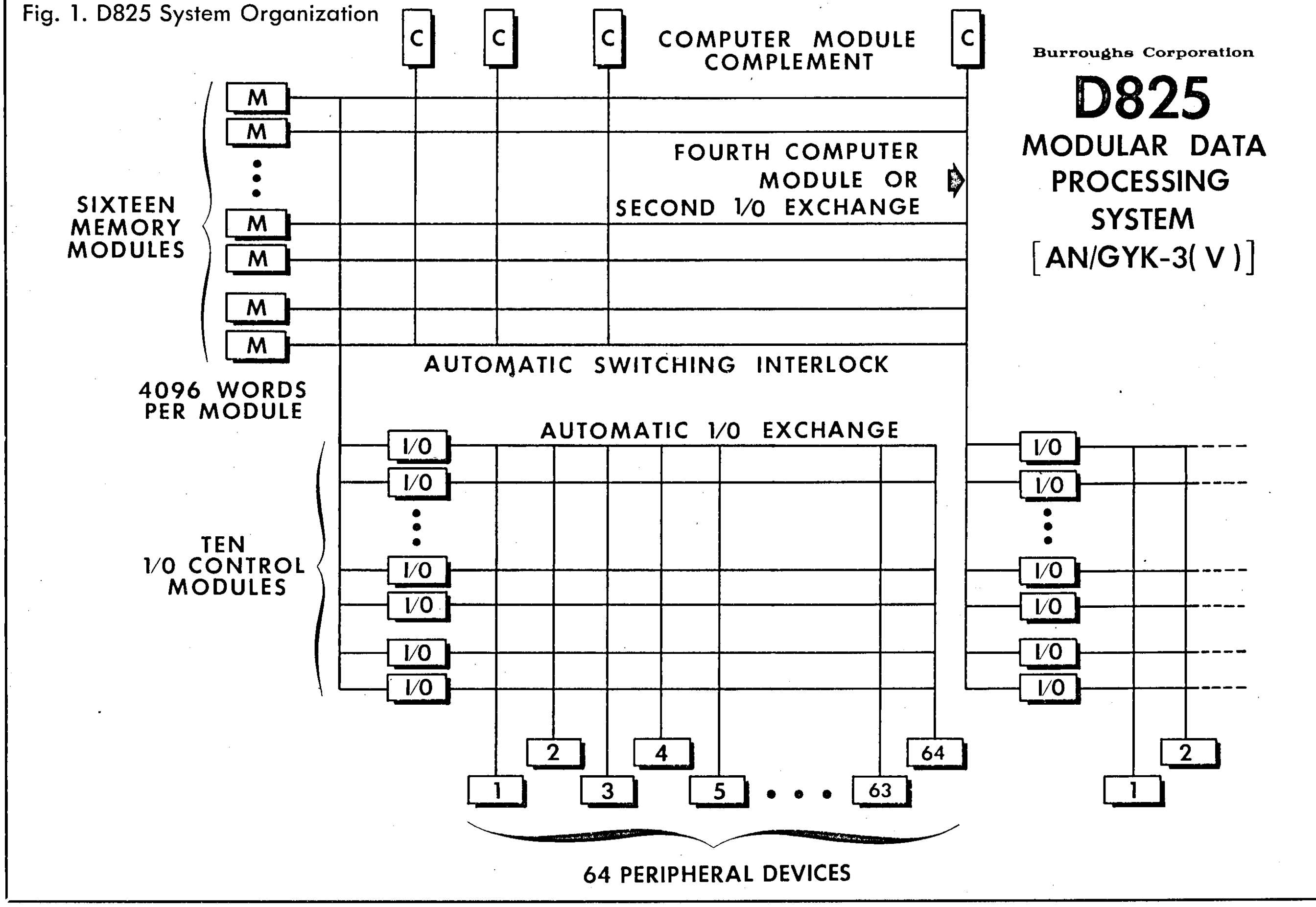
system structure

The system structure that meets the requirements of command/control and real-time processing is shown in Fig. 1. This illustrates the structure of a full-configuration D825.

The availability requirement of many command post applications would demand perhaps total redundancy of a conventional system, but is met in the D825 simply by adding a single additional module of each type to the minimum complement necessary to meet the application. This provides sufficient redundancy to permit uninterrupted operation in an economical system.

For example, if a particular application requires that the system employ one computer module, four memory modules, and two I/O control modules, then one more computer, a fifth memory module, and a third I/O control module are sufficient to supply full redundancy. If one

Fig. 1. D825 System Organization



computer should fail, all of the functions can be performed by the remaining machine, since it has full access to the rest of the system. Furthermore, the additional memory and I/O control modules are "active spares," and need not sit idle awaiting a failure elsewhere. Or, it may be that simply adding the second computer module would sufficiently protect the prime system function, since failure of a module in either the memory or I/O control complements would result only in a *reduction* in, not an *elimination* of, computing capacity.

intercommunication: the switching interlock

The interconnection matrix shown in Fig. 1 is called the *switching interlock*. It provides the many momentary interconnections between modules for the proper functioning of the system. Although shown as an array of crosspoints, the function is distributed among the various modules, which are then interconnected by cabling. The switching interlock also contains circuitry to solve conflicts in the event two or more modules (computer or I/O) attempt simultaneous access to the same memory module. In this unlikely event, the requests for memory are queued in automatic priority fashion, with the peripheral equipment obtaining first access. Conflicts between equally ranked devices are resolved in a fixed manner, the device of lower number obtaining first access. The actual probability of conflicts in attempting to gain access to memory is quite low, first because of a natural distribution of programs and data in the memories, and secondly because when the switching interlock offsets one of the conflicting modules, further conflicts tend to be eliminated.

system control: the aosp

Early in the detailed design, it was apparent that while engineering advances would add considerably to system capability, the program for hardware development could proceed essentially along familiar lines. The approach employed was to apply new and old techniques to a major improvement in system organization. The hardware techniques selected included many wholly new elements, but were otherwise those which had been successfully applied to other projects calling for operation in the military environment.

A more serious problem arose in software design. It was clear that if the potential of the new system configuration was to be realized, a control program coordinating the activity of the several processors would be required. A number of control schemes were examined—master/slave, master processor, job stacking (as in the FORTRAN Monitor)—and rejected for various reasons, either because they did not have the inherent flexibility demanded by the applications, or because they were too heavily oriented toward single-main-frame commercial computers. The most reasonable scheme was the master processor scheme wherein the master does nothing but control the system; however, the extreme waste of capacity when this function was not called for, and the potentials it presented for bottlenecks and failures, caused it to be rejected.

On reflection, it was seen that, since all memory was to be totally shared by all processors in the system, a structure was possible wherein programs or program segments were shifted about from processor to processor, so as to permit direct response to the various interrupts in the system. It was, furthermore, quite clear that programs did not need to be associated with particular processors. Rather than to consider processors as executing programs, it seemed more realistic to think of programs as controlling processors. Out of this thinking grew the concept of an executive routine that would be executed by each processor when its services were needed for obtaining a new job, or for responding to one of the interrupts in the system. This program is known as the AOSP (Automatic Operating and Scheduling Program). It was developed to provide the automatic control framework for efficiently and effectively running multipath, parallel, real-time programs.

The natural result of this method of control would be that processors would seldom be idle, and that a priority program would never experience substantial delay. To effect this unique mode of multiprogram operation, the AOSP maintains a job file for all programs currently entered in the system. One element of this file, for each job, is an "image" of the job, which is transferred to the thin-film registers of a processor when assignment of that job to that processor is made by the AOSP. The image is either the initial data needed by the processor to begin the job, or it is data received from the thin-film registers of an interrupted processor, representing the current point of completion of that job. In either case, the job is already set up (necessary data is stored in main memory).

When a processor seeks a new assignment (because it has completed another program or has responded suitably to some interrupt condition), it runs the AOSP, and if it is assigned to that program, transfers the image of the program from main memory to its own thin-film registers; if this program is then interrupted, its image (revised to the new point of completion) is simply returned to the AOSP, subsequently to be drawn out once again by some other (or the same) processor seeking an assignment, and run from the point of interruption. Processors need not, in fact, be made aware that they are picking up a job in midstream.

An additional, and valuable, capability provided by this operating structure is that program branches may be specified by programmers, so that the AOSP may divide a single program among several processors for simultaneous parallel solution of separate segments. In another common situation, different sets of data are to be applied to a single program; in the D825, two or more processors can perform these tasks in parallel, each processor/task assignment offset from the other(s) by essentially a single instruction.

The AOSP resides totally in main memory of the D825. (Memory space required for AOSP storage varies broadly with the application, since the AOSP, in a given case, is really a selection of routines drawn from a great number of options; something less than one memory module might be considered typical). This choice for implementing the concept was determined by the real-time nature of the problems for which the D825 was designed. It was necessary to establish a control structure which would permit immediate and *automatic* entry of a priority program, without damage to interrupted programs, and which would permit rapid, simple addition or substitution of hardware or AOSP routines into the system structure.

The AOSP performs several important functions in coordinating the activities of the D825. First, it initiates all programs that are part of the system application, allocates space for them in memory, obtains code from systems tape(s), reads all data such as tables, and the like. The functions of job scheduling and configuration determination are also integral parts of the control necessary to operate multiprocessor systems. In addition, the AOSP coordinates all I/O operations, obtains buffer storage, updates lists of I/O devices available to the system, sequences multiple requests to the same data, determines whether data files are present, and if they are not, informs operators that tape reels containing the appropriate files must be mounted.

Programs for the D825 include a directory of all other objects (data, library subroutines, other system programs, etc.) necessary for running each program. The AOSP uses this information to obtain these programs and data, allocate storage space, set up I/O buffer areas, and the like. Of course, other system programs obtained in this manner may require still other system programs, which are obtained in the same way.

So as not to clutter the core memory with programs that may or may not be executed, depending upon run- time decisions, the fetching of a particular program (and all that it entails) can be made conditional.

Another important activity of the AOSP is to effect appropriate responses to all real-time interrupt situations. Both externally initiated interrupts (such as activation of a user console, or the appearance of information on a communication line) and internal interrupts (such as no access to memory, or failure of primary power) are handled by the AOSP.

real-time response: the interrupt system

The D825 interrupt system is comprehensive, with all interrupts distributed to all processor modules in a system. It is also comprehensive in that it includes routine interrupts representing merely momentary hesitations which occur frequently in conjunction with information requests and transfers, as well as interrupts representing hardware crises, for example. The internal (processor-generated) interrupts are:

1. Real-time clock overflow.
2. Attempt to write out of bounds.
3. Illegal instructions.
4. Parity error from memory.
5. No access to memory.
6. Arithmetic overflow.
7. Halt instruction.
8. No presence bit (indirect data address).

The external interrupts are:

1. An I/O operation is completed.
2. An external request (16 possible) has been made.
3. Primary power (which had failed) is now restored.
4. Another processor interrupts this processor.

An interrupt mask register in each processor, set by the AOSP, determines which processor in a system responds to which interrupts. Generally, divided responsibility is desired; otherwise, some functions initiated by interrupt could be delayed if a series of higher priority interrupts were to occur. (Priorities exist primarily within the interrupt response area of the AOSP, and are established to ensure that interrupts which by nature can be delayed do not pre-empt response to interrupts which cannot be delayed—such as servicing incoming messages on communications lines. Priorities of a very different nature—those specifying relative urgency of different jobs—can be specified externally, either as statements included in programs, or as manual interrupts. These priorities, except for the manual insertion option, bear more significantly upon the AOSP than upon the interrupt system).

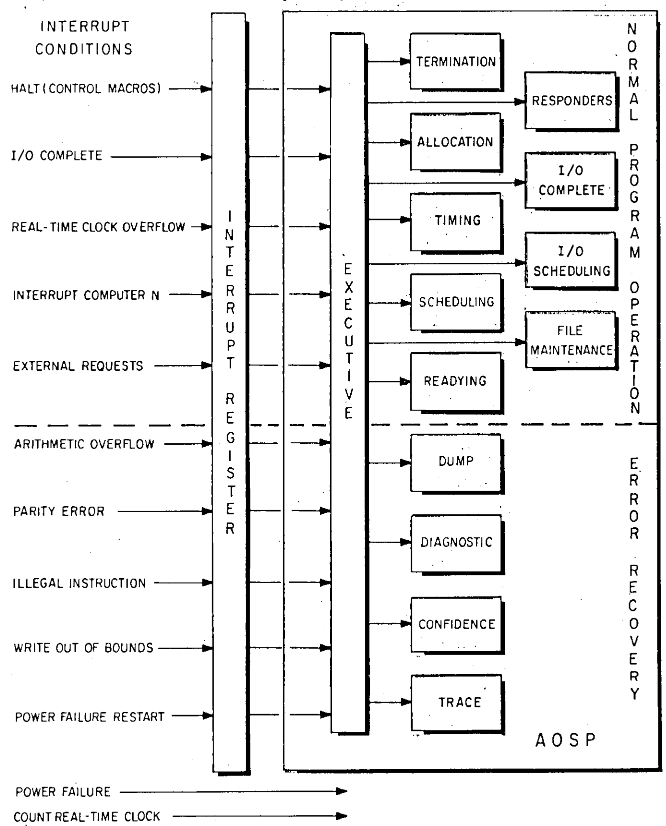
The type of interrupt determines which part of the AOSP is to be activated. Because of the generally divided interrupt-reaction responsibility, it is thus possible to have two or more parts of the AOSP active simultaneously, without conflict. The only possible area of conflict—that of changing AOSP system tables (which are global to all programs in a D825)—is handled by providing programmatic lock-out, or exclusive use of the tables by one processor. When the tables have been updated, they are released to any waiting processor. It might be noted in passing that the feature of exclusive use of tables is available to operational routines, and can be used where two programs must share a common set of data that is undergoing continuous modification.

Fig. 2 is a diagrammatic representation of the interrupt system, and the various AOSP functions invoked by each.

implementation: the system modules

The Memory Module. The D825 memory module contains 4,096 words of 49 bits each (48 information bits plus one parity bit). In addition to the addressing logic, and a part of the switching interlock, it contains its own

Fig. 2. D825 Interrupt System



power supply. It is designed to operate over a wide range of temperature and humidity without the aid of compensating devices, such as heaters and the like. The memory cycle time is 4.33 microseconds and a word is accessed for use in the computer in one microsecond.

The Processor Module. The processor module contains all of the arithmetic, manipulative, and control logic normally associated with a computer. In addition, it has a 128-word magnetic thin-film store that operates at the 3-Mc clock rate of the processor logic. This storage holds a four-position arithmetic stack, 15 index registers, and many of the special addressing registers. D825 programs and data are arbitrarily and separately relocatable. As a result, all data and programs are relatively addressed, and two base address registers are provided to bind the programs being executed.

The D825 employs a variable-length command form permitting zero-, one-, two-, or three-address instructions to be intermixed arbitrarily. Commands are constructed from instruction or address syllables, packed four to a computer word, and strung together as required to construct the commands, without regard for word boundaries. The command list includes a full complement of fixed, floating, logical, and partial field instructions.

The I/O Control Module. The I/O control module is actually a small processor which contains all of the circuitry necessary to independently control and couple the transmission of data in and out of the system, from or to memory and peripheral devices. Both incoming and outgoing data thus pass directly through the I/O control modules, undergoing various format and timing transformations enroute, as appropriate. Maximum transfer rate is two million characters per second.

The I/O commands are transmitted from computer modules under AOSP direction. Commands are transmitted in word-size instructions, known as "control words," that contain information giving the location in memory where information is to be placed or obtained, the direction of data flow, the number of computer words involved, and the peripheral device address. A one-word assembly and distribution register with a two-character or one-syllable buffer is also provided as part of the I/O module logic. Upon completion of an I/O command, the I/O complete interrupt is generated, and a descriptor returned to the AOSP containing error information that may have been detected as part of the command.

The I/O control modules may connect with up to 64 peripheral devices, assembled in any complement of tapes, drums, discs, card punches and readers, paper tape perforators and readers, consoles, displays, high-speed printers, real-time clocks, data converters, and the like. The I/O connections are made through a second exchange (roughly comparable to the switching interlock), making all peripheral devices available to all I/O channels.

The Data Demand Module. For communications applications, an additional module type closely analogous to the I/O control module, called the data demand module (DDM), has been added to the D825 system. The DDM also contains control-word-directed line-scanning and bidirectional information-buffering circuitry with a capacity for up to 512 lines of a mix of 100-200 wpm teletype and 1,200-2,400 bps digital data links. As with the I/O control complement, DDM's (a maximum of five are permitted) share one line into the central switching interlock, and effect external transfers through a third exchange—the data demand exchange—accessed by all communications lines.

The Data Buffer Module. The DDM operates in conjunction with another module known as the data buffer module (DBM). The DBM performs the level matching and, in conjunction with the DDM, line synchronization for each line. In addition, the DBM buffers characters on the slower speed lines, and strips off start and stop bauds where appropriate. The information buffered in the DDM is placed in the memory area designated in the control word. Interrupts are generated when the amount of data designated in the control word has been received or transmitted, thus permitting the processor(s) to proceed with other functions, and to attend to the communications lines only when absolutely necessary.

Typical Complement. The photograph (Fig. 3) shows a typical D825 system. This system consists of two processor modules, two I/O control modules (packaged two per cabinet), and 16,384 words of memory in four modules (also packaged two per cabinet), as well as an I/O complement.

applications and software

The D825 is presently being applied to a variety of command and control problems, including air defense, communications processing, and the like. The prototype system has been in use at the U.S. Naval Research Laboratory for nearly two years. Two other systems are presently in government use. A total of 34 systems has been installed or are in production as part of the U.S. Air Force SAGE BUIC (Back-Up Interceptor Control) network, and Burroughs is under contract to develop an Automatic Message Processing System for the U.S. Army Signal Corps. This system will be of the store-and-forward type, and will be implemented with a D825 system which includes the recently developed data demand and data buffer modules and the data demand exchange.

The programming systems for the D825 include Burroughs-developed JOVIAL and ALGOL '60 compilers, an assembly system, and of course, the AOSP. In addition, there exists a customer-developed NELIAC compiler for the machine. A variety of utility and mathematical subroutines has also been developed, and is part of the system programs available with the computer. ■

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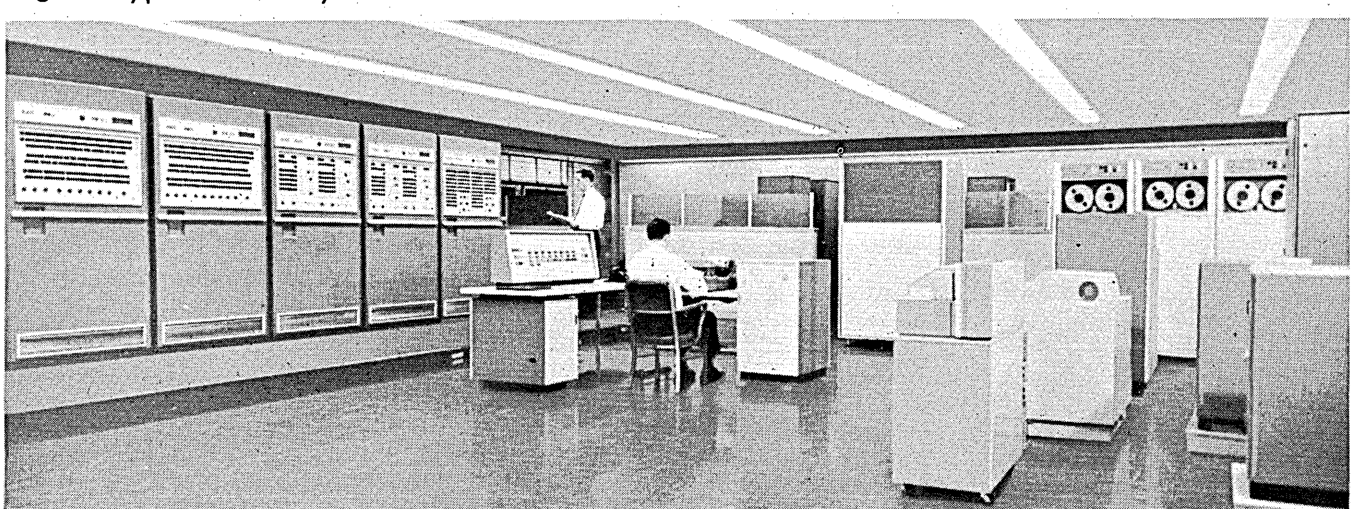
Fig. 3. Typical D825 System



AUTOMATED PAYLOAD CHECKOUT

with a small-scale computer

by E. K. MONTOYA

Computers are firmly established in the fields of mathematical computing and data processing, and they are beginning to be widely employed in the process control field. In the latter use, the emphasis is on production. Applications so far, such as refinery control, have been on high volume, long term production. Industry, in general, has tended to overlook computers for uses other than in established areas, probably feeling, among other things, that computers are too expensive for other than proved tasks.

In the highly competitive computer industry, manufacturers are now producing not only faster and better computers, but are also decreasing costs so that users are now beginning to consider them for many applications that would have been unthinkable a few years ago. In particular, the small-scale computer is suitable for the performance of automatic chéckout procedures.

Today's design engineer, with the advent of space science, is faced with a monumental task, as the complexity

Mr. Montoya is a member of the programming staff of Sandia Corp., Albuquerque, N. M., working with both analog and digital computers. He is responsible for planning and development of programs and techniques for real-time checkout procedures with electronic network configurations, as well as the development of data reduction programs for detection satellites now in orbit. He holds a BS in math from the U. of New Mexico.

and sophistication of systems seem to increase exponentially. He has a dual problem: to evolve an optimum theoretical design, and to follow through the operational phase to insure that the systems will perform according to theory under dynamic testing.

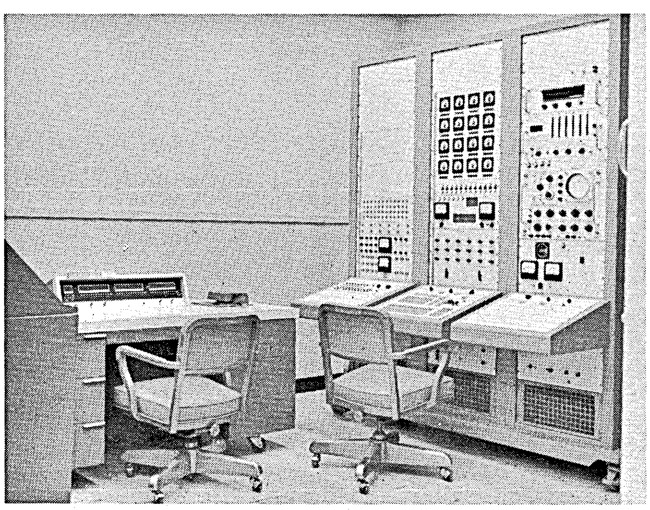
Design engineers will all agree that checkout has become a major operation. If computer checkout is considered, it is usually with misgivings. They are familiar with scope and meter techniques and know exactly what every step should be, being complete masters of any situation. However, if a computer were employed, they would be completely unfamiliar with computer language and operating techniques, and feel that they were at the mercy of a mystic black box over which they had no control. Furthermore, they have no firm convictions about the validity of computer checkout or how long and involved programming may be. So it is not unusual that they often decide to perform checkout by manual methods.

Some time ago, Sandia Corporation became involved in the design of a satellite payload. The delivery schedule allowed little time for design and development of the project. Earlier experiences on projects of a similar but simpler nature made the designers realize that checkout would have to be automated in some manner. Due to the complex nature of the payload, it was inconceivable that a complete and thorough checkout could be accomplished by scope and meter techniques. Design specifications were not frozen and therefore subject to frequent and possibly radical changes. It would not have been practical to design special purpose test equipment, since any payload modifications would probably also require modifications or complete redesign of the test equipment.

It was felt that there was an urgent need for parallel development of the test equipment and the payload. However, the test equipment would have to be flexible to accommodate changes in payload design without requiring radical changes in the test equipment hardware. The decision to employ a computer was made primarily on this basis; changes in payload design could be taken care of by modifying program modules. With these ground rules established, work on the payload, general test equipment, and programs progressed concurrently.

payload description

The payload of the satellite consists of a number of analog transducers that respond to external stimuli, and associated electronics for performing certain logical operations and data handling. The response of the transducers is fed into analog-to-digital converters and then to electronic logic networks for analysis and output. Each transducer has associated analog and digital circuitry that react as a function of the stimuli and generate pulses for distribution throughout the logics network. Observation periods are segmented and the information gathered represents the accumulation for one time segment. The logic of the payload is divided into eight subsystems, a subsystem being defined on the basis of logical divisions of functional circuits. Each subsystem, therefore was semi-independent and a program module could be written to check each one independently. Because weight was a prime consideration, miniaturization was essential. Consequently, a typical subsystem contained an average of 75 modules, with about 20 components per module.



command and data flow

During automatic tests, the computer transmits instructions to the test console in blocks of three 12-bit words that are stored in the computer output buffer and are available for use upon execute-commands until the next block of instructions is transmitted. The instruction decoders decode the buffer information and use it for functions such as setting gates, operating relays, or advancing stepping switches.

Receipt of an execute-command from the computer results in the transmission of the desired combination of stimuli to the payload through the signal generators and the setting up of various monitor indicators on the test console. The data buffer and data handling unit accept reformatted payload data on a cyclic basis from the computer in the form of two 12-bit words and perform all necessary analog-to-digital conversion, decommutation, and circuit routing. The data display consists of a bank of lights indicating present payload command status, 16 meters displaying selected payload state of health indications, and in-line digital readouts for the display of commutator position and payload data frame accumulations.

The computer input buffer consists of loading controls and a 12-bit buffer that is addressable by the computer. It may be loaded from a shift register, a status code generator, or from any one of four 12-line sources of payload subsystem outputs.

A diagnostic program, written for the test console, insures its working order. Running time for this program is about 15 minutes.

general purpose test console

A general purpose test console serves as a buffer between the computer and the system or subsystem under test. A control panel on the test console functions similarly to the computer control console. There are two basic operating modes, an automatic mode and a manual mode, available for selection from the test console. Several operating options are available for either mode. All programs are written so that the test console is queried periodically to see if a change mode or option has been requested. Regardless of the operating mode, the computer programs must keep up with the real-time data flow being generated by the system under test. The data flow is composed of a serial train of data bits being transmitted at a fixed frequency. This data train is segmented by a code word to establish a reference point for the rest of the bits in the segment or for future code words. Programs will automatically go into the "spin mode" or modified "spin mode" of operation in order to stay synchronized with the data when an option has been exercised or when awaiting an operator decision.

In the "spin mode" of operation, the data is simply cycling through the computer without any operation whatsoever being performed on it or without execution of any command, but retaining its basic reference point as acquired by the initial sync search.

In the modified spin mode, the data also cycles through the computer as in the "spin mode" but now each new frame is affected by the previous frame as certain bits of each frame are fed back into the system to simulate operating conditions.

The options in the automatic mode were designed to enable the test operator to either repeat or ignore segments in the test. This feature made it possible to trouble-shoot a particular segment of the circuitry under test without having to run the program through the full test cycle. In this mode, the input stimuli to the system under test is under program control. An automatic option can be exercised by selecting the desired option command with a selector switch on the test console and pressing an execute function switch each time the option is desired. A command matrix is scanned after processing each frame segment to test for any new option or mode of operation to be followed beginning with the next new frame segment coming into the computer. The options available in the automatic mode are: restart the program, in which case the test is started at the beginning; repeat the last step, in which case the last program step that affected the frame segment of interest is repeated; repeat the last section, in which case the last program module is repeated; continue with the next step, in which case the next program step affecting the next frame segment is executed and the program goes into a modified spin loop awaiting an operator decision; continue with the next section, in which case the next program module is executed and the program goes into a modified spin loop as above; continue with the test, in which case the test is under normal program control; continuous printing, in which case the program proceeds normally without stopping on detected errors but printing out the bit configuration for each frame; and stop automating testing, in which case the normal program operation or any of the above continuing operations can be interrupted and the program goes into a modified spin mode.

In the manual mode, a test operator can manually generate problems to feed to the system under test. The program goes into the spin mode of operation when the manual mode has been selected by a function switch and the problem, which consists of selecting an assortment of electronic pulses and voltage levels, is set up manually through a push button arrangement on the test console.

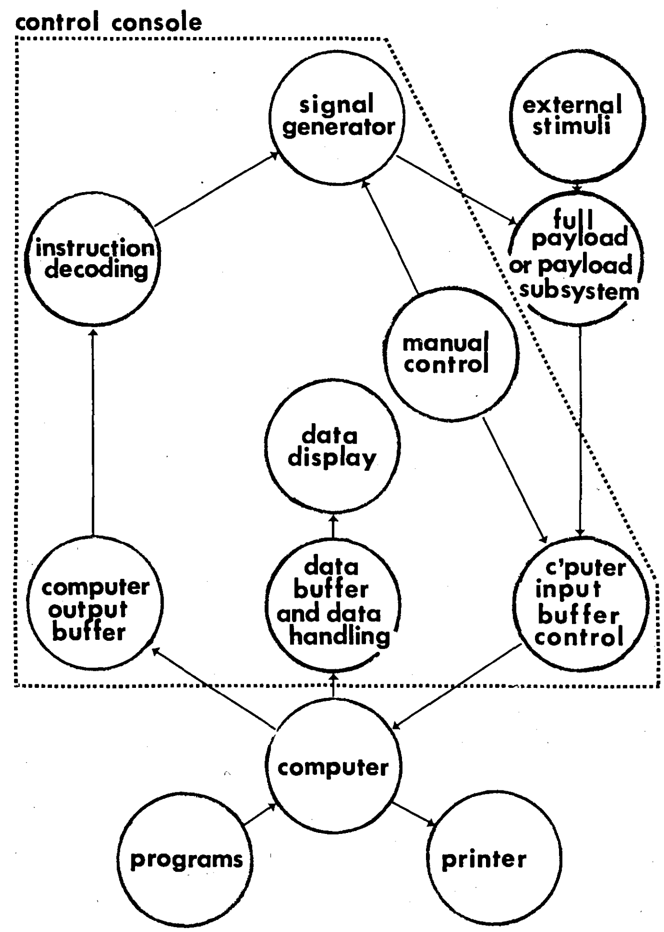
An option command is then given and executed by depressing the execute function switch. The type of options that can be exercised may be such that a particular frame in the data train must be reached before the selected option is executed and the desired results may be of interest at still some later frame. Once the command has been executed and the results generated, the program goes back into the spin mode to await the next operator decision.

typical tests

A typical payload subsystem consists of 16 input and 46 data output lines, plus eight input and three output control lines. This model is designed to detect pulses on the input lines and by adding them with a pulse adder and setting up a voltage level to correspond to the number of pulses fed in, the appropriate N-fold gate is triggered and a bit is accumulated in the corresponding accumulator. When the basic accumulation cycle is complete, the contents of the N-fold accumulators are transferred into a shift register and from there they are shifted out as part of the data train. At this point the accumulators as well as the various gates are reset and made ready for the next accumulation cycle.

A computer program to check this model out generates 35,300 different input conditions as stimuli, thus exercising every circuit in the model in all possible modes. The input lines feed two redundant systems so that, in effect, the number of inputs is doubled for the test. Each input combination constitutes a problem for which the expected output combination generated on from eight to 36 output lines, is known and can be checked. If an error results, the printer prints out the pertinent conditions of the subsystem at the time of the error, including the input combination and response. Control is transferred to the test console at this time to await an operator decision to select a program route to follow by the execution of any one of the test options. It takes approximately four minutes of computer running time to perform a test. When all subsystems are checked out and functioning properly, the problem remains of checking the operation of the full system.

Since the nature of the tests to be performed at Sandia were extensive and core storage was a limiting factor, the test program had to be broken up into several parts designed to perform two basic types of testing.



The first type of test is a closed-loop type, with payload stimuli generated within the test console upon command from the computer and transmitted by hard wire to the payload. The computer then monitors the payload output and verifies its accuracy. If the outputted data are correct, the cycle continues until test completion. Upon error detection, however, all the pertinent data associated within the time increment in which the error occurred are printed, with the portion in error being identified by printing the correct answer immediately beneath it on a second line. At the same time, the automatic portion of the test stops with the program going into a modified spin mode to stay synchronized with the data flow and to await an operator manual command executing one of the options available.

The second type of test is one in which the transducers are excited by stimuli in the form of statistically known sources. The payload data are monitored to verify that they are within acceptable limits as defined on the basis of the characteristics of the known sources.

The average full systems program takes about 40 minutes to run. Most of this time is spent while the computer is waiting on the payload operating in real-time to perform certain transitions, some of which take as long as four minutes to occur after a command has been executed.

programs

A total of 22 programs were written for the checkout of the whole system. There were 10 programs for subsystem checking, 10 for the full system, and two for diagnostic testing of the test console. Programming time amounted to about 2,500 hours, with checkout time averaging about 25 hours per program. It should be kept in mind that this was dual checkout time during which the hardware was checked out along with the program. Most of these programs were revised many times as the hardware was developed. There was no great degree of complexity involved in any of these programs. Actually, the test routines by themselves could be classified as simple.

Because of the limited amount of core storage available, it was necessary to generate input stimuli with the computer for some of the programs. (The use of tables would have taken up too much core). Answers were similarly generated for the same reason. Being prepared to exercise any one of the various options required rather extensive program bookkeeping in order to feed in parameters to a decoding subroutine that determined what option to exercise. Coding of these routines was somewhat involved since core storage was at a premium.

Efficient coding was necessary for the real-time mode of operation because certain logical operations had to be performed on the data between dumps of the data train and still be able to keep up with the data. In some cases, this involved segmenting a particular operation and operating on a segment at a time during slack dump periods of the data train.

operational findings

While it is true the real-time automated testing eliminates many of the problems imposed by manual testing methods, it is also true that some new problems are created. Perhaps the most severe of these is the problem of interfacing the hardware and program. It was found that much needless buckpassing was eliminated during the interfacing period by having the programmer understand the design hardware and similarly having the designer acquainted with the computer and the techniques being used in the programs. Under these conditions, problems that arose were attacked jointly.

Repeatability of errors was a problem that had to be solved if the tests were going to be of any diagnostic value. Without this feature, it would be difficult to isolate faulty components or noise problems.

For a complex electronic network, manual simulation of the exact conditions that create errors can be time consuming and is often difficult. With the computer, it was found that conditions on a network could be simulated automatically in very short periods of time, since a snapshot of the network conditions causing the error were saved in memory for every error. The computer can restore the network to these conditions on execution of a "repeat" option. An on-line printout indicating states of the pertinent logic during the time interval in which the error occurred also was provided. In many cases in which errors were caused by random noise picked up by a network, the step had to be repeated several times in order for the error to be repeated.

The possibility of a single error being fed back into the system, thereby generating erroneous output from that point on, had to be met. To get around this difficulty, it became necessary for the program to modify the predicted results on the basis of the erroneous inputs.

During the subsystem checkout period, problems were encountered, as had been anticipated, that indicated a need for modifications to the payload. These modifications were accomplished, and test procedure changes were accommodated by modifying programs, without modifying the test console. It was found that after a preliminary checkout period, the program thereafter had a high degree of reliability and required only a minimum amount of operator knowledge to perform an extensive and complex test. This enabled the design engineers to delegate the testing operation to technician or operator personnel, thereby allowing the engineers to spend more time on design and research problems.

This particular design group at Sandia feels that this method of hardware checkout is far superior to manual methods, particularly since the scope of checkout was so extensive that only a partial manual checkout could have been accomplished in the allotted time. In general, when manual tests are long and complicated and have to be performed many times, the testing people, while holding to fairly rigorous standards at first, tend to relax the standards as the test is performed many times. With automatic computer testing, the rigor of the test remains the same regardless of the number of times the test is performed. Checkout was performed as a joint effort with programmers and designers speaking a common language understood by both. The complex maze of wires and components in electronic packages took on a new meaning for the programmer, and the designer lost his fear of the computer and learned that he could even communicate with it and make it perform many of his tasks for him. A small scale high-speed computer with 4K core storage was used. It turned out that this computer was no more expensive than the development of special purpose test equipment. Basic machine language, assembled with a standard assembler, was used in programming. More core storage or tape units would have made much of the programming simpler.

The system is now operational at Sandia Corporation where several systems are being built and checked out. Each subsystem is tested a number of times under different environmental test conditions. After all the subsystems have been tested and found satisfactory, they are assembled in the full system and it, in turn, is tested under different environmental conditions. The complete testing of the first assembly that involved program checkout, test console checkout, and hardware checkout, took about 10 weeks. At present, a complete system can be fully tested in less than two weeks. ■

ON-LINE MANAGEMENT SYSTEM INFORMATION

Part two: installation & implementation

by NORMAN J. REAM

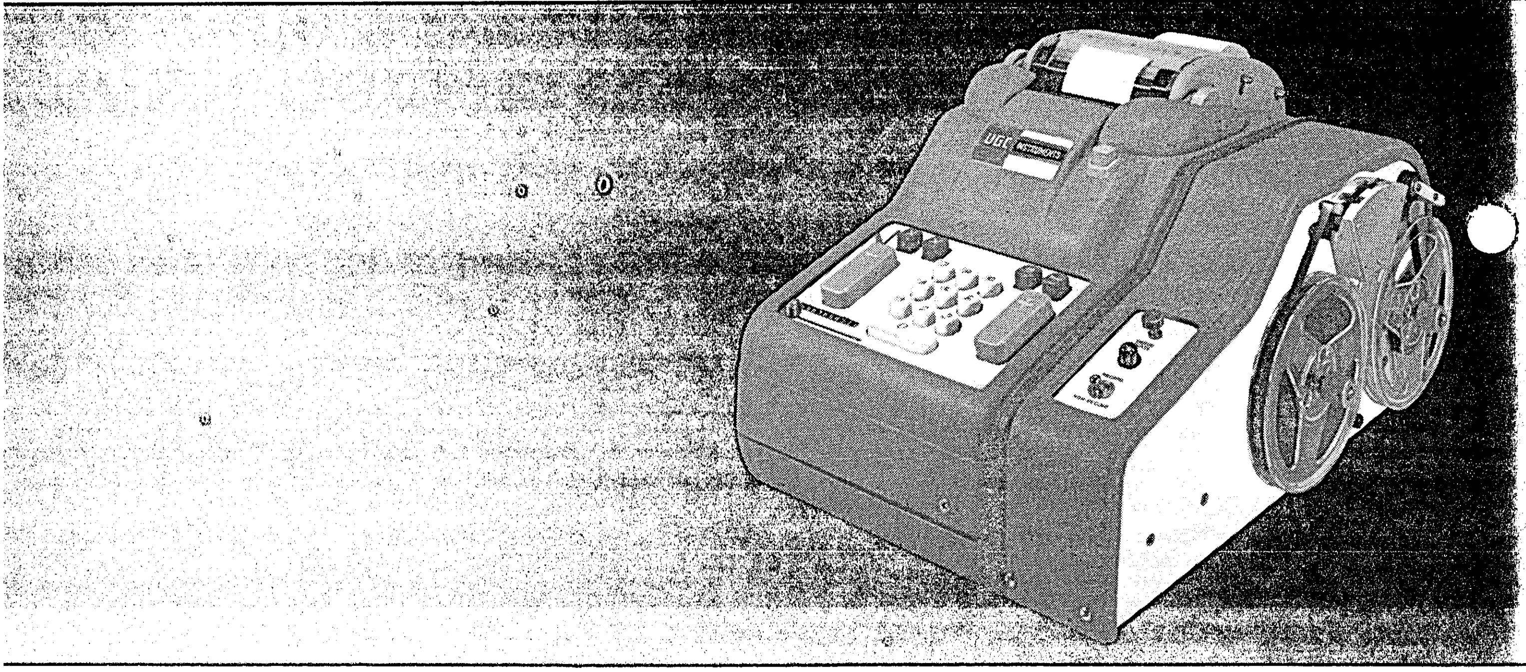
Last month, Mr. Ream defined a real-time management information system as "one which monitors the physical environment but exerts control only indirectly by the production of management type reports or displays." He also detailed the types of reports and the seven basic hardware configurations of such systems.

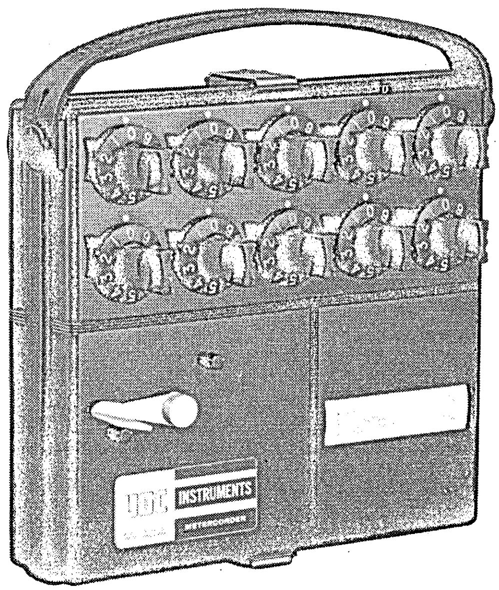
installing a real-time system

Let us first list the steps involved in installing a real-time system: systems genesis or design, hardware selection, programming design and execution, testing and integration, and system cutover. And over all, unfortunately, lies the pall of constant change.

System Design: It is generally agreed that problems in real-time systems to date have not been those of hardware or even generalized software (there is precious little of that), but problems of systems design and programming . . . notably problems of communication between the people involved. Because of the inherent complexity of real-time programs, the systems design work, the foundation for the programming itself, is exceedingly important. The makeup of the design team, the documentation and communications standards adopted, and the feedback system are all critical.

The use of an interdisciplinary team for system design is strongly recommended. This team should include programmers with intimate knowledge of the hardware

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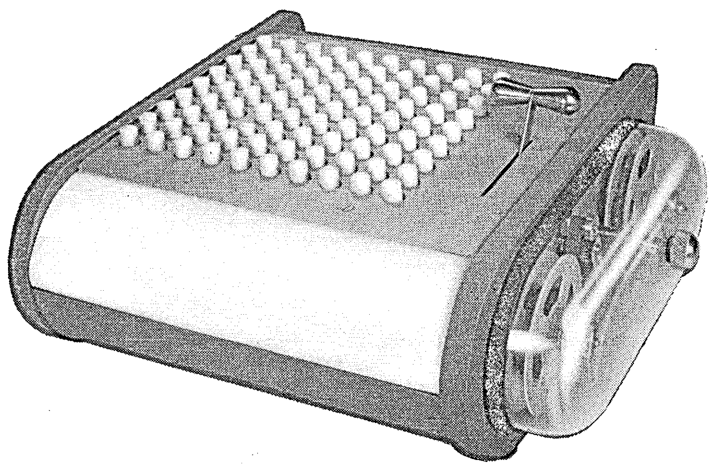

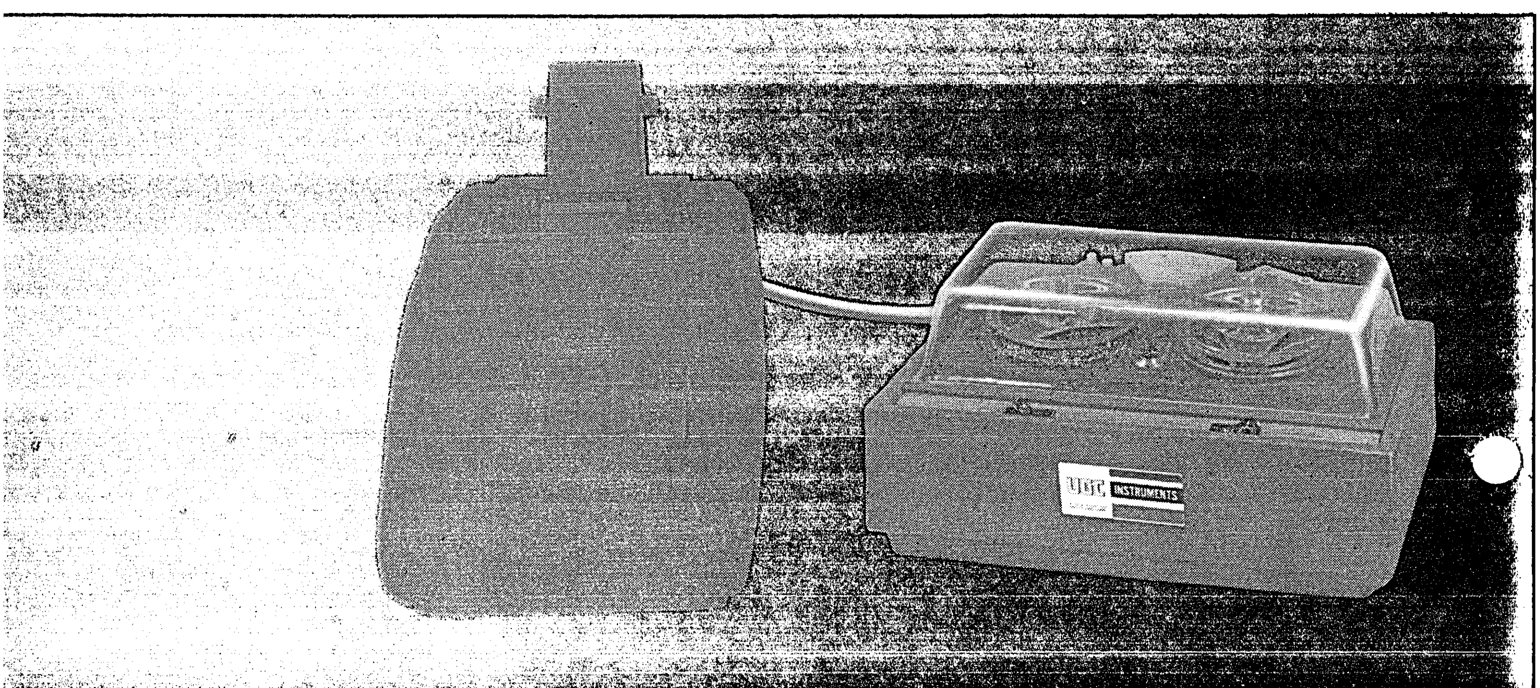
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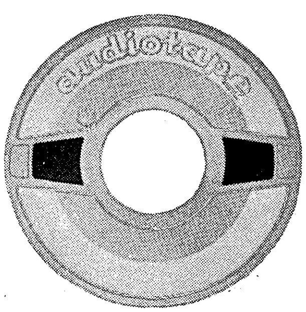

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being considered and its accompanying software, the customer who will be serviced by the system, representatives of the advanced planning section; the team should be supervised by an individual who is familiar with management's plans and objectives, both immediate and far-reaching.

This team must be responsible for problem definition and the operational specifications of the system. They will also be responsible for the broad (logical) system which includes a functional breakdown, a diagram of the main information flow, the initial sequencing of functions and transaction types, and the general allocation of computer capacity among the many tasks set for the system by the various parties involved.

Because programming for large systems costs more per instruction than does programming of less complex jobs and because real-time programming normally is accomplished (because of its size and complexity) by concurrently writing separate segments of the program, great emphasis must be placed on systems design. The key is to provide adequate design controls while the system is still in the formative stages.

At this stage in the design, certain factors must be considered. Are transactions to be treated in a "first in—first out" manner or will individual priorities be assigned to each transaction type? What is the estimated system growth, what are the peak loads in the system, what type of fallback or degraded service is acceptable or sufficient, what standards of reliability are to be adopted, and how will the system recover from a period of downtime?

The design team must also consider costing. At this juncture the programming manager must be consulted. Estimates must be made as to memory and file requirements and educated guesses ventured as to running times. The cost of a particular program feature must be compared to the operational value of its result or to its effect on the available computer capacity and features deleted or added in an attempt to balance the system to acceptable requirements. At this point, redesign is accomplished as necessary in the form of flow diagrams, decision tables and the like.

Another part of the initial systems design is the specification of program interfaces. Too often this is left to develop during the coding process, and experience has shown that this leads to extensive and costly reprogramming at late stages in development.

The system design team should not be disbanded after preliminary development of the system, but should continue to operate even into the implementation phase. The later work of this team will include the design of operational procedures, the investigation of message format options, the evaluation of alternative computational methods, and the design and specification of testing procedures. The team operates as a control and coordination group. Their work and its documentation is of the utmost importance to the success of any real-time system.

Hardware Selection: After systems requirements have been determined, the selection of hardware must be made. Basically there are three criteria for the choice. The size of the computer must be considered with special attention to the potential modularity of the hardware. Because real-time subsystems, e.g. shop order location and inventory control, cross functional lines real-time systems have a marked tendency to grow. It is, therefore, very important that the computer system selected can expand in terms of number of communications channels, size of internal memory, and capacity of file storage.

The throughput speed of the computer must be taken into account. The internal and input-output speeds of the hardware must be such that the rather complex programs typical of a real-time system can operate, with a safety factor for scanning or switchover, at the necessary speeds. But, real-time does not necessarily mean fast. The requirements of the system under development must be considered. Often system response time on the order of several seconds or even minutes is sufficient to fulfill requirements. In a case like this, internal computer speeds in the one-to-three-microsecond range are probably not necessary.

There is no more important criteria for hardware selection than that of reliability. The reliability of not only the central computer, but of the communication channels and of the file storage devices must be carefully evaluated. Usually the question of reliability centers around cost versus system requirements.

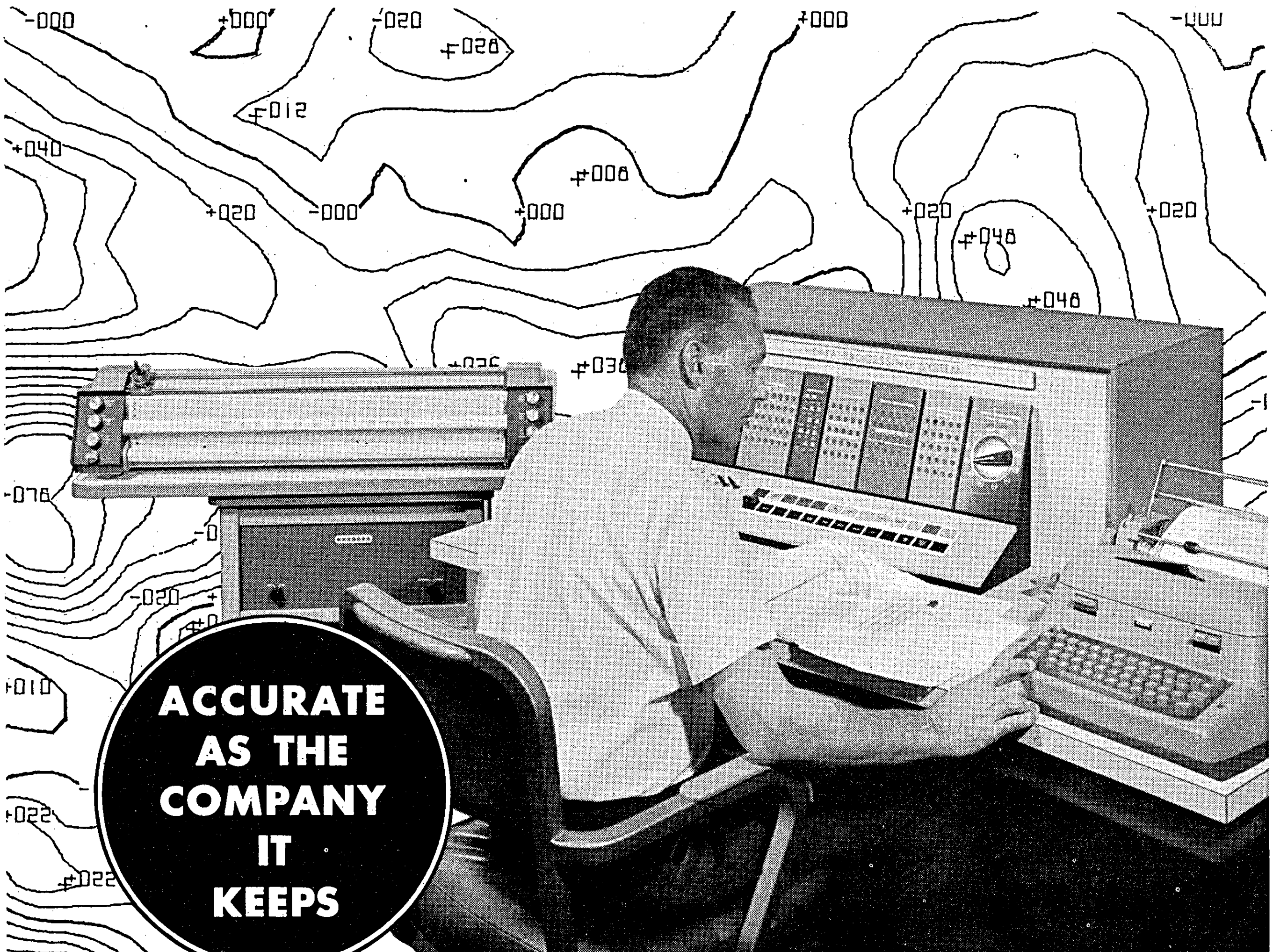
The historical expression of reliability as a percentage of uptime is virtually worthless in the case of a real-time system. While 97% uptime still means 3% downtime, it is much more important to analyze the downtime by duration of down periods and their frequency. In the days of the tube computer, downtime often occurred as many short periods. The present solid state systems fail much less often, but have a tendency to be down longer.

As an example, a computer that averages 97% uptime would be more than adequate for most batch-processing applications. The problem in real-time systems is that the user cannot "buy more time" to catch up. In a real-time system that must operate 24 hours a day, seven days a week, 3% is equal to 1,300 minutes per month. If we break these 1,300 minutes down according to a distribution which assumes more short periods than long ones and use an average of 30 minutes, we find that we can expect 27 periods of 30 minutes or less, 10 of less than one hour, four of less than 1½ hours, one of less than two hours, and one of more than two hours, for a total of 43 periods of downtime. This would not be a satisfactory record. Not only the amount of downtime, but the type, duration, and distribution of periods of downtime become of utmost importance.

Programming: Programming for real-time systems has a history of missed dates. This is partially due to the lack of full problem definition and completed logical system design, partially to the complexity inherent in real-time programs, and partially to the inability of the programming manager to accurately estimate the effort involved.

These problems center around the constraints imposed on programs by the real-time system. The real-time program must sample data streams at prescribed intervals, thereby placing a constraint on the time spent in exception or error processing subroutines. This time limitation and the complexity of program interfaces mean that real-time computer programs cannot be organized in as simple and logical a manner as in batch processing, i.e., they must be time conscious. Also, there is almost always a shortage of internal memory giving rise to the use of program overlays and their attendant problems. A system may consist of scores of tables, 50 to 100 program segments, and hundreds of data items all interacting in real-time with the sequence of execution dependent upon the content of the data streams. Yet no matter how the above factors may vary, the system must continue to operate within the time constraint imposed by input volume. In addition, real-time programs must deal successfully with a great variety of input-output devices of disparate speeds. The problem of errors in a real-time system places an additional burden on the programmer.

Data errors must be dealt with in such a way that the



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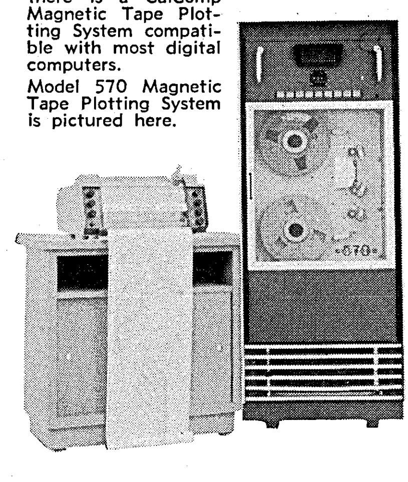

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system is protected against the broadening ripples of false information that are the effect of erroneous data being admitted to the system. Yet the program must keep pace with the ever-present time requirements.

Characteristically, then, the real-time program is one which is composed of many separate segments written concurrently by many different programmers. All of these segments are linked through both independent overlays and through access to the executive routine. The programs are large and very complex and yet must be very fast. They must provide for a validity check of all input data and proper disposition of errors, and the programming system must recognize hardware failure and provide for alternative handling at microsecond speed.

It must be stressed that program segments must "fit" each other exactly under all circumstances. Such concepts as common storage, data preservation and interrupt or trapping linkage are part of program design.

Programming Standards: The need for complete programming standards is obvious. As part of these standards a formal system of documentation plays a large part in determining the relative success of the effort. These standards must include strict rules for the use of the selected programming language, a functional description of the executive routine, including entrance and exit locations, detailed data formats, locations of logical program interfaces, design of major subroutines (input-output, standard computations, etc.), and explicit rules for programming procedures.

A particularly important requirement of the standards package is the development of some type of an information repository index or Communications Pool (COMPOOL). This is a listing of all data elements cross-referenced as to application and use. When a change is contemplated, the COMPOOL is used as a central reference point in order to determine all program segments using this item, the item's origin and final disposition, and its effect on the files. The COMPOOL, which may be designed as a set of tables, can be expanded to include program segment interfaces as well as data items. The COMPOOL will probably have to be mechanized because of its inherent size.

It is not enough to have a system of programming standards, even a well documented system, if its use is half-hearted and sporadic. We come now to the problem of programmer discipline. The programming group must be made aware of the necessity for following the standards publications. A course of training for the programmers should include not only extensive indoctrination into the overall system function and detailed analysis of the hardware and software to be used, but also rigorous training in the use of the standards system and especially the COMPOOL. In addition, careful attention must be given to the analysis of "worth" of various program segments. Programmers have a tendency to polish each individual subroutine in an attempt to squeeze every possible microsecond or core position possible out of the routine. While in theory this is a laudable goal, in practice it is very often neither necessary nor desirable. Here again, close supervision by technically competent personnel is necessary.

In general, the overall goals of the standards package may be summarized as: to break the job down into pieces of a manageable programming size and to provide a framework for organized and formal programmer-to-programmer communication.

The steps to be followed in program development might begin with program component design. By this time the preliminary division of the program into individual segments has been accomplished by the systems design team. Program design involves the more detailed and precise layout of flow diagrams and decision table specifications. Next, an analysis of the transfer function showing the environment for each program component should be accomplished.

At this point, the actual coding of individual subroutines begins. Concurrently with this coding the testing system is being constructed. This system includes test problem design and coding, parameter checking routine, and utility support programs. In systems requiring geographical referrents, they should be incorporated at this point. As each program segment is completed, it goes to test and then to program integration.

Where programming pressure is great, standards and documentation are still of major importance, and relief may be available in the future by using one of the higher level programming languages.

At the present time, most real-time programs have been written in machine-oriented assembly systems. As further experience is gained in real-time programming, languages and compilers will improve and we will see expanded use of high level programming languages.

The executive routine is the keystone of any real-time program. It functions as a scheduler and housekeeper accomplishing the handling of all inputs and outputs, including the construction of queues and the determination of individual transaction priority. It is responsible for supplying to the production programs all subroutines and file data necessary. In addition to these duties, the executive routine provides the accounting for the system in terms of message volumes, controls all program overlay, and performs the necessary switchover or fallback in case of equipment failure.

With all of these functions to perform, the executive routine has a tendency to become terribly complex and large. A better procedure is to design separate subroutines for each of the duties mentioned and to preserve the executive routine itself as little more than a series of standard trapping locations. In this way the executive routine can be fully debugged and ready for use when the first program segments are to be tested. Further, changes can be made in any of the individual functions performed by the executive routine without having to change the executive itself. Since all program segments access the executive routine, this last is a goal worth striving for.

Program testing is an area of real-time programming that deserves the closest scrutiny. This function is much more important in real-time than in batch processing systems. Each program segment must be individually tested for logic and clerical errors, run in conjunction with the executive routine to check linkage, and then incorporated into the system and tested once again. Experience has shown that the errors most difficult to detect show up when the program segment is incorporated into the system. This phase of testing, called system integration, should be carried out over as long a period of time as possible. The entire system should be retested with the addition of each program segment or subroutine. Throughout the testing procedure, extensive test tools must be used. Test data generators are invaluable. Simulators must be sophisticated enough to manipulate all of the variables present in the real environment. Because errors many times refuse to repeat themselves during debugging, sampling programs which monitor the running system and print out the contents of certain storage areas should be used throughout the testing of a program segment. Equipment failure must be introduced in order to test switchover and fallback procedures.

Again, it is the system integration which is the crux of the testing procedure. This exercise must be carried out carefully and documented fully.

The cutover of a real-time system is a critical point in its development. Unlike batch processing systems, once the cutover of a real time system is accomplished, the user is fully committed, i.e., he has virtually no satisfactory way of turning back to his former batch system. Therefore, the process of cutover must be carefully planned. Parallel operation of the new and old systems is a good method of easing cutover problems. However, it is an expensive proposition and the length of parallel is largely dependent on the funds available. In any case, several dry runs of the complete real-time system are an absolute necessity. New problems will arise at this juncture, so time should be allowed in the schedule following this operation for debugging and some reprogramming.

general implementation problems

Let us take a look at what is transpiring at any one time within the confines of a real time programming group. Many individual program segments are being coded while others are in test and still others are undergoing initial specification. Several segments have been linked to the executive routine and are being run against test data to check their logical interfaces. At the same time, the systems design team is screening change requests and receiving feedback from programming. Any system changes instituted are reflected in reprogramming effort and in a change to the COMPOOL.

With this complex activity going on, it is easy to see why the most severe problems in the implementation of a real-time system are in the management of the systems design and programming groups.

The task of a programming project manager involves meticulous control of the work of the programmers. He must allocate the program within the constraints of a limited time resource among the functions it is required to perform, and manage pressures for program change.

Experience has shown that the major problems lie in the manager's inability to accurately estimate the amount of effort involved in programming a real-time system and even more in his lack of ability to correctly judge progress. Estimates and forecasts in large real-time systems have traditionally been off by as much as 100%.

A method for evaluating and incorporating changes without throwing the programming effort into a state of confusion must be found. Here, especially, strict programmer discipline must be maintained.

Engineering groups have been far more successful in meeting deadlines for complex hardware systems than programming groups have been with software systems. True, this is partially due to the tangible nature of hardware, but it is also due in part to better management at the technical level. The programming manager *must* concentrate on an efficient distribution of effort. He *must* invest heavily in manpower in the areas of control and supervision, supervisor training, and technical leadership expended continuously during the course of the project, particularly during the formative stages. These investments will pay handsomely at the culmination of the project. The control of programming quality is particularly difficult and must be continually stressed by the lead programmers.

Fig. 9 shows the conventional project management. The lead programmer customarily has actual programming responsibilities in addition to his supervisory duties. There is not enough supervision here to exercise the necessary control.

Fig. 10 shows a very different organization. Note the staff functions of control and review, which interacts with the design group, and research which has the duty of making sure the system remains modular and has the benefits of any new techniques being developed.

Fig. 9. Conventional Project Organization

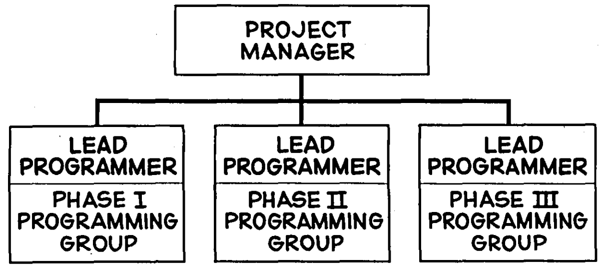
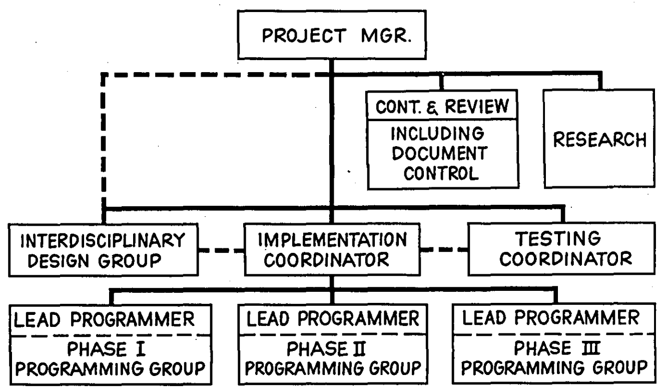


Fig. 10. Recommended Project Organization



The duties of the implementation and testing coordinators are strictly supervisory. They are responsible for making the feedback network function properly. The lead programmer in each group functions solely as technical supervision and control and has no programming duties.

The interdisciplinary design group interacts with the staff functions and with the coordinators to see that designs and changes are being correctly interpreted and implemented.

While this type of organization appears more elaborate and expensive, it will more than pay for itself in the success of the project.

Failure has no reward.

auditing

How does one audit a real-time system? The use of such a system essentially means the elimination of paper and therefore of normal audit trails. Several techniques have been evolved, most of them involving the periodic dumping of files onto magnetic tape and the continual recording of transactions on tape between dumps. This information is periodically structured, sorted and printed to provide an audit trail. In operating a real-time system today there are actually two types of data that the user accumulates—the data needed to run the system and the data necessary to satisfy legal requirements.

information protection

Another problem which confronts the designer of a real-time system if it involves, as most do, inquiries in real

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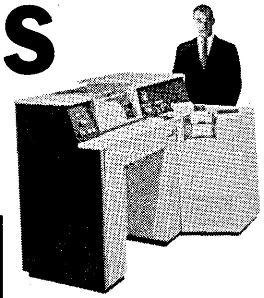

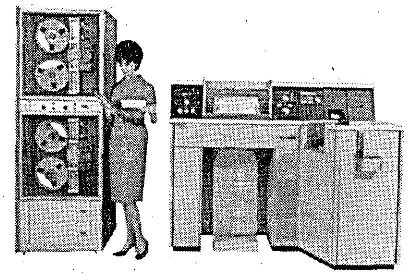

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time is the protection of information. How does the user limit access to certain information?

There are two methods available. The first limits information to particular inquiry units. Most devices emit, as part of their message, a code which identifies that particular machine. The executive routine can examine this code and determine whether or not this particular information may be sent to this unit. The second method limits privileged information to certain individuals rather than devices. This method works much the same as does the first except that the code comes from the individual's badge or pass rather than from the inquiry unit.

training

Experience has shown that in real-time systems, training of associated personnel is of much greater importance than in batch processing systems. It must be impressed on central computer operators that it is etxremely important that they react with speed and efficiency when operator action is required. In several real-time systems it has been found that computer operators had gotten into the habit of being less than expeditious by virtue of long hours spent in control of batch processing systems.

The system's customers must be educated as to their part in the operation. Workmen who will be using data collection devices in a factory should be taken off the floor for instruction in how to enter the various types of transactions. The Sabre system incorporates a full-scale simulator employed in the training of ticket agents. The training of the other type of customer, the one who requires information of the system, is just as important. Again, drawing on our experience, it has been found that rather extensive orientation to the system with particular emphasis on its abilities and limitations produced a marked improvement in the use of the system by customers and more than paid for itself in this way.

There is one more type of training—the most important of all. The training of company management.

management's role

Management pays the bill for the real-time system. Therefore, one of the first tasks involved in the presentation of such a system's specification is gaining management's agreement as to its value. Usually this involves economic justification. The factor needed to enhance the system's earning power is a very difficult one to obtain—management understanding. Corporate management today is becoming educated to the need for compact management intelligence. However, this is not enough. Management has the responsibility of learning the capabilities and limitations of the system which produces this intelligence.

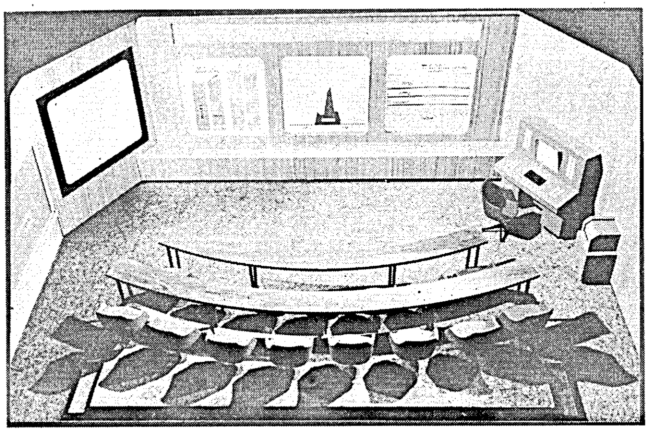
Let us look for a moment at the typical middle management executive through the years. He has seen three data processing conversions: from a manual system to punched card, from punched card to the electronic computer, and now from the computerized batch-processing system to the on-line real-time system. Each time, the executive participates to some extent in the feasibility study and each time, the systems analyst probes the manager's mind to find out what information is needed. Each time, the manager's answer is essentially the same, "Give me just what I'm getting, only faster."

Management must, in the end, set forth what information is needed to attain the company's objectives and must further specify what form this information should take. In order to fulfill this requirement management must participate freely and extensively in the development of the real-time system.

The on-line real-time management information system has unparalleled capability to deliver concise, meaningful, and timely data to all levels of management. It is the only system that can deliver information and management intelligence in a compact form and within established response time. In the end, the information generated sharpens the decisions that in turn shape the future of the company.

The management control room (Fig. 11) exemplifies what we are aiming for. Here status and trend information can be displayed in real time. Statistical analysis and simulations can be run and alternative paths explored. We cannot attain this goal until management understands the real-time information system and learns to use it properly.

Fig. 11. Management Control Room



conclusion

What are our immediate and far-reaching needs? First, hardware. We need more flexible, more reliable, and less expensive hardware. There is no doubt but that we will get this.

Second, a better understanding of systems design and programming problems and how to solve them. From this understanding will come more formal rules for management information systems.

Finally, and most important, the cooperation of management. Every real-time management information system has two goals: the efficient accomplishment of its clerical and control functions, *and* the use of information to produce compact management intelligence — intelligence necessary for the dynamic guidance and growth of the company. ■

The unpublished paper by R. V. Head, mentioned in the references for part I of Mr. Ream's article, will be appearing in a book by Mr. Head,* Real-Time Business Systems, *to be published this fall by Holt, Rinehart and Wintson.

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IBM'S NEW SYSTEM/360

IBM this month announced a new family of computers. Called the "System/360," the line includes six basic main frames covering a broad performance range . . . from the 1401 to STRETCH-plus. Cycle times range from 1,000 to 200 nanoseconds. Main core capacity ranges from 8K to 512K (524,288 characters); a bulk core store offers a maximum capacity of 8-million characters, each directly addressable and available in eight usec. Also available: drums and discs. The family includes 44 I/O devices; 26 of them—including a CRT console, 340K hypertape, a hopped-up 1311, and a 400-million-character random access memory—are brand new.

The six basic systems—Models 30, 40, 50, 60, 62, and 70—are source-language compatible. All share a common instruction repertoire. This includes a standard set of 88 operations, 42 floating point op codes, and eight decimal instructions. In addition, a read-only store is used to process "most" 1401 programs. Word lengths are 8, 16, 32 and 64 bits.

Additional features include memory protection, a "local store" of 16 general-purpose registers, direct addressibility of up to 16-million characters, and a multiplexor channel for the Models 30, 40 and 50.

Software will include FORTRAN, COBOL and new programming language compilers, designed to operate under monitor control. The new family makes use of microelectronic, or hybrid, circuits: transistors and diodes are mounted on a passive ceramic substrate one-half-inch square.

Prices range from roughly $2-3000/month for a typical Model 30 configuration to some $110K/month for an average 70. An 8K Model 30 with four slow-speed tapes, printer and card reader would rent for approximately $5800/month.

Here is a general description of some of System 360's more important features:

Each model of the IBM System/360 consists of a central processing unit—19 combinations of processing speed and memory size are available—a system console and input/output equipment. System/360 includes Models 30, 40, 50, 60, 62 and 70.

Each processor has a main memory; a local store in which index and address registers and arithmetic results are kept; an arithmetic section where additions and comparisons are actually done; and a control section which, in all but one processor, uses read-only storage to tell the arithmetic unit how to accomplish a desired task.

All programs written for the System/360 can be run on any of the processing units—as long as there is sufficient storage and input and output units and no timing dependence in the programs. The 142 operation codes of System/360 machine language are accepted as easily by one processing unit as by another. Input and output equipment such as tape drives, disc files, data cell drives, printers and card read punches can be attached to various processing units.

The difference in the processing units are the range of memory sizes, the operating speed of the functional parts of the processor and the width of the data path—that is, the number of characters the machines move at one time. For instance, the smallest processor moves only one character at a time while the largest moves eight.

System/360 will make use of a "hierarchy of memories." This is a selection of storage facilities ranging from those having cycle times measured in nanoseconds to core memory with cycle times in microseconds . . . and extends to external storage devices such as drums, discs, tapes and strip files with access times that range from milliseconds to tenths of a second. Units such as these provide the ability to store hundreds of millions—even billions—of characters of information on-line with System/360.

360 Memory Performance

Model	Maximum Size In Characters	Cycle Time Per Word In Micro-seconds	Word Width In Data Bits	Effective Cycle Time Per Character
30	64K	2.0	8	2.0 microseconds
40	256K	2.5	16	1.25 "
50	256K	2.0	32	500 nanoseconds
60	512K	2.0*	64	250 "
62	512K	1.0	64	125 "
70	512K	1.0*	64	125 "

*Interleaving will give these memories added speed.

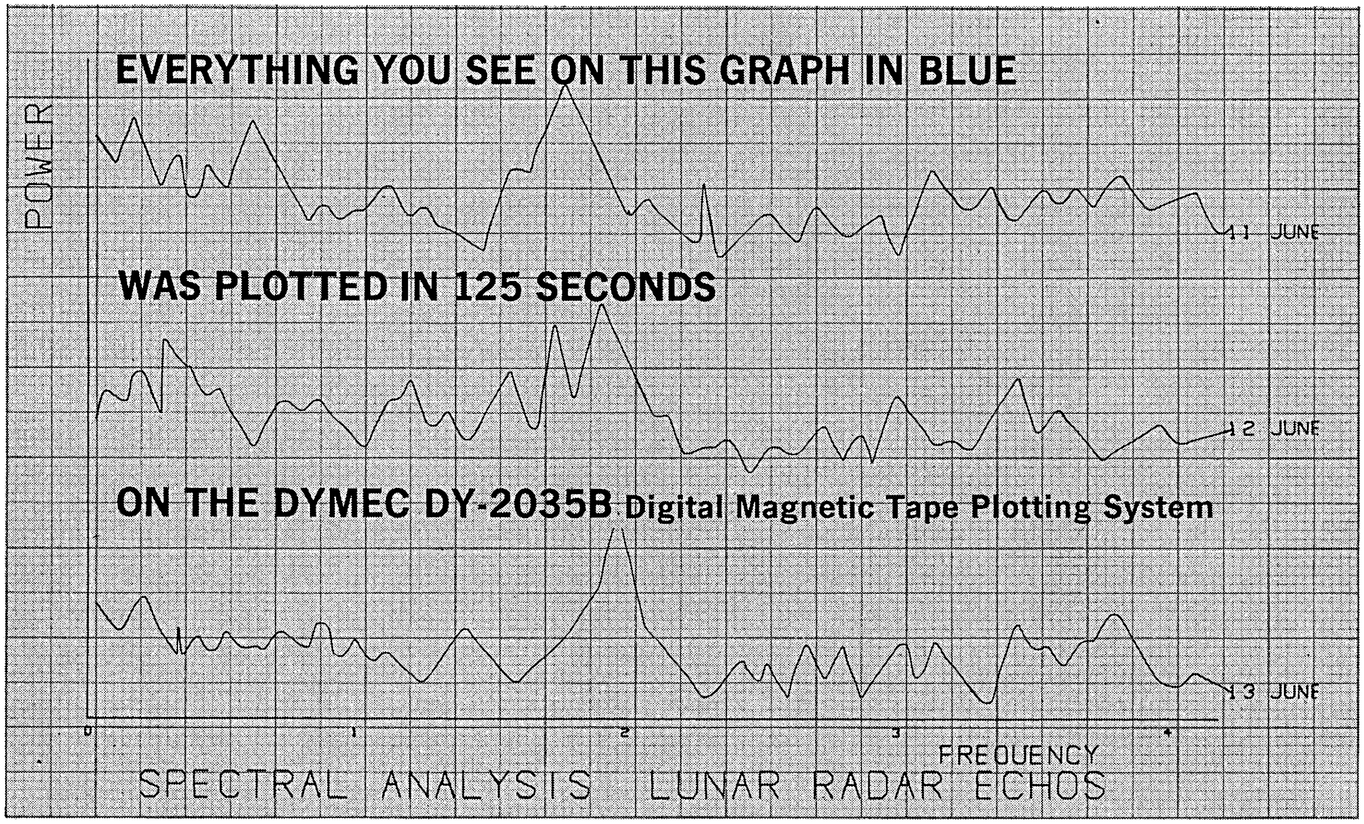
large core storage

One of the most important components in the System/360 hierarchy of memories is the new IBM 2361 core storage. It provides core storage units of one-or two-million character capacity with an eight microsecond cycle time. As many as four units of the large capacity memory can be attached to the largest models of System/360—providing over 8,000,000 characters of storage—all directly addressable.

storage protection

A feature of System/360 is storage protection. It allows several programs to reside in core storage at the same time while one is being executed. It also allows transfer of data from peripheral equipment to memory while other programs already are in memory. Storage protection eliminates danger that one program would inadvertently be placed over, and thereby destroy, another program.

Here is how this storage protection is achieved. Incoming data is assigned a series of bits which are used to identify a block within storage. If the incoming data is not directed

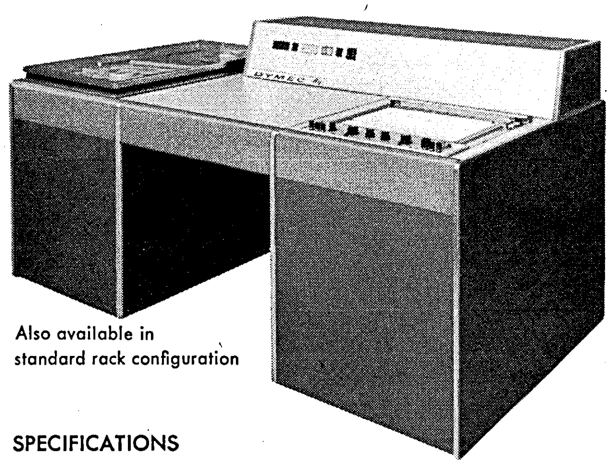


Fast plotting of digital computer data stored on magnetic tape is yours with the DY-2035B System which provides an average plotting speed of 4 inches per second, with slewing as fast as 20 inches per second.

You get more plots for less money. Besides plotting time, you save valuable computer time . . . tape for a 12-minute plot can be prepared in less than 1 minute in the computer. No expensive editing hardware is required. All system operating commands are written directly on the magnetic tape by the computer programmer. Programming documentation and card deck written in FORTRAN II are provided with the system. Check the graph above, including axis scaling and annotation . . . one typical example of the countless computations that the DY-2035B can put in more useful, meaningful x-y chart form.

Easy to use, too. Since all system operating instructions are on the plotting tape, operator responsibility is minimized . . . in fact, the system will operate unattended. An addressable tape search, forward or backward, simplifies finding the exact plot you want. Push a button and plot. Draw smooth graphs or point-plots.

Check the brief details here. Call your Dymec/Hewlett-Packard field engineer for more. Then think about moving fast . . . the DY-2035B does, and it's ready for delivery. More plots, faster, for less money.



Also available in standard rack configuration

SPECIFICATIONS

Plotting speed:	4"/second (slewing speed 20"/sec.)
Plotting accuracy:	Continuous curve, better than 0.2% of full scale; 0.075% with optional 30" x 30" plotter
Resolution:	Binary input: 12 bits of straight binary for each axis BCD (see options): 9999 counts each axis
X-Y recorder:	15" x 10" plot size, automatic chart advance available
Options:	BCD input, 30" x 30" x-y recorder Automatic symbol plotting, tape command (16 symbol printer) Automatic chart advance
Price:	$25,950

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CIRCLE 27 ON READER CARD

to the area indicated by the identification bits, an error condition occurs and the machine reverts to a special routine for the handling of this condition. The identification is also investigated to make sure that the storage area is actually available. If not, the machine reverts to the same error routine in search of another area. Memory protection confines a program coming in to any number of 2,048-character blocks in storage. This feature is especially important in a data communications environment.

local store

Local store is used by System/360 for several things. Here indexing registers are maintained for keeping track of addresses and for storing results of intermediate arithmetic. Local store also provides a place for control words of the programs residing in core storage.

Registers are often loaded and unloaded into main memory to make room for intermediate steps. To eliminate this loading and unloading wherever possible, System/360 processors are equipped with sixteen 32-bit wide floating point registers for accumulating floating point results. The added number of registers also makes possible far larger direct addressing capabilities . . . of up to 16,000,000 characters.

system compatibility

All models of System/360 operate under the same set of instructions through the help of the microprogramming technique. System/360 has been designed as a single system with identical input and output interfaces, an identical set of instructions and identical basic organization.

A user of the System/360 can acquire a more powerful processor and increase the number of tape or file units. If he wants to add small regional computing centers to a large centrally-located processing headquarters, the smaller System/360 installations would have no difficulty interpreting his programs. This type of "downward compatibility" is possible providing adequate memory and input/output units are available and the programs are not time-dependent.

1401 compatibility

Compatibility with the IBM 1401 data processing system has been made possible with a special feature in System/360 Models 30 and 40. Stored logic, or read-only storage, is used for translation.The 1401 machine language operation codes are directed into a read-only storage. There they are translated into signal patterns that will cause the same things to happen—an add, a move to storage, the reading of a card—that would have happened in the 1401.

instruction repertoire

Basic to all models of the System/360 is a "standard" set of 88 operations which include binary and logic operations. A floating point set of operations numbers 42 additional operations to accomplish arithmetic with floating point notation. Finally, decimal arithmetic includes a set of eight operations to accomplish arithmetic with decimal numbers.

In addition to these 138 operation codes, there are two codes for memory protection and two which the machine can use for a direct control feature to get an outside device to read or write without going through a channel.

Variable length instructions are used. Some have no addresses. Others have one or two addresses. The programmer selects the instruction best suited to the operation he wants to perform and location of data he wants to use. This tends to speed programming, to reduce the size of programs, and make machine operation more efficient.

coding system

The IBM System/360 uses an eight-bit binary coding system which permits double packing of decimal digits. Alphabetic characters and special symbols take eight bits with a ninth bit used for odd parity checking. Decimal digits use only four bits, so that two digits can be packed into each eight-bit unit. Decimal arithmetic is actually performed in this double-density format, thus conserving processing time. The nine-bit code is employed on all input and output equipment. Tape drives are equipped with nine-channel heads.

While the eight-bit code—with a ninth parity bit—is standard mode for this system, the processing units will accept the new seven-bit American Standard Code for Information Interchange (ASCII). This code will not permit double-density packing of decimal digits, but will otherwise be handled just as the System/360 code is.

checking

All data paths on the System/360 have continuous monitoring for validity checking of data. Checking is done at eight points within the processor. When an error condition is detected, a controlled interrupt occurs. An error routine is summoned and the error condition is resolved. At the time of the error, the machine situation is captured and stored, so that upon resolution of the error, the program can be resumed where it left off.

Communication and Channel Facilities

Each channel on System/360 is an independently operating device which serves both as a data path and as the controller for all data traffic to and from the input and output devices attached to it. There are two types of channels: the selector and multiplexor channels.

The selector channel is designed primarily for such devices as tape units and disc files. When the selector channel is directed to make connection with one input or output unit, all other units on that channel are locked out until the first unit is released.

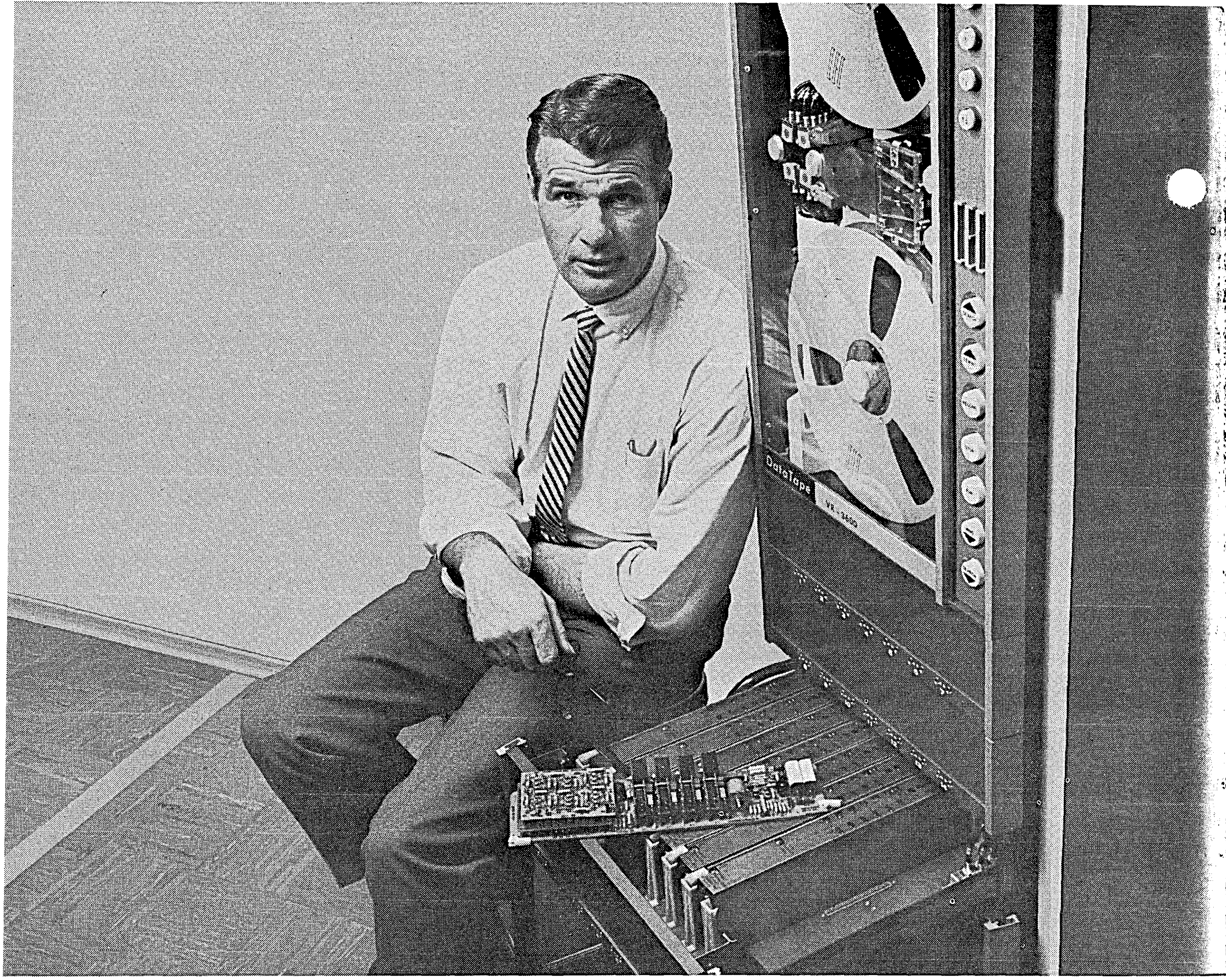
The selector channel is capable of handling high-speed units overlapped with processing, so that a stream of data can be fed to storage while the processing unit is performing arithmetic or logic operations for another phase of the program.

By linking certain input or output units to more than one channel, a variety of ways are open to reach the device, even if other units are occupying one or more of the available channels.

A multiplexor channel is part of System/360 Models 30, 40 and 50. These are the configurations which will most effectively be used to control card read punches, printers, and communications terminals.

The multiplexor channel allows attachment of up to eight data communications units. Up to 31 communications lines can be attached to each of these units. And literally hundreds of terminals can be attached to each of the communications lines. In place of the communications lines, printers, card units and data terminals can be attached to the multiplexor channel.

The multiplexor channel receives a message from an input unit one character at a time in its usual method of operation. In between these characters, the multiplexor



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There is no other recorder/reproducer available today equal to the VR-3600. Its extremely wide bandwidth multichannel system is superior in performance to any comparable instrumentation. In addition, the VR-3600 has the capacity to store vast amounts of data on a minimum amount of tape.

Consequently, the VR-3600 is now considered the ideal "universal" recorder—for the most demanding laboratory use or the storing of pre-and post-detection telemetry information. The following advantages will explain why.

- Each of its 7 or 14 record/reproduce channels can be used for data storage in the 400 cps to 1.5 mc frequency range.
- Signal-to-noise ratio is the highest; distortion the lowest.
- Record and reproduce amplifiers are solid state; the direct system fully amplitude and phase equalized.
- Pushbutton selection of six transport speeds along with associated electronics.
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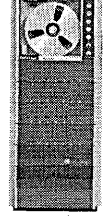
- Tape is constantly cleaned by vacuum/ionization; tension constantly maintained by closed-loop servo control.
- Tape transport skew is less than 0.5 usec; flutter less than 0.30% p-p at 120 ips.
- Automatic end-of-reel sensing stops tape without leaders; transfer switch provides start command for nearby recorder.
- Individual plug-in-equalizers (6 per amplifier) meet all specifications simultaneously. Buy only those required, then set and forget.
- The system may be supplied in single or dual rack configurations, with or without a dolly.

For *all* the outstanding facts about the VR-3600, call CEC or write for Bulletin 3600-X1.



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CIRCLE 28 ON READER CARD

channel sandwiches a character from each of the other units that also want to communicate with the processing unit. There can be up to 248 messages interleaved together on this channel.

All messages are tagged and are separated and assembled within storage by unit control words. Only after being assembled is the message actually serviced by the processing unit. Outgoing messages are tagged so that they are directed to the proper peripheral unit. This channel produces a time-sharing effect, so that many terminals are being served although each terminal appears to have the processor to itself.

The multiplexor channel can also operate like the selector channel in what is called burst mode. This restricts communication to one unit but boosts speed to 200,000 characters a second.

Peripheral Equipment

System/360 peripheral equipment includes storage devices, visual display units, communications equipment, card read punches, printers, a paper tape reader, and character recognition devices. A summary of each type of unit follows:

storage devices

The 2321 data cell drive. Information is stored on and retrieved from magnetic strips, which are held in cells mounted vertically around a rotating cylinder.

Eight data cell drives, with up to 6.4-billion digits, can be linked to one control unit.

The *2311 disc storage drive* holds 7.25 million alphanumeric characters of information, or up to 14.5 million digits, in its 10-pound removable and interchangeable disc pack. Up to eight 2311 drives can be attached to one control unit to provide an on-line capacity of 58-million characters or up to 116-million digits.

magnetic tape equipment

The *IBM 7340 hypertape drives* are designed to read or record information at a rate of 340,000 alphanumeric characters a second or up to 680,000 digits a second.

The *2400 series nine-channel magnetic tape unit* reads and records information in nine data tracks across ½-inch wide tape. Also available with the 2400 series, is a seven-track compatibility feature which enables reading and writing of data at high speeds.

The 2400 series is available in four types. Each type comes in three models, with different information transfer rates. Features available include backword read, and simultaneous read/write.

drum storage

Two drum storage units are available with System/360.

visual display units

The *2250 display unit* provides a dynamic visual presentation of information stored in the computer or in storage files, drums and tapes. An operator at the display can monitor the progress of his program or solution, and can modify and intervene as necessary.

The major element of the 2250 is a console with a 12-inch square display screen (a 21-inch cathode ray tube) on which tables, graphs, charts, alphanumeric characters, or the lines and curves of drawings can be displayed as a series of points. When the full display area is used, 3,848 alphanumeric characters—the contents of a page of information—can be viewed. A built-in electronic marker helps the operator edit messages. When the display console is used as a point plotter, it can plot graphs, charts and drawings with the precision of a square matrix of 1,024 points, or more than one million individually addressable points.

Buffer storage for the 2250 is available in 4,096 and 8,192 character capacities. These buffer storage units hold points, lines and position instructions which may be read from or written at a maximum rate of 238,095 characters a second.

Other features of the 2250 include: A typewritter-like keyboard for entry of all alphanumeric information and control of the electronic marker; a light pen for communication between operator and processor; the *IBM 2840 display control,* which permits up to eight display units to operate in an economical time-sharing configuration. Up to 16,384 characters of storage are available with 2840.

The *1015 inquiry display terminal* is designed to operate as an inquiry device for System/360 Models 30, 40 and 50.

Information is placed into the computer through the 1015's alphanumeric keyboard and is simultaneously displayed on its four-inch-square screen. The 1015 then displays a reply to the inquiry on its screen.

Information (36 alphanumeric and 23 special characters), is displayed at a rate of 600 characters a second. The viewing area has a 30-line capacity of 40 characters each.

communications equipment

The new *IBM 1070 process communication system* is designed for on-line data transmission between remote process locations and a central computer.

Through the use of a multiplexor terminal unit, the *1071,* the system can connect, via four transmission lines, up to 98 terminal stations to the central processor. The processor controls all transmission sequences to and from the terminal stations, performs, checks and handles the required calculations. Input/output devices such as storage files, magnetic tapes, visual displays and printers also can be attached to the processor.

The *7772 audio response unit* can be attached to System/360 Models 30, 40 and 50 through their multiplexor channels. It links the processor with a telephone network to provide a recorded voice response to inquiries made from telephone-type terminals.

The *2701 data adapter unit* provides direct connection for a variety of remote and local external devices over a maximum of 48 half-duplex lines.

The *IBM 2702 transmission control,* which operates at lower speeds than the 2701, is designed for use with System/360 Models 30, 40 and 50. Under interleaved operation, there is an eight-bit buffer per line on the multiplexor channel. Messages to and from the 2702 can be of any length. The basic data communications unit has up to 15 half-duplex lines. It operates at speeds from 75 to 600 bits per second in a start/stop mode.

Two card read/punches are available with System/360.

Several existing magnetic ink and optical character recognition devices will also be available. ■

SJCC exhibit preview

MAKING THEIR DEBUT

PHOTOCIRCUITS CORP.
Glen Cove, N.Y.
Booth No. 64-5

Two paper tape readers and a servo motor being introduced include the 500R and 500RM. The former is a photoelectric unit with a printed motor direct capstan drive. Free-running speed is 500 cps, line-by-line speed is 200 cps, and wind/search is at 1,000 cps. The 500RM is a militarized unit with similar speeds. The Incredyne is a servo motor for high-speed dp hardware. It has an undamped mechanical time constant of 1.8 msec, and rated speed is 3,300 rpm at 40 volts dc.

RADIATION, INC.
Melbourne, Fla.
Booth No. 111-13

Two sets of compatible resistor-transistor digital logic modules operate at bit rates up to 200 kc and to 1 mc. These include four-input NOR, counter shift register, power inverter, emitter follower, complementary driver, and differentiator. They measure 0.4 x 1 x 1.1 inches, with a ¼-inch pin protrusion. Welded circuitry is molded in epoxy and mounted on cast aluminum frames.

CALIFORNIA COMPUTER PRODUCTS INC.
Anaheim, Calif.
Booth No. 77-9

The 670 plotting system produces 240 data reduction graphs or 300 sales analysis curves, cost reduction charts, etc., from a 2,400-foot reel of mag tape. It plots from single or multiple addresses, and provides automatic search for selected addresses. Block addresses are visually displayed during plot and search modes. Computer program controls automatic annotation with curve identification, scale factors, origins, grid and axis generation.

AKTIEBOLAGET ATVIDABERGS INDUSTRIER
Stockholm, Sweden
Booth No. 104-6

Reportedly making their U.S. debut are the Facit Carousel mag tape memory, the 1500 paper tape punch, and the 1000 reader. The Carousel has 64 removable reels, each with a capacity of 80,000 (4-bit) parity-checked decimal digits. Minimum access time is 0.2 seconds. The PE 1000 reads 5, 6, 7 or 8-track paper tape at 500-1,000 cps, and the 1500 punches the same tapes at up to 150 cps.

COOK ELECTRIC CO., DATA-STOR DIV.
Skokie, Ill.
Booth No. 66-7

A new addition to the model 150 family of incremental tape recorders, a unit capable of 650 cps stepping, will be among the units to be shown. This is a modification of the 150-cps unit introduced last fall. Other items: an analog drum recorder and a paper tape reader, both designed for operation in extreme environmental conditions. The model 111 reader operates bidirectionally at 400 cps in zero to 120°F temperatures.

PACKARD BELL COMPUTER
Santa Ana, Calif.
Booth No. 125-8

The operating PB440 computer will have an 8K main memory and 256 words of biax memory. Using improved memory units, main memory cycle time has been cut from a former five to three usec. With this first trade show appearance, the company is announcing the start of deliveries of production units. Also to be demonstrated are the PB250 with card reader, and the Mark III analog computer, manufactured jointly with Computer Products Inc.

SYSTEM DEVELOPMENT CORP.
Santa Monica, Calif.
Booth No. 138

The first public demonstration of its time-sharing system with on-line teletype units on the floors of Exhibit Hall will be held by System Development Corp. Central hardware is the Q-32 situated at the firm's headquarters in Santa Monica, Calif., 3,000 miles away. Operations to be shown include on-line programming and debugging using TINT, an interpretive version of JOVIAL; IPL-TS, an on-line verson of the list-processing language IPL-V, and information retrieval using a Synthex program.

GPS INSTRUMENT CO. INC.
Newton, Mass.
Booth No. 176-7

The 10000 is an analog computer using a basic amplifier with bandwidth from d.c. to over one megacycle per second. The central control console has a removable problem board for patching analog information, and separate control board for patching of command elements (integrator timescale and mode controls, logic modes, etc.). Separation of the analog and command information is said to permit system expansion to nearly 300 amplifiers.

RECORDAK CORP.
New York, N.Y.
Booth No. 144-6

Model PE-1A is a motorized microfilm reader with hardcopy output capability. It accepts 16mm or 35mm film, Recordak film magazines, aperture cards, film jackets, and Micro-File Filmcards. The screen measures 11 x 11 inches, speed is adjustable, and magnification lenses are available. Hardcopy prints can be up to 8 x 10 inches.

ELCO CORP.
Willow Grove, Pa.
Booth No. 118

The APCON and BI/CON connectors are for the OEM market. The Apcon consists of plug, receptacle, and contact in a range of connector sizes. Three-way interlock enables various combinations of plugs/receptacles to be hand-assembled and press locked in side-by-side random patterns. Bi/Con has contact measuring 0.035 inch across greatest width, a pattern of nine contacts on a 0.050 inch grid contained within a 0.1 inch square.

GENERAL DYNAMICS/ELECTRONICS
San Diego, Calif.
Booth No. 141-3

An optional feature which enables display of both film-projected data as well as computer-generated information will be debuted. This combined display is made possible through a Charactron tube with an optical window at the rear; film frames are projected through this window. Thus the computer is used to output only the changing data. Colored films can also be used to effect a multi-color display.

CHRONO-LOG CORP.
Broomall, Pa.
Booth No. 178

The 729 is a programmable clock/calendar system which reads the date and time (up to $\frac{1}{60}$th of a second) into any IBM computer using 729 II, IV, V, VI or 7330 tape drive. Up to nine tape drives can be used on the same mag tape channel. The time reading is not affected by programming errors or machine downtime, and does not require daily setting. Reading in of the date and time is under control of the program.

ANELEX CORP.
Boston, Mass.
Booth No. 160-2

Model 80 is a disc file with removable six-disc kits, a capacity of 3.9 million (seven-bit) characters per kit. Each disc surface has two read/write heads (24 per unit), and a solenoid-actuated mechanical linkage retracts heads automatically in case of power failure. The six-disc unit weighs 12 pounds. Head positioning time is 75 milliseconds; average rotational delay: 12.5 msec.

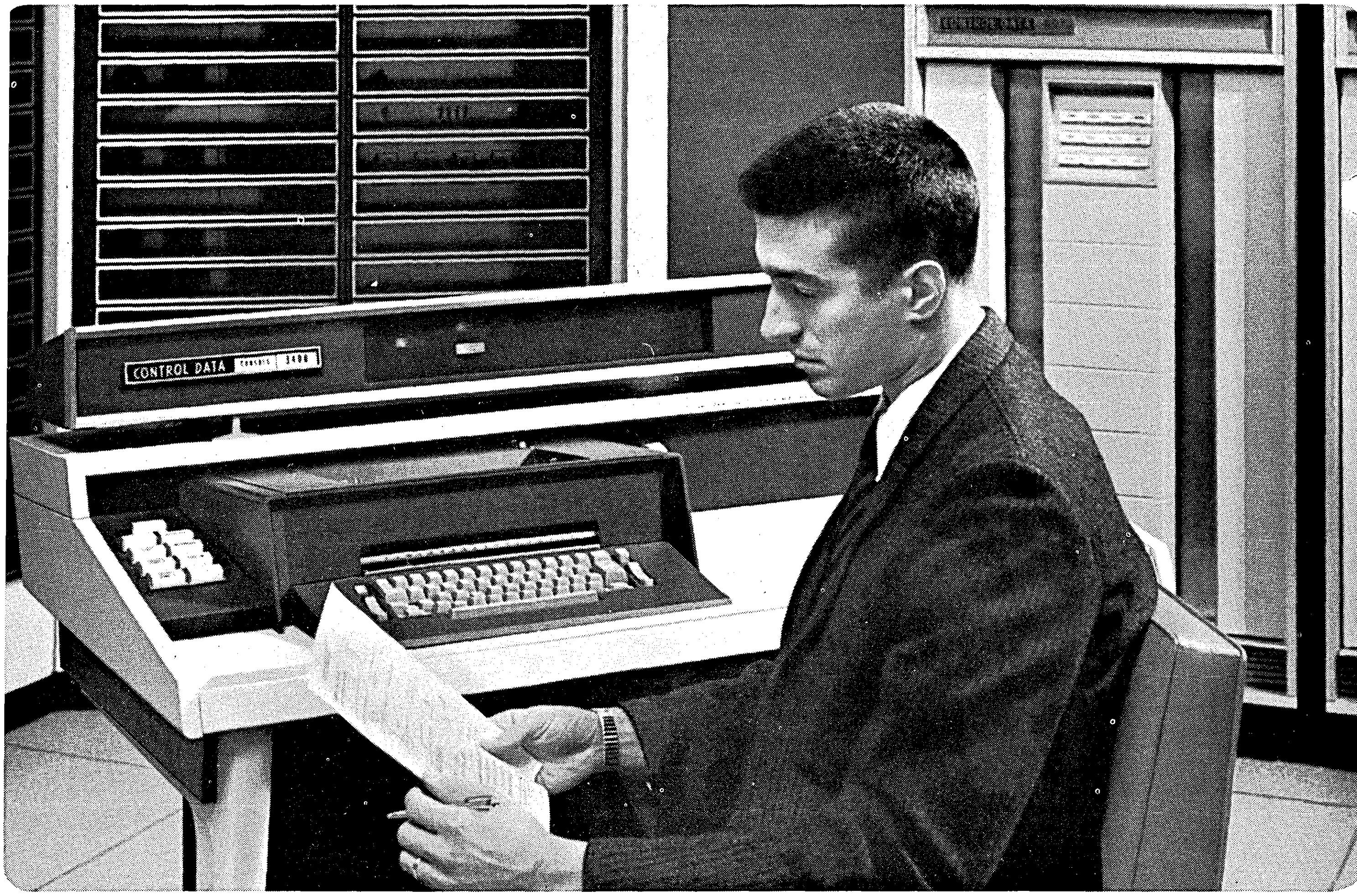
DI/AN CONTROLS INC.
Boston, Mass.
Booth No. 163-4

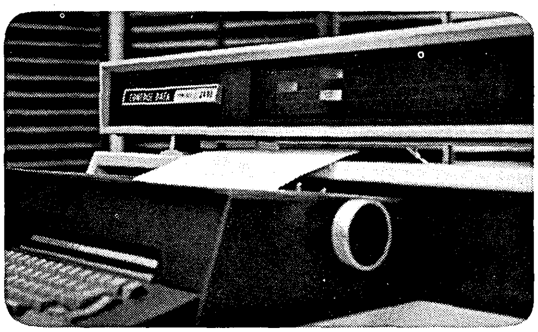
Pulse Interface and Static Interface cards round out the firm's line of magnetic logic cards. The PI-2 provides data input, shift and preset pulses for logic circuits from such sources as contact closures, sine waves, slow voltage changes, etc. The SI-12 consists of 12 transistor inverters which may be connected as six flip-flops for the operation of static displays, etc.

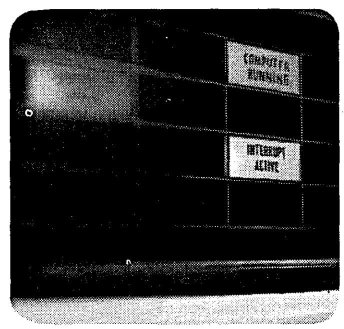
GENERAL KINETICS INC.
Arlington, Va.
Booth No. 190-2

The TC-3 is a portable mag tape certifier. It attaches to an IBM 729 tape drive and, in a single pass, determines which tape areas will give dropout-free operation. Defects are recorded in ink on a circular graphic chart and counted. The operator may select a mode of operation which will cause the tape to stop at a known position where the tape defect may be examined and repaired.

CIRCLE 29 ON READER CARD







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The 3400 uses the same field-proven logic and circuitry developed for the 3600—Control Data's unprecedented large-scale computer system. Further extending this compatibility with the 3600, peripheral systems are interchangeable.

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This system compatibility with the 3600 at medium-scale price is significant in two valuable respects: 3400 price allows users an earlier start in large-scale performance, while the 3400's true upwards compatibility to the 3600 significantly extends the user's system life.

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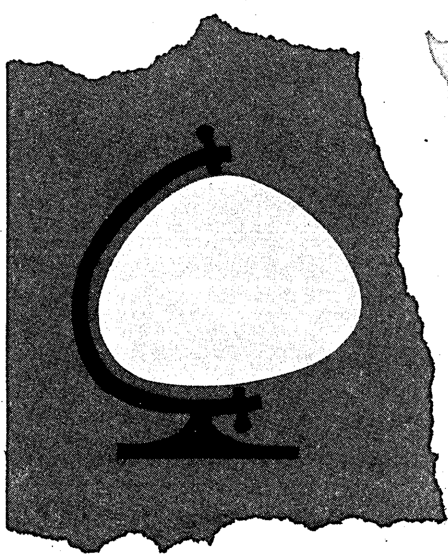

. . . to comprehend

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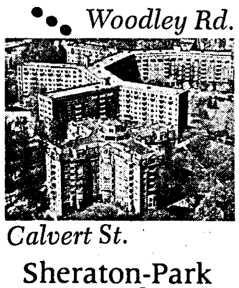

Sheraton-Park Hotel

CON
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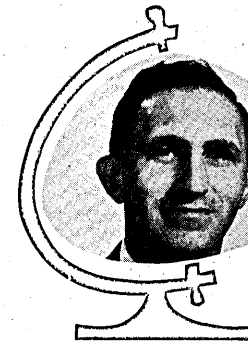
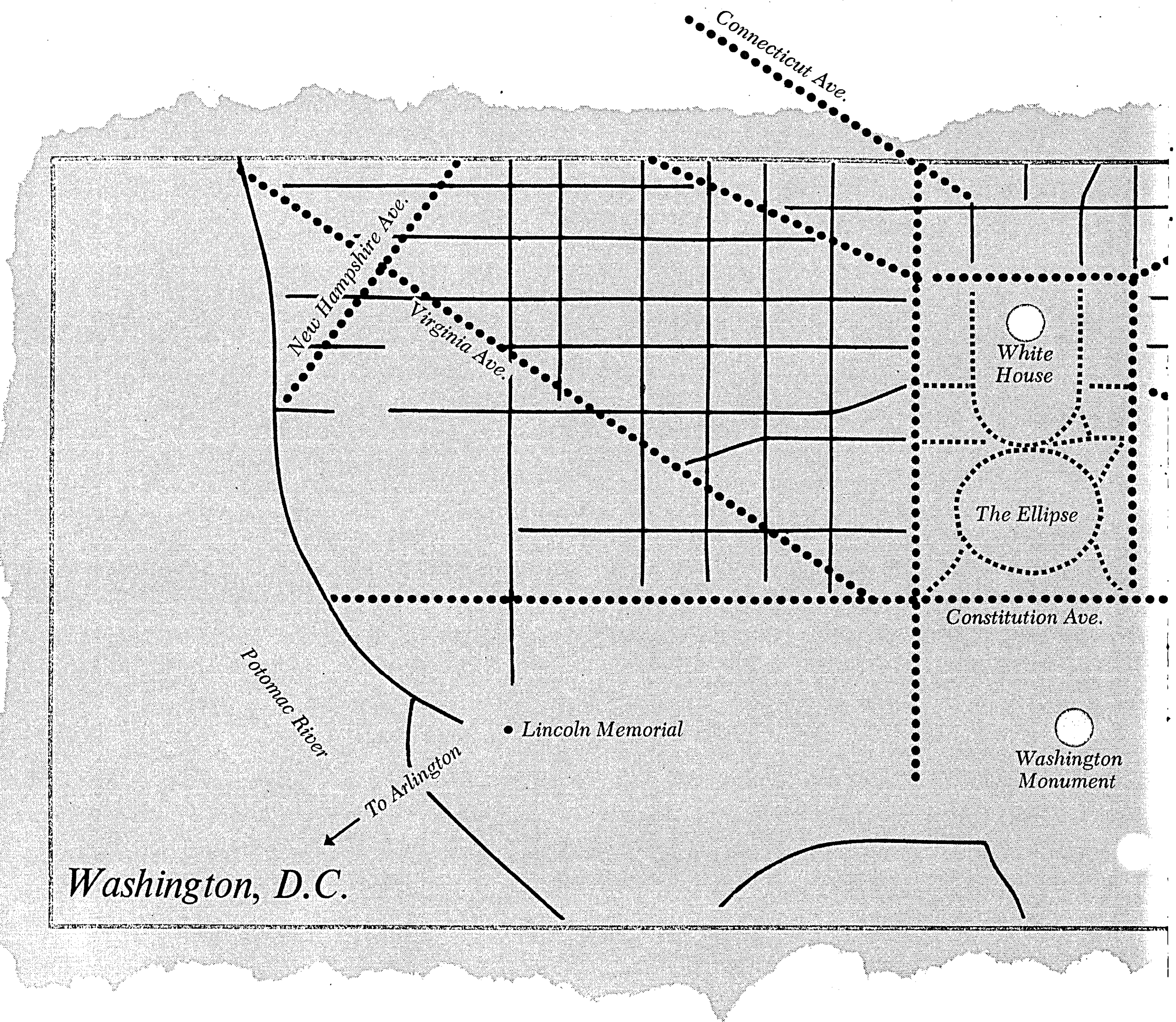




by HERBERT R. KOLLER

The theme of the 1964 Spring Joint Computer Conference, "Problem-Solving in a Changing World," aptly describes the overall purpose of the conference—to appreciate the vast strides being made in the continuing race to keep ahead of the world-wide surge of information and technological advances, and to comprehend the scope of our task in the future.

This year's SJCC will feature more companies sponsoring more new types of hardware and software for more applications than any other joint computer conference.

Making the keynote address will be one of nation's most noted scientific minds, Dr. Jerome Wiesner, former special assistant to the President for Science and Technology, and now with MIT.

A wide variety of fields will be covered at the technical program sessions, each of which will include question-and-answer periods and panel discussions by outstanding people in each area. In addition, several tutorial sessions will complement those in which new developments are presented.

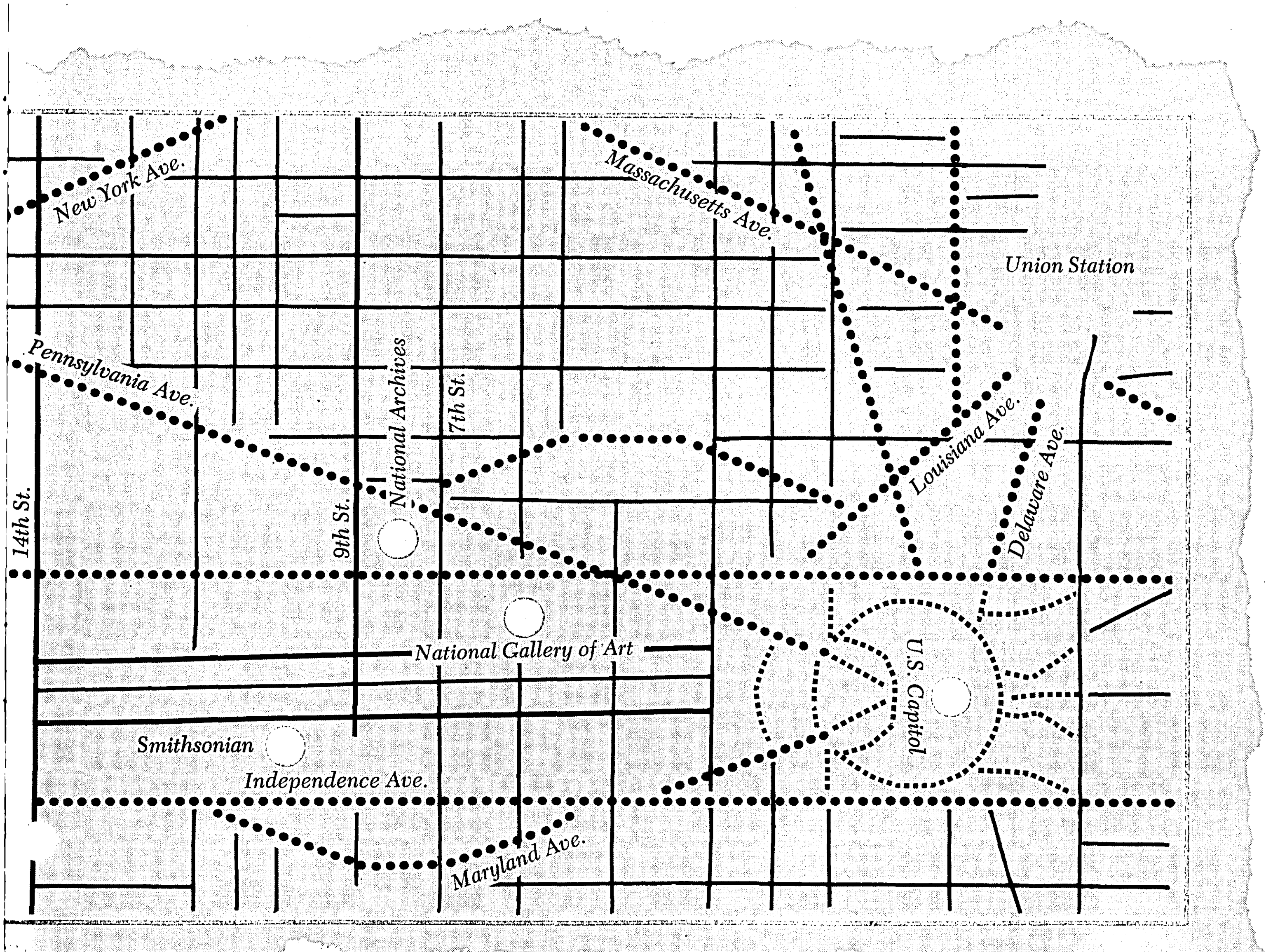
One of the most significant presentations will be a special session on computer education for the blind, including a report on newly-developed techniques for training blind persons for professional computer work.

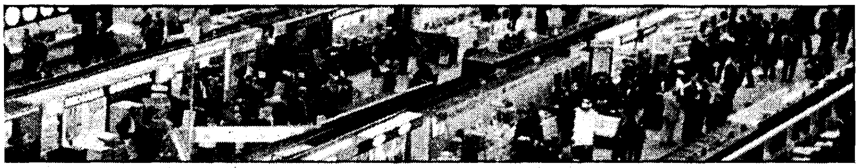
A large number of recent films dealing with computers and information processing technology will be shown continuously at the Computer Science Theater throughout most of the conference.

Among special activities available for attendees will be field trips to some of the outstanding scientific installations in the area, to examine and watch demonstrations of some of the newest computer applications in information technology, weather research and manned space flight.

An extensive program of activities has been prepared for the wives who accompany their husbands to Washington, including a VIP tour of the White House, and visits to Embassy Row and some of the nation's most beautiful shrines.

The committee has spared no efforts in its attempts to make the 1964 SJCC a truly informative one, as well as a highly enjoyable experience for all concerned. We hope you will find it so.





CON FER ENCE PARTICULARS

A special session on "Computer Education for the Blind," a technical session on "Social Implications of Data Processing," and a symposium for local educators are among those scheduled for the 1964 Spring Joint Computer Conference. With the theme, "Problem Solving in a Changing World," the conference will be held on April 21-23 at the Sheraton-Park Hotel in Washington, D.C. As an added feature, three of the technical topics have been split into tutorial and technical sessions.

Sponsored by the American Federation of Information Processing Societies, the SJCC is the 25th national conference. Registration fees are $8 for members of one of the sponsoring societies (ACM, IEEE, and SCI), $10 for non-members, and $2 for fulltime students. Registration desks in the hotel's Continental Room will be open on Monday, April 20, from 5-9:30 pm., on Tuesday and Wednesday from 8 a.m. to 9:30 p.m., and on Thursday from 8 a.m. to 2 p.m. (Early registrants on Monday will receive a free cocktail, compliments of the house).

In the technical program are 12 topics, 14 sessions. Broken down into tutorial and technical sessions are Information Retrieval, Compilers, and Hybrid systems. Other subjects are Business Data Processing, Command and Control, Numerical Analysis, Logic, Layout & Associative Memories, Artificial Intelligence, Multi-Programming, Social Implications of Data Processing, Applications, and Evaluating Computing Systems. These sessions will be held from Tuesday afternoon to Thursday evening.

Tuesday morning at 10, the formal program begins in Sheraton Hall. The keynote speaker, whose topic has not been announced yet, is Dr. Jerome B. Wiesner, dean of MIT's School of Science and former chairman of the President's Science Advisory Committee.

On Wednesday evening, at 8 p.m., there will be a panel discussion on "Establishing Computer Training Opportunities for the Blind."

And at the all-conference luncheon, on Thursday, the speaker will be Sen. Hubert Humphrey (D. Minn.), chairman of the subcommittee on Reorganization and International Organizations, which is interested in, among other things, the documentation, indexing, and retrieval of scientific information.

Social events include the conference cocktail party on Tuesday evening, the luncheon on Thursday and four field trips. They are to the Defense Documentation Center (Tuesday, 1-4:15 p.m.), NASA's Goddard Space Flight Center (Wednesday, 9-noon), the National Library of Medicine (Wednesday, 1:30-4:30 p.m.), and the U.S. Weather Bureau (Thursday, 9-noon). Computer science films also are scheduled.

In Exhibit Hall will be more than 80 exhibitors, including foreign firms. The area will be open on Tuesday from 11 a.m. to 5:30 p.m., Wednesday from 10 a.m. to 6 p.m., and Thursday, 10 a.m. to 5:30 p.m.

An extensive program for the ladies includes an afternoon in Georgetown, tours of the White House, The Mosque, and Embassy Row, and visits to Arlington Cemetery, Lincoln and Jefferson Memorials.

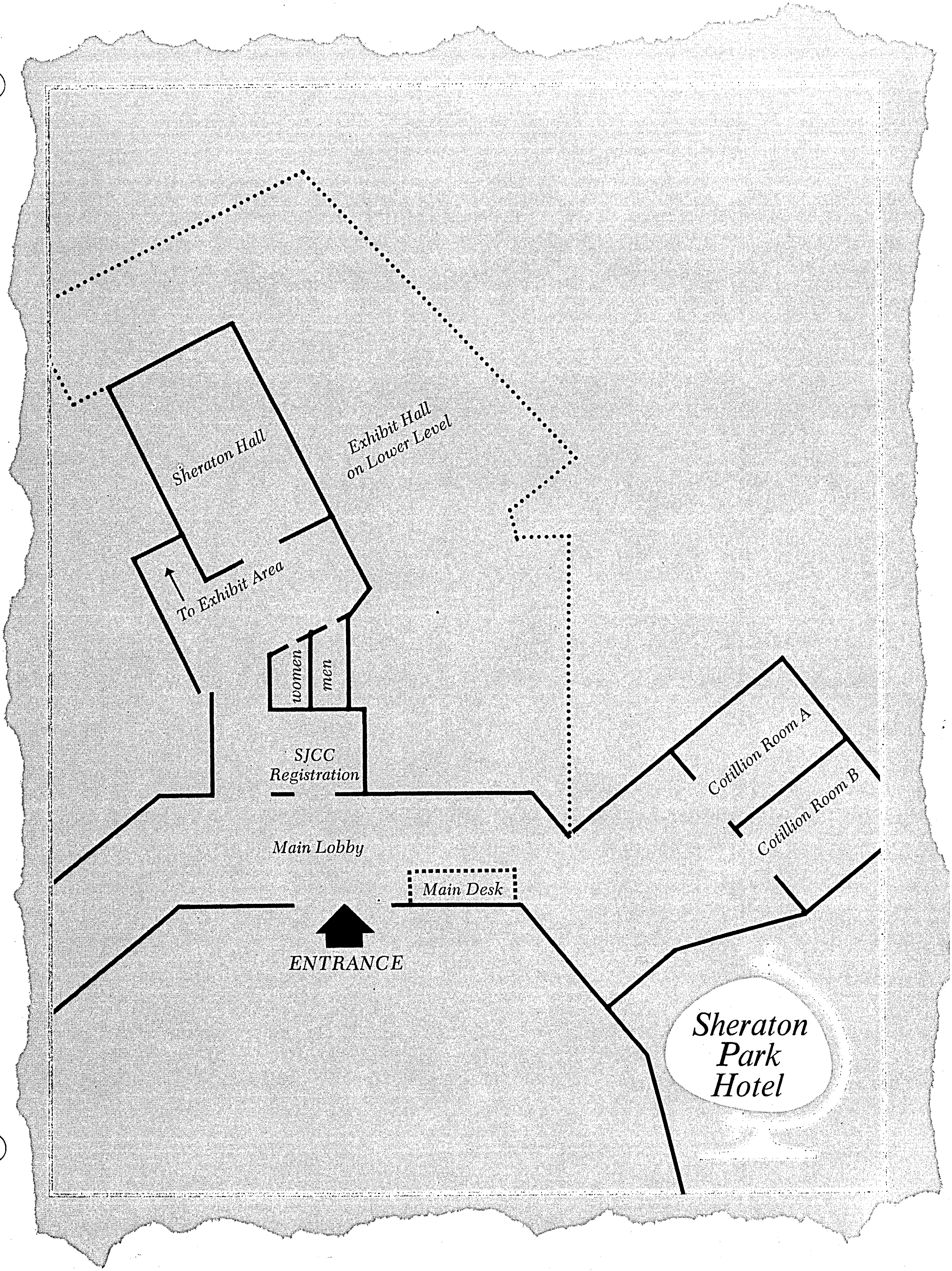


Exhibit Hall
on Lower Level
Sheraton Hall
To Exhibit Area
women
men
SJCC
Registration
Main Lobby
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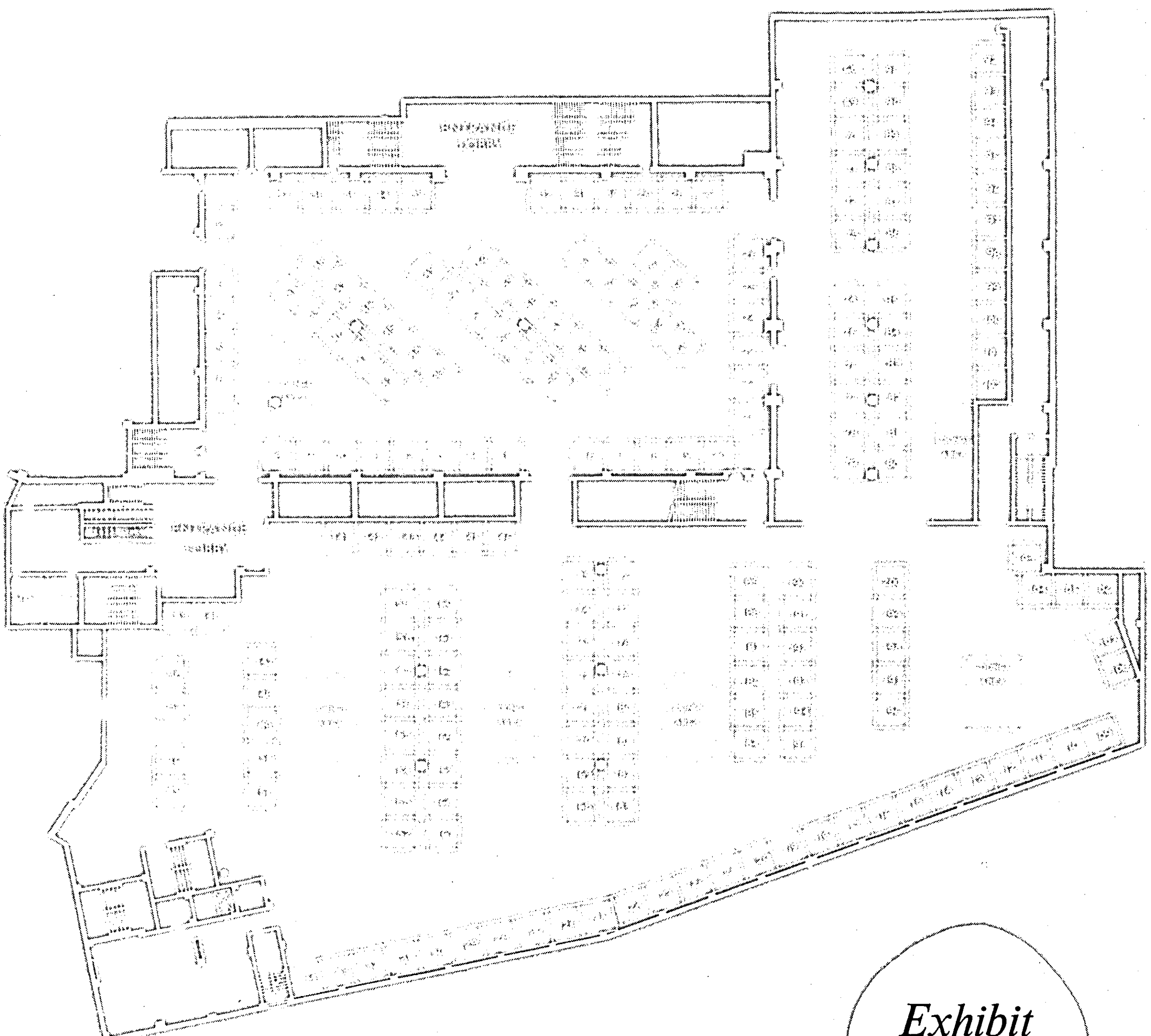
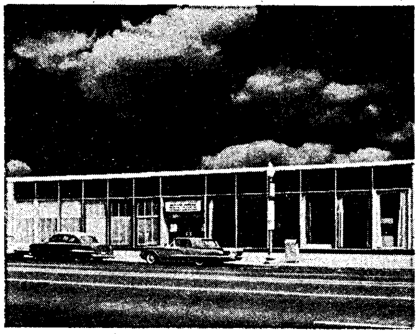


Exhibit Area

THE FIELD TRIPS



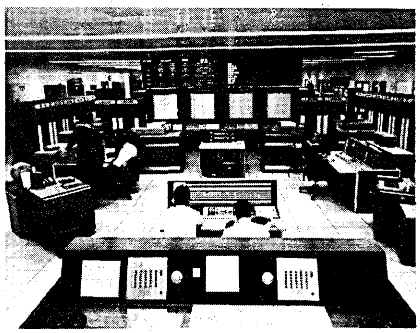
U.S. Weather Bureau

Defense Documentation Center

DEFENSE DOCUMENTATION CENTER

Tuesday, April 21
1:00 to 4:15 p.m.

The Defense Documentation Center, in Alexandria, Va., stores and retrieves scientific and technical documents without charge to DOD contractors and military groups. It will demonstrate this capability with a Univac 1107 computer by processing bibliographic searches and outputting entries from a 700-lpm printer which has 102 (upper and lower case) alphanumeric characters. The center also publishes the semi-monthly Technical Abstract Bulletin, which is distributed to some 6,000 users, and maintains a file of 350,000 documents on eight Fastrand drums. Capacity: 500 million alphanumeric characters. It processes annually more than 1¼ million requests for documents, and expects to handle 9,000 bibliographic searches this year.

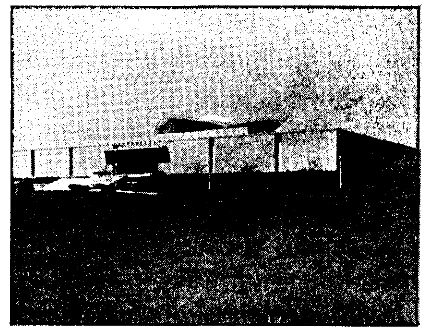


Goddard Space Flight Center

GODDARD SPACE FLIGHT CENTER

Wednesday, April 22
9 a.m. to noon

Scheduled at NASA's Goddard Space Flight Center in Greenbelt, Md., are two demonstrations of satellite orbital and recovery computations. These are the manned space flights of Projects Mercury and Gemini and the Nimbus meteorological satellite. The latter, with a launching scheduled soon, is a follow-on to the TIROS program and, like the latter, has the capability of transmitting photographs of cloud covers upon interrogation from land. Computer configurations include the IBM 7094.



National Library of Medicine

NATIONAL LIBRARY OF MEDICINE

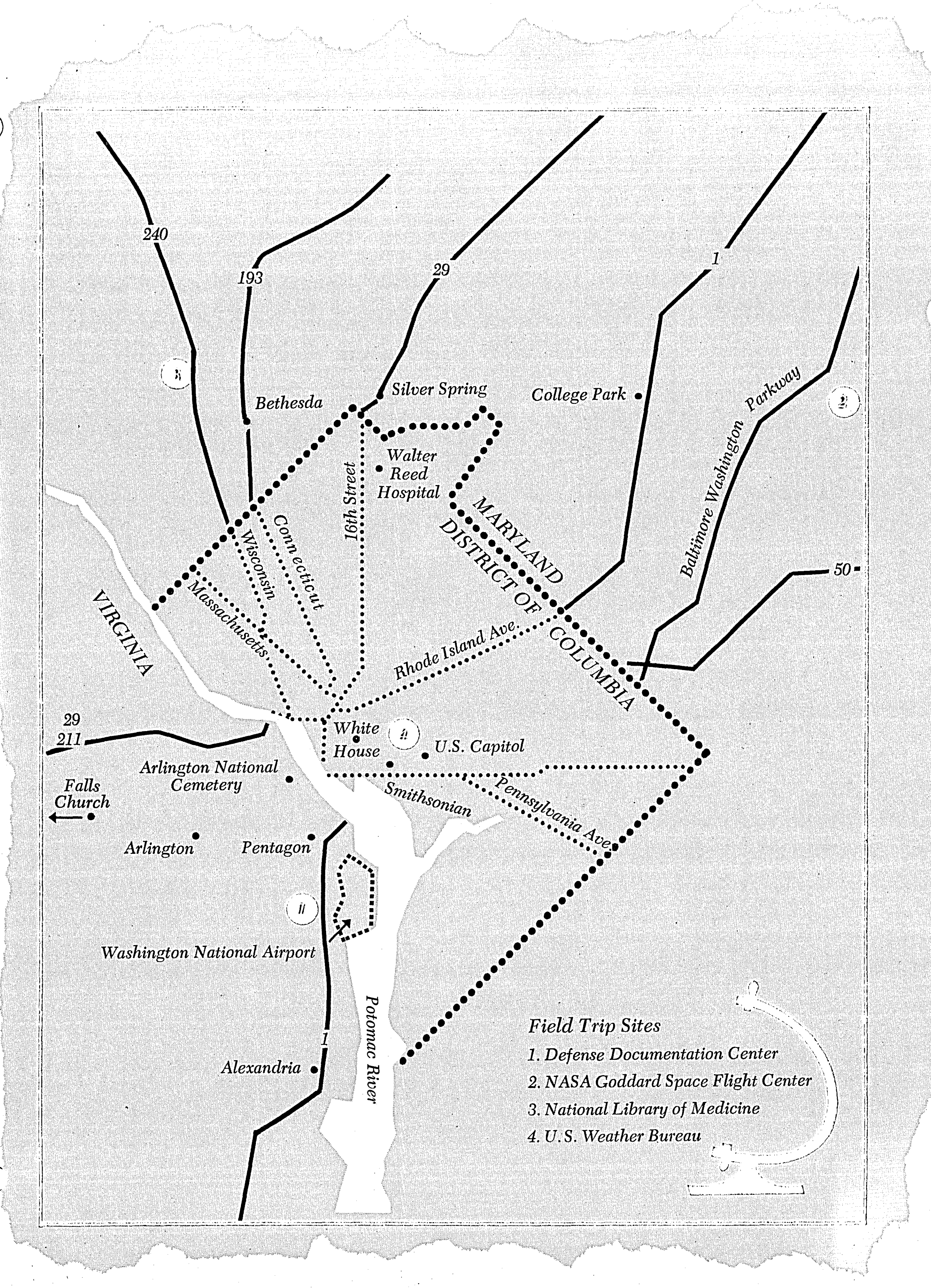
Wednesday, April 22
1:30 to 4:30 p.m.

The first application of a computer to the problems of scientific information handling in a library will be shown at the National Library of Medicine, Bethesda, Md. The library is part of the U.S. Public Health Service. MEDLARS (Medical Literature Analysis and Retrieval System) consists of a Honeywell 800 computer and a special photocomposition machine. It is hoped that the latter, which prints at 440 cps from a font of 226 characters, will be installed in time for the tour. Output from the system includes a monthly *Index Medicus,* which references more than 10,000 articles per issue. Some 14,000 journal issues were indexed in 1961, a figure expected to reach 25,000 by 1969. Also output are recurring and demand bibliographies. The former are current-awareness lists of citations in specialized medical subject areas, and the latter is a special service for anyone engaged in medical research or practice.

U. S. WEATHER BUREAU

Thursday, April 23
9 a.m. to noon

The Weather Bureau tour will be through a simulation research laboratory, and not an operational center where day-to-day forecasts are made. Here, a STRETCH computer is being used in long-range forecast research projects. With a complicated model of the earth's atmosphere, scientists are able to vary such parameters as the earth's topography and water cover, wind velocity and temperature. They can even turn the sun off and on. Some 12-18 hours of STRETCH-time are required for a simulated 24-hour forecast; the longest attempted has been 200 days. With real data: a five- to six-day prognostication.



240
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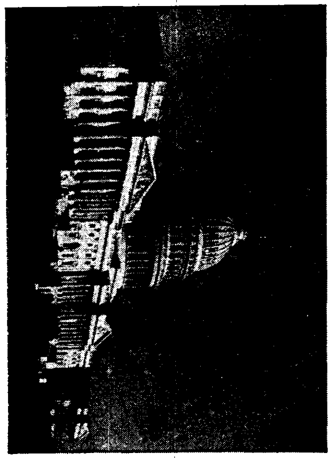
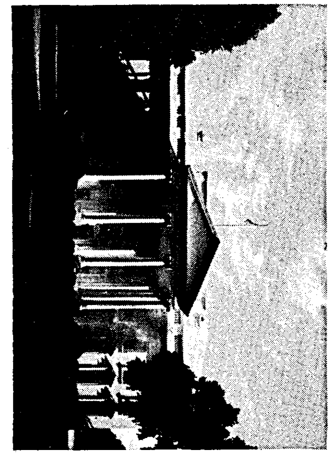
29
1
Bethesda
Silver Spring
College Park
Baltimore Washington Parkway
Walter Reed Hospital
16th Street
Connecticut
Wisconsin
Massachusetts
MARYLAND
DISTRICT OF COLUMBIA
VIRGINIA
50
Rhode Island Ave.
29
211
White House
U.S. Capitol
Arlington National Cemetery
Falls Church
Smithsonian
Pennsylvania Ave.
Arlington
Pentagon
Washington National Airport
Potomac River
1
Alexandria
Field Trip Sites
1. Defense Documentation Center
2. NASA Goddard Space Flight Center
3. National Library of Medicine
4. U.S. Weather Bureau

. . . and some SIDE TRIPS

Capitol Building



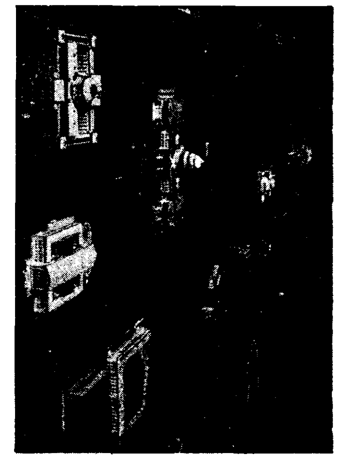
White House, North Portico

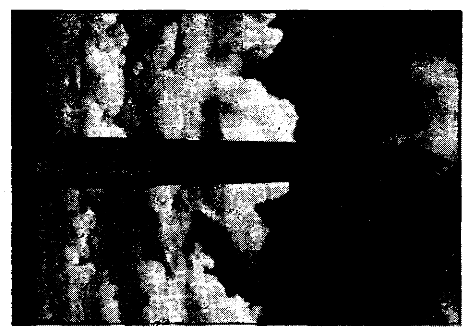


National Gallery of Art

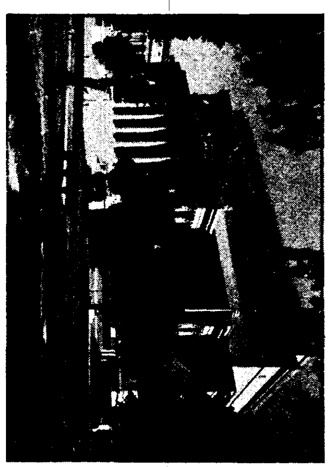
Smithsonian Institution

Capitol Hill

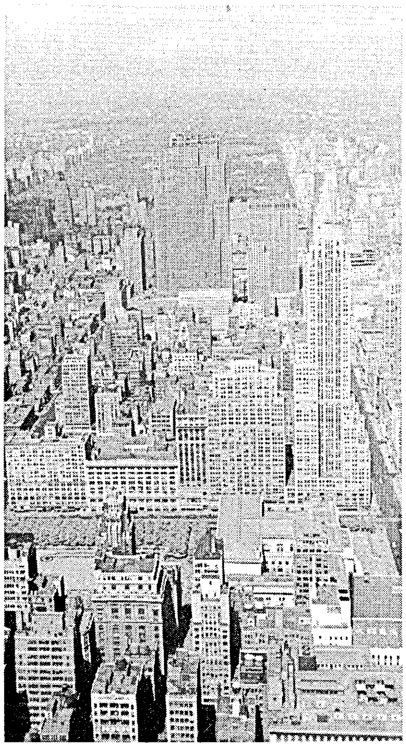




Washington Monument

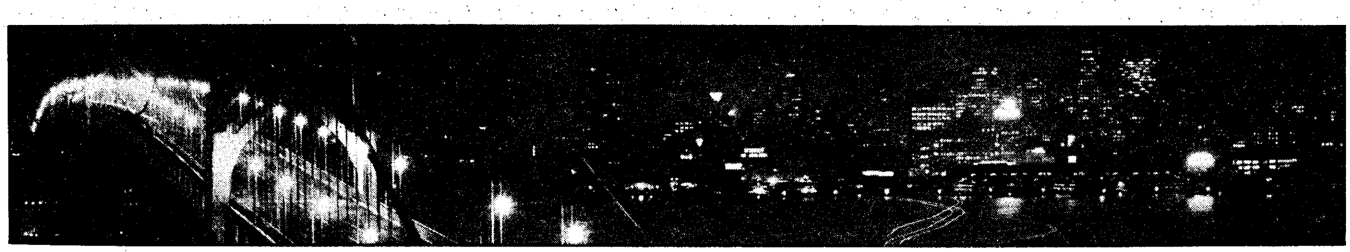


National Archives



THE '64 FALL JOINT

Volume 26 of the AFIPS Conference Proceedings, carrying the technical papers delivered at the '64 Fall Joint Computer Conference, will be datelined San Francisco. The conference will be held Oct. 27-29 at the San Francisco Civic Center. General chairman is Richard I. Tanaka of the Lockheed Missiles & Space Co., and program chairman is David R. Brown of the Stanford Research Institute. Deadline for papers is May 1.

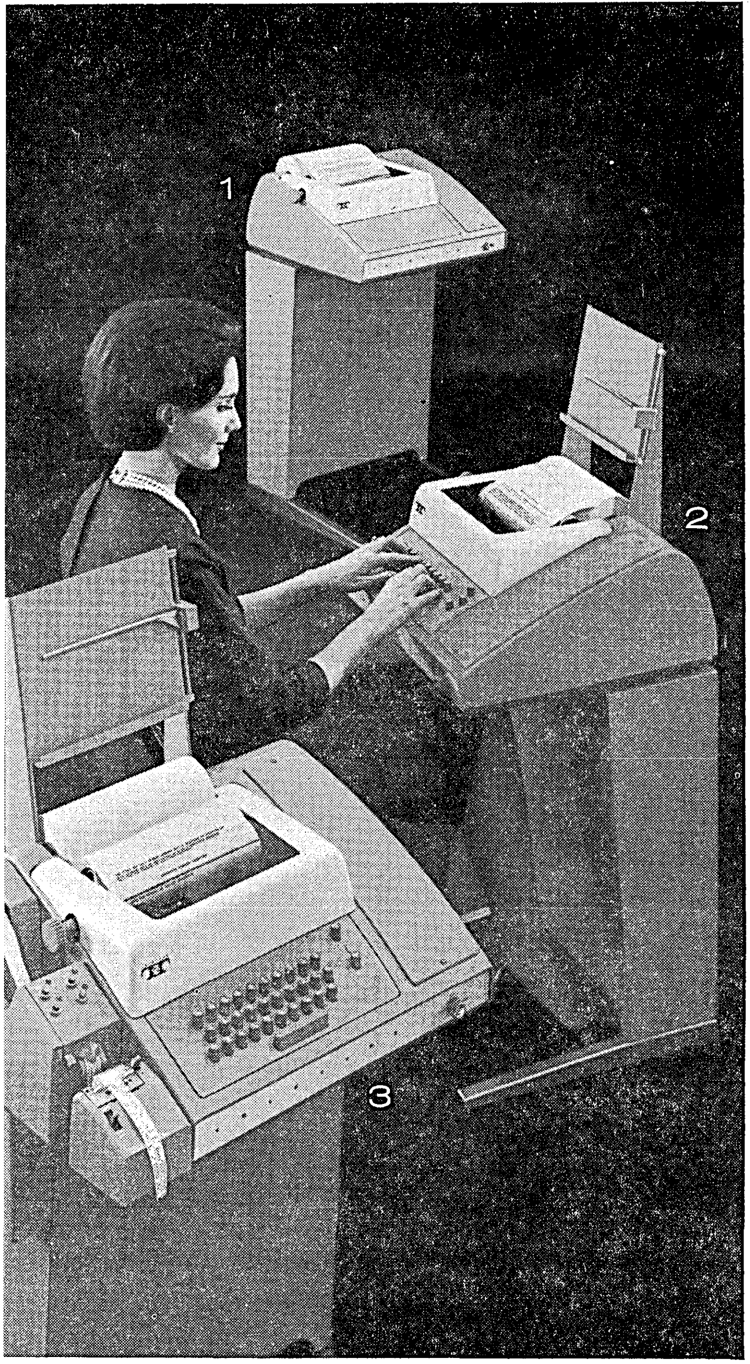


IFIP '65 CONGRESS

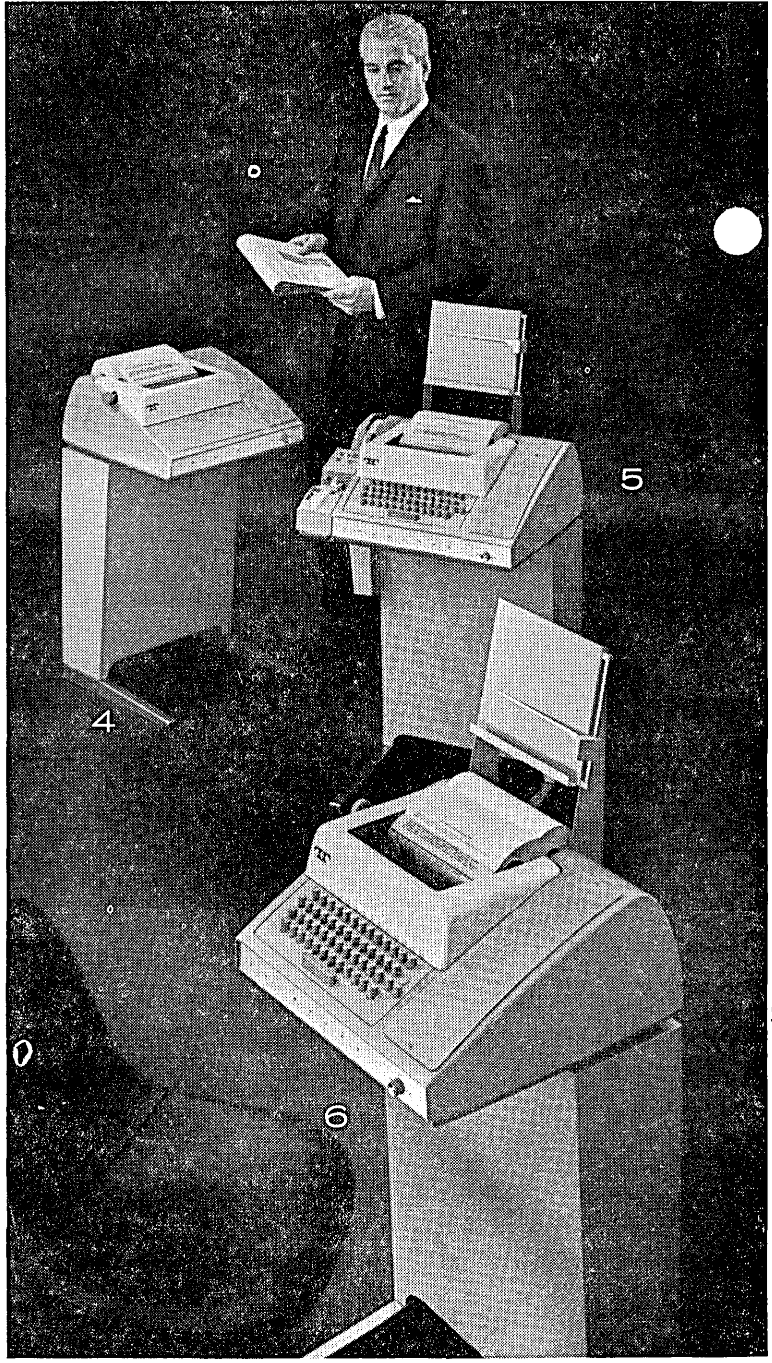
With the convening in the United States of the IFIP Congress 65, the 1965 Spring Joint Computer Conference will not be held. Instead, AFIPS will devote its time to participation in the trienniel, international conference which runs from May 24-29, 1965, at the New York Hilton. It is scheduled to be the largest international conference in information processing.

IFIP (International Federation for Information Processing) is an organization of technical and professional information processing societies in 23 nations, one of which is AFIPS (the American Federation of Information Processing Societies). AFIPS, in turn consists of the Association for Computing Machinery (ACM), the Institute of Electrical and Electronics Engineers (IEEE), and Simulation Councils Inc. (SCI). The president of IFIP is Isaac L. Auerbach of the United States.

The call for papers for this conference, which sets a deadline of Sept. 1, 1964, is an elaborate set of rules; thus, rather than to duplicate it here, interested candidates are asked to write to IFIP Congress 65, 345 East 47th St. (at UN Plaza), New York 17, New York. Exhibits will also form a part of the conference.



MODEL 32 SERIES. This new low-cost series operates at 100 wpm. Has a 3-row keyboard with a 5-level code. Shown above: (1) RO Receive-Only Set. (2) KSR Send-Receive Set. (3) ASR Automatic Send-Receive Set.

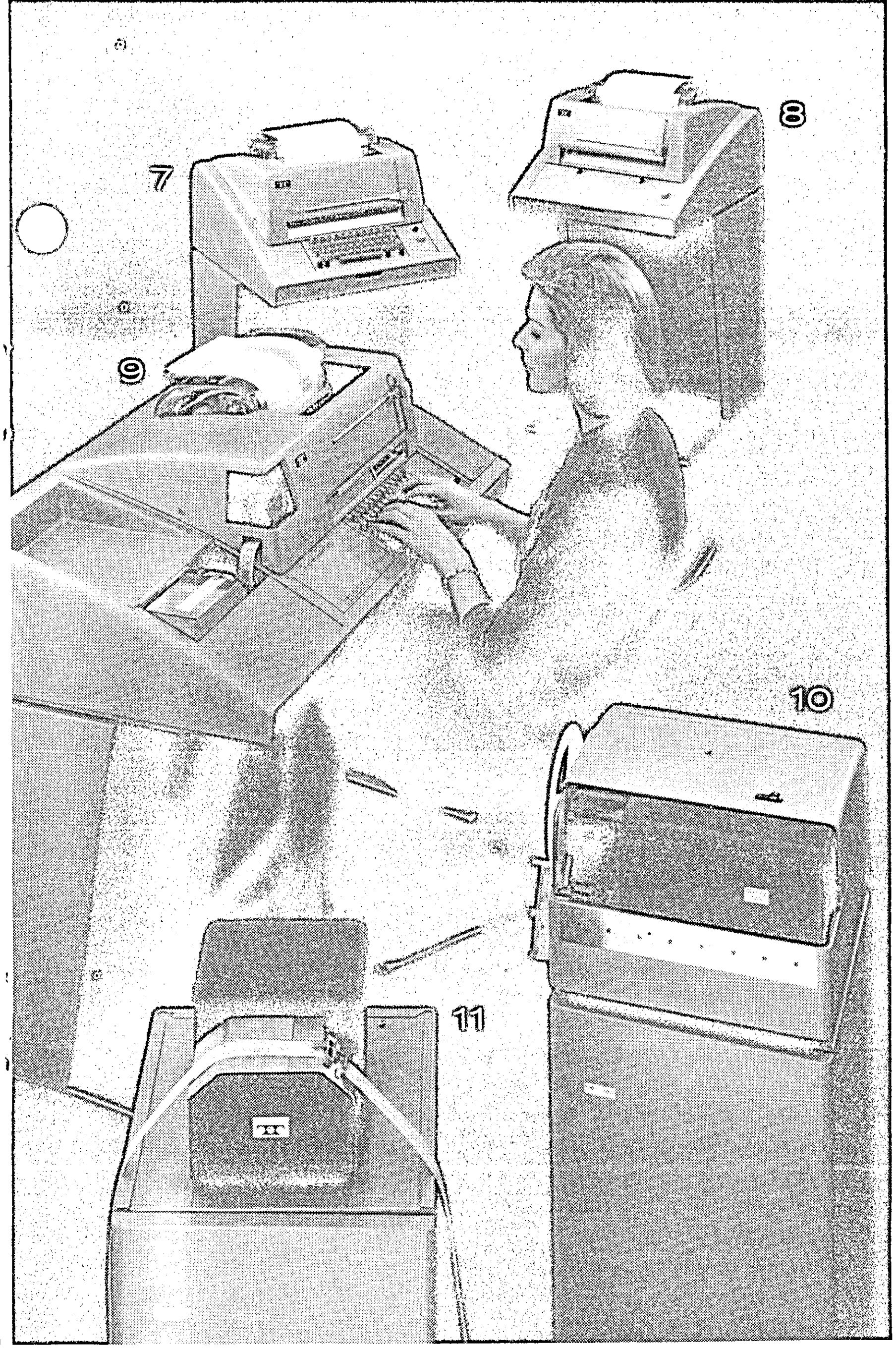


MODEL 33 SERIES. This economical series has a new 4-row keyboard and operates at 100 wpm with an 8-level, 11-unit code. Shown above: (4) RO Receive-Only Set. (5) ASR Automatic Send-Receive Set. (6) KSR Send-Receive Set.

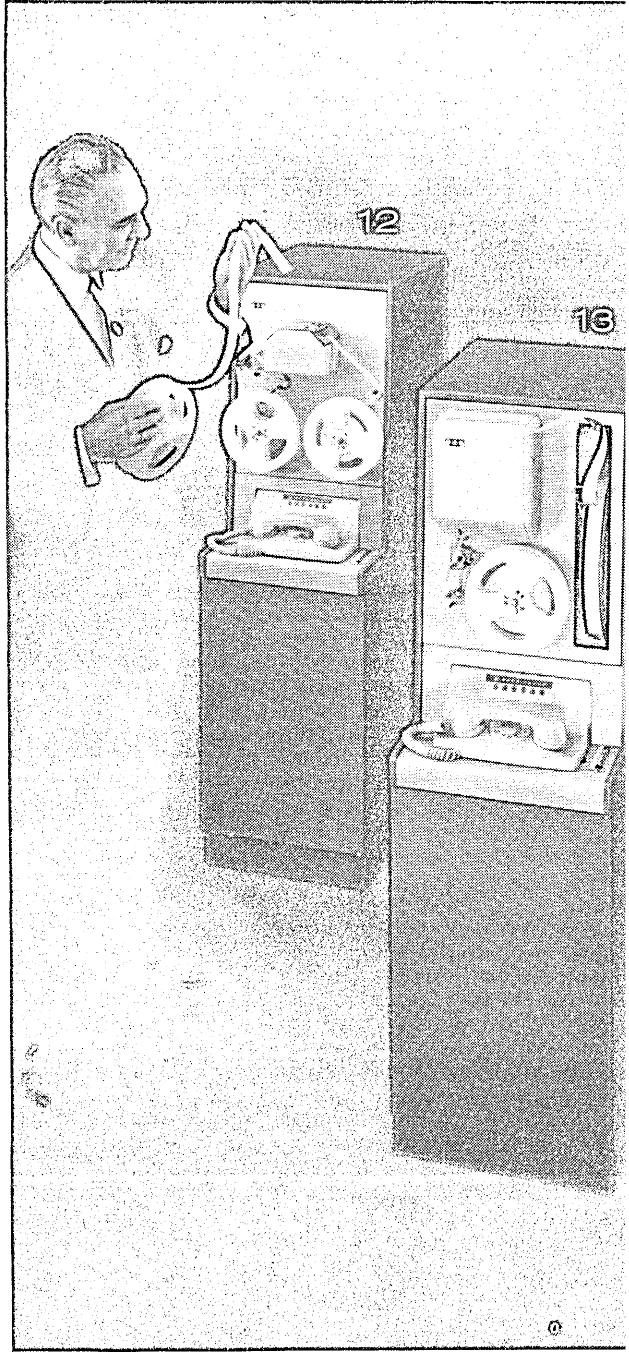
RELIABILITY COSTS LESS THAN

In telephone and telegraph systems throughout the world, Teletype equipment has earned an outstanding reputation for rugged, low-cost reliability. You can take advantage of this same equipment—this same reliability—in your own data communications systems. And the cost is surprisingly low.

The new Teletype Model 33 and 35 series are made for the Bell System and others for operation on 8-level, 11-unit code. Both series can be used for direct communication with data processing equipment. This opens up many possibilities for their use with your systems—both on-line and off-line. The Model 33 and 35 series



MODEL 35 SERIES. A rugged, heavy-duty line that has a new 4-row keyboard and operates at 100 wpm with an 8-level, 11-unit code. Shown above: (7) KSR Send-Receive Set. (8) RO Receive-Only Set. (9) ASR Automatic Send-Receive Set. (10) Self-Contained Tape Punch. (11) Self-Contained Tape Reader.



HIGH-SPEED TAPE-TO-TAPE EQUIPMENT. Used with DATA-PHONE and other communication services over voice circuits, this equipment is capable of 1,050 wpm tape-to-tape transmission. Shown above: (12) Sending Set. (13) Receiving Set.

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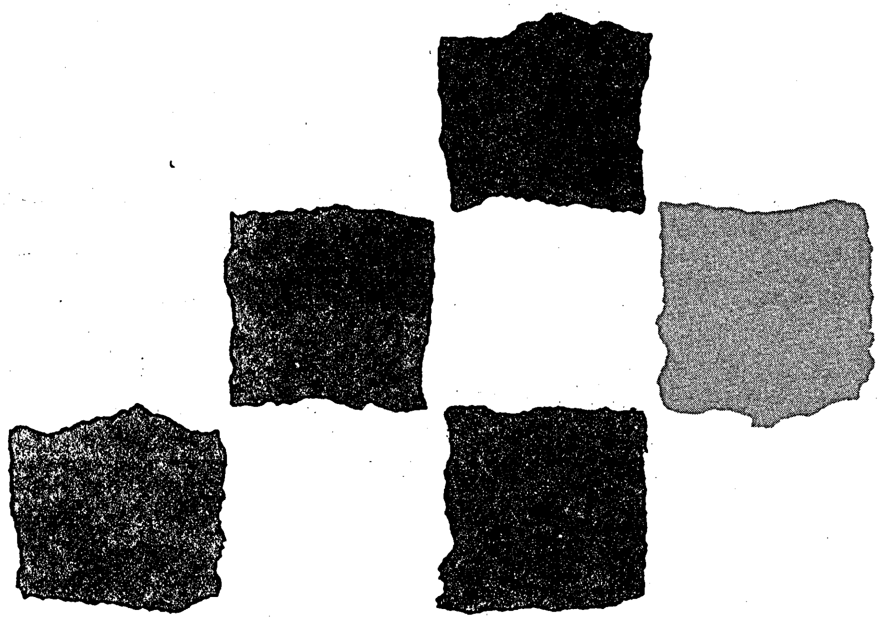


COMPUTER EDUCATION FOR THE BLIND

A special session on "Computer Education for the Blind" will feature a 17-year-old blind programmer. Michael Lichstein, a high school senior and programmer at the Univ. of Cincinnati, will report on the specialized programs he designed that make feasible computer work for the qualified blind. Using the techniques, a blind programmer reportedly can function as effectively and independently as a sighted individual.

The session will convene in Sheraton Hall on Wednesday at 11:30 a.m. All other conference activity, including the computer science theater, will adjourn to permit conference delegates to attend this session. It will be chaired by George G. Heller, national education chairman of the ACM.

The association's national education program for the blind will be presented by Dr. Theodor D. Sterling, director of the computing center, Univ. of Cincinnati Medical School, and chairman of the ACM subcommittee on Computer Education for the Blind. Accomplishments include programs for the IBM 1401 and 7040 that produce braille on the 1403, a 1401 manual in braille, and other teaching aids produced at the university—published in a booklet, "Computer Work for the Blind."

In a special evening session on Wednesday, Dr. Sterling will head a panel discussion on the aspects and problems of training competent blind people to become computer programmers.

THE TECHNICAL PROGRAM

by JACK ROSEMAN

The computer age is at the door step of maturity. In the past 20 years we have witnessed the evolution of the electronic computer from a relatively primitive counting device into its present state as a highly compact, integrated and efficient machine for science and business. The years immediately ahead will undoubtedly reveal many more new uses and unsuspected potentialities of the computer—one of the most challenging creations developed by the mind of man.

The 1964 Spring Joint Computer Conference occurs at an important mid-point in our history. We are as close in time to 1944, the year of the first computer, as we are to that ominous date, 1984. What will materialize? Will the computer be an instrument of man's oppression, as predicted by some, or his liberation, as hoped by many?

The program of the 1964 SJCC indicates our growing awareness of the overall implications of our new computer technology. Communications with the non-computer world have become one of the most important of our responsibilities. No longer do we encapsulate ourselves in a private world. What we work upon, write upon, and talk upon today in the computer industry has an effect that is felt in the farthest corners of the globe. Thus, the theme of this conference—Problem Solving in a Changing World.

The problem of internal communications must also be reckoned with. The industry's commitment to specialization increases as technical and professional people focus their efforts more and more on segments of computing technology. To help relieve this situation, technical sessions at the conference will feature expository papers on fundamentals for those who wish to experience a meaningful exposure to other disciplines than their own. In line with this thinking, there will be more opportunity at each of these sessions for panel discussions, for audience participation and evening informal discussions.

Our communications efforts have been greatly augmented by the proliferation of films dealing with computer topics. Whereas technical papers attract by their nature only limited audiences, most everyone can enjoy and derive value from technical movies properly produced and edited. The theater presentations at the conference should prove one of its more noteworthy features.

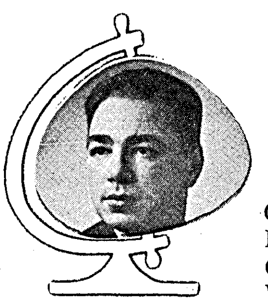
The growing accent on external communications does not mean that we have stinted on the screening and selection effort devoted to technical papers. The program committee and session chairmen have taken great pains to assure the high quality and usefulness of all the papers in the program, as a glance at the conference program indicates. To stimulate an even greater level of quality, AFIPS will present an award of $500 to the paper judged to be most significant from a technical point of view and which has been well presented.

In keeping with the computer industry's growing sense of public responsibility, we have also scheduled both papers and a panel session on the social implications of the new technology and how we can best assist in the utilization of these machines and techniques for the betterment of man. A special educational program for high school counselors is also being planned.

It can no longer be said that we should prepare for a new era. We are already entering that era. The problems of this age are to a large degree created by the technology with which we live. This computer conference affords the opportunity for a few days to stop, look and listen, to take stock, and to ponder the direction in which we are going.

THE SESSION HIGHLIGHTS

APPLICATIONS



Chairman:
DR. JACK MOSHMAN
C-E-I-R Inc.
Washington, D.C.

This session is devoted to illustrating by example some of the applications to which computers are being put. The papers which are being presented, over and above their intrinsic merit as scientific contributions, have been selected to show the diversity of application, making use of some of the more recent developments in the computer sciences.

Two papers are drawn from the behavioral sciences. Gullahorn and Gullahorn describe HOMUNCULUS, a program in the IPL-V language which is used in more than a passive, descriptive mode. The authors demonstrate how the computer can serve in the development of theory itself and in the generation of the logical consequences of certain assumptions which can lead to extensions or modifications of the initial theory.

Meeker, Shure and Moore also go beyond the more common use of the computer for solving or simulating analytical models or for analyzing empirical data. In studying the effects of threats on bargaining behavior, the computer is used to acquire basic information through real-time data processing. The point is made, and illustrated, that useful data may be gathered through computer-administered experimentation; no other experimental means exists to provide similar information.

Molecular biology is another field in which the computing sciences are exploited in a unique way. A model of the cell is proposed that uses string-processing finite automata. The tuning quintuplet notation is employed in a compiler to study the relationships among automata. The algorithmic system, as described, qualitatively simulates the basic biological processes including differentiation, induction or repression of coordinated growth, environmental adaption, cancer development and virus action.

In another area, Coyle and Stewart describe a real-time programming system used to analyze and control the NASA Orbiting Geophysical Observatory series of satellites. The system, operating on telemetered data transmitted from tracking stations, monitors the status of the spacecraft and analyzes data from as many as 50 scientific spaceborne experiments. The analysis may be triggered by a signal from one of the special-purpose consoles without interfering with the continuous real-time processing and without losing the telemetry data.

The generation of computer results in graphical form and recorded on film is not an unusual technique. Knowlton goes this several steps further in describing a technique for producing animated movies by computer. Hardly competitive with Walt Disney, the results may be used to illustrate psychophysical experiments, and for other educational purposes.

At the conclusion of presentation of the prepared papers, a panel will discuss other existing or anticipated applications in various fields. Emphasis will be placed on those areas or types of employment which are uncommon in the light of today's typical installations and problems.

A Computer Technique for Producing Animated Movies
KENNETH C. KNOWLTON
Bell Telephone Laboratories, Murray Hill, N.J.

Simulation of Biological Cells by Systems Composed of String-Processing Finite Automata
WALTER R. STAHL, ROBERT W. COFFIN, HARRY E. GOHEEN
Oregon Regional Primate Research Center, Beavertown, Ore.

Computer Simulation of Human Interaction in Small Groups
JOHN T. GULLAHORN, JEANNE E. GULLAHORN
Michigan State Univ., East Lansing, Mich.

Real-Time Computer Studies of Bargaining Behavior: The Effects of Threat Under Bargaining
ROBERT J. MEEKER, GERALD H. SHURE, WILLIAM H. MOORE JR.
System Development Corp., Santa Monica, Calif.

Real-Time Quick-Look Analysis for the OGO Satellites
R. J. COYLE, J. K. STEWART
Datatrol Corp., Silver Spring, Md.

I consider this session of the 1964 Spring Joint Computer Conference to be very important. Not just important among the other sessions scheduled at this conference, but important in the time scale of the history of computing—in particular, the history of *software*. For several years we have heard the statement that software programming has reached a plateau; it will take something radically new to start us moving again. Now, however, one can feel stirrings, here and there a striking out in a new direction —new ways of organizing hardware and software complexes, new ways of applying both new and old ideas to the automation of software itself, and new ways to communicate between men and/or machines.

How is a newcomer to the field to appreciate these developments? How does one impart to a novice not only the excitement of pushing ahead so fast in so few years, but also the sober judgment so necessary to avoid repeating old mistakes? Everyone who is really involved has been far too busy to take time out to document this important era in computing history. But someone *must* document it before its lessons and accomplishments slip away. We have been down some of these paths before!

Compilers came into their own many years ago—maybe six or seven! Each translator was carefully coded into thousands of instructions; each was a work of art. Occasionally a translator was written in the language it was designed to translate, but this didn't teach us much about the real problem of translation. The fundamental problem of compiler-writing is a special case of the problem which will have to be faced whenever a problem-oriented language comes into being: Given a class of problems which are similar, and which we believe to have some common underlying structure, how do we discover—and how do we represent—that structure? How do we arrange to exploit that common structure creating an algorithm for solving the entire class of problems? More specifically, we need an algorithm which can become specific to a particular problem when the parameters describing the problem are supplied. In terms of compilers, the problem becomes: How does one create a compiler generator which can accept as its parameters the description of the language and of the target computer, and which will produce (or become) a "good" translator for that language to that target computer?

One approach to the solution of this fundamental problem for compilers is the program that writes programs. We sometimes see this in report generators, for example, where a program is produced which is specific to the report desired. Now we must look to an apparently more difficult class of problems, viz., compilers for languages. Procedure-oriented languages, problem-oriented languages, algebraic languages, business-oriented languages, string-manipulation languages, and many others. We need a way to specify the language and generate that translator. It sounds hard, but progress is being made. One of the very important byproducts of the ALGOL effort has been the focusing of attention on ways of describing languages in formal, syntactical notation (such as the "Backus normal form"), and on ways of using such descriptions as the basis for translation strategies.

This session has two goals, then. The first is handled by the historical paper of S. Rosen, which gives an account of the growth of executive systems and the translators that are imbedded in them. In particular, the bibliography provided here should be able to start anyone off in the right direction in finding material on many of the early developments. The other goal of this session is an introduction to some of the latest methods being used in the search for "compiler-generators." The paper by T. Cheatham Jr. and K. Sattley surveys the different approaches which use syntax-directed techniques, explaining how they work and why. Finally, the S. Warshall and R. Shapiro paper describes some new developments along these lines; in fact, a particular method for generating compilers!

TUTORIAL

Programming Systems and Languages: A Historical Survey
SAUL ROSEN
Purdue University, Lafayette, Ind.

Bounded Context Translation
ROBERT M. GRAHAM
MIT Computation Center, Cambridge, Mass.

Syntax-Directed Compiling
T. E. CHEATHAM JR., KIRK SATTLEY
Computer Associates Inc., Wakefield, Mass.

TECHNICAL

A General-Purpose Table-Driven Compiler
STEPHEN WARSHALL, ROBERT M. SHAPIRO
Computer Associates Inc., Wakefield, Mass.

The new technology of automation is increasingly being cast in the role of villain. Spokesmen from labor, government, business, civil rights, and other interest groups engage in spirited oratory on its pros and cons. It is perhaps unfortunately true that when automation is mentioned, Everyman ordinarily thinks of computers and rarely of industrialization and mechanization, including the major portion of industrial process control, none of which has anything to do with computers. The computer is simply too good a symbol to overlook, and is punished out of all proportion to its crimes.

No spokesman in the forum of automation has yet emerged from the technical sector of the information processing community, the sector committed to increasing the sophistication and application of computers. Representatives from this sector should be encouraged to participate in these forums so that the public will be better able to distinguish between those aspects of automation resulting from the use of computers and those caused by industrialization and mechanization.

Additionally, it seems more than prudent—even necessary—for the information processing community to examine the rationale for its existence. As a prerequisite to this examination we must know what the real social implications of information processing are. We may have been guilty of suboptimization: overselling the long-term social dislocations which it brings in its wake. Is information processing a villain? What are the effects of information processing on labor, education, law? How much of automation involves the use of computers, and what are the social implications which can fairly be associated with their use? It is the objective of this session to provoke dialogue on the points mentioned above.

Papers to be presented at the session all agree that the social impact of automation is measurable and growing. This is demonstrated by unemployment statistics. More fundamentally, the question of alternative uses of man's time is discussed, and it is found that no established acceptable substitute for employment exists for the bulk of the U.S. population. Alice Hilton proposes that acceptable substitutes can be created by a process of reeducation concentrating on the young. R. H. Davis cites statistics and trends in the opposing direction. Not only are many of today's unemployed not retrainable, but a disturbing proportion of today's youth is not receiving the minimum educational experience to prepare them for tomorrow's world. They are untrained as well as unretrainable. H. E. Striner proposes that the power of information processing be applied in treatment of the ills of automation by improving the scope and timeliness of matching the jobless with job openings throughout the country.

In the panel discussion following the presentation of papers, social implications will be raised which are not contained in the papers. For example, organizational and political implications are not highlighted, yet increasing centralization of power is a very real phenomenon associated with information processing. Safeguards to assure control of computer-accessible information must be devised to preserve personal privacy, and avoid compromise of corporate trade secrets and government classified information. This would appear to have substantial implications to our juridical and law enforcement systems.

It is clear that this single session will not serve as a definitive or even comprehensive examination of the rationale for information processing. We hope, however, that this session will be the first in a continuing program within the technical sector of the information processing community to deal with these more far-reaching issues.

An Ethos for the Age of Cyberculture
Alice Mary Hilton
A. M. Hilton and Assoc., New York, N.Y.

Information Processing and Some Implications for More Rational Economic Activities
Herbert E. Striner
W. E. Upjohn Institute for Employment Research, Washington, D.C.

The Computer Revolution and the Spirit of Man
Robert H. Davis
System Development Corp., Falls Church, Va.

COMMAND AND CONTROL

Chairman:
Dr. Ruth Davis
Office of the Director of Defense Research and Engineering, Washington, D.C.

The subject matter of command and control is interdisciplinary. It runs the gamut from the design of military strategy to the development of an individual computer program for use by a particular military staff. Topics which fall within this spectrum include means of organization of military commands and staffs to accomplish assigned missions, design of communication systems to allow the prosecution of command and control functions, design, development and implementation of automated information handling systems within military organizations, determination of cost-effectiveness for command and control systems and research and development in support of improved command and control.

It is interesting to reminisce that it was just seven years ago that the first tentative probes were being made to determine both what this subject matter consisted of and what the attendant problems were. The answers were not immediately forthcoming, and the question can still rightfully be posed as to whether we have yet properly defined command and control. Certainly, however, the faults of command and control have been hunted out with great diligence. They include inadequate amounts of information on which to base decisions, unaccessibility to information by decision makers, too slow response times to occurring actions, non-standardized reporting systems, non-survivability of command facilities and of communications, and so on. The solutions have been forthcoming over this seven-year period as a set of now-flourishing offspring. Computer systems have been born, information processing sciences have appeared, automated decision making has been suggested and standardization is preached, but rarely practiced. Many people were hired to correct the deficiencies of the military command and control processes by employing a myriad of practices.

Command and control has during this seven-year period become a household phrase. It has permeated every fiber of military, professional and business society. Can we now evaluate our first solutions to the initial problems or have we instead removed the real problem out of focus and begun to concentrate on solving the problems raised by our "solutions" themselves? We will find no agreed-upon position here. The question is essentially unanswerable as long as no proof exists that we ever understood the real problem initially. There are enough dissidents now, however, to raise a hope that understanding of the real problem is close. These dissidents are those who do grasp the fact that as the problem becomes more difficult of quantitative solution the need for talented leadership becomes more acute than the need for increased machinery. These dissidents are those who realize that processing of information is no substitute for lack of relevant information, that automated display of information is no substitute for trained, effectively supported commanders, and that survivability of command facilities is useless if decision-making has been relegated to only a few. These dissidents are becoming more vociferous.

The papers being presented at the command and control symposium give proof both of our better understanding of the subject and of the wide range of subject matter. One of the speakers who has been involved in command and control for its entire lifetime of seven years puts forth the premise that our huge, inflexible command control systems are actually contributing to the inconsistencies they are supposedly resolving. Even worse, they are contributing to an impending catastrophe within the Department of Defense. Another speaker with extensive experience in managing programming system design projects makes some astute observations concerning the development of such programmed systems. He points out the folly of aiming at too ambitious a goal rather than proceeding towards realizable intermediate goals. Another speaker discusses cost-effectiveness of command and control systems in a meaningful context by isolating the pertinent predominant factors. He makes a plea for a responsible attitude on the part of those contributing to solution of command and control problems, and asks that equipment and software only be recommended if it indeed will be worth the cost to the user. The fourth set of speakers discusses the costing of large programming systems. They point out little appreciated facts that must be taken into account by those responsible for such systems, and collect experientially derived data so that they can be used as planning guides. Each of the papers presented will be subjected to a critical review by a second expert in each field to invite comment by the audience.

On the Evaluation of the Cost-Effectiveness of Command and Control Systems
N. P. Edwards
Weapons Systems Evaluation Group, Washington, D.C.

Fractionization of the Military Context
Frederick B. Thompson
Tempo, General Electric Co., Santa Barbara, Calif.

Some Problems Associated with Large Programming Efforts
Almon E. Daniels
Institute for Defense Analyses, Washington, D.C.

Some Cost Contributors to Large-Scale Programs
Burt Nanus, Leonard Farr
System Development Corp., Santa Monica, Calif.

NUMERICAL ANALYSIS

Chairman:
Dr. R. W. Hamming
Bell Telephone Laboratories
Murray Hill, New Jersey

When compared to most areas of activity in computing, Numerical Analysis is old and hence rather stable. In many processes we are probably well within an order of magnitude of the ultimate efficiency. Thus from Information Theory principles the sampling rates for differential equations require at least two samples per the highest frequency present under the ideal conditions that the samples are known from plus to minus infinity, while current practice uses around ten samples taken from one side only.

In spite of this lack of glamour, Numerical Analysis still plays a vital role in many applications and much remains to be done. The papers of this session show that the field is still active. In particular, the field of finding appropriate ways to set up the differential, or the difference, equations for many situations, especially simulations of dynamical systems, is under active development.

Another area of constant evolution, and in this case one that apparently can be developed much farther, is the area of searching for maxima and minima, sometimes in situations involving the solution of dynamical systems.

After the formal presentation the panel will presumably comment on the papers and their general opinions of the field.

New Difference Equation Techniques for Solving Non-Linear Differential Equations
James M. Hurt
IBM Corp., Kingston, N.Y.

Discontinuous System Variables in the Optimum Control of Second Order Oscillatory Systems with Zeros
William Nevius, Harold Titus
U.S. Navy Postgraduate School, Monterey, Calif.

Two New Direct Minimum Search Procedures for Functions of Several Variables
Bruno Witte
General Dynamics /Astronautics, San Diego, Calif.

EVALUATING COMPUTER SYSTEMS

Chairman:
Jack D. Porter
MITRE Corp.
Bedford, Massachusetts

Computer users have long been faced with the problem of evaluating and selecting edp equipment to match their system requirements. Many methods have been used and a number of papers have appeared in the literature. This session will discuss various techniques with an indication of their applicability and limitations.

Three papers have been selected for formal presentation in this session. The first will describe a complete dp equipment acquisition package including the preparation of system specifications, formats for the proposals to be submitted by the vendors, instructions for the validation of the proposals, and instructions for scoring the proposals. The scoring technique makes use of standardized factors, weights, and formulas. The second paper will describe a cost-value method that attempts to assign dollar values to selected factors. This technique aims at providing the evaluation team with a more natural and simpler basis for comparing the factors involved in the selection. The third paper will describe a computer simulation program called SCERT (Systems and Computers Evaluation and Review Technique) that produces a set of detailed management reports from definitions of the data processing problem and the hardware and software performance factors of the computer configurations being considered. The reports furnish the user with projections of cost, time, memory, and manpower requirements involved in applying the particular computer to his problem.

The session should not be expected to produce any "pat" methods since none exists. Instead it should provide some stimulating and useful ideas, based on the extensive experience of the speakers and panelists, that will materially assist in a particular selection process. We have been very fortunate in enlisting as panelists individuals of experience and responsibility in both government and industry.

Analytical Technique for Automatic Data Processing Equipment Acquisition
SOLOMON ROSENTHAL
Headquarters, USAF, Washington, D.C.

Cost-Value Technique for Evaluation of Computer System Proposals
EDWARD O. JOSLIN
Framingham, Mass.

The Use of a Computer to Evaluate Computers
DONALD J. HERMAN
Comress Inc., Washington, D.C.

The Analog-Hybrid Computer Tutorial session was planned in order to furnish basic information on the present state of these fields of endeavor for those who are active in other fields. It appears to be difficult to obtain tutorial papers for a conference, on any subject; hence this session is limited to one presentation on the subject of hybrid computer simulation.

Hybrid computation came into being, as early as 1958, as a means of simulating the complete mission of certain aerospace vehicles. The task required computational speed exceeding the capabilities of the largest digital computers and a precision beyond that of the best analog computers. Combined systems of large general purpose analog and digital computers were created to solve this type of problem. The experience of these efforts and other experiments with analog and digital techniques in recent years have led to a growing hybrid computer technology. It is considered that these are the formative years in the evolution of a type of computer simulation in which the differences between analog and digital computing technique will dissolve through the development of general purpose scientific simulator systems.

In this session the elements of present day hybrid simulators are discussed; their incompatibilities and limitations are examined. The relationship of the computer system to the simulation problem is analyzed. The application domains in which hybrid computation is and is not appropriate are discussed.

The primary points developed in this paper are, that: (1) there is an ever-growing need for simulation of very complex engineering systems. The process of analysis and building of a computer model for evaluation and prediction of behavior are a required step in many large development programs. The hybrid computer offers a means for many such simulations that would be impractical by other means. Hybrid computation is inherently a tool for very complex simulations rather than simple studies. (2) A hybrid computer is a compatible system of *parallel* computing components, both digital and analog, and a stored program *sequential* machine. The hybrid programmer must be constantly aware at the relative timing of computational events in the *parallel* and *sequential* parts of the system. (3) Hybrid computation is built upon the technology of analog and digital computers and is equally dependent upon the programming methods, software, and procedures of problem analysis that have been developed for each.

Hybrid Computation...What is it?....Who Needs it?
THOMAS D. TRUITT
Electronic Associates Inc., Princeton, N.J.

Recent advances in analog switching techniques and the addition of logic elements and analog memory give the modern analog computer the capability of solving more types of problems. For years the analog computer has been one of the prime means for solving problems expressed in terms of differential equations; now the analog computer has greater flexibility as a mathematical tool.

Hybrid computers are taking advantage of the new capabilities of analog computers and digital differential analyzers. A hybrid computing system solves problems by combining parallel and serial computer techniques. Hybrid computers are tackling problems that are too big, too long, or too fast to be economically solved on a general purpose digital computer or require too great a dynamic range, or too much memory to be solved on an analog computer or digital differential analyzer.

The three papers in this session are all contributed by people who are working on the ASTRAC II (Arizona Statistical Transistorized Repetitive Analog Computers) at the University of Arizona under the direction of Prof. G. A. Korn. All of the papers deal with the development of digital hardware and digital techniques as both an adjunct to and an integrated part of, a modern high speed iterative analog computer. It is refreshing to note the resurgence of university leadership in the fields of research and development as applied to modern computing equipment.

The paper by Baker A. Mitchell, Jr., deals with the implementation of a hybrid analog-digital iterative differential analyzer for system optimization by parameter perturbation using a n-dimensional random walk as the perturbation scheme. The flexibility of the design allows simultaneous optimization of n parameters by a number of variations on the basic random flight; e.g., pure random walk, random walk with reflecting walls and absorbing barriers, and correlated or biased random walk. The logic can be expanded to accommodate higher order Markov processes with various correlation strategies over successive moves.

All of the schemes mentioned above can be implemented with simplicity, reliability and low cost as a result of a unique method of parameter setting which is described in detail.

Handler reports on a delta-sigma modulation system for time delay and analog function storage. Modified delta modulation (delta sigma modulation) permits magnetostrictive delay line function storage of analog data with the significant advantages of pulse regeneration with clock gated logic and relatively inexpensive conversion equipment. Five to 10 msec delay lines with a 2 mc bit-rate accommodate analog signals of up to 8 kc with phase shift below 2 degrees; total dynamic error is within 0.2% of half scale up to 1 kc. An adaptive filter permits a further trade off of accuracy for bandwidth during computation. This paper describes the design of the delta-sigma modulation system and presents test results.

In his paper, Hampton describes the design of a hybrid analog-digital pseudo-random noise generator intended to replace conventional random-noise generators in analog and hybrid computer simulations. It is capable of producing four essentially uncorrelated binary outputs from a single 25-stage shift-register. The length of the pseudo-random output sequence is 33, 554, 431 bits which is equivalent to several computer runs.

This hybrid noise generator has several striking features not generally shared by existing analog noise sources:

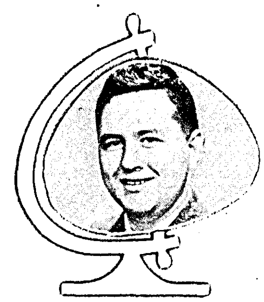
1. The analog noise output is independent of any physical quantity except for the output clamping levels. In particular, the relative amplitude distribution and spectrum are practically unaffected by environmental changes, such as temperature fluctuations.
2. The shift-register may be reset at any time to repeat a sequence of random events exactly, or it may run free.
3. The binary noise bandwidth is simply proportional to the shift-register clock rate (between zero and 4 Mc). This permits exact time scale changes or intermittent operation.
4. The flat spectrum binary noise permits multiplication for correlation experiments by simple analog switching and yields Gaussian noise with any reasonable spectrum by filtering; diode function generators can then be used to produce different amplitude distributions.
5. The noise generator produces binomially distributed digital computer random numbers as well as analog noise.

A Hybrid Analog-Digital Parameter Optimizer for ASTRAC II
BAKER A. MITCHELL JR.
Univ. of Arizona

A 2 mc Bit-Rate Delta-Sigma Modulation System for Analog Function Storage
H. HANDLER
Univ. of Arizona

A Hybrid Analog-Digital Pseudo-Random Noise Generator
R. L. T. HAMPTON
Univ. of Arizona

ARTIFICIAL INTELLIGENCE



Chairman:
DR. H. L. GELERNTER
IBM Research Center
Yorktown Heights, New York

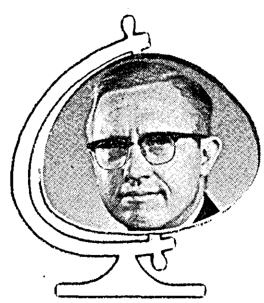
Progress in the area of Artificial Intelligence has been something less than spectacular. Indeed, many of us who had the temerity to predict the course of evolution of this new discipline are likely to be mildly embarassed on reviewing some of our earlier writings. Nevertheless, progress *is* being made in the effort to simulate intelligent behavior with machines, and here and there, awash in a sea of irrelevant, trivial, and sometimes mystical work represented as research in artificial intelligence, a legitimate, and occasionally even a significant achievement will float into view. Unfortunately, in the context of our present ignorance, it is difficult if not impossible to distinguish the significant from the merely legitimate. The papers in this session are at very least members of the latter catagory, and have the additional virture of reporting concrete and stimulating results, rather than announcing work planned or in progress.

A Computer-Simulated On-Line Learning Control System
J. DOUGLAS HILL, G. MCMURTRY, K. S. FU
Purdue Univ., Lafayette, Ind.

A Heuristic Program to Solve Geometric-Analogy Problems
THOMAS G. EVANS
Office of Aerospace Research, Bedford, Mass.

Experiments with a Theorem-Utilizing Program
LARRY E. TRAVIS
System Development Corp., Santa Monica, Calif.

MULTI-PROGRAMMING



Chairman:
DR. WALTER J. BAUER
Informatics, Inc.
Culver City, California

Professionals in the computer business have recently seen increasing use of such phrases as "implicit programming," "on-line programming," "time-sharing," "on-line program de-bugging" and "executive control of multi-computers." However, comprehensive reports on some of the advanced projects using these concepts have been lacking. This session provides a well-documented report on three projects of great importance to the computing field.

The use of computers by many users, simultaneously and remote from the computer, is one of the fastest growing technical areas. Along with this is the associated problem of executive control of systems where remote and simultaneous use is to be accomplished and where the coordinated control of many parts of the system must be accomplished as they simultaneously operate on the data. This is the subject matter of the Multi-Programming session.

The first three papers describe two projects using the time-sharing concept. Both employ large-scale computing systems of modern design. The general philosophy of these projects is to allow convenience of the user at an operating console at some expense of computer efficiencies and programming complexity. They exemplify the modern trend "to bring the programmer and the analyst back to the machine in establishing a total man/machine system which allows convenient user operation." In both of these projects the emphasis is on coordinated control of communication terminals, operating programs and de-bugging systems, under an executive program.

The other paper of the session deals with executive control with less emphasis on remote computer usage. The Univac paper discusses control of multiple modules of a system—a subject of growing importance. More specifically, it deals with a technique for priority control of multi-computer systems in a real time environment.

The first paper reports on the so-called "ARPA time-sharing project" of the System Development Corporation. This system utilizes the AN/FSQ-32 computer of 64,000 words of storage, a PDP-1 and an additional 16,000 words of buffer storage, for inter-computer communication and disc files. The PDP-1 handles the traffic to and from the remote locations. On-line programming and source language de-bugging can take place using time sharing versions of the IPL or JOVIAL languages. Teletype or consoles are employed for remote stations.

The IBM papers report on a project of potential commercial importance. The system is an IBM-7040 computer with disc file storage and a communications system to which are tied a number of IBM 1050 keyboard-printer terminals. This system allows on-line programming and source language de-bugging of FORTRAN statements. A conversational mode of communication between the operator and the machine is developed.

The fourth paper by Univac reports on an executive control program for a multi-computer system. The equipment involved are two USQ-20 computers of 32,000 words of storage tied into a wide variety of input/output equipments and instrumentation. The executive control philosophy developed recognizes the system's tasks in order of system priority, distributes them among the system's computers and controls them in the individual computers. An introspective feature of the control program allows a dynamic realignment of the input/output priorities. The advanced design of the input/output system of the computers is exploited.

The papers of this session are undoubtedly of significance in the computing world. They are the first reports on important large scale projects which have been under development for some time. The system capabilities are in a very advanced state of development. The papers certainly point the way in this new technical area; they deserve careful attention and scrutiny by all.

A General-Purpose Time-Sharing System
E. G. Coffman Jr., J. I. Schwartz, C. Weissman
System Development Corp., Santa Monica, Calif.

Remote Computing: An Experimental System
Part One: External Specifications

T. M. Dunn, J. H. Morrissey
IBM Corp., New York, N.Y.
Part Two: Internal Design

J. M. Keller, E. C. Strum, G. H. Yang
IBM Corp., New York, N.Y.

Multi-Computer Programming for a Large-Scale Real-Time Data Processing System

Gerald E. Pickering, Gordon A. Erickson, Ernest G. Mutschler
Univac, San Diego, Calif.

The title reflects the miscellaneous nature of this session. In it, four papers will be presented. Messrs. Santos, and Arango discuss a form of ternary logic using "Postian functions," and propose some techniques for implementing that logic. Their suggestions include the truth tables for some of the functions, as well as some circuit diagrams and block schematics. Although ternary arithmetic has not found a significant place in digital computer systems, it is refreshing to be reminded of its possibilities.

The paper by Rutman describes an algorithm for the placement of interconnected elements based on minimum word length. Quoting from the author's abstract: "This paper describes in detail a computer program which automatically performs the placement of the components so that the overall interconnection wire length tends to a minimum. The procedure uses integral linear programming, and consists of essentially two parts. The first part reduces the length of the longest wires, and the second reduces the total wire length. This process is shown to be more effective in decreasing total wire length than the usual one-step process. An example of a 500-element placement of circuits for a digital computer is included." This subject is becoming increasingly important as the newer fabrication techniques result in smaller components and denser assemblies.

The third paper, by Simmons, is a highly theoretical and mathematical study of a proposed memory which involves associative addressing and distributed storage. The first paragraph of the manuscript neatly states the reason for interest in "multiple response files" and "associative memories," as follows: "Memory techniques which have so far been developed with computer technology all share limitations imposed by the requirement that a memory address be specified uniquely for storage or retrieval of data. In many problems these addresses are merely 'dummy variables' with the only meaningful order being one derived from the content of the data points themselves; examples of such operations are sorting, interpolating and catalog look-up. Largely because of the astronomical proportions of the computing task assumed by some real (and reasonable) problems in these and other closely allied areas, there has been an increasing interest in the type of memory in which information is stored (and retrieved) on the basis of content."

Messrs. Younker, Heckler, Masher and Yarborough describe the small, experimental, reference-retrieval file which they designed for the Rome Air Development Center. The file is designed to store and search among 5,000 document indexes, each index consisting of an accession number and up to eight descriptors. The machine is based largely on "pattern wired" arrays of ferrite cores which make up the "associative" or "catalog" memories. The paper includes circuit schematics and photographs of the completed equipment.

If time allows, there will be a discussion at the end of the session, not only of the papers, but also of related topics and trends in equipment development. The speakers, three invited panelists, and the audience are expected to take part.

On the Analysis and Synthesis of Three-Valued Digital Systems

PROF. J. SANTOS, H. ARANGO
Universidad Nacional del Sur, Bahia Blanca (Bs. As.), Argentina

An Algorithm for Placement of Interconnected Elements Based on Minimum Wire Length

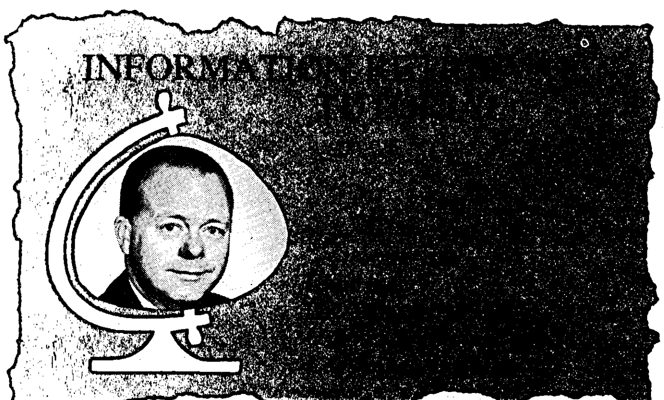
R. A. RUTMAN
AC Spark Plug Div., General Motors Corp., El Segundo, Calif.

Studies of an Associatively Addressed Distributed Memory

G. J. SIMMONS
Sandia Corp., Albuquerque, N.M.

Design of an Experimental Multiple Instantaneous Response File

E. L. YOUNKER, C. H. HECKLER JR., D. P. MASHER, J. M. YARBOROUGH
Computer Techniques Laboratory, Stanford Research Institute, Menlo Park, Calif.



The field of Information Retrieval is on the threshold of explosive growth. New potentials in computing hardware and the increasing burden of information retrieval problems are combining to heighten interest in the field. This session was planned to provide an introduction to the concepts and techniques of this rapidly developing area of interest. At the same time, a review of one of the most critical technical problems was judged appropriate. The first paper, by Harold Borko, will discuss the problems of automatic generation of classification systems.

In an information storage and retrieval system, classification provides a means for organizing a mass of material into groups so that related items are brought together in a systematic fashion. By grouping documents into categories, the number of items to be scanned in response to a search request can be reduced and the efficiency of the system increased. To design a classification system, one must specify the number of classes to be established and the principle to be used in determining class membership. A number of mathematical procedures for devising classification schedules are reviewed; these include factor analysis, clump theory, and latent class analysis. These and similar techniques can also be used to automatically classify documents into correct categories and thus speed up the processing of incoming materials. The initial results appear promising, and further research is being undertaken to determine the retrieval effectiveness of automated indexing and classification systems.

The second presentation, by G. N. Arnovick, J. A. Liles, and J. S. Wood, will be a comprehensive survey in which the state of the art of information storage and retrieval (IS&R) is outlined and presented in a form assimilable by those whose background is technical or, more specifically, oriented to computer hardware but whose knowledge of IS&R techniques and applications is at best limited. The presentation is, therefore, comprehensive but not discursive. On the generally accepted presumption that retrieval of information is as successful as its representation in the file, greater attention is focused on indexing. Some of the controversial issues and unsettled problems, such as the role of relationships and context of index terms, are critically examined. Potential solutions to these problems, including automatic input techniques and statistical approaches, are also discussed. Subsequent consideration is given to the problems of information dissemination, abstracting, storage, retrieval, display, reproduction, and communication links.

It is concluded as a result of the survey, in general agreement with other authors, that IS&R is not yet a well-defined discipline and that techniques of IS&R are lagging the tremendous potentialities of available hardware. A third conclusion is that a far stronger empirical data base is needed to realize effective overall system integration.

Research in Automatic Generation of Classification Systems
DR. HAROLD BORKO
System Development Corp., Santa Monica, Calif.

Information Storage and Retrieval: Analysis of the State of the Art
G. N. ARNOVICK, J. A. LILES, J. S. WOOD
North American Aviation Inc., Downey, Calif.

Much hope has been held for the potential of electronic computers for handling information retrieval problems. As time goes on, we are learning that the intellectual tasks involved in traditional solutions to information retrieval problems are complex to a degree that makes them unlikely to be adaptable for computer systems. New approaches to the way we handle information are going to be needed. Since the capabilities of computers do not match the capabilities of the human mind, it is reasonable to look for other means to solve problems on computers than those that are used in manual solutions. The papers in this session deal with novel ways of looking at information with computers. The knowledge gained from this type of approach is essential to achieving a total solution to the information problem.

The first paper, by M. E. Stevens and G. H. Urban, discusses a "training sequence" of a presumably representative sample of documents from a collection, previously indexed on the basis of human subject content analyses, which is processed by computer to provide *ad hoc* statistical associations between each of the descriptors manually assigned to the sample items and significant words occurring in the titles and texts of abstracts of these items. It is assumed, thereafter, that significant words in titles-and-cited-titles, only, of new items can provide efficient clues for computer assignment of appropriate "descriptors" to these new items. Results are reported for 101 machine tests on 59 different items run against two 100-item "teaching samples." These results are generally comparable to those reported for other assignment-indexing techniques carried out by computer, but the "SADSACT" method minimizes input text requirements. Future plans, including programming consideration, are briefly discussed.

Kuhns and Montgomery see the fundamental problems of an information system as (a) non-selection of pertinent material, (b) selection of non-pertinent material, (c) assimilation of selected material. (By assimilation is meant the incorporation of new material into an existing information processor). In a technical information system, it is supposed that many users will want output in order to verify hypotheses or answer questions, or form new hypotheses. The information correlation experiments presented in this paper suggest an approach to the assimilability problem for the second purpose, and were designed along the following lines:

Assuming that structured information is easier to assimilate than unstructured information, and consequently that degrees of assimilability correspond to degrees of structure, two different degrees of structure were developed for a set of sentence fragments. The structured data was then tested for assimilability by asking experimental participants to derive inferences from the fragment sets.

Results of these experiments are given in detail and a system for quantitative evaluation of inferences is discussed.

Salton and Sussenguth discuss the use of structure matching procedures in information retrieval systems. Many constructs of interest in data processing are conveniently represented in two dimensions by abstract graphs, consisting of sets of points (nodes) and interconnections (branches) between certain pairs of nodes. Typical examples are physical systems such as electrical or pipeline networks, computer process charts, storage allocation schemes, and code marks of various kinds. In information retrieval, in particular, the nodes may represent keywords or terms, and the branches may represent relations between terms. To retrieve information, it is then necessary to compare the two-dimensional structures representing items of information, or documents, with the structures representing search requests.

In the present study an efficient structure matching procedure is outlined which can be used successively to alter the search requests so as to force agreement with the stored information identifications. The procedure is applied to two information retrieval systems: the first one is a system in which document graphs are matched with request graphs, and the other is based on a comparison of syntactically analyzed text excerpts with a stored dictionary of phrases.

Training a Computer to Assign Descriptors to Documents: Experiments in Automatic Indexing
M. E. Stevens, G. H. Urban
National Bureau of Standards, Washington, D.C.

Experiments in Information Correlation
J. L. Kuhns, C. A. Montgomery
Bunker Ramo Corp., Canoga Park, Calif.

Some Flexible Information Retrieval Systems Using Structure Matching Procedures
Gerard Salton, Edward H. Sussenguth Jr.
Harvard Univ., Cambridge, Mass.

BUSINESS DATA PROCESSING

Chairman:
Dr. C. C. Gotlieb
University of Toronto
Toronto, Ontario

The two papers which make up the formal presentation of this session are concerned with quite different levels in data processing. Martin A. Goetz's paper is a technical but clear presentation of some improved methods for internal sorting and for tape sorting by the oscillating merge method. This merge method is extended for use of computers which have tapes that can read only in a forward direction. James C. Miller's paper is a general method for looking at a business as a whole and detailing its components and functions. Although the analysis starts with concepts, it results in the specification of operations, inputs, outputs, and managerial decisions and actions. The method therefore lends itself to computer simulation and application.

After discussing these papers the panel, consisting of C. C. Gotlieb, T. B. Steele, and J. E. Cremeans, will consider business data processing from a scientific point of view. In particular the literature of business data processing will be examined and also those aspects of the subject which scientists should be aware of.

Two New Improvements in Sorting Techniques
Martin A. Goetz
Applied Data Research Inc., Princeton, N.J.

Conceptual Models for Determining Information Requirements
James C. Miller
Arthur D. Little Inc., Cambridge, Mass.

NEWS BRIEFS

GE ADDS 400 HARDWARE TO RUN 1401 PROGRAMS

GE Computer has jumped feet first into the 1401 market with a new hardware adaptation to its 400 family which allows those machines to run 1401 programs as is, in the same fashion as the IBM 1401 and 7010 can in the 1401 compatibility mode. In effect the new device stores special 1401 logic to complement 400 family logic. A 1401 loader is prefixed to the 1401 deck, which is stored in the 400 memory and run.

The device, which can be installed in the main frame on site, will run on the same system configuration used by a 1401, with the exception of 1405 and 1311 disc files, optical character readers or MICR equipment.

Cost for the new unit has not been fixed yet, but GE states that the new 415—low end of the family—will be "competitive" with the 1401 and the Honeywell 200, which uses a translator to run 1401 programs. A four-tape system with 32K-character memory might run $7350/month, according to one GE spokesman. The company will also offer translators for the 1410, primarily because most people code for that machine in Autocode or IOCS.

UPGRADED 1004'S AVAILABLE

One of Univac's problems with its 1004 sales was the questions of those who foresaw a need to upgrade their card systems. Two answers have been announced: a speeded up 1004 and a mag tape system. Present users are being offered the speed pack, which decreases core cycle time to 6.5 usec (19% faster) and increases the card I/O by 50%, to 600 per minute. The cost is $125 per month.

Next step up is the 1004 III, which can take up to two mag tape units at an added rental cost of $800 per month. Data recording is in IBM-BCD or any six-bit code, and variable densities are 200, 556, and 800 bpi. Rental costs are $2,075 to $2,575, and price from $83-103K. Both hardware modifications can be done on-site.

FEDERAL STATISTICAL COSTS RISE

The federal government has reported expenditures for fiscal '63 of 113.7 megabucks for the collection, compilation, processing and publishing of statistical information. This includes almost 23 megabucks for edp hardware and personnel. Of the latter figure, about half was for personnel, the remainder for equipment, supplies, and capital outlay.

Federal expenditures for the statistical function alone increased 23% over fiscal 1961, while the edp cost (above) more than doubled during the same period. Most of this, however, reportedly reflects the replacement of the Census Bureau's Univac I with an 1107, as well as concomitant site preparation costs.

Largest executive department-user of computers for statistical purposes was the Commerce Dept. ($11.5 million), followed by Health, Education, and Welfare ($4.4 million) and Agriculture ($1.7 million).

BURROUGHS MARKETS SLOWER B 200'S, 1401 TRANSLATOR

Burroughs is offering a slowed-down, cut-rate version of its B 200 series. Called the 100 series, the systems offer slower main frames and peripheral equivalents of the B 260, 270 and 280. The 100 features a 10-usec memory instead of the six usec for the 200. New peripheral speeds and monthly rental prices follow, with their 200 equivalents in parentheses: card reader, 400 cpm, $300 (800, $400); printer, 475 lpm, $700 (700 lpm, $1200); MICR document sorter, 1200 documents/min., $1750 (1560, $1200); no change for the card punch. Tapes are restricted to one density (200 bpi) with a 24KC transfer rate.

Main frame rentals for the various systems have been cut as follows: 260: $1500/month; 160: $900/month ($75/month less than the Honeywell 200); 270: $1650/month; 170: $1250; 280: $1585; 180: $1085.

Purchase prices have also been slashed, from $51K for the 260 to $32K for the 160. The metered use plan for the 200 applies to the 100 series, which has a minimum required use of 88 hours. Another gimmick is the availability of a special lease plan under which the equipment is installed for one-half price, after which the customer pays 3/10 of 1% of the monthly rental for every hour used. Thus, a half shift would cost 76% of full shift rental; full shift rental would total 103% of the same use under the regular lease plan.

B 200 series software and utility programs are said to be compatible with the 100 series. Significantly, a translator for the 200's, recently announced, enables them to run programs written for the IBM 1401, 1401-G, 1440, and 1410.

PHONE TRANSMISSION OF PIX, HANDWRITING ANNOUNCED

Two announcements of experimental data communication by telephone lines were made recently. Bell Telephone Labs is using a 240,000 cycle-per-second channel equal in bandwidth to 60 voice circuits. It reportedly has a potential of transmitting 200,000 bps, or 16 8½ x 11-inch facsimile pages per minute (with a 100 line per inch definition).

Also experimental is the transmission of handwriting over voice circuits by General Telephone & Electronics. Electrowriter devices are being used as terminal units; handwriting produced on the device is transmitted in the form of voice-frequency electronic tones to another Electrowriter, and displayed with closed-circuit TV. Having classroom lecture applicability, this system reportedly can send "sound and sight" from Los Angeles to New York for $72.90, compared with a transmission cost of $3,530 using TV gear.

COMPUTER SCHEDULES CLASSES FOR NEW ENGLAND STUDENTS

The scheduling of classes for 17,000 students in 18 secondary schools is being handled on computers by the nonprofit New England Education Data Systems organization. NEEDS is using a 7090/1401 at the Boston

Meet The Problem Solvers from General Electric

They can help you put computers to work where they will do the most good— at the main profit points.

Is your computer profit oriented? Or is it being used mainly on financial and accounting data—functions that in most industrial firms represent less than 5 percent of total operating expenses? General Electric's Problem Solvers, like those at the left, are helping more and more companies save money by putting computers to work in key profit areas such as inventory control, allocation of resources, materials handling, quality control, and distribution.

How would your management react to a 30 to 80 percent cut in inventory, or even perhaps closing a few warehouses? Perhaps they would like to cut the cost of raw materials and parts by 5 to 10 percent (who wouldn't). Or maybe profit from an improvement in the effectiveness of key people—from faster reaction to customer needs, better quality control, automated design—from better scheduling, or better communication. These things are not only possible—they're being done every day by Data Processing and Systems Managers working closely with The Problem Solvers from General Electric.

10-million man-hours' experience. We not only make computers at General Electric. We *use* them. Today, we have 185 computers in operation. Altogether, we have far more than 10-million man-hours' experience in applying computers to the real profit points of business. Let The Problem Solvers share this wealth of know-how with you.

When you and The Problem Solvers have defined the problem and found the best approach to a solution, they will recommend the right combination of General Electric computers, peripheral equipment, and programs to solve it profitably. But analysis of the problem comes first. Hardware second.

What's your problem? Distribution? Labor/machine balance? Materials flow? Discuss it with a Problem Solver from General Electric. Call your nearest General Electric Computer Department office, or write to us here at Box 270, Section J-4, Phoenix, Arizona.

GENERAL ELECTRIC

CIRCLE 32 ON READER CARD

center of CEIR, Inc. Also being prepared are bi-monthly report cards for 12 schools.

To schedule classes for the average high school reportedly requires about two minutes of 90 time, and another hour on the 1401 to print student schedules and class lists. The software is not proprietary, according to G. Ernest Anderson Jr., director of R & D for NEEDS.

MIT INSTITUTES COMPUTERIZED CLASSROOM

A computerized classroom for students of civil engineering has been instituted by MIT. Hardware in the room includes an IBM 1620, a disc file, a teletype unit on-line with two time-shared 7094's, and closed-circuit TV. A regular department course for freshmen and one for graduate students are being taught, and more are planned.

In the freshman class taught by Prof. C. L. Miller, department head, students learn computer languages and solve design problems too complex for presentation in normal classroom settings. The TV is to show close-ups of machine operation. Languages being used are FORTRAN and three civil engineering problem-solvers: COGO, STRESS, and SEPOL.

NAVY USES CRT RECORDER TO PRINT PARTS CATALOG

Using a CRT computer recorder to produce microfilmed pages, the Navy is anticipating a 40% reduction in the cost of producing printed catalogs. Information on 400,000 stock items at the Naval Aviation Supply Office in Philadelphia was punched on cards for input to a 1401/1410, which produced a master tape. This data was displayed by a General Dynamics/Electronics S-C 4020, and converted to microfilm.

The 4020 reportedly produced almost 80 pages per minute (88 lines per page). From the microfilm, page proofs and negatives are produced for the preparation of offset printing plates. The technique was developed by GD/E and the Navy Publications and Printing Service.

● Special review seminars for the DPMA certificate examination will be sponsored this summer by the UCLA Extension Div. They will be held on Saturday mornings, from June 20 through Aug. 29. The exam is tentatively scheduled for Feb. 13, 1965.

● A speed pack which reportedly increases throughput on the Univac 490 by 20% has been announced. It cuts the six-usec memory cycle time to 4.8 usec. Rental cost is $250 per month for a 16K memory, $500 for a 32K store.

● Development of electrochemical models of the human nerve cell by Space-General Corp., El Monte, Calif., has led to talk of a possible electrochemical computer capable of simulating the brain's logic and learning functions. Using iron and silver wires, the artificial nerve cells have the property of inhibition, believed the key to a logic computer. These might be packed 10 billion or more per cubic foot.

● An experimental optical reader which reads handwritten numbers from a sales check is being tested by the Higbee department store in Cleveland, Ohio. For several months, clerks in selected departments will be writing pertinent information after each sale on special punched cards, and these will be read into a 1401. Purpose: to examine the feasibility of capturing merchandising and accounting information from one source document.

● A 1.9-megabuck contract for data reduction services at White Sands Missile Range has been awarded to Telecomputing Services Inc. The firm provides similar services to NASA at Huntsville, Ala., and Slidell, La., and to the USAF at Edwards AFB Rocket Research Labs.

● Systems Programming Corp., Santa Ana, Calif., has been awarded a contract by the Navy to program the inventory portion of the latter's Management Information System, which will run on the fleet of Univac III's set for shipyard installations. Contract value was not announced.

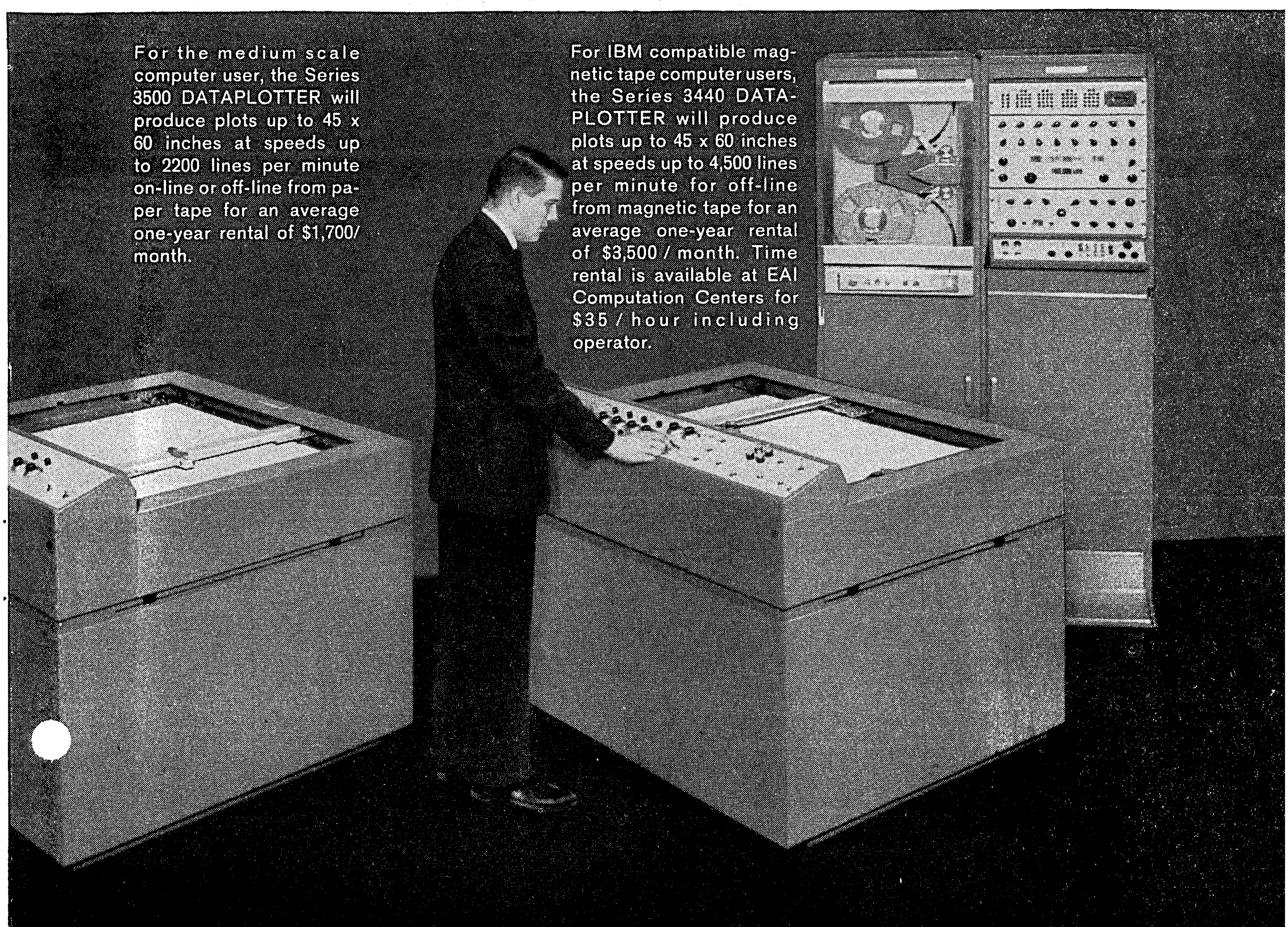
● Honeywell has turned over to the Univ. of Southern California two computers presently installed there, valued at more than 1.7 megabucks. The H-800 and 400 comprise the largest equipment gift ever made to USC, and enables the school to receive an additional $588K from the Ford Foundation under terms of its $6½-million conditional matching grant. More than 100 research projects in the physical and social sciences are being carried on with the hardware, including a study of the effects of smog on animals.

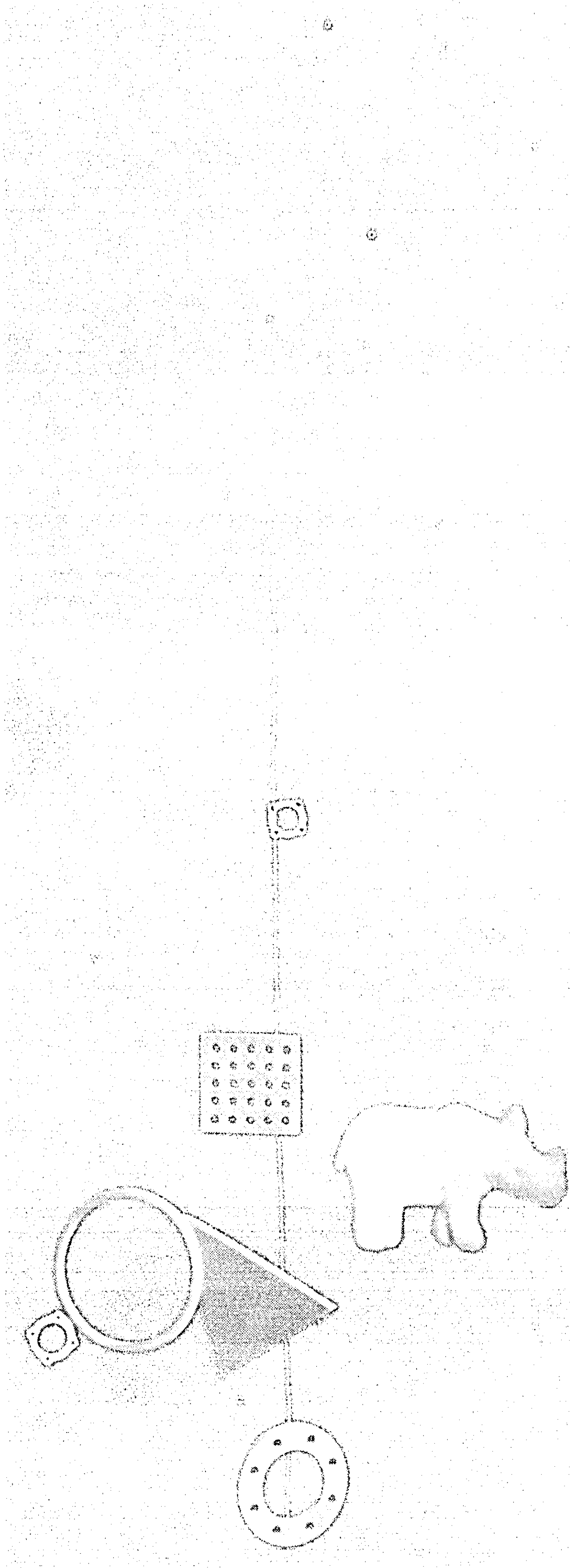
● Research into the statistical reconstructions of the past by compiling large masses of historical data has been undertaken by CEIR Inc., Washington, D.C. Object will be to study the probable results of decisions other than those actually made, in such areas as tax judgments, public utility rate determination, and trust fund administration. Hardware being used: 7090/1401.

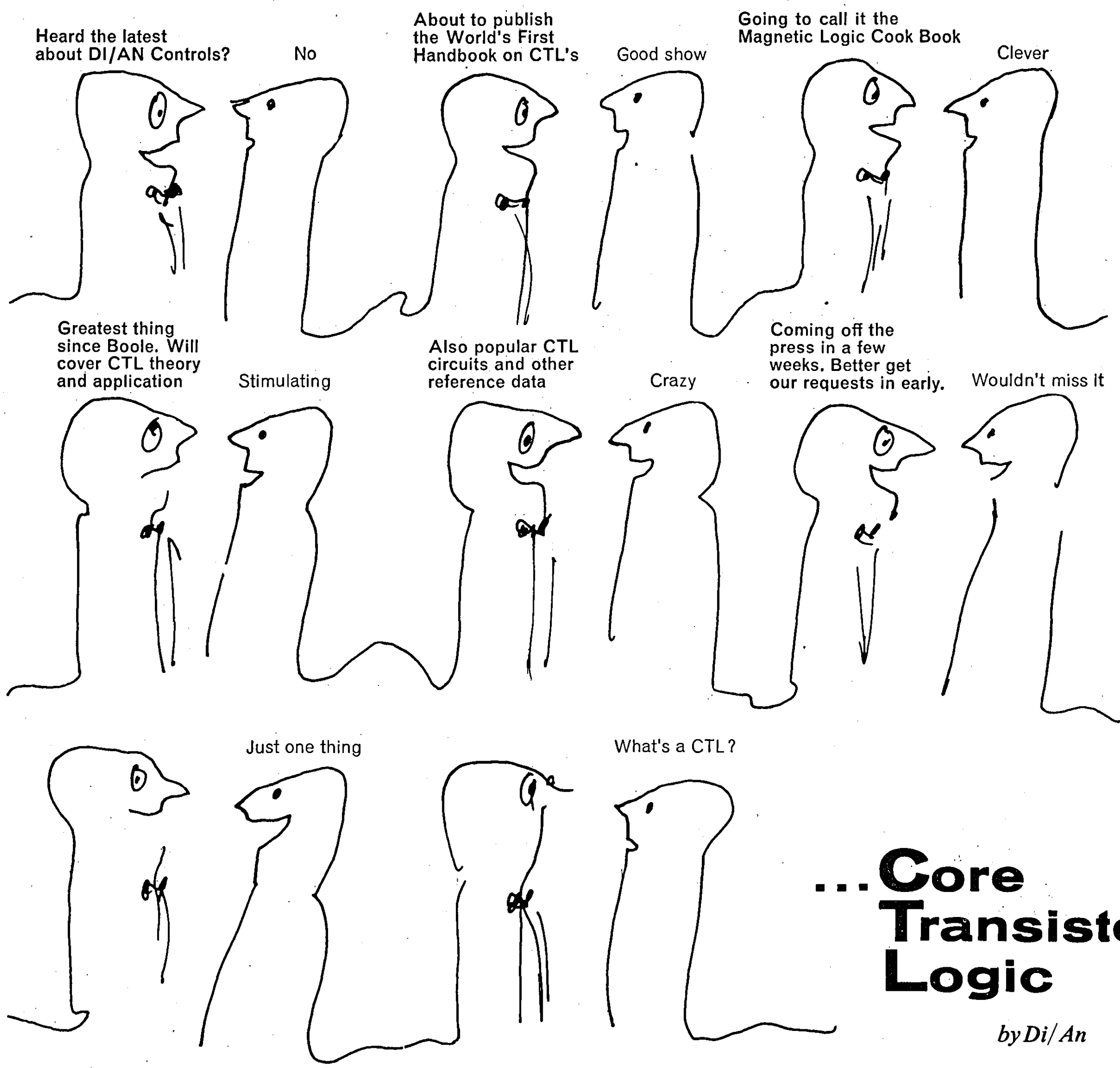
● A Dept. of Defense Computer Institute has been established to teach fundamentals to high-level military and civilian brass of DOD and military departments. The course will include operation of desk-size training versions of hardware, as well as software and applications. Following one-week courses for generals, admirals and civilian counterparts, longer sessions for lower grades are scheduled. Under policy guidance of the Office of Director of Defense Research and Engineering, the institute is operated by the Navy. Captain Horace S. Foote, USN, is director.

● RCA has taken the 4102 military computer which still controls some radar dishes, tied on a TDX in front, and developed a communications processor. The Teletype Data Exchange buffers messages in an 18K-bit glass delay line memory which has run at 26 mc, and can go faster. The 4102, some 10 installed, has a 4½-usec cycle time and 16 levels of interrupt. Also on-line: a Bryant disc and Anelex 1,000 lpm printer.

● A Stanford Univ. 7090 is being programmed to act like a woman patient with anxieties and indecisions toward men. Shouldn't be difficult, really. The computer simulation of personality is being undertaken by Prof. Kenneth Mark Colby, psychiatrist and research associate in computer sciences. Objective is to hold psychotherapeutic sessions with the "patient" without concern for mistakes made in questions asked, as well as to learn how best to modify a patient's behavior. Language used is SUBALGOL.



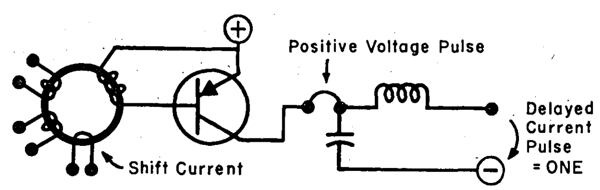




...Core Transistor Logic

by Di/An

A CTL IS . . . a UNIVERSAL logic element, with MAGNETIC storage and delay, made with a toroid having several windings, a transistor, and a pulse delay network.



A logic function is performed when the core is (or is not) driven to the "ONE" state by INPUT or INHIBIT current pulses in either or both of the two windings at the left. A SHIFT current may then be applied through the bottom winding, and if the logic result was "ONE", the core will switch, the flux change will be sensed and amplified, and an output pulse will be delivered by the delay network in time to INPUT or INHIBIT succeeding CTL's. If the logic result was "ZERO," the SHIFT current will not switch the core and an output will *not* appear. A useful voltage output appears at the collector terminal when the core switches from ONE to ZERO. Each CTL can SHIFT (jumper) and INPUT or INHIBIT a number of others. Fan-in is good, too—a 100-legged AND NOT, for instance, with one CTL.

WHAT CTL'S DO...A few examples: counters, clocks, scalers, digital comparators, sorters, adders, and arithmetic units. In short, the CTL's do everything logical —only one type of element is required—ultimate simplicity and economy—minimum design and inventory cost. CTL's are reliable because they don't ask much of the transistor—and we have the data to prove it.

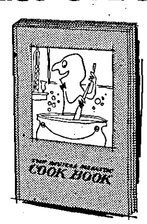
AND they are not triggered easily by noise.

AND they take negligible power—draw current only when they need to change state.

When the power drops out—data stays. That's one big reason why most space vehicles are packed with them.

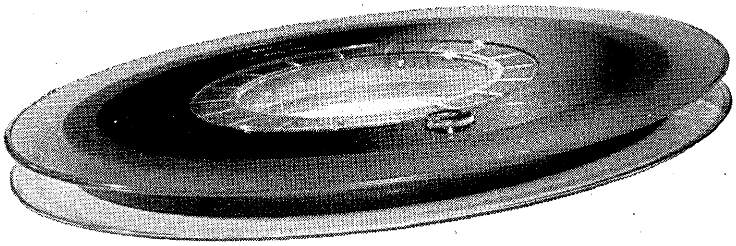
The FREE and easy way to use CTL's

JUST ORDER YOUR COPY OF DI/AN's new hardbound MAGNETIC LOGIC COOK BOOK . . . a practical encyclopedia of proven CTL circuits, indexed by type and application, with some palatable theory on the side.



Di/An Controls, Inc.
944 Dorchester Avenue, Boston, Massachusetts, Zip Code 02125
Tel. (617) AV 8-7700; TWX 617-288-5963 *Leadership in Digital Magnetics*

CIRCLE 36 ON READER CARD



This is a reel of new, **improved** Computape.

What do we mean by improved?

Longer wear, less static build-up, greater reliability than ever before.

Skeptical? Allow us to make a suggestion:

Test it yourself. Against <u>any other</u> tape.

If that doesn't convince you, you're just plain stubborn.

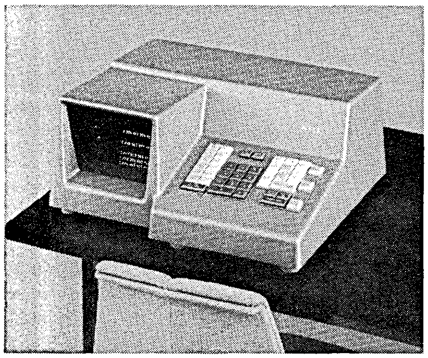
COMPUTRON INC.
122 CALVARY STREET, WALTHAM, MASSACHUSETTS

CIRCLE 38 ON READER CARD

NEW PRODUCTS

electronic calculator

The Scientific has three arithmetic registers, a CRT display, and three memory registers. The latter is for data recall, enabling transfer to and from arithmetic registers (visible on the display) for subsequent operations. The square root of a 23-digit number can be taken in less than two



seconds. It also features automatic decimal point location and compatibility with dp I/O devices such as paper tape punches and readers. WYLE LABORATORIES, 128 Maryland St., El Segundo, Calif. For information:

CIRCLE 200 ON READER CARD

gp computer

The 415 is the smallest member of the Compatibles-400 family. Built in is hardware which enables it to run programs prepared for the 1401, 1401-G, 1440, and 1410. Core memory is from 16-128K characters, and cycle time is 2.3 usec per character. Word size is 24 bits plus parity. Also featured: eight I/O channels, cycle interleaving, and repertoire of more than 200 instructions. Rental costs start at $4,770. GENERAL ELECTRIC COMPUTER DEPT., 13430 N. Black Canyon Highway, Phoenix, Ariz. For information:

CIRCLE 201 ON READER CARD

time-sharing computer

The PDP-6 has 8-256K (36 bit) words of directly-addressable core with an access time of 0.8 usec, 15 index registers and/or 16 accumulators, seven-channel priority interrupt system, and a repertoire of 363 instructions. A Fast Memory module with 16 words has a 0.4 usec cycle time; thus fixed point add time is 2.7 to 4.3 usec, and floating point add: 5.8-8.0 usec. Memory protection and relocation registers are included for time-sharing operations.

Busses link the I/O and memory subsystems to the processing subsystem, and each subsystem functions asynchoronously. Each processor can service up to 128 I/O devices. Software includes FORTRAN II, a monitor and assembler. DIGITAL EQUIPMENT CORP., Maynard, Mass. For information:

CIRCLE 202 ON READER CARD

portable data gatherer

The S-3100 accommodates a mixture of 96 high and low-level inputs, fixed data entry, selectable digital data display, and output recorded in gapped or gapless IBM binary mag tape format. Samples are to 10-bit accuracy at rates to 6,000 sps. EPSCO INC., Westwood, Mass. For information:

CIRCLE 203 ON READER CARD

management software

MENTOR not only monitors such activities as budgets and projects, but also forecasts performance based on past experience. It reportedly differs from PERT, which takes a component approach, by being more system-oriented. It continually updates forecasts in terms of the quality of prior forecasts. It is compatible with FORTRAN systems. COMPUTER CONCEPTS INC., 1012 14th St., N.W., Washington, D.C. For information:

CIRCLE 204 ON READER CARD

mag tape unit

The 570 uses an electro-pneumatic drive, moving tape by contra-rotating, porous capstans against which the tape is forced by air pressure. A multiplex interface permits time-shared use of the drive by two tape controls on the same or different com-

puters. Densities are 200 and 556 bpi, maximum transfer rate: 62KC. The 570 is for use with the PDP-1 and 4. DIGITAL EQUIPMENT CORP., 146 Main St., Maynard, Mass. For information:
CIRCLE 205 ON READER CARD

data transmission

The 27A Duobinary-Datatel uses high frequency radio links to transmit 2,400 bits per second. Slower speeds using fewer channels also are available. The complete system with diversity receivers can be housed in two 6½-foot racks or two 77-inch cabinets. LENKURT ELECTRIC CO. INC., 1105 County Rd., San Carlos, Calif. For information:
CIRCLE 206 ON READER CARD

data logger

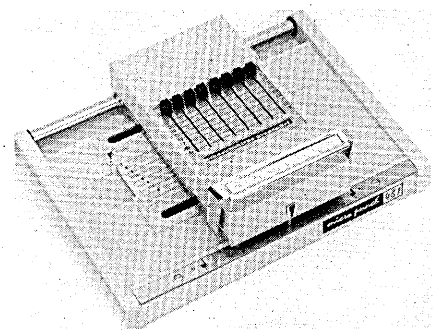
The 725 is for automatic sampling, measuring and recording of low voltages over extended time periods where low-level transducers are used. Measuring range is ±10 microvolts to ±999.9 volts in full-scale ranges of 9.999/99.99 millivolts and .999/9.999 /99.99/999.9 volts. NON-LINEAR SYSTEMS INC., Del Mar Airport, Del Mar, Calif. For information:
CIRCLE 207 ON READER CARD

mag tape reel

An aluminum hub mag tape reel replaces plastic models at no increase in price. Also featured: smaller windows, reportedly without hindering the threading operation. IBM SUPPLIES DIV., P.O. Box 218, Dayton, N.J. For information:
CIRCLE 208 ON READER CARD

portable punch

Model 461 simultaneously prints and punches eight columns of numeric data in any selected field of an 80-column card. Removable program bar



can be cut to order, limiting punching to selected fields. Prints through an inked ribbon; weights eight pounds. PAUL G. WAGNER CO., 2865-71 E. Washington Blvd., Los Angeles, Calif. For information:
CIRCLE 209 ON READER CARD

a-d converters

Four all-silicon devices have conversion rates to 30,000 bps, accuracies up to ±0.01%. Two binary models have output formats of 10 or 13 bits plus sign; two BCD models have three or four decimal digits plus sign. SCIENTIFIC DATA SYSTEMS, 1649 17th St., Santa Monica, Calif. For information:
CIRCLE 210 ON READER CARD

control computer

The DigiTele 3M-2018 has 2K words of memory and a 78-usec operating time. It can receive input from digital transducers, counters, A-D converters, and has uses in data logging and alarming, test stand operations, and automatic plant start-up and shutdown. Prices start at $12K. THE 3M CO., 2501 Hudson Rd., St. Paul, Minn. For information:
CIRCLE 211 ON READER CARD

data communications

The 7711 is a buffered terminal which permits two-way communications: tape-computer, tape-tape, and tape-card. Buffers range from 200 to 2,400 characters of core, and speeds from 150 to 5,100 cps. IBM DATA PROCESSING DIV., 112 E. Post Rd., White Plains, N.Y. For information:
CIRCLE 212 ON READER CARD

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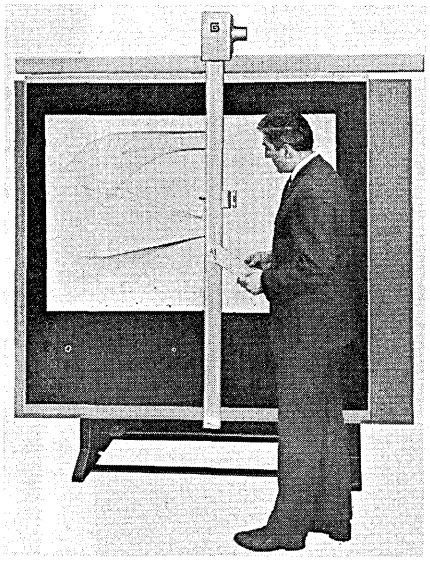
drafting machine

The VP 600 has a table size of 50 x 60 inches, and produces a graphic display of digital information on film, paper, vellum, cloth, Mylar. Drawing



speed: up to 200 inches per minute. Maximum accumulative accuracy is ± 0.010 inch, and repeatability is ± 0.004 inch. GERBER SCIENTIFIC INSTRUMENT CO, P.O. Box 305, Hartford, Conn. For information:

CIRCLE 213 ON READER CARD

jumbo plotter

Model 99.361 has a surface of 45 x 60 inches, and permits scaling from 0.05 to 10 volts per inch. Available are three modes: point, symbol and line plotting. Speed at the first two is 80 per minute with maximum error of ±0.05%; in line mode, 20 per minute with end points accurate to ±0.5%. ELECTRONIC ASSOCIATES INC., Long Branch, N.J. For information:

CIRCLE 214 ON READER CARD

elevated flooring

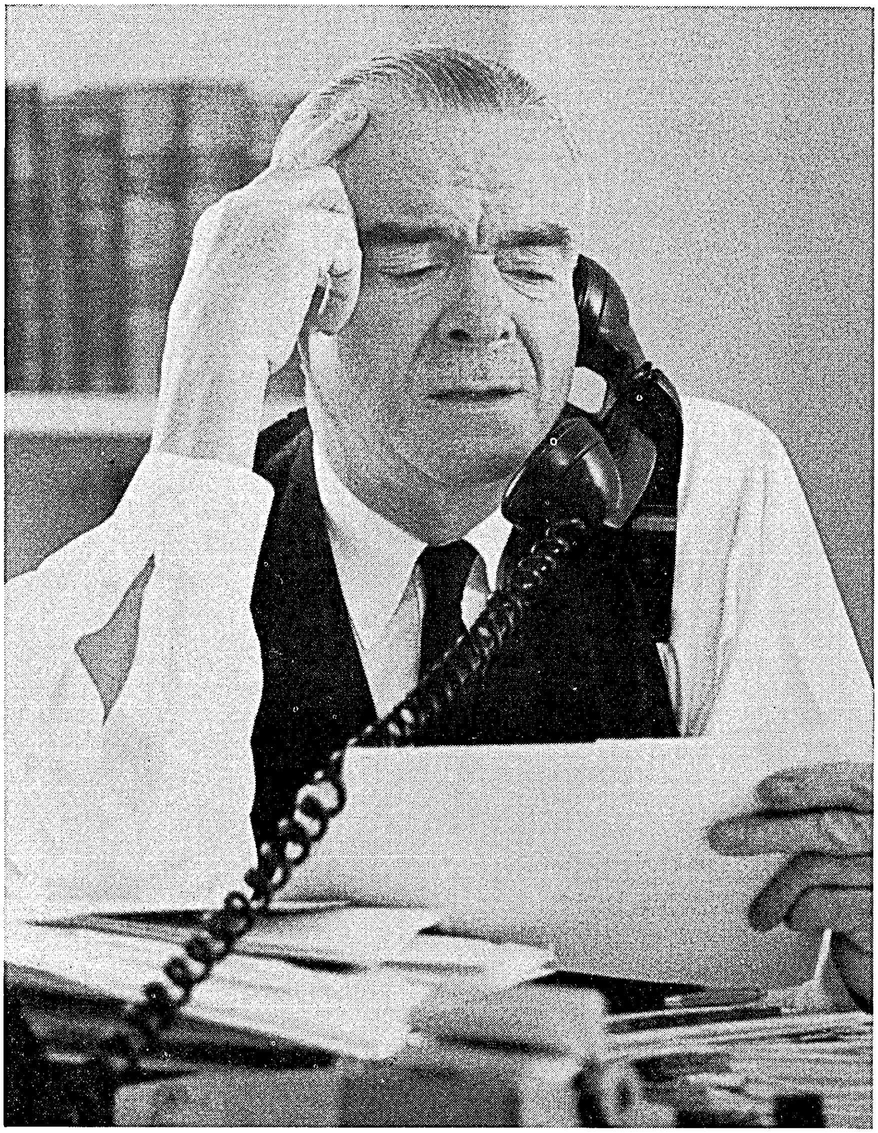
Infin-ac consists of hardwood panels with tapered edges to facilitate fitting and removal, and are available in natural finish, vinyl tile or carpeted units. Laminated panels are non-conductive. D. B. FRAMPTON & CO., INFIN-AC DIV., Huntington Bank Bldg., Columbus, Ohio. For information:

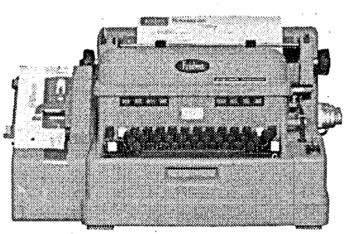
CIRCLE 215 ON READER CARD

mag tape safe

The Data-Safe holds from 44-130 reels in units approved by UL for fire protection of at least four hours at steady 2,000°F. Also adapts to disc packs, CRAM cartridges, microfilm. DIEBOLD INC., Canton, Ohio. For information:

CIRCLE 216 ON READER CARD





NEW PRODUCTS . . .

custom data vault

Built-in repositories for mag tape, etc., have UL-approved protection for four or six hours, and are built to size. Heat transfer between masonry walls and interior minimized with layer of air, and inner door closes out moisture. DATA-AMERICAN EQUIPMENT CO., 333 No. Michigan Ave., Chicago, Ill. For information:

CIRCLE 217 ON READER CARD

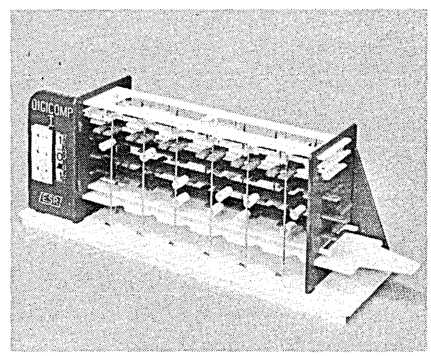
data transmission

The 521 is a Dial-o-verter mag tape terminal which transmits over voice-grade phone lines, Telpak channels and broadband communications facilities. Options include fixed or plugboard-controlled code translation, varying tape density and format. DIGITRONICS CORP., Albertson, N.Y. For information:

CIRCLE 218 ON READER CARD

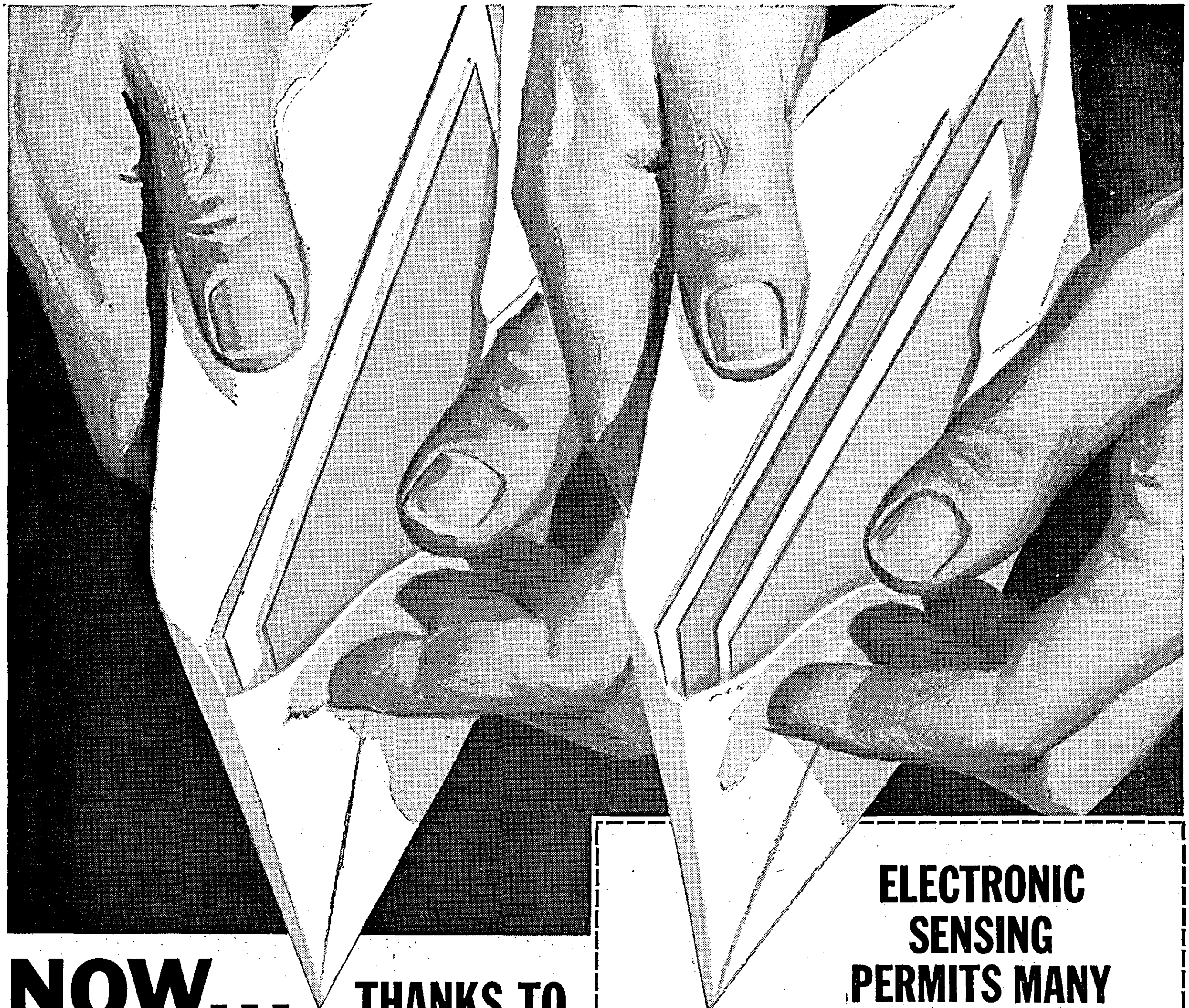
child-scale computer

Digi-Comp is a working digital computer, in plastic, which adds and subtracts in binary, shifts, complements,



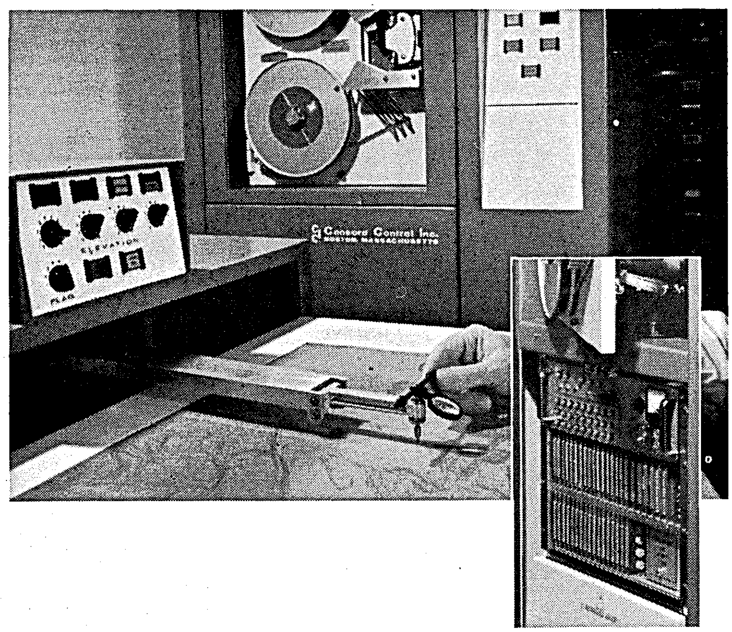
carries, compares and sequences. Measuring 12 x 3½ x 4 inches, it consists of sliding panels, eccentric rods, rubber bands, and "programming" plugs. With 28-page instruction manual, $4.98 ($5.50 postpaid). E.S.R. INC., 34 Label St., Montclair, N.J. For information:

CIRCLE 219 ON READER CARD



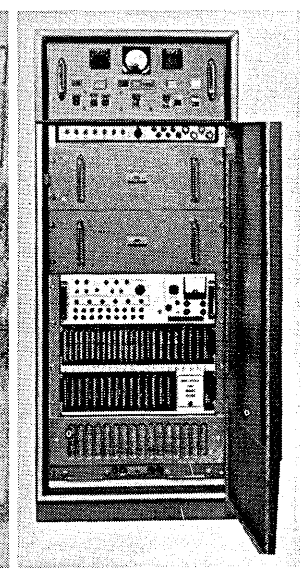
Either way you look at it Fabri-Tek fits the picture

Pictures to digits



With this Floating Arm Graphics Recorder engineered by Concord Control Inc., a U. S. Army Map Service operator traces the contours, shorelines, and highways on a 20 by 30-inch map. Automatically, this graphic data is digitized and stored. Any graphic information described by lines, points or symbols is quickly translated into digits with this amazing machine. Whole libraries of graphic data can be converted to computer format and maintained for instant recall or processing. A Fabri-Tek memory system serves as the buffer storage.

Digits to pictures



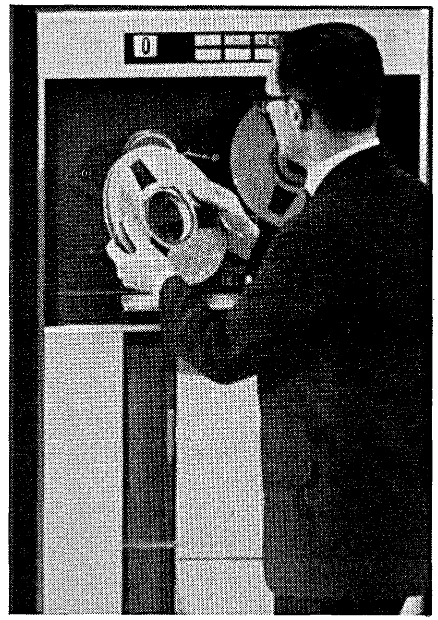
This Tiros satellite cloud photograph was a digital recording until the new Hamilton Standard Facsimile Synthesizer translated it to standard facsimile equipment input. Designed and developed for the United Aircraft Systems Center, this equipment permits graphic information of this type, generated by computers, to be disseminated on a worldwide basis through regular communications systems and facsimile reproducers. Transmission of such data is accomplished by reading out a magnetic tape one scan line at a time into a buffer storage memory. The memory is then gated to a modulator which impresses the data on a carrier to produce a signal identical to the output of a conventional facsimile scanner. A Fabri-Tek memory system serves as the buffer storage.

These are only two of the many ways versatile Fabri-Tek memory systems can be applied. Name your application, any capacity, any speed. We'll bet that Fabri-Tek will fit the picture. Write, call, or wire Robert E. Rife, Fabri-Tek Incorporated, Amery, Wisconsin. Phone: COngress 8-7155 (Area 715). TWX: 715-292-0900.

FABRI-TEK

EXECUTIVE OFFICES: FOSHAY TOWER, MINNEAPOLIS 2, MINNESOTA

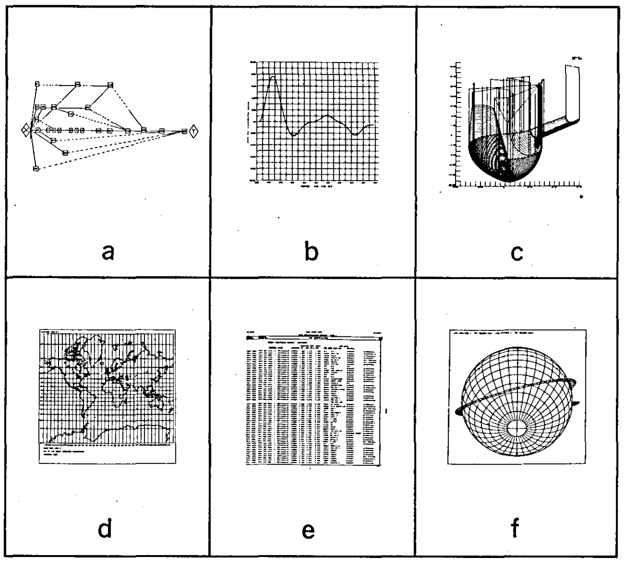
CIRCLE 46 ON READER CARD



Computer Output Questionnaire

Test your knowledge of the latest methods available for displaying and recording the output of large-scale digital computers.

Questions



1 How much time was required to record the above output sample "b" on film.

a. One hour ☐ b. One minute ☐
c. One second ☐ d. One-half second ☐

2 How much time was required to print all of the above samples from tape transport start to delivery of finished paper to the engineer?

a. Thirty seconds ☐ b. Six minutes ☐
c. Twenty-five minutes ☐ d. One hour ☐

3 How much time was required to write the computer program for producing sample "b"?

a. One minute ☐ b. Five minutes ☐
c. One hour ☐ d. Four hours ☐

4 How much large-scale computer time (IBM 7090 class) was required to prepare tape for output sample "b" shown above?

a. Less than three seconds ☐ b. One minute ☐
c. Five minutes ☐ d. Ten minutes ☐

5 How many of the following output types can be produced by one versatile computer recorder already in commercial operation? (1) 16mm microfilm for automatic storage and retrieval; (2) 35mm microfilm; (3) quick-look paper copy; (4) high-quality paper copy for reports and distribution; (5) vellums; (6) page-size film negatives; (7) animated motion picture strips.

a. (1) through (3) ☐ b. (1 through 4) ☐
c. All except (7) ☐ d. All of these ☐

6 Each of the six samples above represents a specific computer output application. Match correct letter code of above samples to each of the applications listed below.

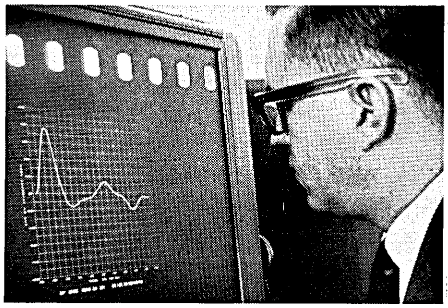
Curve Plotting ______
PERT Charts ______
Tool Path Drawings ______
Orbital Plotting ______
Mapping ______
Alphanumeric Line Printing ______

7 What is the minimum number of hours of daily usage required to justify economically an output device capable of producing all of the above samples in a matter of seconds?

a. Sixteen hours ☐ b. Eight hours ☐
c. Three hours ☐ d. One hour ☐

(Answers may be found on following page)

GENERAL DYNAMICS | ELECTRONICS GD SAN DIEGO



Answers

1 Answer: "d"—The annotated graph sample was recorded in one-half second on a General Dynamics S-C 4020 computer recorder which plots at 10,000 points/second and prints at 7,000 lines/minute. Even the most complicated sample, the map, took only six seconds.

2 Answer: "a"—Using S-C 4020's quick-look printing capability, an impatient engineer could have page-size paper output in less than 30 seconds after computer-generated tape is placed on the tape transport.

3 Answer: "b"—If x, y values of points to be plotted are stored in arrays X and Y; and titles for the graph, its x axis, and its y axis are stored in alphanumeric arrays PGTITL, XTITLE, and YTITLE, respectively, the single statement CALL AICRT3(1,X,Y,NOPNTS, 1,2,2,42, PGTITL, XTITLE, YTITLE, 1,1,32.0,1, DUMMY1, DUMMY2,1, DUMMY3, DUMMY4) will produce a labeled grid, the desired titles and the plotted curve.

4 Answer: "a"—Using the AICRT3 subroutine and its high density tape capability, S-C 4020 accepts data at input rates up to 62,500 six-bit characters per second, economizing on valuable computer time.

5 Answer: "d"—The versatile S-C 4020 produces all these types of output, including computer-generated movies. Movies are produced by creating slightly varying drawings which can be viewed with a motion picture projector.

6 Answers: Curve Plotting, b; PERT charts, a; Tool Path Drawing, c; Orbital Plotting, f; Mapping, d; Alphanumeric Line Printing, e; S-C 4020 allows organizations to use computers to translate output into graphic form for many different departments and groups.

7 Answer: "d"—In many centers where S-C 4020s are in operation, one hour or less of use per day justifies the cost. One user performs a complex plotting job for engineering, in a few minutes, which previously took a large drafting department several days. The same highly precise annotated charts are now produced simultaneously on paper and on microfilm.

For information on S-C 4020, write Dept. E-18, General Dynamics | Electronics, P. O. Box 127, San Diego, Calif.

For more answers on your computer output problems see the General Dynamics | Electronics Exhibit at Spring Joint Computer Conference, April 21-23, Washington, D.C.

NEW FIRMS & mergers in DP

General Kinetics Inc., Arlington, Va., has formed GKI Tape Service Corp., and opened a mag tape rehabilitation and testing center in Arlington. It is headed by Donald H. Blouch.

A Computing Sciences Div. has been formed by the Service Bureau Corp., New York. Headed by D. G. Collins, the division will offer large-scale computing services, such as the 7094 system at the newly-opened Houston, Texas, bureau.

Systems Programming Corp., Santa Ana, Calif., has opened an office in Silver Spring, Md. Placed in charge is Richard P. Castanias, formerly assistant director of the computing center at Notre Dame.

A manufacturing base for Ampex products in Japan has been created with formation of Toshiba Ampex K. K., which will produce computer memory products and instrumentation recorders for sale in Japan.

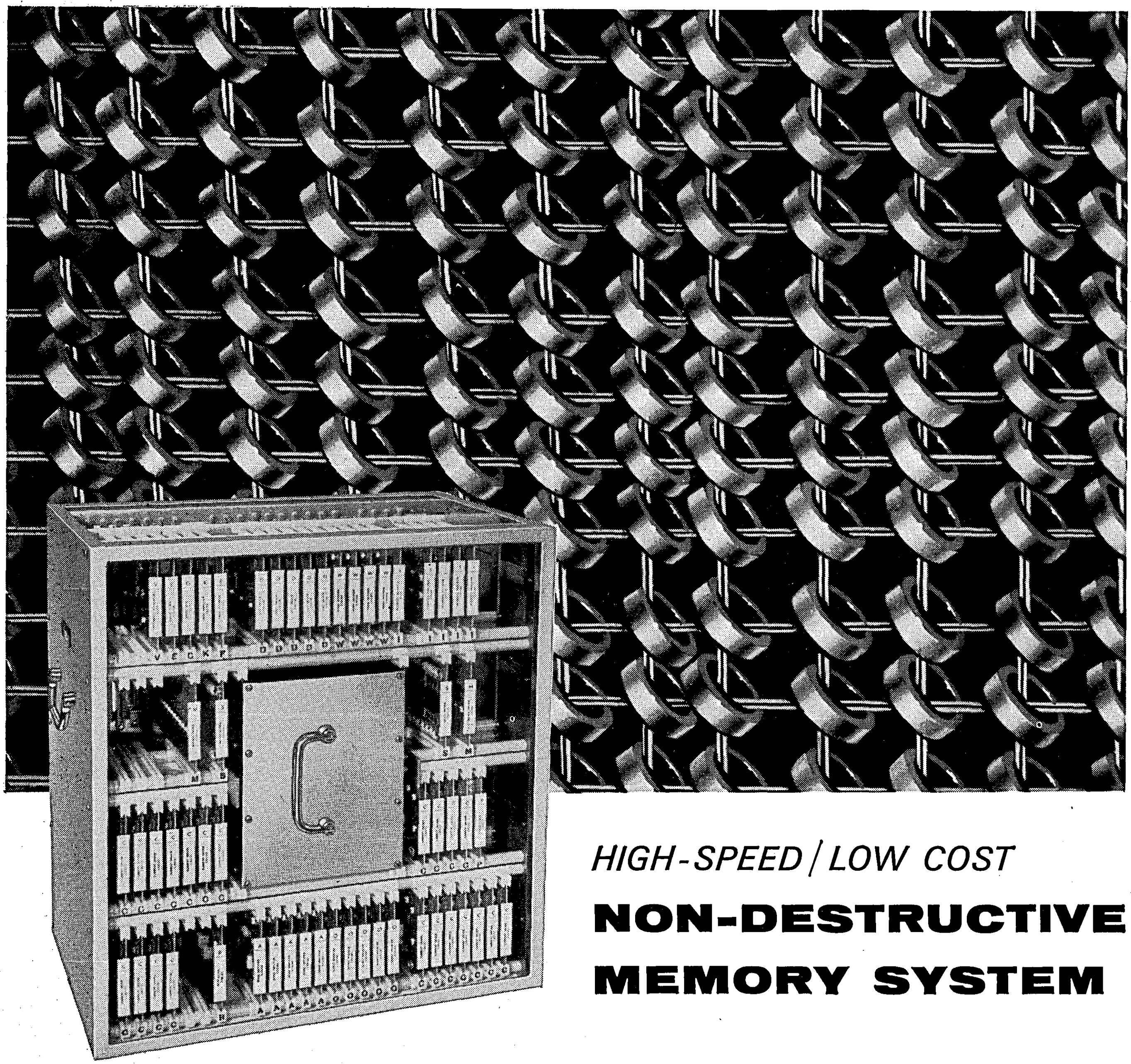
TRW's Numerical Control Systems operation in Cleveland, Ohio, has become part of the Bunker-Ramo Corp., recent consolidation of TRW Computer Div. and Martin Marietta's Electronic Systems & Products Div.

A Digital Products Group has been formed by the Amperex Electronic Corp. Products include counting and logic modules and digital control systems.

Applied Systems Inc., a dp consulting firm, has been formed in River Edge, N.J.

A Retail Total Systems Group has been established by National Cash Register Co. to assist department stores in planning fully integrated dp systems. Headquartered in Dayton, Ohio, the group is headed by L. M. Solganik, former dp manager for NCR's northeast division.

Scientific Computers Inc., Minneapolis, Minn., has acquired Workman Service Inc., which supplies temporary office help, and Workman Tabulating Service Inc. of Minneapolis. SCI is a service bureau firm headquartered in Minneapolis.



HIGH-SPEED / LOW COST

NON-DESTRUCTIVE MEMORY SYSTEM

The North Electric Non-Destructive Memory System uses conventional 50 or 80 mil memory ferrite cores, with information stored in either the saturated major loop or the demagnetized minor loop. Two cores per bit are used to obtain a bipolar sense pulse. System is electrically alterable.

Because of this, the North Electric system is . . .

FAST—No core switching . . . allows multi-megacycle read cycle.

INEXPENSIVE—Uses low cost conventional toroid memory cores versus higher cost multi-apperature devices. Uses conventional X-Y wiring . . . no Indian beadwork techniques or complicated patterns. 100% test of all cores before stringing.

RELIABILITY—No bit rewrite. No chance of losing information during rewrite cycle . . . or creating information due to noise. Two cores per bit provides common mode noise rejection on sense line. No sequencing of power supplies required. No loss of information due to loss of any source voltage.

POWER—Only constant voltage source required. Regulation need only be ±10%. Low power consumption . . . only 72 watts required for 1024 x 20 bit system.

The North Electric concept in Memory Systems has been proved for the past three years in military and commercial applications. For technical description of this technique, write to Product Manager, Memory Systems, and ask for booklet "North Electric Non-Destructive Memory Techniques."

OTHER DIVISIONS:
DEFENSE SYSTEMS—*Electronics • Command and Control Systems*
POWER EQUIPMENT—*Custom Power Systems • Battery Chargers*
TELECOMMUNICATIONS—*Public Telephone Systems & Equipment*

NORTH

NORTH ELECTRIC
ELECTRONETICS DIVISION • GALION, OHIO

CIRCLE 49 ON READER CARD

PB440 THE FIRST REAL SYSTEMS COMPUTER ?

SOME TYPICAL PB440 SYSTEMS APPLICATIONS

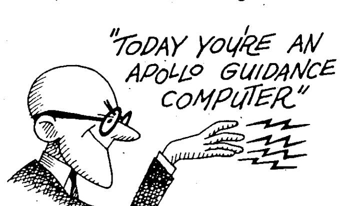
- Telemetry data reduction
- Communications switching and data formatting
- Hybrid analog/digital computing
- Real-time data acquisition
- Command and control
- Automatic checkout
- Launch control
- Antenna steering
- Nuclear reactor control
- Process control

WE THINK SO, but we put the question mark in so you wouldn't accuse us of unabashed arrogance. What we mean is we have a computer that isn't restricted by the fixed logic wired in by the manufacturer. The PB440 has a separate logic memory—distinct from its conventional memory—and commands and word formats are specified by information stored in this logic memory and can be readily changed. In other words, commands and word formats can be tailored by the user to fit the systems problem at hand. Packard Bell provides several command sets and the user can create additional commands as required.

A single PB440 can, in the fraction of a second it takes to reload logic memory, switch from one command set to another and thus from one application to another. No other computer can do this, and that's why we think it is the first real systems computer. Now, the system designer can adapt the computer to the problem, not the problem to a fixed command list and format.

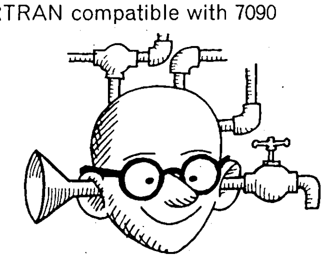
FOR THE SYSTEMS ENGINEER the PB440 can be a special-purpose computer designed (to his specs) for his specific system. But he still has the reliability, versatility, expandability and speed of the PB440 as a general purpose computer. This is all made possible by the Dual-Memory Stored-Logic organization of the PB440.

SPECIFICALLY, the systems engineer should consider the following features:

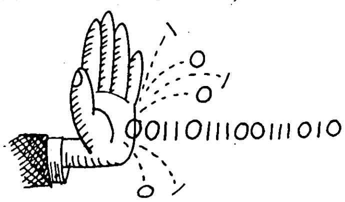


MICROPROGRAMMING the logic memory provides ability to duplicate command lists and formats of other computers. For example, digital guidance computer command structure and format can be developed before hardware prototypes are built. Similarly, you can duplicate the guidance computer in a hybrid simulation of a missile guidance and control system.

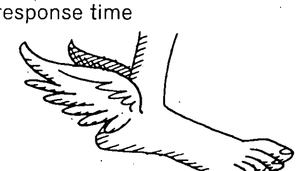
SOFTWARE • More than 100 systems-oriented commands written, more every day
170 scientific commands
FORTRAN compatible with 7090



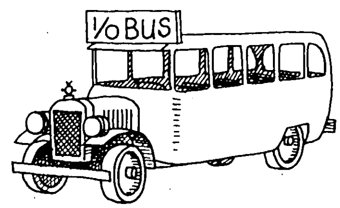
MEMORY ACCESS
Direct memory access from external devices
Simultaneous computation & I/O data transfer
Shared memory feature that permits multiple processor configurations



PRIORITY INTERRUPT • Multi-level, minimum response time

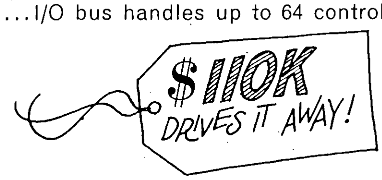


SPEEDS • Memories:
1 μ sec non-destructive logic memory (256 to 4096 words)
5 μ sec main memory (4096 to 32,512 words)
I/O rate to 9.6 million bits per second
Typical execution times, with memory access:
Compare data against upper & lower limits—13 μ sec, including two memory references
Floating point multiply 8 bit exponent,
16 bit mantissa—36 μ sec
24 bit mantissa—42 μ sec
39 bit mantissa—110 μ sec
Fixed point add—3 μ sec
Relocate data within memory—10 μ sec/word
Polar to rectangular coordinate conversion —435 μ sec



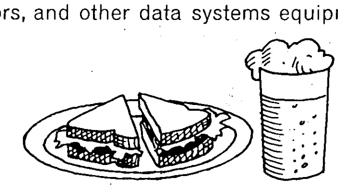
I/O VERSATILITY • Unique I/O bus design means more flexible arrangement of peripheral equipment. User need only add interface electronics as needed; does not pay for hardware capability he will never use. I/O system designed to accept next generation of higher speed peripheral equipment.

GENERAL CHARACTERISTICS • Parallel data handling mode ... 24 bit word length, can be programmed for 12 & 48 bits ... 400KC I/O character transfer rate, 800KC optional ... I/O bus handles up to 64 controllers.



PRICE • Basic computer with 256 word logic memory, 4096 word main memory: $110,000.

PERIPHERAL EQUIPMENT • Magnetic tape at 83.4, 41 or 25KC ... punched cards at 800/min. in and 250/min. out ... 1000 lpm alphanumeric printer ... paper tape at 500 char/sec read, 110 char/sec punch ... Selectric typewriter. Also Packard Bell A to D and D to A converters, multiplexers, commutators, and other data systems equipment.



THERE'S MUCH MORE to be said about the PB440 and its unique concept of Dual-Memory Stored-Logic. We have shelves of technical literature that can handle most of your questions, representatives who should be able to take care of the rest. If you are in Los Angeles, try and drop in for a demonstration. We might even pop for lunch.

Packard Bell Computer
A DIVISION OF PACKARD BELL ELECTRONICS
2700 S. Fairview Street, Santa Ana, California • C-18-7

See Us At the Spring Joint Computer Conference, Booths 125-128

NEW LITERATURE

SOLID-STATE LOGIC: 36-page booklet explains fundamentals of transistorized logic circuits, and describes their functions in computer application. Applications described pertain to circuits in the firm's multi-channel analyzer, a special purpose computer. RADIATION INSTRUMENT DEVELOPMENT LABORATORY, 4501 W. North Ave., Melrose Park, Ill. For copy:

CIRCLE 130 ON READER CARD

SOVIET LITERATURE: A survey of the published literature from 1962-63 on teaching machines and programmed learning in the Soviet bloc is topic of this 24-page book. Included are conferences on programmed instruction, computer-based teaching machines and programmed learning without teaching machines. Price is 75¢. U.S. DEPT. OF COMMERCE, OFFICE OF TECHNICAL SERVICES, JOINT PUBLICATIONS RESEARCH SERVICE, Building T-30, Ohio Drive and Independence Ave., S.W., Washington 25, D.C.

PROJECT SOFTWARE: Four-pager describes PROMOCON (Project Monitor and Control Method) for GE computers, an extension to its CPM program. Included are hardware requirements. GENERAL ELECTRIC COMPUTER DEPT., Phoenix, Ariz. For copy:

CIRCLE 131 ON READER CARD

DATA ACQUISITION & RECORDING: 4-page bulletin describes series 2100S digital data acquisition and recording systems for either sequential or simultaneous operation. Description, features and specifications of the system are included. GULTON INDUSTRIES, Technical Publications Dept., 212 Durham Ave., Metuchen, N. J. For copy:

CIRLCE 132 ON READER CARD

INFORMATION SYSTEM: Brochure describes Chrysler Corp.'s automated message switching system using the Datanet-30. GENERAL ELECTRIC COMPUTER DEPT., Phoenix, Ariz. For copy:

CIRCLE 133 ON READER CARD

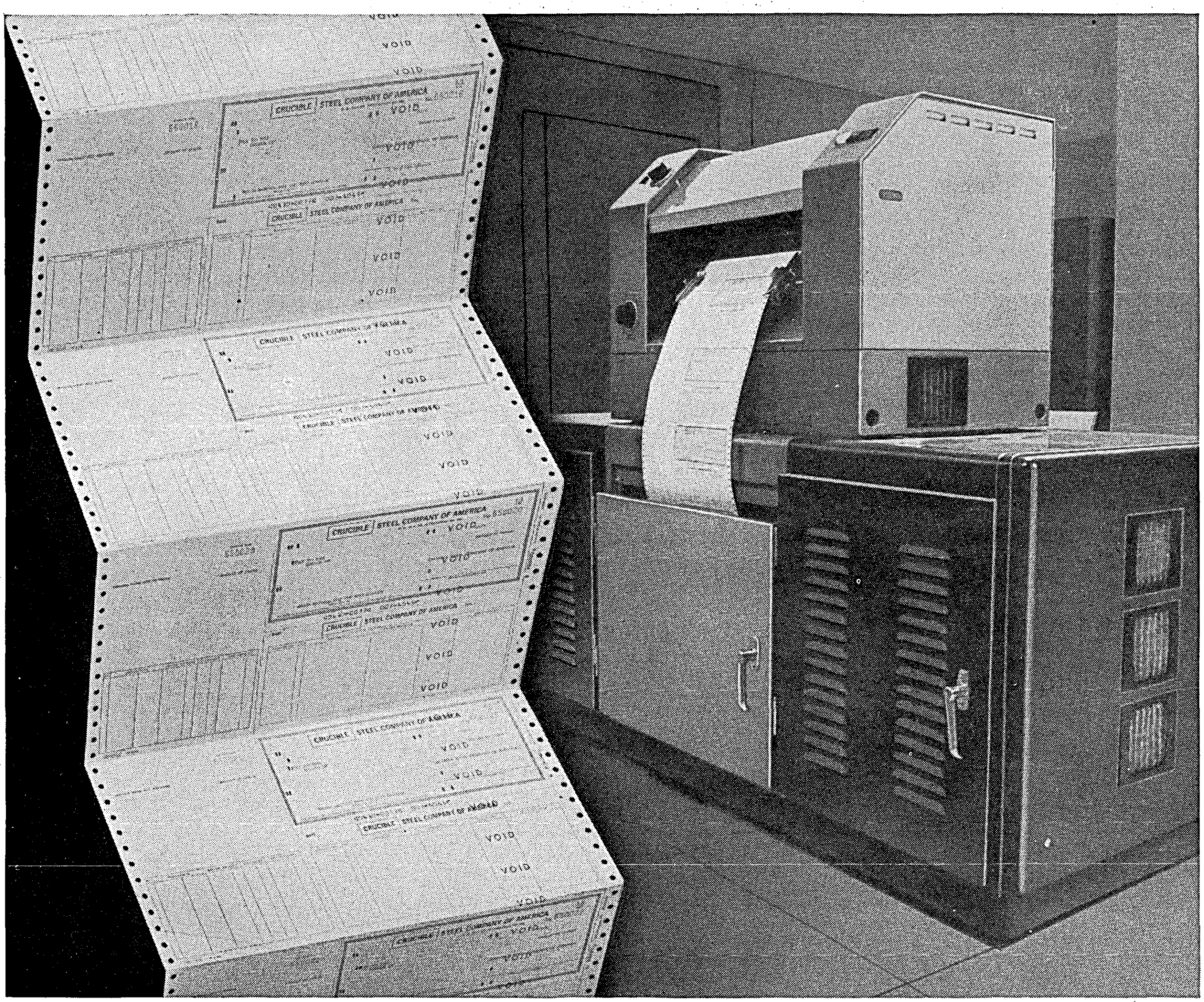
OSCILLOGRAPHIC RECORDERS: Bulletin R-519 describes the line of single- and dual-channel oscillo/riter (tm) recorders and component amplifiers. TEXAS INSTRUMENTS INC., Industrial Products Group, P.O. Box 66027, Houston, Texas. For copy:

CIRCLE 134 ON READER CARD

MATHEMATICAL FUNCTIONS: This 1060-page handbook includes text, *Who put the flexibility into Data Processing at* CRUCIBLE®?

FORMSCARD®

the only continuous tabulating card with NO medial waste strips



Crucible Steel Company of America needed continuous tabulating checks for its accounts payable . . . checks that could be processed at high speeds . . . checks that would eliminate the need for carbons by having *vouchers at both side and bottom.* A tall order? Not for FORMSCARDS!

FORMSCARDS' exclusive continuous tabulating cards offer *unlimited* flexibility, *unlimited* versatility.

That's why Crucible Steel uses eight different FORMSCARD tab checks for various payroll and accounts payable checks . . . why *you* should consider the advantages FORMSCARDS can bring to your firm's systems.

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Forms inc

WILLOW GROVE, PA. Phone: Oldfield 9-4000

- *Efficient operation on any printer at any speed*
- *Easily separated manually or on any burster*
- *Available pre-punched and with vouchers of any size at side, top or bottom*
- *Can be part of multiple part sets*

NATIONAL BUSINESS FORMS ASSOCIATION — FROM COAST TO COAST — MANUFACTURER-MEMBER

Manufacturers of line-hole continuous business forms. Samples on request—Sales representatives in principal cities

CIRCLE 54 ON READER CARD

NEW LITERATURE . . .

tables, graphs, formulas and bibliographies. It is priced at $6.50. U.S. GOVERNMENT PRINTING OFFICE, DIVISION OF PUBLIC DOCUMENTS, Washington, D.C.

PAPER TAPE READERS: Data sheet on the series 500 desk and panel mounted tape readers contains specifications including a timing chart and price information. ROYAL MCBEE CORP., INDUSTRIAL PRODUCTS DIV., 150 New Park Ave., Hartford, Conn. For copy:
CIRCLE 135 ON READER CARD

DIGITAL READOUT: Catalog sheet describes operating principle of this miniature rear-projection type digital readout. Also included are basic features, uses and several examples of how data is displayed by the Shelly Readout. CAL-GLO CO., 111 Eucalyptus Dr., El Segundo, Calif. For copy:
CIRCLE 136 ON READER CARD

D-A CONVERTER: Illustrated bulletin gives technical data on model 116 multi-channel digital-to-analog converter. Table of Options lists modifications which permit use of converter as a link between a digital data system and various analog display and control devices. MONITOR SYSTEMS INC., Fort Washington Industrial Park, Fort Washington, Penna. For copy:
CIRCLE 137 ON READER CARD

LINEAR PROGRAMMING CODE: The LP 90/94 Supplemental Usage Manual which incorporates documentation for various new proprietary routines is priced at $1.50. C-E-I-R INC., 1200 Jefferson Davis Highway, Arlington, Va.

CLOCK-CALENDAR SYSTEMS: Series 729, designed for use with IBM computers, is described and illustrated in a two-page bulletin. CHRONO-LOC CORP., 2583 West Chester Pike, Broomall, Penna. For copy:
CIRCLE 138 ON READER CARD

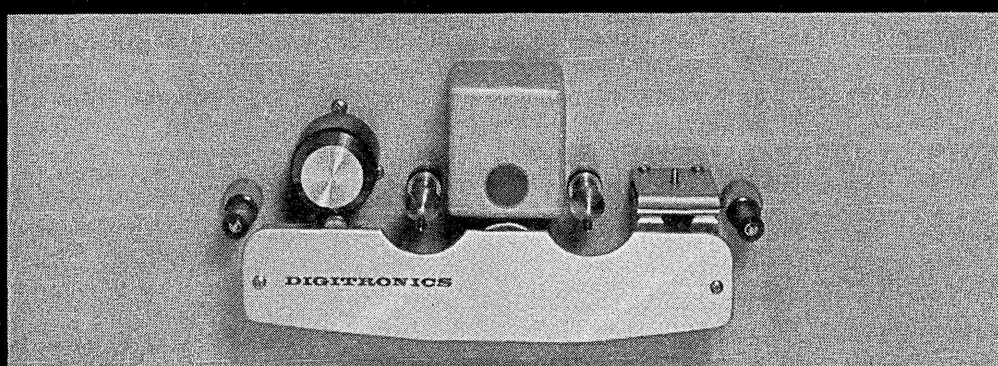
CORE MEMORIES: Brochure presents descriptions, technical features, applications, characteristics and specifications of the 781 random access, 782 sequential access and 783 sequential interlace. ELECTRONIC ENGINEERING CO. OF CALIF., Box 58, Santa Ana, Calif. For copy:
CIRCLE 140 ON READER CARD

NANOLOGIC 100: Booklet discusses this dp system and each of the 10 component modules available. Included are specifications, photographs and prices for each modular unit. CHRONETICS INC., 965 Nepperhan Ave., Yonkers, N.Y. For copy:
CIRCLE 141 ON READER CARD

MINISTORE III: Full specifications, application areas and an explanation of the operation of this general-purpose, random access magnetic core memory are given in an illustrated bulletin. RESE ENGINEERING INC., A & Courtland Sts., Philadelphia, Penna. For copy:
CIRCLE 142 ON READER CARD

CIRCLE 76 ON READER CARD

$1440 for a Digitronics high-speed tape reader?



Yes, and that's the least of it!

We set our sights on building the finest high-speed, photo-electric perforated tape reader, at the lowest possible price. And this is it.

The new Model 3000 is unidirectional. Its bidirectional brother is Model B3000, priced at $1585.

Both models are all solid state with self adjusting brakes and read 5, 6, 7, or 8-level tapes, at speeds up to 700 cps. Silicon photo-diodes in the read head service all eight data channels. Both models measure 19 inches wide by 7 inches high by 8¾ inches deep and weigh 28 lbs. each.

How did we do it?

Proven fundamental design philosophy. Specialized engineering experience. And, a lot of high quality know-how garnered from many years in the high-speed tape reader business.

You'll find no compromise on quality or hardware when you evaluate Models 3000 and B3000. For full details see your local Digitronics Representative. Or, if you prefer, write direct to Digitronics Corporation, Albertson, New York, or call Area Code 516, HT 4-1000.

DIGITRONICS
when every bit counts

CIRCLE 55 ON READER CARD

Q How to get tomorrow's performance with today's hardware?

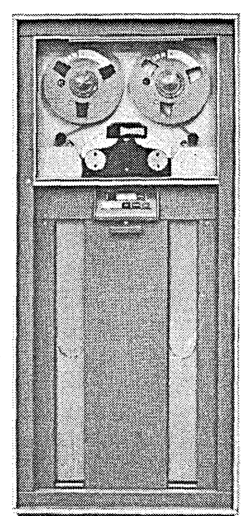
The tremendous pace of the EDP industry imposes a staggering problem on the hardware designer; how to specify critical components in existing system designs for immediate needs, yet, provide advanced performance capabilities for tomorrow's more sophisticated systems. That is the question!

A In transports, the M3000 offers tomorrow's performance today!

The all pneumatic drive M3000, by Midwestern Instruments, is the first of the true "second generation" digital transports described at the (Las Vegas) 1963 FJCC. Compatibility, reliability, and advanced tape performance in a single transport concept . . . such advantages make the M3000 the digital transport with the most to offer the system designer with a problem in the changing world of EDP.

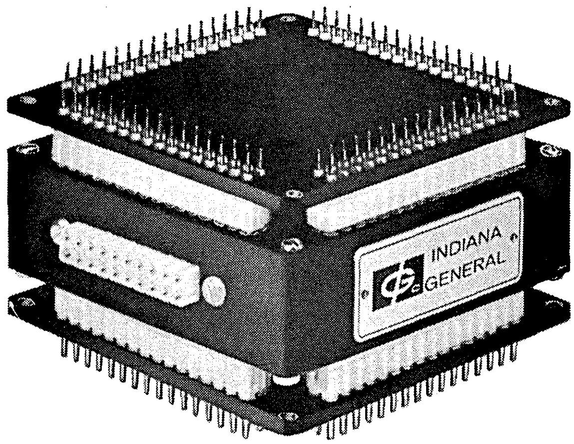
"Problem-Solving in a Changing World" *

* *"COMPUTERS '64: Problem-Solving in a Changing World," theme of the 1964 SJCC at the Sheraton Park Hotel, Washington, D. C.*
Booth 165-167

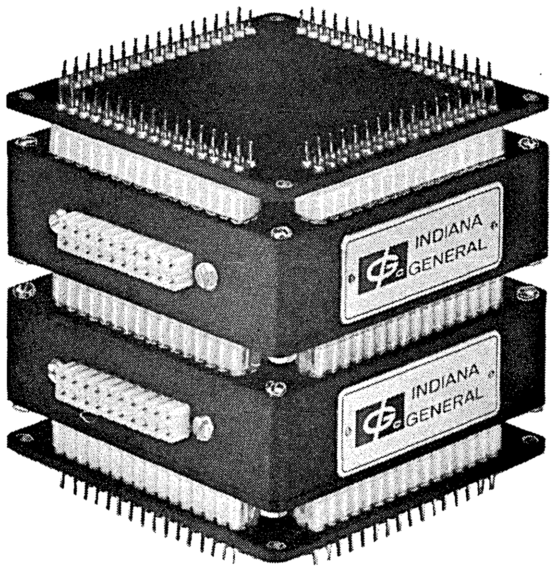


MIDWESTERN INSTRUMENTS
P. O. Box 7509 / Tulsa, Oklahoma / 74105

CIRCLE 56 ON READER CARD



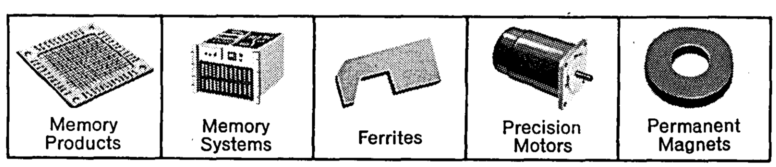
64 X 64 X 10 + 10 MINUTES



=64 X 64 X 20!

NEW, RUGGEDIZED MEMORY STACK IS EXPANDABLE. Now you can double, triple, quadruple the word length of a memory stack made from IGC's connector-type modules. Each module is a self contained array with a standard word length of 10 bits by 100, 256, 1024, 10000 or 16384 words. All leads of an individual module terminate with connectors mounted directly on the enclosure. ■ IGC's new expandable stack meets punishing environmental tests — humidity, altitude, shock and vibration — in compliance with MIL-T-5422 and MIL-E-5272. ■ Matrices strung with Ferramic® standard or wide temperature range cores for full cycle, coincident current speeds down to 600 nanoseconds. ■ Write today for complete information to: Indiana General Corporation, Electronics/Memory Products Division, Keasbey, New Jersey. 400

INDIANA GENERAL



CIRCLE 57 ON READER CARD

people IN DATAMATION

■ Anthony Debons, of the Univ. of Dayton, has been elected president of the Society for Information Display.

■ D. B. Morrissett, former director of Marketing of the IBM World Trade Corp.'s European Operation, has been appointed executive vp and member of the Board for Computer Systems Inc., Richmond, Va.

■ George Eisler, former director, Advanced Planning and Design for Scientific Data Systems, has been appointed executive vice president for that company. Peter Fenchel, previous controller of SDS, was named vp-Finance.

■ Ralph Keirstead, formerly manager of the Stanford Research Institute Computing Center is joining Control Data in Europe. He will be succeeded at SRI by Leonard Leving.

■ Dr. Maxwell C. Gilliland heads the newly-formed Computer Operations of Beckman Instruments, Richmond, Calif. With the firm since 1959, he directs research, development, and marketing of the firm's analog and hybrid computers.

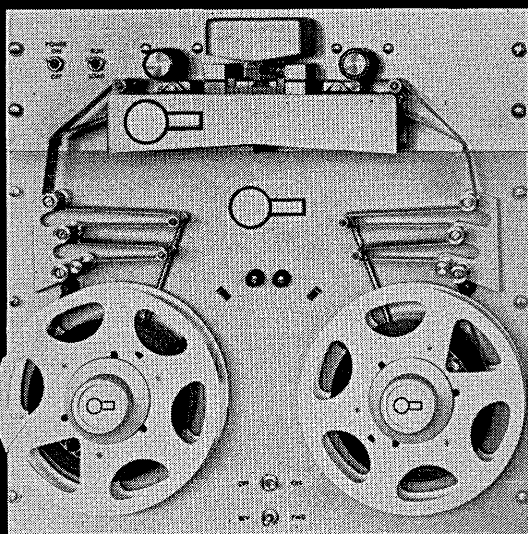
■ Abraham H. Taub has been named professor of Mathematics and director of the Computer Center at the Univ. of California in Berkeley. He was formerly head of the digital computer lab at the Univ. of Illinois. David Evans, professor of electrical engineering, who had been acting director at Berkeley in the absence of Harry Husky, has been named associate director.

■ Charles Hill has been named manager of Computer Systems at Computer Control Company's Western Div. He was formerly manager of Systems Planning for Ampex Computer Products.

■ Dr. Frederick P. Brooks Jr. has been named Advanced Systems Programming manager in the Programming Systems organization of IBM's Data Systems Div., Poughkeepsie. He will continue as IBM processor manager.

REMEX

HOW'S YOUR MTBF?*



MINE'S FINE!

In fact, it's the best! In documented customer reports we know the reliability of our tape readers and spoolers far exceeds normal standards. This is due in part to basically simple conservatively designed transistor circuitry, the use of a unique photovoltaic cell in the sensing element, a minimum number of moving parts, and rugged, precision mechanical construction.

In addition to long, trouble-free life our line of tape readers and spoolers is one of the most complete—up to 1,000 characters per second on standard models and even higher for special applications. All feature truly straight-line loading, self-adjusting brakes, and very high line-at-a-time speeds. Modular packaging of electronics provides easy field replacement to insure maximum "uptime."

Spoolers are high performance bi-directional units with constant tape tension thru spring loaded arms and the self-adjusting electric brakes.

My excellent MTBF* record should be a prime consideration in your selection of a tape reader or reader-spooler combination. You'll find a host of users who are completely satisfied, and it's easy to join this happy throng. Just ask today for our complete literature on whichever model you require.

*Mean Time Before Failure

REMEX / *Rheem Electronics*

5250 WEST EL SEGUNDO BOULEVARD
HAWTHORNE, CALIFORNIA 90251
Telephone: 213-772-5321

CIRCLE 63 ON READER CARD

MOST COMPUTING PER $

Now, from anywhere in the U. S. you can have Data-Center access to a CONTROL DATA® 3600 computer system

CONTROL DATA'S TWIN CITIES DATA CENTER NOW INCLUDES A 3600: The DATA CENTERS DIVISION of Control Data Corporation is pleased to announce the inclusion of a CONTROL DATA® 3600 Computer System in its Twin Cities Data Center. This large-scale system is now available for computation services through any of the corporation's other Data Centers, located in New York, Palo Alto, Washington D. C., Los Angeles, via data-phones communicating directly with the 3600 system in Minneapolis. For utilizing the 3600 on a one-time or regularly-scheduled basis, simply call your nearest Data Center.

The 3600 Computer System at Minneapolis places at your service a core memory of 65,536 48-bit words and 1.5 micro-second cycle time. The system employs double-precision floating point, 10 magnetic tape transports with 120 kc transfer rate and a card reading capability of 1,200 cards per minute. This service is available on a three-shift, five-day/week basis.

COMPLETE RANGE OF SYSTEMS, COMPLETE PROGRAMMING ASSISTANCE

The Minneapolis 3600, coupled with the new Dataphone communications systems, significantly extends the range of computer systems offered by the 1604A and 160A equipment installed in all five of Control Data's Centers. In each, the computers are backed by a complete programming staff, capable of efficiently solving your problems, utilizing FORTRAN 63, COBOL, CDM-3 for linear programming, SCOPE and various nuclear codes. In addition, the Minneapolis Center has a group of specialists in using the large-scale capabilities of the 3600 system. These professional services are available to assist you in all phases of problem formulation, data preparation and debugging.

Your Data Centers representative needs only 20 minutes to show how you can benefit from economical computer service. Call him now.

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295 Northern Boulevard, Great Neck, Long Island, N. Y. / 516 HN 6-2600
212 TU 6-0411

11428 Rockville Pike, Rockville, Maryland / 301 949-8800

3330 Hillview Avenue, Palo Alto, California / 415 321-8920

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DATA CENTERS
DIVISION OF
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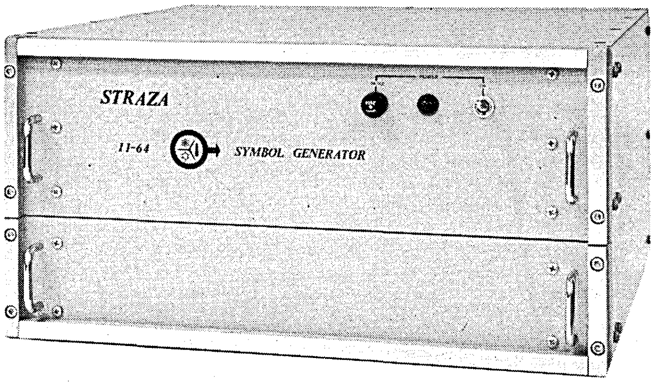
CORPORATION

CIRCLE 58 ON READER CARD

NOW...from *STRAZA*



MODEL 11-64 SYMBOL GENERATOR

more than...

100,000 CH/SEC

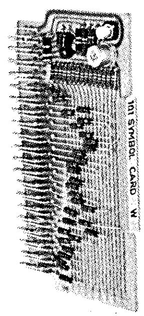
The Straza 11-64 Symbol Generator is a high speed device which accepts digital computer output and converts it to alphanumeric characters and/or symbols at speeds in excess of 100,000 CH/Sec. The Model 11-64 is ideally suited to scientific, military (Command and Control) or business applications. The standard 64-character vocabulary is easily expandable and symbols or characters are interchangeable to provide maximum flexibility, unlimited selection. The Straza 11-64 Symbol Generator is proven reliable. Actual "in-service" performance and tests indicate better than 1500 hours MTBF . . . without adjustment.

The Model 11-64 can be expanded to include a 128-symbol library by the addition of a single symbol card drawer. The additional symbol cards can also be used to increase the resolution of the symbols.

MODEL 11-64 $ 8860.00
MODEL 11-128 11400.00

outstanding features . . .

- Solid state design throughout
- Self-contained power supply
- Short-circuit-proof output stages
- Built-in selection decoder
- Plug-in symbol cards in drawers for easy replacement
- Character font and coding to your specifications



A typical plug-in symbol card (2½"x4½") Extra cards available, wired or kit form $48.00 each

IMMEDIATE DELIVERY

WRITE OR CALL TODAY FOR FULL INFORMATION

STRAZA INDUSTRIES

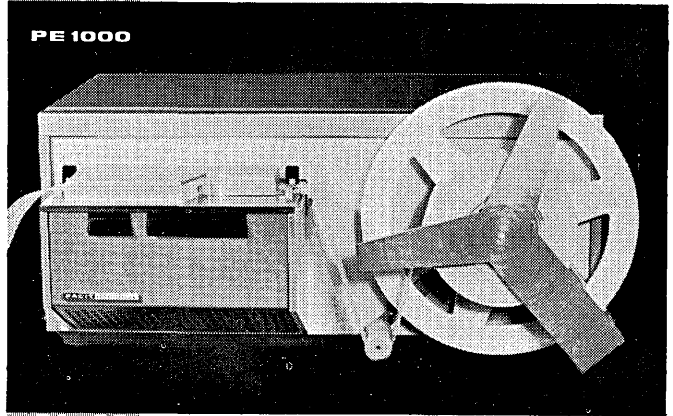
Phone 702-736-1962

164 East Sunset Rd. Las Vegas, Nev. 89109

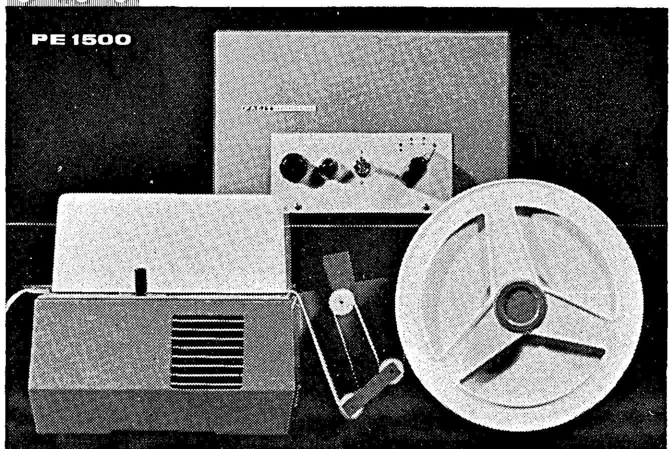
CIRCLE 66 ON READER CARD

FACIT

IN PUT



OUT PUT



Input – 1000 characters/sec.
Output – 150 characters/sec.

More and more firms are selecting Facit punched tape equipment. The computers listed below are among those serviced by Facit products.

AEI 1010 and 959	GIER	SAAB D 21
CAB 500	LGP 30	Telefunken TR 4
Facit EDB and DS 9000	ODRA 1003	Zuse Z 23, Z 25
Ferranti Mercury	RPC 4000	and Z 31

Adapters are also available for the IBM 1401 and 1440/60.

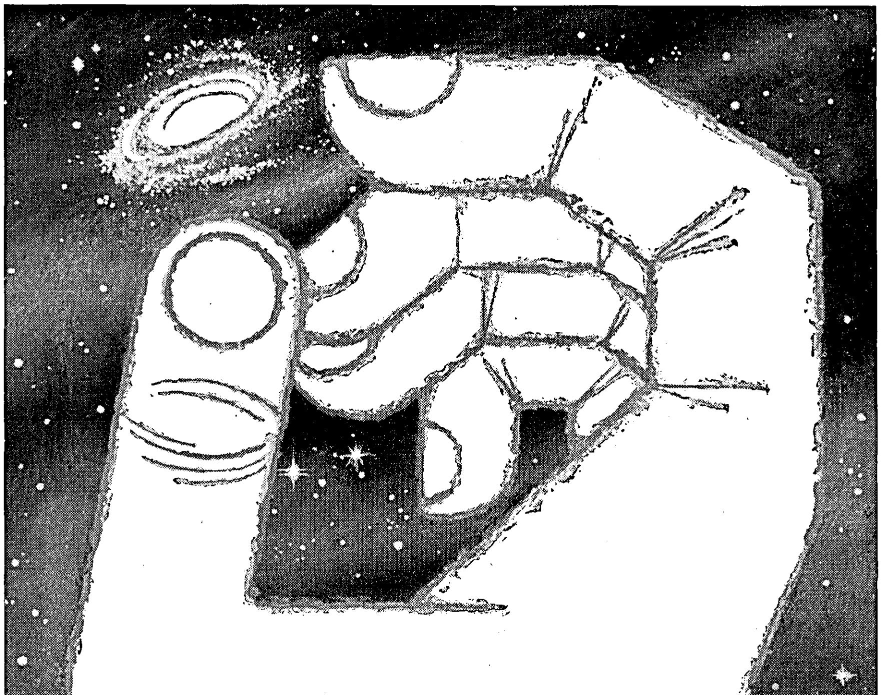
The Facit tape punch is used with most A/D converters – wherever high-speed punching is required. Punch and reader can be used in data communication systems at transmission speeds of up to 1200 baud. Versions are also available for Olivetti tapes.

Quick loading. Easy to convert for 5, 6, 7, 8 track tapes.

Manufacturer	Facit, Fack, Stockholm 7, Sweden
General agents	
Belgium	Thomson-Belge, Brussels
Finland	Finska Kabelfabriken AB, Helsinki.
France	Compagnie Française Thomson-Houston, Chatou (S & O)
Great Britain	Facit-Odhner Electronics Ltd. Rochester, Kent
Holland	Blikman & Sartorius NW, Amsterdam
Italy	Thomson-Espelettra, Milan
Japan	Kjellberg Kabushiki Kaisha, Tokyo
Jugoslavia	Commerce, Ljubljana
Norway	Kongsberg Våpenfabrikk, Kongsberg
Switzerland	Venner AG, Bern
W. Germany	Facit GmbH, Düsseldorf

Stand No. 104, 105, 106 1964, Spring Joint Computer and Exhibition, Washington, April 21, 22, 23.

CIRCLE 65 ON READER CARD



How high is your goal?

Ours are out of sight—in the labyrinth of space. But your opportunities are a tangible reality, here and now at North American's Space and Information Systems Division.

ADVANCED COMPUTING TECHNIQUES

Advanced theoretical and specialized research in computer techniques and applications. Ph.D. and MS degrees in engineering, Math or Physics with seven to ten years experience conducting complex theoretical studies and analysis in computer applications.

SIMULATION SYSTEMS

Seek specialists in integrating computers to all types of peripheral simulation equipment. Experience with complex simulation systems and visual displays with background in electrical or mechanical engineering. Also require specialists with optical physics and mathematics experience.

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To provide technical direction on programs, pre-proposal efforts and project activities in information storage and retrieval, data processing and data presentation. BS/EE, Math, Physics or Linguistics with three to ten years experience required.

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Data analysts and programmers with experience in the acquisition, processing and analysis of engineering data. Emphasis is on real-time applications with reliability and accuracy as major criteria. Data analysis experience in flight and trajectory, propulsion and vibration, and life support systems is required.

Interested? Please contact:
MR. E. D. GATELY
ENGINEERING AND SCIENTIFIC EMPLOYMENT
12214 LAKEWOOD BLVD.
DOWNEY, CALIFORNIA

All qualified applicants will receive consideration for employment without regard to race, creed, color, or national origin.

SPACE AND INFORMATION SYSTEMS DIVISION
NORTH AMERICAN AVIATION

NCR

ELECTRONIC DATA PROCESSING

sales
sales support
systems analysis
programming research
customer representation
EDP instruction

Persons who have programmed magnetic tape computer systems a minimum of two years and who have performed related systems analysis are offered an opportunity to advance in the EDP field. A high level of proficiency in the area of customer contact is essential; a college degree is desired, but not demanded. Salaries are competitive and achievement is rewarded. These professional level positions insure individual level progress with a growing Company in an expanding field.

Current opportunities exist in Dayton, Ohio, and in other key areas throughout the United States.

To investigate these opportunities, address your resume with salary requirements and telephone number to:

Mr. T. F. Wade,
Technical Placement
The National Cash Register Company
Main & K Streets
Dayton 9, Ohio

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CIRCLE 79 ON READER CARD

...but where are all the adjustment knobs?

They just aren't. Because the new 300-line-per-minute *data products* LINE/PRINTER doesn't need any adjusting. It's that simple. And that far advanced over other medium speed printers.

For example, this maximum-reliability printer has single action print hammers, electromechanically controlled (no linkages) and completely free of friction. So not only is there nothing to adjust, but there's far longer operating life with precise, constant timing no matter what the environment is.

Example. The dual tractor paper feed is controlled by a digital stepping motor for positive response to fast single space and skip operations. No clutch, no brakes — and nothing to adjust.

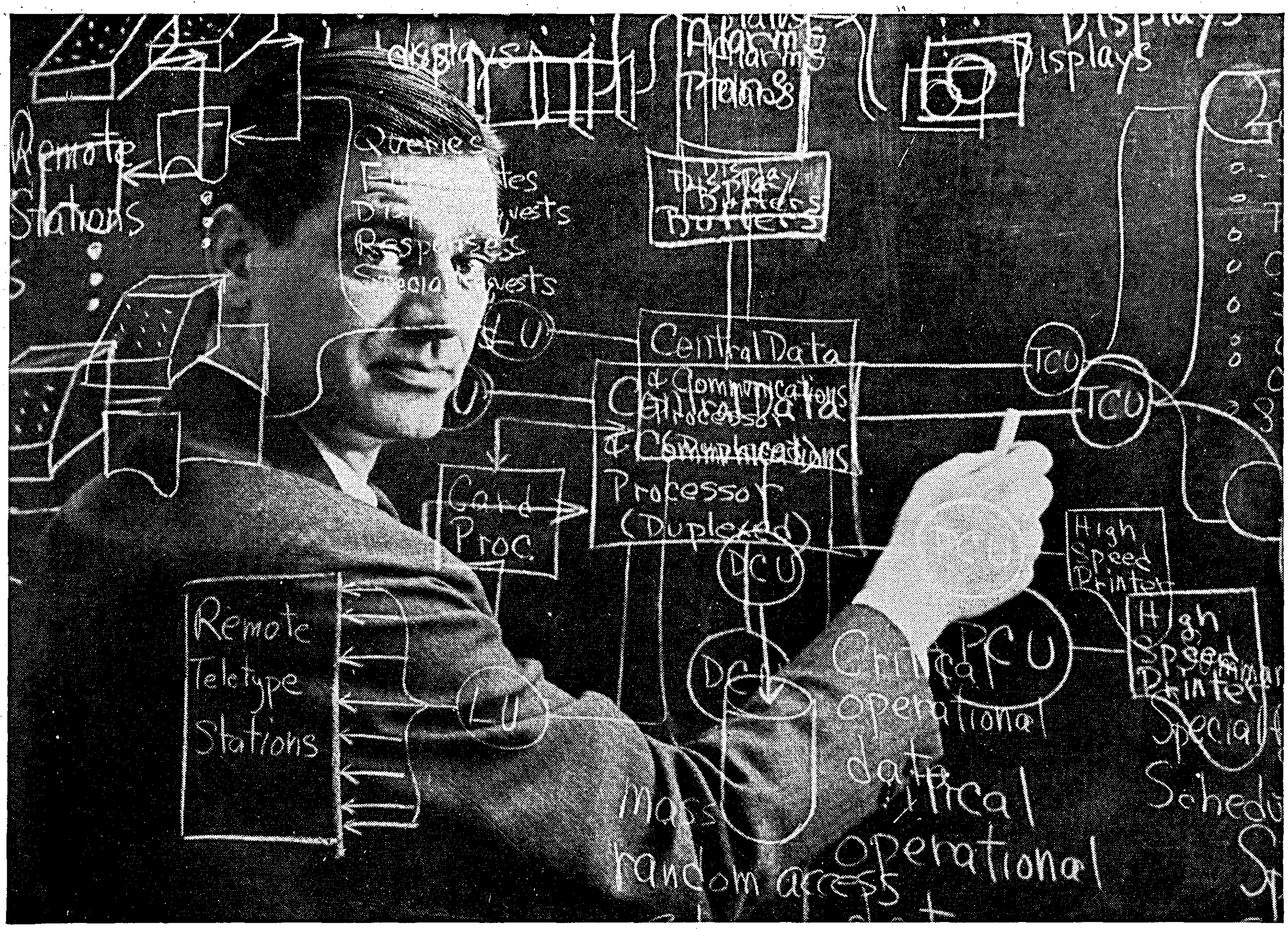
Example. Not only does this printer handle all standard form sizes, but it makes from one to six copies without any penetration or phasing adjustment.

The simple, clean operation of the LINE/PRINTER also includes many other interesting features. Like easy maintenance. And precise alignment controls for the operator. And up to 132 columns. Yet the price tag is competitive with — or lower than — even near-comparable equipment. Even the ribbon costs only a little more than $4 — and is replaceable in seconds.

We've got complete technical data on this Model dp/p-3300 and, by arrangement, a demonstration of a production unit. Contact us.

data products corporation 8535 Warner Drive/Culver City, California/Phone: 837-4491

CIRCLE 68 ON READER CARD



HAVE YOU EVER STEPPED BEHIND THE BLOCK DIAGRAM OF A TOTAL SYSTEM?

The experience can be shattering — or at least surprising for the unwary, or the superficial systems engineer. On the other hand, it can be a rich and rewarding professional experience for those who prefer to take a deeper view of systems.

Our own people tend to spend at least as much time "behind" our functional block diagrams, as in front of them. The approach is to block out the major elements of a system which will fulfill the function desired . . . then identify and isolate the salient problem areas and develop step-by-step solutions to these.

Our recent "RIPS" study illustrates the point:

ITT Data and Information Systems Division undertook a study to determine the space instrumentation requirements to support all U.S. space programs for the time period 1965-1970. Under contract to the Air Force Electronic Systems Division, the study involved the following activities:

1. Detailed analysis of over 40 space programs with a lesser analysis of an additional 100, to determine such items as tracking accuracies required, flight profiles, telemetry requirements, man control requirements, etc.

2. Since present space ranges were organized to support guided missiles and ballistic missiles, this study also produced a concept and plan for integrating these facilities into a global test environment. Control of this global test environment would be concentrated at a center equipped to support both local and global space programs. Provision for range control, test control and information flow between these ranges was included in the detailed concept.

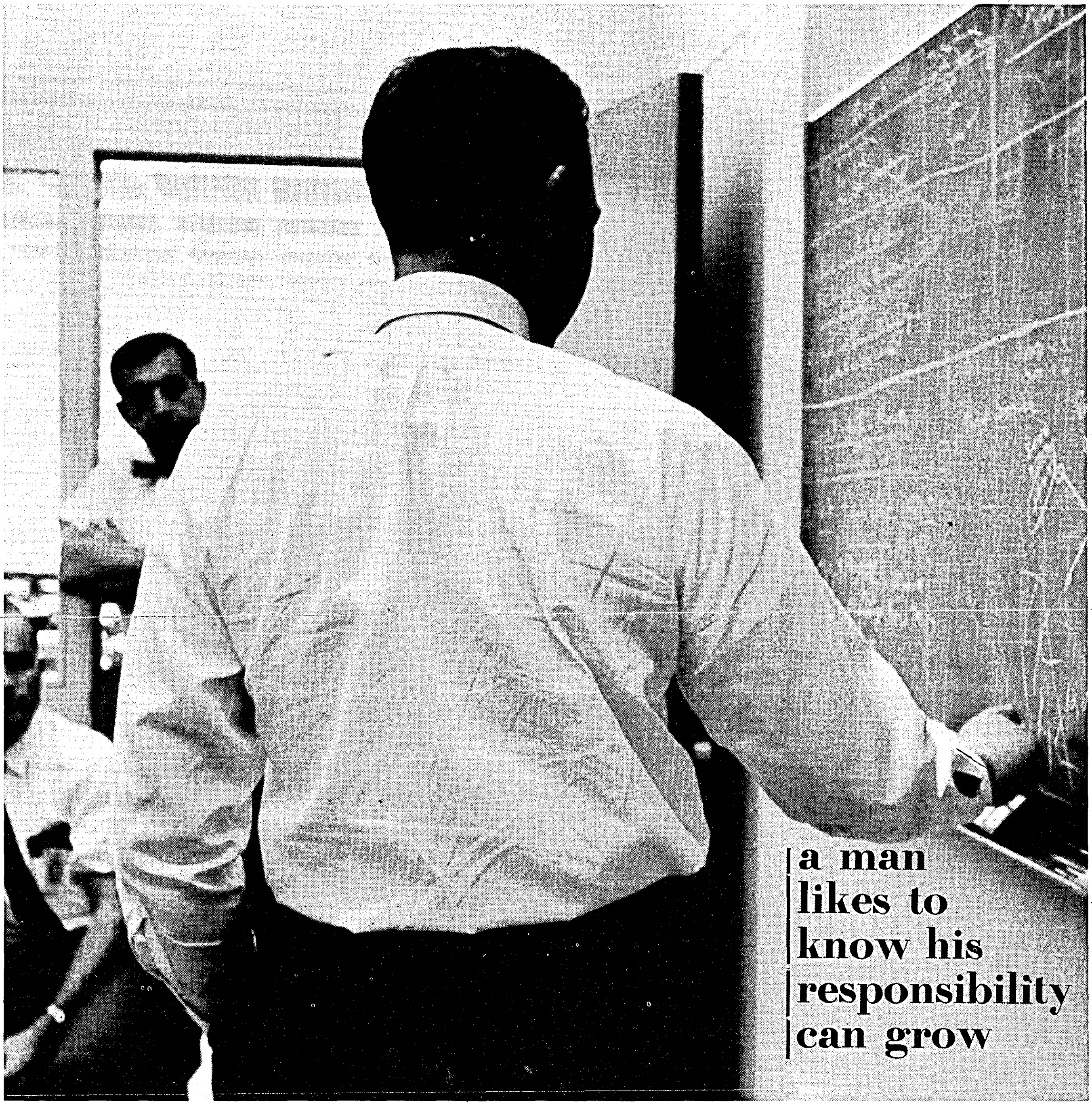
3. Extensive studies were conducted in each area of technology to determine the metric instrumentation required; the capabilities of CW and pulse sensors were investigated in depth. Source of errors including geodetic refraction, timing and others were investigated and an overall error analysis conducted. Timing extensions to provide the accuracies required throughout the globe were also investigated. Calibration techniques using satellites for global calibration of RF and optical instrumentation were explored and suitable recommendations made. The processing, communication and display of information were thoroughly investigated. Planned facilities were mapped out against existing facilities to note deficiencies. Siting facilities were explored and recommendations for their use were made.

4. An analysis was conducted to determine the requirements for new sites to support global missions. Profiles and typical satellite orbits were prepared to determine pass-time capabilities of these stations and to highlight deficiencies in the present systems.

Actually, RIPS represents a relatively small proportion of our total systems activities. When you're ready to explore the opportunity side of DISD, you'll discover a great deal more. A good first step would be to write in confidence to Mr. E. A. Smith, Manager of Employment, Div. 35-MD, ITT Data and Information Systems Division, Route 17 and Garden State Parkway, Paramus, New Jersey. (An Equal Opportunity Employer)

ITT DATA AND INFORMATION SYSTEMS DIVISION

CIRCLE 84 ON READER CARD



Like most of us, you've probably asked yourself at least once in your career, "Where do I go from here?" And quite possibly you changed jobs to answer that question only to come up against blind alleys or blocked avenues of advancement. Collins offers you an opportunity to go just as far as your ability, your initiative, your willingness to handle responsibility can carry you.

Collins is a growth company. The scope of our work in such diverse fields as Space Communication, Data Processing, Avionics, Microwave, Antenna Systems and HF, VHF and UHF Communication, to mention a few, attests to that fact. The continuing growth of our engineering and scientific staff is further proof. The expansion of our Cedar Rapids, Dallas and Newport Beach facilities offers still more. With company growth, expansion of product lines, with development of new products comes the opportunity for your own growth into areas of ever increasing responsibility, as well as financial and material rewards.

If you are a man who knows that growth and responsibility come from individual effort, if you are a man who puts all his creativity, talent and initiative into a project, if you like to know that your efforts will be rewarded with ever increasing responsibility, we'd like to talk with you. Write our manager of professional employment, Dept. 110,

COLLINS RADIO COMPANY
Cedar Rapids, Iowa • Dallas, Texas
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COLLINS

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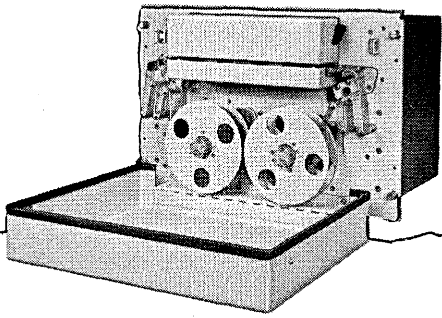
Cook LEADS THE FIELD IN mil spec punched tape readers



Cook supplies punched tape readers for these and other military programs: Polaris . . . Pershing . . . Mauler . . . Titan . . . Minuteman . . . Atlas . . . Athena . . . GPATS . . . F-111.

Now, to satisfy

MIL-T-21200 D CLASS II

Cook announces a new family of punched tape readers with these outstanding capabilities:

- Linear reel servo systems.
- Designed for Mean Time to Failure greater than 2500 hours.
- Modular construction and wire harnessing.
- Alternate tape speeds and logic levels available upon request.

SPECIFICATIONS

	MODEL 111	MODEL 112	MODEL 113
TAPE SPEED	400 char./sec. bi-directional	400 char./sec. bi-directional	200 char./sec. bi-directional 800 char./sec. rewind
STEPPING	Any rate up to the slew speed		
TAPE	Standard 1" wide; eight (8) level code		
REEL CAPACITY	500 feet of 3.0 mil mylar tape	500 feet of 3.0 mil mylar tape	800 feet of 3.0 mil mylar tape
POWER REQUIREMENTS:	115 VAC, 400 cps, 3 ∅	115 VAC, 50-60 cps, 1 ∅	115 VAC, 400 cps, 1 ∅
SIZE:			
Height	12.25"	12.25"	15.75"
Width	19"	19"	19"
Depth behind front panel	10"	10"	12"
Depth in front of panel	3"	3"	3"
LOGIC SIGNALS	Logic "1" +12 vdc Logic "0" 0 vdc		

For further information regarding these products, please contact:

COOK ELECTRIC COMPANY
DATA-STOR DIVISION

See us at the SJCC,
April 21 to 23, 1964.

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CIRCLE 69 ON READER CARD

Wind he's got plenty of...

Do you?

You should.

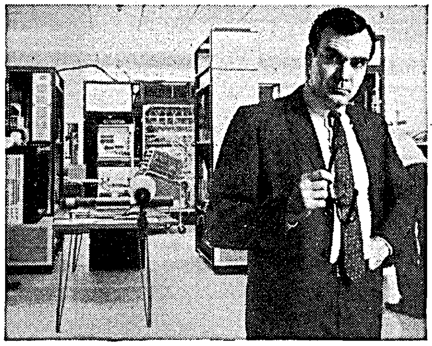
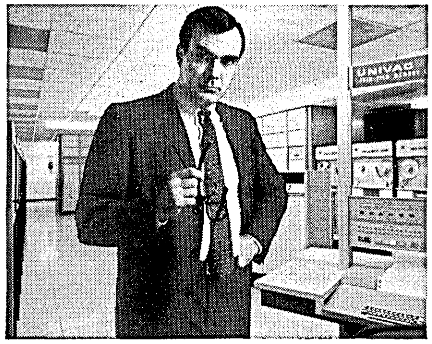
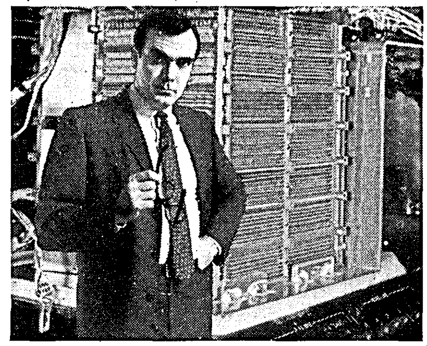
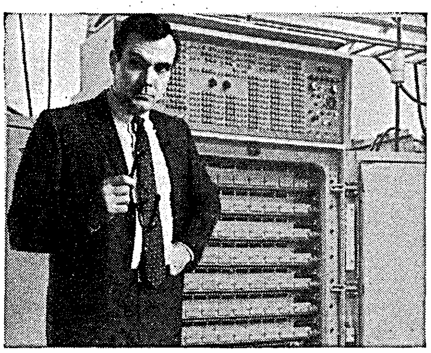
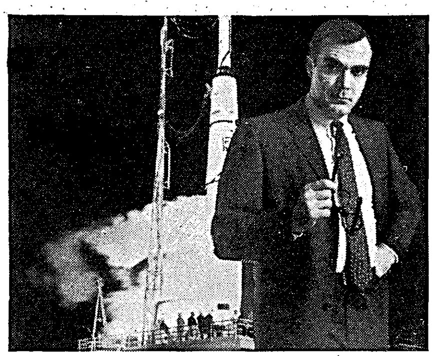
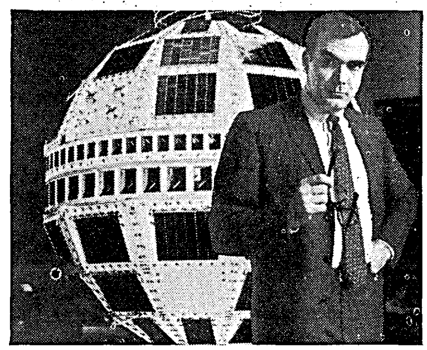
It's important to keep on breathing.

After all, you're a candidate too. For health. For a reasonably long life.

If you're short of breath . . . if you cough too much . . . you may find it tough to win. Don't take chances with these symptoms of respiratory disease.

Take good care of your wind; you'll need it as long as you live. This is the recommendation of your local Christmas Seal organization and the National Tuberculosis Association.

Short of breath?
Cough too much?
Don't take chances.
See your doctor.

AT UNIVAC NO PROGRAMMER IS TYPECAST

He can't be. There are too many diverse contracts in the house to permit stagnation to exist.

Here at UNIVAC-Twin Cities men can move around all over the programming map. For example: into Phase III of Nike work, onto real-time software systems relating to aircraft and missile tracking, into target discrimination, intercept programming, missile guidance, command and control systems, simulation preliminary to hardware design, missile and aircraft flight and computer simulation for design evaluation. Much of this work involves multi-processors. The areas of mechanized design and compilers and language processors are receiving special attention.

The professional environment is complete in every respect. Systems programmers work on their own machines. Development engineers have their own. Software men have a chance to see that hardware design limitations are corrected. Creative interplay between hardware and software R & D activities is a matter of course. The technical content of the work borders on the outer limits of today's knowledge of computer technology. And, programmers can move around geographically as well as professionally.

All in all, UNIVAC-Twin Cities probably ranks as unequalled in industry for its all around environment for the programmer.

PROGRAMMING SUPERVISORS To plan, organize and supervise programming projects, formulate techniques and procedures of programming systems. BS or MS in Math or Science with various combinations of experience in the display engineering activities and 5-10 years' experience.

APPLICATIONS PROGRAMMERS To define, analyze and design solutions to problems, and translate methods developed into computer techniques. BS or MS in Math or Engineering with 3-5 years' large-scale data processing applications experience.

COMMAND AND CONTROL PROGRAMMERS To design real-time information retrieval computer program for AF Intelligence and Command Control Computer Systems. Requires BS in Math, or Science with 3-5 years' sound programming experience.

INTEGRATED PROGRAMMING SYSTEMS Requires BS or MS in Math, Statistics or EE and 2-4 years' experience in programming large-scale digital computers. Must know generative and operational elements and be familiar with auxiliary memory devices.

SYSTEMS PROGRAMMERS To develop large-scale software packages. Requires BS in Math and 2 years' experience in digital computer programming including symbol manipulation, input-output or basic utility routines.

RADAR SYSTEMS PROGRAMMERS BS or MS in Math or Engineering with 2-5 years' experience in systems checkout, radar control, I/O routines, simulation, dynamic radar tests, or executive control to work on advanced real-time systems.

LIBRARY SYSTEMS PROGRAMMERS BS in Math or Science and 2 or more years' experience in assembler-compiler development, simulators (computers, radar/missile), range safety, input/output, mathematical subroutines, or executive control systems.

For more information about these or other openings, or to apply, send your resume to Mr. R. K. Patterson, Employment Mgr., Dept. D-12, Univac Division of Sperry Rand Corp., Univac Park, St. Paul 16, Minn. An Equal Opportunity Employer.

UNIVAC

DIVISION OF SPERRY RAND CORPORATION

DATA PROCESSING MANAGEMENT

As the rapidly expanding world leader of a dynamic consumer goods industry, our new 1401/1410 installation requires senior, highly skilled business applications computer specialists. Successful applicants probably now hold—or are in line for—position of data processing manager . . . or they're supervising an E.A.M. and computer operation.

With us, these senior specialists and managers will be able to apply their intimate knowledge of systems and programming development techniques to a variety of applications ranging from automated purchasing and material control to establishing company policy with statistical projection of sales and quotas. And lots more we haven't even thought of yet.

Since we're a growth company and on the move (sales have about doubled in the past two years) we need vital, aggressive people who have a BS, BA or preferably MBA and from 5-10 years experience. In return, we offer a range of excellent starting salaries, profit sharing, bonuses and a dynamic working environment that will allow you to do computer applications you've always dreamed of.

For those of you attending the EJCC, we'll be doing LOCAL INTERVIEWING April 21-23. Call, in complete confidence, Bill Speich at **ME 8-3900.** Or send your resume and salary requirements, again in complete confidence, to:

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WHAT IS YOUR TRUE WORTH?

You'll never know unless you contact the nation's largest data processing placement service.
Cadillac Associates represents all of the country's leading data processing companies. We presently have over 900 positions coast to coast that should be filled immediately.
With Cadillac, you are represented by men conversant in your discipline. And remember, our placement service is yours in ABSOLUTE CONFIDENCE, WITHOUT OBLIGATION AND FREE OF CHARGE. Client companies pay all costs.

EDP SYSTEMS ANALYSTS $9-14,000
1401 and sub-units. Commercial.
PROGRAMMERS $7-12,000
1401/1410. Commercial.
SOFTWARE DEVELOPMENT $10-16,000
Languages, sub-routines, etc.
SR. PROGRAMMERS $9-15,000
Scientific applications.
PROGRAMMING INSTRUCTORS $12,000
1400-7000 Series. URGENT.
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Analyze sys. in expmtl. prgms.
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LIBRARY SYSTEMS PROGRAMMERS $14,000
Math sub-routines, simulators.
DATA PROCESSING SPECIALIST ....to $18,000
Data reduction, software development.
SCIENTIFIC COMPUTATION ....to $16,000
Analysis—IBM 7090.
JUNIOR PROGRAMMERS $6-9,000
1401. 1-2 yrs. exp.
SYSTEMS/PROGRAMMERS ....to $13,000
Analog simulation on digital equip.

May we help you in absolute confidence and without obligation? For further information on the above or other positions, send us a short resume of your background.

Lon D. Barton, President

CADILLAC ASSOCIATES, INC.
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"Where More Executives Find Their Positions Than Anywhere Else in the World."

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Data Systems Opportunities

COLLEGE DEGREE REQUIRED

—Programming—

Large-scale data handling and computing problems. Extensive and diversified facilities and applications.

—Advanced Systems Analysis—

Software Research and Design: Theoretical structure of programming languages, compilers and executive programs. Often emphasizes the higher mathematics of computation.

—Information Retrieval—

Problem-oriented research and applications: Emphasis on large quantities of data, speed, and utility. Some problems unique.

Starting salaries range from $6770-$15,665 depending on individual's education level and experience. NSA has been established outside the competitive Civil Service System but the liberal benefits associated with Federal Employment are available to all Agency personnel. Applicants must be U.S. Citizens, are subject to a character and loyalty investigation.

MAIL FEDERAL APPLICATION FORM (SF-57) TO:

NATIONAL SECURITY AGENCY

Fort George G. Meade, Maryland ATTN: M342-A

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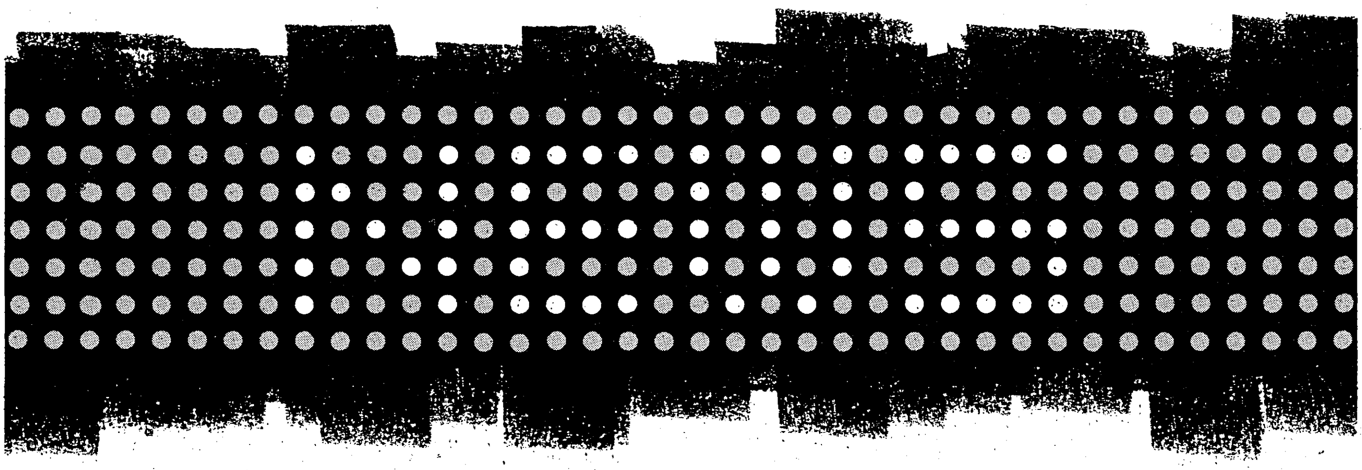
have you heard the



from General Electric?

Understandable if you haven't. News of the fifth and smallest member of the Compatible GE 400 family was just released.

What's news about the GE-415? Briefly, it is the first optional program compatibility unit available in industry: it permits more flexibility; it uses a CAPACITRIX (fixed memory) with permanently stored simulator; it allows a high degree of input-output simultaneity. Its upwards compatibility with its other 4 brothers permits users to move up the scale to larger systems without changing their programs. And . . . there are plenty of users who've outgrown their present systems capabilities.

Engineers and programmers at GE are "outgrowing" their own computer systems. Larger technical contributions are already *at* the corner, One— a new, large-scale, scientific computer system, is of such technical stature we dont' even mind hauling out that time-worn cliche: "it's going to stretch the state-of-the-art."

Our marketing function is outgrowing itself too— today there are 35 sales offices blanketing the country, half of which opened only last year.

Positions now open require BS or MS degree, plus 2 to 3 years' experience in computer field:

ENGINEERING ***OPENINGS in Phoenix, Arizona***

Logic Engineers: Generate logic schematics and other documentation on digital equipment; evaluate operation of equipment, reconcile inconsistencies between design and specifications.

Systems Engineers: Technical leadership qualities essential for development of systems specifications and operating definitions. To assume total responsibility for integration of computer systems design, including synthesis, analysis, applications and reliability.

Diagnostic Programmers: Collaborate with systems engineers on generating programs to test functional operation of large scale digital computer system. Groups of programs to be developed to fully exercise hardware and systems components. Objective: to diagnose 99% of component failures.

Mechanical Engineers: Technical emphasis on mechanisms and mechanical assembly D&D for peripheral equipment. Must have competence in mechanisms, properties of materials, methods of metal and plastic parts fabrication and tool design. Will evaluate and integrate input/output equipment into computer system.

MARKETING ***Opportunities throughout the U.S.***

Sales Representatives (Business & Scientific) Responsible for customer contact and presentation, sales proposals. Will advise and work with applications engineering and product planning staff.

Applications Consultants (Business and Scientific) For pre-and-post sales systems studies; programming instruction and systems analysis.

PROGRAMMERS ***Openings in Phoenix, Arizona***

Applied Research: Programming for diversity of projects encompassing independent machine translation, 1 pass Fortran, D&D of macro-assemblers, report and sort/merge generators, simulations, input/output and operating systems.

Marketing: Programmers to develop benchmark and demonstration programs; develop package programs, e.g. resource allocations, forecasting, transportation problems, linear programming.

Write in strict confidence, including background experience and salary requirements, to: Mr. J. E. Torrey, Computer Department, General Electric Co., Room 56-D, P.O. Drawer 270, Phoenix, Arizona.

GENERAL ELECTRIC

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CIRCLE 91 ON READER CARD

Continued from page 21 . . .

favorable to arguments raised by bill proponents, and somewhat hostile to the banking representatives who were charged on several occasions with evading the intent of Congress in their interpretation of laws now on the books.

No further hearings on the Multer bill have been scheduled.

AUTODIN UPDATING DRAWS 8 BIDDERS

The Defense Dept. has received responses from eight companies for Phase I of its projected "updating," involving creation of 10 overseas message switching centers for the Defense Communication Agency. Successful bidder will supply all computing equipment, a blockbuster job with a price tag in the $20 million-plus area. DCA, not Western Union, will make final selection, though it will still lean heavily on WU's advice. RCA supplied the computers for Autodin's five domestic switching centers, but the spring book touts no favorites.

LATEST REPORT FROM THE POVERTY FRONT

President Johnson, waging war on poverty, has sent to Congress a draft of proposed legislation to create a National Commission on Automation and Technological Progress, composed of 14 members drawn from outside the Government. The proposal, introduced in both houses, is the most recent of a bevy of proposed bills to create commissions, panels etc., to deal with automation-induced unemployment (see Feb., p. 21). Backed by presidential prestige, it's considered the most likely to emerge eventually from the legislative process.

The president's draft legislation was accompanied to the halls of Congress by his second annual Manpower Report which documents in detail the condition of the nation's working force. The report noted that the proportion of manufacturers' capital spending allocated to automation machinery and equipment rose from 12% in 1959 to 18% in 1962, with the amount going still higher in '63.

DOD CLOSES BOOKS ON $200 MILLION PURCHASE

The DOD has closed out the books on its gargantuan $200 million purchase of computers formerly on lease. A complete purchase list hasn't yet been made public, but it's claimed by a DOD spokesman that no installation with a pay-off greater than 42 months was included.Completion of the DOD program brings its ratio of computers owned to all computers to 36%, which compares favorably with the 29% figure for non-DOD government agencies. "For future computer acquisitions," said the spokesman,"we'll use the same criteria -- proximity of pay-off date and system stability -- to determine whether we'll lease or buy."

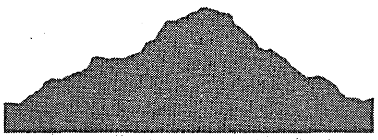
BUREAU TIME GOES A-BEGGIN'

Scads of time remain available on the Bureau of Standards 7094/1410. The system is being operated about a shift and a quarter, the computing load divided about 50-50 between BuSt work and outside clients -- roughly unchanged since announcement of the service bureau experiment. Why the lag? "Having one's own computer is something of a status symbol with most government agencies," one observer noted. "They don't like to go to another agency with computing problems."

ADVERTISERS' INDEX

THE BUNKER-RAMO
SEARCH FOR COMPUTER TALENT

FIELD DATA SYSTEM DESIGN

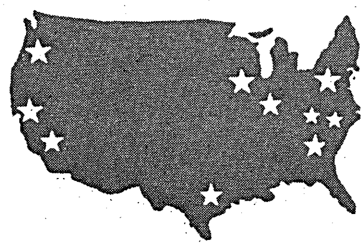


IN THE COOL HIGHLANDS OF SOUTHERN ARIZONA an elite technical team of government and industry specialists is at work applying automatic data processing concepts, techniques and equipment to the needs of the mobile modern Field Army. This program, now beginning its sixth year, is a vital part of the Army's Command Control Information System Project for the 1970's — CCIS-70.

We have been selected to continue in its role of providing technical assistance to the U.S. Army Materiel Command in support of the CCIS-70 Project at Fort Huachuca, Arizona. Challenging assignments exist in advanced areas such as digital data communications, systems integration, man-machine communications, information retrieval and display, programming techniques and languages, simulation techniques and applications, and integrated system testing under field conditions. Facilities include van-mounted computers developed by the Army for field use, associated system devices, and field communications equipment. We have immediate openings for qualified systems analysts, programmers and test engineers who desire to make a significant contribution to the nation's military capabilities in a stimulating professional environment.

At Historic Fort Huachuca and neighboring Sierra Vista, civilian engineers and their families, along with hand-picked Army technical officers and their families, have created an equally stimulating intellectual and social environment. If you would like to join our top-flight technical group at Sierra Vista, contact us now.

INDUSTRIAL PROCESS CONTROL SYSTEMS



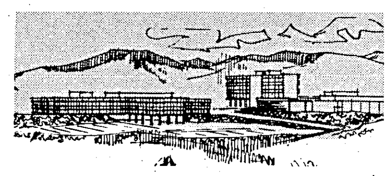
The Bunker-Ramo Corporation is the world leader in applying control computer systems to industrial processes. Growing demands for these systems in the petroleum, chemical, paper, steel, electric utility, and other industries have created openings for qualified people in the following areas:

- **Real-Time Programming**
- **Systems and Process Analysis**
- **Control Systems Engineering**
- **Applications Engineering**
- **Sales Engineering**

at the following locations:

☆Atlanta, Georgia
☆Canoga Park, California
☆San Francisco, California
☆Chicago, Illinois
☆Cleveland, Ohio
☆Pittsburgh, Pennsylvania
☆Philadelphia, Pennsylvania
☆Houston, Texas
☆New York, New York
☆Seattle, Washington

COMPUTER SYSTEMS DESIGN



PROJECT MANAGERS

Challenging project responsibility encompassing development of computer hardware systems for design through delivery. Absolute requirements include BSEE degree and 8 to 12 years' experience with computer systems design or development.

VALUE ENGINEERS

Recent implementation of a Value Engineering program has created immediate needs for value engineers heavily experienced in computer design, with at least 2 years in the field of value engineering and analysis on digital computers main frame and equipment. Successful applicants must demonstrate a capability to set up and perform the engineering analysis program.

SENIOR LOGIC DESIGN ENGINEERS

To provide in-house consulting for advanced computer system planning. Will perform system and logic design inputs to technique development efforts in area of circuit and memory development. Requires BSEE and 5 to 10 years' in circuit and/or logical design of digital computer equipment.

A jointly owned company of Thompson Ramo Wooldridge Inc., and Martin Marietta Corporation, including the former TRW Computer Division.

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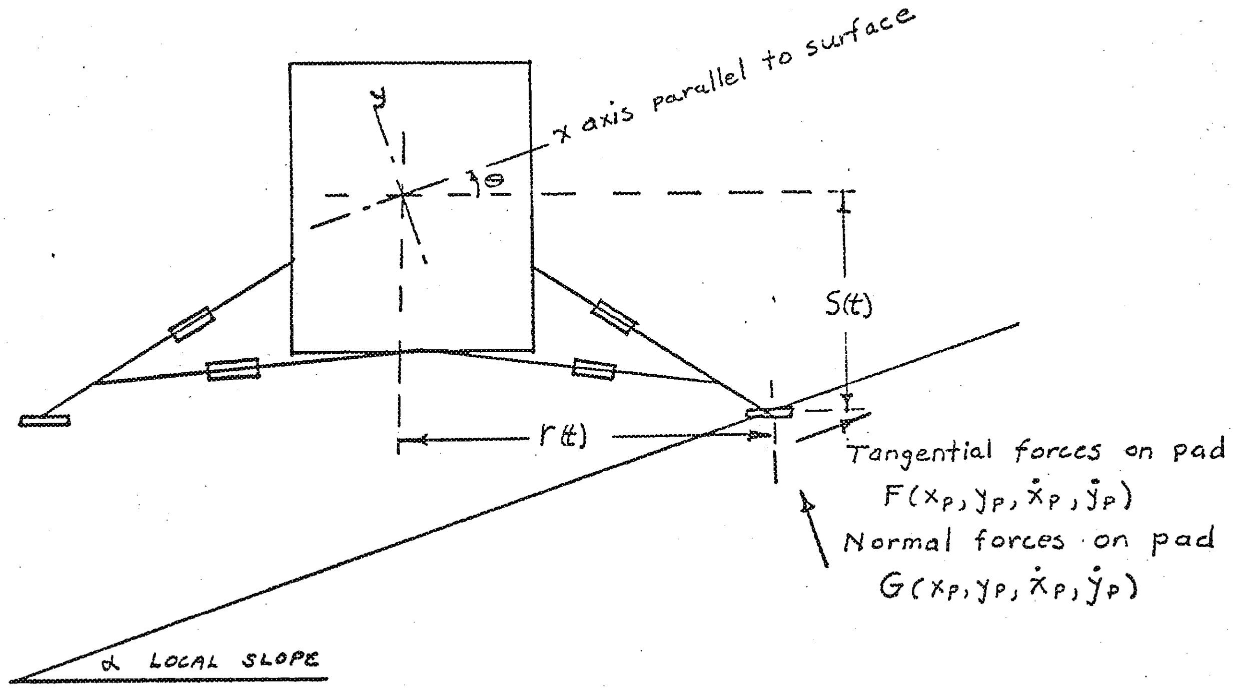


Equations of motion after first impact: Sliding and rotating

$$m\ddot{x} = -mg_M \sin\alpha + F(x_P, y_P, \dot{x}_P, \dot{y}_P)$$

$$m\ddot{y} = -mg_M \cos\alpha + G(x_P, y_P, \dot{x}_P, \dot{y}_P)$$

$$mk^2\ddot{\theta} = F(\quad)[r(t)\sin\theta + S(t)\cos\theta] + G(\quad)[r(t)\cos\theta - S(t)\sin\theta]$$

How do we model F( ) and G( ) for porous, sponge-like surfaces, e.g. as suggested by the "fairy-castle" theory of lunar soils? How will these surface models affect landing dynamics analyses? How can we investigate non-planar landings?

OTHER PROBLEMS FACING BELLCOMM:

- The effect of meteoric infall on lunar surface roughness.
- The relationship of crew performance to habitability, confinement and work-rest cycles.
- Determination of the cooperative roles of the vehicle G and N Systems and earth-based systems in dealing with the total guidance problem.

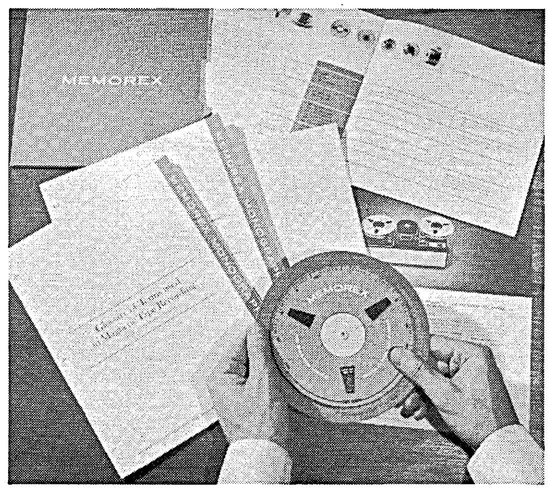
Bellcomm is doing systems engineering on Project Apollo for Headquarters, Manned Space Flight, National Aeronautics and Space Administration. If Bellcomm's problems interest you, address your résumé to Mr. W. W. Braunwarth, Personnel Director, Bellcomm, Inc., Room 1200E, 1100 17th St., N.W., Washington, D.C. 20036. Bellcomm is an equal opportunity employer.

BELLCOMM, INC.
A Bell Telephone System Company

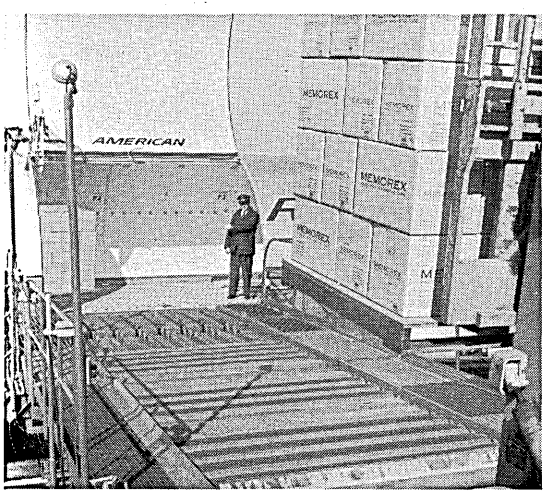
4 REASONS WHY MEMOREX LEADS IN COMPUTER TAPE

(And what it means to you!)

Premium Quality Ask the most demanding computer centers whose tape is used for their ultra-critical applications. You'll find a multi-million dollar vote of confidence placed in the integrity of Memorex products—the result of uncompromised and unvarying product superiority. With Memorex magnetic tape you always benefit from measurably longer tape life, freedom from rejects, greater reliability. (Photo courtesy of Stanford University Computer Center)



Extra Technical Support Authoritative technical backing is the hallmark of Memorex marketing. Manufacturing engineers and tape specialists with experience born of years solving digital recording problems offer help for the asking. Other aids to users include the Memorex Monograph series of informative literature; the Memorex tape slide rule; and technical liaison, of course. Next time you face recording problems, call Memorex!

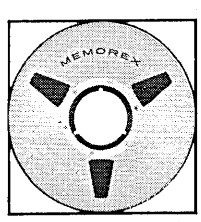


Added Service Close attention to a customer's needs is the rule at Memorex. But not all are technical. It is important to have the right product at the right time and in the right condition. To assure timely delivery and extra care in transportation, Memorex routinely ships via air carrier at no extra cost. What is more, specially designed containers and material handling methods keep tape error-free and pre-test perfect throughout shipment.

Continued Research Memorex Computer Tape is scientifically designed (not the result of cut-and-try methods) to meet highest standards of consistency and reliability. Intensive research in oxides, binders, and process innovations assures continued quality advances. Some results are subtle (an increase in coating durability); some are obvious (the super-smooth surface). But all improvements pay dividends in better performance to Memorex tape users.

Memorex tape is premium tape. No need to pre-check it. You can place Memorex computer tape directly in service—reel after reel.

Memorex certification means what it says: Memorex computer tape is error-free. Extra care, extra steps and scrupulous attention to every detail make it that way. We know the importance to you of having a tape you can depend on.



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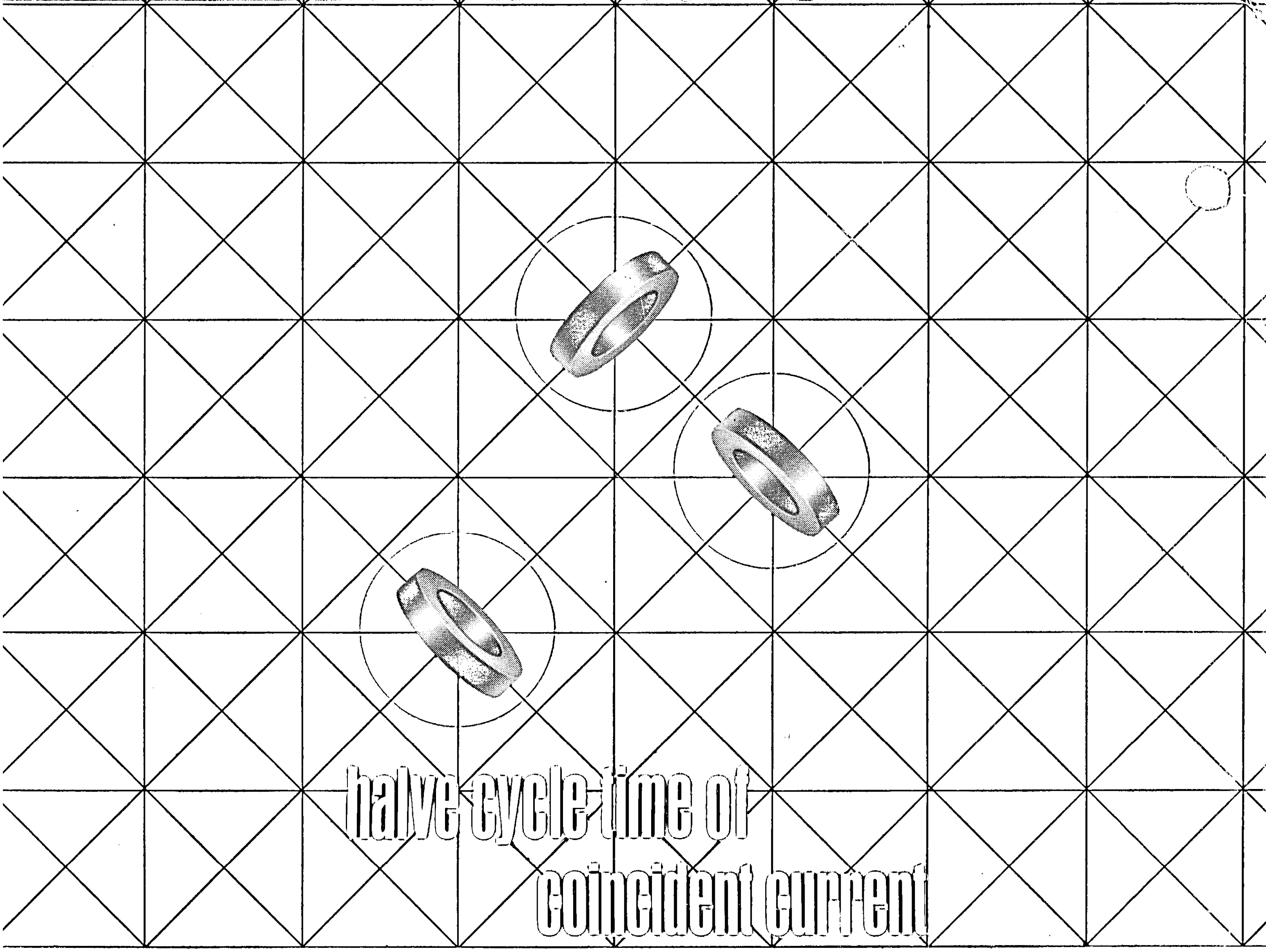
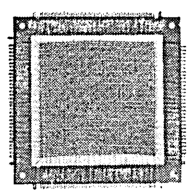
MEMOREX

PRECISION MAGNETIC TAPE

CIRCLE 2 ON READER CARD



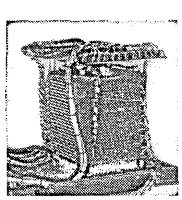
halve cycle time of coincident current core memories



. . . with a new Ferroxcube 20 mil ferrite memory core. Switches in 185 nanoseconds. Available in planes and stacks of all sizes.

☐ Compare squareness, usable drive current requirements (800 in a full select), and wide operating margins to any stack on the market. You'll find Ferroxcube tops them all. And that's not all—these stacks are wired on spacings of 25 mils. This means lowest impedance and shorter line lengths.

☐ These rugged new stacks meet exacting quality standards . . . standards possible because Ferroxcube builds "from the core formulation up."



☐ For fast 1 usec memory cycle times and expert application assistance—call or write Ferroxcube 914-246-2811.

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CIRCLE 3 ON READER CARD