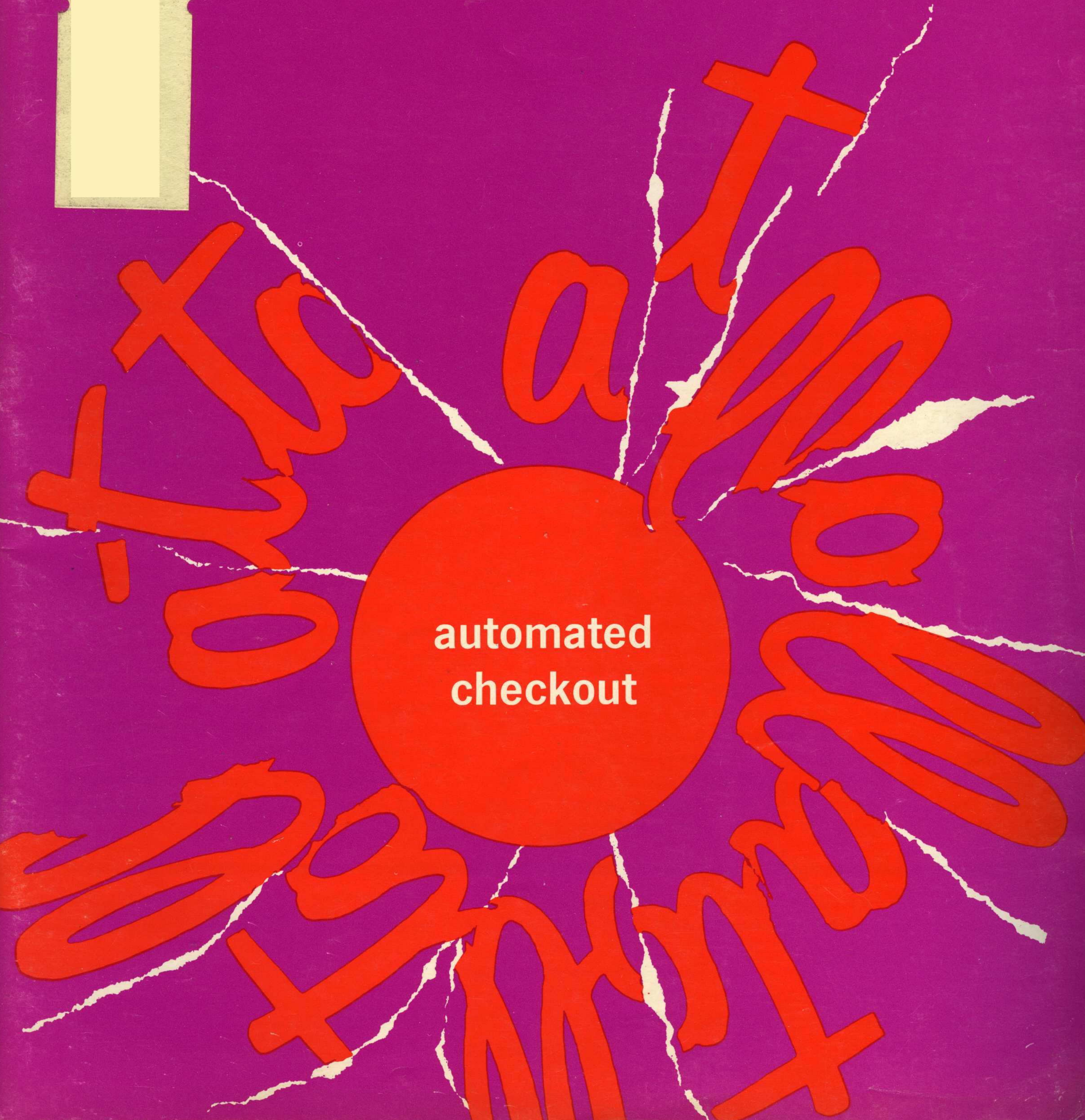
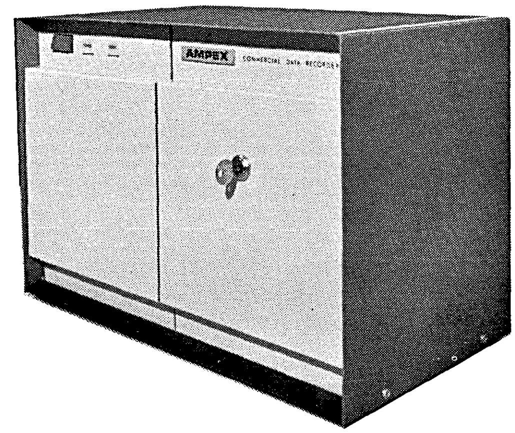
DATAMATION® 65

April



This simple little box



can make a very big improvement in the system you're planning.

If you are a system designer, and if you are planning a process control system, machine tool control, commercial data acquisition, computer input/output, business system, banking system or just about any system for industry—read how the new Ampex incremental Commercial Data Recorder can give you a lot more capability, for a lot less money, than anything else in its field.

Greater capability, lower cost. What makes the new Ampex CDR-1 so much better? It's a magnetic tape recorder. For the first time, designers and manufacturers of systems that use other input/output devices can enjoy **all** the inherent advantages of magnetic tape. The CDR-1 records up to 2400 bits of information per second—incrementally, from random or continuous sources. It plays back up to 3840 bits per second at rates that can be varied to match the input requirements of transmission lines, computers or readout devices. The CDR-1 automatically verifies each bit of data as soon as it is recorded: errors are fewer than 1 in 10,000,000. One small CDR-1 tape cartridge stores as much data as 7000 feet of punched paper. And it can be erased and used again. With all these advantages, over-all operating costs of the CDR-1 are bound to be lower than present systems. With all these advantages, initial cost is competitive—right down to the penny—with most paper tape systems.

Designed to meet a wide range of applications. The CDR-1 can be interfaced with many different types of data transmission control and computer equipment.

Literally fool-proof. Operating the CDR-1 is as simple as slipping the magnetic tape cartridge into a slot. There's no threading, no rewinding. And the cartridge keeps data from being damaged. These are important benefits when it comes to selling your system.

Yours for the asking. Detailed engineering specifications, brochure, or a demonstration of the CDR-1 are yours for the asking. Just send us the coupon.

☐ Please send me brochure and specs of the new CDR-1.
☐ I would like to arrange for a demonstration.

Ampex Corporation
401 Broadway
Redwood City, Calif.

AMPEX

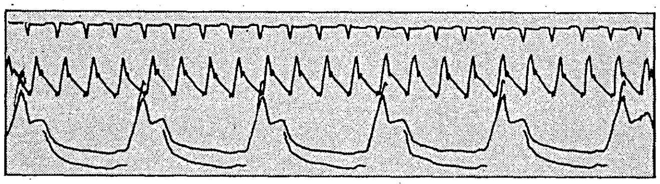
NAME ______________________ COMPANY ______________________

ADDRESS ______________________ CITY ______________________ STATE ______________________

CIRCLE 1 ON READER CARD

DO YOU HAVE A **SIGNAL PROCESSING** PROBLEM? **AMBILOG 200** IS DESIGNED TO SOLVE IT!

Using the best of both analog and digital techniques, the AMBILOG 200™ Stored Program Signal Processor is designed from the ground up to handle the "floods of data" generated in test and research programs. Although such programs cover many fields — biomedical monitoring, geophysical research, test stand instrumentation, automatic weapons checkout, speech analysis — all require complex *signal processing:* multiple input acquisition and output distribution, monitoring, editing, arithmetic, analysis, recording and display. Because of its high processing speed and extensive input/output for both analog *and* digital data, AMBILOG 200 is ideally suited for such tasks. Here are some examples.



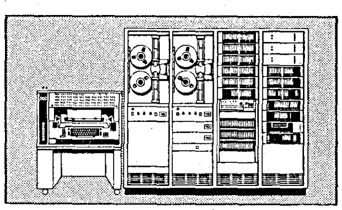
Real Time Waveform Measurement

Peak values, axis crossings, ratios of successive differences, and other characteristics of analog signals are measured in real time. Incoming signals are monitored for events of interest, using complex programmed detection criteria. In a typical biomedical application, the result is a 100-to-1 reduction in the bulk of magnetic tape output records.

$$A(n,w)=\int_0^T W(t)F(n,t)\cos(wt)dt$$
$$B(n,w)=\int_0^T W(t)F(n,t)\sin(wt)dt$$

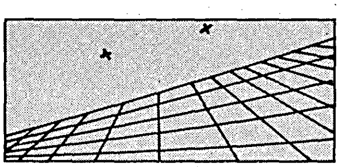
Spectrum Analysis

Parallel hybrid multiplication and summing, 2 microsecond 30-bit digital storage, and a flexible instruction format providing efficient list processing combine to make the AMBILOG 200 powerful in statistical signal analysis techniques such as Fourier transformation, auto and cross correlation, power spectrum density analysis, and generation of histograms of amplitude spectra.



Digitizing and Recording

Multiple inputs, from up to several hundred sources, are routed through a multiplexer switch array under stored program control. At no penalty in sampling rates over conventional systems, the AMBILOG 200 converts incoming data to engineering units for recording or monitoring. An analog-to-digital converter performs a complete 15-bit conversion in 4 microseconds for digital storage, recording or outputing.



Display Generation

Multiple analog outputs facilitate close man-machine relationships in systems involving visual displays. Points of an image stored in memory are rotated through three space angles and projected on a CRT at a 50 Kc rate. Co-ordinate transformation is accomplished simultaneously with digital-to-analog conversion.

For technical reports describing in detail these and similar AMBILOG 200 applications, write I. R. Schwartz, Vice President.

Adage INC
1079 Commonwealth Ave.,
Boston, Massachusetts 02215

CIRCLE 4 ON READER CARD

There are a number of ways to solve every computer systems problem...Here are three new ways from ASI

Advanced Scientific Instruments presents three new performance-rated digital computer systems totally covering the scientific computer market in the $2,150 to $12,500 per month range. These high performance systems in ASI's *ADVANCE* Series are completely upward program compatible and entirely modular in concept thereby allowing upgrading of each of the machines to a higher classification when your requirements demand still greater performance.

Select the system that exactly fits your requirements—then contact ASI!

6050

The *ADVANCE* 6050 has been designed primarily for the general purpose market. It offers capabilities such as; double precision floating point hardware (38 bits mantissa, 9 bits exponent)—floating point multiply 17.1 microseconds—floating point divide 28.5 microseconds. Typical fixed point times include multiply 7.6 microseconds—divide 9.5 microseconds. Direct input/output access to the accumulator register and to memory is also featured.

6070

Designed for use in the fast growing systems market, the 6070 provides a high performance unit with floating point hardware plus multi-processing capabilities. Simultaneous computation is available through an Accelerated-Processing Unit used with the standard processor unit. Sample operating times are; floating point add 9.5 microseconds—floating point subtract 9.5 microseconds—Sine 42 microseconds—Square Root 48 microseconds—Arctan 70 microseconds. Capabilities of the 6070 may be expanded by the addition of multi-processing units.

6080

Fulfilling the requirements of the high performance general purpose user, the *ADVANCE* 6080 offers such features as; memory protect and hardware relocation. These features allow time-shared operations, multi-programming capabilities, and the use of remote stations.

In addition to all the above features, these systems also have the general features of all *ADVANCE* Series computers. They are completely upward program compatible and include a highly flexible high speed instruction repertoire, word size is 24 bits plus parity, memory cycle time is 1.9 microseconds, up to 32,000 words of memory are directly addressable. Three hardware index registers and indirect addressing further expand the large machine capabilities of all these *ADVANCE* Series systems. The latest advancements in microelectronic circuitry have been incorporated in the higher performance members of the *ADVANCE* Series. The 6050, 6070 and 6080 now extend the capabilities of the *ADVANCE* Series equipments already introduced, that is, the *ADVANCE* 6020 and *ADVANCE* 6040 systems.

Contact ASI to see how each of these systems can fit your particular computer system requirements. We stand ready to compare these systems point for point, dollar for dollar with *any* machines in the same market. Write to Advanced Scientific Instruments, 8001 Bloomington Freeway, Minneapolis, Minnesota 55420.

ASI

ADVANCED SCIENTIFIC INSTRUMENTS

DIVISION OF ELECTRO-MECHANICAL RESEARCH, INC.

8001 Bloomington Freeway, Minneapolis, Minnesota 55420

CIRCLE 5 ON READER CARD

DATAMATION®

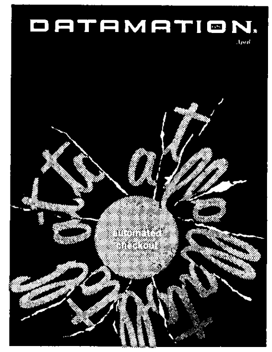
april 1965

volume 11 number 4

automatic information processing for business industry & science

april
1965

volume 11 number 4



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BPA Circulation audited by Business Publications Audit   Member, National Business Publications NBP

Microfilm copies of **DATAMATION** may be obtained from University Microfilms, Inc., 313 No. First St., Ann Arbor, Michigan. DATAMATION is published monthly on or about the tenth day of every month by F. D. Thompson Publications, Inc., Frank D. Thompson, President. Executive, Circulation and Advertising offices, 141 East 44th Street, New York, New York 10017 (MUrray Hill 7-5180). Editorial offices, 1830 W. Olympic Blvd., Los Angeles, California 90006. Published at Chicago, Ill. DATAMATION is circulated without charge by name and title to individuals who qualify by our standards and are employed by manufacturers or users of automatic information-handling equipment in all branches of business, industry, government and the military. Available to others by subscription at the rate of $15.00 annually; single issues (when available) $1.50. Foreign subscriptions are on a paid basis only at a rate of $25.00 annually. No subscription agency is authorized by us to solicit or take orders for subscriptions. Controlled circulation paid at Columbus, O. Form 3579 to be sent to F. D. Thompson Publications, Inc., 205 W. Wacker Dr., Chicago, Ill. 60606. Printed by Beslow Associates, Inc.

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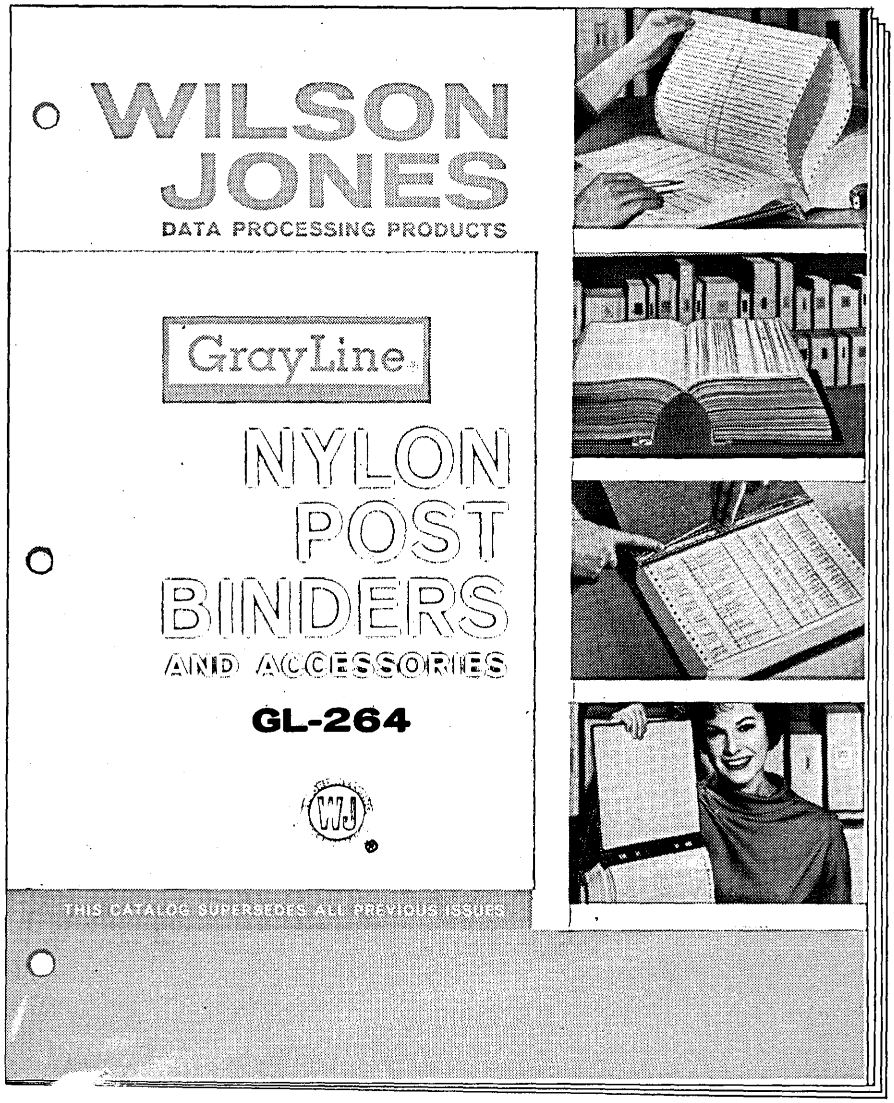

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CIRCLE 8 ON READER CARD

DATAMATION calendar

- A workshop on "Working with Semi-Automatic Documentation Systems" will be held May 3-5 at the Airlie Foundation, Warrenton, Va. Sponsors are AF Office of Scientific Research and System Development Corp.

- National Industrial Production Show of Canada, May 3-7, Toronto, Canada, will include 215 companies who will show 550 types of instruments and controls including computers, dp and N/C equipment.

- International well logging symposium, sponsored by the International Society of Professional Well Log Analysts, will be held May 4-7 at the Sheraton Hotel, Dallas, Tex.

- Industrial Communications Assn.'s annual conference will be held May 4-7, Pittsburgh Hilton Hotel, Pittsburgh, Pa.

- Center for Technology & Administration at American U. will hold the following courses, May 10-13: Advanced Computer Programming, Executive House; Institute on Electronics & Automation & Publishing, International Inn, Wash., D.C.

- Eighth National Power Instrumentation Symposium will be held May 12-14, Commodore Hotel, N.Y. Topic: Automation and Control Around the World.

- The Assn. for Educational Data Systems will hold its second annual meeting, May 12-15 at the Seville Hotel, Miami, Fla.

- Western Systems Conference will be held May 13, Statler Hilton Hotel, Los Angeles, Calif. Theme: Direction & Decision . . . the Management Challenge. Conference is sponsored by Systems & Procedures Assn., southern Calif. chapters.

- The Association of Data Processing Service Organizations, Inc. will hold its Management Symposium May 13-14, Stardust Hotel, Las Vegas, Nev. ADAPSO is the trade association of service bureaus.

CALENDAR . . .

● GUIDE International, user organization for medium- to large-scale IBM systems, will hold its session May 18-21, Statler-Hilton Hotel, Detroit, Mich.

● Brandon Applied Systems, Inc., N.Y. dp consulting firm, is offering following courses: Management Standards for DP, N.Y., May 19-20; Computer Selection and Characteristics Analysis, Wash., D.C., April 28-29 and N.Y., June 9-10.

● Power Industry Computer Application Conference, sponsored by the IEEE Power Group, will be held May 19-21, Jack Tar Harrison Hotel, Clearwater, Fla. Topic: Computers—Their Present and Future Impact.

● Digital Equipment Computer Users Society will hold its spring technical meeting at William James Hall, Harvard U., Cambridge, Mass., May 20-21.

● Annual meeting of POOL will be held May 20-22, Statler Hilton Hotel, N.Y. POOL is the organization of users of General Precision computers.

● IFIP (International Federation for Information Processing) Congress 65, including Interdata 65 Exhibition (May 24-27), will be held at the New York Hilton Hotel, May 24-29.

● College of Engineering, U. of Michigan, is offering a series of 13 noncredit courses for engineers and scientists. Dates run from May 24-August 9; subjects include introduction to optical dp and digital computer engineering; digital computers in realtime; automata theory; operation research; hybrid computation. Fees range from $160-275.

● Conference on "Cybernation, Automation and Human Response," sponsored by the Institute for Cybercultural Research, Inc., will be held May 27-29, Americana Hotel, N.Y.

● Purdue U., Lafayette, Ind., will conduct a course, Computer Models and Simulation Techniques for Power System Engineering, June 7-18.

● Southeastern regional conference of ACM will be held June 10-12, Palm Beach Towers, Palm Beach, Fla.

● MIT, Cambridge, Mass. will sponsor a two-week summer course on Concepts of Management Planning and Control Systems: Theory and Technology, June 15-25.

letters

computers & people

Sir:

Dr. Fein ("Dear Mr. President," Jan., p. 39) makes the fantastic proposal that more data [regarding automation and employment] be obtained by accurately predicting supply and demand for the next 10 years. He admits the difficulties of such a task are so insurmountable that even trained government economists despaired in its wake, but implies all that is required for success is more money, experts, and organization. (To grasp just an inkling of the enormity of this task . . . how simple is it to predict all the breakthroughs to be expected in the computer field in the next 10 years, or just next year? Multiply this by the myriads of fields of technology and you have just one small factor in the complexity of "demand") . . .

DARREL K. LACHEL
Cubic Corporation
San Diego, California

Sir:

I believe Dr. Fein has fallen into the trap of assuming that we can predict over rather long periods of time such amazingly complex and changeable factors as consumer tastes, individual capacity and propensity to consume, the varieties of consumable goods and services, the quality (as opposed to quantity) of such goods and services, birth rate, technological development, national goals, international commitments, etc. So long as we retain our motivation toward progress and our individual freedom of choice, Dr. Fein's proposal is not only "extremely difficult," but also impossible.

WILFRED A. KRAEGEL
Northwestern Mutual Life Insurance Company
Milwaukee, Wisconsin

collector's items

Sir:

It was nice to be complimented by R. L. Patrick, who refers to "the set of original Princeton Reports by Burks, Goldstine, and Von Neumann" as a collector's item (Feb., p. 41). Actually, I was co-author of only the first of these, "Preliminary Discussion of the Logical Design of an Electronic Computing Instrument." This was the report reprinted in DATAMATION.

There were three further reports by Von Neumann and Goldstine, "Planning and Coding of Problems for an Electronic Computing Instrument," in three volumes. These pioneering reports develop programming methods for modern electronic computers, including the use of flow diagrams, a library of subroutines, and combining routines.

All of the Princeton Reports are reprinted in Volume V of Von Neumann's "Collected Works," edited by A. H. Taub, published by Macmillan. This volume contains many other valuable papers on computers. Von Neumann left two unpublished manuscripts in automata theory, which I am editing. These will go to the Univ. of Illinois Press shortly, which will publish them under the title, "Theory of Self-Reproducing Automata."

ARTHUR W. BURKS
Department of Philosophy
University of Michigan
Ann Arbor, Michigan

hungary's maclogal

Sir:

Maclogal, the "stranger-than-fiction" machine from Hungary, may indeed be a "universal logical apparatus," as you have reported (Feb., p. 65). Its memory probably is huge enough to qualify for this classification (in the larger sense) whether its logic qualifies or not. You report that "a news agency gives its storage capacity as 1,260 x 10^{27} alphanumerics." If we assume that each alphanumeric consists of six bits and each core effectively occupies one cubic millimeter (since it has "an outer diameter of 1 mm"), the space required to house the core storage is roughly seven times the volume of the earth!

VICTOR E. WHITTIER
Computation Research Lab.
The Dow Chemical Company
Midland, Michigan

We told you it was stranger than fiction.

dp software

Sir:

In the February issue (p. 17) the comment is made, "To make its 900 series look to programmers like decimal computers, Scientific Data Systems is developing a meta-assembler with Boolean logic." Unfortunately, this is misleading in that our meta-assembler (currently available) incorporates extensive Boolean logic as a standard characteristic . . . [Actually, SDS] is extending its meta-assembler by *incorporating character manipulative procedures.* This extension yields a business language that is free form and character-oriented, somewhat analogous to the Autocoder type assemblers found on character machines.

DONALD H. SUNDEEN
Scientific Data Systems
Santa Monica, California

software copyrights

Sir:

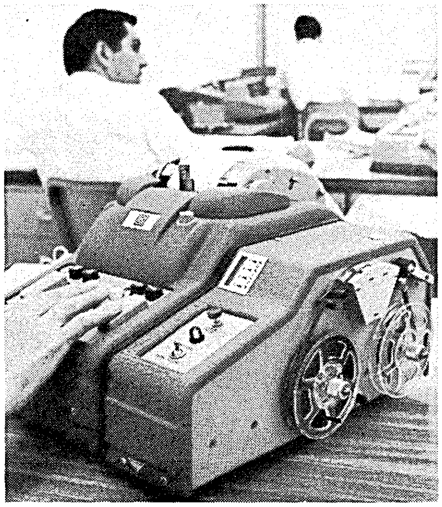
It would appear that it is R. F. Brady who seems to have missed the point (Feb., p. 12) of J. Richard Swenson's somewhat satirical letter in the December issue. Mr. Swenson was obviously trying to point out the misconception among many programmers and management personnel concerning the protection of copyrights for computer programs (i.e., that a copyright can be voided simply by changing a few words in the program). What Mr. Swenson was saying, in effect, was: "Try it and take the consequences when litigation begins."

Although the Copyright Office is somewhat vague in its instructions concerning the copyrighting of programs (e.g., "The detailed practices of the Copyright Office in this area will have to be evolved over a period of time, on the basis of experience"), it has agreed to consider registration for a computer program as a "book" in Class A under certain conditions. Thus, a copyrighted program has the same protection as a book—which obviously cannot be voided by "changing a few words." However, in the end, as Mr. Brady points out, precedent through litigation will have the final word.

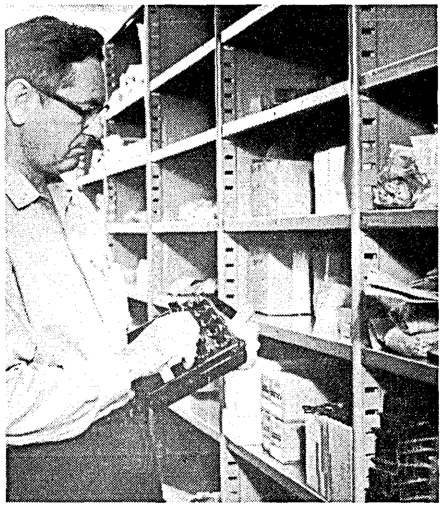
JAMES F. HOLT
Los Angeles, California

Record it...

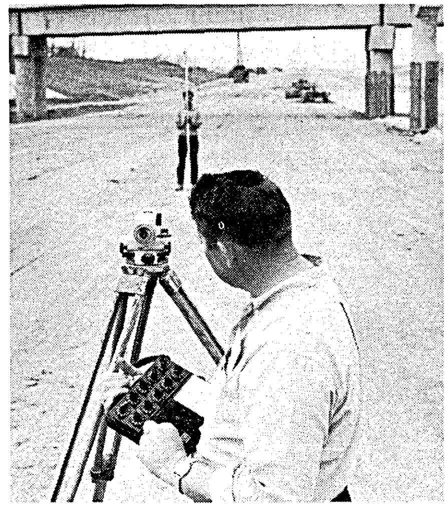
(on magnetic tape)



...in accounting department

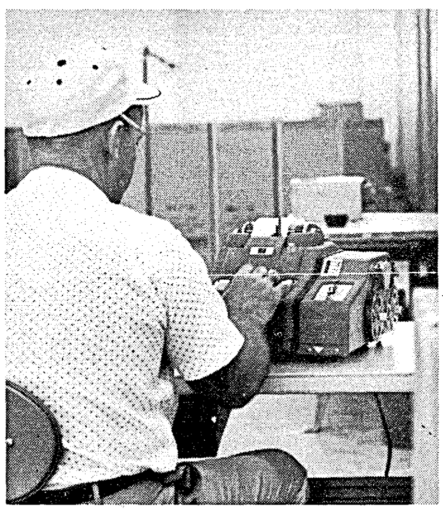


...at the parts bin



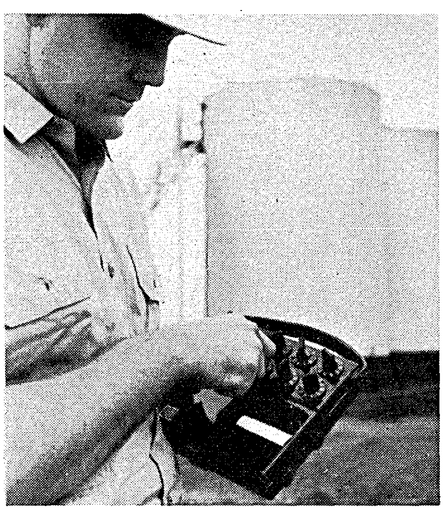
...on the job site

...at the meter



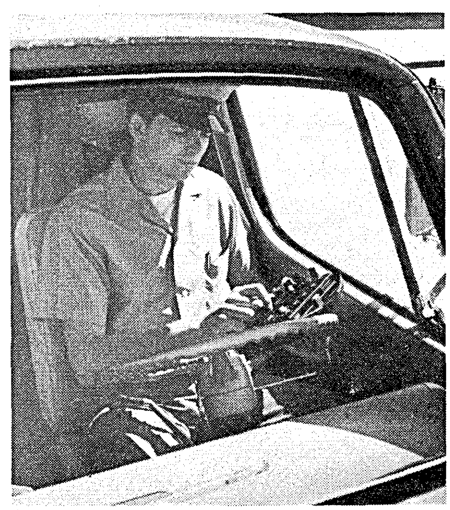
...in the warehouse

...at the cash register



...at the tank farm

...in the payroll department



...in the delivery truck

BUSINESS & SCIENCE

NEW CORE MEMORY FROM EMI

Latest random access core memory is "Nanomemory," a 16K, 56-bit unit with a 350 nanosecond access, and a 900-nsec cycle time. L.A.'s Electronic Memories, Inc., is producing the memory for fall delivery, and says cost per bit will be comparable to one-megabit, two-usec versions. Speed is supposed to be enhanced by short drive lines (none longer than 900 cores), no time separation between read and write currents (because no inhibit current used), and because low noise levels mean no need to pause for noise recovery. Costs are lowered by lack of a fourth inhibiting wire, and by the use of standard 30-mil cores.

Options will include a 700-nsec cycle and 350-nsec access using 20-mil cores, temperature ranges of 0°C to 50°C, and a smaller 28-bit version.

MPPL IN FOR NPL

We hear that a trivial bottleneck was delaying release of some NPL specs: the "initial" problem. Seems Britain objected to NPL, which also stands for National Physical Labs, and suggested MPL, but that one stands for a French company. The result, a new name: MPPL (Multi-Purpose Programming Language).

MOHAWK COPIES A PHILOSOPHY, ORIGINATES A PRODUCT

There's a lot of flutter about a new Herkimer, N.Y. outfit which has announced a device which transcribes info directly onto computer mag tape (see New Products). It's Mohawk Data Sciences Corp., formed last year, and headed by a bevy of ex-Univac people (giving rise to rumbles Univac may sue Mohawk).

Now employing over 50, Mohawk has its sights set on a market for some 75,000 Data Recorders, will offer them directly, through franchise dealers and OEM, the latter especially overseas.

A MDS brochure pitches IBM's industry domination, its plans to capitalize on this, following IBM & CDC product development which matches 6-7-year generation cycles. MDS says it will try to hit gaps in the IBM product line, noting "IBM is, basically, a rental agency." So, evidently, is MDS. One unit costs $7K, rents for $115. The rental goes to Boothe Leasing.

PROFITS, PRODUCTS POPPING AT SDS

Things are poppin' out at Millionaire Max Palevsky's hacienda. SDS (including new subsidiary CSC), has a $30-million backlog; expects to gross $45-million in '65, up its earnings/share from $1.02 to $1.50; delivered the first integrated circuit computer; announced a special-purpose 9300 called the DES-1 (Digital Equation Solver) and two new head-per-track disc files.

Continued on page 19

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CIRCLE 18 ON READER CARD

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Newton Highland

Opportunities exist at other Honeywell Divisions. S

Continued from page 17

The RAD (Rapid Access Disc) 9167 can hold over 8-million six-bit characters on up to four discs, has an average access time of 17 msec, a 480K cps transfer rate; prices go from $23,500 to $100K.

The RAD 9166 has a maximum capacity of 2 million characters; average access time is 34 msec; transfer rate is 60K cps; prices range from $18,500 to $95K.

The DES-1 combines a 9300, a special operator language and programming system (including compiler) for the solution of differential equations.

ONWARD & UPWARD FOR ON-LINE CREDIT

Telecredit, L.A. outfit offering stores on-line checking to see if a would-be check-casher is wanted by the police, now has 1700 customers who get up to 175 calls a month for $35, is still using a hopped-up 305 Ramac. A new service to banks offers a card which permits its customers to cash checks at Telecredit-ed stores. So far, 18 banks with 26 outlets in SoCal are signed-up; 35,000 cards have been issued. Telecredit plans new services once they get their 360 next year.

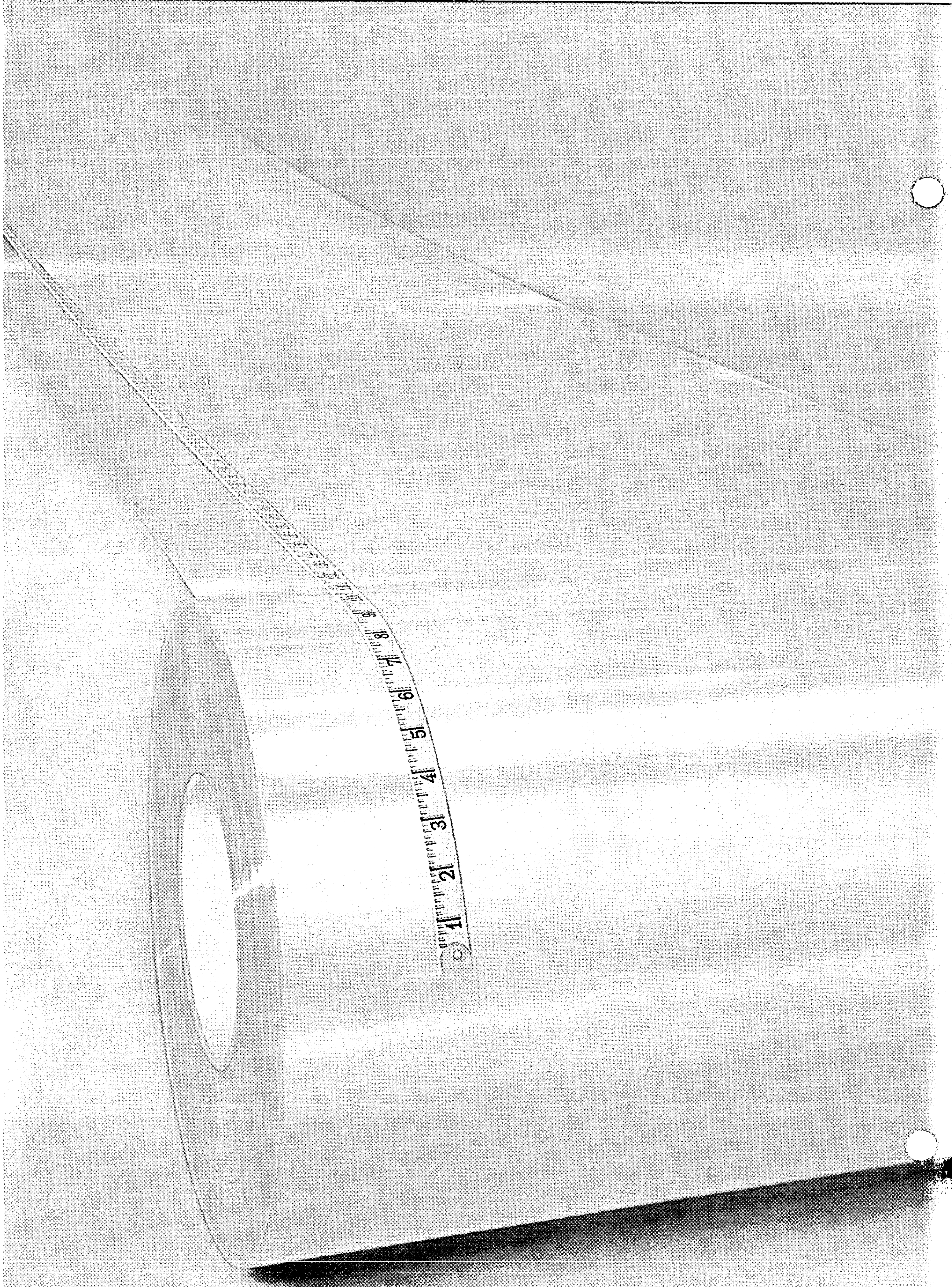
TIME-SHARING FOR CAL.

Latest ARPA-funded time-sharing installation is at the U. of Cal, Berkeley, where a modified 32K-core SDS 930 and a PDP-5 (which will be used to buffer CRT's), will help research into on-line research. The 930 is being changed to offer memory assignment and protection, and will be able to address 128K of core, just in case. Display and drum will arrive next month. The system will have its own operating system, will start with basic assembly language, revamped Fortran, and eventually build its own language and special-purpose translators. The system will have one remote display plus six Teletype consoles initially.

RUMORS AND RAW RANDOM DATA

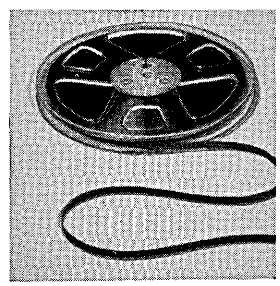
Computer Usage has been awarded a contract by Fujitsu to develop a Fortran IV compiler for the FONTAC computer. Delivery is slated for late fall. The contract, reportedly for $250K, may be the first for foreign software won by the American firm....We understand there are 83 computers installed now in Mexico....Data Display, rocked a bit by the appearance of the cheaper IBM 2260 display, says it will be competitive by the time 2260 deliveries begin.... IBM, evidently tired of the university give-away game, has upped its educational discount to 35-45%. It was 20%....Some wise guy stole a DPMA test at the latest certificate exam. One estimate is that it will cost DPMA $20K to revise the entire test....

It looks as if the U. of Michigan will go 360/66 for its time-sharing system. The 66, the 60/62 with relocation hardware, won out over the GE 625 and CDC relocation versions of the 3800 and the 6400.... Honeywell, which announced 15-million-to-billion-plus-character random access memories this month, will announce the 8200 computer soon. It's in the 360/70 class....IBM has told GUIDE it will support both MPPL (nee NPL) and COBOL; the latter will evidently not be dropped in favor of the newer language.... Raytheon is coming out with a re-vamped 440, yclept 450....Standard Oil of N.J.'s Mel Grosz has joined the war on poverty as a part-time assistant in info processing to Sargent Shriver....People using or contemplating getting LGP-30's will be glad to learn that Librascope is offering maintenance contracts for up to five years....

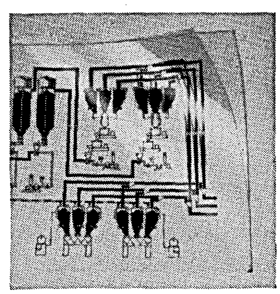


We'll go to any length to make Celanar Polyester Film your best buy!

We mean that literally! Case in point: Customers pointed out that a splice-free roll, tailored to *their* specifications (rather than to the suppliers), would give them a considerable processing advantage. So, unlike the other supplier, we tailor Celanar roll lengths to our customer's specifications. *Your* specifications.



This is just one of the meaningful service advantages causing so many manufacturers to switch to new Celanar polyester film. For magnetic tape. Packaging. Engineering reproduction. Metalizing. Stationery and office supplies. And electrical applications.



Other good reasons include *cleanliness*. New Celanar film is produced in a sealed-off "White Room" clean enough for surgery—the most modern in the industry. For the cleaner the polyester film, the better it processes.

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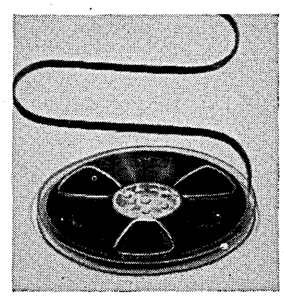

This is the kind of meaningful service you would expect from Celanese Plastics—whose operating philosophy is that the customer, not the supplier, is always right. Celanese Plastics Company, 744 Broad Street, Newark 2, N. J.

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Roll lengths tailored to your specifications, is just one of *six* meaningful service advantages you get when you switch to new Celanar polyester film.

Celanese

CIRCLE 19 ON READER CARD

DATAMATION

WASHINGTON REPORT

ADP POT BOILING ON CAPITOL HILL

The Budget Bureau, at the request of Sen. McClellan, is preparing draft legislation embodying recommendations contained in its recently-issued report on government dp practices and policies. Though BOB has already implemented a number of important changes with its Circular A-71 (see p. 70), several of its most critical recommendations would require enabling legislation and/or appropriations. These include the establishment of a revolving fund "to facilitate the establishment of service centers, equipment pools and time sharing arrangements," a directive to the Bureau of Standards "to establish a centralized research center on computer sciences and technology," and a command to all agencies to cooperate in the pending development of federal dp standards.

The BOB report was also noteworthy for what it did not recommend. The two most notable omissions were establishment within the General Services Admin. of a central procurement responsibility for dp gear, and the inclusion of contractor-operated, government-financed computing equipment in same.

In rejecting these two innovations, long sought by the General Accounting Office, BOB said they would "dilute the responsibility of agency heads for the management of their organizations," and "interfere with direct government agency-contractor relationships unnecessarily." However, BOB did indicate its willingness to go along with an extension of existing guidelines on the purchase or rental of dp equipment to government contractors under cost-reimbursement contracts. If adopted, this would mean, for example, a contractor would be reimbursed only for the purchase cost of his equipment even if accumulated rentals were in excess of that figure.

Copies of the report, as Senate Document 15, are available from the Govt. Printing Office for $0.50.

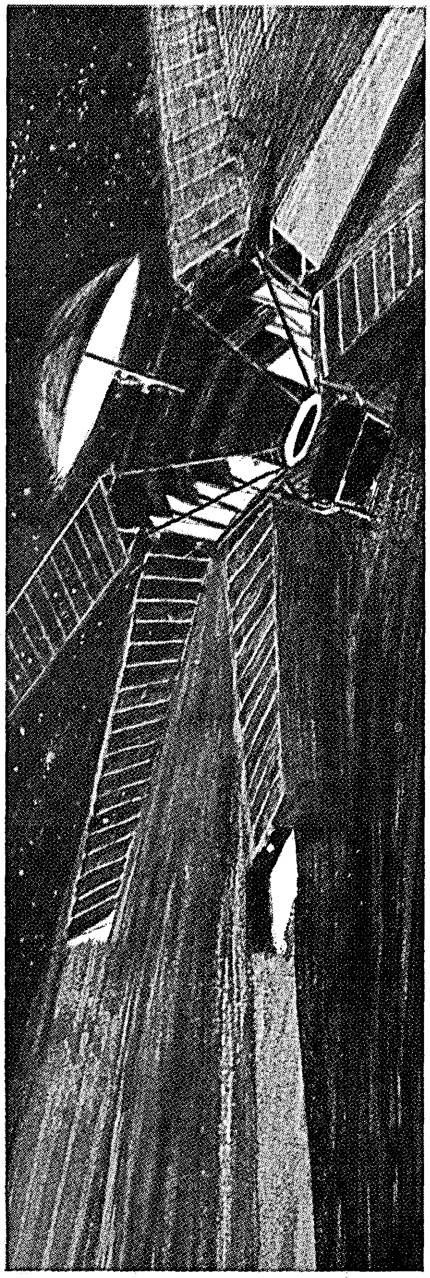
BUSINESS BOOMING IN COMPUTER BONEYARD

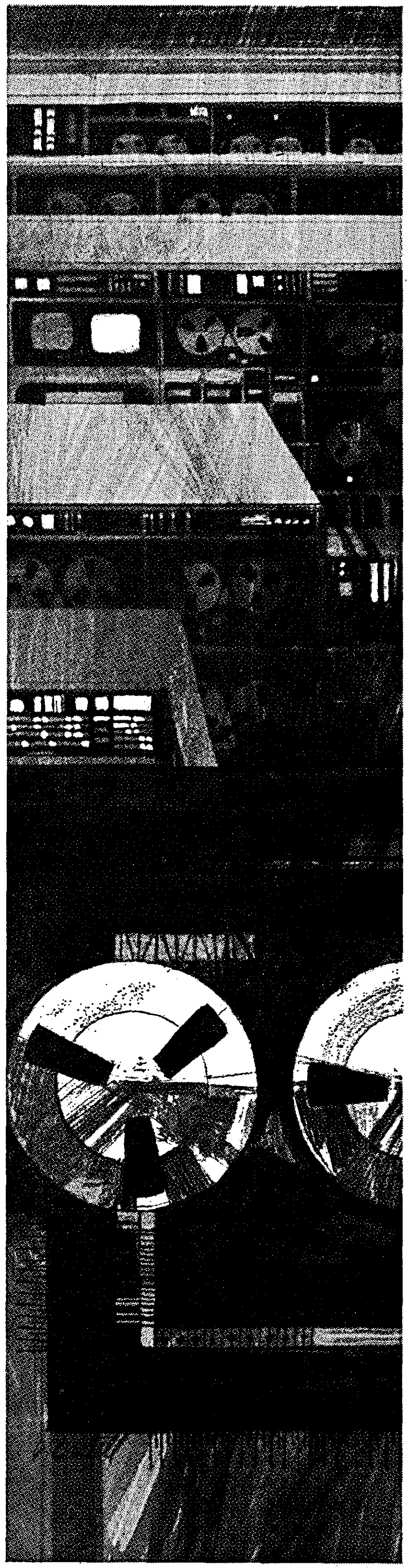
Old computers never die, but they are becoming declared "excess" with increasing frequency within the government. When this happens, the machines fall under the jurisdiction of the recently-formed (mid-'64) ADP Utilization Dept. of the General Services Admin., which attempts to find a home for them, or their component parts, with other government agencies. Unique within GSA, the separate organization reflects the growing awareness of the special nature of dp equipment.

As many as five to 10 systems, along with much peripheral gear, are declared excess each month. This volume is expected to grow exponentially as third-generation hardware arrive on the scene, another reason for the creation of a specialized department. Systems, of course, are either purchased or leased.

"Government-owned equipment is much easier to move," said a department official, "since agencies can obtain it just for the cost of dismantling and shipping."

Continued on page 111





NEW PRODUCTS

check sorter

Mod 1000 reportedly costs one-third of price of other sorters, reads and sorts 600 6-inch MICR documents/minute. It handles documents 6 to 9-inches long, 2¾ to 3⅝-inches wide. There are 10 sort pockets, one reject pocket, each with capacity of 225 checks, and feeder capacity is 1,750 checks. The caster-mounted unit occupies 78 x 18-inches of floor space. LUNDY ELECTRONICS & SYSTEMS INC., MICR/SCAN DIV., Glen Head, N.Y. For information:

CIRCLE 200 ON READER CARD

manual keypunch

The 311 is a portable, desk-top unit capable of punching up to 12 columns of numeric Hollerith code into 51- or 80-column cards, simultaneously interpreting at the top of each column. The 12 columns can be in any area, positioned by an adjustable stop. Readout windows allow visual verification of data before actual punching. DASHEW BUSINESS MACHINES INC., Los Angeles, Calif. For information:

CIRCLE 201 ON READER CARD

gp computers

The 360/64 and 66 are time-sharing processors featuring dynamic relocation with associative memories, and channel controllers. Four of the latter, with four processors and eight memories, can make up a multiprocessing configuration. Cycle time of the 64 is 2 usec for eight characters, and of the 66 is 1 usec. Up to 8 million characters of core are available. IBM-DP DIV., White Plains, N.Y. For information:

CIRCLE 202 IN READER CARD

instrument cleaner

Micro-Duster is portable, compressed lab-clean gas for dusting without abrasion. The gas, dichlorodifluoromethane, is non-toxic, non-corrosive and non-flammable, comes in 15-oz., replaceable can good for 600 one-second cleanings. TEXWIPE CO., Passaic, N.J. For information:

CIRCLE 203 ON READER CARD

mag tape reel

Hub and winding surface of reel are of turned aluminum, machined together for concentricity. Flanges are coupled to the hub by elastic cement, permitting differences in thermal expansion without disturbing flange parallelism. Color-coding of reel is a plastic ring around hub, bearing manufacturer's name and other labeling data. DATA PACKAGING CORP., Cambridge, Mass. For information:

CIRCLE 204 ON READER CARD

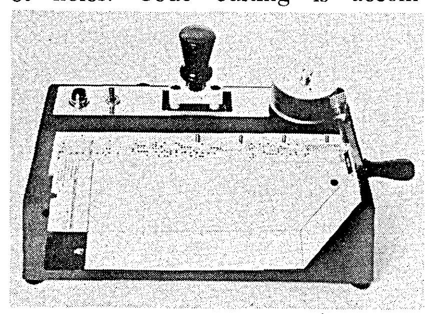
character generator

The CLX33083 is an integrated-circuit unit packaged on two boards. Stroke writing is used for character generation, which includes all digits, all letters except Q and Z, and four special symbols. Two formats are used in the alphanumeric unit, rounding is not available, and speed is up to 50,000 cps. In operation, one input line is provided for each character, while outputs are x and y analog deflection voltages. Temperature range is —25 to +85°C. INFORMATION DISPLAYS INC., Mt. Vernon, N.Y. For information:

CIRCLE 205 ON READER CARD

edge-punched card splice

The 501-EP repairs tears, and reinforces folds, leading edges and sprocket holes. Code editing is accom-



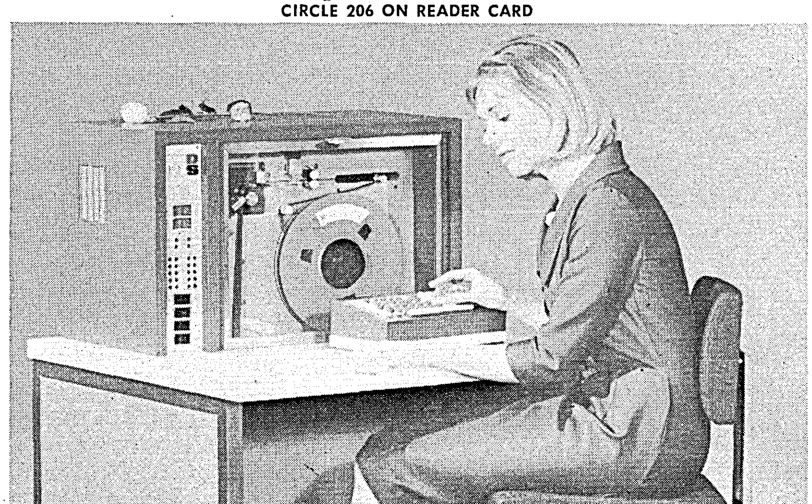
PRODUCT OF THE MONTH

The 1101 Data Recorder combines functions ordinarily performed by a card punch, key verifier, and card-to-mag-tape conversion runs. It transcribes directly from source documents to half-inch tape, and verifies the accuracy of the transcription.

With the 1101, source data is keyed into 80-character core memory and, on command, written on tape. The IBM-compatible unit operates in entry, verify, and search modes, and has skip, duplicate, and automatic verification speeds of 80 usec per data position. Operator can backspace to correct errors on 80-character record being typed. Each record written on tape is automatically read back into core for verification.

Options include a data display, unit record counter (for number of records on tape), self-check digit device, and an alternate program to allow two record formats per run. MOHAWK DATA SCIENCES CORP., Herkimer, N.Y. For information:

CIRCLE 206 ON READER CARD



haps to save himself writing a separate verbal description of the program for documentation. Fig. 2e shows only a small part of the effort implied by Fig. 2c. The total process of Fig. 2e gets the program through the first two sentences of Fig. 2c, and the first seven words of the third sentence.

As is obvious from this narrative, Analysis and Program Design is a demanding task. It requires people who can understand both hardware and coding, and who are capable of thinking about complex logical sequences. If the testing operation involves prime equipment whose operation is complex in detail, it is desirable that a large majority of the programmers have engineering training. If the testing operation involves relatively simple individual tests, even though the total sequence may be long and complex, it is possible to use more people with mathematical or other training. A mixture of both types of personnel is normally required for a large programming job.

Analysis and Program Design may also require diplomatic talents and stubborn perseverance if the prime system or test equipment is ill-defined, ill-documented, or in a state of rapid flux.

coding

Coding begins after a flowchart (or its equivalent, such as a written or mental step-by-step description) has been prepared. The resulting manuscript may be in machine or assembly language, or in a problem-oriented language. For example, a hypothetical POL might yield Fig. 3 from Fig. 2e.

Tape preparation from the coded manuscript is usually of negligible cost compared to the other elements of programming, although the process development may not be, if it has sophisticated features. For example, the development of an automatic-test compiler program may require five to 10 man-years of highly skilled effort.

Coding may or may not be a demanding task, depending on whether (1) schedules permit thorough analysis and design before coding, (2) the computer speed, input-output, and memory size are well in excess of the bare minimum required, and (3) the tester has an "easy" coding structure. If all three of these conditions are true, coding is relatively easy. If one of them is not true, coding may require extra talent or effort, and may react both on the analysis-and-design and on the checkout. The last of the three conditions — coding structure — may be improved greatly by construction of a suitable compiler or interpreter.

checkout

Once coding is complete, and the program tape (or card deck) has been prepared, checkout begins. The first step in checkout is to make the coded program correspond with the original flowchart — that is, "cycling check" or "elimination of blunders." All it proves is that the initial coding has been performed correctly, and it is usually a small part of the checkout process.

The next step of checkout is to make the flowchart correct, and correct the coding accordingly. This is often divided into two phases: "static" checkout and "dynamic" checkout. Static checkout includes all checking which can be performed without real prime equipment. For example, each step of the program may be run individually to make sure that the proper stimulus lines are excited and that the proper input lines are measured.

Both cycling check and static checkout are often facilitated with an off-line data processor program which simulates, at least statically, the internal operation of the automatic test equipment. Such a simulator eliminates waiting in line to work with a limited amount of real test equipment, and permits an extra flexibility of "debugging" control which is useful in diagnosis of errors.

The final step of checkout is dynamic checkout, in which the program is run on real test equipment with real prime equipment. This is the most time-consuming, and by far the most expensive, phase of checkout. In this phase, the program assumes its final role as one complex element of a larger system, and the problems are the usual ones of hardware system integration. For the benefit of those who have not been involved with this kind of harrowing task, some typical problem areas are:

Fig. 3. Hypothetical example of code sheet in problem-oriented language, for flow chart of Figure 2e. Steps 303-305 are the first loop, and 307-311 the second. It is assumed that the computer speed—and the speed of the machine-language implementation of the POL—are such that the steps and loops occupy suitably small numbers of microseconds.

```
  1  DEFINE SERVO TEST FROM 301
  2  DEFINE ACTUATOR RELAY AS DO 23
  3  DEFINE ACTUATOR EXCITE AS DI 37
  4  DEFINE FAIL RELAY 23 FROM 724
  5  DEFINE FEEDBACK VOLT AS AI 43, FULL
     SCALE 10.0 VDC
  6  DEFINE ACTUATOR STUCK FROM 923
  7  ..............etc.
  •
  •
  •
300  ........................
301  BEGIN SERVO TEST
302  SET ACTUATOR RELAY
303  IF ACTUATOR EXCITE IS ON, GO TO 306
304  IN K MSEC AFTER 302, GO TO FAIL
     RELAY 23
305  GO TO 303
306  MEASURE INITIAL FB VOLT = FEEDBACK
     VOLT
307  MEASURE FB VOLT = FEEDBACK VOLT
308  COMPUTE DIFFERENCE = FB VOLT —
     INITIAL FB VOLT
309  IF DIFFERENCE IS GREATER THAN OR
     EQUAL TO J VDC, GO TO 312
310  IN L MSEC AFTER 306, GO TO ACTUATOR
     STUCK
311  GO TO 307
312  ..............etc.
  .
  .
  .
723  ....................
724  BEGIN FAIL RELAY 23
725  ....................etc.
  .
  .
  .
922  ....................
923  BEGIN ACTUATOR STUCK
924  ....................etc.
  .
  .
  .
```

1. The prime equipment (or the automatic tester), being newly designed, is only available for program checkout for a portion of the time. Some of the interruptions are predictable, such as scheduled down time for retrofitting of design changes, or for hooking up and testing newly delivered pieces of the system. Others are not, such as equipment failures (espe-

cially frequent when the designs are new), and late deliveries of pieces of equipment used with the program whose checkout is about to be attempted.

2. The equipment may not act the way it was expected to on the basis of the documentation available to the programmer. The documentation may be inadequate simply because it left out areas which affected the program in ways that the programmer did not predict. (For example, one project had a baffling problem during tests in which the power supply voltage was varied. It turned out that the prime equipment detail specifications had not mentioned transient response speed for the power supplies, since it was not important to normal system operation — but the automatic tester was varying the voltage in steps. The error symptoms were unfortunately quite obscure, and the power-supply specification difficult to obtain, so the checkout schedule was badly dented before the problem was well understood). It may be downright incorrect, because the configuration control was inadequate and the engineers who made "minor" changes didn't tell the programmers about them, or because "unimportant" design deficiencies have not yet been cleaned up. Or, more embarrassingly, the programmer may simply have misinterpreted the information he received.
3. The equipment actually available in the laboratory may be a prototype or engineering version which differs in many respects from the final design. If the programmer has been happily making a production-version program, he has a whole new programming job ahead of him at the last minute. Worse, if the equipment is continually being taken away piecemeal for modification or repair, and replaced by similar but slightly different pieces, the programmer must spend most of his time patching and "kluging" the program to make it reflect the instantaneous state of the equipment. The latter may unfortunately be inevitable with certain kinds of systems.
4. Many of the subtler system checkout problems involve interacting errors in both the program and the equipment. Many others turn out to be pure program or equipment design errors, but require weeks of effort to isolate to the point where this fact is known. If the programmer is not ready to go at least halfway toward becoming a hardware checkout engineer, and vice versa, the program never will get checked out. (For example, was yesterday's short circuit and fire caused (1) by a stuck relay, or (2) by a computer circuit transient which occurs only with certain sequences of commands, or (3) by a program timing which checked the relay too soon, thereby thinking it was open when it was in fact closing?)

(Since this article is addressed to a computer audience, we won't mention the equally unpleasant problems which the program can cause for the equipment checkout engineers).

the role of simulation

Unfortunately, simulation is of limited applicability in dynamic test-program checkout, even when the prime equipment is very expensive. For problems other than automatic test, an analog or digital model may provide an accurate and useful simulation of the overall performance of a prime system (e.g., aircraft stability and maneuver capability, radar tracking capability, etc.). However, the level of detail of such a simulation is limited. In essence, it merely solves the equations characterizing system performance, and does not concern itself with internal electrical or mechanical features of the system, except as they affect parameters of the performance equations. To simulate to the level of detail required for test-program checkout usually requires so much time and effort that checkout on the real equipment is preferable — especially since some of the same factors that make test-program checkout difficult will also make it difficult to provide a realistic simulation of the prime equipment.

In spite of these difficulties a "hardware" model is sometimes useful, if it can provide better access to test points or less functional interdependence than the real prime equipment, or if a special difficulty exists with prime-equipment scheduling.

A suitable problem-oriented coding language may speed checkout somewhat, by easing the communication problems inherent in trying to describe the program's actions to a non-computer-oriented engineer. *Good* flowchart documentation is almost as useful as a problem-oriented coding language, and often a necessary supplement to it. However, (1) it lacks the convincing feature of blunder-free translation to machine language, and (2) it is often harder to get because it may look like an extra task to the programmer instead of an integral part of his job.

Checkout (except for the relatively miniscule job of cycling check) is also a demanding task. The programmer should ideally have a good understanding of the total system, and a personality which will permit him to work with equipment engineers as a part of a unified team. This sort of problem, of course, is common to all system checkout, and its statement merely re-emphasizes the fact that the program is only a part of the system.

additional documentation

"Additional documentation" is the documentation required over and above the minimum flowcharts, coding sheets, and I/O assignments needed to prepare the program. It includes such things as program and system specifications, verbal descriptions at various levels of detail, operator procedures, extra comments on the coding sheets, etc. It is often vital to system success. It can be practically a clerical job if the programmer has kept good records. If not, he may have considerable difficulty reconstructing his past reasoning.

distribution of cost

The cost of programming is sometimes looked upon as a direct programming labor charge. To be sure, there may be charges for the data-processor time absorbed by coding aids, and engineering time used in discussing problems with programmers, but these are usually small compared with the programming labor.

Unfortunately, this viewpoint neglects the cost of scheduling (and supporting) program checkout on the real test and prime equipment. Program checkout is a heavy competitor for time on the prototype GSE and prime system. This affects total project costs because of (1) the effort required of equipment engineers, to maintain the equipment and work with the programmers on the joint total problem of test system checkout, and (2) the usual semi-fixed costs of calendar time on any project. It has sometimes proven necessary to manufacture — and keep up-to-date, and maintain — duplicate prototype equipment for program checkout. ■

Part 2 of this paper, appearing next month, will be devoted to problem-oriented languages for automatic test, and will summarize briefly a few of the conclusions of the recent Project SETE survey.

standard bearer

THE ATOLL CHECKOUT LANGUAGE

by B. L. RYLE

The Saturn/Apollo program can be described only in superlatives—it is the largest most expensive exploration project ever undertaken by man. It has also created management problems which are correspondingly extreme. The result of an attempt to solve one of these problems was ATOLL (Acceptance Test or Launch Language).

Eleven different ATOLL translators are in various stages of completion to be run on a total of six different off-line support systems, for execution, in various combinations, by four different checkout computers.

Reaction to ATOLL has ranged from very enthusiastic ("a big improvement over computer assembly language") to highly critical ("it doesn't do enough"). On the whole, however, it has contributed, by being a standard, to the solution of some of the management control problems associated with the enormous task of programming the many Saturn checkout systems.

The entire approach to developing the big Saturn boosters has been different from that used for Air Force ballistic missile weapons systems. It has been more akin to the "arsenal approach" of the Army, in that much of the development work for the Saturn I, Saturn IB and Saturn V launch vehicles was (and is being) performed in the laboratories of the Marshall Space Flight Center (MSFC) in Huntsville, Ala. These same laboratories are also responsible for the construction of many of the prototype stages. However, Boeing Aircraft, Chrysler Corp., Douglas Aircraft, IBM and North American Aviation are each prime contractors for production of one or more of the stages in the three different models of launch vehicles (Saturn I, IB, and Saturn V).

Because of the large number of component parts in each stage, and the resultant increase in the testing required, automation of the checkout operations was mandatory. Because of a large number of organizations involved, the number of different checkout systems, each incorporating a digital computer, became correspondingly large. The initial impetus for a common language arose from the requirement that NASA and Air Force inspectors had to be able to certify the adequacy and the results of each test applied to each stage. This meant that they had to understand what was happening during an automated test.

An equally compelling argument for commonality arose because of the way in which Saturn test programming was beginning to go in many different directions at the different organizations. Within MSFC, two dissimilar languages were started by two different laboratories. One, HYLA, was intended primarily for launch site operations; the other, QUEST, was intended for the less-demanding stage checkout operations in MSFC's own shops. Elsewhere, Douglas developed still a third language, STOL, and built up an entire operating and support system based on it. At the other extreme, others of the stage contractors were doing test programming in the assembly language of whatever computer their checkout system used.

In late 1963, MSFC issued document number 85M-06078, entitled "Launch and Checkout Computer Program Configuration and Control Plan." This was the official debut of ATOLL, or, rather, of what might be termed "basic ATOLL." It was not, and is not, an exceptionally elegant language. Intended for the "apply-stimulus-measure-response" type of operation which typifies much of stage checkout, it is a language which was designed by test engineers who approached the problem from the standpoint of what they would like to be able to tell the system to do. More important, it has proven to be a useful tool in precisely those areas for which it was intended.

The original concept of ATOLL was that it would be open-ended, and that a group would be set up in the Computation Laboratory at MSFC to monitor and control additions to the language. This concept has been followed. Revision B to 85M06078 was issued October 26, 1964. The somewhat augmented ATOLL described in that document lists a total of 36 operators, some of which are quite similar.

Four general classes of ATOLL operators have been defined:

a. **Stimulation** operators cause a stimulus to be applied

Vice president of Mesa Scientific Corp., Mr. Ryle is in charge of the Southern Operation in Huntsville, Ala. He had been responsible for the firm's Systems Analysis and Applications Div., associated with the development of test-oriented languages, including STOL (Saturn Test Oriented Language), for programming different check-out systems. He has also been associated with Douglas Aircraft and NCR's Electronics Div., and is a graduate of Caltech.

to that portion of the vehicle or stage undergoing automatic checkout or launch testing. See Table 1.

b. **Response** operators are used to verify a response or reaction from the vehicle or stage undergoing automatic checkout or launch testing. See Table 2.

c. **Control** operators are used to time and/or control the logical flow of the automatic test statement sequence. See Table 3.

d. **Utility** operators are all other operators which do not fit clearly into one of the above classes. See Table 4.

The format for ATOLL statements was established as partially fixed-field and partially free-form. As punched on a card, the fields are defined as follows:

Step Number (cc 1-6)
The Step number consists of a four-character alphanumeric Step field followed by a two-character alphanumeric Sub-Step field. The Step field identifies a sequence of test statements; the Sub-Step field identifies statements within this sequence. The Step number serves as a label for the statement.

Operator Field (cc 7-10)
The Operator field is used to enter the desired four-character alphanumeric ATOLL operator code. The code entered determines the usage of the remaining fields. Unused fields are to be left blank.

Condition Field (cc 11)
The Condition field is comprised of a single character which is used to indicate the on-off condition or other conditional information required by the ATOLL operator (e.g., by-level operations or branching conditions).

Value Field (cc 12-19)
The Value field is comprised of a maximum of eight characters which may include sign, six decimal digits, and the decimal point, as required. These values require no scaling or conversion to other systems before being entered into the ATOLL form.

Lower Limit Field (cc 20-25)
The Lower Limit field is comprised of six characters representing sign, four decimal digits, and the decimal point. The Lower Limit field is algebraically added to the Value field to derive the lower tolerance bound for analog measurements.

Upper Limit Field (cc 26-31)
The Upper Limit field is comprised of six characters representing sign, four decimal digits, and the decimal point. The Upper Limit field is algebraically added to the Value field to drive the upper tolerance bound for analog measurements.

Units Field (cc 32-34)
The Units field is comprised of three alphabetic characters which represent the dimensional units to be applied to the analog signal under consideration. When possible these three alphabetic abbreviations should follow good engineering practice. Examples of such three-character mnemonics are:

OHM for Ohm
VDC for Volts Direct Current
VAC for Volts Alternating Current
AMP for Amperes
CPS for Frequency in Cycles Per Second
PSI for Pounds Per Square Inch
RMS for Root Mean Square

Time Field (cc 35-42)
The Time field is comprised of a maximum of eight characters, and is used to express time requirements for certain ATOLL operators. Time may be stated in integral milliseconds by the entry of an integer without decimal point or units. Time may also be stated in seconds,

Table 1: Stimulation Operators

OP CODE	DESCRIPTION
ALOG	A step function, of magnitude given in the Value field, will be applied to the unit on units addressed in the Variable field. An entry in the Time field causes a pulse of the specified duration (in MS) to be applied.
APLY	An analog signal of amplitude given in the Value field, and frequency given in the Variable field, will be applied to the Unit or device addressed in the Variable field.
DISO	Causes the discrete lines addressed in the Variable field to be set to the state given in the Condition field. An entry in the Time field may be used to specify a duration of the condition.
RAMP	Causes a stepped ramp signal to be applied to the unit or device moved in the Variable field. The Value of each step increment is in the Value field, the Lower and Upper Limit fields contain the initial and final values of the ramp signal and the Time field will contain the duration of the signal.
SEND	The Octal word—the Variable field will be output to external switching logic; alternately two storage cells may be addressed and the logical sum of the two will be output.

Table 2: Response Operators

OP CODE	DESCRIPTION
(DELY)	See Table 3
DISI	The Reference Profile entry for the discrete input devices named in the Variable field will be set equal to the contents of the Conditions field. Note: This does not cause sampling of the discrete inputs.
(READ)	See Table 4
(SCAN)	See Table 3
(TEST)	See Table 3

Table 3: Control Operators

OP CODE	DESCRIPTION
BEGN	Causes the following closed sub-test procedure (i.e., subroutine) to be labeled per the contents of the Variable field.
BOOL	Causes the Boolean expression the Variable field to be evaluated. If the result is 1 (true), the next statement will be skipped; otherwise it will be executed.
DELY	Causes a delay until the device or devices named in the Variable field meets a specified gate condition. The Time field, if used, denotes a time interval "OR'd" with the gate. If the device is discrete, the Condition field denotes the gate condition. If the device is analog, the nominal release value is entered in the Value field and the limits around the nominal are entered in the Limits fields.
END	Denotes the end of a main test procedure; control reverts to semi-automatic.
EXEC	Causes the operational sequence (i.e., subroutine or sub-test procedure) sequence named in the Variable field to be executed.
GATE	If the cell named in the Variable field is a counting cell (i.e., countdown clock, EST, etc.) execution will be delayed until the cell is equal to or greater than the contents of the Value field. If the addressed cell is not a counting cell, execution will be delayed until system reference time is equal to or greater than the sum of the contents of the addressed cell and the contents of the Time field.
GOTO	Causes an unconditional branch to the step named in the Variable field.
(INCX)	See Table 4
PBAK	Causes the Executive to retain the step number or label in the Variable field, to be branched to if a backup condition should arise.
PEMS	Similar to PBAK for Emergency stop conditions.

Continued on pg. 35

OP CODE	DESCRIPTION
PMON	Similar to PBAK for Hold conditions.
RCAL	Releases the memory used by the routine named in the Variable field (previously reserved by a CALL statement) back to the system.
RETN	Used to denote the end of a closed Sub-test procedure (i.e., a sequence which started with a BEGN statement).
SCAN	Causes all discrete inputs to be scanned and compared with the reference profile (see DISI). The Time field may contain a delay before scanning is initiated. The Variable field may name one or more recording addresses. Failure to compare results in a "NO-GO" which will cause a reversion to semi-automatic operation (Halt).
SEMI	Halts execution of the test procedure. A message for display may be contained—the Variable field.
TEST	Causes an analog or discrete device named in the Variable field to be tested. A storage cell may also be designated to receive the sampled value. The Condition field may contain "O," "I," "W," "N," "L," or "G," denoting "O," "I" (for discrete) "Within tolerance," "Out of tolerance," "Low" or "High," respectively, as the condition which will cause branching to the statement named in the Variable field. For Analog devices, the nominal value will be entered in the Value field; if applicable, tolerance limits will be entered in the Limits fields.

Table 4: Utility Operators

OP CODE	DESCRIPTION
ALGE	The algebraic equation in the Variable field is evaluated; FORTRAN-like notation used.
CALL	The program, test procedure, subroutine etc., named in the Variable field is input from tape, is necessary, and set-up for execution.
DPLY	Causes the designated information to be output to the designated display device per the contents of the Variable field.
FLAG	Causes flags specified in the Variable field to be set or reset per the condition field entry.
INCX	The pseudo index register designated in the Variable field is incremented by the literal contents of the Value field, and the result compared with the contents of one of the Limits fields; inequality causes branching to the statement named in the Variable field.
LOAD	Loads literal data from the Variable field into sequential reserved cells, starting with the one named in the Variable field.
MOVE	The number of cells named in the Value field is moved from the block first identified in the Variable field to that secondly identified.
NAME	The first operator of any test procedure; establishes the contents of the Variable field as the label of the procedure.
READ	Causes the PCM or Analog channel or channels named in the Variable field to be sampled and stored in the cell or cells also named. Entries in the Value and Limits fields will cause a tolerance check of the sample; a "No-Go" will cause a halt (equivalent to reverting to semi-automatic).
RECD	Causes the data identified in the Variable field to be output and/or recorded per a pre-determined format "built" into the system.
RESV	Equivalent to a BSS in a common memory area; the number of cells named in the Value field is reserved and labeled per the Variable field.
SETT	The time cell designated in the Variable field per the system time reference (for non-counting cells) or per the contents of the Value field (counting cells).
SETX	The pseudo index register named in the Variable field is set to the contents of the Value field.
TABL	Established a sequential list, labeled per the contents of the Step field, and containing, in the successive cells, the successive entries in the Variable field.
TEXT	The contents of the Variable field are treated as comments, or may be labelled for on-line display.

minutes, or hours by using four decimal digits, a decimal point and the appropriate time-unit abbreviation (SEC, MIN, HRS). Examples of the Time field used in this manner are:

32.50SEC
1.333MIN
1.750HRS

Variable Field (cc 43-70)

The Variable field is comprised of up to 28 alphanumeric characters per line which are used to specify arguments, addresses, and all other information required by an ATOLL operator but not contained in the fixed Operand fields. The ATOLL operator used in a test statement will define the usage of the Variable field for that test statement. Overflow lines will be punched on successive cards. The Variable field will be terminated by an end-of-line character ($).

Remarks Field (cc 71-80)

The Remarks field comprises the remainder of the ATOLL form. This field will be used to attach English-language references to test statements and for any other necessary information required for, or by, local applications. This information is punched on the card(s) following the last Variable field information.

The arguments entered in the Variable field are identified by a one-, two-, or three-character alphanumeric prefix, followed by an appropriate unique numeric identification number. The prefix has been defined to consist of a single-character argument class designator and, where appropriate, a one- or two-character "argument address." The latter may be considered as a sub-class designator.

It should be emphasized that the present set of operators is not expected to be mechanized "in toto" at any single installation. Instead, each organization will mechanize those appropriate to the checkout system used and consistent with the operating concepts adopted. Indeed, the present list of 32 operators contains several that are "site-peculiar" and were incorporated to facilitate the transition to ATOLL at one or more of the participating organizations.

One way of describing ATOLL is that it is an Op code set for a psuedo-machine whose primary activities are I/O and whose I/O devices are both numerous and diverse in characteristics. Unfortunately, therein lies its major weakness, an emphasis on the checkout system rather than on the system or device being tested. For example, an analog device is addressed in terms of an internal code related to the pin and connector over which the signal from the device enters the checkout system, rather than being addressed in terms of a vehicle-oriented name which does not vary if the pin-number is changed.

At the present time, ATOLL II is being developed under the auspices of MSFC's Computation Laboratory, as an eventual successor to what is properly ATOLL I. ATOLL II more closely resembles NPL than it does ATOLL I (although compatibility with ATOLL I is a requirement), and is a considerably more powerful language. It incorporates features which permit automatic segmentation of large test programs for overlay purposes, and which permit time-shared operation of a checkout system via a number of operator's consoles.

ATOLL II, as a language, is being designed for the professional programmer of checkout systems as well as for the test or launch engineer who is only a sometime programmer. Hopefully, it will further extend the capabilities of the test engineer to write his own checkout programs in a language that he, and the test inspectors, readily understand. However, until ATOLL II has been shown to be a significant improvement over ATOLL I, the latter will continue to be the standard language to be used in Saturn checkout. ■

SOFTWARE FOR RANDOM ACCESS PROCESSING

the parts list application

by CHARLES W. BACHMAN

The Integrated Data Store[1] is being applied to an increasing number and variety of data processing tasks. One of the earliest was the processing of engineering parts lists. Suited to this assignment by reason of its ability to handle the most complex information structures, the Integrated Data Store is a programming system designed to organize and process records within a random access data storage device, such as a disc, drum or loops. It provides a means of defining data structures (records and chains) and a set of procedural verbs (STORE, RETRIEVE, MODIFY AND DELETE) that operate within the defined data structure.

The facilities of the Integrated Data Structure are supplementary to those of standard programming languages such as COBOL and FORTRAN. Jointly they provide a new opportunity to organize and process data to achieve specified business objectives.

The principal data organization mechanism used by the Integrated Data Store is the chain, which permits a group of related records to be tied together. This tie is accomplished by storing, within each record of the group, the address of the next record of the group. Thus a chain becomes a circular association of records. Fig. 1 illustrates a sample chain. The small diagram at the lower right is the shorthand description of the same chain.

Each chain contains one and only one master record. This record is specified in the data definition as the chain's master. Whenever a master record is stored, the chain is created and the master record's own address is stored in its pointer field.

Each chain may contain any of several detail records —zero, one, 10, or 10,000. Whenever a detail record is stored, it is automatically linked into the chains within which it is defined as a detail. The prior record in the chain

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[1]Bachman, C. W.; Williams, S. B., "A General Purpose Programming System for Random Access Memories," *Proceedings,* Fall Joint Computer Conference, 1964.

is modified to store the address of the new detail record in its pointer field. The new detail will contain the address of the next record of the chain that had been stored in the prior record.

A new detail will be inserted into its chain according to the ordering rule specified in the data description. In the product structure example to be given, one chain will be ordered in data value sequence. The other chain will be ordered by inserting each new detail record as the first detail in the chain.

engineering parts list

The engineering parts list, or bill of materials as it is frequently known, is the foundation of a manufacturing business. Purchase orders, sales invoices, time cards, and stock tickets are essential; but they all reflect peripheral actions. The product must still be made so that it can be sold.

The parts list and the listed engineering drawings are the original Engineering definition of what the product is. It becomes the Manufacturing description of what has to be used to make the product. It is the Accounting basis for preparing cost studies. Finally, it is the customer's basis for ordering spare parts during the life of the product.

At first glance (Fig. 2) the information content of a parts list is deceptively simple. A single parts list identifies and describes a product. It then lists serially the parts or subassemblies used to produce the product, and indicates the quantity required of each part. Normally each of the items listed on a parts list is also given an item number that is relevant to that particular parts list - - i.e. item 1, item 2, item 3, etc.

A very simple data structure can be used to transfer a parts list onto a computer. A master record can be placed on a punched card or magnetic tape representing the parts list heading and a detailed or trailer record added following the master for each item on the parts list. This is the usual approach taken by file designers in processing this type of engineering information. The serial nature of punched cards or magnetic tape closely approximates the serial geometry of paper, the original form of data processing.

This solution suffers from the same problem that affects the original paper parts list, which in itself was an information processing abstraction of the original product structure that it describes. The original product is a thing made out of things which, in turn, are made of other things. Frequently it requires many hundreds of interlocking parts lists to completely describe an item such as a computer or disc storage unit that a customer would want to buy. This is the product structure which really needs to be represented within a computerized information system. From this structure, a simple parts list can be reconstructed and printed. A report showing every place a part is used (where-used list) can be printed. The effect of producing a given quantity of an end product can be reflected down to the lowest level in the product structure through a parts explosion procedure.

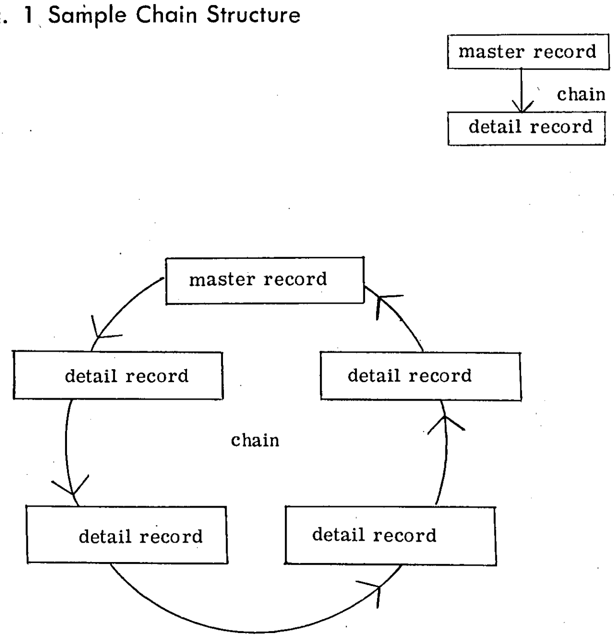
Random access data storage units, such as disc files drums, and magnetic loops, provide an opportunity to build and process information structures of more than one dimension. Given this ability, a fresh new approach may be taken in organizing product structure. A systematic review of the information content of a parts structure is required.

kinds of parts information needed

Fig. 3 (p. 38) shows a schematic representation of the product structure built from the parts lists of Fig. 2. In this illustration seven material items and seven relationships between pairs of material items are shown. Boxes represent material items, lines designate the quantity relationship. Numerals with the relationship lines denote quantities of each respective item required for the manufacture of other items.

For example, the diagram shows that Material Item B requires two of Material Item D, 12 of material Item R, and three of M. In normal manufacturing practice, any given material item may require quantities of from one to 1,000 other material items for its assembly. Of course, if the material item is purchased completely assembled, it may not require any other material item for its manufacture. Material items F, G, and T are examples.

Fig. 1 Sample Chain Structure



Note: The arrow is schematically representing the fact that each record contains the address of the next record in the chain.

Fig. 2 Sample Parts Lists

item B

item no	quantity	mat'l. item
1	2	D
2	12	R
3	3	M

item D

item no	quantity	mat'l. item
1	1	F
2	2	G
3	6	T

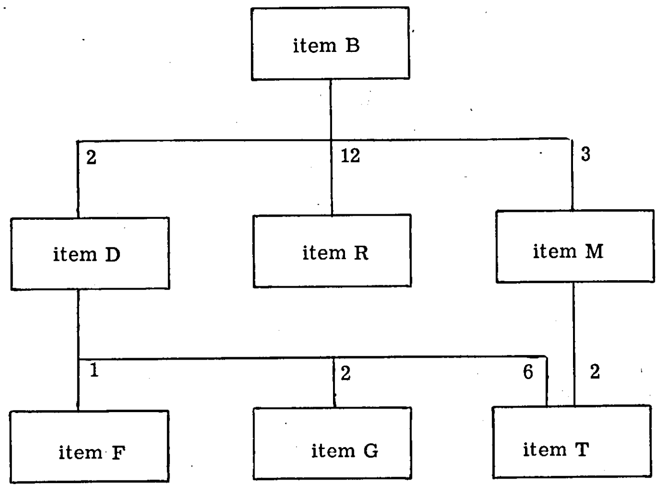
item M

item no	quantity	mat'l. item
1	2	T

In the discussion of material items, it should be noted that the term *higher-level* is applied to a material item which is being produced in the manufacturing operation; *lower-level* is the term for one being consumed in the manufacturing process. The former might be the drive mechanism of a tape transport; the latter a spindle or motor used in its manufacture.

Any given item may be required for use in one or more higher assemblies. Item T, for example, is used by both

Fig. 3 Product Structure



Items D and M. Another item may have no requirements; Item B would be such a piece.

In an actual manufacturing situation, 10,000 material items are frequently found to exist, and 40,000 items are not unusual. The total number of quantity relationships will average from one to three times the number of material items.

From the foregoing discussion of product structuring, it may be seen that: (1) Two different units of information are involved in a parts structure—namely, material items and quantity relationships; (2) Quantity relationships between the material items create a complex network describing the assembly process; and (3) These networks are typically very large in size, comprising tens of thousands of material items and relationships.

Two records will be designed to store information about the parts list structure. The first is called a *material item record*. This will contain two data fields: the *material identification* and the *material description*. The second record is the *submaterial* record. This represents a quantity relationship between two material item records. It contains two data fields, *quantity required*, and *item number*. The *quantity required* field is self-explanatory. The *item number* field is used to number the several submaterial records relating to a given parts list. These numbers, when combined with the material identification of the higher-level material record, serve uniquely to identify each submaterial record.

Two chains have been established to control the association of these records. The first, known as the "call-out" chain (Fig. 4), has as its master record the material item record. This chain will contain as many submaterial records as required to specify all the quantities of lower level items necessary to manufacture the material item designated by the master of the chain.

It should be noted that as each material record is stored, it is automatically made the master record of a call-out chain. Of course, no detail records would be in the chain at that time. Still, there would be a chain field in the record containing the address of the next record in the chain. This next record address would be the address of the material item record itself.

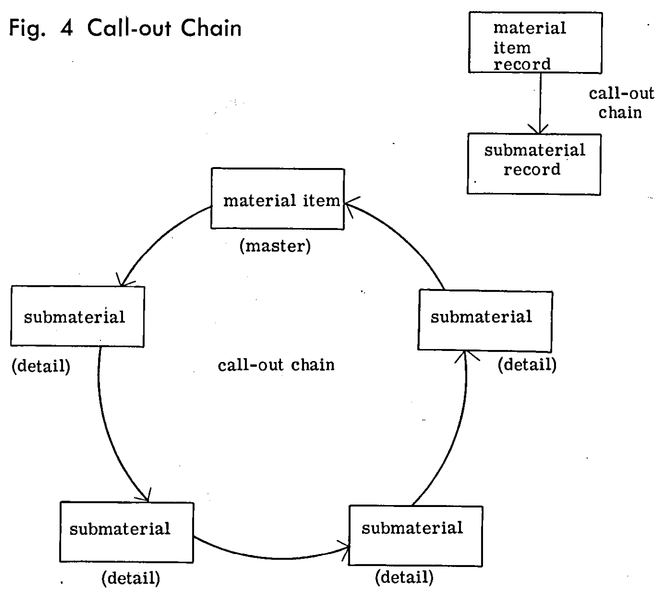
Whenever a new submaterial record is to be stored, it must select one material item record from the thousands of existing material item records to be its appropriate master. It will select the material item record specified by the material identification number which was supplied in the input along with the item number and the quantity required. If for some reason the material item record cannot be retrieved, then an error is indicated and the storage process terminated.

Once the correct material item record is retrieved, it is necessary to determine whether a submaterial record with the same item number is already in the call-out chain. If a duplicate record is detected, the storage process is terminated and an error noted. If the new record is not a duplicate, it will be linked into its proper place in the chain, based upon the sequence of item numbers. The call-out chain is a data-sequenced chain.

A second chain, the "where-used" chain, defines all of the relationships for a material item record where that material item is used in the manufacture of a higher-level material item. The material item record is the master record of this chain too. The submaterial record is again the detail in this chain. In this way the submaterial record creates, via the two chains, the desired relationship between two different material item records.

The small diagram in the upper right corner of Fig. 7 is the record structure diagram. It specifies that there

Fig. 4 Call-out Chain



are two record types (the material item record and submaterial record) and two chains relating them (the call-out chain and the where-used chain). The direction of the arrows indicates that the material item record is the master record of both chains. However, it should be noted that a particular submaterial record always has two different material item records (same record type) as the master records for its where-used and call-out chains.

The submaterial record selects its master record (material item record) in the where-used chain, based upon a second material identification known as submaterial identification. The submaterial identification field is the fourth field supplied with the input. There is no need to sequence the where-used chain; therefore each new submaterial record is inserted as the first detail record in the where-used chain at the time of storage. This form of insertion uses the least amount of computer time.

Fig. 5 shows a sheet of I-D-S/COBOL data definitions describing the material item and submaterial item records. Fig. 6 is a companion record layout sheet showing what is stored in each character of each record. These data definitions generally follow the COBOL data descriptions, with the addition of certain Integrated Data Store statements necessary to guide the automatic storage and retrieval functions.

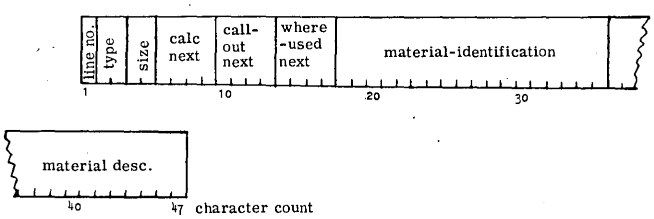
The material item record is specified as a calculated record by the statement, "RETRIEVAL VIA CALC CHAIN." The statement, "RANDOMIZE ON MATERIAL-ID" identifies the data field that will be operated upon by a randomizing routine to derive the location where a given material item record would be normally stored. The Calc Chain is a special chain designed to link together all of the records that randomize to the same location. Thus a scan of all the records in a particular Calc Chain would give access to all the records that have randomized to a location, even though an overflow situation prevented the record from being stored in its normal place.

Fig. 5 I-D-S/COBOL Data Definitions

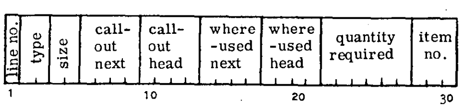
```
DATA DIVISIØN
IDS SECTIØN
MD MATERIAL-FILE; PAGE CØNTAINS 2880 CHAR.; FILE CØNTAINS 8192 PAGES.

01 MATERIAL-ITEM; TYPE IS 100; RETRIEVAL VIA CALC CHAIN.

02 MATERIAL-ID; CLASS 18 ALPHANUMERIC.
02 MATERIAL-DESC; CLASS 12 ALPHANUMERIC.

98 CALC CHAIN DETAIL; RANDØMIZE ØN MATERIAL-ID.
98 CALL-ØUT CHAIN MASTER.
98 WHERE-USED CHAIN MASTER.

01 SUB-MATERIAL; TYPE IS 200; RETRIEVAL VIA CALL-ØUT CHAIN.

02 ITEM-NØ; CLASS 3 NUMERIC.
02 QUANTITY-REQUIRED; CLASS 6 CØMPUTATIØNAL-N.

98 CALL-ØUT CHAIN DETAIN; SELECT UNIQUE MASTER; MATCH-KEY IS
   MATERIAL-ID; CHAIN-ØRDER IS SØRTED; DUPLICATES NØT ALLØWED;
   ASCENDING SØRT-KEY IS ITEM-NØ; LINKED TØ MASTER.
98 WHERE-USED CHAIN DETAIL; SELECT UNIQUE MASTER; MATCH-KEY IS
   SUB-MATERIAL-ID; SYNØNYM SUB-MATERIAL-ID EQUALS MATERIAL-ID:
   CHAIN-ØRDER IS FIRST; LINKED TØ MASTER.
```

Fig. 6 I-D-S File Companion Record Layout

Material-item Record



Submaterial Record



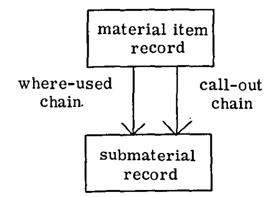
The data "page" is the basic addressable unit of mass memory, which is the location where a record is stored. Only complete pages are transmitted between the computer and its mass memory. Each record's address consists of its page number plus the line number assigned to the record within that page. The data description in Fig. 5 specifies a particular file with 8,192 pages of storage capacity with each page large enough to store 2,880 characters of data. The size of the page and number of pages are specified by the file designer to gain the best performance for the specific mass memory device he is employing.

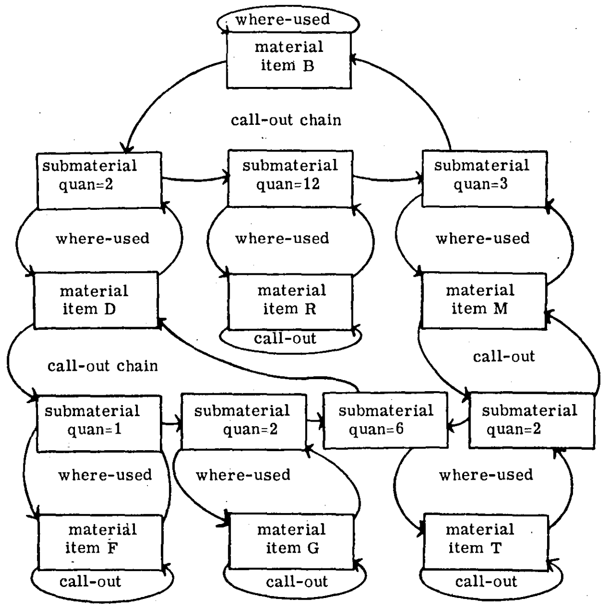
The Integrated Data Store will automatically attempt to store a new submaterial record in the same page as its master record in the call-chain. In normal operation, most of the submaterial records will be stored in the same data page as the material item record, or in the adjacent one. Therefore, no disc time, or only latency time, is involved in retrieving all the records in the call-out chain for a particular material item record. The desire to store a submaterial record near its call-out chain master is specified by the statement in the data description, "RETRIEVAL VIA CALL-OUT CHAIN."

The level 98 entries in the data division specify the relationship of a record to a chain. The initial clause of a level 98 entry names the chain and indicates whether the record is associated with the chain as a master or a detail. In the case of a detail association, the rules for selecting the particular chain master and inserting record into the chain are also specified.

The series of parts lists that made up Fig. 2 were translated into the product structure shown in Fig. 3. This same product structure, when expressed through the Integrated Data Store as records and chains, would appear as the information structure of Fig. 7. A material item record is stored for each material item. A submaterial record is stored for each quantity relationship expressed. Finally, the call-out chains and where-used chains tie together the material item and submaterial records to achieve the information structure which exactly models the original product structure.

Fig. 7 Information of Figs. 1 and 2, organized into material item records and submaterial records, and chained together to create a product structure.





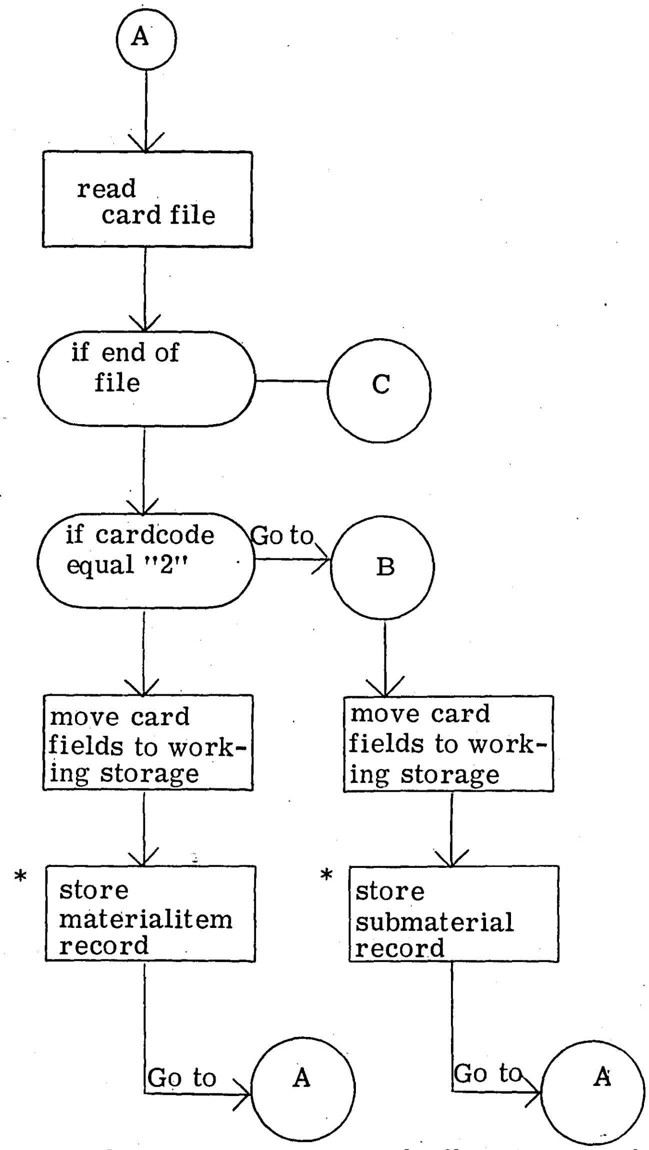
the file-building routine

The building of a file such as the one expressed by the data description of Fig. 5 and the actual records and chains of Fig. 7 would be straightforward. Two different input cards would be designed. The first one would contain a material identification and material description. Its function would be to create a new material item record. For control purposes, this card will contain a card code of "1." A second card would contain the information required to store a new submaterial record. Its card code would be "2."

Fig. 8 is the flow chart of the file-building routine that would read these input cards and store the indicated material item records and submaterial records. It should be noted that all of the functions of finding space to store a new record, initializing chains for master records, and inserting detail records in chains is automatically carried out during the execution of a STORE command. The particular action to be taken is dependent upon the data description of the record to be stored.

In a comprehensive file maintenance routine, additional input card formats would be established for the specification of record modification and deletion functions. I-D-S statements such as "RETRIEVE SUBMATERIAL RECORD, REPLACE QUANTITY-REQUIRED FIELD" and "RETRIEVE MATERIAL ITEM, DELETE" would be used to direct the Integrated Data Store to carry out the file maintenance functions required.

Fig. 8 File Building Routine Flowchart

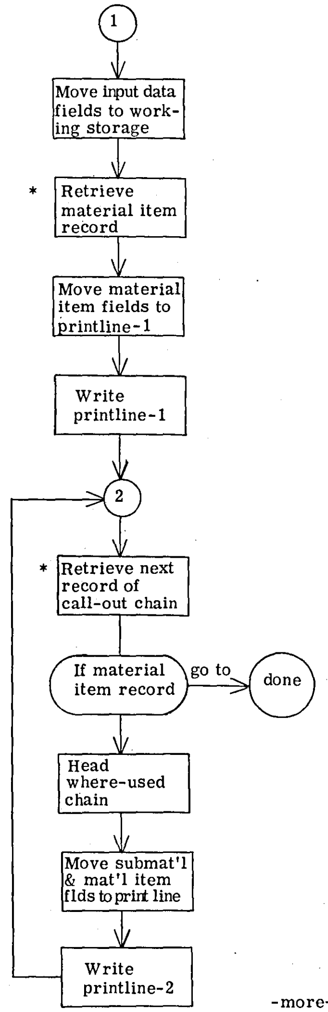


It will be recalled that the purpose of building the file in the first place was to permit the subsequent production of parts lists, where-used lists and parts explosions. A flow chart of the steps necessary to accomplish the preparation of a parts list report is shown in Fig. 9.

A parts list report includes an initial print line (printline-1) containing the material identification and description of the material item for which the report is being prepared. It also includes as many detail print lines (printline-2) as there are items on the parts list. There will be one detail print line for each submaterial record which is a detail in the call-out chain. This detail line contains the item number, quantity required, material identification, and description of the lower-level material item. The item number and quantity required come from the submaterial record. The material identification and the description of the lower-level material item come from the lower-level material item record at the same time the submaterial record is retrieved, through the use of the clause, "HEAD WHERE-USED CHAIN."

This extension of the RETRIEVE command will automatically trace the detail records of the specified chain and retrieve the master record and move its data content to working storage. This action can be accelerated by inserting the clause "LINKED TO MASTER" in the level 98 chain definition of the Data Division. Use of this clause will cause each detail in that chain to contain an additional field. The address of the master record of the chain will be inserted in this additional chain field when the detail is linked into the chain. If this extra pointer is included, the HEAD function can retrieve the master record directly without tracing through all the detail records of the chain.

Fig. 9 Flowchart of Steps Necessary to Prepare a Parts List Report



*Integrated Data Store Functions

Fig. 10 I-D-S/COBOL Statements for Compiling Coding to Produce Parts List Based on Flowchart in Fig. 9

```
STEP-1.
      MØVE CARD-ID TØ MATERIAL-ID, PRINT-ID.
*     RETRIEVE MATERIAL-ITEM RECØRD; MØVE TØ WØRKING-STØRAGE;
          IF ERRØR GØ TØ STEP-4.
      MØVE MATERIAL-DESC TØ PRINT-DESC.
      WRITE PRINT-LINE-1.
STEP-2.
*     RETRIEVE NEXT RECØRD ØF CALL-ØUT CHAIN;
          IF ERRØR GØ TØ STEP-4;
          ØTHERWISE IF MATERIAL-ITEM RECØRD GØ TØ STEP-3;
          ØTHERWISE IF SUB-MATERIAL MØVE TØ WØRKING-STØRAGE:
          HEAD WHERE-USED CHAIN.
      MØVE ITEM-NØ TØ PRINT-ITEM-NØ.
      MØVE QUANTITY-REQUIRED TØ PRINT-QUANTITY.
      MØVE MATERIAL-ID TØ PRINT-SUB-ID.
      MØVE MATERIAL-DESC TØ PRINT-SUB-DESC.
      WRITE PRINT-LINE-2.
      GØ TØ STEP-2.
STEP-3.
      STØP RUN.
```

* Integrated Data Store Statements

Note that the HEAD clause is a convenient means for extending retrieval functions to automatically retrieve the information in the master when required. This information is, in truth, part of the detail record; however, to eliminate redundancy and simplify file maintenance, it is stored in the master record and shared with the other detail records in the chain.

Fig. 10 gives the I-D-S/COBOL procedure division statements which would cause the necessary coding to be compiled to produce a parts list. Asterisks indicate I-D-S commands. The other nine commands are standard COBOL.

The coding to produce a where-used report is similar to that of the parts list report, with the exception of the "RETRIEVE NEXT" command. To produce a where-used report, this command would be changed to read, "RETRIEVE NEXT RECORD OF WHERE-USED CHAIN; . . . HEAD CALL-OUT CHAIN."

product explosion reports

The preparation of a parts explosion report is an important function of a material structure file. It is somewhat more complicated to produce than a parts list and where-used list. However, the I-D-S ability to traverse chains linking the information structure facilitates the preparation of product explosion reports. The myriad pathways of the parts structure make it necessary to do some trail-blazing to avoid losing the route of exploration. An array named "LEVEL-REFERENCE" is used to store the addresses of successive submaterial records as the routine probes downward through the parts structure. The address is used when the bottom level is reached, to back up to the last book and to probe the next branch of the tree-like structure. The array index is a field named "LEVEL." A second array, "LEVEL-QUANTITY," keeps track of the exploded quantity at each book in the structure. Note it uses the same index, "LEVEL." These two arrays need be only as long as the depth of the product structure. The very simple example we have shown has a depth or level of three. Complicated products may have a depth or level of 10 to 15.

Referring back to Fig. 7, the process of explosion would be down from material Item B through the quantity relationship of "2" to Item D, through the quantity relationship "1" to material Item F, then to material Items G, T and R until complete. Fig. 11 illustrates the parts explosion report, based on a requirement for only one material Item (B).

Fig. 11 Simple Parts Explosion Report

Level	Quantity	Description
1	1	item B
2	2	item D
3	2	item F
3	4	item G
3	12	item T
2	12	item R
2	3	item M
3	6	item T

Note that material Item T appears twice in the report because it is used in the manufacture of both material Items D and M. If desired, a slightly more complicated procedure would permit the accumulation of the quantity exploded for these multiple-occurrence items. Programs exist to do level-by-level material requirements explosions as well as cost implosions on the same file.[2]

Fig. 12 lists I-D-S/COBOL procedure statements for carrying out a report preparation for a parts explosion procedure. I-D-S commands are indicated by asterisks. Note that four of the seven I-D-S retrieved procedures are used in this example: "RETRIEVE;" "RETRIEVE NEXT RECORD OF data-name CHAIN;" "RETRIEVE MASTER OF data-name CHAIN," and "RETRIEVE DIRECT."

The field, "DIRECT-REFERENCE" is a communication cell used by the Integrated Data Store. After the execution of each I-D-S statement the address of the record processed is left in this cell. The RETRIEVE DIRECT verb picks up the address of the record to be retrieved in this same cell. A record address as used in this context, and in the context of chain pointers, is made up of the record's page number and line number. These are not hardware addresses.

Fig. 12 I-D-S/COBOL Procedure Statements

```
    STEP5.
        MØVE CARD-ID TØ MATERIAL-ID.
*       RETRIEVE MATERIAL-ITEM RECØRD, MØVE TØ WØRKING-STØRAGE;
            IF ERROR GØ TØ STEP4.
    STEP6.
        MULTIPLY QUANTITY-REQ BY LEVEL-QUAN (LEVEL) GIVING EXPLØDED-QUAN.
        ADD ØNE TØ LEVEL.
        MØVE EXPLØDED-QUAN TØ LEVEL-QUAN (LEVEL), PRINT-QUAN.
        MØVE MATERIAL-ID TØ PRINT-ID.
        WRITE PRINT-LINE-3.
    STEP7.
*       RETRIEVE NEXT RECØRD ØF CALL-ØUT CHAIN;
            IF ERRØR GØ TØ STEP4;
            ØTHERWISE IF MATERIAL-ITEM RECØRD GØ TØ STEP8;
            ØTHERWISE IF SUB-MATERIAL RECØRD MØVE TØ WØRKING-STØRAGE.
        MØVE DIRECT-REFERENCE TØ LEVEL-REF (LEVEL).
*       RETRIEVE MASTER RECØRD ØF WHERE-USED CHAIN;
            MØVE TØ WØRKING-STØRAGE;
            IF ERRØR GØ TØ STEP4.
        GØ TØ STEP6.
    STEP8.
        SUBTRACT ØNE FRØM LEVEL.
        IF LEVEL EQUAL ZERØ GØ TØ STEP9.
        MØVE LEVEL-REF (LEVEL) TØ DIRECT-REFERENCE.
*       RETRIEVE DIRECT;
            IF SUB-MATERIAL RECØRD GØ TØ STEP7.
        GØ TØ STEP7.
    STEP9.
        STØP RUN.
```

* Integrated Data Store Statements

conclusion

Experience to date using the Integrated Data Store shows that its ability to eliminate redundant data can save from 25 to 40% of the space required by conventional file designs. As an example, a material identification number which may be as many as 18 characters in length, need appear only once in the entire file. Normally it would appear in the file once for every time that it appeared on a parts list.

The I-D-S data structuring ability and powerful procedural verbs (STORE, RETRIEVE, MODIFY, AND DELETE) automatically carry out record processing functions which are lengthy, complicated and difficult to program and debug using normal disc file programming techniques. Reductions in time and expense of 25% have already been realized by using the Integrated Data Store to program large integrated business systems.

Operating times have been reduced up to 50% because efficient buffering techniques, data blocking and good data organization are uniformly applied to all I-D-S programs. Implementation schedules and the supply of top-notch programmers are usually too tight to permit hand-coded programs to reach or maintain their potential effectiveness.

The Integrated Data Store received its first thorough testing by General Electric in the summer of 1963 using existing disc storage unit parts explosion routines as test controls. These tests were run on GE-225 computers. Today there are four large integrated business systems pioneering the use of the Integrated Data Store. Several of these systems process their product structure in essentially the form indicated in this article. All of these systems are on GE-215, 225 or 235 computers.

The General Electric Computer Dept. is currently implementing Integrated Data Store Systems for the GE-400 series and 600 series computers. These systems will operate in conjunction with the GE COBOL processors and will be available this coming summer. ■

[2]General Electric Computer Dept.'s publication CPB-279P, "Disc Storage Access Parts Explosion," documents other means of carrying out parts explosions.

HYPHENLESS JUSTIFICATION

typesetting breakthrough

by GEORGE E. KUNKEL and TILMON H. MARCUM

While an increasingly large number of computer and printing organizations continue to struggle with the hyphenation problem in computer produced text, a small team of specialists in the Central Intelligence Agency has developed a novel approach which is amazing in its simplicity and which may make the troublesome end-of-line hyphen a thing of the past in computerized photocomposition.

The success or failure of present computerized book composition systems hinges largely upon the computer's ability to provide correct end-of-line word divisions required for justification. Several years and hundreds of thousands of dollars have been spent in attempting to develop dictionaries and logic which will attain the necessary accuracy required for high quality composition. Existing computer systems cannot yet equal the accuracy of the average keyboard operator in hyphenating end-of-line words although a fairly high degree of accuracy is obtained in some cases. Accuracy is needed in computer composition because of the problem of correcting errors and the constant demand for greater speeds.

With the present state of the art, the printer must choose between a system obtaining high accuracy with proportionately higher computer costs or a less sophisticated system providing a lesser degree of accuracy with the attendant error cost factor. Any system permitting errors poses the problem of new errors being introduced when corrections are required.

The idea of eliminating the end-of-line hyphen is not new. Some newspapers and printers now justify text without hyphens by the use of excessive interword spacing and fixed letter spacing or a combination of both. Some publications appear with an unjustified single or multi-column format. Unfortunately neither of these systems provides acceptable typographic quality for book production.

A primary rule in typesetting is to avoid hyphens wherever possible since they destroy continuity in reading. It is obvious, then, that the real need is for a simple plan which eliminates the end-of-line hyphen without sacrificing typographic quality. Uncle Sam's team feels that they have solved this problem by the use of a variable set size technique on a line-for-line basis.* In simpler terms, this means that a sort of "coefficient of expansion" or contraction is applied to the proportional spacing between characters in each line of text. The line is thus expanded and contracted without destroying the proportional values of the individual character as is the case with fixed letter-spacing. The variation in appearance of the lines of text produced by this method is sufficiently subtle to remain unnoticed by the average reader. The ability to expand and contract provides sufficient latitude in justification so that the need for end-of-line word division is rare. The computer programming and processing which is required for variable set size justification is many times simpler and less costly than that required for end-of-line word division and hyphenation.

In a unit font each character is assigned a proportional unit value, which is valid regardless of the set size. The specified line measure can then be stated in units for each set size. Therefore the computer can accumulate units as it passes through four overlapping (set sizes) zones of justification in which an interword space may be selected for the end of line. This simple logic for line justification thus eliminates the requirements for stored dictionaries for word hyphenation, programmed logic approaches, or a combination of the two, prefix and suffix tables, and stripping and reconstituting routines.

The Central Intelligence Agency prints in its own facilities a number of high quality book-type publications. These publications are set in type on Intertype and Monotype machines and are printed by offset from plates made from positive Mylar proofs pulled directly from the type. For the past five years the majority of this composition has been done on Model F4 Intertype machines operated by TTS tape.

About a year ago, the agency printing engineers and computer specialists began studying the possibility of doing page composition by photocomposing from computer-prepared tape. This study developed the feasibility of this type of composition and a thorough investigation was made of all available photocomposing equipment. After a great deal of study a Model 513 Photon has been obtained for this composition. A primary reason for this selection was the 513's capability of changing set sizes from codes inserted into the computer-prepared tape.

The printing engineers and computer specialists began the job of programming an IBM 1410 computer for this typesetting job. Agency personnel had talked with other printers and computer personnel and had visited numerous printing plants in their investigation of the problems involved in this method of typesetting. Since they were interested in page composition this aspect of the problem received most of the initial attention. It soon became apparent, however, that the primary problem involved in this type of computerized composition was not in page makeup but rather end-of-line word division and hyphenation. Consequently the computer specialists and printing engineers gave consideration to the number of known methods of handling this problem. It was apparent that the end-of-line hyphenating problem would require considerable programming time and computer capacity. Further, it was found that hyphenating inaccuracies, computer capacity, loss of speed, cost of dictionaries, etc., were problems not yet overcome.

Before getting into programming for hyphenation, the agency personnel began a thorough study of any alternatives to end-of-line hyphenation. Since the 513 Photon had been selected for the composing job because of its tape-operated set size changing capability, the agency engineers felt there was a possibility of using this capability for justification without end-of-line hyphens in average book composition. Further study indicated that hyphenless justification of practically any measure of composition was possible by varying set sizes of individual lines.

The varying of set sizes permits a delicate method of proportional letter spacing. Numerous sample pages have been set in which four different set sizes are used and the resulting typography is satisfactory for book composition of relatively high quality. Since the program is not yet operative the described technique was simulated on a Monotype keyboard and the sample pages set on a Monophoto caster.

The system of employing proportionate letter spacing by set size changes will work as follows:

The computer is being programmed to compute for end-of-line decisions utilizing two, three, four or five set sizes close enough in size to each other to be inoffensive typographically and yet disparate enough to significantly increase justification range. The computer will arrive at end-of-line decisions for all set sizes involved, choose the set size in which an interword or other natural line ending code (period, em quad, compounding hyphen, etc.) occurred in the justification range, and incorporate in the output tape the appropriate set size codes to accompany the line.

Many rules and variations in set sizes and data blocks can be developed but the ultimate result is that hyphens can be eliminated or reduced to the degree that they would no longer pose a problem to the computer, the printer, or the reader.

Adoption of this system of typesetting will:

1. Reduce computer processing time.
2. Simplify hyphenation logic and reduce initial programming time and costs.
3. Enable the use of less expensive computer equipment.

This system of phototypesetting from computer-prepared tape has the advantage of completely eliminating the need for the complicated programming now in use for end-of-line hyphenations. This in many instances would indicate that a smaller computer or less peripheral gear may be used for relatively complicated composition. The drastic reduction in the correction problems caused by improper hyphenation is another advantage which many printers will welcome. This is particularly true in the case of photocomposition and its attendant correction problems. Obviously the computer when processing data for this system will need a routine to take care of the inevitable line which will not succumb to the set-size-change method. This routine need only provide for enough expansion and contraction capability in the two lines involved to allow for application of a human decision. A simple solution would be for the computer to produce the lines involved by inserting a hyphen at any point in the troublemaking word which would allow the median set size and a median width interword space. Even with this method the division may be correct, and at least there would always be sufficient latitude for adjustment.

The agency plans to edit tape on the 1410 computer by proofreading one or two computer printouts prior to creation of final tape for use on the photocomposing machine. Thus the rare instance where an end-of-line hyphen would be necessary can be determined from the printout

---

*Set size determines the overall horizontal dimension of the space assigned to a character—it includes space for separation from adjacent letters. Set size also expresses the relationship of one type font to another. The size relationship of one letter to another is expressed in "units of relative value," based on the size of the em (18/18). Therefore the horizontal dimension for a letter is determined:

$$\text{URV} \times \text{SS} = \text{Horizontal dimension}$$

$$\text{Point Size}\left(\frac{1''}{72}\right) = \text{Vertical dimension}$$

Fig. 1

b. Close Support Operations. The lack of concealment, great distances involved, and mobility of forces—each characteristic of desert operations—necessitate increased emphasis on the employment of tactical air in close support of ground operations. The lack of natural cover and concealment makes for ease of target location and provides better than normal conditions for high-level bombing. Installations stand out due to the contrast between regularly shaped objects and the open barrenness of the desert. Movement is readily apparent from the air because of the dust created and the prominence of shadows. Low-level attacks are handicapped by lack of covered approaches; however, this is offset by the increased visibility which enables aircraft to initiate their firing runs from a greater distance. This improved visibility, coupled with the rapid movement, lack of prominent terrain features, and the fluid situations characteristic of desert operations, necessitates positive action to identify friendly

Fig. 2

b. Close Support Operations. The lack of
concealment, great distances involved, and mobility ●—10
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The lack of natural cover and concealment makes
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JUSTIFICATION . . .

and the necessary correction incorporated in the final tape. It should never be necessary to correct hyphenation after the page has been set.*

The relatively high quality of composition possible by this method is illustrated by the accompanying samples. Fig. 1 shows a column of normal composition, 10-point Modern, 19 picas, one set size. This normal composition in a relatively wide measure (19 picas) requires six end-of-line hyphens. Fig. 2 is the same composition using variable set sizes of 10, 10½, and 11. This method of composing eliminates all end-of-line hyphens—the abnormal lines indicated by bullets, and the set size also indicated. Quality of the composition is good, and the variations in letter spacing are not noticeable to anyone not looking for them. It appears that readability of copy is much improved.

Fig. 3 is an example of the hyphenless technique on an 11-pica measure in 8-point type, using three set sizes—7½, 8, and 8½. Eight set was considered normal. Indicated by bullets in Fig. 4 are those lines which used other than eight as the set size. ■

*The authors are indebted to Robert D. Hicks, Ballard Jamieson, and Robert W. Pearson for guidance and assistance during the evolution of the system described here.

Fig. 3

The American prairies are of two kinds. Those which lie east of the Mississippi are comparatively small, are exceedingly fertile, and are always surrounded by forests. They are susceptible of high cultivation, and are fast becoming settled. They abound in Ohio, Michigan, Illinois, and Indiana. They labor under the disadvantages of a scarcity of wood and water—evils of a serious character, until art has had time to supply the deficiencies of nature. As coal is said to abound in all that region, and wells are generally successful, the enterprise of the emigrants is gradually prevailing against these difficulties.

The second description of these natural meadows lies west of the Mississippi, at a distance of a few hundred miles from that river, and is called the Great Prairies. They resemble the steppes of Tartary more than any other known portion of the world; being, in fact, a vast country, incapable of sustaining a dense population, in the absence of the two great necessaries already named. Rivers abound, it is true; but this region is nearly destitute of brooks and the smaller water courses, which tend so much to comfort and fertility.

The origin and date of the Great American Prairies form one of nature's most majestic mysteries. The general character of the United States, of the Canadas, and of Mexico, is that of luxuriant fertility. It would be difficult to find another portion of the world, of the same extent, which has so little useless land as the inhabited parts of the American Union. Most of the mountains are arable; and even the

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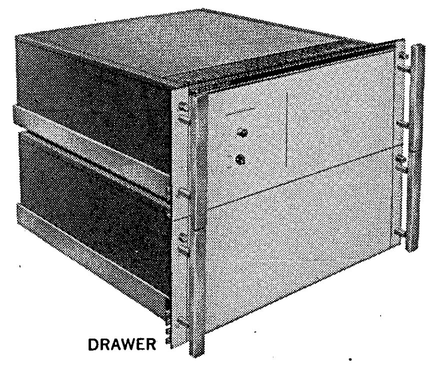
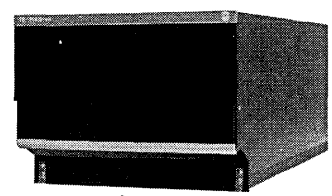
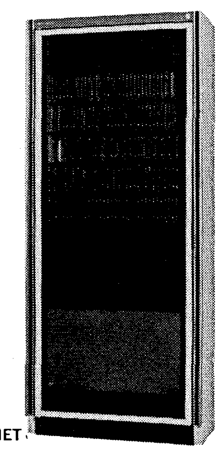


DRAWER



AIRBORNE



CABINET

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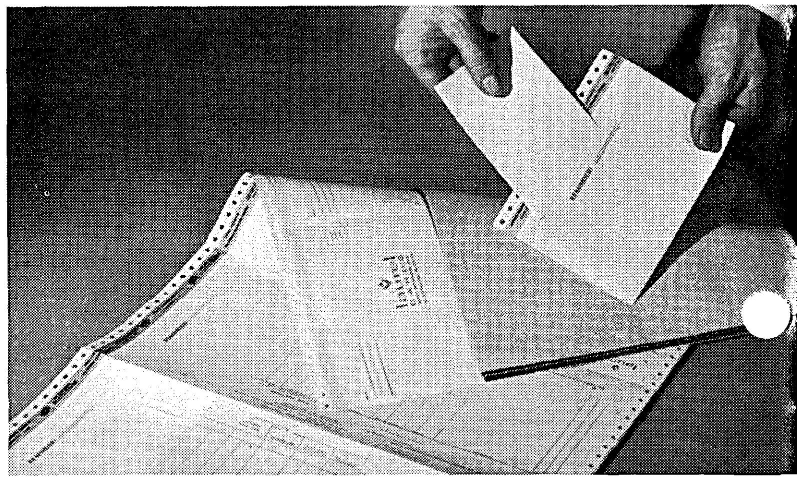

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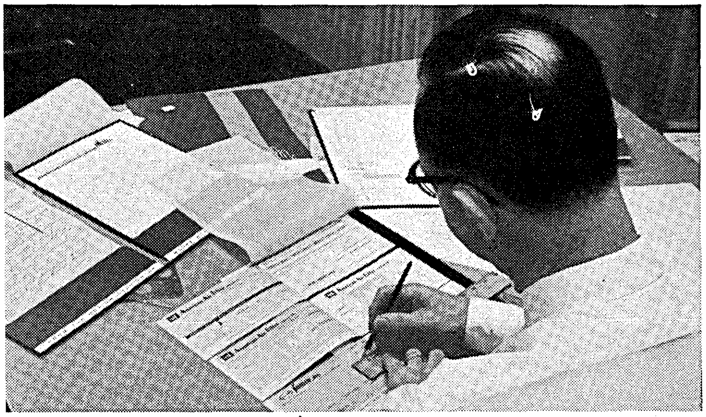

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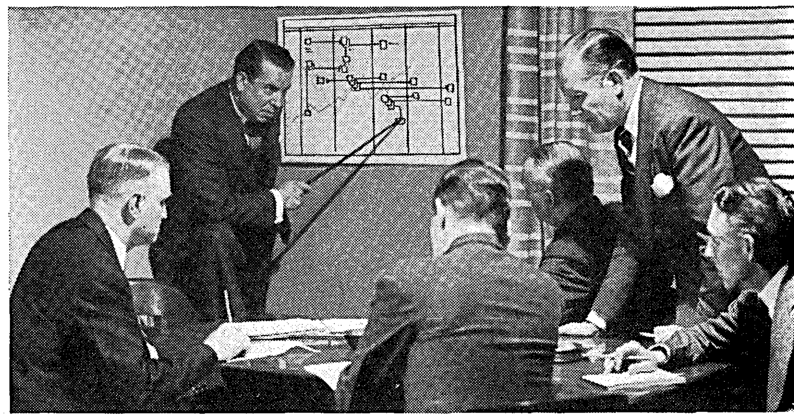

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CIRCLE 22 ON READER CARD

PROGRAMMING 360-CLASS MACHINES

early reactions

bv MARTIN E. HOPKINS

With the announcement of the Spectra 70 computers by RCA, substance is given to the rumors that several manufacturers will build machines that share a set of order codes with the IBM System/360. These computers will have similar features, such as variable length instruction formats and data structure. They will also emphasize the ability to "plug in" a wide variety of I/O devices which will look the same to the stored program.

Man-machine communication, multi-programming and multi-CPU operation will be common with the aid of advanced software. Whether the 360 class machines will share a common set of software is a question I leave to the future . . . and to the patent lawyers. For the present, however, programmers need to know more than the information which is available in basic manuals and sales literature in order to make effective use of these computer systems.

With delivery dates for most users still some time away, actual programming and debugging experience on 360 class machines is, of course, rare. However, for the past year, more than 40 programmers and analysts at Computer Usage Company have planned, programmed and checked out a major software package for the IBM 9020, a 360 class machine. This package includes a monitor, I/O system, assembler, relocatable loader, math and general purpose library, various edit programs and a compiler. A debugging system was included and debugging has been accomplished on an IBM 360/40. The variety of coding was extensive, including the use of I/O, editing, fixed-point decimal, fixed-point binary, floating point and data manipulation instructions. The experience of our programmers ranged from 10 years and a dozen machines to six months work on a single machine; their backgrounds included commercial, scientific, systems and real-time applications. This article is based on our experience in implementing this project; however, we think many of these comments will be applicable to other 360 class machines as well.

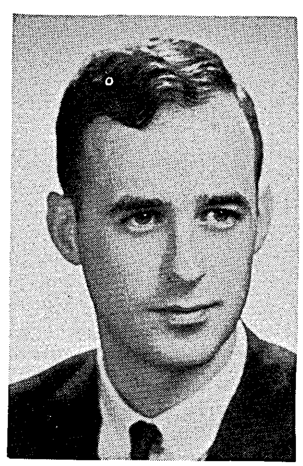
A convenient starting point in this discussion is the importance of using a monitor.

monitor

Large scale users are accustomed to trading some of core storage for the convenience and flexibility gained by using a monitor. With the 360 class computer smaller users will also be introduced to the "joys" of monitor life because it is indispensible for maximum utilization of the hardware. In fact, the 360 class machine should be thought of as a hardware and software (monitor) combination. The reason for this lies in the basic design of the hardware, which allows for numerous interrupts as well as the complexity of a completely asynchronous I/O. The concept of a continuous controlled operation results in many unusual situations which are handled by subroutines initiated by interruptions, which are in turn initiated by the hardware, the problem program or the monitor. For example, if the operator manually spaces the printer to the next page the procedure he follows will probably result in an interrupt which must be identified, acted on, and then control must be returned to the problem program.

True, the hardware allows a much wider range of error detection than most present machines. However, this advantage is somewhat offset by the necessity to pinpoint the exact cause of an error by programming. In addition, interrupts can occur for such reasons as overflow, invalid addressing, or the operator pushing the attention button. When you consider all that the monitor must do, the better part of valor is certainly to use a standard monitor.

Actually, the machine is designed to facilitate the use of a monitor. There is a monitor mode, as distinguished from the problem mode. Certain instructions, mainly I/O, can be executed only in the monitor mode; these are termed "privileged instructions." Communication between



Mr. Hopkins is a senior analyst with Computer Usage Co. Inc., New York City, and head of the firm's Mt. Kisco, N.Y., facility. For the past year, he has led a team of analysts and programmers in writing software and programs for the 360. He has also worked on many projects in systems programming, including the design and implementation of COBOL, as well as FORTRAN compilers and other software and utility systems.

the problem programmer and the monitor is through a Supervisor Call (SVC) instruction. An SVC causes a programmed interrupt, and the monitor takes action on the basis of a parameter in the SVC instruction. Typical actions might be to stack an I/O request, take a dump, begin multiprogramming at a specified address, or request an operator response. The monitor itself can be protected from alteration by a memory protection feature. The problem programmer has no way of executing privileged instructions, except indirectly through the monitor.

the instruction set

The full instruction set available to the problem programmer consists of 131 instructions. In general, most users will want a full set, with the exception of commercial users, who may not want floating point. As with all computers, there are some coding problems; however, it is seldom necessary to have lengthy or slow code (as it is on some word machines), when odd size fields are manipulated, or on character machines, when extensive arithmetic or long moves are attempted.

The 360 class machine does impose one critical consideration on the programmer: more than the usual amount of planning. There are various approaches to almost every coding problem on these machines; a hasty decision or short-cut strategy might lead to unexpected difficulties. For example, when a programmer decides to use decimal rather than binary arithmetic to save conversion time, he cannot conveniently use the computed quantities for address arithmetic because the internal addressing is binary. The choice of radix (binary or decimal) is even more complex and will be considered in detail after the nature of the registers is explained.

register usage

Good programming strategy depends on understanding the registers. There are 16 fixed-point registers, each 32 bits long. The odd- and even-numbered registers are paired for double-length shifts, multiplies, etc. Registers "1" and "2" are implicit operands in some operations, and register "0" is restricted in its use. All the registers can be used as accumulators. The situation is similar to that for the 705-7080, where the ASU's are used as temporaries, counters, etc. A good program must keep many intermediate results in the registers, and thus minimize "saves" and "restores." In addition, the registers can be used as index registers and for linkage.

A 360 class instruction allows only 12 bits for the address; these 12 bits are called the displacement. This means only 4,096 bytes can be addressed directly. Four bits are provided to specify a base register, and the *contents* of this register are added to the 12-bit displacement to obtain an effective address. Some instructions allow the specification of a second register for address modification; this is the index register. Thus, an effective address is formed by *adding* the 12-bit displacement to the contents of the registers specified in the base and index fields. When specified as a base or index, the contents of register "0" is zero. So, in order to address anything beyond the first 4,096 bytes, a base or index must have been loaded. This is a critical consideration in programming; the more bases loaded, the fewer registers available for indexing or use as temporaries. There is an added difficulty in planning due to the even-odd pair arrangement and the special characteristics of registers "0," "1," and "2."

The register problem also extends to the floating-point registers. The four floating-point registers are separate from the 16 fixed-point registers. Only floating-point operations may be performed in them. If there is an operand in a fixed-point register which is to be operated on using floating-point instructions, it must first be stored and then loaded into a floating-point register. This is sometimes inconvenient and makes fixed-float conversions expensive.

Linkage between subroutines will also affect overall register assignment, for it is at this time that one set of registers must be saved and a new set loaded. In addition, one would like to use the registers to transmit either the arguments themselves or their addresses to the called subroutine. This is practical if there are only one or two arguments, but when there are many arguments, it is usually better to have address constants after the "Branch and Link" (BAL) instruction.

Because of the many techniques available, a situation is likely to develop where, in the interest of speed, each programmer may use a different linkage method. At the risk of sometimes producing something less than optimum code, a standard linkage should be decided on and then all programmers be required to use it. This will facilitate communications and greatly reduce coding errors.

program organization

Perhaps our greatest surprise was to discover that programmers had very few problems handling register allocation and use, once they accepted the fact that it required a little prior planning. A surprising number said they could have produced as good code with eight registers as with 16.

The following are some helpful rules in planning register usage:

(1) Break programs into subroutines, each covered by a base register.
(2) Two registers should be permanently reserved for linkage, although they can be used for general purposes between calls.
(3) Subroutines should be assembled separately, and only communicate in a standard manner, either through passing arguments or addressing a common communications area.
(4) Data, constants and temporaries should be kept together for convenient coverage by a base. Large sets of data, such as tables and arrays, which must be addressed via indexing, should also be kept separate.
(5) It is usually sufficient to reserve one base register for data and one for instructions within any subroutine.
(6) Registers should be specified symbolically, so that when register assignments must be changed, it can be done by reassembly.
(7) Save one register for an emergency. A small change in logic may cause a complete rewrite in a tight routine because a register is not available.
(8) The first 4,096 bytes should not be addressed directly; some system probably expects to use them.

It should be mentioned that the writer of a reasonably small program can ignore the base and displacement problem if he desires. Eight registers loaded at the beginning of a program (and never altered) will allow him to address every byte in a 32K machine. This leaves eight registers for accumulators, index registers, and linkage. This technique, however, does not make the most efficient use of the machine.

data layout

The other broad area requiring careful planning is data layout. Early in the analysis stage, it must be decided if numeric data are to be decimal or binary. Each radix has advantages and disadvantages. Binary data is more compact, is operated on faster, and can be used for address

TYPICAL 360 CLASS INSTRUCTIONS

Add Storage to register

5A	R_1	X_2	B_2	D_2
0	8	12	16	20 … 31

The word at the effective address computed by adding the contents of the registers specified by the X_2 and B_2 fields to the value in the D_2 field is added to the contents of the register specified in the R_1 field. The sum is placed in register R_1. 5A is the hexadecimal representation of the operation code. The storage address must be on a word boundary.

Load single precision register to register

38	R_1	R_2
0	8	12 … 15

The first 32 bits of the floating point register specified in the R_2 field are placed in the first 32 bits of the floating point register specified in the R_1 field. Thirty-eight is the hexadecimal representation of the operation code.

Move characters storage to storage

D2	L	B_1	D_1	B_2	D_2
0	8	16	20	32	36 … 47

The characters beginning at the effective address computed by adding the contents of the register specified by the B_2 field to the value D_2, are moved to the effective address computed by adding the contents of register B_1 to the value D_1. L + 1 characters are moved. D2 is the operation code.

Three byte (character) field

Byte 1	Byte 2	Byte 3
0	8	16 … 23

Five decimal digits and sign in packed format

digit 1	digit 2	digit 3	digit 4	digit 5	sign
0	4	8	12	16	20 … 23

Half word fixed point number

S	Value
0	… 15

Full word fixed point number

S	Value
0	… 31

Single Precision Floating Point

S	characteristic	mantissa
0		8 … 31

Double Precision Floating Point

S	characteristic	mantissa
0		8 … 63

computation. However, it must be positioned on a word boundary and requires conversion when the input is unedited. Decimal instructions have two storage addresses, allow for variable length fields, and do not require a register as an operand. However, because decimal instructions may not be indexed, an extra base is often needed. Instructions to convert binary to decimal and vice-versa are available. In most cases we have found that binary data produces the most efficient code.

Standard character size is eight bits (termed a byte), and decimal arithmetic instructions operate on data packed two decimal digits to each byte. This means that in order to add to a field in eight-bit format, it must first be packed, then added to, and finally unpacked. It is possible to save storage and execution time by keeping decimal data in packed format so it can be operated on without packing and unpacking. Again, helpful instructions are provided to pack or unpack decimal data in one instruction when it is necessary to go from one format to another.

There are variable-length "Move" and "Compare" instructions which allow manipulation of odd-size fields not necessarily on a word boundary. They are a great help in coding, and they will operate on binary data. IBM 1400-series programmers should remember that the word length is not automatically built into the data structure. When the word size is carried with the data, it must be a binary count or a special control character. The former can be used to modify an instruction; it is necessary to scan for the latter, but the "Translate and Test" (TRT) instruction facilitates finding a specific character in one instruction. In general, though, the variable-length properties of this machine are less flexible than those of the 1400 series. This may be a good thing because instruction-controlled word length, as found in the RCA 301 or STRETCH, allows easy debugging and produces good code.

The variable-length "Move" allows transfers of up to 256 bytes. This limit can be inconvenient, but it points up a crucial fact about the organization of data. Long moves of data are often unnecessary and should be avoided. Base-displacement addressing allows one to simply load a new base in a register rather than to go through the more time-consuming movement of data to a work or output area. Of course, this sort of coding requires more organization by the programmer.

floating point arithmetic

Each of the four floating-point registers can hold a 64-bit, double-precision floating-point number. Single-precision operations can be performed in the left half. A single-precision floating-point number has a sign, seven-bit characteristic and a 24-bit mantissa. The characteristic is a power of 16, not a power of two, so a number is normalized when any one of the left-hand four bits of the mantissa is a one bit. This means up to three bits can be lost in normalization; thus, the number may have only 21 bits of accuracy. That is a little more than six decimal digits. The 1107 and 7090 give over eight digits.

It may be that most scientific computation will be done in double-precision. In that case, a 56-bit mantissa will give over 15 decimal digits of accuracy, which should satisfy almost everyone. On the larger and faster systems, where most such computation will be done, the time to execute double-precision instructions will be the same or only slightly greater than it would be for single-precision.

debugging

There have been predictions that 360 class programs would be a "nightmare to debug." We have just not found this to be so, even though we had no debugging aid except for a hexadecimal dump. Since the internal addressing is binary and the natural way to group bits is by fours, dumps and listings show locations and storage in hexadecimal. The convention for representing hexadecimal is $0_{10} - 15_{10}$ are equal to $0_{16} - F_{16}$. Surprising as it may seem, programmers learn to do hexadecimal addition and subtraction very quickly, although in most cases it is not necessary, even with relocated programs, because base-displacement addresses need not be modified when the routine is relocated. The tendency to have small subroutines with only local references makes most addresses easy to find by matching the listing and the dump.

Many errors are found quickly because the registers give the programmer a good place to start his search for a bug. The heavy use of subroutines also results in a trail of saved registers, which helps in error detection. Finally, the interruptions caused by illegal addresses and operation codes help to pinpoint bugs at the earliest possible moment.

Patching is difficult and, at first, most programmers reassemble for anything more complex than a one-for-one replacement. The chief source of errors in patching is constructing correct base-displacement addresses for the branches to the patch and back to the main sequence of instructions. Obviously, many small subroutines will help to speed up operations by allowing one to reassemble only the subroutine in error rather than the whole program.

conclusion

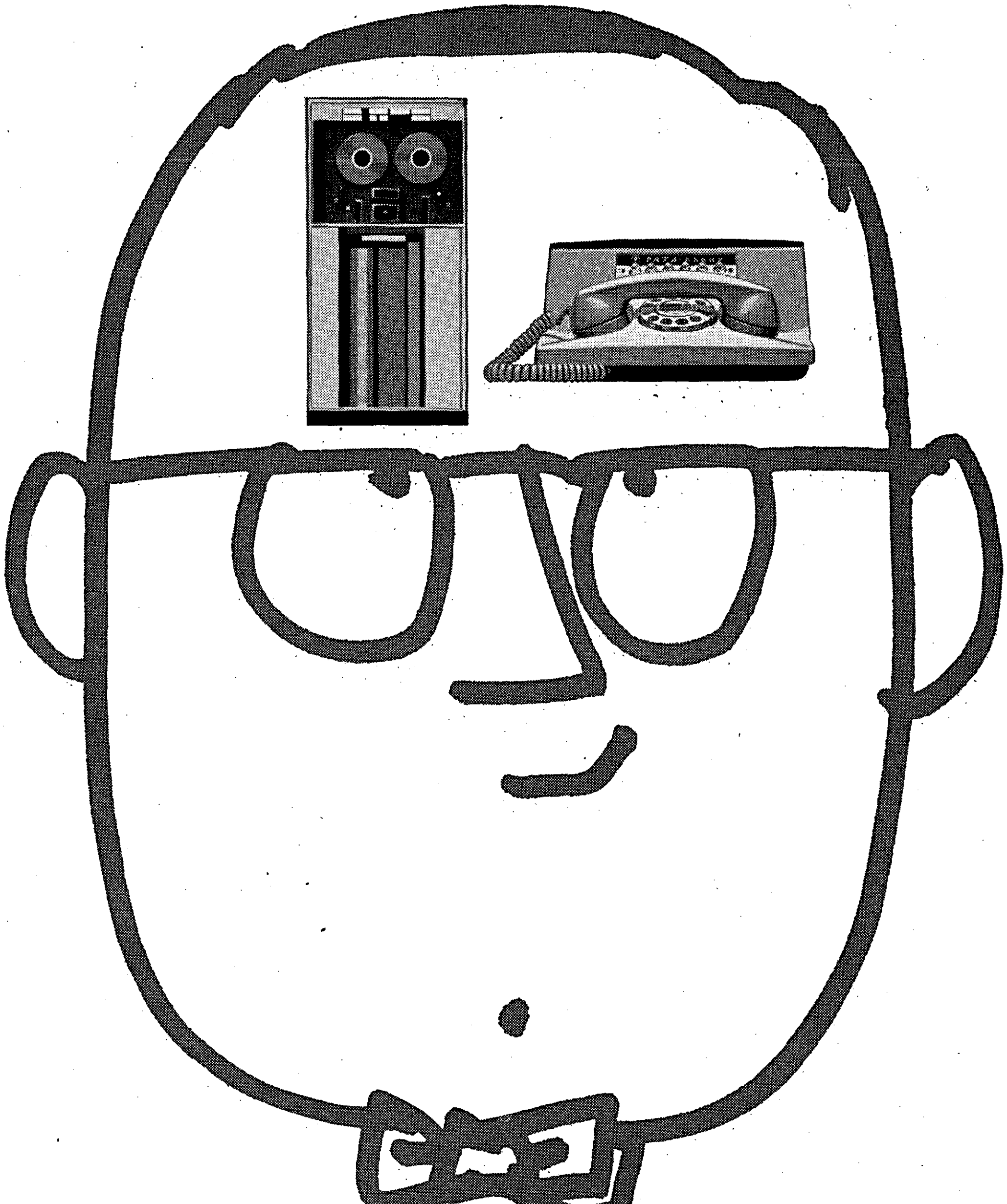
Most of our programmers had an easy time learning the 360 class machine, despite the fact that no classes were available at the time. All learning was through the programmer's reference manual and informal conversations. Although System/360 software was not available when the majority of our work was in progress, we did find the 360 assembler and simulator on the IBM 7090 a great help. We would encourage those with an early 360 order to make heavy use of these packages.

As is the case with almost every new machine, first reactions to 360 class machines are often unfavorable. But in a short time most programmers place them high on their list of good computers. Certain features invite controversy, such as base-displacement addressing. Such addressing is inconvenient at times for coders; however, the good programmer will take advantage of it to address data at different locations without moving it. In addition, the manager will prefer it because it allows the computer to have instructions with small address fields in a family of machines whose core size varies from the very small to 16 million characters.

Each of the various design decisions and trade offs made by the designers of the System/360 was based on sound reasons; programmers who desire to learn these should read "Architecture of the IBM System/360."[1]

In general, we found that 360 class machines require study and a special programming approach, but they are interesting, versatile, and easily programmed in assembly language. ■

1. G. M. Amdahl, G. A. Blaauw, F.P. Brooks Jr., *IBM Journal of Research and Development,* Volume VIII, No. 2 April 1964.



DEVELOPING SYSTEMS TIMING SPECS

by DENNIS G. PRICE and DENNIS E. MULVIHILL

Most people, who are concerned with such things, are aware that they should prepare and issue to manufacturers a "set of systems specifications" before they acquire a computer. These specifications take many forms, but include a description of the applications (even including a few flow charts), and provide volume figures of transactions and master files. Frequently the equipment manufacturer is asked to supply an incredible assortment of information about his hardware and software—often in imposing but irrelevant table form.

Unfortunately, most EDP specifications allow too much discretion to the manufacturer. The specifications then become subject to his interpretation as to what is required, with the result that much time is consumed in discussion with the evaluation group, or, worse yet, the manufacturer may completely misunderstand the requirement and submit a proposal which does not meet the specifications.

If we seem to say that the state of affairs is a sad one, that's because it is indeed sad! While we think those obtaining a first computer can profit most by understanding the contents of this article, our audience we believe could profitably (and regrettably!) include organizations obtaining their second or subsequent computer. We shall describe first the "full" specifications appropriate to acquiring a computer for a "typical" data processing organization: e.g., where 40 or 50 regular runs account for more than 75% of monthly usage. Then we shall discuss alter-

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native approaches more suitable for the "job-shop" type of operation or where a simple upgrading of equipment is required.

objectives

So, what are the objectives of a "full" set of specifications?

a. All quantitative data given to the EDP equipment manufacturer or supplied by him should be on standardized forms, and should be kept to a minimum. They should contain such obvious items as, for example, the number of records for each file.
b. Conceptual systems design should be completed before the preparation of EDP equipment specifications. This includes top level flow charts, record descriptions, current volumes and a rough estimate of volumes for three to five years in the future.
c. The logic EDP system flow charts should tie in to the specification forms.
d. The forms should facilitate preparation by the equipment manufacturer, even to the extent of his being able to keypunch the information as input to a computer program which will generate the timings and configuration he will propose.
e. The forms should be designed so that upon return from the EDP equipment manufacturer they may be evaluated easily by the group which prepared the specifications.

An intensive examination of the existing system must precede preparation of the EDP system flow charts, quantitative information, and record layouts for the proposed system. We assume this has been done prior to the preparation of EDP specifications.

The flow charts must tie into the specification forms. For example, the computer operation DEM 1 (see Fig. 1) refers to the main processing form for run DEM 1 (see Fig. 3). (DEM 1 means Daily Expense-accounting Main processing run number 1).

The flow charts may assume, say, a maximum six-tape system (or, more properly, a system of six logical files) and this is reflected in the specifications flow charts. This does not mean, of course, that the EDP equipment manufacturer is limited to proposing a six-tape system. He may propose more or fewer tapes and wish to propose random access equipment completely, or in part, instead of tape equipment.

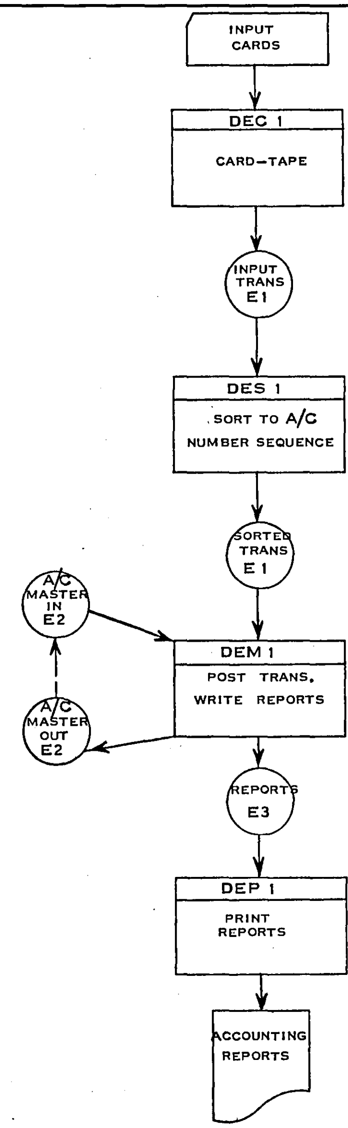
Each of the runs shown on the flow charts must now be described on a timing form. But before describing the forms we have evolved, it is necessary first to distinguish the various kinds of computer runs: media-conversion (peripheral), main processing, sorts and merges.

In the specifications, media conversion runs are concerned with reading cards and converting them to tape, reading tape and punching cards, and reading tape and printing. In contrast, main processing runs are concerned with processing input in a particular way in order to update files, etc. Media conversion runs generally do not make much use of a computer's internal processing ability since they are concerned with simple jobs, whereas main processing runs may make extensive use of the computer's internal processing ability. Because of the complexity of the main processing runs, we only describe one run per form. On the other hand, only one line of a form is required to describe a media conversion run.

Sort and merge runs are in a separate class, since—although they use the computer's internal processing ability extensively—they are usually performed by using a routine supplied by the EDP equipment manufacturer and can be timed using a formula supplied by him. For this reason, it is possible to show each run as only one line on a form.

There has never been any real problem in timing sorts, merges, and media conversion runs, but difficulty has always existed with main processing runs. This has been largely because of the intricacies involved in accurately estimating internal processing time, as opposed to calculating input/output time (assuming that the files were exactly defined).

Fig. 1



the timing specification forms

The intent of the Timing Factor Information Form (Fig. 2 facing page) is to obtain all the factors which are used in the various Timing Specification Forms, so that the information which the manufacturer supplies on these latter forms may be easily audited, and kept to a minimum. Most of the entries are easily understandable by those in the data processing field, but some need explanation:

Instruction Conversion Factor (Item 13)—this is obtained from a detailed block diagram included with the specifications. The objective in the block diagram is to obtain a mix of typical instructions closely related to the actual applications. We exclude Data Moves, Puts and Gets, since these are timed separately. The block diagram may consist of, say, 20 COBOL instructions or statements. (We could, of course, use FORTRAN, or other language, statements if desired). The manufacturer then converts these to equivalent machine language instructions in the way his compiler would act, which, of course, is not necessarily the most efficient conversion. Assume that for a particular manufacturer the 20 COBOL instructions convert to 100 machine language instructions. His "Instruction Conversion Factor" would then be five.

Average Instruction time, Other Instructions (Item 14)—this, too, is obtained from the block diagram. For example, if the 100 instructions of the manufacturer resulting from the block diagram take a total of 600 microseconds, the Average Instruction Time is six microseconds.

Average Number of Storage Elements per Instruction (Item 18)—this information may be obtained from the block diagram. For example, if the 100 instructions that the manufacturer requires take 700 characters of core, then the average number of storage elements is seven, or if 200 "bytes" are required, then the average number of storage elements is two.

The objective of the Main Processing Run Form (Fig. 3, see p. 56) is to separate input/output file time from internal processing time. When the answers for this are obtained, then it is merely a matter of knowing from the type of computer how one may combine input/output time and processing time: e.g., for some computers they may be overlapped. To the result we add final rewind time and set-up time, and thus obtain total run time. (This assumes, of course, that intermediate rewinds for multi-reel files may be overlapped by "flip-flopping" between tape units. In addition, with the use of modern operating systems, it is often possible to overlap final rewind time and set-up time).

The information on the form refers to the main processing run in the sample flow chart. In this example we have four logical files—shown under the Identification section of the form. The number of alphabetic and numeric characters for each record is also shown as is, also, the number of records in the files. The manufacturer then completes the remaining information.

As may be seen from the form, the manufacturer must calculate total access time and total transfer time, for tape or random storage, to obtain the gross total input/output time for each file. Of course, if a random access device is used, the number of records accessed and transferred is not necessarily the number of records in the file, but may be the number of "hits" which is usually the number of transactions. When the time for each file has been calculated, the manufacturer assigns file times to separate channels, if he is proposing more than one channel. (Otherwise, all files are assigned to one channel). The file times which are largest (and with which other files are overlapped) then add to net total file time.

internal processing time

It is usually difficult to estimate internal processing time—consisting of the internal time to process transactions and to pass files. This is because even though it is possible, for a given run, to approximate the number of instructions for a given computer, each computer proposed will have a different instruction repertoire and also possibly a different address structure. It is, therefore, appropriate to use a non-machine oriented language, such as COBOL. The best person to estimate the number of COBOL statements is an experienced computer analyst who has a sound knowledge of the proposed applications.

The analyst's estimate of the number of COBOL instructions required when a "hit" is obtained (i.e., all instructions other than to pass files) is shown on the form in brackets after "Other Instruction Time." The manufacturer must then convert the number of "Other" instructions to the number required for his instruction repertoire and his address type. This is done by multiplying by the "Instruction Conversion Factor."

Another difficulty has been the method of calculating instruction execution time. Various attempts have been made: for example, manufacturers have been instructed to use the time to perform an ADD instruction, or to use some average instruction time based on the manufacturer's experience. These approaches, however, have proved dangerous since they allow too much discretion to the manufacturer or may simply be inaccurate for the applications proposed. For this problem, too, the block dia-

Fig. 2

STATE XYZ DEPARTMENT FINANCE MANUFACTURER

TIMING FACTOR INFORMATION FORM

FOR MAIN PROCESSING

1. Number of tapes frames per alpha char.	FRAMES	10. Data move instruction formula		
2. Number of tape frames per numeric char.	FRAMES	11. Time for get instruction		U.S.
3. Number of tape frames per word	FRAMES	12. Time for put instruction		U.S.
4. Tape start/stop time per block	MS	13. Instruction conversion factor (from block diag.)		
5. Avg. random access file seek time	MS	14. Avg. inst. time other instructions (from block diag.)		U.S.
6. Tape data transfer rate	FRAMES/SEC.	15. Memory cycle time		U.S.
7. Random access file data transfer rate	FRAMES/SEC.	16. Interlock time per block		U.S.
8. Tape recording density	FRAMES/INCH	17. Rewind time per tape reel		MINS.
9. Tape inter-block gap length	INCHES	18. Avg. number of storage elements per instruction (block diag.)		ELEMS.

FOR PERIPHERAL PROCESSING

PRINTER		CARD PROCESSING	
1. Rated print lines per minute	LINES	1. Rated reading cards per minute	CARDS
2. Rated skip lines per minute	LINES	2. Rated punching cards per minute	CARDS
OTHER (scanning etc. – specify)			
1.			
2.			

MANUFACTURER'S NOTES AND REMARKS

gram proves useful, since it provides the "Average Instruction Time for Other Instructions" shown on the Timing Factor Information Form.

The total internal processing time is therefore divided into the following separate sections:

1. Data Move Time: This is calculated by totaling the number of output records from column 9 and multiplying by the Data Move instruction time based on the formula on the Timing Information Form. This assumes that each input record moves to an output area or is generated and moved internally. If input records move to an intermediate work area before moving to an output area, then two moves are involved. Alternatively, "scatter-read" and "gather-write" may reduce move time. In any case the manufacturer must calculate the move time according to his proposed equipment.
2. Puts and Gets: This of course is the total number of input records (Column 9) multiplied by the Get instruction time, plus the total number of output records (Column 9) multiplied by the Put instruction.
3. Other Instruction Time: The manufacturer simply multiplies the number of COBOL instructions shown in brackets, by his Instruction Conversion Factor, and his Average Instruction Time, to obtain the time to process one transaction. This is then multiplied by the number of transactions.
4. Buffer-memory transfer time is obtained by multiplying the total number of words of input and output (total number of frames, column 13, divided by the Number of Tape Frames per Word) by the Memory Cycle Time.
5. Interlock time is obtained by multiplying the total number of blocks from column 11, by the Interlock Time per Block.

We have now obtained Total Processing Time. This is then compared with Net Total File Time (Column 19) and by adding or taking the larger, or some combination of these (whichever is pertinent for the particular computer) we obtain Total Running Time. We then obtain Total Run Time by adding Set-up Time and Rewind Time for the longest reel remaining at the end of the run (assuming flip-flop was available if more than one reel was required for any file: otherwise, intermediate rewind and tape-change time must be added). With recently announced computers, the internal processing speeds are such that for many data processing applications it may be possible to ignore the impact of internal processing time on total run time. In this case, "Total Processing Time" on the form may be excluded when calculating "Total Run Time," since it will be overlapped with file time.

core memory required

We may obtain, through the same form, the total memory required for the run. This is composed of the memory required to accommodate the program and the files.

With regard to memory for the program, it is necessary to provide the manufacturer with the estimated number of COBOL instructions for the input/output processing, and separately for all other instructions. In addition, he is instructed to add a certain percentage to the above amounts of memory to allow for constants, working storage, etc. The manufacturer then multiplies these figures by his Instruction Conversion Factor to obtain the figures

Fig. 3

STATE XYZ DEPARTMENT FINANCE APPLICATION Expenditure Accounting RUN NUMBER DEM 1

COMPUTER SYSTEMS SPECIFICATIONS: MAIN PROCESSING RUN DAILY (FREQUENCY) MANUFACTURER

IDENTIFICATION					MAGNETIC FILE INFORMATION								TOTAL FILE TIME AND OVERLAP INFORMATION						
1 Line Number	2 File Number	3 File Description	4 I-Input, O-Output	5 T-Tape/Disc/Etc.	6 Number of Alphameric Characters per Record	7 Number of Numeric Characters per Record	8 Total Record Length in Frames	9 Total Number of Records in the File	10 Manufacturer's Blocking Factor	11 Number of Blocks in the File	12 Block Length or Fixed Block Length (Frames)	13 Total Frames in File	14 Main Storage Requirements in Words for Block; I/O and Work Area	15 Random Storage Requirements in Frames in File	16 Total File Access Time: Tape or Random Storage (0.0 Mins)	17 Total File Transfer Time: Tape or Random Storage (0.0 Mins)	18 Gross Total Time per File (0.0 Mins)	19 Net Total Time per File (0.0 Mins)	20 File Length (0.0 Reels, Discs, Etc.)
1	E 1	Sorted Trans.	I	T	19	40		2,500											
2	E 2	A/c Master In	I	T	40	72		30,000											
3	E 2	A/c Master Out	O	T	40	72		30,000											
4	E 3	Reports	O	T	25	36		8,000											
5																			
6																			
7																			
8																			
9																			
10																			
TOTALS			X	X	X	X	X	70,500	X		X								

INTERNAL PROCESSING TIME AND TOTAL RUN TIME (0.0 MINS)	
21. Data move time	
22. Puts and gets time	
23. Other instr. time (300.)	
24. Buffer-memory time	
25. Interlock time	
26. Total processing time	
27. Net total file time (col. 19)	
28. Total running time	
29. Rewind time	
30. Set-up time	
31. Total run time	

CORE MEMORY REQUIRED FOR RUN	NO. OF COBOL Statements	CONVERTED YOUR ADDR. TYPE	MEMORY REQ'D IN WORDS
PROGRAM:			
Input/Output Instructions	600		
All Other Instructions	2,400		
Total	3,000		
Add 5 % for Constants, Working Storage, Etc.	150		
FILES:			
From Col. 14			
Total Memory Required			

MANUFACTURER'S NOTES AND REMARKS

for the next column. These figures are then multiplied by the "Average Number of Storage Elements per Instruction" to obtain the number of words of memory required. The number of words required to accommodate the files is obtained from column 14 of the form. Note here that if there are alternate read or write areas, allowance must be made for them. If an executive program is used, the memory required must also be included, of course.

appropriate when the organization is contemplating major changes to its existing systems where there are fewer than, say, 40 Main Processing runs. These situations are in contrast to the specifications suitable for a "job-shop" type of operation.

The job-shop operation occurs quite often in practice, and the type of specifications described above are not particularly appropriate. The reason for this, of course, is

Fig. 4

STATE XYZ DEPARTMENT FINANCE

COMPUTER SYSTEMS SPECIFICATIONS: PRINTING RUNS DAILY (FREQUENCY)

FOR PRINTING WHETHER SIMULTANEOUS WITH A PROCESSING RUN OR NOT											FOR PRINTING WHICH IS SIMULTANEOUS WITH A PROCESSING RUN				
1 LINE NUMBER	2 RUN NUMBER	3 REPORT NUMBER	4 REPORT DESCRIPTION	5 NUMBER OF LINES	6 RATED L P M LESS 10%	7 TOTAL PRINT TIME PER FILE: (0.0 MINS)	8 NUMBER OF SKIP LINES	9 RATED SKIP LPM LESS 10%	10 TOTAL SKIP TIME PER FILE (0.0 MINS)	11 TOTAL PRINTER TIME PER FILE PLUS 4.0 MINS SET-UP (0.0 MINS)	12 ADDITIONAL CPU TIME PER LINE: (0.0 MINS)	13 ADDITIONAL CPU TIME PER FILES (0.0 MINS)	14 TOTAL FILE READ TIMES (0.0 MINS)	15 TOTAL FILE WRITE TIMES (0.0 MINS)	16 ADDITIONAL MAIN STORAGE REQUIREMENTS IN WORDS
1	DEP1	E3	Accounting Reports	8,000											
2	Etc.	Etc.	Etc.												
3															
4															
5															
6															
7															
8															
9															
10															
TOTALS														X	

MANUFACTURER'S NOTES AND REMARKS

The Printing Form (Fig. 4) and the other ones detailed below differ from the Main Processing Form in that they show one run on each line of the form rather than one run per form.

This form is straightforward through column 11, since for each run we are merely computing the total print time and the total skip time for the file being printed. If, however, the printing is to be performed simultaneously with a processing run, it may become necessary to calculate the additional main frame processing time and core memory required. This may then be added to the relevant Main Processing Form by making suitable entries on the last one or two rows, and adjusting "Internal Processing Time and Total Run Time" and "Core Memory Required for Run." Of course, as discussed earlier, if the internal processing time is insignificant, it may be ignored.

A card-tape form, very similar to the Printing Form, merely calculates the total time required for card reading and punching. Since it is so similar to the Printing Form, it is not shown.

The Sort and Merge Form (Fig. 5) contains the information necessary for the manufacturer to calculate the time required to perform a sort or merge according to his formulas or tables.

Fig. 5

STATE XYZ DEPARTMENT FINANCE

COMPUTER SYSTEMS SPECIFICATIONS: SORT AND MERGE RUNS DAILY (FREQUENCY)

1 LINE NUMBER	2 RUN NUMBER	3 SORT OR MERGE	4 FILE NUMBER	5 FILE DESCRIPTION	6 NUMBER OF CHARACTERS PER RECORD	7 NUMBER OF RECORDS	8 LENGTH OF KEY-WORD IN A/N CHARACTERS	9 TOTAL TIME PER FILE: (0.0 MINS)	10 TOTAL TIME PER FILE: IN (0.0 MINS)	11 TOTAL TIME PER FILE PLUS 4.0 MINS SET-UP (0.0 MINS)
1	DES1	S	E1	Input Trans.	50	2,500	12N			
2	Etc.		Etc.	Etc.						
3										
4										
5										
6										
7										
8										
9										
10										
TOTALS										

MANUFACTURER'S NOTES AND REMARKS

other approaches to specifications

The specifications described above are most suitable for an organization obtaining its first computer. They are also that it would be extremely difficult to produce detailed flow charts which describe a myriad of jobs (these may run into hundreds). In addition, the jobs which are run this month may be completely unrelated to the jobs which are run next month, or six months from now.

There is another situation, too, where the organization wishes merely to upgrade its EDP equipment, with little or no systems redesign. This may be desired because, for example, processing volumes are projected to exceed present machine capacity, or the acquisition of new equipment offers advantages because of its lower cost and increased throughput capacity.

In these cases, it is possible to produce the information required for timing analysis by the manufacturer in a much simpler form compared to that described above. Let us assume, for example, that the current equipment consists of a peripheral processor and a main processor. Of course, the exact equipment, languages, and software packages used, would be described in detail. In this case, we might provide the manufacturer with the type of information, as shown in Table I.

From the information provided, the manufacturer will be able to propose equipment which will meet the requirements of the organization during the periods shown—i.e., two years and five years from now.

In order to verify the times which the manufacturer claims for his equipment and relate them to the kinds of operations which the organization actually performs, it is usually desirable to include some benchmark problems with the specifications. These benchmark problems must be representative of the operations performed in the organization. In fact, some approaches to specifications use this method almost exclusively. They say, for example, that benchmark problem A, which takes an hour per month on existing equipment, is representative of 50 hours per month of their operations.

Needless to say, of course, the benchmark problems given the manufacturer must be picked with extreme care, since if they are not representative, the results will be invalid. The problems given to the manufacturer may be written for him in either COBOL or FORTRAN (or some other language for that matter), or the organization may simply choose to give the manufacturer detailed flow charts. This latter method is not as desirable, since it leaves some aspects of the problem open to interpretation by the manufacturer.

Let us assume that the manufacturer has received 10 sample problems. When he is ready to demonstrate on the proposed equipment, the organization will send representatives to take exact timings of the run times. If, in our example, the one hour job took 12 minutes, one would assume that the 50 hours per month for similar work would only take 10 hours per month. In this way, one could calculate the time required for all jobs on the proposed equipment, and thereby validate or invalidate the manufacturer's proposal.

The approaches described in this section are, of course, much simplier than the "full" approach described earlier. In practice, it may well be that some combination of the two methods is required. For example, there may be several Main Processing runs which account for a large percentage of the activity per month. The balance of the activity is made up of job shop applications. A combination of the two approaches would then be the most appropriate.

summary

The flexibility of the "full" approach for the manufacturer is that it enables him quickly to make any assumptions with regard to block size, number of channels, speed of tapes, etc., and then adjust the configuration to obtain a "balanced" system so that in his proposal he will propose the most economical configuration for the whole set of specifications. The flexibility of this approach has, in fact, been demonstrated, since we have had at least one manufacturer program for this approach and key punch data directly from the specification forms. In this way, the manufacturer was able to test automatically over 30 different configurations and pick the one best suited to the specifications.

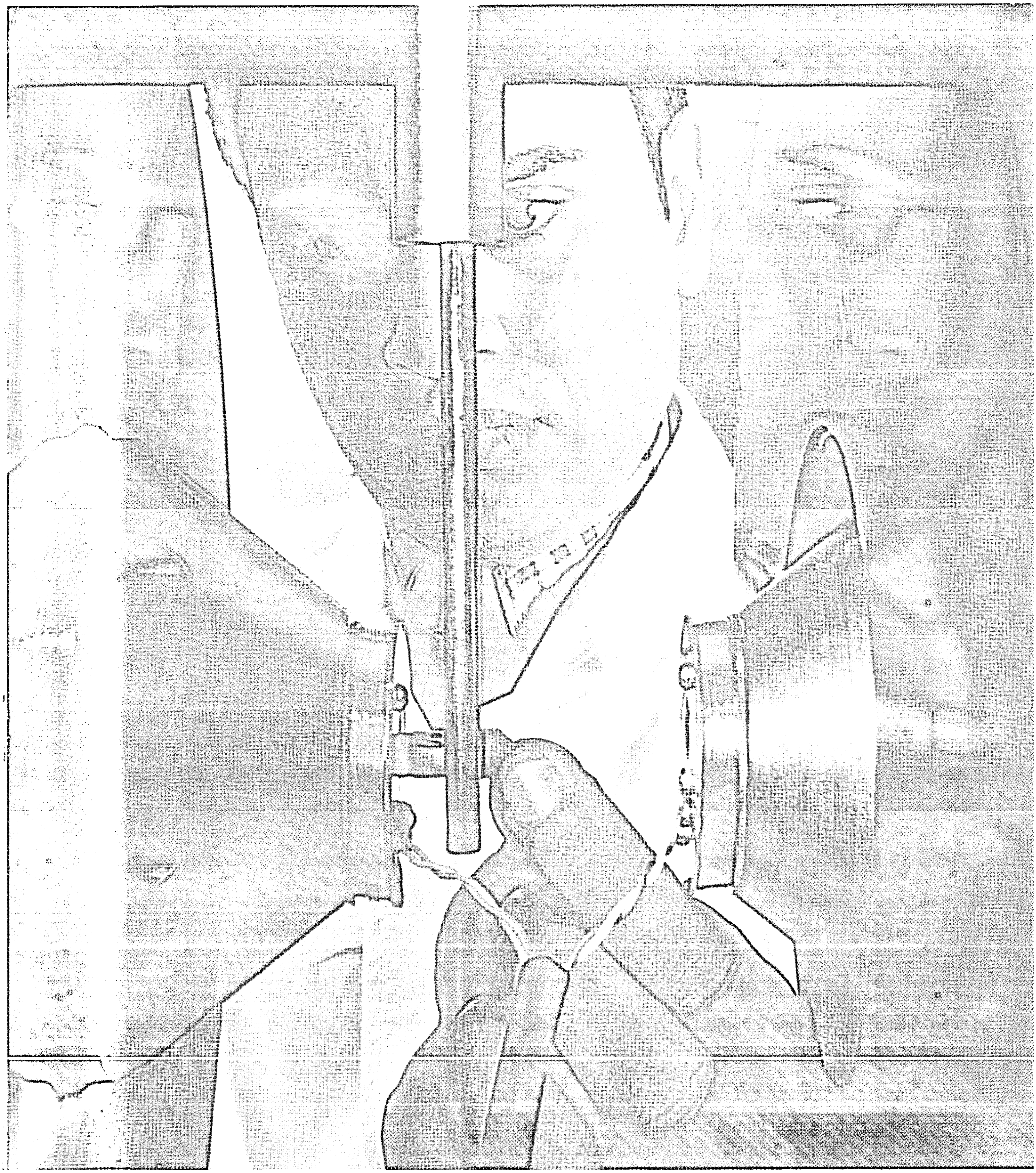
We all know that it is essential to obtain accurate figures on timings to facilitate an evaluation. The methods described above or earlier versions of it have been used in many applications by industrial firms, the federal government, state and foreign governments. Actual run times for main processing runs (which are the only runs difficult to estimate) have come within 5% of the time shown in the form where there has been no significant systems or volume change. In every case, the equipment accepted from the successful bidder has been the correct size to process the applications contained in the specifications.

Although at first glance the method appears overly detailed, it is no more work for the user than less formalized methods, since the information shown is basically the same. Moreover, the manufacturer must make the same calculations as those on the forms, if he is to do an honest job. And you may be assured that "good" specs result in "good" proposals.

The advantages of the "other" approaches described above are primarily that they impose less work on the manufacturer and the organization which prepares the specifications, and secondly they may be more appropriate where the type of operations performed are more in the nature of job shop operations. In these cases, we have found that the approach described is much more appropriate, and will also result in good proposals from the manufacturers. ■

Table I

Function	Meter Time Per Month		
	Present	Two Years Hence	Five Years Hence
Tape Reading and Writing	90	150	300
Internal Processing	30	50	100
Tape Sorting	50	90	180
MAIN PROCESSOR TOTAL	170	290	580
Printing	80	120	160
Card Reading	40	50	70
Card Punching	10	15	20
PERIPHERAL PROCESSOR TOTAL	130	185	250



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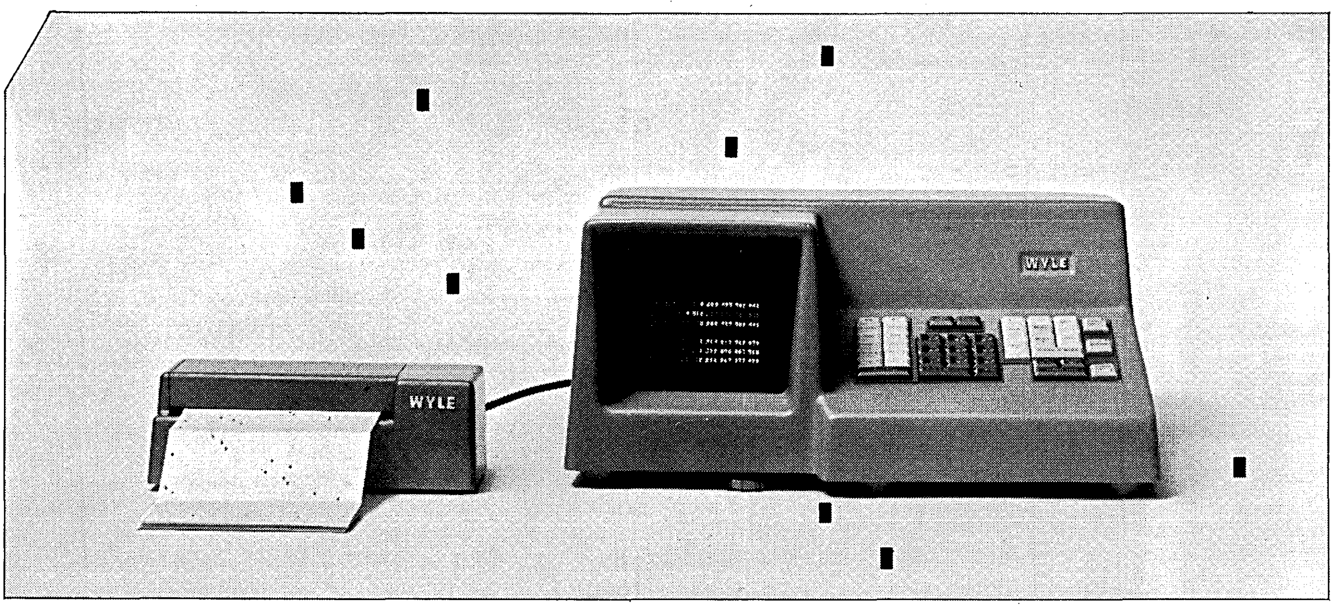

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0	000	000	000	000	.000	495	582	441	Multiplier-Quotient Register
	000	000	004	512	.000	000	000	000	Entry Register
	000	000	000	000	.000	495	582	441	Accumulator Register
	000	000	000	001	414	213	562	373	Storage Register 1
	000	000	000	001	732	050	807	568	Storage Register 2
	000	000	000	002	.236	067	977	499	Storage Register 3

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CIRCLE 27 ON READER CARD

NEW RUSSIAN COMPUTER

A new but un-named Russian computer with performance in the 7090 class has been revealed by a recent translation of a series of four articles from the Russian-language book, "Problems in Computer Mathematics and Computer Technology," Moscow 1963.[1] Although details of the instruction set, I/O control, and programming are lacking, sufficient information is presented on machine organization, timing, error checking, and arithmetic unit operation to permit assessment of the machine's performance and design emphasis.

The ostensible purpose of the machine is solution of problems in mathematical physics, although the heavy emphasis on complete error checking on all arithmetic as well as word transfers might imply possible real-time applications. In any event, the design is strongly oriented toward problems wherein the rate of change of operand locations is low compared to the instruction rate. To this purpose, ferrite core main memory is divided into two parts—a small 63-word, 2-usec operand memory and a large 4,095-word, 4-usec instruction and operand memory. With this orientation in mind, the following table from the translation pretty well indicates the performance of the machine. Asterisked items have been added either from the text or by inference from the text.

Parameter	Characteristics
Number system	Binary
Technique	Floating point, parallel
Range of number values	$\pm$ (10^9-10^{-9})
Number of digits in input and output	7 decimal digits
Word length	39 binary bits
a) mantissa with sign	30 binary bits
b) exponent with sign	6 binary bits
c) check code	3 binary bits
Instruction system	
a) with respect to the operand memory	Three-address
b) with respect to the instruction memory	One-address
Number of instructions	Up to 63
a) control instructions	27
b) arithmetic instructions	32
*Operand memory capacity	63 numbers - 2 μs cycle time
*Instruction memory capacity	4,095 words - 4 μs cycle time
Capacity on magnetic drums[2]	65,000-260,000 words
Flow rate of words from magnetic drums	25,000 words/sec
Capacity on magnetic tapes	300,000 words
Input from punched cards	35 numbers/sec
Output onto punched cards	10 numbers/sec
Output to printer	20 numbers/sec
Execution time for arithmetic and logical operations	8-90 μs
a) floating point addition and subtraction with a 3-digit shifting for normalization	8 μs
b) logical operations (except shifting)	8 μs
*c) multiplication	18 μs average
d) division	40 μs
e) square root computation	90 μs
f) shifting	11-40 μs
*g) branch and index	8 μs
*h) branch conditional	16 μs
Checking of computations	Modulo 7
Number of Radio Tubes	4,000-4,500
Power consumption	30-35 Kw

The first salient feature of the machine design is complete I/O overlap and good data flow balance. The machine uses an 8-usec basic cycle time in such a way that the operand memory uses three 2-usec cycles associated with the three-address instruction, and the fourth cycle is free for a command fetch or for a transfer to the large memory. Likewise, the large memory has one free cycle per 8 usec, to be used for transfer to the operand memory or for drum word transfer. Thus, complete overlap of drum-to-memory and memory-to-memory transfers is possible simultaneously, the drum taking 25% of the large memory free cycles, and the operand memory anywhere from 15% to 75% without interfering with instruction execution.

A second salient feature is complete checking of all operations between and within machine units. A three-bit check sum which is the sum modulus seven of the digits of a register is associated with every word. Check sums are recomputed and compared for all transfers, for all arithmetic operations, for address modification, and for detection of incorrect memory address selection. For arithmetic operations and address modification, independent arithmetic or logical computations are made on the check sum and compared with the check sum of the result. The number representation has been chosen such that the check sum of a sum or product is the sum or product of individual check sums modulus seven. Memory selection is checked by adding into the register content check sum the check sum associated with the location into which it is to be read. Subsequent fetch and check sum computation will detect incorrect memory select.

The third salient feature of the machine is the anticipated carry adder and its employment to provide fast add and multiply times. By departing from the standard pulse logic used throughout the bulk of the machine and using level logic, the carry propogation time associated with the add is 0.5 usec. This is achieved by propogating carries through three-bit groups, between three-bit groups in blocks of nine bits, and between nine-bit blocks. The result is three levels of carry anticipation wherein no carry must pass through more than five logic delays.[3] Numbers can be entered and the settled sum or difference sampled at a 1 Mcps rate, which accounts for the high performance of the multiply and divide instructions. This same high-performance circuitry does not seem to have been applied elsewhere, although it would have been advantageous, for instance, in improving shift-cycle instruction performance.

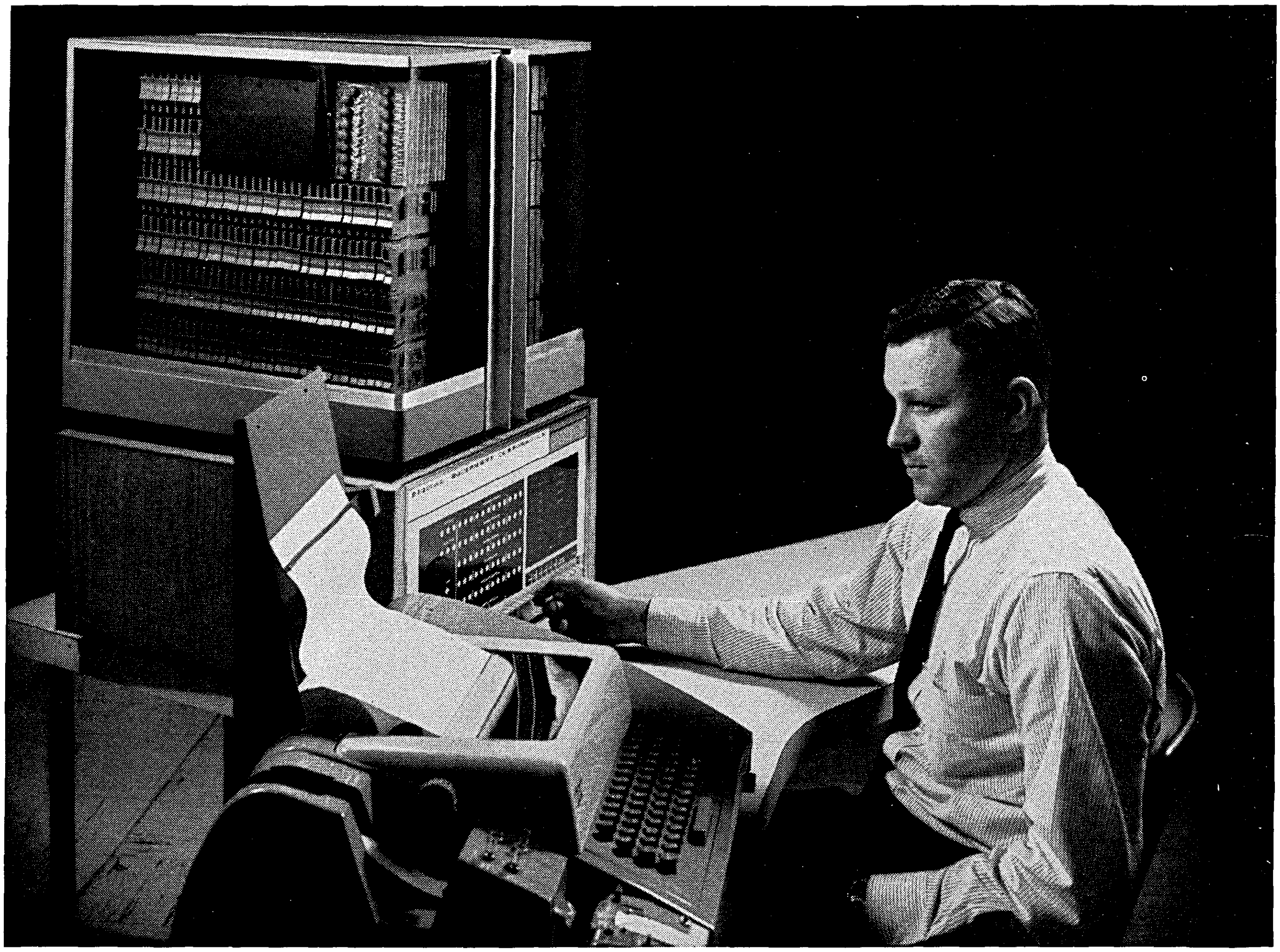
This machine appears capable of executing 200,000 equivalent single address instructions, which, for execution rate, is comparable with U.S. machines in the 7090 class. It is of course severely limited, compared to U.S. machines, in size of memory and the performance of card equipment. The memory disadvantage is offset to a certain extent by the smooth flow to and from the not inconsiderable drum memory. On the whole, the machine represents a modern, competent design, albeit a transistorless embodiment. ■

[1] U.S. Dept. of Commerce, Office of Technical Services, Joint Publications Research Service Translation JPRS: 27,418, entitled, "Digital Computers and Their Units - USSR," 17 November 1964. Cost: $2.00.

[2] The fourth article in the series describes a new magnetic drum. It is 12-inches in diameter, has a surface speed of 1,200 ips, uses air-floated, single-turn magnetic heads, has a bit density of 250 per inch, and a track density of 25 per inch.

[3] See U.S. paper, Weinberger, N., and Smith, J. L., "A One Microsecond Adder Using One Megacycle Circuitry," *IRE Transactions on Electronic Computers*, Vol. EC-5, No. 2, June 1956, pp. 65-73.

The PDP-8 is a high-speed, real time, general purpose digital computer with all the desirable features of the popular PDP-5 plus greater speed and, as is evident, considerably smaller size. Its 1.6 μsec cycle time gives it a maximum computation rate of 312,500 additions per second, and its input/output rate is 625,000 words (7½ million bits) per second.



Besides FORTRAN, the software package includes an on-line debugging program which gives the user dynamic printed program status information and an on-line editing program which lets him add, delete, change or insert single lines or sections of his symbolic program. The system also contains a macro assembler, floating-point software, elementary function subroutines in single- and double-precision arithmetic, and utility, diagnostic, and maintenance routines.

An input/output bus system permits simple connection of numerous standard and custom devices without changes in the central processor. Standard options include analog/digital and digital/analog converters, analog multiplexers, magnetic tape, paper tape, and drum memory systems, cathode tube displays, card punch and readers and other devices.

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CIRCLE 28 ON READER CARD

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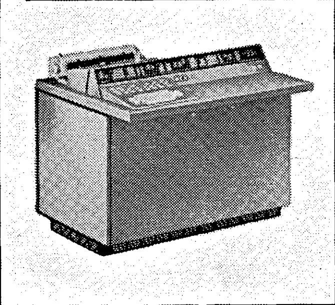

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CIRCLE 29 ON READER CARD

COBOL vs FORTRAN: A SEQUEL

for business dp

by CAPT. J. P. JUNKER and G. R. BOWARD

During the spring of 1964, a large-scale data processing problem was presented to the Data Services Center of Headquarters USAF for solution. Preliminary analysis revealed that:

1. Input to any solution program would be one binary and three BCD tapes totaling in excess of 150,000 logical records.
2. The internal logic of the program would consist primarily of a set of logical decisions applied against specified input fields to determine the nature of output records constructed through selective integration of input.
3. Only limited mathematical computation would be required.
4. Output would be a simple BCD file of approximately 4,000 logical records blocked 10 to the physical record with header.

The programming languages available for our use were FORTRAN II (Unbuffered), FORTRAN IV and COBOL. The decision to use the latter was based largely on our belief that as a generalized data processing language COBOL would provide fuller buffering capabilities, a direct approach to the problem of comparing fields up to 30 characters, character by character, a full complement of editing features and the ability to link directly to IBMAP or FORTRAN IV subroutines should the need arise. In addition, the version of FORTRAN IV available to us at the time had to be eliminated from consideration immediately because of input/output restrictions, and FORTRAN II had in past experience appeared painstakingly slow for data processing applications.

Work was begun on development of the basic program on 18 May 1964 and was completed 14 September 1964. During this period of time the programmer responsible had to learn COBOL directly from the available reference manuals, write the program, and completely debug it. In addition, work on the program was suspended for a period of approximately 60 work days during this time due to higher priority workloads. After completion, the total execution time required for operational use was 7.2 minutes. The results achieved in this project were considered extremely satisfactory and we were particularly pleased by the manner in which COBOL lived up to our expectations.

It was at that time that the article by M. D. Fimple, "FORTRAN VS COBOL," appeared in the August issue of DATAMATION. In his article, Mr. Fimple presented the results of a project that he had recently completed, which was designed to test the data processing capabilities of COBOL against those of a highly modified version of FORTRAN II. It was his conclusion "that FORTRAN on the 7090 does at least as good a job of data processing as does COBOL. . . ." This placed us, we felt, in a position of having to question our decision to use COBOL in the solution to our problem. We decided to set up a set of programs to test the validity of our rationale against Mr. Fimple's conclusions.

test of fortran vs cobol

The first test consisted of the selection of a problem that actually had been encountered. The file to be used in the test consisted of 55,440 logical records, 84 characters in length, and blocked 10 logical records to each physical record on the tape. The first physical record on the tape was preceded by a header and tape mark. The problem consisted of reading the file and testing for certain values within specified fields in each logical record. Based on the results of those comparisons, one of the following actions would be taken for each record:

1. It would *not* be written as output.
2. It would *be* written as output.
3. Eight additional records would be written as output along with the original record. The nature of the additional records would be determined by the contents of the fields tested.

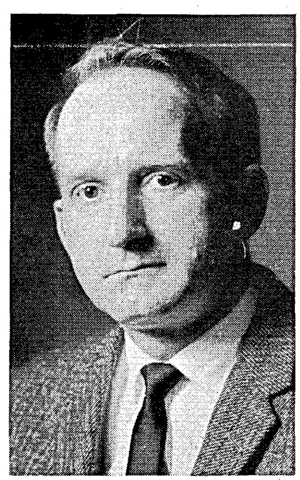
The output tape required exactly the same format as the input to the program. The results of this test are shown in the left hand column of Table I. The computer times shown are execution times only. Note that the COBOL program required less than one-sixth the time required by the FORTRAN II program.

TABLE I

	Blocking Factor = 10	Blocking Factor = 1
IBM 7094 COBOL	2.3 minutes	4.8 minutes
FORTRAN II	15 minutes	10.2 minutes

The right hand column of Table I shows the effect of deblocking the original input and running that input against the same two programs, with only input-output

Captain Junker is chief of the AF Program Documentation Branch in Headquarters USAF's Data Services Center, Washington, D.C. In this post, he is responsible for the production of a series of Air Force planning documents on the 7094. He was formerly chief of section, responsible for maintenance / implementation of 7080 and 1401 systems. He holds a BS in engineering from the U.S. Naval Academy, MS in management sciences from the U. of Michigan.



Mr. Boward is a mathematician with the Data Services Center of Headquarters USAF, with which he has been associated since January of 1962. He graduated with honors from West Chester State College, West Chester, Pa.

statements changed to accommodate the change in blocking factor. The deblocked tape contained only 28,058 logical records with output similarly deblocked. It is interesting to note that by increasing the blocking factor from 1 to 10, we were able to reduce object time of COBOL program by better than 75%, since twice the number of records were processed in half the time. The real significance of deblocking the tapes lies in the fact that unmodified FORTRAN II cannot process input or output physical records greater than 132 characters, nor can it test the end-of-file condition. In order to process the blocked tape in our study, it was necessary to employ a machine language subroutine while reading from and writing on tape.

In order to analyze the effect of providing FORTRAN II with a fairly complete data processing capability as did Mr. Fimple, we ran the same problem against the CENTAUR data processing system. CENTAUR, reportedly very similar to the WDPC package used by Mr. Fimple, was designed by Computer Concepts Inc. for use in the Department of Defense, and extends FORTRAN II to include such features as file descriptions, character-by-character record descriptions, buffered input-output, end-of-file testing, automatic header and trailer processing, and several other data processing features. The results of this test are shown in Table II.

The input to the CENTAUR programs was identically that input to the COBOL and FORTRAN II programs. The

TABLE II

	Blocking factor = 10	Blocking factor = 1
CENTAUR (BINARY)	2.15 minutes	X X X X X X X
CENTAUR (BCD)	5.30 minutes	4.4 minutes

distinction made between CENTAUR (Binary) and CENTAUR (BCD) refers to program output of binary and BCD files, respectively. CENTAUR is designed ideally to output either unblocked BCD report tapes or binary tape files for further processing. Note that the times recorded for the binary file tape and the unblocked report tape are not significantly different from COBOL times previously noted for the same parameters. The CENTAUR time recorded for blocked BCD output is, however, more than twice that of COBOL.

We may conclude here that COBOL seems to do what CENTAUR was designed to do as well as CENTAUR does what CENTAUR was designed to do. And that from the point of view of flexibility COBOL provides a very definite edge. Whether or not CENTAUR as designed requires such flexibility to perform its assigned tasks is a moot point, but we feel that similar conclusions most probably apply in Mr. Fimple's case in that he has modified FORTRAN II to include a version of the WDPC data processing package further modified to effectively process data in accordance with his specified requirements. In short, he is comparing a generalized system to one that appears highly specialized. It is highly doubtful that Mr. Fimple's system could stand up to a broad range of data processing applications as well as COBOL would. COBOL, we feel, provides us the ability to solve any of the data processing problems we have encountered to date without recourse to anything more drastic than an occasional IBMAP subroutine to analyze, for example, the bit configuration of a binary record.

We can readily conclude that the elimination of the programmer does not significantly affect the order of our results.

A second problem using the same input and output files and parameters was designed to remove the variable factor that would normally be associated with the variable competence of the programmers. This is a simple read

TABLE III

Blocking Factor = 10

IBM 7094 (COBOL)	2.08 Minutes
FORTRAN II	13.8 Minutes
CENTAUR (BCD)	7.1 Minutes

and write problem—i.e., a record is read in and a record is written out. It is the same problem as that examined above with the program logic removed. The results are shown in Table III.

conclusions

We believe that the results of this set of tests justify our decision to use COBOL. We also feel that while FORTRAN is a language better suited to problems of a scientific nature, COBOL is definitely superior in data processing areas for the IBM 7094. Certainly, since both COBOL and FORTRAN are presently available to us as a subsystem of the IBSYS system, we should make use of both, separately and in combination, utilizing the best features of each, as requirements arise in the solution of assigned problems. We do not feel, as Mr. Fimple does, that "the selection of language is more dependent on the type of machine than on the type of problems." Such a determination would require actually testing the same problem against both a binary and a character machine. It is interesting to note here that while we have no data available at present relating to execution times, the time required to compile a COBOL test program on the IBM 7080 (a character machine) was more than seven times that required to compile the same program on the 7094.

cautions in use of 7094 cobol

There are some limiting aspects of the IBM 7094 COBOL that may be identified from our experience:

1. The last block of a file may be shorter and may not comply with a specification which calls for an exact number of logical records per physical block. This is due to the fact that 7094 COBOL does not fill out or "pad" the final block with a specified constant when that block is incomplete. This is no limitation if one always operates in IBSYS, but if blocked output from a 7094 COBOL program is to serve as input to a system outside of IBSYS, an incomplete block will result in a record length error which may cause program failure. This fact particularly hampers any translation from 7094 COBOL to 7080 COBOL.
2. The padding constant is not checked on input to 7094 COBOL, and therefore records consisting of all constants are processed as data.
3. Not all fields on file headers and trailers are available for processing.
4. IBM 7094 and 7080 standard file labels are not compatible.
5. It is not possible to call subroutines from the FORTRAN library directly while operating in COBOL. This is a particular limitation when a dump of core is desired.
6. Many of the COBOL options appear to be redundant and their existence more confusing than enlightening.

summary

The verbosity inherent in COBOL, which caused Mr. Fimple some concern, is not considered by the authors to be a significant drawback. In fact, it is because of this verbosity that COBOL is able to provide excellent self documentation within a program as written. In addition, the verbosity in the Data Division presents an advantage, since once that division is constructed, the programmer need no longer consider his input/output procedures in any burdensome detail. The ease with which a COBOL program may be scanned and the ability to analyze such a program in terms of block rather than micro-logic definitely facilitates program maintenance and revision, and effective communication.

COBOL, we feel, is not a very difficult language either to learn or to program. It has already been pointed out that the preparation of the "data bridge," which was a fairly complicated data processing problem, was accomplished at the same time that the programmer was learning COBOL from the IBM reference manual. There are presently several excellent methods of providing COBOL instruction. The Department of Defense makes available to its organizations a COBOL programmed instruction course which is particularly good for beginning programmers. In addition, there are several good commercially available COBOL manuals and several manufacturer's instruction courses.

It is not the purpose of this article to propose COBOL as the all-purpose computer language. As stated earlier, the language employed in the solution of any programming problem should depend on the nature of the problem. Any attempt to restrict language usage regardless of the nature of a problem must in fact restrict the number and nature of solutions to that problem. It is not the purpose of this article to present statistically conclusive evidence on any aspect of programming, but rather to raise what we feel are significant questions about language selection in the programming of data processing applications. The test problems described above clearly demonstrate that IBM 7094 COBOL is superior to other higher languages for data processing applications. ■

filling out the line

THE 115 FROM GENERAL ELECTRIC

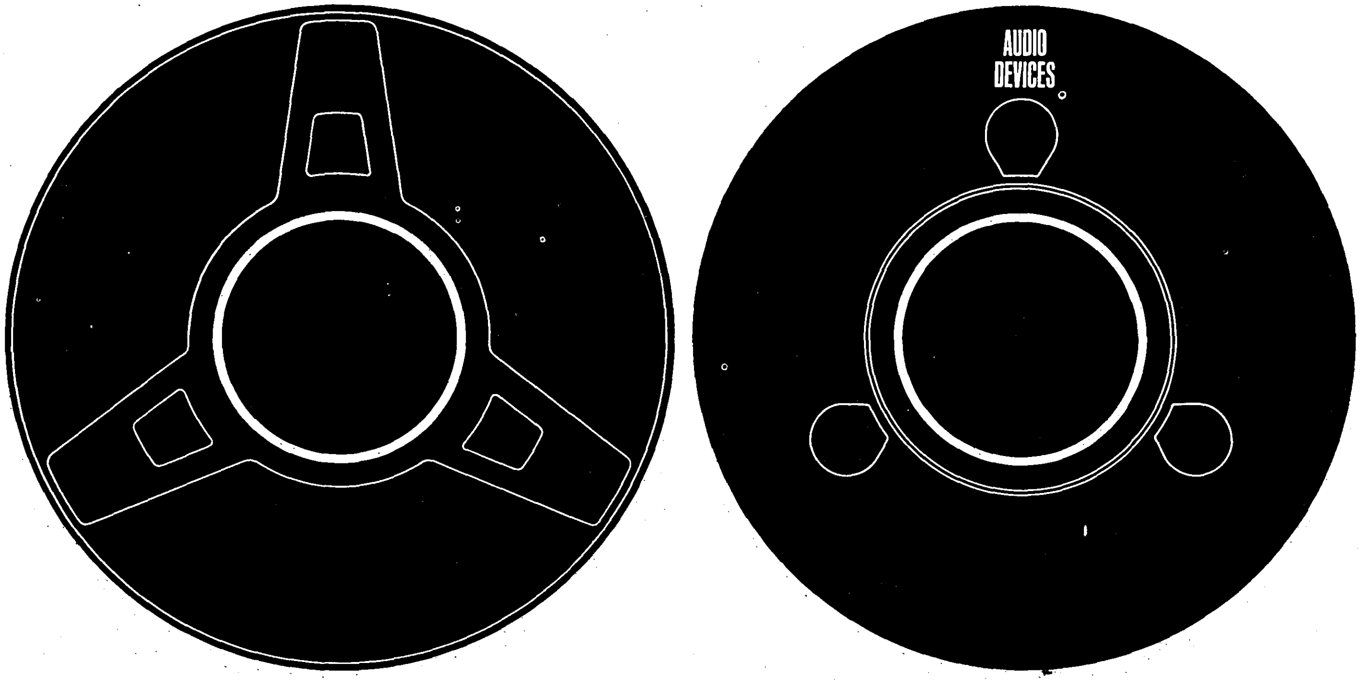
Another small-scale computer, system rentals beginning at $1,075 a month, has been announced. The GE-115 is a card-oriented processor with an access time of 8 usec and a capacity of 8K (8-bit) characters. The system is designed for localized dp as a remote terminal linked by communications lines to a central computer.

Developed by the Italian firm of Olivetti, the 115 reportedly will be produced in the States "as demand rises." First shipment from the manufacturing facility in Milan, Italy, is scheduled for December '65.

Arithmetic operations of the processor can be decimal or binary. The former is performed on up to 16 digits, the latter on fields up to 16 characters. There are 25 instuctions in the repertoire.

Peripherals, developed by Olivetti, Bull (of France), and the GE Computer Dept., include a 300- and 600-cpm card reader, 60- to 200-cpm punch, and 300- and 600-lpm printers; the latter have 64 characters and 136 print positions. There's also a random-access unit with two removable discs, a combined capacity of more than two million (8-bit) characters. Head positioning time is an average 445 milliseconds.

Purchase prices start at $51,600. ■



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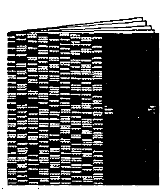

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CIRCLE 50 ON READER CARD

hardware and software standards urged

GOVERNMENT SETS DP GUIDELINES

The honeymoon, if not the romance, between Uncle Sam and the electronic computer is over. After 10 years of relative autonomy in the selection and operation of computing equipment, federal agencies will soon have to toe a common mark in ADP, under the watchful eye of the administration's principal housekeeping officials. That's the significance of a three-page document, bearing the innocuous title of Circular A-71, which was dispatched last month by the Budget Bureau to the heads of all Executive departments and establishments. Its subject: "Responsibilities for the Administration and Management of Automatic Data Processing Activities."

Circular A-71 is the instrument of implementation for most of the recommendations contained in BOB's recently-issued "Report on the Management of Automatic Data Processing in the Government" (see Washington Report, p. 22). The report, which took 18 months to produce, represents the combined efforts of a "working" committee of Agency EDP experts, a top-level "advisory" committee and the last-minute lucubrations of Budget Director Kermit Gordon and his staff. This report and its recommendations, and by extension Circular A-71, carry the written benediction of President Johnson as "administration policy."

The magnitude of the problem, and the amount of money involved, are such that not everyone agrees BOB's recommendations and guidelines are sufficient to cope with the situation. The General Accounting Office, for one, contends that central procurement of all government-financed dp equipment is still a requisite for effective management in this area. BOB maintains this responsibility is best left with the individual agency, or contractor. But while defending, essentially, the status quo in procurement practices, the changes recommended otherwise by the Bureau are strong enough to be considered an "upheaval" in existing dp policies.

Of particular interest within and without the government are those passages in the circular dealing with standardization. BOB has thrown its full weight behind the creation of standards in both hardware and software as quickly as possible, and has nominated the Bureau of Standards to be its cutting edge in this effort. It's BOB policy, says the circular, to arrange "for the approval and promulgation of voluntary commercial standards when it is in the best interests of the Government to do so, and to arrange for the development, approval and promulgation of Federal standards for ADP equipment and techniques on an interim basis, or permanent basis, when voluntary commercial standards are not available or usable."

Without exercising too much imagination, this passage can be read as a veiled threat by the government for commercial interests to get together on standards or the government will act unilaterally. This interpretation is apparently not far off the mark. "We remain dedicated to the concept of the American Standards Association, and of cooperation between commercial interests and the government," said a BOB official, "but if the manufacturers and users can't agree on important essentials we may have to act on our own. Incompatibility is simply costing us too much money."

BOB's concern with standardization is a theme that runs throughout the text of Circular A-71 but many other substantive matters are touched upon. "Perhaps the most important aspect of the circular," said an official, "is that we now have an agreed-upon breakdown of duties and responsibilities in ADP between BOB, GSA, and NBS, and the basis for coordinating these effectively." The following is a brief description, and analysis, of other highlights of Circular A-71.

Budget Bureau: The BOB's role as policy pacesetter for government dp affairs is reaffirmed. It will dispense the broad guidelines, and it will review, and hold accountable, the efforts of agency executives in following them. Among other things, BOB wants standardization, more computer sharing, better hardware and software techniques, and more up-to-date information on government dp resources (a running inventory). It advocates and will work for intra-agency and inter-agency integration of systems. "For example," said a BOB official, "the Veterans Administration on its computers prepares data each month for millions of checks. This data then goes to the Treasury Dept. where the checks are actually prepared on another computer. In turn, these go to the Post Office for sorting and mailing. With integration, these three stages might be combined into one system. Many other such situations exist throughout the government."

General Services Administration: In keeping with its basic housekeeping duties, the GSA is directed to tighten up its contracting procedures, provide more relevant ADP supply schedules, and press for improvements in the terms, conditions and prices of dp equipment. It is directed to support the standardization effort in its procurement specifications, and to provide leadership in computer sharing and exchange between agencies. With an eye to the future, the GSA is also to insure "that planning for the Federal Telecommunications System embraces consideration of the rising need for data communication facilities which provide for high-speed data transmission between computer-based systems." FTS, now primarily voice and teletype, is slated to go digital later this year, and will serve a critical role in ADP planning by civilian agencies.

The Civil Service Commission: The CSC is directed to continue its large-scale dp training program both for worker bees and for high-level government officials. Besides recruiting, training, and otherwise administering for dp personnel, the commission is directed to "anticipate and minimize, to the greatest practicable extent, any adverse effects of automatic data processing upon the people involved."

As for the heads of all other executive agencies, the circular closes by noting that they, and they alone, are "responsible for the administration and management of their total automatic data processing activities." "There's been a tendency in the past on the part of agency heads to regard ADP as a matter for technicians," said a BOB official. "This lets them know officially that they are personally responsible for success or failure in this area, and that this responsibility can't be relegated or delegated."

—James McCrohan


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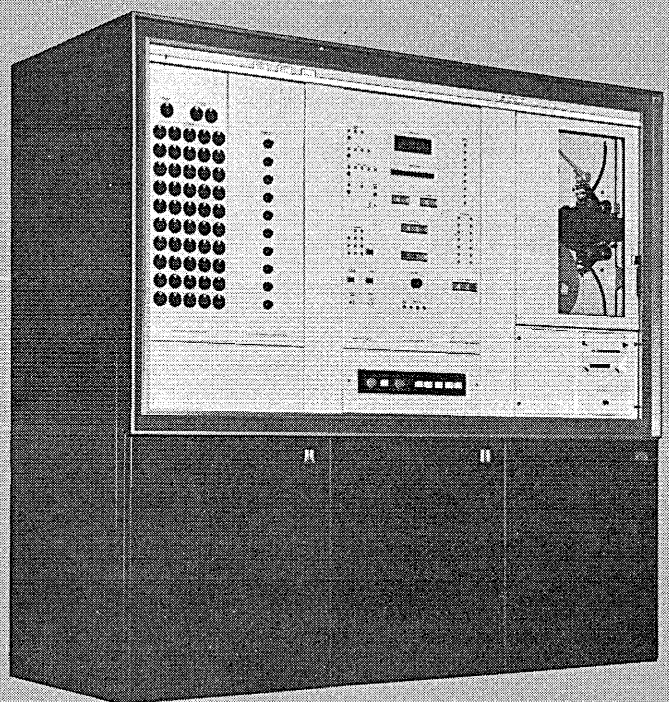

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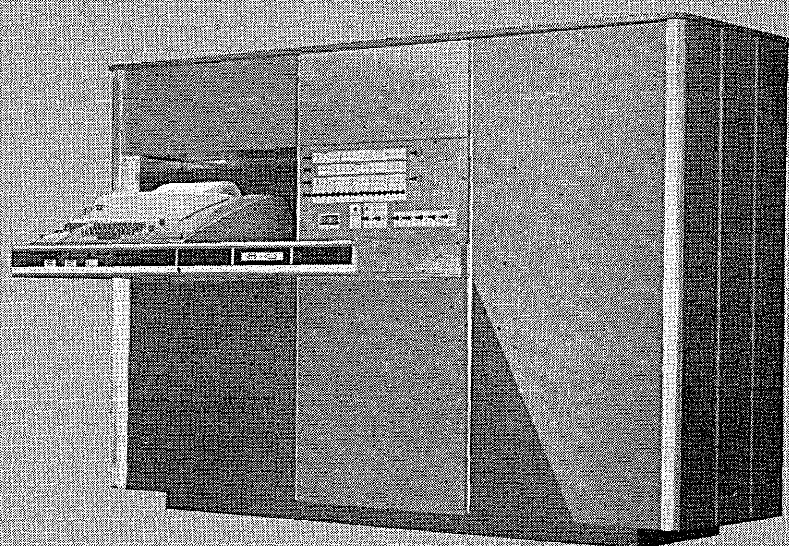

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CIRLE 51 ON READER CARD

ADAMS' COMPUTER CHARACTERISTICS

Fourteen new computers have been added to Section I of the "Computer Characteristics Quarterly," which covers general purpose, solid-state machines made in the U.S. They range from the tiny-scale Digiac 3080 to the super-scale CDC 6800, and include the Spectra 70's by RCA and the Series 200 from Honeywell. The quarterly publication, which also includes military and foreign computers, is available for $10 a year from Adams Associates Inc., 142 The Great Road, Bedford, Mass., which holds the copyright to this listing. ■

SECTION I

	Monthly Rental: Typical (Range)	First Delivery: Month and Year	Processor Speed: Complete Add Time in Microseconds	Storage Cycle Time in Microseconds	Internal Storage: Capacity in Thousand Words	Word Size	Magnetic Tape: Thousands of Characters per Second	Buffering	Read Forward and Reverse	Disc Storage: Capacity per Unit	Access Time in Milliseconds	Thousands of Characters per Second	Drum Storage: Capacity per Unit	Access Time in Milliseconds	Thousands of Characters per Second	Peripheral Devices: Cards per Minute In — Out	Paper Tape Characters per Second In — Out	Printer Lines per Minute	Off-line Equipment	Other Features: Program Interrupt	Index Registers	Indirect Addressing	Floating-point Arith.	Memory Protection	Byte. Manipulation	Console Typewriter	Software: Algebraic Compiler	Business Compiler
CONTROL DATA 6800	$85,000 (65-150)	/67	.1[C]	.25	131	60b	30-240	MR WC	√	74 M	190	1250	4 M	17	2000	1200 250	1000 120	1000[P] 150	3200	√	8	√	√	√	—	√	√	—
	C. Computer utilizes a high degree of parallelism in operations and in functional units of hardware. Approximately ten million operations per second are executed. H. Ten peripheral processors (each with its own 4096 twelve bit memory) are included. P. 136 columns on 1000 lpm printer. Two cathode ray display scopes are part of the console.																											
CONTROL DATA 6400	$45,000 (25-95)	1/66	1.1[C]	1	32-131	60b	30-240	MR WC[H]	√	74 M	190	1250	4 M	17	2000	1200 250	1000 120	1000[P] 150	3200	√	8	√	√	√	—	√	√	—
	C. Memory overlap increases effective speed. H, P. See CONTROL DATA 6800.																											
RCA SPECTRA 70/55	$25,900 (14-60)	7/66	9.72[C]	.84[D]	65-524	1a[F]	30-120	MR WC	√	7.25 M[K]	97.5	156	1 M	8.6	117	1435[M] 300	200 100	1250[P]	√[Q]	√	43[S]	—	√	√	√	√	√	√
	C. 5 x 5 decimal add. D. 4 bytes. F. Memory is organized in eight bit characters or bytes. K. 250 million character magnetic card files are available. M. 550 cpm reader and 100 cpm punch available. P. 132 position printers. 600 and 800 lpm printers also available. Q. RCA SPECTRA 70/15, 70/25, 70/45. S. Up to 16 general purpose registers for each problem state.																											
HONEYWELL Series 200 Model 4200	$25,000	12/66	7.5[C]	.75[D]	32-524	1a[F]	13-90[G]	MR WC	√	7.25 M	97	156	7.8 M[L]	25	102	800[M] 100-400	600 120	1260	same	√	6-30	√	√	√	√	√	√	√
	C. Add time assumes two five-character fields. D. .75 microseconds per 4 characters. F. Variable length instructions operate on variable length data fields. G. One-half and three-quarter-inch Tape Units available. L. Smaller drums available. M. Punch speed depends on the number of columns. 400 cpm reader also available.																											
CONTROL DATA 3300	$15,000 (12-30)	11/66	1.5[C]	.8	8-262	24b[F]	120[G]	MR WC	√	33 M	187	83	4 M	17	2000	1200 250	1000 120	1000[P] 150	—[Q]	√[R]	√[S]	√	√	√	√		√	√
	C. Overlapped core memory banks allow increased internal speed. F. Plus parity. G. Tape units IBM compatible. P. 136 columns on 1000 lpm printer. Q. Second 3300 processor may share memory and act as Satellite system. R. 64 lines. S. 3 hardware.																											
RCA SPECTRA 70/45	$12,500 (8-30)	7/66	21.46[C]	1.44[D]	16-262	1a[F]	30-120	MR WC	√	7.25 M[K]	97.5	156	1 M	8.6	117	1435[M] 300	200 100	1250[P]	√[Q]	√	43[S]	—	√	√	√	√	√	√
	C. Five-character decimal add. D. Per 2 bytes. F, K, M, P. See RCA SPECTRA 70/55. Q. RCA SPECTRA 70/15, 70/25. S. See RCA SPECTRA 70/55.																											
HONEYWELL Series 200 Model 1200	$9,000	2/66	33[C]	1.5[D]	8-131	1a[F]	13-90[G]	MR WC	√	7.25 M	97	156	7.8 M[L]	25	102	800[M] 100-400	600 120	1260	same	√	6-30	√	√	—	√	√	√	√
	C, F, G, L, M. See Model 4200. D. See Model 2200.																											
RCA SPECTRA Model 70/25	$6,000 (4-12)	12/65	33[C]	1.5[D]	16-65	1a[F]	30-120	MR WC	√	—	—	—	—	—	—	1435[M] 300	200 100	1250[P]	70/15	√	√	—	—	—	√	√	—	√
	C. Five-character add-decimal. D. 1-4 bytes. F, M, P. See RCA SPECTRA 70/55.																											
RCA SPECTRA 70/15	$3,000 (2.4-6.7)	10/65	56[C]	2[D]	4-8	1a[F]	30-120	RC	√	—	—	—	—	—	—	1435[M] 300	200 100	1250[P]	same	√	—	—	—	—	√	√	—	√
	C. Five-character add-decimal. D. Per byte. F, M, P. See RCA SPECTRA 70/55.																											
ASI ADVANCE 6040	$2,600[A]	10/65	3.8	1.9	4-32	24b	22.5-62[G]	MR WC	—	—	—	—	—	—	—	800 250	300 110	400[P]	—	√	3	√	—	—	—	√	√	—
	A. Price does not include magnetic tape. G, P. See ASI ADVANCE 6020.																											
HONEYWELL Series 200 Model 120	$2,500	2/66	105[C]	3	2-32	1a[F]	13-90[G]	MR WC	√	7.25 M	97	156	7.8 M[L]	25	102	800[M] 100-400	600 120	1260 450	same	√	6	√	—	—	√	√	√	√
	C, F, G, L, M. See Model 4200.																											
ASI ADVANCE 6020	$2,000[A]	3/65	3.8	1.9	4-32	24b	22.5-62[G]	MR WC	—	—	—	—	—	—	—	800 250	300 110	400[P]	—	√	3	√	—	—	—	√	√	—
	A. Price does not include magnetic tape. G. Tapes are IBM compatible. P. Incremental plotter and analog conversion equipment available.																											
DIGITAL EQUIPMENT PDP-8	$500 (.45-3)	4/65	3.2	1.6	4-32	12b	15-90	MR WC	—	—	—	—	262 K	8.4	16	200[M] 100	300 63.3	1000[P]	—	√	8	√	—	—	—	√	√	—
	M. 800 cpm reader available. P. See PDP-7.																											
DIGITAL ELECTRONIC DIGIAC 3080	$440[A] (.37-.6)	12/64	2000	17000	1-4[E]	25b	—	—	—	—	—	—	—	—	—	100 15	50 50	—	—	—	—	—	—	—	—	√	√[Y]	—
	A. No rental prices announced. Prices derived from purchase price. E. Magnetic Drum. Y. Available April, 1965.																											

1101

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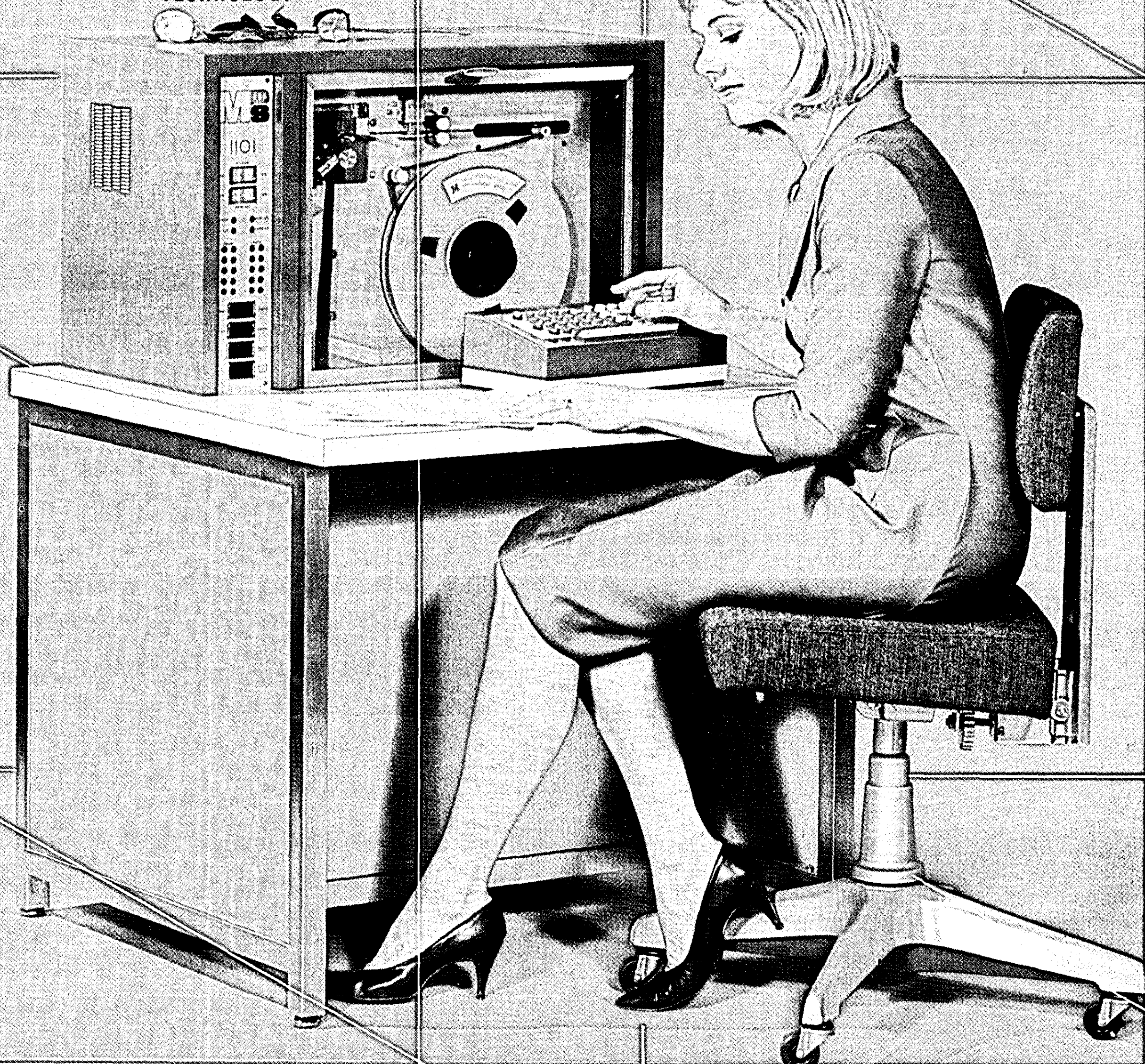

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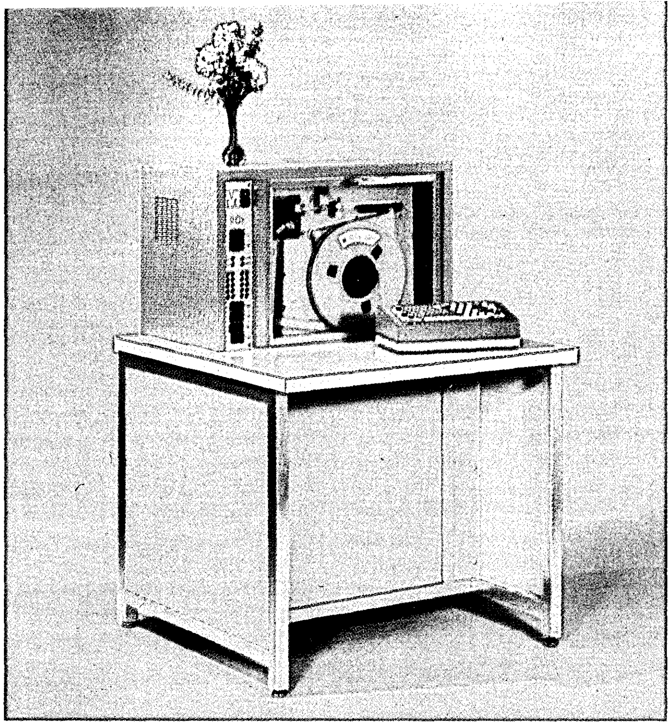

The 1101 color-coded keyboard is designed for maximum keying speed and minimum operator fatigue. It makes changeover of trained operators... from earlier, less efficient keyboard equipment . . . as easy and fast as possible. Keyboard is movable for operator convenience.

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101 KEYED DATA-RECORDER TRANSCRIBES DIRECTLY FROM SOURCE DATA TO COMPUTER MAGNETIC TAPE AND VERIFIES

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AN 1101 "EXCLUSIVE" . . . The 1101 now makes it possible to transcribe information from source documents DIRECTLY to the usual ½″ magnetic tape, on standard reels . . . and to verify the accuracy of the transcription. It combines, in a single 024-size unit, the functions ordinarily performed by a Card Punch, Key Verifier and Card-to-Tape conversion runs. Operation is in any of three modes: ENTRY (original recording), VERIFY, or SEARCH. Desired mode is obtained by a simple switch setting. Machine-function programming flexibility is provided for each mode.

UNMATCHED SAVINGS WITH THE 1101 . . . No punched cards • Less main frame time just to "get in" • Reduced lag time from source to report • Reduced interpreting requirements • Automatic right justification (left zero fill) • Keyboard correction of "sensed" errors during entry, and of those found in verification • 1101 permits and encourages an even keying cadence for greater operator production ✓ ✓ ✓ Skipping speed is over 150 times faster than in existing models • Duplicating speed is 600 times faster • Almost silent operation reduces operator fatigue . . . actually, the sound was deliberately built-in to satisfy the operator • Right-hand justification . . . **at no extra cost** . . . eliminates need for field positioning arithmetic and decision . . . fewer operator decisions ✓ ✓ ✓ Data entry location improved by large illuminated position display • Tape requires less filing space than cards • Greater security of information . . . less danger of losing records on tape than on cards • Work scheduling is flexible . . . no lost time waiting for the right machine • Less down-time and maintenance with completely solid-state electronic elements than with electro-mechanical equipment.

OPTIONAL DEVICES . . . DATA DISPLAY—permits checking of memory content • UNIT RECORD COUNTER . . . counts number of records on tape • SELF-CHECK DIGIT DEVICE . . . arithmetically proves correctness of number at time of entry • ALTERNATE PROGRAM . . . allows two record formats in one run.

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WORLD REPORT

BULL-G.E. ANNOUNCE COMPATIBLE 100'S

Following the now-established 1965 vogue for small and low-cost computers, Bull-General Electric have come out with the Compatibles 100, consisting so far of the Gamma 115 and the 135. The latter is for general release this month; the former is the Olivetti-developed model (see p. 67). Upward compatible with the 400's, their basic prices are $100K and $150K, respectively.

Introduction of this series brings disc file systems in Europe to an almost record low price. An 8K (8-bit-character) Gamma 115 with 2.95-million characters on discs costs around $150K. There is also compatibility between the 100's and Bull's Gamma 10, a $75K punched card computer with orders and installations exceeding 500.

EAST GERMANY BARTERS FOR WESTERN COMPUTERS

First inkling of the real size of potential computer business in Iron Curtain countries has come from East Germany. Following the Leipzig Fair, negotiations are underway with at least three manufacturers for 12 systems in the $600K to $1.5 million class.

The three are reported to be West Germany's Siemens, and the U.K.'s Elliott Automation and ICT. Total value of contracts: $15 million. This is only a fraction of the business that may be expected, according to Minister for Electronics W. Bohme, who spoke of the economy's urgent need to boost information processing facilities. Next on the agenda: large-scale orders for process control systems.

Initial orders are said to be for econometric and scientific computing. Buyers include the optical firm, Zeiss, and textile and chemical companies. Rated fifth among the world's industrial economies, East Germany has only about a dozen computer facilities stocked with locally-made Robotron's, reminiscent of the 650.

U.K. VERSION OF BOB REPORT GETS MIXED REVIEWS

For months, Britain's computer industry has been cliff-hanging in anticipation of a national computer policy promised by the Ministry of Technology. After initial cries of exultation, some Jeremiahs are already casting doubts on its effectiveness for uplifting a sagging industry.

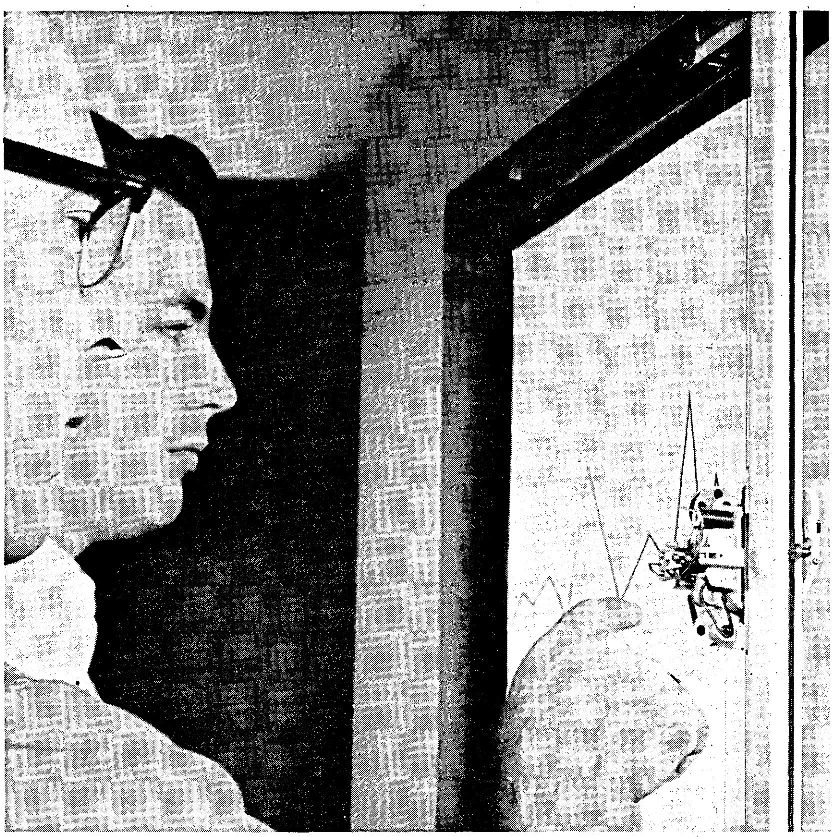
Main points of the administration's plans are $30 million of government money over five years for increasing university facilities; a powerful central advisory body to review all computer purchases in the public sector; much more financial assistance for R&D; and possible establishment of a National Computer Program Library.

Most important plan is the advisory body to supervise the public sector, which covers all utilities, state-sponsored industrial research groups, and universities. With an expected buy-British policy, this would wrap up 30% of the market in terms of installations, considerably more in cash.

PHILIPS AND ELECTROLOGICA MERGER IS RUMORED

Slumbering Dutch electronics giant, Philips GMbh, seems poised to make its long awaited entry into the market. Current reports say that the firm is about

Continued on page 81

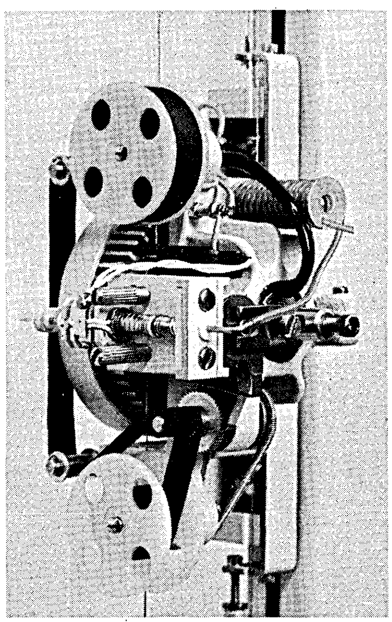


If you really care what your data-display dollar is buying...

Take a cold, hard look at Milgo's New 30"x 30" Vertical-plotting X-Y Recorder.

Compare it for speed. Repeatability. Accuracy. Reliability. Plot visibility. Add-on flexibility. Versatility. Quality. Floor space. Delivery time.

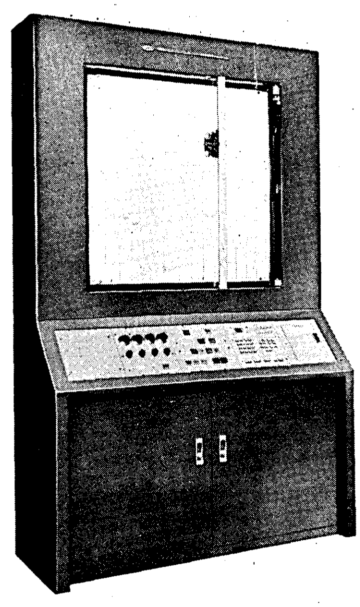
The Milgo solid-state 4021D X-Y Recorder accepts on-line digital inputs from any digital computer; off-line inputs from magnetic tape, punched paper tape, punched cards, a manual keyboard or an analog source. The pen/printer draws lines, curves, and point-plots; it symbol prints with a 50 character symbol printer. Pen and symbol printer interchange electronically in milliseconds. The pen/printer has a slew of 30 ips, with a continuous writing speed of 20 ips. The pen/printer point-plots in either pen or symbol mode at 500 ppm. It prints a random selection alpha-numeric character at 300 per minute. The plotting surface is evenly back-lighted by a variable powerstat control. Plots are clearly visible for 10 feet or more. The complete unit only occupies a 50 by 18 inch floor space. The 4021D was developed and is produced to military standards of quality and



reliability. It is rugged and of modular construction. Installed and operating, it has the lowest feature-for-feature price tag of any 30 by 30 inch plotter available to industrial and commercial users.

Take a cold, hard look, for instance, at the symbol printer and its integral pen and inking system.* The complete unit is 1/3 to 1/4 smaller than competitive units. It has no dangling umbilical cord. Pens are low-mass, jewel-bearing suspended, solenoid actuated. Capillary action prevents spilling at any slew speed or acceleration, and the ink reserve can be filled without disassembly. Ink supply is indicated visually. The arm, only 1 1/4 inches wide, is servo-motor driven at both top and bottom. It is ball-bearing mounted on stainless steel rails, precision ground to within 0.004 inch. It allows accelerations of 400 ips^2 in both X and Y; provides static accuracy within ±0.05% of full scale, and repeatability of ±0.02%.

Milgo offers analog and/or digital recorders in vertical or horizontal models with plotting surfaces up to 45 x 60 inches. If you need to know what your "data-display dollar" can buy, call Tom Thorsen,



Marketing Department, at Milgo Electronic Corporation, 7620 N.W. 36th Avenue, Miami, Florida 33147. Phone: 305 691-1220. TWX: 305 696-4489.

*U. S. Patent No. 3,120,214.

milgo

Continued from page 79

to take a major stake in its tiny neighbor, Electrologica. While Philips hotly denies any such intention, local pundits say talks between the two are an open secret and cooperation between them should begin about May-June. Outcome of such arrangements is expected to be directed toward Philips' activity in military and data communications spheres. The company already has several million dollars staked in fixed-program, wired-in-logic, message switching computers.

NEW RUSSIAN COMPUTER SLATED FOR EXHIBITION

Russia will show her computer prowess at a new Computer Pavilion in the Permanent Exhibition of Achievements in Moscow. Most of the systems to be viewed in coming months are reported to have strong scientific and industrial control backgrounds. But in May, a special show will be devoted to gov't. DP.

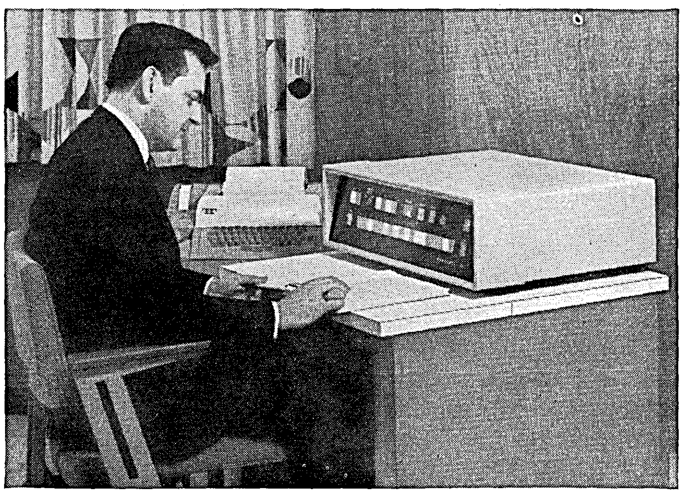
New machine in the line-up is Dnipro 1. Specified as a gp model for control and dp, it is a fixed-point, parallel logic, two-address machine. Capacity is 2,048 to 5,120 (26-bit) words of ferrite in modules of 512 words. Using 6-channel paper tape input, it includes 128-word, plug-in modules for various hardware program functions. Add/subtract times are reported as 125 usec.

Also described in Nauchno-Technicheskie Obshchestra is a fluid logic system, USEPPA (universal system of industrial pneumo-automatic elements). It has three elements: a repeater, fluid amplifier, and a memory element built up from a repeater and amplifier. These components are constructed of laminated plastic with appropriate air channels. Control systems built of USEPPA components have a frequency response of 10 cps. Mass production of computers using these principles is believed to be planned for the Tizpribor industrial automation production plant.

ODDS & ENDS

Japan has moved into second place in the number of computers installed in the Free World. Figures for the end of '64 place the number at 2,000-plus... The Madrid Central Post Office is to install an automatic mail handling system developed by Standard Electrik Lorenz, ITT's German subsidiary (see Sept. '64 Datamation)...A new industrial control machine from Elliott Automation, the Arch 101, will be made and marketed in the U.S. by E-A Industrial Corp., Los Angeles...The Japanese National Railways has test-operated a completely unmanned electric (passenger) train by remote control. It is said to be the first that used an actual train in service. The computer: a Raytheon 250...Call for papers is out for the second British Joint Computer Conference, May '66. Send to Conference Secretariat, Institution of Electrical Engineers, Savoy Place, London WC2...NCR, perking up Down Under, has an order from a South Australia bank for what will be the first on-line system, linking tellers at major branches to a 315... Visiting the island continent May 3-5 to discuss the social/economic effects of automation on Australia will be the U.S.'s John K. Galbraith and Marion B. Folsom (former secy. of HEW), the U.K.'s Norman Fisher and Lord McCorquodale, and the pres. of Sony, Masaru Ibuka...One megabuck is the rumoured price of a CDC 6400 for the U. of Adelaide, still being negotiated.

Announcing the Honeywell 20 Digital Control System



Its low cost, new programming language, accuracy, and speed offer practical solutions to real time system needs.

Designed to handle a wide range of real time and scientific applications, the Honeywell 20 System incorporates either of two central processors—the H21 with a memory cycle time of 6 microseconds or the H22 with a cycle time of 1.75 microseconds. The Honeywell 20 is available either as a component for user systems or as a fully integrated control system. Prices start at $21,000 for a central processor with input/output typewriter and integral tape punch and reader. A typical small control system with a 4K core memory, analog and digital input/output subsystems, A/D and D/A converters, real time clock, and an input/output typewriter costs approximately $55,000.

The H20 System includes a number of hardware and programming features seldom found in a low-cost system:

18-Bit Word Length—plus parity and memory guard bits.

Single Word Instructions—provide 8192 directly addressable core locations.

CONTROLWARE—advanced software package, featuring CONTRAN, also includes FORTRAN II and CAP assembly system.

Core Memory Capacity—2048, 4096, 8192 or 16,384 words of memory prewired for field expansion.

Priority Interrupts—up to 32 hardware levels, with up to 144 interrupt lines per level.

Direct Memory Access—independent path to memory for external I/O operations on a fully buffered, cycle-steal basis.

Three-Address Register Commands—three-address arithmetic and/or logical operations with single word, one cycle, instructions.

Hardware Multiply—a standard feature.

Power Failure Protection—automatic program shutdown and restart without loss of data.

CENTRAL PROCESSORS

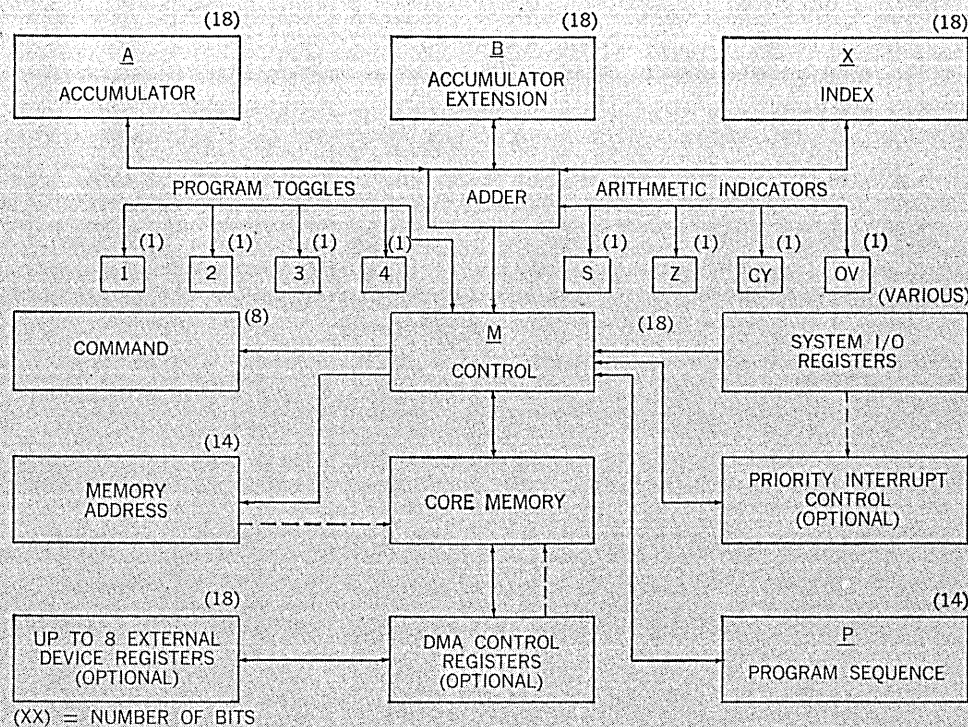
Type—Binary, 2's complement arithmetic, single address.

Typical Operating Speeds—(In microseconds, including memory accessing and indexing.)

	H22	H21
Add	4.8	12.0
Logical	4.8	12.0
Load/Store	4.8	12.0
Multiply	25.0	54.0

Circuitry—Hybrid circuit construction using microcircuit techniques and silicon semiconductors. Environmental: 32-120°F.

Memory—Magnetic core, random access.



INTERNAL REGISTER DIAGRAM—The internal register organization of the Central Processor is shown in the block diagram. Programmed input/output data is transferred in parallel via the M register to or from core memory without disruption of arithmetic registers. Four arithmetic indicators facilitate testing of zero, sign, carry, and over-flow conditions. Four program toggles provide a convenient means of setting and checking program flags. The optional direct memory access registers provide an independent path to memory for high speed devices.

Address Modification—Indexing, indirect addressing.

Parity—Checked or generated on all memory, character input/output, and high-speed direct memory access operations.

Options—Multi-level priority interrupt, direct memory access auxiliary drum memory, magnetic tape unit, high speed paper tape punch, and reader.

INPUT/OUTPUT SUBSYSTEMS

Low-Level Analog Inputs—Standard scanning speed of 200 points per second with an overall accuracy to within ±0.05% full scale on 0 to 50 mv range. Expandable to 1024 inputs.

High-Level Analog Inputs—Scanning speed up to 8,000 points per second with an overall accuracy to within ±0.025% of reading ±1.5 mv on 10 volt range. Expandable to 256 inputs.

Digital Inputs—Transfer speed up to 360,000 bits per second (contacts or voltage levels); up to 1440 inputs in modules of six; up to 240 pulse input counters per system.

Analog Outputs—Solid state D/A converter provides 10-bit resolution; up to 120 outputs in modules of one; up to 720 stepping motor drivers in modules of three.

Digital Outputs—Transfer speed up to 360,000 solid-state switching operations per second, each output individually buffered; up to 1440 outputs in modules of six; on-off (latching) and pulse duration (10 milliseconds to 1 second) types.

CONTRAN

CONTRAN (CONtrol TRANslator) is an advanced compiler-level language combining the most desirable features of FORTRAN IV and ALGOL 60. It is a new concept in multi-programmed, time shared, real time programming.

CONTRAN solves the complex programming problems normally encountered in: the use of a shared primary memory with auxiliary bulk memory; linkages to executive control; responses to asynchronous external interrupts; inter-program communication; compilation and debugging of both related and unrelated programs while the system is performing on-line control.

System programs can be added, deleted or modified on-line providing new opportunities for "live" studies. For the first time, entire real time systems can be programmed in compiler-level language.

For more information, write to

Honeywell

Special Systems Division, Pottstown, Pa. 19464

CIRCLE 37 ON READER CARD

As much as $100,000 of the cost of a hybrid computer went into a non-productive linkage system.
Until Thursday*
When Raytheon Computer introduced the all-digital TRICE/440

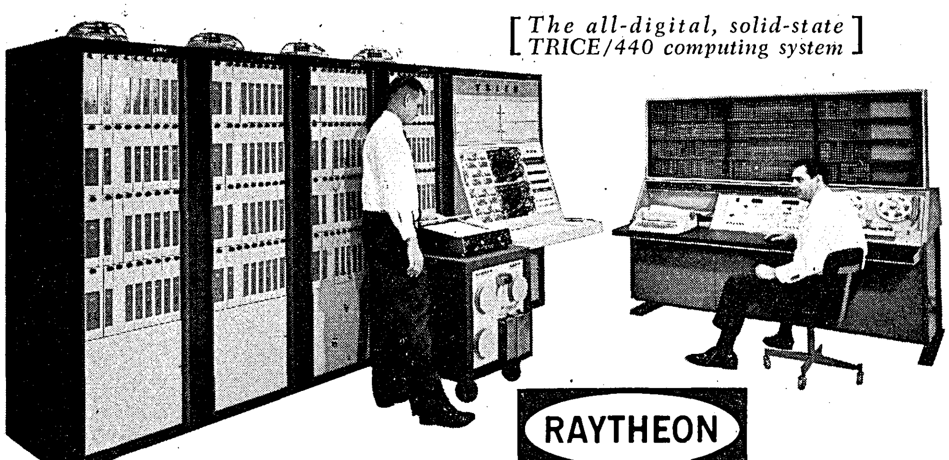
Raytheon Computer's TRICE®/440 hybrid computing system puts $100,000 more of its cost into computing capacity and power than a conventional analog-digital hybrid. Because TRICE/440 is all digital, the usual multi-channel conversion system is eliminated, increasing accuracy and reliability as well as computation efficiency.

Like its analog equivalent, TRICE solves dynamic problems with computing elements programmed through a patchboard. But TRICE is a digital differential analyzer. As such, it offers six-digit accuracy, stability and repeatability, basic dynamic range of $\pm 2^{26}$ with automatic rescaling for applications requiring wider range.

In a typical aerospace simulation, TRICE solves orbital and trajectory equations while the 440 digital computer, with its stored logic, simulates a guidance computer's exact command structure, data format and word length. The 440's 3 microsecond and 200 nanosecond memories make it suitable for real-time applications. Because the two elements of the system are digital, unlimited exchange of variables between the two is possible.

For application data and specifications, write today for Data File H-104J. Raytheon Computer, 2700 South Fairview Street, Santa Ana, California 92704.

*Since Thursday, September 10, 1964, the new TRICE/440 has been solving problems for NASA's Marshall Space Flight Center, Huntsville, Ala., and Manned Spacecraft Center, Houston, Texas.



[The all-digital, solid-state TRICE/440 computing system]

CIRCLE 40 ON READER CARD

NEWS BRIEFS

MONOLITHIC I.C. COMPUTERS ANNOUNCED BY ASI

Three processors have been added to the upward-compatible ADVANCE series of computers by Advanced Scientific Instruments, Minneapolis, Minn. Supplementing the 6020 and 40 are the new 50, 70, and 80. They're designed, respectively, for the gp scientific user, the systems market, and time-sharing applications. Memory cycle time for each is 1.9 usec, and add time is 3.8 usec. Using 24-bit words, memory capacity is up to 32K words of core. Monolithic integrated circuits are used . . . and have been added to the 6040.

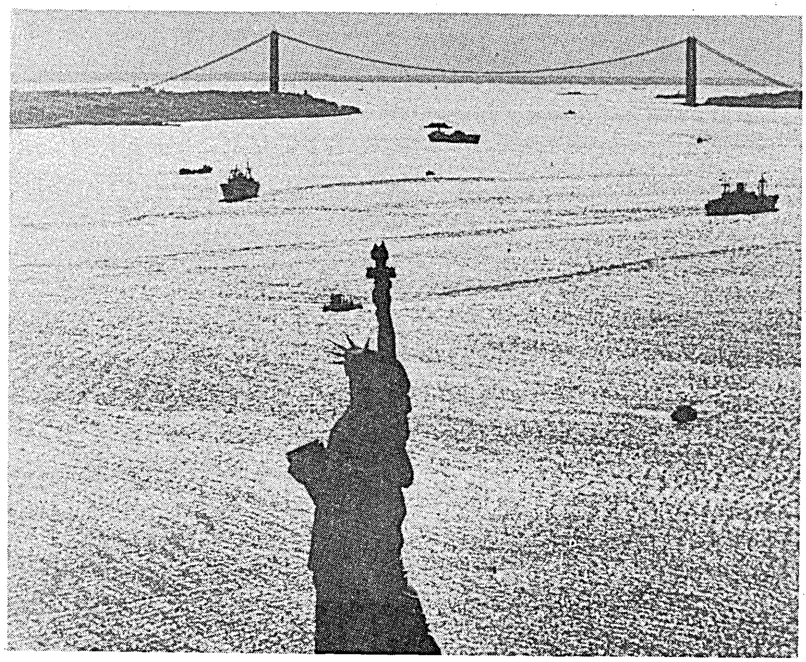
The 6070 features the capability of having multiple processors in the mainframe, running up to six simultaneous operations. Multiply times for the 6050, 70 and 80 are 7.6, 7.6 and 5.7 usec, respectively. Double-precision floating point multiply times (39-bit mantissa, 9-bit exponent) are 17.1 usec for the 50 and 70, and 11.4 usec (24-bit mantissa, 9-bit exponent) for the 6080.

Software will include a one-pass extended FORTRAN II, a one-pass symbolic translator, and operating system. Monthly rentals for systems begin at approximately $2,800, $3,600 and $4,200, and prices at $104K, $132K and $152K. Deliveries are reportedly scheduled to begin this year.

THREE UNIVERSITIES JOIN IN IR PROJECT

The first cooperative information retrieval system among university libraries is being developed by Yale, Harvard, and Columbia. By 1966, the medical libraries of the schools will have a central book catalogue and journal index stored in a computer at New Haven, Conn. On-line typewriter inquiry units and card readers will be installed at each station for retrieval and updating of information. The libraries have already begun putting book data on punched cards for production of catalogue cards and periodic accession lists and for computer input. Only those books produced since 1960 and journals most often used are being included in the computer catalogue which is expected to

IFIP CONGRESS 65 CONVENES IN NEW YORK MAY 24



IFIP Congress 65 will bring more than 5,000 scientists and engineers from 50 countries to the New York Hilton Hotel, May 24 to 29. This third IFIP meeting, chaired by W. Buchholz of IBM Development Laboratory, features the Interdata 65 Exhibition (May 24-27), 76 technical sessions, and reports in the closing session on "Man as an Information - Processing System." Also included are a wide variety of special events and tours.

The technical program, headed by A.S. Householder of Oak Ridge National Labs, is broken down into five general areas: Information Systems (area chairman, J.C. McPherson, IBM Systems Research Institute), Programming (M.K. Woodger, National Physical Laboratory, U.K.), Automata Theory and Switching Theory (V.M. Gloushkov, USSR Academy of Science and Ukrainian Academy of Science), Equipment Design (Prof. J.R. Pasta, Univ. of Illinois), and Mathematical Methods (Prof. J.L. Lions, Univ. of Paris). The five general sessions to be held on these areas will present 15 invited papers.

The 11 special sessions, with 35 invited papers, include: "Mathematical Methods of Optimization," "Partial Differential Equations," "The Future of Switching Elements," "Outlook in the Memory Area," "Organization of Large Storage Systems," "Artificial Intelligence," "Programming Theory," "Programming Practice," "Mechanical Translation," "Design of Information Systems," and "Automata Theory and Switching Theory." Informal discussions on more narrowly defined areas will be held during the symposia, each of which will have five or six short talks, and during the panels.

Highlighting the closing session May 29 will be talks by Heinz Von Foerster, "How to Tell the Birds from the Bees: The Ontogenesis of Information;" Warren S. McCullough and W. L. Kilmer, "The Command and Control System of the Vertebrates;" and Donald M. MacKay, "Information in Brains and Machines."

contain about 750,000 items. Programs for the IR system are designed for a 4K IBM 1401, although purchase of a new computer system is planned.

Five other northeastern universities have been invited to join the network. Among advantages expected from the cooperative venture are an increase in average number of subject headings per book because space problems are eliminated (Yale, which had a 1.6 average per book, now reports a 10.4 average); one-third cost cut in cataloguing current books by eliminating duplication; and easy printout of the catalogue in book form. Future plans include adding graphic transmission systems to the network to eliminate some duplication of materials among the libraries.

THE LONG AND THE SHORT OF COMPUTERS & HIGHWAYS

A nationwide, computerized traffic control network was proposed at the recent annual symposium of the Society for Information Display. According to Dr. Edith M. Bairdain of ITT's Data and Information Systems Div., Paramus, N. J., the network would consist of monitoring devices at entrance, exit, and toll points, capable of scanning windshield stickers bearing pertinent information. It would thus aid law enforcement agencies that have access to a mass data bank ("Be on the lookout for car number . . ."), would warn of traffic congestion ahead ("Detour at St. Louis to avoid floodwaters at Oklahoma City"), and, perhaps most important, make our highways safer. Unfortunately, the lady scientist was unable to deliver her prepared talk; she was recuperating from a traffic accident.

Meanwhile, the Illinois Dept. of Public Safety has installed a 1401 for crime control and highway safety. It is reportedly "the first state to put computers to such effective use in the field of law enforcement."

RESEARCH LAB CONDUCTS ON-LINE BLOOD SAMPLE TESTS

On-line testing of blood samples, said to be an industry first, is underway at Kings County Research Laboratories Inc., Brooklyn, N. Y. Linked to an IBM 1710 control system are 20 Auto Analyzers, which automatically perform up to 10 tests on one sample of blood, and output graphs. Full testing on-line is said to require two minutes, contrasting with 2-3 hours when done manually. In addition, the system reportedly increases reliability and accuracy, and enables the doctor to get formatted, printed results.

The 1710, which can handle up to 200 testers, monitors the performance of the analyzers during tests. When completed, readings are transmitted through a 1711 a-d converter to the computer for comparison with standard and control test values, and the computation of results. Retest is indicated when readings are outside the limits of the control values.

GE-400'S GET PERIPHERALS, TIME-SHARING HARDWARE

Hardware to accommodate time-shared, multiprogrammed operations and to perform scientific computations, as well as seven new peripherals, have been announced by General Electric for the Compatibles/400 family of medium-scale computers. In addition, the access time for the 415 has been cut by 40%, from the former 2.3 to 1.45 usec.

New additions for the central proc-

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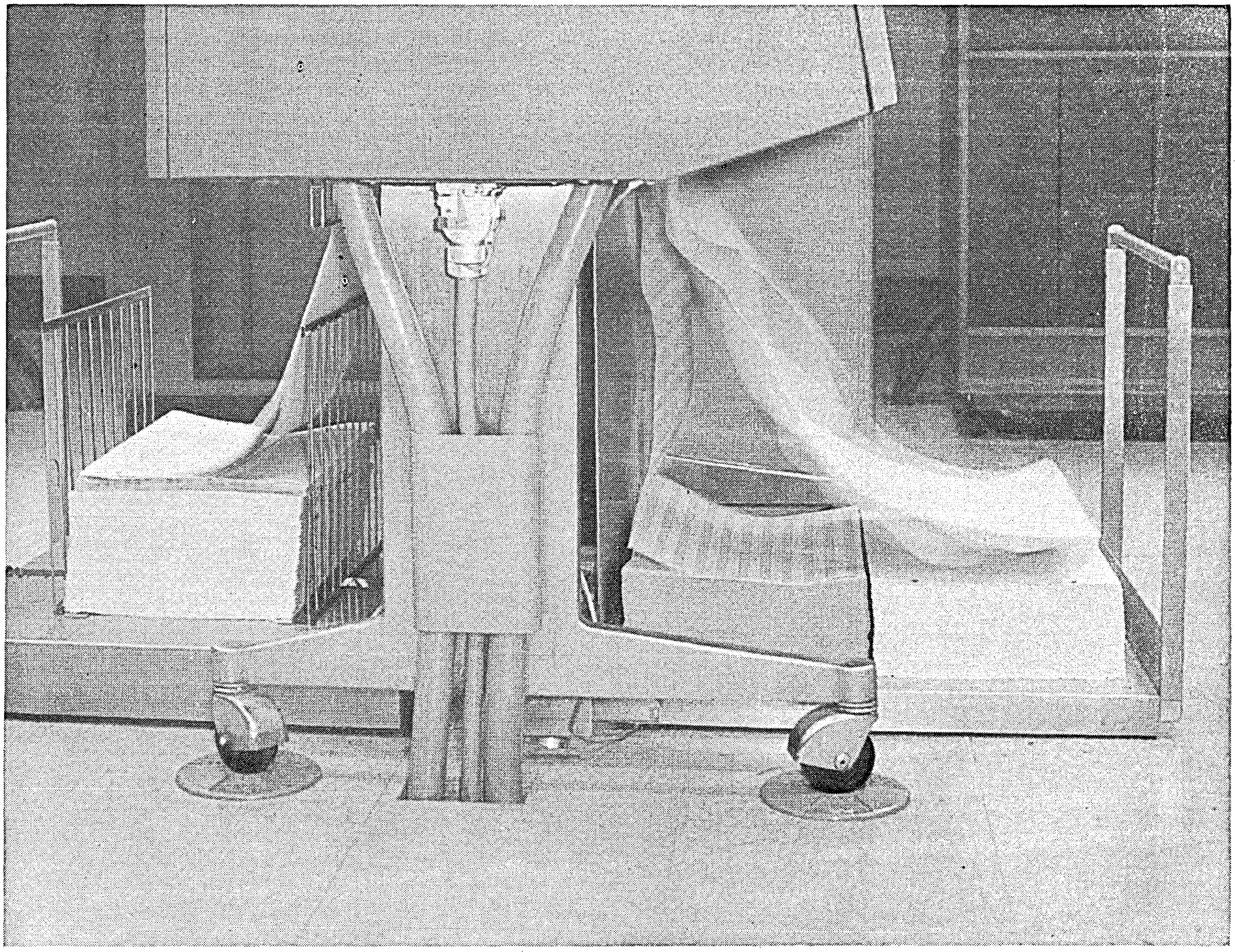

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CIRCLE 38 ON READER CARD

essor include a real-time interrupt clock, memory protection, symbol-controlled movement of blocks of data within memory, more I/O channels, and non-stop mode for switching from one program to another. Floating-point arithmetic units enable the 415, for example, to multiply in that mode in 21.8 usec.

Peripheral devices include a magnetic strip storage unit holding 532 million characters (link eight units and there are four billion characters on-line) and an average access time of 550 msec; a large disc file with a capacity of 800 million characters, and a small unit with a one-disc cartridge holding eight million characters; drum memory storing 12 million characters; and a single- and multi-line communications controller.

PLAN AHEAD: WINTER IN VEGAS

The deadline for papers to be presented at the Fall Joint Computer Conference in Las Vegas is June 15. Initial expressions of interest, with a working title, also are being solicited. Papers on social implications, in addition to surveys and R&D reports, are encouraged. Send a complete draft copy and a 150-word abstract to Mr. Robert Gray, Secretary, Program Committee, 1965 FJCC, P. O. Box 49, Santa Monica, Calif. 90406. The meeting will be held Nov. 30-Dec. 2, 1965.

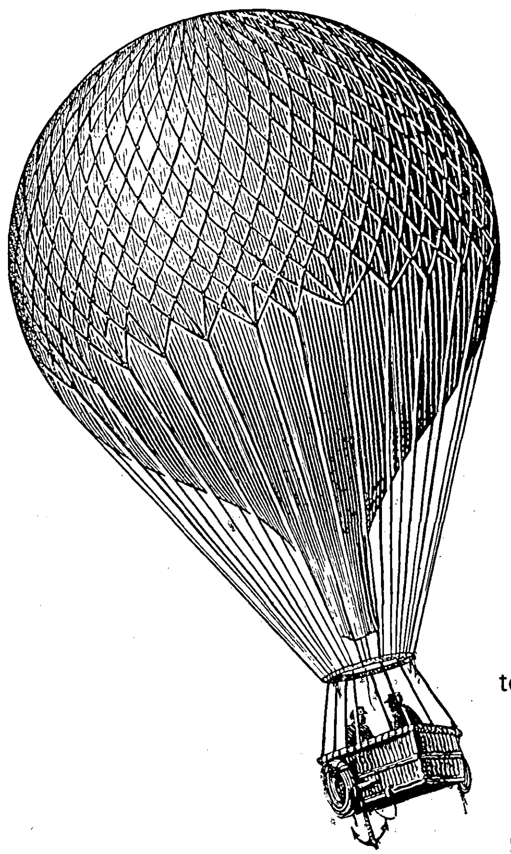
NEW YORK CENTRAL RAILROAD ADDS CAR DISPLAY SYSTEM

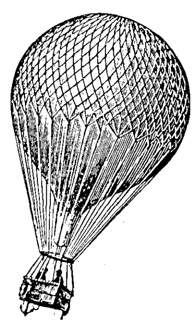
New York Central Railroad has cut answer-time in its boxcar-tracing service from minutes to 140 msec by installing on-line display units at its New York offices. Tied in to an IBM 7010, seven Data Display Inc. Model 10 units can retrieve information on any of the 125,000 freight cars on the line's 10,000 miles of track. Typewriters are also connected to the displays for printout of answers. Typewriter inquiry units were previously used for tracing. It is planned that IBM 1050's will be installed in five cities for remote access to the 7010.

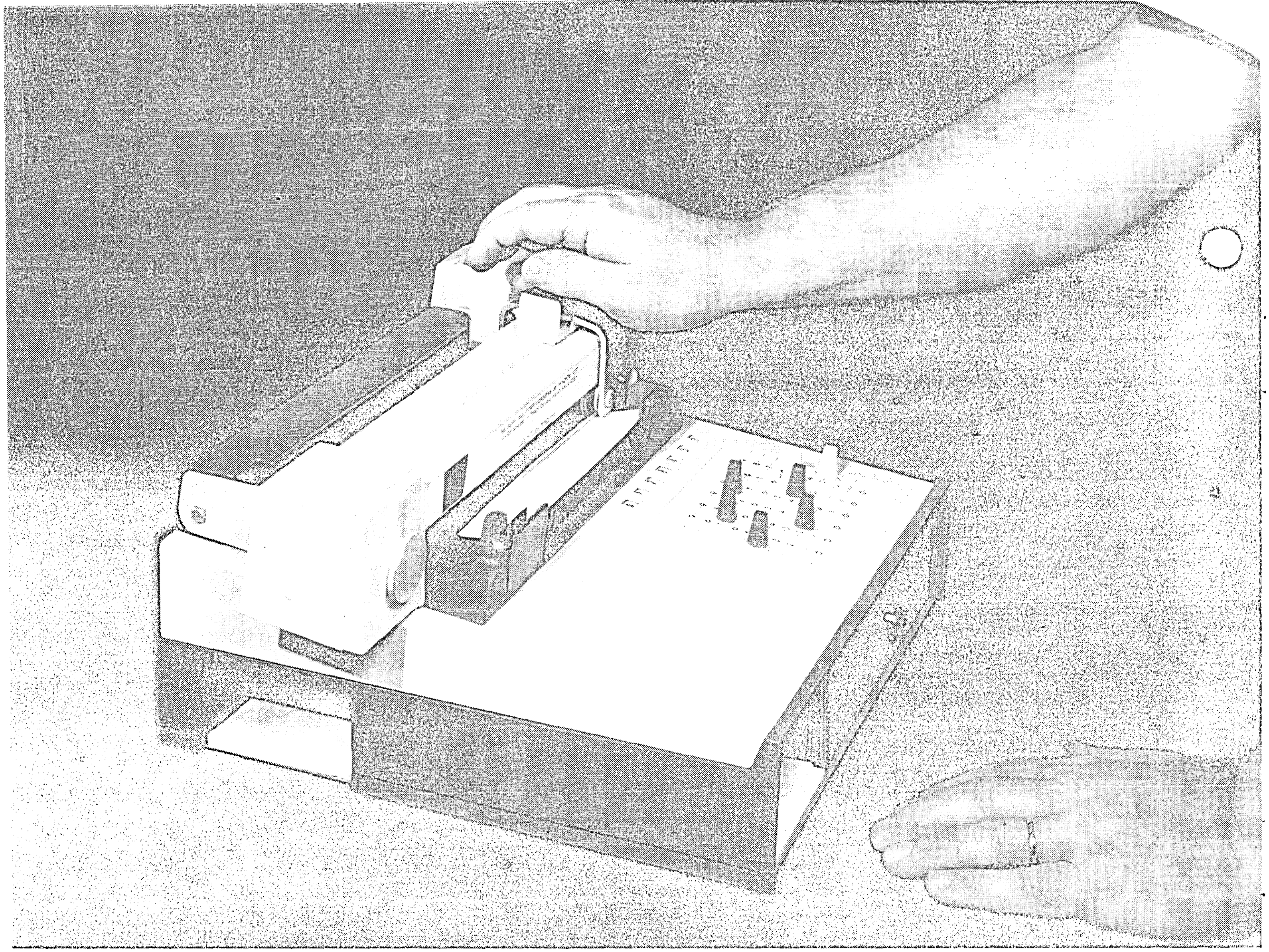
The Car Display system is part of a large communications and computer system NYC has been developing since 1963. Included is a $1.5 million Collins Radio communications system, called Data Central, which handles up to 10 million characters a day. Coded messages and data are transmitted from 259 remote points to the system where they are directed to designated circuits on a priority basis and, in the case of freight data, stored in a memory system for readout on magnetic tape.

● A programming contest for users of time-shared systems, similar to that held at the last Fall Joint Computer Conference, is being planned for the IFIP Congress 65 in New York City. Sponsor will be the ACM's Special Interest Group on Time-Sharing. For details, contact Prof. John McCarthy, Computer Science Dept., Stanford Univ., Stanford, Calif. 94305.

● Citizens National Bank of St. Petersburg has offered up on-line use of its NCR 315 system to correspondent banks. About 30,000 demand deposit accounts of four participating Florida banks are now stored in CRAM units. Through a Teletype inquiry unit, each bank can inquire about accounts and issue "hold," override, or correction control. Also included in the data service are daily updated account statements, sorted checks and deposit slips, and report journals.







with). Therefore, the program must display many continuously-varying quantities in familiar engineering units, print or tape extensive on-line records, accept sudden requests to display arbitrary new sets of data along with the programmed data, and be prepared to branch immediately into emergency hold or shutdown routines held continuously in core.

The standardizable I/O equipment is similar to that in most other types of real-time equipment-control systems. Because it involves a mixture of solid-state switching, relay switching, and analog functions, its internal timing details can be complicated. It provides many opportunities for subtle program errors or equipment design errors, and a crash project can degenerate into an acrimonious engineer-vs-programmer debate because of problems in this area. In addition to the opportunities for error, it also can provide challenges to the computer and the programmer. For example, sometimes it is considered necessary to check the entire configuration of all discrete outputs in the time after one discrete output is changed, but before its corresponding relay contact begins to move. The reason behind this requirement is obvious — to prevent blowing up a space ship from a minor transient in the computer I/O— but the program speed problem it poses is equally obvious.

The specialized test-station equipment has no real counterpart in other computer fields, except perhaps airborne guidance and control. Military weapon systems especially harbor all sorts of high-frequency, low-frequency, digital, pneumatic, hydraulic, optical, . . . signals, all with their own interactions and dynamic characteristics, which must be suitably generated or measured by the automatic test system. If the test engineer and programmer are lucky, and the prime equipment is some simple servo subsystem, the specialized test equipment may be only a few power supplies, signal isolators, and a variable-frequency audio oscillator. More typically, however, to test prime equipment large enough to be considered a complete system, the specialized equipment may occupy three to 300 racks. Fortunately for the programmer, (1) much of this equipment can be checked out independently, so that he does not see it until it is reasonably well debugged; (2) much of it can be considered just transducers (with associated delay times) by the program, and (3) it is usually closer to the test engineer's heart, and therefore higher on his priority list in case of trouble. *Un*fortunately for the programmer, inaccurate or obsolete documentation of this complex equipment's programming characteristics can knock irreparable holes in a program checkout schedule.

With this brief introduction to what an automatic tester is, we can proceed to talk about its programming.

programming

An automatic-test program bears the same relation to an automatic tester as a detailed "cookbook" test procedure bears to a human tester. Preparing either a program or a "cookbook" procedure can demand considerable engineering. However, since the automatic tester can neither think by itself nor learn from experience, an automatic tester program must be more detailed and more specific, and must anticipate beforehand all of the unlikely eventualities which the tester might have to handle. Therefore, the automatic tester program will probably require considerably more engineering effort than most manual "cookbook" procedures.

For purposes of discussion, we might consider automatic-test programming as consisting of four phases:

(1) Analysis and Program Design — typically 30 to 40% of the programming effort
(2) Coding — typically 15 to 20%
(3) Checkout — typically 40 to 50%
(4) Additional Documentation — typically 0 to 5%

It begins with a verbal, rather general, statement of what the test must do. It is completed only when a roll of tape (or equivalent) exists which will cause the tester to do exactly what was desired. This is, of course, a much larger task than coding. It includes many items which are more like engineering than "pure" programming, but which must be performed by the programmer.

analysis and program design

The peculiar problems of automatic-test programming become apparent immediately, in the earliest phases of analysis and program design. Rather than beginning with generalities about "communication," "documentation," and "definition of the problem," let us look directly at a hypothetical but rather typical example, Fig. 2. Fig. 2a is the general objective of the test. Sometimes this is all the programmer gets. Fig. 2b is an extract from a portion of the corresponding manual test procedure — not really specific enough in some areas, and without instructions as to what to do in case of a failure, but quite typical of a manual "cookbook." The parenthetical note about A203's function is an unusual unsolicited gift. To avoid excessive expansion of the figure, this shows only a portion of what is implied by Fig. 2a.

Fig. 2. Hypothetical example of analysis and program design (five parts, figures 2a through 2e, attached)

Fig. 2a. Statement of test requirement

. . . .
Check performance of servo actuator.
. . . . .etc.

Fig. 2b. Manual test procedure

. . . .
Actuator response check, turn-on:
Connect oscilloscope to Test Point A203. Set sensitivity to 1 v/cm and sweep speed to 1 msec/cm. (A203 = actuator feedback pot arm)
Connect oscilloscope trigger input to Test Point A207. Set controls for single sweep, externally triggered, positive slope and level.
Connect a switch from Test Point A207 to Test Point A001. Adjust oscilloscope trigger level and stability so that switch closure triggers oscilloscope.
Observe transient oscilloscope pattern when switch is closed. Waveform should be:

	no "jogs"
smooth curve;	less than 8 msec
not sudden	after start of
break from	trace
zero	

Actuator response check, turn-off:
. . . . .etc.

Sometimes the manual test procedure does not exist. Sometimes the existing manual procedure is inappropriate — for example, when the manual procedure has been developed for factory build-up testing — but the programmer is trying to do automatic field or depot testing of the assembled device. Often "blindly" programming the manual procedure would result in a workable automatic test, but a little computer-based imagination applied to the procedure would result in a much better and less expensive test. Even in cases where none of these comments seem at first to apply, it is only elementary discretion for the programmer to acquire copies of all the original documentation of the equipment under test—performance specifications, drawings, equipment specifications, test specifications (factory, acceptance, field . . .), performance and equipment specifications and drawings of the manual test equipment (if any), telephone numbers of the design engineers, and so on. It is important to note that performance specifications alone are totally inadequate.

Assuming for the moment that a reasonably complete manual test procedure like Fig. 2b does exist, the next step is to try to get a test procedure written in such a way that it can be programmed.

Fig. 2c illustrates what happens when an engineer who has had little contact with computers tries to write a verbal set of requirements for the programmer.

Fig. 2d illustrates some of the questions the programmer might ask in response. The questions fall into four classes: (1) those which request defined, quantifiable criteria for judgments which were not precisely defined, (2) those which ask what to do if such-and-such doesn't act the way it's supposed to, (3) those which must be answered simply because automatic equipment reaction times are often much faster than human reaction times, and (4) those which request further information on test-equipment details. They might also be categorized as (1) questions for the prime-equipment engineer, (2) questions for the test-equipment designer, and (3) questions which a non-engineer programmer might be able to settle himself, if he had sufficient documentation on the test equipment. Fig. 2d epitomizes the most difficult part of automatic-test program design. Note that some of the questions would remain unasked, to the eventual detriment of the system, if the programmer were not acquainted with some rather detailed engineering problems.

Fig. 2e shows a portion of the flowchart which might result if the programmer is trying to be very explicit, per-

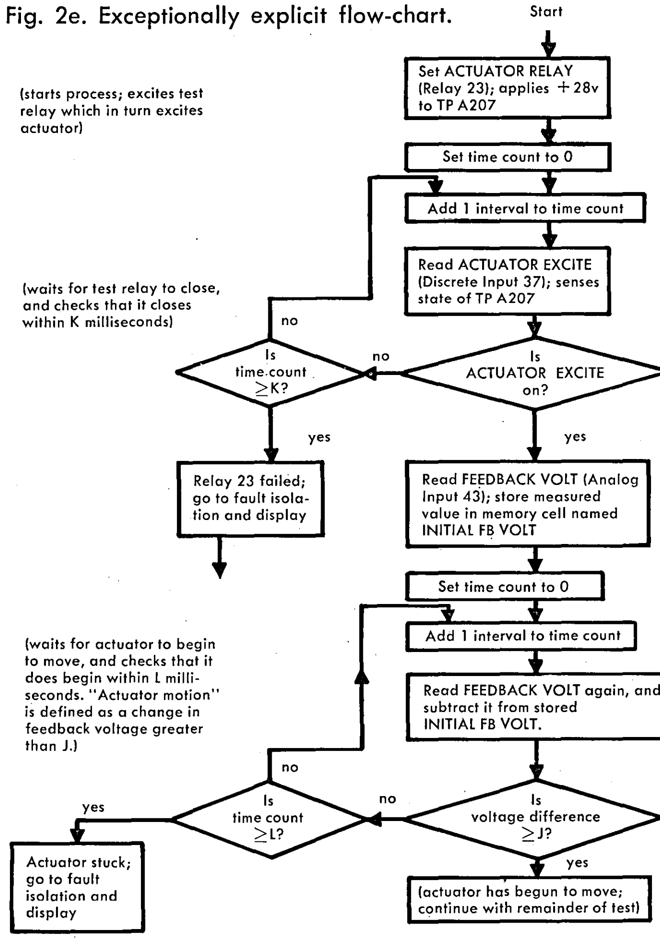
Fig. 2c. Program requirements as they might be stated by a non-computer-oriented engineer

> . . . .
> Apply +28 volts to Test Point A207.
> Observe pot feedback voltage at Test Point A203. It should increase from its initial value on a smooth curve, which eventually may become a straight line (constant velocity). (It should not stay at its initial value for a time, then break sharply away from the baseline—this indicates excessive "stiction".) The increase should terminate sharply, indicating that the actuator has hit the stop, less than 8 milliseconds after the application of voltage. The trace should have no observable "jogs" (indicating irregular frictional binding).
> . . . . .etc.

Fig. 2d. Questions which might be asked by the programmer

1. Which discrete output/relay combination in the test equipment is used to apply voltage?
2. How long does the test relay take to close? That is, how long must I wait for voltage to appear on A207 before I conclude that the test relay has failed? (Note: I must measure time from actual closure of the test relay, not from the time I tell it to close.)
3. Is a short circuit to ground on A207 dangerous? If so, how do I detect it and what do I do about it?
4. Which input lines do I use to read the (discrete) presence of voltage on A207, and to read the analog voltage on A203?
5. What are a "smooth curve" and "break sharply"? If we define a "sharp break" as a change in first time derivative (dV/dt) greater than A volts/sec occurring in less than B msec, what are A and B?
6. What is an "observable jog"? Is it a decrease in slope (decrease in dV/dt) greater than D percent, lasting longer than E msec? If so, what are D and E?
7. How long after application of voltage must I wait for the actuator to begin moving, before I conclude that it is stuck?
8. How do I make sure that the actuator has travelled all the way to its stop, instead of being held up at an intermediate position by unexpected friction? Can I tell by the final value of feedback voltage? If so, what are the upper and lower limits on final feedback voltage (as a percentage of power-supply voltage), indicating that the actuator has travelled the full distance?
9. Is there any failure discovered by this test which should cause emergency shutdown? If so, which? What is the detailed shutdown sequence?
10. What should be printed out or displayed to the operator, and what should the program do next, if
    (a) the test relay does not close
    (b) the actuator does not move (stuck in initial position)
    (c) etc. . . . .
11. .etc.

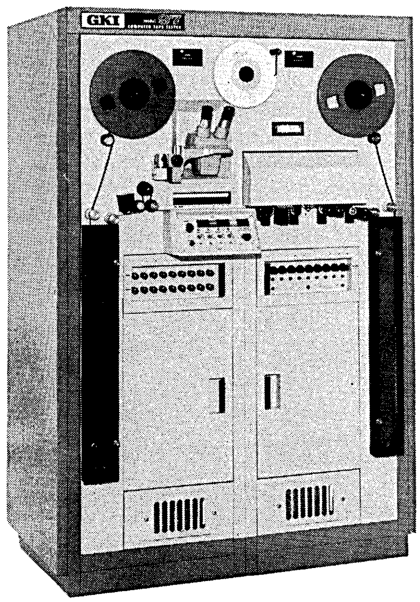
Fig. 2e. Exceptionally explicit flow-chart.



punch), and control panel switches. BENSON-LEHNER CORP., Van Nuys, Calif. For information:
CIRCLE 214 ON READER CARD

mag tape tester

Mod 97 will test nine-track tapes for variations in signal, noise, and tape width, will stop on error in both directions. It checks a potential error three times before recording, thus discriminating between transient and genuine



errors. Features: eye-level circular chart error recorder, work station with illuminator, indicator lights to show on which track an error or flaw is located. GENERAL KINETICS INC., Arlington, Va. For information:
CIRCLE 215 ON READER CARD

core memories

Coincident current systems have read/write cycle times of 1, 2, 4.8, and 10 usec, word lengths from four to 60 bits, and capacities to 16K words. Addressing can be random access, sequential non-interlaced, or sequential interlaced. Optional features include indicator lights, parity check and counters. LOCKHEED ELECTRONICS CO., MEMORY DEVICES DEPT., Los Angeles, Calif. For information:
CIRCLE 216 ON READER CARD

ocr cash register

The series 4500 prints on a paper tape numeric data in an optical font that conforms to the proposed standard of the ASA for dp equipment. The font is also compatible with the IBM 1285 optical reader. MONROE SWEDA SALES REGISTER SYSTEMS, Orange, N.J. For information:
CIRCLE 217 ON READER CARD

ruggedized mag tape

New base for tape, made of polyamide, is said to withstand temperatures to 300°F, and in reel form to 400°F without serious degradation. Applications include aerospace and interplanetary recorders, geophysical and aircraft crash recorders. Tape base reportedly does not decompose until 1,470°F. REEVES SOUNDCRAFT DIV., REEVES INDUSTRIES INC., Danbury, Conn. For information:
CIRCLE 218 ON READER CARD

cleaning cloths

Lint-free cloths measure 7 x 11 inches, come in packages of 50 and 100. ROBINS DATA DEVICES INC., Flushing, N.Y. For information:
CIRCLE 219 ON READER CARD

tape reel container

Fiberglass container, with resilient inner cushion can be used both as a shipping container and office file for mag tape reels. It is available in two-, four-, and six-reel sizes; reels can be 10½ and 14 inches in diameter with one-quarter to one-inch widths. Container colors are black, red, or olive-drab. CRATE-RITE INC., Oakland, Calif. For information:
CIRCLE 220 ON READER CARD

remote industrial printer

REMOPRINT is designed for measurement operations from which digital output is available, such as data logging and repetitive weighing. The unit accepts serial or parallel entry signals and prints 5/32-inch-high alphanumeric characters, up to 19 characters per line, at rate of one operation a second. Options: printing stock in sheets (to 8½ x 11 inches), tickets, or continuous strips with pin-feed automatic advance; automatic time and date printing and manually inserted identification data. TOLEDO SCALE CORP., Toledo, O. For information:
CIRCLE 221 ON READER CARD

all-channel display

The 9047 shows the decimal numeric value of each of 50 channels on a five-inch CRT, allows operator to observe all channel values simultaneously. Data is shown in five columns, each containing 10 channels. Front panel switch selects all-channel or single-channel operation; in latter, the numeric value is enlarged to allow viewing from a distance. SYSTEMS ENGINEERING LABORATORIES INC., Fort Lauderdale, Fla. For information:
CIRCLE 222 ON READER CARD

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CIRCLE 46 ON READER CARD

NEW LITERATURE

CONFERENCE PROCEEDINGS: 353-page book contains 29 seminars ranging from an executive forum of general interest to specialized technical sessions held at the '64 DPMA Conference. Cost: $5.75. DATA PROCESSING MANAGEMENT ASSN., Park Ridge, Ill.

PORTALOG COMPACT COMPUTERS: Twelve-page spec sheet describes modular components for assembling electronic analog simulating and controlling equipment. Portable, lab and on-line simulators for control using operational dc amplifiers may be assembled from standard components. COMPUTER DYNAMICS, INC., Torrington, Conn. For copy:
CIRCLE 130 ON READER CARD

LINEAR PROGRAMMING: Four-page booklet describes applications; what can be achieved; and steps involved in solving a problem in linear programming. MC DONNELL AUTOMATION CENTER, St. Louis, Mo. For copy:
CIRCLE 131 ON READER CARD

TAPE TRANSPORT & CONTROL PROGRAMS: Twelve-page brochure contains specifications, system diagrams, and programming information for tape transport 555 and 552. DIGITAL EQUIPMENT CORP., Maynard, Mass. For copy:
CIRCLE 132 ON READER CARD

POWER PLANT AUTOMATION: 20-page booklet describes Bailey 700 multicomputer control for automation of power plants. The unit-management concept, types of computer and functions, and the simplified activity of the operator are explained. Hardware design, showing how installation is simplified to reduce overall costs, is also included. BAILEY METER CO., Wickliffe, Ohio. For copy:
CIRCLE 133 ON READER CARD

INCREMENTAL DIGITAL TAPE RECORDER: Literature details the one-step production of computer compatible mag tapes from random data by use of incremental digital tape recorders. Includes an eight-page brochure describing three series of incremental recorders with specifications on 200- and 256-bpi packing density models, write only and read/write versions, and portable or rack-mounted configurations. PRECISION INSTRUMENT CO., Palo Alto, Calif. For copy:
CIRCLE 134 ON READER CARD

MAG TAPE: Two data sheets describe and give specifications of mag tape for RCA 301 and Univac computers. AMPEX CORP., Redwood City, Calif. For copy:
CIRCLE 135 ON READER CARD

TECH BRIEFS: Three briefs available on development growing out of space research: Computer Modification Reduces Time of Performing Iterative Division; Inexpensive, Stable Circuit Measures Heart Rate; Logic Redundancy Improves Digital System Reliability. NASA, Wash., D.C. For copy:
CIRCLE 136 ON READER CARD

DISC FILE PAPER: 24-page illustrated article, "Characteristics of the Bryant Series 4000 Disc File," features historical background and philosophy leading to the development, characteristics, application and reliability. BRYANT COMPUTER PRODUCTS, Walled Lake, Mich. For copy:
CIRCLE 137 ON READER CARD

INSTRUCTION TEXTBOOK: 32-page text provides self instruction on binary arithmetic as well as basic concepts of computer numbering systems for beginners. A plastic mat containing binary representation of six-bit alphabetic characters, decimal digits, and a listing of special characters is listed. HONEYWELL EDP, Wellesley Hills, Mass. For copy:
CIRCLE 138 ON READER CARD

INFORMATION STORAGE & RETRIEVAL: One brochure details the purpose and functions of Univ. of Pittsburgh's Knowledge Availability Systems (KAS) Center, established to conduct research on the development and evaluation of knowledge availability systems to operate new systems and to teach courses in their application. Other brochure "Space and Technology Transfer," describes availability of University's aerospace research data to local business firms. UNIV. OF PITTSBURGH, Pittsburgh, Pa. For copy:
CIRCLE 139 ON READER CARD

CIRCUITS: 120-page catalog describes transistorized digital computer circuits in three speeds (500 kc, 5 mc, and 10 mc), especially packaged for educational and industrial training as well as practical digital systems test and design work. Also included is a 64-page insert, the Laboratory Module Handbook, which may be used as a basic primer or text on digital logic and applications. DIGITAL EQUIPMENT CORP., Maynard, Mass. For copy:
CIRCLE 140 ON READER CARD

INFORMATION DIRECTORY: 356-page book, *A Directory of Information Resources in the U.S.: Physical Sciences, Biological Sciences, Engineering,* contains narrative descriptions of the subject specialization, information services, and publications of some 1,100 organizations and institutions in U.S. Professional societies, academic research groups, industrial firms, government offices, and technical libraries are included. Cost: $2.25. SUPERINTENDENT OF DOCUMENTS, GOVERNMENT PRINTING OFFICE, Wash., D.C. 20402.

BUTTON LIGHT: Data sheet describes the TIB series transistor controlled button light with replaceable incandescent lamp and integral switch. Indicator offers three basic switch options isolated from lamp circuitry — normally open, normally closed and normally open and/or normally closed circuits. Actual size drawings of the unit, terminal options, and switch forms plus mounting hole dimensions

are shown. TRANSISTOR ELECTRONICS CORP., Minneapolis, Minn. For copy:
CIRCLE 141 ON READER CARD

PRINTING CALCULATOR: Four-page brochure describes PC 1421 which prints answers in uninterrupted flow, answers up to 21 digits and 14 decimal places, marks decimal point in correct position automatically filling in zeros as needed. MONROE INTERNATIONAL, INC., Orange, N. J. For copy:
CIRCLE 142 ON READER CARD

FLOOR TILE: Laminated plastic floor tile used primarily for access floor systems, is described in four-page bulletin. Surface requires no waxing, sealing or polishing and is available in five colors. Samples included in brochure. GE CO., Coshocton, Ohio. For copy:
CIRCLE 143 ON READER CARD

AF SYSTEMS MANAGEMENT PROGRAM: Bulletin identifies the organizational levels affected by AF Systems Management which is the blueprint by which all space and military systems will be procured and managed by the DOD, lists the major areas and phases of this concept and explains where contractors may find assistance with program implementation. Distribution limited to qualified individuals. PARAGON DESIGN, San Diego, Calif.

DP FOR ELECTRICAL DISTRIBUTORS: Booklet explains computer services designed to provide more effective management control, increase sales, reduce accounts receivable, and minimize inventory. Some of the programs used to accomplish this are described. GE COMPUTER DEPARTMENT, Phoenix, Ariz. For copy:
CIRCLE 145 ON READER CARD

DIGITAL LOGIC MODULE: 36-page brochure gives specifications and logic diagrams for more than 75 modules, including flip-flops, gate expanders, AND and OR gates (with NAND and NOR capabilities), amplifiers, clock generators, crystal-controlled clock generators, inverters, Schmitt triggers, one-shot multivibrators, display drivers, and relay drivers. Modules are available in 300 kc, 1mc, and 8mc. SCIENTIFIC DATA SYSTEMS, INC., Santa Monica, Calif. For copy:
CIRCLE 146 ON READER CARD

HAND RECORDER: Four-page brochure gives specifications and details of operation of HR 303 mag tape digital recorder, developed for use in inventory control, medical accounting, utility meter reading and delivery route. ELECTRIC INFORMATION CO., Broomfield, Colo. For copy:
CIRCLE 147 ON READER CARD

DP SERVICE FOR DRUG STORES: 16-page brochure describes services retail drug stores can obtain from NCR dp centers: accounts receivable reports; "Creditax" records of customer's tax deductible purchases; departmental sales analyses; and salesperson's reports. THE NATIONAL CASH REGISTER CO., Dayton, Ohio. For copy:
CIRCLE 148 ON READER CARD

SOFTWARE: Capabilities ranging from complete software package development and computer design and evaluation to real-time systems and total scientific and business programming are highlighted in brochure. Role in aerospace projects and commercial computer systems development are also reviewed. MESA SCIENTIFIC CORP., Inglewood, Calif. For copy:
CIRCLE 149 ON READER CARD

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New Dura tape to tape code converter, 4 plugboards-$2600.00 Publishers Service Corp. 6333 Penn Ave. So. Minneapolis, Minn. 55423

IBM 7070 System for sale. 5K memory, floating point, five 729II tapes, card reader, punch, printer, tape switching ca-pability. Delivery Jan. 1966. Past usage: one shift. Reasonable price Box 4-2, DA-TAMATION, 141 E. 44th St., N.Y.C. 10017

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DATAMATION
Classified Advertising

The classified section is open for the fol-lowing advertising categories: Used equip-ment; positions wanted; help wanted, edu-cational institutions; maintenance serv-ices; professional cards; hobby products; business opportunities and educational courses. Rates are based on total number of insertions used within each con-tract year.

Minimum for all advertising—1 column inch. Exception—for Situations Wanted we will accept 1/2 inch column. See rates below. Maximum vertical space—4 col-umn inches*. Maximum horizontal 2 col-umn wide by 2 column inches deep. Larger units are billed at display rates.

Rates for advertising (classified only).

	1X	6X	12X
1 column inch ..	40.00	37.00	34.00

* 1 column inch is defined as 1 column wide by 3/4" deep.

Classified rate cannot be earned in com-bination with display advertising.
Rates for Situations Wanted—payable in advance.

For Situations Wanted only:

	1X	3X
1/2 inch column (4 lines of type)	20.00	18.00

Plus $2.00 for box number. Box number counts 1 line. Situations wanted accepted from individuals only.

Mechanical requirements:
1 column inch ....2-3/16"
1/2 inch column ....2-3/16"
3/4" (1 column width 2-3/16")
3/8" (2 column width 4-9/16")

Issuance and closing dates: Issued 15th of month. All copy must be in New York, N. Y., by 10th of preceding month. All copy subject to publisher's approval.

For further information please contact: DATAMATION Magazine, Classified Adver-tising Dept., 141 East 44th Street, New York, N. Y. 10017—212-MU 7-5180.

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CIRCLE 78 ON READER CARD

aba automation conference report

OF BANKERS AND COMPUTERS

About 800 banking people from all over the world gathered in San Francisco last month at the American Bankers Association National Automation Conference to discuss what computers were doing to banking and what banking could do with computers.

The sessions covered the usual spectrum of topics — from Savings Automation and Trust Automation through "A Realistic Look at the Automation Program" to discussion of a "National Computer System."

This last session, chaired by W. Putnam Livingston, of the Bankers Trust Co., was outstanding. First, MIT's Martin Greenberger gave a far-out look at banking of tomorrow, an effort he said he composed at the Project MAC terminal located at his residence. Greenberger thinks it highly probable that banking, 25-30 years from now, will be "a vast electronic information system of national and international scope," in which individual banks may or may not retain their identities.

He listed seven signs of a current metamorphosis which could lead to such a system, and proclaimed the hardware and technology are available for the establishment of a network of terminals at retail outlets tied into regional random access memories.

Spelling out the credit instrument of the future, Greenberger described the universal credit card—"the money key"—"an encoded plastic card that unlocks, by insertion into a simple remote terminal, the current contents of the customer's money box stored in the files of the credit exchange." Balances and credit checks could be made by the computer, and safety checks might be made by photograph or by voice identification.

Supplementing the money key might be "the money card," a small solid-state device which electronically stores dynamic balance information as well as static identification data. Pre-issued for a certain amount, its value would change with every transaction; it would serve as an electronic counterpart of travelers' checks, and would need no on-line link to a random access file.

Using time-sharing as an illustration of the rapidity with which new concepts can be implemented (and predicting that T-S will be the dominant mode of using computers in research, engineering and education by 1969), Greenberger claimed that automatic credit could move in just as swiftly, although it probably won't, because of technical and legal hurdles. But the real hurdle, he said, is inertia, and he appealed to the bankers to get moving, implying that they might otherwise lose their lead to other industries anxious to become

OF BANKERS AND COMPUTERS . . .

the dominant factor in the national credit information system of the future.

John M. Case, a consultant, pushed this last idea a step further, stating the question was not how to get to a no-paper millenium, but "How do we get there before anybody else?" Noting that banking is a system, Case proclaimed "that it had better start acting like one."

He established three needs if banking is to stay in the credit exchange driver's seat: a uniform credit practice and a code to express it; rules and guidelines to permit automatic credit processing; a communications network amongst banks.

John J. Clarke, of the Federal Reserve Bank of N.Y., took a look at some of the legal questions involved in a national system, noting its necessity to keep up with the ever-increasing mountains of checks (60-million checks are processed in this country every business day).

Discussing the problem of correct identification, he mentioned voice recognition (mentioned by another speaker at the conference as having an accuracy somewhere between fingerprinting and handwriting), warned that we must not underestimate the cleverness of the crook, but said he saw no need for new laws to handle the problems arising from mistaken credit transactions.

Raising the question of who should be the proprietor of a national computer system (he called it NATCOM), Clarke guessed that perhaps the Communications Satellite Corp. formula might be a good one—private ownership under rather close federal government control. He noted that a purely private system might run into rather "nasty" anti-trust problems. He concluded with his personal recommendation for the cooperative study of such a system by the ABA and the Federal Reserve Board.

Not all of the sessions were as good as this one. At one meeting, a communications firm representative who was supposed to discuss new communications systems put in an unabashed pitch for his company's ability to perform systems design jobs. Others gave the usual mundane advice, e.g., to form an automation committee before investigating same.

The aforementioned Mr. Livingston delivered an excellent paper on the check's future, which he summed up as "Stop moving checks," emphasizing the necessity of holding paid and canceled checks at the paying bank. Beyond that, it will be necessary, he said, to record magnetic serial numbers on all checks as they are printed, and to pick these up on magnetic tape on the first computer pass. He reviewed the results of a pilot study at his bank, where for three years 120 employees have received monthly statements without receiving checks. The results indicated little need for returning checks.

The second phase of the plan to stop moving checks—leaving them for safekeeping with the first large bank handling them—could be part of a national computer system, which "ties in closely with paying bills by telephone, transmitting checks by facsimile, and . . . no checks at all."

In his keynote address, T. J. Watson Jr. noted that he wasn't there to plug IBM, indicating that if everybody in the room bought his company's equipment, he might be in trouble with the government. He went on to stress the need for "a far more searching and rigorous analysis of the facts and problems than we yet have" in order to understand the relationships between machines and the economy.

At a luncheon talk, GE's Louis T. Rader pulled together some statistics, relating productivity (increasing on the average of 2.9% per year since 1947; 3.7% for the past two years), and between labor efficiency and investment per worker in various industries. "The four industries with the most value added per man-hour also rank at the top in investment per worker," he noted. "And the four least efficient industries in labor utilization rank lowest in investment per worker. The relation here is obvious." And, he claimed, the facts show that industries using the most labor per unit of output and with the lowest investments in plant and equipment have the lowest growth in labor demand and the lowest profits.

Meanwhile, back at the exhibition center, the manufacturers were trying to show how they could help the bankers save money (by decreasing the need for clerical help?), improve customer relations, and spend more money on equipment.

Burroughs and Honeywell had whole systems working, and GE offered an on-line demonstration of a teller's window hooked up to a 415 in Phoenix. Perhaps the biggest fuss was over the new Lundy MICR sorter, which offers slow speeds (5,000 documents per hour) at low, low prices—reportedly one-fourth of the asking price for standard high-speed units. One man representing two small banks (15,000 accounts) in Colorado said such a device would let him put a toe in the mechanization door—using the sorter and telephone lines to hook into a service bureau.

Alert to the banking industry's interest in vast national information utilities and increased customer services was Bell, with a demonstration of how someday you and I can pay our bills on a touch-tone phone, much more rapidly (ouch) than ever before, and without using post-dated checks. It's interesting to note that the term "kiting" was not once heard at the conference.

At another booth, Dun & Bradstreet won the award for the acronym which best reflects a company's name with their DUNS (Dun's Universal Numbering System), a fat volume in which 300,000 manufacturers and 25,000 non-manufacturing firms worth more than $500K (together they account for 90% of the flow of business documents, according to D&B), are assigned seven-digit numbers (six digits plus check). A presumed leading zero will permit expansion later. Already, some leading firms are requesting their vendors to include their DUNS number on their invoices.

And a small (13-man) company in Racine, Wisconsin named MEDAC was there to offer its medical billing program package to banks not in areas already sealed off by franchise restrictions (United California Bank is using it out here).

It was an interesting conference, especially to a non-banking computer-oriented observer. But it was no place for digit haters. Already banking is pursuing with other industries, and through ASA, a thing called CUSIP (Committee on Uniform Security Identification Procedures), which will permit each of some 115-120,000 stocks and security issues to have their own private number. The banks are also interested in establishing a national customer identification numbering system. Then there's the universal credit card with its numbering problems. Eventually, every newborn babe may have a social security number tatooed in some appropriate part of its body.

The conference made one thing clear: banks, although they are often confused and naive about computers and their proper use (as one computerite noted, they tend to confuse automation and mechanization), are planning for these mysterious beasts some applications and systems which will have profound effects upon their own industry, upon how the economy manages its money and its credit . . . and upon the man in the street.

—ROBERT B. FOREST

Continued from page 22

Leased machinery is stickier since would-be users have to part with agency funds to acquire it, or it's just shipped back to the manufacturer. Still, there are a goodly number of buyers for marked-down leased equipment in the "excess" class.

"I could get rid of any number of 7094's if I had 'em," said the official. "With the recent price cuts, they've become a hot item in the government hand-me-down market."

The department lets government dp people know what's available by means of a circular prepared monthly (current distribution: about 500) listing all "excess" equipment. Requests are honored on a first-come, first-served basis.

"We've got people standing in line for 650's, incredible as that may sound. A listing of a 1401 on a recent circular produced more than 20 requests. Of course, most of these responses come from agencies which have a marginal use in mind for the equipment and couldn't justify its acquisition except at very low cost."

Also, much department business is generated by its breaking down, or "cannibalization," of computing systems. Tape drives, card punches, printers, etc., are quickly snapped up; so are the smaller accessories. "We had 9,000 tape cans come in here one day, and they were gone three days later." What happens to government-owned equipment that isn't claimed by any agency? It's declared surplus and usually donated to some educational institute but, says the department, that has happened only rarely up to now.

WARM-BODY CONTRACTORS ESCAPE CSC SWATHE

The recent decision by the Civil Service Commission to restrict use by government agencies of contractor employees is not expected to have substantial impact on the large number of service companies providing programmers and other dp personnel to the government. "The decision is aimed primarily at those agencies which utilize contractor personnel as a means of getting around restrictions on the number of people they can hire directly," noted a staff official on the House Manpower Committee studying the situation.

EDP practitioners are most often obtained from outside companies for legitimate one-shot jobs or because their skills are just not available in the government ranks. Also, computer service contract employees are usually not supervised by federal workers in their daily work, nor are they hired and fired by a government boss — the two principal symptoms of circumvention cited by the Commission in its decision.

"WHERE IS SOFTWARE?" COPYRIGHT OFFICE ASKS

The Copyright Office continues a-sitting and a-rocking, waiting for the response on its offer to copyright computer programs to materialize. The total of copyrighted programs remains at three, the same as a year ago. (This despite the existence of at least one commercial venture in this field). "We've held preliminary discussions with several companies on possible copyrighting of their programs," said a CO official, "but nothing definite ever resulted." The office is a mite put out at this turn of events since it anticipated at least a modest number of applicants.

people IN DATAMATION

■ Monson H. Hayes, formerly vp and gm of the Electronics Div. of Whittaker Corp., has been named president of Consolidated Systems Corp., a subsidiary of Scientific Data Systems.

■ Robert S. Barton, most recently with Control Data in Australia, has joined GE's Computer Dept.

■ Arnold B. Shafritz has been elected vp of Auerbach Corp., Philadelphia, Pa. He is also director of the Information Sciences Div.

■ Three executive changes have taken place at IBM: Dr. Thomas R. Horton has been named vp systems, Systems Development Div.; John M. Norton succeeds him as gm of Advanced Systems Development Div., Armonk, N.Y.; and, Louis D. Stevens has been promoted to manager of the Las Gatos Lab., Las Gatos, Calif.

■ Dr. Donald Drukey has been named manager of the Research and Technology Div., and Guy Dobbs has been appointed manager of newly-formed computer center of System Development Corp., Santa Monica, Calif.

■ C. Gordon Murphy has been appointed president of the Data Systems division of Litton Industries, Canoga Park, Calif. He succeeds John J. Connolly, who was advanced to vp in charge of the Components Group.

■ Daniel Sinnott has been named manager of the Digital Computer Group, Electronic Associates, Inc., West Long Branch, N.J.

■ C. William Tarman has been elected president of, and a director of Meiscon Corp., Chicago-based subsidiary of Control Data Corp. He succeeds James D. Harris, who will remain on the board of directors.

■ Elroy S. Slawinski has been appointed manager of systems and dp department of Allis-Chalmers, Milwaukee, Wis. He was formerly with Bucyrus-Erie.

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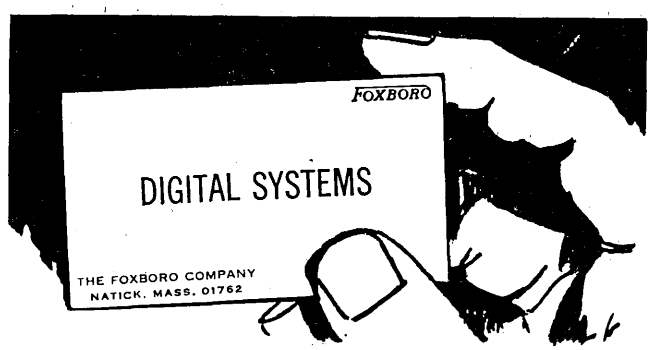

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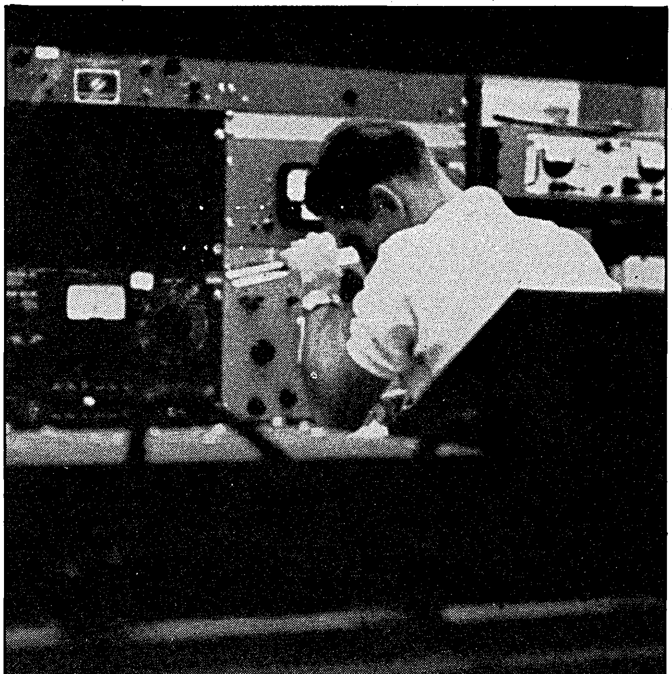

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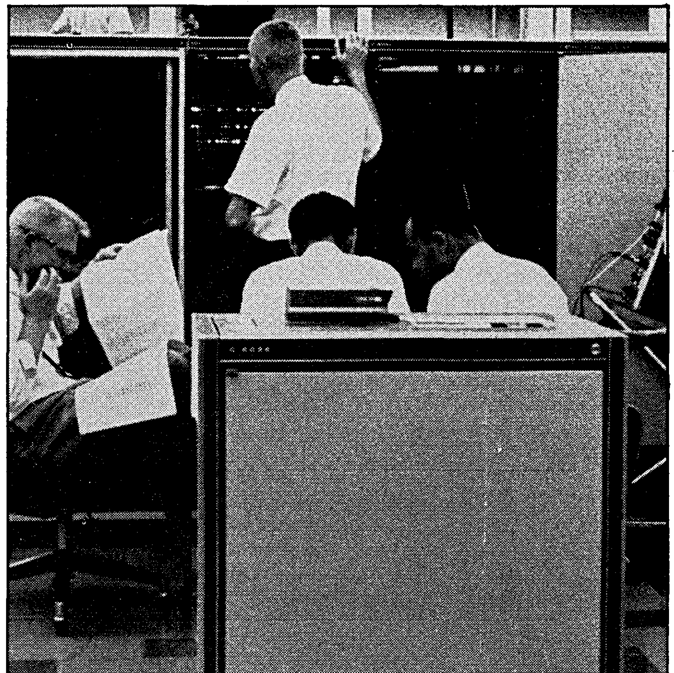

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Photo By David Stemple, Analyst, CUC

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