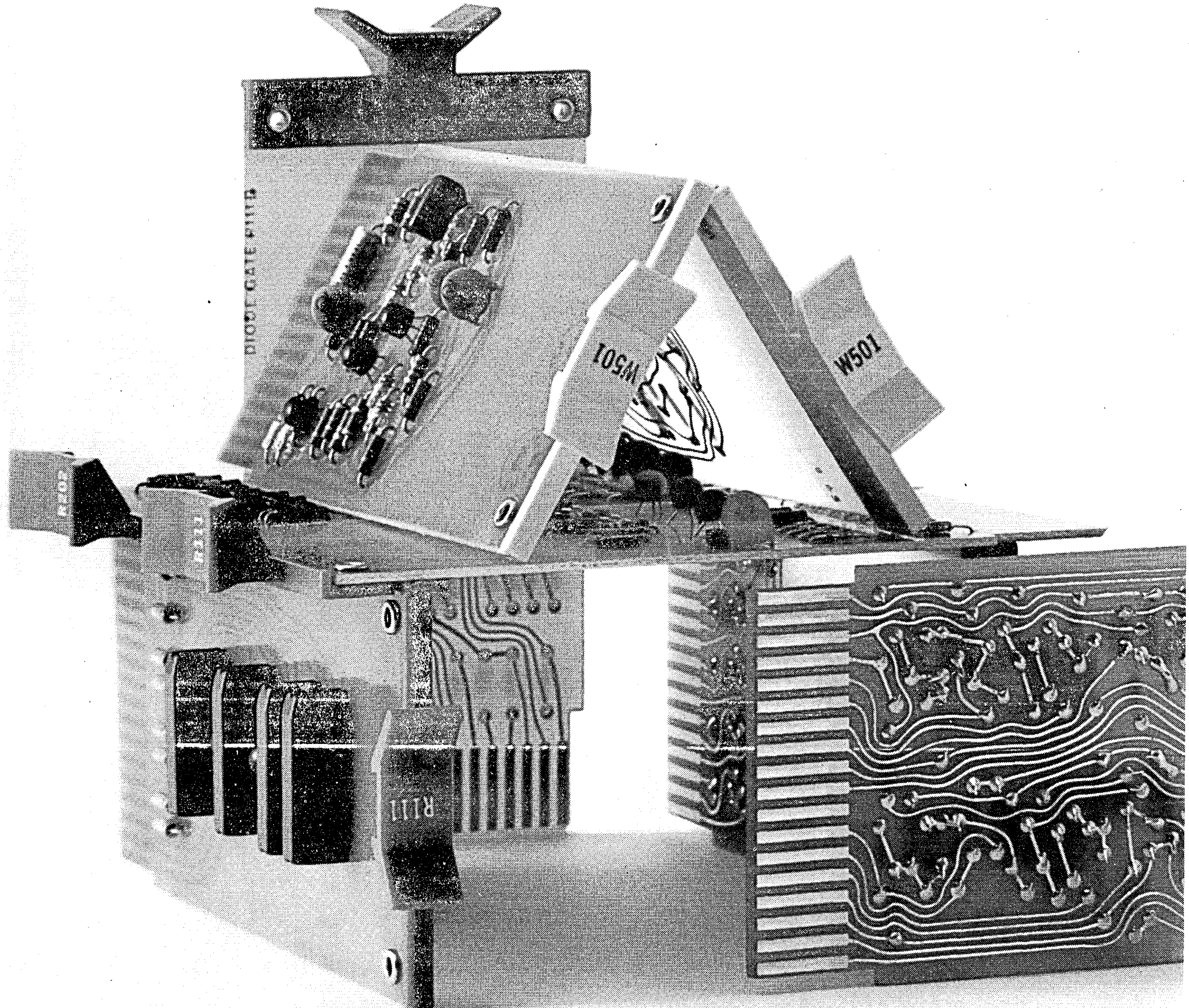
DATAMATION

66

April

ALARUMS & EXCURSIONS . . . the SJCC takes BOSTON



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We will be very surprised if the rest of the industry catches up with our new computer system in the next 5 years.

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It does time sharing in a real-time environment.

It is a totally integrated hardware and software package.

It was designed first of all to handle the heaviest demands of priority-interrupt processing—easily, simply, naturally.

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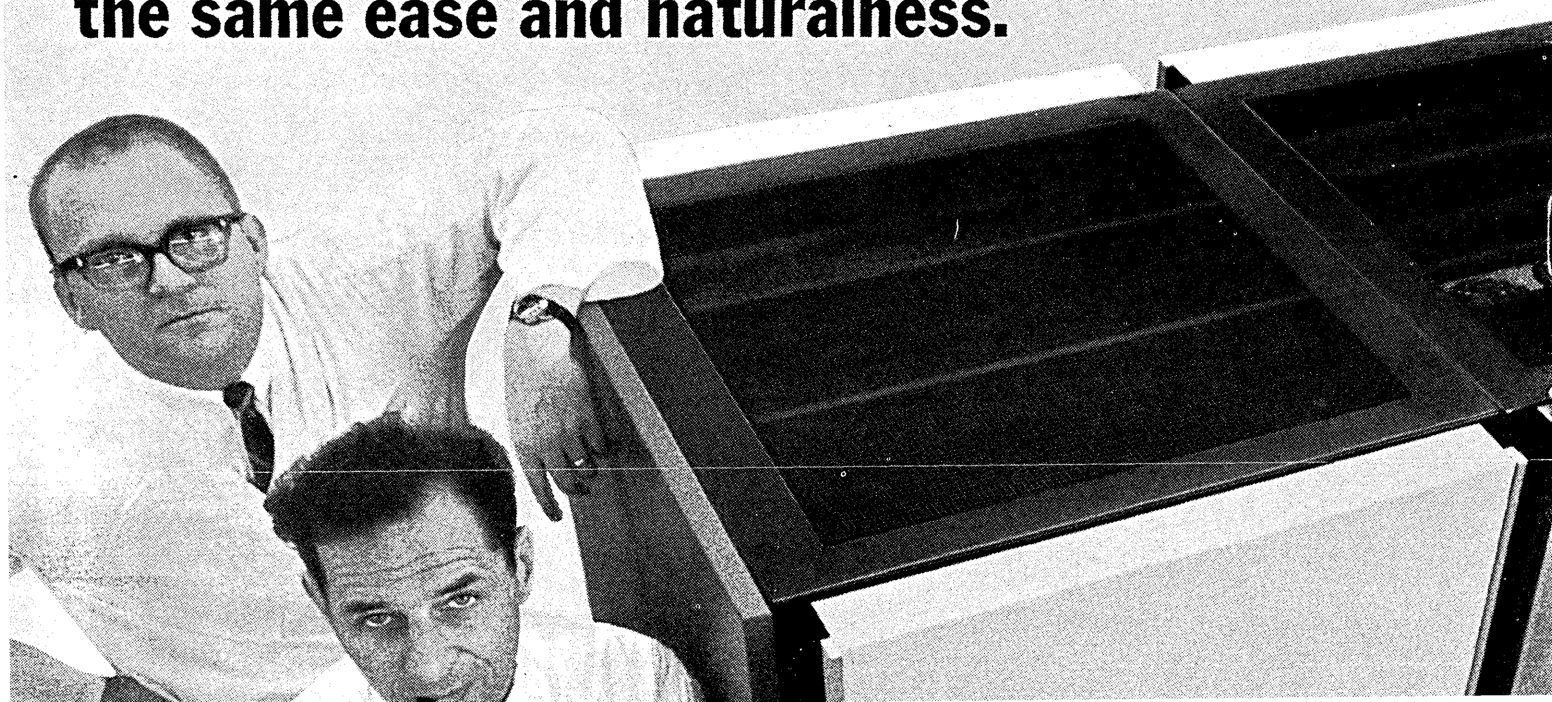

It can completely change its environment from one PL/I program to another in 6 microseconds, under the control of an operating system.

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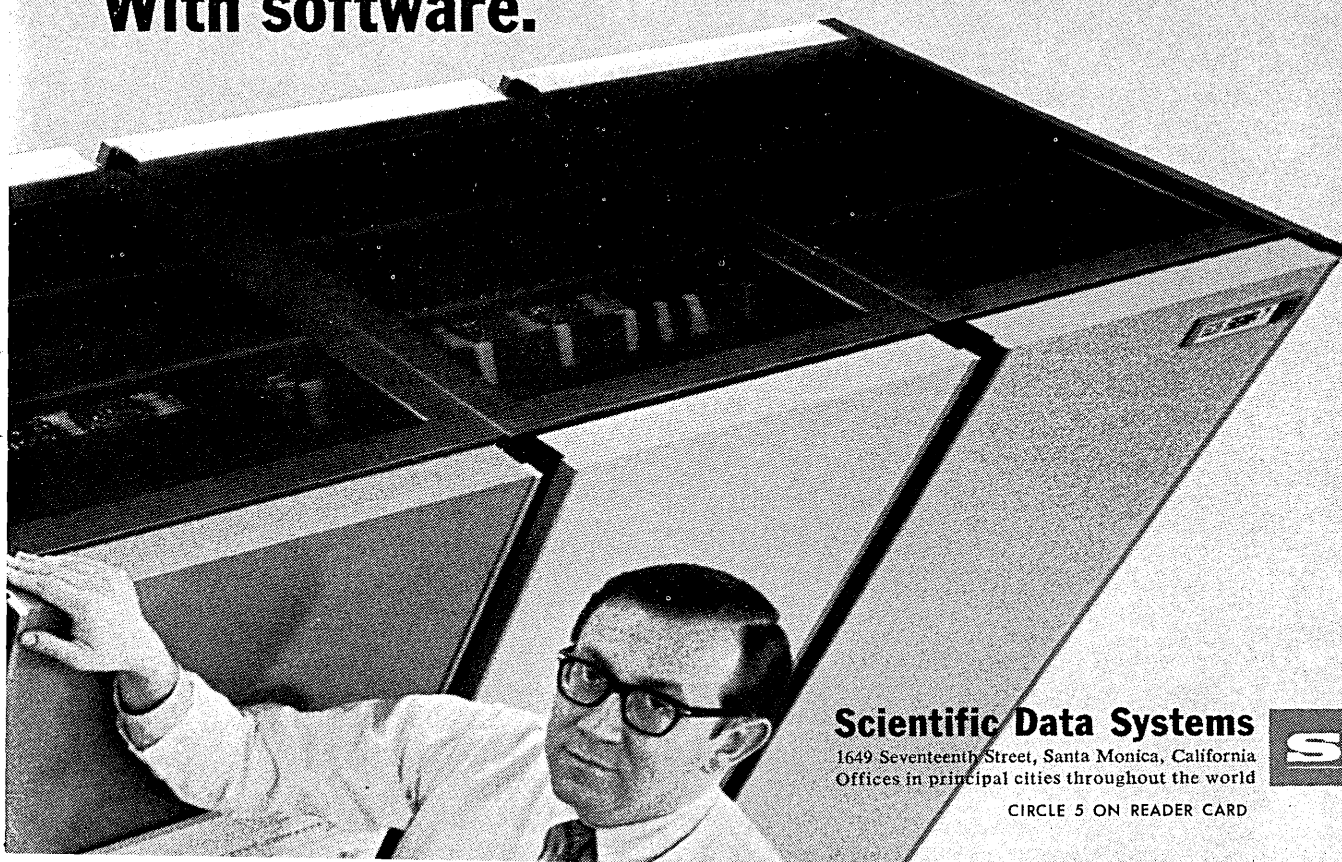

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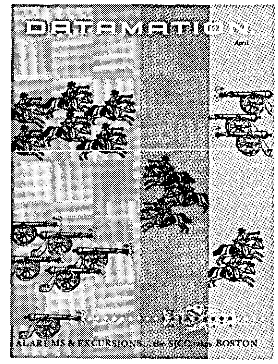
volume 12 number 4



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1830 WEST OLYMPIC BLVD.
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This issue 63,052 copies

Raytheon's 520 is a real-time computer system with a 1 microsecond main memory.

Its new FORTRAN IV is compatible with IBM's 7094 and 360.

Raytheon Computer's FORTRAN IV is language compatible with FORTRAN IV (version 13) used with IBM's 7094 and is a sub-set of the FORTRAN IV designed for System/360 machines. This compatibility in an efficient *one-pass* processor is available only with Raytheon Computer's 520.

With Raytheon's FORTRAN IV you can exchange programs between the 520 and the 7094 and you can debug many 7094/360 programs on a 520 when either of the other machines is not available. Debugging is done faster if the 520 is equipped with its optional 1 microsecond memory and at lower cost, since the 520 runs about 1/20 the cost of the 7094 on an hourly basis. Equipment requirements are minimized too, since Raytheon FORTRAN IV runs on a 520 with an 8K memory.

FORTRAN IV is the third major FORTRAN package Raytheon has made available to 520 users and is a separate and distinct processor from the other two—FORTRAN II and Real-Time FORTRAN IV. This eliminates the overhead processing penalties usually associated with multi-purpose FORTRAN processors. Raytheon FORTRAN IV and Real-Time FORTRAN IV include all the features of the ASA standard.

Raytheon's FORTRAN IV enables real-time and hybrid installations to use the 520 for data reduction and hybrid support programs which otherwise have to be run on a 7094.

The majority of FORTRAN programmers are familiar with this language; those who do require training will be spending their time and your money learning a language that is the most widely used in the industry. Documentation effort and expense are also reduced.

The Raytheon 520, with your choice of either a 2 microsecond or 1 microsecond main memory, and input/output features like keyboard/CRT display station, disc pack and drum memory, direct memory access and improved analog interface units, is currently being specified for hybrid and real-time systems in the $100,000 to $300,000 price range. Your first step is to read the literature. Write today for Data File C-131.

RAYTHEON

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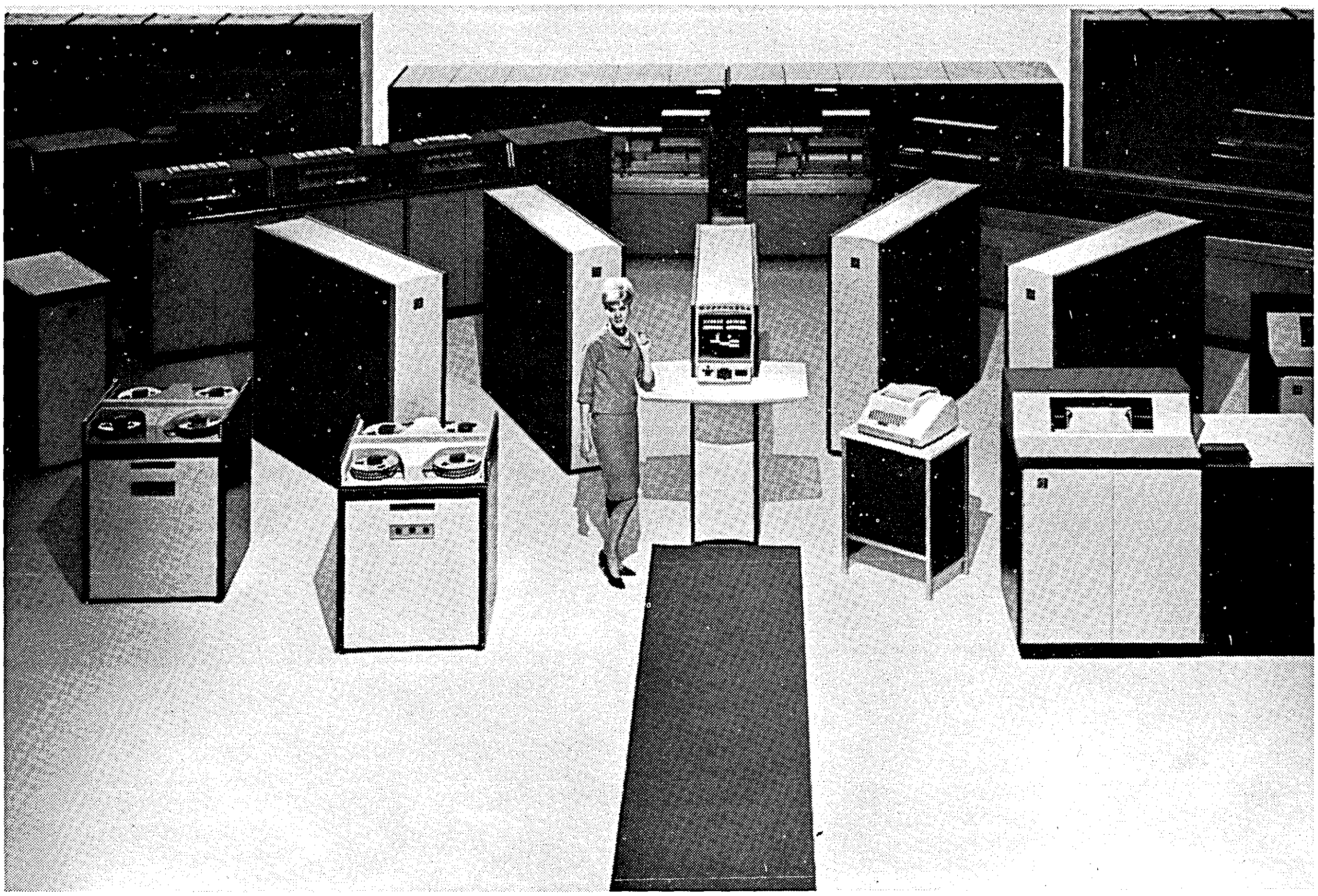
DATAMATION®

april
1966
volume 12 number 4

datamation departments

automatic information processing for business industry & science

Introducing two new Burroughs 500 Systems: B 2500 and B 3500



They're built to respond to your needs instead of making you respond to theirs

These two new *user-oriented* computers are the latest Burroughs 500 Systems to be built by *teams* of hardware and software experts.

Burroughs started this new trend in 1960 with the B 5000, which established the value of integrated hardware/software design. That system's more powerful successor, the B 5500, is still unmatched by the new competitive systems that are modeled after it.

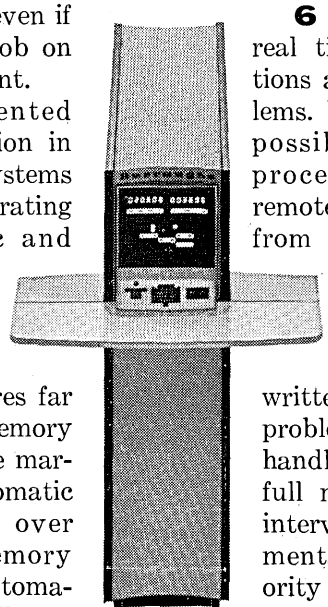
The other Burroughs 500 System, the B 8500, is the most powerful computer system yet designed.

Now, this new level of computer responsiveness to business and scientific problems is available to even the smallest organization with a requirement for electronic data processing.

Here are just a few of the impressive characteristics of the new Burroughs B 2500 and B 3500:

1 Extremely fast hardware speeds, with multimillion digit-per-second data transfers and control memories that operate in billionths of a second.

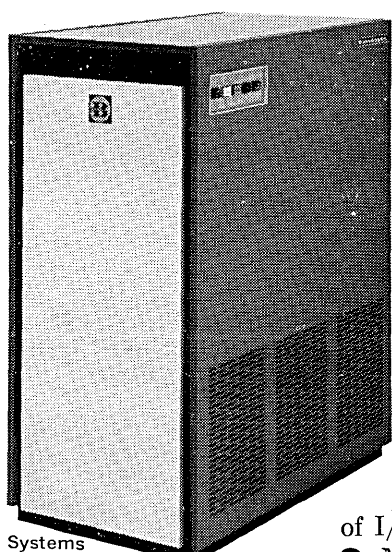
2 The ability to do many unrelated jobs at once (multiprocessing)—and to continue doing them without interruption even if you drop in a rush job on the spur of the moment.



Central Processor

3 An unprecedented degree of self-regulation in low-cost computer systems via a choice of two operating systems: the Basic and Master Control Programs. The Master Control Program, for example, not only does more, but requires far less resident core memory than any other on the market. It provides automatic scheduling, control over multiprocessing, memory and I/O allocation, automatic maintenance of a library of programs and data, program selection and initiation, error correction functions, interrupt handling, maintenance of the system log, and much more.

4 Programing that's so simple it can be started by one programmer and continued by another—or divided up and then integrated by the operating system. Since the housekeeping details are taken over by the operating system, the programmer is free to concentrate on the problem, not on the machine.



Systems Memory

5 Higher level programing languages (COBOL and Fortran) which save time and money. They improve supervision by facilitating review and control of programs and by demanding standardized documentation. They improve communication by removing the "machine language curtain" between those who understand the problem and those who understand the computer.

6 A special suitability to real time, data communications and time sharing problems. With the B 3500, it is possible, for example, to process order-entry from remote locations *and* compile from remote locations *and* execute major production runs at the computer site—all at once. Yet every program is written solely to solve the problem it was assigned to handle. Automatic interrupt, full memory protection, an interval timer, program segmentation, automatic priority scheduling and other features combine to provide quick response to a wide variety of simultaneous demands, with no interference between jobs.

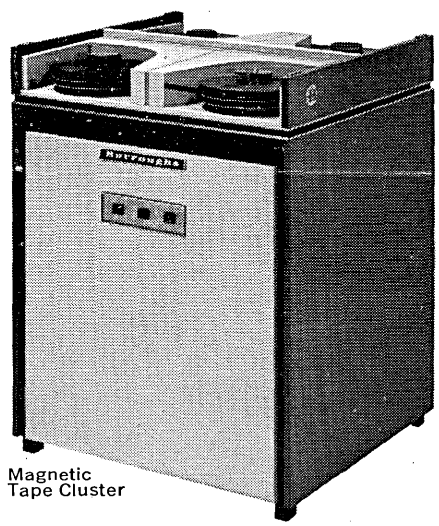
7 The ability to accommodate the fastest random access disk file on the market. Operating speed of this already fast device may now be multiplied by simultaneous use through up to four I/O Channels.

8 From 4 to 20 I/O channels (all of which may be active simultaneously and still leave ample time free for computation) plus multiplexors and exchanges that allow great flexibility and simultaneity of I/O operations.

9 Monolithic integrated circuit design which produces greater speed and reliability and reduces size and costs. The B 2500 and B 3500 make use of two proven concepts in the very forefront of this development: complementary transistor logic and array monolithics.

10 Emulators which make it simple and quick to convert from our B 200/B 300 systems or from 1401, 1440, or 1460 systems. These conversion aids make your old programs immediately usable on the faster, more powerful B 2500 and B 3500.

11 A *responsiveness* to change in all aspects of computer use—from a change in the number of peripheral units to a change in program priorities. From a switch of card to tape or from random access to real time. And under MCP control, when you add new components,



Magnetic Tape Cluster

more memory, more I/O capacity, or upgrade from a B 2500 to a B 3500—anything short of changing the basic method of processing data—*absolutely no reprograming is necessary.* Change on these systems is economical, quick, and orderly.

The B 2500 and B 3500 share in one other important characteristic. They are both products of Burroughs acknowledged excellence in electronic data processing.

Burroughs Corporation

Detroit, Michigan 48232

CIRCLE 9 ON READER CARD

calendar

● Systems and Procedures Assoc. is sponsoring a Southwest Systems Conference April 20, at the Townehouse, Phoenix, Ariz.

● Course on the top management control of edp, sponsored by Automation Training Center, will be held at the Americana Hotel, New York, N.Y., April 21-22. Fee: $175.

● Symposium on computer-aided basic research will meet April 22 at the Steven's Institute, Hoboken, N. J.

● Society of Photo-Optical Instrumentation Engineers is sponsoring a seminar on "The Human in the Photo-Optical System," April 25-26, Sheraton-Tenney Inn, New York, N. Y.

● Meeting of the American Society of Mechanical Engineers on the theme "Computers and Instrumentation" will be April 25-27, Charleston, W.Va.

● Workshop seminar on data management will be held April 25-27, Sheraton Palace Hotel, San Francisco, Calif. Sponsor is American Management Assn.

● RCA Institutes' School of Custom Educational Programs will sponsor two seminars: "Digital Systems Engineering," April 25-29, Los Angeles; and "Digital Electronics," April 25-29, Washington D.C.

● Meeting of the SDS Users' Group will be held April 28-30, Sheraton Boston Hotel, Boston, Mass.

● Telecommunications exposition to be held in conjunction with meeting of Industrial Communications Association will be May 2-5, Queen Elizabeth Hotel, Montreal, Canada.

● Computer Usage Education Inc., will sponsor three seminars: "Time-Sharing," May 3-5, Sheraton-Chicago Hotel, Chicago; "Information Retrieval: Today and Tomorrow," May 10-12, International Hotel, Los Angeles; "The Reprogramming Problem," May 24-26, Twin Bridges Marriott Motor Hotel, Washington, D.C. Fee: $195.

● Honeywell 400/1400 Users Association will meet May 4-6, King Edward Sheraton Hotel, Toronto, Canada.

● National telemetering conference will be May 10-12, Prudential Center, Boston, Mass.

● National colloquium on information retrieval is scheduled for May 12-13, Univ. of Pennsylvania, Philadelphia, Pa.

● Meeting of the Canadian Operational Research Society will be May 12-13, McGill Univ., Montreal, Canada.

● SHARE Design Automation Committee Workshop will meet at the Jung Hotel in New Orleans, May 16-18.

● Course in SIMSCRIPT will be given May 16-20, Southern Simulation Service, Tampa, Fla.

● Seminar on "Management for Numerical Control" is scheduled for May 18, IIT Research Institute, Chicago, Ill.

● Technical symposium on "Developments in Multiprogramming and Multiprocessing," sponsored by the San Diego Council of Data Processing Societies, will be held May 20, San Diego Community Concourse.

● GUIDE International Users Organization will meet at the Queen Elizabeth Hotel in Montreal, Canada, May 24-27.

● Joint spring conference of the Univac Users' Association and the Univac Scientific Exchange will meet May 25-27, Royal York Hotel, Toronto, Canada.

● American Bankers Assn. national automation conference will meet June 6-8, Palmer House, Chicago, Ill.

● Conference on "Advances in Computing" will meet June 10 at the State Univ. of New York at Stony Brook, N.Y. Sponsors are the Long Island chapter of the ACM, and the Computing Center at State Univ. of N.Y.

letters

priorities & costing

Sir:

In "Controlling Computer Operations" (Feb., p. 53), R. S. Haas posed a question about better ways to allocate machine time than by "signature" authority. The local laundry is a simple example of this way in that priority jobs are priced higher. Modern economics proves the virtue of such action for the most efficient allocation of fixed supply products. One direct result of such a course would be to confront the customer with the very proper question: "How important is this job to the person who is most capable of judging its importance, namely me?"

William Hurdlow
Livermore, California

The author replies: "Yes, I agree with his recommendation and see no reason why it can't be implemented in a production shop."

process control software

Sir:

I concur with the author's statements ("Process Control Software," by James D. Schoeffler, Feb., p. 33) that existing languages simply do not adequately fit all the needs of contemporary process control programming. However, in the area of scanning and logging, both common functions of all computer control systems, there is a very adequate and widely-known language which can be used to generate flexible, versatile, and surprisingly efficient programs. I refer to the everyday English spoken by all engineers.

The reality of this can be attested to by the fact that we are presently implementing a system that allows an engineer to "write" these programs by simply filling out a form in the language he commonly uses. It might be of interest to note that the word "standard" does not precede the word "form" in the previous sentence.

I must also take exception to the redundancy of having an off-line monitor as well as an on-line monitor. This is perhaps the basis for the implication in the article that monitors, by their very nature, require enormous quantities of memory when, in fact, a monitor which performs the total executive, interrupt, and I/O control functions for all on-line and time-shared programs can be (and has been) written in less than 1500 words.

Meanwhile who is going to specify RTL (Real-Time Language) and when?

D. G. PISTOLE
Programming Services, Inc.
Tarzana, California

The author replies: "I am very happy that Mr. Pistole agrees that existing languages are not adequately flexible to fulfill the needs of the entire process control industry. His English-language scanning and logging generating program is a good example of what I termed Process Oriented Languages, special purpose languages directed toward the user. Such programs could be produced very economically if a higher level language were available.

"There is a real need for an off-line monitor in the following sense: the off-line monitor is actually a part of the total operating system and operates when there is free time available (that is, time not required by the process). This permits compilation and debugging at the process site without taking the computer off-line, a very useful feature. Mr. Pistole is quite correct in his statement that the monitor itself is not necessarily large.

"A start at specifying RTL has been made at the Systems Research Center, Cleveland, Ohio. This is a cooperative research program sponsored by approximately 12 suppliers and users in the process control industry, including the major computer suppliers."

perpetual calendars

Sir:

Mr. Opler ought to reprogram his UTSS ("Bon Voyage—1984 Style," Jan., p. 24). Barring calendar reform or thermonuclear disaster, July 7, 1984 will be on Saturday, not Monday.

W. M. JACOBS
New York, N. Y.

Datamation welcomes your correspondence concerning articles or items appearing in this magazine. Letters should be double spaced . . . and the briefer the better. We reserve the right to edit letters submitted to us.

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For special applications, ASI has designed the *ADVANCE* 6070 incorporating an auxiliary arithmetic unit capability. The modular concept of the *ADVANCE* Series has been designed to save you time and money. Let us give you more facts. Write or call: ASI Computer Division—EMR—8001 Bloomington Freeway, Minneapolis, Minn. 55420. Phone: 612-888-9581.

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look ahead

MANUFACTURERS COME ALIVE

Charles Adams, who keeps track of such things,notes that no new computers were introduced during the first quarter of '66. Thus no Adams Characteristics in this month's issue. As if to make up for this dearth, March saw two major announcements by SDS and Burroughs (see p. 75). We understand that the Burroughs announcement is only the beginning, folks. Look soon for the 6500; other "500's" will be announced later. Sigma, too, will expand.

ASI makes its move soon with a new member of a new family (see below), and Univac can be expected to remove the veils in June, when it will probably announce a "New Family Line" ranging from small- to medium-scale. A second NFL, medium- to large-scale, incompatible with the first one, will come out later. There are one or two new firms ready to jump into the game ... NCR will have to do something this year, and GE will soon upgrade its 400 family. Let's see ... who does that leave?

IF SDS IS SPRINGING, CAN ASI BE FAR BEHIND?

Following up its family of four 24-bit computers, ASI computer department of Electro-Mechanical Research is switching to the "compacts"— a series of 16-bit (plus parity and protect bits) machines. First to be announced will be the $28K Advance 6130, a totally monolithic i.c. model with cycle times of 0.9 or 1.8 usec; faster memories will be offered as available.

Features will include 4-32K core, three index registers, dual indexing, hardware multiply and divide, multilevel indirect addressing and priority interrupts, hardware memory protection, single and double word-length instructions, and up to six 6- and 8-bit (2 MC) I/O channels. Optional features: direct memory access, real-time clock. Numbering is two's complement. Software will include a basic Fortran, operating and monitoring systems.

1700 COMES ON STRONG, 6800 DISAPPEARS

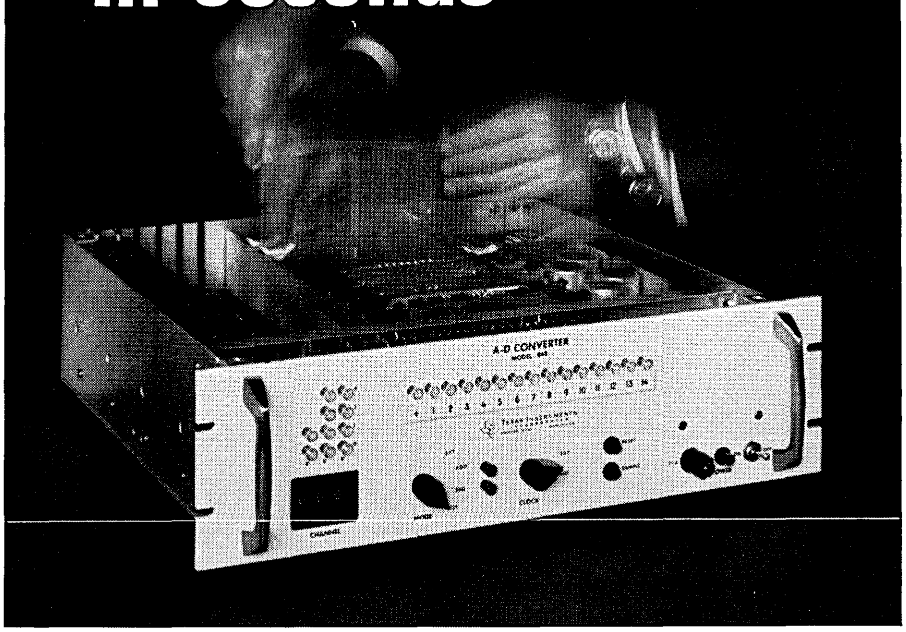
A shot in the arm for Control Data, lurching recently, is an order for 50 1700's from Motorola's Semiconductor division in Phoenix. (Price of a basic 4K 1700: $30K.) On one line, the machines will test transistors, look at costs, orders, then route appropriate numbers of units to customer bins. Other 1700's will be used for quality tests of integrated circuits. Now using 8090's, the company will start switching to 1700's in June, when the new machines start coming in at the rate of two per month. One source says that CDC plans to sell a thousand 1700's over the next two years.

Meanwhile, CDC has decided to pull a curtain of secrecy over its 6800, which is now considered company private. Salesmen are admonished not to quote prices. But there will be a follow-on to the 6600. Deliveries will start in the first quarter of '68.

TAPE CLINIC

A new outfit in Los Angeles called Certron is heading for nationwide marketing of its mag tape rejuvenation and recertifying service. Headed by Ed Gamson, former Ampex vp, the company looks at their business as preventive maintenance — signing up big users for

change converter function, add multiplexing in seconds



...with high accuracy, at high conversion speeds.

You get the flexibility of modular construction, together with outstanding electrical specifications in the Model 848 A-D Converter! Modular construction allows quick, easy, functional conversion changes and the addition of up to 96 single-ended channels of multiplexing (48 differential channels). Specifications include a true 0.01% accuracy (±½ lsb), including built-in sample and hold, and throughput greater than 30,000 conversions per second, including multiplexing. The 848 Converter is a 15-bit binary instrument which uses integrated circuit logic throughout, giving you a reliable instrument in a compact (5¼″ high) package. Logic levels are 4 to 10 volts, output is single or double rail, with four code options: sign and absolute value; offset binary; two's complement; and one's complement.

INDUSTRIAL PRODUCTS GROUP

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periodic tape cleaning and repair. Gamson sees an inviting market — about 1½ million reels of computer tape sold last year and that much again in instrumentation tape — and claims that about 80% of the tape thrown in the corner because it won't work anymore can be brought back to life. They've already convinced much of the local aerospace industry and a few dozen other big installations that the plan is a money saver.

TRANSPACIFIC PROGRAMMING

Hoping to take advantage of more reasonably priced Japanese programming talent, International Computing Services has set up shop in Tokyo, is offering its services to U.S. firms. Headed by Joe Berston, edp pro with six years experience in Japan, the company has a good head start with contracts to develop a banking package for a major American manufacturer, is also translating a 1401 program for the Univac III for a Detroit clothing chain.

LITTON FINDS MARKETS FOR SPECIAL-PURPOSE MACHINES

Amid monthly announcements of gp computers, a "systems house" is quietly designing special-purpose machines for specific systems, and developing for itself a whopper of a market. The application, automatic revenue control, cuts horizontally across the entertainment, distribution, and transportation industries — in short, wherever crowds of people with money or tickets in hand must be accommodated.

For those interested in getting into the game, the ante is high, and most $ must come from in-house. But Litton Industries' Advanced Data Systems Div. is leading the way. Installing an automatic fare-collection system for Illinois Central Railroad and the London Transport system, the ADS is also making a study and developing prototype equipment for the San Francisco Bay Area Rapid Transit District.

The systems include machines to make change, vend, collect, and cancel rides on tickets (some with oxide backing to record rides remaining), and the latest in turnstile design. Change the backdrop but not the props, and you can see this working in parking lots, theatres, and sports arenas — moving people, counting cash, and developing traffic studies simultaneously. And not a nickel is stolen.

RUMORS AND RAW RANDOM DATA

Briskly marketing its 60 megabit, 20-msec access disc, Burroughs expects to have 700 installed by the end of '66. TWA and U.S. Steel have placed orders for 200 102-million-bit, 30 msec access units; USS will have 150 units (that's over 15-billion bits worth) on line. ... Meanwhile, we understand that Bryant has decided to stay out of the removable disc pack business, despite some fairly hefty order temptations. ... We hear that Tektronix, leading scope maker, will enter the display biz. ... Decimal Ascii for punched cards, now being voted on as a proposed standard, will probably fail to achieve X.3 "consensus." If an IBM-led assault succeeds, extended bcd -- as a de facto standard -- will be the likely winner. ... Conversion aids developed by customers may be offered 1108 users by Univac. One is a Lockheed-developed "decompiler" which converts 7094 machine language to Neliac for input to the 1108. Another, from Boeing, translates 7080 Autocoder programs into 1108 language. ... Bob Bemer, who has been coordinating GE software out of Paris, is now stationed at Phoenix. ... Persistent rumbles indicate that Fred Lang, founder and former president of Aries, will form a new software firm. He'll try to attract top-flight people with juicy stock options. HQ will be in Minneapolis.

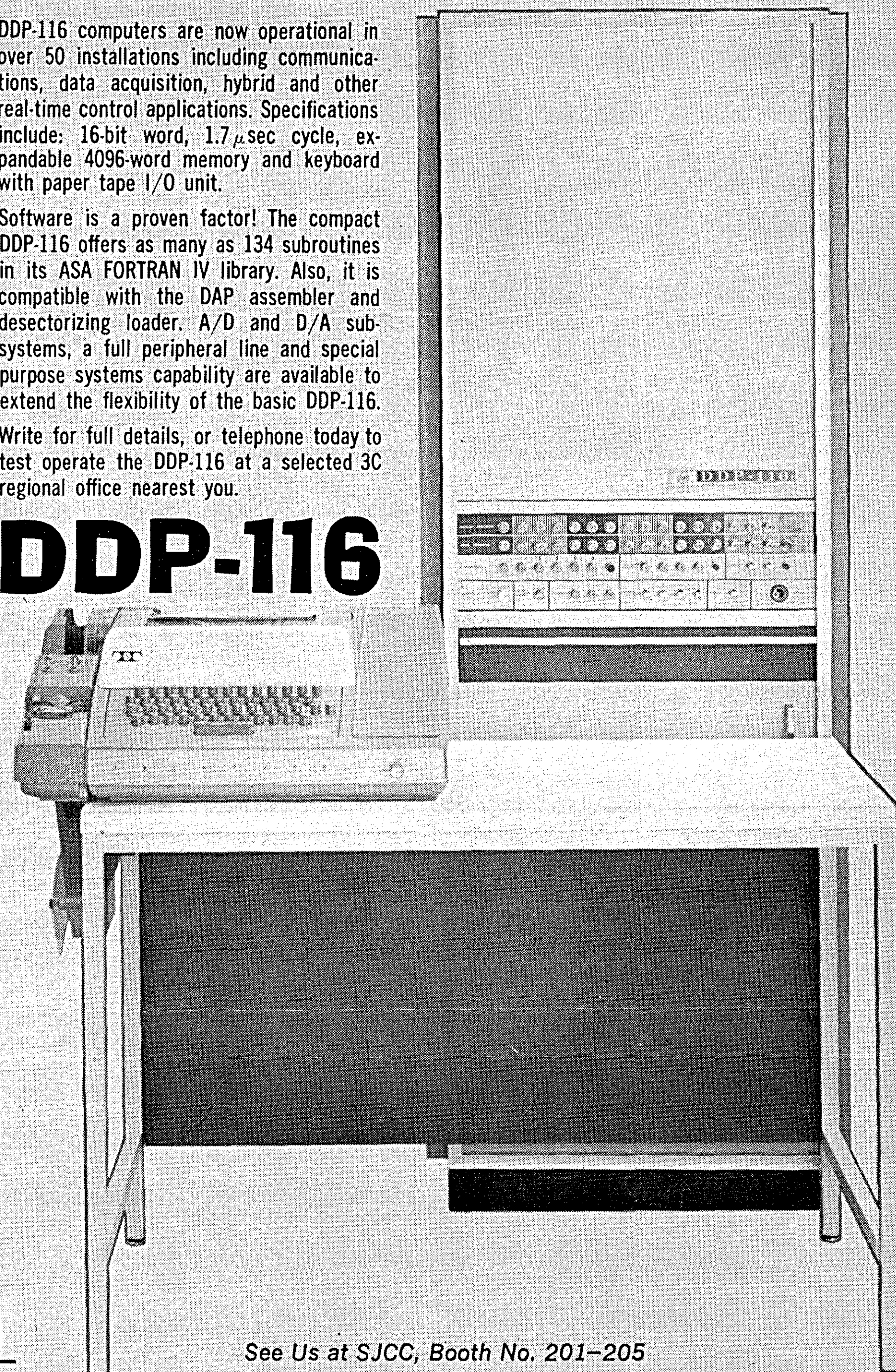
ONLY 3C OFFERS 30 DAY DELIVERY ON THE HOTTEST COMPUTER IN THE $28,500 PRICE RANGE

DDP-116 computers are now operational in over 50 installations including communications, data acquisition, hybrid and other real-time control applications. Specifications include: 16-bit word, 1.7μsec cycle, expandable 4096-word memory and keyboard with paper tape I/O unit.

Software is a proven factor! The compact DDP-116 offers as many as 134 subroutines in its ASA FORTRAN IV library. Also, it is compatible with the DAP assembler and desectorizing loader. A/D and D/A subsystems, a full peripheral line and special purpose systems capability are available to extend the flexibility of the basic DDP-116.

Write for full details, or telephone today to test operate the DDP-116 at a selected 3C regional office nearest you.

DDP-116



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CIRCLE 17 ON READER CARD

editor's readout

ATTITUDES, BELIEFS AND COMMUNICATIONS

Last month in a sunny, windy San Diego, representatives of four major manufacturers faced several hundred SHARE attendees to discuss their companies' plans for PL/I. Speaking for their organizations were Lon Grace (RCA), Dick Zemlin (CDC), Charles Bachman (GE), and Bill McClelland (IBM). (Other manufacturers are thinking about or working on PL/I, but these were the only companies of those invited who accepted.)

Grace noted that while the goal of PL/I might well be machine independence, that the language — which he characterized as "very messy" — is not independent of a certain keypunch. He said RCA's effort so far is "very modest" (a subset called PL_{IJ}), but that the language, like Mt. Everest, cannot be ignored. RCA, quite interested in the prestandardization movement (see last month's Look Ahead), is "delighted at IBM's apparent willingness" to let other manufacturers take a whack at the language.

Zemlin's one-word reaction to PL/I: "expensive." And, he pointed out, the user — whether he realizes it or not — will pay for it what he hinted will be an exorbitant price. He argued that a number of small simple languages would be more economical than a universal language like PL/I, which he described as monolithic. He too stressed the importance of prestandardization development, and suggested that a Language Institute might offer a more orderly approach to software design.

Bachman thinks that the original goal of PL/I — one language for the mixed commercial-scientific installation — might be fading: PL/I is now a replacement for assembly languages. He discussed the economics of software production, indicating that PL/I could bankrupt the smaller manufacturer, prevent all from doing any one thing well. He also discussed standardization.

McClelland stressed the difference between prestandardization and standardization. PL/I, he said, is not ready for standardization; but prestandardization work might help avoid the development of different dialects.

The standardization issue dominated the discussion arising out of questions from the floor. One user said, in effect, to hell with standardization. We want a PL/I compiler now. Let IBM go ahead with it: "If this delays the other manufacturers two to three years, that's tough!" (Applause.)

The discussion revealed and underlined several attitudes about programming language development, standardization and the industry in general . . .. attitudes which cloud cognition and impede, if not paralyze, progress.

Some statements indicate that most users really do not understand that they are paying — and paying dearly — for manufacturer-developed software. In an earlier talk at SHARE, IBM's T. J. Watson pointed out that 360 software costs (which are now estimated at $60 million for 1966) will exceed those for hardware. This is not to say, that at present, a suitable alternative exists. But belief that software is free cripples any attempt to start assessing the true cost — and worth — of software in general and specific programming support packages in particular. And it seems to us that such an attempt is necessary if information processing is ever going to apply some of its techniques to its own affairs.

Another attitude uncovered is that a language in the hand is better than two in the (standards) bush. This one is hard to debate, especially when we contrast the important programming and production problems being faced by the user *right now* to the pace of standards progress . . . and because IBM, with the help of SHARE, made a strenuous effort to come up with one language which would help solve the Babylonian programming languages dilemma. But these facts should not obscure the desperate need for an intelligent industry-wide attack on software design.

Finally, the statements about standardization — the failure to distinguish between that and prestandardization effort (whatever that is), the feeling that standardization sets upper boundaries on and freezes progress — indicate an alarming ignorance of the technical importance of standardization, its effects on compatibility, and the economics thereof. More on this topic in a subsequent issue.

We need more frequent dialogues between manufacturers, users and standards workers. And we need clearer definition and understanding of the attitude underlying their attempts to communicate.

TIME-SHARING MEASUREMENT

system & user characteristics

by ALLAN L. SCHERR

This article describes measurements made of time-shared system performance and user characteristics and discusses how they might be applied to the design of future systems. These measurements, taken on the Project MAC time-shared IBM 7094,[1-3] were made as part of a larger study[4] of analysis techniques for time-shared system performance. Users are characterized by the computational load they place on a system. The system's response to this load is a measure of performance. The statistics presented are the results of measurements made during the three-month period from December, 1964, through Feburary, 1965, and of simulations run thereafter.

First, the operation of the MAC system is briefly explained, and the user community described. The parameters measured are defined, and the measurement techniques described. Then, the results of the measurements are presented. Finally, the usefulness of these measurements in determining aspects of the performance of future systems is discussed.

description of the MAC system

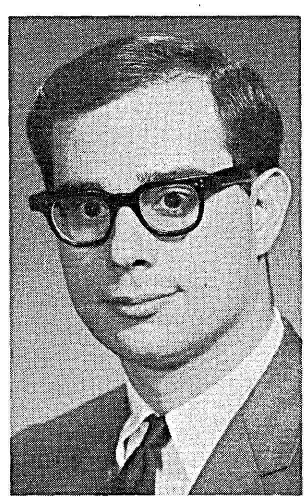
The MAC system, during the period of measurement, consisted of an IBM 7094 (Model I) two 32K 2 usec memories, IBM 1301-2 discs, an IBM 7320 A drum, and an IBM 7750 connected to Teletype Model 35 and IBM 1050 terminals. Other equipment is present (e.g., two tape channels), but is not used during "normal" time-shared operation.

By typing at his console (terminal), a user may communicate with either the supervisory program or a program activated by this supervisor. A line of input for communication with the supervisor is called a "command." Commands cause programs to be loaded from the disc. These programs are queued, and each is executed for a short period of time, not necessarily to completion. The sequence in which programs are run and the duration of each period of processor time is determined by a subroutine in the supervisor called the "scheduling algorithm".

The supervisory program is permanently resident in one of the 32K memories; the other memory is used to hold the command-activated programs while they are being executed. This second memory holds *only one complete program* at a time. The other programs waiting for execution are either on the drum, split between the drum and core, or on the disc prior to the initial loading into core. At the end of a period of processing or "time-slice," the currently running program is dumped into the drum, and the next program to be run is loaded either from the drum or, if it has never run before, from the disc. Only as much of the former program is dumped as is required to make room for the latter. This process is called "swapping." The information swapped between drum and core and loaded from disc to core is called a "core-image."

Users or the programs serving them are considered to be in one of six states. These are:

a. *Dead.* No program is waiting to run for this user; moreover, there is no core-image being saved on the drum. This state is the normal starting point for a user just entering the system. All input lines typed while in this state are commands. After a command is typed, the user's state becomes
b. *Command Wait.* A program is waiting to run for this user, but has not yet run for the first time. When the scheduling algorithm decides to run this program, it is loaded from the disc, and the user's state becomes
c. *Working.* A program is running or waiting to run for this user. A core-image is either in core, on the drum, or split between core and drum. Upon completion of the program, the next state is Dead, Dormant, Input Wait, or Output Wait, depending on the nature of the completion. The Dead state is re-entered on the majority of final program completions; the core-image is erased.
d. *Input Wait.* The user's program required a line of input from the console. Input typed while in this state is sent directly to the program and is not interpreted by the supervisor. Upon the completion of the input line, the program is returned to the Working state. During the time a program is in Input Wait the core-image is saved on the drum.
e. *Output Wait.* Output lines to the console may occur at any time during program execution and are buffered within the 7750. If the program's buffer is full, and the program attempts to write additional



The author is now a staff engineer with IBM's Systems Design Department in Poughkeepsie and was previously associated with Project MAC for two years. He holds SB, SM, and PhD degrees in electrical engineering from MIT and is the author of the book "An Analysis of Time-Shared Computer Systems," published by the MIT Press.

Work reported in this article was supported (in part) by Project MAC, an MIT research project sponsored by the Advanced Research Projects Agency, Department of Defense under Office of Naval Research Contract NONR-4102(01).

[1] Corbato, F. J. et al, *The Compatible Time-Sharing System*, The MIT Press, Cambridge, 1963.
[2] Corbato, F. J. and Glaser, E., "Introduction to Time-Sharing," *Datamation*, November, 1964.
[3] Saltzer, J. H., "CTSS Technical Notes," Technical Report MAC-TR-16, MIT, 1965.
[4] Scherr, A. L., *An Analysis of Time-Shared Computer Systems*, The MIT Press, Cambridge (in press).

output, the program is placed into Output Wait. When the buffer is sufficiently empty to permit restart, the program's state is returned to Working.

f. *Dormant.* This state is functionally identical to Dead except that the core-image is maintained on the drum instead of being erased. This state is entered when it is anticipated that subsequent commands will make use of the core-image. This state may be entered at any time under the control of a key on the user's terminal. In addition, Dormant may be entered for a program-specified period of real time. At the end of this "sleep period" the program re-enters Working and execution is resumed.

the MAC users

The user community, during the period of measurement, consisted of nearly 300 people. Approximately 10% of the usage of the system could be attributed to the staff programmers of Project MAC who were engaged in system maintenance and the development of new time-sharing software. The remainder of the usage was due primarily to research-oriented personnel whose use of the system included simulation of computer systems, (GPSS, etc.), natural language processing (SNOBOL), artifical intelligence (LISP), data reduction, graphical data processing, numerical analysis, (FORTRAN, MAD, FAP, and a version of ALGOL), etc., etc. A small percentage of the usage could be attributed to the administration of Project MAC for personnel records, budget control, etc. It is felt that the Project MAC user community is fairly representative of that found in the computer center of any large university. It is, perhaps, less representative of the typical scientific installation. No claims are made in this regard.

definitions of parameters measured

Most of the measurements which follow are based on what might be considered a basic unit of work on a time shared system, the interaction. The usual form of an interaction is the following sequence of events: the user thinks, types input, waits for a response from the system, and finally watches the response being printed. The process then begins again. The user may be thought of as being in either of two states: 1) The user is waiting for the system to execute a program, or 2) the system is waiting for the user. These two states correspond to Working and Command Wait, respectively. An interaction can now be precisely defined as the activity that occurs between two successive exits from either "working" or "command wait" (transitions between these states excepted).

Fig. 1. Example of a Simple Interaction

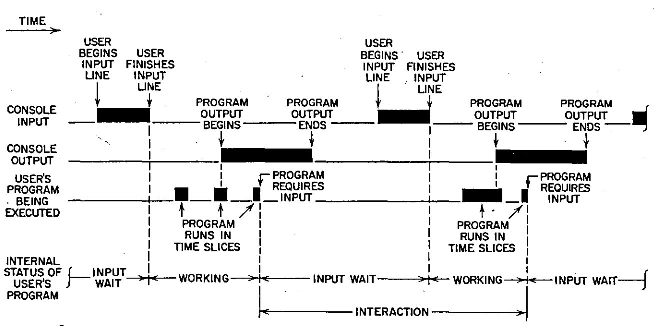


Fig. 1 shows the sequence of events comprising a typical interaction. The activities at the console and processor necessary to complete the interaction are shown along with the states the user's program moves through. Note that the beginning and end of output at the console and the beginning of input have no bearing on the boundaries between interactions. Terminal I/O constitutes a minor load on the system and is therefore subordinated to program activity.

The interaction is divided into two segments. The first portion is the time that the user is in any of the following states: Dead, Dormant, Input Wait, or Output Wait. This part of the interaction will be called the "console portion." The time spent for the console portion is determined by activity at the console: output, input, and thinking. Since the last is generally the chief activity, this time will informally be called the "think time per interaction."

The processor time per interaction is the sum of all time slices used by the program serving the user during an interaction. This time *includes* processor idle time due to disc I/O not overlapped with processing. It is approximately equal to the real time in which the program would run if it were not for time-sharing. The degree of overlapping of disc I/O with processing is strictly a function of the programmer (user). Also included in this time is a small amount of overhead due to the supervisor processing interrupts-scheduling.

The second part of the interaction will be called the "working portion," and corresponds to the user's program being either in Working or Command Wait. The time spent in this portion of an interaction is defined as the response time per interaction.

In the MAC system, the program size parameter is defined as the size of the core-image. Each core-image is assigned a memory bound which may be dynamically changed. For example, the link-loader expands the size of its core-image as it loads subroutines. In order to minimize program size, "common" storage is assigned starting at location zero rather than at 32767 as is conventional in 7090 FORTRAN, etc. Program size was measured on a command entry to either Dead or Dormant.

A command can be alternately defined as being the cause of a sequence of interactions between successive entries into either the Dead or Dormant states. A task is defined as a sequence of commands of the same type. Commands are defined to be one of five types:

1. File Manipulation—printing, combining, splitting, indexing, etc. of disc files (or "data sets".)
2. Source Program Input and Editing—typing in and editing of files containing source programs written in FAP, FORTRAN, MAD, etc.
3. Program Execution and Debugging—link-loading, debugging, and execution of object programs.
4. Compilation and Assembly—processing of source program files to produce object program files acceptable to the link-loader.
5. Miscellaneous—programs to save and resume core-images, programs to generate commands, etc.

The boundary between two different tasks is the changing from one command type to another. This is assumed to occur upon the entrance to either Dead or Dormant.

measurement techniques

The scheduling algorithm in the Project MAC system is entered on every user state change, at the beginning and end of every swap, and every 200 ms. Thus, the scheduling algorithm is constantly aware of the exact status of the system and all its users and provided an excellent point to place a data gathering program. Therefore, data was gathered by a program which ran as part of the scheduling algorithm. This data was reduced to frequency distributions, running totals, etc., *as it was gathered.* This technique eliminated the need to record an elaborate "event stream" for later processing and turned out to require very little space in the supervisor memory (about 2000_{10} locations). Moreover, there was a negligible amount of computation added to system overhead. Approximately 100 usec of computation was required per data point and only on the order of two or three data points were processed per second.

Because it is impossible to accurately control many of the parameters of an actual time-shared system (e.g., the number of interacting users varies with time as people "connect" and "disconnect" their consoles), the results of several simulations are also presented. Suffice it to say that elaborate checks were made to insure that the simulations matched reality by comparing the results of the former with the measurements of the latter. Much more detail may be found in Reference 4.

Except where noted, all of the measurements were made between December 29, 1964, and February 4, 1965, during 112 hours of weekday, 9 a.m. to 5 p.m. operation. Approximately 80,000 commands were monitored. The day-to-day changes in the character of the data was slight, and there was stability in the system as well as user behavior during the period of measurement.

user measurements

Fig. 2 shows the distribution of "think" time per interaction. The impulse of area .12 at time zero is caused entirely by program-generated commands. Other phenomena can be readily identified. The peak under 3 seconds can be attributed to the easily made, trivial responses (e.g., a carriage return on a blank line) occurring while in Input Wait. The peak at around 7 seconds corresponds to the user typing simple commands at their maximum rate. The user must remain in Dead or Dormant for at least two seconds due to the fact that he must

Fig. 2. Probability Density of Time for Console Part of Interaction

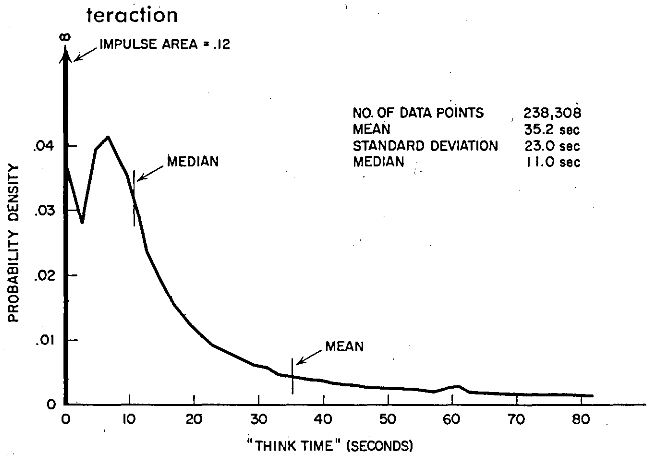
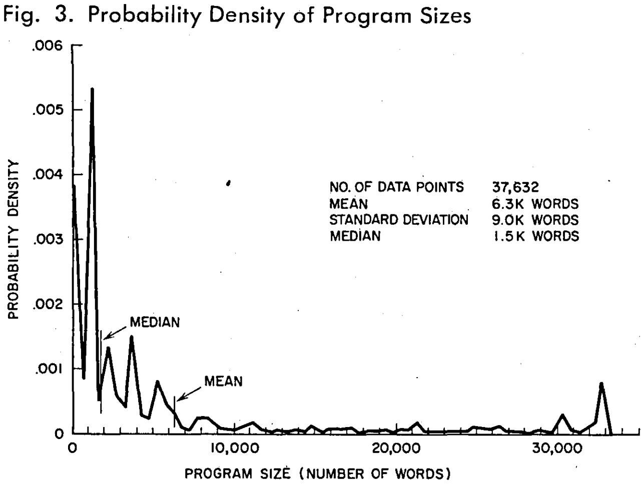


Fig. 3. Probability Density of Program Sizes



wait for a standard "ready" message for the previous command. Superimposed on these maxims is an extensive uniformly distributed time corresponding to both responses requiring the user to stop and think and the times in Output Wait.

The relative probabilities of the user's activity during the console portion of an interaction are:

User typing next command (Dead or Dormant)	.23
User typing program input (Input Wait)	.58
Program waiting for output buffers to empty (Output Wait)	.05
Program "sleeping" (Dormant)	.01
Program-generated command	.12

Fig. 3 shows program size distributions. Most of the peaks in the distribution can be identified as being specific programs (e.g., the MAD compiler). The peak between 1000 and 1500 words can be attributed to the large number of programs consisting only of a few instruc-

Fig. 4. Probability Density of Processor Time per Interaction

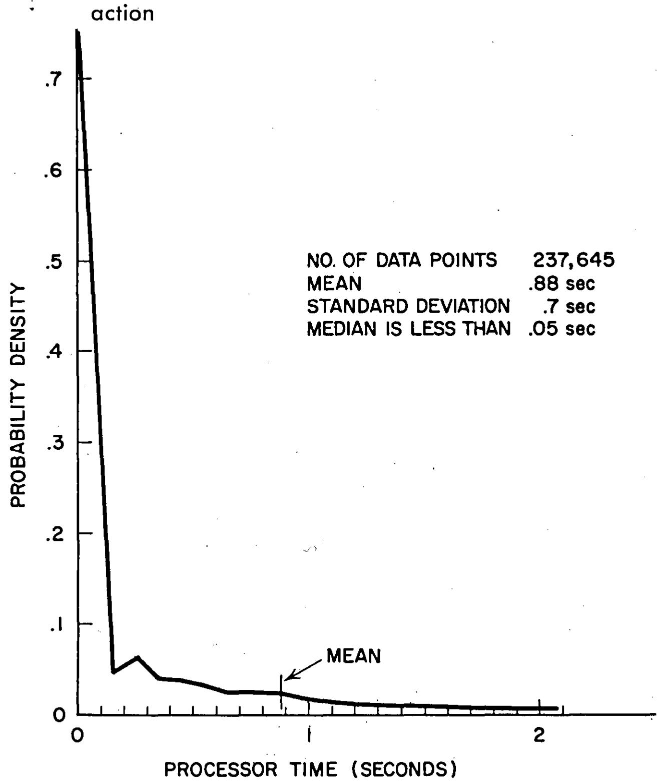
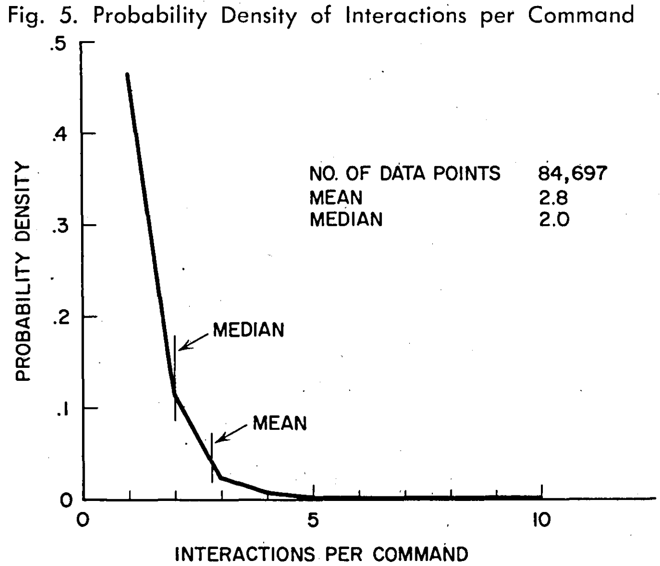


Fig. 5. Probability Density of Interactions per Command



tions and two 470-word buffers for disc I/O. Program sizes were measured in the weeks prior to the remainder of the data due to a size limitation placed on the data-gathering program.

Fig. 4 shows the distribution of processor time per interaction. Measurements have shown that the processor time per interaction includes 3-5% overhead computation by the supervisor and the unoverlapped I/O time required to read, write, or erase approximately 3000 words* of disc storage. Swapping time is *not* included in processor time.

Fig. 5 shows the distribution of interactions per command. Table 1 shows a breakdown of all of the above parameters except program size by task type. The proportion of processor use and of user's time spent for each task type is derived from the measured parameters and is also shown in Table 1.

TABLE 1

	File Manipulation	Program Input and Editing	Program Running and Debug.	Assembly and Compilation	Misc.	Overall
Task probability	.32	.16	.12	.14	.25	—
Command probability	.36	.15	.12	.09	.29	—
Interaction probability	.16	.32	.14	.04	.34	—
Interactions per command (avg.)	1.3	6.3	3.0	1.4	3.4	2.8
Avg. duration of console portion of interaction (sec.)	52	33	38	25	29	35.2
Avg. processor time per interaction (sec.)	1.1	0.4	1.5	3.4	0.6	.88
Prob. of activity during console portion of interaction:						
Typing command	.61	.10	.29	.54	.12	.23
Program-generated command	.18	.06	.04	.16	.18	.12
Input wait	.02	.84	.61	.16	.65	.58
Output wait	.18	.00	.05	.04	.03	.05
"Sleeping"	.00	.00	.02	.10	.02	.01
Avg. interactions per task	2.8	10.7	5.8	1.7	6.3	5.1
Proportion of processsor use	.21	.15	.25	.16	.24	—
Proportion of user's total time	.22	.27	.18	.06	.28	—

system performance

Perhaps the most interesting of the performance parameters from the individual user's point of view is the response time per interaction.

Fig. 6 shows a typical response time distribution, measured from a simulation of the MAC system under a constant load of 25 interacting users.

Fig. 7 is a graph of response time versus processor time on interaction basis and is also a simulation result. Simulation results are used for these two parameters so that the effects of the constantly changing number of interacting users can be eliminated.

Fig. 8 shows the ratio of mean response time per interaction to mean processor time per interaction versus the mean number of interacting users. Each point represents a period of from one to eight hours of actual system

Fig. 6. Probability Density of Response Time per Interaction (Simulation Results)

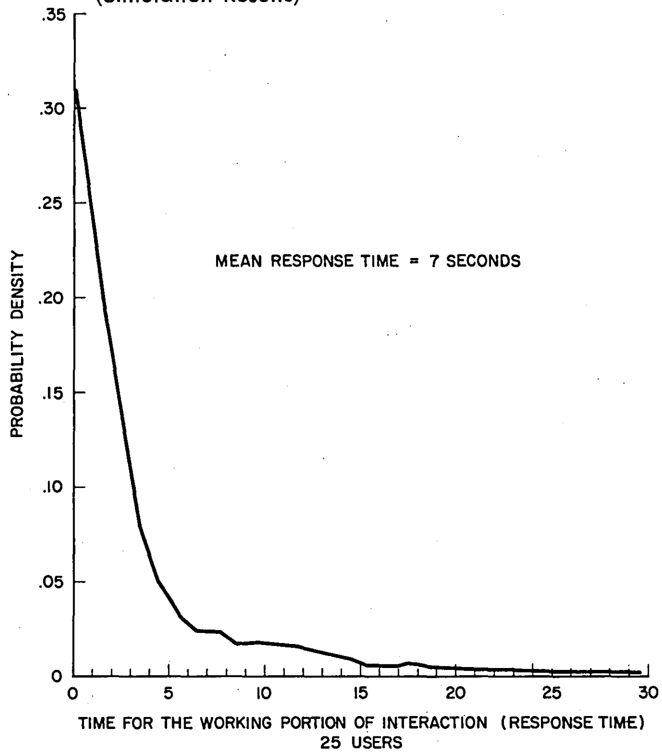
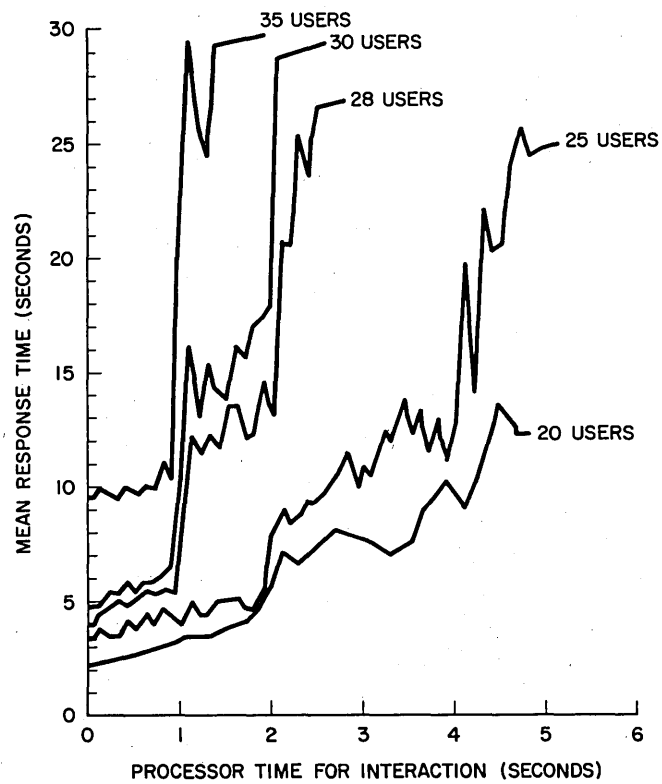


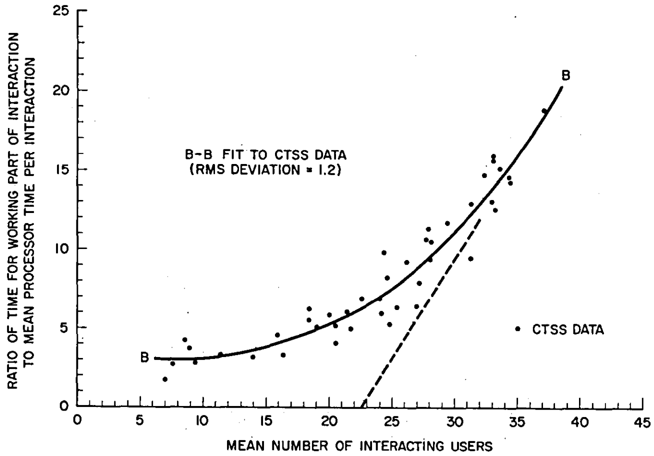
Fig. 7. Mean Response Time vs Processor Time per Interaction (Simulation Results)



* Measured by Mr. Thomas Hastings of the programming staff of Project MAC during the fall of 1964.

operation (i.e., not simulation results). Data from weekend and evening operation is included to give points with fewer numbers of users. The ratio of response to processor time is used rather than just response time in an effort to

Fig. 8. Ratio of Response Time to Processor Time per Interaction vs Mean Number of Interacting Users



normalize the effect of the slight day-to-day changes in mean processor time per interaction. A least-squares, 3rd degree polynomial fit to the data points is also shown.

system saturation

The phenomenon of saturation can be defined in different ways. The author prefers to express saturation in terms of the utilization of the system. Specifically, as the probability that no interacting user is in Working or Command Wait state gets smaller, the system goes further into saturation. Since this probability may become infinitesimal but never absolutely zero, a system is never "completely" saturated. Thus saturation is relative, and a saturation "point" must be defined accordingly.

The degree of saturation can be reduced in many ways: by limiting the total number of interacting users; by decreasing overhead and running times through more efficient system programming; by installing a faster CPU (or an additional processor); better swapping devices, etc.; by using slower consoles, etc.

Saturation can be clearly seen in the plot of the ratio of response time to processor time per interaction as a function of the number of interacting users. At higher loads, the curve of Fig. 8 becomes nearly a straight line. This effect can be derived mathematically.[4]

The saturation point can be defined as the intersection of this straight line with the horizontal axis. For the MAC system, the saturation point is at a load of approximately 22-23 users. This point can also be derived[4] and is the quotient of the mean "think" time per interaction divided by the sum of the mean processor time and mean swap (i.e., idle) time per interaction. For the MAC system, this quantity is $35.2/(.88 + .56) = 24.4$ users.

acceptable performance

Performance has been defined in terms of response time, but it should be clear that there are many other performance metrics of importance. An acceptable performance level for a particular system has no relation to the saturation point. It may, for example, be desirable to operate a system in saturation in order to use the hardware efficiently. However, the response times obtained in saturation operation may be unacceptably high. At Project MAC, it was decided that the system performance with a load of 30 users was adequate. This decision was made after varying the maximum number of users allowed on the system and balancing the user's reactions to the changes in the character of the service provided against system efficiency. Once in saturation, hardware utilization remains nearly constant; and the problem becomes that of balancing the dissatisfaction of some users because of decreased service against the satisfaction of others because more consoles are available. This problem boils down to a question of the desirability of easily available but poorly serviced consoles versus well serviced but relatively unavailable consoles.

With 30 users, the MAC system was saturated, the mean response time per interaction was approximately ten seconds, and CPU utilization for servicing users was 61%. Usage of the drum and disc for the purposes of swapping amounted to 10% and 29%, respectively. It is interesting to note that this CPU utilization is comparable to that of a conventional, batch-processing 7094 installation.

performance predicting models

One of the chief results of the author's use of this data was that accurate performance predictions can be obtained from relatively simple mathematical and simulation models derived from the parameters measured. This accuracy was confirmed by comparing the predictions of models to the actual measured performance of the Project MAC system.

A simple continuous-time Markov Process was used as a model for predicting mean response time and processor usage. Approximating the "think" time and processor time (including overhead swapping time) distributions as exponential distributions with the same mean, it was possible to predict the performance parameters within two or three per cent.

A simulation model was generated which used the distributions of Figs. 2 - 5, and the overall averages of Table 1 as input parameters. The simulation was of sufficient detail so that each of the major events recognized by the scheduling algorithm could be present. Thus, it was possible to use in the simulation program exactly the same subroutine used to schedule the MAC system. Essentially, the level of detail of the simulation matched the data: program execution was handled as merely a requirement for so much processor time; transmission of words between bulk storage and core was simulated as a requirement for a statistically chosen amount of channel time. I/O at the user's console was not included in the simulation because it was considered to place a negligible load on the system.

The above simulation was verified by comparing its predictions to measured data from the actual system. It was then possible to study the behavior of variations on the MAC system with a degree of confidence in the results.

It is felt that similar simulation models could be developed to predict the performance of proposed time-shared systems. Of course, the data presented here must be appropriately translated to reflect the environment of this system. Processor time per interaction must be scaled, the program size distribution changed to reflect the sizes of the standard command programs, etc. It is felt that the think time distribution will remain relatively unchanged under many different circumstances. In any case, using the data of Table 1 and changing the task probabilities appropriately should allow parameters to be selected for a different type of user community.

The author would like to thank the IBM Corporation, his former colleagues at Project MAC, and especially Prof. Herbert M. Teager of MIT for the aid and encouragement of this work. ■

two extra buttons

A PUSHBUTTON TELEPHONE FOR ALPHANUMERIC INPUT

by LEON DAVIDSON

Two current developments in the telephone industry are the gradual conversion to all-numeric calling and the introduction of pushbuttons to replace dials. The telephone companies are making steady progress in their campaign to remove the letters from telephone dials. Each year, more all-numeric local exchange "names" appear. Meanwhile, the pushbutton telephones (Fig. 1, p. 28) are also coming more and more into common use, as the availability of this service steadily increases in all areas of the country. This form of dial provides increased dialing speed since the digit 8, for example, can be transmitted just as rapidly as the digit 1 (as compared with a conventional rotary dial, which takes three times as long to send an 8 as a 1).

Considering both developments in combination leads to an interesting and timely question: Can the telephone dial be used as an alphanumeric input device for computer systems? This paper shows how a 12-button version of the new pushbutton telephone (Fig. 2, p. 28) might be used in a rather simple way as a mixed alphabetic-numeric input device for modern computer systems, without interfering with its ordinary use in placing telephone calls.

Present experiments with multi-terminal computer systems have indicated a current lack of low-cost, simple, input/output devices. This article presents some results of recent studies which show that the pushbutton telephone has many good features when used as a computer input device. Extension of computer services to the average home or business seems to be a reasonable and realistically attainable goal. Wider interest and discussion along this line should stimulate the early availability of other related devices (such as low-cost printer attachments) needed to make the system feasible.

status of telephone dial development

The tone-generating pushbutton telephone is now made and supplied by a number of different telephone equipment manufacturers under various trade names. There is

Dr. Davidson is currently manager of research and development at the computer laboratory of Western Union Management Information Systems Div. His previous experience includes ten years with the Atomic Energy Commission and, most recently, as manager of advanced application development at IBM's Mohansic Laboratory. He received a Ph.D. in chemical engineering from Columbia Univ.

enough standardization in the industry to permit discussion of the subject technically without reference to a specific line of equipment.

Each pushbutton telephone can generate two sets of quasimusical tones, one consisting of four tones and the other of three tones. These tones are assigned to four rows and three columns of a grid layout, respectively. (A tone for a fourth column has been assigned, but is reserved for future use.)[1]

The 4 x 3 grid, defining 12 intersections or tone-pairs, has been used to lay out the present pushbutton dial shown in Fig. 1. Note that the two lower corners are not used, thus providing only 10 "tone-pairs," which are taken to correspond to the 10 digits as used for present telephone calling purposes. Each tone-pair is recognized as a distinct digit by receiving equipment in the telephone company switching system for call purposes.[2]

The design and manufacturing process for these telephones makes it fairly easy to provide working buttons in the two missing corners. Fig. 2 is the layout of a telephone set produced on a commercial basis by a leading manufacturer. The standard receiving equipment can be used at a computer input subsystem or input channel to recognize the full "12 digit" set as sent from such a telephone.

Note that any 10-button arrangement, in which a single button represents a single digit as when dialing a telephone number, can provide only numeric input, whether or not letters also appear on the buttons. The letters on 10-digit rotary dials or 10-button pushbutton telephones are only mnemonic guides to the user, and play no part in the actual switching operation.[3] For obvious reasons, an input string of data composed only of the 10 digits cannot conveniently handle even the most elementary arithmetic problems, let alone handle alphanumeric requirements. There is, for example, no good way to show the start, end, sign, or decimal point in any input number. With 12 buttons, however, a good arithmetical input procedure becomes possible, and a full alphabetic capability can be provided. The remainder of this paper will discuss the use of the two extra buttons to set up a character code for specifying alphanumeric input to a computer via the 12-button telephone dial.

Fig. 1

Fig. 2

assignment of pushbutton character codes

Any alphanumeric character set, to be generally useful, should contain all 10 digits, all letters of the alphabet (26 in English, a few more or less in the alphabets of some other countries) and at least some minimum number of essential punctuation marks, signs, or symbols. Thus, 39 or 40 characters seems to be a reasonable lower limit on the size of a useful character set. For purposes of this discussion, it is assumed necessary to provide a set which includes the 26 English letters, 10 digits, and the four symbol characters:

(   ) Space
(–) Minus
(+) Plus
(.) Dot or Period

making a total of 40 characters.

subdividing the character set

The concept of encoding a character set into subsets, distinguished by characteristic "zone bit" combinations, is familiar to most people who have worked with punched card or punched paper tape systems, character-oriented computer systems, or magnetic tape systems. A broadly similar concept has been used in setting up the character code for the alphanumeric pushbutton dial system discussed in this paper.

The alphabet and the four "punctuation" symbols (30 characters in all) will be divided into three convenient subsets, containing exactly 10 characters each. The assignment of characters to particular subsets depends only on the desired layout of the characters on the faces of the buttons, as will be discussed in the next section. For convenience, the three alphabetic subsets are called the "left," "middle," and "right" subsets, respectively. The digits will be considered to form a fourth 10-character subset.

In the 12-button telephone, 10 of the buttons are called "data buttons." The 40 characters can now be placed on these buttons in any useful or meaningful arrangement, provided that one and only one member of each of the four subsets is placed on each data button. One such layout is shown in Fig. 3, where each data button carries a digit and three letters, one each from the left, middle, and right subsets.

Each of these 10 data buttons can be thought of as generating the computer input character which represents

[1] Meacham, L. A.; Power, J. R.; and West, F.; "Tone Ringing and Pushbutton Calling," *Bell System Technical Journal*, No. 37 (1958) pp. 339-360.
[2] Morrison, C. G., "Central-Office Receiver for Touch-Tone Calling," *Bell Lab Record*, June, 1961, pp. 201-204.
[3] Marill, T.; Edwards, D.; Feurzeig, W.; "Data-Dial: Two-Way Communication with Computers from Ordinary Dial Telephones," *Communications of the A.C.M.*, Vol. 6, No. 10, October, 1963, pp. 622-624.

the actual *digit* which appears on the button, whenever it is pressed.

The two remaining buttons will be called the "function buttons." These carry no characters or symbols,[4] but generate unique characters as computer input when pressed. Call the left function button the "Left" button, and assume it generates some unique computer input code which will be represented by the letter "λ" (Greek letter "lambda"). The right function button will be called the "Right" button, and the unique character which it will generate will be represented by the letter "ρ" (Greek letter "rho").

Several procedures may be set up for using the two function buttons in various sequential combinations to select or identify one of the four subsets: "left," "middle," "right," or "digit." One method, for example, is to depress the Left function button to identify the left subset, the Right function button to identify the right subset, and both function buttons (in succession) to identify the middle subset. When no function button is depressed, the digit subset is automatically selected.

Note that simultaneous depression of two or more buttons on a pushbutton telephone does not generate a valid tone-pair. Therefore, the combination of function buttons and data buttons must be made sequentially, rather than on a simultaneous-pressing basis.

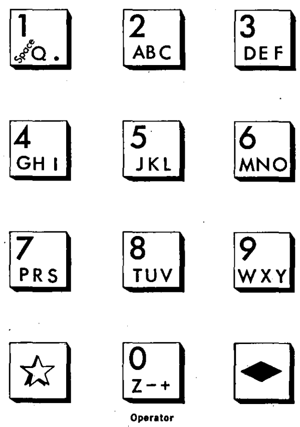


Fig. 3 Layout of 12- button dial with conventional full alphabet (letters Q and Z provided)

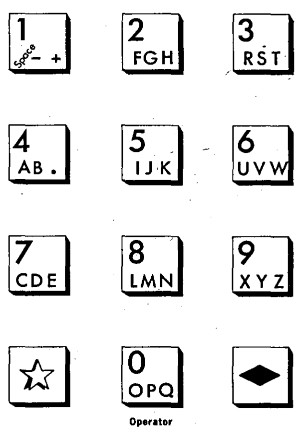


Fig. 4 Layout of 12-button dial with experimental arrangement of alphabet (letter O and numerical 0 on same button)

pushbutton layout

An astronomically large number of different 12-button alphanumeric layouts may be conceived. A full "human-factors" study would be required to select a standard layout for the industry. However, from a number of cases considered in this work, two are presented here as preliminary choices (Fig. 3 and 4). In both, the present "industry standard" arrangement of the 10 digits is preserved (as in Fig. 1 and 2). The new lower left and lower right corner buttons are restricted to use as "function" buttons, and do not represent any specific digits or characters. All alphabetic and other characters appear on the 10 "data" buttons.

For telephone-dialing compatibility, it is desirable to retain the present industry-standard arrangement of the 10 digits themselves. (However, they could easily be converted to the standard office-machine 10-digit keyboard layout by interchanging the second and fourth rows, without affecting the dialing function). Experimentation was limited to assigning the alphabetic and other characters to the digit-buttons, in order to try to meet various criteria. Fig. 3 shows one case which is of special interest. It is based on precisely the same alphabetic layout used on the present pushbutton telephones (Fig. 1) and, of course, agrees with the present rotary dials. Thus, A, B, C, are on the same button as digit 2, while P, R, S, are on digit 7 and W, X, Y, on digit 9. To produce the full alphabet in this case, the missing letter "Z" is restored to the zero-digit button, along with the "minus" and "plus" symbols. The letter "Q", which has never appeared on the American telephone dial, and the characters "space" and "dot" are placed on the digit 1 button.

The chief advantage of the layout in Fig. 3 is that it is compatible with the letter arrangement on existing pushbutton telephones, should any letter-prefixes still be in use by the telephone companies (or the public) at the time that the system might be installed.

The major disadvantage of the "conventional" dial layout of Fig. 3 is the well-known and confusing difference between the locations of the letter "O" and the digit "0". Fig. 4 shows a 12-button dial layout designed to minimize this confusion by putting the "O" and the "0" on the same button. It also, incidentally, restores the letter "Q" to its proper place in the alphabet. (Note that this dial layout could also be used for 10-button telephones of the type shown in Fig. 1, although it is obviously not adaptable to a circular layout of the digits as used on present-day rotary dials.)

effect of frequency distribution on layout

There is a good reason for placing the dot character after the letter B in the alphabetic layout of Fig. 4. It is necessary to press both the Left and the Right function buttons to define the middle letter on any data button. Thus, letters which are used relatively infrequently should be included in the middle subset. The frequency distribution of English letters is often taken to start off something like "etaoin shrdlu . . ." Any letter arrangement should try to keep most of these high-frequency letters out of the middle subset. In Fig. 4, this is done by placing the "dot" character after the letter B, thus keeping both "A" and "E" out of the middle subset. Only "S" and "D" of the 12 letters noted above are found in the middle subset in Fig. 4, and neither of these is in the top six in frequency.

The conventional industry-wide layout of Fig. 3 compares poorly with Fig. 4, when judged on the above basis. Five of the 12 most frequent letters (E, N, H, R, and U) fall in the middle subset, and two of these are among the top six in frequency, E, of course, normally being the letter most frequently used.

For applications which do not involve long input messages consisting of alphabetic text, either layout should prove satisfactory.

procedure for alphanumeric input

The procedure given here would apply to any 12-button layout in which the two function buttons (in this case, the lower left and right corner buttons) do not carry any characters at all. The 10 "data" buttons each carry four alphanumeric symbols, one of which is a digit. The other

[4] As shown in Figs. 2-4, these "function buttons" have been arbitrarily marked with a star and a diamond symbol, respectively, by the telephone companies.

three characters (in the layouts shown here) lie in a separate horizontal line on each button, which permits reference to the "left," "middle," and "right" characters (non-numerics) on each data button.

The essence of the input coding system proposed in this article is that any given non-numeric character or symbol is to be selected and defined by the user as follows:

1. Locate the data button on which the character appears. (Since the alphabet is laid out fairly well sequentially in either layout, this is not difficult after a short learning period.)
2. Push (tap) the button and, at the same time, observe the position of the desired (non-numeric) character on that button.
3. a. If the desired character was the *left* character on its button (for example, "A"), push the corresponding "Left" function button.
   b. If it was the *right* character on its button (for example, "+"), push the corresponding "Right" function button.
   c. If the desired character was the *middle* character on its button (for example, "B"), push *both* "function buttons," *one at a time,* in any order.

If the user wants to select a digit, rather than an alphabetic or special character, it is sufficient merely to press the data button on which the desired digit appears. The user must not press any function button immediately after this. Thus, a string of consecutive digits may be entered with no use at all of the function buttons.

This system of input provides for very simple computer handling and interpretation of mixed alphanumeric input strings. There is no need for any specific user action to identify the start or end of a string or substring of digits or other characters.

Each appearance of a "data button" character (i.e., digit) in the input string is a signal to the computer to decode the preceding part of the input string, starting with the most recent previous "data button" character. The function buttons that have intervened will determine the subset to be applied in translating that previous data character. (In handling the end of an input string, the end-of-message character will serve as the appropriate signal, so the last intended character will not be lost).

Using the dial layout of Fig. 4, the message "8446T44 EAGLE." would generate the following character string as input:

$$8\ 4\ 4\ 6\ 3\ \rho\ 4\ 4\ 1\ \lambda\ 7\ \rho\ 4\ \lambda\ 2\ \lambda\ \rho\ 8\ \lambda\ 7\ \rho\ 4\ \rho$$

For the reader's convenience, this is shown below grouped for decoding, where each appearance of a digit is a signal for the start of a decoding group:

$$8\ 4\ 4\ 6\ 3\rho\ 4\ 4\ 1\lambda\ 7\rho\ 4\lambda\ 2\lambda\rho\ 8\lambda\ 7\rho\ 4\rho$$

The message, as decoded by the computer, when working with the layout of Fig. 4, is then of course:

8446T44 EAGLE.

punctuation and formatting

Punctuation may be specified in a variety of ways, depending on the application being handled. A few simple examples follow, based on the character set used in Figs. 3 and 4.

a. A number is ended by entering its algebraic sign, + or −, or a space character, at the end of its string.
b. A number may include a decimal point or "dot" within its string.
c. An alphanumeric word or name ends with the space character.
d. The end of a sentence or statement may be defined by a dot character followed by two space characters, as in typing.
e. The "end of message" signal can be three or more consecutive taps of either function button, recognizable by hardware.

In an actual installation of the system, a suitable consistent set of punctuation could be set up for each application, and for the system in general.

application considerations

Many forms of output from a computer over telephone lines already have been developed, including "voice-answer" systems as used at stock exchanges. Small low-cost strip printers could readily be developed and produced for use as "hard-copy" output devices. With such outputs available, services could be provided from metropolitan computer centers to professional and business people, as well as to the household. Applications which do not require extensive data-base files would be the most suitable for early exploitation, since there would be no need for long trunk-lines or toll charges to obtain data from a distant computer center and no need for extensive data-gathering for file-updating. Thus, a reminder-message service or an adding-machine service might be an early application. Likewise, a "Shopping-by-phone" service could be provided, in which the housewife could directly enter catalog numbers (which usually contain letters) and other alphanumeric information.

A noteworthy aspect of the use of the 12-button pushbutton telephone is the capability which it provides for direct entry of machinable data into a computer system. In the reminder-message service, the future date and time for issuance of a reminder (back to the originator) can be entered by anyone, over his own office or home telephone, a roadside telephone, or a hotel phone. The text of the reminders might well be audio-recorded for future playback, but the automatic retrieval indexing would be based on the alphanumeric machinable input from the telephone dial. The reminder would be issued to the (stated) home or office phone.

conclusion

The technique of alphanumeric input to a computer system over telephones has been discussed in this paper from the viewpoint of the user, sitting at his telephone.

The economics of these applications will depend on many factors which need still to be resolved by discussions within the industries involved. The outlook seems good for providing low-cost access to computers for use by the general public, if the public interest is aroused in time to help shape these trends.

Although there is much still to be resolved regarding applications and hardware for telephone input-output computer service, wider discussion of these possibilities should help promote the early development of such systems. ■

ACKNOWLEDGMENTS

The procedure for use of the two "function" buttons to define the four alphanumeric subsets was developed with the assistance of Dr. Gerald Goertzel. The adapter used to connect a standard 12-button telephone to the computer system was designed and provided by Messrs. R. A. Jensen, W. J. Levine, T. J. Carlton. Thanks are also expressed to the staff of the Time Sharing Project, who established and maintained the real-time multi-terminal environment in which this system was run. All of the above and the author were in the IBM Advanced Systems Development Division, Mohansic Laboratory, when this work was done.

PROGRAMMING THE COMPACTS

integration of sectored memories

by CHARLES W. WALKER

The recent trend in small computer design has been away from what might be called the classic single-instruction, single-address format that most word-type computers have traditionally employed. The most significant departure is in the method used to address memory. Typically, these computers are unable to directly address more than a small portion of the total memory at any given time. They generally have a memory structure of 2^n words divided into 2^m sectors, each sector having 2^{n-m} words.

The fundamental reason for this type of memory structure is to reduce the number of address bits required in an instruction word. This is very important in the design of short-word-length computers. Take, for example, a computer having a 16-bit word length and 2^{14} (16,384) words of memory. To directly address any word in a 2^{14}-word memory requires an address of 14 bits. If this 14-bit address were required in every instruction word, only two bits would remain for specifying operation codes, indexing and indirect addressing—hardly a practical arrangement. If the memory is divided into 2^m sectors, the address field of the instruction can be reduced by m bits. If the 2^{14}-word memory is divided into 2^5 (32) sectors, the address field can be reduced to nine bits, leaving seven bits to specify the operation code, indexing, etc. This is a very workable arrangement. Several computers have been built with this general structure, some having words as short as 12 bits and sectors as small as 32 words. Of course, as the sector size decreases, the probability of any instruction being able to directly address its operand decreases.

The usual design has the contents of one or two sectors directly accessible to any given instruction. Numerous techniques have been devised to enable any instruction to access all of memory. Among the more common schemes are bank selection, displacement addressing, two words per instruction (to permit a full instruction address), indirect linkage, indexing and various combinations of the above. With instructions generally unable to directly access all of memory, the interaction between hardware and software becomes even more important a consideration than it is with computers employing the classical structure.

Desectorizing™ software was developed to make a computer having a sectored memory appear to the programmer as if all of its memory were contiguous and at all times directly addressable, and to make possible the writing of highly efficient (both in terms of memory utilization and program execution time) relocatable programs. One of the fundamental advantages of desectorizing to the programmer is much the same as one of the fundamental advantages of an assembly program: the programmer need not concern himself with where in memory an operand is located. All that is necessary is to symbolically refer to that operand, and the assembly program will provide the proper instruction address. Desectorizing in conjunction with an assembly program provides, in addition to the symbolic reference to operands, the automatic generation of any linkage necessary to reach that operand if the operand is not directly accessible.

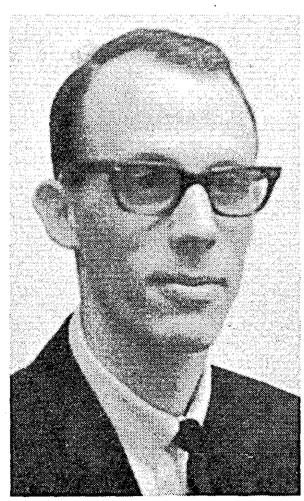
Before embarking on a more detailed description of Desectorizing, it is necessary to describe in some detail the type of computer to which Desectorizing is applicable.

typical sectored memory

Desectorizing has been developed for the Computer Control Company DDP-116 computer, which typically has a memory of 16,384 words divided into 32 sectors, each sector having 512 words. The DDP-116 instruction word consists of an indirect address indicator, an index indicator, a four-bit operation code field, a one-bit sector indicator and a nine-bit intra-sector address.

If the sector indicator is zero, the nine-bit intra-sector address addresses any location in sector 0. If the sector indicator is 1, it addresses any word in the currently active sector. The currently active sector is specified by the most significant five bits of the 14-bit program counter. This means that the DDP-116 instruction can access any one of 512 words in the currently active sector or any one of the 512 words in sector 0. If the indirect indicator is set, specifying indirect addressing, the referenced indirect address word contains an indirect indicator for multiple level indirect addressing, an index indicator for multiple level indexing, and a true 14-bit address. The true 14-bit address in an indirect address link, of course, can specify any word in the total computer memory. Basically then, for the DDP-116 instruction to access an operand neither in the currently active sector nor in sector 0, it is necessary to go through an indirect link to specify the actual operand address. It is this link that is automatically generated by the Desectorizing logic.

Desectorizing is applicable to any machine of similar



Mr. Walker is supervisor of software development at Computer Control Company, Inc., responsible for conceptual design, writing, and checkout of programming systems. Previous affiliations included RCA, GE, and North American Aviation. At RCA's Data Systems Division, he was a senior member of the engineering staff.

design. The primary requirement is that the address extension (which is primarily what the indirect link is in the DDP-116) be located outside the code string—i.e., that it not be necessary for the assembly program or the loader to insert instructions in the code string during assembly or loading. We find that this basically excludes machines utilizing bank selection or two words per instruction because these methods would require that the address extension be inserted in line in the code in the form of a bank select instruction, or the second word of an instruction where necessary in the two words per instruction configuration. Of course, Desectorizing is not necessary with a computer having a two-words-per-instruction configuration provided it is acceptable that every instruction occupy two words. This in effect means that every instruction has a full address and therefore need not be desectorized; however, the program would require up to twice as many memory locations for instructions, and would take up to 50% longer to execute than a comparable desectorized program.

desectorizing operation

Desectorizing results from the combined operation of the assembly program and the Desectorizing loader. The assembly program for the DDP-116 generates an extended object code which includes, in addition to the indirect and index indicators and operation field, a true 14-bit address; thus, the assembly program has generated code as if any instruction could access an operand anywhere in memory. Note that it is not necessary to include the sector indicator bit in the extended object code.

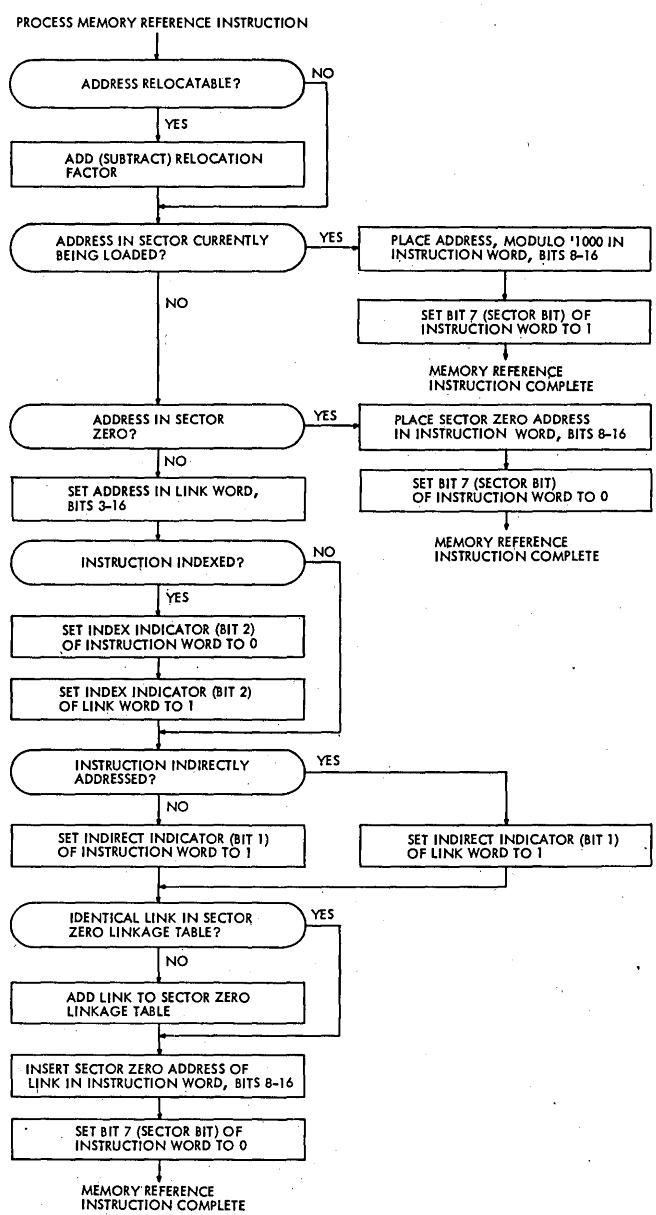
Relocatable programs, which would have been impossible had the programmer been required to do all his own address linkage, now become a trivial operation when applied to extended object code. The Desectorizing assembly program, like any other assembly program, must produce control codes for the loader in addition to the object code. These control codes provide the loader with information regarding the relocatability of each address.

Fig. 1 shows the treatment of memory reference instructions during desectorized program loading. When loading desectorized programs part or all of sector 0 must be reserved for the linkage table that is generated by the loader during the loading process. Referring to Fig. 1, we see that the loader, once having determined that it is processing a memory reference instruction, now checks to see if the instruction address is relocatable. If it is, the relocation factor is either added or subtracted depending on whether the address is positively or negatively relocatable. Note that the relocation factor is added to the true 14-bit operand address taken from the extended object code.

Having now established the absolute location of the operand, the loader checks to see whether the address that it has just developed is in the sector currently being loaded. The sector currently being loaded would be the active sector when the program is executed. If the address is in the sector currently being loaded it is not necessary to generate an indirect link, and the loader truncates the address to nine bits and places this address in the instruction word. The sector bit of the instruction is then set to 1, indicating that the operand is in the active sector and the memory reference instruction processing is complete. If the address is not in the sector currently being loaded, a check is made to see if the address is in sector 0. If so, this is also directly accessible to the instruction and the address is again reduced to nine bits and placed in the address portion of the instruction. In this case, the sector indicator is set to 0 indicating that the operand is in sector 0. If the address is neither in the sector currently being loaded nor in sector 0, a link word is generated. The true 14-bit address is taken from the extended object code and placed in the address portion of the indirect link. A check is then made to see if the instruction is indexed. If it is, the index indicator of the instruction word must be set to 0 since indexing is not desired in accessing the indirect link. The index indicator of the link word must be set to 1 so that indexing takes effect when the final operand address is formed. If the instruction was not indexed, these two steps are skipped.

Next, a test is made to see if the instruction was indirectly addressed. If so, the indirect indicator in the link word is set to 1. If the instruction was not indirectly addressed, the indirect indicator of the instruction word is set to 1. At this point the link word is complete. A search is now made of the linkage table being developed in sector 0. If an identical link is not already in the table, the new link is added to the table. In either case the sector 0 address of the link word is placed in the instruction and the sector indicator bit of the instruction is set to 0. The desectorized memory reference instruction

Fig. 1. Treatment of Memory Reference Instructions During Desectorized Program Loading.



is now complete. Notice that the Desectorizing logic generates an address link only when determined to be necessary at load time and that, if a link is necessary, identical links are never duplicated in the linkage table. This results in very efficient utilization of memory and also permits very efficient relocatable programs since the determination for whether a link was necessary is made at load time and not at assembly time.

advantages for the programmer

Let's look now at how Desectorizing helps the programmer.

Fig. 2 represents, on the left, a segment of a program as the programmer conceived it. The fields on a line reading from left to right are: symbolic location, mnemonic operation, and symbolic address. An asterisk appended to the operation indicates that indirect addressing is desired. Comma 1 appended to the symbolic address indicates that indexing is desired.

Fig. 2 represents, on the right, the same program segment with respect to its proper location in memory. The numbers in the left-most column represent the actual memory locations. We see that a sector boundary exists between location 1777 and 2000. Instructions appearing above the sector boundary cannot directly access operands below the sector boundary, and vice versa. We see on the left the program as it originally appeared. On the right is the program as the programmer must modify it without Desectorizing to take care of the intersector references. In location 1777 the programmer has had to change his instruction from ADD X1 to ADD* (indirect) Z1 and develop an address link Z1 containing the address X1. This address link Z1 must either appear somewhere else in sector 1 or in sector 0. In location 2001 the programmer has had to change the instruction from SUB A3,1 to SUB* (indirect) Z2 and again develop a link Z2 somewhere in sector 0 or in sector 2 containing the address A3,1. Similar changes must be made in locations 2003 and 2004. Note that the address link required in location 2004 is identical to the address link required in location 2001. Had the programmer failed to notice this he would have generated a redundant address link.

When we examine the program text on the right, we find that, although it performs exactly the same function as the program text on the left was intended to perform, it bears little actual resemblance. Instructions that were indexed and not indirectly addressed are now occasionally

Fig. 2

DESIRED PROGRAM					PROGRAM AS IT MUST BE WRITTEN TO ACCOUNT FOR SECTOR BREAK (WITHOUT DESECTORIZING)		
					Z1	ADDRESS	X1
1771	A1	RESERVE	1	SECTOR 1	A1	RESERVE	1
1772	A2	RESERVE	1		A2	RESERVE	1
1773	A3	RESERVE	1		A3	RESERVE	1
1774		LOAD	A1			LOAD	A1
1775		ADD*	A2			ADD*	A2
1776		STORE	A3,1			STORE	A3,1
1777		ADD	X1	SECTOR		ADD*	Z1
2000		ADD	X2	BOUNDARY		ADD	X2
2001		SUB	A3,1			SUB*	Z2
2002		STORE	X3			STORE	X3
2003		ADD*	A1			ADD*	Z3
2004		STORE	A3,1			STORE*	Z2
2005	X1	RESERVE	1	SECTOR 2	X1	RESERVE	1
2006	X2	RESERVE	1		X2	RESERVE	1
2007	X3	RESERVE	1		X3	RESERVE	1
					Z2	ADDRESS	A3,1
					Z3	ADDRESS*	A1

indirectly addressed and not indexed and the actual operand address is removed from the text of the program thus making the program considerably more difficult to debug. In addition, the programmer has had the responsibility for developing three address links and finding some place for these links to be stored. Having modified the original program to load correctly is only half the battle. Next come the inevitable program changes.

Modifications of the desired program, seen in Fig. 3, account for crossing a sector boundary plus its new changes and also the new modifications required to make the changed program execute correctly. We find now in sector 1 that no indirect address links are required. However, the programmer was not sure that Z1 was not used somewhere else so he has not removed it. In sector 2 a new link is required at location 2000. This link is assigned the symbolic location Y1 and has the address A3,1. The programmer has failed to notice that a similar link was previously assigned and identified as Z2. In 2001, a link that was developed to make the program load correctly last time now must be removed because the operand is in sector 2, but the link is in sector 1. Thus another change has been necessary. We find that the programmer has now produced two redundant words to his program, one for being unsure whether he can remove the link in Z1 or not, and one for not observing that the address link Y1 was identical to the address link Z2. This may appear unlikely in a program of this size and certainly it is. However, in a program filling many sectors, it is not difficult to visualize how redundant links might be left in inadvertently or for new redundant links to be generated, particularly as the program grows older and is less fresh in mind. Again, since the programmer has created the address links at assembly time, it is impossible for the loader to relocate the program at load time.

Fig. 3

	DESIRED PROGRAM AS PREVIOUSLY MODIFIED PLUS CHANGES				PROGRAM PLUS CHANGES AS IT MUST BE MODIFIED TO ACCOUNT FOR SECTOR BREAK (WITHOUT DESECTORIZING)		
	Z1	ADDRESS	X1		Z1	ADDRESS	X1
1771	A1	RESERVE	1		A1	RESERVE	1
1772	A2	RESERVE	1		A2	RESERVE	1
1773	A3	RESERVE	1	SECTOR 1	A3	RESERVE	1
1774		LOAD	A1			LOAD	A1
1775		ADD*	A2			ADD*	A2
1776		STORE	A1			STORE	A1
1777		ADD	A3,1	SECTOR		ADD	A3,1
2000		STORE	A3,1	BOUNDARY		STORE*	Y1
2001		ADD*	Z1			ADD	X1
2002		ADD	X2			ADD	X2
2003		SUB*	Z2			SUB*	Z2
2004		STORE	X3	SECTOR 2		STORE	X3
2005		ADD*	Z3			ADD*	Z3
2006		STORE*	Z2			STORE*	Z2
2007	X1	RESERVE	1		X1	RESERVE	1
2010	X2	RESERVE	1		X2	RESERVE	1
2011	X3	RESERVE	1		X3	RESERVE	1
					Z2	ADDRESS	A3,1
					Z3	ADDRESS*	A1
					Y1	ADDRESS	A3,1

In Fig. 4 (p. 34) the program is as originally written and loaded using Desectorizing logic. We notice immediately that the program as written remains exactly as the programmer conceived it, thus it is much easier to debug and to change at a later date. Sector 0 contains the necessary linkage table. We notice also that the linkage has not been inserted in line and thus has not violated one of our fundamental rules for Desectorizing. If we examine the program as loaded into memory we will find that it very closely reflects the program changes that were necessary for the programmer to make as shown in Fig. 2. However, the programmer is not aware of these changes and has not had to concern himself with them.

Fig. 4. Desired Program as Loaded Into Memory Using Desectorizing.

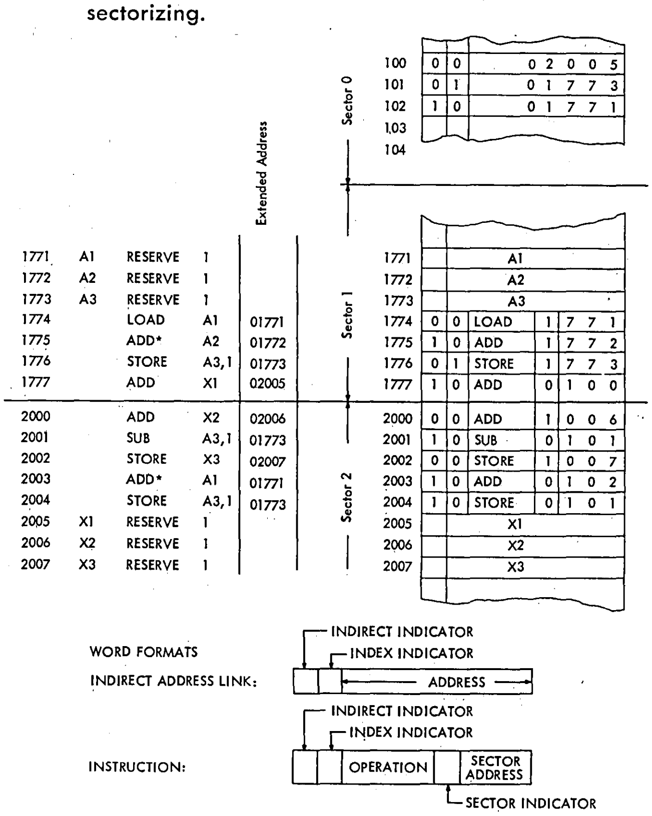
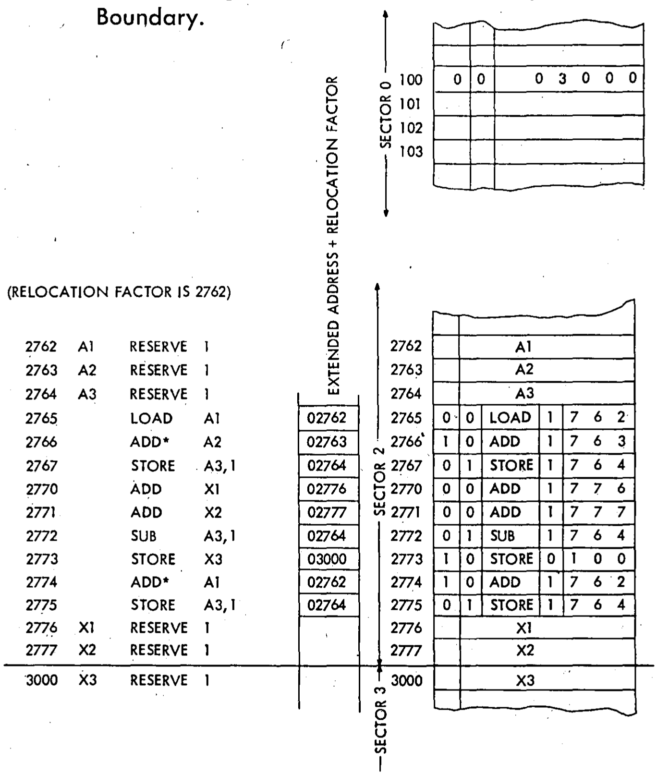


Fig. 5. Desired Program as Relocated Crossing a Sector Boundary.



NOTE THAN ONE ADDRESS LINK IS GENERATED FOR THE REFERENCE TO X3.

Without Desectorizing, as in Fig. 3, when more and more changes are made to the program, the program less and less resembles its original form and thus becomes continually more difficult to debug. With Desectorizing, program changes are made to a program written as originally conceived by the programmer; thus, symbolic addresses remain unchanged and the general character of the program is preserved. Any changes required in the address linkage are automatically handled by the Desectorizing logic.

As shown in Fig. 5, the same program in relocatable mode has been loaded so that the last location (X3) overlaps into sector 3. In the center column is the address portion of the extended object code plus the relocation factor (2762). The right-hand column shows the program as it appears in memory. Note that the reference to X3 (location 2773) requires the generation of an address link. This link appears in the sector 0 linkage table. Of course, if a sector boundary had not been crossed, no linkage would have been generated in sector 0. This example serves to illustrate how the Desectorizing loader is able to load relocatable programs and that, as in absolute programs, the requirement for an indirect address link is determined at load time rather than assembly time.

experience with desectorizing

Desectorizing has been in use with the DDP-116 assembly program (and with the FORTRAN IV compiler) for several months. Experience has shown that certain programming techniques tend to minimize the number of links developed by the loader. The normally good programming practice of dividing a program into relatively small logical modules has been found to be one of the most beneficial methods of minimizing address links. Another is to keep variables close to where they are used rather than placing them all either at the end or at the beginning of the program. Fully relocatable FORTRAN IV programs occupying nearly 16K of memory when loaded with their subroutines have been loaded successfully without overflowing sector 0 with the linkage table. This indicates that having 1/32 of memory available for address linkage appears to be adequate, at least from our experience to date.

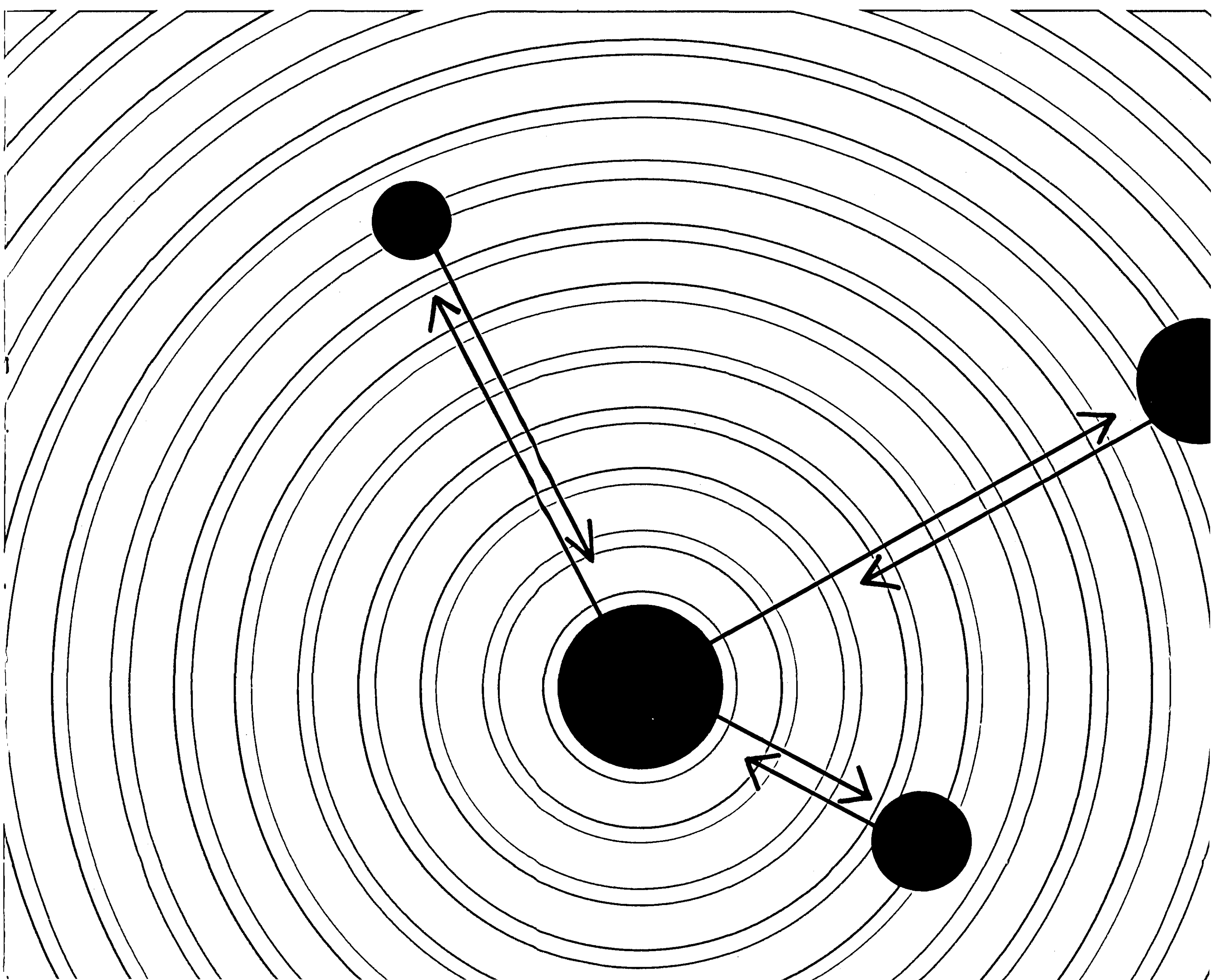
Variations of the Desectorizing logic which first try to place links in the sector that the instruction is in before resorting to sector 0 are now being investigated in case 1/32 of memory proves to be insufficient when loading large programs. Many other variations based on Desectorizing are possible, such as pooling all literals in sector 0 to minimize execution time of the program and the development of various assembly-directing pseudo operations which guide the loader in making more efficient use of storage.

One such pseudo operation currently in use causes the loader to load relocatable programs smaller than a sector wholly within a sector and without requiring any indirect linkage to be generated within that program. This is particularly beneficial when loading programs that have a high use rate (such as arithmetic packages that are used in tight loops, etc.) in that execution time of the program is not increased by the introduction of indirect address links. This may also be important in the development of real-time programs where the programmer is interested in saving every microsecond possible. As more and more experience is gained with Desectorizing, many improvements are certain to be developed, but to date it has proved to be a very effective way of making a computer having a non-contiguously addressable memory appear to the programmer as a contiguously addressable memory and to provide a capability for truly efficient relocation programs. ■

One of a series on topics of importance to data processing management

Honeywell report on Data Communication

Managements across the country are combining the talents of the computer with modern communication techniques to achieve more efficient operations, improved use of corporate resources, tighter control and coordination of operating elements, and faster response to transactions. However, these benefits, and the potential cost savings associated with them, can come only to those managements that have carefully evaluated the response requirements of their data processing operations and have made these major considerations in the choice of a data communication system. This report indicates opportunities for effective and economical data communication, discusses requirements for an "on-time" system, and summarizes the equipment and services available to Honeywell Series 200 users.



DATA COMMUNICATION ADDS REACH TO YOUR COMPUTER

The ability of a data communication system to link computers, or to extend the power of a central computer to remote locations, has tremendous potential for business, industry and government. More specifically, some of the basic functions or activities that are benefitting from this capability are:

1. Customer Order Entry — where the nature of the product or the market necessitates immediate response as to order status.
2. Control of Irreversible Transactions — where complex analyses of information to support such actions as the granting of loans and credit are required for management decisions.
3. Data Collection — where volume, tendency for human error, and extent of processing require greater discipline in collection methods.
4. Control of Interdependent Operations — where involved and complex operations such as job scheduling and production control can benefit from faster exchange and processing of data.
5. File Interrogation — where dynamically changing information such as stock price quotations must be constantly available for quick decision.
6. Customer Service — where response to customer queries within limited waiting time is desired, as in a hospital admission or savings bank system.
7. Information Retrieval — where provision for high-speed insertion, deletion, and access to large volumes of textual material is a requirement.

Although each of these application areas is distinguished by its particular response requirements, there is an "on-time" attribute common to all. "On-time" in one instance may mean instantaneously, or in real time. In another case "on-time" might well be within an hour, a day, or even a week. Since the cost of a system increases rapidly as the response time of the system decreases, the "on-time" requirement of an application becomes an important economic consideration.

THE ON-TIME SYSTEM

A significant feature of the communication-based on-time system is that it places a heavy demand on the computer manufacturer to provide system elements which can function in a wide range of on-time situations. The following sampling of Honeywell data communication applications indicates the flexibility that can be achieved when a product line is geared to this design goal.

☐ A large distributor handles 3,000 orders per day on an inventory of 20,000 items by linking two Honeywell computers at the home office to several warehouses via teletypewriter. Upon receipt of a warehouse order, the computer runs a credit check, computes quantity, brand, size, and price, and transmits the totalled invoice back to the warehouse in only minutes.

☐ A large manufacturer uses a Honeywell computer to control message switching for a nation-wide network of 100 teletypewriter stations concurrently with data processing. The computer receives the message from the sending station, stores it, and forwards it to the receiving station upon availability of an outgoing line.

☐ A racing association system uses two Honeywell computers which, in conjunction with ticket-issuing machines, record all types of pari-mutuel bets and compute odds and payoffs instantaneously.

☐ A Honeywell system handles some 300,000 inquiries per day for a national credit bureau. All credit inquiries are answered within 24 hours.

☐ A trucking firm uses a Honeywell data communication system in which several freight terminals can be linked with the home office. Among other things, the computer calculates charges and transmits final freight bills to the destination terminal before the arrival of the trucks.

☐ A telephone company uses a matched pair of Honeywell computers to provide long-distance operators with split-second voice response to their queries on rate information. The system handles 5,000 inquiries per hour from operators throughout a five-state region. Formerly, it took operators using a rate book 45 seconds or longer to determine the rates.

HARNESSING TWO TECHNOLOGIES

The foregoing examples illustrate the diversity of applications and organizations now using data communication. This diversity will multiply in the near future as data communication developments continue to occur at a rapid pace. Already, central processors have made significant advances in their ability to control large-scale inquiry, data collection and message-switching systems. A greater range of more economical and sophisticated terminals is appearing in the marketplace. Systems design is maturing as evidenced, for example, by more efficient joint voice-data use of telephone services. Communications facilities, services and tariffs offer more flexibility than ever before.

Since the computer is the hub of the data communication system, it is up to the computer manufacturer to provide facilities that will fully exploit the systems design flexibility offered by proliferating developments in communications technology.

DIMENSIONAL DATA COMMUNICATION

Dimensional data communication is one facet of the "dimensional data processing" concept underlying the design of Honeywell Series 200 systems. Under this concept, Series 200 capabilities are available in small increments making it possible to tailor a Series 200 system to meet both the functional and capacity requirements of a user's job. He needn't be saddled with oversized and costly capabilities which he does not need. Furthermore as his workload increases, capabilities can be added or expanded, gradually and economically. Inasmuch as data communications involve both a computer and communications facilities, here's how the dimensional concept applies to both of these.

COMMUNICATION FACILITIES

Most of the elements in a communication system — such as terminals, data sets, and communication lines — are available in a wide variety of types and capabilities and thus offer ample flexibility for precisely tailored systems, initially and as the user grows. However, in order for a computer to communicate over a particular line and with a particular terminal, the computer manufacturer must provide a communication interface designed to handle that specific line-terminal combination. The interface is therefore the key to flexibility and the cornerstone to economical systems design. The greater the variety of communication facilities that the computer can handle, the greater the chances for a system of optimum design.

Honeywell Series 200 systems are available with a full range of communication interfaces providing an extremely broad selection of line-terminal combinations (see accompanying table). Furthermore, the number as well as the variety of lines and terminals that can be combined in a single system are sufficient to fill the requirements of any application.

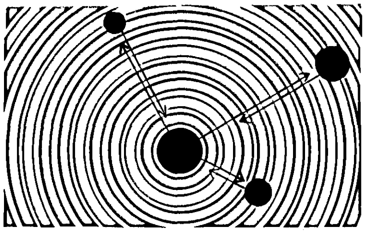
The Series 200 interface capability includes both single-line and multiline communication controls. Both controls are available with either character-by-character or message modes of operation. The single-line controls can send and receive data at the high speeds available through TELPAK, and still faster units can be provided on special order. The multiline controls can handle transmissions over as many as 63 lines simultaneously. It can accept varied combinations of remote terminals and can handle lines with speeds up to 300 characters per second and a total of 7,000 characters per second for all lines, a rate exceeding the requirements even of high-volume, 63-line message-switching systems.

In addition to the wide range of non-Honeywell devices that it can accommodate, Honeywell's Series 200 includes its own excellent terminals. These include CRT display devices and the Data Station, a multipurpose remote terminal. The Data Station features several optional capabilities including direct keyboarding, printing, card reading, paper tape reading and punching, and optical bar code reading — a unique capability for on-line or off-line handling of returnable documents such as insurance premiums and utility bills.

A Partial Listing of Communication Facilities That Can be Incorporated in a Honeywell Series 200 System

Terminal	Service & Line	Data Set	Transmission Speed
DATASPEED[1] 2	Voice-Grade Private Line DDD	202D 202C	105 cps
DATASPEED[1] 5 RECEIVERS	Voice-Grade Private Line DDD	402C	75 cps
DATASPEED[1] 5 SEND UNITS	Voice-Grade Private Line DDD	402D	75 cps
DIGITRONICS DIAL-O-VERTER[2]	Voice-Grade Private Line DDD	202D 202C	150 cps
DIGITRONICS TYPE 1 DIAL-O-VERTER[2]	Voice-Grade Private Line DDD	201B 201A	300 cps 250 cps
FRIDEN COLLECTADATA[3] 30	Voice-Grade Private Line DDD	103F 103A	30 cps
Honeywell Series 200 Computer[4]	Voice-Grade Private Line DDD	201B 201A	300 cps 250 cps
	Telpak A 48 KC Broad-Band Channel	301B	5100 cps
Honeywell Data Station	Voice-Grade Private Line DDD	202D 202C	120 cps
IBM 1050	W. U. 180 Baud Tel. Co. 150 Baud Voice-Grade Private Line	1181.1A 816 103F	14.8 cps
	Tel. Co. TWX-CE Tel. Co. DDD	103A 103A	14.8 cps
IBM Standard STR Series (7702, 1013, 1009, etc.)	Voice-Grade Private Line DDD	202D 202C	150 cps
	Voice-Grade Private Line DDD	201B 201A	300 cps 250 cps
TTY 15, 19, 28	5-Level TTY Circuit	— —	60, 66, 75, or 100 wpm
TTY 33, 35[5]	TWX TWX-CE Tel. Co. 150 Baud DDD	811B 103A 816 103A	100 wpm
TTY 33, 35, 37 Model 1	Voice-Grade Private Line W. U. 180 Baud	103F 1181.1A	100 wpm
UNIVAC 1004/DLT2	Voice-Grade Private Line DDD	201B 201A	300 cps 250 cps
UNIVAC 1004/DLT2B	Telpak A 48 KC Broad-Band Channel	301B	5100 cps
W.U. TELEX	W. U. Telex	W. U. Adapter	66 wpm

[1]Trademark of American Telephone and Telegraph Co.
[2]Trademark of Digitronics Corp.
[3]Trademark of Friden, Inc.
[4]This capability handled by single-line control only
[5]This capability handled by multiline control only



HONEYWELL REPORT ON DATA COMMUNICATION

THE COMPUTER

All Series 200 processors are program compatible. This and the fact that Series 200 encompasses a variety of input/output devices, all of which are available in many levels of capability, enable the user to tailor his system to the exact dimensions of his data communication job.

As an example of the Series 200's modularity, memory for the Model 200 starts at 4K characters and can be enlarged in 4K increments up to 32K and, from there, in increments of 8K up to 65K characters. Similarly, memory cycle times in the Series 200 start at 3 microseconds per character, then drop to 2, 1.5, 1, 188 nanoseconds, and 94 nanoseconds. Hence, the appropriate processor speed and memory size can be selected to meet both conventional and communication loads.

A unique input/output scheme and a hardware interrupt capability enable Series 200 systems to handle communications while *simultaneously* providing high production rates on conventional data processing applications. All Series 200 systems can handle multiple input/output data transfers simultaneously with computing; thus, they can send and receive messages over communication lines at the same time that input/output devices engaged in regular production runs are running at high speeds.

Series 200 also offers a wide range of peripheral capabilities for both real time and batched processing needs. There are 13 magnetic tape units ranging in data transfer rates from 7,200 characters per second to 96,000 characters per second. Honeywell's new Mass Memory File is available in three models, offering a range of on-line storage capacities up to 2.4 billion characters per control unit and random access times as low as 95 milliseconds. For faster access when storage requirements are less, a control/drum subsystem holding up to 20-million characters provides access to any record in an average time of 27.5 milliseconds.

A full complement of software is provided to handle communications for any type of application. This software includes those routines for interrupt handling, real-time input analysis, output stacking, random access storage, line utilization and determination of line availability, and data protection. All communication software may perform in conjunction with Series 200 Operating Systems.

MAKE YOUR OWN COMPARISON

The following table lists important characteristics in a data communication system. Honeywell's capabilities can be compared with those of any other system by filling in the appropriate data in the blank column provided.

Check List of Data Communication Features	Honeywell	Other
CENTRAL PROCESSOR		
Simultaneous production and communications?	Yes	______
I/O interrupt?	Yes	______
Memory protection features?	Yes	______
Program compatibility for backup?	Yes	______
Small-unit modularity?	Yes	______
INTERFACE		
Single- and multiline interfaces?	Yes	______
No. of lines per multiline interface?	Up to 63	______
Character and message modes?	Yes	______
Maximum line speeds: Single-line	5100 cps*	______
Multiline	300/7,000 cps	______
Gradually expandable line-handling capability?	Yes	______
Automatic switching for backup?	Yes	______
SOFTWARE		
Communication-handling routines for:		
Interrupt?	Yes	______
Real-time input analysis?	Yes	______
Output stacking and interfacing?	Yes	______
Random access storage and retrieval?	Yes	______
Line status?	Yes	______
Data protection?	Yes	______
Choice of operating system control?	Yes	______

*Higher speeds on special order

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ELECTRONIC DATA PROCESSING

DATA COMPRESSION

by hardware or software

by WARE MYERS, MICHAEL TOWNSEND and TIMOTHY TOWNSEND

Modern data acquisition systems are capable of producing digital data at high rates, in the tens, or even hundreds of thousands of samples per second. In logging applications, they are operated around the clock for weeks at a time. As a result, enormous volumes of digital data are obtained.

Data compression eliminates redundant data and retains useful data, simplifying the operations which follow digital data acquisition. These operations are recording, transmission, and data reduction, all expensive to various degrees. Also, each operation faces technical limits. For example, in the case of magnetic tape recording there is a limit, in the form of tape speed and packing density, to how much data can be recorded in real time. Transmission, especially over a great distance, is limited by bandwidth. Data reduction is limited by the capacity of the computer, and this limit is particularly pertinent in on-line installations.

Activities which may profit from the use of data compression include test operations, process control, and scientific experiments.

Test operations are of two kinds: relatively low-speed, long-term tests such as those performed in environmental and space-simulation chambers; and high-speed, short-run tests such as the firing of a rocket engine. Even in long-term tests, certain parameters may exhibit transient, high-frequency behavior at intervals, separated by long periods of inactivity.

In process control, it is common to log many parameters on a 24-hour-a-day basis. One problem results—what to do with all the data? If the data is compressed first and then logged, the volume of data which must be examined by the plant operators is greatly reduced. Chemical processes, petroleum refineries, steel mills, utilities, and dry-process plants may profit from data compression.

When experiments are conducted in space or other inaccessible locations, the telemetering of data back to the experimenter may be seriously restricted by bandwidth limitations. The compression of the data, prior to transmission, can greatly increase the proportion of useful data.

It should be noted that the quantity of samples taken cannot be reduced simply by sampling less often. The reason is that the sampling rate is directly related to the frequency of the analog signal. Sampling theory dictates that a signal must be sampled several times faster than the highest frequency component of interest. Thus, the sampling rate must accommodate the maximum frequency that is expected to occur on each signal during a run. Yet, as a matter of practical experience, it is known that many of the data sources in typical instrumentation systems remain quiet a good part of the time.

The periods of inactivity during which the signal is unchanged thus constitute unnecessary or *redundant* data. In general, this redundant data is eliminated by electronically comparing each successive data value with a criterion, rejecting those which fail, and recording or processing those which pass. The data which survives has been *compressed.* Compressed data can better meet the quantity limitations of transmission systems, recorders, and digital computers. Compressed data, too, can be processed through smaller, less expensive systems and can be handled in less time.

Before resorting to data compression, as described here, several other means to cope with excessive data should be utilized, if possible. For example, by careful analysis of engineering requirements, it may be possible to eliminate some measurements altogether. Subcommutation* may be employed when it is known that some data sources change slowly, compared to the average source. On the other hand, supercommuntation may be utilized on a few channels with higher-than-average frequency components.

If an on-line computer or special arithmetic circuits are employed, it may be possible to reduce a vast amount of data to a few "answers." This approach is particularly useful if the answers are to be transmitted over a narrow-band communication link, as would be the case in acquiring information from an interplanetary probe.

types of data compression

Two types of data compression may be distinguished: one where the criterion is a limit, and the other where the criterion is a tolerance. The idea of a limit is illustrated in Fig. 1. (p. 40) Each digital value is compared with an upper limit and a lower limit. If the sample is between the limits, it is discarded. If the sample exceeds the upper limit or falls below the lower limit, it is passed to storage. In the diagram, small circles indicate the significant samples.

The tolerance concept is illustrated in Fig. 2 (p. 40). Here the rule is: if a new digital value varies by more than a predetermined amount, or tolerance, from the last value, the new sample is significant and is passed to storage; if the difference is less than the tolerance, the new sample is not

Ware Myers is a writer-editor at SDS Data Systems, producing engineering bulletins to explain the operation of the company's digital data acquisition systems, and a part-time lecturer in engineering at UCLA. He has also been a systems engineer and supervisor of technical publications and has an engineering degree from Case Institute of Technology and MS in Administration from USC.

*This term and others that may be unfamiliar to readers are defined in a brief glossary at the end of this article.

passed. Small circles identify the samples which are out of tolerance. Note that the tolerance band is shifted each time a significant sample occurs.

These two diagrams show a single channel and a single value of the limits or the tolerance. When more than one channel is involved, it may be necessary to use different values of the limits or tolerance for different channels or groups of channels. For example, measurements using the same type of transducer and signal conditioning equipment may be compared against the same criterion, but measurements from different sensors may require a different criterion.

As the conditions of operation change, the location of the limits may be changed and the width of the tolerance

Fig. 1 Upper Limit—Lower Limit-Type Data Compressor

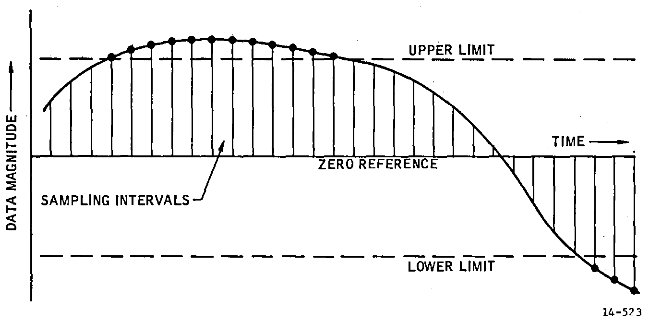
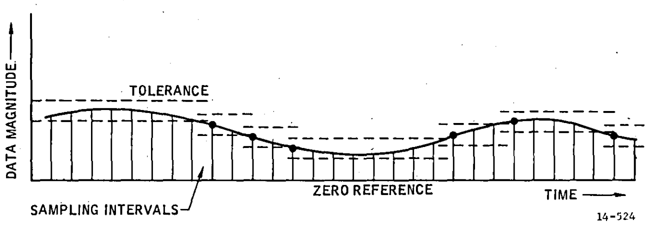


Fig. 2 Tolerance-Type Data Compressor



band may be varied. The source of change commands may be either the operator or an on-line computer.

Elapsed time may be used as a factor in the determination of redundancy. With this technique, the tolerance to be applied is continually decreased as the time elapsed between the last time a sample was recorded and the current instant increases.

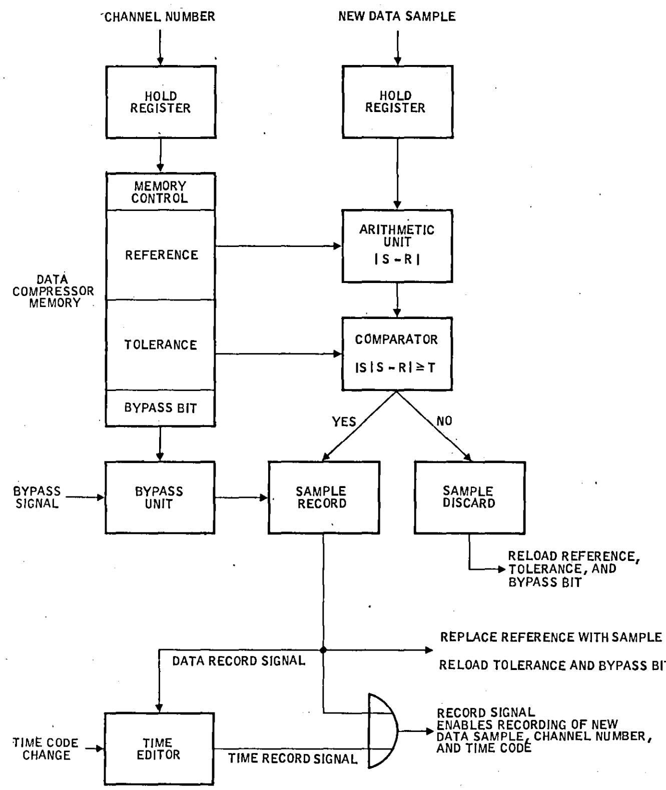
The limit concept may also be used for alarm purposes. In this application, the limits are usually set farther out than in data compression alone. When a sample falls outside these limits, the sample may be displayed and printed out, the printout may be flagged to call attention to it, and contact to an external alarm is activated.

implementation

A data compressor to implement the tolerance concept consists essentially of a memory, an arithmetic unit, a comparator, and logic circuits. The memory is used to store the last significant digital value—termed the reference value—and the tolerance. The arithmetic unit forms the absolute difference between the current sample value and the reference value. The comparator determines whether this difference is greater than or equal to the tolerance. From this comparison, the logic circuits either pass the current sample or discard it.

Implementation of the limits concept requires a memory, a decoding network, a limits storage-device, several comparators, and logic circuits. The memory is used to store—for each channel of the data system—an address which designates one of a number of pairs of limits, contained in the limits storage-device. The decoding network, given one of the addresses, selects one of the pairs of limits. This pair is applied to the comparators where the current sam-

Fig. 3 Simplified Block Diagram of Principles of Operation of Tolerance-Type Data Compressor



ple value is compared with the upper limit and the lower limit. If the sample falls outside the limits, the logic circuits pass the sample value.

It is evident that both types of data compression utilize a series of functions which may be found in a general-purpose digital computer or may be specially designed for a particular application from digital logic circuits.

hardware approach — tolerance method

To meet the requirements for processing data generated by the Mark I Aerospace Systems Environmental Cham-

Michael J. Townsend is an associate systems engineer in the Digital Systems Department of SDS Data Systems. He was responsible for the design of the 200,000-sample-per-second data compressor described in this article and was project engineer on the entire data processing system. He graduated from California Institute of Technology.

ber at Arnold Air Force Station, Tennessee, a high-speed data compressor was designed as part of the system. This unit is capable of receiving and compressing up to 200,000 digital samples per second on up to 1024 channels. Since the compression output rate is limited by the speed of the tape recorder to 3750 samples per second, the overall compression factor must average at least 53.1. In other words, for every significant data value recorded, at least 53 redundant readings must be discarded.

The data samples entering the data compressor (Fig. 3) have been commutated and digitized and are in parallel 11-bit binary form. Also entering the data compressor are channel numbers in binary form. At the beginning of the data-compression cycle, the channel number is applied to the channel-number hold register and the corresponding data sample is applied to the data-value hold register. The contents of the channel-number hold register are next applied to the address input of the data-compressor memory. This memory is a random-access device, and since the channel number is in binary form, one memory location is related to each channel number.

Stored in the data-compressor memory are three numbers, each in binary form. The *reference* number is the last significant data value. The *tolerance* determines whether the next sample value will be found to be significant. The *bypass* number, a single binary bit, simply provides a known condition, on or off, to be used for bypass purposes.

When the memory is interrogated at the location specified by the channel number, these three numbers—reference, tolerance, and bypass, appear in the memory's output registers. The reference value is applied to the arithmetic unit along with the present data value from the data-value hold register. The arithmetic unit forms the absolute binary difference—present sample value minus reference value.

This difference is applied to the comparator, along with the tolerance from memory. The comparator determines whether the difference is greater than or equal to the tolerance. If the sample is within the tolerance, the present data value is redundant and is discarded. The three numbers, reference, tolerance, and bypass, are then returned to memory and the data compressor waits for the next sample and channel number. If the difference is greater than or equal to the tolerance, the present data value is significant. Logic circuits act to replace the reference with the new sample value in memory, restore the tolerance to memory, and pass the present data value on to the recorder.

This series of actions constitutes the basic steps of data compression. Prior to a data run, however, the memory is programmed with the appropriate tolerances. Since each tolerance may range in size from zero to the maximum available to the data sample itself (that is, full scale), and since the resolution of the tolerance is the same as the data value, a tolerance can be found to specify any degree of redundancy. Also, since there is a position reserved in memory for each channel, each channel may therefore be assigned the tolerance appropriate to it and it only.

At the very beginning of a data run, there is, of course, no reference value stored in the data-compressor memory. One sample of each channel is passed, both to be placed in memory as reference and to be recorded on tape for data-reduction use.

The bypass signal is used to record a single sample from each channel periodically, regardless of the result of the comparisons. The bypass procedure enables the system to avoid long intervals with no samples. The bypass signal, selected by a rotary switch, is a clock signal. At the beginning of the selected time period, a transition occurs on the bypass line and triggers the recording process. Bypass time can be established at any intervals desired. In the present system, seven intervals were provided, ranging from five seconds to thirty minutes.

Bypass capability is also useful in checking the performance of the compressor since the bypassed readings may be compared to the edited readings. It is significant to note that the data compressor is not interrupted during the bypass. Both operations are carried on simultaneously. Furthermore, on operator command, the compressor may be set to bypass all data. Any particular channel may also be bypassed, in effect, by setting the tolerance at zero.

It is necessary for a data acquisition system to record time along with data samples, since the time at which the value occurred is itself a significant datum in subsequent data reduction. Yet, during periods of no data recording, time recording should be inhibited also. This is the function of the time editor.

The time editor accepts two logic inputs: the record signal, indicating that a new data value is ready to be recorded; and a time-code change signal. When both of these signals are present, the time editor emits a signal enabling the time code to be recorded on the output tape.

It is important to note that the data compressor passes samples on what may be termed a random basis. That is, different channels are passed through the data compressor on the basis of amplitude variations which are entirely unrelated to sampling rate or to scanning sequence. As a direct consequence, each data sample recorded must be fully identified, both by channel number and by time. Therefore, all of this information—data, channel, and time —must be accumulated and organized in a storage buffer.

If the data compressor passes information faster than the maximum recording rate, the buffer fills to capacity. It rejects further incoming data until data output provides space in the buffer. Recovery from this condition is automatic when the input rate decreases. All data recorded is valid; however, the rejected readings are lost for real-time consideration. In this system, however, a wideband analog recorder holds the analog signals and the rejected data can be recovered later.

If buffer fill occurs, the condition is indicated by a flag on the digital tape. The time of this flag can be used as a target to search the analog tape.

hardware approach — limits method

A design using upper and lower limits as the criteria of data compression is diagrammed in Fig. 4. As in the tolerance data compressor, the channel number and the new data sample, in binary form, are entered into hold registers. The contents of the channel-number hold register are applied to the address input of memory. Stored

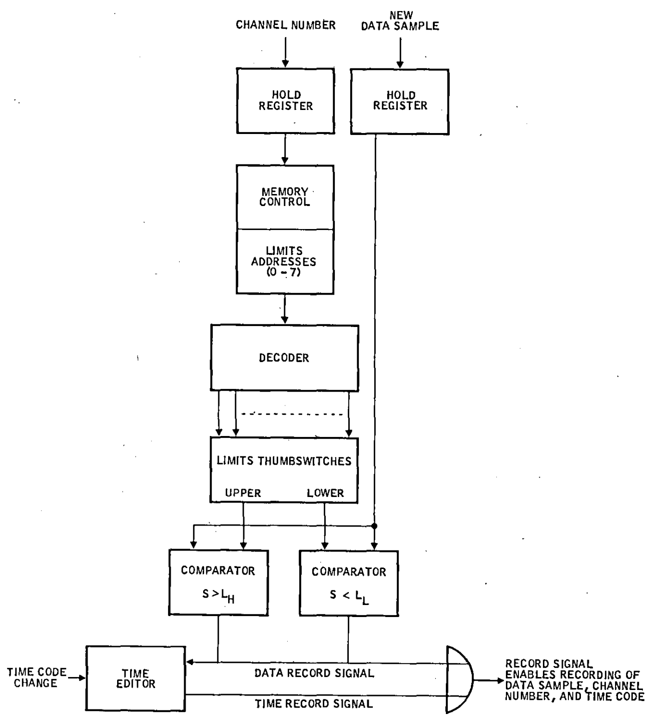
Timothy J. Townsend is a programmer in the Digital Systems Department of SDS Data Systems, with a recent assignment to data compression by computer programming. At UCLA he majored in mathematics, astronomy, and physics.

in memory is a single three-bit binary number for each channel. This number is the address of one of eight pairs of limits.

Each pair of limits originates in a pair of digital thumbwheel switches, located on a control panel. The digiswitches may be set at any decimal number within a four-digit range. Each of these eight low limits and eight high limits may be established at any value from minus full scale to plus full scale with the same resolution as the data sample. Although manual input to the digiswitches is in decimal digits, output is in binary form.

The binary outputs of the digiswitches selected by the three-bit address, representing high limit and low limit, are applied to two comparators. At the same time, the new data sample is entered into the comparators. If the sample exceeds the high limit or falls below the low limit, a data-record signal is produced by the corresponding comparator. This signal, together with the time-record signal

Fig. 4 Simplified Block Diagram of Principles of Operation of Limits-Type Data Compressor



(derived in the same way as in the tolerance data compressor), then produces a record signal which enables data sample, channel number, and time code to be recorded.

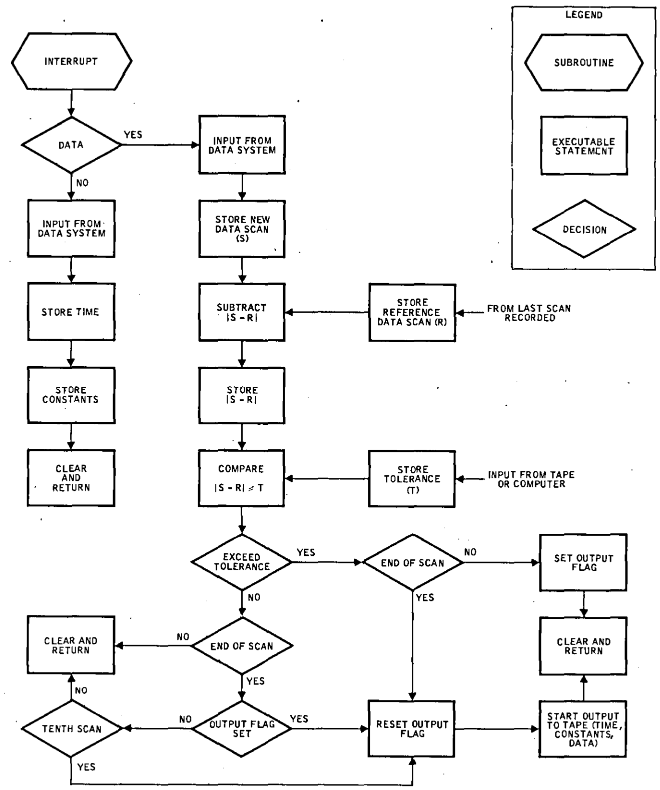
When the tolerance concept and the limits concept are both employed in the same application, the hold registers and memory can be used jointly, realizing some economies in hardware.

computer approach

The use of a digital computer on-line with a data acquisition system to compress data is demonstrated in a system built to instrument a months-long operational test of a nuclear reactor. This system accepts 500 channels but samples them at a fairly slow rate, one sample per channel per second. A program flow chart for data compression alone is contained in Fig. 5. In the actual system other functions—calibration, linearization, conversion to engineering units, alarm check, and diagnostic monitoring—are included in the complete program flow chart.

Referring to Fig. 5, the interrupt which begins this subroutine is given every four milliseconds by a time-of-day clock. The interrupt causes the computer to output in paral-

Fig. 5 Program Flow Chart for Data Compression



lel to the data system either two or three addresses, depending upon the cycling sequence. If the sequence is at the beginning of a new scan, the computer transfers three coded addresses calling for time, constant 1, and constant 2. These numbers are stored in memory, pending output to digital tape if the data value with which they are associated turns out to be significant.

Meantime, if the sequence is beyond the beginning of the scan, the computer transfers two coded addresses calling for data values from two channels. The choice of the data addresses is determined by the information supplied to the computer on paper tape by the operator during the initialization program. Two data values are transferred in parallel to the computer memory and placed in an input table. The first data scan, of course, is always recorded and is also stored in an output table in memory, identified on the flow chart as the reference data scan. Each data sample in the reference scan is subtracted from the corresponding data sample in each new data scan, forming the absolute difference.

This difference is compared with the tolerance values for each channel, also stored in memory. In this instance, the same tolerance value is used for all channels. If the difference falls outside the tolerance value, then the sample is significant. The computer tests for end-of-scan. If the sequence is at end-of-scan, the computer resets an output flag and starts outputting time, constants, and data for the entire scan from memory to digital tape. If the sequence is not at end-of-scan, the computer sets the output flag. On the other hand, if all the data samples are within tolerance at the end-of-scan, as revealed by whether the output flag is set, the computer tests for tenth scan. Every tenth scan is recorded even if all the data values in this scan are within tolerance.

The foregoing is a particular example of data compression by programming a general-purpose computer. General-purpose programming, of course, is highly flexible, permitting other variations of data compression to be easily programmed.

computer or special hardware

As we have seen, both special-purpose digital units and general-purpose computers may be used to accomplish data compression. In the examples given, a specially designed data compressor was employed to handle a very high sample rate—200,000 samples per second. On the other hand, when the sample rate was only 500 per second, data compression was performed by the on-line computer along with a number of other computational and logical functions. The question arises of when to use a computer and when to use a special unit.

For either approach, it is evident that there must be core-memory capacity (or the equivalent in some other form of high-speed memory) to hold the new digital samples, the reference samples, and the tolerances. There must be input registers and an output buyer to format the data for recording. The cost of memory for a special-purpose compressor and the cost of adding memory to an expandable computer memory are comparable. The cost of registers and buffers is similar in either case. The differential cost, in the case of the specially-designed unit, lies in arithmetic, comparator and logic circuits, and in system design. Excess cost, in the case of the computer, lies in features and capabilities not needed for data compression.

Now, if an on-line computer is going to be employed for other functions anyway, and if the computer will have time left in the computation cycle to perform data compression, then certainly it is economical to employ this computer for data compression. For example in the 500-sample-per-second system already referred to, an on-line SDS 910 computer was required to perform the following operations on two data samples every four milliseconds. The time required to process the two data samples, worst case, was estimated to be as follows:

Output two addresses to data system:	200 us
Input two data samples to computer memory:	200
Linearize, convert to engineering units, and alarm check:	1300
Set alarm contacts:	100
Format output table:	100
Data compression:	200
Typewriters and displays:	200
Write magnetic tape:	400
Total time:	2700 us

This processing time, 2700 microseconds, left 1300 microseconds in each computation cycle, an idle time of 32%. In this situation, it is apparent that data compression can be accomplished at no additional cost.

On the other hand, if the system sampling rate is very high, then an on-line computer may not have sufficient capacity to perform data compression in real time, let alone accomplish other functions as well. For example, if the system speed is 200,000 samples per second and data compression takes 100 microseconds per sample, the time to compress 200,000 samples would come to 20 seconds, far exceeding the one second available in real time. Thus, it is clear that data compression, at a sufficiently high sample rate, can be more economically performed by special-purpose equipment.

The 200,000-sample-per-second system employs both a computer (SDS 910) and special data-compression hardware. The computer controls many functions of the data compressor: it can modify tolerances; it can specify which channels are to be sent to the computer; and it can initiate bypass periods. Then, following these manipulations, the computer has time to reduce the compressed data on line.

In this system, the data compressor may be thought of as an extension of the power of the computer, particularly since the normal operation of the data compressor requires no computer time (other than input time for compressed data). So, in this sense, there is an argument, and an application, for both a computer and a hardware data compressor in a large-scale, high-speed data system.

In any proposed application, it is necessary to consider a number of factors before deciding which approach to pursue. What is the sample rate—which in turn depends upon the number of measurements and the frequency characteristics of the analog signals? What is the expected ratio of raw data to compressed data? How many bits precision are necessary? What on-line data reduction operations are required? What is the limiting rate of recording or transmission in the proposed system?

Once these design parameters are approximated, the capabilities of specific computers can be evaluated against the requirements. If available computers fall short, then data compression can be assigned to hard-wired equipment. With the program wired in, a data compressor can achieve a higher speed of operation than a general-purpose computer employing the same level of technology. In the intermediate area, where both approaches are technically possible, the decision rests on economic factors.

DEFINITION OF TERMS

Bypass: a secondary channel permitting a data sample to be routed around the data compressor, regardless of the sample's value, at intervals selected by the operator.

Comparator: an electronic circuit which compares the absolute difference (between the current data sample and the last sample passed) with a redundancy criterion (which may be a tolerance or a limit), and determines whether this difference is greater than, or equal to, the criterion.

Data Compression: the process of reducing the number of digital data samples, which are recorded or transmitted, by excluding redundant samples.

Decoding Network: an electronic circuit which, when a particular combination of inputs is on, produces an output on one of a number of output lines.

Initialization: the process of supplying information (memory locations for data and results, tolerances, limits, etc.) to a computer prior to running a program.

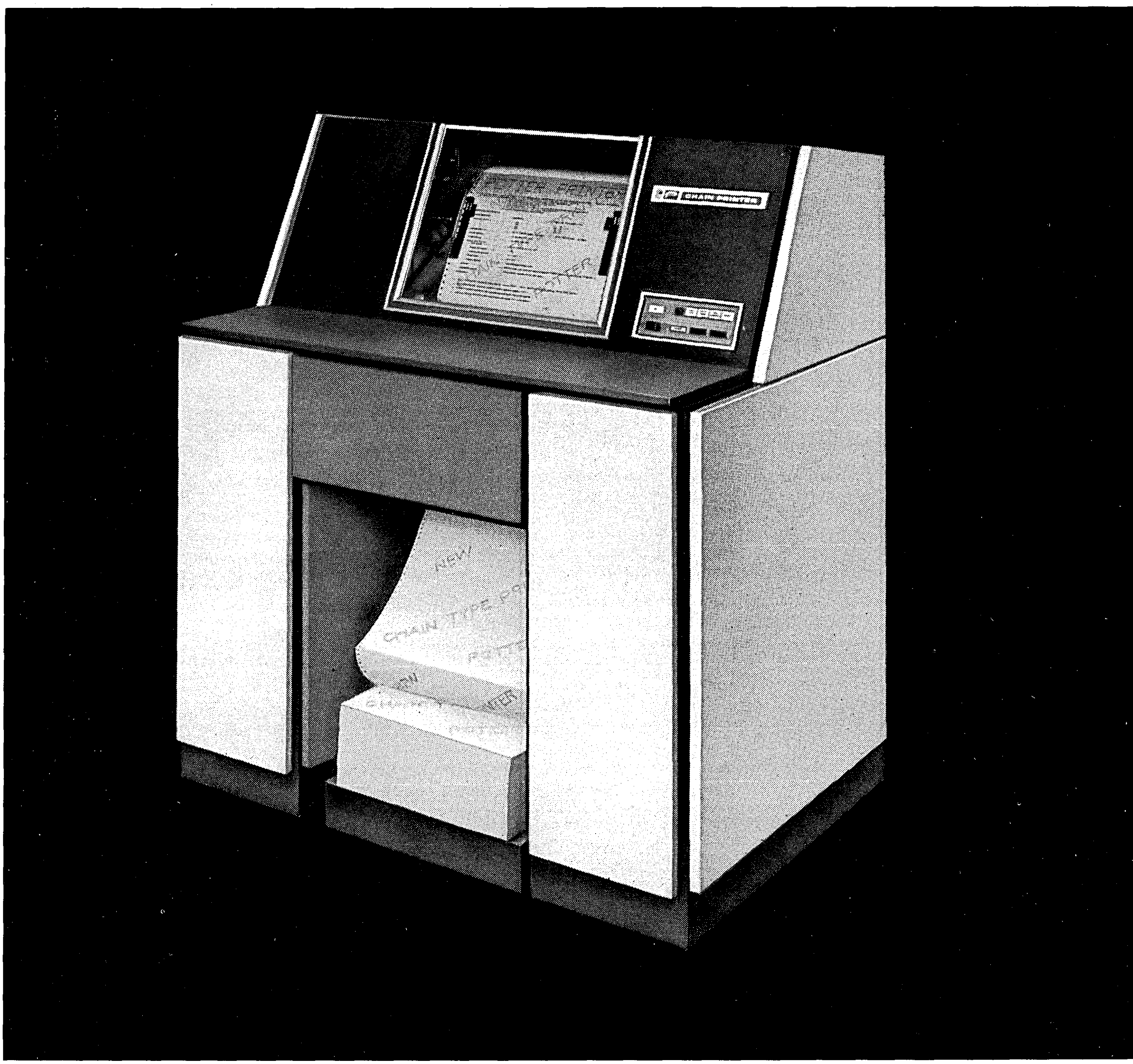
Redundant Data: a data sample close enough in value to the preceding sample from the same source as to be of no interest in connection with subsequent analysis of the experiment or test, except the fact that the data sample is redundant.

Sampling Theory: the sampling theorem (developed by Nyquist in 1928) states that two samples per cycle will completely characterize a band-limited signal; that is, the sampling rate must be twice the highest frequency component. In practice, the sampling rate is ordinarily from five to ten times the highest frequency.

Subcommutation: the act of connecting one data source to a sampled-data system less frequently than other data sources.

Supercommutation: the act of connecting one data source to a sampled-data system more frequently than other data sources.

Time Edit: to exclude the time code from being recorded or transmitted during periods when data samples are not being passed; or conversely, to record or transmit the time code with each data sample passed. ■



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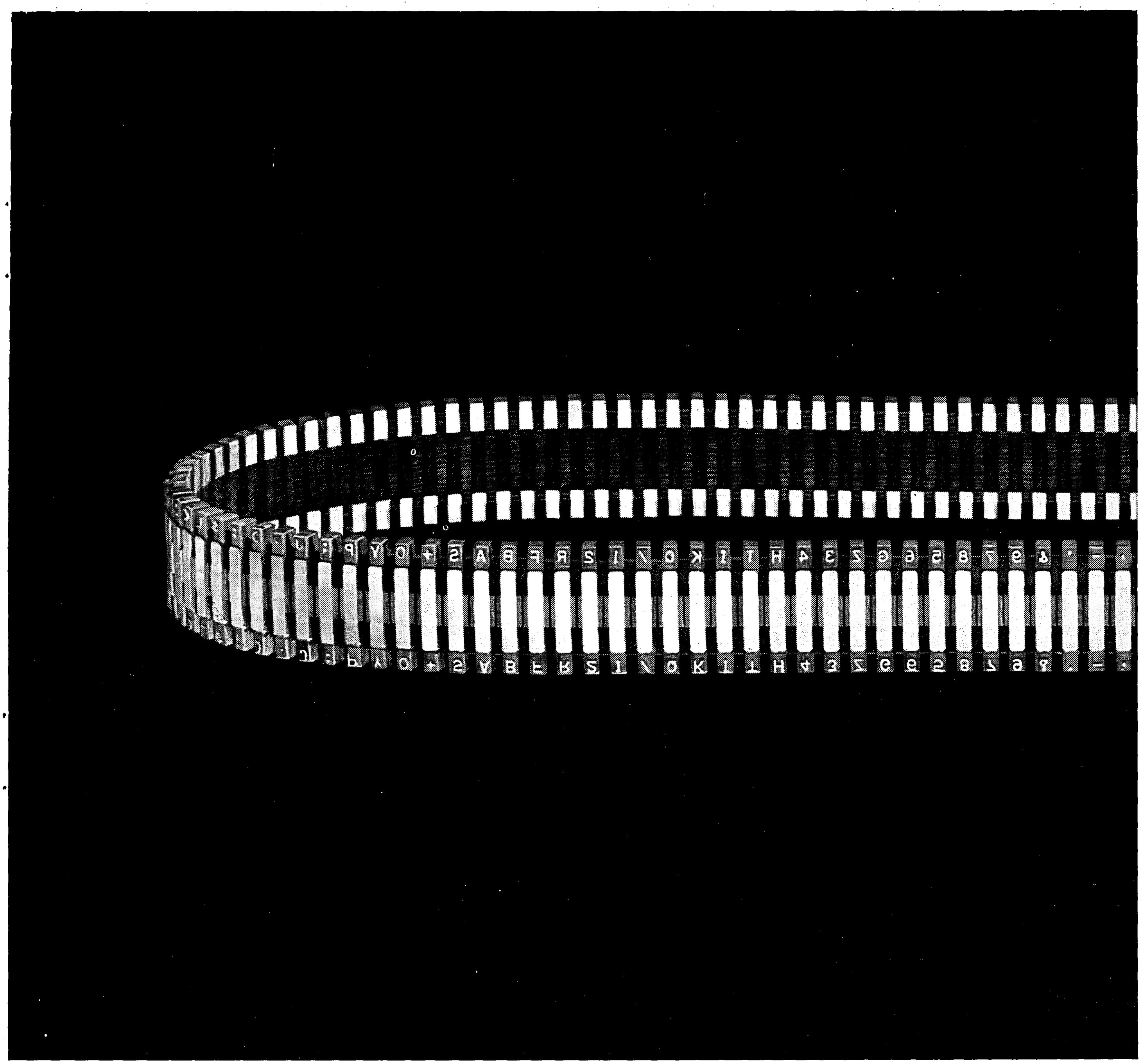

ON-LINE BRANCH BANKING

by ELMER C. MIETHANER

Why install an on-line data processing system? At Western Savings, we heard criticism that ranged from the naive to the philosophical position that on-line teller systems could not be justified in terms of speed. Today's on-line systems are sophisticated and reliable. We believe that the philosophical critics have failed to take into account that speed, or time-saving, is not just a matter of cost per hour. At our bank, as at many others, there is also the nebulous but vital consideration of customer service.

In our system and other on-line installations the computer is always aware of the current status of every account. This means not only speed and better customer service, but electronic control as well. Any depositor can come to any window at any branch and complete a transaction in seconds, without delay or error. Accumulated interest and "no-book" transactions are entered in his passbook automatically.

Western Savings was the first bank to initiate service with an on-line NCR 315 system, beginning March 27, 1964. Since then, the time required to process a typical transaction has been cut by 25%. Again, this time is more important to the customer than it is to the bank; lines seldom form, and when they do, they are short. We make no more telephone calls and no reference to ledger files while the customer stands and waits.

equipment

The teller's machine used in the system is the NCR 42-501, incorporating alphabetic display indicators and an audit tape printer for communication with the teller. The basic machine was designed by bankers for banking requirements, and can operate very satisfactorily without any computer connection. Posting-print speed is 40 characters per second.

The teller's machines are linked through a single cable to a remote controller in the same office (controller capacity: 16 teller's machines). The controller recognizes an active window machine, generates accuracy checks on input and analyzes the validity of all data transmissions on output. We are currently using 15 machines in our main office and two branches.

Signals are adapted for transmission over full duplex telephone lines using Dataphone subsets. The use of these lines reduces data communication (turnaround) time and increases the throughput of each transaction. The data flows between the teller's console and the computer at the rate of 2,000 bits (1,500 bits out) per second.

To send the messages over the voice line, the controller converts the bits from parallel to serial mode. When receiving, the conversion is from serial to parallel mode. A parity bit is generated and validated on each character and a longitudinal bit sum check is performed on each segment sent to and received from the processing facility.

The controller scans each line at the rate of 500 microseconds per line (each window machine can be scanned up to 7,500 times per minute). Upon recognition of transmission failure, the controller independently and automatically attempts three retransmissions before alerting the teller of any communication difficulties.

On returning output messages from the computer, the controller analyzes routing codes, and channels the data to the appropriate window machines.

The 315, located one floor above our main office, has a 10K memory and three CRAM units, served by a central buffer connected to the remote controllers. Input lines are continuously scanned for data. When a message is in buffer, the processor is signaled and the message is taken into memory. Similarly, when the processor has data for a remote location, the data is placed into the buffer, and the processor is released. An unbuffered printer and a card reader complete the system.

on-line processing

Approximately 110,000 accounts are spread over 308 CRAM cards in two separate decks, called the on-line balance file. After an incoming transaction is validated, the appropriate CRAM record is selected, and a teller audit performed. The on-line balance file is updated, and the transaction is assigned a chronological sequence number and stored. Control totals are also maintained.

Window transactions are proved by stripping the transactions from the on-line balance file at the end of the day. A new balance file is written for tomorrow's on-line processing. The daily transactions are then sorted to chronological order by window machine for comparison with the window machine proof run. After proof, this file is sorted to account number sequence prior to reformating for further processing.

The window machine proof run accumulates and balances teller totals, listing them only if an out-of-balance condition exists. This list is then compared with the computer's detail chronological transaction list.

software philosophy

On-line systems in general are similar in mechanics and cost. In choosing our system, we were particularly im-

Mr. Miethaner is comptroller of Western Savings Bank, Buffalo, N.Y., and is responsible for the institution's methods, systems and procedures, and accounting department operations. A past president of the Niagara Frontier chapter of the Institute of Internal Auditors, he has also served on the board of the American Institute of Banking and is currently president of the local chapter of the National Assn. of Bank Auditors & Comptrollers.

pressed with the philosophy of software packages applied to the system. We believe that the design and sophistication of these packages provides, in the first place, the same performance and efficiency for the small user as for the large user, and, in the second place, unique flexibility.

The program has been designed in two sub-packages, an executive package and an application package. The former includes all hardware oriented and communication functions, while the latter is concerned with the updating of accounts, processing of transactions, control of holds, and other general bank functions.

This division places functions that will generally remain fixed in the executive package, and functions related to institution policy in the application package. If the user should desire to implement certain operations in a different fashion, the programmers need to concern themselves only with the application package. Areas where changes might be desired have been anticipated, and the package is designed so that many changes can be implemented within the logical structure provided.

data communications

The executive package in general covers all peripheral unit communication, including all reading of the inquiry buffer, input message assembly, output message control, retry situations, all CRAM read and write, account number look-up, and console typewriter communications. In addition to the symbolic code for the application, the variable information for the executive is specified. A separate program generates autocoding based on these specifications.

Messages from window machines are received in segments (usually two or three segments per message) which must be stored and chained together. The general message area accommodates four categories of data: input messages, output messages, CRAM cards waiting to drop, and available spaces. This area consists of a number of six-slab segments. Each unit of data (a complete input or output message) consists of some number of segments associated by a chain slab (high order one of the six). Each segment of the unit directs us to the next segment (if any) via this chain slab. Available space is considered a single item and its segments are similarly chained.

An active window machine directs us to its associated message via the relative address slab of its file table entry. As segments are added to messages during input, the amount of storage increases and the available space decreases. When segments are no longer needed as is the case when outputting, and are deleted from storage, the amount of storage used decreases and the available space increases.

The executive package assembles messages as the segments arrive. When a complete message is received (indicated by the receipt of the account number), the CRAM will be accessed, the account found, and control is turned over to the application package.

Output is delivered to the executive package in blocks of complete edited segments, which are sent to the window machine. When multiple segments are transmitted to a single window machine, other data can be either sent or received between segments, so that a heavy load on one machine does not reflect on the rest of the system.

Balance file records are variable in length, providing for expansion or contraction of the record number of slabs as provided by the executive package. The application package edits the desired items to be inserted or deleted as indicated by the processing. This information is communicated to the executive package by means of the length slab and an index register. Insertion or deletion is done at the end of the record.

The transaction file is on the same CRAM track as the balance file. As each transaction is created, it is recorded at the end of the balance file track on which its respective balance file record is located. The application package assigns a serial number to each transaction so that the chronological sequence may be determined for later audit trails.

If a given track becomes full (as a result of new accounts or no-book operation), the adjacent track is utilized. Where the immediately adjacent track is also full, the next track is utilized, and so on. Transaction overflow is to the pure transaction file.

Totals from each window machine are recorded on a separate card reserved for data not related to a given account. This area, the pure transaction file, is also used for teller checks and money orders.

typical transaction

When the teller machine is connected to the 315 and ready to process transactions, the indicators read ON LINE and READY. To process a transaction, the depositor fills out a deposit or withdrawal slip and presents it with his passbook to a teller. If necessary, the teller can compare the signature by placing the passbook under the machine's black light, revealing the passbook's invisible signature.

The teller then enters the old balance from the passbook, the amount and type of transaction from the slip, and the depositor's account number. The indicator lights now read PARTIAL MESSAGE until the account number (always the last item) is entered. The information is transferred through telephone lines to the 315, which checks it for accuracy.

The computer usually processes the transaction in less than a second, while the PROCESSOR CONTROL light is lit. The 315 updates its CRAM records, and transmits the posting information. As the teller machine makes the updating entries, the ON LINE and READY lights go on again.

Other signals on the teller machines include OFF LINE, ENTRY ERROR (error in information entered by teller; for example, balance and account number do not agree with what is stored in the computer), SEND ERROR, RECEIVE ERROR, REFER (teller to review printed audit tape), ERROR UPDATE and OVERDRAFT. The ERROR UPDATE signal, informing the teller that the computer is correcting an error that was discovered after the last transaction on the account was processed, is reinforced by an audio signal. Usually, the bank sends a letter to the depositor informing him of the discovered error. When the teller returns his passbook, he points out that the error has been corrected.

A bank may select any six messages for the bottom screen of indicators on the machines, and may also define the conditions under which the computer will turn them on. We chose two, HOLD and UNCOLLECT. HOLD indicates that a withdrawal violates a hold condition on the account. UNCOLLECT indicates a withdrawal includes funds currently in float. In each hold condition, the computer locks the teller's console until the appropriate action is taken.

If messages conveyed by the indicators need amplification, the 315 provides more detailed information by causing the journal tape printer to print a code number visible to the teller. Each teller has a chart of code definitions for reference.

The system enables the bank to establish three levels of override on conditions that may arise in processing transactions. At the lowest level, the teller may depress the "override" key. The intermediate level requires supervisor intervention. At the highest level the system will not accept the transaction, and it must be referred to an officer of the bank.

Control and accuracy are assured during all transactions, since account number and old balance pickups are checked, holds are enforced, and input format is standardized. The computer maintains a positive float control, and enforces the printing of no-book and interest to the passbook prior to printing the current transaction. All necessary audit trails are prepared at the same time that the on-line file is updated, and teller balancing totals are accumulated by both the computer and the teller's machine.

account inquiry

The teller's console can be used to query the computer files. Indexing an account number on the machine, a teller can interrogate the 315 and receive a printout of account number, holds, date of last transaction, passbook balance, current balance, available balance, and amount in float, as a convenience to depositors. The teller may also inquire as to the number of checks in float, and the number of days in float for each.

The system assures that computer records and passbook are in agreement. The teller is able to operate without leaving the window, even for signature verification, and errors caused by incorrect account numbers and incorrect old balance pickups are automatically detected and prohibited. The computer monitors every teller operation.

One of the primary control features of the system is that a complete audit trail is established at the point of original entry for all input-output transactions. Stops, holds, and uncollected funds are automatically under supervisory control, and dormant or inactive accounts are kept in strict control.

Customer convenience is increased by the ability to handle transactions at any window of any branch, and the tellers' machines provide complete validation on deposit or withdrawal slip as well as printing the passbook and audit trail, simultaneously, and in original print. These abilities are available on- or off-line.

off-line processing

In daily off-line processing, a series of programs organize the information accumulated during the day. Reformated transactions in account number sequence are combined with sorted adjustments, net deposits, withdrawals and corrections to update a master account file with today's transactions, and create a daily journal file printout. Intermediate steps in this processing include creation of a sorted adjustments file, a combined transaction file, and a net transaction file. The computation of net transaction not only simplifies interest computation, but also permits the depositor to withdraw and redeposit money on the same day without sacrificing interest. Printouts include an adjustment list of totals, a daily transaction list, and a transfers from list.

In the second run, the computer updates the off-line master file by incorporating the one net transaction on each active account. This master is more than a complete version of the on-line file, which includes only information for processing and describing current status.

As another result of the updating run, the bank gets new control figures by branch and by date, a total on the interest credited for the year to date, and the anticipated interest for the current quarter.

The daily journal file is combined with the payroll savings bond issue list and recap, and a new listing and recap is printed. The daily journal is also printed, listing net transactions on all active accounts. This list provides the account numbers in sequence; the date of the previous transaction (to provide an audit trail), the type of net transaction, the net transaction amount, and the post-transaction balance.

The daily journal listing also provides group totals including the number of new accounts opened during the day, the total amount deposited in the new accounts, the number of transfer accounts, the number of accounts closed, and the total amount withdrawn from the closed accounts. It lists for each branch the total deposits, total withdrawals, the total of all open accounts and the loss or gain for the day.

Weekly, monthly, and quarterly transaction files are also created and printed when necessary. Interest is posted quarterly to the master account file, creating an interest transaction file and simultaneously calculating new anticipated interest. The on-line balance file is updated from the interest transaction file. A yearly closed account file is also created and held for year-end reporting.

Year-end tax reporting programs provide for combining the master account file with a name and address file, and printing 1099's for active and closed accounts. Interest is also cleared for the year to date from the master account records to create a new master account file for the new year's first off-line processing run.

In the near future, we expect to extend programming to include 19,000 mortgages. Home improvement loans are now on the computer.

Our experience with the teller machines in the system has shown that the depositor usually leaves the window within one minute after his arrival. The average savings transaction, including passbook posting, takes four seconds on-line. If the entire system is to be justified with respect to customer service alone, disregarding the system advantages to the bank, its cost would represent about one dollar per account per year at present. Naturally, we expect our accounts to grow, but even at the present figures, we consider the cost to be justifiable and the convenience vital.

We did not have to develop a new account numbering system or add a check digit. Even the most accurate check-digit systems are only about 90% dependable, but by requiring that the account number and the passbook balance entered by the teller agree with the same information stored in memory, our on-line system reduces the possibility of error to a small fraction of 1%. Because the account numbers have not changed, our depositors continue to use their old passbooks.

In event of a line breakdown or other trouble, the tellers simply process the transactions off-line, as they did before their window machines were connected to a computer. When the system is back on the air, the tellers re-enter any off-line transactions at their convenience from the journal tapes. In our experience, down time has been only about 1% per year. NCR provides full back-up for the system.

We have found that the teller's job at the end of the day has been reduced to clearing the machine and counting the cash. The tellers usually leave within a half hour after closing.

Because the period between installation and system startup was short, tellers at our Delaware Park office had an average of two hours training before processing live work. Nevertheless, the transition posed no problems. We found that two tellers can easily share a machine. We are currently using four on-line machines for six windows in each office. Between March and June, tellers from the other offices were assigned for a day or so to Delaware Park for training on actual work. ■

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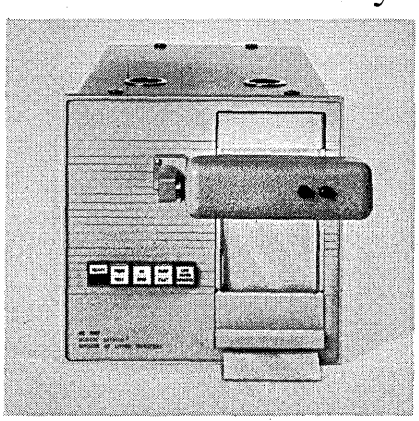

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TIME-SHARING IN BIOMEDICAL RESEARCH

by T. ALLAN PRYOR and HOMER R. WARNER

The computer is fast becoming a useful tool for biomedical research. With this tool, as with others before it, potential users have the right to ask: how will it do my job better and how much will it cost? With these questions in mind the computer system to be described was developed to increase the ease with which certain kinds of biomedical research can be performed and minimize the cost and time for both the investigator and computer.

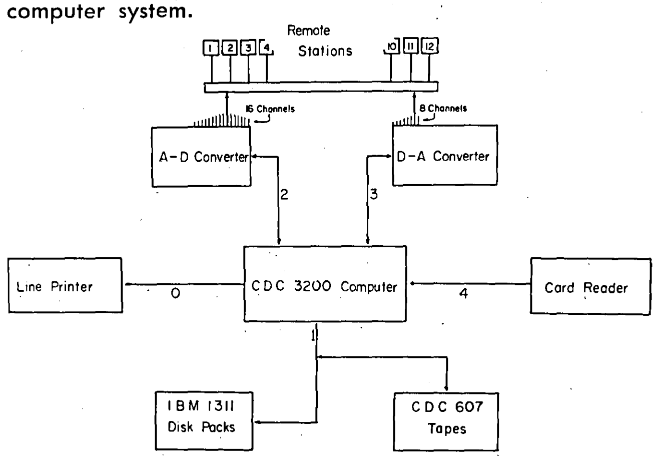
Some specific problems which arise in applying computers to biomedical research are: 1) the need for sampling of biological data over extended periods of time or sampling at very high rates for short intervals, 2) the separation of computer and experimental site, and 3) the need for continual rewriting of research programs as the form of the experiment is changed to accommodate a change in the mathematical model of the biological system. To solve these problems most efficiently a multiple remote station system has been developed. Each station can communicate with a central processor and is able to run experiments in conjunction with one to six other stations, one of which is the card reader and printer at the central processor. The system can process data from several experiments simultaneously as well as perform the more routine card and tape oriented data processing and computing. In most cases the monitoring of experiments takes relatively little computer time from the more conventional computer processing. A time-sharing monitor has been written to accomplish this. The hardware and software of the system, along with several applications, are described in this paper.

Fig. 1 is a diagram of the computer system at the Latter-day Saints Hospital. The system consists of a CDC 3200 computer with five I/O channels and 32,768 24-bit words of memory, and the following peripheral equipment: a high speed line printer connected to computer I/O channel 0, three tape drives and two IBM 1311 disc pack units on channel 1, an analog-to-digital converter connected to channel 2, a digital-to-analog converter on channel 3 and a 1200-card-per-minute card reader on channel 4. Channel assignment was based on job function in order to keep the channels as independent from each other as possible for maximal efficiency of the buffered I/O during simultaneous use of these peripheral devices. An analog computer is available for hybrid computations. It is connected to the central processor using one or more of the analog-to-digital, digital-to-analog channels.

conversion equipment

The analog-to-digital (A-to-D) converter is an 8-bit unit with a maximum conversion rate of 100,000 samples per second. At present there are 16 analog input channels and 16 digital input channels. The digital inputs are 12-bit binary words which are gated directly into the computer. Selection of the analog or digital channel to be used for a particular program is under program control. Various modes of operation are available to the programmer in-

Fig. 1 Block diagram of Latter-day Saints Hospital real-time computer system.



Mr. Pryor received his BS from Long Beach State College and his MS from the University of Utah. He is presently systems director of the digital computer facility at the Latter-day Saints Hospital and assistant research professor of the Department of Biophysics and Bioengineering at the Univ. of Utah.

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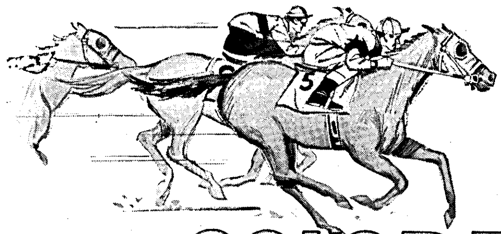

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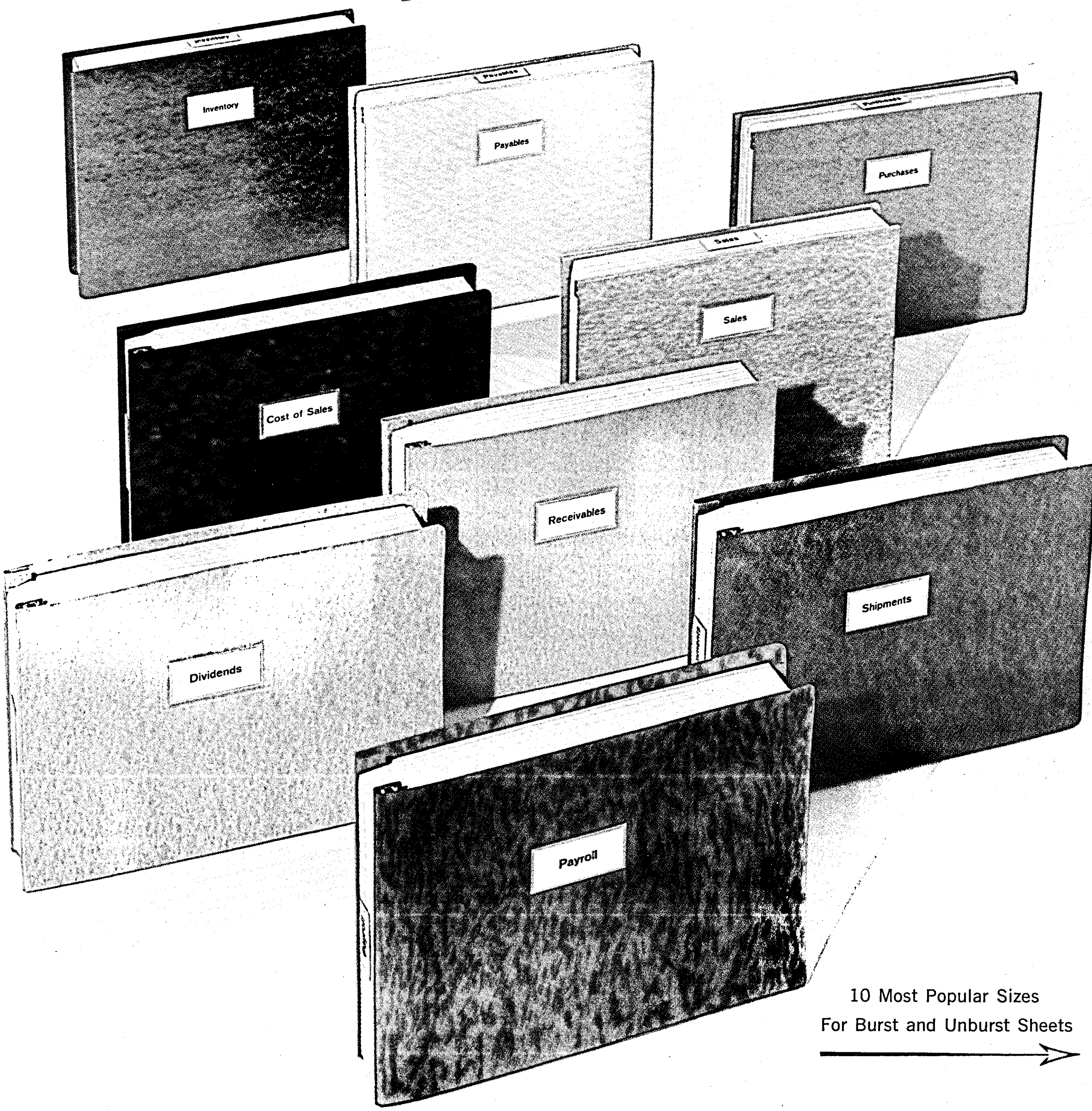

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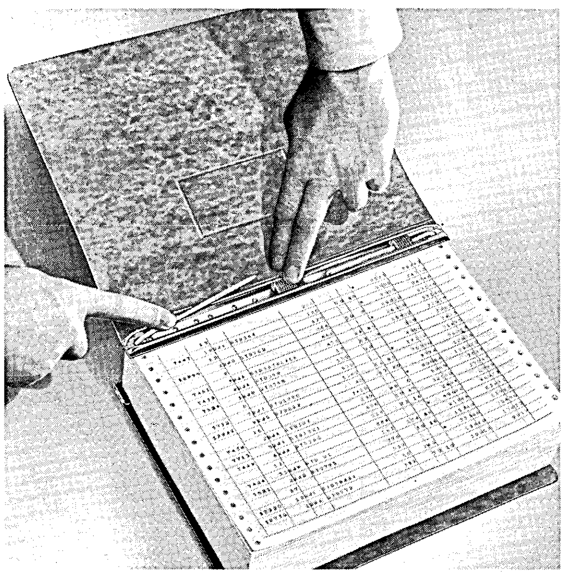

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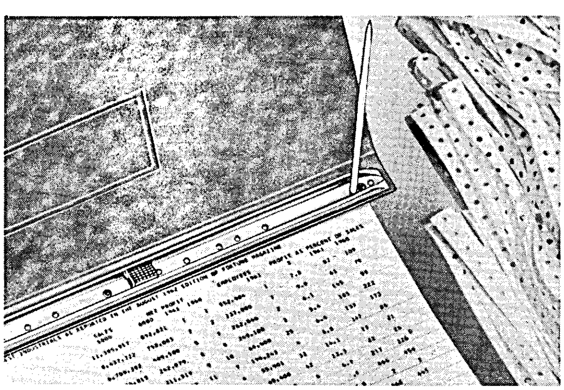

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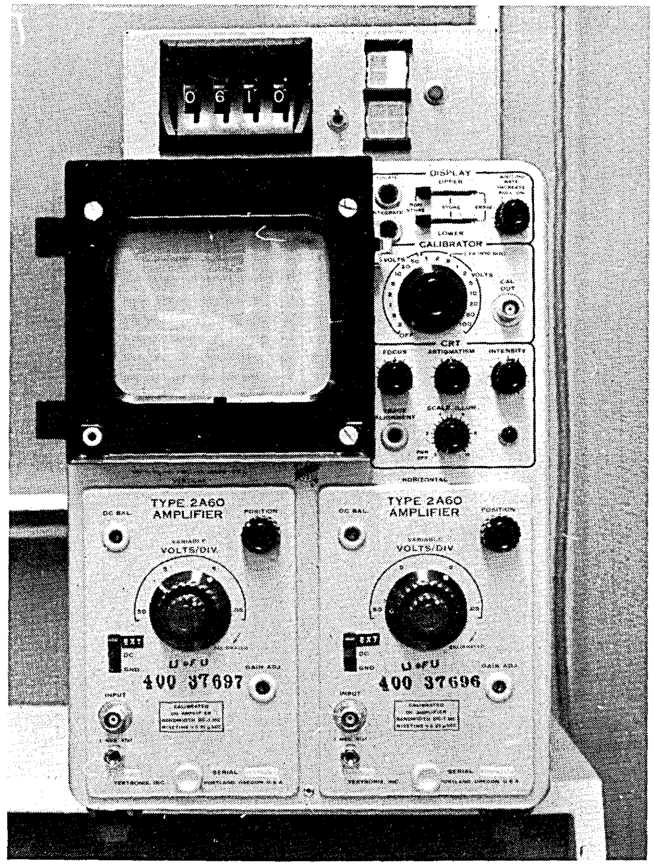
cluding interrupt modes which allow the A-to-D converter to send to the computer an external interrupt when data is ready to be transferred to the computer. Sampling rates of the A-to-D converter can be controlled both internally by the computer or externally through a pulse or sine wave fed directly to the A-to-D converter. In this external sync mode, data will be transferred to the computer only when the A-to-D converter is ready and some other external sync pulse has been supplied. There is also a hold-off feature which restricts sampling and transferring of data from the converter into the computer until an external hold-off pulse has been received by the A-to-D converter. After this pulse has been received, the converter will transfer data in either the internal or external sync mode. Connected with each digital input channel is a four-digit thumbwheel octal switch through which an operator is able to transfer digital information to the computer.

The digital-to-analog (D-to-A) converter has a maximum rate of 100,000 conversions per second and will convert the low-order 8 bits of a 12-bit digital word to an analog voltage varying between 0 and +10 volts. The present system consists of eight analog channels connected to the D-to-A converter. The first two of these channels are hard-wired directly into six Tektronix memory scopes located in the different laboratories. All information displayed on these scopes comes via these two analog channels. The erasing and blanking of any scope is controlled by the program through the use of three banks of relays available on the D-to-A converter. Thus, although data is transferred to all the memory scopes, it will, by use of the relays to control blanking, be visible only on the particular scope whose station has requested the information. The relays not only control the erasing and blanking of the scopes but also control the internal and external sync modes of both converters.

The investigator communicates with the computer through remote stations. Each of these (see Fig. 2) consists of a computer interrupt push button, a digital input dial, a memory scope, and eight small indicator lights. These lights indicate the status of the computer, i.e. which areas of core memory contain active programs and the priority of programs in core or waiting on disc to be run. By pressing the interrupt button with an appropriate code word in the digital input dial, the investigator may request his program be brought into memory. Once in memory the program normally writes on the scope in the laboratory of the investigator the sequence he is to follow. Subsequent interrupts from his station then allow him to communicate with his program and to start and stop the flow of information through the converters.

At locations remote from the hospital the data is transferred to the central processing area via telephone lines.

Fig. 2 A remote station consisting of memory oscilloscope, octal switch, indicator lights and interrupt button.

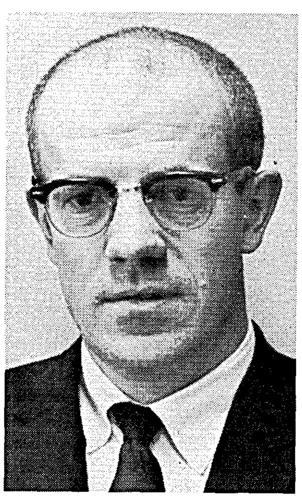


Here the investigator, instead of feeding his data directly into the A-to-D converter, feeds his analog data into the voltage controlled oscillators and a frequency multiplexer. The FM carriers are then transmitted via a private telephone line to the central processing location. Here the FM signals are demodulated and fed into the A-to-D converter for input into the computer. The results of the experiment are in turn relayed back to him using a similar system over another telephone line.

basic programs

Because an investigator may need repeated access to the computer during a long experiment, a monitor program has been developed to control the use of the computer and allow simultaneous experimentation from more than one remote station. Programs written to communicate with the remote stations are written in assembly language. These programs may, however, act as subroutines for a FORTRAN program. Where extensive computation is required on the real-time data, the computational portion of the program is written in FORTRAN and the communication with the A-to-D, D-to-A and remote stations in assembly language.

All user programs are stored on one of the disc packs. When a program is requested, the monitor brings it into core for execution. Through a program priority system, it is possible for one program to be interrupted during execution and another program of higher priority to be initiated. At this time the program of lower priority is



Dr. Warner received his MD from the University of Utah and Ph.D. in physiology from the Univ. of Minnesota. He is presently director of the Cardiovascular Laboratory at the Latter-day Saints Hospital and professor and chairman of the Department of Biophysics and Bioengineering at the Univ. of Utah.

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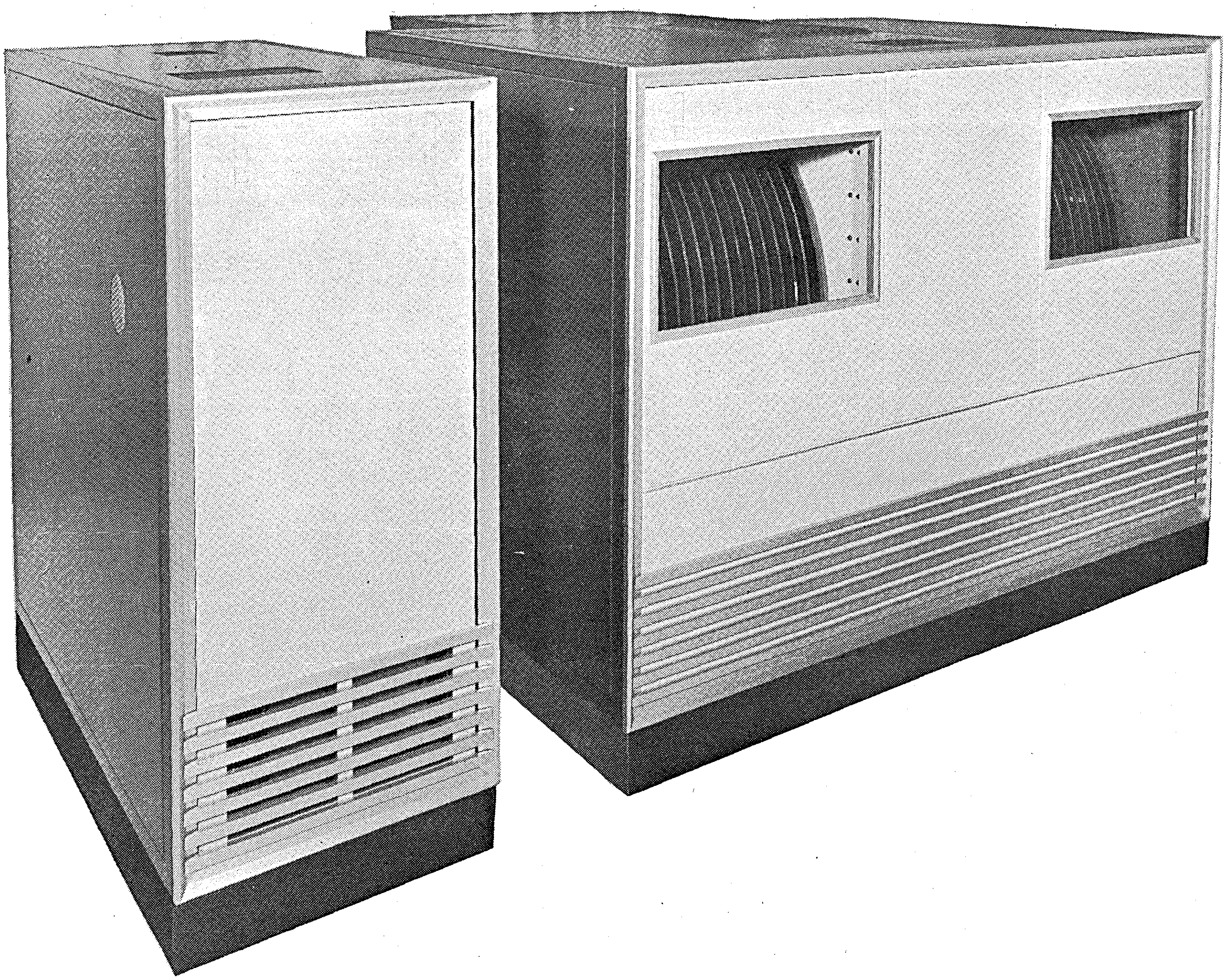


stored in a temporary area on disc to be completed later.

A central print driver has been written to prevent the printed results of one program from being intermixed with another on the line printer. Output from every program, as well as compiled listings, is placed on the disc. At the end of execution of a given program the monitor initiates the disc-to-print program, which then prints in an interrupt mode the entire results of that program. After completion of one print job, the system looks to see if other programs have been completed and require some listing. If so, it initiates the listing of that program. Only FORTRAN programs are allowed to have printed output. The output of the assembly language programs will be to the scopes.

Access to the disc is via a central disc driver. This is to eliminate the moving of the disc arms by many programs causing a loss of data.

Programs written in FORTRAN are compiled into the lower 16K of core. Since they require so much core even for a relatively short program, a priority scheme was developed to use this portion of core most effectively. Priority three was given to FORTRAN-compiled programs which require more than five minutes to run while priority two programs run in less than five minutes. A FORTRAN-compiled program is priority one if it is linked with upper core to one of the assembly language programs. These require highest priority since they use data in real-time from some experiment in progress. This option requires that the program be accessible to the investigator within two seconds in order to insure no loss of data. Although these programs are of highest priority they are swapped on the disc during times of no activity from the station using the high priority program.

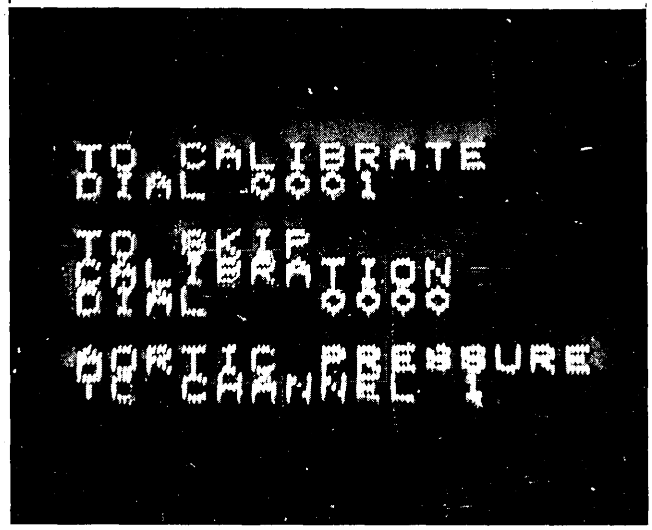
Above this first 16K area the next 12K is set aside for assembly language programs which handle real-time data from the laboratories. These programs are designated real-time programs. These programs are relocatable in this area and upon execution are brought into some part of this 12K area. They remain in core, however, until the experiment is finished or the investigator sends an appropriate code to the computer. All programs in this area are called from the remote stations by depressing the interrupt button after dialing 7XXX in the octal switch, where XXX is the program number. The monitor interprets this as the beginning of program XXX, reads it from the disc into memory and transfers control to the program.

Again, the main function of these upper core programs is to communicate with the experimenter and do the actual transferring of data to and from the computer. For example, these programs may write a control message on a memory scope (Fig. 3) to tell the experimenter to connect his input to certain analog channels or to specify a program option desired. Upon completing these functions the experimenter then presses the interrupt button telling the computer that he has performed the function and is ready to proceed with his experiment. This two-way communication proceeds with the operator controlling the flow of information from the experiment to the computer and the computer asking for data and options in the proper sequence and finally displaying results on the oscilloscope as alphanumeric characters and/or graphs. A more detailed description of several of the programs will be given further on in the paper. The monitor can control A-to-D and D-to-A operations for six such programs in memory at any one time.

The upper 4K words of memory contains the monitor and several special-purpose subroutines which are accessed by all of the real-time programs. One such program is the subroutine to write alphanumeric information on a scope.

Multiplexing between the programs in memory may take place as a result of an interrupt from a remote station or from the real-time clock within the computer. The clock interrupts are normally used to control sampling rates. Each program specifies to the monitor the desired interval between successive samples of its analog input/-output. This interval is added to the reading of a 10KC internal clock and placed in an interrupt mask table to switch control to that program when the next sample is

Fig. 3 A message written on a memory oscilloscope giving procedural instructions to the user.



due. If in any program there is a time delay for operator intervention or for the next sample to be ready, control is returned to the monitor which then tests whether there are other programs to be serviced.

transfer interrupts

Since each of the real-time programs generates so many interrupts requesting that control be transferred to its program, it has been found that there need be no scheduled cycling through the programs by the monitor. The only program not generating interrupts is the FORTRAN program in the lower 16K; but since only one such program is allowed to be executed at any time there is no need to interrupt it periodically to look for other similar programs in core since they do not exist. When a FORTRAN program has been interrupted by some real-time program it takes from 0.1 to 50 milliseconds for the computer to complete the function required by the real-time program and return to the FORTRAN program. There is a small probability of a real-time program being interrupted at a time in the program when it is no longer generating interrupts by an interrupt which initiated a FORTRAN program, thus causing a long delay before returning to complete the real-time program. It has been found through experience, however, that the probability of this happening is negligible. For this reason, cycling periodically through the various programs to determine if they require servicing would only reduce computer efficiency.

FORTRAN-compiled programs are debugged in the normal manner using the compiler diagnostics and a sufficient number of print-outs in the program to inform the programmer of his errors. Debugging the real-time assembly language programs is accomplished on-line through the use of a special debug program. This program uses a memory scope and the on-line typewriter to communicate with the programmer and his program. It permits the programmer to execute a single instruction, read and write in core and execute specified portions of his program without actually stopping the machine or interfering with other experiments

in progress. All options available at the computer console are available to the programmer at the typewriter. At each breakpoint in the program all registers are displayed to the programmer and some option requested. This on-line debugging is considered a necessity if the system is to be a true time-sharing system.

A few programs are not compatible with this time-sharing mode of multiple simultaneous program servicing in that they use an extremely high analog data sampling rate, or special A-to-D synchronizing schemes. An example of such a program will be described later. These programs occupy the computer for only a few seconds and can be scheduled at specific times during the day. To illustrate the use of this system, some programs will be described here which use various features of the system and demonstrate the flexibility which is available at the present time.

examples of users' programs

The first example of a program involves solution of a mathematical model developed to describe the transfer function of pressure receptors in the wall of an artery. The input to these receptors is the pressure in the artery and the output is in the form of nerve spikes or action potentials on the nerve going from the organ to the brain.[1] To test this model, arterial pressure and frequency of nerve firing are sampled from an anesthetized animal. This data is then compared with the frequency of nerve firing generated by the mathematical model. To obtain the data two programs have been written. The first determines the number of nerve fibers which are being detected by the pick-up electrodes. This is accomplished by sampling 1000 action potentials and then returning to the investigator an oscilloscope plot of a histogram of the spike amplitudes. It has been shown that a single fiber fires at essentially a constant amplitude. Amplitudes will vary between fibers due to differences in electrode contact with the fiber. However, because of noise in the recording system, the amplitude histogram of a single fiber has the form of a normal distribution. Upon receiving a histogram, the investigator makes a judgment as to whether there is one or more fibers being recorded. If there are more than one, he continues to dissect the nerve until he obtains a histogram which is unimodal. Here the computer serves as a valuable tool for real-time work. The output of the nerve could easily be stored on magnetic tape and processed at a later date but if due to some error the correct data was not recorded, the experimenter has lost both time and information. With the computer available to him during the experiment, he advances to each new step with the results of the last step already verified.

To obtain the histogram described above, the output of the recording electrodes is fed into a digital logic system which is set to trigger on a given threshold. When a nerve action potential crosses this threshold, it triggers a 500μsec-duration pulse. The computer meanwhile has requested an input of 25 samples from the A-to-D with the converter set in the external sync mode. A sine wave is "anded" with the output of the digital logic system and is fed into the A-to-D converter only during the 500μsec when the nerve spike is above the threshold. The 55KC sine wave is allowed to synchronize the input of analog data into the computer during this time. The computer is programmed to interrupt when the 25-word input buffer is full. This will occur in slightly less than the 500μsec. The maximum amplitude of the action potential will then be determined from these samples and stored for later display in the form of an amplitude histogram. Since the input/output of the computer is buffered, the computer is able to service only those other programs which do not use the A-to-D converter while waiting for a nerve firing. After 1000 action potentials have been so processed, the program calculates an amplitude histogram and displays this via the D-to-A converter as a plot on a memory scope at the investigators station.

Once the investigator is satisfied that he is recording from a single nerve fiber, he calls a second program. This program samples the input to this organ, the arterial pressure, at a rate of 100 samples per second. As it reads in the pressure wave it determines the beginning and ending of each heart cycle. Corresponding points on each succeeding pulse are added and the resulting average waveform is then stored in memory. At the same time the voltage from the nerve is fed through another digital logic system which causes an external interrupt to the computer each time the nerve potential crosses a set threshold. Upon receiving these external interrupts the program reads the real-time clock to determine the frequency of firing at that instant of the heart cycle. Thus, for each averaged point on the pressure wave, an averaged frequency of firing at that point in the cycle is also calculated. Simultaneous with these calculations the averaged pressure wave and frequency of firing are displayed on an oscilloscope at the investigator's station 50 times every second. This, then, enables the investigator to follow the build-up of these averages. When displayed averages become stable the investigator generates a manual interrupt via his station which causes the computer to write the averaged data on a digital tape. At the end of an experiment the investigator may call a FORTRAN program which tests a mathematical model of the organ. This program predicts the time-course of frequency of nerve firing from the time-course of arterial pressure. This predicted frequency of nerve firing is then compared with the actual frequency of nerve firing obtained from the animal as a measure of the validity of the model.

The first two programs described here may either be run on-line real-time, that is, feeding the data from the animal directly into the computer, or the data may be run from analog tape. Since the histogram program uses a special synchronizing scheme with the A-to-D, it must be run at a time when no other real-time programs are being processed. This does not mean that another program cannot be run during the complete experiment, but only during those few seconds that the program is sampling data.

analog processing

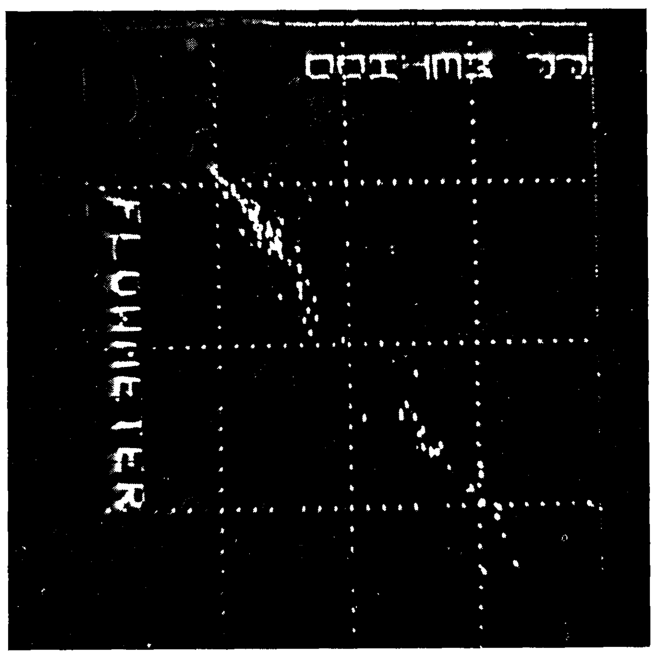
In many instances in the formulating of a mathematical model for some biological system, it is more convenient to program the mathematical model on an analog computer. The investigator tries to match by empirical adjustment of equation parameters the output of the model on the analog computer with actual data which has been recorded from an animal. This process becomes quite time consuming since the investigator must test the model against data obtained under a variety of physiologic states before he can be confident that it is an adequate description of the system. From the raw data, such as blood flow and pressure, many variables must be calculated, such as heart rate, cardiac output, stroke volume, resistance and mean arterial pressure. The time-sharing system allows the digital computer to do much of the work that would normally be done by the investigator at small expense to the computer. A program to do this has been written in two sections. The first part inputs from an analog tape or

[1] Christensen, B. N., Pryor, T. A., and Warner, H. R. "A Technique for the Quantitative Study of Carotid Sinus Behavior." *The Physiologist* 8:134, 1965.

directly from the animal the raw data and calculates the derived variables for a time interval specified by the investigator. It then logs this data on a digital tape for replay later. When the investigator has programmed his model on the analog computer he is then able to call the second portion of the program which reads these variables from the digital tape. With each sweep of the oscilloscope a clamp pulse is generated which initiates the solution in the analog computer and acts as an interrupt to the digital computer. The digital computer outputs these variables through the D-to-A, some acting as forcing functions for the analog computer model and others being displayed on an oscilloscope for comparison with the corresponding variables being predicted by the analog computer model. The output from the digital computer may be at any multiple of real time requested via the digital switch. It would be difficult to justify this mode of operation were it not for time-sharing and multiple-station operation because of the inefficient use of the 3200 by this single program. However, under the multiple-station processing mode, this becomes an effective use of machine time as well as the investigator's own time in developing his mathematical model.

Continuous monitoring of various parameters from an experimental animal is another task readily accomplished by the multiple-station, time-sharing approach. An example of a program to do this is the pressure pulse stroke volume program which provides a means for estimating the amount of blood ejected by the heart on each beat from the contour of the pressure wave recorded in the aorta.[2]

Fig. 4 Comparison of stroke volume determination by pressure pulse method and flowmeter method.



Within ten milliseconds after the end of each heart cycle, an analog voltage is generated to represent each of five variables calculated from the pressure waveform and the input of data can continue indefinitely. The method is based on the fact that the aorta is distensible and acts as a capacitor. Part of the blood that is ejected by the heart

[2] Warner, H. R., Swan, H. J. C., Connolly, D. C., Tompkins, R. G., and Wood, E. H. "Quantitation of Beat-to-Beat Changes in Stroke Volume from Aortic Pulse Contours in Man." *Journal of Applied Physiology* 5:495, 1953.

in each cycle is stored in this distensible tube during the ejection phase; then, during diastole, when the heart is not contracting the stored blood runs out of the arteries as the pressure wave decays. The program consists primarily of a scheme for recognizing the onset of systole and the end of systole or dicrotic notch. The difference in pressure as a function of distance down the aorta at these two points in time is estimated and this pressure difference is related to the difference in volume of the aorta at these same two points in time. The ratio of flow out of the system during systole to flow out of the system during diastole is considered to be proportional to the ratio of the time integrals of pressure over these two periods in time. Then by estimating a single constant which relates stroke volume as measured by the flowmeter to stroke volume as estimated by the pressure pulse method with the dog in a resting state, subsequent beat-by-beat estimates of stroke volume can be made under a variety of physiologic states.

Fig. 4 shows a cross-plot of beat-by-beat estimates of cardiac output made by the pressure pulse method against the measured stroke volume obtained by integrating the output of the flowmeter curve. The correlation between the two methods varies from .92 to .98 under a wide variety of physiologic states including exercise and the infusion of drugs which raise and lower blood pressure and raise and lower heart rate. This continuous monitoring in humans of five important variables in the circulation from a single pressure input is done by using only a small amount of the computer time since other programs are being processed at the same time but still insures accurate pattern recognition of the pressure and flow curves..

At one of the remote stations a typewriter and memory oscilloscope are available for on-line use with the computer. A standard use of the typewriter is entering parameters in mathematical models of various biological systems. The time-course of any variable may be displayed as a function of time on the memory scope and compared with a previous solution. The FORTRAN portion of the model is swapped in and out of memory by a small control program which resides in upper core and controls the communication with the typewriter and the oscilloscope. Thus, the FORTRAN area of core memory is available for other programs except when a new solution of the model is requested. Variables and parameters in the FORTRAN program are referenced through indirect addressing in the control program. The program allows the operator to easily explore the effects of variations in each of the parameters on model performance and is an effective tool for designing experiments and interpreting results.

system evolution

Although this system has been in operation for about 18 months in this laboratory, it has undergone a gradual evolution over this period and will continue to evolve to meet the changing needs of the research community. The programming staff of the laboratory consists of two systems programmers. The rest of the programming is all done by individual researchers and graduate students. The system has recently been put into use on the 3200 system at the Mayo Clinic and will be made available to all 3200 users through Control Data; the company has accepted responsibility for system maintenance. The system is designed to fill a specific need for those engaged in biomedical data of the type generated in a physiology laboratory and is not meant to do all things for all people. Primarily because of this, the system runs efficiently and was implemented by a few people in a short time. An effort is now being made to make the system more readily available to a larger portion of the medical research community in Salt Lake City through expansion of the remote telephone terminal concept. ■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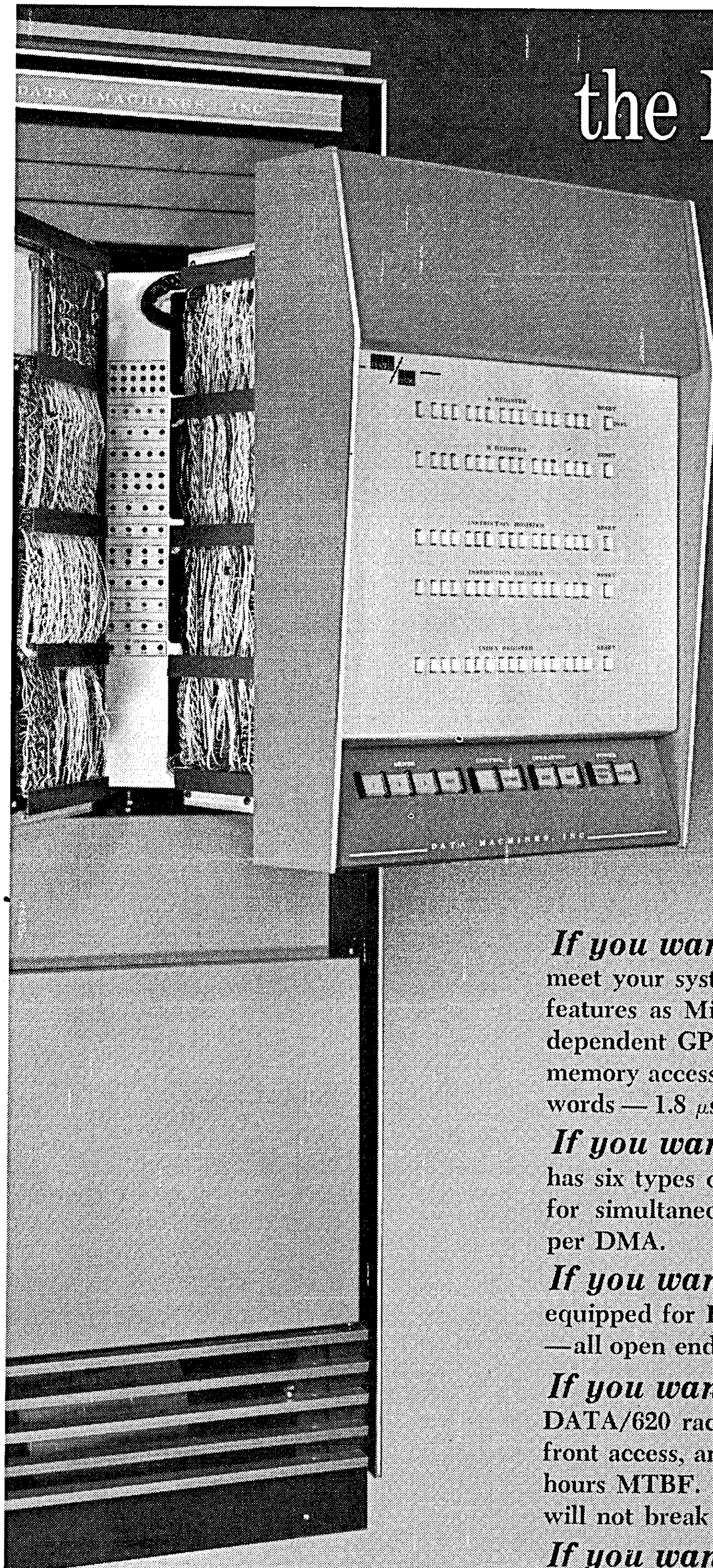

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ARE SMALL, FREE-STANDING COMPUTERS HERE TO STAY?

probably

by FRED GRUENBERGER

If one were to judge the current state of affairs in computing by the number of published lines per subject, then the world seems to be as follows:

> The big, important jobs are done on big machines, run by professionals with the aid of ultra-sophisticated monitor systems.
> The small jobs are done through time-sharing systems via remote consoles.

Little, if anything, in the literature today advocates the use of small, free-standing machines. The man who controls a lonely 1401 or 1620 or 160 and who plans to move up to an 1130 or 1700 or 360/30 may wonder whether he's on the right track. Should he, maybe, sign up now for one of the impending time-shared terminals?

In discussing such a subject, it seems to me vital to define a point in time and stick to it. One tends to confuse what we have now with what we are told to expect. For example, the language of time-sharing systems is one of the virtues currently touted. Now, language is a subject worth considering, but I'd like to cancel it out of this discussion. Therefore, I pick a point in time in which a conversational problem-solving language (like JOSS) is commercially available on some small computer. We can only guess when that time will be—perhaps early 1967.

I maintain that computing-power-per-dollar in small machines is increasing rapidly and will continue to do so. Some of the features now available only through time-sharing will become available on free-standing machines. When that occurs, and when the crossover point in costs is reached (i.e., when it costs the same either way), then attention will focus on the unique advantages of each system of operation.

more for the money

Let me try to bolster my first point—that computing-power-per-dollar is an increasing number. It is probably futile to try to quantify in a simple index a measure of computer-per-dollar, in the same sense that it is fatuous to measure a man's potential with a single number like I.Q. Any such index measures only what it measures, so to speak, but it can still be useful in making broad comparisons. I suggest the following:

$$G = \frac{B(A+M)}{D(L)}$$

where

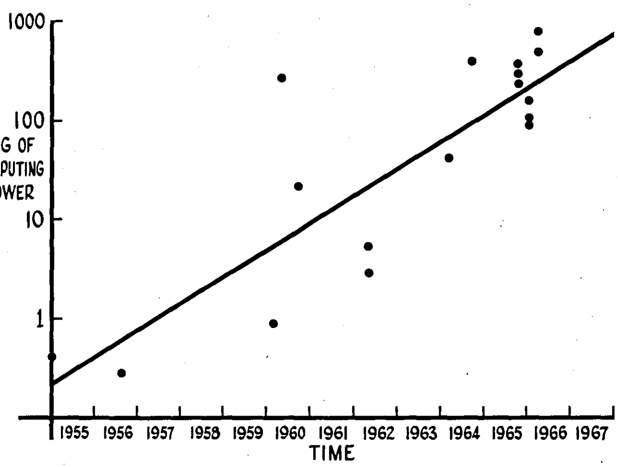
- B = number of bits in main core,
- A = additions per second,
- M = multiplications per second,
- D = dollars per month of CPU rental,
- L = instruction length in bits.

The term M is included to measure something other than addition speed. Some computers penalize (in both machine time and storage space) any multiplication at all, but especially multiple precision. On others, the hardware is such that multiplication comes almost as cheaply as addition. Similarly, the factor L attempts to measure inefficiencies due, for example, to decimal capability.

None of the five factors is wholly objective (D comes closest) and some (M and L) are extremely difficult even to estimate for some machines. In any event, an attempt was made to pinpoint these figures for all small computers, with results as shown in Fig. 1.

Fig. 1 shows the G index plotted on a log scale against time. This line is fitted to data points (by eye). As

Fig. 1



mentioned, the data going into the index is highly subjective. A further complication comes from attempting to assign a point in time to a given machine. Date of first delivery? Date of peak use? Date of announcement?

The value of the index, then, lies in showing a gross trend (as in Fig. 1) or as means of comparing two similar machines.

In any event, we have some basis for asserting that raw

Mr. Gruenberger is now a member of the senior staff at Informatics after many years of association with the RAND Corp. Author of several books on computing, he has a master's degree in mathematics from the Univ. of Wisconsin, where he also served as project supervisor in the Numerical Laboratory.

computing-power-per-dollar for small computers has gone up by some three orders of magnitude in a decade. No existing evidence indicates when this trend might taper off. Whatever we're getting 800 of now, we might expect to get 8000 before 1970.* And the thing we are getting is pertinent to a discussion of time-sharing. Any virtue espoused for time-sharing that relates only to computing power sooner or later can become available in the free-standing machine.

time-sharing advantages

What, then, are the unique virtues of time-sharing, i.e., that **cannot** be made available through the small local computer? Some things seem clear-cut; others less so.

1. **Buy only what you need.** Time-shared systems will probably require a base load (nuisance charge) of, say, an hour a day. Added to that is the (one-time) cost of installing the console, plus the monthly charge for the data set and the per-minute costs of telephone service. From that point on, charges could be entirely on an as-used basis. There need be no worries about keeping the device occupied. (The analogy to the use of electric power is strong.)
2. **Access to powerful tools.** I have postulated a point in time at which a good conversational language (as good as, or better than, JOSS or TINT or MAC's time-sharing language) is available on a free-standing machine. Now, if the loading of that program into the computer is by disc (as on the IBM 1130), then conceivably one could have several languages at his disposal. However, one could always have a wider choice of more powerful languages through a time-shared system, since the processor can be very large and have access to a mass-storage system. The assumptions here are for equivalent cost. For whatever the cost-per-hour to operate a free-standing machine, the same cost-per-hour could hook the user into much greater computing power—and this will remain true for the foreseeable future.
3. **Access to data banks.** Along these same lines, the remote-terminal user can have access to mass storage for other purposes; viz., as a source of data. In a given data-processing situation, the need for computing power might be small (i.e., easily satisfied by a small machine) but the need for data files large, at least momentarily.
4. The use of a remote terminal has obvious advantages in **space-saving and machine maintenance.**
5. The remote terminal may offer **lower pressure on the user.** This may be more psychological than real. There is a feeling, in dealing with a free-standing machine, that dollars are going down the drain during head-scratching time. To some extent, that same feeling should apply to a time-shared terminal. The true situation depends on how the terminal is financed, and to what extent it is saturated.
6. **Queueing problems and turn-around time.** We are getting down to vague and tenuous advantages. It is often claimed that time-shared terminals eliminate queues and reduce turn-around time to zero—an "advantage" that could be attained as readily on a free-standing machine.
7. **Red tape. Current** time-shared systems cut red tape, to be sure, but they are being compared to current operating systems. I see no reason why red tape cannot also be cut for free-standing machines.

Two constants seem to be operating in this area. The cost of terminal gear (typewriters and consoles) will probably remain steady and high unless mass-produced. The cost of communications (i.e., telephone lines and data sets) will also remain fairly constant.

Two factors are variable and dynamic. The cost of free-standing small machines is decreasing rapidly. At the same time, of course, the cost of equipment suitable for central processors for time-sharing is coming down, and the programming for time-sharing may eventually be spread over many installations. There is a race going on.

I suspect that the situation will eventually simmer down to this: a free-standing machine hooked, for short bursts, to a large central facility. Thus, the future might bring us the best of both worlds.

free-standing machine advantages

A similar list can be made of the advantages (over time-sharing) of a free-standing machine.

1. **Lower cost.** If usage approaches one full shift, then the cost of a small computer (rented) approaches $5 per hour, or about half that of any existing or proposed time-sharing system.

   If usage will ever exceed one shift (say, for peak loads), then even greater savings can accrue. A small machine that is owned can be run around the clock, driving the cost-per-hour down to less than $2.
2. **Reliability.** If the time-sharing central processor or the data links break down, then 100 consoles are down, all at once. On the other hand, 100 free-standing machines are hardly likely to be out of commission all at once. One can argue that the overall reliability of equivalent computing power is higher when split 100 ways. Offsetting this is the concept of a duplexed central processor to guard against CPU failure. (What guards us against telephone failure? We have yet to accumulate experience from the existing systems.)
3. **Safety.** Suppose the computing power is being used to interact (in the sense of monitoring, but not in the sense of process control) with a physical experiment. The experimenter might feel more comfortable with an independent machine, and not have to worry about communication links or delays that time-sharing might cause.
4. **Speed.** The ratio of speeds of the large machines to the small ones is now of the order of 3 or 4 to 1. Some of the speed of a large machine (acting as the CPU for a time-shared system) must be dissipated in system overhead; the remainder is distributed among those consoles needing computation. The full attention of a small machine, operating for a single user, could reasonably lead to greater speed.

   A more interesting question is, where will this relationship be a few years from now? I conjecture that the ratio of speeds (large to small machines) will tend toward 1:1 and that the index of computing power for small machines will increase faster than for large machines. If this occurs, then the speed advantage for free-standing machines will accentuate.
5. **Security.** Obviously, classified information cannot be processed by a computer utility without elaborate cryptographic techniques. Even then, security officers would probably have qualms. The same situation would hold for privileged and company confidential information. In order to avoid leakage of such information, processing by a free-standing machine would seem preferable. ■

* The same analysis applied to large machines shows a growth rate of *two* orders of magnitudes in a decade.

SPECIFYING OBJECT-CODE EFFICIENCY

hints for compiler buyers

by CHRISTOPHER J. SHAW

If you want to be really hard-headed about efficiency when you buy a compiler, here's how you might go about it:

First: Code up a small but representative set of test routines in the source language of the compiler, along with some test data for these routines. Opler[1] discusses some of the characteristics to be desired in such test programs. Briefly, they should be designed with at least four purposes in mind:

To determine whether the compiler accepts the full source language.

To determine whether the object code generated by the compiler produces the correct results.

To determine the speed of the compiler.

To determine the efficiency of the object code produced by the compiler, in terms of its use of storage space and execution time.

This note discusses only this last purpose and, for this purpose, the test routines should include statements that reflect the kinds of applications for which the compiler will be used as well as statements that, based on experience with similar compilers, can be expected to produce the most troubling cases of inefficient object code.

Second: After the test routines have been written and debugged in the compiler language, recode them in the assembly language of the target computer. Assign a senior programmer to the task, preferably one with experience in programming for the target machine, and tell him to turn out the tightest code possible, using all the facilities the machine provides. (Questions of trade-offs between storage space and execution time that arise here should be resolved with the same criteria you would want used in your operational programs.) Since almost any code can be improved, you might want to repeat this step a few times, until you're confident you've squeezed out all the fat in the assembly language routines. You will, of course, check these routines out with the test data to see that they too produce the desired results.

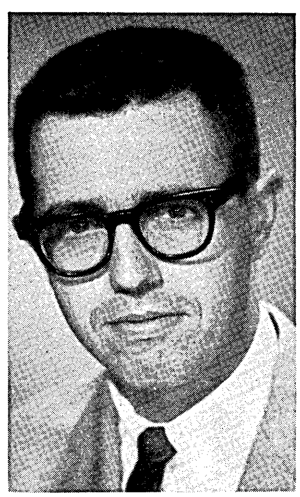
Third: These assembly language routines are then your standard of coding excellence,[2] and you can specify that the compiler you're buying turn out object code that averages no more than x per cent more total instructions (and constants) and y per cent more total execution time, using the same test data (x and $y > 0$).

The question now naturally arises, what are reasonable values of x and y to ask for? Well, this answer depends on a lot of factors, not the least of which are the test routines themselves. But I wonder if some general answer isn't possible, assuming that all you want is a reasonably efficient compiler, for a reasonably straightforward source language, on a reasonably ordinary machine, and at a reasonably competitive price. Under these assumptions, my guess, for x, would be from 20 to 30 per cent; for y, from 10 to 20 per cent.

Fourth: in checking the compiler to see if it meets your standards here, you can afford to allow the compiler builders to rewrite the source language versions of the test routines in an attempt to coax the best possible object code out of their compiler. Needless to say, the compiler-generated object code should do essentially the same computations and produce the same results from the test data as the hand-coded routines.

If the compiler writers do come up with a more efficient set of source routines, you should ask them to document the coding tricks they used to do this. Of course, they may just have discovered a better algorithm than did your assembly language programmer, and their compiler really turns out lousy code. More power to them; you'll just have to grin and bear it.

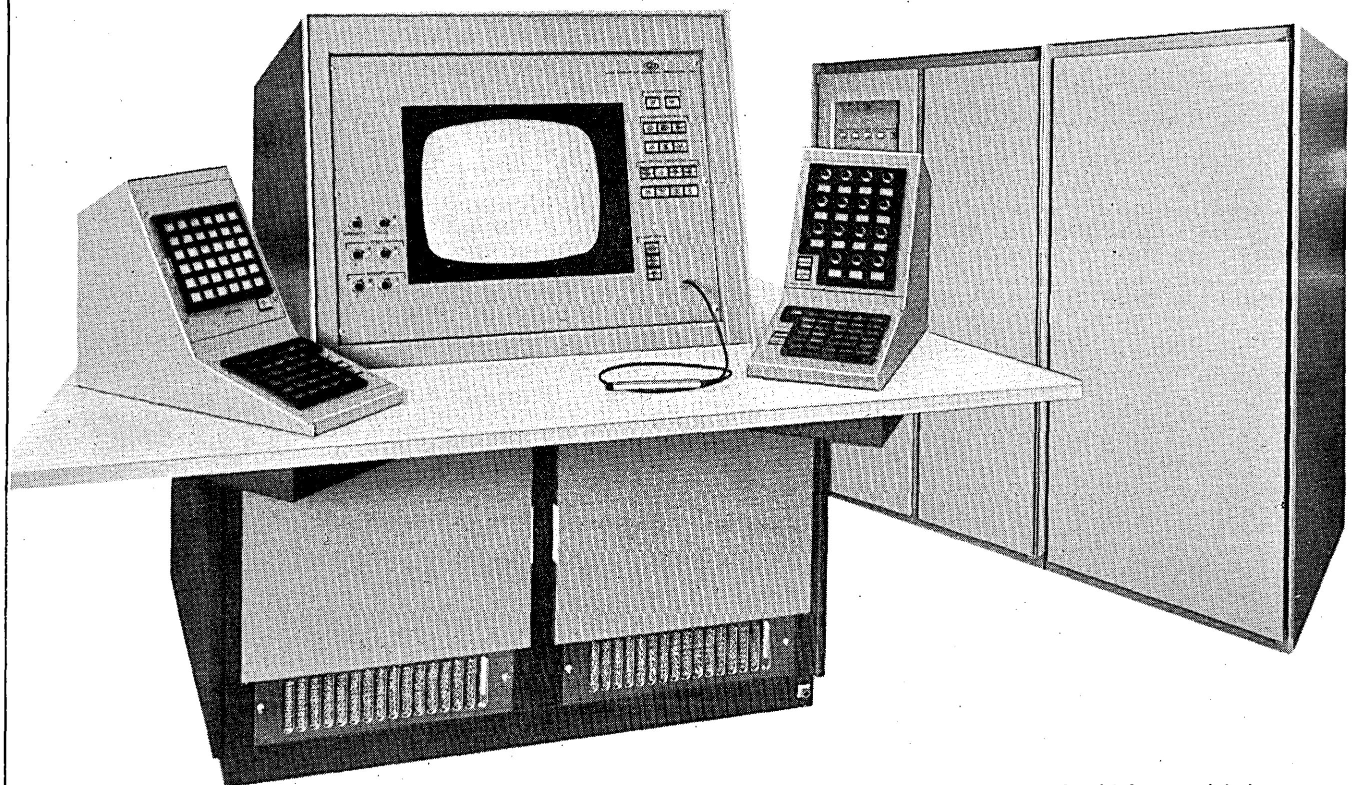
Another objection I've heard to this scheme is that if, as you should, you provide the compiler writers with the test routines as part of the compiler requirements, along with the values for x and y, then they'll be able to build their compiler to handle efficiently just these specific cases. Yet, if you've chosen your cases with care so they cover most of the problems that concern you, then this is exactly what you want them to do. ■



Mr. Shaw heads the information center on Information Processing at System Development Corp., Santa Monica, Calif., and is chairman of the Special Interest Group on Programming Languages of the L.A. chapter of the ACM and chairman of the Special Interest Committee of the ACM. He has participated in language standards work at both the national and international levels. A mathematician, he is a project leader of the Advanced Programming technical staff of SDC's Research & Technology Div.

[1] Measurement of Software Characteristics, Datamation, July, 1964.

[2] You could, in step two, go another route and try to obtain instead a standard of coding mediocrity. This would be harder to do, since it would entail averaging out the programs written by a representative sample of programmers. And it would not serve to measure object-code efficiency any better than would a standard of coding excellence. Furthermore, you couldn't use this standard of coding mediocrity to determine the average efficiency of compiler-produced code unless you applied a similar sampling procedure to obtain a representative set of compiler-language routines.



Picture above shows display console with its associated scanner and control cabinets.
Link Waveform Display/Analyzer is used on line with 7040/7094 computer at Ballistics Systems Division, USAF.

New LINK Waveform Display/Analyzer— precision film reading and recording with one machine.

Here is a new graphic input/output device that can help reduce computer time and programming costs significantly.

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- Scan a film image or waveform and digitize the data.
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- All solid-state circuitry.
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For an informative brochure, write to Advanced Product Sales, General Precision, Inc., Link Group, 1451 California Ave., Palo Alto, Cal.

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3M TASK FORCE Reports:

How to design a total information system

In a previous Task Force Report it was pointed out that microfilm has no peer in the recording of total information. Proper systems design, however, requires the study of several factors in designing any effective information system.

Prior to the selection of equipment, the microimage file form which will be used to establish central and satellite information files must be determined. Strangely enough, the *cost* per page recorded for assimilation into the system may be one of the least important factors in the selection of the microfilm.

In the table below, the cost per page converted for storage is tabulated for the most common microforms. The cost ranges shown, which reflect cost experience in efficiently-planned operating systems, differ little from one form to another *when* a given microform is being used most effectively.

It becomes apparent then that the selection of the microform and thus the equipment used in the system must be based on other considerations. Some of the considerations which relate to the ease of creating, duplicating and distribution of the microform are also shown in the table. In general, that microform should be used which can best be adapted to the natural organization of the information store and which can handle the changes to the store.

Most commonly, aperture cards and microfiche are used to record units of information. Documents recorded on microfiche or aperture cards can be serially identified and simply added to the back of the existing file, or they may be identified as they relate to a segment of the file and interfiled in the proper place. With either of these microforms, replacing a superseded item in the file with a new document can be accomplished with ease.

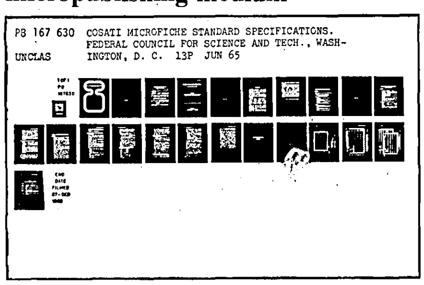
Aperture cards help add new information instantly

Aperture cards, for example, have long been used by larger organizations for recording drawings and related documents in reproducible form. The primary or first generation cards are then replicated to duplicard decks at speeds up to 2000 cards per hour. This provides distribution of the information in compact, reproducible form to satellite files established to serve the various users of the design information.

The rate of change of drawings in many files required that a unit record microform, such as the aperture card, form the basis of the system. With the introduction of the 3M Processor-Camera with its capability to convert documents to microform on a document for document basis, systems based on the aperture card and duplicard could be designed for organizations generating as few as ten new and revised drawings per day.

Similarly, there are several systems in operation and many others under consideration in which the aperture card is used for technical reports, various other business records and published documents consisting essentially of letter-sized pages and ranging from one to sixteen pages in length.

Microfiche as a micropublishing medium



Within the past few years, microfiche has come into its own as a micropublishing medium for larger documents, those greater than thirty pages in length.

The application of present and future technology and design capability will make microfiche an even more useful microform. For example, the equipment and time required to prepare master microfiche from input documents is such that microfiche can only be used economically for micropublishing.

This will change; work on the development of a microfiche camera and processing capability is under way. The objective of this development is equipment which would provide for the conversion of single documents to master microfiche.

Roll film for information collections

In general, two types of information collections may best be handled in roll form. Serial collections which change only by adding new documents to the end of the file, where there is either a broad distribution of document length or a very narrow range of short documents, and where there is a distribution of all of the contents of a roll to given files can most effectively be handled in roll form.

Conversely, for collections such as catalogs where there is frequent change which can be programmed to republication, roll film in cartridges finds excellent application. When the characteristics of the information collection are matched by the best attributes of roll microform, it can be the least costly, most compact form and the one with which there is the least concern for file integrity.

"People" files

Jackets find their best application in establishing unit or "people" files. These are files to which information must be added on some sporadic basis. Since one can add microimages to a jacket, it is the only microform which can be used effectively for this type of open-end file resulting in a unit film form entry.

However, the cost and control which must be exercised in making a series of very short additions to a series of jackets has precluded its use in many files.

Until recently, it was difficult to prepare high quality, contact copy microforms from a jacket for distribution. The advent of the thinner jacket represents an improvement in this regard. However, the bi-axially oriented polyester films used in these jackets has some optical properties which may still adversely affect the quality of print through images from microimages filed in the jacket. From both this standpoint and with respect to the specifications which are being written by both the Federal Government and industry for microfiche, it is improbable that jackets will ever be totally satisfactory as masters for the preparation of microfiche. Jackets find their best application in establishing one central microform store of open-ended files.

For a more complete discussion of a total information management system, please write Dr. David R. Wolf, 3M Company, Building 209, Dept. FDJ-46, St. Paul, Minn. 55119.

3M COMPANY

	Roll Film (and cartridges)	Jackets	Aperture Cards	Microfiche
Cost	Excellent	Fair-Good	Good	Good
Storage Density	Excellent	Fair-Good	Fair-Good	Fair-Excellent
Preparation Cycle				
Batch	Fair-Good	Fair-Poor	Fair-Good	Good
Document	Poor	Very Poor	Good-Excellent	Fair-Poor
Updatability	Fair	Good (1-file)	Good-Excellent	Good-Excellent
Distribution				
Total	Good	Not Applicable	Good-Excellent	Good-Excellent
Profiled	Poor	Not Applicable	Good-Excellent	Fair-Good
Information Retrieval				
Speed	Fair-Excellent	Good	Good	Good
Output				
to Film	Very Poor	Fair	Excellent	Fair-Good
to Hard Copy	Good-Excellent	Fair-Good	Good-Excellent	Good
Cost per 8½ x 11 Page Filed				
Primary File	$0.007-.02	$0.01-.04	$0.01-0.10	$0.03-.06
Secondary Files	.002-.01		0.003-0.02	0.002-.01

CIRCLE 34 ON READER CARD

when's breakfast?

THE FLIGHT TO TOKYO-1984 STYLE

by LT. DORIAN DE WIND

(Inspired by Ascher Opler's article in the January issue, Bon Voyage—1984 Style, Lt. de Wind of the Air Force offers this description of the flight to Tokyo taken by Lester P. Jonas on the advice of his UTSS counselor.)

It is 7:15 a.m. at San Francisco International Airport. The pilot of flight 597, Trans Sonic Airlines, steps into the cockpit of his shiny new Boeing 797 . . . .

AIRBORNE

COMPUTER: Good morning. I have just received your flight plan from traffic control. If you desire to read it I'll print it out.

PILOT: Never mind, I'm running late. How is the aircraft?

COMPUTER: All pre-flight checks have been completed. The airplane is in perfect condition, except for a minor deviation error in the manual compass. Could possibly be an error in my check-out program. Would you like me to obtain a double-check from remote control?

PILOT: Negative, we won't be needing it anyhow, I'll let you do all the flying today . . . . had a rough night. By the way, where are we going today?

COMPUTER: Our destination is Tokyo. I have just received indication that all passengers are aboard. We are ready to go; all seat belts are fastened except yours. Would you please sit down?

PILOT: O.K., what's on the menu for today?

COMPUTER: Will print it out for you while taxiing. Am just receiving taxi and take-off instructions, also weather forecast. Looks like a smooth flight ahead. Will be using runway 27 . . . . presently taxiing to take-off position, take-off time will be 07:31, estimated time en-route 3 hours and 17 minutes, flight altitude . . . . .

PILOT: Tell it to the passengers. The menu looks good. What time is breakfast?

COMPUTER: The master menu program was just checked; breakfast will be served in 30 minutes. Passengers have been briefed, take-off cameras have been programmed on, pressurization completed, final data transmission, ground, and airborne equipment checks all O.K. We are ready for take-off; if this is to be a computer controlled take-off press the "AUTO T/O" button. . . . . Understand. Take-off program and latest weather information have been read in. We are rolling.

PILOT: Congratulations! That was one of the smoothest take-offs I have seen you make yet.

COMPUTER: Thank you. I thought so myself, consider-the strong cross wind. . . . . . Take-off time was 7:31 on the dot. Am presently climbing under ground radar control. In-flight movie playing is the "The Moon Lovers." Landing gear is up. During take-off noticed a change in left yaw response rate of 15 microseconds, have modified the program to compensate for it on future flights. Also discovered a failure in the flight data recording system, switched over to the alternate system and recorded it on the malfunctions log . . .

PILOT: O.K., O.K. . . .

COMPUTER: We are level at 40,000 feet, all in-flight checks completed. We are now under Airways control, the weather in Tokyo is excellent; have been notified there will be five-minute hold in the traffic pattern over Tokyo International, then will land on runway 15 behind Pan American flight 885.

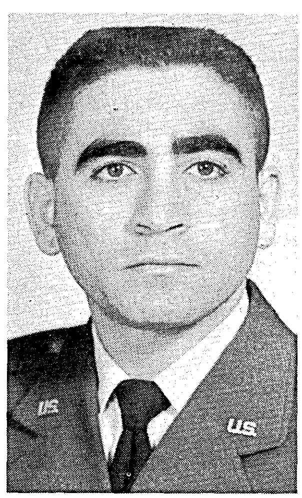
PILOT: Well, I think breakfast should be ready now. Let me know if you need me.

COMPUTER: Before you go, press the "AUTOMATIC MARGINAL CHECK" button so I can perform preventive maintenance checks on my circuitry, but leave the "MONITOR/-INTERRUPT" option on in case I need to go back to the flight program.

Two hours and fifty-two minutes later: An alarm sounds in the cockpit.

COMPUTER: Sorry I had to wake you up, but we just landed at 18:48 Greenwich Mean Time. You will have to take over now, as you know it is against company policy to taxi under computer control on foreign airports.

PILOT: (Sleepy voice) Oh, O.K. Boy, these flights are getting more and more demanding every day!



Lt. de Wind is presently assigned to the Reno Air Defense Sector, where he is responsible for operation and maintenance of the SAGE AN/FSQ-7 computer. He is a graduate of the Air Force Electronic Computer Maintenance Officer Course and intends to complete his studies for a degree in computer science through the Air Force Institute of Technology.

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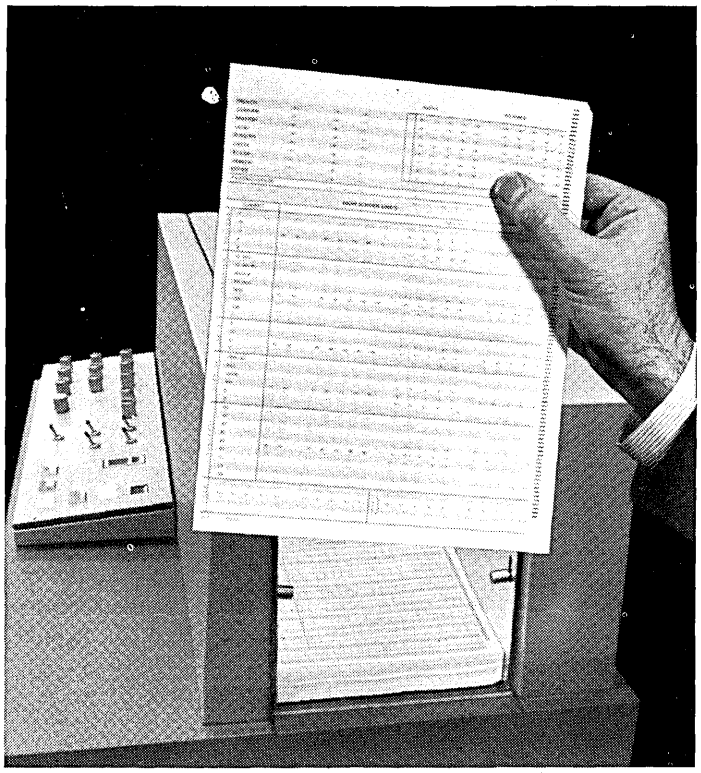

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CIRCLE 35 ON READER CARD

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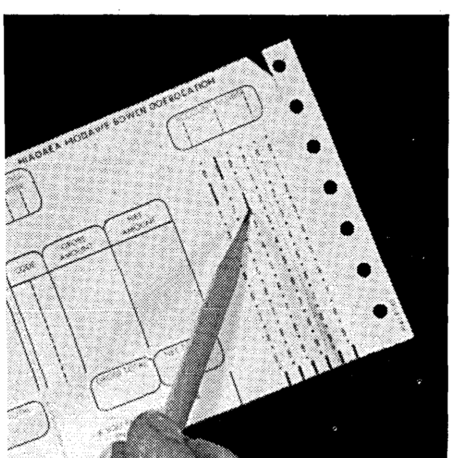
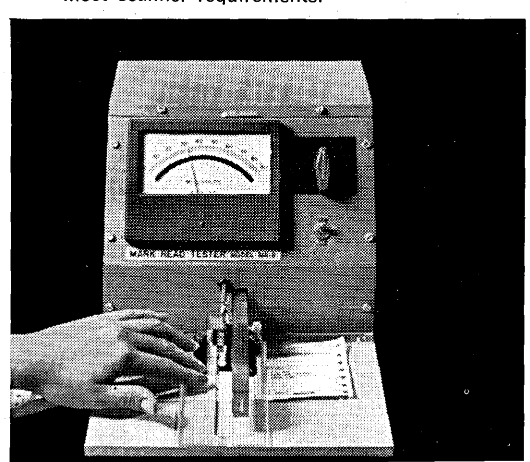
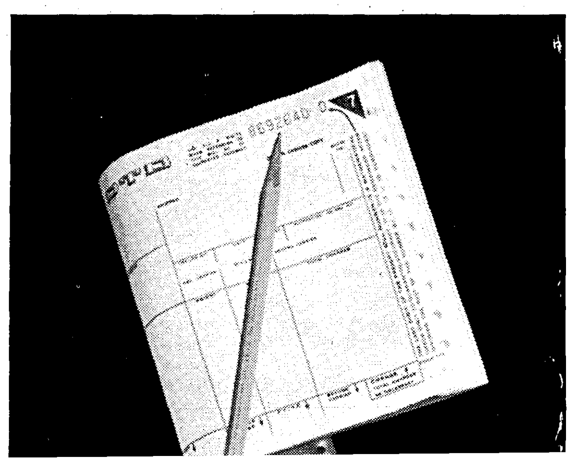






THE BURROUGHS B2500 AND B3500

Whether because winter is done and spring has sprung, or because manufacturers now see where IBM is committing itself, new computer announcements are being made with a rush and a fervor. Last month, Sigma 7 got the Klieg-light treatment from SDS (see March, p. 53). And if industry pundits can be believed, Univac will have a few words about a new machine in June.

Now it's Burroughs' turn. Continuing to produce decimally-oriented computers, the latest entries are the B2500 and B3500, which form part of the Burroughs 500 Systems. (Others in this program-incompatible series are the B5500 and B8500). Functioning decimally all through the mainframe, including the addressing, the 2500 and 3500 take their place between, but overlap, both the B200 and B5500—but are not compatible with either. In the marketplace, they compete with the IBM 360/30 and 40, the RCA Spectra 70/35 and 45, and the 200, 1200 and 2200 from the Honeywell 200 series.

The new machines also speak for the company's commitment to the latest technology. Monolithic integrated circuitry is used throughout the mainframe. Specifically, they're Fairchild Semiconductor's CTuL family.

With the new pair of 500's, the company also emphasizes the use of higher-level languages. Available are both COBOL and FORTRAN IV. Reportedly "open-minded" about PL/I, the company is awaiting the specifications for this language. Some features of the new machines have even been designed to take advantage of COBOL. The adder, for example, operates from left to right (high-order to low-order position), and in comparing numeric fields the machine looks first at the high-order position.

In a further attempt to upgrade the dp operations of its users, Burroughs has drawn on its experience in multiprogramming with the B5500 and added this capability. Several programs can occupy core simultaneously, under the aegis of the Master Control Program operating system; smaller configurations operate under the basic control program. A base register makes possible the use of relative addresses, program boundary (or limit) registers achieve memory protection by preventing the accidental overwriting of one program by another, and priority interrupt is on the basis of a fixed assignment. There's also dynamic storage allocation and the automatic overlay of program segments.

The two computers differ only in internal speed, memory capacity, and the number of I/O channels. The B2500 has from 10,000 to 60,000 characters of core; two characters can be accessed in 2 usec. It can have up to six I/O channels, three of which can be of the high-speed variety. The larger B3500 can have up to 500,000 characters, two of which are accessible in 1 usec. There can be up to 20 I/O channels, 10 of them high-speed.

internal organization

As can be surmised from the memory access rate, the internal code is the 8-bit EBCDIC (Extended Binary Coded Decimal Interchange Code), used also in the 360 and Spectra 70. By means of a programmatically-selectable mode switch, ASCII code can also be executed without translation. Internally, the machines handle 4-bit digits, 8-bit characters, 16-bit words, and 24-bit syllables. Processor instructions, as distinguished from I/O instructions, are variable in length from one to four syllables; thus, instructions may contain from zero to three addresses.

There is a special case of numeric representation for floating-point operands (floating point is optional). These operands are in the 4-bit-digit format, but the mantissa can be of variable length—up to 100 digits.

Arithmetic speeds are perhaps best expressed by examples. In the B3500, it takes 32 usec to add two 5-digit numbers. This includes the time to fetch the instruction data from core, return the sum to core, and to pack and unpack mixed digit and character fields. The same operation in the 2500 requires 64 usec. The floating-point add takes 13.5 usec, plus the normal add times of the mantissas of the two operands.

Including the same operations, the 5 by 5 fixed-point decimal multiply times are 206 and 412 usec for the 3500 and 2500, respectively. Floating-point multiply takes 23.5 usec plus the normal decimal multiply times of the two mantissas.

An important part of the processor is the Address Memory, a 100-nanosecond register with from 24 to 120 words. Eight words are assigned to the processor, and two to each I/O channel. During execution, the processor addresses core memory with words from Address Memory. Thus, memory accesses are not required for information relative to the command itself during execution; that is, accesses during the execution phase are for data only. Peripheral control units use their associated words in Address Memory for data accesses during their I/O operations.

Input-output operations are independent of the processor and of each other, and any or all I/O channels may memory, with a 100-nanosecond cycle time. This is used to store microprograms that initiate and control:

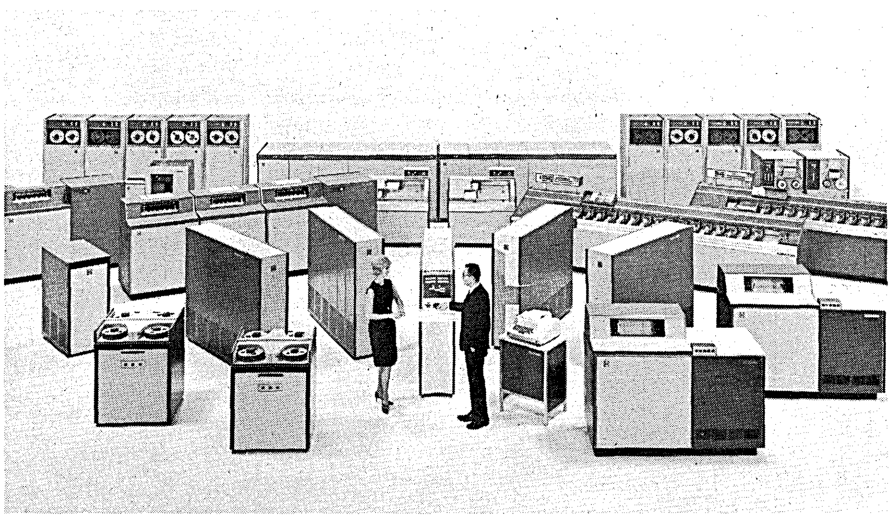
- Memory reads and writes for the processor
- Transmission of data from register to register within the processor
- Loading and unloading the processor's eight words of address memory
- Counting and setting of all the various registers
- The initiation of I/O operations

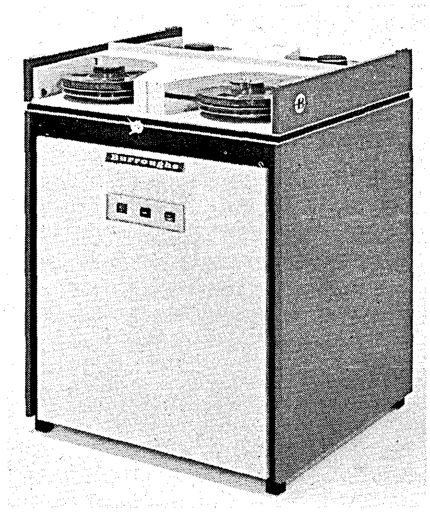
Microprograms are automatically initiated by the op codes of the program instructions as they are fetched from core. Additional read-only storage may be added, including emulators for the B200 series and the IBM 1400 series.

The system memory—for the storage of the software package, the user program library, and for working or general storage functions—is a single magnetic disc with a capacity of 1 or 2 million characters and an average access time of 17 msec. At least one of these units is required when operating with the Master Control Program. Although resident on disc, the MCP also requires 10K of core.

Other peripherals include the regular disc file expandable from 10 million to 2.5 billion characters. With a head-per-track design, the average access time is 20 msec, and the maximum transfer rate is 240KB. In addition to stand-up tape drives, a new unit consists of a cluster of four drives in one cabinet. They operate at 45 ips, have transfer rates of 36KC and 72KC, and rent for approximately $1300 and $1700 per month. Also new are drum printers operating at up to 1,040 lpm.

In the area of communications, there are both single- and multiple-line controls. The latter enables the use of any mix of voice-grade lines. Communications can be with any other 2500 or 3500, the B493 typewriter inquiry station, a mod 33 or 35 Teletypewriter, IBM 1050, Univac 1004, and the Friden 30 On-Line System.





operate simultaneously. The I/O system time-shares core and the Address Memory with the processor, under control of the Central Control unit.

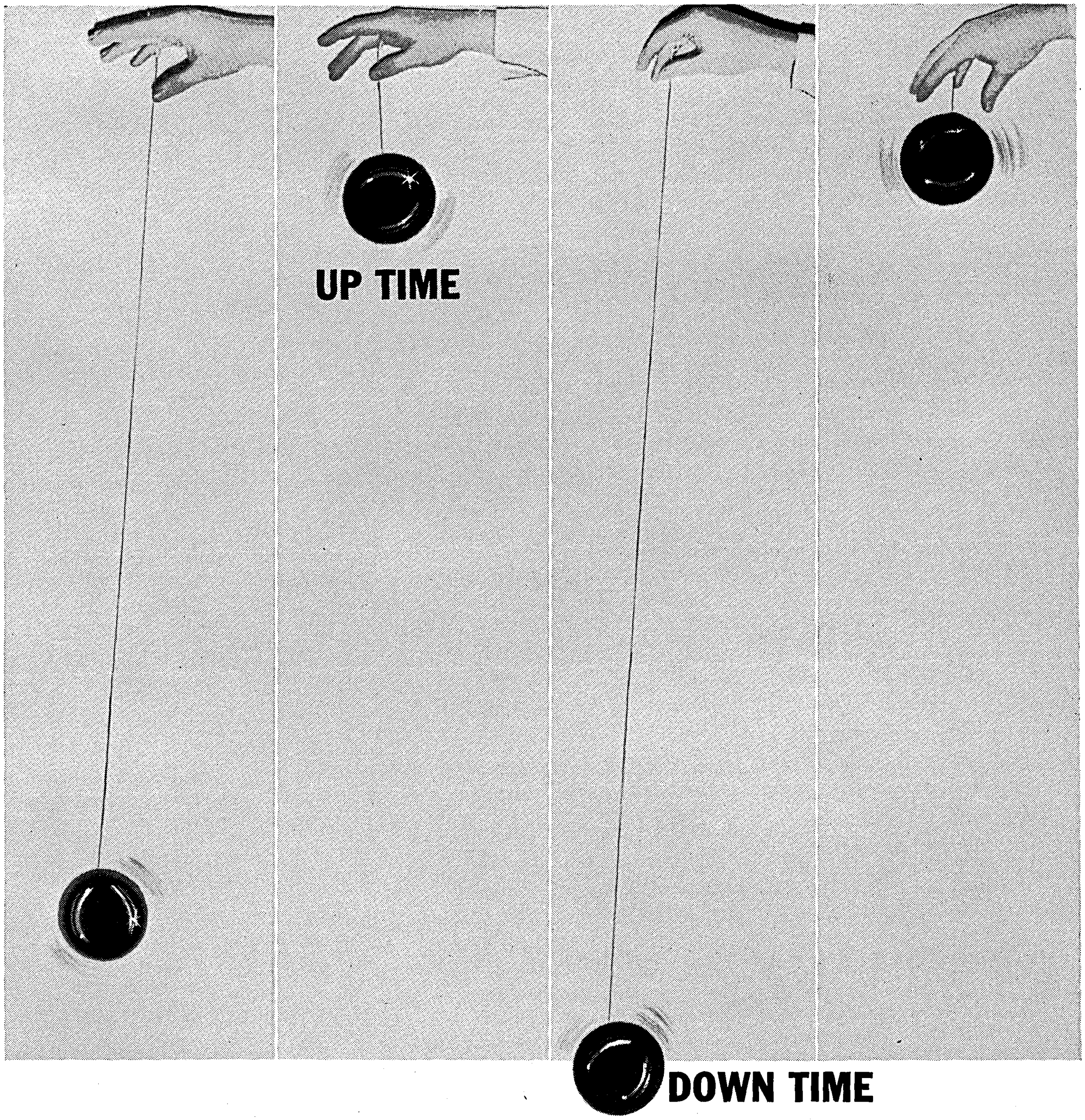
Still another register is the index register, three of which are available to each program in core. Indirect addressing and indirect field length are standard features of the system, and are allowable to any level.

microprograms & emulators

Available also is a read-only storage, a resistive-type

System prices begin at $208,610 ($4,195 per month) for a minimum tape-oriented B2500 and $236,690 ($4,780/month) for a minimum tape-centered 3500. The smallest 2500 with the MCP operating system goes for $5,575/month, and can be purchased for $274,850. A "typical" (but large) commercial B3500 system might include 90K of core, 100 million bytes on discs, eight 72KB tapes, floating point, and other peripherals. The system would rent for $20,720, and sell for $1,032,765.

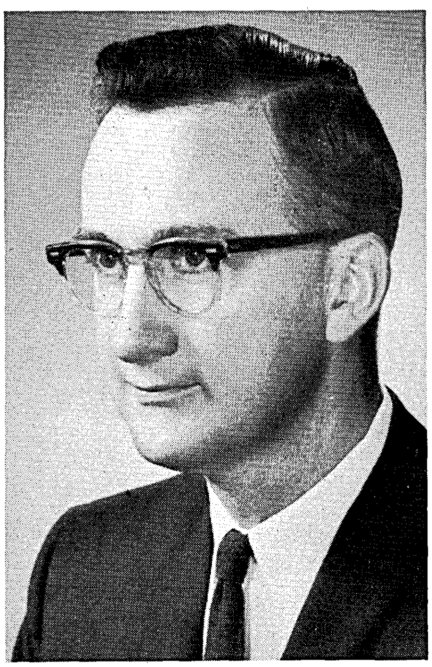
Deliveries of the B2500 are scheduled to begin in January of 1967; first B3500's are slated for May 1967. ■


UP TIME
DOWN TIME

SJCC '66

the chairman's welcome

by Harlan E. Anderson



The 1966 Spring Joint Computer Conference will be held in Boston April 26-28. It is my pleasure to invite everyone who is interested in the information processing field to attend this meeting. In keeping with the pattern of past conferences, a wide range of technical information will be presented. The breadth of the program is a reflection of new applications for computers that are being discovered and old ones that are being expanded in scope.

Information retrieval will receive increased emphasis at this conference. This attention is prompted by the growing concern of professional people who are trying to keep abreast of the large amount of technical information being published. One physicist calculated that if the *Physical Review* continued to grow at the rate it did from 1945 to 1960, it would weigh more than the earth in the next century. Although computers are playing an important role in the solution to these problems, the field is still in an early stage of development. The availability of mass memory devices and information utility concepts makes this a timely subject.

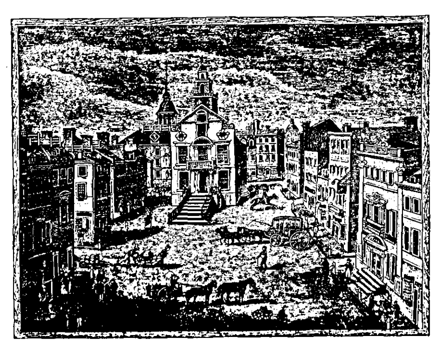
Our keynote speaker, Walter Finke, president of Honeywell EDP, will address the opening session on one phase of this broad subject in his talk, "Information: Dilemma or Deliverance." Our luncheon speaker, Dr. Isaac Asimov, noted science fiction author and speaker, will talk on the subject "Four Steps to Salvation." In addition, a panel discussion will be held on the topic of "The Evolving Library." Several members of a recent summer study group on this topic will be participants in this important panel.

A second area receiving special attention is the role that computers might play in the business transactions of individuals. This will be highlighted in a panel discussion session on the topic, "A Checkless—No Money Economy."

The rapidly evolving time-sharing concepts will be reported on in several technical papers, panel discussions and in tours to organizations in the Boston area.

An innovation in format for this conference will be the combining of a panel of technical leaders with most sessions of technical papers. An abbreviated presentation of the papers will be made so that a review and discussion of its contents may be carried on by the panel. This is part of continuing Joint Computer Conference effort to make the technical programs more interesting and useful to the attendees.

On the non-technical side, Boston is an interesting city to visit, and the conference steering committee has planned opportunities for attendees to participate in a wide spectrum of attractions ranging from the famed Freedom Trail of historical sites to a Boston pops concert.



On behalf of AFIPS, I welcome your attendance at the 1966 Spring Joint Computer Conference. Come and participate fully in the extensive program planned for your benefit. □

conference particulars

From Las Vegas, where little is banned, to Boston . . .

Many in the Outside World think of the city as Old Boston, bound in historical and familial tradition ("where the Lowells speak only to Cabots . . ."). But the Chamber of Commerce talks of a New Boston with a modern architectural facade, and the *New Yorker's* Christopher Rand has written that the technological research and development occurring at local universities, laboratories, and firms have created a Boston in renaissance. The patron for the most part is the federal government, and a major object and instrument of the activity is the computer.

It is at the New Boston's favored landmarks, the Prudential Center and the Sheraton-Boston Hotel, that the Spring Joint Computer Conference will be held on April 26-28. The technical program available to the 4000 computerites expected has been kept to a small number of sessions, 16. Two or three will usually run in parallel, but only one is spotlighted Tuesday at 3:30—time-sharing, which, of course, has been a main focus of computer development in this region. IBM will be the sole manufacturer on the podium. A panel discussion on the meanings of time-sharing will follow Wednesday morning.

A unique feature of the program will be the panel of critics at most sessions, who will give pros and cons on the papers presented. In a session on pattern recognition, M. Minsky of MIT will play "devil's advocate," but we don't know if his MIT computer-controlled "hand" will be used to hook any speakers who may give a bad paper.

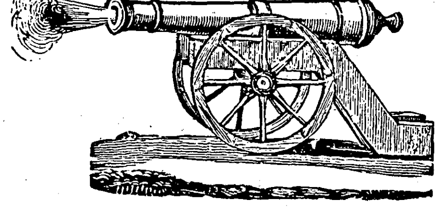
The implications of computers will be discussed by keynoter Walter Finke, president of Honeywell EDP, in his speech, "Information: Dilemma or Deliverance?" If "Four Steps to Salvation" sounds like an interesting luncheon talk, its deliverer makes it more intriguing: Isaac Asimov, science and science-fiction writer and associate professor of biochemistry at the Boston University School of Medicine. (For the ultimate in miniaturization, read his latest, *Fantastic Voyage.*) Also at

the Wednesday luncheon, the W.W. McDowell award for outstanding contribution in the computer field will be presented to Fernando J. Corbató of MIT for his work in large-scale time-sharing systems.

With no advance registration, the sign-up will begin Monday, April 25, at 6:30 p.m. The fees, which include the Proceedings, are $10 for members, $20 for non-members. AFIPS sponsoring societies for SJCC are the Assn. for Computing Machinery, IEEE Computing Group, American Documentation Institute, Simulation Councils Inc., and the Assn. for Machine Translation and Computational Linguistics. On Friday, after the conference, each of these groups will have sessions on such topics as real-time system design, interactive computation, optical scanning, and natural language processing.

About 90 firms will show products and services in War Memorial Auditorium. Expect a packed exhibit area: at time of writing the chairmen were still looking for corners to put more booths. Hours: Tuesday, 11:30-5; Wednesday, 10-8; Thursday, 10-5.

Other conference features include tours of government and university laboratories and manufacturing facilities in the area. Invited students and teachers will have a chance to trade ideas about the use of typewriter and graphic terminals with Richard Warren of MIT and Anthony Oettinger of Harvard. Also on the agenda are 41 computer sciences films (including "The Living Machine") on implications, applications, experiments, and tomorrowland; an amusing clip should be IBM's satire on the evolution of programming. The ladies' program will include a historical tour, visits to the Gardner Museum of antiques and art,



the Botanical Museum at Harvard, and the Heritage Center, and a little wine-tasting at Anthony's Pier 4.

Although there won't be a final summary at the conference, the panels of critics at the sessions, and indeed, the specialists who will be available to the general press and others to discuss the meaning of the session topics, could help make this SJCC one of the better conferences for perspective *and* information. ■

the exhibitors

Exhibitors are categorized according to the products they will be showing.

COMPONENTS & EXPENDABLES

keyboards and control panels	booth numbers
Ohr-Tronics, Inc.	913A
Royal Typewriter Co., Div. of Litton Industries	1106-1108

logic modules	
Brogan Associates, Inc.	207
Computer Control Co., Inc.	201-205
Decision Control Inc.	1204
DI/AN Controls, Inc.	324-325
Digital Equipment Corp.	1009-1012
Raytheon Computer	611-612, 703-704
Scientific Data Systems	314-318, 314A, 401-405
Vermont Research Corp.	602

mag tape and accessories	
Ampex Corp.	319-323
Computron Corp.	1202-1203
U. S. Magnetic Tape Co.	508

memory equipment and systems	
Ampex Corp.	319-323
Computer Control Co.	201-205
Decision Control Inc.	1204
DI/AN Controls, Inc.	324-325
Electronic Associates, Inc.	214-218, 214A, 301-305
Electronic Memories, Inc.	410-411, 410A
Fabri-Tek, Inc.	1309-1311
Fairchild Memory Products	813-814
Ferroxcube Corp.	1401-1403
General Precision, Inc., librascope Group	913-916
Indiana General Corp.	1210-1211
Lockheed Electronics Co.	106-108
Magne-Head, Div. of General Instruments Co.	208-209
RCA Electronic Components & Devices	605-606
Raytheon Computer	611-612, 703-704
Tech-Met, Inc.	613A
Vermont Research Corp.	602

Other	
Corning Glass Works	1316
Digital Equipment Corp.	1009-1012
ELCO Corp.	518
Electronic Associates, Inc.	214-218, 214A, 301-305
Fabri-Tek, Inc.	1309-1311
Ferroxcube Corp.	1401-1403
Sylvania Lighting Products Div.	114

PERIPHERAL EQUIPMENT

character recognition equipment	booth numbers
Control Data Corp.	310-313, 310A, 313A 406-409

data acquisition equipment	
Brogan Associates, Inc.	207
Dartex, Inc.	330
Datamec, Div. of Hewlett-Packard	805-808
Digital Electronic Machines, Inc.	1315
Kennedy Company	206
Ohr-Tronics, Inc.	913A
Raytheon Computer	611-612, 703-704
Redcor Corp.	326-327
Teletype Corp.	1312-1313
Texas Instruments, Industrial Products Div.	333

data conversion equipment	
Adage, Inc.	810-812
Ampex Corp.	319-323
Digital Electronic Machines, Inc.	1315
National Cash Register Co.	1013-1016, 1101-1104
North Atlantic Industries, Inc.	109
Raytheon Computer	611-612, 703-704
Redcor Corp.	326-327

data transmission equipment	
Bell System	613-615
Control Data Corp.	310-313, 310A, 313A, 406-409
Dartex, Inc.	330
Datamec, Div. of Hewlett-Packard	805-808
Digital Electronic Machines, Inc.	1315
Honeywell, EDP Div.	1001-1004
IBM Corp.	414-418, 414A, 501-505
Ohr-Tronics, Inc.	913A
Tally Corp.	903-904
Teletype Corp.	1312-1313

displays	
Brogan Associates, Inc.	207
Control Data Corp.	310-313, 310A, 313A, 406-409
Digital Equipment Corp.	1009-1012
Electronic Associates, Inc.	214-218, 214A, 301-305
General Electric Computer	713-716, 713A, 716A, 801-804
Honeywell, EDP Div.	1001-1004
IBM Corp.	414-418, 414A, 501-505
ITT, Industrial Products Div.	1317
Raytheon Computer	611-612, 703-704
Sanders Associates, Inc.	912, 912A, 1005
Transistor Electronics Corp.	319A, 328

electronic calculator	
Control Data Corp.	310-313, 310A, 313A, 406-409

the exhibitors

Mathatronics, Inc.	608
Olivetti-Underwood Corp.	1301-1302

mag tape transports

Ampex Corp.	319-323
Brogan Associates, Inc.	207
California Computer Products, Inc.	101-105
Control Data Corp.	310-313, 310A, 313A, 406-409
Dartex, Inc.	330
Datamec, Div. of Hewlett-Packard	805-808
Kennedy Company	206
Midwestern Instruments, Inc.	110-112
Potter Instrument Co., Inc.	705-707
Texas Instruments, Industrial Products Group	333

microfilm systems

Benson-Lehner Corp.	905-907
National Cash Register Co.	1013-1016, 1101-1104

plotters

Auto-Trol Corp.	334-335
Benson-Lehner Corp.	905-907
Brogan Associates, Inc.	207
California Computer Products, Inc.	101-105
Electronic Associates, Inc.	214-218, 214A, 301-305

printers

Anelex Corp.	212-213, 213A, 306-307
Brogan Associates, Inc.	207
Datamark, Inc.	1308
Data Products Corp.	1205-1208
DI/AN Controls, Inc.	324-325
Monroe Datalog, Div. of Litton Industries	710-712
Potter Instrument Co., Inc.	705-707
Teletype Corp.	1312-1313

punch & read equipment (card, paper tape)

Datamec, Div. of Hewlett-Packard	805-808
Data Machines, Inc.	1113, 1113A, 1204
Digitronics Corp.	916A
National Cash Register Co.	1013-1016, 1101-1104
Ohr-Tronics, Inc.	913A
Omni-Data, Div. of Borg-Warner Corp.	1114-1115
Photocircuits Corp.	331-332
Remex/Rheem Electronics	1213, 1214
Royal Typewriter Co., Div. of Litton Industries	1106-1108
Soroban Engineering, Inc.	603-604
Tally Corp.	903-904
Teletype Corp.	1312-1313

random access memory systems (discs, drums, etc.)

Anelex Corp.	212-213, 213A, 306-307
Brogan Associates, Inc.	207
Computer Accessories Corp.	1109A
Data Products Corp.	1205-1208
DI/AN Controls, Inc.	324-325
Electronic Memories, Inc.	410-411, 410A
General Precision, Inc., Librascope Group	913-916
Honeywell, EDP Div.	1001-1004
Magne-Head, Div. of General Instruments Co.	208-209
Potter Instrument Co., Inc.	705-707
Tech-Met, Inc.	613A
Vermont Research Corp.	602

other

Auto-Trol Corp.	334-335
Brogan Associates, Inc.	207
Digitronics Corp.	916A
General Computers, Inc.	709A
Redcor Corp.	326-327
Texas Instruments, Industrial Products Div.	333

COMPUTERS

analog	booth numbers
Applied Dynamics, Inc.	511-513
Beckman Instruments, Systems Div.	412-413, 413A, 506-507
Comcor Inc.	1303-1306
Computer Products, Inc.	509
Electronic Associates, Inc.	214-218, 214A, 301-305
Milgo Electronic Corp.	815-816, 901-902
Reeves Instrument Co.	1109-1112

digital

Computer Control Company, Inc.	201-205
Control Data Corp.	310-313, 310A, 313A, 406-409
Data Machines Inc.	1113, 1113A, 1204
Digital Equipment Corp.	1009-1012
Electronic Associates, Inc.	214-218, 214A, 301-305
General Electric Computer	713-716, 713A, 716A, 801-804
IBM Corp.	414-418, 414A, 501-505
Raytheon Computer	611-612, 703-704
Radio Corp. of America EDP	609-610, 701-702
Scientific Data Systems	314-318, 314A, 401-405
Texas Instruments, Industrial Products Group	333
Univac, Div. of Sperry Rand Corp.	210-211, 210A, 308-309

hybrid

Adage, Inc.	810-812
Applied Dynamics, Inc.	511-513
Beckman Instruments Inc., Systems Div.	412-413, 413A, 506-507
Comcor Inc.	1303-1306
Computer Products, Inc.	509
Electronic Associates, Inc.	214-218, 214A, 301-305

the exhibitors

Reeves Instrument Co.	1109-1112

SERVICES

consulting and programming	booth numbers
Applied Data Research, Inc.	1307
Brogan Associates, Inc.	207
Computer Sciences Corp.	514-515
Cybetronics, Inc.	1314
Reeves Instrument Co.	1109-1112
Tech-Met, Inc.	613A

time rental	
Computer Sciences Corp.	514-515
Cybetronics, Inc.	1314
MAI Equipment Corp.	510, 510A
Reeves Instrument Co.	1109-1112

other	
Applied Data Research, Inc.	1307
Bell System	613-615
Cybetronics, Inc.	1314
Fairchild Memory Products	813-814
IBM Corp.	414-418, 414A, 501-505
MAI Equipment Corp.	510, 510A ■

a product preview

what they're showing that's new

ANELEX CORP.
Boston, Massachusetts

Among products being shown are the model 81 disc file, the model 4000 printer being fed data via Dataphone, and the 2610 print station. From the product line of subsidiary Franklin Electronics, there will be model 120A and 2200 digital strip printers.

CIRCLE 170 ON READER CARD

APPLIED DATA RESEARCH INC.
Princeton, New Jersey

The recently-announced, proprietary software system, AUTOFLOW, for producing flowcharts on a line printer, is being shown. Accepting assembly and higher-level languages, the software performs the allocation of symbols, editing, code rearrangement, column and page allocation, and the drawing of connecting lines. The system is leased to users, and is available for the IBM 1401, 1410, and the 360's, Honeywell 200 series, and RCA Spectra 70's and 501.

CIRCLE 171 ON READER CARD

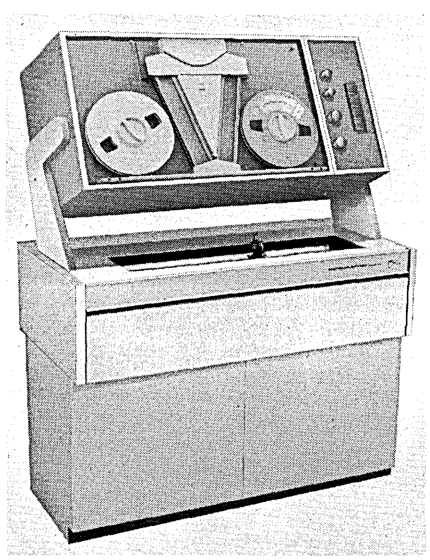
AUTO-TROL
Arvada, Colorado

The model 8030 is an all-digital machine tool director for use with existing machine tools and positioning tables. Input can be from cards, paper and mag tapes; the unit can also be operated manually. Incremental motions as small as 0.0001 inch can be accomplished. A visual display is provided for x and y value registers.

CIRCLE 172 ON READER CARD

BENSON-LEHNER CORP.
Van Nuys, California

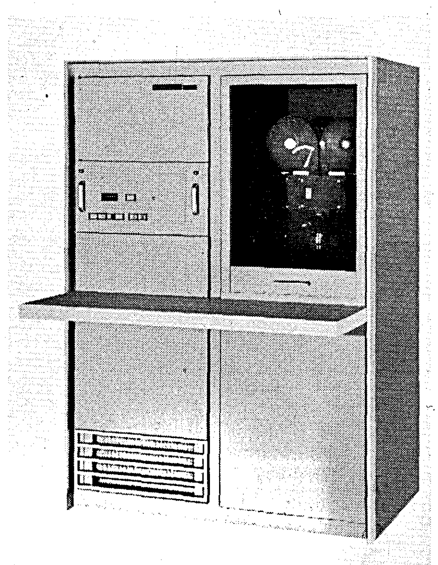
Newly-developed is a card-input Delta Incremental Plotter. The off-line unit includes the plotter, table, and card reader, and reportedly allows up to 100 steps in x and/or y from one computer command. The control unit is also compatible with all on-line plotters for reducing computer write time or to convert from on- to off-line. Another new product is the STE off-line mag tape plotter. It operates from 200- or 556-bpi 7-track tapes with either the gapped or gapless format. It can also be outfitted to run from 556- or 800-bpi tapes, and can be field-modified for 9-track tapes.



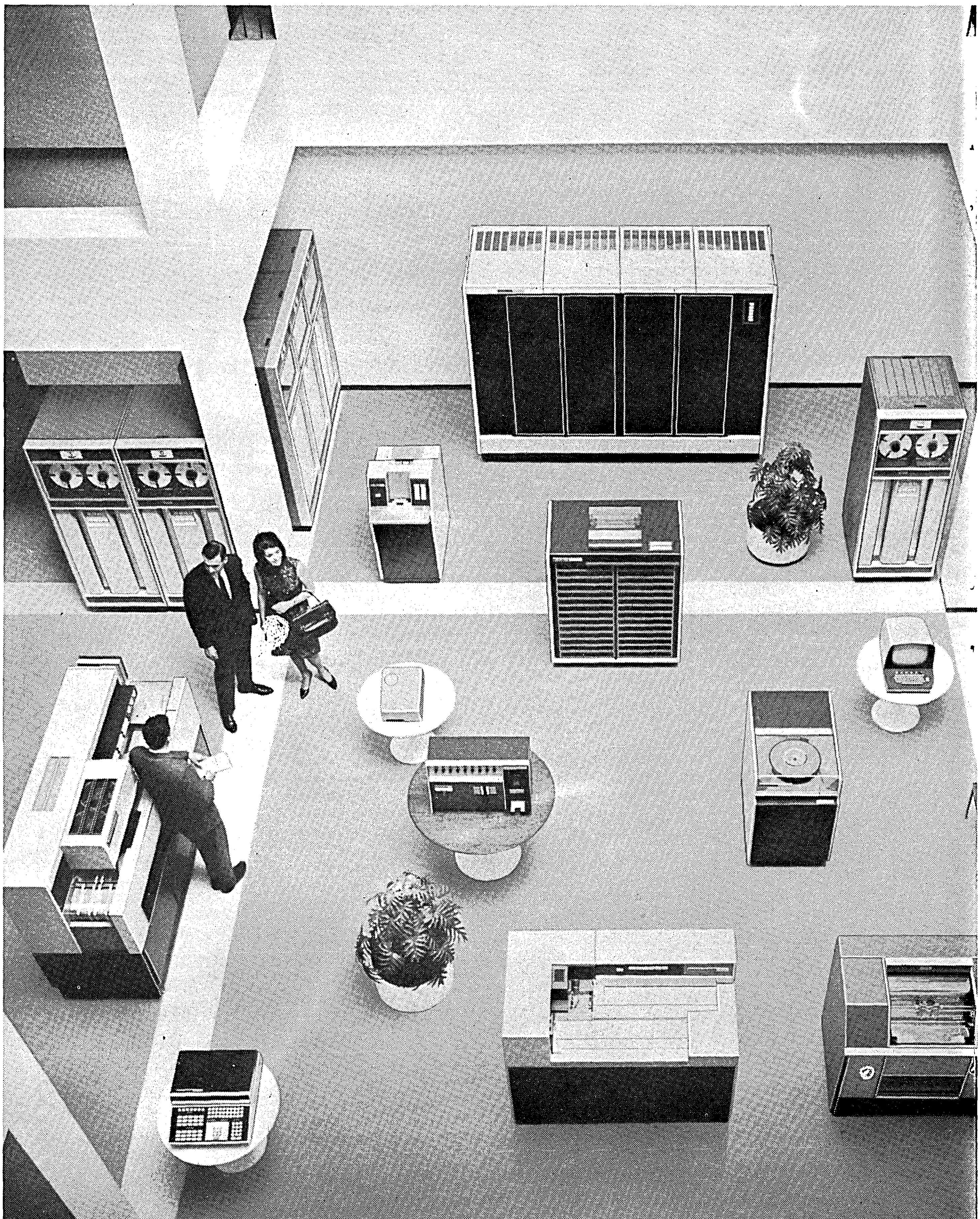
CIRCLE 173 ON READER CARD

CALIFORNIA COMPUTER PRODUCTS INC.
Anaheim, California

The model 835 being introduced is a CRT/microfilm plotting system for any computer output that can be converted to graphic form. It is a digital incre-



mental plotter designed for off-line use with the firm's mag tape drives. Input commands are accepted at up to 100,000 cps, and 35mm microfilm is produced at up to five frames/second.



SEE THESE DEVICES OPERATING IN OUR EXHIBIT AT THE S.J.C.C.

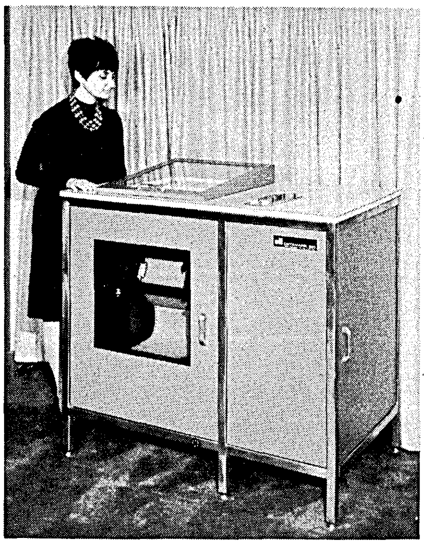
product preview

Either positive or negative transparencies are produced for direct viewing or photographic printing.

CIRCLE 174 ON READER CARD

DATAMARK INC.
Westbury, New York

New line of printers to be exhibited is the 300 Series, designed for communications terminal and small-scale computer output applications. Worst-case print speed is 300 lpm with a 64

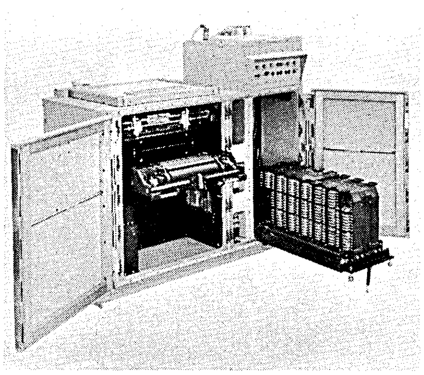


character font; also available is a 96-character font. Frame sizes are available for 80 and 132 columns, the former mountable in a 19-inch relay rack.

CIRCLE 175 ON READER CARD

DATA PRODUCTS CORP.
Culver City, California

Being introduced is the RO-280, a ruggedized line printer that operates on- and off-line under severe environmen-



tal conditions. With a character set that includes letters, numerals and symbols, it prints at up to 1,000 lpm on multicopy fanfold forms and tab cards. The print hammer consists of one moving part.

CIRCLE 176 ON READER CARD

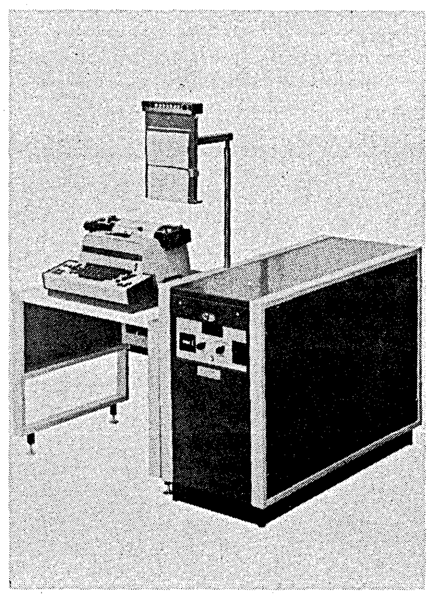
DECISION CONTROL INC.
Newport Beach, California

Being announced is a new line of more than 20 digital logic modules, the Micro VersaLOGIC series. Included are universal flip-flops, delay multivibrators, clock drivers, variety of gating configurations, and a number of pre-connected arrays: binary counters, shift registers, etc. They operate to 5 MC with logic levels ranging from 3.8 to 6 volts (true) and 0 to 0.5 volts (false) with noise rejections of over 1 volt.

CIRCLE 177 ON READER CARD

DI/AN CONTROLS INC.
Boston, Massachusetts

Three new products are being shown: a computer typesetting system (shown), a field-programmable aerospace magnetic timer, and a lister/printer. The typesetting system, model LC-3, uses a special-purpose computer to perform hyphenation, justification, and error correction before the paper tape is punched. In the error correction, one keystroke is used to erase either one letter, a word or an



entire line, obviating the production of idiot tape.

The timer provides discrete timing and interval stepping for 12 sequential events, and can be field-programmed for all 12 intervals. It uses core transistor logic elements and magnetic commutator elements to perform all logic and control functions.

The data printer has 16 columns, prints 40 lines of numeric data per second or 20 lines/second of alphanumeric information. The series DL has an ink-roller with inking capacity of more than 10 million lines.

CIRCLE 178 ON READER CARD

DIGITRONICS CORP.
Albertson, New York

A unidirectional paper-tape handler, the model 6011 handles 5 to 8-level tapes of 11/16, 7/8 and 1-inch widths, interchangeably. No adjustment is required when changing from one width to another. Spooling speed is 30 ips and rewind speed is 40 ips.

CIRCLE 179 ON READER CARD

ELECTRONIC MEMORIES INC.
Hawthorne, California

A new core memory system with a cycle time of 650 nanoseconds is the NANOMEMORY 650. It has a capacity of 16K (84-bit) words and an access time of 300 nsec. Features are silicon circuitry, 2½-D organization, and 20-mil cores.

CIRCLE 180 ON READER CARD

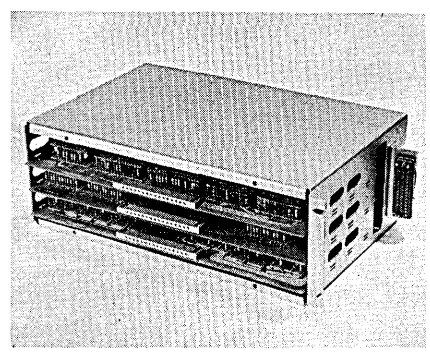
FAIRCHILD SEMICONDUCTOR
Mountain View, California

Entry of the firm into the core memory business will be featured. Shown will be a model of a microcircuit unit with a memory cell using a 16-bit version of the 36-bit cell, in addition to possibly a 2½-D memory system.

CIRCLE 181 ON READER CARD

FERROXCUBE CORP.
Saugerties, New York

The recently-announced line of 10-usec memory systems for the commercial/industrial market is being shown. First system in the line, the FX-12,



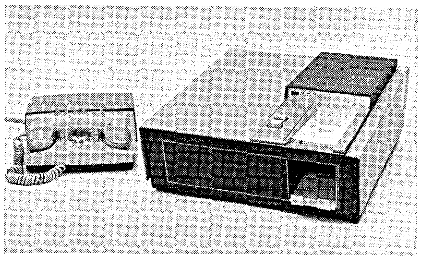
is a small memory with a maximum of 512 (8-bit) words, designed primarily for code or format conversions and speed buffering applications. Featuring all-silicon, cord-wood construction, it measures 15 x 5 x 9 inches.

CIRCLE 182 ON READER CARD

product preview

HEWLETT-PACKARD CO.
DATAMEC/DYMEC DIV.
Mountain View, California

An optical mark reader being introduced is a desk-top unit that performs alphanumeric reading with a variable card format. It is compatible with com-

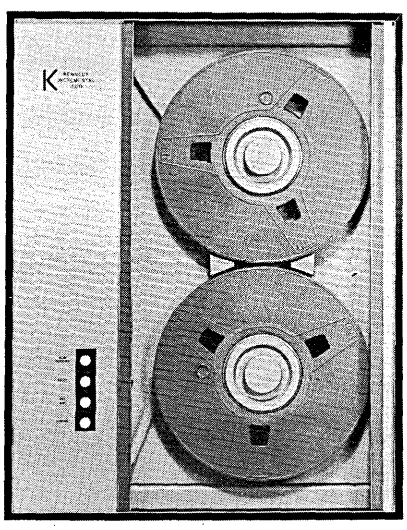


munication modems such as Dataphone, as well as mag tape and Teletypewriter devices and computers. Speed is variable according to output requirements.

CIRCLE 183 ON READER CARD

KENNEDY CO.
Pasadena, California

A new incremental recorder, the model 1500 produces 7-channel mag tape at from zero to 400 steps/second. Features include front access to circuit



cards, binary zero to BCD 10 conversion, straight-through threading, and quick-lock reel hubs. The reels are 10½-inches.

CIRCLE 184 ON READER CARD

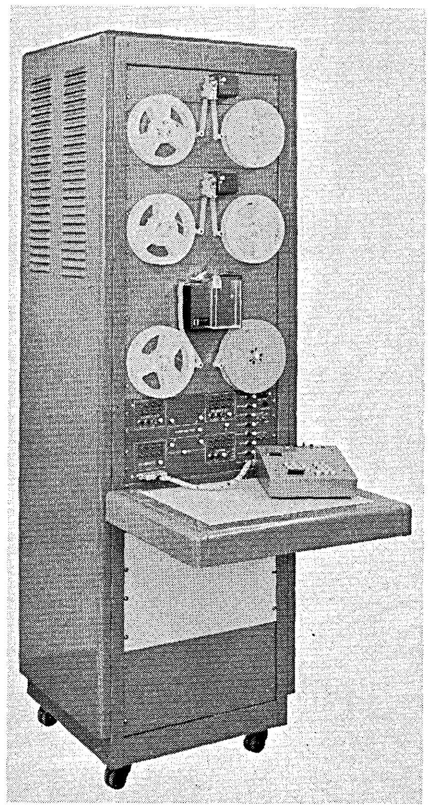
LOCKHEED ELECTRONICS CO.
Los Angeles, California

Two core memory systems are getting their first public showing. The CD 50 has a read-write cycle time of 750 nanoseconds and an access time of 300 nesec. It uses the 2½-D memory organization, has a capacity of 64K (80-bit) words. The model CI-300 is the second unit. Designed for extreme environmental conditions, it has a cycle time of 3 usec and an access time of 800 nsec. Capacity is 16K (32-bit) words.

CIRCLE 185 ON READER CARD

OHR-TRONICS INC.
New York, New York

The System 128 being shown is a complete tape preparation system. It can prepare paper tape from a keyboard (from 18 to 64 keys can be incorporated) with or without parity check, can duplicate tape, compare



two tapes and stop on an error character, can compare and duplicate, and can verify in which a previously-punched tape is compared against key entries and a second verified tape produced.

CIRCLE 186 ON READER CARD

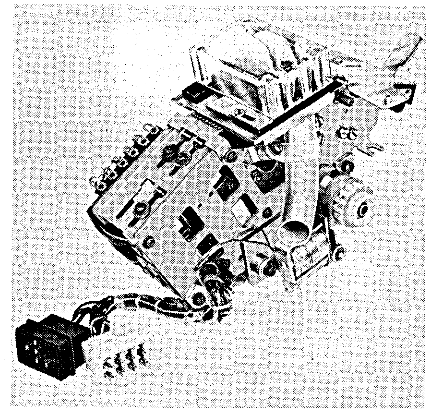
REDCOR CORP.
Canoga Park, California

Being shown is a new series of integrated-circuit hybrid computer linkage systems. Features include simultaneous sample-and-hold, 15-bit ADC capability, input and output transformer coupling, double buffer D-A register, and 100-volt output.

CIRCLE 187 ON READER CARD

ROYAL TYPEWRITER, ROYTRON DIV.
Hartford, Connecticut

Being shown are new punched-tape reader and punch mechanisms. The model 250 is a pin-sensing, wire-contact reader that operates at 17 cps asynchronously and 23 cps synchron-

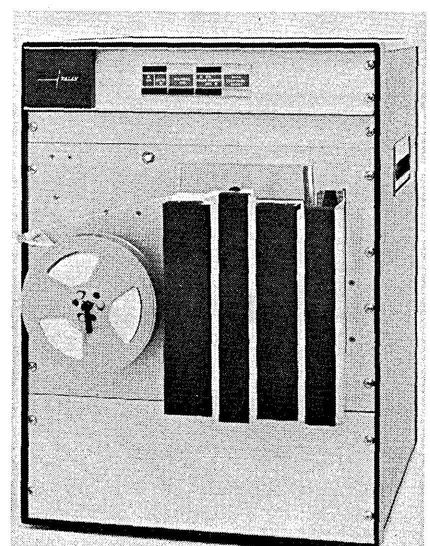


ously. It also comes as an integrated reader station. Operating at the same speeds is the model 200, which punches in accordance with the recommended American standard. This also is available as an integrated station.

CIRCLE 188 ON READER CARD

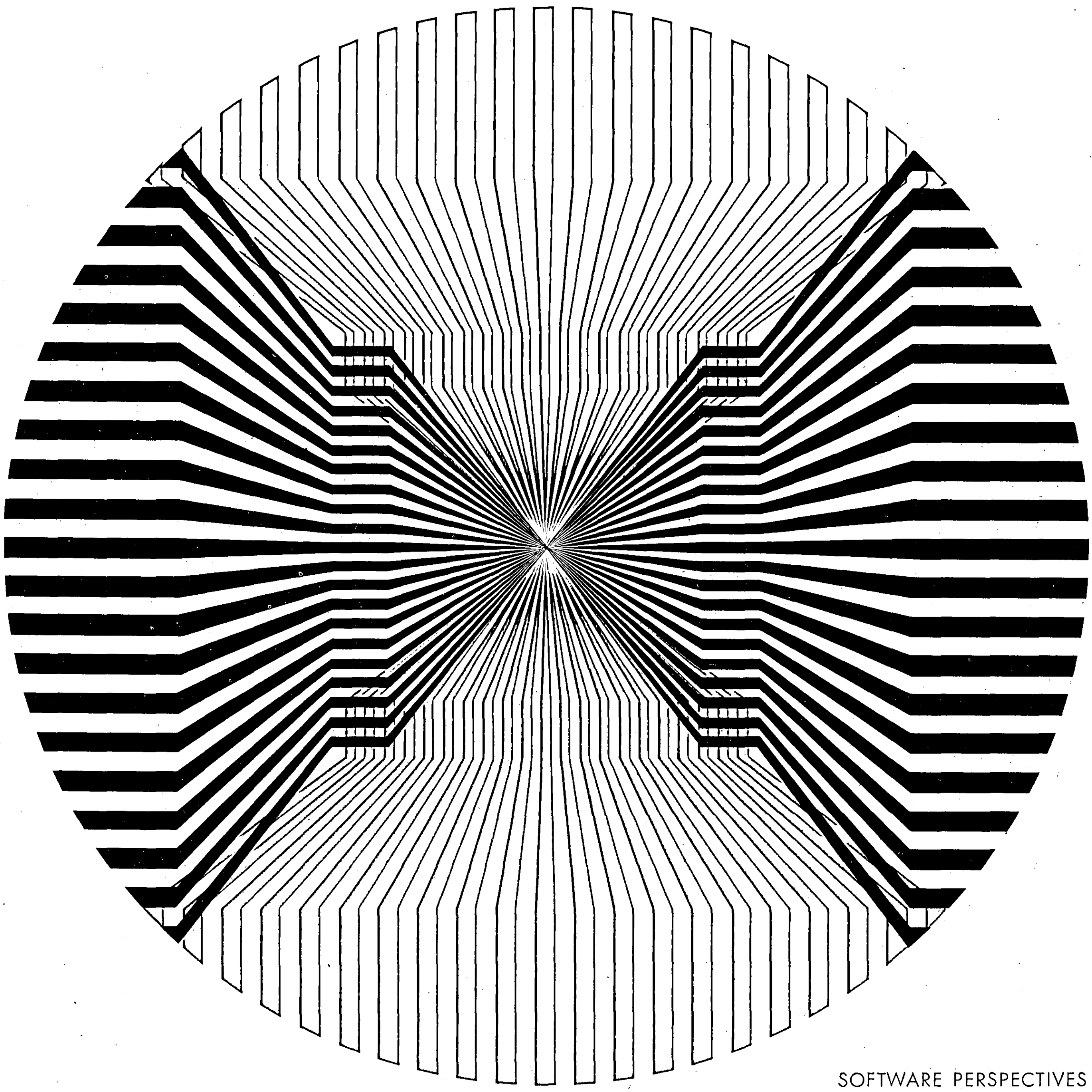
TALLY CORP.
Seattle, Washington

Paper tape communications systems being shown are the System 111 transmitter and 211 receiver. The 111 features a retransmit capability for error control, and transmits at 120 cps. It operates with the Bell 202 C-2, or



equivalent, data set, and handles 5- or 8-level tapes. The 211 receives at the same speed, checks for correct parity after it is punched, and can instruct the retransmission of an incorrect block of data. Unattended operation is another feature. ■

CIRCLE 189 ON READER CARD



the technical program

by Jack L. Mitchell

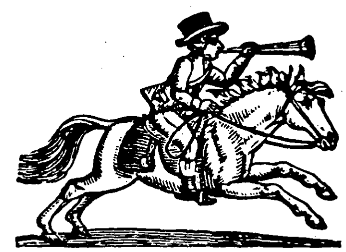
The technical program for the 1966 Spring Joint Computer Conference has been planned to represent the diversified scope of the computer field with no specific overall theme. The program was designed under the assumption that this is a general meeting where good papers on topics of relatively general interest to the information processing community should be considered and that specialized papers should be submitted to one of the journals or a smaller, more specialized meeting. Hopefully, the program will serve the interests of a major cross-section of conference attendees.

No attempt was made to fix the number of papers in a single session. Session chairmen were asked to select only those papers which they felt merited presentation; therefore, there is considerable variation in session length. In order to eliminate schedule conflicts, the afternoon has been divided into two periods. This practice proved to be successful at the 1965 FJCC.

Sixteen sessions are planned; 10 are made up of presentations of formal papers published in the conference proceedings. The formal papers were selected from those submitted in response to the call for papers, and those encouraged by session chairmen. One of the 10 sessions, Coherent Optical Information Processing, is intended to be tutorial; its aim is to familiarize computer specialists with some new techniques available in optical technology. In most sessions, a group of panelists will present a critique of the papers and attempt to place them in proper perspective. This panel will also lead the audience discussion following the papers.

The remaining six sessions are informal (no papers are published in the Proceedings). The format of the session, Display Application Research, is somewhat experimental. Each speaker will present a review of his current research, which will include a movie or TV monitor display in order to provide a realistic picture of the work. The aim is to give an attendee up-to-the-minute results such as he would receive on a personal visit to a particular laboratory. In addition, there will be panel discussions on the meanings of time-sharing, design of large computing systems, computers and a "checkless" economy, hybrid computation, and on the role of computers in present and future libraries.

the sessions



Tuesday, 1 p.m.
Grand Ballroom

Display Applications and Techniques A Panel Discussion

Chairman:
Dr. D. C. Engelbart
Stanford Research Institute
Menlo Park, California

The goals and developments in any area are influenced considerably by the image that people have of the possibilities and needs associated with the area. I happen to feel that the generally-held images relative both to the possibilities for harnessing computer-display working aids and to the corresponding needs associated with pursuing these possibilities, are much more conservative and less challenging than is merited by the current state and potential of our technology. My purpose in selecting the participants and establishing the specifications on their presentations was to do as much as possible for "expanding" the generally-held images as to possibilities and needs.

Two important features about on-line computer-display systems are: (1) the computer operations available for the user to call, and (2) the speed, flexibility, and smoothness with which these operations may be called by a practiced user. The former may be appreciated quite well by reading a descriptive paper. However, the latter aspects of the system are not so easy to communicate by writing, and their composite effect upon the usability and effectiveness of the system is quite significant.

This session is organized to bring out both of these aspects for six research projects that are exploring utilization of computer-display tools for real-life problem solving. To bring out the characteristics of speed, flexibility, and smoothness, each presentation will include either a movie or an actual real-time demonstration with TV monitor displays in the session auditorium. It was specified to each participant that the movie should be made up especially for this presentation, as a representation of the actual current state of his research. Also, to communicate most realistically the "user feel," the various delays in computer operation or user actions involved in the demonstrated processes are to be shown in their real speeds, or clearly indicated otherwise.

Since it is not too difficult to dummy up demonstration operations that can show a flashy succession of amazing display images, I want to emphasize that the presentations will show the things that can be done in line of realistic, purposeful constructive *work*. In other words, each speaker will be presenting serious working tools—if not usable now in a coordinated working system, at least being represented by him as serious candidates for same in a purposeful, exploratory research effort.

W. R. Sutherland, Lincoln Laboratories.
W. H. Ninke, Bell Telephone Labs.
T. O. Ellis and W. L. Sibley, The RAND Corporation.
Cyrus Levinthal, MIT Project MAC.
G. J. Culler, Univ. of California, Santa Barbara.

Tuesday, 1 p.m.
Babbage Room

Optical Processing Techniques

Chairman:
David A. Berkowitz
The MITRE Corporation
Bedford, Massachusetts

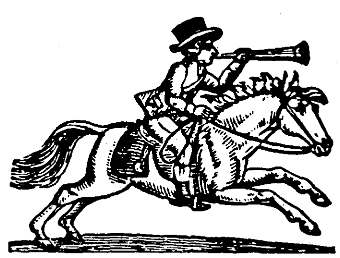
The vigorous renewal of interest in optical and electro-optical information processing occurred within the present decade. Already practical applications have been found for many of the newer techniques in input-output and peripheral computer equipments and in special purpose computers. The coherent optical techniques form a special class within the larger field of novel optical information processing techniques and they will receive special attention in this session. The coherent techniques have been used for various off-line computations. and they give promise of new storage and memory access schemes. In addition, there are developments aimed at on-line coherent optical processing which could ultimately lead to another approach to adaptive image processing.

This session will not have the panel format, but rather will have the more customary organization better suited to a descriptive and tutorial exposition of a relatively unfamiliar field.

The first paper will explore the entire field of optical and electro-optical information processing in very practical terms: what tasks can be, and have been, performed and what is promising in the future. In language meaningful to the computer man, the present capabilities will be described, and the capabilities peculiar to the coherent techniques more clearly set aside.

This paper will be followed by a mathematical and tutorial paper which presents an inquiry into the nature of coherent optical systems and how they differ from non-coherent systems. It also describes, in mathematical terms, how the development of the laser has made these systems more practical.

The third paper will discuss the optical processing of information that can be represented by two-dimensional diagrams, transparencies, etc.



This includes filtering and correlation among the possible linear mathematical operations. Examples of applications to be discussed are the simulation of complex antenna array field patterns and synthetic generation of long linear antenna arrays.

The photographic recording of the various diffraction patterns of objects illuminated by coherent light has come to be called holography. The fourth paper will discuss techniques for making good holograms and how various factors degrade the process. Holographic imagery through irregular media permits exploration of their internal optical properties. There are possible applications of three dimensional holographic recording, in emulsions and other materials, to information storage.

The final paper will discuss the application of the modern semicondutor art to the fabrication of coherent optical transducers, which could be electrically or optically controlled as a function of time. Arrays of spatial modulators fabricated as semiconductor diodes, waveguides for infrared light, and microminiature optical parametric amplifiers are feasible, and experimental examples of each will be shown.

The session hopefully covers the state of coherent optics in a thorough manner, and indicates what is in store for the future.

Computer Applications of Electro-optics, by W. J. Poppelbaum.
Basic Theory of Partial Coherence, by G. B. Parrent, Jr.
The Role of Coherent Optical Systems in Data Processing, by J. J. Cutrona.
Requirements for Hologram Construction, by E. N. Leith, A. Kozma and J. Upatnieks.
Application of Coherent Optical Transducers to Optical Real-Time Information Processing, by D. B. Anderson.

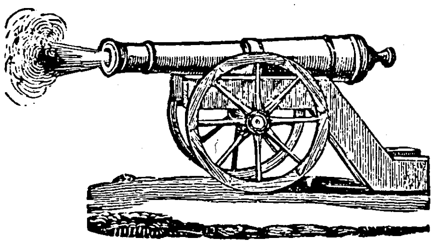
Tuesday, 3:30 p.m.
Auditorium

Trends in Time-Sharing

Chairman:
Dr. E. E. David, Jr.
Bell Telephone Laboratories
Murray Hill, New Jersey

Time-sharing is advertised widely as an economical method for allowing free and rapid man-computer repartee. The several pioneer, experimental time-sharing systems have indeed shown that this new style of computing is feasible technically and economically. In addition, they demonstrate a way of bringing man and machine to bear effectively as a unit on new classes of problems. Such problems abound, for example, in engineering design and in the statistical analysis of data where partial results, trial and error, and user-guided solutions are useful. Experience with consoles and languages has reinforced the importance of concise and effective communications between man and machine. Notably such experience has stimulated new concepts of peripheral hardware and software to match the human eye, ear, and hand. Equally important are languages oriented toward problem terminology and the specialist's mode of expression.

However, additional dividends which are less well known but perhaps



even more significant have come from these experiments. One is the "memory-centered" philosophy, which recognizes the importance of file systems to serve as software archives. These systems must play the role of both a public library and a private file cabinet, and techniques have been developed which permit just this. Adequately indexed and protected file systems are a significant step toward permanent and evolving software repositories and data banks. The new file organizations promise that, for the first time, users effectively can "stand on the shoulders" of earlier programmers.

Time-sharing experiments have pointed to the vital role of multiprogramming and multiprocessing in advanced computer system design. The former contributes efficiency through full utilization and the latter yields adequate capacity and high reliability. These techniques are basic to versatile hardware-software systems which can supply each user and task with the appropriate service; console interaction for those desiring it and production capacity with guaranteed completion time for the routine requiring that.

Hardware designs are feeling the impact of time-sharing, too. Special processors and large, fast secondary memory modules are being tailored for time-shared systems. The reality of computing systems which will be all things to all users is still ahead of us, but that goal is not nearly as remote as it once seemed. The massive hardware-software systems now being created under the catch-all phrase "time-sharing" will represent considerable progress in this direction. The performance of these systems will hinge upon thoughtful strategies for such functions as dynamic memory allocation, memory relocation, scheduling, and file organization, among others. Thus models, simulations, and performance data to provide insight into the properties of various schemes are a topical subject. This time-sharing session presents work toward this objective.

Time-Sharing in the IBM System 360, Model 67, by Charles T. Gibson.

An Analysis of Time-Sharing Computer Systems Using Markov Models, by J. L. Smith.

An Optimization Model for Time-Sharing, by Dennis W. Fife.

A Time-Shared Data Management System Using a Cross-Index File and Self-Defining Entries, by E.W. Franks.

Wednesday, 9 a.m.
Auditorium

The Meanings of Computer Time-Sharing A Panel Discussion

Chairman:
Charles W. Adams
Adams Associates, Inc. and KEYDATA Corp.
Cambridge, Massachusetts

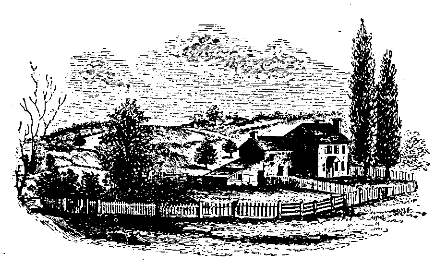
Almost every newsletter, press release and trade journal makes glowing reference to the implications of new developments in computer time-sharing technology. But they tend to ignore the fact that "time-sharing" is a broad term with a variety of meanings, ranging from the small computer used in the morning by the Physics Dept. and in the afternoon by the School of Engineering to the sophisticated message processing and page turning of the general-purpose business or scientific computer utility.

The first meaning that comes to the mind of the computer professional, perhaps, is the one first defined at MIT, in which a large-scale computing capability is put at the disposal of independent users, each treating his remotely-located Teletypewriter as if it were the console of the central facility. Through it he enters and corrects programs, supplies data and receives results without knowledge of, or concern for, the fact that the same machine is being concurrently used by others. Out of MIT's efforts, which date back seven years or more, have come highly encouraging operating experience, new software techniques, and the guidelines for new hardware developments such as now appear in the GE 645 and IBM 360/67.

During the past few years, groups at RAND, SDC and elsewhere have demonstrated impressive time-sharing accomplishments, in many cases using quite small computing systems such as Dartmouth College's BASIC system, which is implemented on relatively modest GE equipment. Profit-oriented entries into the field have appeared not only under such established banners as GE, IBM, CEIR, and Bolt, Beranek & Newman, but also under new names like Allen-Babcock Computing, Inc. And the Advanced Research Projects Agency, sponsor of fast-moving Project MAC at MIT, has continued to expand its leadership by sponsoring a study of interconnected networks of time-shared systems, the development of advanced digital graphical techniques, and the like.

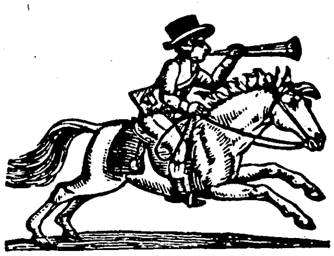
Important as these developments have been, they represent only one aspect of computer time-sharing. Specialized systems built around the need for multiple remote access to a centralized file have undergone extensive development since the early days of American Airlines Reservisor and the SAGE air defense system. Closely related to the sophisticated successors of these early systems are the store-and-forward message switching networks now in use not only by the military and the airlines but by several large corporations as well. Increasingly are the messages not only switched but also processed and responded to, a development typified by the Telecomputing Center of Westinghouse Electric Corp. An increasing number of other specialized systems, like the one operated by Bolt, Beranek & Newman for the Massachusetts General Hospital, fall into this general category.

Yet another form of time-sharing is that in which a variety of different



services, tailored to the needs of individual subscribers but not programmed by them, are provided from a central computer facility. The business data processing services offered by KEYDATA Corp. are representative of such applications. In this case the centralized processing and file storage primarily serve an economic function, to the small user it is of little consequence if the processing is done by a local device or through time-sharing. As National Cash Register, among others, well realizes, questions of convenience, reliability and price will determine whether the needs of the small businessman can best be met by centralized off-line processing of data collected at the point of sale, by small free-standing computers with random access files of a few hundred thousand characters, or by time-shared on-line processing from a central facility.

As times goes on and techniques of forecasting, simulation and strategy evaluation are improved, time-shared processors will come into their own by providing business management with the powerful tool that electronic data processing has long promised but not yet fulfilled. Exploratory work being



done at Westinghouse and at IBM's Education Center, for example, sheds light on the nature and complexity of this problem.

This panel is made up of expert, vocal representatives of several of these different applications of time-sharing. Its objective is both to delineate and establish some measure of the potential significance of each of the many meanings of computer time-sharing—a purposeful task at a time when an increasing number of people are finding such definitions needed but lacking.

James D. Babcock, Allen-Babcock Computing Inc.
L. R. Hague, Westinghouse Electric Corp.
Dr. Thomas E. Kurtz, Dartmouth College.
K. F. Powell, IBM Education Center
Dr. Ivan E. Sutherland, ARPA, Dept. of Defense.
James R. Ziegler, The National Cash Register Co.

Wednesday, 9 a.m.
Babbage Room

Simulation and Model Building

Chairman:
Geoffrey Gordon
IBM Corporation
Armonk, New York

It is virtually impossible to discuss the programming of simulation problems without talking about models. The close association of these two topics reflects the fact that the task of applying digital computers to simulation consists essentially of two parts. One part is to build a model representing the problem to be studied, and the other is programming the model.

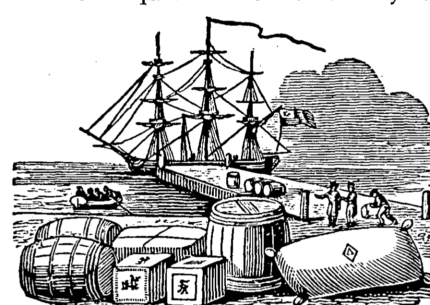
It is, of course, highly desirable to simplify the programming, particularly when the ultimate user of a simulation program is not likely to be a skilled programmer. Many developments have been aimed at easing this problem. Of particular interest are the programming systems that embody general-purpose languages specifically designed for simulation. Each such language has a certain set of concepts that must be used to build models with that language. The questions of how general purpose the concepts can be or whether there will ultimately be one or more standard sets of modeling concepts accepted by simulation users are interesting and will, no doubt, be the subject of much more programming research and development in the future. In the set of papers to be presented in this session, we will see how varied the model building concepts that users need can be. We will also hear about some of the characteristics users are looking for in simulation programming systems to simplify the use of models in the solution of problems.

The first three papers take over modeling concepts that were established first in fields other than that of digital computers. The paper by Syn and Linebarger describes a language that allows models to be described in the manner of an analog computer. This concept has, of course, been introduced before. The paper, however, describes a powerful integration of digital programming techniques with analog concepts, indicating that this type of language will be used in its own right for model building and not just as a means of transferring studies from analog to digital methods of simulation. The paper by Bartee and Lewis similarly describes a method of integrating a digital computer with the concepts of a differential analyzer. Here, however, an actual differential analyzer has been coupled with a digital computer to produce an on-line system, giving the user an unusual degree of control for running and observing the simulation. A third paper by Chang and George builds upon Boolean algebra techniques to develop a language for the analysis of logic networks.

The method described in the paper by Katz illustrates the use of SIMSCRIPT, one of the most widely used general-purpose simulation languages, used here to build a very comprehensive model of a multiprocessing computer system. In contrast, the paper by Wallace and Rosenberg treats the same subject in a different manner. Their paper makes use of Markov chains as a means of simulating systems. The paper's presence in this session may be a trifle odd since the authors offer this approach as an alternative to simulation. They show how a considerable amount of information can be gained about a complex system by applying numerical computation techniques to models of this nature without following the detailed performance of the system. Leaving aside the question of what precisely is and is not simulation, the paper serves to show how a well chosen set of modeling concepts can derive the essential facts about a problem directly.

The paper by Jacoby et al illustrates another interesting approach to the problem of providing simulation users with useful modeling tools. Here, a relatively small amount of programming, built onto a general purpose simulation language, GPSS, derives a simple program for a particular type of problem at considerably less effort than would be required to develop a compiler for a problem-oriented language designed for the type of program.

Finally the paper by Jacobson discusses some of the problems involved in applying simulation to the study of problems irrespective of the language being used. Altogether, the group of papers should be a review of simulation techniques of interest not only to

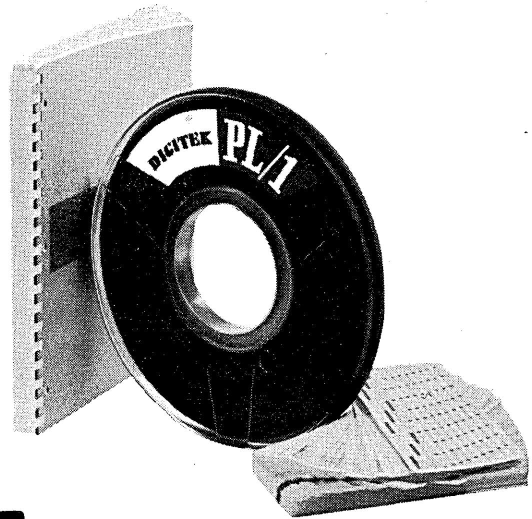


users of simulation but also to individuals interested in the development of general-purpose simulation languages.

DSL/90, A Digital Simulation Program for Continuous System Modeling, by W. M. Syn and Robert N. Linebarger.

A Digital System for On-Line Studies of Dynamical Systems, by T. C. Bartee and John B. Lewis.

Simulation of Logical Decision Networks of Time-Delay Elements by Means of a General Purpose Digital Computer, by



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FOR FABRITEK CIRCLE 61 ON READER CARD →

Decisions in

Ferrite core memories come in various wiring schemes which have inspired such nicknames as "3D", "2D", or "2½D". Manufacturing costs, memory speed and capacity, memory access requirements, and other circuitry considerations are factors which determine the "dimension" selected for a particular memory design.

This brief explanation of five typical memory types makes basic comparisons only. Each particular type fits specific applications efficiently if properly matched to cost and operation criteria.

The most simple form of core memory is the two-wire ("2D") scheme. This form is used for so-called linear-select, word-organized memories. It requires one drive line and one electronic switch for each and every word or word group in the memory and a shared digit-sense line for each and every bit of every word. It can be exceptionally fast. Another version of "2D" uses separate sense and digit lines.

The familiar and versatile four-wire coincident-current system is called "3D" and allows a broad range of memory sizes and speeds to be economically fabricated, and is also very efficient in its use of electronics.

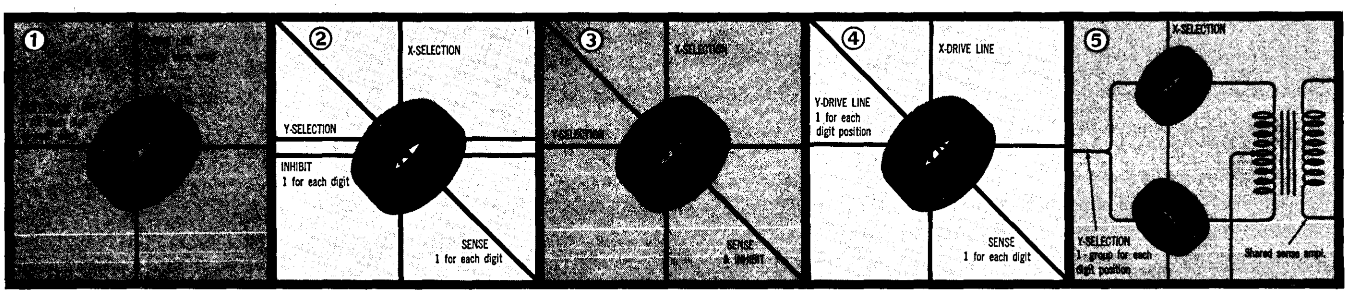
"3D" coincident-current selection can be achieved with 3 wires by sharing sense and inhibit functions on one line.

The "2½D" configuration combines some of the circuit advantages of "3D" with economies of "2D" stack construction.

One "2½D" configuration adds a separate sense line to the 2-wire scheme for a total of three wires.

Another method of achieving "2½D" with two wires through a core, time-shares the ½ read current, the sensing, and the digit writing process on one line.

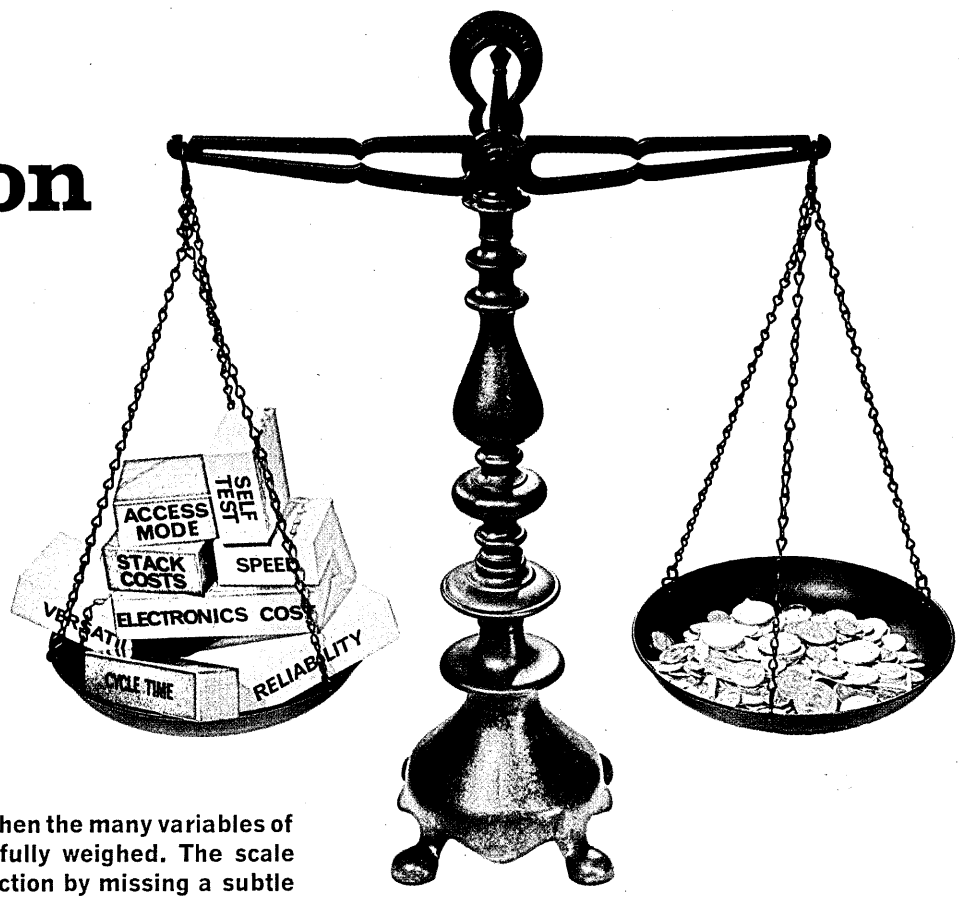
To intelligently select one of the above memory types for a particular application, the computer engineer must weigh many factors carefully. Individually considered, certain features of each are appealing, such as high speed, economy, reliability, and versatility. The final result of the "trade-offs" necessary to best match a memory to an EDP situation must be lowest ultimate cost, with every element of memory economy considered from initial design to long term maintenance.



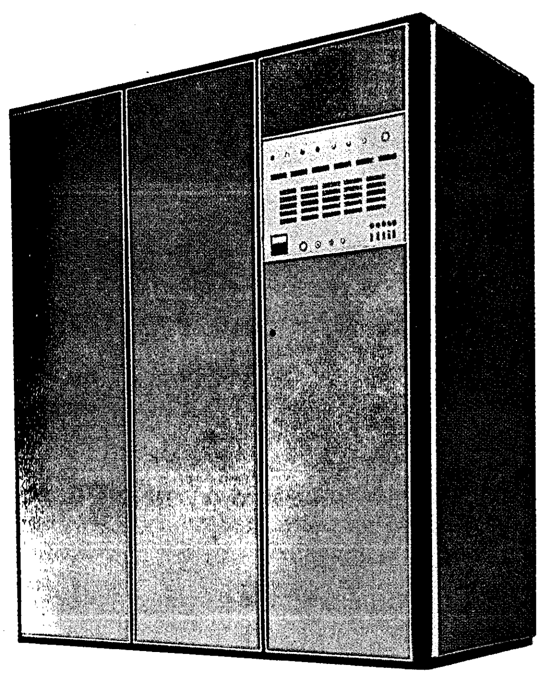
1. 2-D LINEAR SELECT — This system reads "1's" with full or greater switching current on drive line. Rewriting the "1's" is achieved by applying switching currents to both drive and digit-sense lines.
2. 3-D COINCIDENT-CURRENT — The four-wire coincident-current scheme uses coincidence of ½H currents to switch cores and an inhibit line with a cancelling ½H to prevent switching when writing "0's". A separate sense wire is used.
3. 3-D COINCIDENT-CURRENT — Three wires can achieve 3-D coincident-current selection if the sense wire shares the inhibit function. In this system, the sense line carries an inhibiting ½H current when writing "0's".
4. 2½-D COINCIDENT-CURRENT — Three wires are used in this system of "2½D" selection. ½ currents are used on X and Y lines for reading and writing but the Y line is activated with write current only when writing "1's". One X drive line is needed for every bit position to read and write.
5. 2½-D COINCIDENT-CURRENT — This type of 2-wire, "2½D" memory uses balanced sensing and time-shares the Y-axis line for ½H read current, sensing, and digit-write. The nature of this circuit also allows one of the two cores to be selected by polarity of the Y-current.

This is the fifth in a series of six brief discussions on the basic principles of memory systems. If you would like the complete series in booklet form, please circle 61 on reader card.

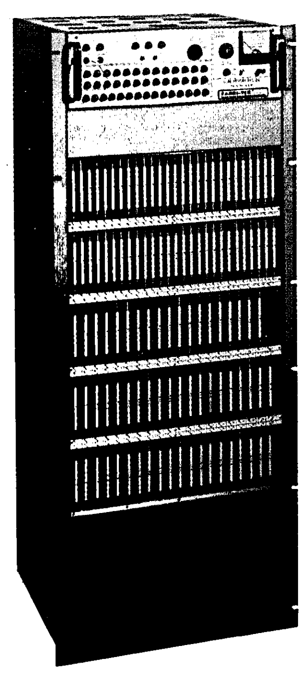
dimension



The lowest ultimate cost results when the many variables of memory type selection are carefully weighed. The scale is easily tipped in the wrong direction by missing a subtle economic factor.



Fabri-Tek's 20-million-bit mass core memory uses 2-wire, 2½-D for coincident-current versatility with 2-wire economy.



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Sixteen Basic Commands Powerful command structure for add, subtract, jumping and shifting

Microinstructions Over 100 commands which can execute four non-memory instructions in a single cycle

Literal Instructions Allow high speed, one character arithmetic or logical operations

Direct Memory Access Permits high speed data transfer between memory and external devices

Memory Protect Allows reading but inhibits writing in the protected area

Hardware Index Register Provides address modification for memory reference instructions

Flexible Subroutine Linkages A single instruction executes a transfer to a subroutine in any core bank and provides the mechanism for a single instruction return to the calling program

Four Addressing Modes Indirect, direct, relative or indexed

Priority Interrupt Channels A priority facility is included to allow external devices to command computer to transfer to specific subroutines

Memory Cycle Time 2 microseconds

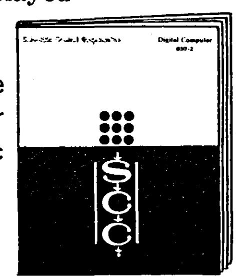
Large Memory Capacity Expandable to 32,768 words in 4,096 word increments

Fully Parallel Operation All arithmetic and logical operations are completed in parallel

Functional Control Console Addressable registers continuously displayed

Other computers available are 24 bit word (SCC 660 or SCC 670) with 2 or 5 μsec memory cycle time.

Literature available.



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the sessions

Yao Nan Chang and Oliver M. George.

Simulation of a Multiprocessor Computer System, by Jesse H. Katz.

Markovian Models and Numerical Analysis of Computer Systems Behavior, by Victor L. Wallace and Richard S. Rosenberg.

SMPS—A Tool Box for Military Communications Staffs, by Kathe Jacoby, Diana Fackenthal and Arno Cassel.

Digital Simulation of Large-Scale Systems, by Robert V. Jacobson.

Wednesday, 1:30 p.m.
Auditorium

Processing Large Files

Chairman:
John A. Gosden
Auerbach Corporation
Arlington, Virginia

This session cannot and will not begin to cover the area embraced by the title. The full title of this session should be: "A selection of three interesting projects that are only related in that each involves large masses of data, describes a technique that reduces the size of one of the problems involved, has been implemented, and should stimulate a useful and interesting discussion." The three techniques are: the automatic correction of errors in large masses of a restricted class of data, the investigation of the behavior of large-scale data systems, and the sifting of literature by professionals for interesting or relevant documents.

All three papers cover topics that should provide an interesting base for discussion. The full papers will be printed in the proceedings and the speakers will only be allowed a brief period to discuss highlights of their subjects. The discussion will be stimulated by a panelist reviewing the paper before questions and comments are entertained. It is hoped that in this way there will be time to ask questions and discuss problems. The panelists will help to ensure that the questions are pertinent and followed up.

The first paper discusses a technique to automate the correction of errors in large volumes of data. Errors in input data have been and will continue to be a source of irritation and a bottleneck when human correction is required. The techniques to be discussed rely upon some common pattern in the data. The successes reported with Christian names are encouraging.

The second paper is concerned with the problem of assisting in the design and evaluation of the design of large data handling systems. Such systems contain large files. It provides a means to test alternative design plans for feasibility and simulate on-line multi-access situations for timing. All of those responsible for large systems should evaluate the payoff of this kind of technique.

The third paper is a report on the design and experience of a system to provide people in the edp field with literature scanning facilities. It is a case of the doctor taking his own medicine. This project is something that everyone who has to keep up with his

field should be interested in, apart from the techniques of implementation.

At first thought, everyone who can justify coming to the conference in order to "keep up" should be interested, and decide if he needs such a service for himself. All three papers are practical, and of importance. The authors will discuss results as well as techniques.

Techniques for Replacing Characters that are Garbled upon Input, by Gary Carlson.

ADAM—A Generalized Data Management System, by T. L. Connors.

The Engineer-Scientist and an Information Retrieval System, by C. Allen Merritt and Paul J. Nelson.

Wednesday, 1:30 p.m.
Babbage Room

Waveform Processing

Chairman:
Dr. Bernard Gold
MIT
Cambridge, Massachusetts

In certain scientific and technological problems, information about the physical phenomenon is available as a waveform, or intensity vs time signal derived from the same phenomenon by means of a transducer. For example, a voice microphone output serves as the input to a speech communication system.

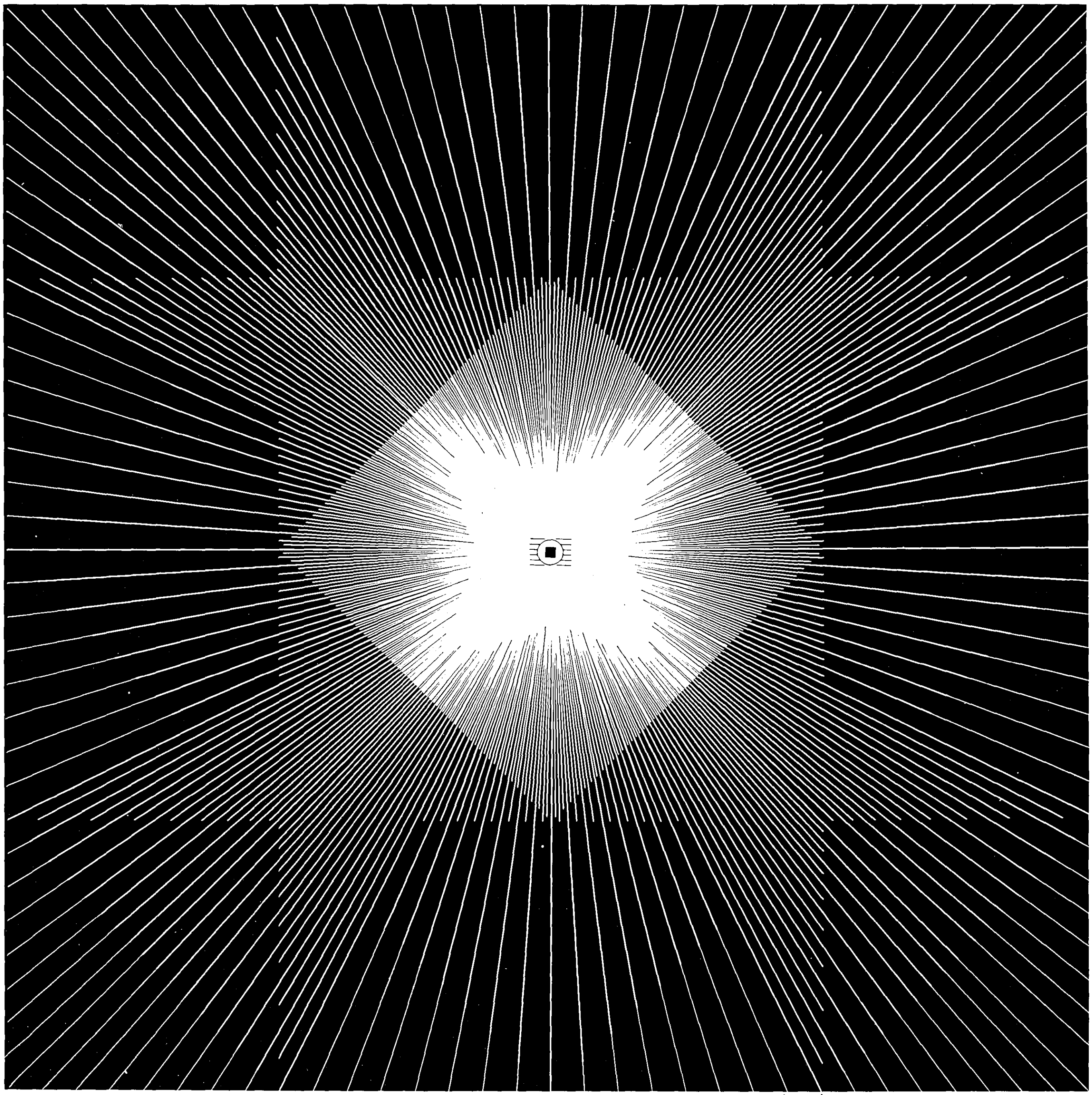
A digital computer can be helpful in providing to the scientist useful information about the waveform. This utility derives from the simulation ability of the computer. As an example, a computer can be programmed to simulate a spectrum analyzer. It can also be programmed to simulate an entire speech communication system.

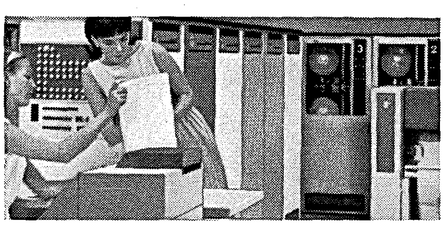
Until recently, the use of digital computers for waveform processing was severely limited because the techniques for digital simulation of linear systems, such as filters and spectrum analyzers, involved lengthy execution times. Typically, the simulation of a simple band pass filter to process one second of a speech signal would take 50 to 100 seconds of running time.

This limitation has, to a large extent been overcome by the development of new techniques. With the z-transform as a mathematical basis, a field of digital network and filter theory, whose possibilities are just beginning to be exploited, appears to be emerging.

Digital processing of signals has been applied to the study of at least three important physical phenomena: speech, seismic signals and brain waves. Experience in these three areas has shown that the success of such processing is highly dependent not only on the programming techniques but also on the nature of the computer facility. For example, it seems that long on-line sessions, direct running of the machine by the research worker, large random access tape memories and flexible input-output control can enhance the signal processing capabilities of a digital computer.

In certain instances, especially when the input signals are at very low frequencies, such as occur in the study of earthquakes, the processing equipment may consist largely of general purpose digital computers. Thus the computer goes beyond simulation of the hardware; it *becomes* the hardware. In other problems—for example, automatic recognition of spoken words—the accumulation of much data on variations among individual speakers may require that a real-time analog spectrum analyzer pre-process the





speech before entry to the computer.

What the above remarks imply is that the problems of computer processing of waveforms can be subdivided into three aspects: a) the design and use of a computer facility especially suitable for signal processing, b) the development of a theory of digital networks, and c) applications to various fields. Of these three aspects, the second seems most likely to develop as a distinct discipline.

Of the three papers listed below to be presented at this first session on the subject of Waveform Processing, two are on aspects of the programming techniques and one is on the application to the design of the data handling equipment used for the Large Aperture Seismic Array (LASA). There will also be a panel discussion on the basic design of a computer for signal processing.

Effects of Quantization Noise in Digital Filters, by B. Gold and C. M. Rader.

A Real-Time Computing System for LASA, by H. W. Briscoe and P. L. Fleck.

High-Speed Convolution and Correlation, by T. G. Stockham, Jr.

Wednesday, 3:45 p.m.
Auditorium

Programming Languages

Chairman:
Thomas Cheatham
Computer Associates
Wakefield, Massachusetts

This session will offer a most interesting and varied collection of papers and will feature a panel discussion of the ideas and issues presented through these papers.

The first paper, by Sassaman, describes a program which translates from IBM 7000 series machine language into FORTRAN. The whole subject area of machine to machine translation has, of course, received a great deal of attention over the past several years (and is receiving particular attention at this point in time when so many installations are converting to 360 and Spectra 70 machines). The paper presents the specific, and encouraging, results achieved by the author, and discusses the many issues and difficulties inherent in such translations.

The second paper, by Metze and Seshu, presents a proposal for a language and compiler for describing computers, rather than the programs to run on computers. Again, there is considerable current interest in the area of such language systems and the present paper should provide a substantial contribution to this rapidly-developing field.

The third and final paper, by Iturriaga, Standish, Krutar and Earley, is concerned with the development of the Formula Algol Compiler using the FSL Compiler Writing System. The "compiler-compiler" problem has received a good deal of attention, and this very well constructed report on the authors' experience in using such a system for the development of a compiler for a quite advanced language will be of interest to all those who are involved in the development of compilers as well as those who are interested in programming language development and extension.

The speakers and chairman will be joined by J. W. Smith of the Rand Corporation and M. Douglas McIlroy of Bell Telephone Laboratories for an informal panel discussion following the formal presentations. I am sure that these gentlemen will provide a stimulating and refreshing conclusion to the session.

A Proposal for a Computer Compiler, by Gernot Metze and Sandaram Seshu.

A Computer Program to Translate Machine Language into FORTRAN, by William A. Sassaman.

Techniques and Advantages of Using the Formal Compiler Writing System FSL to Implement a Formula Algol Compiler, by Renato Iturriaga, Thomas A. Standish, Rudolph A. Krutar, and Jackson C. Earley.

Wednesday, 3:45 p.m.
Babbage Room

Business Applications

Chairman:
F. W. McFarlan
Harvard Business School
Boston, Massachusetts

Successful computer-based management information systems usually require extensive systems development activity which is often of a quite technical nature. Unfortunately, however, the results of even the most careful design may be highly unsatisfactory unless the attendant problems associated with its implementation and integration into the firm's operations are recognized in advance and effectively

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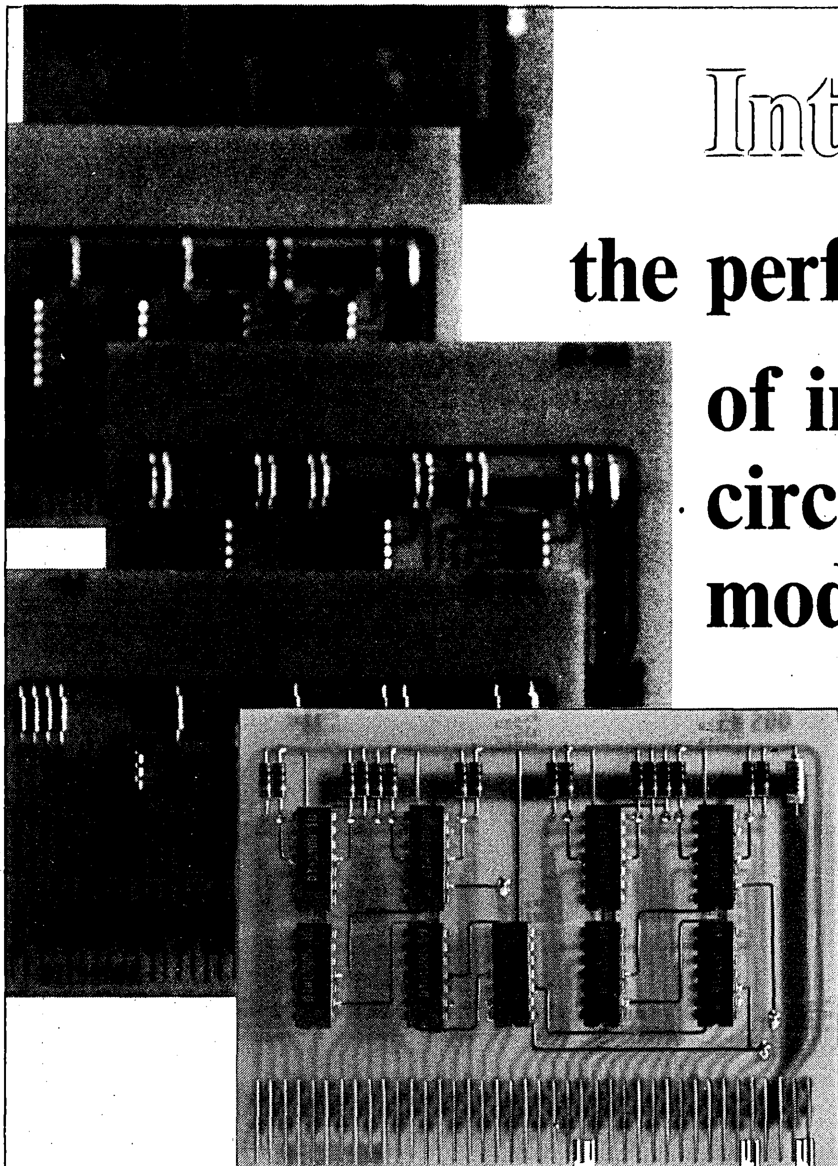

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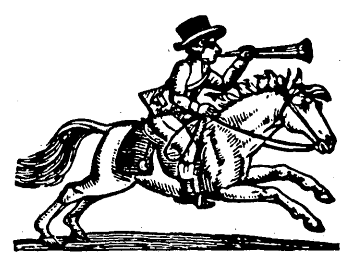
the sessions

planned for. Three papers will be presented which describe how modern information technology has been applied to specific industrial problems. The technical aspects of the systems designs presented in these papers will be of general interest. A second dimension of these papers is a description of the actual and anticipated problems incurred in making each systems operational. This topic will be developed further in the panel discussion following the presentation of the papers.

The session will start with a paper by James Gatto which describes the design of a direct mail system, whose logic is based on information retrieval concepts, and which is used to disseminate promotional material and product information to subscribers on a selective basis. Topics discussed include: structure of problem; actual organization of system; maintenance of system; and problems of implementing the system.

Use of an automatically backed-up computer system to provide a real-time audio response to telephone operators who handle toll calls in a 5-state area is the subject of a paper by Bruce Dale. Following an identification of the problem's nature, Mr. Dale describes the structure of the system's backup



features, design of the system monitor, capacity for system's growth and the project's implementation strategy.

George Duffy and William Timberlake next will describe a business-oriented time-sharing system currently in operation. A description of the system's structure, planning and training prior to its actual introduction, and indication of its principal applications will be included, together with a presentation of the peculiar systems problems inherent in its implementation.

Application of Computer-Based Retrieval Concepts to a Marketing Information Dissemination System, by James J. Gatto.

"Never-Fail" Audio Response System, by Bruce D. Dale.

A Business Oriented Time-Sharing System, by G. F. Duffy and W. D. Timberlake.

Thursday, 9 a.m.
Auditorium

The Evolving Library

Chairman:
Frank E. Heart
MIT Lincoln Laboratory
Lexington, Massachusetts

For some years it has been an article of faith that the digital computer will play a central role in recasting the information paths between people that are served by libraries. Developments in time-sharing technology seem to strengthen this faith. However, the proper mechanism and timing of this library evolution are still quite unclear. As a market for the data processing industry, the library still remains a potential rather than a reality. This session will provide a perspective view of the computer in library evolution and will highlight some avenues of progress. The discussion will include a review of recent research, a description of a specific evolving library system, and some projections about information paths of the near future. The discussion will also include a report on the research suggestions to MIT which were made by a recent major interdisciplinary conference on information transfer.

Libraries and Machines—A Review, by Dr. Burton W. Adkinson.

Coordinated Information Processing in Three Medical Libraries, by Frederick G. Kilgour.

Plans for Information Transfer Experiments at MIT, by Dr. Carl F. J. Overhage.

On-Line Information Networks, by Dr. J. C. R. Licklider.

Thursday, 9 a.m.
Babbage Room

Current Developments in Peripheral Hardware

Chairman:
Rudolph Klein
Univac Engineering Center
Blue Bell, Pennsylvania

Electro-mechanical peripheral hardware has always been an important part of "electronic" computing systems. At first this hardware was largely borrowed from other fields as main development emphasis was concentrated on new processor and memory techniques. As the computer field matures, however, the inadequacy of some of the borrowed approaches is apparent in terms of high manufacturing and maintenance costs, and poor long-term reliability in customer service. These factors have an important effect on sales and profitability.

Bulk data storage can still be accomplished most economically by electromechanical devices—i.e., magnetic tape, drums and discs. Tab cards remain extremely popular in customer applications associated with nearly all commercial installations. The importance of hardware to perform computer peripheral functions is now paramount as many modern systems contain large quantities of this gear used as communications terminals and for on-line mass storage, in addition to the conventional input/output devices. Well over half of system cost can often be attributed to peripherals.

The realities of the present-day computer business demand electromechanical gear of not only improved functional capacity, but also lower maintenance cost and extreme reliability. This session is intended to cover the type of design philosophy now emerging in the industry, as well as examples of new developments with improved functional characteristics. Papers covering new tab card devices, a high-performance incrementing tape transport, and a giant capacity random access storage unit will be presented. Session emphasis is on the engineering design decisions made and solutions to problems encountered during development of these new devices which are intended to meet the stringent demands placed on modern computer peripherals.

A New Look in Peripheral Equipment Design Approach, by Earl Masterson.

A Serial Reader Punch with Novel Concepts, by David W. Bernard, Ronald F. Borelli, Frank V. Thiemann and Frank A. Digilio.

IBM 2560 Multi-Function Card Machine, by C. E. Spurrier.

A New Development in the Transmission, Storage and Conversion of Digital Data, by R. P. Burr, John J. Rheinhold and Roy K. Andres.

IBM 2321 Data Cell Drive, by Allan F. Shugart.

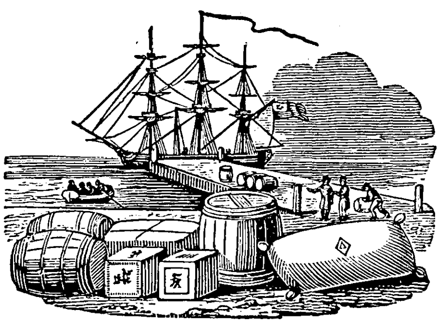
Thursday, 9 a.m.
Grand Ballroom

Analog/Hybrid Techniques

Chairman:
Mark E. Connelly
MIT Electronic Systems Lab.
Cambridge, Massachusetts

The analog/hybrid session this year indicates clearly the growing maturity, sophistication, and scope of combined analog and digital computation techniques. Successful hybrid applications will be described, based on such diverse topics as a nuclear reactor, a helicopter, a distillation column, a free piston engine, displays, and the data processing of seismic, sonar, and biomedical signals. Very evident in all of the papers is an increased emphasis on the high-speed, iterative capabilities of analog equipment. The continuing search for analog-digital combinations that most efficiently meet the requirements of various classes of problems is likewise evident.

The utilization of simulation techniques to provide intellectual leverage in a broad range of scientific and technological investigations is gratifying, but such diversity also has its drawbacks. Genuine contributions to simulation technology itself are often obscured by the specialized language and models employed by specific disciplines. The 1966 Analog/Hybrid session will provide an interesting measure of whatever mutual incomprehensibility already exists between separate



branches of the simulation fraternity.

The next benchmark in the evolution of hybrid simulation facilities is most probably a single digital computer interfaced to service several analog real-time problems simultaneously. The United Aircraft Research Laboratories, which has already put such a facility into operation, will report on its organization and performance in a very timely paper.

In conclusion, as problems get more complex and the bag of computation tricks gets more burdensome, earlier predictions of push-button problem solving and painless programming seem to have gone out of style, replaced by the sober realization that human competence, judgment, and care are as necessary as ever to get credible results.

Hybrid Simulation of a Free Piston Engine, by R. E. Gagne and E. J. Wright.

A Time-Shared Hybrid Simulation Facility, by R. Belluardo, R. Gocht, and G. Paquette.

Hybrid Simulation of a Helicopter, by W. J. Kenneally, E. E. L. Mitchell, I. Hay and G. Bolton.

Hybrid Analog/Digital Techniques for Signal Processing Applications, by Thomas Hagan and Robert Treiber.

Hybrid Simulation of a Reacting Distillation Column, by R. Ruszky and E. E. L. Mitchell.

Transient Neutron Flux Distribution Studies by Compressed and Real-time Computer Complexes, by J. E. Godts and A. S. Weinstein.

Thursday, 1 p.m.
Auditorium

Resource Allocation
A Panel Discussion

Chairman:
Peter G. Neumann
Bell Telephone Labs.
Murray Hill, New Jersey

A multiprogrammed multiprocessor computing facility may be viewed as a pool of resources containing processors, diverse storage media, and input-output equipment. In the past, many of these resources have been managed independently of one another. In order to obtain flexibility and efficiency in the use of multiprocessor systems, however, it is becoming increasingly essential that all resources be managed in a completely coordinated way. The burden must thus fall on a set of utility programs (i.e., a supervisor) and not on the average programmer. The starting point for this panel discussion is the notion of an integrated approach to the allocation and general management of all computer resources. Particular aims are to examine the significance of the interactions among resources, to explore possible useful ap-

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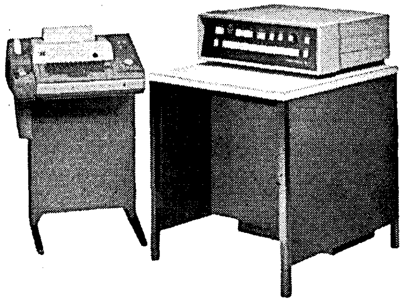


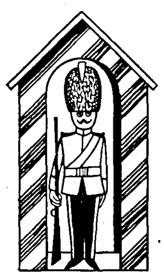
WORD LENGTH — small, scientific computer manufacturing costs are almost linearly proportional to word length. What is the optimum word length? Here are the critical considerations: accuracy and efficiency of data representation; a desirable instruction repertoire; efficient and simplified programming that goes with a directly addressable memory; and suitable architecture for supporting advanced software.

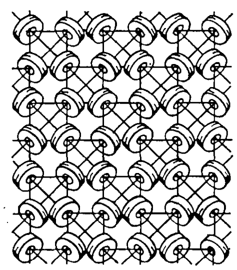
We chose an 18-bit word for our H21 real-time control computer. It gives a data resolution of one part in 262,000 —and packs three alphanumeric characters into each word. The extra bits provide for a larger, more powerful instruction set. And a single word instruction directly addresses a full 8192 word core bank making programming straightforward and efficient . . . no cumbersome, memory wasting addressing schemes, such as paging, double word instruction modes, relative addressing, etc. are necessary.

18BitS

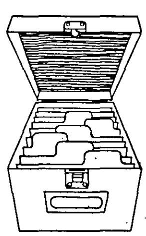
PARITY—it adds a bit to the word length. But it's well worth the investment. Past experience has shown parity to be valuable in ensuring proper system operation and safety. It's also a time-saving maintenance tool. It's a standard feature in the H21.

MEMORY GUARD—a new concept in real-time systems. This feature allows critical system programs (executives, monitors, etc.) to be guarded. Once guarded, a program is protected against accidental modification by undebugged, unguarded programs. Since each word carries its own guard bit, we now have a 20-bit word length . . . and a new dimension in system utility and reliability.

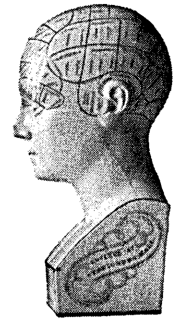




HARDWARE INDEXING—everything an index register can do, programmers can simulate with subroutines. But the tedious and time-consuming programming effort, and the extra memory required, result in false economy. Who cares how much extra memory you have to buy after you've bought the machine? We care . . . we include a "full use" hardware index register to ensure program efficiency.

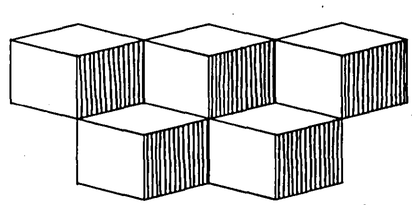


BULK MEMORY—a moving head disc file is cheaper than a head per track. And *less reliable*. And *slower* . . . (moving head disc files have long access times, normally 10 times that of fixed-head discs or drums). In high-performance, real-time systems, fast bulk memory is desirable to simplify system programming. Also core



memory requirements are reduced since fewer programs have to reside permanently in core.

COMPUTER INTERFACE—manufacturing costs could have been pared by building a minimal interface—singular I-O connector, low power bus drivers, etc. But this only defers the cost, multiplied several times, to the user at the time of system tie-in. Therefore, we include multiple I-O connections, husky bus drivers (75ma) and a generous set of clocking and control signals. The H21 interface even packs and unpacks characters into or from memory. The results . . . simple and economic interfaces for real-time systems.



PRICE—the lowest for computers with this capability. For just $21,000 you can get a central processor with 2K memory, and an I-O typewriter with tape punch and reader. An 8K system (that's 8192 words) costs only $32,000. And the delivery is good . . . try us.

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proaches to the overall problem of resource management, and to evaluate the hardware and software implications of these approaches.

A partial example is provided by the storage resources, for which an integrated approach is already beginning to emerge. In particular, consider all those storage devices (e.g., core, on-line secondary and certain off-line devices such as tapes used to extend the on-line secondary) for which storage may be allocated by the supervisor. In general, it is desirable that the actual residence of any piece of information on such a device should be totally unknown to any program outside of the supervisor. This is, in fact, achievable by designing hardware that permits the separation of the notion of residence from the notion of address. In such a design, the non-supervisory program is aware of only a logical address, which the supervisor then converts to a physical address known only to itself.

The complete coordination of all storage management is a step in the desired direction. A second and similar step is the complete coordination of all input and output management. However, these steps are fairly small in comparison to the effort of coordinating all resources at once. The real difficulty is that storage allocation, input-output allocation and processor allocation (more commonly called scheduling) all interact strongly with one another. This is especially true in a dynamically-mixed environment with interactive and noninteractive users, some of whom have by pre-arrangement been guaranteed special services.

A simple example should suffice to introduce the nature of the difficulty. Consider a program which requires six tape drives and enormous core buffers in order to run, and which in addition requires vast amounts of processor time. If all the necessary resources were allocated at some particular time, would system performance for other users remain adequate? If so, might system performance be unduly degraded at some subsequent time? Suppose that the program eventually requires four more tape drives and more core buffers. Can the system afford to satisfy this new request? Can it afford not to satisfy the request, in view of the resources already committed which must thus remain unavailable to other users? This example gives only an inkling of the problems involved.

In summary, the subject of the panel discussion is what might be called the generalized multi-resource scheduling problem. Although this problem is still somewhat ill-defined, it is of rapidly growing significance.

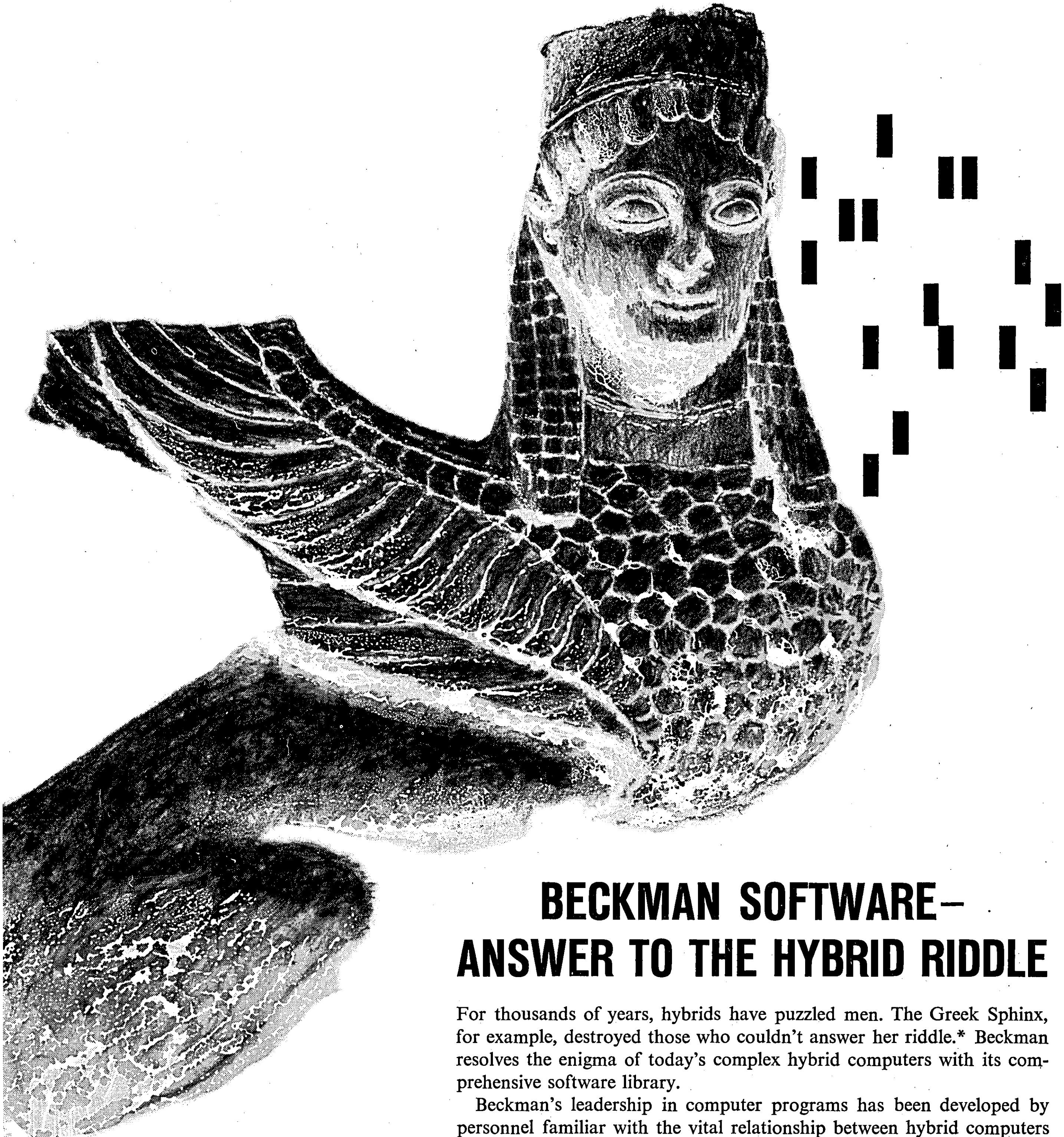
Charles R. Blair, Dept. of Defense.
Edward L. Glaser, MIT Project MAC.
Theodore Kallner, IBM.
Victor A. Nyssotsky, Bell Telephone Labs.
Stephen MacD. Warshall, Computer Associates.

Thursday, 1 p.m.
Babbage Room

Computer Techniques in Pattern Recognition

Chairman:
Oliver G. Selfridge
MIT Lincoln Laboratory
Lexington, Massachusetts

This session describes a broad spectrum of current work in automatic or machine-aided pattern recognition. The emphasis has been on programs that actually are in operational status, and preferably are of actual assistance to someone whose primary concern is not



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CIRCLE 53 ON READER CARD

the computer; another general requirement on the papers is that results have been obtained instead of hopes or plans or promises. As a result, the level of sophistication of the programs is less than many of the discussions of the past decade. But the programs provide one thing that discussion cannot, and that is a certain amount of feedback from experience on real problems. One may get a feeling that there is no universal symbolic approach to the problems of machine pattern recognition, so differing do the techniques seem to be. The first four papers are treated critically by a devil's advocate in the fifth paper.

Pattern Recognition Studies in the Biomedical Sciences, by Robert S. Ledley, John Jacobson, Marilyn Belson, James B. Wilson, Louis Rotolo and Thomas Golab.

A Chess Mating Combinations Program, by George W. Baylor and Herbert A. Simon.

Multidimensional Correlation Lattices as an Aid to Three-Dimensional Pattern Reconstruction, by Samuel J. Penny and James H. Burkhard

A Pattern Recognition Technique and its Application to High Resolution Imagery, by R. D. Joseph and S. S. Viglione.

Review: The Devil's Advocate, by Marvin L. Minsky.

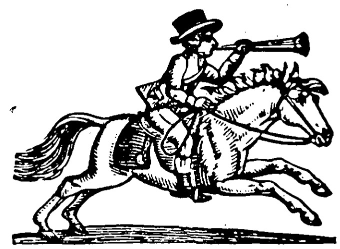
Thursday, 3:30 p.m.
Auditorium

Development of a "Checkless"—"No Money" Economy A Panel Discussion

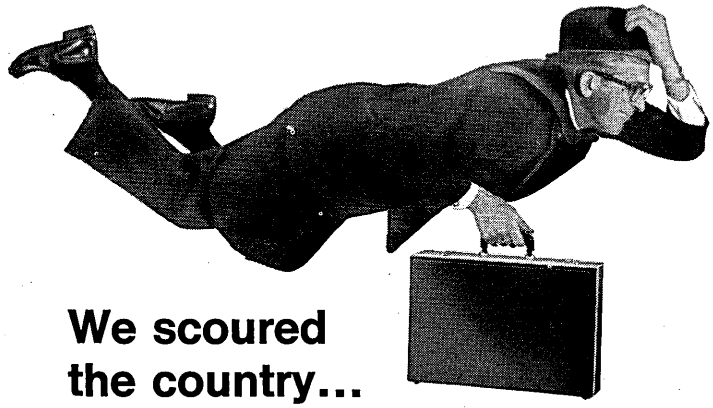
Chairman:
Dale L. Reistad
The American Bankers Assn.
New York, New York

One of the favorite topics of the "blue sky" philosophers in recent years has been the gradual evolution of a "checkless" or "no money" economy. This checkless economy they envisage would be built around a network of ultra-sophisticated computers linked in an on-line/real-time system for all types of financial, credit information, and retail institutions in the country.

As happens so often these days, "blue sky" systems of the past (such as those of Neal J. Dean of Booz, Allen & Hamilton, Inc., dating back to 1957) have become feasible as a result of technological developments. Today all of the major parts of the "checkless" economy system are in being, although they are still not connected in a manner which could replace the check writing operation that we have grown accustomed to. A major New York bank, for example, has completed a two-year study on the non-return of checks which proves that it is not necessary to return checks to customers.



A Delaware bank, working closely with IBM and AT&T, has designed a system in which their customers can charge items or transfer cash by using a plastic identification card and a Card Dialer Touch-Tone telephone connected to the bank's computer. Several large credit bureaus are now either completely computerized or are in the



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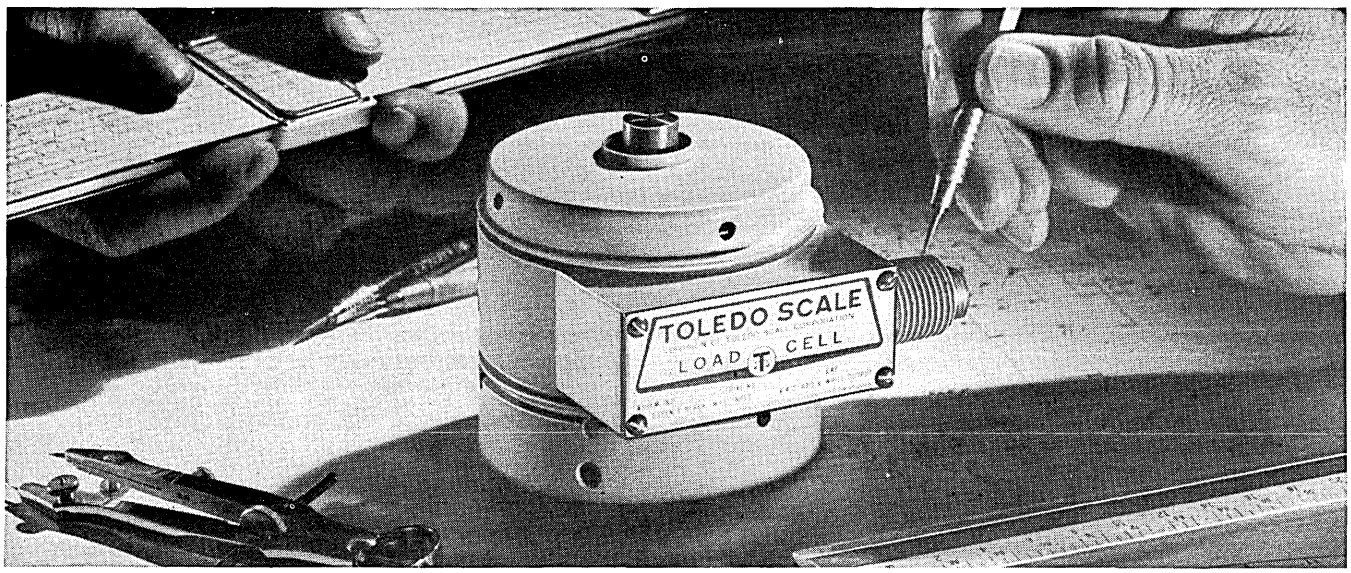

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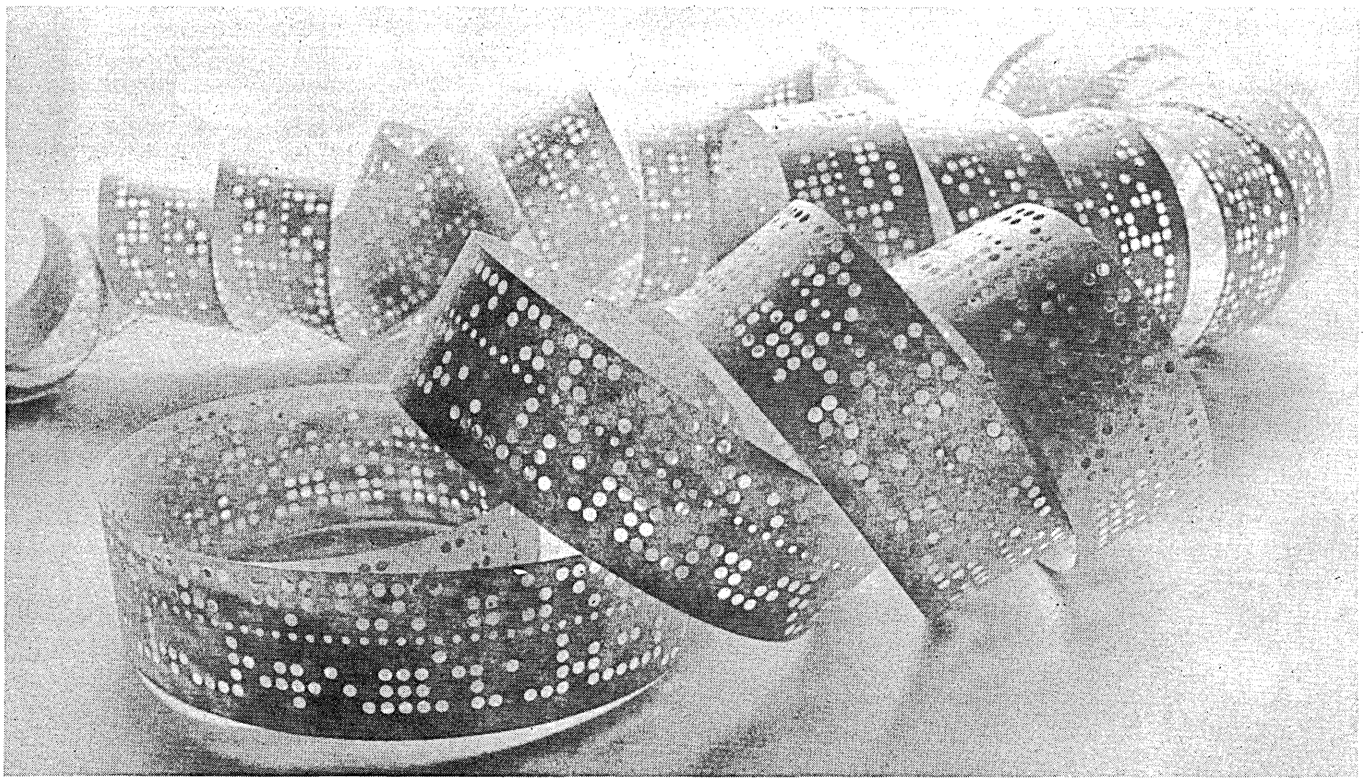
Since no other load cell can touch it in tough applications, you'll want to use it for those easy jobs, too. Write us for specifications.

TOLEDO SCALE SYSTEMS DIVISION

TOLEDO SCALE, TOLEDO, OHIO 43612

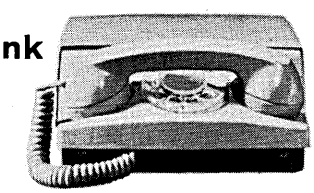
Who knows what our ingenious systems engineers will come up with next? One thing is certain, though. You should talk to them if you have a problem in measurement, material handling, control or data processing.

CIRCLE 56 ON READER CARD



Clark Equipment Company gets data from 127 sales offices, 4 manufacturing plants, and a major warehouse as soon as it's recorded

Bell System communications is the vital link



Bell System data communications services link Clark's distant locations to a centralized computer center at Buchanan, Michigan. The result is better management control of all activities—sales, inventory, purchasing, production, payroll and accounting.

With current and accurate information, Clark management can quickly adjust to changing marketing conditions. Important orders get priority scheduling for production and shipment. And yet, purchasing, production and inventories stay at optimum levels.

An integrated information system of this size uses computer switching with store and forward capabilities. The fully automatic Clark system polls satellite stations, receives and transmits messages, assigns priorities, and converts different speed and code formats to one standard code. Other features of the switching unit provide the necessary supervisory control of the network.

Consider the economies a real-time, integrated information system can bring to <u>your</u> business with automatic data processing linked with fast, reliable communications.

Today's dynamic competition requires many companies to consider organizing for data processing in some phase of their operations. It's important to start organizing communications at the same time.

So when you think of data communications, think of the Bell System. Our Communications Consultant is ready and able to help you plan an integrated information system.

See the latest in data communications.
Visit the Bell System exhibit at the Spring Joint Computer Conference.

Bell System
American Telephone & Telegraph
and Associated Companies

It's the talk of the industry . . .

Whatever "language" your present input or output machines speak – punched card or tape, optical or magnetic – the new low-cost NCR "500" computer systems can understand them. (That's an NCR exclusive.)

Applied to your Vendor Accounting operation, this means a "500" Series computer needs no translating step to communicate with your input or output equipment. Translating steps are costly; a recognized nuisance.

NCR offers you complete, total data processing systems designed and built to work hand in glove with all of their components.

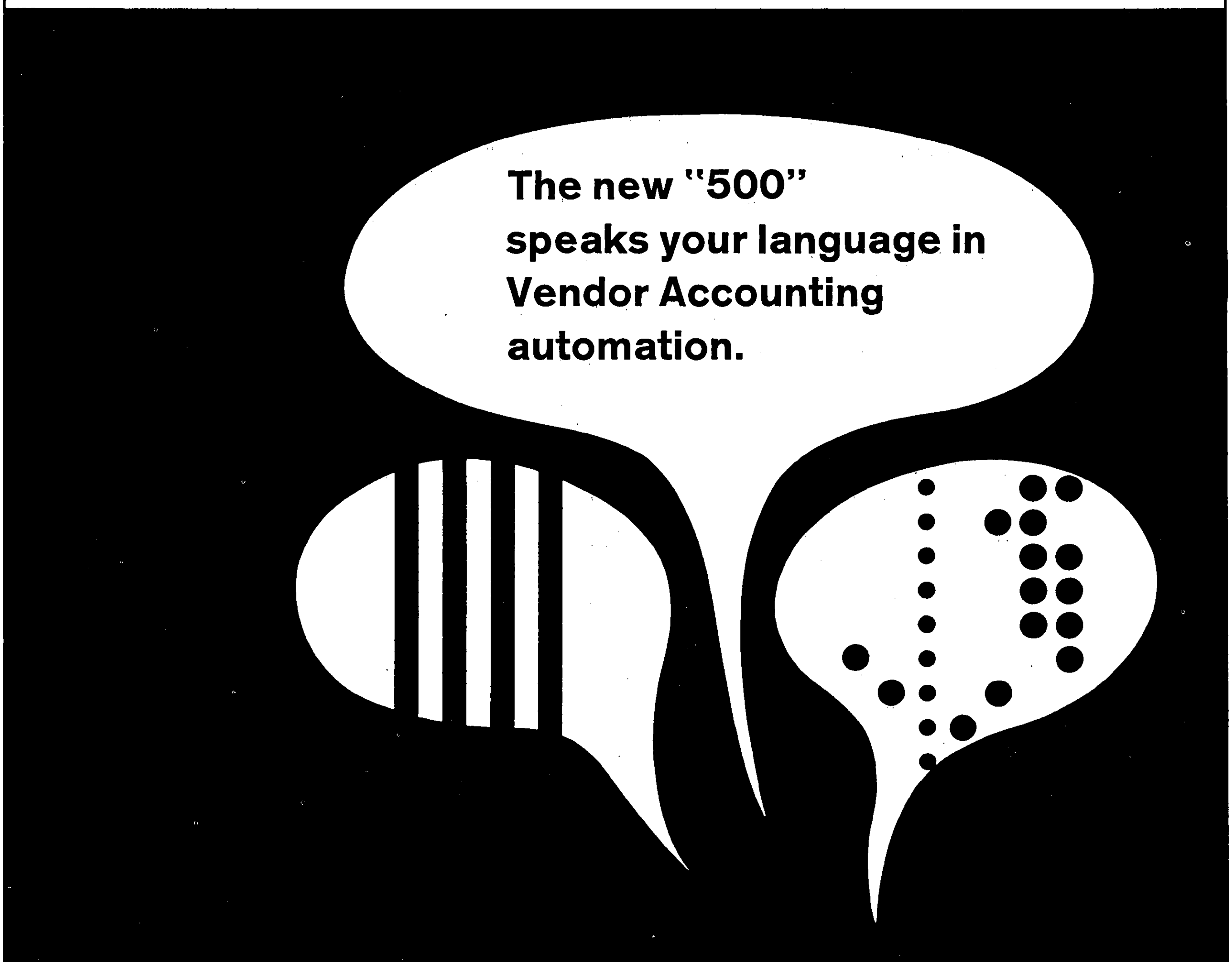
Accounts Payable can be one of the most complex and demanding of accounting applications. But the "500" handles the job with ease.

It provides (1) control over total system, orders, receipts, payments and commitments; (2) audit trail . . . certification of proper accounting procedures and processing pertinent data; (3) voucher . . . verifies calculations, rejects invalid entries and improper vouchers; (4) Disbursements . . . forecasts requirements, earns discounts, writes checks; (5) Distribution . . . proves expense, inventory, general ledger, allocations; (6) Reports . . . exceptions, cash requirements, vendor analysis.

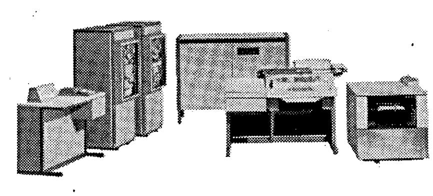
And it does all this with a minimum of personnel, forms, supplies, equipment complexities, computer runs, and (very important), minimum computer costs.

A complete magnetic ledger NCR "500" computer system for Vendor Accounting rents for as little as $765 a month . . . or $1,195 for card system.

Now are we talking your language?



NCR



THE NATIONAL CASH REGISTER COMPANY ® DAYTON, OHIO 45409

CIRCLE 57 ON READER CARD

process of conversion, signaling the start of automation in that sleeping giant, that information utility of the future. The subject of the "checkless" economy has now become popular for thesis writers, including a team from the Harvard Business School that is particularly interested in the emerging integration of the computer, data transmission, and financial interchange sectors of this development.

Neal J. Dean, Booz, Allen & Hamilton
John McCleary, IBM.
Richard Bez, AT&T.
Robert Whitby, Harvard Business School.

Thursday, 3:30 p.m.
Babbage Room

Hybrid Computing Installations A Panel Discussion

Chairman:
W. J. Quirk
The Boeing Company
Huntsville, Alabama

Composed of staff members from three different hybrid installations, this panel was chosen to promote an interchange of concepts and techniques employed by operating hybrid computer facilities. A spirited discussion about trends and applications of hybrid computing by some of the leaders in the field should be expected by all attendees.

Each installation will introduce its facility to acquaint the audience with its capabilities. This introduction will contain, but not be limited to: equipment layout and pertinent hardware operating characteristics, software characteristics, application programs, and computer checkout philosophy.

The presentation by each facility will, due to time limits, dwell only on the major points of their installation, but it should give uninformed listeners a good idea of the operating environment of the facility.

The panel discussion should be very informative and helpful to anyone considering the installation of a hybrid computer. In addition, it will point out the trends of the industry in this area and provide manufacturers and suppliers with goals to meet to satisfy the users.

Ralph Belluardo, Gerald Paquette and Ronald Gocht, United Aircraft.
Don Augustine, Mark Fineberg and John Clancey, McDonnell Aircraft.
Chan F. Hansen and William Pierce, The Boeing Company. ■

a boston promenade

by James Peacock

avenues & appetites

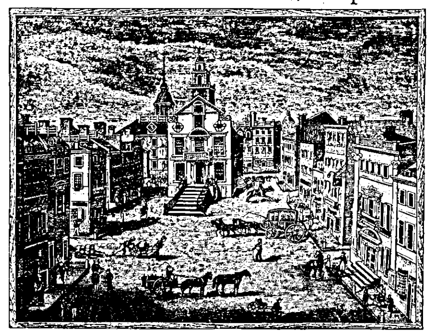
Boston bureau manager for* Business Week, *Mr. Peacock covered technology from New York before moving to New England. A mathematician-turned-journalist, he continues to follow the information-processing field.

Boston's not the town it used to be. Scollay Square's no longer there, redevelopment touches most portions of the city, and the air of change is best illustrated by the new complex in which the SJCC is being held.

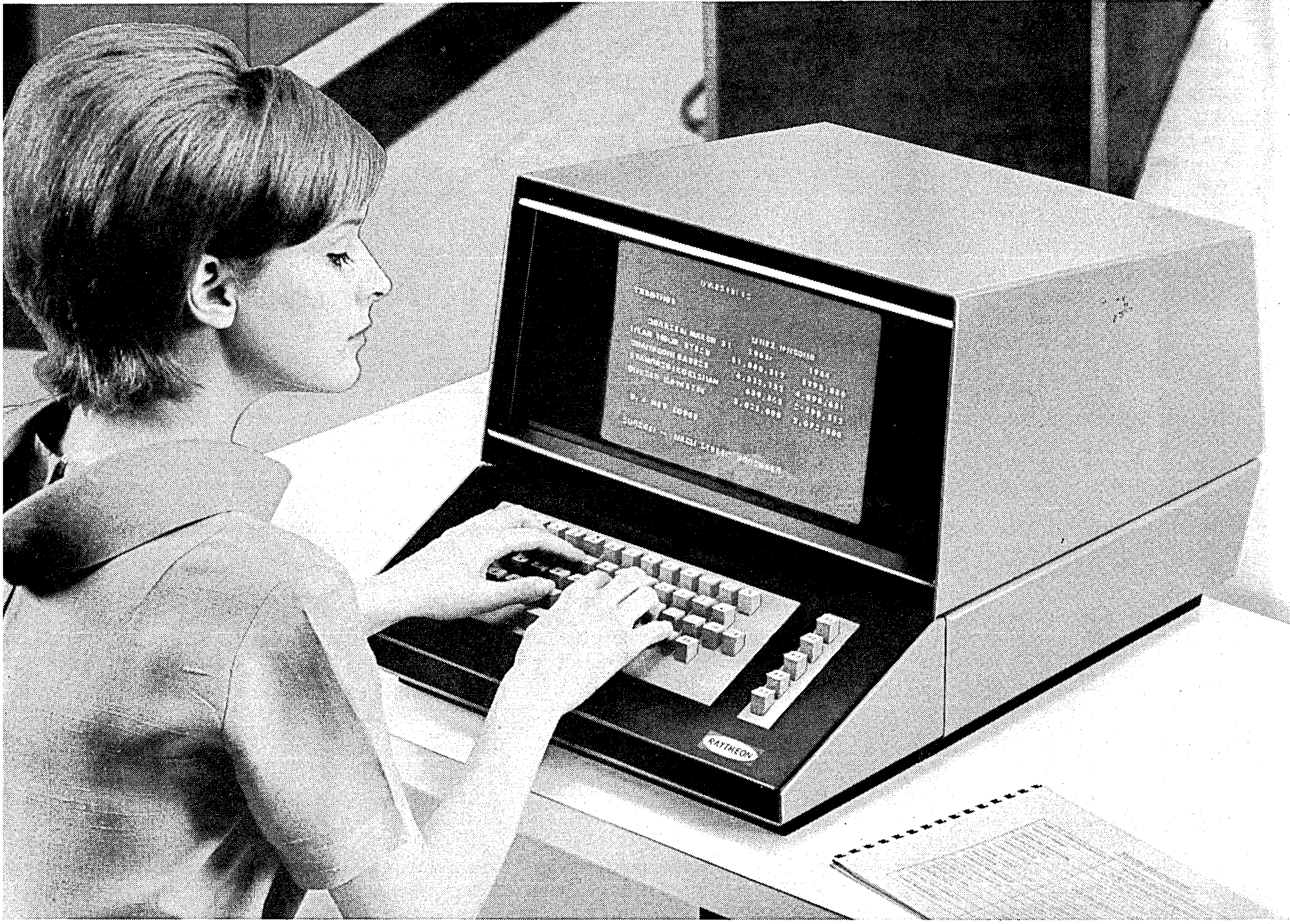
But the old Boston isn't lost.

As you set out to walk the Freedom Trail, walk a "Boston Trail" also. Leave the hotel, find Massachusetts Avenue, and walk down to Commonwealth Avenue. If you would like to sample one of Boston's better attempts to include French cuisine in its international menu—or if you would like a glass of wine and a piece of bread—stop by Les Tuileries, below the Eliot Hotel. Or—if you go a few steps farther and have a friend from Cambridge—you can enjoy the Harvard Club.

But walk down Commonwealth Avenue. Called by some architects the best residential street in a metropolitan



area, this mall holds many facets of



Raytheon introduces a new, low-cost digital information display system

A completely new, low-cost digital information display system for instantly retrieving and displaying data stored in a central computer is now available from Raytheon. This is the latest of thousands of cathode ray tube displays that have been designed and produced by Raytheon during the past 20 years.

The new system, the DIDS-400, interfaces easily with any type of computer and with various types of remote communication lines. It significantly reduces time required by operators to retrieve and edit data.

Up to 1000 alphanumeric characters can be displayed instantaneously. Operators can add to, correct or erase displayed data before returning it to storage without need of card punching and other intermediary processing. Hard copies of the displayed information can also be obtained.

Each DIDS-400 display console contains its own bright display, character generator, refresh memory and power supply. By combining these items in a single, self-contained unit, console dependence on the control unit or computer is greatly reduced, cabling problems are simplified, reliability is increased and the system given greater overall flexibility.

Highly-legible characters and symbols giving a closed-curve appearance are easily readable in normally lighted rooms, offices, and production areas, thus reducing operator fatigue and providing more efficient, error-free operation.

A brochure describing in detail the Raytheon DIDS-400 Digital Information Display System is available. Write: *Manager of Industrial Sales, Dept. D466, Raytheon Company, Wayland, Mass. 01778.*

CIRCLE 59 ON READER CARD

RAYTHEON

boston promenade

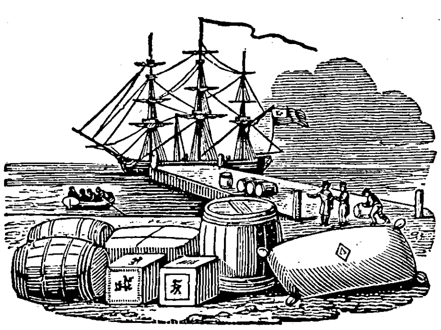
the past. Statues celebrate famous U. S. or New England citizens; the buildings also once housed many of Boston's elite. Now, most of them serve as fashionable apartments or in-town homes for people who can't resist the charm of this section, called Back Bay.

This area was planned. It was created when early Bostonians shaved off the top of Beacon Hill and filled in a portion of the Charles River basin. (And new construction here is a real problem). Cross streets, those which run north-south, are named alphabetically between Hereford (one block from Mass. Ave.) and Arlington.

Between Fairfield and Exeter, on the left, is the Algonquin Club. It is a very good place, so get a Boston friend to take you for drinks and dinner. You'll notice the old-British mode of the help, and the gas lights out front.

As you stroll under trees that, luckily, will be budding, continue to Arlington St. You will soon cross into Boston's beautiful Public Garden, but first you might want to turn right for a half a block to have a drink at the Ritz Carlton Hotel: It's one of the best in the world, and there is something about "The Bar," as the downstairs rendezvous is called.

The Public Garden, across the street, must really be see to be believed. And the swan boats are a must. "Visitors from 'round the world," a Boston tourist guide points out, "consider their trips to Boston incomplete until they ride these famous boats." It is circling the small duck pond, on these boats, where Naval historian Samuel Eliot Morison does



much of his writing. It is here, also, that many of Boston's thousands of students do much of their courting under the guise of study.

East of the Public Garden, just across Charles St., is the Boston Common. This first piece of public property in this country was originally designed as grazing land for cattle belonging to residents of Beacon Hill, and only a few years ago were cows finally banned.

The Hill, which shouldn't be missed, starts just down Charles to the left (north). Capped by the Bullfinch-designed State House, this federally-preserved area is a favorite living place for students, young working people, and the Boston Brahmins. Be sure to see privately-owned, cobblestoned Louisburg Square—probably the "best" residential location in the world.

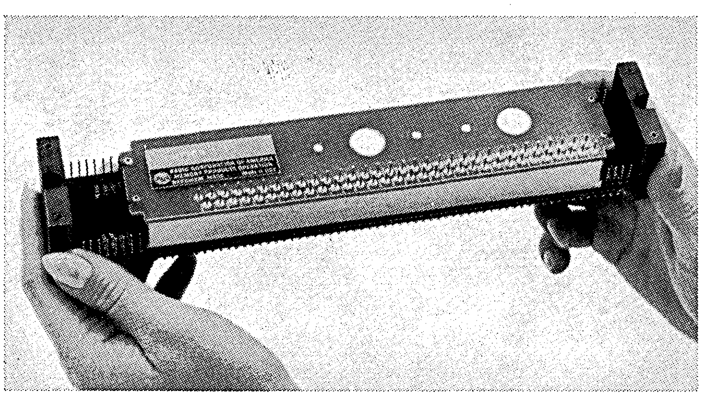
Wander up and around the Hill, or stroll across the hallowed ground of Boston Common, ground that covers a large parking garage. And end up on Tremont St. Along here the Freedom Trail starts; take it.

Before you do, however, you might want to find out why Locke-Ober enjoys its world-wide reputation. It's just around the corner from the start of the Freedom Trail, nestled away in an alley called Winter Place. The heavily paneled downstairs is for men only, but the ladies are welcome on the second floor. If you have a medium-sized party, call ahead and reserve a private dining room on the third floor. It's most practical.

Actually, the same food is available

ASSIGNMENT: BUILD A 16,384-BIT MEMORY STACK FIT FOR OUTER SPACE, TO WITHSTAND:-
50 G SHOCK
10 G VIBRATION
ΔT of -55° to +105°C

Result: This RCA ferrite memory stack, designed to withstand the rigors of space flight, meets the toughest kind of environmental specs:



Vibration—10 g (0 to peak) 5 to 2000 to 5 cps at 1 minute/octave logarithmic sweeps, once along each of 3 mutually perpendicular axes.

Mechanical Shock—50 g, 11 ± 1 msec, half-sine wave, 2 shocks in both directions in each of 3 mutually perpendicular axes, a total of 12 shocks.

ΔT— 5 cycles per MIL-STD-202, Method 102A, within limits of —55° C to +105° C. Unit to operate at specs at 0° C, 25° C and 70° C (without use of heaters or other means of internal temperature control).

How did RCA meet these demanding requirements?

- **By double-testing** each RCA wide-temperature-range ferrite memory core for 100% quality assurance.
- **Precision stringing** an array of 16 planes, each 32 x 32 cores, with continuous wiring through all 16,384 cores; no splices or internal solder joints are permitted. Then 100% testing the entire array.
- **Folding** the 16 planes over to form a continuously wired memory stack—and 100% testing it again.
- **Encapsulating** the stack in silicone rubber and securing it to its support case—and 100% testing it again.
- **Shaking, shocking and temperature cycling** the stack and 100% testing it at three different temperature levels.

Here's one more example of what RCA can do to build memory-system components to meet *your* requirements, regardless of how difficult they may be. Whatever you need in ferrite memory components, call your local RCA Field Office or write, wire or phone: RCA Electronic Components & Devices, Memory Products Operation, Section FD4, 64 "A" Street, Needham Heights 94, Mass. Phone: (617) HI 4-7200.

RCA® **The Most Trusted Name In Electronics**

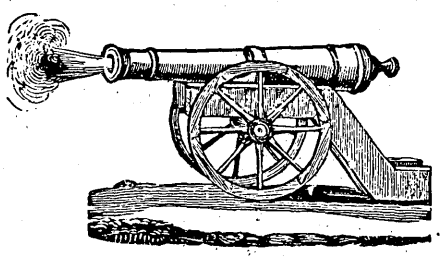
CIRCLE 62 ON READER CARD

boston promenade

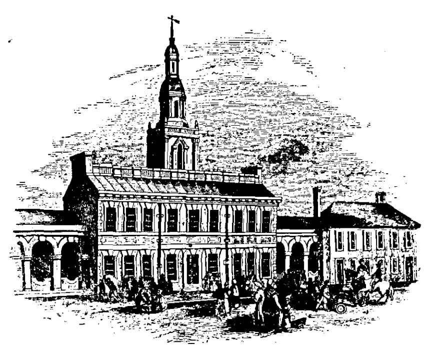
in different decor at Joseph's, on Dartmouth St. just south of Commonwealth. At either place (under the same management) luncheons are quite reasonable; dinners are primarily a la carte and push bills to the upper bound of Boston's pricing structure—a little more expensive, but well worth it.

Now, as you walk the Freedom Trail, you will come close to several good eating spots:

When you are in the Faneuil Hall area—and have enjoyed watching the open-air marketing transactions—try



Durgin-Park. The food there—roast beef in particular—comes in hearty portions. You'll be seated indiscriminately at long tables covered with checkered tablecloths, and may have to wait in a line out front. To avoid this, go in the downstairs bar, have a drink, and get the special ticket that lets you walk up the inside staircase to the dining area. As you walk past standing sides of beef, don't forget to think of lobster, also. Some of Maine's dwindling supply of big ones are waiting in the kitchen.



Many spots around Boston, however, know how to handle the Aristocrat of the Sea, so don't neglect the nearby Union Oyster House—across from where the striking modern Government Center is rising from the Scollay Square haunts so well-known to servicemen during World War II. And if you like steamed clams, this refuge-in-exile for France's Louis XV is the place to go.

As you complete the Freedom Walk, and see from where Paul Revere saw the light, you will be in the North End, an area called home by many of the Italians who live in Boston. It has several good spots for dinner, if you are in an Italian mood. Many Boston buffs will swear that Felicia's has the best northern Italian food in the country.

If you decide to tour Cambridge—the time-sharing capital of the world—just follow Mass. Ave. north from the hotel. Project MAC is only a few blocks across the Charles River (which separates Boston from several universities). Downstairs, in the Technology Square building that houses the center for study of machine aided cognition is a cocktail lounge/restaurant which features "Clocktail Hour." Arrive between 4 and 6 p.m., punch your time card in an antique time clock, and pay the first two digits for each drink. See you at 4:09.

Farther out Mass. Ave., at Harvard, there are a few things going on, also. The Fogg Museum's glass flower collection is world famous, and, like the Fine Arts and Gardner Museums (not far from SJCC headquarters), contains many outstanding paintings.

A beer at the Yard of Ale near Harvard Square goes very well, and there's also a time-sharing console in a nearby Radcliffe dormitory—if you can get in to use it. ■

Have you ordered an IBM/360?

Have you also ordered, or considered, a digital plotter to produce computer data in graphic form?

A picture is still worth ten thousand words – or stacks of printed listings.

Let CalComp show you how volumes of computer output can be reduced to meaningful charts and graphs – automatically, accurately, and completely annotated.

CalComp Plotters are compatible with the IBM/360 and other advanced digital computers . . . and with the computer you now use.

Call "Marketing" for details.

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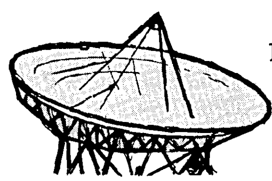
STANDARD OF THE PLOTTING INDUSTRY

CALIFORNIA COMPUTER PRODUCTS, INC.

305 MULLER AVENUE ANAHEIM, CALIFORNIA

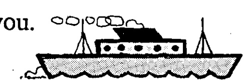
CIRCLE 65 ON READER CARD

If you have data to communicate, why not talk to the world's most experienced data communicator?



Data to communicate?

We have an expression about our data communication modems that will interest you.



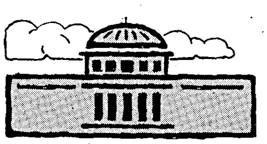
It's "optimum combination of factors."

Best technique (Kineplex). Reasonable cost. Minimum dimensions. Minimum power requirements. Ease of operation.

It's experience that makes such a combination possible.

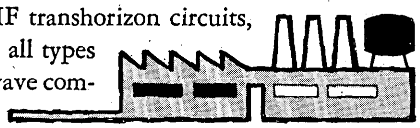
Collins began its continuing research program in data transmission systems shortly after World War II, when the need for more efficient high speed systems of this type became evident.

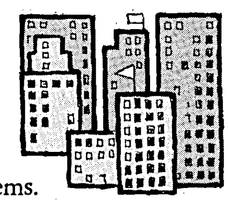
That program has produced many of the landmarks along the industrys' state-of-the-art path.



One of the program's major achievements was the development of Kineplex, a Collins modem technology which is now universally accepted as that which provides minimum error rate with maximum transmission rate per unit of bandwidth.

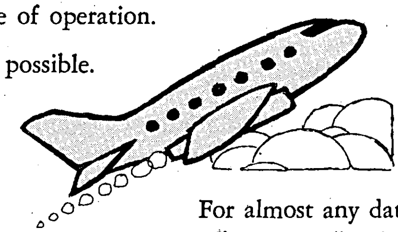
Our field experience with Kineplex has been extensive. Collins modems are used in Atlantic and Pacific transoceanic long range HF circuits, VHF transhorizon circuits, VLF radio circuits, and all types of wireline and microwave communication networks.





Collins modems are serving in tactical and strategic operations for the military, in defense and business applications for the government, in tracking operations in the nation's space effort, and in large and small industrial communication systems.

They also are used in secure voice and teletype systems to transmit encrypted digitized signals.



Collins modems are available in airborne, rack, and cabinet configurations, and in a wide range of data rates — from very slow to extremely high speeds.

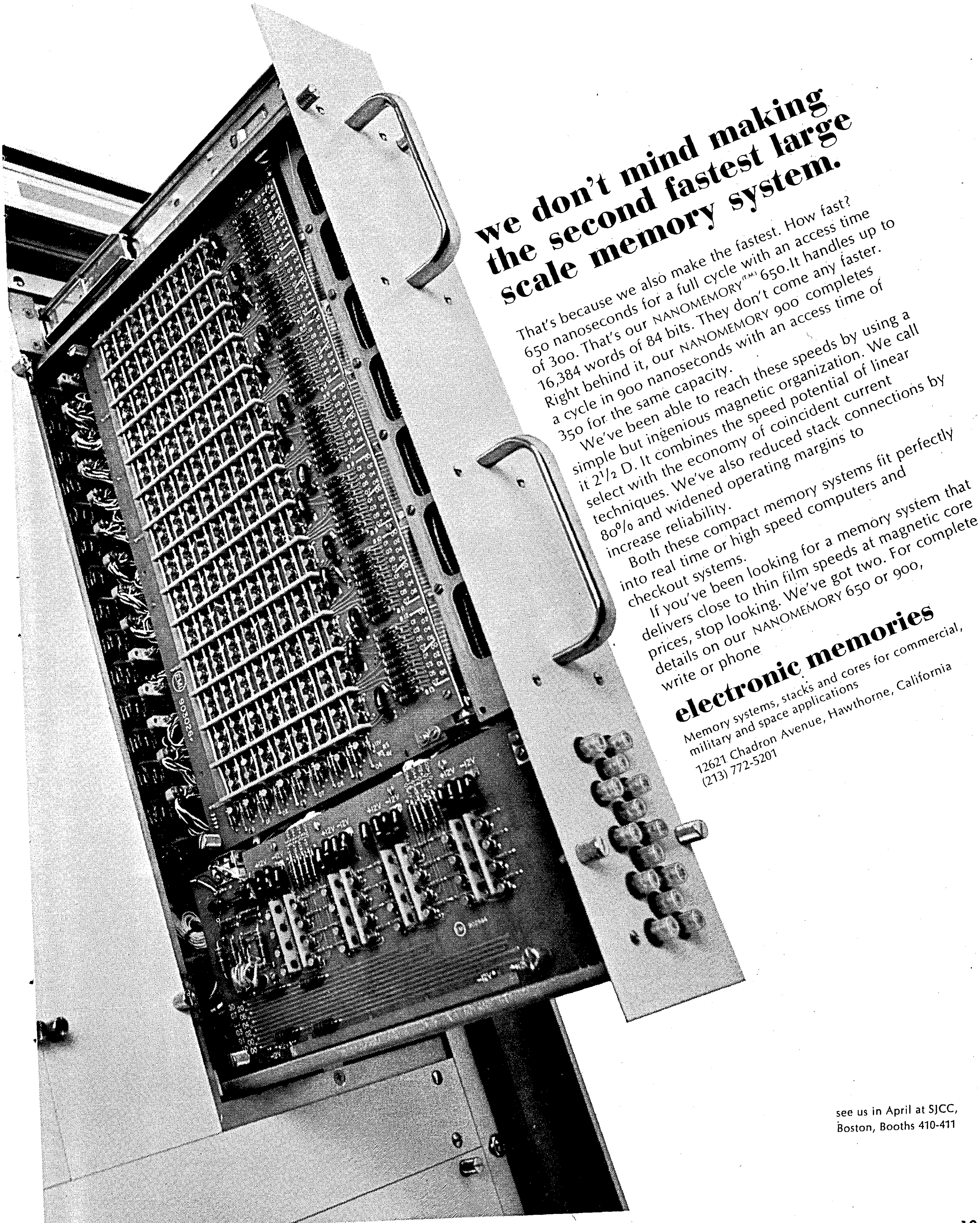
For almost any data transmission problem, Collins is able to offer you an "optimum combination of factors."

For information on specific equipment or applications, call or write to: Data Marketing Department, Collins Radio Company, 19700 Jamboree Road, Newport Beach, California. Phone: (714) 833-0600.

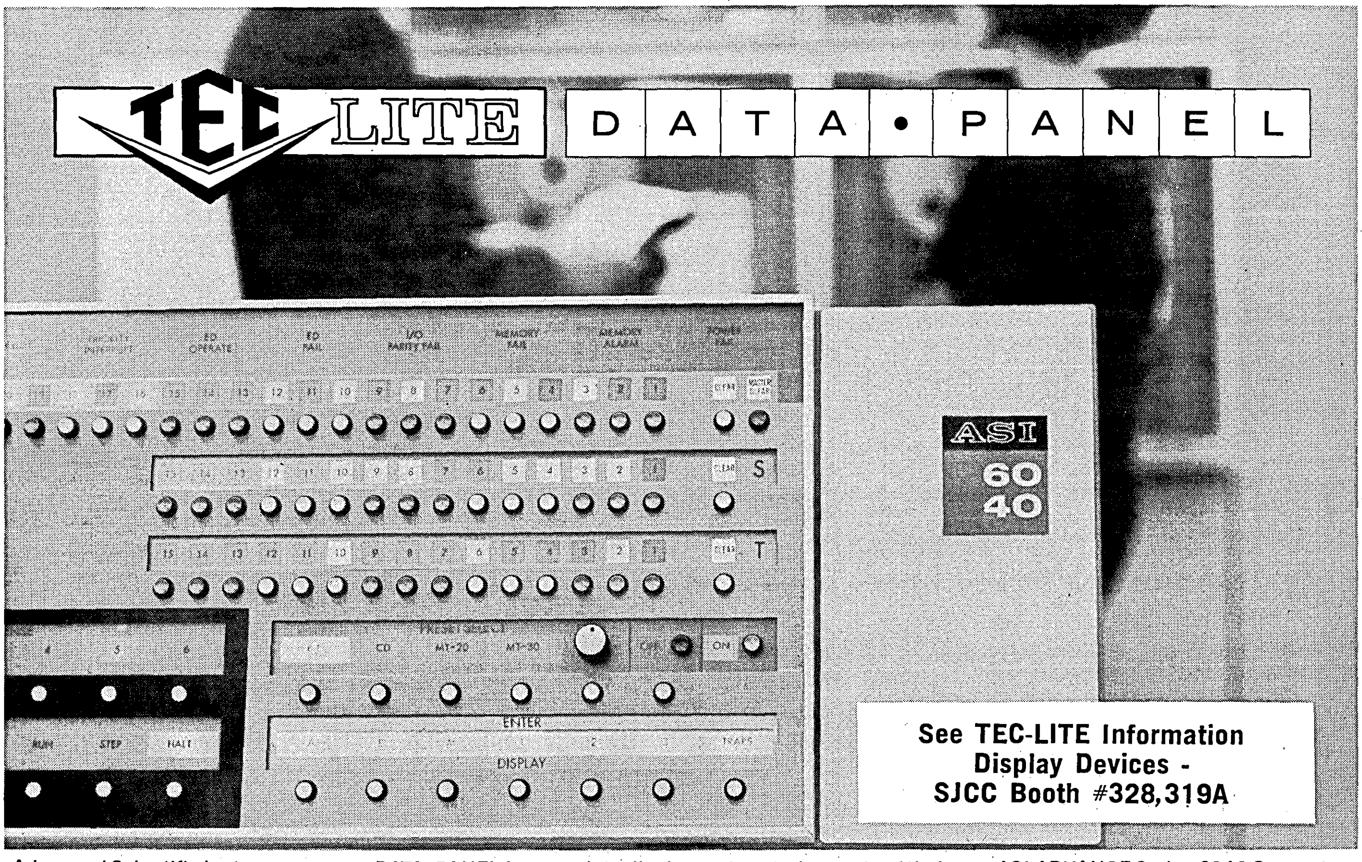
COLLINS RADIO COMPANY • COMMUNICATION / COMPUTATION / CONTROL

COLLINS

WORLD HEADQUARTERS / DALLAS, TEXAS

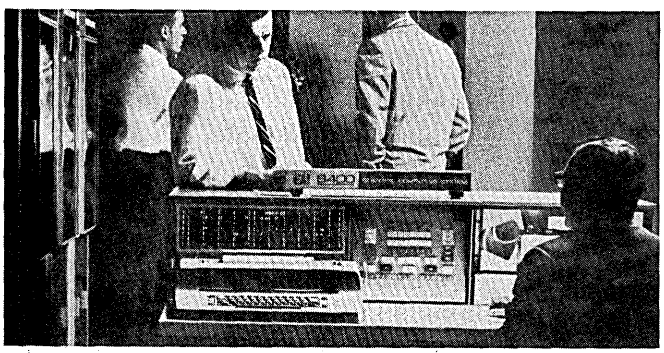


CIRCLE 67 ON READER CARD

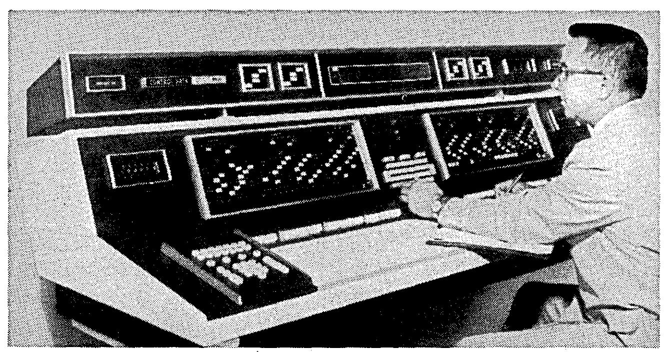


Advanced Scientific Instruments uses DATA•PANEL for complete display and control console of their new ASI ADVANCE Series 6040 Computer.

NEW CONCEPT OF INFORMATION DISPLAY AS DRAMATIC AS TODAY'S COMPUTER DESIGN!



DATA•PANEL indications are visible only when illuminated in EAI 8400 Scientific Computing System by Electronic Associates, Inc. ▲



▲ Two computers are operated from this Control Data Corporation Console which uses six DATA•PANEL Information Displays.

Leading designers of modern computers specify TEC-LITE DATA•PANEL for its dramatic new appearance in operator consoles and maintenance panels. DATA•PANEL offers a new concept of display versatility and visual impact, in addition to greatly increasing operator accuracy.

Extremely flexible visual and mechanical parameters of DATA•PANEL give designers display freedom never before available. There are no restrictions, within practical limits, to the shape, color, size or arrangements of the information displayed. Indications and digital readouts stand out emphatically in color behind smooth planes of glare-free black glass. When "off", legends and indications can be totally invisible until illuminated. For control, complete range of switch actions can be an integral part of DATA•PANEL design.

Write for full-color brochure, specifications and ordering information.

TEC LITE
INDICATING DEVICES

INDICATORS	DATA•PANEL	READOUTS	TEC-SWITCH

Transistor Electronics Corporation

Box 6191 · Minneapolis, Minnesota 55424 Phone (612) 941-1100

CIRCLE 70 ON READER CARD

news briefs

SHARE MEETING HEARS WATSON REPORT ON 360

IBM's top salesman, board chairman T. J. Watson, Jr., faced some 1200 members of SHARE (IBM large scale system users) last month to discuss, among other things, the delays in delivery of 360 software and hardware. Citing the 360 program as one of the largest corporate tasks in history, Watson said the 360 problems "are our own, attributable only to IBM." He noted that logic chip and SLT (IBM's name for their hybrid circuit) problems were being solved: production is up nine times, three plants are now operating at capacity, and chip yields are 70%. Shipments so far total 1360 systems, he said, and the rate will climb to 400/month by May. The 360 will go monolithic integrated circuit, he said.

Commenting on the recent report of the President's Commission on Technology, Automation and Economic Progress (of which he was a member), Watson noted that the press had inaccurately reported the findings of the Commission, highlighting a plan to pay people for not working. This concept of the negative income tax, he said, was not revolutionary (it was part of Goldwater's platform), and the recommendation of the Commission was that Congress look at the substantial poverty payments now being made to see if the money is going where it can do the most good.

The report, he feels, made one of the strongest statements in favor of automation and technological change, pointing out that automation is *not* a massive threat to employment, does not require inhibitive government controls.

Elsewhere at SHARE, members gathered to hear representatives of IBM, CDC, RCA and GE discuss their plans for PL/I. All are interested in it; the three "other guys" will implement it "as soon as appropriate." But the language was variously described as "unwieldy," overly expensive (the user will really foot the bill), and not independent of at least one machine (the keypunch). From the floor, one user said damn the other manufacturers; we need PL/I right now. Let IBM push ahead with it: "If that means a two-, three-year delay for the other manufacturers, that's tough."

At another session IBM reported on OS/360 performance. A multitude of charts and graphs seem to indicate one thing: software is tardy and slower than it should be. But emulation of the 7000 series on the 360 is almost equal to present 7000 speeds. Expectations are that those speeds will be appreciably better by the end of the year. The cry at the conference: Why wait, emulate.

AMA CONFERENCE LOOKS AT COMMUNICATIONS PROBLEMS

By 1972, communications and input/output will account for 60% of data processing costs to the user, Robert Francisco of Western Union told attendees at a recent American Management Assn. conference.

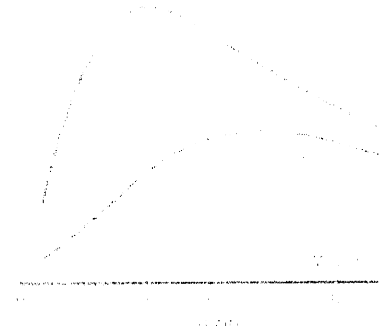
Almost 300 high-level administrative and dp managers crowded into the data communications session to

USC GETS FIRST OF NEW HONEYWELL BRAILLE PRINTERS

The Computer Sciences Laboratory at the Univ. of Southern California has been given a computer-driven Braille printer by Honeywell that can produce 300 Braille "cells" (up to six dots) a second, about 100 times as fast as the most commonly used methods.

USC's unit is the first produced by the company and it is being used in connection with projects for training the blind, together with a special Teletype machine for preparing input, developed by Ray Morrison of the Illinois Bell Co.

In addition to simplifying the training of blind programmers and providing them with a system that can be used efficiently, the Braille unit will be applied to on-order production of educational materials for other blind students. A library is being built up and stored on magnetic tape.



hear what AT&T, WU, and a user had to say about the problems they were facing in adding communications capabilities to their systems.

All panelists noted the great need for systems planning and the innumerable hardware, software, communications facilities, and human considerations. The dilemma is not only the "how," but which piece of equipment and what speed do you need? Francisco noted that there are more than three dozen CRT devices alone on the market now, and if the user is to make the right selection in I/O equipment, he had better start developing a comprehensive file on what is available. W. B. Quirk of AT&T added to a long list of modems available by announcing that Bell Labs is developing a new unit which will provide speeds of 3600-9600 bps over voice channels.

Further improvement in nationwide communications services provided by the common carrier will be up to the user, noted Quirk. For example, he said, there is some demand for a common user wide band service (only private service is now available) but the market is not great enough yet to justify the expense. Francisco noted that WU's microwave system, which will supply all speeds up to 48K bps by the end of the year, now only goes between some of the major U.S. cities. Again, the market is not great enough to extend the service into smaller communities.

Technologically and economically, the equipment exists or will, said D. J. Dantine of Clark Equipment Co., but there are serious problems blocking data communications progress. One is the "inability of Western Union to compete with AT&T on a cost and capability basis." The government, he said, should not attempt to strengthen WU by weakening AT&T, but perhaps should financially aid WU to become competitive. TELPAK should be left alone by the FCC, he thought, disagreeing with the idea that all services should be compensatory (it has been claimed that TELPAK is being supported by Bell voice operations). In the area of private microwave, Dantine felt such systems are "difficult to justify for most corporations, especially because of interconnection restrictions." For example, the private system can't interconnect with the Bell System.

And if all these considerations weren't enough, a major point of other AMA sessions was the increasing, serious shortage of systems analysts and, to a lesser degree, of programming talent to develop data communications/processing systems.

ILLIAC IV PLANNED BY UNIVERSITY OF ILLINOIS

Execution of a contract for over $8 million to build and operate Illiac IV has been authorized by the board of trustees and the University of Illinois. Some $6 million is budgeted for construction of the computer, which may be "up to 50 times faster than any other now contemplated." The contract is from the Department of Defense through the Air Force Rome Air Development Center.

Prof. Daniel L. Slotnick will be in charge of the project, which will be based on his machine organization concept using one control unit and several hundred arithmetic and storage units. Development and construction is expected to take two and a half years.

HUNTER AND HUNTED LINKED BY ON-LINE SYSTEM

For job recruiting, the nation's firms will soon have the chance for on-line access to a computer data bank on college graduates. The College Placement Council of Bethlehem, Pa., a non-profit organization representing about 1,000 colleges and universities and 2,000 U.S. and Canadian employers, has begun to gather resumes from graduates with job experience for its GRAD service (Graduate Resumes Accumulation and Distribution). A thesaurus of job skills has been developed to standardize data input and queries.

GRAD will be in operation by this summer, but it won't include graduating seniors until the class of 1967 or '68. Size potential of the system is indicated by CPC figures on graduates: four million in the last decade and seven million in the next.

GE, which developed the computer file system, is making available for GRAD four GE 235 computers, two Datanet 30's and three 6-megacharacter disc files, located at its Missile and Space Technology Center in Valley Forge. Charges for on-line service are a $10 teletype-connection fee, 50 cents a minute for computer time (each inquiry averages three minutes) and $2 for a copy of each resume, which will be stored on microfilm. Mail inquiries are the same except for connection fee. Graduates pay $10 to have their resumes on file.

The project faces some legal problems as the placement and consulting firm of Information Science, Inc., which also bid on the contract, has filed suit against GE for "unfair competition" in bidding on system develop-

news briefs

ment. ISI claims that GE cut its development bid to "minus zero" in order to "monopolize the new line of commerce" in personnel data systems, and is asking for an injunction against GE and $3 million in damages, penalties, and costs. GE has refuted the charges and says it expects to make a profit on the contract.

ITT DIVISION OPENS WALL STREET SERVICE CENTER

ITT Data Services has opened a Wall Street dp center, the second of a network of satellite computer centers planned for the New York-New Jersey area. An IBM 1460 is processing data and transmitting larger problems, via a 7711 transmission unit, to a 7094 in main ITT center in Paramus, N. J. A variety of computer services is offered, including investment appraisal, short-range economic forecasting, and structural design.

This spring the Paramus center will begin converting to third-generation equipment with the installation of Models 40 and 50 systems. In 1967, a 360/67 time-sharing system will be installed to process not only data from satellite centers but also from on-line terminals located at customers' offices. Other small ITT centers are slated this summer for Princeton, N. J., and mid-town Manhattan.

WU LAUNCHES INFORMATION UTILITY

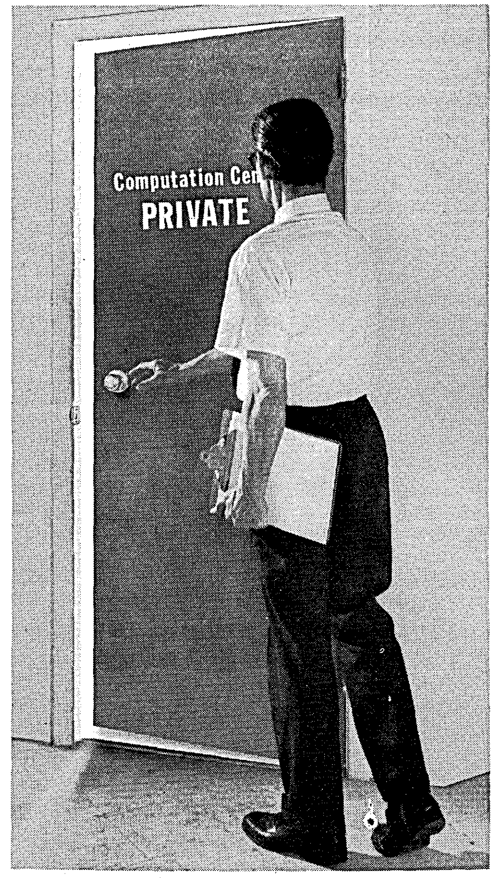
Western Union has formally opened its first computer service center in New York and announced that four others by early 1967 in San Francisco, Chicago, Dallas, and Atlanta. These centers comprise Phase I of a WU information utility program, Info-MAC, which will provide a series of new communications, data processing, and reference file services to WU customers all over the continent. Under Phase II, third-generation systems will go into centers in key cities, including New York, Chicago, and San Francisco, and into smaller, satellite centers in at least 25 additional locales.

Phase I centers, equipped with Univac 418 computers, initially are to provide automatic routing of single and multiple-address messages between Telex customers anywhere in North America, and from Telex to TWX stations in the U.S. AT&T, owner of TWX, has approved the latter arrangement. About 3,000 subscribers are now using the New York center, and by the end of 1966, about 14,000 Telex users in 200 cities are expected to be on-line to the network. Another service being developed is on-line access to information files on various fields, such as the legal reference service soon to go into operation (see Datamation, Feb., p. 79). WU is using and adding Fastrand drums to provide storage for these data banks.

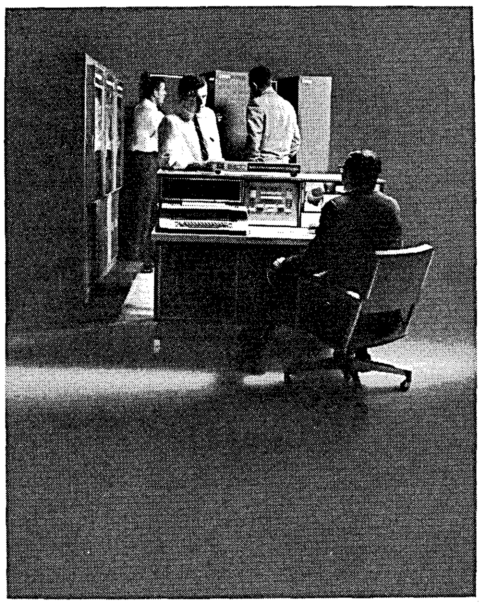
A major feature that will mark the program when it has been fully developed, possibly by 1968 or '69, will be the switching service permitting a customer, using one terminal, to send messages to Telex, TWX, and broadband stations here and to similar stations abroad.

● System Development Corp. has completed a study for the Federal Council for Science and Technology, resulting in recommendation of a national document-handling system for scientific and technical information. The SDC group was headed by Dr. Launor F. Carter and worked with a team from the Committee on Scientific and Technical Information under the direction of William T. Knox. The report recommended organization of a new agency to give policy guidance to various federal departments and

Is the engineer fated to be frozen out of the computer loop?



Not if EAI can help it.



That is why we designed the EAI 8400 Digital Computer.

Often overlooked in digital computation is the battery of people and procedures which stand between the design engineer and the execution of his program. He's working one step away from the machine—and his problem.

This is tough on anybody who is used to the "hands-on" approach to computer usage.

The EAI 8400 fills this gap in man/machine communication.

It's a sophisticated digital computer that brings the engineer and his thinking back into the design loop. Designed to satisfy the stringent requirements of computer simulation, the 8400 lets the creative engineer use the familiar model-building, trial-and-error design process...in real time and faster than real time...in an on-line environment.

We've given the 8400 the power to perform extremely high speed, floating point arithmetic. How important is this? Well, 40% to 60% of all instructions in simulation and real time programs deal with floating point operations.

The EAI 8400 offers a new high level of capability in software. Throughout all phases—program preparation, debug and execution. It has a FORTRAN IV compiler and four other powerful languages. You can talk these languages while being interrupted for real time processing—without even knowing it.

You'll also be hearing a lot about EAI's Dynamic Storage Reallocation—a fundamental innovation that allows programs to be reassigned within memory, at will.

We didn't design the 8400 as the computer to do everything. It was designed specifically to expand the creativity of the engineer and the scientist, and it answers the exacting needs of the simulation laboratory. Why not investigate the EAI 8400 for the solution of your engineering problems? Write for detailed information.

EAI®

ELECTRONIC ASSOCIATES, INC., *West Long Branch, New Jersey*

news briefs

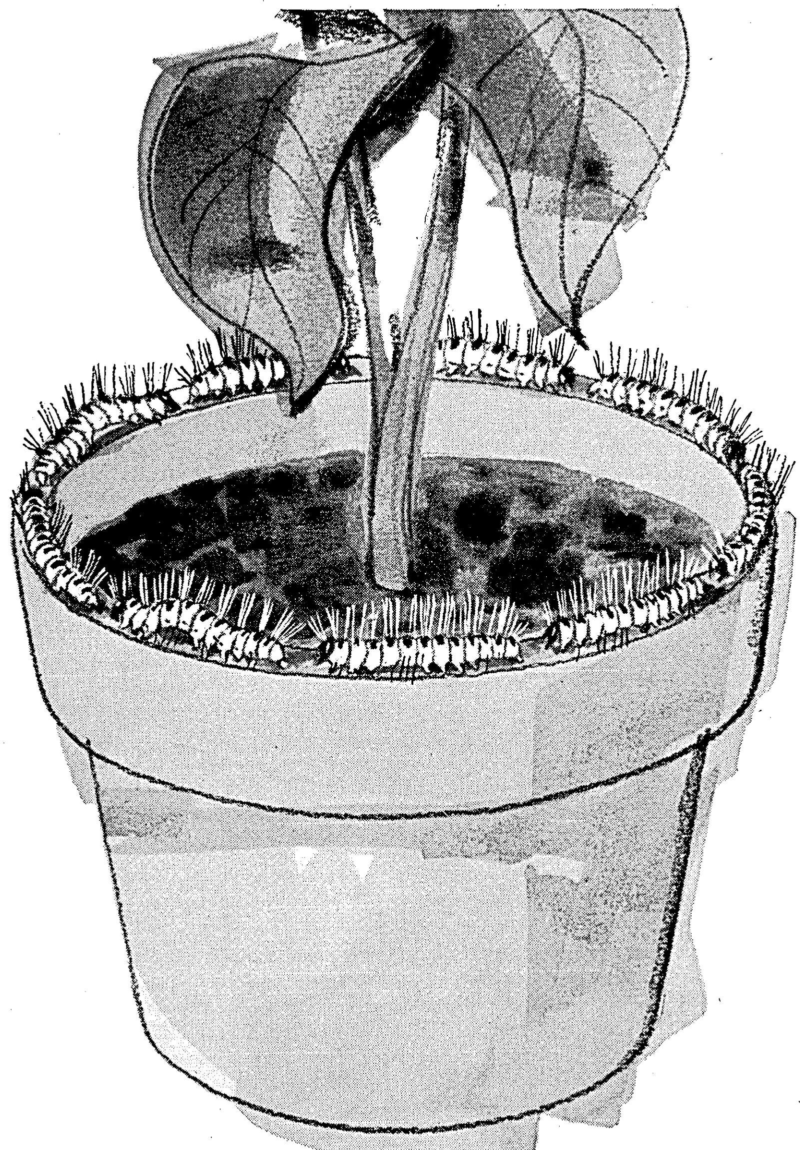
agencies. It also recommended development of a "responsible agent" program in existing organizations to handle document management.

● Pan American Airways is using crt displays to check-in passengers and monitor and plan cargo loading. Agents and load controllers at New York's Kennedy Airport and city terminals are using a total of 28 Bunker-Ramo 212 keyboard/displays which are on-line to an IBM 1440 system. Data on 30 active flights are stored at one time. In the future, Pan Am intends to develop such systems at other major points in the U. S. and abroad.

● The first Honeywell 2200 has been delivered, going to Courtalds Ltd. of Coventry, England. It has a 65K, 1 usec core memory, six tape units, and other peripherals; data transmission equipment is being added, linking the computer to Courtalds factories throughout England. In addition to general business data processing, applications included operations research, simulation, critical path, and a management reporting system specially developed in cooperation with Honeywell.

● Cornell University has ordered an IBM 360/67 time-sharing system, which will be in operation in fall of 1967. It is expected that up to 50 typewriter and display terminals will be linked to the system, which will be applied to teaching, research and administrative tasks. The 360/67 configuration includes two processors with 256K characters of core each, a 4-megacharacter 2301 drum, a 208-megacharacter 2314 disc file, a 400-megacharacter 2321 data cell, six tape units, three printers, and two card read/punch units.

● Minnesota has inaugurated a cooperative program under which many of the state's 180 hospitals will use an on-line central computer complex. Eight hospitals are now using two Honeywell 200 systems at the Minnesota Blue Cross Cooperative Data Center for payroll accounting. Other functions, such as inventory control, payroll and property accounting, preventive maintenance scheduling, patient care management, and laboratory test reporting will be added as the system develops. Cost of the service for a 300-bed hospital is $2,200 a month.

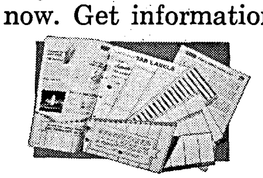


How's this for getting no place slow?

The Processionary Caterpillar *(Roundanda Rounda' Gogo*)* was never much in the initiative department. Seems all these fuzzies want to do is play 'follow the leader'. Set 'em around the rim of a flowerpot and they keep marching around in a circle until they drop off from sheer exhaustion. (This symptom in *homo sapiens* is called the "mistaking-activity-for-accomplishment" syndrome.)

There are more "m.a.f.a." sufferers around than you might imagine. Take our own line of work, for instance: Did you know there are still data processing people using Tab Labels in horizontal 16th-of-an-inch sizes?!! That's right! . . . and they could use Brady Tab Labels in tenth-of-an-inch sizes. Then they'd match the number of print-out-characters-per-inch of their Tab equipment. And why are they using these old style labels? Just because some other Tab Label manufacturers made labels that way from the start, and never thought much more about it.

If you're a "m.a.f.a." sufferer, shake the fuzz now. Get information, samples and prices on Brady Tab Labels by calling your Brady Tab distributor, or writing us today.



*Actually, the scientific name is cnethocampa processionaria.

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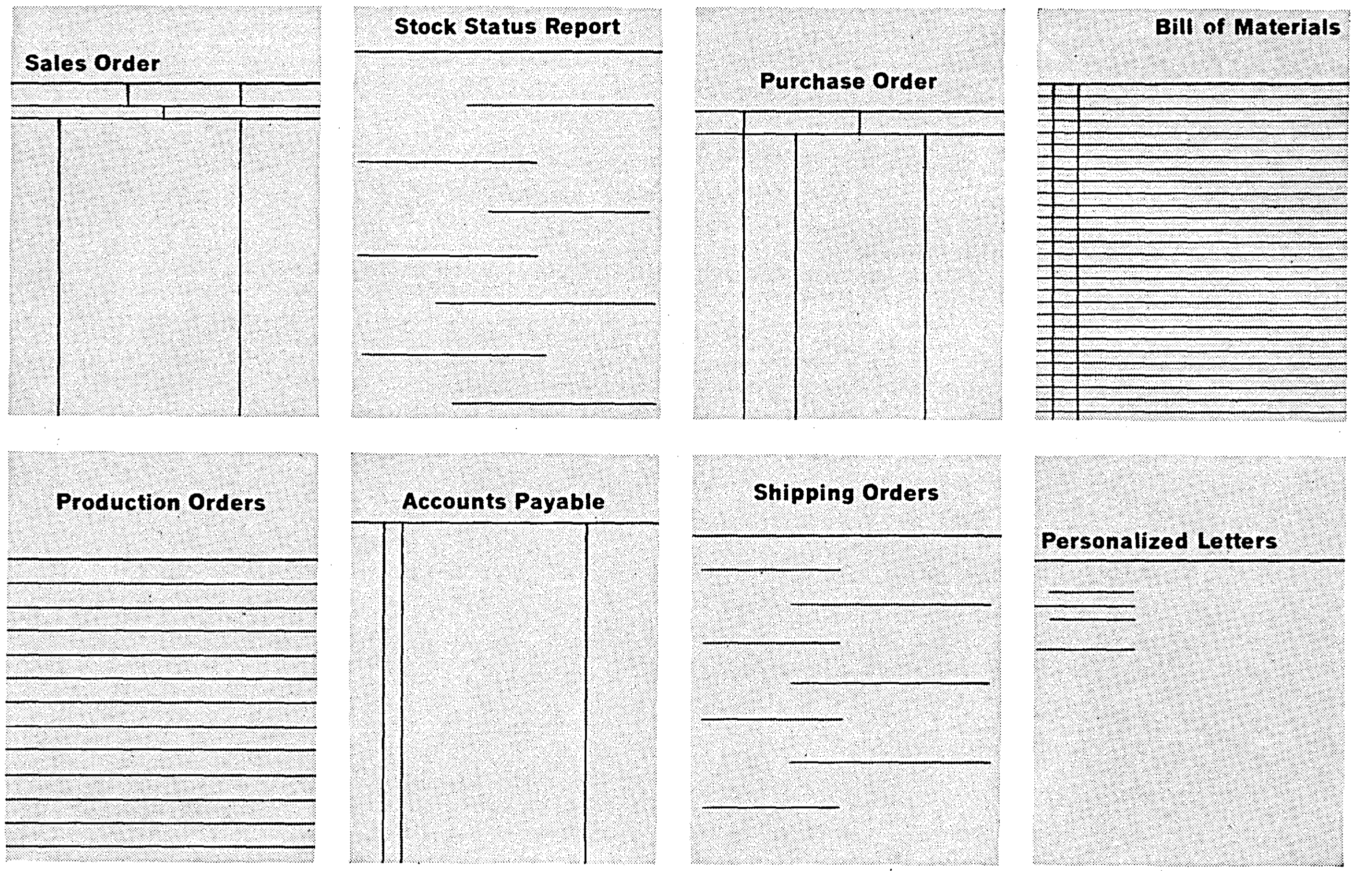
CIRCLE 77 ON READER CARD

Check the office forms you'd like prepared automatically...



Now read about this one machine that automates them all

The Dura® MACH 10®. It automates sales orders, invoices, inventory reports—virtually any business application. Data is read, punched, and typed automatically at up to 175 words per minute. Edge-punch cards or punched paper tape are used to capture repetitive data—accurate data to produce documents. By-product tapes provide information for management decisions before the data is old history. Check into the Dura MACH 10 today. Call your local Dura representative. Or write your name and address on this advertisement and mail to: Dept. D21-46, Dura Business Machines, 32200 Stephenson Highway, Madison Heights, Michigan 48071.

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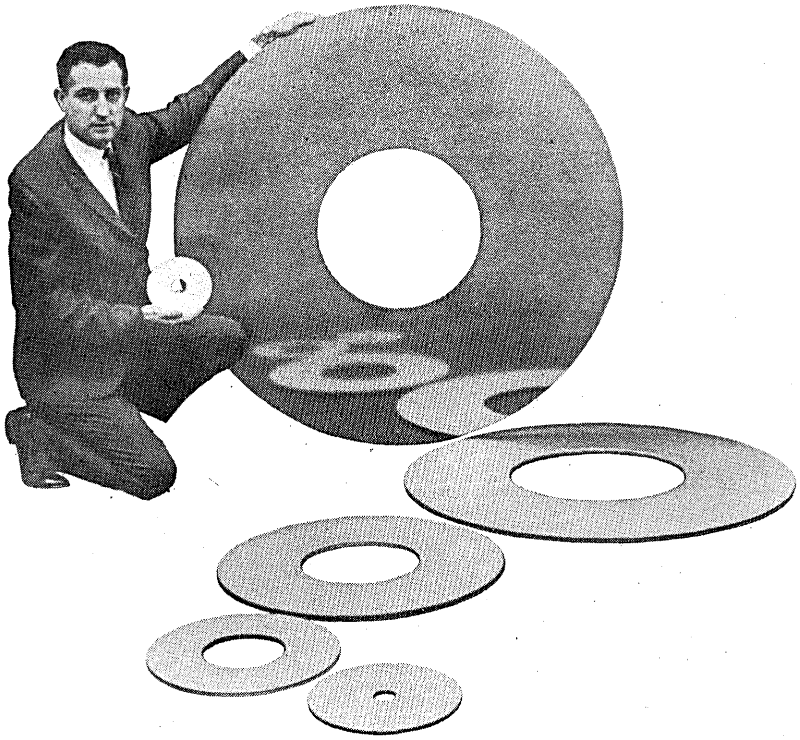
CIRCLE 78 ON READER CARD

No one has a larger line of disc memories.



See the largest line of disc memories available at the Spring Joint Computer Conference, Booth 913-916

Whether your information storage requirements are small or require data stored in millions of bits, Librascope Group of General Precision, Inc., has a disc memory system for every application. These systems have a proven history of reliable performance in computing systems designed for military, business, engineering, and educational applications.

LIBRAFILE mass memories: Large-capacity, high-speed, random-access information storage systems. Two disc sizes available. 48″ discs capable of storing up to 400 million bits. 38″ discs with a capacity of 200 million bits. LIBRAFILE mass memory information retrieval is either fixed-address search or search-by-record content. Access time less than 20 ms. Data transfer rates in the megacycles.

Militarized disc-memory systems: High-speed, random-access, information-storage systems. Consists of disc memory for data storage and an electronic subsystem that provides complete interface, control, and read/write electronics. These systems can be used as a data base for shelter, van, or shipboard applications. Storage capacity of 25 million bits on 24″ discs. Customized capacity up to 80 million bits.

L-400 magnetic-disc memory systems: Provide data storage and transfer in computer systems, peripheral equipment, and other systems where rapid-access memory is a requirement. 24″ disc storage capacity up to 36 million bits.

Airborne disc file: Small, compact file designed for airborne (MIL-E-5400 class 2) applications, as well as for shipboard and mobile field operations. 6¼″ disc with capacity of 1 million bits. Customized airborne memories available with capacity up to 50 million bits.

L-300 disc memory: For use in computer systems and peripheral equipment as main storage, buffer storage, or as a supplemental memory. 10″ disc with a capacity of 275,000 bits.

For complete details, write for our technical bulletins.

Engineers: For career openings, call or send resume in confidence to B. Larson, General Precision, Inc., Librascope Group, 808 Western Avenue, Glendale, California 91201. An equal opportunity employer.

A Plans-for-Progress Company.

GP GENERAL PRECISION INC.

LIBRASCOPE GROUP

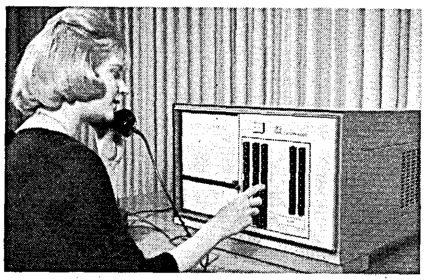
808 Western Avenue
Glendale, Calif. 91201

CIRCLE 79 ON READER CARD

new products

document retriever

The CARD (compact automatic retrieval-display) system is a self-contained desktop microfilm file reader with up to 67,500 pages accessible in an average of 2 seconds. Document images are stored in filmcards, 90 pages to a card; 25 filmcards comprise a magazine; and 30 magazines fit in a reader.



Pushbutton selection from a control panel locates the desired record, positions it in a projector, and displays it on a screen. There is a 24x magnification. Selection of a new record automatically returns the displayed record to the file. HOUSTON FEARLESS CORP., Los Angeles, Calif. For information:

CIRCLE 130 ON READER CARD

gp digital computer

The LSI 8800 is an i.c. computer intended for such applications as data conversion and formatting, message switching, and process control. It has a core memory capacity of 2-65K (8-bit) bytes, cycle time of 1.5 usec, a 600-nsec access time, and data transfer rate of 200K bytes/second. Several cpu's may share the same memory. The I/O facility is a six-channel multiplexer system, expandable to 254 channels, which is externally scanned for interrupt. Interfaces are available for a variety of peripherals and for IBM 360 computers. Software package includes an assembly language called LINGO, a subroutine library, and utility routines. DATA AND CONTROLS DIV., LEAR SIEGLER, INC., Long Island City, N.Y. For information:

CIRCLE 131 ON READER CARD

badge reader

The model 0107 is part of the Transacter line of data collection systems. It accepts 15- or 22-column plastic cards singly, as well as variable data up to 10 digits. With a self-contained scanning control, interface can be directly to a main data collection trunk line. Transmission rate is 120 cps. The model 2013 adapter generates control signals for badge readers via its scanner circuits, and adds fixed digital data, up to 30 characters, to messages. CONTROL DATA CORP., Minneapolis, Minn. For information:

CIRCLE 132 ON READER CARD

incremental cartridge recorder

The 2200 series has writing speeds from zero to 300 steps/second, incremental read to 150 steps/second, and synchronous reading from 250 to 500 steps. Cartridge capacity is 780K 8-bit characters; other models store the same number of 7-bit characters in IBM-compatible format. Read-only or write-only units are also available for 7-channel configurations or the 8-channel ASCII code. KENNEDY CO., Pasadena, Calif. For information:

CIRCLE 133 ON READER CARD

management software

A package called AIMS (automated industrial management system) consists of 10 applications programs for the 315 family of computers. Included are inventory control, forecasting, accounts receivable, etc. Although useable separately, they're intended as a total system, establishing a single master file that accepts inputs and effects exception reporting. NATIONAL CASH REGISTER CO., Dayton, Ohio. For information:

CIRCLE 134 ON READER CARD

multi-function chips

Containing as many as 40 conventional IC functions on a one-layer silicon chip is the Monolithic Digital Functional Arrays. Included are a "fast adder," 4-bit binary register, and a decade frequency divider. The regis-

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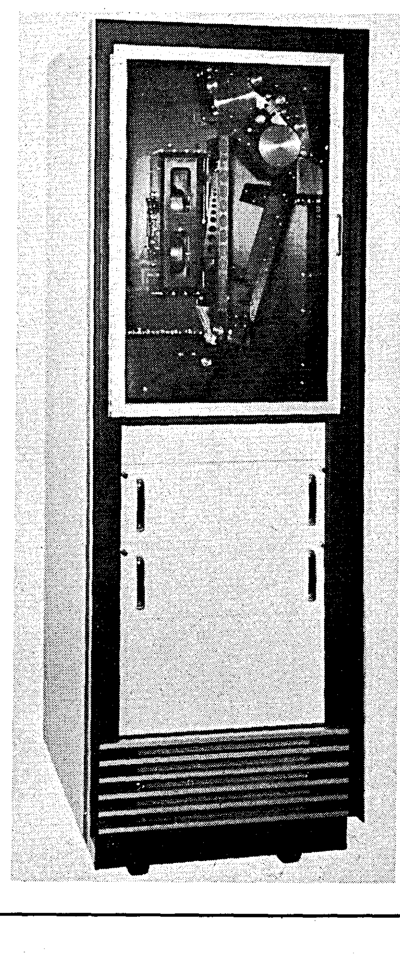
A random-access memory unit holding up to 100 million bits and with

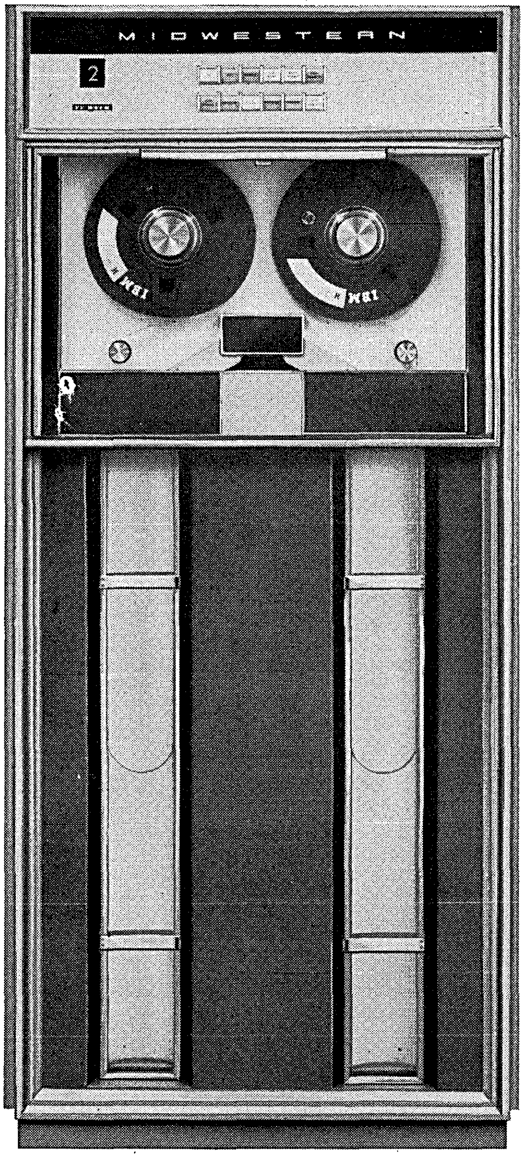


a maximum access times of 50 milliseconds is the model MCM-1. The unit uses flexible magnetic cards mounted in interchangeable cartridges. Each cartridge, which can be loaded or unloaded in less than five seconds, holds 64 cards. And each card has 128 tracks divided into four groups of 32.

One 32-track, dual-gap head provides read-after-write capability. When 32 tracks are processed in parallel, the data rate is 10.4 megabits/second; from one track, in the case of serial recording, it's 325,000 bits/second. Card size is 16 x 4.5 inch.

The machine uses a content address system, and the cards in the cartridge are randomly ordered. When a card is addressed, either by the computer or by the control panel buttons, the address is stored internally. When the extract command is issued, the appropriate card is selected, extracted, and passed over the read/write head. There are two capstans for card recirculation, and a capstan for re-entry, card selection, and extraction mechanisms. Delivery is in six months. COMPUTER ACCESSORIES CORP., Santa Barbara, Calif. For information:

CIRCLE 135 ON READER CARD



How does Midwestern guarantee data reliability?

M4000

DIGITAL TAPE TRANSPORT

COMBINING UNPARALLELED OPERATING DEPENDABILITY WITH THIRD GENERATION COMPUTER SYSTEM PERFORMANCE FOR ADVANCED DATA PROCESSING SYSTEMS

MIDWESTERN INSTRUMENTS
SUBSIDIARY OF THE TELEX CORPORATION

The M4000 pneumatic tape transport system is guaranteed to read tapes recorded to IBM compatability specifications with less than one transient error per 10^9 data bits; at densities to 800 bpi, and at transfer rates to 120 KC. Every production tape transport is factory tested for a minimum of 100 full reel passes; reading and error checking random record length, variable pattern data tapes under full program control. Actual statistical results of these tests, over a number of transports and many thousand full passes, have shown an average data reliability rate of one transient error in 27.1×10^9 characters read. This safety margin, developed from actual test data, makes Midwestern's guarantee of one error in 10^9 a realistic promise, not just another empty claim.

For more information on the M4000, write or call Ralph P. Bohn, Digital Tape Products Division, P. O. Box 1526, Tulsa, Oklahoma 74101. Our phone number is 918-627-1116.

CIRCLE 80 ON READER CARD

ter reportedly can store and transfer up to 250 million bits/second. SYLVANIA ELECTRIC PRODUCTS INC., New York, N.Y. For information:

CIRCLE 136 ON READER CARD

keypunch/verifier

The model 65 can be used as a punch and a verifier. In the punch mode, the holes are shorter than normal, and in the verifier mode they are elongated to standard length. Holes escaping elongation (errors) are subsequently detected by a mod 131 automatic verifier, which runs at 200 cpm. INTERNATIONAL COMPUTERS & TABULATORS LTD., Putney, England. For information:

CIRCLE 137 ON READER CARD

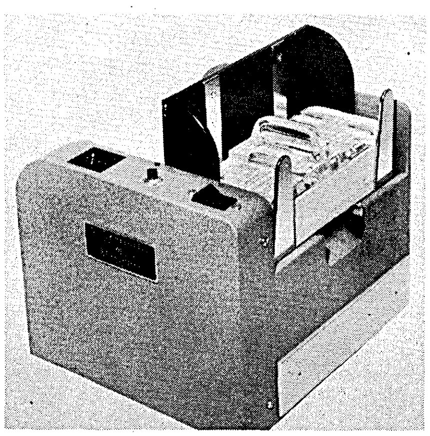
flowchart software

On mag tape is the FLO-TRAN program, which automatically produces flowcharts of FORTRAN IV source decks. Output is on the SC-4020 microfilm plotter in the form of 35mm film or hard copies. In addition to generating flowcharts from input commands, it supplies program listings, and operates in the typewriter fashion for general documentation purposes. The program interprets and classifies source statements, and processes these statements and associated data according to their classification. Binary output tape has SC-4020 commands with information from source cards. Software is by Gavid J. Clark of GE. MARSHALL SPACE FLIGHT CENTER, Huntsville, Ala. For information:

CIRCLE 138 ON READER CARD

card counter

The CC-350 has an input card hopper, card counter, and output stacker, and counts at the rate of five cards/second. There's also a manually-resetable 4-digit counter. Duplicate card sensing and counting circuitry are used for ac-



new products

curacy. SYSTEMATICS OF MISSOURI INC., Kansas City, Mo. For information:

CIRCLE 139 ON READER CARD

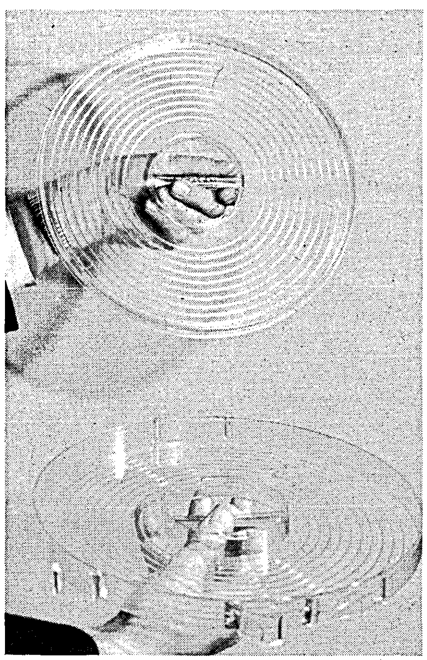
portable digital recorder

DR 1200 digital tape recorder reads and writes IBM computer compatible tape at 200, 556, and 800 bpi at speeds to 120 ips, seven or nine tracks. Weight of the portable unit is 45 pounds and operation takes only 100 watts. RALPH M. PARSONS ELECTRONICS CO., Pasadena, Calif. For information:

CIRCLE 140 ON READER CARD

tape canister

Measuring only 1 1/16-inch wide, styrene container for mag tapes is said to be half-inch thinner than other models. Eliminated are divider inserts to hold tapes in place. A molded hook, an integral part of the canister, per-



mits reels to be suspended on a bar in the cabinet; this and a molded hook form legs for the container when it's in a standing position. DIEBOLD INC., Canton, Ohio. For information:

CIRCLE 141 ON READER CARD

card reader for teletype

CRU automatic card input unit is used in data communications, processing, and collection. When used with standard model Teletype machines, it operates in the same way as the TTY tape reader, without sacrificing any teletypewriter functions. Options allow use with computer equipment, billing and accounting machines, or numerical process control systems. DIGITAL ELECTRONIC MACHINES, Kansas City, Mo. For information:

CIRCLE 142 ON READER CARD

automatic writing machines

The 2300 series of Flexowriters includes five new models, all with speeds up to 145 words/minute, with varying capabilities depending on ap-

plication needs. Featuring quiet operation, the series read and punch 8-channel tape. FRIDEN, INC., San Leandro, Calif. For information:

CIRCLE 143 ON READER CARD

paper tape reader

A photoelectric paper tape reader, the PTR-60 competes in cost with mechanical units and is suitable for data processing and machine tool control applications. Opaque tape is read at 150 characters/minute; and optional feature permits reading of translucent tape. The PTR-60 operates on a step-pulse supplied by the user. OMNIDATA DIV., BORG-WARNER CORP., Philadelphia, Pa. For information:

CIRCLE 144 ON READER CARD

paper-tape correction system

Editmaster Series 110 is an automatic tape-merging system for editing and correcting tapes to be used in photographic and metallic typesetting. The original and correction tapes are loaded on upper and lower stations, respectively, and the unit produces a third, corrected, six- or eight-level tape at 110 cps. The 110 searches for the point of error on the original at 500 cps. PHOTON, INC. Wilmington, Mass. For information:

CIRCLE 145 ON READER CARD

drum memory

The model 52 system, with clocking, read-write, and address decoding elec-

new products

tronics, has an 80-track storage capacity of 10-200K bits and a data rate of 200K bps. A 60-cycle power source provides speeds of 1800 or 3600 rpm and a maximum access time of 34 or 17 msec. A 400-cycle power source for higher speeds is also available. VERMONT RESEARCH CORP., Springfield, Vt. For information:

CIRCLE 146 ON READER CARD

laboratory computers

Micro-LINK II and III are integrated circuit systems designed primarily for use as laboratory or satellite computers. Both models offer 2K-32K word memories, in increments of 2K, but II has an 8-usec cycle time, and III has a 2-usec time. A full complement of peripherals, including oscilloscope, is included in each basic system. SPEAR INC., Waltham, Mass. For information:

CIRCLE 147 ON READER CARD

computer room file

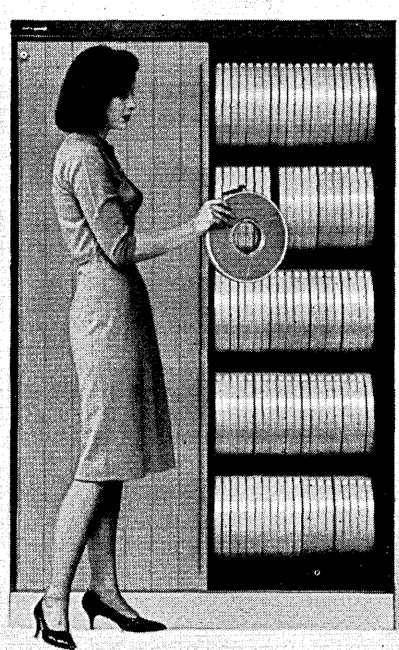
Jumbo Spacefinder file is multipurpose unit suitable for a variety of office, data processing, and computer room materials. Storage compartments in-

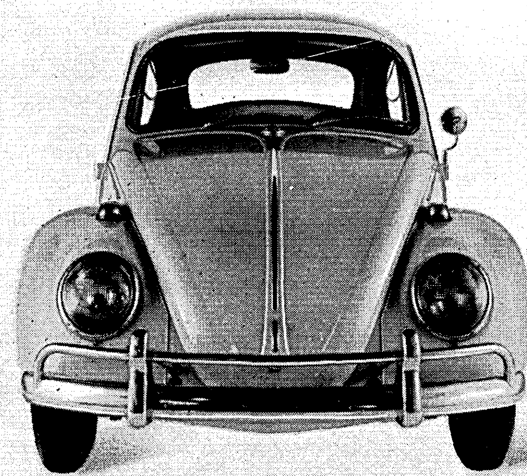
clude tape reel rack and large-document bins. TAB PRODUCTS CO., San Francisco, Calif. For information:

CIRCLE 148 ON READER CARD

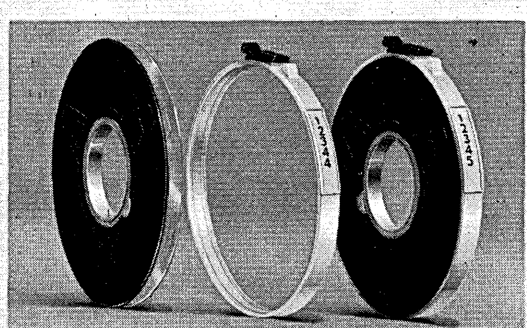
i.c. data on microfilm

The Integrated Circuit Information Retrieval System has microfilmed specs on IC's offered by a specific industry, as well as all available application notes and price lists. It is updated every 60 days. Hardware is a tabletop selector. By pushbutton, user finds a descriptor card that shows location of every spec in the file fulfilling the description. He can search in any order of descriptors and determine which





There are all kinds of space-savers.
The one on the left is called the TAPE-SEAL™ System.
It takes the bugs out of tape storage and handling.



You get a lot more mileage out of a tape library with the Tape-Seal System*. This new system for storing and handling computer tape features a unique belt that is 45% narrower and 90% lighter than a canister. Because the belt hangs in storage, it doesn't need wire supports like a canister does. In the floor space you're now using to store 96 tapes in canisters, you can store 200 in Tape-Seal Belts. Handling? A breeze. Tape protection? Better than ever. Labelling? A real pleasure, for the first time. So write for complete details soon, won't you? Before tape storage problems drive you buggy.

(When you order new tapes, insist that they be shipped without canisters. Buy Tape-Seal Belts and save.)

*Patents Pending

Wright LINE DATA PROCESSING ACCESSORIES

161 GOLD STAR BOULEVARD, WORCESTER, MASS. 01606 A division of Barry Wright Corporation BW

CIRCLE 85 ON READER CARD

new products

descriptors are excluding circuits he'd like to consider. ASCAM INC., Palo Alto, Calif. For information:

CIRCLE 149 ON READER CARD

control software

The Free-Time System package makes possible both off- and on-line computations with the GE/PAC 4000 computer line. Placing a low priority on such functions as scientific calculations, inventory control, etc., it enables these to run on a time-shared basis while the machine controls a process. G.E. PROCESS COMPUTER BUSINESS SECTION, Phoenix, Ariz. For information:

CIRCLE 150 ON READER CARD

data cell holders

Line of dp accessories to hold datacell cartridges, which must be kept upright even when removed from the drive, includes a carrying case for up to three cells plus a tape or notebook; rolling cart that holds five cells, tapes, disc packs; other carts with capacities up to 40 cells; and library fixtures holding multiples of 10. LUNDE LUGGERS, Granada Hills, Calif. For information:

CIRCLE 151 ON READER CARD

tape drive

The model SC-1080 operates bidirectionally at 150 ips, 800-bpi NRZ or 1600-bpi phase-modulated recording. It is 7- or 9-channel (IBM 729 and 360/2400 or ASCII) compatible. A single-capstan transport, it loads automatically once tape is threaded directly from the supply to the take-up reel. No pinch rollers, valves, guide rollers or air guides are used. POTTER INSTRUMENT CO. INC., Plainview, N.Y. For information:

CIRCLE 152 ON READER CARD

automatic tester

Using paper tape for the program data, the 9400 can be used for a variety of tasks by changing the tape. Results of a test, such as out-of-tolerance conditions, can be programmed to automatically stop or modify the test. Front panel keyboard allows manual insertion of data. The basic system consists of a digital voltmeter or multimeter, input scanner, tape reader, and data control unit. AUTO-DATA INC., San Diego, Calif. For information:

CIRCLE 153 ON READER CARD

new literature

TAPE RECORDING HEADS: 10-page catalogue lists three types of heads offered by manufacturer, including erase heads, record/playback heads, and combination heads that record, playback and erase. 24 basic heads are illustrated. MICHIGAN MAGNETICS, Vermontville, Mich. For copy:
CIRCLE 154 ON READER CARD

DATA CONDITIONING SYSTEM: Eight-page brochure features description of system that uses analog input and digital output and consists of compatible off-the-shelf modules. Systems may also incorporate high-level and low-level commutation or may combine the two. Brochure shows diagrams of low, high and high-low switching and lists system specifications. BECKMAN INSTRUMENTS INC., Fullerton, Calif. For copy:
CIRCLE 155 ON READER CARD

ANALOG COMPUTERS: 12-page booklet describes basic principles of analog computation and explains problem-solving technique that can be used to increase engineering efficiency. Several types of computer modules are described, and sample problems are stated and solved. ELECTRONIC ASSOCIATES INC., West Long Branch, N.J. For copy:
CIRCLE 156 ON READER CARD

COMPUTER GAMES: 43-page review shows how war operations and business activities of industrial operations can be simulated with the aid of the computer. Special developments include the use of heuristic problem-solving techniques in games, and the development of specialized computer hardware and software for gaming purposes. Order No. AD-623 091, *Computer-Aided Information Systems for Gaming*. Cost: $2. CLEARINGHOUSE, U. S. DEPT. OF COMMERCE, Springfield, Va. 22151.

PUNCHED TAPE READERS: 12-page brochure covers specifications and applications of SBR-642 and 5100 series; gives definitions, punched tape dimensions and coding standards; and shows handlers/spoolers and tape-length chart. CHALCO ENGINEERING CORP., Gardena, Calif. For copy:
CIRCLE 157 ON READER CARD

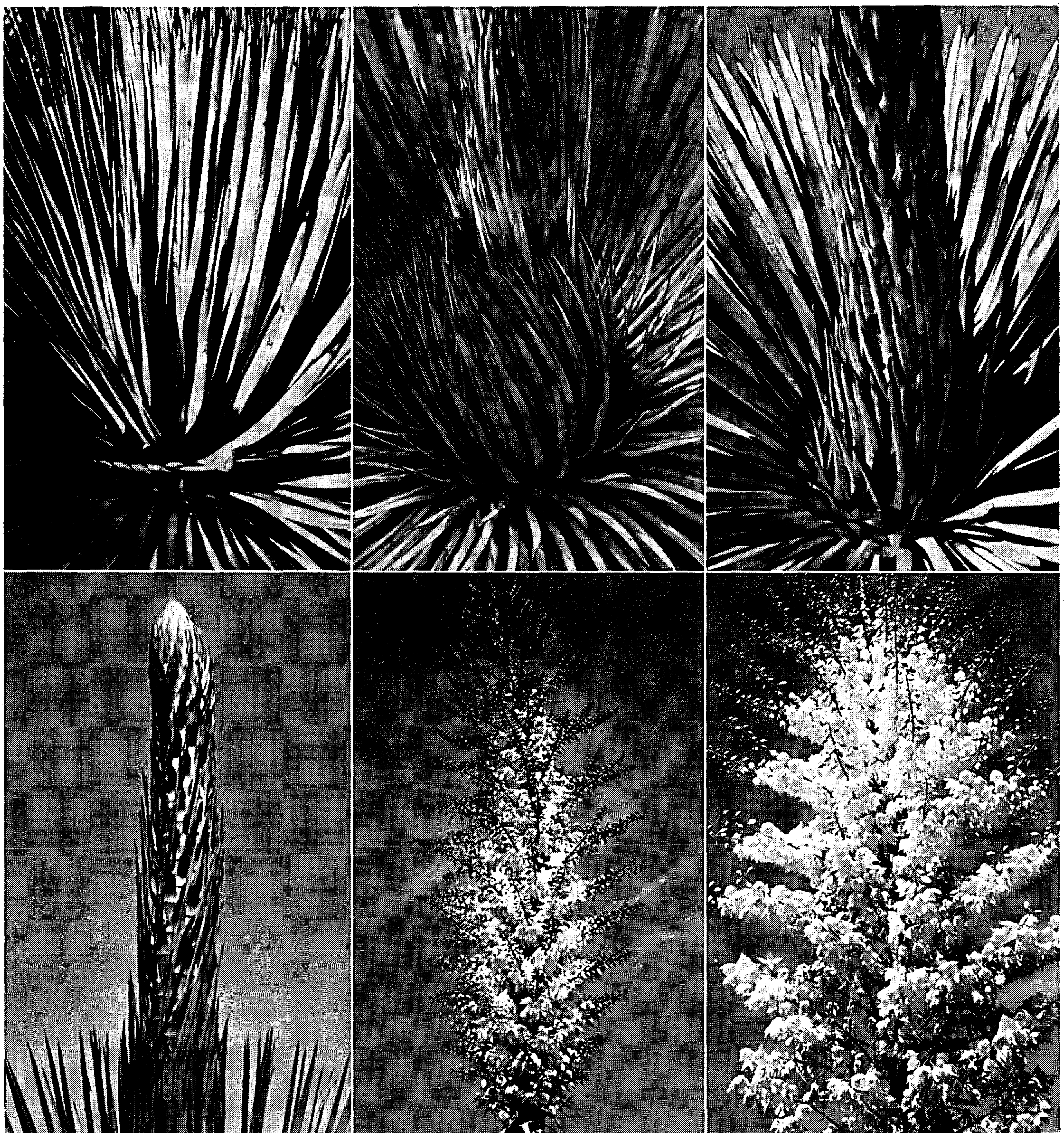
CIRCUIT TECHNOLOGY: 20-page brochure describes Solid Logic Technology (SLT), used in IBM computers. Included are sections on circuits, explanations of the concept, chip and module and circuit packaging techniques. IBM CORP., Hopewell Junction, N.Y. For copy:
CIRCLE 158 ON READER CARD

DATA COMMUNICATIONS SYSTEM: How terminal equipment is being used in a variety of different data communications systems is described in 10-page brochure. Included are systems in use for billing, ordering and distributing, centralized accounting operations and inventory control. Examples include businesses from food processing and drug manufacturing to steel production, investment banking, trucking and electricity. TELETYPE CORP., Skokie, Ill. For copy:
CIRCLE 159 ON READER CARD

DP IN INSURANCE: 71-page report prepared for the Dept. of Labor, covers various aspects of this industry and has chapters on extent, pace, developments and outlook of office automation, employment in dp jobs, impact of dp on employment trends, and outlook and implications for the next decade. Report resulted from two mail surveys in 1963, covering over 400 companies, having nearly 90% of the industry's employment. Cost: $.45. Bulletin No. 1468. SUPERINTENDENT OF DOCUMENTS, U.S. Government Printing Office, Wash., D. C. 20402.

FUNCTION MODULES: 12-page bulletin describes function modules and their use in control systems. Also included are general specifications for over 30 encapsulated analog function modules and descriptions of controllers, recorders, transmitters, preamplifiers, and computers which utilize modules. CONSOLIDATED ELECTRODYNAMICS CORP., Pasadena, Calif. For copy:
CIRCLE 160 ON READER CARD

MANUFACTURING CONTROL: Four-page booklet covers descriptions of inventory control methods, linear pro-



new literature

gramming, discrete production resource allocation, stochastic simulation, data collection, user benefits and services associated with the total system approach. MCDONNELL AUTOMATION CENTER, St. Louis, Mo. For copy:

CIRCLE 161 ON READER CARD

PRESET COUNTER: Two-page bulletin describes model PR-40, which is lightweight, small size, built with integrated circuits. Single or dual channel models may be used in industrial counting, batching and measuring applications with photoelectric, magnetic, or other transducers. Counting speeds from dc to 1-megacycle. UNITED COMPUTER CO., Tempe, Ariz. For copy:

CIRCLE 162 ON READER CARD

INDUSTRIAL COMPUTER SYSTEM: 12-page booklet illustrates how PCP 88 computers are used in master-slave relationship. Explained are parallel cascade processing, how the control system operates and is programmed, and how the supervisory computer functions. Center spread shows four compatible system configurations. THE FOXBORO CO., Foxboro, Mass. For copy:

CIRCLE 163 ON READER CARD

TECHNIQUES FOR TABLE LOOK-UP: Designed for practicing programmers who understand basic computer programming, 21-page book explains how to search via the sequential, the merge, binary, formula, and the computed position look-up. Cost: $1; microfiche $.50. No. K-DP-515. CLEARINGHOUSE, U.S. DEPT. OF COMMERCE, Springfield, Va. 22151.

CONTROLLED COMPUTER ROOM SYSTEMS: Four-page booklet illustrates and describes environment and operating cooling systems designed for computer rooms in banks, laboratories, hospitals and other commercial and industrial buildings. General specifications and data are listed. BLAZER CORP., East Rutherford, N.J. For copy:

CIRCLE 164 ON READER CARD

VIDEOFILE DOCUMENT STORAGE & RETRIEVAL SYSTEM: 12-page booklet explains the concept of recording document images on mag tape, and covers frame size, recording a document, organizing the file, ordered and random filing, updating and file expansion, videofile system modules, and features a flow chart of document filing and retrieving. Remote stations and uses of videofile system are also included. AMPEX CORP., Redwood City, Calif. For copy:

CIRCLE 165 ON READER CARD

CORE TEST JIG: Bulletin describes model 4031, which makes possible analysis of switching ferrite memory cores of 20, 30 and 50 mil size. Jig provides identical test circuit conditions, assuring repeatability of test results and accurate analysis of core performance. Included also are schematic diagram of the circuit and electrical specifications. COMPUTER TEST CORP., Cherry Hill, N.J. For copy:

CIRCLE 166 ON READER CARD

DIGITAL PLOTTING SYSTEM: 16-page booklet summarizes digital incremental plotting system and presents pertinent points of consideration in evolution of plotting systems. Comparative specifications and the available equipment are included. CALIFORNIA COMPUTER PRODUCTS, INC., Anaheim, Calif. For copy:

CIRCLE 167 ON READER CARD

ODP COUPONS: Six-page pamphlet provides description of original document processing coupon system. Flow charts show how payments are processed and chart compares this system with punch card and MICR books. CUMMINS-CHICAGO CORP., Chicago, Ill. For copy:

CIRCLE 168 ON READER CARD

MAG TAPE UNIT: Tape transports feature a servo-controlled single-capstan drive mechanism that eliminates tape wear and dynamic skew associated with pinch roller mechanisms. Six-page brochure describes two available standard versions: Model 95461 and 95462, and lists features and general specifications and describes control panels. SCIENTIFIC DATA SYSTEMS, Santa Monica, Calif. For copy:

CIRCLE 169 ON READER CARD

ANALOG INDUSTRIAL CONTROL SYSTEMS: Introductory section of 16-page catalog presents principles of operations with schematics of materials and fluids processing systems. Separate sections present descriptions and photography of eight physical presence sensors and matched components available to transmit, amplify, receive, record, track and control process signals from the sensor and to initiate corrective action. INDUSTRIAL CONTROLS DIV., GENERAL PRECISION, INC., Morton Grove, Ill. For copy:

CIRCLE 190 ON READER CARD

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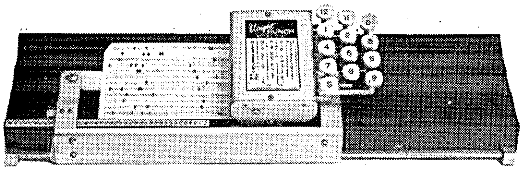

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world report

$300-MILLION NADGE SYSTEM NOW QUESTIONABLE

Fast-fading from the grasp of mainframe, communications and defense systems manufacturers is the $300 million NATO air defense and ground environment system, NADGE. On two counts this scheme looks to be coming apart at the seams. First hitch is contract price, and the second came with de Gaulle's threat to take France out of NATO. Bids were due in the fall of '65, but late specs by the NADGE Management Office caused a delay until January.

Three consortia bid, as forecast earlier here, with ITT, Westinghouse, and Hughes as primes. All are understood to have included letters stating that the full project (a computer-based defense line covering nine countries from Norway to Turkey) would demand an additional $100 million. Already stretched financially, the management office considered either cutting one country from the network or reducing the system capability. Proposals to drop Turkey were unacceptable; the result: a reduction in the long distance radar scan capability to bring costs down to original estimates.

No sooner had this been settled than the "de Gaulle bombshell" dropped amidst already harassed bidders. Problem is whether to continue NADGE for the eight other countries, and also whether to re-form members of the consortia. These had been diplomatically agreed, with French, German, and British membership included so that the European countries contributing substantially to NATO funds received business roughly proportional to their defense payments.

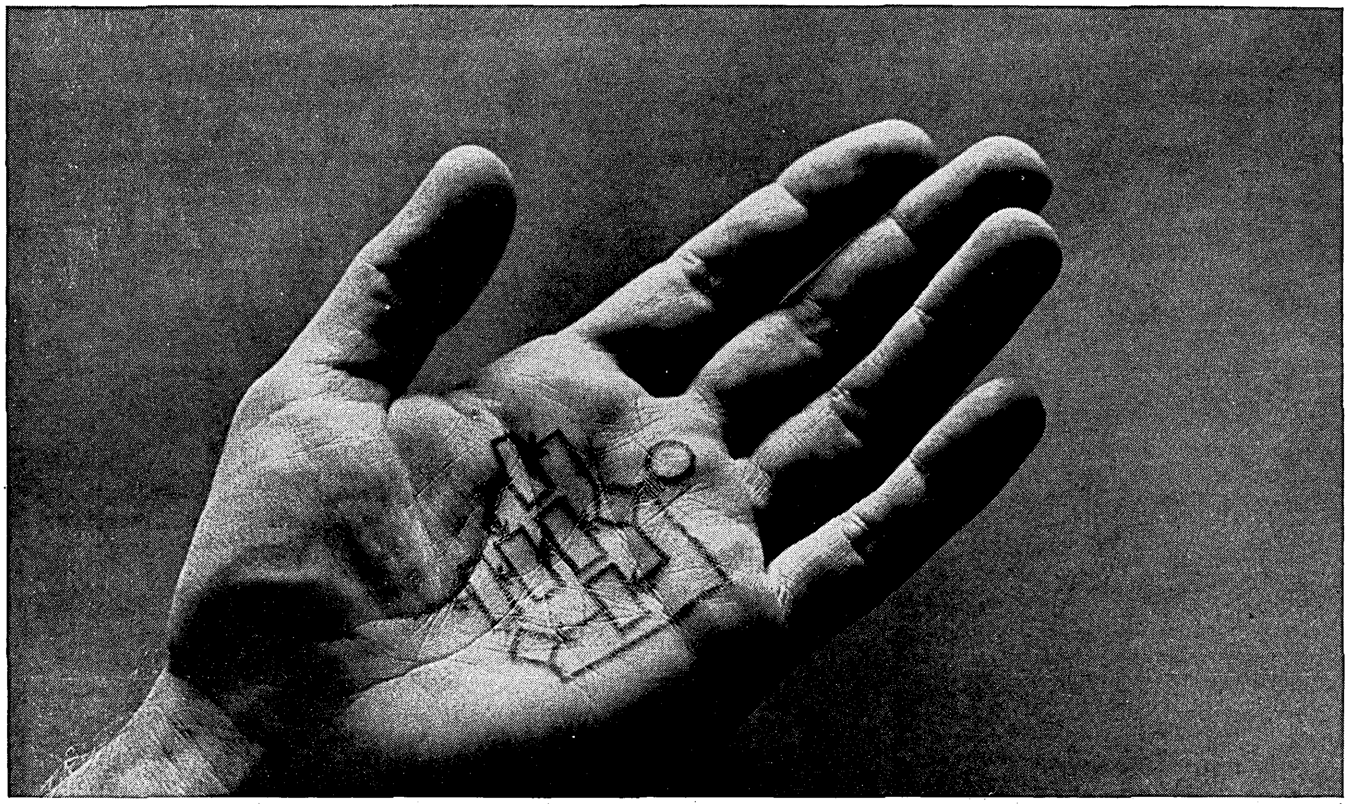
Further ramifications of this mess are likely effects on firms specifically chasing the strategic markets. Paris has become a natural base for this activity with its SHAPE and NATO offices. France, for example, is the only extra-United States territory where IBM maintains a Federal Systems Div. to serve Europe. Others are in the same boat and may perforce move if France goes ahead and contracts out of NATO.

COMPUTER ROLE IN U.K. DEFENSE GROWS

Defense is also a major issue in Britain right now. The government's budget for 1966-67 of $6.5 billion is a part of a drastic reshaping of the country's policies. But implementation depends on a return to power of the Socialistic administration after March 31 elections. On this eve of the election, political pollsters are computer processing their samples and forecasting a runaway victory for the incumbents.

Changes in defense, under Prime Minister Wilson, bring in a new fleet of cruisers with computer-based weapons systems. To be equipped with the Royal Navy's ADA (Action Data Automation), this will bring several multiple-processor contracts for real-time machines. Ferranti is tipped as a likely contract winner with its Hermes computer. This is the CPU end of a complex similar to one Ferranti installed in Britain's aircraft carrier Eagle. A second-generation Poseidon was used in the Eagle. Its successor, Hermes, is a more compact machine.

(Continued on page 151)



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• They have the chance to grow within the company, to take on new responsibilities.

• They realize all the accompanying rewards, both professionally and personally.

If you're a concerned, go-places programmer, this data could be an important factor in your "master program" for the future. Consider these points of fact. Then consider the many diversified career opportunities available at IBM's Federal Systems Division in Bethesda, Maryland, in the areas listed: Real-Time Scientific Systems, Information-Retrieval Systems, Management Information Systems, Research.

These positions require a B.S. or B.A. degree or equivalent, and at least one year's experience in information handling or programming.

To obtain more information about your future chances with IBM, write, outlining your experience, to: Mr. J. B. Farrington, Dept. 701R, IBM Federal Systems Center, Federal Systems Division, 7220 Wisconsin Avenue, Bethesda, Maryland.

It's your future.

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IBM®

(Continued from page 149)

According to a Navy systems designer, ADA has some advantages over the comparable U.S. NTDS. However, Poseidon handled logistics for administration as well as fire and command procedures. Implementing an operating system caused considerable delay to the software teams.

Approximately $100 million has been budgeted for ADA equipment and extensions to the national air traffic control complex. Major computer contracts for the latter have gone to Plessey, with smaller ones to Ferranti and Marconi. Also mentioned in the defense estimates is "a special study of future defense requirements for on-line data processing equipment, with the intention of drawing up a spec for a family of computers to meet the bulk of these needs."

GERMAN CITY PLANS FULL-TIME DP SCHOOL

What is believed to be the first full-time and local authority-sponsored school for data processing is planned for Boeblingen near Stuttgart, Germany. Of the $450,000 capital building cost, 80% is to be shouldered by the local department of education. Due for opening in 1967-68, the school will take 100 high school graduates in the 18-19 age group. 50% of the education in a 32-hour week will be in computers, the rest will be in general subjects such as languages and math. Intended to beat a possible shortage of up to 100,000 personnel by the mid-'70s, the school may be a fore-runner of others in major German cities.

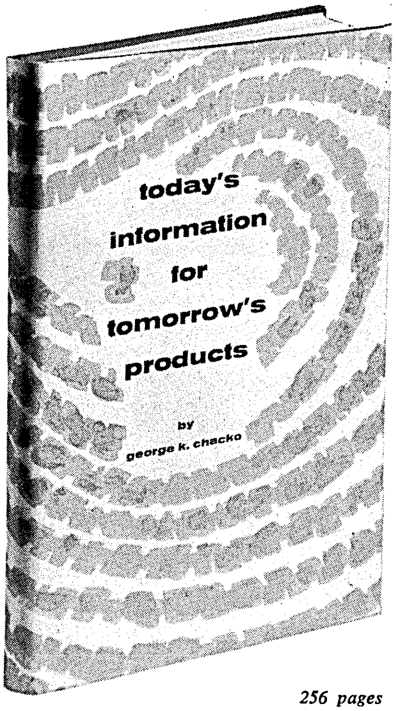
GERMAN USERS AWAIT SMALL UNIVAC COMPUTER

German salesmen unable to replace 1004's and 1005's say users are awaiting an early or late-summer Univac announcement. Supposedly, the machine will rent for upwards of $1K/month, is 360-compatible up to the mod 40, and features a 2-usec plated wire memory. Processors are said to be upgraded by a turn of a console knob, which "unmasks" surplus store, and have up to a million low-cost, plated-wire bits.

BITS & PIECES

Bull-GE has topped the 1,000 mark with orders for the Gamma 10, a $65K-plus card computer. Introduced prior to GE's takeover of the French firm, more than 500 have been delivered. ... The European Computer Manufacturers Assn. has formed a PL/I committee, TC 10. Most major European firms are represented in the 13-man group. ... London pundits figure either RCA, Univac or GE will be first with a PL/I compiler; IBM is a long shot. ... Britain's General Electric Co. (no relation) will make and market the Sigma 7 under an SDS license. ... Japan's Electronic Industries Assn. is reported to have forced Osaka Univ. to refuse an IBM 7090 donation and take a Nippon Electric 2200-500. Reason: Buy Japanese. In Europe, IBM has successfully given 90's to five key universities, accompanied by research endowments for post-graduates. ... After only two years with its IBM 1410 seat reservation system, Scandinavian Airlines approaches capacity. Consideration is being given to a new system in 1968. ... Delays in 360 deliveries reportedly has the U.K.'s Martins Bank, with five on order, looking elsewhere. In France, Shell Oil is awaiting its mod 65; the European trend-setter, though, is also shopping around.

Must reading for all concerned with operations research . . .



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an operations research approach

By George K. Chacko, The MITRE Corporation

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TODAY'S INFORMATION FOR TOMORROW'S PRODUCTS deals with operations research rather than with an assortment of mathematical techniques about information handling. It is concerned with *strategies of policy* instead of with techniques of suboptimization. Drawing its illustrations and case histories from real life, the book develops an integrated way of looking at widely varying entities that enter into decision-making with respect to tomorrow's products—consumer products, durable goods, weapons systems, space technology and hardware, and services of all types. Employing only a bare minimum of mathematics, TODAY'S INFORMATION FOR TOMORROW'S PRODUCTS will be of interest to all persons working in management research and operations, as well as to graduate and undergraduate students in these and related fields. Theory and practice are expertly blended in this highly lucid and engaging work by an international expert.

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PART IV—discusses the philosophy of information usage, presenting still another new concept—Concomitant Coalitions—and explores the implications of this concept for committing today's resources to tomorrow's plans and hopes. Throughout the book the importance of policy strategies is constantly stressed, utilizing the technique of analogy.

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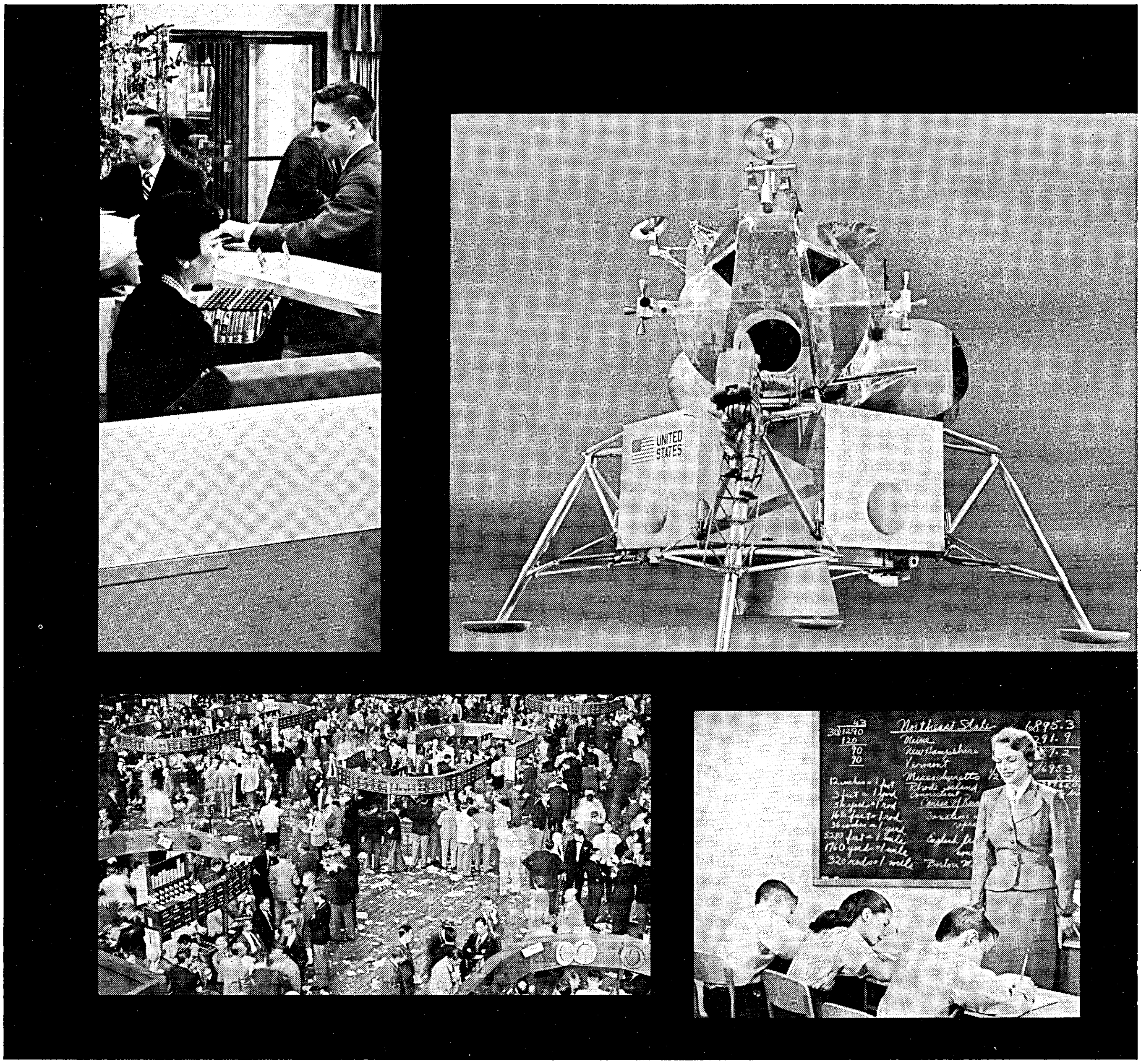
UNITED STATES

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New scientific research laboratory for high energy particle physics, located on Stanford University Campus, has openings for high level professional programmers in the following areas.

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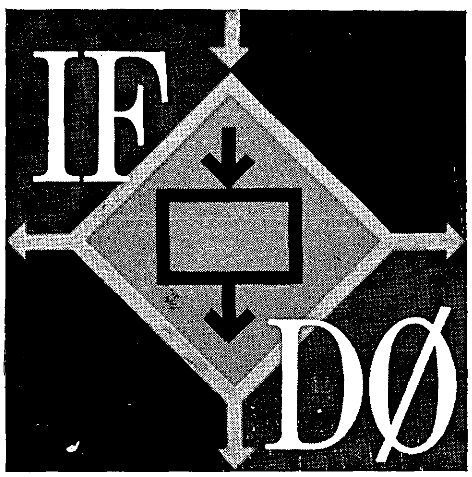

Qualified applicants will have a Master's Degree in Computer Science, Mathematics, Statistics, or Physics; or a Bachelor's of Science Degree with appropriate experience.

PROGRAMMING SYSTEMS

Responsibilities will include the development of real-time analysis and control programs, advanced assembly routines, special purpose compilers, and system simulators.

Qualified applicants will have a Master's Degree in Computer Science, or equivalent, with appropriate experience.

In addition to the opportunity to be associated with a new laboratory that will be an international center for high energy particle physics research, the above positions offer the many benefits available to career professional employees of Stanford University.

If you have education and experience in one or more of the areas mentioned above, you are invited to address your résumé to G. F. Renner, Professional Employment Manager, Stanford Linear Accelerator Center, P. O. Box 4349, Stanford, California.

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washington report

GOVERNMENT STUDY DEALS WITH COMPUTER LEASERS

Fortress IBM, under siege once again: the General Accounting Office, in a recent ruling, gave a qualified OK to a procurement procedure whereby independent leasing companies could take title to government-leased dp equipment, exercise the purchase option, and lease it back. Result would be substantially lower long-haul rentals for the user agencies, and a stifling of long-lucrative IBM lease revenues. The General Service Administration is currently conducting a census of equipment that might profitably be given such procurement treatment (or purchased outright by the government through the revolving fund authorized in the recently-enacted Brooks Bill).

Big money is involved. Currently the government is forking over almost $300 million annually for tab and computer rentals, most of this going to IBM. Having observed private concerns achieve good-sized savings through the purchase-leaseback procedure — 20% in some cases — GSA feels the same thing can be done in the government. IBM has not yet made known any official reaction to the new GSA tack; but it's a good bet some deep thinking is now going on in the appropriate executive suites. IBM's acquiescence is needed to implement the purchase-leaseback technique via lease companies, at least so thinks GAO. Since IBM contracts with the government contain a "non-assignable" clause on leased equipment, leasing companies can be designated as "agents" of the government only if IBM agrees, GAO believes. "If ... responsible officials of IBM (i.e., those who have authority to waive contract provisions such as involved here) have been or are contacted and agree to the proposed procedure ... we will interpose no legal objection to such procedure," wrote acting Comptroller General Frank Weitzel to GSA chief, Lawson Knott. Weitzel noted pointedly that no such indication has yet been forthcoming. Other government execs believe, however, IBM will not stand in the way of procurement procedures which have become standard practice in private industry for fear of antagonizing its number one customer.

FULL-TIME DP NEGOTIATORS ARE IN GSA FUTURE

In another move to streamline government dp procurement procedures, GSA has requested, and the Budget Bureau has blessed, funds in fiscal 1967 for a roving team of dp contract negotiators to "assist" civilian agencies strike better dickers with manufacturers for their goodies. Currently, these negotiations are conducted solely by agency personnel within the framework of the Federal Supply Schedules and BOB guidelines. GSA, feeling much more muscular since passage of the Brooks Bill, believes the civilian agencies would strike better deals if they draw upon the services of a full-time expert staff, rather than rely just upon the FSS and the knowledge

(Continued on page 157)

(Continued from page 155)

acquired in their once-in-a-while procurements. The new team of negotiators, to be located in the GSA HQ procurement group, will concern itself principally with the larger dp procurements, attempt to put together multi-system deals involving several agencies. This approach hopefully will enable the Government to take better advantage of its bargaining potential, cut some of the fat out of computer procurements. Undoubtedly, these helpful negotiators will again pose for the line agencies the spectre of "big brother" control over their dp operations.

HOUSE COMMITTEE PROBES COMMUNICATIONS COSTS

The high cost of transmitting data in a long-distance time-sharing hookup was one of the subjects under scrutiny in hearings held recently by the House Small Business subcommittee. Gist of the complaint was that present AT&T rates, the same as are assessed for long-distance phone calls, are not reflective of actual costs and are repressive of a promising new industry. AT&T's side of the story will be heard at a future session. Back at the FCC, where a general investigation of Ma Bell's pricing structure is under way, no sense of urgency on time-sharing rates can be discerned. The results of the present study are not likely to be ready for two years, if then. The only hope for a sooner relief, according to an FCC official, would be AT&T's voluntary lowering of these rates if its execs felt themselves being cornered. "That's one of the best ways to take the heat off something like this," he said, "... it's occasionally happened in the past."

PRESSURE MOUNTS TO OPEN EAST EUROPE MARKET

Strong pressures are being placed on the Commerce Dept. and the executive branch in general to ease the rules proscribing shipment of computers to Eastern Europe and the Soviet Union. In the next several years, it's reasoned, installation of third-generation equipment will throw scads of second-generation computers out of work, but this still-sophisticated gear can readily find homes overseas because of a still-lengthy useful life.

Better trade relations with the communist bloc is a plank in the Johnson platform, and some manufacturers point to the growing commerce in computers between the Reds and Western European nations, a market that might forever be denied the U.S. unless open trading is permitted. On the other hand, the administration is mindful of its role as leader of the Western military alliance.

A possible denouement might be the relaxation of embargoes on computers of "demonstrably civilian use," according to a top Commerce official, as a step to be taken in conjunction with the 15 other nations subscribing to the COCOM listings. The effort would still be made to hold back sale of any computers which might be construed as being of military use. It's admitted, however, the distinction between civilian and military use would be hard to maintain on computers once they have slipped behind the Iron Curtain.

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This opening calls for a BS or MS degree in chemistry, or the biological or pharmaceutical sciences desirable. Experience should include computer processing procedures and mechanized information handling techniques such as micro-image storage and display devices.

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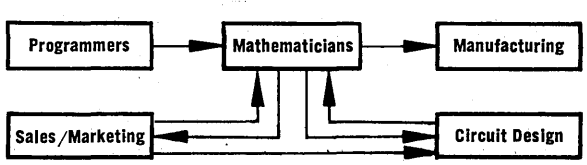

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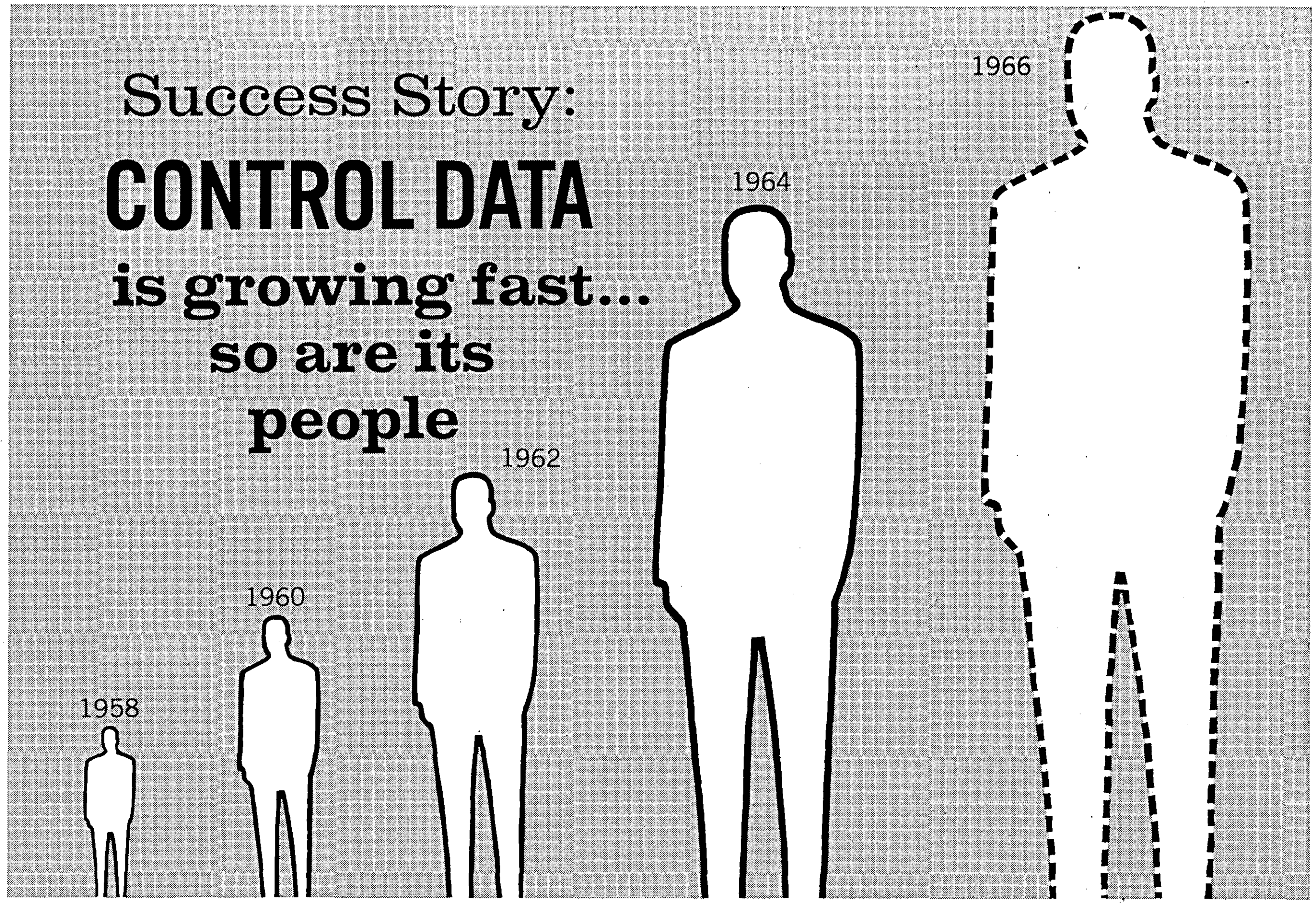

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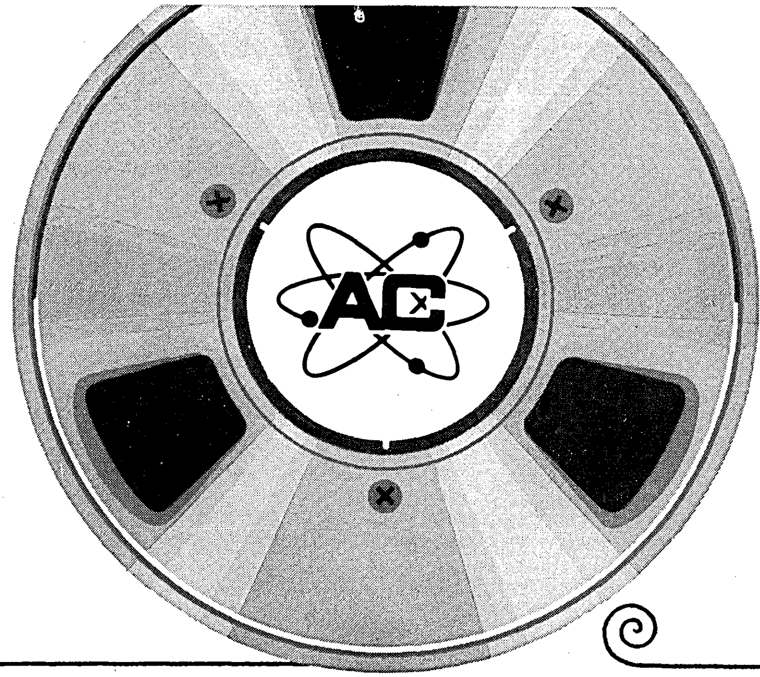
books

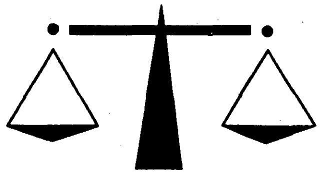
Management Operations Research, by Norbert Lloyd Enright, Holt, Rinehart and Winston, 1965.

The foreword sets a lofty aim, to describe the principles and methods of Operations Research in a simplified nonmathematical form for the practical manager and the interested student. "It should equip him to make many applications of OR himself, and caution him when he will need to call for assistance from experts."

The first of four parts deals with the general nature 'of Operations Research as a management science. The audience to which the book is directed could easily feel that management science (OR) should take over the responsibilities of, and make up for the deficiencies in, accounting, controllership, market research, and economics. The second chapter deals with a presumed conflict between traditional accounting and management science. The third chapter deals with a case history of a firm that decided to diversify instead of putting money into product research and development. The factors that management should have examined are typical of most sound management decisions, and it stretches a point to say that OR would have been the cure.

The fourth chapter has some excellent warnings about the problems of effectiveness in getting Operations Research results successfully applied in the firm. "Four seem to be particularly detrimental: (1) overemphasis on technique; (2) poor communication between the OR team and management; (3) failure to make use of the experience and judgment of operating managers; and (4) inadequate participation of management in the project." These points are amplified, and should be carefully considered by practitioners and by employers of Operations Research. "The decision to use linear programming not only cost the company money unnecessarily, but also *left management's real problem unsolved.*" "It is difficult for people with different technical backgrounds or functional responsibil-





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ities to come to agreement and understanding on a common problem." "The model was a complete waste of effort because the OR work was treated as a research project with *no appreciation of the urgency of the situation.*" (Italics supplied by reviewer.)

After this well-taken sermon on looking for the real problem instead of technique, Part Two of the book spends the next six chapters on linear programming, illustrating five different techniques of solution and a couple of case histories. There is a short chapter on MAPI analysis, two on PERT, and one on Line-of-Balance analysis.

Part Three manages to cover Inventory Management in 50 pages. Part Four deals with sampling and statistical analysis. There are several cases and problems for the student in an appendix.

The interested student will find that the tools of management science are covered so quickly as to give him little understanding of the use of these tools and techniques, and little (except Chapter Four) on how to find the right problem, how to monitor the progress of the project, how to evaluate and implement the results.

Most of the chapters seem to be based on papers that other authors have published, and fail to demonstrate any real practical experience on the part of Professor Enright.

Three matters of style make the book difficult to read.

The author uses "OR" instead of spelling out "management science" or "operations research." He treats the initials of Machinery and Allied Products Institute and Program Evaluation and Review Techniques as proper names: Mapi and Pert.

Except in Chapter 10, the tables referred to in text are located at the end of the chapter, usually five to seven pages away from the reference. Some of these tables contain the entire message of the chapter in capsule form.

Finally, the author shows little familiarity or sympathy with the power of expression possible with careful English. Fowler should have seen several sentences, of which the following may serve as an example. "Management's efforts are concerned with the utilization of the productive, financial, sales, personnel, and related resources of the company towards optimization regarding final profit."

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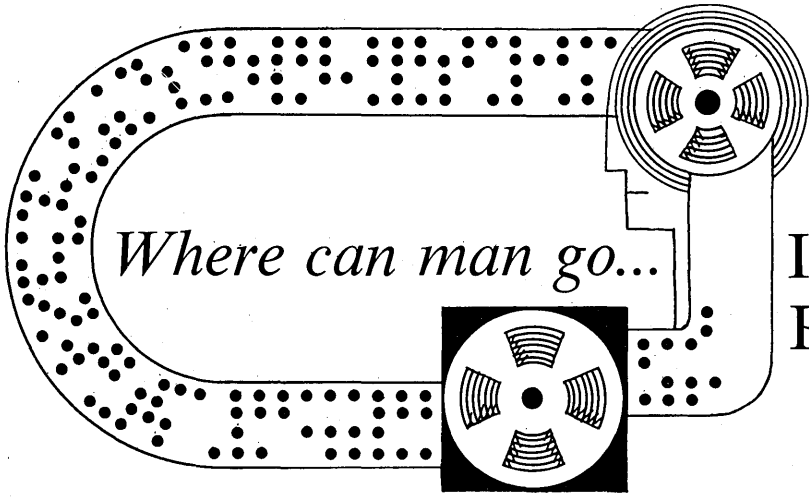

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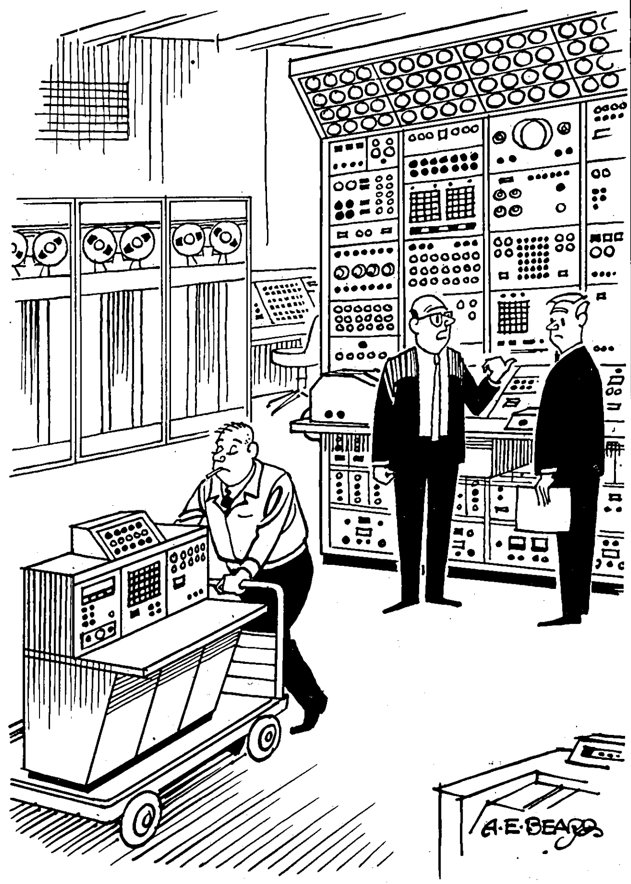

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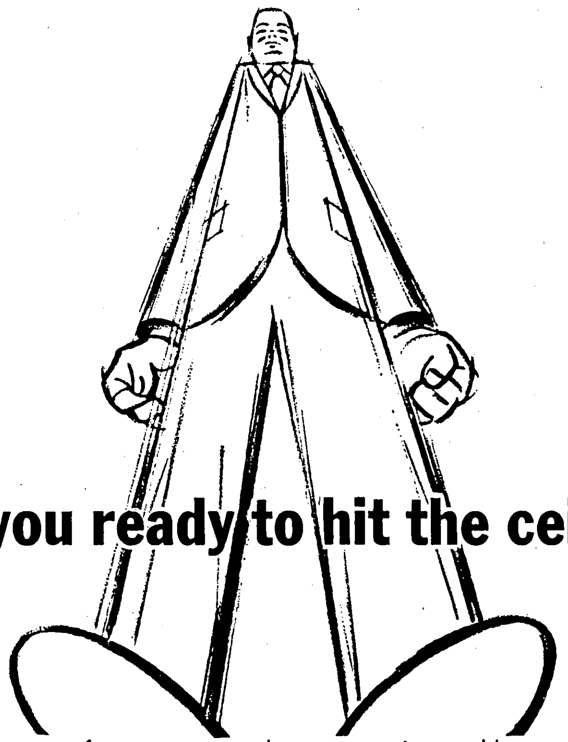

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COMMUNICATIONS — We need people who can help conceive new communications systems, recommend development programs to achieve these, and analyze special communications requirements generated by new systems concepts. Work areas include systems planning, analysis, simulation and design for command and control systems, missile and space systems and test range and weapons support systems, engineering of communication networks, range instrumentation, tactical air control, and survivable communications.

SENSOR SYSTEMS — Scientists and engineers are now needed to conduct theoretical and experimental programs on advanced radar and optical detection and tracking systems. Work includes advanced radar systems planning, design and analysis with emphasis on radar signal design, signal processing, parameter estimation, target radar characteristics, and radar coverage. Basic studies are to be conducted of sensor systems and sub-systems with focus on receiver techniques, spectrum analysis, delay-line techniques, signal processing, pulse compressors, MT and HF propagation.

TACTICAL SYSTEMS — One of our current systems engineering projects is 407L TACS (Tactical Air Control System) — a system encompassing all mobile communications systems, electronics systems and operating facilities required for command and control of deployed USAF tactical forces. Openings are available for Systems Engineers who have experience, or training in a combination of several of the following: digital data processing and displays; system test planning, instrumentation and evaluation; ground based radar systems; communications (voice and data transmission); operations analysis.

TELEMETRY — Engineers are needed to work with telemetry and instrumentation. Particular work areas include telemetry standards, systems, and techniques for both airborne and ground applications. Experience should include design or analysis of telemetry systems as well as modulation theory, RF techniques and receiving and transmitting antenna systems.

COMPUTER PROGRAMMING — People needed with experience in the development and support of monitors, compilers, real-time simulations, time-sharing systems, etc.

If you have at least three years' experience and a degree, preferably advanced, in electronics, mathematics or physics, contact us. Write in confidence to Vice President — Technical Operations, The MITRE Corporation, Box 208AU, Bedford, Massachusetts.

MITRE also maintains facilities in Washington, D. C., Patrick Air Force Base and Tampa, Florida, as well as Colorado Springs. MITRE's overseas facilities are in Paris and Tokyo.

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Pioneer in the design and development of command and control systems, MITRE was formed in 1958 to provide technical support to agencies of the United States Government. MITRE's major responsibilities include serving as technical advisor and systems engineer for the Electronic Systems Division of the Air Force Systems Command and providing technical assistance to the Federal Aviation Agency and the Dept. of Defense.

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people

■ John G. Morey, recently elected to the board of directors of the ARIES Corp., has also been chosen manager of the corporation's new offices in New York City.

■ Lawrence M. Isaacs has been appointed staff vice president, management information systems, Radio Corporation of America, New York City.

■ Robert M. Gordon has joined Scientific Data Systems, Santa Monica, Calif., as manager, applications programming. He was formerly with Raytheon Computer.

■ Milton F. Tucker has been named manager, computer communications for the McDonnell Automation Center, McDonnell Aircraft Corp., St. Louis, Mo.

■ George E. Monroe has been chosen deputy manager of the computer systems and engineering division, Planning Research Corp., Los Angeles, Calif.

■ Raymond F. Parmentier has been named manager of the Associated Spring Corp.'s new computer service center, Bristol, Conn.

■ Ralph W. Pearson will head the business development program at Computer Sciences Corp.'s new systems programming division, El Segundo, Calif. He was a former sales executive with the Burroughs Corp.

■ Yougene J. Lamar, associated with the Burroughs Corp. for 27 years, has been appointed vice president, planning, of the Uptime Corporation, Golden, Colo.

■ Systems analysts Verne Van Vlear and James L. Ryan have been added to the staff of Tymshare Inc., Los Altos, Calif., time-sharing service which opened its doors April 1.

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Professional individuals whose background and interests are in systems, engineering or applications programming are invited to submit a resume to **Mr. F. P. Wilson, Employment Manager, 460 Sierra Madre Villa, Pasadena, Calif.**

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- **COHERENT OPTICAL PROCESSING,** spatial filtering, optical correlation, electro-optical systems and components.
- **DIGITAL COMPUTER DESIGN,** systems analysis, logic and circuit design, real-time computer control.
- **ANALOG COMPUTERS AND SYSTEMS,** information theory, control theory, circuit and servo analysis, correlation techniques.
- **REAL-TIME COMPUTER PROGRAMMING,** mathematical analysis, scientific computing.

Assignments involve research and development in automatic extraction of information from photographic records, image processing and analysis, adaptive and trainable control systems, digital and hybrid computing techniques, and advanced real-time computer control applications.

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THE Bendix CORPORATION

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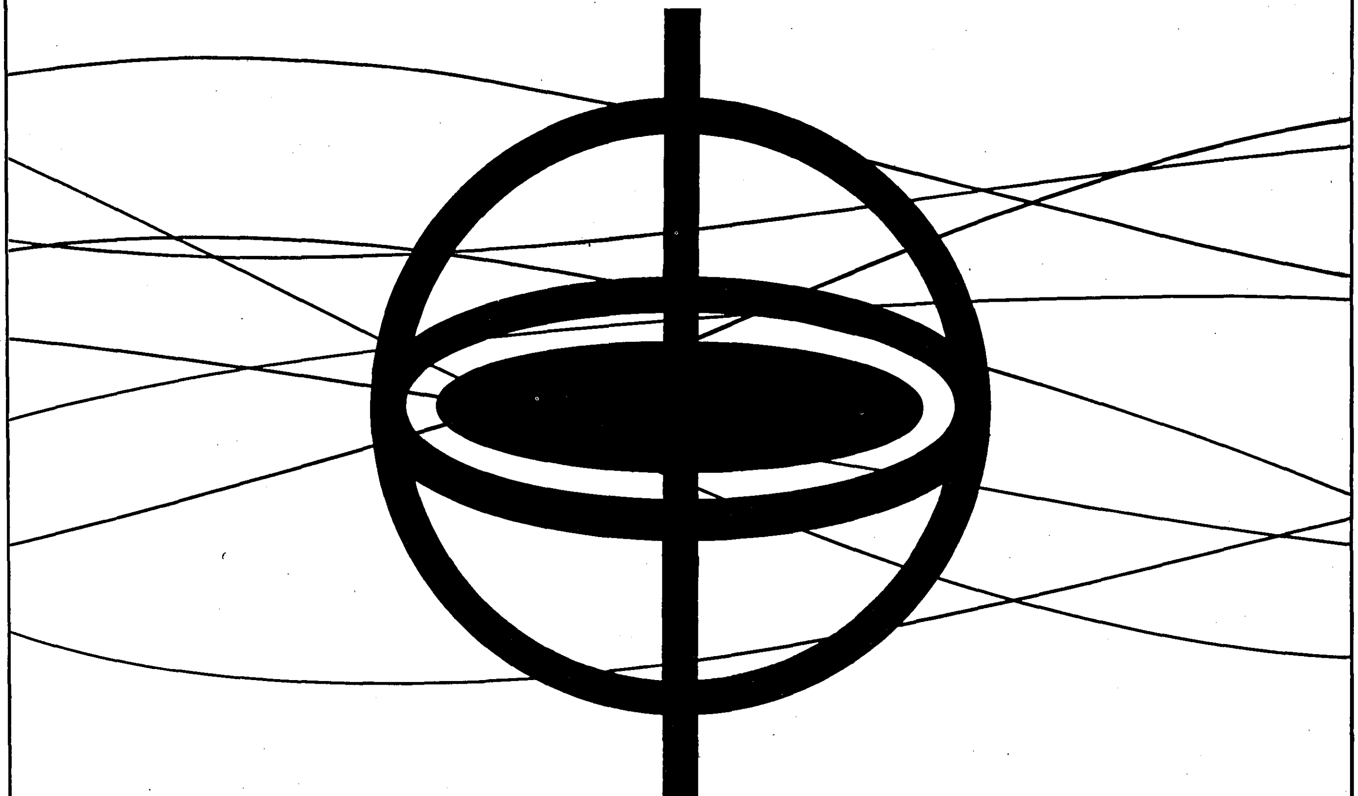
Stability



The stability of a body in motion can best be evaluated when interfering forces are severe enough to test its structure or divert it from a pre-established direction. A corporation is a body of people in motion and its stability is measured by planned achievement.

As a corporation NCR has been tested for more than 79 years. Throughout this period, direction has been maintained and objectives achieved. The objective of NCR? Better systems for business. This singleness of purpose with balanced diversification has led to growth and the TOTAL SYSTEMS concept. The products and services of NCR, made possible by practical research and development, are respected throughout the world in 120 countries.

Research and development at NCR is broad and reflects a seriously considered investment of past years. Plans for future expansion of facilities reflect a faith in the stability of the Company and in the devoted talents of NCR men of science who will add impetus to overall plans.

The stability of NCR is conducive to the advancement of career-minded scientific and engineering personnel. Creative efforts are rewarded with responsible, challenging work. Professional individuals at NCR find the personal stability, understanding and encouragement required for growth.

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Computer Engineers:

Check these Boeing assignments

Openings for computer engineers at Boeing Aerospace Group installations across the country span the entire discipline. Boeing computer facilities are among the nation's finest. The largest known single hybrid computer system in the world, for example, is at Boeing's Simulation Center at Huntsville. The others are equally distinguished. The following are some of the positions now open:

Senior Computer Engineers

Requirements include an M.S.E.E. or B.S.E.E., plus 3 to 5 years' directly related experience in computer design, computer logic design, analysis of computer controlled checkout equipment, or complex weapon systems simulation. Positions are available for:

Computer Systems Engineers—Responsibilities include conducting system studies and analyzing and translating overall system requirements into associated sub-system specifications covering both hardware and software. Duties involve providing technical support in the development and integration of digital computers for research and project programs of deep space, missile, and airborne systems, and their associated checkout equipments.

Computer Research Engineers—Assignments involve supporting planetary and missile system efforts by application of logic design optimization procedures, adaptive techniques, Boolean analysis, and hybrid functions. Duties involve performing research, conducting studies, and directing development of unique special purpose and advanced general purpose computers. Duties also include the development of special logic circuit designs and the utilization of integrated microcircuits required for advanced and unique computer implementation.

Data Processing and Display Engineers—Responsibilities include analyzing overall systems objectives and defining

Boeing Computer Center

requirements for communications, display and advanced data processing sub-systems and resolving difficult system integration problems employing microelectronic techniques. Additional duties include the simulation of complex systems by hybrid equipment, and the development of new processing and display techniques relating to sensors, instrumentation, communications, guidance and control. Positions are also available in advanced memory and display research.

Information Systems Simulation Engineers—Positions require applying simulation techniques to information systems in order to validate accuracy and adequacy of functional system design prior to physical implementation. Applicants must have a broad background in computer-oriented problem areas, and be capable of assuming major responsibilities involving both computer software and computer hardware.

Computer Systems Engineers

Requirements for the following positions are a B.S., M.S., or PhD. in engineering, physics or mathematics, preferably with experience in computer applications, computer systems analysis or related fields:

Computer Applications—Develop digital computer systems for calculating trajectories and trajectory optimization, guidance and control, loads and stresses, and temperature distributions.

Design and implement real time and near real time spacecraft performance computer programs. Assignment will involve coordination with other contractors and participation in space flight control.

Analyze and design computer programs and information processing systems to be used in support of operational command and control systems. Experience in the fields of information retrieval or query languages is desirable.

Computer Systems Analysis—Evaluate, develop and implement programming languages and compiler systems for scientific computing systems. Experience in large scale systems, design and development of compilers or major applications programs is desirable.

Develop and implement software systems for small and medium size computers used for on-line data acquisition and processing, military and space systems simulation and crew training simulators.

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the forum

The Forum is offered for readers who want to express their opinion on an aspect of information processing. Your contributions are invited.

THE INFORMATION IMPLOSION

It is a truly horrifying conclusion, but one becoming ever more tenable, that the computer has done more to aggravate man's paper work burden than to ameliorate it. What goes into a data processing system need not necessarily come out, but all too frequently the input is transduced and magnified into reports and statements of monstrous girth, which seem to serve but little purpose beyond the puzzlement and harrassment of the alleged beneficiaries of the information system. The tolerance threshold of these report recipients is remarkable, but it would probably drop considerably if management ever found out that one of their computer technicians' current preoccupations is with improvement in high-speed printer speed, there having been no significant "breakthrough" here in the past few years.

The role of the computer as a kind of paper work Sorcerer's Apprentice is viewed with alarm by Congressman Arnold Olsen (D. Mont.) who notes that forays into the "Federal Paper Work Jungle" by his subcommittee on Census and Government Statistics indicate "that any overall savings brought about by EDP are more imagined than real. In fact, there is substantial evidence available that EDP is increasing our national paper work load."*

Mr. Robert Widener, president of the New York firm Information Management Facilities, attributes this data generation and assimilation problem to the professional computer man's almost chronic inability to slim down his charge's output and make it sexy enough to attract the managerial interest it deserves. IMF specializes in the design of board rooms and briefing centers crammed with batteries of communication aids designed to transform the computer's squalid digital disgorgement into multi-hued charts and pictures, projected in wide-screen splendor for an executive audience lolling comfortably in capacious swivel chairs. (Thus, as the quarterly sales curve—color it red—is overlaid on that for the same quarter last year to show a startling dip, the president swivels abruptly to confront his sales vice-president who cringes nervously in the luminous half-light.) The most celebrated IMF installation is the windowless chamber used by the Bell System in Chicago for executive seminars on data communications.

The American Management Association has for some time sponsored a Continuing Seminar on Management Information Systems, with participants drawn from the ranks of top systems men in major U.S. companies. This seminar (which has, in fact, been continuing since 1955 with no signs of abatement) recently felt impelled to create a subcommittee on Management Control Center Systems to examine the benefits which would accrue to management by the establishment of an information management facility. The subcommittee, which presumably partakes of its parent's immortality, will study the technology associated with the organization and presentation of the products of the information system. Not surprisingly, one of the first things this new group did was to compare notes with IMF.

There has also emerged, as a rallying point for those interested in coping more effectively with the swelling torrent of indigestible data, the Society for Information Display. Although AFIPS has not yet clutched this society to its bosom, it *has* been granted diplomatic recognition by the IMF and MCCS people.

One of the things that the Society for Information Display does is hold conventions. And one of the inevitable by-products of such confabs is—you guessed it—a volume of proceedings. Thus, paradoxically, SID finds itself producing information about information and, in so doing, contributing at one level removed to the amount of data created by computer technology. And this—the generation of information that would not be needed if there were no computers generating information—brings us to Part Two of the problem.

For if there has been an explosion of information cranked out by the computer for managerial scrutiny, there has also occurred what might be termed an information implosion: an astounding increase in the amount of data *about* computers directed toward those who engineer and program the machines. Some people in the field have responded to this new challenge by saying the hell with it, resigning themselves to an ever-narrowing specialist's role with an attendant reduction in the range of technical literature with which they must be conversant.

Those of us who sense the anomaly of a general purpose computer driving its devotees into increasingly specialized professional niches must strive mightily to stay afloat on the rising sea of data. Were it not for the ACM's Computing Reviews, which surveys some 200 U.S. and foreign professional journals, and the Data Processing Digest, which covers about 150, it is likely that the technicians would go under long before the managers.

If Representative Olsen is receptive to suggestions, I would like to propose that he introduce legislation requiring that:

1. Governors be placed on all high-speed printers to limit their speed to 250 lines per minute.
2. All applications of computers to typesetting be proscribed forever, in order to nip in the bud yet another assault by the computer on information production.
3. A 50% excise tax be levied on all books and journals which contain the terms "information explosion" or "management information system."

And if any of this violates the First Amendment, then the next convention I would like to see held is a constitutional convention.

—ROBERT V. HEAD

*Hon. Arnold Olsen, "Is This Trip Necessary?" Remarks before the Washington, D. C. Chapter of the Association for Computing Machinery, January 21, 1965.

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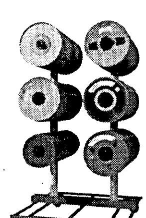

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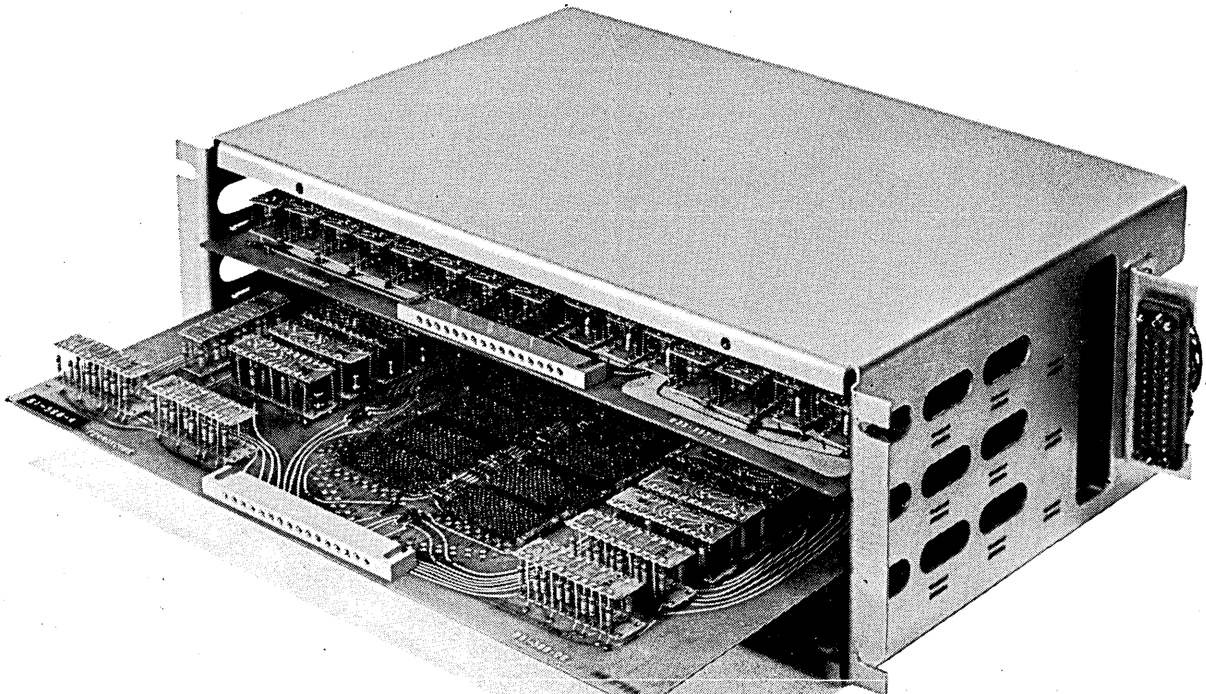

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You may wonder about the FX-12's adaptability to your operations. We've standardized a memory system with a wide range of applications: small business machines, I/O equipment, data acquisition, transmission and display systems. Now that we've got an assembly line, our core memory is priced low enough to compete with core-rope, delay line, flip-flop, relay or other small capacity memory systems. And the FX-12 is a lot more versatile and reliable than those other types. Listen to these specs:

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