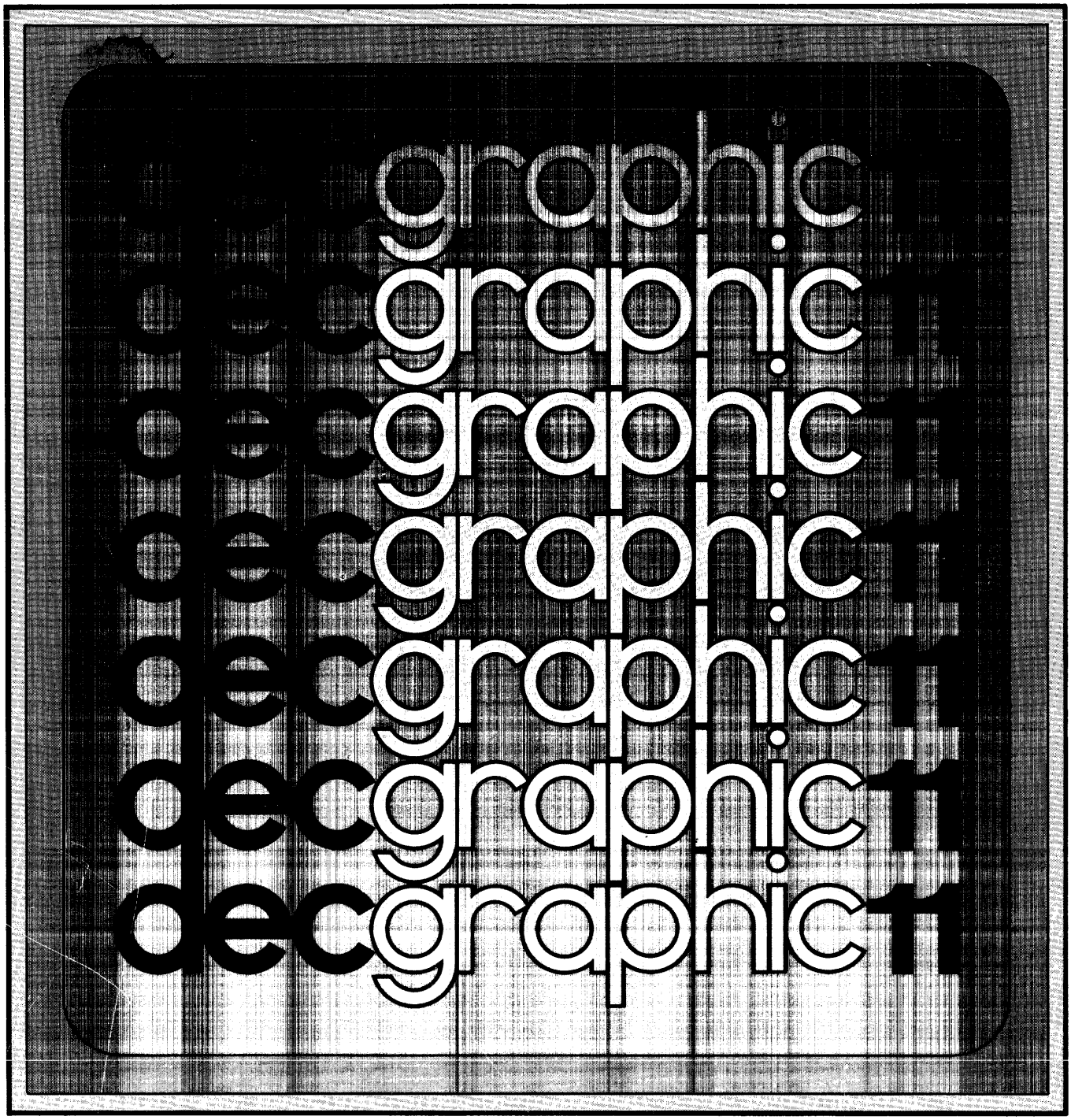
GT44
user's guide



DEC-11-HGT44-A-D

GT44
user's guide

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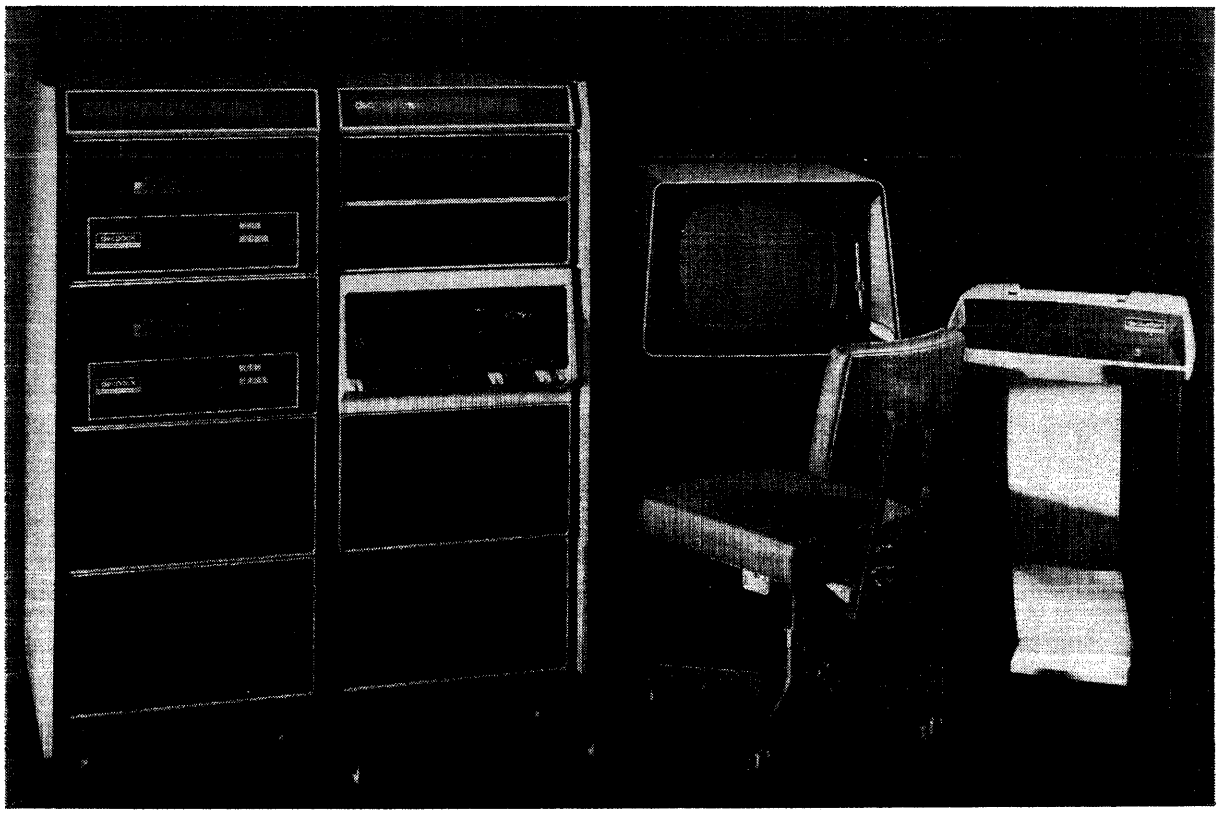


GT44 Graphics System

1.1 PURPOSE AND SCOPE

This guide describes the operation of the GT44 Graphics System. The following information is included: system description and operation, equipment specifications, controls and indicators, start-up procedures, and programming techniques. It is the intention of this guide to tie together the functional units that make up the GT44 Graphics System, to present in brief, information of relevance to the user, and to reference, where necessary, additional and more detailed sources of information.

1.2 GENERAL DESCRIPTION

The DECgraphic 11/40 GT44 Graphics System is a powerful disk-based PDP-11/40 to which graphic capabilities have been added. The GT44 is designed for applications that require a visual display, a high order of computation capability, and mass data storage. With its two disk drives, the GT44 has access to 2.4 million 16-bit words of data at any time. Its 16K of core memory allows use of an operating system such as RT-11/GT, yet leaves adequate room for user programs. The CRT monitor/light pen combination and the DECwriter provide for user-system interaction. Because graphic capabilities have been added to the software system, processor and display utilization is simplified.

1.3 SYSTEM DESCRIPTION AND OPERATION

The GT44 Graphics System comprises the following components:

a. PDP-11/40 Computer
   1. Unibus
   2. KD11 Central Processor
   3. KY11-D Programmer's Console
   4. MF11-L 16K Core Memory
   5. Power Supply

b. VT11 Graphic Display Processor

c. VR17 CRT Display Monitor

d. 375 Light Pen

e. LA30 DECwriter with DL11 Asynchronous Interface

f. Two RK05 Disk Drives with RK11-D Controller

g. BM792YB Bulk Storage Bootstrap Loader ROM.

Figure 1 shows the relationship of the GT44 components to the Unibus. The following sections briefly discuss these components.

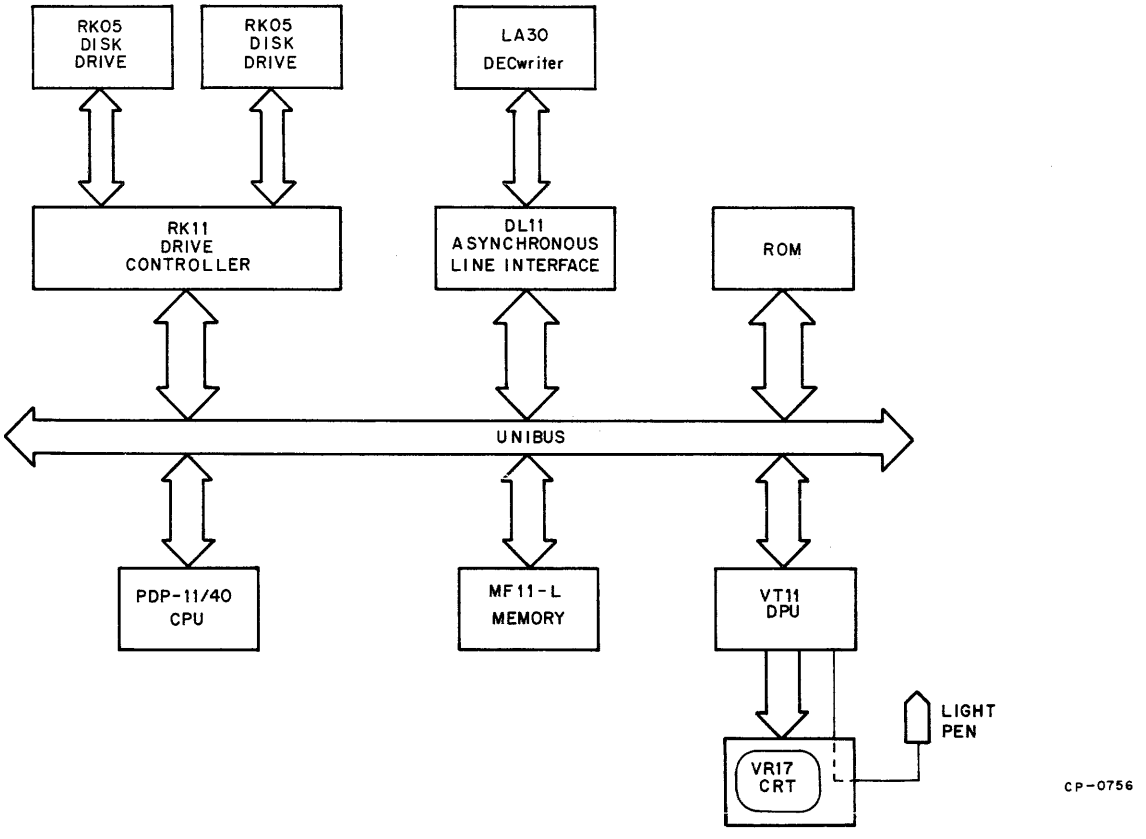


Figure 1 Relationship of GT44 Components to the Unibus

1.3.1 PDP-11/40 Computer

The PDP-11/40 is a 16-bit general purpose, parallel logic, microprogrammed computer using single and double operand instructions and 2's complement arithmetic. The PDP-11/40 contains a multiple word instruction processor, which can directly address up to 28K words of core memory. All communication among system components (including processor, core memory, and peripherals) is performed on a single high-speed bus, the Unibus. Because of the bus concept, all peripherals are compatible, and device-to-device transfers can be accomplished at the rate of 2.5 million words per second. All system components and peripherals are linked by the Unibus and power connectors, and all peripherals are in the basic system address space. Therefore, all instructions applied to data in memory can also be applied to data in peripheral device registers, enabling peripheral device registers to be manipulated by the processor as flexibly as memory.

Subsequent paragraphs present a brief functional description of the PDP-11/40.

1.3.1.1 Unibus – The Unibus provides high-speed communication between system components. With bidirectional data, address, and control lines, the Unibus allows data transfers to occur between all units on the bus, with control of the bus an important factor in these transfers. The fixed repertoire of bus operations is flexible enough for speed and design economy, yet provides a fixed specification for interfaces. The asynchronous nature of these operations also eases design and operation. The repertoire of bus operations is:

DATI, DATIP, DATO, DATOB – data operations
INTR, PTR (BR, NPR) – control operations

Full 16-bit words or 8-bit bytes of information can be transferred on the bus between the master and slave. The DATI, DATIP operations transfer data into the master; DATO, DATOB operations transfer data out of the master. When a device is capable of becoming bus master and requests use of the bus, it is for one of two purposes: to make a Direct Memory Access (DMA) transfer of data directly to or from another device or memory without processor intervention, or to INTeRrupt (INTR) program execution and force the processor to branch to a specific address where an interrupt service routine is located.

Bus control is obtained under a Non-Processor Request (NPR) for the DMA or under a Bus Request (BR) for an INTR. A device can perform a DMA after acquiring bus control via a BR.

Requests for the bus can be made at any time on the BR and NPR lines. Transfer of bus control from one device to another is made by the processor priority arbitration logic which grants control of the bus to the device having the highest priority. NPRs are accorded higher priority than BRs. The NPRs are serviced before and immediately after Unibus data cycles, in addition to specific times during WAIT or TRAP sequences. The BRs are serviced upon completion of the current instruction if the requesting priority exceeds that of the processor.

The PDP-11/40 processor has a special role in bus control operations as it performs the priority arbitration to select the next bus master. The processor assumes bus control when no other device has control.

The Unibus originates in the processor with the M981 Internal Unibus and Terminator module, which carries the Unibus from the processor to the next system unit. All 56 Unibus signals and 17 grounds are carried in this one module. A 120-conductor Mylar cable is used to connect system units in different mounting boxes or to connect a peripheral device removed from the mounting box.

A complete description of the Unibus, including specifications, is presented in the *PDP-11 Peripherals Handbook.*

1.3.1.2 KD11-A Processor – The KD11-A Processor decodes instructions; accepts, modifies, and outputs data; performs arithmetic operations; and controls allocation of the Unibus among external devices. The processor contains sixteen hardware registers, eight of which are programmable. Two of the eight programmable registers are specifically used for processor operation: a program counter (PC) and a stack pointer (SP); the remaining six serve as arithmetic accumulators, index register, and autoincrement and autodecrement registers.

The eight non-programmable registers are used for storage of a variety of functions including: intermediate address, source and destination data, a copy of the instruction register, the last interrupt vector address and console operation data.

Because of the flexibility of hardware registers, address modes, instruction set, and DMA, PDP-11/40 programs are written in directly relocatable codes. The processor also includes a full complement of instructions that manipulate byte operands and provisions for byte swapping. Either words or bytes may be displayed on the programmer's console.

Any of the eight programmable internal registers can be used to build last-in, first-out stacks. One register serves as a processor (or system) stack pointer for automatic stacking. This stack-handling capability permits save and restore of the program counter and status word in conjunction with subroutine calls and interrupts. This feature allows true reentrant codes and automatic nesting of subroutines.

The Unibus serves the processor and all peripheral devices; therefore, there must be a priority structure to determine which device becomes bus master. Generally, a device requests use of the bus for one of two reasons: to make a non-processor transfer of data directly to or from memory, or to interrupt program execution and force the processor to branch to an interrupt service routine. An NPR is granted by the processor at the end of bus cycles and allows device-to-device data transfers without processor intervention. A BR is granted by the processor at the end of an instruction and allows the device to interrupt the current processor task.

The processor recognizes four levels of hardware BRs, with each major level containing sublevels. Many devices can be attached on each major level, with the device that is electrically closest to the processor given priority over other devices on the same priority level. The priority level of the processor itself is programmable within the hardware levels; therefore, a running program can select the priority level of permissible interrupts.

Additional speed and power are added to the interrupt structure through the use of the PDP-11/40 fully vectored interrupt scheme. With vectored interrupts, the device identifies itself, and a unique interrupt service routine is automatically selected by the processor. This eliminates device polling and permits nesting of device service routines. The device interrupt priority and service routine priority are independent to allow dynamic adjustment of system behavior in response to real-time conditions.

The Unibus addresses generated by the KD11-A Processor are 18-bit direct byte addresses, even though the PDP-11/40 word length and operational logic is 16-bit word length. Thus, while the PDP-11/40 word can only contain address references up to 32K words (64K bytes), the KD11-A Processor can reference addresses up to 128K words (256K bytes).

In addition to the word length constraint on basic addressing space, the uppermost 4K words of address space are reserved for peripheral control, status, and data registers. In the basic PDP-11/40 configuration, all address references to the uppermost 4K words of 16-bit address space (160000–177777) are converted to full 18-bit references with bits 16 and 17 always set to 1. Thus, a 16-bit reference to address 173224_8 is automatically converted to a full 18-bit I/O device register address of 773224_8. Consequently, the basic PDP-11/40 configuration can address up to 28K words of core memory and 4K words of I/O device registers.

A detailed description of the KD11-A Processor is contained in the *KD11-A Processor Manual,* DEC-11-HKDAA-A-D.

1.3.1.3 KY11-D Programmer's Console – The KY11-D Programmer's Console provides the programmer with a direct system interface. The console allows the user to start, stop, load, modify, examine, step, or continue a program. Console displays indicate processor operation and the contents of the address and data registers. The console is mounted as the front panel of the processor mounting box and is connected to the processor by two cables.

The programmer's console interacts with the processor through a microprogram control located in the processor. The console contains only indicators (light-emitting diodes), switches, and the contact bounce filtering circuits for the control switches. Console operation does require certain Unibus operations through the processor: DATO for DEP and DATI for EXAM. For single-step operation, the processor responds to a Console Bus Request (CBR) whose priority supersedes all other BR priorities.

Console operation, including descriptions of all controls and indicators, is presented in Paragraph 2.1. Detailed descriptions of console logic circuits are contained in the *KD11-A Processor Manual,* DEC-11-HKDAA-A-D.

1.3.1.4 MF11-L Core Memory – The PDP-11/40 in the GT44 contains an MF11-L Core Memory with 16K word capacity. The MF11-L consists of 2 MM11-L memories mounted on a double system unit backplane. Each MM11-L is an 8K, 16-bit word memory consisting of three modules. The backplane has additional unused slots which can be used to accomodate a third optional MM11-L 8K memory.

The core memory uses the Unibus for data transfers to and from the processor and other devices. The core memory, however, is never bus master. Because of the Unibus structure, the memory can be directly addressed by the processor or any other master device. Because of double operand instructions, every location in core can function as a true arithmetic accumulator.

The memory does not enter the priority structure because it is always a slave device. The master device, however, can request use of the Unibus, and thus the memory, through either a BR or an NPR. Because the memory is completely independent of the processor, any master device can perform direct data transfers with memory without processor intervention.

1.3.1.4.1 MM11-L Core Memory – The following paragraphs briefly describe the MM11-L memories, which make up the MF11-L memory. For more detailed descriptions of the MM11-L and MF11-L memories, refer to the *MM11-S, MF11-L, and MF11-LP Core Memory Systems Manual,* DEC-11-HMFLA-B-D.

The MM11-L Core Memory is a read/write, random access, coincident current, magnetic core type memory with a cycle time of 900 ns and Unibus access time of 400 ns. The memory is organized in a 3D, 3-wire planar configuration. It provides 8192 (8K) 16-bit words that are both word and byte addressable.

The memory is organized into 16-bit words, each word containing two 8-bit bytes. The bytes are identified as the low-order byte (bits 07—00) and the high-order byte (bits 15—08). Each byte is addressable and has its own address location. Low bytes are always even numbered and high bytes are odd numbered. Full words are addressed at even-numbered locations only. When a full word is addressed, the high byte is automatically included. For example, the 8K memory has 8,192 words or 16,384 bytes; therefore, 16,384 locations are assigned. Address 000000 is the first low byte, address 000001 is the first high byte, 000002 is the second low byte, 000003 is the second high byte, etc.

The MM11-L consists of three modules: a G110 Hex module containing the memory control logic and data channels; a G231 Hex module containing the memory driver logic; and an H214 Quad module containing the memory core stack.

The memory control logic acknowledges the request of the master device, determines which of the four basic operations (DATI, DATIP, DATO, or DATOB) is to be performed, and sets up appropriate timing and control circuits to perform the desired read or write operation. It also contains the inhibit drivers and sense amplifiers as well as device selector logic to determine if the memory bank has been addressed from the Unibus. The control logic includes a 16-bit flip-flop storage register. During DATI operations, this register stores the contents of the memory location being read (destructive read) so that the data can be written back into memory (restored). The register is also used during DATO and DATOB cycles to store incoming data from the Unibus lines so that it can be written into core memory.

The memory driver logic includes: address selection logic that decodes the incoming address to determine the core specifically addressed; the switches and drivers that direct current flow through the magnetic cores to ensure the proper polarity for the desired function; and the X and Y current generators that provide the necessary current to change the state of the magnetic cores.

The ferrite core memory stack consists of 16 memory mats arranged in a planar configuration. Each mat contains 8192 ferrite cores arranged in a 128 X 64 matrix. Each mat represents a single bit position of a word. Each ferrite core can assume a stable magnetic state corresponding to either a binary 1 or binary 0. Even if power is removed from the core, the core retains its state until changed by appropriate control signals.

1.3.1.5 Power System – The PDP-11/40 power system consists of an 861 Power Controller, an H742 Power Supply, three H744 +5 V Regulators, two H745 −15 V Regulators, and interconnection and power distribution cabling.

The 861 Power Controller controls all ac power input to the processor cabinet. The controller is equipped with a circuit breaker for overload protection and a thermostat for excessive heat protection. The power controller provides switched ac outputs (uncontrolled) which provide power for the entire cabinet and related peripherals. (A second 861 Power Controller is located in the drives cabinet. The two controllers operate in parallel. The DECwriter and display monitor may be plugged into the switched outputs of either controller.)

The H742 Power Supply takes ac input power from the 861 Power Controller, generates and distributes dc power and control signals to the system, and provides ac power to the logic cooling fans and H744 and H745 regulators.

There are three control signals generated: a clock signal, a DC LO logic signal, and an AC LO logic signal. The clock signal is used by the VT11 Graphic Display Processor to synchronize the display. The AC LO and DC LO signals warn the processor of imminent power failure, allowing the processor time to perform a power-fail sequence.

The H744 and H745 regulators generate +5 V and −15 V outputs, respectively, which are distributed to the KD11-A Processor and MF11-L Memory backplanes and the KY11-D console. H744 +5 V also goes to the VT11 Graphic Display Processor backplane.

1.3.2 VT11 Graphic Display Processor

The VT11 Graphic Display Processor is the "heart" of the GT44 Graphics System. It is the VT11 that generates the displays and drives the CRT.

The VT11 processor consists of three hex-height modules that are mounted on a 4-slot systems unit backplane. The unit is mounted inside the PDP-11/40 cabinet.

The VT11 interfaces with the system by way of the Unibus. It obtains ±22 V power from the VR17 CRT and +5 V power from the PDP-11/40 power supply.

The VT11 is a high performance display processing unit that operates as a peripheral of the PDP-11/40. The VT11 is started by the central processor when a valid address is placed in the Display Processor Program Counter (DPC). The VT11 responds by issuing NPRs and fetching its display program from memory locations specified by the DPC. Once the display processor is granted control of the Unibus it can fetch its display program, and execute it independently.

The VT11 also issues interrupts to the central processor when it encounters an illegal character code or unresponsive memory. If enabled by program, it will issue an interrupt when instructed to stop, or when a light pen hit is sensed.

The VT11 is a stable device that requires only minimum adjustments because it employs a combination of digital and analog techniques as opposed to analog circuits alone. The vector function operates efficiently, providing a good compromise of speed and accuracy and assuring a precise vector calculation. The presentation and accumulation of vectors means that every point of a vector is available in digital form.

All beam position calculations are done digitally. After plotting each vector, the end-point position is automatically updated to the digitally calculated values, preventing accumulated errors or drift. Four different vector types — solid, long dash, short dash, and dot dash — are possible through standard hardware.

The VT11 character generator has both upper and lower case capability with a large repertoire of displayable characters. The display is the automatically refreshing type rather than the storage type so that a bright, continuous image, with excellent contrast ratio, is provided during motion or while changes are being made in the elements of the picture. A hardware blink feature is applicable to any characters or graphics drawn on the screen. A separate line clock input to the display processor permits the VT11 to be synchronized to line frequency.

The VT11 includes logic for descender characters such as *p* and *g*, positioning them correctly with respect to the text line. In addition to the 96 ASCII printing characters, 31 special characters are included which are addressed through the shift-in/shift-out control codes (Appendix A). These special characters include some Greek letters, architectural symbols, and math symbols. Characters can be drawn in italics simply by selecting the feature through the status instruction bit. Eight intensity levels permit the brightness and contrast to be varied so that the scope can be viewed in a normally lighted room.

The instruction set consists of five control instructions and six data formats. The control instructions set the mode of data interpretation, set the parameters of the displayed image, and allow branching of the instruction flow. Data can be interpreted in any of six different formats, allowing multiple tasks to be accomplished efficiently from both a core usage and time standpoint. The graph/plot feature of the VT11 automatically plots the X or Y axis according to preset distances as values for the opposite axis are recorded.

For a detailed description of the VT11 Graphic Display Processor see the *VT11 Graphic Display Processor Manual*. DEC-11-HVTGA-A-D.

1.3.3 VR17 Cathode Ray Tube Monitor

The VR17 is a completely self-contained CRT display that provides a 9.25 inch by 9.25 inch viewing area in a compact package. The VR17 requires only analog X and Y position information and intensity signals to generate sharp, bright displays. Except for the CRT itself, the unit is composed of all solid state circuits, utilizing high-speed magnetic deflection to enhance brightness and resolution.

In addition, the VR17 construction is modular for easy maintenance. Any subassembly or major component can be replaced in minutes, using only a screwdriver.

For a detailed description of the VR17 CRT monitor see *VR14 and VR17 CRT Display User's Manual*, DEC-12-HVCRT-D-D.

1.3.4 375 Light Pen

The 375 Light Pen is a pencil-shaped light detector for use by the operator in a wide range of interactive applications.

The 375 uses a photo-sensitive transistor for high gain and fast response. In addition, an infrared doped phosphor and matching spectral response in the photo-detector used in the 375 yields very good light pen capability, without the normally attendant visual flicker of the fast phosphor component.

The 375 is connected to the VR17 by a flexible cable attached to the front panel of the CRT monitor; it is easily removed by simply unplugging it from the CRT panel. The G840 Light Pen Amplifier is situated inside the VR17 cabinet. The output of the light pen amplifier is fed to the VT11 by way of the scope cable.

1.3.5 LA30-S DECwriter and DL11 Asynchronous Line Interface

The LA30-S DECwriter is a dot matrix impact printer and keyboard for use as a hard copy I/O terminal. It is capable of printing a set of 64 ASCII characters at speeds up to 30 characters per second on a sprocket-fed 9-7/8 inch continuous form. Data entry is from a keyboard capable of generating 128 characters.

The LA30-S is a serial asynchronous device, and therefore uses the DL11-A Asynchronous Line Interface to interface it with the Unibus. Serial information read or written by the LA30 DECwriter is assembled or disassembled by the DL11 for parallel transfer to or from the Unibus. The DL11 also formats the data from the Unibus so that it is in the format required by the LA30. The interface provides the flags that initiate these data transfers and causes a priority interrupt to indicate the availability of the LA30 DECwriter.

The DL11 transfers data via processor DATI and DATOB bus cycles. Although a DATO can be used, normal operation consists of a DATOB transfer because the LA30 DECwriter and the interface handle byte rather than word data. The interface can acquire bus control through a BR and is normally set at the BR4 priority level. Because the DL11 interface operates through an interrupt, no NPR hardware exists.

The DL11 consists of a single quad module which is installed in the processor in a Small Peripheral Controller (SPC) slot. This module contains address selection logic for decoding the incoming bus address, an interrupt control for generating the interrupt, and receiver/transmitter logic that performs the conversion and formatting functions.

The LA30 DECwriter controls and indicators are covered in Paragraph 2.1.3. A detailed description of the DECwriter is contained in the *LA30 DECwriter Maintenance Manual,* DEC-00-LA30-DD. A detailed description of the DL11 interface is presented in the *DL11 Asynchronous Line Interface Manual,* DEC-11-HDLAA-A-D.

1.3.6 RK05 Disk Drives and RK11-D Disk Drive Control

The GT44 Graphics System contains two RK05 Disk Drives. Each RK05 is a self-contained, random-access, data storage device that is especially well suited for use in small or medium size computer systems, data acquisition systems, terminals, and other storage applications. Power to the disk drives is controlled by an 861 Power Controller mounted at the bottom of the drives Cabinet. Each RK05 Disk Drive has its own internal power supply.

The RK05 is a moving-head disk drive that uses RK03-KA disk cartridges for data storage. Data is stored on both sides of the disk by a pair of movable heads, which are always positioned over opposing surfaces of the same cylinder simultaneously. Each side of the disk contains 203_{10} tracks, each of which contains 12_{10} sectors capable of storing 400_8 or 256_{10} data words.

The sector format consists of 15_8 words of preamble terminating in a sync bit, followed by a one-word header, 400_8 data words, a one-word checksum, and one word of postamble. Sector pulses signal the beginning of each sector, and an index pulse indicates the last sector, that the sector following is sector 0.

The RK11 Controller and the RK05 Disk Drives form the disk drive system, which interfaces with the PDP-11/40 processor via the Unibus. One RK11 can control up to eight RK05 Disk Drives.

The RK11 contains seven 16-bit programmable hardware registers, addressed from the Unibus, that provide the software interface between the RK11 and the Unibus. Table 1 lists these registers and their addresses. (A more detailed discussion of RK11 registers is provided in Paragraph 4.2).

Table 1
RK11 Registers

Name	Abbreviation	Address
RK11 Drive Status Register	RKDS	777400
RK11 Error Register	RKER	777402
RK11 Control Status Register	RKCS	777404
RK11 Word Count Register	RKWC	777406
RK11 Bus Address Register (Current Memory Address)	RKBA	777410
RK11 Disk Address Register	RKDA	777412
RK11 Data Buffer Register	RKDB	777416

Through software control, the RK11 can perform four control functions (Control Reset, Seek, Drive Reset, and Write Lock) and four data transfer functions (Write, Read, Write Check, and Read Check). For example, a disk data transfer is initiated by the CPU by storing a word count in RKWC, a memory address in RKBA, a disk address in RKDA, and a code for "go" and direction (read or write) in RKCS. More detailed information on the RK05 Disk Drive and the RK11-D Disk Drive Controller may be found in the *RK05 Disk Drive Maintenance Manual* (DEC-00-RK05-DB) and the *RK11-D and RK11-E Moving Head Disk Drive Controller Manual* (DEC-11-HRKDA-B-D).

1.3.7 BM792YB Bulk Storage Bootstrap Loader

The BM792YB Bootstrap Loader is a 32-word, diode matrix ROM, implemented on a quad size module, which is situated in the PDP-11/40 mounting box. The BM792YB program starting address is 773100.

The actual bootstrap loader program, stored in the first 256 words of a disk is transferred from the disk into read-write memory by the BM792-YB program. The transfer is started from location 0 of the disk and the loaded routine is assumed to be operative at read-write memory location 0. The BM792-YB program jumps to location 0 after a satisfactory completion of the transfer, so that there is automatic starting of the actual bootstrap loader program. If error conditions occur during the running of the BM792-YB program, the program starts over again.

The sequence of operations used by the bulk storage bootstrap loader is as follows:

1. It determines which device is to be read from by sensing an address set in the Switch Register.
2. It reads 256 words stored from the disk, starting with address 0 of the disk.
3. The loader then stores the 256 words in read-write memory sequential locations, starting with location 0.
4. The loader checks for errors and starts the program over if any errors occur.
5. The loader then jumps to read-write memory location 0 for automatic starting of the actual bootstrap loader program.

A program listing for the bulk storage bootstrap loader is provided in Appendix B. For a detailed description of the BM792YB bootstrap loader refer to the *BM792 Read-Only-Memory and MR11-DB Bootstrap Loader Manual* (DEC-11-HBMD-D).

1.4 EQUIPMENT SPECIFICATIONS

Specifications of the components that make up the GT44 Graphics System are covered in the following paragraphs.

1.4.1 PDP-11/40 Processor

Refer to the *PDP-11/40 Processor Handbook* for detailed coverage of PDP-11/40 specifications.

1.4.2 VT11 Graphic Display Processor

Power Input
- +5 V at 8 A
- +15 V at 100 mA
- +22 V at 500 mA
- −22 V at 500 mA

Instruction Word Length
- 16 bits

Raster Definition
- 10 bits

Viewable Area
- X = 1024 raster unit (1777_8)
- Y = 1024 raster units (1777_8)

Paper Size
- 12 bits

Hardware Blink
- Programmable

Hardware Intensity Levels
- 8

Line Frequency Synchronization
- Hardware programmable

Character Font
- 6 X 8 dot matrix

Characters/Line
- 73 (85 possible)

Number of Lines
- 42

Character Set
- 96 ASCII — upper and lower case plus 31 specials (Greek letters, math symbols, etc.) (Refer to Appendix A)

Control Characters
- Carriage return
- Line feed
- Backspace

Italics
Hardware programmable

Line Type
Solid
Long dash
Short dash
Dot-dash

Data Formats
Character (2 char/word)
Short Vector (1 word)
Long Vector (2 words)
Point (2 words)
Relative Point (1 word)
Graphplot X/Y (1 word/pt)

DPU Instructions
Set Graphic Modes
Jump
No operation (NOP)
Load Status Register A
Load Status Register B

1.4.3 VR17 CRT Display Monitor

Viewable Area
9.25 in. X 9.25 in.

Brightness
> 25 fL (measured using a shrinking raster technique)

Contrast Ratio
>10:1

Phosphor Type
P39 doped with IR

Pincushion
±1% of full scale to best-fit line

Spot Size
< 20 mils inside the usable screen area at a brightness of 30 fL, full width at half maximum (FWHM)

Jitter
< ±1/2 spot diameter

Repeatability
< ±1 spot diameter (repeatability is the deviation from the nominal location of any given spot)

Gain Change
From a fixed point on the screen, less than ±0.3% gain change for each ±1% line voltage variation

Temperature Range
0 to 50° C (operating)

Relative Humidity
10 to 90% (noncondensing)

Linearity
Maximum deviation of any straight line will be < 1% of the line length measured perpendicular to a best-fit straight line.

Deflection Method
Magnetic (70° diagonal deflection angle)

Focus Method
Electrostatic

High Voltage
10.5 kV dc nominal (voltage proportional to input line voltage). Supply is self-contained and equipped with a bleeder resistor.

Shielding
CRT is fully enclosed in a magnetic shield.

Overload Protection
Unit is protected against fan failure or air blockage by thermal cutouts. Power supply and amplifiers are current limited. Phosphor protection is provided against fault conditions.

1.4.4 375 Light Pen

Length
5.0 in. (12.7 cm)

Diameter
0.45 in. (tapered to 0.35 in.)
(1.143 cm) (0.889 cm)

Light Sensing
Phototransistor

Connector
Phone Plug

Signal Amplification
G840 Light Pen Amplifier Module in VR17 CRT Display

1.4.5 LA30 DECwriter and DL11 Asynchronous Line Interface

Printing Speed
30 characters/second, asynchronous. 30 line feeds/second, 300 ms carriage return

Line Length
80 character positions

Character Spacing
10 characters/in.

Line Spacing
6 lines/in.

Paper
9-7/8 in. wide continuous form, tractor driven (1/2 in. pitch X 9-3/8 in. wide X 0.150 in. diameter feed holes)

Copies
One part: 12 to 20 lb papers
Two part: 12 to 13 lb paper
7 to 7-1/2 lb carbon

Ribbon
4 mil Nylon, 1/2-in X 120 ft, medium inking

Typeface
5 X 7 dot matrix

Printing Characters
64 upper case ASCII subset (lower case codes print in upper case)

Keyboard Characters
97 or 128 (switch selectable)

Code
USASCII – 1968

Temperature
50° F (10° C) – 122° F (50° C)

Humidity
5 to 90% (non-condensing)

Dimensions
Depth – 24 in. (0.6 lm)
Width – 20-1/2 in. (0.5 m)
Height – 31 in. (0.79 m)

Weight
110 lb (50 kg)

DC Power Supply
Self-contained (DEC Type H735)

Power Input
115/230 Vac ± 10%
50/60 Hz
300W, maximum

Interface
DL11-A* 20 mA active current loop. Baud rate selectable from LA30 console.

1.4.6 RK05 Disk Drive and RK11-D Controller

RK05 Disk Drive

Storage Medium
Type – Single disk magnetic cartridge
Disk Diameter – 14 in.

Magnetic Heads
Number – Two

Recording Density and Format
Density – 2200 bpi max.
Tracks – 406 (200 plus 3 spares on each side of the disk)
Cylinders – 203 (two tracks each)
Sectors (records) – 4872 (12 per revolution)/6496 (16 per revolution)

Bit Capacities (unformatted)
Per Disk – 25 million
Per Inch – 2040 (max. at inner track)
Per Cylinder –115,200
Per Track – 57,600
Per Sector – 4,800/3,844

Access Times
Disk Rotation – 1500 ± 30 rpm
Average Latency – 20 ms (half rotation)
Head Positioning – 10 ms – for adjacent tracks
(including settling time) – 50 ms – average
85 ms – for 200 track movement

Bit Transfer
Transfer Code – Double frequency, nonreturn-to-zero recording
Transfer Rate – 1.44M bits per second

*DL11 Registers and Interrupts are covered in Paragraph 4.2.

Electrical Requirements

Voltage – 115/230 Vac @ 50/60 Hz
Power – 250 VA
Starting Current – Power only: 1.8A
Start spindle: 10A (for 2 seconds)

Environment

Ambient Temperature – 50° to 110° F (67° to 73° C nominal)
Relative Humidity – 8% to 80% (non-condensing)
Barometric Pressure – 30 ± 3 mm hg

Dimensions and Weight

Width – 19 in.
Depth – 26-1/2 in.
Height – 10-1/2 in.
Weight – 110 lb.

RK11-D Controller

Environmental Limits

Temperature – 60° to 110° F ambient (operating)
Relative Humidity – 20 to 80% without condensation (operating)
Vibration/Shock – To prevent data errors, extreme vibrations should be avoided while the disk drives are transferring data (operating)

Format

Drive Format –

1 disk cartridge/disk drive
203 cylinders/disk drive
2 disk surfaces/disk drive
2 tracks/cylinder
12 sectors/track

Data Word Format –

16-bit data word
$256_{10} = 400_8$ Data words/sector
$3072_{10} = 6000_8$ data words/track
$614{,}400_{10}$ data words/surface
$1{,}247{,}232_{10}$ data words/disk drive
Bit Density – approximately 2200 bpi

Recording Method – Double frequency

Data Transfer Path – Unibus NPR

2.1 OPERATING CONTROLS AND INDICATORS

The following paragraphs describe the GT44 Graphics System control switches and indicators by component.

2.1.1 PDP-11/40

The PDP-11/40 Operator's Console (Figure 2) provides the following facilities:

STATUS INDICATORS

RUN
Lights when the processor clock is running. It is off when the processor is waiting for an asynchronous peripheral data response, or during a RESET instruction. It is on during a WAIT or HALT instruction.

PROCESSOR
Lights when the processor has control of the bus.

BUS
Lights when the UNIBUS is being used.

CONSOLE
Lights when in console mode (manual operation). Machine is stopped and is not executing the stored program.

USER
Lights when the CPU is executing program instructions in User mode.

VIRTUAL
Lights when the ADDRESS Register display shows the 16-bit virtual address. Not applicable without Memory Management option.

CONSOLE SWITCHES

POWER	OFF	Power to the processor is off.
	ON	Power to the porcessor is on and all console switches function normally.
	LOCK	Power to the processor is on, but the control switches are disabled. The Switch Register is still functional.

Switch Register (Up = 1) (Down = 0)
Used to manually load data or an address into the processor.

Control Switches

LOAD ADRS (depress to activate)
Transfers contents of the Switch Register to the Bus Address Register.

Figure 2 PDP-11/40 Programmer's Console

The resulting bus address is displayed in the ADDRESS Register, and provides an address for EXAM, DEP, and START. The LOAD Address is not modified during program execution. To restart a program at the previous start location, the START switch is activated.

EXAM (depress to activate)
Causes the contents of the location specified by the bus address to be displayed in the DATA Register. If the EXAM switch is depressed again, the contents of the next sequential word location are displayed (bus address is incremented automatically). If an odd address is specified, the next lower even address word will be displayed.

CONT (depress to activate)
Causes the processor to continue operation from the point at which it had stopped. The switch has no effect when the CPU is in the RUN state. If the program had stopped, this switch provides a restart without a System Reset.

ENABLE/HALT	ENABLE	Allows the CPU to perform normal operations under program control.
	HALT	Causes the CPU to stop. Depressing the CONT switch will now cause execution of a single instruction.

START (depress to activate)
If the CPU is in the RUN state, the START switch has no effect.

If the program had stopped, depressing the START switch causes a System Reset signal to occur; the program will then continue only if the ENABLE/HALT switch is in ENABLE.

DEP (raise to activate)
Deposits contents of the Switch Register into the location specified by the bus address. If the DEP switch is raised again, the Switch Register contents (which were probably modified) are loaded into the next word location. (Bus address is incremented automatically.) If an odd address is specified, the next lower even address word will be used.

DISPLAYS

ADDRESS Register
Displays the address of data just examined or deposited. During a programmed HALT or WAIT instruction, the display shows the next instruction address.

DATA Register
Displays data just examined or deposited. During HALT, general register R0 contents are displayed. During single instruction operation, the processor status word (PS) is displayed.

A more detailed description of PDP-11/40 console switches and indicators may be found in the *PDP-11/40 System Manual,* DEC-11-H40SA-A-D.

2.1.2 VR17 CRT Display Monitor

The VR17 front panel contains:
ON-OFF/BRIGHTNESS Switch – Full counter clockwise rotation shuts off VR17 power. It also shuts off +22 V supply to the VT11 Graphic Display Processor. Clockwise rotation increases VR17 display brightness.

POWER Indicator – Lights when operating power is present.

2.1.3 LA30 DECwriter

Aside from the keyboard, the following controls and indicators are on the DECwriter console (Figure 3).

Control/Indicator	Function
READY	Lamp – Indicates power-up on printer electronics and that the DECwriter is READY for use. Indicates an interrupt is enabled by keyboard electronics, if INT bit is set by software.
LOCAL LINE FEED	Switch – When depressed, causes a local line feed to be applied to the printer without a code being sent out to the computer. This control will also disrupt printing, but no characters will be lost.
MODE LOCAL LINE	2-Position Switch – Selects either local or on-line operation.
BAUD RATE 110, 150, 300	3-Position Switch – Selects the Baud rate clock frequencies for 110, 150, and 300 Baud.

More detailed operating information may be found in the *LA30 DECwriter Manual,* DEC-00-LA30-DC.

2.1.4 RK05 Disk Drive

RK05 front panel controls and indicators (Figure 4) are listed in Table 2.

2.1.5 Circuit Breakers and Fuses

The user should be aware of the following circuit breakers and fuses. If a circuit breaker trips upon being reset, or if a fuse blows upon replacement, there is a malfunction in the system. Appropriate repair procedures should then be followed.

2.1.5.1 Circuit Breakers – There is one circuit breaker on each 861 Power Controller panel. The power controllers are located at the bottom of each GT44 cabinet. The power controller in the drives cabinet is accessed by removing the lower front panels. The power controller in the processor cabinet, and a circuit breaker mounted on the H742 Power Supply panel, are accessible by pulling the PDP-11/40 processor out on its slide mounts.

There is a circuit breaker on the rear of each RK05 Disk Drive mounting box. These are accessible through the drives cabinet rear door.

A circuit breaker, located at the rear of the LA30 DECwriter, controls its ac power.

2.1.5.2 Fuses – There are three fuses at the rear of the VR17 CRT Display Monitor marked LINE, POS, and NEG. The POS and/or NEG fuses may blow, yet leave the VR17 power indicator lit.

3.1 GT44 OPERATING PROCEDURES

The user should be familiar with all the controls and indicators previously discussed before attempting to apply procedures listed in the following paragraphs.

Figure 3 LA30 DECwriter Console

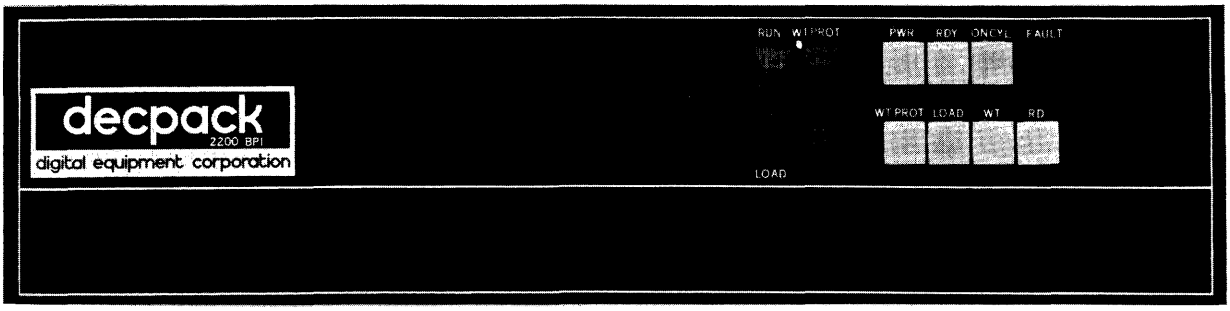


Figure 4 RK05 Controls and Indicators

Table 2
Controls and Indicators

Controls and Indicators	Description	Controls and Indicators	Description
RUN/LOAD (rocker switch)	RUN position a. locks the drive front door b. accelerates the disk to operating speed c. loads the read/write heads d. lights the RDY indicator LOAD position a. unloads the read/write heads b. stops the disk rotation c. unlocks the drive front door d. lights the LOAD indicator **CAUTION** **Do not switch to the LOAD position during a write operation, as this results in erroneous data being recorded.**	RDY (indicator)	Lights when the RK05 is ready for a read/write/seek operation.
		ON CYL (indicator)	Lights when: a. the drive is in the READY condition b. a seek or restore operation is not being performed c. the read/write heads are positioned and settled.
		FAULT (indicator)	Lights when: a. erase or write current is present without a WRITE GATE or, b. the linear positioner transducer lamp is inoperative. Goes off when the WT PROT switch is pressed or when the drive is recycled through a RUN/LOAD sequence.
WT PROT (rocker switch – spring-loaded off)	Placing this momentary contact switch in the WT PROT position lights the WT PROT indicator, prevents a write operation, and turns off the FAULT indicator if lit. Placing this switch in the WT PROT position a second time turns off the WT PROT indicator and allows a write operation.	WT PROT (indicator)	Lights when: a. the WT PROT switch is pressed or, b. the operating system sends a Write Protect command. Goes off when the WT PROT switch is pressed a second time or when the drive is recycled through a RUN/LOAD sequence.
PWR (indicator)	Lights when operating power is present.		

Table 2 (Cont)
Controls and Indicators

Controls and Indicators	Description
LOAD (indicator)	Lights when the RK05 is ready to accept a disk cartridge.
WT (indicator)	Lights when a WRITE operation occurs.
RD (indicator)	Lights when a READ operation occurs.

3.1.1 GT44 Start Up Procedures

1. Determine that the GT44 power cords are connected to an appropriate electrical outlet.
2. Turn the PDP-11/40 console key switch to the POWER position.
3. Determine that RK05 POWER indicators are lit.
4. Turn the VR17 front panel ON-OFF/BRIGHTNESS switch 3/4 of the way in the clockwise direction. The red power indicator light just below the switch should be on at this time.
5. Press the PDP-11/40 console ENABLE/HALT switch down to halt the computer.
6. Set the RK05 RUN/LOAD switch to LOAD. The LOAD indicator will light.
7. Open upper RK05 drive (System Device 0) front door and load the System Disk Cartridge. Ensure that it is properly seated and close door.
8. Ensure that the RK05 WT PROT indicator is off.
9. Set the RK05 RUN/LOAD switch to RUN. This starts disk rotation and loads the heads. When the disk reaches operating speed, the RDY indicator will light.
10. Ensure that the LA30 DECwriter is powered and on LINE.
11. Place 773100 in the Switch Register (SR). This is the starting address of the bootstrap program in the read-only memory (ROM).
12. Depress LOAD ADRS to load the address into the PDP-11/40.
13. Place 777406 in the SR. This is the address of the RK11 Disk Drive Controller Word Count Register.
14. Place the ENABLE/HALT switch to its uppermost (ENABLE) position.
15. Depress the PDP-11/40 START switch. This causes the RT-11 Monitor to be loaded into core memory and run. The Monitor will respond by printing the following on the DECwriter:

    RT-11 VXX

    - Where XX is the version number of the Monitor.

The GT44 is now ready for use. If a backup system disk is not available, a copy should now be made.

3.1.1.1 Duplicating the System Disk – The following procedure is used for duplicating the system disk:

1. With the RT-11 Monitor running on the GT44, set the RUN/LOAD switch of the lower RK05 Disk Drive (System Device 1) to LOAD.
2. When the LOAD indicator lights, open drive door and insert a blank disk cartridge. Ensure that it is properly seated and close the door.
3. Set the RUN/LOAD switch to RUN, and wait for the RDY indicator to light.
4. Ensure that the WT PROT indicator of System Device 1 is off.

5. Depress WT PROT switch of System Device 0 (the upper RK05 Disk Drive) once. Its WT PROT indicator should light.

6. On the DECwriter TYPE:

Response	Comment
R PIP <CR>	<CR> is used to indicate the Carriage Return Key.
* RK1:A=RK0:/S<CR>	
* RK1:MONITR.SYS=RK0:MONITR.SYS/U<CR>	
*	This indicates that copying is completed.

3.1.2 GT44 Failure Procedures

The following procedures should be followed in the event the GT44 fails to operate properly. If, after performing these checks, equipment operation is still unsatisfactory, the user should notify the DEC Field Service Office of the problem.

CAUTION

Do not reset any circuit breakers, or check fuses, unless the PDP-11/40 console power switch is in the OFF position. If circuit breakers trip upon being reset, or if fuses blow upon being replaced, the user should abort these failure procedures and notify the DEC Field Service Office.

If, with the PDP-11/40 console power switch in the POWER position, the GT44 is completely inoperative:

1. Check that Indicators 1 and 2 on the 861 Power Controllers are lit. If not: a) verify that the 861 controller power cords are properly seated in the wall receptacles; and b) verify that the required power (115 or 230 ac) is present at the wall receptacles.

2. Ensure that the circuit breaker (CB1) on each 861 Power Controller panel is in the ON position.

3. Ensure that the LOCAL ON-OFF-REMOTE ON switch on each 861 Power Controller panel is in the REMOTE ON position.

4. Verify that all plugs connecting to each 861 Power Controller panel are properly seated.

If, with the PDP-11/40 console power switch in the POWER position, certain unit(s) shows no power indication:

1. Determine which 861 Power Controller the unit(s) gets its power from. (The RK05 and PDP-11 obtain power from the 861 controller in their respective cabinets. The DECwriter and VR17 Display Monitor may obtain power from either controller.)

2. Check that Indicators 1 and 2 on the corresponding 861 Power Controller are lit. If not: a) verify that the controller power cord is properly seated in the wall receptacle and b) verify that the required power (115 or 230 ac) is present at the wall receptacle.

3. Ensure that the circuit breaker (CB1) on the corresponding 861 Power Controller panel is in the ON position.

4. Ensure that the LOCAL ON-OFF-REMOTE ON switch on the corresponding 861 Power Controller panel is in the REMOTE ON position.

5. Verify that all plugs connecting to the 861 Power Controller panel are properly seated.

6. Make the following checks corresponding to each unpowered unit:

PDP-11/40

a. Pull out the PDP-11/40 on its slide mounts. Check that the H742 Power Supply indicator lamp is lit. If it is off, ensure that the H742 Power Supply circuit breaker (CB1) is in the ON position. Verify that the H742 Power Supply is plugged into its power controller.

VR17 CRT Display Monitor

a. Verify that the VR17 ON-OFF/BRIGHTNESS switch is rotated 3/4 of the way in the clockwise direction.

b. Verify that the VR17 is properly plugged into a switched output of an 861 Power Controller.

c. Check the LINE fuse at the rear of the VR17. Replace if faulty.

LA30 DECwriter

a. Verify that the DECwriter is properly plugged into an 861 Power Controller.

b. Ensure that the circuit breaker (accessible at the rear door) is in the ON position.

c. Verify that paper is properly positioned in the LA30.

RK05 Disk Drives

a. Verify that the RK05 circuit breaker (CB1) at the rear of the drive mounting box is on.

If there is no CRT display:

1. Verify that the VR17 ON-OFF/BRIGHTNESS switch is rotated 3/4 of the way in the clockwise direction.

2. Check the two fuses at the rear of the VR17, marked POS and NEG. Replace if faulty.

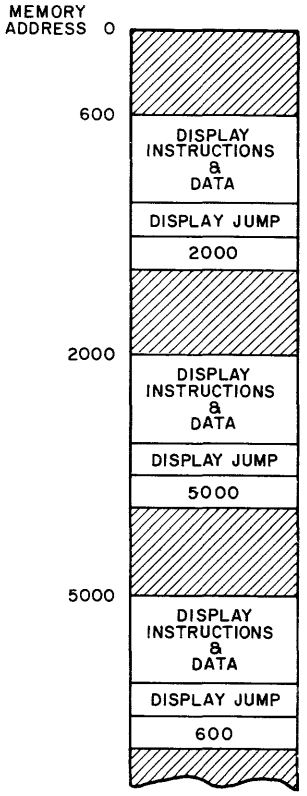
3. With power off, verify that the scope cable is firmly seated at the VR17 and at module A320 in the processor mounting box.

4.1 GT44 PROGRAMMING CONCEPT

The user should view the GT44 Graphics System as two separate programmed processors: a PDP-11/40 computer (CPU) and a display processor (DPU). The PDP-11/40 is programmed to initiate the display, and is then free to execute its own program.

All instructions available on the PDP-11/40 are executable in the GT44. Figure 1 shows the relationship of the GT44 components to the Unibus.

The DPU communicates directly with the MF11-L memory by way of non-processor requests (NPRs), i.e., DMA requests. The PDP-11/40 CPU, connected in parallel, also uses the MF11-L memory for executing its own PDP-11 code. The DPU executes display instructions stored in semi-contiguous memory locations called display lists. A memory layout example is shown in Figure 5. The Display Program Counter (DPC) in the DPU is addressed by the CPU, via the Unibus, and the data MOVed to the DPC becomes the starting address of the display list.



Shown are three "lists" of display instructions and data chained together by Display Jump instructions into one, closed display file. The shaded memory areas can be used by the CPU for PDP-11 code, data, buffer registers, etc.

Figure 5 Memory Layout Example

4.2 IMPORTANT ADDRESSES

PDP-11/40

CPU General Registers (only console addressable)	R0	777700
	.	.
	.	.
	.	.
	R7	777707

NOTE

All addresses are Unibus addresses; Unibus address bits (17:16) are automatically set to 1, if address bits (15:13) are 1s. Thus address 177700 becomes 777700. All addresses are in octal.

Switch Register (Read Only) 777570
Display Register (Write Only)

CPU Status Register (Read/Write except for bit 4 which is Read only) 777776

Contents:

Carry	Bits	0
Overflow		1
Zero		2
Negative		3
Trace Trap		4
Priority		(7:5)
Not Used		(11:8)
Previous Mode		(13:12)
Current Mode		(15:14)

VT11 Graphic Display Processor

Display Program Counter (DPC) (Read/Write) 772000

If the DPU has stopped, attemping to write an odd number into this address resumes the display.

Display Status Register (Read Only) 772002

Contents:

Stop Flag	Bits	15
Mode		(14:11)
Intensity		(10:8)
Light Pen Flag		7
Shift Out		6
Edge Indicator		5
Italics		4
Blink		3
Spare (Not Used)		2
Line		(1:0)

X Status Register (Read Only) 772004

Contents:

X Position	Bits	(9:0)
Graphplot Increment		(15:10)

Y Status Register (Read Only) 772006

Contents:

Y Position	Bits	(9:0)
Character Register		(15:10)

(Note: When in the SHIFTED OUT character mode, and an illegal code ($040 \rightarrow 137_8$) is fetched, the program is interrupted. The Character Register can then be read to find the dispatch to a user routine that is used to draw some special character.)

Display Processor Interrupt Vector Addresses

Stop Interrupt = 320
Light Pen Interrupt = 324
Time Out and Shift Out Interrupt = 330
(All display interrupts are requested at level BR4)

DL11 – DECwriter Interface Addresses

Receiver Status Register (RCSR) 777560

Contents:

Not Used	Bits	(15:12)	
RCVR ACT (Receiver Active)		11	(Read Only)
Not Used		(10:8)	
RCVR DONE (Receiver Done)		7	(Read Only)
RCVR INT ENAB (Receiver Interrupt Enable)		6	(Read/Write)
Not Used		(5:0)	

Receiver Buffer Register (RBUF) 777562

Contents:

Not Used	Bits	(15:8)	
Received Data Bits		(7:0)	(Read Only)

Transmitter Status Register (XCSR) 777564

Contents:

Not Used	Bits	(15:8)	
XMIT RDY (Transmitter Ready)		7	(Read Only)
XMIT INT ENB (Transmitter Interrupt Enable)		6	(Read/Write)
Not Used		(5:3)	(Read/Write)
MAINT (Maintenance)		2	
Not Used		(1:0)	

Transmitter Buffer Register (XBUF) 777566

Contents:

Not Used	Bits	(15:8)	
TRANSMITTER DATA BUFFER		(7:0)	(Write Only)

DECwriter Interrupt Vector Addresses
(Interrupt requested at level BR4)

Keyboard Interrupt	60
Printer Interrupt	64

RK11-D Disk Controller

Drive Status Register (RKDS) 777400
(Read Only)

Contents:

Drive Ident.	Bits	(15:13)
Drive Power Low		12
High Density Disk Drive		11
Drive Unsafe		10
Seek Incomplete		9
Sector Counter OK		8
Drive Ready		7
Access Ready		6
Write Protect Status		5
Sector Counter = Sector Address		4
Sector Counter		(3:0)

Error Register (RKER) 777402
(Read Only)

Contents:

Drive Error	Bit	15
Overrun		14
Write Violation		13
Seek Error		12
Programming Error		11
Non-Existent Memory		10

Contents (Cont):

Data Late	Bit	9
Read Timing Error		8
Non-Existent Disk		7
Non-Existent Cylinder		6
Non-Existent Sector		5
Not Used		(4:2)
Checksum Error		1
Write Check Error		0

Control Status Register (RKCS) 777404

Contents:

Error	Bit	15	(Read Only)
Hard Error		14	(Read Only)
Search Complete		13	(Read Only)
Not Used		12	
Inhibit RKBA Increment		11	(Read/Write)
Format		10	(Read/Write)
Not Used		9	
Stop On Soft Error		8	(Read/Write)
Control Ready		7	(Read Only)
Interrupt On		6	(Read/Write)
Memory Extension		(5:4)	(Read/Write)
Function		(3:1)	(Read/Write)
Go		0	(Write Only)

Word Count Register (RKWC) 777406
(Read/Write)

Current Bus Address Register (RKBA) 777410
(Read/Write)

Disk Address Register (RKDA) 777412

Contents:

Drive Select	Bits	(15:13)
Cylinder Address		(12:5)
Surface		4
Sector Address		(3:0)

Data Buffer Register (RKDB) 777416
(Read Only)

Disk Drive Interrupt Vector Address 220
(requested at level BR5)

For additional information on RK11 registers, refer to *RK11-D and RK11-E Moving Head Disk Drive Controller Manual,* DEC-11-HRKDA-B-D.

BM792 Bootstrap ROM

Starting Address 773100

4.3 PDP-11/40 INSTRUCTION SET

A detailed description of the PDP-11/40 instruction set is presented in the *PDP-11/40 Processor Handbook.* This guide assumes that the reader is familiar with the PDP-11/40 instruction set and its general operation.

4.4 VT11 INSTRUCTION SET

The display processor instruction set consists of five basic instructions: Set Graphic Mode, Jump, No-Op, Load Status Register A, and Load Status Register B. Figure 6 shows the breakdown, by bit position, of each instruction. Figure 7 provides similar information for the data words that accompany the instructions.

NOTE

The user should not insert 1-bits into those positions indicated as spare or unused.

4.5 PROGRAMMING EXAMPLES

The following programming examples are meant to provide the user with a basic introduction to GT44 programming technique. They have been kept brief in order that the points being illustrated not be lost as would be the case if larger, operational program examples were used.

Table 3 is a list of suggested mnemonics for GT44 operation.

4.5.1 Initializing the Display Processor

To start the DPU, the CPU executes a short program that loads the Display (processor) Program Counter (DPC) with the starting address (SA) of the display file. The Stack Pointer must also be initialized to an address above 400_8 to prevent a stack overflow if an interrupt occurs.

Program Listing 1 illustrates these two operations.

4.5.2 Display File

The program in Program Listing 2 causes a 200_8 unit box to be drawn with the lower left corner at screen location $500,500_8$. Initially, the DPC is loaded with the starting address. Then the display parameters, e.g., intensity, are established and the mode set to Point. The four vectors are drawn after the Point is executed and, to conclude the file, the last commands reload the DPC with the display file starting address. This results in the display file being re-executed; the CRT display is refreshed.

Program Listing 1

Address	Instruction/Data	Mnemonic	Comment
1000	012706	MOV #500, R6	Initialize the
1002	500		Stack Pointer
1004	012737	MOV #SA, @ #DPC	Load the DPC
1006	2000		with SA = 2000
1010	172000		
1012	00001	WAIT	Wait (or other PDP-11 code)

Program Listing 2

Address	Instruction/Data	Mnemonic	Comment
		. = 1000	
1000	012706	MOV #500, R6	Initialize the
1002	500		Stack Pointer
1004	012737	MOV #2000, @ #DPC	Load the DPC
1006	2000		with SA = 2000
1010	172000		
1012	000001	WAIT	Wait
		. = 2000	
2000	117124		Point mode, intensity
		POINT+INT4+LPOFF	4, no light pen, no
		+BLKOFF+LINED	blink, solid lines.

Program Listing 2 (cont)

Address	Instruction/Data	Mnemonic	Comment
2002	500	500	Unintensified point
2004	500	500	at X = 500, Y = 500
2006	110000	LONGV	Long Vector mode
2010	40200	200+INTX	Δ X = 200, Δ Y = 0
2012	0	0	intensified
2014	40000	0+INTX	Δ X = 0, Δ Y = 200,
2016	200	200	intensified
2020	60200	200+INTX+MINUS	Δ X = -200, Δ Y = 0,
2022	0	0	intensified
2024	40000	0+INTX	Δ X = 0, Δ Y = -200
2026	20200	200+MINUS	intensified
2030	160000	DJMP	Jump to start of
2032	2000	2000	display file.

Note that since the parameters (intensity level, no blink, and line type) are specified in the Point instruction, they need not be re-specified in the Long Vector instruction (2006) because they will not change unless the appropriate enable bits are set. The enable bits also allow the user to change, for example, the line type but not the intensity. In this case, only the line type enable bit is changed, not the intensity enable bit. This retention of current, not-to-be-changed, values, saves both execution time and memory storage space.

4.5.3 Application of the Stop Interrupt

The Stop interrupt provides close interaction between the CPU and the DPU. The program in Program Listing 3 restarts the display after the halt and interrupt sequence. This occurs at the end of each pass.

Program Listing 3

Address	Instruction/Data	Mnemonic	Comment
		. = 1000	
1000	012706	MOV #500, R6	Initialize the
1002	500		Stack Pointer
1004	012737	MOV #2000, @ #DPC	Load the DPC with
1006	2000		SA = 2000
1010	172000		
1012	000001	WAIT	Wait for interrupt
1014	776	BR.-2	Jump back one instruction
		. = 320	DPU sends Stop interrupt
320	400	400	Address of next instruction to be executed after a Stop interrupt
322	200	200	Processor status
		. = 400	(BR level 4)
400	012737	MOV #1, @ #DPC	Resume the display
402	01		
404	172000		
406	02	RTI	Return from interrupt
		. = 2000	
2000	117124	POINT+INT4+LPOFF +BLKOFF+LINED	Point mode, intensity 4, no light pen, no blink, solid lines.

Program Listing 3 (cont)

Address	Instruction/Data	Mnemonic	Comment
2002	500	500	Unintensified point
2004	500	500	at X = 500, Y = 500
2006	110000	LONGV	Long Vector Mode
2010	40200	200+INTX	Δ X = 200, Δ Y = 0,
2012	0	0	intensified
2014	40000	0+INTX	Δ X = 0, Δ Y = 200,
2016	200	200	intensified
2020	60200	200+INTX+MINUS	Δ X = -200, Δ Y = 0
2022	0	0	intensified
2024	40000	0+INTX	Δ X = 0, Δ Y = -200,
2026	20200	200+MINUS	intensified
2030	173400	DSTOP	Enable STop interrupt, Stop
2032	160000	DJMP	Jump to start of
2034	2000	2000	display file after a Resume

After initializing the DPU, the CPU waits for an interrupt. The DPU executes the display file, eventually performing the Stop with interrupt enabled. This causes a vectored interrupt to address 320_8.

Since the Stack Pointer was initialized to 500_8, the CPU stores its processor status and program counter in location 500_8 and 476_8 respectively; it pushes them on the "stack". Once stored, the CPU goes to location 320_8 and uses its contents as the address of the interrupt routine. The CPU takes the contents of location 322_8 as its new processor status. In this example, location 400_8 is the address of the interrupt handler and the CPU proceeds to that location.

The interrupt handler simply MOVes the number 1 to the DPC which is interpreted as a Resume by the DPU. As the DPU resumes operation, it will fetch and interpret the next instruction after stopping; in this case a DJMP, back to the start of the display file. The final instruction of the interrupt handler is a Return from Interrupt (RTI), restoring the CPU to the status and location present before the interrupt, i.e., it pops two words off the stack. A computer branch back one instruction is executed, thus placing the CPU in a WAIT condition again.

4.6 PROGRAMMING RESTRICTIONS

As with any complex system, certain restrictions must be observed by the user if trouble-free operation is to be expected. In the case of the VT11, the programmer should be aware of certain programming limitations so that the hardware may be exercised more proficiently without violating hardware rules.

4.6.1 Stop and Sync, Microcoding

Stop and Sync appear in the Load Status A instruction. However, selection of both conditions in any given Load Status A instruction should be avoided. Priorities have been built into the VT11 hardware concerning the action on the microcoding of these bits. The rules are as follows:

1. Sync and Stop
   Sync will override Stop. The display will stop but will resume in sync with the line frequency.
2. Stop and Sync with Stop Interrupt Enabled
   Setting Stop with the Stop Interrupt enabled and Sync must be avoided. Under these conditions, the DPU will stop, post an interrupt, and restart automatically in sync with the line frequency. Since the Sync resume happens rather randomly with respect to the interrupt, the effect of this microcoding is undetermined.

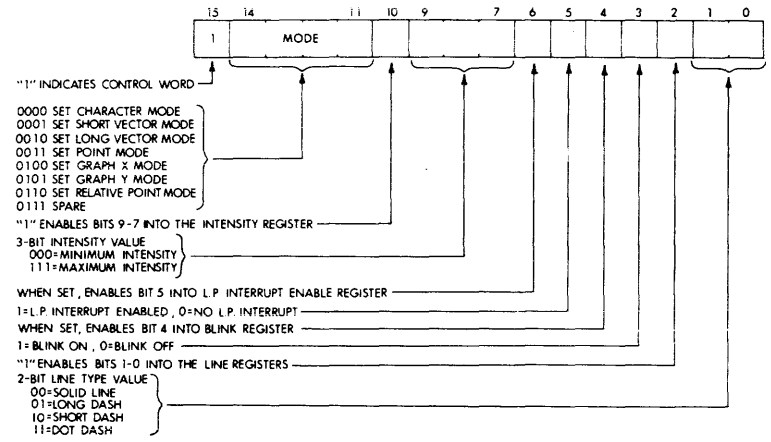
4.6.2 Display File Changes

Restarting a Running Display – Restarting the DPU while the DPU is running should be avoided. It is possible to "catch" the CPU in the middle of a bus operation causing inconsistent or undetermined operation.

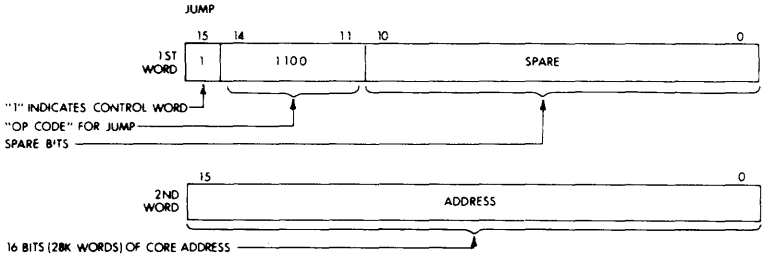
It is recommended that the DPU be halted with a Stop instruction before restarting it again.

Modification of the File – Dynamic modification of the display file should be avoided when possible. Normally the file can be modified dynamically without consequence. However, it is possible to cause problems when modifying

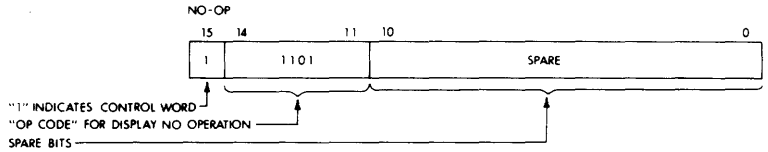
SET GRAPHIC MODE



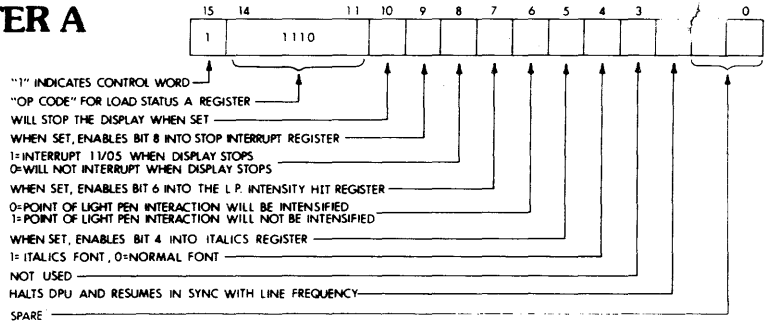
JUMP



NO-OP



LOAD STATUS REGISTER A



LOAD STATUS REGISTER B

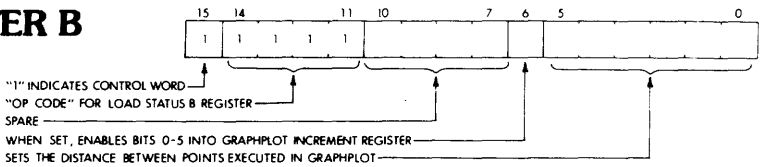
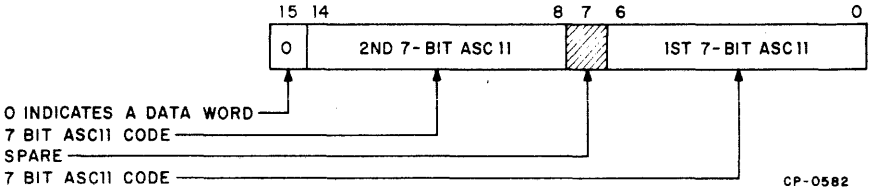
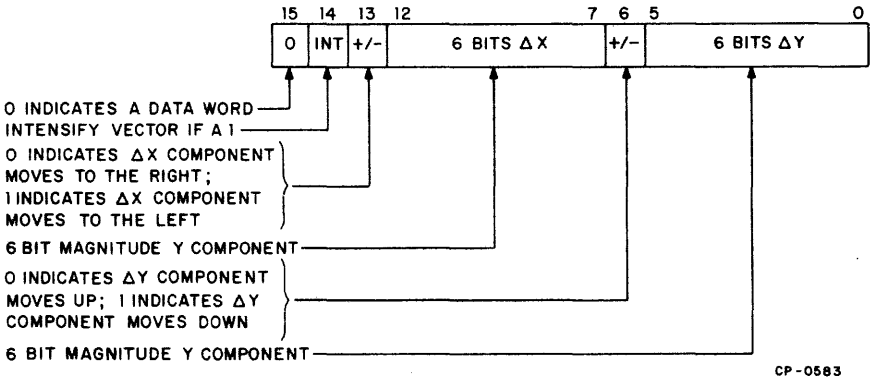


Figure 6 Instruction Word Functions

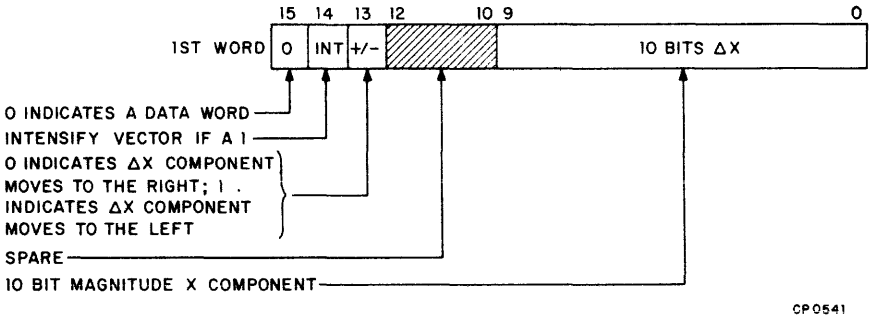
CHARACTER DATA FORMAT- Mode 0000



SHORT VECTOR MODE- Mode 0001



LONG VECTOR DATA FORMAT- 0010



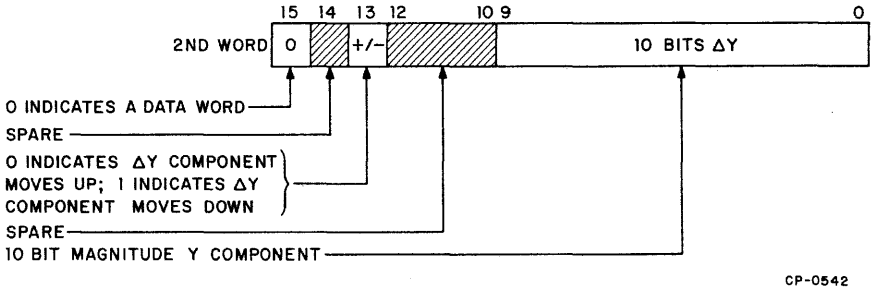
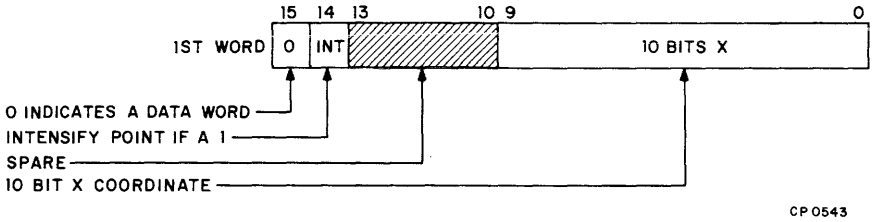
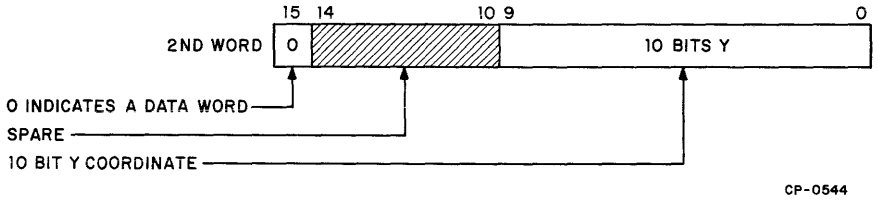


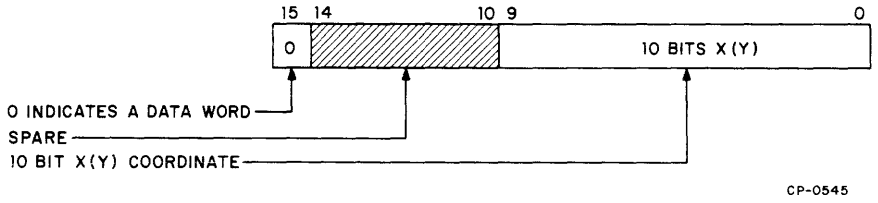
Figure 7 Data Word Formats (Sheet 1 of 2)

POINT DATA MODE- Mode 0011





GRAPHPLOT X- Mode 0100
GRAPHPLOT Y- Mode 0101



RELATIVE POINT MODE- Mode 0110

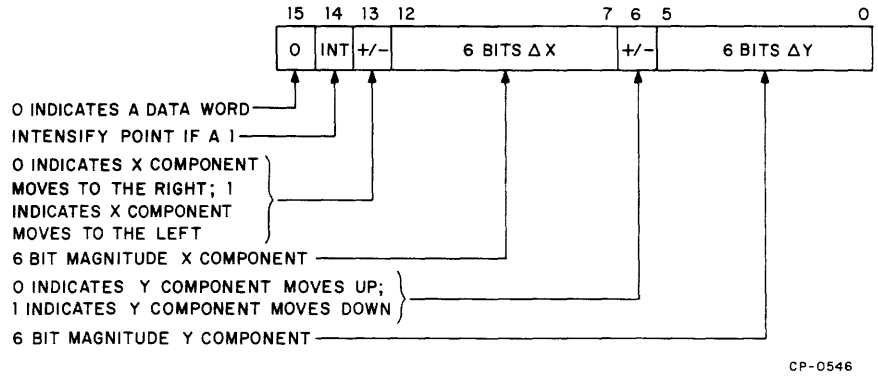


Figure 7 Data Word Formats (Sheet 2 of 2)

Table 3
Recommended GT44 Mnemonics

	Mnemonic = Value			Function
Group 1				
	CHAR	=	100000	Character Mode
	SHORTV	=	104000	Short Vector Mode
	LONGV	=	110000	Long Vector Mode
	POINT	=	114000	Point Mode
	GRAPHX	=	120000	Graphplot X Mode
	GRAPHY	=	124000	Graphplot Y Mode
	RELATV	=	130000	Relative Point Mode
	INT0	=	2000	Intensity 0 (Dimmest)
	INT1	=	2200	Intensity 1
	INT2	=	2400	Intensity 2
	INT3	=	2600	Intensity 3
	INT4	=	3000	Intensity 4
	INT5	=	3200	Intensity 5
	INT6	=	3400	Intensity 6
	INT7	=	3600	Intensity 7 (Brightest)
	LPOFF	=	100	Light Pen Off
	LPON	=	140	Light Pen On
	BLKOFF	=	20	Blink Off
	BLKON	=	30	Blink On
	LINE0	=	4	Solid Line
	LINE1	=	5	Long Dash
	LINE2	=	6	Short Dash
	LINE3	=	7	Dot Dash
Group 2				
	DJMP	=	160000	Display Jump
Group 3				
	DNOP	=	164000	Display No Operation

Table 3 (Cont)
Recommended GT44 Mnemonics

Mnemonic = Value				Function
Group 4				
	STATSA	=	170000	Load Status A Instruction
	DSTOP	=	173400	Display Stop and Interrupt
	SINON	=	1400	Stop Interrupt On
	SINOF	=	1000	Stop Interrupt Off
	LPLITE	=	200	Light Pen Hit On
	LPDARK	=	300	Light Pen Hit Off
	ITAL0	=	40	Italics Off
	ITAL1	=	60	Italics On
	SYNC	=	4	Halt and Resume in Sync
Group 5				
	STATSB	=	174000	Load Status B Instruction
	INCR	=	100	Set Graphplot Increment
Group 6 (Vector/Point Mode)				
	INTX	=	40000	Intensify Vector or Point
	MAXX	=	1777	Maximum Δ X Component
	MAXY	=	1777	Maximum Δ Y Component
	MINUSX	=	20000	Negative Δ X Component
	MINUSY	=	20000	Negative Δ Y Component
Group 7 (Short Vector Mode)				
	MAXSX	=	17600	Maximum Δ X Component
	MAXSY	=	77	Maximum Δ Y Component
	MISVX	=	20000	Negative Δ X Component
	MISVY	=	100	Negative Δ Y Component

2-word instructions such as a Display Jump. For example, if the DPU fetched the first part of a DJMP while the CPU modified the second word, the DPU will process the DJMP order code and will take the modified second word as a correct address, causing the DPU to branch to a non-intended address. It is recommended that the DPU be halted before modifying the display file and that care be exercised in selecting the sequence of commands used to modify the file.

4.6.3 Non-Flicker Display

The quality of the image displayed on the screen is determined by many factors. Primarily, the display is controlled by internal adjustments (contrast, focus, etc.) and the external BRIGHTNESS control on the front panel. However, programming is also instrumental in producing better image quality. The selectable brightness feature, one of the display parameters controlled by the Set Graphic Mode instruction, is one example of the role that programming plays. Another is the control of image flicker, the repetitive dimming and brightening of all vectors and characters on the screen. Flicker, in this case, is caused by a relatively long program execution time, i.e., the time from the beginning of the display frame until the program recycles and the display is repeated. If this time is longer than about 1/30 of a second, the screen fluorescence will decay (the image will become dimmer), and then brighten when the next frame begins, to the point where flicker is apparent. When the program time is less than 1/30 second, the display is reintensified before the image dims noticeably and there is no apparent flicker. Consequently, the objective, from a programming standpoint, is not to exceed this (1/30 second) execution period when designing a display program.

Program time, as defined above, and where vectors make up most of the display, is primarily determined by two factors: vector magnitude or length, and the number of vectors in the display frame. The longer the vectors and the greater the number of vectors the longer the display frame will be. Figure 8 shows the allowable limits, considering these two factors, for a flickerless display, defined here as display frames $\leqslant$ 32 ms (about 1/30 second). Note that a third factor is also present: the vector word to mode word ratio. If this is a 1:1 ratio, then fewer vectors are allowed because the mode word itself requires time to be decoded – time that must be subtracted from the 32 ms period. However, this time is more efficiently used when the ratio increases, i.e., when a mode word is accompanied by a number of vectors; the total number of allowable vectors is increased. This is shown in Figure 8 as the shaded area for each vector length with the top line being the practical limit. If vector lengths vary, as is usually the case, the total number of each length must be taken into account; the aggregate must not cause the frame time to exceed 32 ms.

4.7 ADVANCED PROGRAMMING TECHNIQUES

4.7.1 Subroutines

This programming method is used when a section of display code is repeated a number of times during the execution of a display file. It precludes the need to store multiple copies of the routine in memory and therefore makes more efficient use of available storage space. Writing effective display subroutines is accomplished through use of the Stop Interrupt instruction (DSTOP) followed by an identifier that informs the interrupt service routine what to do or where to go. Figure 9 shows an example of how a display subroutine can be repeatedly called by the main display file. An example of an interrupt service routine is shown below. It is assumed that register R5 is used for the subroutine stack. STKST is the starting location for the subroutine stack.

	Mnemonic	Comment
STPINT:	TST @ DPC	Test the address DPC is pointing to.
	BEQSTOP0	If it contains a valid non-zero address, go to the next instruction; if not go to STOP0.
	MOV DPC,-(R5)	Push current DPC on stack.
	ADD #2, @R5	The stack now contains the return address from the subroutine.
	MOV @ DPC,DPC	Move address pointed to by DPC into the DPC, i.e., go to the subroutine.
	RTI	Exit

	Mnemonic	Comment
STOP0:	CMP R5, STKST	Is the subroutine stack empty?
	BEQ TOP	Yes, go to top of display file.
	MOV (R5)+,DPC	No, pop off a word and go there, i.e., return to display file.
	RTI	Exit
TOP:	MOV#START,DPC RTI	Restart at top of display file and exit.

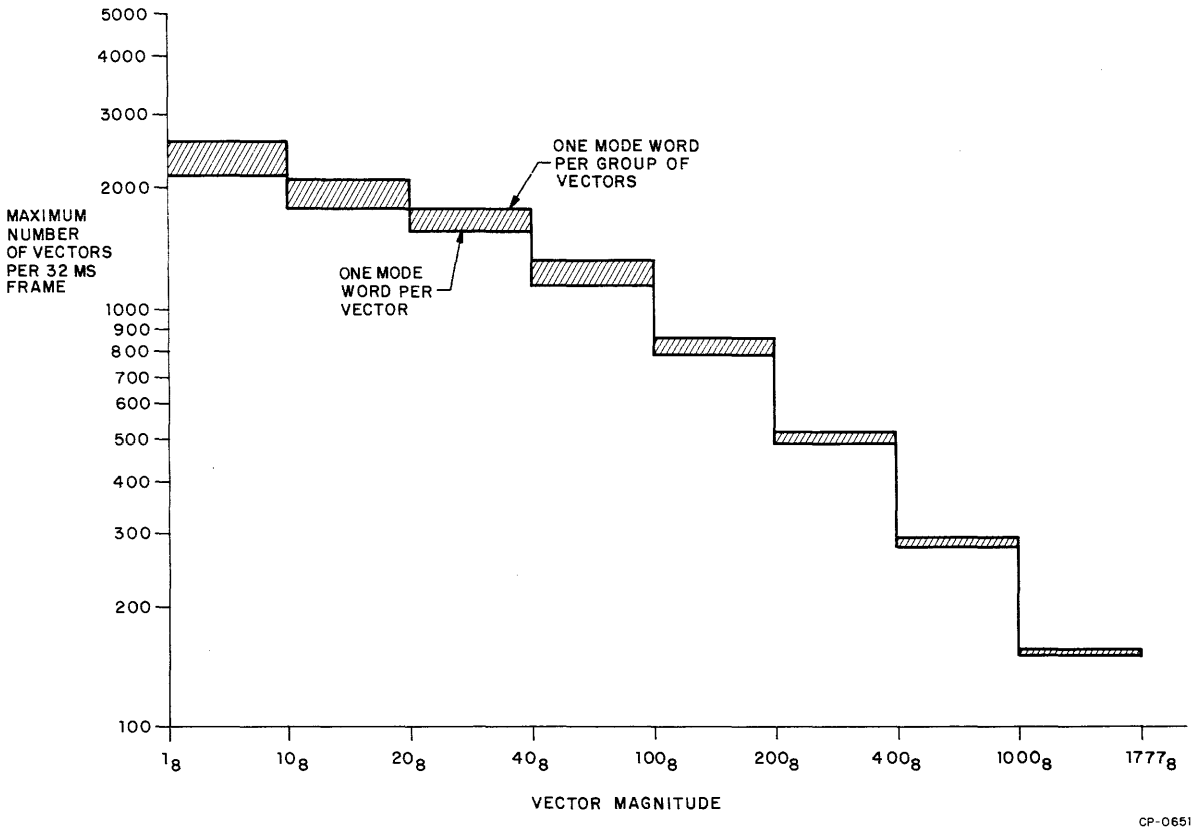


Figure 8 Non-Flicker Display as Determined by Vector Quantity and Magnitude

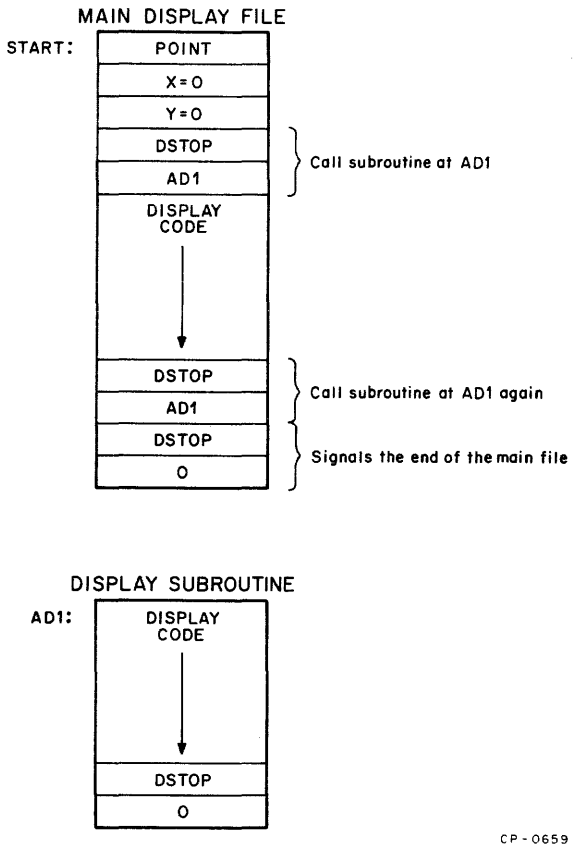


Figure 9 Subroutining Example

4.7.2 Light Pen Interaction

The DPU is stopped when a light pen (LP) "hit" occurs during the display of a vector, character, or point, provided light pen interrupts are permitted (bits 5 and 6 of the Set Graphic Mode word must both be true to enable the light pen interrupt function).

Priorities permitting, the LP hit interrupts the PDP-11. The interrupt service routine that is called in as a result of the LP interrupt has access to three data in the DPU (the data can be read by specifying the addresses indicated):

- Display Program Counter (DPC) Addr = 172000. Points to the instruction/data word following the data word on which the LP hit occurred.
- The X position of the display at the time the DPU stopped, Addr = 172004. A 10-bit absolute number.
- The Y position of the display at the time the DPU stopped, Addr = 172006. A 10-bit absolute number.

The service routine can respond to the LP interrupt by restarting the display in one of two ways:

- Resume the display — the operation in progress at the time of the interrupt is allowed to continue. Program example: MOV #1,DPC.
- Restart the display — the operation in progress at the time of the interrupt is abandoned and a new display program routine is initiated. Program example: MOV #SA,DPC.

4.7.3 Special Characters

The 31 special characters in the VT11 display character set (Appendix A) are addressed through use of ASCII codes Shift Out (016_8) and Shift In (017_8).

When the DPU detects the character code 016_8, the hardware enters the Shift mode. In this mode, codes 000 through 037_8 are decoded as special characters (the appendix contains a list of VT11 character codes). Note that when the DPU is in the Shift mode, the Shift Out code (016_8) itself is a legitimate printing character. The DPU is returned to the non-special character ASCII set (non-shift mode) when Shift In is decoded. Unlike the Shift Out code, the Shift In code (017_8) does not cause a special character to be displayed. If, when in the Shift mode, the DPU detects a code $\leqslant 040_8$, the PDP-11 is interrupted by a Shift In/Time Out interrupt vector. This is because only the special characters (codes 000 through 037_8) are legal when in the Shift mode. The PDP-11 now has access to the 6 low order bits of the 7-bit illegal code. These 6 bits could be used, for example, as an index to a table of software generated characters.

4.7.4 Edge Violations

An edge violation occurs if either the X or Y coordinate indicated for a relative display causes the display to go outside the physical limits of the CRT face. (Vectors, relative points, characters, and graphplots are classified as relative type displays.) In the event of an edge violation, the edge flag in the status word is set and the display is clipped (terminated) at the edge of the screen; wrap-around does not take place. However, there is one exception in which wrap-around can occur. The VT11 hardware is capable of counting only up to 4095_{10}, i.e., 12 bits. Therefore, if the vector position exceeds this 12-bit limit, the count overflows to 0 and wrap-around occurs. For example, if four consecutive vectors with the same coordinates (Δ X = 1023, Δ = 1) are read, only the first vector is displayed; it is the only one that can be displayed within the physical address space. The other three vectors cause the count to legally exceed the 12-bit field. If a fifth vector, with the coordinates of Δ X = 10 and Δ Y = 0, is decoded, the vector will appear on the left of the display; the hardware has caused the display to wrap around. This relative X and Y counting is performed in a 12-bit circular fashion. Absolute points are limited to 10-bit addressing.

4.8 GT44 SOFTWARE

Utilization of the software supplied with the GT44 is covered in the following manuals:

RT-11 System Reference Manual, DEC-11-ORUGA-A-D

BASIC/RT-11 Language Reference Manual, DEC-11-LBACA-A-D.

APPENDIX A
CHARACTER CODES

7 Bit (octal)	ASCII Representation	Keyboard	GT44 Printing	GT44 Printing When Preceded By Shift-Out = 016
000	NUL	CTRL @		λ
001	SOH	CTRL A		α
002	STX	CTRL B		ϕ
003	ETX	CTRL C		Σ
004	EOT	CTRL D		δ
005	ENQ	CTRL E		Δ
006	ACK	CTRL F		∿
007	BEL	CTRL G		∂
010	BS	CTRL H	Backspace	∩
011	HT	CTRL I (TAB)		ψ
012	LF	CTRL J (LF)	Line Feed	÷
013	VT	CTRL K		o
014	FF	CTRL L		∴
015	CR	CTRL M (CR)	Carriage Return	μ
016	SO	CTRL N		£
017	SI	CTRL O		Shift In
020	DLE	CTRL P		π
021	DC1	CTRL Q		‖
022	DC2	CTRL R		Ω
023	DC3	CTRL S		σ
024	DC4	CTRL T		ϒ
025	NAK	CTRL U		ϵ
026	SYN	CTRL V		←
027	ETB	CTRL W		→
030	CAN	CTRL X		↑
031	EM	CTRL Y		↓
032	SUM	CTRL Z		⌜
033	ESC	CTRL [(ALT)		⊥
034	FS	CTRL \		≠
035	GS	CTRL]		≈
036	RS	CTRL~		∨
037	US	CTRL –		□
040	SP	SPACE BAR	Space 1 character	
041	!	SHIFT 1	!	
042	"	SHIFT 2	"	
043	#	SHIFT 3	#	

7 Bit (octal)	ASCII Representation	Keyboard	GT44 Printing	GT44 Printing When Preceded By Shift-Out = 016
044	$	SHIFT 4	$	
045	%	SHIFT 5	%	
046	&	SHIFT 6	&	
047	'	SHIFT 7	'	
050	(	SHIFT 8	(	
051	)	SHIFT 9	)	
052	*	SHIFT :	*	
053	+	SHIFT ;	+	
054	,	,	,	
055	- (minus)	-	-	
056	.	.	.	
057	/	/	/	
060	0	0	0	
061	1	1	1	
062	2	2	2	
063	3	3	3	
064	4	4	4	
065	5	5	5	
066	6	6	6	
067	7	7	7	
070	8	8	8	
071	9	9	9	
072	:	:	:	
073	;	;	;	
074	<	SHIFT ,	<	
075	=	SHIFT -	=	
076	>	SHIFT .	>	
077	?	SHIFT /	?	
100	@	@	@	
101	A	SHIFT A	A	
102	B	SHIFT B	B	
103	C	SHIFT C	C	
104	D	SHIFT D	D	
105	E	SHIFT E	E	
106	F	SHIFT F	F	
107	G	SHIFT G	G	
110	H	SHIFT H	H	
111	I	SHIFT I	I	
112	J	SHIFT J	J	
113	K	SHIFT K	K	
114	L	SHIFT L	L	
115	M	SHIFT M	M	
116	N	SHIFT N	N	
117	O	SHIFT O	O	
120	P	SHIFT P	P	
121	Q	SHIFT Q	Q	
122	R	SHIFT R	R	
123	S	SHIFT S	S	
124	T	SHIFT T	T	

7 Bit (octal)	ASCII Representation	Keyboard	GT44 Printing	GT44 Printing When Preceded By Shift-Out = 016
125	U	SHIFT U	U	
126	V	SHIFT V	V	
127	W	SHIFT W	W	
130	X	SHIFT X	X	
131	Y	SHIFT Y	Y	
132	Z	SHIFT Z	Z	
133	[	[	[	
134	\	\	\	
135	]	]	]	
136	^	^	^	
137	-	-	-	
140	`	SHIFT @	`	
141	a	A	a	
142	b	B	b	
143	c	C	c	
144	d	D	d	
145	e	E	e	
146	f	F	f	
147	g	G	g	
150	h	H	h	
151	i	I	i	
152	j	J	j	
153	k	K	k	
154	l	L	l	
155	m	M	m	
156	n	N	n	
157	o	O	o	
160	p	P	p	
161	q	Q	q	
162	r	R	r	
163	s	S	s	
164	t	T	t	
165	u	U	u	
166	v	V	v	
167	w	W	w	
170	x	X	x	
171	y	Y	y	
172	z	Z	z	
173		SHIFT [	{	
174		SHIFT \	¦	
175		SHIFT]	}	
176	~	SHIFT ^	~	
177	RUB OUT	R.O.	■	

APPENDIX B
BM792-YB BULK STORAGE
BOOTSTRAP LOADER PROGRAM LISTING

```
                ; REGISTER ASSIGNMENTS:
        000000  R0=%0
        000001  R1=%1
                ;
173100  013701          MOV     @#177570,R1     ;READ SWITCH REG FOR ....
        177570
173104  000005  BEGIN:  RESET                   ;FORCE CLEAR IF RETRY
173106  010100          MOV     R1,R0           ;....DEVICE WC ADDRESS
173110  012710          MOV     #-256.,@R0      ;SET TO READ 256 WORDS
        177400
173114  020027          CMP     R0,#177344      ;IS IT DECTAPE?
        177344
173120  001007          BNE     START           ;NO. GO TO START
173122  012740          MOV     #4002,-(R0)     ;YES. MOVE TAPE TO FRONT
        004002
173126  005710          TST     @R0             ;WAIT FOR ERROR!
173130  100376          BPL     .-2
173132  005740          TST     -(R0)           ;IS IT ENDZONE?
173134  100363          BPL     BEGIN           ;NO. TRY AGAIN
173136  022020          CMP     (R0)+,(R0)+     ;ADJUST POINTER
173140  012740  START:  MOV     #5,-(R0)        ;NOW START ACTUAL READ
        000005
173144  105710          TSTB    @R0             ;WAIT FOR DONE
173146  100376          BPL     .-2
173150  005710          TST     @R0             ;ERROR ENCOUNTERED?
173152  100754          BMI     BEGIN           ;IF SO START OVER
173154  105010          CLRB    @R0             ;FOR DECTAPE,STOP TRANSPORT
173156  000137          JMP     @#0             ;GO TO ROUTINE LOADED
        000000
        000001          .END


BEGIN       000004R         R0      =%000000        R1      =%000001
START       000040R         .       = 000062R
```

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