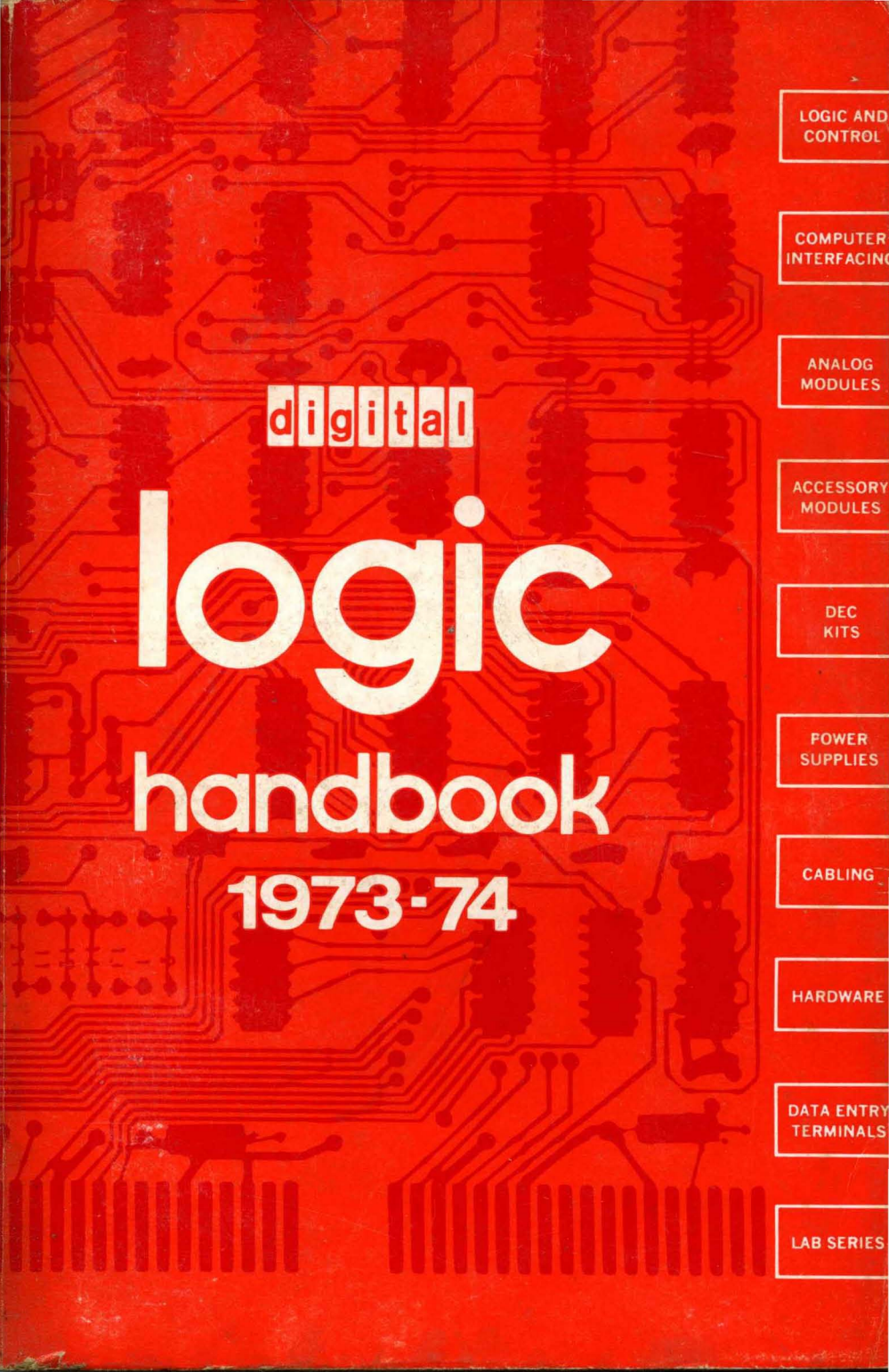
digital
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handbook
1973-74
LOGIC AND CONTROL
COMPUTER INTERFACING
ANALOG MODULES
ACCESSORY MODULES
DEC KITS
POWER SUPPLIES
CABLING
HARDWARE
DATA ENTRY TERMINALS
LAB SERIES

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logic handbook 1973-74

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Prices quoted are in U.S. dollars and apply to the United States only. The availability of products listed and the prices quoted herein are subject to change without notice.

contents

product index

TYPE	PAGE	PRICE	SIZE LHW #	POWER V	POWER mA	TITLE
714	378	200.00		+5	7000	Power Supply
728	381	240.00		+10	7500	Power Supply
				−15	8500	
728A	381	260.00		+10	7500	Power Supply
				−15	8500	
782	374	128.00		+10	400	Power Supply
				−15	3000	
782-A	374	148.00		+10	400	Power Supply
				−15	3000	
783	383	240.00		+10	7500	Power Supply
				−15	8500	
783A	383	260.00		+10	7500	Power Supply
				−15	8500	
911	497	9.00				Patchcords (10/pkg.)
913	481	25.00				Patchcords (100/pkg.)
914-7	500	4.00				Power Jumpers (10/pkg).
914-19	500	4.00				Power Jumpers (10/pkg.)
915	481	33.00				Patchcords (100/pkg.)
917	483	50.00				Daisy Chain
932	477	.60				Bus Strip
933	477	1.00				Bus Strip
934	477	50.00				Wire Wrapping Wire (1000 ft. roll)
935	478	60.00				Wire Wrapping Wire (1000 ft. roll)
937	476	7.00/pkg.				25 Gray handles per package
939	478	1.50				Bus Strip
1907	439	9.00				Panel Cover
1945-19	439	20.00				Hold Down Bar
4913	500	25.00				Mounting Racks
12-01954	462	25.00				Mounting Slides
12-09703	462	52.00				Tilt Slides
17-00001	394	1.00/ft.				Cable, Flat Coax 9-conductor
17-00002	394	0.75/ft.				Cable, 1.25" Mylar Flat Mylar 10-cond.
17-00003	394	1.50				Cable, Round Coax 9-conductor
70-05909	462	50.00				AC Distribution Panel
74-06782	462	6.00				Kickplate
74-06793	462	8.00				Kickplate

Number of socket slots required.

TYPE	PAGE	PRICE	SIZE LHW	#	POWER V	mA	TITLE
91-07575	394	0.60/ft.					Cable, Ribbon 20-cond.
91-07599	394	2.00/ft.					Cable, Twisted pair Coax 36-conductor
91-07722	394	2.00/ft.					Cable, Flat 40-conductor
A123	278	58.00	SSS	1	+5	45	Four-Channel Multiplexer
					+10	18	
					−20	50	
A160	280	150.00	SDD	4	+15	25	High-Impedance Multiplexer Expander
					−15	25	
A161	282	200.00	SDD	4	+15	35	High-Impedance Multiplexer with Output Buffer
					−15	35	
A162	285	160.00	SDD	4	+5	30	High-Impedance Multiplexer with Decoder
					+15	35	
					−15	35	
A163	288	210.00	SDD	4	+5	30	High-Impedance Multiplexer with Decoder & Buffer
					+15	35	
					−15	35	
A164	291	175.00	SDD	4	+15	40	Constant Impedance Multiplexer Expander
					−15	40	
A165	293	225.00	SDD	4	+15	40	Constant Impedance Multiplexer with Output Amplifier
					−15	40	
A166	295	185.00	SDD	4	+5	30	Constant Impedance Multiplexer Expander with Decoder
					+15	40	
					−15	40	
A167	297	240.00	SDD	4	+5	30	Constant Impedance Multiplexer with Decoder & Output Amplifier
					+15	40	
					−15	40	
A207	300	45.00	SSS	1	+15	6	Operational Amplifier
					−15	10	
A260	302	150.00	SDD	4	+15	20	Dual Amplifier Card
					−15	20	
A404	306	130.00	SDS	2	+15	22	Single Sample & Hold for 10-bit Systems
					−15	35	
A460	308	200.00	SDD	4	+15	12	Single Sample & Hold for 12-bit Systems
					−15	12	
A461	308	250.00	SDD	4	+15	20	Single Sample & Hold with Input Buffer for 12-bit Systems
					−15	20	
A613	310	200.00	SDS	2	+5	60	12-Bit BCD or Binary DAC
					+15	35	
					−10	7	
					−15	60	

Number of socket slots required.

TYPE	PAGE	PRICE	SIZE LHW #	POWER V	mA	TITLE
A618	312	125.00	SDD 4	+5	135	10-Bit D/A Converter,
				+10.06	60	Single Buffered
				+15	25	
				−15	85	
A619	312	325.00	SDD 4	+5	135	10-Bit D/A Converter,
				+10.06	60	Single Buffered
				+15	25	
				−15	85	
A620	314	125.00	SDD 4	+5	190	10-Bit D/A Converter,
				+10.06	60	Double Buffered
				+15	25	
				−15	85	
A621	314	125.00	SDD 4	+5	190	10-Bit D/A Converter,
				+10.06	60	Double Buffered
				+15	25	
				−15	85	
A623	316	350.00	SSS 1	+5	315	12-Bit D/A Converter,
				+15	25	Double Buffered
				−15	25	
A660	318	300.00	SDD 4	+5	45	12-Bit Multiplying D/A
				+15	25	Converter, Straight
				−15	25	Binary
A661	320	300.00	SDD 4	+5	45	12-Bit Multiplying D/A
				+15	25	Converter, BCD
				−15	25	
A662	322	300.00	SDD 4	+5	45	12-Bit Multiplying D/A
				+15	25	Converter, 2's Com-
				−15	25	plement
A663	324	350.00	SDD 4	+5	125	12-Bit Multiplying D/A
				+15	25	Converter, Buffered
				−15	25	Straight Binary
A704	326	184.00	SDS 2	−15	250	Reference Supply
A811	328	350.00	SDD 4	+5	300	10-Bit A/D Converter
				+15	20	
				−15	160	
A860	330	200.00	SDD 4	+5	150	12-Bit Industrial A/D
				+15	20	Converter
				−15	20	
A861	333	300.00	SDD 4	+5	420	High-Speed 12-Bit Uni-
				+15	55	polar A/D Converter
				−15	12	
A862	335	300.00	SDD 4	+5	420	High-Speed 12-Bit Bi-
				+15	55	polar A/D Converter
				−15	12	
A990	337	4.00	SSD 2			Amplifier Board
A992	337	4.00	SSD 2			Amplifier Board
BB11	471	90.00				System Unit for General Interfacing

Number of socket slots required.

TYPE	PAGE	PRICE	SIZE LHW #	POWER V	mA	TITLE
BC02F-XX	395	33.00				91-07575 Cable (W018-W023)
BC02L-XX	395	30.00				91-07575 Cable (W021-W021)
BC02M-XX	395	30.00				91-07575 Cable (W021-W022)
BC02P-XX	395	30.00				91-07575 Cable (W022-W022)
BC02S-XX	395	30.00				91-07575 Cable (W023-W023)
BC02W-XX	395	30.00				91-07575 Cable (W028-W028)
BC02X-XX	399	58.00				91-07575 Cable (M908-M908)
BC02Y-XX	395	31.00				91-07575 Cable (W011-W021)
BC03A-XX	396	38.00				17-00001 Cable (W011-W011)
BC03B-XX	396	37.00				17-00001 Cable (W011-W021)
BC03C-XX	396	36.00				17-00001 Cable (W021-W021)
BC03D-XX	396	36.00				17-00001 Cable (W021-W022)
BC03E-XX	397	29.00				17-00002 Cable (W031-W031)
BC03F-XX	397	28.00				17-00002 Cable (W033-W033)
BC03J-XX	396	36.00				17-00001 Cable (W028-W028)
BC03H-XX	398	54.00				17-00002 Cable (M901-M901)
BC04A-XX	395	15.00				91-07575 Cable (W011-OPEN)
BC04B-XX	395	18.00				91-07575 Cable (W018-OPEN)
BC04F-XX	395	15.00				91-07575 Cable (W023-OPEN)
BC04L-XX	396	18.00				17-00001 Cable (W011-OPEN)
BC04M-XX	396	18.00				17-00001 Cable (W021-OPEN)
BC04N-XX	396	18.00				17-00001 Cable (W022-OPEN)
BC04P-XX	400	36.00				17-00001 Cable (M904-OPEN)
BC04T-XX	398	27.00				17-00002 Cable (M901-OPEN)

Number of socket slots required.

TYPE	PAGE	PRICE	SIZE LHW #	POWER V	mA	TITLE
BC04U-XX	398	22.00				17-00002 Cable (M903-OPEN)
BC04W-XX	399	28.00				91-07575 Cable (M908-OPEN)
BC04Z	403	See Listing				91-07722 Cable (H856-OPEN)
BC08A	398	See Listing				17-00002 Cable (M903-M903)
BC08B	400	See Listing				17-00001 Cable (M904-M904)
BC08C	398	See Listing				17-00002 Cable (M903-Two W031)
BC08D	400	See Listing				17-00001 Cable (M904-Two W011)
BC08J	401	See Listing				91-07722 Cable (H856-M953)
BC08K	401	See Listing				91-07722 Cable (H856-M955)
BC08L	402	See Listing				91-07722 Cable (Two H856-M954)
BC08R	403	See Listing				91-07722 Cable (H856-H856)
BC11A	404	See Listing				91-56-92-6 Cable (M919-M929)
Cab A	445	411.00				Cabinet
Cab B	456	431.00				Cabinet
Cab C	456	437.00				Cabinet
Cab D	456	390.00				Cabinet
Cab E	457	410.00				Cabinet
Cab F	457	340.00				Cabinet
Cab I	458	476.00				Cabinet
Cab J	458	419.00				Cabinet
Cab K	459	365.00				Cabinet
DECkits	359	See Kits				
H001	439	7.00				0.75″ Mounting Brackets (pr)
H002	439	15.00				2.00″ Mounting Brackets (pr)
H014	447	20.00				Mounting Panel
H019	454	70.00				Mounting Bar
H020	439	15.00				19″ Mounting Frame Casting
H021	439	7.00				End Plate
H022	439	20.00				End Plate
H024	439	7.00				End Plate 8.5 inches
H025	439	20.00				End Plate 8.5 inches with Terminal Block
H500	492	375.00				Computer Lab (120 Vac)

Number of socket slots required.

TYPE	PAGE	PRICE	SIZE LHW #	POWER V	mA	TITLE
H500A	492	375.00				Computer Lab (240 Vac)
H510	495	995.00				K Series Logic Lab
H520	503	995.00				M Series Logic Lab
H701	374	116.00		+10	400	Power Supply
				−15	3000	
H701-A	374	136.00		+10	400	Power Supply
				−15	3000	
H704	375	200.00		+15	400	Power Supply
				−15	400	
H707	375	400.00		+15	1500	Power Supply
				−15	1500	
H710	377	180.00		+5	5000	Power Supply
H716	379	150.00		+5	4000	Power Supply
				−15	1500	
H726	380	200.00		+5	7000	Power Supply
H800-F	433	8.00				Connector Block
H800-W	433	8.00				Connector Block
H801-F	433	2.00				Replacement Pins
H801-W	433	2.00				Replacement Pins
H802	434	4.00				Connector Block
H803	435	13.00				Connector Block
H805	435	4.00				Connector Block
H807	436	5.00				Connector Block
H808	437	10.00				Connector Block
H809	437	4.00				Replacement Pins
H810	479	99.00				Hand Wire Wrapping Tool (24 ga.)
H810-A	479	99.00				Hand Wire Wrapping Tool (30 ga.)
H810-B	479	150.00				Hand Wire Wrapping Tool (24 & 30 ga.)
H810-C	480	150.00				Battery Operated Wire Wrapgun (24-gauge sleeve & bit)
H810-D	480	150.00				Battery Operated Wire Wrapgun (30-gauge sleeve & bit)
H810-E	480	100.00				Battery Operated Wire Wrapgun
H811	479	24.00				Hand Wrapping Tool
H811-A	479	24.00				Hand Wrapping Tool
H812	479	10.00				Hand Unwrapping Tool (24-gauge)
H812-A	479	10.00				Hand Unwrapping Tool (30-gauge)
H813	479	30.00				Bit (24-gauge)
H813-A	479	30.00				Bit (30-gauge)
H814	479	21.00				Sleeve (24-gauge)

Number of socket slots required.

TYPE	PAGE	PRICE	SIZE LHW #	POWER V	POWER mA	TITLE
H814-A	479	21.00				Sleeve (30-gauge)
H820	483	48.00				Grip Clips (1000/pkg.)
H821	483	98.00				Grip Clips (1000/pkg.)
H825	482	146.00				Hand Crimping Tool
H826	482	210.00				Hand Crimping Tool
H850	475	10.00				Module Handle Extender
H851	438	15.00				Connector (edge)
H852	475	7.00				Module Holder (rib type, 25/pkg.)
H853	475	7.00				Module Holder (non rib type, 25/pkg.)
H854	426	12.00				I/O Connector (40-pin male) Board Mount
H856	423	8.00				I/O Connector (40-pin female) Cable Mount
H911-J, R	445	151.00				Mounting Panel
H911-K, S	445	161.00				Mounting Panel
H913	446	270.00				Mounting Panel
H914	446	125.00				Mounting Panel
H916	446	270.00				Mounting Panel
H917	446	260.00				Mounting Panel
H920	450	170.00				Module Drawer
H921	450	15.00				Front Panel
H923	450	75.00				Chassis Slides
H925	451	250.00				Module Drawer
H933	449	15.00				System Unit Mounting Panel
H933-A	449	37.00				H933 with 3-H800
H933-B	449	37.00				H933 with 3-H800
H933-C	449	54.00				H933 with 3-H803
H933-D	449	42.00				H933 with 3-H808
H941-AA	453	125.00				19″ Mounting Panel Frame
H941-BA	453	70.00				Cover (5.5″)
H941-BB	453	80.00				Cover (8.5″)
H950-AA	461	163.00				Frame
H950-BA	461	47.00				Full Door
H950-CA	461	47.00				Full Door
H950-DA	461	47.00				Mounting Panel Door
H950-EA	461	47.00				Mounting Panel Door
H950-FA	461	20.00				Mounting Panel Door Skin
H950-G	462	60.00				Table Top Assembly
H950-HA	461	48.00				Short Door (21″ mounting)
H950-HB	462	48.00				Short Door (22.75″ mountings)
H950-HC	462	48.00				Short Door (26.25″ mountings)

Number of socket slots required.

TYPE	PAGE	PRICE	SIZE LHW #	POWER V	mA	TITLE
H950-HD	462	48.00				Short Door (31.5″ mountings)
H950-HE	462	48.00				Short Door (36.75″ mountings)
H950-HF	462	48.00				Short Door (42″ mountings)
H950-HG	462	48.00				Short Door
H950-HH	462	48.00				Short Door
H950-HJ	462	48.00				Short Door
H950-HK	462	48.00				Short Door
H950-LA	462	9.00				Frame Panel
H950-LB	462	7.00				Frame Panel
H950-PA	462	8.00				Cover Bezel Panel (5.25″)
H950-QA	462	11.00				Cover Bezel Panel (10.5″)
H950-SA	462	4.00				Filter
H952-AA	462	57.00				End Panel
H952-BA	462	23.00				Stabilizer Feet (pair)
H952-CA	462	40.00				Fan Assembly
H952-EA	462	7.00				Caster Set
H952-FA	462	2.00				Leveler Set
H952-GA	462	44.00				Filler Strip
H957-AA	466	142.00				Frame
H957-BA	466	60.00				Full Door Rear Mount (RH)
H957-CA	466	60.00				Full Door Mount (LH)
H957-DA	466	36.00				Mounting Panel (Plenum) Door, rear mount (RH)
H957-EA	446	36.00				Mounting Panel (Plenum) Door, rear mount (LH)
H957-FA	466	63.00				End Panel, right hang
H957-FB	466	63.00				End Panel, left hang
H957-GA	466	36.00				Filler Strip Group (3)
H957-HA	466	50.00				Fan Assembly (500 CFM)
H957-JA	466	9.00				Bottom Cover Plate
H957-LA	466	20.00				Logo Frame Panel
H957-SA	466	4.00				Filter
H9190	454	250.00				Mounting Panel
See Control Handbook for K Series Modules						
K731	385	30.00	SST 3	+5	1000	Source Module
K732	387	27.00	SSQ 4	+5	2000	Slave Regulator
K741	390	30.00		12.6	1000	Power Transformer
K743	390	45.00		12.6	6000	Power Transformer
K771	389	35.00				Display Supply

Number of socket slots required.

TYPE	PAGE	PRICE	SIZE LHW	#	POWER V	mA	TITLE
K900	496	185.00					Control Panel—Power Supply
K901	497	125.00					Patch Board Panel
K902	498	145.00					Indicator Switch Panel
K903	499	155.00					Patch Panel Board
K940	441	6.00					Mounting Support
K941	441	6.00					Mounting Frame
K943-R	444	96.00					Mounting Panel
K943-S	444	96.00					Mounting Panel
Kit-H	362	See Listing					DEC KIT, I/O, 4 Words IN/4 Words OUT
Kit-F	364	See Listing					DEC KIT, I/O, 3 Words IN/4 Words OUT
Kit-K	365	See Listing					DEC KIT, I/O, 8 Words IN
M002	21	10.00	SSS	1	+5	16	Logic HIGH Source
M040	22	39.00	SSS	1	+5	47	Solenoid Driver
					−15	9	
M050	24	31.00	SSS	1	+5	47	50 mA Indicator Driver
					−15	16	
M051	155	31.00	SSS	1	+5	47	Positive to Negative
					−15	16	Logic Level Converter
M060	25	55.00	SSS	1	+5	80	Solenoid Driver
M100	156	50.00	SSS	1	+5	60	Bus Data Interface
					−15	10	
M101	158	24.00	SSS	1	+5	82	Bus Data Interface
M102	160	60.00	SSS	1	+5	130	Device Selector
					−15	40	
M103	162	45.00	SSS	1	+5	110	Device Selector
M105	164	65.00	ESS	1	+5	338	Address Selector
M107	166	105.00	SDS	2	+5	245	Device Selector
M108	168	45.00	SSS	1	+5	137	Flag Module
M111	27	22.00	SSS	1	+5	87	Inverter
M112	28	35.00	SSS	1	+5	50	NOR Gate
M113	30	18.00	SSS	1	+5	71	NAND Gates
M115	30	18.00	SSS	1	+5	41	NAND Gates
M116	29	20.00	SSS	1	+5	30	Six 4-Input NOR Gates
M117	30	19.00	SSS	1	+5	41	NAND Gates
M119	30	18.00	SSS	1	+5	19	NAND Gates
M121	33	23.00	SSS	1	+5	50	AND/NOR Gate
M133	34	27.00	SSS	1	+5	160	Two-Input NAND Gates
M135	35	32.00	SSS	1	+5	100	Eight 3-Input NAND Gates
M139	36	28.00	SSS	1	+5	50	Three 8-Input NAND Gates
M141	37	29.00	SSS	1	+5	117	NAND/OR Gates
M152	39	36.00	SSS	1	+5	265	Dual 1 of 8 Decoder
M155	41	30.00	SSS	1	+5	55	4-Line to 16-Line Decoder

Number of socket slots required.

TYPE	PAGE	PRICE	SIZE LHW	#	POWER V	mA	TITLE
M159	43	35.00	SSS	1	+5	150	Arithmetic/Logic Unit
M160	47	33.00	SSS	1	+5	30	AND/NOR Gate
M161	48	55.00	SSS	1	+5	120	Binary to Octal/Decimal Decoder
M162	50	63.00	SSS	1	+5	102	Parity Circuit
M165	51	30.00	SSS	1	+5	130	8 Buffers
M168	52	45.00	SSS	1	+5	250	12-Bit Magnitude Comparator
M169	54	33.00	SSS	1	+5	50	Gating Module
M191	55	22.00	SSS	1	+5	130	ALU Look-Ahead Logic
M202	58	29.00	SSS	1	+5	57	Triple J-K Flip-Flop
M203	59	26.00	SSS	1	+5	55	8 R/S Flip-Flops
M204	60	34.00	SSS	1	+5	74	General-Purpose Buffer & Counter
M205	61	33.00	SSS	1	+5	90	General-Purpose Flip-Flops
M206	62	30.00	SSS	1	+5	87	General-Purpose Flip-Flops
M207	64	33.00	SSS	1	+5	96	General-Purpose Flip-Flops
M208	66	84.00	SSS	1	+5	184	8-Bit Buffer/Shift Register
M230	68	105.00	SDS	2	+5	860	Binary to BCD & BCD to Binary Converter
M232	70	125.00	SSS	1	+5	200	16-Word RAM
M236	72	50.00	SSS	1	+5	330	12-Bit Binary Up/Down Counter
M237	74	50.00	SSS	1	+5	330	3-Digit BCD Up/Down Counter
M238	76	35.00	SSS	1	+5	180	Dual 4-Bit Binary Synchronous Up/Down Counter
M245	78	28.00	SSS	1	+5	130	Dual 4-Bit Shift Register
M246	80	21.00	SSS	1	+5	160	5 D-Type Flip-Flops
M248	82	15.00	SSS	1	+5	130	Dual 4-Bit Multipurpose Shift Register
M253	84	73.00	SSS	1	+5	390	16-Word X 12-Bit RAM
M260	88	221.00	SDS	2	+5	375	4-Word X 12-Bit Associative Memory
M261	91	40.00	SSS	1	+5	175	4-State Motor Translator
M262	93	65.00	SDS	2	+5	350	10-State Motor Translator
M302	95	46.00	SSS	1	+5	166	Dual Delay Multivibrator
M306	97	27.00	SSS	1	+5	120	Integrating One Shot
M310	99	58.00	SSS	1	+5	89	Delay Line
M360	100	68.00	SSS	1	+5	50	Variable Delay
M401	101	55.00	SSS	1	+5	80	Variable Clock
M403	103	30.00	SSS	1	+5	70	RC Multivibrator Clock
M404	105	65.00	SSS	1	+5	535	Crystal Clock
M405	106	100.00	SSS	1	+5	50	Crystal Clock

Number of socket slots required.

TYPE	PAGE	PRICE	SIZE LHW #	POWER V	POWER mA	TITLE
M410	107	70.00	SSS 1	+5	95	Reed Clock
M452	108	40.00	SSS 1	+5	77	Variable Clock
M500	170	55.00	SSS 1	+5	160	Negative Input/Positive
				−15	64	Output Receiver
M501	109	25.00	SSS 1	+5	31	Schmitt Trigger
M502	172	26.00	SSS 1	+5	49	Negative Input Conver-
				−15	92	ter, High-Speed
M506	173	52.00	SSS 1	+5	81	Negative Input Conver-
				−15	115	ter, Medium-Speed
M507	175	45.00	SSS 1	+5	42	Bus Converter, Medium-
				−15	115	Speed
M510	177	51.00	SSS 1	+5	170	I/O Bus Receiver
M521	111	16.00	SSS 1	+5	56	K to M Converter
M602	112	28.00	SSS 1	+5	213	Pulse Amplifier
M606	113	43.00	SSS 1	+5	188	Pulse Generator
M610	115	20.00	SSS 1	+5	41	Open Collector 2-Input NAND Gate
M617	117	26.00	SSS 1	+5	97	4-Input Power NAND Gate
M622	178	45.00	SSS 1	+5	210	8-Bit Positive Input/ Output Bus Driver
M623	180	40.00	SSS 1	+5	71	Bus Driver
M624	181	45.00	SSS 1	+5	89	Bus Driver
M627	118	29.00	SSS 1	+5	136	NAND Power Amplifier
M632	183	55.00	SSS 1	+5	175	Positive Input Negative
				−15	40	Output Bus Driver
M633	185	50.00	SSS 1	+5	100	Negative Bus Driver
				−15	40	
M650	187	25.00	SSS 1	+5	37	Negative Output Con-
				−15	29	verter
M652	188	26.00	SSS 1	+5	122	Negative Output Con-
				−15	202	verter
M660	119	25.00	SSS 1	+5	71	Positive Level Cable Driver
M661	120	15.00	SSS 1	+5	111	Positive Level Driver
M671	121	52.00	SSS 1	+5	112	M to K Converter
M706	123	150.00	SDS 2	+5	400	Teletype Receiver
M707	128	150.00	SDS 2	+5	375	Teletype Transmitter
M730	190	160.00	SDS 2	+5	400	Bus Interface
M731	190	160.00	SDS 2	+5	400	Bus Interface
				−15	90	
M732	194	160.00	SDS 2	+5	400	Bus Interface
M733	194	165.00	SDS 2	+5	400	Bus Interface
				−15	125	
M734	198	105.00	SDS 2	+5	325	I/O Bus Input Multi- plexer
M735	200	135.00	SDS 2	+5	425	I/O Bus Transfer Register
M736	203	125.00	SDS 2	+5	400	Priority Interrupt Module

Number of socket slots required.

TYPE	PAGE	PRICE	SIZE LHW	#	POWER V	mA	TITLE
M737	207	120.00	SDS	2	+5	300	12-Bit Bus Receiver Interface
M738	209	105.00	SDS	2	+5	250	Counter Buffer Interface
M783	211	30.00	ESS	1	+5	70	UNIBUS Drivers
M784	212	30.00	ESS	1	+5	200	UNIBUS Receivers
M785	213	35.00	ESS	1	+5	118	UNIBUS Transceiver
M786	214	220.00	EDS	2	+5	600	Device Interface
M795	218	200.00	EDS	2	+5	600	Word Count and BUS Address Module
M796	221	100.00	ESS	1	+5	180	UNIBUS Master Control Module
M798	224	40.00	ESS	1	+5	320	UNIBUS Drivers
M901	406	15.00	SSS	1			Flat Mylar Cable Connector
M903	406	10.00	SSS	1			Flat Mylar Cable
M904	412	10.00	SSS	1			Coaxial Cable Connector
M906	132	20.00	SSS	1	+5	440	Cable Terminator
M907	226	16.00	SSS	1	+5	10	Diode Clamp
M908	416	10.00	SSS	1			Ribbon Connector
M909	227	14.00	SSS	1			Terminator
M910	228	20.00	SSS	1	+5	1350	Terminator
M912	413	25.00	SDS	2			Coax Cable Connector
M915	406	30.00	SSS	1			Ribbon Cable Connector
M917	416	10.00	SSS	1			Ribbon Cable Connector
M918	406	10.00	SSS	1			Flat Mylar Cable Connector
M920	356	45.00	SDT	1			UNIBUS Connector Module
M922	406	6.00	SSS	1			Flat Mylar Cable Connector
M925	406	9.00	SSS	1			Flat Mylar Cable Connector
M926	406	27.00	SSS	1			Flat Mylar Cable Connector
M927	412	6.00	SSS	1			Coax Cable Connector
M935	356	45.00	SSS	1			Internal Bus Connector
M953	423	25.00	SSS	1			Flat Cable Connector
M954	423	27.00	SSS	1			Flat Cable Connector
M955	423	27.00	SSS	1			Flat Cable Connector
M957	416	21.00	ESS	1			Ribbon Cable Connector
M975	428	35.00	SDS	2			Flip Chip to H854 Adapter
M1103	133	14.00	SSS	1	+5	80	2-Input AND Gates
M1307	134	12.00	SSS	1	+5	100	4-Input AND Gates
M1500	229	35.00	ESS	1	+5	300	Bidirectional Bus Interfacing Gates
M1501	232	50.00	ESS	1	+5	300	Bus Input Interface
M1502	234	100.00	EDS	2	+5	750	Bus Output Interface
M1510	237	100.00	EDS	2	+5	600	Bus Device Selector

Number of socket slots required.

TYPE	PAGE	PRICE	SIZE LWH	#	POWER V	mA	TITLE
M1621	240	125.00	EQS	4	+5	777	DVM Data Input Interface
M1623	243	150.00	EQS	4	+5	1600	Instrument Remote Control Interface
M1701	135	17.00	SSS	1	+5	110	Data Selector
M1703	247	75.00	EQS	4	+5	555	OMNIBUS Input Interface
M1709	250	125.00	EQD	8	+5	830	OMNIBUS Interface Foundation Module
M1713	137	13.00	SSS	1	+5	70	16-Line to 1-Line Data Selector
M1801	254	350.00	EQS	4	+5	1450	16-Bit Relay Output Interface
M73XX	263		See RTM Listing				
M7390	139	275.00	EDS	2	+5 +10 −15	700 3 80	Asynchronous Transceiver
M7820	258	100.00	ESS	1	+5	550	Interrupt Control, UNIBUS
M7821	260	100.00	ESS	1	+5	725	Interrupt Control, UNIBUS
M9100	143	30.00	ESS	1			H854 to H854 to Flip Chip Adapter
Power Supplies	369						
RT01	486		See Listing				Numeric Data Entry Terminal
RT02	486		See Listing				Alphanumeric Data Entry Terminal
W011	416	6.00	SSS	1			Ribbon Cable Connector
W018	416	9.00	SSS	1			Ribbon Cable Connector
W020	416	8.00	SSS	1			Ribbon Cable Connector
W021	416	6.00	SSS	1			Ribbon Cable Connector
W022	416	6.00	SSS	1			Ribbon Cable Connector
W023	416	6.00	SSS	1			Ribbon Cable Connector
W024	412	6.00	SSS	1			Ribbon Cable Connector
W027	416	7.00	SSS	1			Ribbon Cable Connector
W028	412	6.00	SSS	1			Coax Cable Connector
W031	406	5.00	SSS	1			Flat Mylar Cable Connector
W033	406	5.00	SSS	1			Flat Mylar Cable Connector
W940	341	70.00	EQD	8			Wire Wrappable Module
W941	341	40.00	EDD	4			Wire Wrappable Module
W942	341	140.00	EQD	8			Wire Wrappable Module with Sockets
W943	341	75.00	EDD	4			Wire Wrappable Module with Sockets
W950	341	65.00	EQD	8			Wire Wrappable Module
W951	341	40.00	EDD	4			Wire Wrappable Module

Number of socket slots required.

TYPE	PAGE	PRICE	SIZE LWH	#	POWER V	mA	TITLE
W952	341	140.00	EQD	8			Wire Wrappable Module with Sockets
W953	341	75.00	EDD	4			Wire Wrappable Module with Sockets
W960	344	8.00	SSS	1			MSI Mounting Board
W964	345	10.00	SSS	1			Collage Universal Terminator
W966	346	85.00	EQD	8			OMNIBUS Wire Wrap Module
W967	346	165.00	EQD	8			OMNIBUS Wire Wrap Module with Sockets
W968	347	45.00	EQS	4			Collage Mounting Board
W969	347	30.00	EDS	2			Collage Mounting Board
W970	348	4.00	SSS	1			Blank Module
W971	348	8.00	SDS	2			Blank Module
W972	348	4.00	SSS	1			Blank Module
W973	348	6.00	SDS	2			Blank Module
W974	348	9.00	SSS	1			Blank Module
W975	348	18.00	SDS	2			Blank Module
W979	351	20.00	SDS	2			Collage Mounting Board
W980	352	14.00	SSS	1			Module Extender
W982	353	18.00	ESS	1			Module Extender
W984	354	30.00	EDS	2			Module Extender
W987	355	40.00	EQS	4			Quad Module Extender
W990	349	2.00	SSS	1			Blank Module
W991	349	5.00	SDS	2			Blank Module
W992	349	2.00	SSS	1			Blank Module
W993	349	4.00	SDS	2			Blank Module
W998	349	4.00	SSS	1			Blank Module
W999	349	9.00	SDS	2			Blank Module
W9720	357	6.00	ESS	1			Blank Module, Copper Clad on both sides
W9721	357	8.00	EDS	2			Blank Module, Copper Clad on both sides
W9722	357	13.00	EQS	4			Blank Module, Copper Clad on both sides

Number of socket slots required.

foreword

This ninth edition of the LOGIC HANDBOOK is your guide to the most extensive line of products offered by Digital Equipment Corporation for implementing electronic logic designs for instrumentation, computer interfacing, data gathering or control. This handbook is a basic reference for anyone involved in specifying, manufacturing or using solid-state logic.

Our M Series TTL integrated circuit modules are featured in this edition. The M Series line consists of more than 100 modules ranging from basic and fundamental logic modules to self-contained computer interfacing modules and the M Series Logic Lab for use in breadboarding M Series logic designs.

The impact of advancing technology can be seen in M Series evolution. From the beginning, M Series was TTL-integrated, circuit-oriented; the current trend is toward MSI and LSI. The result is more complexity (and more built-in design solutions) per module. Many of the modules in this handbook amount to full-scale digital subsystems.

Further versatility has been added to the M Series line by the availability of three Interfacing Kits, described herein. The kits offer the user the capability of implementing more complex input/output interfacing between a PDP-11 computer and peripheral equipment at low cost and minimum design time.

A new design concept has been made available to the designer of digital systems with the availability of RT Modules listed in this handbook. These modules, using the Register Transfer concept, cut design time drastically, reduce documentation and demand only a fundamental knowledge from the system designer.

This edition of the handbook also covers the A Series of analog modules, the W Series of wire wrappable modules, collage and blank boards in the FLIP CHIP form factor, and a complete line of power supplies and hardware. An expanded section on cabling and cable accessories has been added to simplify system interconnection design. All these support functions provide a total capability for designing, implementing, and assembling a modular system, small or large, at the lowest cost per function in the industry.

A new dimension has been added to this edition with the inclusion of two popular data entry terminals. These are the RT01 Numeric Data Entry Terminal and the RT02 Alphanumeric Data Entry Terminal. Both terminals implement low-cost applications in the areas of management information systems, medical and clinical laboratories, industrial and production monitoring, banking transactions.

Extensive noncatalog products and services are available from DIGITAL. If you require unique functions that are not listed in this handbook, contact your local DIGITAL office (listed inside the back cover). The product you need may be available as a noncatalog item. In addition, DIGITAL maintains a Special Module Products Group with complete capability of design, layout, manufacturing and test. Custom product capability is not limited to modules alone but extends to the support hardware and accessories, including cabling, wire wrapping and cabinets.

A worldwide staff of DIGITAL sales engineers is prepared to respond to your technical and commercial needs. From a backlog of logic system design experience, DIGITAL may have a detailed solution to your application or interface requirement.

Please address any comments on this handbook, or inquiries concerning special services, to:

Digital Equipment Corporation
146 Main Street
Maynard, Massachusetts 01754

Attn: Logic Products
Sales Support Manager

introduction

ORGANIZATION OF HANDBOOK

This edition of the LOGIC HANDBOOK is organized in eight functional sections for maximum ease of reference. With each section, module descriptions are presented in alphanumeric order by module designation. To locate a specific module, consult the Product List at the beginning of the handbook.

Logic and Control: This section includes all of the M Series basic logic modules and those complex functional modules that are not computer-interface oriented. An introduction to this section describes the basic characteristics of the TTL integrated circuits which are the principal active elements of M Series.

Computer Interfacing: This group includes the M Series complex functional modules that simplify interfacing to the PDP-11 UNIBUS or PDP-8/e, 8/m OMNIBUS. Also in this group are the modules for interfacing the external I/O bus of earlier PDP-8 family computers plus level converters and other interface-oriented support modules. Introductory information defines the control and data signals of the OMNIBUS, UNIBUS, and external I/O bus.

Analog: The A Series of analog modules supports the M Series by providing a two-way translation between continuously varying real-world voltage measurements and the digital realm of control and computation. The present A Series emphasizes 10- and 12-bit performance in a family of mutually compatible functions—multiplexers, operational amplifiers, sample-and-hold circuits, D/A and A/D converters, reference voltage sources and an expanded group of multiplying D/A converters.

Accessory Modules: DIGITAL offers a wide line of wire wrappable, collage, and blank modules in the FLIP CHIP form factor for experimenting and breadboarding by users who want to work directly with discrete components and integrated circuit packages. Included in this section are module extenders and PDP-8/e, 8/m OMNIBUS bus connectors.

DECkits: These kits offer greater interfacing capability to the PDP-11 UNIBUS at the lowest cost possible. Complex logic module building block concepts are now expanded to greater limits of versatility in kit form. Capable of performing a highly complex computer interface, the kit is a collection of logic modules assembled by the user to a prewired system unit.

Power Supplies: This section describes a wide selection of H and K Series dc power supplies for small and large systems. Summary tables are included that will help the system designer select the power supply appropriate to his system.

Cabling: This edition of the handbook presents a greatly expanded section on M and W Series cables and cabling accessories. DIGITAL offers a complete line of prefabricated cables for interconnection of free-standing logic systems as well as computer-based installations. Bulk cables and cable cards are available so that the user can design and construct his own custom interconnections with a minimum of custom design and planning.

Hardware: DIGITAL makes a complete line of hardware accessories to support its module series. Module connectors are available for as few as one module to as many as 64 in a single 19" mounting panel. A complete line of cabinets is available to house the modules and their connector blocks, as well as provide a convenient means for system expansion. Wiring accessories and a complete selection of support hardware simplify all phases of physical construction. This edition's hardware selection is expanded to include the latest cabinet and hardware features.

Data Entry Terminals: This section describes Data Entry Terminals which provide easy, low-cost access to total information in a computer. They offer ideal communication links in numerous situations that require interactive communication between both local and remote operators and the central data processor.

Typical applications are: Stockroom Inventory Control, Management Information, Production Line Monitoring, Security Systems, Credit Checking, Banking Transactions.

The terminals feature Teletype and EIA serial line compatibility. Interface to a computer is accomplished via a standard full-duplex 4-wire data communications Teletype interface. Standard interfaces are available for the PDP-8, -10, -11, -12, -15, and -16 computers. Modem interface signals corresponding to EIA RS-232C specifications are also provided.

Lab Series: This group includes the COMPUTER LAB digital logic trainer, the K Series Logic Lab (a rack-mounted, plugboard-panel breadboarding and training facility for K Series modules) and the M Series Logic Lab (a console and rack structure that mounts and interconnects M Series modules for training, experimentation, and system design).

M SERIES MODULE SELECTOR GUIDE

Available as a companion to this handbook is the M Series Module Selector Guide, a pocket-sized chart that is used for a quick look-up of the characteristics of the M Series modules and the most important supporting hardware and accessories and power supplies in this handbook. Contact your local DIGITAL Sales Office for a free copy of the Module Selector Guide.

DIGITAL EQUIPMENT CORPORATION ENGINEERING SERVICES

In addition to supplying a complete line of standard and special hardware and accessories, Digital Equipment Corporation also provides an engineering, design and manufacturing service in support of customer applications. These services are available upon request and consist of the following:

Special Logic Modules: Many of the same advanced manufacturing and testing techniques which DIGITAL employs to produce its standard modules are applied to building special modules. DIGITAL engineers can provide full module design and development services or they can work with user-supplied drawings and parts lists, depending upon user needs.

Wire Wrapping: Using the latest in automatic wire wrapping equipment, DIGITAL can efficiently wire and check connector panels according to customer-supplied wire list and specifications.

Special Cables: When standard cables and cable lengths are not applicable to customer requirements, DIGITAL offers a complete cable fabrication service to build special cables according to customer specifications.

Interface Design: DIGITAL maintains a staff of experienced applications engineers who are capable of designing or providing design information for interfacing DIGITAL computers to custom control systems and equipment.

Logic Arrays: Special-purpose logic systems can be efficiently designed and built from customer-supplied data. DIGITAL's capability extends from limited production system to high-volume production and insures both optimum design and high reliability at a reasonable cost to the customer.

SPECIAL SYMBOLS AND ABBREVIATIONS

Logic symbols used in this handbook conform, in general, to widely accepted MIL standards. All basic M Series logic symbols (AND, OR, NAND, NOR, Inverter, Flip-Flop) are described in the introduction to the M Series logic and control modules.

Input Loading and Output Drive

On the logic diagrams of this handbook, input and output loading, expressed in TTL unit loads, appear in boxes terminating each input or output signal line. In the 2-input NAND gate example of Figure 1, both inputs (pins A1 and B1) present one TTL unit load. The output (pin C1) is capable of driving 10 TTL unit loads. The arrows eliminate any possible confusion as to the direction of signal flow.

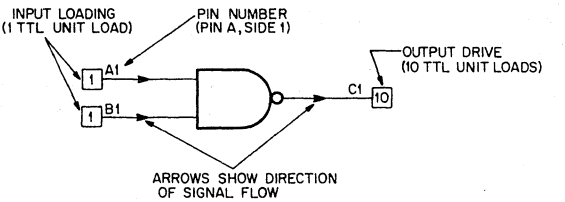


Figure 1. Logic Diagram Input Loading and Output Drive Symbols

Bus Drivers and Receivers

Drivers and receivers that transfer data along the bidirectional transmission lines of the PDP-8/e, 8/m OMNIBUS or the PDP-11 UNIBUS differ somewhat from similar TTL NAND gates or inverters. Typical examples are shown in Figure 2. The "B" in the loading box indicates that the driver or receiver circuit is to be connected to an OMNIBUS or UNIBUS signal or control line. In this application, unit loading need not be considered. "R" identifies a line receiver and "D" identifies a line driver. Inputs to line receivers or drivers may also be standard TTL levels, in which case, TTL unit loads are shown as usual in the loading box.

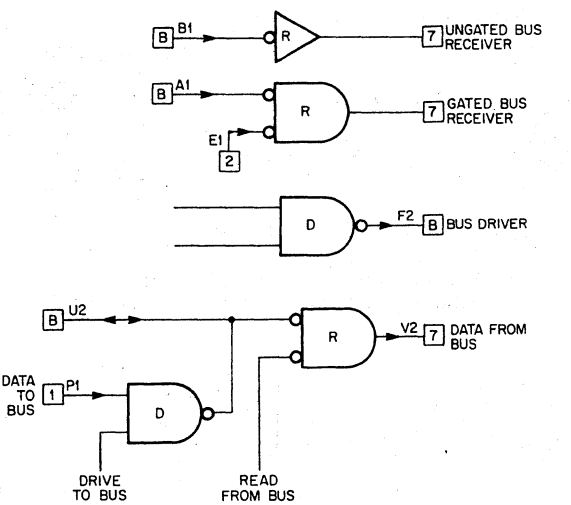


Figure 2. Bus Driver and Receiver Symbols

Electrical characteristics of these circuits are described in the introduction to M Series Computer Interfacing Modules.

Level Converters
Whenever logic levels are translated from one set of voltages to another, the conversion is shown taking place in a square level-converter symbol. Inside the box, the corresponding logic levels are related in a simple truth table. The example of Figure 3 shows a level converter stage that accepts TTL levels (LOW and HIGH) and delivers DEC negative voltage levels (—3 V and ground).

Input loading is two TTL unit loads. Whenever loading is peculiar, it is defined in a note on the drawing as in the output of Figure 3.

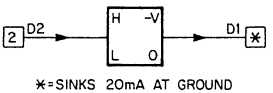


Figure 3. Typical Level Converter

Special Analog Symbols
Symbols used on analog circuit drawings to represent multiplex switches and operational amplifiers are shown in Figure 4. Loading boxes for analog inputs and outputs contain the letter "A"; do not connect such signals to logic levels.

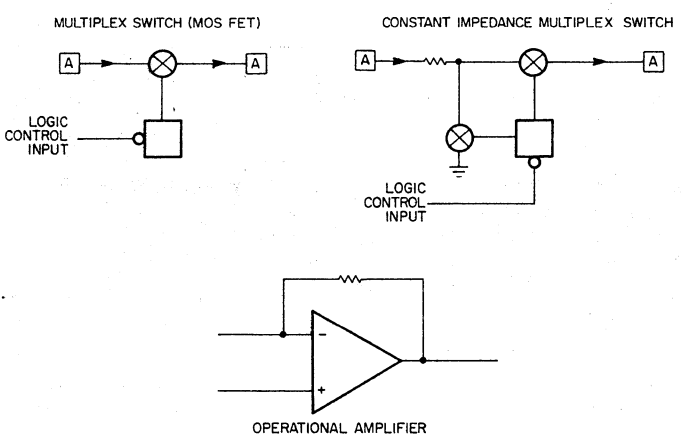


Figure 4. Special Analog Symbols

Signal and Function Names
Inputs and outputs of M Series logic modules may be assigned a signal name, a function name, or both. (See Figure 5.) Signal names appear *outside* blocks or logic symbols to identify typical input or output signals.

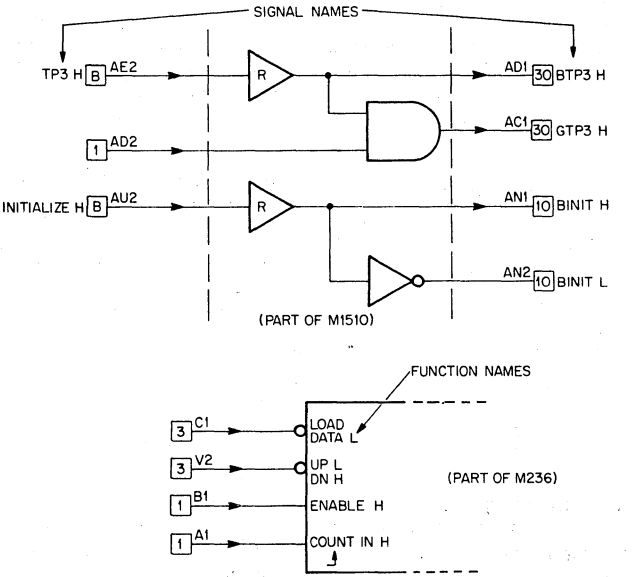


Figure 5. Signal and Function Names

Digital Equipment Corporation uses standard terminology to name signal lines to aid the reader in determining their active state. Either an H or L follows the signal name mnemonic, separated by a space. This letter indicates the asserted (true) state of the signal. An H means the signal is asserted when HIGH (+3 V) and an L means the signal is asserted when LOW (0 V). For example, a UNIBUS data line is called BUS D00 L and a grant line is called BUS BG4 H.

On the logic diagrams of many computer interfacing modules in this handbook, signal names peculiar to one computer, such as the PDP-11, appear as an example of typical usage. Signal names may be changed to those of another computer or interfacing device if logically appropriate.

Function names appear *inside* the blocks of functional modules. They identify the *function* of input or output signals. The user may add his own signal names.

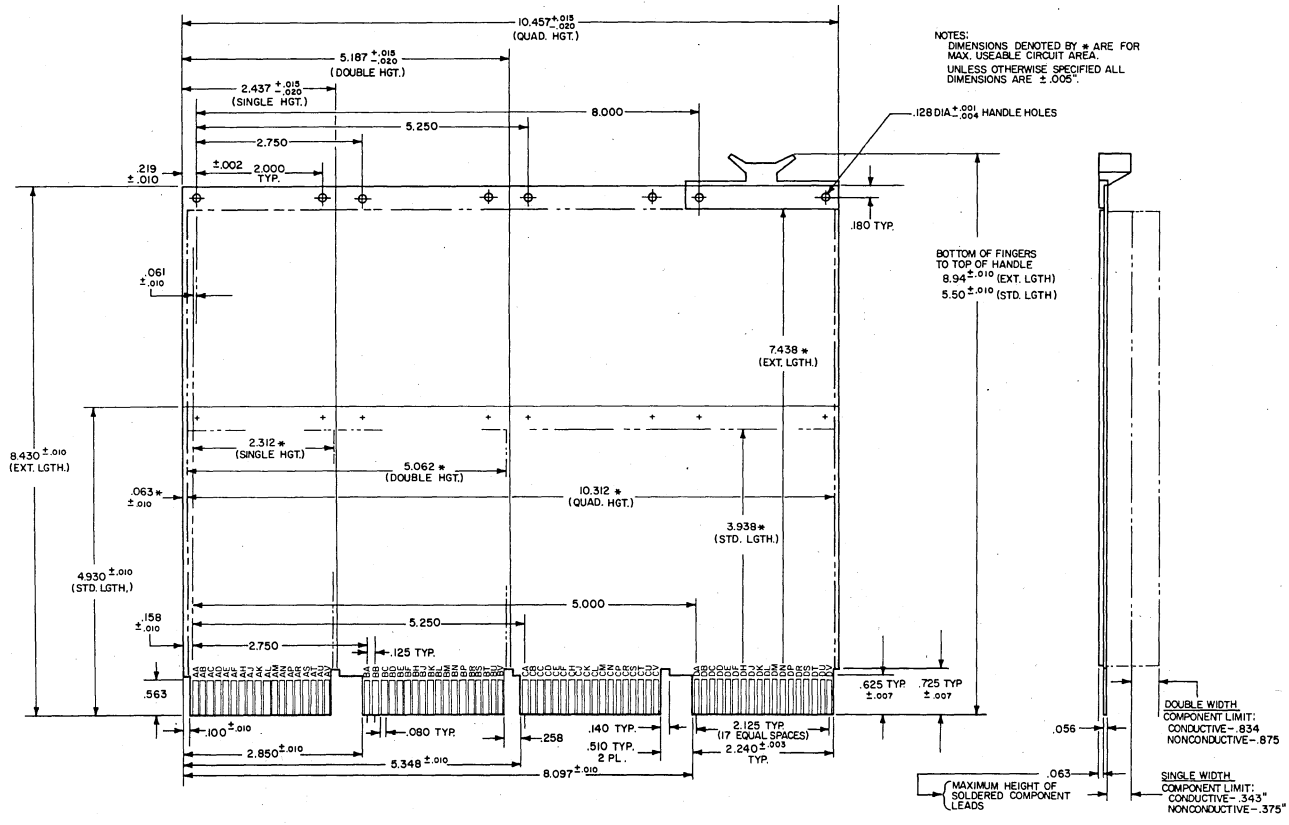
Abbreviations

Abbreviations used in signal and function names in this handbook are defined in Table 1.

Table 1—Abbreviations

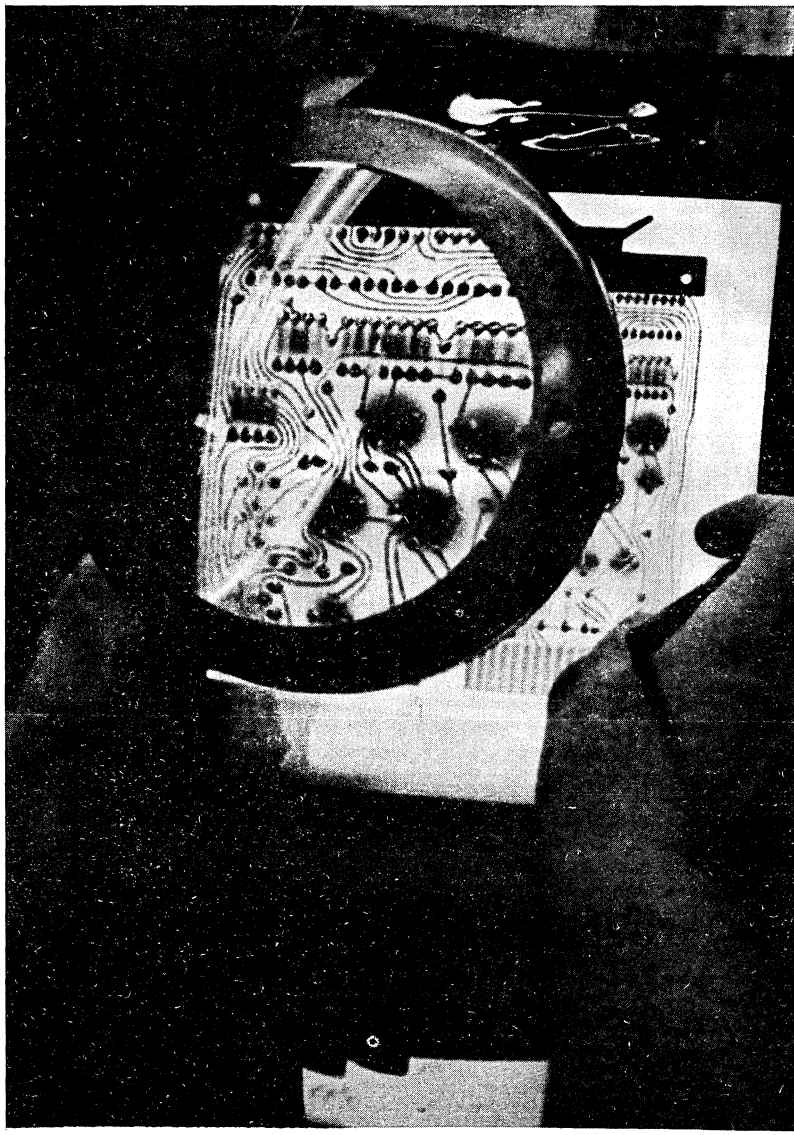
ABBREVIATIONS	DEFINITION
ALTN	Alternate
AMPL	Amplifier
ANLG	Analog
BPS	Bits Per Second
CAP	Capacitor
CLR	Clear
CMPR	Compare
COM	Common
CONT	Control
CVRSN	Conversion
DAC	Digital to Analog Converter
EXT	External
GND	Ground
H	High (TTL +3 V Logic Level)
INIT	Initialize
INT, INTR	Interrupt
INTL	Internal
L	Low (TTL 0 V Logic Level)
OUT	Output
P.I.	Program Interrupt
POT	Potentiometer
PRGM	Program
REF	Reference
RTN	Return
SER	Serial
S.H.	Sample and Hold
TRIG	Trigger

MODULE DIMENSIONS



m series

logic and control modules



DEC Module assembly lines combine automated manufacturing steps with visual inspection and computer controlled testing.

M-SERIES LOGIC AND CONTROL MODULES

Modules in this section appear in numerical order. The six functional categories of M-Series logic and control modules are:

GATES	
M111	Inverter
M112	NOR Gates
M113	NAND Gates
M115	NAND Gates
M116	NOR Gates
M117	NAND Gates
M119	NAND Gates
M121	AND/NOR Gates
M133	Input NAND Gates
M135	NAND Gates
M139	NAND Gates
M141	NAND/OR Gates
M160	AND/NOR Gates
M169	Gating Module
M610	Open Collector NAND Gates
M1103	AND Gates
M1307	AND Gates
M1701	Data Selector

FLIP-FLOPS	
M165	8 Buffers
M202	Triple J-K Flip-Flop
M203	8 R/S Flip-Flops
M204	General-Purpose Buffer & Counter
M205	General-Purpose Flip-Flops
M206	General-Purpose Flip-Flops
M207	General-Purpose Flip-Flops
M208	8-Bit Buffer/Shift Register
M232	16-Word RAM
M245	Shift Register
M246	5 D-Type Flip-Flops
M248	Multipurpose Shift Register
M253	16-Word $\times$ 12 Bit RAM
M260	Associative Memory

TIME RELATED	
M302	Dual Delay Multivibrator
M306	Integrating One Shot
M310	Delay Line
M360	Variable Delay
M401	Variable Clock
M403	RC Multivibrator Clock
M404	Crystal Clock
M405	Crystal Clock
M410	Reed Clock
M452	Variable Clock

M501	Schmitt Trigger
M521	K to M Converter
M602	Pulse Amplifier
M606	Pulse Generator
M671	M to K Converter

NUMERIC

M152	Dual 1 of 8 Decoder
M155	4 Line to 16 Line Decoder
M159	Arithmetic/Logic Unit
M161	Binary to Octal Decimal Decoder
M162	Parity Circuit
M168	12-Bit Magnitude Comparator
M191	ALU Look Ahead
M230	Binary to BCD & BCD to Binary Converter
M236	12-Bit Binary Up/Down Counter
M237	3-Digit BCD Up/Down Counter
M238	Synchronous Up/Down Counter
M1713	16 Line-to-Line Data Selector

LOGIC AMPLIFIERS

M040	Solenoid Driver
M050	Indicator Driver
M060	Solenoid Driver
M617	4-input Power NAND Gates
M627	NAND Power Amplifier
M660	Positive Level Cable Driver
M661	Positive Level Driver

MISCELLANEOUS

M002	Logic HIGH Source
M261	4-State Motor Translator
M262	10-State Motor Translator
M706	Teletype Receiver
M707	Teletype Transmitter
M906	Cable Terminator
M7390	Asynchronous Transceiver
M9100	854 to 854 Flip Chip Adapter

M Series modules contain high speed TTL logic in both general purpose and functional logic arrays. TTL was chosen for its high speed, capacitance drive capability, high noise immunity and choice of logical elements. High performance integrated circuit modules are now available at approximately one half the price of their discrete or hybrid counterparts.

In addition to the reduced cost of integrated circuits, Digital's advanced manufacturing methods and computer controlled module testing have resulted in considerable production cost savings, reflected in the low price of all M Series Modules.

GENERAL CHARACTERISTICS

M Series high-speed, monolithic integrated circuit logic modules employ TTL (transistor-transistor logic) integrated circuits which provide high speed, high fan out, large capacitance drive capability and excellent noise margins. The M Series includes a full digital system complement of basic modules which are designed with sufficient margin for reliable system operation at frequencies up to 6 MHz. Specific modules may be operated at frequencies up to 10 MHz. The integrated circuits are dual in-line packages.

The M Series printed circuit boards are identical in size to the standard FLIP CHIP™ modules. The printed circuit board material is double-sided providing 36-pins in a single height module. Mounting panels (H910 and H911) and 36-pin sockets (H803 and H808) are available for use with M Series modules. Additional information concerning applicable hardware may be found in the Power Supply & Hardware and Accessories section of this handbook.

M Series modules are compatible with Digital's K Series and, through the use of level converters, are compatible with all of Digital's other standard negative voltage logic FLIP CHIP® modules.

TTL NAND GATE

The basic gate of the M Series is a TTL NAND GATE. Figure 1 is the basic two input NAND gate schematic diagram. The circuit is divided into 3 major sections, the multiple emitter input, the phase splitter and the totem pole output circuit. The two diode model of a transistor shown in Figure 2 will be used in the analysis of the circuit. A forward biased silicon junction (i.e. diode) gives a voltage drop of about 0.75 volts and a saturated silicon transistor has a collector emitter voltage of 0.4 volts average. These two figures will be used throughout the following discussion.

With either input at the LO logic level (0.0V-0.8V) the multiple emitter input transistor will be ON with its base residing at about $0.75 + 0.4 = 1.15$ volts. The three diode string consisting of Q_1's base collector diode, Q_2's base emitter diode, and Q_4's base emitter diode will have only 1.15 volts across it and will therefore be conducting only leakage currents ($0.75 + 0.75 + 0.75 =$ 2.25 volts required for forward bias). With no current flowing into the base emitter junction of Q_2, the transistor will be OFF and its collector emitter voltage is alowed to rise. Similarly with no current flowing in the base emitter diode of Q_4 the transistor is OFF and its collector emitter voltage is allowed to rise. When both Q_2 and Q_4 are OFF, Q_3 is freed to pull the output voltage to a HI level. The voltage levels present in the circuit with one or more LO inputs is shown in Figure 4.

If both inputs are HI (2.4-3.6 volts) the head of the three diode string will reside at about 2.25 volts and there will be a current path from the 4K base resistor on the input transistor through the diode string to ground as shown in Figure 5. With current flowing in the base emitter junctions of both Q_2 and Q_4, both transistors will be turned ON. Q_3 is held OFF whenever Q_2 is ON. The output is driven LO (0.0V-0.4V) by transistor Q_4. The voltage levels present in the circuit with both inputs HI and are shown in Figure 6.

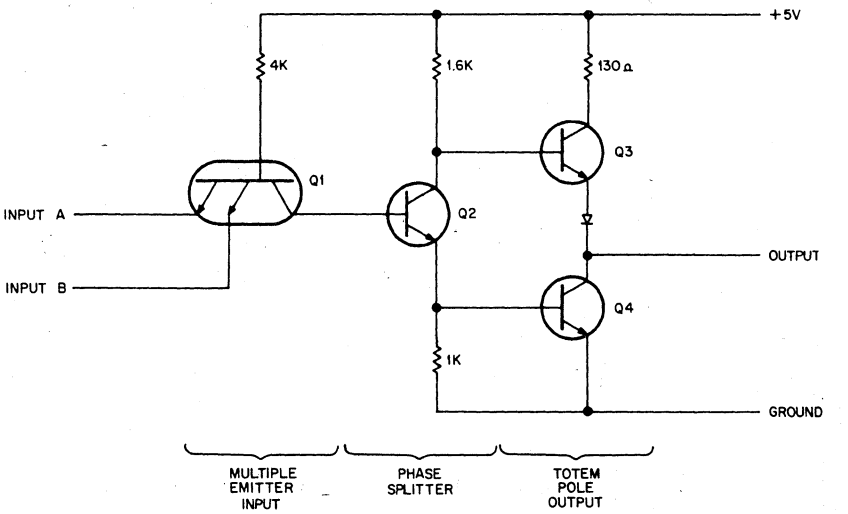


Figure 1 TTL NAND Gate Schematic Diagram

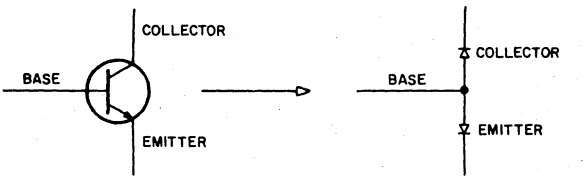


Figure 2 Two Diode Model For Transistor

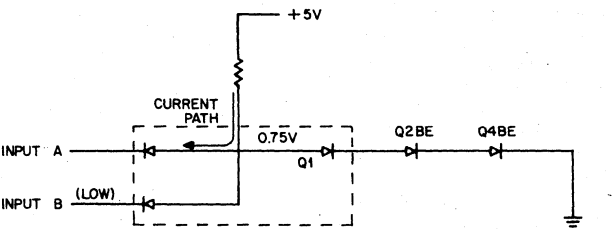


Figure 3 Diode Equivalent NAND Gate Circuit, One Input LO

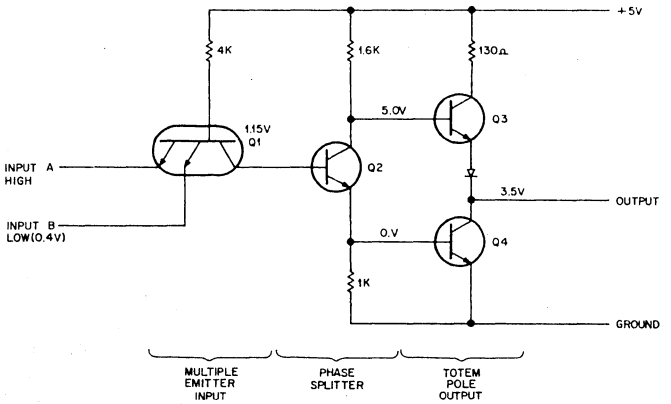


Figure 4 TTL NAND Gate Schematic Diagram, One Input LO

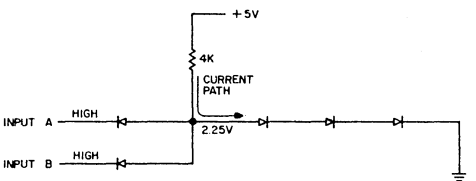


Figure 5 Diode Equivalent NAND Gate Circuit, Both Inputs HI

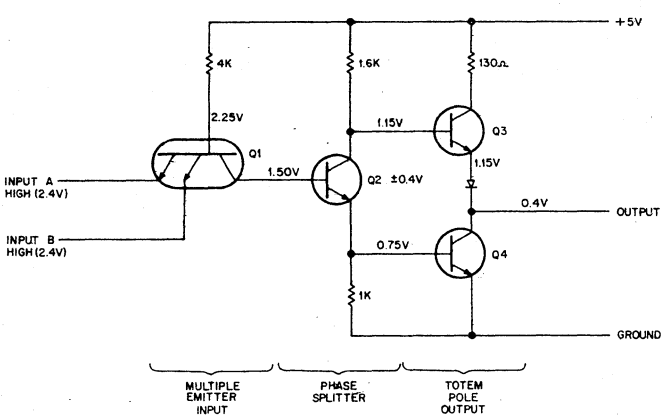


Figure 6 TTL NAND Gate Schematic Diagram, Both Inputs HI

OPERATING CHARACTERISTICS

Power Supply Voltage: 5 Volts ± 5%

Operating Temperature Range: 0° to 70°C

Speed: M Series integrated circuit modules are rated for operation in a system environment at frequencies up to 6 MHz. Specific modules may be operated at higher frequencies as indicated by the individual module specifications.

LOGIC LEVELS AND NOISE MARGIN
A gate input will recognize 0.0 volts to 0.8 volts as logical LO and 2.0 volts to 3.6 volts will be recognized as a logical HI. An output is between 0.0 volts and 0.4 volts in the logical LO condition. The logical HI output condition is between 2.4 volts and 3.6 volts. Figure 7 shows diagrammatically the acceptable transistor-transistor logic levels. The worst case noise margin is 400 millivolts that is, an output would have to make at least a 400 millivolt excursion to cause an input which is connected to it to go into the indetermined voltage region. For instance if an output were at 0.4 volts (worst case logical LO) there would have to be a + 400 mv swing in voltage to cause inputs connected to it to go into their indetermined region.

Input and Output Loading: The input loading and output drive capability of M Series modules are specified in terms of a specific number of unit loads. Typically the input loading is one unit, however certain modules may contain inputs which will present greater than one unit load. The typical M Series module output will supply 10 unit loads of input loading. However, certain module outputs will deviate from a 10 unit load capability and provide more or less drive. Always refer to the individual module specifications to ascertain actual loading figures.

Unit Load: In the logic 0 state, one unit load requires that the driver be able to sink 1.6 milliamps (maximum) from the load's input circuit while maintaining an output voltage of equal to or less than +0.4 volts. In the logic 1 state, one unit load requires that the driver supply a leakage current 40 microamps (maximum) while maintaining an output voltage of equal to or greater than +2.4 volts.

Timing: M Series pulse sources provide sufficient pulse duration to trigger any M Series flip-flop operating within maximum propagation delay specifications. Detailed timing information appears later in this section and in the module specifications.

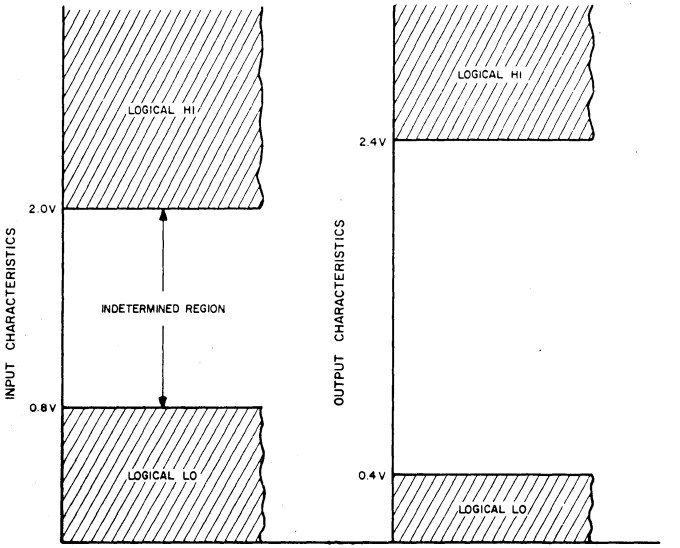
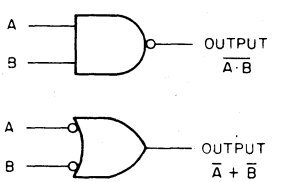


Figure 7 Logic Levels

NAND Logic Symbol: Logic symbology used to describe M Series modules is based on widely accepted standards. Logic symbols and a truth table for the NAND gate are shown in Figure 8.



A	B	OUTPUT
L	L	H
L	H	H
H	L	H
H	H	L

Figure 8 NAND Gate Logic Symbol and Truth Table

The first symbol is visually more effective in applications where two high inputs are ANDed to produce a low output. The second symbol better represents an application where low inputs are ORed to produce a high output.

TTL AND/NOR GATE

With a few modifications, the basic TTL NAND gate can perform an AND/NOR function useful in exclusive OR, coincidence, line selection and NOR gating operations. The modified circuit is shown in simplified form in Figure 9.

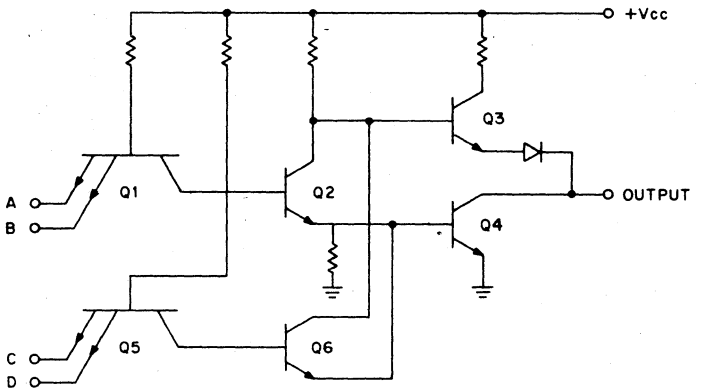
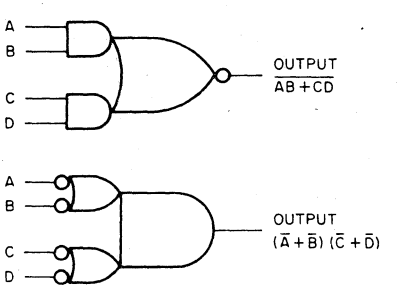


Figure 9 TTL AND/NOR Gate Simplified Schematic

Circuit Operation: The basic elements of the TTL NAND gate are used without modification. The phase-splitter (Q2) is paralleled with an identical transistor (Q6), also controlled by multiple-emitter input transistor which receives two additional inputs, C and D. When either of the input pairs are high, the phase inverter operates to switch the output voltage low. Circuit performance is essentially identical to the TTL NAND circuit.

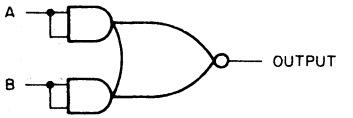
AND/NOR Logic Symbol: The logic symbols for the AND/NOR gate are shown and defined in Figure 10.



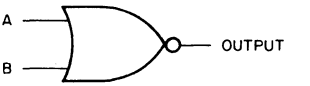
A	B	C	D	OUTPUT
H	H	ANY		L
ANY		H	H	
L	H	L	H	H
L	H	H	L	
H	L	H	L	
H	L	L	H	

Figure 10 AND/NOR Gate Logic Symbols and Truth Table

NOR Configuration: The AND/NOR gate can perform a straight NOR function if the AND gate inputs are tied together as shown in Figure 11.



AND/NOR INPUTS TIED

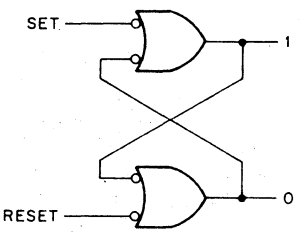


RESULTING NOR SYMBOL

Figure 11 NOR Connection of AND/NOR Gate

NAND GATE FLIP-FLOPS

RS Flip-Flop: A basic Reset/Set flip-flop can be constructed by connecting two NAND gates as shown in Figure 12.



PREVIOUS STATE		INPUT CONDITION		RESULT	
1	0	SET	RESET	1	0
L	H	L	H	H	L
H	L	H	L	L	H
L	H	H	H	NO CHANGE	
H	L	H	H	NO CHANGE	
H	L	L	H	NO CHANGE	
L	H	H	L	NO CHANGE	
L	H	L	L	H*	H*
H	L	L	L	H*	H*

*Ambiguous state: In practice the input that stays low longest will assume control.

Figure 12 RESET/SET NAND Gate Flip-Flop

CLOCKED NAND GATE FLIP-FLOPS

The Reset-Set flip-flop can be clock-synchronized by the addition of a two-input NAND gate to both the set and the reset inputs. (See Figure 13.) One of the inputs of each NAND is tied to a common clock or trigger line.

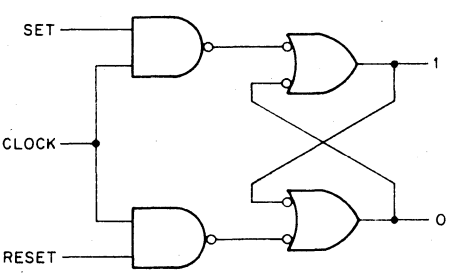


Figure 13 Clocked NAND Gate Flip-Flop

A change of state is inhibited until a positive clock pulse is applied. The ambiguous case will result if both the set and reset inputs are high when the clock pulse occurs.

M SERIES GENERAL-PURPOSE FLIP-FLOPS

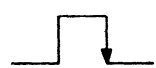
Two types of general-purpose flip-flops are available in the M Series, both of which have built-in protection against the ambiguous state characteristic of NAND gate flip-flops.

FLIP-FLOP CLOCK INPUT SYMBOLS

The D type flip-flop is a true leading (positive going voltage) edge triggered flip-flop and the D input is locked out until the clock input returns to low. The symbol to indicate this function will be as follows;

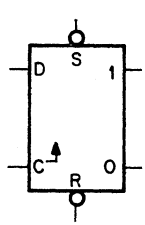
D TYPE FLIP FLOP CLOCK

The operation of the J-K type flip-flop is to transfer the information present at the J and K inputs just prior to and during the clock pulse to the master flip-flop when the threshold is passed on the leading (positive going voltage) edge of the clock pulse. The information stored in the master flip-flop is transfered to the slave flip-flop, and consequentially to the outputs, when the threshold is passed on the trailing (negative going voltage) edge of the clock pulse. The symbol to indicate this function will be as follows;

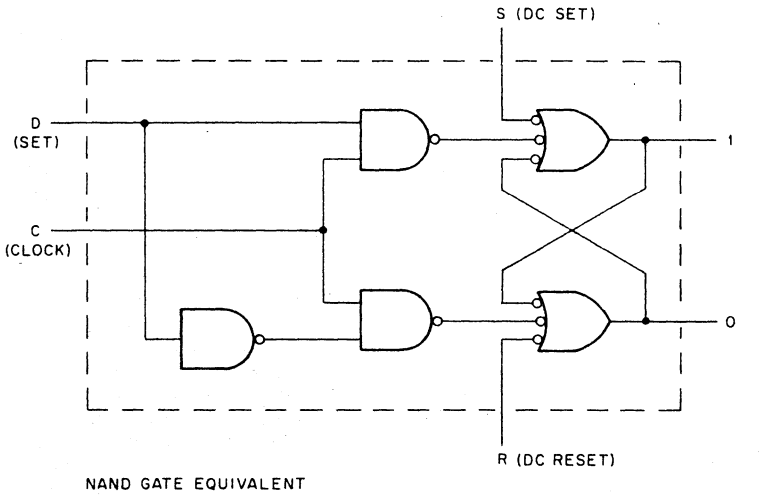


J K TYPE FLIP FLOP CLOCK

D Type Flip-Flop: The first of these is the D type flip-flop shown in Figure 14 In this element, a single-ended data input (D) is connected directly to the set gate input. An inverter is provided between the input line (D) and the reset input. This ensures that the set and reset levels cannot be high at the same time.



LOGIC SYMBOL



SIMPLIFIED NAND GATE EQUIVALENT

Figure 14. D Type General Purpose Flip-Flop

The flip-flop proper employs three-input NAND gates to provide for dc set and reset inputs.

D type flip-flops are especially suited to buffer register, shift register and binary ripple counter applications. Note that D type devices trigger on the leading (or positive going) edge of the clock pulse. Once the clock has passed threshold, changes on the D input will not affect the state of the flip-flop due to a lockout circuit (not shown).

A characteristic of the D type flip-flop which is not illustrated in the NAND gate equivalent circuit is the fact that the D input is locked out after the clock input threshold voltage on the leading (positive going voltage) edge of the clock has been passed. The D input is not unlocked until the clock input threshold voltage of the trailing (negative going voltage) edge has been passed.

"MASTER-SLAVE J-K FLIP-FLOP"

The two unique features of a J-K flip-flop are: A) a clock pulse will not cause any transition in the flip-flop if neither the J nor the K inputs are enabled during the clock pulse, and B) if both the J and the K inputs are enabled during the clock pulse, the flip-flop will complement (change states). There is no indeterminate condition in the operation of a J-K flip-flop.

A word of caution is in order concerning the clock input. The J and K inputs must not be allowed to change states when the clock line is high, the output will complement on the negative going voltage transition of the clock. It is for this reason that the clock line must be kept low until it is desired to transfer information into the flip-flop and no change in the states of the J and K inputs should be allowed when the clock line is high.

The J-K flip-flops used are master-slave devices which transfer information to the outputs on the trailing (negative going voltage) edge of the clock pulse. The J-K flip-flop consists of two flip-flop circuits, a master flip-flop and a slave flip-flop. The information which is present at the J and K inputs when the leading edge threshold is passed and during the clock high will be passed to the master flip-flop (The J and K inputs must not change after the leading edge threshold has been passed). At the end of the clock pulse when the threshold of the clock is passed during the trailing (negative going voltage) edge, the information present in the master flip-flop is passed to the slave flip-flop. If the J input is enabled and the K input is disabled prior to and during the clock pulse, the flip-flop will go to the "1" condition when the trailing edge of the clock occurs. If the K input is enabled and the J input is disabled prior to and during the clock pulse, the flip-flop will go to the "0" condition when the trailing edge of the clock pulse occurs. If both the J and K inputs are enabled prior to and during the clock pulse, the flip-flop will complement when the trailing edge of the clock pulse occurs. If both the J and K inputs are disabled prior to and during the clock pulse, the flip-flop will remain in whatever condition existed prior to the clock pulse when the trailing edge of the clock pulse occurs.

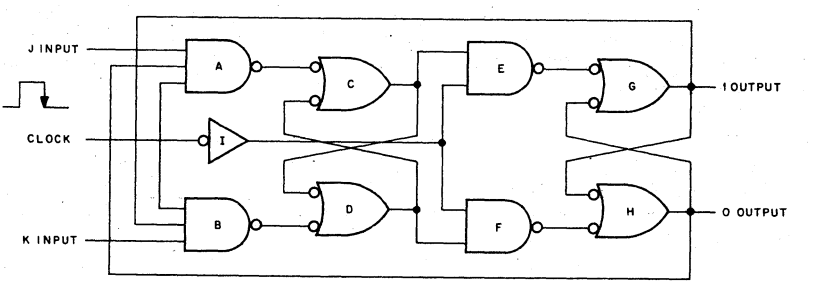


Figure 15. Master-Slave J-K Flip-Flop

Figure 16 shows a functional block diagram of a master slave J-K flip-flop using NAND gates. Gates C and D are the master flip-flop. Gates G and H are the slave flip-flop. Gates A and B are the steering network of the master flip-flop and the steering network for the slave flip-flop is comprised of gates E, F, and 1. The 1 output of the master flip-flop is point X. The operation of the flip-flop will be studied by examining the "1" to "0" transition of the flip-flops, with both the J and the K inputs enabled with a HI level before the clock pulse. When the leading edge of a HI clock pulse occurs, gate B will be enabled with three HI inputs. This will provide a RESET signal for the master flip-flop which will then go to the "0" condition. The slave flip-flop remains in the "1" condition while the clock pulse is HI because gate I is providing a LO signal to both gates E and F, thereby blocking inputs to the slave flip-flop. When the trailing edge of the clock pulse occurs, gate F will be enabled with a HI level at both its inputs and a RESET signal will be provided to the slave flip-flop, which will then go to the "0" condition. The next clock pulse, with both the J and K enabled, would cause the master flip-flop to go to the "1" condition on the leading edge of the clock pulse and cause the slave flip-flop to go to the "1" condition on the trailing edge of the pulse. Figure 16 is a truth table for the J-K flip-flop showing all eight possible initial conditions.

INITIAL CONDITIONS				FINAL CONDITIONS	
OUTPUTS		INPUTS		OUTPUTS	
1	0	J	K	1	0
L	H	L	L	L	H
L	H	L	H	L	H
L	H	H	L	H	L
L	H	H	H	H	L
H	L	L	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	L	H	H	L	H

Figure 16. Master-Slave J-K Flip-Flop Truth Table

UNUSED INPUTS (GATES AND FLIP-FLOPS)

Since the input of a TTL device is an emitter of a multiple-emitter transistor, care must be exercised when an input is not to be used for logic signals. These emitters provide excellent coupling into the driving portions of the circuit when left unconnected. To insure maximum noise immunity, it is necessary to connect these inputs to a source of Logic 1 (High). Two methods are recommended to accomplish this:

1. Connect these inputs to a well filtered and regulated source of +3 volts. Pins U1 and V1 are provided on the M113, M117, M119, M121, M617, and M627 for this purpose.

2. Connect these inputs to one of the active inputs on the same gate. This results in a higher leakage current due to the parallel emitters and should be considered as an additional unit load when calculating the loading of the driving gate.

Connection of unused inputs to the supply voltage, Vcc, is not advisable, since power supplies are subject to transients and voltage excursions which could damage the input transistor.

TIMING CONSIDERATIONS

Standard Timing Pulse: In digital system design, a reference for system timing is usually required. The M Series modules M401 or M405 produces a standard pulse which provides such a reference. The standard pulse derived from each of these two modules is shown in Figure 17.

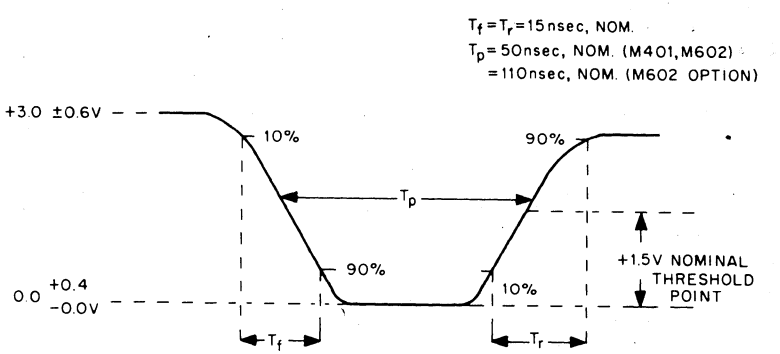


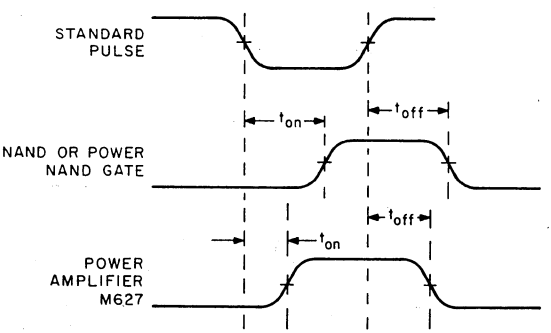
Figure 17 Standard Pulse

NAND Gate and Power Amplifier Propagation Delays: The standard pulse (Figure 17) is distributed throughout a system in negative form to maintain the leading edge integrity. (Since the TTL gate drives current in the logic 0 state, the falling edge is more predictable for timing purposes.) However, the standard pulse is of the wrong polarity for use as a clocking input to the type D and J-K flip-flops, requiring the use of a local inverter. Ordinarily, a NAND inverter is adequate. Where high fan-out is necessary, a M617 Power NAND is preferred.

For applications requiring both high fan-out and critical timing the M627 Power Amplifier is available. This module contains extremely high-speed gates which exhibit turn-on times differing by only a few nanoseconds.

Simultaneity is desirable in clock or shift pulses distributed to extended shift registers or synchronous counters.

Delays introduced by inverting gates and power amplifiers are illustrated in Figure 18. (Delays are measured between threshold points.)



DELAY (NANOSECONDS)			
t_{on}		t_{off}	
TYP.	MAX.	TYP.	MAX.
18	29	8	15
7	—	5	—

Figure 18 NAND Gate and Power Amplifier Delays

Flip-Flop Propagation Delays: D type flip-flops trigger on the leading or rising edge of a positive clock pulse; the propagation delay is measured from the threshold point of this edge. The set-up time of the D flop is also measured from this threshold point. Data on the D input must be settled at least 20 nanoseconds prior to the clock transition. The advantage of the D-flip-flop, however, is that the leading edge triggering allows the flip-flop AND gates to propagate while the clock pulse is still high. Figure 19 illustrates this situation.

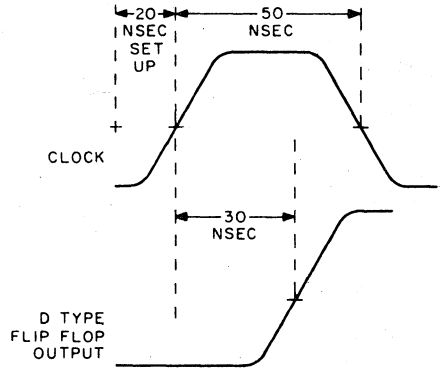


Figure 19. D Type Flip-Flop Timing

JK type flip-flops are, in effect, trailing edge triggering devices as explained previously. The only restriction on the J and K inputs is that they must be settled by the time that the rising edge occurs. Timing is shown in Figure 20.

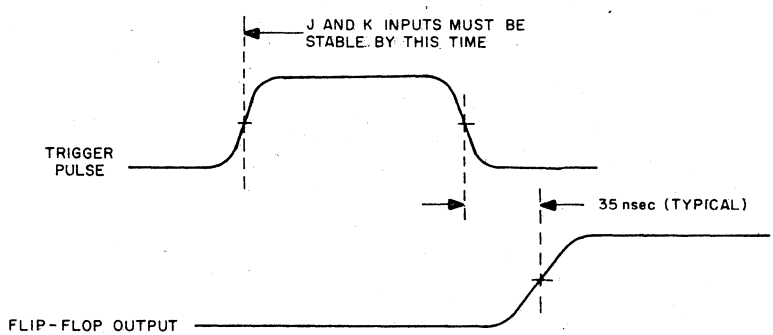


Figure 20. J-K Flip-Flop Timing

When using the dc Set or Reset inputs of either flip-flop type, propagation delays are referenced to the falling edge of the pulse. This is due to the inverted sense of these inputs. When resetting ripple type counters (where the output of one flip-flop is used as the trigger input to the next stage) the reset pulse must be longer than the maximum propagation delay of a single stage. This will ensure that a slow flip-flop does not introduce a false transition, which could ripple through and result in an erroneous count.

One-Shot Delay: Calibrated time delays of adjustable duration are generated by the M302 Delay Multivibrator. When triggered by a level change from a logical one to a logical zero, this module produces a positive output pulse that is adjustable in duration from 50 to 750 nsec with no added capacitance. Delays up to 7.5 milliseconds are possible without external capacitance. (See M302 specification.) Basic timing and the logic symbol are shown in Figure 21. The 100 picofarad internal capacitance produces a recovery time of 30 nsec. Recovery time with additional capacitance can be calculated using the formula;

$$t_r \text{ Nanoseconds} = 30 \frac{C \text{ Total (Picofarads)}}{100}$$

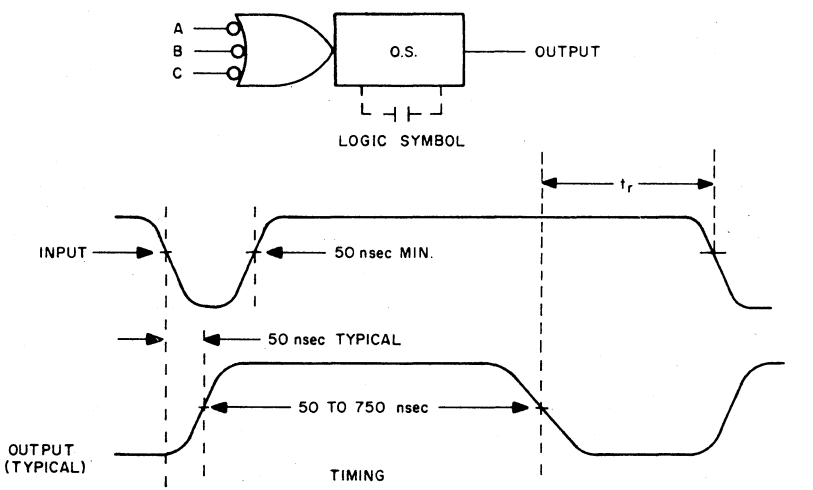


Figure 21. One-Shot Delay Timing and Logic Symbol

SYSTEM OPERATING FREQUENCY

Although individual propagation delays are significant in the design of digital logic, even more important is the maximum operating frequency of a system which is composed of these individual modules. Specifically designed systems may be operated at 10 MHz, but a more conservative design may result in a somewhat lower operating speed. M Series modules can be designed into a system with a 6 MHz clock rate with relative ease. This system frequency is derived by summing the delays in a simple logic chain:

1. A standard clock pulse width of 50 nsec is assumed. This period is measured from the threshold point of the leading edge to the threshold point of the trailing edge.

2. One flip-flop propagation delay of 35 nsec from the trailing edge of the clock pulse to the threshold point of the final state of the flip-flop is allowed.

3. Two gate-pair delays of 30 nsec each are assumed. (A gate-pair consists of two inverting gates in series.) Two gate-pair delays are usually required to perform a significant logic function with a minimum of parallel operations. The two gate-pair delays total 60 nsec.

The time necessary to perform these operations before the next occurrence of the clock pulse is the sum of the delays; 50 + 35 + 60, or 145 nsec. Allowing 20 nsec for variations within the system, the resulting period is 165 nsec, corresponding to a 6 MHz clock rate. This timing is demonstrated in Figure 22.

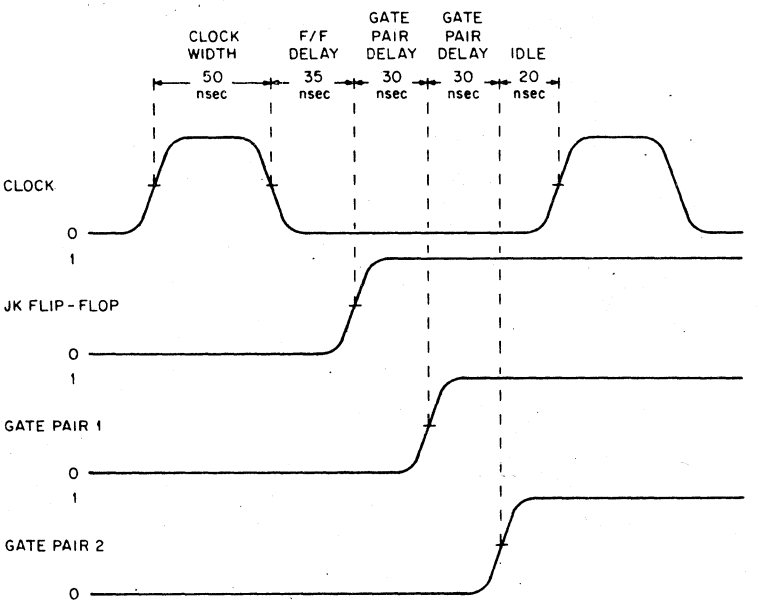


Figure 22. Delays Determining System Operating Frequency

Substitution of a D type flip-flop results in a similar timing situation. In a system using both D and J-K flip-flops, note that the D flip-flop triggers on the leading edge of the clock pulse and the J-K flip-flop triggers on the trailing edge. When calculating system timing using D flip-flops, remember that the flip-flop inputs must be settled at least 20 nsec prior to the occurrence of the clock pulse.

Preparation of a timing diagram that considers delays introduced by all logic elements will aid the designer in achieving predictable system performance.

M002
LOGIC HIGH SOURCE

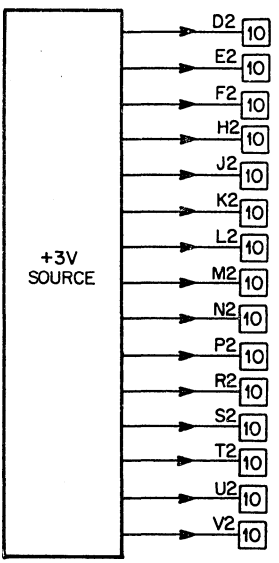
MISCELLA-NEOUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$10



Volts	Power mA (max.)	Pins
+5	16	A2
GND		C2, T1

To hold unused M Series TTL gate inputs HIGH, the M002 provides 15 outputs at +3 volts (logic HIGH) on pins D2 through V2. Up to 10 unused M Series gate inputs may be connected to any one output. If an M002 circuit is driven by a gate, it appears as two TTL unit loads or 3.2 mA at ground.

M040
SOLENOID DRIVER

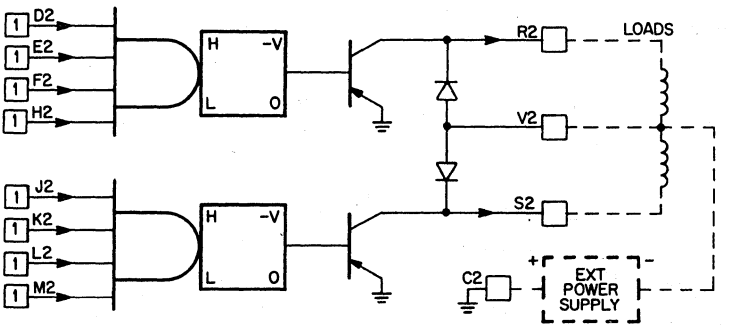
LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$39



Volts	Power mA (max.)	Pins
+5	47	A2
GND		C2, T1
—15	9	B2

The M040 contains two identical high-voltage driver circuits. Each consists of a 4-input positive NAND gate that controls a PNP transistor switch. The switch is capable of sinking up to 600 ma of current from an external power supply of up to —70 volts. One terminal of the load device (relay, etc.) must be connected to the external voltage, the other to the driver output. The positive terminal of the external supply connects to the module ground.

APPLICATIONS

The M040 can drive relays, solenoids, stepping motor windings and similar inductive loads.

Restrictions: Not recommended for

Indicator drive
115 V ac applications
Logic level conversion

FUNCTIONS

ON Condition: Each driver sinks current from the external circuit when all four control inputs are HIGH. The amount of current is determined by the external voltage and load impedance. (The internal switch is a saturated PNP transistor.) Typical output voltage when sinking 0.6 A is —2 volts.

OFF Condition: When one or more control inputs is LOW, the internal switch is a high impedance and the output voltage approaches the external voltage source. The output circuit draws a small amount of leakage current (typically 100 μA for a 70-volt external supply).

Anti-Kickback: Pin V2 of the driver module must be connected to the external supply so that the drivers will be protected from the back voltage generated by inductive loads. If the wire to the power supply is more than three feet long, it may have to be bypassed at the module with an electrolytic capacitor to reduce the pulse overshoot caused by the inductance of the wire.

Improving Recovery Time: If pin V2 is connected to the supply through a resistor, the recovery time of inductive loads can be decreased at a sacrifice in maximum drive voltage capability. Maximum rated supply voltage less actual supply voltage should be divided by load current to find the maximum safe resistance. When both circuits on a module are used, the load current for the above calculation is the sum of the currents.

PRECAUTIONS

Grounding: High current loads should be grounded directly at pin C2 of the M040, rather than at a frame or bus ground.

Parallel Operation: No more than two circuits should be paralleled to drive loads beyond the current capabilities of single circuits.

SPECIFICATIONS

Current sinking capability: 600 mA per circuit, max.

External supply voltage: 70 V dc max.

Circuit Delay: Typical propagation delay for each circuit is 5 μs (between 10% and 90% voltage points) for an external supply voltage of 70 volts.

M050
50 MA INDICATOR DRIVER

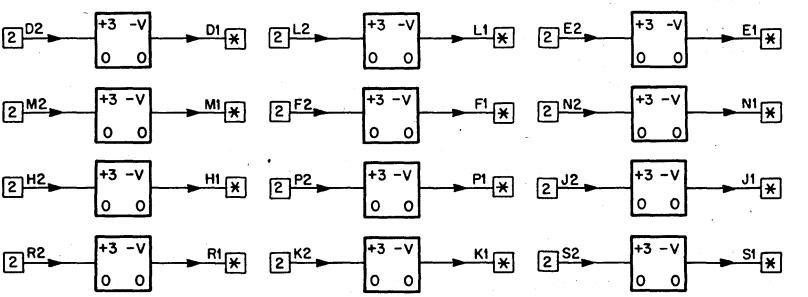
LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$31



* = 50 MA, -30V MAX.

Volts	Power mA (max.)	Pin
+5	47	A2
GND		C2
—15	16	B2

The M050 contains twelve transistor inverters that can drive miniature incandescent bulbs such as those on an indicator panel.

APPLICATIONS

The M050 is used to provide drive current for a remote indicator, such as Drake 11-504, Dialco 39-28-375, or Digital Indicator type 4908, or as a level converter to drive 4917 and 4918 indicator boards.

Restrictions: Do not use to drive inductive loads (relays, solenoids).
Note: For those applications requiring the sinking of current, refer to K Series.

FUNCTIONS

A LOW level on the input of the driver causes current to flow in the output.

SPECIFICATIONS

Each output is able to drive 50 mA into an external load connected to any voltage between ground and —30 volts.

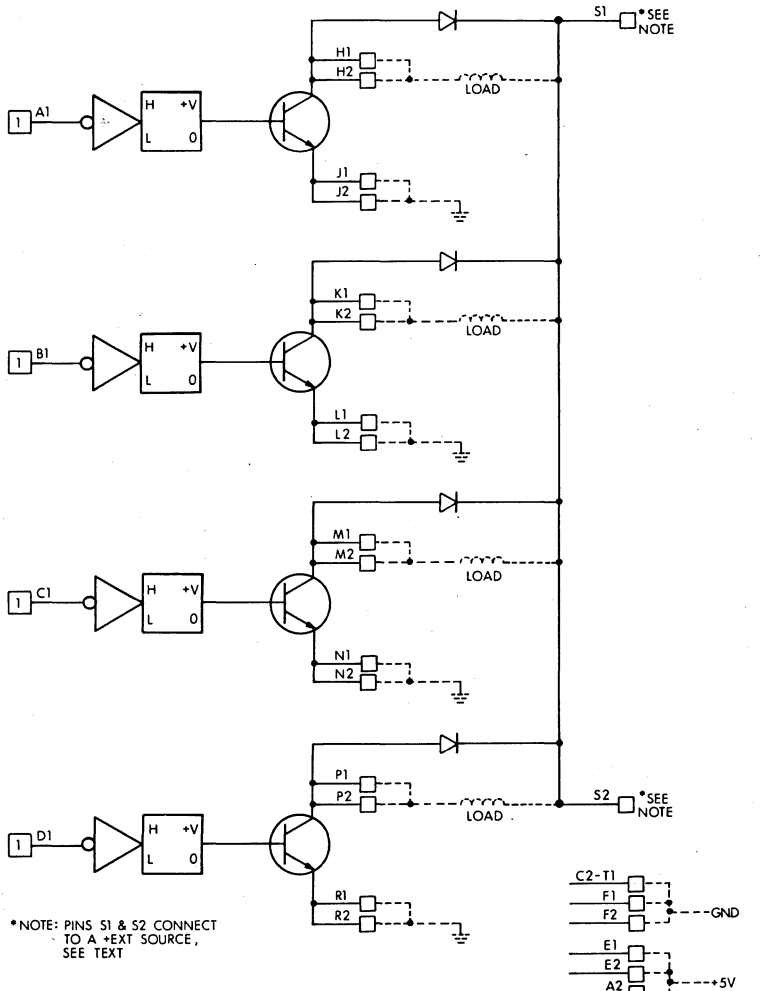
M060
SOLENOID DRIVER

LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single

Price
$55



Volts	Power mA (max.)	Pins
+5	80	A2, E1, E2,
GND		C2, T1, F1, F2,
Text	See Text	S1, S2

The M060 module consists of four identical high-current driver circuits. Each circuit contains an inverting gate that controls an NPN transistor switch. A low level, at any input, will turn on the switch which is capable of driving loads up to 1.2 amps with external power supply voltages of up to +75 V dc.

APPLICATIONS

The M060 module can be used to drive relays, solenoids, and any similar inductive loads requiring current of up to 1.2 amps.

It is not recommended for lamp-driving tasks; for this application, the M050 module should be utilized.

EXTERNAL POWER SUPPLY

An external power supply must be used to power the loads. This supply may be a maximum of 75 V dc. In connecting the power supply, the positive terminal should be connected to pins S1 and S2, and the negative terminal to ground.

One side of the load device must connect to the external supply and the other side to the driver output.

FUNCTIONS

ON Condition: Each switch activates the load device when the circuit is a logic Low, 0. In this condition, the circuit supplies current which is determined by the external power supply voltage and the load impedance must not exceed 1.2 amps.

OFF Condition: When the input is high, the switch is open and a high impedance exists. In this condition, there is a small amount of leakage current flow which is typically less than 100 μA for an external supply voltage of 75 V dc.

CONNECTIONS and PRECAUTIONS

Note that the emitter and collector on each transistor switch, and the external power supply inputs, each have two pin connections. These dual connections are required because of the high current capability of the circuit. In each case, the pins should be tied together as shown by the dotted lines on the diagram. It should also be mentioned that the emitter connections of each transistor switch must tie to ground, preferably at pin C2 of the logic block.

SPECIFICATIONS

Current Capability: 1.2 amps per circuit (max)
External Supply Voltage: 75 V dc (max)
Circuit Delay: 10 μs (typical)—15 μs (max)

M111
INVERTER

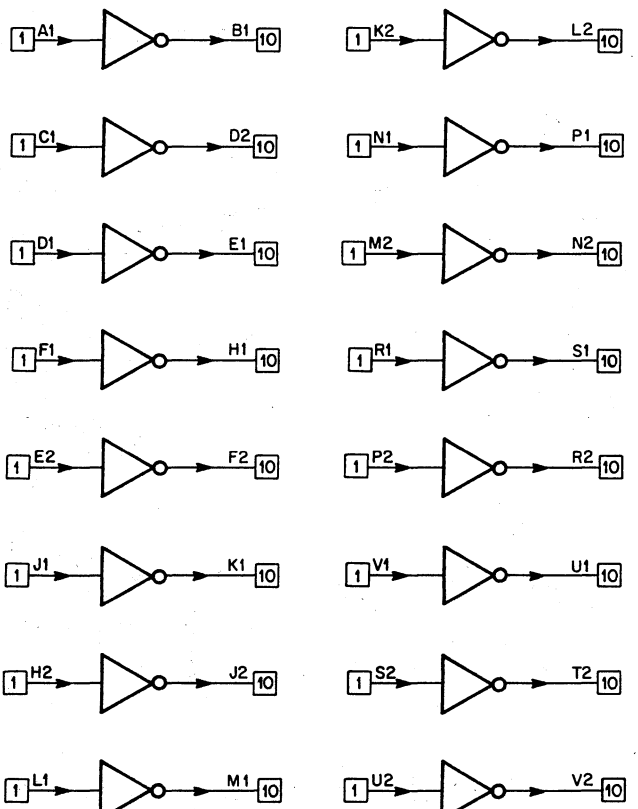
GATES

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$22



Volts	Power mA (max.)	Pins
+5	87	A2
GND		C2, T1

Sixteen Inverters with input/output connections as shown.

APPLICATIONS

- Output Expansion
- Logical Inversion

M112
NOR GATE

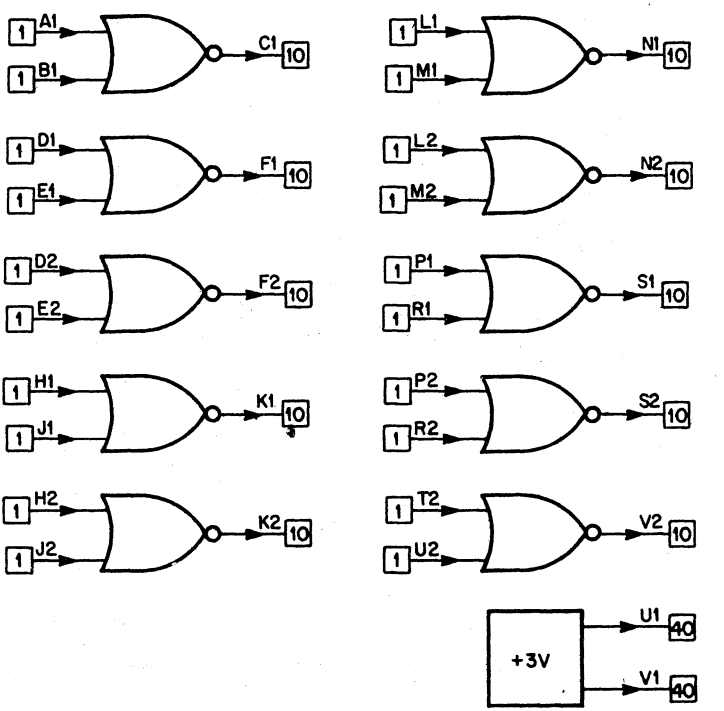
GATES

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$35



Volts	Power mA (max.)	Pins
+5	50	A2
GND		C2, T1

The M112 contains ten positive NOR gates, each performing the function A+B. Pins U1 and V1 provide two separate logic HIGH sources (+3V) each capable of holding up to 40 unused M Series inputs HIGH.

APPLICATIONS

- Logic gating

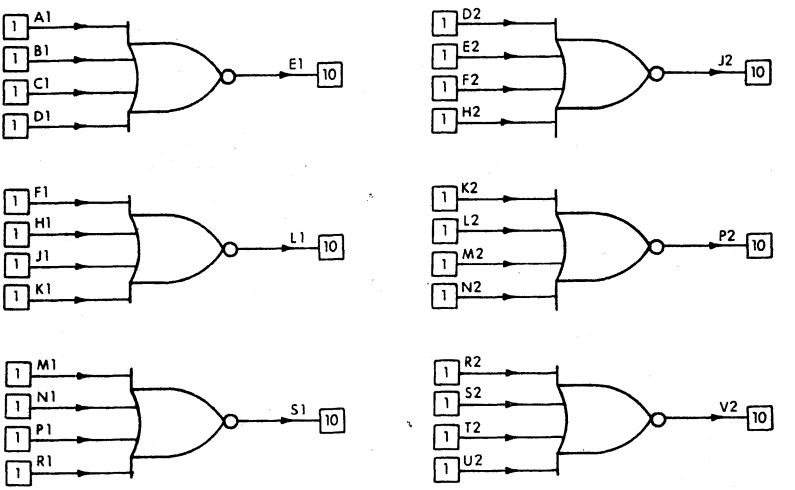
M116
6 4-INPUT NOR GATES

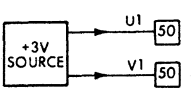
GATES

M SERIES

Length: Standard
Height: Single
Width: Single

Price
$20





Volts	Power mA (max.)	Pins
+5	30	A2
GND		C2, T1

The M116 module consists of six high-speed, 4-input, positive logic NOR gates. Pins U1 and V1 provide two separate logic HIGH sources (+3V), each capable of holding up to 50 unused M Series inputs HIGH.

APPLICATIONS

- Logic gating

SPECIFICATIONS

Maximum propagation delay to a logic HIGH or LOW is 10 ns.

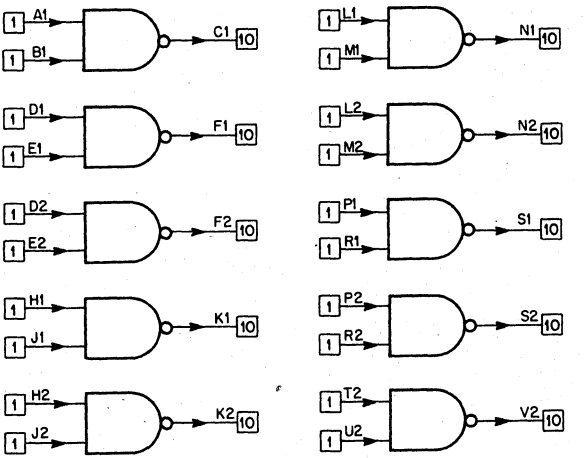
M113, M115, M117, M119
NAND GATES

GATES

M SERIES

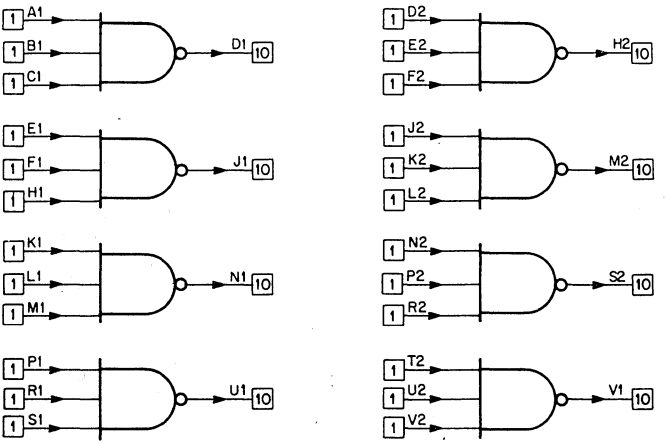
Length: Standard
Height: Single
Width: Single

Price:
M113 — $18
M115 — $18
M117 — $19
M119 — $18

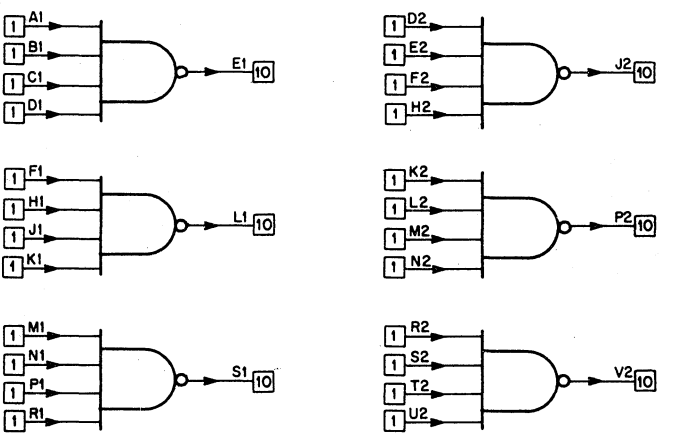


M113 2-INPUT NAND GATES

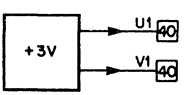
Volts	Power mA (max.)	Pins
+5	71 M113	A2
+5	41 M115	A2
+5	41 M117	A2
+5	19 M119	A2
GND		C2, T1

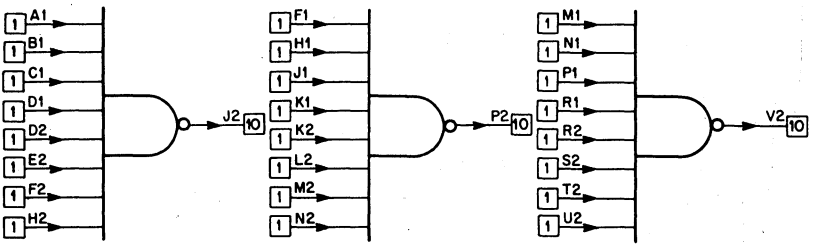


M115 3-INPUT NAND GATES



M117 4-INPUT NAND GATES





M119 8-INPUT NAND GATES

These modules provide general-purpose gating for the M Series, and are most commonly used for decoding, comparison, and control. Each module performs the NAND function ($\overline{\bullet B \bullet C \bullet \text{——} N}$), depending upon the number of inputs.

APPLICATIONS

- Logic gating

FUNCTIONS

M113—Ten two-input NAND gates that also may be used as inverters.
M115—Eight, three-input NAND gates.
M117—Six, four-input NAND gates.
M119—Three, eight-input NAND gates.

Unused inputs on any gate must be returned to a source of logic HIGH, for maximum noise immunity. In the M113, M117, M119, M121, M617 and M627 modules, two pins are provided (U1 and V1) as source of +3 volts for this purpose. Each pin can supply up to 40 unit loads. M103, M111 and M002 provide additional sources of logic HIGH level.

SPECIFICATIONS

Typical propagation delay of M Series gates is 15 ns.

M121
AND/NOR GATE

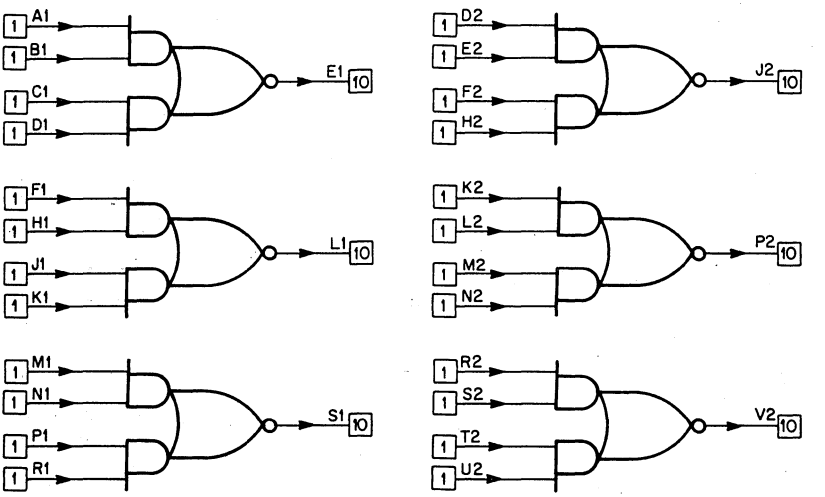
GATES

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$23



Volts	Power mA (max.)	Pins
+5	50	A2
GND		C2, T1

The M121 module contains six AND/NOR gates which perform the function $\overline{(A \cdot B + C \cdot D)}$. By proper connection of signals to the AND inputs, the exclusive OR, coincidence, and NOR functions can be performed.

APPLICATIONS

- Logic Gating

SPECIFICATIONS

Propagation Delay: Typically 15 ns

M133
TWO-INPUT NAND GATES

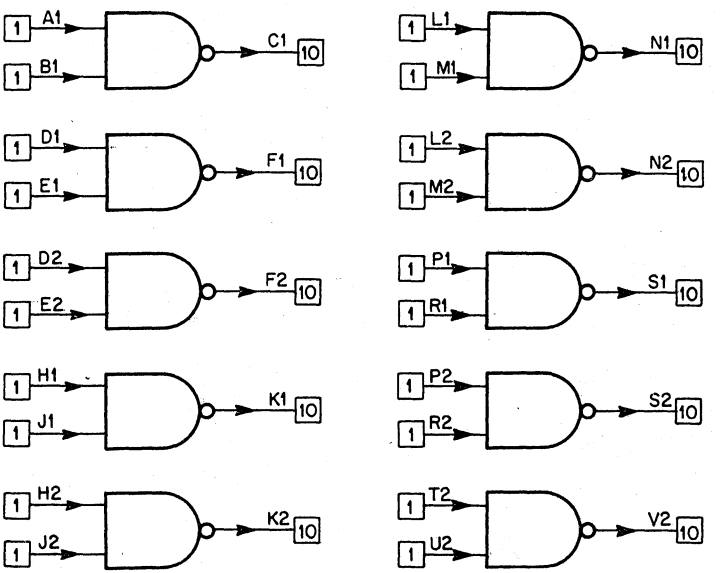
GATES

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$27



Volts	Power mA (max.)	Pins
+5	160	A2
GND		C2, T1

This module provides general-purpose high-speed NAND gating.

APPLICATIONS

The high-speed characteristic of these gates frequently will solve tight timing problems in complex systems.

SPECIFICATIONS

Maximum output propagation delay to a logic HIGH or LOW is 10 ns.

Unused inputs on any gate must be returned to a source of logic HIGH for maximum speed and noise immunity.

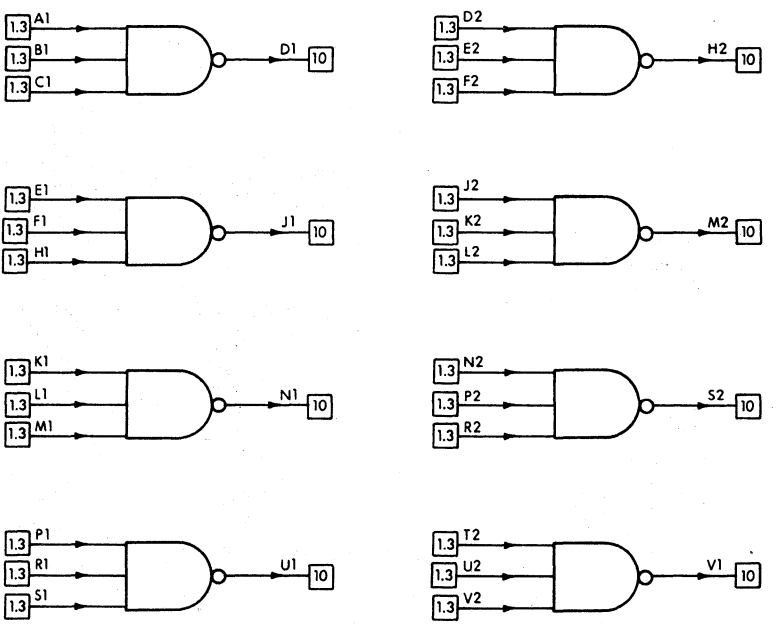
M135
8 3-INPUT NAND GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single

Price
$32



Volts	Power mA (max.)	Pins
+5	100	A2
GND		C2, T1

The M135 module consists of eight high-speed, 3-input, positive logic NAND gates. It is pin-compatible with the M115 module.

APPLICATIONS

- Logic gating

SPECIFICATIONS

Maximum propagation delay to a logic HIGH or LOW is 10 ns.

NOTE: All unused inputs must be returned to a source of logic HIGH for maximum noise immunity.

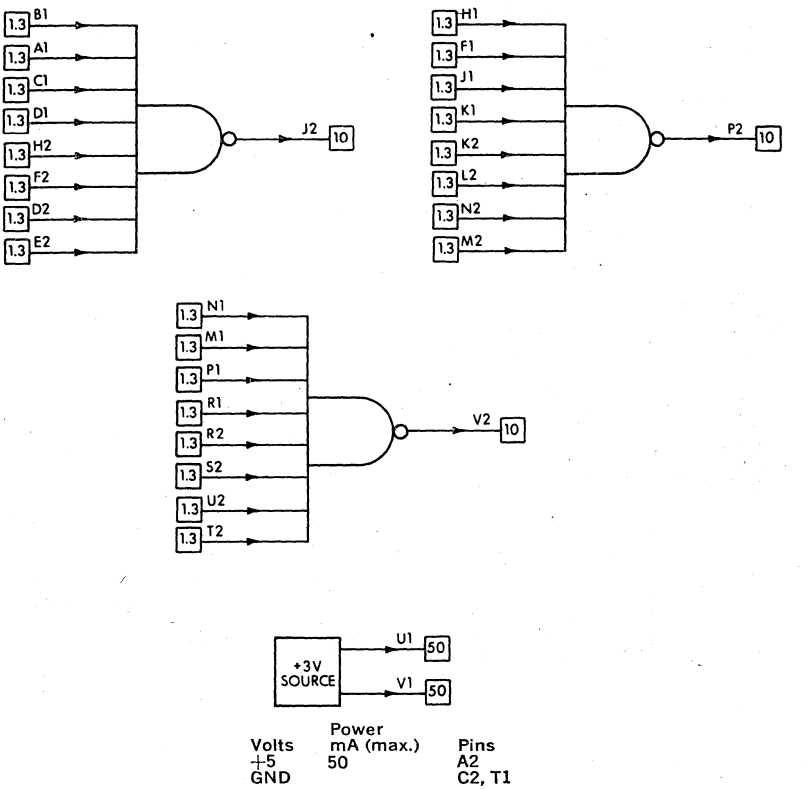
M139
3 8-INPUT NAND GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single

Price
$28



Volts	Power mA (max.)	Pins
+5	50	A2
GND		C2, T1

The M139 module consists of three high-speed, 8-input, positive logic NAND gates. Pins U1 and V1 provide two separate logic HIGH sources (+3 V,) each capable of holding up to 50 unused M Series inputs HIGH.

APPLICATIONS

- Logic gating

SPECIFICATIONS

Maximum propagation delay to a logic HIGH or LOW is 10 ns.

NOTE: All unused inputs must be returned to a source of logic HIGH for maximum noise immunity.

M141
NAND/OR GATES

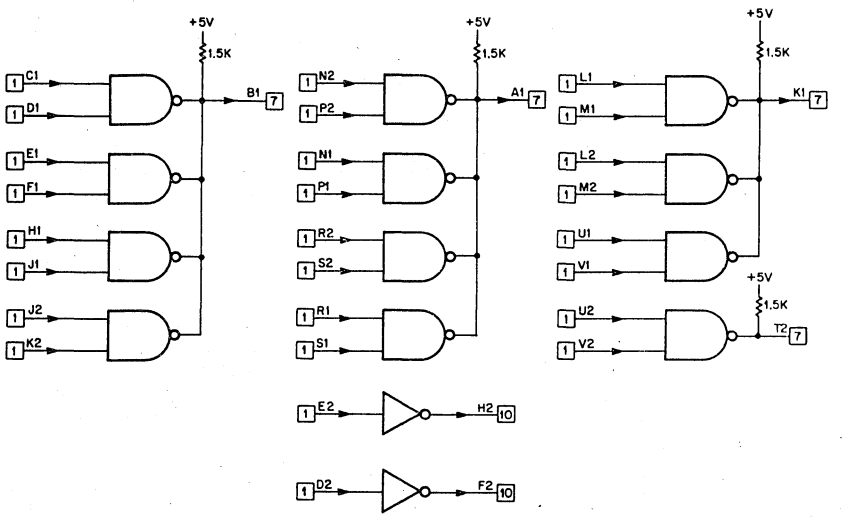
GATES

M SERIES

Length: Standard
Height: Single
Width: Single

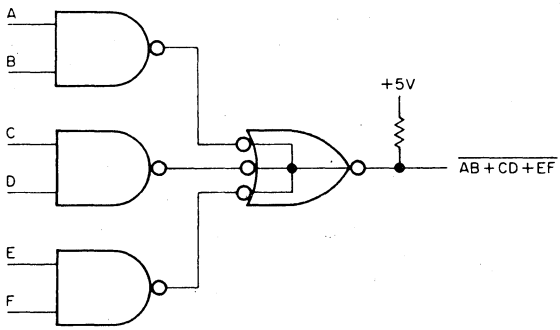
Price:

$29



Volts	Power mA (max.)	Pins
+5	117	A2
GND		C2, T1

This module provides NAND/OR gates arranged in four groups consisting of 4, 4, 3, and 1 two-input NAND gates respectively. The outputs in each group are connected together to provide a wired OR for low levels. The function of these gates can be shown as:



By using one of the two inverters provided, a true AND/OR function can be realized. A maximum of four groups of gates can be connected together. Connection is made by merely connecting output pins together.

APPLICATIONS

- Logic Gating

FUNCTIONS

The M141 NAND/OR gate performs two levels of logic. The first is the NAND function which is identical to the M113 NAND gate. The second level is that of a wired OR for low logic levels. The two-input NAND gate which is used in the M141 does not have the standard TTL output circuit, but only the lower half of the totem pole output. This allows the outputs of these gates to be connected together and to share a common pull-up resistor.

SPECIFICATIONS

Propagation Delay: 70 ns max.

Loading: The load resistor of each output presents 2 unit loads when connected to another output. For example, when four groups are connected together, 3 groups present two unit loads each to the fourth group, totalling 6 unit loads. This leaves 1 unit load capability.

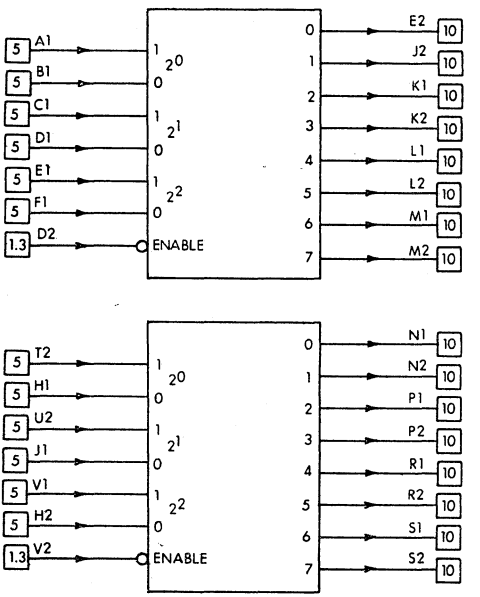
M152
DUAL 1-of-8 DECODER

NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single

Price
$36



Volts	Power mA (max.)	Pins
+5	265	A2
GND		C2, T1

The M152 module consists of two identical binary-to-octal decoders. Each requires complementary inputs.

With the addition of a simple inverter circuit, the module may be used as a single 1-of-16 decoder using the ENABLE lines as the highest order address lines.

The outputs are asserted HIGH when selected.

APPLICATIONS

The module may be used for applications such as memory address decoding.

The module may also be used as a demultiplexer by supplying the data at the ENABLE input at the same frequency as a control clock, and generating the binary address 0 through 7 from the control clock and applying these addresses to the address pins of the decoder. The data is routed to output 0 through 7.

SPECIFICATIONS

Propagation Delay

From:	To:
Any Data Input	Any Output = 12 ns (max)
Either ENABLE Input	Any Output = 24 ns (max)

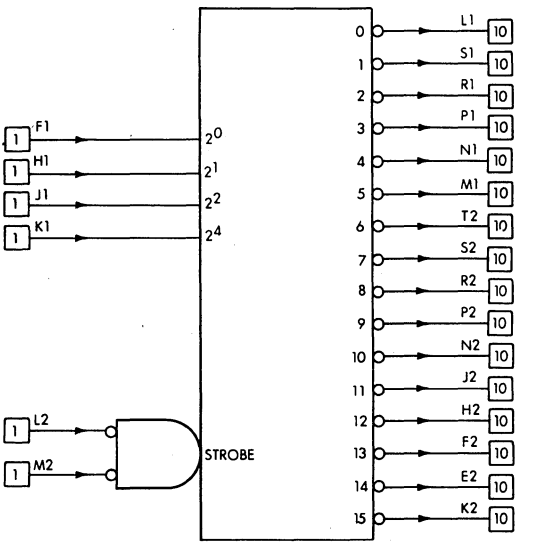
M155
4-LINE TO 16-LINE DECODER

NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single

Price
$30



Volts	Power mA (max.)	Pins
+5	55	A2
GND		C2, T1

The M155 module decodes four binary-coded inputs into one of sixteen mutually exclusive outputs when both STROBE inputs, L2 and M2, are Low. The demultiplexing function is performed by using the four input lines to address the output line, passing data from one of the STROBE inputs with the other STROBE input LOW. When either STROBE input is HIGH, all outputs are HIGH. Refer to the Truth Table.

SPECIFICATIONS
Propagation Delay

From:	To:
Data Inputs	HIGH or LOW Output = 36 ns (max)
Either STROBE Input	HIGH or LOW Output = 30 ns (max)

TRUTH TABLE

INPUTS						OUTPUTS															
L2	M2	K1	J1	H1	F1	L1	S1	R1	P1	N1	M1	T2	S2	R2	P2	N2	J2	H2	F2	E2	K2
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	L	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High, L = Low, X = irrelevant

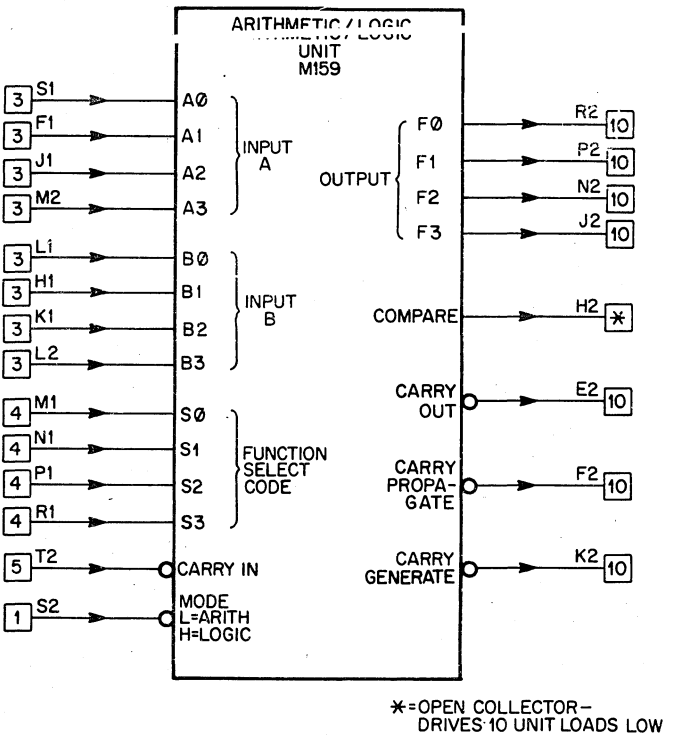
M159
ARITHMETIC/LOGIC UNIT

NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single

Price:
$35



Volts	Power mA (max.)	Pins
+5	150	A2
GND		C2, T1

The M159 can perform 16 word-oriented arithmetic operations and 16 bit oriented logic functions. Arithmetic operations are performed on two 4-bit input words and an input carry to produce one 4-bit output word and a carry out. In the logic mode the M159 looks like four 2-input functional gates. Where N indicates one out of four, the output F_N depends only on the inputs A_N, B_N, and the logic function code selected.

The M159 is fully cascadable. The CARRY OUT of the less significant M159 should be connected directly to the CARRY IN of the next more significant M159. The CARRY PROPAGATE and CARRY GENERATE output should be used with a carry look-ahead module or left unconnected.

The COMPARE output goes High whenever all the "F" outputs go High. This output is open-collector so that it can be wire-AND connected when M159 modules are cascaded. An example of how this output can be used is shown in the table below.

When the arithmetic operation A minus B minus 1 is selected, the M159 can be used as a comparator.

A and B Data Inputs	COMPARE Output	CARRY OUT
$A > B$	0	0
$A = B$	1	1
$A < B$	0	1

The maximum propagation delay from the "A_N" or "B_N" bit input to the output bit "F_N" in the logic mode is 48 nsec. which does not change as M159's are cascaded. In the arithmetic mode, the maximum delay from the "A" or "B" word input to the "F" word output, CARRY OUT, or COMPARE is 50 nsec. which increases by 19 nsec. per additional cascaded M159 when carry look-ahead is not used. When carry look-ahead is used, the maximum additional delay is limited to 20 nsec. for up to three additional M159's.

Table of Logic Mode Operations

(MODE Input = 1)

(CARRY IN has no affect on Logic Mode Operations)

Function SELECTION CODE				**NOTE** that F_N is complemented when the Function Selection Code is complemented		Complemented Function SELECTION CODE			
S3	S2	S1	S0	Bit F_N Equals	Bit F_N Equals	S3	S2	S1	S0
0	0	0	0	$\overline{A}_N$	A_N	1	1	1	1
0	0	0	1	$\overline{A}_N$ AND $\overline{B}_N$	A_N OR B_N	1	1	1	0
0	0	1	0	$\overline{A}_N$ AND B_N	A_N OR $\overline{B}_N$	1	1	0	1
0	0	1	1	0	1	1	1	0	0
0	1	0	0	$\overline{A}_N$ OR $\overline{B}_N$	A_N AND B_N	1	0	1	1
0	1	0	1	$\overline{B}_N$	B_N	1	0	1	0
0	1	1	0	(A_N AND $\overline{B}_N$) OR ($\overline{A}_N$ AND B_N)	(A_N AND B_N) OR ($\overline{A}_N$ AND $\overline{B}_N$)	1	0	0	1
0	1	1	1	A_N AND $\overline{B}_N$	$\overline{A}_N$ OR B_N	1	0	0	0

Table of Most Useful Arithmetic Mode Operations

(MODE Input =0)

Function				Word F Equals	
SELECTION CODE				CARRY IN = 1	CARRY IN = 0
S3	S2	S1	S0		
0	0	0	0	WORD A	WORD A plus 1
0	0	0	1		
0	0	1	0		
0	0	1	1	Minus 1 (2's Comp.)	ZERO
0	1	0	0		
0	1	0	1		
0	1	1	0	A Minus B Minus 1	A Minus B
0	1	1	1		
1	0	0	0		
1	0	0	1	A plus B	A plus B plus 1
1	0	1	0		
1	0	1	1		
1	1	0	0	A Times 2	A Times 2 plus 1
1	1	0	1		
1	1	1	0		
1	1	1	1	A Minus 1	A

Table of Less Useful Arithmetic Mode Operations

(MODE Input = 0)

Function				Word F Equals	
SELECTION CODE				CARRY IN = 1	CARRY IN = 0
S3	S2	S1	S0		
0	0	0	0		
0	0	0	1	A OR B	A OR B plus 1
0	0	1	0	A OR $\overline{B}$	A OR $\overline{B}$ plus 1
0	0	1	1		
0	1	0	0	A plus (A AND $\overline{B}$)	A plus (A AND B) plus 1
0	1	0	1	(A OR B) plus (A AND $\overline{B}$)	(A OR B) plus (A AND B) plus 1
0	1	1	0		
0	1	1	1	(A AND $\overline{B}$) minus 1	A AND B
1	0	0	0	A plus (A AND B)	A plus (A AND B) plus 1
1	0	0	1		
1	0	1	0	(A OR $\overline{B}$) plus (A AND B)	(A OR B) plus (A AND B) plus 1
1	0	1	1	(A AND B) minus 1	A AND B
1	1	0	0		
1	1	0	1	(A OR B) plus A	(A OR B) plus A plus 1
1	1	1	0	(A OR $\overline{B}$) plus A	(A OR B) plus A plus 1
1	1	1	1		

M160
AND/NOR GATE

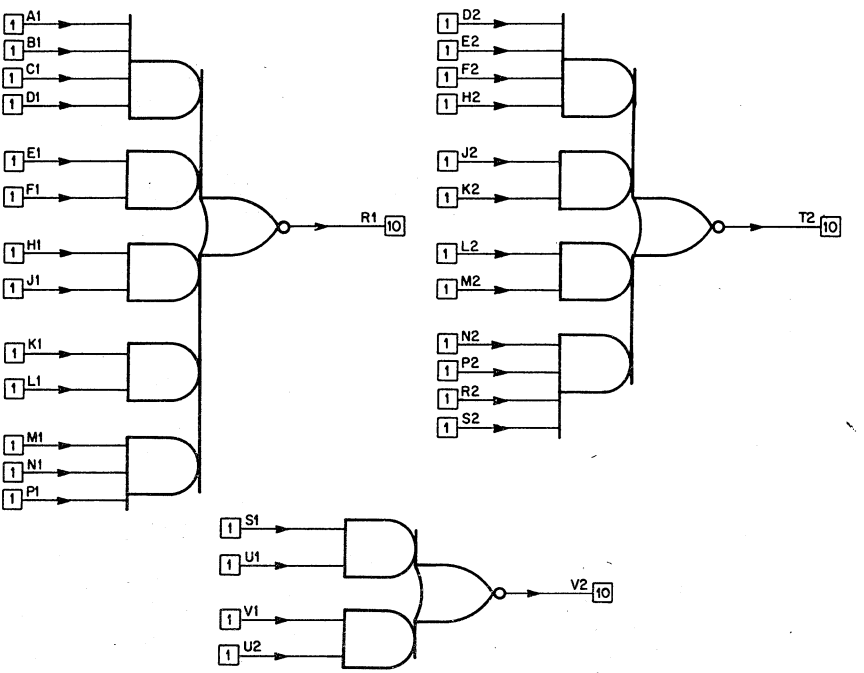
GATES

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$33



Volts	Power mA (max.)	Pins
+5	30	A2
GND		C2, T1

The M160 module contains three general-purpose AND/NOR gates which perform functions similar to those of the M121.

APPLICATIONS
These gates can be used to select and place on a single output any of several input signals.

SPECIFICATIONS
Typical propagation delay of an M160 gate is 20 ns.

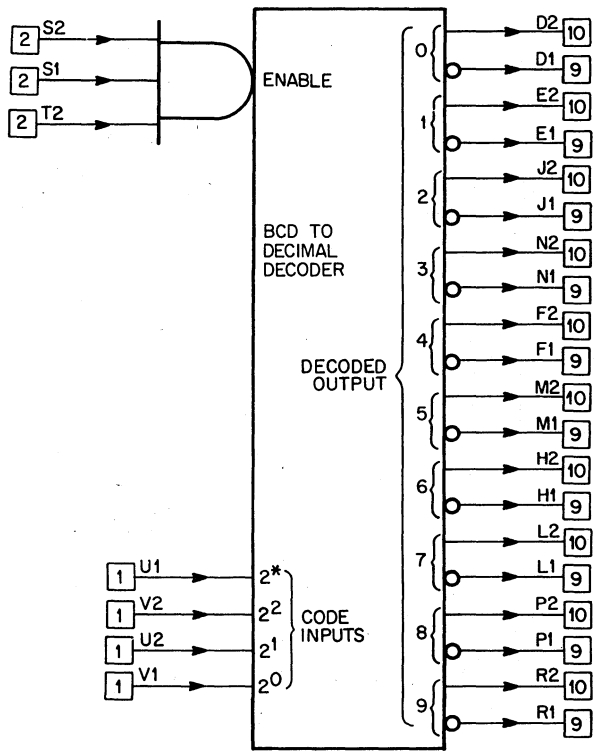
M161
BINARY TO OCTAL/DECIMAL DECODER

NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single

Price:
$55



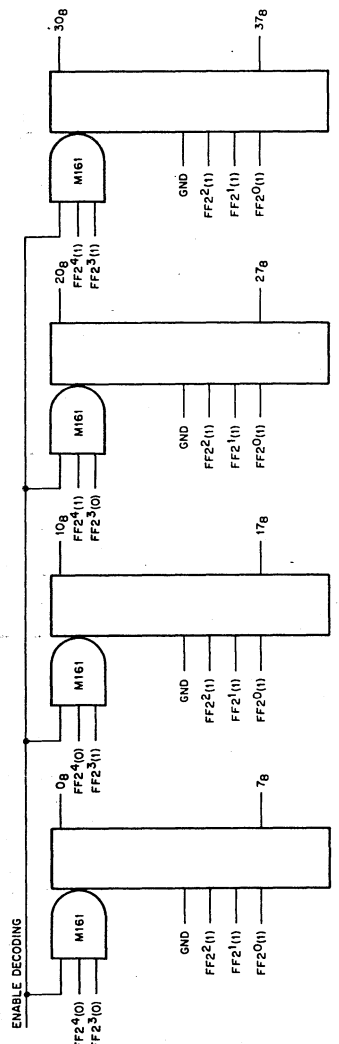
Volts	Power mA (max.)	Pins
+5	120	A2
GND		C2, T1

The M161 is a functional decoding module which can be used as a binary-to-octal or binary-coded decimal (8421 or 2421 codes) to decimal decoder. In the binary-to-octal configuration, up to eight M161's can be linked together to provide decoding of up to six bits. Three ENABLE inputs are provided for selective enabling of modules in decoders of more than one digit. In the octal mode, the bit 2* input is connected to ground, which automatically inhibits the 8 and 9 outputs. Connections for a 5-bit binary/octal decoder (4 modules) are shown below. The figure assumes that the inputs to the decoder

are the outputs of flip-flops such as FF2° (1), 1 output side; and FF2° (0), 0 output side.

The 2* input may be of decimal value 2, 4, 6, 8 as long as illegal combinations are inhibited before connections to the inputs, and the 4-2-1 part of the code is in binary.

The propagation delay through the decoder is typically 55 nsec in the binary-to-octal mode, and 75 nsec in the BCD-to-decimal mode. The maximum delay in the BCD-to-decimal mode is 120 nsec, frequency-limiting this module to 8HMz when used in this fashion. The enable inputs can be used to strobe output data providing inputs 2° — 2* have settled at least 50 nsec prior to the input pulse.



5-BIT BINARY/OCTAL DECODER

M162
PARITY CIRCUIT

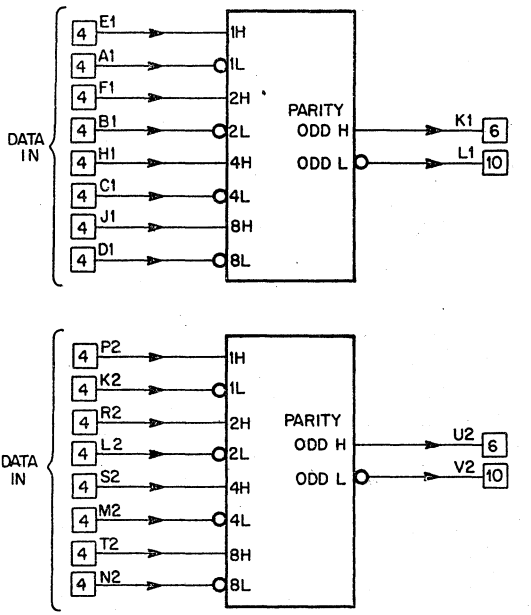
NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$63



Volts	Power mA (max.)	Pins
+5	102	A2
GND		C2, T1

The M162 contains two parity detector circuits. Each circuit indicates whether the binary data presented to it contains an ODD or EVEN number of ONES. The data and its complement are required as shown.

APPLICATIONS

- Parity checking

FUNCTIONS

Indication of ODD PARITY is given by a HIGH level at pins K1 and U2 respectively. Pins L1 and V2, when HIGH, indicate EVEN PARITY or no input.

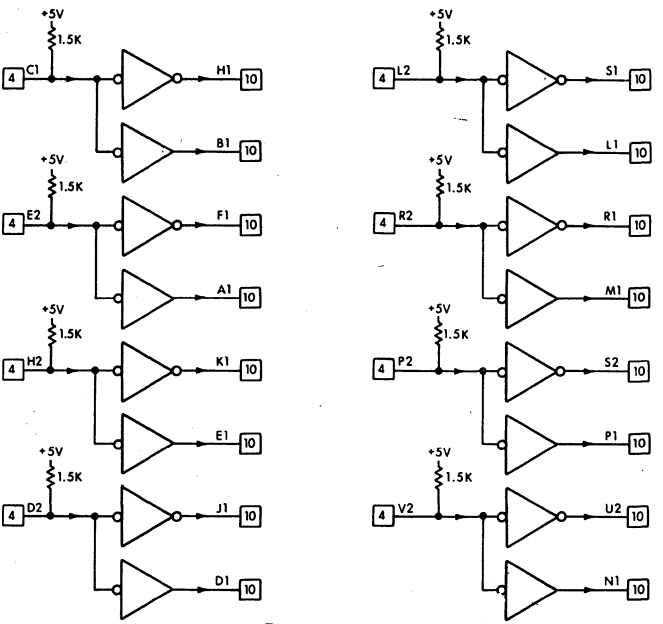
M165
8 BUFFERS

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single

Price
$30



Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, F2, J2, K2, M2, N2, T1, T2

The M165 module is designed for use with circuits having open-collector output stages. The module provides a pull-up resistor for the open-collector stage and buffers the output through an inverting gate and a noninverting gate.

There are eight similar circuits on the M165 module. The value of the pull-up resistor on each input allows open-collector outputs which can sink at least 10 mA, and have a total leakage not exceeding 1.3 mA, to drive the M165 module, plus one other high-speed TTL load.

SPECIFICATIONS
Propagation Delay

From:	To:
Input	Inverting Output, HIGH or LOW = 10 ns (max)
Input	Noninverting Output, HIGH or LOW = 15 ns (max)

M168
12-BIT MAGNITUDE COMPARATOR

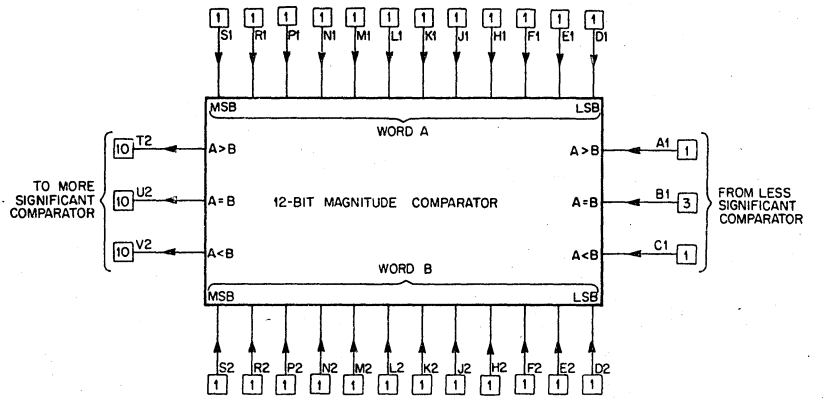
NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$45



Volts	Power mA (max.)	Pins
+5	250	A2
GND		C2, T1

The M168 12-Bit Magnitude Comparator performs magnitude comparison of two 12-bit words. When the comparison inputs are not connected to the comparison outputs of another M168, the "A=B" input must be connected to a logical "1". The A>B and A<B inputs may individually be made a logic "1" or logic "0". However, connecting both these inputs to GND, a logic "0" is recommended.

The M168 Comparator may be cascaded to compare longer words. The outputs T2, U2, and V2 should be connected to the corresponding inputs of the next comparator which are A1, B1, and C1 respectively. The inputs of the first comparator must all be made a logical "1".

The propagation delay time from Data (A and B) to outputs is 48 nsec typical and 72 nsec maximum for one unit.

When cascading the total typical time is 48 nsec plus 36 nsec per additional unit. The total maximum time is 72 nsec plus 54 nsec per additional unit.

INPUTS				OUTPUTS		
A > B	A = B	A < B	Data	A > B	A = B	A < B
1	0	0	A > B	1	0	0
1	0	0	A = B	1	0	0
1	0	0	A < B	0	0	1
1 or 0	1	1 or 0	A > B	1	0	0
1 or 0	1	1 or 0	A = B	0	1	0
1 or 0	1	1 or 0	A < B	0	0	1
0	0	1	A > B	1	0	0
0	0	1	A = B	0	0	1
0	0	1	A < B	0	0	1

M169
GATING MODULE

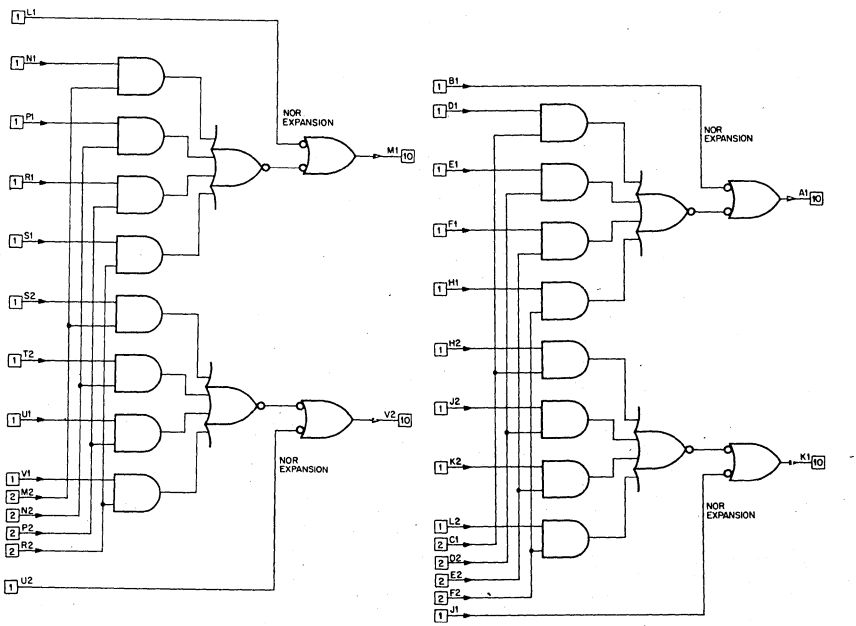
GATING

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$33



Volts	Power mA (max.)	Pins
+5	50	A2
GND		C2, T1

The M169 contains groups of 4-input AND/NOR gates prewired as four stages of a 4-input, 1-output multiplexer or similar gating function.

APPLICATIONS

- Multiplexers
- Register Select and Bussing

FUNCTIONS

Raising a DATA INPUT to a HIGH and selecting a corresponding INPUT ENABLE line generates a HIGH at the appropriate ENABLED OUTPUT, A1, K1, M1 or V2. Any of the ENABLED OUTPUTS may be enabled directly through an M121 or M160 AND/NOR gate, used as a NOR Expander.

SPECIFICATIONS

Maximum input to output propagation delay for any circuit is 45 ns.

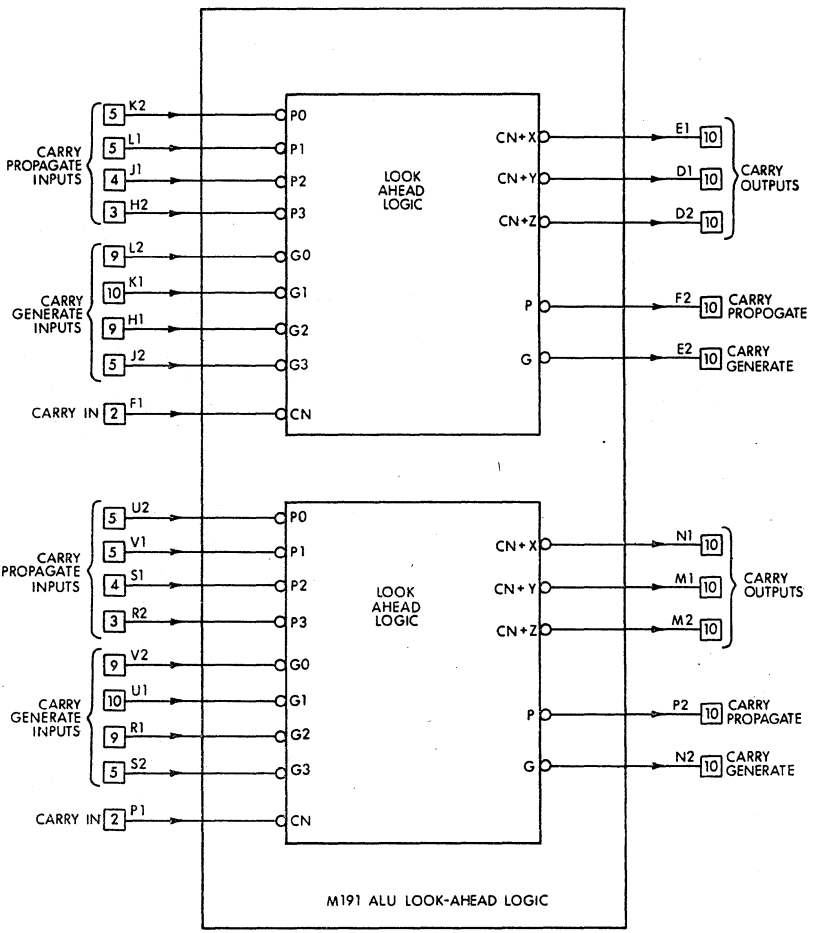
M191
ALU LOOK-AHEAD LOGIC

NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single

Price
$22



Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, T1

The M191 contains two high-speed look-ahead units to be used to reduce the propagation delay of cascaded M159 Arithmetic Logic Units for Arithmetic Mode operations. The propagation delay is the maximum delay time from "A" to "B" word input to the "F" word output or COMPARE output. This time is 50 ns for one ALU and increases by 19 ns for each additional cascaded ALU without use of the M191. This increase is due to the 19-ns delay from 'A" or "B" word input to the first CARRY OUT and the added 19-ns delays to each succeeding CARRY OUT. However, when a look-ahead CARRY OUTPUT is substituted for an ALU CARRY OUTPUT, this time increase is only 7 ns per additional ALU. These advanced look-ahead CARRY OUTPUTS are determined by the states of the CARRY GENERATE, CARRY PROPAGATE and CARRY IN inputs.

APPLICATIONS

Figures 1 and 2 illustrate use of the module for up to 16-bit and 32-bit applications respectively.

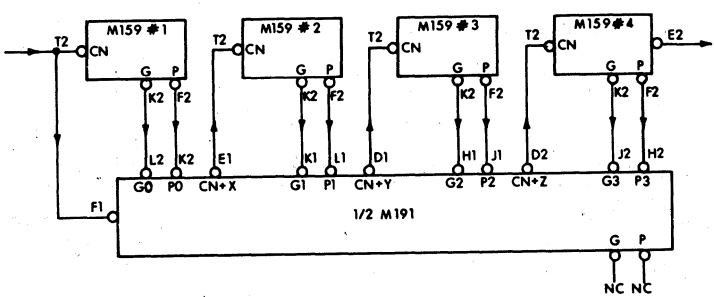


Figure 1. 16-Bit Application of M191 with M159.

NOTES:

1. Propagation Delay Time = 50 ns + 7 ns + 7 ns + 7 ns = 71 ns
2. CN+4 of most significant M159 (#4) becomes final CARRY OUT
3. For 12-bit application, M159 #4 not used; for 8-bit application, M159 #3 and #4 not used.

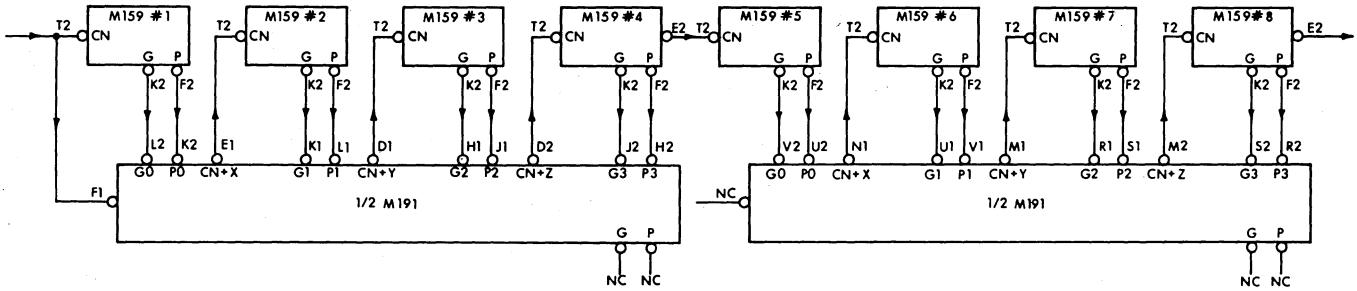


Figure 2. 32-Bit Application of M191 with M159.

NOTES:
1. Propagation Delay Time = 50 ns + 7 ns + 7 ns + 7 ns + 19 ns + 7 ns + 7 ns + 7 ns = 110 ns
2. CN+4 of most significant M159 (#8) becomes final CARRY OUT
3. For 28-bit application, M159 #8 not used; for 24-bit application, M159 #8 and #7 not used, etc.

M202
TRIPLE J-K FLIP-FLOP

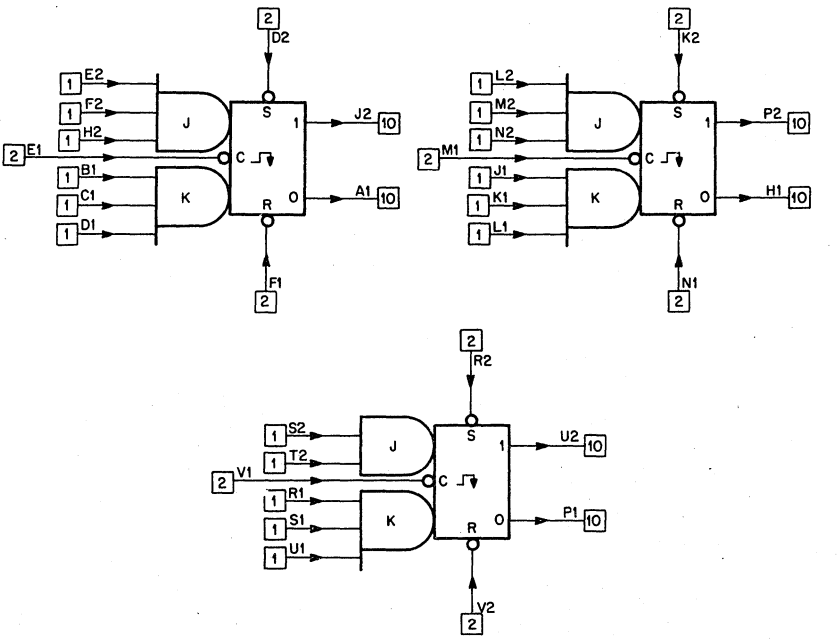
FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$29



Volts	Power mA (max.)	Pins
+5	57	A2
GND		C2, T1

The M202 contains three J-K flip-flops augmented by multiple-input AND gates.

APPLICATIONS

- For general use as gated control flip-flops or buffers.

FUNCTIONS

See M207 for detailed description of logical operation. The J-K flip-flops used in this module are identical to flip-flops used in the M207 except on the M202 clock inputs, J-K inputs, direct clear, direct set and both output lines for each flip-flop are independent.

PRECAUTION

Set and clear lines should be tied to "1" level when not used.

M203
8 R/S FLIP-FLOPS

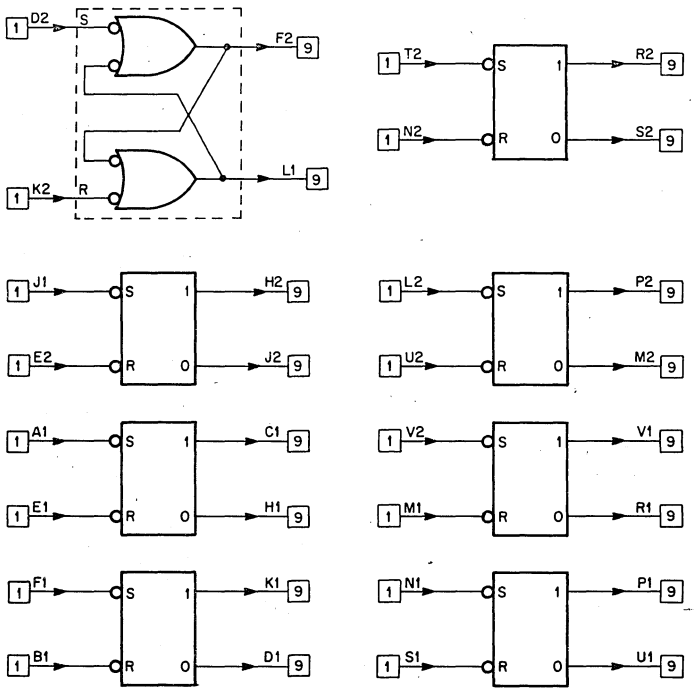
FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$26



Volts	Power mA (max.)	Pins
+5	55	A2
GND		C2, T1

The M203 is made up of 8 R/S-type flip-flops. Each flip-flop is made up of two 2-input NAND gates with cross-coupled outputs.

APPLICATIONS

- R/S flip-flops provide an inexpensive method of storage.

PRECAUTIONS

Care must be taken not to place the SET and RESET inputs LOW at the same time. The last of the inputs to go HIGH will determine the final state of the flip-flop.

SPECIFICATIONS

The propagation delay of the M203 is approximately 30 ns.

M204
GENERAL-PURPOSE BUFFER AND COUNTER

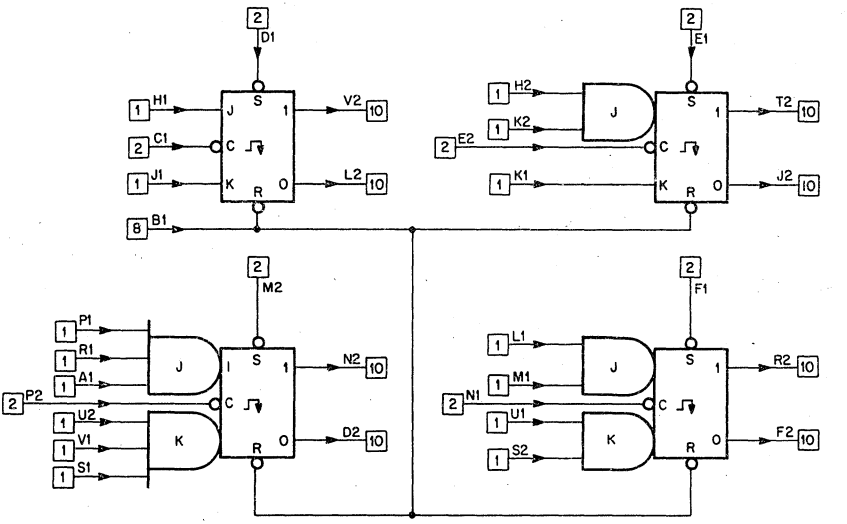
FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$34



Volts	Power mA (max.)	Pins
+5	74	A2
GND		C2, T1

The M204 contains four J-K type flip-flops, augmented by multiple-input AND gates. The gating scheme permits the formation of counters of most moduli up to 16, by simple connector wiring. Clock, present, and input lines for each flip-flop are independent. A common CLEAR input is provided.

APPLICATIONS

- For general use as gated control flip-flops or buffers
- Counters
- Shift Registers

FUNCTIONS

Input information is transferred to the outputs when the threshold point is reached on the trailing (negative going voltage) edge of the clock pulse.

Logical operation of the J-K flip-flops used in this module is identical to the M207 (described in detail) except for the addition of preset inputs to the M204.

M205
GENERAL-PURPOSE FLIP-FLOPS

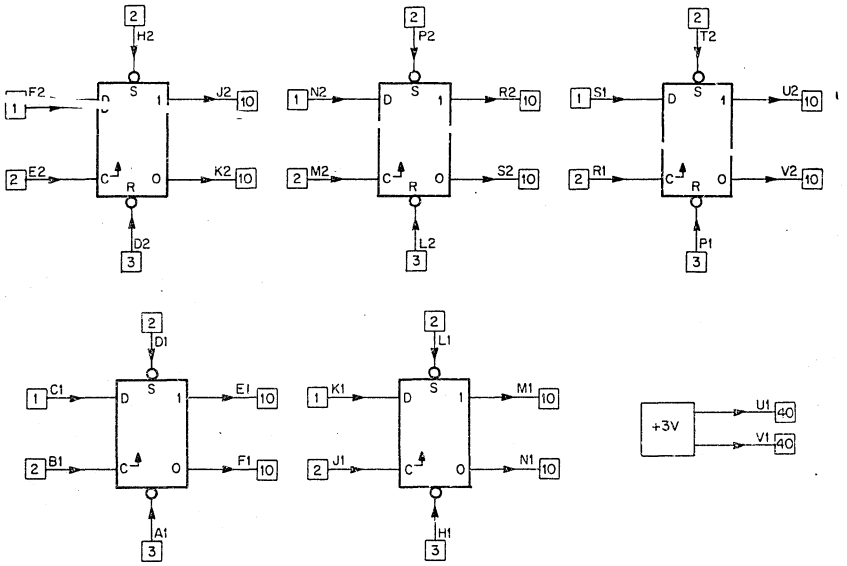
FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$33



Volts	Power mA (max.)	Pins
+5	90	A2
GND		C2, T1

The M205 contains five separate D-Type flip-flops. Each flip-flop has independent gated data, clock, dc set, and dc reset inputs.

APPLICATIONS

- Storage Registers
- Counters and Shift Registers
- Flags and Control Storage

FUNCTIONS

For each flip-flop, information present on the D input is transferred to the output when the threshold is reached on the leading (positive going voltage) edge of the clock pulse.

SPECIFICATIONS

Information must be present on the D input 20 ns (max) prior to a standard clock pulse and should remain at the input at least 5 ns (max) after the clock pulse leading edge has passed the threshold voltage. Data transferred into the flip-flop will be stable at the output within 50 ns, maximum. Typical width requirement for the clock, dc reset and dc set pulses is 30 nsec each.

M206
GENERAL-PURPOSE FLIP-FLOPS

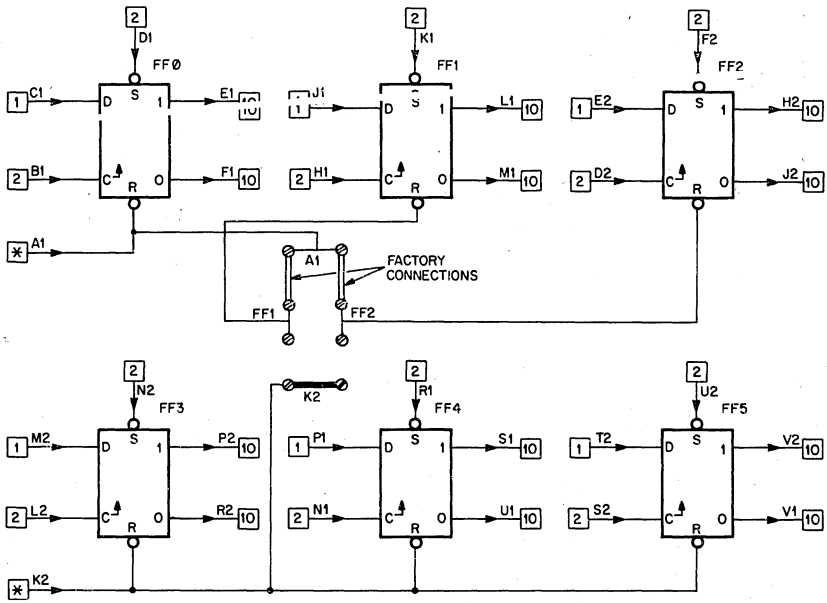
FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$30



Volts	Power mA (max.)	Pins
+5	87	A2
GND		C2, T1

The M206 contains six separate D-Type flip-flops. Each flip-flop has independent gated data, clock, and dc set inputs.

APPLICATIONS

- Registers
- Counters and Shift Registers
- Flags and Control Storage

FUNCTIONS

For each flip-flop, information present on the D input is transferred to the output when the threshold is reached on the leading (positive going voltage) edge of the clock pulse.

Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flip-flops. All M206 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows.

CONFIGURATION	CLEAR 1 (A1)	CLEAR 2 (K2)	DELETE JUMPER	ADD JUMPER
3-3	FF0, 1, & 2	FF3, 4, & 5		
4-2	FF0 & 1	FF2, 3, 4, & 5	A1 to FF1	K2 to FF1
5-1	FF0	FF1, 2, 3, 4, & 5	A1 to FF2 A1 to FF1	K2 to FF2 K2 to FF1

A common CLEAR for all six flip-flops can be obtained by wiring pins A1 and K2 together externally.

PRECAUTION

Any unused SET or RESET input should be connected to a logic HIGH source.

Note that the loading of each CLEAR line is calculated on the basis of 3 unit loads per flip-flop. For example, the 4-2 configuration results in 12 unit loads at input K2 and 6 unit loads at input A1.

SPECIFICATIONS

Information must be present on the D input 20 ns (min) prior to a standard clock pulse and should remain at the input at least 5 ns (min) after the clock pulse leading edge has passed the threshold voltage. Data transferred into the flip-flop will be stable at the output within 50 ns, maximum. Typical width requirement for the clock, dc reset and dc set pulses is 30 nsec each.

M207
GENERAL-PURPOSE FLIP-FLOPS

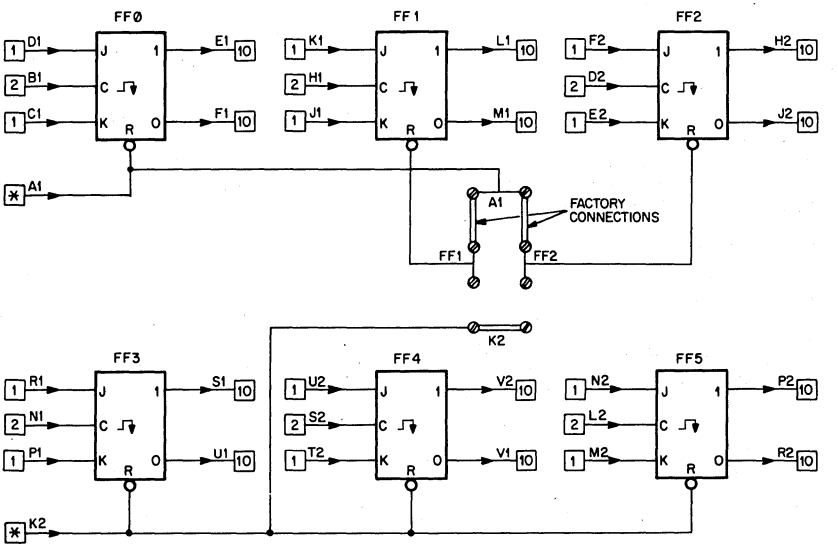
FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$33



*=2 UNIT LOADS PER FLIP-FLOP

Volts	Power mA (max.)	Pins
+5	96	A2
GND		C2, T1

The M207 contains six general-purpose J-K type flip-flops.

APPLICATIONS

- Buffers
- Control Flip-Flops
- Shift Registers
- Counters

FUNCTIONS

A truth table for clock set and reset conditions appears below. Note that when the J and K inputs are both HIGH, the flip-flop complements on each clock pulse.

STARTING CONDITION (OUTPUT)		INPUT CONDITION		RESULT AT END OF STANDARD CLOCK PULSE (OUTPUT)	
1	0	J	K	1	0
L	H	L	L	No change	
		L	H	No change	
		H	L	H	L
		H	H	H	L
H	L	L	L	No change	
		L	H	L	H
		H	L	No change	
		H	H	L	H

Two CLEAR inputs are provided, with jumper terminals for optional clearing in groups of 3 and 3 (standard), 4 and 2, 5 and 1, or 6 and 0. Provision is made on the printed circuit board for changing the configuration of the two CLEAR lines to the flop-flop. All M207 modules are supplied with the 3-3 configuration, but the grouping can be changed as follows:

CON-FIGURATION	CLEAR 1 (A1)	CLEAR 2 (K2)	DELETE JUMPER	ADD JUMPER
3-3	FF0, 1, & 2	FF3, 4, & 5		
4-2	FF0 & 1	FF2, 3, 4, & 5	A1 to FF1	K2 to FF1
5-1	FF0	FF1, 2, 3, 4, & 5	A1 to FF2 A1 to FF1	K2 to FF2 K2 to FF1

SPECIFICATIONS

J and K inputs must be stable during the leading-edge threshold of a standard CLOCK input and must remain stable during the positive state of the CLOCK. Data transferred into the flip-flop will be stable at the output within 30 ns (typical) of the CLOCK pulse trailing edge threshold (negative going voltage).

Application of a LOW level to an R input for at least 25 ns resets the flip-flop unconditionally.

PRECAUTION

Any unused SET or RESET input should be connected to a logic HIGH source.

M208
8-BIT BUFFER/SHIFT REGISTER

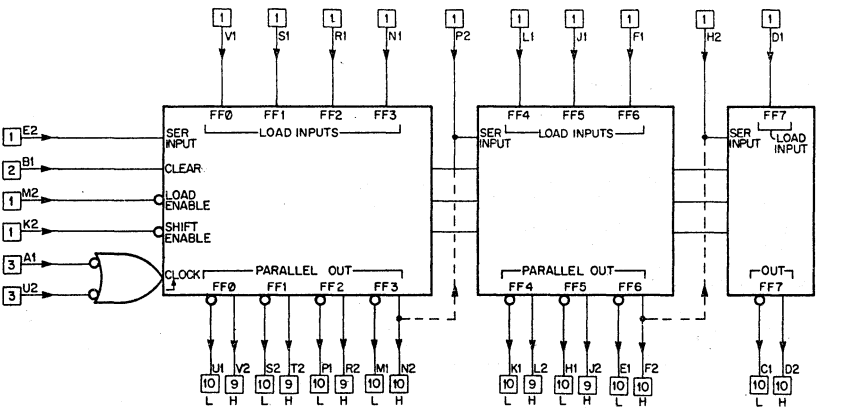
FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$84



Volts	Power mA (max.)	Pins
+5	184	A2
GND		C2, T1

The M208 is an internally connected 8-bit buffer/shift register. Provisions are made for gated single-ended parallel load, bipolar parallel output, and serial input. The shift register is divided into three segments:

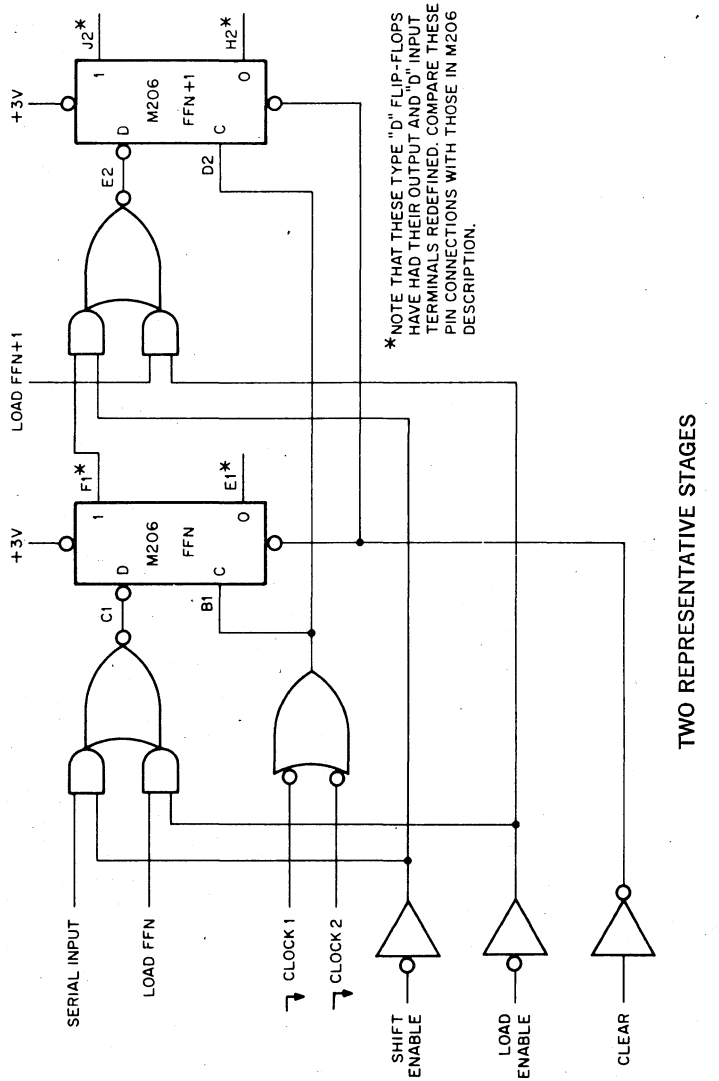
Bits 0 through 3: Serial input to bit 0, bipolar outputs from bits 0 through 3.

Bits 4 through 6: Serial input to bit 4, bipolar outputs from bits 4 through 6.

Bit 7: Serial input to 7, bipolar outputs from bit 7.

FUNCTIONS

Each of the register groups shares a common shift line (the ORed CLOCK 1 and CLOCK 2 inputs) and a common parallel load line (LOAD ENABLE). To form a 6-bit shift register, for example, the true output of bit 3 is connected to the serial input of stage 4. A shift register of 8 bits may be constructed from a single module. Modules may be cascaded to form shift registers of any desired length. A few additional stages may be formed more economically from NAND and AND/OR gates plus a D-type flip-flop. A representative stage of this type is illustrated. Two CLOCK inputs are provided so that individual LOAD and SHIFT CLOCK sources may be used.



PRECAUTIONS

Care must be taken that the clock inputs remain in the HIGH state in the off condition because either input going to the LOW state will produce a positive edge at the output of the NAND gate and trigger the D type flip-flop.

SPECIFICATIONS

Data shifted or parallel loaded into the M208 will appear on the outputs within 55 ns (max) of the CLOCK pulse leading edge threshold. LOAD and SHIFT ENABLE levels and parallel data must be present at least 50 ns prior to a CLOCK pulse. Propagation delay from the leading edge of a CLEAR pulse to the outputs is 40 ns max.

M230
BINARY TO BCD AND BCD TO BINARY CONVERTER

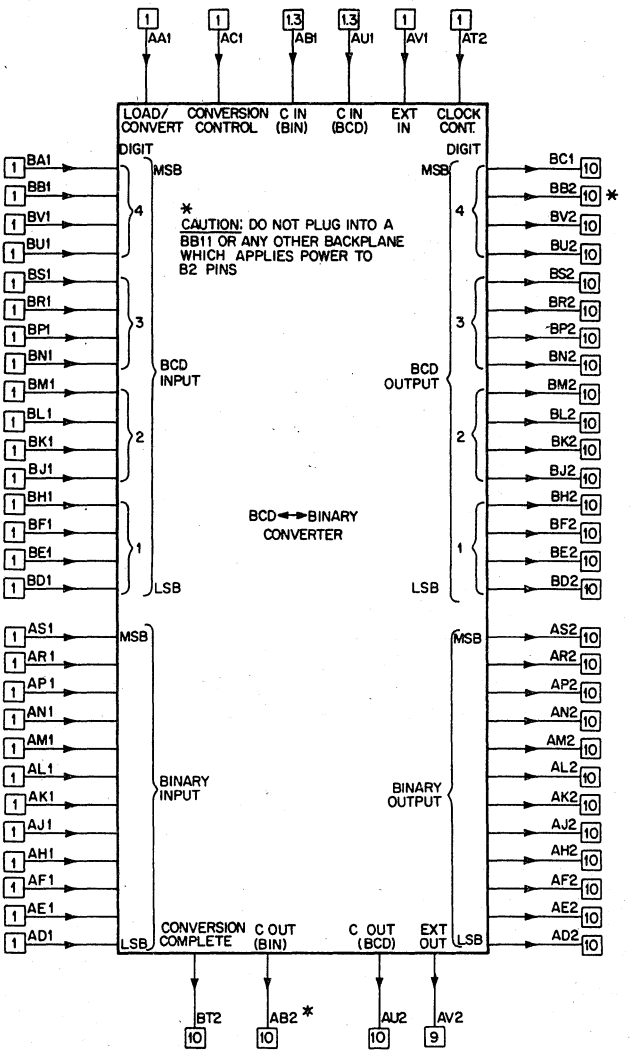
NUMERIC

M SERIES

Length: Standard
Height: Double
Width: Single

Price:

$105



Volts	Power mA (max.)	Pins
+5	860	A2
GND		C2, T1

*CAUTION
Pins AB2 and BB2 both carry logic signals, no power; therefore do not plug the M230 into a BB1 system unit since the cor responding BB11 pins both carry –15V.

The M230 converts a binary number to its binary coded decimal equivalent or a binary coded decimal number to its binary equivalent.

The maximum number that can be converted from either binary to BCD or BCD to binary is 4095 which is 7777_8. This converter utilizes a counting technique where the count frequency is typically 5 MHz. Therefore, the conversion time for the maximum number 7777_8 is typically 0.82 millisec.

The M230 is fully cascadable. When using more than one M230 the C_{OUT} BIN. must be connected to the C_{IN} BIN. and the C_{OUT} BCD must be connected to the C_{IN} BCD of the next higher significant unit. C_{IN} BIN. and C_{IN} BCD of the least significant unit must be made a logic "1". C_{OUT} BIN. and C_{OUT} BCD of the most significant unit may be left open.

CONVERSION CONTROL on pin AC1 will cause a Binary to BCD conversion when connected to ground and a BCD to Binary conversion when connected to a logic "1" source. When cascading M230's, connect all CONVERSION CONTROL inputs in parallel.

LOAD/CONVERT on pin AA1 reads the input data when connected to a logic "1" level and starts the conversion when this input is returned to a logic "0" level. When cascading M230's, connect all LOAD/CONVERT inputs in parallel.

CONVERSION COMPLETE on pin BT2 goes High when the conversion process is finished.

EXT. IN on pin AV1 and EXT. OUT on pin AV2 convey conversion finished information between cascaded M230's. This information travels from the most significant M230 to the least significant M230. Therefore, the EXT. IN of the most significant M230 **must** be connected to a logic "1" source. Each EXT. OUT is connected to the EXT. IN of the next less significant M230. The EXT. OUT of the least significant M230 is left unconnected.

CLOCK CONTROL on pin AT2 of the least significant M230 should be enabled by connecting it to a logic "1" source. All others should be connected to ground.

The following is an ordered summary for operating a single M230:

1. Make the conversion control (pin AC1) a logic "0" for converting Binary to BCD or a logic "1" for converting BCD to Binary.
2. When converting Binary to BCD, connect the Binary number to the BINARY INPUTS and ground the BCD INPUTS. Conversely, when converting BCD to Binary, connect the BCD number to the BCD INPUTS and ground the BINARY INPUTS.
3. C_{IN} BIN., C_{IN} BCD, EXT. IN, and CLOCK CONTROL inputs should be tied to a source of logic "1". The outputs C_{OUT} BIN., C_{OUT} BCD, and EXT. OUT should be left unconnected.
4. Pulse the LOAD/CONVERT input with a positive pulse of 150 nsec. minimum pulse width. There is no limit on the maximum width of this pulse. Conversion begins on the negative going edge of this pulse.
5. When converting Binary to BCD read the BCD OUTPUT for the BCD equivalent. For converting BCD to Binary read the BINARY OUTPUT for the Binary equivalent. The CONVERSION COMPLETE OUTPUT becomes a logic "1" when the conversion is through.

M232
16-WORD RAM

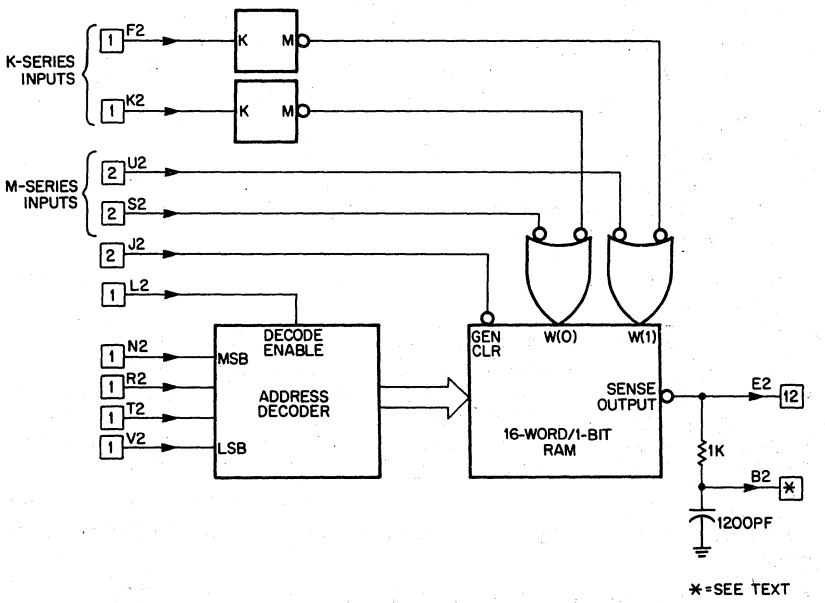
FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$125



Volts	Power mA (max.)	Pins
+5	200	A2
GND		C2, T1

The M232 provides individually addressable storage for 16 bits.

FUNCTIONS

Each bit is addressed by a 4-bit code on input lines N2, R2, T2, and V2. If a binary 0 is stored at an accessed address, the output sense pin E2 remains HIGH. If a binary 1 is stored, the output sense signal goes LOW.

Writing with M Series signals is achieved by causing pin U2 to go LOW for a binary 1 or by causing pin S2 to go LOW for a binary 0 after a location has been accessed. Writing with K Series signals is achieved by causing pin F2 to go HIGH for a binary 1, or pin K2 to go HIGH for a binary 0 after a location has been accessed.

All locations can be accessed simultaneously and all bits cleared to binary 0 by a 5-microsecond LOW signal on the GENERAL CLEAR pin J2. Pin B2 is a special-purpose OUTPUT SENSE connection which is used when module outputs are ORed or connected in parallel as is done in some PDP-14 systems.

SPECIFICATIONS

Access Time: Access to an addressed location occurs 25 ns after the DECODE ENABLE pin L2 goes HIGH.

Write Pulse (M Series): 25 ns min.

Write Pulse (K Series): 5 μs min.

Clear Pulse (J2): 5 μs min.

M236
12-BIT BINARY UP/DOWN COUNTER

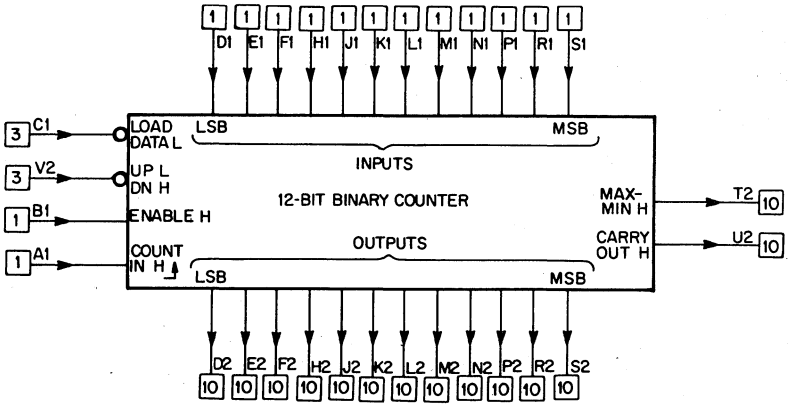
NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$50



Volts	Power mA (max.)	Pins
+5	330	A2
GND		C2, T1

The M236 is a 12-bit synchronous binary up/down counter. It has a single control input that can switch the counting mode from up to down without disturbing the contents of the counter. The M236 is fully cascadable and programmable. Cascading simply involves paralleling the respective ENABLE, LOAD DATA, and UP/DOWN signals while one CARRY-OUT signal drives the COUNT IN input of the next M236.

APPLICATIONS

The programmability of the M236 makes it ideal for use as a modulo-N divider. Modification of the count length is easily done by setting the DATA input lines to N and loading each time the count down reaches zero. When counting down the MAX-MIN output goes HIGH when all twelve bits equal zero.

FUNCTIONS

COUNT IN: Counting occurs on a positive transition of the COUNT IN line. This input must remain LOW for at least 50 ns before the count. Time between pulses can be no less than 50 ns. There is no maximum for pulse width or time between pulses. The maximum count frequency is 10 MHz.

ENABLE: The ENABLE input permits counting while it is HIGH, and disables counting while it is LOW. Critical timing factors that must be observed when changing the enabled state are:

1. To enable counting, the ENABLE line must remain HIGH from 70 ns before to 30 ns after the positive transition of the COUNT IN signal.

2. To disable counting, the ENABLE line must go LOW at least 40 ns before the COUNT IN signal goes LOW, and remain LOW until at least 40 ns after the positive transition of the COUNT IN signal.

LOAD DATA: The outputs assume the same state as their associated data inputs, independent of the count, when LOAD DATA goes LOW for at least 50 ns. Loading data overrides all other input signals and may be done at any time. The maximum propagation delay from the LOAD DATA input to any output is 50 ns. The DATA inputs will have no effect upon the outputs within 15 ns after the LOAD DATA line goes HIGH.

UP/DOWN CONTROL: A logic LOW on this line yields an up count. A logic HIGH on this line yields a down count. This control signal may be changed when the COUNT IN signal is HIGH. It must not be changed while the COUNT IN is LOW or during the 40 ns period before the COUNT IN signal goes LOW.

CARRY OUT: When the counter has reached either the maximum up count state (7777 octal) or the minimum down count state (0000 octal), the CARRY OUT signal follows the COUNT IN signal. The maximum delay time from the COUNT IN transition to the CARRY OUT transition is 60 ns.

MAX-MIN: This provides a logic HIGH output when the counter has reached either the maximum up count state (7777 octal) or the minimum down count state (0000 octal). The maximum delay time for this output measured from the positive going edge of the COUNT IN signal is 120 ns. This signal is also used to accomplish look-ahead for very high speed operations.

Cascading: When cascading M236's, the CARRY OUT should be connected to the COUNT IN of the next more significant unit. Also, the respective LOAD DATA, UP/DOWN, and ENABLE signals must be paralleled.

M237
3-DIGIT BCD UP/DOWN COUNTER

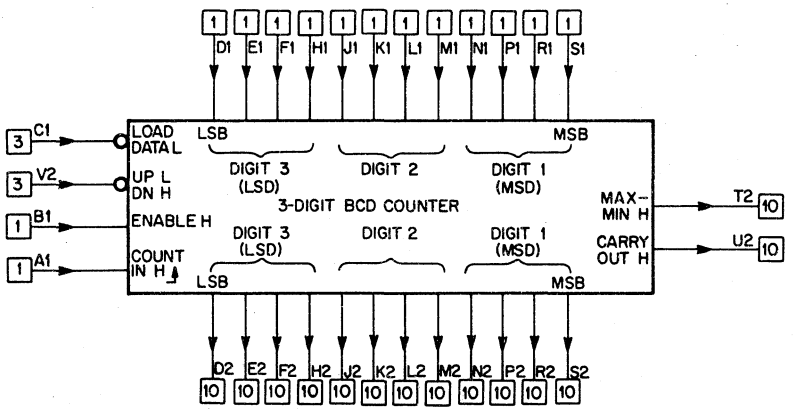
NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$50



Volts	Power mA (max.)	Pins
+5	330	A2
GND		C2, T1

The M237 is a 3-digit synchronous BCD up/down counter. It has a single control input that can switch the counting mode from up to down without disturbing the contents of the counter. The M237 is fully cascadable and programmable. Cascading simply involves paralleling the respective ENABLE, LOAD DATA, and UP/DOWN signals while one MAX/MIN signal drives the ENABLE input of the next M237.

APPLICATIONS

The programmability of the M237 makes it ideal for use as a modulo-N divider. Modification of the count length is easily done by setting the DATA input lines to N and loading each time the count down reaches zero. When counting down the MAX/MIN output goes HIGH when all three digits equal zero.

FUNCTIONS

COUNT IN: Counting occurs on a positive transition of the COUNT IN line. This input must remain LOW for at least 50 ns before the count. Time between pulses can be no less than 50 ns. There is no maximum for pulse width or time between pulses. The maximum count frequency is 10 MHz.

ENABLE: The ENABLE input permits counting while it is HIGH, and disables counting while it is LOW. Critical timing factors that must be observed when changing the enabled state are:

1. To enable counting, the ENABLE line must remain HIGH from 70 ns before to 30 ns after the positive transition of the COUNT IN signal.

2. To disable counting, the ENABLE line must go LOW at least 40 ns before the COUNT IN signal goes LOW, and remain LOW until at least 40 ns after the positive transition of the COUNT IN signal.

LOAD DATA: The outputs assume the same state as their associated data inputs, independent of the count, when LOAD DATA goes LOW for at least 50 ns. Loading data overrides all other input signals and may be done at any time. The maximum propagation delay from the LOAD DATA input to any output is 50 ns. The DATA inputs will have no effect upon the outputs within 15 ns after the LOAD DATA line goes HIGH.

UP/DOWN CONTROL: A logic LOW on this line yields an up count. A logic HIGH on this line yields a down count. This control signal may be changed when the COUNT IN signal is HIGH. It must not be changed while the COUNT IN is LOW or during the 40 ns period before the COUNT IN signal goes LOW.

CARRY OUT: When the counter has reached either the maximum up count state (999) or the minimum down count state (000), the CARRY OUT signal follows the COUNT IN signal. The maximum delay time from the COUNT IN transition to the CARRY OUT transition is 60 ns.

MAX-MIN: This provides a logic HIGH output when the counter has reached either the maximum up count state (999) or the minimum down count state (000). The maximum delay time for this output measured from the positive going edge of the COUNT IN signal is 120 ns. This signal is also used to accomplish look-ahead for very high speed operations.

Cascading: When cascading M237's, the CARRY OUT should be connected to the COUNT IN of the next more significant unit. Also, the respective LOAD DATA, UP/DOWN, and ENABLE signals must be paralleled.

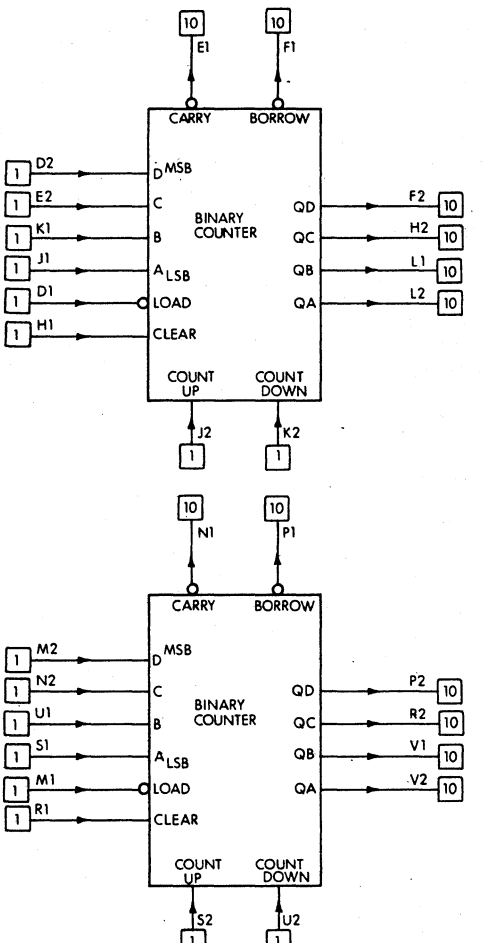
M238
DUAL 4-BIT BINARY SYNCHRONOUS UP/DOWN COUNTER

NUMERIC

M SERIES

Length: Standard
Width: Single
Width: Single

Price
$35



Volts	Power mA (max.)	Pins
+5	180	A2
GND		C2, T1

The M238 module consists of two identical 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other.

The outputs are triggered by a LOW to HIGH level transition of either COUNT input. The direction of the counting is determined by which COUNT input is pulsed while the other COUNT input is High.

The counters are fully programmable; that is, the outputs may be preset to any state by entering the desired data at the DATA inputs while the LOAD input is LOW. The output will change to agree with the DATA inputs independently of the COUNT pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A CLEAR input has been provided which forces all outputs to the LOW level when a HIGH level is applied. The CLEAR function is independent of the COUNT and LOAD inputs.

These counters were designed to be cascaded without the need for any external circuitry. The counters can be cascaded by feeding the BORROW and CARRY outputs to the COUNT-DOWN and COUNT-UP iuputs respectively, of the succeeding counter.

SPECIFICATIONS
Refer to Table 1.

TABLE 1

Parameter	From Input	To Output	Max.
f max	—	—	10 MHz
t set up	—	—	25 ns
tp	Count-up	Carry	50 ns
tp	Count-down	Borrow	50 ns
tp	Either-Count	Q	50 ns
tp	Load	Q	50 ns
tp	Clear	Q	50 ns

f max = Maximum Clock Freq.
tp = propagation delay time, for either a High-going or Low-going output change.

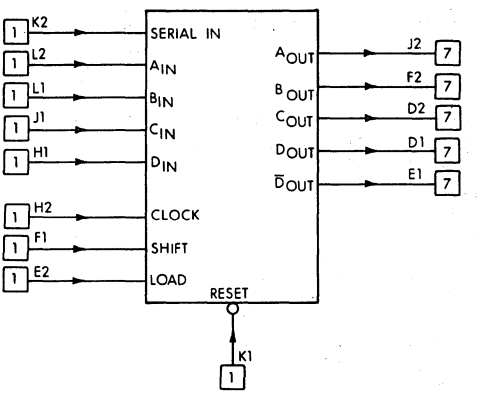
M245
DUAL 4-BIT
SHIFT REGISTER

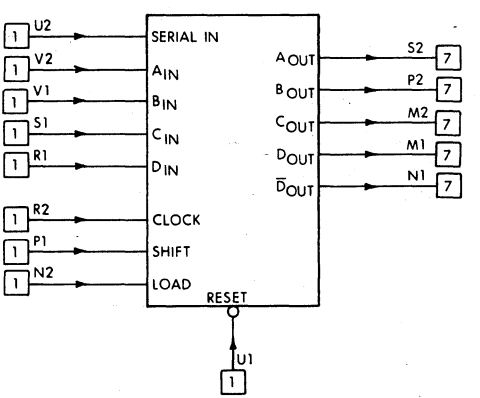
FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single

Price
$28





The M245 module consists of two 4-bit shift registers with both serial and parallel data entry capability. They are shift-right only registers; that is, the output data is shifted from A toward D.

Three control modes are possible: serial shift right, parallel enter mode, and no change or hold mode. These control modes are chosen by inputs at the SHIFT and LOAD lines as shown in the Truth Table.

In the serial mode of operation, data present at the SERIAL INput, when the SHIFT input is High, is loaded on the Low-going edge of the CLOCK pulse.

In the parallel entry mode, data present at the data inputs A IN through D IN, when the LOAD line is High, is loaded on the Low-going edge of the CLOCK pulse.

The hold mode is created by holding both the LOAD and SHIFT lines Low. By doing this, the CLOCK pulse will have no effect on the output, regardless of data present at the SERIAL INputs or DATA INputs.

A RESET line has been provided for the registers which will clear the internal flip-flop circuitry.

SPECIFICATIONS

Transfer Rate	= 10 MHz (max)
SHIFT Set-up Time	= 50 ns (min)
LOAD SET-up Time	= 50 (min)
DATA IN Set-up Time	= 25 ns (min)

Propagation Delay

From:	To:
CLOCK	Output (HIGH or LOW) = 50 ns (max)

TRUTH TABLE

CONTROL STATE	LOAD	SHIFT
Hold	L	L
Parallel Entry	H	L
Serial Shift Right	L	H

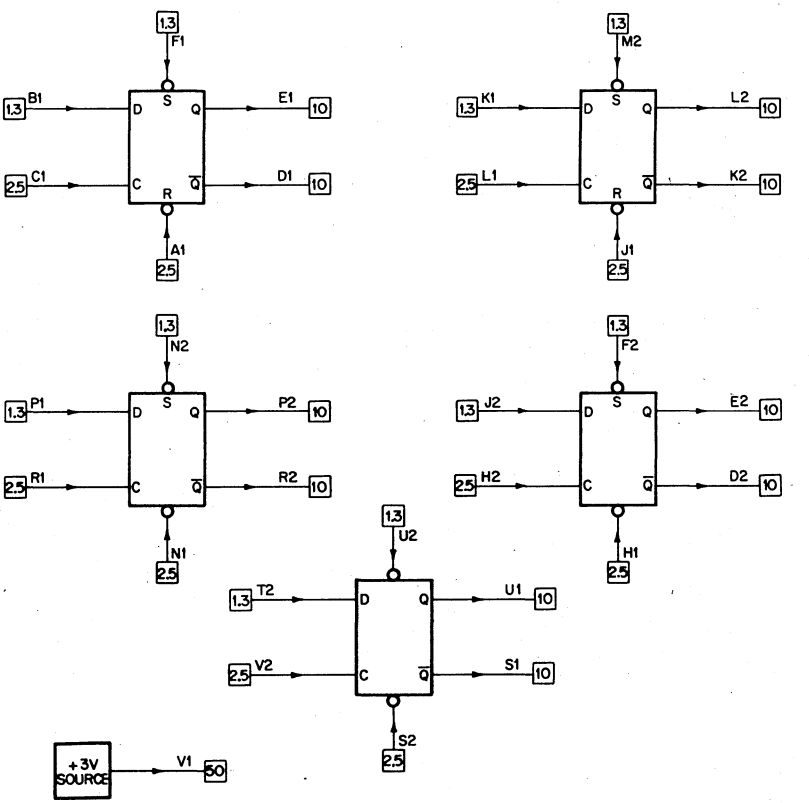
M246
5 D-TYPE FLIP-FLOPS

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single

Price
$21



Volts	Power mA (max.)	Pins
+5	160	A2
GND		C2, M1, T1

The M246 module contains five high-speed, general-purpose, D-type flip-flops. Each flip-flop has its SET(S), RESET(R), CLOCK(C), DATA(D), and outputs brought out to separate pins.

The information at the D or DATA input is transferred to the Q output on the positive-going edge of the CLOCK pulse. The CLOCK-triggering occurs at a voltage level of the CLOCK pulse and is not directly related to the transition time of the positive-going pulse.

SPECIFICATIONS

Clock Freq	= 10 MHz (max
CLOCK Pulse	= 25 ns (min)
SET Pulse	= 50 ns (min)
RESET Pulse	= 50 ns (min)
DATA Set-up Time	= 25 ns (min)

Propagation Delay Time

From:	To:
SET or RESET	LOW or HIGH Output = 40 ns (max)
CLOCK	LOW or HIGH Output = 40 ns (max)

TRUTH TABLE (Each Flip-Flop)

t_n	t_n+1	
INPUT D	OUTPUT Q	OUTPUT Q
L	L	H
H	H	L

where: t_n = bit time before CLOCK pulse

where: t_{n+1} = bit time after CLOCK pulse

NOTE: The M246 module also contains a +3V logic High source at pin V1 which can be used to tie up to 50 M Series inputs High.

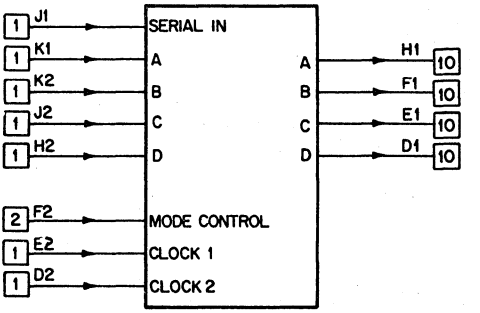
M248
DUAL 4-BIT
MULTIPURPOSE SHIFT REGISTER

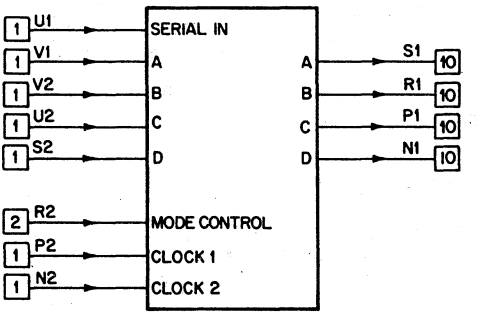
FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single

Price
$15





Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, T1

The M248 module consists of two 4-bit Shift registers—multipurpose in the fact that they are capable of either serial or parallel entry, shifting right, or with simple external connections, shifting left.

When a logic LOW is applied to the MODE CONTROL input, a shift right operation is performed by clocking at the CLOCK 1 input. In this mode, serial data is entered at the SERIAL INput. CLOCK 2 and parallel inputs A through D are inhibited.

When a logic HIGH is applied to the MODE CONTROL input, it allows entry of parallel data through inputs A through D and CLOCK 2. This mode permits parallel loading of the register or, with external interconnection, shift left operation. In this mode, shift left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop; that is, D output to C input, etc., and serial data is entered at input D.

Two clock inputs are available which permit separate clock sources to be used for the shift right and shift left modes. If both modes can be clocked from the same source, the clock input may be applied to both CLOCK 1 and CLOCK 2. The transfer of information to the output pins occurs when the clock input goes from a logic High to a logic Low.

SPECIFICATIONS

Shift Freq = 10 MHz (max)

Propagation Delay

From:	To:
CLOCKS	High or Low Output = 40 ns (max)

Set-up Time:

SERIAL Input A, B, C, D = 20 ns (min)
MODE CONTROL with respect to CLOCKS = 25 ns (min)

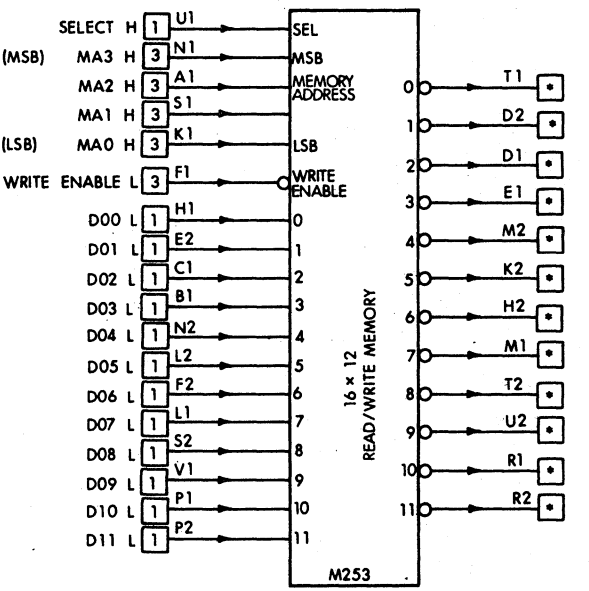
M253
16-WORD X 12-BIT RAM

FLIP-FLOPS

M SERIES

Length: Standard
Height: Single
Width: Single

Price
$73



*FAN-OUT DEPENDS ON PULL-UP RESISTOR (SEE TEXT)

Volts	Power mA (max.)	Pins
+5	390	A2
GND		C2, J2, T1, V2

The M253 module is a 192-bit read/write random access bipolar semiconductor memory, organized in a 16-word by 12-bit array.

Each of the 16 memory words is accessible through the 12 data outputs (00-11). Word addressing is in straight binary format on input pins K1, S1, A1, and N1. An overriding memory SELECT input is provided which will protect the information stored in memory when it is Low. The memory is volatile, and information will be lost if the supply voltage is removed.

APPLICATIONS

This module may be used as a scratchpad memory of 16 words by 12 bits with other modules of the same type, or may be used to construct larger memory arrays where fast reading and writing are required.

FUNCTIONS

Data on input pins D0-D11 will be written into the memory when the SELECT is HIGH and the WRITE ENABLE is LOW. The location in which it is desired to write the data must be addressed in binary format at the address inputs. The data outputs will assume the opposite state of the information at the data inputs within 100 nanoseconds after the LOW- to HIGH-going edge of the WRITE ENABLE pulse.

To guarantee that writing will occur, the input data, SELECT, and the address lines must all attain a stable level at least five nanoseconds before the WRITE ENABLE input goes LOW. These inputs must maintain this stable level until at least five nanoseconds after the WRITE ENABLE returns HIGH. The WRITE ENABLE input should go LOW for a minimum of 40 nanoseconds.

When the WRITE ENABLE and the SELECT are both HIGH, writing cannot take place and the memory is in the read mode. Data stored in the memory will appear at the data outputs when a binary address is present at the address inputs. The access time for retrieving data from memory is 100 nanoseconds. Readout is nondestructive, and the data outputs are inverted from the data originally stored.

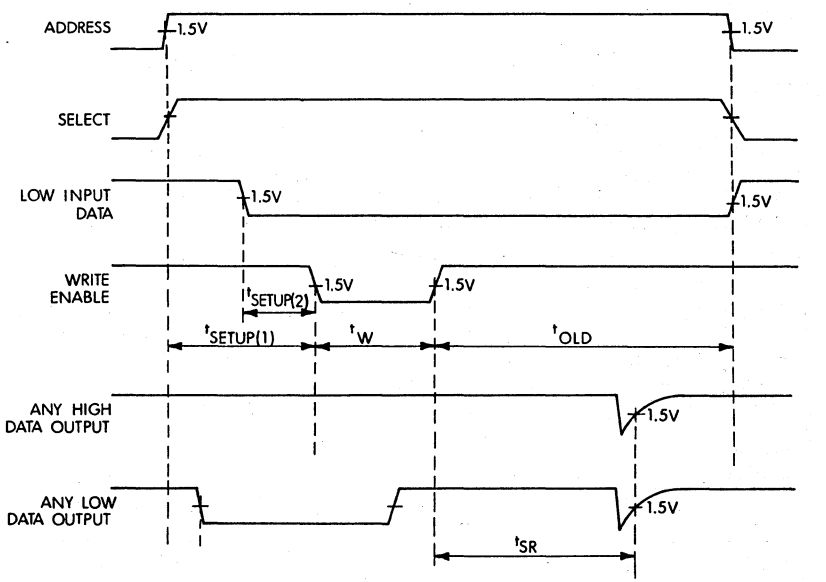
SELECT	WRITE ENABLE	Memory Operation	Output Conditions
H	H	Read	Complement of Selected Word
H	L	Write	Undefined
L	H	Do Nothing	H
L	L	Do Nothing	Complement of Data Inputs

The data outputs (00-11) are open-collector stages that require either a resistor to +5 volts or the M165 module, to act as a pull-up load. Outputs may be connected together. The value of the pull-up resistor to be used on the data outputs should be calculated from the following equation:

$$\frac{5.25}{10 - M_L} \leq R \leq \frac{2.35}{N(0.3) + M_H}$$

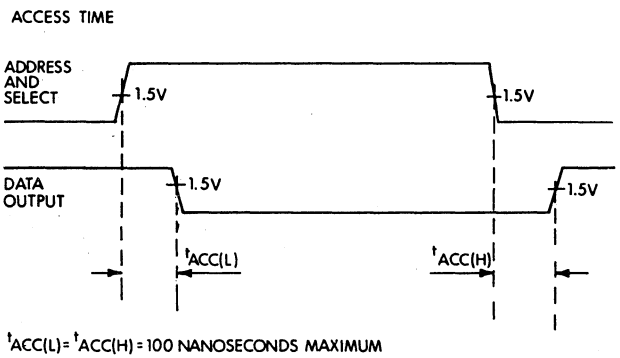
where: M = number of TTL loads driven by output,
N = number of outputs wire-ORed.
L = TTL unit load input current at low in mA,
H = TTL unit load input current at high in mA,
R = pull-up resistor in Kilohms.

TIMING



	Parameter	Min	Max
t_W	Write Pulse Width	40 ns	
$t_{set\text{-}up\ (1)}$	Write set-up time. Write enable to follow address enable by (high or low level data)	5 ns	
$t_{set\text{-}up\ (2)}$	Write set-up time. Write enable to follow data by	5 ns	
t_{HOLD}	Address, Enable or Data to follow Write Enable by	5 ns	
t_{sr}	Sense recovery time after Write	5 ns	100 ns

SPECIFICATIONS



$^{t}ACC(L) = {}^{t}ACC(H) = 100$ NANOSECONDS MAXIMUM

Maximum Capacitive Load:
30 pF for access time to be within its specified maximum value.

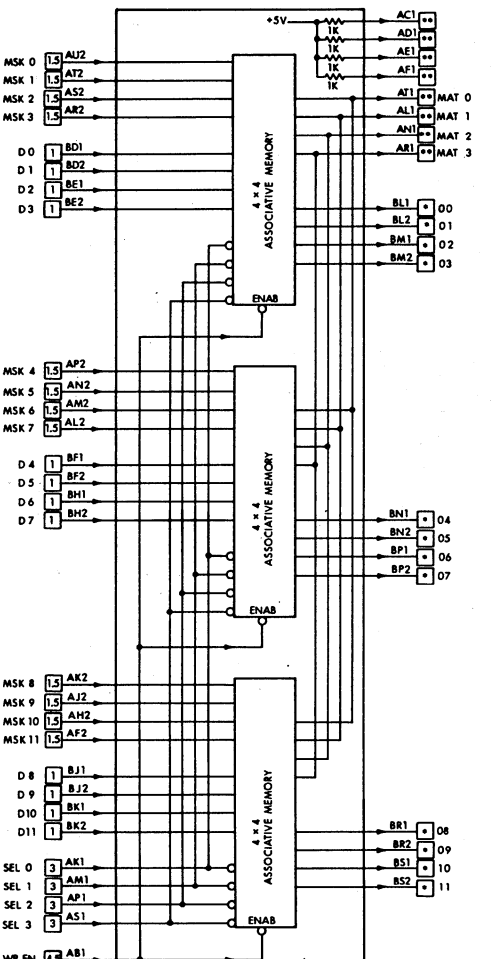
M260
4-WORD X 12-BIT
ASSOCIATIVE MEMORY

FLIP-FLOPS

M SERIES

Length: Standard
Height: Double
Width: Single

Price
$221



*FAN-OUT DEPENDS ON PULL-UP RESISTORS
**REFER TO FORMULA GIVEN IN THE TEXT

Volts	Power mA (max.)	Pins
+5	375	A2

The M260 is a high-speed 48-bit associative random access memory. It is a 4-word by 12-bit array in which the equality search is performed on all bits in parallel. All inputs and outputs are compatible with TTL levels.

To perform an equality search, the 12 bits of data on which the search is to be performed are presented at the data inputs (D0-D11) with the WRITE ENABLE input High and the bit enable lines (MSK0-MSK11) Low. The outputs (MAT0-MAT3) associated with the matched word will then go High.

Because the memory consists of three 4x4 memory units, the match outputs are paralleled as shown in the logic diagram. As an example, for the MAT0 output to go High, bits 0, 4, and 8 of the data word stored in the memory location being addressed would have to equal the corresponding data on input lines D0, D4, and D8. If, however, an MSK input line is held High, a match is forced on the corresponding bit in all words regardless of the state of the data input bit.

Data can be written into the memory through the data inputs (D0-D11) under control of the address inputs (ADD SEL 0 — ADD SEL 3) and the appropriate when the write enable (WR ENB) is Low. When writing information into the memory, both the data and address inputs should reach a stable level at least 10 nanoseconds before the WRITE ENABLE goes Low and both data and address should remain stable for at least 10 nanoseconds after the WRITE ENABLE goes High. Data will be present at the data outputs (00-11) not later than 80 nanoseconds following the High to Low transition of the WRITE ENABLE pulse.

Reading can occur either during an equality search or a write operation. If a single word is addressed, that word will appear at the data outputs. If more than one word is addressed, the wired-OR of the addressed words will appear at the data outputs. Readout is nondestructive.

All outputs are open-collector and require either a pull-up resistor connected to +5 volts, or the M165 module.

The value of the resistor to be used as a pull-up for the outputs should be calculated from the following equation:

Data Outputs:

$$\frac{5.25}{10 - M \cdot L} \leqslant R \leqslant \frac{2.35}{N(.05) + M \cdot H}$$

Match Outputs:

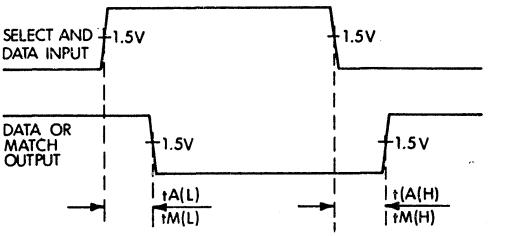
$$\frac{5.25}{10 - M \cdot L} \leqslant R \leqslant \frac{2.35}{N(.55) + M \cdot H}$$

Where: M = number of TTL loads driven by output
N = number of outputs wire-ORed
L = TTL unit load input current at low in mA
H = TTL unit load input current at high in mA
R = pull-up resistor in kilohms

APPLICATION
May be used for comparing and locating data. Can be used as a learning memory, with suitable gating, by loading any word into memory which is not already contained in storage.

SPECIFICATIONS

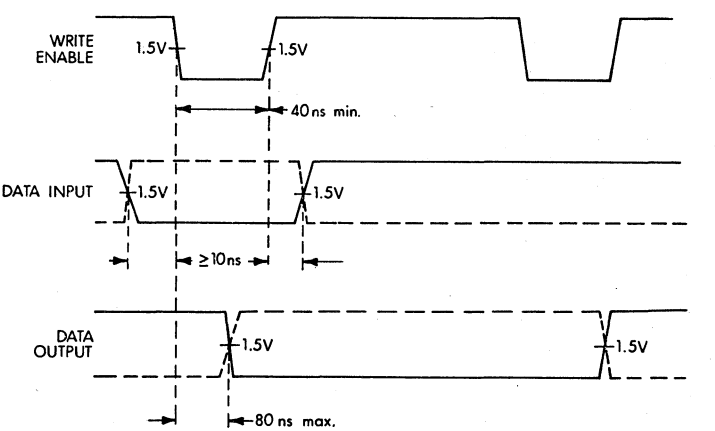
Propagation Delay:



Address to data output delay	t_A (L)	=	30	ns	maximum	0	ns	minimum
	t_A (H)	=	35	ns	maximum	0	ns	minimum
Data bit to match output	t_M (L)	=	35	ns	maximum	0	ns	minimum
	t_M (H)	=	40	ns	maximum	0	ns	minimum

Maximum Capacitive Load: 30 pF for access and matched delays to be within their specified maximum values.

Timing:



This diagram assumes that the address line is Low at least 10 nanoseconds before the WRITE ENABLE goes Low and remains Low for the remainder of the diagram.

M261
FOUR-STATE MOTOR TRANSLATOR

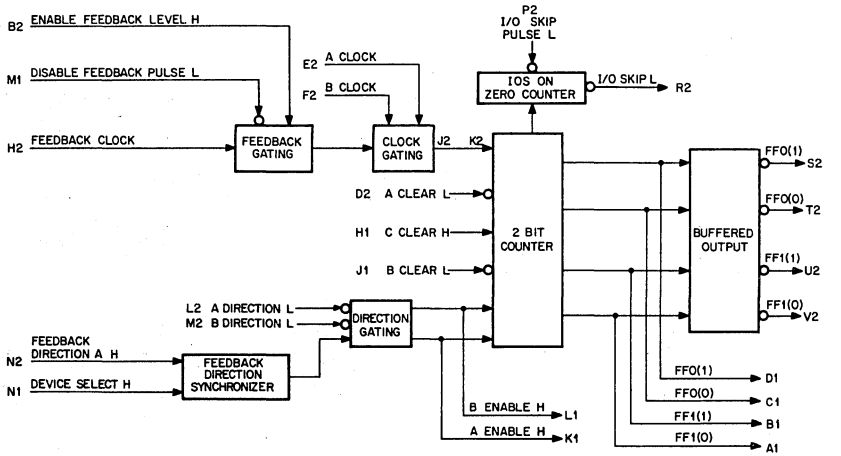
MISCELLANEOUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$40



Volts	Power mA (max.)	Pins
+5	175	A2
GND		C2, T1

The M261 motor translator will develop the sequence of patterns necessary to step a Sigma or Superior Electric type stepping motor (4 winding). It is a 2-bit switch-tail ring counter which, if initially cleared, would be in state 1. (Fig. 1)

State	Flip Flop	0	1
1		0	0
2		0	1
3		1	1
4		1	0

FIGURE 1

State	Winding	A	B	C	D
1		1	1	0	0
2		0	1	1	0
3		0	0	1	1
4		1	0	0	1

1 = current supplied to winding

FIGURE 2

The state sequence (1, 2, 3, 4, 1, . . . or 1, 4, 3, 2, 1, . . .) is determined by the direction gating. The pattern for motor stepping (Fig. 2) is achieved by assigning flip flop outputs to windings; A-FF1(1), B-FF0(1), C-FF1(0), D-FF0(0). These buffered flip flop outputs can enable K-series DC drivers to energize the selected winding.

The translator is clocked by a High to Low transition on A CLOCK or B CLOCK. The ORed clock signal must be jumpered externally to the counter (J2-K2). DIRECTION is stored in an RS flip flop and can be loaded by asserting one of the direction inputs Low. This arrangement facilitates the use of M103 or M107 device selectors; the first pulse of an IOT (input/output transfer instruction) sets the direction, the second clocks the counter.

For closed loop operation, the direction flip flop may be synchronized with the motor shaft rotation. If there is a direction level available from the transducer, this level should be asserted high when the direction of rotation is the same as that represented by the A DIRECTION L input to the flip flop. This gating may be disabled by DEVICE SELECT H. The clock input for feedback operation is a Low to High transition and is ORed with the other clocks after gating. The two gating signals are an enable, asserted High, and a pulse or level asserted Low which truncates the clock pulse after it has made its transition. This is necessary because the clock signal is from an asynchronous device and is often a square wave which remains High a long time (20-100 μs) after the clocking transition. This High level at the clock input of the counter will mask subsequent transitions on the other clock inputs.

This module may be used in conjunction with the I/O skip facility on a computer. An IOT at I/O SKIP PULSE L and both flip flops in the zero state will cause I/O SKIP L to be generated.

The unbuffered flip flop outputs are available for additional gating. These lines are electrically distinct from the buffered outputs.

M262
TEN-STATE MOTOR TRANSLATOR

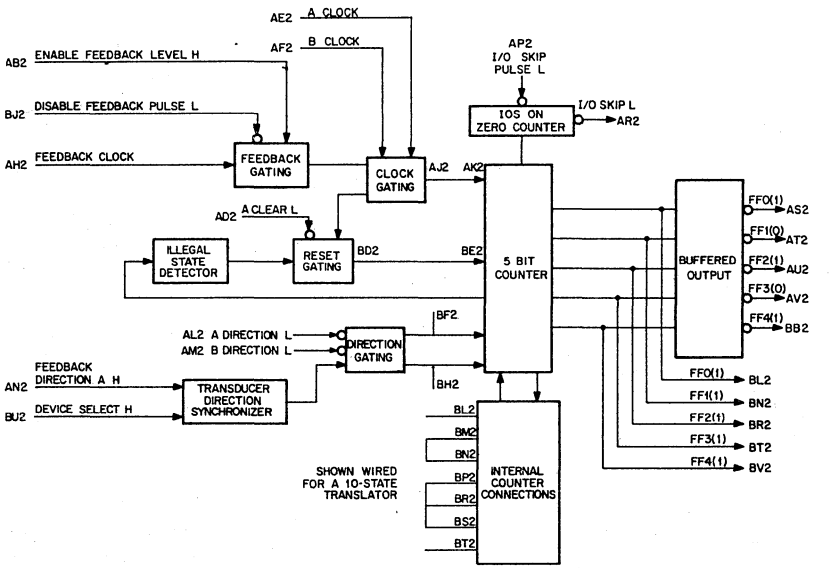
MISCELLA-NEOUS

M SERIES

Length: Standard
Height: Double
Width: Single

Price:

$65



Volts	Power mA (max.)	Pins
+5	350	AA2, BA2
GND		AC2, BC2

The M262 motor translator will generate the sequence of patterns necessary to step a Fujitsu type stepping motor (5 winding). It is a double height module with a five bit switch-tail ring counter which may be truncated to four or three bits by external jumpers.

BM-BN	BM-BN	BL-BP
BP-BR	BP-BN	BT-BM
BR-BS	BT-BS	
10-state jumpers	8-state jumpers	6-state jumpers

State	FLIP FLOP 0	1	2	3	4
1	0	0	0	0	0
2	1	0	0	0	0
3	1	1	0	0	0
4	1	1	1	0	0
5	1	1	1	1	0
6	1	1	1	1	1
7	0	1	1	1	1
8	0	0	1	1	1
9	0	0	0	1	1
10	0	0	0	0	1

FIGURE 2

State	Winding A	B	C	D	E
1	1	1	1	0	0
2	0	1	1	0	0
3	0	1	1	1	0
4	0	0	1	1	0
5	0	0	1	1	1
6	0	0	0	1	1
7	1	0	0	1	1
8	1	0	0	0	1
9	1	1	0	0	1
10	1	1	0	0	0

FIGURE 3
1 = current supplied to winding

FF2 is removed for the 8-state counter and both FF1 and FF2 are bypassed for the 6-state counter.

After the counter is cleared it will be in state 1. (Fig. 2) The state sequence (1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 1 . . . or 1, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1 . . .) is determined by the direction gating. The pattern for motor stepping (Fig. 3) is achieved by assigning flip flop outputs to windings; FF0(1)-A FF2(1)-B, FF4(1)-C, FF1(0)-D, FF3(0)-E. These buffered flip flop outputs can enable K-series DC drivers to energize the selected windings.

The translator is clocked by a High to Low transition on A CLOCK or B CLOCK. The ORed clock signal must be jumpered externally to the counter (AJ-AK). Direction is stored in an RS flip flop and can be loaded by asserting one of the direction inputs Low. This arrangement facilitates the use of M103 or M107 device selectors; the first pulse of an IOT (input output transfer instruction) set the direction, the second clocks the counter.

With a 5-bit counter there are 32 (2^5) possible states, but the counter is clocked through a ring of only 10 states (Fig. 2). Gating is available to detect illegal states and clear the counter to state 1. This gating must be connected by an external jumper (BD-BE).

For closed loop operation, the direction flip flop may be synchronized with the motor shaft rotation. If there is a direction level available from the transducer, this level should be asserted High when the direction of rotation is the same as that represented by the A DIRECTION L input to the flip flop. This gating may be disabled by DEVICE SELECT H. The clock input for feedback operation is a Low to High transition and is ORed with the other clocks after gating. The two gating signals are an enable, asserted High, and a pulse or level asserted Low which truncates the clock pulse after it has made its transition. This is necessary because the clock signal is from an asynchronous device and is often a square wave which remains high a long time (20-100 μs) after the clocking transition. This High level at the clock input of the counter will mask subsequent transitions on the other clock inputs.

This module may be used in conjunction with I/O skip facility on a computer. An IOT at I/O SKIP PULSE L and both flip flops in the zero state will cause I/O SKIP L to be generated.

The unbuffered flip flop outputs are available for additional gating. These lines are electrically distinct from the buffered outputs.

M302
DUAL DELAY MULTIVIBRATOR

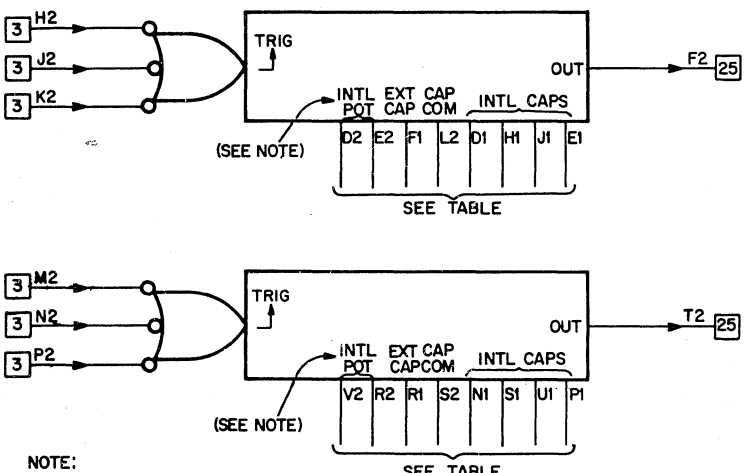
TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$46



Volts	Power mA (max.)	Pins
+5	166	A2
GND		C2, T1

The M302 contains two delays (one-shot multivibrators) which are triggered by a level change from HIGH to LOW or a pulse to LOW whose duration is equal to or greater than 50 ns. When the input is triggered, the output changes from LOW to HIGH for a predetermined length of time and then returns to LOW.

The delay time is adjustable from 50 ns to 7.5 ms using the internal capacitors and can be extended by adding an external capacitor.

APPLICATIONS

- Time delays
- Variable width pulses

FUNCTIONS

Delay Range: The basic DELAY RANGE is determined by an internal capacitor. The delay range may be increased by selection of additional capacitance which is available by connecting various module pins or by the addition of external capacitance. An internal potentiometer can be connected for fine

delay adjustments within each range or an external resistance may be used. If an external resistance is used, the combined resistance of the internal potentiometer and the external resistance should be limited to 10,000 ohms.

Delay Range	Capacitor Value	Interconnections Required	
		Delay 1	Delay 2
50 ns — 750 ns	100 pF (internal)	None	None
500 ns — 7.5 μs	1000 pF (internal)	D1 — L2	N1 — S2
5 μs — 75 μs	0.01 μF (internal)	H1 — L2	S1 — S2
50 μs — 750 μs	0.10 μF (internal)	J1 — L2	U1 — S2
500 μs — 7.5 ms	1.00 μF (internal)	E1 — L2	P1 — S2
Above 7.5 ms	Add external capacitors between specified pins	F1 — L2	R1 — S2

Adjustable Delays: Connect pins D2 to E2 for delay 1 and V2 to R2 for delay 2 in order to add the internal potentiometers. NOTE: If there is no external pot, these pins must be jumpered.

Without a potentiometer, the delay will not recover. An external potentiometer of less than 10 K ohms can be used by connecting it between E2 or R2 and ground pin C2. Use of an external adjustment resistor will cause some increase in jitter. It is recommended that leads to an external potentiometer be twisted pairs and as short as possible.

PRECAUTIONS

Care should be exercised in the selection of external capacitors to assure low leakage as leakage will affect the time delay.

SPECIFICATIONS

Trigger Input Fall Time: Must be less than 400 ns

Recovery Time: Defined as the time all inputs must remain HIGH before any input goes LOW to trigger the delay

1. Without external capacitance: 30 ns min.
2. With external capacitance: 300 C ns min. where C is in nanofarads

M306
INTEGRATING ONE SHOT

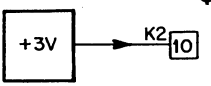
TIME RELATED

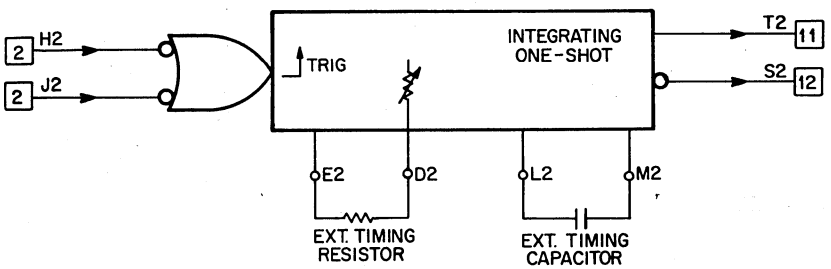
M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$27



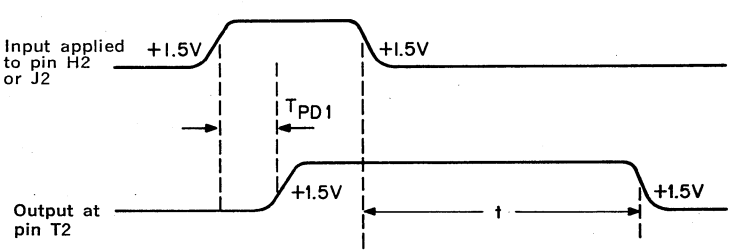


Volts	Power mA (max.)	Pins
+5	120	A2
GND		C2, T1

The M306 is a zero-recovery-time integrating monostable multivibrator with complementary outputs. The M306 has the ability to respond to an input even while in the active state, so that successive inputs above a preset frequency can postpone the return to the inactive state indefinitely.

FUNCTIONS

The operation of the M306 is illustrated in the timing diagram shown below:



The integration period is measured from the trailing edge of the input pulse to the trailing edge of the output pulse. The approximate integration time may be calculated by the following:

$$t \sim .68\,(R + 800\,\Omega)\,(C + 75 \times 10^{-12}F) + 70 \times 10^{-9}\ \text{Sec.}$$

where R is in ohms and C is in farads. The width of the input pulse is independent of the integration time.

Timing Capacitors: Coarse adjustment of the integration period is accomplished by customer-supplied capacitors which may be attached to module pins L2 and M2. When using polarized capacitors, the positive terminal should be connected to pin L2. Two split lugs are provided on the module for those customers who would like to permanently install the capacitor on the module itself. The minimum equivalent parallel resistance of capacitor leakage should always exceed 250K ohms.

Timing Resistance: Fine adjustment of the timing period may be accomplished by a multiturn potentiometer provided on the module. Provision is also made to allow the customer to connect an external timing resistor or potentiometer between pins D2 and E2. When an external potentiometer is used, care should be taken to prevent the coupling of externally generated electrical noise into the module. The maximum resistance of the timing resistance, including the internally provided potentiometer, should not exceed 25,000 ohms. If an external timing resistor is not used, pins D2 and E2 must be connected together.

SPECIFICATIONS

Trigger Duration: An input pulse of 30 ns will trigger the M306. TPD1 = 40 ns max.

Output Duration: The minimum pulse width is 225 ns and maximum pulse width is limited only by capacitor leakage (40 sec is a typical maximum).

Stability: The inherent temperature stability of the M306 is normally —.06% per degree C, exclusive of the temperature coefficient of the timing capacitor.

M310
DELAY LINE

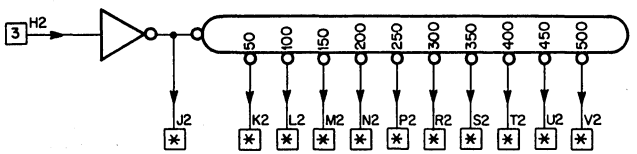
TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$58



*=SEE TEXT

Volts	Power mA (max.)	Pins
+5	89	A2
GND		C2, T1

The M310 consists of a tapped delay line with associated circuitry and two pulse amplifiers. The total delay is 500 nanoseconds with taps available at 50 nanosecond intervals.

APPLICATIONS

- Timing pulse trains
- Pulse spacing

FUNCTIONS

The time delay is increased when the amplifier is connected to the delay line taps in ascending order as follows: J2, K2, L2, M2, N2, P2, R2, S2, T2, U2, and V2. The tap J2 yields the minimum delay and the tap V2 yields the maximum delay.

Loads J2-V2 designed to be loaded only by E1 or H1. They will not drive standard TTL loads.

The pulse amplifiers are intended to be used to standardize the outputs of the delay line. The output of the pulse amplifier is a positive pulse whose duration is typically 50 to 200 nanoseconds. These amplifiers are not intended to be driven by TTL IC logic.

M360
VARIABLE DELAY

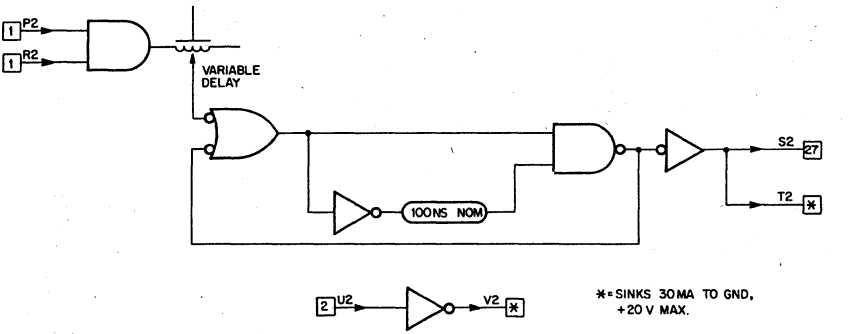
TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$68



Volts	Power mA (max.)	Pins
+5	50	A2
GND		C2, T1

The M360 contains an adjustable delay line with a standardizing amplifier. The delay is adjustable between the limits of 50 ns to 300 ns by means of a slotted screw which is accessible from the handle end of the module.

FUNCTIONS

The output consists of a positive pulse whose width is nominally 100 nanoseconds and the leading (positive going voltage) edge of which is delayed with respect to the leading (positive going voltage) edge of the input by a length of time determined by the setting of the delay line adjustment.

Pins T and V are outputs consisting of open collector NPN transistors that can sink 30 milliamperes to ground.

Precautions: Voltage applied to pins T and V must not exceed +20 volts.

SPECIFICATIONS

The resolution of the delay adjustment is approximately one nanosecond.

M401
VARIABLE CLOCK

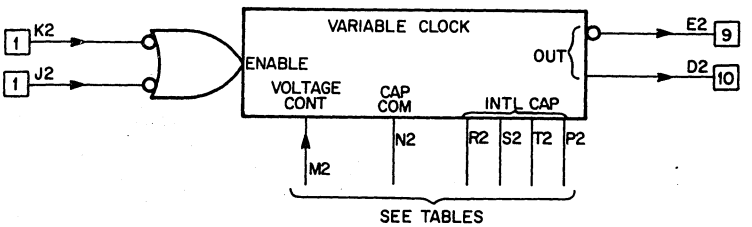
TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$55



Volts	Power mA (max.)	Pins
+5	80*	A2
GND		C2, T1

* using printed circuit board revision E or later

The M401 Variable Clock is a stable RC-coupled multivibrator which produces standard timing pulses at adjustable repetition rates.

Repetition rate is adjustable from 175 Hz to 10 MHz in five ranges. Internal capacitors, selected by jumper pin connections, provide coarse frequency control. An internal potentiometer provides continuously variable adjustment within each range.

A 0 to 10 volt control voltage will vary the frequency over about 30% of each frequency range.

APPLICATIONS

This module is intended for use as the primary source of timing signals in a digital system.

FUNCTIONS

Start Control: A two-input OR gating input is provided for start-stop control of the pulse train. A level change from HIGH to LOW with fall time less than 400 ns is required to enable the clock.

Frequency Range:

Frequency Range	Interconnections Required	
1.5 MHz to 10 MHz	(100 pf)	NONE
175 KHz to 1.75 MHz	(1000 pf)	N2 — R2
17.5 KHz to 175 KHz	(.01 μfd)	N2 — S2
1.75 KHz to 17.5 KHz	(0.1 μfd)	N2 — T2
175 Hz to 1.75 KHz	(1.0 μfd)	N2 — P2

Fine Frequency Adjustment: Controlled by an internal potentiometer. No provision is made for any external connections. An external capacitor may be added by connection between pins N2 and C2.

Voltage Control of Frequency: The M401 may also be voltage controlled by applying a control voltage to pin M. This feature is available only in M401 modules using printed circuit board revision E or later. The voltage applied to pin M should be limited to the range of 0 volts to +10.0 volts. This voltage swing will allow the frequency to be shifted by approximately 30 percent in the frequency range using the internal capacitors of 1.0, 0.1, 0.01 and 0.001 μF. If the voltage applied to pin M is dc or low frequency (below 1 kHz), pin M will appear approximately as a +1.0 volt source with a Thevenin resistance of 800 ohms. Modulating the M401 with a 10 volt P-P signal about a center frequency, as derived by the application of a mean voltage of +5 volts to pin M, will yield a typical frequency excursion in excess of plus or minus 15% about the center frequency. Typical frequency excursions which may be obtained are shown below:

Voltage applied to Pin M	CAPACITOR			
	1.0 ufd.	0.1 ufd.	0.01 ufd.	.001 ufd.
0	1.000	10.00	100.0	1000
+1	1.054	10.49	104.6	1036
+2	1.101	10.94	109.2	1071
+3	1.147	11.39	113.6	1108
+4	1.193	11.83	118.0	1142
+5	1.238	12.26	122.2	1181
+6	1.282	12.69	126.4	1271
+7	1.325	13.10	130.4	1295
+8	1.368	13.50	134.2	1312
+9	1.408	13.87	137.7	1322
+10	1.443	14.20	140.9	1323
				Output frequency in KHz

SPECIFICATIONS

Maximum delay from enabling inputs to output E2 is 50 nanoseconds. The output pulse width is 50 nanoseconds.

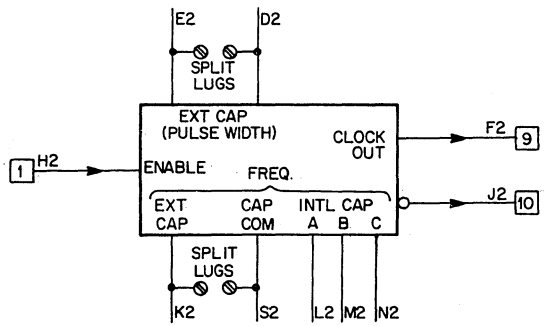
M403
RC MULTIVIBRATOR CLOCK

TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single

Price:
$30



Volts	Power mA (max.)	Pins
+5	70	A2
GND		C2, T1

The M403 is an RC Multivibrator Clock which produces standard 10-microsecond timing pulses at repetition rates adjustable from 1 kHz to 50 kHz in three ranges. Internal capacitors, selected by jumper pin connections, provide coarse frequency control, while an internal potentiometer provides continuously variable adjustment within each range.

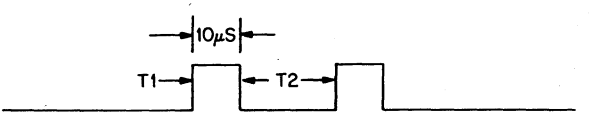
APPLICATIONS
This module can be used as a source of digital timing signals.

FUNCTIONS
ENABLE Input: The clock circuit is enabled by a HIGH level on pin H2. If a LOW level is applied to pin H2, the clock output at F2 will time out and return to ground and the output at pin J2 will time out and go HIGH. To prevent an erroneous count, pin H2 should not be retriggered for one complete period. This will allow the circuit to settle.

Selecting Frequency Range: The frequency range is selected by jumpers at backplane pins:

FREQUENCY RANGE	INTERCONNECTION REQUIRED
1 kHz to 5 kHz	N2 — S2
5 kHz to 20 kHz	M2 — S2
20 kHz to 50 kHz	L2 — S2

Lowering Frequency: If frequencies below the capabilities of this circuit are necessary, external capacitance can be added. Time 2 (see illustration) can be changd by installing capacitors to the split lugs provided or between pins K2 and S2. New timing values can be calculated using the following equation:



CLOCK H OUTPUT

$T2 = 0.32\,RC\,(1 + 0.7/R)$

T2 is in seconds, R is in ohms, and C is in farads. The internal potentiometer varies between 5.1K and 50K ohms.

Increasing Pulse Width: Larger pulse widths can also be obtained by adding capacitance to the other set of split lugs provided or between pins E2 and D2. The same equation as above may be used for T1 with the following exception:

$$C = 4.7 \text{ picofarads} + \text{capacitance added}$$

SPECIFICATIONS
Rise Time: 25 ns (max.)
Fall Time: 25 ns (max.)

M404
CRYSTAL CLOCK

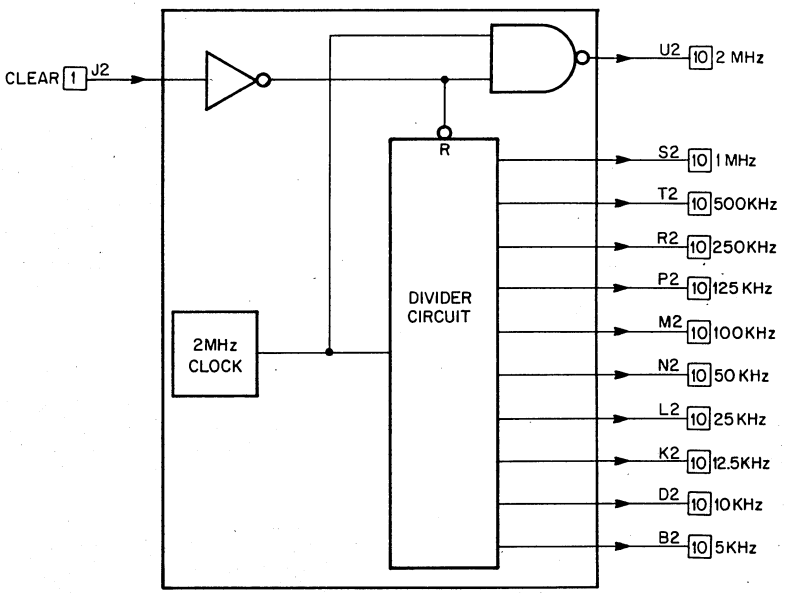
TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$65



Volts	Power mA (max.)	Pins
+5	535	A2
GND		C2, T1

The M404 clock contains a 2 MHz crystal oscillator and frequency dividers.

A HIGH on the CLEAR input clears the frequency divider and all outputs go LOW except the 2 MHz output, which goes HIGH.

SPECIFICATIONS

Accuracy: Maximum error from specified output frequency is 0.01% between 0 degrees C and +55 degrees C.

M405
CRYSTAL CLOCK

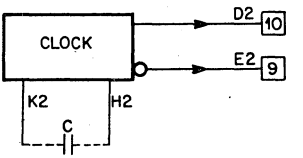
TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$100



Volts	Power mA (max.)	Pins
+5	50	A2
GND		C2, T1

The M405 employs a crystal oscillator to provide a highly stable, precisely known frequency between 5 kHz and 10 MHz. The frequency within this range may be specified by the user.

APPLICATIONS

- Stable clock frequencies

FUNCTIONS

Outputs: Outputs at pins D2 and E2 are respectively positive and negative going 50 ns pulses. Pulses at pins D2 and E2 are time shifted by one gate delay with the negative pulse at pin E2 leading the positive pulse at D2 by a maximum of 20 ns. The output pulse width can be modified by the addition of an external capacitor between pins K2 and H2. This capacitor will increase the output pulse width by approximately 1 ns per 2.5 pF of additional capacitance.

SPECIFICATIONS

Frequency Stability: 0.01% of specified value between 0 degrees C and +55 degrees C.

Ordering Information: When ordering the M405, always specify frequency. Allow six weeks for delivery.
Standard Stock Frequencies: 1.333 MHz, 2.000 MHz, 5.000 MHz.

M410
REED CLOCK

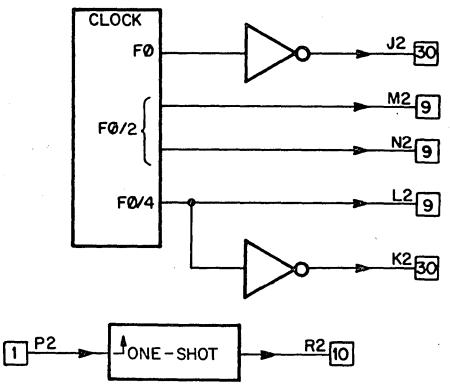
TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$70



Volts	Power mA (max.)	Pins
+5	95	A2 C2, T1

The M410 is a free-running contactless-resonant-reed-tuned clock which provides stable timing signals for a system using the M706 and M707 Teletype converter modules.

FUNCTIONS

Outputs: Pin R2 drives 10 unit loads with a nominal 150 ns positive output pulse. Pin J2 drives 30 unit loads at F0. Under normal operating conditions, pins L2, M2, N2 are used as test points. Pins N2 and M2 drive 9 unit loads at F0/2. Pin L2 drives 9 unit loads at F0/4. Pin K2 drives 30 unit loads at F0/4.

SPECIFICATIONS

Overall Frequency Stability: Better than 0.1% in the temperature range from 0 degrees C to 70 degrees C. Available clock frequencies are listed below. A pulse amplifier is provided for the generation of nominal 150 ns pulses.

Available Frequencies: (F0 in Hz) = 400 (50 baud), 550, 600 (75 baud), 750, 880 (110 baud), 1200 (150 baud), 1800, 2000, 2200, 2400 (300 baud).

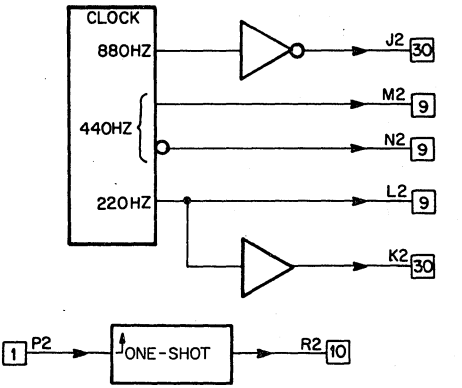
M452
VARIABLE CLOCK

TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single

Price: $40



Volts	Power mA (max.)	Pins
+5	77	A2
GND		C2, T1

The M452 is a free-running clock which generates the necessary timing signals for the PDP-8/I Teletype control. The available output frequencies are 880 Hz, 440 Hz and 220 Hz. The pulse amplifier is provided for the generation of nominal 150 ns pulses.

APPLICATIONS

- PDP-8/I Teletype Control

FUNCTIONS

Pin J2 drives 30 unit loads at 880 Hz. Pins N2 and M2 drive 9 unit loads at 440 Hz. Pin L2 drives 9 unit loads at 220 Hz. Pin K2 drives 30 unit loads at 220 Hz. Pin R2 drives 10 unit loads with a nominal 150 ns positive output pulse. Under normal operating conditions, pins L2, M2, N2 are used as test points.

SPECIFICATIONS

Frequency adjustment of this module is limited to less than 5% and the overall clock stability with respect to supply voltage and temperature variations is about 1%.

M501
SCHMITT TRIGGER

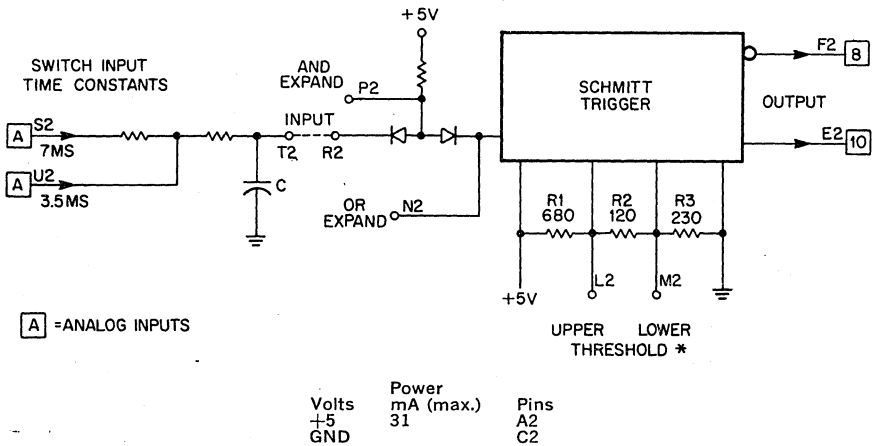
TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$25



The M501 is a Schmitt Trigger with variable thresholds and complementary positive logic outputs.

APPLICATIONS

- Switch Filter
- Pulse Shaper
- Threshold Detector

FUNCTIONS

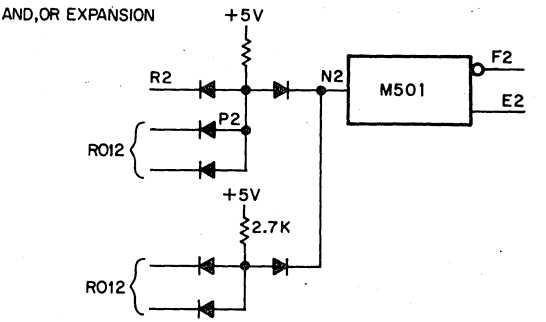
The input on pin R2 is compared with the thresholds set on pins L2 and M2 UPPER and LOWER respectively.

Pin F2 goes to LOW when the input on R2 rises above the UPPER THRESHOLD, having been below the LOWER THRESHOLD.

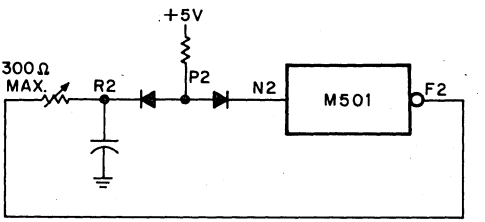
Pin F2 rises to +3 volts when the input on R2 falls below the LOWER THRESHOLD, having been above the UPPER THRESHOLD.

Pin E2 is the complement of F2.

Miscellaneous Input Functions: AND and OR expansion may be performed on P2 and N2. Modules R001 and R012 provide the diodes required. An integrator is provided on the input, allowing switches to be connected to the Schmitt Trigger with contact bounce effects eliminated. Two switch time constants are provided. Inputs to pin S2 result in a 7 ms time constant to pin U2 3.5 ms.



Oscillator Connection: Connecting a resistor from output pin F to input pin R with pin T tied to pin R forms an oscillator.



SPECIFICATIONS

Input Signal Swing: The voltage on pin R2 is limited to plus or minus 20 volts.

Thresholds: The UPPER and LOWER THRESHOLDS are preset at 1.7 and 1.1 volts. They may be modified by the addition of a resistor in parallel with the internal network; however, the UPPER THRESHOLD must not exceed 2.0 volts or the LOWER THRESHOLD fall below 0.8 volts.

R	IN	PARALLEL WITH	R2 — THRESHOLD CLOSER
R		PARALLEL	R1 — UPPER RISES
R		PARALLEL	R3 — LOWER FALLS

Input Pin R2 Loading: 2.7K ohms to +5 volts or 1.8 mA at ground.

Pin P2 AND EXPAND input
Pin N2 OR EXPAND input
Pin S2 RC SWITCH input filter 7 ms
Pin U2 RC SWITCH input filter 3.5 ms
Pins L2, M2 are available for threshold modification

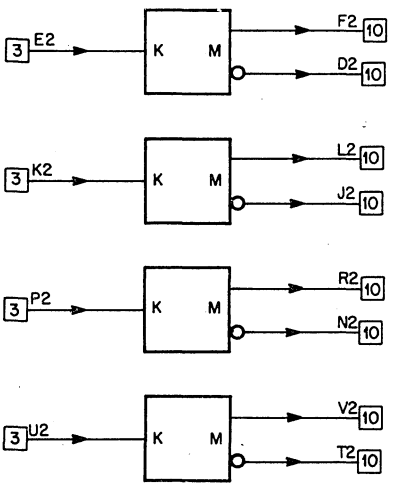
M521
K TO M CONVERTER

TIME RELATED

M SERIES

Length: Single
Height: Single
Width: Single

Price: $16



Volts	Power mA (max.)	Pins
+5	56	A2
GND		C2

The M521 K Series to M Series Converter contains four circuits which can convert any K Series input to complementing M Series outputs.

APPLICATIONS

- Rise Time Conversion — K to M Series

FUNCTIONS

Typically, a K Series input would have a 7 μs rise time and a 1.5 μs fall time. The M521 speeds both these rise and fall times to approximately 15 ns. The input circuit has built-in hysteresis and is slowed to a maximum frequency of 100 KHz.

SPECIFICATIONS

Each input represents three K Series unit loads.

M602
PULSE AMPLIFIER

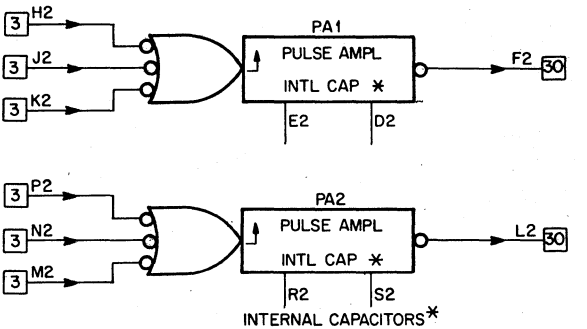
TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$28



*=JUMPER E2-D2 OR R2-S2 FOR 110ns PULSE WIDTH. STANDARD PULSE WIDTH IS 50ns.

Volts	Power mA (max.)	Pins
+5	213	A2
GND		C2, T1

The M602 contains two pulse amplifiers which provide power amplification, standardize pulses in amplitude and width, and transform level changes into a standard pulse.

FUNCTIONS

A negative pulse output is produced when the input is triggered by a transition from HIGH to LOW. An internal capacitor is brought out to pin connections to permit the standard 50 ns output pulse to be increased to 110 ns (nominal).

SPECIFICATIONS

Propagation Time: 30 ns max. between input and output thresholds.

Recovery Time: Equal to that of the output pulse width. The input must have a fall time (10% to 90% points) of less than 400 ns and must remain below 0.8 volts for at least 30 ns. Maximum PRF is 10 MHz.

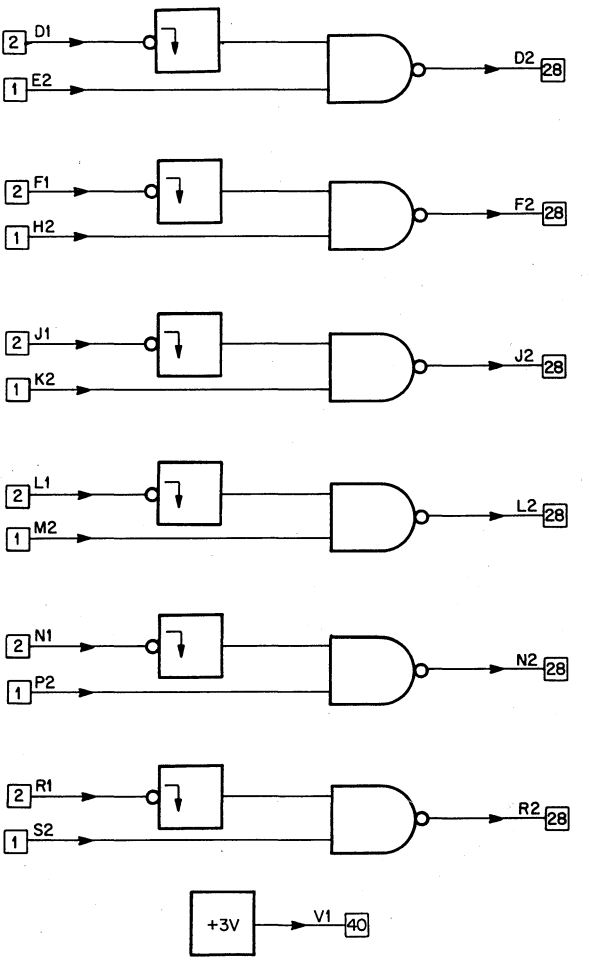
M606
PULSE GENERATOR

TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single

Price: $43



Volts	Power mA (max.)	Pins
+5	188	A2
GND		C2, T1

The M606 contains six pulse generators.

APPLICATIONS
The M606 may be used for setting or clearing of flip-flops by applying the output of the M606 to the direct CLEAR or SET inputs of up to 14 flip-flops.

FUNCTIONS
Each circuit will produce a pulse to ground in response to a level shift from HIGH to LOW to the input.

Pin V1 is a source of logic HIGH and can supply ten unit loads.

SPECIFICATIONS
All outputs consist of a pulse to ground level with a time duration of at least 30 ns but not greater than 100 ns.

M610
OPEN COLLECTOR
TWO-INPUT NAND GATE

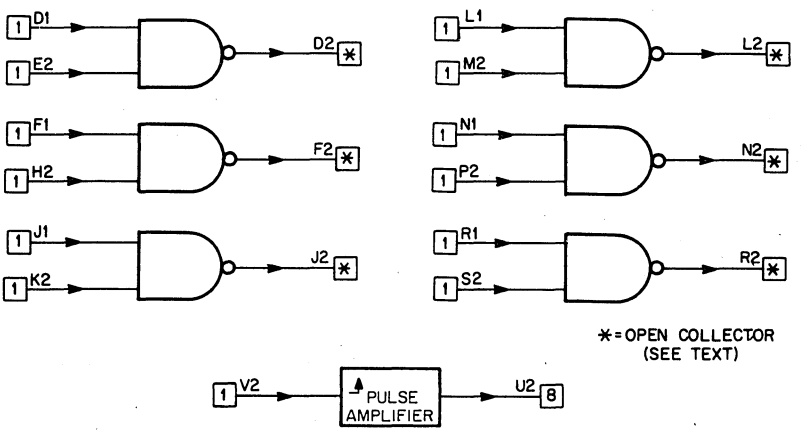
GATES

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$20



Volts	Power mA (max.)	Pins
+5	41	A2
GND		C2, E1, H1 M1, P1, S1

The M610 contains 6 two-input NAND gates with open collector outputs. It also contains a pulse amplifier which does not have an open collector output.

SPECIFICATIONS

Outputs: D2, F2, J2, L2, N2, R2 are capable of sinking 16 mA to ground.

NAND Gate Maximum Propagation Delay: 15 ns when the output goes from HIGH to LOW; however, when the output goes LOW to HIGH, the propagation delay depends upon the load impedance. As an example, with the load shown in the figure, the maximum propagation delay time from a logic LOW to a logic HIGH is 45 ns.

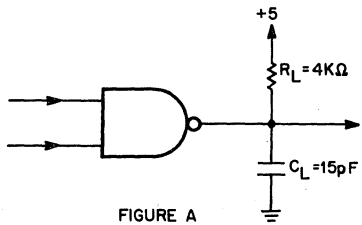


FIGURE A

Pulse Amplifier Maximum Propagation Delay: 60 ns for both HIGH going and LOW going output pulse transitions.

M617
FOUR-INPUT POWER NAND GATE

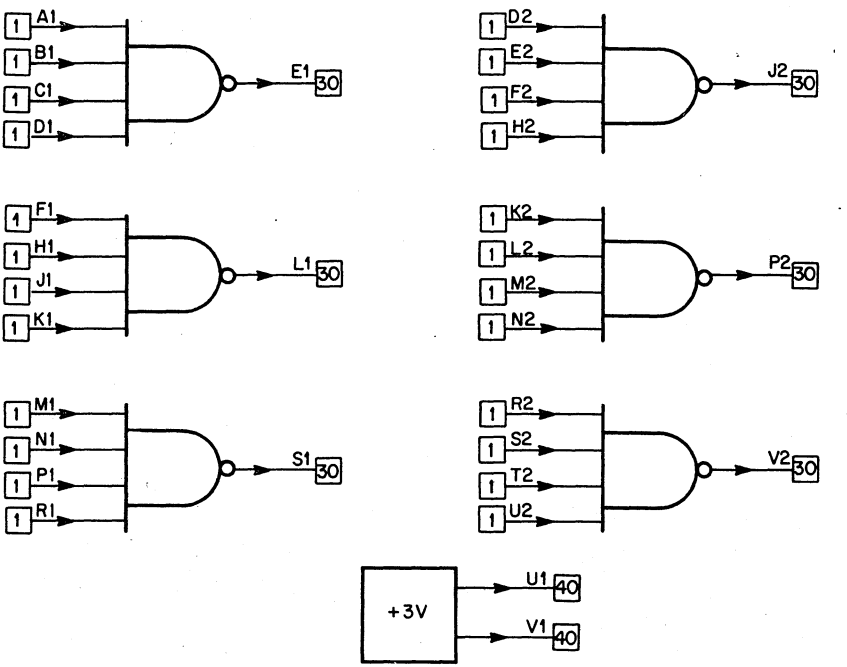
LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$26



Volts	Power mA (max.)	Pins
+5	97	A2
GND		C2, T1

The M617 contains 6 four-input NAND gates each capable of driving up to 30 unit loads.

FUNCTIONS

Physical configuration and logical operation are identical to the M117.

SPECIFICATIONS

Typical gate propagation delay is 15 ns.

M627
NAND POWER AMPLIFIER

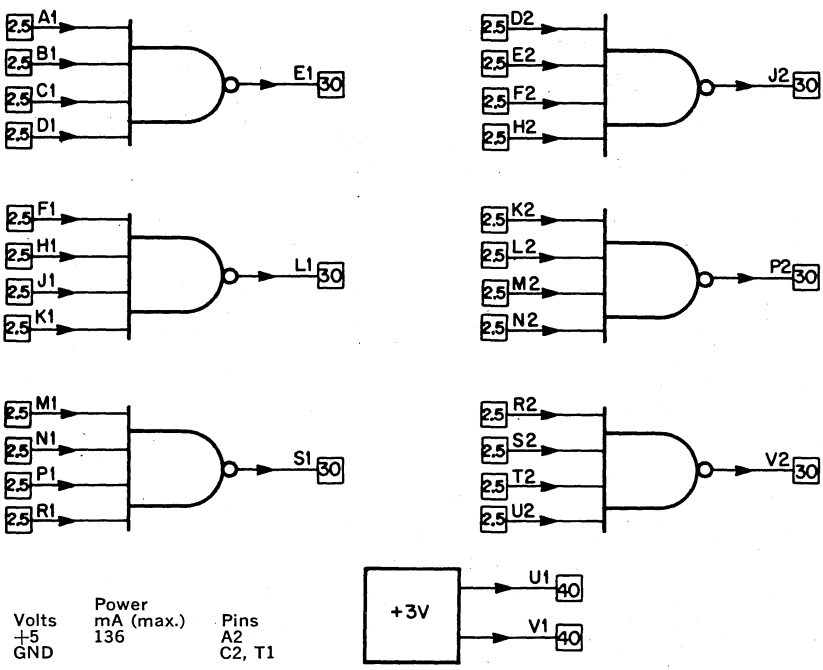
LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$29



Volts	Power mA (max.)	Pins
+5	136	A2
GND		C2, T1

The M627 provides six 4-input NAND gates that combine power amplification with high-speed gating.

APPLICATIONS

For high fan-out of clock or shift pulses to expanded counters and shift registers.

PRECAUTIONS

1. In pulse amplifier applications, unused inputs should be connected to the +3 volt pins provided.
2. To utilize the timing accuracy of this module, wire runs of minimum length are recommended.

SPECIFICATIONS

Propagation Time: Typically 6 ns between input and output transitions.

M660
POSITIVE LEVEL CABLE DRIVER

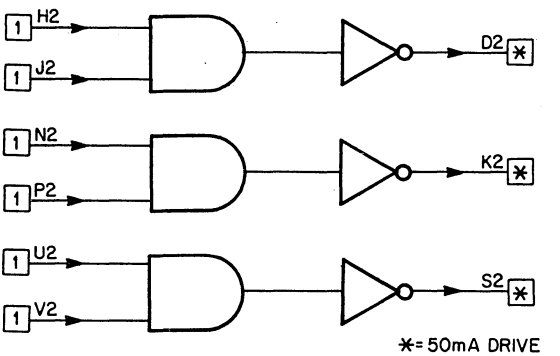
LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$25



Volts	Power mA (max.)	Pins
+5	71	A2
GND		C2

The M660 Cable Driver consists of three NAND gate circuits each of which will drive a 100-ohm terminated cable with M Series levels or pulses of duration greater than 100 ns.

SPECIFICATIONS

Outputs: Can sink 50 mA at a logic LOW, and can source 50 mA at a logic HIGH.

M661
POSITIVE LEVEL DRIVER

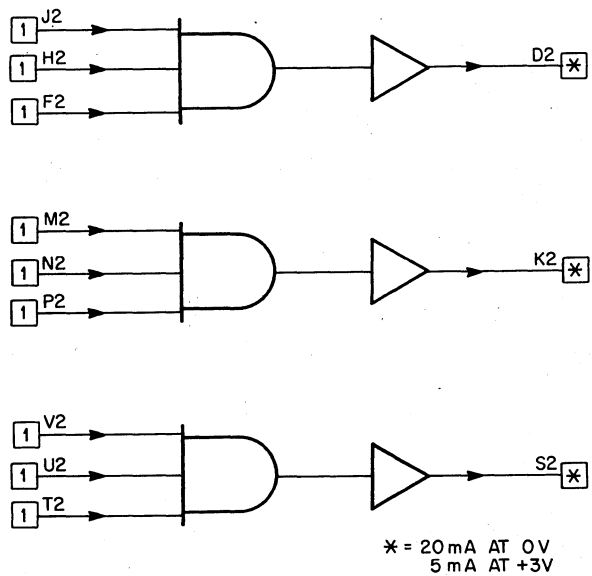
LOGIC AMPLIFIERS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$15



Volts	Power mA (max.)	Pins
+5	111	A2
GND		C2

The M661 contains three AND circuits which may be used to drive low impedance unterminated cable with M Series logic levels or pulses of duration greater than 100 ns.

SPECIFICATIONS

Outputs: Can sink 20 mA at a logic LOW, and can source 5 mA at a logic HIGH.

M671
M TO K CONVERTER

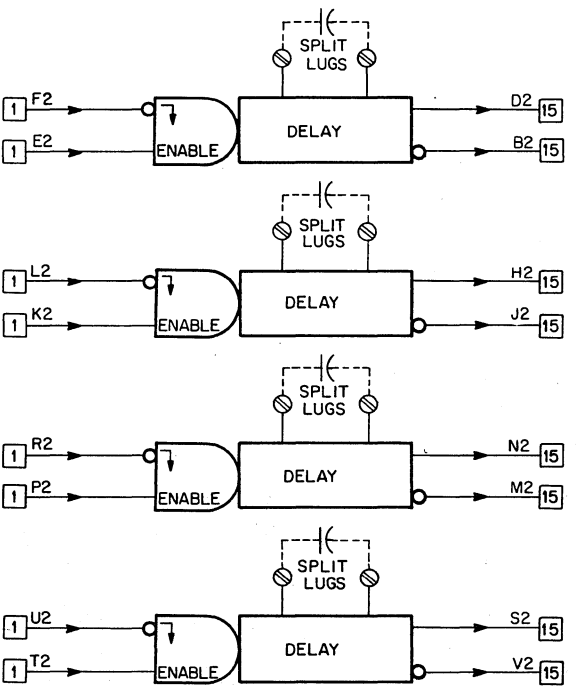
TIME RELATED

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$52

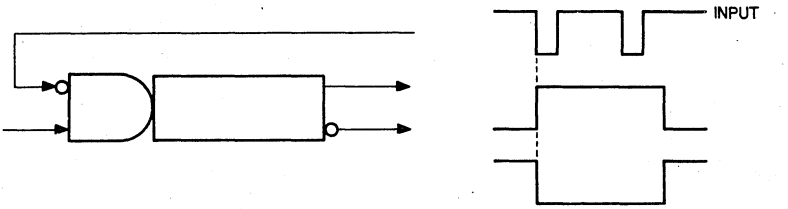


Volts	Power mA (max.)	Pins
+5	112	A2
GND		C2

The M671 M Series to K Series Converter contains four pulse stretching circuits which can convert an M Series input pulse of duration exceeding 50 ns to complementary K Series output pulses of 10 to 15 μs.

FUNCTIONS

Triggering: When the ENABLE input is HIGH, the delay is triggered by the negative-going edge of the trigger input pulse:



This circuit is insensitive to input transitions during its timeout period as shown in the example above.

Increasing Output Pulse Width: Non-electrolytic capacitors can be connected to the split lugs provided in each circuit if K Series output pulse widths longer than 15 μs are desired. Pulses of up to 40 seconds are possible using this technique. When capacitance is added, the output pulse width is increased by 6400 C seconds where C is the capacitance added in farads.

Precautions: Unused inputs should be connected to logic levels that will hold them in their unasserted states. Unused inputs that would be asserted High should be grounded. Unused inputs that would be asserted Low should be connected to a source of logic High. Also refer to "Unused Inputs" in the alphabetical index.

SPECIFICATIONS

Output drive: Each output is capable of driving a 15 mA load.

M706
TELETYPE RECEIVER

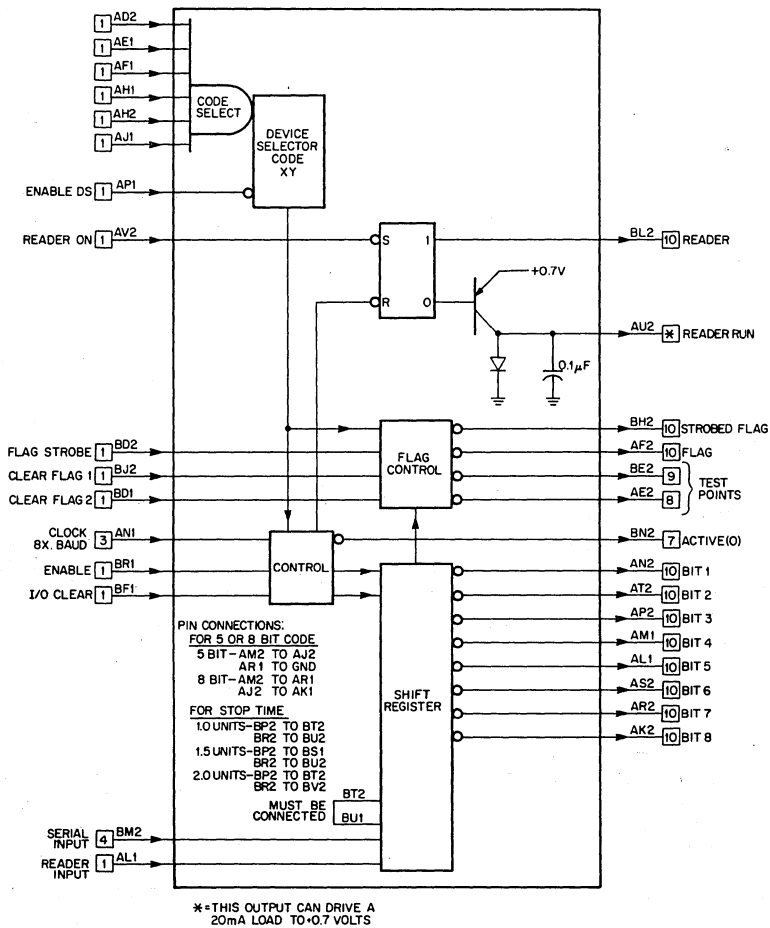
MISCELLANEOUS

M SERIES

Length: Standard
Height: Double
Width: Single

Price:

$150



Volts	Power mA (max.)	Pins
+5	400	AA2, BA2
GND		AC2, AT1, BC2, BT1

The M706 Teletype Receiver is a serial-to-parallel teletype code converter self contained on a double height module. This module includes all of the serial-to-parallel conversion, buffering, gating, and timing (excluding only an external clock necessary to transfer information in an asynchronous manner between a serial data line or teletype device and a parallel binary device). Either a 5-bit serial character consisting of 7.0, 7.5, or 8.0 units or an 8-bit serial character of 10.0, 10.5, or 11.0 units can be assembled into parallel form by the M706 through the use of different pin connections on the module. When conversion is complete, the start and stop bits accompanying the serial character are removed. The serial character is expected to be received with the start bit first, followed by bits 1 through 8 in that order, and completed by the stop bits. Coincident with reception of the center of bit eight, the Flag output goes low indicating that a new character is ready for transmission into the parallel device. The parallel data is available at the Bit 1 through Bit 8 outputs until the beginning of the start bit of a new serial character as received on the serial input. See the timing diagram of Figure 1 for additional information.

In addition to the above listed features, the M706 includes the necessary logic to provide rejection of spurious start bits less than one-half unit long, and half-duplex system operation in conjunction with the M707. Device selector gating is also provided so that this module can be used on the positive I/O bus of either the PDP8/I or the PDP8/L. To obtain additional applications information on the M706, write for Applications Note AP-M-013.

Inputs: All inputs present one TTL unit load except where noted. When input pulses are required, they must have a width of 50 nsec or greater.

Clock: The clock frequency must be eight times the serial input bit rate (baud rate). This input can be either pulses or a square wave. Input loading on the clock line is three unit loads.

Enable: This input when brought to ground will inhibit reception of new characters. It can be grounded any time during character reception, but returned high only between the time the Flag output goes to ground and a new character start bit is received at the serial input. When not used this input should be tied to a source of +3 Volts.

I/O Clear: A high level or positive pulse at this input clears the Flag and initializes the state of the control. When not used, or during reception, this input should be at ground.

Code Select Inputs: When a positive AND condition occurs at these inputs the following signals can assume their normal control functions—Flag Strobe, Read Buffer, and Clear Flag 1. Frequently these inputs might be used to multiplex receiver modules when a signal like Read Buffer is common to many modules. The inputs can also be used for device Selector inputs when the M706 is used on the positive I/O bus of the PDP8/I or PDP8/L. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If it is desired to bypass the code select inputs, they can be left open and the Enable D.S. line tied to ground.

Clear Flag 1: A high level or positive pulse at this input while the code select inputs are all high, will clear the Flag. When not used, this line should be grounded. Propagation delay from input rise until the Flag is cleared is a maximum of 100 nsec. The Flag cannot be set if this input is held high.

Clear Flag 2: A high level or positive pulse at this input, independent of the state of the code select inputs, will clear the Flag. All other characteristics are identical to those of Clear Flag 1.

Flag Strobe: If the Flag is set, and the code select inputs are all high, a positive pulse at this input will generate a negative going pulse at the Strobed Flag output. Propagation delay from the strobe to output is a maximum of 30 nsec.

Read Buffer: A high level or positive pulse at this input while the code select inputs are all high will transfer the state of the shift register to outputs Bit 1 through Bit 8. Final parallel character data can be read by this input as soon as the Flag output goes to ground. Output data will be available a maximum of 100 nsec after the rising edge of this input. See the timing diagram of Figure 1 for additional information.

Reader On: A low level or ground at this input will turn the internal reader flip-flop on. This element is turned off at the beginning of a received character start bit. This input can also be pulsed by tying it to one of the signals derived at output pins AE2 or BE2. A low output will exist at pin BE2 if the M706 is addressed and the clear Flag 1 (pin BJ2) is high. A low output will exist at pin AE2 if the M706 is addressed and the Clear Flag 1 (pin BJ2) is high or if Clear Flag 2 (pin BD1) is high.

Serial Input: Serial data received on this input is expected to have a logical zero (space) equal to +3 Volts and a logical 1 (mark) of ground. The input receiver on the M706 is a schmitt trigger with hysterisis thresholds of nominally 1.0 and 1.7 Volts so that serial input data can be filtered up to 10% of bit width on each transition to remove noise. This input is diode protected from voltage overshoot above +5.9 Volts and undershoot below —0.9 Volts. Input loading is four unit loads.

Outputs: All outputs can drive ten unit loads unless otherwise specified.

Bits 1 through 8: A read Buffer input signal will transfer the present shift register contents to these outputs with a received logical 1 appearing as a ground output. If the Read Buffer input is not present, all outputs are at logical 1. When the M706 is used for reception of 5-bit character codes, the ouput data will appear on output lines Bit 1 through 5 and bits 6, 7, 8 will have received logical zeros.

Active (0): This output goes low at the beginning of the start bit of each received character and returns high at the completion of reception of bit 8 for an 8-bit character or of bit 5 for a 5-bit character. Since this signal uses from ground to +3 Volts one-half bit time after the Flag output goes to ground, it can be used to clear the flag through Clear Flag 2 input while the Flag Output after being inverted can strobe parallel data out when connected to Read Buffer.

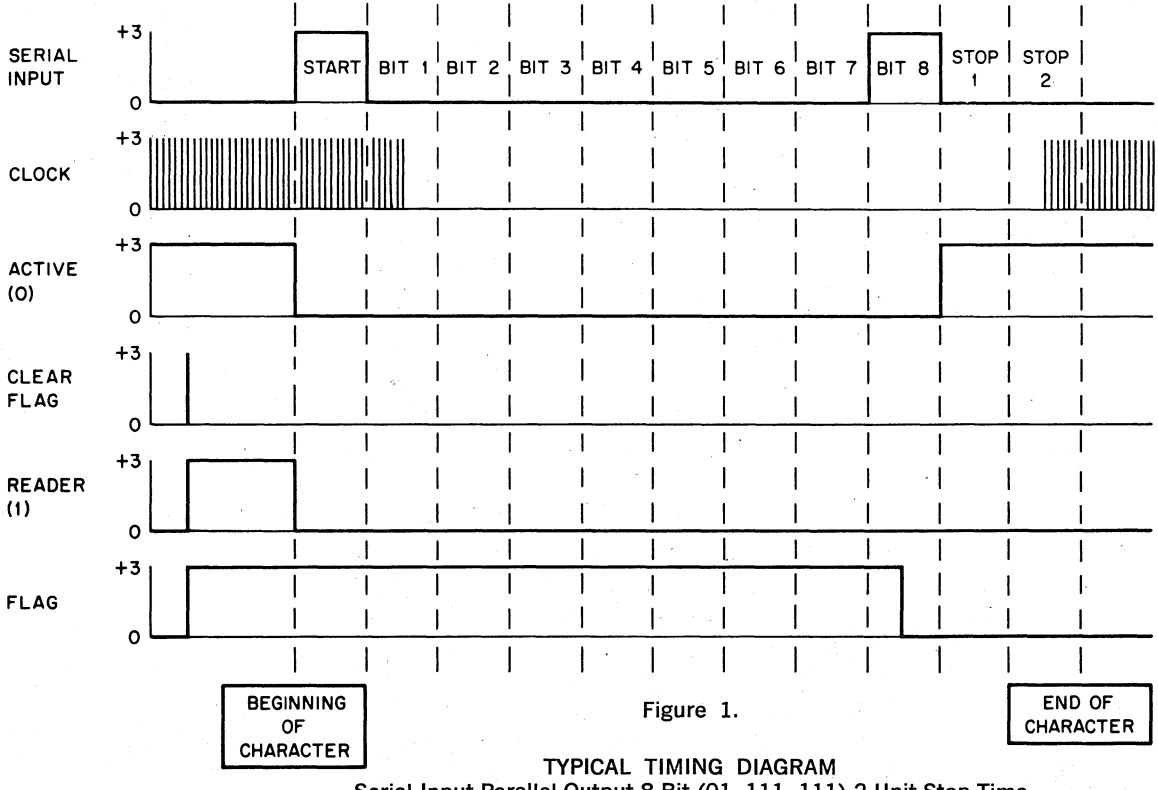


Figure 1.

TYPICAL TIMING DIAGRAM
Serial Input-Parallel Output 8-Bit (01, 111, 111)-2 Unit Stop Time

If an M706 and M707 are to be used in half duplex mode, this output should be tied to the Wait input of the M707 to inhibit M707 transmission during M706 reception. Output drive is eight unit loads.

Flag: This output falls from +3 Volts to ground when the serial character data has been fully converted to parallel form. Relative to serial bit positions, this time occurs during the center of either bit 8 or bit 5 depending respectively on the character length. If the M706 is receiving at a maximum character rate, i.e. one character immediately follows another; the parallel output data is available for transfer from the time the Flag output falls to ground until the beginning of a new start bit. This is Stop bit time plus one-half bit time.

Strobed Flag: This output is the NAND realization of the inverted Flag output and Flag Strobe.

Reader (1): Whenever the internal reader flip-flop is set by the Reader ON input, this output rises to +3 Volts. It is cleared whenever a start bit of a new character received on the serial input.

Reader Run: For use with Digital modified ASR33 and ASR35 teletypes which have relay controlled paper tape readers. This output can drive a 20 ma at +0.7 Volts load. The common end of the load can be returned to any negative voltage not exceeding —20 Volts.

Pin AE2: This output is the logical realization of NOT (Clear Flag 1 or Clear Flag 2 or I/O Clear) and is a +3 Volts to ground output level or pulse depending on the input. This signal can be used to pulse Reader On for control of Reader Run as used in DEC PDP8/I or PDP8/L computers.

Pin BE2: This output is brought from +3 Volts to ground by an enabled Clear Flag 1 input. It can be connected to Reader On for a different form of control of Reader Run.

M707
TELETYPE TRANSMITTER

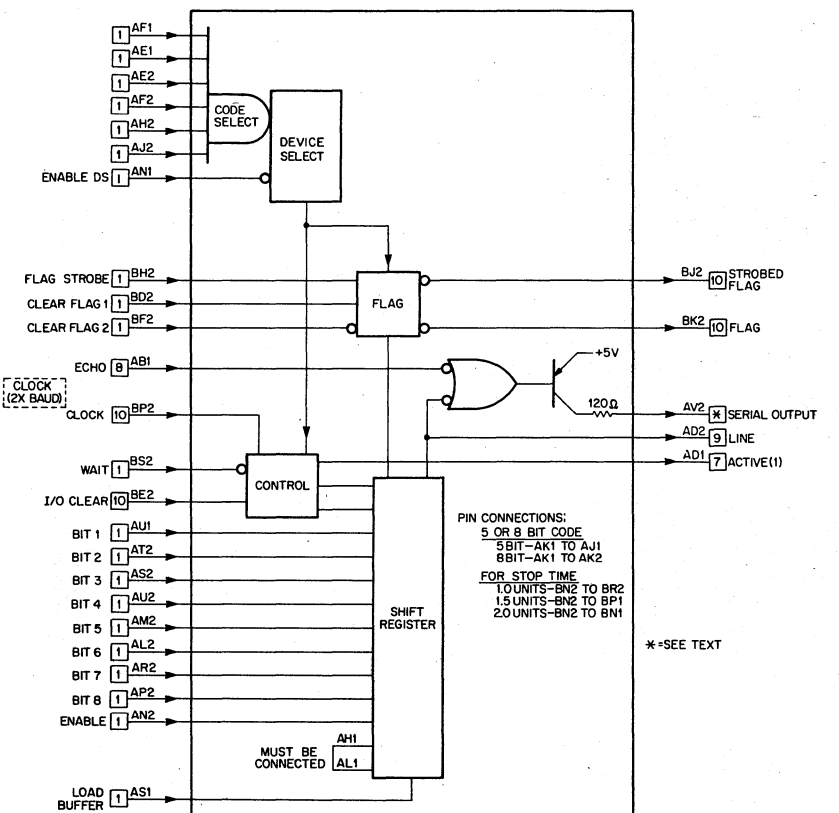
MISCELLA-NEOUS

M SERIES

Length: Standard
Height: Double
Width: Single

Price:

$150



Volts	Power mA (max.)	Pins
+5	375	A2
GND		C2, T1

The M707 Teletype Transmitter is a parallel-to-serial teletype code converter self contained on a double height module. This module includes all of the parallel-to-serial conversion, buffering, gating, and timing (excluding only an external clock) necessary tot ransfer information in an asynchronous manner between a parallel binary device and a serial data line or teletype device. Either a 5-bit or an 8-bit parallel character can be assembled into a 7.0, 7.5, or 8.0 unit serial character or a 10.0, 10.5, or 11.0 unit serial character by the M707 through the use of different pin connections on the module. When conversion is complete, the necessary start bit and selected stop bits (1.0, 1.5, or 2.0 units) have been added to the original parallel character and transmitted over the serial line. The serial character is transmitted with the start bit first, followed by bits 1 through 8 in that order, and completed by the stop bits. Coincident with the stop bit being put on the serial line, the Flag output goes low indicating that the previous character has been transmitted and a new parallel character can be loaded into the M707. Transmission of this new character will not occur until the stop bits from the previous character are completed. See the timing diagram of Figure 1 for additional information.

In addition to the above listed features, the M707 includes the necessary gating so that it can be used in a half-duplex system with the M706. Device selector gating is also provided so that this module can be used on the positive bus of either the PDP8/I or the PDP8/L. To obtain additional applications information on the M707 write for Applications Note AP-M-013.

Inputs: All inputs present one TTL unit load with the exception of the Clock input which presents ten unit loads. Where the use of input pulses is required, they must have width of 50 nsec or greater.

Clock: The clock frequency must be twice the serial output bit rate. This input can be either pulses or a square wave.

Bits 1 through 8: A high level at these inputs is reflected as a logic 1 or mark in the serial output. When a 5-bit code is used, bit inputs 1 through 5 should contain the parallel data, bit 6 should be considered as an Enable, and bits 7, 8 and Enable should be grounded.

Enable: This input provides the control flexibility necessary for transmitter multiplexing. When grounded during a Load Buffer pulse, this input prevents transmission of a character. It can be driven from the output of an M161 for scanning purposes or in the case of a single transmitter, simply tied to +3 Volts.

Wait: If this input is grounded prior to the stop bits of a transmitted character, it will hold transmission of a succeeding character until it is brought to a high level. A ground on this line will not prevent a new character from being loaded into the shift register. This line is normally connected to Active (0) on a M706 in half duplex two wire systems. When not used, this line should be tied to +3 Volts.

Code Select Inputs: When a positive AND condition occurs at these inputs the following signals can assume their normal control functions—Flag Strobe, Load Buffer, and Clear Flag 1. Frequently these inputs might be used to multiplex transmitter modules when signals like Load Buffer are common to many modules. These inputs can also be used for device selector inputs when the M707 is used on the positive bus of the PDP8/I or PDP8/L. The

code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If it is desired to by-pass the code select inputs, they can be left open and the Enable DS line tied to ground.

Clear Flag 1: A high level or positive pulse at this input while the code select inputs are all high, will clear the Flag. When not used, this line should be grounded. Propagation delay from input rise until the Flag is cleared at the Flag output is a maximum of 100 nsec. The Flag cannot be set if this input is held at logic 1.

Clear Flag 2: A low level or negative pulse at this input will clear the Flag. When not used this input should be tied to +3 Volts. The Flag will remain cleared if this input is grounded. Propagation from input fall to Flag output rise is a maximum of 80 nsec. If it is desired to clear the flag on a load buffer pulse, Clear Flag 2 can be tied to pin AR1 of the module.

Flag Strobe: If the Flag is set, and the code select inputs are all high, a positive pulse at this input will generate a negative going pulse at the Strobed Flag output. Propagation delay from the strobe to output is a maximum of 30 nsec.

I/O Clear: A high level or positive pulse at this input clears the Flag, clears the shift register and initializes the state of the control. This signal is not necessary if the first serial character transmitted after power turn-on need not be correct. When not used, or during transmission, this input should be at ground.

Load Buffer: A high level or positive pulse at this input while the code select inputs are all high will load the shift register buffer with the character to be transmitted. If the Enable input is high when this input occurs, transmission will begin as soon as the stop bits from the previous character are counted out. If a level is used, it must be returned to ground within one bit time (twice the period of the clock).

Outputs: All outputs present TTL logic levels except the serial output driver which is an open collector PNP transistor with emitter returned to +5 Volts.

Serial Output: This open collector PNP transistor output can drive 20 mA into any load returned to a voltage between +4 Volts and −15 Volts. A logical output or mark is +5 Volts and a logical 0 or space is an open circuit. If inductive loads are driven by this output, diode protection must be provided by connecting the cathode of a high speed silicon diode to the output and the diode anode to the coil supply voltage.

Line: This output can drive ten TTL unit loads and presents the serial output signal with a logical 1 as +3 Volts and logical 0 as ground.

Active: During the time period from the occurrence of the serial start bit and the beginning of the stop bits, this output is high. This signal is often used in half duplex systems to obtain special control signals. Output drive is eight TTL unit loads.

Flag: This output falls from +3 Volts to ground at the beginning of the stop bits driving a character transmission. The M707 can now be reloaded and the Flag cleared (set to +3 Volts). This output can drive ten TTL unit loads.

Strobed Flag: This output is the NAND realization of the inverted Flag output and Flag Strobe. Output drive is ten TTL unit loads.
+3 Volts: Pin BJ1 can drive ten TTL unit loads at a +3 Volts level.

Power: +5 Volts at 375 mA. (max.)

Size: Standard, double height, single width FLIP CHIP module.

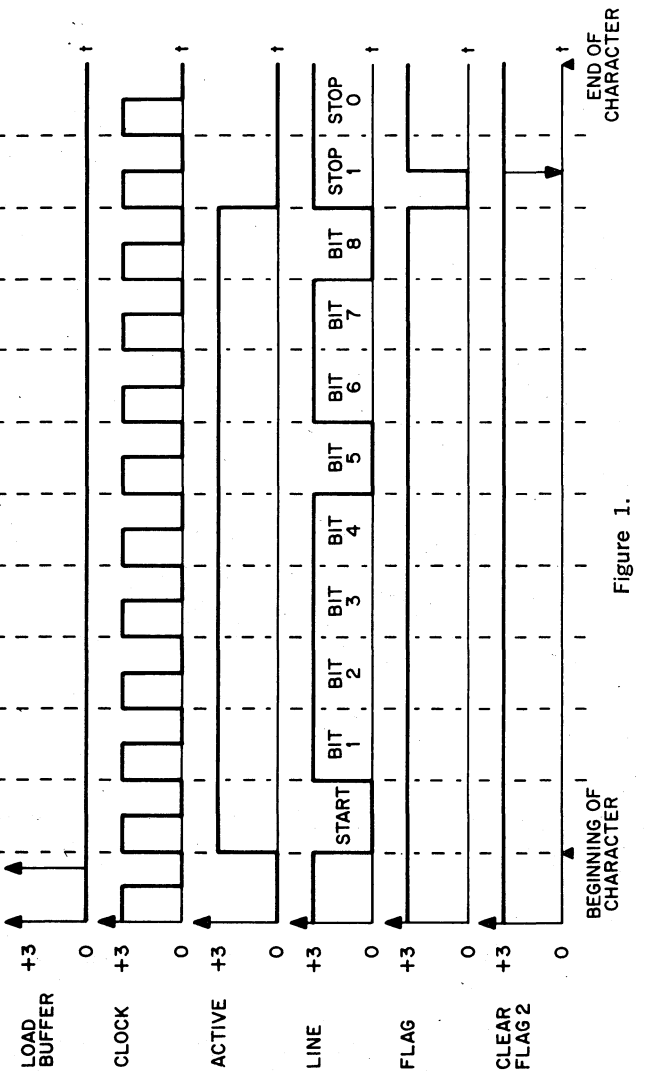


Figure 1.
Typical Timing Diagram, Parallel input, 8-Bit Character (11, 110, 110) With two bit Stop time.

M906
CABLE TERMINATOR

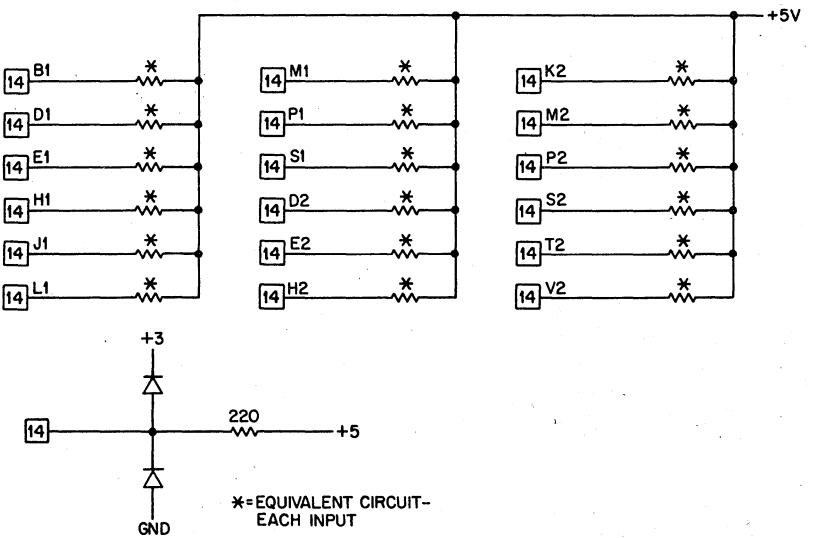
MISCELLANEOUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$20



Volts	Power mA (max.)	Pins
+5	440*	A2
GND**		A1, C1, F1, K1, N1, R1, T1 C2, F2, J2, L2, N2, R2, U2

* all signal lines grounded
** all ground pins must be grounded

The M906 cable terminator module contains 18 load resistors which are clamped to prevent excursions beyond +3 volts and ground. It may be used in conjunction with M623 to provide cable driving ability similar to M661 using fewer module slots.

APPLICATIONS

The M906 may be used to terminate inputs. In this configuration M906 and M111 are a good combination.

This module is normally used with standard M Series levels of 0 and +3 volts to partially terminate 100-ohm cable. It presents a load of 22.5 mA or 14 TTL unit loads at ground and, therefore, must be driven from at least an M116-type circuit or, preferably, a cable driver.

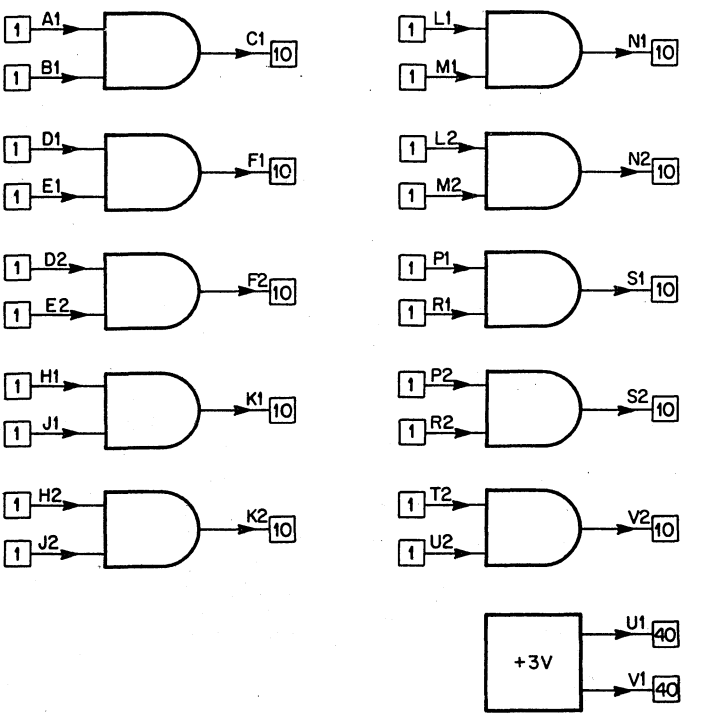
M1103
TWO-INPUT AND GATES

GATES

M SERIES

Length: Standard
Height: Single
Width: Single

Price:
$14



Volts	Power mA (max.)	Pins
+5	80	A2
GND		C2, T1

The M1103 contains ten 2-input AND gates. Unused inputs on any gate must be returned to a source of logic HIGH for maximum noise immunity. Two pins are provided (U1 and V1) as a source of +3 volts for this purpose.

APPLICATIONS

- Positive AND or negative OR gating

M1307
FOUR-INPUT AND GATES

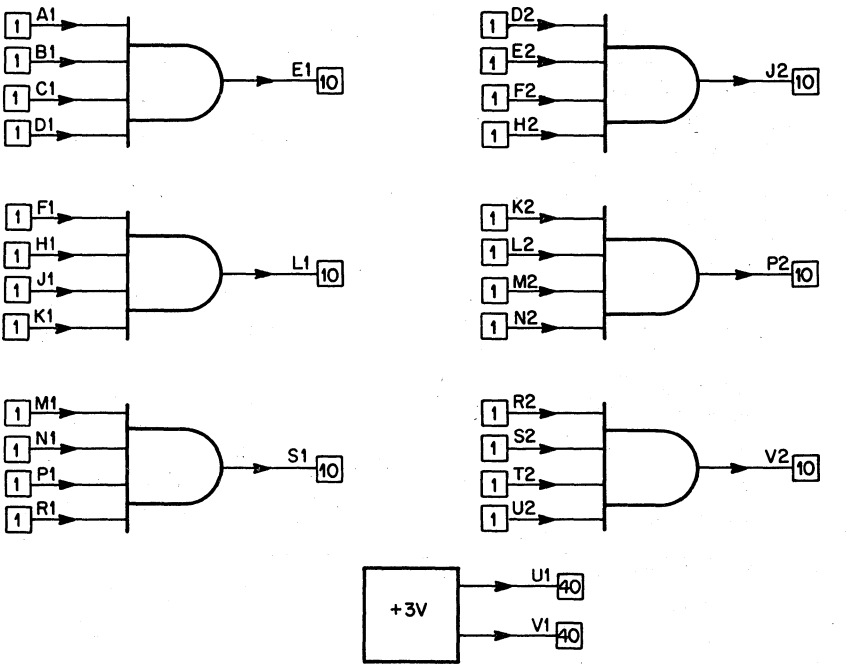
GATES

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$12



Volts	Power mA (max.)	Pins
+5	100	A2
GND		C2, T1

The M1307 contains six high speed 4-input AND gates. Unused inputs on any gate must be returned to a source of logic HIGH for maximum noise immunity. Two pins are provided (U1 and V1) as a source of +3 volts for this purpose.

APPLICATIONS

- Positive AND or negative OR gating

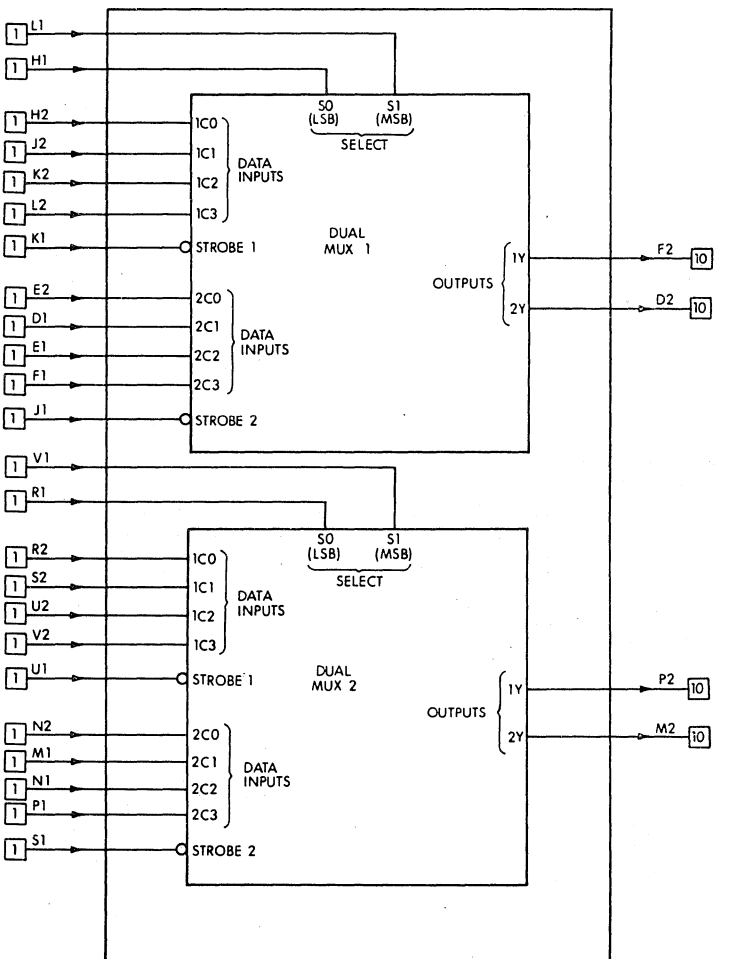
M1701
DATA SELECTOR

GATES

M SERIES

Length: Standard
Height:
Width: Single

Price
$17



Volts	Power mA (max.)	Pins
+5	110	A2
GND		C2, T1

The M1701 Data Selector contains two independent dual 4-line to 2-line multiplexers on a single-height module. Each dual multiplexer has two groups of DATA INPUTS, two STROBES, two OUTPUTS and common SELECT inputs. An OUTPUT becomes active for a DATA INPUT when the DATA INPUT is addressed by the SELECT lines and the corresponding STROBE brought LOW.

APPLICATIONS

- Multiplexing for parallel-to-serial conversion
- Timesharing
- Sampling

TRUTH TABLE

FUNCTIONS

SELECT		DATA INPUTS					
S1	S0	C3	C2	C1	C0	STROBE	OUTPUT Y
X	X	X	X	X	X	H	L
L	L	X	X	X	L	L	L
L	L	X	X	X	H	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
H	H	L	X	X	X	L	L
H	H	H	X	X	X	L	H

X = irrelevant

PROPAGATION DELAY TIMES

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MAX	UNIT
t_{PLH}	Data	Y	25	ns
t_{PHL}	Data	Y	30	ns
t_{PLH}	Address	Y	40	ns
t_{PHL}	Address	Y	40	ns
t_{PLH}	Strobe	Y	35	ns
t_{PHL}	Strobe	Y	30	ns

t_{PLH} = propagation delay time, Low-to-High-level output.
t_{PHL} = propagation delay time, High-to-Low-level output.

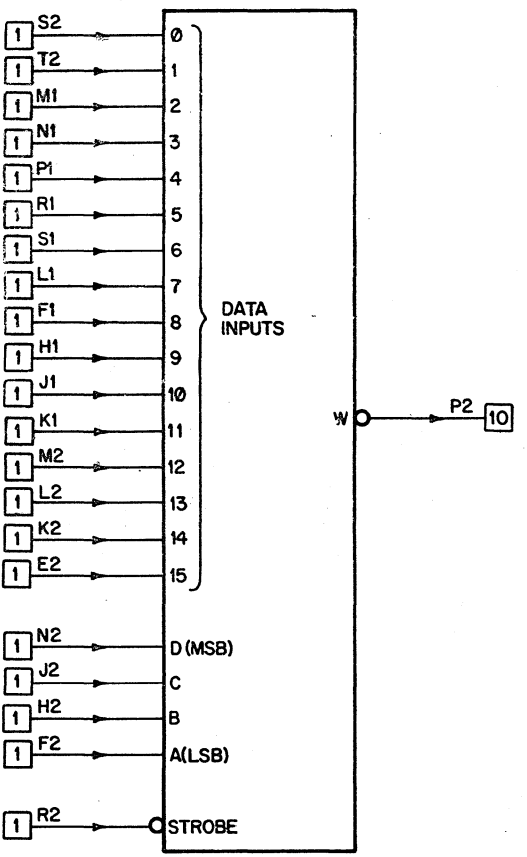
M1713
16-LINE TO 1-LINE DATA SELECTOR

NUMERIC

M SERIES

Length: Standard
Height: Single
Width: Single

Price
$13



Volts	Power mA (max.)	Pins
+5	70	A2
GND		C2, T1

The M1713 module is a 1-of-16 data selector/multiplexer. Its operation can best be described by the following **TRUTH TABLE:**

					INPUTS															OUTPUT
D	C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	H
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	L
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	H
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	L
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	H
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	L
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	H
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	L
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	H
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	L
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	H
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	L
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	H
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	L
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	H
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	L
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	H
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	L
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	H
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	L
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	H
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	L
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	H
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	L
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	H
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	L
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	H
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	L

When used to indicate an input condition, X = High or Low

SPECIFICATIONS

Propagation Delay

FROM:	TO:
Input A, B, C, D	Output W = 50 ns (max)
STROBE	Output W = 40 ns (max)
D0 through D15	Output W = 30 ns (max)

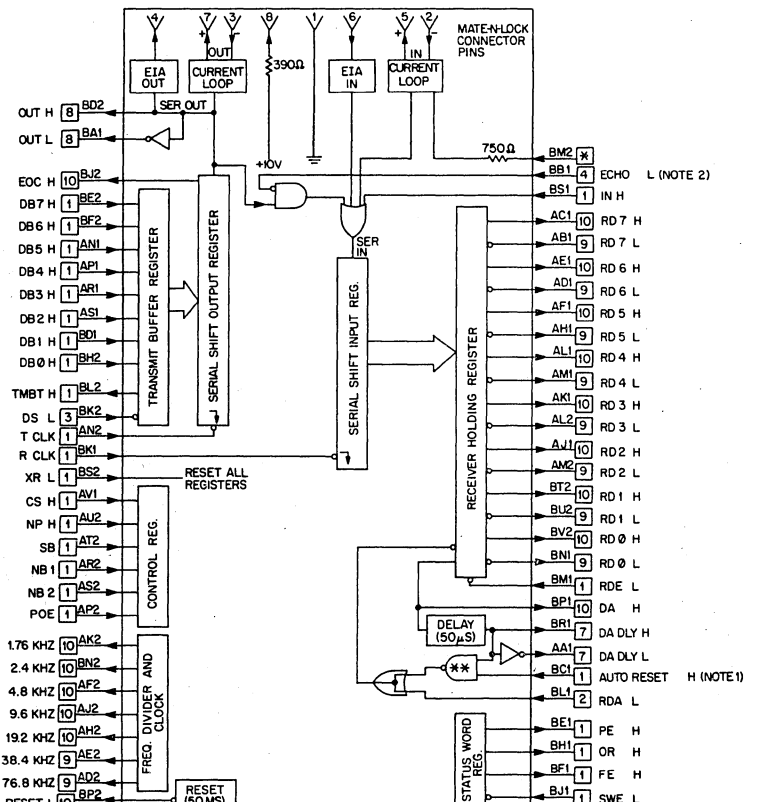
M7390
ASYNCHRONOUS TRANSCEIVER

MISCELLA-NEOUS

M SERIES

Length: Extended
Height: Double
Width: Single

Price: $275



NOTES: *=TIED TO -15V WHEN M7390 USED TO DRIVE CURRENT LOOP
**=OPEN COLLECTOR OUTPUT
1. MUST BE TIED TO GROUND IF RDA L NOT USED
2. MAY BE LEFT OPEN IF ECHO NOT DESIRED

Volts	Power mA (max.)	Pins
+5	700	BA2
+10	3	AV2
GND		BC2
−12*	80	BR2
−15*	80	BB2

*Requires −12 V or −15 V only, not both.

DESCRIPTION

The M7390 asynchronous transceiver is a modular subsystem which provides asynchronous serial line compatibility for data communications applications. The M7390 combines input/output level converters, parallel-to-serial and serial-to-parallel conversion, and a crystal controlled clock, into one module.

APPLICATIONS

The M7390 can be used for computer terminal applications, data entry devices or any system which requires asynchronous serial line compatibility. The M7390 may also be used to drive modems conforming to EIA RS-232C specifications or current-operated devices such as Teletypes.

FUNCTIONS

There are three groups of functions on the M7390—error detection, data, and control.

Error Detection: The error function of the module allows three types of errors to be detected. These are:

1. Parity: If the received parity bit does not agree with the expected parity bit, the parity error flag is set.
2. Overrun: The receiver section of the M7390 is fully double buffered. Therefore, one full character time is allowed to remove the received data from the receiver buffer before a new character is assembled and transferred. If the character is not removed before a new one is loaded, the overrun flag is set.
3. Framing: Since the M7390 is asynchronous, the absence of a stop bit can be detected. For example, an eight bit data character would have one start bit, eight data bits, and one or two stop bits. Therefore, a stop bit is expected as the 10th bit to be received. If the 10th bit is in the logic TRUE (marking) condition no error is detected. However, if the 10th bit is a logic FALSE (spacing) condition, the framing error flag is set. The framing error flag is useful for detecting open lines or null characters.

Data Functions: The M7390 performs serial-to-parallel and parallel-to-serial conversion. The parallel side of the module is TTL compatible. The serial inputs and outputs are available as three signal sources: EIA, current loop or TTL. The current loop and EIA input and output are available only on the eight-pin MATE-N-LOK connector on the front of the module.

The EIA input corresponds to RS-232C specifications. In addition to the EIA signals RECEIVED DATA and TRANSMITTED DATA, the DATA TERMINAL READY signal and SIGNAL GROUND are also provided.

The current loop input/output is designed to operate on a 20 to 100 mA current loop. The M7390 uses optical couplers to provide 1500 volts of isolation between the M7390 ground and power and the driving source. The serial input will respond to a 20 mA current flow. Current flow is a marking condition (binary 1). The external source must not exceed 35 volts dc open circuit voltage or 100 mA current. The serial output is a transistor switch that can turn a current loop on or off. The open circuit voltage of the current source must not exceed 35 volts dc.

The TTL versions of the serial input and output signals are available on the module pins and may be used in place of the level converter signals.

Control: The M7390 provides full control of the receiver and transmitter sections. All control pulses must be greater than 250 ns in width. Data to be loaded into the module must be present 250 ns before the DATA STROBE pulse.

Receiver Control Signals:

DA	Data Available
DA DLY	Delayed Data Available
AUTO RESET	Allows DA to be automatically reset.
RDE	Receiver Data Enable. Places data and control signals on the pins of the module.
RDA	Reset Data Available

Transmitter Control Signals:

TBMT	Transmitter Buffer Empty
ECO	End of Character

Error Control and other Signals:

NP	No Parity
POE	Parity Odd or Even
SWE	Status Word Enable
CS	Control Strobe
NB1, NB2	Number of Bits in data word
SB	Number of Stop Bits (1 or 2)
XR	External Reset (clears all registers)
RESET	Negative pulse used for clearing module during power-up.
RCLK	Receiver Clock Input
TCLK	Transmitter Clock Input

PRECAUTIONS

1. EIA and current loop connections are available on an 8-pin MATE-N-LOK connector located in the handle position on the B half of the board.
2. Provision is made to power this module from either −15 or −12 volts dc. Do not use both simultaneously.
3. Current loop input and output circuits must not have more than 35 volts peak applied or greater than 100 mA current flow.
4. The M7390 contains an MOS LSI chip. Care must be taken in proper handling and grounding of the module to prevent damage to the MOS chip.
5. The +10 volt dc supply is required only if the EIA level converters are used, or if the module is going to be used as a current source.
6. If the M7390 is used as a current source, 20 mA additional current must be supplied by the −15 volt and the +10 volt power supplies.

SPECIFICATIONS

Data Format: Asynchronous, serial by bit, least significant bit first.
Input/Output Level (Serial):

1. EIA RS-232C: Binary 1 = −3 to −25 volts dc
   Binary 0 = +3 to +25 volts dc
2. Current Loop: Mark (Binary 1) = 20 to 100 mA current flow
   Space (Binary 0) = <3 mA current flow
3. TTL: Binary 1 = HIGH
   Binary 0 = LOW

Data Rates: 110, 150, 300, 600, 1200, 2400, 4800 Baud.

Character Format: One start, 5, 6, 7, 8 data, parity (if requested), one or two stop bits.

Clock Frequencies (kHz): 1.76, 2.4, 4.8, 9.6, 19.2, 38.4, 76.8

Input/Output Levels (Parallel): All TTL compatible.

MORE INFORMATION

Additional information is available by writing to:

Logic Products Applications Group
Digital Equipment Corporation
146 Main Street
Maynard, Mass. 01754

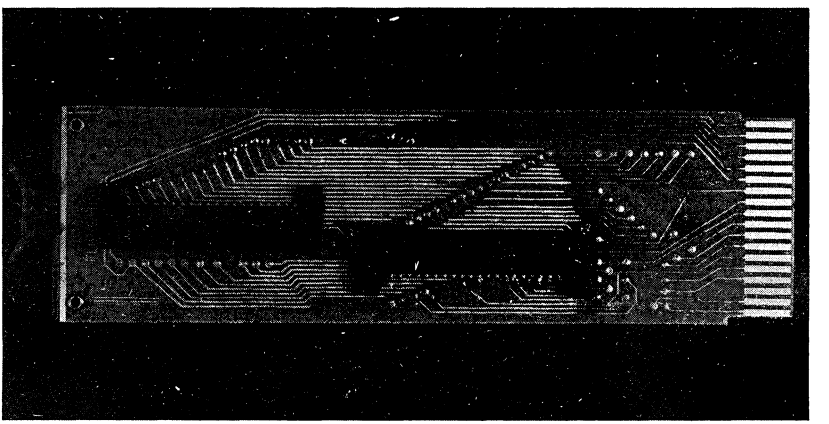
M9100
H854 TO H854 TO
FLIP CHIP ADAPTER

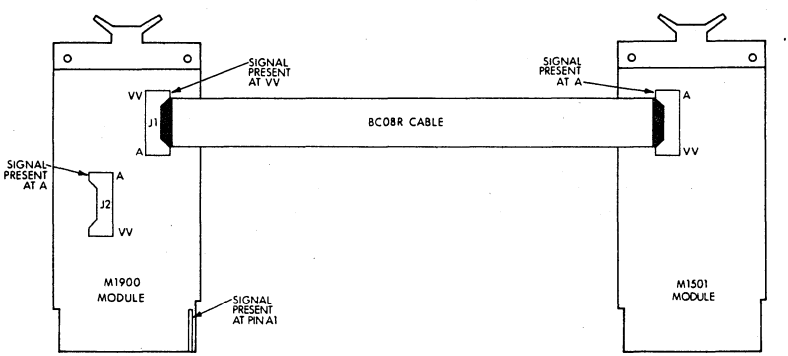
MISCELLA-
NEOUS

M SERIES

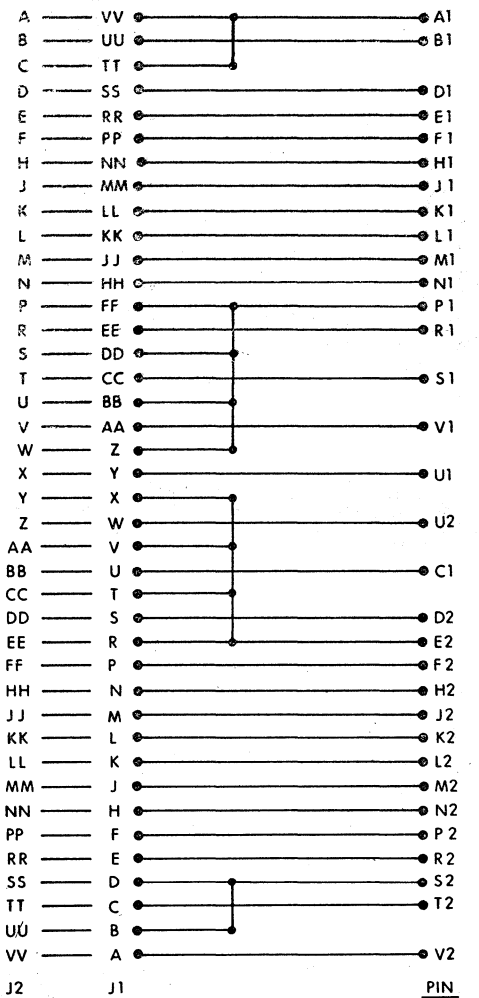
Length: Extended
Height: Single
Width: Single

Price
$30



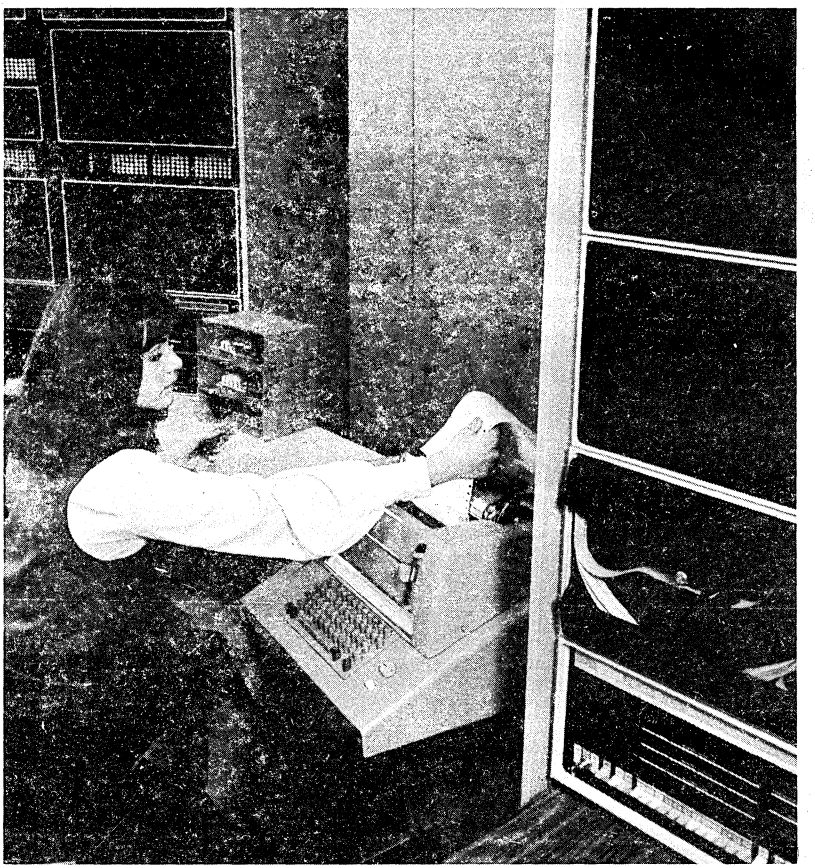


The M9100 can be used with any cable that has an H856 conductor on one or both ends, such as the BC08J, BC08K, BC08R, or the BC04Z series. Signals coming from or going to an external device will usually plug into J2. While, signals coming from or going to an interfacing module will usually plug into J1. The M9100 is simply a "T" or "Y" type adapter where as many signal lines as possible are handled separately. Because the FLIP CHIP connector (i.e. module fingers) is limited to 32 independent lines, several of the 40 lines available on the H854's that are usually used for ground connections have been wired together on the adapter. To allow the user the greatest flexibility, none of the signal lines are preconnected to either ground or power pins on the FLIP CHIP connector.


A VV A1
B UU B1
C TT
D SS D1
E RR E1
F PP F1
H NN H1
J MM J1
K LL K1
L KK L1
M JJ M1
N HH N1
P FF P1
R EE R1
S DD
T CC S1
U BB
V AA V1
W Z
X Y U1
Y X
Z W U2
AA V
BB U C1
CC T
DD S D2
EE R E2
FF P F2
HH N H2
JJ M J2
KK L K2
LL K L2
MM J M2
NN H N2
PP F P2
RR E R2
SS D S2
TT C T2
UU B
VV A V2
J2
J1
PIN

m series

modules for computer interfacing



M SERIES MODULES FOR COMPUTER INTERFACING

Design and support of interfaces for the PDP computers is a growing function of M Series logic. This edition of the Logic Handbook emphasizes a collection of modules for interfacing to the PDP-8/e, 8/m OMNIBUS or external I/O bus, the PDP-11 UNIBUS, or the external I/O bus of earlier members of the PDP-8 family. Using MSI and LSI technology, many of these designs provide complete interfaces on a single module.

OMNIBUS and UNIBUS INTERFACE MODULES

The OMNIBUS and UNIBUS are electrically compatible and, despite differences in computer architecture, the general sequence of I/O data transfers is similar from the viewpoint of an external device. Interface modules therefore can be adapted, with a minimum of supporting interface logic, to operate with either computer bus. The M1502, for example, provides up to 16 bits of buffered output from either bus. For PDP-11 UNIBUS compatibility, the M1502 is supplemented by an M105 address selector and an M7820 Interrupt module. For PDP-8/e or 8/m, an M1500 Bus Gates module and the M1510 Device Selector provide the necessary OMNIBUS control functions.

Other modules have been tailored specifically for one bus or the other. For example, the M1702 provides buffering for 12 words of data input on a single quad-height module that plugs directly into the OMNIBUS structure.

The M1702, like most OMNIBUS or UNIBUS interfacing modules, interconnects to external equipment through 40-pin flat cable connectors mounted on the module itself. (See the description of the H854 and H856 connectors in the CABLING section of this handbook.)

Modules available for interfacing to the UNIBUS or OMNIBUS are summarized below. Others are in development. For an up-to-date listing, contact your local DIGITAL Sales Office.

UNIBUS or OMNIBUS	
M1500	Bidirectional Gates
M1501	Data Input
M1502	Data Output
M1621	DVM Data Input
M1623	Instrument Remote Control
M1801	16-Bit Relay Output

UNIBUS Only	
M105	Address Selector
M783	UNIBUS drivers (input)
M784	UNIBUS receivers (output)
M785	UNIBUS Transceiver
M786	Device Interface
M795	Word Count and Bus Address
M796	UNIBUS Master Control
M798	UNIBUS Driver
M7820	Interrupt Control
M7821	Interrupt Control

M1510	Bus Device Selector
M1702	12-Word Buffered Input
M1703	1-Word Input
M1709	OMNIBUS Interface

Signals on the PDP-11 UNIBUS that are used for programmed and interrupt I/O control are defined in Table 1. For complete information on interfacing to the UNIBUS, see Part II of PDP-11 PERIPHERALS AND INTERFACING HANDBOOK, 1972.

Signals on the PDP-8/e, 8/m, OMNIBUS that are used for programmed and interrupt I/O control are defined in Table 2. For complete information on interfacing to the OMNIBUS, see Chapter 9 of the PDP-8/e and PDP-8/m SMALL COMPUTER HANDBOOK, 1972.

OMNIBUS/UNIBUS Electrical Characteristics

The OMNIBUS and UNIBUS bus structures both employ bidirectional data and control lines plus a few unidirectional control signals. Each bus line is a matched and terminated transmission line that must be received and driven with devices designed for that specific application. (See Figure 1.) All M Series modules designed for interconnections to the OMNIBUS or UNIBUS employ special line driver and line receiver circuits appropriate for such bus lines. All drivers (identified by a "D" in the logic symbol) are open-collector gates that control the bus through a wired-OR connection. All receivers (identified by the "R" in the logic symbol) are high-impedance gates that present a minimum of loading to the bus line.

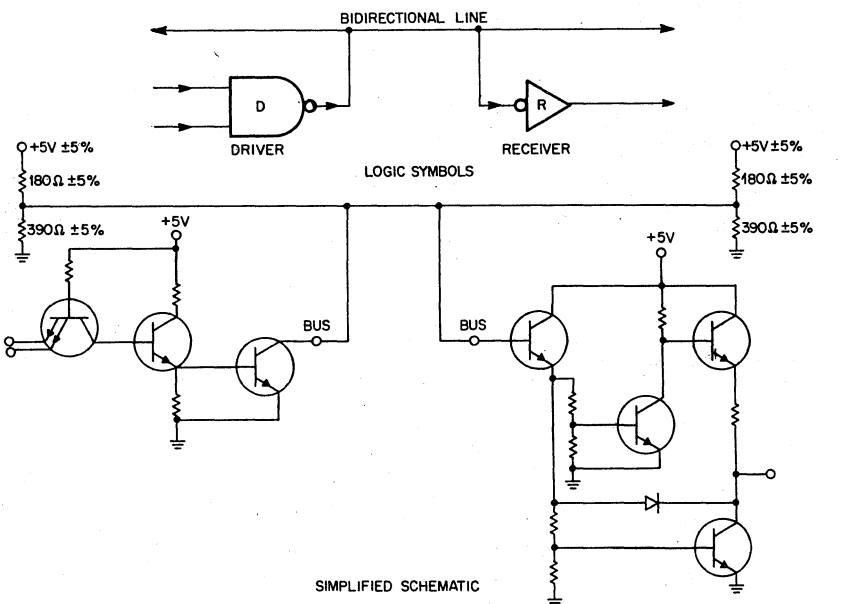


Figure 1. Bidirectional Bus Circuits

Bus drivers and receivers may be connected to OMNIBUS or UNIBUS lines without any concern for loading or drive capability. Often, however, a module may have unused circuits that can be used with TTL devices provided the following loading rules are observed:

Receiver Loading: The bus receiver presents two unit loads to a TTL input.

Driver Sink Capability: The open-collector bus drivers are capable of sinking 50 mA, with a collector voltage of 0.8 volts or less. The collector voltage, when not sinking current, must be less than +6 volts. Leakage current is less than 25 μA.

Table 1. UNIBUS I/O Signal Summary

SIGNAL	DEFINITION
A <17:00>*	Address Lines. The 18 address lines are used by the master device to select the slave (a unique memory or device register address) with which it will communicate. Lines A <17:01> specify a unique 16-bit word. In byte operations, A00 specifies the byte being referenced. Peripheral devices are normally assigned an address from within the bus address allocations from 760000-777777 (program addresses, 160000-177777).
D <15:00>	Data Lines. The 16 data lines are used to transfer information between bus master and slave.
C <1:0>	Control Lines. These two bus signals are coded by the master device to control the slave in one of four possible data transfer operations.

C1	C0	Operation
0	0	DATI—Data In
0	1	DATIP—Data In, Pause
1	0	DATO—Data Out
1	1	DATOB—Data Out, Byte

MSYN	Master and Slave Synchronization. A control signal used by the master to indicate to the slave that address and control information is present.
SSYN	Slave Synchronization. The slave's response to the master (usually a response to MSYN).
PA, PB	Parity Bit Low (PA) and Parity Bit High (PB). These signals are for devices on the UNIBUS that use parity checks. PB is the parity of the high-order byte (that transferred on D <15:08>) and PA is the parity of the low-order byte (D <07:00>).
BR <7:4>	Bus Request Lines. These four bus signals are used by peripheral devices to request control of the bus.

*Angle brackets enclose groups of lines; A < 17:00 > = A17 through A00 inclusive.

BG <7:4>	Bus Grant Lines. These signals are the processor's response to a bus request. They are asserted only at the end of instruction execution, and in accordance with the priority determination.
NPR	Non-Processor Request. This signal is a bus request from a peripheral device to the processor.
NPG	Non-Processor Grant. This signal is the processor's response to an NPR. It occurs at the end of a bus cycle.
SACK	Selection Acknowledge. SACK is asserted by a bus-requesting device that has received a bus grant. Bus control passes to this device when the current bus master completes its operation.
INTR	Interrupt. This signal is asserted by the bus master to start a program interrupt in the processor.
BBSY	Bus Busy. This signal is asserted by the master device to indicate bus is being used.
INIT	Initialization. This signal is asserted by the processor when the START key on the console is depressed, when a RESET instruction is executed, or when the power fail sequence occurs. INIT may also be used to clear and initialize peripheral devices by means of the RESET instruction.
AC LO	AC Line Low. This signal starts the power fail trap sequence, and may also be used in peripheral devices to terminate operations in preparation for power loss.
DC LO	DC Line Low. This signal remains cleared as long as all dc voltages are within specified limits. If an out-of-voltage condition occurs, DC LO is asserted by the power supply.

Table 2. OMNIBUS I/O Signal Summary

SIGNAL	DEFINITION
MDO-11	Provides IOT instruction code. Bits 3-8 contain the device select code; bits 9-11 specify the operation select code.
I/O PAUSE L	Gates the device select and device operation codes into the programmed I/O interface decoders and generates BUS STROBE at TP3 and NOT LAST XFER H.
TP3H	TP3H clears the flag and clocks the output buffer of a programmed I/O interface.
INTERNAL I/O L	INTERNAL I/O is grounded by the device selector decoder.
DATA0-11	The 12 DATA lines called DATA BUS serve as a bidirectional bus for both input and output data between the AC register in the processor and the interface buffer register.
C lines C0, C1, C2	Signals C0, C1, C2 control the data path within the processor and determine if data is to be placed onto the DATA BUS or received from the DATA BUS. They also develop control signals required to load either the AC register or the PC register.
SKIP L	An IOT checks the flag and causes the device logic to ground the SKIP line if the flag is set.
INT RQST L	INT RQST is the method by which the device signals the processor that it has data to be serviced.
BUS STROBE L	BUS STROBE is used to load the AC and PC registers. Unless special I/O operations are being performed, the designer of an interface need not concern himself with BUS STROBE.
NOT LAST XFER L	A ground level on this line indicates to the processor that the next BUS STROBE does not terminate the I/O transaction.
RUN L	When low, RUN indicates that the machine is executing instructions.
TS1 L TS2 L TS3 L TS4 L	These time state lines are high if negated, and low if asserted. Each time state precedes its corresponding time pulse. Time states are always 200 ns or more in duration, and change 50 ns after the leading edge of the time pulse.
TP1 L TP2 L TP3 L TP4 L	These 100-ns positive-going pulses originate in the timing module. The exact spacing of the timing pulses is a function of fast or slow cycle.
INITIALIZE H	INITIALIZE is a positive-going 600-ns pulse used to clear AC, LINK, and flags in peripherals.

EXTERNAL I/O BUS (POSITIVE LOGIC)

The traditional input/output structure for the PDP-8 family computers is the external I/O bus for programmed and interrupt-controlled data transfers. The positive-logic form of this bus, originally developed for the PDP-8/I and PDP-8/L, is compatible with TTL logic. Many modules and peripheral controllers developed for this bus structure are in demand and fully supported by DEC. Positive-bus modules and controllers can also be used with a PDP-8/e or 8/m that is equipped with a KA8-A Positive I/O Bus Interface option.

Earlier negative-logic versions of the PDP-8 family computers can be converted for use with positive-bus modules or options by the addition of a DW08 negative-to-positive bus converter option.

M Series functional modules and level converters for use with the positive-logic external I/O bus include:

M101	Bus Receivers (data output)
M103 M107	Device Selectors
M108	Flags
M623 M624	Bus Drivers (data input)
M730	Bus Output Interface (positive logic output)
M731	Bus Output Interface (negative logic output)
M732	Bus Input Interface (positive logic input)
M733	Bus Input Interface (negative logic input)
M734	3-Word Input Multiplexer
M735	Input/Output Interface
M736	Priority Interrupt Control
M737	Bus Receiver Interface
M738	Counter-Buffer Interface
M907	Diode Clamping for Bus Lines

Signals of the external I/O bus are defined in Table 3. For a complete description of external bus interfacing, see Chapter 10 of the PDP-8/e and PDP-8/m SMALL COMPUTER HANDBOOK, 1972.

Table 3. External I/O Bus Signal Summary.

SIGNAL	DEFINITION
B Initialize	This line is asserted when the processor is initially powered up or when the start key is depressed. Usually performs housekeeping on all peripheral devices—for example, resets all flip-flops on power up.
AC00-11	These lines carry information from the peripheral device to the accumulator. (Input)
BAC 00-11	These lines carry information from the accumulator to the peripheral devices. (Output)
BMB 00-11	These lines carry the device identifier code, a unique address to which only one device will respond.
INTERRUPT REQUEST	This line is activated by the device flag and, when asserted, causes the processor to JMS to location 0 of memory field 0 and disables the interrupt system. (Input)
BIOP 1	This line, when active, is ordinarily used to test device flags. (Output)
SKIP	This line, when active during an IOP, will set the Skip flip-flop in the processor.
BIOP 2	This line, when active, is ordinarily used to clear the device flag and/or cause the device to operate. (Output)
CLEAR AC	This control line, when asserted, changes the mode of I/O input transfer to a jam transfer. (Input)
BIOP 4	When active, is ordinarily used to effect data transfers to or from the peripheral devices. (Output)
B Run	When active, signals peripheral devices that the processor is executing instructions. (Output)
BTS1 and BTS3	These lines are used to sync peripheral devices to the processor. (Output)

NEGATIVE BUS

Some models of the PDP-8/I and earlier models of the PDP-8 family employed an I/O bus structure that is logically identical to the positive-logic external I/O bus except for the logic levels which are ground and −3 volts. The following M Series functional modules simplify adapting negative-bus computer I/O signals to controllers using positive TTL logic:

M100	Data Output from Negative Bus (pin compatible with M101 which does the same function for the positive bus)
M102	Device Selector (pin compatible with the M103 positive-bus device selector)
M632 M633	Drives negative bus input lines

In addition, there is a wide assortment of level converters for two-way compatibility between the negative bus and M Series modules:

M051 M650 M652	Positive in, negative out
M500 M502 M506 M507	Negative in, positive out

For detailed electrical characteristics and timing on the negative I/O bus, refer to a 1970 (or earlier) edition of the SMALL COMPUTER Handbook.

PDP-15 Bus

The following modules were developed specifically for interfacing with the PDP-15 I/O bus, but may be used in many other positive logic applications.

M510	Positive bus receiver
M622	Positive bus driver
M909 M910	Bus line terminators

M051
POSITIVE TO NEGATIVE LOGIC LEVEL CONVERTER

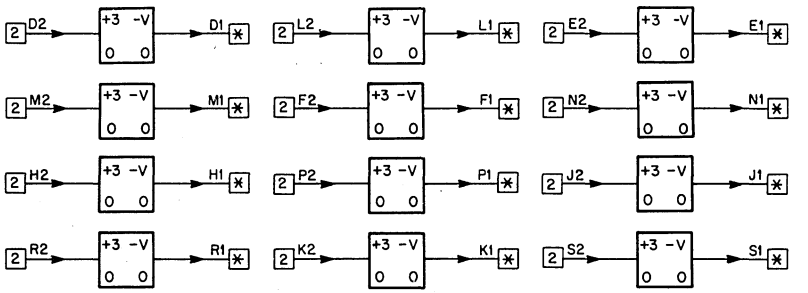
LEVEL CONVERTERS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$31



*= 20 MA, -6V MAX. * = 50 MA, -30V MAX.

Volts	Power mA (max.)	Pin
+5	47	A2
GND		C2
—15	16	B2

The M051 contains twelve level converters that can be used to shift M and K Series logic levels to negative logic levels of ground and —3 volts.

APPLICATIONS

- Interfacing to negative bus PDP computers
- Interfacing to R/B/W Series Logic Systems

Restrictions: Do not use for indicator drive or current sinking.

FUNCTIONS

A grounded input on the driver causes the output to be grounded.

SPECIFICATIONS

The output circuit consists of an open collector PNP transistor that can drive 20 mA to ground. —6 volts maximum may be applied to the output.

M100
BUS DATA INTERFACE

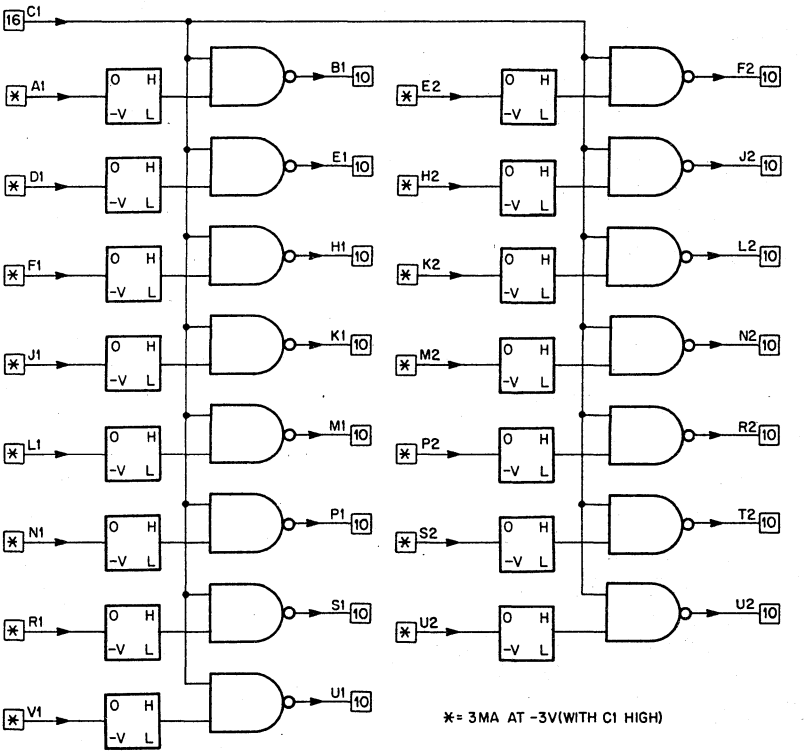
8-FAMILY NEG. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$50



Volts	Power mA (max.)	Pin
+5	60	A2
GND		C2
−15	10	B2

The M100 Bus Data Interface contains fifteen circuits for convenient reception of data from the PDP-8, PDP-8/I negative voltage bus. It is pin compatible with the M101 Positive Bus Data Interface.

APPLICATIONS

- Output data transfer expansion for PDP-8, PDP-8/I

FUNCTIONS

Each input line is connected to M Series levels and gated to the output by the ENABLE signal. Each circuit has the following function:

INPUT	ENABLE	OUTPUT
0V	L	H
0V	H	L
—V	L	H
—V	H	H

(L and H refer to standard M Series Levels of 0 and +3V. —V refers to negative input. (See Threshold Switching Level.)

PRECAUTIONS

The enable line of the M100 cannot be used as a strobe line. The output signals are indeterminate for a period of 200 ns after the enabling line has become true. The enable is intended to be controlled by the option select output of the M102.

SPECIFICATIONS

Input Loading: The loading presented to the negative voltage bus differs from the loading using the standard bus modules (i.e., R107, R111) in that the data lines are loaded only if the device is selected.
Threshold Switching Level: —1.5 volts typ.
Propagation Delay: 40 ns typ.

M101
BUS DATA INTERFACE

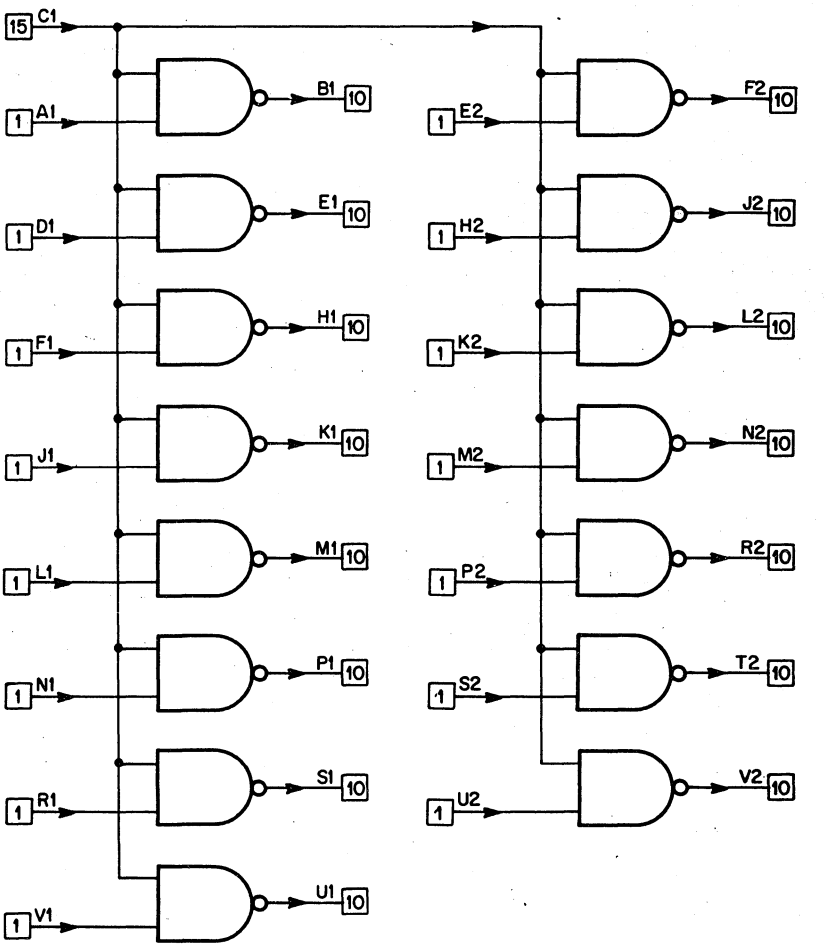
8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$24



Volts	Power mA (max.)	Pins
+5	82	A2
GND		C2, T1

The M101 contains fifteen, two-input NAND gates arranged for convenient data strobing from the PDP8/I or PDP8/L positive bus.

APPLICATIONS

- PDP8/I, PDP-8/L Positive Bus Output Expansion
- Can also be used as inverters or a data multiplexer

FUNCTIONS

Inputs are NAND gated to the output by the common ENABLE input (C1).

SPECIFICATIONS

Inputs and outputs have standard M Series levels and propagation time. All data inputs are protected from a negative voltage of more than —0.8 volts.

M102
DEVICE SELECTOR

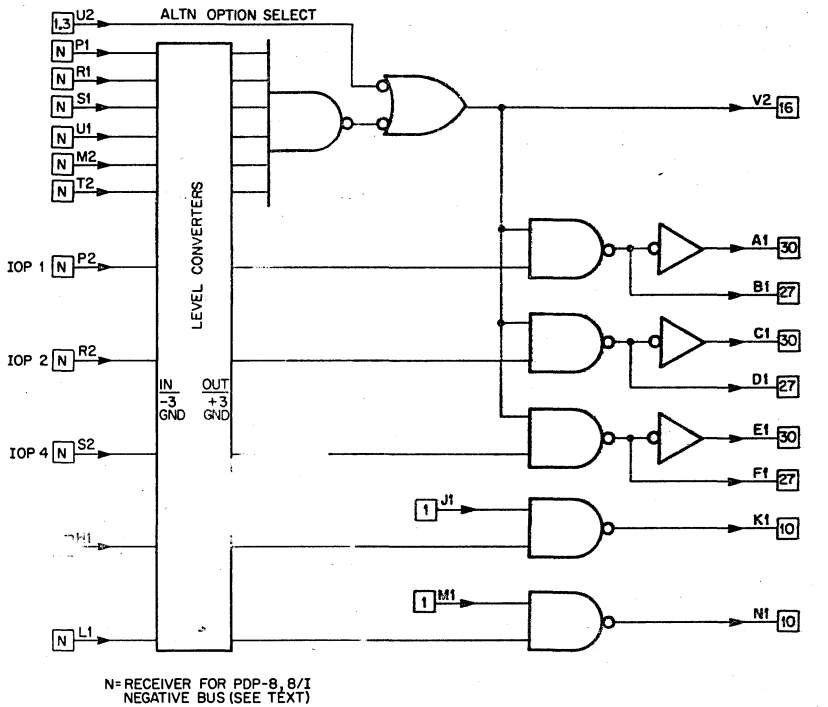
8-FAMILY NEG. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$60



Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, T1
−15	40	B2

The M102 is used to decode the six device address bits transmitted in complementary pairs on the negative BMB bus of the PDP-8, PDP-8/I. The outputs of the M102 are compatible with M Series TTL logic. The M102 is pin compatible with the M103 Positive bus device selector with the exception of the address inputs.

APPLICATIONS

- Design of custom M Series interfaces for negative bus PDP-8, PDP-8/I.

FUNCTIONS

OPTION SELECT: The OPTION SELECT output is HIGH when all negative-bus code inputs (P1-T2) are at ground. (Note: PDP-8, PDP-8/I BMB outputs are asserted at ground.) The OPTION SELECT ENABLE input is an M Series level that can override the code input.

IOP ENABLE: When the OPTION SELECT output is enabled, IOP pulses from the computer are gated to output pins A1-F1. Both LOW to HIGH and HIGH to LOW pulse output polarities are provided.

Gated Inverters: Two single-input inverters are provided which function as follows:

Neg. Input (H1, L1)	Gating Input	Output
0V	L	H
0V	H	H
—V	L	H
—V	H	L

SPECIFICATIONS

Negative Input Levels: Negative inputs (—V) are nominally —3V and ground. Threshold Switching Level is —1.5V typ.

Negative Input Loading: BMB input loading is 1 mA, shared among the inputs that are at ground.

IOP Input Loading: P2, R2, S2, H1 and L1

0.2 mA, when V in = 0 volts
0.0 mA, when V in = —3 volts

Propagation Delay: 40 ns typ.

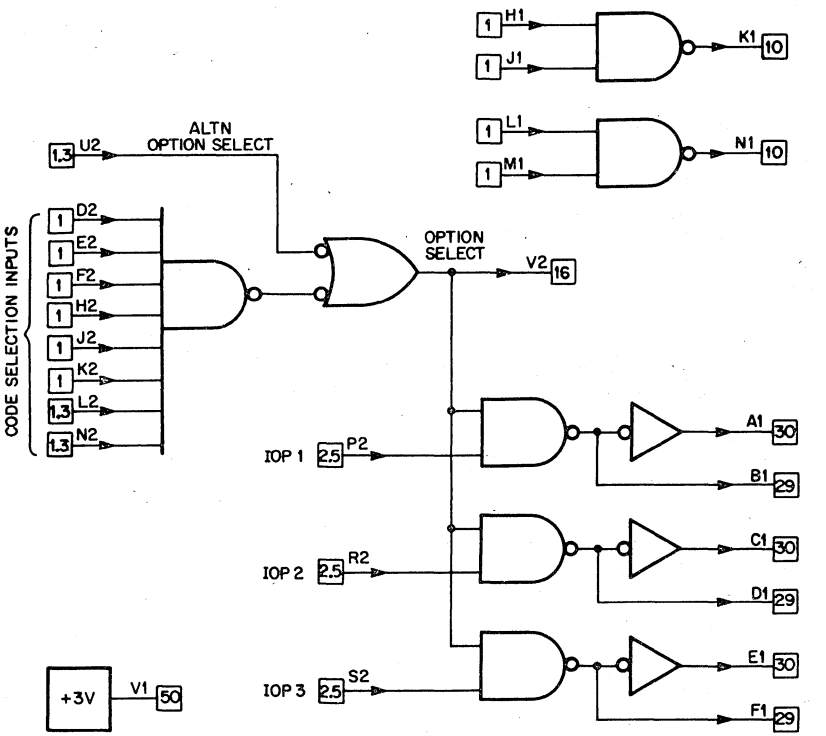
M103
DEVICE SELECTOR

8-FAMILY
POS. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:
$45



Volts	Power mA (max.)	Pins
+5	110	A2
GND		C2, T1

The M103 is used to decode the six device bits transmitted in complement pairs on the positive bus of the PDP8/I and PDP8/L. Selection codes are obtained by selective wiring of the bus signals to the code select inputs D2, E2, F2, H2, J2, and K2. This module also includes pulse buffering gates for the IOP signals found on the positive bus of the above computers. Two two-input NAND gates are also provided for any additional buffering that is required.

APPLICATIONS

- Special-purpose M Series Interfaces for positive bus PDP-8/I, PDP-8/L

FUNCTIONS

OPTION SELECT: The OPTION SELECT output is HIGH when all code inputs (D2-N2) are HIGH. The OPTION SELECT ENABLE input is able to override the code input.

IOP ENABLE: When the OPTION SELECT output is enabled, IOP pulses from the computer are gated to output pins A1-F1. Buffered and unbuffered outputs are provided (of opposite polarity).

Unused Inputs: Unused code inputs should be connected to a source of logic HIGH. Inputs U2, L2, and N2 need not be tied to logic HIGH.

SPECIFICATIONS

Input Protection: All inputs which receive positive bus signals are protected from negative voltage undershoot of more than 0.8V.

M105
ADDRESS SELECTOR

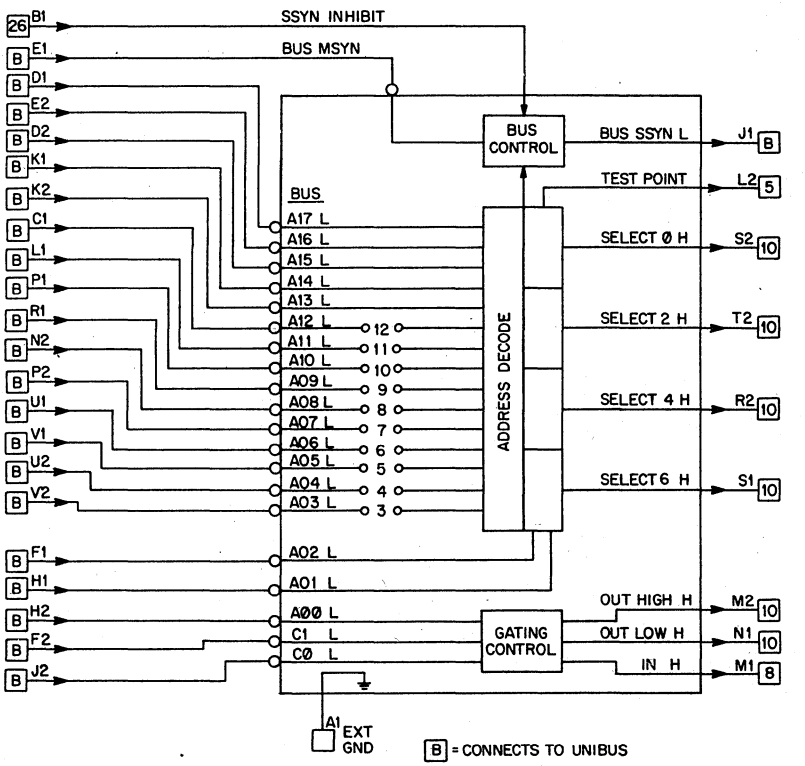
PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single

Price:

$65



Volts	Power mA (max.)	Pins
+5	338	A2
GND		C2, T1

The M105 is used in PDP-11 device interfaces to control the flow of data between the device registers and the UNIBUS. It provides gating signals for up to four device registers that indicate a register is being referenced and three control signals that indicate the path for data flow.

The selector decodes the 18-bit address A <17:00> as follows: A <17:13> defines the memory "page" assigned to peripheral devices (external bank) and must all be asserted. A <12:03> is determined by jumpers on the card.

When the jumper is "in" the selector will look for a zero on that address line. A02 and A01 provide a coding array for the four SELECTED addresses. A00 is for byte control.

Signals for gating control are determined by decoding A00, C1, and C0. The signals obtained are: IN, OUT LOW, and OUT HIGH.

$$\text{IN} = \text{DATI} + \text{DATIP}$$
$$\text{OUT LOW} = \text{DATO} + (\text{DATOB} \bullet \overline{\text{A00}})$$
$$\text{OUT HIGH} = \text{DATO} + (\text{DATOB} \bullet \text{A00})$$

IN is used to gate data from a device register onto the bus. OUT LOW is used to gate D <07:00> into the low byte of a device register. OUT HIGH is used to gate D <15:08> into the high byte of a device register.

In relation to bus control, the M105 is actually the "slave" in the relationship when data transfer occurs on the Unibus.

SSYN is asserted whenever it sees its address being referenced and MSYN is asserted. SSYN is negated when MSYN is negated. There is an approximate 100 nsec. delay between receiving MSYN and the assertion of SSYN to allow for decoding.

EXT GND is used for testing purposes and should be tied to ground in normal operation.

SSYN INHIBIT can be left open when not used.

M107
DEVICE SELECTOR

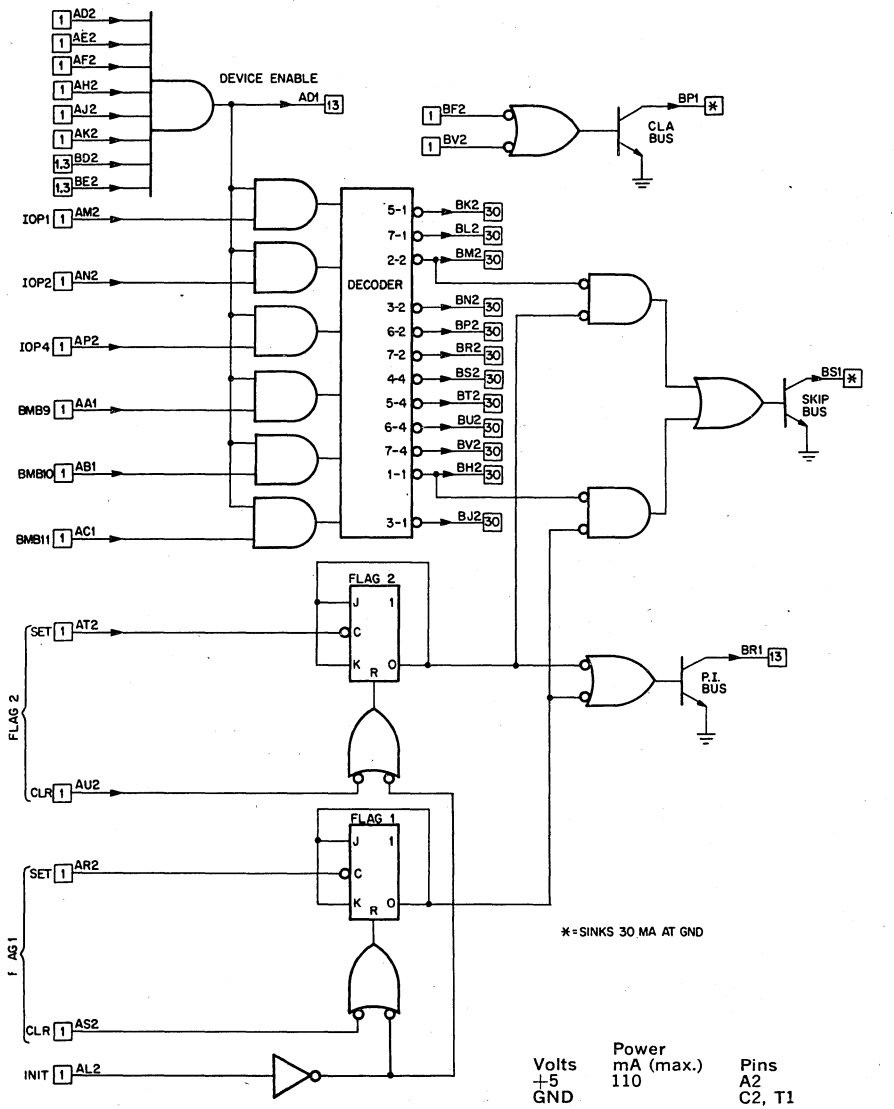
8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Double
Width: Single

Price:

$105



Volts	Power mA (max.)	Pins
+5	110	A2
GND		C2, T1

The M107 is a device selector which, by the use of extended decoding of the BMB lines 9 through 11, will provide seven discrete IOT pulses. Five additional IOT pulse outputs are provided to allow the user to reduce software requirements by the combining of IOT codes. The IOT instruction and the IOP times at which the various IOT pulses occur at the module pins are outlined in the following chart:

Module Pin	IOT	AT IOP TIME		
		1	2	4
BH2	1 – 1	X		
BM2	2 – 2		X	
BJ2	3 – 1	X		
BN2	3 – 2		X	
BS2	4 – 4			X
BK2	5 – 1	X		
BT2	5 – 4			X
BP2	6 – 2		X	
BU2	6 – 4			X
BL2	7 – 1	X		
BR2	7 – 2		X	
BV2	7 – 4			X

Example: If an IOP-7 is issued, IOT pulses will exist only at output pins BL2 (7-1), BR2 (7-2) and BV2 (7-4). IOT pulses will not exist at any other output pin.

The M107 also contains two flag flip-flops which may be directly cleared or set. The outputs of the flag flip-flops are connected to the skip and program interrupt lines. Interrogation of the flags is accomplished by IOT 1 – 1 for flag 1 and IOT 2 – 2 for flag 2.

The M107 also provides two inputs to accomplish the "clear the accumulator" function.

Outputs: Option Select Pin AD1 can drive 13 TTL loads. Bus driver outputs pins BP1, BS1, and BR1 are open collector NPN transistors and can sink 30 ma. at ground. The maximum voltage applied to these outputs must not exceed +20 Volts and each output is diode protected against negative undershoot in excess of −0.9 Volts.

M108
FLAG MODULE

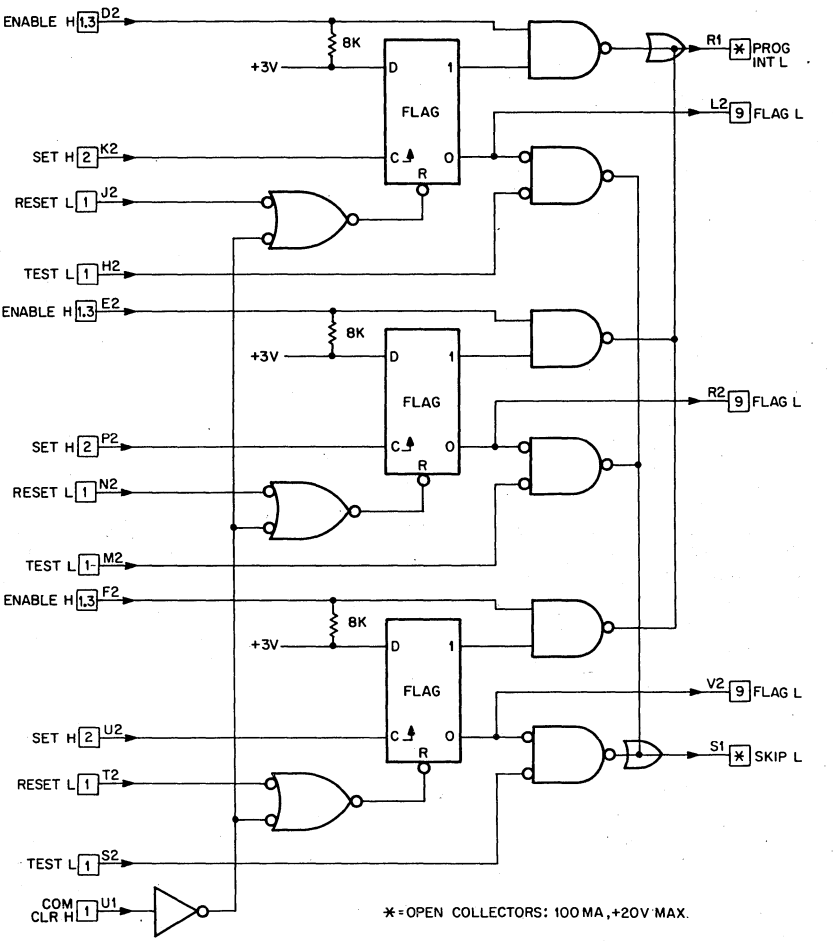
8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$45



Volts	Power mA (max.)	Pins
+5	137	A2
GND		C2, T1

The M108 contains three general-purpose clocked flip-flops for use in flag applications in I/O interfaces, etc. Gating is provided so that the flags can be individually set or gated to the program interrupt inputs of a positive-bus PDP-8 computer.

APPLICATIONS

- Device Ready logic in custom device interfaces for positive-bus PDP-8 computers

FUNCTIONS

CLEAR Inputs: Each flag flip-flop may be independently cleared or all flip-flops may be cleared simultaneously.

Flag Outputs: The output of each flag flip-flop is gateable and is open collector ORed to the Program Interrupt bus.

The output of each flag flip-flop is passed through a gate and open collector to the skip bus. This facility allows the user to test for a flag.

The 0 side of each flip-flop has been extended to module pins for peripheral control.

SET Inputs: Each flip-flop may be independently set by the application of the leading (positive going voltage) edge of a pulse or level to the clock inputs.

Disabling PI Feature: If use of the Program Interrupt feature is not desired, the ENABLE inputs (D2, E2, F2) must be connected to ground. If Program Interrupt is desired, no connections to the ENABLE inputs are required.

SPECIFICATIONS

Pin R1, (PI Function) and S1 (Skip Function) are open collector NPN Transistors and will sink 100mA to ground. The voltage applied to these outputs must not exceed +20 volts.

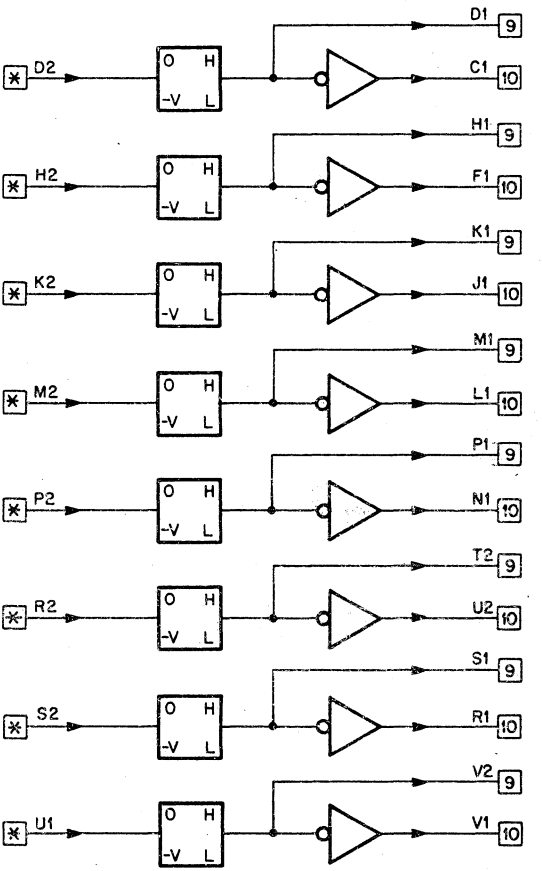
M500
NEGATIVE INPUT POSITIVE OUTPUT RECEIVER

PDP-15 BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price: $55



*=1mA AT GROUND

Volts	Power mA (max.)	Pins
+5	160	A2
GND		C2, T1
−15	64	B2

The M500 module is used to convert negative input signals to positive output signals. Each card contains eight converters and is pin compatible with the PDP-15 positive receiver card (M510).

FUNCTIONS

A ground input at D2 will yield a +3 at D1 and ground at C1. Do not connect to pin E2 (used for manuf. test only).

SPECIFICATIONS

Propagation time (each circuit):

FROM	TO	ns (max.)
Input	Output	40

M502
HIGH SPEED
NEGATIVE INPUT CONVERTER

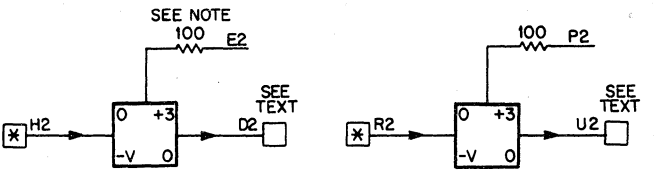
LEVEL CONVERTERS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$26

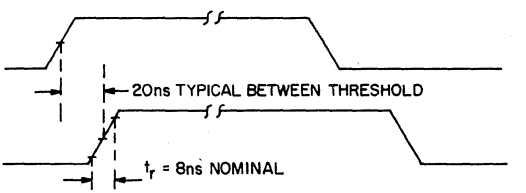


*=EQUIV. OF 3 MA CLAMPED LOAD

Volts	Power mA (max.)	Pins
+5	49*	A2
GND		C2, T1
−15	92	B2

NOTE
CONNECT TO OUTPUT WHEN NOT DRIVING 92Ω COAX.

* Add 44 mA for each 100 ohm resistor connected to outputs.



The M502 contains two non-inverting high-speed signal converters which interface standard negative (−3 volts and ground) logic levels or pulses with M and K Series positive logic modules. These converters provide sufficient current drive at a low output impedance for system interconnections by means of terminated 92-ohm coaxial cable.

FUNCTIONS

Outputs: Each output can drive a terminated 92-ohm coaxial cable and supply an additional 30 mA at +3 volts or sink an additional 30 mA at ground.

SPECIFICATIONS

The converters operate at frequencies up to 10 MHz with typical output rise and fall times of 8 ns. Propagation times for output rise and fall are typically 20 ns.

Input loading is equivalent to a 3 mA clamped load.

Output rise and fall times depend on the length of coaxial cable driven. When coaxial cable is not driven, switching speeds are increased by connecting the 100-ohm resistor to the output.

M506
MEDIUM SPEED
NEGATIVE INPUT CONVERTER

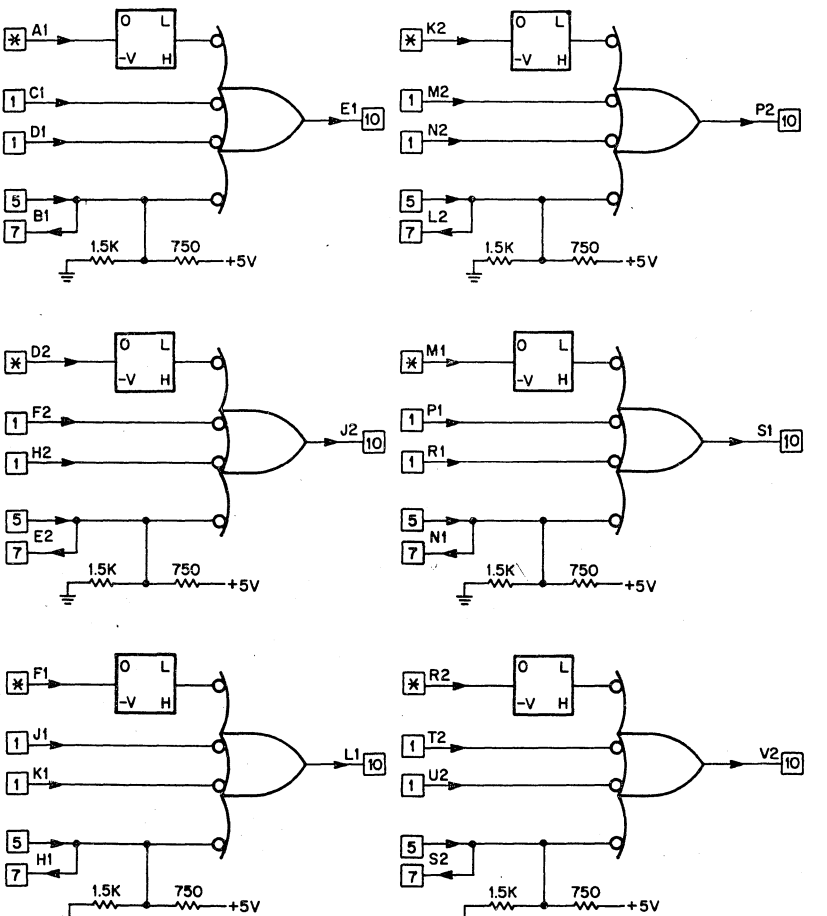
LEVEL CONVERTERS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$52



*=10mA AT GND, DIODE CLAMPED

Volts	Power mA (max.)	Pins
+5	81	A2
GND		C2, T1
−15	115	B2

The M506 contains six noninverting signal converters which can be used to interface the negative logic levels or pulses of duration greater than 100 ns to M and K Series positive logic levels of +3 volts and ground.

In addition to the negative level inputs, each converter circuit has three additional NOR inputs for positive logic levels of +3 volts and ground. A source of logic HIGH for unused inputs is provided at each gate.

FUNCTIONS

(Pins A1, etc.)	IN	OUT
	−3V	0V
	0V	+3V

SPECIFICATIONS

These converters operate at frequencies up to 2 MHz with typical rise and fall propagation times of 70 ns and 40 ns respectively.

All negative level inputs (A1, D2, . . . R2) present a 10 mA load at ground.

> **Caution:** These inputs are diode-clamped to −3 volts; input voltages greater than −3 volts may draw excessive current.

M507
MEDIUM SPEED
NEGATIVE BUS CONVERTER

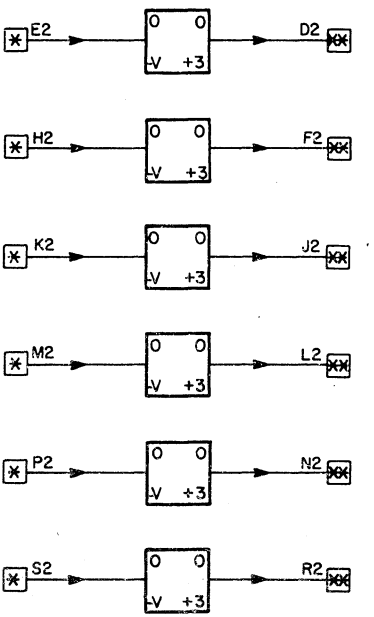
LEVEL CONVERTERS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$45



* = 10 mA CLAMPED LOAD
** = SINKS 100 mA TO GND; +20V MAX.

Volts	Power mA (max.)	Pins
+5	42	A2
GND		C2, T1
−15	115	B2

The M507 contains six inverting level shifters which will accept −3V and GND as inputs. The input to each level shifter consists of a 10 mA clamped load and is diode protected against positive voltage excursions.

The output consists of an open collector NPN transistor. The output of each level shifter will sink 100 mA to GND.

The output transistor is protected against negative voltage excursions by a diode connected between the collector and GND. The output rise is delayed by 100 ns for pulse spreading.

APPLICATIONS

The M507 is used to convert negative voltage logic levels or pulses of duration greater than 100 ns to M Series levels (or pulses).

FUNCTIONS

INPUT	OUTPUT
GND	GND
−3V	+3V

SPECIFICATIONS

Input loading is equivalent to a 3 mA clamped load.

Each output can sink 100 mA to GND. Maximum voltage applied to any output is +20 volts.

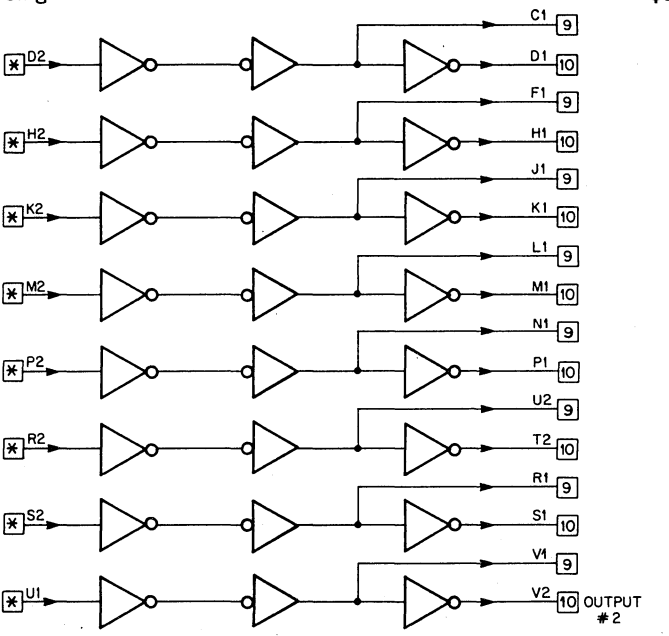
M510
I/O BUS RECEIVER

PDP-15
BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:
$51



Volts	Power mA (max.)	Pins
+5	170	A2
GND		C2, T1, F2 J2, L2, N2

The M510 is a positive input/output receiver card for use with the PDP-15. It contains 8 high-impedance input circuits of at least 27K ohms and input switching thresholds of about +1.5 V. Each receiver has two outputs, one of the same polarity as the input, the other, the complement of the input. The receiver card can be used anywhere on the PDP-15 I/O Bus.

PRECAUTIONS

Do not connect to pin E2 (used for manuf. test only). Power (B+) must be applied at all times since the input impedance drops to 1K ohm when power is off.

SPECIFICATIONS

Inputs: The input impedance is 27K ohms (min.). Each input load current is 80 mA (max.) and the threshold switching level is 1.4 to 1.6 volts.

Outputs: Output no. 2 delay = 50 ns (from input).

M622
EIGHT-BIT POSITIVE INPUT/OUTPUT BUS DRIVER

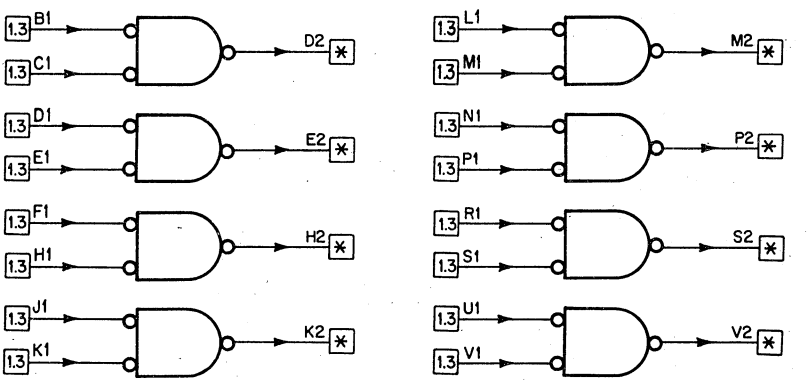
PDP-15 BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$45

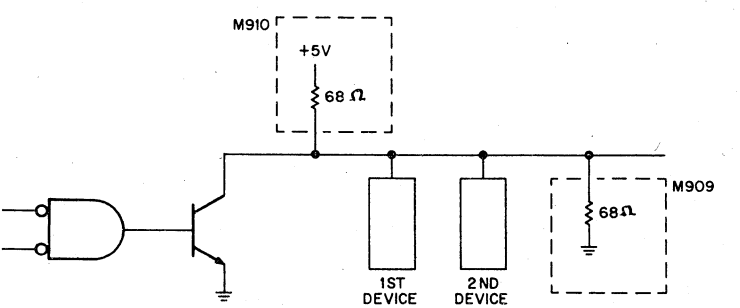


* = DRIVES PDP-15 POSITIVE BUS

Volts	Power mA (max.)	Pins
+5	210*	A2
GND		C2, T1, F2, J2, L2, N2, R2, U2

* excluding output current

The M622 contains 8 two-input AND gate bus drivers for convenient driving of the positive input bus of the PDP-15. The output consists of an open collector NPN transistor.



Pull-up resistors of 68 ohms to +5.0 V (supplied on M910) must be tied to the output and the last device should terminate all lines to ground with a 68-ohm resistor (supplied on M909).

PRECAUTIONS

Outputs: The maximum voltage applied to the output transistor must not exceed +20 volts and the collector current must not exceed 100 mA.

SPECIFICATIONS

Propagation Time: Typically 25 ns.

M623
BUS DRIVER

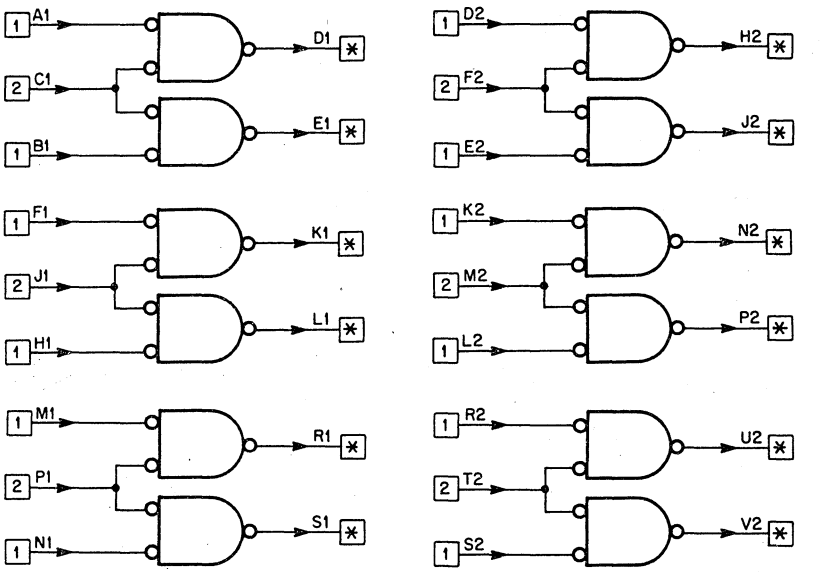
8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$40



*= SINKS 100 MA TO GROUND, +20V MAX.

Volts	Power mA (max.)	Pins
+5	71*	A2
GND		C2, T1
		U1, V1

* does not include output current

The M623 contains 12 two-input AND gate bus drivers for convenient driving of the positive input bus of either the PDP-8/I or PDP-8/L. The output consists of an open collector NPN transistor.

APPLICATIONS

- Driving PDP-8/I or PDP-8/L positive input bus

FUNCTIONS

A driver output will be at ground when both inputs are at ground.

SPECIFICATIONS

Output Drive: Each driver can sink 100 mA at ground and can withstand a maximum output voltage of +20 volts.

Output Rise and Fall Times: Typically 30 ns when a 100 mA resistive load is connected to a driver output.

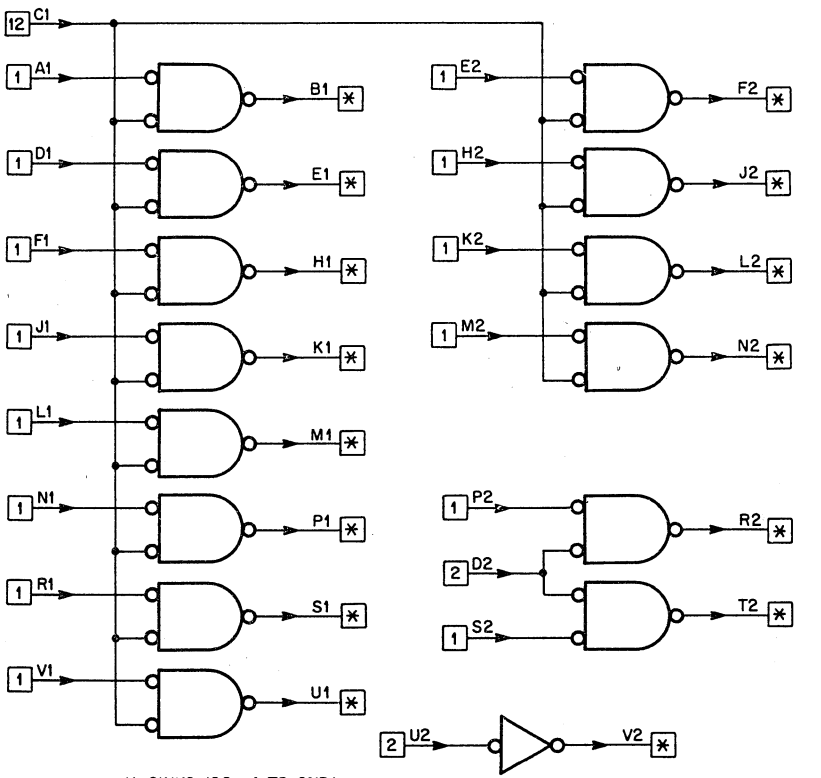
M624
BUS DRIVER

8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price: $45



*=SINKS 100 mA TO GND; +20V MAX.

Volts	Power mA (max.)	Pins
+5	89*	A2
GND		C2, T1

* driver outputs not connected

The M624 contains 15 bus drivers intended for convenient driving of the positive input bus of either the PDP-8/I or PDP-8/L. Twelve of the drivers have a common gate line for selecting data. There are three additional drivers, two sharing a common gate line and the third without a gate line. These three additional drivers were intended to accommodate the functions of PROGRAM INTERRUPT, IO SKIP and CLEAR AC.

Each output consists of an open collector NPN transistor.

APPLICATIONS

- PDP-8/I or PDP-8/L positive input bus driving

SPECIFICATIONS

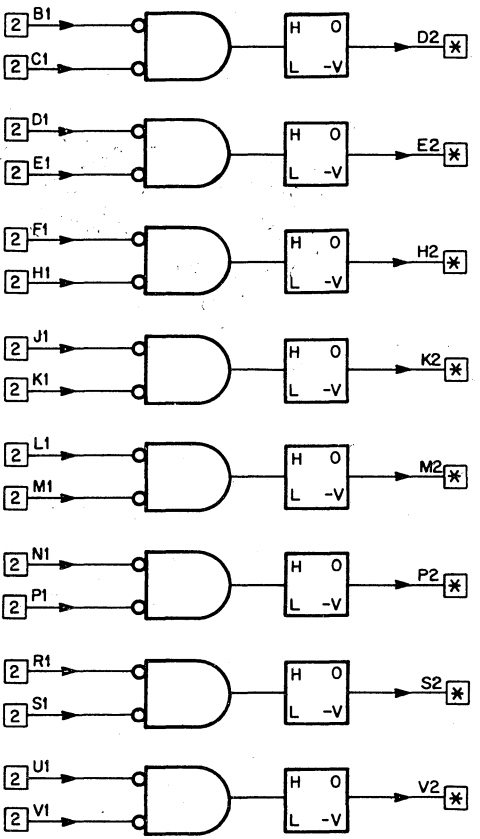
All outputs can sink 100 mA to ground. Voltage applied to the output should be equal to or less than +20 volts. Output rise and fall times are typically 30 ns when a 100 mA resistive load to +5 volts is connected to a driver output.

M632
POSITIVE INPUT NEGATIVE OUTPUT BUS DRIVER

8-FAMILY NEG. I/O BUS

Length: Standard
Height: Single
Width: Single

Price: $55



* = SINKS 100 mA AT GND

Volts	Power mA (max.)	Pins
+5	175	A2
GND		C2, T1, F2, J2, L2, N2, R2, U2,
−15	40*	B2

* excluding output current

The M632 contains eight two-input AND gate bus drivers for convenient driving of the negative bus of the PDP-8/I or PDP-8/L.

FUNCTIONS

Each stage operates according to the following truth table:

INPUTS	OUTPUT
LL	0V
LH	—V
HL	—V
HH	—V

SPECIFICATIONS

Output Drive: The output is internally clamped to keep it between —3 volts and ground. The output current must not exceed 100 mA.

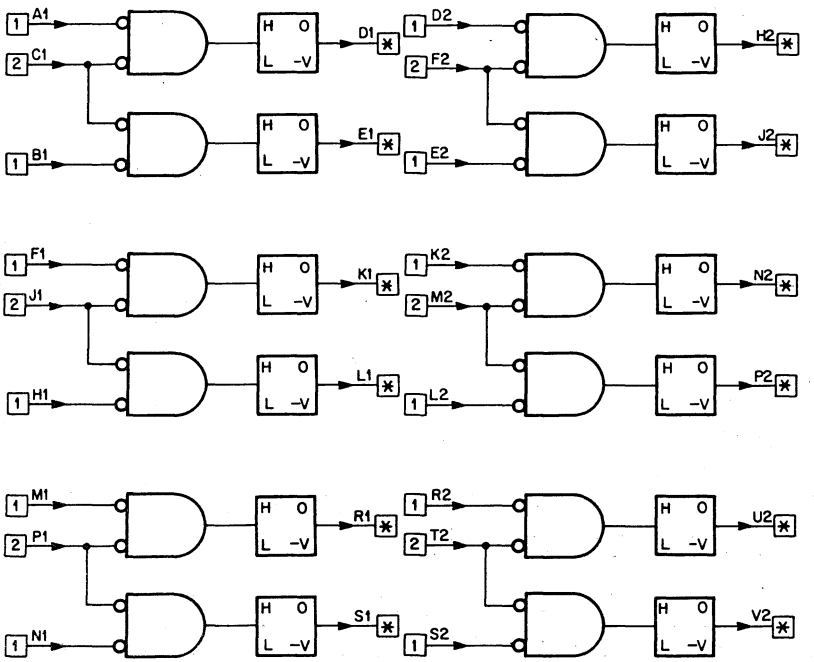
Propagation Delay: 50 ns max.

M633
NEGATIVE BUS DRIVER

8-FAMILY
NEG. I/O BUS

Length: Standard
Height: Single
Width: Single

Price:
$50



* = DRIVES PDP-8, PDP-8/I NEGATIVE BUS

Volts	Power mA (max.)	Pins
+5	100	A2
GND		C2, T1
−15	40	B2

The M633 contains 12 bus drivers intended for convenient driving of the negative bus of the PDP-8, PDP-8/I. Each driver consists of an open collector PNP transistor. It is pin-compatible with the M623 positive voltage bus driver.

FUNCTIONS
Each stage operates according to the following truth table:

INPUTS	OUTPUT
LL	0
LH	—V
HL	—V
HH	—V

SPECIFICATIONS:
Output Drive: Each output is an open collector PNP transistor capable of supplying 20 mA from ground. Voltage applied to the output should not exceed —6 volts.

Propagation Delay: Typically 40 ns.

M650
NEGATIVE OUTPUT CONVERTER

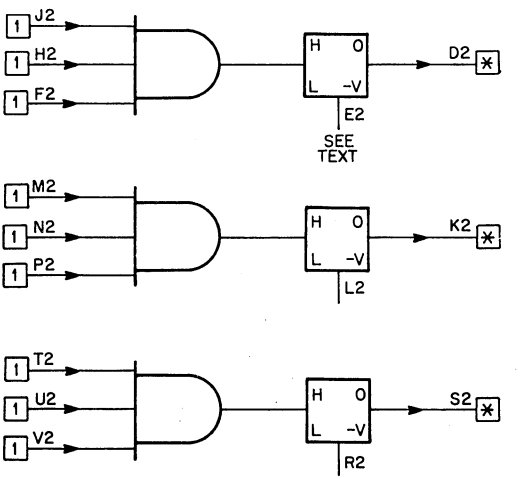
LEVEL CONVERTERS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$25



*=20 MA AT GND OR -3V

Volts	Power mA (max.)	Pins
+5	37	A2
GND		C2, T1
−15	29	B2

The M650 contains three noninverting signal converters which can be used to interface the positive logic levels or pulses (of duration greater than 100 ns) of K and M Series to digital negative logic levels of −3 volts and ground. These converters provide current drive at a low output impedance so that unterminated cables or wires can be driven with a minimum of ringing and reflections.

FUNCTIONS

A positive AND condition at the input gate produces a ground output. If any input is at ground, the converter output is at −3 volts.

SPECIFICATIONS

The converters operate at frequencies up to 2 MHz with maximum rise and fall total transition of respectively 75 ns and 115 ns. By grounding pin E2 (L2 or R2) the rise and fall total transition times can be increased to avoid ringing on exceptionally long lines. The converter then operates at frequencies up to 500 kHz with typical rise and fall total transition times of 500 ns.

Each output is capable of driving 20 mA at ground and at −3 volts.

M652
NEGATIVE OUTPUT CONVERTER

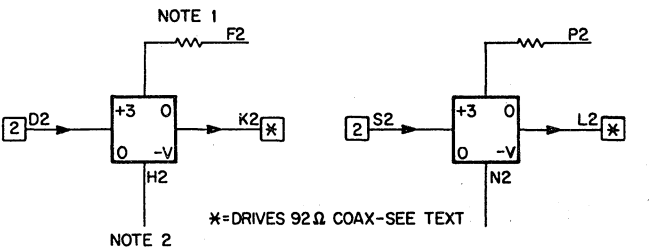
LEVEL CONVERTERS

M SERIES

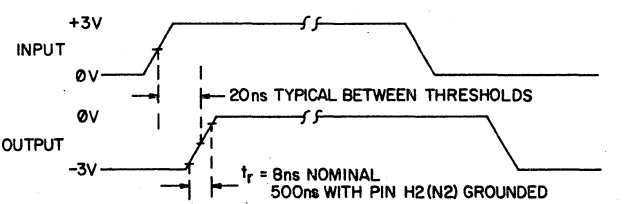
Length: Standard
Height: Single
Width: Single

Price:

$26



NOTES:
1. CONNECT TO OUTPUT WHEN NOT DRIVING 92 Ω COAX.
2. CONNECT TO GROUND PIN FOR 500 ns RISE TIME



Volts	Power mA (max.)	Pins
+5	122	A2
GND		C2, M2
−15	202	B2

The M652 contains two noninverting high-speed signal converters which can be used to interface the positive logic levels or pulses of the K and M Series to digital negative logic levels of −3 volts and ground. These converters provide current drive at a low output impedance so that system interconnections can be made using terminated 92-ohm coaxial cable.

FUNCTIONS
Each section:

INPUT	OUTPUT
L	−3V
H	0V

SPECIFICATIONS

Timing: The converters operate at frequencies up to 10 MHz with typical output rise and fall times of 8 ns. Propagation times for output rise and fall are typically 20 ns. The slope of the output transition can be decreased by grounding an internal RC network, to avoid ringing on exceptionally long lines. The converter then operates at frequencies up to 1 MHz.

Inputs: Positive logic levels of 0 and +3 volts (nominal). Input signals more positive than +6 volts will damage the circuit.

Outputs: Each output can drive terminated 92-ohm coaxial cable and supply an additional 20 mA at ground or sink an additional 20 mA at −3 volts. Output rise and fall times are dependent on the length of coaxial cable driven. When coaxial cable is not driven, switching speeds will be increased by connecting the 100-ohm resistor to the output.

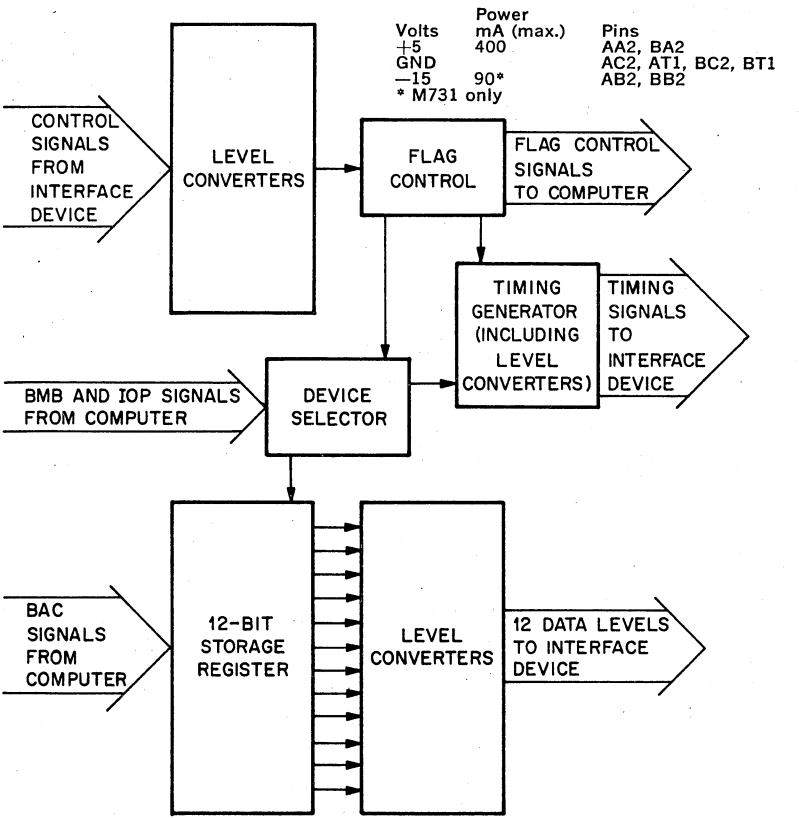
M730 & M731 BUS INTERFACES

8-FAMILY POS. I/O BUS

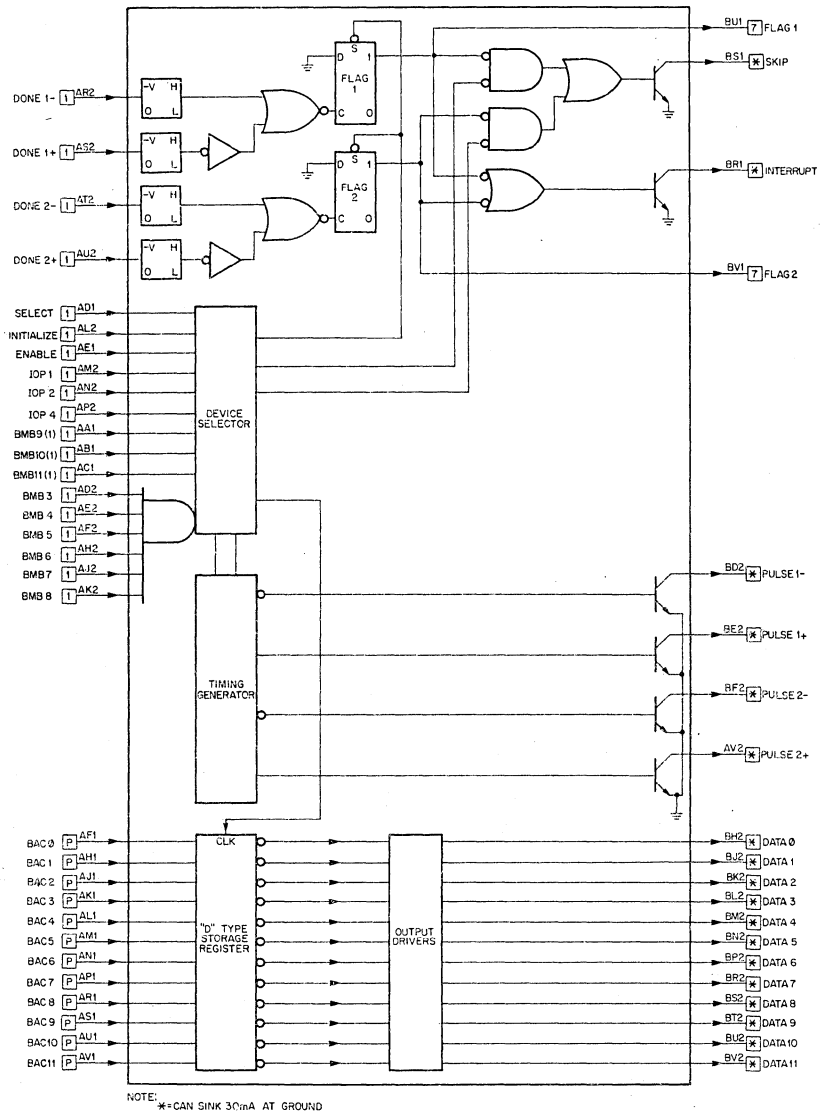
M SERIES

Length: Standard
Height: Double
Width: Single

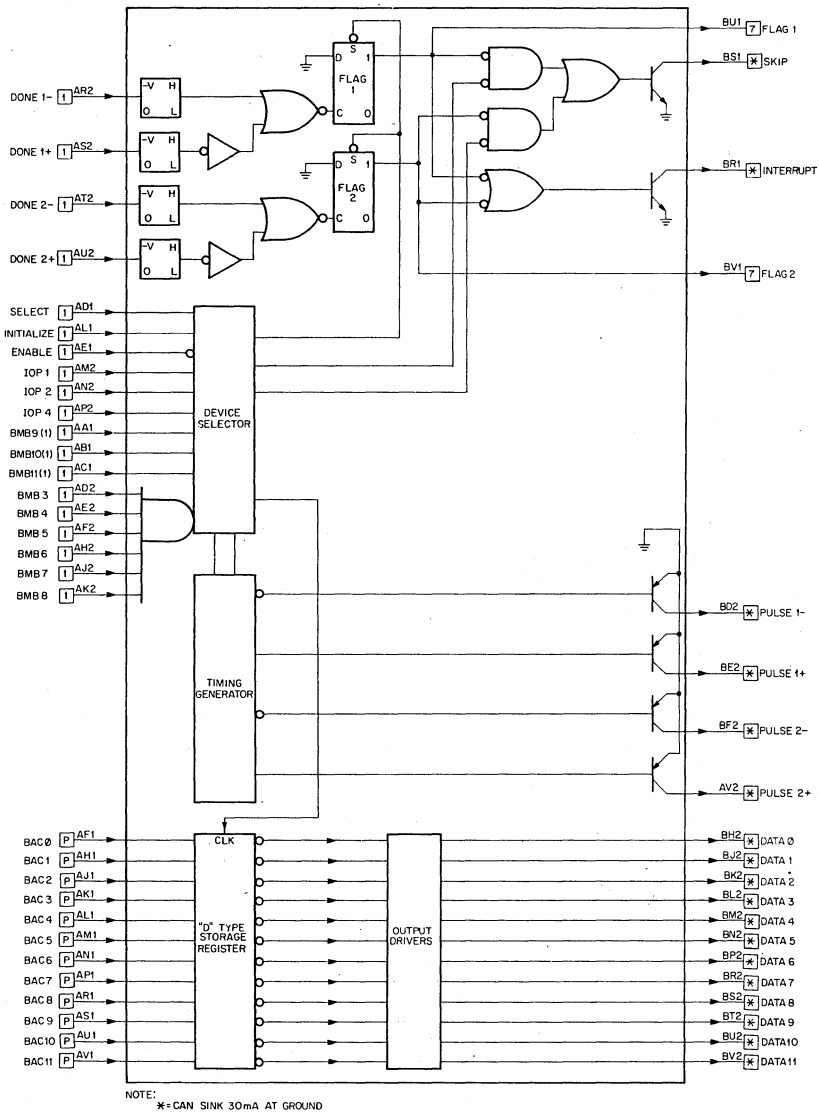
Price:
M730 — $160
M731 — $160



The M730 and M731 interface modules provide extremely flexible interface control logic to connect devices, systems, and instruments to the output half of the programmed I/O transfer bus of either a PDP8/I or a PDP8/L positive bus computer. Peripheral equipment which operates either asynchronously or synchronously to a computer and expects to receive data from that computer, can to a large degree be interfaced by either the M730 or M731. Basic restrictions on the device or system to be interfaced are simply that it receive data in parallel, provide one or more control lines, and operate at a data transfer rate of less than 20 KHz. Complete interfaces to such peripheral gear as card punches and other repetitive devices is possible using the M730 and M731; however part of the controlling functions, such as counting etc. must be performed by computer software.



BUS INTERFACE — M730 (POSITIVE OUTPUT)



BUS INTERFACE — M731 (NEGATIVE OUTPUT)

Functionally, these modules contain five distinct sections which are as follows:

1. Device Selector—This logic network converts the buffered memory buffer (BMB) signals and IOP timing pulses from the computer into internal module control pulses.

2. Timing Generator—Through the use of device selector signals, control signals from the interfaced device, and module jumpers, this unit can supply variable width pulses or synchronous control levels at amplitudes specified in section 5 below.

3. Storage Register—This 12-bit flip-flop buffer register provides output data storage for information to be transmitted to the interfaced device.

4. Flag Control—Provisions for generation of I/O Skip and Program Interrupt signals for the computer are made in this area.

5. Level Converters—All level converters from the storage register or timing generator are open—collector transistor types which can drive 30 ma at ground. The M730 has npn drivers and can interface loads returned to a maximum positive supply of +20 Volts and the M731 has pnp drivers which can interface loads returned to a maximum negative supply of −20 Volts. Level converters which input control signals to the Flag control can receive signals of the same polarity and magnitude as the output drivers can sustain.

Thresholds on the input converters are +1.5 Volts and −1.5 Volts for the M730 and M731 respectively. All positive voltage levels are compatible with K and M series and all negative voltage signals are compatible with R, B and W Series.

For additional information, technical specifications and applications assistance, a Digital module specialist can be contacted at any Digital Sales office. Application Note AP-M-017 contains useful information concerning the use of the M730 and M731.

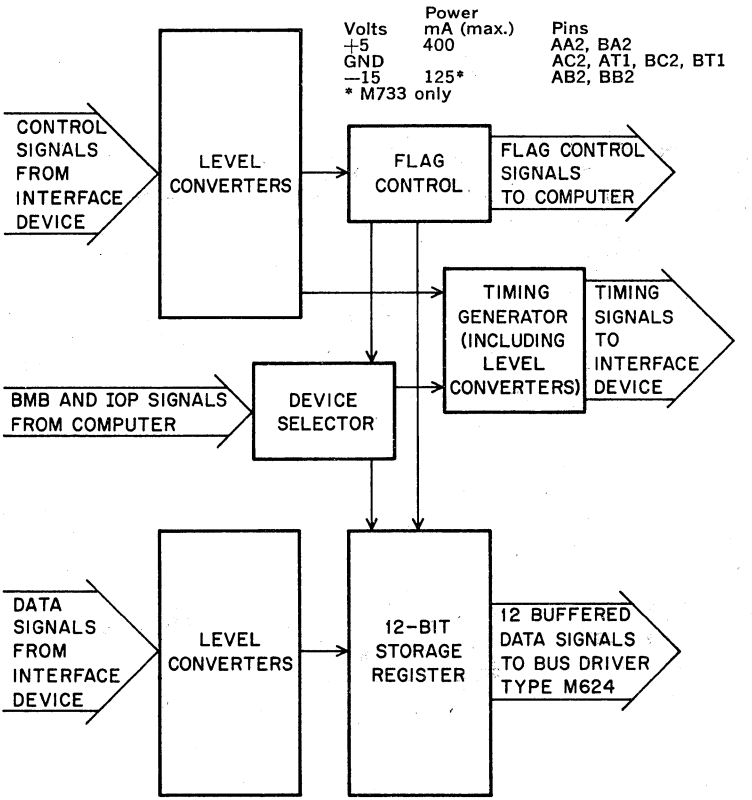
M732 & M733
BUS INTERFACES

8-FAMILY POS. I/O BUS

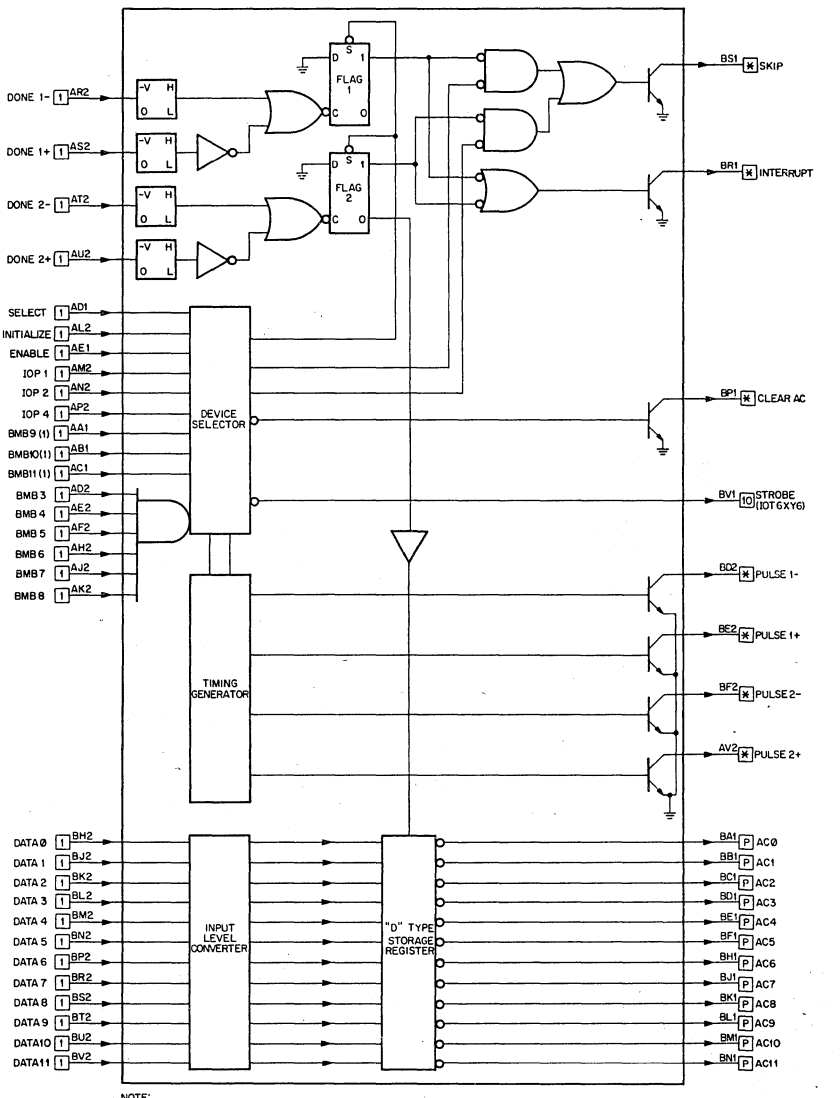
M SERIES

Length: Standard
Height: Double
Width: Single

Price:
M732 — $160
M733 — $165

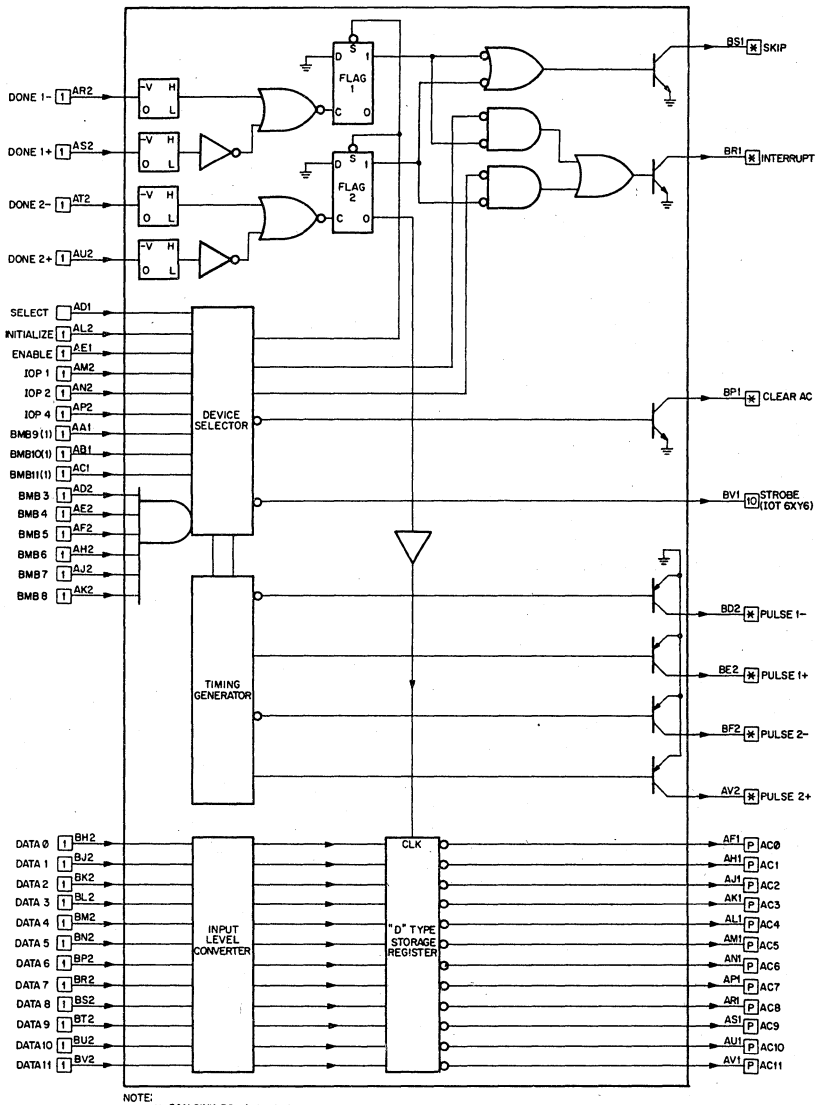


The M732 and M733 interface modules provide extremely flexible interface control logic to connect devices, systems, and instruments to the input half of the programmed I/O transfer bus of either a positive bus PDP8/I or PDP8/L computer. Peripheral equipment which operates either asynchronously or synchronously to a computer and expects to transmit data to that computer, can to a large degree be interfaced by either the M732 or M733. Basic restrictions on the device or system to be interfaced are simply that it transmit data in parallel, provide one or more control lines, and operate at a data transfer rate of less than 20KHZ. Complete interfaces to such peripheral gear as card readers and other repetitive devices is possible using the M732 and M733; however, part of the controlling functions such as counting, etc., must be performed by computer software.



NOTE: *=CAN SINK 30mA AT GROUND

BUS INTERFACE — M732 (POSITIVE INPUT)



NOTE:
*=CAN SINK 30mA AT GROUND

BUS INTERFACE — M733 (NEGATIVE INPUT)

Functionally, these modules contain five distinct sections which are as follows:

1. Device Selector—This logic network converts the buffered memory buffer (BMB) signals and IOP timing pulses from the computer into internal module control pulses.

2. Timing Generator—Through the use of device selector signals, control signals from the interfaced device, and module jumpers, this unit can supply variable width pulses or synchronous control levels at amplitudes specified in section 5 below.

3. Storage Register—This 12-bit flip-flop buffer register provides input data storage of information received from the interfaced device. Information is loaded into this register by a control line from the peripheral.

4. Flag Control—Provisions for generation of I/O Skip and Program Interrupt signals for the computer are made in this area.

5. Level Converters—All level converters from the timing generator are open collector transistor types which can drive 30 mA at ground. The M732 has npn drivers and can interface loads returned to a maximum positive supply of +20 Volts and the M733 has pnp drivers which can interface to a maximum negative supply of −20 Volts. Level converters which input control and data signals to these modules can receive signals of the same polarity and magnitude as the output drivers can sustain. Thresholds on the input converters are +1.5 Volts and −1.5 Volts for the M732 and M733 respectively.

   All positive voltage levels are compatible with K and M Series and all voltage signals are compatible with R, B, and W Series.

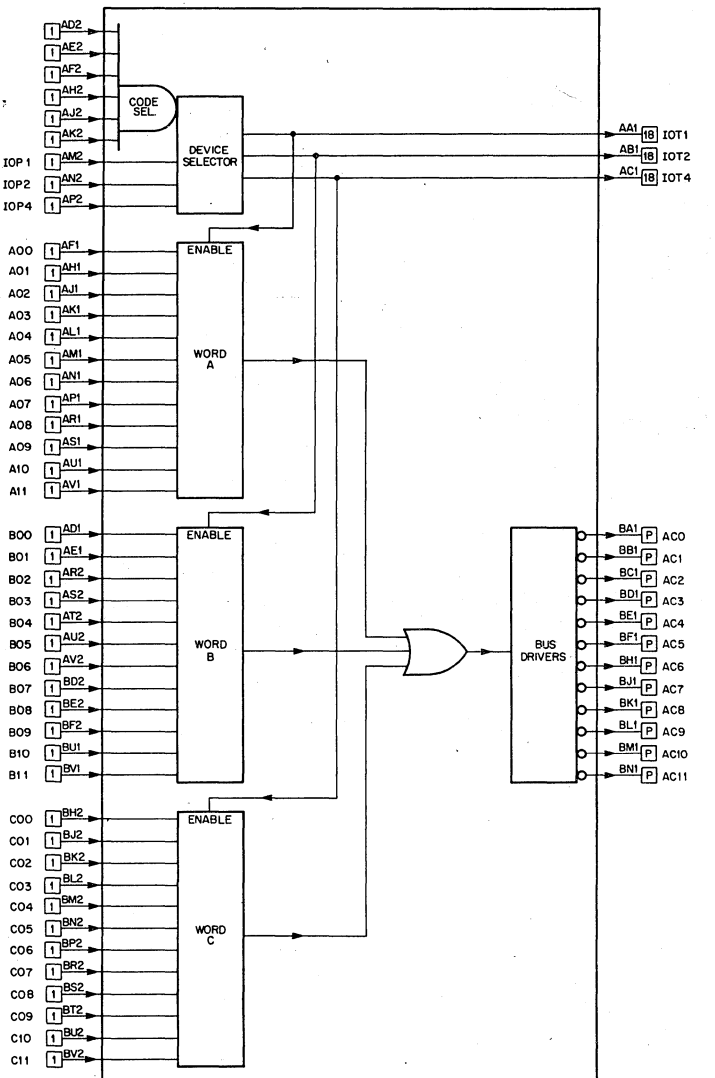
For additional information, technical specifications and applications assistance, a Digital module specialist can be contacted at any Digital Sales Office. Application Note AP-M-018 contains useful information concerning the use of the M732 and M733.

M734
I/O BUS INPUT MULTIPLEXER

8-FAMILY POS. I/O BUS

M SERIES

		Volts	Power mA (max.)	Pins	Price:
Length:	**Standard**	+5	325	AA2, BA2	
Height:	**Double**	GND		AC2, AT1, BC2, BT1	**$105**
Width:	**Single**				



The M734 is a three-word multiplexer used for strobing 12-bit words on a positive voltage input bus, usually the input of the PDP-8/I or the PDP-8/L. Device selector gating is provided. The data outputs of the M734 Multiplexer consist of open collector NPN transistors which allow these outputs to be directly connected to the bus.

FUNCTIONS

Code Select Inputs: When a positive AND condition occurs at these inputs, the pulse inputs IOP1, IOP2, and IOP4 are enabled for use in strobing input data. The code select inputs must be present at least 50 ns prior to any of the three signals that they enable. If all select inputs are not required, unused inputs must be tied to a source of +3 volts (pin AL2). These inputs are all clamped so that no input can go more negative than −0.9 volts.

IOP1, 2, 4: These 50 ns (or longer) positive pulse inputs strobe 12-bit words A, B, and C to the bus driver. All three lines are clamped so that no pulse input can go more negative than −0.9 volts.

Data Inputs: Bits 0-11 on words A, B, and C are strobed 12 bits at a time. Bus driver output lines (0-11) correspond to the selected word input lines (0-11). A HIGH data input forces a bus driver output to ground during a data strobe. Data signals must be present at least 30 ns prior to issuance of IOP 1, 2, or 4.

Bus Driver: These open collector NPN transistor bus driver outputs can sink 100 mA at ground. Each driver output is protected from negative undershoot by a diode clamp. When this module is used with the PDP-8/I or PDP-8/L, these outputs would be connected to the accumulator input lines of the I/O bus. Typical rise and fall times at these outputs with a 100 mA resistive load are 100 ns.

Data Strobes: Pins $\overline{AA1}$, AB1, and AC1 appear coincident with IOP1, IOP2, and IOP4 respectively only if the code select inputs are all HIGH.

+3 Volts—Pin AL2: Can hold 19 inputs at a logic HIGH level.

PRECAUTIONS

Bus driver maximum output voltage must not exceed +20 volts.

M735
I/O BUS TRANSFER REGISTER

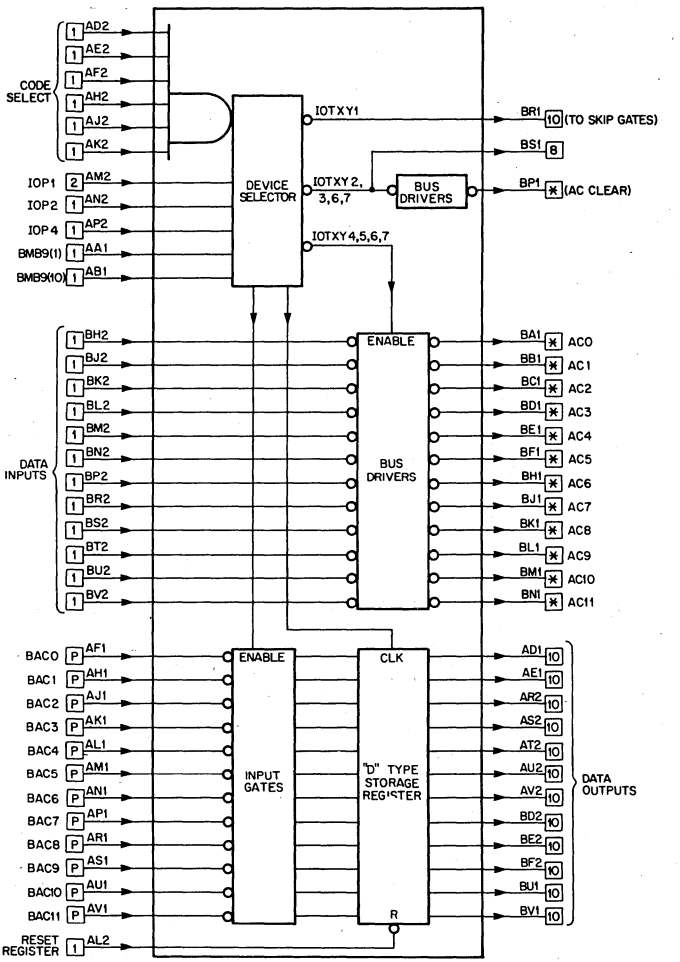
8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Double
Width: Single

Price:

$135



NOTE:
*= CAN SINK 100mA TO GROUND

Volts	Power mA (max.)	Pins
+5	425	AA2, BA2
GND		AC2, AT1, BC2, BT1

The M735 provides one 12-bit input bus driver and one 12-bit output buffer register for input and output data transfers on the positive I/O bus of either a PDP8/I or a PDP8/L. Device selector gating plus additional signal lines provide the flexibility necessary for a complete interface with the exception of flag sense signals. Use of the M735 is not restricted to a computer, as it can be used in many systems to provide reception and transmission of data over cables.

Inputs:
All inputs present one TTL unit load with few exceptions as noted in the functional descriptions below:

Code Select Inputs: When a positive AND condition occurs at these inputs, the pulse input gates for IOP1, IOP2, and IOP4 are enabled for use as detailed below. The code select inputs must be present at least 50 nsec prior to any of the three signals that they enable. If all select inputs are not required, unused inputs must be tied to a source of +3 Volts. These inputs are all clamped so that no input can go more negative than −0.9 Volts. When this module is used with the PDP8/I or PDP8/L these inputs would be connected to BMB outputs 3-8 to generate a device code. Where required in discussions below, this 6-bit device code will be referred to as code XY.

IOP1, 2, 4, BMB9(1) and BMB10(1): These three IOP's 50 nsec or longer positive pulse inputs, in conjunction with control level inputs BMB9(1) (Pin AA) and BMB10(1) (Pin AB1) provide all of the necessary signals for operation of this module. Table 1 below indicates the recommended use of these pulses and levels. A"1" or "0" in this table indicates the presence or absence respectively of a pulse (an IOP) or the logic level at pins AA1 or AB1.

IOP 4	IOP 2	IOP 1	BMB 9(1)	BMB 10(1)	PDP/8 Mnemonic	Module Operation
0	0	1	0	0	IOTXY1	+3V → OV output pulse on pin BR1 used for skip function.
0	1	0	0	1	IOTXY2	+3V → OV output pulse on pin BS1, bus driver output on BP1 pulsed to ground and is used for the AC clear function.
0	1	1	0	1	IOTXY3	Load output register from accumulator outputs on IOP1 execute IOTXY2.
1	0	0	1	0	IOTXY4	Data inputs strobed onto accumulator inputs.
1	0	1	1	0	IOTXY5	Load output register on IOP1, Execute IOTXY4.
1	1	0	1	1	IOTXY6	Execute IOTXY2, and IOTXY4.
1	1	1	1	1	IOTXY7	Execute IOTXY3, and IOTXY4.

The M735 module operation as associated with the various mnemonic IOT codes is quite explicit with the exception of IOTXY5. This code (IOTXY5) would be used to load zeros into the M735 with IOTXY1 and then to load into the AC the data present at the data inputs of the bus driver when IOTXY4 occurs. In this particular operation the AC has been effectively cleared as the content of the AC was zero during IOTXY1 thereby allowing the transfer of data into the AC without the use of the AC clear command usually generated by IOT2.

Although it is not implicit from Table 1, BMB9(1) and BMB10(1) inputs are gated in a positive OR circuit, so that when the M735 is not used on a PDP8/I or PDP8/L I/O bus one of these inputs can be grounded and the other used for control. They must appear at least 50 nsec prior to an IOP pulse. If the M735 is used with one of the above computers, these inputs must be tied to the corresponding I/O bus lines. The input load on IOP1 is two TTL unit loads. All five inputs are clamped so that no input can go more negative than —0.9 Volts.

Data Inputs: Each data input when at ground, enables the corresponding bus driver output to be pulsed to ground during IOTXY4. A high input will inhibit the bus driver from being strobed. Since each input is ANDed with IOTXY4, any change of data after this strobe begins will change the bus driver output.

Accumulator Inputs: The input level presented to these inputs will be the same as that assumed by the buffer outputs after executing inputs strobes IOTXY, 5, or 7. Input data must be present at least 50 nsec prior to an IOP. Each input is protected from negative undershoot by a diode clamp.

Reset Register Pin AL2: A positive pulse of 50 nsec or longer at this input sets all buffer outputs to ground. When high, this input overrides any data loading from the accumulator inputs. The output register will be cleared within 70 nsec from the rising edge of this input. Diode input clamping is provided to limit negative undershoot to —0.9 Volts.

Outputs:
Pin BR1: This output can drive ten TTL unit loads and has a propogation delay of less than 20 nsec. See Table 1.

Bus Driver: These open collector npn transistor bus driver outputs, including pin BP1, can sink 100 ma. at ground. The maximum output voltage cannot exceed +20 Volts and each driver output is protected from negative undershoot by a diode clamp. When this module is used with the PDP8/I or PDP8/L, output pins BA1—BN1 would be connected to the accumulator input lines and pin BP1 to the clear accumulator line of the I/O bus. Typical rise and fall TTT of these outputs with a 100 mA. resistive load are 100 nsec.

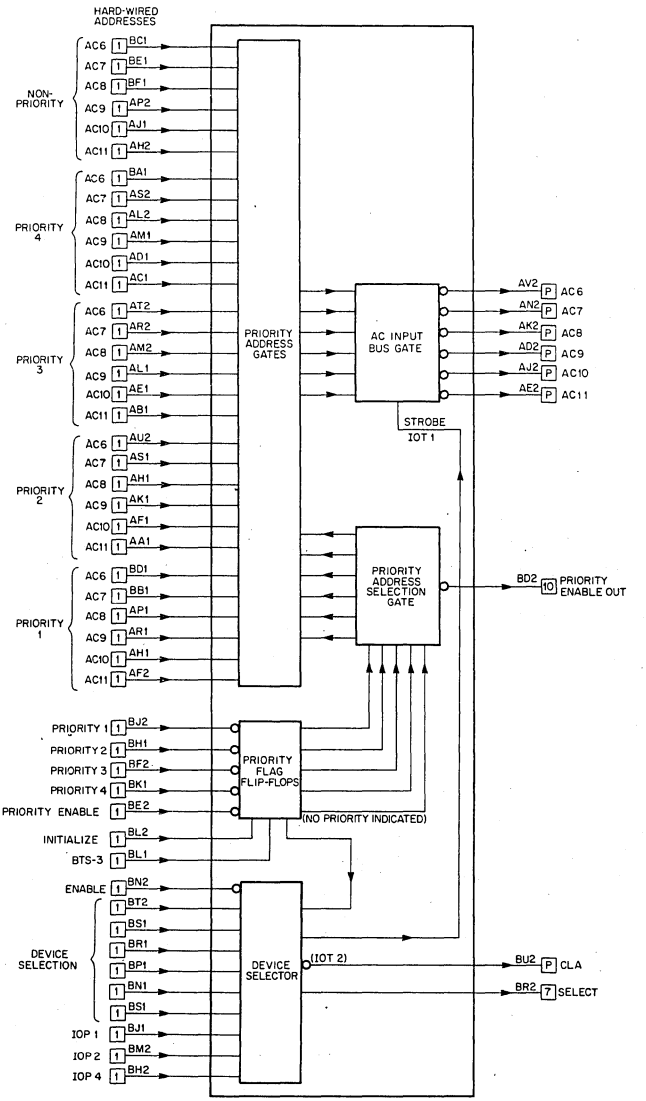
Buffer Outputs: Each output can drive ten TTL unit loads.

M736
PRIORITY INTERRUPT MODULE

8-FAMILY POS. I/O BUS

M SERIES

		Volts	Power mA (max.)	Pins	Price:
Length:	**Standard**				
Height:	**Double**	+5	400	A2	
Width:	**Single**	GND		C2, T1	**$125**



The M736 is used in conjunction with the PDP8/I or 8/L to provide the capability of assigning priorities to various I/O devices connected to the I/O bus of the computer. The M736 can be used to assign priorities for one thru four external devices. Priority assignment may be provided for more than four devices by using additional M736 modules for each additional group of four devices. All M736's in a particular priority system would utilize the same device code.

THEORY OF OPERATION

Basically the M736 module consists of the following:

1. The M103 device selector function.
2. A Bit Time State-3 (BTS-3) input.
3. Four priority input lines.
4. Priority enable line, input and output.
5. Five groups of six gates, each of which is capable of being hard wired to provide address information to locate subroutings to service the various devices associated with the priority interrupt system. The output of each of these gates is strobed onto the accumulator input bus on lines AC(6) thru AC(11).

SEQUENCE OF OPERATION

The external device activates its skip and/or interrupt FLAG flip-flop. The activation of the FLAG causes two things to happen; (a) The computer's interrupt request line is pulled to ground. This tells the computer that an external devices requires service and requests the computer to jump to an I/O priority interrupt service subroutine as soon as the computer completes its present cycle. (b) The external device FLAG pulls to ground the appropriate hard wired priority line connected to a "D" flip-flop in the M736.

A Bit Time State-3 (BTS-3) pulse from the computer is applied to the clock input of the "D" flip-flop to which the activating device flag is connected, as mentioned in section 1b above, and causes this flip-flop in the M736 to set. If more than one priority devices called to be serviced at the same time, all of the associated priority "D" flip-flops in the M736 would be set at this time. The outputs of the priority flip-flops in the M736 are connected to a priority gate structure which is arranged in such a manner that only one output line will be activated and that line will be associated with the external device with the highest priority.

This activated output of the priority gate structure is applied to one group of six two-input gates which make up the address gate. The other input of each of the six two-input gates of the address gate is hard wired to provide a discrete address which will correspond to the starting location of the particular subroutine associated with that priority request. Each of the six output lines of the activated address gates is applied to one input of a two-input gate of the AC input strobe gate.

The computer now has had time to jump to the priority interrupt service routine and now issues a device selection code corresponding to the hard wired device selection code assigned to the M736 priority interrupt modules. This device selection code will pre-enable the IOP gates of the M736 of M736's.

The computer now issues an IOP-2 pulse to the IOP-2 gate of the M736 module. The output of the IOP-2 gate now produces an IOT-2 pulse which causes the "Clear the AC" line of the I/O bus to be pulled to ground, and thereby clears the AC.

The computer issues an IOP-1 pulse to the IOP-1 gate of the M736 module. The output of the IOP-1 gate produces an IOT-1 pulse which is applied to the strobe inputs of the AC input bus gate. As the other inputs of the AC input bus gate are connected to the outputs of the address gate, appropriate lines of the AC input bus (AC 6 thru AC 11) will be pulled to ground thereby loading into the AC the starting address of the subroutine associated with the particular priority I/O device to be serviced.

The computer now refuses to accept any further interrupt requests and jumps to the subroutine with the particular starting address which was loaded into the AC. The service routine of the particular priority device contains an instruction to clear the interrupt flag flip-flop of the particular I/O device and at the end of the subroutine issues the M736 device selector code with an IOP-4 which clears the priority flag flip-flops of the M736. The computer now turns on the priority interrupt system capability which allows the computer to service any future interrupt requests.

USING THE M736 PRIORITY INTERRUPT MODULES

1. Assign a device selection code to the M736 priority system and connect the device selection inputs of the M736 to the proper device selection lines to assure decoding for that code. If more than one M736 is used connect the device selection lines for each M736 in exactly the same manner. Each M736 will use the same device selection code.
   These inputs are: BT2, BS1, BR1, BP1, BN1 and BS2.
2. Connect the enable input, BN2, of each M736 to +3V.
3. Connect the IOP-1 input, BJ1, to the IOP-1 bus line.
4. Connect the IOP-2 input, BM2, to the IOP-2 bus line.
5. Connect the IOP-4 input, BH2, to the IOP-4 bus line.
6. Connect the BTS-3 input, BL1, to the BTS-3 bus line.
7. Connect the outputs of the external I/O device flag flip-flops to the priority

NOTE: In normal operation, IOP-4, is not required as the flag flip-flop in the external priority I/O device is cleared by the subroutine servicing that device. When the flag in the I/O device is cleared, the next BTSO3 pulse will load the disabled flag outpu tinto its respective priority flag flip-flop in the M736 effectively clearing the priority flag flip-flop. flip-flop.

inputs in such a manner as to pull the corresponding priority input line of the M736 to GRD when the device flag is activated. These inputs are as follows:

1st priority	BJ2	1st	M736 Module
2nd priority	BH1	"	" "
3rd priority	BF2	"	" "
4th priority	BK1	"	" "
5th priority	BJ2	2nd	" "
6th priority	BH1	"	" "

Carry on for additional priority interrupt devices.

8. Assign starting address to the subroutines which will service each priority interrupt device attached to the priority interrupt system. Also assign a starting address for the subroutine to service non-priority devices. Hard-wire the various starting address of the service routines as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Priority 1	BD1	BB1	AP1	AR1	AH1	AF2
Priority 2	AU2	AS1	AN1	AK1	AF1	AA1
Priority 3	AT2	AR2	AM2	AL2	AE1	AB1
Priority 4	BA1	AS2	AL2	AM1	AD1	AC1
NON-Priority	BC1	BE1	BF1	AP2	AJ1	AH2

NOTE: If more than four external I/O devices require priority assignments, the NON-priority address inputs BC1, BE1, BF1, AP2, AJ1 and AH2 of the M736 module used for the first four highest priorities, *must* be connected to GRD. If more than two M736 modules are required all of the NON-priority address lines of each module except the last M736 containing the lowest priorities, must be connected to GRD. The NON-Priority address is hardwired to the NON-Priority address inputs of only the lowest priority M736 module. All un-used priority address inputs must be grounded. Logic 1 level for address may be obtained from module pin BV2 of each M736 module. Lower priority addresses would be hardwired on succeeding M736 modules in the same order hard wired to the second M736 module as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Priority 5	BD1	BB1	AP1	AR1	AH1	AF2
Priority 6	AU2	AH2	AK2	AD2	AJ2	AE2

9. Connect the AC input bus gate outputs to the AC bus as follows:

	AC(6)	AC(7)	AC(8)	AC(9)	AC(10)	AC(11)
Module Pins	AV2	AH2	AK2	AD2	AJ2	AE2

10. Connect the Priority Enable input line BE2, of the M736 with the highest priorities, or the only priorities, to ground.

11. If lower priorities of 5 or more are assigned, connect the Priority output of the module with the higher priorities, Pin BD2, to the next M736 module (with the next following four lesser priorities) Priority enable input pin BE2.

12. Last, but not least, connect the INITIALIZE input, BL2 to the Initialize line of the computer I/O bus.

M737
12-BIT BUS RECEIVER INTERFACE

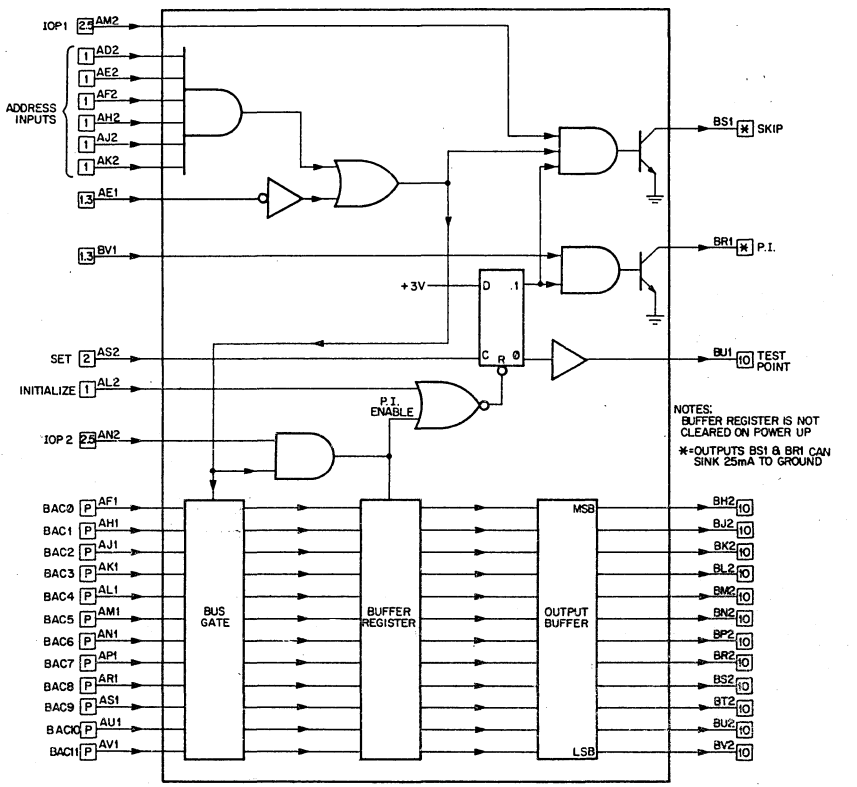
8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Double
Width: Single

Price:

$120



Volts	Power mA (max.)	Pins
+5	300	AA2, BA2
GND		AC2, AT1, BC2, BT1

The M737 12-Bit Bus Receiver Interface is completely contained on a double height, single width module.

The M737 was designed primarily to receive and store in a buffer register twelve parallel data bits from the positive bus of the PDP-8/I or PDP-8/L. The M737 is pin compatible with the M738 Counter-Buffer Interface, the M107 Device Selector, the M108 Flag Module, and the 12-Bit Bus Paneloid E100. The 12-Bit Bus Receiver Interface, M737, consists of three basic sections: device selector, flag, and buffer register section.

Device Selector Section
The device selector section contains six address inputs which are to be connected to the proper BMB bits for address selection. IOP 1 input is used to generate an IOT 1 which is used internally to test the flag. The output of flag test gate is connected directly to the skip bus with an NPN transistor. The output of the address selection gate is connected to the bus gate of the buffer register section and functions as an option select level. IOP 2 is used for two purposes. It is internally connected in such a manner as to clear the flag and to load the buffer register with the contents of the BAC lines.

The Flag Section
The flag section is used to generate a programmed interrupt. The flag flip-flop may be set by a level shift from low to high (a positive going voltage) applied to the set input at pin AS2. The output of the flag is connected to the P. I. line by way of a P. I. enable gate and an open collector NPN transistor. The output of the flag is also connected to pin BU1. The flag is reset by IOP2 applied to pin AN2 or by initialize pulses applied to Pin AL2.

Buffer Register Section
Data from the bus is applied to the inputs of the bus gate. The bus gate prevents the buffer register from loading the bus when M737 is not addressed. The bus gate is enabled by the option select level derived internally from the output of the device selector section. The buffer register is loaded by jam transfer upon the command of an IOT2 instruction. The output of the buffer register is buffered by the use of TTL circuitry.

Inputs: All inputs which receive positive bus signals are protected against negative voltage undershoot. AE1, BV1 represent 1.25 TTL unit loads. These two inputs need not be tied to a logic 1 source when not used.

AM2, AN2 represent 2.5 TTL unit loads.

AS2 represents 2 TTL unit loads.

All other inputs represent 1 TTL unit load.

Outputs: BS1, BR1 will sink 25 MA to ground. Voltage applied to these outputs must not be allowed to exceed +20 Volts. These outputs are protected against negative voltage undershoot and consist of open collector NPN transistors.

All other outputs will drive 10 TTL unit loads.

M738
COUNTER-BUFFER INTERFACE

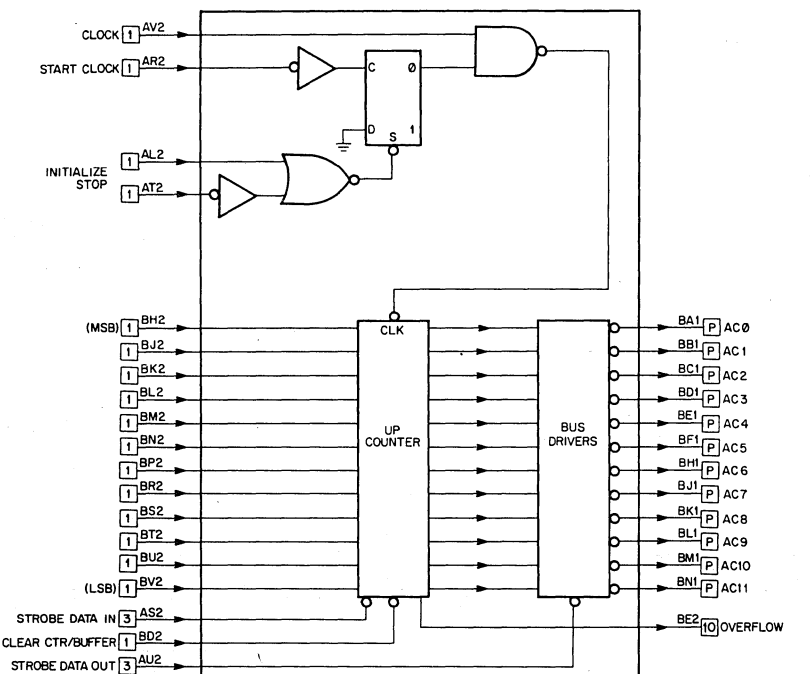
8-FAMILY
POS. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$105



Volts	Power mA (max.)	Pins
+5	*	AA2, BA2
GND		AC2, AT1, BC2, BT1

*250 mA—no strobe onto bus
370 mA—during bus strobe

The M738 provides a 12-bit binary up-counter that can be read to the positive external I/O bus of a PDP-8/I or PDP-8/L. The counter can be cleared or preset to a starting value by a jam transfer from an external device. When a count enable flag is set, the counter operates as an up-counter in response to external clock pulses. The content of the counter can be strobed to the I/O bus through data gates under program control.

APPLICATIONS

- Interfacing a counting register to I/O bus
- Parallel buffered data transfer to I/O bus

FUNCTIONS

Loading Counter/Buffer: The 12-bit counter/buffer consists of three MSI, 4-bit presetable counters connected in tandem. Twelve parallel bits of data may be applied to the data inputs and then transferred into the counter by the application of a LOW level (250 ns or longer) to the STROBE DATA IN pin AS2. This input could be an IOT pulse from an M102 or M107.

Clearing Counter/Buffer: The counter may be cleared by a logic LOW at least 3 μs in duration applied to the CLEAR COUNTER/BUFFER input pin BD2. The requirement of a 3 μs pulse precludes the direct use of an IOT pulse for clearing the counter. If it is required to clear the counter by an IOT pulse, an M302 dual delay multivibrator could be used to stretch the IOT pulse length.

Bus Driver: The 12-bit bus driver strobes the contents of the buffer counter onto the bus when a logic LOW is applied to the STROBE DATA OUT pin AU2. The input to the STROBE DATA OUT pin AU2 would normally be an IOT pulse derived from an M103 or M107.

All bus driver outputs consist of open collector NPN transistors which are capable of sinking 25 mA to ground. Voltage applied to these outputs must not exceed +20 volts. The outputs are diode-protected against negative voltage undershoot in excess of −0.9 volts.

CLOCK ENABLE Flip-Flop: The clock enable flip-flop gates clock pulses to the counter/buffer. This flip-flop may be cleared by a logic HIGH pulse to pin AL2 or by a logic LOW to the STOP input AT2. When the flip-flop is cleared, clock pulses applied to the clock input, pin AV2, are not counted.

Counting: Clock pulses may be counted by setting the COUNT ENABLE flip-flop with the application of a logic LOW pulse to the START CLOCK input AR2. The four inputs—CLOCK, START CLOCK, STOP and INITIALIZE—require a minimum pulse width of 50 ns and, therefore, could use IOT pulses derived from the device selectors M103 or M107.

Tandem Operation: At times, it may be desirable to connect two or more M738 module counters in tandem. This may be accomplished by connecting the "overflow" output pin BE2 of the first M738 to the START CLOCK input pin AR2 of the next M738. Also, the signal on pin AR2 must be inverted and connected to CLOCK pin AV2. The clear pulse time duration should be an additional 3 μs for each M738 added in tandem: i.e., 24 bits would require a 6 μs clear pulse.

M783
UNIBUS DRIVERS

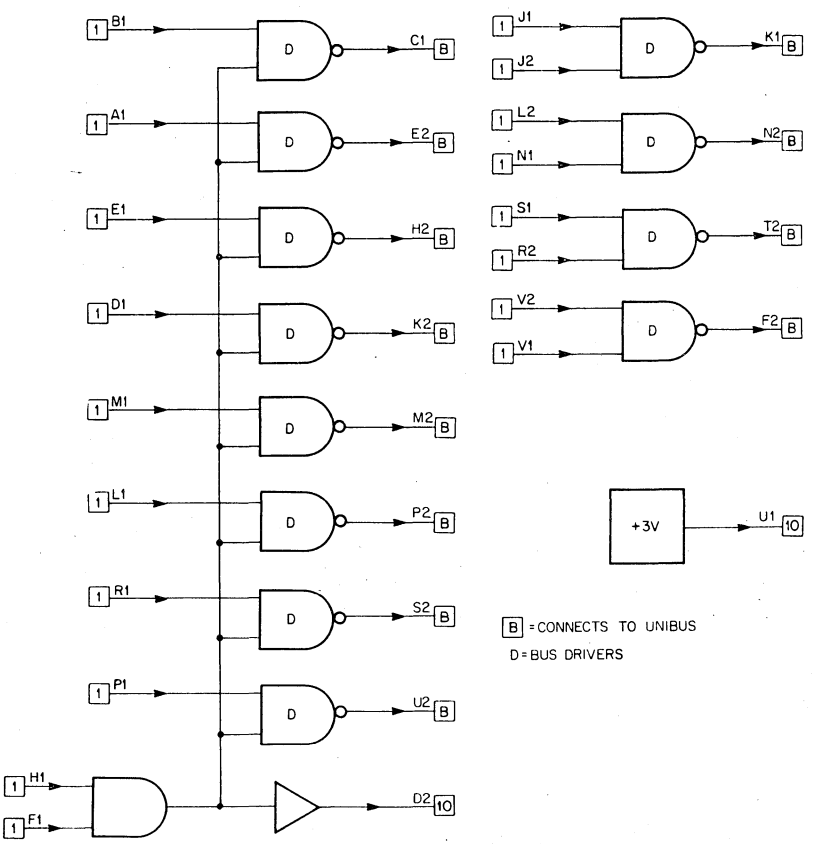
PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single

Price:

$30



Volts	Power mA (max.)	Pins
+5	70	A2
GND		C2, T1

The M783 consists of 12 drivers to be used as an input interface to the UNIBUS of the PDP-11. Pin U1 provides +3 volts as a source of logic HIGH for 10 TTL loads.

M784
UNIBUS RECEIVERS

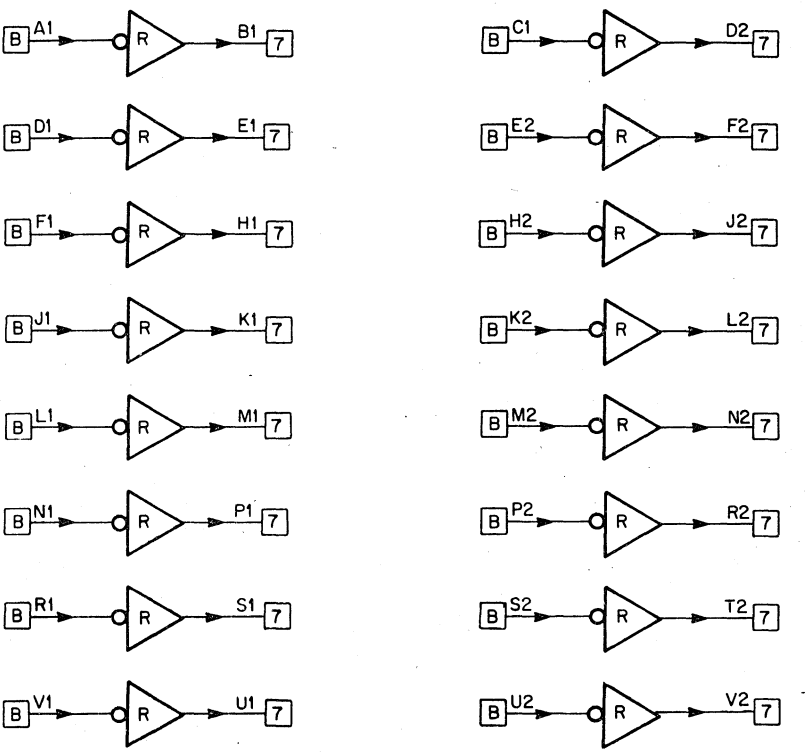
PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single

Price:

$30



Volts	Power mA (max.)	Pins
+5	200	A2
GND		C2, T1

R= BUS RECEIVER
B =CONNECTS TO UNIBUS

The M784 consists of 16 inverting receivers that are used as an output interface from the UNIBUS of the PDP-11.

SPECIFICATIONS

Input Loading: All inputs present one UNIBUS receiver load. (See UNIBUS description.)

Output Drive: Each output has a fan-out capability of 7 standard TTL loads.

M785
UNIBUS TRANSCEIVER

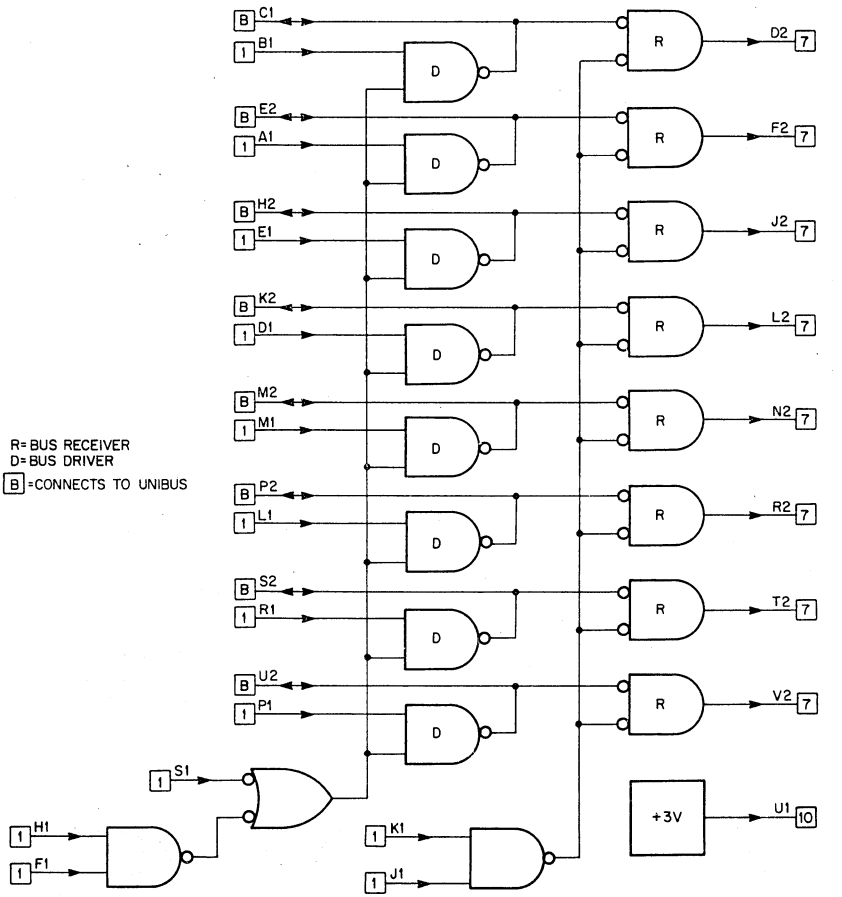
PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single

Price:

$35



Volts	Power mA (max.)	Pins
+5	118	A2
GND		C2, T1

The M785 consists of eight drivers and eight receivers for use as a device interface with the PDP-11 UNIBUS. Pin U1 provides +3 volts and has an output capability of 10 TTL loads. Driver gates have open collectors and are capable of sinking 50 mA with a collector voltage of less than 0.8 volts.

M786
DEVICE REGISTER INTERFACE

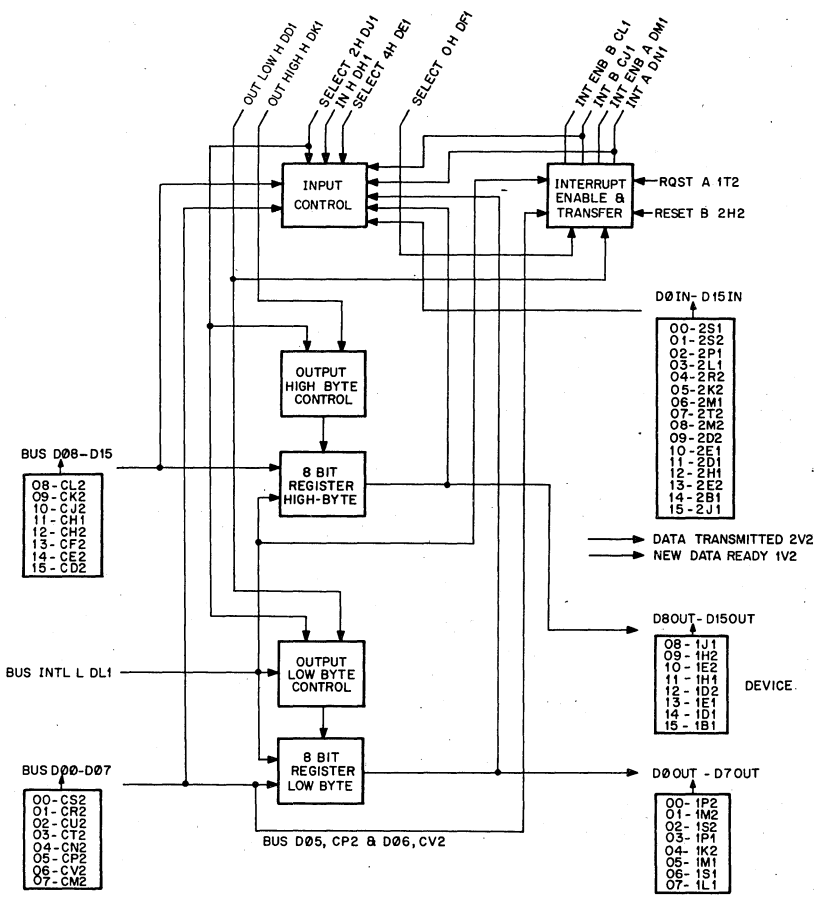
PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Double
Width: Single

Price:

$220



Volts	Power mA (max.)	Pins
+5	600	AA2, BA2
GND		AC2, BC2
		AT1, BT1

The M786 is a PDP-11 interface module containing all the logic necessary for transfers of 16-bit input and output data between a PDP-11 system and an external device. All I/O connections are made using the connector blocks mounted on the module.

APPLICATIONS

For interfacing to the PDP-11, the M786 must be used with the M105 Address Selector. The M105 decodes the UNIBUS address lines and causes transfer of information through the M786 module under program control. Interrupt circuitry is also built into the M786 module and can be used in conjunction with the M7820 module or equivalent. An example of a typical PDP-11 interface using the M786 module is illustrated in Figure 1.

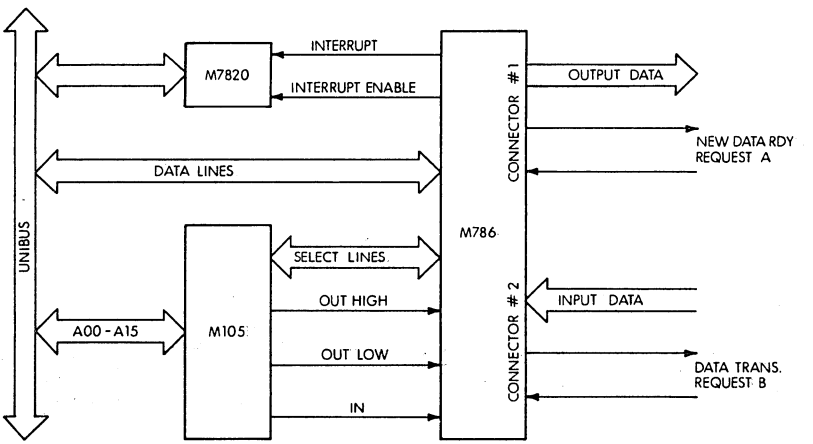


Figure 1. Typical PDP-11 Interface

FUNCTIONS

Registers: The M786 module contains a 16-bit register interfaced to the computer bus data lines by ungated receivers. Data from the computer is clocked into the registers by strobing signals OUT LOW with SEL 2 and OUT HIGH with SEL 2 derived from the M105 module. The user has the option of reading whole words (OUT LOW with SEL 2 and OUT HIGH with SEL 2) or 8-bit bytes (OUT LOW with SEL 2 for a low byte and OUT HIGH with SEL 2 for a high byte). All register outputs go to I/O connector No. 1 where cables from an external device can be attached.

The M786 module signals the external device through the NEW DATA signal each time new data is loaded into the 16-bit register. Register outputs may be read back onto the computer bus by program-enabling the IN 4 and SEL 2 signals from the M105 module.

Drivers: Sixteen bits of TTL data may be received from an external device via cables attached to I/O connector No. 2. These input lines are protected by clamping diodes to prevent input signal swings above or below the normal TTL levels. Each of these input signals can be read onto the computer bus by means of bus drivers which are enabled by the IN H and SEL 4 signals from the M105 module.

The M786 module signals the external device through the DATA TRANSMITTED signal that data has been read onto the computer bus.

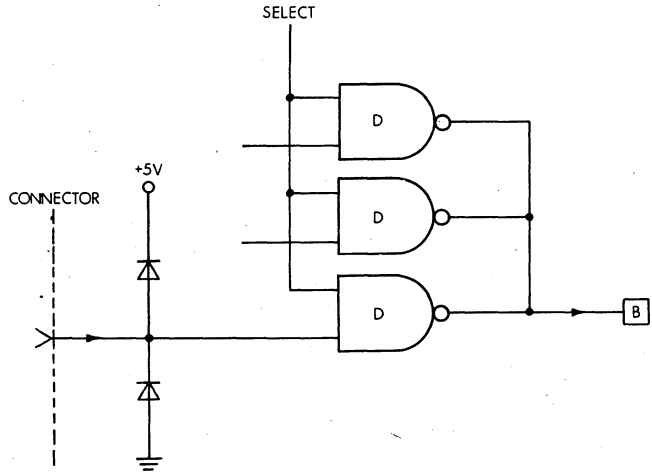


Figure 2. Typical Input Circuit

Interrupt: Each I/O connector also has an additional request line (REQUEST A on connector No. 1, REQUEST B on connector No. 2) which may be asserted High by the external device to initiate an interrupt or to generate a flag that may be tested as part of a peripheral status-checking program. Whether these two request lines cause an interrupt is determined by two Interrupt Enable flip-flops (INTR ENB A, INTR ENB B) which may be set under program control to enable interrupt capability for either an A or B interrupt or both if dual interrupts are required.

For interrupt capability, an INTR ENB and a REQUEST signal are applied to an M7820 module or equivalent. These two signals must be both A or B signals; for example INTR ENB A and REQUEST A.

The priority level of both interrupts on the M786 module must be the same, with the interrupt which is back panel-wired closest to the processor having the highest sublevel priority. The M786 module contains a priority jumper plug which is normally set at BR5. If other priorities are desired, different plugs may be purchased.

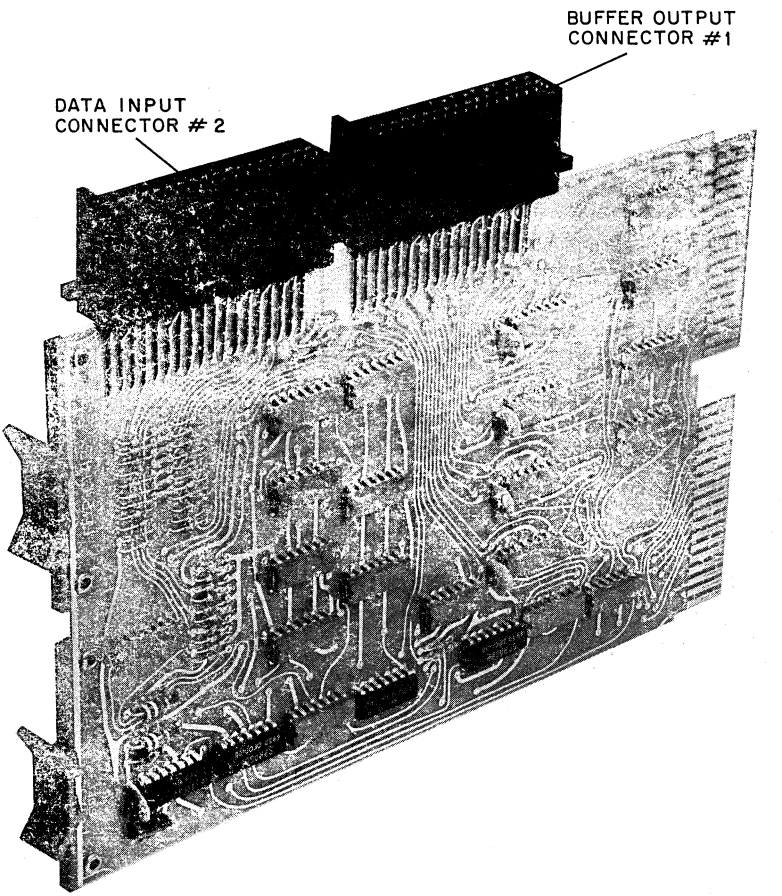
Status Gates: Status gates on the M786 module give the programmer the ability to check the states of the REQUEST and INTR ENBL signals. These gates are software-enabled through the address selector (M105 module) signals SEL 0 and IN H.

SPECIFICATIONS

Propagation Time:

FROM	TO	ns (max)
Bus DATA	I/O Connector	100
I/O connector	Bus DATA	35
Flag Clock Inputs	Flag output	40

I/O Connector Cables:
The I/O connector accepts the M904 and M927 Cable Connectors which contain solder lugs and can be used with ribbon cable, twisted pair cable, or open wire.



M786 Device Register Interface

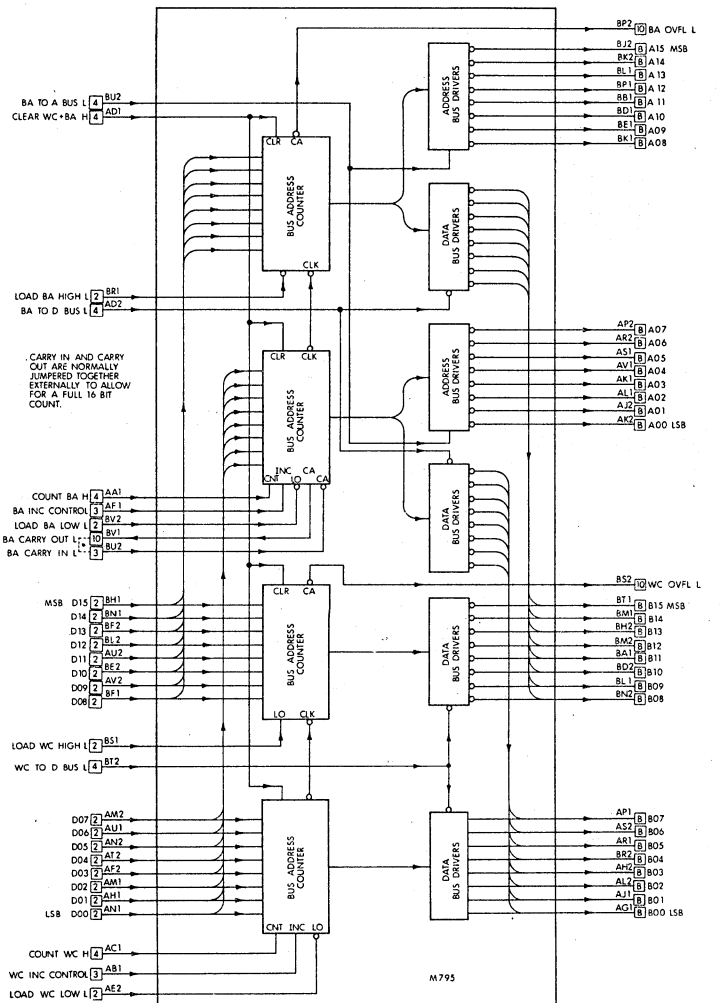
M795
WORD COUNT AND BUS ADDRESS MODULE

PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Double
Width: Single

Price: $200



Volts	Power mA (max.)	Pins
+5	600	AA2, BA2
GND		AC2, AT1, BC2, BT1

The M795 Word Count and Bus Address Module is used to interface Direct Memory Access (DMA) devices to the UNIBUS. This module contains two 16-bit counters. One counter is used to count the number of data transfers that occur. The other counter is used to specify the bus address of the data to be transferred.

FUNCTION

Word Counter

Block transfer devices that function as bus master during data transfers usually require two registers to hold the parameters of the transfer. One parameter is the transfer word count. Initially, this register (WC) is loaded with the 2's complement of the number of items to be transferred to or from memory. This number is placed on the BUS DATA lines (D00-D15) and clocked into the WORD COUNT register in two 8-bit bytes using the LOAD WC L (low byte) and LOAD WC + 1 L (high byte) inputs. After each data transfer is complete, the WC register is incremented by clocking the COUNT WC H input. If the new value of the WC register is 0 which is indicated by an overflow at the WC OVFL L output, further transfers are inhibited and the block transfer is complete. Information can be transferred in either words (16 bits each) or bytes (8 bits each), because the WC register may also be used as a byte counter.

Address Counter

The second parameter used in block transfers is the transfer address. Initially, a bus address register (BA Counter) is loaded with an address that specifies the memory location to or from which data is to be transferred. This address is loaded from the BUS DATA lines (D00-D15) in two 8-bit bytes using the LOAD BA L (low byte) and LOAD BA+1 L (high byte) inputs. The BA register is incremented after each transfer by clocking the CLOCK BA H input. The register continually "points" to sequential memory locations.

BUS Drivers

Outputs of both the Word Counter and BA Counter are connected to a set of UNIBUS drivers so that the counter contents can be gated to the DATA BUS when the appropriate enable signals (BA TO BUS L and WC TO D BUS L) are asserted. In addition, the BA register has a set of drivers with independent outputs to allow it to drive the ADDRESS BUS when the BA TO BUS L input is asserted.

Counter Increments

The BA register can be incremented by either 1 or 2 as a function of the BA INC CONTROL input (High=1, Low=2). This incrementation capability allows addressing of either sequential bytes or words. The register is incremented on the trailing edge of a positive pulse applied to the COUNT BA H input of the register. The carry between bits 03 and 04 is broken and brought out to pins BV1 (BA CARRY OUT L) and BU1 (BA CARRY IN L). Normally these pins are connected together externally to allow for a full 16-bit count. They can, however, be controlled to inhibit the carry and to force repeated addressing of 16 sequential byte addresses. This feature can be used in device-to-device transfers. An overflow pulse (BA OVFL L) is provided as an output whenever the register is incremented from all 1's to all 0's.

The WC register is incremented by either 1 or 2 as a function of the WC INC CONTROL input (High=1, Low=2). The register increments on the trailing edge of a positive pulse applied to the COUNT WC H input of the register. An overflow pulse is also available at pin BS2 (WC OVFL L). Both registers reset to 0's whenever the CLEAR WC+BA H signal is asserted.

The storage elements on the M795 module are not edge triggered devices. Data must be established and held for the duration of the loading pulse.

APPLICATIONS

This module is used to interface direct memory access (DMA) devices to the UNIBUS.

SPECIFICATIONS

Propagation Time:

FROM	TO	ns (max.)
CLEAR WC+BA	WC+BA Outputs	125
LOAD WC L	WC Outputs	75
LOAD WX+1 L	WC Outputs	75
COUNT WC H	WC Outputs	60
LOAD BA L	BA Outputs	75
LOAD BA+1 L	BA Outputs	75
COUNT BA H	BA Outputs	60

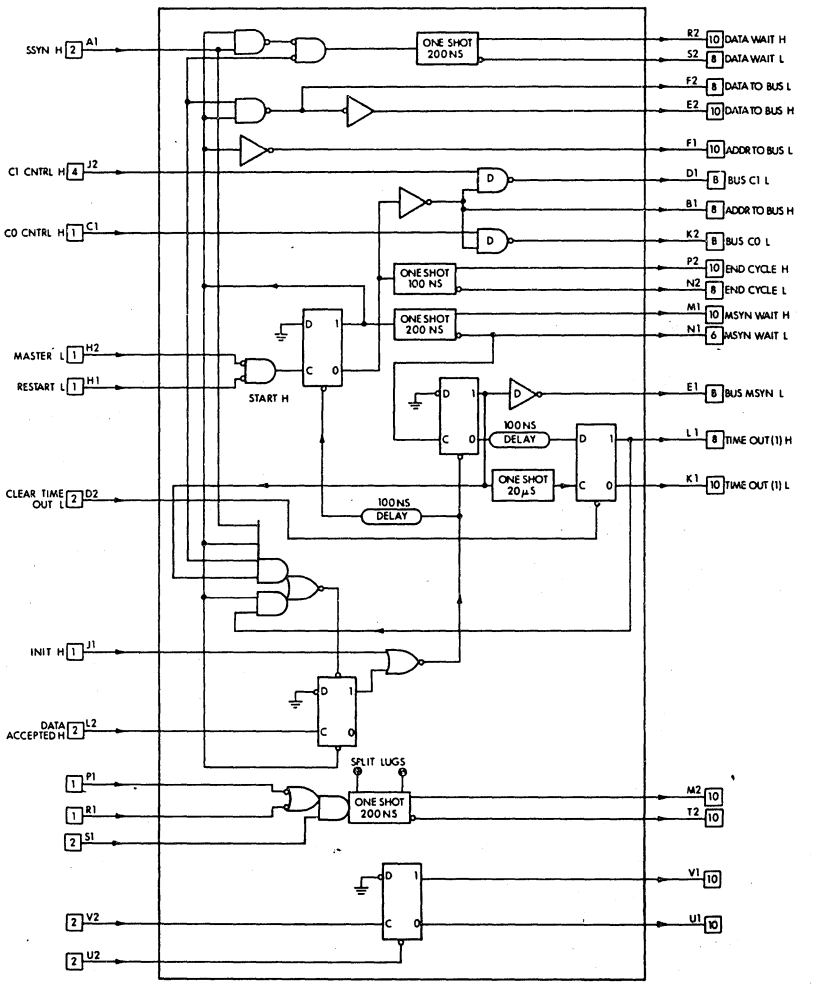
M796
UNIBUS MASTER CONTROL

PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single

Price: $100



Volts	Power mA (max.)	Pins
+5	130	A2
GND		C2, T1

The M796 UNIBUS Master Control Module provides extremely flexible control operations on the UNIBUS when a device is functioning as bus master. In addition to controlling the four transfer operations (DATI, DATIP, DATA, and DATOB), the M796 module generates strobe and gating signals which transfer both addresses and data to and from the bus; handles deskewing of data received from the bus; protects against data transfers to nonexistent devices by the use of time-out circuits; and provides a flip-flop and integrating one-shot that can be used by the customer for special control functions.

Any device in the PDP-11 system may have the capability of gaining control of the bus and, as bus master, of transferring data to and from other slave devices on the bus. This operation is performed independently of processor control and is usually referred to as Direct Memory Access (DMA). The logic necessary to gain control of the UNIBUS is provided by either the M7820 or M7821 Interrupt Control modules.

Upon becoming bus master, the device is free to conduct a data transfer. A DATI cycle is performed if the device needs data (either a word or byte) from memory; a DATO cycle is performed if the device is storing a word of data in memory (DATOB cycle for byte storage); a two-cycle DATIP, DATO(B) operation is performed if data held in memory is to be modified as in the case of increment memory or add to memory functions.

In order to execute one of these transfer cycles, the M796 must set Bus C0 and Bus C1 for the required type of data transfer, assert the MSYN signal, and then wait for the SSYN response from the slave. Data must either be gated to the Bus data lines on a DATO cycle or be received and strobed at the proper time on a DATI cycle.

The Bus C1 and Bus C0 outputs of the M796 can directly drive the UNIBUS and are asserted as a function of the control inputs C1 CNTRL H and C0 CNTRL H. Table 1 lists the states of the control inputs for the four possible bus cycles.

Table 1. Control Line Input States for M796

C1	C0	Bus Cycle
L	L	DATI
L	H	DATIP
H	L	DATO
H	H	DATOB

The data transfer sequence is triggered by meeting the AND condition of both Lows and RESTART L (HI). Usually these two inputs are tied together and are connected to the MASTER L signal produced by the M7820 or M7821 Interrupt Control Module. When the AND condition is met, it produces the START signal, which is an internal signal in the M796 module. At the transition of the START signal, both Bus C1 and Bus C0 are asserted as determined by their respective control inputs. The ADRS to Bus signals are also asserted and are used to gate the address of the slave onto the bus address lines (Bus A 17:00). If an output cycle is specified (C1 — 1), the DATA TO BUS signals (both H and L) are also asserted and are used to gate data to be transferred to the slave onto the bus data lines (Bus D 15:00). The MSYN WAIT one-shot outputs are asserted for 200 nanoseconds after START becomes true and are used to clear the interrupt request flags in the master device. When the MSYN WAIT one-shot times out, the BUS MSYN L signal is asserted. The master device then waits for a response from the slave.

In a data output cycle (DATO), assertion of SSYN causes BUS MSYN to be negated immediately. After a 100-nanosecond delay, BUS C1, BUS C0 ADRS TO BUS and DATA TO BUS are negated. When these signals drop, the END CYCLE pulse appears and is usually used to release control of the bus.

In a data input cycle (DATI), the assertion of the SSYN input produces a 200-nanosecond pulse that appears as DATA WAIT. This delay allows time for the incoming data to deskew and settle. The trailing edge of the DATA WAIT pulse can be used to clock data from the slave into the master device. If a strobe pulse is necessary, the trailing edge of DATA WAIT can be used to trigger the one-shot provided on the module. In either case, once data is received, a positive-going edge is applied to DATA ACCEPTED L causing BUS MSYN to be negated initially, followed by negation of ADDR TO BUS, BUS C1, and BUS C0 100 nanoseconds later.

A TIME-OUT flip-flop is set if a SSYN response fails to occur within 20 microseconds after BUS MSYN is asserted. When this flip-flop is set, the bus cycle is not performed. The TIME-OUT flip-flop is cleared by asserting the CLEAR TIME OUT L input.

The M796 module provides a special flip-flop that has the clock (V2), reset (U2), 1 side (V1) and 0 side (U1) available to the customer. The flip-flop is clocked by a positive transition on the clock input.

An integrating one-shot is also provided on the module. This one-shot is triggered whenever the output of the gating input becomes true: $(\overline{R1} + \overline{P1}) - S1$. The output pulse width at pins T2 and M2 is 150 nanoseconds but can be lengthened by adding capacitance across the pair of split lugs on the module. The following equation can be used to determine the approximate value of the added capacitance:

$$T_{pw} = 0.32\ (RC)$$

where T_{pw} is in milliseconds, R is in ohms, and C is in microfarads. (The internal resistance is 5.6 kilohms.)

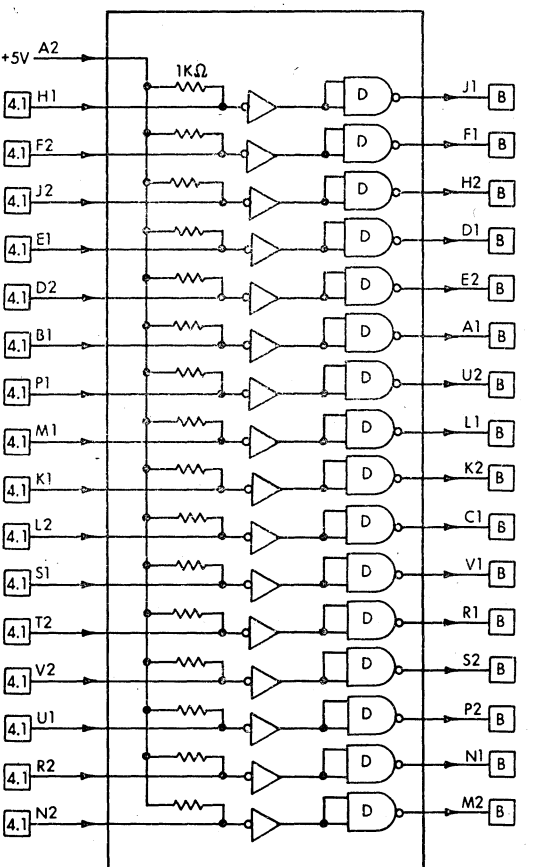
Note that all times mentioned above represent nominal values with a tolerance of ± 25%. The delays and pulses provided by the module are controlled by simple RC circuits: therefore, if the user has any special requirements, part substitutions can be made to alter these time constants.

M798
UNIBUS DRIVERS

PDP-11
UNIBUS

Length: Extended
Height: Single
Width: Single

Price:
$40



Volts	Power mA (max.)	Pins
+5	320	A2
GND		C2, T1

This module consists of 16 noninverting UNIBUS drivers. The module is used in device interfaces to minimize the loading effect caused by attaching several drivers to the same UNIBUS signal line, as in the case of a device containing multiple registers. Loading of signal lines on the UNIBUS is restricted to the equivalent of one UNIBUS receiver input and two UNIBUS driver outputs per device.

In addition, the M798 module allows the UNIBUS to be driven by standard open-collector TTL gates. The inputs to each M798 driver circuit are pulled up to +5 V through a 1-kilohm resistor. As shown in Figure 1, an internal wired OR bus is created that is driven from standard open-collector gates (available on M141 and M149 modules) or from UNIBUS drivers (available on M783 module).

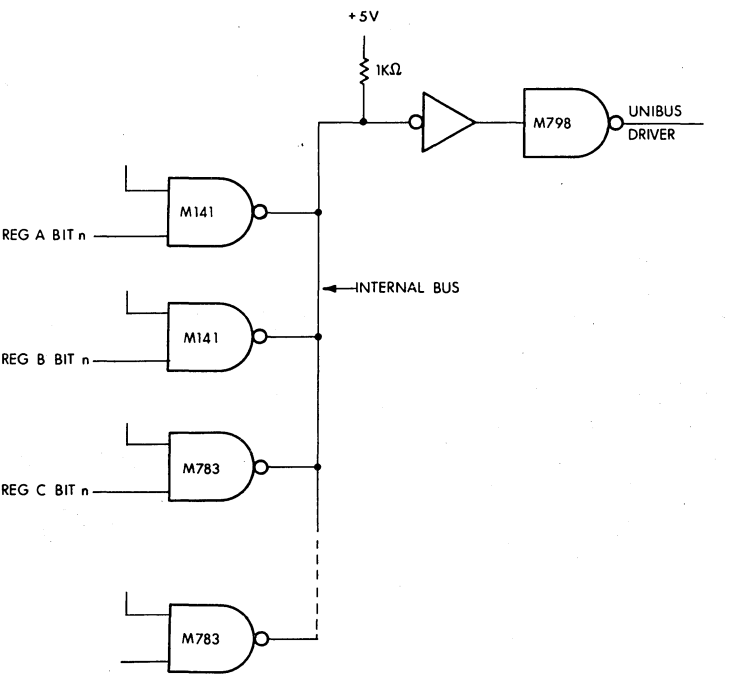


Figure 1. Typical Use of M798

SPECIFICATIONS

Output Driver: The output Low voltage for each of the 16 outputs is 0.8 volts maximum with 50 mA current sink. The output High leakage current is 25 microamperes maximum.

Propagation Delay: The propagation delay between the 16 inputs and the driver outputs is 60 nanoseconds maximum.

M907
DIODE CLAMP CONNECTOR

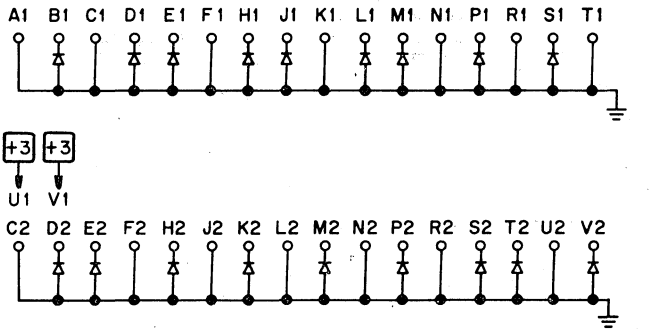
8-FAMILY POS. I/O BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$16



Volts	Power mA (max.)	Pins
+5	10	A2
GND		A1, C1, F1, K1, N1, R1, T1 C2, F2, J2, L2, N2, R2, U2

The M907 is used to provide proper undershoot ground clamps for positive I/O bus signals not using M103 or M101 inputs.

The M907 also provides +3 volts for clamping 25 unused inputs. Diode clamps appear on signal leads used in double-sided alternate-ground I/O cables.

M909
TERMINATOR

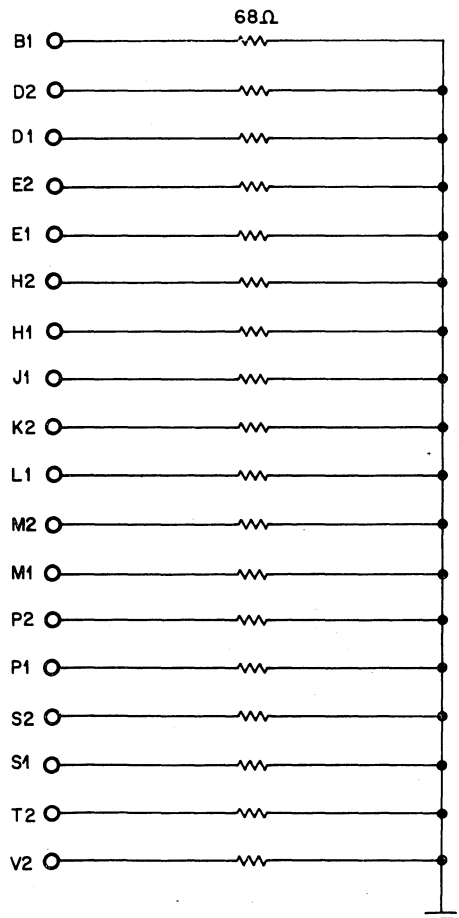
PDP-15
BUS

M SERIES

Length: Standard
Height: Single
Width: Single

Price:

$14



Volts	Power mA (max.)	Pins
+5	NONE	
GND		A1, C1, C2, F1, J2, K1 L2, N1, N2, R1, R2, T1, U2

The M909 module contains eighteen 68-ohm resistors tied to ground through a common bus.

APPLICATIONS

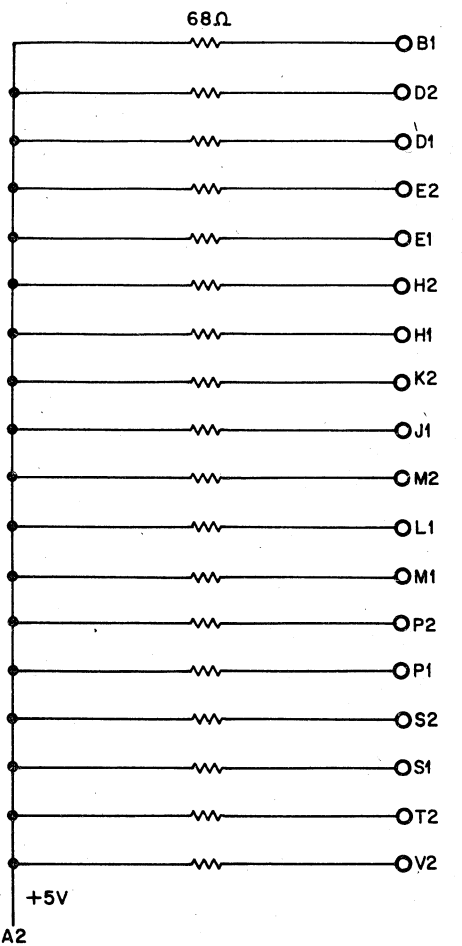
This module is intended to be used with the M910 to form half of the biasing circuit used in the driving network of the M622.

M910
TERMINATOR

PDP-15 BUS

M SERIES

		Volts	Power mA (max.)	Pins	Price:
Length:	**Standard**	+5	1350	A2	
Height:	**Single**	GND		A1, C1, C2, F1, F2, J2, K1 L2, N1, N2, R1, R2, T1, U2	**$20**
Width:	**Single**				



The M910 module contains eighteen 68-ohm resistors tied to a common +5 volt bus.

APPLICATIONS

This module is intended to be used with the M909 to form half of the biasing circuit used in the driving network of the M622.

M1500
BIDIRECTIONAL BUS INTERFACING GATES

UNIBUS/ OMNIBUS

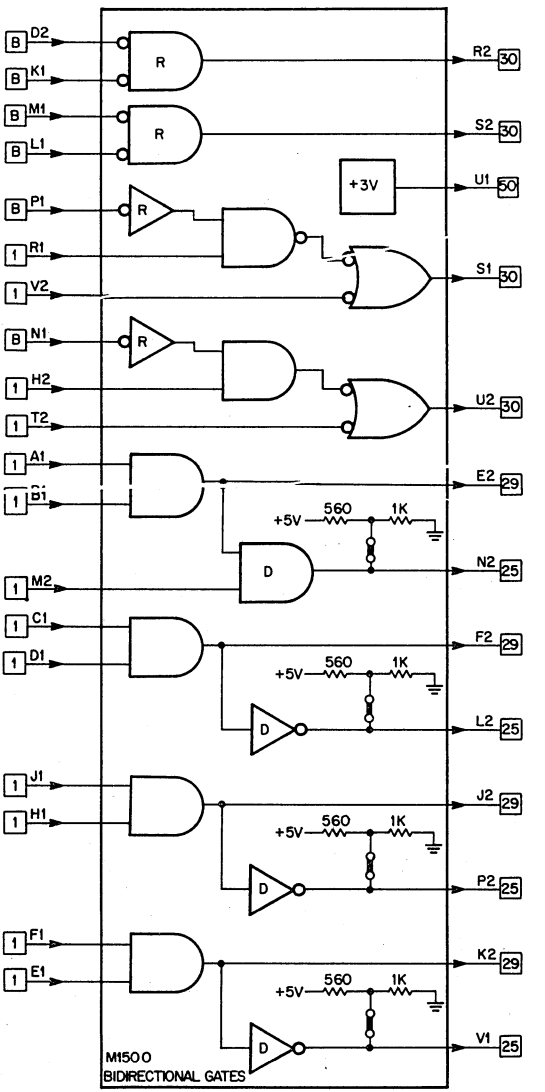
M SERIES

Length: Extended
Height: Single
Width: Single

Volts	Power mA (max.)	Pins
+5	300	A2
GND		C2, T1

Price:

$35



This module provides gating arrangements useful for interfacing to the PDP-8/e, PDP-8/m and PDP-11 computers. It is designed specifically to provide additional gating and output drive when using the M1501-M1502 Input/Output modules. Examples are shown in Figures 1 and 2.

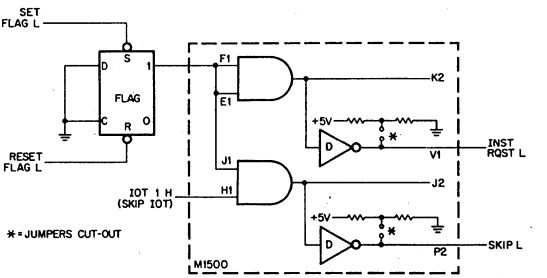


Figure 1. Skip and Interrupt Drivers for PDP-8/e or PDP-8/m Interfacing.

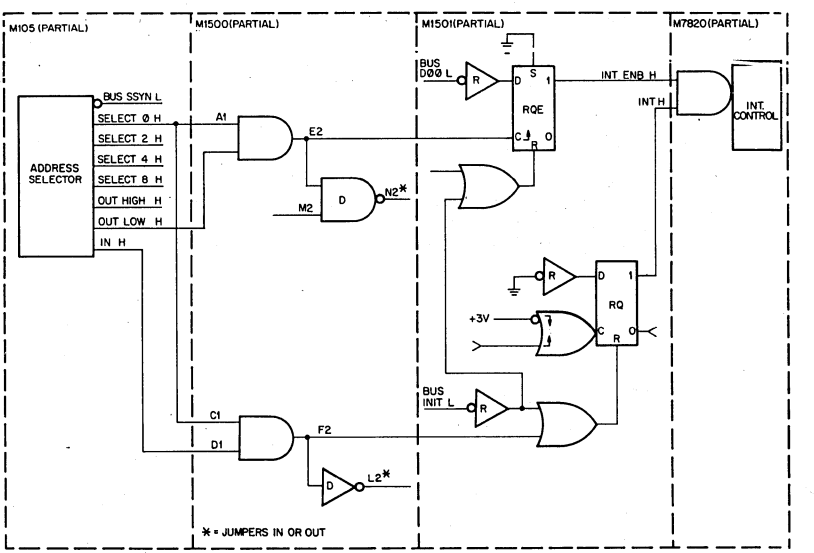


Figure 2. Using M1500 AND Gates with M1501 in PDP-11 Interfacing.

APPLICATIONS

PDP-11 Interfacing:

1. ANDing SELECT signals with direction signals (OUT HIGH, OUT LOW) to load registers
2. ANDing SELECT signals with direction signals (OUT HIGH, OUT LOW) to form set or reset pulses
3. Receiving the INIT (initialize) signal from the UNIBUS and distributing it via high-power drivers

PDP-8/e, PDP-8/m Interfacing:

1. Generation of addditional SKIP and INT RQST signals to supplement those available on the M1510
2. ANDing BTP3 with an IOT for loading registers

General-Purpose Use:

1. Providing general-purpose high fan-out drivers
2. Providing a stage of inversion with high fan-out capability

Restrictions: The module is electrically, but not mechanically, compatible with the PDP-8/e OMNIBUS. Do not plug the module directly into the OMNIBUS. OMNIBUS signals may be connected to appropriate module pins by backplane wiring. This module is designed for use in bus expansion hardware such as:

BB11 Blank System Unit (PDP-11 UNIBUS)
H9190 Bus Expander (PDP-8/e OMNIBUS)

FUNCTIONS

Inputs marked B present one bus receiver load to the UNIBUS or OMNIBUS. All other inputs are standard TTL; unit loads are shown on the logic diagram.

Output drivers marked D provide open collector outputs with jumpered-in pull-up resistors to enable their use in general logic applications. These outputs may be used to drive UNIBUS or OMNIBUS lines if the associated jumpers are cut out by the user.

All other outputs provide standard TTL drive as shown on the logic diagram.

M1501
BUS INPUT INTERFACE

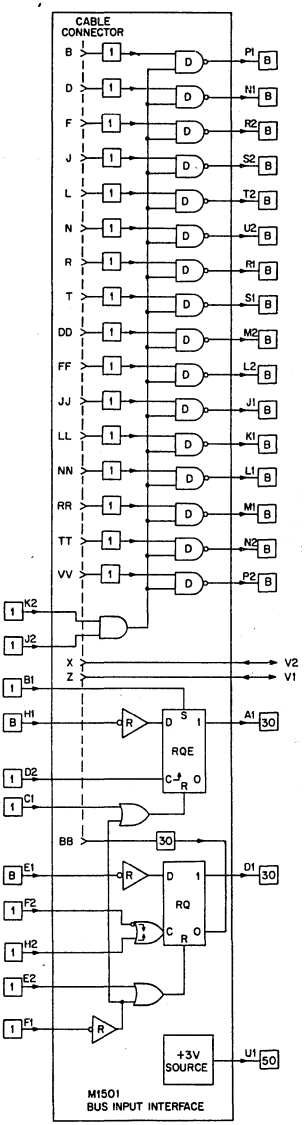
UNIBUS/ OMNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single

Price:

$50



Power		
Volts	mA (max.)	Pins
+5	300	A2
GND		C2, T1

The M1501 contains 16 bus drivers for interfacing parallel input data to a bidirectional data bus structure such as the PDP-11 UNIBUS or the PDP-8/e OMNIBUS. The module includes two control flags that can be used for interrupt request and enable. Data inputs from an external device enter a 40-pin flat cable connector mounted on the module itself. All inputs are diode-clamped to ground and +5 volts.

APPLICATIONS
This module is designed for use in bus expansion hardware such as:

BB11 Blank System Unit (PDP-11 UNIBUS)
H9190 Bus Expander (PDP-8/e OMNIBUS)

Expandability: In PDP-11 applications, up to four M1501 modules (64 bits) can be controlled by one M105 Address Selector module, one M7820 Interrupt Control module, and one M1500 Bus Gates module. Similarly, several M1501's can be combined for multiple word input to a PDP-8/e by using an M1510 Bus Device Selector module.

Restrictions: The module is electrically, but not mechanically, compatible with the PDP-8/e OMNIBUS. Do not plug the module directly into the OMNIBUS. OMNIBUS signals may be connected to appropriate module pins by backplane wiring.

FUNCTIONS
Input from Cable: Data is gated from the input connector to the bus when both loading inputs (AK2, AJ2) are HIGH.

Send/Receive Control Signal: Two additional lines are provided from the cable connector (Pins X and Z) to the module to allow communications between the device and the computer.

Flags: A request flag (RE) and a request enable flag (RQE) are included on the M1501. Both flags can be cleared on start-up directly from the GENERAL CLEAR bus line. Both flag clock inputs are transition sensitive. The data input to each flag is buffered by a bus receiver; thus, status data can be entered directly from a bus line if desired. The request enable flag clock input responds to a HIGH going transition. The request flag has an input that is sensitive to a LOW going transition and an input that is sensitive to a HIGH going transition. (Whichever input is not used should be connected to the proper logic level to unassert it.) The user is given the maximum degree of freedom to use the request enable flag as a D flop or as an RS flop because all inputs are accessible.

The output of each flag is fully buffered to protect the flag data as well as to provide high output drive.

SPECIFICATIONS
Propagation Time:

FROM	TO	ns (max.)
40-Pin Connector Inputs	Bus Data Outputs	50
Flag Clock Inputs	Flag Outputs	75

M1502
BUS OUTPUT INTERFACE

UNIBUS/ OMNIBUS

M SERIES

Length:	**Extended**		Power		**Price:**
Height:	**Double**	Volts	mA (max.)	Pins	
Width:	**Single**	+5	750	A2	
		GND		C2, T1	**$100**

The M1502 is a versatile buffered output interface for up to 16 data bits, arranged in two 8-bit bytes. The module accepts data from a bus structure such as that provided in PDP-8/e or PDP-11. Storage flip-flops are included. Outputs are supplied both to a 40-pin flat ribbon connector and to the backplane. Open-collector output drivers with pull-up resistors are included on the module. Three flip-flops with type D as well as type RS inputs are provided as flags or synchronizing devices.

APPLICATIONS

This module is designed for use in bus expansion hardware such as:

BB11 Blank System Unit (PDP-11 UNIBUS)
H9190 Bus Expander (PDP-8/e OMNIBUS)

Although intended for parallel data output, this module may be used to drive indicators or relays.

Expandability: In PDP-11 applications, up to four M1502 modules (64 bits) can be controlled by one M105 Address Selector module, one M7820 Interrupt Control module, and one M1500 Bus Gates module. Similarly, several M1502's can be combined for multiple word output from a PDP-8/e, by using an M1510 Bus Device Selector module.

Restrictions: The module is electrically, but not mechanically, compatible with the PDP-8/e OMNIBUS. Do not plug this module directly into the OMNIBUS. OMNIBUS signals may be connected to appropriate module pins by backplane wiring.

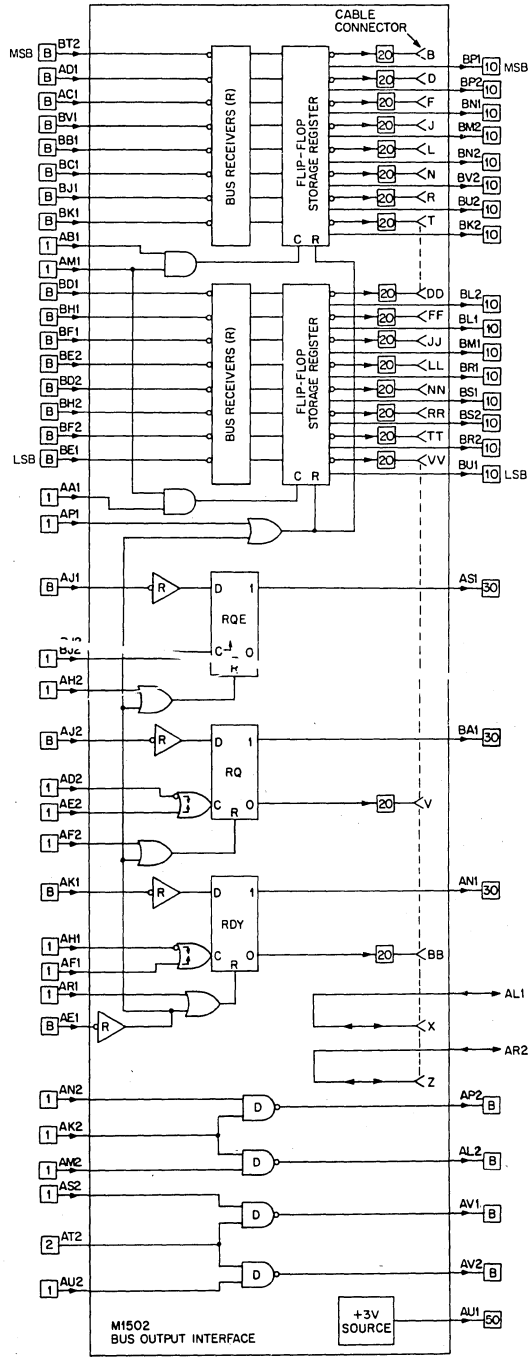
FUNCTIONS

Input from Bus: Data is loaded from the bus to the storage register on a positive transition of the loading input (AM1), which loads all 16 stages. Separate loading inputs are also provided for the lower and upper bytes (AB1 and AA1).

Flags: Three edge-triggered flip-flops are provided. Two of the flags may be triggered by either negative or positive transitions; these supply buffered drive to 40-pin connector outputs. The third flag is triggered by positive-going transitions only, but has a SET input available at the backplane. This flag provides an output to the backplane only.

All flags have separate reset inputs and may also be cleared by a common reset line. The set and reset functions occur on logic HIGH levels. Unused inputs should be connected to a logic level that will unassert them.

Note: Any of the flag outputs can be wired from the backplane to one of the spare bus driver gates (AP2, etc.) for use as READY or INTERRUPT outputs.


CABLE CONNECTOR
MSB
LSB
BUS RECEIVERS (R)
FLIP-FLOP STORAGE REGISTER
RQE
RQ
RDY
+3V SOURCE
M1502
BUS OUTPUT INTERFACE

Spare Lines: Two additional lines are provided between the cable connector and the module for additional communication between the module and the external device. These lines are diode protected against voltage over shoot below −0.75 volts or above +5.75 volts.

SPECIFICATIONS
Propagation Time:

FROM	TO	ns (max.)
BUS DATA Input	40-Pin Output	100
FLAG CLOCK Input	40-Pin Output	150
FLAG SET or CLEAR Input	Backplane Output	100

Output Drive: Outputs to the 40-pin connector are supplied by open-collector high-voltage drivers. Resistors included on the module provide pull-up or current sinking for up to 20 TTL unit loads. If the supplied resistors are removed, the output stages will sink up to 40 mA at logic LOW and will withstand a HIGH level of up to +30 volts. These outputs may therefore be used to drive many types of indicators and even relays. However, if inductive loads are driven, diodes should be wired across each load to swamp inductive kickback.

M1510
BUS DEVICE SELECTOR MODULE

PDP-8/E, 8/M OMNIBUS

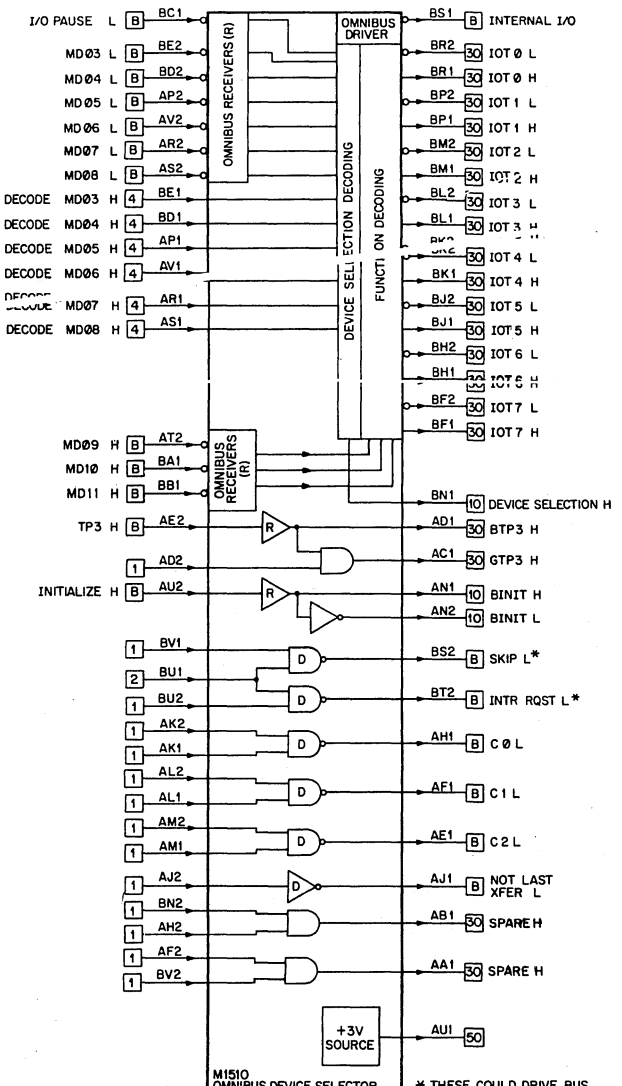
M SERIES

Length: Extended
Height: Double
Width: Single

Volts	Power mA (max.)	Pins
+5	600	AA2, BA2
GND		AC2, AT1, BC2, BT1

Price:

$100



The M1510 Bus Device Selector is designed for use with the PDP-8/e and PDP-8/m computers. It provides a convenient and efficient method of decoding the device code for an interface system. The M1510 decodes the six device selection bits to produce a device selection level. It also decodes the three function selection bits to produce a one-of-eight function level output.

The M1510 contains bus drivers for: SKIP, INT RQST, C0, C1, C2 (control signals), INTERNAL I/O, and NOT LAST XFER; bus receivers for INITIALIZE, TP3, I/O PAUSE, MD LINES; and a binary-to-octal decoder for MD LINE decoding and generating a one-of-eight function level signal.

APPLICATIONS

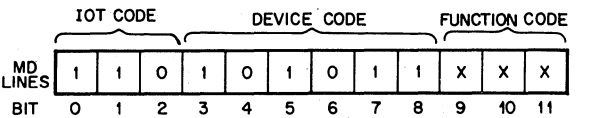
This module is designed for use in bus expansion hardware such as:

H9190 Bus Expander (PDP-8/e OMNIBUS)

Restrictions: The module is electrically, but not mechanically, compatible with the PDP-8/e OMNIBUS. Do not plug the module directly into the OMNIBUS. OMNIBUS signals may be connected to appropriate module pins by backplane wiring.

FUNCTIONS

Decoding: To decode a device code on MD lines 03 through 08, enter the code in the DECODE MD inputs by grounding the zeroes and leaving the ones disconnected. The example below shows the connections that will detect device code 53 (octal).



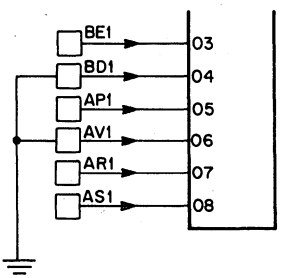


Figure 1. Detecting Device Code 53 (octal)

Spare Circuits: Additional AND gates, open collector NAND gate drivers and non-inverting drivers are available on the M1510. These devices are useful as general M Series devices if some standard bus signals (e.g., TP3, INIT, C LINES) are not needed.

SPECIFICATIONS
Propagation Time:

FROM	TO	ns (max.)
I/O PAUSE	Device Selection Output	100
	IOT Outputs	100

M1621
DVM DATA INPUT INTERFACE

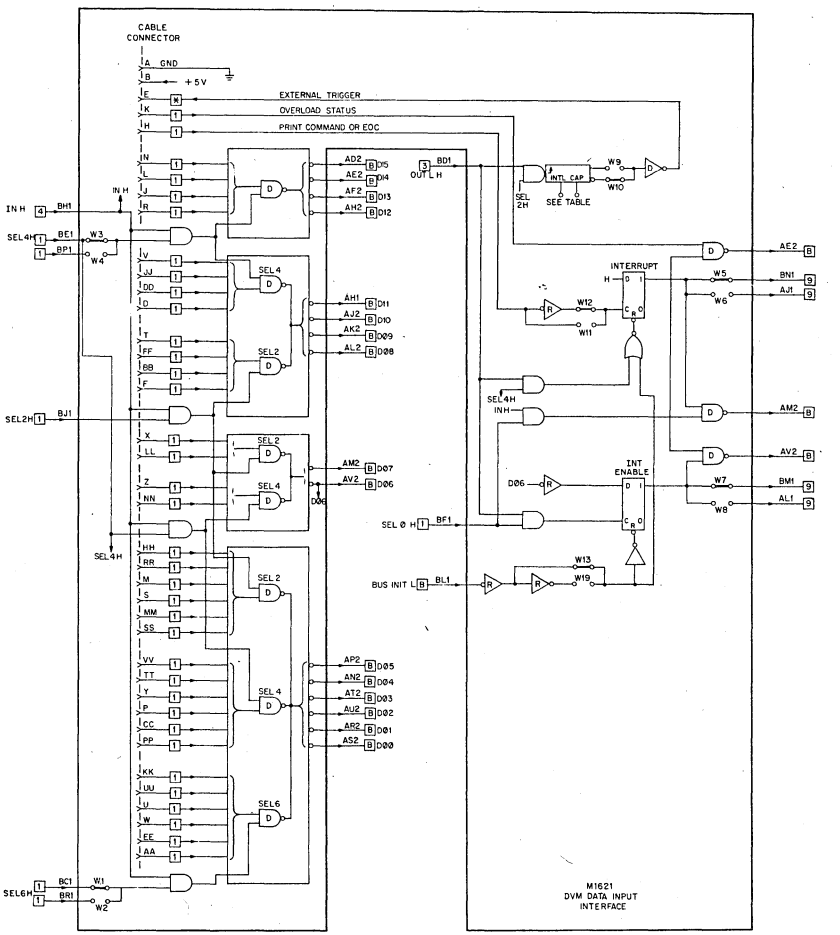
UNIBUS/ OMNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single

Price:

$125



Volts	Power mA (max.)	Pins
+5	777*	A2
GND		C2, T1

* plus current required by instrument

The M1621 is a PDP-11 and PDP-8/e, 8/m interface module containing all the bus drivers and control logic needed to input TTL-level information from several types of digital voltmeters and multimeters. All inputs from the instruments enter a 40-pin cable connector mounted on the module.

Some of the digital voltmeters and multimeters that can be interfaced by the M1621 are:

Fluke	Model 8200A, 8400A
Hewlett-Packard	Model 3450A, 3480A
Data Precision	Series 2000
Systron-Donner	Model 7110
Dana	Model 4800

The user should first compare the interfacing requirements of his particular instrument with the capabilities of this module. Many instrument manufacturers have various control options which should be chosen carefully for compatibility with the M1621.

APPLICATIONS

PDP-11 Interfacing: For interfacing to the PDP-11, the M1621 must be used with the M105 Address Selector (or equivalent). The M105 decodes the UNIBUS address lines and causes transfer of information through the M1621 under program control. Interrupt circuitry is also built into the M1621 and can be used in conjunction with the M7820 or equivalent. An example of a typical PDP-11 interface using the M1621 is illustrated in Figure 1.

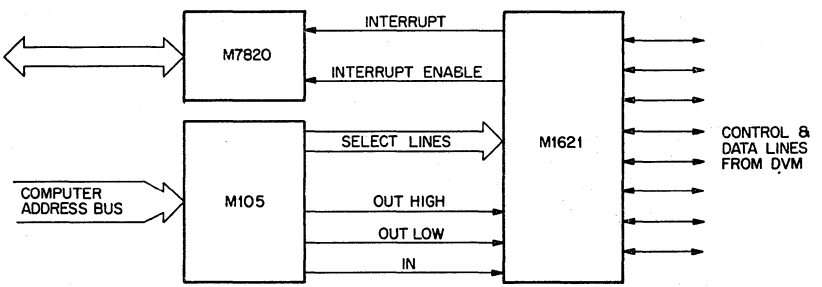


Figure 1. Typical PDP-11 Interface

PDP-8/e Interfacing: To interface to the PDP-8/e, the M1621 must be used with the M1510 Bus Device Selector which performs the same functions as the M105 besides having skip capability. For a PDP-8/e interface, it is necessary to change jumpers on the M1621 control inputs. Remove jumpers W1, W3, and W13. Insert jumpers W2, W4, and W14.

Restrictions: The module is electrically, but not mechanically, compatible with the PDP-8/e OMNIBUS. Do not plug the module directly into the OMNIBUS. OMNIBUS signals may be connected to appropriate module pins by backplane wiring. This module is designed for use in bus expansion hardware such as:

BB11 Blank System Unit (PDP-11 UNIBUS)
H9190 Bus Expander (PDP-8/e OMNIBUS)

FUNCTIONS

Bus Drivers: The bus drivers on the M1621 are arranged in separately enabled groups of input words. A 12-bit word normally transfers the DVM's range and function data outputs. Another 16-bit word transfers the first four digits of data output. The third six-bit word might represent the fifth digit of data output plus the overrange and polarity outputs. Each word can be strobed to the computer bus by signals created by the M105. The output circuits consist of bus drivers connected in a wired-OR arrangement as shown in Figure 2. Note that input lines from the DVM are protected by clamping diodes to prevent input signal swings above or below the normal TTL levels.

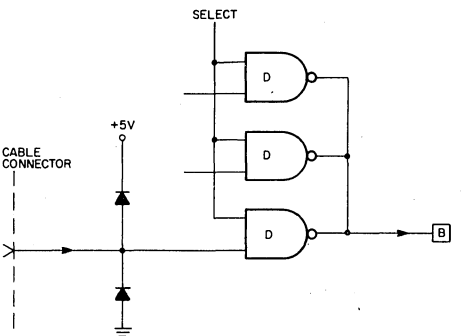


Figure 2. Typical Input Circuit

Flags: The INTERRUPT flag can be set by the PRINT COMMAND or END OF CONVERSION signal from the instrument. Jumpers (W11, W12) are provided which allow the user to select whether the positive or negative transition will set the flag. Interrupt capability is enabled by a second flag INTERRUPT ENABLE, which can be set under program control. Both the INTERRUPT and INTERRUPT ENABLE flags are applied to an M7820 (or equivalent) for computer interrupt. The INTERRUPT flag can be cleared by signals from the M105 (or M1510); both flags are always cleared by computer power up.

Jumper pair W5-W6 selects one of two Interrupt signals (INTR A or INTR B). With W5 in place and W6 removed, INTR A is selected. With jumpers reversed, INTR B is selected.

Jumper pair W7-W8 selects one of two Interrupt Enable signals (INTR ENB A or INTR ENB B). With W7 in place and W8 removed, INTR ENB A is selected. The reverse selects INTR ENB B.

Status Gates: Status gates on the M1621 give the programmer the ability to check the states of the INTERRUPT and INTERRUPT ENABLE flags and the overload status of the external instrument. These gates are software enabled through the address selector (M105 or M1510).

Trigger Pulse Generator: For triggering of external equipment, the M1621 contains a one-shot circuit that can be triggered from the device selector (M105 or M1510). The output pulse width is adjustable from 2 to 12 μs by a trimpot on the module. Longer pulses can be obtained by adding a capacitor at the split lugs on the module. The following equation can be used to determine added capacitance:

$$Tpw=0.32(RC)$$

where Tpw is in milliseconds, R is in ohms, and C is in microfarads. (The internal trimpot varies from 5.2K to 50 K ohms.)

M1623
INSTRUMENT REMOTE CONTROL INTERFACE

UNIBUS/ OMNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single

Price:

$150

The M1623 is a PDP-11 and PDP-8/e, 8/m interface module containing all the bus drivers and control logic needed to remotely program several types of digital voltmeters and programmable power supplies. All outputs to the instrument are through a 40-pin cable connector mounted on the module.

Some of the digital voltmeters and power supplies that can be interfaced by the M1623 are:

DIGITAL VOLTMETERS

Fluke	Model 8200A, 8400A
Hewlett-Packard	Models 3450A, 3480A
Data Precision	Series 2000
Systron-Donner	Model 7110
Dana	Model 4800

PROGRAMMABLE POWER SUPPLIES

Fluke	Models 4210A, 4216A, 4250A, 4265A
Hewlett-Packard	Models 6130B, 6129B, 6131B

The user should first compare the interfacing requirements of his particular instrument with the capabilities of this module. Many instrument manufacturers have various control options which should be chosen carefully for compatibility with the M1623.

APPLICATIONS

PDP11 Interfacing: For interfacing to the PDP-11, the M1623 must be used with the M105 Address Selector (or equivalent). The M105 decodes the UNIBUS address lines and causes transfer of information through the M1623 under program control. Interrupt circuitry is also built into the M1623 and can be used in conjunction with the M7820 or equivalent. An example of a typical PDP-11 interface using the M1623 is illustrated in Figure 1.

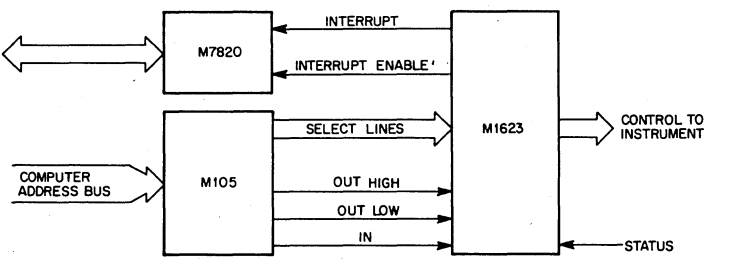
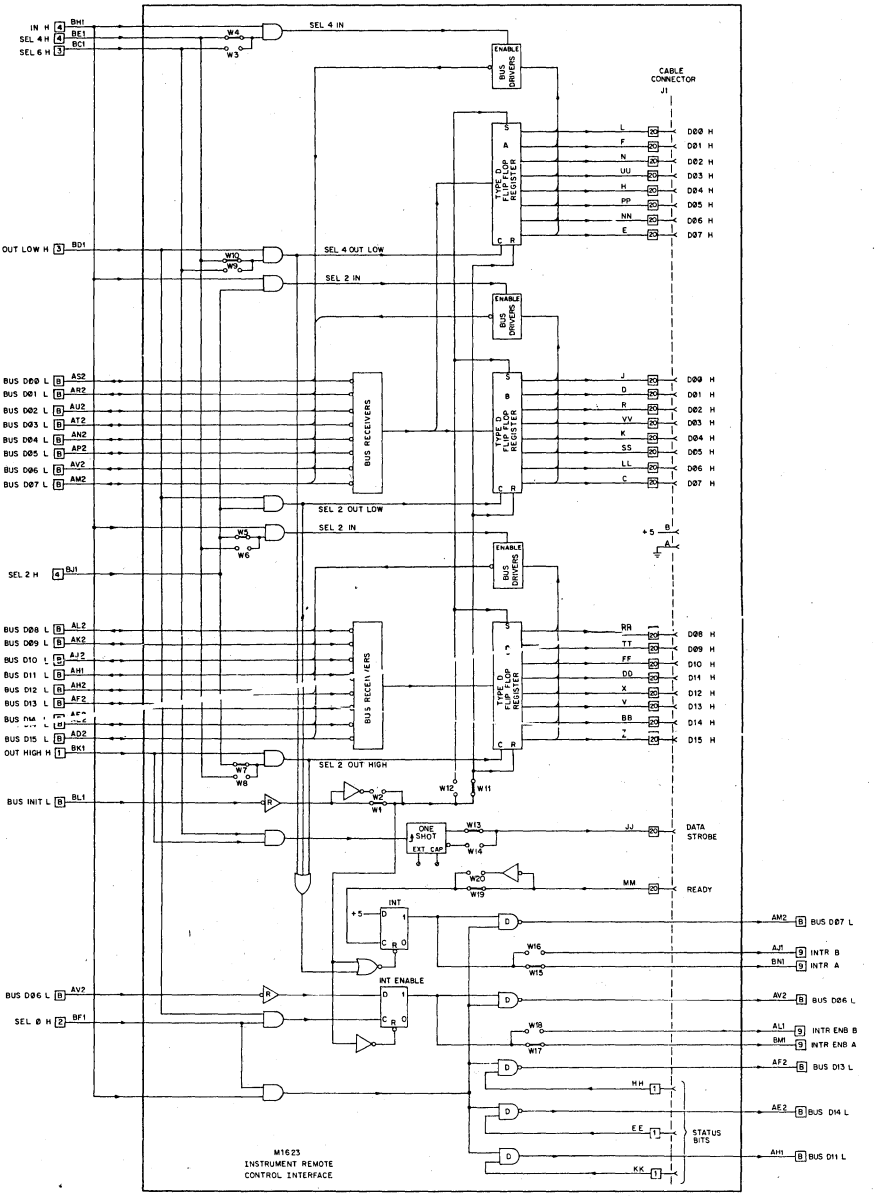


Figure 1. Typical PDP-11 Interface



Volts	Power mA (max.)	Pins
+5	1600 *	A2
GND		C2, T1

*** plus current required by instrument**

PDP-8/e Interfacing: To interface to the PDP-8/e, the M1623 must be used with the M1510 Bus Device Selector which performs the same functions as the M105 besides having skip capability. For a PDP-8/e interface, it is necessary to change jumpers on the M1623 control inputs. Remove jumpers W1, W4, W5, W7 and W10. Insert jumpers W2, W3, W6, W8 and W9.

Restrictions: The module is electrically, but not mechanically, compatible with the PDP-8/e OMNIBUS. Do not plug the module directly into the OMNIBUS. OMNIBUS signals may be connected to appropriate module pins by backplane wiring. This module is designed for use in bus expansion hardware such as:

BB11 Blank System Unit (PDP-11 UNIBUS)
H9190 Bus Expander (PDP-8/e OMNIBUS)

FUNCTIONS

Registers: The M1623 contains two registers, one 8-bit and one 16-bit, both interfaced to the computer bus data lines by ungated receivers. Data from the computer is clocked into the registers by strobing signals derived from an M105 or M1510. The user has the option of strobing whole words or 8-bit bytes. All register outputs go to the 40-pin connector.

Flags: The INTERRUPT flag can be set by the CONVERSION COMPLETE or READY signal from the instrument. Jumpers (W19, W20) are provided which allow the user to select whether the positive or negative transition will set the flag. Interrupt capability is enabled by a second flag, INTERUPT ENABLE, which can be set under program control. Both the INTERRUPT and INTERRUPT ENABLE flags are applied to an M7820 (or equivalent) for computer interrupt. The INTERRUPT flag can be cleared by register-load signals from the M105 (or M1510); both flags are always cleared by computer power-up.

Jumper pair W17-W18 selects one of two interrupt enable signals (INTR ENB A or INTR ENB B). With jumpr W18 in place and W17 removed, INTR ENB B is selected, and the reverse of the jumpers selects INTR ENB A.

Jumper pair W15-W16 selects one of two interrupt signals (INTR A or INTR B). With jumper W16 in place and W15 removed, INTR B is selected, and the reverse of the jumpers selects INTR A.

Register Content Check: To add flexibility to this module, gates are provided to allow the program to check the state of each register output. Each register bit is fed to a bus driver which can be enabled by a signal from the M105 (or M1510).

Register Preset Jumpers: The M1623 also has the option of either setting or clearing the registers during computer power-up. Jumper W11 will cause all register bits to clear on power-up. If W11 is removed, and W12 inserted, all register bits will set on power-up.

Status Gates: Status gates on the M1623 give the programmer the ability to check the states of the INTERRUPT and INTERRUPT ENABLE flags and the status of the external instrument (overflow, remote enable, and latch status, for example). These gates are software enabled through the address selector (M105 or M1510).

Trigger Pulse Generator: For triggering of external equipment, the M1623 contains a one-shot circuit that can be triggered from the device selector (M105 or M1510). The output pulse width is adjustable from 2 to 12 μs by a trimpot on the module. Longer pulses can be obtained by adding a capacitor at the split lugs on the module. The following equation can be used to determine added capacitance:

$$Tpw=0.32(RC)$$

where Tpw is in milliseconds, R is in ohms, and C is in microfarads. (The internal trimpot varies from 5.2K to 50K ohms.) Jumpers (W13, W14) are provided which allow the user to select either a positive or negative output pulse.

SPECIFICATIONS

Output Drive: Outputs to the 40-pin connector are supplied by open-collector high-voltage drivers. Resistors included on the module provide pull-up or current sinking for up to 20 TTL unit loads. If the supplied resistors are removed, the output stages will sink up to 40 mA at logic LOW and will withstand a HIGH level of up to +30 volts. These outputs may therefore be used to drive many types of indicators and even relays. However, if inductive loads are driven, diodes should be wired across each load to swamp inductive kickback.

M1703
OMNIBUS INPUT INTERFACE

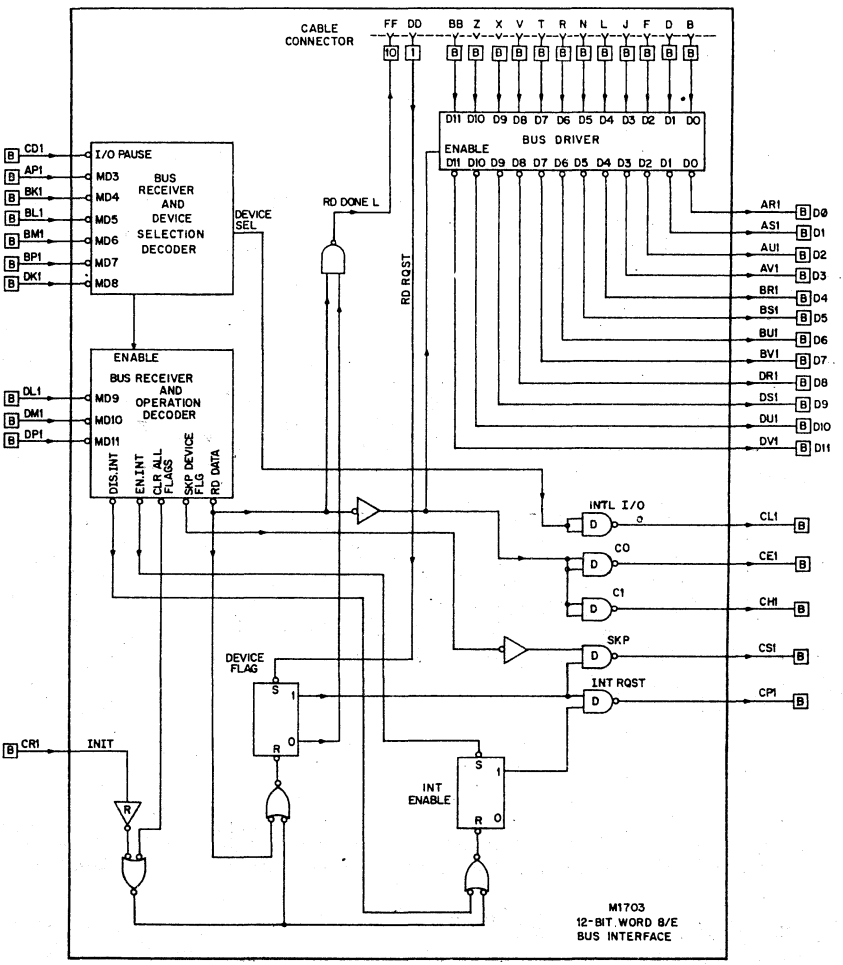
PDP-8/E, 8/M OMNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single

Price:

$75



Volts	Power mA (max.)	Pins
+5	555	AA2, BA2, CA2
GND		AC2, BC1, BC2, CC1, CC2, DC1, DC2
		AN1, AN2, BN1, BN2, CN1, CN2, DN1, DN2
		AT1, AT2, BT1, BT2, CT1, CT2, DT1, DT2
		AF1, AF2, BF1, BF2, CF1, CF2, DF1, DF2

The M1703 provides, on a single quad-height module, a complete, self-contained interface that will input 12 bits of parallel TTL-level data to the PDP-8/e or 8/m OMNIBUS, under interrupt or programmed I/O control. The M1703 plugs directly into the OMNIBUS connector assembly, and the external device plugs into a 40-pin flat cable connector on the module itself. The module includes a device selector, an operation decoder, flags, and all control logic needed to request interrupt and respond to programmed I/O commands on the OMNIBUS. Command codes assigned to this module include:

ENABLE AND DISABLE INTERRUPT
CLEAR FLAGS
SKIP IF DEVICE FLAG SET
READ DATA

A device selection code of 14 (octal) is assigned to this module but the code can be changed by moving wire jumpers.

FUNCTIONS

Device Selection Decoder: The device is addressed through this decoder when I/O PAUSE is asserted and the octal device code for the decoder is received through <MD03:08>. The decoder output asserts the INT. I/O line and enables the operation decoder.

Operation Decoder: The select bits (MD09, 10 and 11) determine the type of operation to be performed when the operation decoder is enabled by the device selection decoder.

DATA <00:11>: Data from the external device is applied to the bus drivers on these lines. A READ DATA command enables the bus drivers and asserts C0 and C1, thereby entering the data into AC0-11 via corresponding OMNIBUS data lines.

READ RQST: When the external device is ready to input stable data, it applies a logic LOW for at least 50 ns on this control line, to set the DEVICE FLAG. READ DONE goes HIGH within 60 ns after READ RSQT goes LOW.

DEVICE FLAG: After being set by a LOW on the RD RQST line, this flag initiates an interrupt request (if INTERRUPT is enabled). This flag is sensed by the SKIP control line.

INTERRUPT RQST: When this line is asserted by the DEVICE FLAG, an interrupt request is sent to the computer which responds by executing a JMS0 instruction.

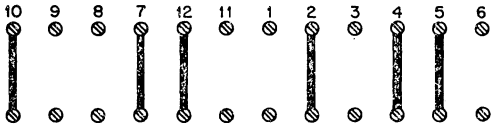
INTERRUPT ENABLE: This flip-flop is set to enable and cleared to disable the interrupt request function.

SKIP Control Line: If the device flag is set, the instruction SKIP ON DEVICE FLAG asserts the SKIP line, incrementing the contents of the computer's program counter.

READ DONE: This line stays HIGH as long as the DEVICE FLAG is set, and signals the end of a data transfer by going LOW after the end of a RD DATA pulse.

Changing the Device Code: The device selection decoder is preset for a device code of 14 octal. However, split lugs on this module permit the code to be changed by the user to any octal number from 00 to 77. To obtain the

desired octal number, jumper the split lug pairs that select the binary equivalent of the device code, as shown below:



A. PHYSICAL LAYOUT OF SPLIT LUGS
(SHOWING JUMPERS FOR DEVICE CODE 14 OCTAL)

ADD JUMPER AT:	DEVICE CODE					
	8^1			8^0		
	2^2	2^1	2^0	2^2	2^1	2^0
BIT = 1	1	3	5	7	9	11
BIT = 0	2	4	6	8	10	12

EXAMPLE

0	0	1	1	0	0	BINARY EQUIV. OF 14 OCTAL
2	4	5	7	10	12	REQUIRED JUMPERS

B. DETERMINING JUMPERS FOR NEW CODE ASSIGNMENTS

IOT INSTRUCTION ASSIGNMENTS

Octal Code	Instruction	Purpose
6140	Disable Interrupt	Clears the INTERRUPT ENABLE flag to disable the INT RQST line
6141	Enable Interrupt	Sets the INTERRUPT ENABLE flag to enable the INT RQST line
6142	Clear Flags	Clears the DEVICE FLAG, asserts READ DONE and clears INTERRUPT ENABLE flag
6143	Skip if Device Flag Set	Asserts the SKIP line if the DEVICE FLAG is set. The computer responds by incrementing the program counter so that the next instruction is skipped.
6144	Read Data	Transfers input data bits <00:11> to <AC00:11> through the OMNIBUS data lines. Also clears the DEVICE FLAG, allowing the RD DONE output to go LOW when the data transfer is complete.

SPECIFICATIONS

Propagation Time:

FROM	TO	ns (max.)
LOW on RD RQST input	RD DONE going HIGH	60

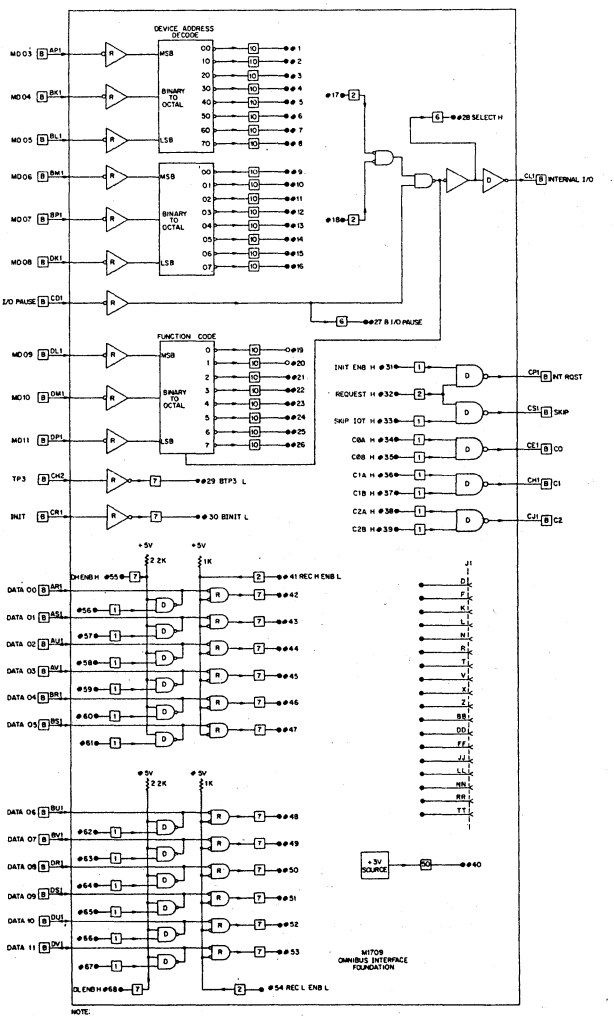
M1709
OMNIBUS INTERFACE FOUNDATION MODULE

PDP-8/e, -8/f, -8/m OMNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single

Price: $125



NOTE:
● REPRESENTS WIRE WRAP PINS

Printed Ckt. Rev.: B
Ckt. Schem. Rev.: A
Printed: August 1972

Board Size:
L—Extended
H—Quad
W—Single

No. Slots: 4

Price: $125.00

Volts	Power mA (max.)	Pins
+5	830	AA2, BA2, CA2
GND		All pins CNFT

DESCRIPTION

The M1709 OMNIBUS Interface Foundation module is a generalized interface card that is constructed to allow the user to build a custom design using integrated circuits (ICs) which can be directly inserted into the OMNIBUS. All required OMNIBUS interface logic, i.e., bus drivers/receivers, device selectors, and interrupt/skip circuitry is provided. IC mounting pads with wire wrappable pins are made available for custom circuitry. Pads accommodate all common types of Dual-In-Line Pack (DIP) ICs with up to forty pins.

Connection to user-equipment is made via standard cables (BC08R or BC04Z) that plug directly into the M1709 module board. The H851 card edge connector, allows several M1709 modules or W966/W967 wire wrappable modules to be strapped together to accommodate more extensive designs.

APPLICATIONS

Since both analog and digital circuitry are available in DIP form, quite complex systems may be built. Some of the typical applications for the M1709 module are:

- Multiword input and/or output
- Instrument interfaces
- Interprocessor communication
- Oscilloscope controller (D/A)
- Peripheral control (data terminals, etc.)
- Interfacing of:

  A/D converters
  Multiplexers
  Counters
  Shift registers
  Read-Only Memories (ROMs)
  Arithmetic Logic Units (ALU)

FUNCTIONS

The preassembled circuitry of the M1709 module can be classified into four categories: Device and Function Selection, Data Bus Interface, Interrupt and Skip Interface, and Control Line Interface.

Device and Function Selection: Device address decoding is performed with a pair of binary-to-octal decoders (3 to 8 line). OMNIBUS lines MD03 through MD08 are decoded and one output of each decoder is ANDed (by wire wrapping) to sense a "device selected" condition. Any code from 01_8 to 77_8 is selectable via wire wrap jumper selection.

The "device selected" condition is, in turn, ANDed with the I/O PAUSE signal to drive the OMNIBUS signal INTERNAL I/O. This signal is also made available at a wire wrap pin as SELECT H.

Function decoding is performed by a binary-to-octal decoder (3 to 8 line). OMNIBUS signals MD09 through MD11 are decoded to form the eight IOT 0 through IOT 7 signals. These TTL signals are made available at numbered wire wrap pins for ease of connection to user-installed IC logic.

Data Bus Interface: The 12 OMNIBUS Data Lines, DATA 00 through DATA 11, are received with special high-impedance circuitry and TTL signals are made available at wire wrap pins. In addition, each data line has a special BUS driver circuit assigned to it. Input to these drivers is available at wire wrap pins and is TTL-compatible for direct connection to user-installed IC logic.

Enabling inputs are provided for both data line receivers and drivers.

Interrupt and Skip Interface: BUS driver circuits are available for driving the OMNIBUS INT RQST and SKIP lines. The INT RQST driver has an enabling input which can be used to inhibit the interrupt request while maintaining the ability to test the interrupt condition via the SKIP facility. Input to these drivers is TTL-compatible and made via wire wrap pins.

Control Line Interface: BUS driver circuits are connected for asserting the three OMNIBUS data transfer mode signal lines—C_0, C_1, C_2. Input to these drivers is TTL-compatible and made via wire wrap pins.

Miscellaneous Interface Signals: OMNIBUS signals TP3 and INITIALIZE are received with high impedance circuits. These signals are made available in TTL-compatible form at wire wrap pins as BTP3 and BINIT, respectively. A source of +3 volts is made available at a wire wrap pin.

OMNIBUS Signals made Available to the User*
In addition to those OMNIBUS signals mentioned previously, the following 40 OMNIBUS signals are made available to the user at wire wrap pins. The complete set of signals available is sufficient to allow the user to accomplish all program transfer **and** data break interface operations.

OMNIBUS Signal Name	Pin
MA0	AD1
MA1	AE1
MA2	AH1
MA3	AJ1
MD0	AK1
MD1	AL1
MD	AM1
MD DIR	AK2
MA4	BD1
MA5	BE1
MA6	BH1
MA7	BJ1
MD6	BM1
MD7	BP1
INT STROBE	BD2
BRK IN PROG	BE2
MA, MS LOAD CONT	BH2
OVERFLOW	BJ2
BREAK DATA CONT	BK2
BREAK CYCLE	BL2
BUS STROBE	CK1

*These OMNIBUS signals (except ± 15 V) require high impedance/low leakage current driving and receiving circuitry. (Use DEC 380 and 8881 ICs.)

OMNIBUS Signal Name	Pin
NOT LAST XFER	CM1
CPMA DISABLE	CU1
MS, IR DISABLE	CV1
TP1	CD2
TP2	CE2
TP3	CH2
TP4	CJ2
TS1	CK2
TS2	CL2
TS3	CM2
TS4	CP2
LINK DATA	CR2
LINK LOAD	CS2
MA8	DD1
MA9	DE1
MA10	DH1
MA11	DJ1
+15 V	DA2
−15 V	DB2

SPECIFICATIONS

Signals to and from the OMNIBUS are received or driven with special high impedance circuitry to minimize bus loading.

CAUTION

All requirements for timing should be in accordance with the PDP-8/e and -8/m Small Computer Handbook.

All signals to and from external equipment or user-installed IC logic must be standard TTL-compatible levels.

M1801
16-BIT RELAY
OUTPUT INTERFACE

UNIBUS/ OMNIBUS

M SERIES

Length: Extended
Height: Quad
Width: Single

Price:

$350

The M1801 is a PDP-11 and PDP-8/e, 8/m interface module containing all the bus receivers, relay drivers, and control logic needed to program 16 isolated single-pole relay contacts. The relay contacts are available at two 40-pin cable connectors mounted on the module.

APPLICATIONS

PDP11 Interfacing: For interfacing to the PDP-11, the M1801 must be used with the M105 Address Selector (or equivalent). The M105 decodes the UNIBUS address lines and causes transfer of information through the M1801 under program control. Interrupt circuitry is also built into the M1801 and can be used in conjunction with the M7820 or equivalent. An example of a typical PDP-11 interface is shown in the M1623 description.

PDP-8/e Interfacing: To interface to the PDP-8/e, the M1801 must be used with the M1510 Bus Device Selector which performs the same functions as the M105 besides having skip capability. Two separate 8-bit words or one 12-bit word can be loaded from the OMNIBUS. For a PDP-8/e interface, it is necessary to remove jumper W33 and insert jumper W34 on the bus INIT input.

Restrictions: The module is electrically, but not mechanically, compatible with the PDP-8/e OMNIBUS. Do not plug the module directly into the OMNIBUS. OMNIBUS signals may be connected to appropriate module pins by backplane wiring. This module is designed for use in bus expansion hardware such as:

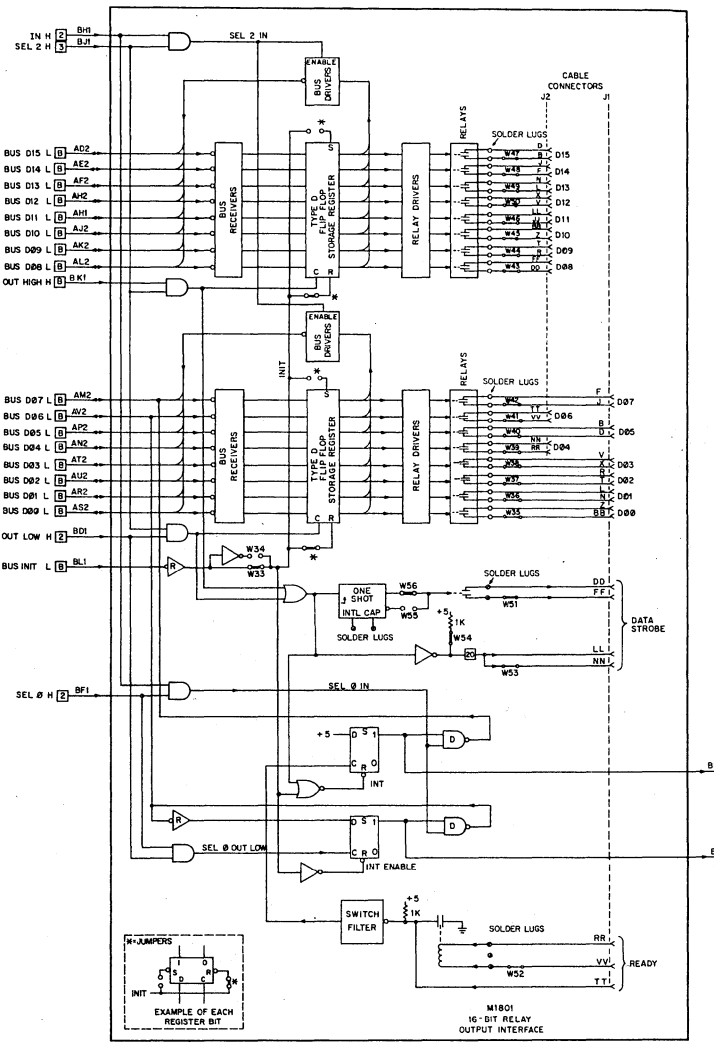
BB11 Blank System Unit (PDP-11 UNIBUS)
H9190 Bus Expander (PDP-8/e OMNIBUS)

FUNCTIONS

Registers: The M1801 contains two 8-bit registers, both interfaced to the computer bus data lines by ungated receivers. Data from the computer is clocked into the registers by strobing signals derived from an M105 or M1510. The user has the option of strobing a single 16-bit word or two 8-bit bytes. A logic HIGH loaded into a register bit activates the corresponding relay output. Each relay output has a jumper and split lugs which allow the user to insert contact filter circuits.

Data Strobe Outputs: Either of the register-loading input pulses will trigger the two DATA STROBE output circuits. One of these outputs is a transistor driver circuit capable of sinking 100 mA (clamped to +5 volts). If jumper W54 is removed, the user can switch up to 20 volts at this output.

The second DATA STROBE circuit contains a one-shot which drives a relay to provide a momentary contact closure. The one-shot has an internal potentiometer for pulse-width adjustment from 5 to 20 ms. External capacitance can be added to split lugs on the module to increase the contact



Volts	Power mA (max.)	Pins
+5	1450	A2
GND		C2, T1

closure time. Jumpers (W56 and W55) are provided which allow the user to choose whether the relay output will be energized on a HIGH or LOW logic level. Both DATA STROBE outputs are available at the 40-pin connector.

READY Relay and Level Inputs: When the interfaced device has received data, it can signal the M1801 that it is ready for another transfer by energizing the READY relay. This relay has a 5-volt coil rating and pulls in at 4.2 volts. A jumper (W52) and split lugs are provided for users who want to add a voltage divider circuit. A second method of ready signaling is to apply a voltage level (less than +12 V) to connector pin TT. Contact filtering (0.6 ms min.) is provided for either READY input to prevent false triggering. The switch filter output sets the INTERRUPT flag, thus requesting more data.

Flags: The INTERRUPT flag can be set by the READY signal from the external equipment. The positive transition will set the flag. Interrupt capability is enabled by a second flag, INTERRUPT ENABLE, which can be set under program control. Both the INTERRUPT and INTERRUPT ENABLE flags are applied to an M7820 (or equivalent) for computer interrupt. The INTERRUPT flag is cleared by the register-loading signals from the M105 (or M1510); both flags are always cleared by computer power-ups.

Register Content Check: To add flexibility to this module, gates are provided to allow the program to check the state of each register output. Each register bit is fed to a bus driver which can be enabled by a signal from the M105 (or M1510).

Register Preset Jumpers: Each register bit on the M1801 has a jumper which causes that particular bit to clear on power-on. If the user wishes to set a particular bit, he must remove the jumper provided and install the particular jumper which sets that bit. Care should be taken to insure that both the set and clear jumpers are not inserted simultaneously.

DATA Bit	Jumper to CLEAR	Jumper to SET
D00	W1	W2
D01	W3	W4
D02	W5	W6
D03	W7	W8
D04	W9	W10
D05	W11	W12
D06	W13	W14
D07	W15	W16
D08	W17	W18
D09	W19	W20
D10	W21	W22
D11	W23	W24
D12	W31	W32
D13	W29	W30
D14	W27	W28
D15	W25	W26

Status Gates: Status gates on the M1801 give the programmer the ability to check the states of the INTERRUPT and INTERRUPT ENABLE flags. These gates are software-enabled through the address selector (M105 or M1510).

CAUTION
When the high output voltage or current capabilities of the M1801 are used, the M1801 should be shielded from all computer circuitry.

SPECIFICATIONS
Relay Contact Ratings:

Voltage:	100 V max.
Current:	0.5 A max.
Power:	10 W max. resistive load
Insulation resistance:	1,000 megohms

Data Strobe Output:

Current Sinking:	100 mA max.
Voltage:	20 V max.

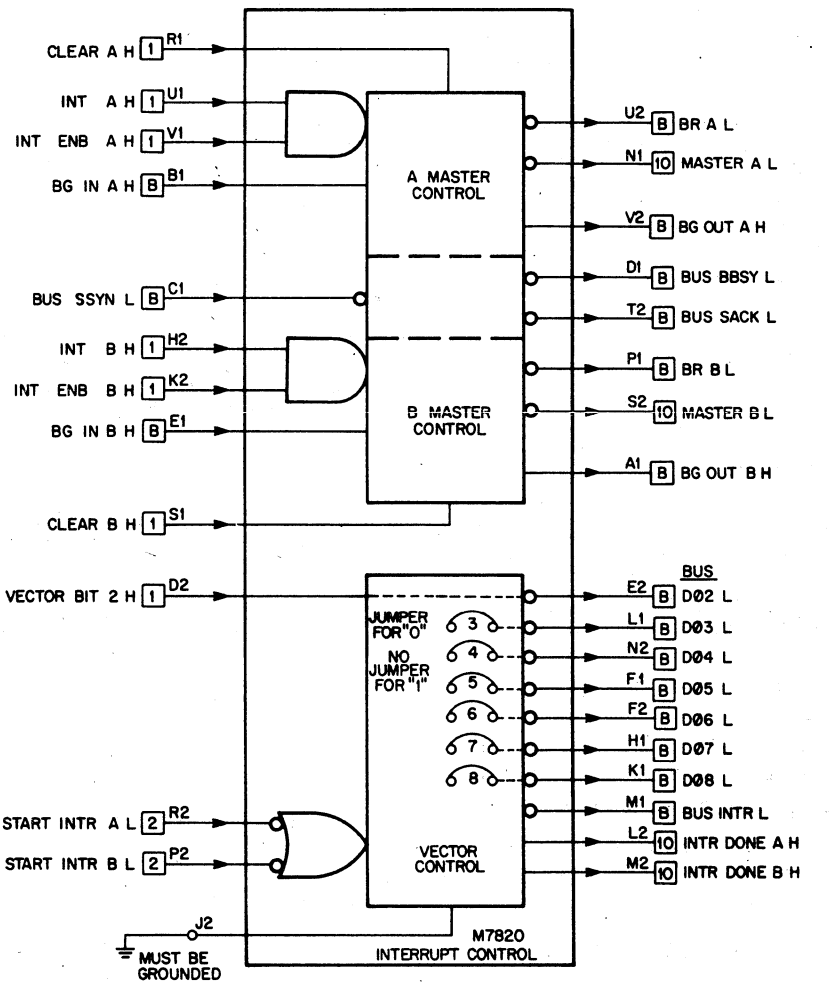
M7820
INTERRUPT CONTROL

PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single

Price: $100



Volts	Power mA (max.)	Pins
+5	290	A2
GND		C2, T1

The M7820 is used in PDP-11 device interfaces. It consists of logic circuits that can be divided into three functional sections: Master Control A, Master Control B, and INTR Control.

The Master Control circuits are used to gain control of the UNIBUS for satisfying the need to either gain direct memory access (DMA), or to perform the INTR bus operation which alters program flow.

To become master of the bus involves a question of priority. Briefly, this priority question is split into three phases: 1) bus request lines, 2) processor's priority level, and 3) physical placement of a device on the UNIBUS.

1) NPR (highest)
   BR7
   BR6 (except for trap instructions)
   BR5
   BR4 (lowest)

2) The processor acknowledges BR's of level > N: where N is an Octal number in processor's status register. (NPR's are not affected.)

3) Highest priority goes to the device closest to the processor on the unique bus grant chain.

Theory Of Operation

If a device wants control of the bus, it asserts both INT A and INT ENB A. Then a request is made on a BR. This then leads to priority determination and a BG results. Now the Master Control A responds with BUS SACK. The processor sees this acknowledgement and removes BG. When BUS BBSY and BUS SSYN are negated, the Master Control A removes its BR and asserts BUS BBSY itself. It also asserts Master A when it is in control of the bus. Now the device can use the bus. To release control of bus, the device can assert CLEAR A or negate: INT A or INT ENB A. Master Control B is identical to A.

The INTR operation transfers a "vector address" to the processor. At this address is stored two consecutive words: 1) The starting address of the interrupt service routine, and 2) A status word. When the processor detects this, a trap sequence is initiated (current value of PC and current status of PS are stored and new ones are fetched). Now the interrupt service routine is executed.

To start the process: START INTR A or START INTR B is asserted. Then BUS INTR is asserted along with a 7-bit address. This is transferred onto the data lines: BUS D <08:02> providing a range of 000 to 374 (OCTAL) in increments of 4. D <08:03>are controlled by jumpers, which when "in," force the bit to zero. The processor seeing BUS INTR asserts BUS SSYN. When this is detected, an INTR DONE A is asserted which negates the START INTR signal. This in turn negates BUS INTR, which negates BUS SSYN. As a result, a trap sequence is initiated. Vector bit 2 controls D02. When it is asserted D02 is asserted. It does not control any other bits.

The grant chain to tie in the Master Control is as follows:

BG IN has 390Ω to GND and BG has 180Ω
+5 Volts.

EXT GND is used for testing purposes and should be tied to ground in normal operations.

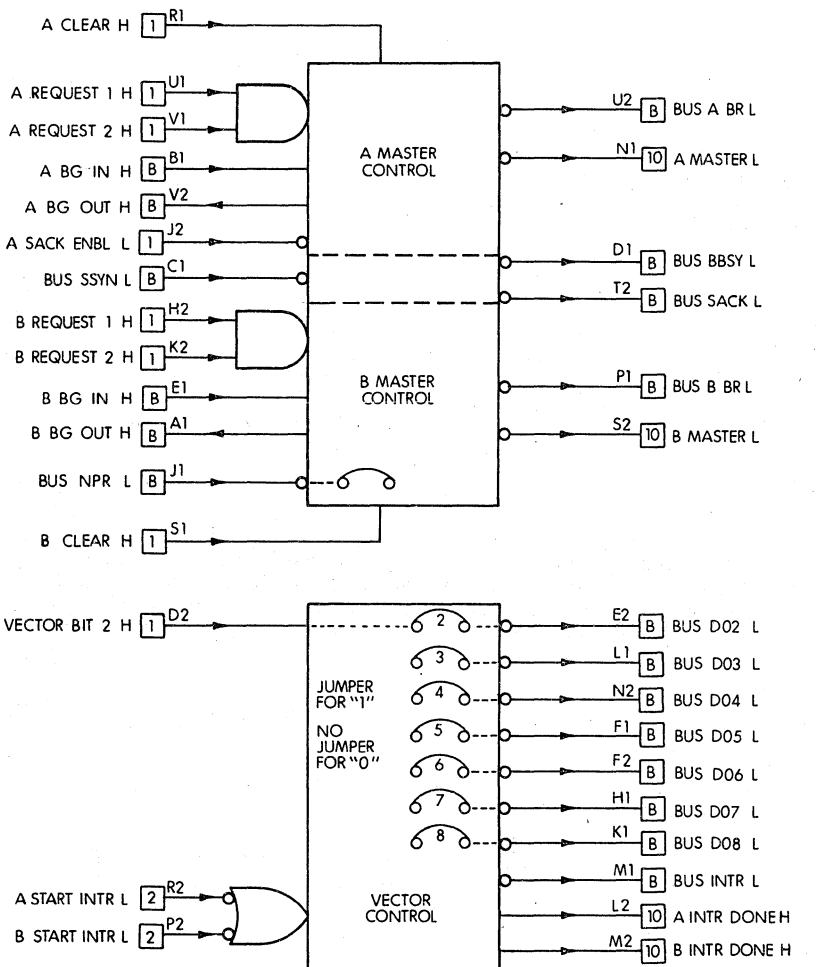
M7821
INTERRUPT CONTROL MODULE

PDP-11 UNIBUS

M SERIES

Length: Extended
Height: Single
Width: Single

Price: $100



Volts	Power mA (max.)	Pins
+5	550	A2
GND		C2, T1

The M7821 Interrupt Control Module is a replacement for the M7820 that improves PDP-11 system performance. In almost all cases, it may be used directly in place of the M7820, without making any changes to hardware or software. A block diagram of the module is shown in the figure.

NOTE

The following description assumes the reader understands the function and operation of an M7820.

The M7821 does **not** have two identical Master Control halves. For devices which use one half of the module to become master with an NPR and one half for a BR, the A half (Request Bus pins U1 and V1) must be used for NPR and the B half (Request Bus pins H2 and K2) must be used for BR.

The NPR half of the module has the ability to prevent the un-assertion of BUS SACK for devices that do more than one data cycle each time they request the bus. This is done by holding pin J2 high until the beginning of the last bus cycle. SACK will be unasserted as soon as pin J2 goes low, and the input on J2 can, therefore, be a pulse or a level. Pin J2 is active only when the Master signal is asserted (pin N1 is low), and, therefore, pin J2 may be permanently grounded if only one bus cycle is done for each request.

NOTE

The M7820 requires pin J2 to be grounded for the interrupt section of the module to work, so the M7821 is compatible when used as a replacement.

The BR half of the module does not have the ability to hold BUS SACK asserted and always drop SACK when BUS BBSY is asserted. However, this section of the module does have some special circuitry that looks at the BUS NPR line which must be wired to pin J1 on the M7281. This circuitry, if it sees the assertion of the bus grant line to which the module is wired while BUS NPR is asserted, will block the grant and return SACK. When BBSY becomes unasserted from the last bus master, the M7821 will then clear SACK off the bus. The processor will then be able to service the NPR, improving the latency time for NPR devices.

CAUTION

Only some PDP-11 processors will work with the special circuitry described above. There is a jumper on the M7821 module which, when cut, prevents the special circuitry from working.

NOTE

Pin J1 is unused on the M7820 module, and if BUS NPR is not wired to this pin, the special jumper noted above must be cut.

If both halves of the M7821 are used for BR requests, pin J2 must be grounded and the jumper may be cut as required. If both halves are used for NPR requests, pin J2 may be used as required, and the jumper must be cut. Please note that if the normally BR half (Request Bus pins H2 and K2) are used for NPR's, only one bus cycle may be done per request.

The interrupt section of the module has been changed slightly also. **The jumpers on the M7821 module must be left in to generate a "one" in that bit position of the vector, and cut out to generate a "zero."** This is the reverse of the M7820. A jumper has also been added to vector bit 2. If the module is to be used the same way as a M7820, the jumper for bit 2 must be left in. However, if only one vector is being generated by the module, pin D2 should be permanently wired to a high level, and then the jumpers can be used to assign vectors to every vector location (4 bytes) without changing backpanel wiring. Note that the jumper for bit 2 must also be in for a one and cut for a zero.

SUMMARY OF COMPATIBILITY CONSIDERATIONS:
On the M7820, pin J2 must be grounded for the interrupt section to work. If pin J2 is grounded, then an M7821 module can be directly plugged in if the special jumper is cut, the vector bit 2 jumper is left in, and the rest of the jumpers are cut appropriately.

POWER: +5 Volts at 725 mA (max)
The grant chain to tie in the Master Control as follows: BG IN has 390Ω to GND and BG OUT has Ω180 to +5 Volts

SIZE: Extended length, single height, single width FLIP CHIP module.

rtm modules

REGISTER TRANSFER MODULES

The impact of advancing digital design technology is highlighted by the Register Transfer (RT™) Series of modules listed in this section.

Register Transfer defines the next higher level of computing machine design above sequential and combinatorial logic operations. Digital system design is removed from the realm of the pure logic designer and is made easily achievable by persons such as students, laboratory technicians, researchers, etc.

A standard flowchart, which includes register designations, provides full information for constructing the system. The need for extensive documentation is dramatically reduced and system trouble-shooting is considerably simplified.

RT modules can be operated in 8-bit or 16-bit register configurations; registers may be linked to form words of 24, 32, or higher numbers of bits.

Existing functions can be expanded simply by adding steps to the flowchart, installing new modules, and making the extra wiring connections.

The modules are especially useful at the university teaching level, in experimental, medical, and research laboratories, industrial control, materials handling and manufacturing.

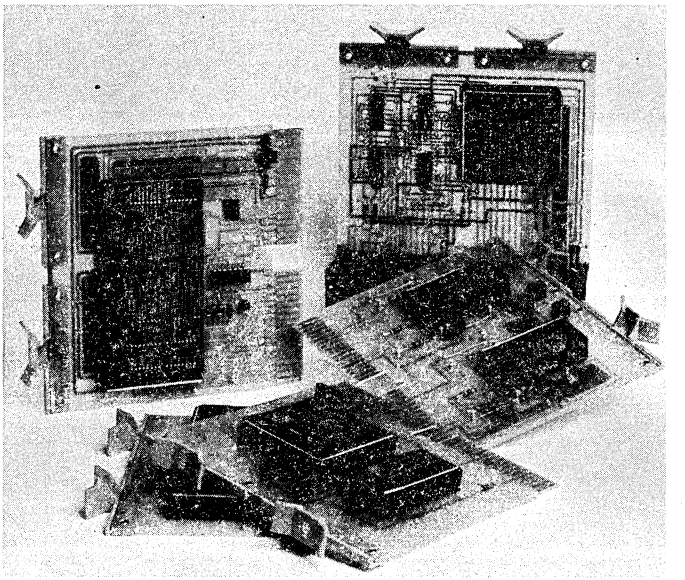
The concept of RT modules is not new; however, this implementation is aimed at providing a powerful and low-cost design tool to digital system engineers. To design a system with these modules, the user need only be familiar with the concept of registers and register operations, and possess a fundamental understanding of the flowchart.

REGISTER TRANSFER MODULES

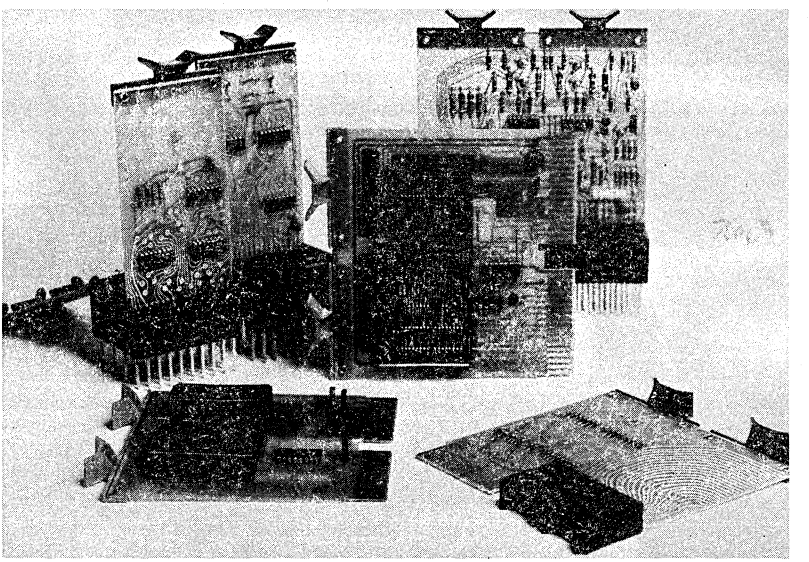
RTM

Module #	Title	Price
M962	Bus Terminator	$30.00
M7300	GPA Control	$165.00
M7301	GPA Register	$135.00
M7304	K Bus Sense	$115.00
M7305	TR Transfer Register	$100.00
M7306	Flag Module	$40.00
M7307	RT-10M-Constants Generator	$100.00
M7310	RT K Evoke	$40.00
M7311	RT D GPI	$100.00
M7312	RT K-Two-Way Branch	$40.00
M7313	Serial Interface DC-16-A	$325.00
M7314	RT W Eight Way Branch	$40.00
M7315	RT K Subroutine Return	$50.00
M7316	RT T Output Interface	$75.00
M7317	RT T Input Interface	$50.00
M7318	RT M Scratch Pad	$200.00
M7319	16 X 256 Scratch Pad Memory	$350.00
M7320	Byte Register	$115.00
M7323	Contact Interrogation Unit	$80.00
M7327	PCS 16 Instruction Memory	$225.00
M7328	PCS 16 Evoke Decoder	$50.00
M7329	PCS 16 Mux.	$50.00
M7332	BC Bus Control	$150.00
M7333	DC 16A Adapter	$25.00
M7334	Light & Switch Interface	$250.00
M7336	PCS 16-E	$150.00

a series
analog modules



The A Series analog module line has been substantially expanded. Shown here are a few of the new units.



The A Series additions are DTL and TTL compatible and compatible with DEC K and M Series modules, computers, control systems and standard instrumentation.

NOTES ON OPERATIONAL AMPLIFIERS

I. INTRODUCTION

This article describes some of the basic characteristics and uses of operational amplifiers. It is written especially for people with a digital background, but with a limited exposure to analog technology. The equations presented are not exact, but are good engineering approximations, which are accurate enough for most applications. It is hoped that this simplified discussion will provide more insight into the uses and limitations of operational amplifiers than a more rigorous approach.

The operational amplifier is a basic building block in analog work, much the same way as a NAND gate can be a basic building block in a digital computer. An operational amplifier (op amp) together with other components such as resistors and capacitors, can be used to perform addition, subtraction, integration, and many other functions. Op amps can be used to make oscillators, active filters, and even digital circuits such as Schmitt triggers, gates, and flip-flops. When used with A/D and D/A converters in data processing work, op amps perform such functions as scale changing, offsetting, and isolation between source and load.

II. GENERAL CHARACTERISTICS

An operational amplifier can be considered a 3 terminal device, plus a common or ground return, see Fig. 1. Chopper-stabilized op amps, which will not be considered here, have the Plus Input permanently tied to ground. The op amp is really a difference amplifier, in that it amplifies only the difference between the two inputs, and tries to reject any DC or AC signal that is common to both inputs.

Op amps are characterized by high DC gain, high input impedance, low output impedance, and a gain that decreases with increasing frequency. Op amps used without feedback would be operating open loop, a rare situation; but with feedback the operation would be closed loop. The use of properly applied negative feedback stabilizes the operation of the composite circuit against changes in the amplifier, and provides its versatility and usefullness.

When an op amp is working in the linear region, two approximations can be made to help in the analysis of the circuit configuration. First, the voltages of the two inputs are the same; and second, no current flows into or out of the input terminals. Fig. 2 shows a simple inverting amplifier. Assume the Minus Input is 0 volts, the same as the Plus Input, and that no current flows into the Minus Input, called the summing junction. Then $i_I = i_F$, and some simple manipulations show that the gain is equal to $-R_F/R_I$. Similar reasoning applied to the non-inverting amplifier of Fig. 3 shows that the gain is equal to $+\frac{R_I + R_2}{}$. An easy way to remember this is to think of the two resistors as forming a tapped divider network.

III. SPECIFICATIONS

Specifications are usually given for open loop performance, so that the user has to interpret and calculate how this will affect his particular closed loop circuit. The following section will give some brief descriptions of what some of the specifications mean.

Settling time. This is the time it takes the output to get within and stay within a certain amount of is final value, after the input has received a step input, see Fig. 4. This parameter is important when an amplifier is used in front of an A/D converter, since the A/D should not begin its conversion until the amplifier has settled.

Overload recovery. It takes an overload recovery time for the output to first assume its proper value after an overdriving input signal has been removed. However, the output still has not settled, and this extra time must be waited before the output is valid.

Slew rate. This term is comparable to rise or fall time in a digital circuit. It is a measure of how fast the output can change. If an amplifier output could go from 0 volts to 10 volts in 2 μsec, it would have a slew rate of 5 volts/μsec.

Frequency for full output. This is the maximum frequency at which a full scale sine wave (such as +10 to −10 volts) can be assured at the output, without noticeable distortion. In many ways this is real frequency limitation of an op amp, since up to this frequency there are no other restrictions on the amplitude of the input signal.

Frequency for unity gain. The open loop gain of an amplifier is equal to one at this frequency. But the input signal must be restricted in amplitude such that the maximum rate of change of output (slew rate) is not exceeded. Usually only millivolt signals may be processed at this frequency, therefore the full amplifier bandwidth is not usable for normal data processing systems.

Impedance. The input impedance is simply the resistance between the two inputs. The common mode impedance is the highest resistance attainable with feedback.

Common mode rejection. This is a measure of how well an amplifier will not respond to a signal common to both inputs. If used as a voltage follower, an op amp with a common mode rejection ratio (CMRR) of 10,000 could have error of 1 mv if the input were 10 v. (10/10,000 volts).

Voltage offset. The inability to achieve perfect balance in the input circuit causes the output to respond to an apparent signal when the inputs are tied to ground. For an inverting amplifier, the output error due to the input voltage offset is equal to the offset times the closed loop gain plus one. With an input offset of 3 mv, and a gain of 1, the output error would be 6 mv. Fortunately, initial voltage offset can be trimmed with a potentiometer at the right place in the circuit.

Current offset. Current offset (or bias current) multiplied by the feedback resistor (Fig. 2) produces an output error. This effect can be minimized by using the differential offset (the difference in offset currents for the two inputs) when the resistance seen from both inputs to ground are equal. For Fig. 2, the Plus Input should than be returned to ground through a resistor equal to the parallel combination of R_I and R_F.

Output ratings. The output voltage and current ratings imply a minimum value for the load resistor. 10 volts and 5 ma would correspond to a load resistor of 2 K. In an inverting amplifier, the feedback resistor is a load for the output, and the current through this resistor must be subtracted from

the amount of current still available at the output. All really useful operational amplifiers can be shorted to ground without damage, but shorting to a voltage will usually destroy some of the circuitry.

IV. APPLICATIONS

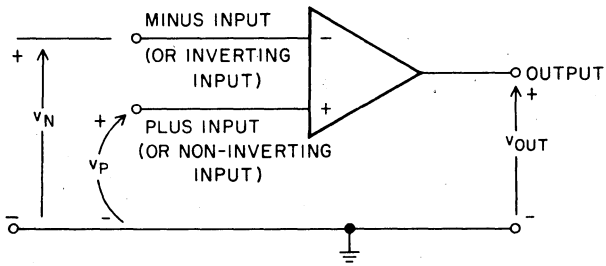
Some common configurations for operational amplifiers are shown in Figs. 5 through 10. The pin letter assignments correspond to the op amps sold by Digital Equipment Corp. If these op amps are used, the jumper between Pin S and the Minus input should be removed.

The voltage follower, Fig. 5, features high input impedance, but will have an error depending on the CMRR. Large voltages cannot be handled, since common mode voltage ratings should not be exceeded. The inverter configuration, Fig. 7, is very versatile and does not have a common mode voltage problem, since both inputs are near ground. Large input voltages can be handled if the input resistor is made appropriately large. One disadvantage of the inverting configuration is that the input impedance is relatively low, essentially equal to the input resistor. When a gain trim potentiometer is used, the gain accuracy by itself becomes irrelevant. What is important is gain resolution (mostly determined by the potentiometer), and the gain stability (mostly determined by the temperature coefficients of the input and feedback resistors). The ratio of the closed loop gain to the open loop gain gives the suitability of an amplifier as far as static accuracy is concerned. With a closed loop gain of 5, and an open loop gain of 10,000, an amplifier could be used in a system with an allowable error of 1 part in 2,000.

The possibility of oscillation must always be considered when feedback amplifiers are used. Usually the more feedback used, the greater is the tendency to oscillate. Oscillations can always be attributed to phase shift. Therefore, stabilization of operational amplifiers involves phase shifting to oppose oscillation. In Fig. 7, the feedback capacitor allows high frequency signals to be fed back to the inverting input (degenerative feedback) with a phase lead. In the inverting configuration, the output will be 180° out of phase with the input at low frequencies, and the feedback signal will oppose the input signal. At high frequencies, the e are additional phase lags in the amplifier and feedback circuitry. If the feedback signal has a total phase shift (lag) of 360° with a gain through the amplifier and feedback network of greater than 1, the amplifier will oscillate, since the input and output are in phase.

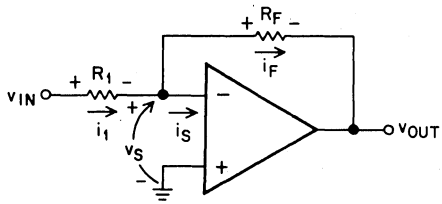
V. REFERENCES

1. "An Operational Amplifier Application Manual"
   Analog Devices, Inc., Cambridge, Mass.
2. "Handbook of Operational Amplifier Applications"
   Burr-Brown Research Corp., Tucson, Arizona
3. "Linear Integrated Circuits Applications Handbook"
   Fairchild Semiconductor, Mountain View, California
4. "Applications Manual for Operational Amplifiers"
   Philbrick/Nexus Research, Dedham, Mass.



$v_{OUT} = A(v_P - v_N)$, WHERE A IS THE AMPLIFIER GAIN

Fig. 1, Basic Operational Amplifier Symbol



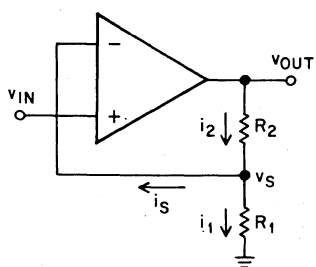
ASSUME: $v_S = 0$ THEN $i_1 = i_F$

$i_S = 0$

$$\frac{v_{IN}}{R_1} = -\frac{v_{OUT}}{R_F}$$

$$\frac{v_{OUT}}{v_{IN}} = -\frac{R_F}{R_1}$$

Fig. 2, Inverting Amplifier



ASSUME: $v_S = v_{IN}$

$i_S = 0$

THEN $i_1 = i_2$

$$\frac{v_S}{R_1} = \frac{v_{OUT} - v_S}{R_2}$$

$$\frac{v_{IN}}{R_1} = \frac{v_{OUT} - v_{IN}}{R_2}$$

$$v_{IN} R_2 = v_{OUT} R_1 - v_{IN} R_1$$

$$\frac{v_{OUT}}{v_{IN}} = +\frac{R_2 + R_1}{R_1}$$

Fig. 3, Non-Inverting Amplifier

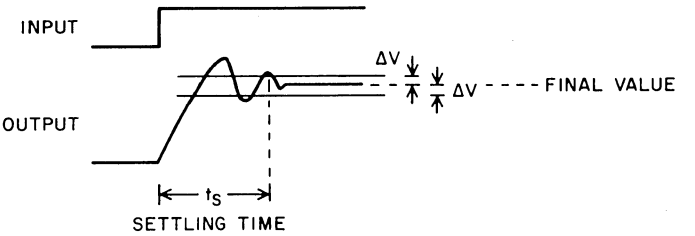


Fig. 4, Settling Time

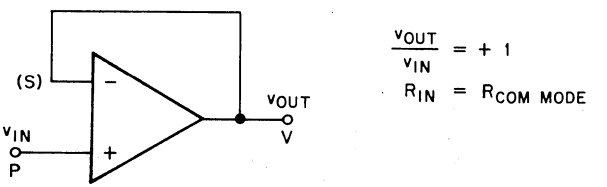


Fig. 5, Voltage Follower

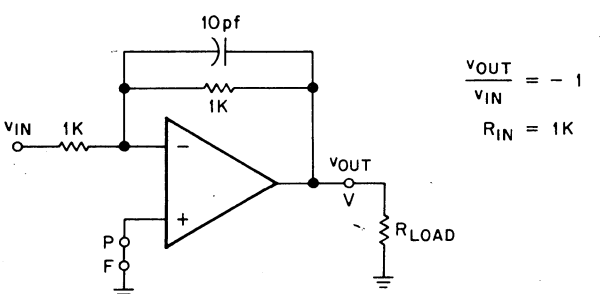
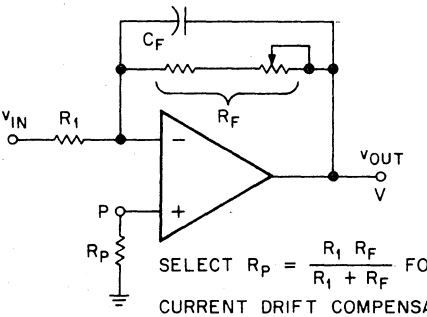


Fig. 6, Inverter



$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_1}$$

$R_{IN} = R_1$

GAIN STABILITY DEPENDS ON THE INPUT AND FEEDBACK RESISTOR, AND GAIN TRIM POTENTIOMETER.

SELECT $R_P = \frac{R_1 R_F}{R_1 + R_F}$ FOR CURRENT DRIFT COMPENSATION.

TYP VALUES

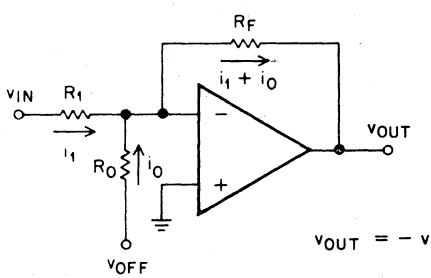
R_1 1K TO 10K

R_F 1K TO 100K

R_P 500Ω TO 5K

THE USE OF C_F REDUCES THE TENDENCY OF THE OP AMP TO OSCILLATE

Fig. 7, Adjustable Gain and Current Compensation



$$V_{OUT} = -V_{IN}\left(\frac{R_F}{R_1}\right) + \underbrace{\left[-V_{OFF}\left(\frac{R_F}{R_O}\right)\right]}_{\text{OFFSET}}$$

Fig. 8, Offsetting

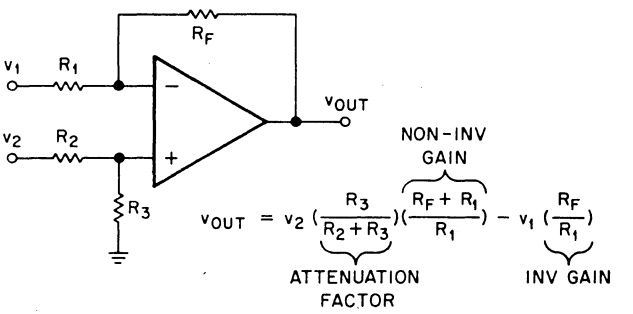


Fig. 9, Differential Gain

2^n and Resolution

2^n	# OF BITS n	RESOLUTION (%)	PPM
1	0	100.0	1,000,000
2	1	50.0	500,00
4	2	25.0	250,000
8	3	12.5	125,000
16	4	6.25	62,500
32	5	3.125	31,250
64	6	1.563	15,625
128	7	0.781	7,812
256	8	0.391	3,906
512	9	0.195	1,953
1 024	10	0.0977	977
2 048	11	0.0488	488
4 096	12	0.0244	244
8 192	13	0.0122	122
16 384	14	0.00610	61
32 768	15	0.00305	31
65 536	16	0.00153	15
131 072	17	0.000763	8

OFFSET BINARY (BIPOLAR)

+ FULL SCALE −1 LSB	111111111111
+ 3/4 FULL SCALE	111000000000
+ 1/2 FULL SCALE	110000000000
ZERO	100000000000
− 1/2 FULL SCALE	010000000000
− 3/4 FULL SCALE	001000000000
− FULL SCALE +1 LSB	000000000001
− FULL SCALE	000000000000

STRAIGHT BINARY (UNIPOLAR)

+ FULL SCALE −1 LSB	111111111111
+ 3/4 FULL SCALE	110000000000
+ 1/2 FULL SCALE	100000000000
ZERO +1 LSB	000000000001
ZERO	000000000000

TWO'S COMPLEMENT (BIPOLAR)

+ FULL SCALE −1 LSB	011111111111
+ 3/4 FULL SCALE	011000000000
+ 1/2 FULL SCALE	010000000000
ZERO	000000000000
− 1/2 FULL SCALE	110000000000
− 3/4 FULL SCALE	101000000000
− FULL SCALE +1 LSB	100000000001
− FULL SCALE	100000000000

BINARY CODED DECIMAL (UNIPOLAR)

+ FULL SCALE −1 LSD	1001 1001 1001
+ 3/4 FULL SCALE	0111 0101 0000
+ 1/2 FULL SCALE	0101 0000 0000
ZERO + LSD	0000 0000 0001
ZERO	0000 0000 0000

A123
FOUR-INPUT MULTIPLEXER

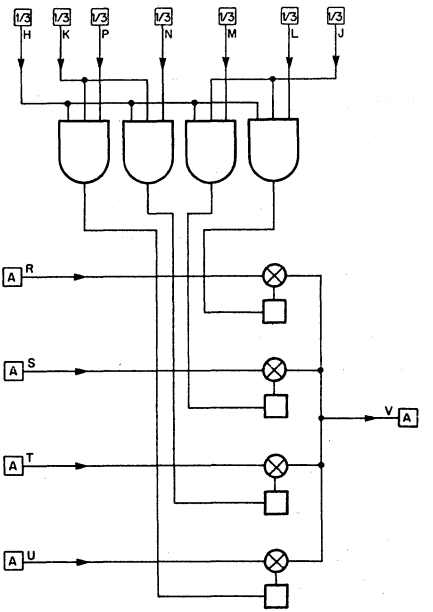
MULTI-PLEXERS

A SERIES

Length: Standard
Height: Single
Width: Single

Price:

$58



A =ANALOG SIGNALS
(DO NOT CONNECT TO LOGIC LEVELS)

Volts	Power mA (max.)	Pins
+10	18	D2
+5	45	A2
GND		C2, T1
−20	50	E2

The A123 Multiplexer provides 4 gated analog switches that are controlled by logic levels of 0V and +3V. The module is equivalent to a single-pole, 4-position switch, since one output terminal of each MOS FET switch is tied together. If all three digital inputs of a circuit are at +3V (or not connected) the two output terminals are connected together. If any digital input is at 0V, the switch terminals are disconnected. Two switches should not be on at the same time. The analog switch can handle signals between +10V and −10v, with currents up to 1 mA.

The positive power supply must be between +5V and +15V, and at least equal to or greater than the most positive excursion of the analog signal. The negative power supply must be between −5 and −20v, and at least 10 Volts more negative than the most negative excursion of the analog signal. The voltage difference between the two supplies must not be more than 30V.

SPECIFICATIONS

Digital Inputs	
Logic ONE:	+2.4v to +5.0V
Logic ZERO:	0.0v to +0.8V
Input loading:	0.5mA at 0Volts
Analog Signal	
Voltage range:	+10v to −10v
Current (max.):	1 mA
Output Switch	
On resistance, max.:	1000 ohms
On offset:	0 Volts
Off leakage, capacitance:	10 nA, 10 pF
Turn on delay, max.:	0.2 μsec
Turn off delay, max.:	0.5 μsec

A160
HIGH IMPEDANCE MULTIPLEXER EXPANDER

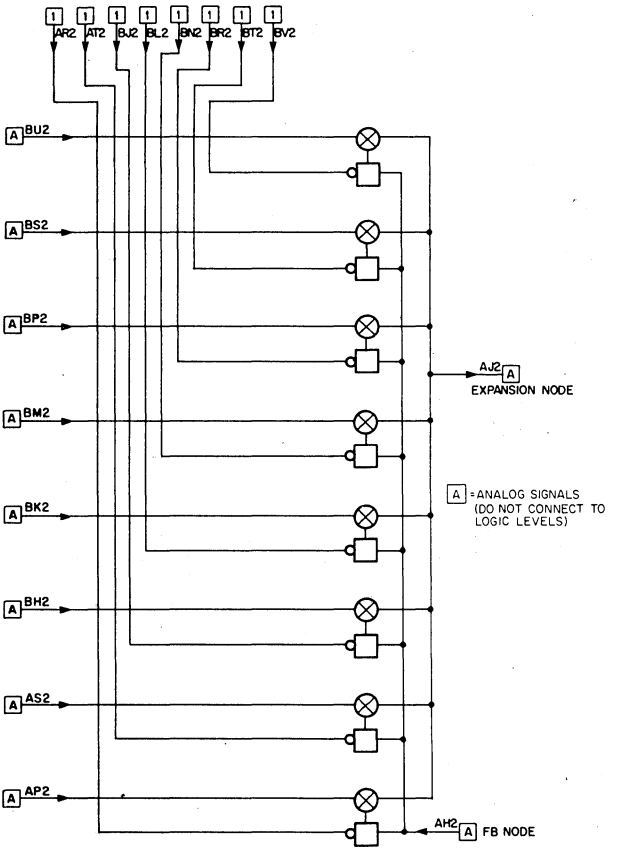
MULTI-PLEXERS

A SERIES

Length: Standard
Height: Double
Width: Double

Price:

$150.



Volts	Power mA (max.)	Pins
+15	25	AD1, AD2
GND	ANALOG	AF1, AF2
−15	25	AE1, AE2

The A160 is a high impedance multiplexer expander consisting of 8 independent FET channels.

This unit may be used with any of the DEC high impedance multiplexers to perform single or double level multiplexing. It also may be used to expand the channel capabilities of the A162, A163, and A164, Multiplexer.

The A160 is DTL and TTL compatible and may be used with DEC's standard K and M Series logic modules. Each channel has its own channel selector driver and may be controlled from an external source such as a shift register, clock, or gating function.

Advanced shielding techniques and optimized circuit layout have been employed in the A160, ensuring stable operation under normal ambient electrostatic and electromagnetic conditions, as well as allowing minimal cross-talk between channels.

SPECIFICATIONS

Analog Inputs:	8 single ended
Input Voltage Range:	±10V. Maximum full scale
Expander Node:	Common point of 8 channels brought out to a common pin for input to external buffer amplifier
Feedback Input:	Feedback control point of multiplexer switches connected to output of buffer amplifier
Input Leakage:	0.5 nano Ampere max., per channel
Input Feedthrough Capacity:	4 pF per channel
OFF Channel Capacity:	7 pF per channel, shunt capacity at common node
ON Resistance of Channel (Without Buffer):	1000 ohms
Max. Input Voltage	±15V.
Switching plus Settling Time:	5 μsec., max., to settle to within .01% of full value for full scale excursion with zero source impedance
Output Range:	Same as input (±10 VFS)
Transfer Accuracy:	±0.01% of full scale at 25° C.
Selector Input (Direct into Multiplexer):	One TTL Load
ON Level	Logic Zero (0 Volts)
OFF Level	Logic One (+3 Volts)

A161
HIGH IMPEDANCE MULTIPLEXER WITH OUTPUT BUFFER

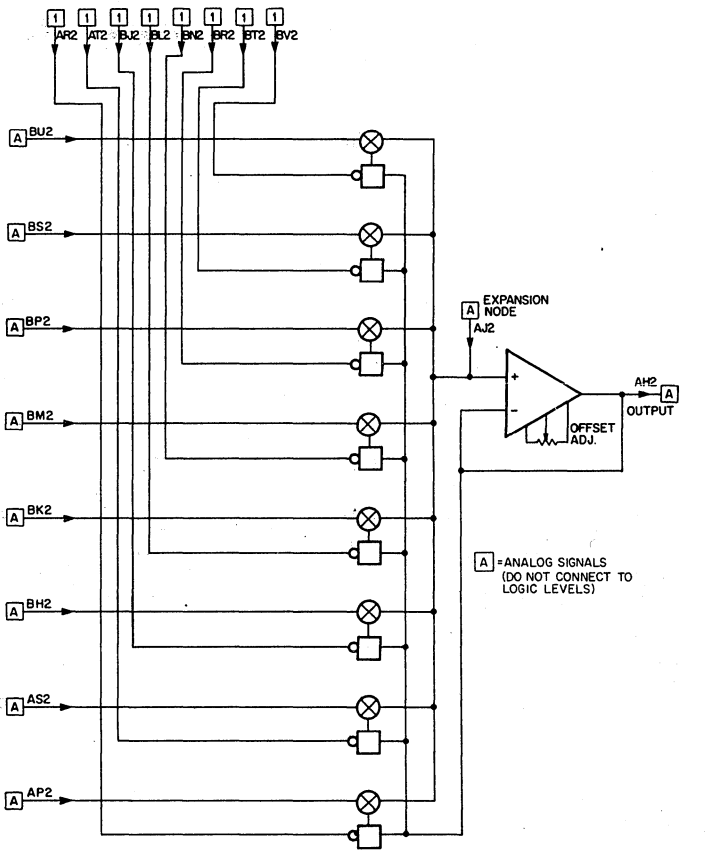
MULTI-PLEXERS

A SERIES

Length: Standard
Height: Double
Width: Double

Price:

$200.



Volts	Power mA (max.)	Pins
+15	35	AD1, AD2
GND	LOGIC	AC1, AC2, BC1, BC2
GND	ANALOG	AF1, AF2
−15	35	AE1, AE2

The A161 is a high impedance multiplexer consisting of 8 independent FET switched channels and a noninverting unity gain follower amplifier, designed for application where accuracy, high speed, and high input independance are prime requirements.

This unit is DTL and TTL compatible and may be used with DEC K and M Series logic modules. It will also provide excellent performance with systems employing sample and holds, high speed multiplexing, A/D converters, as well as single and double level multiplexing.

Provided on the A161 are eight channel select lines, which may be controlled from an external source such as a shift register, clock, or gating function.

The A161 has been engineered and factory adjusted to provide rated performance. It also employs advanced shielding techniques and optimized circuit layout, ensuring stable operation under normal ambient electrostatic and electromagnetic conditions, as well as allowing minimal crosstalk between channels.

The A161 has the capability of output channel expansion simply by typing in the A160 or A162 Multiplexer Expanders.

SPECIFICATIONS

Analog inputs:	8 single ended
Input voltage range:	±10 V. Maximum full scale
Expander node:	Common point of 8 channels brought out to pin as well as to input of buffer amplifier.
Input leakage:	0.5 nano Ampere, max., per channel
Input feedthrough capacity:	4 pF per channel
OFF channel capacity:	7 pF per channel, shunt capacity at common node
Series ON resistance of channel:	1000 ohms
Shunt ON Resistance to ground:	10^8 ohms min.
Switching plus settling time:	5 μsec., max., to settle to within .01% of final value for full scale excursion with zero source impedance
Fault protection:	Current limiting to 10 mA. provided
Max. Input Voltage (Without Damage):	±15 V.
Output Range:	Same as input (±10 VFS)
Output Current:	±20 mA., maximum
Output Protection:	Short circuit protection, indefinitely to ground

Amplifier Offset:	Adjustable to zero
Transfer Accuracy:	±0.01% of full scale at 25° C.
Temp. Coefficient:	30 μV/° C.
Selection Inputs (Direct into Multiplexer):	One TTL Load
ON Level:	Logic Zero
OFF Level:	Logic One

A162
HIGH IMPEDANCE MULTIPLEXER WITH DECODER

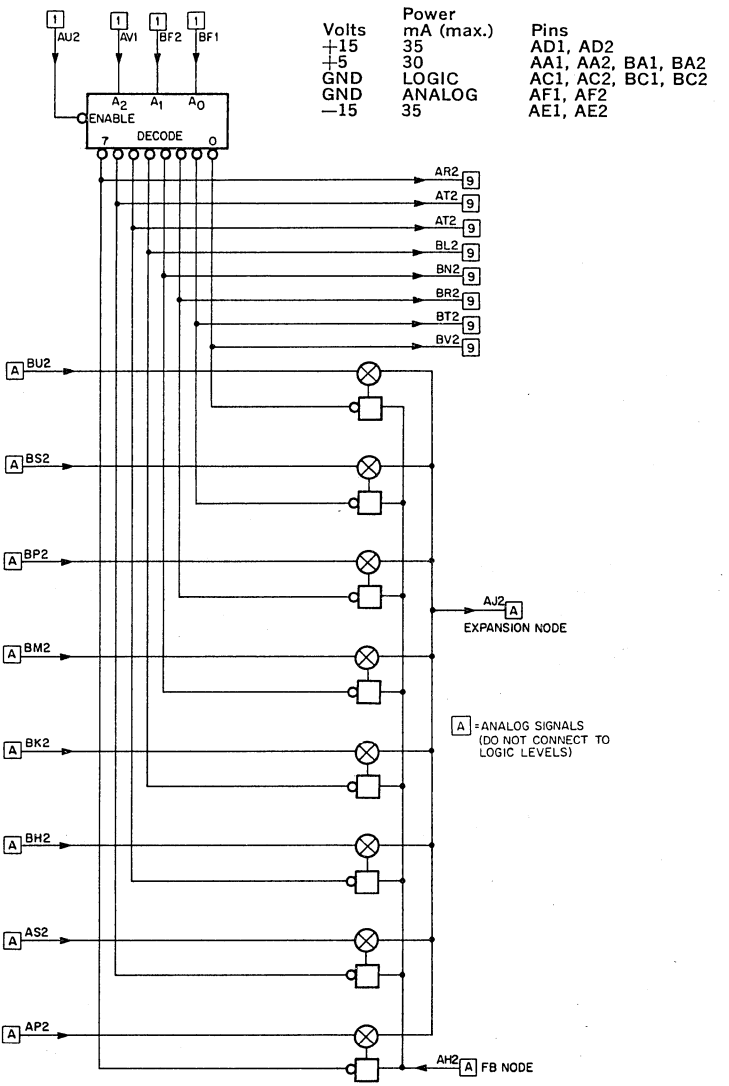
MULTI-PLEXERS

A SERIES

Length: Standard
Height: Double
Width: Double

Price:

$160.



Volts	Power mA (max.)	Pins
+15	35	AD1, AD2
+5	30	AA1, AA2, BA1, BA2
GND	LOGIC	AC1, AC2, BC1, BC2
GND	ANALOG	AF1, AF2
−15	35	AE1, AE2

The A162 is a high impedance multiplexer with decoder consisting of 8 independent FET switched channels. Included on this module is a gated binary to octal decoder for selecting any of the eight high speed channels.

The A162 may be used as a stand-alone multiplexer or with any of the high impedance multiplexers to perform single or double level multiplexing. It also may be used as an expander to increase the channel capabilities of the A163 or A164, Multiplexers.

This unit has been engineered and factory adjusted to provide rated performance, and is fully compatible with DTL and TTL systems.

The A162 employs advanced shielding techniques and optimized circuit layout, ensuring stable operation under normal ambient electrostatic and electromagnetic conditions, as well as allowing minimal crosstalk between channels.

SPECIFICATIONS

Analog Inputs:	8 Single Ended
Input Voltage Range:	±10 V. Maximum full scale
Expander Node:	Common point of 8 channels brought out to a common pin for connection to the input of the external buffer amp.
Feedback Input:	Feedback control point of multiplexer switches connected to output of buffer amplifier.
Input Leakage:	0.5 nano Ampere, max., per channel
Input Feedthrough Capacity:	4 pF per channel
OFF Channel Capacity:	7 pF per channel, shunt capacity at common node
ON Resistance of Channel (Without Buffer):	1000 ohms
Switching Plus Settling Time:	5 μsec., max., to settle to within .01% of final value for full scale excursion with zero source impedance

Decoder

Decoder:	One of 8 lines, decoded, binary
Decoder Outputs:	Select: Logic zero De-select: Logic one
Decoder Inputs—	
A0 IN to A2 IN:	Address Lines One TTL Load High = One

Decoder Gate Input:	Logic zero enables decoder out
Fault Protection:	Current limiting to 10 mA provided
Max. Input Voltage (Without DaDmage):	±15 V.
Output Range:	Same as input (±10 VFS)

A163
HIGH IMPEDANCE MULTIPLEXER
WITH DECODER AND BUFFER AMPLIFIER

MULTI-PLEXERS

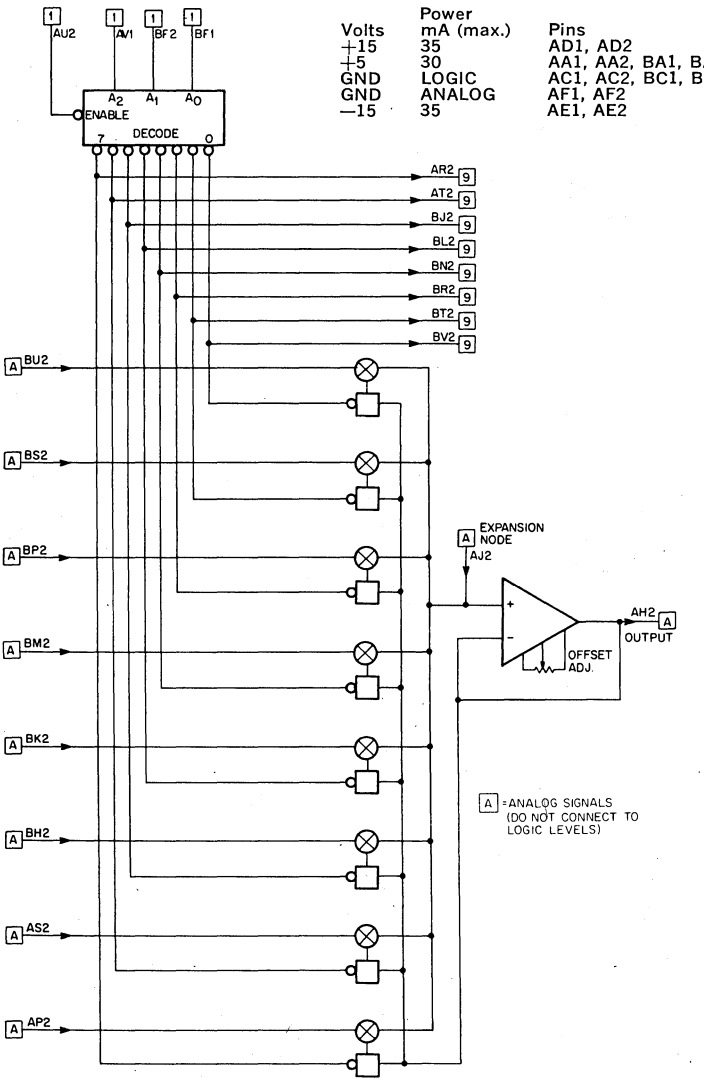
A SERIES

Length: Standard
Height: Double
Width: Double

Price:

$210.

Volts	Power mA (max.)	Pins
+15	35	AD1, AD2
+5	30	AA1, AA2, BA1, BA2
GND	LOGIC	AC1, AC2, BC1, BC2
GND	ANALOG	AF1, AF2
−15	35	AE1, AE2



The A163 is a high impedance multiplexer consisting of 8 FET switched channels, a noninverting unity gain follower amplifier, and an 8 bit binary to octal decoder for channel selecting.

This unit was designed for application where accuracy, speed, and high input impedance are important factors. It also may be used in systems which employ sample and holds, D/A converters, and high speed multiplexing.

Provided on the A163 is an expansion node, which when used in conjunction with either of the high impedance multiplexer expanders (A160, A162) will provide additional input channels.

The A163 is fully compatible wiht DTL and TTL logic levels and may be used with DEC's standard K and M Series digital logic modules.

This module has been engineered and factory adjusted to provide proper operation over the specified range.

Optimized circuit layout has been employed in the packaging of the A163 ensuring minimal crosstalk between channels. Advanced shielding techniques of the switching circuitry have been used to allow proper operation under normal ambient electrostatic and electromagnetic conditions.

SPECIFICATION

No. of Inputs:	8 Single Ended
Input Voltage Range:	±10 V. maximum full scale
Expander Node:	Common point of 8 channels brought out to pin as well as to input of buffer amplifier
Input Leakage:	0.5 nano Ampere, max., per channel
Input Feedthrough Capacity:	4 pF per channel
OFF Channel Capacity:	7 pF per channel, shunt capacity at common node
ON Resistance of Channel (Without Buffer):	1000 ohms
Switching Plus Settling Time:	5 μsec, max. to settle to within .01% of final value for full scale excursion with zero source impedance
Fault Protection:	Current limiting to 10 mA provided
Max. Input Voltage (Without Damage):	±15 V.
Output Range:	Same as Input (±10 VFS)
Output Current:	±20 mA, max.
Output Protection:	Short circuit protection, indefinitely to ground

Amplifier Offset:	Adjustable to zero
Transfer Accuracy:	±0.01% of full scale at 25° C.
Temp. Coefficient:	30 μV/° C.

Decoder

Decoder:	One of 8 lines, decoded, binary
Decoder Outputs:	Select: Logic zero De-select: Logic one
Decoder Inputs—	
A0 IN to A2 IN:	Address Lines One TTL Load
Decoder Gate Input:	Logic zero enables decoder out

A164
CONSTANT IMPEDANCE MULTIPLEXER EXPANDER

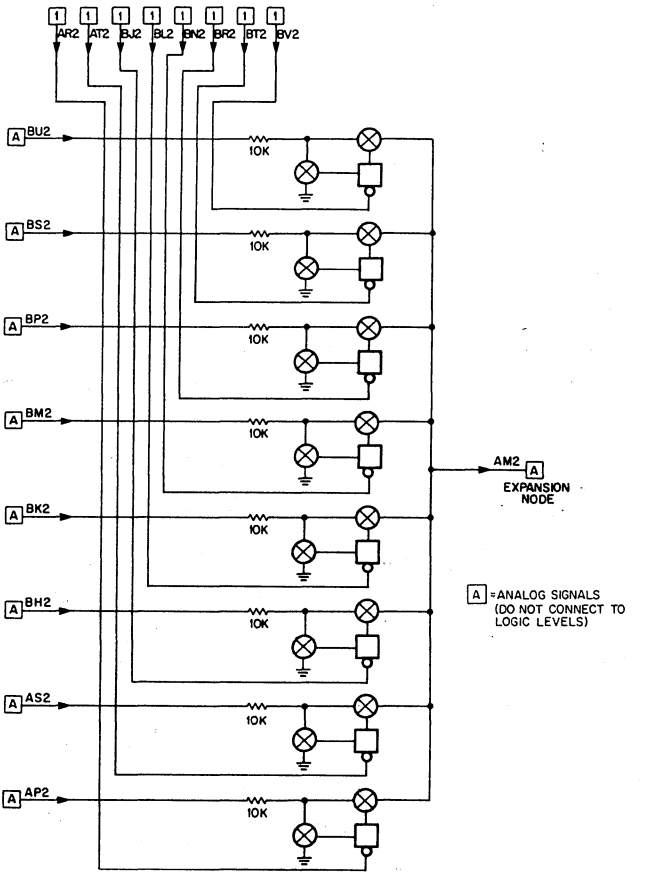
MULTI-PLEXERS

A SERIES

Length: Standard
Height: Double
Width: Double

Price:

$175.



Volts	Power mA (max.)	Pins
+15	40	AD1, AD2
GND	LOGIC	AC1, AC2, BC1, BC2
GND	ANALOG	AF1, AF2
−15	40	AE1, AE2

The A164 is an 8 channel constant impedance multiplexer expander utilizing eight FETS to switch the input signal through eight precision resistors either to ground (OFF) or to a virtual ground null point of an operational amplifier (ON).

This unit is used primarily with the A165, A166, and the A167 as a means of providing additional input channels. It may also be used to do high voltage multiplexing and input scaling.

The A164 does not contain an output amplifier; therefore, to ensure proper operation, the output must be terminated into a buffer amplifier whose gain is equal to minus one. The A164 or the A165 may be used to accomplish this if the A164 is being used as an expander to either of these modules. If used as a stand alone module, the A260 dual amplifier card may be used as a buffer amplifier.

Provided on the A164 are eight channel select lines. These lines are brought to pin connections and may be controlled from an external source such as a shift register, clock, or gating functions.

SPECIFICATIONS

Number of Inputs:	8
Input Impedance:	10,000 ohms
Input Range:	±10 Volts
Switching Plus Settling Time:	5 μsec to .01%
Expander Node:	Summing point brought to pin to allow expansion of number of channels.
Switch Leakage:	0.5 nano Amp per "OFF" channel
Feedthrough (all channels OFF & 20 Vp-p at inputs):	−86dB at 1 kHz (Ratio = 20,000: 1)
Select Lines (1 TTL Load)—	
"ON":	Logic Zero
"OFF":	Logic One

A165
CONSTANT IMPEDANCE MULTIPLEXER WITH OUTPUT AMPLIFIER

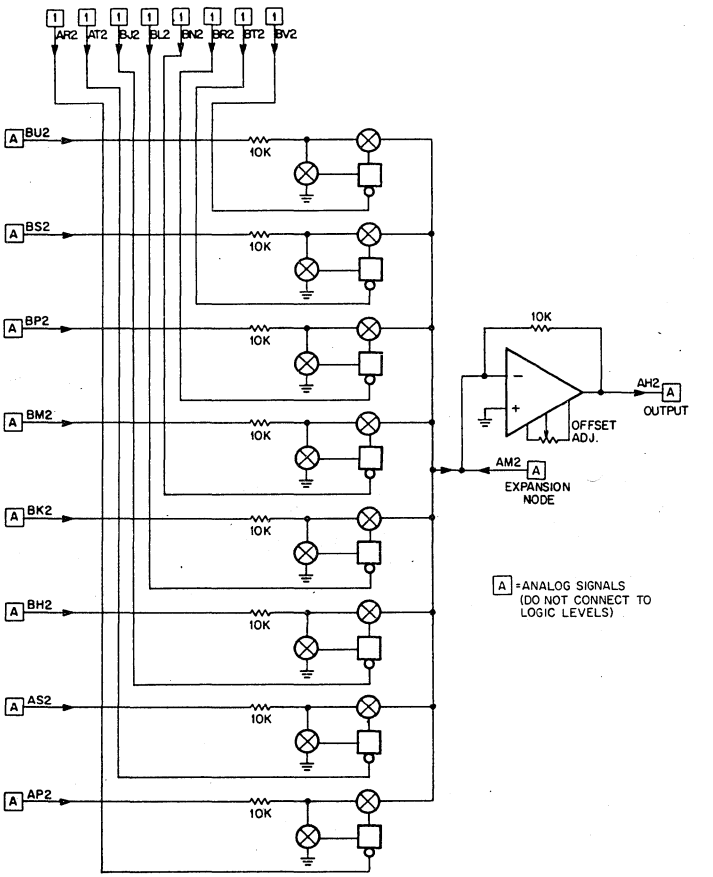
MULTI-PLEXERS

A SERIES

Length: Standard
Height: Double
Width: Double

Price:

$225.



Volts	Power mA (max.)	Pins
+15	40	AD1, AD2
GND	LOGIC	AC1, AC2, BC1, BC2
GND	ANALOG	AF1, AF2
−15	40	AE1, AE2

The A165 is a constant impedance multiplexer consisting of eight independent channels which utilize FETS to switch the input signal through precision resistors into either a ground (OFF) or a virtual ground of an operational amplifier (on).

Included on this module is the operational amplifier, which has been factory adjusted to yield a gain of minus one. Also included on the A165 are eight channel select lines which may be controlled from an external source, such as a shift register, clock, or gating functions.

The A165 is DTL and TTL compatible and may be used with DEC's standard "K" and "M" Series modules to perform control functions.

The A165 may also be used in the multiplexing of high voltage or input scaling. It also may be used in conjunction with other constant impedance multiplexers.

DEC's constant impedance multiplexers have been engineered and packaged using optimized circuit layouts to ensure minimal crosstalk between channels. Advanced shielding techniques allow stable operation under normal ambient electrostatic and electromagnetic conditions.

SPECIFICATIONS

Number of Inputs:	8
Input Impedance:	10,000 ohms
Input Range:	±10 Volts
Output Range:	±10 Volts, inverted with respect to input.
Output Drive:	20 mA.
Switching Plus Settling Time:	5 μsec to .01%
Expander Node:	Summing point brought to pin to allow expansion of number of channels.
Switch Leakage:	0.5 nano Amp per "OFF" channel
Transfer Ratio:	Minus one for 10V range
Transfer Accuracy:	±0.015% of full scale
Temp. Coefficient of Offset:	50 μV/degrees C.
Temp. Coefficient of Gain:	7 PPM/degrees C.
Feedthrough (all channels OFF & 20 Vp-p at inputs):	—86dB at 1 kHz (Ratio 20,000 :: 1)
Select Lines (1 TTL Load)—	
"ON":	Logic Zero
"OFF":	Logic One

A166
CONSTANT IMPEDANCE MULTIPLEXER EXPANDER WITH DECODER

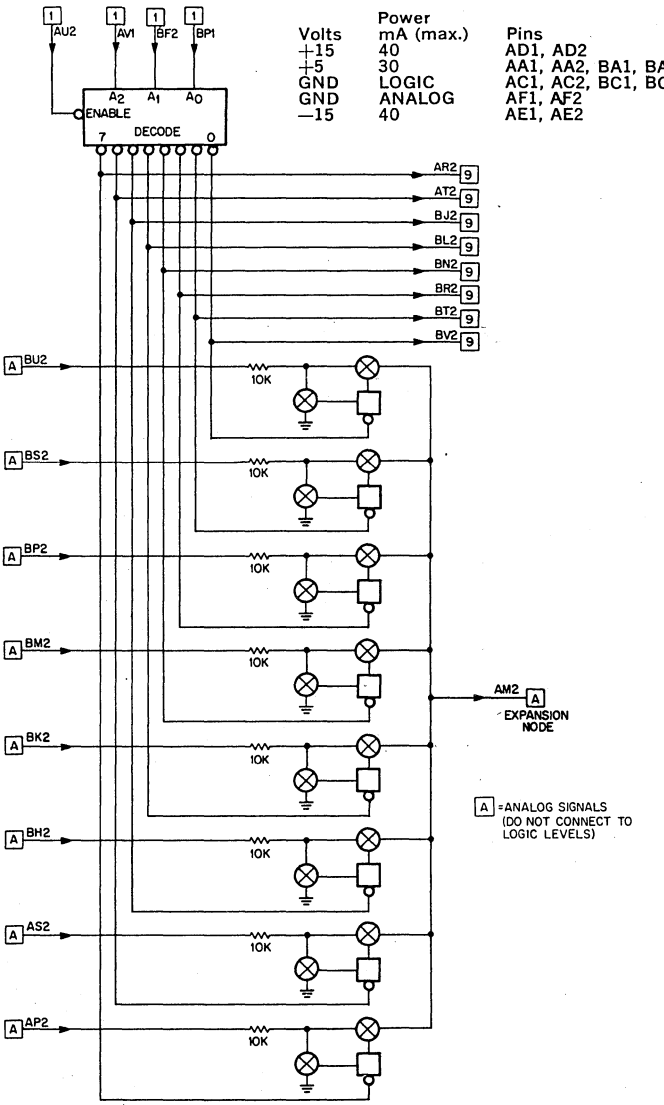
MULTI-PLEXERS

A SERIES

Length: Standard
Height: Double
Width: Double

Price:

$185.



Volts	Power mA (max.)	Pins
+15	40	AD1, AD2
+5	30	AA1, AA2, BA1, BA2
GND	LOGIC	AC1, AC2, BC1, BC2
GND	ANALOG	AF1, AF2
−15	40	AE1, AE2

The A166 is a constant impedance eight channel multiplexer with decoder.

This unit can be used for multiplexing high voltage signals, single level or double level multiplexing, input scaling, or as a means to expand the channel capabilities of either the A165 or A167 DEC multiplexer.

Contained on the A166 as a binary to octal decoder which can be used to select either randomly or in sequence any of the eight analog input channels.

If the A166 is to be used as a stand alone multiplexer, its output must terminate into the null point of a buffer amplifier whose feedback resistor is 10,000 ohms.

SPECIFICATIONS

Number of Inputs:	8
Input Impedance:	10,000 ohms
Input Range:	±10 Volts
Switching Plus Settling Time with output amp	5 μsec to .01%
Expander Node:	Summing point brought to pin to allow expansion of number of channels.
Switch Leakage:	0.5 nano Amp per "OFF" channel
Transfer Accuracy:	±0.015% of full scale
Feedthrough (all channels OFF & 20 Vp-p at inputs):	—86dB at 1 kHz (Ratio 20,000: 1)

Decoder

Decoder:	One of 8 lines decoded, binary
Decoder Outputs:	9 TTL Loads Select = Logic Zero Deselect = Logic One
Select Lines (1 TTL Load)—	
"ON":	Logic Zero
"OFF":	Logic One
Decoder Inputs—	
A0 IN to A2 IN:	Address Lines—3 bit binary code One TTL Load Positive Voltage = Logic One
Decoder Gate:	One TTL Load Logic One yields disable Logic Zero yields enable

A167
CONSTANT IMPEDANCE MULTIPLEXER
WITH DECODER AND OUTPUT AMPLIFIER

MULTI-PLEXERS

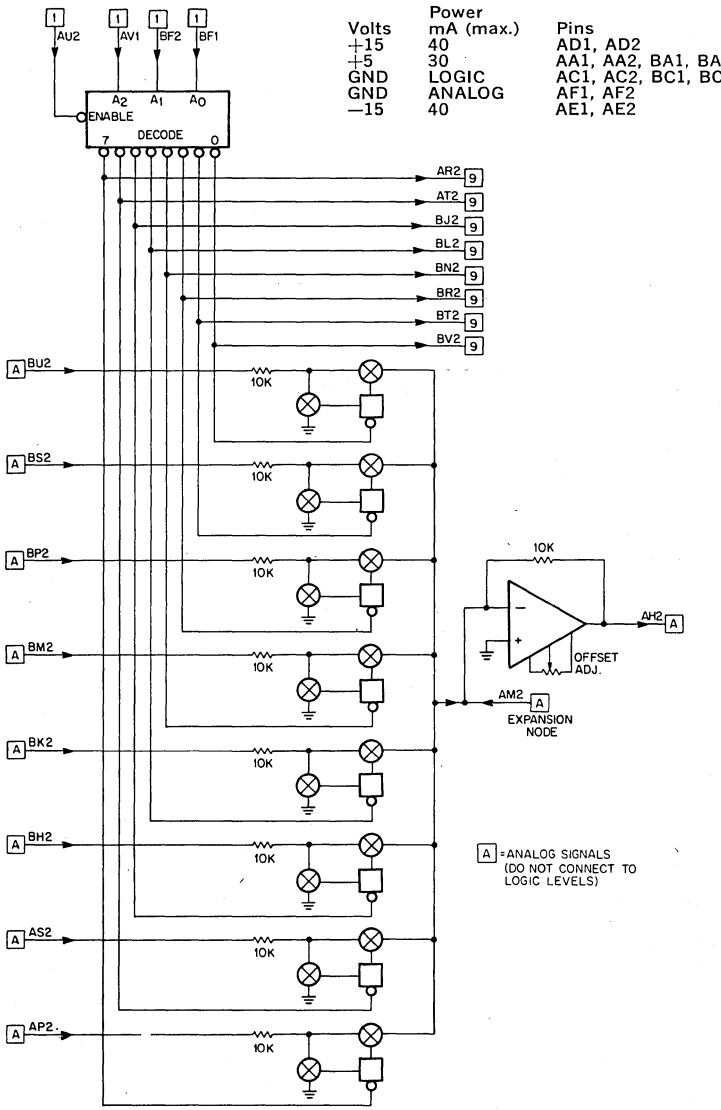
A SERIES

Length: Standard
Height: Double
Width: Double

Price:

$240.

Volts	Power mA (max.)	Pins
+15	40	AD1, AD2
+5	30	AA1, AA2, BA1, BA2
GND	LOGIC	AC1, AC2, BC1, BC2
GND	ANALOG	AF1, AF2
−15	40	AE1, AE2



The A167 is an eight channel constant impedance multiplexer with output amplifier and decoder. The operation of the A167 is performed in the same manner as any of the other DEC constant impedance multiplexers, where the input signal is switched via FETs to either ground (OFF) or into a virtual ground null point (ON) of the operational amplifier.

This unit may be used for multiplexing of high voltages, input scaling, and in situations that require single or double level multiplexing.

The A167 has the capability of being expanded by any of the constant impedance multiplexers (A166, A164). The limitation to the number of channel expansions will depend upon system specifications, speed, leakage current of OFF channels, and the output drive capabilities of the source.

The output amplifier has been factory adjusted and preset to a gain of minus one. The decoder is an eight bit binary to octal decoder with gating facilities on the decoder to control its states.

Advanced shielding and layout techniques have been employed on the A167 to allow stable operation under normal ambient electrostatic and electromagnetic conditions as well as minimal crosstalk between channels.

SPECIFICATIONS

Number of Inputs:	Eight
Input Impedance:	10,000 ohms
Input Range:	±10 Volts
Output Range:	±10 Volts
Output Drive:	20 mA.
Switching Plus Settling Time:	5 μsec to .01%
Expander Node:	Summing point brought to pin to allow expansion of number of channels.
Switch Leakage:	0.5 nano Amp per "OFF" channel
Transfer Ratio:	Minus one for 10V range
Transfer Accuracy:	±0.015% of full scale
Temp. Coefficient of Offset:	50 μV/degrees C.
Temp. Coefficient of Gain:	7 PPM/degrees C.
Feedthrough (all channels OFF & 20Vp-p at inputs):	—86dB at 1 kHz (Ratio 20,000 : 1)
Select Lines (1 TTL Load)—	
"ON":	Logic Zero
"OFF":	Logic One

Decoder

Decoder:	One of eight lines decoded, binary
Decoder Outputs:	9 TTL Loads Select = Logic Zero Deselect = Logic One
Decoder Inputs—	
A0 IN to A2 IN:	Address Lines—3 bit binary code One TTL Load Positive voltage = Logic One
Decoder Gate:	One TTL Load Logic One yields disable Logic Zero yields enable

A207
OPERATIONAL AMPLIFIER

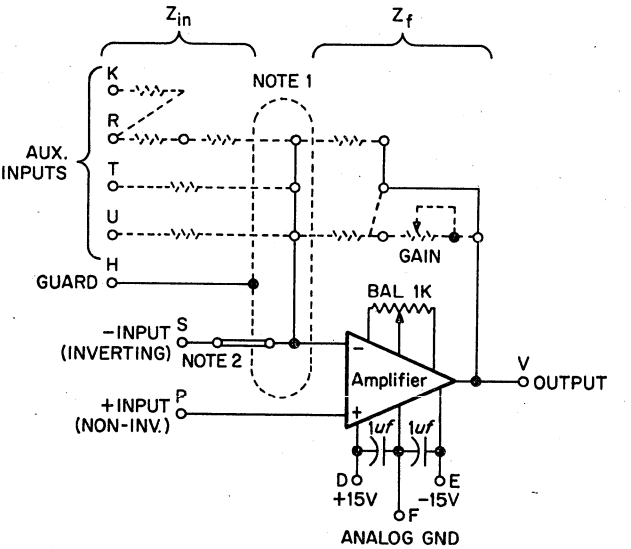
AMPLIFIERS

A SERIES

Length: Standard
Height: Single
Width: Single

Price:

$45



Volts	Power mA (max.)	Pins
+15	6	D2
GND	ANALOG	F2
−15	10	E2

NOTE 1. Mounting holes are provided on the module so that input and feedback components can be added. Components shown with dashed lines are not included with the module.

NOTE 2. This jumper comes with the module. It may be removed to suit circuit requirements.

NOTE 3. Pins L & M can be connected together to improve settling time, but parameters such as drift and open loop gain are degraded.

The A207 is an economical Operational Amplifier featuring fast settling time (5 μs to within 10 mv), making it especially suited for use with Analog-to-Digital Converters. The A207 can be used for buffering, scale-changing, offsetting, and other data-conditioning functions required with A/D Converters. All other normal operational amplifier configurations can be achieved with the A207.

The A207 is supplied with a zero balance potentiometer. Provisions are made on the board for the mounting of input and feedback components, including a gain trim potentiometer. The A207 is pin-compatible with the A200 Operational Amplifier.

SPECIFICATIONS—At 25°C, unless noted otherwise.

	Pins L & M Connected	Differences with Pins L & M Not Connected
Settling Time*		
Within 10 mV, 10V step input, typ:	3 μsec	6 μsec
Within 10 mV, 10V step input, max:	5 μsec	8 μsec
Within 1 mV, 10V step input, max:	7 μsec	10 μsec
Frequency Response		
Dc open loop gain, 670 ohm load, min:	15,000	100,000
Unity gain, small signal, min:	3 MHz	
Full output voltage, min:	50 kHz	
Slewing rate, min:	3.5v/μsec	
Overload recovery, max:	8 μsec	
Output		
Voltage, max:	±10V	
Current, max:	±15 mA	
Input Voltage		
Input voltage range, max:	±10 V	
Differential voltage, max:	±10V	
Common mode rejection, min:	10,000	
Input Impedance		
Between inputs, min:	100 k ohms	
Common mode, min:	5 M ohms	
Input Offset		
Avg. voltage drift vs. temp, max:	60 μV/°C	30 μV/°C
Initial current offset, max:	0.5 μA	
Avg. current drift vs. temp, max:	5 nA/°C	
Temperature Range	0°C to +60°C	

*Gain of 1, inverting or non-inverting configuration.

A260
DUAL AMPLIFIER CARD

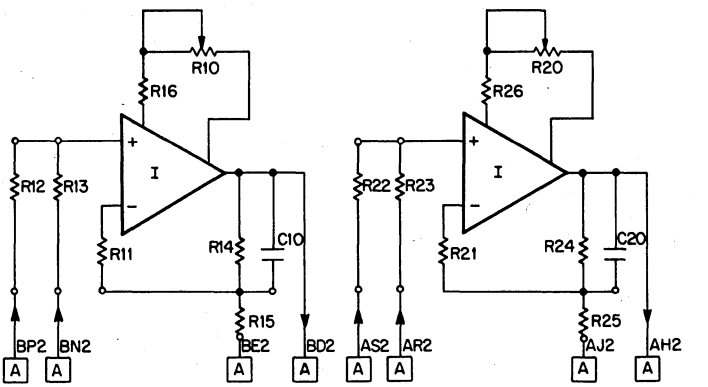
AMPLIFIERS

A SERIES

Length: Standard
Height: Double
Width: Double

Price:

$150.



A = ANALOG SIGNALS
(DO NOT CONNECT TO
LOGIC LEVELS)

Volts	Power mA (max.)	Pins
+15	20	AD2
GND	ANALOG	AF2
−15	20	AE2

The A260 is a universal dual amplifier card which contains two independent operational amplifiers. Provisions have been made for mounting input and feedback components so that the A260 may be used in a variety of modes.

Some of the configurations in which the A260 may be used are:

1. Voltage follower with a gain of plus one.
2. Voltage follower with positive gain of greater than one.
3. Attenuated follower with positive gain of less than one.
4. Differential amplifier with differential input and single ended output.
5. Inverter with negative gain of one or greater.

The A260 may also be used as the output buffer for the A160 and A164 multiplexer series, as well as the input buffer for the A400 series sample and hold modules. Individual offset adjustments are provided for on each amplifier.

SPECIFICATIONS

Description:	Two differential amplifiers mounted on one board with provision for mounting resistors in a variety of modes.
Offset:	Adjustments provided to adjust offset to zero.

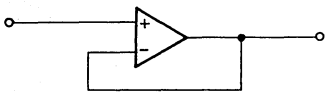
Configurations

A.	Follower	High input impedance, gain of plus one.
	Transfer Accuracy:	±0.01% of FS
	Settling Time (0 to 10v):	1.5 μs to .01%
	Output drive:	20 mA., short circuit proof to ground.
	Input/output range:	±10 Volts
	Input impedance:	1000 megohms
	Temp. Coefficient:	30 μV/°C.
B.	Follower with Gain—	High input impedance, positive gain greater than one.
	Transfer accuracy:	Function of resistors provided.
	Gain:	Determined by $\frac{R14 + R15}{R15}$
	Settling Time:	(Gain) x (1.5 μs) to .01%
	Output Drive:	20 mA. short circuit proof to ground.
	Input/Output range:	±10 Volts
	Input Impedance:	⩾100 megohms
	Temp. Coefficient:	30 μV/° C. (referred to input)
C.	Attenuated follower—	Input attenuator, positive gain less than one.
	Gain:	$\frac{R13}{R12 + R13}$ (see schematic)
	Transfer Accuracy:	Function of resistors provided.
	Settling Time:	1.5μs to .01% if not limited by attenuator.
	Input Range:	0 to ±100 Volts, max.
	Output Range:	±10 Volts

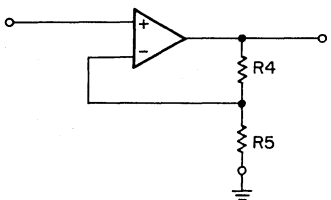
Output Drive:	20 mA., short circuit proof to ground.
Input Impedance:	R12 + R13
Temp. Coefficient:	30 μV/° C. plus input attenuation.
D. Differential Amplifier:	Differential input, single ended output.
Gain:	$\frac{R14}{R15}$
Transfer Accuracy:	Function of resistors provided.
Settling Time:	(Gain) x (1.5μs)
Input Voltage (Signal plus common mode):	$(1 + \frac{1}{Gain}) \times$ (10V) max.
Output Range:	±10 Volts
Output Drive:	20 mA., short circuit proof to ground.
Temp. Coefficient:	(30 μV/° C) x (1 + Gain)
Common Mode Rejection:	Function of resistor matching in each input > 86dB for .01% resistor watch in addition to transfer accuracy of .01%
E. Inverter	Negative gain of one or greater

Specs same as differential amplifier, except input referenced to ground.

1. FOLLOWER

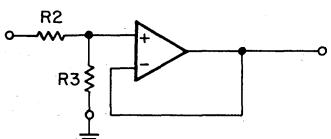


2. PLUS GAIN



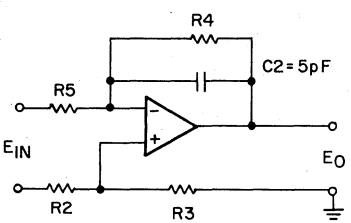
$$\frac{E_O}{E_{IN}} = \frac{R4+R5}{R5}$$

3. POSITIVE GAIN LESS THEN ONE



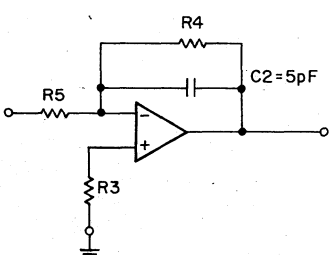
$$\frac{E_O}{E_{IN}} = \frac{R3}{R3+R2}$$

4. DIFF. INPUT



$$\frac{E_O}{E_{IN}} = \frac{R4}{R5}$$

5. INVERTER



$$\frac{E_O}{E_{IN}} = \frac{R3}{R4}$$

R12 R22	R13 R23	R14 R24	R15 R25
0Ω	∞	0	∞
0Ω	∞	5K G=	5K +2
		9K G=	1K +10
50K G=	50K +1/2	0	∞
20K	20K G=	20K 1	20K
∞	10K G=	20K −1	20K

A404
SAMPLE AND HOLD

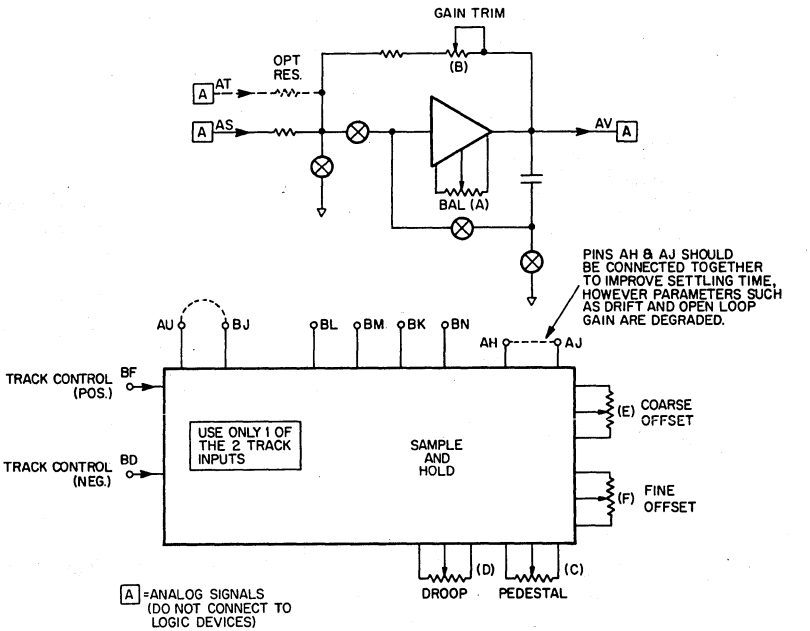
SAMPLE & HOLD

A SERIES

Length: Standard
Height: Double
Width: Single

Price:

$130



Volts	Power mA (max.)	Pins
+15	22	AD2
GND	ANALOG	AC2, AF2
−15	35	AE2

JUMPER CONNECTIONS TO OFFSET OUTPUT

MODE		
PIN	TRACK (sample)	HOLD
BF (pos)	+ 3v or open	0v
BD (neg)	−3v or open	0v

Positive	Negative
AU to BJ	AU to BJ
	BL to AD
BM to AE	
BK to AF	BN to AF

Analog gnd (pin AF) and digital gnd (pin AC) must be connected together at one point in the system.

The A404 Sample & Hold has an acquisition time of 6 μsec for a 10 volt signal to within 10 mV (0.1%). The circuit inverts the input signal, and has an input impedance to 10 k. Features of the circuit include potentiometers to control the pedestal and the droop of the output signal.

Two digital Track Control (sample) inputs are provided: one for negative logic (0v & −3v), and the other for positive logic (0v & +3v). Either input by itself will perform the necessary control, and the inadvertent application of both digital signals will cause no damage to the circuit.

Potentiometers are also provided for zero balancing, gain trim, and offset adjustment (up to ±10v). If offsetting is desired, connections should be made according to the table shown with the diagram.

SPECIFICATIONS—At 25°C, unless noted otherwise. Pins AH & AJ are connected together.

Acquisition Time	
Within 10 mV, 10V step input, typ:	4 μsec
Within 10 mV, 10V step input, max:	6 μsec
Within 2.5 mV, 10V step input, max.	11 μsec
Aperture Time, max:	0.2 μsec
Gain	−1.000 (adjustable ±0.2%)
Input	
Voltage range, max:	±10V
Impedance:	10k ohms
Output	
Voltage range, max:	±10V
Current, max:	10 mA
Pedestal*	
Initial pedestal:	Adjustable to less than 1 mV
Pedestal variation vs. temp, max:	0.2 mV/°C
Droop	
Initial droop:	Adjustable to less than 5 mV/ms
Droop variation vs. temp, max:	2 mV/ms/°C
Track Control	
Pos. (pin BF)	+3V, Track 0V at 2 mA, Hold
Neg. (pin BD)	−3V, Track 0V at 1 mA, Hold
Board Size	1 double height board, single module width
Temperature Range	0°C to +50°C

*Difference in output voltage when changing from Track to Hold mode.

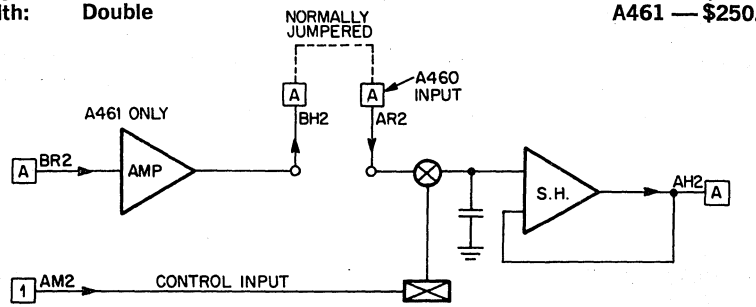
A460/A461
SAMPLE AND HOLD

SAMPLE & HOLD

A SERIES

Length: Standard
Height: Double
Width: Double

Price:
A460 — $200.
A461 — $250.



A =ANALOG SIGNALS (DO NOT CONNECT TO LOGIC LEVELS)

Volts	Power mA (max.)	Pins
+15	12, 20*	AD2
GND	ANALOG	AF2
−15	12, 20*	AE2

*with buffer

The A460 and A461 are one-channel sample and hold modules used to sample the value of a changing analog signal at a particular point in time and store this information as a stable analog voltage level. The A460 is without input buffering; the A461 includes a unity-gain input buffer amplifier. When the A461 is used an external jumper is required between pins BH2 and AR2.

Provided on the A460 and A461 is a select line which can be used to control the sample or hold operation of the module.

Both the A460 and A461 are DTL and TTL compatible and may be used with standard "M" or "K" Series modules in control and system configurations.

The output circuitry consists of a buffer amplifier with output drive capability of 20 mA. Both the A460 and A461 are compatible with DEC "A" Series high impedance and constant impedance multiplexers and may be used with either to perform various levels of multiplexing.

SPECIFICATIONS

Transfer Accuracy at 23° C.:	±0.01% FS in Hold mode
Input/Output Voltage Range:	±10V Full Scale
Transfer Characteristic:	+1 (non-inverted)
Acquisition Time (to 0.01%):	5 microseconds for −10V to +10V excursion
Aperture Time	Less than 50 nanoseconds
Input Impedance (During Sample Time)—	
(With No Buffer):	100 ohms in series with 0.002 microfarad capacitor
(With Buffer):	1000 megohms in parallel with 10 pF.
Output Drive:	20 mA.
Pedestal in Sample mode:	10 mV max.
Hold Decay:	15 μV per millisecond
Offset:	Adjustable to zero
Temp. Coefficient of Offset:	50 μV per degree C.
Control Input (1 TTL Load)—	
Sample:	Logic Zero
Hold:	Logic One

A613
12-BIT D/A CONVERTER

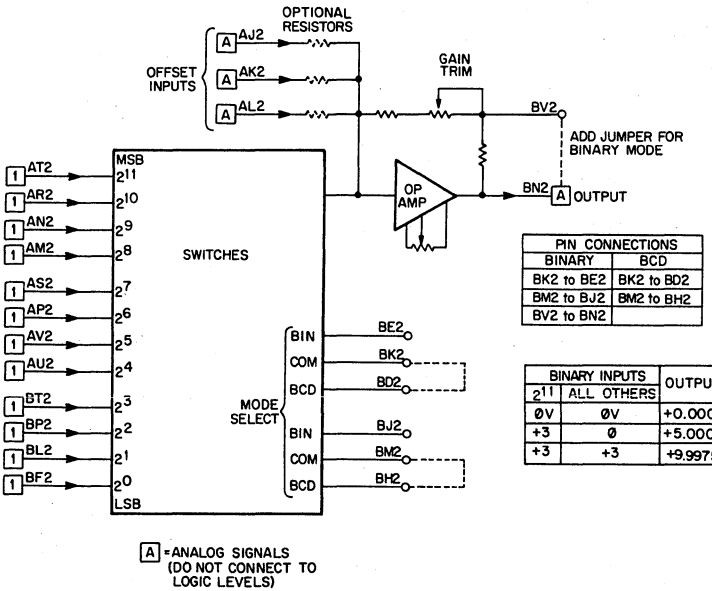
DIGITAL TO ANALOG

A SERIES

Length: Standard
Height: Double
Width: Single

Price:

$200



PIN CONNECTIONS	
BINARY	BCD
BK2 to BE2	BK2 to BD2
BM2 to BJ2	BM2 to BH2
BV2 to BN2	

BINARY INPUTS		OUTPUT
2^{11}	ALL OTHERS	
ØV	ØV	+0.000V
+3	Ø	+5.000V
+3	+3	+9.9975V

Power		
Volts	mA (max.)	Pins
+15	35	AD2
+5	60	AA2
GND	LOGIC	AC2
GND	ANALOG*	AF2
−10 REF	−7**	AH2
−15	60	AE2

* Analog and Logic ground must be connected together at some point in the system
** reverse current

The A613 is a 12-bit Digital-to-Analog Converter for moderate speed applications. The module is controlled by standard positive logic levels, has an output between Ov and +10v, and will settle within 50 μsec for a full scale input change. The input coding can be either straight binary or 3 decades of 8421 BCD with only simple connector jumpers required to take care of the change.

The A613 requires a −10.0v reference that can supply negative current, such as an A704. Provisions are made for adding up to 3 extra resistors to implement offsetting functions. Potentiometers are provided for zero balancing, and gain trim.

An input of all Logic 0's produces zero volts out; all Logic 1's produces close to +10v out. The operational amplifier output can be shorted to Ground without damaging the circuit.

SPECIFICATIONS

Inputs

Logic ONE:	+2.0V to +5.0V
Logic ZERO:	0.0V to +0.8V
Input loading:	1 mA (max.) at 0 Volts

Output

Standard:	0V to +10V
Optional, (requires Positive REF)	10v range between −10V and +10V
Settling time, (10V step):	50 μsec
Output current:	10 mA
Capacitive loading:	0.1 μF (without oscillation)

Binary Dig. In.	Analog Out	BCD (8421)	Analog Out
000 — 00	0.0000v	000	0.000v
000 — 01	+0.0025	001	+0.010
100 — 00	+5.0000	050	+0.500
111 — 11	+9.9975	500	+5.000
		999	+9.990

Accuracy	Binary	BCD
At +25°C:	±0.015% of full scale	±0.05% of full scale
Temp. coef:	±0.001%/°C (plus drift of REF)	±0.002%/°C (plus drift of REF)

Temperature Range

+10°C to +50°C

If the Output is accidentally shorted to Ground, the output amplifier will not be damaged.

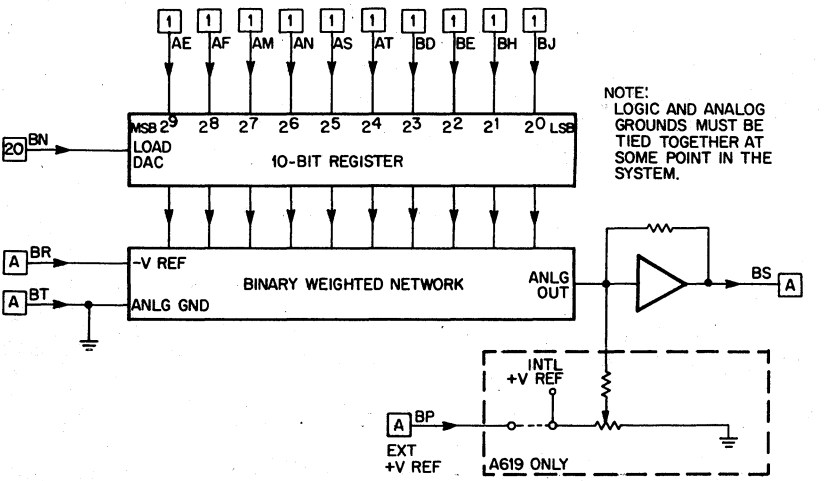
A618 AND A619
10-BIT D/A CONVERTER
SINGLE BUFFERED

DIGITAL TO ANALOG

A SERIES

Length: Standard
Height: Double
Width: Double

Price:
A618 — $125.
A619 — $125.



Volts	Power mA (max.)	Pins
+15	25**	BV2
+5	135	AA2
GND	LOGIC	AC2
GND	ANALOG	BT2
−10.06*	60	BR2
−15	35**	BU2
−15	50	AB2

* ref.
** plus output loading

The A618 and the A619 Digital to Analog Converters (DAC) are double width in the lower (B section) half. The converters are complete with a 10-bit buffer registers, level converters, a precision divider network, and a current summing amplifier capable of driving external loads up to 10 mA. The reference voltage is externally supplied for greatest efficiency and optimum scale factor matching in multi-channel applications.

The A619 DAC output voltage is bi-polar while the A618 DAC output voltage is uni-polar.

Binary numbers are represented as shown (right justified) in Table 1:

TABLE 1

Binary Input	Analog Output (Standard)	
	A618	A619
0000_8	0V	−5V
0400_8	+2.5V	−2.5V
1000_8	+5.0V	0Volts
1400_8	+7.5V	+2.5V
1777_8	+10.0V	+5V

SPECIFICATIONS

OUTPUT:

Voltage: A618	0 to +10 volts
Voltage: A619	±5 volts
Current:	10 mA. (max)
Impedance:	<0.1 ohm
Settling Time:	
(Full scale step, resistive load)	<5.0 μs
(Full scale step, 1000 pf)	<10.0 μs
Resolution:	1 part in 1024
Linearity:	±0.05% of full scale
Zero Offset:	±5 mV. (max)
Temperature Coefficient:	<0.2 mV/°C
Temperature Range:	0 to 50°C

INPUT

Level: 1 TTL Unit Load
Pulse: (positive)

Input loading: 20 TTL Unit load	
Rise and Fall Time:	20 to 100 nsec
Width:	>50 ns
Rate:	10^6 Hz max.

Timing:

Data lines must be settled 40 ns before the "LOAD DAC" pulse (transition) occurs.

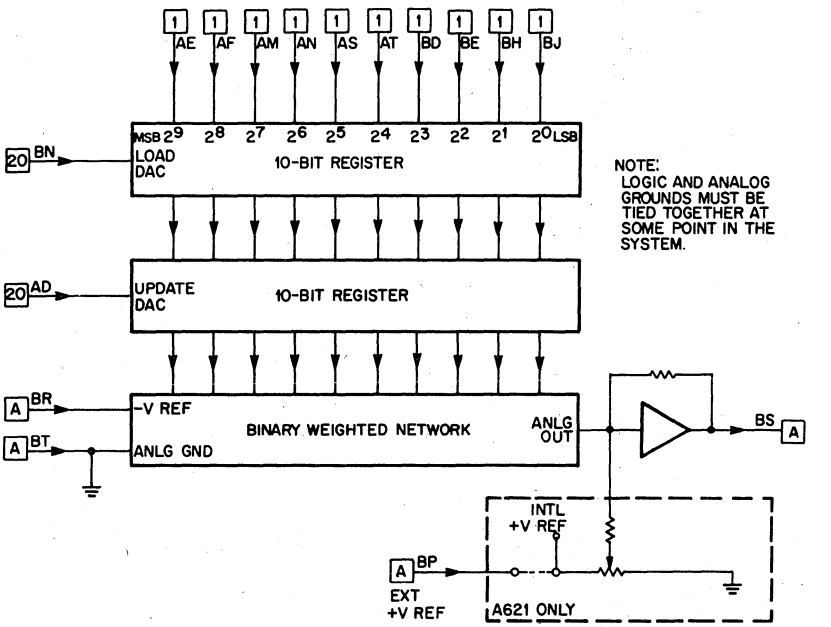
A620 AND A621
10-BIT D/A CONVERTER
DOUBLE BUFFERED

DIGITAL TO ANALOG

A SERIES

Length: Standard
Height: Double
Width: Double

Price:
A620 — $125.
A621 — $125.



Volts	Power mA (max.)	Pins
+15	25**	BV2
+5	190	AA2
GND	LOGIC	AC2
GND	ANALOG	BT2
−10.06*	60	BR2
−15	85**	BU2
−15	50	AB2

* ref.
** plus output loading

The A620 and the A621 Digital-to-Analog Converters (DAC) are double-width in the lower (B section) half. The converters are complete with two 10-bit buffer registers, level converters, a precision divider network, and a current summing amplifier, capable of driving external loads up to 10 mA. The reference voltage is externally supplied for greatest efficiency and optimum scale-factor matching in multi-channel-application.

The A621 DAC output voltage is bi-polar while the A620 DAC output voltage in uni-polar.

The double-buffered DAC's are offered to satisfy those applications where it is imperative to update several analog output simultaneously. When DAC's deliver input to a multi-channel analog tape system or update the constants of an analog computer, the double-buffer feature may be necessary to prevent skew in the analog data.

Binary numbers are represented as shown (right justified) in Table 1:

TABLE 1

Binary Input	Analog Output (Standard)	
	A620	A621
0000_8	0V	−5V
0400_8	+2.5V	−2.5V
1000_8	+5.0V	−0 Volts
1400_8	+7.5V	+2.5V
1777_8	+10.0V	+5V

SPECIFICATIONS

OUTPUT:

Voltage: A620	0 to 10 Volts
Voltage: A621	±5 Volts
Current:	10 mA. (max)
Impedance:	<0.1 ohms
Settling Time:	
(Full scale step, resistive Load)	<5.0 μs
(Full scale step, 1000 pf)	<10 μs
Resolution:	1 part in 1024
Linearity:	±0.05% of full scale
Zero Offset:	±5 mV. (max)
Temperature Coefficient:	<0.2 mV/°C
Temperature Range:	0 to 50°C

INPUT:

Level: 1 TTL Unit load
Pulse: (positive)

Input loading:	20 TTL Unit load
Rise and Fall Time:	20 to 100 ns
Width:	>50 ns
Rate:	10^6 Hz (max)

Timing:

1. Data lines must be settled 40 ns before the "LOAD DAC" pulse (transition) occurs.
2. The "Update DAC" pulse must occur more than 100 ns after the "LOAD DAC" pulse.

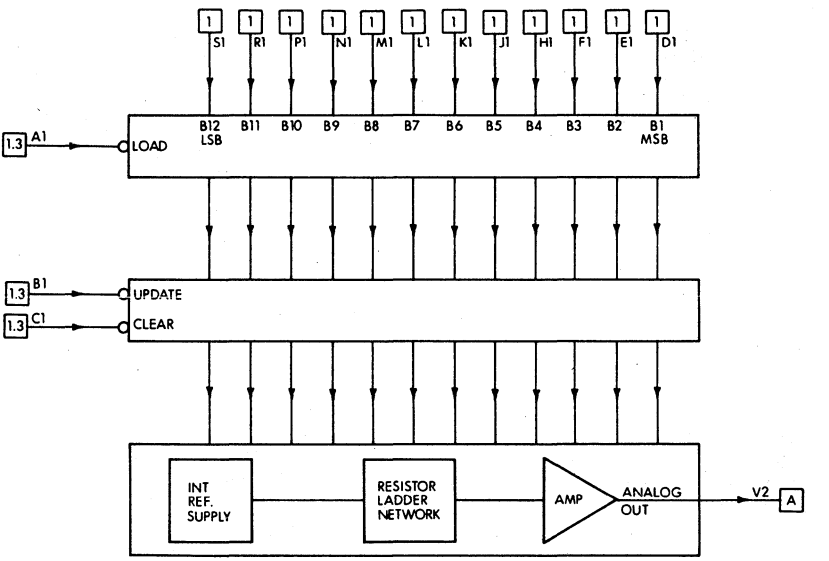
A623
12-BIT DOUBLE-BUFFERED DAC

DIGITAL TO ANALOG

A SERIES

Length: Standard
Height: Single
Width: Single

Price
$350



Volts	Power mA (max.)	Pins
+15	25	D2
+5	315	A2
GND	LOGIC	C2, T1
GND	ANALOG	F2, U2
—15	25	E2

The A623 module is a 12-bit double-buffered digital-to-analog converter. It provides a means of converting 12 binary bits into analog voltages in less than 5 microseconds. It contains an internal reference power supply; therefore, no external supply is needed.

Table 1 shows the output conditions for corresponding inputs.

TIMING

1. Data must be present at the inputs 25 ns before the LOAD pulse goes Low, and the LOAD pulse must remain Low for at least 50 ns.
2. The UPDATE pulse must go Low no sooner than 75 ns after the LOAD pulse, and should remain Low for at least 50 ns.
3. The DAC is cleared by a Low level on the CLEAR input that remains Low for at least 50 ns.

TABLE 1

OUTPUT VOLTAGE	INPUT CODE		INPUT CODE	INPUT COUNTS	
	BASE (10)	BASE (8)	2'S COMPLEMENT BINARY	BASE (8)	BASE (10)
+10.235	2047	3777	011111111111	+3777	+2047
+10.000	2000	3720	011111010000	+3720	+2000
+5.120	1024	2000	010000000000	+2000	+1424
+5.000	1000	1750	001111101000	+1750	+1000
+0.005	0001	0001	000000000001	+0001	+0001
0.000	0000	0000	000000000000	0000	0000
−0.005	4095	7777	111111111111	−0001	−0001
−5.000	3096	6030	110000011000	−1750	−1000
−5.120	3072	6000	110000000000	−2000	−1024
−10.000	2096	4060	100000110000	−3720	−2000
−10.240	2043	4000	100000000000	−4000	−2043

SPECIFICATIONS

Input Code:	Two's complement
Resolution:	1 part in 4096
Step Width:	5.0 mV
Output Range:	−10.240 V −full scale +10.235 V +full scale
Output Current:	± 5 mA (max)
Output Impedance:	1 ohm (max)
Settling Time:	5 μs to ± 1/2 LSB—with a 2K load resistor and a 1000 pF load capacity.
Absolute Accuracy:	± 0.025% of full sale ± 1/2 LSB
Overload Protection:	Direct short to GND or any power input will not harm the circuit.
Linearity:	± 1/2 LSB (2.5 mV)
Offset Voltage:	0 V ± 50 PPM/°C of full scale
Operating Temp. Range:	0°C to 70°C

A660
12-BIT MULTIPLYING D/A CONVERTER

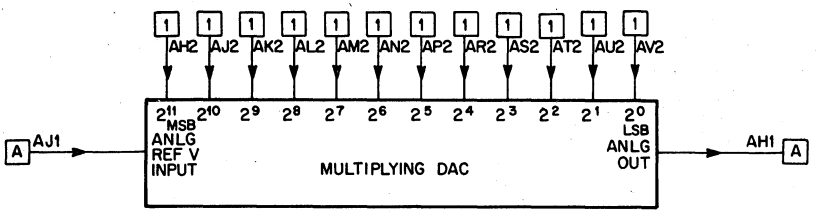
DIGITAL TO ANALOG

A SERIES

Length: Standard
Height: Double
Width: Double

Price:

$300.



NOTE:
LOGIC AND ANALOG GROUNDS MUST BE TIED TOGETHER AT SOME POINT IN THE SYSTEM.

A = ANALOG SIGNALS (DO NOT CONNECT TO LOGIC LEVELS)

Volts	Power mA (max.)	Pins
+15	25	AD1, AD2
+5	45	AA1, AA2, BA1, BA2
GND	LOGIC	AC2, BC2
GND	ANALOG	AF1, AF2
−15	25	AE1, AE2

The A660 is a precision 12 bit multiplying digital to analog converter whose output is the product of the external analog reference voltage supplied and digital code presented.

This D/A Converter is DTL and TTL compatible, requires essentially zero warmup time. It also may be used in either unipolar or bipolar operations.

This unit may be used in applications where precision digital control must be exercised over an analog signal. It also may be used in systems requiring synchro to digital conversion, AC transducer digitization, or in hybrid computation.

When operating in conjunction with an external DC reference source, the A660 may be used as a conventional D/A converter with the output polarity determined by the reference voltage polarity.

The A660 employs advance shielding techniques which allow proper operation under normal ambient electrostatic and electromagnetic conditions.

SPECIFICATIONS

Number of Bits:	12
Coding:	Binary—Absolute Value
Input Logic Levels:	High = Logic One I TTL Load
Accuracy—(dc to 4 kHz)	±.025% FS, ±0.01% of output
Temp. Coefficient of Offset:	200 microvolts/° C.
Temp. Coefficient of Range:	20 PPM/° C.
Feedthrough (for 20 V. p-p sine wave; all bits off):	at 1 KHz: 1 mV RMS
Analog Reference Input Range:	±10 v. Full Scale
Input Impedance:	10 k ohms
Frequency:	Down 0.02% at 20 kHz
Phase Shift:	< 7° at 20 kHz
Output Range:	±10 V.
Output Current:	15 mA.
Short Circuit Protection:	Indefinitely to ground
Phase	Output in Phase with Ref.

Attenuation Range—Absolute Value

DIGITAL				OUTPUT
000	000	000	000	0.0000 Volts
111	111	111	111 Binary	(0.9976) X (Input Ref.) Volts

Settling Time to Digital Change: 12 μs to 0.015% of full scale

POWER SUPPLY

Requires ±15V power supply voltages to remain within 1% of 15 volts.

A661
12-BIT BCD MULTIPLYING D/A CONVERTER

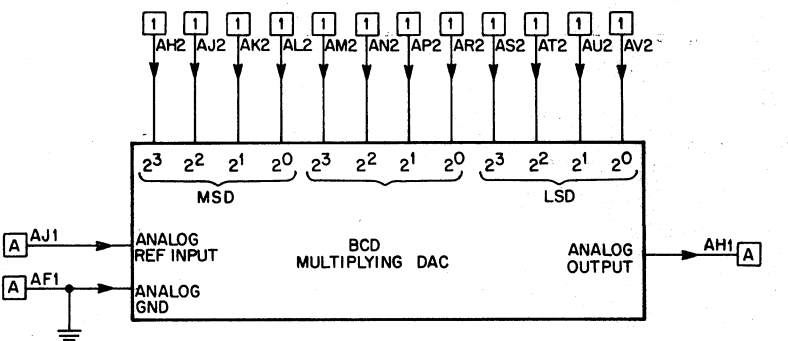
DIGITAL TO ANALOG

A SERIES

Length: Standard
Height: Double
Width: Double

Price:

$300.



A =ANALOG SIGNALS
DO NOT CONNECT TO LOGIC LEVELS

NOTE:
LOGIC AND ANALOG GROUNDS MUST BE TIED TOGETHER AT SOME POINT IN THE SYSTEM.

Volts	Power mA (max.)	Pins
+15	25*	AD1, AD2
+5	45	AA1, AA2, BA1, BA2
GND	LOGIC	AC2, BC2
GND	ANALOG	AF1, AF2
−15	25*	AE1, AE2

*Exclusive of load.

The A661 is a precision 12 bit multiplying digital to analog converter whose output is the product of the external analog reference voltage supplied and digital code presented.

This D/A converter is DTL and TTL compatible, requires essentially zero warmup time. It also may be used in either unipolar or bipolar operations.

This unit may be used in applications where precision digital control must be exercised over an analog signal. It also may be used in systems requiring synchro to digital conversion, ac transducer digitization, or in hybrid computation.

When operating in conjunction with an external dc reference source, the A661 may be used as a conventional D/A converter with the output polarity determined by the reference voltage polarity.

The A661 employs advanced shielding techniques which allow proper operation under normal ambient electrostatic and electromagnetic conditions.

SPECIFICATIONS

Number of Bits:	12
Coding:	BCD—Absolute Value
Input Logic Levels:	High = Logic One 1 Unit TTL Load
Accuracy (dc to 4 kHz):	± .025% FS ± 0.01% of Reading
Temperature Coeff. of Offset:	200 Microvolts/°C
Temperature Coeff. of Range:	20 PPM/°C
Feed through for (20V P-P sine wave; all bits off):	@ 1 kHz: 1mV RMS
Analog Reference Input Range:	± 10V Full Scale Min.
Input Impedance:	> 10k ohms
Frequency:	Down less than 0.02% @ 20 kHz
Phase Shift:	< 7° @ 20 kHz Maximum
Settling Time for —F.S. to +F.S. Digital Increment:	12 μsec to .015% of FSR
Output Range:	± 10 Volts (min)
Output Current:	15 mA (min)
Short Circuit Protect.:	Indefinitely to Ground
Phase:	Output in Phase with Reference

Attenuation Range—Absolute Value

DIGITAL	OUTPUT
000 000 000 000	0.0000 volts
111 111 111 111 Binary	(0.9990) x (input ref.) volts

POWER SUPPLY

Requires ±15V power supply voltages to remain within 1% of 15 volts.

A662
12-BIT 2'S COMPLEMENT D/A CONVERTER

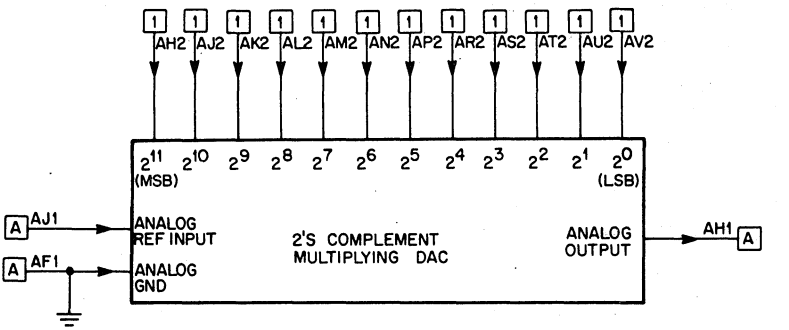
DIGITAL TO ANALOG

A SERIES

Height: Standard
Length: Double
Width: Double

Price:

$300.



A =ANALOG SIGNALS
(DO NOT CONNECT TO LOGIC LEVELS)

NOTE:
LOGIC AND ANALOG GROUNDS MUST BE TIED TOGETHER AT SOME POINT IN THE SYSTEM.

Volts	Power mA (max.)	Pins
+15	25*	AD1, AD2
+5		AA1, AA2, BA1, BA2
GND	LOGIC	AC2, BC2
GND	ANALOG	F1, AF2
−15	25*	AE1, AE2

* Exclusive of load.

The A662 is a precision 12 bit multiplying digital to analog converter whose output is the product of the external analog reference voltage supplied and digital code presented.

This D/A converter is DTL and TTL compatible, requires essentially zero warmup time. It also may be used in either unipolar or bipolar operations.

This unit may be used in applications where precision digital control must be exercised over an analog signal. It also may be used in systems requiring synchro to digital conversion, ac transducer digitization, or in hybrid computation.

When operating in conjunction with an external dc reference source, the A662 may be used as a conventional D/A converter with the output polarity determined by the reference voltage polarity.

The A662 employs advanced shielding techniques which allow proper operation under normal ambient electrostatic and electromagnetic conditions.

SPECIFICATIONS

Number of Bits:	12
Coding:	Binary, 2's Complement
Input Logic Levels:	High = Logic One 1 Unit TTL Load
Accuracy—(dc to 4 kHz):	± .025% FS ± 0.01% of Reading
Temp. Coeff. of Offset:	200 Microvolts/°C
Temp. Coeff. of Range:	20 PPM/°C
Feedthrough for 20V P-P sine wave: (all bits off)	@ 1 kHz: 2mV RMS
Analog Reference Input Range:	± 10V Full Scale Min.
Input Impedance:	> 10k ohms
Frequency:	Down less than 0.02% @ 20 kHz
Phase Shift:	< 7° @ 20kHz Maximum
Settling Time for −F.S. to +F.S. Digital Increment:	12 μS to .015% of FSR
Output Range:	± 10 Volts
Output Current:	15 mA
Short Circuit Protect.:	Indefinitely to Ground
Phase:	Output Phase Depends on B1

Attenuation range—bipolar

DIGITAL	OUTPUT
100 000 000 000	(−1) × (Input Ref.) Volts
000 000 000 000	0.0000 Volts
011 111 111 111	(0.99951) × (Input Ref.) Volts

POWER SUPPLY

Requires ±15V power supply voltages to remain within 1% of 15 volts.

A663
12-BIT STRAIGHT BINARY D/A CONVERTER WITH BUFFER

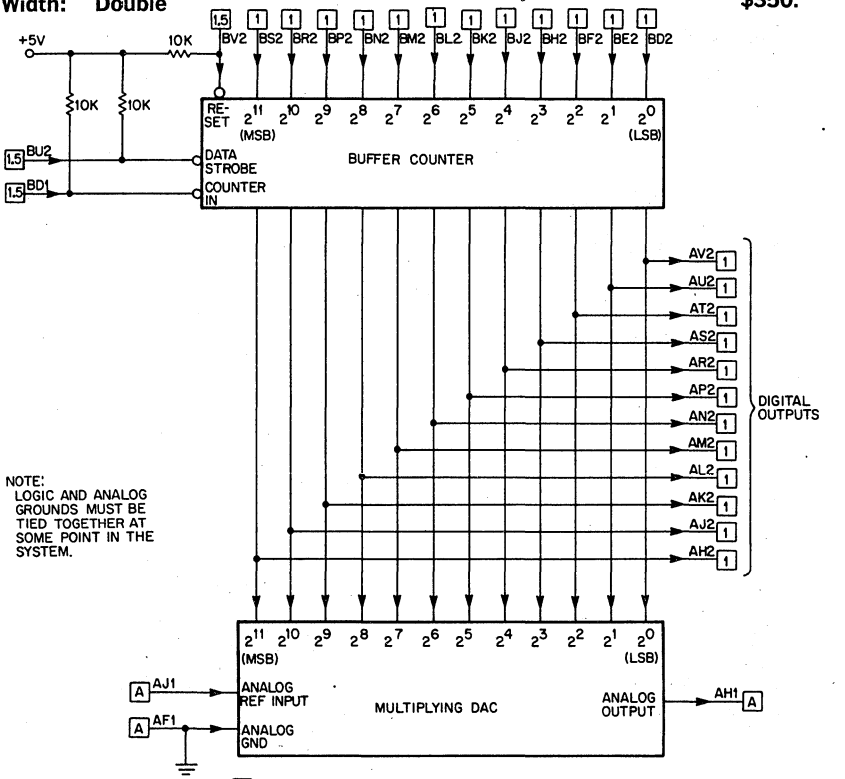
DIGITAL TO ANALOG

A SERIES

Length: Standard
Height: Double
Width: Double

Price:

$350.



A =ANALOG SIGNALS
DO NOT CONNECT TO LOGIC LEVELS

Volts	Power mA (max.)	Pins
+15	25*	AD1, AD2
+5	125	AA1, AA2, BA1, BA2
GND	LOGIC	AC2, BC2
GND	ANALOG	AF1, AF2
−15	25*	AE1, AE2

*Exclusive of Load

The A663 is a precision 12 bit multiplying digital to analog converter whose output is the product of the external analog reference voltage supplied and digital code presented. A 12 bit Buffer Counter provides input to the D/A Converter and external digital outputs.

This D/A Converter is DTL and TTL compatible, requires essentially zero warmup time. It also may be used in either unipolar or bipolar operations.

This unit may be used in applications where precision digital control must be exercised over an analog signal. It also may be used in systems requiring synchro to digital conversion, ac transducer digitization, or hybrid computation.

When operating in conjunction with an external dc reference source, the A663 may be used as a conventional D/A converter with the output polarity determined by the reference voltage polarity.

The A663 employs advanced shielding techniques which allow proper operation under normal ambient electrostatic and electromagnetic conditions.

SPECIFICATIONS

Number of Bits:	12
Coding:	Binary — Absolute Value
Input Logic Levels:	High = Logic One
Accuracy (dc to 4 kHz):	± .025% FS ± 0.01% of Reading
Temperature Coeff. of Offset:	200 Microvolts/°C
Temperature Coeff. of Range:	20 PPM/°C
Feed through for (20V P-P sine wave; all bits off):	@ 1 kHz: 1mV RMS
Analog Reference Input Range:	± 10V Full Scale Min.
Input Impedance:	> 10k ohms
Frequency:	Down less than 0.02% @ 20 kHz
Phase Shift:	< 7° @ 20 kHz Maximum
Counter Input: (normally high)	Ripple Counter counts once each time input signal goes low for 0.5 μs (min).
Reset (normally high):	Resets buffer to all lows when signal goes low for 0.5 μs (min). Overides all other digital inputs.
Data Transfer	Normally High Level, transfers data when brought low for 0.5 μs min
Settling Time for —F.S. to +F.S. Digital Increment:	12 μs to .015% of FSR (from low going edge of the Data Strobe pulse or Counter In pulse).
Settling Time for Worst Case One Count (mid scale):	5 μs to 0.015% of FSR (from the low going edge of the counter in pulse).
Output Range:	± 10 Volts (min)
Output Current:	15 mA (min)
Short Circuit Protect.:	Indefinitely to Ground
Phase:	Output in Phase with Reference

Attenuation Range—Absolute Value

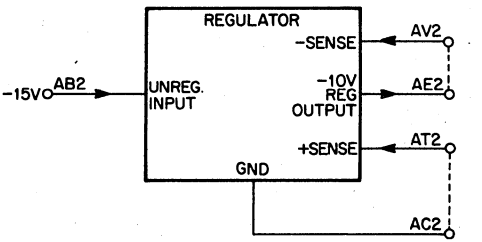
DIGITAL	OUTPUT
000 000 000 000	0.0000 Volts
111 111 111 111 Binary	(0.99976) × (Input Ref.) Volts

A704
REFERENCE SUPPLY

Length: Standard
Height: Double
Width: Single

Price:

$184



Volts	Power mA (max.)	Pins
—15*	250	AB2
GND	ANALOG	AC2

* plus or minus 2 volts

The A704 Reference Supply converts an ordinary —15 volt logic supply voltage into a precisely adjustable regulated —10 volt reference source for A/D and D/A converters of up to 13 binary bits.

FUNCTIONS

Remote Sensing: The input to the regulating circuits of the A704 is connected at sense terminals AT (+) and AV (—). Connection from these points to the load voltage at the most critical location provides maximum regulation at a selected point in a distributed or remote load.

When the sense terminals are connected to the load at a relatively distant location, a capacitor of approximately 100 μF should be connected across the load at the sensing point.

Preloading: The supply may be preloaded to ground or —15 volts to change the amount of current available in either direction. For driving DEC Digital/Analog Converter modules, —125 mA maximum can be obtained by connecting a 270-ohm plus or minus 5%, one-watt resistor from the reference output (pin AE2) to ground (pin AC2).

SPECIFICATIONS

Input Power	−15 V
Use:	See text for sensing and preloading
Output:	−10 V
Current:	−90 to +40 mA
Regulation:	0.1 mV, no load to full load
Temperature Coefficient:	1 mV/8 hrs 1 mV/15 to 35 degrees C 4 mV/0 to 50 degrees C
Peak-to-Peak Ripple:	0.1 mV
Adjustment Resolution:	0.01 mV
Output Impedance:	0.0025 ohms

A811
10-BIT A/D CONVERTER

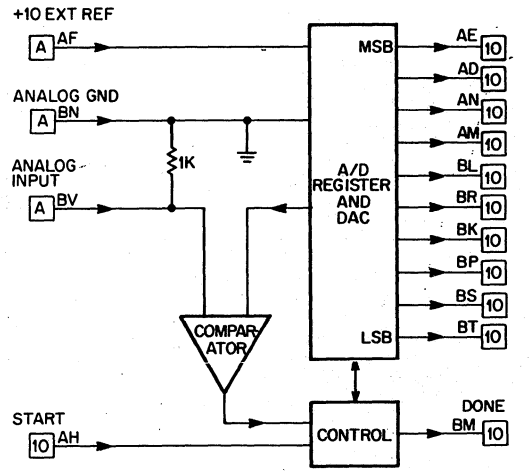
ANALOG TO DIGITAL

A SERIES

Length: Standard
Height: Double
Width: Double (A Section only)

Price:

$350

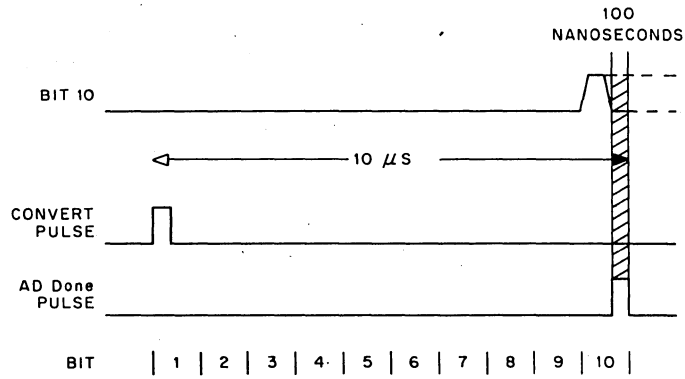


NOTE:
LOGIC AND ANALOG GROUNDS MUST BE TIED TOGETHER AT SOME POINT IN THE SYSTEM.

Volts	Power mA (max.)	Pins
+15*	20	BU2
+5	300	AA2
GND	LOGIC	AC2
GND	ANALOG	BN2
−15*	160	AV2

*Supply voltages must be regulated to within 1%.

The A-811 is a complete, 10-bit successive approximation, analog to digital converter with a built in reference supply. Conversion is initiated by raising the Convert input to logic 1 (+4 volts). The digital result is available at the output within 10 microseconds. An A/D Done Pulse is generated when the result is valid. The A-811 uses monolithic integrated circuits for control logic, output register, and comparator.



Options:
The input impedance of the A/D converter can be raised to greater than 100 megohms by adding an input amplifier module. A sample and hold amplifier module may also be included. The impedance of the converter with sample and hold is 10,000 ohms. Both options may be included simultaneously if high impedance and narrow aperture are both required.

SPECIFICATIONS

	Max.	Min.
Convert Pulse Input:		
Input loading	10 TTL unit load	
Pulse Width	500 nsec	100 nsec
Pulse Rise Time	250 nsec	—
A/D Done Pulse Output:		
Pulse Width	300 nsec	100 nsec
Digital Output:		
Logical "0"	+0.4V	0V
Logical "1"	+3.6V	+2.4V
Output Current "0"	16 mA	
Output Current "1"	−0.4 mA	
Input:		
Input Voltage	0 to +10V	
Input Impedance	1000 ohms	
Resolution:	10 bits	
Accuracy:	0.1% of full scale	
Temperature:		
Coefficient:	0.5 mV/°C	
Operating Temperature:		
	0°C to 50°C	
Conversion Rate:	100 kHz (max)	
Output Format:	Parallel Binary Uni-polar	

A860
12-BIT INDUSTRIAL A/D CONVERTER

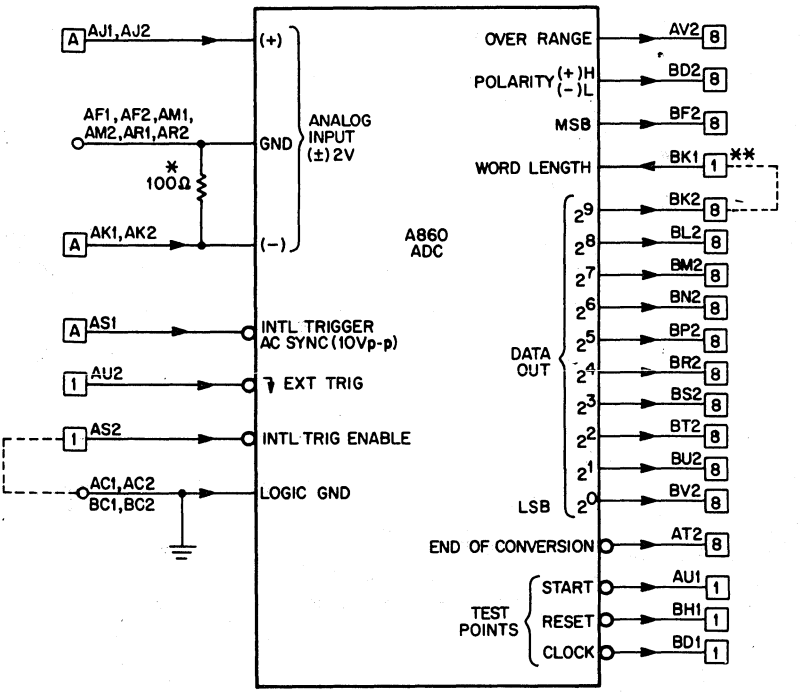
ANALOG TO DIGITAL

A SERIES

Length: Standard
Height: Double
Width: Double

Price:

$200.



* = REMOVE FOR DIFFERENTIAL INPUT
** = MUST BE CONNECTED TO ONE OF THE DATA OUT BITS

Volts	Power mA (max.)	Pins
+15*	20	AD1, AD2
+5	150	BA1, BA2, AA1, AA2
GND	LOGIC	BC1, BC2, AC1, AC2
GND	ANALOG	AF1, AF2, AM1, AM2 AR1, AR2
−15*	20	AE1, AE2

*must be regulated to within 0.3%.

The A860 is a 12-bit (sign + 11-bit magnitude) A/D converter using the dual-slope integrating technique in which the analog input signal is sampled and integrated for a fixed period of time (about 3 ms). The resulting dc level is then quantified by integrating an internal reference voltage and counting the time until the result equals the input sample level. Depending on the magnitude of the sampled analog voltage, this time is 6 ms or less. Since the worst case time for integration and conversion is 9 ms, the maximum useable conversion rate is a little greater than 100 conversions (1200 bits) per second.

APPLICATIONS

The 860 is especially useful in a noisy industrial environment. Integrating the analog voltage effectively reduces medium and high frequency ac noise. The high input impedance of the A860 makes it convenient for applications using analytical instruments, strain gauges, and resistance bridges.

FUNCTIONS

Start of Conversion: Start of conversion can be controlled externally or can be self-starting when the ENABLE INTERNAL TRIG is asserted LOW.

Converted Word Length: The number of bits converted can be controlled by gating or wiring the WORD LENGTH input to an appropriate output bit. (see WORD LENGTH below)

Connection for Differential Input: The (—) input of the differential analog input is connected to ground through a 100-ohm resistor. For a true differential input, remove the resistor but be careful to keep the input common mode voltage to less than + or — 1.25 volts.

INTL TRIG AC SYNC: The internal trigger will sync on the negative peak of a 10-volt peak-to-peak signal applied to this input. The ac input impedance is 2K ohms nominal.

INTL TRIG ENABLE: Must be LOW to enable the internal trigger. Must be HIGH if an external trigger is used.

EXT TRIG: A negative transition on this input resets the converter and starts a new conversion.

WORD LENGTH: When BK1 is connected to BK2, the word length is maximum (11 bits plus sign). Word length and conversion time can be reduced by connecting control input BK1 to a less significant DATA OUT bit. (However, BK1 must be connected to one of the DATA OUT bits.)

Sign Plus Magnitude Coding: The POLARITY bit is HIGH if the analog (+) input voltage is greater than the (—) input voltage.

The OVER RANGE bit is LOW if the magnitude of the analog input voltage is less than 2.0 volts.

The MSB bit is LOW if the magnitude of the analog input voltage is less than 1.0 volt.

The binary magnitude of the analog input voltage is present on the MSB and DATA OUT lines when the END OF CONVERSION signal goes LOW.

END OF CONVERSION: Goes LOW when a conversion is complete. This signal is HIGH during conversion.

SPECIFICATIONS

Accuracy at 23 degrees C:	Error less than ± 0.05% of input voltage ±1 mV
Conversion Time:	Less than 9 ms
Sample Aperture Time:	3 ms max. (part of conversion time)
Analog Input Voltage Range:	+2 V to −2 V
DC Input Impedance:	1000 megohms minimum
Common Mode Rejection:	70 dB min. dc to 60 Hz
Common Mode Voltage Limit:	+1.25 V or −1.25 V (average of both input voltages with respect to analog ground)
Analog Input Voltage Limit:	+2.25 V or −2.25 V (either input with respect to analog ground)
Internal Trigger Rate:	2 per second nominal
AC SYNC Voltage:	10 volts ac ±1 V with allowable dc offset of ±2 V

POWER SUPPLY
Requires ±15V power supply voltages to remain within 1% of 15 volts.

A861
HIGH SPEED 12-BIT UNIPOLAR A/D CONVERTER

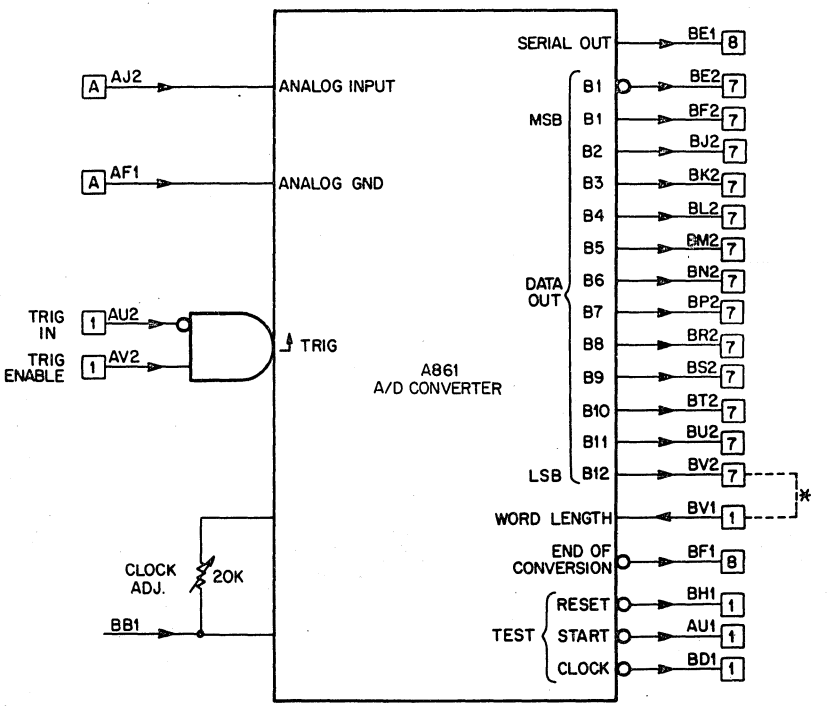
ANALOG TO DIGITAL

A SERIES

Length: Standard
Height: Double
Width: Double

Price:

$300.



*=MUST BE CONNECTED TO ONE OF THE DATA OUT BITS.

Volts	Power mA	Pins
+15	55	AD1, AD2
+5	420	AA2, BA2, AA1, BA1
GND	LOGIC	AC2, BC2, AC1, BC1
GND	ANALOG	AF1, AF2, AK2
−15	12	AE1, AE2

The A861 provides up to 12 bits of adjustment-free analog to digital conversion in the range from 0 to +10 volts. The A861 uses the fast successive approximation technique, is complete with an internal reference voltage, and includes a self-contained adjustable clock that allows control of the conversion time from 12 to 48 microseconds. Analog and digital ground returns are separate to minimize potential ground loop problems. Advanced shielding techniques make the A861 relatively immune to ambient electrostatic and electromagnetic conditions.

APPLICATIONS

- Computer Interfacing
- Biomedical Data Conversion
- Process Control Systems
- Instrumentation Data Conversion

SPECIFICATIONS

Analog Input Voltage Range:	0 to +10 volts
Analog Signal Input Loading:	2.5K returned to +5 volts
Conversion Time:	Adjustable from 12 to 48 μs
Resolution:	12 bits
Accuracy vs Speed @ 23°C:	±0.01% of FS @ 48 μs conversion ±0.015% of FS @ 24 μs conversion ±0.05% of FS @ 12 μs conversion
References:	Internal +5V and +10V (adjustable)
Temperature Coeff. of Offset:	0.001% of FS per degree C
Temperature Coeff. of Gain:	12 ppm per degree C
SERIAL DATA:	NRZ code, available during conversion
DATA OUT:	12 bits of parallel data and the complement of the MSB are available 250 ns after the END OF CONVERSION goes HIGH.
CODE:	Straight Binary
WORD LENGTH:	Must be connected to the DATA OUT bit the user wants to be the LSB
TRIG ENABLE:	A HIGH on this input and a negative transition on the TRIG IN starts the conversion
TRIG IN:	A negative transition on this input and a HIGH on the TRIG ENABLE starts the conversion
Clock Adjust:	Multi-turn pot to control conversion time from 12 μs to 48 μs

A862
HIGH SPEED 12-BIT BIPOLAR A/D CONVERTER

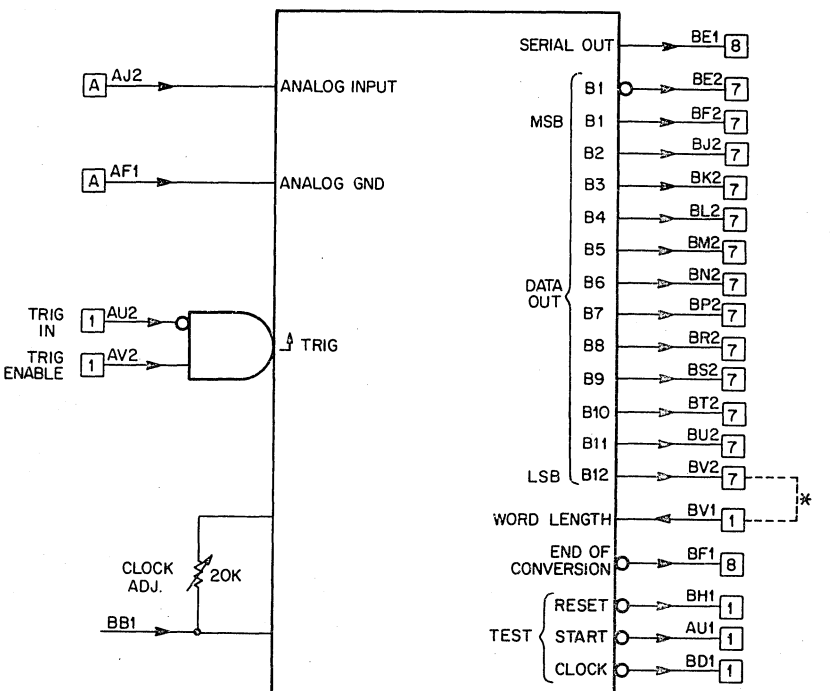
ANALOG TO DIGITAL

A SERIES

Length: Standard
Height: Double
Width: Double

Price:

$300.



*=MUST BE CONNECTED TO ONE OF THE DATA OUT BITS.

Volts	Power mA	Pins
+15	55	AD1, AD2
+5	420	AA2, BA2, AA1, BA1
GND	LOGIC	AC2, BC2, AC1, BC1
GND	ANALOG	AF1, AF2, AK2
−15	12	AE1, AE2

The A862 provides up to 12 bits of adjustment-free analog to digital conversion in the range from −10 to +10 volts. The A862 uses the fast successive approximation technique, is complete with an internal reference voltage, and includes a self-contained adjustable clock that allows control of the conversion time from 12 to 48 microseconds. Analog and digital ground returns are separate to minimize potential ground loop problems. Advanced shielding techniques make the A862 relatively immune to ambient electrostatic and electromagnetic conditions.

APPLICATIONS

- Computer Interfacing
- Biomedical Data Conversion
- Process Control Systems
- Instrumentation Data Conversion

SPECIFICATIONS

Analog Input Voltage Range:	−10 to +10 volts
Analog Signal Input Loading:	5K returned to +5 volts
Conversion Time:	Adjustable from 12 to 48 μs
Resolution:	12 bits
Accuracy vs Speed at 23 degrees C:	±0.01% of FS @ 48 μs conversion ±0.015% of FS @ 24 μs conversion ±0.05% of FS @ 12 μs conversion
References:	Internal +5V and +10V (adjustable)
Temperature Coeff. of Offset:	0.001% of FS per degree C
Temperature Coeff. of Gain:	12 ppm per degree C
SERIAL DATA:	NRZ code, Offset Binary available during conversion
DATA OUT:	12 bits of parallel data and the complement of the MSB are available 250 ns after the END OF CONVERSION goes HIGH.
CODE:	Offset Binary: use the MSB 2's Complement: use the complement of the MSB
WORD LENGTH:	Must be connected to the DATA OUT bit the user wants to be the LSB
TRIG ENABLE:	A HIGH on this input and a negative transition on the TRIG IN starts the conversion
TRIG IN:	A negative transition on this input and a HIGH on the TRIG ENABLE starts the conversion
Clock Adjust:	Multi-turn pot to control conversion time from 12 μs to 48 μs

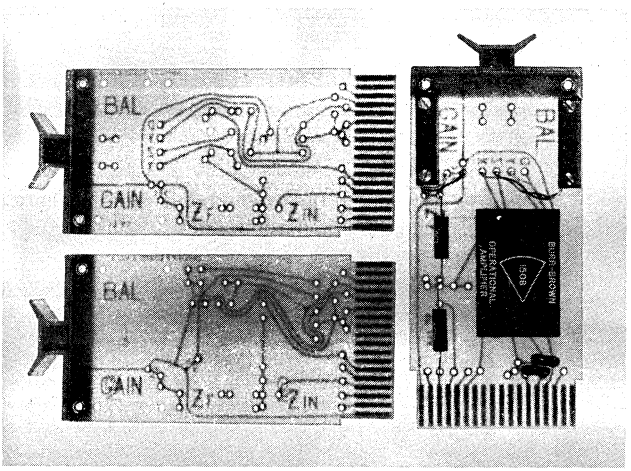
A990, A992
AMPLIFIER BOARDS

AMPLIFIERS

A SERIES

Length: Standard
Height: Single
Width: Double (typ. amp.)

Price:
A990 — $4
A992 — $4



Many types of commercially available operational amplifiers can be mounted in the holes provided on these predrilled etched boards. Mounting holes and printed wires provide for balance trim, gain trim, and feedback networks required to build such common operational devices as voltage followers, inverting or non-inverting amplifiers, integrators, differentiators, summers and subtractors. Most amplifiers listed in the table below require ±15V regulated supplies which are readily available from the amplifier manufacturers. Notable exceptions are Analog Devices' Models 101, 103, and 104 which may be used with standard DEC +10V, −15V supplies at some sacrifice in voltage range (+5, −10V) and noise.

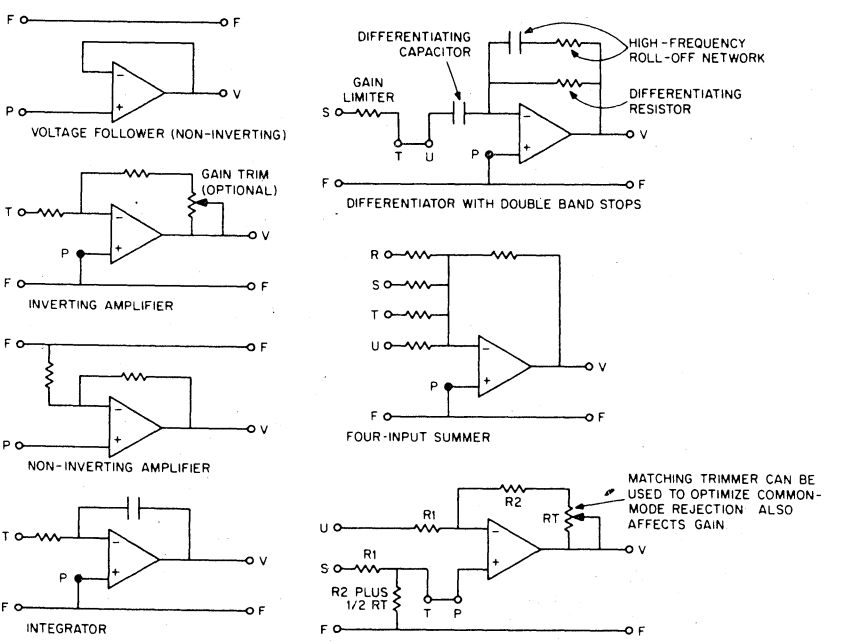
Power: Positive at pin D, negative at pin E, common at pin F for all types. Space is provided for mounting bypass capacitors used with some high frequency amplifiers.

Trimming: Mounting holes on 1" centers at the handle end accept wirewound potentiometers for balance and feedback (gain) trimming. Gain rheostat may be connected in series with feedback components to allow precise adjustment of gain using inexpensive 1% feedback resistors. Board is etched

to allow for use without gain trimming, and one pointed conductor must be cut at caret marks to put a rheostat in the circuit. Gain rheostat stray capacitance to ground is driven by amplifier output.

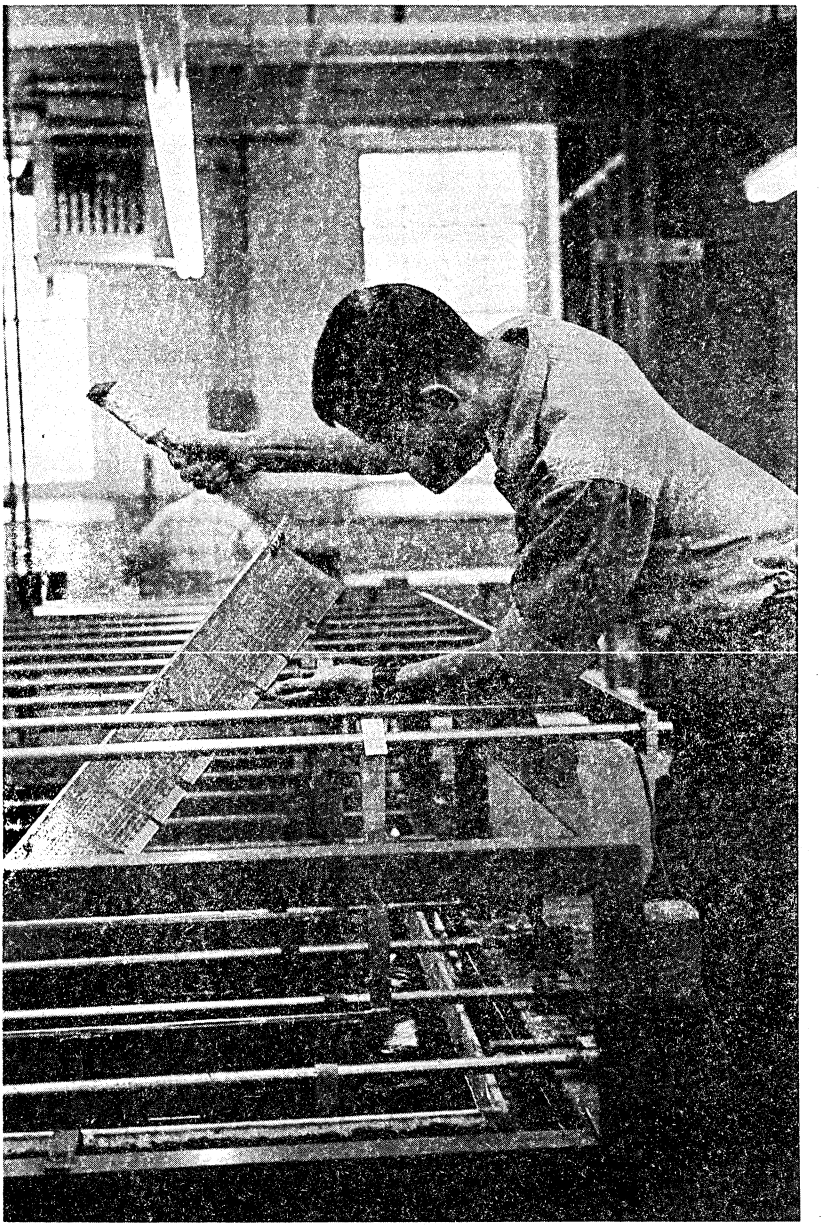
Amplifier Supplier	Types accepted by A990	Types accepted by A992 (boosters too)
Analog Devices	101, 102, 104, etc.	103, 106, 107, etc.
Burr-Brown*	1500-15,15C 1500-25	—
Data Device Corp.	—	most types, except boosters
Nexus	Case K or Case L	Case Q
Philbrick	—	Case PP
Union Carbide	—	most types
Zeltex	—	Case A

*Except Burr-Brown differential output and chopper stabilized types: Perforated board W994 or other blank module may be used to mount non-standard configurations.



accessory modules

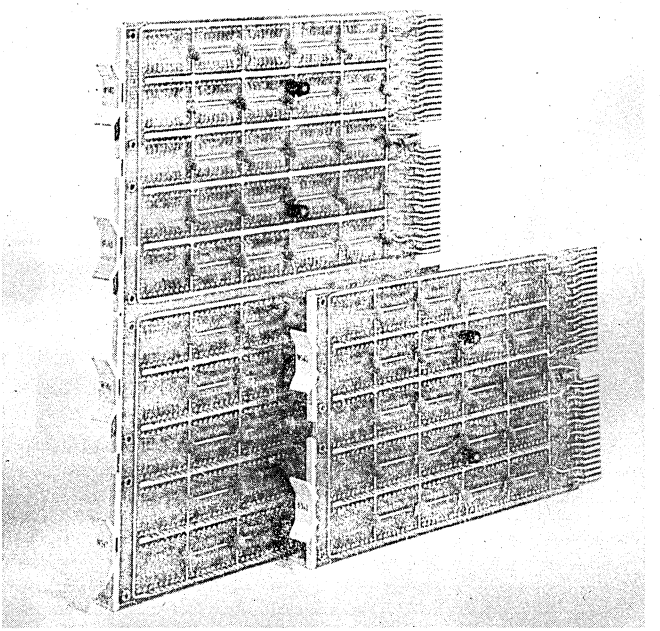
DEC offers a wide line of wire wrappable, collage, and blank modules in the FLIP CHIP form factor for experimenting and breadboarding by users who want to work directly with discrete components and integrated circuit packages. Included in this section are module extenders and PDP-8/e, 8/m OMNIBUS bus connectors.



Checking the appearance of board contacts being gold-plated. Our 100 micro-inch plating is verified by periodic checking on a radiation gauge.

W940-W943, W950-W953 WIRE WRAPPABLE MODULES

ACCESSORY MODULES



W940 W941

These wire wrappable boards with wire wrappable pins will accommodate dual-in line IC's. Two separate leads 30-gauge may be wire wrapped to each pin. All boards have accommodations for 14 and/or 16 pin dual-in line IC's. However, the W950, W951, W952 and W953 boards also have accommodations for 24 pin dual-in-line IC's. Some boards are supplied with low profile IC sockets. The boards are designed to offer customer flexibility by providing additional pin locations for mounting discrete components,such as transistor sockets and potentiometers. These boards offer the user such advantages as easy construction of prototypes and low cost limited production runs. The following table describes each individual module:

MODULES W940, W942
W950, W952

← AA2, BA2, CA2, DA2, —+5

← { AC2, AT1, BC2, BT1 / CC2, CT1, DC2, DT1 } —GND

MODULES W941, W943
W951, W953

← AA2, BA2 —+5

← { AC2, AT1 / BC2, BT1 } —GND

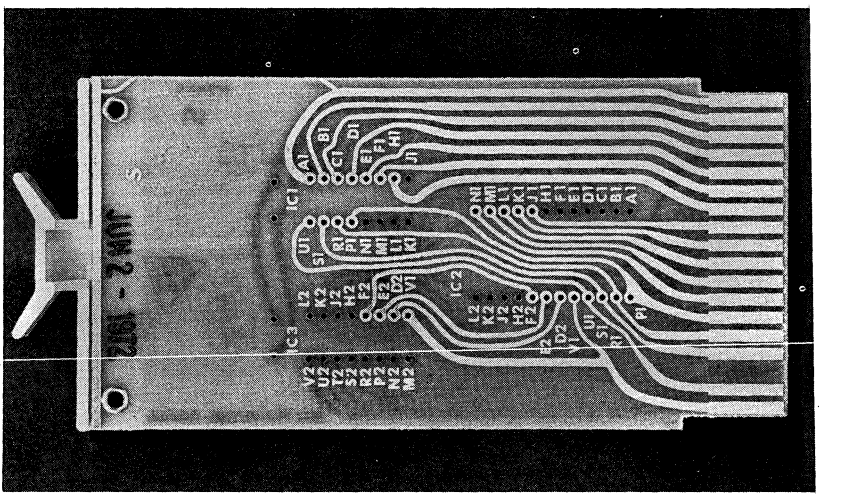
MODULE	CONNECTOR PINS	SIZE	DESCRIPTION	PRICE
W940	144	Entended length Quad height	Accommodates up to 50 14 and/or 16 pin IC's with or without sockets. (sockets not included)	$70.00
W941	72	Entended length Double height	Accommodates up to 25 14 and/or 16 pin IC's with or without sockets. (sockets not included)	$40.00
W942	144	Entended length Quad height	Contains low profile IC sockets. Accommodates up to 50 14 and/or 16 pin IC's	$140.00
W943	72	Entended length Double height	Contains low profile IC sockets. Accommodates up to 25 14 and/or 16 pin IC's	$75.00
W950	144	Entended length Quad height	Has 30 14 and/or 16 pin type accommodations. Also contains 8 24 pin type accommodations that can also accommodate 14 and/or 16 pin IC's. IC's may be mounted with or without sockets (sockets not included).	$65.00
W951	72	Entended length Double height	Has 15 14 and/or 16 pin type accommodations. Also contains 4 24 pin type accommodations that can also accommodate 14 and/or 16 pin IC's. IC's may be mounted with or without sockets (sockets not included).	$40.00
W952	144	Extended length Quad height	Contains 30 16-pin low-profile IC sockets that can accommodate 14-pin or 16-pin IC's. Also contains eight 24-pin low-profile IC sockets that can accommodate 24-pin IC's as well as 14-pin or 16-pin IC's.	$140.00

W953	72	Extended length Double height	Contains 15 16-pin low-profile IC sockets that can accommodate 14-pin or 16-pin IC's. Also contains four 24-pin low-profile IC sockets that can accommodate 24-pin IC's as well as 14-pin or 16-pin IC's.	$75.00

W960
MSI MOUNTING BOARD

ACCESSORY MODULES

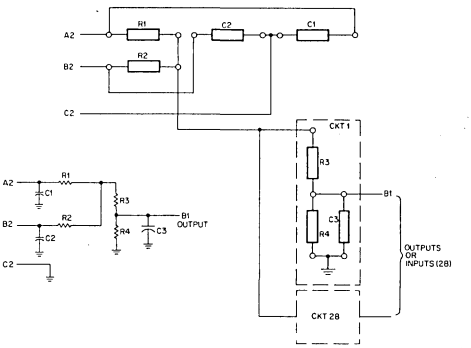
The W960 is a single-height, standard-length, double-sided PC board that can accommodate either two 14 or 16 pin dual-in-line IC's, or one 24 pin dual-in-line IC with or without socket(s). All IC pins are brought out to connector pins.



W960 — $8

W964
UNIVERSAL TERMINATOR BOARD

ACCESSORY MODULES



Typical Circuit Configuration.

The W964 is a blank, etched and drilled module for mounting components which will provide a variety of termination or voltage source circuits for up to 28 signal pins. Each signal pin may have two components connected to ground (pin C2) and one component connected to a common point as shown in the schematic diagram. The potential of the common point is determined by components which connect it to pin A2 and/or pin B2. The schematic diagram shows the physical layout of this section as well as the electrical connections.

Any components can be mounted on the board provided the physical size is similar to a ¼-watt resistor or disk capacitor.

The W964 may be used to terminate single lines, for mounting pull-up resistors, for open-collector devices or to provide various output voltages via voltage-divider networks.

Single height, single width.

Current depends on components used.

Pin assignments:

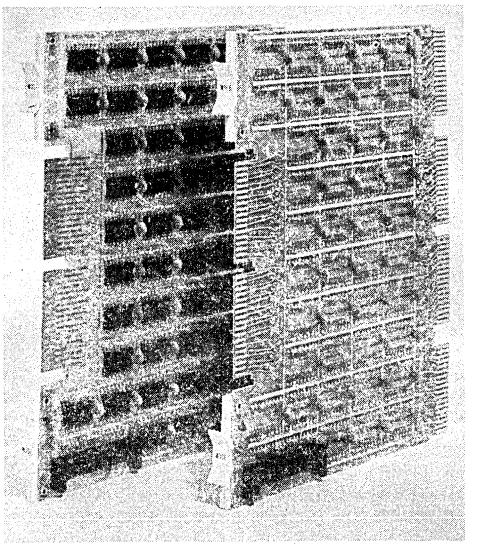
Output/Input (28)	B1, D1, E1, F1, H1, J1, K1, L1, M1, N1, P1, R1, S1 D2, E2, F2, H2, J2, K2, L2, M2, N2, P2, R2, S2, T2, U2, V2
Voltage	A2, B2*
GND	C2

* In many systems, pin B2 is bussed to —15 V dc.

W964 — $8.00

W966, W967
WIRE WRAPPABLE MODULES

ACCESSORY MODULES



W967 W966

The W966 is the 8/e collage mounting board. It is double sided, extended length, and quad height with wire wrappable pins. It will accommodate 14 and/or 16 pin dual-in-line IC's with or without 16 pin sockets. Two separate leads may be wire wrapped to each pin. Up to 42 IC's can be mounted on the W966. Discrete components may be directly soldered onto the board. The top center of the W966 board has 72 terminal fingers with terminating wire wrap pins. An I/O connector (male) terminating in wire wrap pins is mounted on the left side of the W966 board to provide access to the "outside world" when using BC08J-XX cable with a double sided connector board or a BC08K-XX single sided connector board. Both connector boards have 18 conductor lines.

All power and ground lines are common to the 8/E "OMNIBUS".

← AA2, BA2, CA2 —— +5

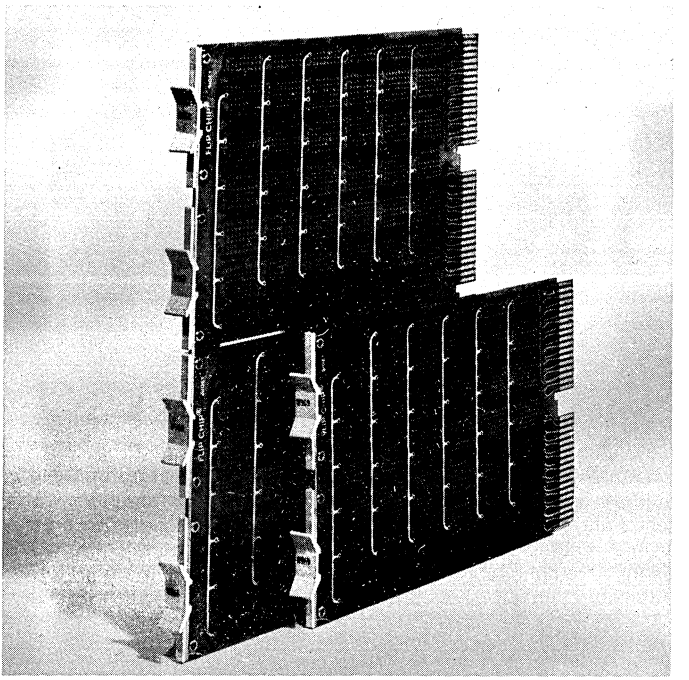
← { AC1, AC2, AF1, AF2, AN1, AN2, AT1, AT2
BC1, BC2, BF1, BF2, BN1, BN2, BT1, BT2
CC1, CC2, CF1, CF2, CN1, CN2, CT1, CT2
DC1, DC2, DF1, DF2, DN1, DN2, DT1, DT2 } —— GND

The W967 is similar in all details to the W966 except that the W967 is supplied with 42 low profile IC sockets.

W966 — $85
W967—$165

W968, W969
COLLAGE MOUNTING BOARDS

ACCESSORY MODULES



W968 W969

The W968 and W969 collage mounting boards will accommodate 14 and/or 16 pin dual-in line IC's with or without 16 pin wire wrap sockets and/or solder sockets. The W968 is a double-sided, quad-height, extended length board and can accommodate up to 72 IC's.

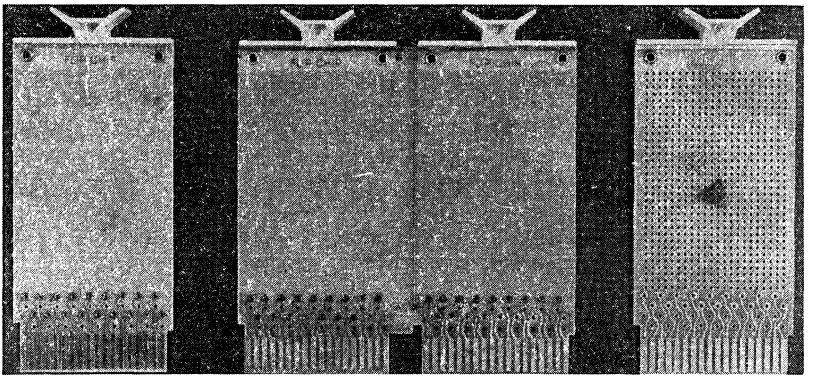
The W969 is the double-height version of the W968 and can accommodate up to 36 IC's. Among the unique uses of the collage boards are that they facilitate construction of prototypes and production of limited runs.

W968	W969
← AA2, BA2, CA2, DA2 —+5	← AA2, BA2 —+5
← { AC2, AT1, BC2, BT1 / CC2, CT1, DC2, DT1 } —GND	← { AC2, AT1 / BC2, BT1 } —GND

W968—$45
W969—$30

W970-W975, W990-W999 BLANK MODULES

ACCESSORY MODULES



W970 W971 W974

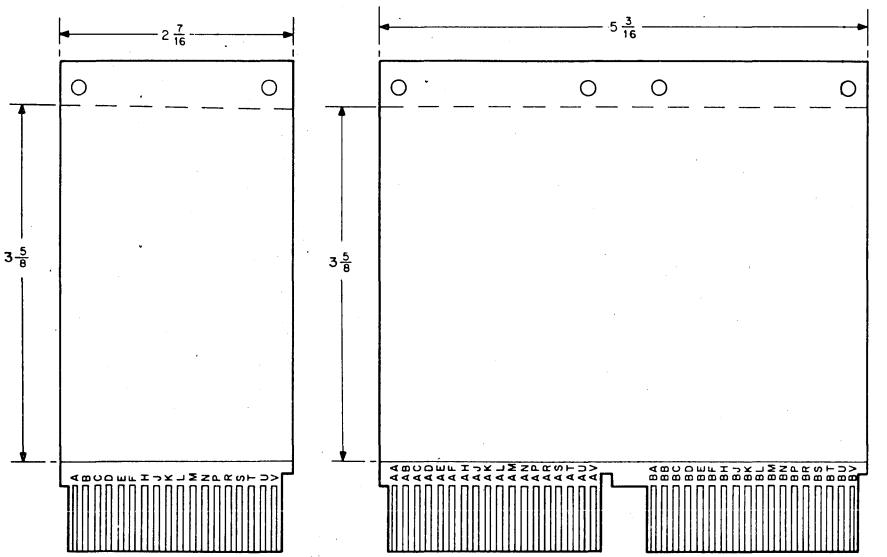
These 10 blank modules offer convenient means of integrating special circuits and even small mechanical components into a FLIP CHIP system, without loss of modularity. Both single- and double-size boards are supplied with contact area etched and gold plated. The W990 Series modules provide connector pins on only one module side for use with H800 connector blocks. W970 series modules have etched contacts on both sides of the module for use with double density connectors Type H803, and low density Type H808.

Module	Connector Pins	Size	Handle	Description	Price
W970	36	Standard length Single height	Attached	Bare board, no split lug terminals.	$ 4.00
W971	72	Standard length Double height	Attached	Bare board, no split lug terminals.	$ 8.00
W972	36	Standard length Single height	Attached	Copper clad, to be etched by user.	$ 4.00
W973	72	Standard length Double height	Attached	Copper clad, to be etched by user.	$ 6.00

Module	Connector Pins	Size	Handle	Description	Price
W974	36	Standard length Single height	Attached	Perforated, 0.052" holes, 36 with etched lands. The holes are on 0.1" centers, both horizontally and vertically. Contact both sides.	$ 9.00
W975	72	Standard length Double height	Attached	Perforated, 0.052" holes, 72 with etched lands. The holes are on 0.1" centers, both horizontally and vertically. Contact both sides.	$18.00
W990	18	Standard length Single height	Attached	Bare board, split lug terminals.	$ 2.00
W991	36	Standard length Double height	Attached	Bare board, split lug terminals.	$ 5.00
W992	18	Standard length Single height	Attached	Copper clad, to be etched by user.	$ 2.00
W993	36	Standard length Double height	Attached	Copper clad, to be etched by user.	$ 4.00
W998	18	Standard length Single height	Attached	Perforated, 0.052" holes, 18 with etched lands. The holes are on 0.1" centers, both horizontally and vertically.	$ 4.00
W999	36	Standard length Double height	Attached	Perforated, 0.052" holes, 36 with etched lands. The holes are on 0.1" centers, both horizontally and vertically.	$ 9.00

W972, W973, W992, W993 BLANK COPPER CLAD MODULES

ACCESSORY MODULES



W992 W993

Type W992 and W993 are single side copper clad boards. The diagrams above indicate the copper clad area that is usable for etching purposes. The identifying numbers are etched from the clad using a minimum of etchable area. Type W972 and W973 are equivalent to the above types but have copper clad on both sides.

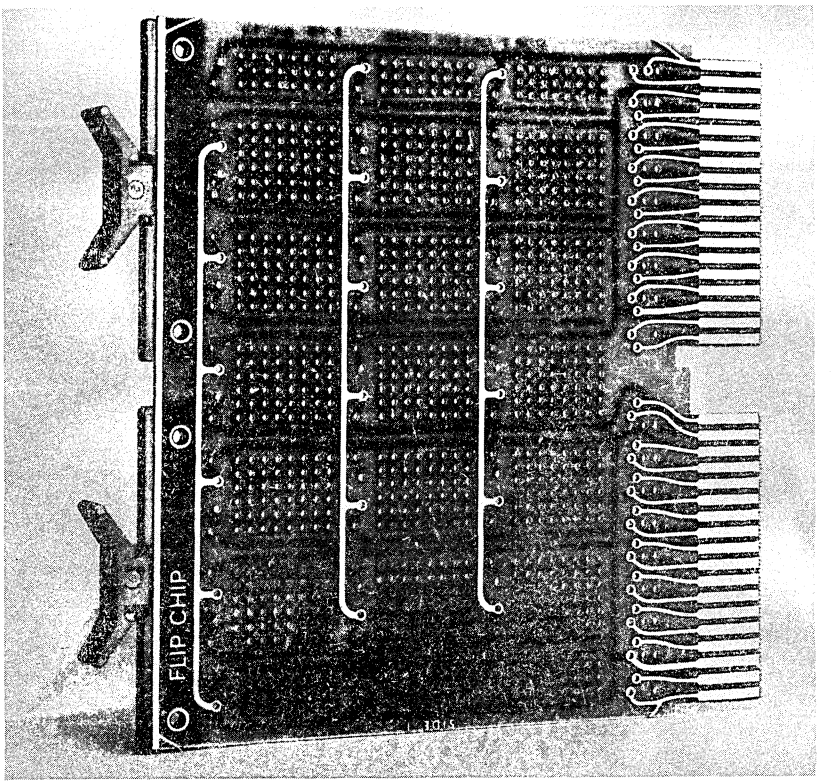
W972 — $4
W973 — $6
W992 — $2
W993 — $4

W979
COLLAGE MOUNTING BOARD

ACCESSORY MODULES

The W979 Collage Mounting Board will accommodate 14 and/or 16 pin dual-in-line IC's with or without 16 pin wire wrap sockets and/or solder sockets.

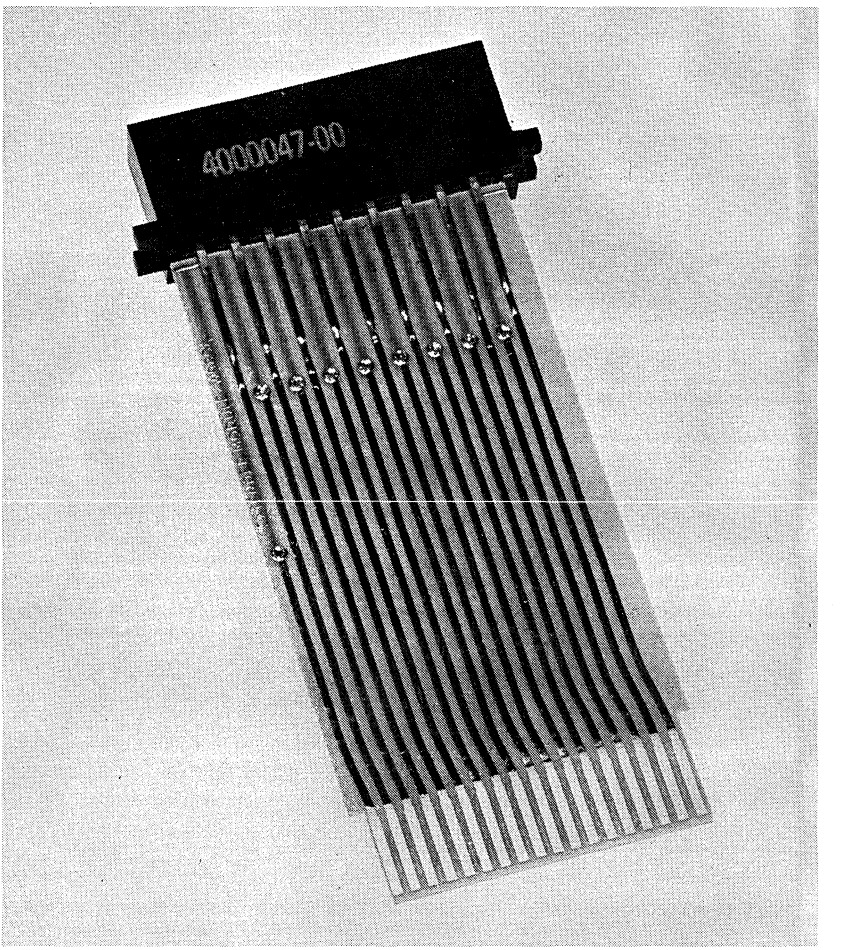
It is the double-height, standard-length version of the W969.



W979 — $20

W980
MODULE EXTENDER

ACCESSORY MODULES



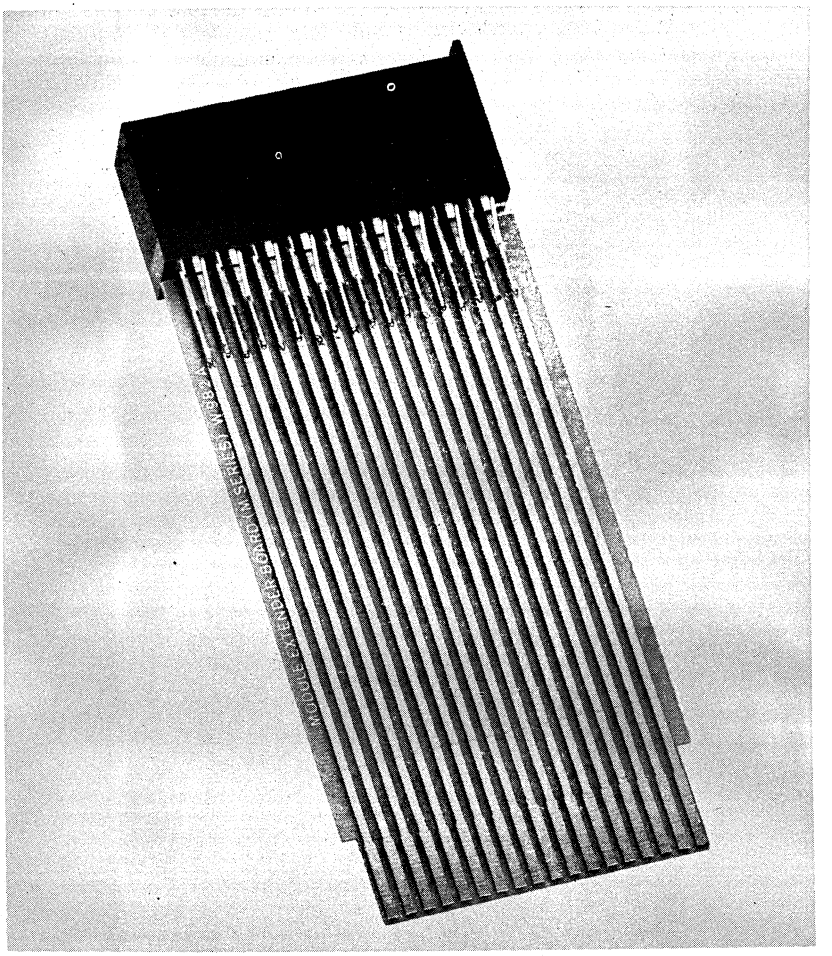
The W980 Module Extender allows access to the module circuits without breaking connections between the module and mounting panel wiring.

For double size flip-chip modules use two W980 extenders side by side. The W980 is for use with A, K and W Series 18 pin modules.

W980 — $14

W982
MODULE EXTENDER

ACCESSORY MODULES

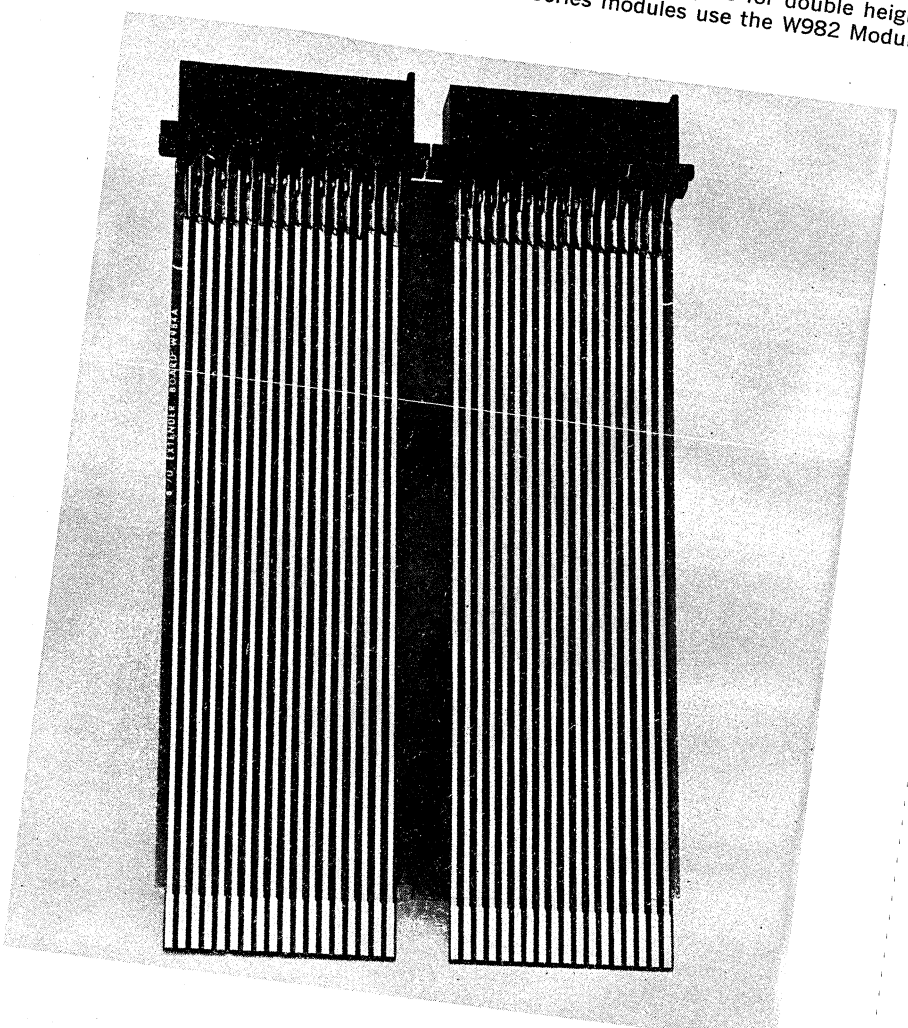


The W982 serves a function similar to the W980 except it contains 36 pins for use with M series modules. The W982 can be used with all modules in this catalog. A, K, and W series modules will make contact with only 2 side pins. A2, B2, etc.

W982 — $18

W984
MODULE EXTENDER

The W984 Module Extender allows access to the module circuits without breaking connections between the module and module panel wiring. It is double height and extended length with 72 connector pins for double height M Series modules. For single height M Series modules use the W982 Module Extender.



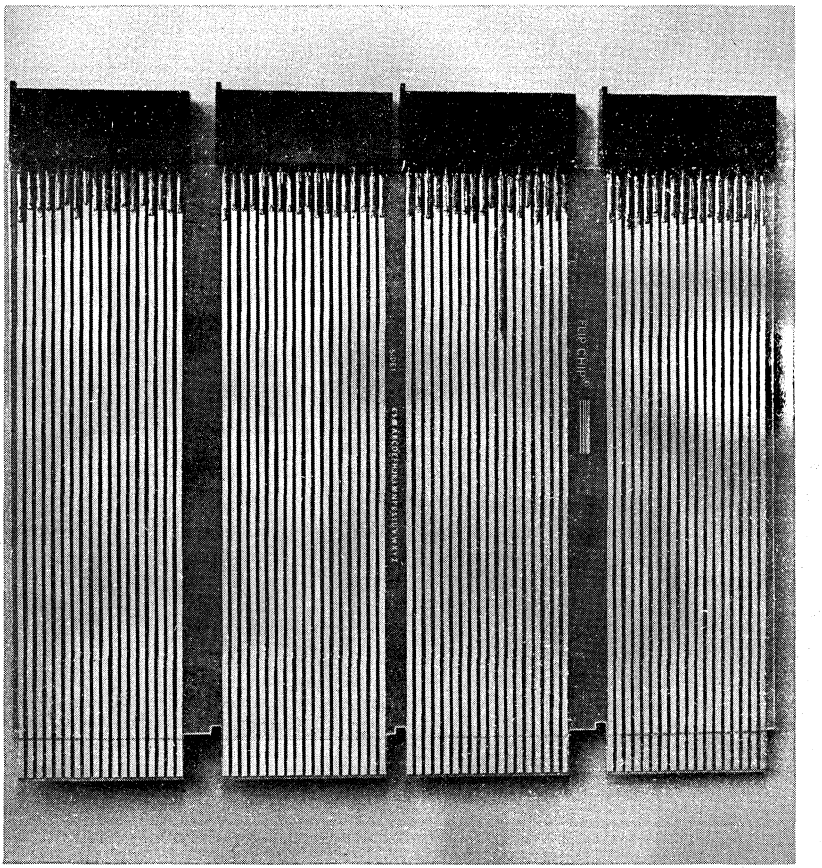
W984—$30

W987
MODULE EXTENDER

ACCESSORY MODULES

Length: Extended
Height: Quad
Width: Single

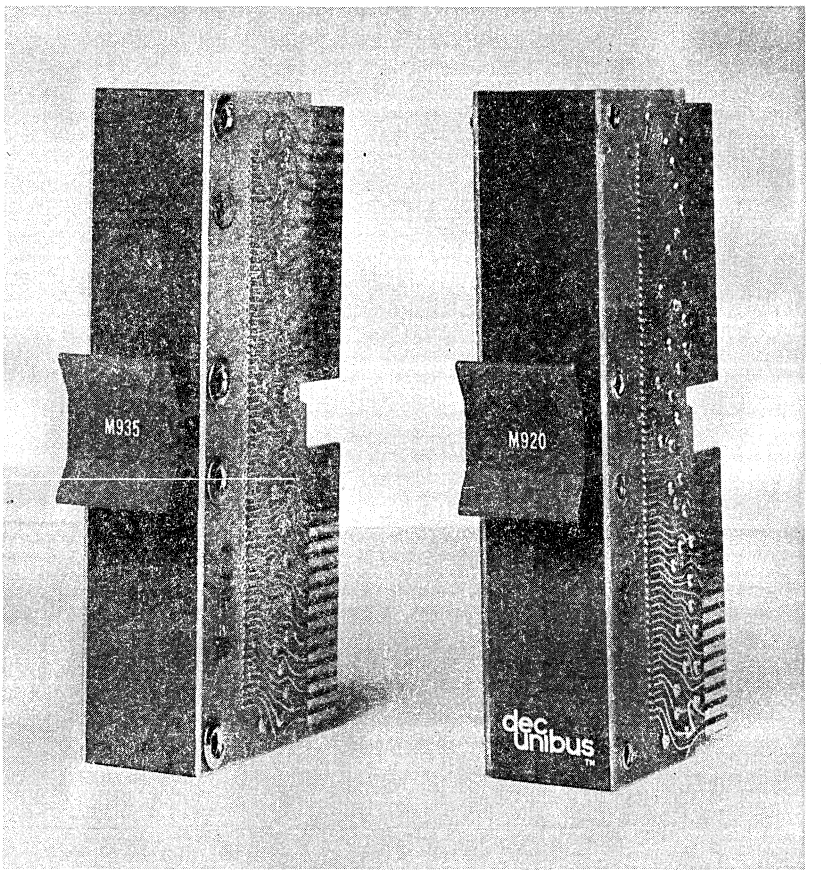
Price
$40



The W987 Module Extender allows access to quad-high modules without breaking the electrical connections between the module and the module panel wiring. It is an extended length, quad-height, single-width module with 144 connector pins for quad-height M Series modules.

M920 AND M935 BUS CONNECTOR MODULES

ACCESSORY MODULES



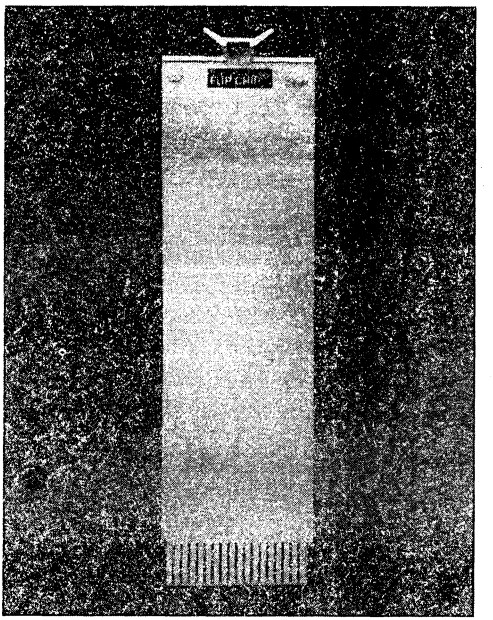
UNIBUS Jumper Module M920—The M920 Module is a double module that connects the UNIBUS from one system unit to the next. The printed circuit cards are on one-inch centers. A single M920 Module carries all 56 UNIBUS signals and 14 grounds.

M935 Bus Connector—used to interconnect 8/e assemblies. The H9190 may be connected to the 8/e OMNIBUS using two M935's.

M920—$45.00
M935—$45.00

W9720, W9721, W9722 BLANK COPPER-CLAD MODULES

ACCESSORY MODULES



These three copper-clad etch boards offer a user the means by which he may etch his own circuits on a board that is compatible with other DEC accessories and systems. All three boards are copper-clad on both sides.

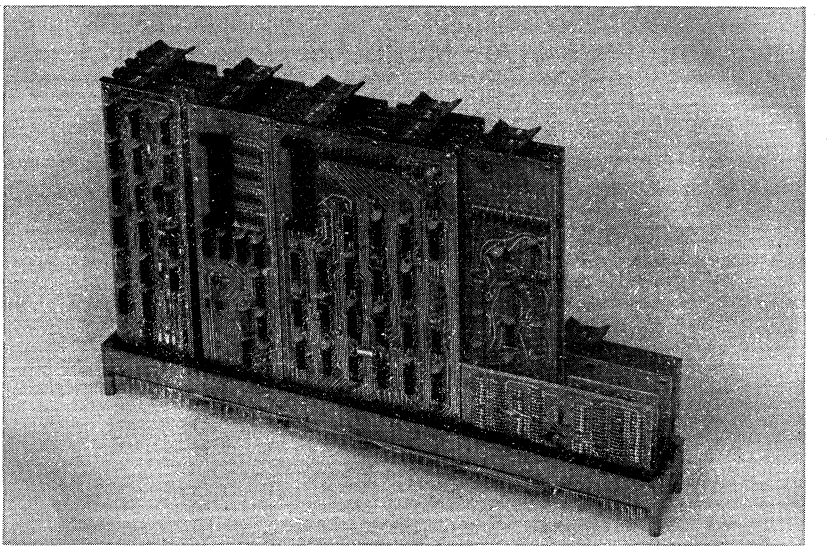
The W9720 is an extended-length, single-height, single-width, double-sided module. The board is comprised of the etch board and one attached handle secured with reusable nylon hardware.

The W9721 is an extended-length, double-height, single-width, double-sided module. The board is comprised of the etch board and two attached handles secured with reusable nylon hardware.

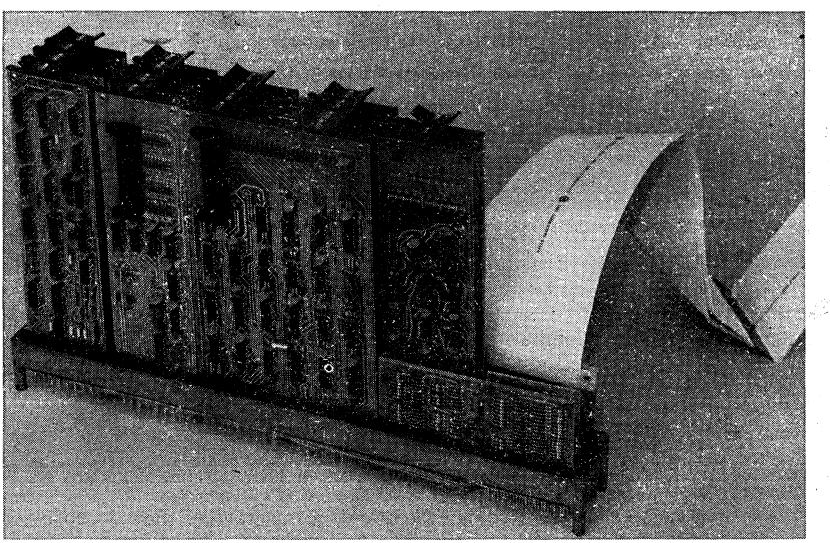
The W9722 is an extended-length, quad-height, single-width, double-sided module. The board is comprised of the etch board and four attached handles secured with reusable nylon hardware.

NOTE: Those wishing to place their own titles on the module may do so by purchasing a 937 which consists of blank gray handles and eyelets.

W9720	$ 6
W9721	$ 8
W9722	$13



Typical DECkit11 with UNIBUS Connector



Typical DECkit11 with UNIBUS cable for remote location

deckits

modular computer interfacing

DECkits

INTRODUCTION

M Series Logic Modules have been developed over a period of time, from a collection of fundamental logic components (gates and flip-flops) to complex MSI- and LSI-implemented logic arrays. In some instances full-scale digital subsystems are available, such as the M1709 OMNIBUS Interface Foundation Module, which allows the user to interface a wide variety of equipment to PDP-8/e, PDP-8/f, and PDP-8/m computers.

In a continuing effort to offer greater interfacing capability for the lowest cost possible, the complex logic module building block concept is being expanded to greater limits of versatility in kit form.

A kit is basically a collection of logic modules assembled by the user to a prewired system unit, capable of performing a highly complex computer interface at low cost to the user.

The three kits described in this section are PDP-11 Input/Output Kits which allow the processor to communicate with a variety of peripheral devices by either receiving and/or transmitting the appropriate number of 16-bit data words via the computer. Provisions are included which will enable computer interrupts to be made at preassigned (hardwired) priority levels.

The kits are defined in full or maximum configuration, i.e., the system unit wiring and the recommended complement of modules define the maximum I/O capability. If the user wishes, a lesser capability may be achieved by removing the appropriate modules and modifying the system unit wiring to his own specifications.

The kits described in the following section are all I/O kits and all are designed to interface with the PDP-11 computer. Added interfacing versatility and design cost-effectiveness will be added in future kits which will

a) interface with the PDP-8/e, PDP-8/f, PDP-8/m computers,

b) offer other interfacing operations in addition to input/output.

GENERAL DESCRIPTION

DECkit11 Series is a set of complete PDP-11 UNIBUS interfaces that are configured with Digital Equipment Corporation parts and assembled by the user. The kits consist of M Series modules, cables, and a prewired backplane (standard systems unit). No additional wiring or design is required by the user for standard configurations. For any other variation, refer to KIT VARIATIONS section.

The UNIBUS interface portion of these kits uses the versatile M1501 Bus Input Interface and the M1502 Bus Output Interface modules. Each of these functional modules transfers 16 bits of data to or from the PDP-11 UNIBUS. The DECkit11 Series combines the versatility of standard interface modules with the simplicity and convenience of a fully engineered package.

These kits enable the PDP-11 processor to communicate with peripheral devices by reading in a particular number of 16-bit data words and/or by sending out a number of 16-bit data words or two 8-bit bytes. Provisions are included in several of the kits to enable computer interrupts to be made at preassigned (hardwired) priority levels.

FEATURES

- Low cost
- Expandable—variable number of I/O channels; several kits may be stacked to make larger arrays
- Complete interface packages that are directly compatible with the PDP-11 UNIBUS
- User-selected register addresses
- Full 16-bit storage for data outputs
- High-voltage, high-current, open-collector data output capability for directly driving cables, instruments, etc.
- Interrupt capability
- Multiple 8-bit byte or 16-bit **output** capability
- Multiple 16-bit word **input** capability
- External input/output connections via convenient connectors
- One I/O cable for every **input** or **output** word
- User-defined variations are possible

KIT VARIATIONS

Other Input/Output applications of fewer 16-bit words may be accomplished, including the determination of different interrupt priorities, by deleting certain modules and by slight modification of the backplane wiring. Kit modification details are contained in the respective kit data sheet. PDP-11 Peripherals and Interfacing Handbook is suggested as source of additional information on the subject of UNIBUS interfacing. For more immediate requirements, design assistance is available from the Logic Products Sales Support Group of Digital Equipment Corporation, who may be contacted through your local DIGITAL Sales Office.

HARDWARE/ACCESSORIES

If mounting space is available in the existing PDP-11 processor mounting box, the DECkit can be installed there and jumpered to the existing panels by a UNIBUS Connector Module, M920. Power is supplied from the processor power supply, or from an additional H720 C or D Power Supply.

If the Interface Kit is installed in a separate mounting rack, the UNIBUS is extended to that rack with a BC11A cable. This cable is available in various standard lengths from 2 ft. to 35 ft.

Input/Output Cables

There are presently two types of cables available for use with the H854 (male) connectors or the M1501 and M1502 modules. They are both fabricated from a 40-conductor flat cable material. They differ only in termination conductors.

Type	Connectors
BC08R-XX[1]	H856 to H856[2]
BC04Z-XX[1]	H856 to open-ended[2]

Notes: 1. XX is length in feet
2. H856 is a female connector

HOW TO ORDER

Fully configured Kits may be ordered by specifying the appropriate Kit letter designation, as follows:

Description	Order
DECkit11-H	Kit11-H
DECkit11-F	Kit11-F
DECkit11-K	Kit11-K

Less than fully configured Kits may be ordered by referring to the individual Interface Kit Data Sheet.

MODULE WARRANTY

Refer to Warranty Section of this Handbook.

SYSTEM UNIT WARRANTY

The BB11 System Unit is warranted against defects in workmanship and material under normal use and service for a period of one year from the date of shipment.

SERVICE

Field Service is available on a time-and-materials basis. For full information, contact your local DIGITAL Field Service office.

INDIVIDUAL KIT DESCRIPTIONS

DECkit11-H

The DECkit11-H, when fully configured, is capable of reading four 16-bit words from a peripheral device into a PDP-11. See Figure 1. It is also capable of writing four 16-bit words, or eight 8-bit bytes, from a PDP-11 to a peripheral device. Each input word is supplied with an interrupt capability to signal the processor that the word should be read. Two interrupts are serviced on level 5 and two on level 6. Figure 2 is a module utilization diagram of a fully configured DECkit11-H.

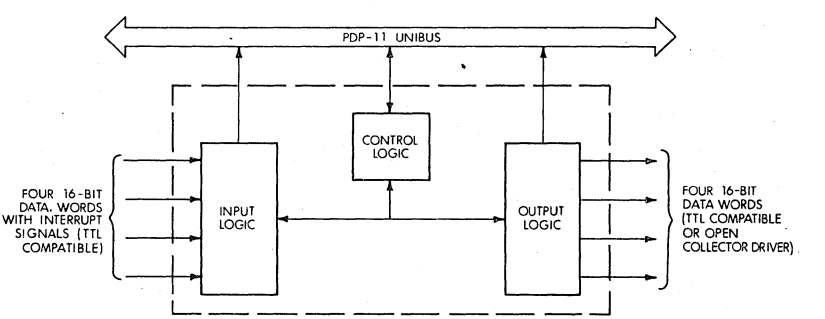
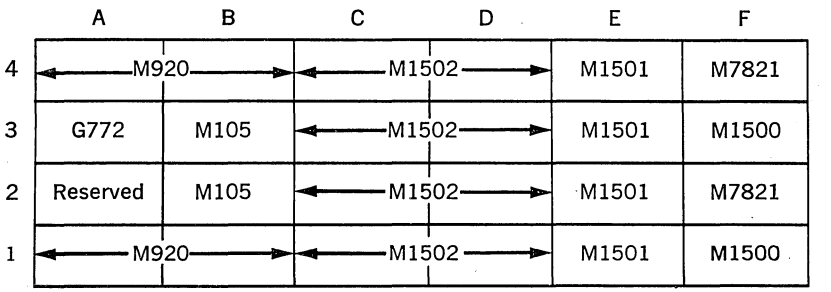


Figure 1. DECkit11-H Functional Block Diagram.



BB11-H (Pin Side Up)

Figure 2. Module Utilization Diagram of a Fully Configured DECkit11-H Backplane.

TABLE I

Parts List DECkit11-H

ITEM	STOCK NO.	DESCRIPTION	MAX. QTY.	UNIT PRICE
1	BB11-H	Pre-wired Backplane for DECkit11-H,	1	$165
2	M105	Address Selector Module	2	65
3	M7821	Interrupt Control—UNIBUS	2	100
4	M1500	Bus Gates Module	2	35
5	M1501	Bus Input Interface Module	4	50
6	M1502	Bus Output Interface Module	4	100
7[1]	M920	Internal Bus Connector	1	45
8[1]	BC11A-XX**	PDP-11 UNIBUS Cable	1	*
9[2]	BC08R-XX**	Cable, H856-H856	8	*
10[2]	BC04Z-X**	Cable, H856—Open End	8	*

Items 1-6 comprise basic kit.
Items 7-10 are required accessories. Refer to notes for appropriate usage.
[1] Order either Item 7 or Item 8, not both.
[2] Order either Item 9 or Item 10, not both.
* Refer to Cable Section of this Handbook.
** XX is length in feet.

DECkit11-F

The DECkit11-F when fully configured is capable of reading three 16-bit words from a peripheral device into a PDP-11. See Figure 3. It is also capable of transferring one 16-bit word, or two 8-bit bytes, from a PDP-11 to a peripheral device. Each word, both input and output, is supplied with an interrupt capability on priority level 7. Figure 4 shows a module utilization diagram of a fully configured kit.

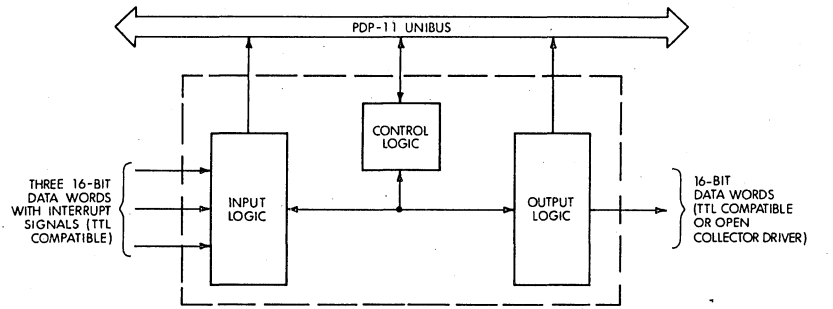


Figure 3. DECkit11-F Functional Block Diagram

	A	B	C	D	E	F
4	← M920 →					M7821
3	G772		See Note 1		M1501	M1500
2	Reserved	M105			M1501	M7821
1	← M920 →		← M1502 →		M1501	M1500

BB11-F (Pin Side Up)

Notes: 1. Shaded slots represent those unused by the Kit. These may be used for additional M, A, W or K Series modules.

Figure 4. Module Utilization Diagram of a Fully Configured DECkit11-F Backplane.

TABLE II

Parts List DECkit11-F

ITEM	STOCK NO.	DESCRIPTION	MAX. QTY.	UNIT PRICE
1	BB11-F	Pre-wired Backplane for DECkit11	1	$165
2	M105	Address Selector Module	1	65
3	M7821	Interrupt Control—UNIBUS	2	100
4	M1500	Bus Gates Module	2	35
5	M1501	Bus Input Interface Module	3	50
6	M1502	Bus Output Interface Module	1	100
7[1]	M920	Internal Bus Connector	1	45
8[1]	BC11A-XX**	PDP-11 UNIBUS Cable	1	*
9[2]	BC08R-XX**	Cable, H856-H856	4	*
10[2]	BC04Z-X**	Cable, H856—Open End	4	*

Items 1-6 comprise basic kit.
Items 7-10 are required accessories. Refer to notes for appropriate usage.
[1] Order either Item 7 or Item 8, not both.
[2] Order either Item 9 or Item 10, not both.
* Refer to Cable Section of this Handbook.
** XX is length in feet.

DECkit11-K

The DECkit11-K when fully configured, is capable of reading eight 16-bit words from a peripheral device into a PDP-11. See Figure 5. It does not have any output or interrupt capability. Figure 6 shows a module utilization diagram of a fully configured kit.

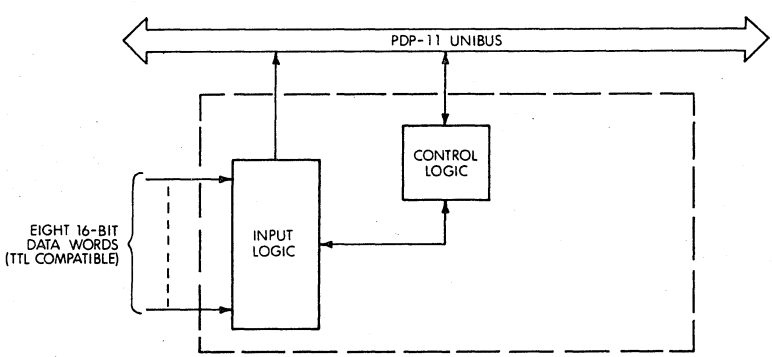
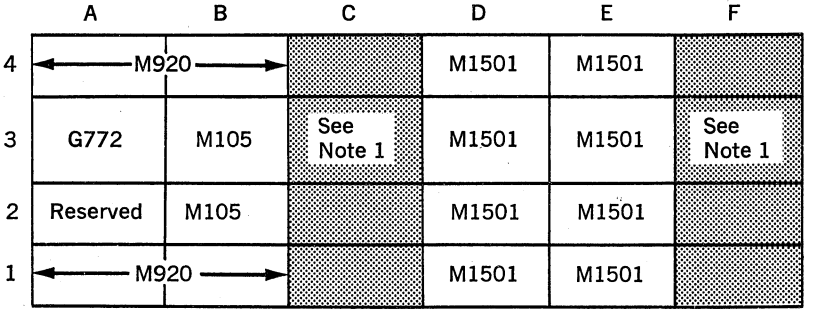


Figure 5. DECkit11-K Functional Block Diagram.



BB11-K (Pin Side Up)

Notes: 1. Shaded slots represent those unused by the Kit. These may be used for additional M, A, W or K Series modules.

Figure 6. Module Utilization Diagram of a Fully Configured DECkit11-K Backplane.

TABLE III

Parts List DECkit11-K

ITEM	STOCK NO.	DESCRIPTION	MAX. QTY.	UNIT PRICE
1	BB11-K	Pre-wired Backplane for DECkit11-K	1	$165
2	M105	Address Selector Module	2	65
3	M1501	Bus Input Interface Module	8	50
4[1]	M920	Internal Bus Connector	1	45
5[1]	BC11A-XX**	PDP-11 UNIBUS Cable	1	*
6[2]	BC08R-XX**	Cable, H856-H856	8	*
7[2]	BC04Z-X**	Cable, H856—Open End	8	*

Items 1-3 comprise basic kit.
Items 4-7 are required accessories. Refer to notes for appropriate usage.
[1] Order either Item 4 or Item 5, not both.
[2] Order either Item 6 or Item 7, not both.
* Refer to Cable Section of this Handbook.
** XX is length in feet.

KIT SELECTION GUIDE

Table IV may be used to determine which fully configured kit will fulfill the user's data transfer requirments.

Table V may be used to determine which fully configured kit will fulfill the user's interrupt requirements. If the selections in Table I and II do not match, there is no kit available for the user's needs.

If the user's requirements are less than a fully configured kit, refer to the Data Sheet for the kit that most closely fulfills the requirements.

Table IV. Data Transfer Needs vs. Kit Number

Number of 16-Bit **INPUT** Words **Required** per Kit.	Number of 16-Bit **OUPUT** Words **Required** Per Kit.				
	0	1	2	3	4
0		11-H 11-F	11-H	11-H	11-H
1	11-H 11-F 11-K	11-H 11-F	11-H	11-H	11-H
2	11-H 11-F 11-K	11-H 11-F	11-H	11-H	11-H
3	11-H 11-F 11-K	11-H 11-F*	11-H	11-H	11-H
4	11-H 11-K	11-H	11-H	11-H	11-H*
5	11-K				
6	11-K				
7	11-K				
8	11-K*				

* Indicates a fully configured kit.

Table V. Interrupt Needs vs. Kit Number

Number of **INTERRUPTS** Associated with **INPUT** Words **Required** per Kit.	Number of **INTERRUPTS** Associated with **OUTPUT** Words **Required** per Kit.	
	0	1
0	11-H 11-F 11-K	11-F
1	11-H 11-F	11-F
2	11-H 11-F	11-F
3	11-H 11-F	11-F*
4	11-H*	

* Indicates a fully configured kit.

power supplies

Power supplies for both large and small systems and reference supplies are available.

Each of the power supplies with a frequency-sensitive regulating transformer is available in a multi-voltage 50-cps version. All 50-cps supplies have the same input connections. The line input is on pins 3 and 4. Jumpers should be connected depending on the input voltage. These connections are shown with a schematic.

POWER SUPPLIES & ACCESSORIES SUMMARY

+5V POWER SUPPLIES (POSITIVE LOGIC USE)

Part No.	Input Specs	Output Specs	Dimensions	Remarks	Price
H710	105-125 Vac 210-250 Vac (47-63 Hz)	5 Vdc @ 5A 1% Regulation	5¼" x 8" x 6"	Short Circuit Proof Floating Output Remote Sensing Over-Voltage Protection Parallel Operation	$180.00
714	120/240 Vac (47-500 Hz)	+5 Vdc @ 7A 1% Regulation	5" x 6" x 6" Flat Surface Mount	Floating Output Short Circuit Proof Parallel Operation Over-Voltage Protection	$200.00
H716	120/240 Vac (47-63 Hz)	+5 Vdc @ 4.0A 3% Regulation −15 Vdc @ 1.5A 5% Regulation	5¼" x 4⅛" x 12¾" Type H021 Mounting Frame	Floating Output Short Circuit Proof Parallel Operation Over-Voltage Protection for +5 Vdc Output	$150.00
H726	120/240 Vac (47-500 Hz)	+5 Vdc @ 7.0A 1% Regulation	16½" x 2¼" x 6½" Panel Mounted	Floating Output Short Circuit Proof Parallel Operation Over-Voltage Protection	$200.00

+10V, −5V SUPPLIES (NEGATIVE LOGIC USE)

Part No.	Input Specs	Output Specs	Dimensions	Characteristics	Price
H701	115V (60Hz)	−15V @ 3A +10V @ 0.4A	Chassis Mounted 8″ x 5″ x 5¾″	Floating Output Parallel Operation	$116.00
H701A	112.5, 123.5, 195, 220, 235V (50Hz)				$136.00
782	Same as H701		Panel Mounted 19″ x 5″ x 5¾″	Same as H701, H701A	$128.00
782A	Same as H701A				$148.00
728	Same as H701	−15V @ 8.5A +10V @ 7.5A	Chassis Mounted 16⅝″ x 8¾″ x 5⅜″	Same as H701, H701A	$240.00
728A	Same as H701A				$260.00
783	Same as H701	Same as 728, 728A	Panel Mounted 19″ x 8¾″ x 5¾″	Same as H701, H701A	$240.00
783A	Same as H701A				$260.00

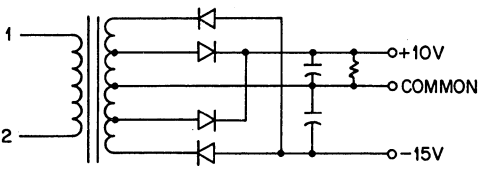
±15V POWER SUPPLIES

Part No.	Input Specs	Output Specs	Dimensions	Remarks	Price
H704	105-125 Vdc (47-420 Hz)	2/±15 Vdc Outputs @ 400 mA .1% Regulation	3⅞" x 5¼" x 6⅞"	2-15V Floating Outputs Overload Protection Remote Sensing Parallel Operation	$200.00
H707	Same as H704	2/±15 Vdc Outputs @ 1.5A .1% Regulation	4" x 5" x 5½"	Same as H704	$400.00

SPECIAL SUPPLIES AND ACCESSORIES

Part No.	Input Specs	Output Specs	Dimensions	Remarks	Price
K731 Source Module	105-130V Line 12.6 Vac Input from Power Transformers K741 or K743	+5 Vdc @ 1.0A 5% Regulation Power for Pin A of K Series Modules	3 Standard Module Widths	Current Capability can be increased using K732 Regulators	$30.00
K732 Slave Regulator	105-130V Line 12.6 Vac Input from Power Transformers K741 or K743	Used with K731 to Regulate Output Current	4 Standard Module Widths	Three K732's Controlled from One K731 Extend Output to +5 Vdc @ 7.0A	$27.00
K741 Power Transformer	120/240 Vac (50 or 60 Hz)	12.6 Vac for K731 or K732 Modules	3½" x 5" (Plate)	Can be mounted using two K943 Mounting Panels	$30.00
K743 Power Transformer	120 Vac (50-60 Hz)	12.4 Vac @ 2.0A 12.6V for K731 or K732 Modules	5" x 5" (Plate)	Can be mounted using two K943 Mounting Panels	$45.00
K771 Display Supply	120 Vac (50-60 Hz)	Provides Power for up to Six K671 Display Tubes	2¾" x 2¾" x 4" without K671 Display Tubes		$35.00

H701, H701A, 782, 782A POWER SUPPLIES + 10, − 15 VOLTS



The 782 and 782A power supplies are ruggedly built, low cost units that fit into a standard 19-inch rack. The H701 and H701A are identical to these units, except they can be mounted on a chassis or panel in applications where space is added to an existing device. The basic supply can be mounted in various configurations and is identical to the power supplies used in models 700D and H900. The Types 782A and H701A are Power Supplies with 50 Hertz transformers. The Types 782 and 701 are 60 Hertz.

ELECTRICAL CHARACTERISTICS

Input Voltage: H701: 115 V 60 cps. H701A: 112.5, 123.5, 195, 220, 235 V, 50 cps. See "50 cps power"

Output Voltage: +10 V, −15 vdc, floating

Output Current: −15V: ½ to 3 amp; +10 V: 0 to 0.4 amp.

Line and Load Regulation: The output voltage remains between −14.5 and −16.5 V for the −15 output, and within +9.2 and +11.5 V for the +10 output, when load varies from minimum to maximum and line voltage varies ±10%.

P-P Ripple: Less than 0.6 V for +10 output. Less than 0.6 V for −15 output; 20% more ripple on the 50-cps type.

Line Frequency Tolerance: ±2% of line frequency.

MECHANICAL CHARACTERISTICS

Height: 5-3/4"

Width: 4-15/16"

Length: 8"

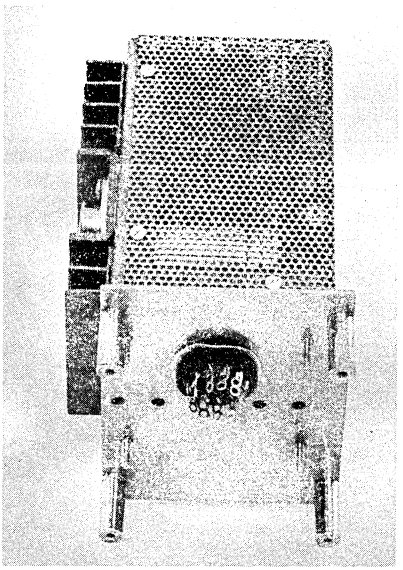
Finish: Chromicoat

Power Connections: Screw terminals are provided on transformer for input power conections. Output power connections are made via tab terminals which fit the AMP "Faston" receptacle series 250, part #41774 or Type 914 power jumpers. All required mounting hardware is supplied with this unit.

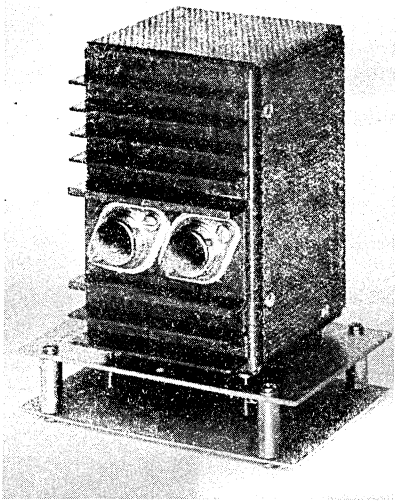
H701	— $116.00	782	— $128.00
H701A	— $136.00	782A	— $148.00

H704, H707
DUAL POWER SUPPLY
15 Volts

POWER SUPPLIES



H704



H707

These supplies differ only in dimensions and output current capabilities: 400 mA and 1.5 Amperes respectively for the H704 and H707. May be mounted on the bars in an H920 drawer, taking the space of two connector blocks.

APPLICATION
D/A and A/D power supply.

MECHANICAL CHARACTERISTICS
DIMENSIONS: 3⅞" x 5¼" x 6⅞" height (H704)
DIMENSIONS: 4" x 5" x 5½" height (H707)
CONNECTIONS: All input-output wires must be soldered to octal socket at the base of the power supply.
OPERATING TEMPERATURE: —20 to +71°C ambient

POWER CONNECTIONS:
Input power connections are made via tab terminals which fit the AMP "Faston" receptacle series. Output power is supplied to solder lugs. All required mounting hardware is supplied with this unit. See 914 power jumpers.

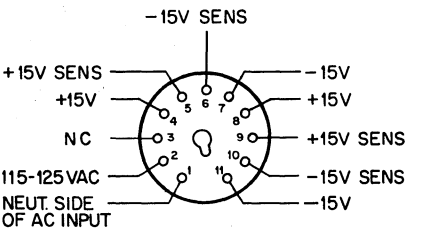
Length: 8″ Height: 6″
Width: 5″ Finish: Chromicoat

ELECTRICAL CHARACTERISTICS

INPUT VOLTAGE: 105 to 125 vac; 47-420 cps.
OUTPUT VOLTAGE: floating 15 V
OUTPUT VOLTAGE ADJUSTMENT: ±1 V each output
REGULATION: 0.05% line, 0.1% load for both voltages
RIPPLE: 1 mv rms max for both outputs
OVERLOAD PROTECTION: The power supply is capable of withstanding output short circuits indefinitely without being damaged.

IF REMOTE SENSING IS NOT USED, CONNECT:

4 TO 5 (+15V OUT)
6 TO 7 TO 8 TO 9 (AC GND)
11 TO 11 (—15V OUT)



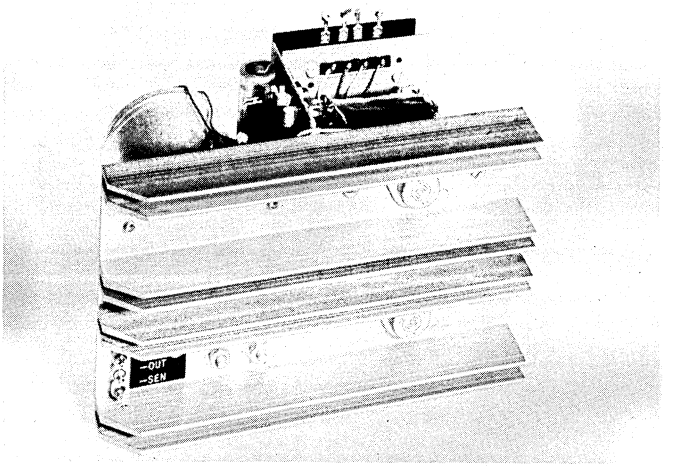
POWER SUPPLY 2

The H704 and H707 contain two 15 Volt floating power supplies. To get ±15 Volt supply, connect pins 7 and 8 and use this point as ground. Pin 4 will now be at positive 15 Volts and pin 11 will be negative 15 Volts.

H704 — $200
H707 — $400

H710
POWER SUPPLY

POWER SUPPLIES



The H710 power supply is ruggedly built, low cost, regulated, floating output, five volt power supply that can be mounted in an H920 chassis drawer or used as a free standing unit. Remote sensing to correct for loss due to long lines is provided. When shipped from the factory, the remote sensing inputs are jumpered to their respective outputs. Especially useful in systems that require maximum repeatability from K303 timers in the millisecond region.

INPUT VOLTAGE: 105-125 VAC or 210-250 VAC 47-63 HZ

OUTPUT VOLTAGE: 5 vdc.

P-P RIPPLE: Less than 20 mv.

OUTPUT CURRENT:
0-5 amps. short-circuit protected for parallel supply operation.

LINE AND LOAD REGULATION:
The output voltage will not vary more than 50 mv over the full range of load current and line voltage.

OVERVOLTAGE PROTECTION:
The output is protected from transients which exceed 6.9 Volts for more than 10 nsec. However, the output is not protected against long shorts to voltages above 6.9 Volts.

POWER CONNECTIONS:
Input power connections are made via tab terminals which fit the AMP "Faston" receptacle series. Output power is supplied to solder lugs. All required mounting hardware is supplied with this unit. See 914 power jumpers.

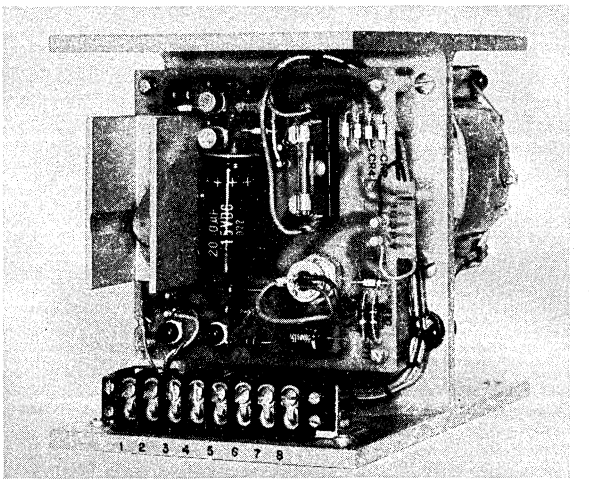
Length: 8"
Width: 5"

Height: 6"
Finish: Chromicoat

H710 — $200

714
POWER SUPPLY

POWER SUPPLIES



The Type 714 power supply provides +5 volts at up to 7 amps with overvoltage protection. This supply is ruggedly constructed on a compact aluminum I-beam chassis suitable for mounting on any flat panel. Electrical characteristics are identical to the H726 power supply but the Type 714 does not include a built-in on-off switch or convenience outlet.

MECHANICAL CHARACTERISTICS

Size: 5" H x 6" W x 6" D. Maximum outside dimension.

Weight: 7 pounds.

Mounting: Four tapped holes, 10-32 thread.

Input/Output Connections: Screw terminals on barrier strips accept as large as No. 16 wire.

ELECTRICAL SPECIFICATIONS

Input: 120/240 V ac, 47 to 500 Hz, normally supplied wired for 120 V ac.

Output: +5 volts with 5 mV rms ripple and noise, max. Line and load regulation combined is ±1% or less.

Temperature Range: −20° C to 71° C.

Dissipation: 80 watts maximum.

714 — $200

H716
POWER SUPPLY

POWER SUPPLIES

Type H716 provides +5 Volts at 4 amperes and —15 Volts at 1.5 amperes with over voltage protection for +5 Volts. This dual voltage power supply is designed to be mounted at the right end of any mounting panel. The supply is mounted by using the four holes in the Type H020. The supply takes 2 connector blocks of Type H800, H803, or H808. This provides 48 module slots with Types H800 and H803, 24 slots with Types H800 and H803 and 24 slots when Type 808 is used.

MECHANICAL CHARACTERISTICS

Maximum Dimensions 5¼" x 4⅛" x 12¾" deep

Power input via Amphenol 160-5 or equivalent connector with an Amphenol 160-5 or equivalent, in parallel.

Low voltage connections are by slip on terminals.

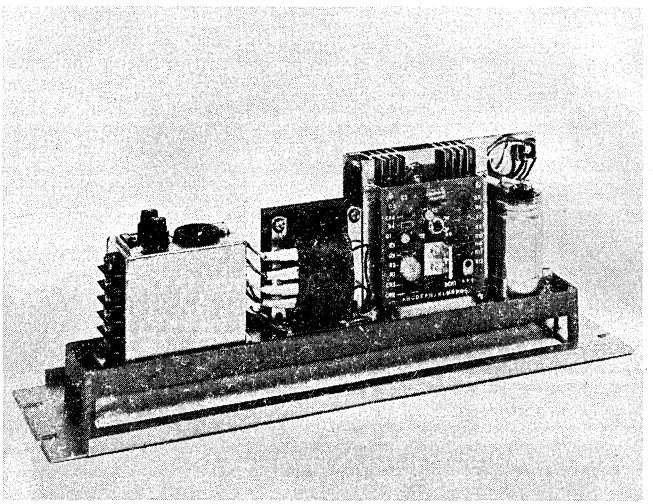
ELECTRICAL SPECIFICATIONS

Input:	120/240 vac ± 10%, 47-63 Hz. Normally supplied wired for 120V. For 240 Volts change transformer tap connections.
Output 1:	+5V, adjustable from 4.5 to 5.5 Volts at 4 amperes maximum. Line-Load-Ripple total regulation ±3%.
Output 2:	—15V ±5% at 1.5 amperes, maximum. Line-Load-Ripple total regulation ±5%.
Temp. Range:	Above specifications are over a range of 0-50°C.

H716 — $150

H726
POWER SUPPLY

POWER SUPPLIES



The H726 power supply provides +5 volts at 7 amps with over-voltage protection. A convenience outlet as well as an off switch for the 5 V supply are supplied; both may be operated in parallel. This power supply is built into a systems unit mounted via the two mounting screws in the systems unit. The H014 mounting plate may be used to mount the supply horizontally in a 19" rack.

MECHANICAL CHARACTERISTICS

Maximum Dimensions: 16.5" x 2.23" x 6.5" deep.

Power Input: Screw terminals on terminal strip.

5 Volt Output: 0.25" Faston connectors on terminal strip.

ELECTRICAL SPECIFICATIONS

Input: 120/240 V ac, 47 to 500 Hz, normally supplied wired for 120 V ac.

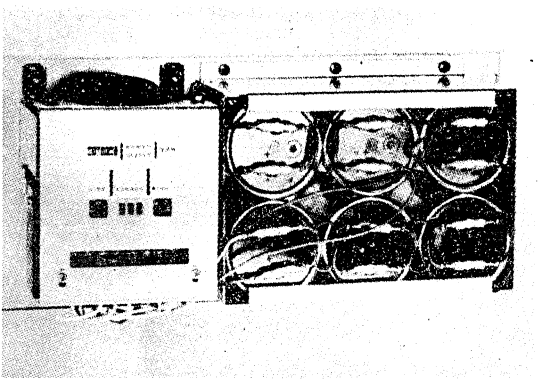
Output: +5 volts with 5 mV rms ripple and noise, max. Line and load regulation combined is ±1% or less.

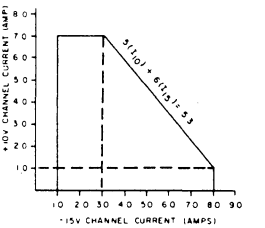
Temperature Range: —20° C to 71° C.

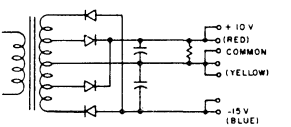
H726 —$200

TYPE 728, 728A POWER SUPPLIES + 10, − 15 VOLTS

POWER SUPPLIES







The Types 728 and 728A (+10, −15 v) Power Supplies are capable of withstanding wide line and load variations for general system use. When used singly, the 10-v channel can supply 0 to 7.5 amp, or the 15-v channel can supply 1.0 to 8.5 amp. The 728 Power Supply is electrically identical to the 783 but is made on a shorter chassis specifically designed for mounting on the plenum door of a DEC computer cabinet.

ELECTRICAL CHARACTERISTICS

INPUT VOLTAGE: 728: 115 v, 60 cps, 728A: 112.5, 123.5, 195, 220, 225 v, 50 cps. See "50 cps power."

OUTPUT VOLTAGE: +10 v, −15 vdc, floating.

OUTPUT CURRENT: 1) When only one output is loaded: +10 v: 0 to 7.5 amp −15 v: 1.0 to 8.5 amp. 2) When both outputs are loaded: +10 v: 0 to 7 amp*, −15 v: 1.0 to 8.0 amp.* At least 1.0 amp must be drawn from the −15 v channel to assure proper load regulation.

LINE AND LOAD REGULATION: The output voltage remains between −14.5 to −16.5 v for the −15 v channel and within +9.5 to +11.5 v for the +10 v channel, when load varies from minimum to maximum and line voltage varies from 105 to 125 vac.

P-P RIPPLE: Less than 0.7 v for +10 v output; less than 0.7 v for − 15 v output (20% more ripple on the 50 cps type).

LINE FREQUENCY TOLERANCE: ±2% of line frequency.

*The sum of the output currents is limited by the following equation: $5(I_{10}) + 6(I_{15}) = 53$ (see Figure).

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 16⅝ in.

PANEL HEIGHT: 8¾ in.

DEPTH: 5⅜ in.

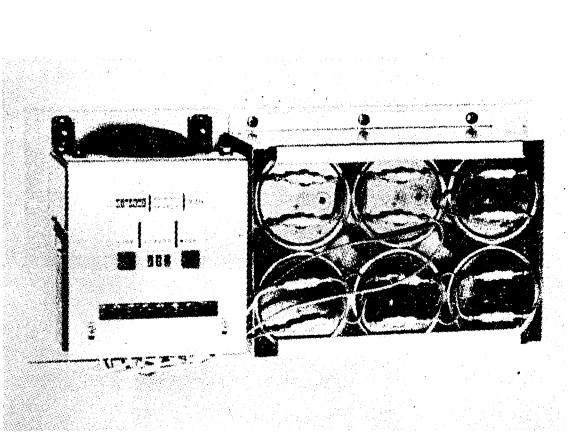
FINISH: Chromicoat.

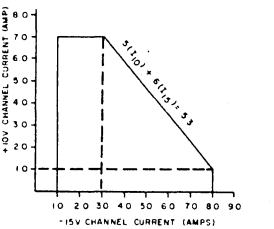
POWER INPUT CONNECTION: Screw terminals on transformer.

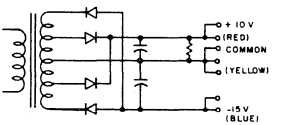
POWER OUTPUT CONNECTION: Heyman tab terminals to fit with AMP "Faston" receptacles series 250, part 41774 or Type 914 power jumpers.

728	— $240.00
728A	— $260.00

TYPE 783, 783A POWER SUPPLIES + 10, − 15 VOLTS







The Type 783 Power Supply (+10, −15 v) is a simple, rugged supply capable of withstanding wide line and load variation for general system use. The graph above shows the permissible region of operation when both outputs are used. When used singly, the 10-v output can supply 0 to 7.5 amp, or the 15-v output can supply 1.0 to 8.5 amp. It is designed for mounting in a standard 19-in. rack. The Type 783A is a 783 Power Supply with a 50-cps transformer.

ELECTRICAL CHARACTERISTICS

INPUT VOLTAGE: 783: 115 v, 60 cps. 783A: 112.5, 123.5, 195, 220, or 235 v, 50 cps. See "50 cps power."

OUTPUT VOLTAGE: +10 v, −15 vdc, floating.

OUTPUT CURRENT: 1) When only one output is loaded: +10 v: 0 to 7.5 amp −15v: 1.0 to 8.5 amp. 2) When both outputs are loaded: +10 v: 0 to 7.0 amp*, −15 v: 1.0 to 8.0 amp*. At least 1.0 amp must be drawn from the −15 v channel to assure proper load regulation.

LINE AND LOAD REGULATION: The output voltage remains between −14.5 and −16.5 v for the −15 v output and within +9.5 and +11.5 v for the +10 v output, when load varies from minimum to maximum and line voltage varies from 105 to 125 vac.

P-P RIPPLE: Less than 0.7 v for +10 v output. Less than 0.5 v for −15 v output. (20% more ripple on the 50-cps type.)

LINE FREQUENCY TOLERANCE: ±2% of line frequency.

*The sum of the output currents is limited by the following equation: $5(I_{10V}) \pm 6(I_{15V}) = 53$.

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19 in.

PANEL HEIGHT: 8¾ in.

DEPTH: 5⅜ in.

FINISH: Chromicoat

POWER INPUT CONNECTION: Screw terminals on transformer.

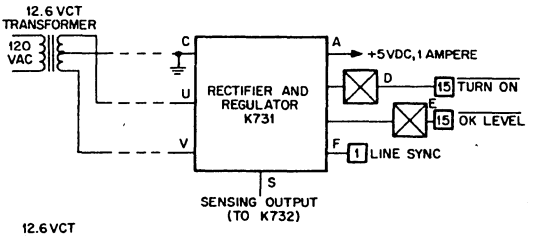
OUTPUT POWER CONNECTION: Heyman tab terminals designed to mate with AMP "Faston" receptacles series 250, part #41774 or Type 914 power jumpers.

783	— $240.00
783A	— $260.00

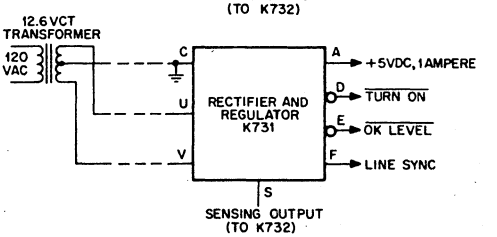
K731 POWER SOURCE MODULE

POWER SUPPLIES

NEMA



MIL



(TRIPLE THICKNESS MODULE)

TRIPLE THICKNESS

The K731 supplies +5 volt DC power to pin A of all K Series modules and provides several specialized once-per-system control functions. Any source of center-tapped 12.6 v (50 or 60 Hz) allows the K731 to deliver up to 1 amp dc, which is sufficient to operate most typical control systems of up to 32 modules. The K731 is short-circuit proof.

This module is normally plugged into one of the innermost sockets on a K941 mounting bar, where its large components occupy space otherwise unused.

The turn-on output goes to ground during the power-up transient, and remains at ground until after the supply voltage has fully reached its quiescent value. It may be used to initialize flip-flops to a known starting condition.

The OK level output goes to ground when the supply voltage reaches 90% of its final value, and returns positive when less than 90% of full voltage is available. It is normally used as an enabling input to the K273 Retentive Memory module.

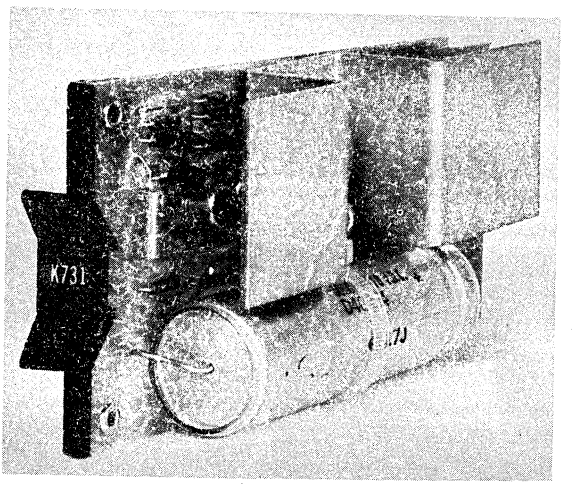
The line sync output allows a K113 or K123 gate to switch in synchronism with ac supply zero-crossings. This permits the line frequency to drive a real-

K731—$30

time clock, or serve as the standard in a phase-locked loop with K303 timers, where higher frequencies must be synchronized with the line. Line sync fan-out is limited to 1 ma (for high fanout, use K113 or K123 for distribution). None of the K731 logic outputs may be used to obtain the OR function, and they may not be wired to any other output.

K731 delivers up to 1 ampere when used with a 12.6 volt tranformer rated for 105-130 volt line. For 5% input voltage reduction (12.0v tranformer or 100 volt line) the output current capability decreases 10%.

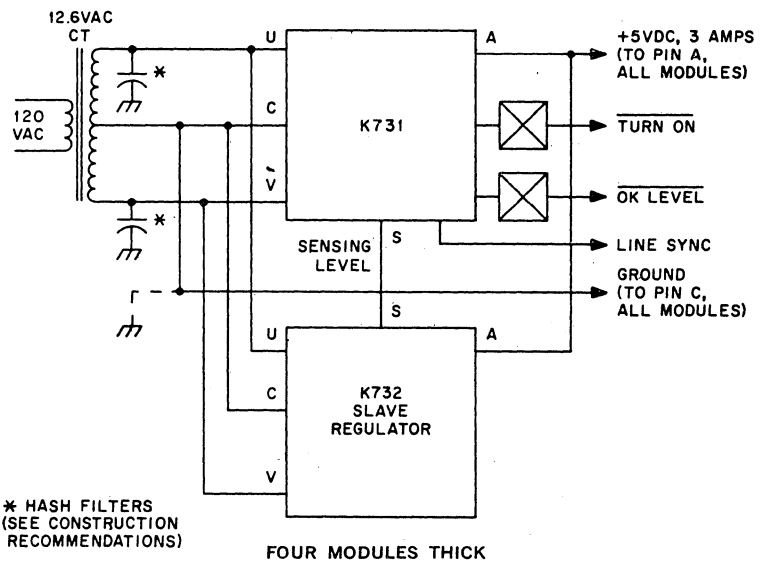
The K731 can also be used with M Series modules provided overvoltage protection is not necessary, since voltage regulation is ±5%.



K732 SLAVE REGULATOR

POWER SUPPLIES

NEMA



FOUR MODULES THICK

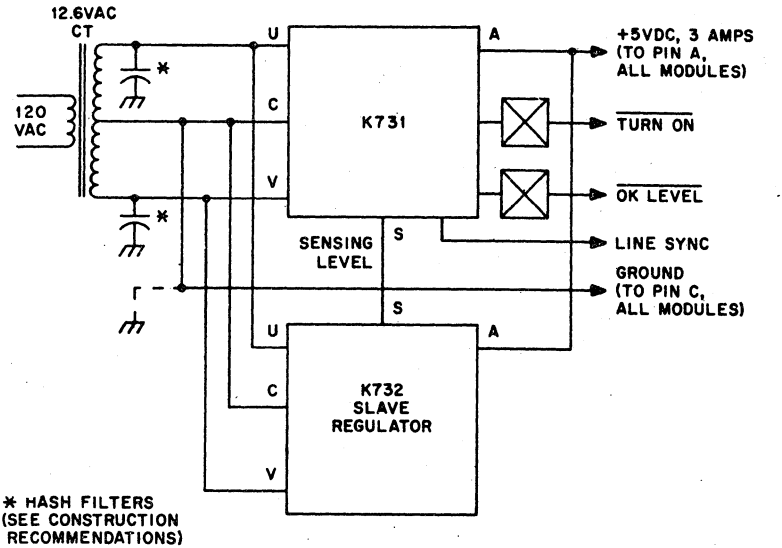
This module is normally tied to corresponding pins A,C,S,U, and V of a K731 Source. For each unit of current emitted by the K731, the K732 emits two. Up to three K732 slaves can be controlled by a single K731 for a total system current of 7 amperes.

In high-current systems, use short heavy wires for transformer secondary connections. Loss of 5% of secondary voltage in either ground return or transformer output leads will reduce regulator current ratings more than 10%.

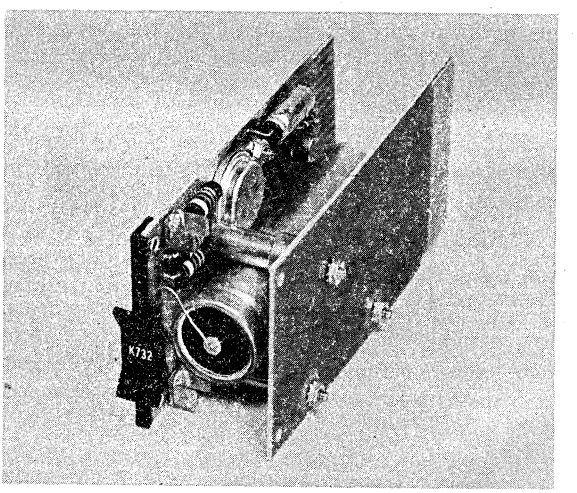
Tabs near the handle end of the K732 may be connected to K741 or K743 transformers by using convenient 914 Power Jumpers. Then by wiring pins U and V to corresponding pins on K731, AC connections are provided through the K732 to the source module. To avoid loss of regulation, do not connect a K732 until enough modules have been plugged in to draw a reasonable current (several hundred milliamperes).

For self contained low-ripple supplies see H710, and H716.

K732—$27



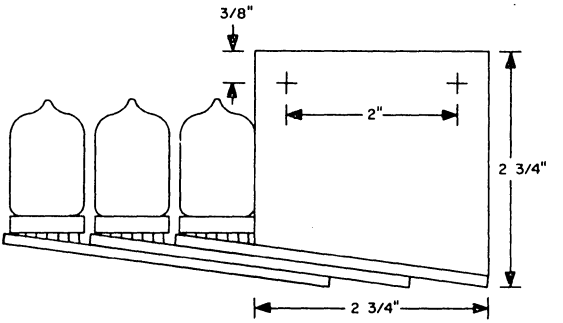
FOUR MODULES THICK



One K731 plus up to 3 K732 can provide from 1 to 7 amperes at +5v.

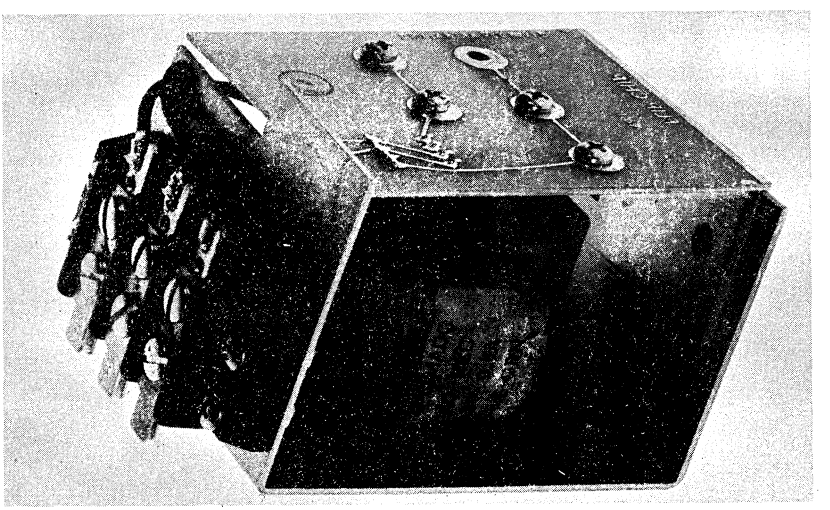
K771
DISPLAY SUPPLY

POWER SUPPLIES



(SHOWN WITH 3 K671'S)

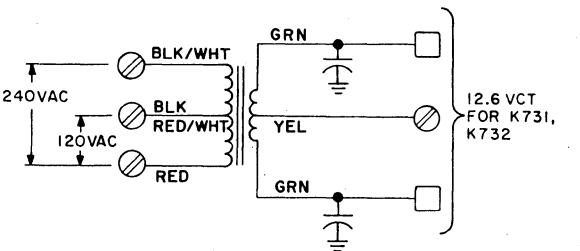
Shown above from the viewing side, the K771 supplies power and a convenient two-screw mounting for up to 6 K671 display tubes. Display tubes are stacked to the left, the first tube board being attached to the K771. The second tube board attaches to the first, and so on. Board mounting screws provide both mechanical mounting and electrical power connections. The two panel mounting screw locations dimensioned above have No. 6 steel threaded inserts. Several 1″ holes using a standard chassis punch may be cut on 0.8″ centers for viewing display tubes. To seal opening against dust, a 3″ by 3-6″ piece of Lucite® or Plexiglas® may be assembled between display and mounting surface. Power 120 VAC enters the supply from a terminal strip at the rear. Total depth behind mounting surface: 4″.



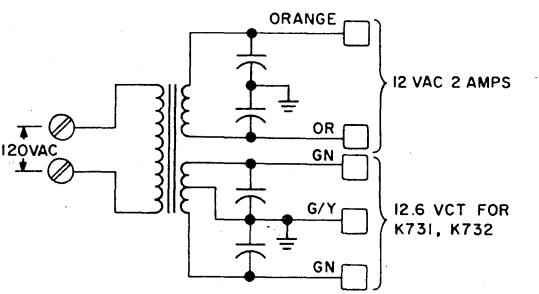
K771 — $35

K741, K743
POWER TRANSFORMERS

POWER SUPPLIES



K741



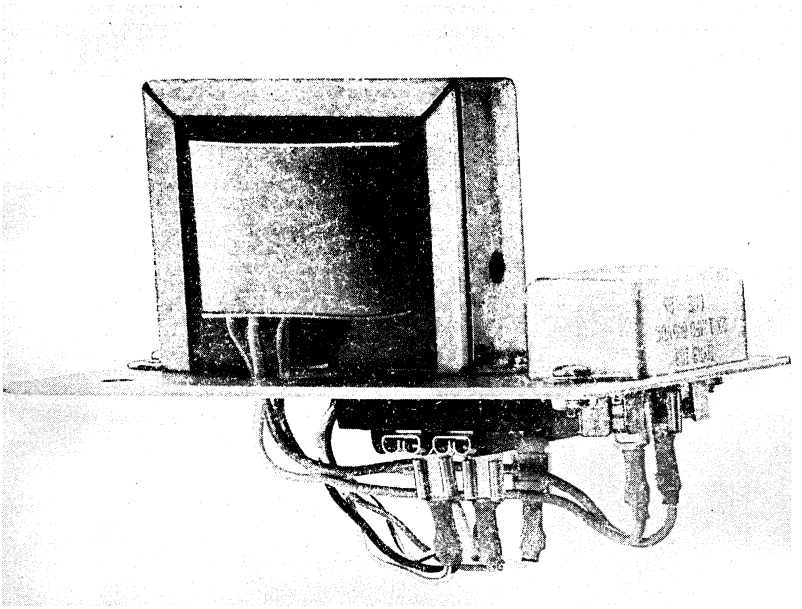
K743

These hash-filtered, 50/60 Hz transformers supply K731 Source and K732 Slave Regulator modules. The K743 also provides an auxiliary winding for use with K580 Dry Contact Filters, K681 or K683 Lamp Drivers (requires additional bridge rectifier, and the K730 Supply and Control Module. Type 914 Power Jumpers are convenient for connecting to tab terminals on these transformers and on the K732 and K943. Both transformers have holes at the corners of the chassis plate for mounting on K980 endplates:

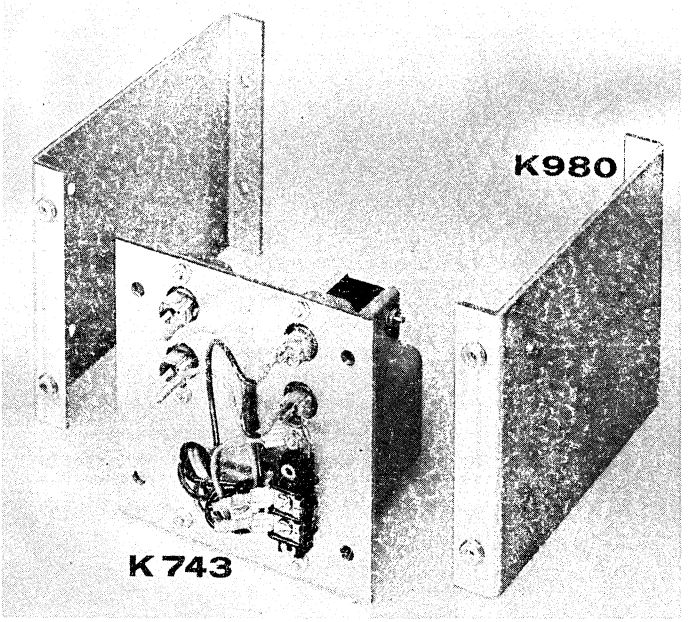
	PLATE DIMENSIONS	HOLE CENTERS	MATCHING K980 Ctrs.
K741	3½" x 5"	2½" x 3⅜"	2½"
K743	5" x 5"	4" x 3⅜"	4"

The K741 is sufficiently light in weight to be mounted on one side only, as at the end of a K943 mounting panel.

K741 — $30
K743 — $45



K741



K743

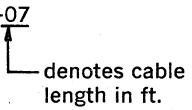
cables and accessories

Digital provides a complete line of pre-assembled cables, cable cards and cable accessories which are compatible with DEC and customer supplied equipments. In addition some cables are available in customer specified lengths for special applications.

Cable Ordering Information
The standard lengths of most of the pre-assembled cables are 3, 5, 7, 10, 15 and 25 feet. Cables listed with an xx designation are available in lengths specified by the customer, however the length must be ordered in increments of feet only.

To determine the cost of special length cables, the price per foot of the type of cable required is added to the basic price of the pre-assembled cable.

Example: BC02L-07 $34.20 Total Cost



1—BC02L-xx	$30.00
7 ft. ribbon at 0.60/ft.*	4.20
	$34.20

*cost/ft x 2 for double cables

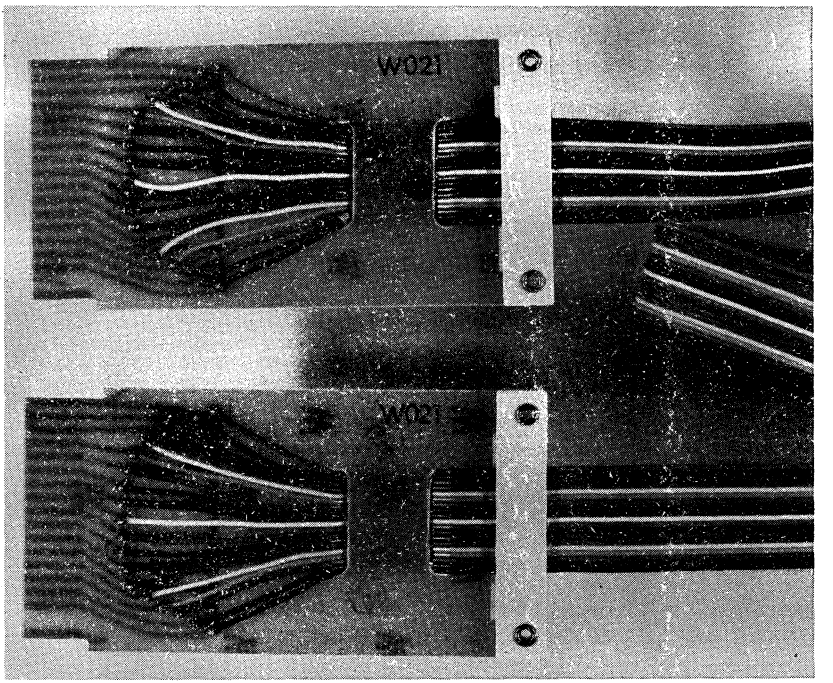
CABLE TYPES AVAILABLE

CABLE TYPE	PART NO.	PRICE/FOOT
20 Conductor Ribbon	91-07575	$ .60
9 Conductor Flat Coax	17-00001	1.00
19 Conductor 1 1/4" Mylar (Flexprint)	17-00002	.75
9 Conductor Round Coax	17-00003	1.50
40 Conductor Flat Cable	91-07722	2.00
36 Twisted Pair Coax	91-07599	2.00

STANDARD CABLES
(SINGLE SIDED CONNECTOR CARDS)

RIBBON CABLES
(20 CONDUCTOR)

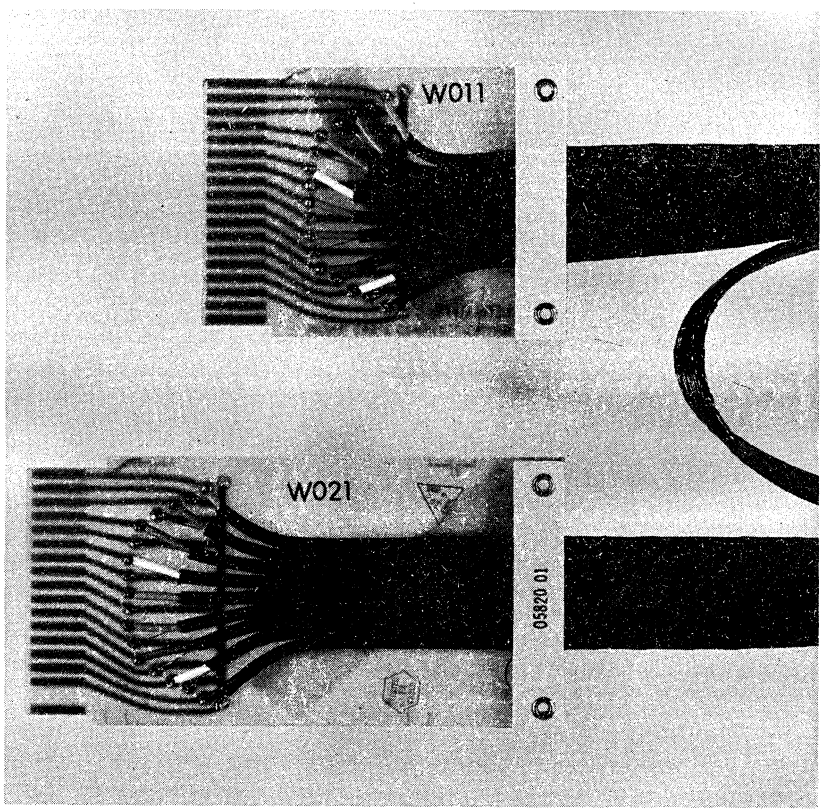
TYPE	CONNECTORS	BASIC PRICE
BC02F-XX	W018-W023	$33.00
BC02L-XX	W021-W021	30.00
BC02M-XX	W021-W022	30.00
BC02P-XX	W022-W022	30.00
BC02S-XX	W023-W023	30.00
BC02W-XX	W028-W028	30.00
BC02Y-XX	W011-W021	31.00
BC04A-XX	W011-OPEN END	15.00
BC04B-XX	W018-OPEN END	18.00
BC04F-XX	W023-OPEN END	15.00



CABLE TYPE BC02L

FLAT COAX CABLES
(9 CONDUCTOR)

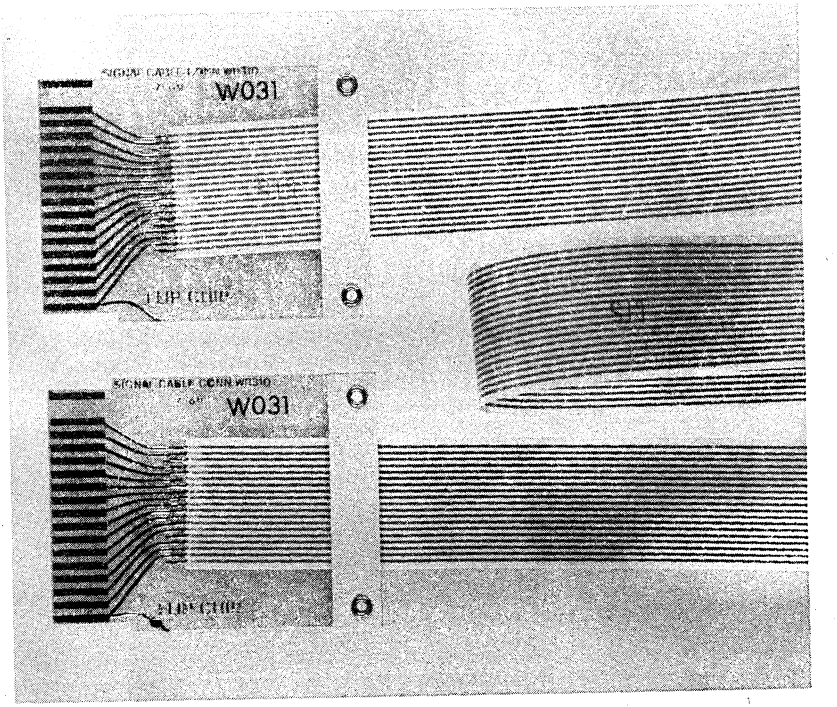
TYPE	CONNECTORS	BASIC PRICE
BC03A-XX	W011-W011	$38.00
BC03B-XX	W011-W021	37.00
BC03C-XX	W021-W021	36.00
BC03D-XX	W021-W022	36.00
BC03J-XX	W028-W021	36.00
BC04L-XX	W011-OPEN END	18.00
BC04M-XX	W021-OPEN END	18.00
BC04N-XX	W022-OPEN END	18.00



CABLE TYPE BC03B

FLAT MYLAR CABLES
(19 CONDUCTOR)

DESIGNATION	CONNECTORS	BASIC PRICE
BC03E-XX	W031-W031	29.00
BC03F-XX	W033-W033	28.00



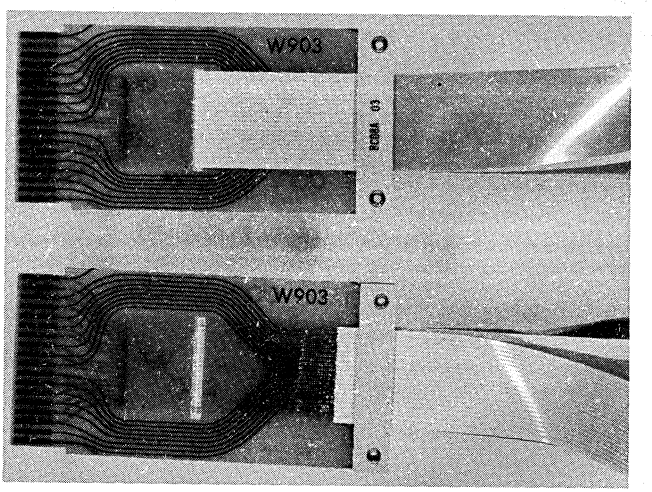
CABLE TYPE BC03E

STANDARD CABLES
(DOUBLE SIDED CONNECTOR CARDS)

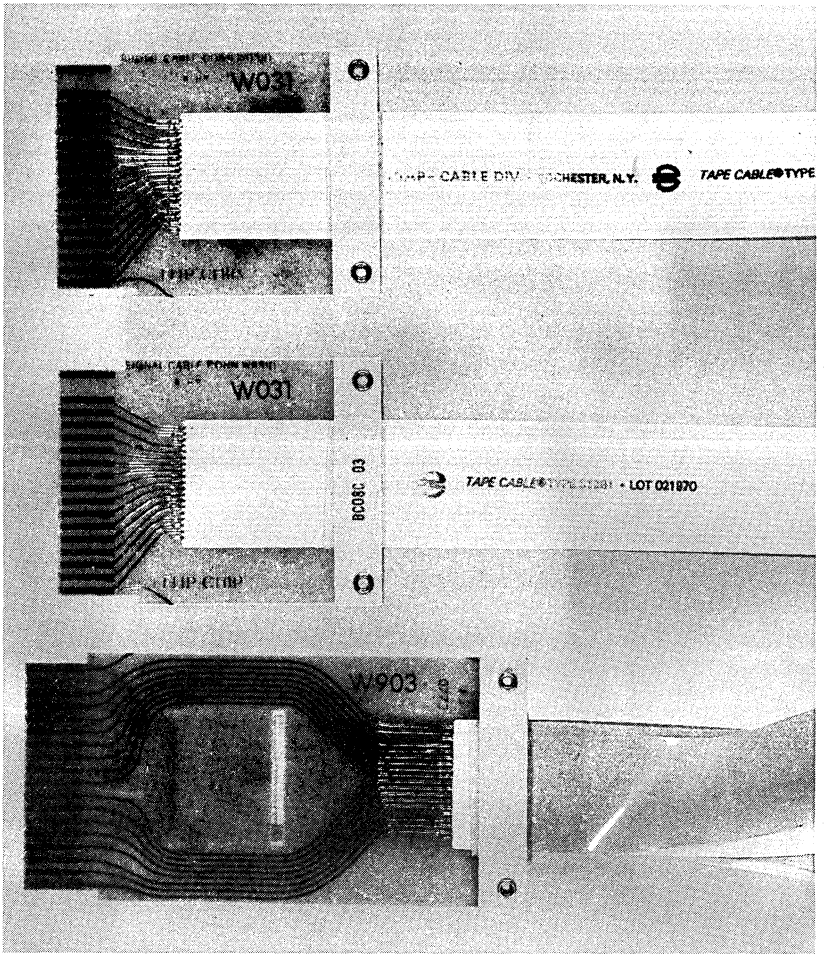
All M Series cables connector cards are double sided and attached to double cables unless otherwise noted.

FLAT MYLAR CABLES
(19 CONDUCTOR—1 1/4")

TYPE	CONNECTORS	PRICE
BC03H-XX	M901-M901	$54.00
BC04T-XX	M901-OPEN END	27.00
BC04U-XX	M903-OPEN END	22.00
BC08A-01	M903-M903	45.00
BC08A-03	M903-M903	48.00
BC08A-05	M903-M903	51.00
BC08A-07	M903-M903	54.00
BC08A-10	M903-M903	59.00
BC08A-15	M903-M903	66.00
BC08A-25	M903-M903	81.00
BC08C-01	M903-2/W031	46.00
BC08C-03	M903-2/W031	49.00
BC08C-05	M903-2/W031	52.00
BC08C-07	M903-2/W031	55.00
BC08C-10	M903-2/W031	60.00
BC08C-15	M903-2/W031	67.00
BC08C-25	M903-2/W031	82.00



CABLE TYPE BC08A



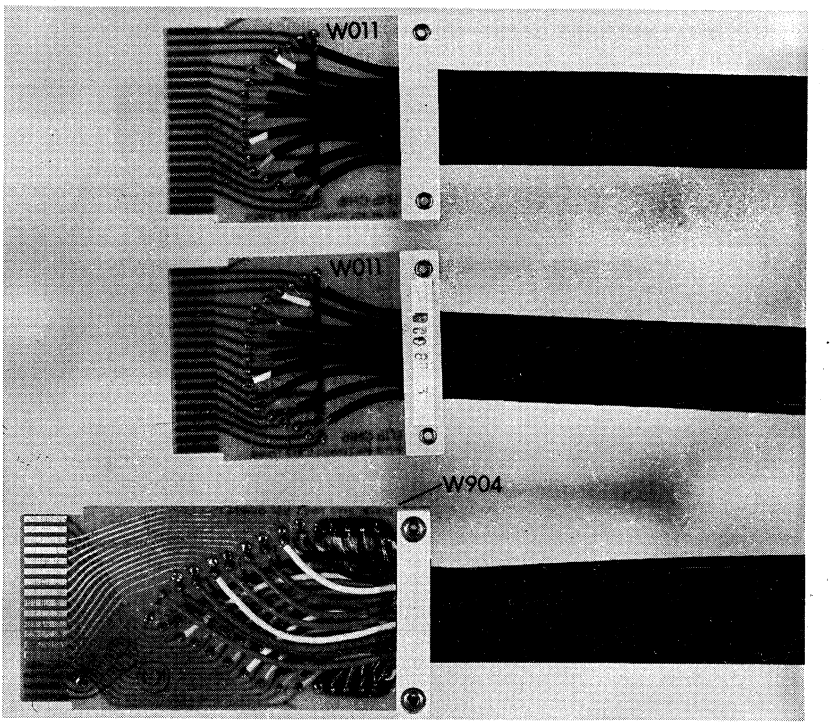
CABLE TYPE BC08C

RIBBON CABLE
(20 CONDUCTOR—DOUBLE)

TYPE	CONNECTORS	BASIC PRICE
BC02X-XX	M908-M908	$58.00
BC04W-XX	M908-OPEN END	28.00

FLAT COAX CABLES
(19 CONDUCTORS—DOUBLE)

TYPE	CONNECTORS	PRICE
BC04P-XX	M904-OPEN END	$ 34.00
BC08B-01	M904-M904	$ 70.00
BC08B-03	M904-M904	74.00
BC08B-05	M904-M904	78.00
BC08B-07	M904-M904	82.00
BC08B-10	M904-M904	88.00
BC08B-15	M904-M904	98.00
BC08B-25	M904-M904	118.00
BC08D-01	M904-2/W011	74.00
BC08D-03	M904-2/W011	78.00
BC08D-05	M904-2/W011	82.00
BC08D-07	M904-2/W011	86.00
BC08D-10	M904-2/W011	92.00
BC08D-15	M904-2/W011	102.00
BC08D-25	M904-2/W011	122.00

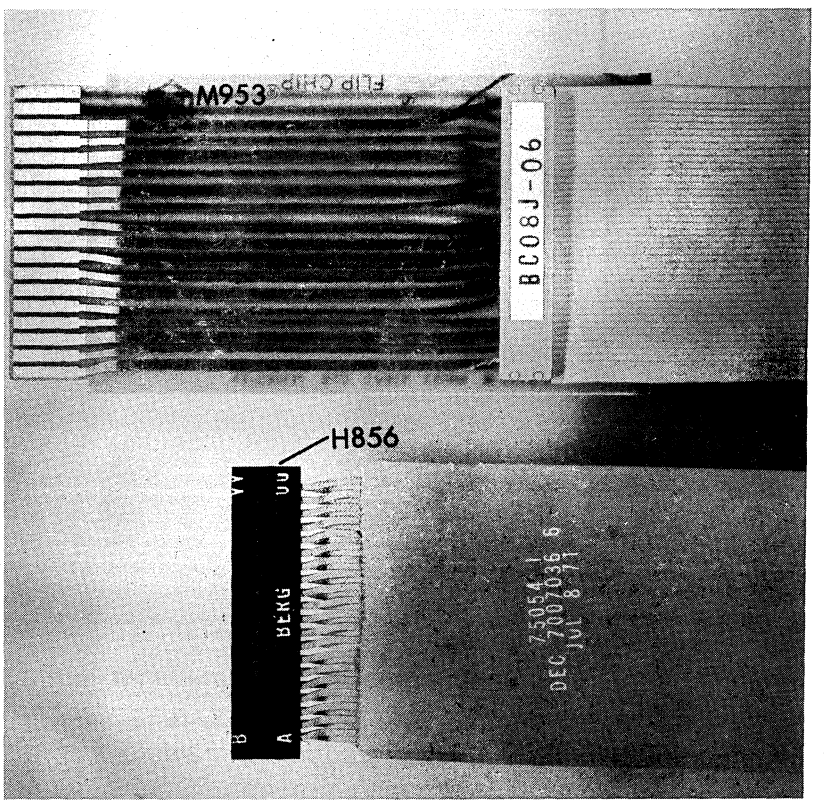


CABLE TYPE BC08D

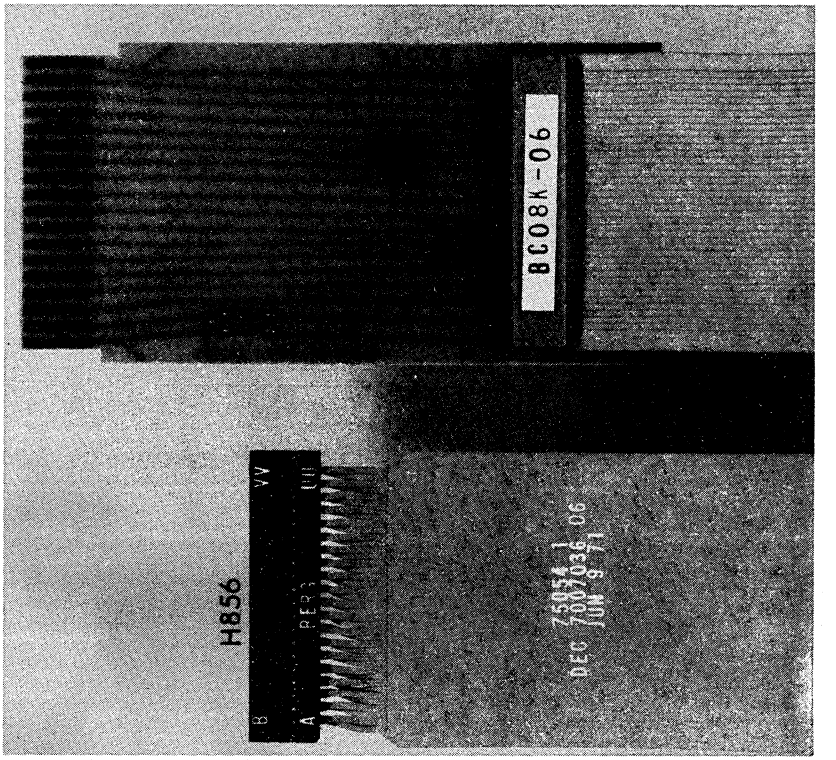
FLAT CABLES
(40 CONDUCTOR—18 SIGNALS/ALT GNDS)

TYPE	CONNECTORS	PRICE
BC08J-06	H856-M953	$ 70.00
BC08J-10	H856-M953	80.00
BC08J-15	H856-M953	90.00
BC08J-25	H856-M953	110.00
BC08J-50	H856-M953	160.00
BC08K-06	H856-*M955	65.00
BC08K-10	H856-*M955	75.00
BC08K-15	H856-*M955	85.00
BC08K-25	H856-*M955	105.00
BC08K-50	H856-*M955	155.00

* M955 single sided board



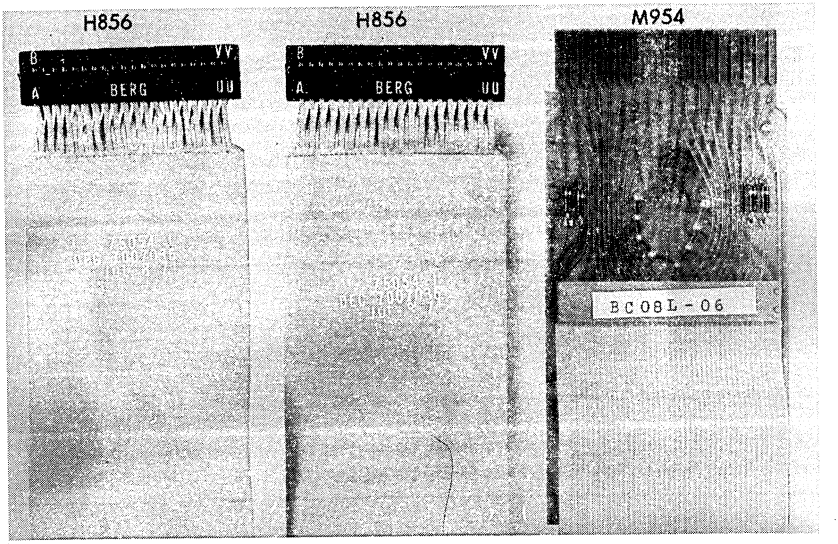
CABLE TYPE BC08J



CABLE TYPE BC08K

FLAT CABLE
(40 CONDUCTOR—36 SIGNALS)

TYPE	CONNECTORS	PRICE
BC08L-06	2/H856-M954	$110.00
BC08L-10	2/H856-M954	130.00
BC08L-15	2/H856-M954	150.00
BC08L-25	2/H856-M954	190.00
BC08L-50	2/H856-M954	290.00



CABLE TYPE BC08L

FLAT CABLES
(40 CONDUCTOR—40 SIGNAL LINES)

TYPE	CONNECTORS	PRICE
BC08R-01	H856-H856	$ 42.00
BC08R-06	H856-H856	54.00
BC08R-10	H856-H856	62.00
BC08R-20	H856-H856	82.00
BC08R-25	H856-H856	92.00
BC08R-50	H856-H856	142.00
BC08R-60	H856-H856	162.00
BC08R-100	H856-H856	240.00
BC08R-130	H856-H856	300.00
BC08R-160	H856-H856	360.00
BC04Z-01	H856-OPEN END	$ 14.00
BC04Z-06	H856-OPEN END	23.00
BC04Z-10	H856-OPEN END	32.00
BC04Z-15	H856-OPEN END	42.00
BC04Z-25	H856-OPEN END	58.00
BC04Z-50	H856-OPEN END	90.00

Cables BC08J, BC08K, BC08L, BC08R, and BC04Z are terminated at one end by a female connector which is available separately under Part No. H856. The male I/O connector which mates with the H856 cable and is available under part no. H854 for custom applications.

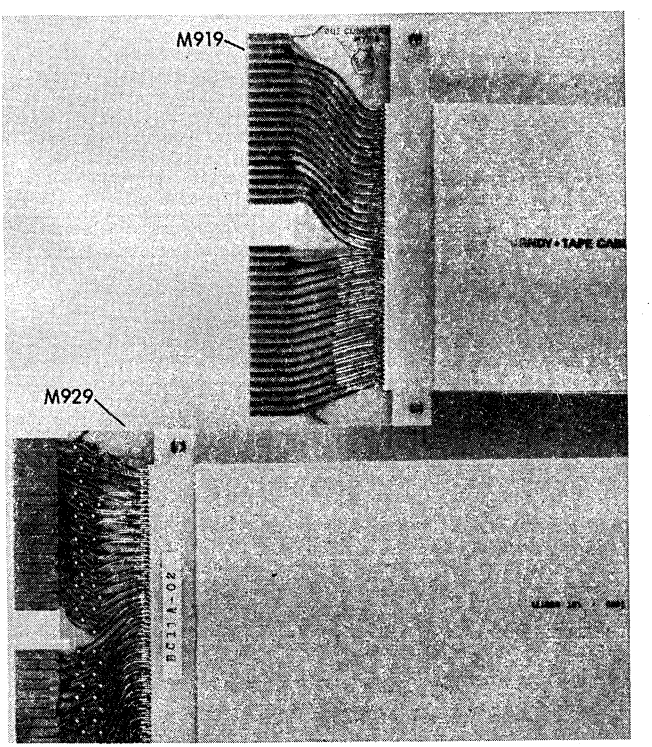
BC11A UNIBUS CABLE

The BC11A Cable consists of two 60 conductor flat mylar Flexprint cables used to connect system units in different mounting drawers or to connect peripheral devices not located within the drawer.

The 120 Conductors include all 56 UNIBUS signals and 64 ground lines.

FLAT MYLAR CABLES
(60 CONDUCTOR—DOUBLE)

TYPE	CONNECTORS	PRICE
BC11A-02	M919-M929	$ 90.00
BC11A-05	M919-M929	100.00
BC11A-08F	M919-M929	105.00
BC11A-10	M919-M929	110.00
BC11A-15	M919-M929	125.00
BC11A-20	M919-M929	140.00
BC11A-25	M919-M929	160.00
BC11A-35	M919-M929	180.00

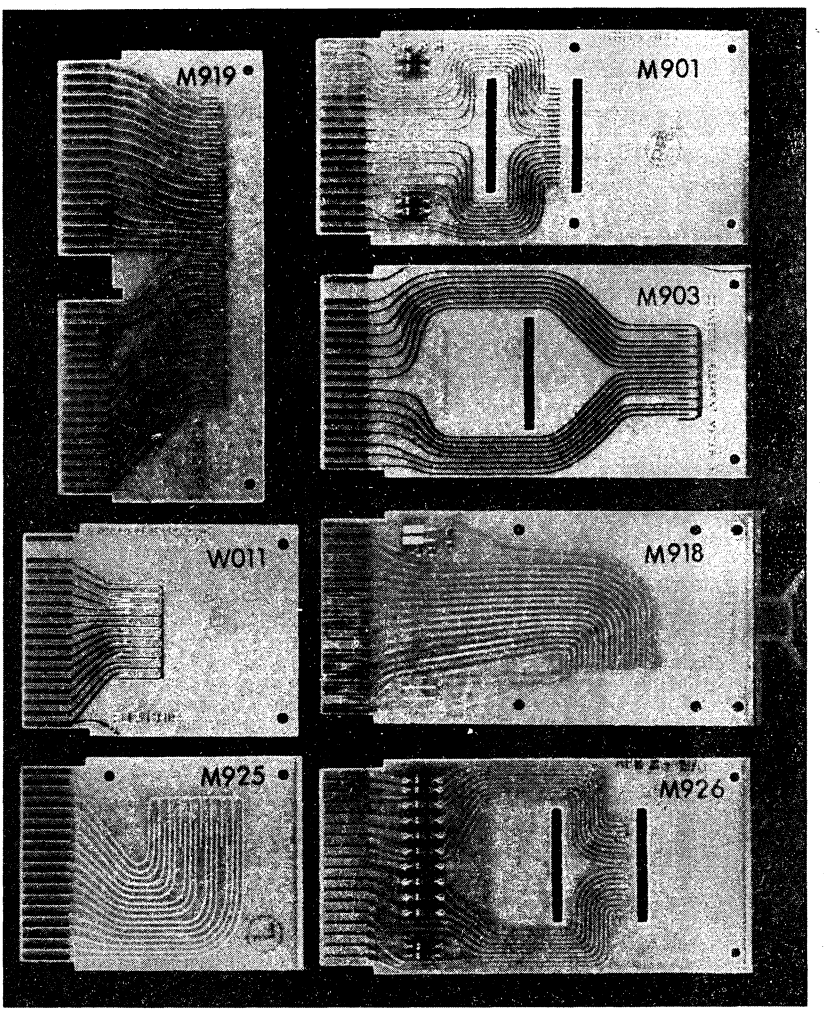


CABLE TYPE BC11A

FLAT MYLAR CABLE CONNECTORS

CABLE ACCESSORIES

Flat mylar cable connectors are available for use with 1 1/4 inch mylar Flat mylar cable (19 conductor) and 3 3/4 inch mylar (60 conductor). A series of double sided boards allows the connection of two cables per connector board.



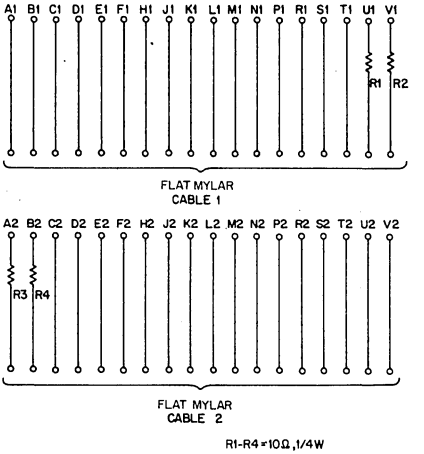
TYPICAL FLAT MYLAR CABLE CONNECTORS

FLAT MYLAR CABLE CONNECTORS
(1 1/4"—19 CONDUCTOR)

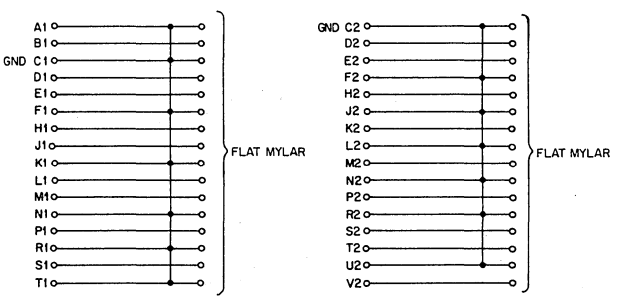
TYPE	NO. OF SIDES	CABLES NO. OF	PIN CONNECTIONS		BOARD SIZE & (TERM)	PRICE
			SIGNAL	GROUND		
M901	2	2	36 (4-10Ω resistors)	None Assigned	Single Height/ Single Length (PC Solder)	15.00
M903	2	2	18	14 Alternate	Single Height/ Single Length (PC Solder)	10.00
M915	2	2	24 (W/390Ω Clamp) 9 (Direct)	2	Single Height/ Single Length (PC Solder)	30.00
M918*	2	2	36	None Assigned	Single Height/ Single Length (PC Solder)	10.00
M922**	2	2	36	None Assigned	Single Height/ Single Length (PC Solder)	6.00
M925*	2	2	18	19 (Alternate)	Single Height/ Short Length (PC Solder)	9.00
M926	2	2	12 (W/100Ω Resistors) 24 (Direct)	None Assigned	Single Height/ Single Length (PC Solder)	27.00
W031	1	1	9	9	Single Height/ Short Length (PC Solder)	5.50
W033*	1	1	18	None Assigned	Single Height/ Single Length (PC Solder)	5.25

** Jumpers or Resistors required (see schematic)
* Cable connects at right angle to board

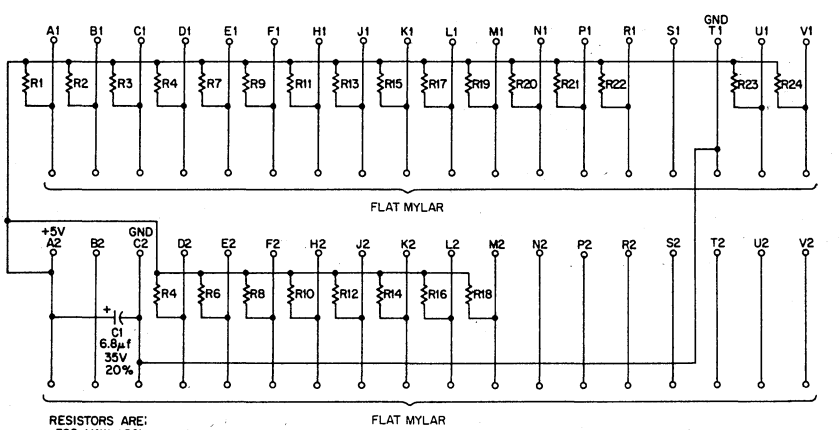
FLAT MYLAR CONNECTOR BOARD SCHEMATICS



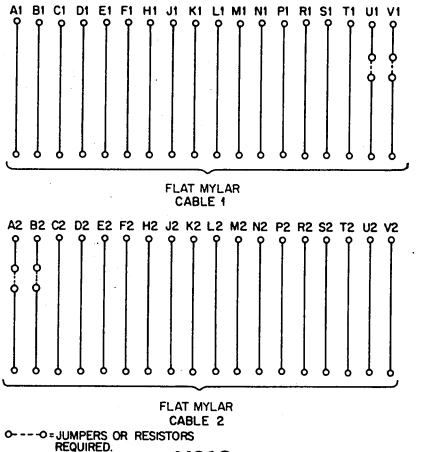
M901



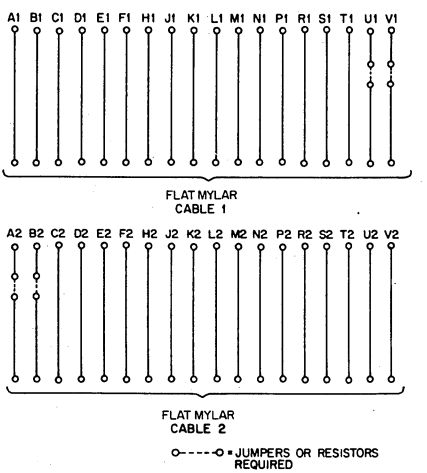
M903



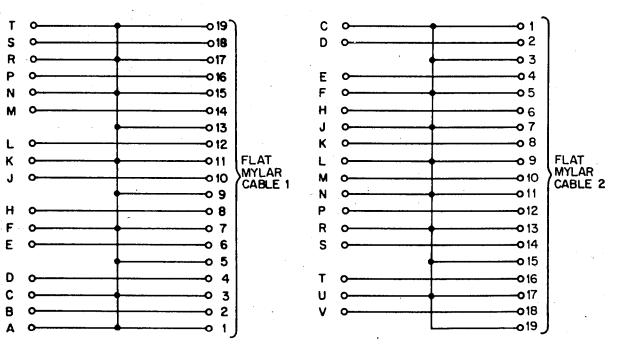
M915



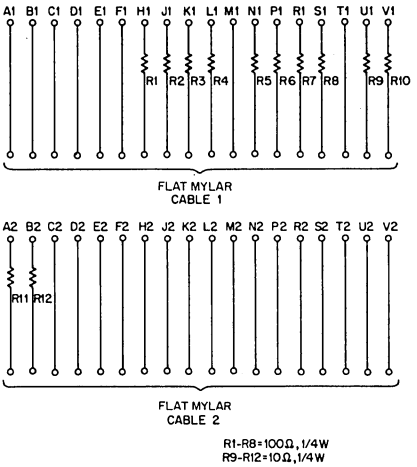
M918



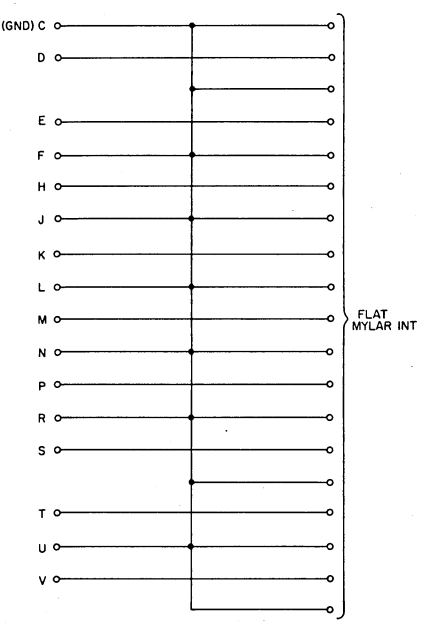
M922



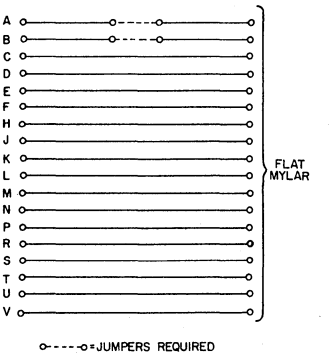
M925


A1 B1 C1 D1 E1 F1 H1 J1 K1 L1 M1 N1 P1 R1 S1 T1 U1 V1
R1 R2 R3 R4 R5 R6 R7 R8 R9 R10
FLAT MYLAR CABLE 1
A2 B2 C2 D2 E2 F2 H2 J2 K2 L2 M2 N2 P2 R2 S2 T2 U2 V2
R11 R12
FLAT MYLAR CABLE 2
R1-R8=100Ω, 1/4W
R9-R12=10Ω, 1/4W

M926


(GND) C
D
E
F
H
J
K
L
M
N
P
R
S
T
U
V
FLAT MYLAR INT

W031

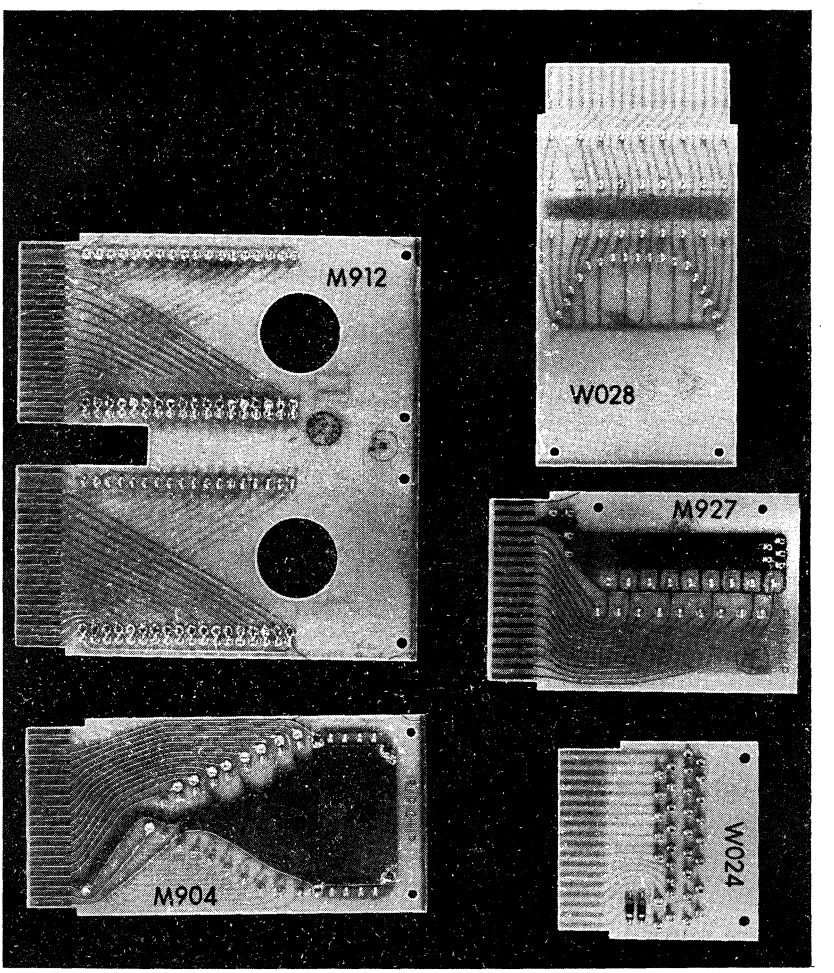


W033

COAX CABLE CONNECTORS

CABLE ACCESSORIES

Coax cable connectors are available for use with both 9-conductor flat coax cable (DEC No. 17-00001), 9 conductor round cable (DEC No. 17-00003), and 36 conductor, twisted pair cable (DEC No. 91-07599). Both single and double sided connector can be provided.



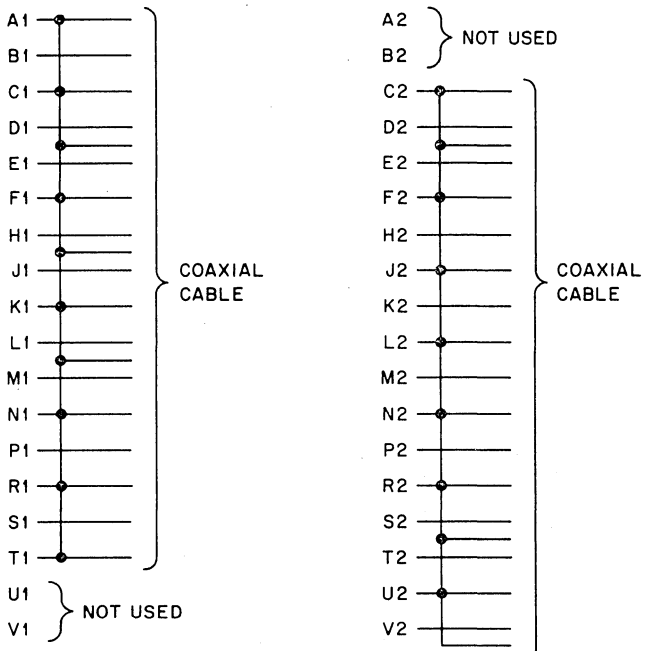
TYPICAL COAX CABLE CONNECTORS

COAX CABLE CONNECTORS
(9 CONDUCTOR)

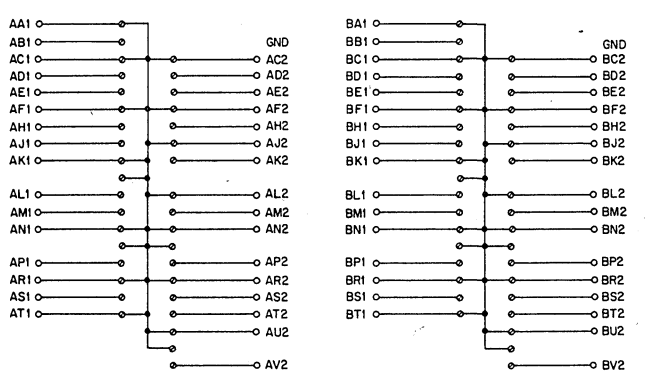
TYPE	NO. OF SIDES	NO. OF CABLES	PIN CONNECTIONS		BOARD SIZE & (TERM)	PRICE
			SIGNAL	GROUND		
M904	2	2	18	13 (Alternate)	Single Height/ Single Length (Split Lug)	10.00
M927	2	1	18	18 (Alternate)	Single Height/ Short Length (Split Lug)	6.00
W024	1	1	16	2	Single Height/ Short Length (Split Lug)	6.00
W028*	1	1	9	10 (Alternate)	Single Height/ Single Length (Split Lug)	6.00

NOTE: Connectors W011, W021, W022 are also used with 9 conductor coax cable (Refer to Ribbon Connectors for details).

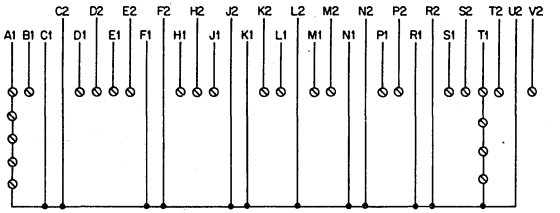
* Jumpers or Resistors required (see schematic)


A1
B1
C1
D1
E1
F1
H1
J1
K1
L1
M1
N1
P1
R1
S1
T1
COAXIAL CABLE
U1
V1
NOT USED
A2
B2
NOT USED
C2
D2
E2
F2
H2
J2
K2
L2
M2
N2
P2
R2
S2
T2
U2
V2
COAXIAL CABLE

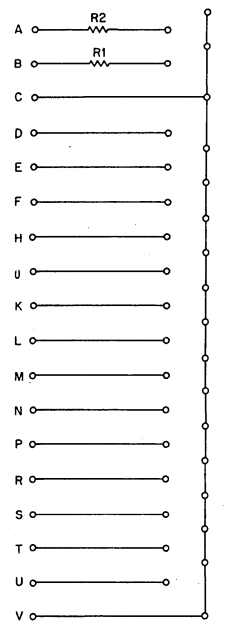
M904


AA1
AB1
AC1
AD1
AE1
AF1
AH1
AJ1
AK1
AL1
AM1
AN1
AP1
AR1
AS1
AT1
GND
AC2
AD2
AE2
AF2
AH2
AJ2
AK2
AL2
AM2
AN2
AP2
AR2
AS2
AT2
AU2
AV2
BA1
BB1
BC1
BD1
BE1
BF1
BH1
BJ1
BK1
BL1
BM1
BN1
BP1
BR1
BS1
BT1
GND
BC2
BD2
BE2
BF2
BH2
BJ2
BK2
BL2
BM2
BN2
BP2
BR2
BS2
BT2
BU2
BV2
• SPLIT LUGS

M912

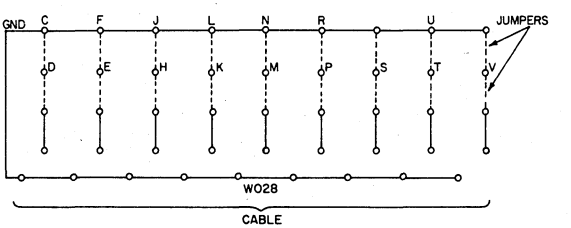


M927



R1, R2=10Ω, 1/4W

W024

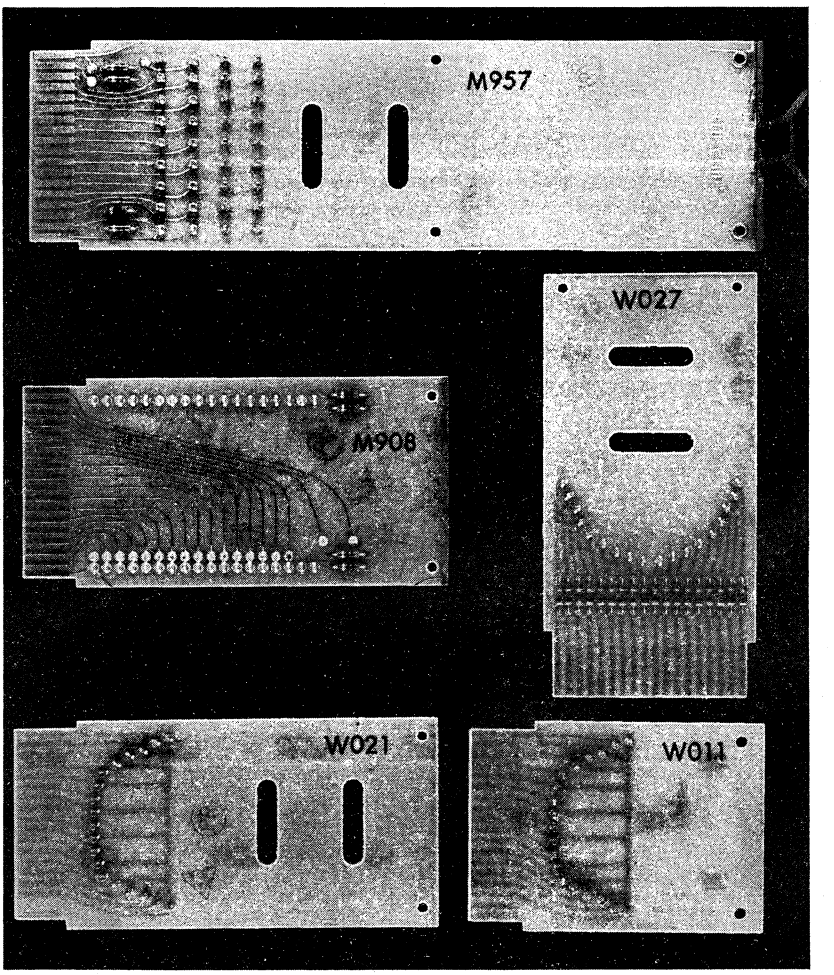


W028

RIBBON CABLE CONNECTORS

CABLE ACCESSORIES

Cable connectors are available for use with 20 conductor ribbon cable (DEC No. 91-07575). The cable conductors are soldered directly to split lugs on the boards. The M908 and M957 are double sided boards to allow the connection of two 20-conductor cables per board.

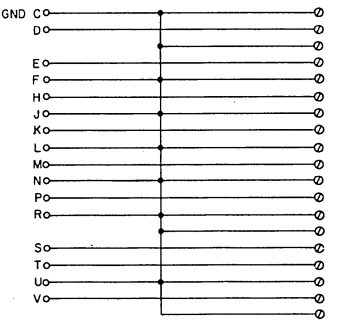


TYPICAL RIBBON CABLE CONNECTORS

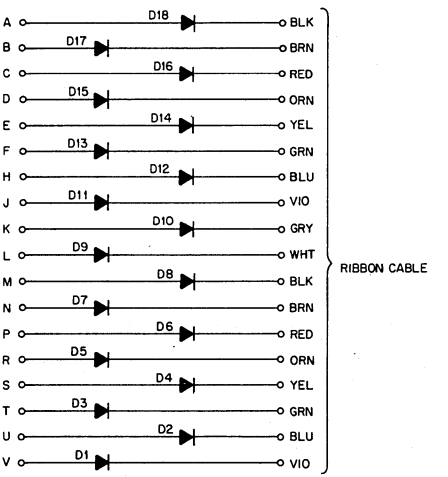
RIBBON CABLE CONNECTORS (20 CONDUCTOR)

TYPE	NO. OF SIDES	NO. OF CABLES	PIN CONNECTIONS		BOARD SIZE & (TERM)	PRICE
			SIGNAL	GROUND		
W011	1	1	9	9 (Alternate)	Single Height/ Short Length (Split Lug)	$6.00
W018	1	1	18 (W/D664 Diodes)	None Assigned	Single Height/ Short Length (Split Lug)	9.00
W020	1	1	18 (W/1500Ω Resistors)	None Assigned	Single Height/ Single Length (Split Lug)	8.00
W021	1	1	9	9 (Alternate)	Single Height/ Single Length (Split Lug)	6.00
W022	1	1	9 (W/100Ω Loads)	9 (Alternate)	Single Height/ Single Length (Split Lug)	6.00
W023*	1	1	18	None Assigned	Single Height/ Single Length (Split Lug)	6.00
W027	1	1	18 (3000Ω Resistors)	None Assigned	Single Height/ Single Length (Split Lug)	7.00
M908	2	2	4 (W/10Ω Resistors) 32 (Direct)	None Assigned	Single Height/ Single Length (Split Lug)	10.00
M917	2	2	18	14 (Alternate)	Single Height/ Single Length (Split Lug)	10.00
M957	2	2	36	None Assigned	Single Height/ Extended Length (Split Lug)	21.00

* Jumpers or Resistors required

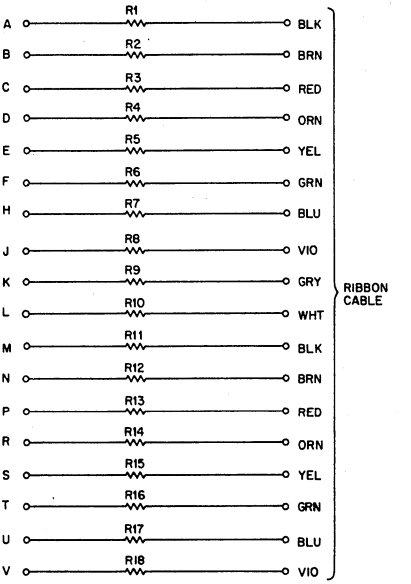


W011

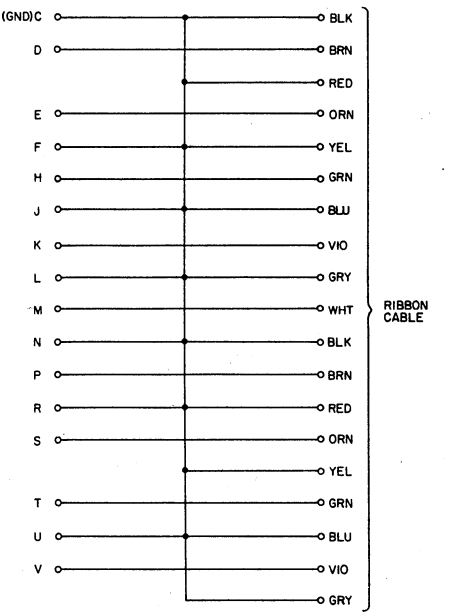


ALL DIODES ARE D664

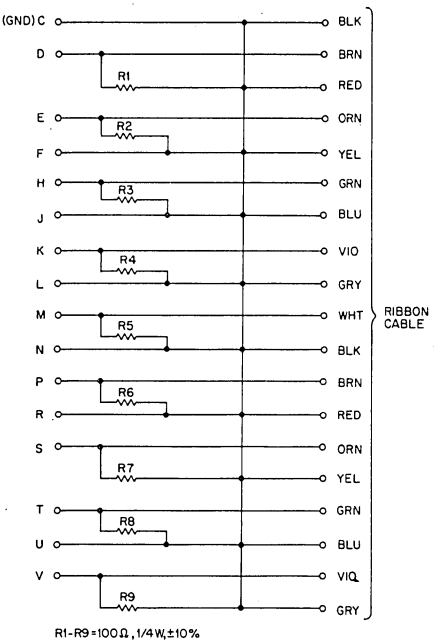
W018


A
B
C
D
E
F
H
J
K
L
M
N
P
R
S
T
U
V
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
BLK
BRN
RED
ORN
YEL
GRN
BLU
VIO
GRY
WHT
BLK
BRN
RED
ORN
YEL
GRN
BLU
VIO
RIBBON CABLE
RESISTORS ARE:
1500Ω ,±5%

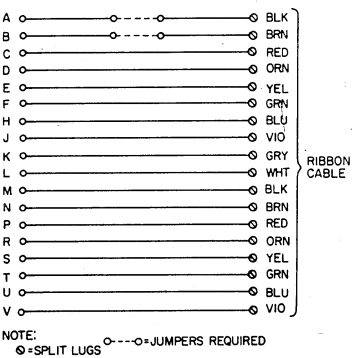
W020


(GND)C
D
E
F
H
J
K
L
M
N
P
R
S
T
U
V
BLK
BRN
RED
ORN
YEL
GRN
BLU
VIO
GRY
WHT
BLK
BRN
RED
ORN
YEL
GRN
BLU
VIO
GRY
RIBBON CABLE

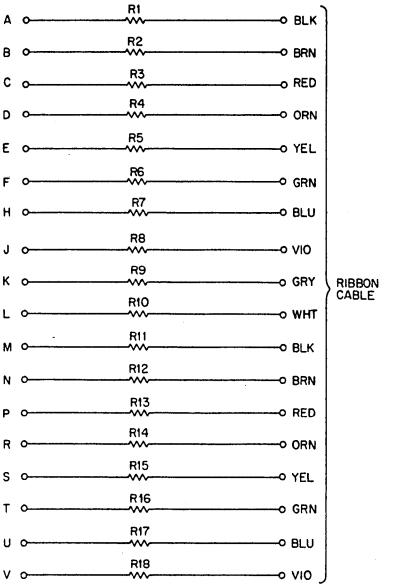
W021


(GND) C
D
E
F
H
J
K
L
M
N
P
R
S
T
U
V
R1
R2
R3
R4
R5
R6
R7
R8
R9
BLK
BRN
RED
ORN
YEL
GRN
BLU
VIO
GRY
WHT
BLK
BRN
RED
ORN
YEL
GRN
BLU
VIO
GRY
RIBBON CABLE
R1-R9 = 100Ω, 1/4W, ±10%

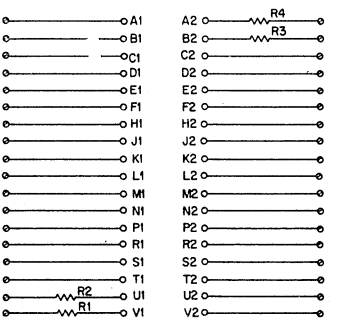
W022


A
B
C
D
E
F
H
J
K
L
M
N
P
R
S
T
U
V
BLK
BRN
RED
ORN
YEL
GRN
BLU
VIO
GRY
WHT
BLK
BRN
RED
ORN
YEL
GRN
BLU
VIO
RIBBON CABLE
NOTE:
⊘ = SPLIT LUGS
o---o = JUMPERS REQUIRED

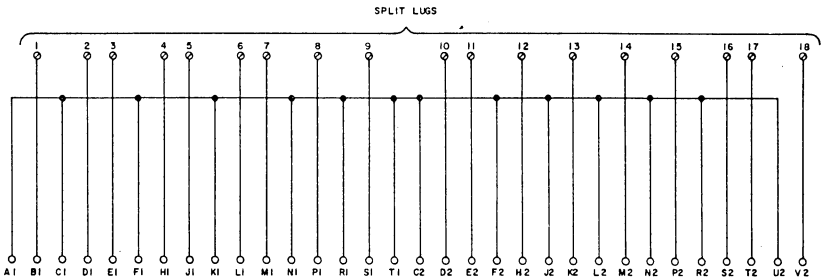
W023


A R1 BLK
B R2 BRN
C R3 RED
D R4 ORN
E R5 YEL
F R6 GRN
H R7 BLU
J R8 VIO
K R9 GRY
L R10 WHT
M R11 BLK
N R12 BRN
P R13 RED
R R14 ORN
S R15 YEL
T R16 GRN
U R17 BLU
V R18 VIO
RIBBON CABLE
ALL RESISTORS ARE: 3000, 1/4W, ±5%

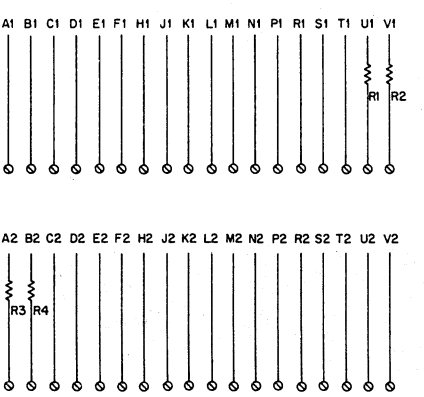
W027


A1
B1
C1
D1
E1
F1
H1
J1
K1
L1
M1
N1
P1
R1
S1
T1
U1
V1
R2
R1
A2
B2
C2
D2
E2
F2
H2
J2
K2
L2
M2
N2
P2
R2
S2
T2
U2
V2
R4
R3
R1-R4=10Ω, 1/4W
⊗ SPLIT LUG

M908


SPLIT LUGS
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
A1 B1 C1 D1 E1 F1 H1 J1 K1 L1 M1 N1 P1 R1 S1 T1 C2 D2 E2 F2 H2 J2 K2 L2 M2 N2 P2 R2 S2 T2 U2 V2

M917

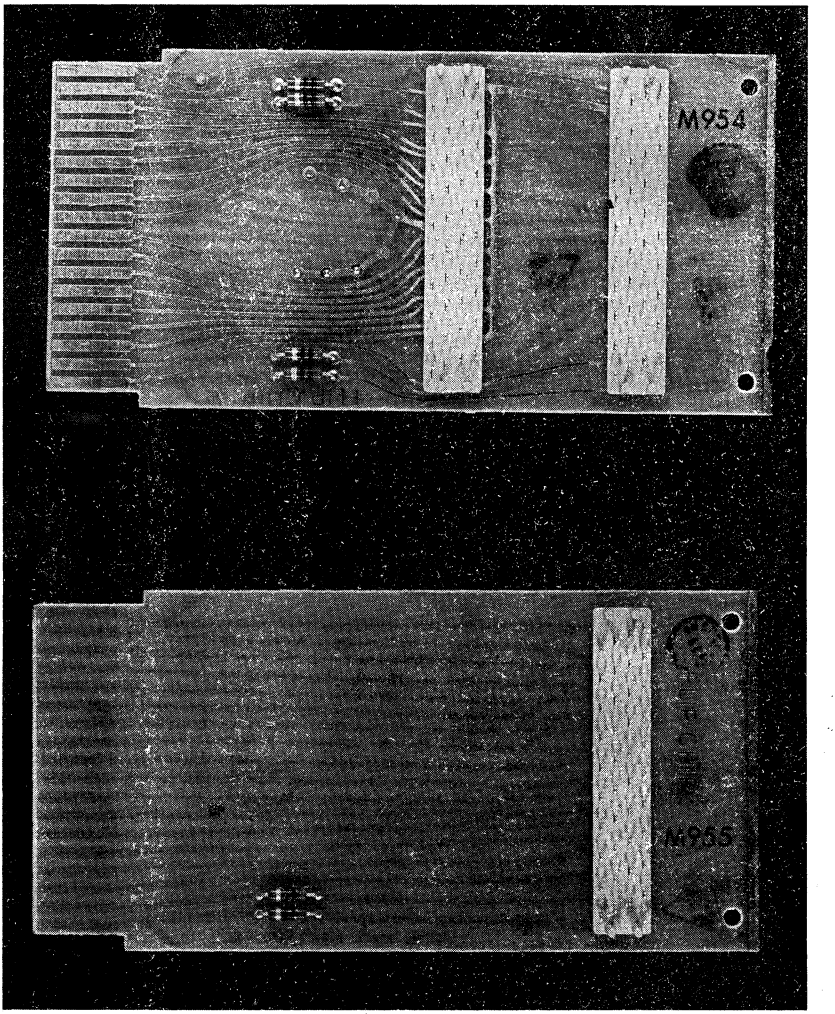

A1 B1 C1 D1 E1 F1 H1 J1 K1 L1 M1 N1 P1 R1 S1 T1 U1 V1
R1
R2
A2 B2 C2 D2 E2 F2 H2 J2 K2 L2 M2 N2 P2 R2 S2 T2 U2 V2
R3
R4
R1-R4=10Ω, 1/4W

M957

FLAT CABLE CONNECTORS

CABLE ACCESSORIES

A series of solderless cable connectors are provided for use with 40 conductor flat cable (DEC No. 91-07722). These connectors are used for general interface and with the PDP-8e.



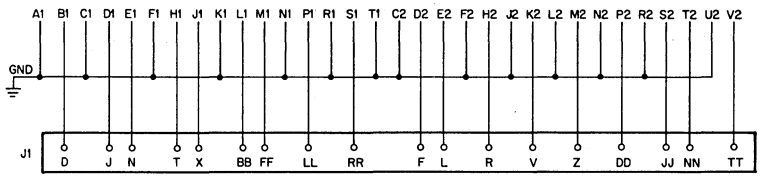
TYPICAL FLAT CABLE CONNECTORS

FLAT CABLE CONNECTORS
(40 CONDUCTOR)

TYPE	NO. OF SIDES	NO. OF CABLES	PIN CONNECTIONS		BOARD SIZE & (TERM)	PRICE
			SIGNAL	GROUND		
H856	Not Applicable	1	40	None Assigned	Mates with H854 (Board Mounted Male)	8.00
M953	2	1	18	18 (Alternate)	Single Height/ Single Length (Solderless Connect J1)	$25.00
M954*	2	2	36	None Assigned	Single Height/ Single Length (Solderless Connect J1 & J2)	27.00
M955	1	1	18	None Assigned	Single Height/ Single Length (Solderless Connect J1)	27.00

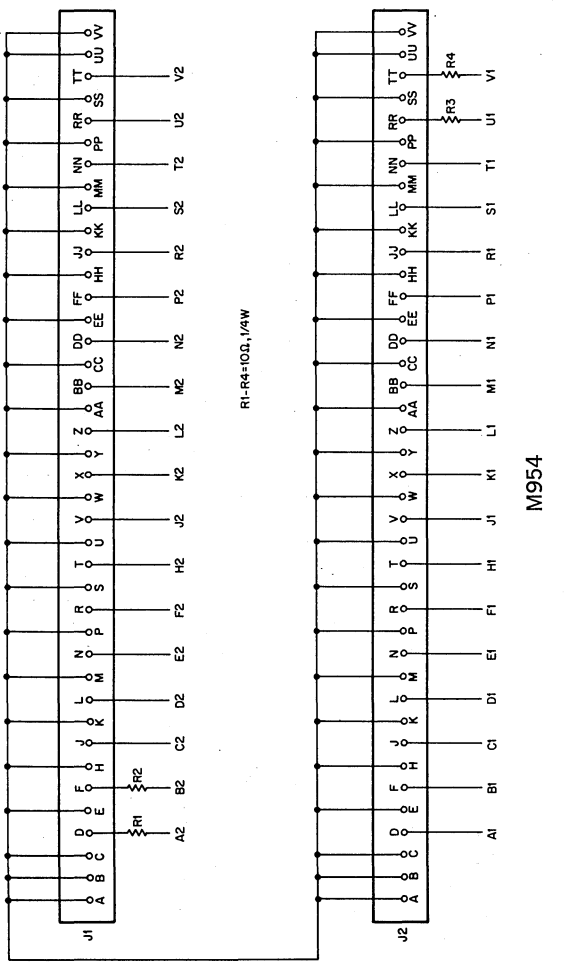
* Jumpers or Resistors required

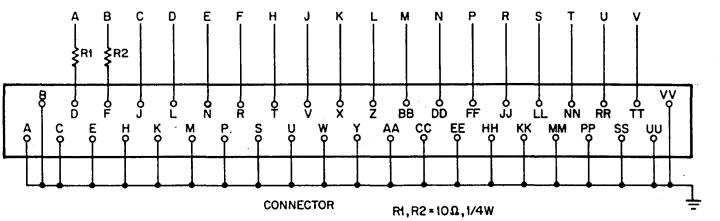
FLAT CABLE CONNECTOR BOARD SCHEMATICS



ALL OTHER PINS ON J1 = GROUND

M953



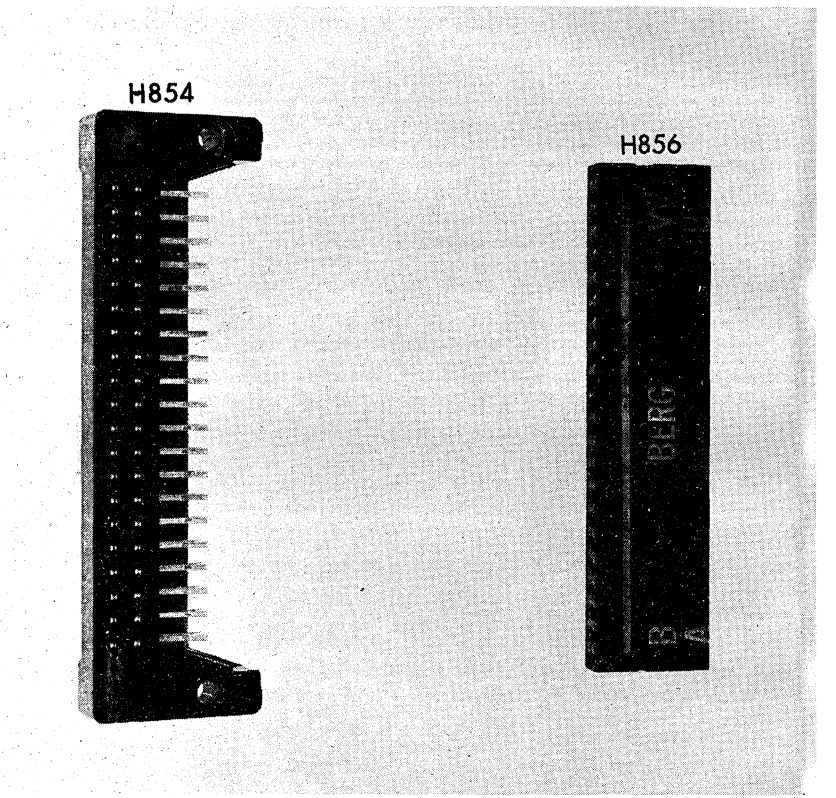

A B C D E F H J K L M N P R S T U V
R1
R2
B D F J L N R T V X Z BB DD FF JJ LL NN RR TT VV
A C E H K M P S U W Y AA CC EE HH KK MM PP SS UU
CONNECTOR
R1, R2 = 10Ω, 1/4W

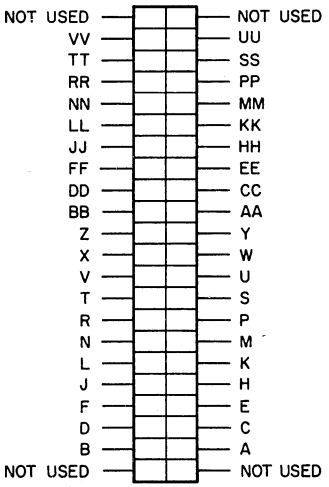
M955

I/O CONNECTOR
H854 AND H856

CABLE ACCESSORIES

The H854 is an I/O connector (male) housing that can be mounted at right angles to a PC module board and soldered in place. The H854 mates with the H856 (female) which is used to terminate a 40-conductor flat cable as shown on cables BC08J, BC08K, BC08L, BC08R and BC04Z. All 40 pins can be used for the transfer of signals. Purchased separately, the H856 consists of a connector housing and 40 contacts. The contacts of the H854 are premounted in the housing.





H856 PIN ASSIGNMENTS

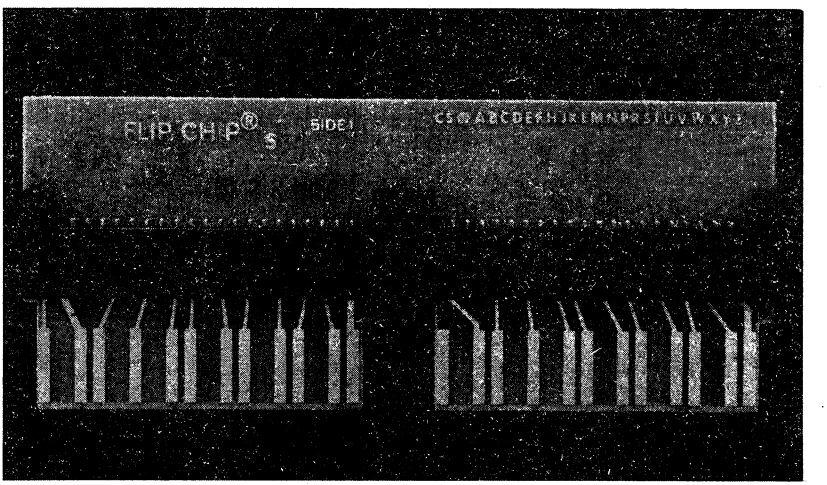
H854 — $12.00
H856 — $ 8.00

M975
FLIP CHIP TO H854 ADAPTER

CABLE ACCESSORIES

Length: Special
Height: Double
Width: Single

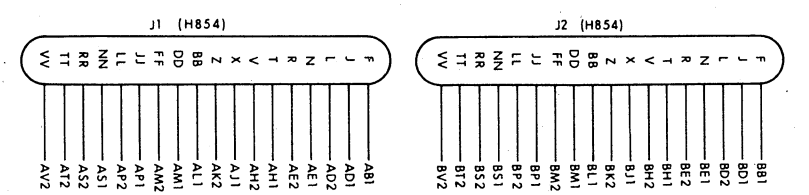
Price: $35



The M975 is an adapter board for use in systems where the need for inputting or outputting logic panel wiring to H854 connectors is desired. The M975, because of its special height, can accommodate up to two BC08J cables. The two H854 connectors on the M975 are not electrically connected and should not be confused with the M9100. When the M975 is installed in the logic panel, it protrudes only 1-1/2 inches. This refers to its special length.

APPLICATIONS

The M975 is compatible with all M Series logic. Although designed primarily for use with the PDP-11, it can be used almost anywhere there is accommodation for a double-height module.



NOTE: All point on J1 and J2 not shown are grounded.

hardware

Digital manufactures a complete line of hardware in support of its module series. Module connectors are available for as few as one module and as many as 64 in a single rack (H020). A complete line of cabinets is available to house the modules and their connector blocks, as well as providing a convenient means for system expansion.

Coupled with the recent additions to the hardware line, Digital has made every effort to maintain or improve the high standards of reliability and performance of its present line. Through the availability of a wide range of basic accessories DEC feels that it is offering the logic designer the necessary building blocks which he requires for complete system design.

WIRING HINTS

These suggestions may help reduce mounting panel wiring time. They are not intended to replace any special wiring instructions given on individual module data sheets or in application notes. For fastest and neatest wiring, the following order is recommended.

(1) All power & ground wiring and any horizontally bussed signal wiring. Use Horizontal Bussing Strips Type 932 for type H800, 933 for type H803, or 939 for type H808.

(2) Vertical grounding wires interconnecting each chassis ground with pin C grounds. Start these wires at the uppermost mounting panel and continue to the bottom panel. Space the wires 2 inches apart, so each of the chassis-ground pins is in line with one of them. Each vertical ground wire makes three connections at each mounting panel.

(3) All other ground wires. Always use the nearest pin C above the pin to be grounded, unless a special grounding pin has been provided in the module.

(4) All signal wires in any convenient order. Point-to-point wiring produces the shortest wire lengths, goes in the fastest, is easiest to trace and change, and generally results in better appearance and performance than cabled wiring. Point-to-point wiring is strongly urged.

The wire size for use with the H800 connector blocks and 1943 mounting panel is 24 for wire wrap, and 22 for soldering. The size for use with H803 block and H911 mounting panel is #30 wire. Larger or smaller wire may be used depending on the number of connections to be made to each lug. Solid wire and a heat resistant spaghetti (Teflon) are easiest to use when soldering.

Adequate grounding is essential. In addition to the connection between mounting panels mentioned above, there must be continuity of grounds between cabinets and between the logic assembly and any equipment with which the logic communicates.

When soldering is done on a mounting panel containing modules, a 6-V (transformer) soldering iron should be used. A 110-V soldering iron may damage the modules.

When wire wrapping is done on a mounting panel containing modules, steps must be taken to avoid voltage transients that can burn out transistors. A battery- or air-operated tool is preferred, but the filter built into some line-operated tools affords some protection.

Even with completely isolated tools, such as those operated by batteries or compressed air, a static charge can often build up and burn out semiconductors. In order to prevent damage, the wire wrap tool should be grounded except when all modules are removed from the mounting panel during wire wrapping.

AUTOMATIC WIRING

Significant cost savings can be realized in quantity production if the newest automatic wiring techniques are utilized. Every user of FLIP CHIP modules benefits from the extensive investment in high-production machinery at Digital, but some can go a step further by taking advantage of programmed wiring for their FLIP CHIP digital systems.

While the break-even point for hand wiring versus programmed wiring depends upon many factors that are difficult to predict precisely, there are a few indications:

1. One-of-a-kind systems will probably not be economical with automatic wiring, unless a customer has high overhead costs and performs a time-consuming (costly) hand assembly.

2. At the other end of the spectrum, production of 50 or 100 identical systems of almost any size would be worth automating, not only to lower the cost of the wiring itself but also to reduce human error. At this level of volume, machine-wired costs can be expected to be considerably less than the cost of hand wiring.

3. For two to five systems of several thousand wires each, a decision on the basis of secondary factors will probably be necessary: ease of making changes, wiring lead time, reliability predictions, and availability of relevant skills are factors to consider.

Digital can supply further information to those interested in programmed wiring techniques. Contact Logic Products Marketing, DEC, Maynard, Mass. 01754.

COOLING OF FLIP CHIP MODULES

The low power consumption of K and M series modules results in a total of only about 25 watts dissipation in a typical 1943 Mounting Panel with 64 modules. This allows up to six panels of modules to be mounted together and cooled by convection alone, if air is allowed to circulate freely. In higher-dissipation systems using modules in significant quantities from the A series, the number of mounting panels stacked together must be reduced without forced-air cooling. In general, total dissipation from all modules in a convection-cooled system should be 150 watts or less.

The regulating transformers used in most DEC power supplies have nearly constant heat dissipation for any loading within the ratings of the supply. Power dissipated within each supply will be roughly equal to half its maximum rated ouput power. If power supplies are mounted below any of the modules in a convection-cooled system, this dissipation must be included when checking against the 150 watt limit.

CONNECTOR BLOCKS

The Series 800 Connector Blocks are compatible with a wide variety of both single and double sided DEC modules and connector boards. The Summary is a general listing of the types available. For detailed information, refer to the connector block descriptions which follow.

CONNECTOR BLOCK SUMMARY

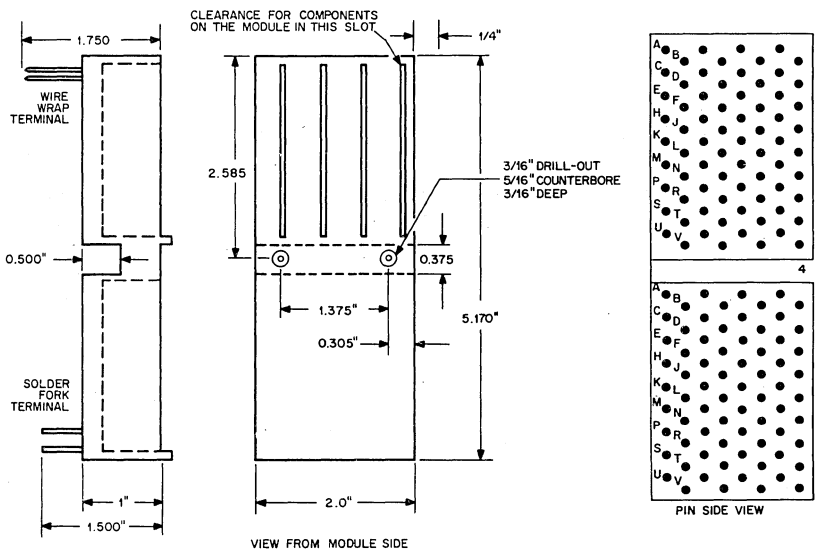
BLOCK PART NO.	NO. OF SLOTS	CONTACTS PER SLOT	NO. OF CONTACT SIDES	WIRE WRAP PIN SIZE	BUS STRIP NO.	MODULE TYPE
H800	8	18	1	24 (AWG)	932	All Except M Series
H802	1	18	1	24 (AWG)	None	All Single Height Except M Series
H803	8	36	2	30 (AWG)	933	All
H807	1	36	2	30 (AWG)	None	All Single Height
H808	4	36	2	24 (AWG)	939	All

H800-W, H800-F CONNECTOR BLOCKS

HARDWARE

This is the 8-module socket assembly used in FLIP CHIP mounting panels. Because of its 18 pin connectors, it can be used for all modules except those with pins on both sides of the board. Pin dimensions are .031 inches by .062 inches and may be of either a wire wrap or solder fork type. Number 24 awg. gauge wire should be used with these connectors.

The drawings below show the pertinent dimensions.



REPLACEMENT CONTACTS TYPES H801-W, H801-F

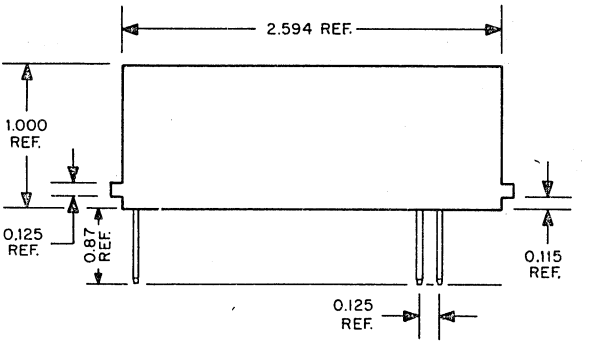
These contacts are offered in packages of 18 for replacement purposes. In each package, nine straight and nine offset contacts are included, enough to replace all contacts in one socket.

H801-W is for wire-wrap connectors; H801-F is for solder-fork connectors.

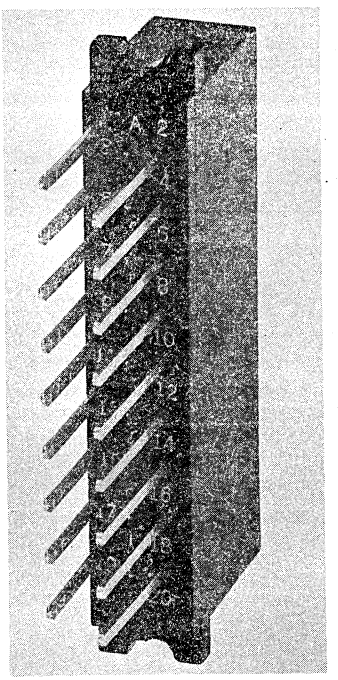
H800F—$8
H800W—$8
H801F—$2
H801W—$2

H802
CONNECTOR BLOCK

HARDWARE



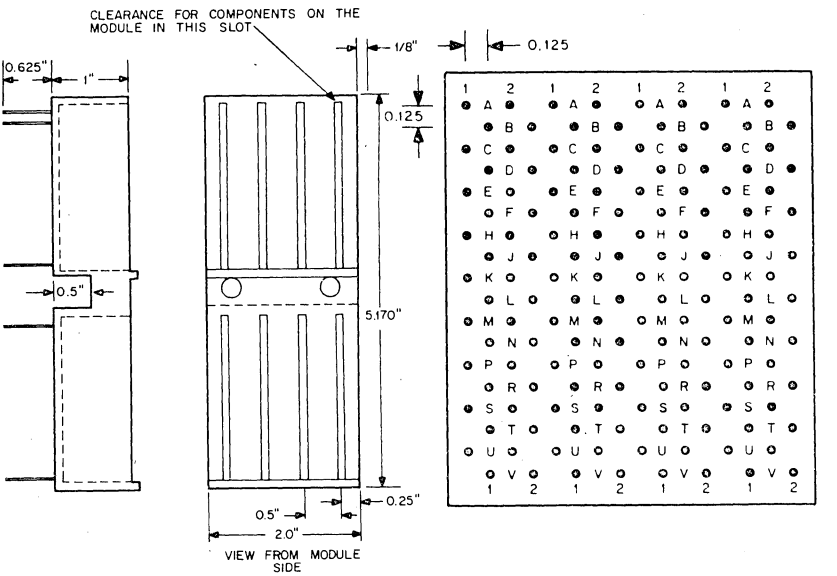
This is an 18 pin connector block for a single FLIP CHIP® module. It can be used to mount all modules except those with pins on both sides of the board. Pin dimensions are .031 inches by .062 inches and may be of the wire wrap type only. Number 24 wire should be used with this connector.



H802—$4

H803, H805
CONNECTOR BLOCK AND PINS

HARDWARE



The H803 is the 8-module molded Connector Assembly used in the H911 mounting panels. For each of the eight modules, it provides a 36-pin connector with the wirewrap pins forming a 0.125-inch staggered grid as shown above. This connector is designed to be used with M Series modules; however, it can also be used with all other series listed in this handbook.

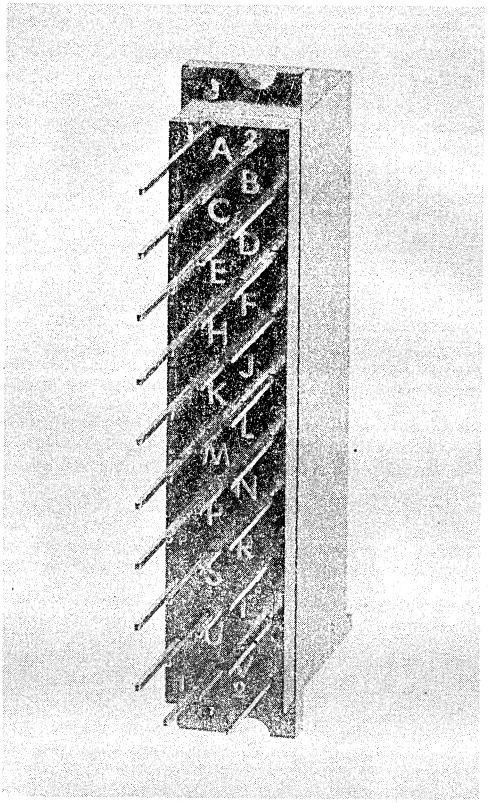
The blocks have the same physical dimensions as the H800 with the exception of pin length. These blocks are only available with wire wrap pins which are designed to be wrapped with number 30 wire. Pin dimensions are 0.025 inches square. W&K Series 18 pin modules will make contact with only the 2-side pins (A2, B2, etc.).

H805 is a package of 36 pins (18 left and 18 right) to be used as replacements in H803 blocks.

H803 — $13
H805 — $4

H807
CONNECTOR BLOCK

HARDWARE

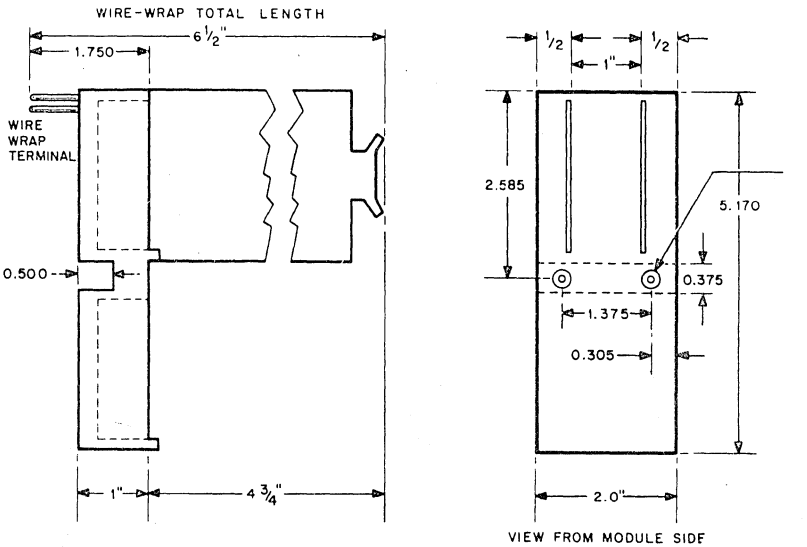


This is a 36 pin single slot connector. It is provided for M-Series modules but can be used with modules or connector boards in the K and W Series. Uses include mounting in confined or irregular spaces. Often the H807 is used to terminate a connector board at a remote location. The H807 is available only with wire wrap pins.

H807 — $5

H808 CONNECTOR BLOCK AND H809 PINS

HARDWARE

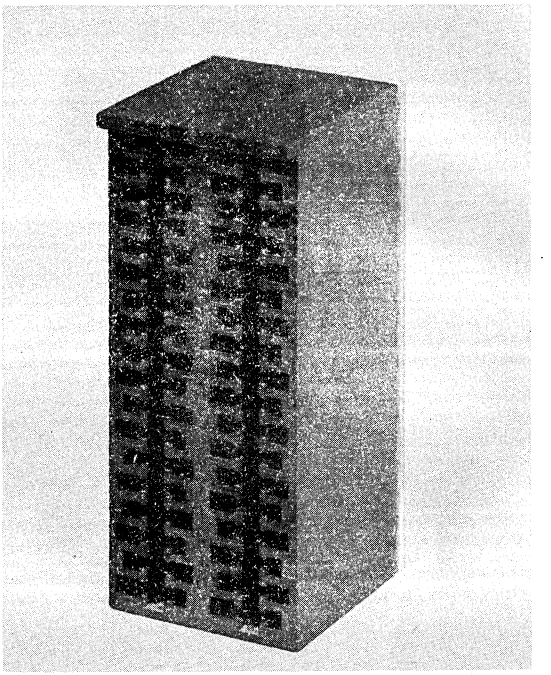


The H808 is a relatively low density connector block for use with all modules in the catalog. This includes A, K, M, and W Series modules. The connector provides 4 module slots each having 36 pins. On A,K and W Series modules only the 2 side pins, (A2, B2, etc.) will make contact. This connector adds a measure of convenience and versatility to the many uses to which these catalog modules can be applied. Hand wiring of connector pins is more easily accomplished for M Series prototype work. H800 and H808 connector blocks can be mixed for M and A, K, W module mixing purposes. Wire wrapping patterns can be maintained even though module letter series are mixed because H800 & H808 pin layout is identical. H809 is a package of 36 replacement pins, 18 left and 18 right.

H808—$10
H809—$ 4

H851
EDGE CONNECTOR

HARDWARE

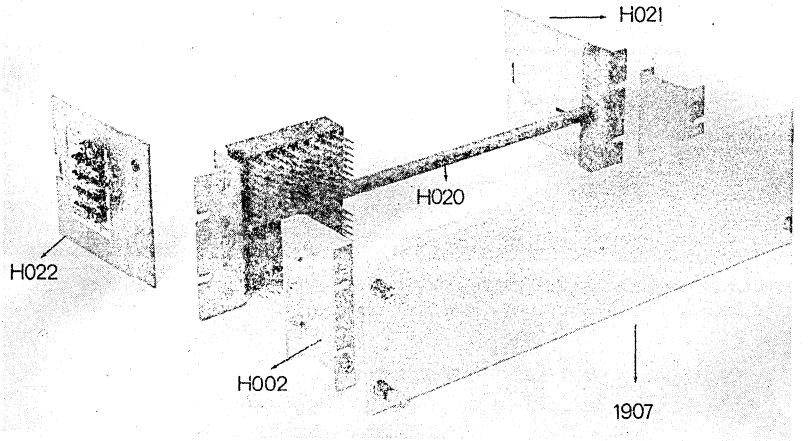


The H851 edge connector is used to bus signals from the top center terminal fingers to an adjacent quad board with similar terminals.

H851 — $15.00

H001, H002, H020, H021, H022 H024, H025 AND 1907 COVER MOUNTING PANEL HARDWARE

HARDWARE



Pairs of brackets. H001 provides ¾" standoff to mount 1907 over mounting panel wiring. H002 provides a 2" setback so a control panel with switches, lamps, etc. can be mounted flush with mounting rack or cabinet in front of logic wiring.

The H020 consists of a 19" mounting frame casting. Components which can be mounted on this frame include, H800, H803, H808 connector blocks, power supplies or customer components that are adapted to the frame mounting requirements.

H021—Single offset end plate which mounts to the H020. This end plate provides a mount for the 1945-19 hold down bar, if required.

H022—Single end plate similar to the H021 on which is mounted a terminal block assembly for ease of parallel power wiring to adjacent panels.

H024—Single offset end plate 8½" (Extended length version of H021).

H025—Single offset end plate 8½" (Extended length version of the H022 with terminal block).

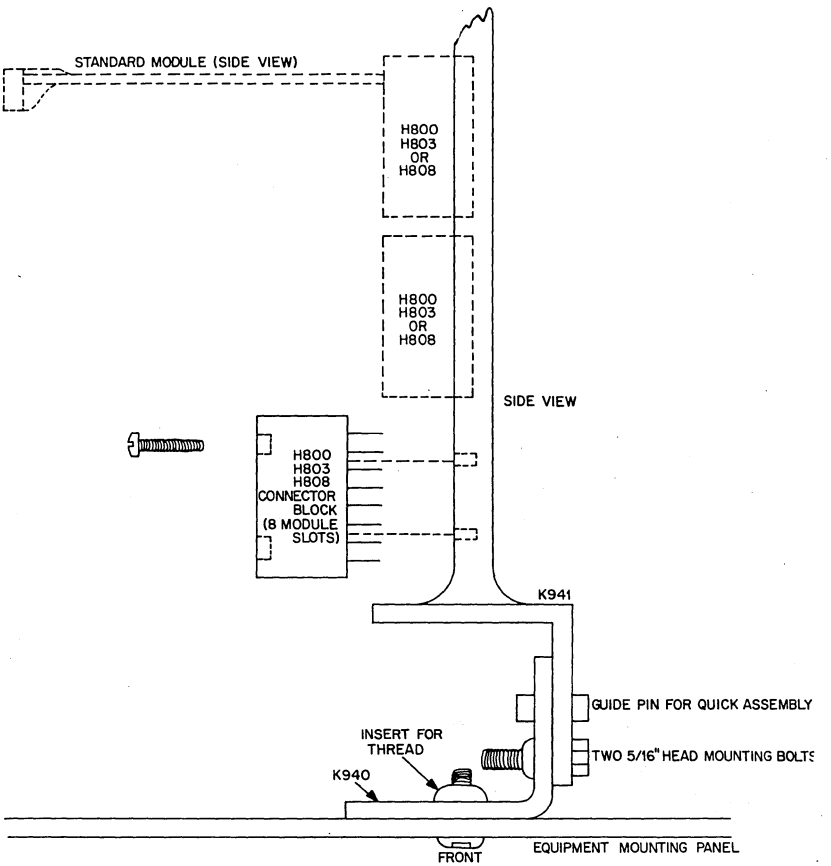
1945-19 HOLD DOWN BAR: Reduces vibration and keeps modules securely mounted when panel or system is moved. Adds ½ in. to depth of mounting panel.

1907 Panel Cover—Blue or brown tweed painted aluminum cover with captive screws to mate threaded bushings in K980 and H001. Adds to appearance while protecting system against vibration and tampering. When choice of color is not specified, blue will be supplied.

H001 — $7	H022 — $20
H002 — $15	1945-19 — $20
H020 — $15	1907 — $9
H021 — $7	
H024 — $7	
H025 — $20	

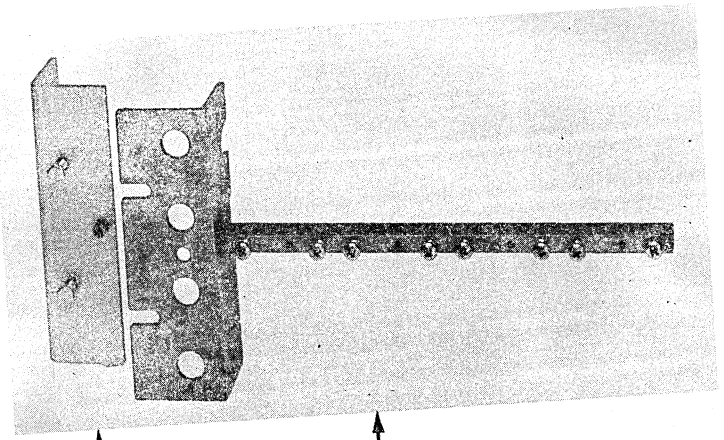
K940, K941
MOUNTING HARDWARE

HARDWARE



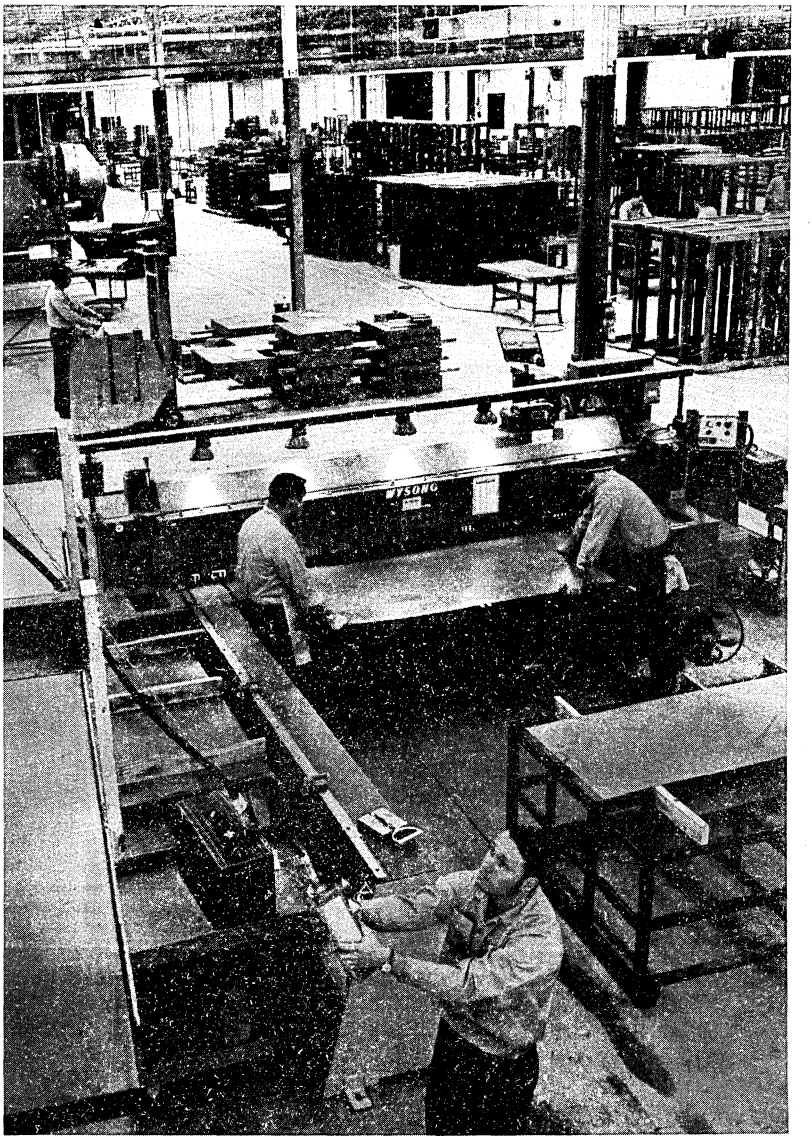
This convenient mounting hardware permits logic connector pin wiring to be done before logic is installed in the enclosure.

K940 is a mounting support that attaches to the enclosure. K941 is a removable bracket that mounts up to four H800, H803, or H808 connector blocks. Any connections to external equipment are made through the ribbon connectors of interface signal modules (K508, K524, K604, K644) to the K716 Interface Block.



TOP VIEW

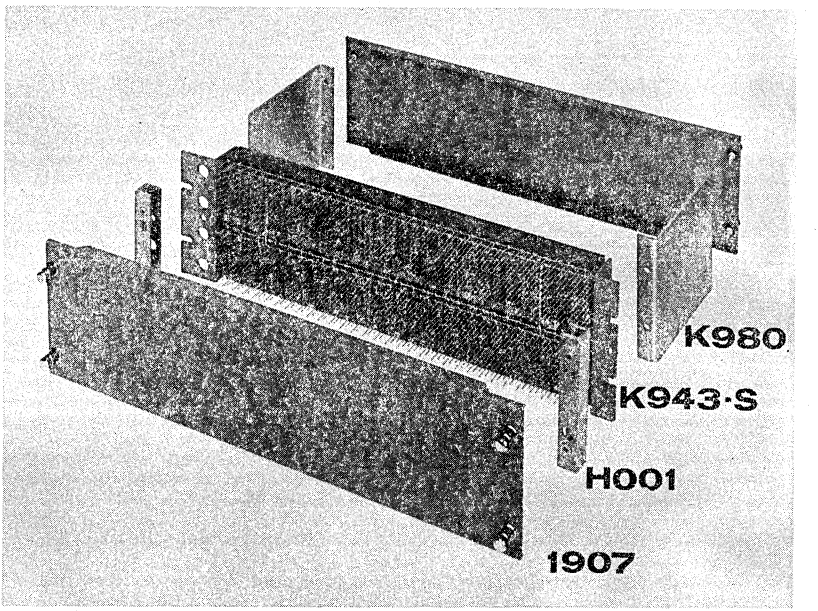
K940 — $6
K941 — $6



Cabinets for DEC systems are manufactured in this portion of DEC's recently opened Westfield, Massachusetts production facility.

K943-R, K943-S
19" MOUNTING PANEL

HARDWARE



These low-cost, 19" panels have 64 18-pin connector sockets with either wire wrap (S) or solder fork (R) contact pins. They are shipped with connector blocks installed and pins A and C bussed.

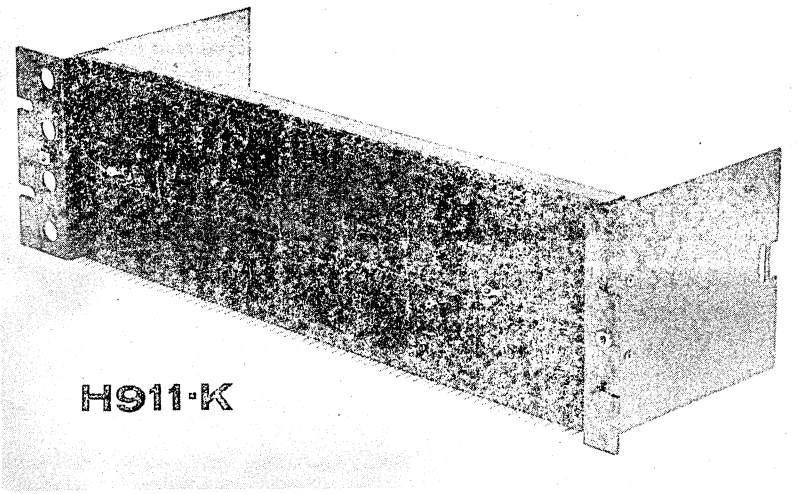
No terminal strips are included in the K943 since power regulators K731 and K732 will normally be plugged in to make power connections, or power connections may be hardwired to pins A and C. If hold-down is required to prevent modules from backing out under vibration, order a pair of end plates —K980 (or K981, 8-1/2" extended-length version of K980). If further extension is needed, an H001 (3/4") may be added as shown in the photo; or, for even further extension, an H002 (2") may be substituted for the H001.

These assemble by means of added nuts on the rear of the rackmount screws. They accept the painted 1907 cover plate making a hold-down system that contacts the module handles and can allow flat Mylar cables to be threaded neatly out the end. Rack space: 5-1/4". See photos showing K943-S, K980, 1907, and H001.

K943-R	— $96
K943-S	— $96
K980	— $ 6
K981	— $10
H001	— $ 7
H002	— $15

H911-J, H911-K, H911-R, H911-S MOUNTING PANEL

HARDWARE



The H911 19 inch mounting panel uses eight H803 connector blocks and houses sixty four, 36 pin connectors. Mechanical dimensions are identical to those of the H910.

The H911 is available with wire wrap pins only, and is generally used for M Series modules.

The unit is a combination of the following parts:

H020 — Mounting frame
H021 — Standoffs
H803 — Connector blocks
933 — Bussing strips (optional with H022 standoff)

The H911-J is not prewired or bussed for power.
The H911-K does have prewired power.
The H911-R similar to H911-J except with 8½" extender end plates.
The H911-S similar to H911-K except with 8½" extender end plates.

933 BUS STRIP — For H911 mounting panel, makes wiring power and register pulse busses easy.

Consult following table for mounting panel options and ordering information.

H911-J — $151
H911-K — $161
H911-R — $151
H911-S — $161

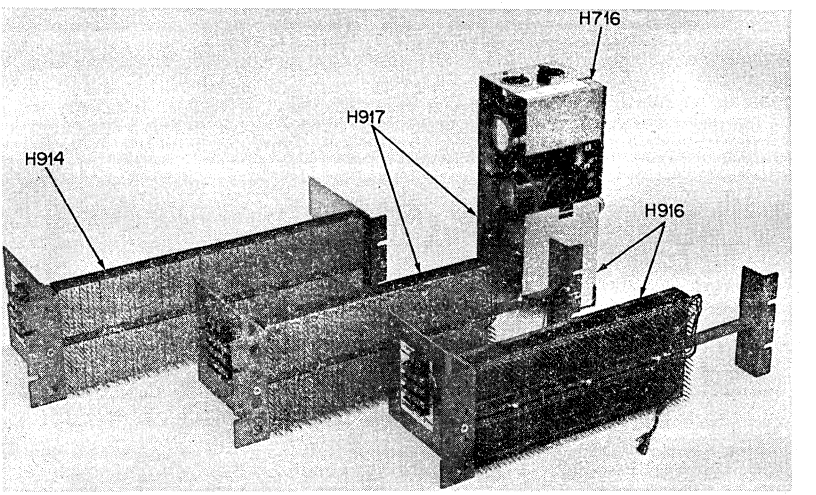
H914, H916 & H917 MOUNTING PANEL

HARDWARE

H914 — This panel houses 8 low density H808 connector blocks. The panel will hold 32 of either A, K, M or W Series modules. It can be used for expanding slot capacity in conjunction with H913 or alone using other voltage supply options, e. g. K731 and K732 combinations. Mechanical characteristics are like those of the H911.

H916 — This panel contains an H716 power supply and 6 H803 (green) connector blocks. The unit provides for forty-eight, 36 pin module slots. Although generally used for mixes of M and A series modules, K and W series modules can also be accommodated.

H917 — This panel is similar to the H916 panel except 6 low density H808 connector blocks are supplied instead of H803 blocks. With these connector blocks, 24 module slots are available, allowing the use of any module series. Electrical and mechanical characteristics are similar to those of type H916 with the exception of the connector blocks.



H913	$270
H914	$125
H916	$270
H917	$260

TABLE OF MOUNTING PANELS WITH & WITHOUT POWER SUPPLY

ORDER NO.		AVAILABLE VARIATIONS						PRICE
PANEL	ORDER LETTER	X	V	F	W	B	P	
H911	J, R	*			*	*		$151
H911	K, S	*			*	*	*	$161
H914	L	*			*	*		$125
H916	M		*		*	*	*	$270
H917	N		*		*	*	*	$260
K943	R	*		*			*	$ 96
K943	S	*			*		*	$ 96

X = NO POWER
V = POWER OPTION
105-125 VAC OR
210-250 VAC
47-63 Hz

P — PREWIRED FOR POWER

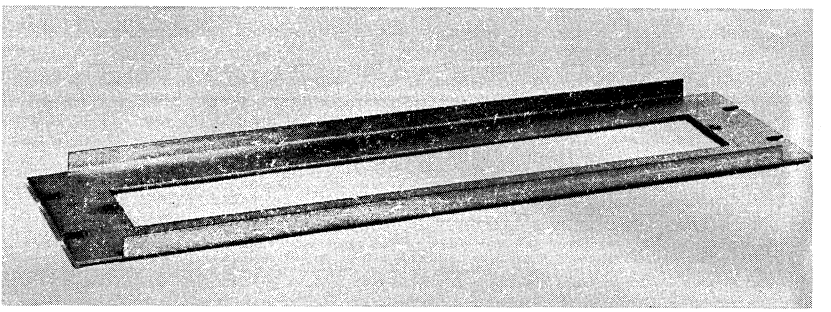
F — SOLDER FORKED CONNECTIONS
W — WIRE WRAP CONNECTIONS

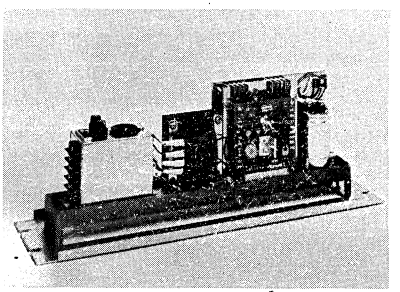
B — POWER INPUT VIA TERMINAL BLOCK. BOTH CONVENTIONAL SCREW CONNECTIONS AND TAPER TABS CAN BE USED

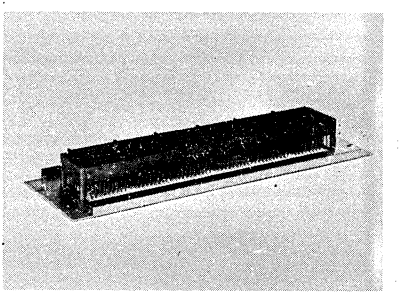
Example Order: H911KX
This describes a Type H020 casting with 8 Type H803 wire wrap connectors and ground wired to a terminal block incorporated into the end plate assembly.

H014
MOUNTING PANEL

HARDWARE





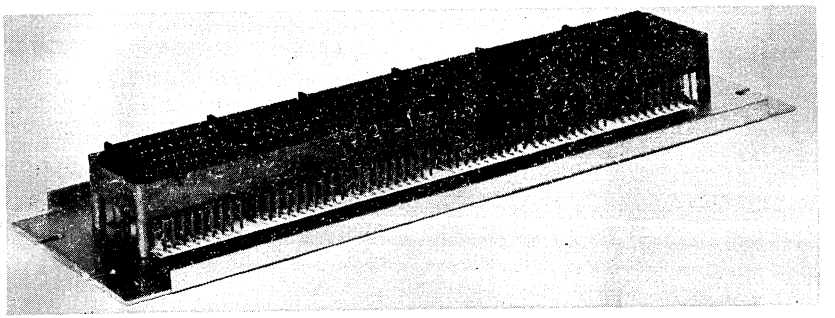


The H014 is a 5-1/4" mounting panel for a standard 19" rack or cabinet. The H014 may be used to mount the H726 power supply or an H933 systems unit casting. When the H933 systems unit casting is mounted on an H014, the back plane pins are available behind the H950-P bezel cover panels.

H014 — $20

H933
SYSTEMS UNIT CASTING

HARDWARE



The H933 Systems Unit Casting provides a way to mount standard DEC connector blocks on a flat panel such as the H014. Casting dimensions are 16½" by 2¼". The H933 may be ordered plain or with connector blocks installed:

Item	*Description*
H933	SYSTEMS UNIT MOUNTING PANEL
H933-A	H933 with 3 H800-W connectors—24-18 pin
H933-B	H933 with 3 H800-F connectors—24-18 pin
H933-C	H933 with 3 H803 connectors—24-36 pin
H933-D	H933 with 3 H808 connectors—12-36 pin

H933 — $15
H933-A — $37
H933-B — $37
H933-C — $54
H933-D — $42

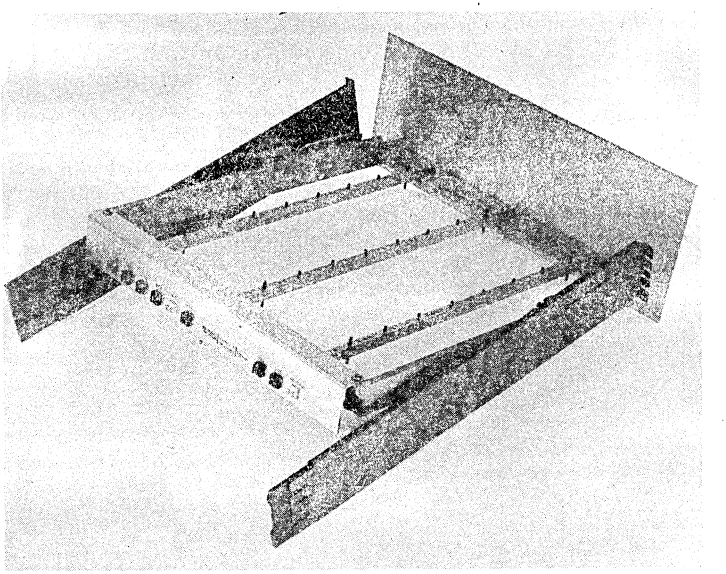
H920
MODULE DRAWER

HARDWARE

The H920 Module Drawer provides a convenient mounting arrangement for a complete digital logic system. The H920 has space for 20 mounting blocks in addition to an H710, or H716 power supply, or 24 mounting blocks without a supply. It accepts H800, H803, and H808 mounting blocks and fits standard 19" racks. Width of the H920 is 16¾", depth is 19" and height is 6¾" including an H921 front panel. The H920 is equipped with a bracket for distributing power within the drawer, or to other drawers or mounting panels. Mounting arrangements are provided for the H921 front panel and H923 slide tracks.

The H921 front panel is designed for use primarily with the H920 Module Drawer. It provides mounting space for switches, indicators, etc. The H921 is pre-drilled and ready to mount on the H920. Height of the H921 is 6¾", width is 19".

H923 chassis slides are intended for use with the H920 Module Drawer. The H923 allows the user to slide the drawer out of the rack and tilt the drawer for easy access to either the pin or module side.



H920—	$170
H921—	$ 10
H923—	$ 75

H925
MODULE DRAWER

HARDWARE

The H925 Module Drawer provides mounting space for H800, H803, and H808 connector blocks to accommodate up to 144 modules. The connector blocks mount pins upward on the H925 for easy access during system checkout.

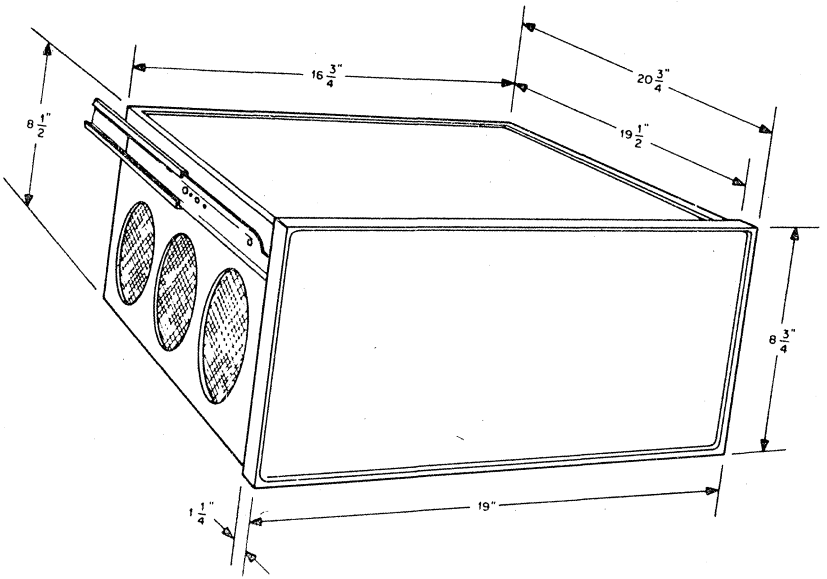
The right side of the H925 is provided with three axial flow fans (300 cfm) which are mounted internally. They provide cooling air flow across the mounted modules.

For power supply mounting in the H925 cabinet, omit 4 connector blocks thereby deleting 32 module slots, when using the H800 or H803 connector blocks. If the H808 blocks are used, 16 module slots are deleted. Mount the power supply externally if all logic mounting space is required.

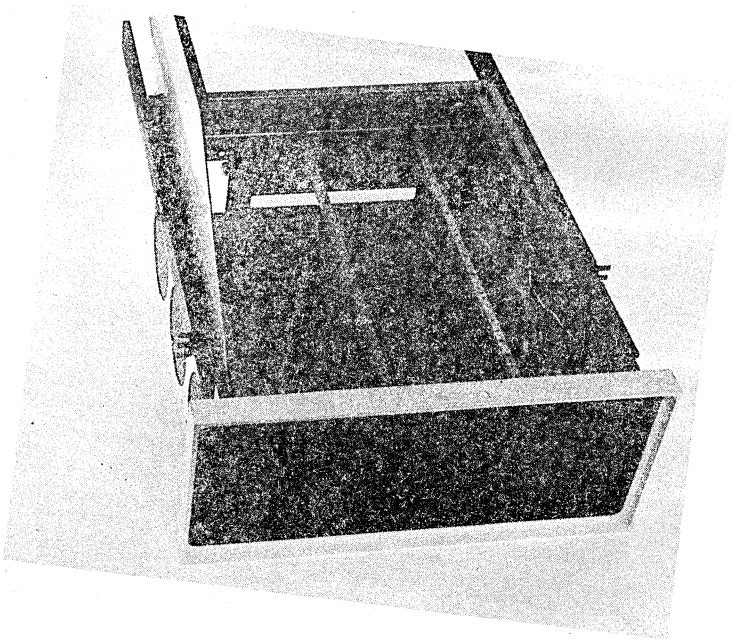
For ease of mounting, the H925 is provided with two non-tilting slides, similar to Grant type SS-168-NT. Considering possible servicing, the H925 should be mounted with enough height for using bottom access.

The H925 includes top and bottom cover plates along with an attractive bezel and front subpanel. The subpanel is made of sturdy 16-guage metal for mounting front panel controls and accessories. The bezel is designed for installing a customer-supplied dress panel. The dress panel should have a thickness of $\frac{1}{8}$". The H925 fits all DEC 19" racks.

H925—$250



H925



452

H941AA
19" MOUNTING PANEL FRAME

HARDWARE

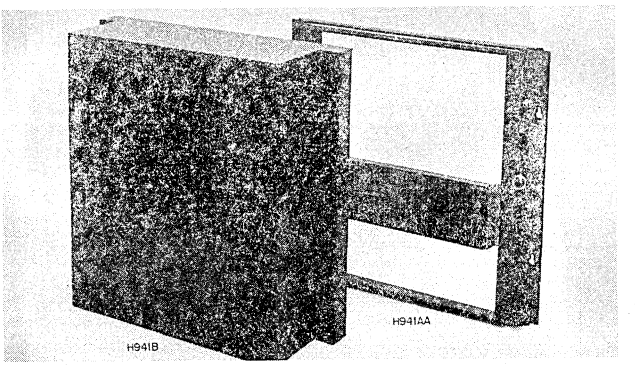
This rugged steel frame holds four 19" x 5¼" mounting panels. A quick-release pin snaps out to allow the two-piece frame to swing open for easy access to the back panel wiring and connections. The construction of this frame allows sufficient rigidity for vertical or horizontal mounting. The Black Tweed finished aluminum cover affords mechanical protection for the circuitry as well as a neatly finished appearance for your digital logic system. The cover attaches to the frame with two thumb-release, positive-grip fasteners.

The H941 AA holds up to 32 H800, H803 and H808 Connector Blocks. It provides up to 256 module slots with H800 and H803 Connector Blocks and 128 slots with the H808's. The frame is designed to accept K943, H911, H914, 1943 Module Panels and H900, H910, H913, H916, H917 panels with power supplies. These panels attach to the pre-tapped frame with 10-32 x ½" machine screws.

Frame Height: 23"
Frame Width: 24"
Overall Depth (Cover and Frame):

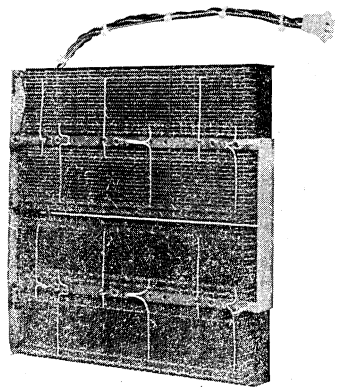
H941-AA—8"
H941-BA—8"
H941-BB—11"

Frame Mounting Hole Centers: 12 x 22½"
Frame Mounting Bolt: ¼" dia.
Weight (Cover and Frame): Approx. 25 lbs.
Cover Material: .093" Sheet Aluminum

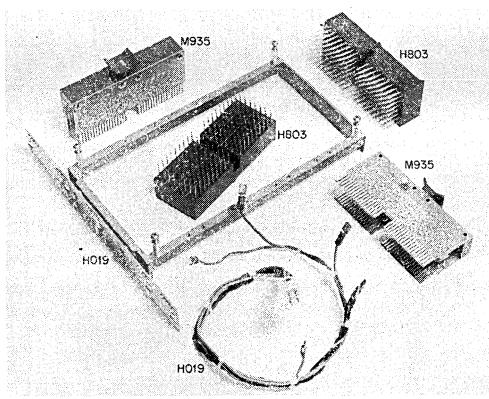


H941-AA (Mounting Panel Frame 19")	— $125
H941-BA (Cover 5½")	— $ 70
H941-BB (Cover 8½")	— $ 80

H9190, H019
PDP-8e INTERFACE HARDWARE



H9190 Mounting Panel—contains M Series connector blocks with 8/e-type packaging for PDP-16 options or standard M Series modules. Also included are the 8/e power wiring harness and power bus board. There is M Series power bussing for all but the four slots in the first column. Four mounting spacers allow the H9190 to be easily mounted in the second half of an 8/e chassis.



H019 Mounting Bar—an aluminum casting with the power bus board and power wiring harness. It also includes four mounting spacers for mounting in an 8/e chassis. Up to ten connector blocks of any type may be accommodated by this frame.

H950, H954 AND H957 SERIES CABINETS

HARDWARE

The Logic Products Group offers standard 19" mounting cabinet frame assemblies in two series—H950-AA (68 25/32" high x 25" deep x 63" mounting space) and H957 (50" high x 25" deep x 42" mounting space).

The above-listed cabinet frame assemblies offer complete flexibility and expandability to present and future DEC customers, single users, multiple users and original equipment manufacturers. The enclosure area in these cabinet frames is adaptable to customer-designed hardware, logic module racks, power supplies, computer systems, and peripherals.

The cabinet frame assemblies are constructed of rugged 12- and 13-gauge steel. The frame uprights have 9/32" holes drilled at standard EIA spacing (5/8-5/8-1/2) the full length of the 42" and 63" front and rear mounting panel heights.

Note: The cabinets described in the following pages, Cabinet A through H, do not include in their listed price the front cabinet mounting options.

Cabinet customers have the option of selecting the type of front cabinet hardware mounting of their choice. Consult the H950 parts list for prices and add to basic cabinet price listed.

Cabinet A

1—H950-AA 19" Mounting Frame (71 7/16" w/casters x 25" x 63"), includes mounting hardware
1—7406782 Kickplate (Lower Cab Trim)
*1 pr. H952-BA Stabilizer Feet
1—H952-FA Leveler Set (4)
*1—H950-LA Logo Frame Panel
2—H952-AA End Panels
1—H950-BA Full Door Rear (Right Hanging)
1—H952-EA Caster Set (4)
1—H952-CA Fan Assembly

Cabinet A—List Price—$411.00

OPTION: Front Cabinet Mounting/Cover Panels—
H950-P (5 1/4") and/or H950-Q (10 1/2")

* H950-SA Filter (for fan) Assembly
* See Special Considerations Sections 5, 8 and 13.

Cabinet B

1—H950-AA 19" Mounting Frame (71 7/16" w/casters x 25" x 63") includes mounting hardware
1—7406782 Kickplate (Lower Cab Trim)
*1 pr. H952-BA Stabilizer Feet
1—H952-CA Fan Assembly
1—H952-EA Caster Set (4)
1—H952-FA Leveler Set (4)

*1—H950-LA Logo Frame Panel
2—H952-AA End Panels
1—H950-DA Mounting Panel Rear Door (Right Hanging)
1—H950-FA Mounting Panel Door Skin

Cabinet B—List Price—$431.00

OPTION: Cabinet Front Mounting/Cover Panels—
H950-Q (10 1/2") and/or H950-P (5 1/4")

* H950-SA Filter (for fan assembly)
* See Special Considerations, Sections 5, 8, and 13.

Cabinet C

1—H950-AA 19" Mounting Frame (71 7/16" w/casters x 25" x 63") includes mounting hardware
1—7406793 Kickplate (Lower Cab Trim)
*1—H950-LA Logo Frame Panel
1—H952-CA Fan Assembly
1—H952-EA Caster Set (4)
1—H952-FA Leveler Set (4)
2—H952-AA End Panels
1—H950-DA Mounting Panel Door (Right Hanging)
1—H950-BA Full Door Rear (Right Hanging)

Cabinet C—List Price—$437.00

OPTION: Front Cabinet Mounting/Cover Panels—
H950-P (5 1/4") and/or H950-Q (10 1/2")
Short Doors—See H950 Cabinet Parts List—
H950-HA—HK—short door selection.

* H950-SA Filter (for fan assembly)
* See Special Considerations, Sections 5, 8, and 13.

Cabinet D

1—H950-AA 19" Mounting Frame (71 7/16" w/casters x 25" x 63") includes cover filter and mounting hardware
1—7406793 Kickplate (Lower Cab Trim)
1—H952-CA Fan Assembly
*1—H950-LA Logo Frame Panel
1—H952-EA Caster Set (4)
1—H952-FA Leveler Set (4)
2—H952-AA End Panels
1—H950-BA Full Door Rear (Right Hanging)

Cabinet D—List Price—$390.00

OPTION: Front Cabinet Mounting—Cover Panels—
H950-P (5 1/4") and/or H950-Q (10 1/2")
Short Doors—See H950 Parts List—
H950-HA—HK—Short Door Selection.

* H950-SA Filter (for fan assembly)
* See Special Considerations, Sections 5, 8, and 13.

Cabinet E,
Same as Cabinet D, except:
1—H950-DA Mounting Panel Door Rear (Right Hanging) and
1—H950-FA Mounting Panel Door Skin,
are substituted for:
1—H950-BA Full Door Rear (Right Hanging)

Cabinet E—List Price—$410.00

OPTIONS: Front Cabinet Mounting—
Same as listed for Cabinet D

Cabinet F (H961-A)
Add-on—Designed for combining two or more cabinets, in the H950 Series. No end panels are required (H952-AA).
1—H950-AA 19" Mounting Frame (71 7/16" w/casters x 25" x 63"), includes mounting hardware
1—74-6793 Kickplate (Lower Cab Trim)
1—H950-FA Mounting Panel Door Skin
1—H950-EA Mounting Panel Door Plenum (Left Hanging)
1—H952-CA Fan Assembly
1—H952-EA Caster Set (4)
1—H952-FA Leveler Set (4)
*1—H950-LA Logo Frame Panel
1—H952-GA Filler Strip (Front and Rear)

Cabinet F—List Price—$340.00

OPTIONS: Front Cabinet Mounting
Same as used for Cabinet D.

* See Special Considerations Section 13, 2

Cabinet I—Short Cabinet Series
1—H957-AA 19" Mounting Frame (50" w/casters x 25" x 42") includes mounting hardware
1—H957-BA Full Door—Rear Mounting (Right Hanging)
1—H957-DA Mounting Panel Door—Rear Mounting (Right Hanging)
1—H957-FA End Panel (Right Hanging)
1—H957-FB End Panel (Left Hanging)
1—H957-LA Logo Frame Panel
1—H957-SA Filter
*1—H957-HA Fan Assembly
*1 pr H952-BA Stabilizer Feet
1—H952-EA Caster Set (4)
1—H952-FA Leveler Set (4)
1—74-6782 Kickplate

* See Special Considerations Section 5, 14

Cabinet I—List Price—$476.00

OPTION: Front Cabinet Mounting/Cover Panels H950-P (5¼") and/or H950-Q (10½").

Cabinet J

1—H957-AA 19" Mounting Frame (50" w/casters x 25" x 42") includes mounting hardware
1—H957-BA Full Door—Rear Mounting (Right Hanging)
1—H957-FA End Panel (Right Hanging)
1—H957-FB End Panel (Left Hanging)
1—H957-LA Logo Frame Panel
*1—H957-HA Fan Assembly
1—H952-EA Caster Set (4)
1—H952-FA Leveler Set (4)
1—74-6793 Kickplate
1—H957-SA Filter

* See Special Considerations Section 14

Cabinet J—List Price—$419.00

OPTION: Front Cabinet Mounting/Cover Panels H950-P (5¼") and/or H950-Q (10½"). Short Doors from H950-AA (21") through H950-HF (42") only.

OPTION: Front Cabinet Mounting/Cover Panels H950-P (5¼") and/or H950-Q (10½").
Short Doors from H950-HA (21") through H950-HF (42") only.

Cabinet K

Add On Cabinet—Designed for Combining Two or More Cabinets in the H957 Series—No End Panels Required (H957-FA, FB).

1—H957-AA 19" Mounting Frame (50" w/casters x 25" x 42") includes mounting hardware
1—H957-BA Full Door—Rear Mounting (Right Hanging)
1—H957-HA Fan Assembly
1—H957-EA Mounting Panel Door (Plenum) Rear Mounting (Left Hanging)
1—H952-EA Caster Set (4)
1—H952-FA Leveler Set (4)
1—74-6793 Kickplate
1—H957-LA Logo Frame Panel
1—H957-SA Filter
1—H957-GA Filler Strip Set (3) Front, Rear and Top
*1—H957-HA Fan Assembly
1—H954-CA Fan Assembly (Bottom Mounted)

* See Special Considerations Section 14

Cabinet K—List Price—$365.00

Cabinet Specials

Non-standard cabinet configurations are made to order by using the two basic cabinet frame assemblies—H950-AA (68 25/32" x 25" x 63"), H954-AC (49 8/16" x 25" x 42 1/16") and H957-AA (47 12/16" x 25" x 42")

It is recommended that all cabinet specials have the following basic parts:

1. H950 Series Cabinet
   A—H950-AA Frame (71 7/16" height w/casters x 25" x 63")
   B—H952-EA Caster Set (4)
   C—H952-FA Leveler Set (4)
2. H954 Series Cabinet
   A—H954-AC Frame (51 12/16" height w/casters x 25" x 42")
   B—H952-EA Caster Set (4)
   C—H952-FA Leveler Set (4)
   D—H954-UA Cabinet Cover
3. H957 Series Cabinet
   A—H957-AA Frame (50" height w/casters x 25" x 42")
   B—H952-EA Caster Set (4)
   C—H952-FA Leveler Set (4)

Consult H950, H954 and H957 Cabinet Parts List to complete special cabinet configuration. **Cabinets are shipped assembled.**

Special Considerations
Before ordering a cabinet, the following should be considered:

1. If logo frame H950-LA or H950-LB is used, short doors and/or cover panels H950-P (5¼")—H950-Q (10½") can be used for cabinet front mounting.
2. When ordering a cabinet to add to an existing system with a H950-AA frame assembly, or in joining two or more cabinets front and rear, filler strip H952-GA is used. (See Cabinet F and Cabinet K.)
3. If power supplies with meters or switches are mounted to the rear mounting panel, (plenum) door H950-DA (RH) or H950-EA (LH), a full door H950-DA (RH) or H950-LA (LH) is needed. (See Cabinet C.)
4. The mounting panel door skin 950-FA bolts to the plenum door H950-DA (RH) or H950-EA (LH) and is used in place of a full door when hardware mounted to the plenum door (mounting panel door) does not require servicing. (See Cabinet B, E, and F.)
5. When using stabilizer feet H952-BA, the kickplate #7406782 (lower cab trim) is used. If short doors are used, special mounting is required.
6. When using fan assembly, indicate direction of airflow (up or down).
7. When using short doors, make certain that the equipment for cabinet installation will not interfere with door height.
8. The filter H950-SA for use with H952-CA fan assembly should be ordered only for fans that are to be used for airflow intake.
9. Fan assembly specifications for H952-CA and H957-AA are 500 CFM.
10. H952-EA casters add 2 4/16" to cabinet frame assembly height.
    H950-AA—Cabinet frame height w/casters—71 7/16".
    H957-AA—Cabinet frame height w/casters is 50".
11. Short doors H950-HA (21") through H950-HK (63") series—Dimensions of the doors listed in Parts List only cover mounting panel height; e.g., the H950-AA cabinet frame has 63" mounting panel height. Using a H950-HA (21") short door would leave 42" of mounting panel space.
12. Doors for rear mounting are listed as right hanging in Cabinets A, B, C, D, E. Left hanging doors may be substituted by changing suffix letters as listed in Parts List.
    Key: (RH)—Right Hanging
    (LH) Left Hanging
13. The H950-LA Logo Frame Panel is an aluminum extrusion that can be supplied with a blank adhesive inlay strip in assorted color combinations. "When the inlay strip is ordered as part of a cabinet, there is no charge for the inlay. Inlay strips ordered separately are priced at $15.00 each." The adhesive inlay strip designed for PDP-8/E, PDP-11 require the H950-LB Logo Frame or H957-LA.
    1. Adhesive inlay color strip available for use with H950-LA frame panel
        a. Brown/Yellow
        b. Navy Blue/Bright Copen Blue
        c. Bright Chartreuse/Lime Peel
    2. Adhesive inlay color strips available for use with H950-LB panel.
        a. Terra Cotta/Amber
        b. Magenta/Bright Rose
14. The Fan Assy. H957-HA may be mounted on top of rear frame or rear mounting door. When mounted to bottom of frame or mounting panel door, a bottom cover plate H957-JA must be used for upward air flow through cabinet.

Color
Basic color of cabinet hardware is black. Gray is used for end panels and the inlay of the cover panels.

Customized painting will be accepted with a minimum lot release of 10 cabinets at an extra charge of $10 per cabinet painted. The customer must supply a color chip for color desired. DEC will not inventory custom painted cabinets without special consideration.

Order should be sent to Module Marketing Services. No cabinet hardware will be accepted for credit or exchange without the prior written approval of DEC, and without the proper return authorization number (RA#). **No cabinet returns are accepted on special paint orders.**

Prices do not include state or local taxes. Prices, discounts, and specifications are subject to change without notice.

Cabinet Discount Schedule
The following discount schedule is for cabinet purchases only. The discount is computed from the total list price of cabinet parts purchased. On blanket purchase orders, minimum releases of ten units (cabinets) or balance is required.

Sale in Dollars	Discount
$ 500 - $ 999	8%
1000 - 1499	12%
1500 - 2499	20%
2500 - 4999	25%
5000 - 7499	26%
7500 - 9999	28%
$10,000 - And up	30%

PARTS AND PRICE LIST H950 SERIES CABINET

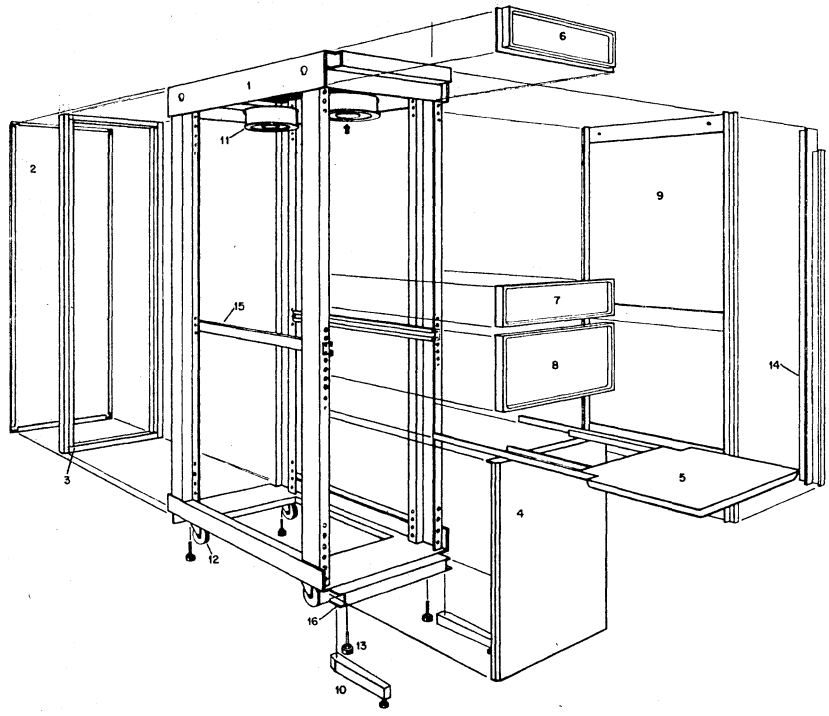
Catalog No.	Description	List Price
H950-AA	Frame, 19" wide, 69" hi, 25" deep, 63" mounting panel, includes mounting hardware.	$163.00
H950-BA	Full Door (RH), front and rear door mounting	47.00
H950-CA	Full Door (LH), front and rear door mounting	47.00
H950-DA	Mounting Panel (Plenum) Door, (RH) rear mounting	47.00
H950-EA	Mounting Panel (Plenum) Door, (LH) rear mounting	47.00
H950 FA	Mounting Panel Door Skin	20.00
H950-HA	Short Door (covers 21" mounting)	48.00

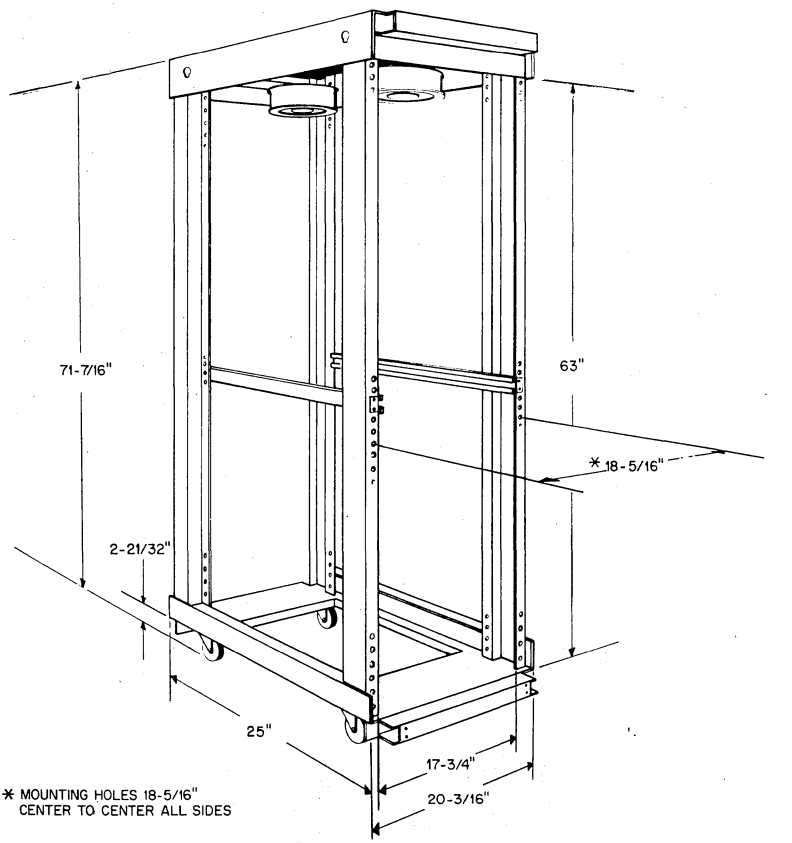
H950-HB	Short Door (covers 22¾" mounting)	48.00
H950-HC	Short Door (covers 26¼" mounting)	48.00
H950-HD	Short Door (covers 31½" mounting)	48.00
H950-HE	Short Door (covers 36¾" mounting)	48.00
H950-HF	Short Door (covers 42" mounting)	48.00
H950-HG	Short Door (covers 47¼" mounting)	48.00
950-HH	Short Door (covers 52½" mounting)	48.00
H950-HJ	Short Door (covers 57¾" mounting)	48.00
H950-HK	Short Door (covers 63 "mounting)	48.00
H950-G	Table Top Assembly (19" wide, 21 7/32" x 1¾")	50.00
H950-LA	Frame Panel Aluminum	9.00
H950-LB	Frame Panel Plastic	7.00
H950-PA	5¼" Bezel Cover Panel	8.00
H950-QA	10½" Bezel Cover Panel	11.00
H950-SA	Filter (for Fan Assembly)	4.00
*H952-AA	End Panel (require 2 per cabinet)	57.00
H952-BA	Stabilizer Feet (pair)	23.00
H952-CA	Fan Assembly (specify airflow), top mounted	40.00
H952-EA	Caster Set (4)	7.00
H952-FA	Leveler Set (4)	2.00
H952-GA	Filler Strip (front and rear), joining two cabinets	44.00
7406782	Kickplate (use with H952-BA)	5.00
7406793	Kickplate (Lower Cab Trim)	8.00
12-9154	Mounting Slides	25.00
12-9703	Tilt Slides	52.00
70-5909	AC Distribution Panel	50.00

PART DESIGNATIONS

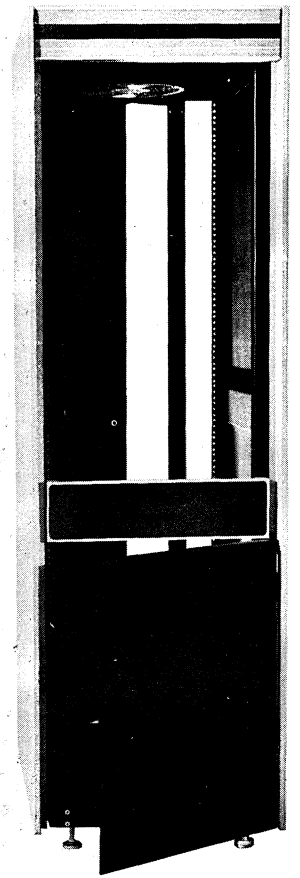
H950 SERIES CABINET

1. Frame
2. Full Door
3. Mounting Panel (Plenum) Door
4. Short Door
5. Table Top Assembly (19" wide, 21 7/32" x 1¾")
6. Frame Panel
7. 5¼" Bezel Cover Panel
8. 10½" Bezel Cover Panel
9. End Panel (require 2 per cabinet)
10. Stabilizer Feet (pair)
11. Fan Assembly (specific airflow), top mounted
12. Caster Set
13. Leveler Set
14. Filler Strip (front & rear), joining two cabinets
15. Slides
16. Kickplate

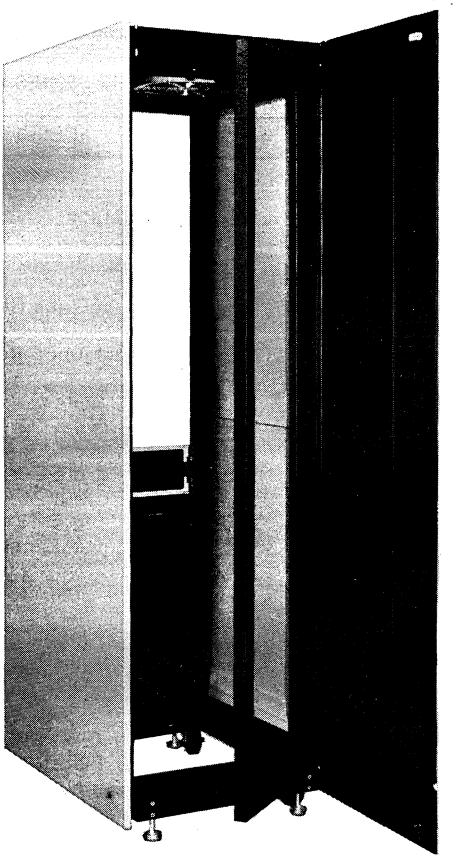




H950 CABINET DIMENSIONS



Front view of H950 frame.



Rear view of H950 frame.

PARTS AND PRICE LIST

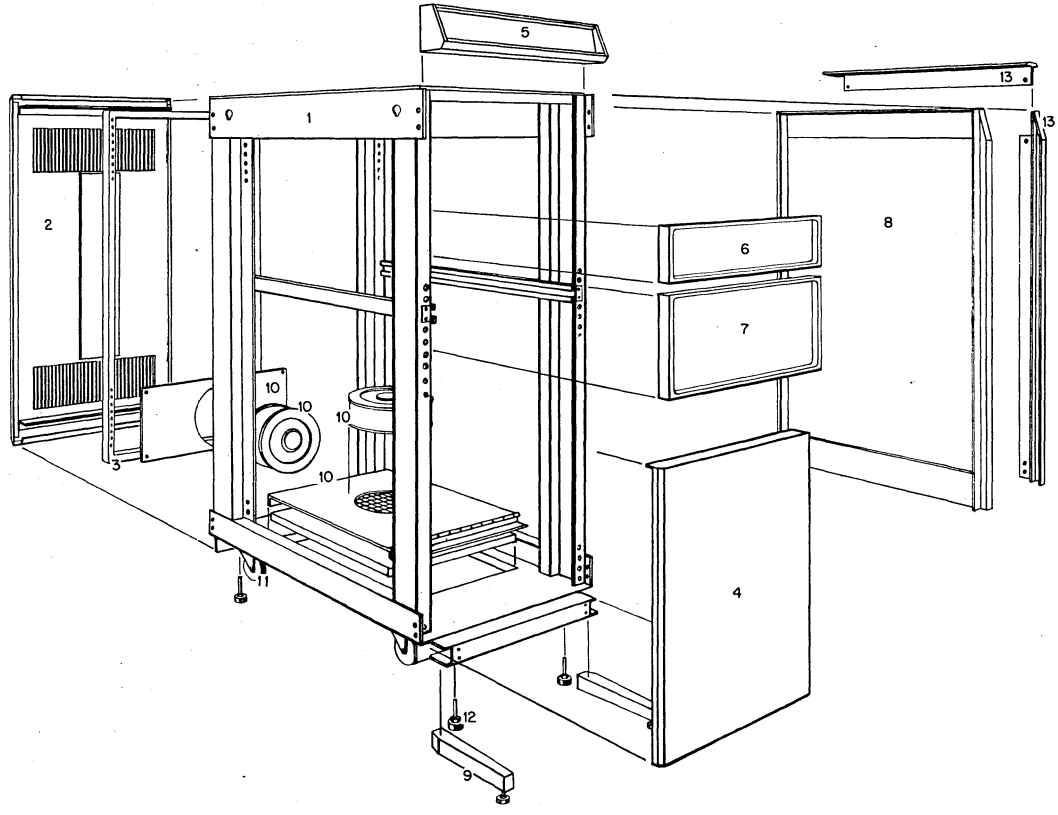
H957 SERIES CABINET

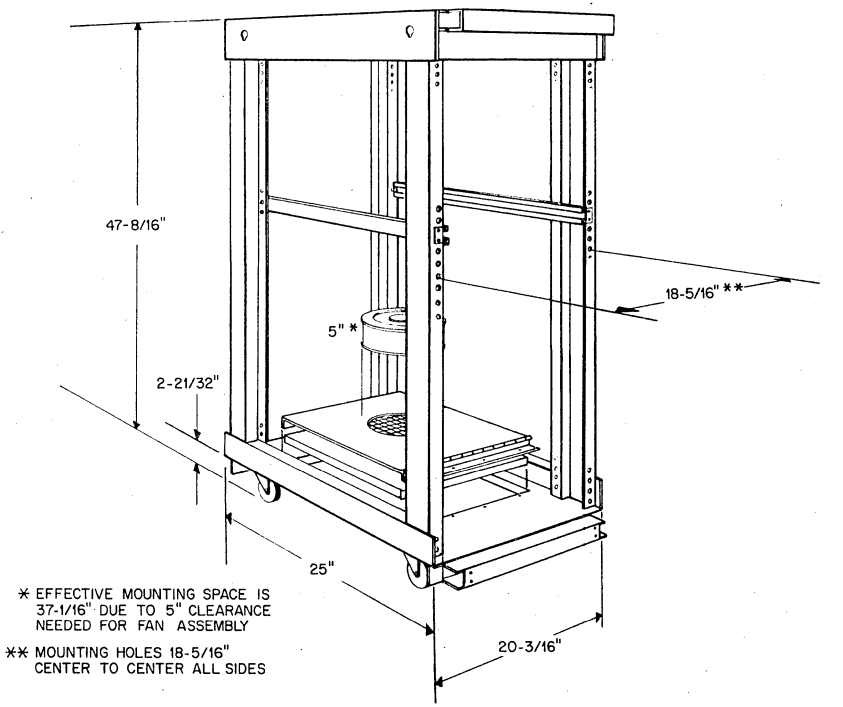
CATALOG NO.	DESCRIPTION	LIST PRICE
H957-AA	Frame 19" Wide 47 8/16" High 25" Deep, 47" Mounting Panel includes Mounting Hardware	$142.00
H957-BA	Full Door Rear Mounting (Right Hanging)	60.00
H957-CA	Full Door Rear Mounting (Left Hanging)	60.00
H957-DA	Mounting Panel Door Rear Mounting Plenum (Right Hanging)	36.00
H957-EA	Mounting Panel Door Rear Mounting Plenum (Left Hanging)	36.00
H950-HA	Short Door (Covers 21" Mounting)	48.00
H950-HB	Short Door (Covers 22¾" Mounting)	48.00
H950-HC	Short Door (Covers 26¼" Mounting)	48.00
H950-HD	Short Door (Covers 31½" Mounting)	48.00
H950-HE	Short Door (Covers 36¾" Mounting)	48.00
H950-HF	Short Door (Covers 42" Mounting)	48.00
H950-PA	5¼" Bezel Cover Panel	8.00
H950-QA	10½" Bezel Cover Panel	11.00
H952-BA	Stabilizer Feet (Pair)	23.00
H952-EA	Caster Set (4)	7.00
H952-FA	Leveler Set (4)	2.00
H957-FA	End Panel (Right Hanging)	63.00
H957-FB	End Panel (Left Hanging)	63.00
H957-GA	Filler Strip Set (3) Top, Front and Rear	36.00
H957-HA	Fan Assembly (500 CFM)	50.00
H957-JA	Bottom Cover Plate	9.00
H957-LA	Logo Frame Panel	20.00
H957-SA	Filter	4.00
74-06782	Kickplate (use with H952-BA)	6.00
74-06793	Kickplate (Lower Cabinet Trim)	8.00

PART DESIGNATIONS

H957 SERIES CABINET

1. Frame
2. Full Door
3. Door Mounting Panel
4. Short Door
5. Logo Frame Panel
6. 5½" Bezel Cover Panel
7. 10½" Bezel Cover Panel
8. End Panel
9. Stabilizer Feet
10. Fan Assemblies
11. Caster Set
12. Leveler Set
13. Filler Strip Set

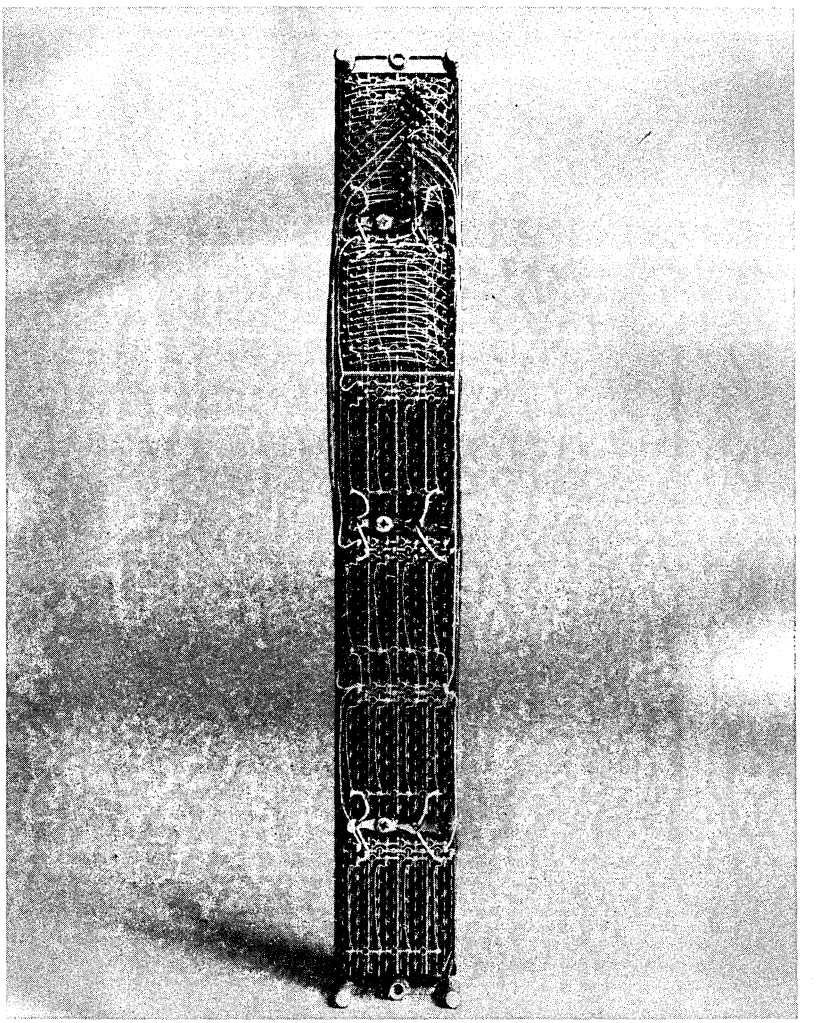




H957 CABINET DIMENSIONS

BB11
SYSTEM INTERFACING UNIT

HARDWARE



The BB11 is a prewired system unit used for general interfacing. It consists of three 288-pin blocks assembled end-to-end in a casting which can be mounted in the basic PDP-11 box or extension box. Six of the module slots are used for b[illegible] power connectors. These slots are:

POWER-A3
UNIBUS-A1-B1 and A4-B4
+5 Volts to all A2 pins
−15 Volts to all B2 pins (except in slots A1, B1, A4 and B4)
Ground to all C2 and T1 pins.

BB11 POWER PIN ASSIGNMENTS

PIN	POWER
A1	−15V
A2	+5V
B1	−15V
B2	−15V
C1	−15V
C2	GND
D1	−15V
D2	GND
E1	−15V
E2	GND
F1	−15V
F2	GND
H1	−15V
H2	+5V
J1	−15V
J2	+5V
K1	−15V
K2	+5V
L1	−15V
L2	+5V
M1	−15V
M2	+5V
N1	GND
N2	−25V
P1	GND
P2	LTC L
R1	GND
R2	ACLO L
S1	GND
S2	DCLO L
T1	GND
T2	+8V
U1	GND
U2	+8V
V1	GND
V2	+8V

NOTE

POWER IS IN MODULE SLOT A3 OF ALL SYSTEM UNITS MOUNTED IN BA11 MOUNTING BOXES EQUIPPED WITH H720 POWER SUPPLIES.

WIRE WRAPPING SERVICE

The electronics industry has long been aware of the many advantages of wire wrapping over soldering for interconnecting electronic circuits. Soldering introduces numerous human errors and presents problems of cold solder joints, flux removal and overheating sensitive components. Automatic, computer-controlled wire wrapping, however, not only eliminates the problems associated with soldering but adds many technical and economic benefits unattainable with soldering. Automatic wire wrapping provides extremely high reliability, high production rates, elimination of human error, long-life connections, simple mechanical inspection techniques, high density wiring, rework ability, reduced labor and reduced inspecting time.

Digital Equipment Corporation has developed an extensive high-production wire wrapping capability and offers to its customers the significant cost savings of automatic wire wrapping. Digital can provide a full wire wrapping service and our "Smooth-Flo" processing insures control at each step in the process.

DIGITAL automatically verifies the correctness of the wiring on each panel with its computer-controlled Automatic Wire Test equipment. This verification is a standard part of DIGITAL's wire wrapping service and is provided at no charge. The only restriction is that the size of the panel be limited to four connector blocks high by ten connector blocks wide. No price reduction is given for elimination of the verification service.

For additional information on DIGITAL's wire wrap service, write for wire wrap data sheets available from Logic Products, Digital Equipment Corporation, Maynard, Massachusetts 01754.

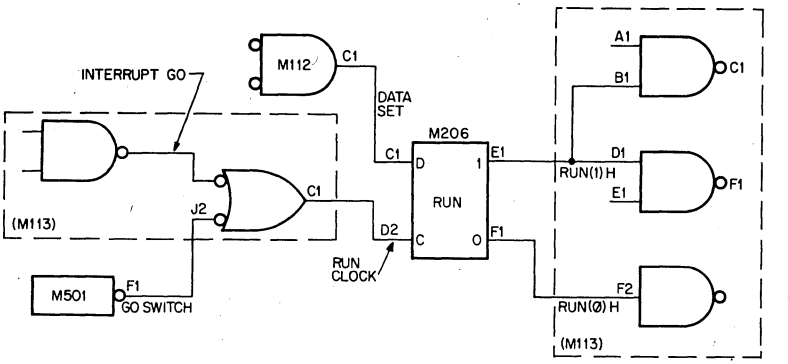
Customer Requirements

A wire listing prepared by the customer on Digital Form DR22A must accompany the purchase order, specifying which mounting panels are being purchased. In addition, if any special bussing is needed, a copy of the updated bussing diagram must also accompany the purchase order. It is extremely important that complete wire listing and bussing information be received with each order. Pricing of a wire wrapping order cannot be completed until the source deck has been processed and buss print received. These are needed to determine wire count and number of points to be bussed.

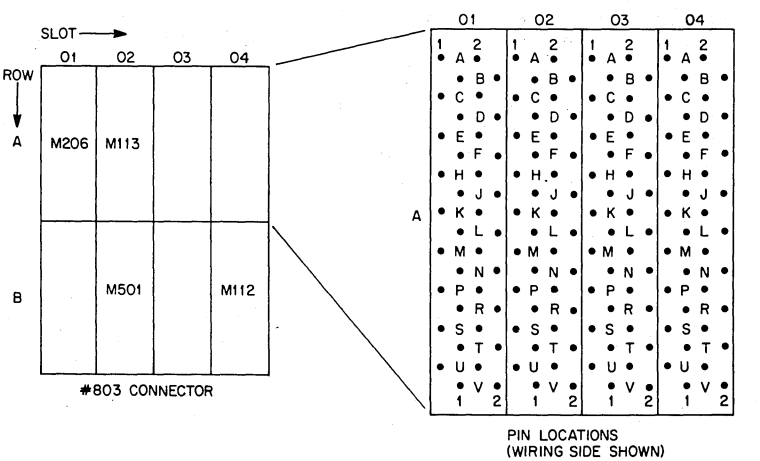
For the purpose of identifying specific pins and module slots for wire listings, the panels or connectors are viewed from the wiring side as shown.

The wiring list is compiled from the logic design diagrams together with module utilization charts. The pin numbers, signal names and logic module type are specified for each of the logic functions on the diagram as shown.

The location of a module and the utilization of each of the logic functions are compiled on the Module Utilization drawing. These drawings prevent the use of the same logic circuit more than once.



LOGIC DESIGN DIAGRAM



MODULE UTILIZATION DIAGRAM

Wire listing form DR22-A should be filled out in the following manner to facilitate processing:

DR22-A for LOGIC 1

A	B	C	DR22-A
SIGNAL NAMES	RUN PIN	LINE NO. OR REMARKS	LINE NO.
Run Clock	A02C1		
	A01D2		
Data Set	B04C1		
	A01C1		
Run 1	A01E1		
	A02B1		
Run 0	A01F1		
	A02F2		
GO SW	B02F2		
	A02J2		

Column Designations

A. Signal—Identifies a particular run and can be any alphanumeric character up to a maximum of 22 characters.

NOTE: 1. Only one name may be used for a particular wire run

2. Like signals should be combined if on different sheets, or they will be combined later by computer processing.

B. Run Pin—Four or five digits (see Absolute Pin Identification) lists the address of each pin in a wire run. (May express maximum of 65 pins for any one run.) These addresses do not have to appear in order and, along with their signal name, can be on separate sheets.

C. Remarks and Line Number—Available for convenience of user and need not be filled in.

SPECIAL SERVICES

The customer will receive one copy each of the Name Sort and Pin Sort lists at no charge.

DIGITAL will perform special bussing where required. The rate for this is $0.20 (including the cost of the buss strip) per point.

Delivery

The normal delivery time for wire wrapped panels is two to four weeks after receipt of the purchase order, accurate source inputs (card or wire list), and updated bussing diagram if special bussing is required.

On repeat orders for the same panels and wiring configuration, normal delivery time is often reduced to almost half that of initial processing time.

*30 ga. Set-up Charge	$125.00
*24 ga. Set-up Charge	175.00
30 ga. Wire/Cost per Wire (2 connections)	.30
24 ga. Wire/Cost per Wire (2 connections)	.25

.20 per point for special bussing, including buss strip

* One time charges are not discountable

STANDARD CHARGES FOR SMOOTH FLO SERVICE

Excluding hardware costs, the following price schedule applies to wire wrap services from DEC:

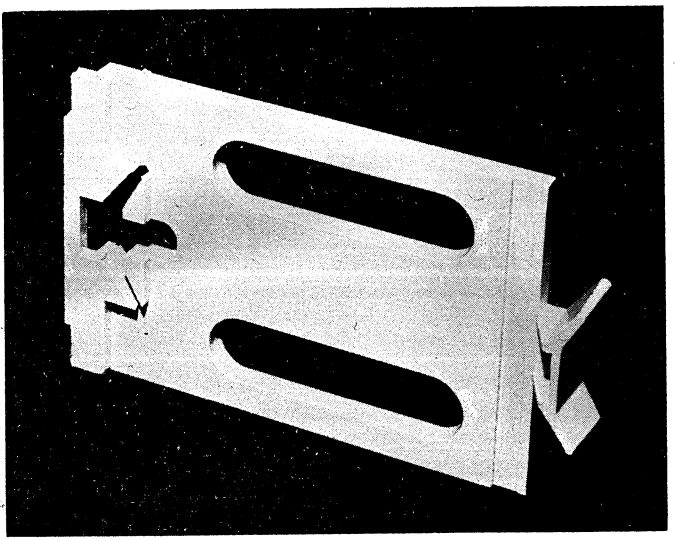
24 Gauge Wire One Time set-up charge	$175(1)
cost per wire	25¢*
30 Gauge Wire One Time set-up charge	$125(2)
cost per wire	30¢*
Special Bussing	
cost per point	20¢

*2 connections

NOTE (1) Over 1000 to 2000 wires one time set-up charge $250.
(2) Over 1000 to 2000 wires one time set-up charge $225.
Over 2000 wires one time set-up charge for 24 gauge and 30 gauge wire will be determined at the time of the inquiry.

H850, H852, H853 MODULE ACCESSORIES

SUPPORT HARDWARE



H850 HANDLE EXTENDER

The H850 Handle Extender mounts over the existing handle of a standard height module to provide compatibility with the 8½ inch extended modules.

When using two or more W940, W941, W942, W943, W950 or W951 boards in parallel in logic connector blocks, rigidity of the boards is maintained by using the H852 rib type holder between board handles 1 and 2, 3 and 4, and using the H853 non-rib type holder between board handles 2 and 3.

H850 (pkg/10)	$10.00
H852 (pkg/25)	$ 7.00
H853 (pkg/25)	$ 7.00

937
MODULE ACCESSORY

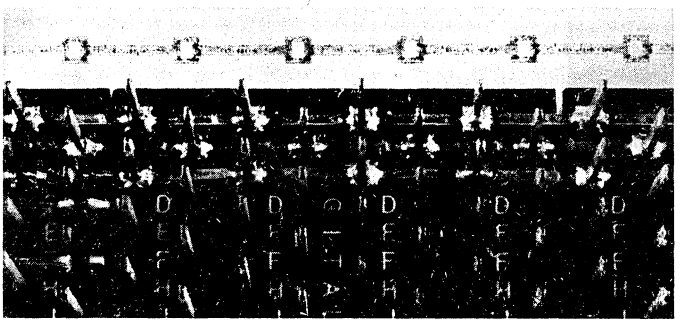
SUPPORT HARDWARE

The 937 is a package of 25 blank gray module handles with eyelets to permanently install them on a blank copper-clad board or a wire wrap board by the user. The purpose of the handles is to allow the user to put his own identification on the module if he so desires. The handles are compatible with all DEC modules.

937 — $7.00 Pkg/25

932, 933, 934, 935, 936, 939 H810, H810-D, H810-E, H811, H812, H813, H814 WIRING ACCESSORIES

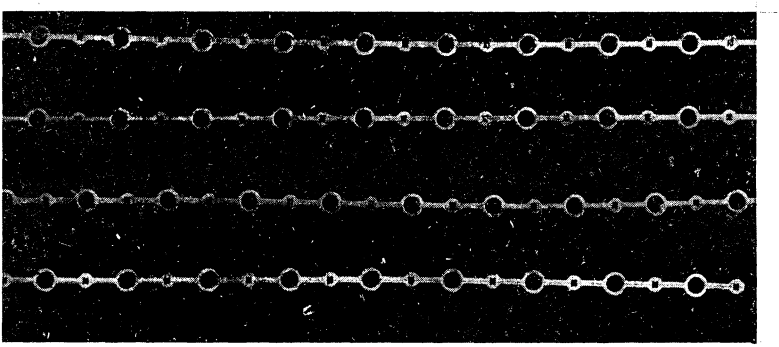
ACCESSORIES



932 BUS STRIP

Simplifies wiring of register pulse busses, power, and grounds. Same as used in K943 with H800 blocks.

932 — $0.60 each



933 BUS STRIP

Simplifies wiring of power, ground and signal busses on mounting panels using H803 connectors.

933 — $1 each

934 WIRE WRAPPING WIRE

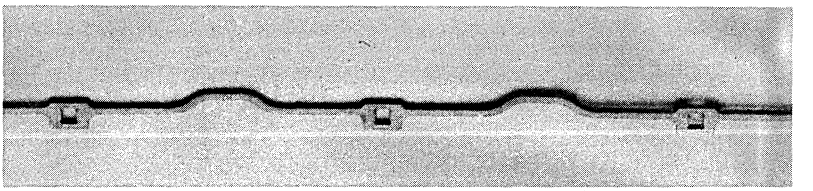
1000 ft. roll of 24 gauge solid wire with tough, cut-resistant insulation. (Use Teflon insulated wire instead for soldering.)
For use with H800 connectors.

934 — $50

935 WIRE-WRAPPING WIRE

1000 foot roll or 30 gauge insulated solid wire for use with H803 connectors.

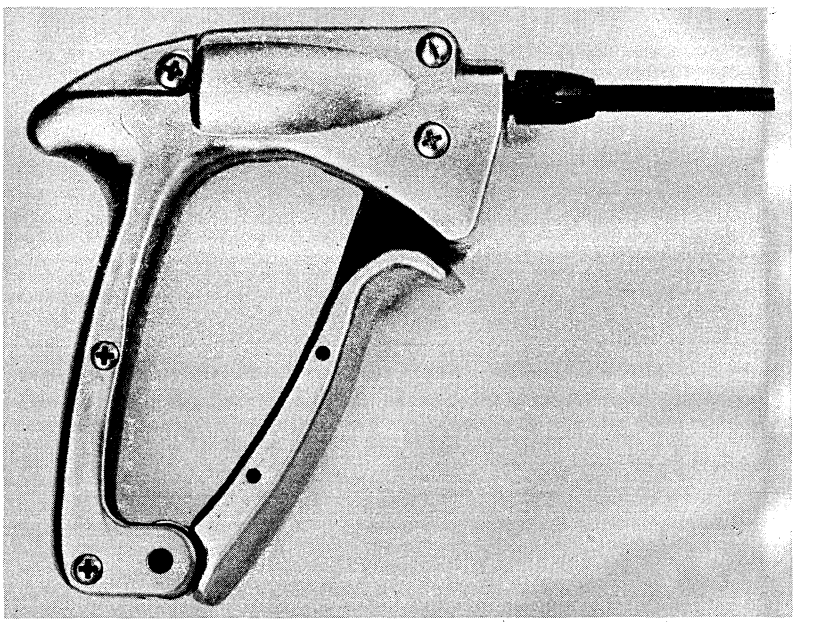
935 — $60



939 BUS STRIP

For use with H808 connectors.

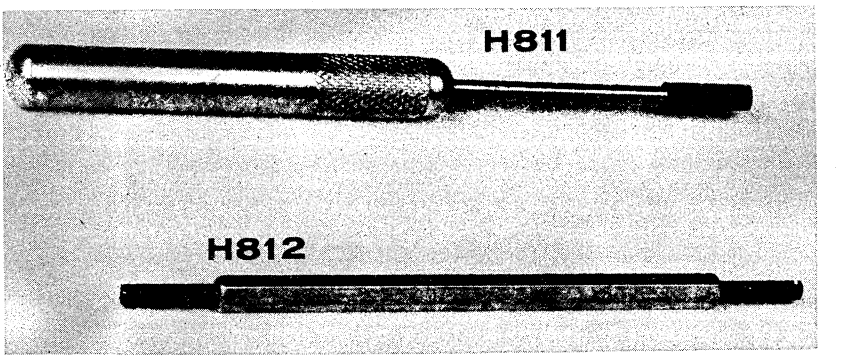
939 — $1



H810 PISTOL GRIP HAND WIRE WRAPPING TOOL

The type H810 Wire Wrapping Tool is designed for wrapping #24 solid wire on Digital-type connector pins. The H810 Kit includes the proper sleeves and bits. It is recommended that five turns of bare wire be wrapped on these pins. This tool may also be purchased from Gardner-Denver Co. (Gardner-Denver part No. 14H-1C) with No. 26263 bit and No. 18840 sleeve for wrapping #24 wire. When ordering from Digital specify the sleeve and bit size desired for #24 wire.

H810(24) — $ 99
30 ga. H810-A — $ 99
30 and 24 ga. H810-B — $150



The Type H811 Hand Wrapping tool is useful for service or repair applications. It is designed for wrapping #24 solid wire on DEC Type H800-W and H808 connector pins.

Wire wrapped connections may be removed with the Type H812 Hand Unwrapping tool.

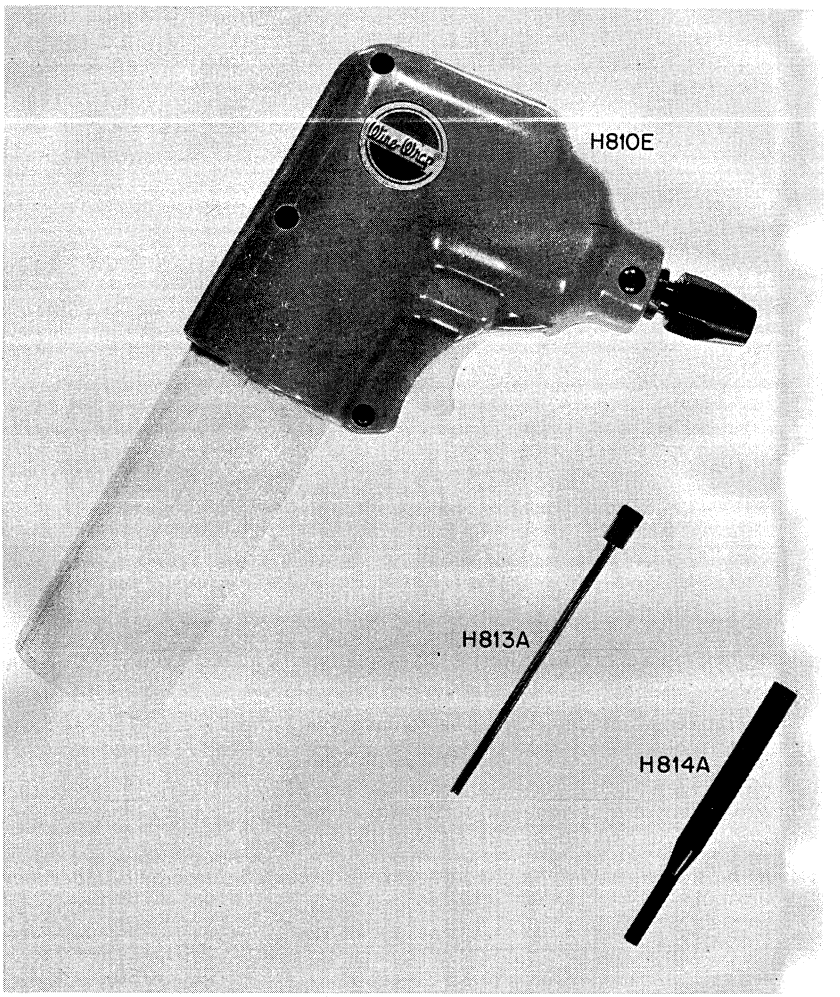
The H811-A and H812-A are equivalent to the H811 and the H812 except that the A versions are designed for #30 wire. The H813 is a #24 bit; H813-A, a #30 bit. The H814 is a #24 sleeve; H814-A, a #30 sleeve.

None of the Wire Wrapping Tools will be accepted for credit under any circumstances.

H811(24) — $24
H811-A(30) — $24
H812(24) — $10
H812-A(30) — $10
H813(24) — $30
H813-A(30) — $30
H814(24) — $21
H814-A(30) — $21

The Battery Powered Wire Wrap Gun is equipped with a rechargeable Nickel cadmium battery and requires no ac power connection while in use. The gun is available with a 24 gauge sleeve and bit (810-C), a 30 gauge sleeve and bit (810-D) and without the sleeve and bit (H810-E).

Also available from Gardner Denver Co. Model 14R2 (Battery Powered Gun) with No. 507063 bit (H813A) and No. 507100 sleeve (H814A)



H810-C	$150
H810-D	$150
H810-E	$100

913, 914, 915, 917
H820, H821, H825, H826
WIRING ACCESSORIES

ACCESSORIES

913 AND 915 PATCHCORDS

These patchcords provide slip-on connections for FLIP CHIP mounting panels and are available in color-coded lengths of 2, 3, 4, 6, 8, 12, 16, 24, 32, 48, and 64 inches. All cords are shipped in quantities of 100 in handy polystyrene boxes. Type 913 patchcords are for 24 gauge wirewrap and use AMP Terminal Type #60530-1. Type 915 patchcords are for 30 gauge wirewrap and use AMP Terminal Type #85952-3.

PATCHCORD COLOR-CODE

Size	Color	Size	Color
2″	brown	16″	yellow
3″	black/white	24″	yellow/white
4″	red	32″	green
6″	red/white	48″	green/white
8″	orange	64″	blue
12″	orange/white		

H820 AND H821 GRIP CLIPS FOR SLIP-ON PATCHCORDS

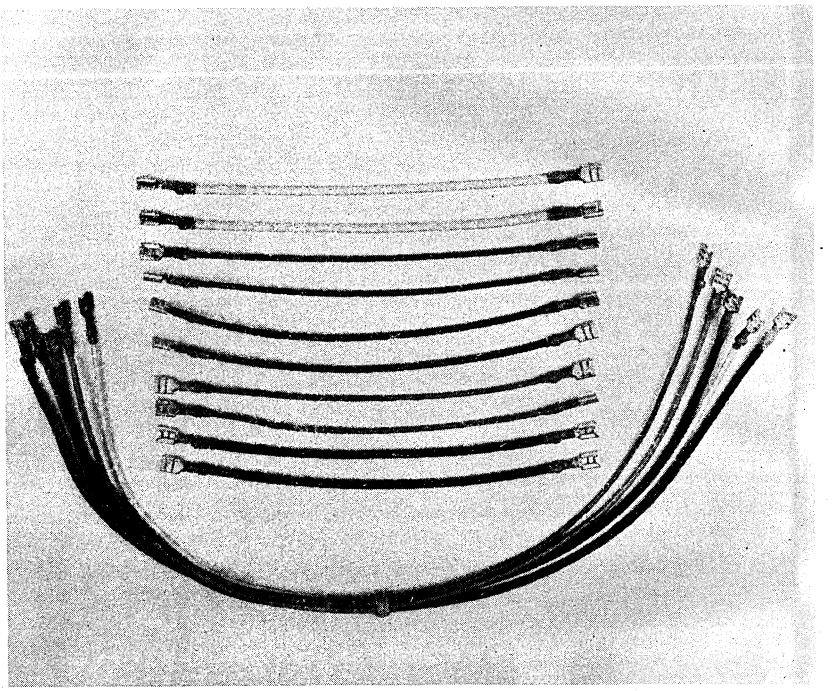
The type H820 and H821 GRIP CLIPS are identical to slip-on connectors used in respectively the 913 and 915 patchcords. These connectors are shipped in packages of 1000 and permit fabrication of patchcords to any desired length. H820 GRIP CLIPS will take size 24-20 awg. wire. H821 GRIP CLIPS will take size 30-24 awg. wire.

H825 HAND CRIMPING TOOL

Type H825 hand crimping tool may be used to crimp the type H820 GRIP CLIP connectors. Use of this tool insures a good electrical connection. This tool may also be obtained from AMP, Inc. as AMP part #90084.

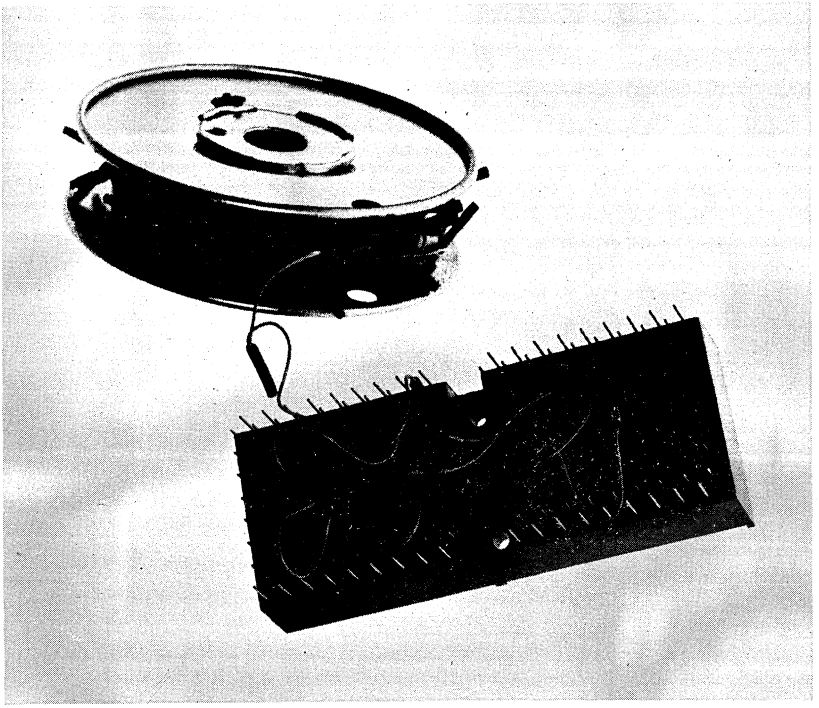
H826 HAND CRIMPING TOOL

Type H826 hand crimping tool may be used to crimp the type H821 GRIP CLIP connectors.



914 POWER JUMPERS

For interconnections between power supplies, mounting panels, and logic lab panels, these jumpers use AMP "Faston" receptacles series 250. Specify 914-7 for interconnecting adjacent mounting panels, or 914-19 for other runs of up to 19 inches. 914-7 contains 10 jumpers per package; 914-19 contains 10 jumpers per package.



917 DAISY CHAIN

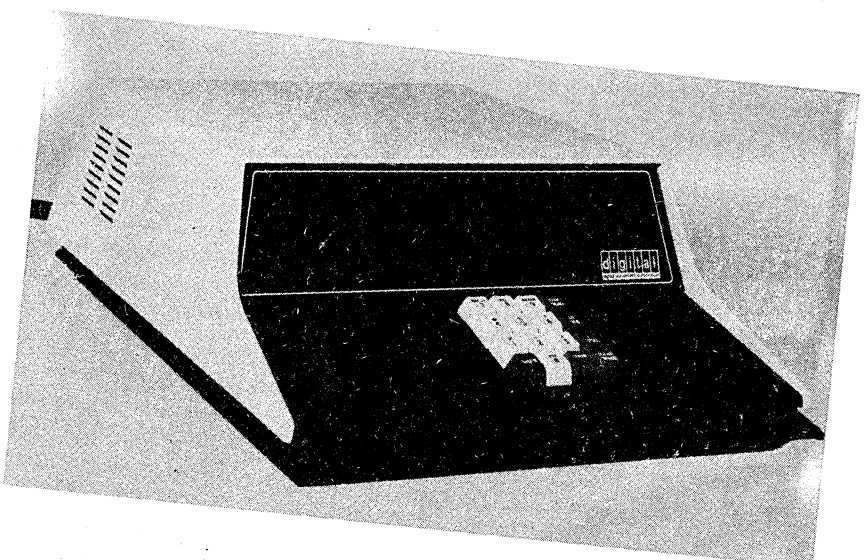
Type 917 is a continuous length of unbroken #25 AWG stranded wire. 250 gold plated and insulated terminals are crimped at predetermined intervals on each reel. In conjunction with type H803 or type H807 connector blocks and M Series modules, hand patch wiring of prototype systems is easily and quickly accomplished. All that is required is a reel of type 917 Daisy Chain and wire cutters. These dependable push on connections are also easily removable, making this wiring technique ideal in cases where wiring and unwiring for changing systems needs is required. If ever a third lead is necessary a type 915 patchcord can be used if placed on the pin before the Type 917 termination. Two contact spacings available at 2½" or 5".

917 — 2.5 — blue
917 — 5 — white

Also available from:
Berg Electronics
New Cumberland, Pa. 17070
Tel. (717) 938-6711

913 —	$ 25	pkg. of 100
914-7 —	$ 4	pkg. of 10
914-19 —	$ 4	pkg. of 10
915 —	$ 33	pkg. of 100
H820 —	$ 48	pkg. of 1000
H821 —	$ 98	pkg. of 1000
H825 —	$146	
H826 —	$210	

DATA ENTRY TERMINAL RT01



DATA ENTRY TERMINAL RT02

data entry terminals

RT01 and RT02 DATA ENTRY TERMINALS

TERMINALS

The RT01 and RT02 Data Entry Terminals offer both local and remote operation featuring Teletype and EIA serial line compatibility. Interface to a computer is accomplished via a standard full duplex 4-wire data communications Teletype interface. Standard interfaces are available for the PDP-8, -10, -11, -12, -15, and -16 Computers. Modem interface signals corresponding to EIA RS-232C specifications are also provided.

RT01 NUMERIC DATA TERMINAL

The RT01 transmits 16 unique characters (or 30 with optional shift key) which a monitoring computer may use for either numeric data or control functions. It can display up to 12 decimal digits on either 4, 8, or 12 NIXIE* display tubes. Four status indicators are also included on the console.

RT02 ALPHANUMERIC DATA TERMINAL

Data is entered via a 16-pad keyboard which includes a shift key to enable entry of a full 30 characters that the monitoring computer may interpret as either numeric data or control functions. It can receive, store, and display 32 alphanumeric characters on a single-line, gas discharge-type readout panel.

*Trademark Burroughs Corporation

APPLICATIONS

The RT01 and RT02 provide easy, low-cost access to total information in a computer. These data terminals offer an ideal communication link in such typical applications as stockroom inventory control, management information, production line monitoring, security systems, and banking transactions.

ASCII CODES

Table 1 lists the ASCII codes which will be transmitted to the communications network when its associated key on the RT02 and RT01 models with optional shift key is depressed.

Table 1. Transmitted Codes

Unshifted Characters			Shifted Characters		
Keyboard Name	ASCII Name	$(Code)_8$*	Keyboard Name	ASCII Name	$(Code)_8$*
0	0	060	ASK	D	104
1	1	061	×	*	052
2	2	062	—	—	055
3	3	063	+	+	053
4	4	064	@	@	100
5	5	065	%	%	045
6	6	066	?	?	077
7	7	067	BREAK	NUL	000
8	8	070	REL	ESC	033
9	9	071	BEGIN	STX	002
SHIFT	N.A.	N.A.	SHIFT	N.A.	N.A.
.	.	056	ERROR	DEL	177
SPACE	SP	040	CLEAR	LF	012
TOTAL	T	124	÷	/	057
YES	ACK	006	GO	G	107
SEND	CR	015	STOP	ETX	003

*Parity bit (Even) **not** shown in this table.

When communicating with the RT02's alphanumeric display the following ASCII Codes listed in Column "A" are required to display the characters listed in Column "B".

Table 2. Received Codes Display Characters

Column "A" Received ASCII $(Code)_8$	Column "B" Displayed Character	Column "A" Received ASCII $(Code)_8$	Column "B" Displayed Character
060	0	127	W
061	1	130	X
062	2	131	Y
063	3		
064	4	132	Z
065	5	040	SP
066	6	041	!
067	7	042	"
070	8	043	#
071	9	044	$
100	@	045	%
101	A	046	&
102	B	047	'
103	C	050	(
104	D	051	)
105	E	052	*
106	F	053	+
107	G	054	,
110	H	055	—
111	I	056	.
112	J	057	/
113	K	072	:
114	L	073	;
115	M	074	<
116	N	075	=
117	O	076	>
120	P	077	?
121	Q	133	[
122	R	*134	~
123	S	135	]
124	T	*136	{
125	U	*137	}
126	V		

*Modifications to ASCII code (3 total)

PRICES—RT01 TERMINAL

Type	Description	Price
RT01-AA	Numeric Data Entry Terminal ..... 4 Programmable Status Indicators; 16-key, 16-character Keyboard; Asynchronous Interface; 110 Baud, 115 Vac	$ 600.00
RT01-AB	Same as AA except 230 Vac	600.00
RT01-BA	Same as AA except 300 Baud	600.00
RT01-BB	Same as AA except 300 Baud, 230 Vac	600.00
RT01-CA	Numeric Data Entry Terminal ..... 4 Programmable Status Indicators; 16-key, 30-character Keyboard; Asynchronous Interface; 110 Baud, 115 V ac	650.00
RT01-CB	Same as CA except 230 Vac	650.00
RT01-DA	Same as CA except 300 Baud	650.00
RT01-DB	Same as CA except 300 Baud, 230 Vac	650.00

TERMINAL OPTIONS

RT01-NA	4-digit Nixie Display with Storage, Control ..... and Driver Electronics	100.00
RT01-NB	Same as NA except 8-digit Nixie	200.00
RT01-NC	Same as NA except 12-digit Nixie	300.00

INTERFACE OPTIONS

For complete ordering and price information, refer to Logic Products Terminal

INSTALLATION	Field Service Installation	60/unit
MAINTENANCE	Maintenance Contract	10/unit

PRICES—RT02 TERMINAL

RT02-AA	Alphanumeric Data Entry Terminal ..... 32-digit Alphanumeric Display; 16-key, 30-character Keyboard; 110, 150, 300, and 1200 Baud Communication Rates 115 Vac (TTY interface cable included)	$1300.00
RT02-AB	Same as AA except 230 Vac	1300.00

INTERFACE OPTIONS

For complete ordering and price information, refer to Logic Products Terminal Price List.

INSTALLATION	Field Service Installation	75/unit
MAINTENANCE	Maintenance Contract	10/unit

SPECIFICATIONS
RT01

General

Line Voltage:	115 VAC, 230 VAC, 47-62 Hz
Power:	30W maximum
Size:	15"Wx13"Dx6"H
Weight:	12 lbs.

Display

Lamps:	4 Programmable Status Indicators
Digits:	4, 8, or 12 Nixie Tubes
Decimal Point:	Programmable over 12 digits

Control Functions

Clear Display:	Code $(100)_8$
Load Status Indicators:	Code $(120)_8$ to $(137)_8$ "P" through "←"

Keyboard

Number of Keys:	16
Character Set:	ASCII
Number of Characters:	16
Keyboard Construction:	Environmentally sealed

Optional Keyboard

Number of Keys:	16
Character Set:	ASCII
Number of Characters:	30 (with shift key)
Keyboard Control:	N-Key rollover
Keyboard Construction:	Environmentally sealed

Data Input/Output

Levels:	TTY 20mA isolated current loop EIA RS-232-C
Transmit/Receive Rates:	110/110 baud 300/300 baud
Character Format:	8-Level asynchronous serial ASCII 2 Stop bits (110 baud) 1 Stop bit (300 baud)
Input/Output Connectors:	4-Lug Jones strip (TTY) Cinch DB 25P (EIA)

General

Line Voltage:	115 VAC, 230 VAC, 47-63 Hz
Power:	50W maximum
Size:	14⅜"Wx15⅞"Dx16¼"H
Weight:	14 lbs.

Alphanumeric Display

Number of Character Positior	32
Character Set:	64-character modified ASCII
Character Height:	0.2"
Character Aspect Ratio:	5 x 7
Color:	Red
Viewing Angle:	120°

Display Control Functions

Clear Display:	Code $(012)_8$
Blank Display:	Code $(016)_8$
Unblank Display:	Code $(017)_8$

Keyboard

Number of Keys:	16
Character Set:	ASCII
Number of Characters:	30 (with shift key)
Keyboard Control:	N-Key rollover
Keyboard Construction:	Environmentally sealed

Data Input/Output

Levels:	TTY 20mA isolated current loop EIA RS-232-C
Transmit/Receive Rates:	110/110 baud 150/150 baud 300/300 baud 1200/1200 baud 110/1200 baud 150/1200 baud
Character Format:	8-Level asynchronous serial ASCII 2 Stop bits (110 baud) 1 Stop bit (150, 300, 1200 baud) Even Parity
Input/Output Connectors:	8-Pin Mate-N-Lok (TTY) Cinch DB 25P (EIA)

lab series

COMPUTER LAB

LAB SERIES

The COMPUTER LAB is a high performance low-cost digital logic trainer. It uses the same monolithic integrated transistor-transistor logic circuitry used in DIGITAL's latest computers.

The digital logic fundamentals presented by the COMPUTER LAB can foster a basic understanding of computer technology for the computer career oriented user, or for a user applying computers for the first time. The COMPUTER LAB will also help the math-oriented user understand "new math" concepts, as computer logic operates with binary numbers according to Boolean algebraic laws.

Wiring is easy because of the standard logic symbology used on the front panel and the color coded Patchcords which are easily inserted and removed. An improper circuit will not damage the COMPUTER LAB. The faulty circuit merely "waits" for correction.

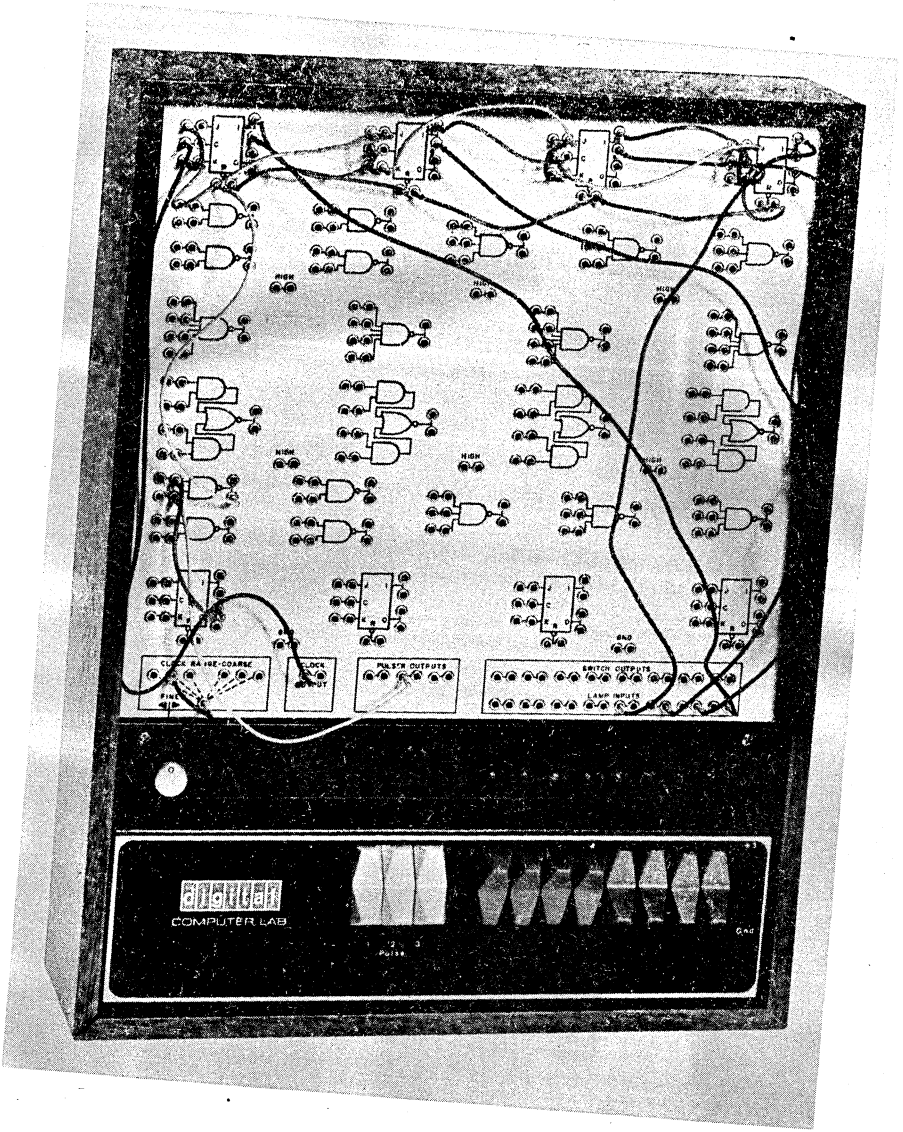
Features:

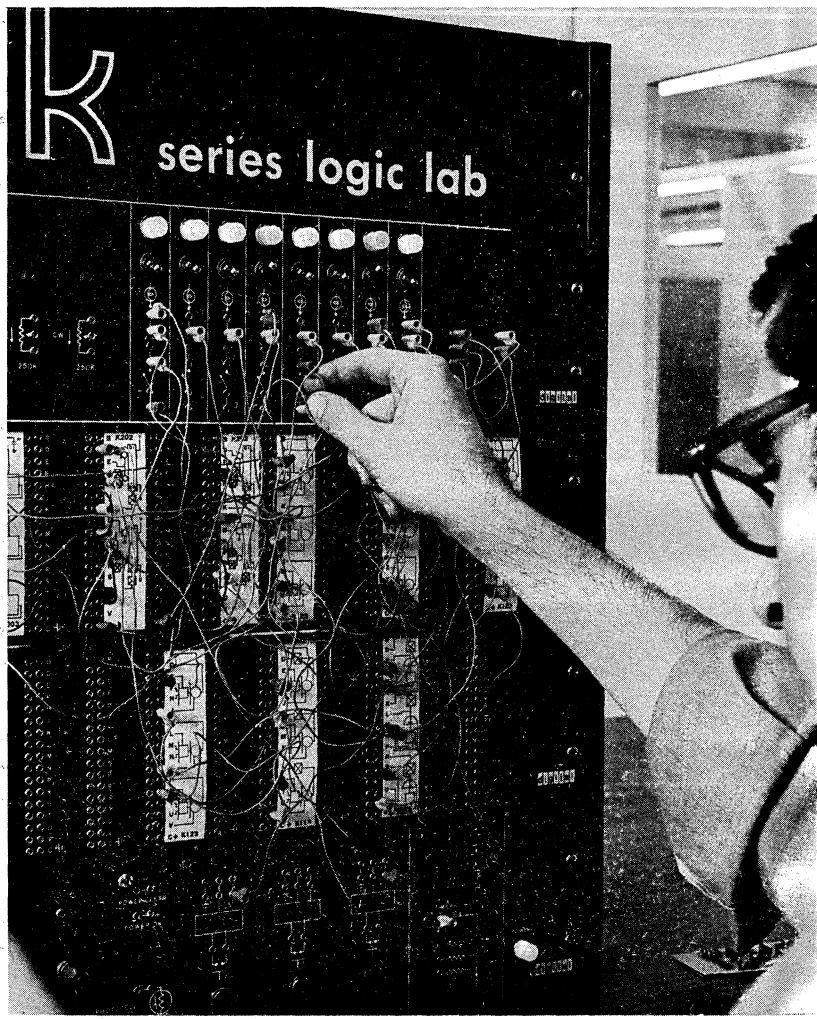
- Transistor—Transistor logic circuitry as used in DIGITAL's PDP computers
- Teaches modern computer logic
- Easy to use: MIL-STD 806 logic symbology on front panel
- Portable: Dimensions of 12½" x 17" x 3¼", weighing only 11 lbs.
- Comprehensive Workbook provides:
  - —Ten detailed chapters
  - —More than 30 experiments
  - —Over 200 hours of laboratory study
  - —Dozens of tables and diagrams
  - —An extensive appendix of supplementary information
- Instructor's Guide with answers, additional text, extra problems, course plans, at only $5.00
- Low cost: COMPUTER LAB, Workbook and Patchcord set, ready to use

H500 — $375
H500A* — $375

*220v

QUANTITY	NET PRICE/EACH
2-9	$350
10-19	325


digitaldigital
COMPUTER LAB
HIGH
HIGH
HIGH
HIGH
HIGH
HIGH
CLOCK RATE-COARSE
FINE
CLOCK OUT
PULSE OUTPUTS
SWITCH OUTPUTS
LAMP INPUTS
GND
GND
Pulse


series logic lab

K-SERIES LOGIC LAB

LAB SERIES

INTRODUCTION

The K Series Logic Laboratory is designed for use with K Series Modules. It is a device for building prototype systems for experimentation and proof of logic design as well as an effective tool for learning solid state control logic.

It is excellent for training users in digital logic techniques by enabling an individual to construct logical networks, with a "hands on approach" to learning control systems for Industrial Applications.

The K Series Logic Lab is a completely self contained system consisting of a power supply, photo cell, pulse generator, switch controls, indicators, mounting hardware and a recommended basic complement of logic modules necessary to construct a working system. The system is expandable and can accommodate additional K901 patchboard panels for mounting additional logic modules.

EDUCATION AND TRAINING

As a training device the K Series Logic Lab offers the engineer, technician, and user a step by step approach to building an understanding of various digital logic functions, such as, AND, OR and the operations of NAND and NOR etc. The user has the option of using NEMA or MIL spec symbology when making logic connections. Symbology cards on basic logic modules for use with the K901 patchboard panel are printed with NEMA on one side and MIL SPEC 806 on the reverse side.

BREADBOARDING AND TESTING

The logic laboratory power supply is capable of supplying 5V-DC for about 100 modules. There is no restriction on the size of a system which can be implemented, since additional patchboard panels can be ordered and "K" Logic Laboratories interconnected directly.

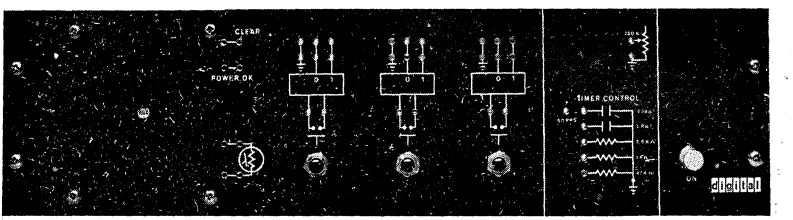
There is no substitute for actually building the system and verifying the logic.

Some common uses of the Logic Laboratory are listed below. Many of these are described in detail in the Control Handbook and part III in the 1969 Positive Edition Logic Handbook.

Timer Sequencers	Serial Adder
Shifter Sequencers	Stepping Motors Control
Parallel Counters	Pulse Generator
Pulse Rate Multiplier	Annunciator

K900
CONTROL PANEL — POWER SUPPLY

LAB SERIES



The K900 is a combination power supply and input control panel. The input devices include a photocell, three push button pulsers and timing components for a K303 clock mounted in a K901 panel. Clock timing components are provided for frequency steps in ranges of 2Hz to 60Hz and 200Hz to 6K Hz. Wiring diagrams for properly connecting the clock are shown in the logic and control handbooks (reference K303). The power supply can drive approximately ten type K901 panels of K series flip chip™ logic. Pulsers consist of a K501 schmitt trigger with a K581 switch filter. Power is supplied by K731, K743 and K732 power supply modules.

Electrical Characteristics

Input voltage: Power supply: 115V 50-60 cps
Output voltage: +5 VDC ±10%
Output current: 3 amp

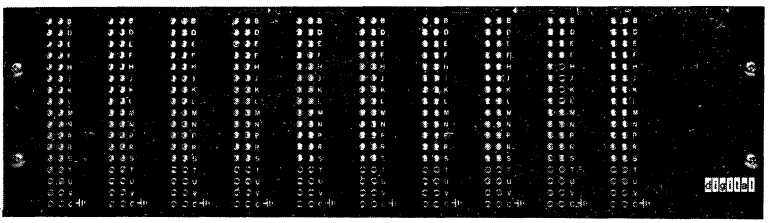
Mechanical Characteristics

Panel width: 19"
Panel height: 5 3/16"
Depth: 12"
Finish: black
Power Output connection: Hayman Tab terminals which fit AMP "Faston" receptacle series 250, part 41774 or Type 914 Power Jumpers.
Power Unit connection: 18/3 AC power cord

K900 — $185

K901, 911
PATCH BOARD PANEL

LAB SERIES



K901 PATCHCORD MOUNTING PANEL

This panel provides up to ten FLIP CHIP modules with power and patch connections. Space between patching sockets allows insertion of logic diagrams. Logic diagrams are printed on all FLIP CHIP module data sheets. More permanent plastic diagrams are available for those modules listed.

PANEL WIDTH: 19 in.
PANEL HEIGHT: 5 3/16 in.
DEPTH: 6 1/2 in. with FLIP CHIP modules inserted

FINISH: Black
POWER INPUT CONNECTIONS: Tabs which fit AMP "Faston" receptacle series 250, part 41774.

911 PATCHCORDS

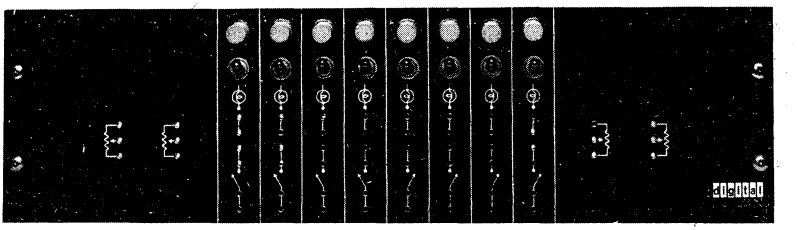
DEC Type 911 Banana-Jack Patchcords are supplied in color-coded lengths of 2 in. (brown), 4 in. (red), 8 in. (orange), 16 in. (yellow), 32 in. (green), and 64 in. (blue). Patchcords may be stacked to permit multiple connections at any circuit point on the graphic panels of the DEC K901 Mounting Panel. The cords are supplied in snap-lid plastic boxes of ten for handy storage.

K901 — $125
911 — $9/pkg. of 10

K902

INDICATOR SWITCH PANEL

LAB SERIES



The H902 Panel provides facilities for control and observation of the Logic Laboratory. It contains eight indicator lights and a lamp driver module, eight toggle switches and four potentiometers. Connections to these devices are made with Type 911 Stacking Banana-Jack Patchcords.

INDICATORS: Indicators inputs accepts signals of +5V and ground. An open circuit input will light the indicator. If the input is returned to ground, the indicator will not light. The load is 1 mA.

TOGGLE SWITCHES: The toggle switches are single pole, single throw with a logic diagram to show the open and closed positions.

POTENTIOMETERS: The potentiometers are 250,000 ohms. They may be used to control the frequency of delay one-shots or clock circuits in the K901 Mounting Panel.

MECHANICAL CHARACTERISTICS

PANEL WIDTH: 19 in.
PANEL HEIGHT: 5 3/16 in.
DEPTH: 6 1/2 in.

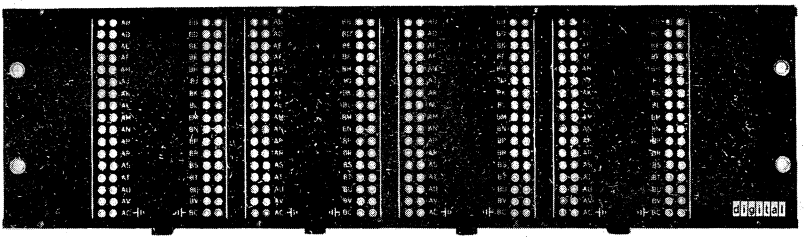
FINISH: Black
POWER INPUT CONNECTIONS: Tabs which fit AMP "Faston" receptacle series 250, part 41774.

K902 — $145

K903

PATCH PANEL BOARD

LAB SERIES



This patch panel provides logic power and patch connections for four double-height or eight single height FLIP-CHIP ® modules. The panel was designed particularly for K Series double height modules including the interfacing modules (K5xx and K6xx). Two K903 panels cannot however be mounted together on a mounting rack due to socket overhang at the bottom of each K903 panel. Space between patching sockets allows insertion of logic diagrams. Logic diagrams are printed on all FLIP-CHIP® module data sheets. More permanent plastic diagrams are available for those modules listed.

PANEL WIDTH: 19 in.
PANEL HEIGHT: 5 3/16 in.
DEPTH: 6 1/2 in. with FLIP-CHIP® modules inserted.

FINISH: Black
POWER INPUT CONNECTIONS: Tabs which fit AMP "Faston" receptacle series 250, part 41774

K903—$155

4913, 914

MISCELLANEOUS ACCESSORIES

LAB SERIES

4913 MOUNTING RACK

The 4913 Mounting Rack provides support for a and up to four K901 Patchcord Mounting Panels, for a total of up to 40 FLIP CHIP modules ready to be patched together for experiments. It may also be used to mount general purpose mounting panels such as the K943. The power supply must be mounted at the bottom for stability.

Height: 26¼ in.

Threads for mounting panels: 10-32

914 POWER JUMPERS

For interconnections between power supplies, mounting panels, and logic lab panels, these jumpers use AMP "Faston" receptacles series 250. Specify 914-7 for interconnecting adjacent mounting panels, or 914-19 for other runs of up to 19 inches. 914-7 contains 10 jumpers; 914-19 contains 5.

4913	— $25
914-7	— $ 4
914-19	— $ 4

BASIC EQUIPMENT LISTS

BASIC LOGIC LABORATORY

1-K901	Patchboard panel	125.00
1-K902	Indicator Switch Panel (complete with K683 module)	145.00
1-K900	Power Supply and Control Panel (complete with Power modules)	185.00
1 pair—4913	Mounting Rack	25.00

RECOMMENDED LOGIC MODULES AND PATCHCORDS FOR USE WITH THE LOGIC LABORATORY

		UNIT PRICE	TOTAL PRICE
4-K003	Expander	5.00	20.00
2-K012	Expander	8.00	16.00
3-K113	Gate	11.00	33.00
3-K123	Gate	12.00	36.00
2-K134	Inverter	13.00	26.00
1-K161	Decoder	25.00	25.00
1-K174	Comparator	24.00	24.00
1-K184	Rate Multiplier	25.00	25.00
2-K202	Flip-flop	27.00	54.00
1-K206	Flip-flop	20.00	20.00
2-K210	Counter	27.00	54.00
1-K220	Up-down Counter	55.00	55.00
1-K230	Shift Register	40.00	40.00
1-K303	Timer	27.00	27.00
1-K323	One shot delay	35.00	35.00
1-K376*	Timer Control (0.1-3.0 sec)	15.00	15.00
1-K378*	Timer Control (1.0-30 sec)	15.00	15.00
1-K373*	Timer Control (20 Hz-600 Hz clock)	11.00	11.00
1-K522	Sensor Converter	25.00	25.00
4 pks. of 10 patchcords (911-2")		9.00	36.00
5 pks. of 10 patchcords (911-4")		9.00	45.00
2 pks. of 10 patchcords (911-16")		9.00	18.00
1 pkg. of 10 patchcords (911-16")		9.00	9.00
26 symbology cards		.25 ea.	6.50

Complete K-Series logic lab with workbook and modules listed — H510 $995.00

Asterisk* denotes symbology cards unavailable. Symbology cards for use with K901 patchboard panel, .25 ea., minimum purchase of $5.00 applies.

IF ADDITIONAL K901 PATCHBOARDS ARE ORDERED:

1-911-4"	pkg. of 10 patchcords	9.00
1-911-8"	pkg. of 10 patchcords	9.00
1-911-16"	pkg. of 10 patchcords	9.00
1-911-32"	pkg. of 10 patchcords	9.00

K-SERIES INTERFACE MODULES

Recommended logic modules for input/output functions.

AC Input/Output

1-K578	120 VAC Input converter	80.00
1-K614	120 VAC Isolated AC switch	88.00

DC Input/Output

1-K580	Dry Contact Filter	28.00

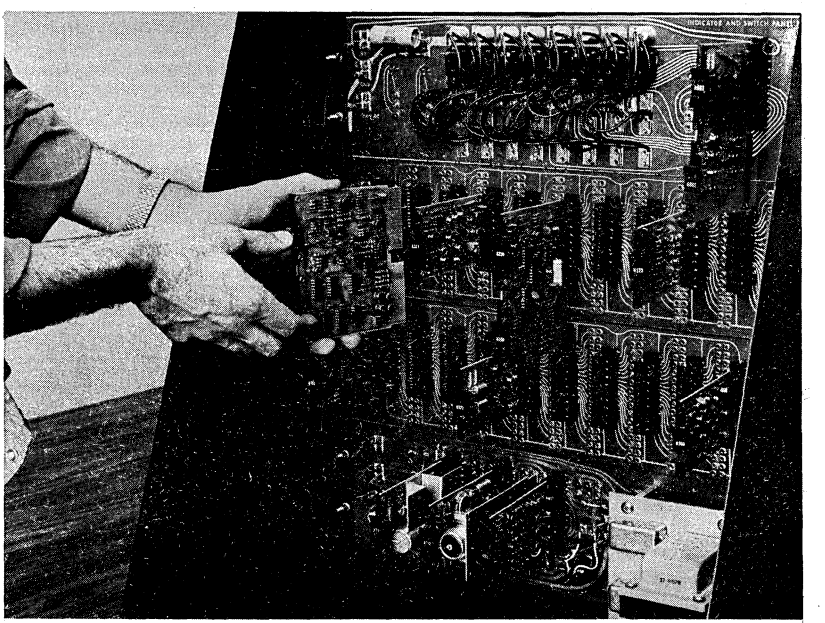
Listed below are a number of DC output drivers that may be used:

1-K644	DC output Driver	66.00
	or	
1-K656	DC output Driver	80.00
	or	
1-K658	DC output Driver	128.00

Each additional K series workbook	5.00

Note: only 3 out of 4 circuits are available when using above 3 modules with the K901 mounting panel.

Reference logic or control handbook for additional module information and selection.



A rear view of the K Series Logic Lab shows how modules are plugged into mounting panels.

M SERIES LOGIC LAB

LAB SERIES

Introduction
The M Series Logic Lab is a highly versatile unit that can be used succeessfully at all stages of digital logic design, from training, to experimentation, to systems design, to final system checkout. It can be used to build prototype logic systems or as a tool to test and design actual hardware. Educationally, it provides the designer with a flexible system for experimentation as well as a basic unit for learning the fundamentals of electronic circuitry and logic design.

The Logic Lab's exceptional training abilities stem mainly from the fact that the student can design and actually construct his logic networks directly on the unit. This provides valuable practical reinforcement of theoretical concepts.

The M Series Logic Lab is designed for use with any Series of DEC modules which uses +5 Volts for power.

The M Series Logic Lab is a completely self-contained system, consisting of a power supply, lights, switches, and two racks of connector blocks. The system is expandable and can accommodate an additional rack of connector blocks.

Education and Training
As a training device, the M Series Logic Lab offers the user an easy step-by-step way to gain an understanding of various logic functions, such as AND, OR, NAND, NOR, etc. Because this tool is not limited to any one technology, it can be used to study not only TTL but also DTL, ECTL, and other types of logic.

Breadboarding and Testing
The Logic Lab power supply can supply +5 V dc at 6.5 amps (max.). This supplies sufficient current for systems using all module slots.

The Logic Lab is an effective tool for bridging the gap between paper design and a fully tested, marketable product.

Console
The Console consists of a light and a switch panel. The light panel is made up of 80 lights arranged in four rows of 16 lamps and four rows of four lamps. The user can write designations on the panel adjacent to each lamp.

The switch panel has three groupings of switches—16 on/off-type switches, two on/off-type switches, and two pulser-type switches. This switch configuration provides highly versatile control.

Connector Racks
The M Series Logic Lab has two 19" racks of low-density H808 connector blocks. Each rack contains eight connector blocks and each connector block has four module slots; therefore, there are 32 module slots per rack for a total of 64 module slots in the standard M Series Logic Lab. One additional rack can be mounted increasing the available module slots to 96. Regardless of how many racks are used, four slots must be dedicated to receiving flexprint cables from the switch and light panels.

Power bussing of pins A2, C2, T1 is also available as a standard item on the rack of connector blocks.

CABLES

Switch Board (Switches are numbered from right to left)

S0-Pin E1	S8-Pin R2	C1-Pin E2
S1-Pin D1	S9-Pin P2	C2-Pin F2
S2-Pin C1	S10-Pin N2	
S3-Pin B1	S11-Pin M2	P1-Pin A1
S4-Pin V2	S12-Pin L2	P2-Pin D2
S5-Pin U2	S13-Pin K2	
S6-Pin T2	S14-Pin J2	
S7-Pin S2	S15-Pin H2	

Light Board
First letter of each title below designates the row of lights. Lights are numbered on the indicator panel from right to left.

Second letter designates cable from indicator panel.

Third letter and associated number designates pin in a module slot used for light function.

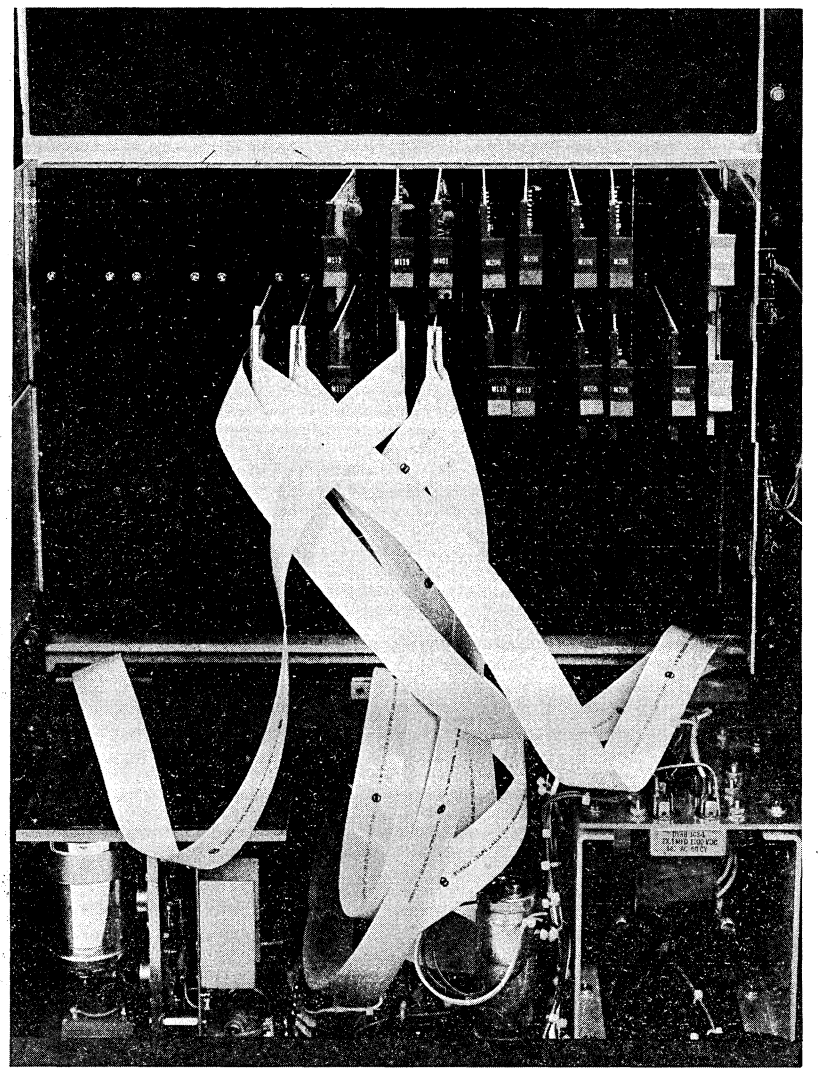
A0 pin BV1	B0 pin BU1	C0 pin BR1	D0 pin BS1
A1 pin BJ1	B1 pin BH1	C1 pin BM1	D1 pin BB1
A2 pin BL1	B2 pin BF1	C2 pin BN1	D2 pin BC1
A3 pin BP1	B3 pin BK1	C3 pin BE1	D3 pin BD1
A4 pin BE2	B4 pin BR2	C4 pin BA1	D4 pin BT2
A5 pin BS2	B5 pin BL2	C5 pin BD2	D5 pin BH2
A6 pin BF2	B6 pin BM2	C6 pin BK2	D6 pin BN2
A7 pin CK2	B7 pin BV2	C7 pin BU2	D7 pin CF2
A8 pin CE2	B8 pin CR2	C8 pin BJ2	D8 pin CT2
A9 pin CS2	B9 pin CL2	C9 pin BP2	D9 pin CM2
A10 pin CN2	B10 pin CU2	C10 pin CH2	D10 pin CA1
A11 pin CV2	B11 pin CJ2	C11 pin CV1	D11 pin CB1
A12 pin CP2	B12 pin CD2	C12 pin CU1	D12 pin CC1
A13 pin CR1	B13 pin CS1	C13 pin CK1	D13 pin CE1
A14 pin CP1	B14 pin CM1	C14 pin CH1	D14 pin CF1
A15 pin CN1	B15 pin CL1	C15 pin CD1	D15 pin CJ1
E0 pin AP1	F0 pin AS1	G0 pin AJ1	H0 pin AH1
E1 pin AR1	F1 pin AU1	G1 pin AK1	H1 pin AF1
E2 pin AN1	F2 pin AM1	G2 pin AL1	H2 pin AE1
E3 pin AA1	F3 pin AC1	G3 pin AB1	H3 pin AD1

H520-A (240v./50Hz) ALSO AVAILABLE

For complete information, request M Series Data Sheets from Logic Products, Digital Equipment Corp., Maynard, Mass. 01754.

M Series Logic Lab H520 — $995

M SERIES LOGIC LAB (FRONT VIEW)



M SERIES LOGIC LAB (REAR VIEW)

about digital equipment corporation

In approximately 15 years, DIGITAL EQUIPMENT CORPORATION has grown from three employees and one floor of production space in a converted woolen mill, to a major international corporation. DIGITAL now employs more than 10,000. Our products are manufactured in several plants, and are sold and serviced from customer support centers in the United States, Canada, Japan, Australia and seven European countries.

We produce a wide variety of computer and control products ranging from logic modules to large time sharing computer systems. In addition to those logic modules and associated equipment detailed in this handbook, DIGITAL also manufactures 12-, 16-, 18- and 36-bit computers, peripheral devices, special systems, accessories, programmable controllers and a wide variety of software.

DIGITAL first began manufacturing computer-related equipment in 1957 when we introduced a line of solid state logic modules. These were initially used to test and build other manufacturers' electronic equipment. The logic module product lines have been continually broadened, and DIGITAL now ranks as the world's largest manufacturing supplier of digital logic modules, producing more than three million per year.

Our first computer, the PDP-1 was introduced a decade ago, selling for $120,000 while competitive machines were priced over $1 million. Ever since the PDP-1, DIGITAL has specialized in on-line, real-time computers.

The PDP-5, introduced in 1963, was the first truly small computer. The PDP-8 series, the PDP-5 successor announced in 1965, is one of the most popular and successful families of computers ever produced.

DIGITAL is a leading force in small computers, but it also has been a pace-setter in other parts of the industry. For example, one of the first time sharing systems ever built incorporated a PDP-1. DIGITAL introduced the first large-scale, commercially available time sharing system in 1965—the PDP-6. Its successor, the DECsystem-10, can do more at a price well under $1 million than competitive systems costing several times as much.

With more than 18,000 computers now installed, DIGITAL is the second largest manufacturer in terms of installations.

In industry, DIGITAL computers provide engineers with a powerful control and testing tool. They control blast furnaces and open hearths, monitor slab mills and finishing mills, and control and monitor a variety of machine tools, transfer and material handling equipment. DIGITAL computers guided the SS MANHATTAN as she sailed the Northwest Passage, and are being used in testing the Boeing 747 jumbo jet, and the Anglo-French Concorde supersonic airplane.

In science, our computers have cut the researchers experiment time with direct, on-line data reduction. DIGITAL computers control and monitor powerful nuclear reactors, control X-ray diffractometers, analyze nuclear spectroscopy data, and assisted in the analysis of lunar rock samples. They are used extensively in environmental research and pollution control.

In virtually all DIGITAL computer installations, DIGITAL solid state logic is used for interfacing or control application.

GENERAL INFORMATION

FINANCIAL RESULTS

Total Sales (in millions)		Net Income (in millions)	
1972	$187.6	1972	$15.3
1971	146.8	1971	10.6
1970	135.4	1970	14.4
1969	91.2	1969	9.4
1968	57.3	1968	6.8
1967	38.8	1967	4.5
1966	22.7	1966	1.9

DIGITAL EQUIPMENT CORPORATION
CORPORATE HEADQUARTERS

Maynard, Massachusetts

MANUFACTURING PLANTS

Mountain View, California
Maynard, Massachusetts
Natick, Massachusetts
Springfield, Massachusetts
Westfield, Massachusetts
Westminster, Massachusetts
San German, Puerto Rico
Kanata, Ontario, Canada
Galway, Ireland
Tachi, Taiwan

SPECIAL SYSTEMS

Anaheim, California
Wallensteinplatz 2, West Germany
Reading, Berkshire, England

TOTAL EMPLOYES 10,000

GENERAL DESCRIPTION OF DIGITAL PRODUCTS
(Excluding those discussed in this Handbook)

COMPUTERS

PDP-8E, PDP-8F, PDP-8M, the lower cost successors to the PDP-8/I and PDP-8/L. They are the outgrowth of the largest concentration of minicomputer engineering, programming and user expertise in the world. Among the PDP-8/E features are: a unique internal bus system called OMNIBUS™, which allows the user to plug memory and processor options into any available slot location; the availability of 256 words of read only or read/write memory; a 1.2 microsecond memory cycle time; the use of TTL integrated circuitry with medium scale integration; expansion to 32,768 12-bit words; low cost mass storage expansion with DECdisk, DECtape, or the new DECcassette.

PDP-11 A family of expandable general purpose computers with 4,096 basic words of standard core memory, each word 16 bits in length. Memory cycle time is 1.2 microseconds. Machine uses integrated circuitry and has some medium-scale integration in central processor. Models are PDP-11/05, -10, -15, -20, -40, -45.

PDP-12 Laboratory computer system capable of executing PDP-8 and LINC-8 programs. It has basic 4,096-word core memory. Each word is 12 bits in length. Basic laboratory system includes interactive graphics capability, magnetic tape storage, A/D converter, and prewired, real-time clock.

PDP-15 A medium-scale series with an 18-bit word length, available in 5 complete software operating systems and 8 applications packages.

DECSYSTEM-10 General purpose large computer with basic memory of 8,192 (36-bit) words, expandable to 262,144. Will handle up to 63 time-sharing users simultaneously with batch and real-time jobs at the same time.

COMPUTER-BASED SYSTEMS

The following describes a sample of some of the hardware/software application systems available from DIGITAL.

IDAC SYSTEMS Small computer-based systems for industrial data acquisition, process control, data logging, process monitoring and quality testing, uses simplified language designed for engineers, not programmers.

LAB-11 and LAB-8/E Small computer-based data signal averaging systems used in bio-medical, chemistry, and physics laboratories. Include software for other functions.

TSS-8 and RSTS-11 Small computer-based general purpose time-sharing systems designed to accommodate up to 16 users with a variety of software for many tasks.

TYPESET-8 & TYPESET-11 Small computer-based system for setting type, producing punched tape containing all hyphenation, justification and format commands needed to set 12,000 lines of copy per hour.

CDP Small computer-based gas liquid chromatography system that will service 20 or more gas chromatographs simultaneously. It reduces and analyzes data accurately, repetitively and economically.

CLINICAL-LAB-12 Real-time, on-line multiterminal small computer system designed to provide the clinical laboratory with an economical means of data collection, data reduction, and analysis.

EDUCATIONAL SYSTEMS These systems include computer and a variety of applications software. In the group are single language time-sharing systems and hardware/software calculator replacements.

DISPLAYS A variety of displays are available for all applications where the speed and flexibility of graphic communications increase system efficiency.

SPECIAL SYSTEMS Digital's special systems group custom builds hardware and software systems for special applications.

SOFTWARE A comprehensive line of software is available with DIGITAL's hardware. Assemblers, debugging routines, editors, monitors, floating point packages and mathematical routines, diagnostic programs, are made available.

DIGITAL has also developed such conversational, interpretive languages as: FOCAL, an on-line langauge used as a tool by students, engineers and scientists in solving a wide variety of numerical problems; and DIBOL, a business-oriented computer language designed to bring the speed and power of PDP-8 family computers to small and medium-size business establishments.

OPTIONS & PERIPHERALS Analog/Digital converters, display and plotting equipment, drums and disks, magnetic tape equipment, card equipment, line printers, teletypwriters and many others.

SUPPLIES Power supplies, cabinetry, mounting hardware, tape, tape reels, storage racks, teletype ribbon and paper.

WARRANTY

WARRANTY 1—B, R, W, M, K, AND A MODULES — All B, R, W, M, K, and A modules as shown in the Logic Handbook and Control Handbook, as revised from time to time, are warranted against defects in workmanship and material under normal use and service for a period of ten years from date of shipment providing parts are available. DEC will repair or replace, at DEC's option, any B, R, W, M, K, or A module found to be defective in workmanship or material within ten years of shipment for a handling charge of $5.00 or 10 per cent of list price per unit, whichever is higher. Handling charges will be applicable from one year after delivery.

WARRANTY 2—SYSTEM MODULES, LABORATORY MODULES, HIGH CURRENT PULSE EQUIPMENT, G, S, H, AND NON-CATALOG FLIP-CHIP MODULES — All items referenced are warranted against defects in workmanship and material under normal use and service for a period of one year from date of shipment. DEC will repair or replace, at DEC's option, any of the above items found to be defective in workmanship or material within one year of shipment. Repair charges will be applicable from one year after delivery with repair charges varying depending on the complexity of the circuit.

The Module Warranty outside the continental U.S.A. is limited to repair of the module and excludes shipping, customer's clearance or any other charges.

Modules must be returned prepaid to DEC. Transportation charges covering the return of the repaired modules shall be paid by DEC except as indicated in previous paragraph, and will be made on a UPS basis, where available, or Parcel Post insured. Premium methods of shipment are available at customer's expense and will be used only when requested. If DEC selects the carrier, DEC will not thereby assume any liability in connection with the shipment nor shall the carrier be in any way construed to be the agent of DEC. Please ship all units to:

Digital Equipment Corporation
Module Marketing Services
Repair Division
146 Main Street
Maynard, Mass. 01754

No module will be accepted for credit or exchange without the prior written approval of DEC, plus proper Return Authorization Number (RA#).

All shipments are F.O.B. Maynard, Massachusetts, and prices do not include state or local taxes. Prices and specifications are subject to change without notice.

DISCOUNT SCHEDULE

Aggregate List Price	Applicable Discount
$ 5,000 - 9,999	3%
10,000 - 19,999	5%
20,000 - 49,999	10%
50,000 - 99,999	15%
100,000 - 249,999	18%
250,000 - 499,999	20%
500,000 - 999,999	22%
1,000,000 - AND OVER	25%

Discounts apply to any combination of FLIP CHIP Modules.

See separate cabinet discount schedule on page 461

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INTERNATIONAL

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Digital Equipment Corporation International Europe
81 Route de l'Aire
1211 Geneva 26, Switzerland
Telephone: 42 79 50 Telex: 22 683

FRANCE
Equipment Digital S.A.R.L.
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327 Rue de Charenton, 75 Paris 12ème, France
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GRENOBLE
10 rue Auguste Ravier, F-38 Grenoble, France
Telephone: (76) 87 56 01/02 Telex: 32 882 F (Code 212)

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Telegram: Flip Chip Koeln
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Am Forsthaus Gravenbruch 5-7
Telephone: 06102-5526 Telex: 41-76-82
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3 Hannover, Podbielskistrasse 102
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