pdp15
pdp15/76
unichannel 15

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INTRODUCTION

This guide describes in more detail, the UNICHANNEL 15 operation and features presented in the RK15 Disk Cartridge System Option Bulletin.

The first section .....presents a look at the UC15 system architecture.

The second section.....describes the PIREX montior system; how to use it and other software aids.

The final section......provides, for those interested in creating their own programs, a complete hardware specification including IOT and register descriptions.

Supplementing this guide are two manuals:

Unichannel 15 System Maintenance Manual:..DEC-15-HUCMA-A-D

UC15 Software Manual:.....DEC-15-XUCMA-A-D

The maintenance manual describes the details of the MX15-B and the DR15-C logic and gives maintenance details.

The software manual describes the details of the PIREX Monitor.

UNICHANNEL - 15 HARDWARE ARCHITECTURE

The term UNICHANNEL was created because it emphasizes the union of Digital's UNIBUS with the big computer concept of the programmable I/O channel. UNICHANNEL 15 unites low cost, mass produced peripherals with big computer software and performance on the PDP-15.

UNICHANNEL 15 (UC15) is a peripheral processor for the PDP-15 utilizing the PDP-11/05 minicomputer. It provides the PDP-15 with a second general purpose processor and a second high speed I/O bus; the UNIBUS. This UNIBUS is an 18-bit pathway permitting transfer of either 18-bit words, 16-bit PDP-11 words, or two 8-bit bytes.

The UC15 allows flexible low cost configuration and expansion of PDP-15 systems.

The UC15 minimizes the peripheral processing load on the PDP-15 allowing maximum computational throughput in a low-priced, medium scale system.

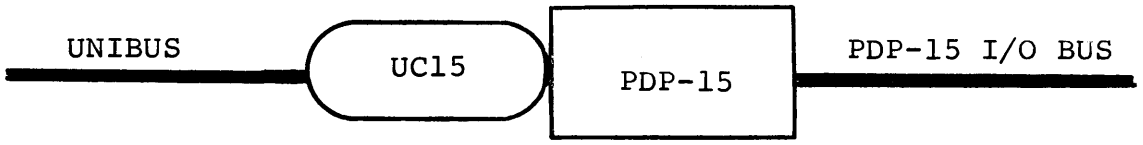


FIGURE 1: Simplified UC15 Diagram

UNICHANNEL 15 OPERATION

There are three major components of the UC15:

1. A PDP-11/05 computer with "local" PDP-11 memory.
2. An MX15-B memory multiplexer which allows both the PDP-15 processor and the PDP-11 processor to share common memory. The shared memory is ordinary 18-bit PDP-15 core memory.
3. An "interrupt link" to provide a real-time means of interprocessor communications.

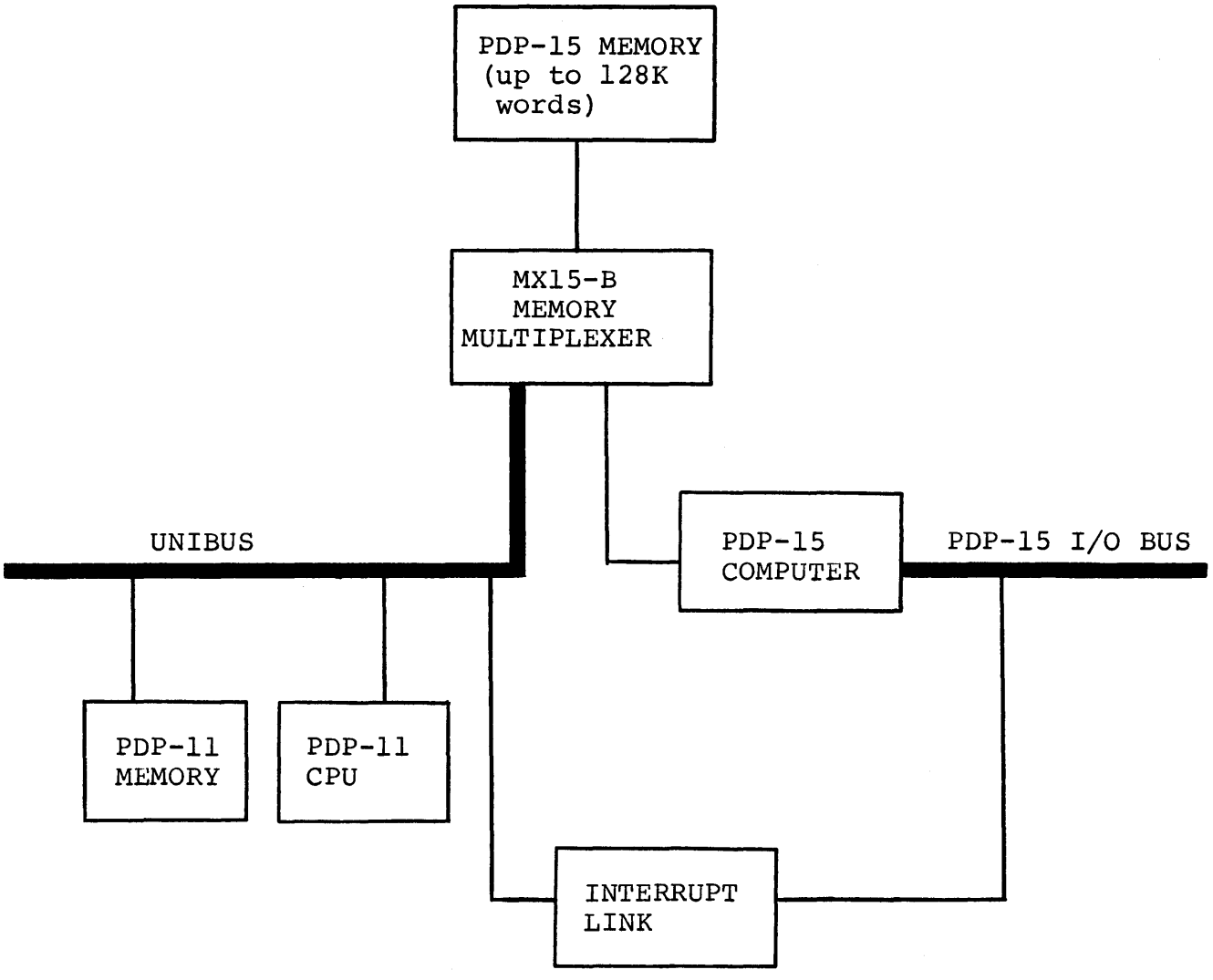


Figure 2: Diagram of UC15 Hardware Interrelationships

SUMMARY - UNICHANNEL 15 HARDWARE ARCHITECTURE

This particular architecture was chosen because of its many advantages.....

PDP-15 Memory is addressable by the UNIBUS. Hence, DMA transfers from and to such secondary storage devices as disks are direct.

The interrupt link provides inter-processor signaling on a microsecond basis. This is ideal for efficient real-time service -- a necessity for flexible I/O control.

All PDP-15 systems may be upgraded by adding the UC15. All memory remains useable.

Cost is minimized by allowing the PDP-11 to share the PDP-15 console and paper tape loader system.

Maximum use of the PDP-15 memory is maintained through synchronization overlap with memory use by the MX15-B. This "pre set up" technique increases the number of memory cycles per second when both PDP-15 and PDP-11/05 are accessing the common PDP-15 memory.

The UNIBUS provided by the UC15 is electrically compatible with any device meeting UNIBUS interfacing specifications with the following restraints:

1. UNIBUS lengths must be kept short.

2. No provision is made for UNIBUS parity.

Data in the common PDP-15 memory may be treated as either 18 or 16 bit words or as (2) 8-bit bytes.

True simultaneous parallel processing is possible in the local and common memories.

The DMA rate is high and the worst case and average latencies are low for maximum I/O performance.

Finally, the system is highly modular allowing flexibility in configuration and excellent software utilization and control. The system permits variations in both local and common memory size. It allows almost any combination of PDP-15 and UNIBUS peripherals.

UNICHANNEL - 15 SOFTWARE ARCHITECTURE

The hardware architecture is complimented by sophisticated system software. PDP-15 software systems running with a UNICHANNEL system relies on PIREX, a compact multitasking peripheral executive. In addition to PIREX, Digital supplies UNIBUS device drivers, UNICHANNEL compalible handlers, and supporting utility functions.

The software system used by UC15 consists of two parts:

1. One component is a mutli-programming peripheral processor executive called PIREX and is executed by the PDP-11.

2. The other component is an operating system in a PDP-15. (e.g. DOS-15 or BOSS-15).

PIREX

PIREX is a multi-programming executive designed to accept any number of requests from a PDP-15 or PDP-11 and process them on a priority basis while processing other tasks concurrently. PIREX services all Input/Output requests from the 15 in parallel on a controlled priority basis. Requests to busy routines (called tasks) are automatically queued (entered into a waiting list) and processed whenever the task in reference is free. In a background environment, PIREX is also capable of supporting any number of priority driven software tasks initiated by the 15 or the 11 itself.

Figure 3 shows the communications flow in a UNICHANNEL system. The possible links which may exist in the system are as follows:

1. Handler to driver to allow the PDP-15 to use a UNICHANNEL device.

2. Handler to non-driver task to allow the PDP-11 to intercept output and manipulate it or store it for spooling.

3. Program to non-driver task to allow cooperative processing on the two CPU's as occurs in the use of the MAC-11 assembler.

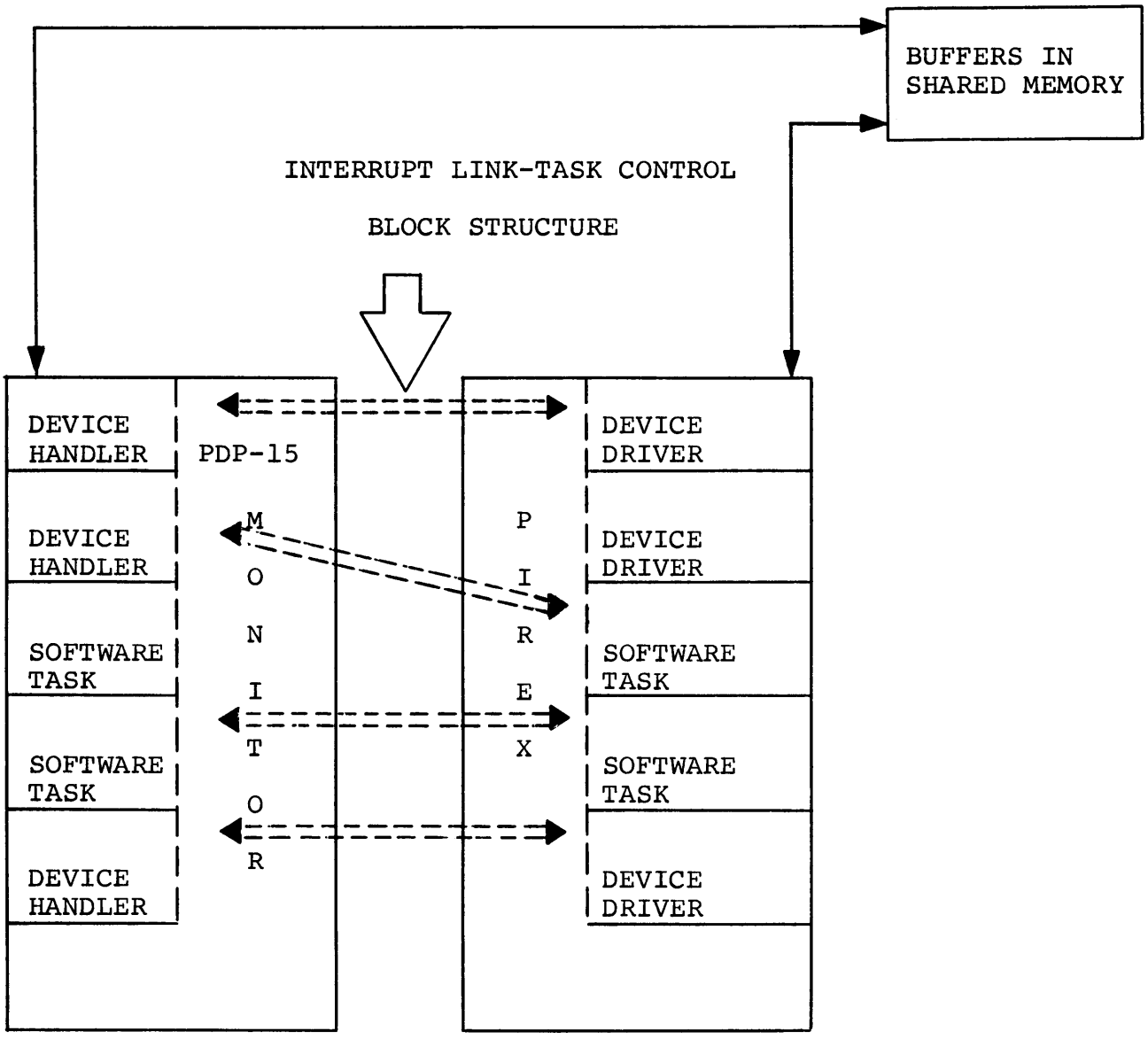
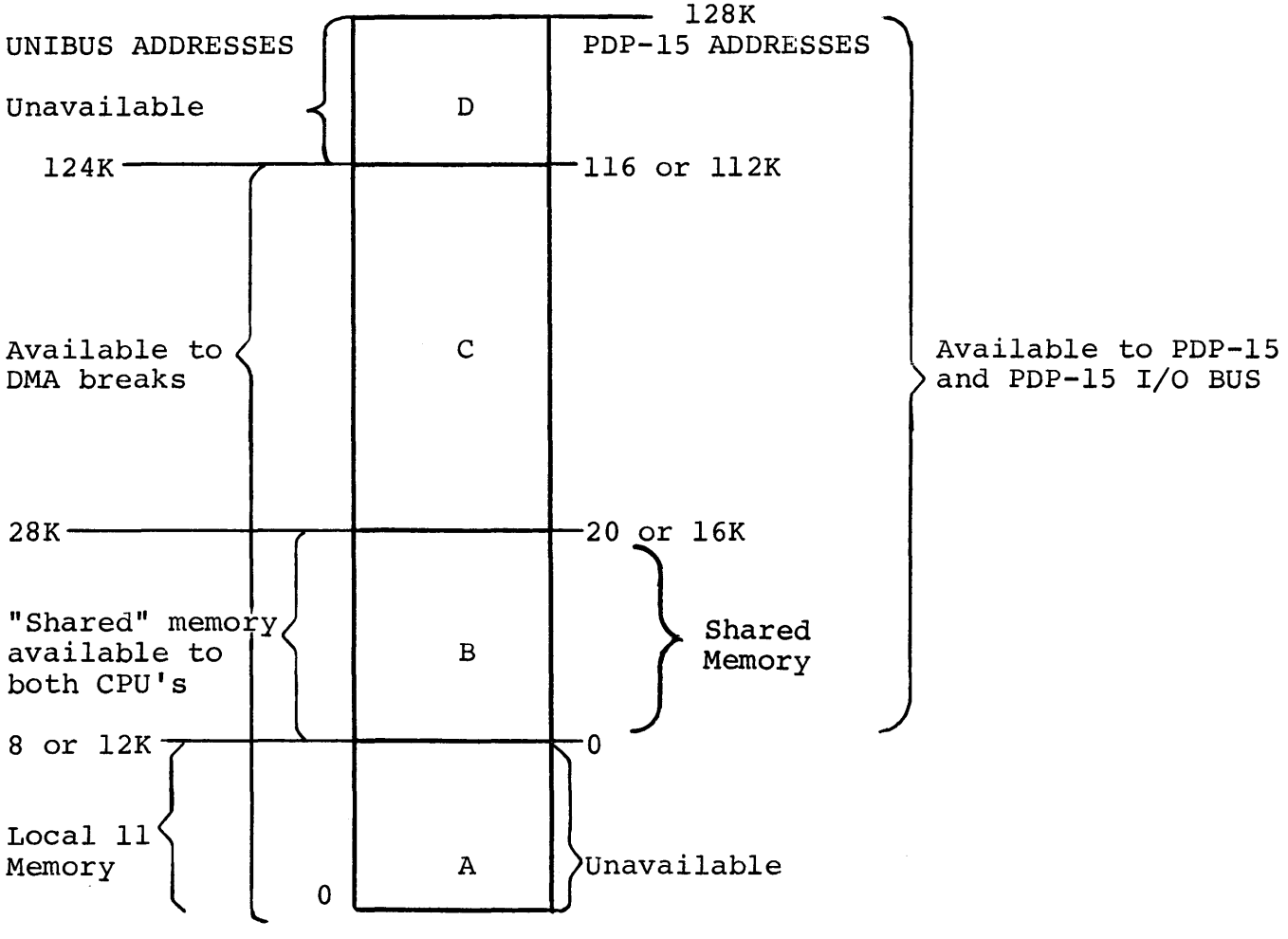


Figure 3 : DIAGRAM OF UNICHANNEL SOFTWARE SYSTEM

MEMORY LAYOUT

Figure 4 details the memory map which exists on UNICHANNEL System. Note that both the 11 and 15 parts of the system can operate concurrently, all memory contention is resolved by the MX15-B. Note also, that if the 11 system operates with area "A" complete simultinaiety is possible because no memory contention can occur.



"Local" PDP-11 Memory = A
"Shared" Memory = B
PDP-11 CPU Address Space = A + B
UNIBUS DMA Address Space = A + B + C
PDP-15 Address Space = B + C + D

Figure 4 : UNICHANNEL SYSTEM MEMORY MAP

PIREX TASKS

The PIREX software system consists of several routines to support multi-programming among tasks. These routines perform such functions as: context switching, node manipulation and scheduling. The tasks which execute in this environment are device drivers, directives to PIREX, or merely software routines which execute in a background mode.

Device drivers are tasks which typically perform rudimentary device functions (e.g.: read, write, search, process interrupts, etc.), Directives are tasks which perform some specific operation for a task under PIREX. The connecting and disconnecting tasks to/from PIREX are performed by the CONNECT and DISCONNECT directives. The third type of tasks are software routines which execute in a background mode of operation. The MACRO-11 assembler and Spooler are both run as background tasks.

To support multiprogramming among tasks, each task is required to have a format as shown in the figure below:

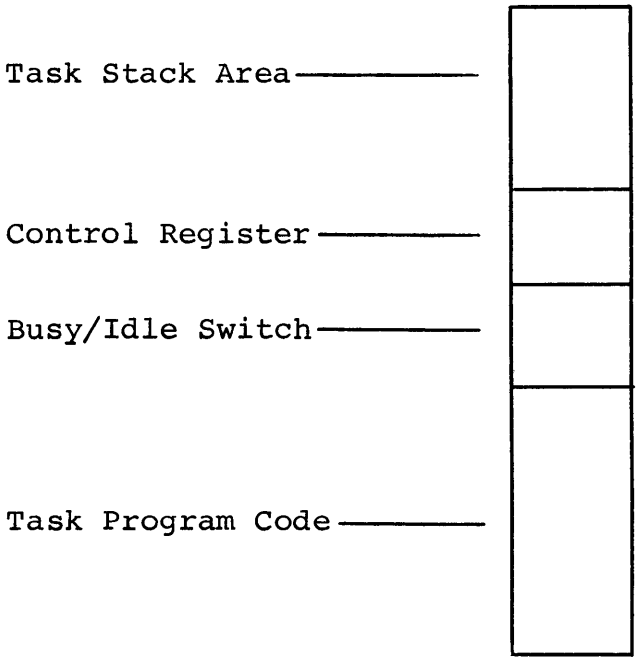


Figure 5 TASK FORMAT

The execution of a Task by PIREX is accomplished by first scanning the Active Task List (ATL). The ATL is a priority-ordered linked list of all active Tasks in the current system currently capable of running. An Active Task is one which:

1. Is currently executing.

2. Has a new request pending in its deque (double ended queue).

3. Has been interrupted by a higher priority task.

When a runnable task is found, the stack area and general purpose registers belonging to the task are restored and program control transferred to it. Program execution begins at the first location of the task program code (See Figure 2.1) or at the point where the task was previously interrupted by a higher priority task. When a task is interrupted by other tasks, its general purpose registers and stack are saved. The ATL is rescanned when a new request is issued to a task or when a previous request is complete.

When the PIREX Software System is running, it is normally executing the NUL task (a PDP-11 WAIT Instruction); The NUL task is run whenever there are no requests pending, a task suspends itself in a wait state, or while all other tasks are waiting for I/O previously initiated. When the PDP-15 issues a request to the PDP-11 to be carried out by PIREX, it does so by interrupting the 11 at Level 7 (the highest PDP-11 Interrupt Level) and simultaneously passing it an address of a Task Control Block (TCB) through the interrupt Link.

An 11 task can issue requests via the IREQ MACRO.
The contents of the TCB completely describe the request (task addressed, function, optional interrupt return address and level, status words, etc....) The TCB will usually reside in the PDP-15 memory and must be directly addressable by the 11. (i.e. It resides in shared memory).

Error conditions are passed back to the 15 in the Task Control Block (TCB) along with status information necessary for complete control and monitoring of a particular request. Usually the request is to a device on the 11 but other types are allowed.

Task Control Blocks are used for communication with PIREX and tasks running under it. The general format of a TCB consists of three words followed by optional words necessary for task communication. Optional words, generally are used to pass buffer addresses, commands and device status as may be appropriate.

```
TCB:   (API TRAP ADDRESS *400(8)) + API LEVEL
       (FUNCTION CODE *400(8)) + TASK CODE NUMBER

REV:   REQUEST EVENT VARIABLE
       (Optional Words)
```

Figure 6 STANDARD TCB FORMAT

The "TRAP ADDRESS" is a PDP-15 API trap vector and has a value between Ø and $377_{(8)}$. Location Ø here corresponds to location Ø in the PDP-15. The API Level is the priority level at which the interrupt will occur in the PDP-15 and has a value between Ø and 3. A Ø signifies API "Level" Ø , a 1 for level 1 etc... The API trap address and level are used by tasks in the PDP-11 when informing the 15 that the requested operation is complete (e.g...a disk block transferred or line printed).

The Task code number is a positive number between Ø and 128 that tells PIREX which task is being referenced, (Tasks are addressed by a numeric value rather than by name).

The Function Code determining whether hardware interrupts are to be used at the completion of the request. If the code has a value of Ø, an interrupt is generated at completion of the request; If a 1, an interrupt is not made.

The Request Event Variable, commonly called REV or just EV, is initially cleared by PIREX (set to zero) and then set to a value "n" (by the associated task) at the completion of the request. The values of "n" are:

Ø = request pending or not yet completed.

1 = request successfully completed.

-2 = (mod 2·16-1) non-existent task referenced.

-3 = (mod 2·16-1) illegal API level given (illegal values are changed to level 3 and processed).

-4 = (mod 2·16-1) illegal directive code given.

-777 = (mod 2·16-1) request node was not available from the Pool, i.e. the POOL was empty, and the referenced task was currently busy or the task did not have an ATL node in the Active Task List.

NOTE -- the Task Control Block specification clearly defines a modular communications structure with minimum impact on PDP-15 software.

ADDING DRIVERS TO PIREX

A powerful feature allows the PDP-15 to bring in a PDP-11 driver, (into either its own memory or the 11's local memory) connect it to PIREX via a connect directive (a disconnect directive) is also provided) and then issue I/O requests through PIREX to the driver. The user can now take full advantage of the existing and future PDP-11 peripherals along with an elaborate queuing structure built into PIREX allowing complete parallel processing.

MACRO 11 ASSEMBLER (MAC11) AVAILABLE)

A MACRO 11 Assembler is provided. This assembler is a Macro subset of the existing PDP-11 Macro assembler and is slightly modified to run under the control of DOS-15 and PIREX.

To accomplish this, the MACRO assembler (MAC11) is loaded by the 15 as a core image into bank 1 of the 15. MAC 11 is then connected up as a low priority driver to PIREX and requested to begin the assembly. The 11 then carries out the actual assembly while the 15 handles all of the opening and closing of files, reading and writing of test and object information until the assembly is complete. To the user at the console teletype, MAC 11 appears to be just a DOS-15 system program which is loaded in and run by the 15.

NOTE: That any customer developed software should of course, take into account PIREX context switch, the bandwidth of the UNIBUS 18 and latency consideration of the associated system.

SUMMARY

As one can easily see, the UC15 software system is a powerful tool to the user who requires the utmost in flexibility and utility. UC15 also provides an expansion capability beyond any system currently available.

INTERRUPT LINK

The following section describes the registers and control of the interrupt link. This link is used to pass Task Control Block Pointers (and through them the information in Task Control Blocks) between the PDP-15 and PDP-11 systems. The hardware which comprises this link consists of a DR15-C special purpose interface to the PDP-15, I/O BUS, and 2 DR11-C general purpose UNIBUS interfaces. The DR15-C is controlled by PDP-15 IOT's while the DR11's are accessed as registers on the UNIBUS.

Register Descriptions (PDP-11)

(CSR) 767770 Bit 6 - when bit 6 is a 1, it will enable an interrupt on BR5 to TV 300, if the API DONE flag is set in bit 7 of 767770.

Bit 7 - API DONE - set to 1 whenever none of the 4 API channels has a request pending.

NOTE: Neither of these bits is expected to be used in normal systems programming.

(ODB) 767772 Low byte - contains the API address for an API level Ø break. Loading a new value in the byte causes the appropriate API flag to be set in the DR15-C and and API break in the PDP-15 will occur, is the API is enabled and no higher activity is occuring. It also will cause a PI interrupt if API is not installed.

High byte - contains the API address for an API level 1 break. Same conditions as low byte.

(IDB) 767774 Bit Ø - contains bit "2" of the Task Control Block Pointer (TCBP). See note under bit 1.

Bit 1 - contains bit "1" of the TCBP.

NOTE: That reading 767774 does not effect the new TCBP flag in bit 7 of 767760.

Bit 6 - API 2 DONE flag - when a 1 indicates that there is no API level 2 request pending before the PDP-15. When a 1 also indicates the 767762 low byte may be loaded with a new API level 2 address to cause a new API interrupt level 2 and set the API 2 flag in the DR15-C.

Bit 7 - API Ø DONE flag - when a 1 indicates that there is no API level Ø request pending before the PDP-15. When a 1 also indicates that 767772 low byte may be loaded with a new API level Ø and set the API Ø flag in the DR15-C.

Bit 8 - Local Memory Size bit Ø - the least significant bit of a two bit field which specifies the number of 4K word memory banks that are connected to the UNIBUS.

Bit 9 - Local Memory Size Bit 1 - the most significant bit of a two bit field which specifies that number of 4K memory banks are connected to the UNIBUS.

LMS1	LMS0	
0	0	0 Local Memory
0	1	4K Local Memory
1	0	8K Local Memory
1	1	12K Local Memory

Bit 14 - API 3 DONE flag - when a 1 indicates that there is no API level 3 request pending before the PDP-15. When a 1 also indicates that 767762 high byte may be located with a new API level 1 address to cause a new API interrupt at level 3 and set the API 3 flag in the DR15-C.

Bit 15 - API 1 DONE flag - when a 1 indicates that there is no API level request pending before the PDP-15. When a 1 also indicates that 767772 high byte may be loaded with a new API level 1 address to cause a new API interrupt at level 1 and set the API in the DR15-C.

(CSR) 767760 Bit 6 - ENABLE TCBP (Task Control Block Pointer) INTERRUPT - When a 1 allows and interrupt on BR level 7 to TV 310 upon receipt of a new TCBP from the PDP-15.

Bit 7 - NEW TCBP flag - is set to 1 whenever the PDP-15 issues IOT 706006 thus placing a new TCBP in 767764 and bits 0 and 1 of 767774. It is cleared by the PDP-11 doing a DATI to location 767764.

(ODB) 767762 Low byte - contains the API address for an API level 2 break. Same conditions as 767772 low byte.

High byte - contains the API Address for an API level 3 break. Same conditions as 767772.

(IDB) 767764 TCBP (Task Control Block Pointer) - bits 3-17. This contains the lowest 15 bits of the address sent by the PDP-15. Note: that the address is "word" aligned. Note also that doing a DATI to this register lowers the New TCBP flag (767760 bit 7) and also sets the DONE flag cleared by IOT 706002 in the PDP-15.

PDP-15 IOT's

706001 SIOA - Skip I/O Accepted. Tests whether the TCBP DONE flag is set indicating the PDP-11 has read the TCBP and skips the next location if the DONE flag is a 1.

706002 CIOD - Clear I/O Done. Clear the TCBP DONE flag.

706006 LIOR - Load I/O Register and clear TCBP DONE flag. Places the contents of the PDP-15 "AC" into an 18-bit buffer register. The output of the buffer register is seen by the PDP-11 as TCBP at location 767764 and bits 0 and 1 767764. The IOT also causes the TCBP DONE flag to be cleared and in the PDP-11 causes bit 7 to be set in location 767760, which in turn causes the PDP-11 to do an interrupt at BR 7 to TV location 310.

706112 RDRS - Read Status Register - Clears the AC and loads the contents of the DR15-C status register into the AC. (This effectively moves the DR15-C enable interrupt bit into bit 17 of the AC).

706122 LDRS - Load Status Register. Loads the contents of the AC into the DR15-C status register. (Places value of AB bit 17 in the DR15-C "enable interrupts" bit).

706104 CAPIO - Clear APIO flag in DR15-C.

706124 CAPI1 - Clear AP11 flag in DR15-C.

706144 CAPI2 - Clear AP12 flag in DR15-C.

706164 CAPI3 - Clear AP13 flag in DR15-C.

706101 SAPIO - Tests the AP10 flag in the DR15-C and skips the next instruction if the flag is 1.

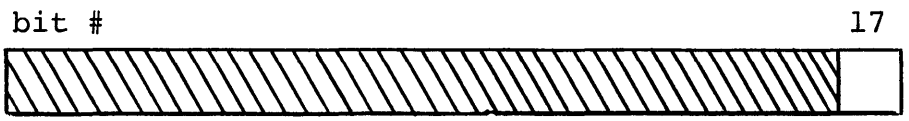
706121 SAPI1 - Tests the API1 flag in the DR15-C and skips the next instruction if the flag is 1.

706141 SAPI2 - Tests the API2 flag in the DR15-C and skips the next instruction if the flag is 1.

706161 SAPI3 - Tests the API 13 flag in the DR15-C and skips the next instruction if the flag is 1.

PDP-15 STATUS REGISTER (DR15-C)

Bit 17 Enable PI/API interrupts. When a 1 enables interrupts from the PDP-11 processor. Note this bit is set to a 1 by initialize and the CAF instruction. It can only be cleared by using the LDRS (IOT 706122) instruction.

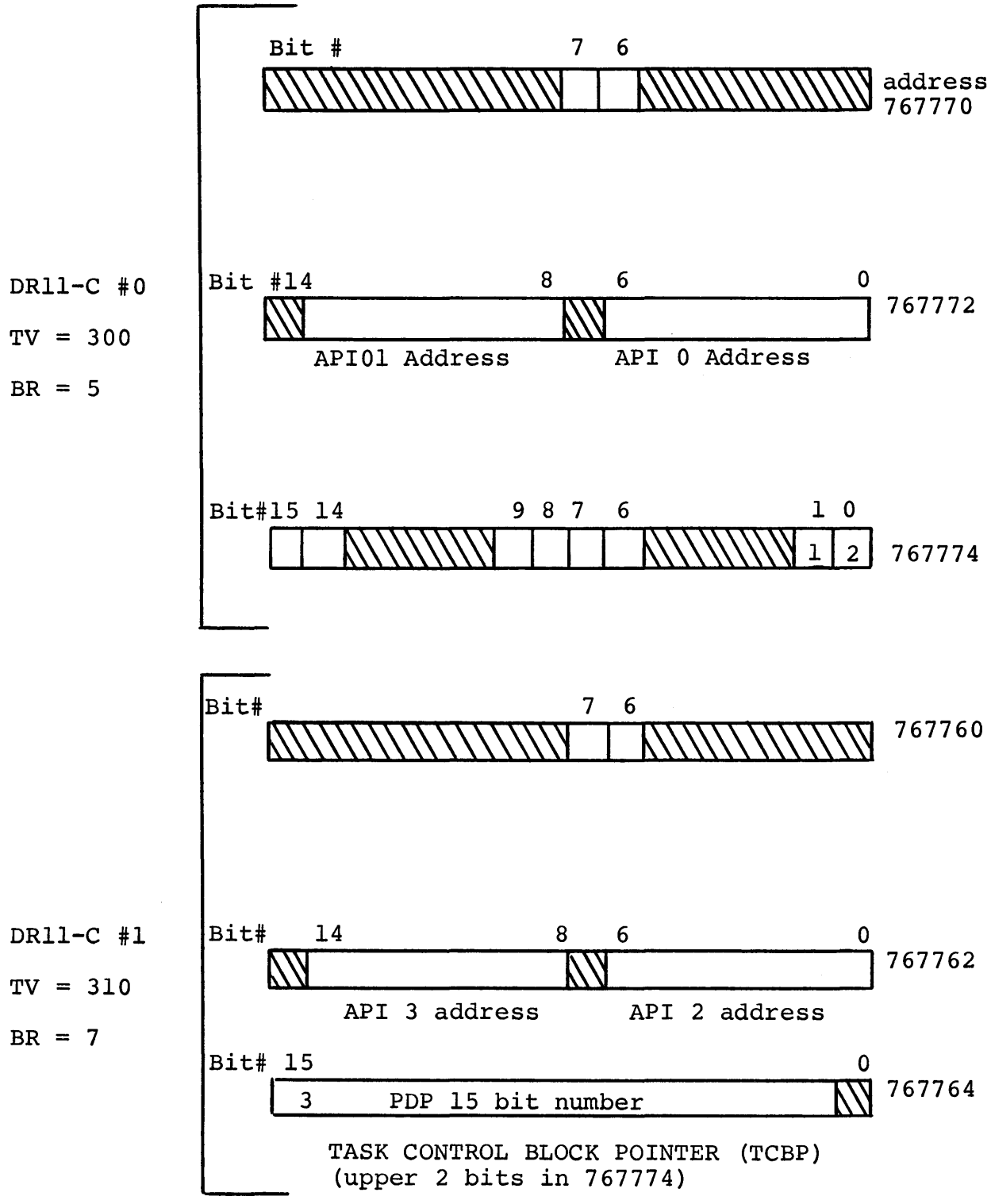


enable PI/API

Figure 7

Figure: 8

PDP-11/05 CONTROL REGISTERS



MX15-B MEMORY MULTIPLEXERS

When the PDP-15 memory is accessed by the PDP-11/05 or any NPR UNIBUS device, the addresses are relocated by the MX15-B multiplexer.

The MX15-B multiplexer not only relocates the UNIBUS addresses but emulates byte operations in PDP-15 memory. Hence normal PDP-11 programs, with byte read and byte write operations may be executed from PDP-15 memory. Also such byte oriented NPR devices as Mag Tape may make transfers directly to PDP-15 memory.

Note: That the PDP-11 processor can access the PDP-15 memory which is between the end of local memory and the 28K of address space available to its address scheme.

A. Output - PDP-15 Memory Bus

Will connect to MM15, MX15-A, and ME15 memories.

B. Inputs

PDP-11: Modified UNIBUS with PA and PB used as D16 and D17 respectively. It meets all other UNIBUS specs. Defined as UNIBUS/18, input would have a lower address bound that could be fixed to any 4K multiple address 0-120K. This would be specified as jumpers. Note that only 8K and 12K of local memory will be supported by diagnostics and systems programs. Hence, the maximum commonly addressable memory (11 processor) will be 20K or 16K. An upper limit would be provided as 124K.

The addresses presented from the PDP-11 are relocated to prevent location 0 being the same physical address on each machine. The PDP-11 will be able to be relocated by 4K increments to 124K. Local PDP-11 memory is restricted to 4 increments.

Note that any "write" operation to a common memory location by 8 bit or 16 bit UNIBUS devices causes PDP-15 data bits 0 and 1 of the location to be forced 0.

PDP-15: Standard 15 Memory Bus Interface - no upper and lower bounds. No relocation. Emphasis is on minimum delay through multiplexer for this port.

If both processors request at the same time, PDP-15 will get use of the memory. When requests are not simultaneous, a first come, first served mode operates. Practically, all this means is that the 15 and 11 will alternate access to common memory except under the special conditions described above. NOTE: No local memory is provided on the PDP-15.

Bus Loading: MX15-B.....2 PDP-15 memory bus load
Drives 4 PDP-15 memory bus loads

DR15-C/DR11-C...1 Unibus Load
1 PDP-15 I/O bus load

Power: (Steady State)
UNICHANNEL 15 (no peripherals)..5 at 115V
2.5A at 230V

Voltage: 115 Vac $\pm$ 10% or 230 Vac $\pm$ 10%

Frequency: 50 $\pm$ 2 Hz or 60 $\pm$ 2 Hz

Environmental: Temperature.....10^{o} to 50^{o}C
Relative Humidity.....20% to 95%

UC15 Cabinet Dimensions: Depth:....30in (0.76m)
Width:....21 in. (0.53m)
Height:...72 in. (1.83m)
Weight:...150 lbs. (70 kg)-not including peripherals.

Unibus Compatability: Can be used with any PDP-11 family processor that does not use parity. On those systems with parity, the parity must be disabled.

Memory Cycle: MX15-B normally adds 200 ns to both the PDP-15 and the PDP-11 cycle times.

DMA Facility to Common Memory:

Maximum transfer rate.....415K words/sec
Worst-case latency.....6 μs (no DCH transfers in PDP-15)
12 μs (DCH transfers in PDP-15)
Average latency.....2.5 μs

DMA Facility to PDP-11/05 Local Memory:

Maximum Transfer rate.....1 million words/sec
Worst-case latency.....7.2 μs
Average latency.....2.5 μs

SYSTEM CONFIGURATION

The UC15 cabinet will replace the curent disk cabinet immediately to the left of the PDP-15 processor.

The increased spacing will require longer I/O or memory bus cables in some installations.

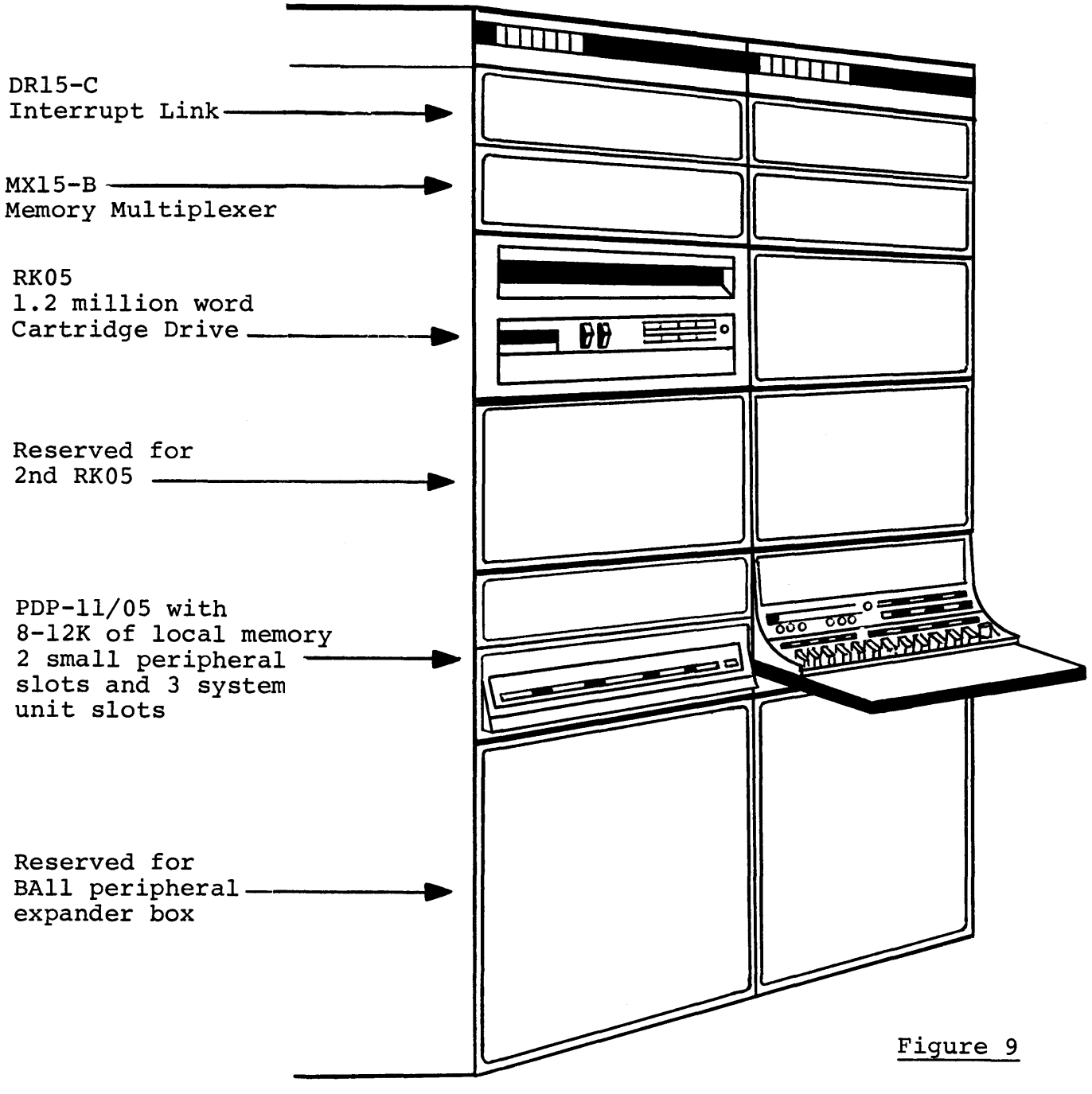


Figure 9

SYSTEM RESTRICTIONS

RK05 (RK11) Disk Pack Capability

The 18 bit RK11 disk pack will not be able to be read by RK11-C or RK11-D system (16-bit only systems).

This means that data bases and PDP-11 files created on 18-bit RK11 systems may not be taken directly to an PDP-11 only system. The transfer medium for such a transfer would have to be Mag Tape.

This situation was chosen to make RK11-C and RK11-D packs compatible (i.e. ....all PDP-11 only systems).

Memory Limits

UNIBUS NPR devices can access a maximum of 124K. The amount of shared memory available to UNIBUS NPR devices is 124K less the amount of local memory. In a "normal" configuration the PDP-11/05 would have 8K of memory, in which case the available PDP-15 memory would be limited to 116K. This limit is due to the fact that UNIBUS/18 peripherals must have access to all memory. The maximum memory of the 11 without some relocation option would be 28K.

Note: That the PDP-11 with 8K of local memory can only address the lowest 20K of common memory to access Task Control Blocks set up by the PDP-15.

I/O Latency

Multiport memories always have increased worst case latency over a single port-non-competitive situation. This system is no exception. The PDP-11 normally gives an "NPR break" a worst case latency to BSSY of 7.0 usec. On this system, we must add to that time, the time it requires the PDP-15 to do three I/O memory cycles (5.0 usec.). The worst case latency is, hence, 12.0 usec.

CAF/RESET Limitations

The following timing considerations are of interest to programmers:

A RESET instruction may cause the PDP-15 to incorrectly read the API address. The Console RESET and CAF instruction may violate UNIBUS specifications. Hence, random "initialize" pulses may cause system malfunctions. The following guidelines must always be followed:

1. CAF must not be executed while there is a Task Control Block Pointer (TCBP) waiting to be read by the PDP-11.

2. RESET must not be executed while there are API requests pending for the PDP-15.

3. RESET must not be executed if there is any NPR activity on the UNIBUS. All active NPR devices must be shut down in a power fail sequence prior to executing RESET.

PDP-15 UNICHANNEL OPTIONS

UC15-HE	Peripheral Processor: 11/05 or 11/10-NC or - SA, 2 DR11-C, DR15-C, MX15-B, DD11-B, KY11-JH, H950, 115V.	8K Local Memory
UC15-HF	Peripheral Processor: 11/05 or 11/10-ND or - SB, 2 DR11-C, DR15-C, MX15-B, DD11-B, KY11-JH, H950, 230V.	8K Local Memory
UC15-HK	Peripheral Processor: 11/05 or 11/10 - NC or - SA, 2 DR11-C, DR15-C, MX15-B, DD11-B, KY11-JH, H950, MM11-K, 115V.	12K Local Memory
UC15-HL	Peripheral Processor: 11/05 or 11/10-ND or - SA , 2 DR11-C, DR15-C, MX15-B, DD11-B, KY11-JH, H950, MM11-K, 230V.	12K Local Memory
RK15-HE	RK05-AA, RK11-E, UC15-HE, 115V, 60Hz	
RK15-HF	RK05-BB, RK11-E, UC15-HF, 230V, 50Hz.	
RK15-HH	RK05-AB, RK11-E, UC15-HF, 230V, 60Hz.	
RK15-HJ	RK05-BA, RK11-E, UC15-HE, 115V, 50Hz.	
RK15-HK	RK05-AA, RK11-E, UC15-HK, 115V, 60Hz.	
RK15-HL	RK05-BB, RK11-E, UC15-HL, 230V, 50Hz.	
RK15-HM	RK05-AB, RK11-E, UC15-HL, 230V, 60Hz.	
RK15-HN	RK05-BA, RK11-E, UC15-HK, 115V, 50Hz.	
15/76-DE	KP15, ME15-EA, LA30-CA, PC15, KE15, KW15, TC15, TU56, RK15-HE, 115V, 60Hz.	
15/76-DF	KP15, ME15-EB, LA30-CD, PC15-A, KE15, KW15, TC15, TU56, RK15-HF, 230V, 50Hz.	
15/76-DK	KP15, ME15-EA, LA30-CA, PC15, KE15, KW15, TC15, TU56, RK15-HK, 115V, 60Hz.	
15/76-DL	KP15, ME15-EB, LA30-CD, PC15-A, KE15, KW15, TC15, TU56, RK15-HL, 230V, 50Hz.	
15/76-ME	KP15, ME15-EA, LA30-CA, PC15, KE15, KW15, TC59-D, TU10, RK15-HE, 115V, 60Hz.	

15/76-MF	KP15, ME15-EB, LA30-CD, PC15-A, KE15, KW15, TC59-D, TU10, RK15-HF, 230V, 50Hz.
15/76-MK	KP15, ME15-EA, LA30-CA, PC15, KE15, KW15, TC59-D, TU10, RK15-HK, 115V, 60Hz.
15/76-ML	KP15, ME15-EB, LA30-CD, PC15-A, KE15, KW15, TC59-D, TU10, RK15-HL, 230V, 50Hz.

NOTE: For further information and extra copies of this manual please contact the PDP-15 Marketing Department at the following address:

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