PERMANENT MEMORANDUM

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SUBJECT Programmed Data Processor - 4 Technical Specification

TO PDP Distribution List

ABSTRACT This is the specification for the PDP-4 computer - an 18-bit, 10-microsecond machine designed by DEC.

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TECHNICAL SPECIFICATIONS

FOR

PROGRAMMED DATA PROCESSOR - 4

I. DESCRIPTION

The DEC Programmed Data Processor - 4 is a stored program digital computer designed for use as a component with other equipment such as keyboards, printers, analog/digital converters, typewriters, paper-tape punches, etc. The stored program concept brings the flexibility and economy of a standard product to applications which have required special purpose systems.

The PDP-4 is a single-address, 18-bit fixed-word, parallel computer. It can have either 1024, 4096, or 8192 words of core memory with a cycle time of 9 microseconds. A complete order code structure, indirect addressing, and program/data interrupt are standard features.

II. BLOCK DIAGRAM DISCUSSION

A block diagram of the PDP-4 system is shown in Figure 1. The machine is a device which distributes information to, and collects information from other devices, according to a stored program (or set of rules).

A. Internal Processor

The Internal Processor carries out arithmetic operations, controls memory, and controls information entering and leaving the machine.

B. Operator Console

The Console enables the status of the Internal Processor to be observed, and modified, and consists of lamps and switches.

C. Memory

The Memory provides a storage for instructions to be performed by the Internal Processor. It also holds information being collected or distributed.

D. Information Collection and Distribution Device Selection

This functional block provides collection facilities for incoming information, buffering for outgoing information, and control for devices operated by the program.

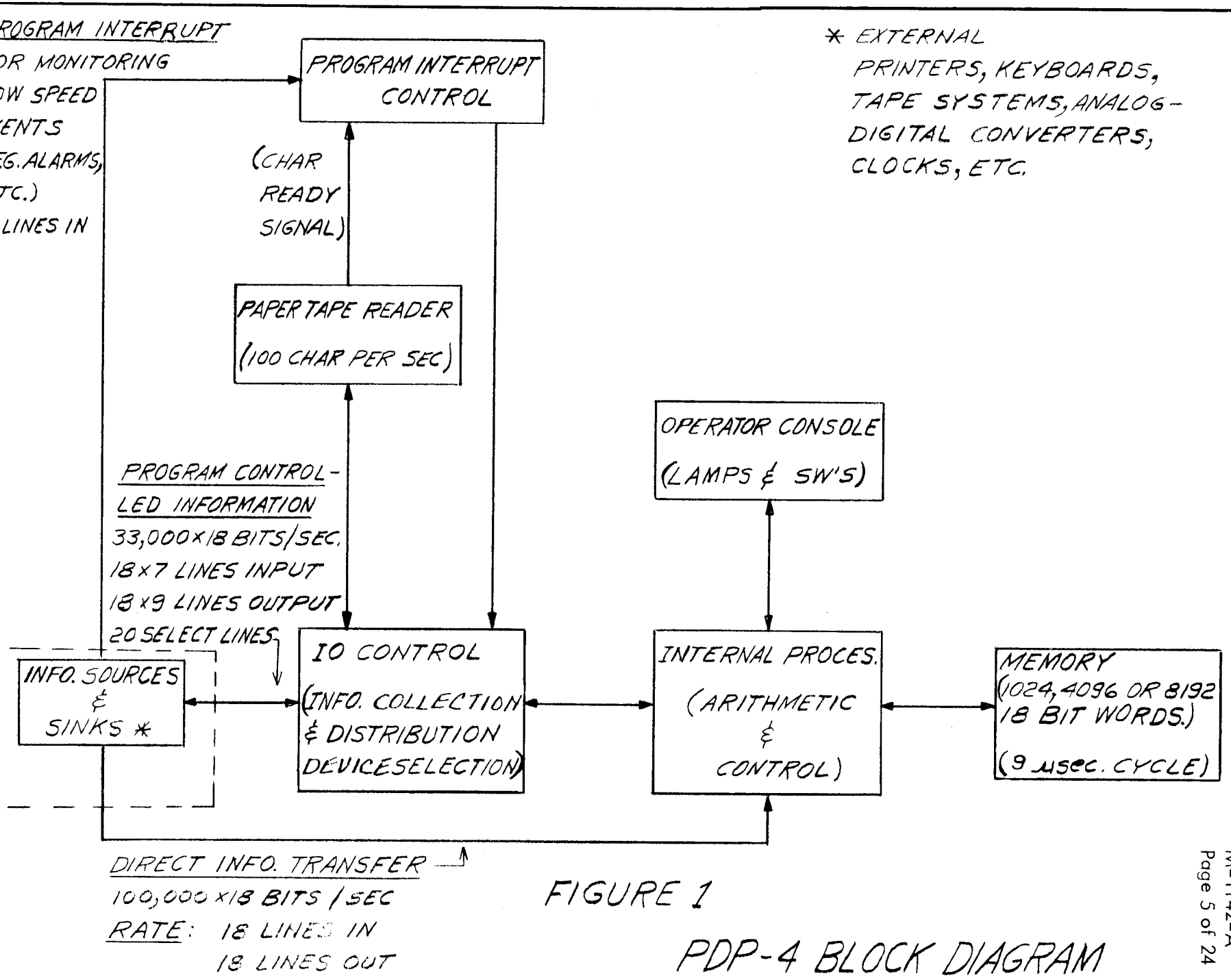


FIGURE 1

PDP-4 BLOCK DIAGRAM

E. Tape Reader

The Tape Reader allows information to be read from perforated paper tape, through the information collector, to the Internal Processor.

F. Program Interrupt Control

This control provides the Internal Processor with information about interruption requests. Whenever a request (flag) is a "one", the control interrupts the program.

III. DETAILED REGISTER CONFIGURATION

The computer registers and control elements in the Internal Processor are shown in Figure 2.

The registers function as follows:

A. Memory Address Register (MA)

This 13-bit register is used to address (or select) a memory word or cell. Thus, 8192 words of memory can be directly addressed.

The MA can be cleared. Information can be read in from MB, PC, or external sources.

B. Memory Buffer Register (MB)

This 18-bit register holds information that is read from a selected memory cell (specified by MA). Upon reading information from a cell, the cell is cleared.

The MB also specifies the information written back into the selected cell. The cycle time of the memory, 9 microseconds, is the time required to read information from a cell (which clears the cell) and re-write the same (or different) information into the cell.

The MB can be cleared. Information can be read in from memory, PC, AC, or external sources. A one can be added to the contents of MB.

C. Program Counter

This is a 13-bit register which contains the address of the cell in memory from which the next instruction will be taken.

The PC can be cleared. Information can be read in from MA, MB, or ADDRESS Switches (AS). A one can be added to the contents of MA.

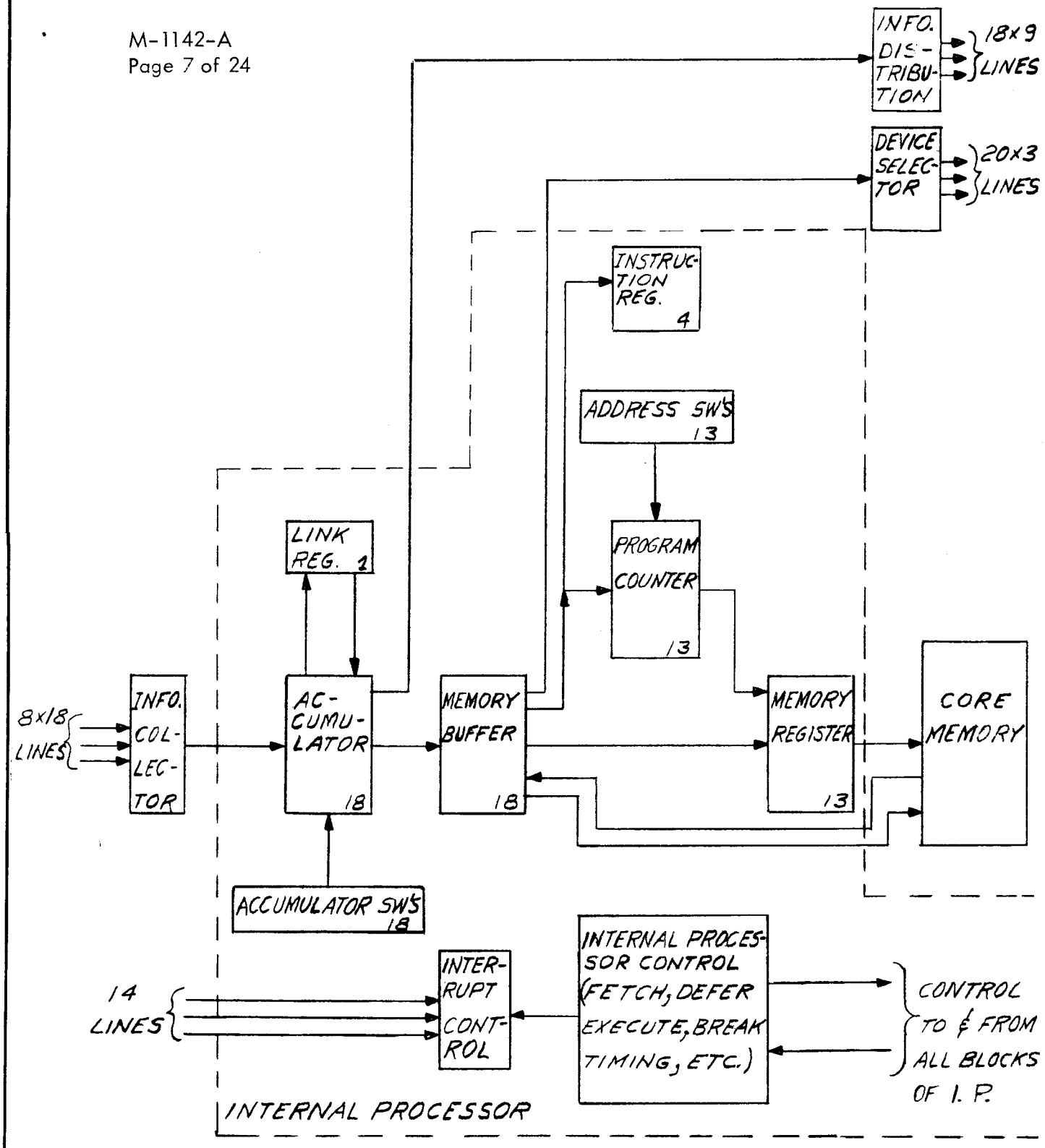


FIGURE 2

INTERNAL PROCESSOR

D. Instruction Register (IR)

This 4-bit register contains the instruction currently being performed by the machine.

Information can be read into IR from the MB.

E. Accumulator (AC)

This 18-bit register, together with the MB, performs the arithmetic operations. The AC can be cleared, complemented, shifted right or shifted left. The C(MB)* can operate on the C(AC) to form the arithmetic sum (one's or two's complement), the logi-can AND, or exclusive OR. The result remains in AC.

The logical OR of the C(AC) and the AC switches may be placed in the AC.

F. Carry Link (L)

This 1-bit register is used to extend the facilities of the AC. It may be cleared, complemented, and shifted (as part of the AC). It is used as an overflow flip-flop for 1's complement arithmetic and as a carry register for 2's complement arithmetic. This feature greatly simplifies multiple precision arithmetic.

IV. PRIMARY CONTROL STATES

A. Fetch (F)

This state is present during the memory cycle when a cell is brought from memory as an instruction. The cell specified is the C(PC). PC is incremented by one during Fetch.

B. Execute (E)

This state occurs for those instructions requiring an operand and is the memory cycle during which the operand is obtained and the instruction is executed.

C. Defer (D)

The defer state is that cycle during which the effective address is obtained. The defer state is selected by placing a "one" in bit position 5 of the instruction. When deferring is specified, a memory cycle occurs during which the contents of the cell of the deferred address are used to form the effective address. The instruction part of the cell is ignored when obtaining the effective address.

* C(MB) means the contents of MB.

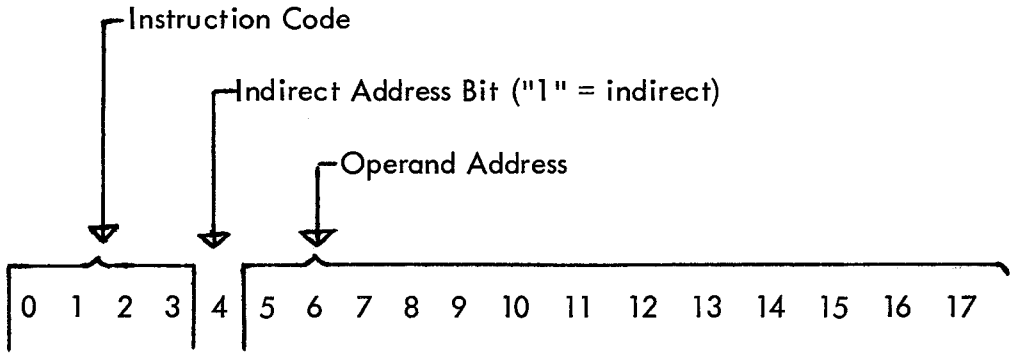
D. Break (B)

The break state occurs when external sources are either transferring information with memory or controlling the sequence of the program. A data interruption or program interruption causes this state.

V. INSTRUCTIONS

A. Memory Reference Instructions

The Memory Reference instructions are defined below. The format of instruction word bits is:



Memory Reference Instructions

Mnemonic Code	Octal Code	Time (μsec)	Operation
dzm Y	00	18	Deposit zero in memory. The contents of register Y are changed to zero. The original contents of Y are lost. 0 =>* C(Y)
dac Y	04	18	Deposit Accumulator. C(AC) are deposited in memory register Y. The C(AC) are unaffected by this operation. C(AC) => C(Y)
jms Y	10	18	Jump to Subroutine. C(PC) are deposited in memory register Y. The next instruction will be taken from Y + 1, the beginning of the subroutine. C(PC) => C(Y), Y+1 => C(PC)

* => means replaces

Memory Reference Instructions (continued)

Mnemonic Code	Octal Code	Time (μsec)	Operation
lac Y	20	18	Load AC. The (CY) replace the C(AC). The previous C(AC) are lost. The C(Y) are unaffected. C(Y) => C(AC)
xor Y	24	18	Exclusive OR. The exclusive OR logical function is performed on a bit-by-bit basic between the C(AC) and C(Y). The result is left in the AC and the original C(AC) are lost.
add Y	30	18	One's Complement Add. The C(Y) are added to the C(AC) in 1's complement arithmetic.* The result is left in the AC and the original C(AC) is lost. The Link bit is set to a one if the magnitude of the sum of C(Y) and C(AC) is greater than $2^{17} - 1$. C(AC) + C(Y) => C(AC)

$C(AC)_i$ original	$C(Y)_i$	$C(AC)_i$ final
0	0	0
0	1	1
1	0	1
1	1	0

*In 1's complement arithmetic, negative numbers are represented by a "1" in the sign position (bit 0 or left-most bit) of the word. Each digit of the word decreases in significance from bit 1 to bit 17. The negative of a 1's complement number is formed by complementing the number. The complement of a binary number is formed by changing all ones to zeros and all zeros to ones. In 1's complement convention the number zero may be represented by either all ONE's (-0) or by all ZERO's (+0). Minus zero results when:

1. adding -0 and -0
2. adding -n and +n
3. adding -0 and +0

Memory Reference Instructions (continued)

Mnemonic Code	Octal Code	Time (μsec)	Operation
tad Y	34	18	Two's Complement Add. The C(Y) are added to C(AC) in 2's complement arithmetic.* If there is a carry out of bit 0 of the Accumulator, the Link will be set to ONE. This feature is useful in multiple precision arithmetic. C(AC) + C(Y) => C(AC)
xct Y	40	9+ instruction execute time	The instruction in register Y will be executed. The computer will act as if the instruction located in Y were in the place of the xct Y.
isz Y	44	18	Index and Skip if Zero. The C(Y) are replaced by C(Y)+1. The C(AC) are unaffected by this instruction. The addition is done using two's complement arithmetic. If the resulting sum is zero, the instruction following the isz is skipped. C(Y)+1 => C(Y), if C(Y)+1 =0 then C(PC)+2 => C(PC)
and Y	50	18	Logical AND. The logical AND function is performed on a bit-by-bit basis between C(AC) and C(Y). The result is left in the AC and the original C(AC) are lost. $C(Y)_i$** · $C(AC)_i$ => $C(AC)_i$.

$C(AC)_i$ original	$C(Y)_i$	$C(AC)_i$ final
0	0	0
0	1	0
1	0	0
1	1	1

* In 2's complement arithmetic, a negative number is represented by a "1" in the sign position. The negative of a 2's complement number is formed by complementing it and adding one to the result.

** $C(Y)_i$ means C(Y), bit i.

Memory Reference Instructions (continued)

Mnemonic Code	Octal Code	Time (μsec)	Operation
jmp Y	60	9	Jump. The C(PC) are reset to address Y. The next instruction that will be executed will be taken from memory register Y. The original contents of the PC are lost. Y => C(PC)

B. Augmented Instructions

The augmented instructions are defined as follows:

Mnemonic Code	Octal Code	Time (μsec)	Operation
opr	74	9	Operate. The operate instruction is a microprogramming instruction. That is, various actions are specified by individual bits in the "address" portion of the instruction. Within certain restrictions, several actions can be called for in the same operate instruction. The operate is also the conditional skip instruction. When a particular condition is present, the following instruction will be skipped. The operations are specified by bits as indicated in Table 1.
iot	70	9	In-Out Transfer. This instruction is used to select an input or output device. The instruction forms a microprogram and has the format indicated in Table 2.

TABLE 1. OPERATE INSTRUCTION GROUP

Mnemonic Code	Operation		Octal Code of Address Part	Sequence (or time) of Occurrence (0, 1, 2, or 3)
cla	Clear AC, 0 => C(AC)		10,000	1
cll	Clear Carry Link, 0 => C(L)		4,000	1
cma	Complement AC, $\overline{C(AC)}$ => C(AC)		1	2
cml	Complement Carry Link, $\overline{C(L)}$ => C(L)		2	2
ral	Rotate AC and L left one position $C(AC_i) \Rightarrow C(AC_{i-1})$ $C(AC_0) \Rightarrow C(L)$, $C(L) \Rightarrow C(AC_{17})$		10	2
rar	Rotate AC and L right one position $C(AC_i) \Rightarrow C(AC_{i+1})$ $C(AC_{17}) \Rightarrow C(L)$, $C(L) \Rightarrow C(AC_0)$		20	2
oas	"Inclusive OR" AC Switches with AC $C(ACS) \vee C(AC) \Rightarrow C(AC)$		4	2
hlt	Halt the machine, 0 => C(RUN)		40	3
sza	Skip on zero AC (plus zero)	3-bit decoding	100	0
sna	Skip on non-zero AC		200	0
spa	Skip on plus AC		300	0
sma	Skip on minus AC		400	0
spl	Skip on L = 0		500	0
sml	Skip on L = 1		600	0

TABLE 2. IN-OUT TRANSFER INSTRUCTION GROUP

Function	Command Bits
Specifies the in-out instruction (Operation Code 70)	0-3
May be used to select sub-device	4-5
Selects the device	6-11
May be used to select sub-device	12
Clears the AC at event time 2 if a "one"	13
Clears the AC at event time 1 if a "one"	14
Transfers an IOT pulse at event time 3 if a "one"	15
Transfers an IOT pulse at event time 2 if a "one"	16
Transfers an IOT pulse at event time 1 if a "one"	17

Bits 13-17 may be used together in any combination to allow various types of in-out command structures, and these may handle 1, 2, or 3 devices per selection (bits 4 - 12) depending upon the requirements of the device. The spacing between event times is 2 microseconds. It is possible to form 3×2^9 unique selection pulses on 3×2^9 separate wires.

VI. OPERATOR CONSOLE

The function of the keys, switches, and indicators on the control panel is given in Tables 3, 4, and 5, respectively.

TABLE 3. CONSOLE KEYS

Key	Function
START	Starts the computer. The first instruction is taken from the memory at the address indicated by the ADDRESS switches.
STOP	Causes the computer to stop at the completion of the memory cycle in progress at the time of key operation
CONTINUE	Causes the computer to resume operation, beginning at the address specified by the PC.
EXAMINE	Sets the contents of the memory cell selected by the ADDRESS switches into the AC and MB. The MA will contain the address of the memory cell being examined. The PC will contain the address of the next memory cell.
DEPOSIT	Sets the word selected by the ACCUMULATOR switches into the memory at the location specified by the ADDRESS switches. The results will remain in the AC and MB. The MA register will contain the address of the memory cell holding the information. The PC will contain the address of the next cell.
EXAMINE NEXT	Sets the contents of the memory, at the address specified by the PC, into the AC and the MB. The C(PC) are indexed by one. The MA will contain the address of the register examined.
DEPOSIT NEXT	Sets the contents of the ACCUMULATOR switches into the memory at the location specified by the PC. The C(PC) will be indexed by one. The MA will contain the address of the register holding the information.

TABLE 4. CONSOLE SWITCHES

Switch	Function
ACCUMULATOR	Contains a word to be manually deposited into memory by means of the DEPOSIT or the DEPOSIT NEXT key, or to be brought into the AC under program control.
ADDRESS	Contains the memory address for the START, EXAMINE, and DEPOSIT keys.
SINGLE STEP	Causes the computer to halt at the completion of each memory cycle. Repeated operation of the CONTINUE key will step the program one cycle at a time so that the state of the machine can be examined at each step.
SINGLE INSTRUCTION	Causes the computer to stop at the completion of each instruction.
REPEAT	Causes operations initiated by a key to be repeated as long as the key is depressed. The operations are performed at the rate set by the SPEED switch.
POWER	Turns on power.
SPEED	Controls the REPEAT interval from approximately 40 microseconds to 8 seconds.

TABLE 5. CONSOLE INDICATORS

Indicator(s)	Function
ACCUMULATOR	Indicates the contents of the Accumulator.
MEMORY BUFFER	Indicates the contents of the Memory Buffer register.
INSTRUCTION	Indicates the binary code of the instruction being executed.
MEMORY ADDRESS	Indicates the contents of the Memory Address register.
PROGRAM COUNTER	Indicates the contents of the program counter.
LINK	Indicates the contents of the Carry Link.
BREAK, EXECUTE, DEFER, FETCH	Indicates that the next memory cycle will be an execute, break, defer, or fetch primary control state, respectively.
RUN	Indicates the computer is executing instructions.

VII. PROGRAMMED IN-OUT CONNECTIONS

A. General

The input-output equipment operation consists of specifying iot instructions which affect the state of selected devices. The iot instruction is microprogrammed to allow one basic instruction to handle many devices (by changing the bits of the command). The command pulses occur at various times to allow flags to be sampled (and an instruction skipped), buffers to be cleared, data to be transmitted to or from the AC, and action to be taken by the devices. All data are transmitted to or from the AC.

The various portions of the machine which handle these control and information transmission functions are shown in Figure 2.

B. Device Selector (DS)

The Device Selector (DS) consists of a group of coded elements which produce pulses when the iot instruction corresponding to its address code is given. The DS pulses occur at event times 1, 2, and 3 and are present if the appropriate code bit (bits 17, 16, and 15) is present in the iot instruction. Each event time is separated by 2 microseconds. If another element is added in the Device Selector, 3 additional coded pulses are available. The selector pulses are standard DEC 500KC logic pulses. A selector pulse can drive 18 units of base load, when used according to the rules given in the DEC Digital Logic Handbook. Functionally, the pulses can be used to:

a. Set or reset control flip-flops.

b. Transmit information to an external register from PDP-4 through the Information Distributor.

c. Read in information to PDP-4 from external registers or devices through the Information Collector.

Bits 6-12 of the iot instruction select the pulses, thus up to 2^6 or 64 elements can form the DS, giving 64 x 3 unique pulses on 64 x 3 wires. The pulses are 0.4 microseconds in duration, and -3 volts in amplitude. The standard DS contains provisions for up to 20 selector elements.

C. Information Collector (IC)

The IC allows information to be collected. Information must appear in the form of static levels, and these levels are read into the AC by Device Selection (DS) pulses. The read-in (sampling, or strobing) operation consists of applying a DS pulse to the strobe input of the IC, which "ands" with the information present, and the results are transmitted to the AC. The AC must contain a 0 at the time the inputs are sampled.

All 18 information inputs to the IC are sampled simultaneously. The program for "reading in" is:

a. cla - Clear AC (AC must equal 0).

b. iot - Selected device (sample the selected AC inputs or device outputs).

c. dac Y - Deposit C(AC) (the C(AC) is sent to a particular memory cell, Y).

The IC has connections for 8 groups of 18 bit information inputs, and 8 strobe inputs. Thus, 8 x 18 signals may be interrogated. The PDP-4 is equipped with 4 groups active, of the 8 possible groups. Additional DEC modules may be added to activate the remaining 4 channels.

The incoming information signal polarities are:

0 volts = binary "0" bit transmitted to AC.

-3 volts = binary "1" bit transmitted to AC.

D. Information Distributor (ID)

The Information Distributor distributes the static information, contained in the AC, to various devices. The output signals of the ID are sent to all devices requiring AC information. The devices then sample the ID with the DS pulses when required.

The program for transmitting information from a particular cell is:

a. lac Y - Load the AC with contents of cell Y.

b. iot clear selected output register - Prepare for information.

c. iot transmit - The information is sampled and placed in output register.

The signal polarities are:

-3 volts = AC bit contains a "0"

0 volts = AC bit contains a "1"

Eight (8) groups of 18 outputs are available in the ID.

E. I-O SKIP Facility (IOS)

The IOS facility allows PDP-4 programs to skip (or branch) according to various extra machine (or IO) states. There are 8 inputs to IOS. The DS pulses strobe an input, and if the condition is present, the instruction following the iot which gave the DS pulse will be skipped.

The conditions for skipping are:

-3 volts = skip

0 volts = do not skip

The DS pulse must occur at event time 1.

VIII. IN-OUT EQUIPMENT OPERATION

A. General

The operation of the input-output equipment connected to PDP-4 is handled by various DS select pulses. The select pulses are:

a. Sample device flag conditions which are fed into IOS.

b. Reset external registers.

c. Read in information to external registers from AC via the ID.

d. Read in information from external registers to the AC via the IC.

e. Control the device.

B. Punched-Paper Tape Reader

PDP-4 contains a tape reader which reads 5, 7, or 8 hole perforated tape at the rate of 100 lines per second.

The reader control logic contains an 18-bit buffer (RB) which is used to collect an 18-bit word in one of the operating modes. The logic contains a flag which is up (or a one) when RB is full. The RB can be read into the AC, and the flag can be cleared. The address of the reader command set is 01.

The octal instructions for the tape reader are:

700101 Skip the following instruction if the RB full flag is a one.

700112 Clear the AC. Clear the RB full flag. Read in the RB contents into AC.

700144 Clear the RB full flag. Clear the RB. Fetch an 8-bit word from tape. The alphanumeric character, lateral 8 holes on tape, is read into the least significant bit positions, 10 - 17.

700104 Clear the RB full flag. Clear the RB. Fetch an 18-bit binary mode word from tape. A line of tape is read in the binary mode only if hole 8 is punched. Hole 7 is ignored and the remaining 6 holes constitute 2 octal digits or 1/3 of an 18-bit word; thus 3 lines of tape are read and assembled.

A sequence of instructions (in memory locations 40-43) to fetch an alphanumeric character from paper tape and place the character in AC is:

```
40/   700104   /Request character
41/   700101   /Skip instruction when character
42/   600041   /Return to check flag
43/   700112   /Clear AC, read in the character
```

C. Printer-Keyboard (Optional)

The Printer-Keyboard is Teletype Model 28, consisting of a printer and keyboard. Commands can be given to print or to interrogate the keyboard. The speed of keyboard input or printing is 10 characters per second. Each time a key is struck, the 5-bit code for the key struck is placed in the Keyboard Buffer (KB), and the KB full flag is set to a one.

The keyboard commands are DS pulses, 03, and are:

700301 Skip the next instruction if KB is full (the KB full flag is a one).

700312 Clear the AC. Clear the KB full flag. Read the contents of KB into the AC, via the IC. The code is read into AC bit positions 13 - 17.

The printer control allows information to be printed through a Printer Buffer (PTB). A flag is used to signal when PTB is free, or when the printer may print the next character. The commands which control PTB are the DS series 04 and are:

700401 Skip if the PTB free flag is a one. (Printer is available for next character.)

700402 Clear the PTB. Clear the PTB free flag.

700404 Read the 5-bit code for the character to print into PTB from AC (via ID) bits 13 - 17. Print the character specified by the code. The PTB flag will become a "one" when the character is finished printing.

700406 Clear the PTB. Clear the PTB free flag. Read the code for the character to print to PTB. Print the character.

A sequence of instructions (in memory locations 50 - 52) to print a character on the printer from the AC is:

```
50/     700406      /Print character
51/     700401      /Skip when printer free
52/     600051      /Return until printer free
```

The code for the various printer-keyboard characters is given in Table 6.

D. Paper-Tape Punch (Optional)

The Teletype BRPE Punch may be connected to PDP-4. The punch operates at 63.3 lines or characters per second and 5, 7, or 8 hole tape may be punched.

A Punch Buffer (PB) is used, and the operation is similar to the printer. A PB free flag is used to signal when a new character code may be loaded into PB. The commands which control the punch are DS series 02 and are:

700201 Skip if PB free flag is a one. (A new character may be loaded into PB.)

700202 Read the 8-bit code for the character to punch from AC bits 11 - 17 via ID to PB. Punch the character.

700206 Clear PB. Clear PB free flag. Read the code for character to punch to PB. Punch the character.

TABLE 6. TELETYPE CODE

Character	Octal Code	Character	Octal Code
A -	30	Q 1	35
B ?	23	R 4	12
C :	16	S Bell	14
D $	22	T 5	01
E 3	20	U 7	34
F !	26	V ;	17
G &	23	W 2	31
H #	05	X /	27
I 8	14	Y 6	25
J '	32	Z "	21
K (	36	Space	04
L)	11	Carriage Return	02
M .	07	Line Feed	10
N ,	06	Figures	33
O 9	03	Letters	37
P 0	15		

IX. PROGRAM INTERRUPT

The program interrupt is a feature which allows certain conditions to interrupt the program. It is used to speed the processing of input-output devices, or allow certain alarms to halt the computer and a program to retain the pre-alarm state. When a keyboard has been struck, or a character from the tape reader is assembled, the program may be interrupted, and the condition processed. Any one of 14 signals may cuase an interruption of a program. Each of the 14 signals are similar and the polarities are:

-3 volts = interrupt the program

0 volts = no effect

When the interrupt occurs, the contents of the PC are stored in memory location 0. The program resumes in memory location 1. The interrupt program is responsible for finding which of the 14 signals caused the interruption. The program is also responsible for removing the condition which caused the interruption and allows only the interrupt program to run.

When the condition for interruption is removed, a de-interrupt iot signal may be given, followed by the instruction jmp i 0. The interrupted program will resume.

The two program levels are:

a. Interrupted program - the normal program.

b. Interrupt program - the program which runs beginning in location 1. When a second interruption condition occurs and the interrupt program is running, the signal will have no effect. That is, there is only one level of interruption.

The iot interrupt instructions for the DS 00 series are:

700001 Turn off the interrupt mode. The interruption signals will have no effect. When the machine is started, it started with the interrupt mode off.

700002 Turn on the interrupt mode. Interrupt signals are active, and interruption may occur.

700004 Return from the interrupt state. The jmp i 0 instruction will return to the interrupted program, and signals will be free to interrupt.