

CHAPTER 5
ENGINEERING DRAWINGS

5.1 GENERAL

This chapter contains a complete set of engineering drawings pertaining to the basic PDP-9 system. A formal set of engineering drawings is also shipped with each PDP-9 system, including those for all ordered options. Where a discrepancy exists between furnished drawings and those contained in this chapter, it must be assumed that the drawings furnished with the machine are correct.

5.2 USE OF DRAWING CODES

DEC engineering drawing numbers are encoded as to drawing type, major assembly, and series. A drawing number such as BS-KD09-A-11 contains the following information: BS, block schematic type; KD09, the I/O control section of the PDP-9; A, the manufacturing series; 11, the eleventh drawing in the I/O control series, which happens to be the teletype control schematic. The complete glossary of drawing type codes is as follows:

AD	Assembly Drawing	LO	Layout Drawing
AR	Arrangement Drawing	MU	Module Utilization Drawing
BD	Functional Block Diagram	PL	Parts List
CD	Cable Diagram	RS	Replacement Schematic
CP	Component List	SP	Specification Drawing
CS	Circuit Schematic	TD	Timing Diagram
FD	Flow Diagram	UA	Unit Assembly
IC	Interface Cabling Diagram	WD	Wiring Diagram
		WL	Wiring List

5.3 DRAWING CONVENTIONS

Block schematics are multipurpose drawings that combine signal flow, logic functions, circuit type, physical location, and other pertinent information. Individual circuits are shown in block form, using special symbols which define the circuit operation. These symbols are explained in the Logic Handbook C-105.

5.4 SIGNAL MNEMONIC INDEX

All signals originating in the PDP-9 are listed in alphanumeric order below. The Origin column locates the source of each signal to the particular logic drawing, using the abbreviated drawing number system, Volume I, Section 1.7.5.

<u>Signal</u>	<u>Origin</u>	<u>Description</u>
0 → CMA	KC19(1)	Clear the <u>control memory address register</u>
0 → MBI	KC19(2)	Clear the <u>memory buffer input gate</u>
0XEN	KD3(1)	Enable devices 0X
00XXEN	KD3(1)	Enable devices 00XX
+1	KC19(1)	Increment the ADR
1 → ACI	KC19(2)	Set the <u>accumulator register input gate</u>
+1 → CA INH	KD2(2)	Inhibit increment of DCH CA register
1 → MBI	KC19(2)	Set the <u>memory buffer input gate</u>
1 → PCI	KC12	Set the <u>program counter input gate</u>
13 → CMA	KC19(1)	Set CM address to 13
ΔMB	KC19(2)	<u>Change the memory buffer contents</u>
A, B, C	KC10(1)	Program start timing flip-flops
A BUS00-05	KC20(1)	A bus contents
A BUS06-11	KC20(2)	A bus contents
A BUS12-17	KC20(3)	A bus contents
A BUS LINK	KC15	Recirculate LINK status
AC00-05	KC20(1)	Accumulator register contents
AC06-11	KC20(2)	Accumulator register contents
AC12-17	KC20(3)	Accumulator register contents
AC D	CS3	Display the accumulator register contents
ACI	KC19(2)	<u>Accumulator register input gate</u>
ACO	KC19(3)	<u>Accumulator register output gate</u>
AC RD	KD3(3)	Read the accumulator register contents into core memory

<u>Signal</u>	<u>Origin</u>	<u>Description</u>	<u>Signal</u>	<u>Origin</u>	<u>Description</u>
AC RD(B)	KC19(2)	Read the accumulator register contents into core memory.	ARO RESTORE	KC12 KC10(2)	Restore the <u>arithmetic register output gate</u>
AC SIGN	KC15	AC00 status	AROS	KC10(2)	Save the <u>arithmetic register output gate</u>
ADDR SW03-17	CS3	Address switch contents	AUT INX	KC14	Increment the contents of indirectly addressed core memory register 00010-17
ADOF	KC15	<u>Add data</u> overflow, ADD instruction and DCH add-to-memory	AXS	KC19(2)	ADD, XOR, SAD instruction gate
ADR00-05	KC21(1)	Adder register contents	B BUS00-05	KC21(1)	B bus contents
ADR06-11	KC21(2)	Adder register contents	B BUS06-11	KC21(2)	B bus contents
ADR12-17	KC21(3)	Adder register contents	B BUS12-17	KC21(3)	B bus contents
ADR=0 SAVE	KC15	ADRA=0, ADRB=0 status	BK	KD3(2)	Start program break process
ADRA=0	KC21(1) KC21(2)	ADR00-08=0	BK CA	KC10(1)	CA cycle of DCH break (memory extension control)
ADRB=0	KC21(2) KC21(3)	ADR09-17=0	BK0 BK0(0)B BK0(1)B BK1 BK1(0)B BK1(1)B	KD3(3) KC10(1)	Break cycle counter
ADRL ADRL(B)	KC15	Adder link	BK SYNC	KD3(2)	Synchronize program break entry
ADSO ADSO(G)	KC19(2) KD7(1)	<u>Address switches output gate</u>	BS SW3-4	MC2	Core memory bank selection switches
AM GRANT	MC1(2)	Grant core memory access to DMA channel	CAF EN CAF EN(B)	KD3(1)	Clear all flags enable
AM STROBE	MC2	Core memory strobed for DMA channel access	CAL	KC12	CAL instruction gate
AM SYNC AM SYNC(1)B AM SYNC BUS	MC1	Synchronization for DMA cycle	CI17	KC14	Initiate a carry into ADR17
AND	KC19(1)	AND instruction gate	CJIT	KC12 KC19(3)	<u>CAL/JMS/Interrupt Transfer gate</u>
API D	CS3	Display the optional API channel activity	CLK	KC10(1)	Main clock pulse
API IO CLR	KD3(2)		CLK(B)	KD3(2)	
API ON BUS	KD7(1)	Gate optional API activity onto I/O bus (B)	CLK DLY'D	KD3(3)	Main clock pulse delayed 500 ns
API 0,1,2,3 RQ	KD2(2)	Request API channel break	CLK EN	KD3(3)	Enable the real-time clock
AR00-05	KC20(1)	Arithmetic register contents	CLK FLG	KD3(2)	Real-time clock flag
AR06-11	KC20(2)	Arithmetic register contents	CLK POS	KC10(1)	Main clock pulse
AR12-17	KC20(3)	Arithmetic register contents	CLK RQ	KD3(2)	Real-time clock request
AR D	CS3	Display the arithmetic register contents	CLK SYNC	KD3(2)	Synchronize the real-time clock cycle
ARI	KC19(2)	<u>Arithmetic register input gate</u>			
ARO	KC19(3)	<u>Arithmetic register output gate</u>			

<u>Signal</u>	<u>Origin</u>	<u>Description</u>	<u>Signal</u>	<u>Origin</u>	<u>Description</u>
CLL	KC13	Clear the LINK	DCH RQ	KD2(2) KD3(2)	DCH break request
CLR	KC16	Clear the /1, ACO gates, set the SAO, ARO gates	DCH SYNC SAVE	KD3(2)	Save the DCH SYNC status
CLR I	KC19(2)	Clear the MBO, ACI, ARI, PCI, MQI gates	DEI	KC19(1)	Initiate the defer or execute cycle
CLR PUN	KD10(1)	Clear the punch buffer and punch flag	DIGIT READ DRIVE	MC1(2)	Turn on core memory address selectors
CLR RDR	KD9(1)	Clear the RDR FLG, RDR 1, RDR 2 flip-flops	DIGIT READ ON	MC2	Turn on DIGIT READ DRIVE, DIGIT READ SINK
CMA00-05	KC19(1)	<u>Control memory address register contents</u>	DIGIT WRITE DRIVE	MC1(2)	Turn on core memory address selectors
CM CLK	KC10(1)	Main clock pulse to control memory	DIGIT WRITE SINK	MC1(2)	Turn on core memory address selectors
CM CURRENT	KC16	Turn on control memory address selectors	DLY	KD3(3)	Clock pulse delayed 500 ns
CMG00-07	KC17	Control memory current lines	DONE	KC19(1)	Instruction DONE gate
CML	KC13	Complement the LINK	DONE(1)B	KD3(2)	
CMPL	KC13	Complement the ADR contents	DPY D	CS3	Display x,y buffers of optional 34H Display
CMP00-07	KC17	Control memory current lines	DPY ON BUS	KD7(1)	Gate x,y buffers of optional 34H Display onto the IO Bus(B)
CMSL00-35	KC17 KC18(2)	Control memory sense lines	DS00-05 DS00P-05P	KD3(1)	Device select bits
CM STROBE A,B,C,D	KC16	Strobe the control memory	EAE	KC19(1)	Optional <u>extended arithmetic element</u> gate
CM STROBE DLYD	KC16		EAE D	CS3	Not wired
CONT	KC19(1)	<u>Continue</u> gate	EAE-P EAE-R	KC19(1)	Optional <u>extended arithmetic element</u> gate
CO00-05	KC21(1)	Carry out of ADR00-05	EAE STROBE DLYD	KC16	CM STROBE delayed for optional extended arithmetic element
CO06-11	KC21(2)	Carry out of ADR06-11	END BIT 0	KC15	LINK to ADRL to AC17. Also for optional extended arithmetic element gating
CO12-17	KC21(3)	Carry out of ADR12-17	END BIT 17	KC15	Optional extended arithmetic element gating
DASO	KC13	<u>Data switches output</u> gate	EXT EXT(1)B	KC19(3) KD3(3)	<u>External</u> transfer gate (program breaks)
DATA OFLO	KC15	DCH add-to-memory data overflow	FEED HOLE	KD9(2)	Reader no-tape sensor
DATA SW00-17	CS3	Data switch contents	FWD FD and NDX	KD10(1)	Punched tape drive power
DB RESTORE	KD3(1)		GO DLY	KD9(1)	Reader enable delay
DBR	KD3(1)	<u>Debreak and restore</u> the interrupted program	IND CLK	KC10(1)	Gate CP register contents for display
DBR(B)	KC15		IN CLR	KC16	Generate CLR I
DCH	KC19(1)		INC V DCH	KD3(2)	Enter DCH or RTC WC cycle
DCH BK DLY	KD3(1)	Illuminate the DCH display indicator			
DCH EN	KD3(1)	Enable the DCH Multiplexer W104			
DCH GRANT DCH GRANT P	KD3(1)	Grant core memory access to the DCH			
DCH INX	KD3(3)	Increment the DCH WC or CA register			

<u>Signal</u>	<u>Origin</u>	<u>Description</u>	<u>Signal</u>	<u>Origin</u>	<u>Description</u>
IND EN	KC10(1)	Enable console display selector switch	IOP4	KD3(1) KD3(3)	Input/output pulse 4
INC MB	KD2(2) KD3(3)	Increment the memory buffer contents	IOP1P	KD3(3)	Input/output pulse 1
IN LAST UNIT	KD11(1)	Last keyboard code unit shifted into input buffer	IOP2P	KD3(3)	Input/output pulse 2
INPUT IO RESTART	KD8 KD3(3)	Restart control memory after manual read-in, EAE, or IOT instruction	IOP4P	KD3(3)	Input/output pulse 4
INT RD RQ BUS	KD3(3)	Internal read request bus	IO PWR CLR	KD3(1)	I/O power clear pulse
INT SKP RQ BUS	KD3(1) KD9(1) KD10(1) KD11(1) KD11(2)	Internal skip request bus	IO PWR CLR POS	KD3(1)	
IO0	KD3(3)	Input/output transfer cycle counter	IO RESTART	KD3(3)	Restart control memory after manual read-in, EAE, or IOT instruction execution.
IO1			IO RUN(1)	KD3(1)	Computer RUN condition to I/O devices
IO ADDR 03-17	KD2(2)	DCH and optional API channel address	IO SKIP	KD3(3)	Skip next instruction on SKIP RQ from I/O device
IO ADDR 03(B)-17(B)	KD5		IO SYNC	KD3(1)	Synchronize program break entry
IO ADDR 12,16,17	KD5	Optional API channel address	IO SYNC IN	KD3(2)	Synchronize program break entry
IO ADDR D	CS3	Display DCH or optional API address	IO SYNC POS	KD3(2)	Synchronize program break entry
IO ADDR ON BUS	KD7(1)	Gate DCH or optional API address onto I/O bus (B)	IO SYNC SP	KD3(1)	Synchronize optional API break entry
IO BUS00-05	KC21(1)	I/O bus contents	IOT	KC12	<u>Input/output transfer gate</u>
IO BUS06-11	KC21(2)		IOT0002	KD3(1)	IOT command
IO BUS12-17	KC21(3)		IOT0004	KD3(1)	
IO BUS00-17	KD2(1)		IOT0102	KD9(1)	
IO BUS00(B)-08(B)	KD7(1)	I/O bus buffered	IOT0104	KD9(1)	
IO BUS09(B)-17(B)	KD7(2)		IOT0204	KD10(1)	
IO BUS ON	KC19(3)	ADR to I/O bus gate	IOT0302	KD11(1)	
IO CLK(B)	KD3(3)	Main clock pulse	IOT0404	KD11(2)	
IO CLK POS	KD3(2)	Main clock pulse	IOT3344	KD3(1)	
IO CLR	KD3(2)	Clear PROG SY, PROG SYNC, BK	IOT(B)	KD3(1)	<u>Input/output transfer gate</u>
IO OFLO	KD3(2)	DCH or RTC operations completed	IOT OR ARO	KC12	Set ARO gate for programmed output transfer
IOP1	KD3(1) KD3(3)	Input/output pulse 1	IOT PWR CLR	KD3(1)	
IOP2	KD3(1) KD3(3)	Input/output pulse 2	IR00-04	KC12	Instruction register contents
			IRI	KC19(1)	<u>Instruction register input gate</u>
			ISZ	KC12	ISZ instruction gate
			KBD FLG	KD11(1)	Keyboard flag
			KBD SEL	KD11(1)	Keyboard select
			KBD SEL(B)		

<u>Signal</u>	<u>Origin</u>	<u>Description</u>	<u>Signal</u>	<u>Origin</u>	<u>Description</u>
KCT	CS3	CONTINUE key	MA06(0) \wedge MA07(0)	MC1(1)	Memory address register bits decoded for address selection
KCT(B)	KC10(1)		MA06(0) \wedge MA07(1)		
KDN	CS3	DEPOSIT NEXT key	MA06(1) \wedge MA07(0)		
KDP	CS3	DEPOSIT key	MA06(1) \wedge MA07(1)		
KDPDN	KC10(1)	DEPOSIT/DEPOSIT NEXT key	MA10(0) \wedge MA11(0)		
KDPDN V RI	KC19(3)	DEPOSIT/DEPOSIT NEXT key or READ-IN key	MA10(0) \wedge MA11(1)		
KDPM	CS5	DEPOSIT key (maintenance)	MA10(1) \wedge MA11(0)		
KEY	KC19(2)	Key gate	MA10(1) \wedge MA11(1)		
KEY BUS	KC10(1)	Key bus	WR(1) \wedge MA05(1)		
KEY BUS(B)			WR(1) \wedge MA05(0)		
KEY DLY	KC10(1)	Delay key-activated RUN condition	WR(1) \wedge MA05(1)		
KEY INIT POS	KC10(1)	Initiate key operations	MA JAM DIGIT	MC1(1)	Strobe address into memory address register
KEY \wedge KDPDN	KC13		MA JAM PAR		
KEN	CS3	EXAMINE NEXT key	MA JAM WORD		
KEYS	CS5		MAS03-04	MC2	Memory address bits decoded for expanded memory
KEX	CS3	EXAMINE key	MB00-05	KC21(1)	Memory buffer register contents
KIO	CS3	I/O RESET key	MB06-11	KC21(2)	
KIOA3, A4, A5	KC10(1)	Key process address to control memory	MB12-17	KC21(3)	
KMT	CS5	Key (maintenance)	MBI	KC19(2)	<u>Memory buffer input gate</u>
KRI	CS3	READ-IN mode key	MBI(1)B	KC28	
KSP	CS3	STOP key	MBO	KC19(3)	<u>Memory buffer output gate</u>
KST	CS3	START key	MBS00-17	MC3	Core memory input mixer bits
KXDM	CS5	EXAMINE/DEPOSIT key (maintenance)	MEM DONE	MC1(2)	Core memory cycle done
LAR	KC15	Arithmetic register link	MEM DONE(1)B		
LI	KC19(1)	<u>LINK input gate</u>	MEM STROBE	MC2	Core memory strobed for CP access
LINK	KC15	Accumulator register link	MEM STROBE(B)	KC28	
LIO	KC13	Load I/O data onto I/O bus	MK	CS5	
LOCK	CS5	Lock the console controls	MODE	MC1(2)	Core memory access mode
LOT	KC12	LAW/OPR/IOT instruction gate	MQ00-05	KC20(1)	Optional multiplier/quotient register contents
MA05-13	MC1(1)	Memory address register contents	MQ06-11	KC20(2)	
MA14A-17A			MQ12-17	KC20(3)	
MA14B-17B			MQ D	CS3	Display the optional multiplier/quotient register contents
			MQI	KC19(2)	Optional <u>multiplier/quotient</u> input gate
			MQO	KC19(3)	Optional <u>multiplier/quotient</u> output gate
			NDX	KD10(1)	Punch the tape feed holes

<u>Signal</u>	<u>Origin</u>	<u>Description</u>	<u>Signal</u>	<u>Origin</u>	<u>Description</u>
NOSH	KC13	NO SHIFT gate	PROG SY	KD3(2)	Synchronize program interrupt entry
O BUS00-05	KC20(1)	O bus contents	PROG SY(1)B		
O BUS06-11	KC20(2)		PROG SYNC		
O BUS12-17	KC20(3)		PROG SYNC(1)B		
O BUS00-17	KC22				
O BUS L	KC15	LINK status to optional EAE	PUN	KD10(1)	Punch mechanism operating
OFLO	KC14	DCH,RTC word count overflow	PUN ACT	KD10(1)	Actuate punch mechanism
OFLO	KC15	ADD instruction overflow	PUN FEED	KD10(2)	Punch feed holes manually
OP	KC12	OPR instruction gate	PUN FLG	KD10(1)	Punch flag
OR ACI	KC12	Set the ACI gate for programmed input transfer	PUN HOLE 1-8	KD10(1)	Punch buffer bits to punch solenoids
OR MBO	KC12	Set the MBO gate for LAW instruction	PUN LINE	KD10(1)	Enable punch solenoid drivers
PB10-17	KD10(1)	Punch buffer contents	PUN NO TAPE	KD10(1)	Punch out of tape
PC05	KC20(1)	Program counter contents	PUN PWR	KD10(1)	Punch power
PC06-17	KC20(2)		PUN PWR ON	KD10(1)	Punch power on
PC012-17	KC20(3)		PUN SEL	KD10(1)	Punch select
PC D	CS3	Display the program counter contents	PUN SPD	KD10(1)	Punch motor up to speed
PCI	KC19(2)	<u>Program counter input gate</u>	PUN SYNC	KD10(2)	Punch motor in punching position
PCO	KC19(3)	<u>Program counter output gate</u>	PV	KC12	Memory <u>protection violation</u>
PCO RESTORE	KC10(2)	Restore the PCO gate	PWR(B)	KD9(1)	Reader power on
PCOS	KC10(2)	Save the PCO gate	PWR CLR POS	KC10(1)	Power clear pulse
PIE	KD3(2)	Program interrupt enable	RB00-17	KD9(2)	Reader buffer contents
PIE(0)	KD3(2)	Program interrupt disable	RD HOLE 1(B)-7(B)	KD9(2)	Punched tape contents
PK CLR	KC10(1)	Power and key clear pulse	RD HOLE 7(C)	KD9(2)	Punched hole 7
PK CLR(B)	MC2		RD HOLE 8(B)	KD9(2)	Punched hole 8
POST CLK	MC2	Main clock delayed/strobe the MODE flip-flop	RD HOLE 8P V ALPHA	KD9(2)	Reader binary or alpha mode
PRE-STROBE	MC2	Generate MEM STROBE, STROBE SAL, STROBE SAR	RD IO BUS	KD7(1)	
PRE-WRITE OFF	MC2	Set MEM DONE, issue AM GRANT	RDR 1	KD9(1)	Read first line of tape into reader buffer
PROG INT RQ	KD2(1)	Program interrupt request	RDR 2	KD9(1)	Read second line of tape into reader buffer
	KD3(2)		RDR A	KD9(1)	Reader line index count
	KD9(2)		RDR A(0)B	KD9(2)	
	KD10(1)		RDR A(1)B	KD9(2)	
	KD11(1)		RDR ALPHA	KD9(1)	Reader alpha mode
	KD11(2)				

<u>Signal</u>	<u>Origin</u>	<u>Description</u>	<u>Signal</u>	<u>Origin</u>	<u>Description</u>
RDR B	KD9(1)	Reader line index count	SD00-01	KD3(1)	Special device select bits
RDR B(0)B	KD9(2)		SD00P-01P		
RDR B(1)B	KD9(2)		SEN	KC10(2)	Computer RUN sensor
RDR CLK	KD9(1)	Reader clock pulse	SEN(1)B	KC10(1)	
RDR CLK EN	KD9(1)	Reader clock enable	SHIFT	KC15	Shift ADR contents enable
RDR COUNT	KD9(1)	Reader line index count	SHL1	KC13	Shift ADR contents left one position
RDR D	CS3	Display the reader buffer contents	SHL2	KC13	Shift ADR contents left two positions
RDR FEED	KD9(2)	Feed tape manually without reading	SHR1	KC13	Shift ADR contents right one position
RDR FLG	KD9(1)	Reader flag	SHR2	KC13	Shift ADR contents right two positions
RDR FLG(B)	KD8		SKIP	KC14	<u>Skip next instruction gate</u>
RDR GO	KD9(1)	Enable reader clock	SKIP RQ	KD2(1)	Skip request from I/O device
RDR INDEX	KD9(1)	Reader clock pulses	SKPI	KC19(1)	<u>Skip input gate</u>
RDR NO TAPE	KD9(1)	Reader out of tape	SM	KC19(2)	<u>Start memory gate</u>
RDR ON BUS	KD7(1)	Gate reader buffer contents onto I/O bus (B)	SPEED 2,3,4	CS3	Repeat speed selections
RDR PWR	KD9(1)	Reader power	SPEED WIPER	CS3	Repeat speed switch wiper
RDR RUN	KD9(1)	Generate RUN	STATUS D	CS3	Display the I/O device status bits
RDR SEL	KD9(1)	Reader select	STATUS ON BUS	KD7(1)	Gate the I/O device status bits onto I/O bus (B)
RDR SEL(B)			STOP DLY	KD9(1)	Decelerate the reader motor
RD RQ	KD2(1)	Read request from I/O device	STOP DLY	KD9(1)	Permit reader motor to restart
RD RQ(B)	KD3(3)		STOP DLY POS	KD9(1)	Disable reader clock
RD START RQ	KC10(1)	Read manually entered tape word into core memory	STROBE DLYD	KC16	Control memory strobe delayed
RD STATUS	KD11(1)	Read teletype status	STROBE SAL	MC2	Strobe the left hand sense amplifiers
R12(1)B	KD8	Manually entered tape word count	STROBE SAR	MC2	Strobe the right hand sense amplifiers
RQ MBI	KC19(2)	Turn on <u>memory buffer input gate</u>	SW EXD	CS3	Optional memory extend mode switch
RSB	KD8	Select reader binary mode	SW SGL INST	CS3	Single instruction switch
RUN	KD9(1)	Set RDR GO	SW PARITY	CS3	Optional memory parity switch
RUN	KC10(1)	Computer program started	SW PRTCT	CS3	Optional memory protect switch
RUN(1)B			SW REPT	CS3	Repeat switch
RUN(0)	KC10(1)	Computer program stop	SUB	KC19(1)	<u>Subtract gate</u>
SA00-17	MC6	Sense amplifier contents	SYNC CLK	MC2	Set AM SYNC if AM RQ is present
SAO	KC19(3)	<u>Sense amplifier output gate</u>			
SAO(0)B	KC15				

<u>Signal</u>	<u>Origin</u>	<u>Description</u>
<u>TAPE</u>	KD10(2)	Punch out of tape
TI	KC19(1)	<u>Test for indirect address gate</u>
T-PRNTR FLG	KD11(2)	Teleprinter flag
T-PRNTR SEL	KD11(2)	Select teleprinter
T-PRNTR SEL(B)		
TTI00-07	KD11(1)	Teletype input buffer contents
TTI CLK	KD11(1)	Teletype input clock
TTI D	CS3	Display the teletype input buffer contents
TTI FULL	KD11(1)	Teletype input buffer is full
TTI INITIALIZE	KD11(1)	Initialize teletype input buffer and controls
TTI LOAD	KD11(1)	Load the teletype input buffer
TT IN ACT	KD11(1)	Teletype input circuits active
TTI ON BUS	KD7(1)	Gate teletype input buffer contents onto I/O bus (B)
TT KBD IN	KD11(1)	Teletype keyboard input
TT KBD IN(B)		
TT LINE	KD11(2)	Actuate teleprinter to generate space or mark
TTO00-07	KD11(2)	Teletype output buffer contents
TTO CLK	KD11(2)	Teletype output clock
TTO EN	KD11(2)	Teletype output enable
TTO EQ	KD11(2)	All teletype output buffer bits serially shifted into teleprinter
TTO LOAD	KD11(2)	Load the teletype output buffer
TTO OUT ACT	KD11(2)	Teletype output circuits active
TT RDR RUN	KD11(1)	Release teleprinter magnet to generate marks and spaces
TTO START	KD11(2)	Start teletype output operations
TTO STOP	KD11(2)	Stop teletype output operations
UM(0)B	KD3(3)	<u>User Mode disabled (Memory Protect Option)</u>
UM(1)B		<u>User Mode enabled (Memory Protect Option)</u>
WORD READ	MC1(2)	Turn on core memory address selectors
WORD READ ON	MC2	Turn on WORD READ
WORD WRITE	MC1(2)	Turn on core memory address selectors

<u>Signal</u>	<u>Origin</u>	<u>Description</u>
WRITES OFF	MC2	Turn off core memory address selectors
WRITES ON	MC2	Turn on DIGIT WRITE DRIVE, DIGIT WRITE SINK
WR RQ	KD2(2) DK3(3)	Write request from I/O device
<u>WR RQ(B)</u>	KD3(2)	

5.5 ENGINEERING DRAWING LIST

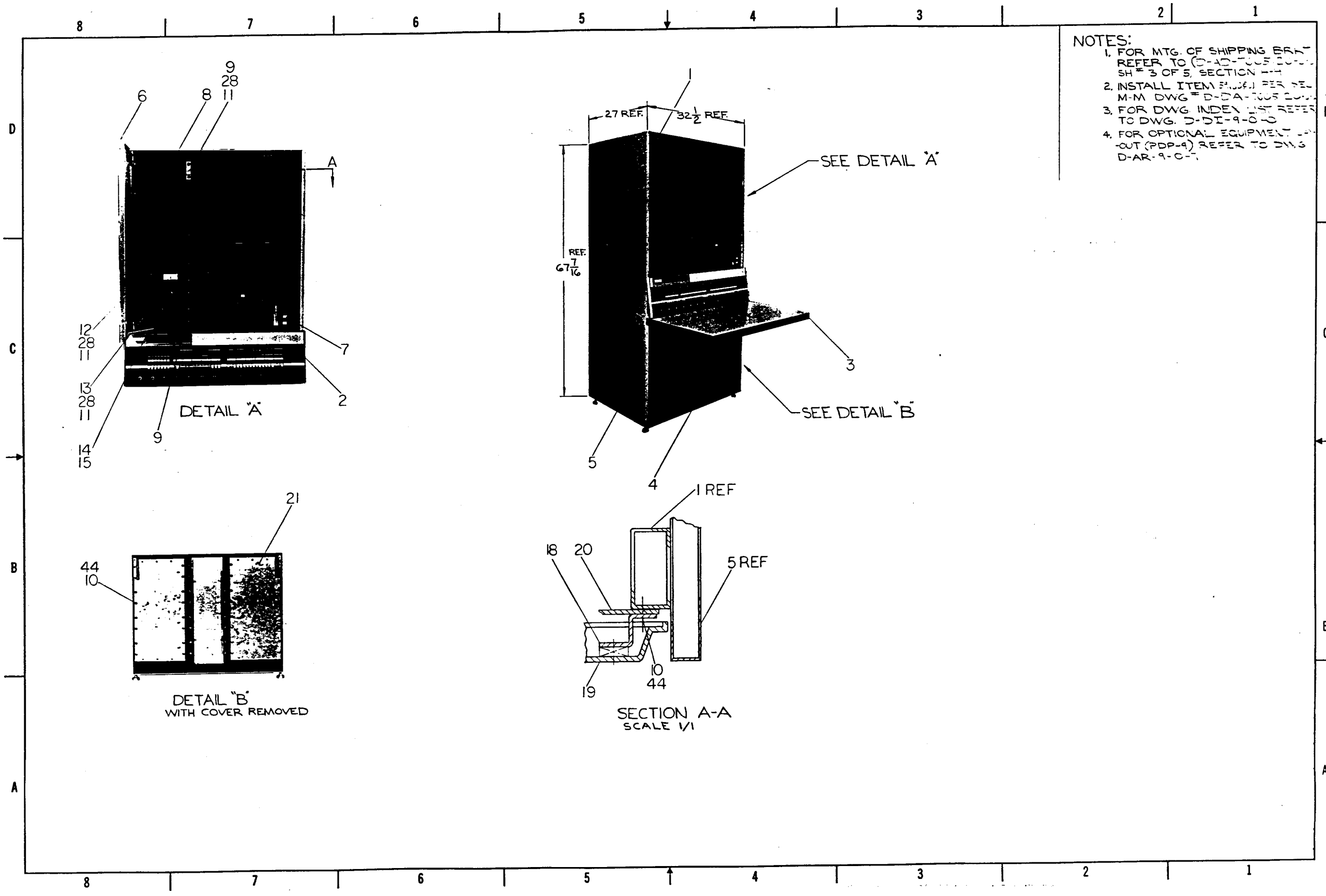
A list of the full complement of engineering drawings contained in this chapter follows.

<u>Drawing Number</u>	<u>Title</u>	<u>Revision</u>	<u>Page</u>
<u>System Drawings</u>			
D-UA-9-0-0	PDP-9 Assembly (sheet 1)	E	12
D-UA-9-0-0	PDP-9 Assembly (sheet 2)	E	13
D-UA-9-0-0	PDP-9 Assembly (sheet 3)	E	14
A-PL-9-0-0	PDP-9 Assembly Parts List (sheet 1)	E	15
A-PL-9-0-0	PDP-9 Assembly Parts List (sheet 2)	E	15
A-PL-9-0-0	PDP-9 Assembly Parts List (sheet 3)	E	16
A-PL-9-0-0	PDP-9 Assembly Parts List (sheet 4)	E	16
A-PL-9-0-0	PDP-9 Assembly Parts List (sheet 5)	E	17
D-IC-9-0-1	Power Wiring	--	18
D-CD-9-0-2	Cable Diagram	E	19
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D-CS-9-0-4	Console Indicators	A	21
D-CS-9-0-5	Maintenance Area Wiring	--	22
C-CS-709-0-1	709 Power Supply	B	23
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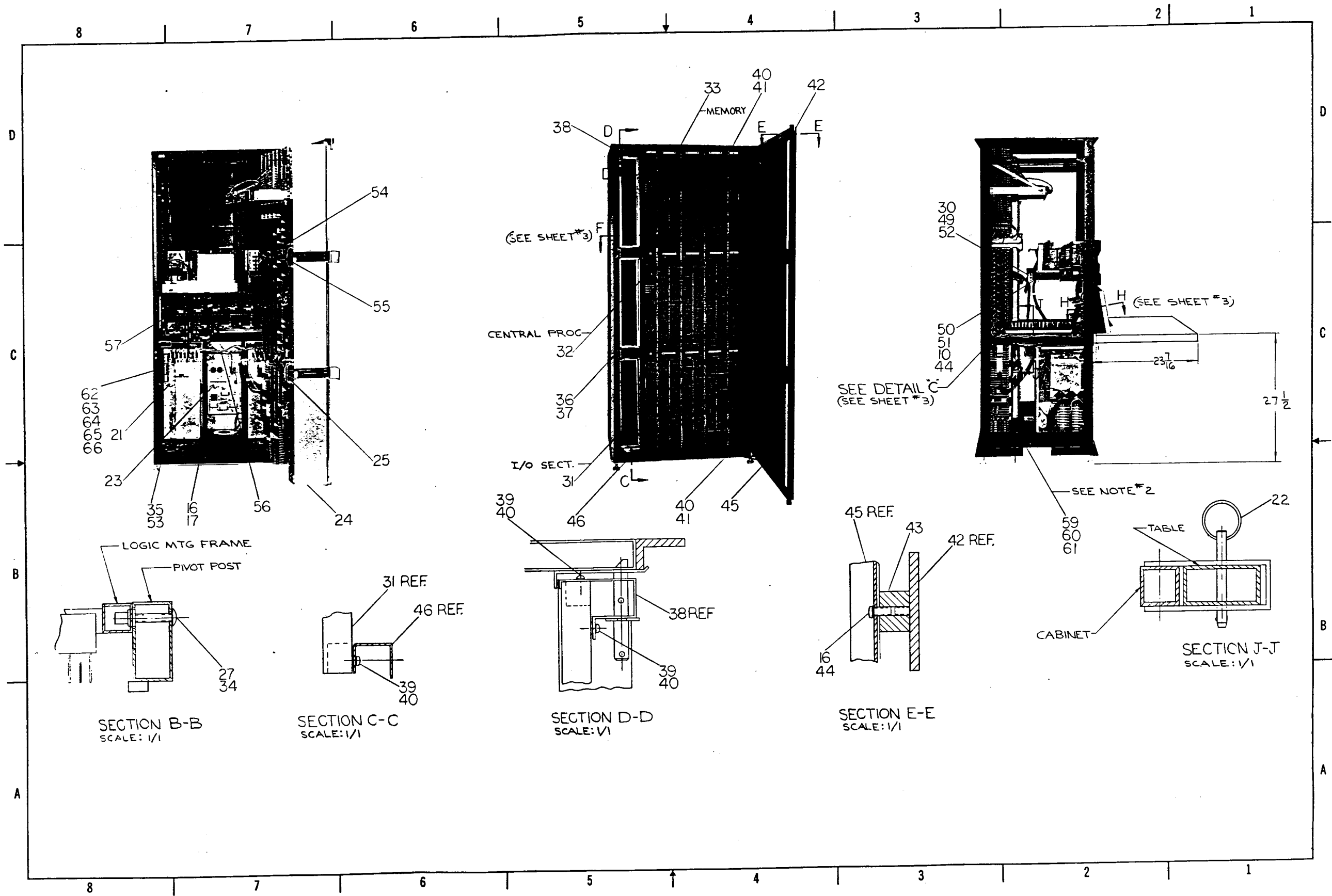
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A-PL-KC09-A-0	Assembly Parts List	B	28	D-BS-KC09-A-20	AC, AR, MQ, PC (sheet 2)	C	55
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D-FD-KC09-A-4	Execution Flow (sheet 2)	C	33	D-BS-KC09-A-22	Shift X2 Gates	B	60
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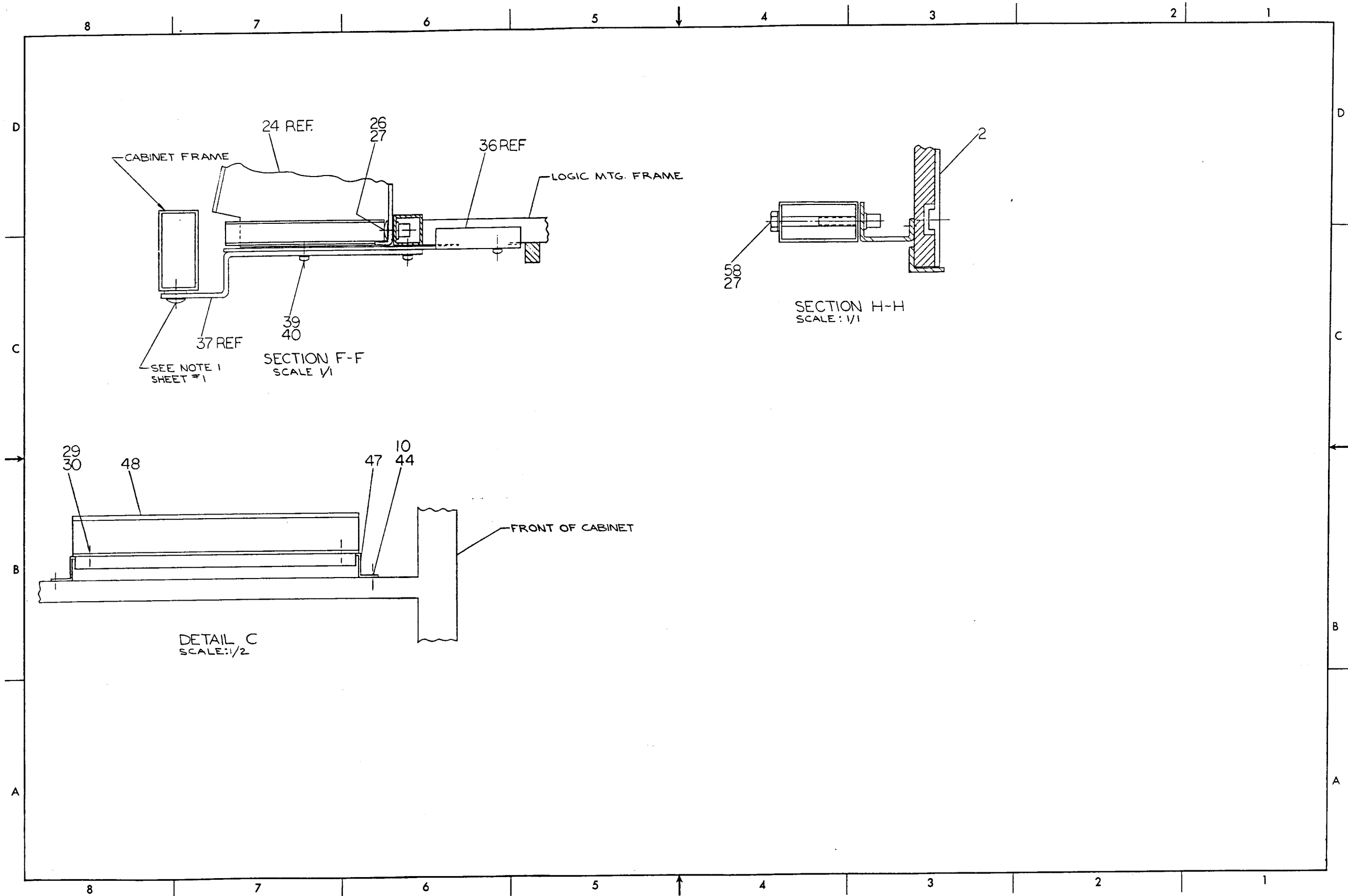
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D-IC-KD09-A-12	I/O Checkout Cables (sheet 1)	C	130	A-WL-PC01-0-1	Reader Block Wiring List (sheet 2)β	--	141
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D-TD-KD09-A-20	Reader Timing	--	137	A-PL-PC09-0-0	Reader and Punch Unit Parts List (sheet 1)	--	149
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D-TD-KD09-A-22	Teletype Timing (sheet 2)	A	140	B-MU-7005120-0-1	Reader Module Utilization List	--	151
				B-AD-7005160-0-0	Reader Bus Bar	--	151



- NOTES:**
1. FOR MTG. OF SHIPPING BRKT REFER TO (D-AD-705 2000) SH # 3 OF 5, SECTION 1-1
 2. INSTALL ITEM #1000 PER REL. M-M DWG # D-DA-705 2000
 3. FOR DWG. INDEX LIST REFER TO DWG. D-DI-9-0-0
 4. FOR OPTIONAL EQUIPMENT LAYOUT (PDP-9) REFER TO DWG. D-AR-9-0-7



D-UA-9-0-0 PDP-9 Assembly (Sheet 2)



D-UA-9-0-0 PDP-9 Assembly (Sheet 3)

PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION		DEC. STOCK NO.
			ITEM	STOCK SIZE — CAT. NO. — MFG.	
1	A-PL-7005243-0-0	1		CABINET FRAME ASSY (PDP-9)	7005243
2	A-PL-7005235-0-0	1		CONSOLE ASSY	7005235
3	A-PL-7005090-0-0	1		TABLE	7005090
4	A-PL-7405181-0-0	1		DETACHABLE COVER	7405181
5	E-IA-7405092-0-0	2		END PANEL	7405092
6	A-PL-7005250-0-0	1		DOOR ASSY	7005250
7	A-PL-PC09-0-0	1		READER, PUNCH (PC09)	
8	C-MD-7405722-0-0	4		PANEL, BLANK	7405722
9	B-MD-7405437-0-0	2		STRIKER PLATE	7405437
10		40		SCR PHL HD TRUSS #10-32 x 3/4 SST	
11		24		WASH. 3/8 O.D. x 1/4 I.D. x .020 THK NYLON	
12	A-PL-7005280-0-0	1		MARGINAL CHECK ASSY	7005280
13	A-PL-7005256-0-0	1		MAINT. PANEL ASSY	7005256
14	B-MD-7405500-0-0	1		DOOR STOP ROD	7405500
15		1		RATCHET PLATE HS-47285 CARR FASTN.	
16		8		SCR. PHL HD TRUSS #10-32 x 1/2 SST	

A-PL-9-0-0 PDP-9 Assembly Parts List (Sheet 1)

PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION		DEC. STOCK NO.
			ITEM	STOCK SIZE — CAT. NO. — MFG.	
17		4		NUT "KEPS" #10-32 SST	
18	C-IA-7405570-1-0	8		COVER RETAINER	7405570-1-0
19	D-SC-3405331-0-0	4		COVER	3405331
20	B-MD-5100	4		STD PANEL "C" SIZE	7402016
21	A-PL-709-0-0	2		709 POWER SUPPLY	
22		2		FASPIN #34-D-4-14R LEHIGH METALS	
23	A-PL-841-A-0	1		841-A POWER CONTROL	
24	A-PL-7005229-0-0	3		FAN & MARGINAL CHK ASSY	7005229
25	A-PL-7005499-0-0	1		JUMPER SET	7005499
26		9		SCR PHL HD TRUSS 1/4-20 x 5/8 SST	
27		22		WASH. EXT TOOTH 1/4-20 SST	
28		24		SCR PHL HD TRUSS #10-32 x 3/4 (BLK PASSIVATE)	
29		2		SCR PHL HD PAN #8-32 x 1/2 SST	
30		6		NUT KEPS #8-32 SST	
31	A-PL-KD09-A-0	1		I/O ASSEMBLY (KD09-A)	
32	A-PL-KC09-A-0	1		C/P ASSEMBLY(KC09-A)	

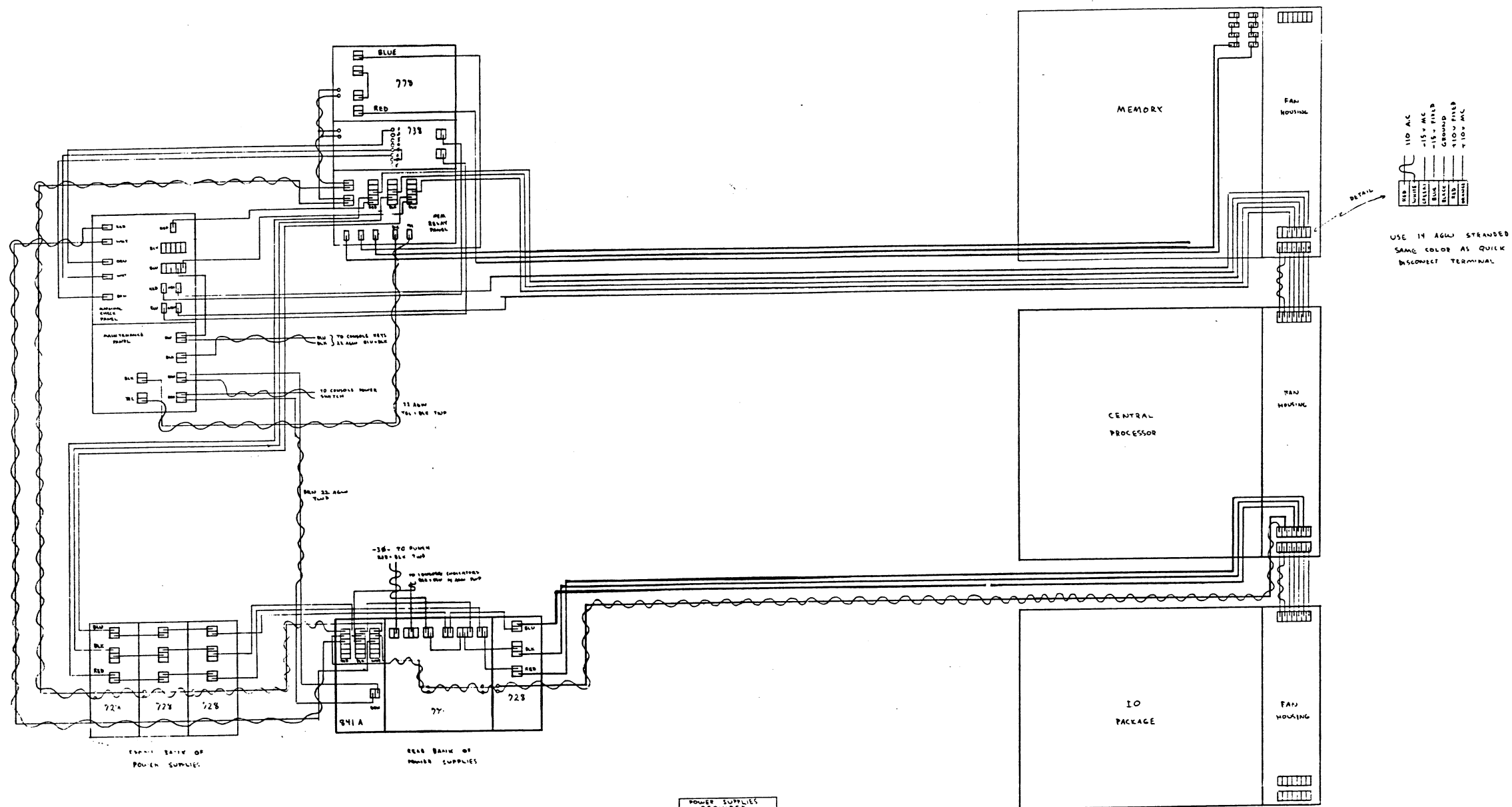
A-PL-9-0-0 PDP-9 Assembly Parts List (Sheet 2)

PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION		DEC. STOCK NO.
			ITEM	STOCK SIZE — CAT. NO. — MFG.	
33	A-PL-MC70-B-0	1		MEMORY UNIT MC70-B	
34		9		SCR PHL HD TRUSS 1/4-20 x 1-1/2 SST	
35	B-MD-7405521-0-0	1		DOOR SUPPORT (SHIPPING)	7405521
36	B-MD-7405093-0-0	2		INTERMEDIATE SUPPORT	7405093
37	C-MD-7405291-0-0	2		SHIPPING BRKT	7405291
38	A-PL-7005439-0-0	1		LATCH BRACKET	7005439
39		14		SCR PHL PAN HD #6-32 x 5/8 SST	
40		18		WASH INT TOOTH #6	
41		4		SCR PHL PAN HD #6-32 x 1/4 SST	
42	D-MD-7405278-2-0	1		VENT STRIP (RED)	7405278-2-0
43	A-MD-7405321-0-0	4		SPACER, VENT STRIP	7405321
44		44		WASH EXT TOOTH #10	
45	A-PL-7005171-0-0	1		REAR DOOR ASSY	7005171
46	C-MD-7405315-0-0	1		MAGNET CATCH	7405315
47	D-MD-7405327-0-0	1		CABLE HOLD DOWN BRACKET	7405327
48	C-MD-7405633-0-0	1		CABLE DUCT #1	7405633

A-PL-9-0-0 PDP-9 Assembly Parts List (Sheet 3)

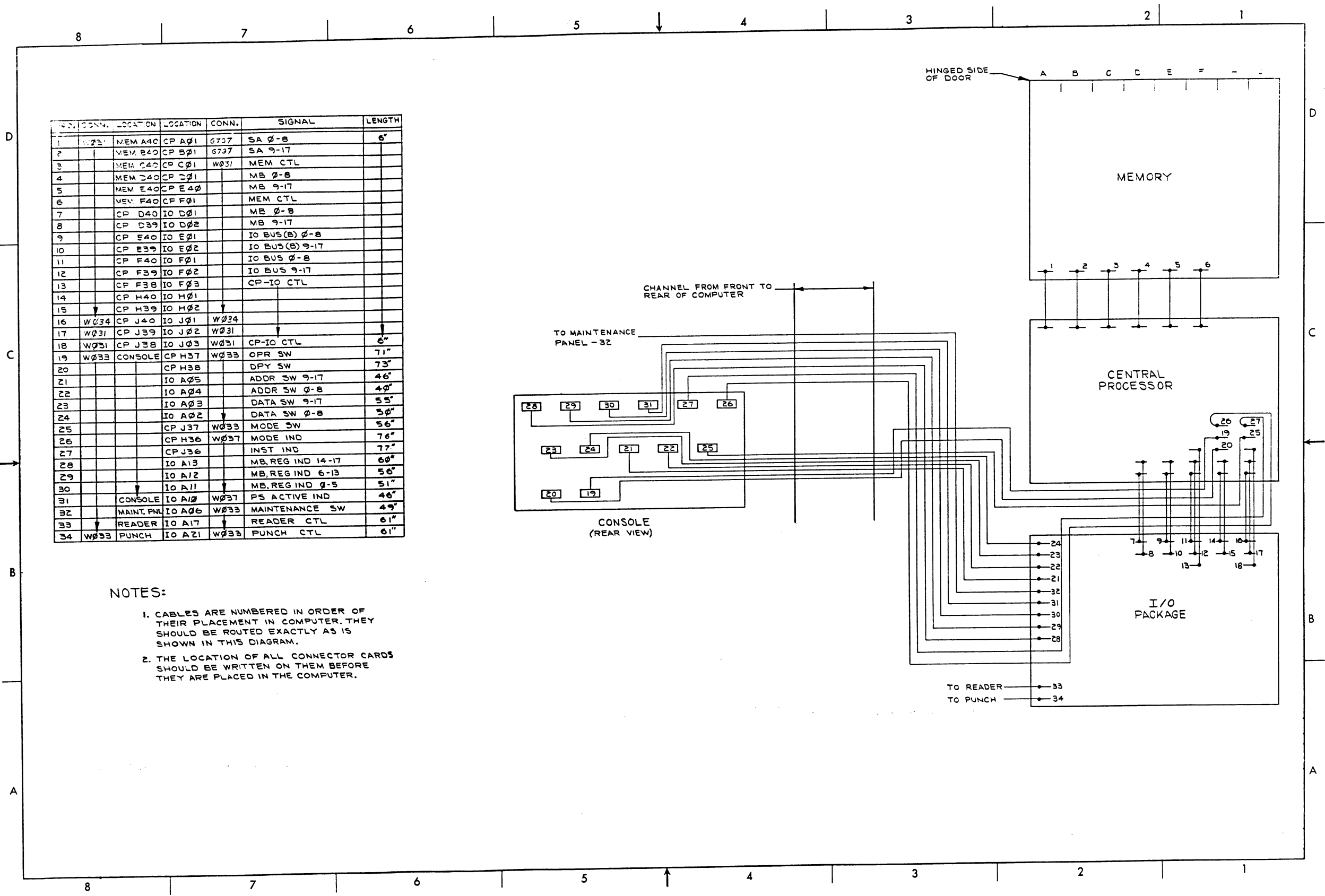
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION		DEC. STOCK NO.
			ITEM	STOCK SIZE — CAT. NO. — MFG.	
49	D-SC-3404701-3-0	1		SLIDE BRACE	3404701-3-0
50	D-SC-3404701-1-0	1		CHASSIS TRACK (LEFT)	3404701-1-0
51	D-SC-3404701-2-0	1		CHASSIS TRACK (RIGHT)	3404701-2-0
52		4		SCR PHL HD PAN #8-32 x 3/8 SST	
53		2		SCR FLAT HD M.S. #6-32 x 1" SST	
54	D-IA-7005417-0-0	2		CABLE W021-W028 SHUNT RES	7005417
55	D-IA-7005418-0-0	2		CABLE W021-W028 SERIES RES	7005418
56	J-IA-7005376-0-0	1		POWER CABLE PDP-9	7005376
57	C-AD-7005372-0-0	1		CABLE SET	7005372
58		4		SCR PHL HD TRUSS 1/4-20 x 2-1/2 SST	
59		2		BOLT SO HD 3/8-16 x 8" LG	
60		2		WASH FLAT 7/8 O.D. x 13/32 I.D. x 5/64 THK	
61		2		NUT, HEX 3/8-16	
62	C-MD-7406466-0-0	1		MARG CHECK ADAPTER	
63	B-IA-7005486-0-0	1		SHORTING PLUG	
64		1		SOCKET S-306-FP CINCH JONES	1203519

A-PL-9-0-0 PDP-9 Assembly Parts List (Sheet 4)



POWER SUPPLIES REQUIRED	
TYPE	NO.
728	4
738	1
778	1
779	1
841 A	1

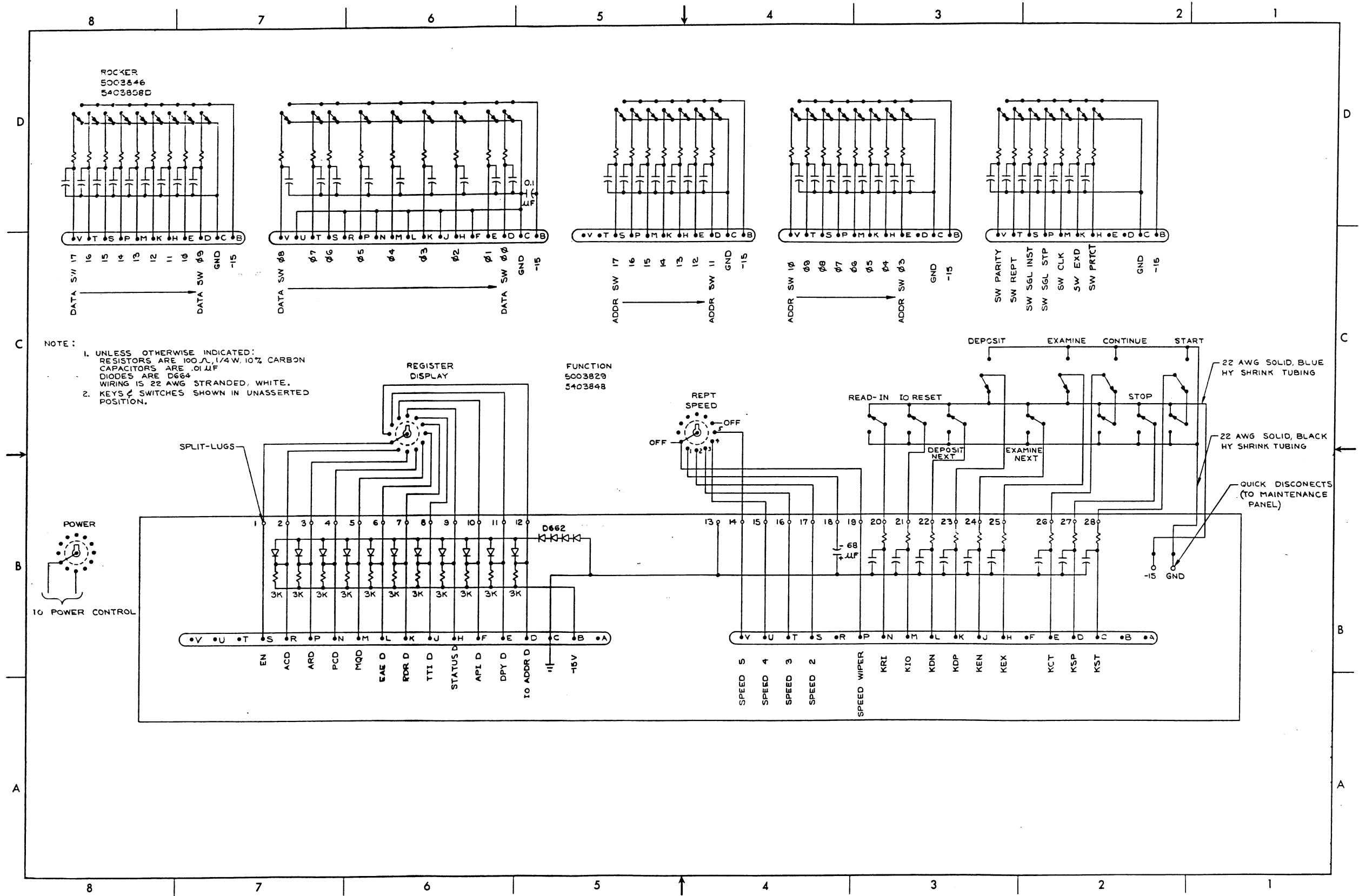
D-IC-9-0-1 Power Wiring



NO.	CONN.	LOCATION	LOCATION	CONN.	SIGNAL	LENGTH
1	W031	MEM A40	CP A01	G737	SA 0-8	6"
2		MEM B40	CP B01	G737	SA 9-17	
3		MEM C40	CP C01	W031	MEM CTL	
4		MEM D40	CP D01		MB 0-8	
5		MEM E40	CP E40		MB 9-17	
6		MEM F40	CP F01		MEM CTL	
7		CP D40	IO D01		MB 0-8	
8		CP D39	IO D02		MB 9-17	
9		CP E40	IO E01		IO BUS(B) 0-8	
10		CP E39	IO E02		IO BUS(B) 9-17	
11		CP F40	IO F01		IO BUS 0-8	
12		CP F39	IO F02		IO BUS 9-17	
13		CP F38	IO F03		CP-IO CTL	
14		CP H40	IO H01			
15		CP H39	IO H02			
16	W034	CP J40	IO J01	W034		
17	W031	CP J39	IO J02	W031		
18	W031	CP J38	IO J03	W031	CP-IO CTL	6"
19	W033	CONSOLE	CP H37	W033	OPR SW	71"
20			CP H38		DPY SW	73"
21			IO A05		ADDR SW 9-17	46"
22			IO A04		ADDR SW 0-8	40"
23			IO A03		DATA SW 9-17	55"
24			IO A02		DATA SW 0-8	50"
25			CP J37	W033	MODE SW	56"
26			CP H36	W037	MODE IND	76"
27			CP J36		INST IND	77"
28			IO A13		MB, REG IND 14-17	60"
29			IO A12		MB, REG IND 6-13	50"
30			IO A11		MB, REG IND 0-5	51"
31		CONSOLE	IO A10	W037	PS ACTIVE IND	46"
32		MAINT. PNL	IO A06	W033	MAINTENANCE SW	49"
33		READER	IO A17		READER CTL	61"
34	W033	PUNCH	IO A21	W033	PUNCH CTL	61"

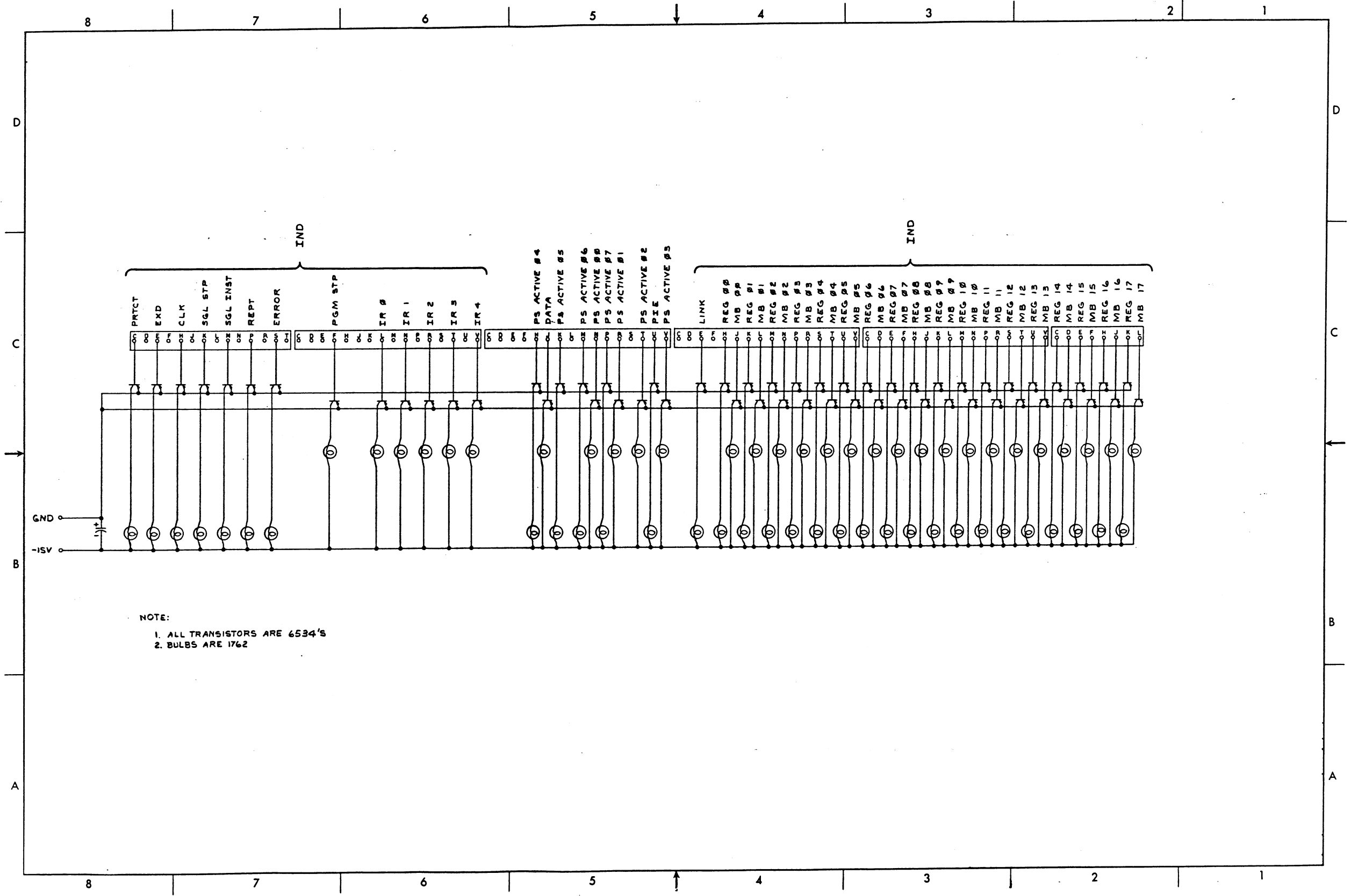
- NOTES:
1. CABLES ARE NUMBERED IN ORDER OF THEIR PLACEMENT IN COMPUTER. THEY SHOULD BE ROUTED EXACTLY AS IS SHOWN IN THIS DIAGRAM.
 2. THE LOCATION OF ALL CONNECTOR CARDS SHOULD BE WRITTEN ON THEM BEFORE THEY ARE PLACED IN THE COMPUTER.

D-CD-9-0-2 Cable Diagram



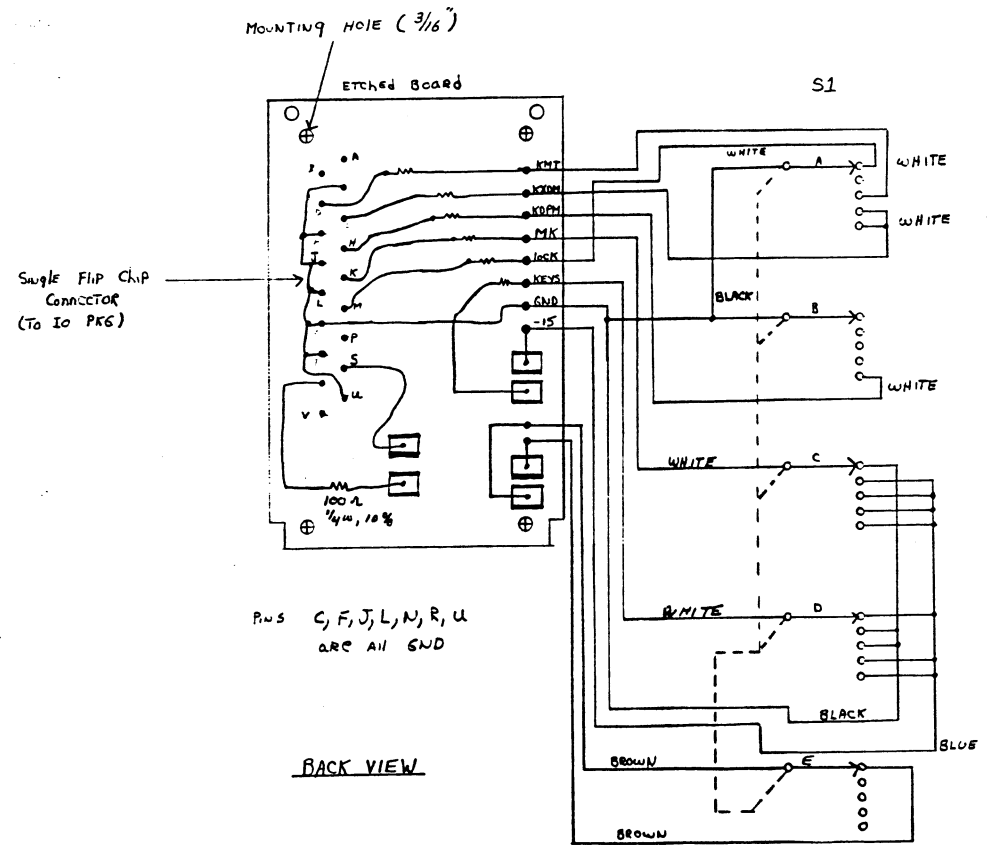
NOTE:
 1. UNLESS OTHERWISE INDICATED:
 RESISTORS ARE 100Ω, 1/4 W, 10% CARBON
 CAPACITORS ARE .01μF
 DIODES ARE D664
 WIRING IS 22 AWG STRANDED, WHITE.
 2. KEYS & SWITCHES SHOWN IN UNASSERTED POSITION.

D-CS-9-0-3 Console Keys and Wiring Diagram



D-CS-9-0-4 Console Indicators

Maintenance PANEL WIRING



PWS C, F, J, L, N, R, U ARE ALL GND

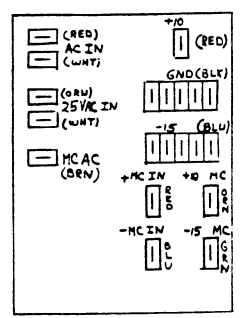
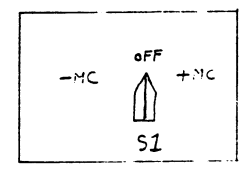
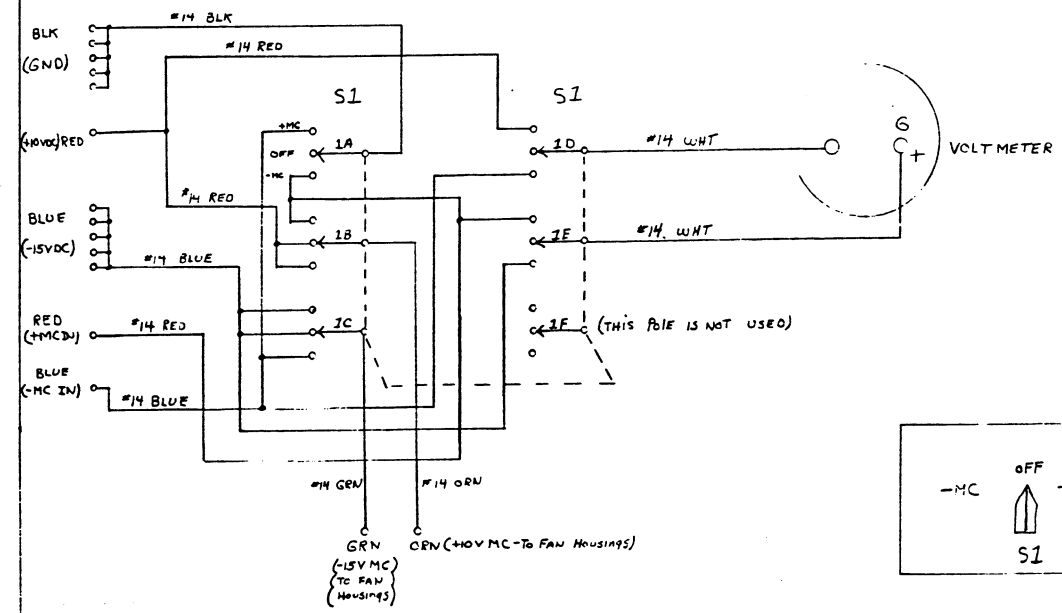
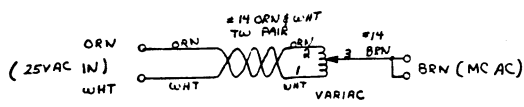
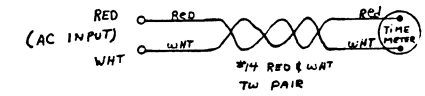
BACK VIEW

ETCHED BOARD
POP-9 Maintenance Panel
"5003944-0-0 C

UNLESS OTHERWISE SPECIFIED:
All Resistors are 1/4W 10%
All Capacitors are .01MFD DISK SPRAGUE
All wiring is #22 gauge (stranded)

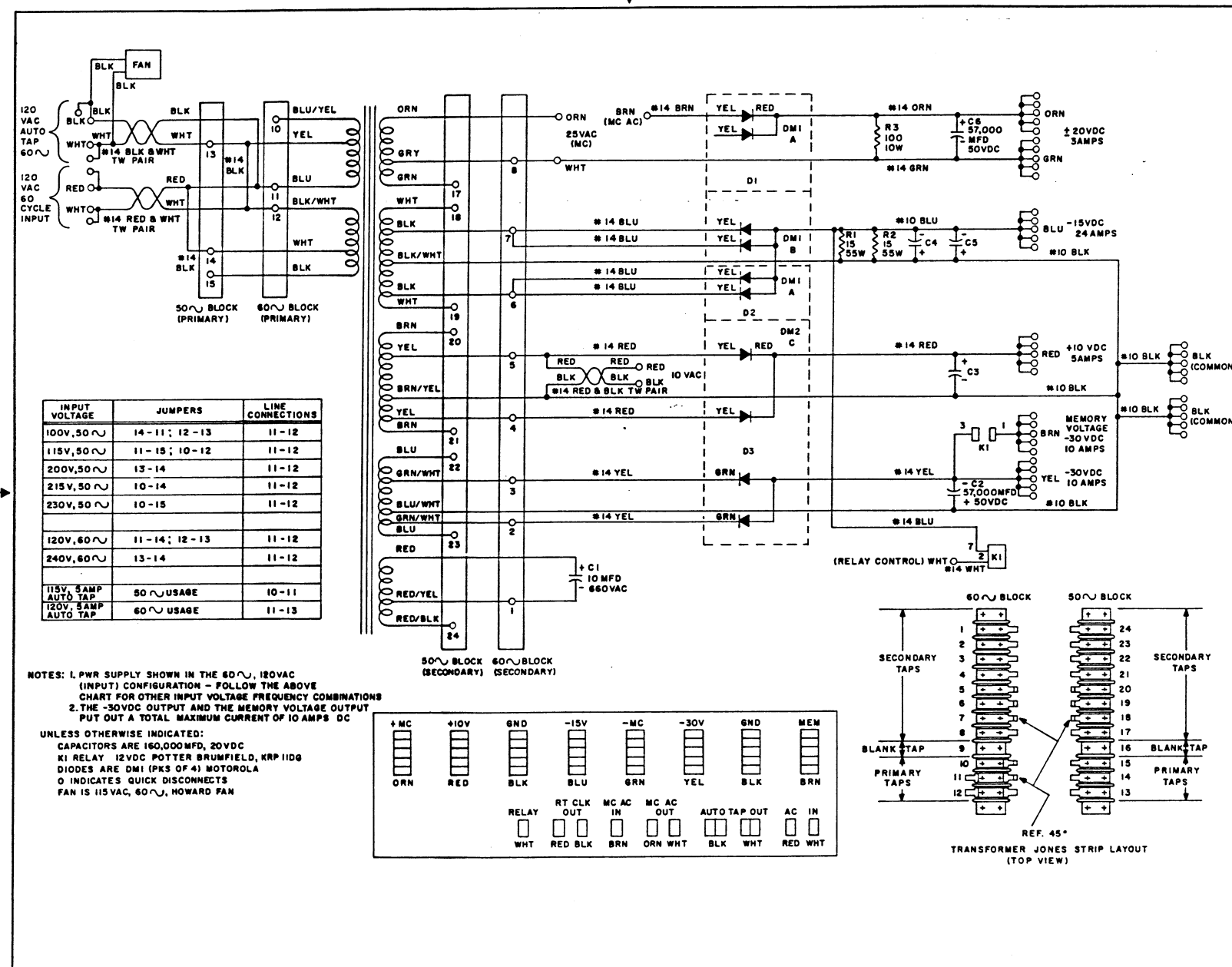
S1 (6M-5P26)
LOCK
NORMAL
MAINTENANCE
EXAMINE
DEPOSIT

MARGINAL CHECK PANEL WIRING

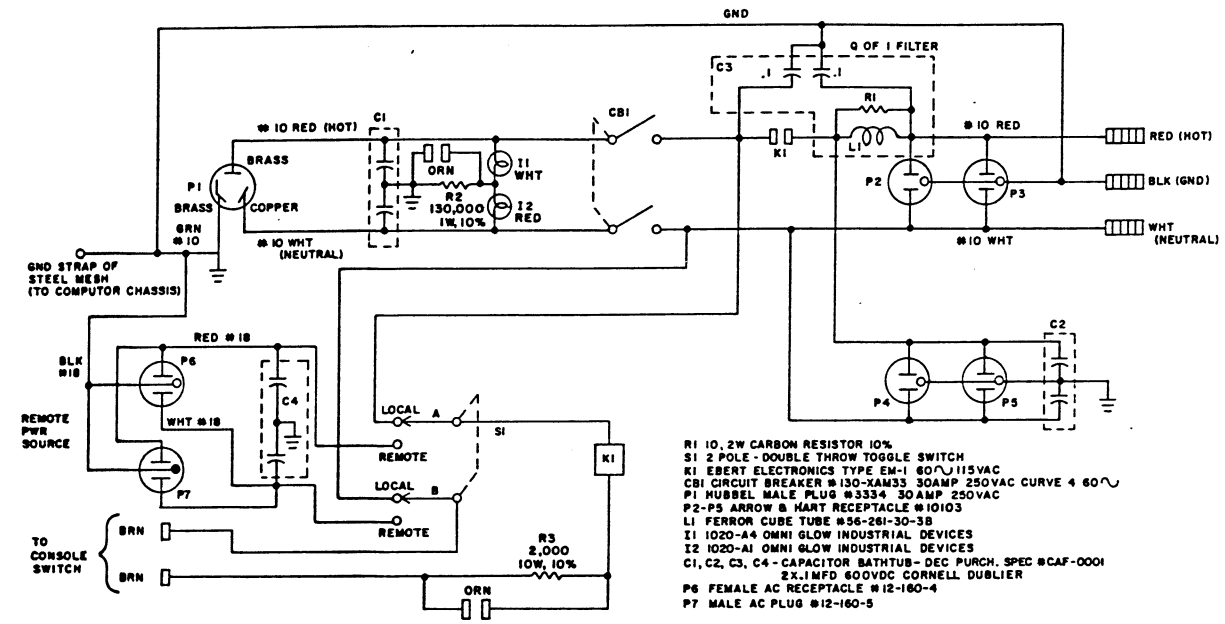


MARGINAL CHECK
Tab PANEL

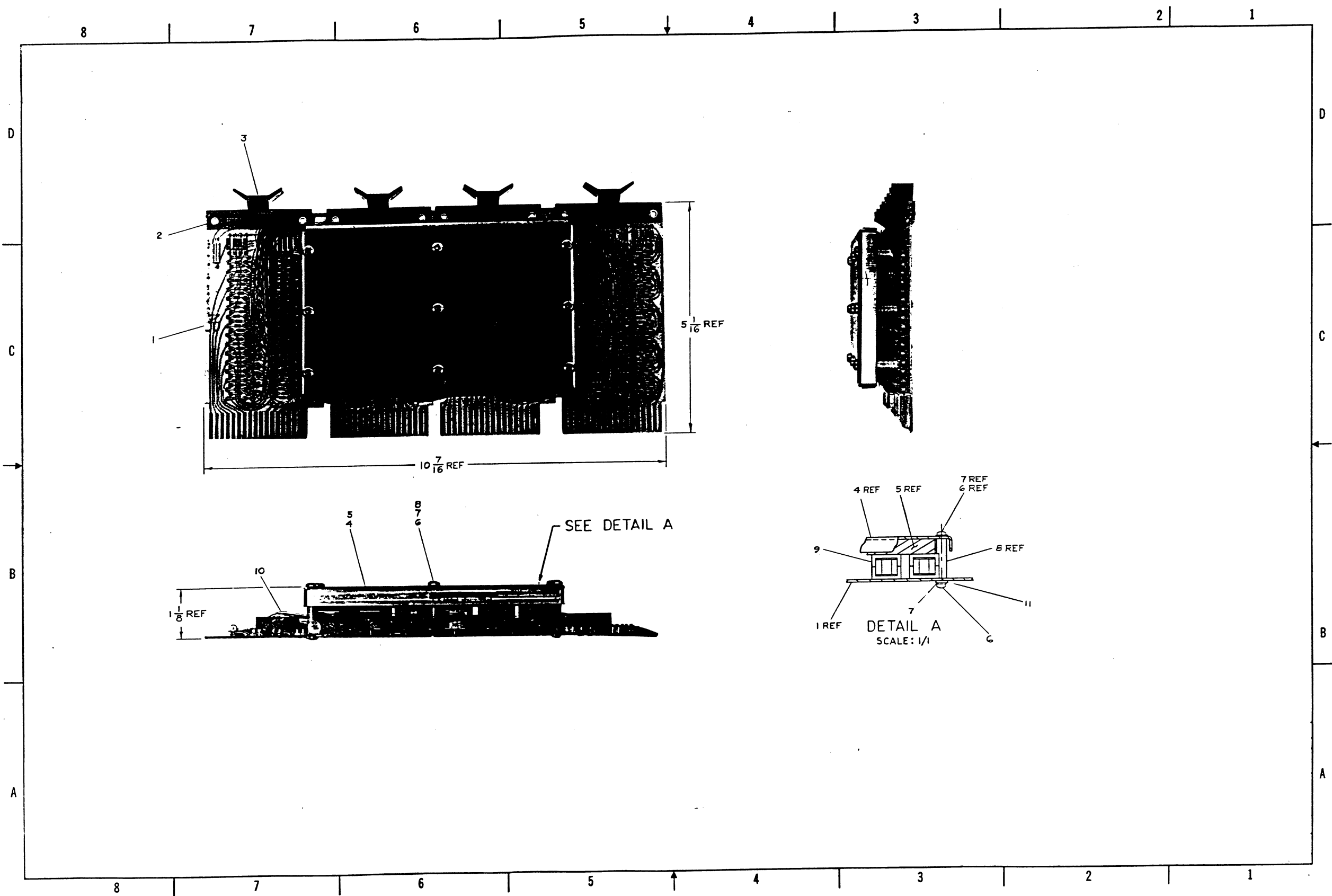
- UNLESS OTHERWISE SPECIFIED:
1. TIME METER Hobbs
 2. VARIAC (0-40VAC) 10B-40 POWERSTAT
 3. S1 Heavy Duty 3 Pos; 6 Pos 34-12451
 4. Voltmeter 10-0-10 VDC (SE 2 1/2" version)



C-CS-709-0-1 709 Power Supply



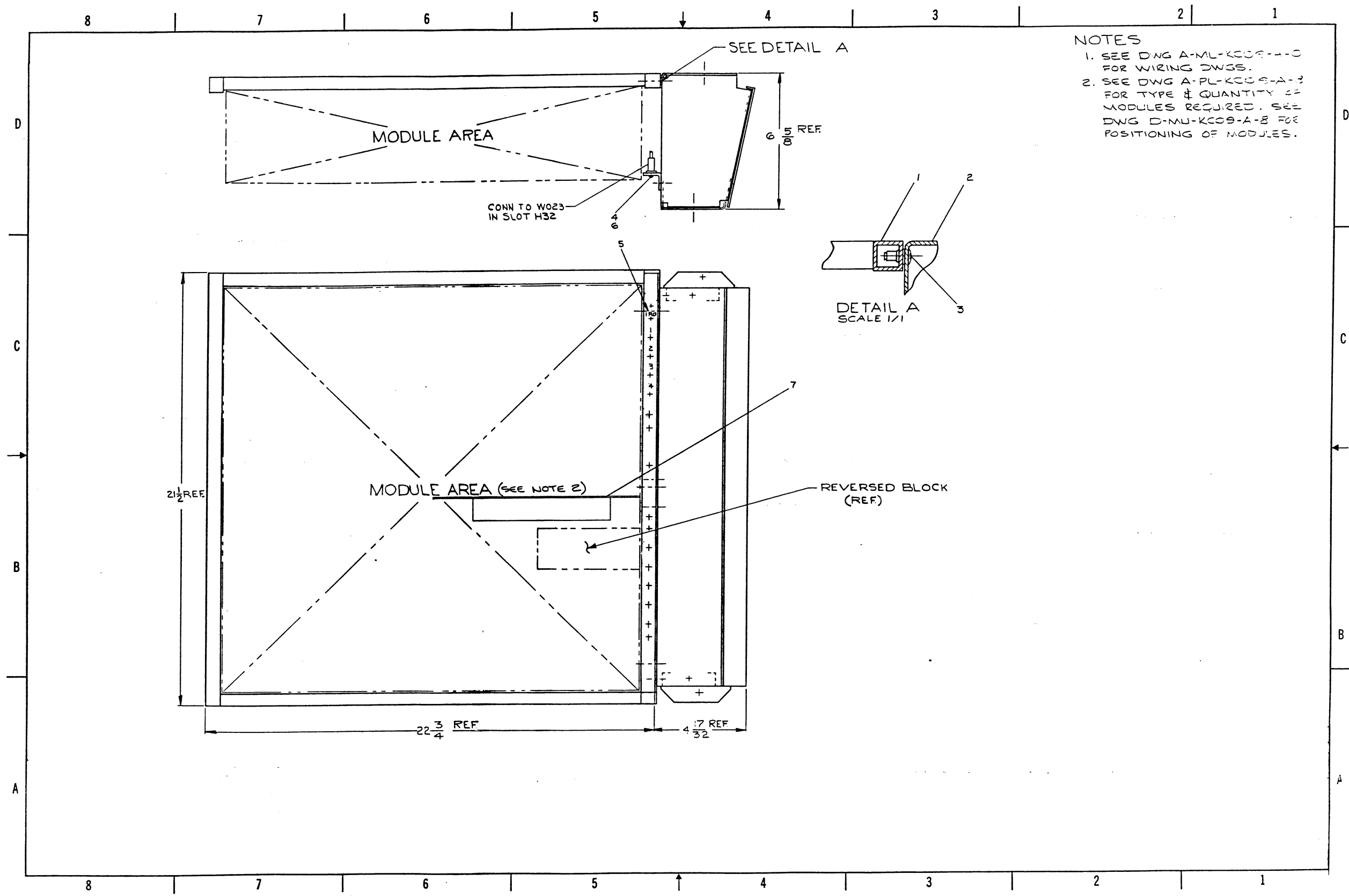
B-CS-841-A-1 841A Power Control



D-UA-MC09-A-0 Control Memory Type MC09-A

PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION		DEC. STOCK NO.
			ITEM	STOCK SIZE — CAT. NO. — MFG.	
1	D-UA-G920-0-0	1		G920 ASSEMBLY	
2		8		EYELET GS-4-9 STIMPSON	
3	MD-C-100151-1-0-2	4		HANDLE (GREEN) LABEL "MC09"	1202258
4	C-MD-5503916-0-0	1		COVER PLATE	
5		2		FOAM POLYURETHANE (RECLAIMED) #18 DENSITY 2 9/16 x 3 9/16 x 3/8	
6		18		SCR PHL H PAN #6-32 x 1/2 SST	
7		18		WASH LOCK INT #6 SST	
8		9		STAND-OFF #6T-1000 CURRENT INC	
9		36		"E" CORE #CF-903 INDIANA GEN.	
10		AR		WIRE #27 COPPER PLY HEAT STRIP	
11		9		WASHER NYLON #6 x 1/32 THK	

A-PL-MC09-A-0 Control Memory Type MC09-A

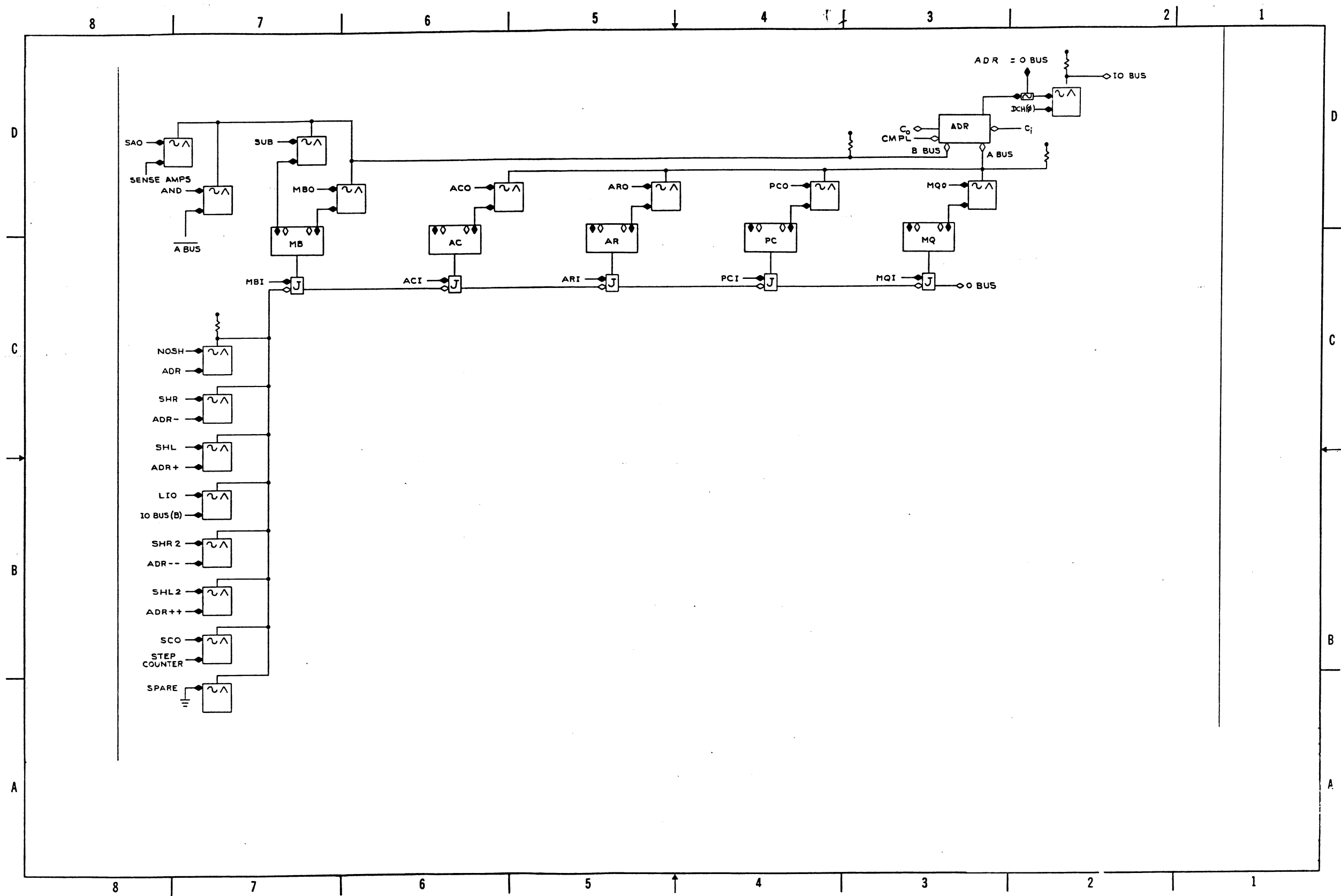


- NOTES
1. SEE DWG A-ML-KC09-A-0 FOR WIRING DWGS.
 2. SEE DWG A-PL-KC09-A-3 FOR TYPE & QUANTITY OF MODULES REQUIRED. SEE DWG D-MU-KC09-A-8 FOR POSITIONING OF MODULES.

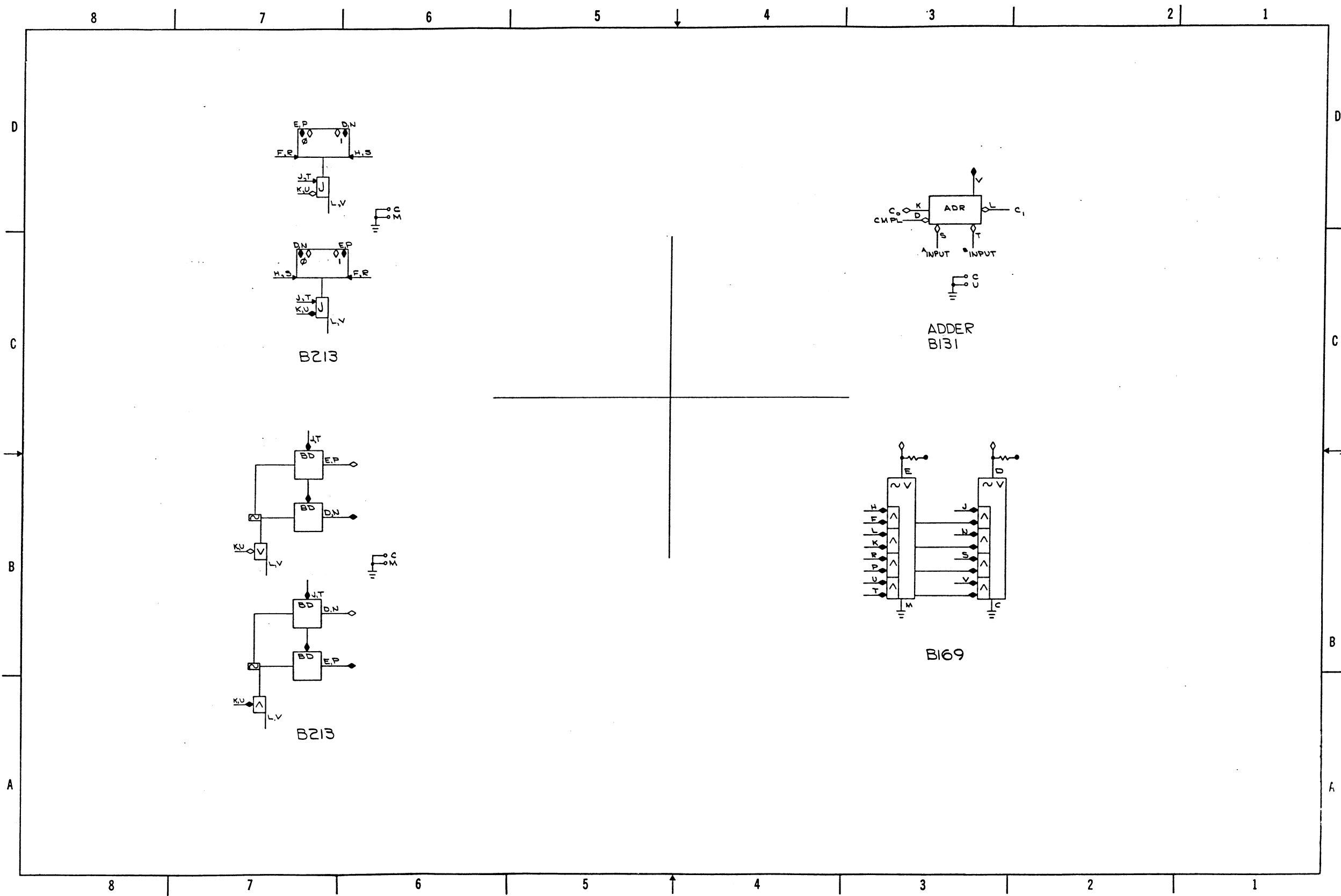
D-UA-KC09-A-0 Unit Assembly

PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION		DEC. STOCK NO.
			ITEM	STOCK SIZE — CAT. NO. — MFG.	
1	D-AD-7005303-0-0	1		CENTRAL PROCESSOR BUS ASSEMBLY	7005303-0-0
2	A-PL-7005229-0-0	1		FAN & MARGINAL CHECK ASSY	7005229-0-0
3		3		SCR PHL TRUS HD 1/4-20 x 5/8 SST	
	A-ML-KC09-A	REF		MDL (CENTRAL PROCESSOR ASSY)	
	D-MU-KC09-A-8	REF		MODULE UTILIZATION LIST	
	A-PL-KC09-A-8	REF		MODULE LIST	
4	D-IA-7005385-0-0	1		AIR BAFFLE SW ASSY (KC09-A)	7005385-0-0
5	A-SS-7405842-0-0	AS REQD		SCOTCHCAL STICKERS	7405842-0-0
6		2		SCR PHL HD PAN 6-32 x 9/16 SST	
7	A-PL-MC09-A-0	1		CONTROL MEMORY MC09-A	

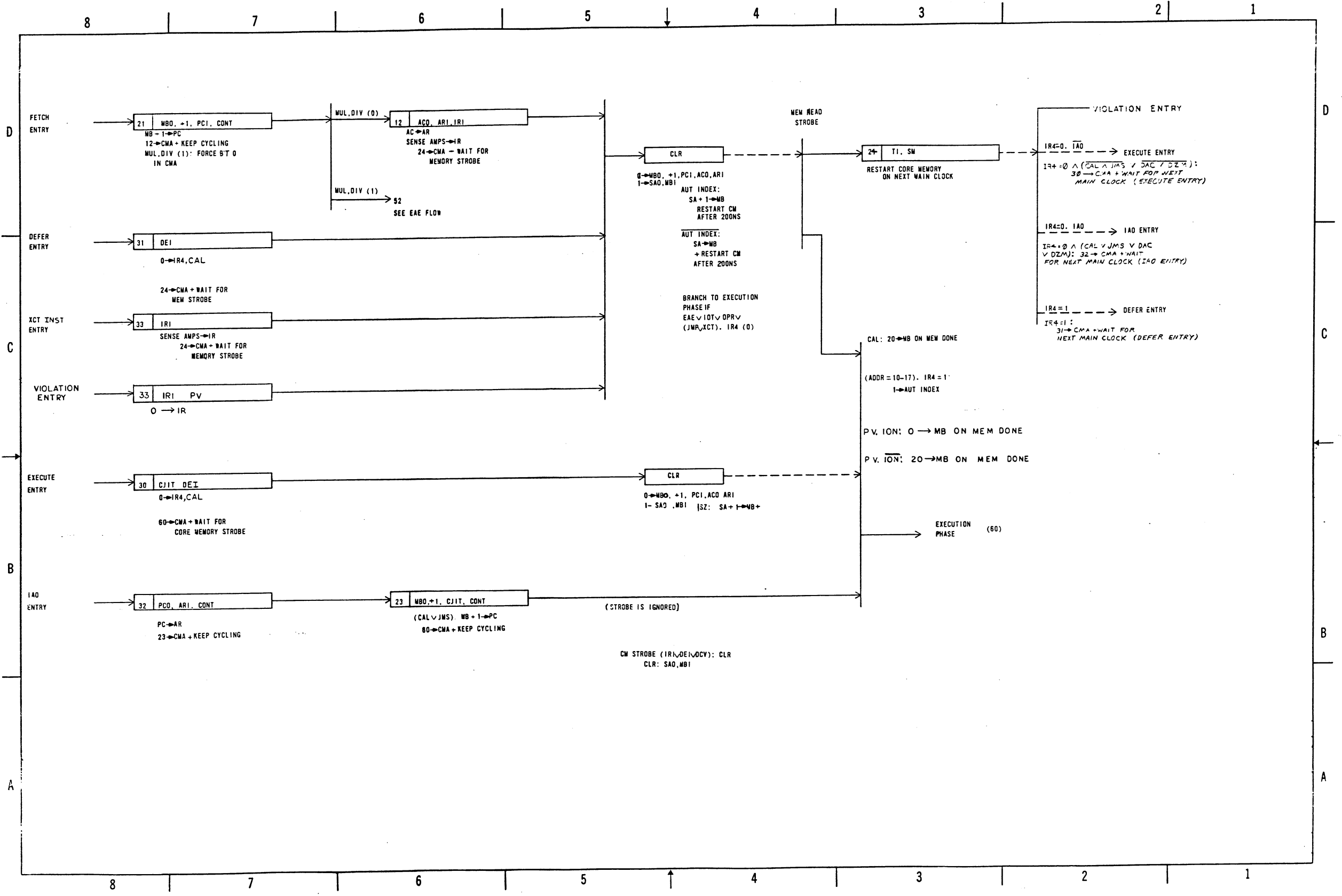
A-PL-KC09-A-0 Assembly Parts List



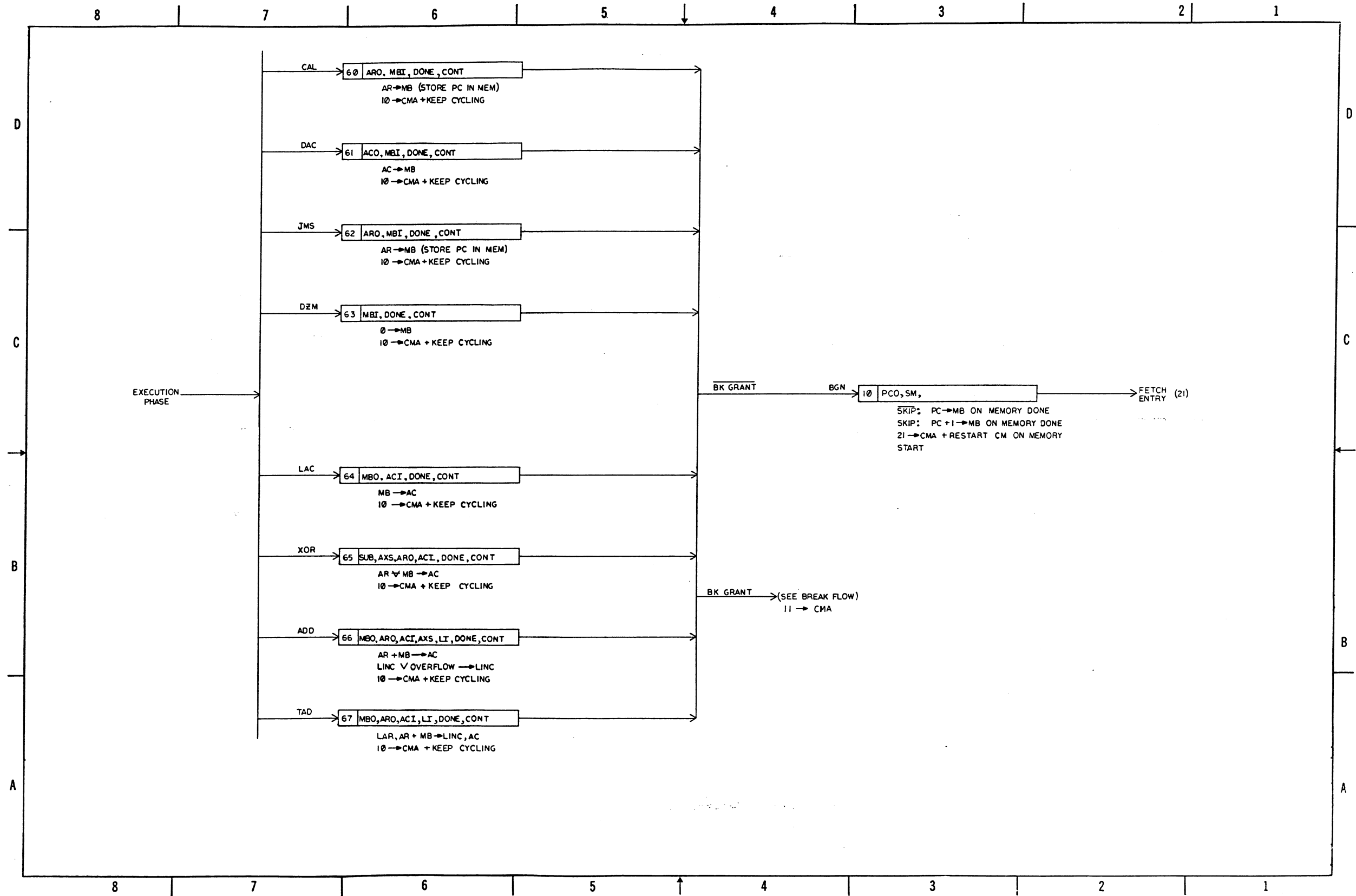
D-BS-KC09-A-1 Register Configuration



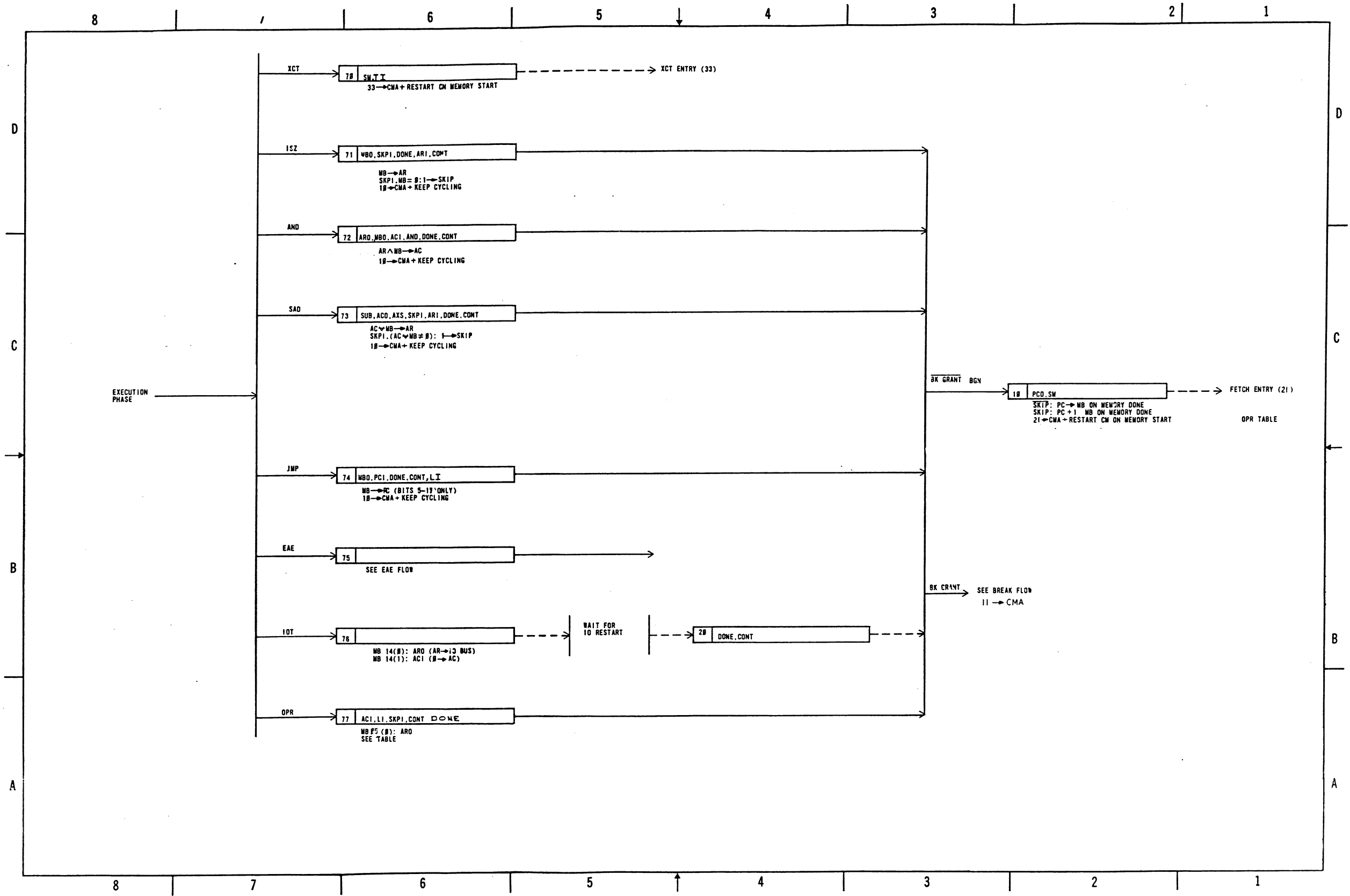
D-BS-KC09-A-2 Special Modules



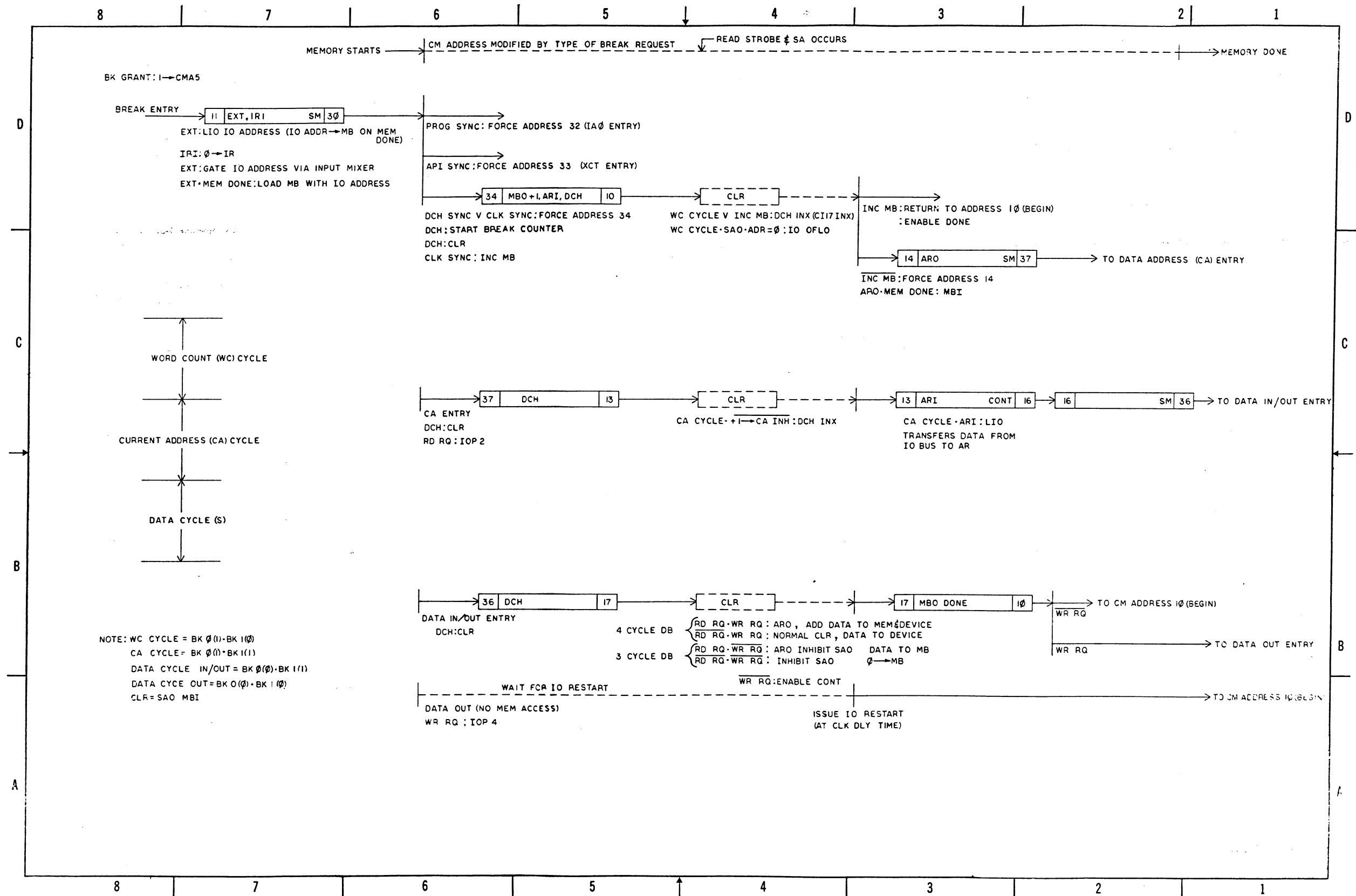
D-FD-KC09-A-3 Operand Fetch Flow



D-FD-KC09-A-4 Execution Flow (Sheet 1)

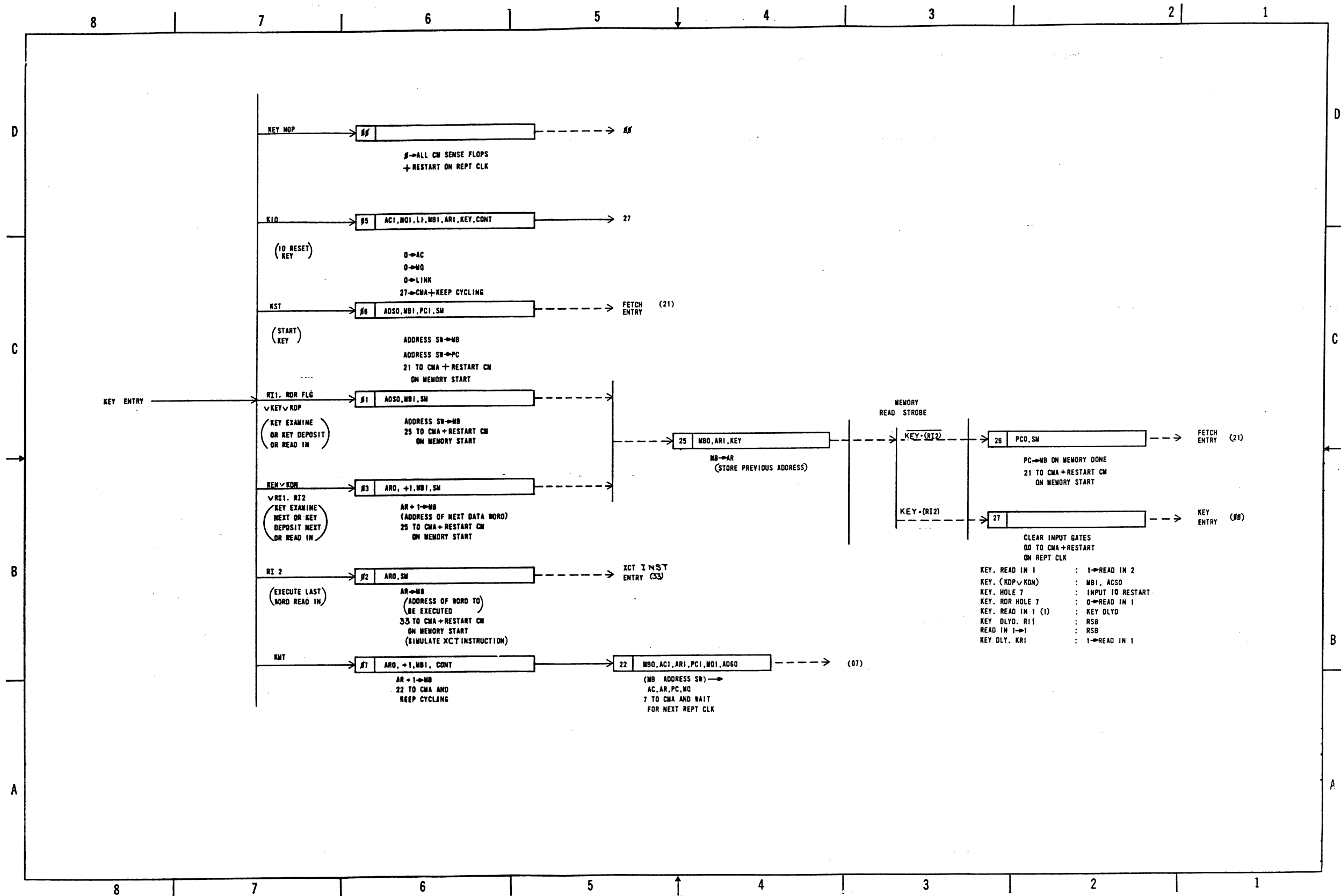


D-FD-KC09-A-4 Execution Flow (Sheet 2)



NOTE: WC CYCLE = BK 0(1) · BK 1(0)
 CA CYCLE = BK 0(1) · BK 1(1)
 DATA CYCLE IN/OUT = BK 0(0) · BK 1(1)
 DATA CYCLE OUT = BK 0(0) · BK 1(0)
 CLR = SAO MBI

D-FD-KC09-A-5 Break Flow



KEY. READ IN 1 : 1 → READ IN 2
 KEY. (KDP, KDH) : MB1, ACSD
 KEY. HOLE 7 : INPUT 10 RESTART
 KEY. RDR HOLE 7 : 0 → READ IN 1
 KEY. READ IN 1 (1) : KEY DLYD
 KEY DLYD. R11 : RSB
 READ IN 1 → 1 : RSB
 KEY DLY. KRI : 1 → READ IN 1

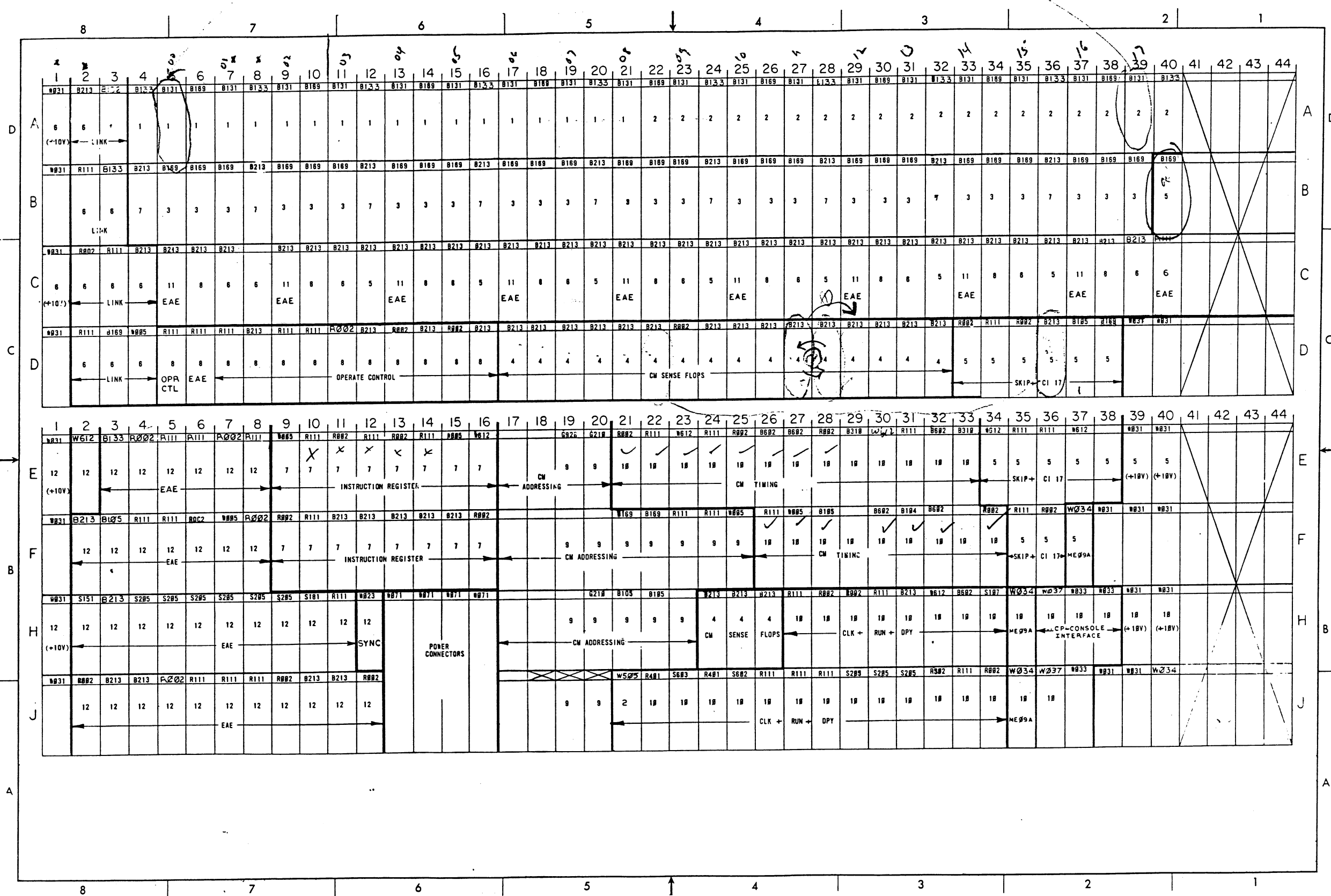
D-FD-KC09-A-6 Key Flow

PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION			DEC. STOCK NO.
			ITEM	STOCK SIZE	CAT. NO. — MFG.	
		1	B104	INVERTER		
		4	B105	INVERTER		
		19	B131	ADDER		
		41	B169	INVERTER		
		75	B213	FLIP-FLOP		
		2	B310	DELAY LINE		
		7	B602	PULSE AMPLIFIER		
		2	G210			
		1	G920			
		18	R002	DIODE NETWORK		
		30	R111	DIODE GATE		
		1	R302	DELAY ONE SHOT		
		2	R401	CLOCK		
		1	S107	INVERTER		
		3	S205	DUAL FLIP FLOP		
		1	S602	PULSE AMPLIFIER		

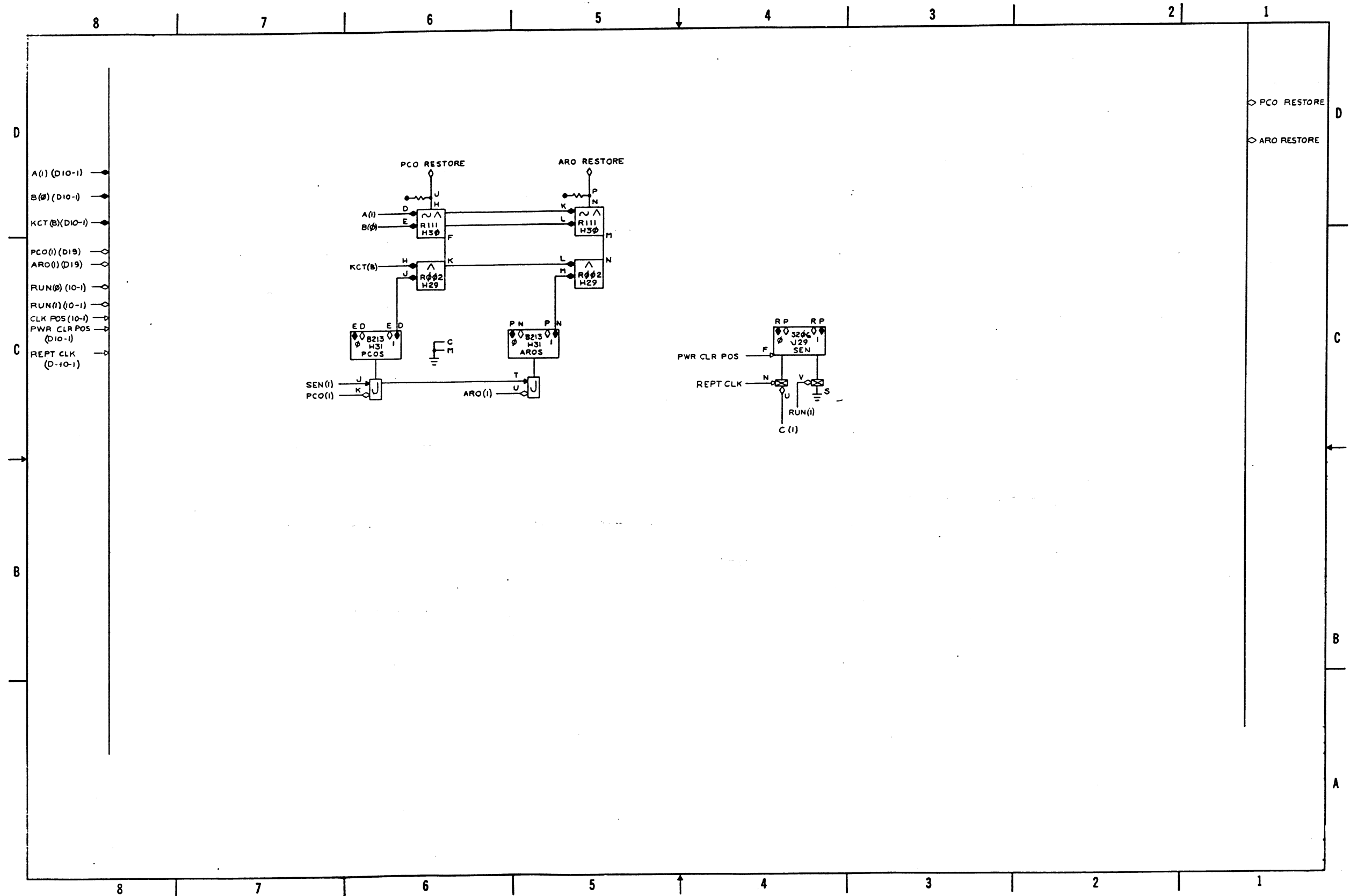
A-PL-KC09-A-8 Module Parts List (Sheet 1)

PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION			DEC. STOCK NO.
			ITEM	STOCK SIZE	CAT. NO. — MFG.	
		1	S603	PULSE AMPLIFIER		
		5	W005	CLAMPED LOADS		
		20	W031	SIGNAL CABLE CONN		
		3	W033			
		2	W036			
		4	W071	POWER CONN		
		1	W505			
		5	W612	PULSE AMPLIFIER		
		10	B133			

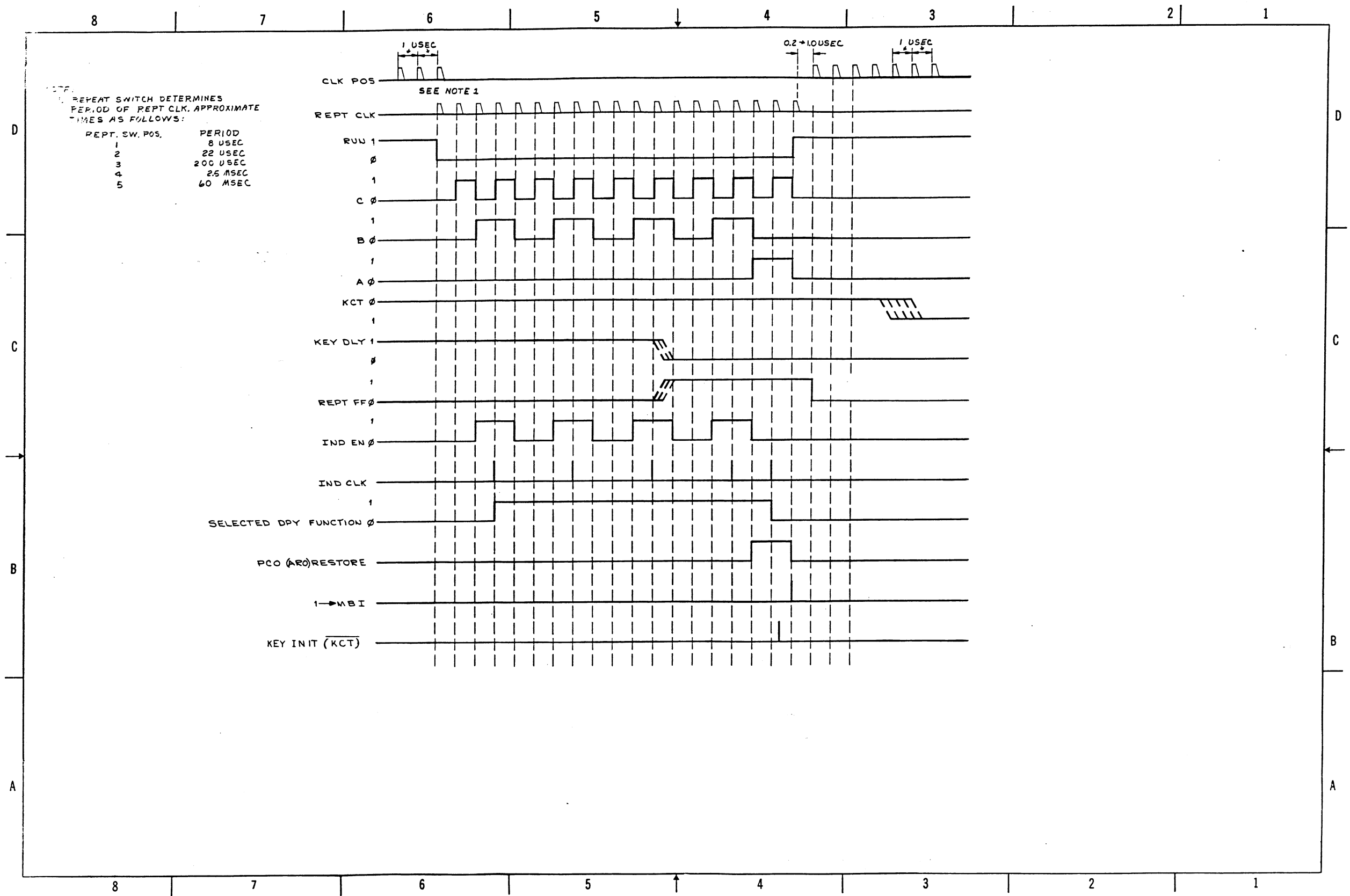
A-PL-KC09-A-8 Module Parts List (Sheet 2)



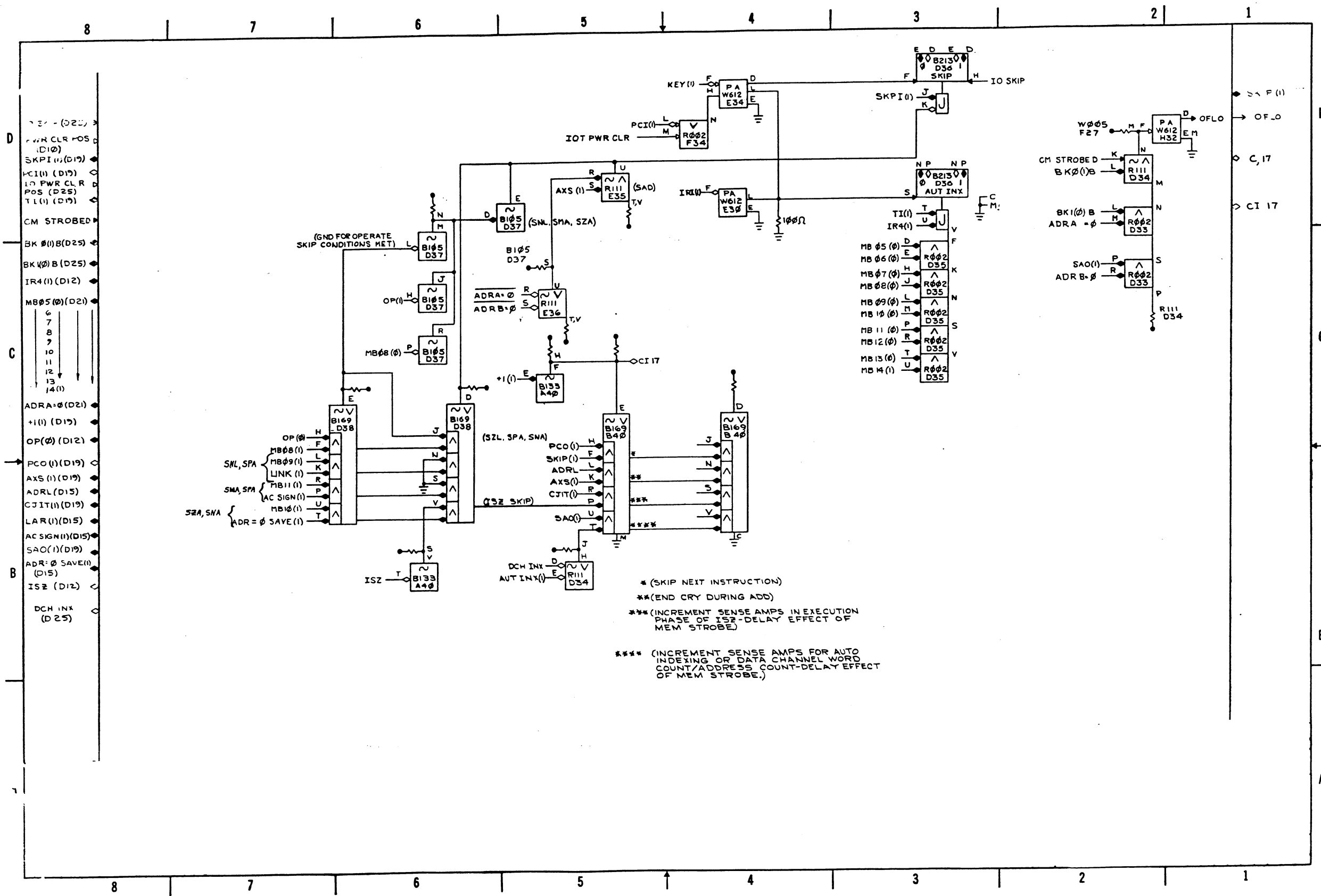
D-IC-KC09-A-9 MC Switch Configuration



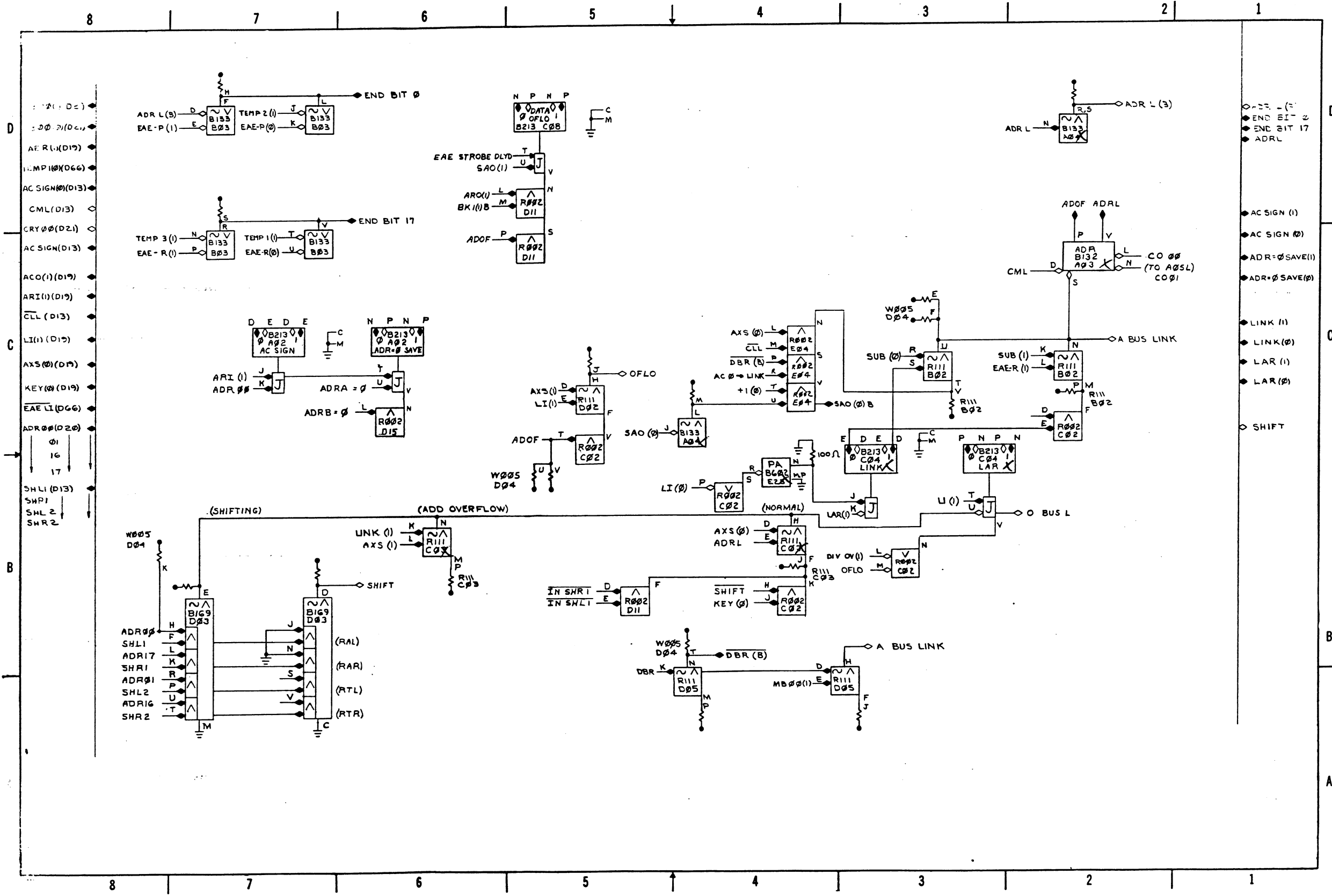
D-BS-KC09-A-10 Clock, Run, and Display (Sheet 2)



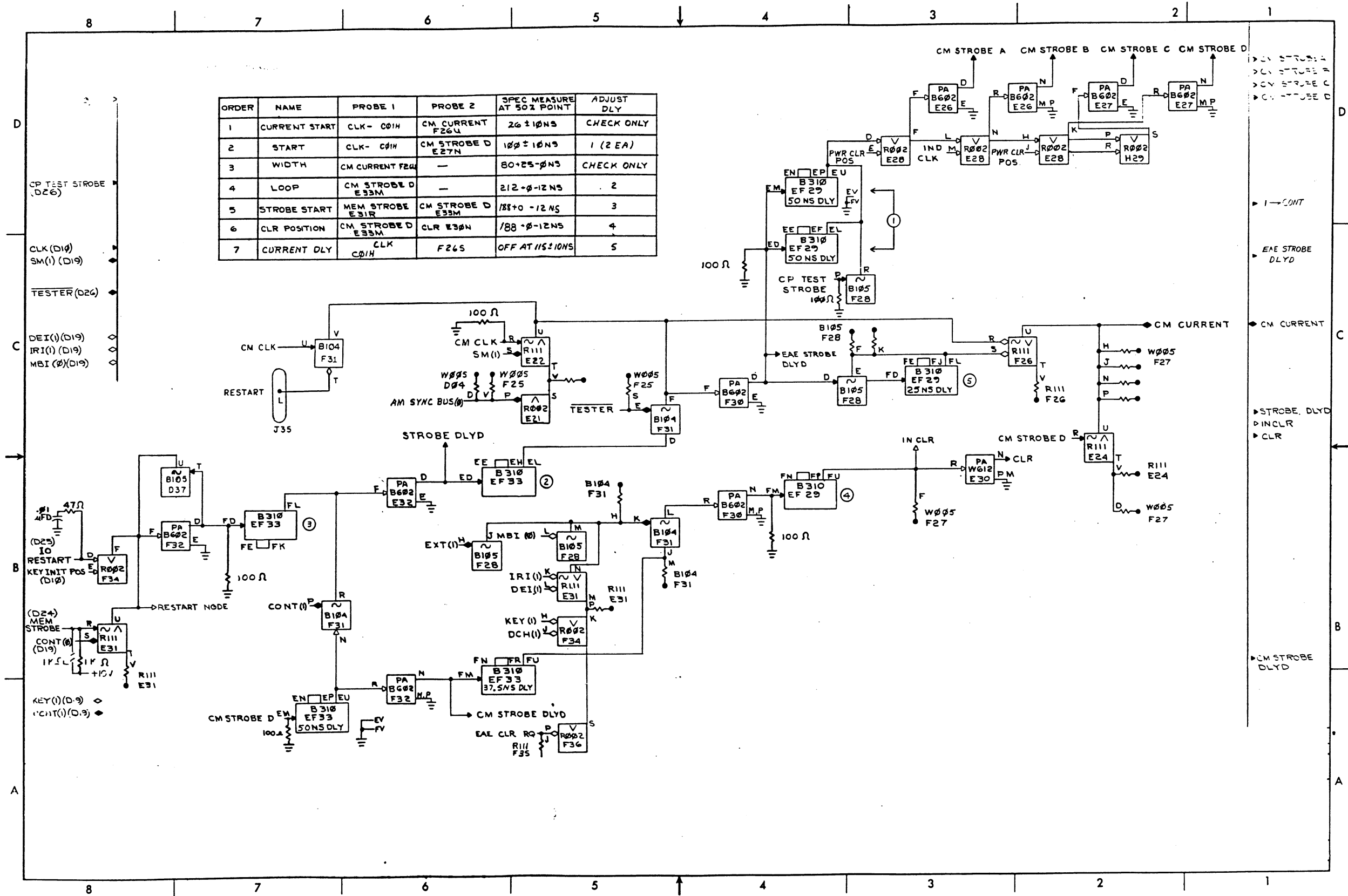
D-TD-KC09-A-11 Clock, Run, and Display Timing



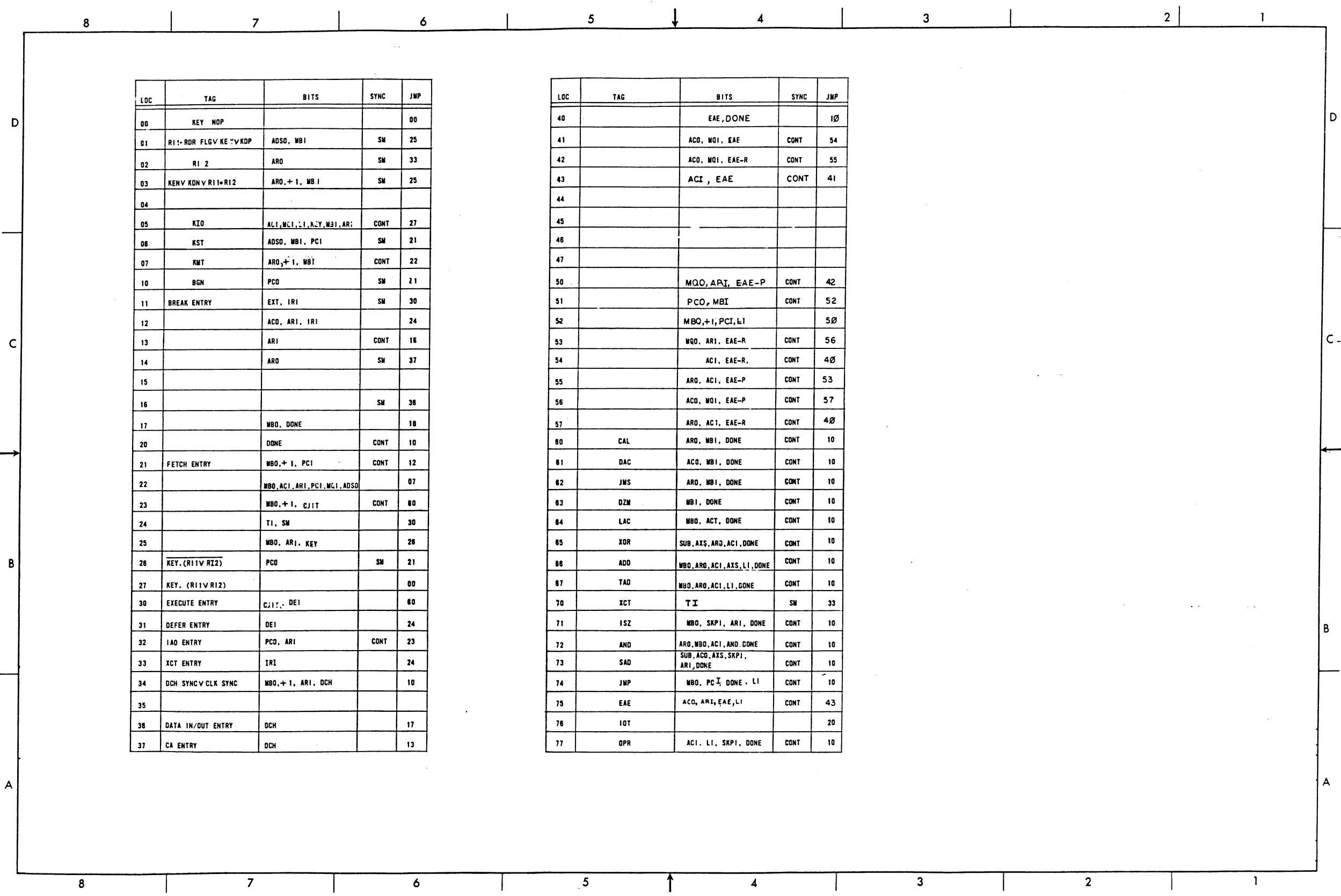
D-BS-KC09-A-14 Skip and CI17



D-BS-KC09-A-15 LINK Control



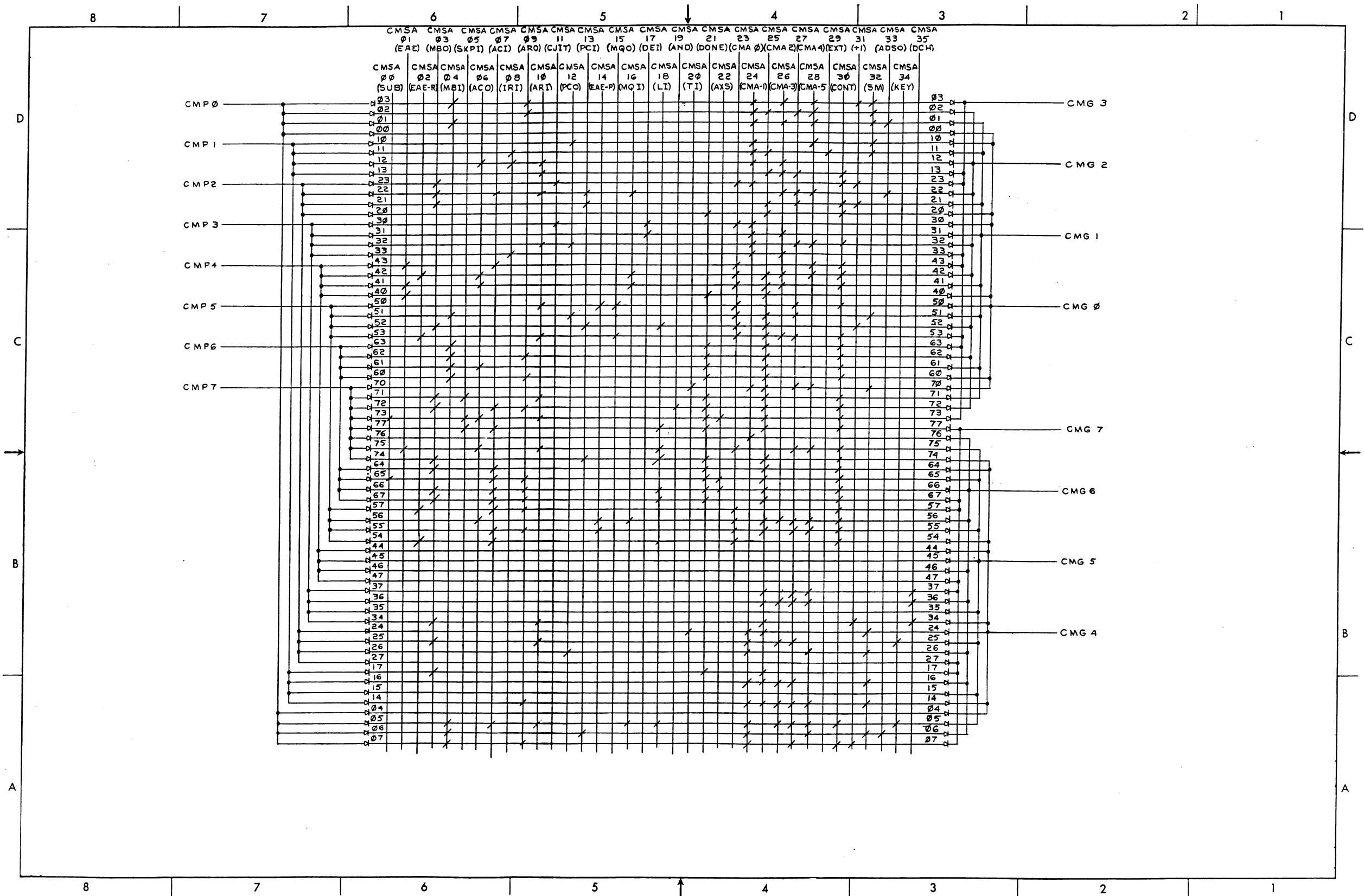
D-BS-KC09-A-16 CM Timing



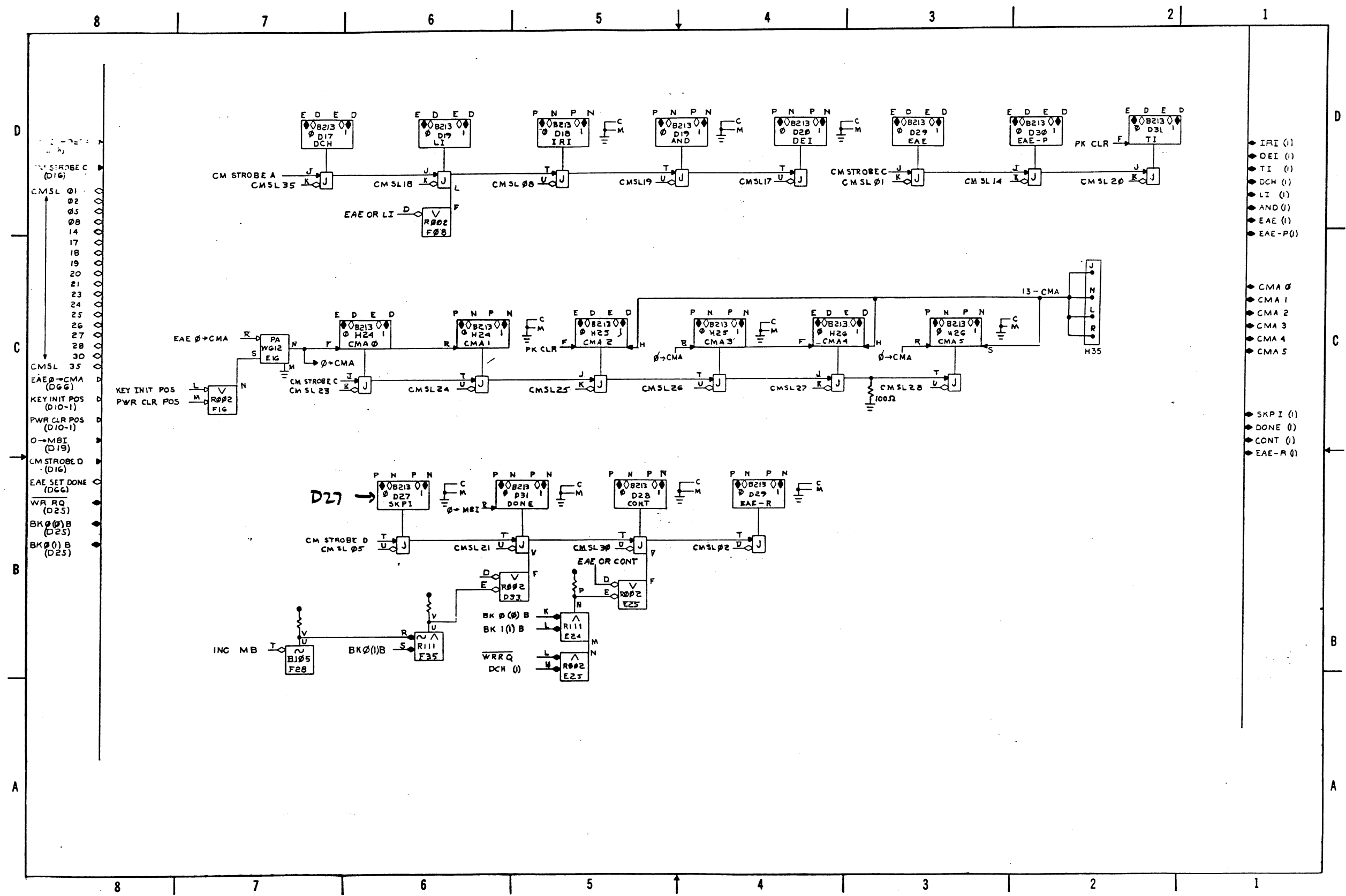
LOC	TAG	BITS	SYNC	JMP
00	KEY NOP			00
01	R11-RDR FLGV KE-VKDP	ADSO, MBI	SM	25
02	R1 2	ARO	SM	33
03	KENV KDN V R11-R12	ARO, + 1, MBI	SM	25
04				
05	KIO	ALI, MBI, LI, KCY, MBI, ARI	CONT	27
06	KST	ADSO, MBI, PCI	SM	21
07	KMT	ARO, + 1, MBI	CONT	22
10	BGN	PCO	SM	21
11	BREAK ENTRY	EXT, IRI	SM	30
12		ACO, ARI, IRI		24
13		ARI	CONT	16
14		ARO	SM	37
15				
16			SM	38
17		MBO, DONE		18
20		DONE	CONT	10
21	FETCH ENTRY	MBO, + 1, PCI	CONT	12
22		MBO, ACI, ARI, PCI, MBI, ADSO		07
23		MBO, + 1, CJIT	CONT	80
24		TI, SM		30
25		MBO, ARI, KEY		28
26	KEY. (R11 V R12)	PCO	SM	21
27	KEY. (R11 V R12)			00
30	EXECUTE ENTRY	CJIT, DEI		80
31	DEFER ENTRY	DEI		24
32	IAO ENTRY	PCO, ARI	CONT	23
33	XCT ENTRY	IRI		24
34	DCH SYNC V CLK SYNC	MBO, + 1, ARI, DCH		10
35				
38	DATA IN/OUT ENTRY	DCH		17
37	CA ENTRY	DCH		13

LOC	TAG	BITS	SYNC	JMP
40		EAE, DONE		10
41		ACO, MBI, EAE	CONT	54
42		ACO, MBI, EAE-R	CONT	55
43		ACI, EAE	CONT	41
44				
45				
46				
47				
50		MBO, ARI, EAE-P	CONT	42
51		PCO, MBI	CONT	52
52		MBO, + 1, PCI, LI		50
53		MBO, ARI, EAE-R	CONT	56
54		ACI, EAE-R	CONT	40
55		ARO, ACI, EAE-P	CONT	53
56		ACO, MBI, EAE-P	CONT	57
57		ARO, ACI, EAE-R	CONT	40
60	CAL	ARO, MBI, DONE	CONT	10
61	DAC	ACO, MBI, DONE	CONT	10
62	JMS	ARO, MBI, DONE	CONT	10
63	DZM	MBI, DONE	CONT	10
64	LAC	MBO, ACT, DONE	CONT	10
65	XOR	SUB, AXS, ARO, ACI, DONE	CONT	10
66	ADD	MBO, ARO, ACI, AXS, LI, DONE	CONT	10
67	TAD	MBO, ARO, ACI, LI, DONE	CONT	10
70	XCT	TI	SM	33
71	ISZ	MBO, SKPI, ARI, DONE	CONT	10
72	AND	ARO, MBO, ACI, AND, DONE	CONT	10
73	SAD	SUB, ACO, AXS, SKPI, ARI, DONE	CONT	10
74	JMP	MBO, PCI, DONE, LI	CONT	10
75	EAE	ACO, ARI, EAE, LI	CONT	43
76	IOT			20
77	OPR	ACI, LI, SKPI, DONE	CONT	10

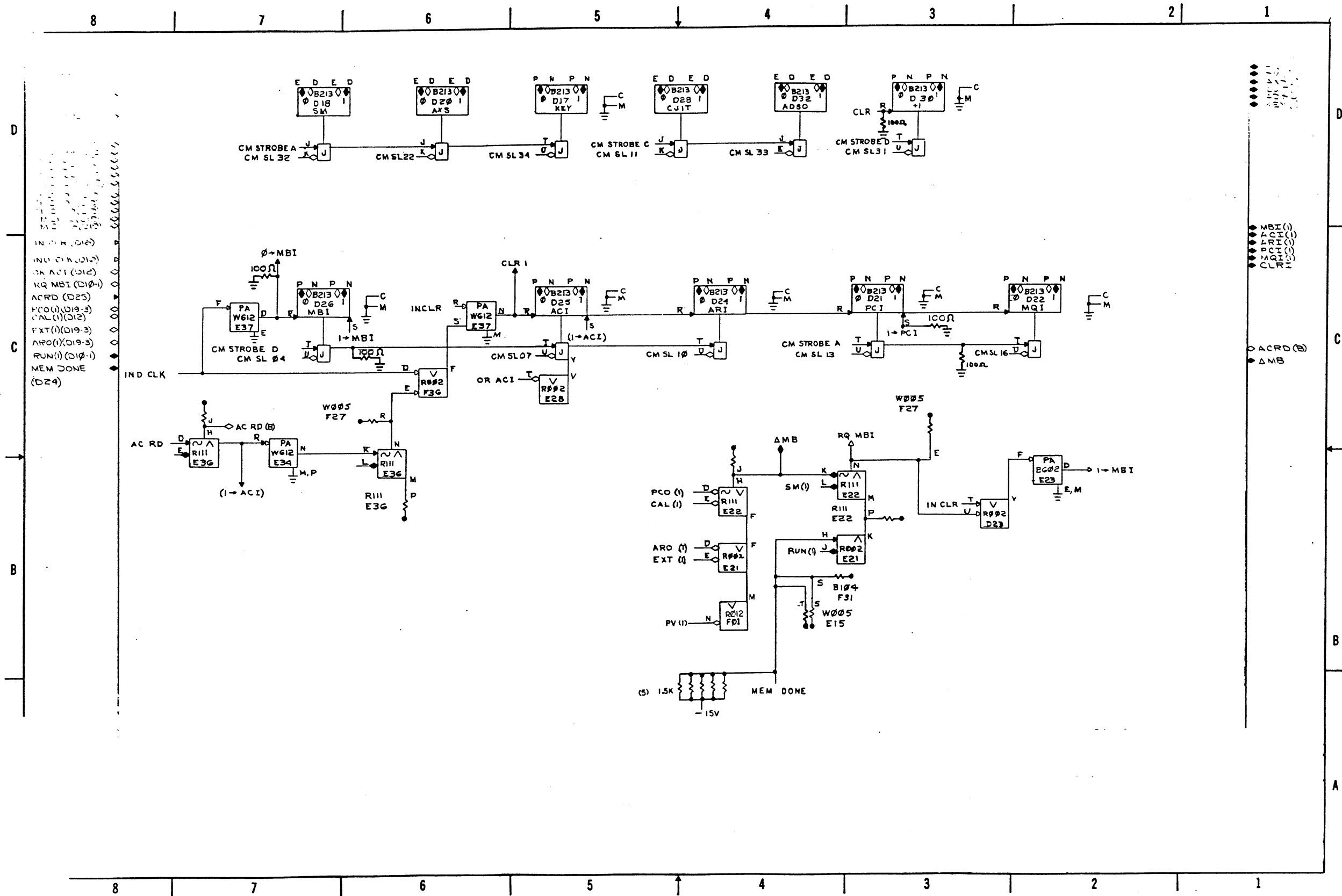
D-FD-KC09-A-18 CM Wiring Matrix and Program (Sheet 1)



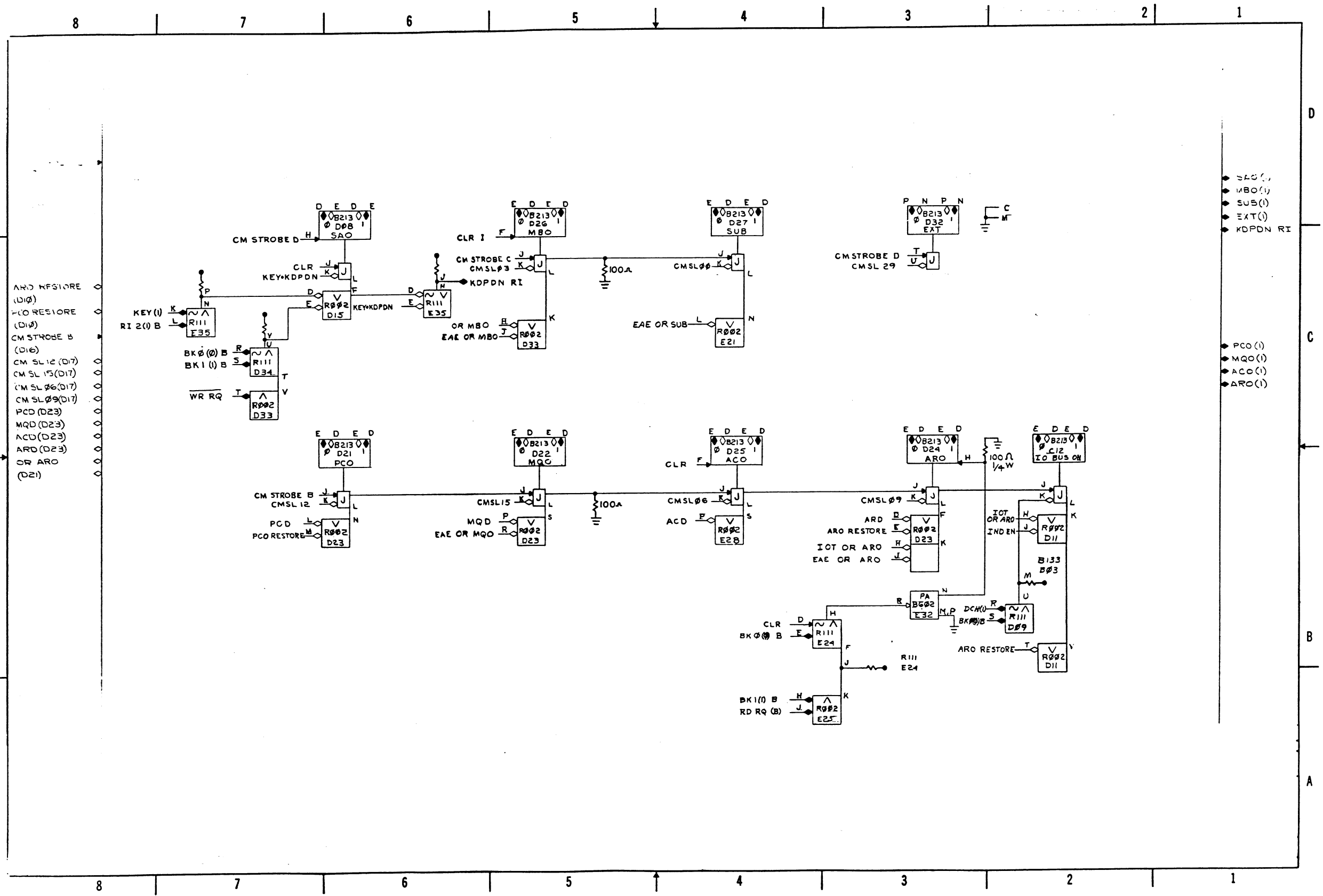
D-FD-KC09-A-18 CM Wiring Matrix and Program (Sheet 2)



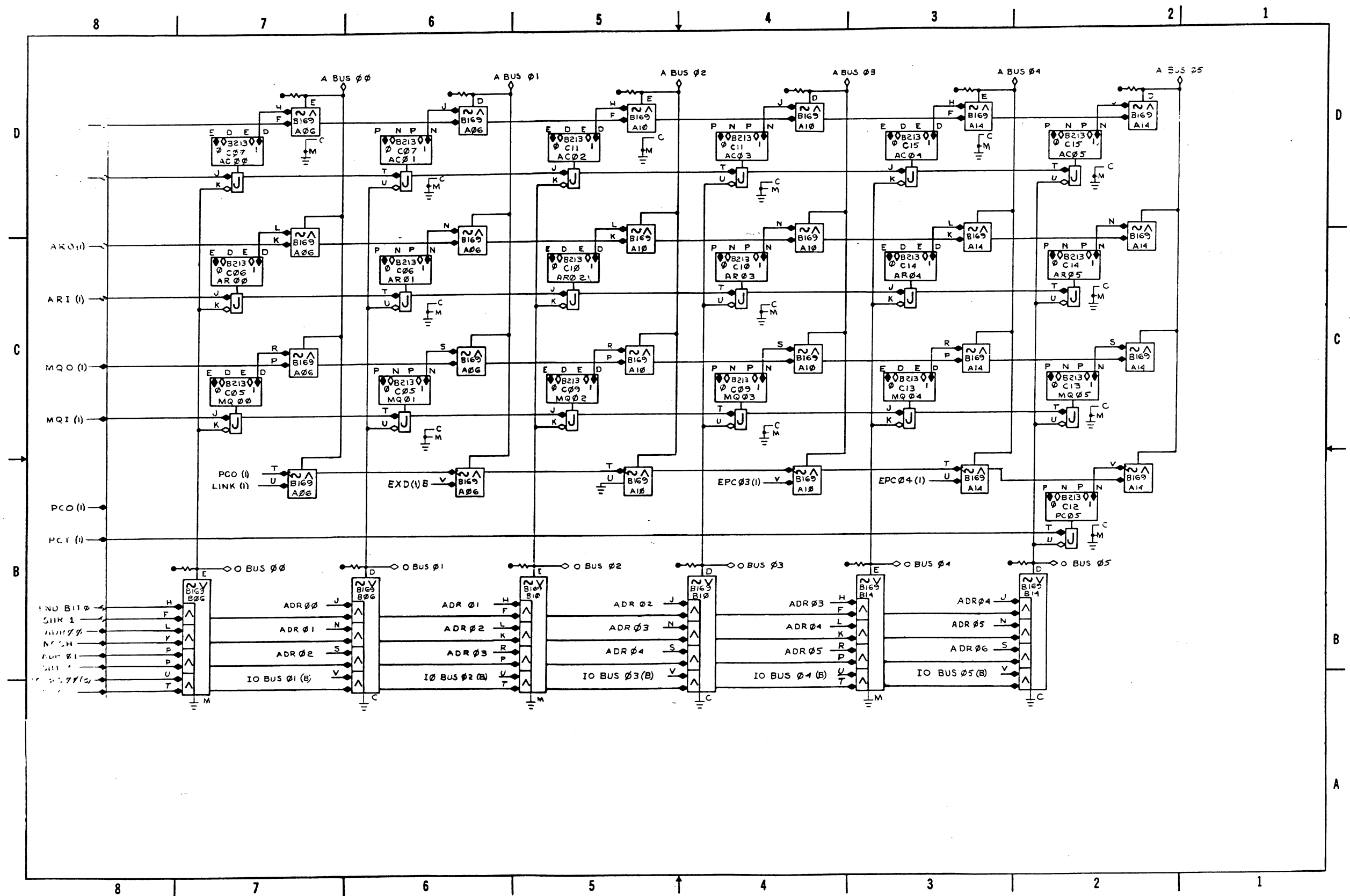
D-BS-KC09-A-19 CM Sense Flip-Flops (Sheet 1)



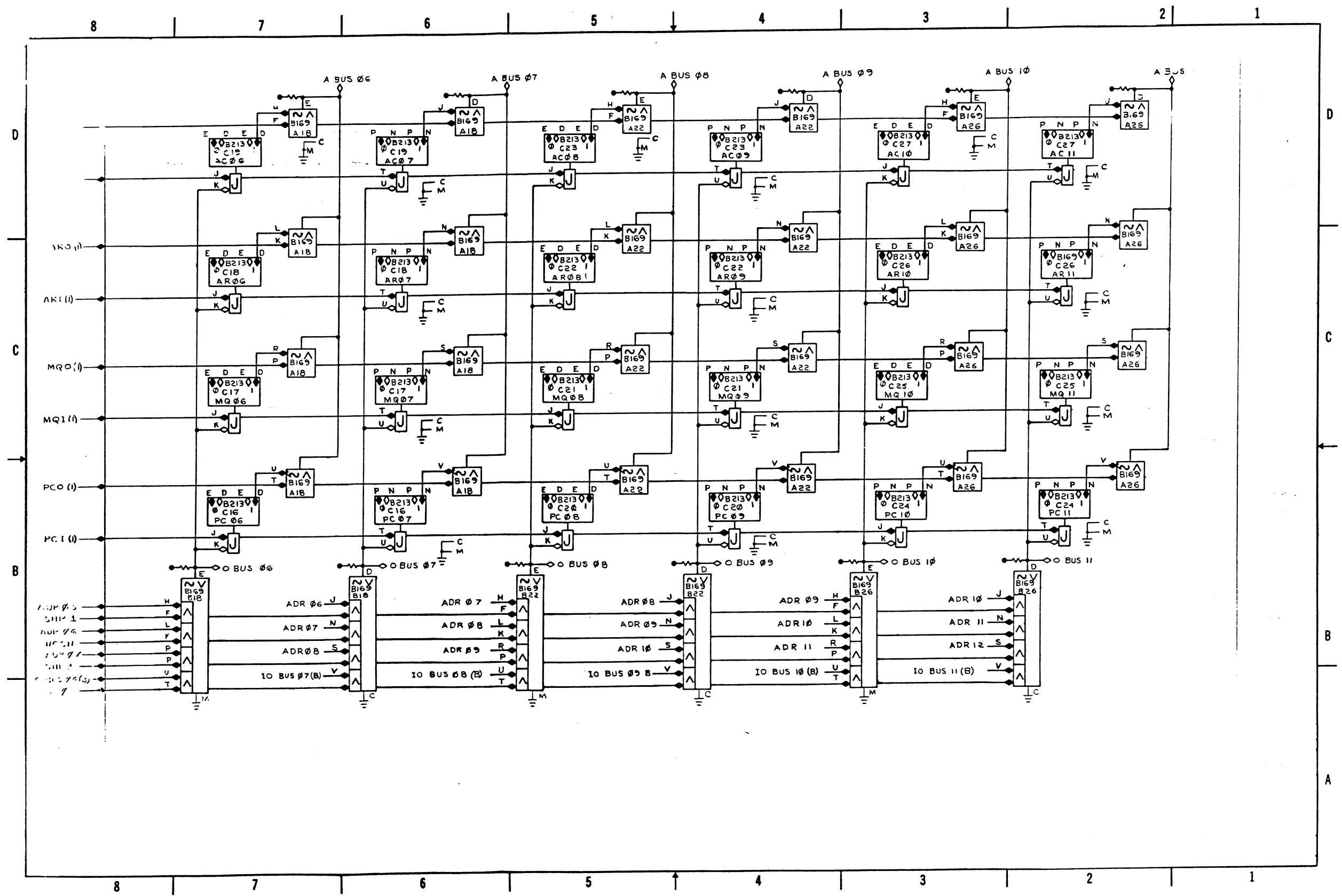
D-BS-KC09-A-19 CM Sense Flip-Flops (Sheet 2)



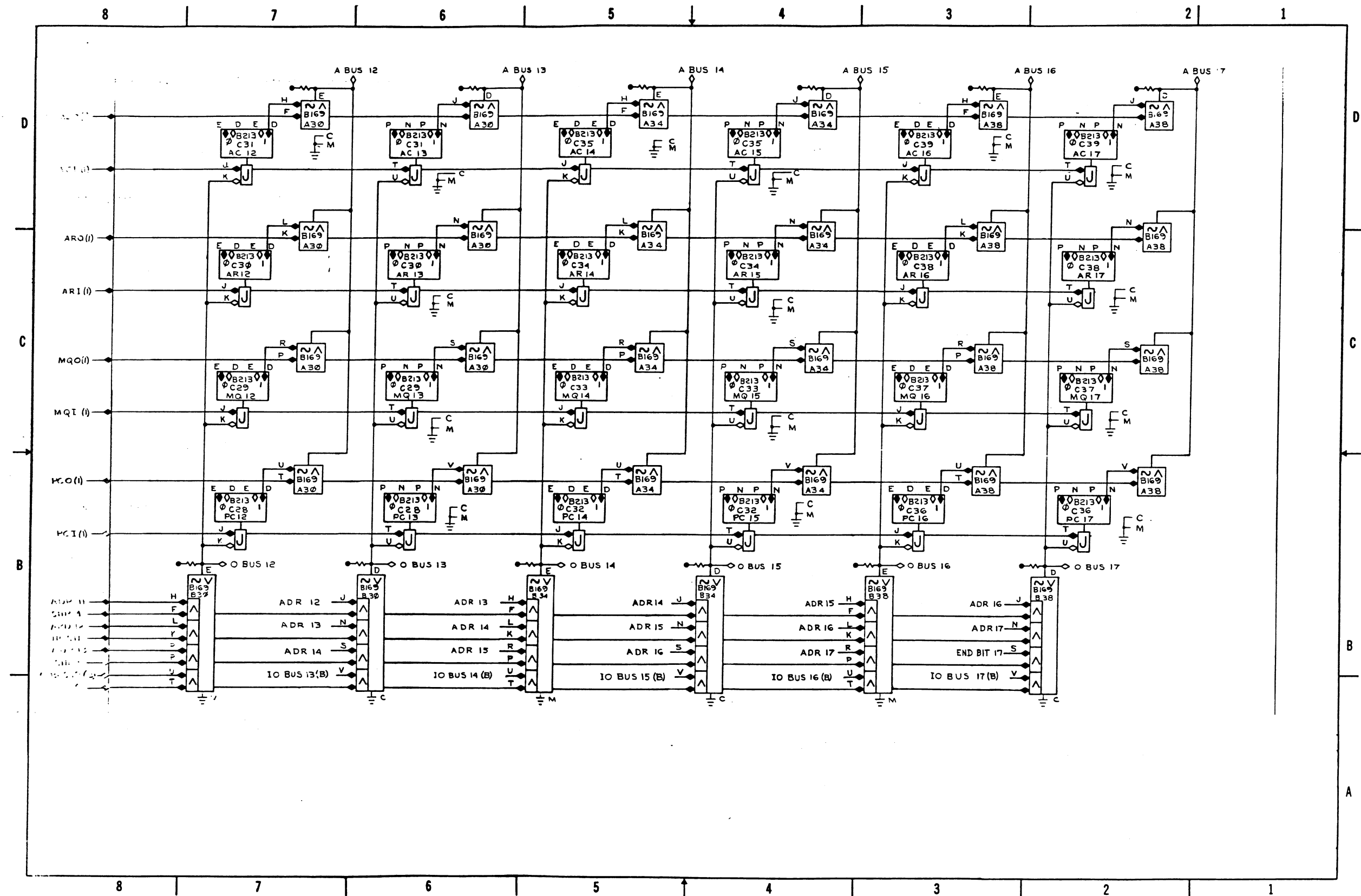
D-BS-KC09-A-19 CM Sense Flip-Flops (Sheet 3)



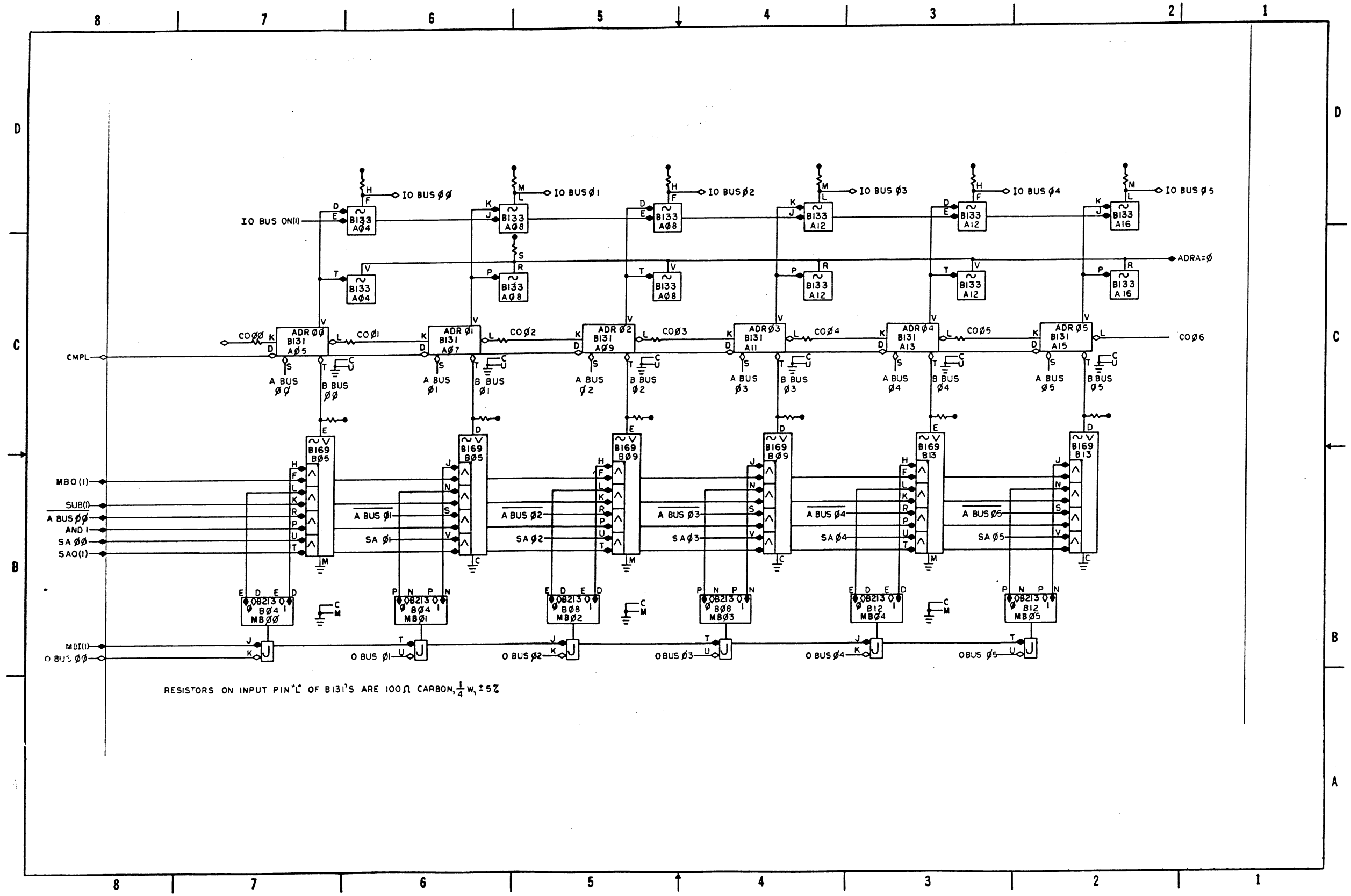
D-BS-KC09-A-20 AC, AR, MQ, PC (Sheet 1)



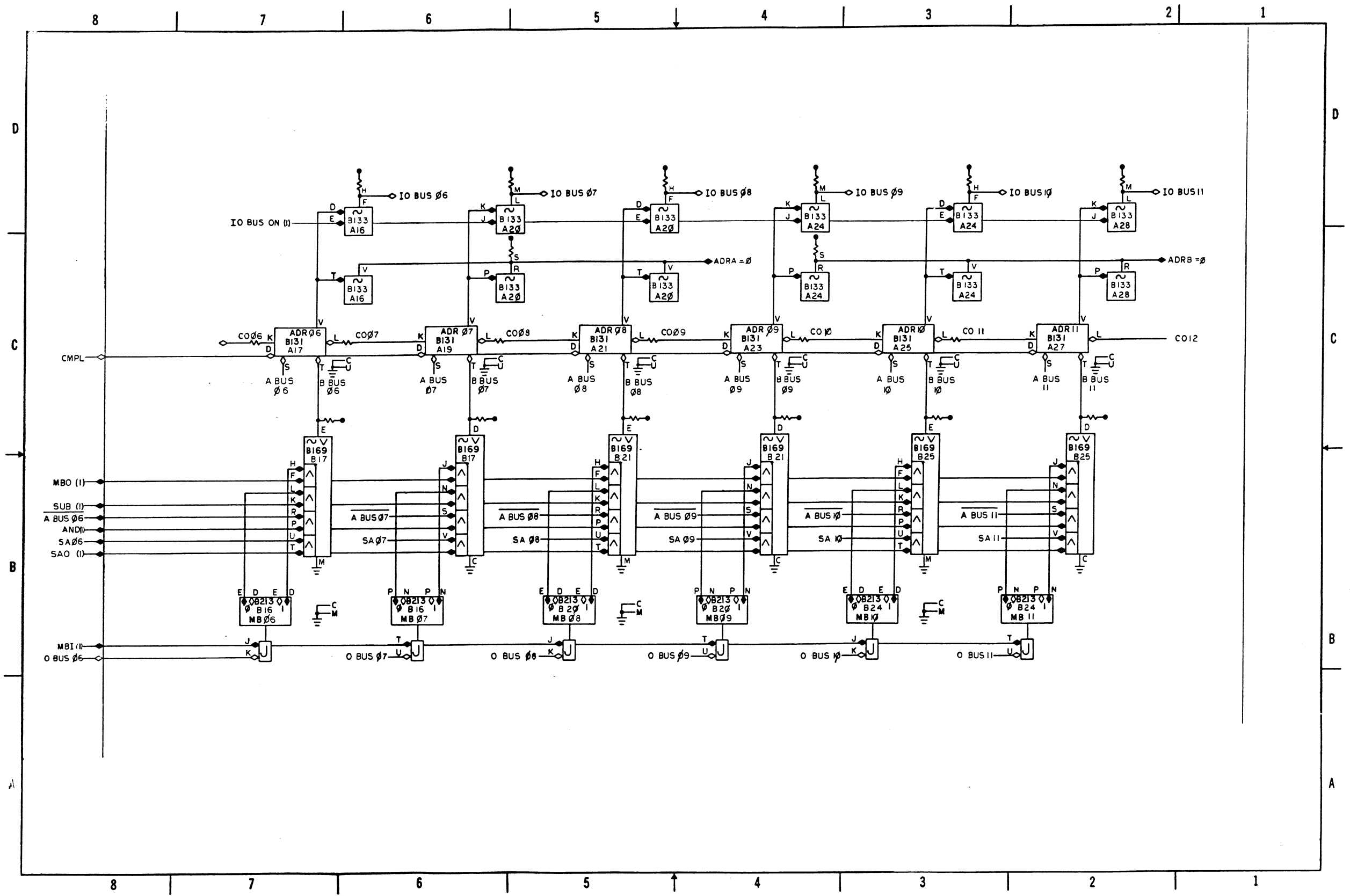
D-BS-KC09-A-20 AC, AR, MQ, PC (Sheet 2)



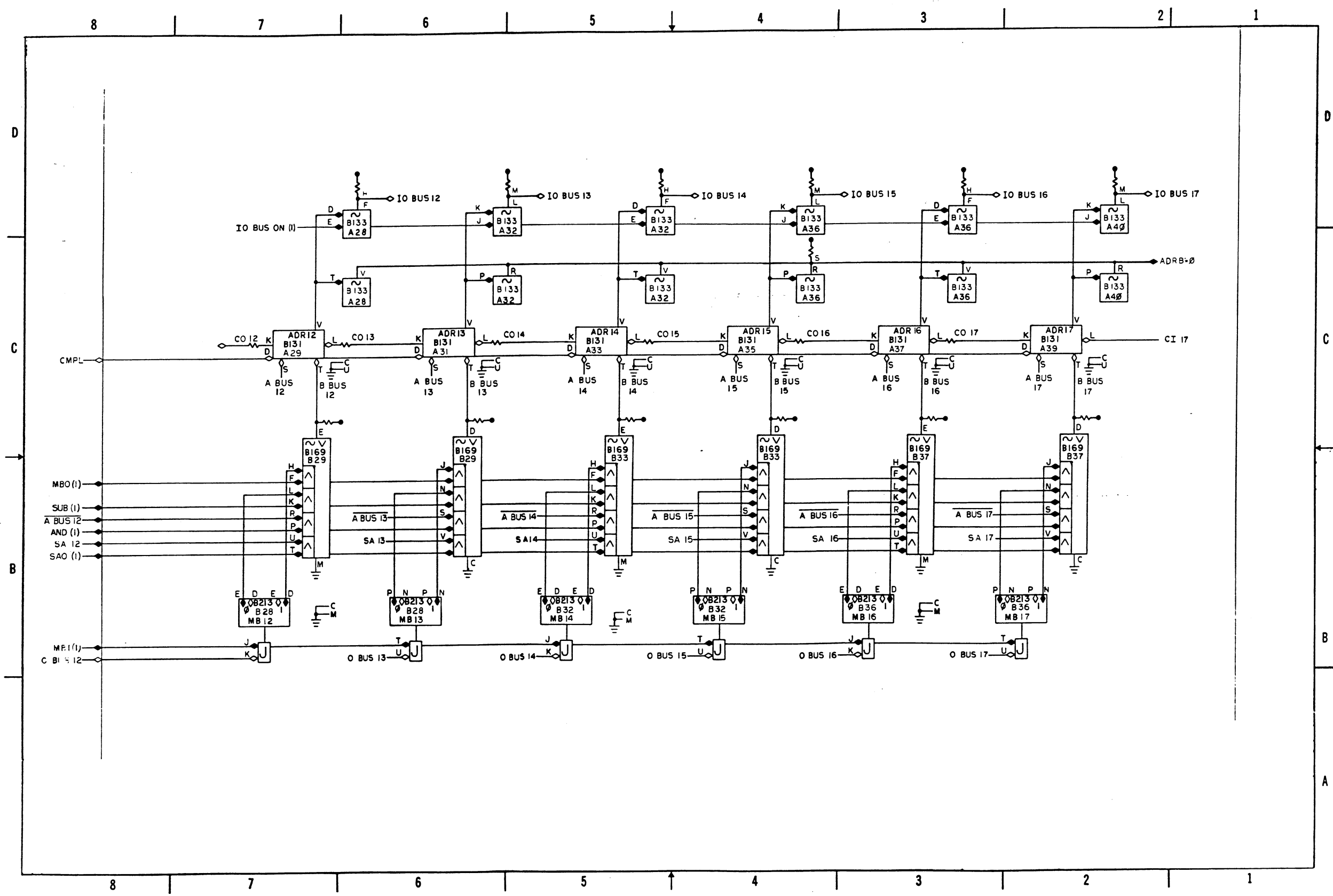
D-BS-KC09-A-20 AC, AR, MQ, PC (Sheet 3)



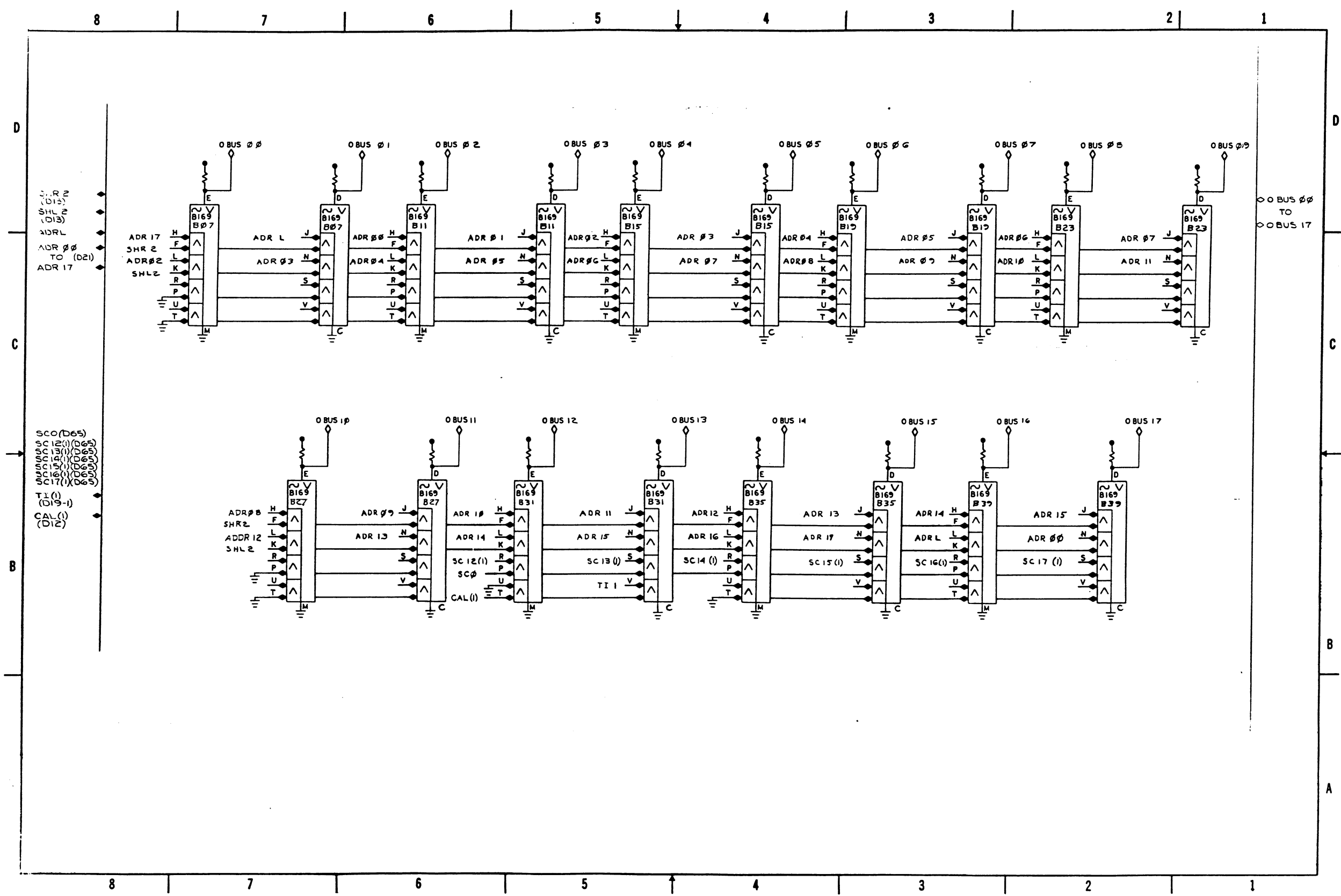
D-BS-KC09-A-21 MB and Adder (Sheet 1)



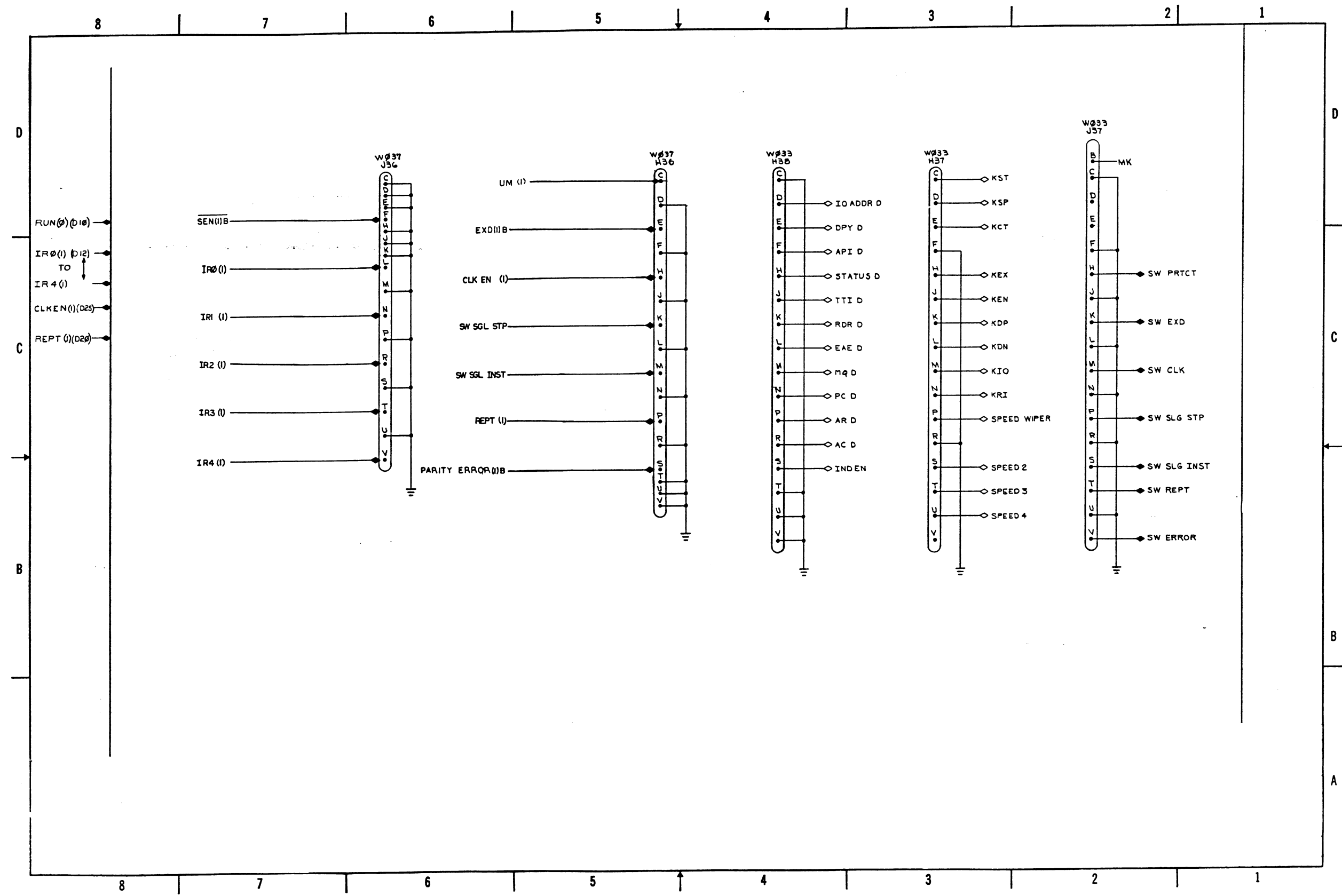
D-BS-KC09-A-21 MB and Adder (Sheet 2)



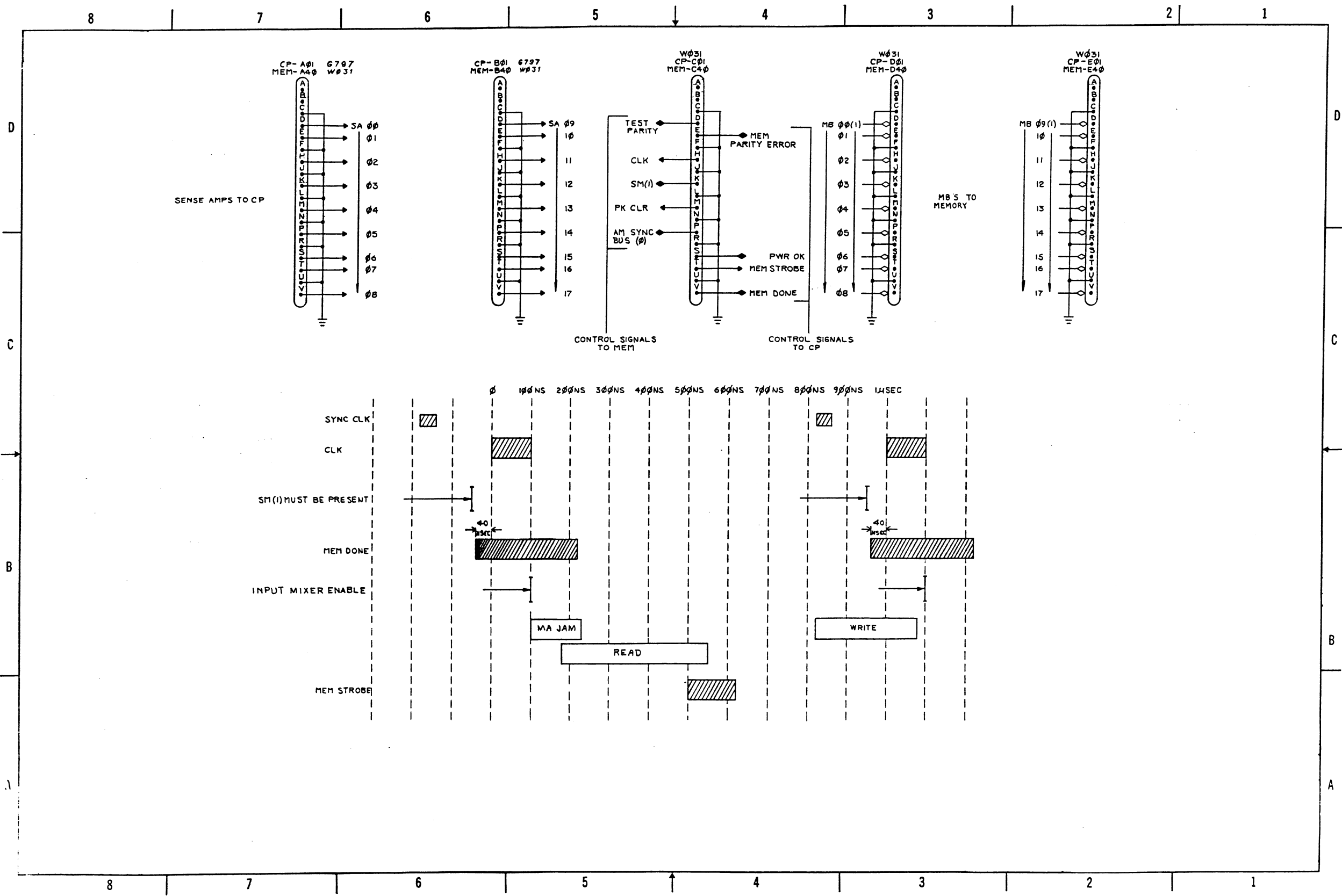
D-BS-KC09-A-21 MB and Adder (Sheet 3)



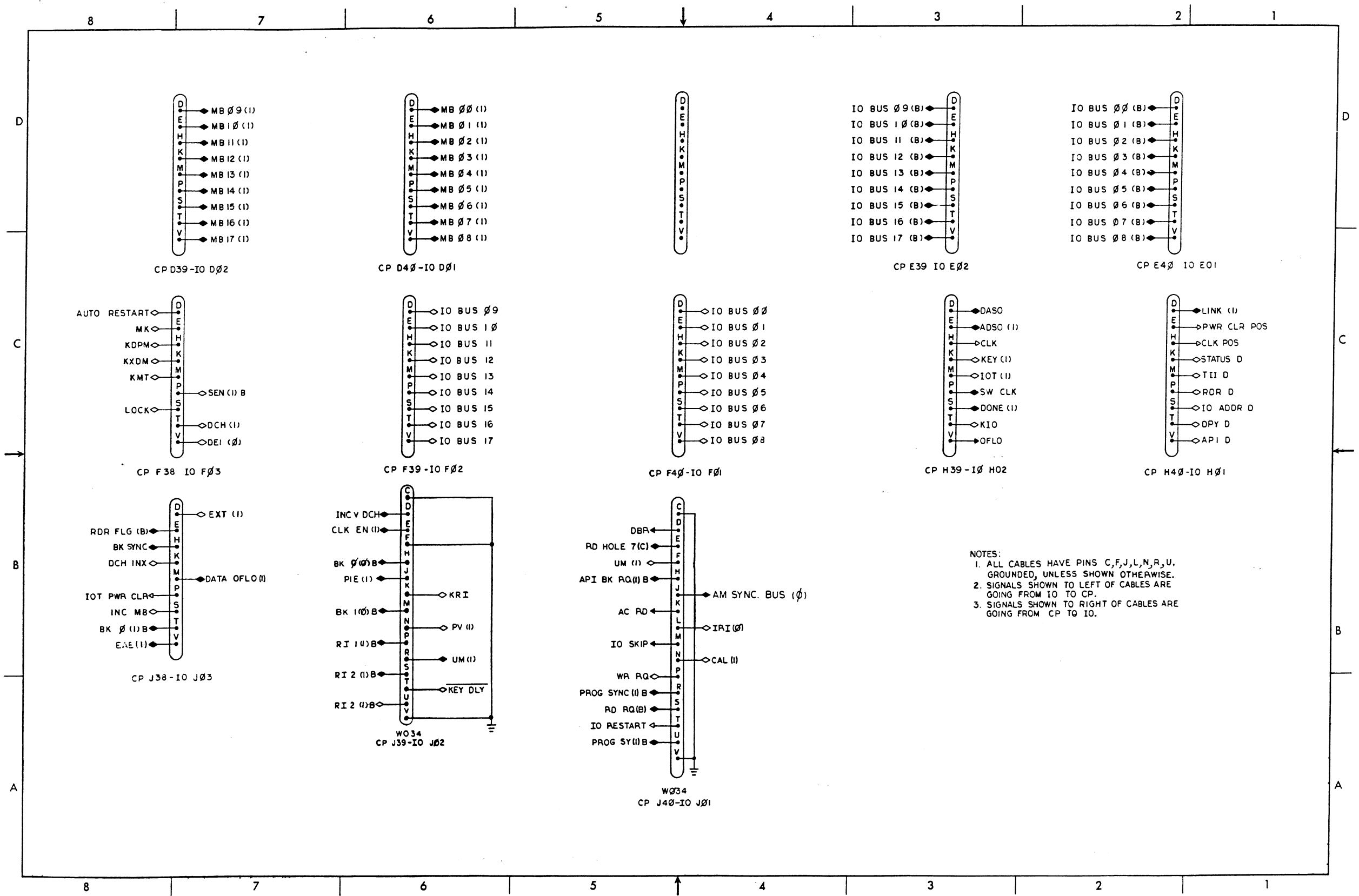
D-BS-KC09-A-22 Shift X2 Gates



D-IC-KC09-A-23 CP/Console Interface

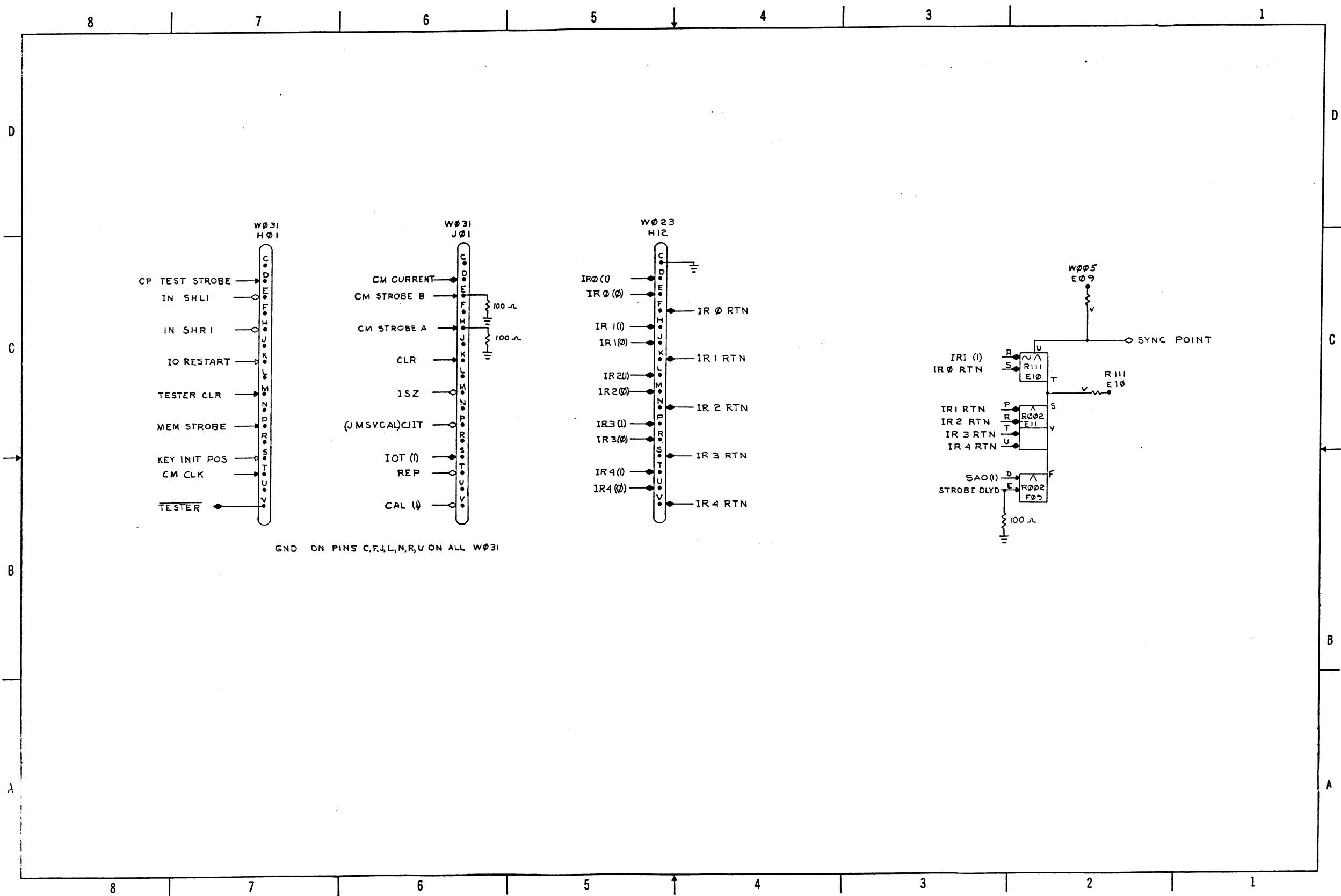


D-IC-KC09-A-24 CP/Memory Interface



NOTES:
 1. ALL CABLES HAVE PINS C,F,J,L,N,R,U,
 GROUNDED, UNLESS SHOWN OTHERWISE.
 2. SIGNALS SHOWN TO LEFT OF CABLES ARE
 GOING FROM IO TO CP.
 3. SIGNALS SHOWN TO RIGHT OF CABLES ARE
 GOING FROM CP TO IO.

D-IC-KC09-A-25 CP/IO Interface



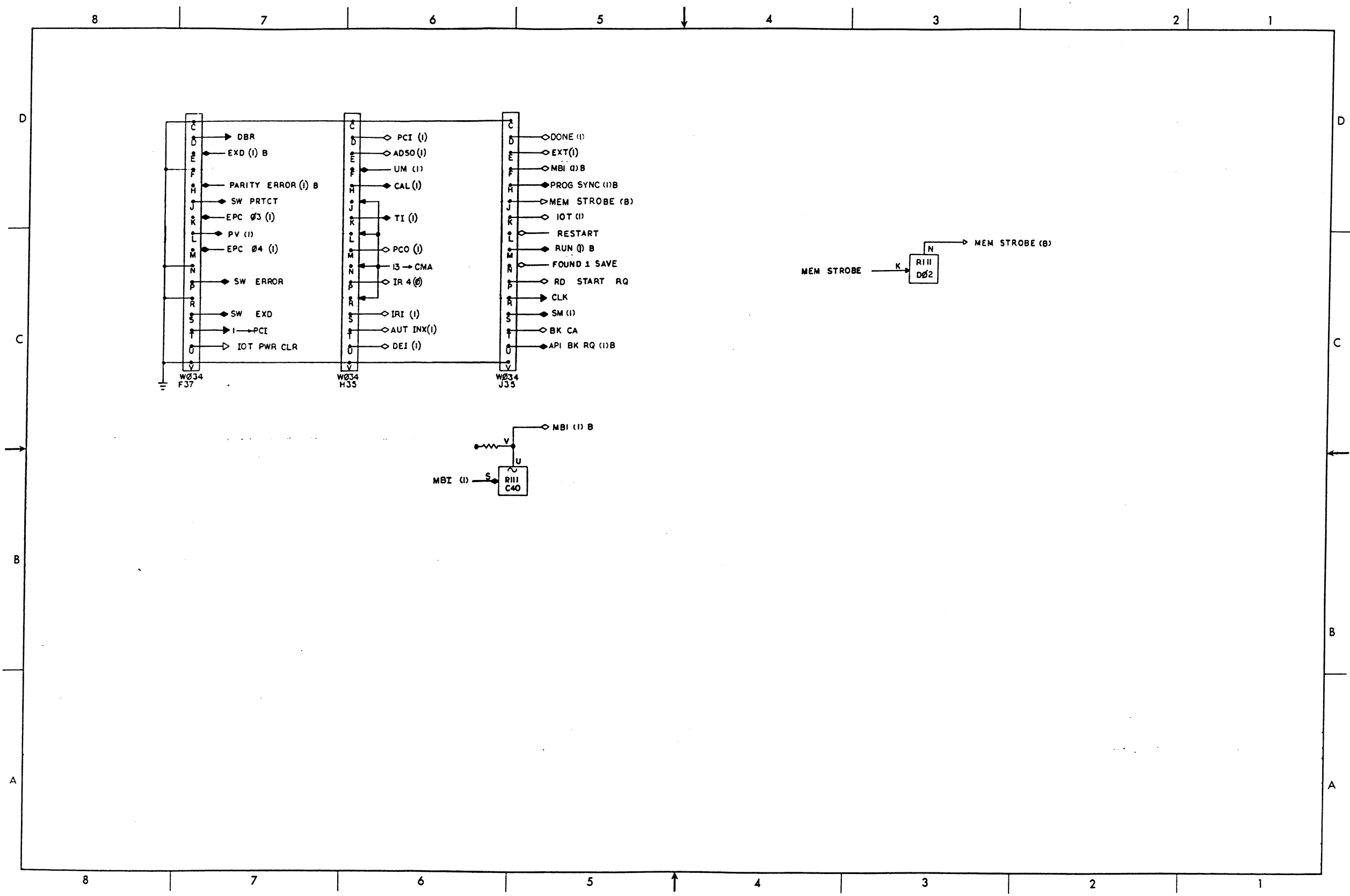
D-BS-KC09-A-26 CP/Tester Interface

COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
* Jumper TEMP I (I) \diamond	Jumper		B03T	B03C	
* Jumper SCO(1)	Jumper		B31P	B31C	
CM Strobe DLYD	100 μ 1/4 W		F11S	F11C	
CM Strobe D	150 Ω 1/4 W		D08H	D08C	
CM Strobe A	100 Ω 1/4 W		D22T	D22C	
CM Strobe B	\updownarrow		D25J	D25C	
CM Strobe C	\updownarrow		D26J	D26C	
\emptyset MBI	100 1/4W		D26R	D27C	
ACT	.001MFD +150 Ω		J12P	J12C	
F30D	100 Ω 1/4 W		E29D	E29C	
CM CLK	100 Ω 1/4 W		E22R	E22C	
CM Strobe D	150 Ω 1/4 W		E33M	E33C	
Strobe DLYD	100 Ω 1/4 W		F09E	F09C	
CP Test Strobe	\updownarrow		F28P	F28C	
F30N	100 Ω 1/4 W		F29M	F29C	
F32D	100 μ 1/4 W		F33D	F33C	
I/O Restart	47 μ +.01 MFD		F34D	F34C	
F36N	.01UF 50V		F36N	F36C	
KDPM	15K Ω 1/4 W		F36L	F36B	
LOCK	15K Ω 1/4 W		F36T	F35B	
MEM Strobe	1K Ω 1/4 W		H01P	H01A	
CM Strobe C	100 Ω 1/4 W		H26T	H26C	
KMT	15 K 1/4 W		H27S	H27B	
CM Strobe B	100 Ω 1/4 W		J01E	J02C	
CM Strobe A	\downarrow		J01H	J01C	
CLR	\downarrow		J01K	H01U	

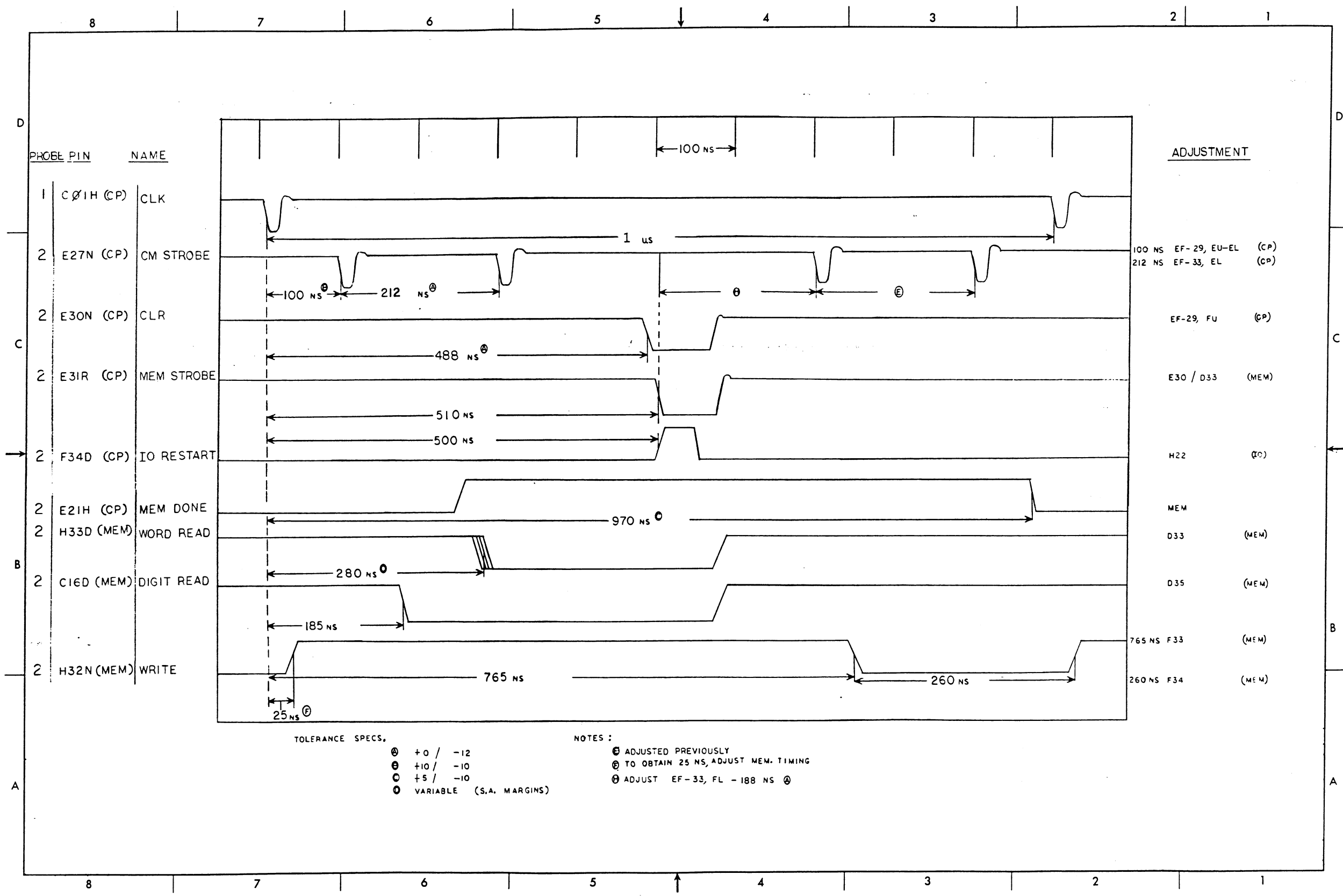
A-CP-KC09-A-27 External Components List (Sheet 1)

COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
Key Delay's	50 MFD 50V	-	J32R	J32S	+
Key Delay's	.047 MFD 100V	-	J32H	J32J	+
J34V	.01 MFD 50V		J34V	J34C	
KXDM	15 K Ω 1/4 W		J34H	J34B	
1 \rightarrow PCI	100 Ω 1/4 W		D21S	D21C	
*JUMPER ADRL (B)	JUMPER		B03D	B03N	
*AC0 \rightarrow LINK	15K Ω 1/4 W		E04R	E04B	
SPEED WIPER	4700pf		J24T	J24C	
MEM STROBE	150 Ω 1/4 W		E31R	E31C	
SCOV (I)	750 Ω 1/4 W		H06P	H06B	
**EXD (1) B \blacklozenge	JUMPER		F37E	F36C	
**EPC03 (1) \blacklozenge	JUMPER		F37K	F37C	
**EPC04 (1) \blacklozenge	JUMPER		F37M	F38C	
E32N	100 Ω 1/4 W		D24H	D24C	
* F05T	JUMPER		E05T	F05C	
***API BK RQ	JUMPER		F22R	F22C	
EAE-P- PULSE	100 Ω 1/4 W		F02J	F02C	
E23N	100 Ω 1/4 W		C04J	C04C	
*** Jumpers removed when API is installed					
* Jumpers Removed when EAE Modules are installed					
** Jumpers Removed when KG09A Mem Ext Control Is Installed					
MEM DONE	1.5K 1/4W		C01V	C02B	
			E15S	E15B	
			E15T	E16B	
			E21H	E21B	
MEM DONE	1.5K 1/4W		F31S	F31B	

A-CP-KC09-A-27 External Components List (Sheet 2)



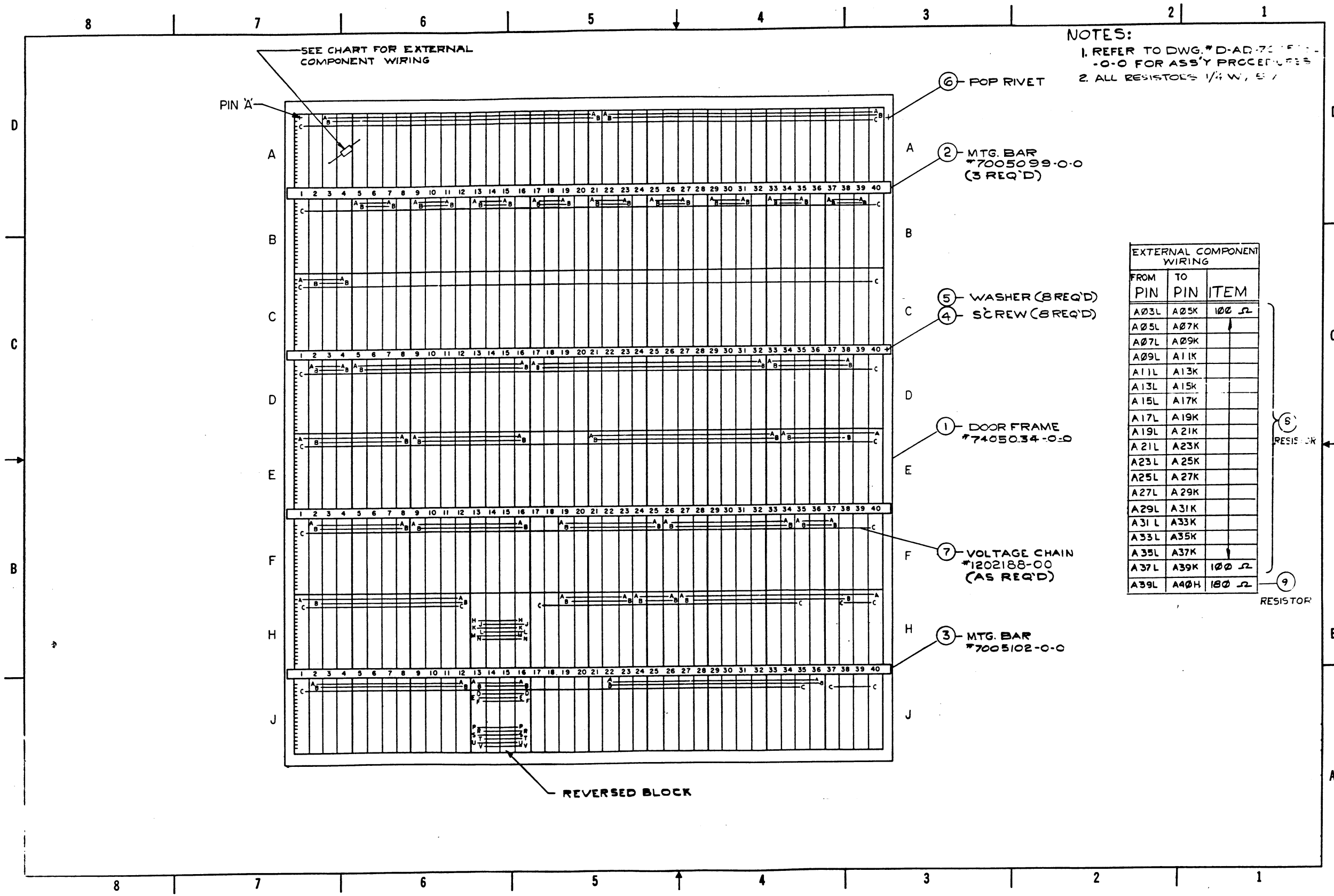
D-CD-KC09-A-28 CP Memory Extension/Parity Interface



TOLERANCE SPECS.
 ⓐ +0 / -12
 ⓑ +10 / -10
 ⓒ +5 / -10
 ⓓ VARIABLE (S.A. MARGINS)

NOTES:
 ⓐ ADJUSTED PREVIOUSLY
 ⓑ TO OBTAIN 25 NS, ADJUST MEM. TIMING
 ⓒ ADJUST EF-33, FL - 188 NS ⓐ

D-TD-KC09-A-29 System Timing



SEE CHART FOR EXTERNAL COMPONENT WIRING

NOTES:
 1. REFER TO DWG. #D-AD-705303-0-0 FOR ASSY PROCEDURES
 2. ALL RESISTORS 1/4 W, 5%

⑥ POP RIVET

② MTG. BAR
 #7005099-0-0
 (3 REQ'D)

⑤ WASHER (8 REQ'D)

④ SCREW (8 REQ'D)

① DOOR FRAME
 #7405034-0-0

⑦ VOLTAGE CHAIN
 #1202188-00
 (AS REQ'D)

③ MTG. BAR
 #7005102-0-0

EXTERNAL COMPONENT WIRING		
FROM PIN	TO PIN	ITEM
A03L	A05K	100 Ω
A05L	A07K	↑
A07L	A09K	
A09L	A11K	
A11L	A13K	
A13L	A15K	
A15L	A17K	
A17L	A19K	
A19L	A21K	
A21L	A23K	
A23L	A25K	
A25L	A27K	
A27L	A29K	
A29L	A31K	
A31L	A33K	
A33L	A35K	
A35L	A37K	↑
A37L	A39K	100 Ω
A39L	A40H	100 Ω

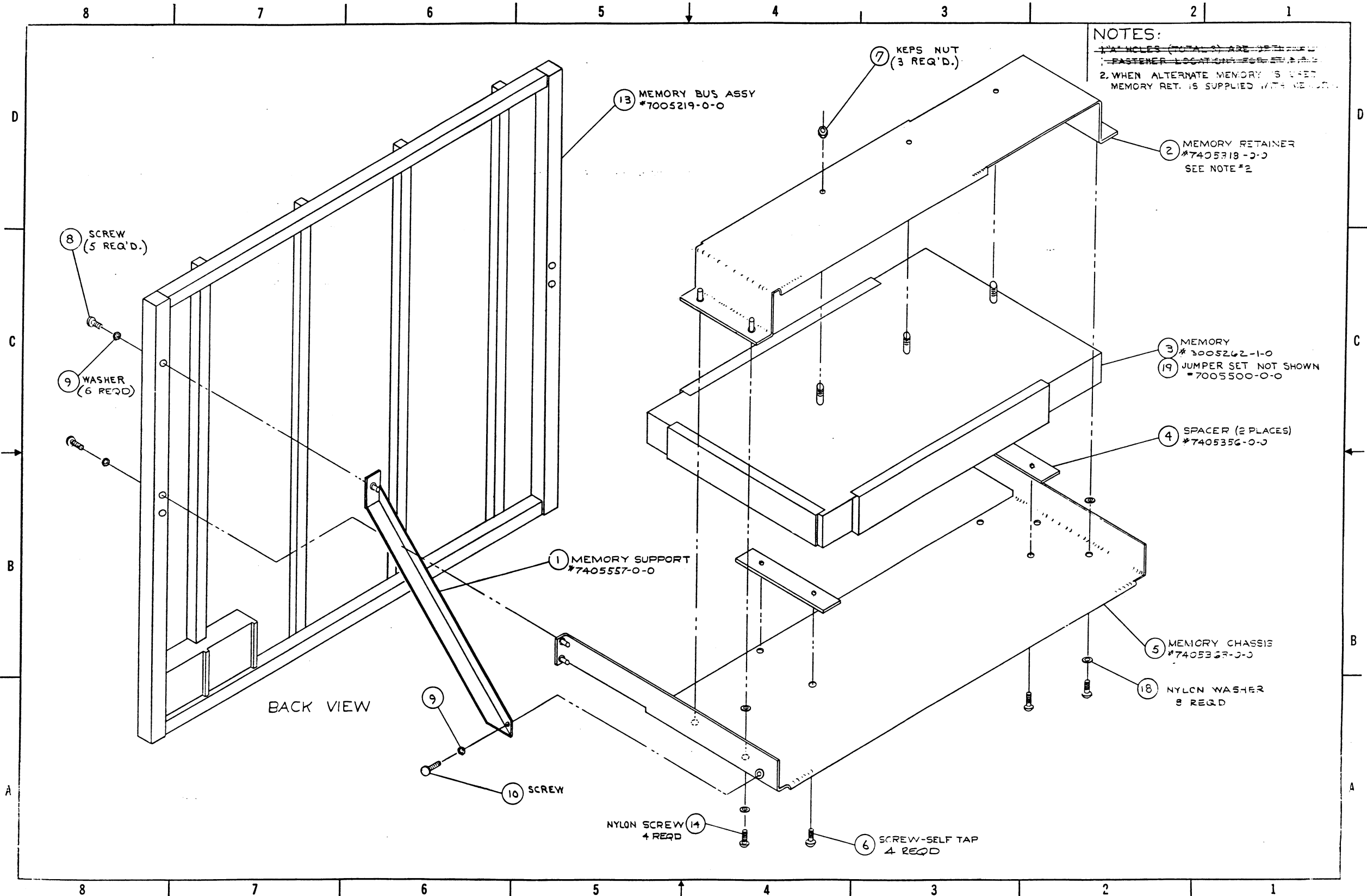
⑤ RESISTOR
 ⑨ RESISTOR

REVERSED BLOCK

D-AD-7005303-0-0 CP Bus Assembly

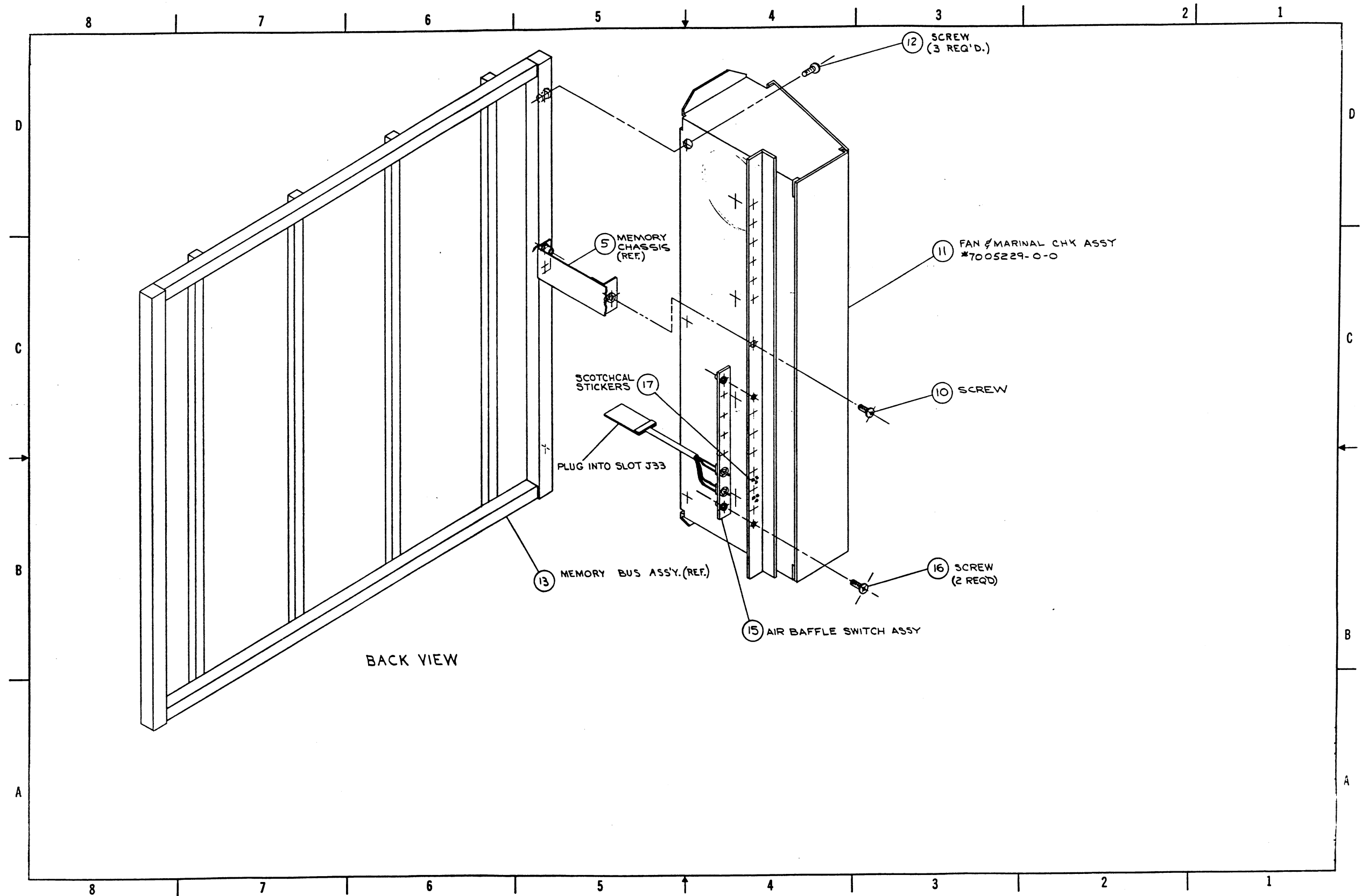
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION		DEC. STOCK NO.
			ITEM	— STOCK SIZE — CAT. NO. — MFG.	
1	E-IA-7405034-0-0	1		DOOR FRAME (MTG BAR)	
2	D-AD-7005099-0-0	3		MTG BAR ASSY (CONN BLOCKS)	
3	D-AD-7005102-0-0	1		MTG BAR ASSY (ONE REVERSE BLK)	
4		8		SCREW PHL PAN HD #8-32 x L. 1/4 SST	
5		8		WASHER LOCK INT TOOTH #8 SST	
6		1		POP RIVET 1/8 DIA x 3/16 LG.	
7		AR		VOLT-CHAIN-PURCH SPEC-CHV 0001	12-3584-032
8		18		RESISTOR-CARB 100 OHM 1/4W 5%	
9		1		RESISTOR-CARB 180 OHM 1/4W 5%	

A-PL-7005303-0-0 CP Bus Assembly

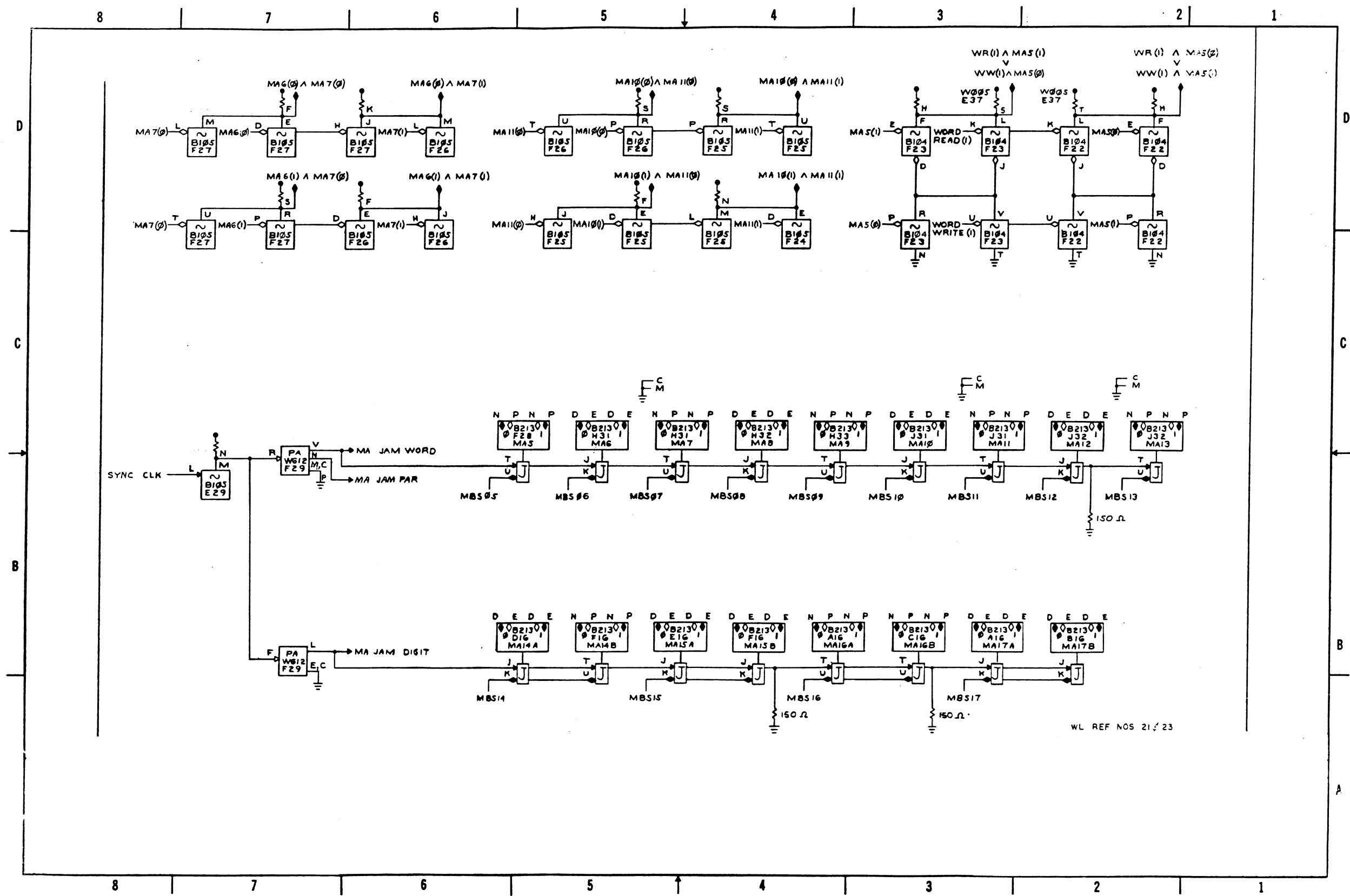


NOTES:
 1. ALL HOLES (TOTAL 3) ARE SPACED TO FASTENER LOCATION SEE DRAWING
 2. WHEN ALTERNATE MEMORY IS USED MEMORY RET. IS SUPPLIED WITH MEMORY.

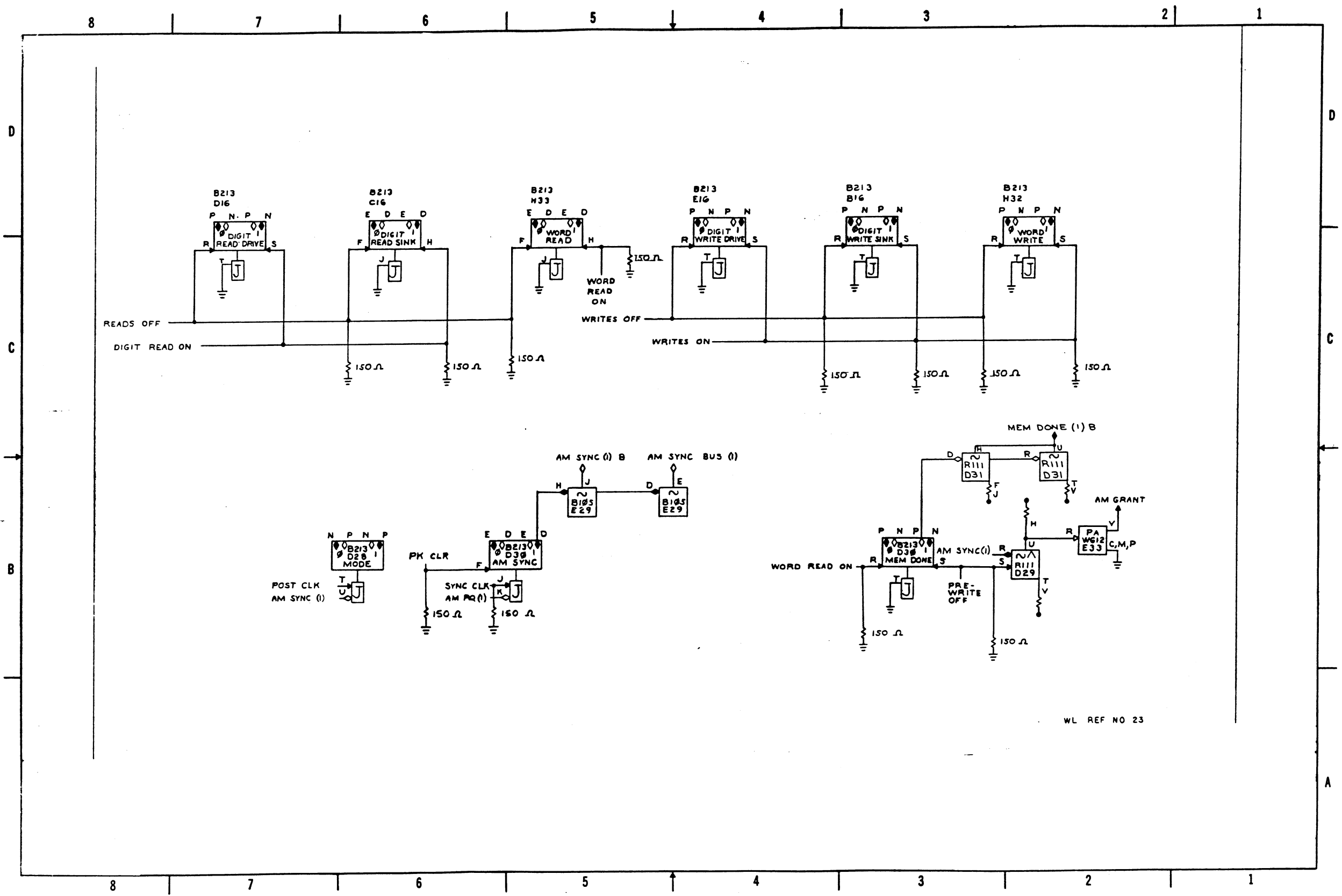
D-UA-MC70-B-0 Unit Assembly (Sheet 1)



D-UA-MC70-B-0 Unit Assembly (Sheet 2)

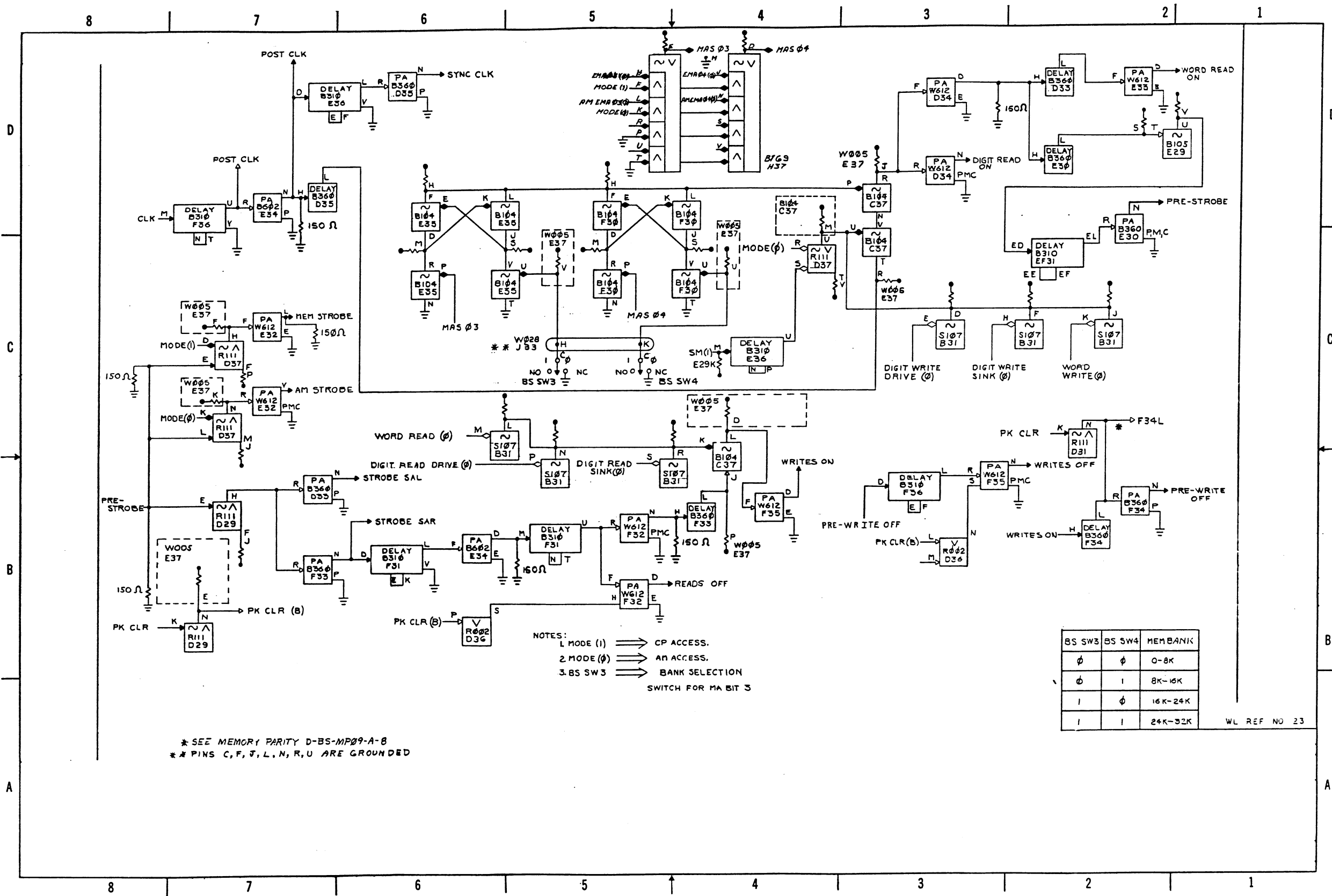


D-BS-MC70-B-1 Memory Control (Sheet 1)



WL REF NO 23

D-BS-MC70-B-1 Memory Control (Sheet 2)



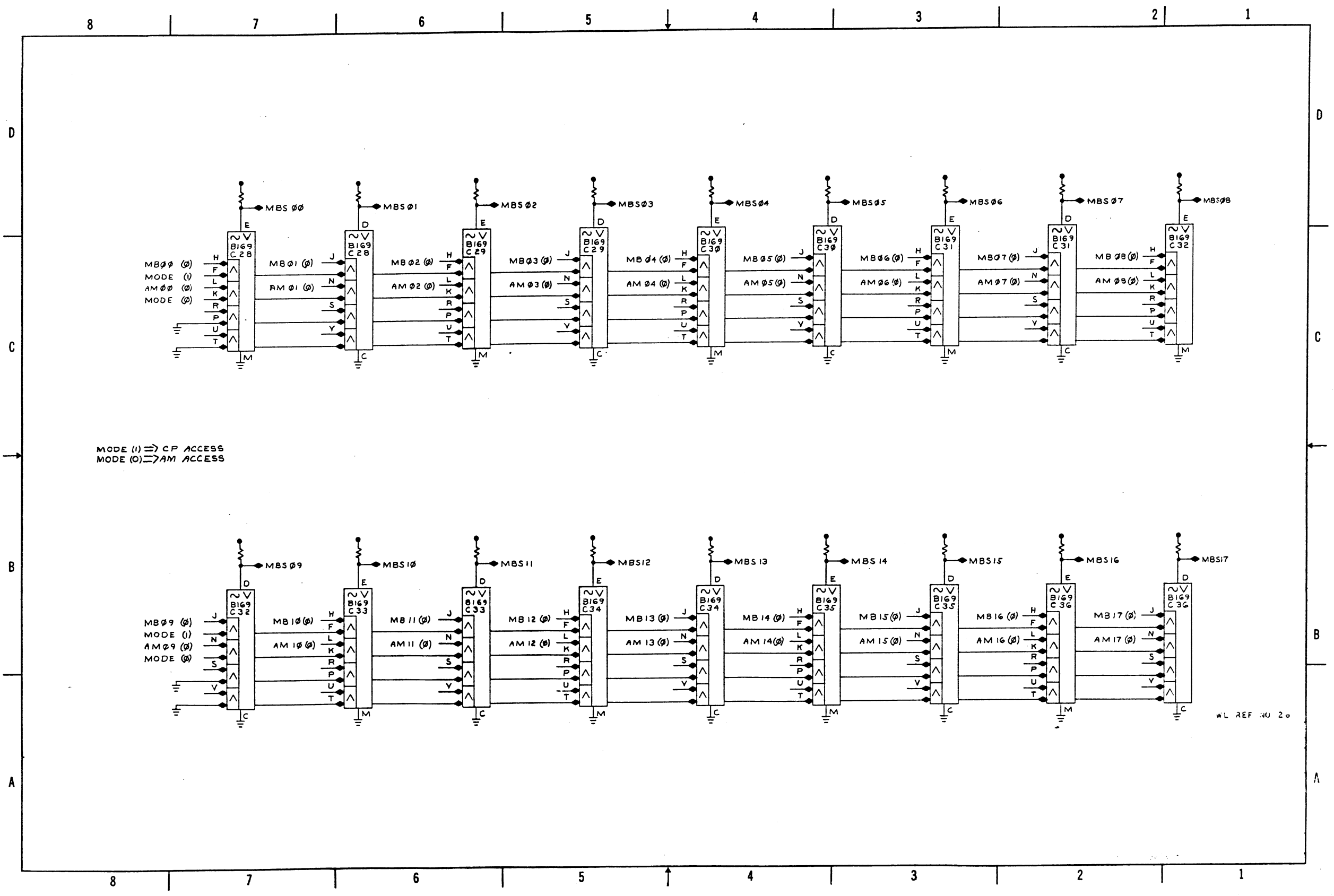
NOTES:
 1. MODE (1) → CP ACCESS.
 2. MODE (φ) → AM ACCESS.
 3. BS SW 3 → BANK SELECTION
 SWITCH FOR MA BIT 3

BS SW3	BS SW4	MEMBANK
φ	φ	0-8K
φ	1	8K-16K
1	φ	16K-24K
1	1	24K-32K

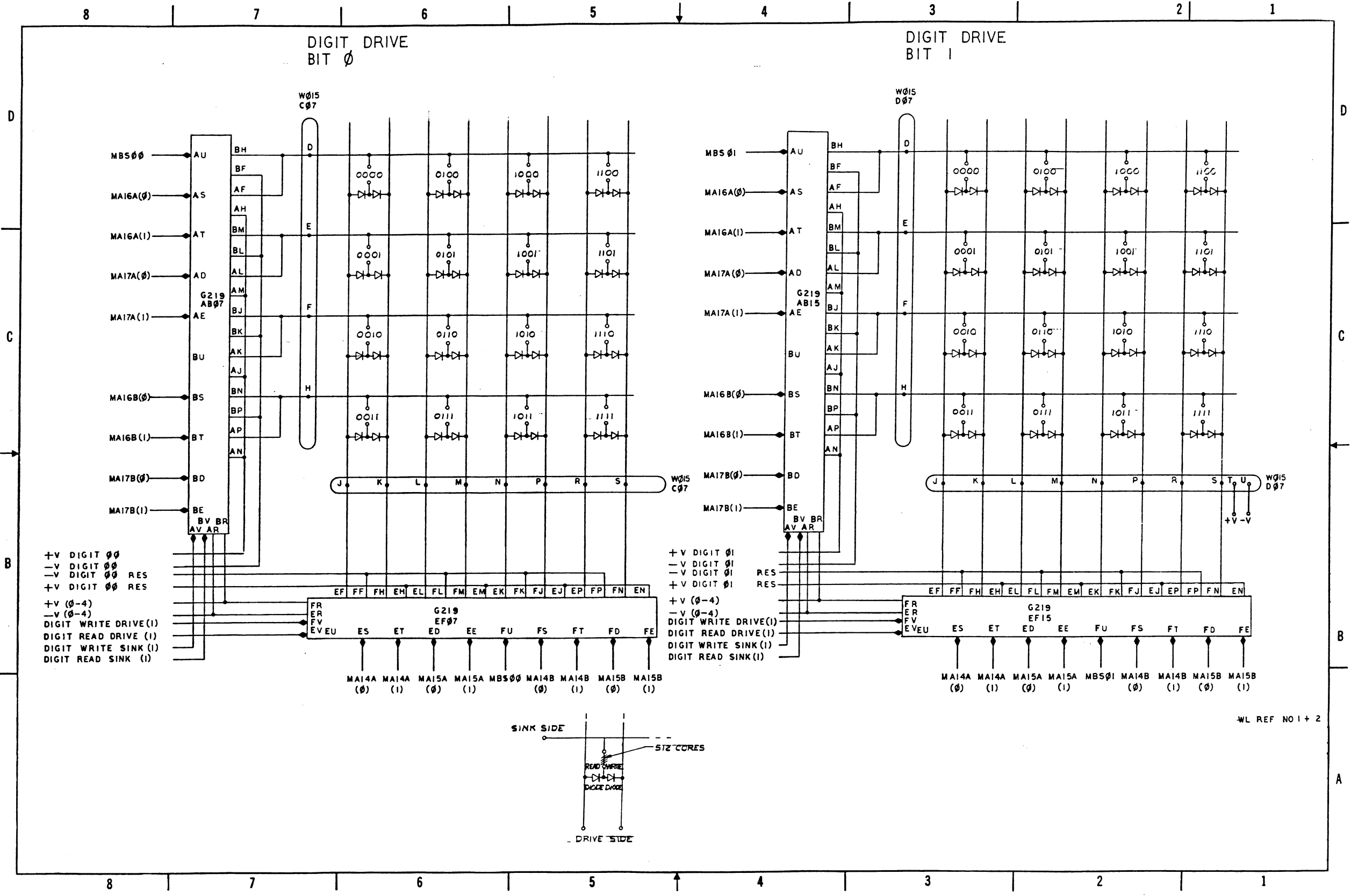
* SEE MEMORY PARITY D-BS-MP09-A-B
 ** PINS C, F, J, L, N, R, U ARE GROUNDED

WL REF NO 23

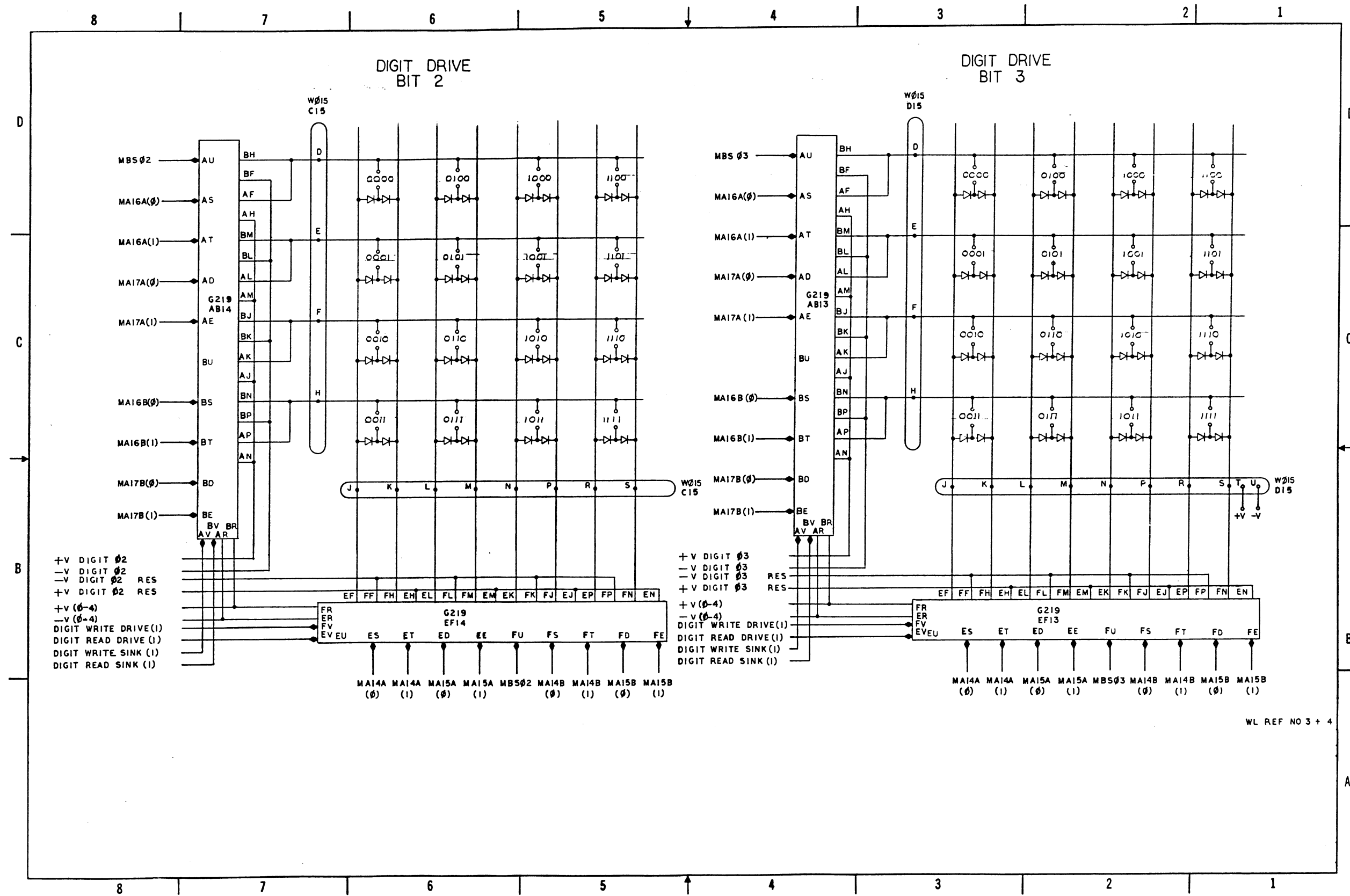
D-BS-MC70-B-2 Memory Timing Chain



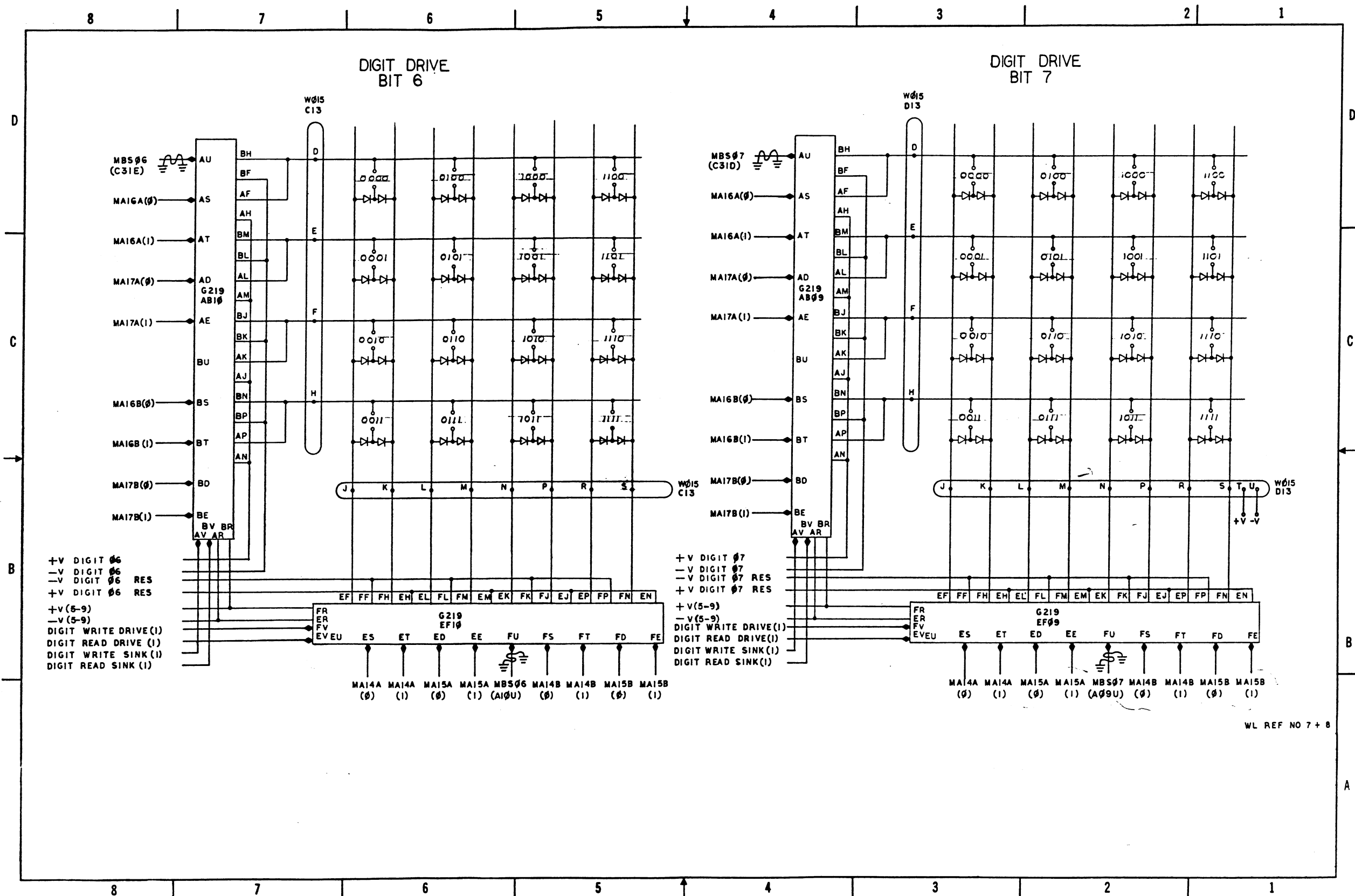
D-BS-MC70-B-3 Memory Input Mixer



D-BS-MC70-B-4 Digit Drive Bits 0-17 (Sheet 1)



D-BS-MC70-B-4 Digit Drive Bits 0-17 (Sheet 2)

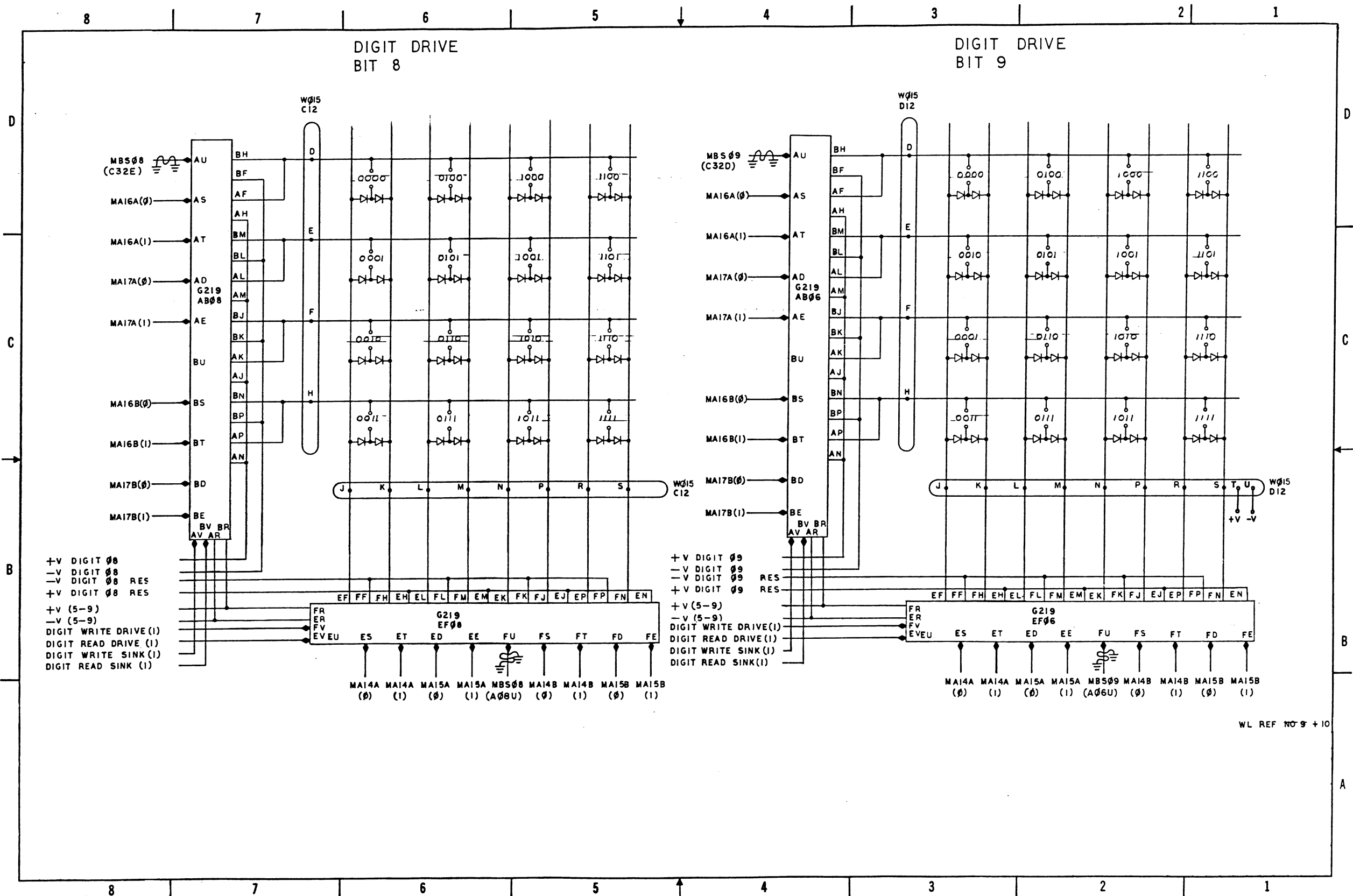


+V DIGIT 06
 -V DIGIT 06
 -V DIGIT 06 RES
 +V DIGIT 06 RES
 +V(5-9)
 -V(5-9)
 DIGIT WRITE DRIVE(I)
 DIGIT READ DRIVE(I)
 DIGIT WRITE SINK(I)
 DIGIT READ SINK(I)

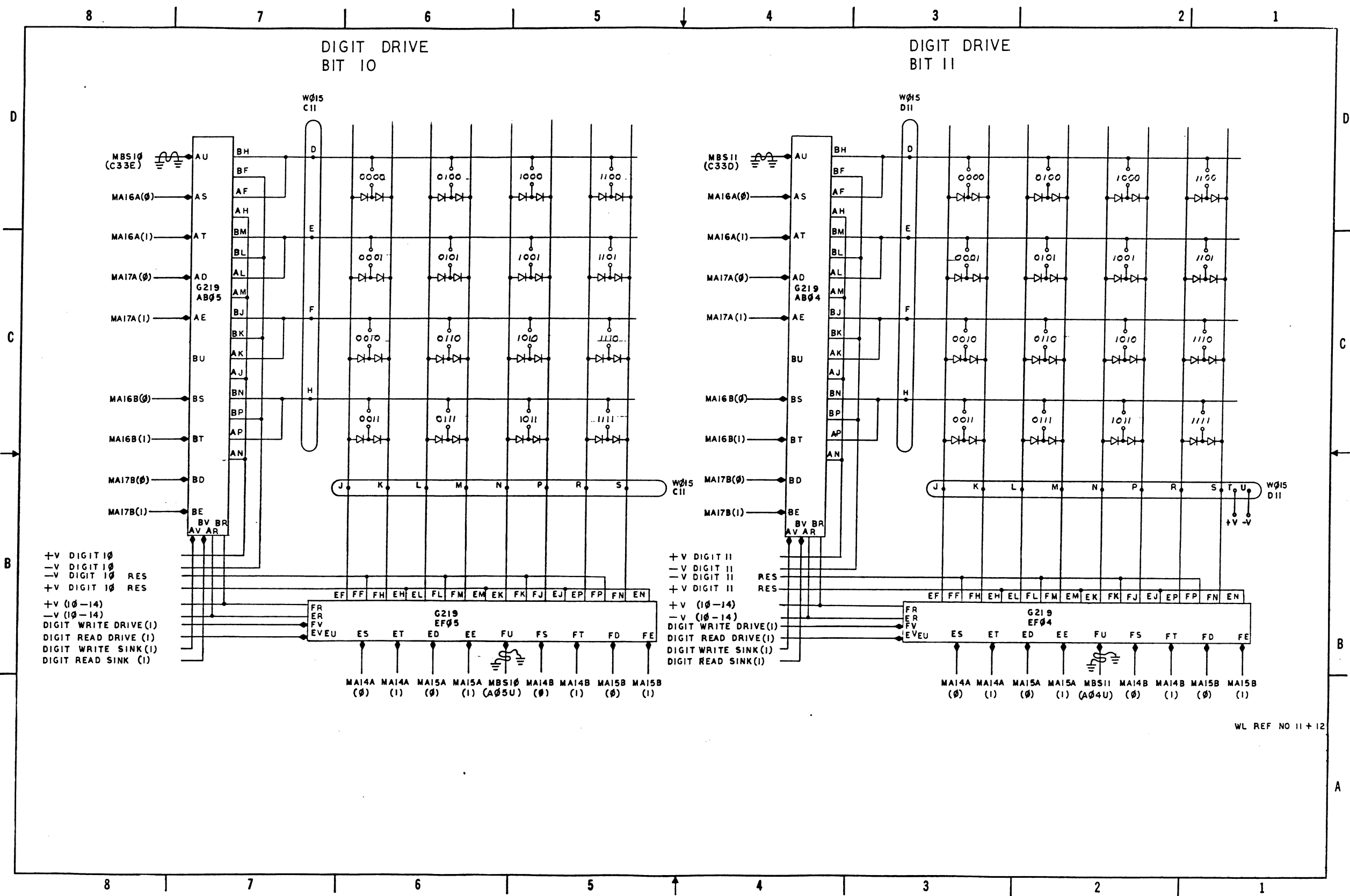
+V DIGIT 07
 -V DIGIT 07
 -V DIGIT 07 RES
 +V DIGIT 07 RES
 +V(5-9)
 -V(5-9)
 DIGIT WRITE DRIVE(I)
 DIGIT READ DRIVE(I)
 DIGIT WRITE SINK(I)
 DIGIT READ SINK(I)

WL REF NO 7 + 8

D-BS-MC70-B-4 Digit Drive Bits 0-17 (Sheet 4)

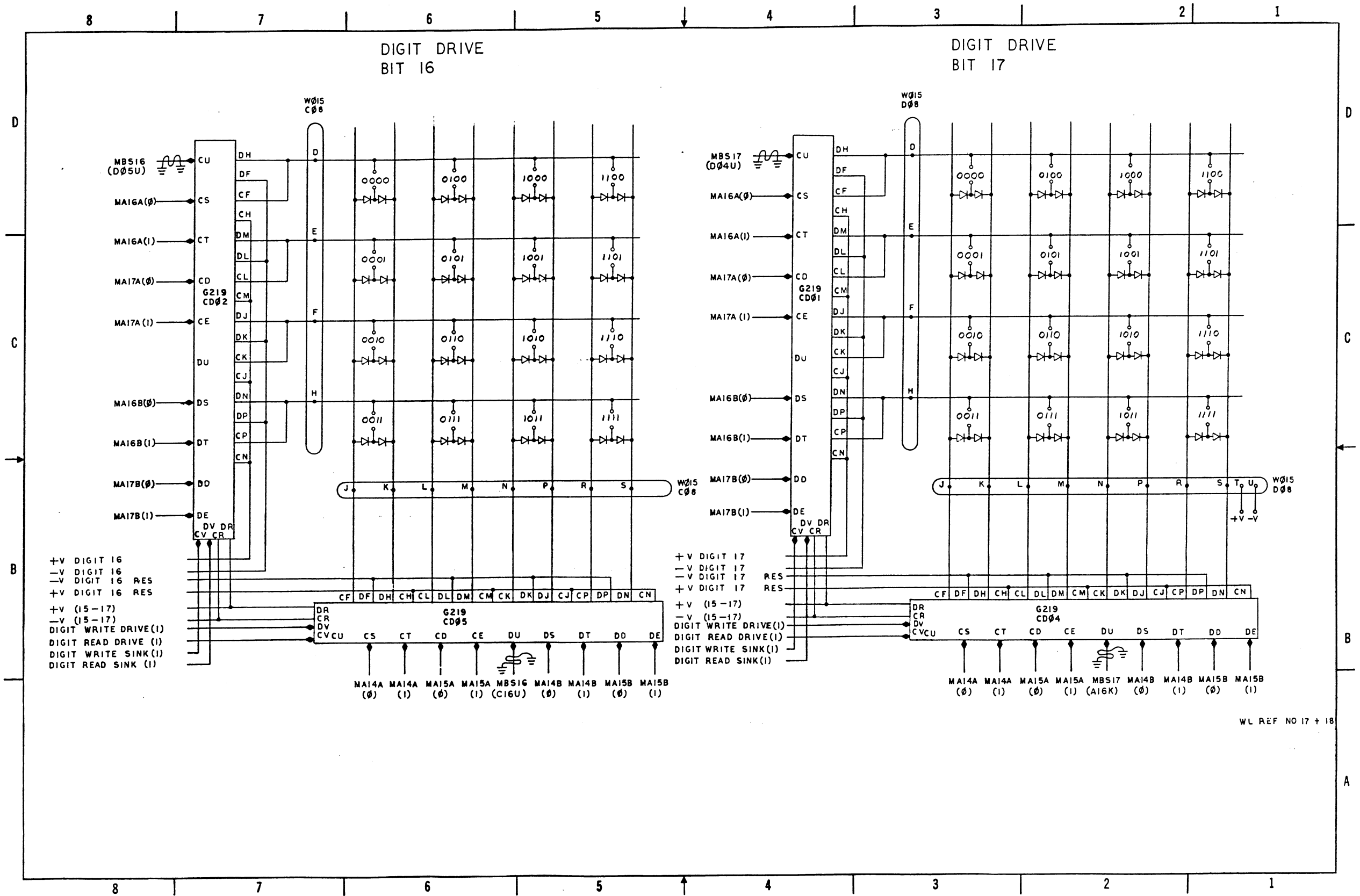


D-BS-MC70-B-4 Digit Drive Bits 0-17 (Sheet 5)

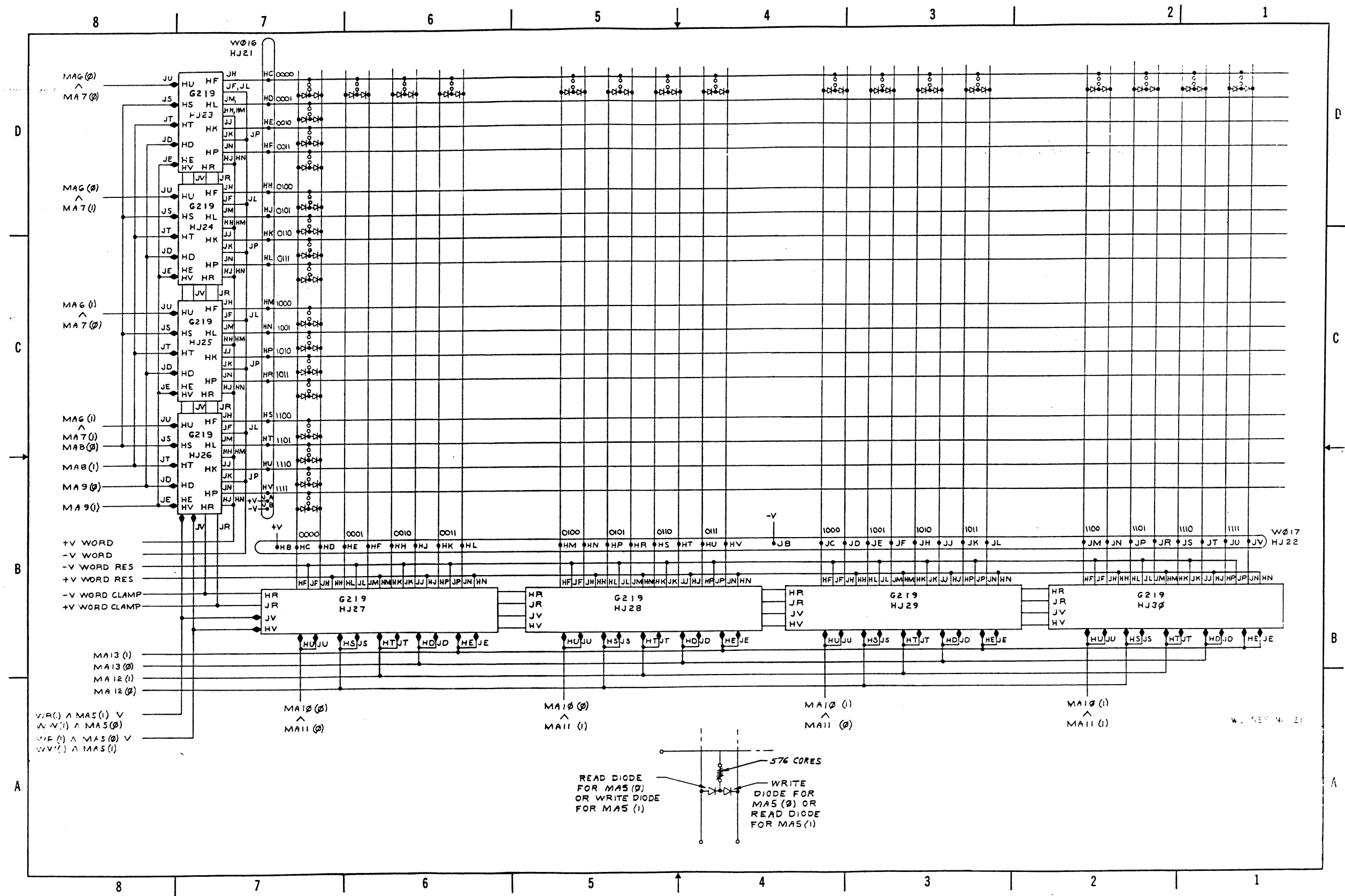


D-BS-MC70-B-4 Digit Drive Bits 0-17 (Sheet 6)

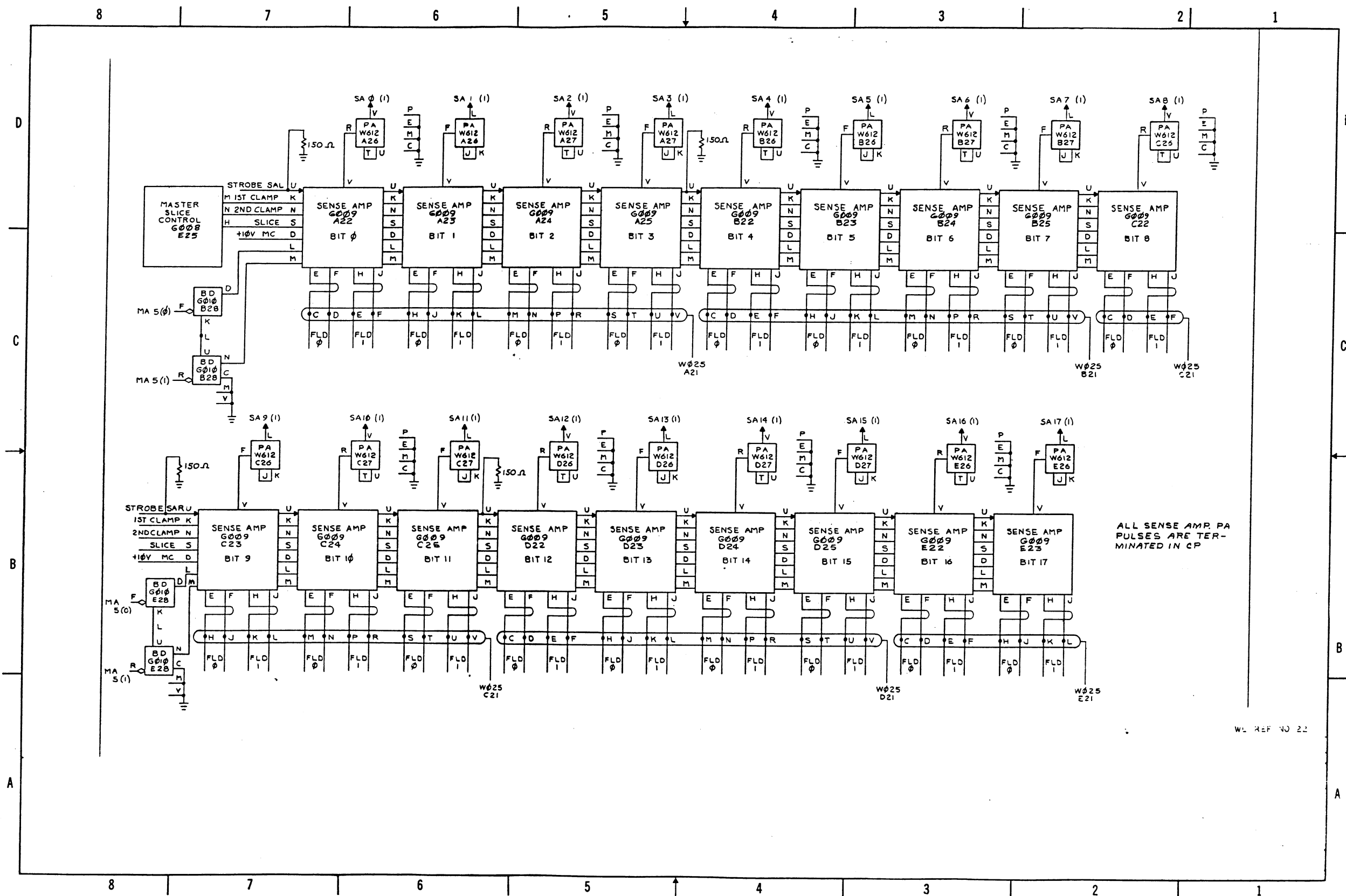
WL REF NO 11 + 12



D-BS-MC70-B-4 Digit Drive Bits 0-17 (Sheet 9)

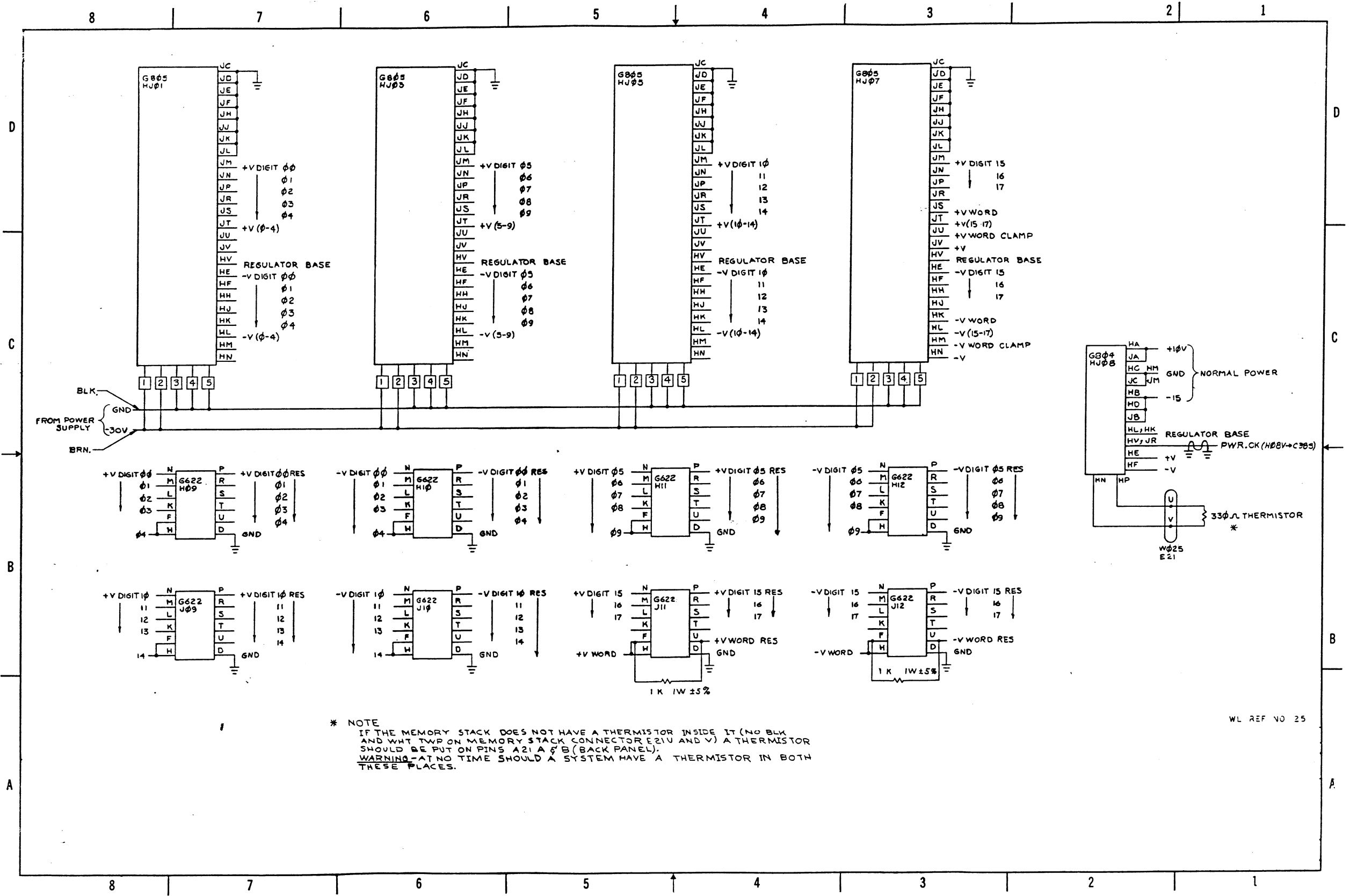


D-BS-MC70-B-5 Word Selection



D-BS-MC70-B-6 Sense Amplifiers

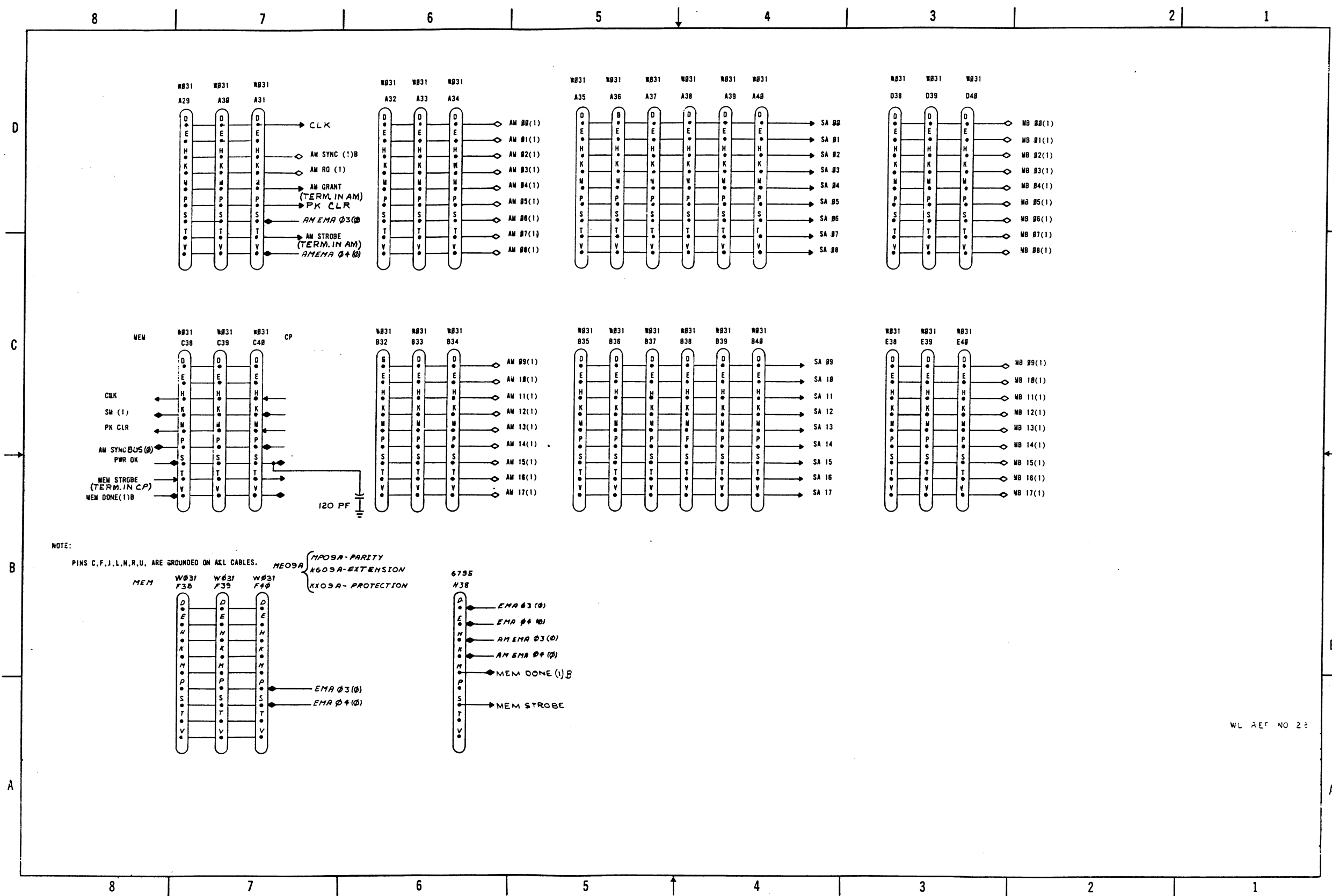
WL REF NO 22



* NOTE
 IF THE MEMORY STACK DOES NOT HAVE A THERMISTOR INSIDE IT (NO BLK AND WHT TWP ON MEMORY STACK CONNECTOR E21U AND V) A THERMISTOR SHOULD BE PUT ON PINS A21 A & B (BACK PANEL).
 WARNING - AT NO TIME SHOULD A SYSTEM HAVE A THERMISTOR IN BOTH THESE PLACES.

WL REF NO 25

D-BS-MC70-B-7 Memory Power



NOTE:

PINS C, F, J, L, N, R, U, ARE GROUNDED ON AXL CABLES.

MEMO9A {
 MPO9A-PARITY
 K609A-EXTENSION
 KX09A-PROTECTION

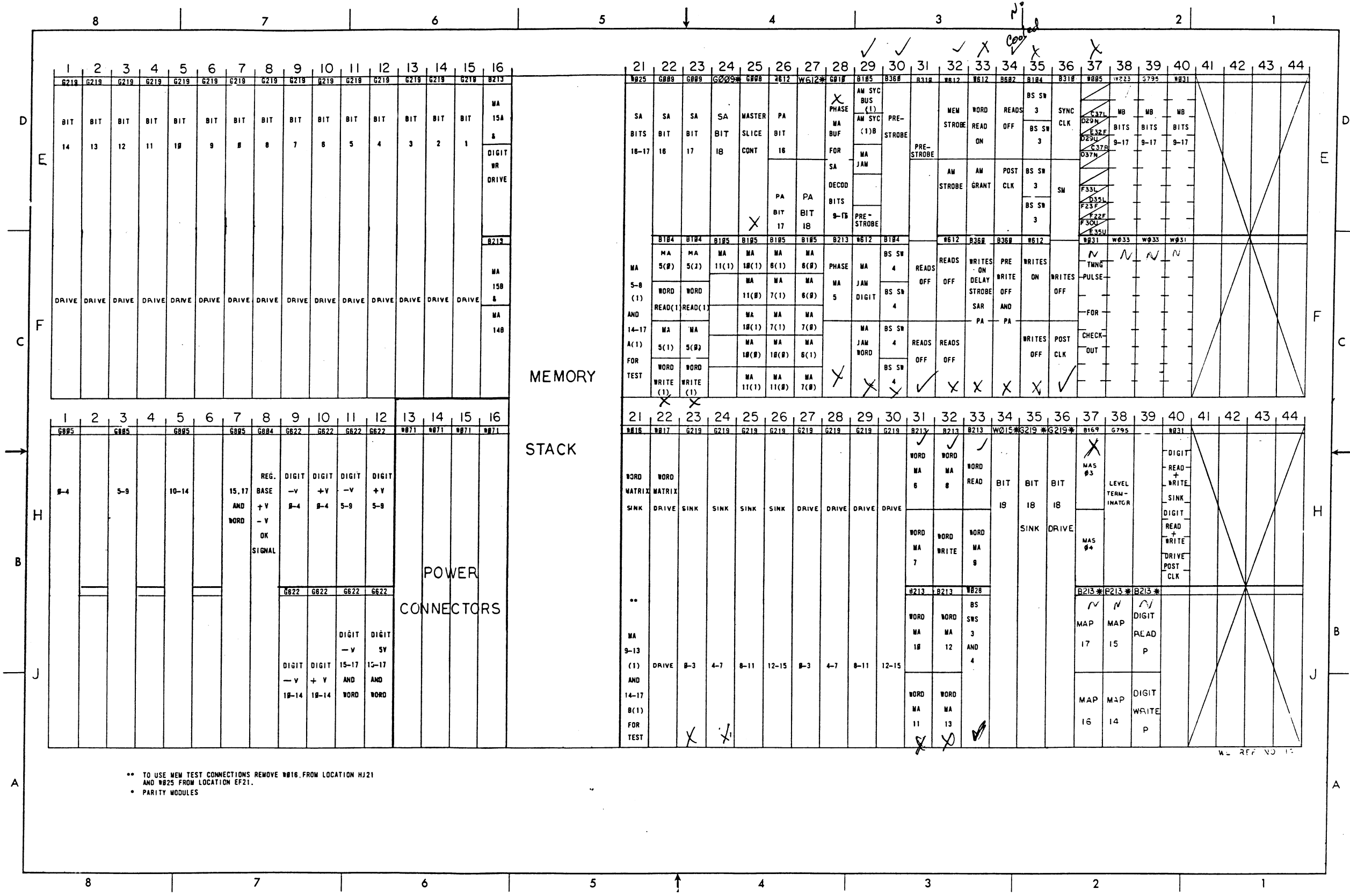
WL REF NO 23

D-BS-MC70-B-8 Mem/AM Cable Connections



*** THE G795 LEVEL TERMINATORS ARE PLACED IN A33 + E33 WHEN THE DM09 A OPTION IS USED

D-BS-MC70-B-9 Module Utilization (Sheet 1)



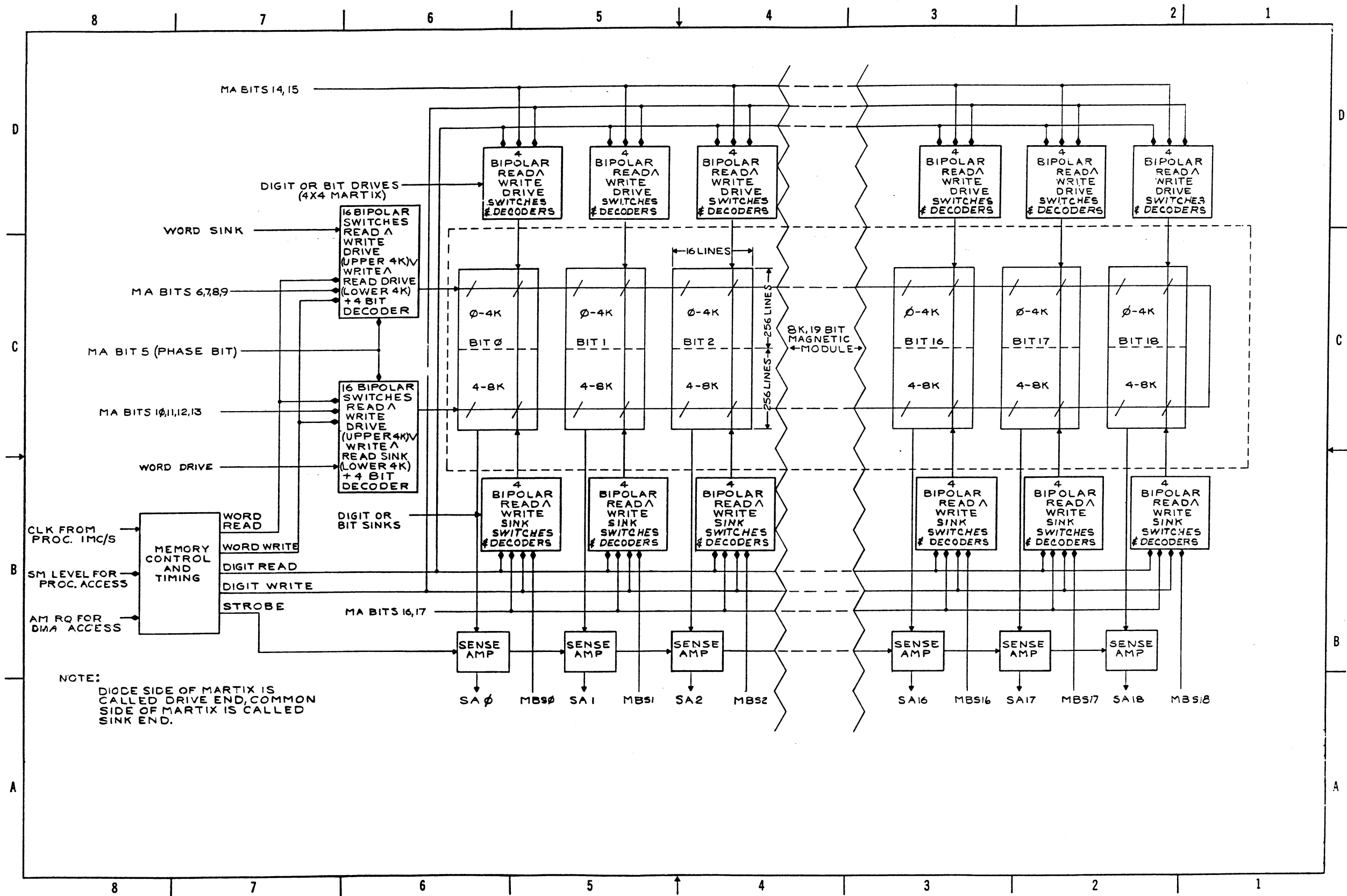
D-BS-MC70-B-9 Module Utilization (Sheet 2)

PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION			DEC. STOCK NO.
			ITEM	STOCK SIZE	CAT. NO. — MFG.	
		5	B104		INVERTER	
		5	B105		INVERTER	
		9	B169		INVERTER	
		14	B213		FLIP FLOP	
		2	B310		DELAY	
		5	B360		DELAY WITH PULSE AMPLIFIER	
		1	B602		PULSE AMPLIFIER	
		1	G008		MASTER SLICE CONTROL	
		18	G009		2 INPUT SENSE AMPLIFIER	
		2	G010		SENSE AMPLIFIER SELECTOR	
		44	G219		MEMORY SELECTOR	
		8	G622		RESISTOR BOARD	
		1	G804		CONTROL FOR G805	
		4	G805		REGULATOR	
		1	R002		DIODE NETWORK	
		2	R111		DIODE GATE	

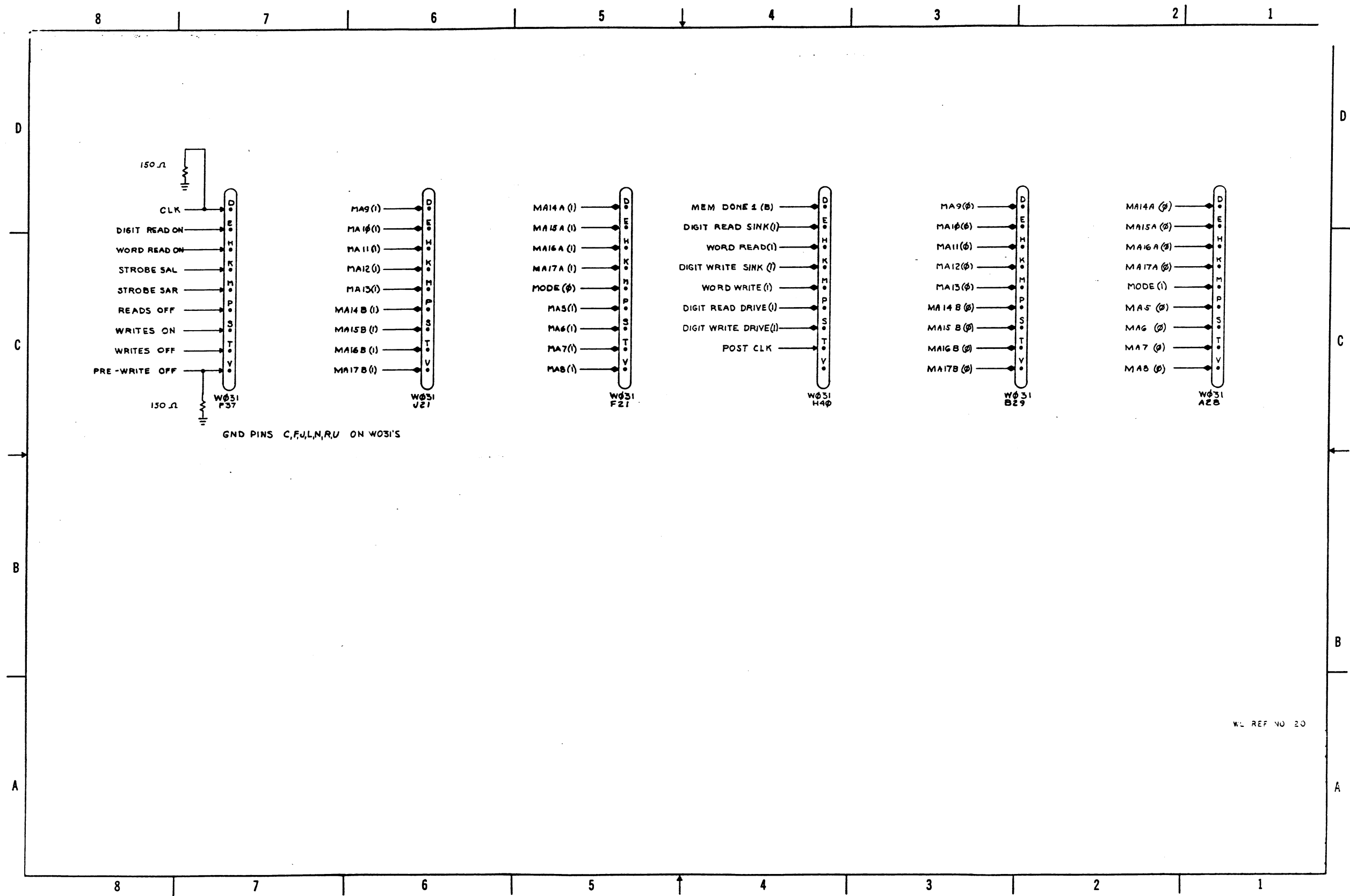
A-PL-MC70-B-9 Module Parts List (Sheet 1)

PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION			DEC. STOCK NO.
			ITEM	STOCK SIZE	CAT. NO. — MFG.	
		1	W016		WORD SINK STACK CONN.	
		1	W017		WORD DRIVE STACK CONN.	
		12	W025		CONNECTOR BOARD	
		1	W028		CABLE CONNECTOR	
		35	W031		CABLE CONNECTOR	
		4	W071		POWER CONNECTOR	
		15	W612		PULSE AMPLIFIER	
		1	S107		INVERTER	
		3	G795		CABLE TERMINATOR	

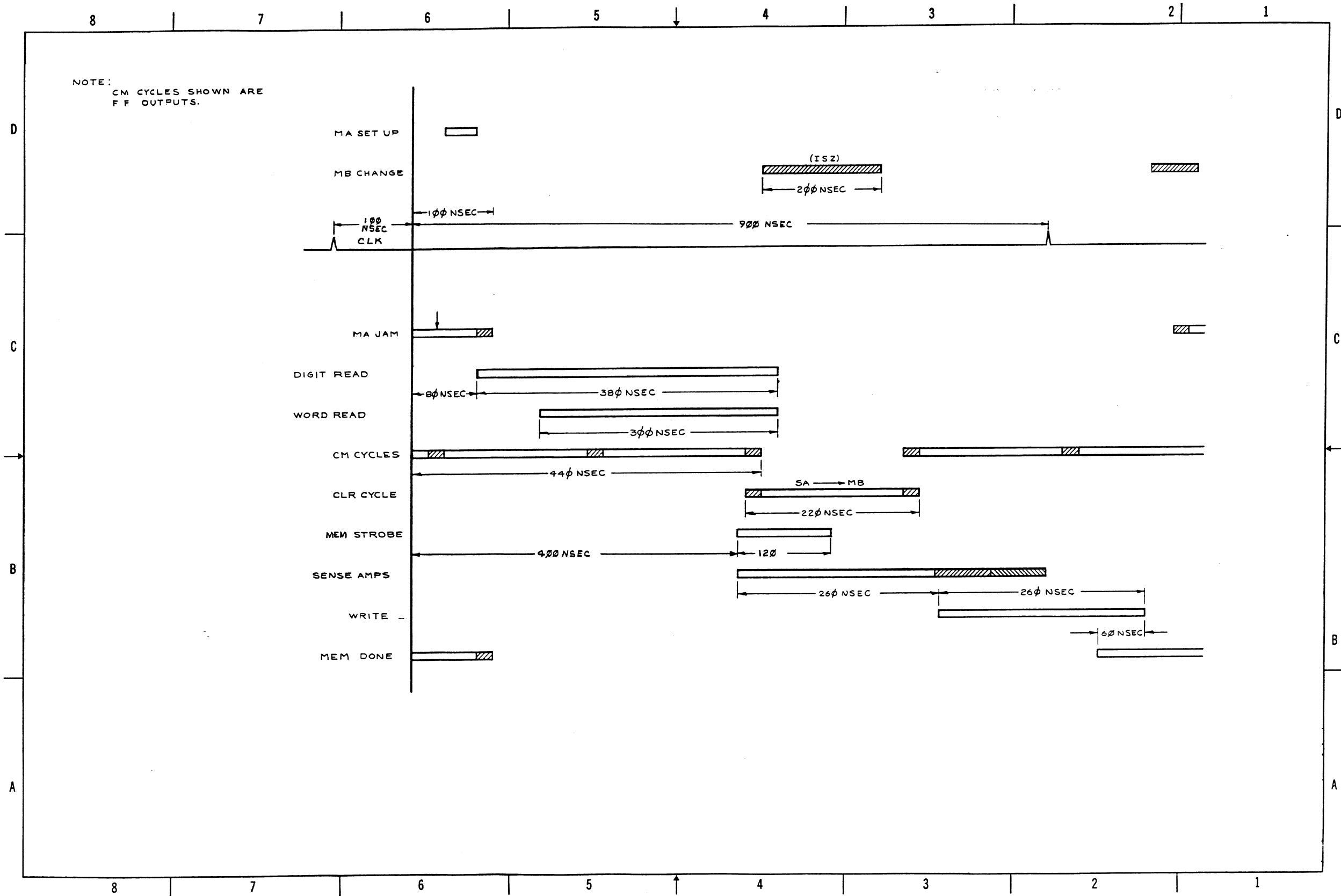
A-PL-MC70-B-9 Module Parts List (Sheet 2)



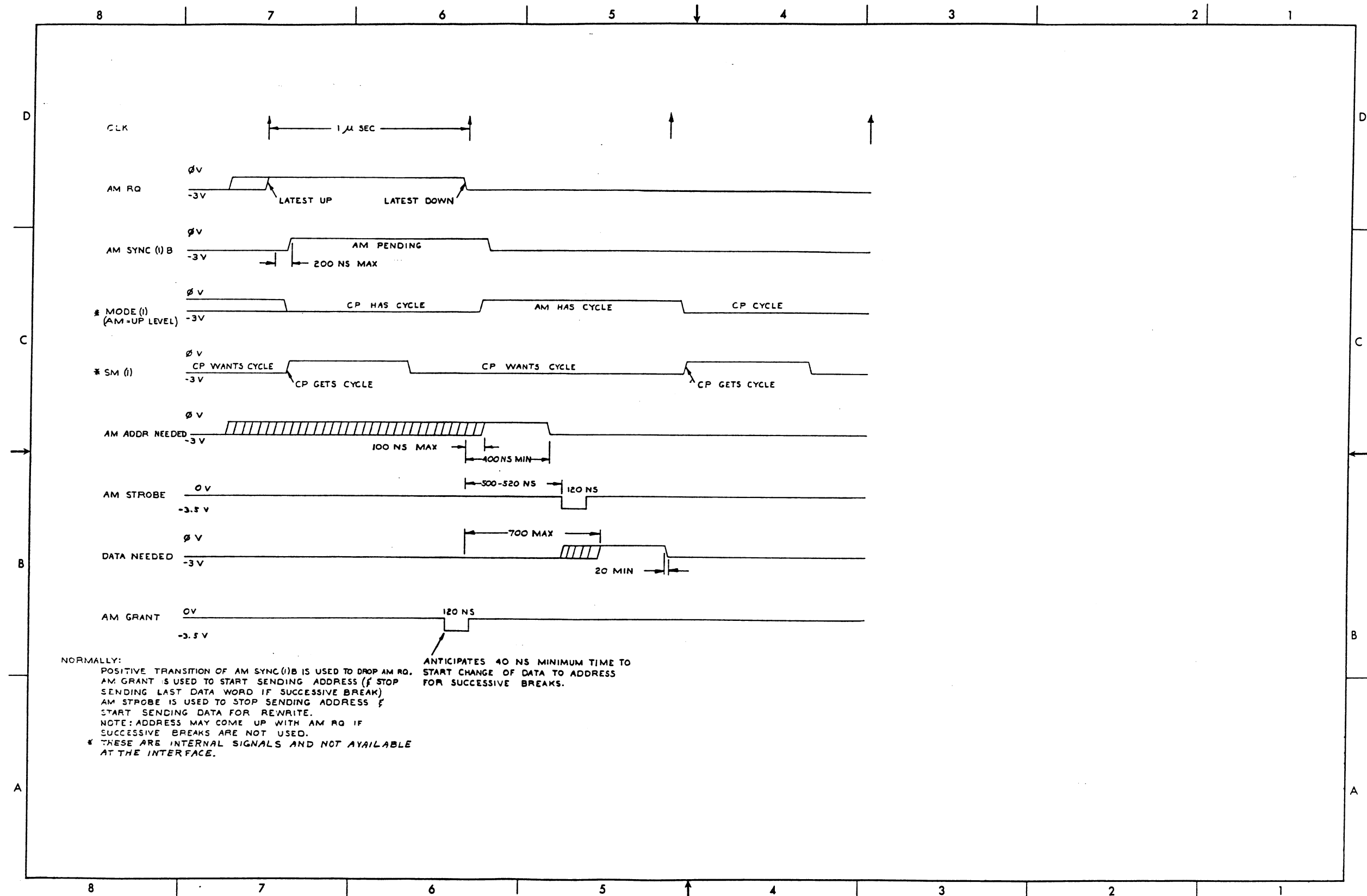
D-BD-MC70-B-10 Functional Block Diagram



D-BS-MC70-B-11 Memory Test Connections



D-TD-MC70-B-14 Mem/CP Timing



NORMALLY:
 POSITIVE TRANSITION OF AM SYNC (i) B IS USED TO DROP AM RQ.
 AM GRANT IS USED TO START SENDING ADDRESS (f STOP SENDING LAST DATA WORD IF SUCCESSIVE BREAK)
 AM STROBE IS USED TO STOP SENDING ADDRESS f
 START SENDING DATA FOR REWRITE.
 NOTE: ADDRESS MAY COME UP WITH AM RQ IF SUCCESSIVE BREAKS ARE NOT USED.
 * THESE ARE INTERNAL SIGNALS AND NOT AVAILABLE AT THE INTERFACE.

ANTICIPATES 40 NS MINIMUM TIME TO START CHANGE OF DATA TO ADDRESS FOR SUCCESSIVE BREAKS.

D-TD-MC70-B-15 DMA Interface Timing

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
BIT 0 FLD 0	A21C	A22E	BLK } TWP	
↓	A21D	A22F	WHT } ↑	
BIT 0 FLD 1	A21E	A22H		
↓	A21F	A22J		
BIT 1 FLD 0	A21H	A23E		
↓	A21J	A23F		
BIT 1 FLD 1	A21K	A23H		
↓	A21L	A23J		
BIT 2 FLD 0	A21M	A24E		
↓	A21N	A24F		
BIT 2 FLD 1	A21P	A24H		
↓	A21R	A24J		
BIT 3 FLD 0	A21S	A25E		
↓	A21T	A25F		
BIT 3 FLD 1	A21U	A25H		
↓	A21V	A25J		
BIT 4 FLD 0	B21C	B22E		
↓	B21D	B22F		
BIT 4 FLD 1	B21E	B22H		
↓	B21F	B22J		
BIT 5 FLD 0	B21H	B23E		
↓	B21J	B23F		
BIT 5 FLD 1	B21K	B23H		
↓	B21L	B23J		
BIT 6 FLD 0	B21M	B24E	BLK } TWP	
↓	B21N	B24F	WHT } ↓	

A-WL-MC70-B-16 TWP Wiring Sheets (Sheet 1)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
BIT 6 FLD 1	B21P	B24H	BLK } TWP	
↓	B21R	B24J	WHT } ↑	
BIT 7 FLD 0	B21S	B25E		
↓	B21T	B25F		
BIT 7 FLD 1	B21U	B25H		
↓	B21V	B25J		
BIT 8 FLD 0	C21C	C22E		
↓	C21D	C22F		
BIT 8 FLD 1	C21E	C22H		
↓	C21F	C22J		
BIT 9 FLD 0	C21H	C23E		
↓	C21J	C23F		
BIT 9 FLD 1	C21K	C23H		
↓	C21L	C23J		
BIT 10 FLD 0	C21M	C24E		
↓	C21N	C24F		
BIT 10 FLD 1	C21P	C24H		
↓	C21R	C24J		
BIT 11 FLD 0	C21S	C25E		
↓	C21T	C25F		
BIT 11 FLD 1	C21U	C25H		
↓	C21V	C25J		
BIT 12 FLD 0	D21C	D22E		
↓	D21D	D22F		
BIT 12 FLD 1	D21E	D22H	BLK } TWP	
↓	D21F	D22J	WHT } ↓	

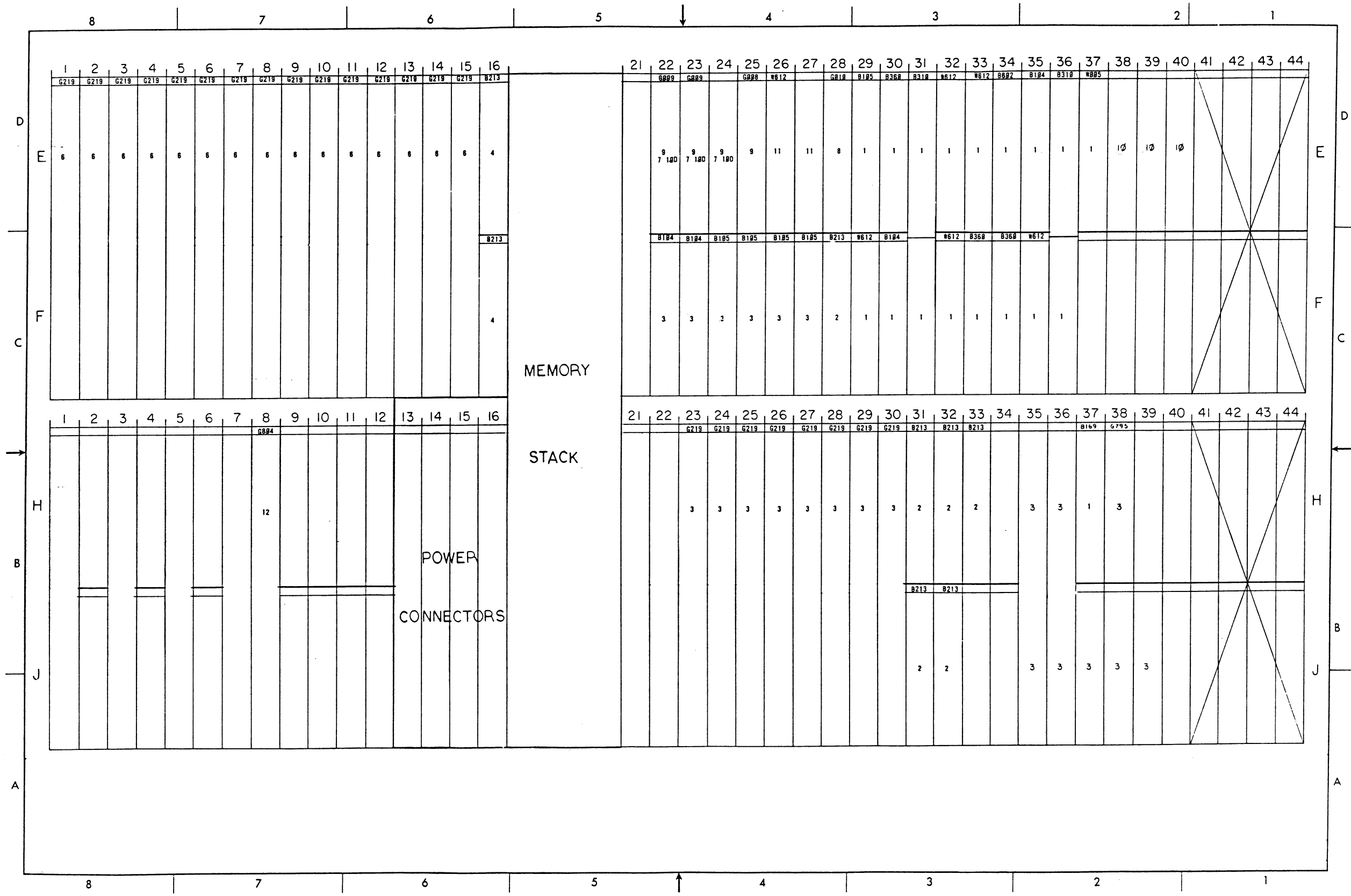
A-WL-MC70-B-16 TWP Wiring Sheets (Sheet 2)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
BIT 13 FLD Ø	D21H	D23E	BLK } TWP	
↓	D21J	D23F	WHT } ↑	
BIT 13 FLD 1	D21K	D23H		
↓	D21L	D23J		
BIT 14 FLD Ø	D21M	D24E		
↓	D21N	D24F		
BIT 14 FLD 1	D21P	D24H		
↓	D21R	D24J		
BIT 15 FLD Ø	D21S	D25E		
↓	D21T	D25F		
BIT 15 FLD 1	D21U	D25H		
↓	D21V	D25J		
BIT 16 FLD Ø	E21C	E22E		
↓	E21D	E22F		
BIT 16 FLD 1	E21E	E22H		
↓	E21F	E22J		
BIT 17 FLD Ø	E21H	E23E		
↓	E21J	E23F		
BIT 17 FLD 1	E21K	E23H		
↓	E21L	E23J		
PARITY BIT FLD Ø	E21M	E24E		
↓	E21N	E24F		
PARITY BIT FLD 1	E21P	E24H	BLK } TWP	
↓	E21R	E24J	WHT } ↓	

A-WL-MC70-B-16 TWP Wiring Sheets (Sheet 3)

SIGNAL NAME	FROM PIN	TO PIN	COLOR	REMARKS
MBS Ø5	C30C	B11C	BLK } TWP	
↑ Ø5	C30D	A11U	WHT } ↑	
Ø5	A11C	H11C		
Ø5	A11U	F11U		
Ø6	C31C	A10C		
Ø6	C31E	A10U		
Ø6	A10C	H10C		
Ø6	A10U	F10U		
Ø7	C31M	A09C		
Ø7	C31D	A09U		
Ø7	B09C	H09C		
Ø7	A09U	F09U		
Ø8	H08C	B08C		
Ø8	F08U	A08U		
Ø8	A08C	C32C		
Ø8	A08U	C32E		
Ø9	H06C	B06C		
Ø9	F06U	A06U		
Ø9	A06C	C32M		
Ø9	A06U	C32D		
1Ø	B05C	H05C		
1Ø	A05U	F05U		
1Ø	C33M	A05C		
1Ø	C33E	A05U		
↓ 11	H04C	A04C	BLK } TWP	
MBS 11	F04U	A04U	WHT } ↓	

A-WL-MC70-B-16 TWP Wiring Sheets (Sheet 4)

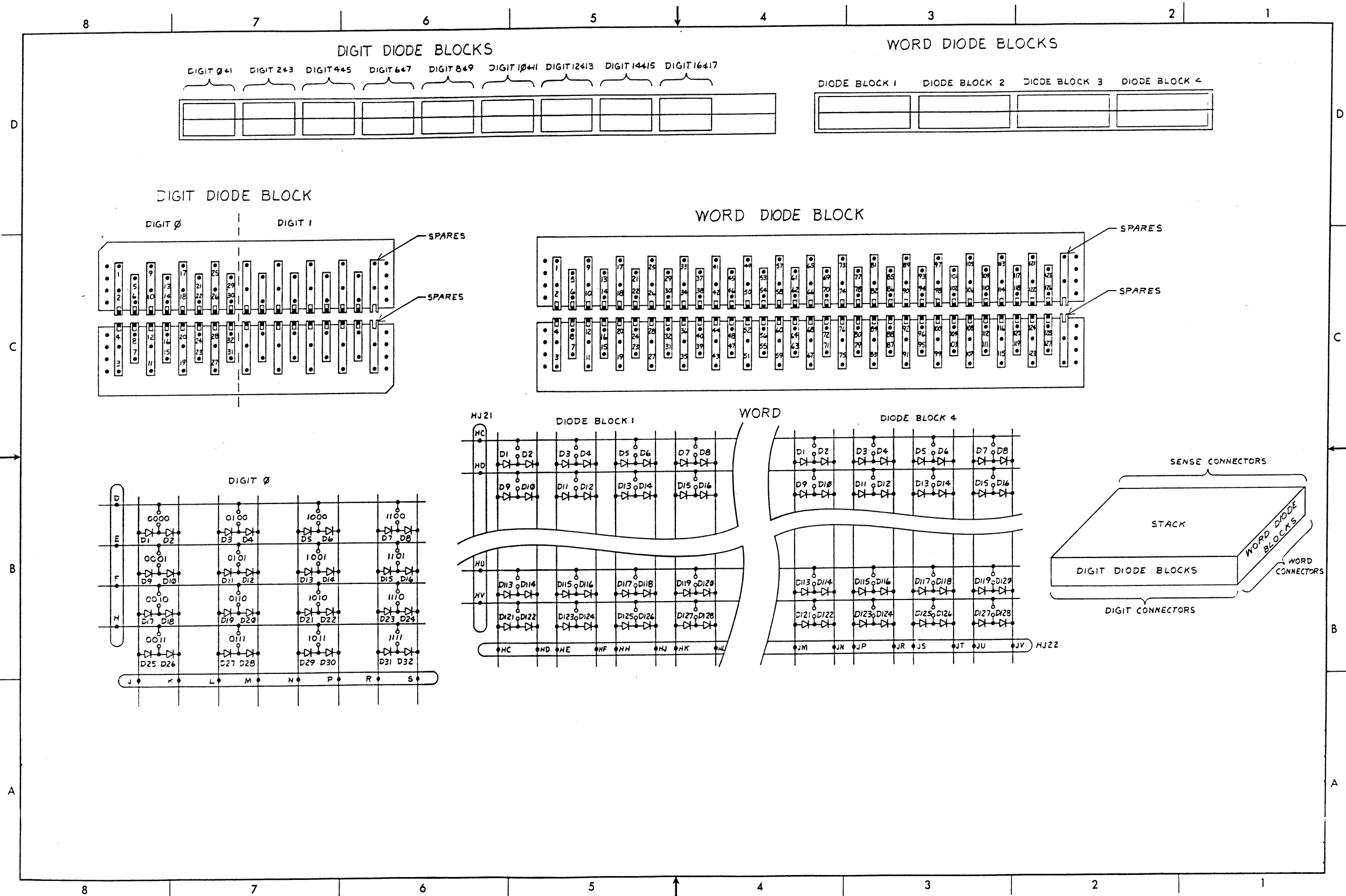


D-SP-MC70-B-17 MC Switch Configuration (Sheet 2)

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS						
ENGINEERING SPECIFICATION				DATE 6/9/67		
TITLE EMI MEMORY STACK INSTALLATION PROCEDURE						
REVISIONS						
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
	ORIG.	69				
	ADDED "E&L"	87	D.A.	7/14/67		

- Remove the memory from the wooden box.
- Inspect all cables for broken wires, cold solder or broken components.
- Remove the KEP nuts from the top of the stacks mounting screws.
- Remove the stack holddown bar from the stack frame. Be sure you save the four white nylon washers that are used as spacers between the stack holddown bar and stack frame.
- Inspect the stack frame to be sure the stack mount blocks are covered with electrical tape. These blocks will be nylon on future machines.
- Place the stack, with the manufacturers label up on to the edge of the stack frame.
- Place the sense winding cables (W025 double boards) into the locations shown in figure 1.
- Place the W016 card into locations HJ21. Place the W017 card into locations HJ22.
- Place the white nylon washers over the four holes in the stack frame.
- Place the metal holddown bar over the stack bolts, positioning the stack so that the holddown may be fasten to the stack frame.
- Fasten the stack holddown bar to the stack frame using the nylon bolts provided.
- Fasten the stacks to the holddown bar with the kep nuts provided.

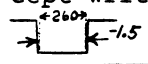
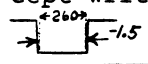
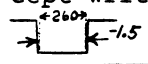
ENGINEERING SPECIFICATION		digital	CONTINUATION SHEET																																													
TITLE EMI MEMORY STACK INSTALLATION PROCEDURE																																																
<p>13. Insert the digit drive cables (W015) using the table in figure 1.</p> <p>14. The stack holddown bar should be isolated from the stack frame via the nylon washers and nylon bolts. With an ohm meter try to measure continuity between the stack holddown bar and stack frame - there should be none. If you read continuity, reinspect the nylon washers, and bolt position.</p>																																																
<p>REAR VIEW</p>																																																
<p>SENSE WINDING CABLES AS VIEWED FROM WIRING SIDE OF LOGIC</p>																																																
<p>PDP-9 MEMORY INSTALLATION</p>																																																
<p>FIG 1</p> <table border="1"> <thead> <tr> <th colspan="3">CABLE LOCATION *</th> </tr> </thead> <tbody> <tr><td>1</td><td>C, D, 7</td><td>W015</td></tr> <tr><td>2</td><td>CD15</td><td>W015</td></tr> <tr><td>3</td><td>CD14</td><td>W015</td></tr> <tr><td>4</td><td>CD13</td><td>W015</td></tr> <tr><td>5</td><td>CD12</td><td>W015</td></tr> <tr><td>6</td><td>CD11</td><td>W015</td></tr> <tr><td>7</td><td>CD10</td><td>W015</td></tr> <tr><td>8</td><td>CD9</td><td>W015</td></tr> <tr><td>9</td><td>CD8</td><td>W015</td></tr> <tr><td>10</td><td>HJ21</td><td>W016</td></tr> <tr><td>11</td><td>HJ22</td><td>W017</td></tr> <tr><td>12</td><td>EF21</td><td>W025</td></tr> <tr><td>13</td><td>CD21</td><td>W025</td></tr> <tr><td>14</td><td>AB21</td><td>W025</td></tr> </tbody> </table> <p>*ALL CARDS ARE DOUBLE BOARDS</p>				CABLE LOCATION *			1	C, D, 7	W015	2	CD15	W015	3	CD14	W015	4	CD13	W015	5	CD12	W015	6	CD11	W015	7	CD10	W015	8	CD9	W015	9	CD8	W015	10	HJ21	W016	11	HJ22	W017	12	EF21	W025	13	CD21	W025	14	AB21	W025
CABLE LOCATION *																																																
1	C, D, 7	W015																																														
2	CD15	W015																																														
3	CD14	W015																																														
4	CD13	W015																																														
5	CD12	W015																																														
6	CD11	W015																																														
7	CD10	W015																																														
8	CD9	W015																																														
9	CD8	W015																																														
10	HJ21	W016																																														
11	HJ22	W017																																														
12	EF21	W025																																														
13	CD21	W025																																														
14	AB21	W025																																														



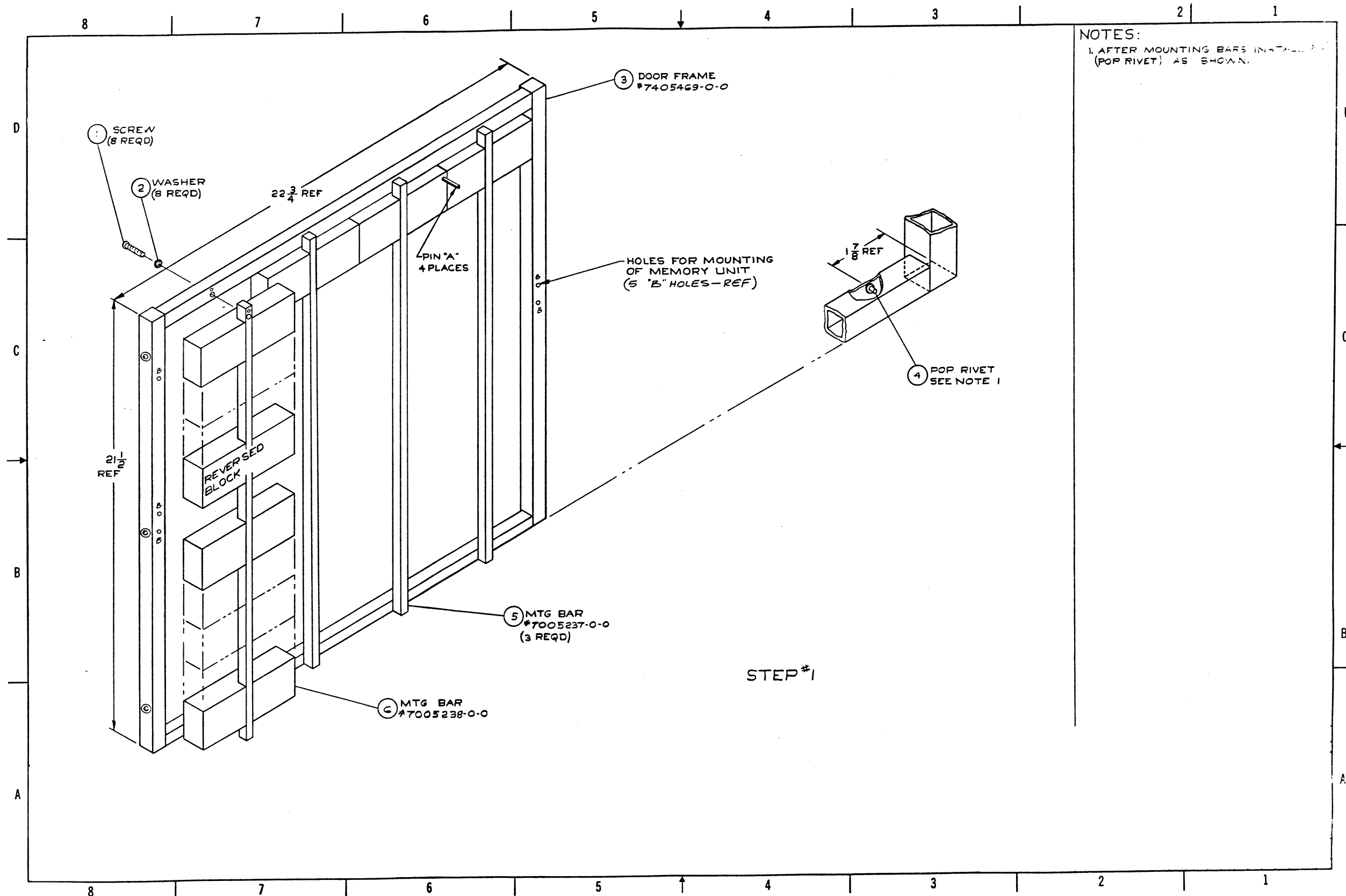
D-SP-MC70-B-19 EMI Diode Identification

DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS						
ENGINEERING SPECIFICATION				DATE 8/1/67		
TITLE "CORE MEMORY ON-LINE ADJUSTMENT PROCEDURE"						
REVISIONS						
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
—	Original	89	D.Ringleb	7/67	R.DIETER	7/67

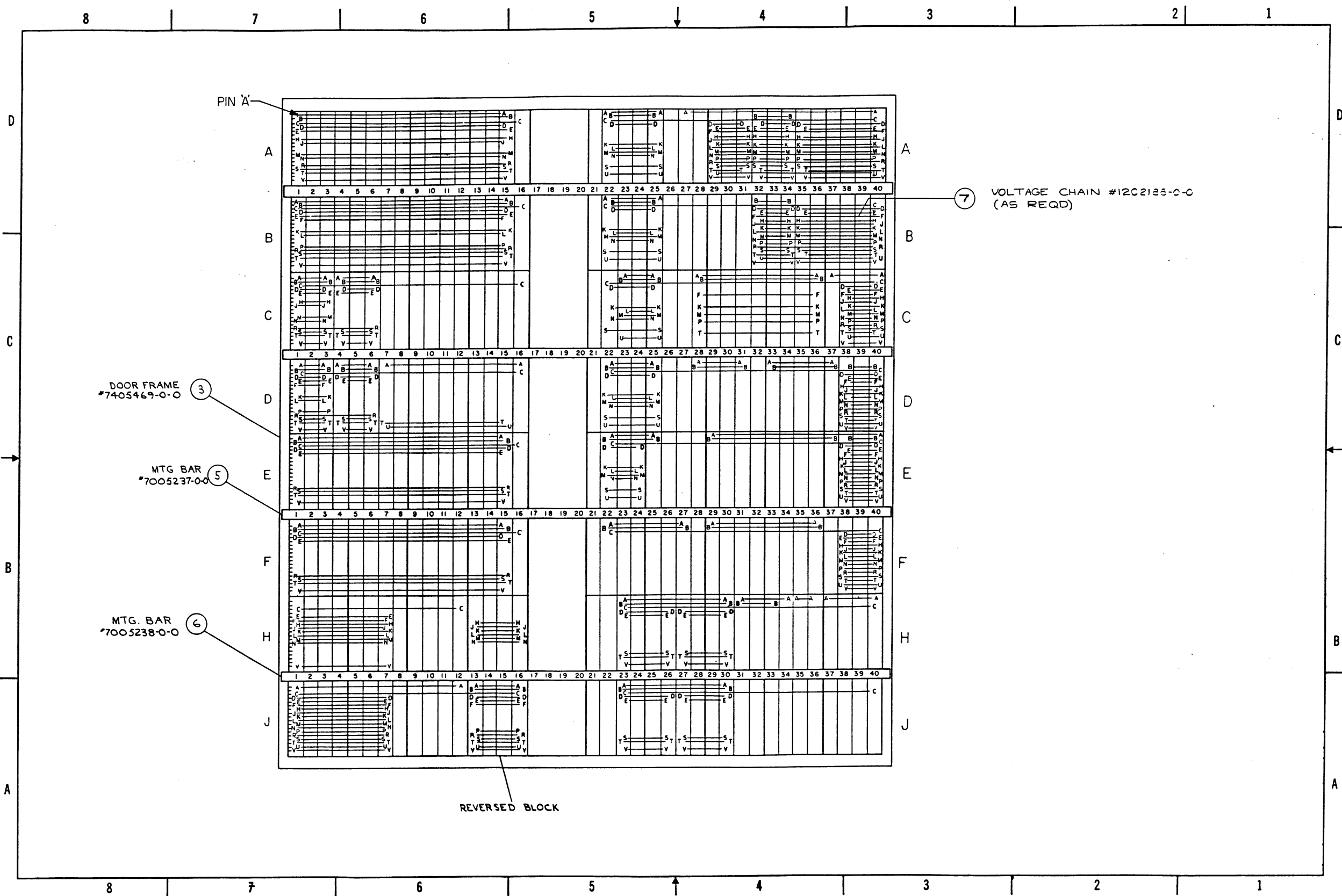
A-SP-MC70-B-20 Core Memory On-Line Adjustment (Sheet 1)

ENGINEERING SPECIFICATION		digital	CONTINUATION SHEET																																																	
TITLE "CORE MEMORY ON-LINE ADJUSTMENT PROCEDURE"																																																				
<p>All variables are adjusted to the specified settings in the memory off-line test. However, the following settings should be verified.</p> <p style="text-align: center;">At room Temp. (25°C)</p> <table border="1" style="width: 100%; border-collapse: collapse; margin: 10px 0;"> <thead> <tr> <th style="width: 25%;">VOLTAGE NAME</th> <th style="width: 25%;">NEG PROBE</th> <th style="width: 25%;">POS PROBE</th> <th style="width: 25%;">VOLTAGE</th> </tr> </thead> <tbody> <tr> <td>Memory Voltage</td> <td>H01M</td> <td>J01M</td> <td>23.5V</td> </tr> <tr> <td>2nd Stage Clamp</td> <td>E25B</td> <td>E25N</td> <td>6.0V</td> </tr> <tr> <td>Slice Level</td> <td>E25H</td> <td>E25A</td> <td>≈ 4.2V*</td> </tr> </tbody> </table> <p>*The 4.2V is only an approximate setting and obtaining the specified positive and negative spread on sense amp. margins in the off-line test may cause this setting to be 4.2 ±.2V.</p> <p style="text-align: center;">Voltage adjustments to be made with a multimeter.</p> <p style="text-align: center;">At room Temp. (25°C)</p> <table border="1" style="width: 100%; border-collapse: collapse; margin: 10px 0;"> <thead> <tr> <th style="width: 12.5%;">DLY NAME</th> <th style="width: 12.5%;">LOC</th> <th style="width: 12.5%;">PROBE1</th> <th style="width: 12.5%;">PROBE2</th> <th style="width: 12.5%;">DLY</th> <th style="width: 42.5%;">COMMENTS</th> </tr> </thead> <tbody> <tr> <td>MA SET-UP</td> <td>D35</td> <td>F36M</td> <td>C16D</td> <td>180</td> <td rowspan="4" style="vertical-align: middle;"> All measurements from -1.5 V of leading edge going neg. except write;  </td> </tr> <tr> <td>STAGGER</td> <td>D33</td> <td>C16D</td> <td>H33D</td> <td>*80NS</td> </tr> <tr> <td>STROBE</td> <td>E30</td> <td>C16D</td> <td>E32L</td> <td>320NS</td> </tr> <tr> <td>PAUSE</td> <td>F33</td> <td>E32L</td> <td>H32N</td> <td>260N</td> </tr> <tr> <td>WRITE</td> <td>F34</td> <td>-</td> <td>H32N</td> <td>260NS</td> <td></td> </tr> </tbody> </table> <p>*This is only an approximation. The actual STAGGER time is defined in the off-line test by optimizing Peak/Strobe (setting the strobe on the core output peak for maximum sense amp. margins).</p> <p>If the MA SET-UP, PAUSE or WRITE delays are incorrect. They should be adjusted to the specified value by varying the appropriate delay. However, if the STROBE setting is off the STAGGER delay should be increased or decreased by the same amount. (This is to keep the Peak/Strobe optimization which the misadjusted memory can be assumed to have had.)</p>				VOLTAGE NAME	NEG PROBE	POS PROBE	VOLTAGE	Memory Voltage	H01M	J01M	23.5V	2nd Stage Clamp	E25B	E25N	6.0V	Slice Level	E25H	E25A	≈ 4.2V*	DLY NAME	LOC	PROBE1	PROBE2	DLY	COMMENTS	MA SET-UP	D35	F36M	C16D	180	All measurements from -1.5 V of leading edge going neg. except write; 	STAGGER	D33	C16D	H33D	*80NS	STROBE	E30	C16D	E32L	320NS	PAUSE	F33	E32L	H32N	260N	WRITE	F34	-	H32N	260NS	
VOLTAGE NAME	NEG PROBE	POS PROBE	VOLTAGE																																																	
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WRITE	F34	-	H32N	260NS																																																

A-SP-MC70-B-20 Core Memory On-Line Adjustment (Sheet 2)



D-AD-7005219-0-0 Memory Bus Assembly (Sheet 1)



DOOR FRAME
#7405469-0-0 (3)

MTG BAR
#7005237-0-0 (5)

MTG. BAR
#7005238-0-0 (6)

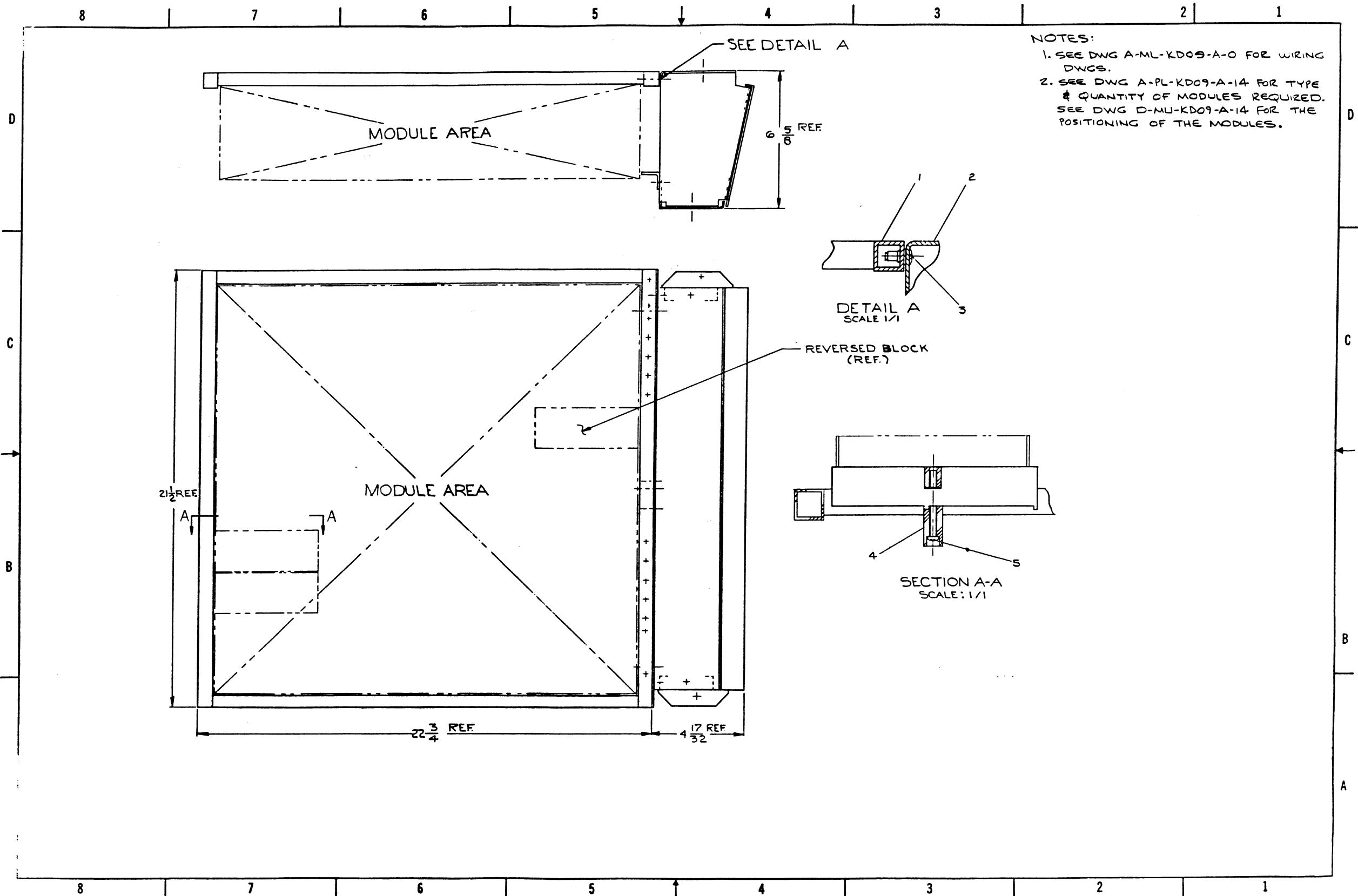
(7) VOLTAGE CHAIN #1202185-0-0
(AS REQD)

REVERSED BLOCK

D-AD-7005219-0-0 Memory Bus Assembly (Sheet 2)

PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION		DEC. STOCK NO.
			ITEM	STOCK SIZE — CAT. NO. — MFG.	
1		8		SCREW PHL PAN H 8-32 x 1 1/4 SST.	
2		8		WASHER LOCK INT #8- SST	
3	E-IA-7405469-0-0	1		DOOR FRAME (MEMORY)	
4		1		POP RIVET 1/8 DIA. x 3/16 LG.	
5	D-AD-7005237-0-0	3		MTG BAR (9 CONN BLOCKS)	
6	D-AD-7005238-0-0	1		MTG BAR (ONE REVERSED BLOCK)	
7		AR		VOLT CHAIN PUR SPEC #CHV 0001	1202188-0-0

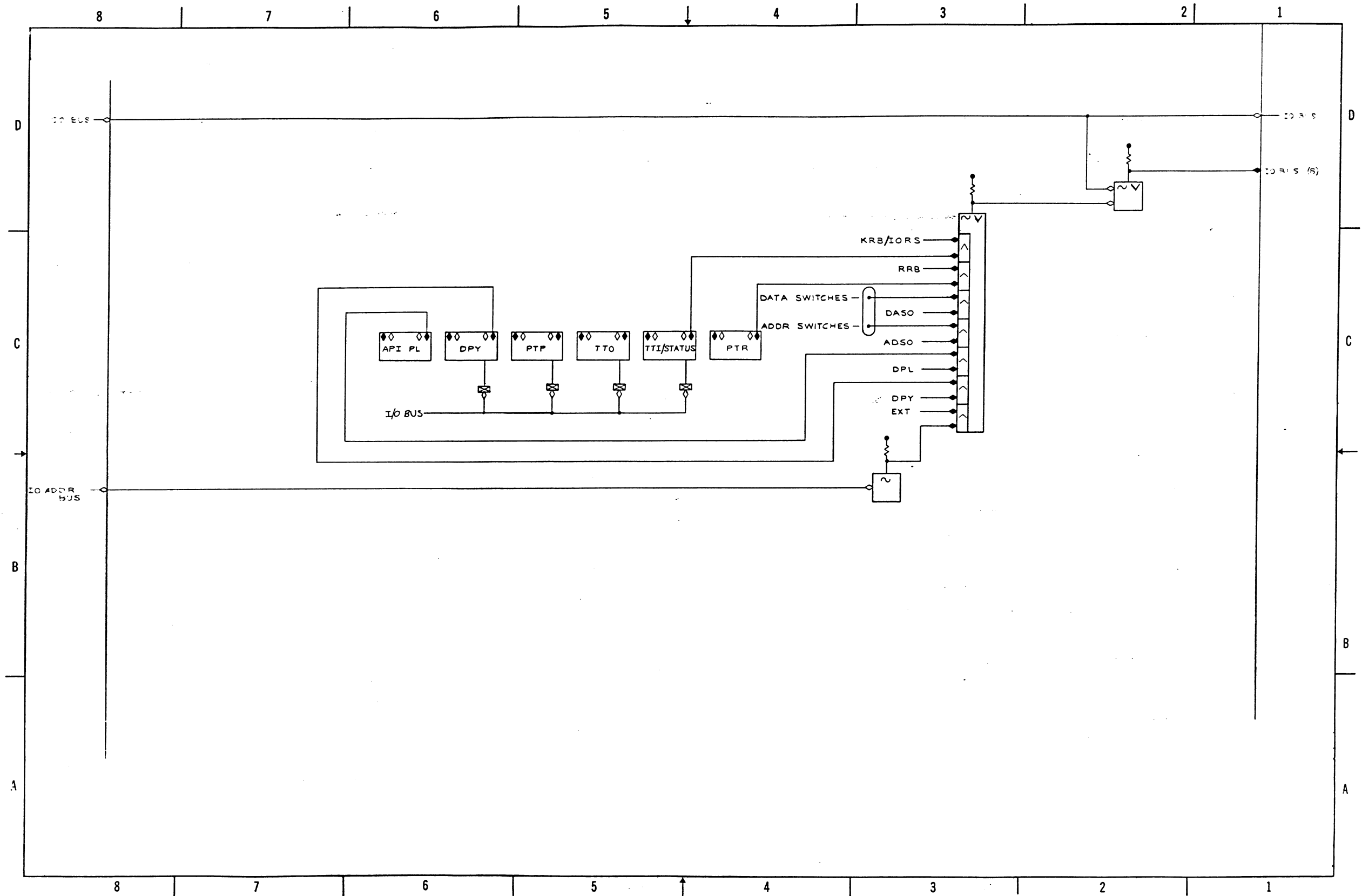
A-PL-7005219-0-0 Memory Bus Parts List



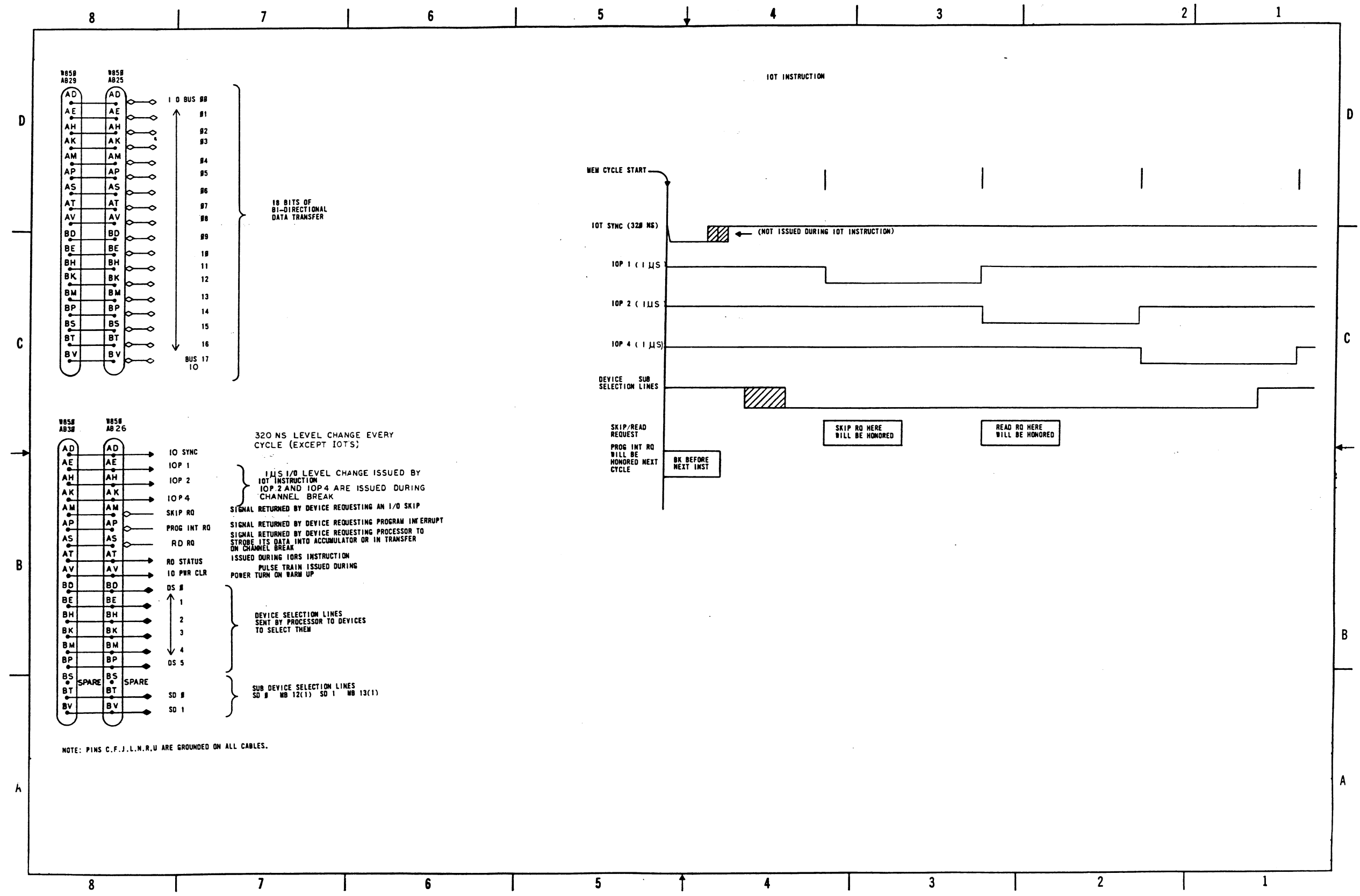
D-UA-KD09-A-0 Unit Assembly

PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION		DEC. STOCK NO.
			ITEM	STOCK SIZE — CAT. NO. — MFG.	
1	D-AD-7005302-0-0	1		I/O BUS ASSEMBLY	7005302-0-0
2	A-PL-7005229-0-0	1		FAN & MARGINAL CHECK ASSY	7 005229-0-0
3		3		SCR PHL TRUS HD 1/4-20 x 5/8 SST	
	A-ML-KD09-A	REF		MDL (I/O ASSEMBLY)	
	D=MU-KD09-A-14	REF		MODULE UTILIZATION LIST	
	A-PL-KD09-A-14	REF		MODULE LIST	
4	B-MD-7406047-0-0	1		BLOCK RETAINER	7406047-0-0
5		2		SCR PHL HD PAN #8-32 x 1 5/8 SST	

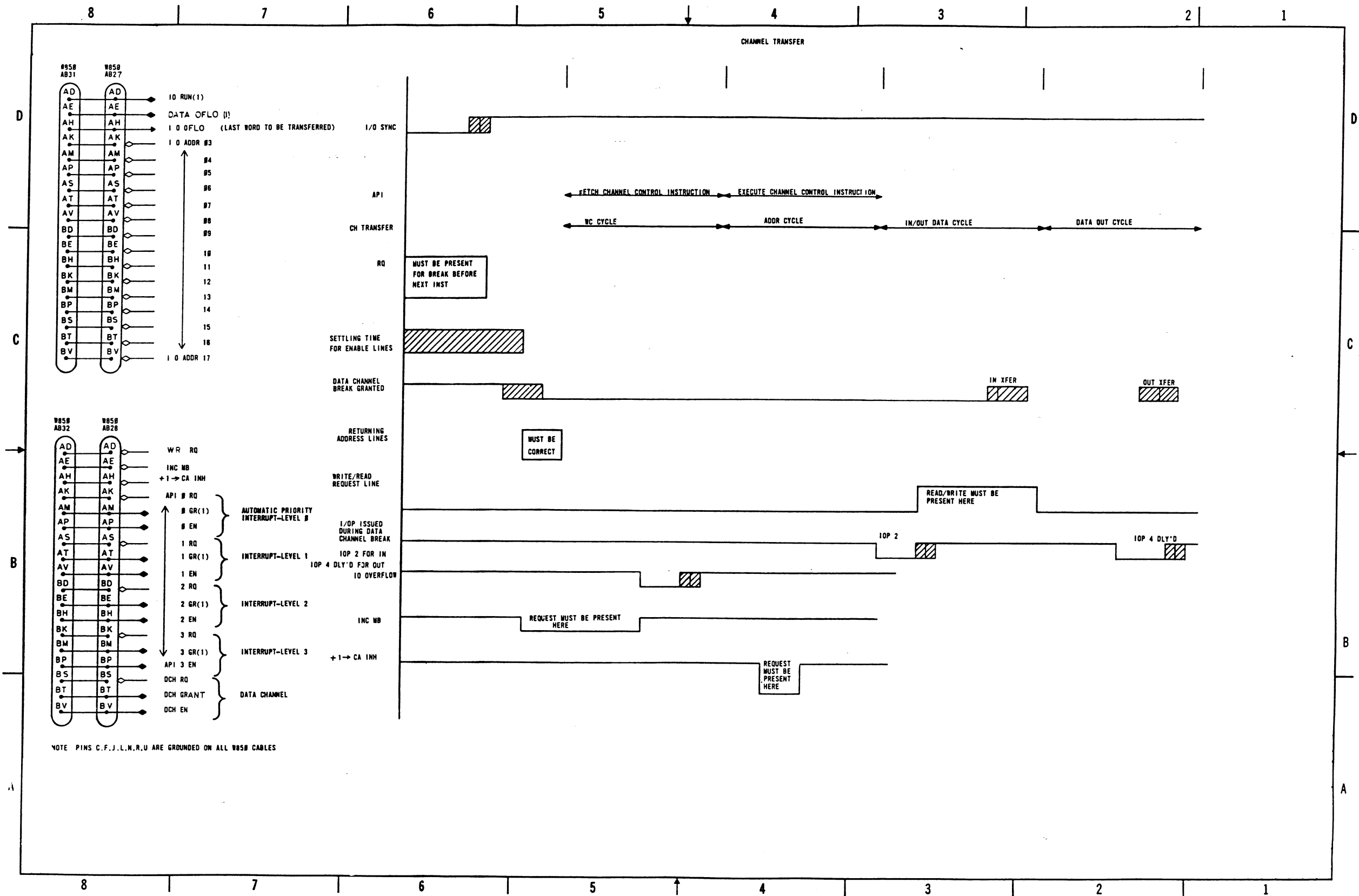
A-PL-KD09-A-0 Assembly Parts List



D-BS-KD09-A-1 IO Configuration

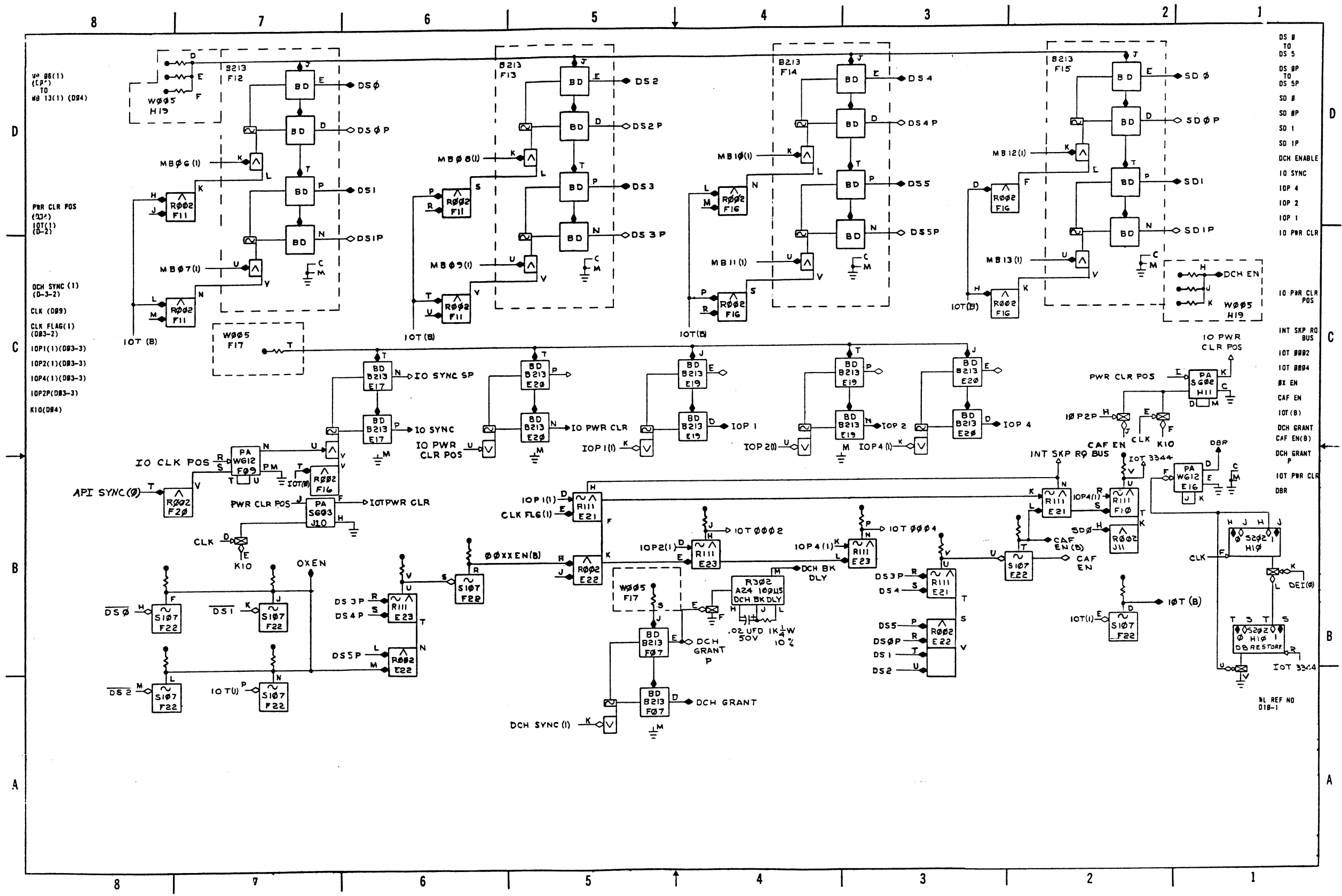


D-TD-KD09-A-2 IO Bus Interface (Sheet 1)

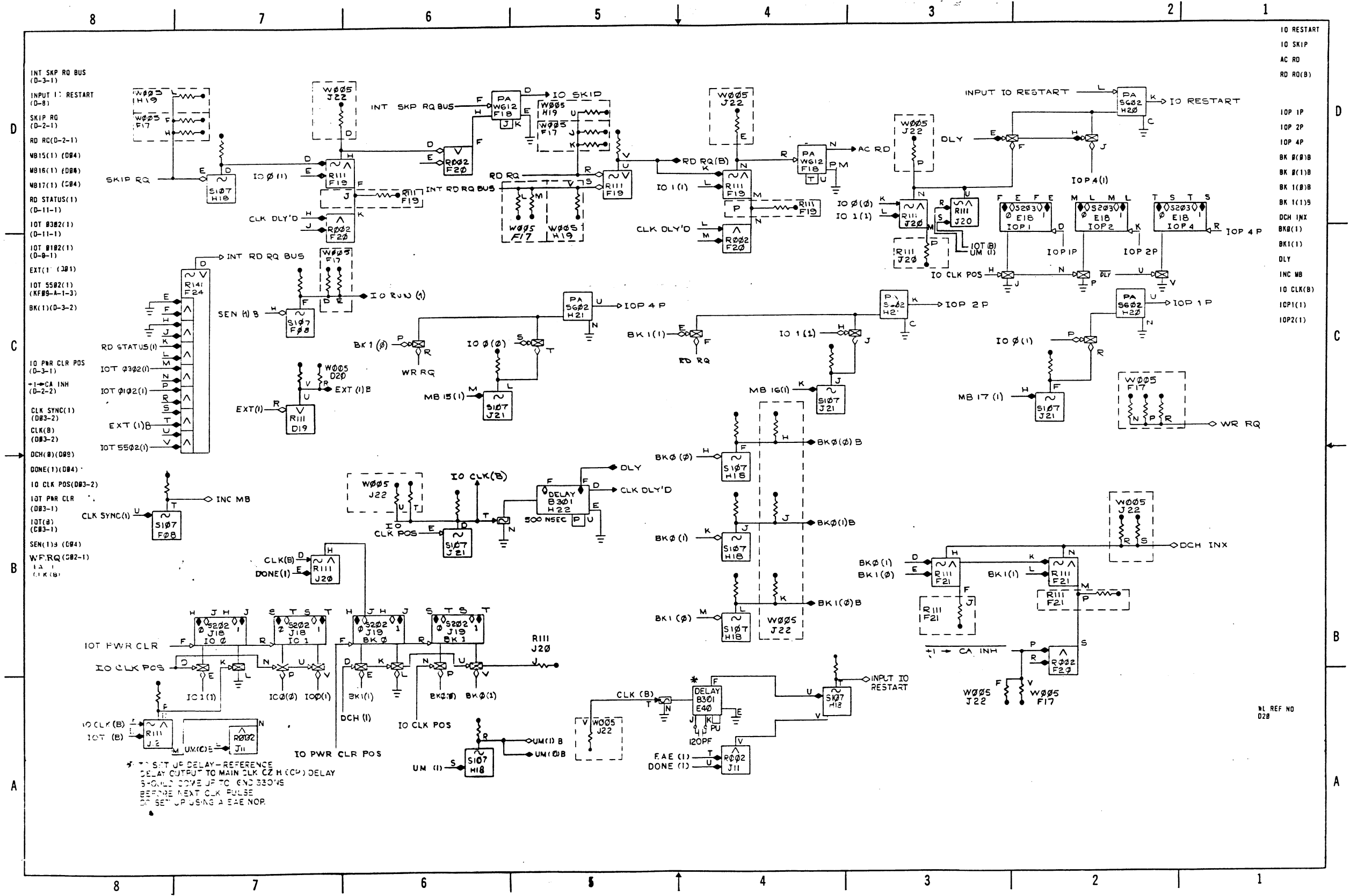


NOTE PINS C.F.J.L.N.R.U ARE GROUNDED ON ALL W858 CABLES

D-TD-KD09-A-2 IO Bus Interface (Sheet 2)



D-BS-KD09-A-3 IO Control (Sheet 1)



INT SKP RQ BUS (D-3-1)
 INPUT 1: RESTART (D-8)
 SKIP RQ (D-2-1)
 RD RQ(D-2-1)
 MB15(1) (DB4)
 MB16(1) (DB4)
 MB17(1) (DB4)
 RD STATUS(1) (D-11-1)
 IOT #302(1) (D-11-1)
 IOT #102(1) (D-9-1)
 EXT(1) (DB1)
 IOT 5502(1) (KF89-A-1-3)
 BK(1)(D-3-2)

IO PWR CLR POS (D-3-1)
 IOT #302(1) (D-3-1)
 IOT #102(1) (D-2-2)
 CLK SYNC(1) (DB3-2)
 CLK(B) (DB3-2)
 DCH(B)(DB3)

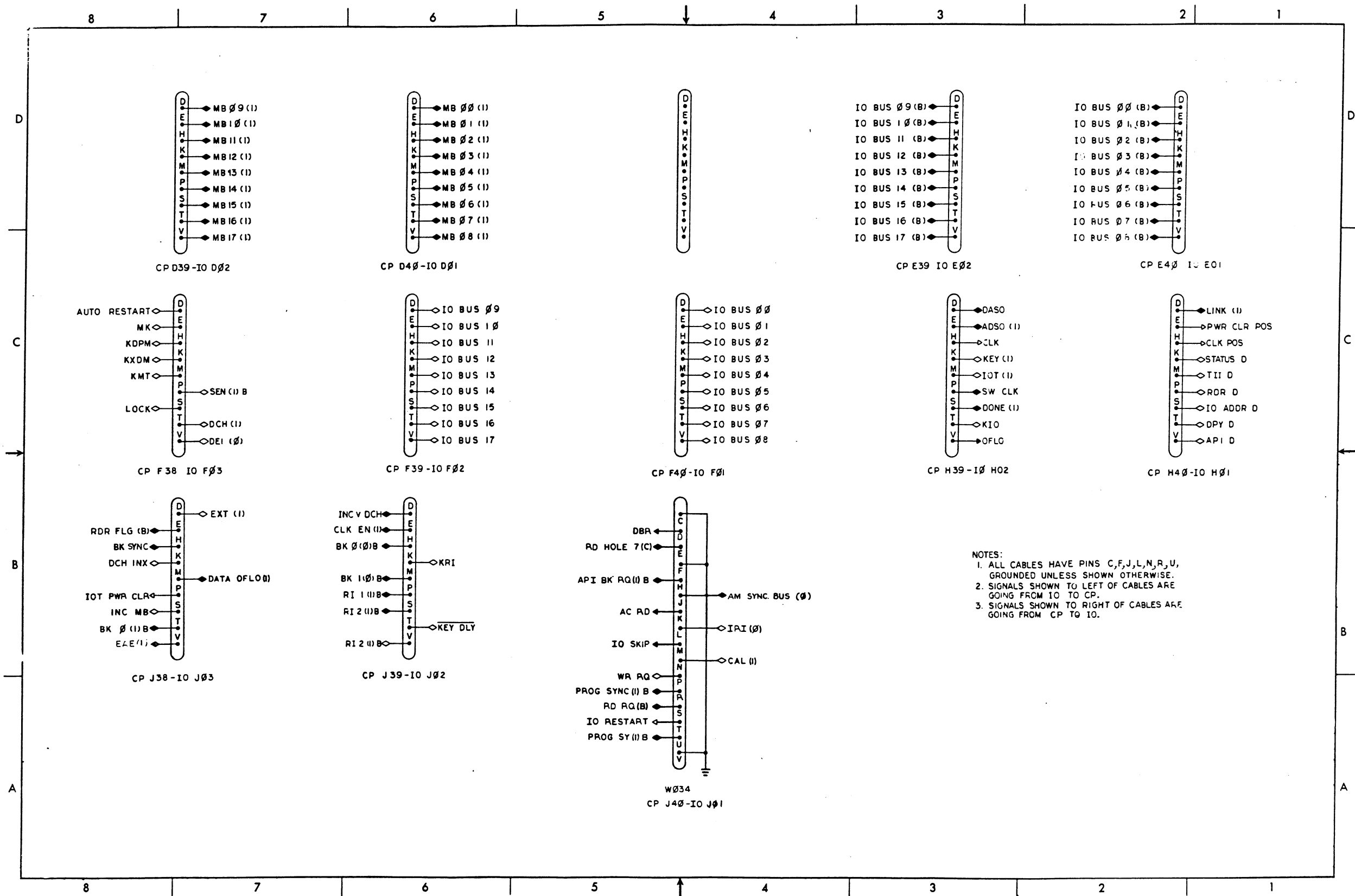
DONE(1)(DB4)
 IO CLK POS(DB3-2)
 IOT PWR CLR (DB3-1)
 IOT(B) (DB3-1)
 SEN(1)(DB4)
 WFR RQ(SB2-1) (1 X(B))

* TO SET UP DELAY-REFERENCE DELAY OUTPUT TO MAIN CLK C2 H(C4) DELAY SHOULD COME UP TO END 3304S BEFORE NEXT CLK PULSE OR SET UP USING A EAE NOP.

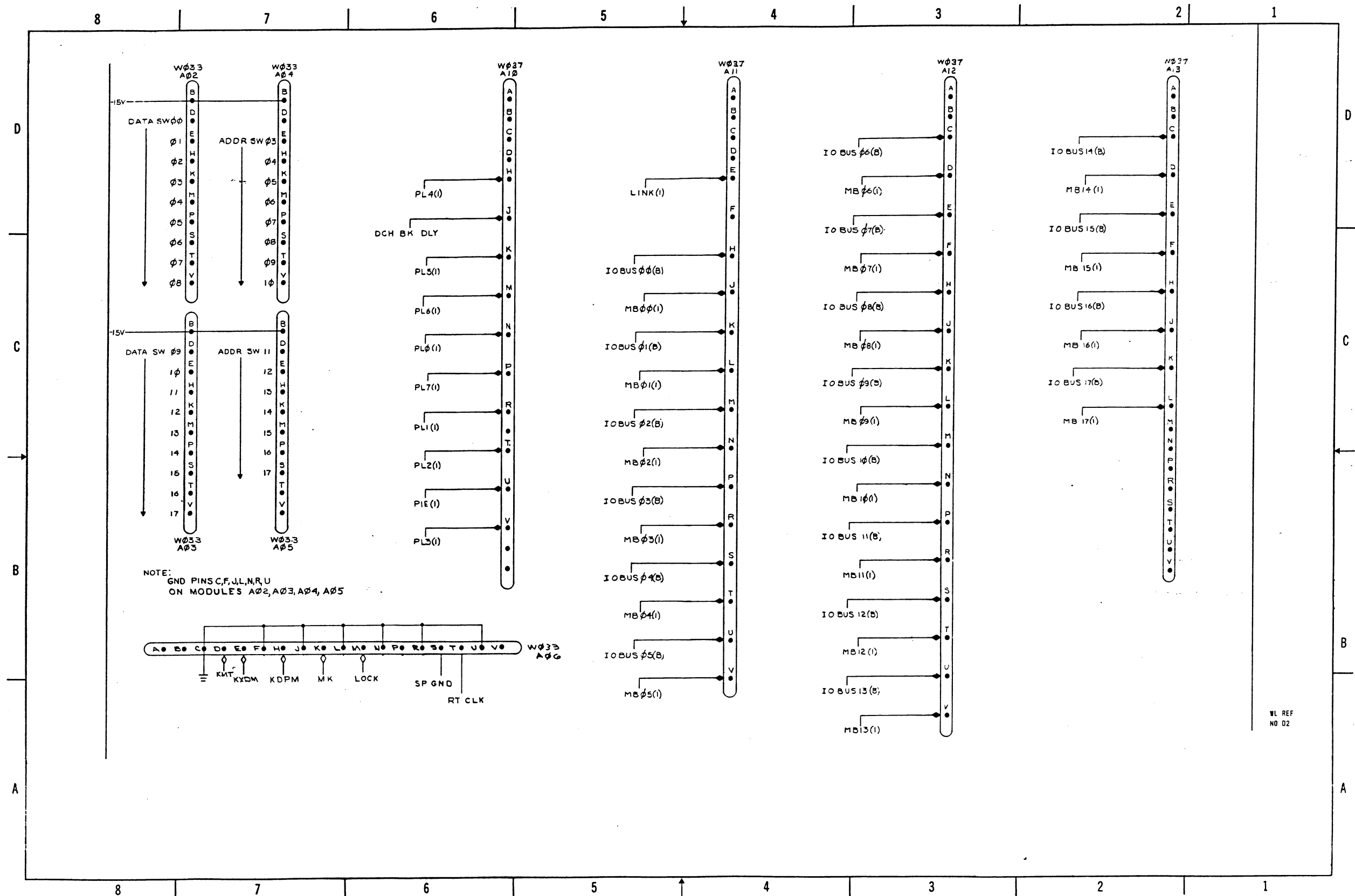
IO RESTART
 IO SKIP
 AC RD
 RD RQ(B)
 IOP 1P
 IOP 2P
 IOP 4P
 BK #0(B)
 BK #1(B)
 BK 1(B)
 BK 1(B)
 DCH INX
 BK#(1)
 BK1(1)
 DLY
 INC MB
 IO CLK(B)
 IOP1(1)
 IOP2(1)

NL REF NO 028

D-BS-KD09-A-3 IO Control (Sheet 3)

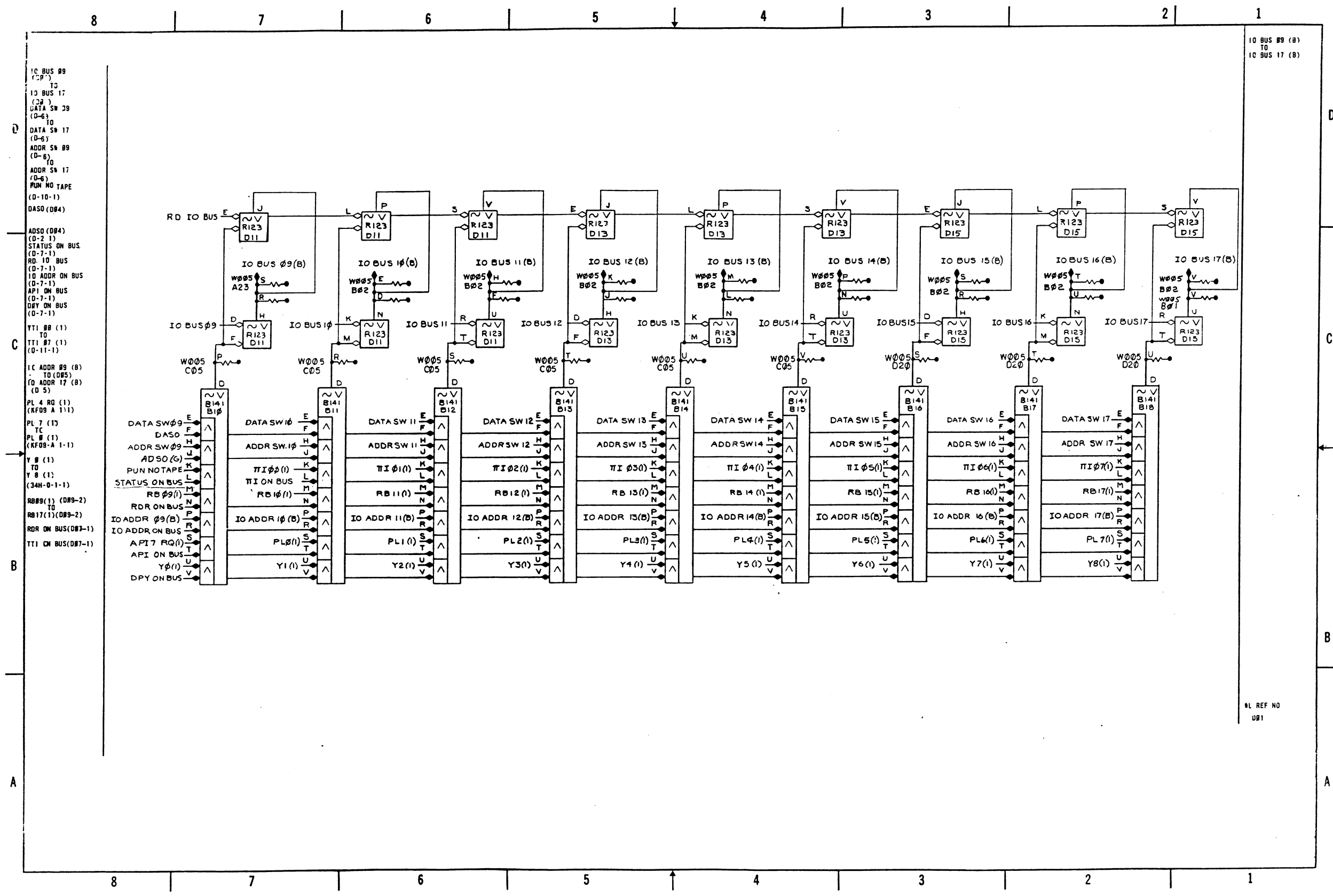


D-IC-KD09-A-4 IO/CP Cable Interface

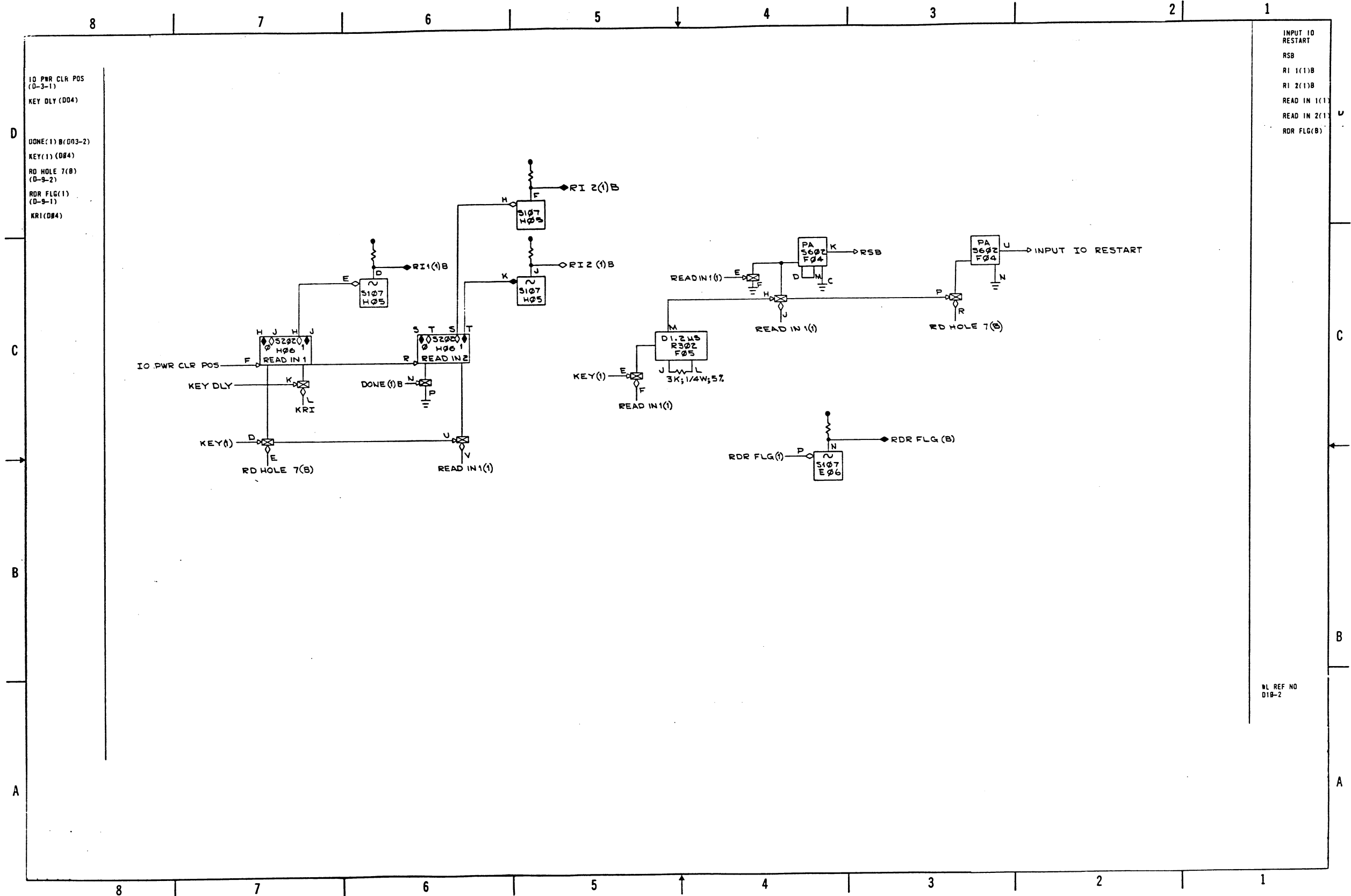


D-BS-KD09-A-6 IO/Console Interface

WL REF
NO 02

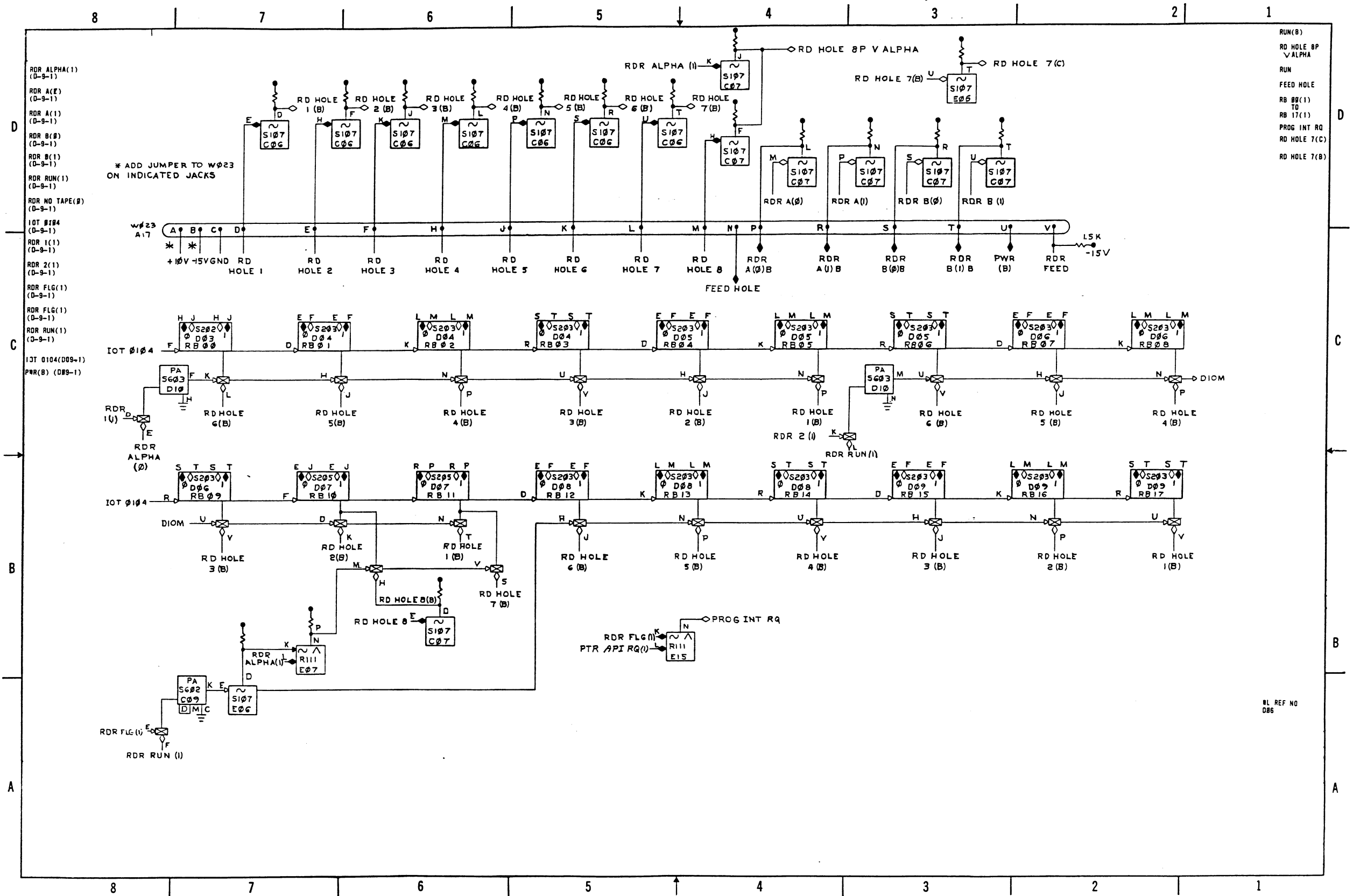


D-BS-KD09-A-7 Input Mixer (Sheet 2)

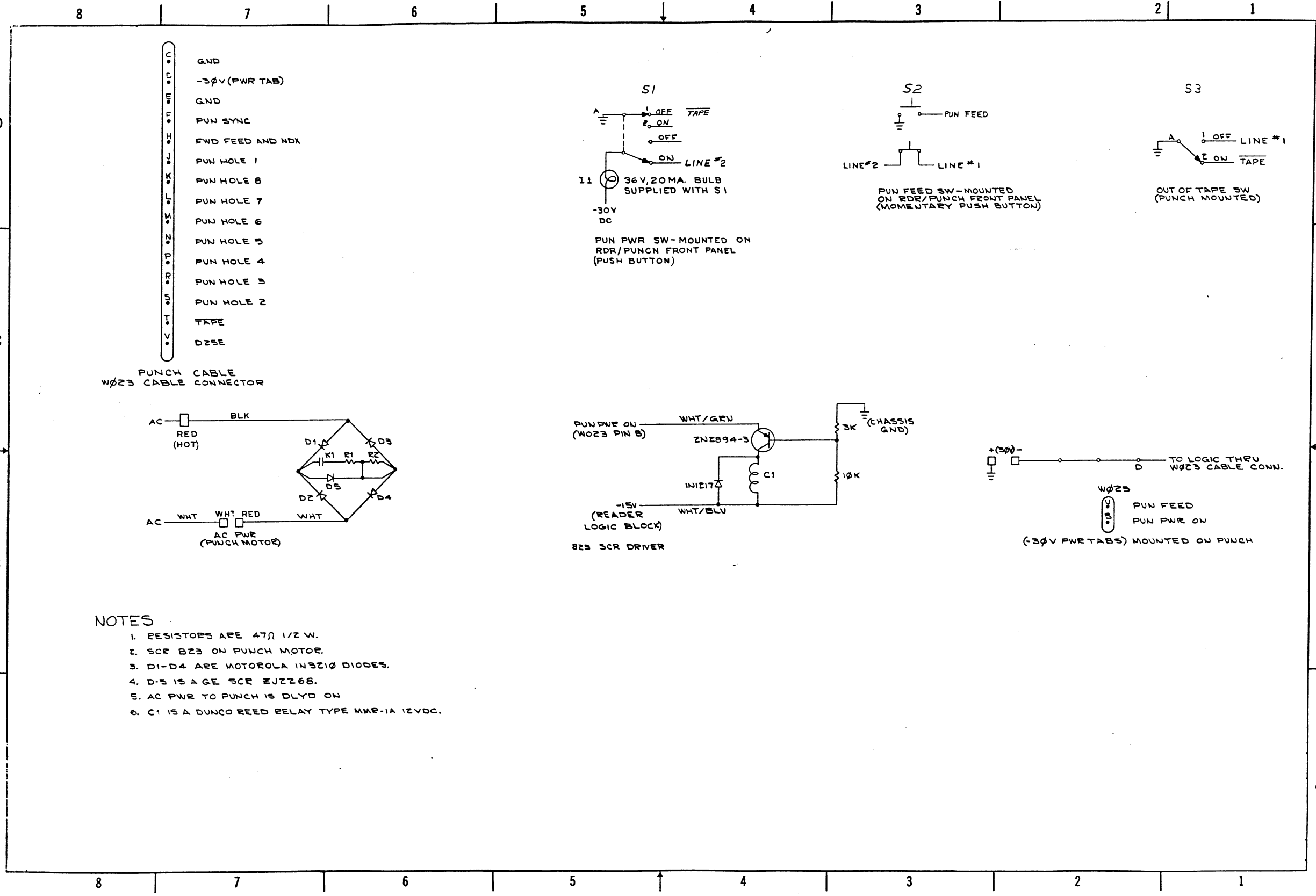


NL REF NO
018-2

D-BS-KD09-A-8 Read-In-Mode



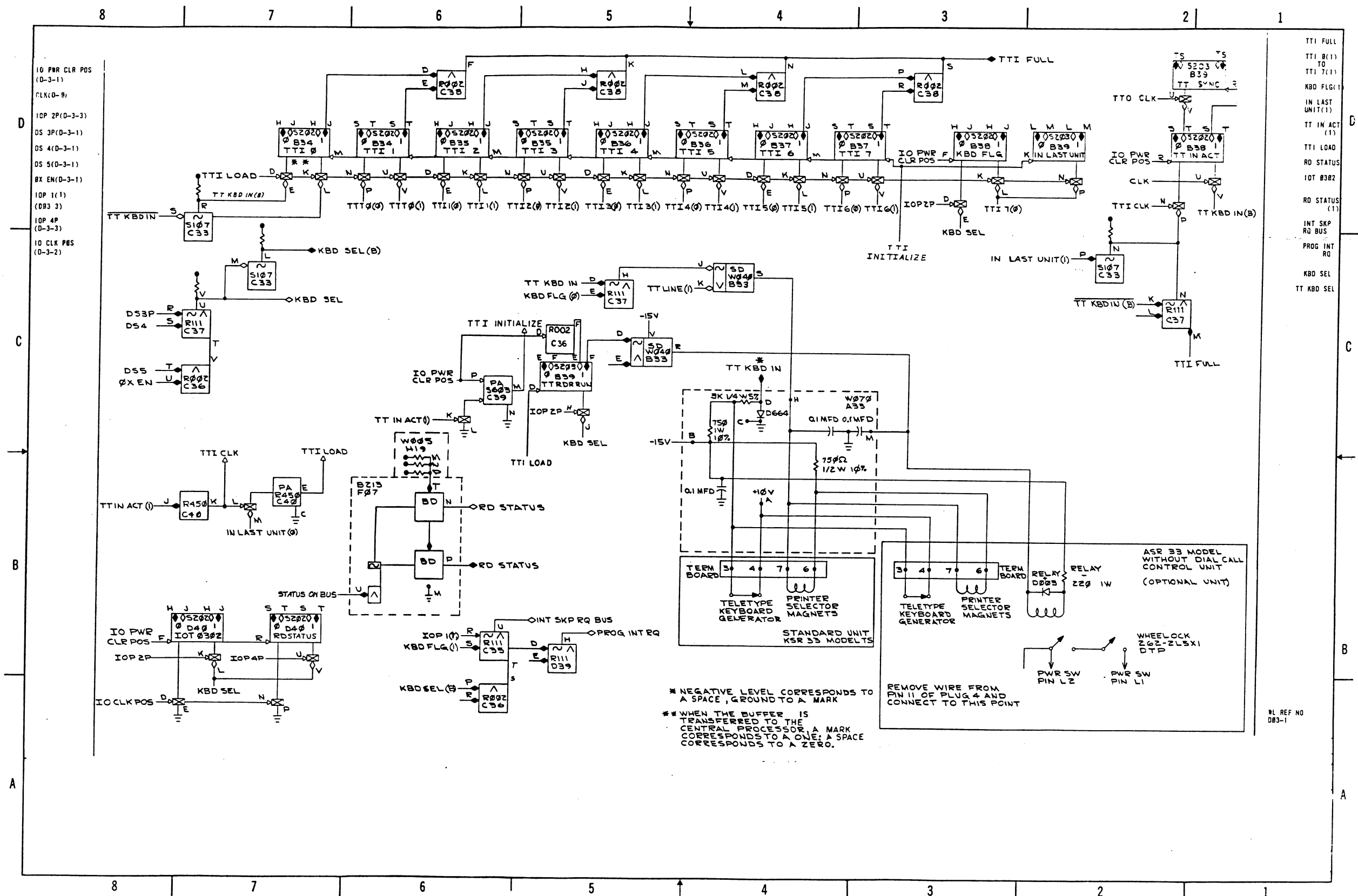
D-BS-KD09-A-9 Reader Control (Sheet 2)



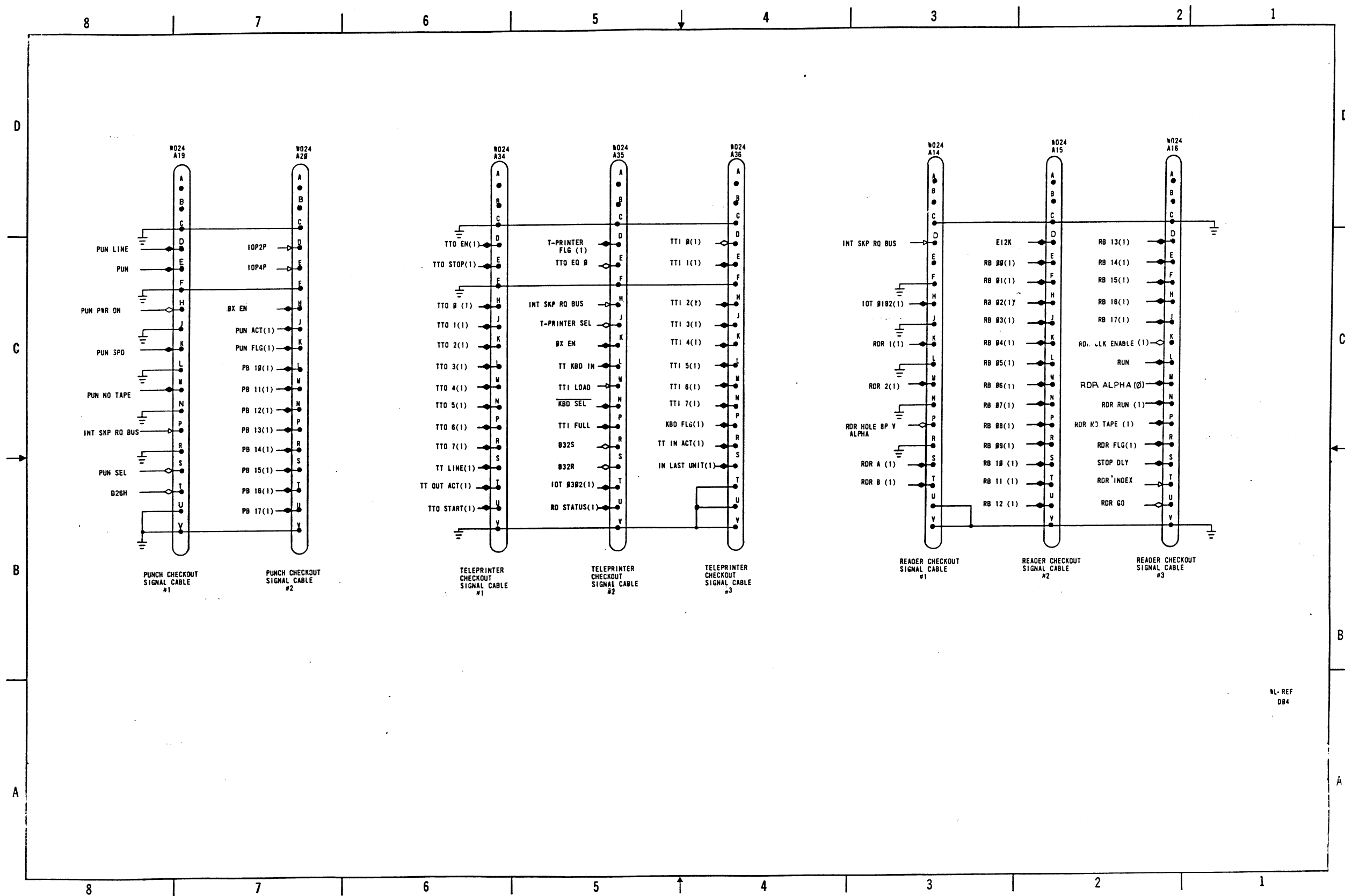
PUNCH CABLE
W023 CABLE CONNECTOR

- NOTES
1. RESISTORS ARE 47Ω 1/2 W.
 2. SCR BZ3 ON PUNCH MOTOR.
 3. D1-D4 ARE MOTOROLA 1N3210 DIODES.
 4. D-5 IS A GE SCR ZJ2268.
 5. AC PWR TO PUNCH IS DLYD ON
 6. C1 IS A DUNCO REED RELAY TYPE MMR-1A 12VDC.

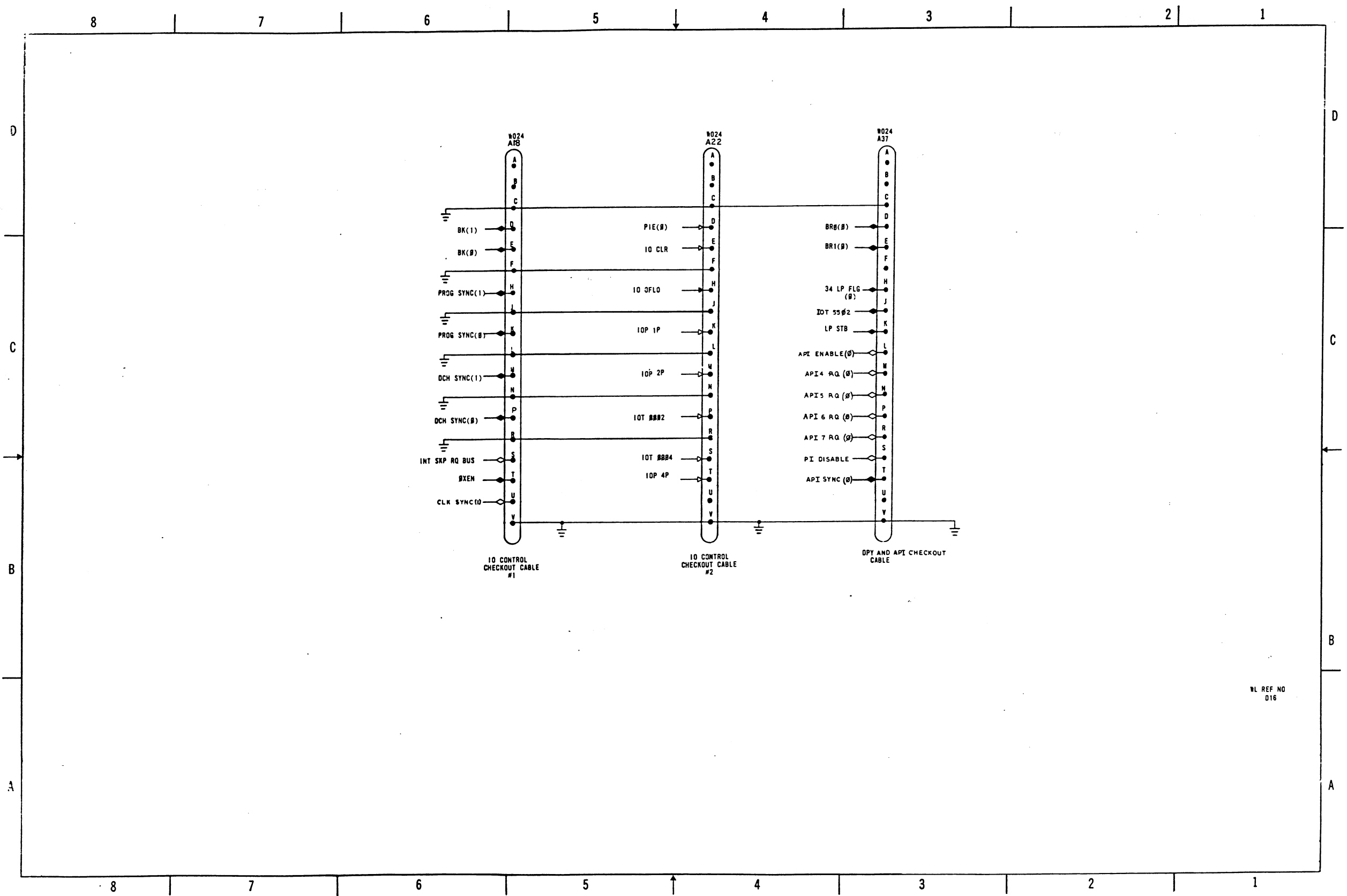
D-BS-KD09-A-10 Punch Control (Sheet 2)



D-BS-KD09-A-11 Teletype Control (Sheet 1)



D-IC-KD09-A-12 IO Checkout Cables (Sheet 1)



WL REF NO
016

D-IC-KD09-A-12 IO Checkout Cables (Sheet 2)

PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION		DEC. STOCK NO.
			ITEM	STOCK SIZE — CAT. NO. — MFG.	
		8	B213	- FLIP FLOP	
		2	B301	- DELAY (ONE SHOT)	
		1	G903	CLOCK ACCELERATOR	
		10	R002	- DIODE CLUSTER	
		22	R111	- DIODE GATE	
		19	R141	- DIODE GATE	
		4	R302	- DELAY (ONE SHOT)	
		1	R303	- INTEGRATING ONE SHOT	
		1	R401	- CLOCK	
		1	R450	VARIABLE CLOCK	
		14	S107	INVERTER	
		24	S202	- DUAL FLIP FLOP	
		8	S203	- TRIPLE FLIP FLOP	
		7	S205	- DUAL FLIP FLOP	
		7	S602	- PULSE AMPLIFIER	
		4	S603	- PULSE AMPLIFIER	

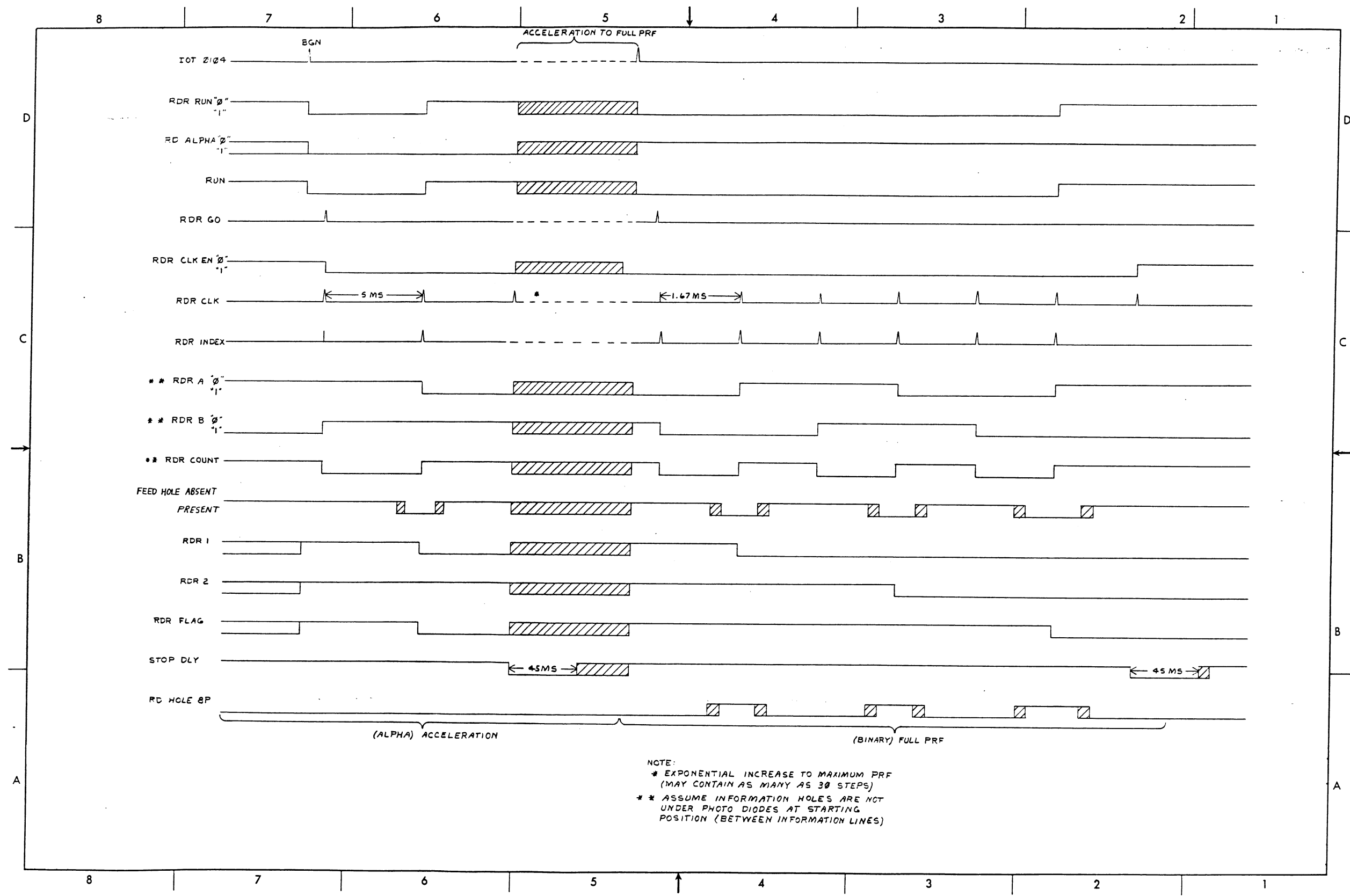
A-PL-KD09-A-14 Module Parts List (Sheet 1)

PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION		DEC. STOCK NO.
			ITEM	STOCK SIZE — CAT. NO. — MFG.	
		7	W005	- CLAMPED LOAD	
		1	W021	- SIGNAL CABLE CONN.	
		2	W023	- CONNECTOR BOARD	
		11	W024	- CONNECTOR BOARD	
		13	W031	- SIGNAL CABLE CONN	
		6	W040	- SOLENOID DRIVER	
		7	W990	- INDICATOR DRIVER	
		1	W070	- TELETYPE CONNECTOR	
		4	W071	- POWER CONNECTOR	
		1	W501	- SCHMITT TRIGGER	
		1	W520	- COMPARATOR	
		3	W612	- PULSE AMPLIFIER	
		10	W033	SIGNAL CABLE CONN.	
		6	R123	DIODE GATE	

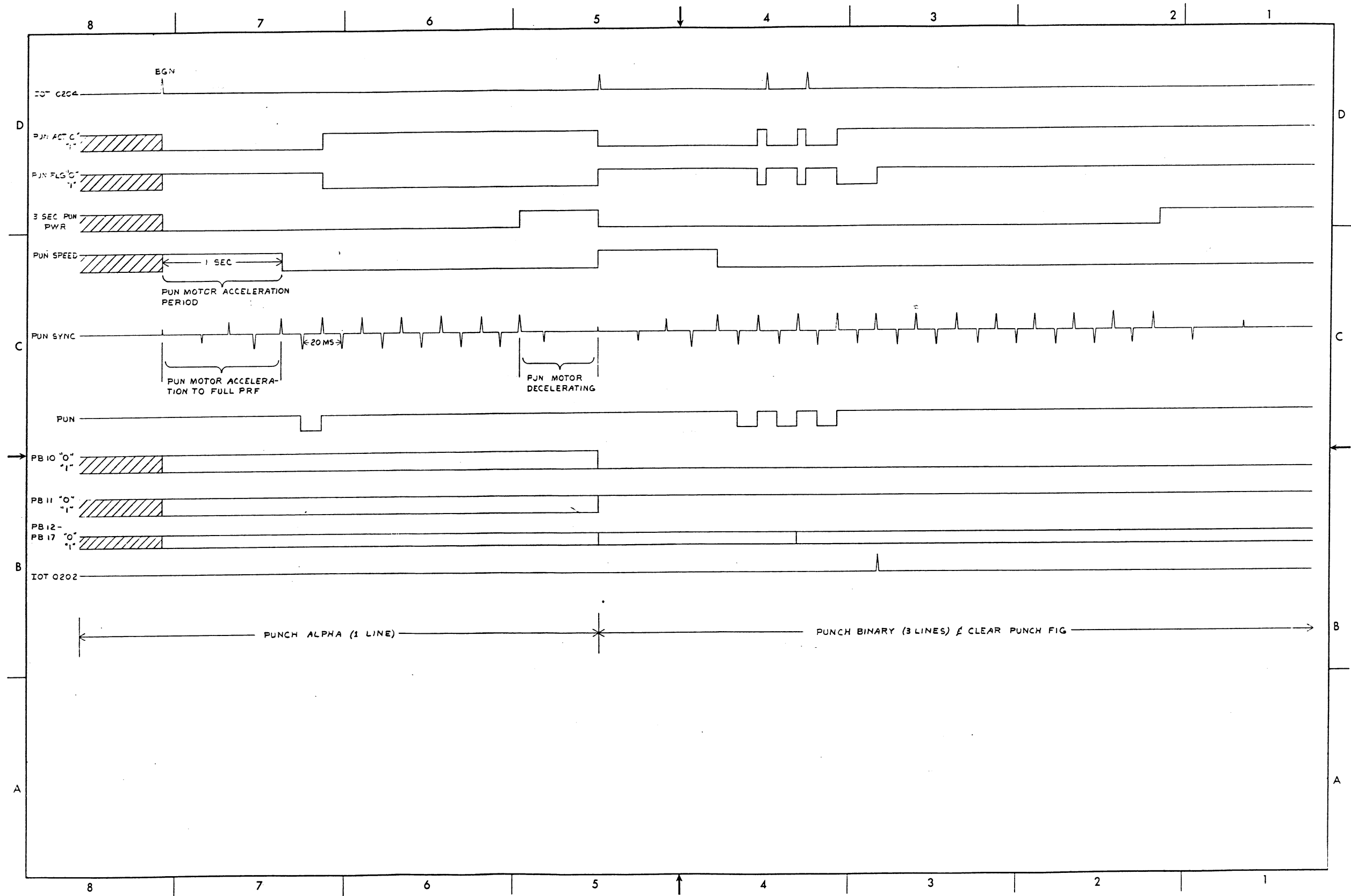
A-PL-KD09-A-14 Module Parts List (Sheet 2)

COMPONENT NAME	VALUE	POL.	FROM PIN	TO PIN	POL.
CAPACITOR	2.2 MF TAND ± 10%	-	C25H	C25J	+
RESISTOR	2.7K ±5% 1/4W		C25J	C25L	
CAPACITOR	.01 MFD	-	D25E	D25C	+
RESISTOR	4.7K ±10% 1/4W		D26K	D26B	
RESISTOR	10K 1/4W ± 10%		A21T	B21B	
CAPACITOR	175 MFD TAND ± 10%	-	C27J	C27C	+
RESISTOR	20K 1/4W ± 5%		C27P	C27S	
CAPACITOR	39 MFD 10V THND ± 10%	-	C25R	C25S	+
RESISTOR	24K 1/4W ± 5%		C25S	C25U	
CAPACITOR	.02 MFD 50V	-	A24H	A24J	+
RESISTOR	3K 1/4W ± 5%		F05J	F05L	
RESISTOR	1.5K 1/4W		A17V	B17B	
RESISTOR	1K 1/4W ± 10%		A24J	A24L	
RESISTOR	3K 1/4W ± 5%		D21P	D21B	
CAPACITOR	120PF ± 5%		E40J	E40K	
* PRE API SYNC	JUMPER		J10S	J10C	
** 34 DISPLAY	JUMPER		F40T	F40C	
** REMOVE JUMPERS WHEN 34 DISPLAY INSTALLED.					
* REMOVE JUMPERS WHEN API INSTALLED.					

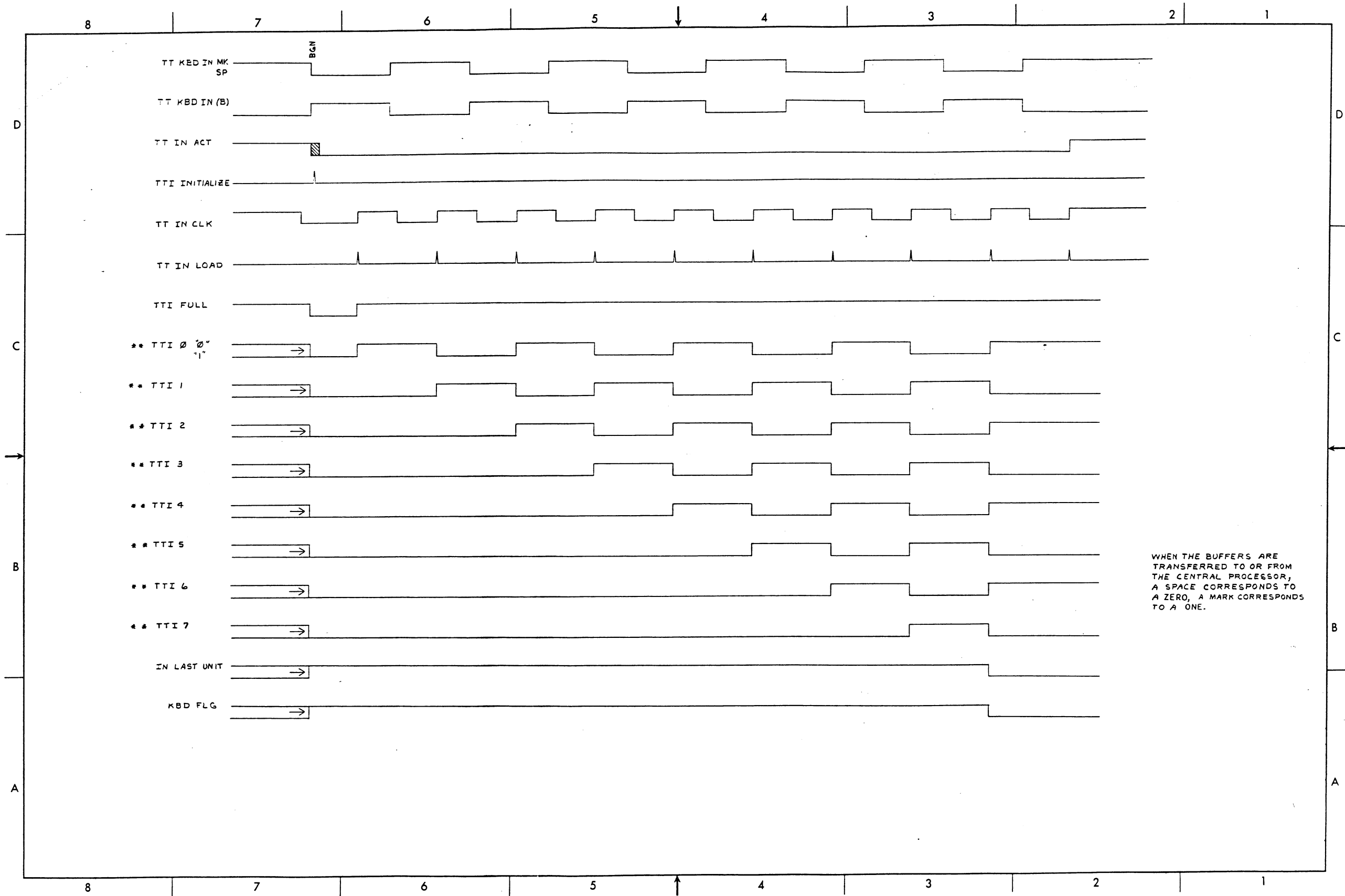
A-CP-KD09-A-16 External Component List



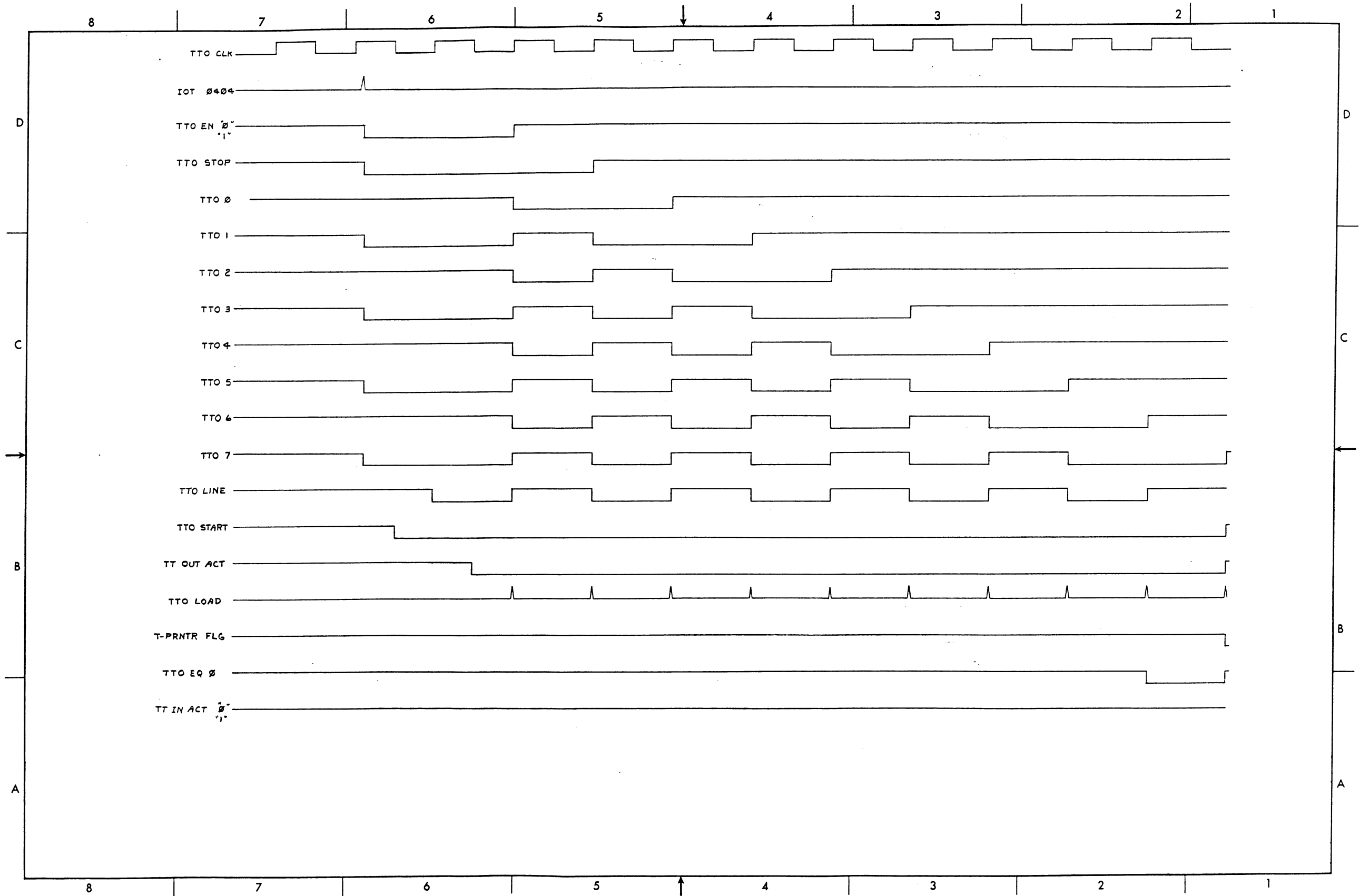
D-TD-KD09-A-20 Reader Timing



D-TD-KD09-A-21 Punch Timing



D-TD-KD09-A-22 Teletype Timing (Sheet 1)



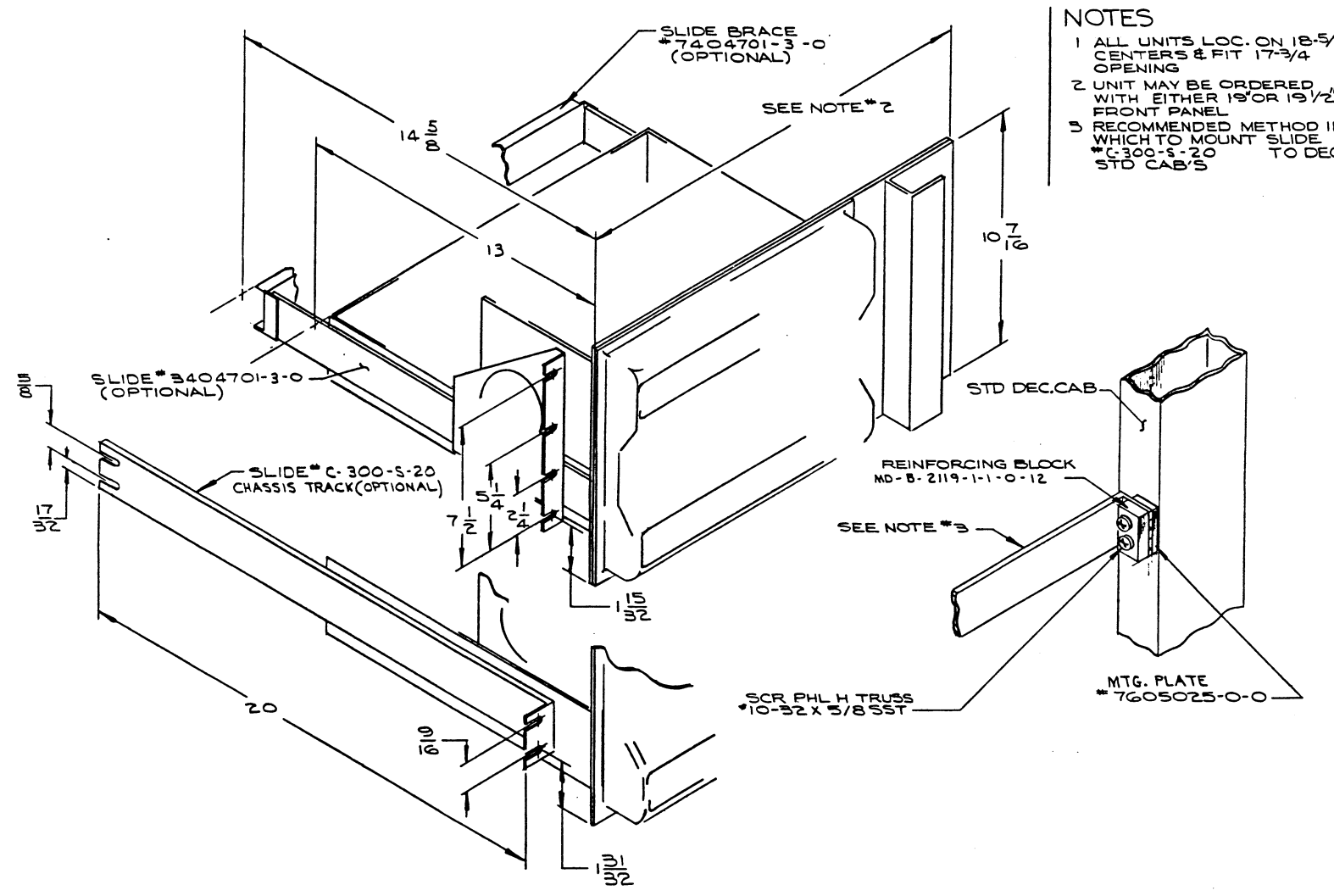
D-TD-KD09-A-22 Teletype Timing (Sheet 2)

COLOR	NAME	PIN	PIN	REMARKS
BUSS BAR	+10A	A01A	A02A	
↓		A02A	A03A	
		A03A	A04A	
BUSS BAR	+10B	B01A	B02A	
↓		B02A	B03A	
		B03A	B04A	
BUSS BAR	-15A	A01B	A02B	
↓		A02B	A03B	
		A03B	A04B	
BUSS BAR	-15B	B01B	B02B	
↓		B02B	B03B	
		B03B	B04B	
BUSS BAR	GROUND A	A01C	A02C	
↓		A02C	A03C	
		A03C	A04C	
BUSS BAR	GROUND B	B01C	B02C	
↓		B02C	B03C	
		B03C	B04C	
BUSS BAR	-30 A	A03V	A04V	
	-30 B	B03V	B04V	
	POWER A	A03E	A04E	
	POWER B	B03E	B04E	
	FEED HOLE F INPUT	B01D	B02D	
	8	B01E	B02E	
↓	7	B01F	B02F	

A-WL-PC01-0-1 Reader Block Wiring List (Sheet 1)

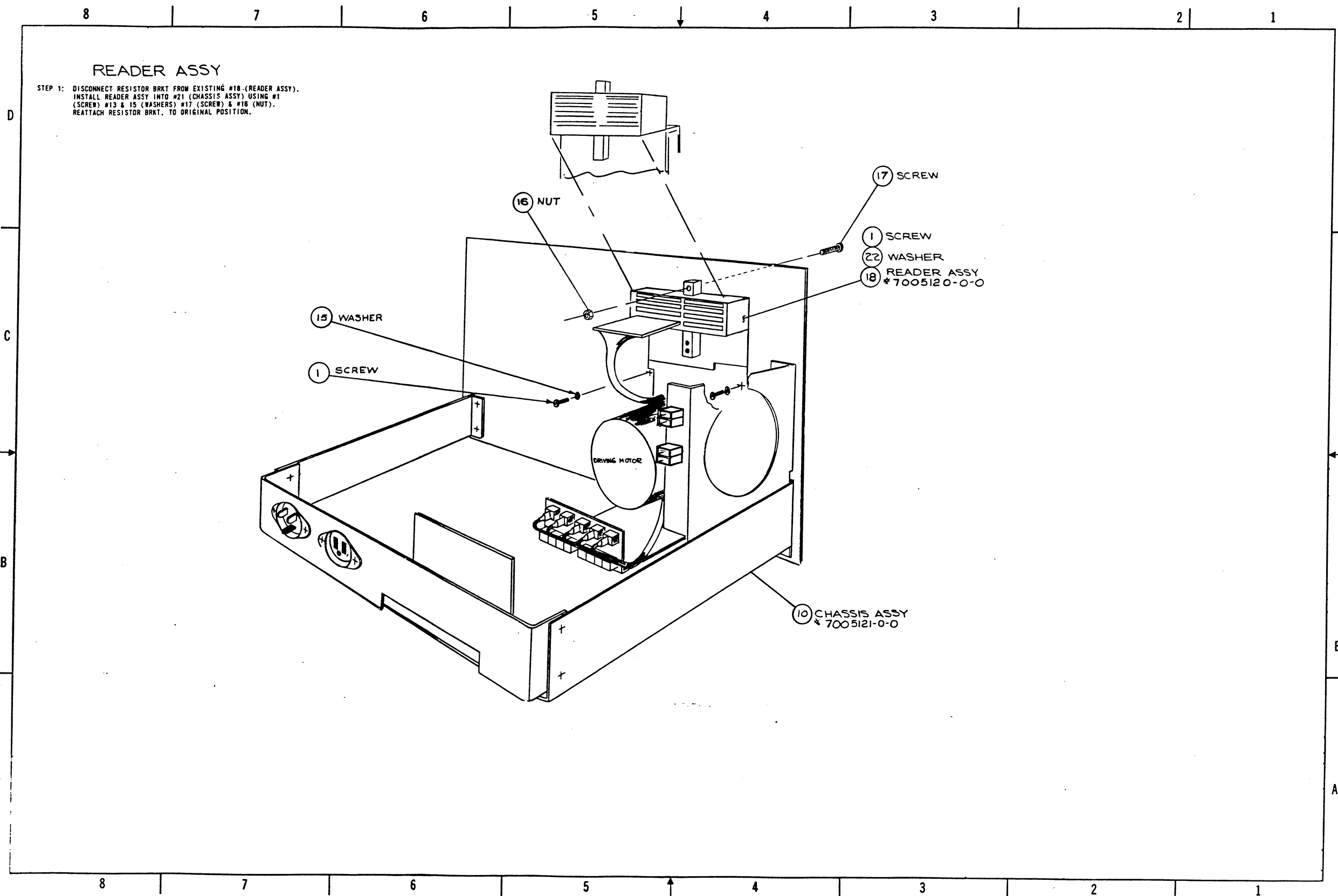
COLOR	NAME	PIN	PIN	REMARKS
BUSS BAR	HOLE 6 INPUT	B01H	B02H	
	5	B01J	B02J	
	4	B01K	B02K	
	3	B01L	B02L	
	2	B01M	B02M	
	1	B01N	B02N	
	COMMON	B01P	B02P	
	HOLE 1 OUTPUT	A01D	A02D	
	2	A01E	A02E	
	3	A01F	A02F	
	4	A01H	A02H	
	5	A01J	A02J	
	6	A01K	A02K	
	7	A01L	A02L	
	8	A01M	A02M	
	FEED HOLE OUT	A01N	A02N	
#22 AWG YEL	A(0)	A01P	A04D	
		A04D	A04K	
	A(1)	A01R	A03D	
		A03D	A03K	
	B(0)	A01S	B04D	
		B04D	B04K	
	B(1)	A01T	B03D	
		B03D	B03K	

A-WL-PC01-0-1 Reader Block Wiring List (Sheet 2)

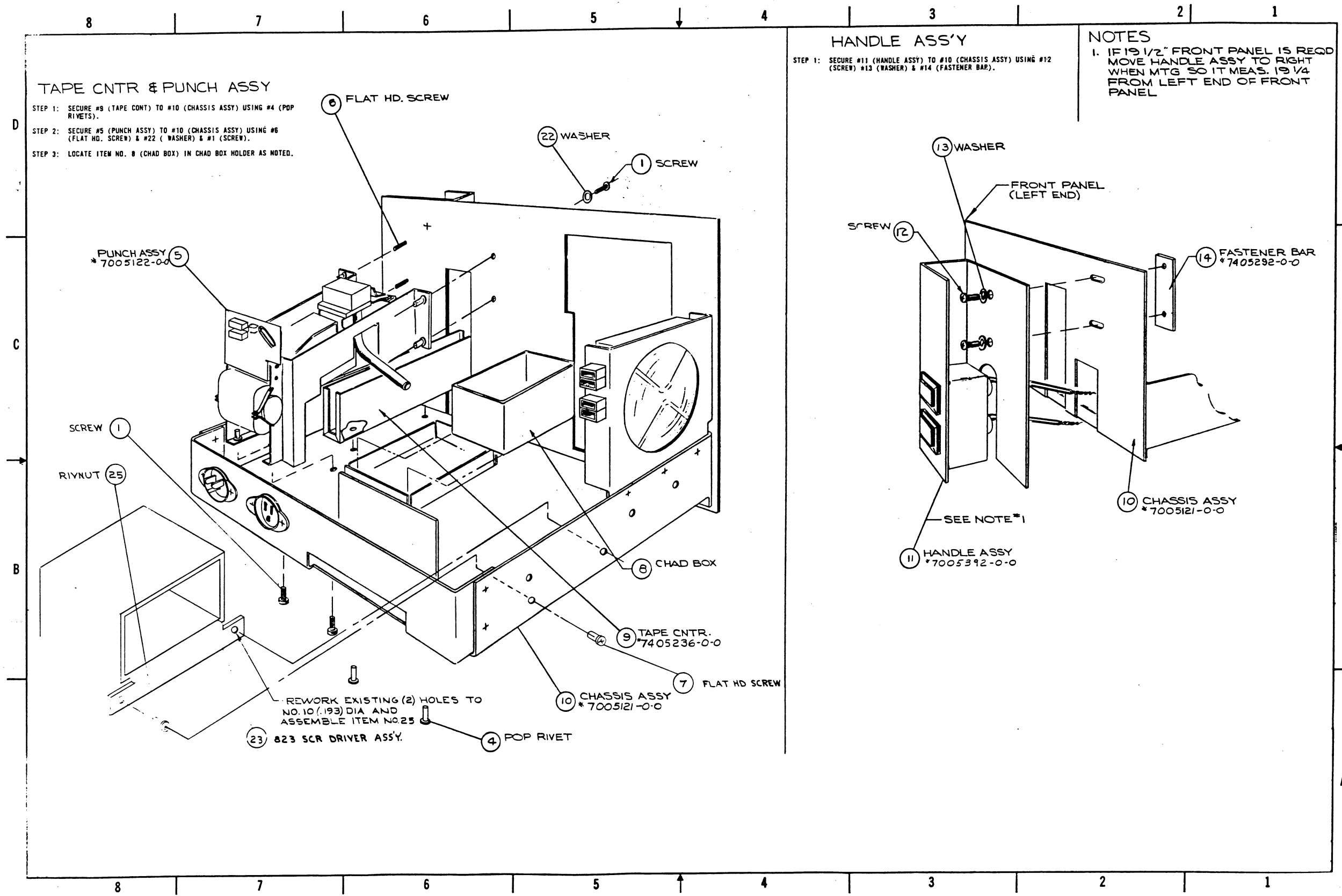


- NOTES
- 1 ALL UNITS LOC. ON 18-5/16 CENTERS & FIT 17-3/4 OPENING
 - 2 UNIT MAY BE ORDERED WITH EITHER 19" OR 19 1/2" FRONT PANEL
 - 3 RECOMMENDED METHOD IN WHICH TO MOUNT SLIDE #C-300-S-20 TO DEC STD CAB'S

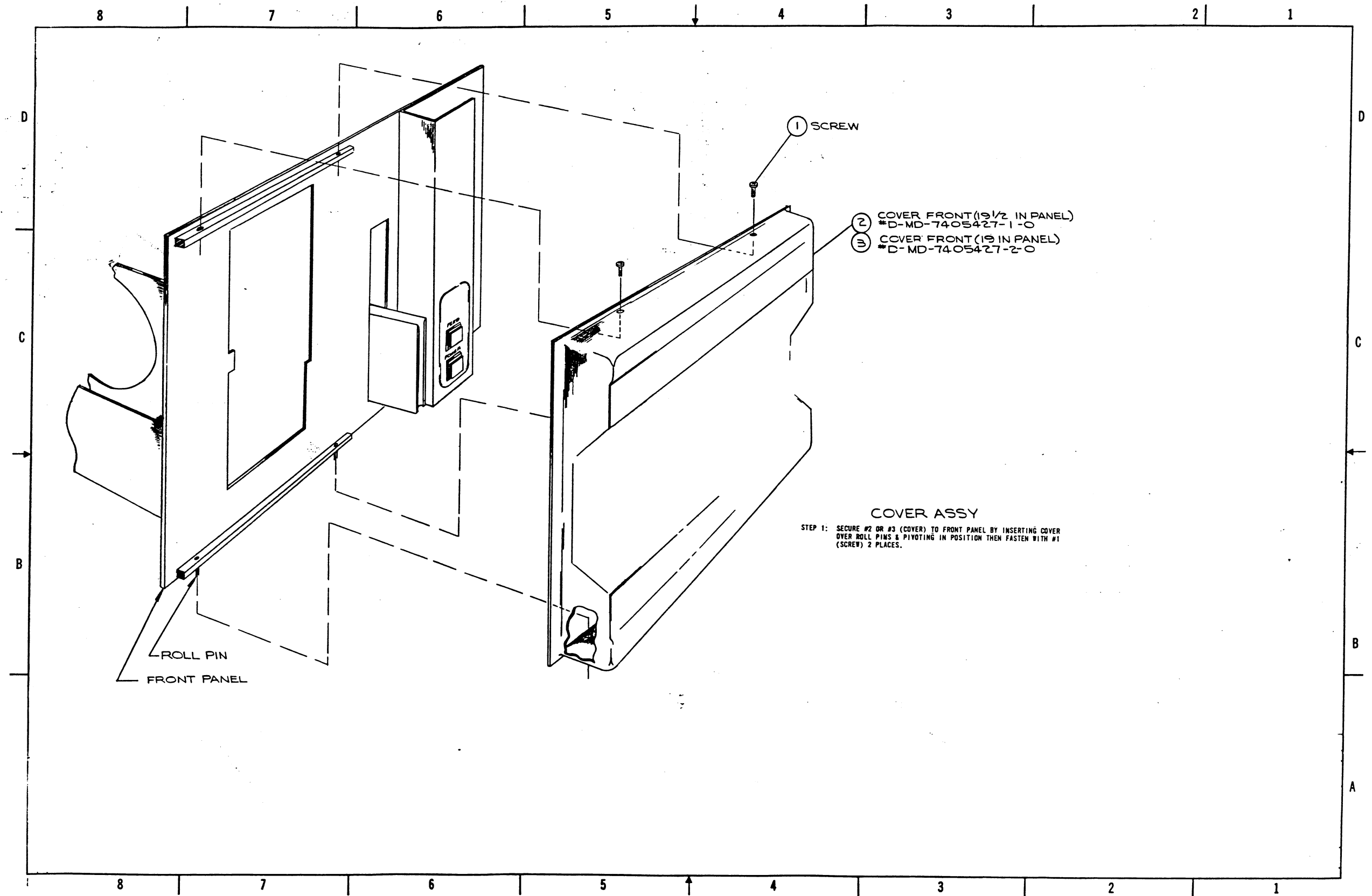
C-OD-PC01-0-4 Reader Outline Drawing



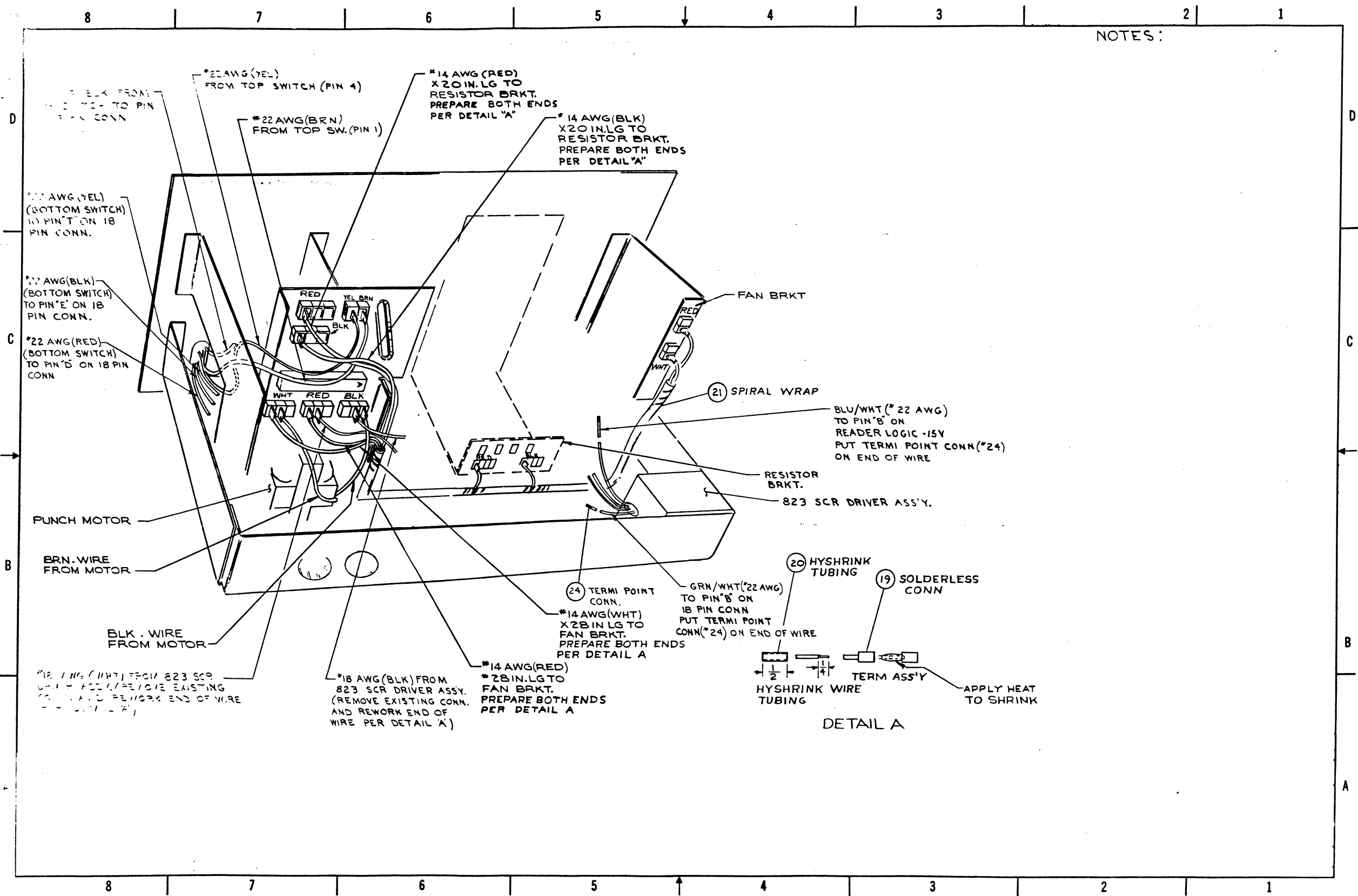
D-UA-PC09-0-0 Reader Punch Unit Assembly (Sheet 1)



D-UA-PC09-0-0 Reader Punch Unit Assembly (Sheet 2)



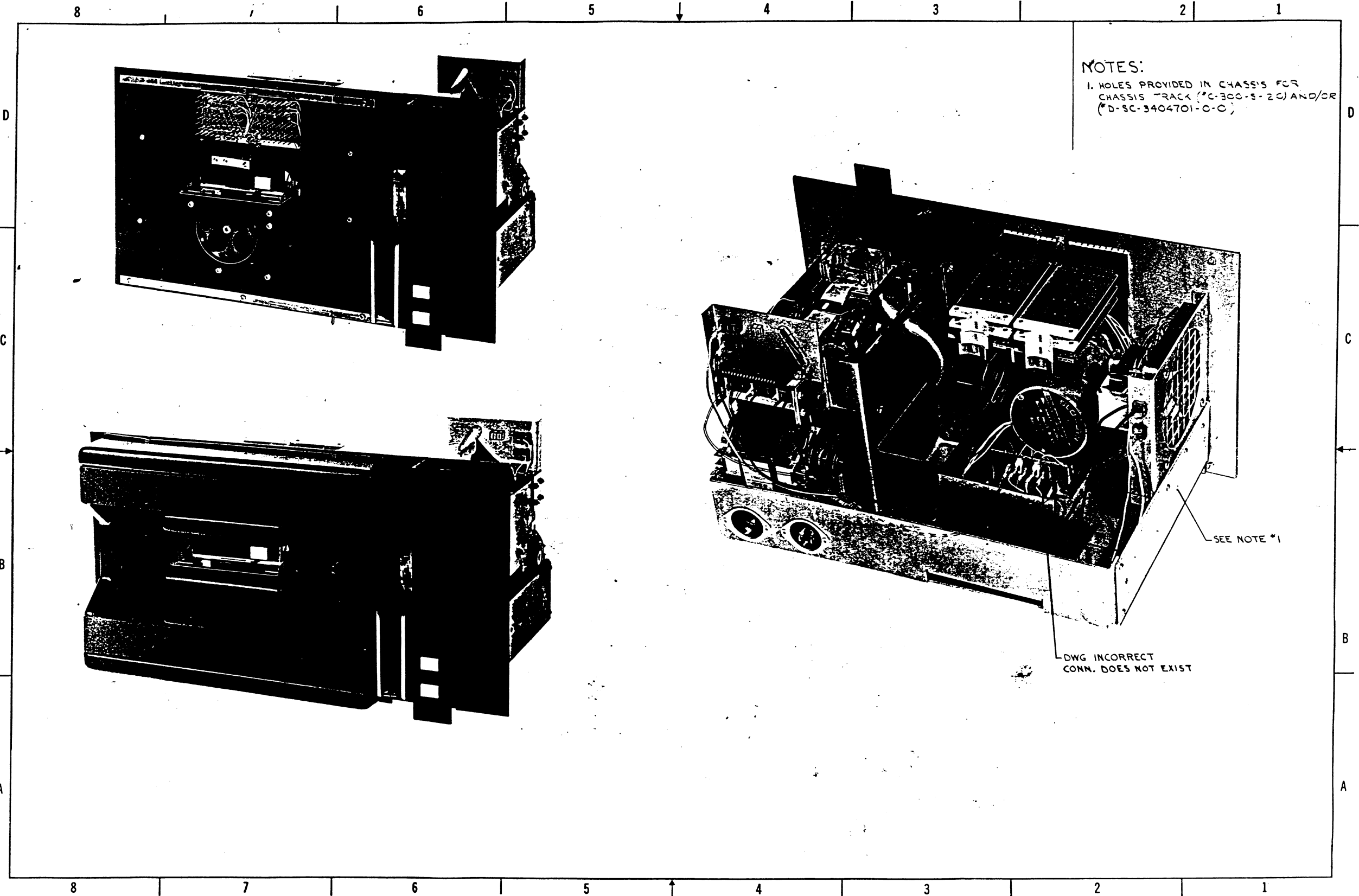
D-UA-PC09-0-0 Reader Punch Unit Assembly (Sheet 3)



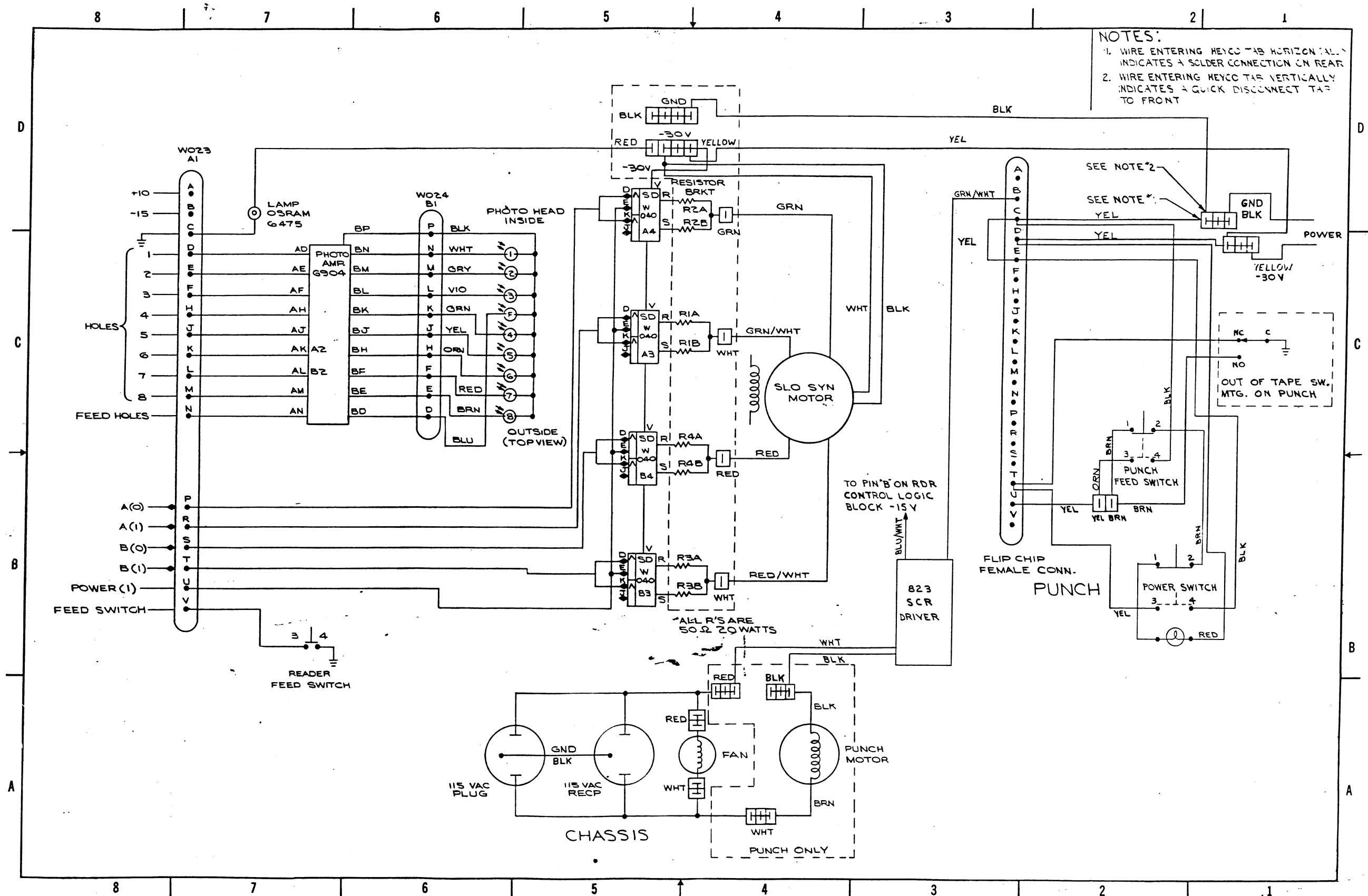
NOTES:

- *22 AWG (YEL) FROM TOP SWITCH (PIN 4)
- *14 AWG (RED) X 20 IN. LG TO RESISTOR BRKT. PREPARE BOTH ENDS PER DETAIL "A"
- *14 AWG (BLK) X 20 IN. LG TO RESISTOR BRKT. PREPARE BOTH ENDS PER DETAIL "A"
- *22 AWG (BRN) FROM TOP SW. (PIN 1)
- *22 AWG (YEL) (BOTTOM SWITCH) TO PIN "D" ON 18 PIN CONN.
- *22 AWG (BLK) (BOTTOM SWITCH) TO PIN "E" ON 18 PIN CONN.
- *22 AWG (RED) (BOTTOM SWITCH) TO PIN "S" ON 18 PIN CONN.
- FAN BRKT
- (21) SPIRAL WRAP
- BLU/WHT (*22 AWG) TO PIN "B" ON READER LOGIC -15V. PUT TERMI POINT CONN (*24) ON END OF WIRE
- RESISTOR BRKT.
- 823 SCR DRIVER ASS'Y.
- PUNCH MOTOR
- BRN. WIRE FROM MOTOR
- BLK. WIRE FROM MOTOR
- (24) TERMI POINT CONN.
- *14 AWG (WHT) X 28 IN LG TO FAN BRKT. PREPARE BOTH ENDS PER DETAIL A
- GRN/WHT (*22 AWG) TO PIN "B" ON 18 PIN CONN. PUT TERMI POINT CONN (*24) ON END OF WIRE
- (20) HYSHRINK TUBING
- (19) SOLDERLESS CONN
- *18 AWG (BLK) FROM 823 SCR DRIVER ASSY. (REMOVE EXISTING CONN. AND REWORK END OF WIRE PER DETAIL "A")
- *14 AWG (RED) * 28 IN. LG TO FAN BRKT. PREPARE BOTH ENDS PER DETAIL "A"
- HYSHRINK WIRE TUBING
- TERM ASS'Y
- APPLY HEAT TO SHRINK
- *14 AWG (WHT) FROM 823 SCR DRIVER ASSY. (REMOVE EXISTING CONN. AND REWORK END OF WIRE PER DETAIL "A")

D-UA-PC09-0-0 Reader Punch Unit Assembly (Sheet 4)



D-UA-PC09-0-0 Reader Punch Unit Assembly (Sheet 5)

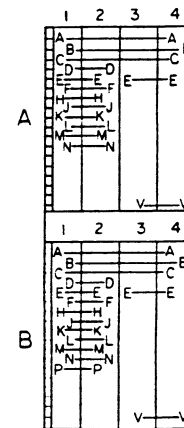


NOTES:
 1. WIRE ENTERING KEYCO TAB HORIZONTALLY INDICATES A SOLDER CONNECTION ON REAR.
 2. WIRE ENTERING KEYCO TAB VERTICALLY INDICATES A QUICK DISCONNECT TAB TO FRONT.

D-BS-PC09-0-2 Reader and Punch Block Schematic

	A	B
4	W040	W040
3	W040	W040
2	PHOTO AMPLIFIER (OUTPUT) G904 (INPUT)	
1		W024A PHOTO HEAD

B-MU-7005120-0-1 Reader Module Utilization List



B-AD-7005160-0-0 Reader Bus Bar