EK-VT18X-TM-001

VT180
SERIES
TECHNICAL MANUAL

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PREFACE

This manual contains information needed by a service engineer or technician to install, operate, test, and repair the VT180 to the field replaceable unit level. Included are explanations of the features, options, capabilities, and technical characteristics of the VT180 as well as general reference data. The information is presented in seven chapters and three appendices.

Chapter 1 of this manual contains VT180 specifications and documentation ordering information.

Chapter 2 provides basic operator information, including use of the keyboard, use of set-up modes for setting or changing terminal characteristics, and simple troubleshooting using the audio and visual indicators.

Chapter 3 provides the installation, start-up, and system checkout procedures as well as interface information.

Chapter 4 provides guidance for using the CP/M® operating system.

Chapter 5 describes the procedure for setting the transmission characteristics of the serial ports.

Chapter 6 contains a technical description of the basic VT100 and the VT18X personal computing option.

Chapter 7 provides information needed to service the VT180. This includes module configuration, testing, troubleshooting, adjustments, and removal and installation of module and mechanical assemblies.

Appendix A contains programming information for the VT180 series, including interface timing considerations and descriptions of control functions the VT180 responds to, both in ANSI mode and Digital VT52-compatible mode.

Appendix B provides a recommended spares list.

Appendix C contains a glossary of terms, acronyms, and abbreviations used in this manual.

In the examples of dialog between the operator and the computer, the dialog the operator types is underlined.

CHAPTER 1
INTRODUCTION AND SPECIFICATIONS

1.1 GENERAL DESCRIPTION

The VT180 series of video terminals is a group of personal office computers designed to function in two, quickly accessible operational modes.

1. In computer mode the VT180 operates like a personal computer.

2. In terminal mode the VT180 emulates a VT100 video terminal and can be used as a remote terminal to an external host computer.

The VT180 has the software functionality and features of a VT100 when it is used in terminal mode. If the VT180 is used in computer mode, it will run CP/M prepackaged application programs. It will also offer the user a choice of several programming languages for the development of unique programs.

The VT180 provides local mass memory storage through a dual disk drive. Two more disk drives may be added as an option if more mass storage capacity is needed.

Information and control signals are routed between the VT180, the host computer, and a variety of external devices by four external input/output ports (multipin connectors). The four external ports are:

1. The disk drive port
2. The communications port
3. The printer port
4. The general purpose serial port.

The disk drive port is dedicated to communications between the VT180 processor and the disk drives. The other three ports permit the VT180 processor, when running the proper application programs, to communicate with the host computer and external devices. Among these devices are printers, acoustic couplers, modems, paper tape readers and punches, magnetic cassette and cartridge drives, X-Y plotters, and laboratory instruments.

A fifth port, the console port, is an internal port that permits the VT180 processor to communicate with the terminal keyboard and video screen. This is the port through which CP/M normally routes the system dialog.

1.2 PHYSICAL DESCRIPTION

The VT180 personal office computer consists of three basic units: the VT180 terminal, a detachable keyboard, and a dual disk drive. Figure 1-1 shows these basic units.

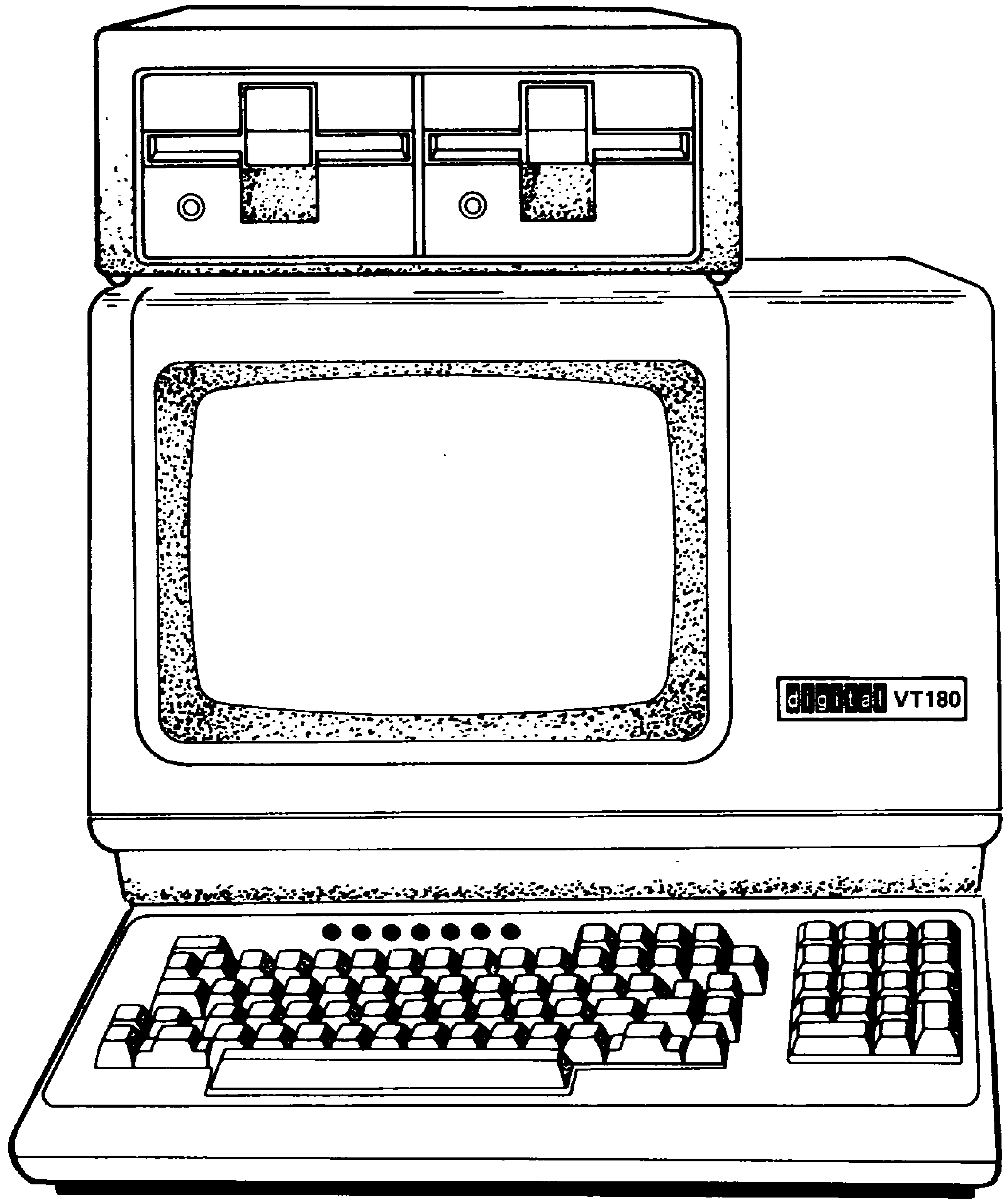


Figure 1-1 The VT180 Personal Office Computer

The VT180 terminal contains the following basic subunits and optional subunits.

1. Basic subunits

   - CRT video monitor
   - Power supply
   - Backplane, wire frame, and radio frequency (RF) shield
   - Terminal controller module
   - CP/M processor module (VT18X control module)
   - VT180 paddle board

2. Optional subunits

   - Advanced video option (AVO)
   - Additional dual disk drive

The keyboard is a replaceable unit of the VT180. It is connected to the rear of the terminal cabinet by an attached, three-conductor power and signal cable. The main keyboard contains a key arrangement similar to an ordinary typewriter. In addition to the standard typewriter keys, there are special function keys that permit the user to generate escape sequences, control sequences, and cursor control commands. The main keyboard also contains seven LED indicators, which show the current terminal status. A keypad placed next to the main keyboard contains a second set of numeric keys and special function keys. The numeric keys duplicate the numeric keys on the main keyboard and are useful for certain number-handling programs. A small speaker mounted inside the keyboard case provides audio feedback and attention signals (keyclicks and bells) for the user.

The two disk drives of the basic VT180 are installed in a mounting box that contains the power supply for the drives. The power switch for the drives is located on top of the mounting box. Input/output control and data signals appear on two EIA connectors located on the rear of the mounting box. One connector is used to connect the disk drives to the rear of the VT180 terminal. The second connector is used when the system is expanded with an additional disk drive unit.

1.3 VT180 SPECIFICATIONS

1.3.1 System Physical Dimensions

One or two RX180 disk drives may be installed on the top of the monitor or next to either side of the monitor. The overall dimensions of the various system configurations are listed in Table 1-1.

Table 1-1 System Configuration Dimensions

Configuration	Width	Height	Depth
One RX180 on the top of the monitor	45.72 cm (18.00 in)	47.62 cm (18.75 in)	57.78 cm (22.75 in)
Two RX180s on the top of the monitor	45.72 cm (18.00 in)	58.42 cm (23.00 in)	57.78 cm (22.75 in)
One or two RX180s on the side of the monitor	79.37 cm (31.25 in)	36.83 cm (14.50 in)	57.78 cm (22.75 in)

1.3.2 Unit Physical Dimensions

Table 1-2 lists the dimensions and weight of each component of the VT180.

Table 1-2 Physical Specifications of Components

Component	Height	Width	Depth	Weight	Minimum Table Depth
Monitor	36.83 cm (14.5 in)	45.72 cm (18 in)	36.20 cm (14.25 in)	13.6 kg (30 lb)	NA*
Keyboard	8.89 cm (3.5 in)	45.72 cm (18 in)	20.32 cm (8 in)	2.0 kg (4.5 lb)	51.4 cm (20.25 in)
Dual Disk Drive RX180	10.79 cm (4.25 in)	33.49 cm (13.19 in)	30.32 cm (11.94 in)	7.3 kg (16 lb)	NA*

*NA = Not applicable

1.3.3 Environmental Specifications

Operating Specifications

Temperature	10° C (50° F) to 40° C (104° F)
Relative humidity	10% to 90%
Maximum wet bulb	28° C (82° F)
Minimum dew point	2° C (36° F)
Altitude	2.4 km (8,000 ft)

Nonoperating Specifications

Temperature	–40° C (–40° F) to 66° C (150.8° F)
Relative humidity	0% to 95%
Altitude	9.1 km (30,000 ft)

1.3.4 Electrical Specifications

Line voltage (Single-phase, two-wire) (Switch-selectable)	95 Vrms to 128 Vrms 187 Vrms to 268 Vrms
Line frequency	50 Hz operation = 49–51 Hz 60 Hz operation = 59–61 Hz
Current	3.0 Arms maximum at 115 Vrms 1.5 Arms maximum at 230 Vrms

1.4 VIDEO DISPLAY CHARACTERISTICS

CRT	30 cm (12 inch diagonal measure, P4 phosphor)
Format	24 lines of 80 characters or 14 lines of 132 characters (selectable)

Character	7 dot by 9 dot matrix with descenders
Character size	
80-column mode 132-column mode	3.35 mm by 2.0 mm (0.132 in by 0.078 in) 3.35 mm by 1.3 mm (0.132 in by 0.051 in)
Active display size	203 mm by 127 mm (8 in by 5 in)
Character set	96-character ASCII subset (upper- and lowercase, numbers, and punctuation)
Cursor type	Keyboard-selectable, blinking block character or blinking underline

1.5 KEYBOARD

General	83-key detachable unit with a 1.9 m (6 ft) coiled cord attached
Key layout	65-key arrangement and sculpturing similar to a standard typewriter; with 18-key numeric keypad
Numeric keypad	18-key with period, comma, minus, enter, and four general purpose function keys
Visual indicators	Seven LEDs; three are dedicated — ON-LINE, LOCAL, and KBD LOCKED; four are user-programmable

1.6 AUDIBLE SIGNALS

Keyclick	Sound simulates a typewriter
Bell	Sounds upon receipt of BEL code; sounds eight characters from the right margin (keyboard-selectable)
Multiple bell	Sounds upon detection of an error in set-up save or recall operation

1.7 COMMUNICATION CHARACTERISTICS

Type	EIA RS232
Speeds (Baud rate)	Full duplex: 50, 75, 110 (two stop bits), 134.5, 150, 200, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 9600, and 19,200
Code	ASCII
Character format	Asynchronous
Character size	Seven or eight bits; keyboard-selectable (If 8-bit characters are selected, the eighth bit is always space.)

Parity	Even, odd, or none (keyboard-selectable)
Synchronization	Keyboard-selectable via automatic generation of XON and XOFF control codes

1.8 DISK DRIVE CHARACTERISTICS

Performance

Rotational speed	300 r/min nominal
Access time	
Track to Track Average	25 ms maximum
Average	335 ms maximum
Settling time	20 ms maximum
Track density	48 tracks/in (TPI)
Number of tracks	40
Recording density	2768 bits/in (BPI)
Transfer rate	125K bytes/s
Latency (average)	100 ms
Sectoring	Soft
Head load time	50 ms maximum

Storage capacity (bytes MFM)

Unformatted (per disk)	250,000
Formatted	184,320
(nine records/track)	
Per track	4,608
Per sector	512

Error Rates (with SHUGART SA104 media or equivalent)

Soft read errors	1 per 10^9 bits read
Hard read errors	1 per 10^{12} bits read
Seek errors	1 per 10^6 seeks

Media Type

Industry standard flexible disk oxide on 0.08 mm (0.003 in) Mylar™	133.4 mm (5.25 in) square jacket

Mylar™ is a trademark of DuPont de Nemours & Company, Inc.

1.9 RELATED DOCUMENTATION

1.9.1 Digital Hardware and Software Documentation

The following is a list of Digital hardware and software documentation containing information of possible interest to users of the VT180 personal office computer.

Title	Document Number
VT180 Series Pocket Service Guide	EK-VT18X-PS
VT180 User's Guide	AA-M044A-TV
VT18X Unpacking Guide	EK-VT18X-PG
VT18X Upgrade and System Test Guide	ED-VT18X-IN
CP/M Reference Manual	AA-M054A-TV
Pocket Reference Card	EK-VT18X-RC

These documents can be ordered from:

Digital Equipment Corporation
Accessories and Supplies Group
P.O. Box CS2008
Nashua, New Hampshire 03061

1.9.2 Other Documentation

Title	Order From
Intel 8080 Microcomputer Systems User's Manual	Intel Corporation 3065 Bowers Avenue Santa Clara, California 95051
Zilog Z80 Technical Manual	Zilog, Inc. 10340 Bubb Road Cupertino, California 95014
EIA Specifications RS-232-C and RS-170	Electronic Industry Association EIA Engineering Department 2001 Eye Street, N.W. Washington, D.C. 20006
ANSI Standards X3.41-1974, X3.64-1977, 3.4-1977	Sales Department American National Standards Institute 1430 Broadway New York, N.Y. 10018

CHAPTER 2
OPERATING INFORMATION

2.1 INTRODUCTION
This chapter contains a general overview of how the VT180 operates and describes the VT180's controls and indicators. The basic terminal set-up and operating procedures are also described. Detailed operating information may depend on the computer software.

2.2 TERMINAL OPERATION
The VT180 terminal operates in either personal computer mode, on-line terminal mode, off-line (local) mode, or set-up mode. This section provides an overview of the four terminal modes.

The VT180 terminal is on-line when the ON-LINE indicator on the keyboard is on. While on-line, the VT180 can transmit and receive character codes from either the VT18X control module if in computer mode or the host computer if in terminal mode. Keyboard entries are placed in a keyboard character buffer until transmitted to either the VT18X control module or the host computer. Character codes received from the VT18X control module or host computer are placed in an input character buffer until processed. When processed, the received characters are taken from the buffer and displayed on the screen. Figure 2-1 is a general block diagram showing the transmitted and received data path between the keyboard, the VT18X control module or host computer, and the screen while the VT180 terminal is on-line. The solid lines show the data path with the VT180 terminal on-line and operating in personal computer mode.

When the LOCAL indicator is on, the VT180 terminal is off-line. While off-line, the terminal cannot transmit or receive character codes. The terminal is considered disconnected from the VT18X control module and the host computer. Therefore, character codes transmitted to the terminal while it is off-line are lost, although keyboard entries are displayed on the screen. Figure 2-2 is a general block diagram showing the data path between the keyboard and the screen while the VT180 terminal is off-line.

2.3 CONTROLS AND INDICATORS
The VT180 has many controls and indicators. They can be arranged in four groups: terminal monitor and disk drive power controls, keyboard controls, keyboard indicators, and audible indicators.

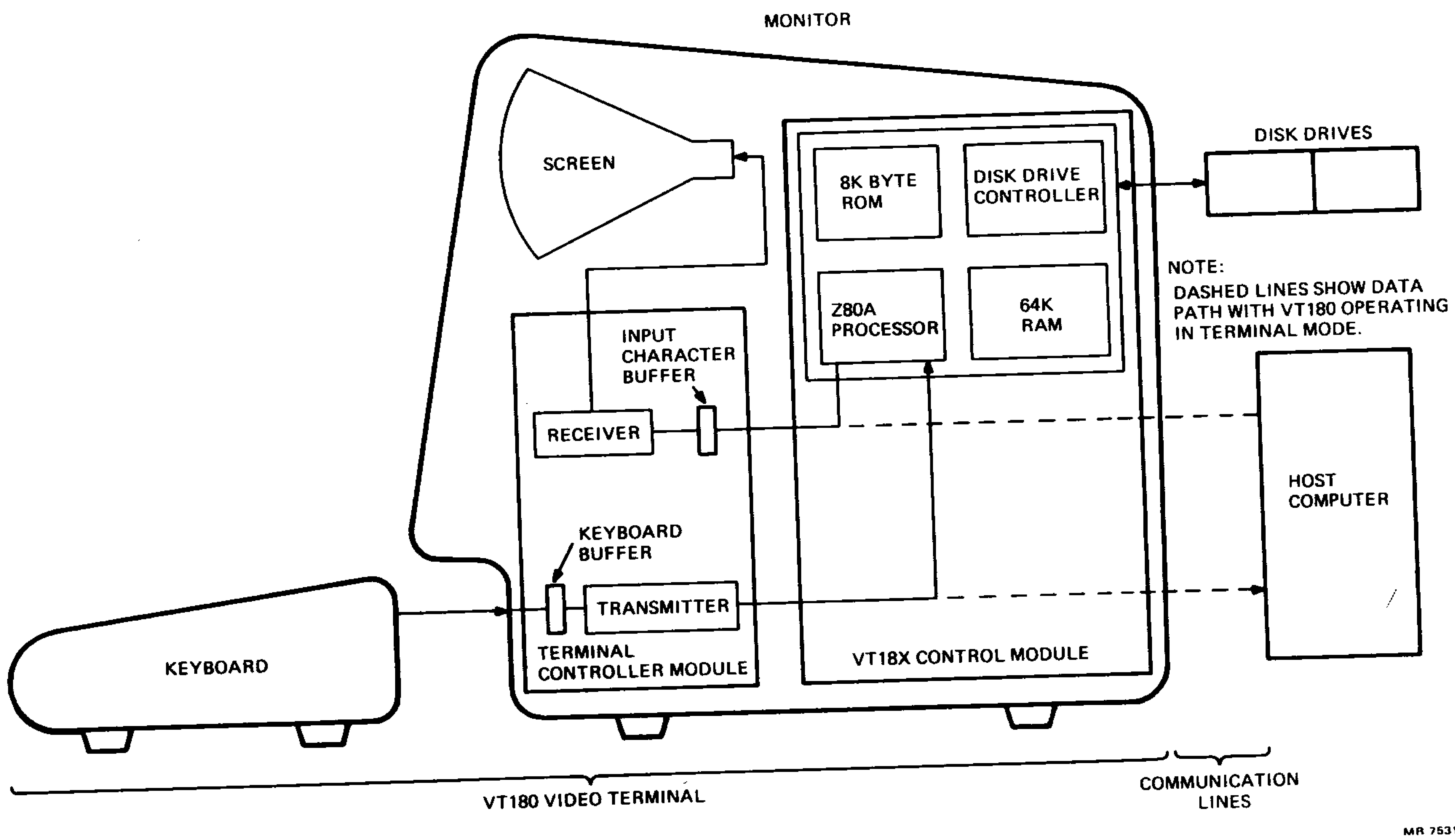


Figure 2-1 VT180 On-Line General Block Diagram

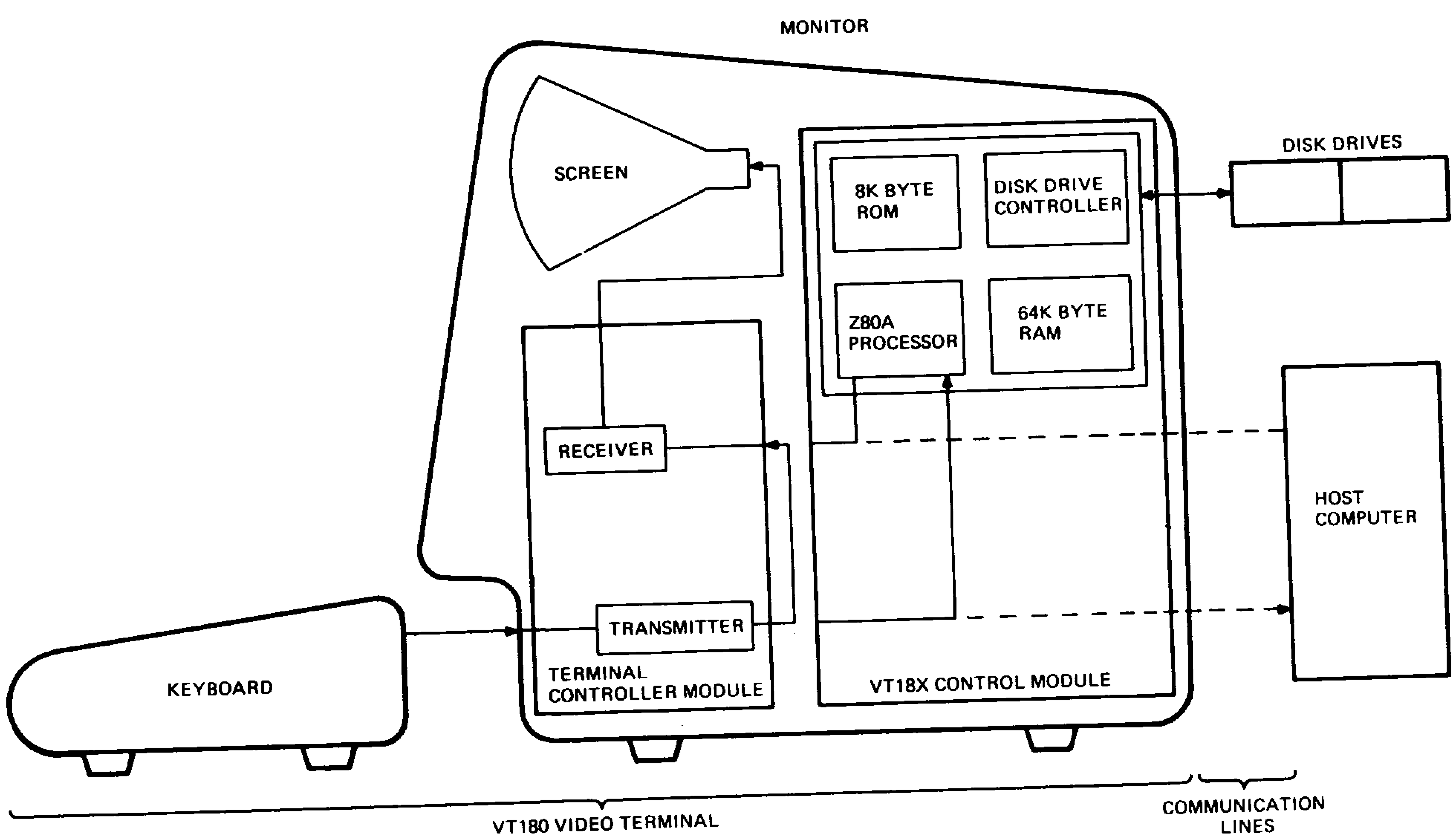


Figure 2-2 VT180 Off-Line General Block Diagram

2.3.1 Terminal Monitor and Disk Drive Power Controls

The terminal monitor and disk drives each have a power switch and a voltage selector switch. The power switch controls the application of ac input power, and the voltage selector switch selects the correct ac voltage range. Figure 2-3 shows the location of these switches. The ac voltage ranges are specified in Paragraph 1.3.4. Note that the voltage selector switch does not select the ac line frequency of the terminal. The ac line frequency is selected by the SET-UP B power feature. (See Paragraph 2.6.5.5.)

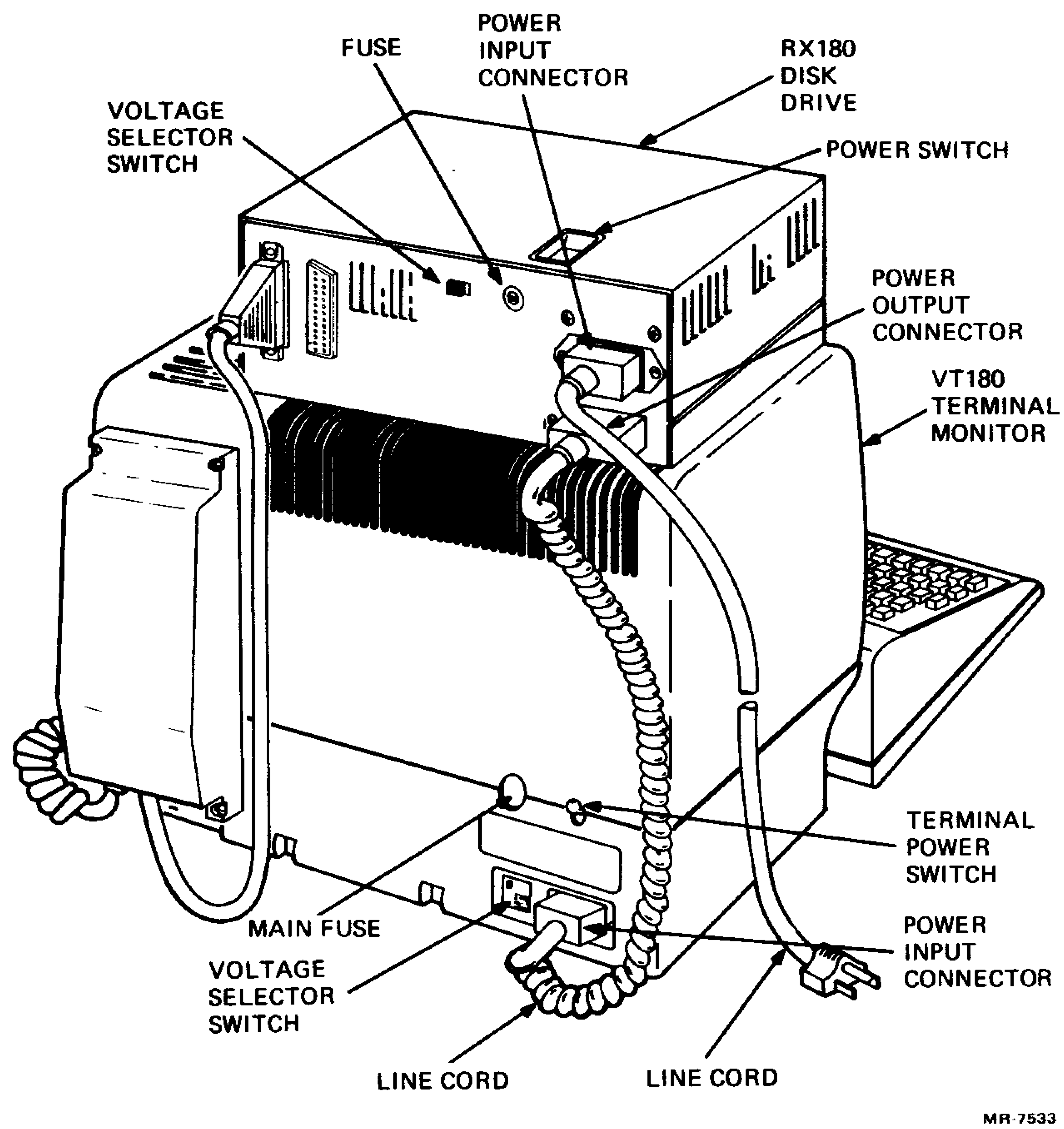


Figure 2-3 VT180 Power Controls

When selecting the voltage range, the fuse on both the terminal monitor and disk drive must have the proper rating for the selected voltage.

CAUTION
Failure to set the voltage selector switches correctly and use the correct fuse may damage the units.

The ac power is routed to the terminal monitor through the disk drive power switch. Therefore, to apply power to the terminal monitor, both the disk drive power switch and the terminal monitor power switch must be on.

Application of power to the monitor should light either the keyboard ON-LINE or LOCAL indicator. Refer to Paragraph 2.4 for more information about the keyboard indicators.

Turning the ac power off may cause the present set-up features to change. Refer to Paragraph 2.6.4 for more information about the effects of the power switch on set-up feature selections.

2.3.2 Keyboard Controls

The VT180 terminal keyboard has a main keyboard and an auxiliary keypad. The main keyboard contains standard typewriter keys that are arranged and that operate like a typical typewriter. There are also a number of additional keys that are used for VT180 functions. The auxiliary keypad is arranged for rapid entry of numerical data or function characters. Figure 2-4 shows the main keyboard and auxiliary keypad key arrangement.

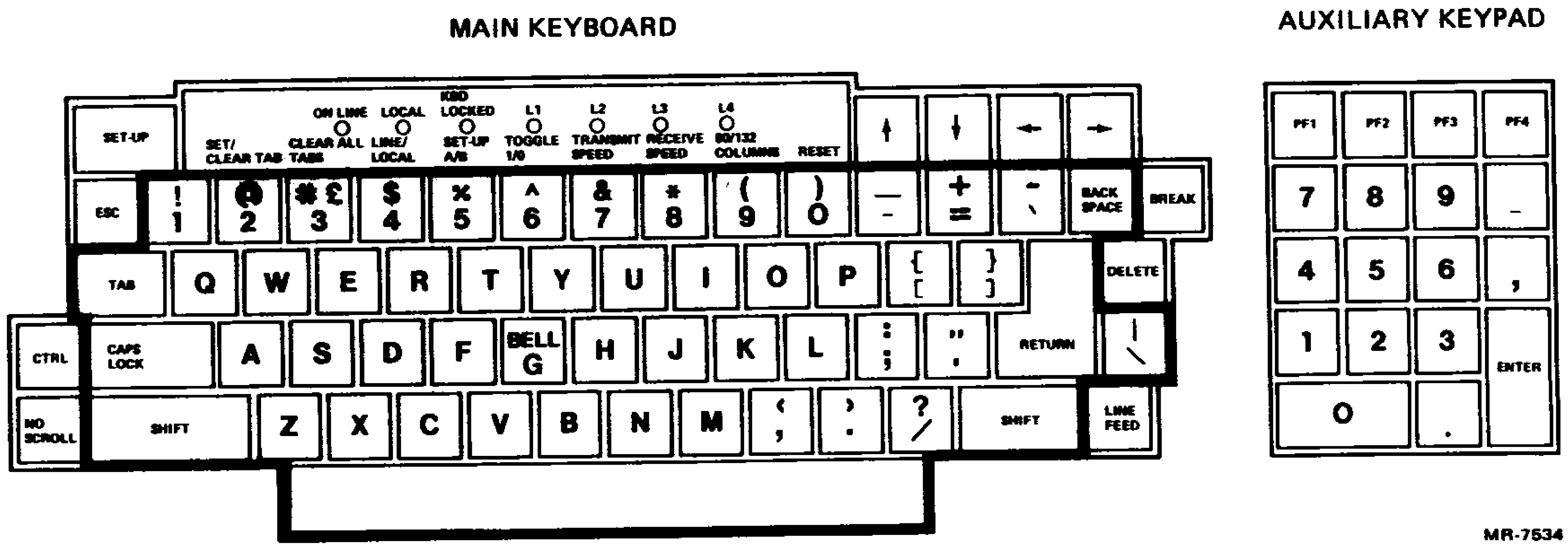


Figure 2-4 VT180 Terminal Keyboard

Some keys on the keyboard immediately generate one or more character codes when pressed. Other keys, such as CTRL, SHIFT, and CAPS LOCK, do not generate character codes but modify the character codes generated by other keys. If two character code keys are pressed at the same time, the character codes are generated immediately. The terminal does not wait for the keys to lift, but generates the character codes as soon as possible. If three character code keys are pressed at the same time, the character codes of the two keys pressed first are generated immediately. The character code of the third key is generated after the first key lifts.

The keys are divided into four groups. They are the standard keys, function keys, set-up keys, and auxiliary keypad keys.

2.3.2.1 Standard Keys – The shaded keys shown in Figure 2-4, with the exception of CAPS LOCK and RETURN, identify the keys that are labeled as standard typewriter keys. Pressing any letter or number key causes the corresponding character to appear on the monitor.

SHIFT and CAPS LOCK modify the character codes generated by standard keys and are described in the following paragraphs. RETURN has a special meaning when the VT180 is operating in computer mode. It is discussed in Paragraph 2.3.2.2.

CAPS LOCK

CAPS LOCK is a two-position latching key. If it is latched in the down position, alphabetic keys generate uppercase character codes regardless of SHIFT. If it is latched in the up position, alphabetic keys generate lowercase character codes. Numeric and special symbol keys are not affected by CAPS LOCK. Similarly, CAPS LOCK does not affect the function keys or auxiliary keypad keys.

SHIFT

When SHIFT is pressed, the standard keys on the main keyboard generate uppercase character codes. SHIFT does not affect the function keys or auxiliary keypad keys. If a key does not have an uppercase function, the SHIFT key is ignored.

2.3.2.2 Function Keys – Figure 2-5 identifies the function keys on the VT180 keyboard. These keys generate function character codes. The use of these character codes is defined by the computer software or communication system. The following paragraphs provide a general description of each function key.

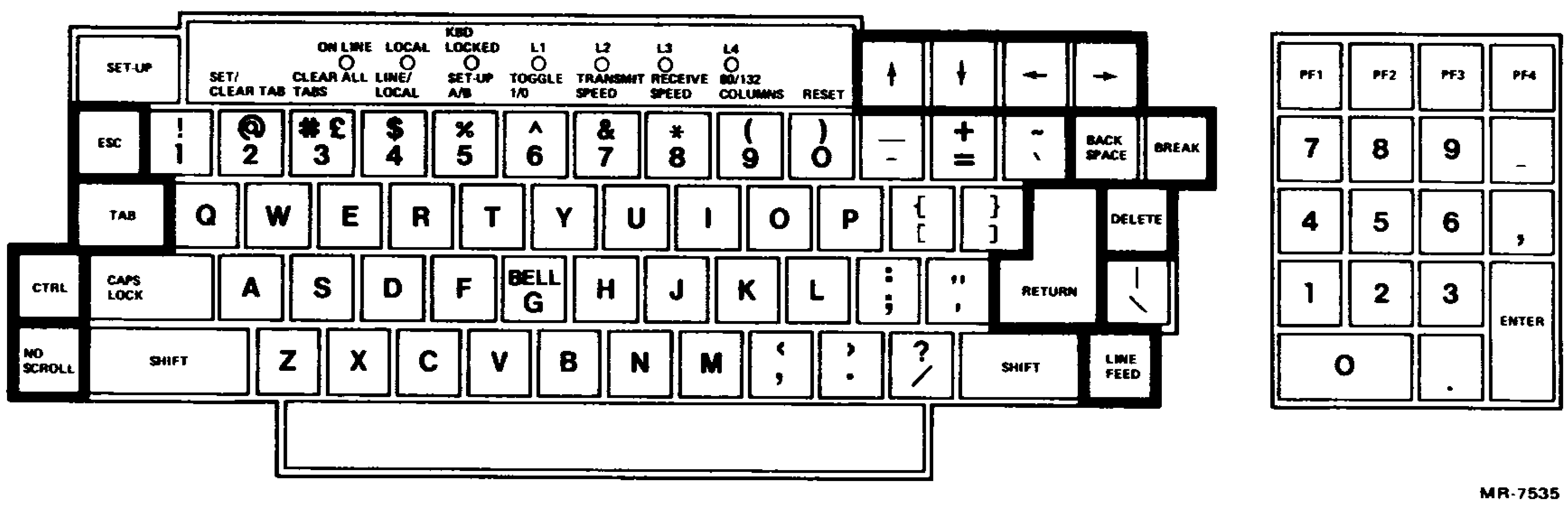


Figure 2-5 Function Keys

NO SCROLL

NO SCROLL controls scrolling in the VT180 terminal. Scrolling is the upward or downward movement of existing lines on the screen to allow new lines to be displayed. When this key is first pressed, scrolling stops. When it is pressed again, scrolling continues.

NOTE
NO SCROLL operates only when the auto XON/ XOFF SET-UP B feature is on.

BREAK

BREAK transmits a break signal to the external host computer when the VT180 is in terminal mode. The computer response to the break signal depends on the computer and the software used. When SHIFT is in the down position, BREAK generates a long break disconnect. The long break disconnect signal turns off the data terminal ready signal to disconnect the host computer from the VT180. When CTRL is pressed, BREAK transmits an answerback message to the host computer. If the VT180 is in computer mode, BREAK has no visible effect when pressed before, during, or after a command to CP/M.

↑ ↓ ← → (Cursor Control Keys)

These keys generate cursor control commands when the VT180 is in terminal mode. The cursor is an indicator (an underline or block) that shows the line and column where the next character is displayed. The cursor will move in the direction of the arrow each time the key is pressed.

When the VT180 is in computer mode, the cursor control keys interact with CP/M to generate special cursor control codes used by such application programs as WordStar®. CP/M alone does not attach a special meaning to these keys and will question any command they are imbedded in.

In set-up mode, the ↑ and ↓ keys increase or decrease display brightness. The ← and → keys move the cursor left and right.

ESC (Escape)
ESC generates the escape control character code. In terminal mode, the ESC key transmits a code that normally has a special meaning to your system. In many applications, pressing this key tells the system to consider the next keys pressed as a command.

If the VT180 is in computer mode, pressing ESC causes CP/M to echo

^[

and nothing more happens. Any effort to mix ESC with normal CP/M commands will fail, with a question mark displayed on the screen and a return to the CP/M prompt.

TAB
TAB generates the tab control character code.

CTRL (Control)
When CTRL is pressed, pressing another key generates a control character code. The control character codes recognized by the host computer (in terminal mode) or CP/M (in computer mode) are described in Appendix A.

BACKSPACE
Pressing the BACKSPACE key while the VT180 is in terminal mode generates the backspace control character, which moves the cursor one column to the left. If the cursor is at the left margin when BACKSPACE is pressed, no further action occurs.

In computer mode, pressing BACKSPACE erases the character to the left of the cursor and moves the cursor one column to the left. CP/M allows characters to be erased by repeated backspace operations until the beginning of the line has been reached; it then ceases to respond to the operation of this key.

DELETE
DELETE generates a delete (DEL) control character code. In terminal mode, the deleted character may or may not be erased from the screen, depending on computer software.

In computer mode, the character to the immediate left of the cursor is erased and then displayed a second time. CP/M allows characters to be erased by repeated delete operations until the beginning of the line has been reached; it then ceases to respond to the operation of this key.

RETURN
RETURN generates either a carriage return or the carriage return <CR> and line feed <LF> control character codes. The characters generated are selected using the line feed/new line SET-UP B feature. The RETURN key is used to terminate commands to the host computer in terminal mode or the VT18X control module in computer mode.

WordStar® is a registered trademark of MicroPro, Inc.

LINE FEED
LINE FEED generates a line feed <LF> control character code, which causes the cursor to move vertically to the next line in the current column position.

2.3.2.3 Set-Up Keys – Figure 2-6 identifies the keys used while operating in set-up mode. There are two set-up feature displays: SET-UP A and SET-UP B. The following paragraphs describe the keys that are used in set-up mode.

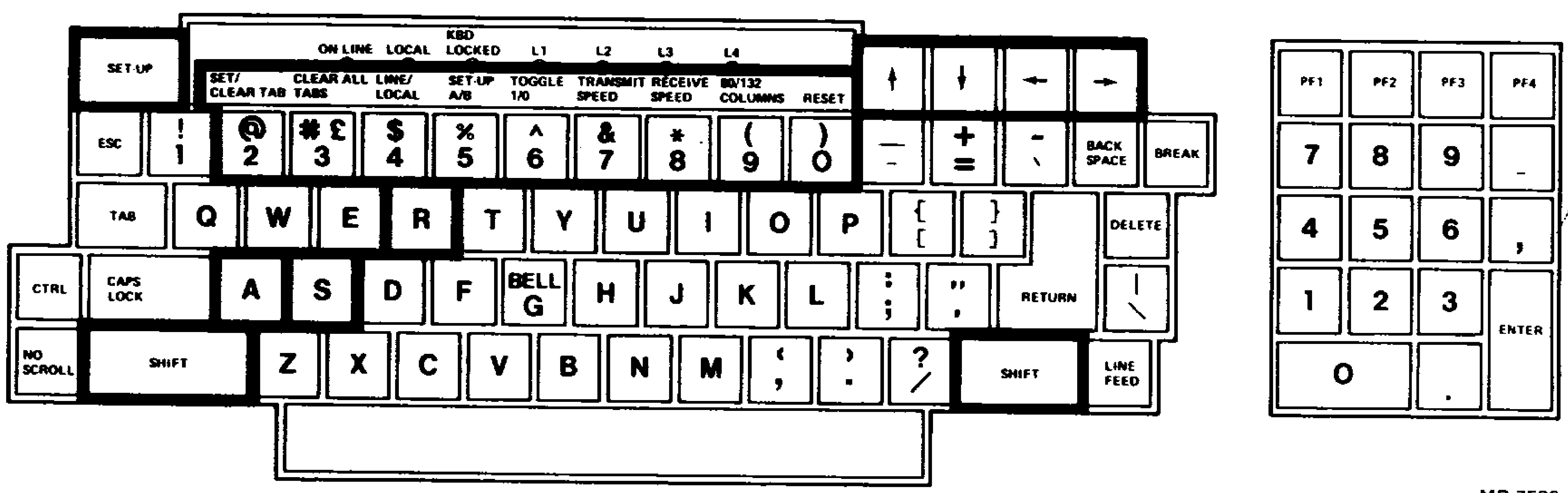


Figure 2-6 Set-Up Keys

NOTE
Read the set-up features and step-by-step feature selection procedures described in Paragraph 2.6 before using the SET-UP keys.

SET-UP
SET-UP places the VT180 in set-up mode. The SET-UP key is used in conjunction with other keys to examine or change terminal operating modes.

@
2 (Set/Clear Tab)
In SET-UP A, set/clear tab sets or clears individual horizontal tabs stops. This key does not function in SET-UP B.

 # £
3 (Clear All Tabs)
In SET-UP A, clear all tabs clears all horizontal tab stops. This key does not function in SET-UP B.

$
4 (On/Off Line)
In any set-up display, on/off-line switches the terminal between on-line and off-line. In on-line, the terminal can transmit and receive character codes. In off-line, the terminal cannot transmit or receive character codes, and keyboard entries are displayed on the screen.

%
5 (Set-Up A/B)
In any set-up display, set-up A/B switches the terminal between SET-UP A and SET-UP B.

^
6 (Toggle 1/0)
In SET-UP B, toggle 1/0 changes the feature selected by the cursor. This key does not function in SET-UP A.

&
7 (Transmit Speed)
In SET-UP B, transmit speed selects the transmit speed (baud rate) used by the communications port of the VT180 terminal. This key does not function in SET-UP A.

*****
8 (Receive Speed)
In SET-UP B, receive speed selects the receive speed (baud rate) used by the communications port of the VT180 terminal. This key does not function in SET-UP A.

(
9 (80/132 Columns)
In SET-UP A, 80/132 columns selects the display line size. The size is either 80 or 132 columns per line. This key does not function in SET-UP B.

)
0 (Reset)
In either SET-UP A or B, reset starts the reset sequence. This sequence has the same result as turning the power switch off and then on.

↑ ↓ (Brightness)
In either SET-UP A or B, ↑ (up arrow) increases and ↓ (down arrow) decreases the brightness of the display.

← → (Cursor Control Keys)
In either SET-UP A or B, ← (left arrow) and → (right arrow) move the cursor left and right.

A
In SET-UP B, hold down the SHIFT key, press the A key, and then release both keys to enter the answer-back message. When entering the answerback message all keyboard keys can be used.

R
In any set-up display, hold down the SHIFT key and press the R key to recall the set-up features stored in the terminal's permanent memory.

S
In any set-up display, hold down the SHIFT key and press the S key to store the set-up features in the terminal's permanent memory.

2.3.2.4 Auxiliary Keypad Keys – The auxiliary keypad can be used to generate either the same character codes as the main keyboard or function characters. The computer selects the type of characters generated by these keys.

When the auxiliary keypad generates the same codes as the main keyboard, the minus sign, comma, period, and numeric keys of the auxiliary keypad correspond to the unshifted keys on the main keyboard. The SHIFT keys on the main keyboard do not affect keypad characters.

When the auxiliary keypad generates function character codes, the use of these character codes is defined by the computer software. The program function keys (PF1 through PF4) on the auxiliary keypad always generate control sequences. These keys are distinguished by the fact that they send three characters rather than one each time they are pressed. Certain application programs may make use of these keys when the VT180 is operating in terminal mode. These keys are not used when the VT180 is in computer mode because CP/M does not understand them and will issue an error message if they are imbedded in commands.

The ENTER key duplicates the function of the RETURN key on the main keyboard.

2.4 VISUAL INDICATORS

The seven LEDs on the main keyboard are used to indicate internal VT180 terminal conditions, display error codes during self-test, and display user-programmable information during normal operation. The keyboard indicators are shown in Figure 2-7, and their functions are described in the following paragraphs.

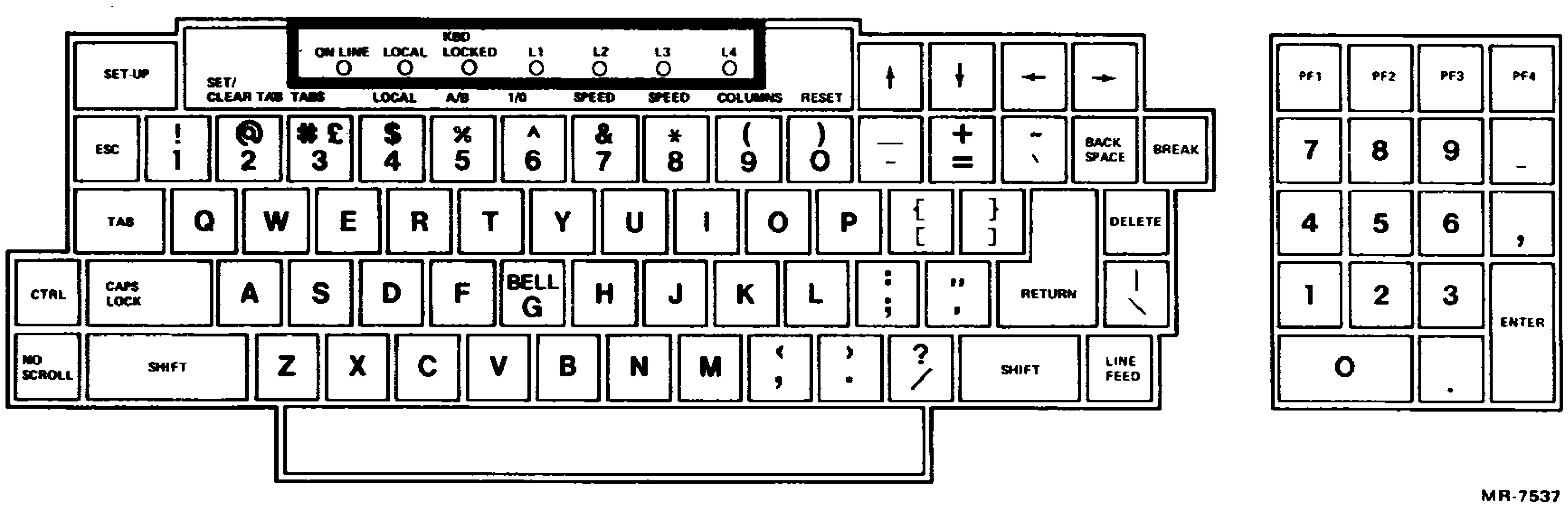


Figure 2-7 Keyboard Indicators

2.4.1 ON-LINE

The ON-LINE indicator is lit when the terminal is on-line and can transmit and receive character codes. The illumination of either ON-LINE or LOCAL implicitly shows that the keyboard and disk drive is connected and ac power is applied to the VT180.

2.4.2 LOCAL

The LOCAL indicator is lit when the terminal is off-line and cannot transmit or receive character codes from either the internal computer or host computer. When the terminal is off-line, characters from the keyboard are displayed on the screen.

2.4.3 KBD LOCKED

KBD LOCKED is lit when the keyboard is in the locked condition. The keyboard locked condition occurs when the keyboard character buffer is full and cannot hold more characters from the keyboard. The keyboard character buffer holds character codes from the keyboard before they are transmitted to the computer. When KBD LOCKED is on, any character codes sent from the keyboard are lost. If the keyclick SET-UP B feature is on, keyclicks are not generated when keys are pressed.

NOTE

The terminal can receive characters from the computer during the keyboard locked condition.

The keyboard locked condition ends when character codes in the keyboard character buffer are transmitted to the computer. After the characters have been transmitted, the KBD LOCKED turns off and keyclicks can be generated (if the keyclick SET-UP B feature is on).

The keyboard locked condition also ends after entering and exiting set-up. Entering and exiting set-up with the KBD LOCKED on, however, erases the characters held in the keyboard buffer before they are transmitted. Refer to Paragraph 2.6.1 for more information about entering and exiting set-up.

2.4.4 L1 through L4 Indicators
These indicators are controlled by the computer and are defined by the computer software. During power-up or reset, L1 through L4 indicate errors found as a result of running the ROM-based diagnostics.

2.5 AUDIBLE INDICATORS
The VT180 terminal uses two audible indicators: a keyclick and a bell tone. The following paragraphs describe these indicators.

2.5.1 Keyclick
The terminal generates a keyclick when a key is pressed, with the following exceptions.

1. SHIFT and CTRL do not generate keyclicks because they do not generate character codes. They modify the character codes generated by other keys.

2. Keyclicks are not generated when the KBD LOCKED indicator is on; character codes from the keyboard are lost.

3. Keyclicks are not generated when the keyclick SET-UP B feature is off.

2.5.2 Bell Tone
The terminal generates a bell tone in each of the following cases.

1. When the bell character is received from the computer

2. When the cursor is eight characters away from the right margin and the margin SET-UP B feature is on

2.6 SET-UP MODE
The VT180 has an extensive set of operating features that allow the terminal to be configured for specific applications. These built-in features are selected by pressing the appropriate keyboard key while the terminal is operating in set-up mode. The selected features are stored in a nonvolatile memory (NVR) that always remembers which features have been selected, as if a switch had been set.

When you enter set-up mode, the status of features stored in temporary memory shows on the screen. You can then change the features and store any new feature selections either temporarily (by leaving set-up mode) or on a fixed basis (by performing a save operation). In either case, terminal operation reflects the new feature selection. If a recall operation is performed, the terminal is reset, or terminal power is turned off, all temporary feature settings are replaced by features that have been stored on a fixed basis.

2.6.1 Entering and Exiting Set-Up
You can enter set-up while either on-line or off-line by pressing the SET-UP key. However, if the VT180 is on-line and in terminal mode, select the auto XON/XOFF SET-UP B feature to prevent losing received characters. Refer to Paragraph 2.6.5.5 for more information about this feature.

If the auto XON/XOFF SET-UP B feature is not used, characters may be lost. Therefore, disconnect the terminal immediately before entering set-up. To disconnect a communication line and prevent the terminal from receiving characters while in set-up, hold down the BREAK key and press SHIFT. In correctly configured modems (data sets) this causes a communication line disconnect.

When entered, the set-up mode provides two summaries of the current status of VT180 features. The first display, SET-UP A, displays the location of the tab stops set and a visual ruler that numbers each character position on the line. The second display, SET-UP B, summarizes the current status of the other terminal features.

The terminal features can be reviewed and changed by pressing the SET-UP key (shown in Figure 2-8) when the CP/M prompt indicates that the system is waiting for a command. Pressing SET-UP once causes the terminal to put up the SET-UP A display shown in Figure 2-9, and pressing the 5 key causes the terminal to put up the SET-UP B display shown in Figure 2-10. SET-UP B can only be entered from SET-UP A.

To exit set-up mode, press the SET-UP key.

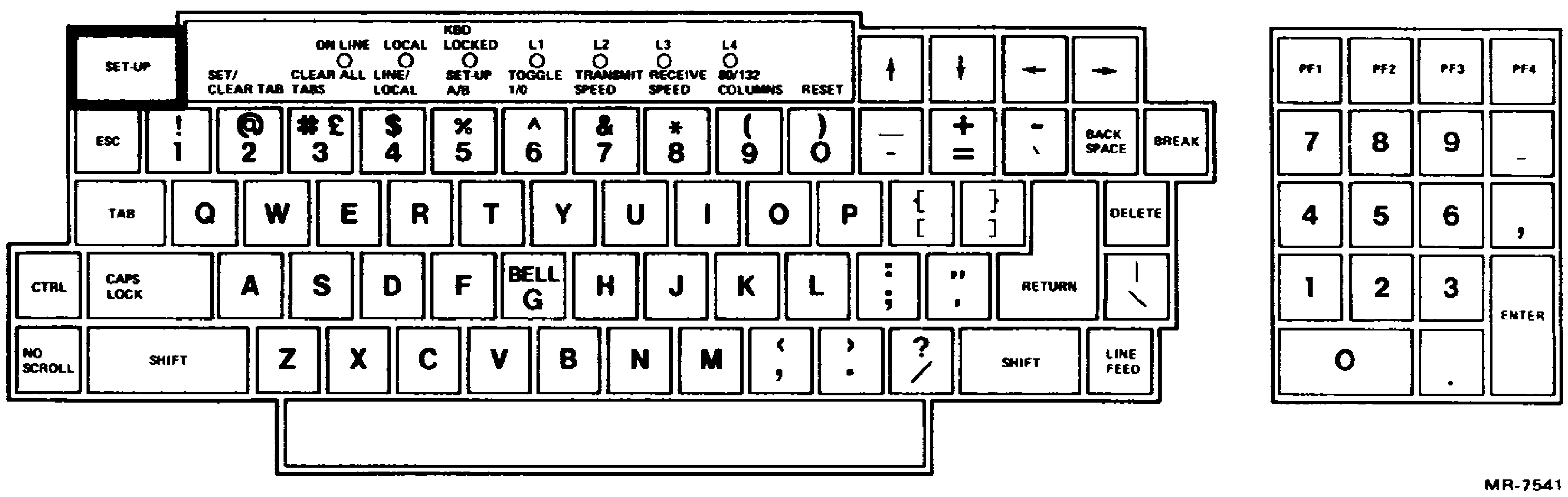


Figure 2-8 The VT180 SET-UP Key

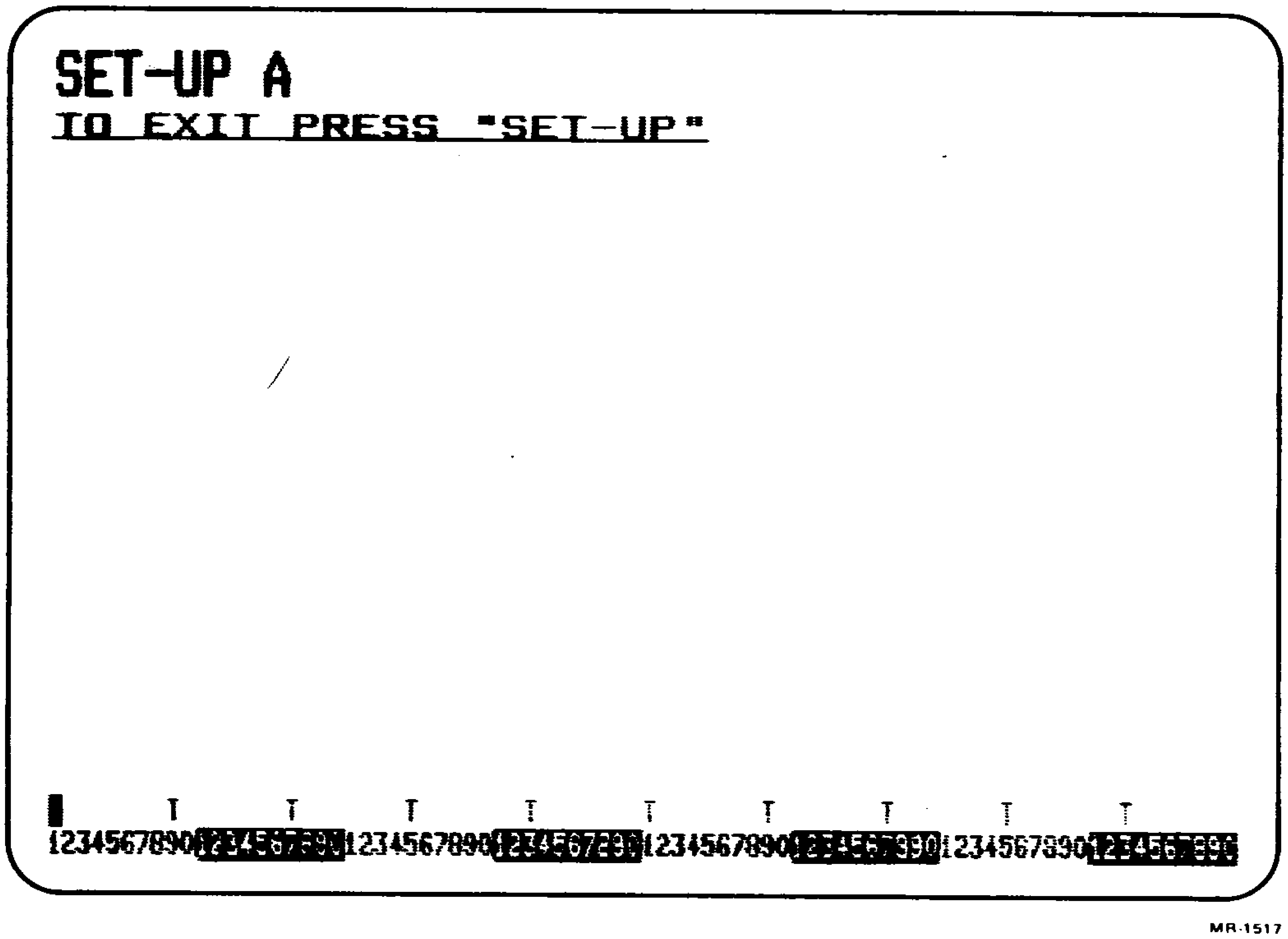


Figure 2-9 SET-UP A Display

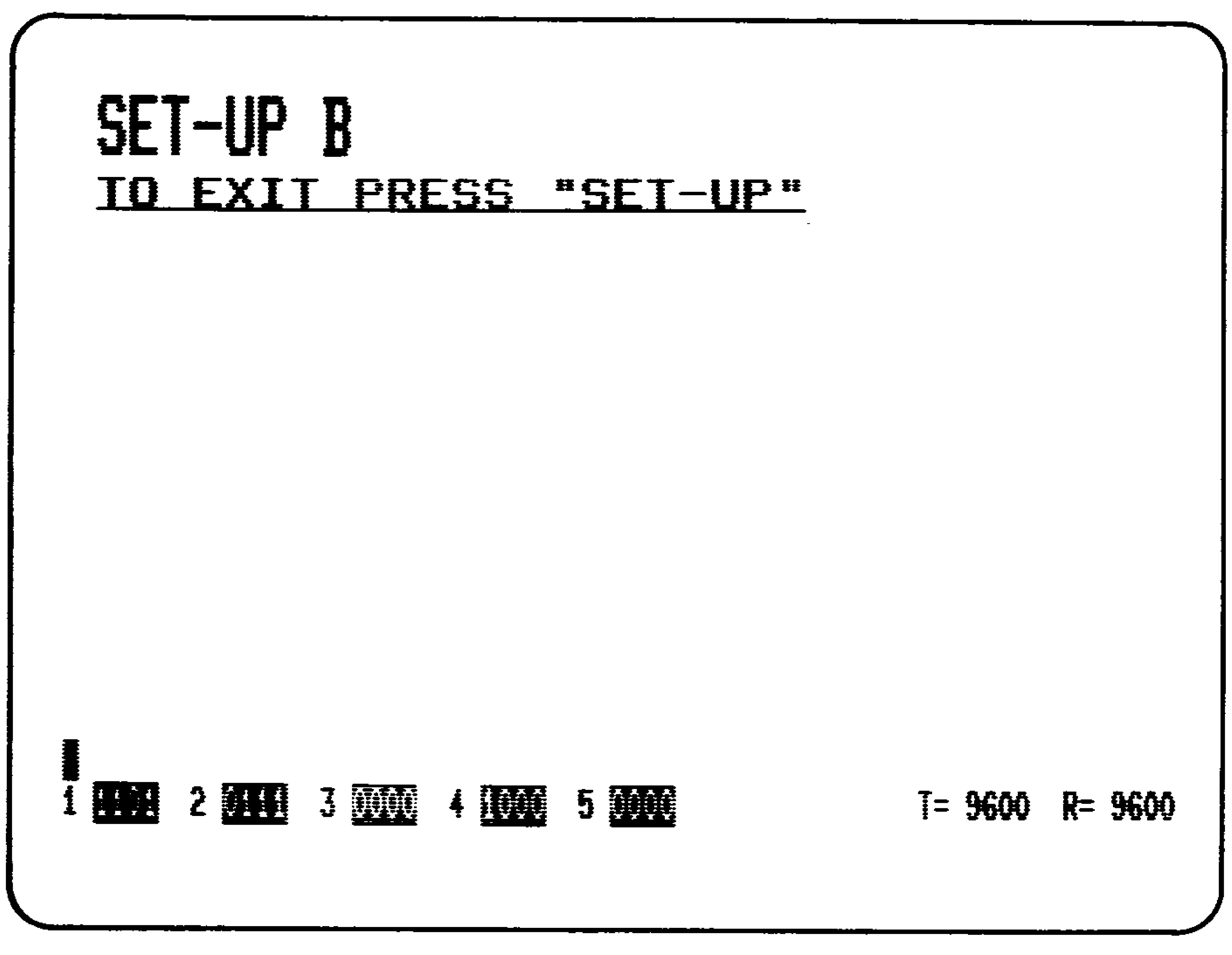


Figure 2-10 SET-UP B Display

2.6.2 Set-Up Feature Types

Set-up features are used to change the operational characteristics of the VT180. Set-up features can be divided into four types: operator preference, terminal communication compatibility, CP/M compatibility, and installation. These feature types are described in the following paragraphs and are summarized in Table 2-1.

Table 2-1 Set-Up Feature Types

Set-Up Feature	Operator Preference	Communication Compatibility	Installation	CP/M Compatibility
On/off-line		X		
Screen brightness	X	X		
Columns per line		X		
Tab stops		X		
Scroll	X	X		
Auto repeat	X			
Screen background	X			
Cursor	X			
Margin bell	X			
Keyclick	X			
ANSI/VT52		X		X
Auto XON/XOFF		X		X
US/UK character set		X		
Wraparound		X		X
Line feed/new line		X		X
Interlace			X	
Power			X	X
Data/parity bits		X*		
Transmit speed		X*		
Receive speed		X*		
Answerback		X*		

*These features may be selected only for communications between the terminal and an external host computer. The data/parity bits and transmit and receive speed are fixed when the VT180 operates in computer mode.

2.6.2.1 Operator Preference Features – These features configure the VT180 as the operator prefers. They do not affect information transfers between the terminal and the host computer (in terminal mode) or the keyboard and internal computer (in computer mode).

2.6.2.2 Communication Compatibility Features – These features configure the terminal so that it is compatible with the communications characteristics of either the host computer (in terminal mode) or the internal computer (in computer mode). Many combinations of set-up features are used when communicating with either computer. An error in the selection of these features may stop communications or cause incorrect information to be transferred between the terminal and either computer.

2.6.2.3 Installation Features – These features configure the terminal for operation in different installations. If the location of the terminal is changed, verify these feature selections.

2.6.3 Set-Up Feature Selection

Set-up features can be selected by the host computer or by the keyboard when the VT180 is in terminal mode. When the VT180 is in computer mode, set-up features can be selected only by the keyboard. Features currently selected by the host computer are shown by the set-up feature display. The host computer is limited in the number of features it can change. The set-up features the host computer can change are listed in Table 2-2.

Table 2-2 Set-Up Features the Host Computer Can Change

Set-Up Feature	Can Be Changed
On/off-line	
Screen brightness	
Columns per line	X
Tab stops	X
Scroll	X
Auto repeat	X
Screen background	X
Cursor	
Margin bell	
Keyclick	
ANSI/VT52	X
Auto XON/XOFF	
US/UK character set	X
Wraparound	X
Line feed/new line	X
Interlace	X
Parity sense	
Parity	
Bits per character	
Power	
Transmit speed	
Receive speed	
Answerback	

To select set-up features from the keyboard, you must enter set-up. Changing any or all set-up features is a simple operation and is generally performed by following the same basic steps.

1. Enter set-up mode by pressing the SET-UP key.

2. Select the appropriate set-up mode by pressing the 5 key on the main keyboard each time you want to switch from SET-UP A to SET-UP B or from SET-UP B to SET-UP A.

3. Position the cursor above the feature switch or tab stop to be changed. To position the cursor, the SPACE bar, ←, →, TAB, and RETURN keys may be used. Some features do not use this step since a specific key is dedicated to changing the feature.

4. Change the feature setting by pressing either the 6 key on the main keyboard or the appropriate dedicated key. Each time the key is pressed the feature changes, generally to the opposite state.

5. Store the set-up features, if desired, by performing a save operation.

6. Press SET-UP to exit set-up mode.

2.6.4 Restoring and Saving Set-Up Features

Set-up features may be stored temporarily in an operating memory or on a fixed basis in the user-permanent nonvolatile RAM (NVR) memory. To temporarily store one or more features, exit set-up mode after changing the feature(s). The VT180 will then operate as needed by the new features until one of the following conditions is met.

1. The set-up features are changed again.
2. The system is turned off.
3. The original features are restored.

Set-up features may be temporarily changed as often as needed, but the original features stored in permanent memory will always be restored to the operating memory when the system power is turned off and then on again.

2.6.4.1 Restore – The original features may also be restored without turning off the system power by executing a restore command from the keyboard. The restore command is executed by pressing the SHIFT and R keys at the same time while in set-up mode. The terminal will clear the screen and display the word WAIT briefly in the upper left corner, then return to the SET-UP A display. Note that the restore operation erases any text that was on the screen when the terminal entered set-up mode. It does not, however, have any effect on CP/M unless the restored features are incompatible with CP/M programs.

2.6.4.2 Save – The save command stores set-up features on a fixed basis in permanent memory. The next time the system is powered up, the terminal will have the set-up features that were active when the save command was executed. This command permits saving those terminal features that are needed each time the system is powered up.

The save command is executed by pressing the SHIFT and S keys at the same time while in set-up mode. The screen will momentarily go blank and the message WAIT is displayed in the upper left corner. The terminal then returns to SET-UP A mode.

NOTE

The save operation must be performed at the keyboard. The host computer cannot perform this operation, although it can temporarily modify the setting of some VT180 features.

2.6.4.3 Reset – The system reset command forces the VT180 computer to restart the operating system program, causes the terminal to go through its self-test program, erases all feature selections previously in operating memory, and restores feature selections that are stored in permanent memory to the operating memory. The reset command can be executed from the keyboard. Pressing the 0 key while in set-up mode causes a system reset.

The terminal self-test is identifiable, when executed after the terminal has warmed up, by a brief display of random characters and patterns, followed by a bell tone and, when the test is successful, a return to on-line mode (the ON-LINE indicator above the 4 key lit). If the self-test is unsuccessful, the reset operation will conclude with the terminal in local mode (the LOCAL indicator above the 4 key lit). An error code displayed in the upper left corner of the screen may identify hardware failures.

Note that the reset command is automatically executed when the system is turned on as well as when the 0 key is pressed in set-up mode.

2.6.5 Set-Up Features

The set-up features that follow are arranged according to the set-up display in which they appear. There are three types: general set-up features that can be changed in any set-up display, SET-UP A features, and SET-UP B features.

NOTE

Unless otherwise stated, entering set-up mode and changing features does not result in the loss of data displayed on the screen.

2.6.5.1 General Set-Up Features – The on-line/local and screen brightness set-up features may be changed in any set-up display although the initial setting of screen brightness is normally performed in SET-UP A. Dedicated keys are used to select these features.

On-Line/Local

This feature places the terminal either on-line or off-line. While on-line, the keyboard ON-LINE indicator is illuminated and the terminal can transmit and receive character codes. Keyboard entries are transmitted to either the internal computer or host computer through CP/M and characters received from either computer are displayed on the screen.

While off-line, the LOCAL indicator is illuminated. The terminal cannot transmit and receive characters through CP/M, and it cannot communicate with either the internal computer or the host computer. The keyboard transmits its output directly to the terminal. This mode aids in distinguishing between hardware and software failures.

When the VT180 terminal is placed off-line, three things happen.

1. The terminal disconnects from the host computer or internal computer.
2. It erases the terminal input buffer (where received characters are held before display).
3. It erases the terminal keyboard buffer (where characters to be transmitted are held before transmission).

This mode is enabled when the 4 key is pressed. This action will cause the ON-LINE indicator above the 4 key to turn off and the LOCAL indicator to turn on. If SET-UP A is exited (by pressing the SET-UP key), keyboard entries will be displayed on the screen but CP/M does not respond to any CP/M commands. The terminal is returned to on-line mode by pressing the SET-UP key and then pressing the 4 key.

Screen Brightness

This feature adjusts the brightness of the terminal screen. Each time you press the ↑ (up arrow) key, the display becomes brighter by a small increment, and each time you press the ↓ (down arrow) key, it becomes dimmer. CP/M ignores screen brightness. Set this attribute to give a display that is comfortable to you.

2.6.5.2 SET-UP A Features – The SET-UP A display (Figure 2-9) summarizes the number of columns per line and the tab stop selections. SET-UP A features are selected using dedicated keys.

80/132 Columns
This feature selects a display of either 80 or 132 columns per line. When 80 columns per line is selected, the screen is 80 columns wide and 24 lines long. When 132 columns per line is selected, the screen is 132 columns wide and 14 lines long (24 lines if the VT180 is equipped with the advanced video option). The displayed lines for the 132 columns per line selection are the same width on the screen as for the 80 columns per line selection, but the columns are closer together (Figure 2-11).

The VT180 terminal normally provides 80 columns for character display. Certain application programs, however, may require a wider screen. Pressing the 9 key when SET-UP A is selected causes the screen to change from 80 to 132 columns. Pressing the key again (while in SET-UP A) returns the terminal to its original 80-column state.

NOTE

Entering SET-UP A does not erase any text displayed on the screen, although it will be temporarily replaced by the SET-UP A display. Changing screen width, however, *will* erase the screen, although it will not affect any control program that may be running at the time.

CP/M formats the screen on the assumption that the terminal is in 80-column mode. No damage will be done (except for decreased legibility) however, if the screen is set to 132-column mode.

Set/Clear Tab and Clear All Tabs
The bottom line of the SET-UP A display (Figure 2-9) is a ruler that numbers each column position on a line. Each T above the ruler indicates a presently-selected tab stop. Tab stops are column positions selected on the lines of the terminal screen. The cursor can tab, or advance, to the column with the tab stop.

You can erase all the the tab stops by pressing the 3 key, clear all tabs. You can erase individual tab stops by moving the cursor over a given stop and pressing the 2 key, set/clear tab. Add tab stops by moving the cursor to the correct location and pressing the 2 key.

Note that the 2 key reverses the state of the selected location. If a tab stop is present, pressing the 2 key erases it; if a tab stop is not present, pressing the 2 key installs it.

CP/M needs no specific tab stop settings. The settings shown in Figure 2-9 will be acceptable for most application programs.

2.6.5.3 SET-UP B – To enter SET-UP B, press the 5 key when the SET-UP A display is on the screen. The display will change to that shown in Figure 2-10. The features available for manipulation in SET-UP B are encoded as shown in Figure 2-12. Each feature has two modes, identified by 0 and 1. Modes are changed by positioning the cursor over the desired feature and pressing the 6 key. If your selected feature is in mode 0, pressing the 6 key changes it to 1 and vice versa.

The data/parity bits, transmit speed, and receive speed features are selected using dedicated keys when the VT180 is operating in terminal mode. When the VT180 is operating in computer mode, these features are fixed and need not be selected.

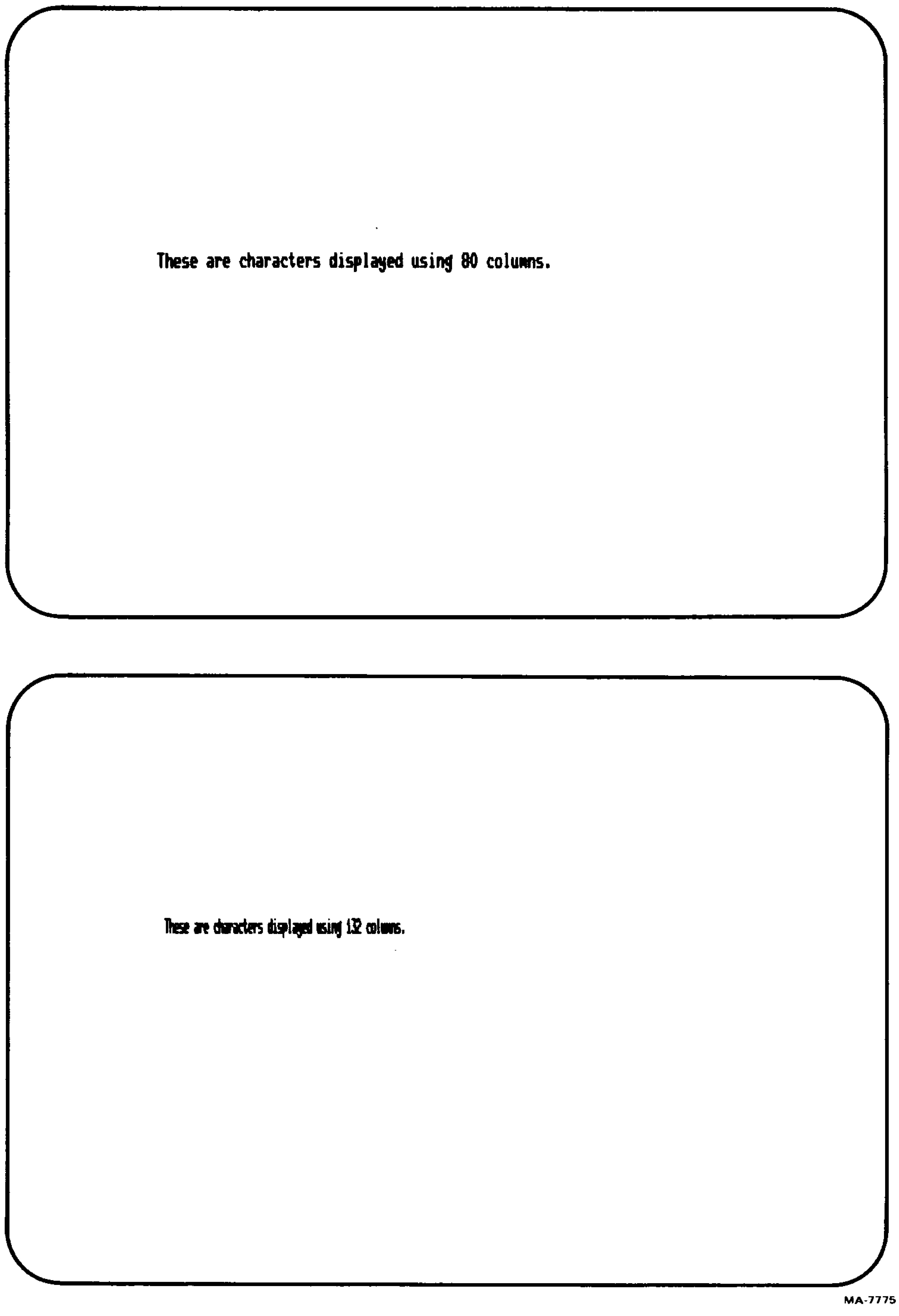


Figure 2-11 80- and 132-Column Displays

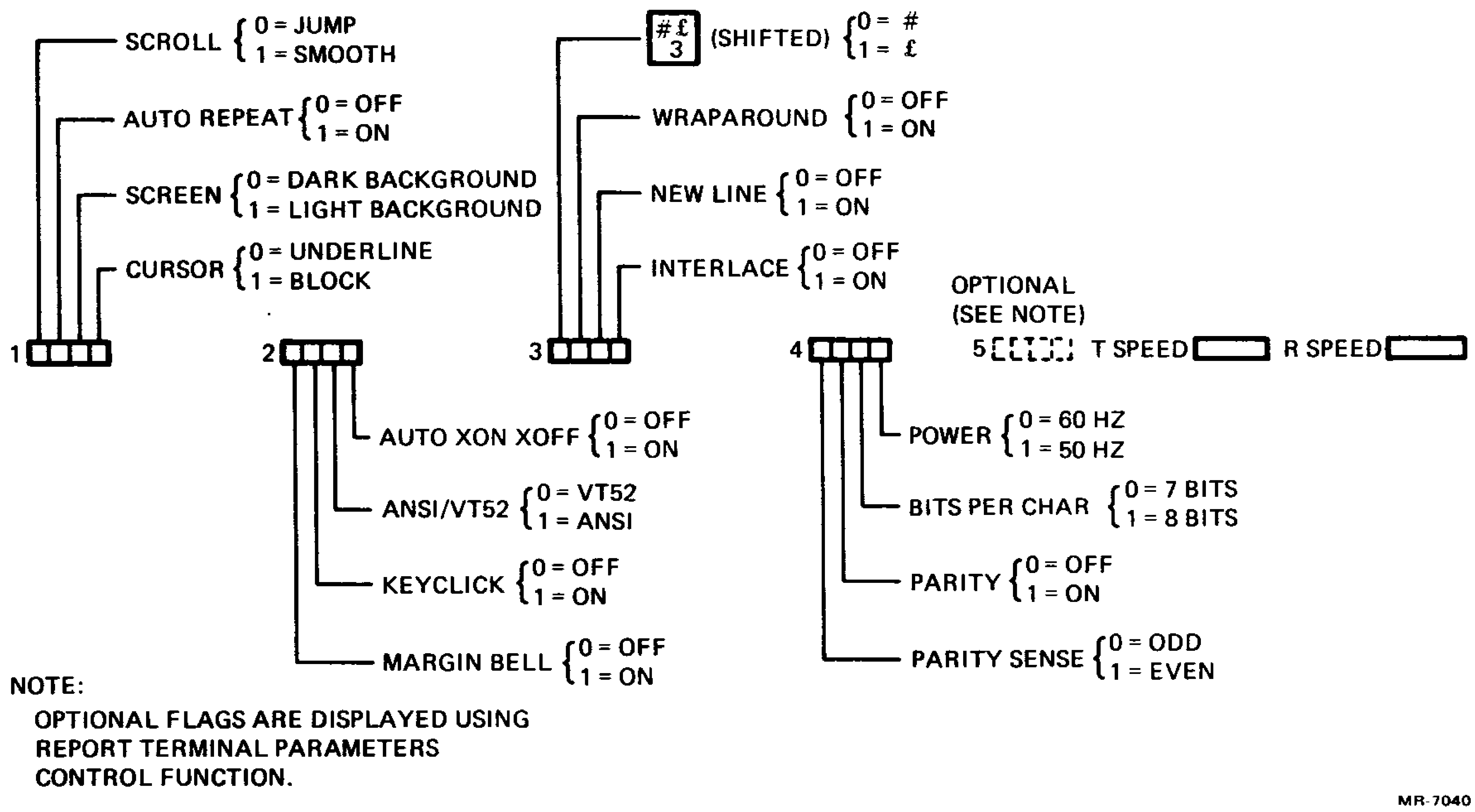


Figure 2-12 SET-UP B Summary

2.6.5.4 SET-UP B, User Preference Features – All of the following SET-UP B features can be set according to user preference. They are selected by moving the cursor over the desired feature and pressing the 6 key to obtain the correct mode.

Scroll

The VT180 terminal can scroll text up the screen slowly and smoothly or swiftly and unevenly. These two modes are called smooth scrolling and jump scrolling. Smooth scrolling moves the text a scan line at a time (that is, 1/256th of the screen height); jump scrolling moves text a printed line at a time (that is 1/24th of the screen height). The advantage of smooth scrolling is that the eye can follow the text up the screen as it moves. The disadvantage is that smooth scrolling takes twice or three times as long to deal with a screenful of text as does jump scrolling. Set the digit for this feature to 1 to select smooth scrolling.

NOTE

Smooth scroll mode allows a maximum of six lines of data per second to be added to the screen. The auto XON/XOFF feature must be enabled and supported by the host computer to make sure that data is not lost when smooth scroll mode is enabled. The auto XON/XOFF feature must be enabled when the VT180 is operated in the personal computer mode.

Auto Repeat

Auto repeat allows a key to be automatically repeated at a rate of about 30 characters per second when the key is held down for more than one-half second. The auto repeat feature affects all keyboard keys except the following.

SET-UP	TAB
ESC	RETURN
NO SCROLL	CTRL and any key

Set the digit associated with this feature to 1 to enable auto repeat.

Screen Background

This feature allows you to select the background of the screen display. In normal screen mode, the display contains light characters on a dark background; in reverse screen mode, the display contains dark characters on a light background. The normal and reverse screen displays are shown in Figure 2-13. Set the digit associated with this feature to 1 for black characters on a white background.

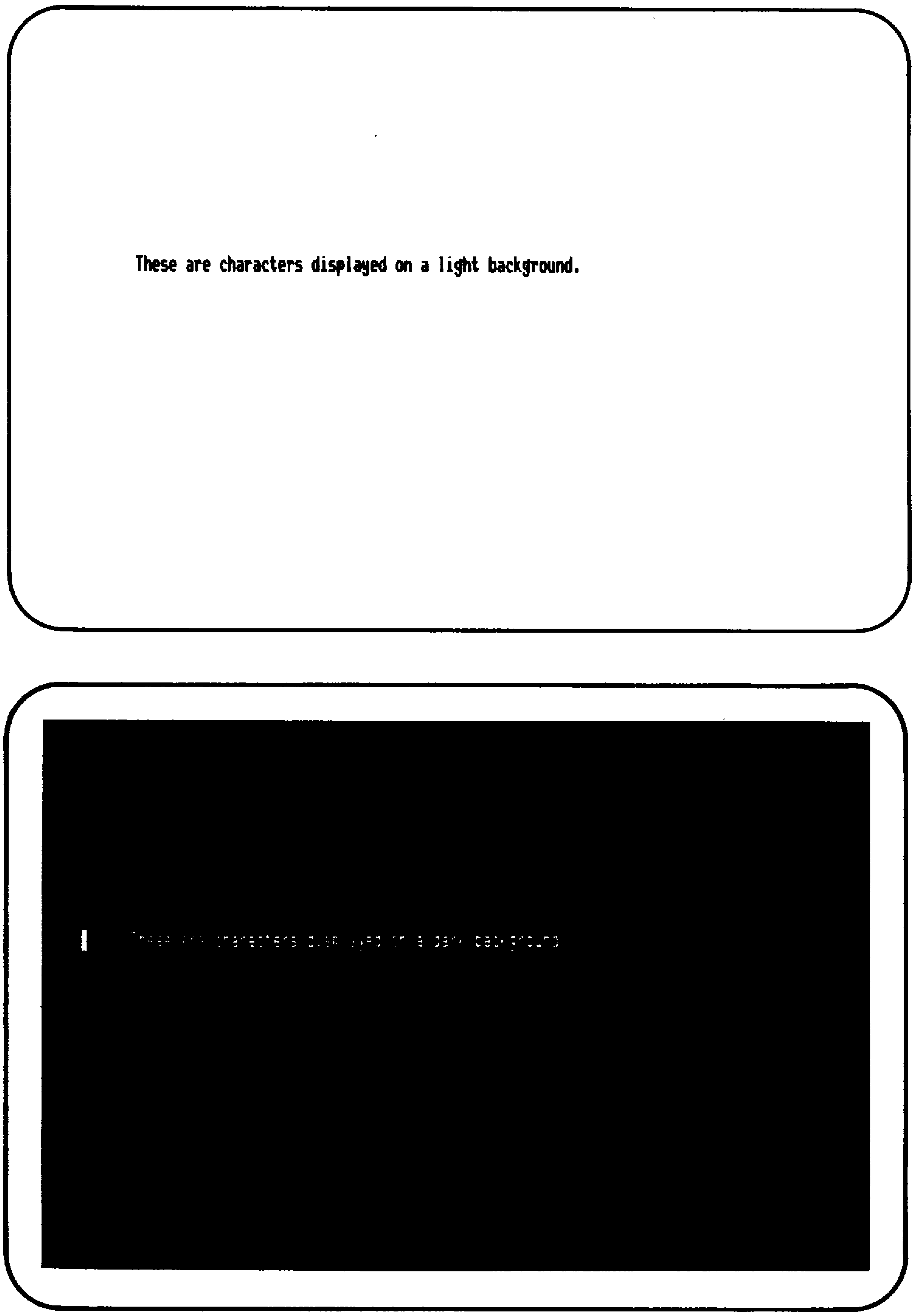


Figure 2-13 Screen Background

Cursor
The VT180 has two cursor displays to indicate the active positions where the next character will be placed on the screen. The cursor may be either a blinking underline or a blinking block. Set the digit associated with this feature to 1 for the flashing square cursor. The cursor selection may perform an additional function; see the SGR escape sequence definition in Appendix A.

Margin Bell
The margin bell feature is much the same as the bell in a typewriter. If the cursor is eight characters from the end of the current line while typing, the VT180 sounds a tone to alert the operator. Set the digit associated with this feature to 1 to enable the margin bell.

Keyclick
The VT180 keyboard can operate silently or can provide a typewriter-like click each time a key is pressed. Research and experience has shown that an operator is more accurate when there is audible feedback from the keyboard. Like the bell tone, the keyclick volume is not adjustable. Set the digit associated with this feature to 1 to enable keyclick.

United States/United Kingdom Character Set
The VT180 contains character sets for the United States and the United Kingdom. The difference between the two sets is one character, the number sign (#) or British pound sterling symbol (£). When the standard United States character set is selected, the uppercase 3 key on the main keyboard displays the # character. The £ character is displayed when the United Kingdom character set is selected. Set the digit associated with this feature to 0 to select the United States character set.

Interlace
In normal operation, the VT180 terminal uses only 256 of the available 512 scan lines to paint characters on the screen. That is, it skips every other available line. Interlace permits all 512 lines to be used and may improve the output of hard copy or video devices connected to the video output connector. Interlace generally produces sharper images when the screen is being photographed. To human eyes, however, interlace causes the screen image to appear to tremble in a disconcerting way. Usually operators prefer to have this feature off. Set the digit associated with this feature to 1 to enable interlace.

2.6.5.5 SET-UP B, CP/M Compatibility Features – Certain SET-UP B features must be set to provide compatibility between the CP/M operating system and the VT180 in computer mode. These features are selected by moving the cursor over the desired feature and pressing the 6 key on the main keyboard to obtain the correct mode.

ANSI/VT52 Mode
The VT180 terminal follows two programming standards: American National Standards Institute (ANSI) and VT52. In ANSI mode, the VT180 generates and responds to programmed sequences according to ANSI standards X3.41-1974 and X3.64-1977. In VT52 mode, the VT180 terminal is compatible with previous Digital software using the VT52 video terminal. Both ANSI and VT52 modes are described in Appendix A of this manual. Set the digit associated with this feature to 1 to enable ANSI mode, which is CP/M compatible.

Auto XON/XOFF
The VT180 can automatically generate synchronizing codes XON (DC1) and XOFF (DC3). XOFF stops data transmission from the host computer to the terminal; XON resumes transmission. With the feature enabled, the VT180 generates the XOFF code when one of the following occurs. (The auto XON/XOFF feature must be enabled when the VT180 is operated in personal computer mode.)

1. The internal buffer is almost full.
2. The NO SCROLL key is pressed.
3. The terminal is placed in set-up mode.
4. CTRL/S is pressed.

The VT180 transmits the XON code to continue transmission from host computer to terminal when one of the following occurs.

1. The buffer empties.
2. The NO SCROLL key is pressed again.
3. The terminal is taken out of set-up mode.
4. CTRL/Q is pressed.

If the host computer software does not support the XON/XOFF codes, data sent during buffer full conditions or when the VT180 is in set-up mode may be lost. Set the digit associated with this feature to 1 to enable auto XON/XOFF, which is CP/M compatible.

NOTE

The VT180 always stops transmission when an XOFF (DC3) code is received and resumes transmission when an XON (DC1) code is received regardless of the auto XON/XOFF feature setting.

Wraparound
When this feature is enabled, the 81st or 133rd character (depending on the line size selected) inserted on a line is automatically placed in the first character position of the next line. If the wraparound feature is not enabled, the 81st or 133rd character and all following characters are overwritten into the last character position of the current line. CP/M compatibility requires that this feature be off; set the digit associated with this feature to 0.

New Line
The new line feature enables the RETURN key on the terminal to function like the return key on an electric typewriter. When the new line feature is enabled, pressing the RETURN key generates the carriage return <CR> and line feed <LF> codes. When a line feed code is received, the code is interpreted as a carriage return and line feed.

When the new line feature is disabled, the RETURN key generates only the <CR> code; an <LF> code causes the terminal to perform a line feed only.

NOTE

If double line feeds occur consistently, turn this feature off because the host computer is already performing this function.

CP/M compatibility requires that this feature be off; set the digit associated with this feature to 0.

Power
During initial installation, the terminal display must be set to match the power line frequency. In the United States this is 60 Hz. Set the digit associated with this feature to 0 for 60 Hz and to 1 for 50 Hz.

2.6.5.6 SET-UP B, Host Computer Compatibility – The SET-UP B features that must be selected for communication with the host computer include the transmit/receive baud rate, and serial character format (parity sense, parity, and bits per character). The settings for these features must be obtained from the host computer programmer, operator, or system manager since there are many combinations of settings designed to work with particular computers and special software. These feature settings normally change only when you need to communicate with a different computer or a unique software package.

Parity sense, parity, and bits per character are set by moving the cursor over the feature in the SET-UP B display and pressing the 6 key on the main keyboard to select the correct mode for that feature.

Parity Sense
The parity sense feature defines which of the two methods of parity checking, odd or even, is being used by the VT180. If the parity feature is on, the terminal's parity sense must be matched to the parity the host computer is sending. If the parity sense features do not match, most characters sent to the host computer are rejected even though the character was received correctly by the VT180. If parity incompatibility occurs, the checkerboard character (▒) appears on the screen in place of the received character.

NOTE
If the parity feature is turned off, the parity sense selection is ignored.

Parity
When enabled, parity checks for correct data transmission. If a transmission error occurs, the VT180 detects it and indicates its presence by placing a checkerboard character (▒) on the screen in place of the character with the error. The parity sense feature determines if the parity is even or odd. When parity is disabled, the parity bit is not included in the transmitted character and is ignored in received characters.

Bits per Character
This feature allows the terminal to transmit and receive either 7- or 8-bit characters. When set for 8-bit operation, bit 8 is set to a space (or 0) for characters transmitted and is ignored for all characters received.

Transmit Speed and Receive Speed
Transmit speed selects the speed (baud rate) and the number of stop bits per character transmitted by the terminal. This feature of the terminal must be set to match the host computer receive speed.

Receive speed selects the speed (baud rate) and the number of received character stop bits expected by the terminal from the host computer. This feature of the terminal must be set to match the host computer transmit speed.

The VT180 in terminal mode can transmit or receive at any one of the following preselected speeds: 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 9600, and 19,200 baud. In terminal mode only, the VT180 may transmit data at one speed and receive data at a different speed; this is called split baud operation. In personal computer mode, the VT180 communicates internally at a fixed speed of 15,700 baud.

When you enter SET-UP B, two numbers are displayed at the lower right-hand corner of the screen (see Figure 2-10). One number is preceded by T SPEED and identifies the speed (in bits per second) at which the terminal will transmit information to any device it is connected to. The second number is preceded by R SPEED and identifies the speed at which the terminal expects to receive information.

These speed settings can be changed to match the requirements of the host the VT180 is connected to. These changes are made in SET-UP B by means of the 7 and 8 keys. Pressing the 7 key changes the transmit speed to the next higher setting; pressing it again repeats the process, and so on, until the highest speed (19,200) has been reached. At this point, the speed cycles around to its lowest value (50) and the process continues. Press the key until you reach the speed you require.

Receive speed changes are made in precisely the same way, except that you use the 8 key. You can, if you wish, change the transmit and receive speeds simultaneously by pressing the 7 and 8 keys together.

The number of stop bits is automatically selected when the transmit or receive speed is set.

2.6.5.7 SET-UP B, Answerback Message – Answerback is a question and answer sequence in which the host computer asks the terminal to identify itself. The terminal identifies itself by sending a message consisting of up to 20 characters to the host computer. The entire answerback sequence takes place automatically without affecting the screen or requiring operator action. The answerback message may also be transmitted by pressing the CTRL and BREAK keys at the same time. This feature is not used in computer mode.

Setting the answerback message differs from setting any other terminal feature. An answerback message (see Figure 2-14) can be typed into the VT180 using the following steps.

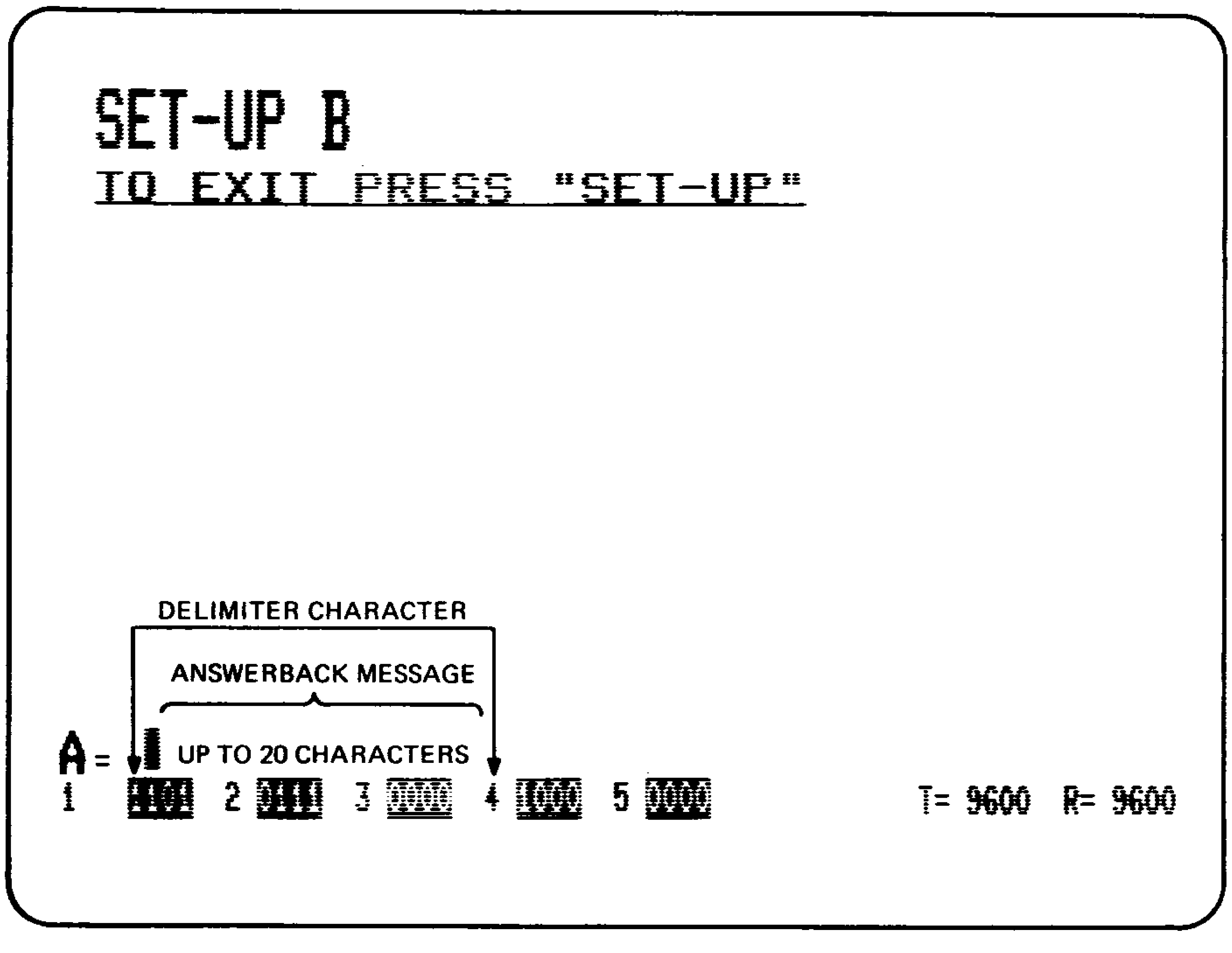


Figure 2-14 Answerback Message Display

1. Place the terminal in SET-UP B mode.

2. Press the SHIFT and A keys at the same time. The terminal responds by placing A = on the screen. (The SHIFT key is required. The CAPS LOCK key does not work here.)

3. Type the message delimiter character, which may be any character not used in the actual answerback message. (The message delimiter character is not part of the answerback message.) If a mistake is made when typing the answerback message, type the message delimiter character again and go back to step 2. This is the only way to correct errors in the answerback message.

4. Type the answerback message. The message may be up to 20 characters, including space and control characters. Control characters are displayed as a diamond character to indicate their presence in the message.

5. Typing over 20 characters ends the answerback message. You can also end the answerback message by typing the message delimiter character. Once the message delimiter character is typed, the answerback message disappears from the screen.

Once the above steps have been completed, the answerback message is temporarily stored in the VT180 and can be saved with the save operation.

CHAPTER 3
INSTALLATION AND INTERFACE INFORMATION

3.1 GENERAL

This chapter contains the information needed to unpack and install the VT18X upgrade kit to convert the VT100 to a VT180. The system installation procedure describes how to select the correct input voltage for either 115 Vac or 220–240 Vac operation, site considerations, and cabling information. The power-up and checkout procedure using ROM-based and diskette-based diagnostics is also provided.

3.2 SITE CONSIDERATIONS

The design of the VT180 normally poses few constraints on selecting a place to install the terminal. In most cases, any environment suitable to the operator is a satisfactory environment to operate the terminal in. Extremes of temperature and humidity should be avoided. A summary of VT180 guaranteed operating conditions may be found in Chapter 1.

The VT180 system consists of a modified VT100 terminal, a detachable keyboard, and either one or two dual disk drives. The dimensions of the basic units are shown in Figure 3-1.

NOTE

When installing the VT180, make sure that all power and signal cables are free from any stress, sharp bends, or obstructions. Also, be sure the position of the units allows access to the power controls on the back of the monitor and disk drive unit.

Several ventilation openings on the terminal and disk drive prevent these units from overheating. The disk drive has ventilation openings on the back, sides, and bottom of the unit. The ventilation openings for the terminal are located on the top, back, and bottom of the unit. Do not place any objects in a position that will block the air flow to these openings. Also, do not allow liquids, coins, paper clips, and other objects to enter the ventilation openings. These objects may damage the terminal or disk drive if they are allowed to come in contact with internal circuitry.

The VT180 system can be placed on a desk or tabletop. However, people usually prefer the keyboard at standard typewriter table height rather than desk height. The placement of the disk drive in relation to the terminal will depend on whether the system has one or two RX180 disk drives. If the system has one disk drive, it can be placed on top or on either side of the terminal, as shown in Figure 3-2. In a VT180 system with two disk drives, unit 1 is placed on top of unit 2 and both units can then be placed on either side of the terminal.

Position the terminal so that it faces away from light sources that reflect off the screen. If reflected light is a problem, nonreflective and antiglare screens are available from Digital. Static mats are also available for installations with static electricity problems.

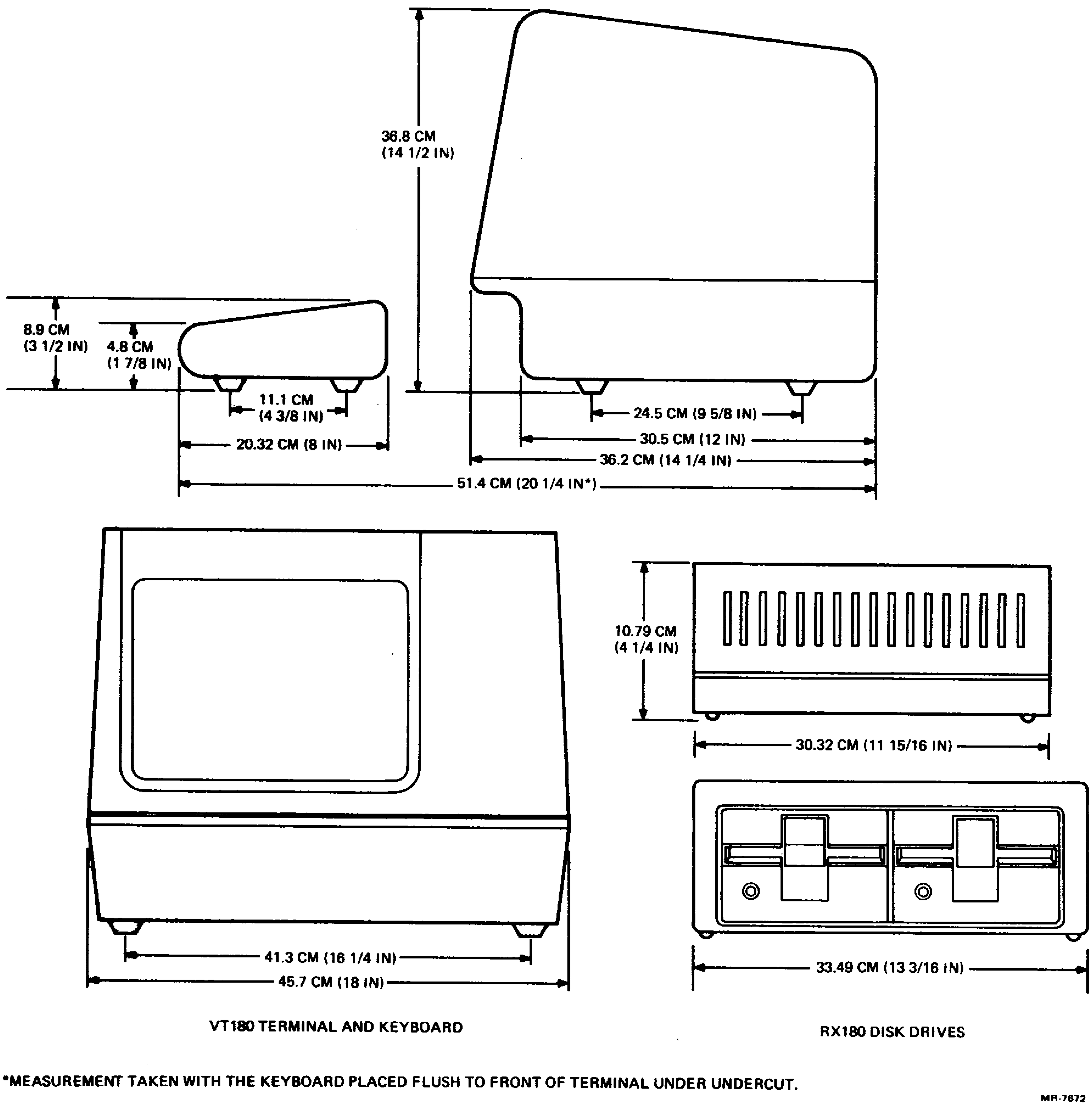


Figure 3-1 VT180 Unit Dimensions

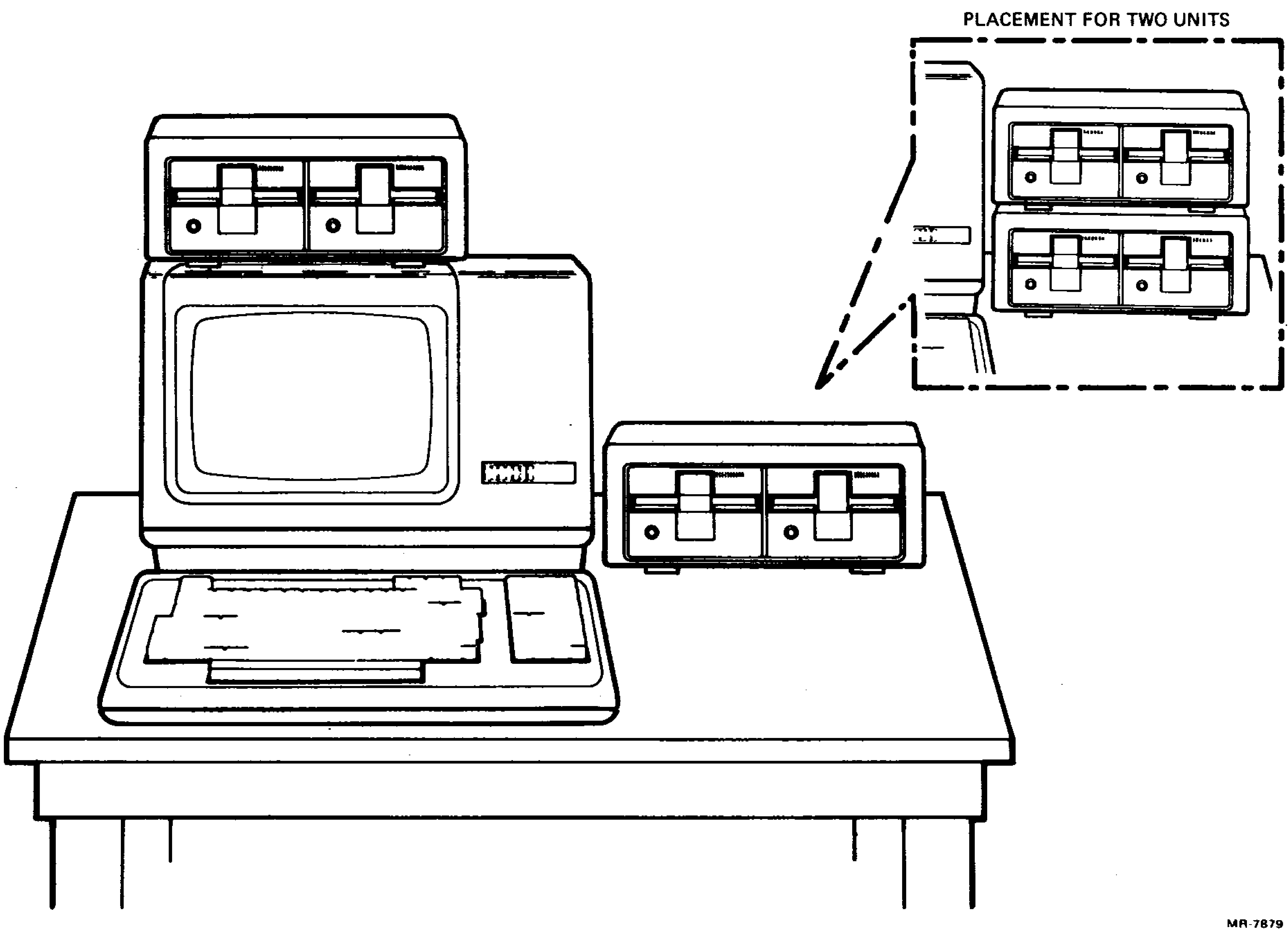


Figure 3-2 Alternatives for Placement of the Dual Disk Drive Units

3.3 UNPACKING AND INSPECTION

The VT180 system consists of a VT100 terminal and the VT18X Personal Office Computing Upgrade Kit. This unpacking and inspection procedure assumes that the user has a VT100 installed on site and wants to add the VT18X option kit to upgrade the terminal to a VT180 personal office computer. The VT18X upgrade kit is packed in a reinforced carton, which contains the following parts.

Parts Kit		Part Number
1	VT18X control module	54-15152-AA
1	VT180 paddle board	54-15150
1	VT100 expansion backplane	54-13384-01
1	Shield, card cage (RF shield)	74-25604-01
1	Shield, rear (module access cover)	74-26146
1	Cable access cover (wort cover)	74-26145
2	Card guides	12-12405
1	Cable, 16-conductor	70-08612-OM
1	RX180 dual disk drive unit (drives A and B)	RX180-AB
1	BC26K cable, terminal to disk	17-00297
1	Line cord, coiled	17-00150-01
1	Box of small miscellaneous mounting hardware	

If the VT18X upgrade kit includes two disk drive units, the second disk drive unit (drives C and D, order number RX180-AE) is shipped in a separate carton that contains the following parts.

	Part	Part Number
1	RX180-AD dual disk drive unit (drives C and D)	RX180-AD
1	BC26Z cable, disk-to-disk	17-00298
1	Line cord	17-00150-02

Instructions for unpacking the VT18X option kit are provided by the *VT18X Unpacking Guide* (EK-VT18X-PG). This unpacking guide will be the first item that is removed from the shipping carton when it is opened (Figure 3-3).

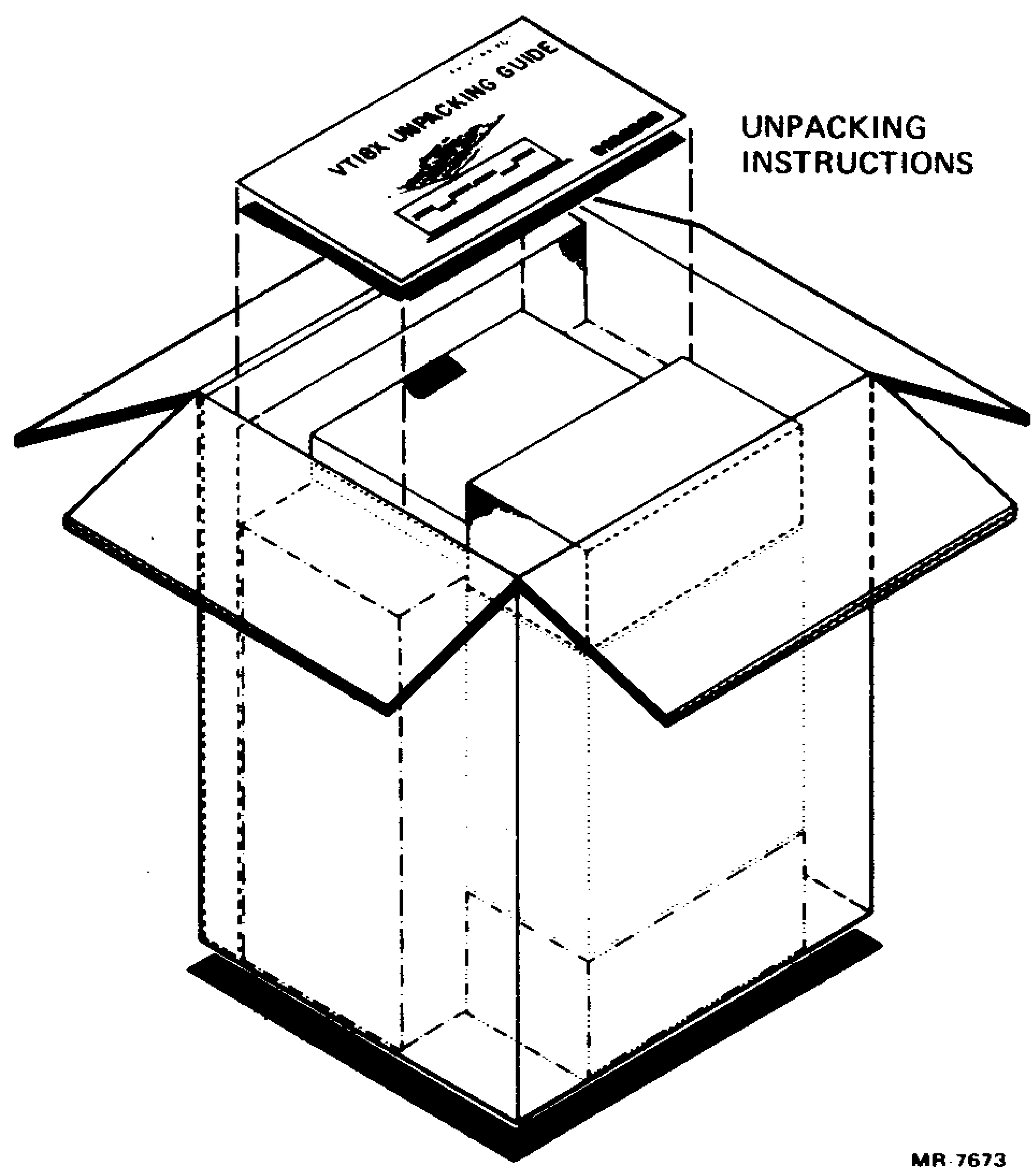


Figure 3-3 VT18X Shipping Carton

If a second disk unit (drives C and D) is included in the shipment, instructions for unpacking the unit are provided by the *RX180 Unpacking Guide* (EK-RX180-PG). This unpacking guide is contained in the RX180 shipping carton.

3.4 VT18X UPGRADE KIT INSTALLATION

This section describes the procedure for adding the VT18X upgrade kit to the VT100 video terminal. The kit also adds an RF shield to the VT100. New government rules have specified shielding of electronic equipment to prevent interference with radio equipment.

The VT18X option can be installed only in certain models of the VT100 series of terminals. Table 3-1 lists the models of the VT100 that can and cannot use the VT18X option.

Table 3-1 VT100 Series Terminals that Can and Cannot Use the VT18X Option

Model	Use VT18X Option	Cannot Use VT18X Option	Reason
VT100-AA, -AB	X		
VT100-L, - N	X		
VT100-WA, -WB	X		
VT100-WC, -WZ		X	Foreign character set
VT100-X	X		
VT101		X	Nonexpandable
VT102		X	Nonexpandable
VT103		X	LSI-11 backplane
VT105 (VT1X5)		X	Lose graphics capability
VT125		X	Lose graphics capability
VT131		X	Nonexpandable
VT132*		X	Lose block mode and local edit capability

*The terminal can use the VT18X option if it is reconfigured to a basic VT100, but it loses the feature(s) mentioned.

The tools needed for installing the VT18X upgrade kit are as follows.

1 ¼ inch nut driver
1 Phillips head screwdriver, number 1
1 Flat blade screwdriver
1 Needlenose pliers

NOTE
The VT180 does not support the 20 mA option (VT1XX-AA), nor the printer port option (VT1XX-AL, -AM, -AU, -AV).

3.4.1 Check the ROMs on the Terminal Controller Module

To use the VT18X on the VT100, the ROMs on the terminal controller module must be the same as for a standard VT100. The ROMs are the memory chips that plug into the sockets on the terminal controller module. The ROMs contain the program for the terminal operation. If the ROMs are not the same as those for the VT100, they may cause an error message or an unexpected halt. Use the following procedure to check these ROMs.

1. Remove ac power from the VT100 by setting the 1/0 switch on the back of the VT100 to 0. (See Figure 3-4.) Remove the ac line cord from the wall receptacle and from the back of the VT100. Save this ac line cord, as it will be needed later.

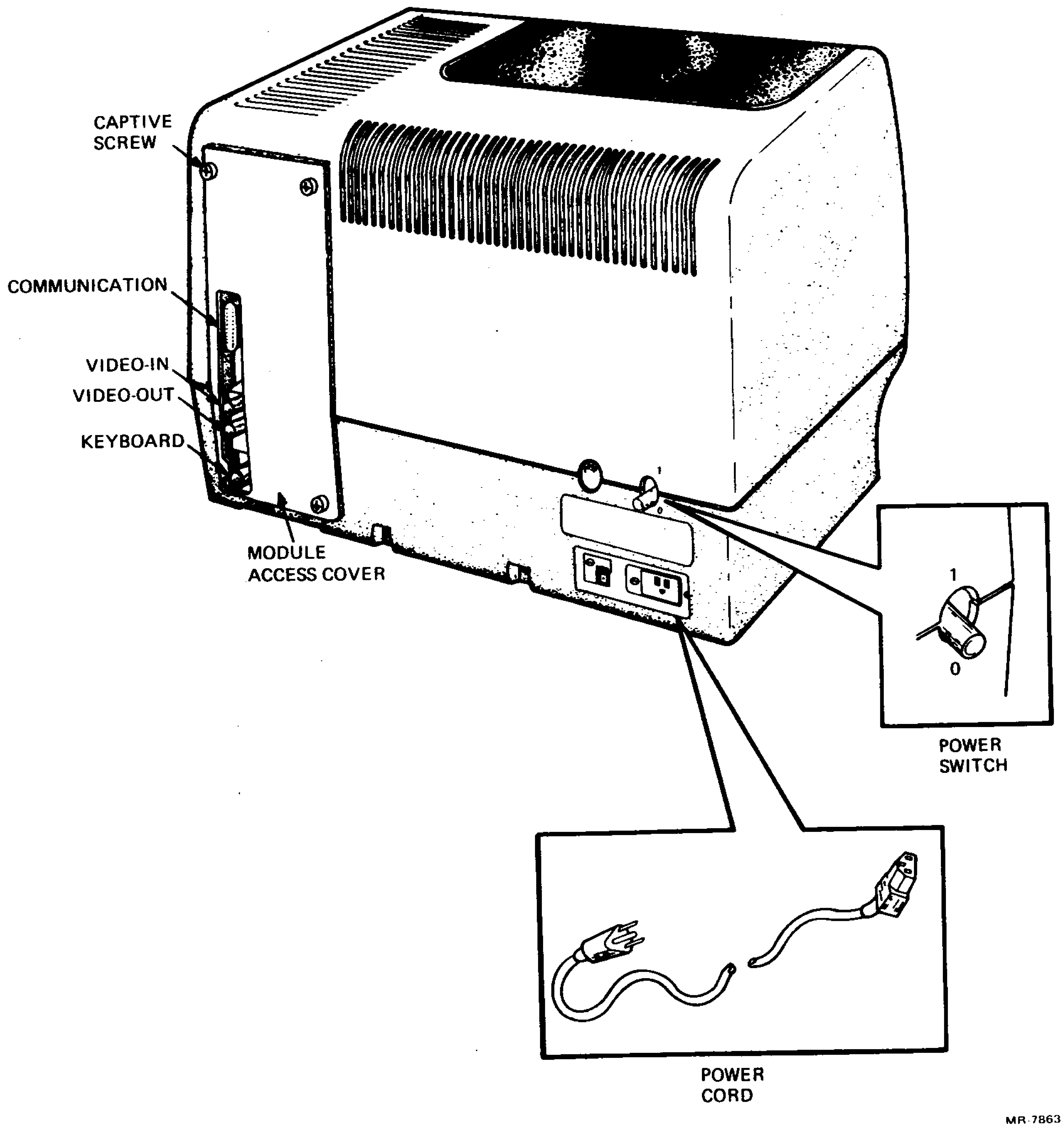


Figure 3-4 VT100 Video Terminal (Rear View)

2. Unplug the keyboard and the communication cable if it is attached to the back of the terminal. Unplug any video-in or video-out cables. (See Figure 3-4.)

3. With a screwdriver, loosen the four captive screws from the module access cover at the back of the terminal. Remove this cover; it will not be used with the VT180. (See Figure 3-4.)

4. Remove the terminal controller module (Figure 3-5) from the left side of the module access opening on the back of the terminal. Disconnect the ground wire, if present, from the module.

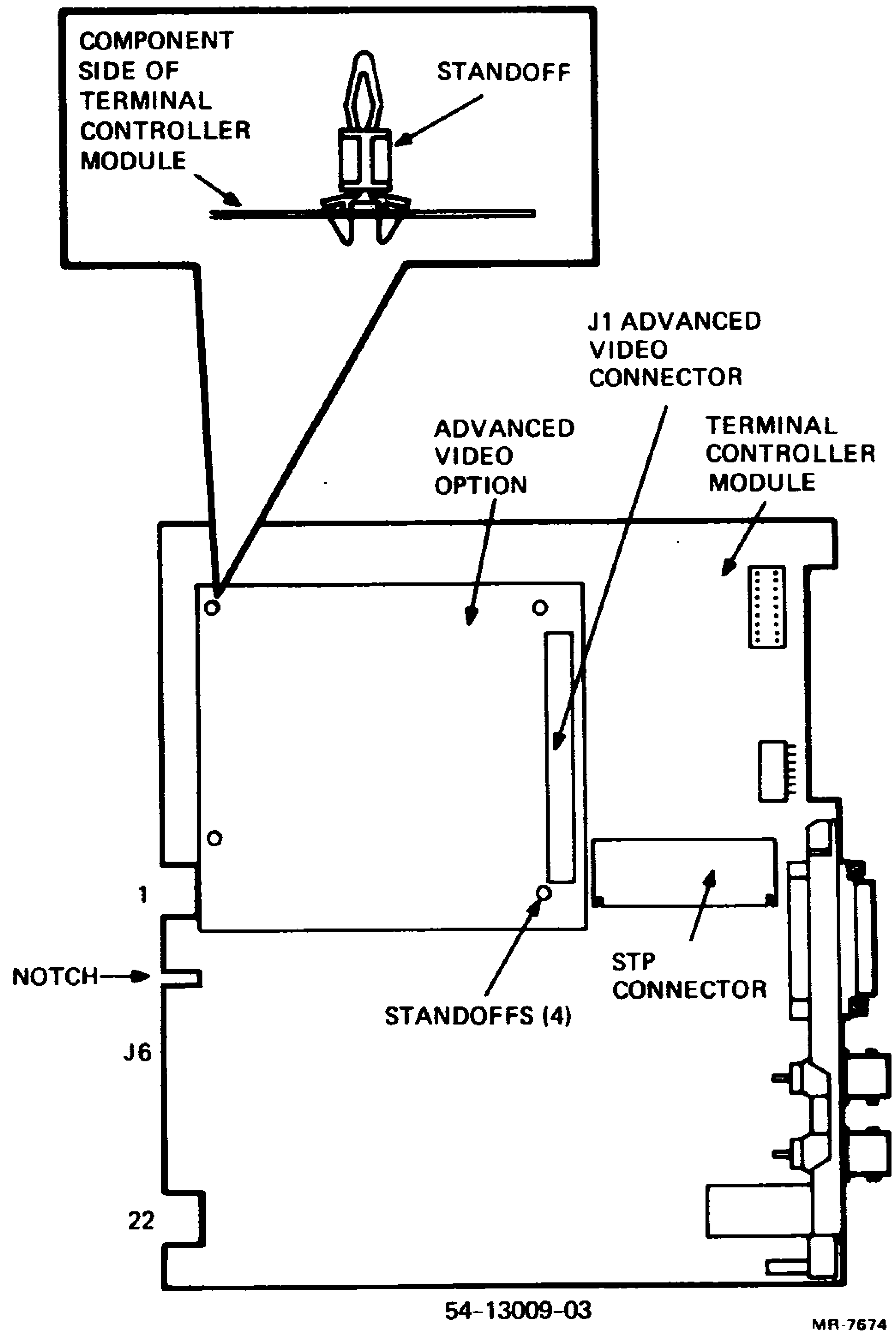


Figure 3-5 Advanced Video Option Removal and Installation

5. If present, remove the advanced video option (AVO), shown in Figure 3-5, from the terminal controller module.

6. Remove any module installed in the STP connector on the terminal controller module (Figure 3-5). The printer port option (VT1XX-AC) is not used in this new computer. If a printer port option is removed, go to Paragraph 3.4.13 for special instructions; if not, continue with step 7.

7. Check the ROMs on the terminal controller module, and compare the numbers on the module with the numbers in Figure 3-6. They should be the same; if not, go to Paragraph 3.4.13 for ROM removal and replacement.

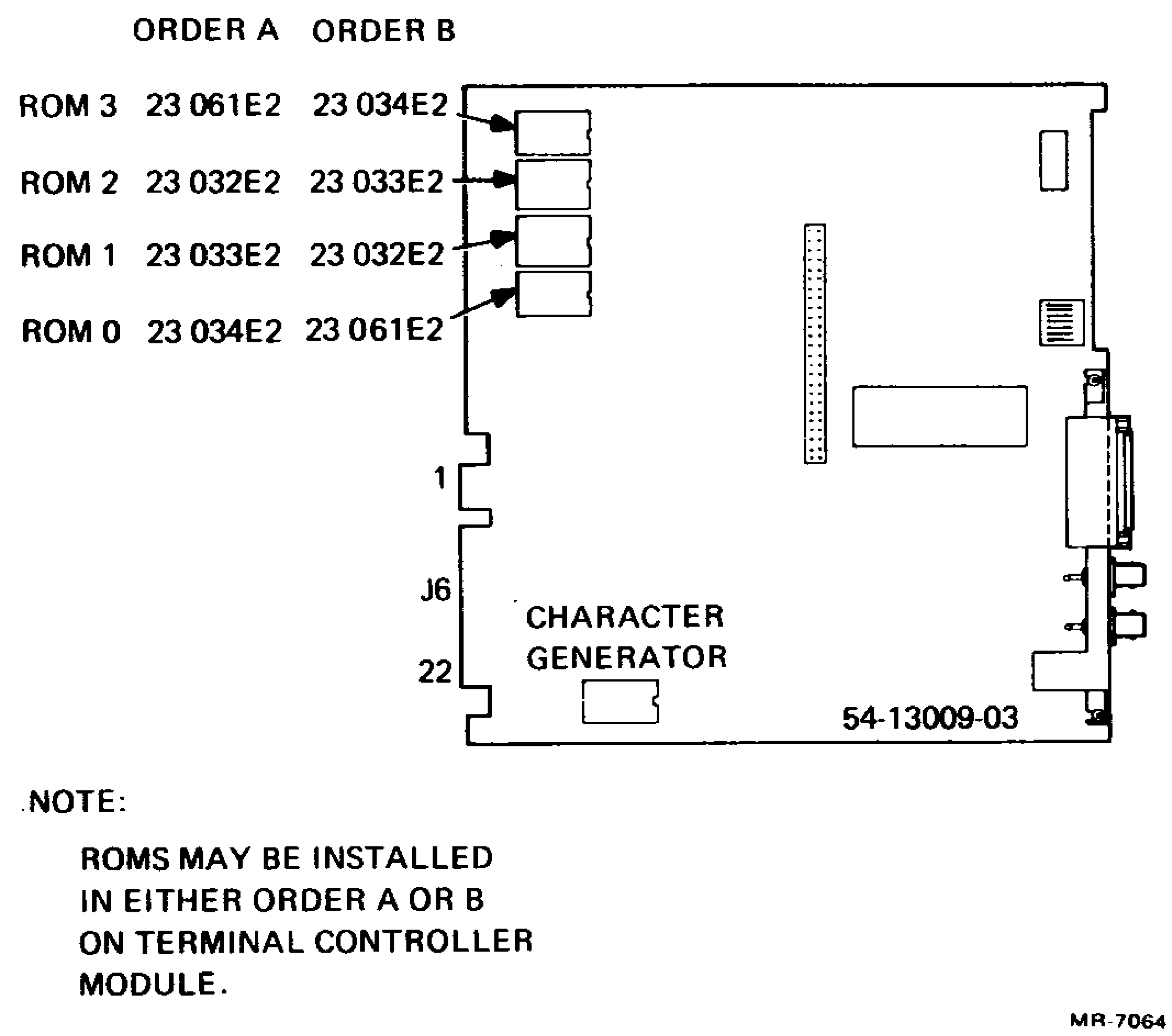
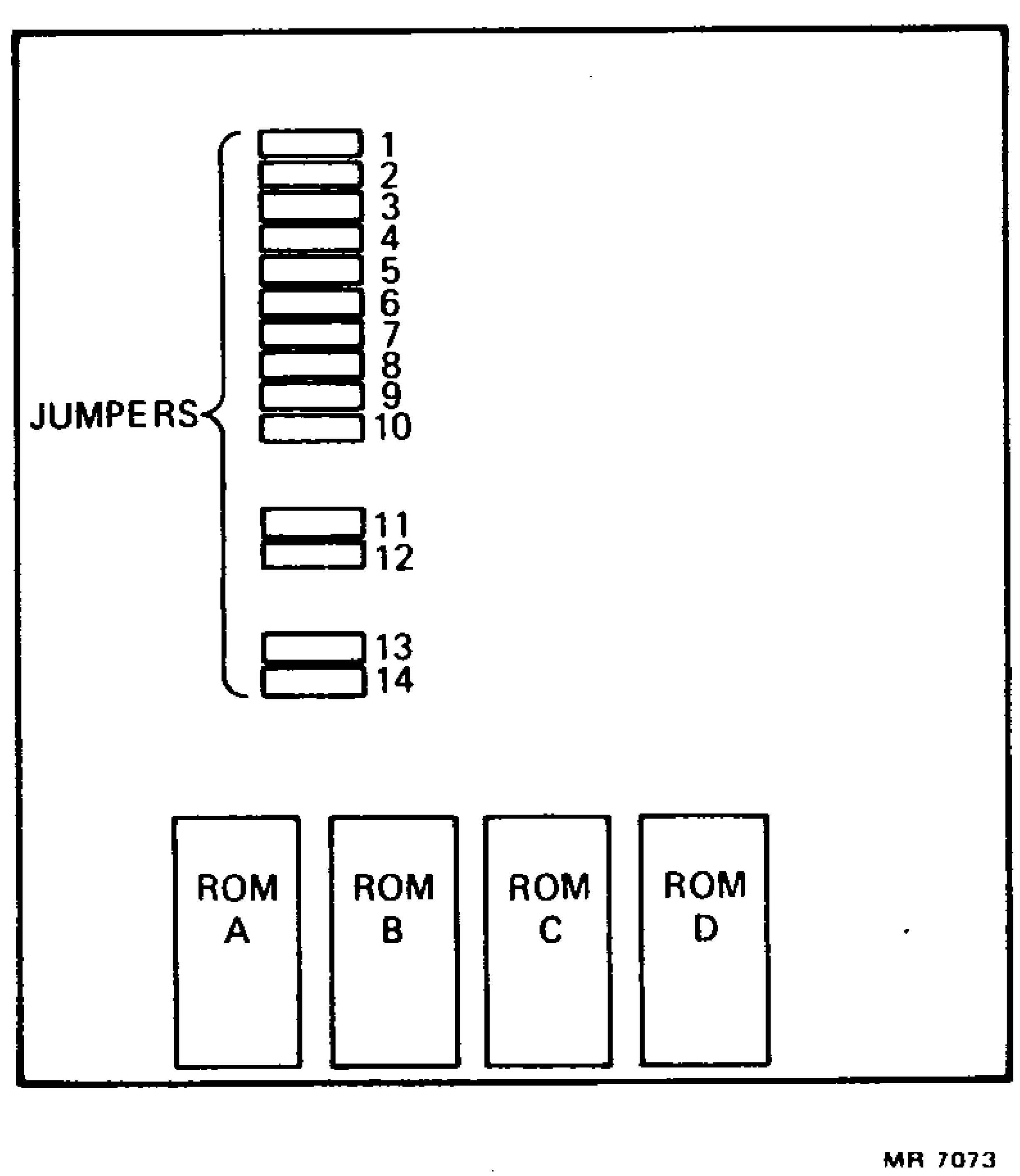


Figure 3-6 Checking ROM Numbers on the Terminal Controller Module

8. If previously removed, check for the presence of ROMs and jumpers (or switches) on the advanced video option (AVO). Except for a VT100 with a word processing option, the VT180 uses no ROMs or jumpers on the AVO. (See Figure 3-7.) If the AVO has switches instead of jumpers, see Figure 3-8.



3-7 Advanced Video Option with Jumpers

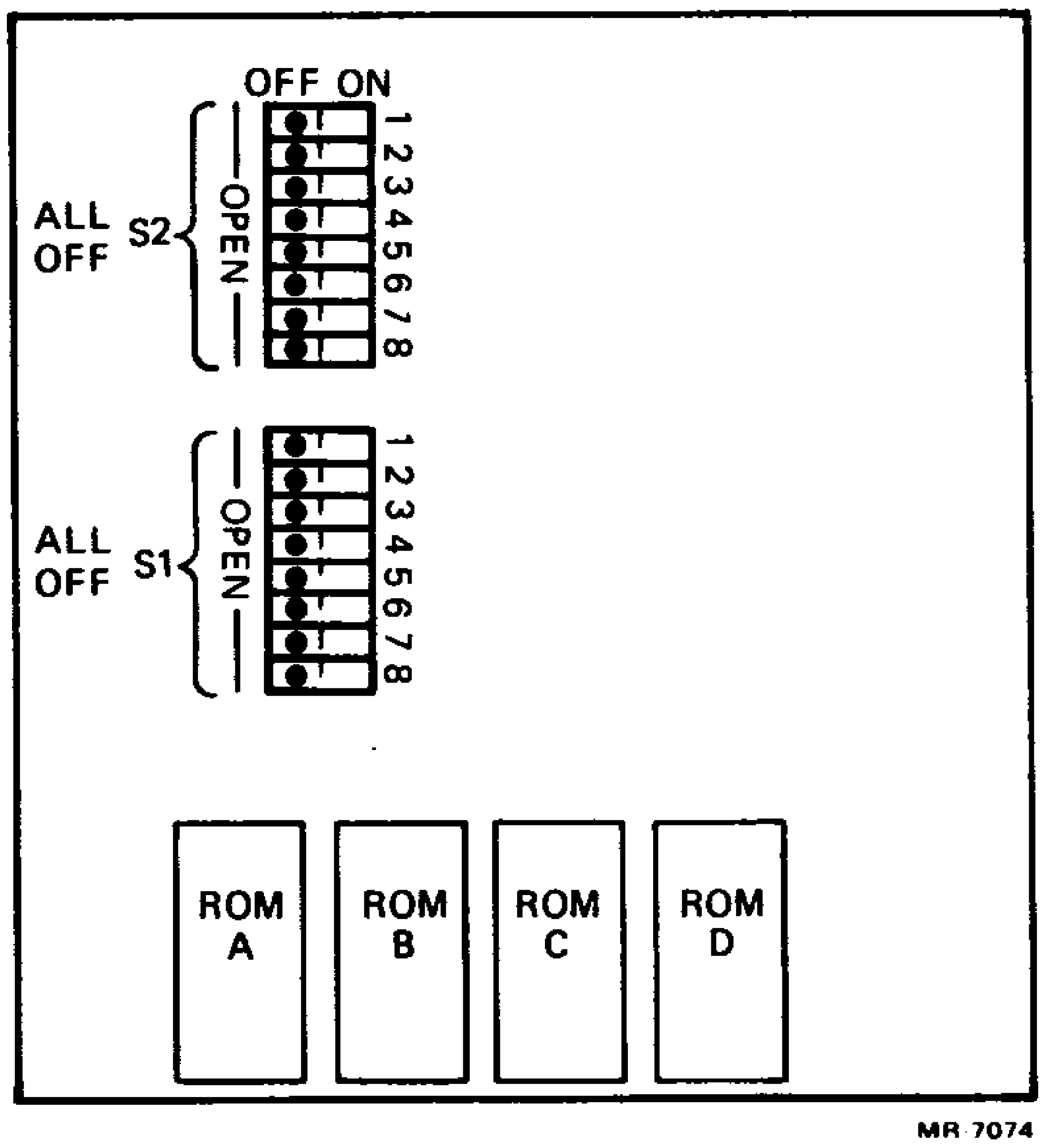


Figure 3-8 Advanced Video Option with Switches

NOTE
For an AVO on a VT100 terminal with a word processing option installed (VT100-WA, WB), refer to Paragraph 3.4.14 for special configuration.

9. Reinstall the advanced video option on the terminal controller module. (See Figure 3-5.)

3.4.2 Install the VT180 Paddle Board
Use the following procedure to install the VT180 paddle board.

1. Insert the VT180 paddle board (54-15150) in the STP connector on the terminal controller module (Figure 3-9). Fasten this paddle board to the terminal controller module through the fiber spacer with a 4-40 by ¼ inch Phillips head screw and a flat nylon washer.

2. Place one end of the 16-conductor ribbon cable in connector J2 on the VT180 paddle board. Extend the cable to the right of the module (Figure 3-9). Make certain that the red line on the ribbon cable is facing pins 1 and 16 of connector J2.

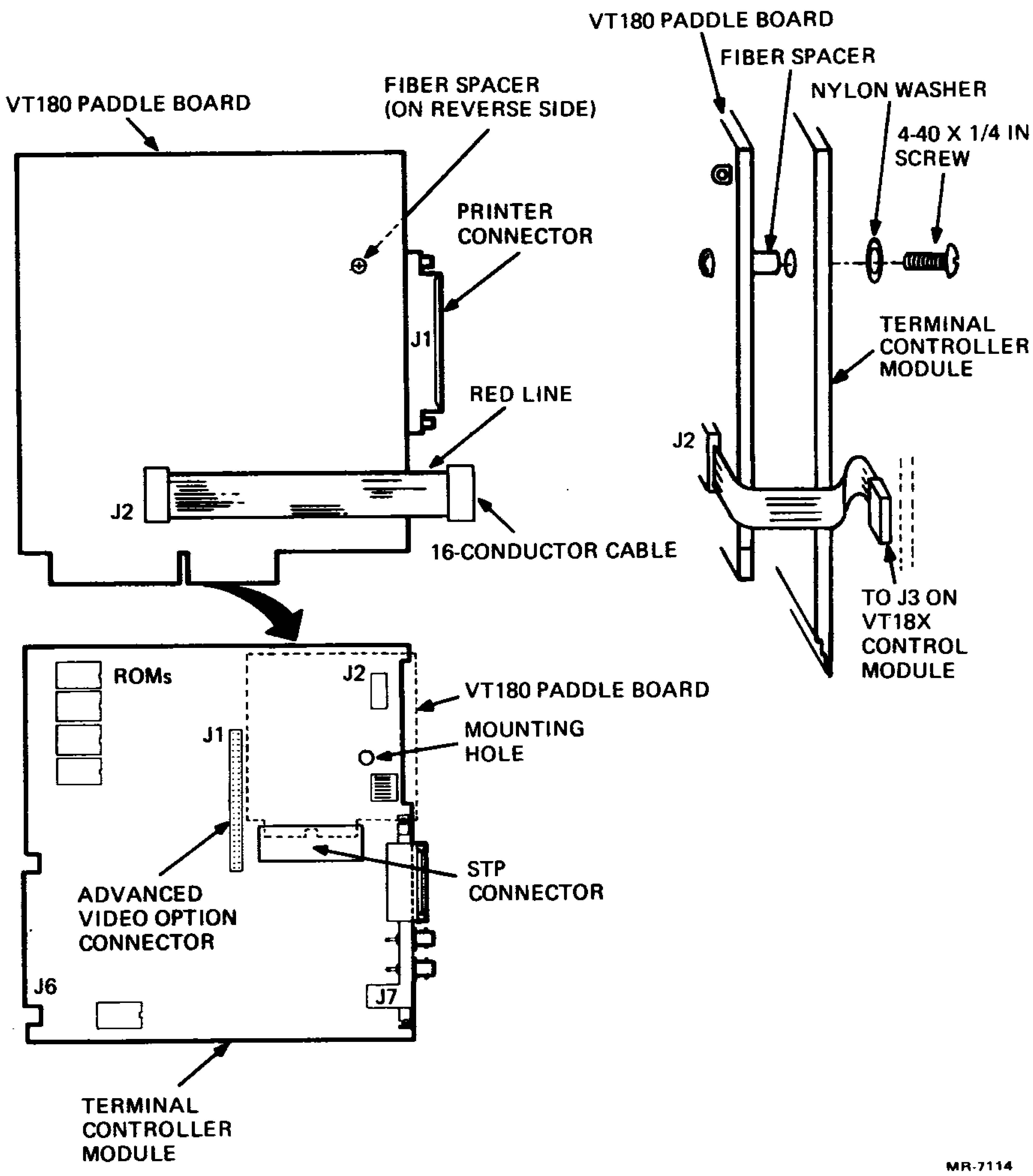


Figure 3-9 Installing the VT180 Paddle Board

3.4.3 Install the Expansion Backplane on the Card Cage

Use the following procedure to install the VT100 expansion backplane.

1. Remove the top cover on the video terminal as follows.

   a. Using a scriber, release the two front pop fasteners found under the video screen. (See Figure 3-10.)

   b. Next, release the two pop fasteners found under the lower back edge of the bottom cover. (See Figure 3-10.)

   c. Remove the top cover by lifting it straight up.

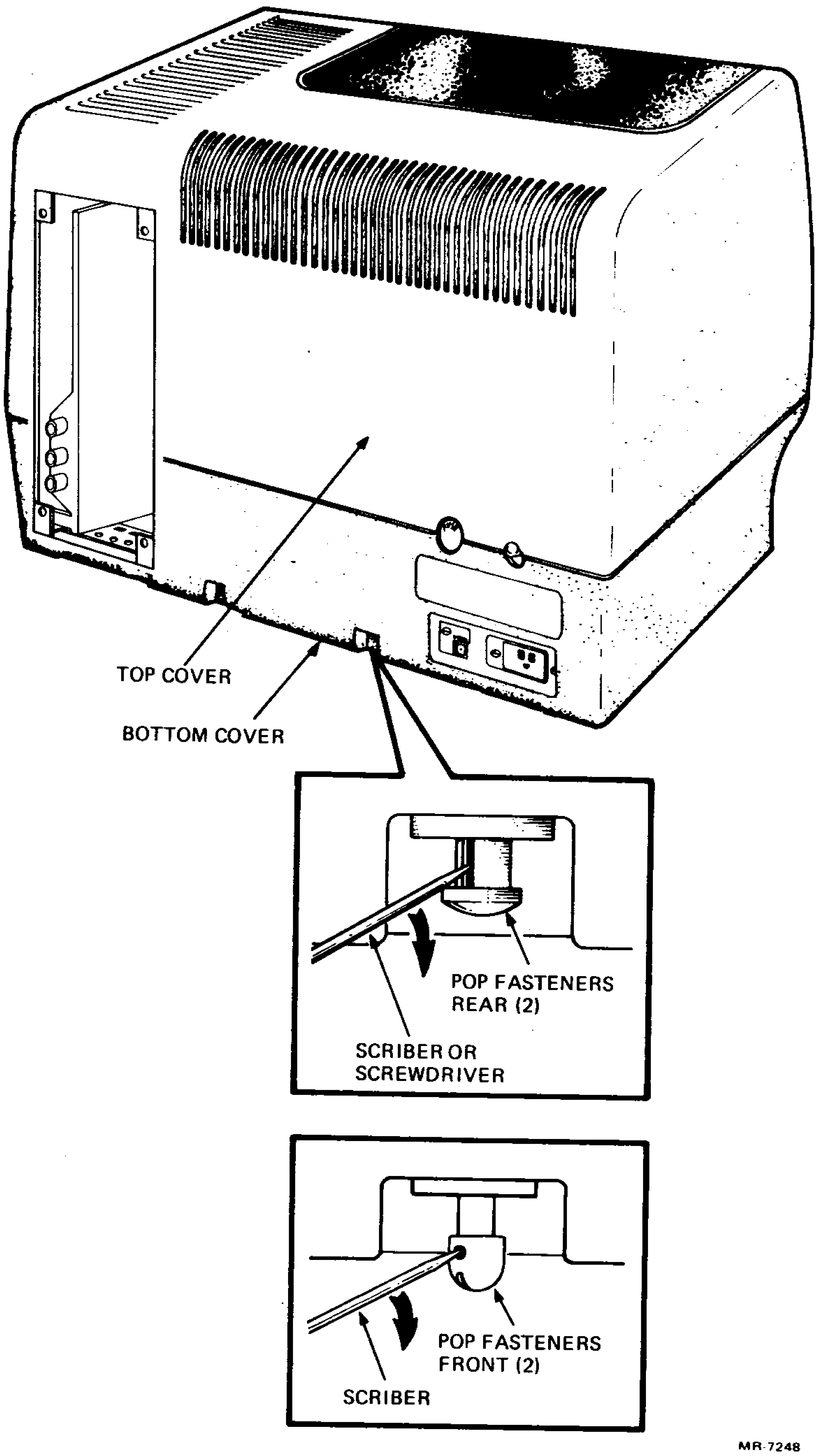


Figure 3-10 Top Cover Removal

2. Remove the bottom cover on the video terminal as follows.

   a. When facing the front of the terminal, turn it on its left side and remove the four screws (if present) fastening the bottom cover to the chassis during shipment. Save these screws if the terminal is to be sent to another location. Turn the terminal upright (Figure 3-11).

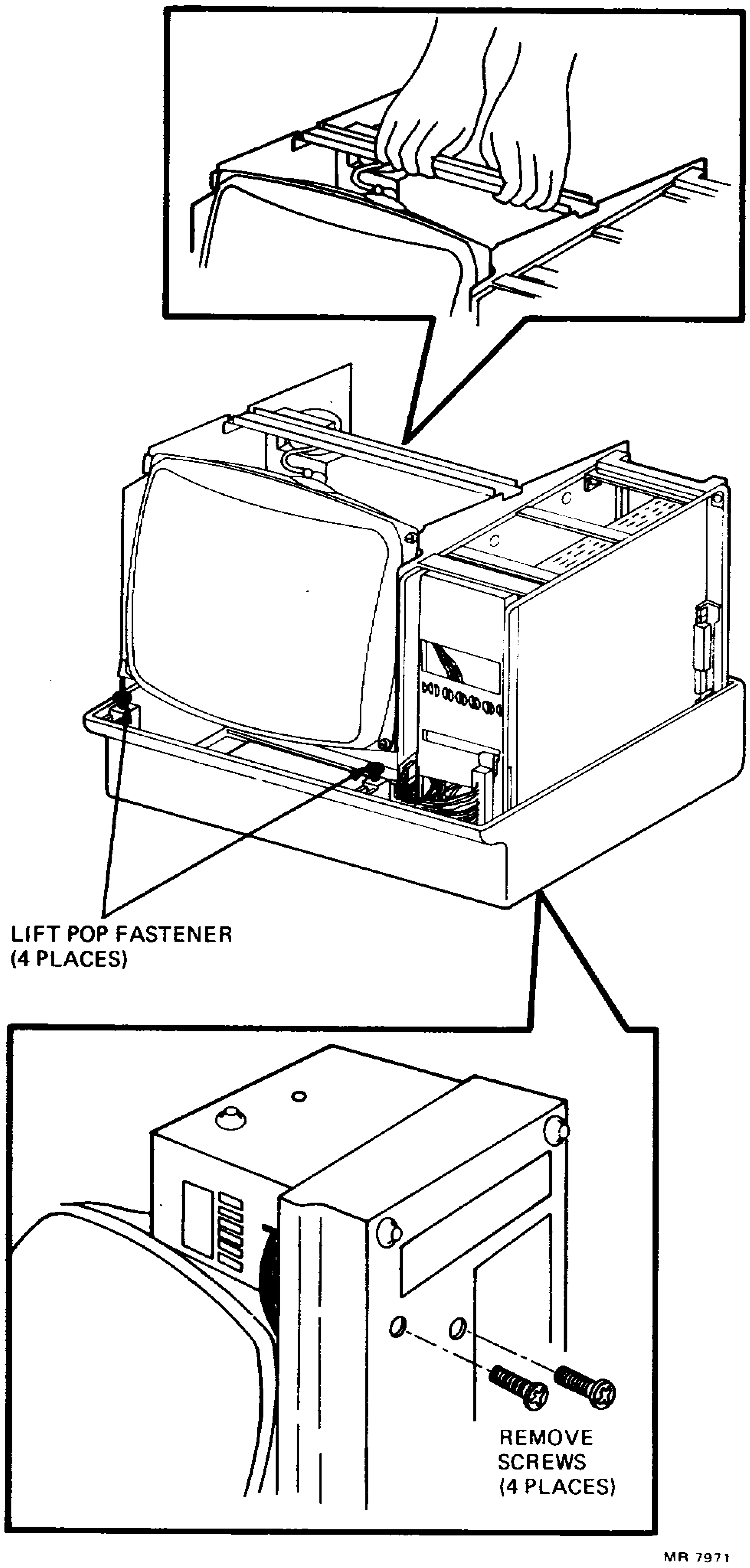


Figure 3-11 Removing the Bottom Cover

b. Find the four pop fasteners holding the chassis to the bottom cover. Pull the fasteners up until they click.

c. Using both hands, grasp the chassis by its center support bar and lift it up and out of the bottom cover.

3. Remove the 22-pin connector (Figure 3-12) from the front, right chassis by releasing the two retaining rings from its edge with needlenose pliers, or lift the clips off the top and bottom of the connector and discard.

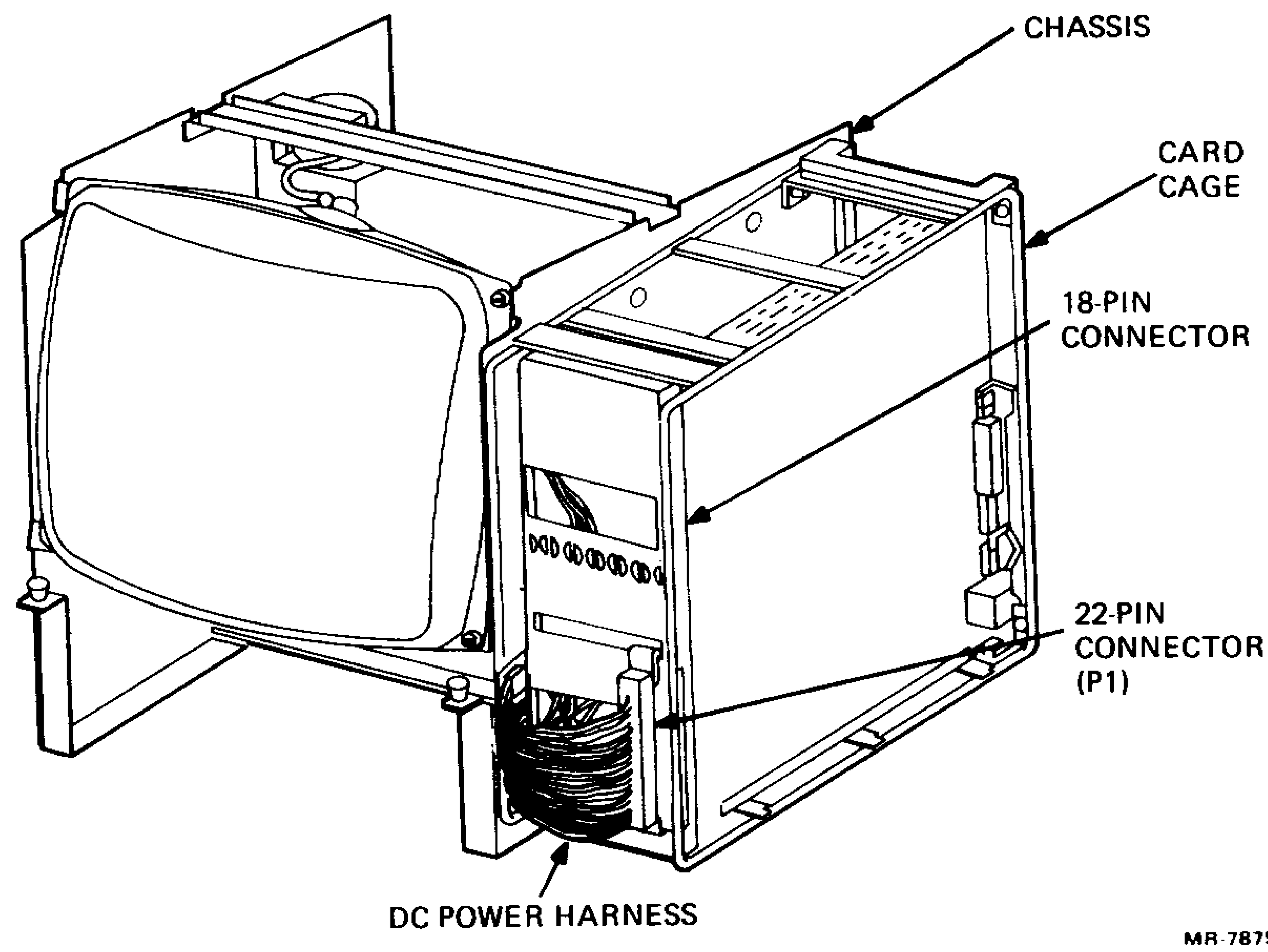


Figure 3-12 Disconnecting the dc Power Harness

4. The expansion backplane, shipped with the VT18X personal office computing option, has a key plug in connector J6 on the backplane. (See Figure 3-13.) This key plug is for the new VT100 terminal controller module (54-13009-03), which has a slot in its edge connector J6.

   Examine the terminal controller board in your VT100 for a notch in connector J6. (See Figure 3-6.) If the notch is not present, you will have to remove the key plug from J6 of the expansion backplane or you will not be able to insert the module into the backplane. Use needlenose pliers to pull the key plug out of the connector on the backplane.

5. Install the VT100 expansion backplane (54-13384-01) to the front, right chassis on the terminal. Use four 4-40 by ½ inch screws, round fiber spacers, and kep nuts. (See Figure 3-14.) Install the screws through the top and bottom holes in connectors J4 and J6 on the expansion backplane and fasten the backplane to the card cage.

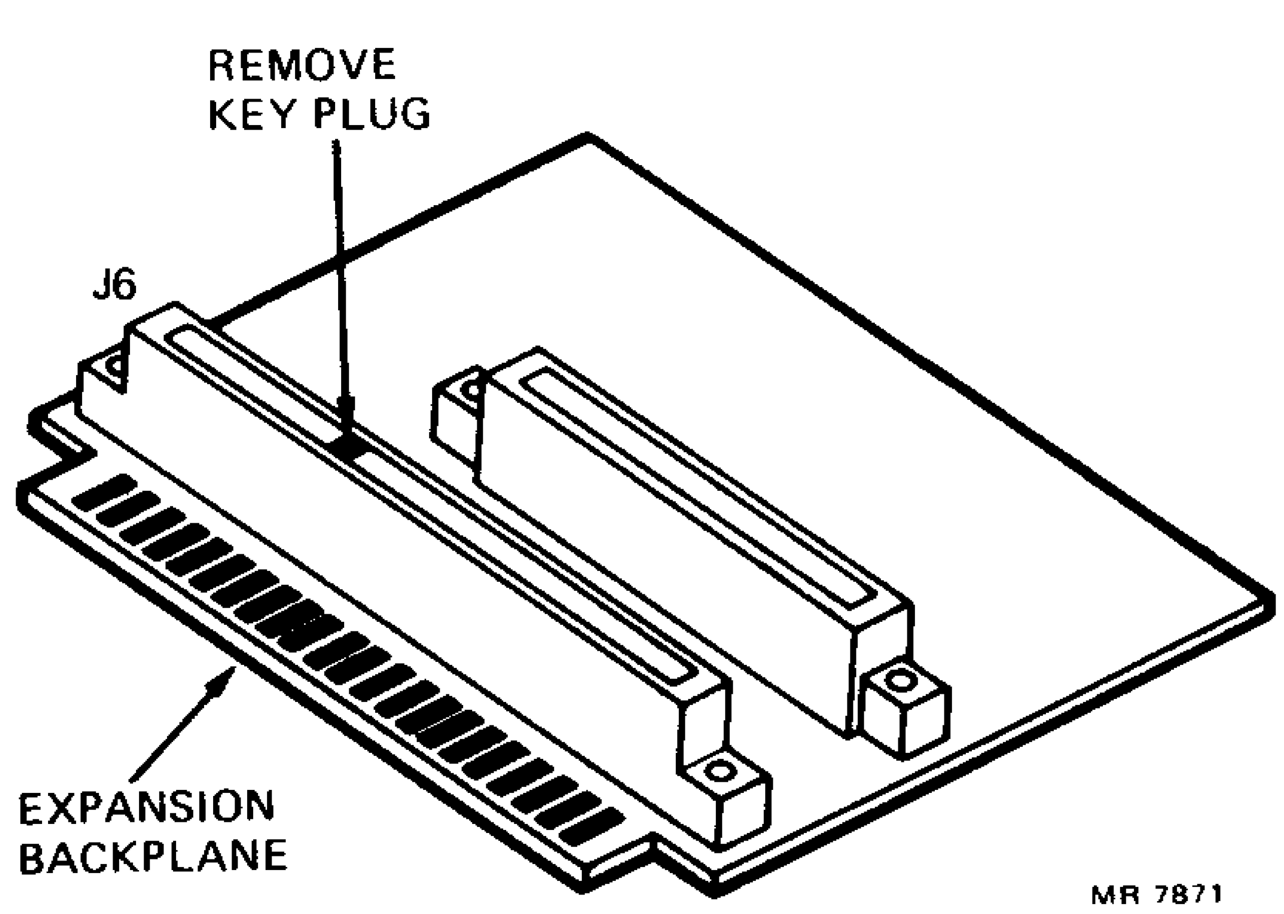


Figure 3-13 Remove the Key Plug from the Expansion Backplane

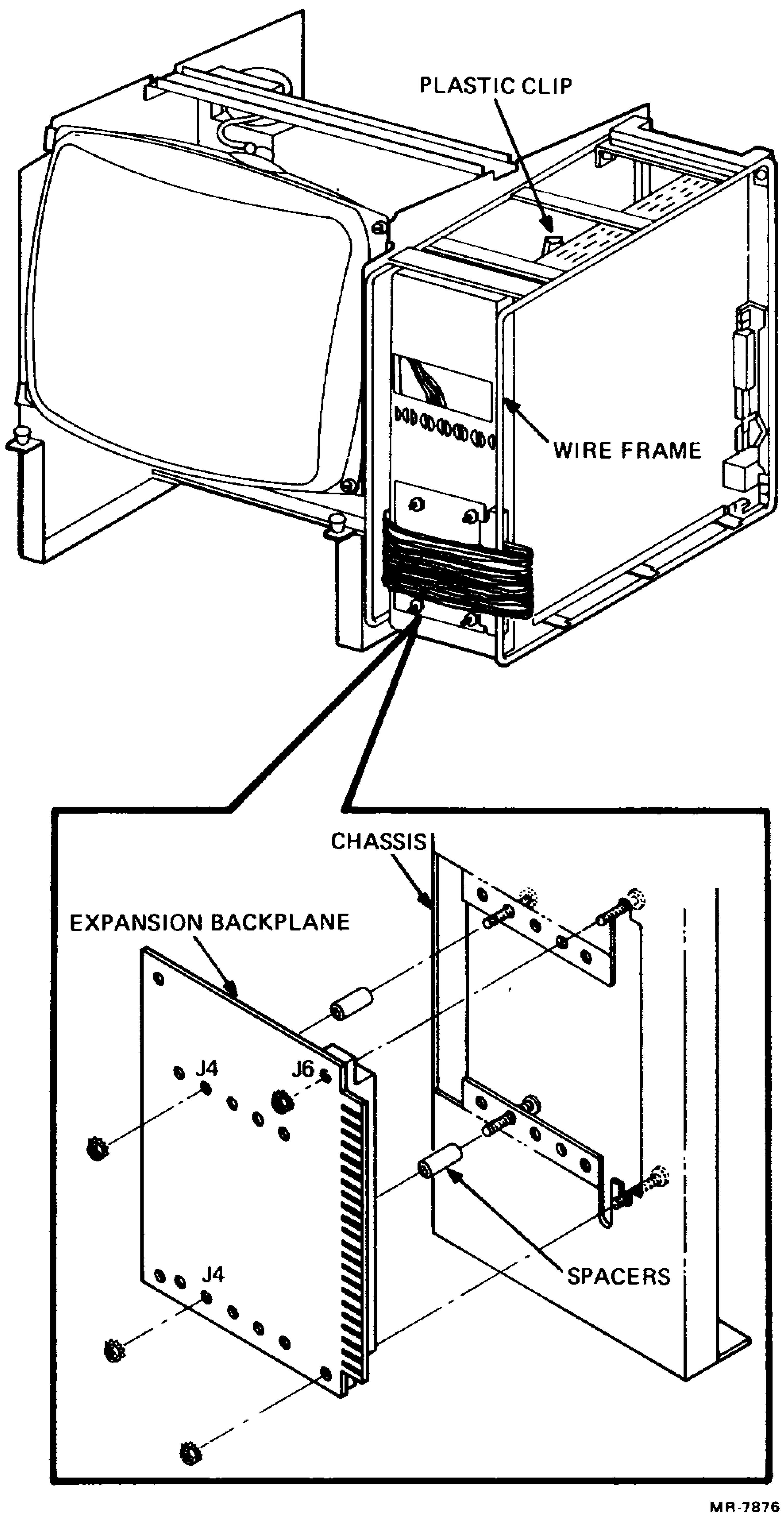


Figure 3–14 Installing the Expansion Backplane

6. Bend the dc power harness around the card cage and install the 22-pin connector on the expansion backplane module fingers. You may have to remove the shorter wires from the plastic clip on the chassis. The dc power harness must be flat against the chassis to permit the RF shield to slide over it during the installation.

NOTE

On early VT100 video terminals (prior to 1979), a nylon key plug was installed in the VT100 dc power harness between pins 5 and 6 of connector P1. This plug ensured correct alignment of the terminal controller module, which had a slot in its connector J6. The slot was later removed and the key plug was no longer needed.

When installing the VT18X into an early VT100, you must remove the key plug from connector P1 of its dc power harness or it will not fit on the edge of the new expansion backplane. Use needlenose pliers and pull the key plug out of the connector.

3.4.4 Install the Card Guides

Install a card guide at the top and at the bottom of the card cage so they are lined up with connector J2 of the expansion backplane. (See Figure 3-15.)

NOTE

The tabs on the card guide break easily; use a steady vertical pressure when installing them.

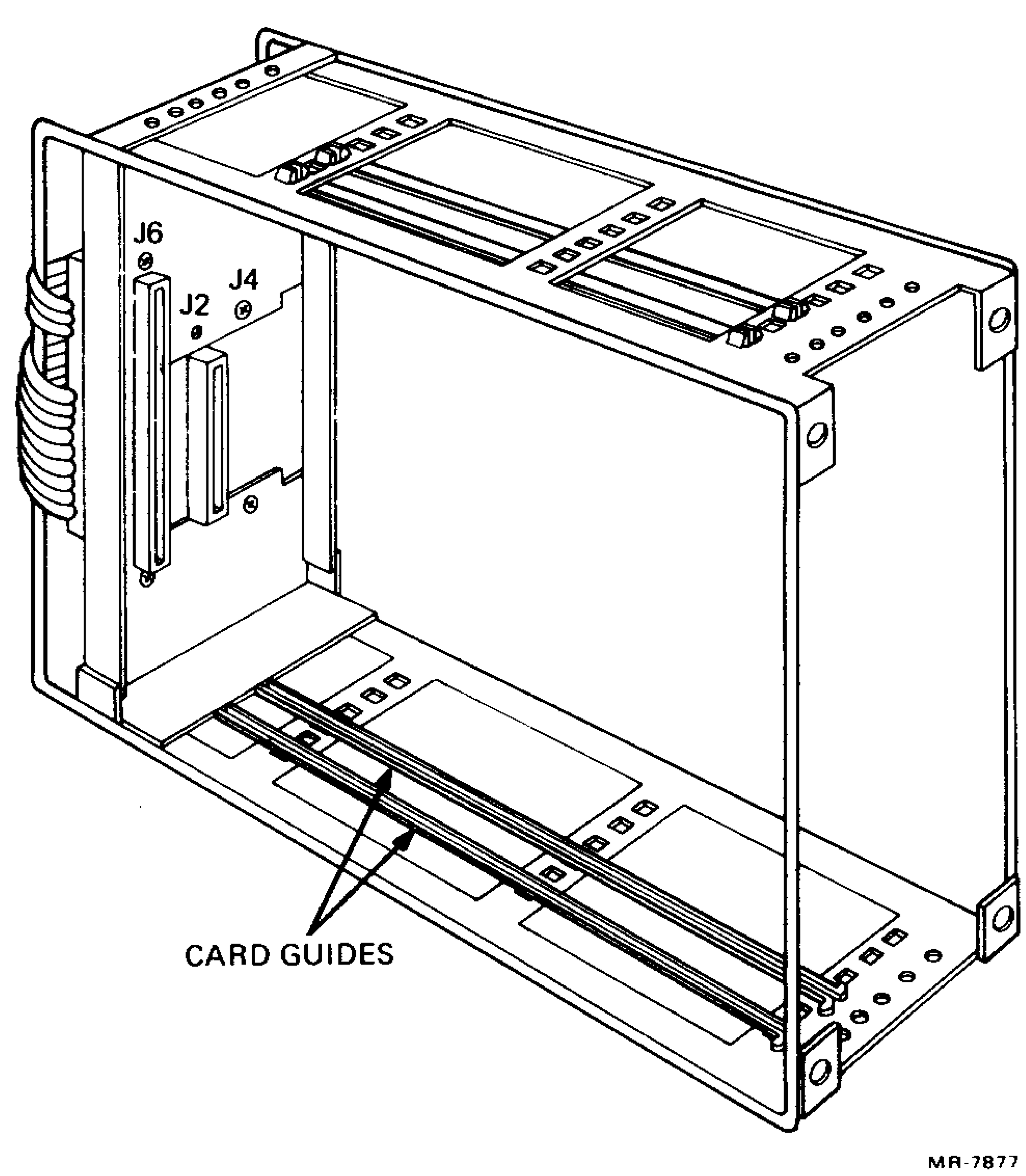


Figure 3-15 Installing Card Guides

3.4.5 Install the RF Shield

Use the following procedure to add the RF shield to the video terminal.

NOTE

Set the chassis on a protective material to protect the terminal's parts and the surface on which you are working.

1. Set the chassis on end with the card cage up (Figure 3-16).
2. Remove the four ¼ inch hex-head screws from the card cage – two on the top and two on the bottom.
3. Slide the RF shield on the card cage (Figure 3-16).
4. Using a scriber, line up the screw holes and install the same four hex-head screws.

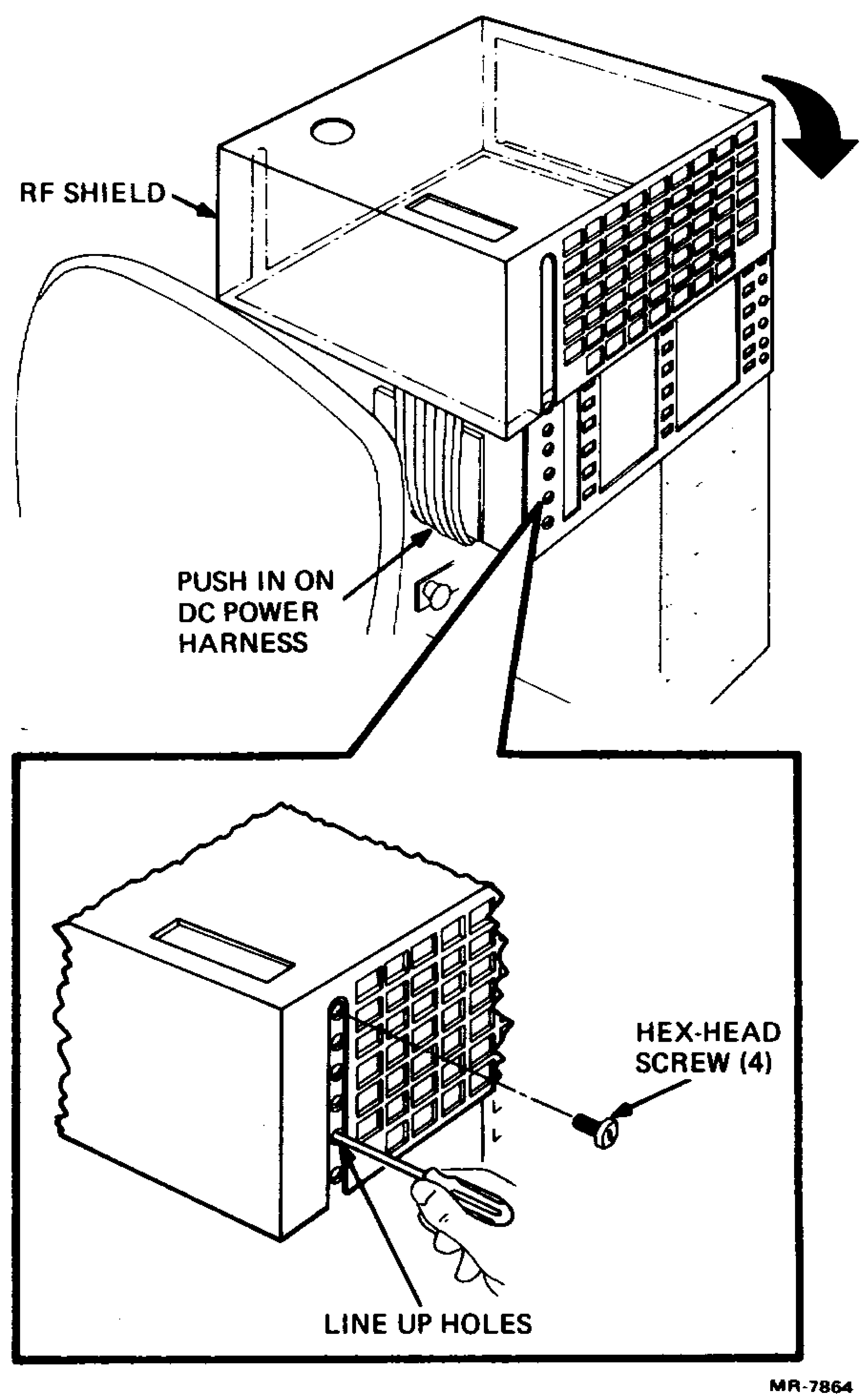


Figure 3-16 Installing the RF Shield

3.4.6 Install the Terminal Controller Module

Install the terminal controller module in its original slot (J6) in the left side of the card cage (Figure 3-15).

3.4.7 Install the VT18X Control Module

Use the following procedure to install the VT18X control module.

1. Check the communications switches on the VT18X control module (Figure 3-17) for the correct positions, which are listed in Table 3-2. The switches, as set, allow you to run the VT180 with most full- and half-duplex communications modems with application software. Table 3-2 shows the standard configuration and the function enabled by each switch.

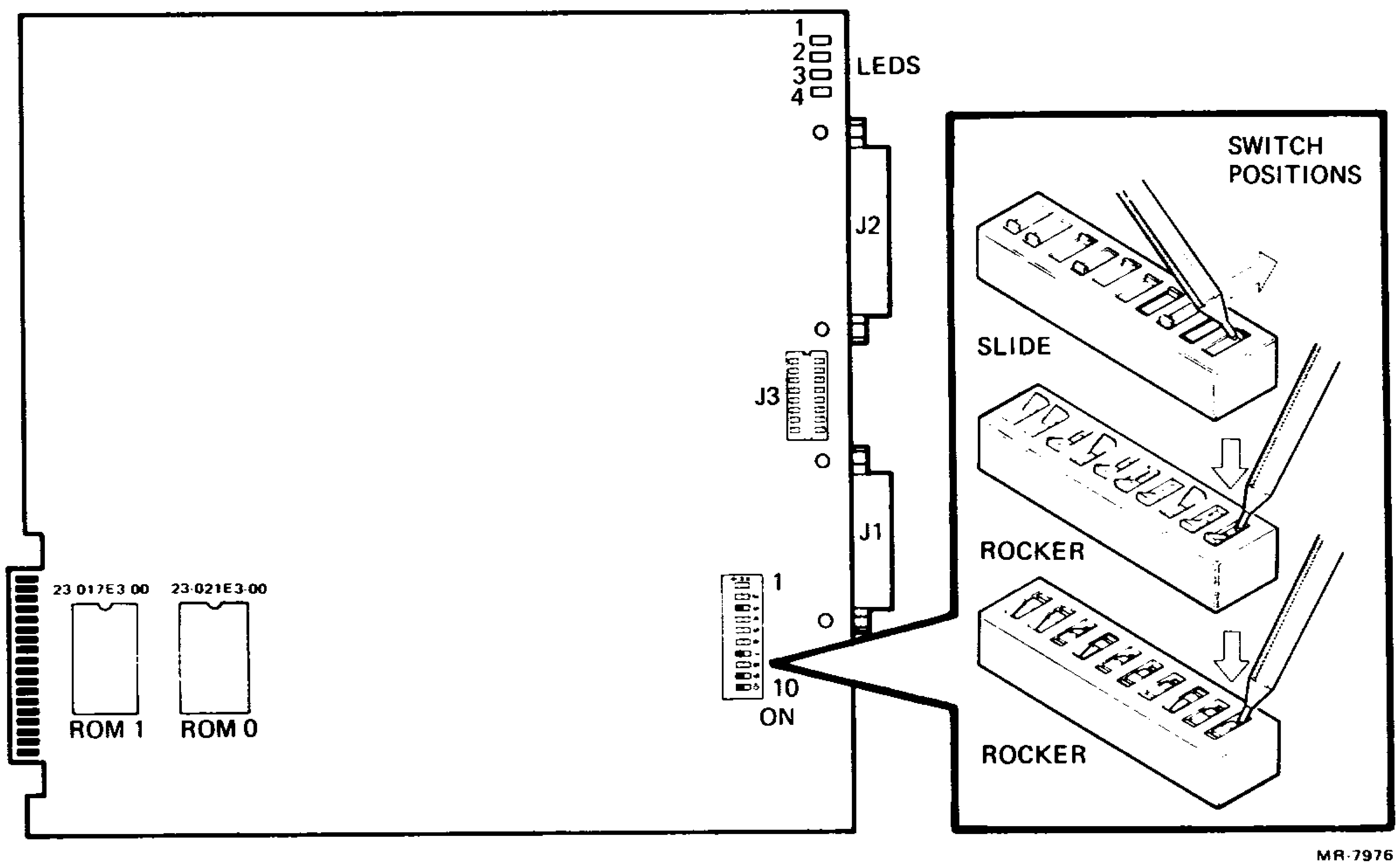


Figure 3-17 Setting the VT18X Control Module Switches

Table 3-2 VT18X Control Processor Module Communication Switches

Switch	Standard Setting	Name	Function Enabled	Source	Comm Port (J1) Pin Assignment	Circuit CCITT/ EIA
1	On	RTS	Request to send	From VT180	4	105/CA
2	On	CTS	Clear to send	To VT180	5	106/CB
3	Off	SCTS	Secondary clear to send	To VT180	13	121/SCE
4	On	SI (SRLSD)	Speed indicator (FDX) (Secondary carrier detect) (HDX)	To VT180	12	112/CI (109/CF
5	On	SRTS	Secondary request to send	From VT180	11	120/SCA
6	On	TXD	Transmitted data	From VT180	2	103/BA
7	Off	STXD	Secondary transmitted data	From VT180	14	118/SBA
8	On	SRTS	Secondary request to send	From VT180	19	120/SG
9			Not used			
10	Off	SPDS	Speed select (HDX)	From VT180	23	111/CH

2. Next, slide the VT18X control module partially in the card guides for J2 of the backplane. (See Figure 3-15.)
3. Attach the 16-conductor ribbon cable from the VT180 paddle board to the IC connector J3 on the VT18X control module. Do not invert the cable; the red line on the cable should be on top, as shown in Figure 3-18.
4. Slide the VT18X control module into connector J2 of the backplane (Figure 3-15).

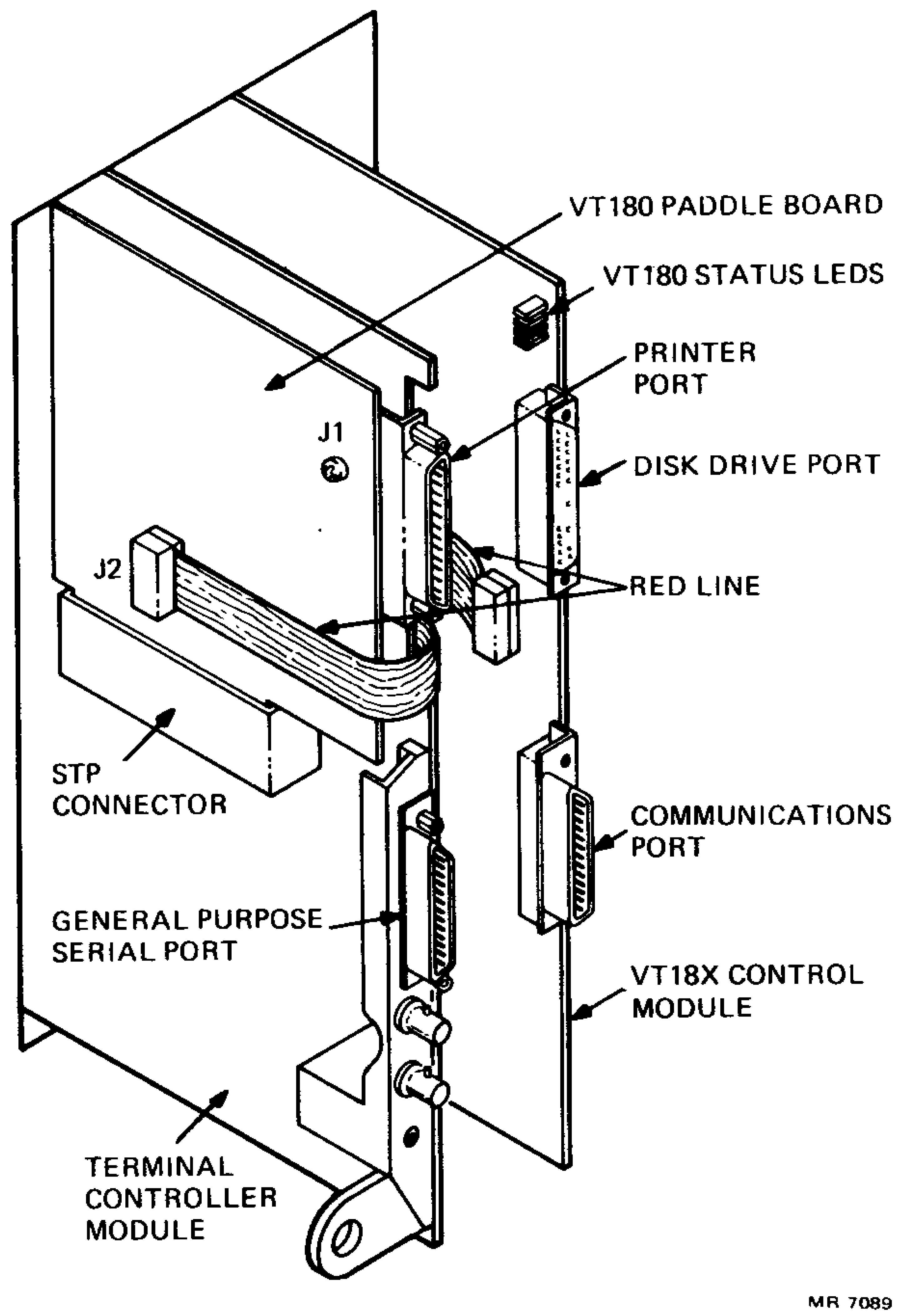


Figure 3-18 Installing the VT18X Control Module

3.4.8 Install the Chassis in the Bottom Cover

Place the chassis in the bottom cover and fasten the bottom cover with the four pop fasteners. If the terminal is to be sent to another location, turn the terminal on its left side and install the screws previously removed from the bottom (Figure 3-11).

3.4.9 Install the VT180 Logo

Use the following procedure to install the VT180 logo.

1. With a small screwdriver and pliers, remove the two retaining rings that hold the VT100 logo to the inside of the top cover. (See Figure 3-19.)

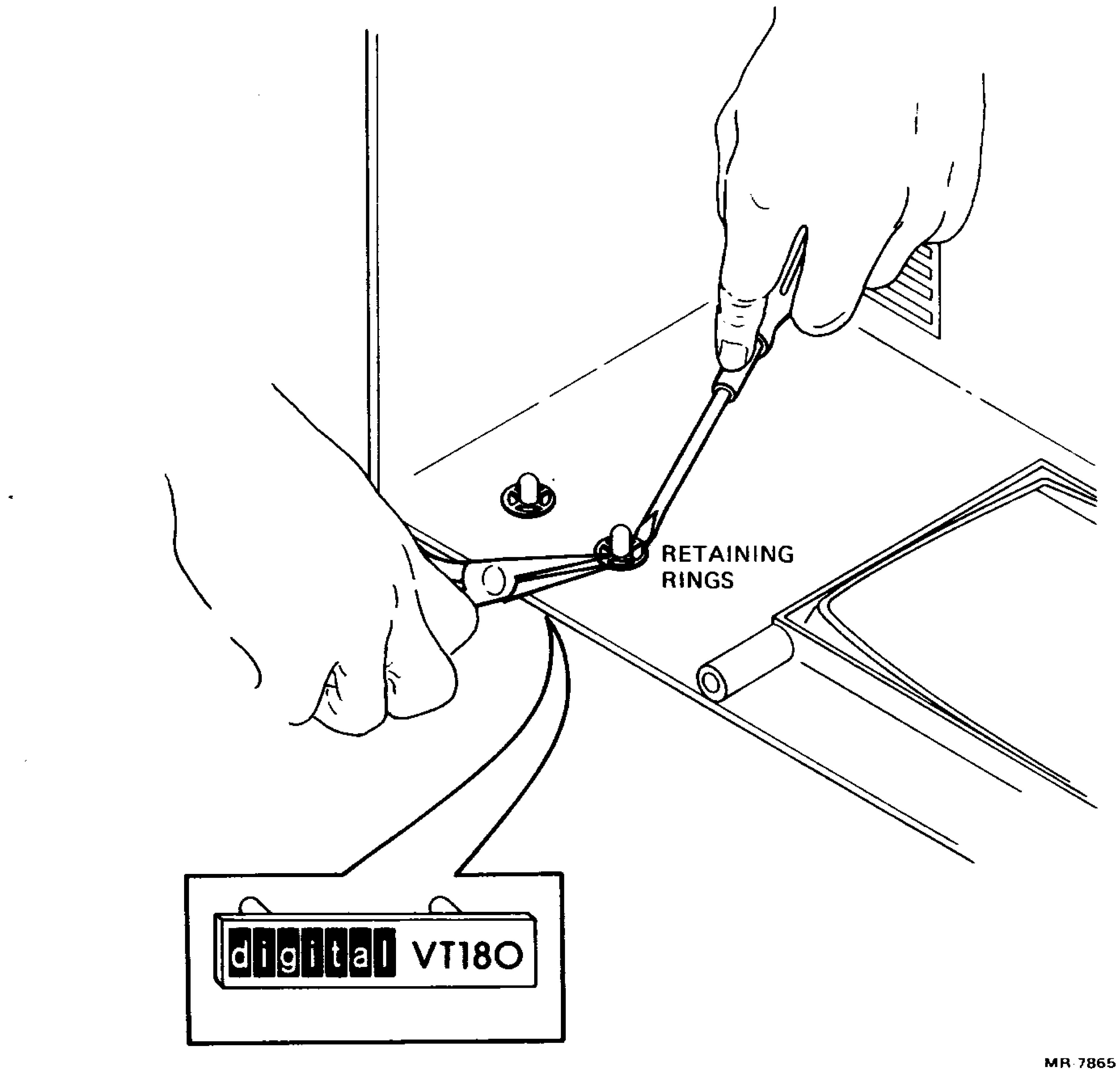


Figure 3-19 Removing the VT100 Logo and Installing the VT180 Logo

2. Remove the VT100 logo and place the VT180 logo in its place.

3. Secure the VT180 logo with the two retaining rings found in the small parts box.

3.4.10 Install the Top Cover

Place the top cover on the chassis and fasten it to the bottom cover with four pop fasteners. Press up on the fasteners until they click (Figure 3-10).

3.4.11 Install the New Metal Module Access Cover (Rear Shield)

Install the new metal module access cover over the module access opening, aligning its holes with the connectors on the modules. Install this cover as follows.

1. Place one 1⅛ inch hex standoff (90-00001-12) in each of the four corners of the cover, grounding the cover to the chassis. (See Figure 3-20.)

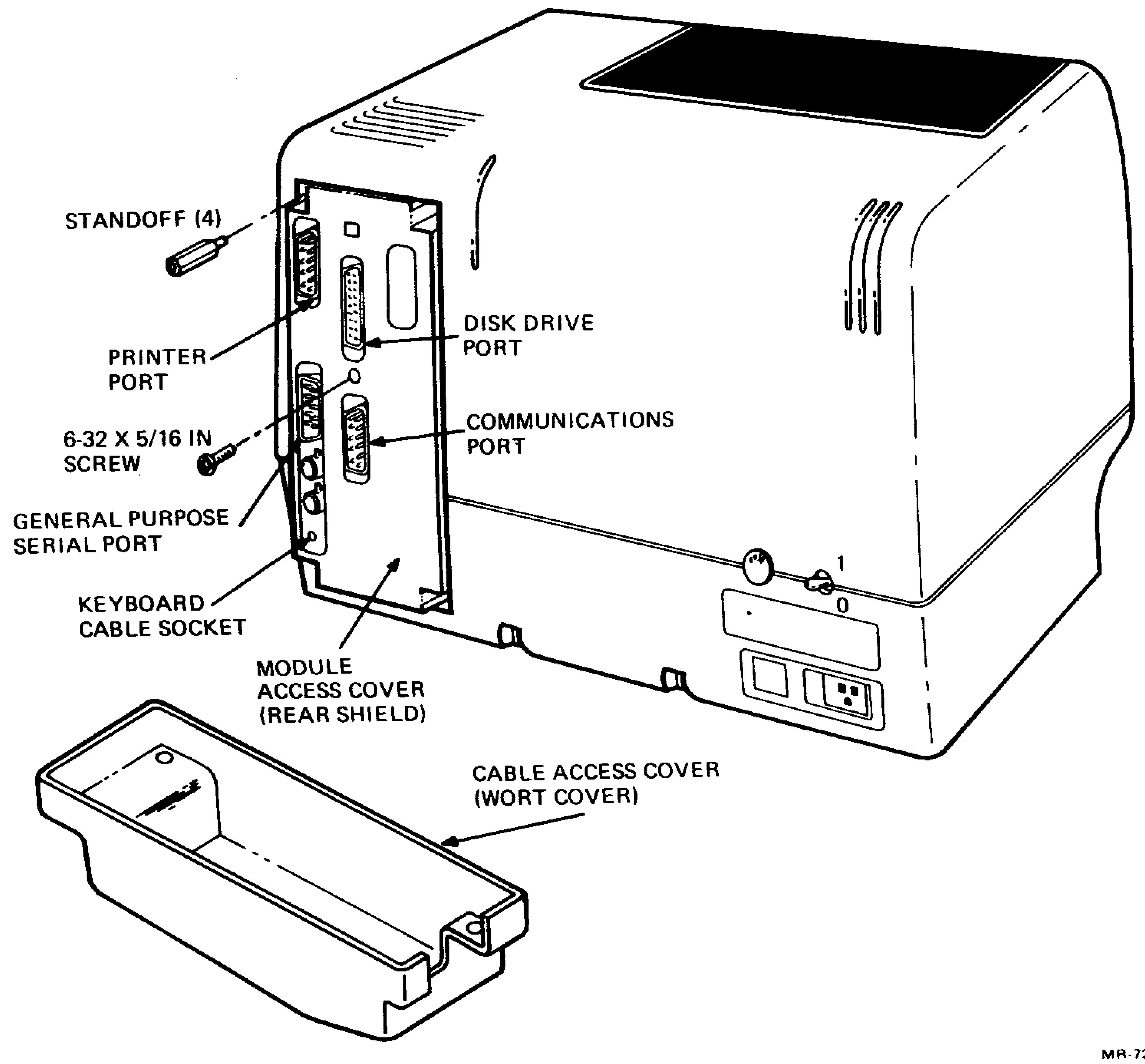


Figure 3-20 Installing the Module Access Cover (Rear Shield)

2. Place one 6-32 by 5/16 inch screw in the center of the cover, grounding the VT18X control module to the cover.

3. Do not install the cable access cover (wort cover) at this time. It will be installed after the cables are connected to the terminal.

3.4.12 Checking the RX180 Drive Select Switches

The RX180 disk drive unit contains drive select switches that are used to configure the drives as A and B or C and D. The VT18X upgrade kit includes the RX180-AB dual disk drive unit configured as drives A and B. If the system includes a second dual disk drive unit, it will be configured as drives C and D. The dual disk drive unit also contains an IC socket on each drive, which is used to terminate the I/O bus with a terminator resistor pack. The terminator resistor pack is always installed in the socket on drive A. The drive select switches and terminator resistor must be checked before the disk drive unit(s) are cabled into the system.

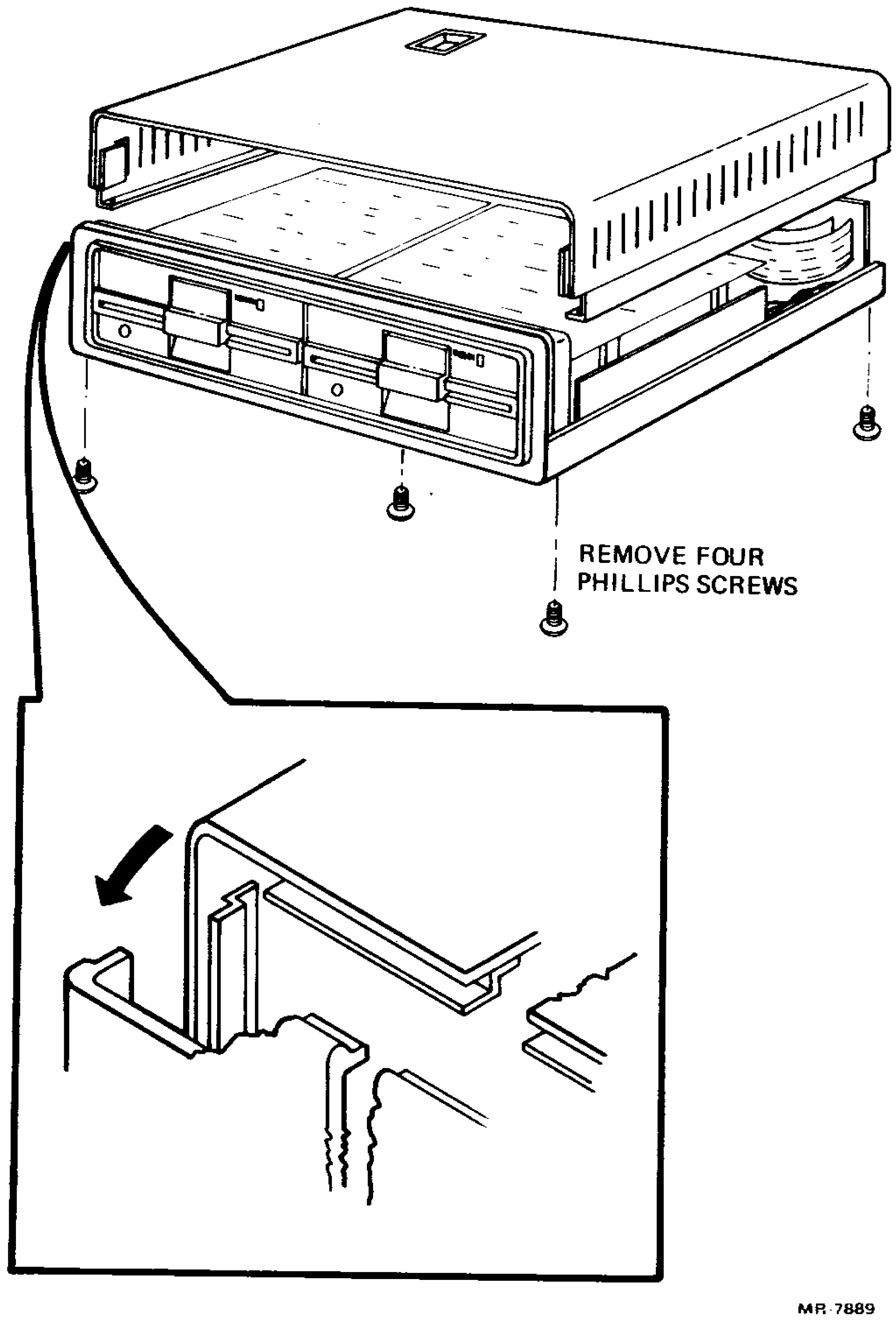


Figure 3-21 Disk Unit Top Cover Removal

3.4.12.1 Disk Drive Unit Top Cover Removal – Perform the following steps to remove the disk drive unit top cover (Figure 3-21).

1. Turn the disk drive unit on its side.

2. Remove the four Phillips head screws and washers from the four corners of the bottom of the disk drive unit.

3. Using both hands, tip the unit back on its base, facing you.

4. Facing the front of the unit, grasp the rear corners of the top cover and guide the rear of the top cover up so as to clear the ON/OFF switch opening. Slide the cover backwards and store it in a safe place.

3.4.12.2 Setting the Drive Select Switches – Find the switch pack on the disk drive unit. Two switches are set on the switch pack for each disk drive, as shown in Figure 3-22.

1/16/84
AB units are Shugart model # 400L
CD units are TEAC FD-50A-03-U
have 6 dip switches positions 1-6
Appear to require switch 5 on in addition to those shown

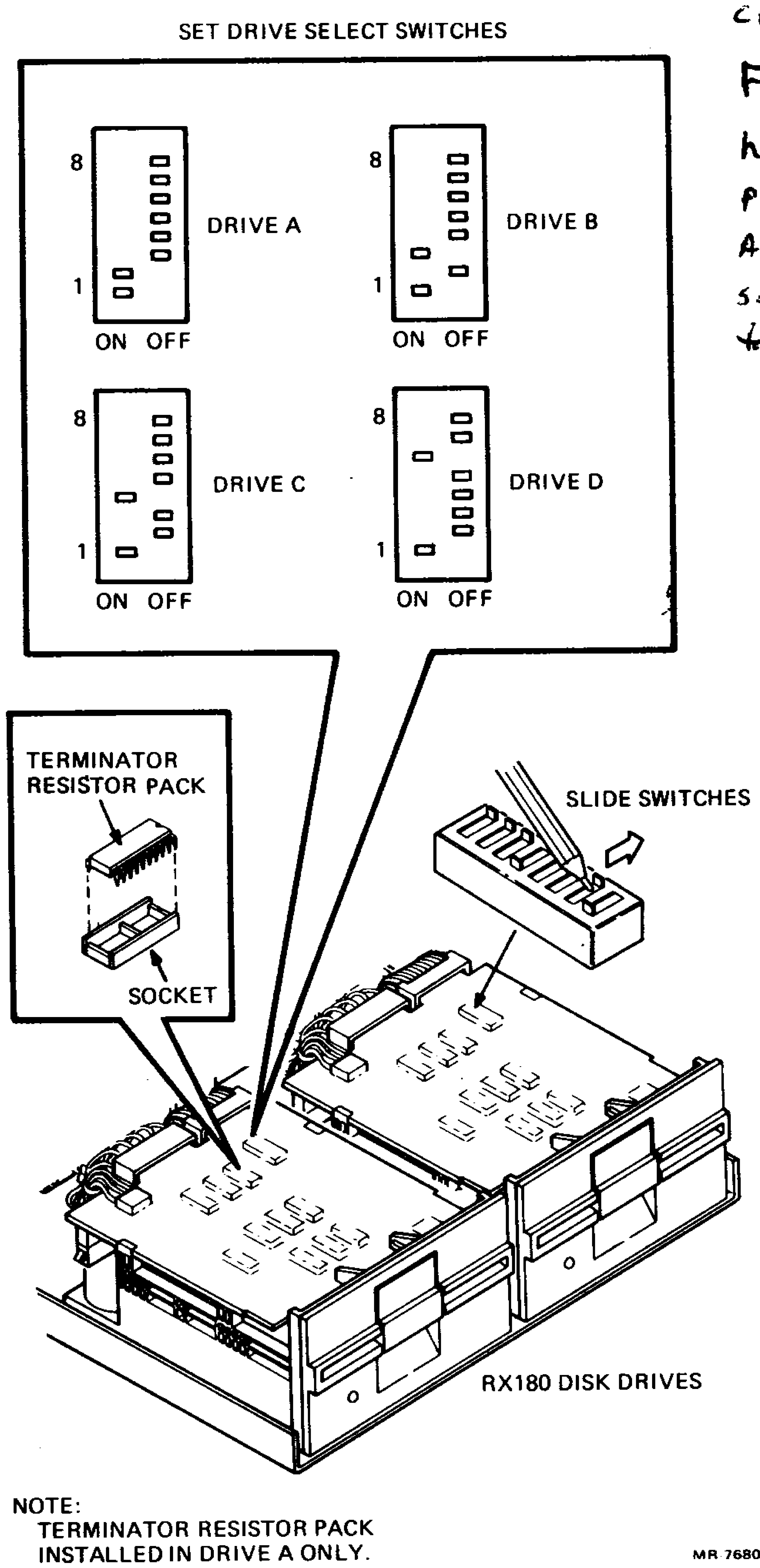


Figure 3-22 Setting the Drive Select Switches

3.4.12.3 Terminator Resistor Pack – Check the IC socket (Figure 3-22) on drive A to make certain a terminator resistor pack is installed. This resistor pack terminates the I/O bus. The IC socket on drives B, C, and D should not have a terminator resistor pack installed.

3.4.12.4 Disk Drive Unit Top Cover (Reinstallment) – Perform the following steps to reinstall the disk drive unit top cover.

1. Set the top cover on the base so the cover clears the front of the two disk drives.
2. Place the disk drive unit assembly on its back panel and slide the lower front edge of the top cover under the disk drives.
3. Turn the unit upside down and align the four holes in the top cover with the four holes in the base. Secure the top cover to the base with four Phillips head screws and star washers.
4. Make sure all screws in the base of the unit are tight.
5. Place the unit on its base and make sure the plastic insert for the 1/0 switch is correctly in place.

3.4.13 ROM Removal and Installation

If you need to replace one ROM to update your terminal or if you need to replace all four ROMs on the terminal controller module (when removing a printer port option), use the following procedure.

1. Find the ROM part numbers on the terminal controller module (Figure 3-6).
2. If a printer port option is removed, remove the ROMs on the terminal controller module and replace them with the ROMs you saved when you installed the printer port option.

ROM Socket	Remove ROMs	Install ROMs
ROM 0	23-095E2	23-061E2
ROM 1	23-096E2	23-032E2
ROM 2	23-139E2	23-033E2
ROM 3	23-140E2	23-034E2

   If necessary, new ROMs can be ordered using the above part numbers. Contact your local Digital Sales office.

3. Unpack the ROM from its container, but do not remove the ROM from the conductive foam. Press the foam against the surface of the terminal controller module to remove static charges. Then remove the ROM from the conductive foam.
4. Referring to Figure 3-23, align the ROM so the notch on the end of the ROM is on the same side as the notch on the IC socket. Check that all ROM pins are equally spaced and straight before inserting the ROM into the IC socket.
5. Using even pressure, press the top of the ROM until it is completely in the socket. If you notice friction, remove the ROM and check for correct pin alignment.
6. After the ROM is inserted, check to see that all ROM pins are correctly installed in the socket.

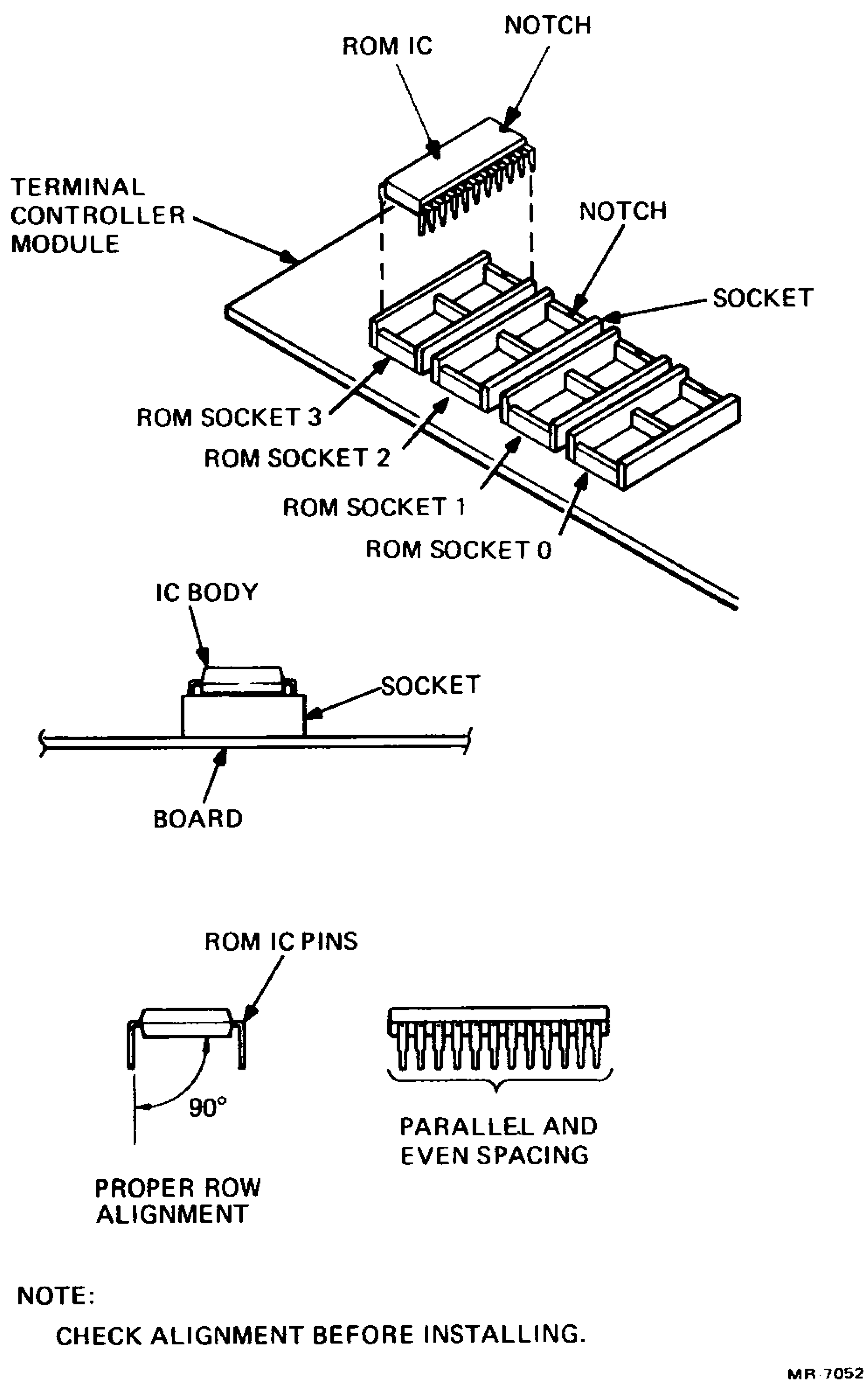


Figure 3-23 ROM Installation

3.4.14 Word Processing Option

A VT100 word processing terminal (VT100-WA or -WB) can be upgraded to a VT180. A word processing terminal has one ROM installed in the ROM A position on the advanced video option (AVO). (See Figure 3-7 or 3-8.) The ROM part number and the jumpers installed (or the switches set) on the AVO are as follows.

ROM A Part Number	**Jumpers Installed**	**Switches Set**
23-069E2	1 and 7 (See Figure 3-7)	2 and 8 on switch pack 2 (See Figure 3-8)

3.5 SYSTEM INTERCONNECTIONS

Place the terminal, keyboard, and disk drive unit(s) on a desk or table top in the desired positions (Figure 3-2). The only tools necessary for installing the VT180 is a 3 mm (1/8 inch) blade screwdriver and a number 1 Phillips screwdriver. More tools may be necessary when installing accessories or options.

3.5.1 Terminal Installation

Perform the following steps to install the terminal.

1. Make sure the unit is not connected to the power source.
2. Attach the BC26K terminal-to-disk I/O cable (17-00297) to the disk port on the module access cover (Figure 3-24). Seat and secure the connection by gently tightening the hold-down screws using a 3 mm (1/8 inch) screwdriver.

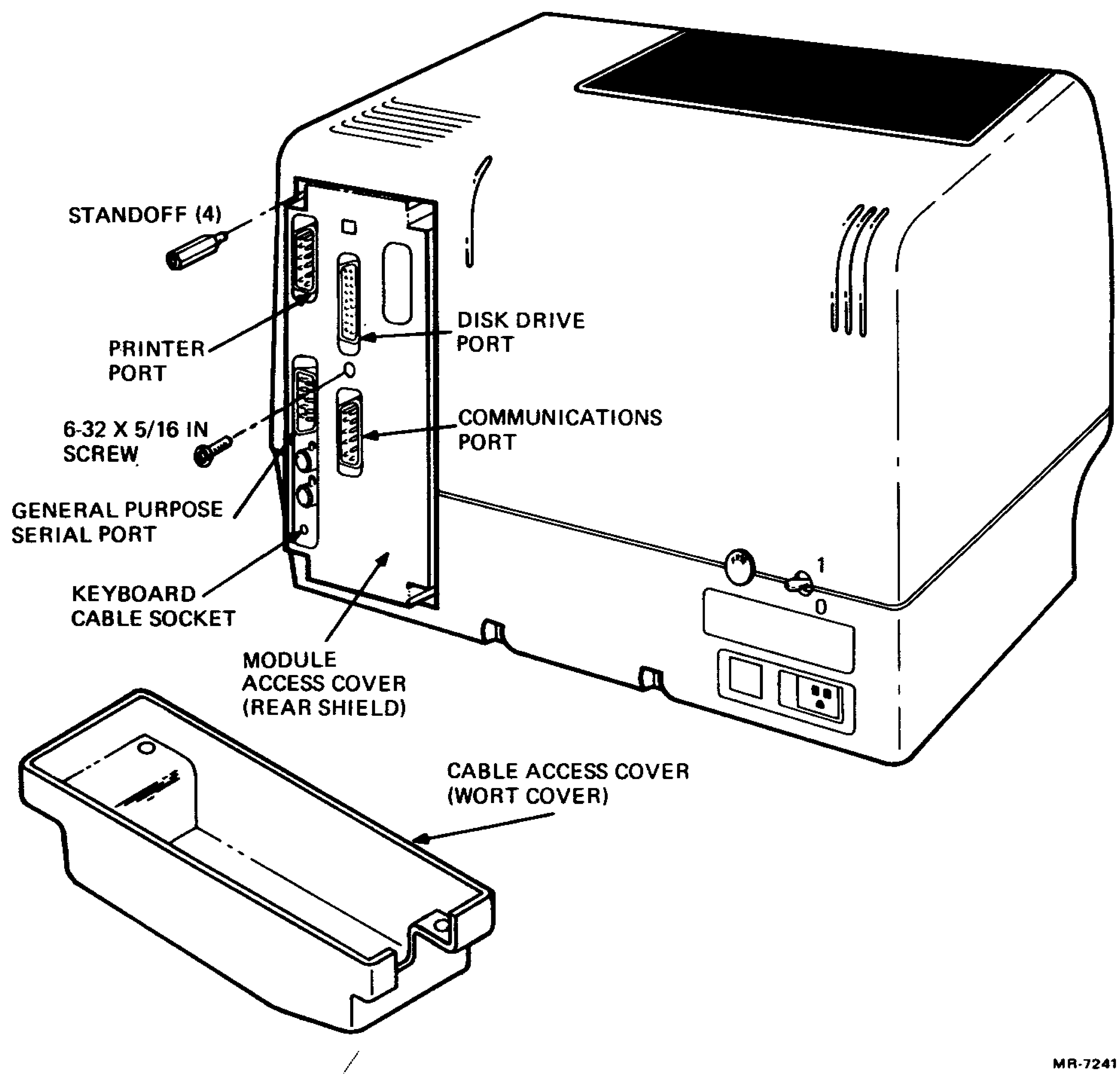


Figure 3-24 Terminal Cable Connectors

3. Plug the keyboard cable into the keyboard cable socket on the terminal controller module.

4. Check the terminal for the correct voltage range selection. The terminal can operate with either 115 Vac or 220–240 Vac input power.

CAUTION
Failure to select the correct voltage range will damage the terminal.

A label over the power receptacle indicates the factory selected input voltage range. Check this label, the voltage selector switch, and the fuse in order to be sure that the voltage range of the terminal is the same as your local ac power source.

Remove the fuse holder cap by pressing it in and turning it counterclockwise. Check the fuse for a rating of 3 A (PN 90-07217). Replace the fuse by pressing it in and turning it clockwise.

5. Turn the power ON/OFF switch to the off (0) position.

3.5.2 Install the RX180 Disk Drive Unit(s)

Use the following procedure to install one or two dual disk drive units.

CAUTION
If you have two disk drive units, they are not interchangeable unless the drive select switches are reset and the resistor terminator pack is installed as explained in Paragraph 3.4.12.3. RX180-AB is factory configured as drives A and B; RX180-AD is factory configured as drives C and D.

1. Check the voltage selector switch on the back of each disk drive unit. The voltage selector switch must be set to match the local ac power source. Make certain that the installed fuse is rated at 3 A (PN 90-07217). The voltage selector switch and fuse locations are shown in Figure 3-25.

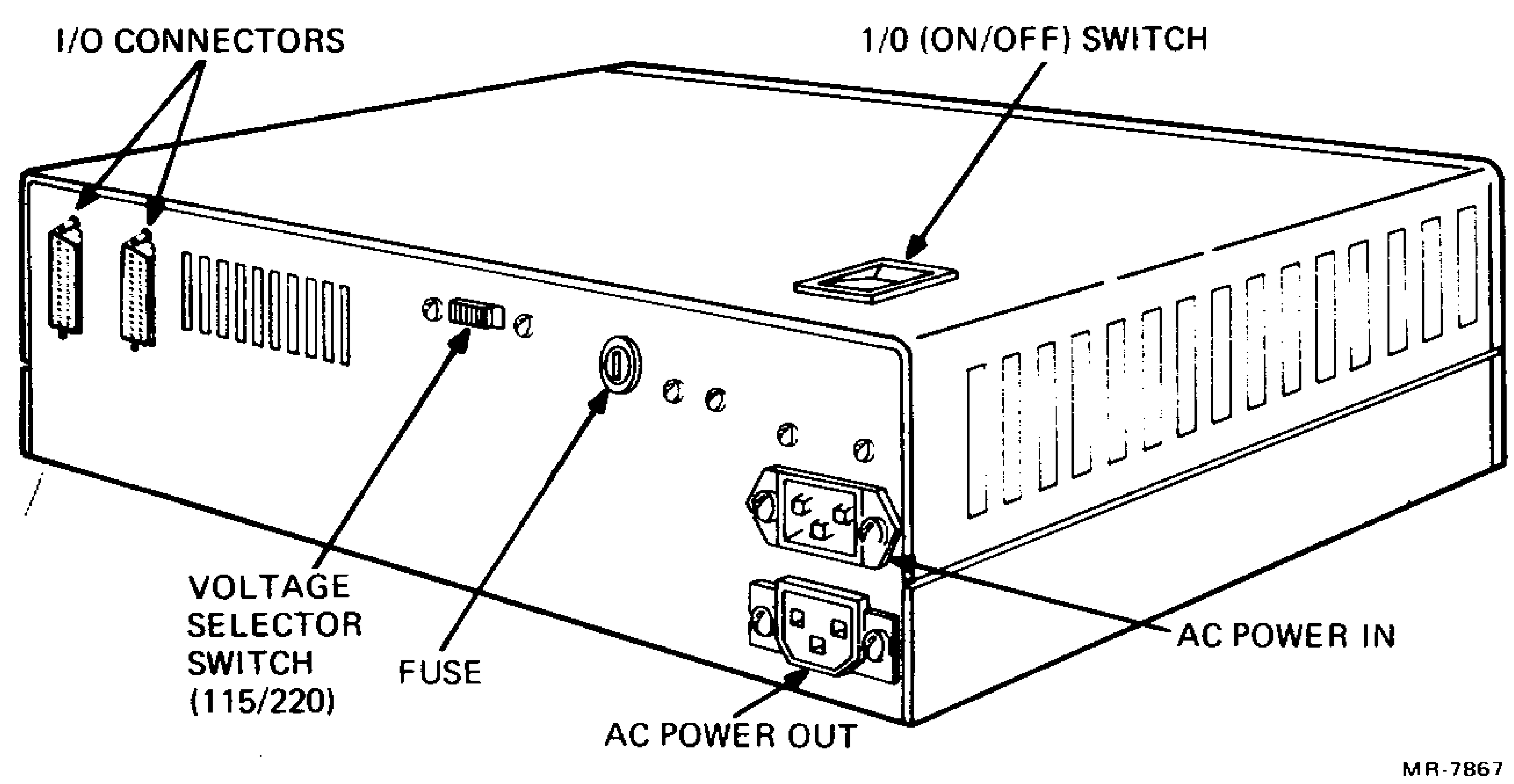


Figure 3-25 RX180 Dual Disk Drive Unit (Rear View)

CAUTION
If you connect 220 V to a disk drive unit that is set for 115 V, you will blow its fuse and may damage its power supply.

2. If you have one disk drive unit, place it on the top or on either side of the video terminal. (See Figure 3-2.)

NOTE
If placing the disk drive unit on top of the video terminal, do not cover the ventilation openings on top of the terminal.

3. If you have two disk drive units, place RX180-AB (drives A and B) on top of RX180-AD (drives C and D). Set the power ON/OFF switch on RX180-AD (drives C and D) to the on (1) position.

4. Attach the BC26K cable from the terminal's disk port to the left conductor (as viewed from the back) of the bottom (or only) disk drive unit. See Figures 3-26 and 3-27.

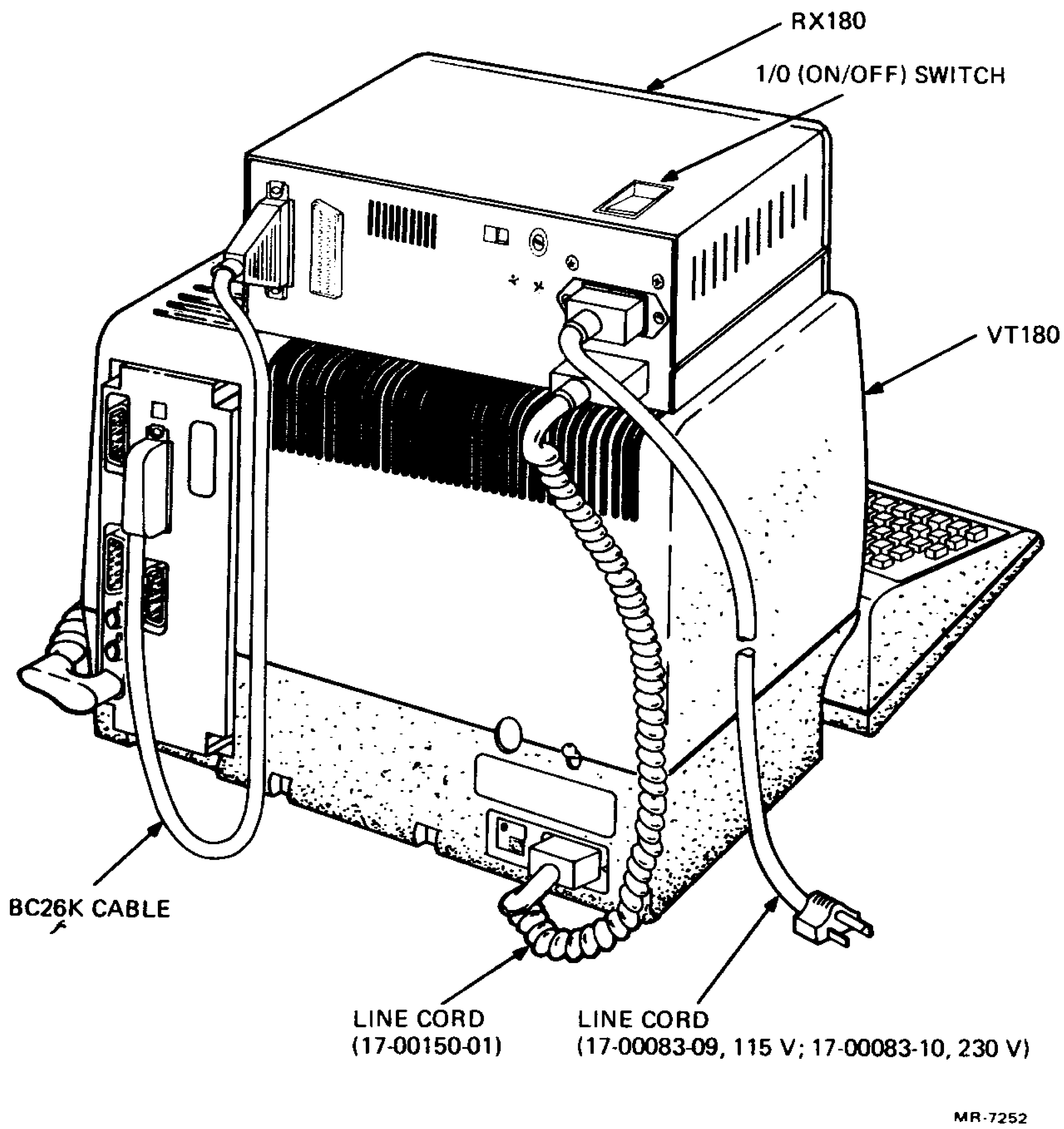


Figure 3-26 VT180 Cable Connections with One Disk Drive Unit

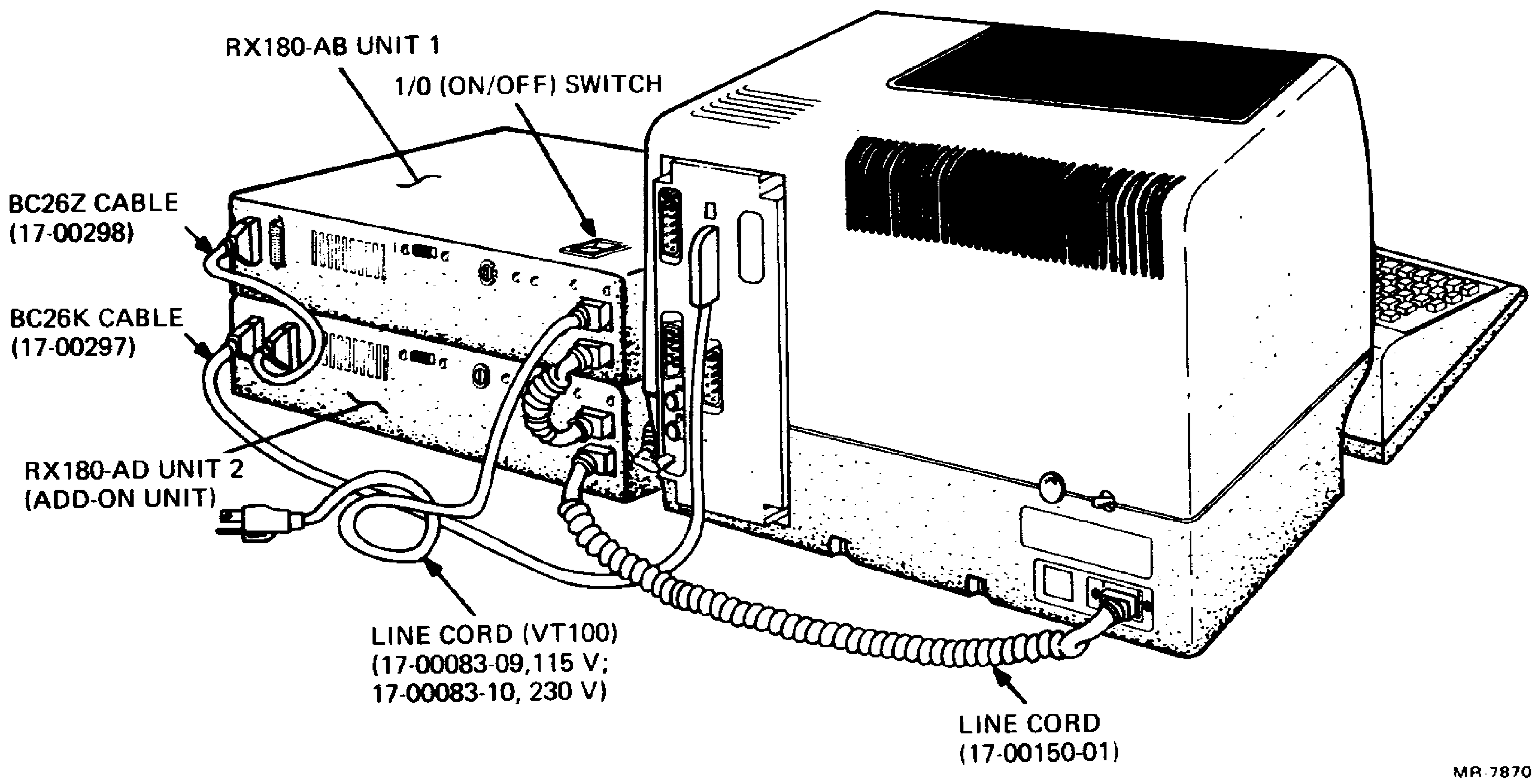


Figure 3-27 VT180 Cable Connections with Two Disk Drive Units

5. If you have two disk drive units, attach the BC26Z 20 cm (8 inch) disk-to-disk I/O cable (17-00298) from the right connector on the bottom disk drive unit (drives C and D) to the left connector on the top disk drive unit (drives A and B).

6. Find the ac line cord previously removed from the video terminal and attach this ac line cord to the ac input of the top or only disk drive unit. (See Figure 3-26.) Do not plug the other end of this cable into an ac wall receptacle at this time.

7. If you have two disk drive units, plug the end of a coiled line cord with prongs in the ac output of the top disk drive unit and the other end without prongs in the ac input of the bottom disk drive unit (Figure 3-27).

8. Plug the end of a coiled line cord with prongs into the ac output of the bottom (or only) disk drive unit; plug the other end with prongs in the ac input of the video terminal.

When the VT180 has been correctly cabled, it should look like either Figure 3-26 or 3-27.

3.5.3 Serial Port Connections

Connections to the printer, communications, and general purpose ports (Figure 3-22) will depend on the specific system configuration. These ports permit the VT180 to communicate with a remote host computer and a large variety of external devices.

3.5.3.1 Printer Port – If a printer such as Digital's LA120 or LA34 is used with the VT180, attach a null modem cable (BC26U or the equivalent) to the 25-pin printer connector. This cable terminates at both ends with an RS-232 female connector. Attach the other end of the cable to the printer I/O connector. Make sure the connectors are completely seated and secure the connections on both ends of the cable by gently tightening the captive screws on the top and bottom of the connectors (Figure 3-28).

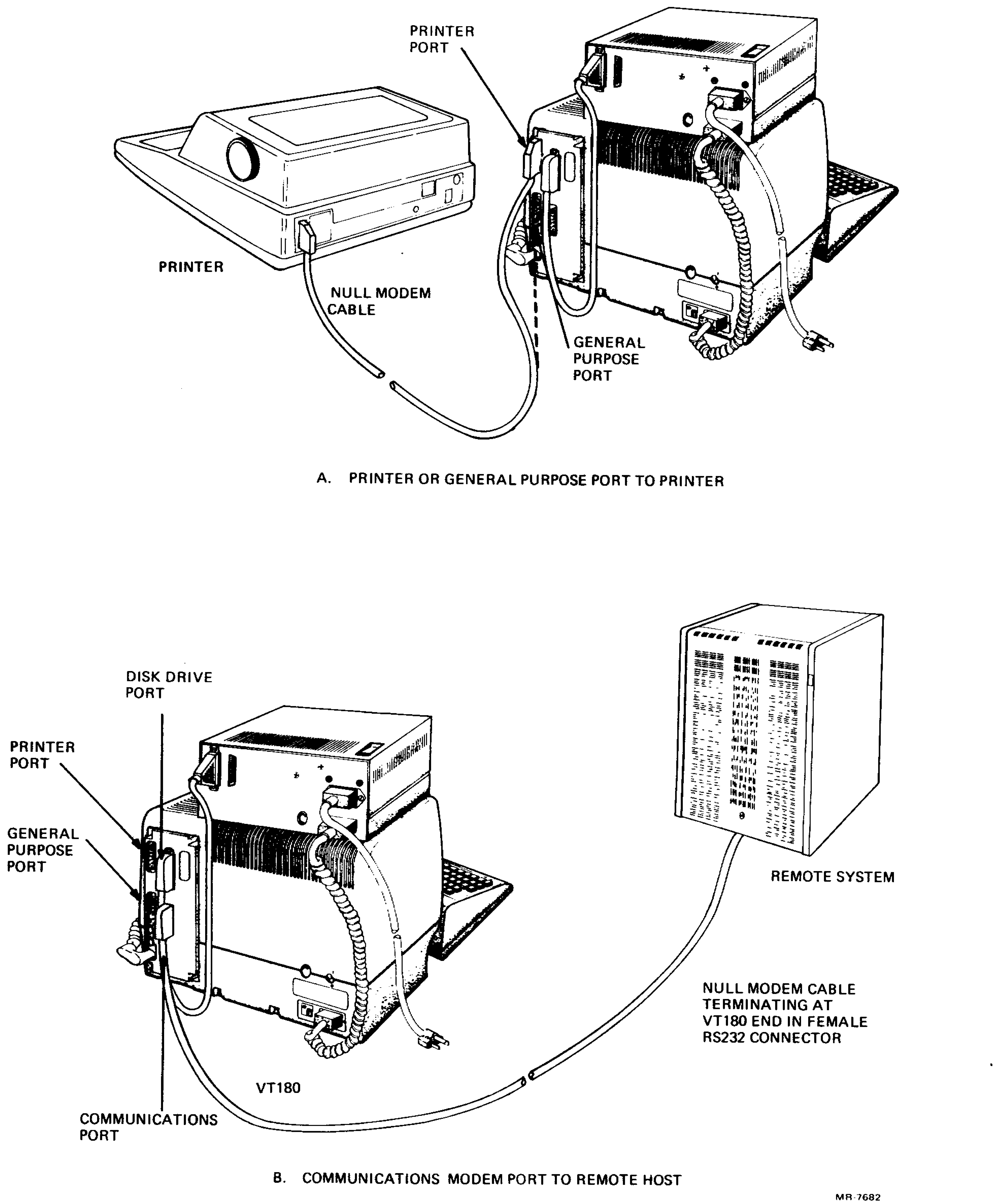


Figure 3-28 Connecting Devices to the Serial Ports

3.5.3.2 Communications Port – This port is used to communicate with an external host computer when the VT180 is operated in terminal mode. Connect the RS-232 female connector end of a null modem cable (BC26R, BC22B, or the equivalent for asynchronous modems or BC22C for synchronous modems) to the communications port connector. Make sure the connector is fully seated and secure the connection by gently tightening the hold-down screws on the connector. Connect the other end of the cable to the host computer and secure the connection (Figure 3-28).

3.5.3.3 General Purpose Port – CP/M allows this serial port, like the printer port, to be assigned as the console device. With such an assignment, a keyboard printer like the LA34 could be used as a hard copy console and the normal printer port could be used to communicate with a LQP02 letter quality printer. If the LA34 printer is to be used as a hard copy console, connect the null modem cable (BC26U or the equivalent) to the general purpose port connector. Make sure the connector is completely seated and secure the connection by gently tightening the hold-down screws on the connector (Figure 3-28).

Using four Phillips head screws, install the cable access cover (Figure 3-24) to the rear of the VT180 terminal after all cable connections are secured. All cables must be aligned with the opening at the bottom of the cable access cover.

3.6 POWER-UP PROCEDURE

A power-up self-test verifies correct operation of the VT180 each time it is powered up or reset by a reset command (pressing the 0 key while in SET-UP A). The self-test program does the following.

1. It waits until the VT100 terminal successfully executes its own self-test. (This means that if the VT100 detects faults in its own operation, VT100 error characters may appear on the screen, but nothing further will happen.)

2. When the system self-test program receives acknowledgment of a successful VT100 self-test, it executes a fast test of all major system components. This test confirms:

   a. That the VT180 computer can communicate with the terminal (the T+ characters appearing at the beginning of the start-up dialog are a part of this test)

   b. That the computer can correctly execute machine language instructions

   c. That data can be written to and accurately retrieved from memory

   d. That the computer can identify and transmit control information to the serial ports

   e. That the computer can identify and transmit control information to the disk drives.

The ROM-based self-test program runs in two modes: a short mode when the system is powered up (or reset) and a long mode when the self-test option S is selected after the start-up message appears on the screen. The long mode S tests more VT180 features and takes more time than the short mode.

Perform the following procedure to power up the terminal and run the power-up self-tests.

CAUTION
Do not leave diskettes in the RX180 during power-up or power-down.

1. First, make sure the power is off by setting the 1/0 switch on the top disk drive unit to 0 (off). See Figure 3-25.

2. Plug the ac line cord from the back of the top disk drive unit into a wall receptacle.

3. Set the 1/0 switch on the back of the video terminal to 1.

4. Set the 1/0 switch on the bottom disk drive unit (if installed) to 1.

NOTE

If two disk drive units are installed, the 1/0 switch on the bottom disk drive unit should stay at 1 (on). Power for the entire system is turned on and off by the 1/0 switch on the top disk drive unit.

5. Set the 1/0 switch on the top disk drive unit to 1 (on). The 1/0 switch for each disk drive unit should light up. The system takes approximately 15 seconds to warm up, complete its self-tests. and display the start-up messages. The following indicators will be noted during power-up.

   a. The self-test start beep sounds.
   b. The keyboard ON-LINE LED is turned on.
   c. The red LED on the left front of the disk drive unit is turned on and then off.
   d. The red LED on the right front of the disk drive unit is turned on and then off.
   e. The red LED on the left front of the disk drive unit is turned on.
   f. The self-test complete beep sounds.
   g. The start-up message appears on the screen as follows.

```
T+
  VT18X Version 2.1 28-JUN-82
Copyright 1982 Digital Equipment Corp
Press A, B, C, D, S, or T

A = Start System (drive A)
B = Start System (drive B)
C = Start System (drive C)
D = Start System (drive D)
S = Execute Self-test
T = Enter Terminal Mode
```

NOTE

If an illegal character is typed, a question mark (?) is printed and the message is repeated.

3.6.1 Self-Test Error Messages

If the power-up self-test program encounters an incorrect system condition as it executes, the program stops automatically and the screen displays an error message. In general, error messages issued at system start-up come either from the VT100 terminal or the VT180 read-only memory. Error messages coming from the VT100 consist of one-character displays appearing at the upper left corner of an otherwise blank screen. These messages may include the numerals 0 through 9, the alphabetic characters A through O, and the symbols :, ;, <, =, ?, and @. An error condition may also be indicated by an error code on the keyboard L1–L4 LEDs.

Error reporting as a result of a fault in the VT18X control module or disk drive units appears in two forms: a message in English that points to the defective circuit appears on the screen and the LEDs on the VT18X control module display the error in hex code. If an error is indicated on power-up, refer to Chapter 7 for more information about self-test errors, error codes, and their meaning.

If the VT180 powers up correctly, select the desired set-up features as described in Chapter 2 and proceed with the system checkout.

3.7 SYSTEM CHECKOUT

System checkout is performed after the power-up self-tests are successfully completed and the set-up features have been selected. System checkout consists of running the ROM-based self-tests in long mode S while formatted diskettes are installed in the disk drives and then running the diskette-based diagnostics for a more complete system checkout.

The VT180 diagnostic tests to be run during system checkout are of two types.

1. A ROM-based diagnostic that is run automatically on power-up or, optionally, on reset (pressing 0 while in SET-UP A).

2. A VT18X diskette-based diagnostic that you run by starting the diskette in either disk drive. The procedure for formatting diskettes is described in Paragraph 4.5.

3.7.1 ROM-Based Diagnostic

The ROM-based diagnostic runs automatically on power-up and checks the internal logic of the VT180 modules. This diagnostic assumes that no diskette is loaded. If the ROM-based diagnostic runs successfully, the Main System menu prints on the video terminal as shown in Paragraph 3.6.

If an error occurs and the video terminal is working, the error will be reported by an error message on the video terminal that points to the location of the failure. Refer to Chapter 7 for additional information.

3.7.2 VT18X Diskette Diagnostic

The VT18X diskette diagnostic resides on one diskette (BJ-T040B-MV). The diagnostic is loaded from this diskette; then it requires two formatted diskettes to perform the read/write tests on each disk drive. During testing, the contents of the formatted diskettes are destroyed.

You select the diagnostic to run in one of three modes.

1. Initial test – This is the disk drive test that checks out each disk drive. The test takes 5½ minutes for a dual disk drive system and 11 minutes for a four disk drive system.

2. Extended test – This selection runs the disk drive test above, a RAM test, and the basic communications test. This extended test takes 10 minutes for each dual disk drive unit.

3. Individual test – This selection allows you to run the previous tests one at a time on the drive you select. In addition, there are tests to check the communications ports, a printer (if installed), and a synchronous communications test. Run time for these tests depends on the tests you select.

The starting procedure, tests performed, and the error messages for this diagnostic are found in Chapter 7.

3.7.3 Hardware Installation Complete

When the initial test and the extended test of the VT18X diskette diagnostic run successfully one time, the VT18X hardware installation is complete. If you have a printer on your system, the printer confidence test should also run successfully.

Refer to the *VT180 User's Guide* to copy diskettes and to run the CP/M software.

3.8 INTERFACE INFORMATION

The VT180 operates on full-duplex, asynchronous communication lines to communicate with the external host computer and a variety of external devices via three EIA RS232C serial line connectors. The interface to the disk drives is provided by a 37-pin, D-type connector. Two female BNC connectors are used to interface to external video devices. The following paragraphs describe the signals on these interface connectors.

3.8.1 Communications Interface Connector

This port is used to communicate to another computer. It has full modem support and supports the same signals as the VT131. United States and European full- and half-duplex modems can be supported by this port. The port has ASYNC as well as BISYNC modes with a RS232C (V.24/V.28) physical interface conforming to CCITT V.21, V.22, and V.23. Break detection by this port is supported.

The transmit and receive baud rates for this port are derived from the baud rate clocks on the terminal controller module. Therefore, the transmit and receive baud rates selected in the VT180's set-up mode are the transmit and receive baud rates used for this port. Baud rates supported are 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 9600, and 19,200.

Any and all protocols to be supported by this port, other than pass-through mode, are run as applications under CP/M.

The recommended cable for this port under asynchronous communications is a BC26R-XX. Other cables that will work are BC22B-10 and BC22B-15. A BC22C-10 must be used for bisynchronous operation. This 25-pin, D-type EIA connector resides on the VT18X control module and is covered by the wort cover. Table 3-3 lists the signals for the communications interface connector.

3.8.2 Printer Interface Connector

This is a general purpose printer port that provides an RS232C serial interface compatible with Digital printers. EIA signals supported are transmit data, receive data, and data terminal ready. Software programmable baud rates to be supported are 75, 150, 300, 600, 1200, 2400, 4800, and 9600. Software programmable character formats supported are 5, 6, 7, and 8 bits/character with 1, 1½, and 2 stop bits/character. Software should support XON/XOFF restraint protocol for this port. The 25-pin, D-type EIA printer connector physically resides on the VT180 paddle board. The recommended cable for this port is a BC26U-15. A BC22A will also work but is a second choice. Table 3-4 lists the signals for the printer interface connector.

Table 3-3 Communications Interface Connector

Pin Number	Signal Description	Mnemonic
1	Protective ground	PROT GND
2	Transmitted data	TXD
3	Received data	RXD
4	Request to send	RTS
5	Clear to send	CTS
6	Data set ready	DSR
7	Signal ground	SGND
8	Receive line signal detector (carrier detect)	RLSD
9	Not used	N/U
10	Not used	N/U
11	Not used	N/U
12	Speed indicator/secondary receive line signal detector	SI/SRLSD
13	Secondary clear to send	SCTS
14	Secondary transmit data	STXD
15	Transmitter clock	TSET
16	Not used	N/U
17	Receive clock	RSET
18	Not used	N/U
19	Secondary request to send	SRTS
20	Data terminal ready	DTR
21	Not used	N/U
22	Ring indicator	RI
23	Speed select	SPDS
24	Not used	N/U
25	Not used	N/U

Table 3-4 Printer Interface Connector

Pin Number	Signal Description	Mnemonic
1	Protective ground	PROT GND
2	Transmitted data	TXD
3	Received data	RXD
6	Data set ready	DSR
7	Signal ground	GND
20	Data terminal ready	DTR

3.8.3 General Purpose Serial Interface Connector

This port is provided as a general purpose RS232C interface. Signals supported are transmit data, receive data, and data terminal ready. Software programmable baud rates to be supported are 75, 150, 300, 600, 1200, 2400, 4800, and 9600. Software programmable character formats supported are 5, 6, 7, and 8 bits/character with 1, 1½, and 2 stop bits/character. Signals are passed through a ribbon cable to the VT180 paddle board from the VT18X control module. The recommended cable to be used on this port is a BC26S-XX. Another cable that would suffice would be a BC22A-10 or -25. Table 3-5 lists the signals for the general purpose serial interface connector.

Table 3-5 General Purpose Serial Interface Connector

Pin Number	Signal Description	Mnemonic
1	Protective ground	PROT GND
2	Transmitted data	TXD
3	Received data	RXD
4	Request to send	RTS
6	Data set ready	DSR
7	Signal ground	GND
20	Data terminal ready	DTR

3.8.4 RX180 Disk Port Connector

This is an interface designed to control up to four 4¼ inch disk drives. The controller supports double-density drives using MFM recording. Only soft-sectored, single-sided diskettes are supported. The interface adheres to drive capability and signal definition of the ANSI standard interface for disk drives. The connector to the drives is a 37-pin, D-type connector, which physically resides on the VT18X control module and is covered by the cable access cover. Table 3-6 lists the signals for the RX180 disk port connector.

3.8.5 External Video Connections

In addition to the EIA interface, the VT180 can easily interface to external video devices. These video devices may act either as a slave to the VT180 when connected to the composite video output or provide synchronized video to the VT180 video section when connected to the video input. The external video connectors are the two female BNC connectors found on the back of the terminal just below the general purpose serial interface connector. The upper BNC connector (J8) is the video input while the lower BNC connector (J9) is the video output.

Table 3-6 RX180 Disk Port Interface Connector

Pin Number	Signal Description	Mnemonic
1	Ground	GND
2	Not used	N/U
3	Ground	GND
4	Not used	N/U
5	Ground	GND
6	Select 3	SEL3 L
7	Ground	GND
8	Index	INDEX L
9	Ground	GND
10	Select 0	SEL0 L
11	Ground	GND
12	Select 1	SEL1 L
13	Ground	GND
14	Select 2	SEL2 L
15	Ground	GND
16	Motor on	MOTOR ON L
17	Ground	GND
18	Direction	DIR L
19	Ground	GND
20	Step	STEP L
21	Ground	GND
22	Write data	WRT DATA L
23	Ground	GND
24	Write gate	WG L
25	Ground	GND
26	Track 00	TK00 L
27	Ground	GND
28	Write protect	WRT PRT L
29	Ground	GND
30	Read data	RD DATA L
31	Ground	GND
32	Reserved	N/U
33	Ground	GND
34	Drive ready (opt)	READY L

3.8.5.1 Composite Video Output Connector (J9) – The composite video output provides EIA RS170 output generated by combining the video signal with a composite sync signal. The output contains all video data appearing on the VT180 screen except that video that comes from J8. The output has the following nominal characteristics (Figure 3-29).

1. Output impedance = 75 ohms, dc-coupled.

2. Sync level = 0 V.

3. Black level = approximately 0.3 V when loaded with 75 ohms.

4. White level = approximately 1.0 V with a 75 ohm load.

5. The composite sync waveform conforms to EIA RS170 standards. The vertical interval is composed of six equalizing pulses, six vertical synchronizing pulses, and six more equalizing pulses. The timing is as follows.

Equalizing pulse width	= 2.33 μs ±50 ns
Vertical pulse width	= 27.28 μs ±200 ns
Horizontal pulse width	= 4.771 μs ±50 ns
Horizontal blank width	= 11.84 μs ±50 ns/80-column mode
	= 12.34 μs ±50 ns/132-column mode
Front porch	= 1.54 μs ±50 ns

3.8.5.2 Video Input Connector (J8) – An analog signal applied to the video input is ORed with the internal video signal such that the beam intensity at any point on the screen corresponds to the intensity of that signal, which tends to make the beam brighter at that point. A video signal on this input affects only the internal screen and does not appear on the composite video output. This input has the following nominal characteristics.

1. Input impedance = 75 ohms, dc-coupled.
2. Black level = 0 V.
3. White level = 1.0 V.
4. Maximum continuous input = ±2.0 V.

The external video source must be synchronized to the VT180; it may do this by referencing the composite sync on the composite video output. This means that the VT180 video input will not synchronize with any composite video source including the composite video output of another VT180.

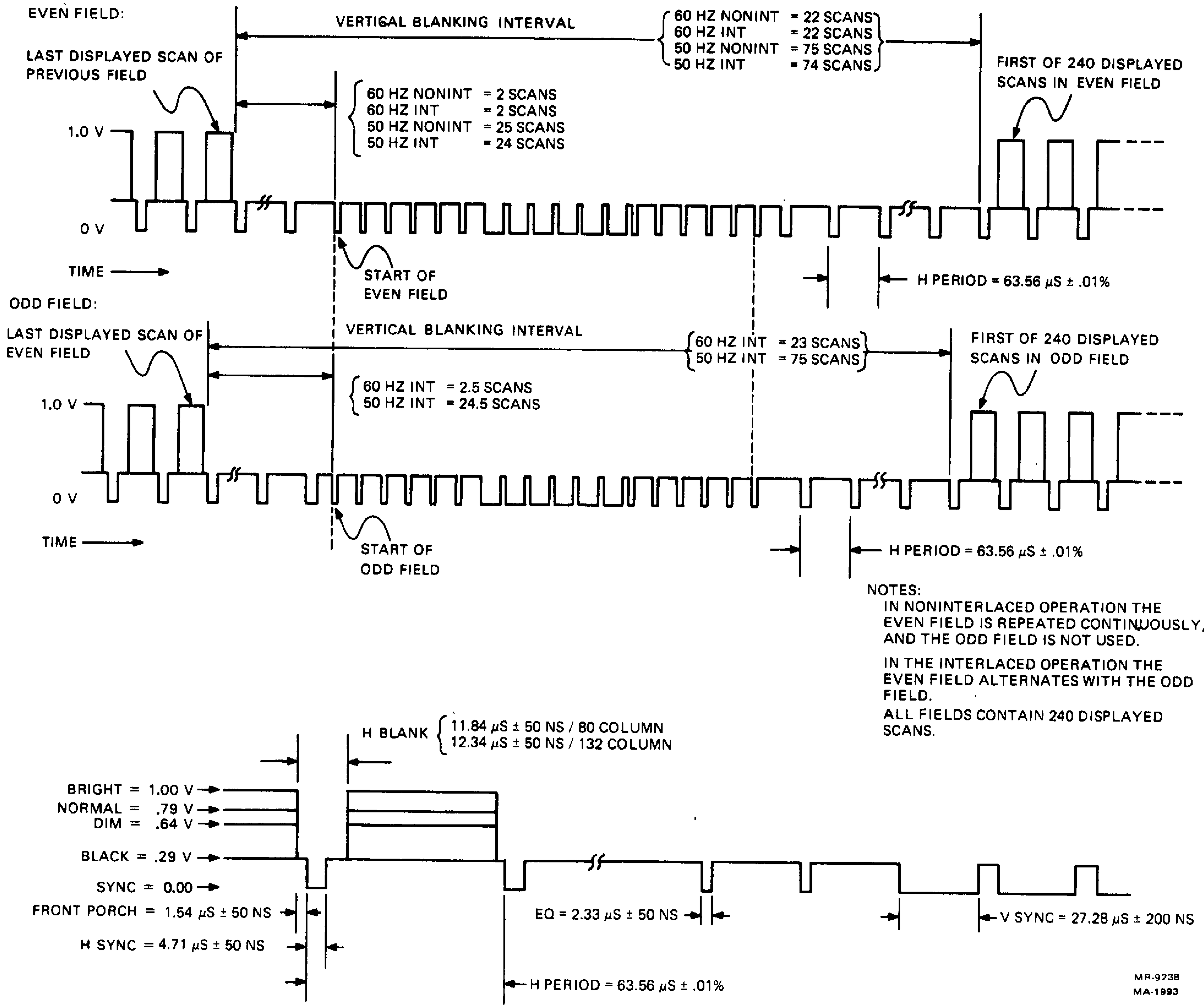


Figure 3-29 Composite Video Output

CHAPTER 4
VT180 CP/M OPERATION

4.1 CP/M INTRODUCTION

CP/M is the operating system that governs all activities taking place in the personal computer. Application programs that run on the VT180 do so under CP/M's control. An application program permits the user to perform a particular task, such as planning a budget or analyzing data. Many programs are available that are compatible with the VT180 and CP/M.

Communication with the VT180 is accomplished by typing commands to CP/M on the keyboard. CP/M accepts commands for a variety of actions including:

1. Listing the names of files on a diskette
2. Copying diskettes
3. Copying individual files
4. Creating text files
5. Displaying text files at the terminal
6. Printing files on a hard copy printing device
7. Deleting files
8. Running programs.

4.2 DISKETTES AND FILES

CP/M deals with a broad spectrum of information including programs, text, and data. Information is organized in the form of files, and the files are stored on diskettes. File names distinguish electronic files in much the same way as labels on file folders distinguish paper files in a cabinet.

4.2.1 Storing Information on Diskettes

The computer stores and retrieves files by referring to tracks and sectors on a diskette (see Figure 4-1). VT180 diskettes have 40 tracks (numbered 0 through 39), each composed of nine sectors. Sectors store blocks of bytes, each byte representing one character such as a letter, a digit, or a symbol. Since each sector has a unique location on the diskette, the computer can find a particular sector on a particular track and store information in it or retrieve information from it.

The amount of information stored on a diskette depends on the diskette's density. Double-density diskettes can hold twice as much information as single-density diskettes. VT180 diskettes are double-density.

4.2.2 Using Diskettes

Because information on a diskette can be corrupted by accident, human error, or temperature and humidity, it is important to copy or back up diskettes. You generate working copies and store the originals, or master diskettes, as insurance against disaster.

The CP/M diskette is called the system diskette because it contains the operating system. Always copy a system diskette when you first receive it. If you have not already done so, copy and label the CP/M system diskette according to the procedure in Paragraph 4.5. Other diskettes containing programs, the data generated by programs, or text, should be copied periodically.

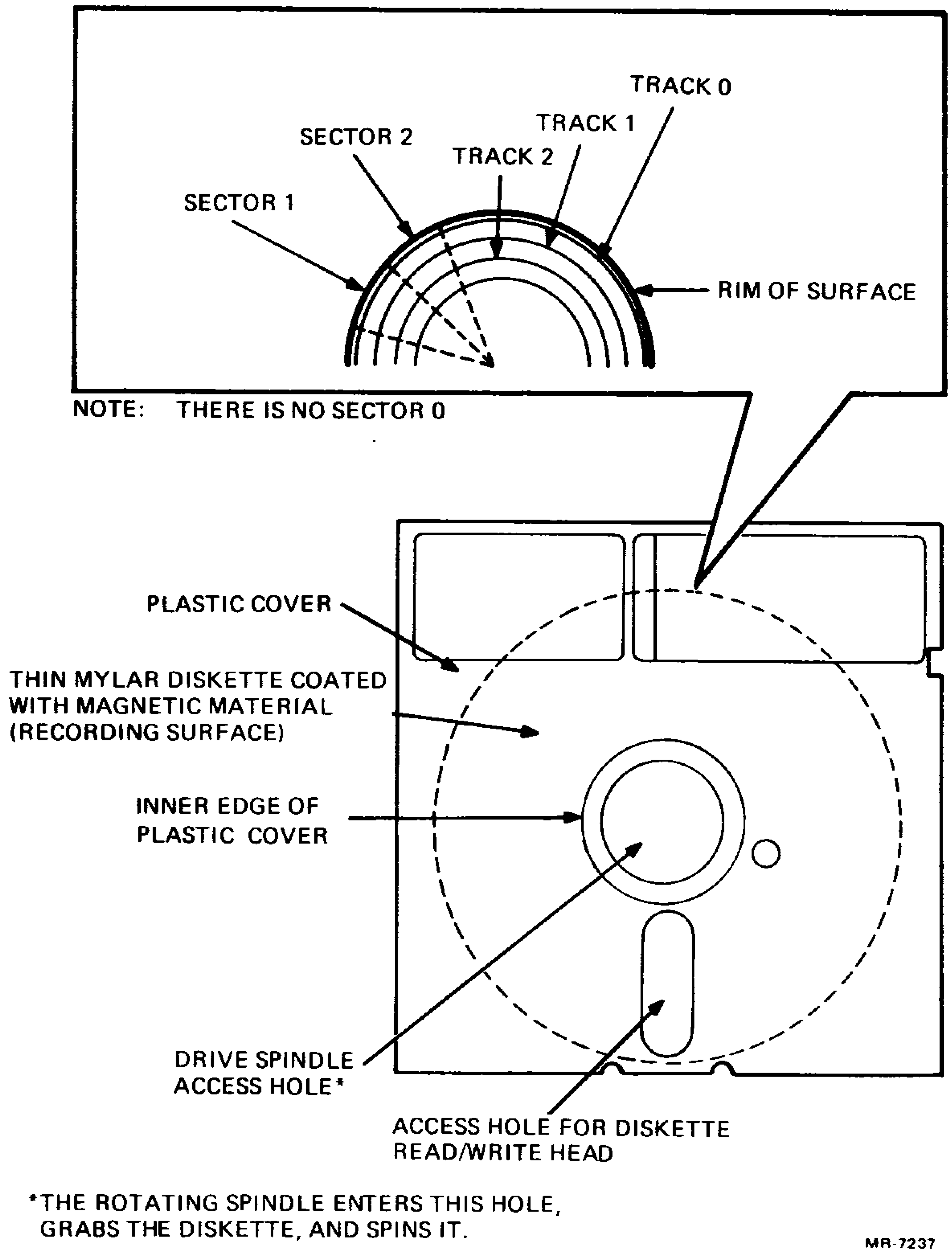


Figure 4-1 Tracks and Sectors on a Diskette

NOTE

Occasionally, it is possible to install a diskette that does not seat itself properly in its drive. This can cause unreliable operation resulting in loss of data or data that is inaccessible. To guard against this possibility, always insert the diskette carefully, pushing it gently back in the drive as far as it can go. Shut the drive door securely. If you encounter any difficulty inserting the diskette or latching the drive door, remove the diskette and try again.

4.3 LOADING CP/M INTO VT180 MEMORY

CP/M may be loaded into the VT180 after the system is powered up and has successfully completed the automatic self-test. Execute the following steps to load the CP/M into the VT180. Press no keyboard keys other than those specified. If an unspecified key is inadvertently pressed, remove any installed diskette(s) and start over.

1. Open disk drive A, remove any diskette that may be there, and replace it in its envelope. Do not insert another diskette at this time.

CAUTION

Handle the diskette only by the edges of its plastic cover. Do *not* touch the diskette surfaces with your fingers (see Figure 4-2). Keep diskettes away from electronic apparatus, electric motors, magnets, and screwdrivers. Do not lay diskettes, even for a short time, on top of the disk drive unit or on top of the terminal.

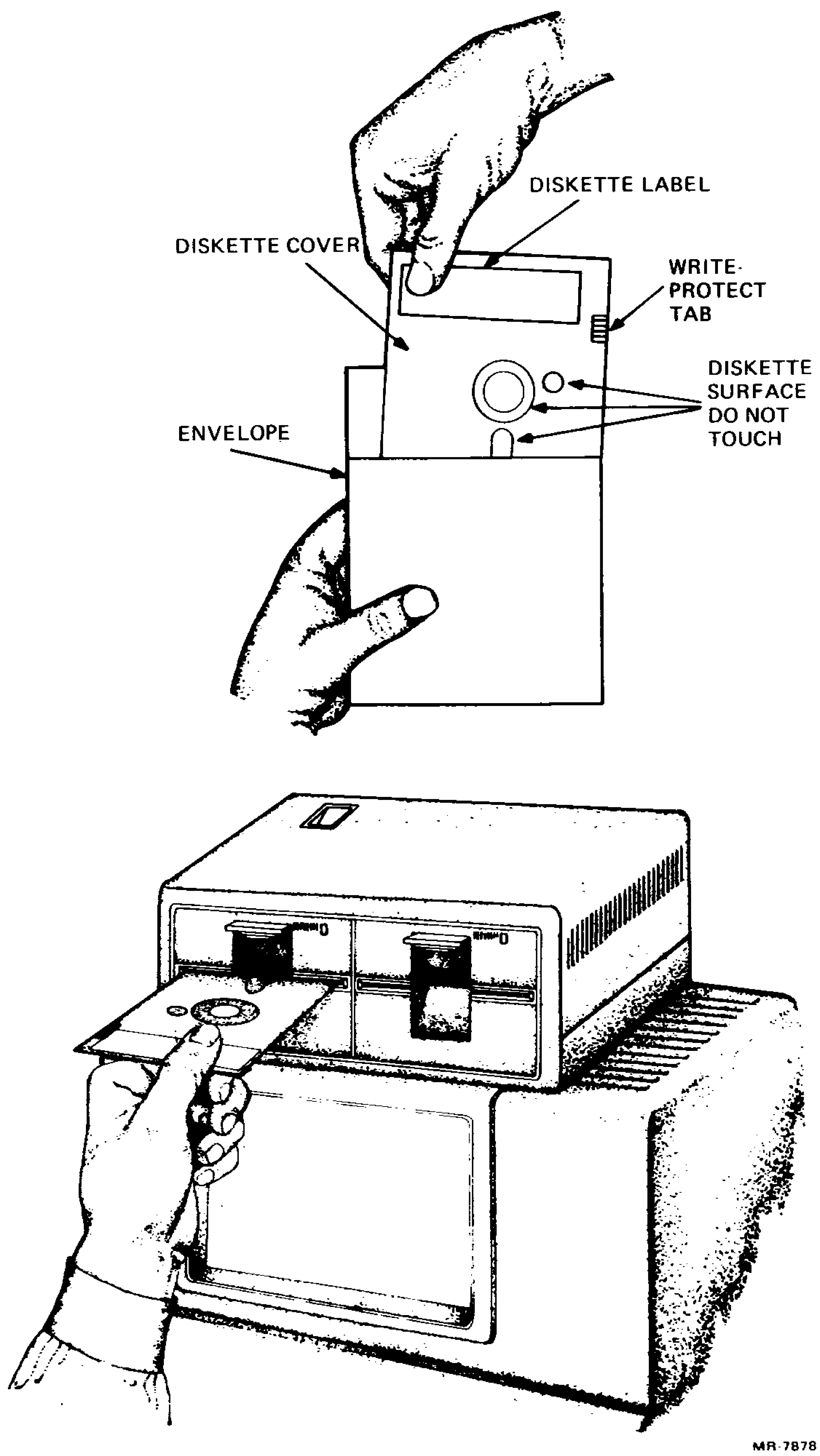
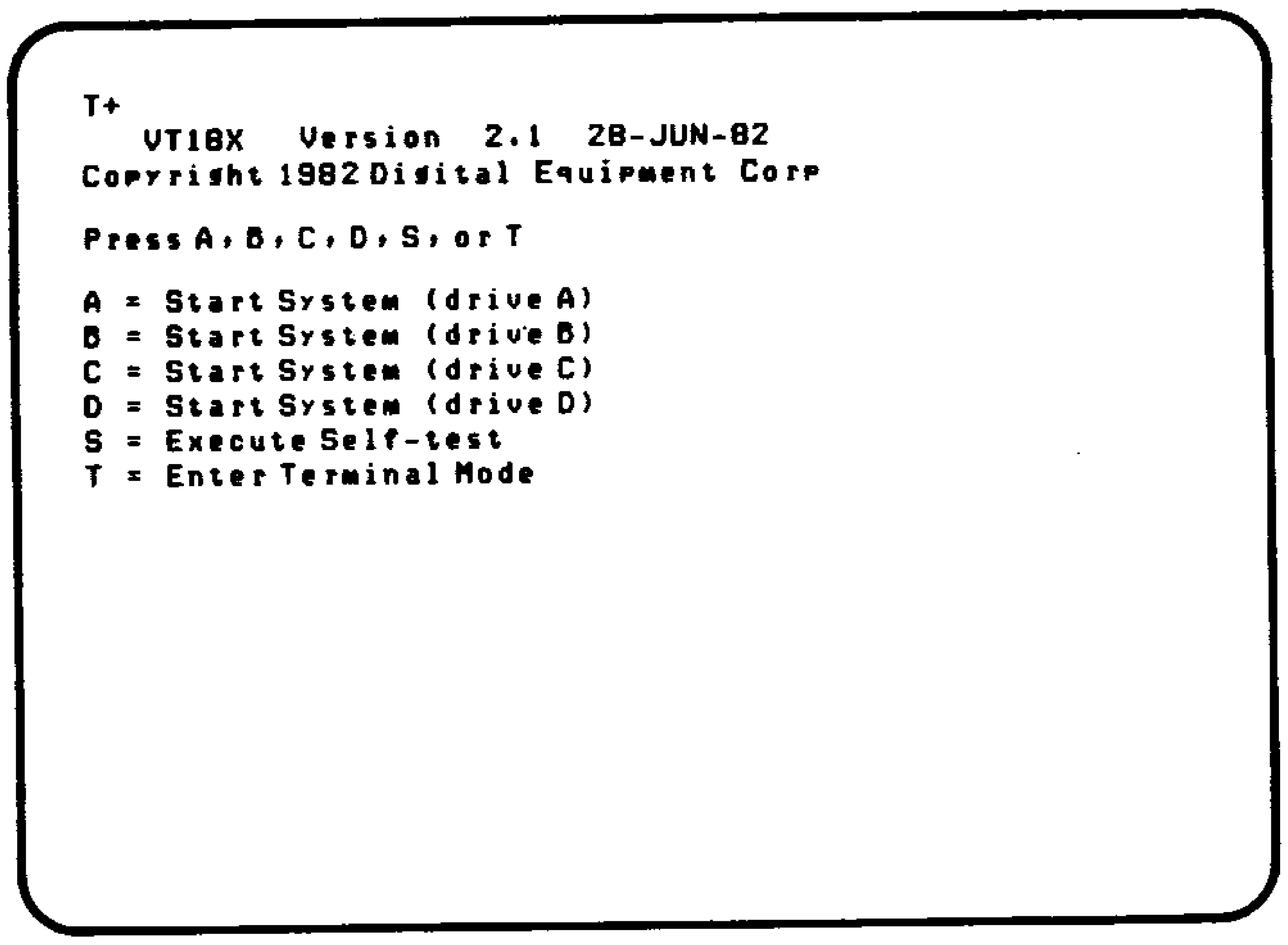


Figure 4-2 Loading the Diskette

2. Turn on the system power switch. If it is already on, turn off the power switch, wait for about four seconds, and then turn on the power switch again. After 20 or 30 seconds (sooner if you restarted a warm VT180), the automatic VT180 self-test should be completed, and the screen should display messages like those in Figure 4-3.



NOTE:
IF VERSION NUMBER IS OTHER THAN 2.1, CHECK THE VT18X CONTROL MODULE FOR LATEST REVISION ROMS.

MR-7880

Figure 4-3 Main System Menu

3. Find your CP/M master system disk (labeled CP/M-05-Version 1.0-BIN-5.25) and slide it out of its protective envelope (see Figure 4-2).

4. Insert the CP/M master system disk in drive A. Be sure to orient the disk with the label up and the write-protect tab to the left. (See Figure 4-2.)

5. Press A. You should immediately hear clicking and whirring sounds from drive A. This means that the system has begun reading the CP/M programs from the diskette into the VT180's memory.

   After a few seconds, the VT180 screen will clear and then display text like that shown in Figure 4-4. This means that the start-up process has successfully concluded and that the system is waiting to be told what to do next. If at this point the screen does not display text like that shown in Figure 4-4, proceed as follows.

   a. **The system is new and is being started up at your site for the first time.** Confirm that you have followed the above instructions exactly. Double-check connections and switch conditions and repeat the preceding steps.

   b. **The system has run successfully in the past for someone else.** Contact the last user and ask for help. The VT180 is a very flexible system and can be left in operational modes that the CP/M programs cannot deal with. If the last user cannot help, turn to Chapter 7, Service Information.

```
CP/M VERSION 2.2 (1.0)
(C) 1981 Digital Research Inc.

A>
```

MR-7259

Figure 4-4 Start System Display (Drive A)

6. If the system is being run for the first time after being installed, type DIR, then press the RETURN key. The system should display the contents of your CP/M master diskette. Check the names displayed on your screen against those shown in Figure 4-5.

```
A>DIR
A: LOAD     COM : PIP      COM : DDFMT    COM : MOVCPM   COM
A: DDCOPY   COM : SYSGEN   COM : ASM      COM : SUBMIT   COM
A: XSUB     COM : DDT      COM : STAT     COM : DUMP     COM
A: ED       COM : PSETUP   COM
A>
```

MR-7260

Figure 4-5 Directory Display

If you are the first user of a newly installed system, you must make a copy of the CP/M master diskette before running any other programs. The procedure for copying diskettes is described in Paragraph 4.5.

CAUTION

Copying the CP/M master diskette is very important. *Do not try to use the CP/M software without first making a copy of it and storing the original in a safe place.* This procedure guarantees a reliable source that can be copied again if any given copy is accidentally corrupted or destroyed.

If the system is not newly installed and the copies of the CP/M master disk have already been made, you may proceed in one of two possible directions.

1. If you have run CP/M on the VT180 before, you probably know what you want to do and will need to glance at appropriate parts of this manual only enough to remind you of details you have forgotten.

2. If you are running CP/M on the VT180 for the first time, you should carefully read the remainder of this chapter and Paragraph 2.3.2 (Keyboard Controls) of Chapter 2. If you have never used diskettes before, you should also read the Appendix (Storing, Handling, and Using Flexible Disks) in the *VT180 User's Guide*. If information is needed on the CP/M commands, they are also described in the *VT180 User's Guide*.

4.4 ENDING AN OPERATING SESSION

To end a VT180 operating session, remove and put away all diskettes. Then turn off the power switch on top of the disk drive unit.

CAUTION
Never turn system power on or off while a diskette is inserted in any drive.

4.5 COPYING THE CP/M MASTER DISKETTE

To make a copy of the CP/M master diskette, perform the following procedure. This procedure assumes you have started up the system with the CP/M master system diskette in drive A, as described at the beginning of this chapter.

1. Find a diskette with a blank label in the software distribution package. Slide it out of its envelope and insert it in drive B.

2. Type the commands when instructed to do so. The commands to be typed by the user in this procedure are indicated by an underline. <RET> throughout this procedure indicates you must press the RETURN key.

   <u>DDFMT<RET></u>

   The system will respond with the following display.

   DISK DDEN FORMAT/VERIFY PROGRAM
   4/82 REV A.1

   SELECT DRIVE (A,B,C OR D) OR RETURN TO EXIT

3. Respond to this display by pressing B.

   The system will display:

   INSERT NEW DISK IN DRIVE B
   TYPE RETURN TO CONTINUE, E TO EXIT :

4. Press <RET>.At this point, drive B will begin whirring and clicking and the system will display:

   n TRACK xx

   where n alternates between the letters F (format) and V (verify) and xx shows an incrementing number from 0 to 39.

   After some seconds, the system will display:

   V TRACK 39 - DISK FORMAT / VERIFY COMPLETED

   INSERT NEW DISK IN DRIVE B
   TYPE RETURN TO CONTINUE, E TO EXIT :

5. Press E. The system will return to the CP/M prompt:

   A>

   Your screen should now look like Figure 4-6. Your new diskette is ready to receive data. To copy the CP/M master system diskette to drive B, continue as follows.

```
A>DDFMT

DISK DDEN FORMAT/VERIFY PROGRAM
10/81  REV A.1

SELECT DRIVE (A,B,C OR D) OR RETURN TO EXIT : B

INSERT (OR REINSERT) NEW DISK IN DRIVE B
TYPE RETURN TO CONTINUE, E TO EXIT :
V TRACK  39 - DISK FORMAT/VERIFY COMPLETED


INSERT NEW DISK IN DRIVE B
TYPE RETURN TO CONTINUE, E TO EXIT : E
A>
```

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Figure 4-6 Format/Verify Display

6. Type DDCOPY<RET>. The system will respond by displaying:

   DISK DDEN COPY / VERIFY PROGRAM
   10/81 REV A.0

   SELECT SOURCE DRIVE (A, B, C OR D) :

7. Type A. The system will reply:

   SELECT DESTINATION DRIVE (B, C, D OR N(ULL))
   OR RETURN TO EXIT :

8. Type B. The system will respond:

   INSERT SOURCE DISK IN DRIVE A
   INSERT DESTINATION DISK IN DRIVE B

   COPY S(SYSTEM), D(ATA) OR B(OTH) :

   If you have been following the steps in this section, your source diskette (the CP/M master) is already in drive A, and your destination diskette (the blank diskette that you just formatted) is in drive B.

9. Press B. The system will display:

   COPYING ALL TRACKS
   nn TRACK xx

   where nn will alternate between the letters RS (read source), WD (write destination), and RD (read destination); xx will indicate which of the 40 tracks (numbered 0 to 39) is currently being copied or verified.

   When the copying operation is complete, the system will display:

   RD TRACK 39 - COPY / VERIFY COMPLETE TO DRIVE B

   SELECT DESTINATION DRIVE (B, C, D OR N(ULL))
   OR RETURN TO EXIT :

10. Press <RET>. The system will now display:

    INSERT SYSTEM DISK TO REBOOT
    TYPE RETURN TO CONTINUE

11. Press <RET>. The system will now display the CP/M prompt:

    A>

    Figure 4-7 shows the entire copy dialog.

12. Remove the diskette from drive B and replace it in its envelope.

13. Label this diskette CP/M Distribution Backup.

14. Repeat the formatting/copying process a second time with another blank diskette, and label this diskette CP/M Working Copy.

15. Remove the CP/M master diskette from drive A, return it to its envelope, and store it and the backup copy in a safe place.

```
A>DDCOPY

DISK DDEN COPY/VERIFY PROGRAM
10/81 REV A.0

SELECT SOURCE DRIVE (A,B,C OR D) : A

SELECT DESTINATION DRIVE (B,C,D OR N(ULL))
 OR RETURN TO EXIT : B

INSERT SOURCE DISK IN DRIVE A
INSERT DESTINATION DISK IN DRIVE B

COPY S(YSTEM), D(ATA) OR B(OTH) : B

COPYING ALL TRACKS
RD TRACK 39  - COPY/VERIFY COMPLETE TO DRIVE B

SELECT DESTINATION DRIVE (B,C,D OR N(ULL))
 OR RETURN TO EXIT :

INSERT SYSTEM DISK TO REBOOT
TYPE RETURN TO CONTINUE
A>
```

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Figure 4-7 Copy/Verify Display

4.6 USING THE VT180

The CP/M control program must be transferred from the diskette into the VT180 memory whenever the VT180 is to be used in personal computer mode as described in Paragraph 4.3. This is called bootstrapping or booting the system. There are two ways to start the system: by performing a cold start or a warm start.

A cold start is performed when:

1. The power switch is off and you have to turn it on before starting the system. If you have not already turned on the power, follow the directions in Chapter 2 for starting the VT180.

2. The power is already on, the system was previously started, and you want to reset the system (for example, to switch from terminal mode to computer mode). To perform a reset, press the SET-UP key and then the RESET key (the zero key on the main keyboard).

A warm start is performed when the system was previously started, and you want to restart it (for example, after you change diskettes in a drive or if some condition the system encountered caused it to stop). To restart the system, use the command called <CTRL/C>. Press the control key (CTRL on the keyboard) and hold it down while typing the letter C.

This section explains how to proceed when it is necessary to perform a cold or warm start.

When you turn on the power, the VT180 displays the Main System menu shown in Figure 4-3. When you perform a reset, the VT180 displays the messages shown in Figure 4-8. When you type <CTRL/C>, CP/M is reactivated and displays A>.

When CP/M displays the messages, type A to start CP/M from drive A. The terminal displays the message shown in Figure 4-4.

CAUTION

Always start CP/M from drive A since many of the application programs you will run require it to be there. Failure to do so may result in loss of data or damage to the CP/M software.

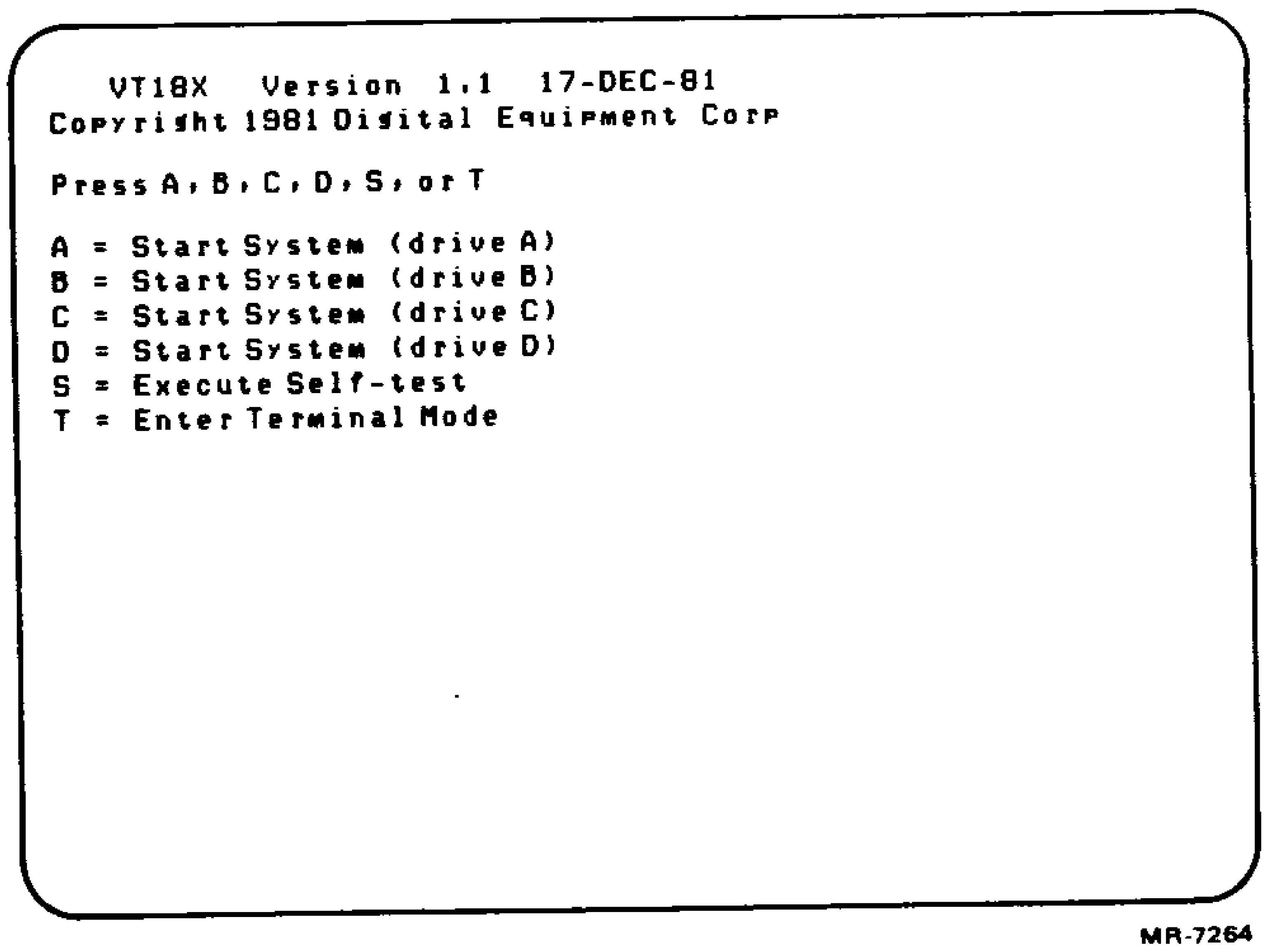


Figure 4-8 Reset Display

4.7 CONVERSING WITH CP/M

When CP/M is ready to accept commands, it displays a prompt at the left side of the terminal screen. Because it can access up to four disk drives, CP/M always prompts with the name of the drive it is currently accessing (A, B, C, or D) and a right-angle bracket (>). For example, if the current or active drive is drive A, CP/M displays:

A>

and waits for a command. Commands can be issued to CP/M whenever it displays the prompt.

4.8 ISSUING COMMANDS

Generally, after typing a command, pressing the RETURN key tells CP/M to execute the command. In this manual, the symbol <RET> means that the RETURN key should be pressed. Some CP/M programs, however, display messages such as <CR> (for carriage return), or RETURN to indicate that the RETURN key must be pressed.

A few CP/M programs ask questions requiring a single-character response. Some of these programs process the response as soon as it is typed, without waiting for the RETURN key to be depressed. In such instances, care must be exercised since a typing error could alter or destroy the software.

The best protection against trouble is to write-protect diskettes where instructed to do so, and to keep copies of the software. You can protect any diskette from being written on by any program by using the self-sticking write-protect tabs provided by the manufacturer. Apply these tabs as shown in Figure 4-9. This mechanism prevents the inadvertant destruction of data by you or anyone else. The write-protect tab may be removed at any time to return the diskette to its normal, writable state.

4.9 RESIDENT AND TRANSIENT CP/M COMMANDS

CP/M recognizes two kinds of commands: resident and transient. Resident commands are built in to CP/M. You will not see them in the directory; but the programs for them are part of the CP/M operating system. Any time the system is running, the commands are in memory and can be used. The resident commands follow.

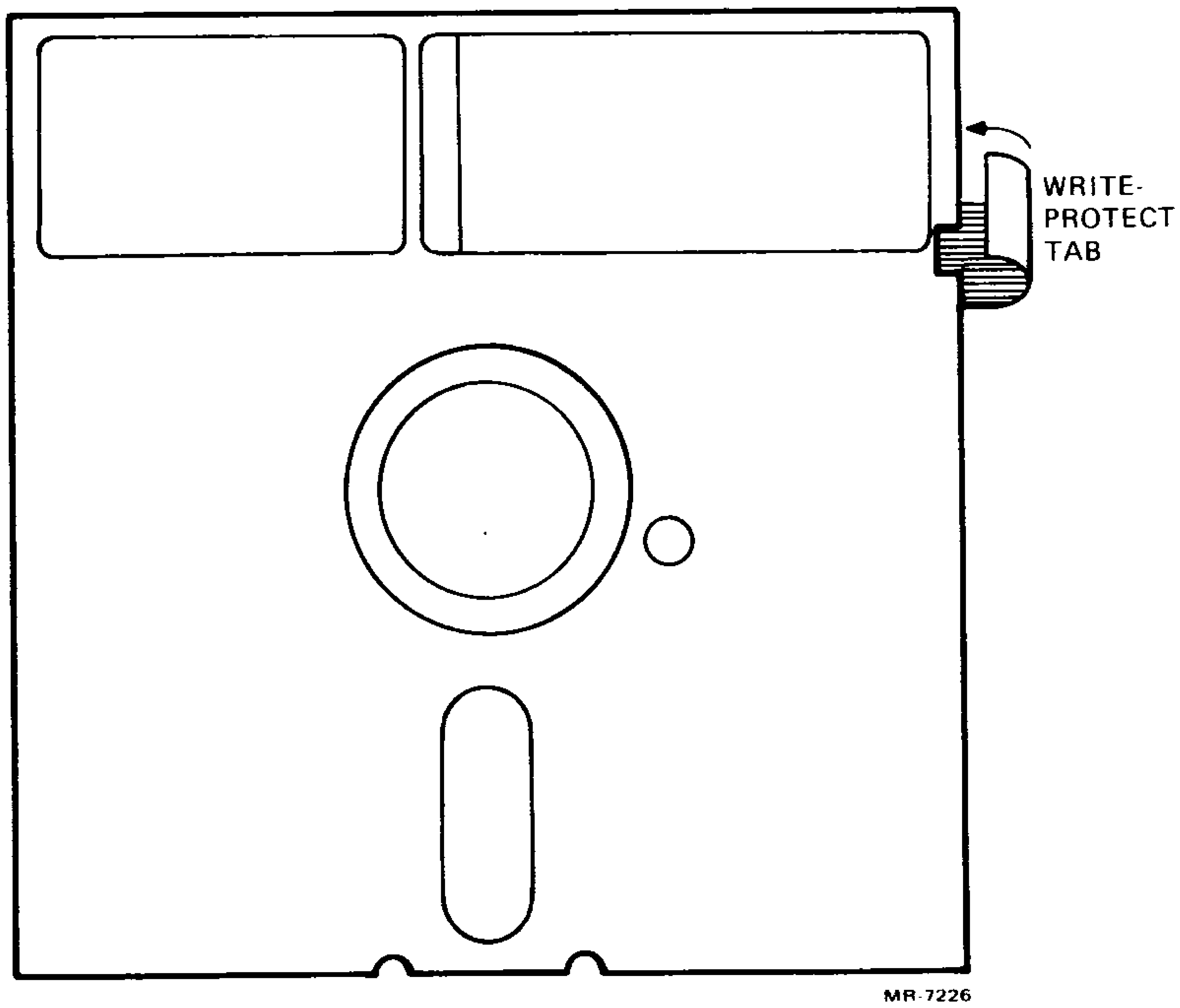


Figure 4-9 Applying a Write-Protect Tab

DIR	Displays a directory.
ERA	Deletes a file or files from a diskette.
REN	Renames a file.
TYPE	Displays the contents of a file.

Transient commands are not usually in memory when CP/M is running. Because the programs for them are longer than those for the resident commands, transient commands exist as files on a diskette and must be brought into the computer's memory before they can be used. Transient commands have the file type .COM. If such a file is on the diskette in the current drive, you can invoke it by typing the file name, as you did when you ran DDFMT. Otherwise, you must find which diskette it is on, load the diskette in a drive, and specify that drive when you type the file name. Alternatively, you can copy the file to the current diskette if space permits. Examples of transient commands that are used most frequently follow.

DDCOPY.COM	Copies a diskette.
DDFMT.COM	Formats diskettes.
ED.COM	Creates and modifies text files.
PIP.COM	Copies files.
STAT.COM	Provides information about files and diskettes.

For additional information on using CP/M commands, refer to the *VT180 User's Guide*.

4.10 RUNNING APPLICATION PROGRAMS

CP/M is a popular operating system because many application programs have been written to run under it. These programs have been developed by numerous companies. Because procedures for running such programs can vary, you will have to consult the documentation that comes with them for detailed operating instructions. In general, however, the VT180 makes it easy to run an application program. Usually, it will have the file type .COM and it may be invoked simply by typing its name.

CHAPTER 5
SETTING THE SERIAL PORTS' TRANSMISSION CHARACTERISTICS

5.1 INTRODUCTION

This chapter describes the procedure for setting the transmission characteristics of the serial ports using the PSETUP command. More information on this command and the other CP/M commands may be found in the *VT180 User's Guide*.

5.2 PSETUP

The PSETUP command runs PSETUP.COM, which allows you to change the transmission characteristics of the VT180 serial ports to match the transmission characteristic of the external devices connected to these ports. On a new system, the VT180 sets these characteristics at start-up to the default conditions specified in Table 5-1. If these defaults are not compatible with the devices you wish to connect to these ports, you must select appropriate characteristics with PSETUP.

Table 5-1 Serial Port Default Characteristics

Port	Transmission Speed (Baud Rate)	Bits/ Character	Stop Bits	Parity
Printer	1200	7	2	None
General purpose	1200	8	1	None
Communications	*	8	1	None

*Last saved transmission speed in SET-UP B.

NOTE

PSETUP allows you to set serial port characteristics on a temporary or permanent basis. The temporary change preserves the selections only until the next cold or warm start. The permanent change rewrites the default areas on the disk so that the new characteristics persist until you run PSETUP and change them again. If the situation does not permit saving serial port characteristics, you can use SUBMIT and XSUB to automate set-up changes and thus avoid having to run PSETUP manually each time you use a serial port. See XSUB in the *VT180 User's Guide* for examples of such a procedure.

The PSETUP command has the following form:

PSETUP<RET>

PSETUP accepts user responses in two modes.

1. Menu, in which PSETUP displays menus you can select desired options from.
2. Concise, in which PSETUP allows option selections to be linked together.

5.2.1 Menu Mode
Run PSETUP by typing its name in response to the CP/M prompt.

PSETUP<RET>

The system will respond by loading and starting PSETUP.COM, which will display the following.

SERIAL PORT CONFIGURATION CONTROL VERSION 1.X
COMPLETE SELECTION BY PRESSING <RETURN> KEY

NOTE: THIS PROGRAM MODIFIES MEMORY AND THE SYSTEM DISK.

PRESS KEY	FOR
B	BAUD RATE SELECTION
C	COMM PORT DATA/STOP BITS/PARITY
G	GENERAL PURPOSE PORT DATA/STOP BITS/PARITY
P	PRINTER PORT DATA/STOP BITS/PARITY
S	SHOW ALL SELECTIONS MADE
D	SET PARAMETERS TO DEFAULT VALUES
R	RETURN TO CP/M

A discussion of these selections follows.

5.2.1.1 Baud Rate Selection – If this option is selected, PSETUP asks you to choose a baud rate for both the general purpose port and the printer port. You must choose a baud rate for the general purpose port (even if you are not using it) before you are allowed to choose a rate for the printer port. PSETUP does not give you the option of setting the communications port baud rate since this can be done in terminal SET-UP B (see Chapter 2). The default baud rate for the general purpose port is 1200; for the printer port it is also 1200.

5.2.1.2 Communications Port Data/Stop Bits/Parity – Select this option if you are using the communications port for something other than terminal mode operation. Note that terminal mode is controlled by a program in read-only memory (ROM) that accepts whatever transmission characteristics have been installed through VT180 SET-UP B (see Chapter 2). However, only the ROM program can modify the behavior of the communications port hardware in response to changed VT180 set-up conditions. CP/M programs are unable to make use of the VT180 parameter exchange protocol.

If option C is selected, PSETUP asks you to choose between seven or eight data bits, one or two stop bits, and even, odd, or no parity. Refer to the documentation for the device in question to determine how these attributes should be set. The default transmission characteristics of the communications port are eight data bits, one stop bit, no parity.

5.2.1.3 General Purpose Port Data/Stop Bits/Parity – If this option is selected, PSETUP asks you to select seven or eight bits, one or two stop bits, and odd, even, or no parity. Refer to the documentation for the device in question to determine how these attributes should be set. The default transmission characteristics of the general purpose port are eight data bits, one stop bit, no parity.

5.2.1.4 Printer Port Data/Stop Bits/Parity – If this option is selected, PSETUP asks you to select seven or eight data bits, one or two stop bits, and odd, even, or no parity. Refer to the documentation for the device in question to determine how these attributes should be set.

The default transmission characteristics of the printer port are seven data bits, two stop bits, no parity. This is equivalent to eight data bits with the eighth bit fixed at mark, and one stop bit. It is also equivalent to seven data bits, parity equal to fixed mark, and one stop bit.

5.2.1.5 Show All Selections Made – If this option is selected, PSETUP displays all selections you have made during the current session.

5.2.1.6 Set Parameters to Default Selections – This option permits a quick return to the last saved conditions of the serial ports.

5.2.1.7 Return to CP/M – This selection causes PSETUP to implement whatever selections you have made and then returns to the CP/M prompt.

NOTE

Pressing RETURN alone in response to a given menu causes all selections provided by the menu to be set to their default condition.

5.2.2 Concise Mode

Once you become familiar with the selection sequences required to affect particular set-up changes on given serial ports, the set-up operation can be shortened considerably by using PSETUP's concise mode. In this mode, you simply string together all the expected responses to the various PSETUP menus, separating each entry with a comma, and terminate the entire string with a RETURN. The second example that follows shows how this might be done.

NOTE

With one exception, concise mode executes the S option (which shows current changes and defaults) after the selection string is executed. That exception is the case in which the string ends with R, which causes the S option to be bypassed. In this case, PSETUP asks if you want to make the selections permanent, then implements the selections, and returns to the CP/M monitor.

5.3 PSETUP EXAMPLES

5.3.1 Menu Mode

The following example shows PSETUP used to set the printer port to 300 baud, 8 data bits, 1 stop bit, no parity. (The general purpose port is also set to 300 baud, but this is an incidental side effect of PSETUP's requirement that both printer and general purpose port baud rates be set at the same time.)

```
A>PSETUP<RET>

SERIAL PORT CONFIGURATION CONTROL VERSION 1.X
COMPLETE SELECTION BY PRESSING <RETURN> KEY

NOTE: THIS PROGRAM MODIFIES MEMORY AND THE SYSTEM DISK.

      PRESS KEY          FOR

      B                  BAUD RATE SELECTION
      C                  COMM PORT DATA/STOP BITS/PARITY
      G                  GENERAL PURPOSE PORT DATA/STOP BITS/PARITY
      P                  PRINTER PORT DATA/STOP BITS/PARITY
      S                  SHOW ALL SELECTIONS MADE
      D                  SET PARAMETERS TO DEFAULT VALUES
      R                  RETURN TO CP/M

P<RET>
GP (GENERAL PURPOSE PORT)

      PRESS KEY          FOR BAUD RATE

      1                    75
      2                   150
      3                   300
      4                   600
      5                  1200
      6                  2400
      7                  4800
      8                  9600

3<RET>
P (PRINTER PORT)

      PRESS KEY          FOR BAUD RATE

      1                    75
      2                   150
      3                   300
      4                   600
      5                  1200
      6                  2400
      7                  4800
      8                  9600

3<RET>
```

PRESS KEY	FOR
B	BAUD RATE SELECTION
C	COMM PORT DATA/STOP BITS/PARITY
G	GENERAL PURPOSE PORT DATA/STOP BITS/PARITY
P	PRINTER PORT DATA/STOP BITS/PARITY
S	SHOW ALL SELECTIONS MADE
D	SET PARAMETERS TO DEFAULT VALUES
R	RETURN TO CP/M

B<RET>

PRESS KEY	FOR
7	7 DATA BITS
8	8 DATA BITS .p2;8<RET>

PRESS KEY	FOR
1	1 STOP BIT
2	2 STOP BITS

1<RET>

PRESS KEY	FOR
D	NO PARITY
E	EVEN PARITY
O	ODD PARITY

D<RET>

PRESS KEY	FOR
B	BAUD RATE SELECTION
C	COMM PORT DATA/STOP BITS/PARITY
G	GENERAL PURPOSE PORT DATA/STOP BITS/PARITY
P	PRINTER PORT DATA/STOP BITS/PARITY
S	SHOW ALL SELECTIONS MADE
D	SET PARAMETERS TO DEFAULT VALUES
R	RETURN TO CP/M

S<RET>
COMM PORT BAUD RATES FROM SET-UP B
GP (GENERAL PURPOSE) PORT = 300 BAUD
PRINTER PORT = 300 BAUD
PRINTER PORT PARAMETERS = 8 DATA BITS, 1 STOP BITS, NO PARITY

PRESS KEY	FOR
B	BAUD RATE SELECTION
C	COMM PORT DATA/STOP BITS/PARITY
G	GENERAL PURPOSE PORT DATA/STOP BITS/PARITY
P	PRINTER PORT DATA/STOP BITS/PARITY
S	SHOW ALL SELECTIONS MADE
D	SET PARAMETERS TO DEFAULT VALUES
R	RETURN TO CP/M

R<RET>
YOU CAN MAKE YOUR CURRENT SELECTIONS TEMPORARY (UNTIL THE NEXT WARM OR COLD START) OR PERMANENT (UNTIL YOU RERUN THIS PROGRAM).

DO YOU WISH TO MAKE YOUR CURRENT SELECTIONS PERMANENT? (Y OR N)

N<RET>
A>

5.3.2 Concise Mode
The following example uses concise mode to specify the same transmission characteristics for the printer port as those specified in the previous menu mode example.

A>PSETUP<RET>
.
.
.

PRESS KEY	FOR
B	BAUD RATE SELECTION
C	COMM PORT DATA/STOP BITS/PARITY
G	GENERAL PURPOSE PORT DATA/STOP BITS/PARITY
P	PRINTER PORT DATA/STOP BITS/PARITY
S	SHOW ALL SELECTIONS MADE
D	SET PARAMETERS TO DEFAULT VALUES
R	RETURN TO CP/M

B,3,3,P,8.1,D,S,R<RET>
COMM PORT BAUD RATES FROM SET-UP B
GP (GENERAL PURPOSE) PORT = 300 BAUD
PRINTER PORT = 300 BAUD
PRINTER PORT PARAMETERS = 8 DATA BITS, 1 STOP BIT, NO PARITY

YOU CAN MAKE YOUR CURRENT SELECTIONS TEMPORARY (UNTIL THE NEXT WARM OR COLD START) OR PERMANENT (UNTIL YOU RERUN THIS PROGRAM).

DO YOU WISH TO MAKE YOUR CURRENT SELECTIONS PERMANENT? (Y OR N)

N<RET>
A>

5.4 PSETUP ERROR MESSAGES

An inappropriate response to a menu in menu mode causes PSETUP to repeat the selected menu. An inappropriate specifier in concise mode causes PSETUP to abort the remainder of the string and display the menu for the operation that was current at the point the error was encountered.

Note that you cannot make serial port selections permanent if your PSETUP diskette is equipped with a write-protect tab. The effort to do so generates:

WRITE ERROR - DRIVE drv TRACK t SECTOR s

This occurs because making the serial port selections permanent involves writing the new set of default conditions to the system area on the write-protected diskette.

CHAPTER 6
TECHNICAL DESCRIPTION

6.1 INTRODUCTION

This chapter provides a technical description of the VT180 operating principles for repair or maintenance personnel. The VT180 is presented as a system consisting of several functional or replaceable subunits. The subunits will be described at the system level followed by a functional description of each subunit in its own section. Interaction between subunits is discussed in the section about the subunit most involved in the particular process.

The VT180 hardware is described both to the block diagram level and the functional block diagram level. The VT180 Field Maintenance Print Set (MP00633), the VT18X control module circuit schematics (CS 5415152-0-1), and the VT180 paddle board circuit schematics (CS 5415150-0-1) contain circuit details for the various subunits. These circuit schematics may be used while studying this chapter.

Numbers may be given in binary, octal, decimal, or hexidecimal (hex). The normal form will be decimal for scalar or ordinal values, and hex for data and addresses. Numbers are subscripted B for binary, Q for octal, H for hex, and there is no subscript for decimal.

6.2 SYSTEM DESCRIPTION

The VT180 personal office computer is a VT100 terminal that has been upgraded by installing a VT18X personal office computing upgrade kit. The addition of the VT18X upgrade kit provides the basic VT100 with the capability to operate in either personal computer mode or terminal mode. In personal computer mode, the VT180 runs under the control of an operating system called CP/M. CP/M allows the VT180 to run the many available CP/M programs that have been developed for various applications. In terminal mode, the VT180 retains VT100 functionality, and thus is capable of communicating with an external host computer.

The VT180 has the following features.

1. Full VT100 functionality (except for printer port emulation)
2. Two operating modes (personal computer or terminal)
3. Extensive power-up self-test diagnostics
4. Z80® instruction set VT18X control module
5. A VT131 hardware compatible communications port
6. A printer port
7. A general purpose serial port
8. One or two RX180 dual disk drive units with up to 720K bytes of formatted data

6.2.1 System Subunits

The VT180 consists of a VT100, a VT18X control module, one or two RX180 dual disk drive units, a VT180 paddle board, RF shielding, signal and power cables, and miscellaneous mounting hardware. The various subunits of the VT180 are shown in the block diagram of Figure 6-1.

Z80® is a registered trademark of Zilog, Inc.

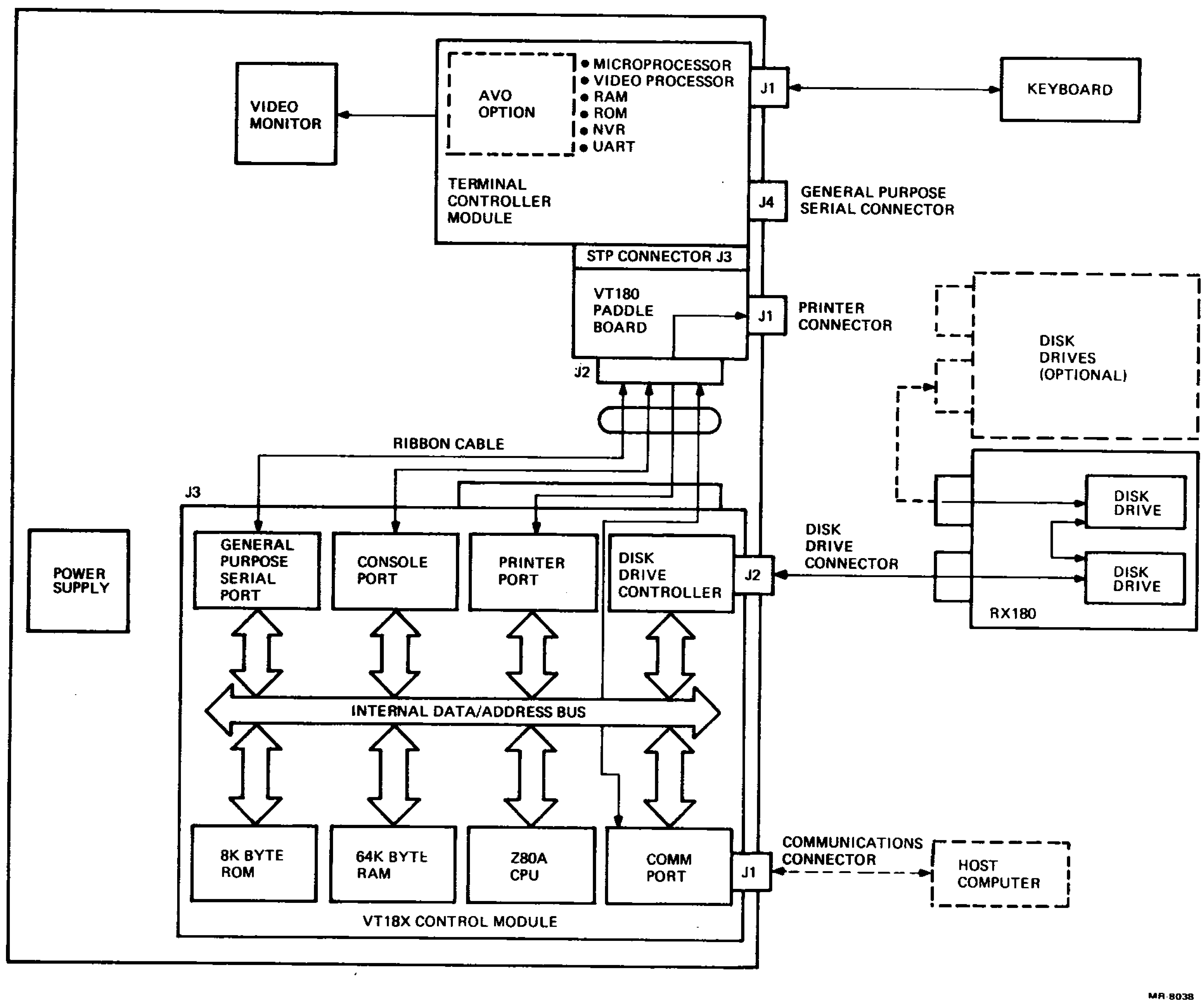


Figure 6-1 VT180 System Block Diagram

6.2.1.1 Terminal Controller Module – The terminal controller is a single module that manages all displays and all communication between the keyboard and the host computer. Everything else connects to it. The terminal controller contains these functional components.

1. A microprocessor to manage terminal operations

2. A video processor for converting data to recognizable patterns

3. 3072 bytes of random-access memory (RAM) for screen data storage and microprocessor scratch memory

4. 8192 bytes of read-only memory (ROM) containing the microprocessor's programming to operate the terminal with its particular features

5. A nonvolatile RAM (NVR) to store the user-selectable operating features without requiring hardware switches

6. An asynchronous serial receiver-transmitter (UART) for data exchange with the personal computer or host computer

7. EIA level converters to adapt the on-board input and output (I/O) signals to the communications interface

6.2.1.2 Advanced Video Option (AVO) – The advanced video option provides greater display capacity, and it can carry extra firmware for the expanded functionality of other products in the VT180 series. The AVO is mounted on the terminal controller module.

6.2.1.3 Video Monitor – The video monitor is a video screen that displays exchanges between the operator and the personal computer or the host computer. It can display data in two modes: 80 characters by 24 lines, or 132 characters by 14 lines (or, with the AVO, 132 by 24). With the control circuitry on the terminal controller board, the CRT can perform many special character display functions.

6.2.1.4 VT180 Power Supply – The power supply converts the ac power line to the four dc voltages required by the terminal. It has a switching regulator for highest efficiency and coolest operation.

6.2.1.5 Keyboard – The keyboard is a typewriter-style input device for the operator. It has a loudspeaker for user feedback, keyclicks and bells, and indicators (LEDs) that show internal states of the terminal.

6.2.1.6 VT18X Control Module – The VT18X control module is a single-board microcomputer with a Z80A processor operating at 4 MHz and with 64K bytes RAM, 8K bytes software deselectable ROM, 4 communications ports, and an RX180 disk drive controller. The communications ports and disk drive controller functions are described in the following paragraphs.

Console Port
The console port communicates with the VT180 via the STP connector. Transmit and receive baud rates are fixed by the 15.7K bytes local clock on that connector. The console supports RS-232C signals, including transmit data, receive data, and data terminal ready from the VT180 for control. Software must support the XON/XOFF protocol for this port.

Communications Port
This port is used to communicate to another computer. It has full modem support and supports the same hardware signals as the VT131. It can support United States and European full- and half-duplex modems. The port has ASYNC as well as BISYNC modes with an RS-232C (V.24/V.28) physical interface conforming to CCITT V.21, V.22, and V.23. Break detection by this port is supported. The transmit and receive baud rates for this port are derived from the baud rate clocks on the terminal controller module. Therefore, the transmit and receive baud rates selected in the VT180's SET-UP B mode are the transmit and receive baud rates used for this port.

NOTE

It is important to note that the standard VT100 communications port (J4) on the terminal controller module now becomes a general purpose serial port, and the full communications port to the host computer is now the 25-pin, D-type connector (J1) on the VT18X control module.

Baud rates supported by the communications port are 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 9600, and 19,200. This port also has the capability to select external send and receive clocks supplied by a modem. Any and all protocols to be supported by this port, other than terminal emulation pass-through mode, are run as applications under CP/M. The recommended cables are BC26R-10 and BC22B-10. A BC22C-10 must be used for bisynchronous operation.

Certain transmit and receive signals on the communications port are routed through a ten position switch on the VT18X control module. This switch is used to configure the module for use with various communications modems. Refer to Paragraph 6.6.6 for the modem switch configurations.

Printer Port
This is a printer port that provides an RS-232C serial interface compatible with Digital printers. EIA signals supported are transmit data, receive data, and data terminal ready. Programmable baud rates supported are 75, 150, 300, 600, 1200, 2400, 4800, and 9600. Programmable character formats supported are 5, 6, 7, and 8 bits/character with 1, 1½, and 2 stop bits/character. Parity can be configured to none, odd, or even. Software should support XON/XOFF protocol for this port. This port requires a null modem cable. The 25-pin, D-type EIA printer port connector physically resides on the VT180 paddle board in the normal printer port location. The recommended cable for this port is a BC26U-15. A BC22A will also work but is a second choice.

General Purpose Serial Port
This port is provided as a general purpose RS-232C interface. Signals that are supported are transmit data, receive data, and data terminal ready. Programmable baud rates supported are 75, 150, 300, 600, 1200, 2400, 4800, and 9600. Parity can be configured to none, odd, or even. Programmable character formats that are supported are 5, 6, 7, and 8 bits/character with 1, 1½, and 2 stop bits/character. This port uses the VT100 communications port connector (J4) on the terminal controller module. Signals are passed from the VT18X control module through a ribbon cable to the VT180 paddle board. This port requires a null modem cable. A BC26U-XX is the recommended cable for this port. Another cable that may be used is a BC22A in either 10 or 25 foot length.

Disk Drive Unit Interface
This interface controls up to four 5¼ inch disk drives. The controller circuit supports double-density drives using a phase locked loop (PLL) circuit. Only soft-sectored, single-sided diskettes are supported. The interface adheres to drive capability and signal definition of the ANSI standard interface for disk drives. The connector to the drives is a 37-pin, D-type shielded cable (BC26K). This connector physically resides on the VT18X control module.

6.2.2 VT100 and VT18X Control Module Interconnection
The terminal controller module is interconnected to the VT18X control module by a 16-pin cable to the VT180 paddle board. This interconnection is very important in the operation of the VT180. All four serial ports on the VT18X control module depend upon signals from this connector. The INIT line from the terminal controller module to the Z80A CPU is also supplied via this channel. A 16-pin ribbon cable (70-08612-OM), which is 27.94 cm (11 inches) long, is used for the connection.

6.2.3 VT180 Paddle Board
The VT180 configuration has its own paddle board, which consists of the board (50-15149); a 25-pin, D-type EIA connector for the printer port; a jumper; and a 16-pin socket. Other components are present for FCC considerations. The 16-pin socket is used to connect the STP port and the VT18X control module. Printer, communications clocks, and general purpose serial port signals are supplied by the 16-pin ribbon cable connecting the VT100 terminal controller module and the paddle board.

6.2.4 RX180 Disk Drive Unit
The RX180 disk drive unit consists of two disk drives. In double-density operation, the RX180 will store 360K bytes of formatted data (180K bytes per drive). Two versions of the RX180 are available: an

RX180-AB, which is configured as CP/M drives A and B, and an RX180-AD, which is configured as drives C and D.

The RX180 contains its own power supply and is controlled by the VT18X control module via the disk drive connector, J2. The ac power cabling is serially routed through the drive units to the VT180 terminal. This routing scheme allows the user to power up the entire VT180 in a two drive unit system by using the power switch on the top drive unit.

6.3 VT100 FUNCTIONAL DESCRIPTION

The basic VT100 consists of the functional blocks shown in Figure 6-2. All of the subunits shown, with the exception of the keyboard, reside inside the terminal cabinet. This section provides a general description of each of the functional blocks.

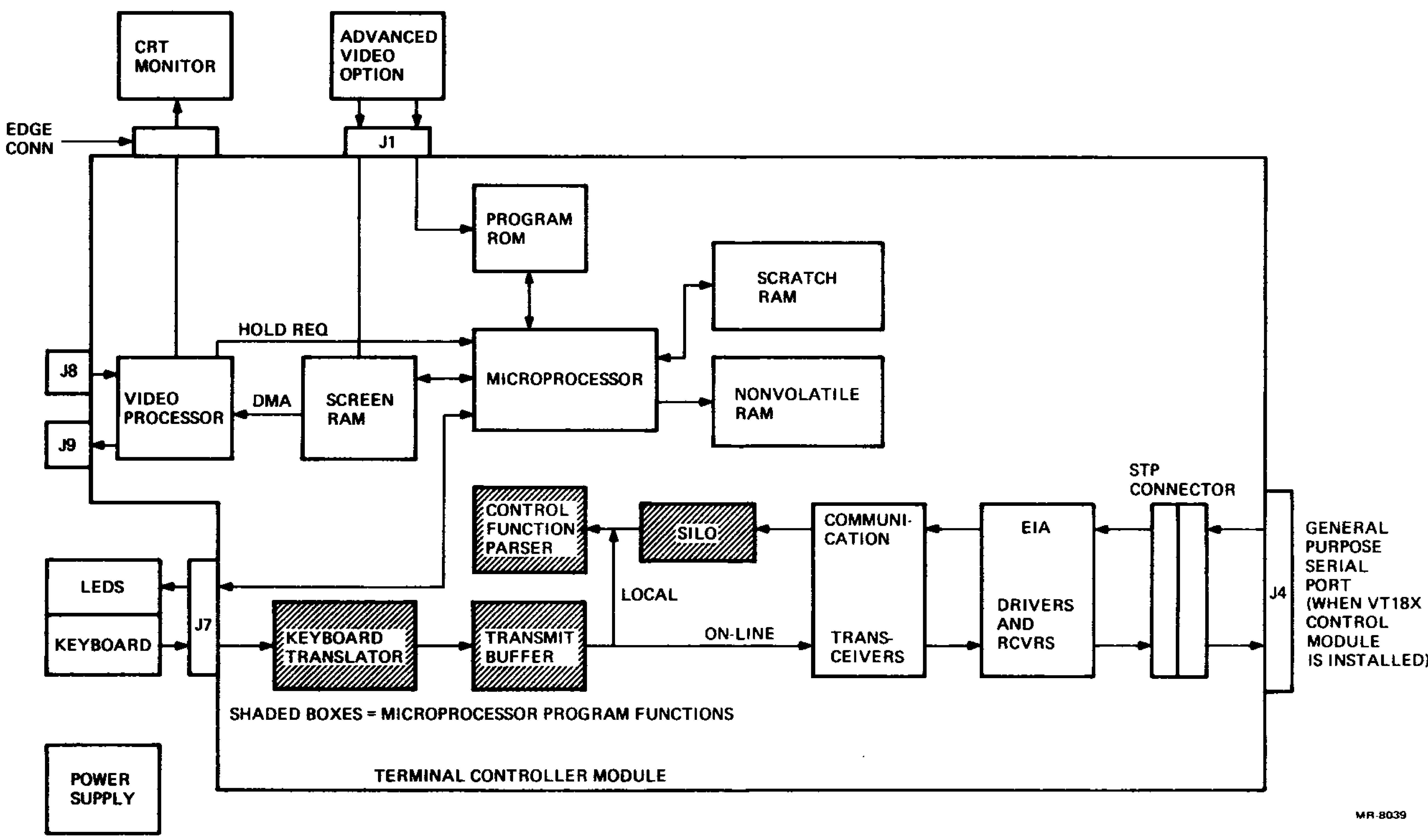


Figure 6-2 VT100 Functional Block Diagram

6.3.1 Microprocessor

A microprocessor (8080A) manages all terminal input and output operations. It also provides the intelligence that enables the VT100 to respond to and generate a wide range of ANSI control functions and to emulate the characteristics of the VT52. Several of the microprocessor's program functions are effectively in series with data paths in the terminal. These functions have their own blocks in the functional block diagram to clarify the processes involved. These blocks are shaded to indicate that they are program functions or that the microprocessor controls data transfers between the blocks. The microprocessor is a computer with its instructions in program ROM (read-only memory) and its working memory in the scratch RAM (random-access memory). Terminal parameters for start-up are stored in the nonvolatile RAM (NVR). The advanced video option (AVO) normally contains extra RAM, as described in Paragraph 6.3.5. It can also contain extra program ROM.

6.3.2 Program ROM

The VT100 program ROM is an 8K by 8 memory containing instructions and data tables for the terminal's microprocessor. Memory comes in four 2K packages (later VT100s may have a single 8K package). Checksum data stored in each ROM allows the terminal to confirm the condition of its programming during self-test.

6.3.3 Scratch RAM

The scratch RAM is the portion of RAM on the terminal controller that is not used for the screen RAM. That is, the RAM is 3K bytes long, but only about 2.3K bytes are used for screen display. The rest of the RAM contains the microprocessor stack, set-up data, various flag bytes, the communication silo, the keyboard buffer, and so on.

6.3.4 Nonvolatile RAM

The nonvolatile RAM (NVR) does not lose its data when its power is off. It stores all user-selectable features and parameters and the answerback message so that they are available each time the terminal is turned on. Even the screen intensity can be stored. There are no mechanical switches needed for configuration.

6.3.5 Advanced Video Option

The advanced video option (AVO) contains the 1K by 8 of extra screen RAM needed to expand the display from 14 lines of 132 characters to 24 lines. It also contains a 4K by 4 RAM to store an extended set of attributes for all characters. The AVO has an additional segment of video processor to manage the four extra bits of data. Sockets for ROMs and jumper- or switch-programmable decoders allow expansion or overlay of program memory. The AVO is a replaceable subunit of the VT180.

6.3.6 Keyboard

The keyboard is the user's input device to the terminal. The keyboard's output is a serial data signal that travels along the same wire as data coming from the terminal. The keyboard contains a bidirectional interface circuit, a set of keyswitches arranged like a typewriter, circuits to send the key information to the interface, LED indicators, and a small loudspeaker for keyclicks and bells. The connection to the terminal is a three-wire coil cord carrying signals, power, and ground. The keyboard is a replaceable subunit of the VT180.

6.3.7 LEDs

The terminal can inform the user of some internal conditions, such as on-line, local, and keyboard locked, through the LEDs on the keyboard. The LEDs also may indicate the location of a failure during self-test. They are user-programmable during normal operation.

6.3.8 Keyboard Translator

The output for each key is a number that represents the key's location (address) in the keyboard switch matrix. The microprocessor's keyboard translator translates the address to the industry-standard ASCII code.

6.3.9 Transmit Buffer

The ASCII codes wait in a transmit buffer until they can be transmitted. Some keys (such as the numeric keypad in application mode) produce control functions that are three bytes long. The transmit buffer is nine bytes long and thus can store at least three keys of any kind.

6.3.10 Communication Transmitter

The communication transmitter is one-half of a programmable universal synchronous/asynchronous receiver-transmitter (PUSART) and its associated circuitry and firmware routines. The PUSART is programmed to place data in a standard asynchronous format by adding control and error detection bits to the original byte. The communication transmitter thus takes the parallel ASCII keycodes out of the keycode buffer, converts them to serial form, and delivers them to the EIA interface.

6.3.11 Communication Receiver

Data that the host sends to the terminal enters the communication receiver, which is the other half of the PUSART. The PUSART accepts serial data from the interface and converts it to parallel form. The PUSART also checks for errors and records them in a status byte. The microprocessor reads the data and then the status byte to confirm the correctness of the data. If an error is detected, a checkerboard is displayed on the screen instead of a character. If the microprocessor is busy managing the display, it devotes only enough time to the communication receiver to get the incoming code and check it for special codes requiring immediate action.

6.3.12 Silo

The rest of the incoming codes are stored in a part of RAM memory called a silo. This memory maintains the order of the data as it arrives; the first data to arrive leaves first. This memory gives incoming data a place to wait when the microprocessor cannot transfer data from the communication receiver to the screen RAM as fast as it arrives. The silo control routine checks the filling of the silo and can issue XON and XOFF commands to the host to try to keep from overfilling.

In local mode, data from the keyboard bypasses the communication receiver and transmitter and the silo.

6.3.13 Control Function Parser

When the microprocessor has enough time, it takes data from the silo and puts it through a control function parser routine in the microprocessor. Each code is tested to see if it is in the control range (<20H or 7FH). If it is, the microprocessor acts on it immediately. Line feed, for example, causes a one line scroll. If the code is 1BH (escape), more codes are read from the silo until the characters that define a control function are seen. Then the microprocessor executes the control function immediately or discards it if it is not a valid function. Noncontrol codes are recognized by the parser and are immediately written directly into the screen RAM.

6.3.14 Screen RAM

The screen RAM is a memory that stores data for display on the screen (CRT monitor). The memory is organized according to the set-up line length specifications. Basic terminal memory can hold 24 lines of 80 characters or 14 lines of 132 characters. With the extra memory provided by the advanced video option, the screen size may increase to 24 lines of 132 characters and four additional bits are appended to each character location to allow expanded character attributes. A character attribute modifies the display of that character relative to the preset values for the entire screen (that is, blinking, underline, etc.).

Most of the time the microprocessor can write to or read from the screen RAM. About 10 percent of the time, during the first scan of each 10 scan lines of characters, the video processor overrides the microprocessor and takes full control of the screen RAM, providing its own addresses to access the memory. This complete control of memory by a device other than the microprocessor, which is normally in control, is called a direct memory access (DMA). The DMA allows fast access of data in memory because the microprocessor does not have to perform all the steps of addressing, reading, and writing to a destination. The video processor needs the fast access because the data rate required to display a line of characters on the CRT is greater than the microprocessor can handle.

6.3.15 Video Processor

The microprocessor puts displayable data in the screen RAM. The video processor direct memory accesses (DMAs) data a line at a time from the RAM. It converts the ASCII-encoded data into streams of pulses that, when converted to light on a CRT screen, appear to form characters on the screen. Custom ICs provide the complex timing and control signals required for this conversion. The video processor can be programmed by the user to perform the conversion at different rates (called refresh rates) to minimize flicker at different power line frequencies. A number of other aspects of video processor operation can be programmed as well.

6.3.16 CRT Monitor

The cathode ray tube (CRT) monitor is a simplified, monochrome television set. It converts electrical pulse streams into dots of light by using a moving electron beam to excite a phosphor on the face of the tube. A video input from the video processor enters a cathode drive circuit that regulates the strength of the electron beam. The cathode driver is a linear amplifier that allows the CRT to display different intensities (gray scale). The monitor uses timing pulses from the video processor to drive the horizontal and vertical electron beam deflection circuits. These circuits cause the beam to travel down the screen slowly while rapidly moving sideways to draw horizontal traces called scans. This beam movement produces a pattern that is called a raster; the display system is called raster scanning. Because the beam repeatedly passes by each location on the screen, the video processor, synchronizing its output with the motion of the beam, makes rows of dots of light align forming characters.

The screen does not hold its image after the electron beam has painted dots on it. For the eye to perceive it as continuously illuminated (that is, without flickering) the screen must be repainted, or refreshed, repeatedly – some 30 or more times per second. Stray magnetic fields and electrical noise at the power line frequency can also cause distortions in the display. If the refresh frequency is different from the power line frequency, the distortions appear to move up or down the display. This is very noticeable. Most distortions disappear by matching the refresh rate to the power line frequency. The VT100 can refresh at either of the two world power frequencies, 50 Hz or 60 Hz, satisfying both flicker and distortion requirements. (Refresh is not locked to the power line but is close enough to conceal most distortions.)

The CRT monitor, the monitor circuit board, and the flyback transformer are replaceable subunits of the basic VT100.

6.3.17 Power Supply

The power supply provides enough power to run the basic terminal and a few options. It is a switching-type power supply to allow highest efficiency and to minimize the heat load on the rest of the terminal. It rectifies line voltage directly (without a transformer) and uses a transistor to chop the resulting high dc voltage to about 30 kilohertz. This ultrasonic ac is stepped down in a relatively tiny transformer and then regulated at low voltage to give the various outputs. The power supply is a replaceable subunit of the basic VT100.

6.3.18 Standard Terminal Port

The standard terminal port (STP) is a shorting connector in series with the communications port, the modem control lines, and some power and timing lines. By connecting to the terminal through this port, options can exchange signals with the terminal controller or intercept terminal host communications from inside the terminal cabinet.

6.3.19 EIA Drivers and Receivers

The Electronic Industries Association (EIA) interface used on the terminal controller module is the RS-232-C unbalanced bipolar voltage standard. The terminal controller has two types of ICs that provide conversion between EIA levels and the TTL levels used on the controller board. One IC is a line driver that outputs EIA levels for TTL inputs, and the other is a receiver that senses the EIA levels on the input line and converts them to TTL.

6.4 FIRMWARE INTRODUCTION

Figure 6-3 portrays the basic VT100 as a system with four levels of operation.

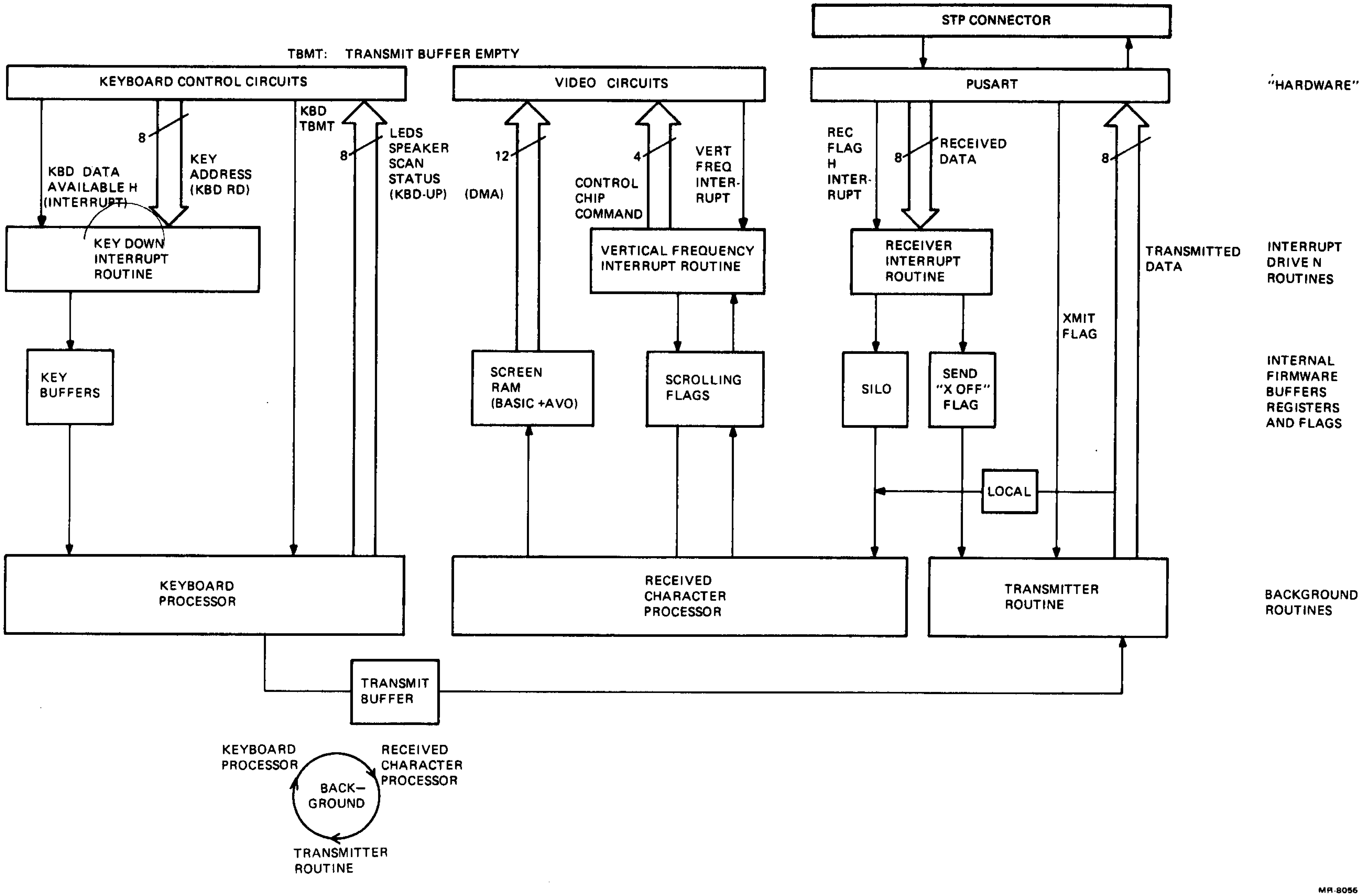


Figure 6-3 VT100 Firmware Block Diagram

At the deepest level, the background routines continually repeat in order to manage functions that do not require precisely timed responses. The keyboard processor commands the keyboard to perform address scans, controls the bell and LEDs, and manages the conversion of key information from hardware-dependent codes to ASCII. The transmitter routine manages the transmission of ASCII data to the host. The received character processor examines incoming data, manages the silo, initiates special functions as specified in the data, and writes displayable data into the screen RAM. When the terminal is in local mode, a logical shortcut bypasses the communication process and allows the keyboard data to enter the received character processor directly.

The background routines work on the internal buffers, registers, and flags, which are logical devices located in hardware and RAM. These are physical locations in hardware that contain information placed there by the hardware and by the firmware. The key buffers store up to three key addresses for the keyboard processor to pass through the transmit buffer to the transmitter routine for transmission to the host or CP/M processor. The screen RAM, which stores the displayable data, is the largest segment of RAM. The scrolling flags contain data for the scrolling process in the video processor. The silo stores data coming from the host in case the received character processor cannot transfer data to the screen RAM as fast as it arrives. The send XOFF flag, set by the silo manager, signals the transmitter routine to send the XOFF code to the host to halt transmission and prevent silo overflow.

Interrupt routines are segments of the firmware that take precedence over other business in the microprocessor because of the short-lived nature of the data that they handle. The key down interrupt routine is initiated by the appearance of data at the keyboard control circuits. It instructs the microprocessor to get the key address from the keyboard UART and put it in the key buffer. The vertical frequency interrupt routine occurs every fiftieth or sixtieth of a second and provides synchronization of video routines with the actual display timing. The receiver interrupt routine moves incoming data from the communication transceiver to the silo.

At the exterior level of the VT100 system, the hardware responds to the firmware by exchanging data between the user and the host computer or CP/M processor in forms that are understandable to each.

6.5 TERMINAL CONTROLLER DESCRIPTION

The 8080 microprocessor residing on the terminal controller module controls all of the basic VT100 functions. The 8080 performs all of the usual functions of a stored program computer, fetching instructions and data from ROM and RAM and responding to service requests from various devices in the system. Because of technical limitations in the implementation of the microprocessor hardware, some high-speed counting and timing circuits and some power circuits are located in peripheral ICs made with a different semiconductor technology. These components are bipolar (8224, 8228) while the 8080 is NMOS.

6.5.1 8080 Microprocessor

The 8080 (Figure 6-4) contains a set of general and special purpose registers (the register array), timing and control logic that responds to machine code instructions, and an accumulator and arithmetic logic unit that perform the computations associated with the microprocessor operation.

The stack pointer is an important register that points to the bottom of the stack. The stack is a last-in/first-out area in RAM that stores information about the current process when a subroutine or interrupt branches away from the current instruction sequence. By storing this information at the beginning of an interruption and restoring it at the end of the interruption, the 8080 can continue the main program without any disturbance. This is the meaning of the interrupt process as it applies to the interrupt-driven routines mentioned in the firmware block diagram in Figure 6-3.

Most of the pins on the 8080 are tristate data and address lines. Four pins are power supplies and ground. Descriptions of the others follow.

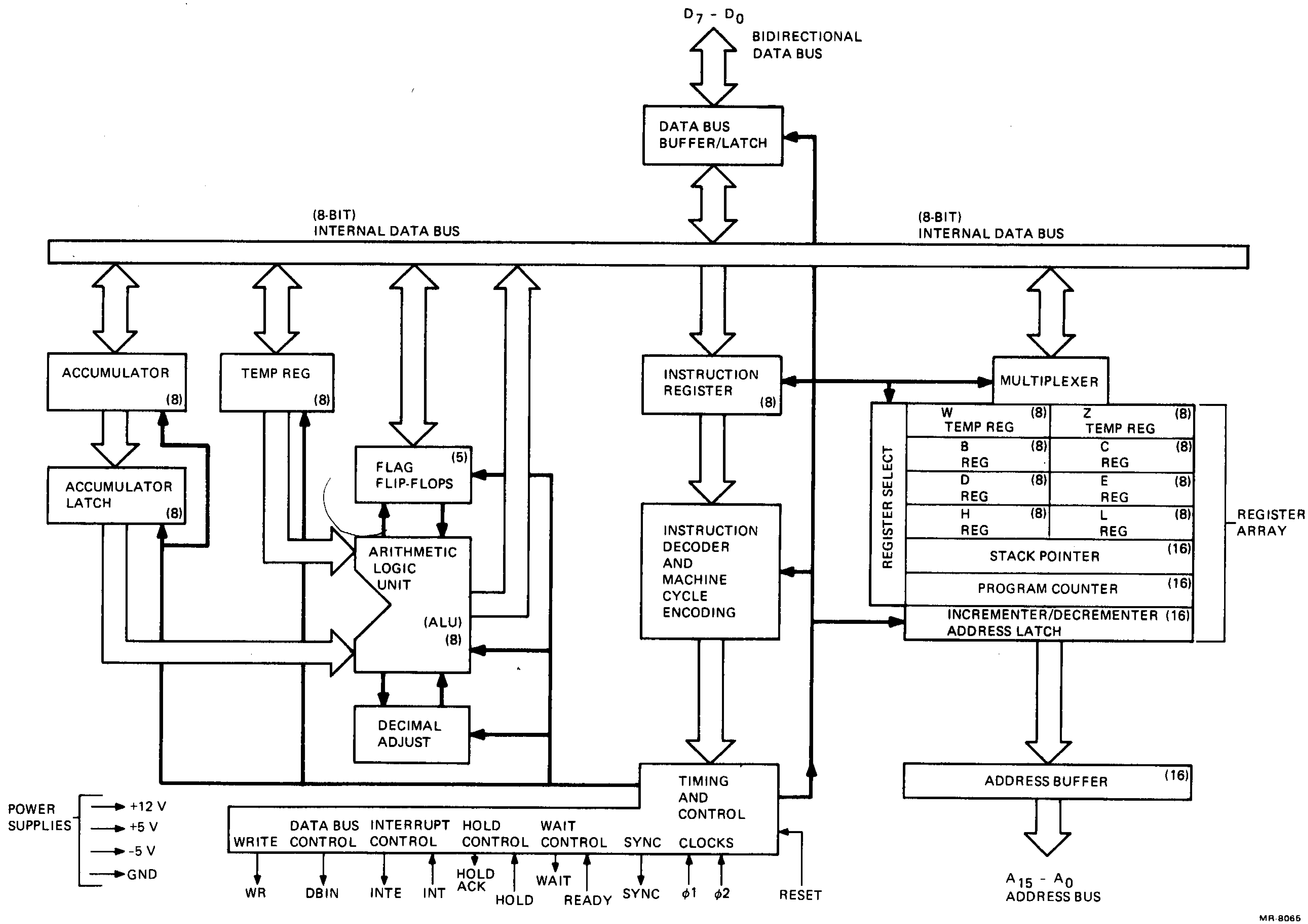


Figure 6-4 Microprocessor Block Diagram

HOLD is an input that lets another device get control of the buses when the 8080 finishes the current machine cycle. Hold request from the video processor is the input signal.

HLDA (hold acknowledge) output indicates that the buses will be given up for the hold state.

INT (interrupt request) input accepts an INTR H signal that causes a read of the interrupt vector address and a branch to it.

READY is input for use with slow memory or I/O. If low, the 8080 enters the wait state (an indefinite portion of a machine cycle). It is not used in the VT100.

WAIT is output acknowledging the wait state. It is not used by the VT100.

INTE (interrupt enable) output indicates whether interrupts have been enabled or disabled with the related instructions or by servicing an interrupt request. It is not used by the VT100.

0/1, 0/2 are clock phases 1 and 2. These are inputs to drive the 8080.

SYNC is output that indicates the beginning of each machine cycle. It combines with the clock in the 8224 to produce status strobe (STSTB).

RESET clears the program counter so that when it is released, the program starts at location zero. It is used to initiate the power-up sequence and self-test.

WR (write) output controls memory and I/O writes by indicating the stable period of the data bus during a write instruction.

DBIN (data bus in) output indicates that the data bus can accept data.

For more detail, see Intel Corporation's 8080A manual.

6.5.2 Data Bus and System Controller

The microprocessor data bus passes directly to the 8228 bus driver and system controller. This device provides TTL output buffering and level translation for the MOS 8080 bus. Because of the large number of devices on the data bus, the drive capability of some devices would be exceeded at times if all devices were on the same bus. (The keyboard UART is the weakest low-level current driver.) To distribute the load, the bus is split into those devices that communicate bidirectionally or are only read by the microprocessor and those that are only written into. Read and writable devices are on the bidirectional data bus (DB). The write-only devices are driven by a one-way bus buffer and are on the data output (DO) bus. The terminal controller block diagram (Figure 6-5) shows which devices are on each bus.

The ROMs do not have sufficient high-level current capacity to drive all of the other inputs on the bus. Inactive devices have their outputs tristated, but their inputs still draw enough current to accumulate a significant load over the entire bus. Pull-up resistors are connected to the bus to provide the additional current required. Their resistance is selected to supply enough current to meet high-level needs on the bus without exceeding the low-level sink capacity of any driving device.

Pull-up resistors are used on the output-only DO bus because the baud rate generator, a MOS device, has an input threshold higher than TTL driver E58 is guaranteed to deliver. Pull-up resistors ensure that the data lines rise enough.

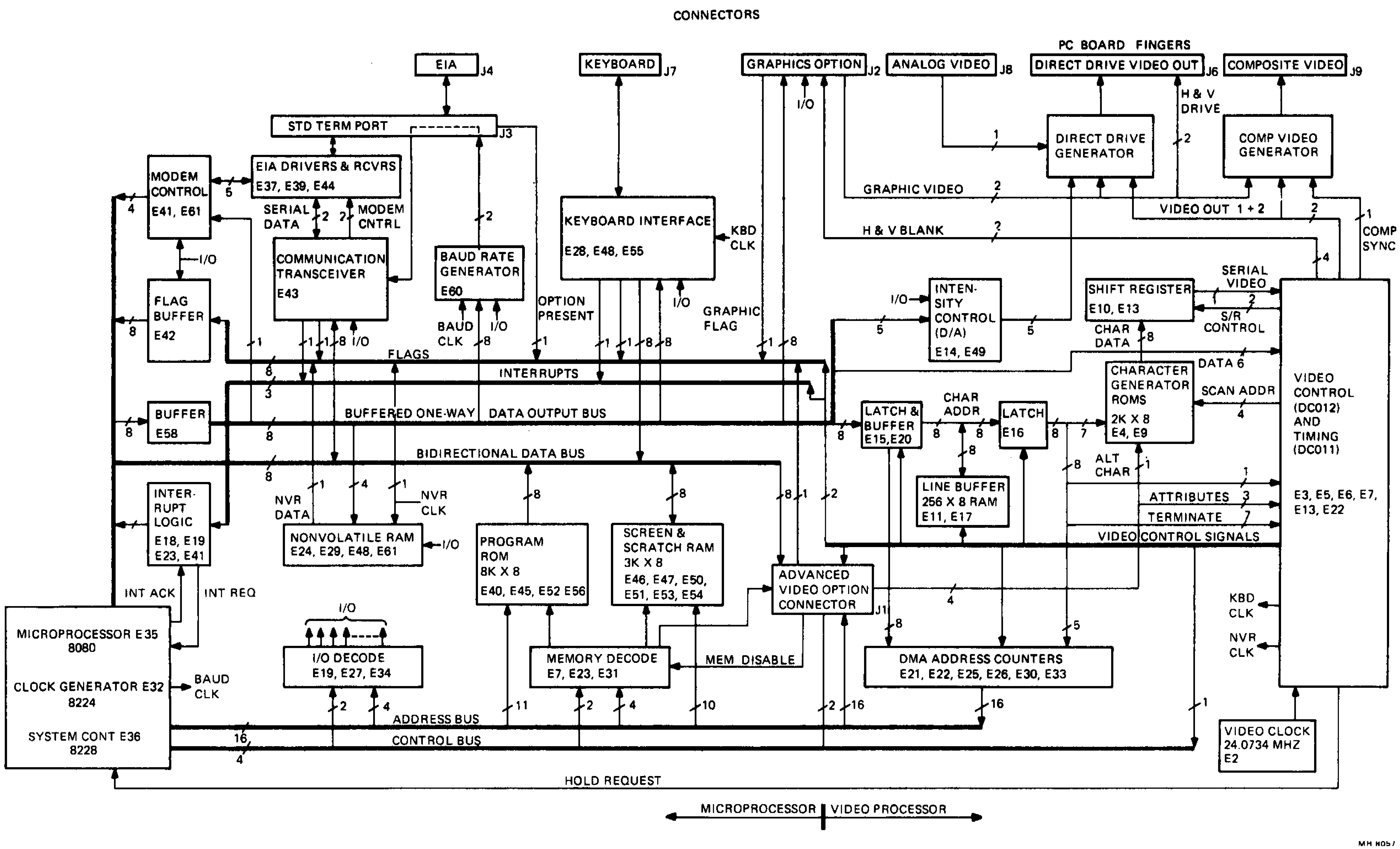


Figure 6-5 Terminal Controller Block Diagram

An additional function of the 8228 is a combination logic decode of the 8080 status byte. This byte, output by the 8080 at the beginning of each machine cycle, contains flag bits indicating the nature and function of the cycle. The byte is latched into the 8228 by the status strobe (STSTB) signal from the clock generator. In combination with three control output bits from the 8080, the system controller produces interrupt acknowledge (INTA), memory read and write (MEM WR,RD), and input/output read and write (I/O WR,RD). These signals reduce the external decoding requirements while saving pins on the 8080 package.

When the video processor asserts hold request during a direct memory access (DMA) of the screen RAM, the 8228 floats its outputs. Since these include the memory control signals, the video processor must provide its own memory control. The DMA enable signal, buffered into the MEM RD line by gate E28 (pin 13), provides memory read enabling during the DMA. The other control signals are pulled high by the pull-up resistors.

6.5.3 Clock Generator

The 8224 provides the asymmetrical two-phase clock required by the 8080 logic. Its running frequency is crystal-controlled. An LC circuit on the tank input improves the crystal's mode stability. The capacitor in series with the crystal compensates for internal phase shifts in the 8224 at the high operating frequency. The 24.8832 MHz crystal frequency gets divided by 9 to produce a 361.69 ns clock period. The buffered TTL phase 2 output clocks the PUSART and the baud rate generator. The system clock period for the microprocessor is 361.69 ns.

The sync signal from the 8080 combines with an internal clock phase to produce the status strobe (STSTB) during the last ninth of the first state of each machine cycle. STSTB latches the status byte into the 8228 system controller.

The ready input is not used in the VT100. It is an asynchronous input that gets synchronized to the machine cycles in the 8224. The synchronized signal can cause the microprocessor to enter a wait state during a memory access to wait for slow memory to respond. Memory used in the VT100 matches the processor speed so ready is not used.

The reset input is a Schmitt trigger. Its input is the +5 volt supply delayed by an RC circuit with a diode bypass for fast discharge. The reset input is held low until well after all power supplies have settled. When the capacitor voltage reaches the Schmitt threshold, reset is released and the microprocessor begins operation at memory location 0 (the start of the firmware ROM). The inverted and noninverted reset signals clear other portions of the terminal controller.

6.5.4 Bus Timing

The bus timing diagram in Figure 6-6 illustrates the basic time relations between the address, data, and control lines in the microprocessor system. The figure distinguishes between write and read cycles, with the exception of the three top lines. These show the constants of the system: the two clock phases from which all timing is derived, and the address bus that always provides the current address for either kind of cycle early in the cycle. Numbers on the diagram represent specified minimum/maximum nanoseconds between signals for normal operation.

Starting with the write cycle, note that the status strobe signal (STSTB L) shown in the read section occurs at the same point in the write cycle. Therefore, the status strobe latches the status byte into the 8228 during the first clock cycle. The 8228 delivers the decoded memory write L or I/O write L (MEMW or IOW) signals in the third clock cycle when data to be written is stable. The 8080 data bus, DB bus, and DO bus graphs show the propagation delays between the three buses. The 8080 bus is the output pins on the chip. The DB bus is the output of the buffered 8228 bidirectional bus, and the DO bus is the unidirectional buffered output-only bus.

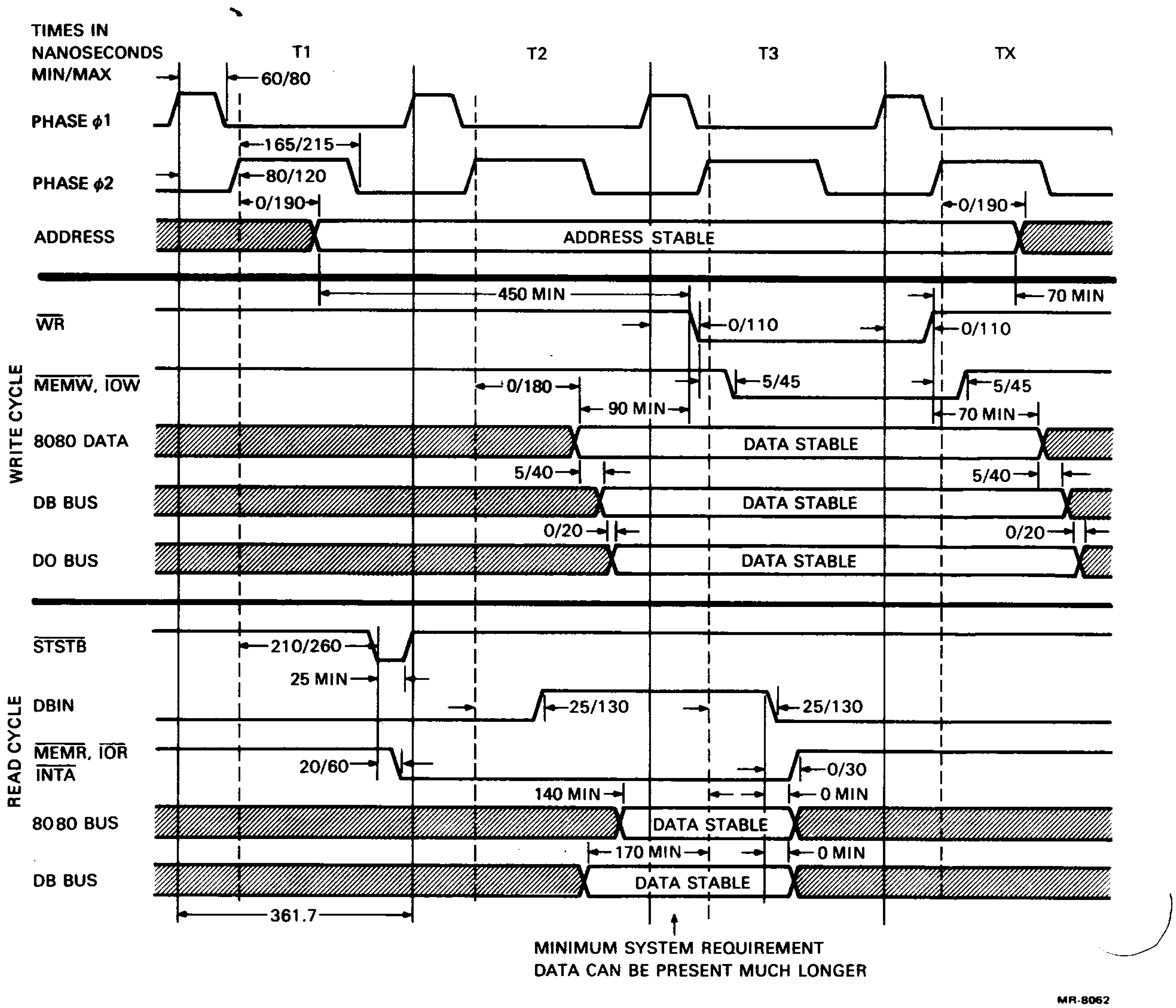


Figure 6-6 Microprocessor Bus Timing

In the read cycle, the memory read L signal (along with I/O read L and interrupt acknowledge L: MEMR, IOR, INTA) starts early to enable the chip selects and allow the data buses to stabilize. Data bus in (DBIN) goes high before data settles but does not latch data into the 8080 until its falling edge, when data is settled. The two bus graphs show the assertion of stable data and also show the delay through the bidirectional bus buffer to the 8080 data bus.

6.5.5 Microprocessor Memory

The basic terminal controller contains 8192 bytes (8K bytes) of program ROM and 3072 bytes (3K bytes) of static RAM. (One byte equals eight bits.) The original board utilizes four 2K by 8 ROM ICs; later versions may use a single 8K by 8 ROM. The RAM is six 1K by 4 ICs arranged in pairs. The microprocessor can address up to 64K memory locations. Some of these locations are reserved for future expansion. The memory map of Table 6-1 shows the portions of addressable space that are reserved as well as those areas that are available for new applications.

Table 6-1 ROM and RAM Memory Map

K Bytes	Address (Hex)	Description		Physical Location
0	0000	8K × 8	Basic ROM	TCB*
	1FFF			
8	2000	3K × 8	Screen and scratch RAM	TCB*
	2BFF			
11	2C00	1K × 8	AVO screen RAM	AVO**
	2FFF			
12	3000	4K × 4	Attribute RAM	AVO**
	3FFF			
16	4000	16K × 8	Unassigned	
	7FFF			
32	8000	2K × 8 2K × 8 2K × 8 2K × 8	Program memory expansion (use 2K × 8 ROM/EPROM)	AVO**
	9FFF			
40	A000	8K × 8 8K × 8	Program memory expansion (use 8K × 8 ROM)	AVO**
	BFFF			
48	C000	16K × 8	Unassigned	
	FFFF			
64				

*TCB = Terminal controller board
**AVO = Advanced video option

6.5.5.1 Memory Map – The basic terminal controller board contains 8K bytes of program ROM and 3K bytes of screen and scratch RAM. These account for the locations from 0000H to 2BFFH in memory. The advanced video option adds another 1K byte of RAM (2C00H to 2FFFH) to increase the number of characters that can be displayed. The AVO also contains additional memory for character attributes. This memory is only 4 bits wide, but to address each location in correspondence with each of the 4K characters, it uses another 4K of addresses from 3000H to 3FFFH.

The next 16K locations (4000H to 7FFFH) are unassigned. However, 4000H to 4FFFH can be addressed by the video processor using the DMA address counters, so 4000H to 4FFFH could be used for additional screen RAM with 5000H to 5FFFH as associated attribute storage.

Above 7FFFH is an 8K area intended for additions or changes to the program ROM in 2K segments, and above that is an area intended for the same purpose but in one 8K segment. The top 16K are unassigned.

6.5.5.2 Memory Devices – Each ROM has three ANDed chip select inputs that are mask-programmed to be either active-high or active-low. This eliminates the need for external inverters. The two address lines, A11 and A12, are decoded to select one of four ROMs. The third chip select line is common to all four ROMs. In later VT100s, jumpers W2 and W3 can be used to select either a high or low assertion for this single chip select to allow for 64K ROMs that do not have a programmable chip select. Table 6-2 shows the addressing of the ROMs.

Table 6-2 ROM Chip Select Addressing

Address Line 11	Address Line 12	Chip Select 2	Chip Select 3	ROM Selected
0	0	Active low	Active low	1
1	0	Active high	Active low	2
0	1	Active low	Active high	3
1	1	Active high	Active high	4

6.5.5.3 ROM Decoding – The program ROM is enabled when the top half of memory decoder E31 is enabled and the correct address space is requested by the microprocessor. MEM RD or MEM WR from the 8228, in the absence of MEM DISABLE, enables the decoder. The ROM is in addresses 0H to 1FFFH, so A13 (the 8K bit) is not asserted during ROM reads. Bit A12 is low or high for 0–4K or 4–8K sections of ROM. The decoded outputs from both states are ORed to provide one of the select signals for the ROM. Then bits A11 and A12 at two of the chip select lines enable the outputs in one of the 2K segments. The low 11 bits address one of the 2K bytes in the enabled ROM. If the program is in one 8K ROM, A11 and A12 are used as regular address lines; only one chip select line enables its outputs.

6.5.5.4 RAM Decoding – If A13 is asserted, the memory space between 2000H and 3FFFH is being addressed. The ROM outputs are disabled and the decoded output from the top half of the decoder enables the bottom half. Now bits A10 and A11 are decoded to select 1K segments of the screen RAM. The 1K by 4 RAMs are paralleled in pairs to make each location eight bits wide. There is 3K on the basic video board. The fourth 1K is located on the AVO; its addressing is decoded separately.

6.5.5.5 Memory Disable – Memory disable turns off all memory on the terminal controller board. It is used by options that plug into the advanced video option connector:

1. To replace (overlay) existing memory

2. To disable the terminal controller memory when using memory above 4000H (since the terminal controller does not decode A14, A15).

The advanced video option can contain overlaying program memory. This is a set of address locations and the AVO can be jumper programmed to decode and provide data for these locations. Since the main memory may also be decoding the same location, the AVO must assert MEM DISABLE to disable the main memory (ROM and RAM) so that only one data byte is asserted on the bus.

6.5.6 I/O Decoding

The I/O address space is divided into two regions. One contains the 8251 PUSART and has address bit A01 always low; the other region contains all other I/O devices and has bit A01 always high. The list of I/O addresses in Table 6-3 illustrates this by the presence of hex 2 in the low half of each non-PUSART address byte.

Table 6-3 List of Hex I/O Addresses

Address	Device
Read or write	
00H	PUSART data bus
01H	PUSART command port
Write-only (decoded with I/O WR L)	
02H	Baud rate generator
42H	Brightness D/A latch
62H	NVR latch
82H	Keyboard UART data input
A2H	Video processor DC012
C2H	Video processor DC011
Read-only (decoded with I/O RD L)	
22H	Modem buffer
42H	Flags buffer
82H	Keyboard UART data output

6.5.6.1 PUSART Read and Write – When bit A01 is low, the PUSART is enabled. The I/O RD and WR signals from the 8228 control the read or write operation. Address bit A00 selects either the command or data register for the I/O operation.

6.5.6.2 I/O Read and Write – When bit A01 is high, the PUSART is disabled. Bit A01 high is one of two signals required to enable the I/O write decoder (E27). I/O WR is the other signal. Address bits A05, A06, and A07 select one of the seven writable I/O devices. These are the baud rate generator, the brightness control D/A latch, the NVR latch, the keyboard UART transmit buffer, the DC011 video timing chip (E6), and the DC012 video control chip (E5).

Only three I/O devices are readable, so their addresses were chosen to allow read decoding directly from the three address lines. When the 8228 asserts I/O RD, I/O WR deasserts and decoder E27 is disabled. I/O RD enables the gates in E34 to allow reading of the keyboard UART receive buffer, the flag buffer, or the modem control signal buffer, depending on which address bit is asserted.

6.5.7 Interrupt Vector

When any of the three interrupting devices (communication receiver, vertical frequency, or keyboard) sets interrupt request (INTR H) through gate E23, the current instruction is completed. Then the microprocessor sets its interrupt acknowledge (INTA) status bit and performs an instruction fetch. The address requested in the fetch is the contents of the program counter. Its value is ignored in the interrupt process, but it is not incremented as it would be in a normal fetch cycle. The INTA bit is decoded from the status word in the 8228 system controller; it enables the tristate interrupt vector buffer (E41), which then presents a restart (RST) instruction to the data bus. Main memory does not conflict with the vector buffer because the 8228, in decoding the interrupt status word, does not produce the memory read or write command bits needed for address decoding. (Refer to Table 6-4.)

Table 6-4 Interrupt Addresses

Address (Hex)	Interrupting Device
00H	Power-up (not hardware driven)
08H	Keyboard
10H	Receiver
18H	Receiver and keyboard
20H	Vertical frequency
28H	Vertical frequency and keyboard
30H	Vertical frequency and receiver
38H	Vertical frequency, receiver, and keyboard

The RST instruction disables further interrupts, pushes the current program counter contents (the location of the next instruction in the interrupted program) onto the stack, and decrements the stack pointer. Then the program counter is loaded with the bits in the address field of the RST instruction. This field is produced by the interrupt signals of the interrupting devices. The signals are passed onto the data bus as bits in the address field (bits 3, 4, and 5). The rest of the instruction is hardwired through diodes that supply high level to the other data bits during INTA and that are reverse-biased to isolate these data bus lines when the vector buffer is inactive.

The RST address field, when mapped into the same bit locations in the program counter, defines a set of eight 8-byte long memory spaces at the beginning of the memory. The first address, 0, is the starting point for the terminal controller program and is not used for interrupts. The program is normally started by a hardware reset signal that sets the program counter to 0. It can also be started by an escape sequence that the host can send to force the program to jump to zero, or in set-up mode the RESET key can be pressed. The other seven memory spaces, starting at 8, 16, etc., contain jumps to places in an interrupt handling routine that can mediate requests for service from any of the seven combinations of interrupting devices.

At the end of the interrupt service routine, the stack is popped, interrupts are enabled, and the interrupted program continues.

Early VT100s can disable the receiver interrupt by programming D4 in the NVR latch. However, this is never used by the VT180. Later VT100s have the ability to add a communications transmit buffer empty interrupt by adding W6. The 8080 would then have to distinguish transmit and receive interrupts by testing the transmit flag on the flag buffer. This provision is not used on the VT180.

6.5.8 Communication Transceiver

The terminal controller module interfaces to the CP/M processor or host computer through the standard terminal port (STP) connector. An 8251 programmable universal asynchronous receiver-transmitter (PUSART), illustrated in Figure 6-7, drives the STP port. This device takes parallel data from the transmit buffer on the terminal control module, converts the parallel data to a serial format, and transmits the data through the STP connector. Data from the CP/M processor or host computer is received in serial format by the PUSART, converted to parallel data, and sent to the silo for processing. Three kinds of data can be exchanged between the basic VT100 and the CP/M processor or host computer: control characters, control functions, and displayable characters.

PUSART clocks are derived from the microprocessor clock. The microprocessor clock crystal was selected to provide a frequency within the limits of the 8080 that could be readily divided to provide standard baud rates. The division occurs in programmable baud rate generator E60 (see Figure 6-5). This device contains two independent counters that allow different receive and transmit baud rates (split baud rates). Each counter has 4 input lines to select 1 of 16 rates. Thus, a 1-byte load into the device can set up both send (transmit clock) and receive (receive clock) rates. The baud rate generator's input register is written into as a device in the I/O address space.

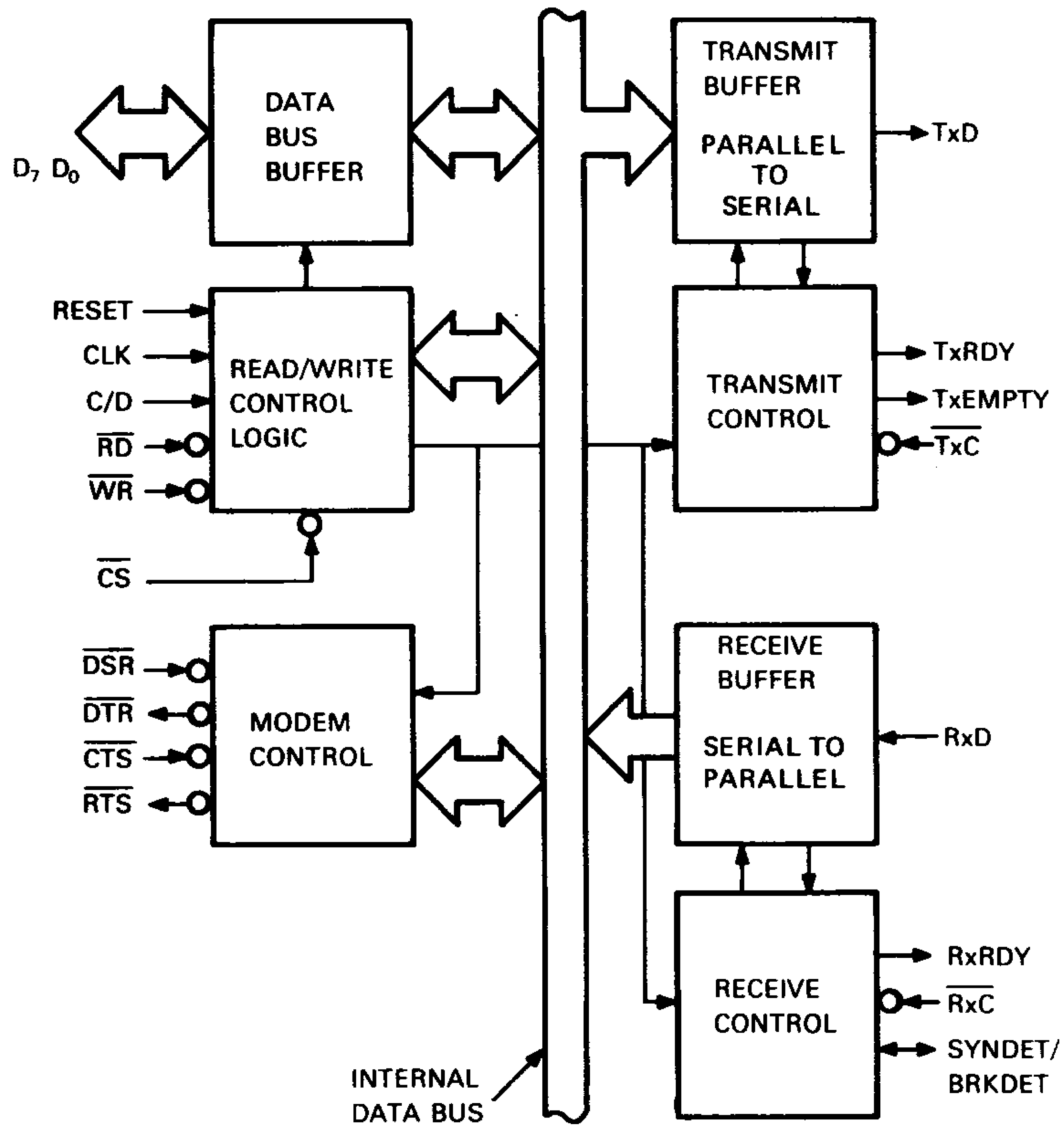
The baud rate generator E60 is factory mask-programmed with the division ratios required to get standard baud rates from the crystal frequency. The 4-bit input is an address for a ROM location containing the set-up information for each rate. The outputs of the baud rate generator are sent to the PUSART as the transmitter (TxC) and receiver (RxC) clock signals.

Certain pins on the PUSART are labeled with standard modem control designations. These pins are readable [data set ready (DSR)] or writable [data terminal ready (DTR) and request to send (RTS)] as buffered bits in the PUSART's status and control bytes. Other signals from the modem pass through EIA level translators with Schmitt trigger inputs to a tristate buffer that, when enabled by the MODEM RD command, presents them to the data bus. Another signal [speed select (SPDS)] is written from the data bus into the NVR latch, which is a convenient extra latch position. None of these signals are used to support modem control in the basic VT100. See Chapter 3 for more interface information.

6.5.8.1 Data Transmission – When the microprocessor wants to send a character out, it checks the XMIT flag at the flag buffer. If this flag is high, the transmit buffer is empty and can accept data. If the flag is low, the microprocessor continues through its background program and returns to check again later.

When the flag is high, the microprocessor loads a data byte into the transmit buffer. The PUSART is double-buffered; this means that there is a second data buffer inside that is automatically loaded from the first buffer. The second buffer's contents get start and stop bits and parity (if enabled) appended and are shifted out by the continuously running clock. Immediately after the second buffer is loaded, the transmit flag goes high and the first (transmit) buffer can be loaded again.

6.5.8.2 Data Reception – Any data that appears on the receive data line is shifted into the internal receive shifting buffer. When a full character of bits has arrived, the start, stop, and parity bits are stripped. Parity is checked, and if bad, the parity error flag in the status word is set. Data is transferred to the receive data buffer, and the receive flag is set. This flag requests an interrupt from the microprocesor. The microprocessor then has the amount of time it takes the next character to shift in, to read the first character. After reading the character, the microprocessor reads the status byte to check the integrity of the data. If the microprocessor does not read the receive data buffer in time, the second character writes over the first one. The first character is lost and an overrun error is reported in the status word. The checkerboard character appears on the screen for all errors.



PIN NAME	PIN FUNCTION
D_7 D_0	DATA BUS (8 BITS)
C/$\overline{D}$	CONTROL OR DATA IS TO BE WRITTEN OR READ
$\overline{RD}$	READ DATA COMMAND
$\overline{WR}$	WRITE DATA OR CONTROL COMMAND
$\overline{CS}$	CHIP SELECT
CLK	CLOCK PULSE (TTL)
RESET	RESET
$\overline{TxC}$	TRANSMITTER CLOCK
TxD	TRANSMITTER DATA
$\overline{RxC}$	RECEIVER CLOCK
RxD	RECEIVER DATA
RxRDY	RECEIVER READY (HAS CHARACTER FOR CPU)
TxRDY	TRANSMITTER READY (READY FOR CHAR. FROM CPU)
$\overline{DSR}$	DATA SET READY
$\overline{DTR}$	DATA TERMINAL READY
SYNDET/ BRKDET	SYNC DETECT/ BREAK DETECT
$\overline{RTS}$	REQUEST TO SEND DATA
$\overline{CTS}$	CLEAR TO SEND DATA
TxEMPTY	TRANSMITTER EMPTY

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Figure 6-7 8251A PUSART Block Diagram

The microprocessor checks each received character as it comes from the PUSART. Only four characters cause any special action at this time. Control codes XON and XOFF are immediately processed while NULL and DELETE are discarded. Everything else gets put in a 64 character (128 characters in later model terminals) first-in/first-out space in the scratch area of RAM called the silo (Figure 6-2). The silo processor routine maintains this area by updating two locations called SILIN and SILOUT. After the current action is finished, the microprocessor gets the longest-waiting character out of the silo and range checks it. If it is less than 20 H, it is a control character and the microprocessor processes it. If it is 20 H or above, the microprocessor puts it in the next character position in the screen RAM.

When the VT180 is in local mode, the communications transmitter and receiver and silo are bypassed and any inputs from the keyboard are acted on immediately by the microprocessor. The data terminal ready signal (DTR) is unasserted in local mode.

6.5.8.3 PUSART Programming – The microprocessor can program the PUSART to operate with several standards and parameters. Many of these parameters are predetermined by the VT180 specifications. Character length, number of stop bits, parity enabling and format, baud rate multiplication factor, and asynchronous operation are all programmed in at power-up through the mode instruction (Figure 6-8) from the stored set-up information. Address bit A00 selects either the command register in the PUSART for writing the byte containing this information or the transmit buffer for normal operation. The programmable baud rate generator provides the selected baud rate from set-up data.

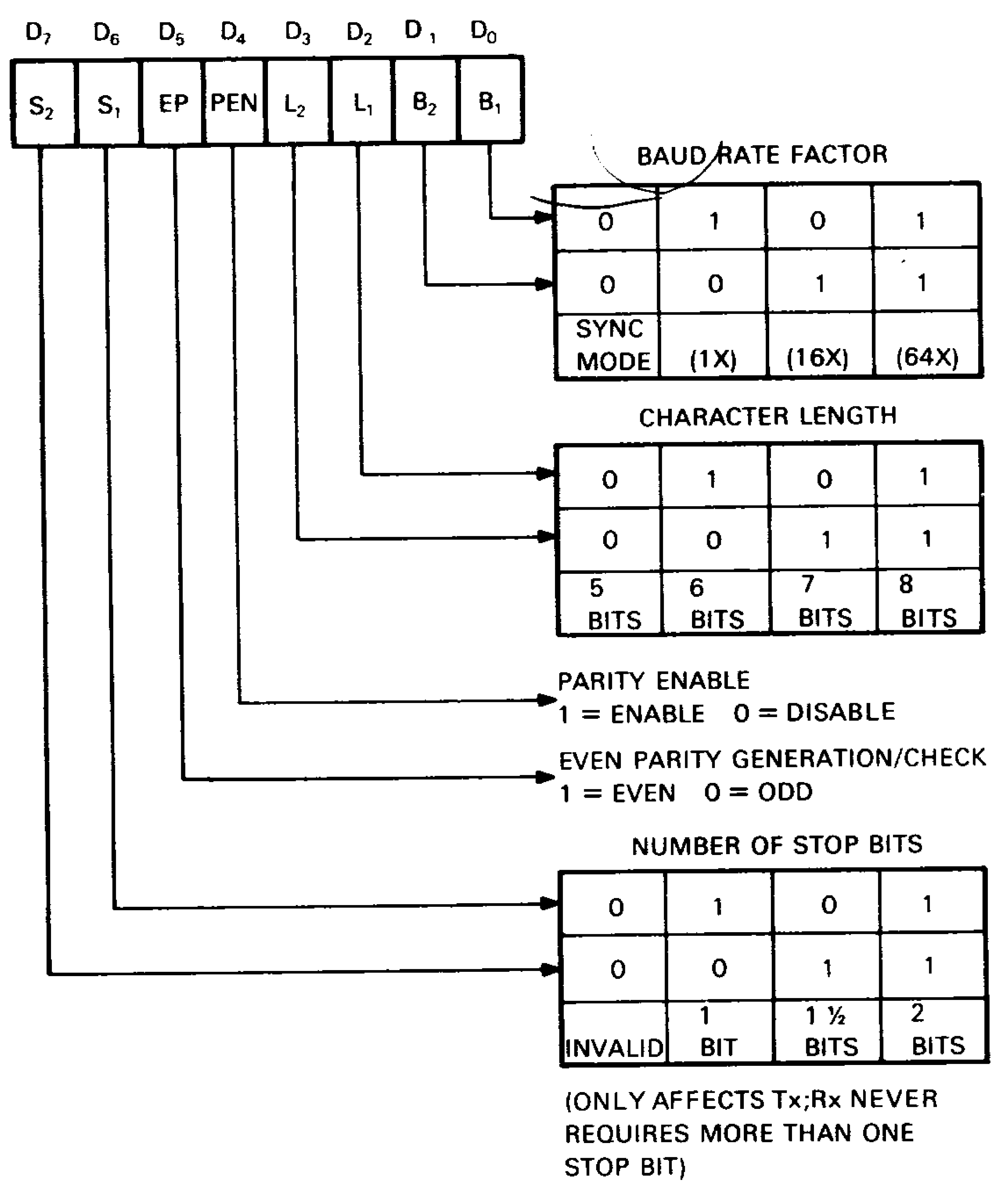


Figure 6-8 Mode Instruction

After the PUSART mode of operation is selected by writing a mode instruction, PUSART operation is controlled by writing a command instruction (Figure 6-9). Once the mode instruction has been written into the PUSART, all further control writes (C/D=1) load a command instruction. A reset operation (internal or external) returns the PUSART to the mode instruction format.

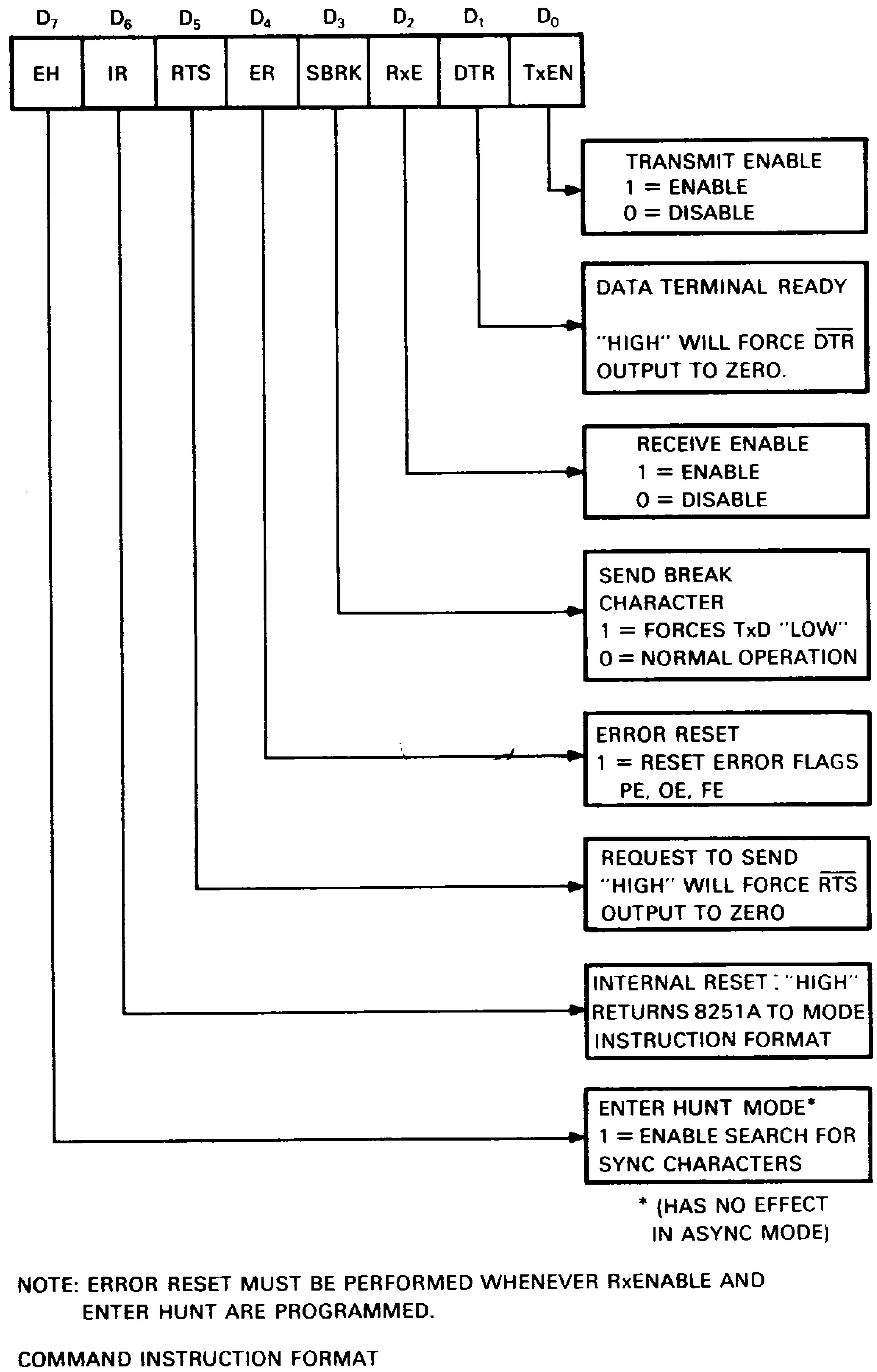


Figure 6-9 Command Instruction

The status of the PUSART can be read by the microprocessor by performing a read with C/D=1. Some of the bits in the status word (Figure 6-10) have the same meaning as output pins on the PUSART chip. The status word may be a maximum of 28 clock periods behind the event causing the update. This clock, from the microprocessor's phase 2 TTL signal, is the clock for the internal operation of the PUSART. It is a dynamic device requiring internal refresh at regular intervals.

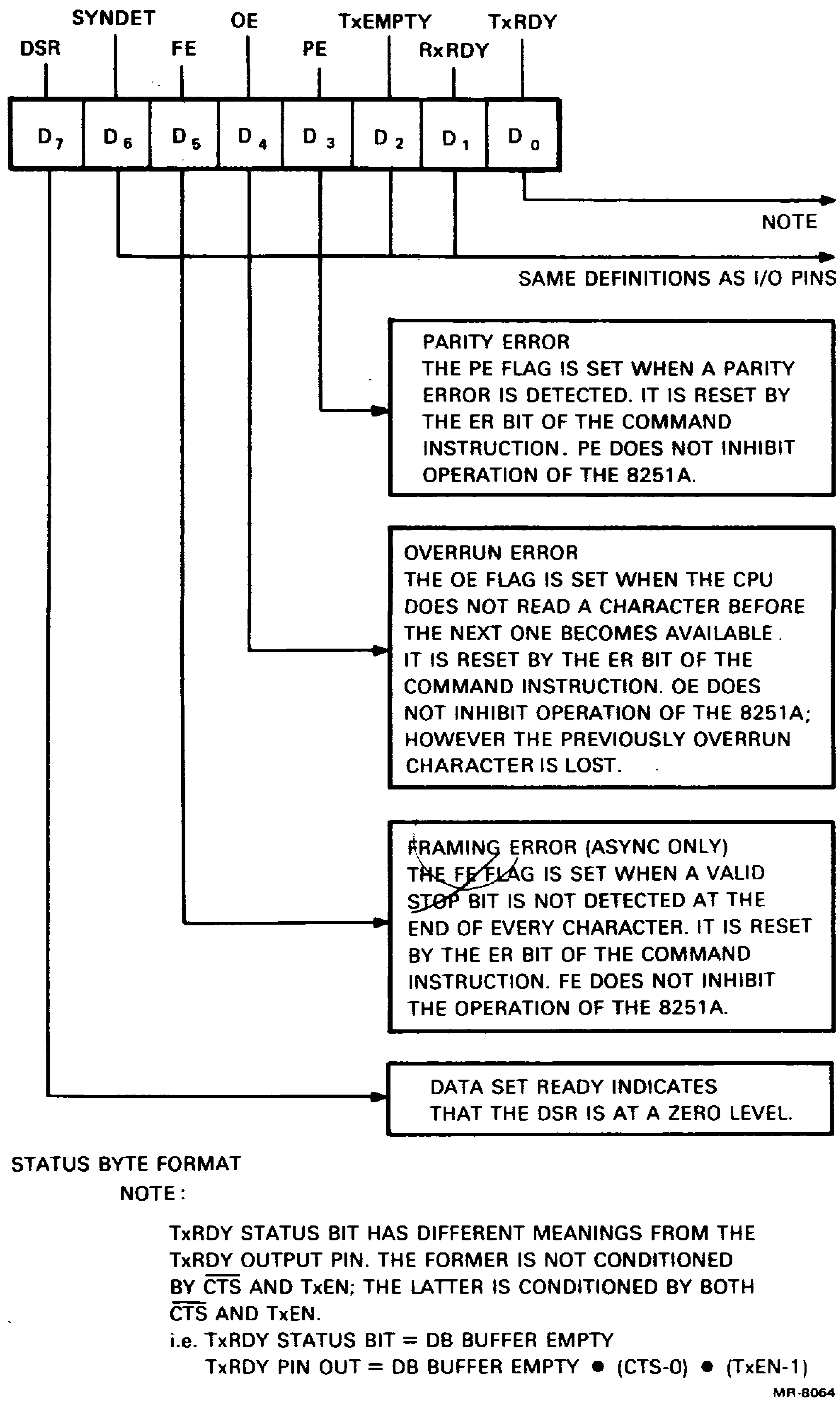


Figure 6-10 Status Byte Format

6.5.9 Standard Terminal Port

The standard terminal port (STP) is a printed circuit board edge connector on the terminal controller module that contains 20 pairs of contacts. When no board is plugged into the connector, the pairs of contacts meet. All EIA data and modem control signals plus the two baud clocks pass through this connector.

When the VT18X control module is connected to the STP connector through the ribbon cable and the VT180 paddle board, some of the EIA data and modem control signals are routed to and from the console, general purpose, and communications PUSARTs residing on the VT18X control module. The EIA data and modem control signals used by the VT18X control module are summarized in Table 6-5.

Table 6-5 EIA Data and Modem Control Signals

STP Pin	Signal	Function
2	CON REC DATA	Console received data from terminal controller PUSART
6	CON XMIT DATA	Console transmitted data to terminal controller PUSART
16	CON DTR	Console data terminal ready from terminal controller PUSART
27	CON CLK	Console operating clock (15.7 k baud) from terminal controller video processor
5	TRM REC DATA	Received data from general purpose serial port connector
8	TRM XMT DATA	Transmitted data to general purpose serial port connector
13	TRM DTR	Data terminal ready from general purpose serial port connector
28	COM TXC	Communication transmit clock from terminal controller baud rate generator
30	COM RXC	Communication receiver clock from terminal controller baud rate generator

6.5.10 Nonvolatile RAM

The nonvolatile RAM (NVR) is used to store programmable set-up information that would otherwise have to be reentered every time the power was turned on or else stored in mechanical switches.

The ER1400 (NVR) is a 1400-bit memory arranged as 100 14-bit words. Data and addresses enter or leave the device in serial form through a single bidirectional line. Information is shifted with an external clock. Identification of the meaning of the bit stream is made by setting three control lines that specify the operation in progress. The block diagram of the NVR is shown in Figure 6-11.

6.5.10.1 NVR Control – NVR operation is controlled by three data inputs derived from signals obtained from the microprocessor. Seven combinations of these three data inputs are used to specify the NVR command states. These command states determine the operation in progress and are listed in Table 6-6.

6.5.10.2 Microprocessor Management – During an NVR operation, the microprocessor uses 21 bytes of scratchpad memory to set up a group of NVR address or data bits. Each group consists of 20 bits of address or 8 bits of data with another 6 bits of fill for the 14 bit NVR word. These groups must enter the NVR serially, with precise timing. The microprocessor cannot calculate the groups fast enough to keep up with the shifting process while also managing the shifting process, so it saves time by precalculating and storing each group of bits. Then it reads the stored groups and delivers them to the NVR at the NVR clock rate through the NVR latch.

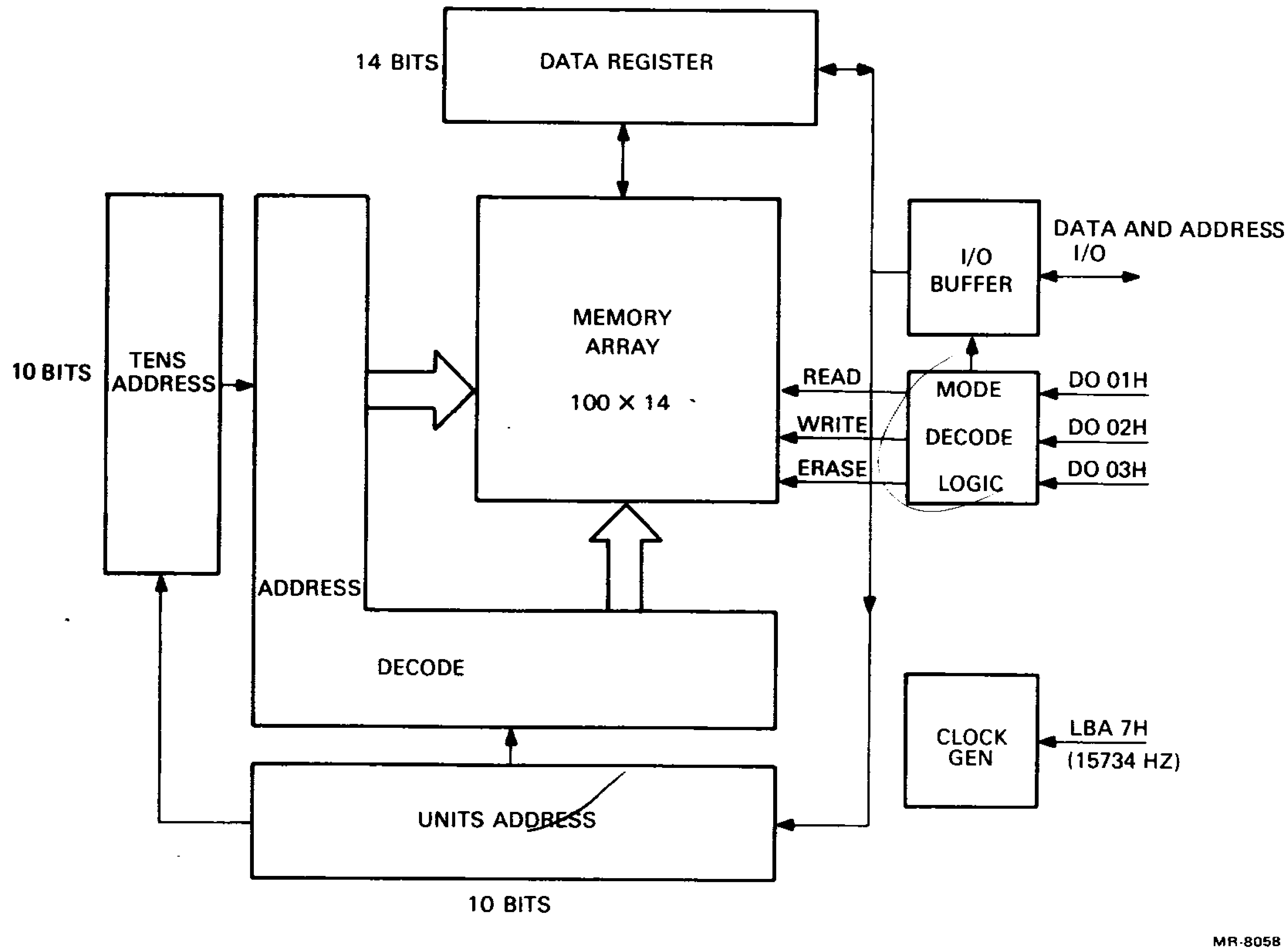


Figure 6-11 NVR Block Diagram

The microprocessor serializes its data by rotation in a register. It combines the data with command bits to control the NVR device. Output from the microprocessor reaches the NVR through an external NVR latch. The latch is updated at each clock during an NVR operation.

The microprocessor reads the NVR during the power-up process. The bits are deserialized by rotation as they are read in. Although 14 bits from each NVR word are written or read, only 8 bits are used by the microprocessor. The data goes into location in the scratch portion of RAM for use during a later portion of the power-up.

6.5.10.3 NVR Timing – The NVR clock is the lowest frequency line buffer address signal (LBA 7H). It occurs at the horizontal line rate, 15.734 kHz. This is the bit shifting rate during address and data transfers. A read operation requires only a single clock cycle to transfer data into the data register, but an erase or write of a word takes 20 milliseconds.

When shift data out mode is entered, the first data bit may appear, but it will become stable 25 μs later. Subsequent data bits will be shifted out on the falling edge of the clock flag (rising edge of the signal on pin 5 of the chip) and will become valid 25 μs later. This means that, following a change to shift data out mode or a falling edge of clock flag during this mode, a delay of 25 μs must occur before reading of the NVR data flag is attempted. The first bit shifted in when writing is the first bit shifted out when reading.

When using the ER1400, it is necessary to operate with interrupts off.

6.5.11 Keyboard Interface

The keyboard interface is a bidirectional interface that separates incoming data from outgoing data on a single wire. The interface circuits contain a hardwired programmed universal asynchronous receiver-

Table 6-6 NVR Control States

Command State	Control Inputs D003 H	D002 H	D001 H	NVR Operation
0	H	H	H	Standby. The device output floats.
3	L	L	H	Accept address. Two 1 of 10 addresses are shifted in at the clock rate. The first group is the 10's decade and the second is the 1's decade of the 1 of 100 word address.
2	H	L	H	Erase. The word stored ~~at the~~ addressed location is erased to all zeros.
7	L	L	L	Accept data. The data register accepts serial data shifted from the I/O pin. The address register remains unchanged.
6	H	L	L	Write. The word contained in the data register is written into the location designated by the address register.
4	H	H	L	Read. The addressed word is read from memory into the data register.
5	L	H	L	Shift data out. The output driver is enabled and the contents of the data register are shifted out.
1	L	H	H	Not used.

transmitter (UART), a comparator, and supporting gate circuits that encode the transmitted terminal data and keyboard clock. The UART converts parallel data from the terminal controller data out lines (DO 07–00 H) into serial data that is sent to the gate circuits. The gate circuits encode the data and keyboard clocks into a pulse-width modulated signal that is sent to the comparator and then transmitted to the keyboard over the single wire.

Serial data from the keyboard is received by the comparator, converted to TTL voltage levels, and then sent to the serial input of the UART. The UART converts the serial data input to parallel data for transfer to the data bus (DB 07–00 H).

6.5.12 Video Processor

The video processor is the heart of the monitor display. It is composed of the devices shown on the right side of the terminal controller block diagram (Figure 6-5). This section discusses the general mechanism that converts data into a visible display, followed by a discussion of the two central devices (the timing and control chips) and a general discussion of all the other blocks on the video processor side of the block diagram. The interactions between the data paths on the left of the diagram and the processor on the right are covered in Paragraph 6.5.13.

The video processor converts data into an electrical signal that a CRT monitor can turn into visible letters, numbers, and symbols. The video processor works with the characteristics of the CRT monitor to do this. The following is a brief description of these characteristics.

The Raster
The raster is the area on the CRT screen that is scanned by an electron beam moving in a regular pattern. Deflection coils cause the beam to quickly scan a series of horizontal lines while moving relatively slowly down the screen. This scanning repeats quickly and constantly, and persistence of vision makes the entire screen look continuously scanned. The beam may be on or off, lighting the fluorescent phosphor on the face of the CRT or leaving it dark, but the beam's continuous motion traces and defines the raster.

Character Formation
As the beam moves in its horizontal scans, it can be turned on and off very quickly. This means that a spot of light (called a dot) can be produced anywhere along each horizontal scan line. Each scan contains the same number of potential dots. If only one dot is lit in a scan but dots in the same position on several successive scans are also lit, the screen appears to have a vertical line on it. This ability to line up dots on different scans is the key operating feature of the video processor.

Limiting our discussion to 80 column lines for this description, each character that can be displayed on the monitor is made up of a matrix of dots, ten wide and ten high. There are 800 dots in a scan and the raster is made of 240 scans. Therefore, there are 80 groups of 10 dots in each scan horizontally, and 24 groups of 10 scans vertically. Each 10 dot by 10 scan group is a character cell, where a character can be displayed. There are 80 by 24 character cells on the screen. As the electron beam scans the raster, the video processor turns the beam on and off, assembling the characters scan by scan.

Video Processor Data
When we say the characters are assembled scan by scan, we mean that only one scan of information about a character is displayed and then the same scan for the next character is displayed. This continues to the end of a line of characters. Then the next scan of the first character is displayed, followed by the same scan of the next character, and so on. Therefore, each character must enter the video processor ten times, once for each scan, and remain only until the next character in the line is displayed.

Each character in a line is stored in one of a group of adjoining locations in the screen RAM. (See Figure 6-12 for the video processor functional diagram.) The process of moving a line of character data from the screen RAM to the video processor takes the same amount of time as a scan. During data movement the microprocessor cannot use the RAM; so, to give the microprocessor as much working time with the RAM as possible, the video processor accepts the line of character data for display during the first scan and stores it in its line buffer at the same time for use during the other nine scans. Movement of data from the screen RAM to the line buffer by the video processor is called direct memory access (DMA). During the DMA, the video processor provides addresses to the screen RAM with the address counters. The data is stored in the line buffer that gets its addresses from the line buffer address (LBA) outputs from the DC011 timing chip. Both kinds of addresses change values when they receive a clock (called character clock) that occurs after each ten dots. This clock makes the character data in the video processor change at the right times to provide proper alignment of the display.

The character latches hold the data coming from the screen RAM or line buffer and ensure that the data remains stable for long enough periods to be written into the line buffer or the video shift register. The buffer between the latches is tristatable and, during non-DMA time, prevents the normal data flow on the microprocessor data bus from interfering with the video processor's reading of data from the line buffer.

Video Processor Character Generation
Data, coming either from the screen RAM for scan 1 or the line buffer for scans 2 through 10, becomes part of an address to a character generator ROM. The rest of the address comes from a scan counter in the DC012 control chip. The scan counter addresses the ROM according to which of the ten scans is to be displayed. The 4-bit scan counter skips over the other 6 possible addresses to the ROM, so the ROM contains data in only 10 out of 16 locations. The output of the ROM is eight bits that represent the pattern of

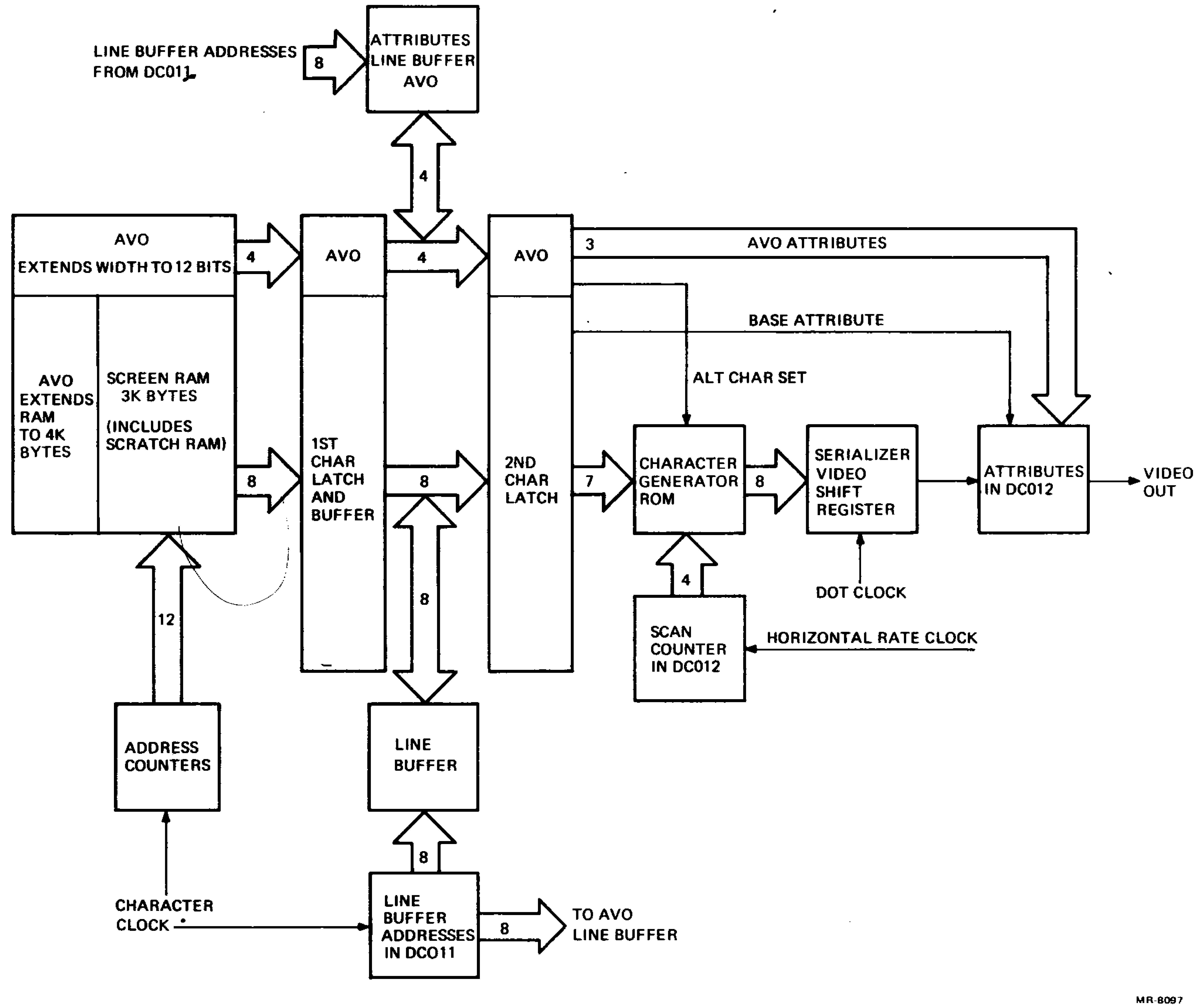


Figure 6-12 Video Processor Functional Diagram

sequential dots to be displayed for that character on that scan. The eight bits enter the video shift register, a serializer that converts the eight parallel bits into a 1-bit wide stream. An extra flip-flop stores the last bit so it can be output to the stream two or three extra times (depending on line length) to fill the intercharacter space. The stream enters the DC012 control chip, where the final adjustments for video display are made, and then the video signal goes to the CRT monitor.

Attributes

Three attributes apply to the monitor display: character, line, and screen. Character attributes provide a special appearance to characters as they appear on the CRT screen. In the basic VT100 (without an advanced video option) only one bit of memory (called the base attribute bit) is available to each character on the screen. The original character data from the screen RAM is eight bits wide, but only seven bits define the character itself. The eighth bit defines the base attribute. The attribute bit bypasses the character generator ROM and video shift register and enters the DC012. There it controls the presence or absence of the attribute as that character is displayed. The base attribute is displayed as either reverse video or underline, depending on the selection of the cursor at set-up. It is invoked by the base attribute bit. Reverse video appears as all ten scans of a character cell reversed (black changes to white and vice versa). Thus, if two vertically adjacent characters are in reverse video, no black space appears between them. Underline forces the ninth scan on. (The ninth scan is forced off with reverse video screen attribute.) Once a character attribute or combination of attributes is set, all displayable characters sent to the terminal have that attribute regardless of where they are placed on the screen. This continues until the attribute selection is changed.

Line attributes are double-height, double-width, and scroll. The monitor displays single-width, double-width or double-height, double-width characters on a line by line basis. All characters on one line appear in the same mode. Double-width lines are generated by displaying each dot of a character twice in the horizontal direction. Double-height, double-width lines are generated by displaying each dot of a character four times (twice horizontally and twice vertically). The top and bottom halves of a double-height, double-width line must be entered as two separate lines of characters. The scroll attribute indicates that a line is part of the scrolling region.

Screen attributes affect the entire screen's characteristics at once. They include the base attribute selection (reverse or underline as mentioned under character attributes), reverse video over the entire screen, 80 or 132 character line length, 50 or 60 Hz refresh rate (chosen according to the local power supply), interlaced or noninterlaced operation, and jump or smooth scrolling of data over the screen.

Advanced Video Option (AVO)
The AVO extends the length of the screen RAM so more characters can be displayed in 132 column mode. In addition, it allows each character to have four more attributes, for a total of five. Three of the AVO attribute bits enter the DC012 to control displayable features of each character. The fourth AVO attribute bit controls the selection of an extra character set by switching in an optional alternate character generator ROM that can provide non-ASCII characters or other special displays.

To provide the extra attribute bits, the AVO widens the entire screen RAM by 4 bits to make each character location 12 bits wide. It also contains a 4-bit wide extension of the character latches and a 4-bit wide attribute line buffer, addressed by the same LBA signals as the regular line buffer. This extension treats the attribute data with the same timing as the character part of the circuit and matches each character with its attributes.

With the AVO present, reverse video, underline, bold, and blinking are all available singly or in combination. Reverse and underline appear as described above with the addition that if both reverse and underline are asserted, the underscore is forced dark instead of light. Bold increases the intensity of the display. The blink rate is about half that of the cursor or about 0.5 Hz. Cursor selection is independent of character attributes when the AVO is installed.

6.5.12.1 Timing Chip Description – The DC011 is a custom designed, bipolar, integrated circuit that provides most of the timing signals required by the video processor. Internal counters divide the output of a 24.0734 MHz oscillator (located elsewhere on the terminal controller module) into the lower frequencies that define dot, character, scan, and frame timing. The counters are programmable through various input pins to control the number of characters per line, the frequency at which the screen is refreshed, and whether the display is interlaced or noninterlaced. These parameters can be controlled through set-up mode or by the host. In the following discussion, refer to the block diagram in Figure 6-13.

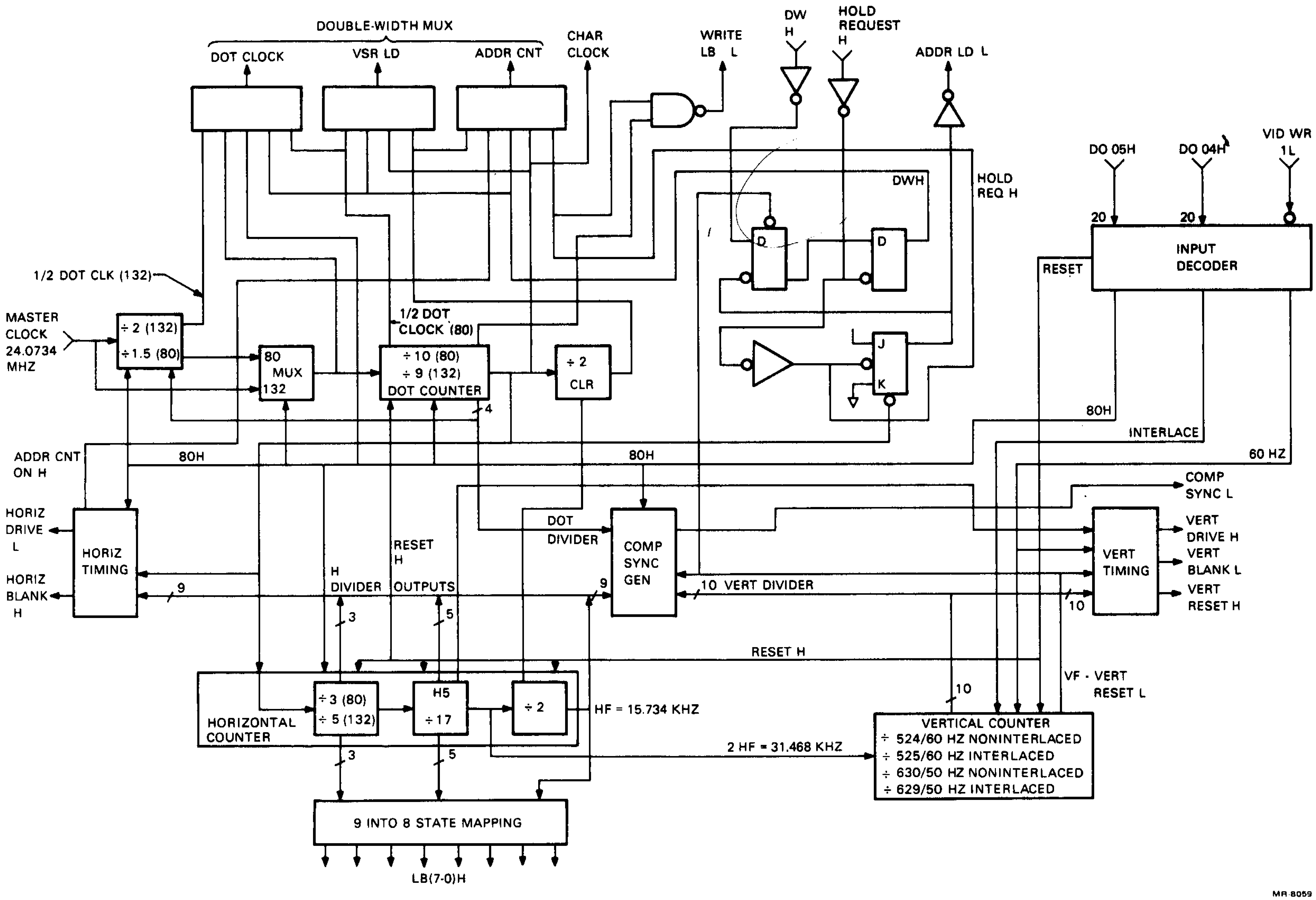


Figure 6-13 DC011 Timing Chip Block Diagram

Input Decoder
The input decoder responds to commands on pins 20 and 21 (connected to DO 04 H and DO 05 H of the 8080 bus respectively) whenever the VIDEO WR 1 L pin is low. The outputs of the decoder select 80/132 column, 60/50 hertz refresh, and interlaced/noninterlaced modes of operation. Table 6-7 shows that when DO 05 H is low the number of columns is programmed according to the state of DO 04 H, and when DO 05 H is high the refresh rate is programmed. Interlaced mode is always selected when the column mode is set, and noninterlaced mode is selected when the refresh rate is set. The interlace mode that is in use depends on whether the number of columns or the refresh rate was selected last.

Table 6-7 Video Mode Selection (Write Address = C2H)

Inputs D005 H Pin 21	D004 H Pin 20	Configuration	Function
0	0	80-column mode	Sets interlaced mode
0	1	132-column mode	
1	0	60 hertz mode	Sets noninterlaced mode
1	1	50 hertz mode	

In addition to strobing data into the input decoder, VID WR 1 L acts as a reset signal for the DC011. Whenever VID WR 1 L is low, the counters in the DC011 are held in a cleared state. Resetting the counters serves no purpose in the VT100 because the remainder of the VT100 synchronizes itself to the DC011, but a reset is useful for testing both individual chips and complete modules. Writing into the DC011 is never done unless the mode is being changed because it would cause the counters to reset and disturb the display.

80/132 Column Selection
The column mode is changed by modifying the divisors of three of the counters in the DC011. The first of these counters divides the input clock (MASTER CLK) by 1.5 to produce the dot rate clock for 80-column mode. The DOT CLK output provides the signal that controls the shifting of dots out from the video shift register. A multiplexer determines what rate DOT CLK will have for the entire screen by selecting either the output of the divide-by-1.5 in 80-column mode or by selecting the 24 MHz MASTER CLK directly in 132-column mode. The other two counters affected by 80/132 selection are the dot counter and the horizontal counter.

Dot Counter
The dot counter uses four flip-flops to divide the DOT CLK that was selected by the multiplexer by 10 (in 80-column mode) or by 9 (in 132-column mode). The output of the dot counter is the character rate clock, which is used to move character codes in the latches that are outside the DC011. Character clock is further divided by the horizontal counter. CHAR CLK is unaffected by double-width mode. The output of the next-to-last flip-flop is used for the write enable signal for the line buffer RAMs (WRITE LB L). This signal allows the data and address changes, caused by the rising edge of CHAR CLK, to become stable before writing is enabled. It then disables writing before CHAR CLK rises again. WRITE LB L is gated directly with HOLD REQ H so that it is active only during DMAs. Intermediate signals from the four flip-flops are used by various other functions in the DC011 such as the double-width multiplexer and the composite sync generator.

Double-Width Multiplexer
The double-width multiplexer (MUX) produces the three signals whose timing must be changed when a line of characters is switched between single- and double-width modes. The frequency of DOT CLK must be divided in half on a double-width line so that the video shift register will shift half as often, making each dot (and therefore each character) twice as wide as it would be in single-width mode. In order for the video shift register to work properly with the half-rate DOT CLK in double-width mode, the load signal for the shift register (VSR LD H) must still come every 10 dots (80-column mode) or 9 dots (132-column mode). Therefore, loads must occur at every other CHAR CLK. Similarly, incrementing the DMA address counters occurs on every other CHAR CLK to ensure that characters that are stored sequentially in the screen RAM are presented to the shift register at the correct time for each VSR LD H pulse.

In single-width mode, the double-width MUX directs the output of the 80/132 MUX to the DOT CLK pin, providing either a 16 MHz or 24 MHz output. To get the half-rate DOT CLK for 80-column mode, the double-width MUX selects the output of the first flip-flop in the dot counter, which acts as a divide-by-2 because the dot counter is dividing by 10 and 10 is an even number. In 132-column mode the same selection cannot be made because the dot counter is dividing by 9. But the divide-by-1.5 is not needed in 132-column mode, so this divider is converted to a divide-by-2. The double-width MUX selects its output when a double-width line is displayed in 132-column mode.

The load input of the video shift register used in the VT100 is a synchronous input. This means that when the load input is high, the rising edge of DOT CLK causes a parallel load to be performed instead of a shift. To get one load and many shifts for each character, VSR LD H can only last for that one cycle of DOT CLK that is adjacent to CHAR CLK. Furthermore, transitions of VSR LD H must satisfy set-up and hold times with respect to the rising edge of DOT CLK. In single-width modes, VSR LD H is one dot time wide, generated from the outputs of the dot counter, and its set-up and hold times are guaranteed by internal propagation delays. In double-width mode, VSR LD H is created by selecting every other CHAR CLK and then delaying this signal by one single-width dot time.

The signal that increments the DMA address counter (ADDR CNT) has the same timing as CHAR CLK, but it does not run continuously. ADDR CNT can only be generated if HOLD REQUEST H is high. It is further controlled by a signal from the horizontal timing section (ADDR CNT ON H) that allows ADDR CNT to provide exactly three pulses, in single-width mode, before HORIZ BLANK H goes low. The three pulse delay primes the external character latches so that the dots for the first character on a line are being loaded into the video shift register at the same moment that HORIZ BLANK H enables the video at the beginning of a scan. The only change made to ADDR CNT for double-width operation is that every other pulse is deleted, beginning with the first pulse.

Horizontal Counter
The block diagram in Figure 6-13 shows the horizontal divider broken into three stages. The first divider is programmable according to the number of columns selected and is driven by CHAR CLK from the dot counter. For 80-column mode the divisor is 3; for 132-column mode the divisor is 5. The total division from MASTER CLK to the output of this first divider is 45, independent of column mode (for 80-column mode: $1.5 \times 10 \times 3 = 45$; for 132-column mode: $1 \times 9 \times 5 = 45$). Therefore, the operation of all of the remaining dividers in the DC011, which are driven from the first horizontal counter, is also independent of the column mode.

The second stage of the horizontal divider has a divisor of 17, which is chosen to give the required number of displayable columns plus about 28 percent more to allow time for the monitor to execute a horizontal retrace. The last stage is a simple divide-by-2 that provides the horizontal frequency. Therefore, at its input, the signal will have a frequency twice that of the horizontal frequency. This is required by the vertical dividers to create interlaced operation. The total division from CHAR CLK provided by the horizontal divider is 102 in 80-column mode and 170 in 132-column mode. In either mode the frequency at the output of the horizontal counter is 15.734 kHz.

Horizontal Drive and Horizontal Blank
Two timing signals are generated from the horizontal counter to control those system functions occurring at the scan rate. These signals begin at the end of a scan and last until the horizontal counter is incremented past a specific state that is decoded to turn the signals off. The monitor requires a pulse at the end of every scan to tell it when to initiate a retrace and begin the next scan; the duration of this pulse must be between approximately ¼ and ½ of one scan. Figure 6-14 shows HORIZ DRIVE L as produced by the DC011. The slight difference in timing between 80- and 132-column modes is the result of design convenience and is not significant to the operation of the VT100.

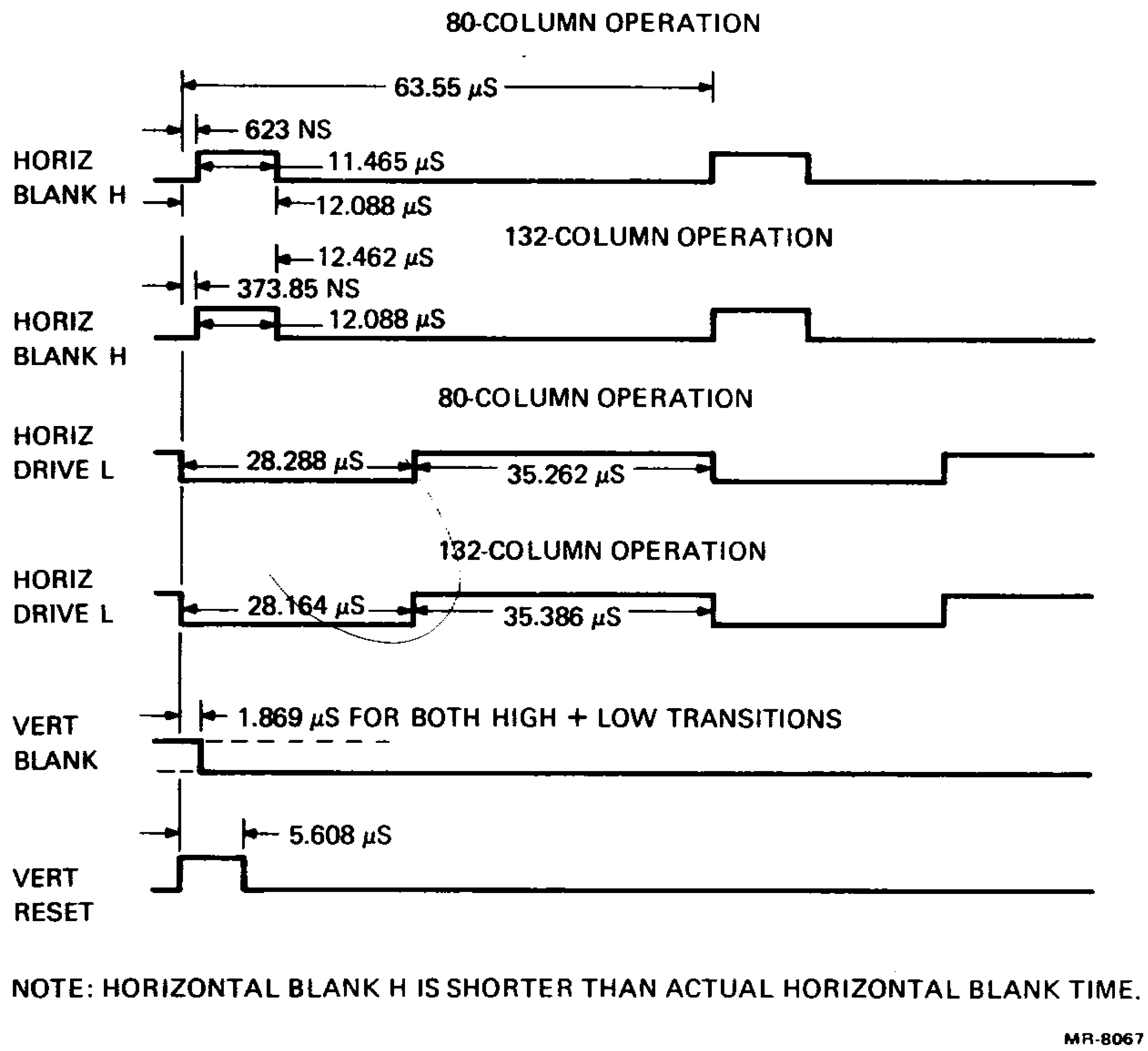


Figure 6-14 Horizontal Timing

HORIZ BLANK H is designed to allow 83 characters during the forward scan in 80-column mode and 137 characters in 132-column mode. The extra characters are included for possible future use such as a field of indicators along the right margin of the screen or as extra symbols inserted to mark text.

The rising edge of HORIZ BLANK H is resynchronized to CHAR CLK to eliminate the accumulated delay of the horizontal counter. The falling edge of HORIZ BLANK H occurs between two CHAR CLKs to meet some requirements of the DC012, but inside the DC012 HORIZ BLANK is delayed to the falling edge of CHAR CLK so that the beginning of each displayed scan will coincide with a character boundary.

Line Buffer Addressing
The line buffer memory stores one line of characters during a scan on which a DMA occurs and then recalls these characters on each successive scan until the next DMA. Because the line buffer is a random-access memory, it has address inputs that must be provided with a sequence of addresses that change at each CHAR CLK such that each character is stored in a unique location. The horizontal counter can pro-

vide such addresses because it is incremented through a series of unique states that repeat in the same sequence on every scan. Because of the three stages that comprise the horizontal counter, there are nine flip-flops whose outputs must be converted into the eight line buffer address (LBAs) outputs. The conversion is possible because the 9 flip-flops represent a maximum of 170 states in 132-column mode (8 bits can represent 256 states). The DC011 contains gates that combine the output of the ninth flip-flop in the horizontal counter with the outputs of the other eight to generate some addresses that are not otherwise represented by the eight. The resulting LBAs do not follow a normal binary counting sequence; the sequence of unique addresses repeats exactly on each scan.

Several of the LBAs are used as general purpose clocks in the VT180. LBA 3 and LBA 4 are used to generate timing for the keyboard. These signals satisfy the keyboard's requirement of two squarewaves, one twice the frequency of the other, even though every sixteenth transition is delayed (the second stage of the horizontal counter divides by 17, not 16). LBA 7 is used by the nonvolatile RAM.

Vertical Operation

To paint a complete picture on the screen, the monitor moves the electron beam slowly from the top of the screen to the bottom while it is also moving the beam quickly from left to right to paint each scan. The vertical sweeps of the beam must be repeated continuously so that the picture is refreshed often enough to prevent flicker. In television terminology, a single pass of the beam from the top of the screen to the bottom (and the data displayed during that time) is referred to as one field. A complete picture, which may contain one or more fields depending on the type of interlacing in use, is called one frame. When the VT180 is used in noninterlaced mode, each successive field is identical and therefore only one field is contained in each frame. During interlaced operation in the VT180, there are two types of fields that alternate with each other so that each frame consists of two fields. Even fields start at the top of the screen and display 240 scan lines before reaching the bottom. Odd fields place their first scan line between the first and second scans of the preceding even field and then place each additional scan between succeeding scans of the even field. Interlacing the even and odd fields gives a whole frame of 480 scans instead of 240 scans. This provides increased vertical resolution.

In noninterlaced operation, commands to the monitor to begin a new field are always coincident with commands to begin a new scan. This causes the beam to always be in the same vertical position when the first displayed scan is begun. In interlaced mode, odd fields begin with a command for a new frame that occurs halfway through a scan line. This causes the beam to have moved down the screen from where it would have been during an even field (by the distance that it moves in one-half of a scan) when the first displayed scan is begun. Even and odd fields are made to alternate by including an odd number of half-scans in every field. This is in contrast to noninterlaced operation, where each field contains only complete scans. The monitor always displays the same video information on both even and odd fields. Interlaced mode is provided for future use by options that desire increased vertical resolution.

Vertical Counter

The 10-bit vertical counter, shown in Figure 6-13, determines the frequency at which the screen is refreshed by counting the number of horizontal scans included in each field. The vertical counter uses the 31.468 kHz output of the horizontal counter so that it can count the half-scans required for interlaced operation. Figure 6-13 lists the four available divisors that select the interlace mode and keep the refresh frequency as close to the local power line frequency as possible (to minimize interference with the screen from nearby equipment). The vertical frequencies produced by these divisors are approximately 1/20 Hz above or below the nominal power line frequency.

Vertical Outputs

Three outputs are derived from the flip-flops in the vertical counter to control the vertical refresh operations in the VT180. These signals are shown for all four modes in Figures 6-15 and 6-16.

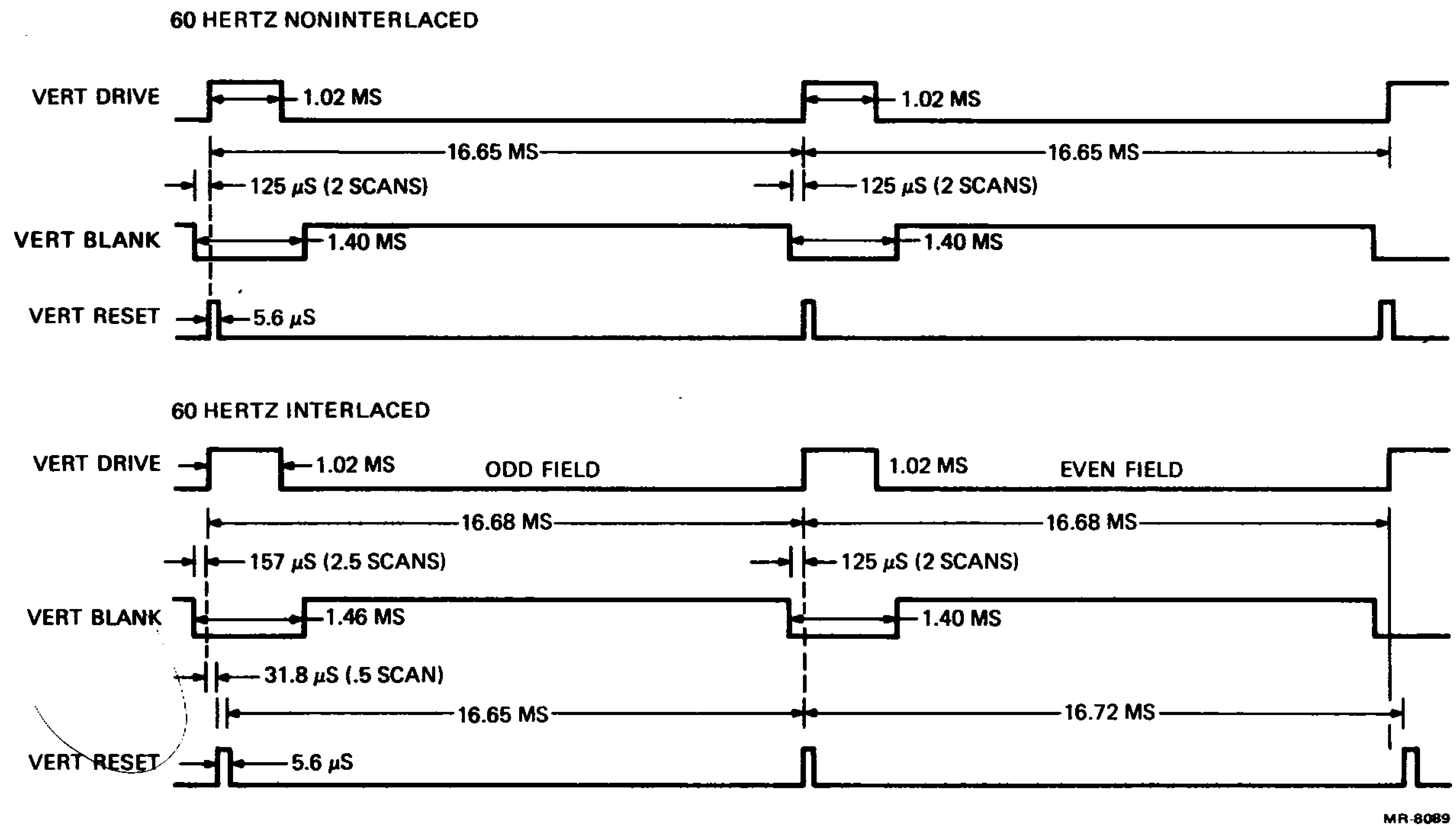


Figure 6-15 Vertical Signals – 60 Hz

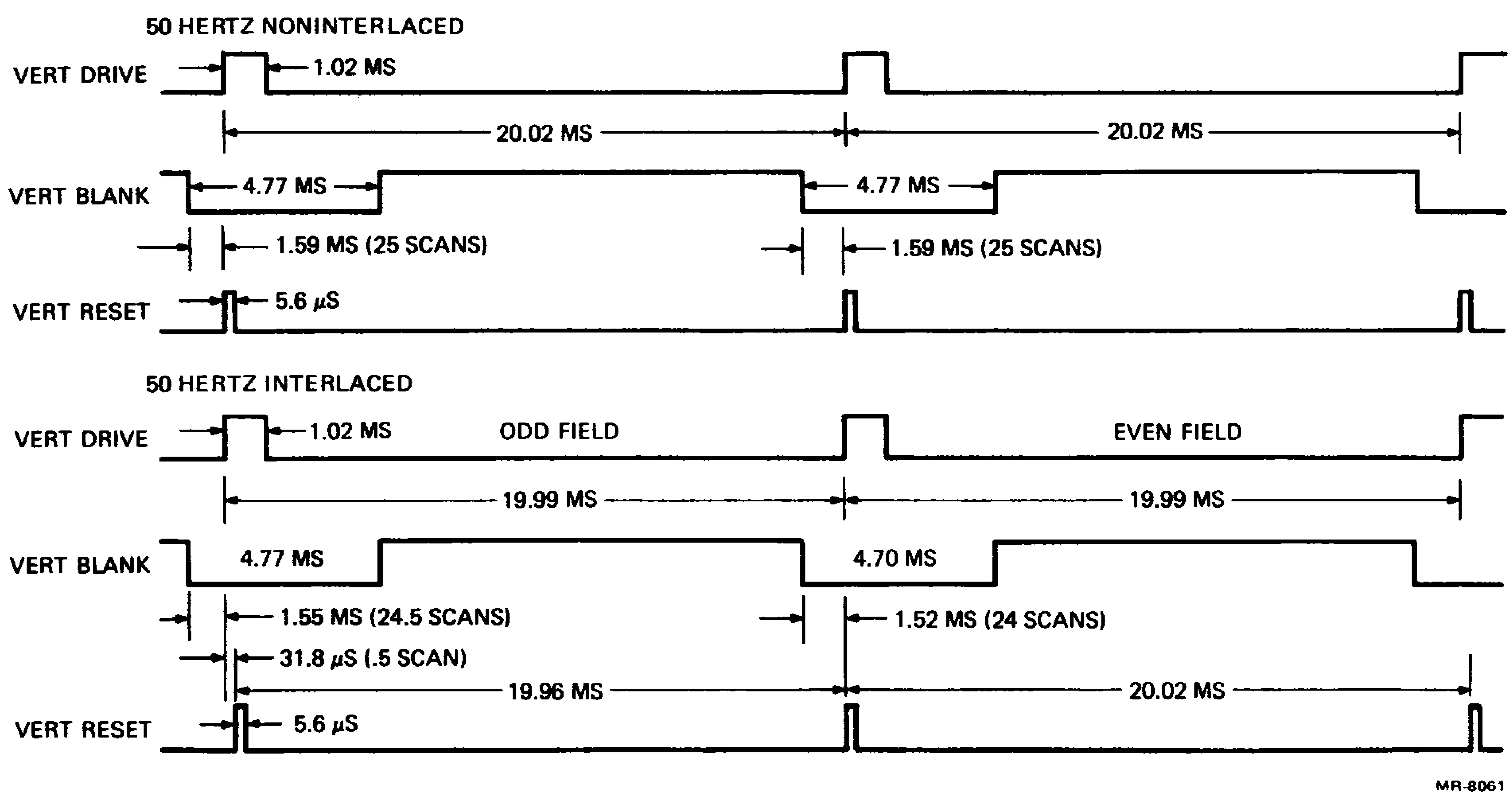


Figure 6-16 Vertical Signals – 50 Hz

VERT DRIVE H is issued at the bottom of the screen to initiate a vertical retrace followed by a new vertical scan. This operation is analogous to the effect of HORIZ DRIVE L on horizontal scans. The time between any two VERT DRIVE Hs is a constant, equal to an even number of half-scans in noninterlaced mode and equal to an odd number of half-scans in interlaced mode.

VERT BLANK L always enables exactly 240 scans during any field and blanks any remaining scans. Furthermore, VERT BLANK L is always turned off exactly 20 scans after VERT RESET H in 60 Hz mode and 50 scans after VERT RESET H in 50 Hz mode. VERT BLANK L is always adjusted to display complete scans even during odd fields in interlaced mode.

VERT RESET H initiates the DMA process at the start of every field. When VERT RESET H goes high, the DMA address counters are reset to point to address 2000H in the screen RAM, all line attributes are cleared, and the scroll counter in the DC012 is preset to the value stored in the scroll latch. (See the DC012 description for more explanation.) During noninterlaced operation and on even fields, VERT RESET H occurs at the same time as VERT DRIVE H; but, on odd fields VERT RESET H is delayed one-half of a scan to match the start of a horizontal scan. The relationship of VERT RESET H and transitions of VERT BLANK L to HORIZ BLANK H and HORIZ DRIVE L is depicted in Figure 6-14. Notice that VERT BLANK L always turns on or off when the video is already blanked by HORIZ BLANK H.

Composite Sync
The COMP SYNC L signal supplied by the DC011 is combined with video information by the terminal controller board to produce the composite video signal that appears on J9 at the back of the VT180. An external monitor can use the composite video signal to reproduce the image displayed on the monitor screen. This is accomplished by using the video information to control beam intensity and the composite sync waveform to synchronize the raster to the video information.

The composite sync generator in the DC011 uses outputs from the dot, horizontal, and vertical counters to generate the complex timing of COMP SYNC L. COMP SYNC L consists of one of the vertical intervals depicted in Figure 3-29 followed by 240 horizontal sync pulses, another vertical interval. The vertical synchronizing interval consists of a transition from horizontal sync pulses to six equalizing pulses, six vertical sync pulses, six more equalizing pulses, and then a return to horizontal sync pulses. Two vertical intervals are shown in Figure 3-29. The vertical interval that begins an odd field is similar to that which begins an even field except that the equalization and vertical sync pulses are shifted by one-half scan with respect to the horizontal sync pulses. In noninterlaced mode, all fields are even fields; but, in interlaced mode, every other field is an odd field. Figure 3-29 also shows the relationship of COMP SYNC L to both HORIZ BLANK H and VERT BLANK L. COMP SYNC L meets the requirements of EIA RS-170 and the NTSC standards for sync pulse generators.

Hold Request, Address Load, and Double-Width
The logic associated with HOLD REQ H, ADDR LD L, and DW H is shown in Figure 6-13. The falling edge of HOLD REQ H sets ADDR LD L to the low state; ADDR LD L is subsequently cleared by the falling edge of CHAR CLK, thus creating a short low pulse on ADDR LD L at the end of each DMA. ADDR LD L stores, in their respective registers, all line attributes and the memory address of the next line to be accessed by a DMA. The rising edge of HOLD REQ H causes the value of DW H that was stored in the holding flip-flop by the previous ADDR LD L to be transferred to a second flip-flop whose output controls the double-width MUX. This means that the value of DW H stored at the end of one DMA by ADDR LD L does not actually become effective until the beginning of the next DMA. The holding flip-flop for DW H is cleared by VERT RESET H at the start of every field. HOLD REQ H is also used to enable ADDR CNT and WRITE LB L only during DMAs. Interactions of HOLD REQ H with other signals during a DMA are further defined in Figure 6-19.

6.5.12.2 Control Chip Description – The control chip (DC012), like the timing chip, is a custom bipolar device. It accepts attribute specifications and timing signals and delivers addresses for the character generator ROM and attributes for the video output to the monitor. It also generates the hold request signal that halts the microprocessor and initiates DMAs to get lines of characters. Refer to the block diagram, in Figure 6-17.

The DC012 performs three main functions.

1. Scan count generation. This involves two counters, a multiplexer to switch between the counters, double-height logic, scroll and line attribute latches, and various logic controlling switching between the two counters. This is the biggest part of the chip. It includes all scrolling, double-height logic, and feeds into the underline and hold request circuits.

2. Generation of hold request. This uses information from the scan counters and the scrolling logic to decide when to generate hold request.

3. Video modifications: dot stretching, blanking, addition of attributes to video outputs, and multiple intensity levels.

Input Decoder Functions
The input decoder accepts a 4-bit command from the microprocessor when VID WR 2 L is asserted. Table 6-8 lists the commands.

The low eight values are used to load the scroll latch with the offset for smooth scroll. The scroll latch is loaded in two passes, first writing the two least significant bits and then the two most significant bits. Because the offset is a decimal value controlling ten display scans, the combination setting the most significant bits to 11B is not used in the VT180 (11B covers the range 12–16).

The input decoder also toggles the blink flip-flop by complementing the state of the flip-flop whenever 1000B is written. The blink flip-flop invokes blink only where the blink attribute is set.

To save external hardware, the vertical frequency interrupt flip-flop is located in the DC012 because a spare pin was available. It is set by the falling edge of vertical reset. It is cleared by writing 1001B into the input decoder.

Set and clear of reverse field are not toggled because the absolute state is important and there is no feedback for the system to detect the current state. Therefore, the two states are explicitly set to their desired values.

1100B means you set the base attribute to underline and 1101B means you set the base attribute to reverse video. 1110B and 1111B are for future specification.

Any time the input decoder is loaded with 11XXB, the blink flip-flop gets cleared. This is the only way to initialize blink in the chip testing process. The firmware does not currently use the ability to clear the blink flip-flop but if hard copy output was being implemented, it could be used to set the blink to a known state during a freeze.

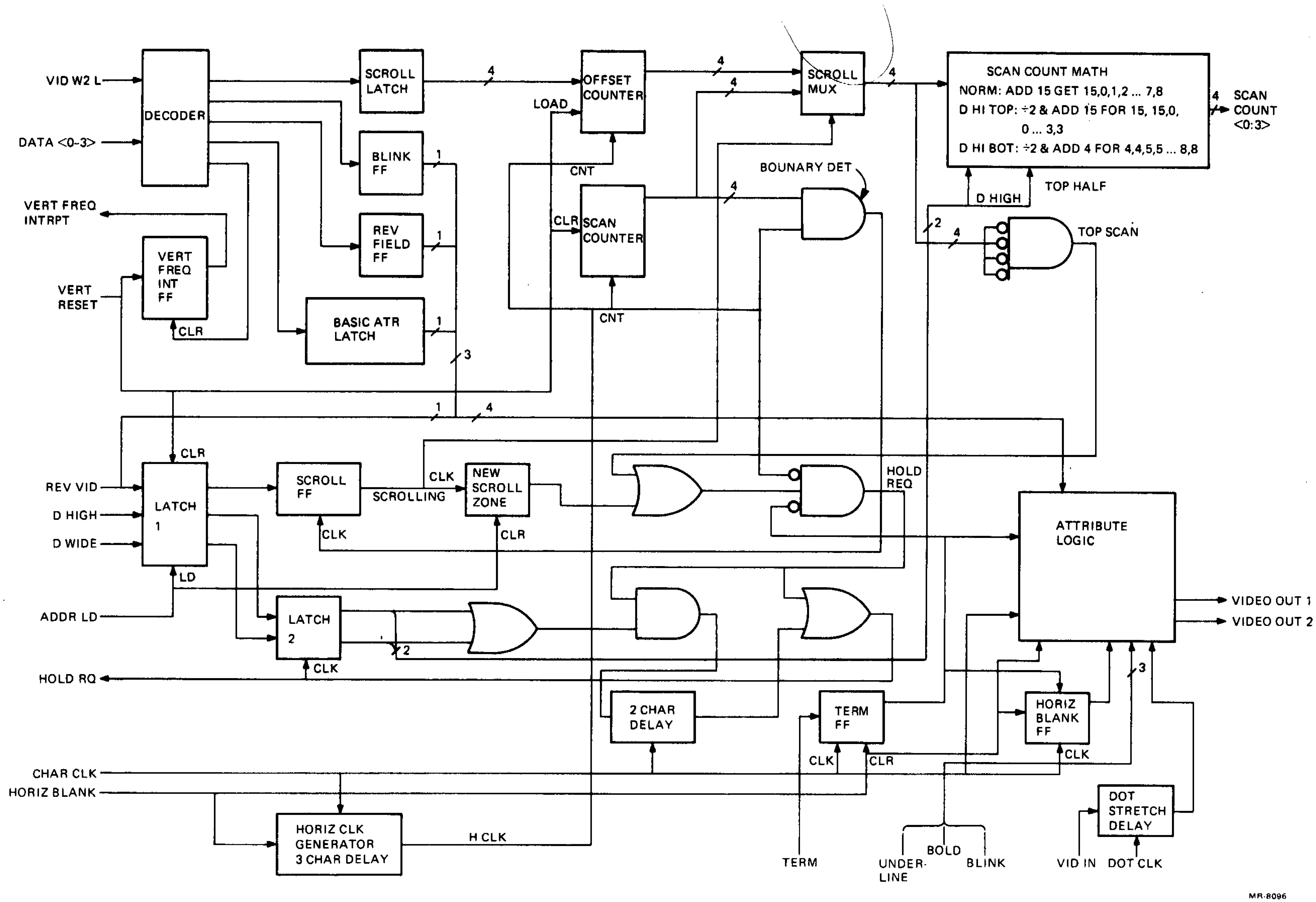


Figure 6-17 DC012 Control Chip Block Diagram

Table 6-8 Control Chip Commands (Write Address = A2H)

D3	D2	D1	D0	Function
0	0	0	0	Load low order scroll latch = 00
0	0	0	1	Load low order scroll latch = 01
0	0	1	0	Load low order scroll latch = 10
0	0	1	1	Load low order scroll latch = 11
0	1	0	0	Load high order scroll latch = 00
0	1	0	1	Load high order scroll latch = 01
0	1	1	0	Load high order scroll latch = 10
0	1	1	1	Load high order scroll latch = 11 (not used)
1	0	0	0	Toggle blink flip-flop
1	0	0	1	Clear vertical frequency interrupt
1	0	1	0	Set reverse field on
1	0	1	1	Set reverse field off
1	1	0	0	*Set basic attribute to underline
1	1	0	1	*Set basic attribute to reverse video
1	1	1	0	*Reserved for future specification
1	1	1	1	*Reserved for future specification

*These functions also clear blink flip-flop.

Attribute Latches

The line attributes are managed by two latches that store the scrolling, double-height (DH), and double-width (DW) bits. The first latch stores the incoming data when address load (ADDR LD) goes low at the end of a DMA. Scrolling means that the next line will be part of the scrolling region; DH means the next line will be double height; and DW specifies top or bottom half for double-height lines. There is no double-height, single-width combination, so in double-height, double-width is assumed. The DW pin also tells the DC012 to extend hold request during double-width. The second set of latches for double-width and double-height are clocked by the rising edge of hold request (similar to the second latch for double-width in the DC011) to invoke the attributes at the beginning of the new line. The first latch stores those attributes from the end of one DMA to the beginning of the next. It is the outputs of the second latch that invoke attributes in the chip. The scroll bit is invoked by a different signal that will be discussed later. The pin defining scrolling is the same pin as reverse video; it means scrolling when loaded in by ADDR LD L and it means reverse video at all other times. The reverse video signal passes from the input pin around the first latch directly to the attribute logic.

Scroll Counter

The scroll counter consists of two 4-bit, divide-by-10 counters called the scan counter and the offset counter. Both are clocked at the horizontal rate to count scans. The scan counter is cleared by vertical reset so that it starts at zero and counts by tens down to the end of the screen.

The offset counter is loaded with the contents of the scroll latch by vertical reset. The scroll latch is loaded by the microprocessor and defines the offset between the scan and offset counters for an entire frame because the offset counter is only loaded at vertical reset time. The microprocessor will load the latch with the offset for the next frame during the current frame.

At the beginning of a frame, the two counters divide by ten but start at different numbers. If not currently scrolling, the offset is zero and there is no functional difference between the counters. If in the middle of a smooth scroll, the offset will be some other value from one to nine. The scan address outputs from the chip to the character generator ROM are either the output of the offset counter or of the scan counter, depending on whether the current line is in or out of the scrolling region, respectively. One of the two counters is selected by a 4-bit wide multiplexer (MUX) whose output is the counter in use. The MUX is controlled by the scroll flip-flop, which is the second latch for the scroll attribute bit. Most line attributes (double-height, double-width) take effect when hold request goes high for the line in which they are effective. They always take effect with the actual data being displayed. However, the scroll flip-flop can only change state when crossing one of the fixed ten scan boundaries that are defined when the scan counter reaching zero.

When the scan counter reaches zero a change can occur from a nonscrolling to a scrolling region or from a scrolling to a nonscrolling region since this is normally where one line of data changes to the next if the line were not scrolling. To get into or out of a scrolling region, the scan counter must be at zero. A 4-bit boundary detect decoder gate is connected to the outputs of the scan counter and clocks the scroll flip-flop when all its inputs are zero. If the input to the scroll flip-flop (from the scrolling attribute latch) has been low and goes high at the end of the previous line's DMA, on zero (boundary detect) the output of the scroll flip-flop, which is the control line of the MUX, causes the MUX to switch from the scan to the offset counter. At the bottom of the scrolling region, the last DMA in the region gets a line from the screen RAM with its scroll attribute not set. When the next zero boundary is reached, as defined by the scan counter, the scroll zone is exited. This happens because the scroll flip-flop will get a zero input again, which will switch the MUX back to the scan counter right in the middle of the line that was part way through scrolling.

Scan Count Math

The scan count output of the scroll MUX goes through combinatorial logic that looks at the double-height bit and the top and bottom half bit and decides whether those scan counts need to be modified for double-height before going out of the chip. If double-height is not asserted, the top and bottom half bit is ignored and the scan is passed through with 1 subtracted in modulo 16 arithmetic. (Thus, 0 becomes 15, 3 becomes 2, 9 becomes 8.) If double-height is asserted and top half is asserted, then the operation is to divide the scan count by 2, and continue to subtract 1 after dividing by 2 so the first scan equals 15, the second scan equals 15, and the third scan equals 0. If bottom half is asserted, the operation is to divide by 2 and add 4. This particular arithmetic arrangement was designed for an external component that is no longer needed. Otherwise, dividing by 2 (and adding 5 for the bottom half) would be sufficient. The scan count changes on the rising edge of HORIZ BLANK H.

Generation of Hold Request

Hold request is the signal to the microprocessor that makes it give up control of the data bus. Then the video processor can DMA a line of data out of the screen RAM and place the data in the line buffer. Two principle conditions can generate hold request. The most common is when the output of the counter in use equals zero, meaning on the first scan of a new line of characters. (The counter in use, which is the output of the scroll MUX, is either the output of the offset or scan counter, depending on whether the current line is in or out of a scrolling region.) When a new line of characters starts, a hold request is needed to get the line's data; and therefore, a detector at the output of the scroll MUX detects scan zero of the counter in use.

The other condition for generating hold request is at the top of a new scrolling region. This is necessary because as the CRT beam moves from a nonscrolling region into a scrolling region, it switches from the last scan of a normally registered line to the first displayed scan of a line that is scrolling. Assuming the scrolling region is in midscroll, the first scan is not the zero scan of the scrolling line, so the counter in use is not zero. The new scroll zone flip-flop (whose clock input comes from the scroll flip-flop that controls the scroll MUX) is triggered by entrance into a scrolling region. When the new scroll zone flip-flop is set, it forces a hold request even if the counter in use is not also zero. If the counter in use is zero (implying an offset of zero between scrolling and nonscrolling lines) there are two simultaneous causes for hold request.

The new scroll zone flip-flop is cleared by ADDR LD that occurs at the end of the hold request generated by the new scroll zone flip-flop. That is, the new scroll zone flip-flop generates hold request. Hold request is cleared either by terminate or horizontal blank, whichever comes first (the VT100 is programmed so that terminate is always first). Termination of that hold request feeds back through ADDR LD and clears the new scroll zone flip-flop. More about hold request follows a discussion of horizontal blank and terminate.

Horizontal Blank and Terminate

Horizontal blank, in addition to blanking the video output, clears the terminate flip-flop and generates an internal timing signal (horizontal time reference) for clocking counters.

A short signal that occurs on every horizontal scan and lasts only a few character times is needed in the chip to clock flip-flops and to disable the decoder gates that detect boundaries and generate hold requests while the counters settle. Horizontal blank cannot be used for this purpose because hold request and boundary detect (and other signals) need to be settled well before horizontal blank ends. The required short signal comes from a small counter triggered by horizontal blank and further clocked by character clock. The counter has two outputs: a two character clock wide signal that enables and disables the boundary detect flip-flop (that drives the scroll flip-flop) and a three character clock wide signal (H CLK) that enables the hold request gate. Boundary detect is enabled earlier than the hold request gate so that the existence of scrolling can set up the new scroll zone flip-flop before hold request is enabled. A gate combines the output of the new scroll zone flip-flop and the output of the boundary detector (counter in use equals zero). The output of that gate is combined with H CLK (three character clocks long following horizontal blank) to generate the rising edge of hold request three character times after the rising edge of horizontal blank. It is also combined with the signal from the terminate flip-flop to end hold request when a terminator is detected.

If terminate did not cut off hold request, then hold request would be disabled by the next falling edge of the H CLK signal, but the VT180 is programmed to always end hold request with terminate. If the VT180 was not working correctly, hold request might be ended by horizontal blank.

Terminate causes a number of functions inside the DC012. The terminate input is not direct; it is sampled on each rising edge of character clock and latched into a flip-flop. When detected, it ends any hold request in progress. In normal screen mode, it blanks the video output, but in reverse screen mode it forces the video output to the dim intensity level. The terminate flip-flop output feeds back to its own input so that, as soon as the flip-flop is clocked with terminate asserted, the flip-flop latches itself up.

Once the terminate flip-flop is latched up by feedback from its output, there is only one way to clear it: through the asynchronous clear input. The flip-flop must not be cleared until horizontal blank has taken over blanking the video output; therefore, the clear is delayed slightly (by one character time after the onset of horizontal blank). The clear is maintained until just before the character clock, which corresponds to the first character on the screen, because data on the video data bus may be undefined and might contain extraneous terminates. These must not be detected during the horizontal blanking interval because they would latch up the terminate flip-flop for an entire scan. However, the internal signal that blanks the video outputs of the DC012 during the horizontal blanking interval cannot be used to clear the flip-flop directly because it must release the video output at the exact beginning of the first character on the screen, and the terminate flip-flop must be capable of detecting the terminator in the first character position. If the internal blanking signal was used to clear the terminate flip-flop, the release time of the flip-flop would not be satisfied; and it might miss a terminate in the first character position (as would be found in set-up and the top and bottom fill lines). Therefore, the horizontal blank output of the DC011 is made to end approximately one-half character time before video unblanking to release the clear on the terminate flip-flop. Inside the DC012, the falling edge of horizontal blank H is delayed to the following character clock to provide the correct video blanking.

Double-Width and Hold Request
The first occurrence of terminate or horizontal blank at the end of a DMA normally gates hold request off. But in double-width mode, hold request is extended by two character times. This is required because each character appears twice in the external character latch pipeline. To get the first and second byte of the next line's address correctly placed with respect to address load, the end of hold request must be delayed by two character times after terminate or horizontal blank. This delay occurs either when double-width is asserted alone or at any time double-height is asserted (because double-height implies double-width). Combine hold request with a two character time delayed version of hold request to give a hold request that starts at the normal time but ends two character times later.

Attributes
The attribute section of the DC012 decides how to interpret various combinations of attribute inputs. A number of different inputs determine attributes applied to each character. There are the four attribute pins: reverse video H, underline L, bold L, blink L. There are also internal signals, mostly from the input decoding section, that affect attributes. These are the blink flip-flop (toggled by the input decoder to provide blink timing), the reverse/normal field flip-flop (set by input decoder), the base attribute flip-flop (set by the input decoder to select whether the reverse video pin is interpreted as reverse or underline), and the scan counts (from the output of the double-height section, that enable the underline on the correct scan). These inputs are applied to a combination of gates that feed into a 4-bit latch before controlling the video outputs. This latch is clocked by character clock to change the attributes during the intercharacter space.

Normal characters appear uninverted at normal intensity by asserting VID OUT 2 whenever VID IN H is asserted. Bold characters are the same as normal characters except that VID OUT 1 and 2 are enabled. Reverse characters (exclusive-OR of reverse video and reverse screen) normally have dim backgrounds with black characters so that the large white spaces have the same impact on the viewer's eye as the smaller brighter white areas of normal characters. Bold and reverse asserted together give a background of normal intensity. Blink applied to nonreverse characters causes them to alternate between their usual intensity and the next lower intensity. (Normal characters vary between normal and dim intensity. Bold characters vary between bright and normal intensity.) Blink applied to a reverse character causes that character to alternate between normal and reverse video representations of that character. Underline causes the ninth scan of a character to be forced to white of the same intensity as the character for nonreversed characters, and to black for reverse characters.

Dot Stretcher
The dot stretcher reduces the video bandwidth required in the monitor (especially in 132 mode) by making the minimum dot width 80 nanoseconds. Wider dots give the CRT time to reach full intensity before turning off again. This makes vertical lines appear to have the same intensity as horizontal lines, rather than looking dimmer because of the brightness loss . The dot stretcher works by delaying the VIDEO IN H signal by one dot time (using a flip-flop clocked by dot clock) and then ORing the undelayed and delayed signals.

6.5.12.3 Address Counter and Data Structure in RAM – Refer to the print set and to Figure 6-5. The address counter (E21, E22, E25, E30) consists of three 4-bit binary counters that can be preset. They are cascaded to form 12 bits with an additional flip-flop that provides a thirteenth bit of address to the screen RAM. Vertical reset clears the counter to an initial hardwired value of 2000H so that the video processor always begins to process from that location after a vertical reset. The counter is loaded with a new address at the end of each DMA when the address load signal appears. The counter counts forward from this address at the character clock rate, using the address count (ADDR CNT H) signal. ADDR CNT H only occurs during hold request; thus, the counter only counts during the DMA portion of each line. The address is loaded at the end of the DMA scan and held until the next DMA begins. The thirteenth bit is programmed by D4 in the high byte of a DMA address. The VT100 firmware programs this bit high to access address 2000H plus the contents of the 12-bit counter. But if D4 were programmed low, DMAs would access address 4000H plus the contents of the 12-bit counter.

In double-width mode, the address count pulses occur half as often as in normal width. The line buffer receives the normal number of WRITE LB pulses, however, so each character gets copied into two adjacent locations in the line buffer.

6.5.12.4 Address Latch Buffer – Tristatable latches (E26, E33) store the address counter outputs for a character period to increase the speed of RAM accesses. This would otherwise be slowed by the long propagation delay of the address counters. The buffers provide sufficient output power to drive the address bus of the basic terminal controller board and the AVO, if present. The outputs are disabled during the non-DMA period to prevent conflict with the microprocessor address bus.

6.5.12.5 Line Buffer – Data arrives at the screen RAM latch (E20) during a DMA cycle and is latched in by the character clock. During the DMA, the tristate buffer (E15) is enabled. Data passes through it to the line buffer (E11, E17) for storage and to the character generator latch input (E16). The line buffer is a 256 by 8 RAM that can hold one full line of data including the three end bytes. The line buffer is written when WRITE LB L is asserted in the middle of each character clock period. Its outputs are disabled during the DMA by the hold request signal. During non-DMA operation, the screen RAM latch samples the 8080 data bus at the character rate; but the tristate buffer is off so the 8080 data has no effect. However, the outputs of the line buffer are enabled and the same data is presented to the character generator latch as was presented during the previous DMA scan.

6.5.12.6 Character Generator – The character generator is a ROM that is addressed by the coded representations of the desired characters stored in the screen RAM. Each code is used as the high 7 bits of the address to a 2K by 8 ROM. (That provides enough storage for 128 characters). The eighth character bit is the base attribute input to the DC012. The low four address bits are provided by the scan counter in the DC012. The seven character bits combine with the 4-bit scan count from the DC012 to give an 11-bit address to the ROM. The data stored at each (scan + character) address is eight bits representing the presence or absence of dots of light at sequential horizontal positions within that scan. Figure 6-18 shows the patterns supplied in the standard character generator ROM.

If the alternate character generator ROM and the advanced video option are present, the AVO may assert ALT CHAR SET L to disable ROM E4 and enable ROM E9 when the alternate character set attribute is set. If the AVO is installed without the alternate character ROM, any character cell in which the alternate set is selected will appear white (or black if in reverse video).

If the AVO is installed without the alternate character ROM, any character cell in which the alternate set is selected will appear white (or black if in reverse video).

If it is necessary to use a different main character set than the one provided in the VT180 but an alternate character set is not required, the following arrangement may be used.

1. Cut jumper W1 to disable the main ROM.

2. Plug a new main ROM into the alternate character ROM socket.

3. The new main ROM must be programmed exactly as the alternate ROM except that the chip select on pin 18 must be programmed for high assertion.

To use a UV erasable PROM in the socket for E9 (which must have Intel 2716 pinouts), cut jumper W4 and insert jumper W5 to put +5 volts on pin 21. The access time of the ROM must be less than 300 ns to guarantee operation in 132-column mode.

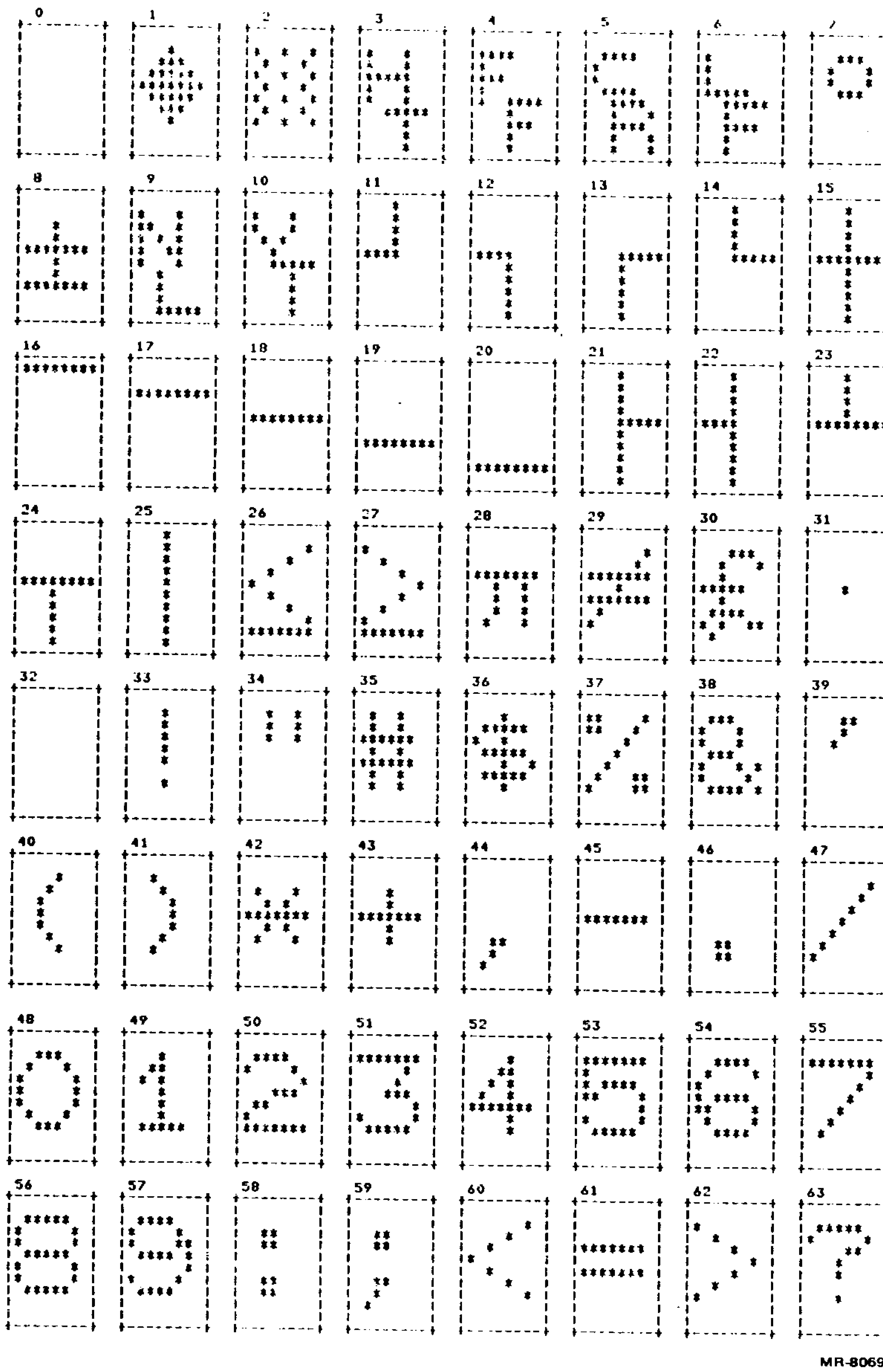


Figure 6-18 Character Generator ROM Patterns (Sheet 1 of 2)

6.5.12.7 Video Shift Register – When VSR LD H is asserted, seven of the eight output bits from the character generator ROM are latched into the shift register. The eighth is latched into a flip-flop. At the same time, the last bit shifted out by the video shift register (VSR) during the previous character time is latched into the first bit position in the VSR. The VSR is continuously clocked by the dot clock. The first bit shifted out in the new character time has the same value as the last bit of the previous character. This provides horizontal continuity of characters from one character cell to the next. The seven new bits are then shifted out.

Meanwhile, the flip-flop that stored the eighth bit has delivered that bit to the serial input of the shift register. This bit was shifted into each successive register position as the first eight bits were shifted out. Now the shifting continues, for one more bit in 132 mode and for two more bits in 80 mode, causing the last bits shifted out to be the value that was stored in the flip-flop.

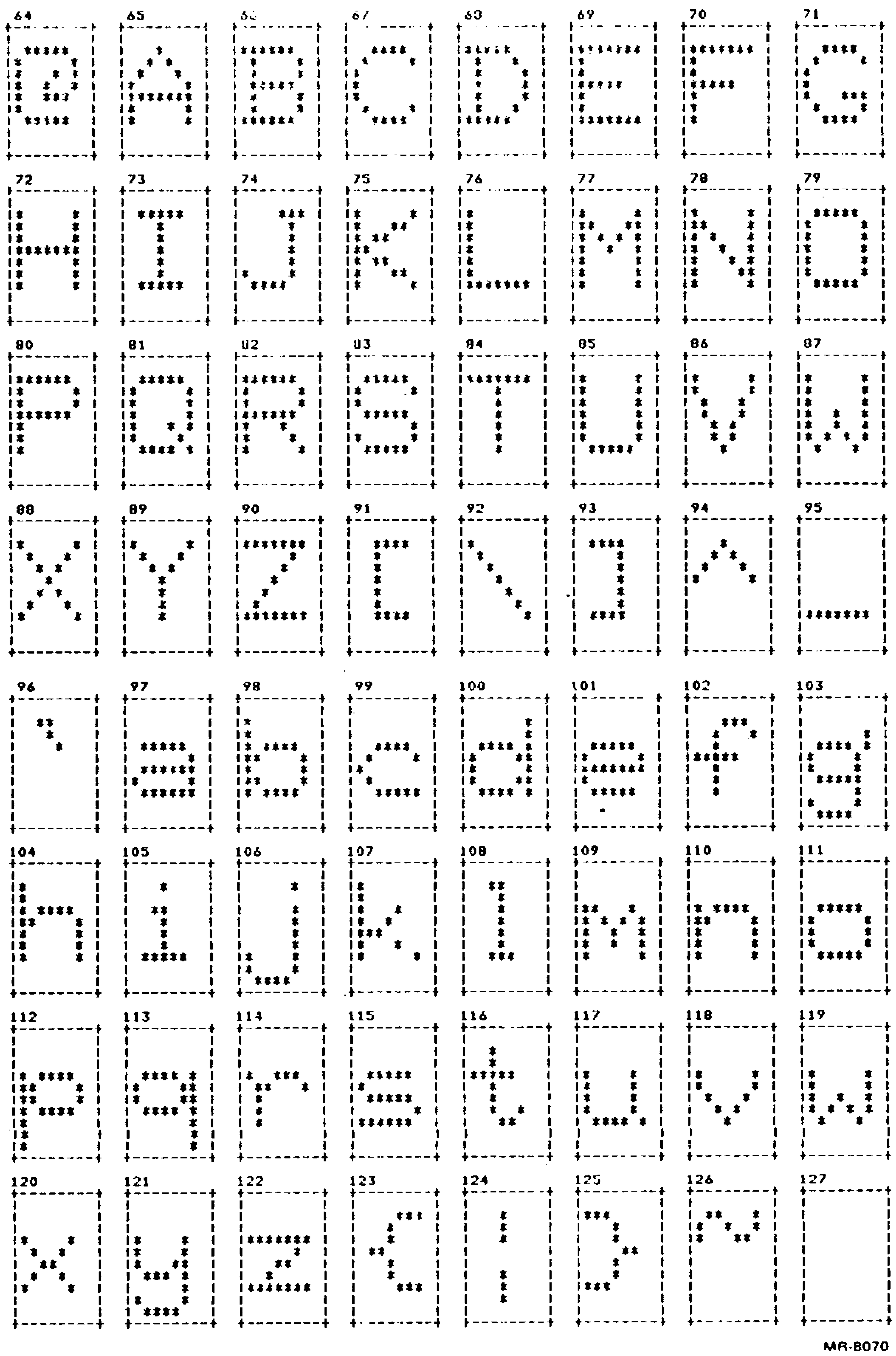


Figure 6-18 Character Generator ROM Patterns (Sheet 2 of 2)

VSR LD H then latches the next character into the VSR and flip-flop, with the last multiply-shifted bit in the first position. In this way, one bit from the character ROM defines the two or three dots between characters, while seven bits define the character itself.

At the end of the scan, horizontal blanking forces the flip-flop output low. Since blanking lasts more than one character time, the low level will be shifted to the first position before the start of the next line. This ensures that the first dot on the next scan will be at the screen background level.

6.5.12.8 Terminator – The seven bits of each character address in a line go to an eight-input terminator detector gate as they are passed to the character generator ROM. Only seven bits are examined because the eighth bit is an attribute and does not contribute to the uniqueness of a character. The last bytes in each line are a terminator character and two address bytes. Only the terminator character activates the gate. During the character time when the terminator reaches the detector gate, the first address byte is at the input to the character generator latch and the second address byte is at the input to the screen RAM latch. On the next character clock, the terminator causes the DC012 to blank the display and end the hold request. The latch outputs now contain the two address bytes. The low order byte is at the inputs to counters E30 and E25, while the low four bits of the high byte are at E21. The fifth bit is at the input to flip-flop E22. This bit is normally high; it allows future development of screen RAM size. The high three bits go to the line attribute inputs to the DC012.

The address load (ADDR LD L) pulse, timed to arrive before the next character clock after the terminator, loads the address counters, flip-flop, and DC012 inputs with the two final bytes. The counters and flip-flop designate the address of the first character of the next line to be displayed.

6.5.12.9 DMA Cycle Timing Diagram – Figure 6-19 shows the complex timing in the video processor during the first scan of each new line of characters. The entire scan is shown, with the repeating portion compressed into the area represented by dashed lines. The diagram is for 80 columns, single-width display, as the VT180 is currently programmed. Diagrams in the DC011 timing chip description (Paragraph 6.5.12.1) show the differences in signals in other modes.

The first line shows the character clock. This continuous signal is the time reference for all DMA events.

The terminator occurs at the end of the previous scan. TERM L goes low for one character clock and then goes to an unspecified state that depends on the random characters that appear at the terminator detector gate. Character clock continues to shift data through the character latches, but invalid data is present in the character latches and is stored in the line buffer until just after DMA ENA is asserted. The terminator forces the video output to black or white (depending on normal or reverse screen), effectively blanking the end of the line (Paragraph 6.5.12.10). It also ends any DMA process in progress. The terminator's blanking effect is taken over by horizontal blank, and the terminate flip-flop in the DC012 is held cleared until just before the first character in the next scan. This prevents undefined data from triggering the flip-flop and blanking the whole scan.

Horizontal blank occurs 3 characters after terminate in 80-column mode and 5 characters after terminate in 132-column mode. It forces all video to black (regardless of normal or reverse screen) for the horizontal retrace interval. The horizontal blank signal, as an output from the DC011, ends one-half character before the video actually needs to unblank. This early transition releases the clear for the terminate flip-flop in the DC012. The blank signal is resynchronized to character clock in the DC012.

Hold request silences the microprocessor so that the video processor can DMA data out of the screen RAM. It is initiated when the scan counter in use is equal to 0, or at the setting of the new scroll zone flip-flop. The terminate flip-flop must be cleared for hold request to occur. The start of hold request is delayed by three character times from horizontal blank to allow the counter in use to settle before the 0-boundary is detected. Hold request is ended by the detection of terminate at the end of a DMA scan.

DMA enable is generated from hold request and the microprocessor's hold acknowledge (HLDA) by discrete logic on the board (E22). It is enabled by the first rising edge of LBA4 if HLDA from the 8080 microprocessor is available. This ensures that the 8080 has given up the bus before DMA ENA H enables the DMA address counters onto the bus and drives MEM R low. DMA ENA H is cleared by the end of HOLD REQ H. While the use of LBA4 ensures that enough time has elapsed from the start of HOLD REQ H to guarantee that the 8080 is in its hold state, the use of HLDA H on the D input of the DMA enable flip-flop is required to prevent HOLD REQ from preventing a power-up cycle in the 8080.

The character latch data bus is shown to be tristated from the start of hold request until the start of DMA enable. Then it starts moving data through the video circuits.

Address count begins three character times before the end of horizontal blank (Paragraph 6.5.12.1).

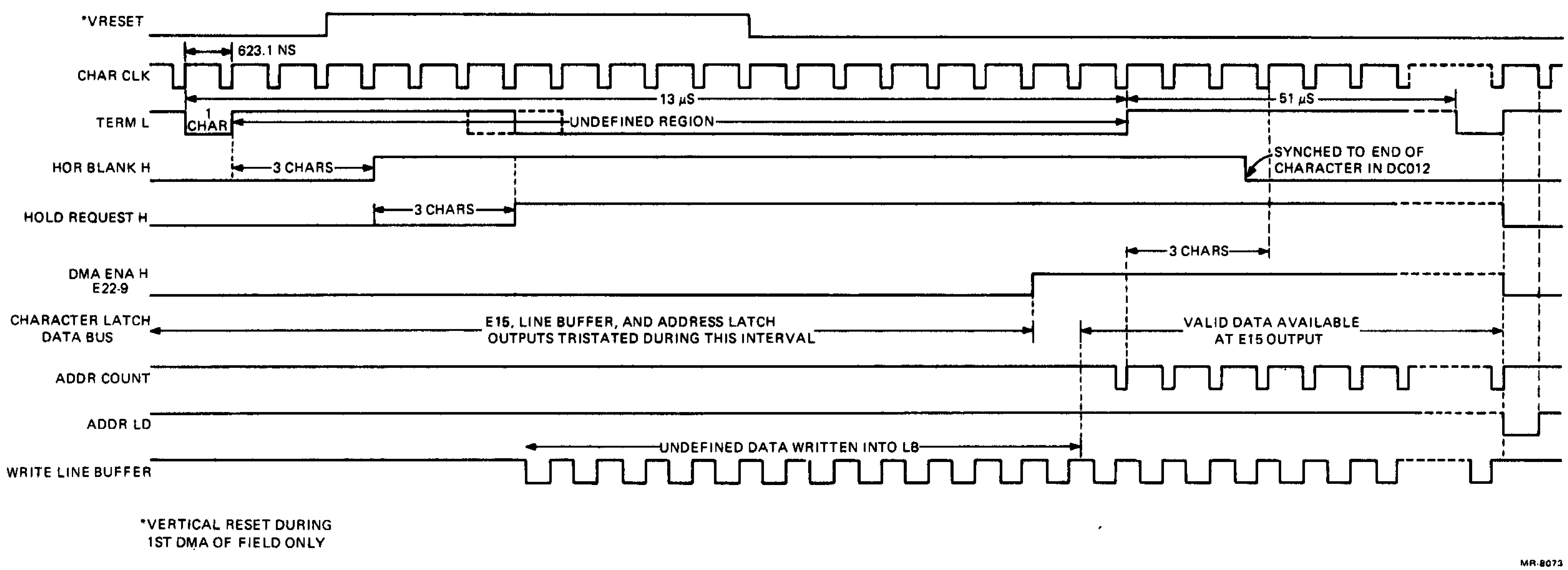


Figure 6-19 DMA Cycle Timing Diagram

Address load is triggered by the falling edge of HOLD REQ H. It stores the line attributes for the next line and loads the address counters with the pointer address bytes at the end of the DMA line of characters. This address is the location of the first character of the next line to be DMAed.

Write line buffer L is described in Paragraph 6.5.12.1.

6.5.12.10 Video Blanking – The display is blanked by horizontal blank during the horizontal retrace interval, and by vertical blank during the vertical retrace interval. These hardware signals ensure that the CRT beam is turned off while it moves backward through the active screen area. Horizontal blank controls the video signal inside the DC012. Vertical blank controls the video signal at the video output circuit.

The horizontal blanking signal is timed to provide 83 columns of unblanking in 80-column mode, and 137 columns of unblanking in 132-column mode. The VT180 is currently programmed so that the three or five extra columns are blanked by terminate. In normal screen mode, this termination forces the beam to black, but in reverse screen, termination forces the beam to the screen background intensity. This means that in reverse screen mode, the last character that can fit on the screen is three or five characters in from the right edge of the illuminated screen. Because hardware blanking allows 83 or 137 columns on the screen, future program developments may allow the microprocessor to format the screen RAM for this ability. The main adjustment is to the position of the terminator and address bytes relative to the starting location of the line. Terminate, as the first character in the line, creates short lines during the vertical blanking interval to conserve memory while maintaining synchronization of the line address system.

6.5.12.11 Video Input and Output – The following paragraphs briefly describe the operation of the terminal controller video input and output circuits.

Direct Drive Video
The two video outputs from the DC012, video out 1 and video out 2, are combined with the vertical blank signal in two open collector nand gates of the direct drive generator. The outputs of the open collector gates are wire-ANDed with graphic 1 and 2 IN from any option board that may be present. The combined video and graphic signal is used to control the conduction of a transistor (Q4) to produce four different voltage levels, which are sent via the PC board fingers to the video monitor to vary the intensity of the screen display. The four voltage levels represent the four levels of intensity visible on the screen: black, dim, normal, and bright.

Composite Video Out
The combined video and graphic signal, along with the composite sync signal from the DC011, is used to control conduction of a transistor (Q2) in the same manner as described for direct drive video.

The result is a 75 ohm output (J9) from the terminal controller module consisting of four intensity levels (including black) and composite sync. This signal can directly drive a standard video monitor, or sync can be extracted to synchronize an external device for input to the terminal. The output is dc coupled. Although the use of dc coupling is not in strict agreement with EIA specification RS-170, this presents no problem with most monitors because they are usually ac coupled.

Video In
The video input stage terminates a standard video signal in 75 ohms. The video input is amplified by a linear biased transistor (Q5) and sent via the PC board fingers to the video monitor. The video input affects only the display on the internal monitor; it does not appear at the composite video output.

6.5.12.12 Intensity Control – The video input and output circuits can produce a range of voltages (as compared with circuits that can produce only two values, white or black levels for example). To do this they are biased into linear operating conditions. Because of the high power dissipation that results, the video circuits use discrete transistors.

Direct drive video is the output from the terminal controller to the video monitor's cathode driver transistor. It is a combination of video out 1 and 2 signals from the video processor, and by means of a transistor Q3, the signal from the video input (analog video in J9). The monitor already receives horizontal and vertical deflection signals directly from the terminal controller, so the terminal's video input only requires picture information. If the blanking level on the video input is greater than zero volts, the screen background intensity cannot be black. Note that composite sync on the input is also ignored by the terminal controller, because the terminal's timing is produced entirely by a crystal and cannot be synchronized to external signals. External sources may be synchronized with the composite sync signal that appears at the output jack (J9).

Transistors Q3 and Q4, in parallel, are one amplifier with common emitter and collector resistors. The collector load of the parallel transistors is the input impedance of the monitor to ground in parallel with a five resistor ladder network. The resistor inputs come from digital to analog latches via open collector buffers. The D/A latches are written into as an I/O device by the microprocessor. In set-up mode, the 8080 microprocessor uses the up and down cursor keys as inputs to a 5-bit software up-down counter. At each vertical reset, the microprocessor writes the current contents of the counter into the latch. Thus there are 32 possible intensity levels available, controlled from the keyboard, and frequently updated to minimize the effects of soft errors. Note that the variable intensity only applies to the internal monitor.

6.5.13 Microprocessor – Video Processor Interface

The microprocessor communicates with the video processor in the following ways.

1. During set-up, the microprocessor reads the set-up specifications and writes them into the DC011 and DC012 to establish screen attributes.

2. The contents of the screen RAM directly control the display of the lines and characters. This region of memory contains the displayable characters, their attributes, the line attributes, and the addresses that link one line to the next. The microprocessor modifies and updates this information in the intervals between DMAs. During each DMA, the video processor copies one line of characters from the screen RAM for display on the screen.

3. During smooth scrolling, the microprocessor updates the scroll latch in the DC012.

6.5.13.1 Screen Memory Organization – Three bytes of control data are located at the end of each line of characters. The first byte, called the terminator, is 7FH and is a unique character that the video processor recognizes as the end of the line. (The high bit is not tested by the terminator gate but is set to zero to avoid complications in the attribute circuits.) Five bits of the next byte and all of the last byte are an address pointing to the first character of the next line to be displayed. The three remaining bits in the first byte define the line attributes of the line pointed to by the address. The high bits of the address are hardwired at the address latch so that when vertical reset clears the address counter, it will point to the ROM-RAM boundary at 2000H.

During power-up or reset the microprocessor writes terminators and addresses into the screen RAM according to the specified line length and refresh rate. The 50/60 Hz refresh choice causes the microprocessor to arrange fill lines to place the beginning of the display in the right time slot relative to the vertical reset and vertical blanking signals. The line length determines the locations of the control bytes. For 80 column lines, the memory space is arranged in 83-byte intervals; for 132 columns, the interval is 135.

The memory organization for 80 column, 60 Hz mode is shown in Figure 6-20. Location 2000H is the start of the RAM space. When vertical reset resets the DMA address counter in the video processor to zero, the counter latch points to this location. The first 18 bytes are fill lines. Byte 2 is the only one written differently when 50 Hz refresh is selected. The change causes a longer fill time during the longer vertical blanking interval.

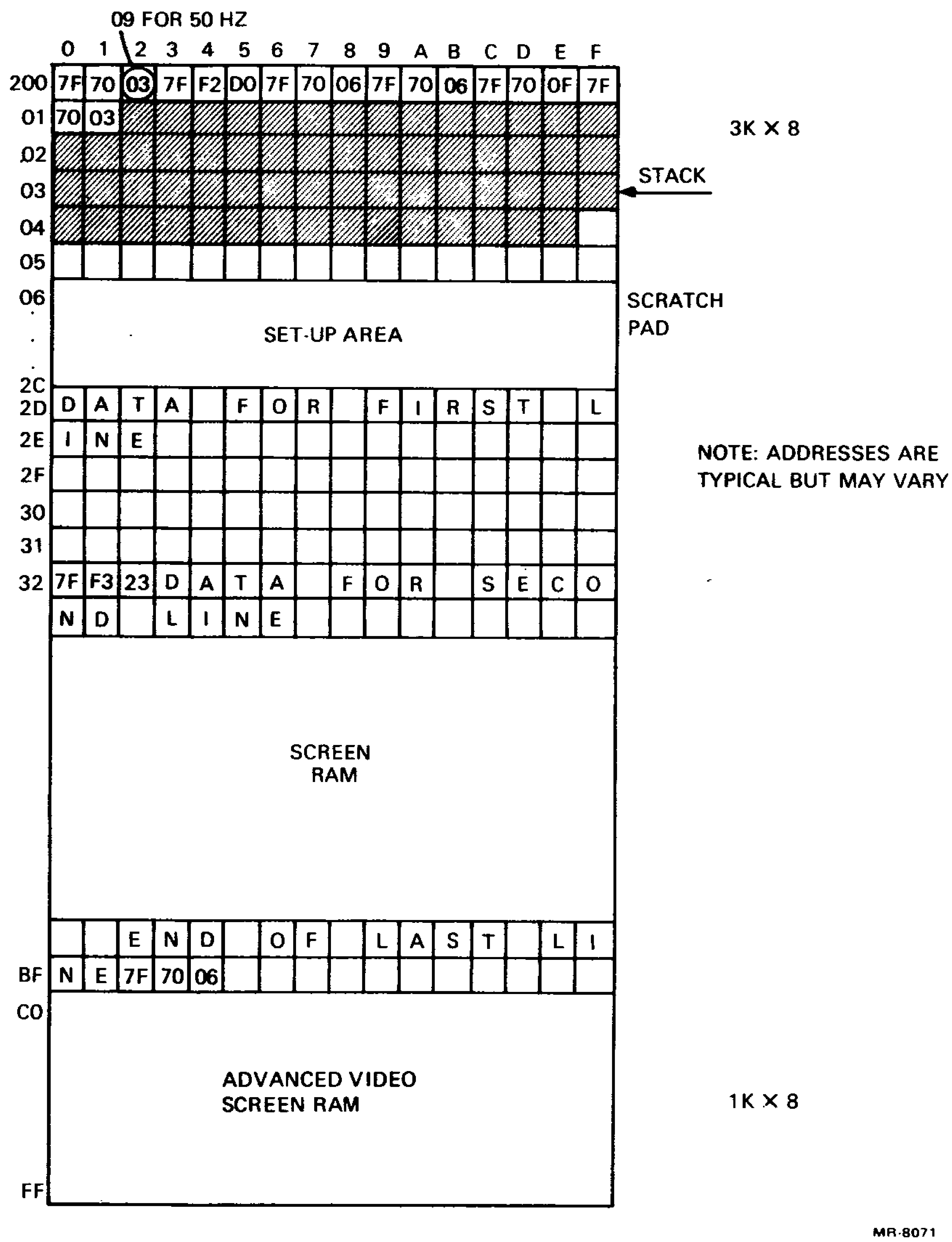


Figure 6-20 Screen RAM Organization – 80 Column, 60 Hz

About 700 bytes of RAM are reserved for the microprocessor stack, scratchpad, and set-up areas. The rest of the 3K RAM is devoted to screen information. At program start, the microprocessor reads the contents of the NVR into the set-up area. Then the microprocessor reads the set-up parameters, erases the screen area, and writes in terminator and address/attribute bytes at the selected line length intervals. The address at the end of each line points to the first location of the next line. At start-up, this is the next physical location. The end of the last line points to a fill line, which points to itself. The fill line repeats until vertical reset.

6.5.13.2 Line Organization – In 132-column mode, 25 lines are set up in the RAM for a 24 line screen, and 15 lines are set up for a 14 line screen. With the advanced video option, 25 lines are set up for either 80 or 132 column lines. Except during a smooth scroll, only 24 lines are seen. But the microprocessor keeps the twenty-fifth line erased in reserve, and when a scroll takes place, the twenty-fifth line becomes visible as the new top or bottom line (depending on scroll direction). All new characters after the command that caused the scroll, go into this line. In preparation for a full screen scroll up, the microprocessor writes the address of the repeating fill line into the twenty-fifth line pointer as well as the twenty-fourth line pointer. This saves processing time during the address rearranging that is a part of each scroll.

The line organization changes when the first scroll occurs. Pointer addresses are revised any time a line is added to or removed from the screen. The extra line is used whenever the screen needs to be scrolled up or down. Then the extra line is displayed; and the old top or bottom line is scrolled off screen, erased, and made available as the new twenty-fifth line.

6.5.13.3 Scrolling Region – A scrolling region may be established on the screen on a horizontal line basis, within which data may be inserted or lines scrolled without affecting the positions of data outside the region. Only one region may be defined at a time, but it may be repeatedly redefined. Full screen scrolling is a special case in which the region margins and the screen margins are the same. A control sequence defines the region by specifying the line numbers of the top and bottom of the region. When the control sequence arrives, the microprocessor stops taking characters from the silo and waits for the current scroll to end. It then checks the parameters for legality (top less than bottom, bottom less than 14 or 24). If they are bad, the sequence is ignored and the next character is taken from the silo. If they are good, they are stored in locations labeled top and bottom. Then, starting at the pointer address on the last fill line, the microprocessor sets the fill line's scroll attribute bit to scroll or no scroll depending on the specification for top margin. The microprocessor then jumps to the end of the addressed line, setting its scroll attribute bit. The microprocessor continues down through the screen RAM until it reaches the top line of the scrolling region. It sets that attribute bit to scroll. Jumping down through the region, the microprocessor continues setting line attributes to scroll until it reaches the bottom line in the scrolling region. From there to the end of the screen it sets the bit to no scroll.

6.5.13.4 Cursor – The microprocessor keeps a running account of the cursor position. It starts at the reset position, line 1 – column 1 (top left corner) and responds to any change in position that might result from receiving a new character, a cursor position command, a line feed, etc. The microprocessor calculates the appropriate screen RAM address from the combination of previous line and column plus change in position, or from the specified line and column in a direct cursor address (DCA) control sequence. The microprocessor then records the current setting of the base attribute bit of the character at that address and then periodically inverts the attribute bit, showing the operator that the cursor is located at the spot on the screen where the attribute appears and disappears.

When a line scrolls on the screen, its location in RAM remains the same. To keep the cursor at the same screen location as before, representing the cursor moving down through the lines, the microprocessor calculates a new address for the cursor at the same column number but in the RAM location corresponding to the next line. Then, after resetting the attribute at the old location to its original value, it records and then toggles the attribute bit at the new location.

The attribute bit that the microprocessor toggles and the appearance on the screen depend on the set-up selection of the cursor attribute and on the absence or presence of the AVO. If the AVO is not installed, the microprocessor toggles the eighth bit in each character word. A set-up selection of reverse video causes the microprocessor to set the DC012 to interpret its base attribute input (REV VID H) as reverse video. If set-up specifies that underline is to be used for the cursor, the DC012 is set to interpret the base attribute as underline instead of reverse. Notice that without the AVO the cursor selection determines the appearance for all characters on the screen that have the attribute asserted. Furthermore, the microprocessor will accept the commands for either reverse or underline to assert the attribute.

With the AVO present, the microprocessor tells the DC012 to interpret the base attribute as reverse video. The cursor selection in set-up determines whether the microprocessor toggles the base attribute bit (eighth character bit) to get reverse video or one of the bits in the AVO RAM to get underline. With the AVO present, cursor selection is independent of attributes and all attributes are available at the same time.

6.5.13.5 Set-Up – The set-up area is a portion of the scratch RAM. It contains 8-bit bytes that are passed between the RAM and the NVR. Here is a list of the set-up area contents. This list is subject to change.

22 bytes	–	Answerback message (20 characters and 2 delimiters)
17 bytes	–	Tabs encoded in bits
1 byte	–	80/132-column mode
1 byte	–	Intensity
1 byte	–	Mode byte for PUSART
1 byte	–	On-line/local
1 byte	–	Switchpack 1 (scroll, auto repeat, screen, cursor)
1 byte	–	Switchpack 2 (bell, keyclick, ANSI/VT52, XON/XOFF)
1 byte	–	Switchpack 3 (US/UK #, wraparound, new line, interlace)
1 byte	–	Switchpack 4 (parity sense, parity, bits/character, power)
1 byte	–	Switchpack 5 (STP – visible only when the option is installed)
1 byte	–	Transmit baud rate
1 byte	–	Receive baud rate
1 byte	–	Parity
1 byte	–	Checksum for NVR

When the SET-UP key is pressed, the silo locks and any scroll in progress is allowed to finish. Now the 25th line (Extra) is available for one of the lines at the bottom of the screen. Another 135 bytes are available as line Extra2 for use as the other of the two bottom lines or for the NVR buffer area and the WAIT message displayed during NVR operations. Another 125 bytes are the set-up screen RAM. They store the words "SET-UP A" twice (for double-height) and the words "To exit press SET-UP" with the three lines' terminator and address bytes, plus 19 more terminators and addresses for the 19 blank lines in the middle of the set-up screen.

For SET-UP A, the microprocessor performs a routine to fill the line at the bottom of the screen with a ruler. The other free line displays the cursor and letters T to indicate tab positions. Then the microprocessor counts from the beginning of the tab bytes in the set-up area to find the bit corresponding to the column number where the cursor is. If the bit is set, the microprocessor writes the letter T in the current cursor position. Keys (set/clear tab, clear all tabs) on the keyboard can toggle the setting of the bit in the set-up area, and the microprocessor writes or erases the T to agree.

For SET-UP B, the microprocessor displays the data contained in the switchpack and baud rate area by writing corresponding information into the bottom line. Switchpack 5 is only displayed if the option present flag is asserted at the STP. The other free line is not written into but is used to display the cursor position and to display the answerback message when the message is being entered. The switchpack data is changed by a key on the keyboard (toggle 1/0).

The nonswitchpack data is changed by separate keys. These include parameters that display themselves — line/local, displayed in the LEDs, and 80/132 column, seen on the screen. Transmit and receive are displayed numerically. Parity is displayed numerically in later models. Switching between set-up fields and starting reset can also be done with separate keys on the keyboard.

6.6 VT18X CONTROL MODULE DESCRIPTION

The VT18X control module is designed to fit into an option slot of the VT180 expansion backplane to allow the VT100 to function as a personal office computer in addition to its usual function as a satellite terminal to an external host. The module contains a Z80A microprocessor, which gives the terminal the capability to run existing control programs for microprocessor (CP/M) applications.

The VT18X control module has the following general features.

1. 4.0 MHz Z80A CPU.
2. 64K byte dynamic RAM with hardware refresh.
3. Up to 8K byte ROM selected upon power-up and software deselectable and configurable for 2716 type UV EPROMs.
4. Console port for communication with the basic VT100.
5. Serial printer port for Digital printers.
6. Communications port running at a baud rate set through the VT180 set-up mode with full VT131 communications hardware support and a synchronous external clock select mode.
7. General purpose serial port.
8. Communications receive-only interrupts.
9. Real time clock interrupt (13.2 ms).
10. Disk drive controller for up to four 5¼ inch 48 TPI disk drives with MFM recording technique (double-density).
11. All I/O devices are accessible by Z80 I/O instruction only.

Figure 6-21 shows the major logical subunits of the VT18X control module and their relation to the address bus, the data bus, and the I/O connnectors. The function of each logical subunit is described in the following paragraphs.

6.6.1 Z80A CPU

The Z80A is an 8-bit, parallel central processor unit (CPU). The Z80A transfers data and internal state information through an 8-bit, bidirectional data bus (D7–0 H). Memory and peripheral device addresses are transmitted over a separate 16-bit, unidirectional address bus (A15–0 H). Six Z80A outputs are used to control various functions performed by the logic circuits on the VT18X control module. Three inputs from the logic circuits on the VT18X control module are used for CPU control.

The Z80A internal registers contain 208 bits of read/write memory that are accessible to the programmer. These registers include two sets of six general purpose registers, which may be used individually as either 8-bit registers or as 16-bit register pairs. In addition, there are two sets of accumulator and flag registers. A group of exchange instructions makes either set of main or alternate registers accessible to the programmer. The Z80A also contains a stack pointer, a program counter, two index registers, a refresh register (counter), and an interrupt register. The CPU requires only a single +5 V power supply source. All output signals are fully decoded and timed to control the memory and I/O devices. The Z80A block diagram is shown in Figure 6-22.

The Z80A operates at 4.0 MHz with no wait states for RAM, one wait state for ROM, and those wait states automatically inserted by the CPU for I/O instructions. All I/O is done by Z80A input or output instructions (no memory mapped I/O). Resets are done automatically upon power-up or can be done explicitly through the set-up reset sequence of the VT180. (The VT180 must be firmware operational.) Applications running with hardware dependencies are not supported. Only CP/M operating system calls for I/O are supported.

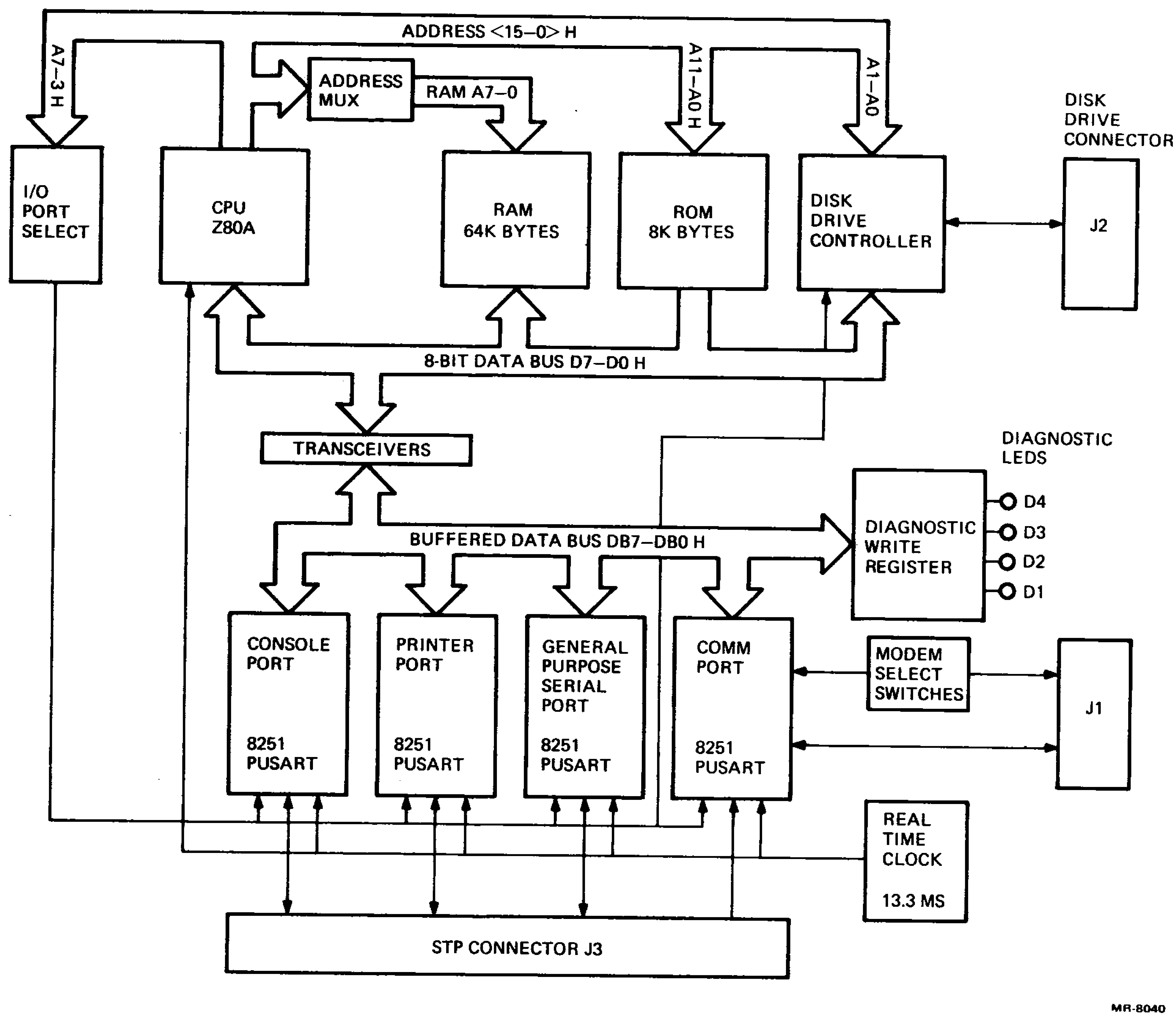


Figure 6-21 VT18X Control Module Block Diagram

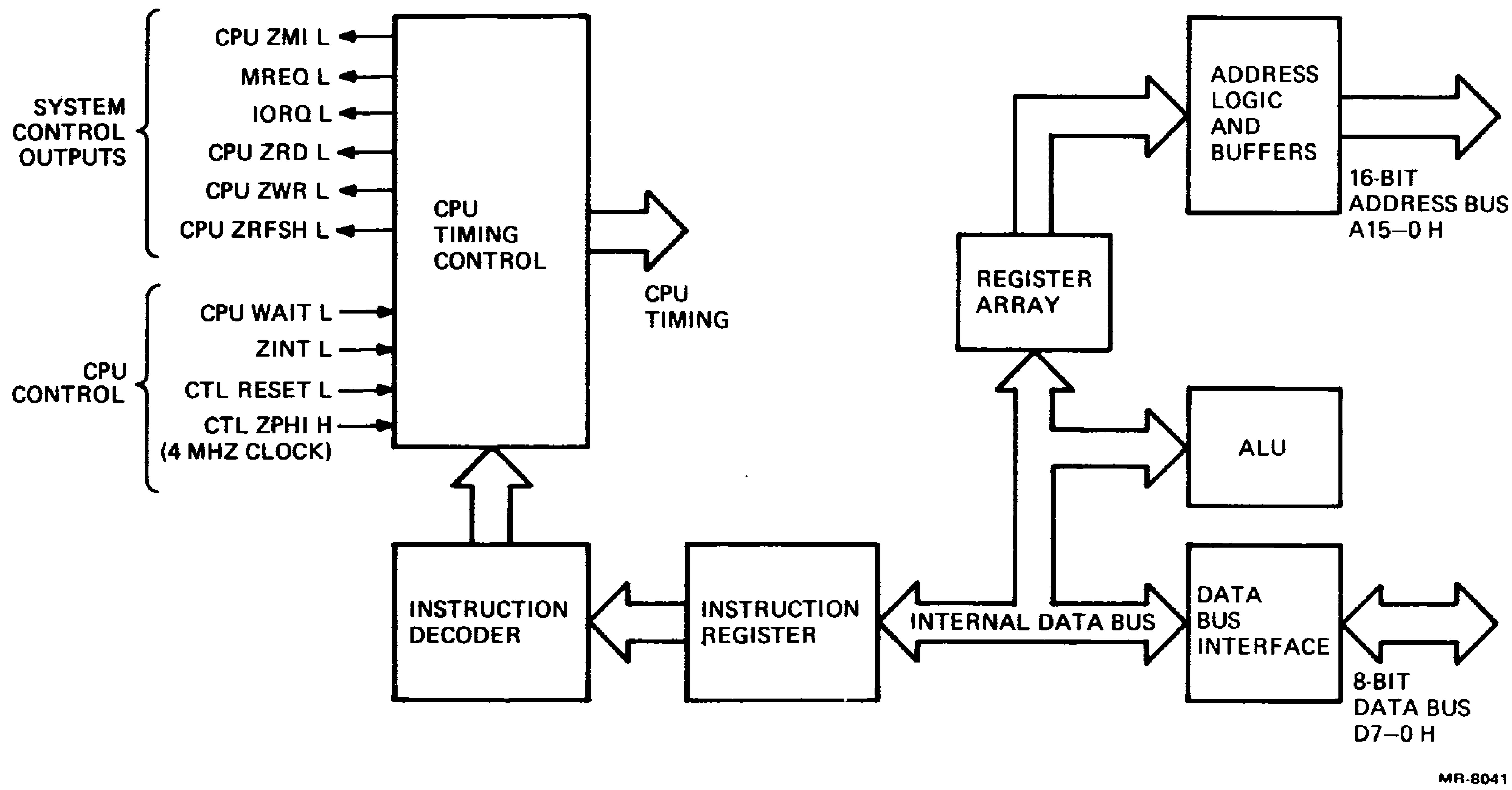


Figure 6-22 Z80A CPU Block Diagram

6.6.2 Interrupts

The CPU accepts interrupts from the four 8251A PUSARTs and the real time clock (RTC). Figure 6-23 shows the relationship of the interrupting devices to the CPU and the address and data buses.

A PUSART will interrupt the CPU whenever its receiver buffer contains a character that is ready for input to the CPU. A CPU restart to location 10H occurs upon detection of an interrupt signal from any of the four PUSARTs. The CPU must then poll the PUSARTs to determine the source of the interrupt.

The real time clock signal (CYARTC H) interrupts the CPU every 13.3 ms and causes a restart to location 18H. RTC interrupts take precedence over PUSART interrupts and are reset by a dummy read to location 90H. All interrupts, including the RTC, are turned off while doing a disk drive I/O. Therefore, the RTC cannot be used for a time of day clock and is used only for communications control signal timing.

The interrupt output signals from the four PUSARTs and RTC are ORed together and become the maskable interrupt (INT) input to the CPU. Interrupts are implemented by the CPU as mode 0 maskable interrupts. A maskable interrupt is one that must be enabled in software in order to operate. In mode 0 interrupt operation, the interrupting device places a restart instruction on the data bus, which is then acted on six times by the CPU. The restart instruction causes an unconditional jump to location 10H for a PUSART interrupt or to location 18H for an RTC interrupt.

Interrupt Request/Acknowledge Cycle

The CPU samples the ZINT L signal with the rising edge of the last clock cycle (CTL ZPHI H) at the end of any instruction. When an interrupt is accepted, the CPU ZMI L cycle is generated. During this CPU ZMI L cycle, IORQ L becomes active to indicate that the interrupting devices can place an 8-bit vector on the data bus. The CPU automatically adds two CPU WAIT L states to this cycle.

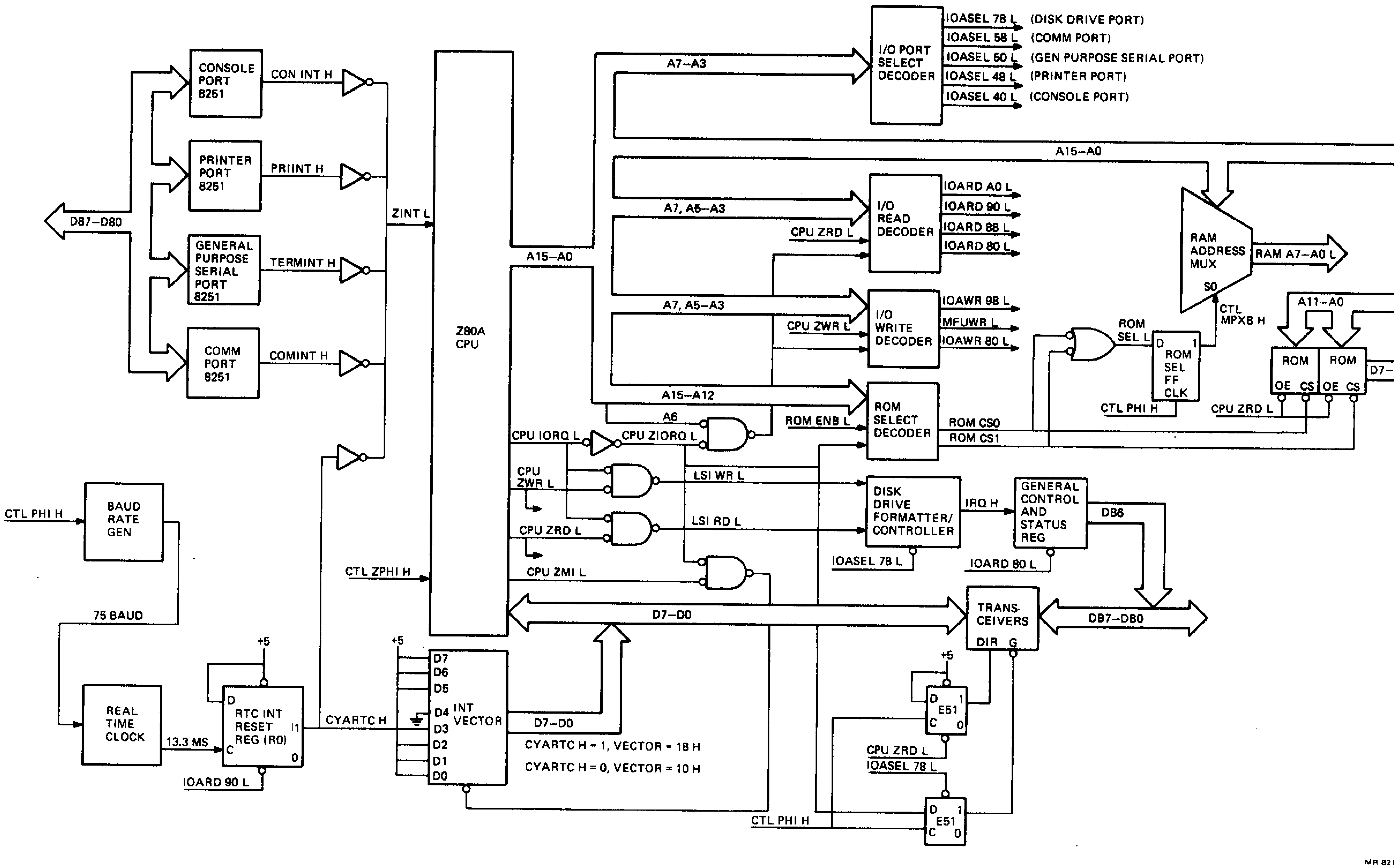


Figure 6-23 Microprocessor Interrupt Block Diagram

6.6.3 64K Byte RAM

The VT18X control module has 64K bytes of directly addressable RAM available for CP/M. The RAM is comprised of eight 64K by 1 parts whose address and control lines are connected in parallel. The bidirectional RAM data lines are connected to the CPU via the data bus (D7–D0 H). The block diagram in Figure 6-24 shows the RAM and its relationship to the CPU and associated logic.

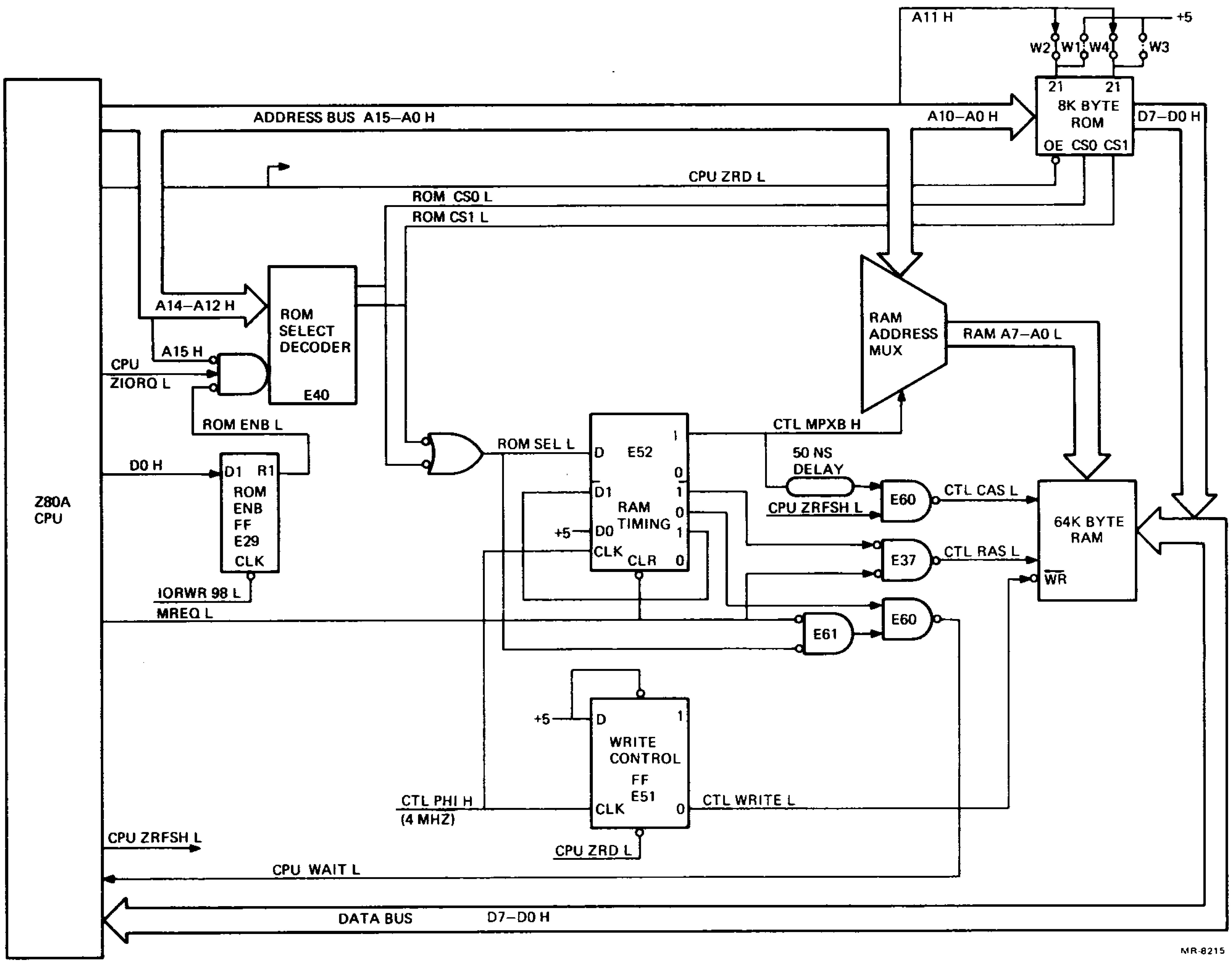


Figure 6-24 RAM and ROM Block Diagram

The RAM is 7-bit hardware refreshed by the CPU ZRFSH L signal. The RAM is refreshed during the third and fourth CTL PHI H clock pulses of a machine cycle one (M1) of an instruction op code fetch. CPU ZRFSH L together with MREQ L indicates that the lower seven bits of the address bus (A6–A0 H) can be used as a refresh address to the RAM.

The RAMs used are 64K parts with 128-cycle refresh. Only RAMs with the following Digital part numbers can be used.

21-18467-01
21-18470-01
21-18472-01

Before operating the RAM, a minimum of eight RAS cycles must be given to ensure data integrity. This can be accomplished by eight op code fetches or dummy reads from the RAM.

Memory Read or Write Cycle

A memory read or write cycle begins after the CPU places the contents of the program counter on the address bus (A15–A0 H). Approximately one-half clock cycle later, MREQ L goes active to indicate that the address bus holds a valid address for a memory read or write operation. MREQ L together with the output of the RAM timing FF D1 produces the row address strobe (CTL RAS L). The column address strobe (CTL CAS L) is generated 50 ns after CTL RAS L becomes active.

The read signal (CPU ZRD L) is connected to the clear input of the write control FF. In a read operation, CPU ZRD L goes active after the first CTL PHI H clock pulse and clears the write control FF. CTL WRITE L becomes active and allows the RAM data to be placed on the data bus.

In a memory write cycle, the write control FF is set as it was in a read cycle. However, in a memory write cycle CPU ZRD L is inactive and does not clear the write control FF. CTL WRITE L, therefore, is active and allows the data (D7–D0 H) to be written into the RAM location specified by address bits A15–A0 H.

6.6.4 8K Byte ROM

The VT18X control module contains space for up to 8K bytes of ROM (two 24-pin sockets). Figure 6-24 shows the ROM and its relation to the address bus, data bus, and associated logic. The ROMs supported are of the 2716 (2K × 8) and 2732 (4K × 8) pin out variety, with access times less than or equal to 450 ns.

The ROM contains diagnostics for the module, bootstrap code for CP/M, and a pass-through mode, which passes data between the VT180 and the communications port. (After ROM is disabled, the pass-through terminal mode is only available as an application run under CP/M.) The ROM is enabled upon power-up at location 0000 H and can be enabled or disabled by the least significant bit (D0 H) in port 98H. When the ROM is disabled, the full 64K bytes of RAM can be addressed. Figure 6-25 shows the 64K byte memory map with the ROM enabled and disabled.

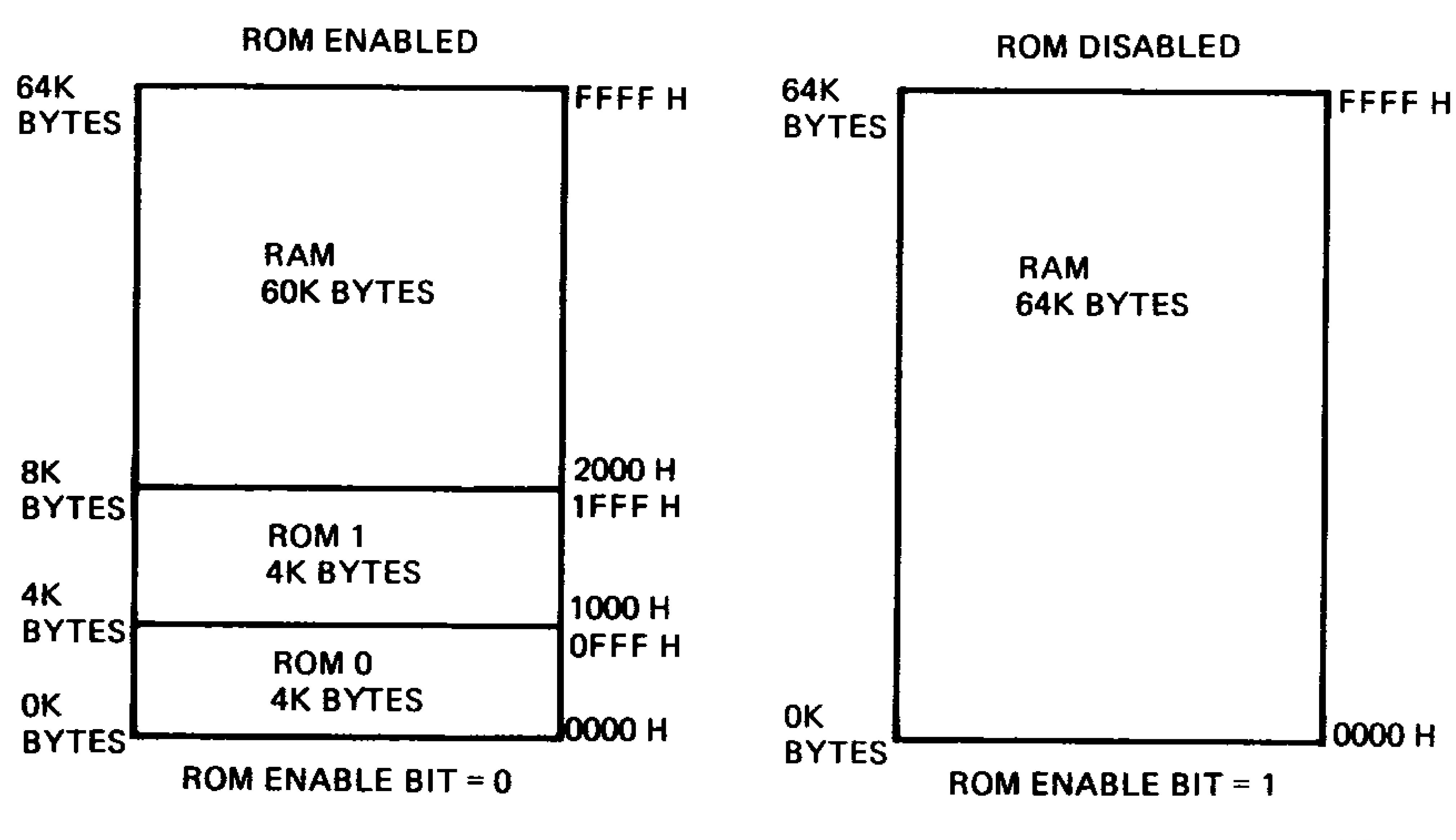


Figure 6-25 64K Byte Memory Map

ROM Read Operation
Address bits A14–A12 H are used by the ROM select decoder to select the ROM to be read. If bits A14 through A12 are low, ROMCS0 L is active and ROM 0 is selected. If bit A12 is high and A14–A13 are low, ROMCS1 L is active and ROM 1 is selected. Address bit A15 L, together with CPU ZIORQ H and ROM ENB L enable the ROM select decoder. D0 H clocked into the ROM enable FF by IOAWR L will cause ROM ENB L to become inactive and disable the ROM select decoder. When D0 is low, it causes ROM ENB L to become active and enable the ROM when clocked by IOAWR L. The output of the ROM select decoder, ROMCS0 L or ROMCS1 L is sent to the chip select input of the ROMs and to an OR gate to produce ROM SEL L. ROM SEL L is the D input of a RAM timing FF. When ROM SEL L is clocked into the FF by CTL PHI H, CTL MPXB goes low and disables the RAM address multiplexer. CPU ZRD L then enables the ROM to output the data (D7–D0 H) from the location specified by the RAM address bits A10–A0 H.

6.6.5 Console Port
The console port on the VT18X control module communicates with the terminal controller module via the VT180 paddle board installed in the STP connector. The console transmit and receive data, transmit and receive clocks, and modem control signals are connected to a 16-pin IC socket (J3) on the VT18X control module. These signals are then routed to the terminal controller module through a ribbon cable connected to IC socket (J2) on the VT180 paddle board. Figure 6-26 shows the I/O ports and their relation to the I/O connectors, the data bus, and control logic. Transmit and receive baud rates are fixed by the 15.7 k baud clock (CON CK H) input on pin 3 of connector J3. This console clock is obtained from the video timing circuit (DCO11) on the terminal controller module.

RS-232C signals supported by the console port include transmit data (CON XMIT DATA H), receive data (CON REC DATA 1 H), and data terminal ready (CON DTR L) from the terminal controller module for control. Software must support XON/XOFF protocol for this port.

Console Port Functional Description
Address bits A5–A3 and A7–A6 from the CPU are used for select and enable inputs by the I/O port select decoder. The console PUSART is enabled when the CPU places address 40H on the address bus. The I/O port select decoder uses address bits A7–A3 of address 40H to generate IOASEL 40 L. This signal is applied to the select input to enable data to be written into or read from the console port data and control and status registers.

Address bit A0 applied to the console PUSART control/data (D/D) input is used, in conjunction with the write (LSIWR L) and read (LSIRD L) signals, to inform the PUSART that the word on the data bus (DB7–0 H) is either a data character, control word, or status information. If A0 is high, the word on the data bus is control and status information. If A0 is low, the word on the data bus is data information.

The LSIWR L signal obtained by ANDing the CPU ZWR L and IORQ L signals asserted by the CPU is used to inform the console PUSART that it is outputting data or control words. The CPU asserts LSIRD L when it reads data or status information from the console PUSART.

Data transmitted by the console PUSART is taken from the data bus in parallel and converted to a serial bit stream by the PUSART's transmitter buffer. The transmitter buffer inserts the appropriate bits (based on communications techniques) and a composite serial stream of data (CON XMIT DATA H) is clocked out by CON CK H to pin 10 of connector J3. CON XMIT DATA H is also sent to the console loopback multiplexer to be used as the received data input to the console PUSART during diagnostic testing. The transmitted data output on pin 10 of J3 is sent to the received data input of the communications PUSART on the terminal controller module.

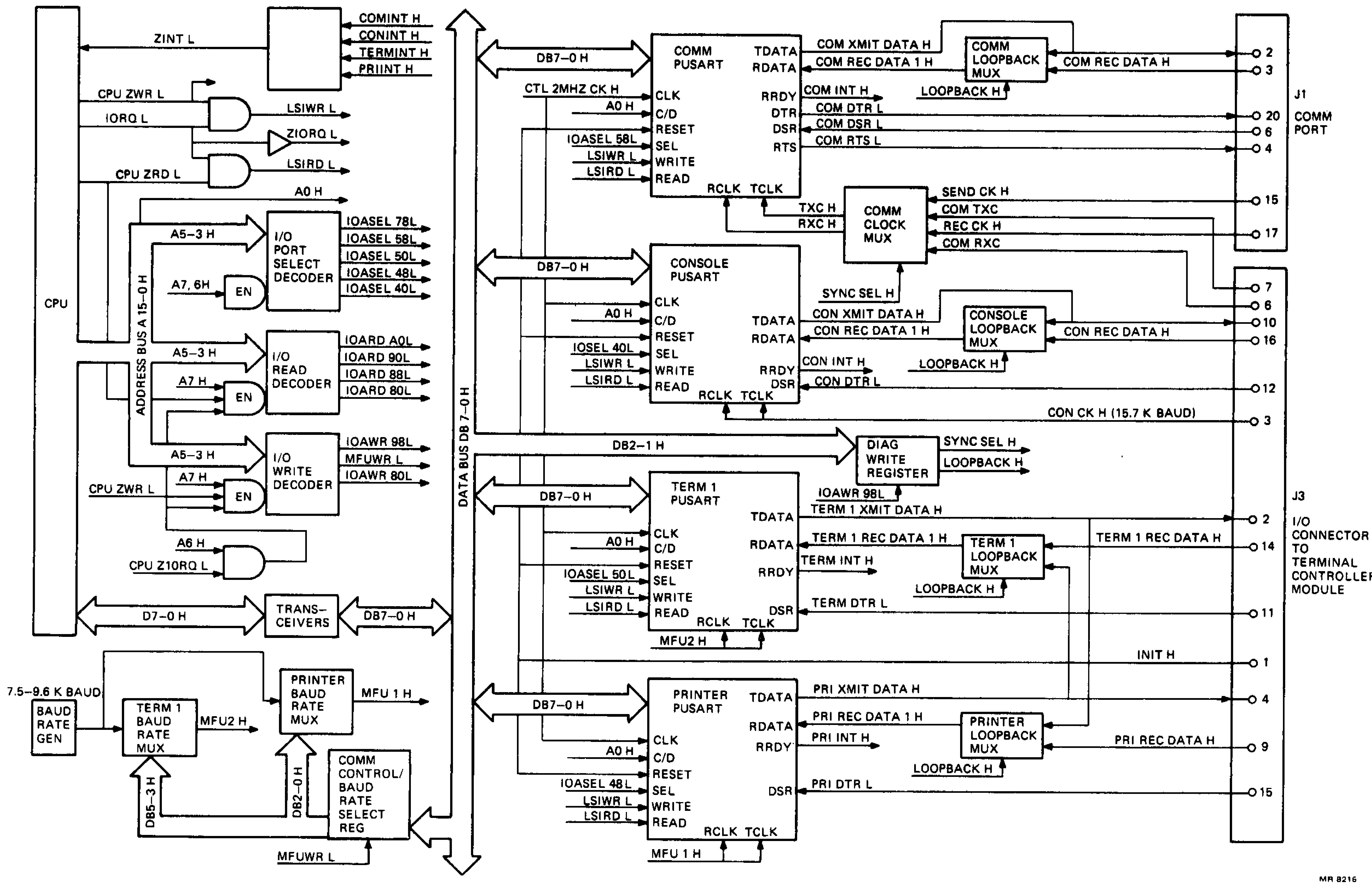


Figure 6-26 I/O Port Control Block Diagram

Data (CON REC DATA H) is received by the console PUSART from pin 16 of I/O connector J3 via the console loopback multiplexer. The received data for the console PUSART is data transmitted by the communications PUSART on the terminal controller module. The received serial data is clocked into the console PUSART by CON CK H, converted to parallel format in the receiver buffer, and checked for bits or characters that are unique to the communications technique. The console PUSART then asserts CON INT H to inform the CPU that the receiver buffer contains a valid character ready for input to the CPU.

The console data terminal ready (CON DTR L) connected to the data set ready (DSR) input of the console PUSART is obtained from the data terminal ready (DTR) output of the communications PUSART on the terminal controller module.

6.6.6 Communications Port

The communications port (Figure 6-26) is used to communicate with a host computer when the VT180 is operated in terminal mode. It has full modem support and supports the same signals as the VT131. United States and European full- and half-duplex modems can be supported by RS-232C (V.24/V.28) physical interface conforming to CCITT V.21, V.22, and V.23. This port supports break detection. The transmit and receive baud rate clocks for this port are derived from the baud rate generator on the terminal controller module. Therefore, the transmit and receive baud rates selected in the VT180's set-up mode are the transmit and receive baud rates for this port and must be set to match the transmit and receive baud rates of the host computer. Baud rates supported are 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 9600, and 19.2 k baud. Any and all protocols to be supported by this port, other than pass-through mode, are run as applications under CP/M.

The communications port contains a ten position switchpack (E22), which must be set to permit operation with a particular modem. Figure 6-27 shows the switches and the modem signals that must be switched. Table 6-9 describes the various modems supported by the communications port and the switch configuration required for each modem.

The communications port signals are connected to a 25-pin, D-type EIA connector residing on the VT18X control module.

Table 6-9 Communication Modem Switch Configuration

Modem Type	Switch Settings* S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
Bell 103-X 300B, FDX, ASYNC, 2-W, 113-X	C	C	O	C	O	C	O	C		O
Bell 202-X 1200 B, FDX, ASYNC, 2-W,	C	C	O	C	O	C	O	C		O
1200B, BDX, ASYNC, 4-W	C	C	O	C	O	C	O	C		O
Bell 212A 1200B, FDX, ASYNC, 2-W**	C	C	O	C	O	C	O	C		O

*Switch S9 not used. C = Closed, O = Open
**S10 must be closed when using the speed select feature of the Bell 212A.

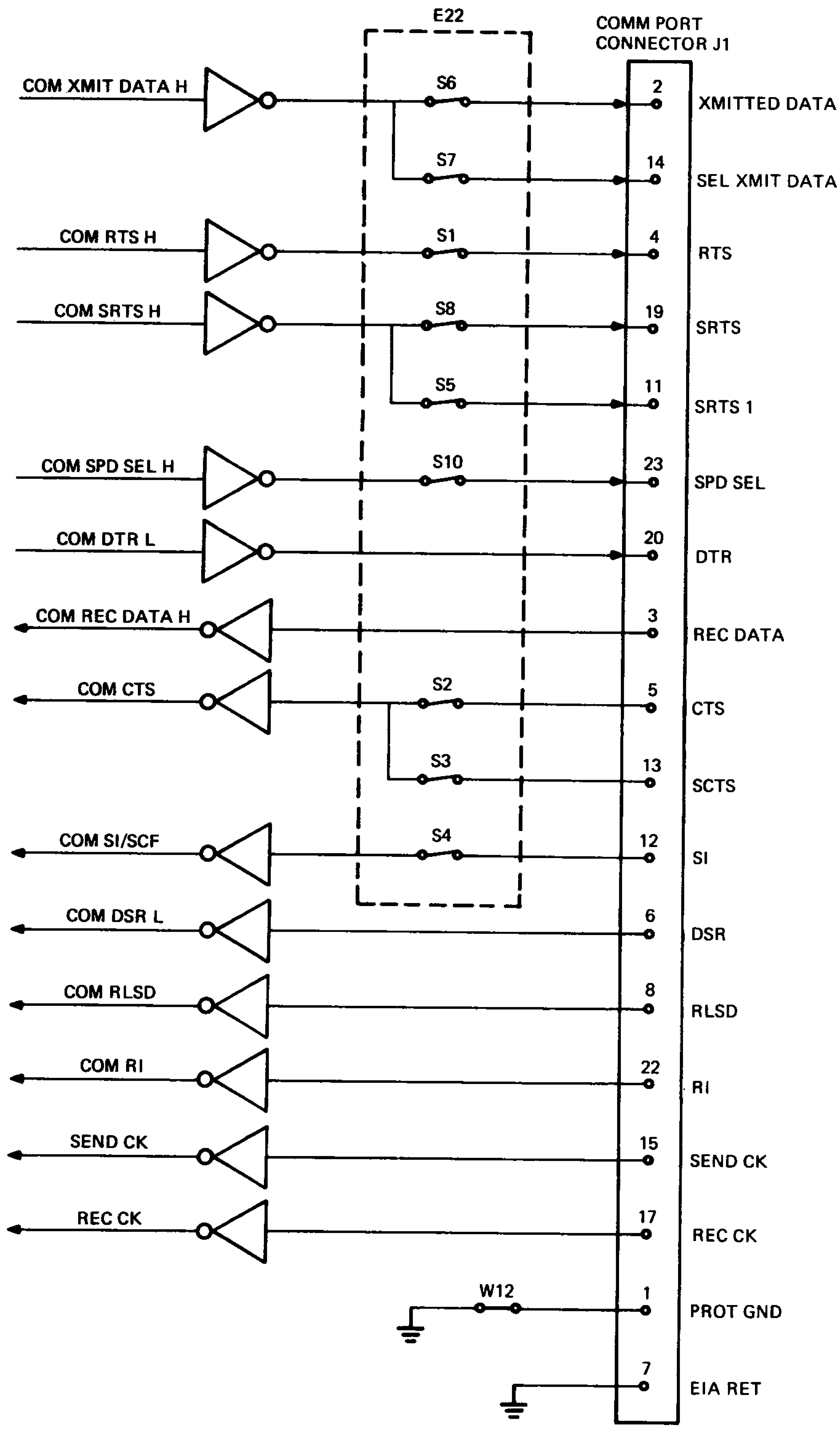


Figure 6-27 Communications Port Modem Switches

Communications Port Functional Description

The communications PUSART is enabled for reading or writing by IOASEL 58 L from the I/O port select decoder when the CPU places address 58H on the address bus. Address bit A0, together with write (LSIWR L) or read (LSIRD L) are used to perform the same function for the communications PUSART as they did for the console PUSART. If A0 is high, the word on the data bus is control and status information. If A0 is low, the word on the data bus is data information.

Serial data transmitted (COM XMIT DATA H) is clocked out of the PUSART by TXC H and routed to pin 2 of the communications port connector (J1). The transmitted serial data is also applied to the communication loopback multiplexer to be used as the received data input to the communications PUSART during diagnostic testing.

Serial data (COM REC DATA H) is received from the host computer via pin 3 of the communications port connector (J1) and clocked into the communications PUSART by RXC H. The communications PUSART converts the serial data to parallel data, checks for bits and characters that are unique to the communications techniques, and then asserts COM INT H to inform the CPU that the receiver buffer contains a valid character ready for input to the CPU.

The communications PUSART receives its transmitter (TXC H) and receiver (RXC H) clocks from the communications clock multiplexer. The transmitter and receiver clock inputs to the clock multiplexer are obtained from two sources. SEND CK H and REC CK H are received from the host computer via pins 15 and 17 or communications port connector (J1). COM TXC and COM RXC are received from the baud rate generator on the terminal controller module via pins 6 and 7 of connector J3. The status of SYNC SEL determines which set of clocks will be used by the communication PUSART. SYNC SEL is high when bit 2 (DB2) of the diagnostic write register (address 98 H) is programmed to one. When SYNC SEL is high, the host computer supplies the transmitter and receiver clocks for the communications PUSART. SYNC SEL is low when the VT180 is operated in personal computer mode and the transmitter and receiver clocks are supplied by the baud rate generator on the terminal controller module.

The three modem control signals (COM RTS L, COM DSR L, and COM DTR L) are always programmed at power-up to allow normal full-duplex operation with some modems when a standard EIA cable is installed between the modem and the VT180.

6.6.7 Printer Port

This is a general purpose printer port (Figure 6-26), which provides an RS-232C interface compatible with Digital printers. EIA signals supported are transmit data, receive data, and data terminal ready. Software programmable baud rates to be supported are 75, 150, 300, 600, 1200, 2400, 4800, and 9600. Software programmable character formats supported are 5, 6, 7, and 8 bits/character with 1, 1½, and 2 stop bits/character. Software should support XON/XOFF protocol for this port. The 25 D-type pin EIA printer connector physically resides on the VT180 paddle board in the normal printer port location and, just as previous VT100 printer ports have, uses a null modem cable to attach to a printer.

Printer Port Functional Description

The printer PUSART is enabled for reading or writing by IOASEL 48 L when the CPU places address 48H on the address bus. Address bit A0 with write (LSI WR L) or read (LSIRD L) is used to perform the same functions for the printer PUSART as it did for the console PUSART. If A0 is high, the word on the data bus is control and status information. If A0 is low, the word on the data bus is data information.

Serial data transmitted (PRI XMIT DATA H) is clocked out of the PUSART by MFU1 H and routed to pin 4 of I/O connector J3. The transmitted serial data is also applied to the term 1 loopback multiplexer to be used as the received data input to the term 1 PUSART during diagnostic testing.

Serial data (PRI REC DATA H) during normal operation is received from the printer on pin 9 of the I/O connector J3 and routed through the printer loopback multiplexer to the receiver data input of the printer PUSART. During diagnostic testing, the transmitted data (TERM 1 XMIT DATA H) from the term 1 PUSART is routed through the loopback multiplexer to become the receiver data input for the printer PUSART. The received serial data is clocked into the receiver buffer of the printer PUSART by MFU 1. The PUSART then notifies the CPU that a character is ready for input by asserting PRI INT H.

The MFU 1 signal is used as both transmitter and receiver clocks for the printer PUSART. Therefore, split baud operation is not supported by the printer port. MFU 1 is the output of the printer baud rate multiplexer whose eight baud rate inputs are obtained from the baud rate generator. The baud rate for MFU 1 H is selected by programming bits 2–0 of the communications control/baud rate select register at address 90H.

6.6.8 General Purpose Serial Port

This port is provided as a general purpose RS-232C interface. Signals supported are transmit data, receive data, and data terminal ready. Software programmable baud rates to be supported are 75, 150, 300, 600, 1200, 2400, 4800, and 9600. Software programmable character formats supported are 5, 6, 7, and 8 bits/character with 1, 1½, and 2 stop bits/character. This port uses the term 1 PUSART (Figure 6-26). The term 1 PUSART transmits and receives data through connector J4 on the terminal controller module. Note that connector J4 was used as the communications port connector in the VT100. In the VT180, however, J4 is used as a general purpose serial port. Signals are passed between the term 1 PUSART and the general purpose serial port J4 via the VT180 paddle board and ribbon cable connected to I/O connector J3 on the VT18X control module.

General Purpose Serial Port Functional Description

The term 1 PUSART is enabled for reading or writing by IOASEL 50 L from the I/O port select decoder when the CPU places address 50H on the address bus. Address bit A0 with write (LSIWR L) or read (LSIRD L) is used to perform the same functions for the term 1 PUSART as it did for the console PUSART. If A0 is high, the word on the data bus is control and status information. If A0 is low, the word on the data bus is data information.

Serial data transmitted (TERM 1 XMIT DATA H) is clocked out of the PUSART by MFU 2 H and routed to pin 2 of I/O connector J3. The transmitted serial data is also applied to the printer loopback multiplexer to be used as the received data input to the printer PUSART during diagnostic testing.

Serial data (TERM 1 REC DATA H) is received from pin 14 of the I/O connector J3, routed through the term 1 loopback multiplexer, and clocked into the PUSART by MFU 2 H. The term 1 PUSART converts the serial data to parallel data, checks for bits and characters that are unique to the communications techniques, and then asserts TERM INT H to inform the CPU that the receiver buffer contains a valid character ready for input to the CPU.

The MFU 2 H signal is used as both transmitter and receiver clocks for the term 1 PUSART. Therefore, split baud operation is not supported by the general purpose serial port. MFU 2 H is the output of the term 1 baud rate multiplexer whose eight baud rate inputs are obtained from the baud rate generator. The baud rate for MFU 2 H is selected by programming bits 5–3 of the communications control/baud rate select register at address 90H.

6.6.9 Terminal Controller and VT18X Control Module Interconnections

The VT18X control module is connected to the terminal controller module via a 16-pin ribbon cable to the VT180 paddle board. Figure 6-28 shows the signal interconnections and indicates the signal direction through the ribbon cable and paddle board. This interconnection is very important in the operation of the

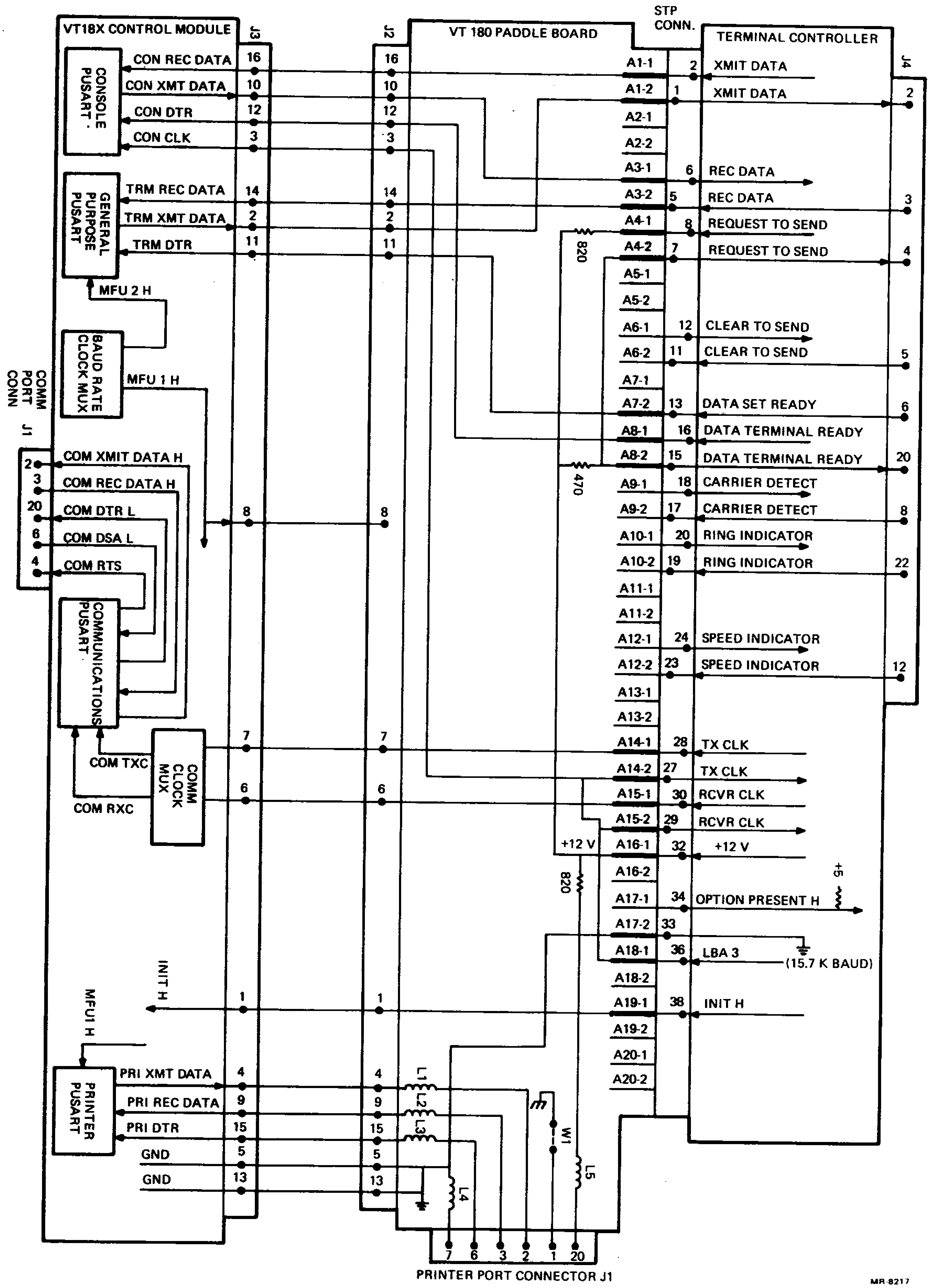


Figure 6-28 Terminal Controller and VT18X Control Module Interconnections

VT180. All four serial ports depend upon signals from the STP connector. Note that the transmit and receive data lines for the communications PUSART and printer PUSART are not routed through the STP connector but instead are routed through individual connectors. The INIT signal from the terminal controller module is also routed through the STP connector to the VT18X control module and is used as a general reset signal (CTL RESET) for all four serial ports and other logic on the module.

6.6.10 Disk Drive Controller

The disk drive interface is designed to control up to four 5¼ inch disk drives. The controller supports double-density drives using a phase-locked loop (PLL) circuit. Etch is also present on the VT18X control module for a state machine data separator, which is suitable for single-density operation, but it is not used. The controller circuits support only soft-sectored, single-sided diskettes.

The disk drive controller converts binary data from the CPU into modified frequency modulated (MFM) data. The MFM data is then transmitted to the disk drive where it is recorded on the diskette. MFM is a magnetic recording method for disk drives in which a clock signal is encoded in the flux transitions recorded on the diskette. When reading data from the diskette, the disk drive controller synchronizes on the data transitions, and with a PLL and MFM decoder, recovers the clock and data.

The disk drive controller data and control lines are routed to a 37-pin, D-type connector (J2) that physically resides on the VT18X control module. Connection from connector J2 to the disk drives is made via a 37-pin shielded cable (BC26K).

6.6.10.1 Disk Drive Controller Functional Description – The disk drive controller is comprised of a disk drive formatter/controller, a phase-locked loop, and associated logic. The functional relationship of the major components is shown in Figure 6-29 and described in the following paragraphs.

6.6.10.2 Formatter/Controller – The disk drive formatter/controller is a 40-pin, MOS, LSI circuit chip (WD1793). The 1793 IC contains a number of registers and other logic, which are used to manage the various functions provided by the formatter/controller. A brief description of the internal registers and associated logic is given in the following paragraphs.

The formatter/controller will accept eleven commands from the CPU. The commands are loaded into the command register to specify the disk drive operation presently being executed. The commands are divided into four types and are described in Paragraph 6.6.14.

Data Shift Register

This 8-bit register assembles serial data from the read data input (RAW READ) during read operations and transfers serial data to the write data (WD) output during write operations.

Data Register

This 8-bit register is used as a holding register during disk read and write operations. In disk read operations the assembled data byte is transferred in parallel to the data register from the data shift register. In disk write operations, information is transferred in parallel from the data register to the data shift register. When executing the seek command the data register holds the address of the desired track position. This register is loaded from or gated onto D7–D0 under processor control.

Track Register

This 8-bit register holds the track number of the current read/write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during diskette read, write, and verify operations. The track register can be loaded from or transferred to D7–D0. This register should not be loaded when the device is busy.

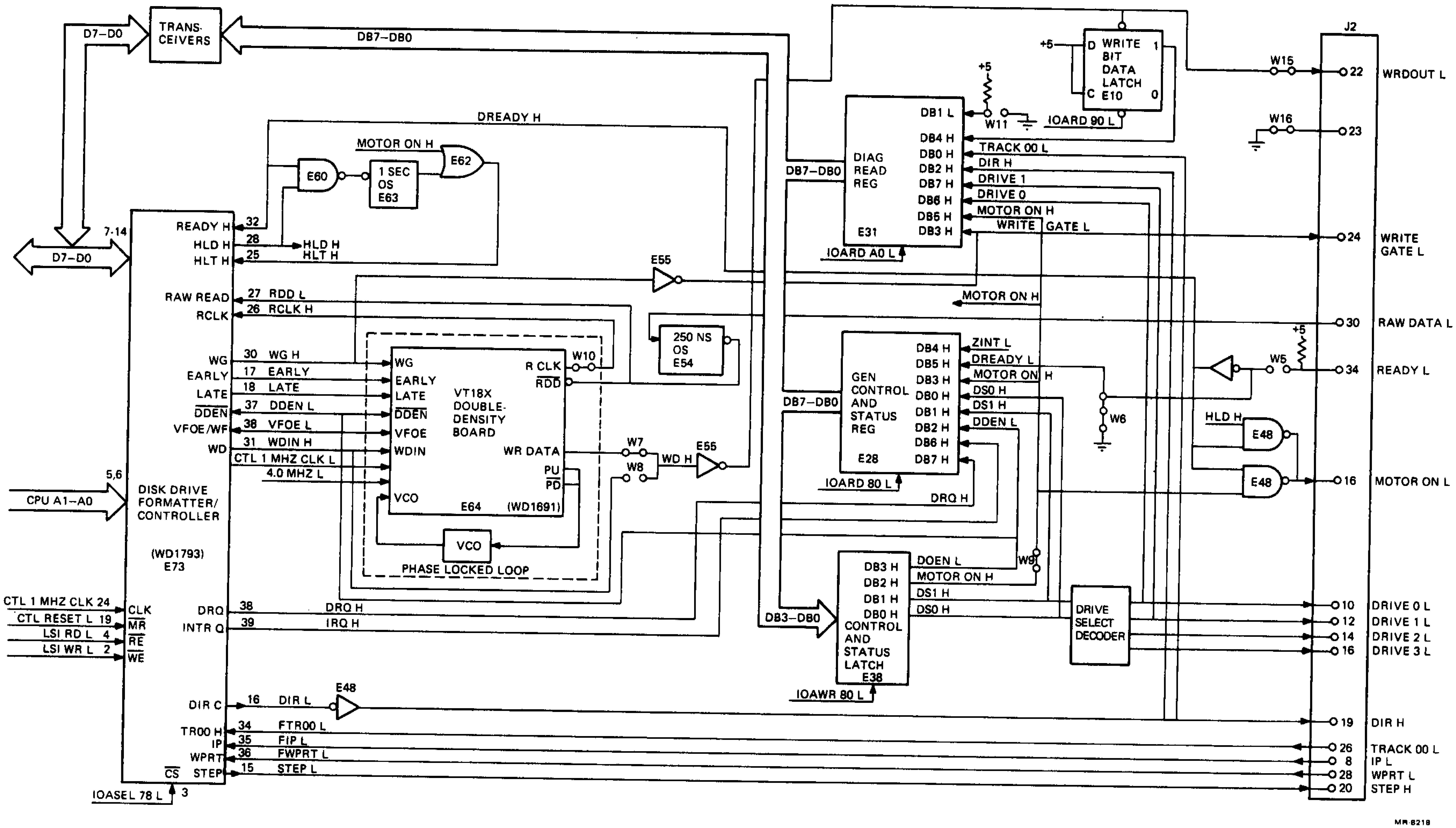


Figure 6-29 Disk Drive Controller Block Diagram

Sector Register (SR)
This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk read or write operations. The sector register contents can be loaded from or transferred to D7–D0. This register should not be loaded when the device is busy.

Command Register (CR)
This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a forced interrupt. The command register can be loaded from D7–D0 but not read onto D7–D0.

Status Register (STR)
This 8-bit register holds device status information. The meaning of the status bits is a function of the type of command previously executed. This register can be read onto D7–D0 but not loaded from D7–D0.

CRC Logic
This logic is used to check or to generate the 16-bit cyclic redundancy check (CRC). The polynomial is: $G(x)=x^{16}+x^5+1$. The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic Logic Unit (ALU)
The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the diskette recorded ID field.

Timing and Control
All computer and disk drive interface controls are generated through this logic. The internal device timing is generated from an external crystal clock (CTL 1 MHz CLK) applied to pin 24.

The formatter/controller has two different modes of operation according to the state of DDEN. When DDEN equals 0, double-density (MFM) is assumed. When DDEN equals 1, single-density (FM) is assumed.

AM Detector
The address mark detector detects IC, data, and index address marks during read and write operations. The input/output signals of the formatter/controller are divided into two basic groups. Signals that are used for CPU interface control and those that are used for disk drive interface control. The signal functions and their pin locations are listed in Table 6-10.

Table 6-10 Formatter/Controller Pin Identification

Pin Number	Pin Name	Pin Symbol	Signal Mnemonic	Function
1	No connection	NC		Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	Master reset	MR	CTL RESET L	A logic low on this input resets the device and loads hex 03 into the command register. The not ready (status bit 7) is reset during MR ACTIVE. When MR is brought to a logic high, a restore command is executed regardless of the state of the ready signal from the drive. Also, hex 01 is loaded into sector register.
20	Power suplies	Vss		Ground
21		Vcc		+5 V ±5%
40		Vdd		+12 V ±5%
Computer interface:				
2	Write enable	WE	LSI WR L	A logic low on this input gates data on D7–D0 into the selected register when CS is low.
3	Chip select	CS	IOASEL 78 L	A logic low on this input selects the chip and enables CPU communication with the formatter/controller.
4	Read enable	RE	LSI RD L	A logic low on this input controls the placement of data from a selected register on the D7–D0 when CS is low.
5,6	Register select lines	A0, A1	CPU A0–A0 H	These inputs select the register to receive/transfer data on the D7–D0 lines under RE and WE control:

A1	A0	RE	WE
0	0	Status reg	Command reg
0	1	Track reg	Track reg
1	0	Sector reg	Sector reg
1	1	Data reg	Data reg

Table 6-10 Formatter/Controller Pin Identification (Cont)

Pin Number	Pin Name	Pin Symbol	Signal Mnemonic	Function
7–14	Data access lines	DAL7–0	D7–D0 H	Eight bit inverted bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by WE or transmitter enabled by RE.
24	Clock	CLK	CTL 1 MHz CLK	This input requires a free-running square-wave clock for internal timing reference, 1 MHz for drives.
31	Write data	WD	WDIN H	A 250 ns (MFM) pulse per flux transition. WD contains the unique address marks as well as data and clock.
32	Ready	READY	DREADY H	This input indicates disk readiness and is sampled for a logic high before a read or write operation is performed. If ready is low, the read or write operation is not performed and interrupt is generated. Type I operations are performed regardless of the state of ready. The ready input appears in inverted format as status register bit 7.
33	Write fault VFO enable	WF/VFOE	VFOE L	This is a bidirectional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled. (HLT = 1) VFOE will then go high until 8 bytes (MFM) before the address mark. It will then go active until the last bit of the second CRC byte of the data field. VFOE will remain low until the end of the data field.
34	Track 00	TR00	FTR00 L	This input informs the formatter/controller when the index hole is positioned over track 00.
35	Index pulse	IP	FIP L	This input informs the formatter/controller when the index hole is encountered on the diskette.

Table 6-10 Formatter/Controller Pin Identification (Cont)

Pin Number	Pin Name	Pin Symbol	Signal Mnemonic	Function
36	Write-protect	WPRT	FWPRT L	This input is sampled whenever a write command is received. A logic low terminates the command and sets the write-protect status bit.
37	Double-density	DDEN	DDEN L	This pin selects either single- or double-density operation. When DDEN = 0, double-density is selected. When DDENN = 1, single-density is selected.
38	Data request	DRQ	DRQ H	This open drain output indicates that the DR contains assembled data in read operations, or the DR is empty in write operations. This signal is reset when serviced by the CPU through reading or loading the DR in read or write operations, respectively.
39	Interrupt request	INTRQ	IRQ H	This open drain output is set at the completion of any command and is reset when the status register is written to.
Disk drive interface:				
15	Step	STEP	STEP L	The step output contains a pulse for each step.
16	Direction	DIRC	DIR L	Direction output is active high when the head is stepping in, active low when the head is stepping out.
17	Early	EARLY	EARLY	This indicates that the write data pulse occurring while early is active (high) should be shifted early for write precompensation.
18	Late	LATE	LATE	This indicates that the write data pulse occurring while late is active (high) should be shifted late for write precompensation.
22	Test	TEST	NOT USED	This input is used for testing purposes only and should be tied to +5 V or left open by the user unless interfacing to voice coil actuated motors. (It is not used by the VT18X control module.)

Table 6-10 Formatter/Controller Pin Identification (Cont)

Pin Number	Pin Name	Pin Symbol	Signal Mnemonic	Function
23	Head load timing	HLT	HLT H	When a logic high is found on the HLT input, the head is assumed to be engaged.
25	Read gate	RG	NOT USED	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization. (It is not used by the VT18X control module.)
26	Read clock	RCLK	RCLK H	A nominal square-wave clock signal derived from the data stream (raw data) is provided to this input from the PLL.
27	Raw read	RAW READ	RDD L	The data inputs signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	Head load	HLD	HLD L	The HLD output controls the loading of the read/write head against the media.
29	Track greater than 43	TG43	NOT USED	This output informs the drive that the read/write head is positioned between tracks 44–76. This output is valid only during read and write commands. (It is not used by the VT18X control module.)
30	Write gate	WG	WG H	This output is made valid before writing is to be performed on the diskette.

6.6.10.3 Phase-Locked Loop – The phase-locked loop (PLL) consists of a 20-pin IC (WD 1691) and an external voltage controlled oscillator (VCO). The PLL performs different functions during the writing and reading operation. During a write operation, the PLL receives the composite stream of data, clocks (WDIN H) from the formatter/controller, and sends it to the disk drive where it is recorded as flux transitions on the diskette. During a read operation, the composite stream of data and clocks (RAW DATA L) from the diskette are separated by the PLL into data pulses (RDD L) and clocks (RCLK H), and then input to the formatter/controller. The input/output signal functions of the WD 1691 are described in Table 6-11.

Table 6-11 WD 1691 Pin Identification

Pin Number	Pin Name	Pin Symbol	Signal Mnemonic	Function
1	Write data input	WDIN	WDIN H	Ties directly to the formatter/controller WD pin and jumper W8. W8 is not installed for double-density operation.
2,3,4,19	Phase 2,3,1,4	02 03 01 04		4 phase inputs to generate a desired write precompensation delay. It is not used by the VT18X control module.
5	Strobe	STB		Strobe output from the 1691. Strobe will latch at a high level on the leading edge of WDIN and reset to a low level on the leading edge of 04. It is not used by the VT18X control module.
6	Write data output	WDOUT	WD H	Serial, precompensated write data stream to be sent to the disk drive's WRDOUT L line.
7	Write gate	WG	WG H	Write gate input from the formatter/controller.
8	VFO enable write fault	VFOE/WF	VFOE L	Input from the formatter/controller. Enables data recovery circuit in conjunction with WG H.
9	Track 43	TG43		Not used by the VT18X control module.
10	Vss	Vss	GND	Ground
11	Read data	RDD	RDD L	Composite clock and data stream input from the disk drive.
12	Read clock	RCLK	RCLK H	RCLK signal generated by the WD1691, connected to the formatter/controller.
13	Pump up	PU	PU H	Tristate output that will be forced high when the PLL requires an increase in VCO frequency.
14	Pump down	PD	PD L	Tristate output that will be forced low when the PLL requires a decrease in VCO frequency.

Table 6-11 WD 1691 Pin Identification (Cont)

Pin Number	Pin Name	Pin Symbol	Signal Mnemonic	Function
15	Double-density enable	DDEN	DDEN L	Double-density select input. When DDEN is low, double-density is selected.
16	Voltage controlled oscillator	VCO	VCO	A nominal 2.0 MHz (5¼ inch drive) master clock input from VCO.
17, 18	Early late	EARLY LATE	EARLY LATE	Early and late signals from the formatter/controller used to determine write precompensation.
20	Vcc	Vcc	Q = 5 V	+5 V ±10° C power supply.

The MFM recording method produces an undesirable shifting of the peaks of adjacent flux transitions on the diskette so that they are moved from the position where they were written. Figure 6-30 shows binary data encoded into MFM format and Figure 6-31 shows how the diskette flux reversals shift the peaks of the composite read voltage waveform. The PLL includes a write precompensation circuit to shift the data in a direction opposite to that expected by the peak shift of the composite read voltage waveforms as a result of the MFM encoding. The write precompensation circuit uses the EARLY LATE and WDIN H signals from the formatter/controller in conjunction with the 1.0 MHz and 4.0 MHz clock signals to generate the precompensated MFM write data output (WRDOUT L).

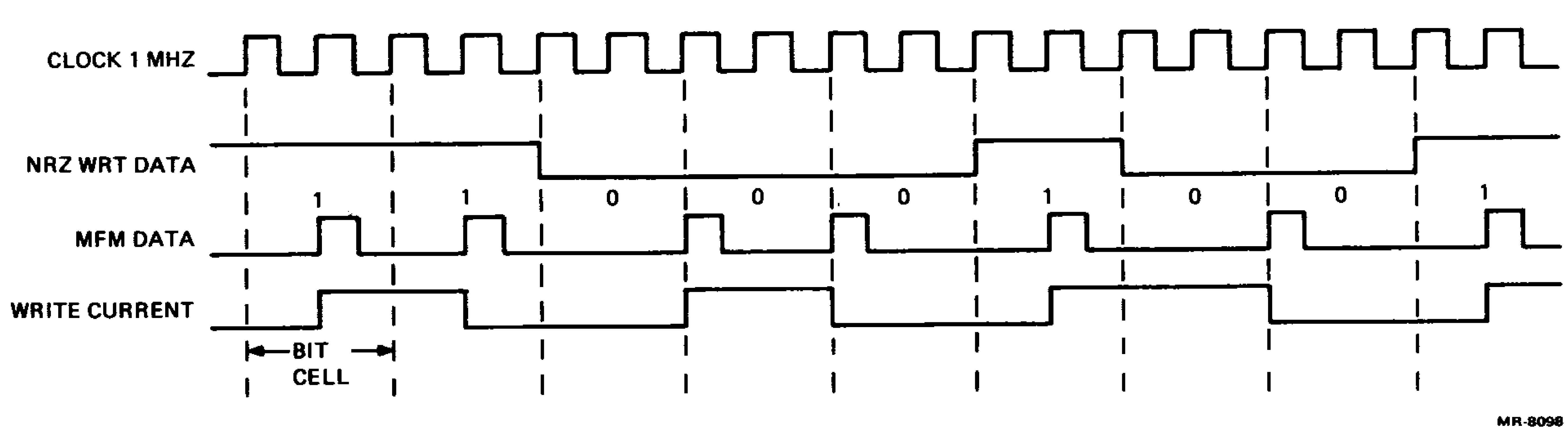


Figure 6-30 MFM Encoding

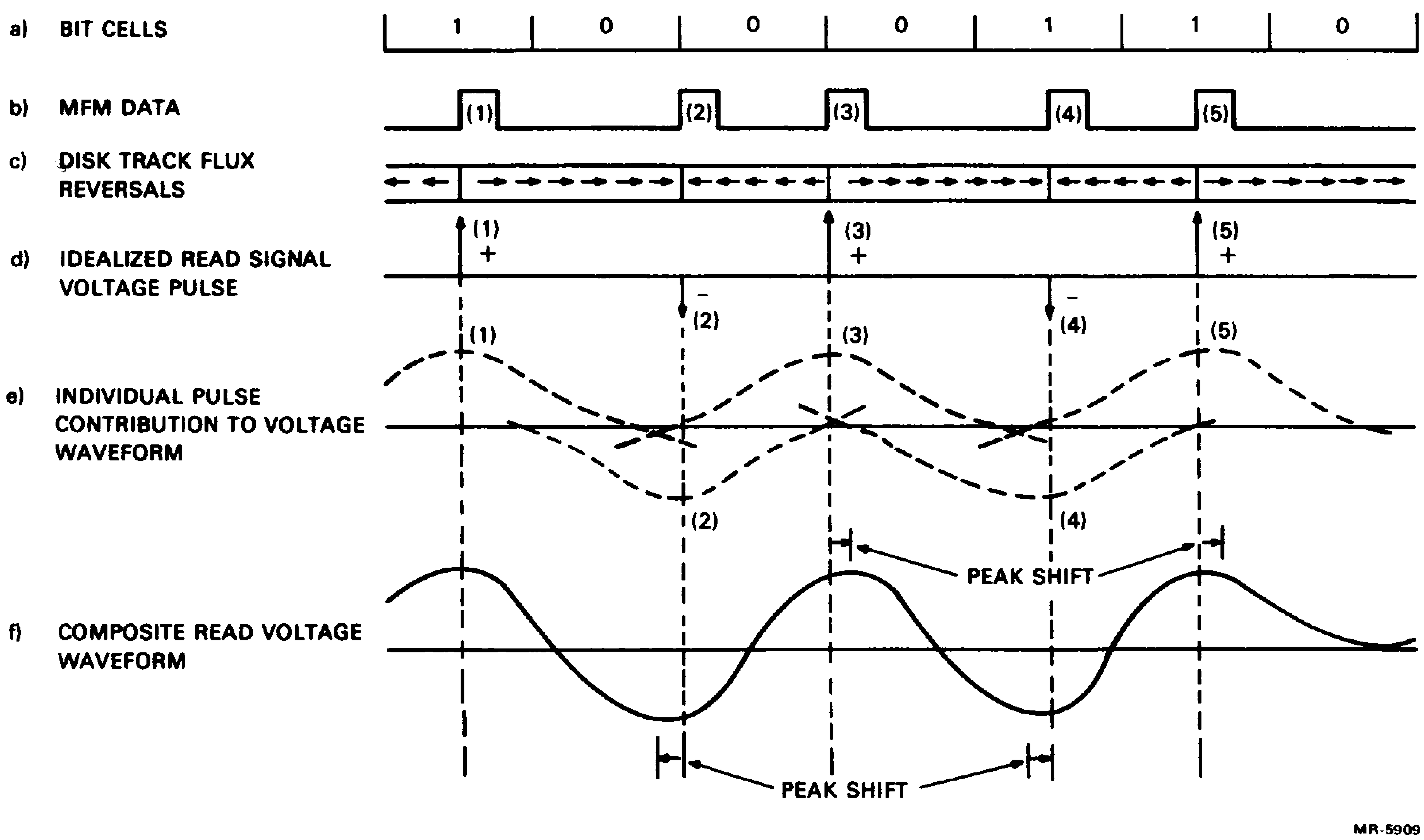


Figure 6-31 Peak Shift Waveform

During a read operation, a data separator circuit in the WD 1619 ensures the correct time relationship between the data (RDD L) and clock (RCLK H) signals when they are recovered from the composite data stream (RAW READ L) received from the disk drive. The data separator circuit uses four input signals (DDEN L, VCO, RDD L, and VFOE L) and produces three outputs: PU, PD, and RCLK. The data separator is enabled when the write gate (WG H) signal goes low and allows the VFOE signal from the formatter/controller to control a phase comparator in the PLL. VFOE goes low during a read operation after the head in the disk drive has loaded and settled. VFOE then goes high until eight bytes before the address mark. It then goes active until the last bit of the second CRC byte of the data field. VFOE remains low until the end of the data field.

When the RDD input to the WD 1691 goes low while VFOE and WG are low, the pump up (PU) and pump down (PD) signals become active. PU and PD are three-state output signals used to control the frequency of the VCO and therefore the frequency of RCLK H. The frequency of RCLK when DDEN equals zero (MFM operation) is the VCO frequency divided by eight. One half of the RCLK time period is used as a window for the read data. If the RDD line has made its transition in the beginning of the RCLK window, PU will go to a logic 1 state to request an increase in VCO frequency. If the RDD line has made its transition at the end of an RCLK window, PU will go to its high impedance state and PD will go to a logic zero requesting a decrease in VCO frequency. When the leading edge of RDD occurs in the center of the RCLK window, both PU and PD remain three-stated, indicating that no adjustment of the VCO free-running frequency is needed. The VCO circuit includes a 50,000 ohm potentiometer, which is used to set the free-running frequency of the oscillator.

6.6.10.4 Disk Drive Controller Registers – The disk drive controller circuit includes two 8-bit registers (Figure 6-29), a diagnostic register, and a general control and status register. The diagnostic register is a read-only register that receives inputs from the disk drive interface connector (J2) and sends outputs to the data bus (DB7–DB0). The inputs provide the CPU with information on the current status of controller functionality during diagnostic testing. The contents of the diagnostic register may be obtained by performing a read to address A0 L.

The general control and status register holds various control and status information for the disk drive as well as the VT18X control module. The lower 4-bits of the register are read/write and can be accessed by a read or write to address 80H. The upper four bits of the register are read-only and are accessed by performing a read to address 80H.

6.6.10.5 Disk Drive Controller Latches – Two data latches are used by the disk drive controller to store control and status information. The write data bit latch is a D-type FF that is set whenever write data is sent to the disk drive. The output of the write data bit latch is sent to the diagnostic read register as bit 4 and is used during diagnostic testing to determine if data is being written out to the disk drive. The write data out bit is reset by a read to address 90H.

The control and status latch is a 4-bit latch used to store the disk select signals (DS1–DS0), the MOTOR ON H bit, and the double-density enable (DDEN) bit. These bits are obtained from DB3–DB0 and are stored in the latch by performing a write to address 80H. DDEN is sent to the disk drive formatter/controller, the PLL, and the general control and status register. MOTOR ON H is sent to the general control and status register, the diagnostic read register, the formatter/controller, and the disk drive via pin 16 of connnector J2. DS1 and DS0 are sent to the general control and status register and are used to inform the CPU of the disk drive currently selected. DS1 and DS0 are also sent to the drive select decoder to select one of four drives depending on the binary combination of bits 1–0 stored in the control and status latch. The drive select signals (DRIVE 3 L–DRIVE 0 L) are sent to the disk drives via connector J2 to enable the read/write logic of the selected drive.

6.6.10.6 Disk Drive Interface Connector – The control and data lines for interfacing the disk drive controller to the disk drives are routed to a 37-pin, D-type connector (J2) on the VT18X control module. The control and data lines and the pins to which they are connected are listed in Table 6-12.

Table 6-12 Disk Drive Interface Connector Signals

Pin Number	Signal	Mnemonic	Direction	Function
6	Select 3	Drive 3 L	Out	This signal initiates a head load on drive 3 when it goes low.
8	Index	IP L	In	This signal is obtained each time the disk drive senses the index hole in the diskette. The signal indicates the start of a diskette track.
10	Select 0	Drive 0 L	Out	This signal initiates a head load on drive 0 when it goes low.
12	Select 1	Drive 1 L	Out	This signal initiates a head load on drive 1 when it goes low.
14	Select 2	Drive 2 L	Out	This signal initiates a head load on drive 2 when it goes low.
16	Motor on	MOTOR ON L	Out	This signal turns on the drive motor when it goes low.

Table 6-12 Disk Drive Interface Connector Signals (Cont)

Pin Number	Signal	Mnemonic	Direction	Function
18	Direction	DIR H	Out	When a logical 1 is present on this line, the read/write head will move away from the center of the disk when a pulse is applied to the step line. When this line is a logical low, a step pulse will move the read/write head to the center of the disk.
20	Step	STEP H	Out	When this line is pulsed low, the read/write head will move in the direction defined by the direction line.
22	Write data	WRDOUT L	Out	This signal is the data to be written on the diskette. Each transition from a logical 1 to a logical 0 causes the read/write head current to be reversed, thereby writing a data bit. This line is enabled when write gate is active.
24	Write gate	WRITE GATE L	Out	When this line is a logical 0, write data can be written on the diskette.
26	Track 00	TRACK 00 L	In	When this signal is low, it indicates that the read/write head is positioned at track zero (outermost track).
28	Write-protect	WPRT L	In	When this signal is low, it indicates that a write-protected diskette is installed in the drive.
30	Read data	RAW DATA L	In	This signal input is the composite clock and data stream from the disk drive.
34	Drive ready	READY L	In	This optional signal input from the disk drive is not used, and it is tied to a pull-up resistor. The READY L signal is grounded internally on the VT18X control module by jumper W6.

NOTE: Pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, and 33 are connected to ground. Pin 32 is reserved.

6.6.11 VT18X Control Module Input/Output Addresses

Data or control and status information is read from or loaded (written) into the various data, control and status, and diagnostic read/write registers in the VT18X control module by the CPU under software control. These registers are read or loaded by the program using instructions referring to a particular register address. Table 6-13 lists the I/O addresses and the registers they access. The format and bit functions of the various registers are described in detail in the following paragraphs.

Table 6-13 VT18X Control Module I/O Addresses

Address	Register
40H	Console port data register
41H	Console port control/status register
48H	Printer port data register
49H	Printer port control/status register
50H	General port data register
51H	General port control/status register
58H	Communications port data register
59H	Communications port control/status register
78H	Disk drive controller control/status register WO/RO
79H	Disk drive controller track register R/W
7AH	Disk drive controller sector register R/W
7BH	Disk drive controller data register R/W
80H	General disk drive control/status register R/W
88H	Communications status register RO
90H	Communications control/baud rate select register WO
90H	Real time clock interrupt reset register RO
98H	Diagnostic write register WO
AOH	Diagnostic read register RO

6.6.12 Communications Data and Control and Status Registers

The four communications ports use 8251A programmable communications interfaces and should be programmed alike. Prior to starting data transmission or reception, the PUSART must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the PUSART and must immediately follow a reset operation. The control words are split into two formats: a mode instruction and a command instruction. The mode instruction can be programmed in either a synchronous or asynchronous format. The asynchronous mode instruction can be used by all of the I/O ports, but synchronous mode can only be used by the communications port control and status register (59H).

The PUSARTs are programmed as follows; first, the control and status registers 41H, 49H, 51H, and 59H must be programmed with the synchronous or asynchronous mode byte. Then, the same register must be written with a command byte. A read of those locations reveals the current status of that PUSART. The PUSART data registers (40H, 48H, 50H, and 58H) hold the 8-bit data byte to be transmitted or received. The formats and bit definitions for the data and control and status registers are described in the following paragraphs.

6.6.12.1 Asynchronous Mode Instruction Format (41H, 49H, 51H, 59H) WO – Whenever a data character is transmitted by the CPU in the synchronous mode, the PUSART automatically adds a start and the programmed number of stop bits to each character. Also, an odd or even parity bit is inserted prior to the stop bit(s) as defined by the mode instruction.

Whenever a character is received in the asynchronous mode, the PUSART checks the validity of the start, data, parity, and stop bits. If an error has not been detected, PUSART strips the start, parity, and stop bits and then loads the data character into the parallel I/O buffer of the PUSART. The asynchronous mode instruction format is shown in Figure 6-32. Table 6-14 describes the bits.

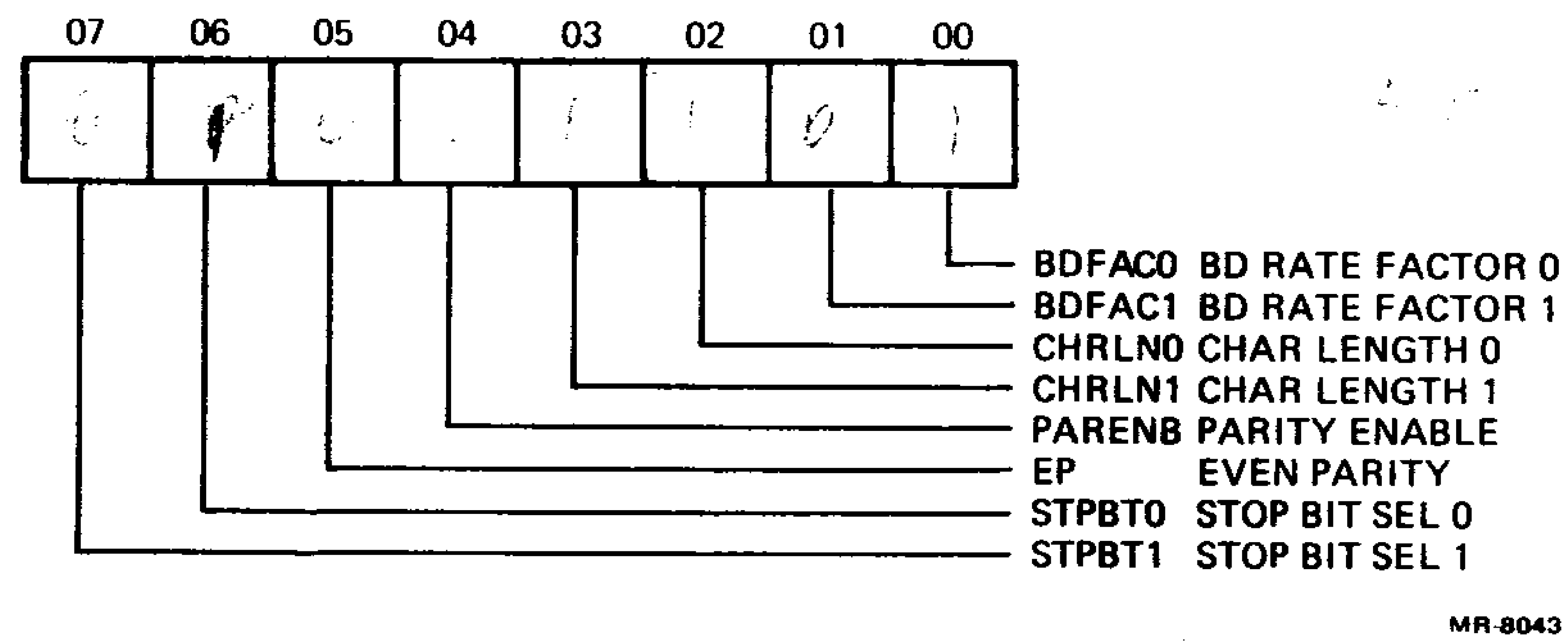


Figure 6-32 Mode Instruction Format, Asynchronous (41H, 49H, 51H, 59H) WO

Table 6-14 Asynchronous Mode Instruction Bit Description

Bits	Name	Description
0, 1	Baud rate factor select	These bits hold the encoded value of the bits to be selected. **Bit 1** **Bit 0** **Mode Selected** 0 0 Synchronous mode 0 1 1 × clock 1 0 16 × clock 1 1 64 × clock
2, 3	Character length select	These bits hold the encoded value of the character length to be selected. **Bit 3** **Bit 2** **Character Length** 0 0 5 bits 0 1 6 bits 1 0 7 bits 1 1 8 bits
4	Parity enable	When set, this bit enables parity. When clear, no parity is used.
5	Even parity generation/check	When set, this bit enables an even mode of parity and when clear, odd parity is enabled.
6, 7	Number of stop bits	These bits hold the encoded value of the number of stop bits that are used. **Bit 7** **Bit 6** **Stop Bits** 0 0 Invalid 0 1 1 bit 1 0 1½ bits 1 1 2 bits

6.6.12.2 Synchronous Mode Instruction Format (59H) WO – The communications port is the only port that may be programmed to operate in the synchronous mode. In the synchronous mode, the PUSART can be programmed to transmit one or two sync characters followed by a stream of data characters. When the PUSART receives data in the asynchronous mode, character synchronization can be internally or externally achieved. The synchronous mode instruction format is shown in Figure 6-33. Table 6-15 describes the bits.

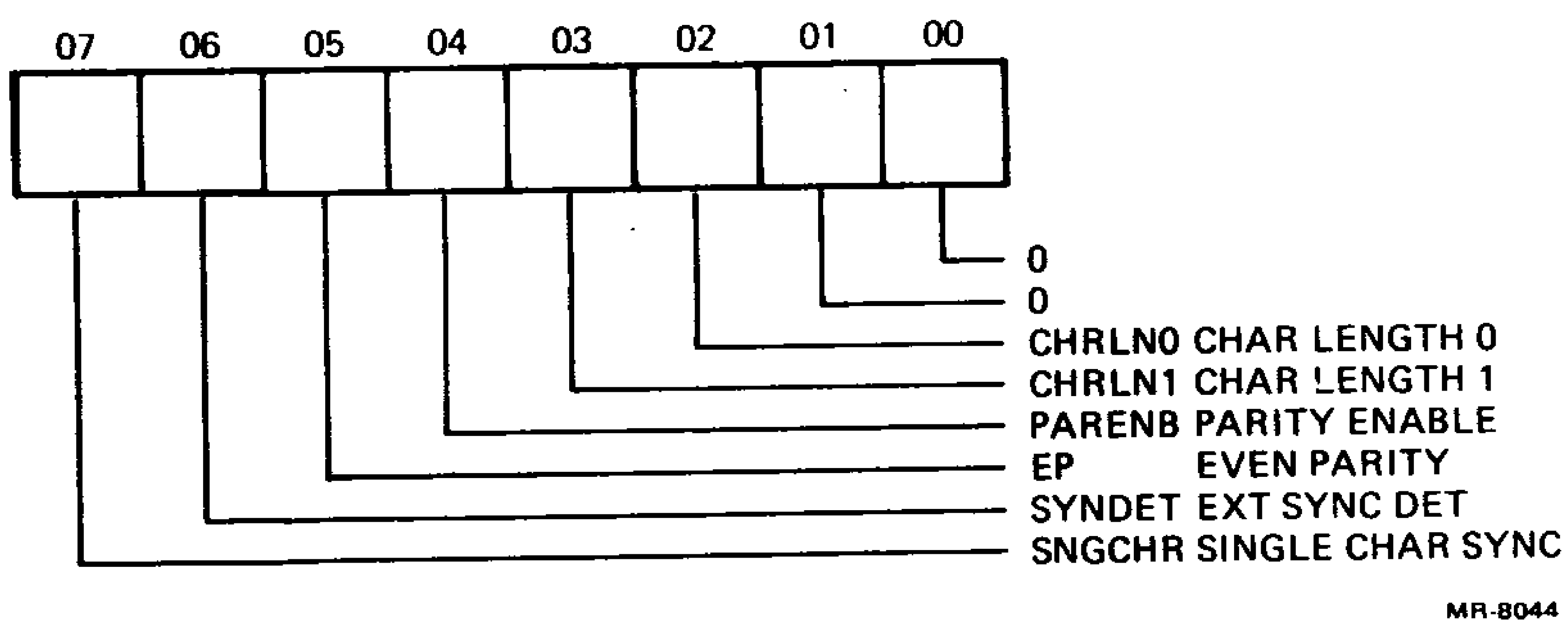


Figure 6-33 Mode Instruction Format, Synchronous (59H) WO

Table 6-15 Synchronous Mode Instruction Bit Description

Bits	Name	Description
0, 1		Always 0.
2, 3	Character length select	These bits hold the encoded value of the character length to be selected. **Bit 3 / Bit 2 / Character Length** 0 0 5 bits 0 1 6 bits 1 0 7 bits 1 1 8 bits
4	Parity enable	When set, this bit enables parity. When clear, no parity is used.
5	Even parity generation/check	When set, this bit enables an even mode of parity and when clear, odd parity is enabled.
6	External sync detect	When set, the PUSART is in external sync detect mode and character synchronization is achieved by an external input. When clear, the PUSART is in internal sync mode and will output a sync detect pulse to indicate that it has located the sync character in receive mode.
7	Single character sync	When set, single sync character mode is selected. When clear, double sync character mode is selected.

6.6.12.3 Command Instruction Registers (41H, 49H, 51H, 59H) WO – Once the mode has been set in the 8251, a command has to be issued. This is done by issuing a command to the same location that the mode instruction was programmed into. The command instruction format is shown in Figure 6-34. Table 6-16 describes the bits.

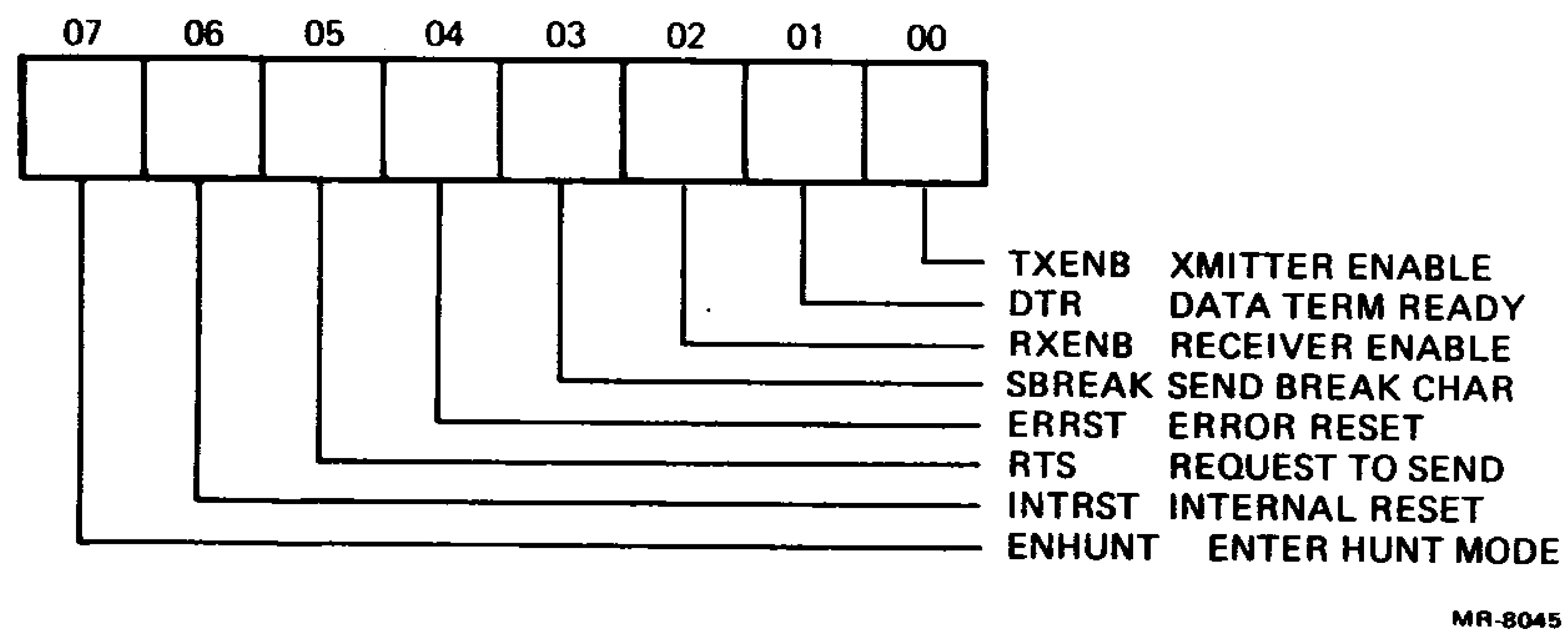


Figure 6-34 Command Instruction Format (41H, 49H, 51H, 59H) WO

Table 6-16 Command Instruction Bit Description

Bits	Name	Description
0	Transmitter enable	This bit must be set to enable the transmitter function.
1	Data terminal ready	This is a general purpose control bit that can be used for anything but is usually used to signify DTR. A one written to this register forces the DIR output pin to a zero.
2	Receiver enable	This bit must be set to enable the receiver function.
3	Send break character	A one written to this bit forces the TXD output pin low.
4	Error reset	Writing a one to this bit results in the parity error, overrun error, and framing error status bits being reset.
5	Request to send	This is a general purpose control bit that can be used for anything but is usually used to signify RTS. A one written to this register forces the RTS output pin to a zero.
6	Internal reset	A high on this bit internally resets the 8251A and returns it to mode instruction format.
7	Enter hunt mode	A one enables a search for sync characters in the data stream.

6.6.12.4 Status Read Registers (41H, 49H, 51H, 59H) RO – This register holds the status of the 8251A's operation. Note that the status may not be valid for 14 microseconds after the actual event occurred. The status read register format is shown in Figure 6-35. Table 6-17 describes the bits.

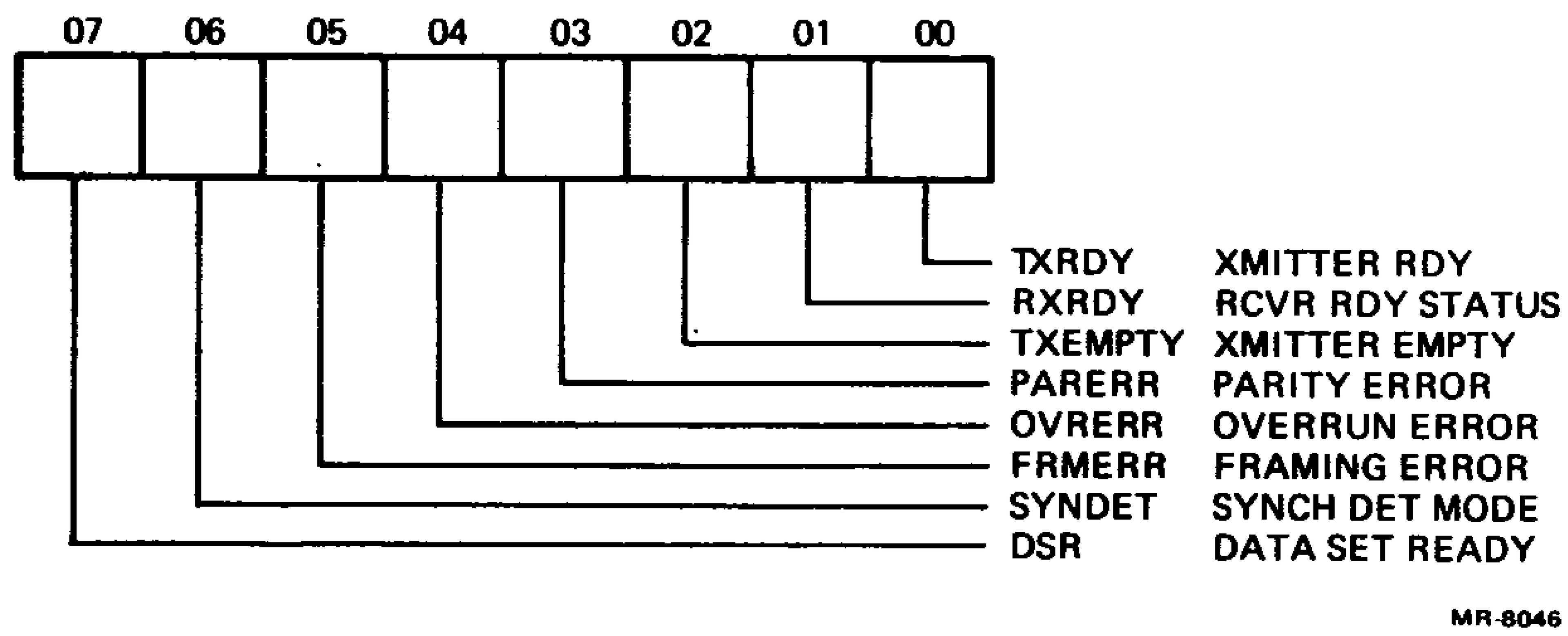


Figure 6-35 Status Read Format (41H, 49H, 51H, 59H) RO

Table 6-17 Status Read Register Bit Description

Bits	Name	Description
0	Transmitter ready status	This bit has a different meaning than the TXRDY pin on the 8251A. The status bit is not conditioned by CTS and TXENB while the TWRDY pin is conditioned by these signals.
1	Received ready	This bit corresponds with the output pin of the same name. When set, it means that the receive data buffer is full and the CPU must read it. This is the bit that is wire ORed from the 8251As to create a restart (16 H) of the Z80A.
2	Transmitter empty status	This bit also has a corresponding I/O pin with the same meaning. When set, it indicates that the transmitter data buffer is empty and waiting for service.
3	Parity error status	This flag is set when a parity error is detected. It is reset through the error reset bit in the command registers. When set, this bit does not inhibit the operation of the 8251A.
4	Overrun error status	The overrun error status bit is set when the CPU does not read a character from the receive data buffer before the next one comes along. It is also reset by the error reset bit in the command registers. In the case of an overrun, the character is lost and the 8251A continues operation.

Table 6-17 Status Read Register Bit Description (Cont)

Bits	Name	Description
5	Framing error status (asynchronous only)	The framing error status bit is set when a valid stop bit is now detected at the end of every character. It is reset by the error reset bit in the command register of the 8251A. This flag does not inhibit the operation of the 8251A.
6	Sync detect status	This bit is used for synchronous mode for SYNDET and may be used as either input or output. It is programmable through the command register. It is reset to output mode low upon a reset. When used as an output, the SYNDET pin will go high to indicate that the 8251A has located the sync character in receive mode. While in bi-sync mode, the SYNDET line will go high in the middle of the last bit of the second sync character. SYNDET is automatically reset when a status read operation occurs.
7	Data set ready status	When set, this bit indicates that the DSR pin is low.

6.6.12.5 Transit Data Buffer Register (40H, 48H, 50H, 58H) WO – This is a write-only, 8-bit register that holds the data to be transmitted from the 8251A. The transmit data format is shown in Figure 6-36. Table 6-18 describes the bits.

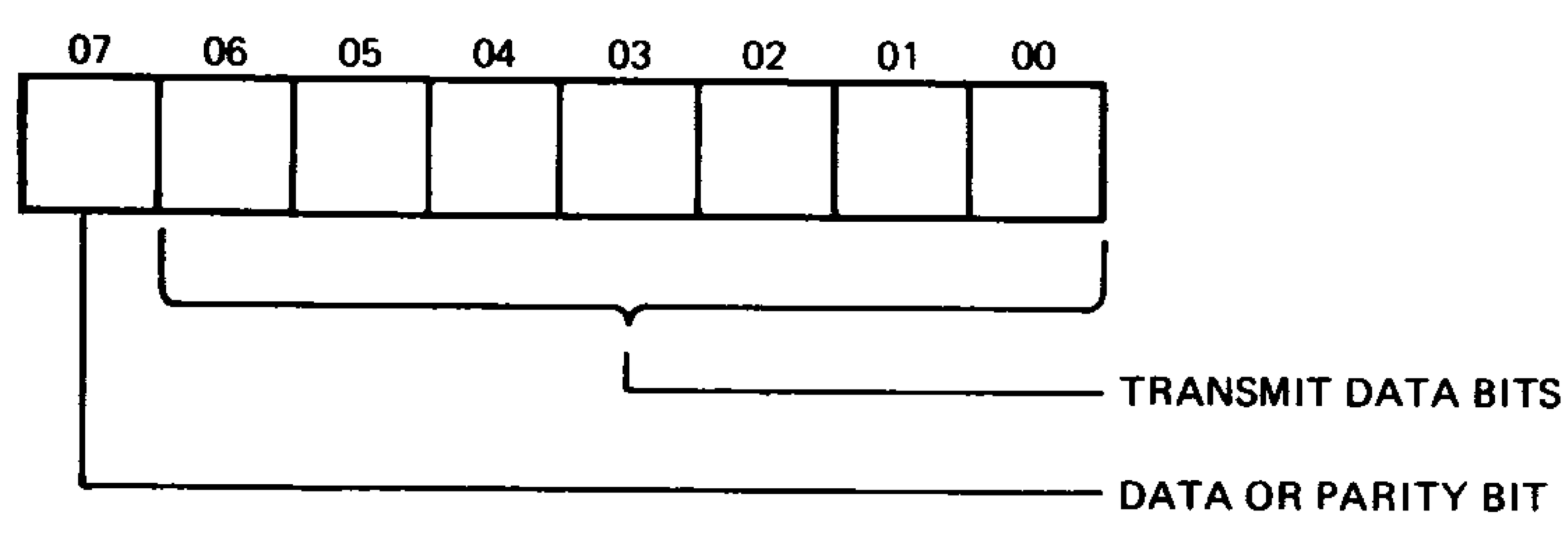


Figure 6-36 Transmit Data Format (40H, 48H, 50H, 58H) WO

Table 6-18 Transmit Data and Received Data Bit Description

Bits	Name	Description
7:0	Transmit data	Bit 0 is the least significant bit and bit 7 is the most significant bit. If seven data bits plus parity are selected, bit 8 is the parity bit. If character length is defined as 5, 6, or 7 bits, the unused bits are set to zero.
7:0	Received data	Bit 0 is the least significant bit and bit 7 is the most significant. If character length is defined as 5, 6, or 7 bits, the unused bits will be zero.

6.6.12.6 Received Data Buffer Register (40H, 48H, 50H, 58H) RO – This read-only, 8-bit register contains the received character after the receiver ready (RXRDY) bit becomes asserted. The received data format is shown in Figure 6-37. Table 6-18 describes the bits.

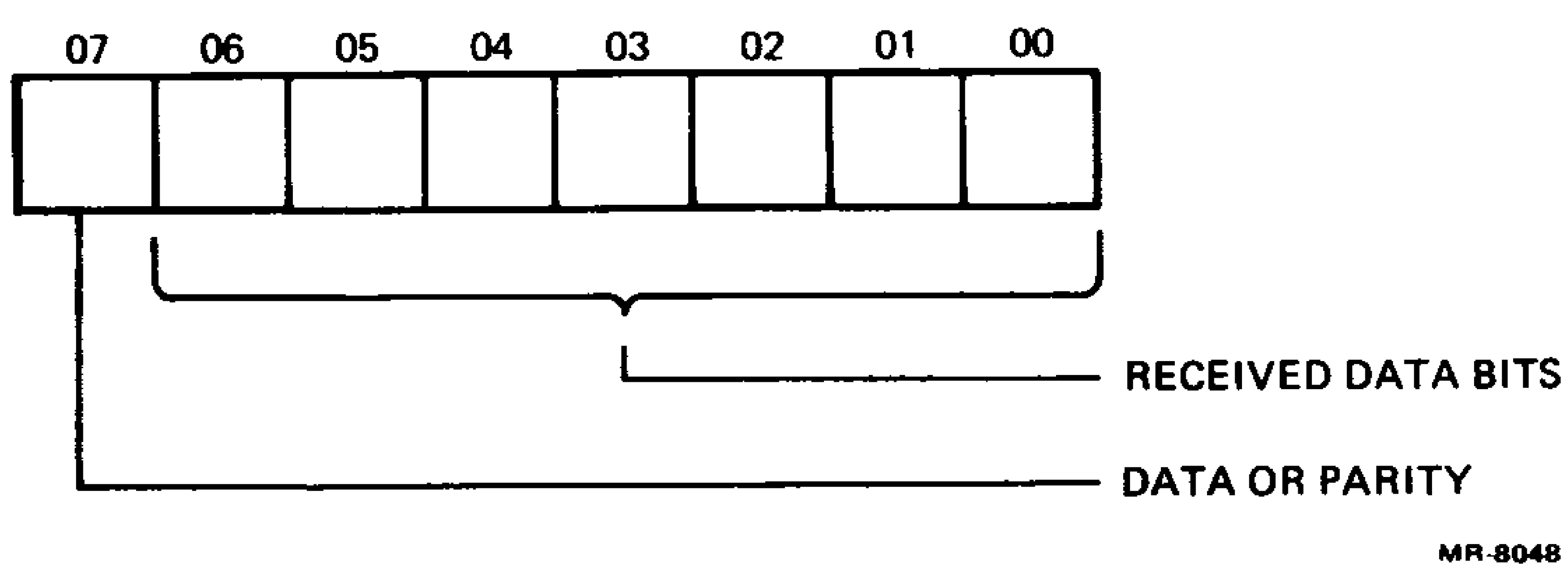


Figure 6-37 Received Data Format (40H, 48H, 50H, 58H) RO

6.6.13 Disk Drive Controller Registers

The disk drive controller contains four 8-bit registers that define and execute the programmed controller functions. These registers (command/status, track, sector, and data) are physically located in the disk drive formatter/controller IC (WD 1793) and are described in Paragraphs 6.6.13.1 through 6.6.13.5.

6.6.13.1 Command Register (Write-Only) – This 8-bit register at address 78H is used as a write-only register when it is loaded by the program with the command that is to be executed by the drive. Table 6-19 summarizes the command types that are written into this register.

NOTE

When bits are defined to be 1s or 0s (as in Table 6-19) they should not be changed in the specific commands.

Table 6-19 Disk Drive Controller Commands

Command Type	Command	Bits 7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	v	r1	r0
I	Seek	0	0	0	1	h	v	r1	r0
I	Step	0	0	1	u	h	v	r1	r0
I	Step in	0	1	0	u	h	v	r1	r0
I	Step out	0	1	0	u	h	v	r1	r0
II	Read sector	1	0	0	m	0	e	0	0
II	Write sector	1	0	0	m	0	e	0	a0
III	Read address	1	1	1	0	0	e	0	0
III	Read track	1	1	1	0	0	e	0	0
IV	Force interrupt	1	1	0	1	I3	I2	I1	I0

Table 6-20 shows the delay that must be observed between operations of registers. Tables 6-21 and 6-22 show type I command bit descriptions and flags. Tables 6-23, 6-24, and 6-25 show type II command and type III command bit descriptions and flags.

Table 6-20 Required Delays

Operation	Next Operation	Delay Required (MFM)
Write to command register	Ready busy bit (Status bit 0)	12 μs
Write to command register	Read status bits 1–7	23 μs
Write to any register	Read from different register	0
Write to track, sector or data register	Read from same register	8 μs
Write to any register	Write to another register	14 μs
Interrupt request	Read status register	4 μs

Table 6-21 Type I Command Bit Description

Bits	Name	Description
0, 1	Stepping rate (r1, r0)	These bits control the rate at which the stepping pulses are sent to the disk drive. See Table 6-22 for stepping rate breakdown.
2	Track verify (v)	This bit determines if there is a verification operation to take place on the destination track. During verification the head is loaded, and after a 30 ms delay, the HLT input is sampled. After a 1.0 second motor start-up time, the HLT input becomes active. When HLT is set, the first ID field is read off the diskette. The track address of the ID field is compared to the track register. If there is a match and a valid ID CRC, the verification is complete and an interrupt is generated. If not valid, the seek error status is set.
3	Head load flag (h)	This bit determines if the head is to be loaded at the beginning of a command. If the head is loaded, then the head remains loaded until either the formatter/controller receives a command that specifically disengages the head or 15 revolutions of the diskette have passed with the busy bit equal to 0.
4	Update (step commands) (u)	When set (1), the track register is updated for each step; otherwise the track register is not affected.
5–7		Determine the command to be executed.

Table 6-22 Type I Command Flags

Flag	Name	Function
h	Head load flag (bit 3)	h = 1, Load head at beginning h = 0, Unload head at beginning
v	Verify flag (bit 2)	v = 1, Verify on destination track v = 0, No verify
r1, r0	Stepping motor rate (bits 1–0)	r1 r0 0 0 6 ms 0 1 12 ms 1 0 20 ms 1 1 30 ms
u	Update flag (bit 4)	u = 1, Update track register u = 0, No update

Table 6-23 Type II Command Bit Description

Bit	Name	Description
0	Data address mark	When set upon a write sector command, this bit defines a data mark (OFBH) to be written on the diskette. If the bit is not set, then a deleted data mark (OF8H) is written onto the diskette. When writing valid data on the diskette, this bit should be set.
1		Always 0.
2	30 millisecond delay	When set during a command, there is a 30 ms delay before reading begins. For maximum controller throughput, this bit should be 0. It should be set if the last command was a seek or new drive select. (See Table 6-25.)
3		Always 0.
4	Multiple sector	When set, this bit allows multiple sectors to be transferred.
5–7		Determine the command to be executed.

Table 6-24 Type III Command Bit Description

Bits	Description
0, 1	Always set to 0.
2	Same as bit 2 for type II commands. (See Table 6-25.)
3–7	Determine the command to be executed.

Table 6-25 Type II and III Command Flags

Flag	Name	Function
m	Multiple record flag (bit 4)	m = 0, Single record m = 1, Multiple records
a0	Data address mark (bit 0)	a0 = 0, 373° (data mark) a0 = 1, 370° (deleted data mark)
e	30 ms delay (bit 2)	e = 1, 30 ms delay e = 0, No delay

Type IV Command Bit Description
This command can be loaded into the register at any time. If there is a current command under execution, the command is terminated. See Table 6-26 for a description of conditions that terminate the command.

Table 6-26 Type IV Command Flags

Flag	Name	Function*
I0	Interrupt condition flag 0	I0 = 1, Not ready-to-ready transition
I1	Interrupt condition flag 1	I1 = 1, Ready-to-not ready transition
I2	Interrupt condition flag 2	I2 = 1, Index pulse
I3	Interrupt condition flag 3	I3 = 1, Immediate interrupt

*I3-I0 = 0, terminate with no interrupt.

6.6.13.2 Status Register (Read-Only) – This read-only register also resides at the same address (78H) as the command register. It contains the 8-bit status resulting from the completion of a command. The definition of the status bits varies according to the type of command executed. The format of the status register and bit definitions for all type I and type II (read and write sector) commands is shown in Figures 6-38, 6-39, and 6-40. Tables 6-27, 6-28, and 6-29 describe the bits.

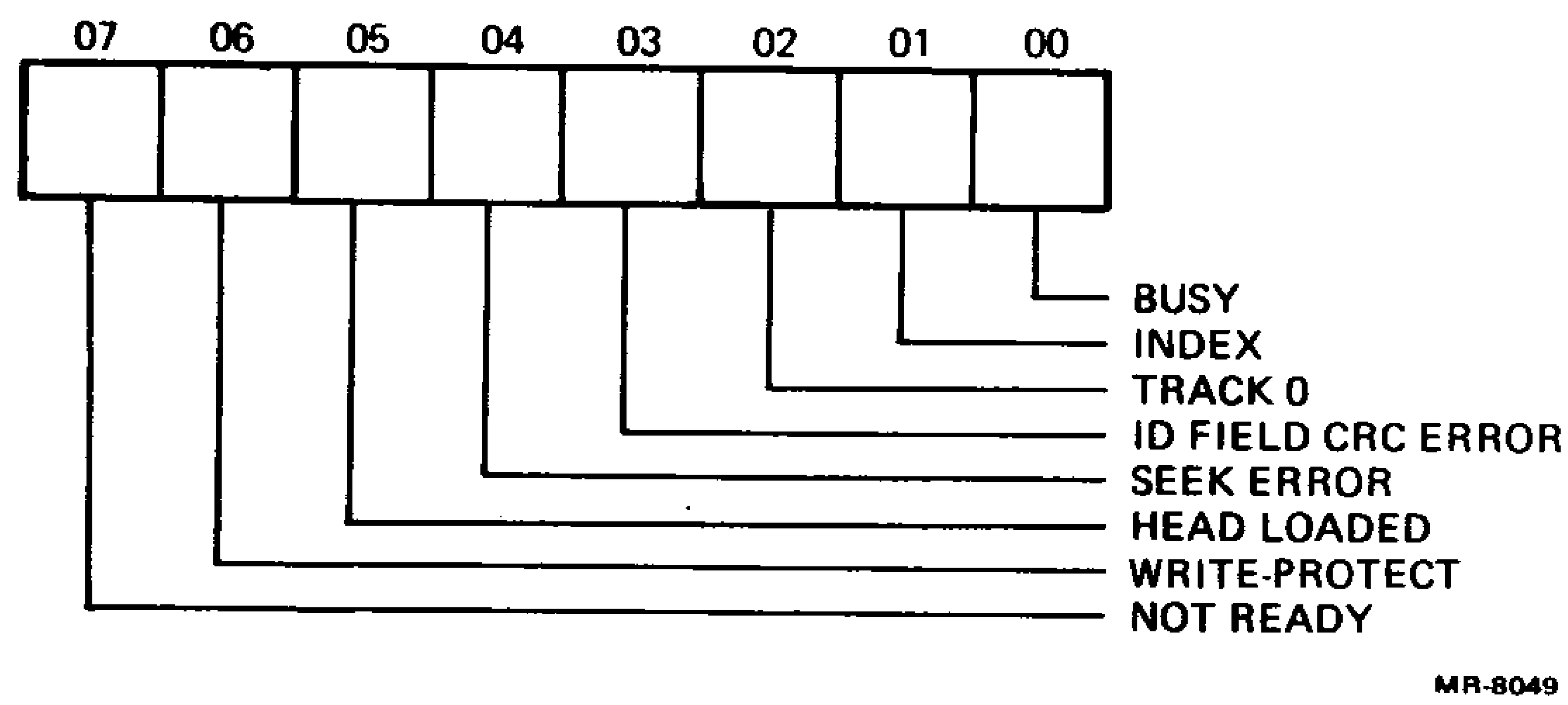


Figure 6-38 Type I Status Register Format

Table 6-27 Type I Status Register Bit Description

Bits	Name	Description
0	Busy	When this bit is set (1), the formatter/controller is currently executing a command. Only a type IV command can be issued when this condition exists.
1	Index	When this bit is set (1), the index pulse is currently occurring.
2	Track 0	When this bit is set (1), the read/write head is currently positioned at track 0.
3	ID field CRC error	When set, this means that there was a CRC error of the ID field.
4	Seek error	When set, a seek error was encountered meaning that the destination track address was not found.
5	Head loaded	This bit reflects the current status of the head. When set, the head is loaded and the HLD output is asserted.
6	Write-protect	When set, the bit means that the current diskette is write-protected. An attempt to write a sector sets the interrupt flag.
7	Not ready	When set, the bit indicates that the disk drive is not ready. This could mean that the disk drive is not up to speed, the diskette is in upside down, or the door is open. This bit must be clear before any commands are issued to the formatter/controller.

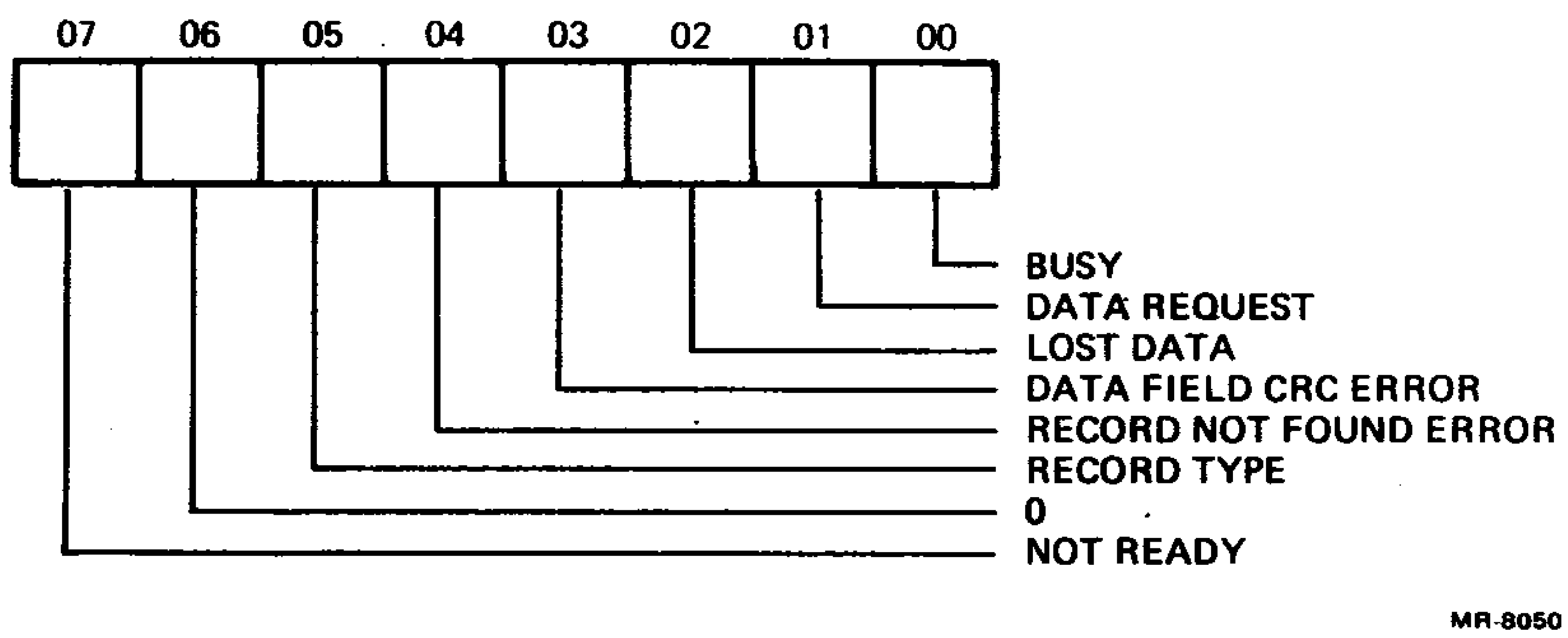


Figure 6-39 Type II Read Sector Status Register Format

Table 6-28 Type II Read Sector Status Register Bit Description

Bits	Name	Description
0	Busy	Same as type I status.
1	Data request	When set, this bit means that the data register is full and is waiting for the CPU to read the register.
2	Lost data	When set, this bit means that the data register had not been serviced within 27.5 microseconds and the data in the data register is not valid.
3	Data field CRC error	When set, this bit indicates that the CRC of the read data field does not check with the data CRC that was written on the diskette.
4	Record not found error	When set, this bit means that a data address mark was not found within 43 bytes of the last ID field CRC byte.
5	Record type	This bit reflects the type of data mark that was encountered during the read. When set, a deleted data mark was found. If clear, a data mark was encountered.
6		Always set to 0.
7	Not ready	Same as type I not ready status bit.

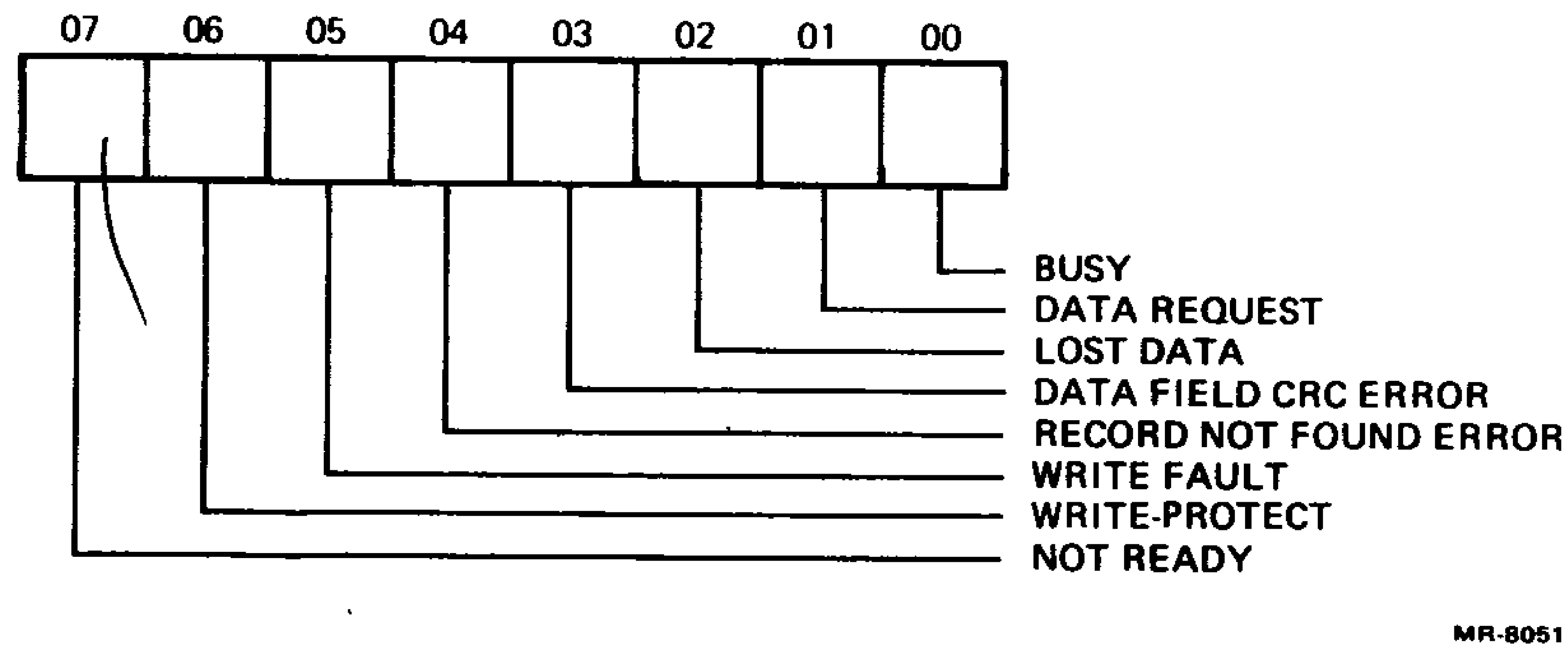


Figure 6-40 Type II Write Sector Status Register Format

Table 6-29 Type II Write Sector Status Register Bit Description

Bits	Name	Description
0	Busy	Same as type I status busy bit.
1	Data request	When set, this bit means that the data register is empty, and it is waiting for the CPU to write the register.
2	Lost data	When set, this bit means that data register had not been written within 23.5 μs and the data on the diskette is not valid (zero bytes are substituted for data lost).
3	Data field CRC error	When set, this bit indicates that the CRC of the data that was written does not check with the data CRC that was written on the diskette.
4	Record not found error	When set, this bit means that a data address mark was not found within 43 bytes of the last ID field CRC byte.
5	Write fault	When this bit is set it indicates that there is a fault with the drive's write electronics.
6	Write-protect	When this bit is set after a write command, an attempt was made to write on a write-protected disk.
7	Not ready	Same as type I not ready status bit.

6.6.13.3 Track Register (Read/Write) – This R/W 8-bit register holds the updated address (00 H–39 H) of the current read/write head. It is incremented by one every time the head is stepped toward the spindle and decremented by one every time the head is stepped away from the spindle. The contents of the register are compared with the recorded track number in the ID field during diskette read, write, and verify operations. The track register address is 79H.

6.6.13.4 Sector Register (Read/Write) – This read/write 8-bit register holds the address (01 H–09 H) of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during diskette read and write operations. The sector register address is 7AH.

6.6.13.5 Data Register (Read/Write) – For a seek operation, this 8-bit read/write register holds the address of the desired track position. During data transfers, this register is the data buffer for the diskette. The data register address is 7BH.

6.6.14 Disk Drive Command Summary

The VT18X control module accepts 11 commands for disk drive control. Commands should only be loaded into the command register when the busy status bit is off. The one exception is the force interrupt command. The busy status bit is set when a command is executed.

6.6.14.1 Type I Commands – Type I commands are for head positioning. The stepping rate of these commands is dictated by the disk drive. The recommended stepping rate is r1 = 1 and r0 = 1 (30 ms). The head load flag determines if the head is loaded at the beginning of the command. Otherwise, the head is loaded at the end of a command. The verification flag allows a verification operation to take place on the destination track. The verification consists of reading the first encountered ID filed off the diskette. The track address of the ID field is compared to the track register. If there is a match and a valid ID CRC, the verification is complete. If not valid, the seek error status bit in the formatter/controller is set. The step, step-in, and step-out commands contain an update flag for updating the track register when this bit is set after the step has been completed.

6.6.14.2 Type II Commands – The type II commands allow you to read and write sectors of the diskette. Prior to loading the type II command into the command register, the sector register must be loaded with the desired sector number. Upon receipt of the command, the busy status bit is set. If the e flag is set (normal case), the head is loaded and the HLT signal is sampled after 30 ms. Otherwise, no delay is incurred after a command. The HLT does not become active until 1.0 second after the head is loaded. This allows the spindle motor to have time to accelerate. The formatter/controller then attempts to find the ID field with the specified track and sector. If it is not found within four revolutions of the diskette, the record not found status bit is set. Otherwise, the command is executed by the formatter/controller generating data requests (DRQs) for servicing the data register.

Each of the type II commands contains an m flag that determines if multiple sectors are to be read or written, depending upon the command. When set, multiple sectors are read or written with the sector register internally updated for address verification on the next track. The formatter/controller continues to do the transfers until the sector register exceeds the number of sectors on the track or until a force interrupt command is loaded into the command register. If the sector register exceeds the number of sectors on the track, the record not found status bit is set. When the head is loaded, the busy status bit is set; and when an ID field is encountered that has the correct track, sector, side numbers, and correct CRC, the data field is presented to the CPU (read) or presented by the CPU (write). At the end of the read operation, the type of data address mark encountered is recorded in the status register (bit 5). On a write operation, the a0 flag (bit 0) determines the type of data address mark to be written onto the diskette. If set, a deleted data mark is written. If reset, a data mark is written.

6.6.14.3 Type III Commands – These commands allow you to read and write format information on the diskette. The read address command is to read in the six bytes of the ID field (track number, side number, sector address, sector length, and two bytes of CRC). The read track command is to read a full track of raw information. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. The write track command is used to format a diskette.

6.6.14.4 Type IV Command – This command allows you to terminate an operation upon the condition specified in bits 3–0. See Table 6-26 for descriptions of the termination conditions.

6.6.15 General Control and Status Register (80H)

This 8-bit register holds various control information for the disk drive and the VT18X control module. The lower four bits are read/write, while the upper four bits are read-only.

The general control and status register format is shown in Figure 6-41. Table 6-30 describes the bits.

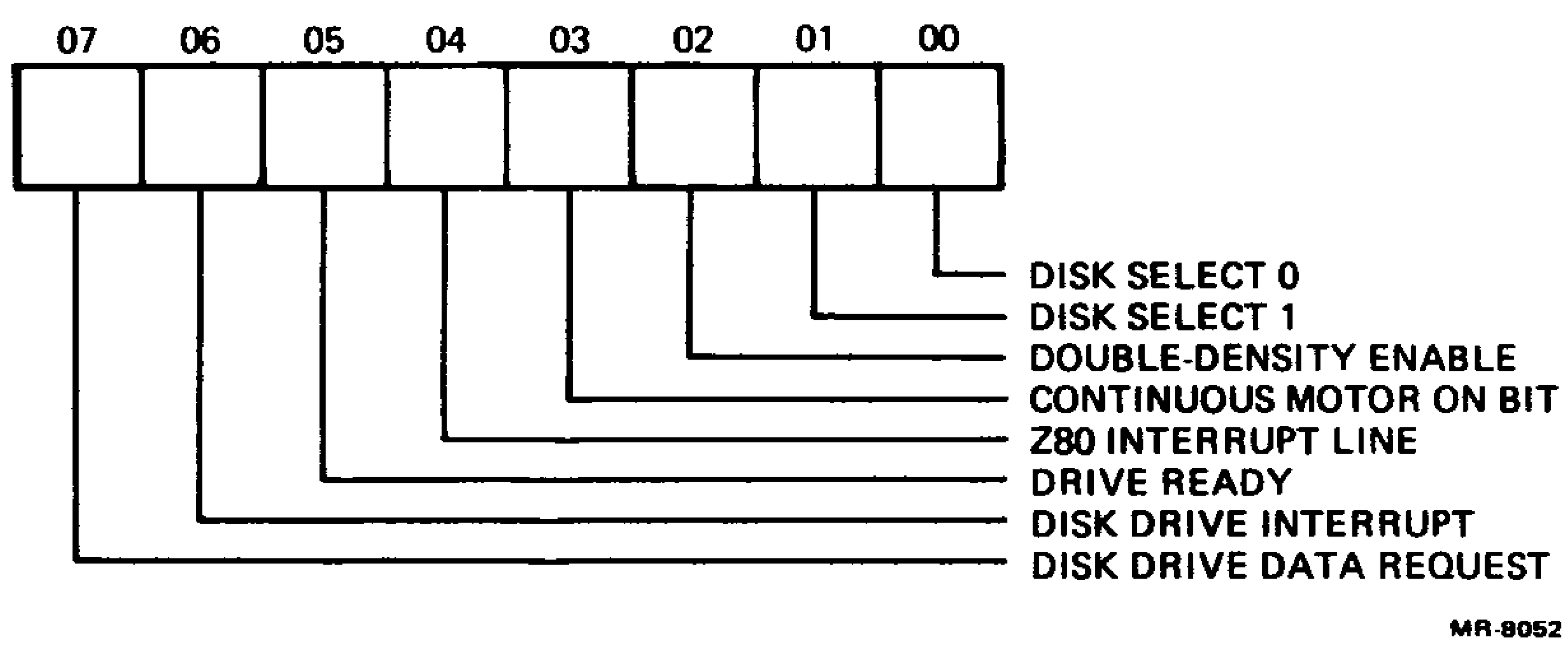


Figure 6-41 General Control and Status Register Format

Table 6-30 General Control and Status Register Bit Description

Bits	Name	Description
0, 1	Disk drive select	These bits hold the encoded value of the current disk drive to be selected. The configuration is as follows. **Bit 1** / **Bit 0** / **Drive Selected** 0 / 0 / Drive 0 0 / 1 / Drive 1 1 / 0 / Drive 2 1 / 1 / Drive 3
2	Double-density enable	When low (0), this bit enables the read/write electronics of the formatter/controller in double-density mode. Since single-density will never be run on the system, this bit should always be low.
3	Motor on	When set (1), this bit turns on the motor if W9 is installed. When cleared (0), the motor is under the control of a three second delay before it is shut off.
		NOTE **When the motor is first turned on using this bit, a one second software delay must be observed before accessing the drive.**
4	Z80 interrupt	When low (0), it means that the interrupt line of the Z80 CPU is asserted low (0). When high (1), no interrupt is pending.
5	Drive ready	This bit indicates the status of the drive ready line of the interface. It is a read-only bit.
6	Disk drive controller interrupt	When set (1), the disk drive controller has gone through a control sequence that normally would end in an interrupt. It is cleared by reading the floppy status register.
7	Disk drive controller data request	This is a read-only bit that is a direct copy of the bit in the disk drive controller status register with one exception — the case of issuing a read or write sector command with DRQ still asserted.
		NOTE **When a command is issued, bit 7 is cleared internally (disk drive status) but not externally. Therefore, if the DRQ bit is set, the data register should be read in order to reset the external DRQ line, before issuing read or write commands.**

6.6.16 Communications Status Register (88H)

This read-only register holds the status of modem control signal lines on the communications port as well as the status of the ROM enable bit. The communications status register format is shown in Figure 6-42. Table 6-31 describes the bits.

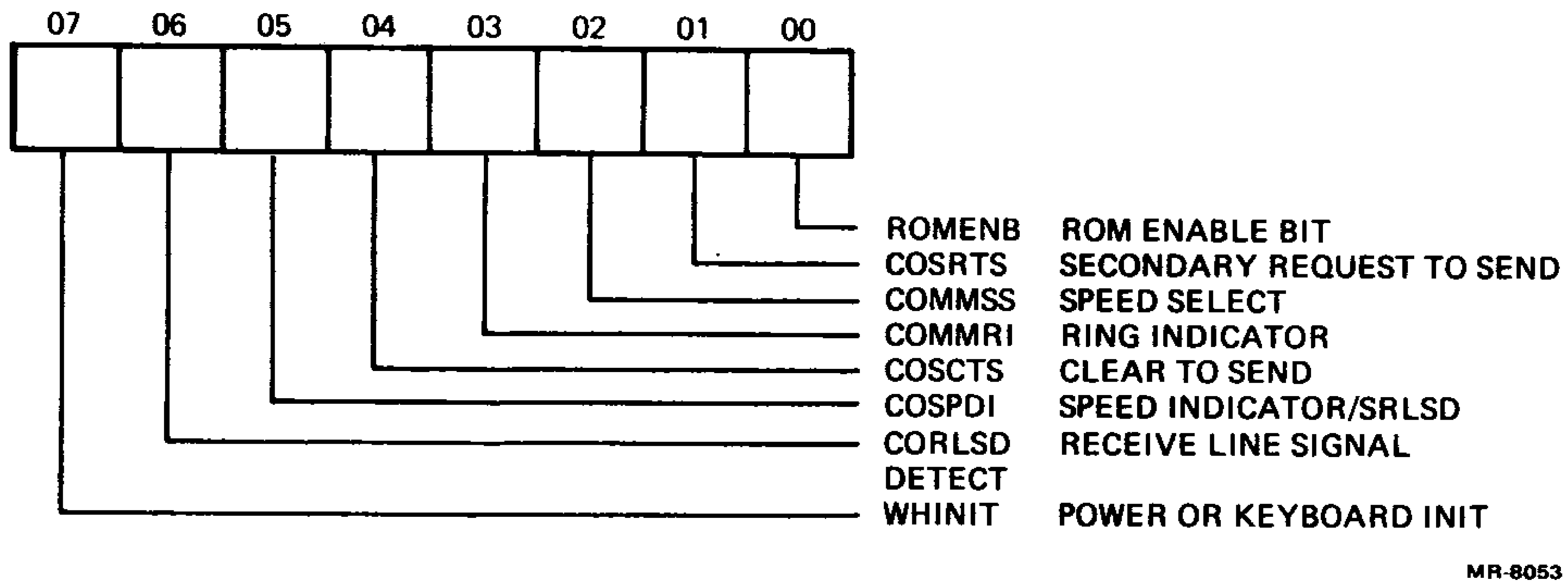


Figure 6-42 Communications Status Register Format

Table 6-31 Communications Status Register Bit Description

Bits	Description
0	When clear (0), this bit indicates the presence of the ROM starting at location 0000H. When set (1), the ROM is disabled and 64K bytes of RAM is available to the user. This bit represents the status of bit 0 in the diagnostic write register (98H).
1	This bit reflects the status of the SRTS line of the communications port as set by bit 6 of the communications control register.
2	This bit reflects the status of the speed select line of the communications port as set by bit 7 of the communications control register.
3	This bit reflects the status of the ring indicator line of the communications port.
4	This bit reflects the status of the clear to send line of the communications port.
5	This bit reflects the status of the speed indicator line or the secondary receive line signal detect line of the communications port.
6	This bit represents the status of the receive line signal detect line of the communications port.
7	This bit allows diagnostics to determine whether the system was initialized by a power on INIT or a keyboard initialize. After power on INIT, this bit will be set and should be cleared by a dummy read of register 90H so that subsequent initializes through the keyboard are detected by a low (0) condition.

6.6.17 Communications Control/Baud Rate Select Register (90H)

Bits 0–2 in this register select the printer baud rate. Bits 3–5 select the terminal port's baud rate while bits 6 and 7 toggle modem signals. This is a write-only register.

The communications control/baud rate select register format is shown in Figure 6-43. Table 6-32 describes the bits.

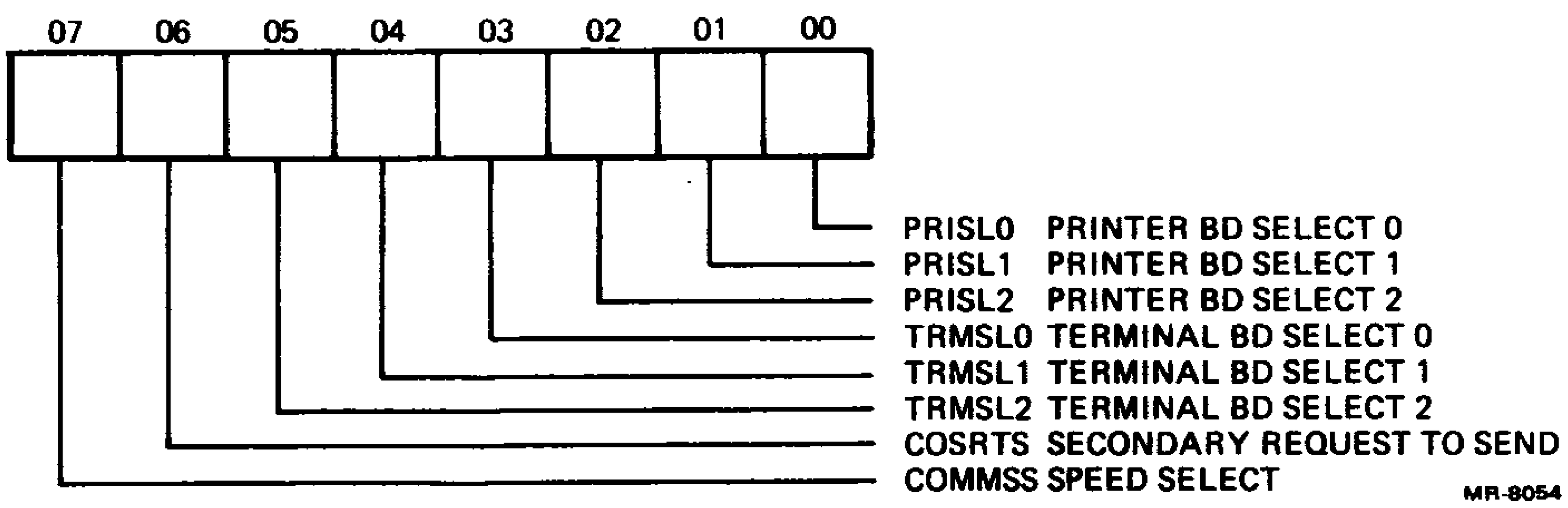


Figure 6-43 Communications Control/Baud Rate Select Register Format

Table 6-32 Communications Control/Baud Rate Select Register Bit Description

Bits	Description
0–2	These bits hold the encoded value of the baud rate to be selected for the printer port.

Bits 2	1	0	Baud Rate
0	0	0	75
0	0	1	150
0	1	0	300
0	1	1	600
1	0	0	1200
1	0	1	2400
1	1	0	4800
1	1	1	9600

Bits	Description
3–5	These bits hold the encoded value of the baud rate to be selected for the general purpose terminal port.

Bits 5	4	3	Baud Rate
0	0	0	75
0	0	1	150
0	1	0	300
0	1	1	600
1	0	0	1200
1	0	1	2400
1	1	0	4800
1	1	1	9600

6.6.18 Interrupt and INIT Reset Register (90H)

This register must be read while in an interrupt service routine for the real time clock in order to reset the interrupt line. This is merely supplying a dummy read to clear the interrupt. Any data read back has no significance. The same dummy read operation must be done to reset the who initialized (WHOINIT) line (bit 7) of the communications status register so that the next initialize sequence can be recognized. A read also resets the write data output (bit 4) in the diagnostic read register. A read from this register resets both of the bits.

6.6.19 Diagnostic Write Register (98H)

This write-only register is used for diagnostic control purposes. The upper four bits (7–4) directly address four LEDs that are turned on during a power-up or an INIT. Also contained in this register is a bit used during diagnostic testing to loopback all communications transmitted data to the communications receiver inputs. The diagnostic write register format is shown in Figure 6-44. Table 6-33 describes the bits.

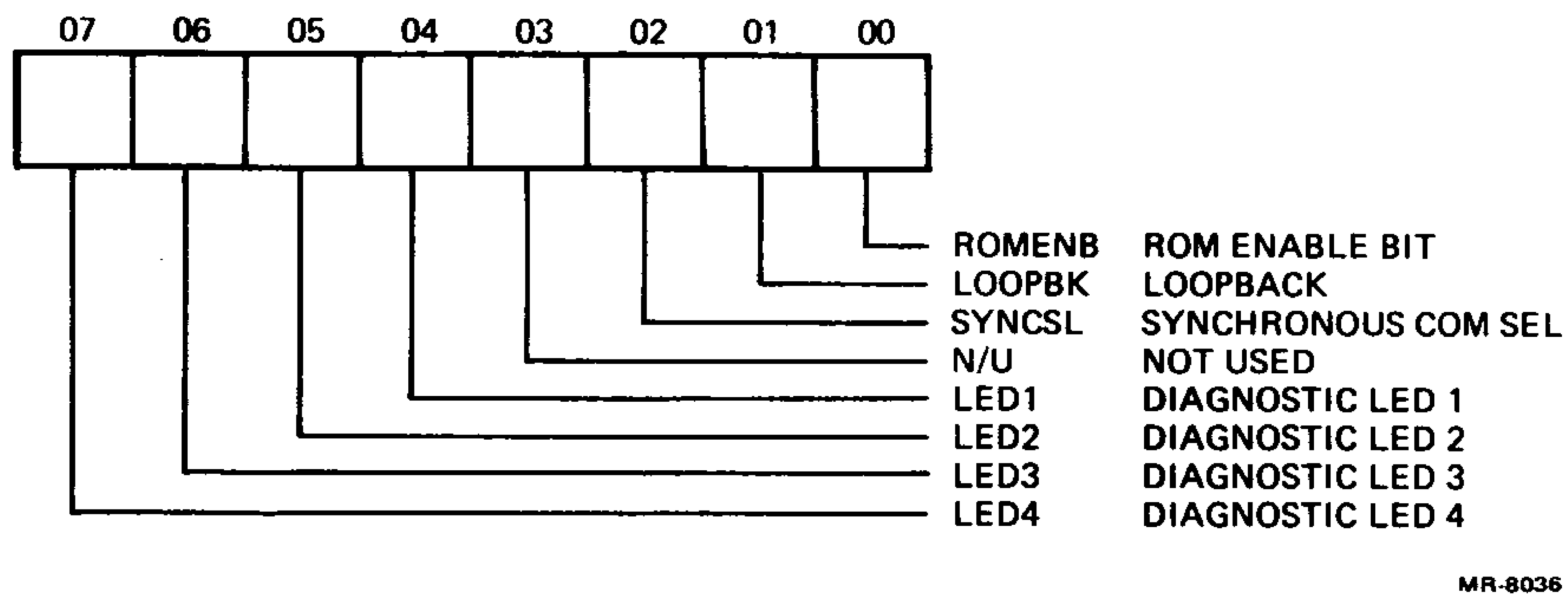


Figure 6-44 Diagnostic Write Register Format

Table 6-33 Diagnostic Write Register Bit Description

Bits	Description
0	This bit is cleared (0) upon an initialize to enable 8K bytes of ROM space starting at location 0000H. The ROM can be disabled by writing a 1 to this location, but the user must be careful not to write a 1 while executing code from ROM.
1	When set (1), this bit enables the transmit data of the communication and console ports to be looped back to the receive data of those same ports. Also, the transmit data of the printer and general terminal ports are looped back to the receive data line of the opposite port to allow checking of baud rates. This allows acceptable testability of the communications ports.
2	When this bit is set (1), the transmitter and receiver baud rates for the communications PUSART are supplied by the modem connected to the communications port. When low (0), the transmitter and receiver baud rates for the communication PUSART are the baud rates selected during VT180 set-up mode.
3	Not used.
4–7	These bits directly control the four LEDs on the VT18X control module. They are cleared upon an INIT, turning the LEDs on. When the bits are set, the LEDs are turned off.

6.6.20 Diagnostic Read Register (A0H)

This read-only register allows diagnostics to read signals from the disk drive interface connector so as to determine, as much as possible, controller functionality. The latched write data bit is latched so that the diagnostic can see if data is being written out. This bit is reset by a read to the address of 90H. The diagnostic read register format is shown in Figure 6-45. Table 6-34 describes the bits.

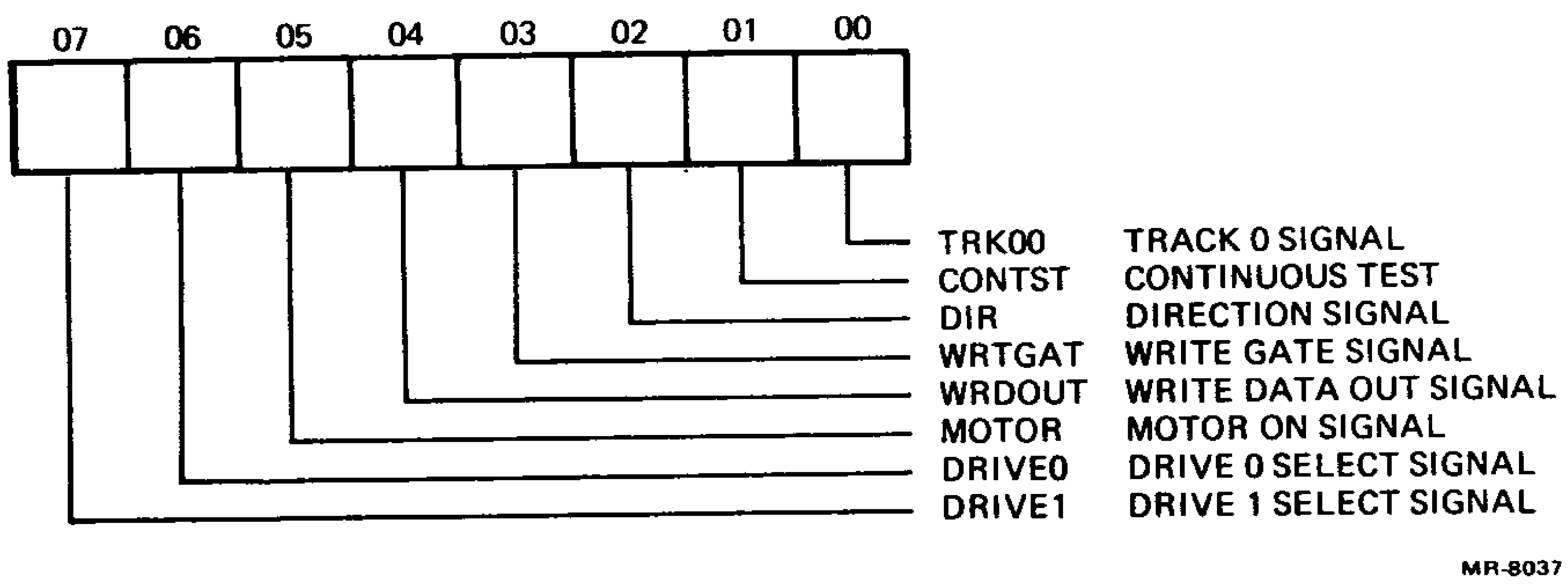


Figure 6-45 Diagnostic Read Register Format

Table 6-34 Diagnostic Read Register Bit Description

Bits	Description
0	When set (1), this bit informs the formatter/controller that the R/W head is positioned over track 0.
1	This bit is used only for manufacturing testing. It is set to 1 for normal operation.
2	When set, this bit indicates that the R/W head is stepping away from the spindle. When low, the R/W head is stepping toward the spindle.
3	When cleared, this bit indicates that writing may be performed.
4	When set, this bit indicates that write data has been sent to the disk drive.
5	When set, this bit indicates that the disk drive motor is turned on.
7, 6	These bits indicate which disk drive is currently selected. The bit indications are as follows.

Bit 7	Bit 6	Drive Selected
0	0	Drive 0
0	1	Drive 1
1	0	Drive 2
1	1	Drive 3

6.7 VT180 PADDLE BOARD DESCRIPTION

The VT180 paddle board is a printed circuit board (Digital part number 50-15149) that is 11.45 cm (4.51 inches) wide and 12.47 cm (4.91 inches) high. The printed circuit board contains a 25-pin, D-type EIA connector for the printer port, a jumper, a 16-pin socket, and a 40-pin edge connector that plugs into the STP connector on the terminal controller module. The printed circuit board also contains pull-up resistors for modem control signals and filter components needed to satisfy FCC requirements. The 16-pin socket is used to connect signals between the STP connector and the VT18X control module. Printer, communications clocks, and general purpose serial port signals are supplied by the 16-pin ribbon cable connecting the terminal controller module and the VT180 paddle board. Table 6-35 describes the 16-pin IC socket (J2) connnector signals, and Table 6-36 lists the printer port J1 signals.

Table 6-35 VT180 Paddle Board Signals

J2 Pin No.	Mnemonic	Direction*	Description
1	INIT	In	When asserted high, the VT100 is issuing an initialize to the VT18X control module.
2	TRM XMT DATA	Out	This signal is the transmitted data line to the 25-pin, D-type connector extending from the terminal controller module.
3	CON CLK	In	This signal is the local clock that the VT180 uses to talk with the VT18X control module. This signal is a 15.7 k baud signal that originates in the terminal controller module.
4	PRI XMT DATA	Out	This signal is the transmitted data line to the 25-pin, D-type connector extending from the VT180 paddle board.
5	GND		This is the logic ground between the terminal controller module and the VT18X control module.
6	COM RXC	In	This signal is the communications receive clock. The signal frequency is set through the VT180 SET-UP B mode as the value called R SPEED XXXX, where XXXX multiplied by 16 is the frequency of this signal.
7	COM TXC	In	This signal is the communications transmit clock. The signal frequency is set through the VT180 SET-UP B mode as the value called T SPEED XXXX where XXXX multipled by 16 is the frequency of this signal.
8	MFU1	Out	This signal is the printer baud rate of the printer port on the VT18X control module. This signal is not used in the VT180.
9	PRI REC DATA	In	This signal is the received data line from the 25-pin, D-type connector extending from the VT180 paddle board.
10	CON XMT DATA	Out	This is the transmitted data line to the terminal controller module via the STP connector.

*Direction of these signals as viewed from the VT18X control module.

Table 6-35 VT180 Paddle Board Signals (Cont)

J2 Pin No.	Mnemonic	Direction*	Description
11	TRM DTR	In	This signal is the data terminal ready signal from the 25-pin, D-type connector supporting the general purpose serial port.
12	CON DTR	In	This is the data terminal ready signal from the terminal controller module.
13	GND		This is a logic ground between the terminal controller module and the VT18X control module.
14	TRM REC DATA	In	This is the received data from the general purpose serial port.
15	PRI DTR	In	This is the data terminal ready signal from the 25-pin printer connector.
16	CON REC DATA	In	This signal is the received data input from the terminal controller module.

*Direction of these signals as viewed from the VT18X control module.

Table 6-36 Printer Port Signals

Pin Number	Signal Description	Mnemonic	Direction*
1	Protective ground	PROT GND	
2	Transmit data	TXD	Out
3	Receive data	TXD	In
6	Data set ready	DSR	In
7	Signal ground	GND	
20	Data terminal ready	DTR	Out**

*Direction of these signals as viewed from the VT18X control module.
**This output is always asserted high.

6.8 VT100 MONITOR

Two monitors have been used in VT100 production. Early VT100s used a monitor manufactured by Ball Brothers that is identified by Digital part number 30-14590. (For a description of the Ball Brothers monitor, refer to the *VT100 Series Technical Manual.*) Later terminals used a monitor manufactured by Elston, and this monitor is identified by Digital part number 30-16080. Most of the circuitry in these monitors is standard television technique, and this description simply highlights the signal path. An overview of the general principles of the horizontal section is included since this circuit is not intuitively understandable from an examination of the schematic. It is also the likely candidate for failure because of high stresses in the components.

6.8.1 Elston Monitor Board Description (Digital part number 30-16080)

6.8.1.1 Video Driver – The cathode driver stage gets its operating supply of 38 volts from a winding of the flyback transformer. R108 is the collector load resistor. C101 bypasses the emitter resistor to improve high frequency response. The stage is intended to be biased by the driving circuit (direct video out in the terminal controller). R105 couples the video signal to the cathode limiting current flow if the CRT arcs.

6.8.1.2 Brightness – The brightness control circuit gets its −150 volt operating supply from the horizontal output circuit. A charge pump (C104, C105, CR103, CR104) produces a large negative voltage by inverting the large positive swings in the stage. The brightness voltage returns to the +38 volt video output power supply rather than ground, to allow the brightness control output to vary from −42 to +17 volts. The brightness control potentiometer R109 varies the bias on the first grid of the CRT. C107 bypasses currents resulting from internal CRT arcs from the high voltage anode and also bypasses video signals from the grid to ground.

6.8.1.3 Vertical Oscillator – The vertical oscillator receives its synchronizing drive through inverter-buffer Q298. R331 and C314 are a low pass filter on the input for noise immunity. The input is ac-coupled so that if the drive stops in either a high or low state, the circuit can self-oscillate to keep the beam moving on the CRT.

Basically, the oscillator is an RC timer with R333 and R334 through CR304 charging a capacitor made of C318 and C319 in series. As the voltage across the capacitor rises, emitter follower Q309 drives the output amplifier Q310 so that its collector current rises at the same rate. CR304 is two diode drops to compensate for the drops in Darlington Q309 so the voltage at the base of Q310 is the same as the voltage at the top of C318. When Q308 receives a vertical drive pulse, it discharges the capacitor.

R341 and R342 are positive feedback to the junction of C318 and C319. As Q310's emitter voltage rises with increasing current, the two resistors couple that voltage back to the timing capacitor. This makes the voltage across the capacitor rise faster than it would with only the charging current from R333 and R334. But because the rise in capacitor voltage causes Q310 to turn on more, the feedback voltage increases as well. The exponential rise in Q310's output current that results closely matches the variations in L301's current. This is explained more under Linearization (Paragraph 6.8.1.6).

6.8.1.4 Self-Oscillation – If the vertical circuit does not receive a drive signal, it oscillates by itself to keep the electron beam moving to prevent a phosphor burn. The self-oscillation period is longer than the period between vertical drive pulses so the drive pulses, when present, always control the vertical scanning rate.

Without a drive signal, Q308 is off. The regular RC circuit produces a rising voltage at the base of Q310. While Q310's output moves the electron beam, its base voltage is coupled to Q308 through R335 and CR302. When the voltage rises above the diode drops of CR302 and Q308 base-emitter junction, Q308 turns on, discharging the timer and cutting off Q310. The retrace voltage that forms at L301 is coupled by

R344, C316, and R339 back to Q308 to keep it on long enough to complete a retrace even though the voltage from Q310's base (that started the cycle) has started to decrease. After the voltage at L301 falls (due to current flow to the yoke), the drive to Q308 is gone, Q308 turns off, and the self-oscillation cycle begins again.

6.8.1.5 Vertical Output – Consider L301, which is a large inductor, to be a constant current source. Assume that the yoke starts with a current that deflects the beam to the top of the screen and that Q310 is off. The current flows out of L301 through C321 and into the yoke. Q310 now turns on with a gradually rising voltage on its base. Q310 thus draws an increasing amount of current from the junction of L301 and the yoke. Because L301's current is relatively constant, less current is available for the yoke; so as Q310's current increases the yoke's current decreases. Eventually Q310 passes all of L301's current and the yoke current is zero with the beam in the center of the screen. As the current in the collector of Q310 increases further, the current in the yoke reverses and adds to the current coming from L301. This opposite current deflects the beam toward the bottom of the screen. Now the vertical drive pulse turns Q310 off, and L301 produces a large positive voltage to try to maintain its constant current. This voltage rapidly reverses the current in the yoke and makes the beam return to the top of the screen very quickly. Q310 turns back on and the cycle repeats.

C320, R338, and R340 limit the voltage across L301 during vertical retrace.

6.8.1.6 Linearization – Because L301 is not an infinitely large inductor, it is not a perfect current source. Current through it decreases gradually until the beam reaches the center of the screen and then increases again toward the end of the cycle. This nonramp component of the current would cause character height to vary from top to bottom if allowed to pass to the yoke. The exponential drive to Q310 as a result of feedback causes Q310 to accept the varying current from L301 at the same time that a ramp current through the yoke is maintained.

6.8.1.7 Horizontal Driver – The horizontal driver receives a TTL level drive pulse from the terminal controller. R468 limits the base current to Q413. C435 provides noise immunity for the drive input.

When the input is high, Q413 is on. With pin 6 of transformer T403 pulled low by Q413 and with about half the supply voltage at pin 4, there is approximately 6 volts across the primary winding 4-6. The secondary winding 3-2 sees one quarter of this voltage across itself due to the 4:1 turns ratio, but no current flows because Q414's base-emitter junction is reverse biased. Meanwhile, current increases through winding 4-6 while Q413 is on, storing energy in T403's core. When the drive signal falls, turning Q413 off, winding 3-2 reverses polarity. Current now flows from T403 winding 3-2 through Q414's base-emitter junction, Q414 saturates, and the horizontal output functions as discussed in the following paragraphs.

When the drive signal goes high again at the beginning of horizontal retrace, Q414 needs to turn off very quickly to minimize dissipation. The purpose of opposite polarities in T403 is to force Q414 off by turning Q413 on. When Q413 turns on, winding 3-2 reverses polarity again and this voltage forces Q414's base-emitter junction into a reverse biased state, rapidly discharging Q414's stored base charge and cutting off Q414's collector current.

R470 limits the peak current through Q413. R470 and R471 (if present) limit the on time of Q414. C443 (if present) speeds up the turn-off of Q414. C436 limits the peak voltage that develops across Q413 caused by leakage inductance in the primary of T403 that prevents complete coupling of the primary energy into the secondary. C437 filters Q413's power supply.

6.8.1.8 Horizontal Deflection Operation – The horizontal output circuit consists basically of Q414, CR406, C438, C441, and the horizontal deflection yoke. Assume that the beam is at the center of the screen during a scan. Refer to the waveform diagram (Figure 6-50) for reference points T0 through T4.

T0: Right half of scan (Figure 6-46)

Initial Condition: The current through the yoke is zero. C441 is charged to +15 volts. Q414 is on.

Action: Current now flows out of the yoke through Q414, pushed by the voltage across C441. The voltage across C441 is nearly constant so the current through the yoke's inductance increases linearly. As the current increases, the beam moves to the right of the screen. The magnetic field building in the yoke stores energy.

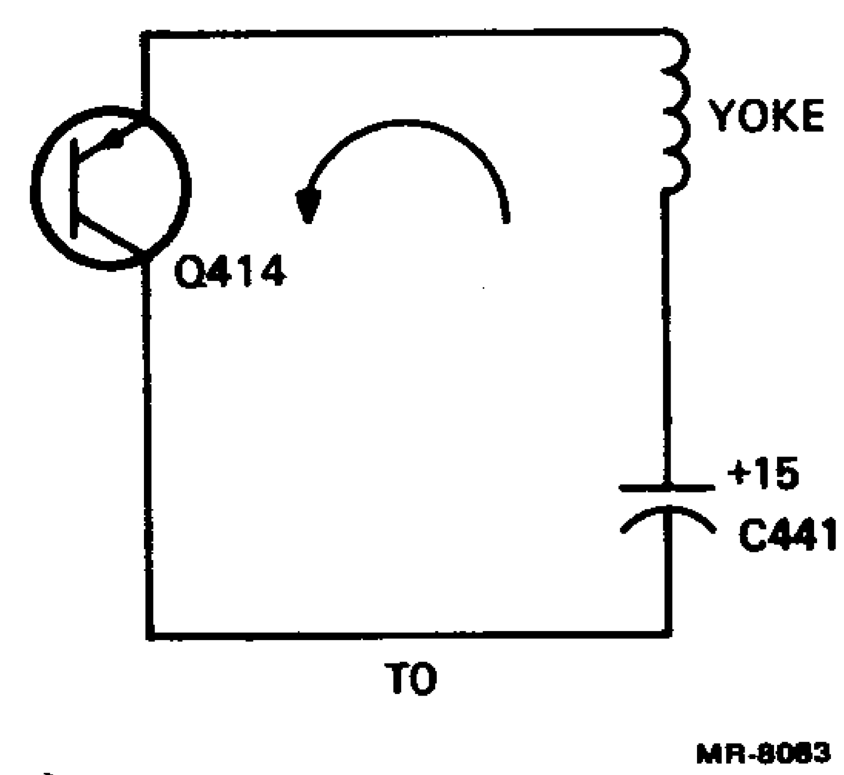


Figure 6-46 Horizontal Deflection Current – T0

T1: Start of retrace (Figure 6-47)

Initial Condition: Current out of the yoke is maximum. Q414 is switched off. C438, which had been grounded by Q414, has zero volts across it.

Action: Current continues to flow out of the yoke by inductive inertia as the stored magnetic field collapses. C438, which is a small valued capacitor, quickly charges to a high voltage. This voltage opposes current flow and causes a rapid reduction in current. The beam quickly returns to the center of the screen.

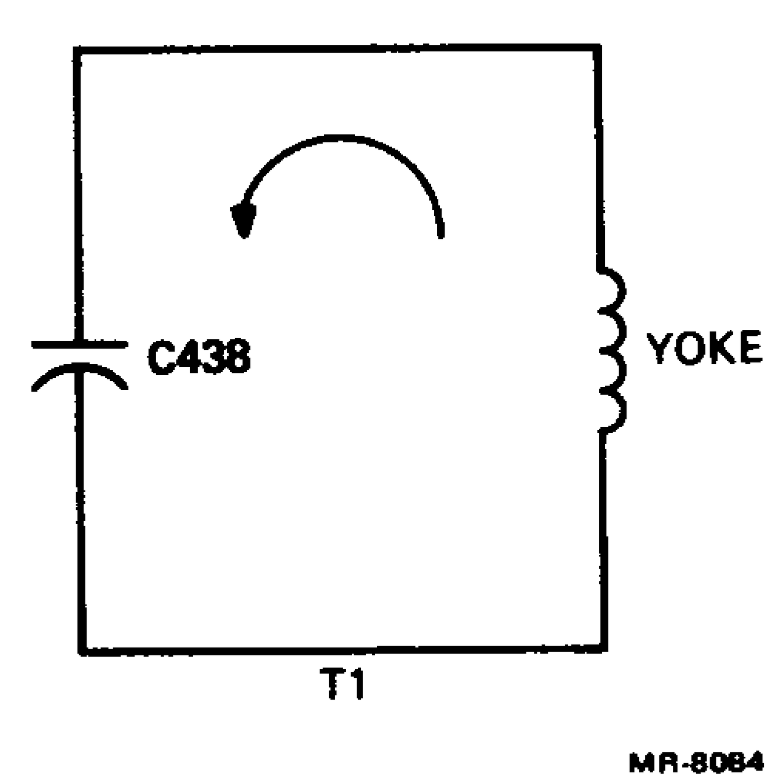


Figure 6-47 Horizontal Deflection Current – T1

T2: Middle of retract (Figure 6-48)

Initial Condition: Current through the yoke is zero. C438 is charged to +175 volts.

Action: The high voltage across C438 causes a rapid rise in current into the yoke. The beam moves to the left of the screen.

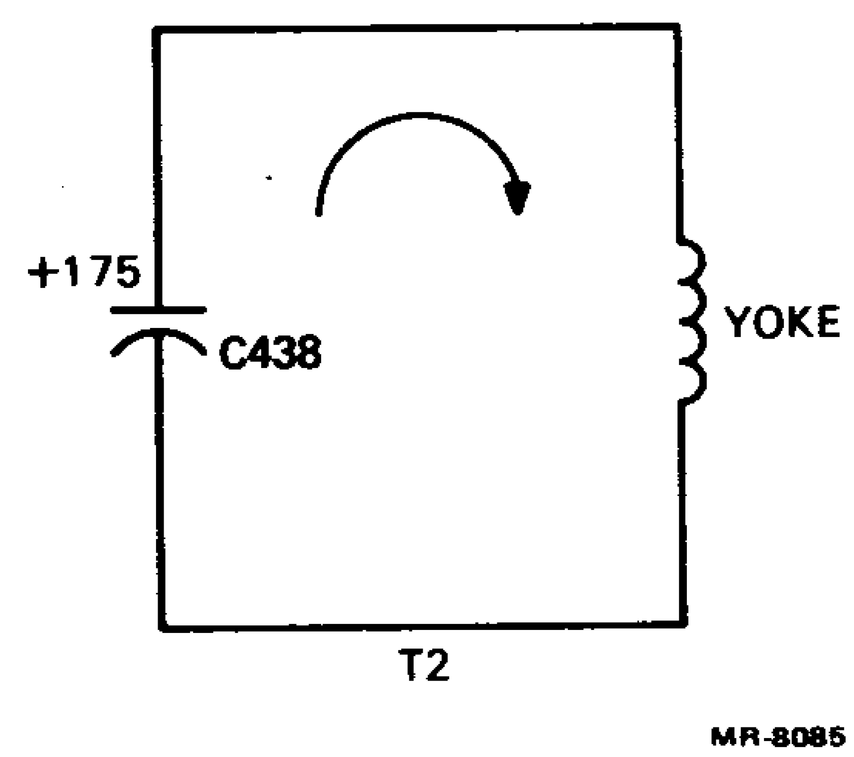


Figure 6-48 Horizontal Deflection Current – T2

T3: Start of scan (left half) (Figure 6-49)

Initial Condition: Current into the yoke is maximum. C438 is discharged.

Action: Inductive inertia makes the top of the yoke slightly negative, forward biasing CR406 to provide a return path for current out of the bottom of C441. The yoke current gradually decreases as the magnetic field collapses and discharges into C441 against the voltage across C441. The beam moves to the center of the screen.

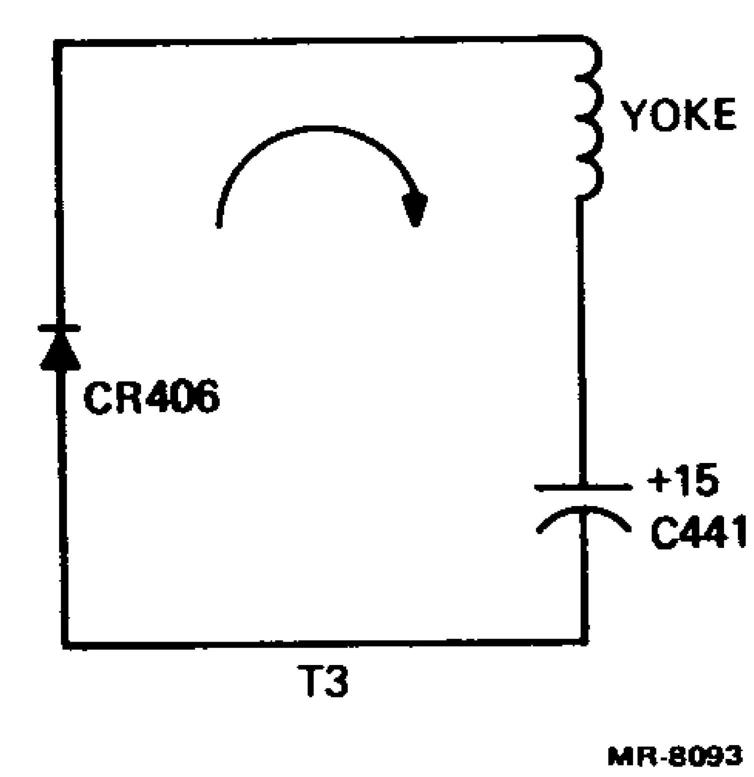


Figure 6-49 Horizontal Deflection Current – T3

T4: Return to T0

6.8.1.9 Horizontal Output Circuit – (Refer to Figure 6-50.) L403 adds a variable inductive reactance that controls current in the circuit to vary the scan width. L402 is a magnetically biased inductor whose reactance varies nonlinearly with changes in yoke current. This, with R481 and C442, provides correction for nonlinearity caused by the decaying exponential rate of current increase in the yoke caused by the yoke's resistance. It does this by allowing more voltage across the yoke at the end of the scan. This is needed, because as current increases, the voltage drop increases across the resistance of the yoke tending to reduce the rate of current increase.

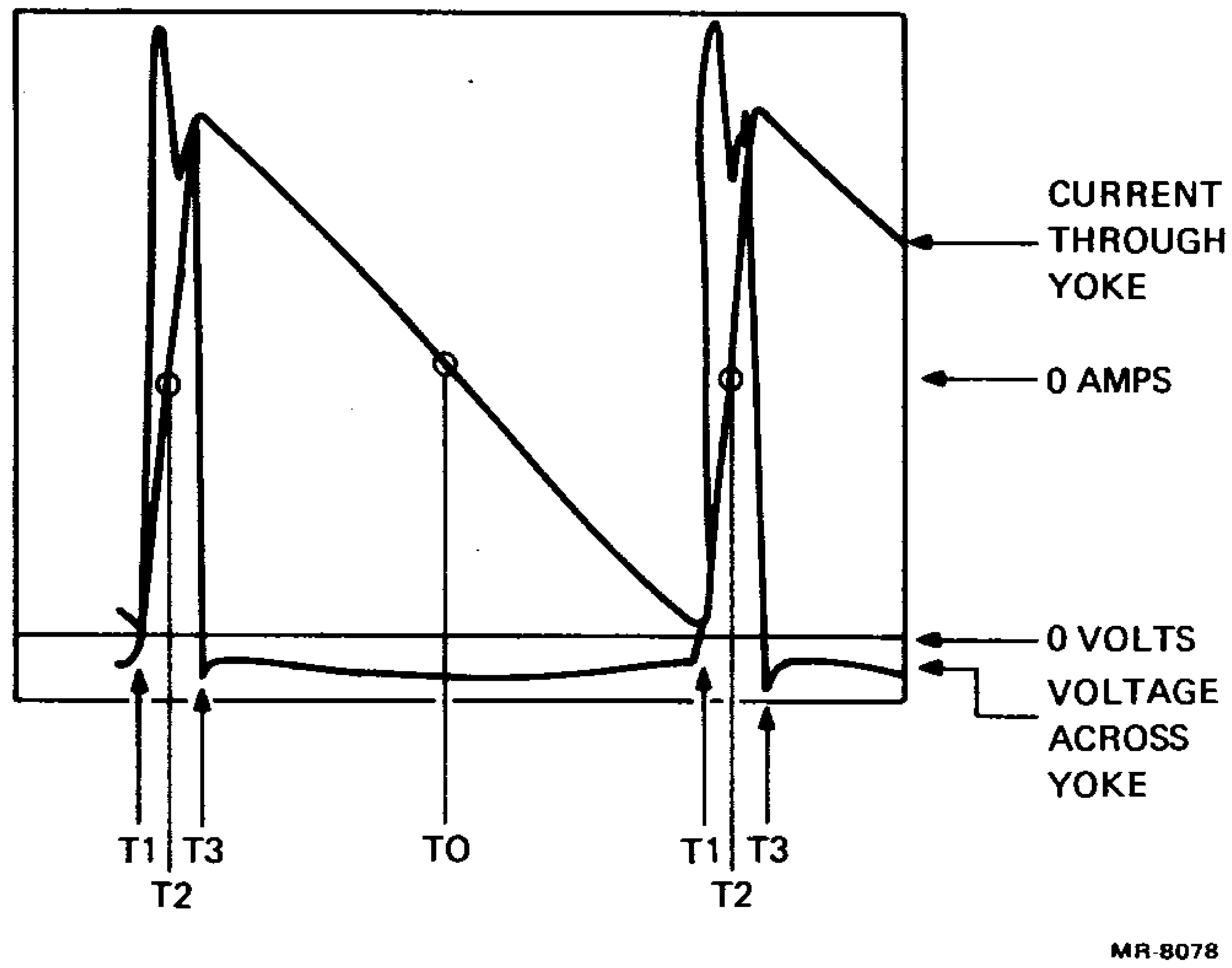


Figure 6-50 Horizontal Deflection Waveforms

Power enters the circuit through the primary of the flyback transformer. CR408 and C439 work with an autotransformer winding on the primary to boost the stage's operating voltage to +15 volts. The output circuit shuttles yoke current back and forth between C438 and C441, losing only a small amount of power in resistive losses. Therefore, the average current through the flyback primary is small (approximately 800 mA). C438 is relatively small so that the voltage drop across its reactance can provide S correction for the horizontal scan. This compensates for the difference between the arc of the tube face and the arc of the beam's deflection. Each time Q414 turns off, a 175 volt pulse, lasting the interval of horizontal retrace, appears at the dotted end of the flyback primary. This pulse passes into the flyback secondary to provide high voltages for the CRT.

6.8.1.10 High Voltage and Focus – When the 175 volt pulse appears on the flyback primary at retrace, the flyback secondary produces 12 kV, which is rectified by CR407 and filtered by the capacitor made by the aquadag (graphite) coatings on the inside and outside of the CRT's glass envelope. Screen and focus grid voltages of about 370 volts come from a lower voltage winding on the flyback and are rectified by CR409. For the cathode driver, 38 volts comes from another winding and is rectified by CR102.

6.9 POWER SUPPLY

The power supply is a switching supply that has 95 watts capacity with four separate voltage outputs. Figure 6-51 is a block diagram of the power supply.

6.9.1 Power Input

The input to the supply consists of an electromagnetic interference (EMI) filter, an on/off switch, a fuse, and a 120/230 voltage selector switch. Either on 120 Vac or 230 Vac input, thermistors R1 and R50 reduce the start-up inrush currents to safe levels. For 120 Vac operation a voltage doubler rectifier is used;

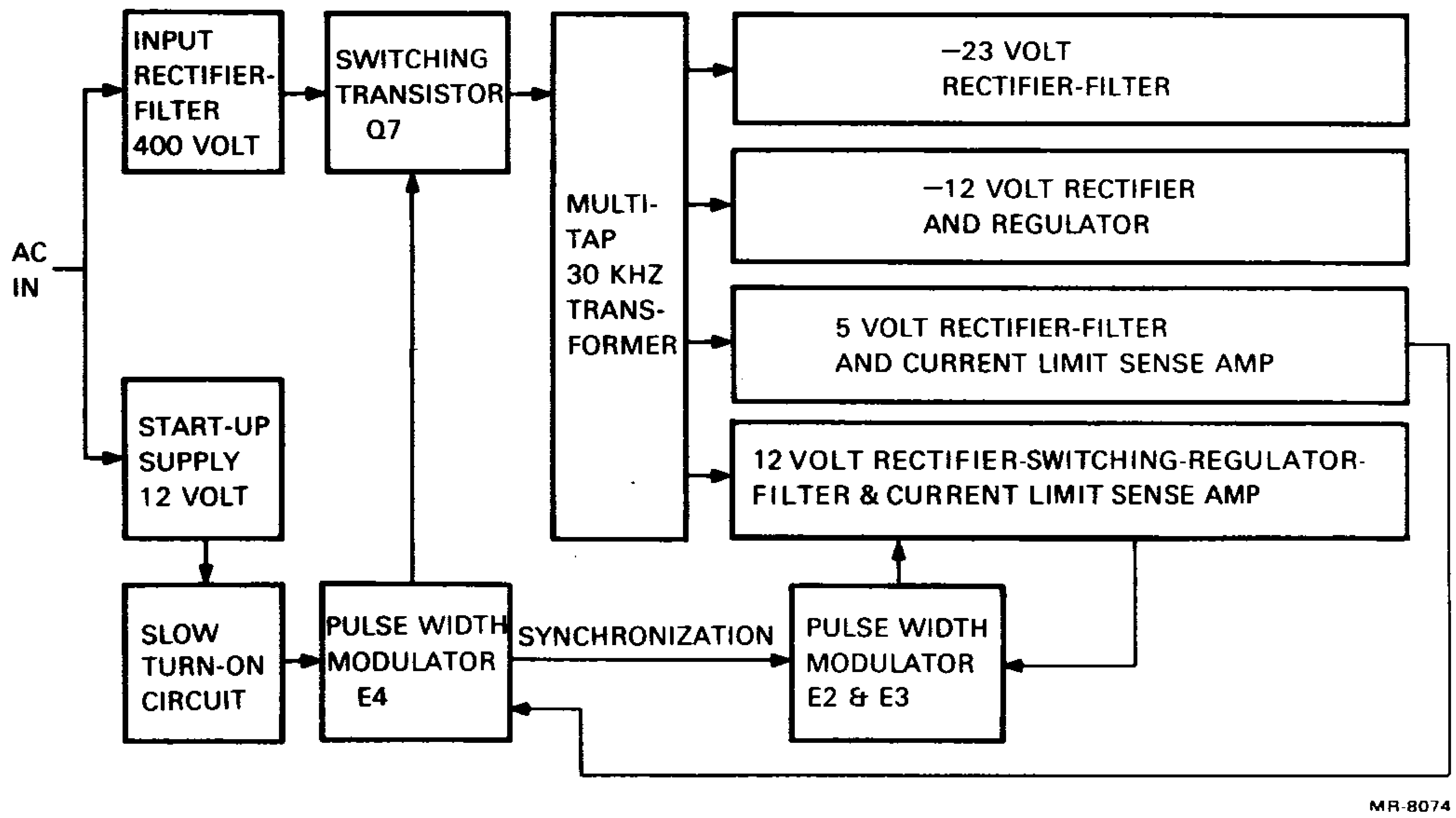


Figure 6-51 VT100 Power Supply Block Diagram

for 230 Vac operation a full wave bridge rectifier is used. The storage voltage across both C9 and C14 varies with the input line voltage from 200 to 360 Vdc. R19 and R20 are bleeder resistors.

6.9.2 Start-Up Circuit

Transformer T2 is a start-up transformer that supplies the power to start the control circuit. The ac voltage on the primary of T2 is stepped down, rectified, and filtered by C33. The dc voltage is applied to the input of +12 volt regulator Z2. The output passes through two diodes, D24 and D25, to the control circuitry. When the unit is turned on, the only voltage supplying power to the control circuit is from the regulator Z2. After the outputs come up, the +12 output is fed back through diode D34 to the control circuitry. Because it is higher than that delivered by the start-up circuit, this voltage will back bias D24 and D25, isolating the Z2 regulator. This scheme of returning the output through D34 enables the power supply to also meet its ride-through specification (ability to supply power during brief outages).

6.9.3 Control Circuit

The control circuit in the power supply is designed around the 3524 pulse width modulator (PWM) IC. It houses a voltage reference, error amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switcher, current limit circuit, and a shutdown circuit. Refer to the regulator IC block diagram in Figure 6-52 and the power supply timing diagram in Figure 6-53.

The oscillator frequency is determined by resistor R18 and C7. The ramp generated by C7 is used as a reference for the comparator. The discharge time of C7 determines the pulse width of the oscillator output pulse. This pulse is used as a blanking pulse to ensure that the outputs of the 3524 cannot turn on simultaneously. Capacitor C5 ensures that the blanking pulse is wide enough.

The error amplifier in the 3524 is a transconductance amplifier with an output (pin 9) impedance of approximately 5 megohms. Pin 9 is a convenient point to place the compensation network, R30, C17, and R13. It is also an ideal point to turn off the switching regulator and to put the slow-turn-on circuit. The slow-turn-on circuit consists of D39, R51, D40, and C34. When the power supply is initially turned on, pin 9 is pulled to ground by C34 through D39. As C34 charges slowly and exponentially, pin 9 follows, turning the power supply on slowly and exponentially. The current that charges C34 comes from pin 9 and the +12 volt start-up. Pin 9 operates at a dc level that is determined by the input error voltage into the amplifier. C34 eventually charges to +12 volts, thus back biasing D39. When the supply is turned off, C34 discharges through D40, allowing the supply to be ready for another soft start.

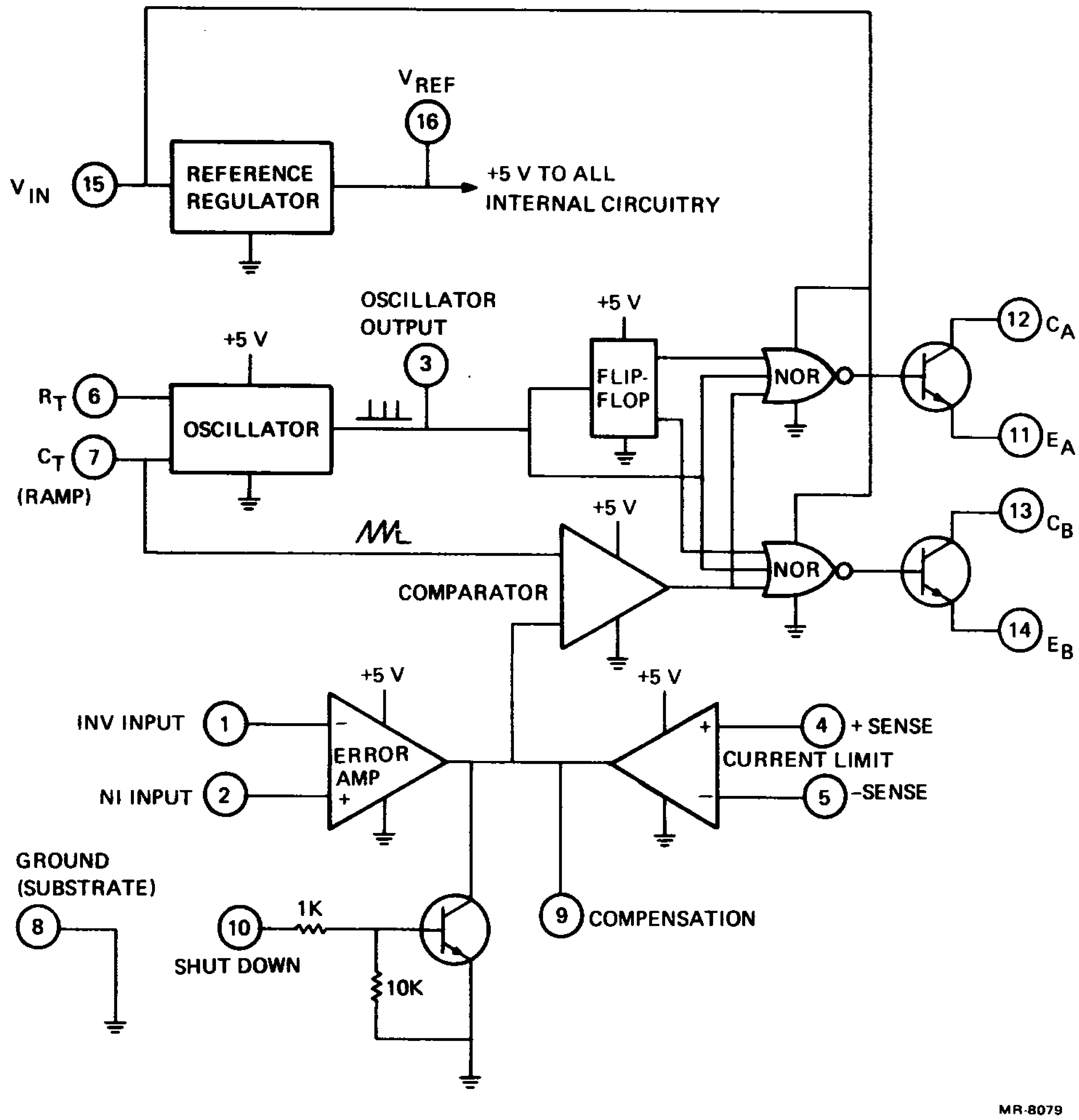


Figure 6-52 3524 Regulator Block Diagram

The inverting side (pin 1) of the input to the error amplifier is tied to the +5 volt output through a dividing network, R32 and R48. The noninverting side (pin 2) is referenced to a 5.1 volt zener, D38, through a divider network, R41 and R49. An error appearing at the input causes pin 9 (output of the error amplifier) to shift. This dc level shift is tied into an input of a comparator. As mentioned earlier, the ramp generated by C7 is tied into the other input of the comparator. This is the means by which the regulator is pulse width modulated.

The actual frequency of the oscillator is 60 kHz. The switching frequency of the power supply is one-half that of the oscillator, 30 kHz, because only one of the single-ended outputs is used. This output (pin 13) a pulse width modulated wave, turns transistor Q4 on and off. When Q4 is off, Q3 supplies base current to Q2, turning it on. D7 and D8 are antisaturating diodes. R14 limits the base drive, and R15 and C4 are a speed-up circuit to turn Q2 on and off fast. When Q2 is on, Q7 (high voltage switch) is off.

Current flows from +12 through R11, D6, and winding 5,6 of pulse transformer T3 through transistor Q2 to ground. The circuit remains in this state until the base drive to Q2 is removed by the control circuit. When Q2 turns off, the voltage across T3 winding 5,6 reverses, causing all the dotted ends of windings in T3 to become negative. Current starts to flow into the base of Q7. This causes collector current to flow. This current flows through winding 1,2 of T1, through the transistor and winding 2,1 of T3. The current in winding 2,1 of T3 produces current flow in windings 3,4 and 7,8 of T3. The action that takes place is

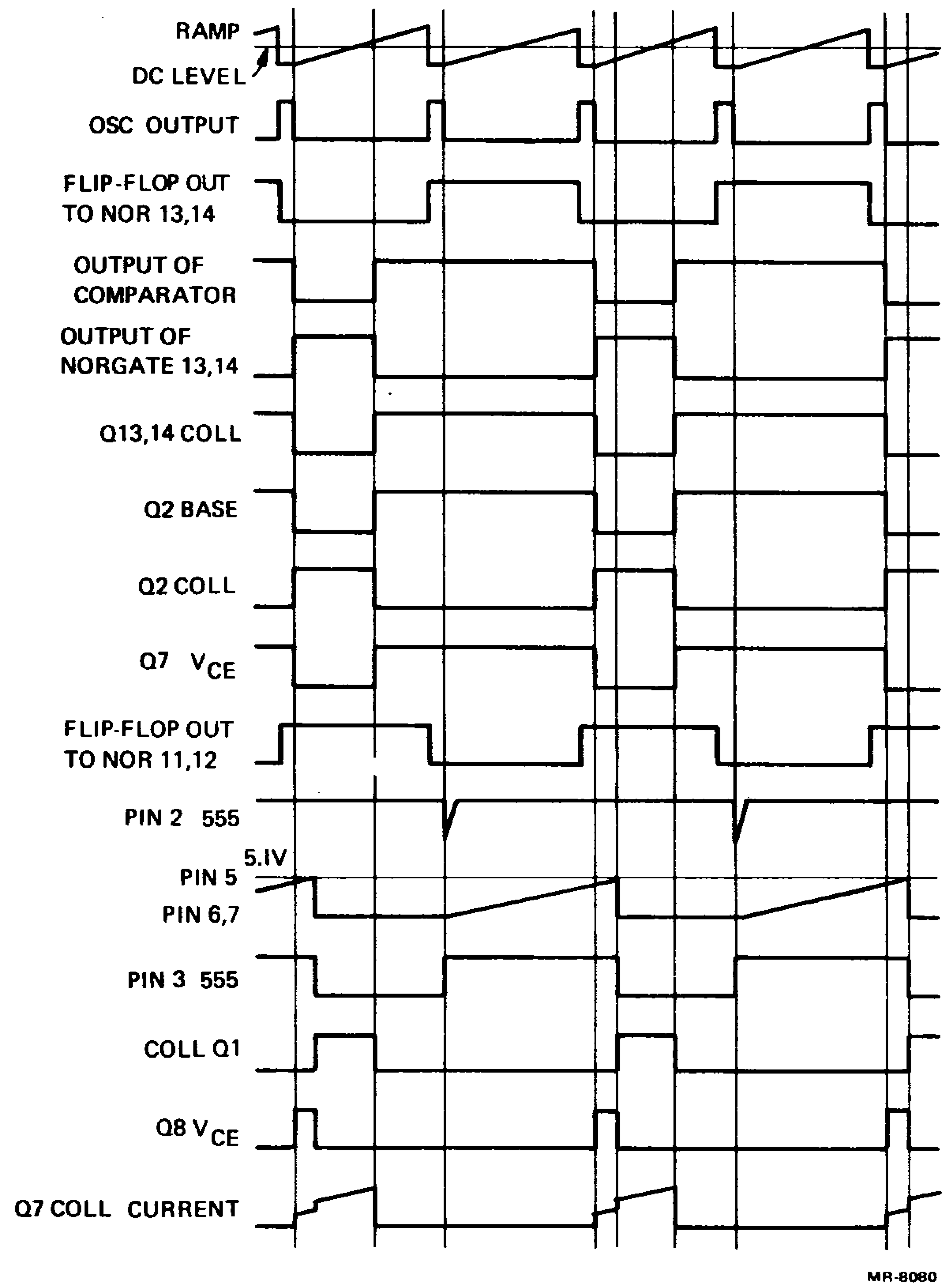


Figure 6-53 Power Supply Timing Diagram

regenerative and causes Q7 to snap on. When Q7 conducts, energy is transferred from the primary of T1 to the secondary. The positive voltage at terminal 5 of T1 charges capacitor C6 through D14 and R21. The voltage at terminal 5 depends on the conduction time of the switch. When the control circuit switches Q2 on, C6 discharges through D9, winding 5,6 of T3 and transistor Q2. The current through winding 5,6 of T3 makes all dotted ends positive on T3. The negative polarity on the base of Q7 turns it off. D11 is across T3 and Q2 for noise immunity. Diodes D41, D12, and D3 are antisaturation diodes. C19, R27, and D27 form the snubbing network.

Winding 1,3 of T1 is a reset winding. On turn-off, this winding clamps the collector of Q7 to two times the storage voltage. It is also used for resetting the high frequency transformer core.

6.9.4 Outputs

There are four secondary outputs. The −23 volt output is rectified by D28, filtered by C18, and passed on through a 300 ohm resistor. The output goes to two zeners mounted on the video board. The 300 ohm resistor limits power dissipation in the zeners and also dissipates all power under short circuit conditions.

The −12 volt output consists of a rectifier diode (D29), filter capacitor (C20), and a regulator Z1.

The voltage at winding 9,10 of T1 is rectified by D36 and goes into an averaging network L2 and C31.

The catch diode, part of D36, completes the conduction path when Q7 is off. When Q7 is on, there is a voltage on the secondary, with pin 9 being positive. D36 is forward biased, and current flows through L2. This causes the inductor current to increase at this time. With the switch open, stored energy in the inductor forces the current to continue to flow to the load and return through the catch diode (D39). The voltage across L2 is now reversed and is approximately equal to the output voltage. During this time the current in L2 decreases. The average current through L2 equals the load current. Since C31 keeps the output voltage constant, the load current will also be constant.

The +12 volt output circuitry works in the same manner except the voltage at winding 4,5 is turned on by Q8 and turned off by the voltage at terminal 5 going negative.

The current limit circuits for the +5 and +12 outputs have identical configurations; only some resistance values differ. The voltage at pin 5 of the comparator referenced to the junction of R16 and R37 is compared to the voltage drop across R37. When the voltage across R37 increases to a point where pin 6 is more positive than pin 5, E1 switches and pin 7 goes low, pulling pin 9 of E4 to ground and thus turning off the switching regulator.

The +12 volt control circuitry is synchronized to the 3524 pulse width modulator at a 30 kHz rate. When pin 12 of E4 is high, capacitor C15 charges up from the +12 start-up through R29, R26, and D13. The polarity on the capacitor is such that when pin 12 of E4 goes low, the emitter of Q6 is pulled negative with respect to the base, which is at ground. Q6 saturates, pulling pin 2 of E3 down and thereby allowing the ramp generated at pins 6 and 7 by C13 to ramp up. Pin 6 is the threshold pin. The input to this pin is compared to the voltage at pin 5. When the voltage at pin 6 is equal to that of pin 5, pin 7 discharges capacitor C13 and pin 3 of E3 goes low. Whenever the voltage at pins 6 and 7 is ramping up, the output of E3, pin 3, is high.

C13 is the timing capacitor for the +12 volt pulse width modulator. C13 is charged from a voltage-controlled current source. The voltage at pin 5 of E3 is connected to the 5 volt reference. Thus, when the voltage across C13 reaches 5 volts (pin 6 of E3), the output of E3 pin 3 drops low, turning Q1 off and thereby turning Q8 on. Q7 and Q8 are turned off simultaneously when Q2 is turned on. The pulse width that determines the length of time Q8 is on is determined by the rate of voltage rise on capacitor C13. The faster C13 charges, the longer Q8 conducts. The error voltage that determines the rate of rise on C13 is generated by error amplifier E2. The noninverting input of the error amplifier is referenced to D38, a 5.1 volt zener. The inverting input is divided up by R2 and R3 and senses the +12 volt output. Any difference creates an error signal on pin 6 of E2. This increase or decrease in voltage at pin 6 divided by R33 generates a proportional change in current through Q5, thereby changing the rate of voltage charge on capacitor C13. As described above, the change in rate of charge affects the pulse width.

R4, C1, and R5 are the compensating components of error amplifier E2. D1 and D2 are antisaturating diodes. R6 limits the base drive and R7 and C3 are a speed-up circuit to turn Q1 on and off.

6.9.5 Power Supply Specifications

6.9.5.1 Input Specifications

Voltage

Single-phase, two-wire	90–128 Vrms (switch-selected). 180–256 Vrms.

Frequency	47–63 Hz.
Current	2.2 Arms maximum at 115 Vrms. 1.1 Arms maximum at 230 Vrms.
Input power	250 VA apparent 150 W maximum.
Power factor	Ratio of input power to apparent power is greater than 0.6 at full load and minimum input voltage. The VT180 appears capacitive to the line.
Leakage current	When installed in a VT180 terminal, current to ground is 0.5 mA maximum. Each line to ground at 250 Vrms sine, 50 Hz.
Current limiting	When installed in video terminal, 3.0 A normal blow fuse.

Electrical magnetic interference susceptibility

Conducted transients	Single voltage transient without causing system degradation: 600 V at 2.5 W/s maximum.
Single voltage transient, survival	1000 V at 2.5 W/s maximum.
Average transient power, survival	0.5 W maximum.
Conducted cw noise	Unit operates without error at conducted noise levels up to 10 kHz–30 MHz: 3 Vrms. RF field susceptibility: 10 kHz–30 MHz: 2 V/M; 30 MHz–1 GHz: 5 V/M with power supply installed in video terminal.

Power line disturbance

Ride-through capability	The power supply provides a minimum of 20 ms ride-through during a power outage condition. Ride-through capability is at low line and full load. During this time, all power supply outputs must be within their specified limits.
Overvoltages	The power supply withstands an overvoltage of 110% of the maximum input voltage(s) specified in Paragraph 6.9.5.1 for one second without causing system degradation or damage.
Undervoltages, disturbances, and outages	The power supply is capable of withstanding undervoltage disturbance and power interruptions without physical damage.

Hi-pot	Input to frame for 1 min – 2.15 kV dc; input to output for 1 min – 2.5 kVrms.

Output specifications

General	The dc output distribution provides dc outputs. The dc distribution buses define dc output specifications. Distribution systems must be designed according to this document since no output voltage adjustments are provided.
Output power	+5 V at 1.5 A minimum to 11.0 A maximum. +12 V at 1.0 A minimum to 2.75 A maximum. −12 V at 0.0 A minimum to 0.5 A maximum. −23 V at 10 mA.

+5 V Specifications

Total regulation	±5%
Static line regulation	±0.75%
Static load regulation	±2.0%
Long term stability	0.1% – 1000 hrs
Thermal drift	±0.025% – degrees C
Ripple	150 mV peak-to-peak for frequencies less than 66 kHz
Dynamic load regulation	±2.2% (see notes)
Noise	1% peak at frequencies greater than or equal to 100 kHz (noise is superimposed on ripple)

−12 V Specifications

Total regulation	±5%
Static line regulation	±0.5%
Static load regulation	±1.0%
Long term stability	0.1% – 1000 hrs
Thermal drift	±0.025% – degrees C
Ripple	240 mV peak-to-peak for frequencies less than 66 kHz
Dynamic load regulation	±1.1% (see notes)
Noise	1% peak at frequencies greater than or equal to 100 kHz (noise is superimposed on ripple)

−12 V Specifications

Total regulation	±5%
Static line regulation	±0.5%
Static load regulation	±1.0%
Long term stability	0.1% - 1000 hrs
Thermal drift	±0.025% - degrees C
Ripple	240 mV peak-to-peak for frequencies less than 66 kHz
Dynamic load regulation	±1.1% (see notes)
Noise	1% peak at frequencies greater than or equal to 100 kHz (noise is superimposed on ripple)

−23 V Specifications

Total regulation	±10%
Static line regulation	±2%
Ripple	500 mV peak-to-peak

NOTES

1. **For all outputs, the long term stability and thermal drift specifications apply after a five minute minimum warmup, measured at the dc distribution buses with an averaging meter.**

2. **Dynamic load regulation is measured in +25% load steps from a starting point of 75% of full load. Measurements are made at the power supply terminals.**

3. **Zener diodes for −23 V supply are located at the load and not on the power supply.**

Ripple and noise	Ripple and noise must be measured with a wide band oscilloscope in the differential mode between ground and the output under test. The oscilloscope must be grounded so as to minimize spurious responses. The specification applies only to repetitive voltage variations that occur while operating with a constant input voltage and fixed load.

Overload protection

+5 V output	Current limit with foldback. Limit point is 18 A maximum; foldback is 6.0 A maximum.
+12 V output	Current limit with foldback. Limit point is 6 A maximum; foldback is 3 A maximum.
−12 V	Internal current limit of the three-terminal regulator is per Digital specifications PS-19-12048-02.
−23 V	Current limited to less than 150 mA.
Voltage adjustments	None.
Weight	1.68 kg (3.7 lbs) maximum.

6.9.5.2 Cooling – Cooling is by natural convection. Adequate space must be provided around the supply to allow a free flow of air.

6.10 KEYBOARD DESCRIPTION

The VT180 keyboard is a typewriter-like array of momentary, normally-open switches. The array is mounted in a small case with a speaker for audio feedback and electronics for interfacing the array to the terminal. The keyboard connects to the terminal controller board through a three-conductor cable that plugs into the back of the terminal cabinet. The cable carries power, ground, and a complex bidirectional data and clock signal. The terminal sends the clock signal and a status word that controls the LED indictors, the bell, and the keyboard scan process. The keyboard sends the row and column address of each key that is pressed. The terminal's microprocessor then translates that address into an ASCII character and transmits it serially to the host through a UART or performs internal actions such as set-up and no scroll. Refer to Paragraph 6.5.8 for a discussion of UART principles.

This section describes the operation of the keyboard and its interface to the hardware and software in the terminal.

6.10.1 Keyboard Block Diagram

Figure 6-54 is the keyboard block diagram. The bidirectional interface separates incoming data from outgoing data on the single signal line. Incoming data from the terminal contains a clock that passes directly to the UART and the address counter circuit. Then the data and clock are integrated. The duty cycle encoded data becomes serial data. The UART deserializes the terminal data and produces an 8-bit parallel output. These bits control the bell and LEDs and start address scanning, depending on which bits were set by the terminal in the keyboard status byte.

The address counters start on command and send row and column addresses to the keyboard switch array. When an address matches a key that is down, the key down signal strobes that address into the UART. The UART serializes the address and the bidirectional interface sends it to the terminal.

6.10.2 Keyboard UARTs

Information is exchanged between the terminal and the keyboard in serial form. One start bit, eight data bits, and one stop bit are transmitted using a clock derived from the horizontal timing circuits in the terminal. Besides timing the serialization of data in the terminal, the clock is also transmitted to the keyboard to time its circuits. The terminal data is a status byte that controls the keyboard by commanding key scans and other functions.

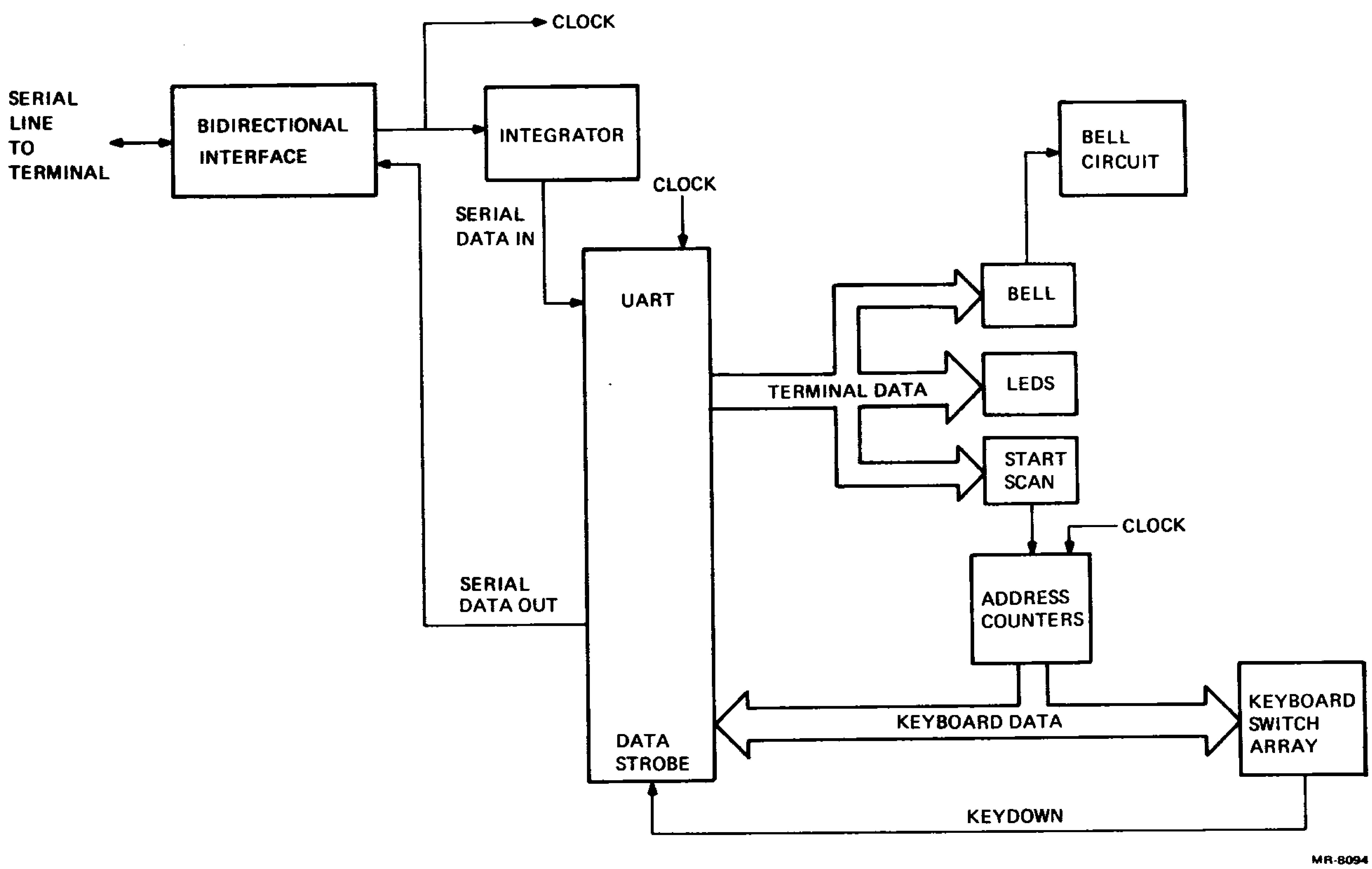


Figure 6-54 Keyboard Block Diagram

The keyboard transmits its data in the same format and with the same clock. Its data is the addresses of whatever keys are down during a scan. The last key address sent has the highest address possible and is always sent to indicate to the microprocessor in the terminal controller that the scan is complete.

6.10.3 Keyboard Status Byte

The terminal controls the keyboard through a status byte that it sends through the interface along with the keyboard clock. The first six bits of the 8-bit byte (Figure 6-55) control the on-line/local, keyboard locked, and four user-programmable LEDs on the keyboard. Every time the status byte is sent, it refreshes the LEDs even if no new action is being taken. The seventh bit is sent only once in a vertical interval and initiates the scanning process in the keyboard. The eighth bit, if sent only once, causes the keyboard speaker to click. (Keyclick is defeatable at set-up.) If the bit is sent approximately 200 times in a row for about a quarter second, it sounds a bell.

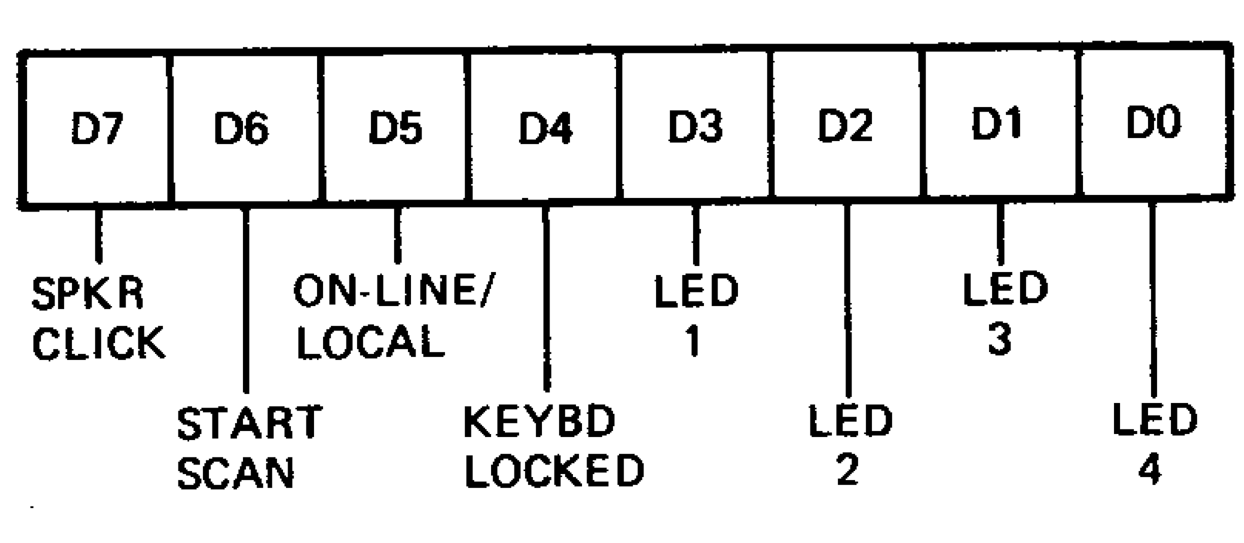


Figure 6-55 Keyboard Status Byte

The operating clock for the keyboard interface comes from an address line in the video processor (LBA4). This signal has an average period of 7.945 microseconds. Each data byte is transmitted with one start bit and one stop bit, and each bit lasts 16 clock periods. The total time for each data byte is 160 times 7.945 or 1.27 milliseconds. Each time the transmit buffer empty flag on the terminal's UART gets set (when the current byte is being transmitted), the microprocessor loads another byte into the transmit buffer. In this way, the stream of status bytes to the keyboard is continuous.

6.10.4 Key Address Counter

Keyboard addresses are outputs from a counter that correspond to locations in a keyswitch matrix. The counter can address all locations in the matrix. If a keyswitch is closed, the counter output addressing that location is transmitted. The address counter is a pair of 4-bit binary counters arranged so that only the top seven bits go to the switch matrix. These outputs also connect directly to the UART transmit data inputs. The output of the first bit in the counter is a squarewave with a period equal to the amount of time that each key is sampled during a scan. Key down L appears at the input to flip-flop E6 when the counter reaches the address of a key that is pressed. Half a sample period later, the first counter bit clocks the key down signal through flip-flop E6. The half period delay allows any glitches in the address counter to settle before key down asserts data strobe. Data strobe loads the UART transmit buffer with the address count present at the data input at that moment. That address count represents the key that was down when key down was asserted.

The UART, which is double-buffered, deasserts transmit buffer empty while the transmit (outer) buffer is full. This stops the counter by blocking the clock at gate E4. As soon as the data moves into the inner shifting register, the transmit buffer empties, TBMT is asserted, and the count continues. In this way, any number of key addresses can be sent to the terminal. The time the scan takes to finish varies with the number of keys down. On the first address load, when transfer from the transmit buffer into the shifting register is immediate, the UART reasserts TBMT almost immediately. For address loads later in the scan, the UART deasserts TBMT for a longer period because an address that loads into the transmit buffer must wait with the counter stopped until the previous transmission is done. Because the transmission time is 160 counts and the complete address scan takes only 128 counts, there is a minimum wait of 32 counts or about 20 percent of a character transmission time between the scan of address 7FH and the transmission of address 7FH if the first key in the scan was down. (Refer to Figure 6-56.)

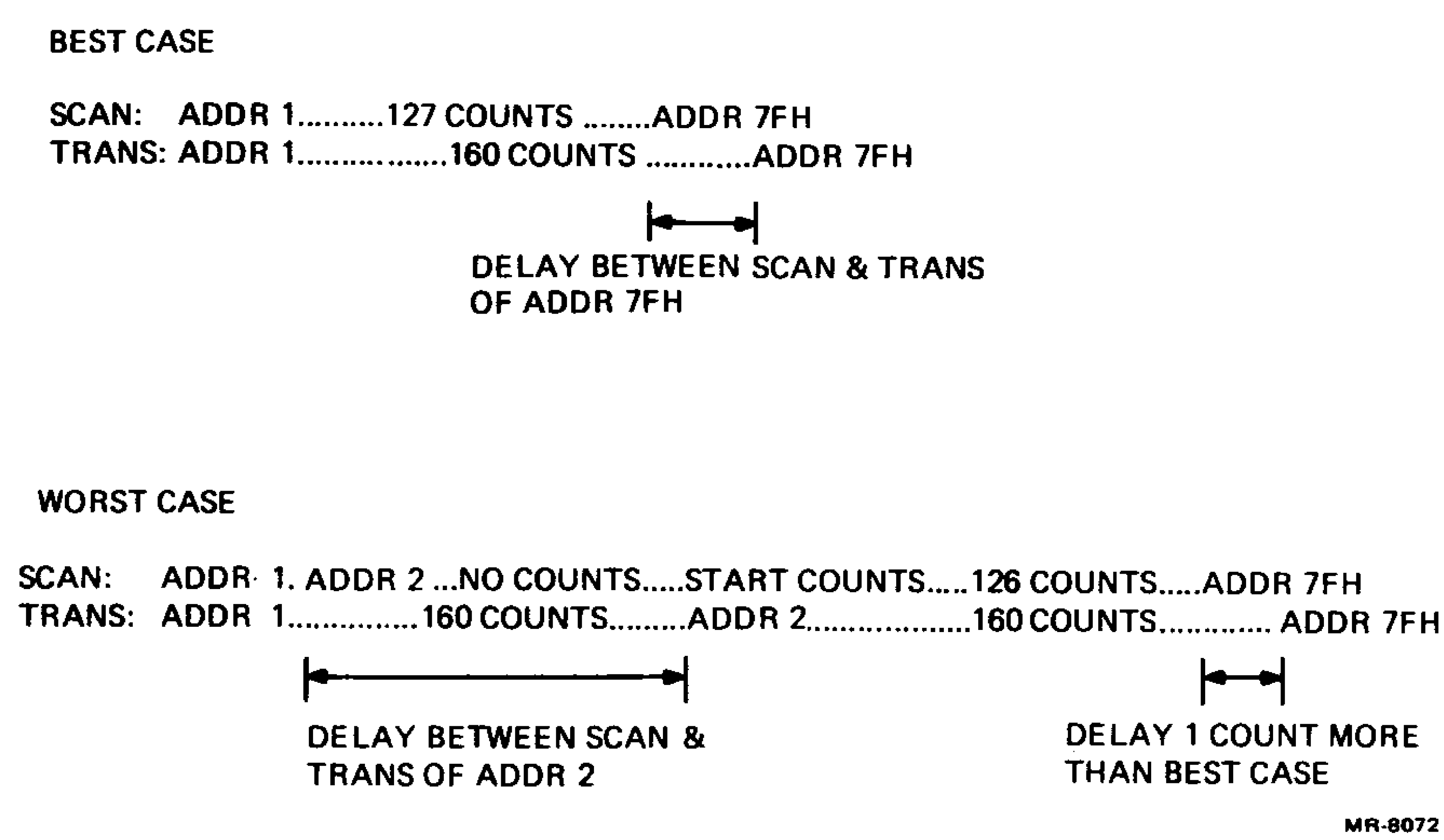


Figure 6-56 Key Address Transmission Delays

Because it is hardwired, the highest address (7FH) always asserts key down and gets transmitted, indicating end of scan to the terminal. The highest bit also clocks flip-flop E3, which clears the counters and stops the count. This is the only way that the scan is terminated. The scan begins again when the terminal sends the start scan bit in the status byte to the keyboard. When the data arrives, the UART asserts its data available flag. On the next clock transition, flip-flop E6 passes a short, clock-synchronized data available pulse to gate E5, resetting the flag in the process. E5 combines the data available pulse with the start scan bit, if present, to clear E3 and allow the count to begin.

After the terminal starts the scan, it waits for the 7FH address and then for a vertical interrupt (a synchronizing signal) before it will start the scan again. If there are a lot of keys down, the scan may take more than one vertical interval to finish. The keyboard ignores further requests to scan until the current scan is complete.

Here is a formula that estimates the delay between the time that the terminal asserts the start scan bit at its UART and the time that the terminal UART asserts data available upon receiving the final address 7FH. The clock driving the address counter and UART has a period of 7.945 μs. The serial transmission of an address takes 160 clock periods (16 clocks per bit, 8 data bits, 1 start and 1 stop bit).

160	start scan command word to keyboard
+ m	counts to first key
+ n × 160	for n keys down
+ 160	transmission of 7FH

Total × 7.945 = microseconds

For example, suppose that one key, #24, is down.

160	start scan command word to keyboard
+ 24	counts
+160	transmission of key #24 address
+160	transmission of 7FH

504 × 7.945 = 4004 microseconds (4.0 μs)

6.10.5 Key Scanning and Address Formation

The keyboard is an array of contact pairs arranged in 16 rows and 8 columns (Figure 6-57). One side of each pair is connected to all the others in its column and each column connects to +5 volts through a resistor. Each of the eight columns also connects to an input on the eight-to-one multiplexer E14. The other side of each contact pair connects to all the others in its row and to an output on one of the one-to-eight demultiplexers E11 and E13. The seven outputs of the keyboard scan counter control the multiplexer and demultiplexers. The rows are selected by the lower four bits and the columns by the upper three.

A low input to the selected column line on the multiplexer causes a key down L signal. If a key is pressed when the row and column address is not on its position, the unselected demultiplexer line is high and there is no change in level across the contacts. If the demultiplexer line is selected, it is low and the closed contact pulls the column low through the resistor. Each column is scanned top to bottom as the low four address lines count; then the next column is selected and scanned. The complete keyboard scan takes about 1 millisecond when no keys are down.

The last row and column position (address 7FH) is wired to always indicate key down. This value indicates to the terminal that the scan is ended.

COLUMNS

ROWS (LSD) \ COLUMNS (MSD)	7	6	5	4	3	2	1	0
0	9	.	8	7	↑	←	→	ALWAYS OPEN
1	3	,	ENTER	PF4	PF3			
2	6	5	2	PF2	PF1	↓		
3	–	4	1	0	BACK-SPACE	BREAK		DELETE
4		RETURN		LINE FEED	+ =	~ `	}]	RETURN
5	? /	> .	" '	| \	) 0	_ -	{ [	P
6	M	< ,	: ;	L	* 8	(9	I	O
7	SPACE BAR	N	J	K	^ 6	& 7	U	Y
8	V	B	H	G	% 5	$ 4	R	T
9	C	X	D	F	@ 2	# £ 3	E	W
A	Z	NO SCROLL	S	A	TAB	ESC	! 1	Q
B	SET-UP							
C	CTRL							
D	SHIFT							
E	CAPS LOCK							
F	ALWAYS CLOSED							

MR-8066

Figure 6-57 Keyboard Switch Array

6.10.6 Bidirectional Interface Operation

The terminal sends data and clocks to the keyboard; the keyboard sends data only. Transmission is asynchronous, full duplex, serial, 8-bit data with 1 start bit and 1 stop bit over a single signal line. Four states can exist on the line, representing the two signal states from each end of the line.

Both signals may coexist on the same wire, originate at opposite ends, and simultaneously communicate provided that sensing resistors are put at each end. The interface works by observing the voltage variations on its input (across the sensing resistor) while biasing the input in an opposite direction with its own output signals so that only input variations can cause enough change to exceed the threshold of detection.

6.10.6.1 Interface Line – Refer to the keyboard interface schematic, Figure 6-58. If one side of the line is at +12 volts and the other is at ground, then by Ohm's Law, the center of the two equal resistors will be at V/2 = 6 volts. If both sides are at 0 or 12, the center will be identically at 0 or 12. Thus the signal line can either have no current flow but with the junction of the two resistors at either 0 or 12 volts, or the junction can be at 6 volts with current flow to the left or to the right, thereby representing the four required states.

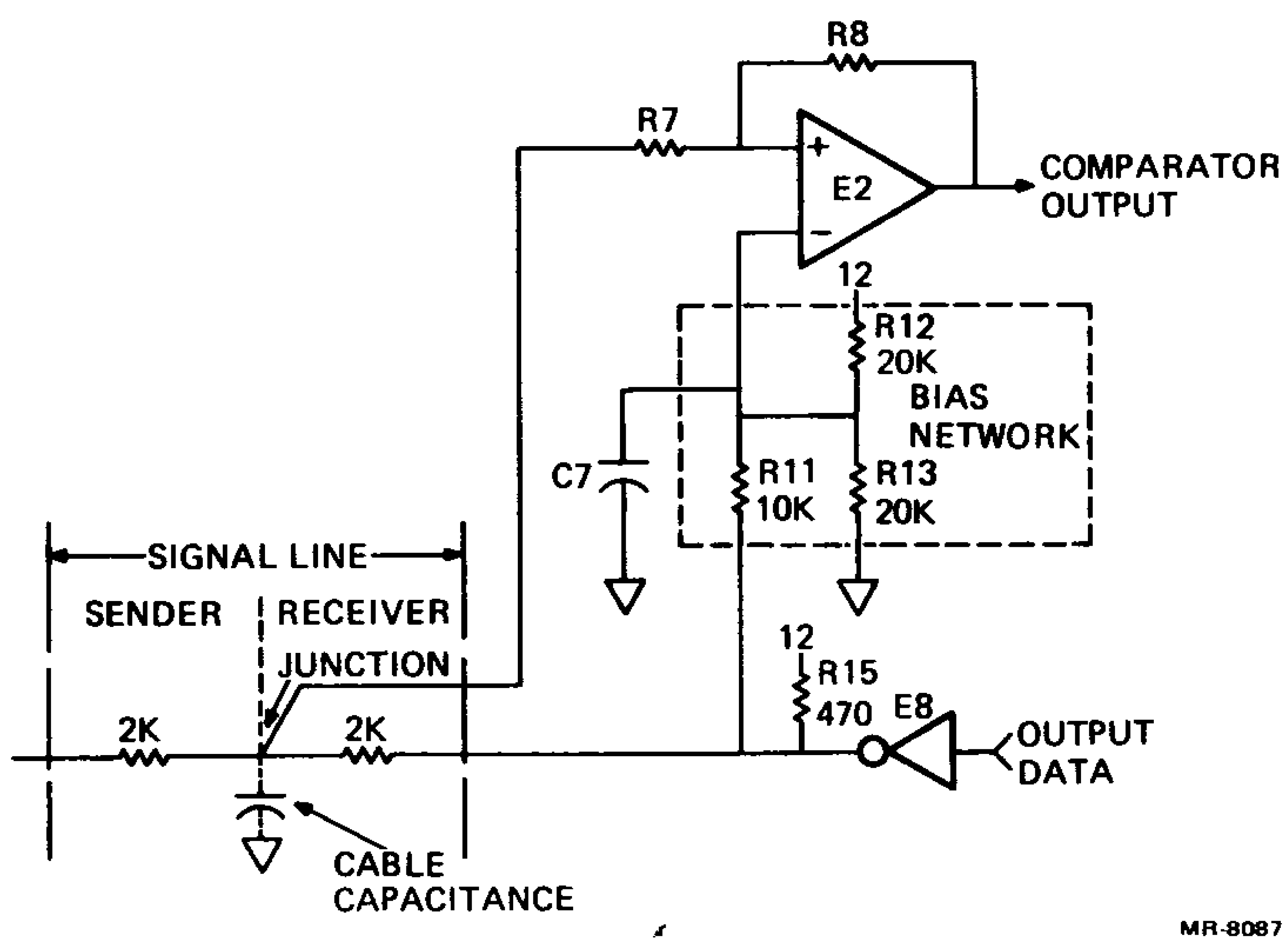


Figure 6-58 Keyboard Interface Circuit

6.10.6.2 Receiving Side – The receiving side of the keyboard interface separates the incoming signal from its own output by delivering a sample of its output to the inverting input of a comparator. Refer back to Figure 6-58. This provides an additional input for the comparator, which compensates for the variation that occurs on the noninverting input at the same time that the output changes. R12 and R13 (both approximately 20 kilohm) and R11 (10 kilohm) are a divider providing bias to the comparator. If E8 (an open collector driver) is off (high), then the end of R11 connected to E8 is essentially at +12 volts through R15 (470). The R11, R12, R13 divider outputs 9 volts at the junction of the three resistors. If E8 is on (low), the end of R11 connected to the output of E8 is at ground, and the divider outputs 3 volts.

Meanwhile, the signal from the other end of the signal line is admitted to the noninverting input of the comparator through a resistor (R7) whose value is small compared to the comparator's high input impedance. The positive feedback resistor R8 provides a small amount of hysteresis to improve the circuit's noise immunity.

For the case where the junction is at 12 volts, there is no ambiguity about what signal the sender is sending. The comparator must produce a high output because the sender is outputting a high level. (The receiver is also sending a high level but no distinction between the two needs to be made.) The bias network presents a 9 volt signal to the inverting input, so the comparator sees a +3 volt difference and goes high.

For the case where the junction between the sender and the receiver is at 0 volts, there is again no ambiguity. The comparator must produce a low output because both sender and receiver are outputting low levels. The bias network presents a 3 volt signal to the inverting input, so the comparator sees a −3 volt difference and goes low.

For the case where the junction is at 6 volts, either end could be the high or low sender. The decision is made at each end by each circuit examining its own output to decide whether it or the other end is sending a particular level. If the sending end is at 0, the noninverting input sees 6 volts. The receiving end is outputting 12 volts, and the network outputs 9 volts to the inverting input. The comparator sees a difference of −3 volts and outputs low in recognition of the low level at the sending end. If the sending end is at +12, the noninverting input sees 6 volts. The receiving end is outputting 0 volts, and the network outputs 3 volts to the inverting input. The comparator sees a difference of +3 volts and outputs high in recognition of the high level at the sending end.

Table 6-37 summarizes the effects of the various signals.

Table 6-37 Keyboard Receiver Signals

Sending End	Receiving End	Noninverted Input (Junction)	Inverted Input	Difference	Output
0	0	0	3	−3	0
0	12	6	9	−3	0
12	0	6	3	+3	5
12	12	12	9	+3	5

Keyboard Cable Compensation
C7 compensates the circuit for the capacitance of the cable. If C7 were not present, the output of the comparator would glitch when the output driver on the same end of the line changed state. This would be caused by the output signal propagating immediately to the inverting input of the comparator but being delayed (by the RC time constant of the line) to the noninverting input. C7 is chosen so that the time constant of the line is the same at both inputs. Because the resistance seen at the middle of the line is approximately 1000 ohms (two 2 kilohm resistors in parallel) and the resistance seen at the inverting input is approximately 5000 ohms (one 10 kilohm and two 20 kilohm resistors in parallel), C7 is about one-fifth of the cable capacitance. The value is not critical because the ratio of the two time constants can be as large as two and still provide acceptable noise immunity.

6.10.6.3 Terminal Data Encoding – The keyboard requires a clock for its operation and is provided with one by the terminal controller side of the interface. To transmit a clock independently of data on the same wire, the terminal side of the interface generates a clock signal within which data is encoded as a pulse width modulation. The terminal circuit produces a 75 percent high pulse width output for the mark state. Data transmission causes the clock output to switch between 75 and 25 percent pulse width (duty cycle).

Figure 6-59 is a timing diagram that illustrates the formation of the pulse width modulation. Three nand gates, I, II, and III, combine three signals, data, LBA 3, and inverted (not) LBA 4. The three gate outputs are wire-ANDed so that all three must have high outputs to produce a high to the out inverter, which drives the terminal's end of the bidirectional interface. The timing is not precisely correct in this drawing because the LBA signals, addresses to the line buffer in the video processor, are not pure squarewaves and have variations in their periods (see Paragraph 6.5.12.1). These variations give the keyboard signal the appearance of clustering in groups of four, but they do not affect the operation of the circuit.

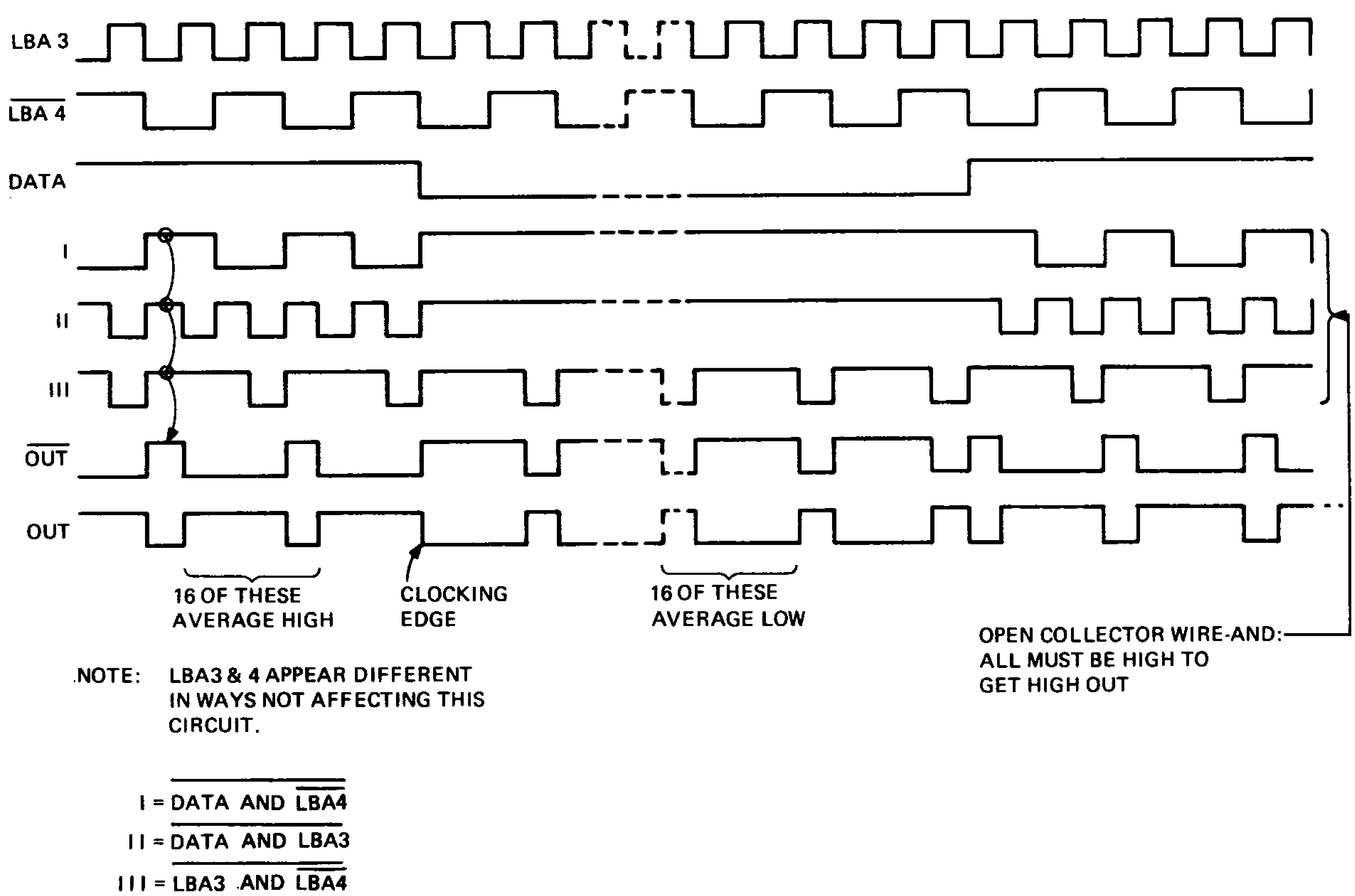


Figure 6-59 Encoding of Terminal Data and Clock

The negative transition of each output pulse occurs at the clock interval regardless of the presence of data. This transition is therefore the reference point for the keyboard clock at the receiving end.

6.10.6.4 Combined Interface Signal – Figure 6-60 illustrates the four possible conditions on the interface line when the effect of the clock is included. Figure 6-61 shows all four states and the transitions between each of them. Two series sensing resistors in the interface circuit divide the signal in half at the wire. Therefore, although the drivers swing 12 volts at each end, the figures show only 6 volt variations.

6.10.6.5 Decoding of Data from Terminal – The keyboard recovers the modulated clock signal sent by the terminal but must also separate the data from the clock. The signal is sent directly to the UART and address counter circuits as a clock. The negative edge of the clock occurs at a fixed interval while the positive edge varies according to the duty cycle modulation. The keyboard circuits use the negative edge and ignore the variable pulse width.

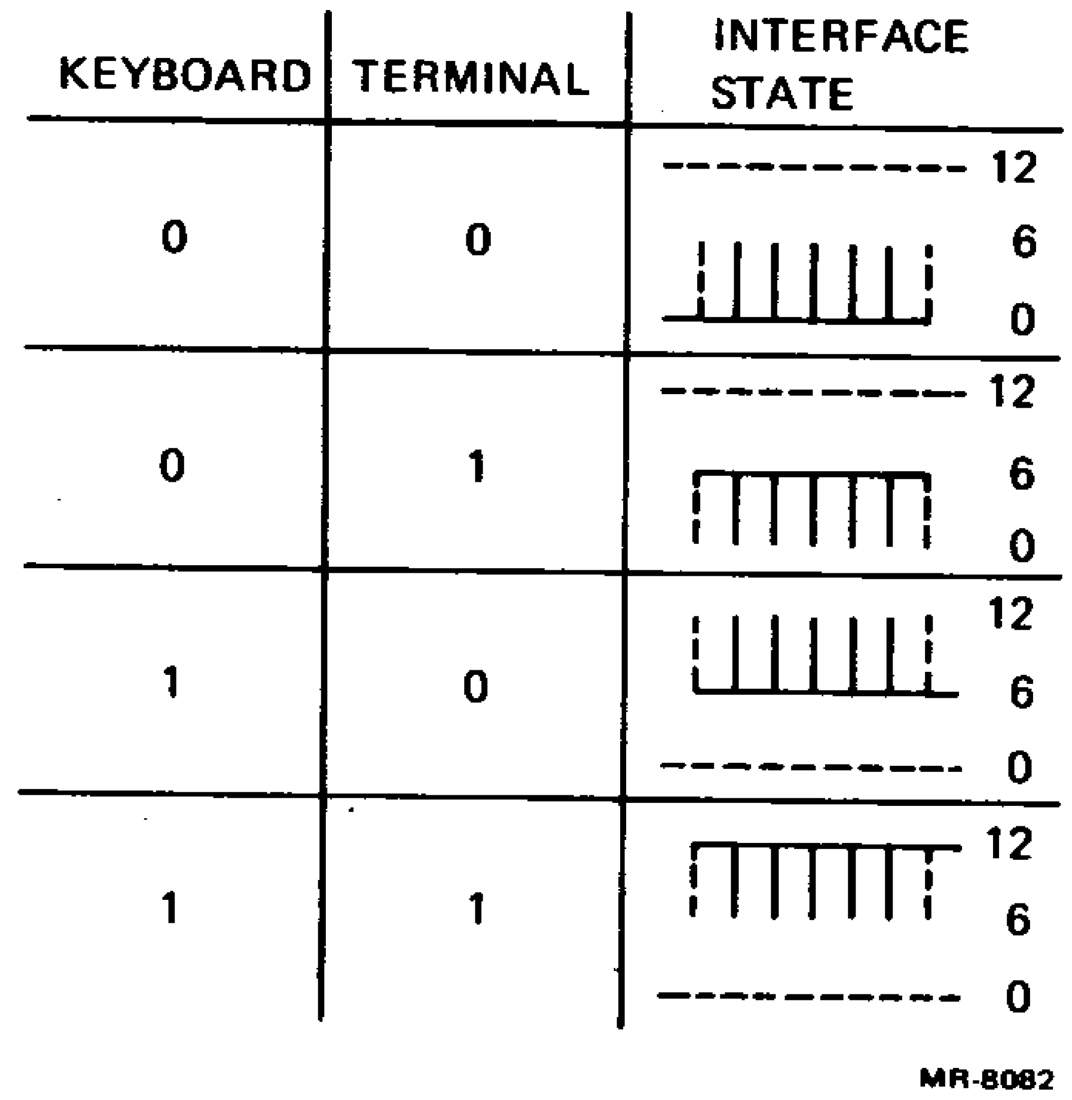


Figure 6-60 Four Keyboard Interface States

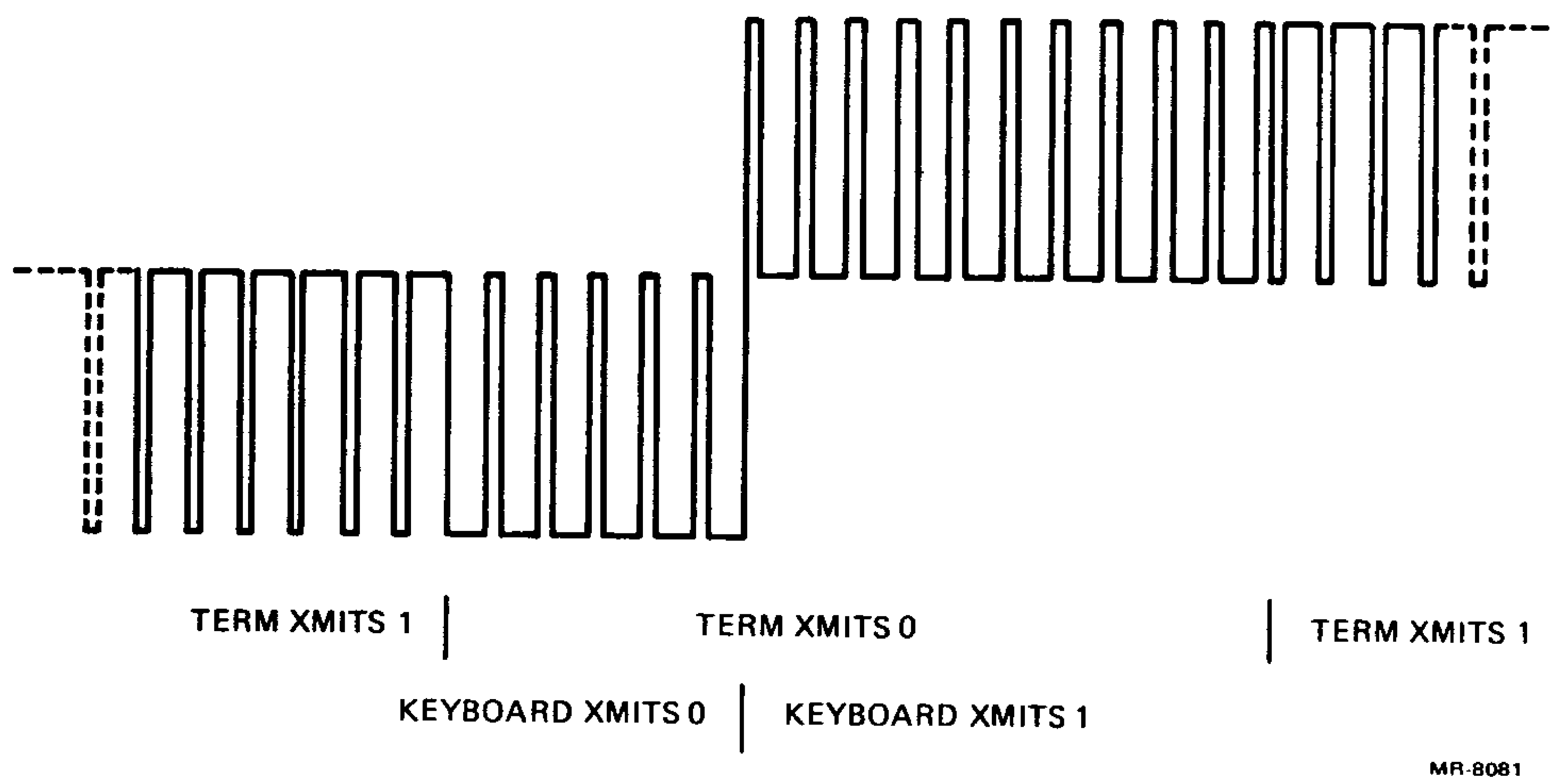


Figure 6-61 Keyboard Interface Signal

Data is extracted from the combined clock-data by a simple resistor-capacitor filter on one input to a comparator. The other comparator input is referred to one-half the power supply. Because the duty cycle of incoming data is either ¼ or ¾, the capacitor charges to that proportion of the supply voltage over the 16 clock periods of each bit. The comparator switches when the capacitor voltage rises or falls past the reference value. The short duty cycle of zeros averages to a low voltage that holds the comparator output low. The long duty cycle of ones averages to a high voltage and switches the comparator to a high state. The comparator output goes to the serial data input of the UART where it is deserialized. When all ten bits of a transmitted character are loaded into the UART, it asserts data available. This signal enables the bell and scan start if the appropriate bits were set in the byte. The LED bits remain latched at the parallel output of the UART until the next command byte arrives.

6.10.6.6 Keyboard Output – The keyboard UART serial output goes directly to an open collector driver that swings its end of the bidirectional signal line between 0 and +12 volts. This is shown as E8 and R15 in Figure 6-58. The circuit is identical at both ends of the interface.

6.10.7 Bell

The keyclick/bell circuit provides audio feedback and attention signals for the user. A bit in the keyboard status word controls the bell. Refer to Figure 6-62 for the circuit. Capacitor C8 charges to +5 volts through resistor R16. The speaker connects between the capacitor and the collectors of the transistors in E1. When a single status word contains the bell bit, flip-flop E3 toggles and turns on E1. C8 discharges through the speaker and E1, generating a click. When the voltage on C8 falls low enough, it clears E3. E1 turns off and C8 charges up for the next click. The value of C8 is selected to determine the volume of the click. D8 protects the transistors from inductive spikes from the speaker.

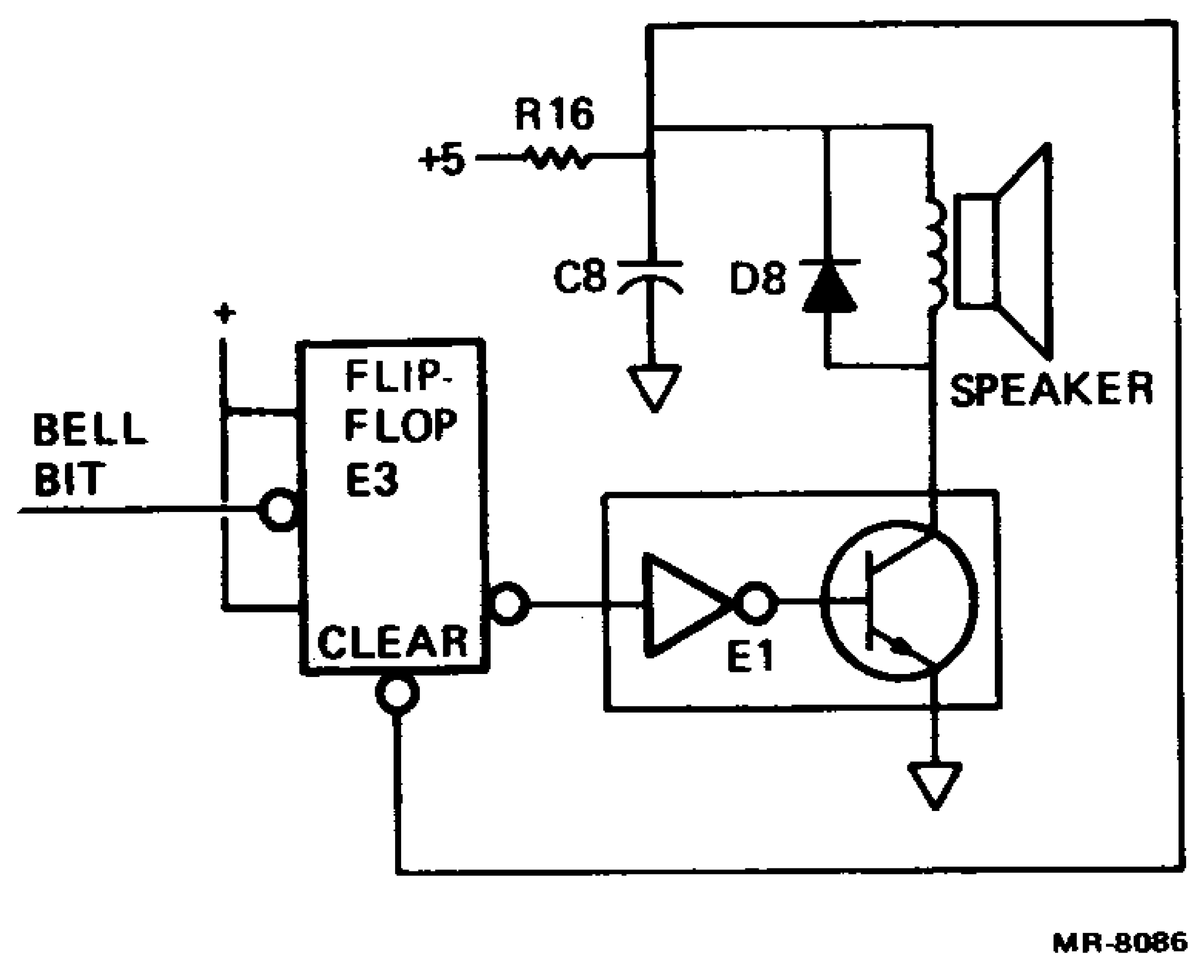


Figure 6-62 Bell Circuit

If the bell bit is set for many words in succession, the UART latch holds the data output constant. A one clock period pulse from the data available flip-flop E6 gates the bell bit through E5 to form a clock to E3. As C8 discharges through the speaker and E1, E3 clears itself, turning E1 off. Then C8 charges up again until the next data available pulse clocks E3 on again to repeat the discharge cycle. C8 discharges fast enough so each data available pulse (which arrives every 1.28 ms) triggers a cycle, allowing the circuit to produce an 800 hertz tone. Bell is generated by setting the bell bit for 0.25 seconds (about 200 status words). Each cycle of the tone is at a reduced amplitude compared with the single keyclick because R16 is selected to limit C8's charging rate. The overall effect of the tone on the ear is that of a beep.

6.10.8 Keyboard Interrupt Routine

When the microprocessor on the terminal controller module responds to an interrupt from the keyboard UART and reads a key address from the UART data output, it immediately range tests the address. The function key addresses are all above the regular key addresses, with set-up the lowest at 7BH and the always closed key at 7FH. An incoming function key address causes a bit to be set in a flag byte called keys (Figure 6-63).

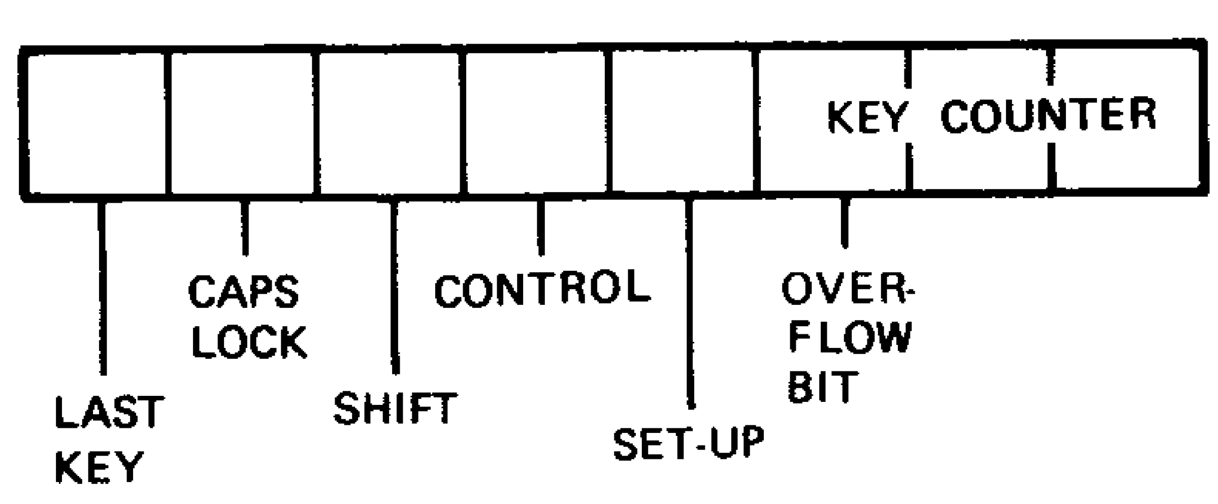


Figure 6-63 Keys Flag Byte

When a key address below the function range arrives, the microprocessor checks the low three bits in keys for the key count. If the count is less than three, the key address is stored in a three place new key address buffer and the counter is incremented. If the count is already three, the counter is incremented but the key address is discarded.

6.10.9 Logical Keyboard Processor

The logical keyboard processor is that portion of the operating firmware that manages the interpretation and transmission of keyboard data. It consists of several processes.

6.10.9.1 Key Recognition – For a key to be recognized as a new key, it must not have been down in the scan before entry is accepted. The microprocessor checks each key's history at each scan. If a key was down during the last scan, it is old and is not entered. Only new keys, those not previously seen, are entered. This system allows a key to be held down without being continuously entered at each scan. (This process and auto repeat are discussed later.)

If a key is detected as down for the first time in a while, the microprocessor assumes that it has been pressed. During the scan when the key is first down, the contacts may bounce for several milliseconds. The time window when the contact is scanned is very short. If the contact happens to be bouncing open during that interval, it is not detected in that scan but the time between scans is long so it is finished bouncing by the next scan and is detected normally. If the contact happens to be closed for the first scan while still bouncing, it is detected. It is also detected on the next scan after it has stopping bouncing but now it is an old key and is not reentered.

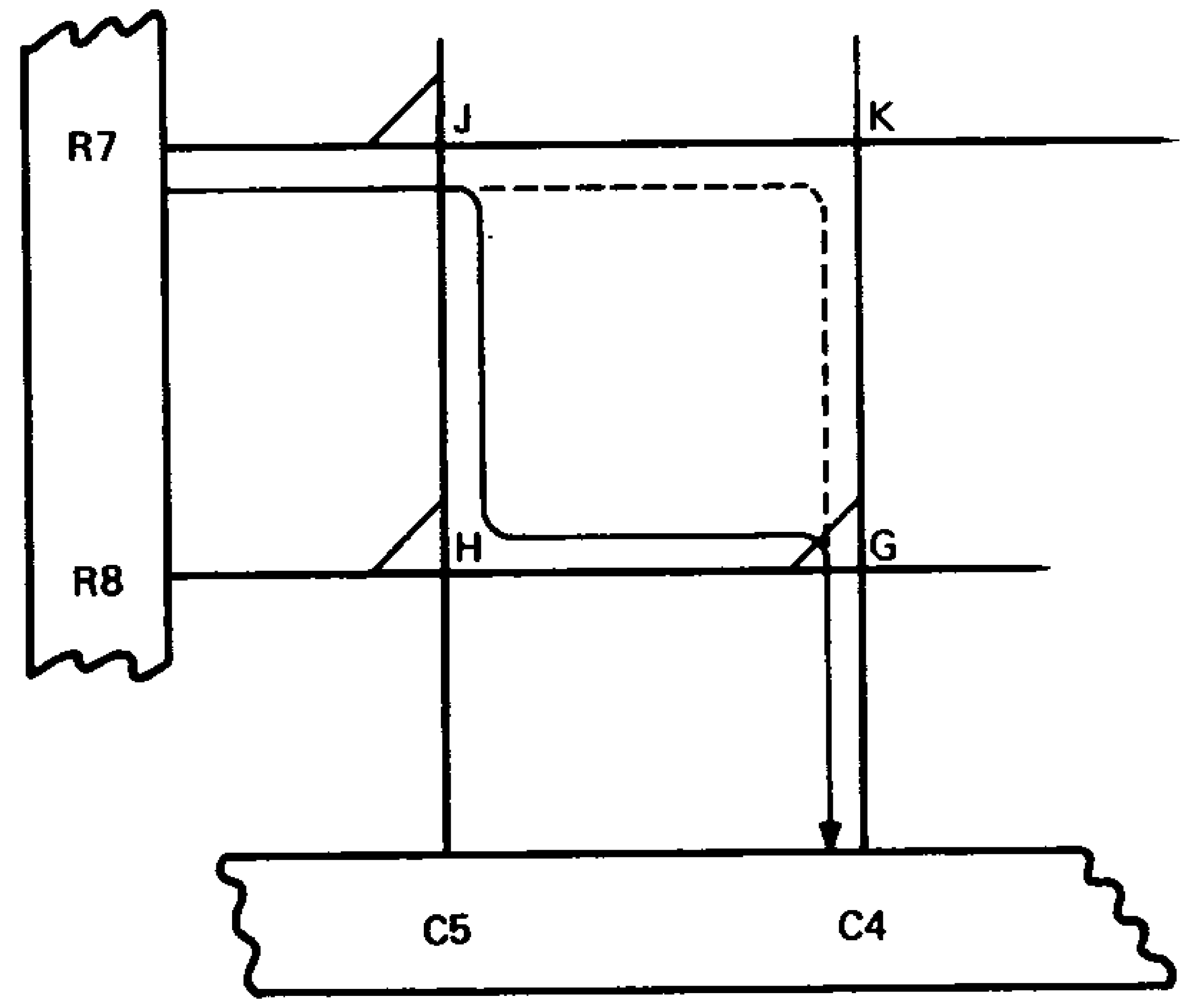
When the microprocessor is free to perform its background routines, it processes the results of the last keyboard scan. First it checks the high bit of the key's byte to see if the scan is finished. If it is not, the microprocessor continues with other work (exits). If it is , the microprocessor checks the key counter overflow bit representing four or more keys sent in the scan. If the bit is set, the microprocessor clears the new key address buffer and exits.

If the overflow bit is not set, the first key is taken from the new key address buffer and tested. If it is either the SET-UP or NO SCROLL key, the microprocessor acts on it immediately and branches to the appropriate routine. It then returns to the keyboard process.

Another three place buffer contains the keys from the last scan. The microprocessor compares the three new keys with those in the old key buffer. If an old key is not in the new key address buffer, that key is cleared from the old key buffer. New keys then go into the old key buffer. Each key address is only seven bits long, so the high bit in each key entry is used to indicate how long that entry has been in the buffer. If a key is new, the bit is set to 0. This means that the microprocessor has only seen the key once. If the key appears in the new key address buffer on the next scan, the microprocessor sets the high bit to 1, converts the key address to an ASCII code, and sends it to the keycode buffer. Only one key is converted and sent in each cycle of the logical keyboard processor routine. Since the set bit indicates that the key has been sent, in the next cycle that key will be ignored and the next key will be processed.

6.10.9.2 Key Rollover – Key rollover means that more than one key can be down at the same time and be accepted. Normally the VT100 accepts three-key rollover. If the keys were pressed during different keyboard scans, they will be accepted in the order in which they were pressed. If they were all pressed during the same keyboard scan, they will be accepted in the order of their addresses.

Certain conditions will limit the rollover to only two keys. The 2.5 key rollover specification reflects the presence of these conditions. Because there are no isolating diodes in the switch matrix, certain patterns of contact closure can produce false key down indications. Specifically, three switches closed in three corners of a rectangular pattern, as in Figure 6-64, will cause a fourth apparent key address to be sent to the terminal. (Refer back to Figure 6-56 to see how the pattern fits into the row-column configuration.) For this reason, although any number of key addresses may be sent by the keyboard during a scan, no more than three may be sent if any are to be accepted. If four or more appear, the terminal ignores all of them and waits for a scan with only three. The special function keys (SHIFT, CAPS LOCK, CONTROL, SET-UP) are in a part of the matrix where there is no pattern sensitivity and no ambiguity. They all are accepted in the same scan with the regular keys and are not counted in the three-key maximum.



SCANNING ORDER	OUTPUT
COLUMN 5-ROW 7	J
C5-R8	H
C4-R7 (C4 SEES C5–R7	K (FALSE 4TH KEY)
THROUGH G, H)	G
C4-R8	

MR-8077

Figure 6-64 Sneak Path

The sneak path problem is also the reason that the keyboard processor looks for the appearance of a key in two successive scans. In Figure 6-64, the keys are scanned in the order J, H, K, G. Normally, the keyboard processor counts the number of keys in a scan and ignores all of them if the count is over three, as it is in this case. But it is possible for a user to briefly press keys J, H, and G and then release G before the scan is completed. Then the keyboard processor might see J, H, the false key K, and, because G was lifted just before it was scanned, register only three keys. One key would be false, but with a count of only three, all would be accepted. To prevent this, the keyboard processor looks for the same keys two scans in a row. Because the G key is released, the K key does not appear in the second scan, and only J and H appear and are accepted by the keyboard processor.

6.10.9.3 Generation of Codes – Because the keys are essentially randomly ordered with respect to the ASCII standard, the program ROM includes several look-up tables that assist in the generation of ASCII codes. Most keys convert directly from an address to an ASCII code. The codes for alphabetic keys with SHIFT or CAPS LOCK down are formed from the tables with bit 5 forced to 0 to produce uppercase alphabetic codes. Holding down the control key when another key is pressed causes another table look-up.

If the key is in the table of valid control codes, that keycode is changed by forcing bits 5 and 6 to 0. For example, the ASCII code for the letter g is 67H. Holding down the control key and typing G transmits the ASCII code 07H.

	B7	B6	B5	B4	B3	B2	B1	B0
Normal code	x	1	1	0	0	1	1	1
Control code	x	0	0	0	0	1	1	1
Shift code	x	1	0	0	0	1	1	1

Nonalphabetic keys have a second look-up table that provides the shifted code given the unshifted code. CAPS LOCK performs the shift function only on alphabetic codes, leaving the nonalphabetics to be performed with an extra shifting action. If a key that does not make a standard control code is pressed with CTRL, it is not sent.

6.10.9.4 Keyboard Transmit Buffer – Some keys generate three byte ASCII codes. For example, when the auxiliary keypad is in alternate mode, it transmits escape sequences that a system can be programmed to interpret in a special way. Cursor control keys also send escape sequences that the operator can use to control the cursor position. To store the codes that might be generated by three simultaneous keys, a 9-byte buffer is provided for the communications port. If the buffer fills up, the keyboard is locked and the appropriate LED lights. When a key is about to be converted to ASCII and stored in the buffer, the microprocessor checks the buffer to see if there is room. Since any key might produce three bytes of code, the microprocessor must be sure that there are at least three places available in the buffer. If six 1-byte keys have been sent, the next 1-byte key leaves only two places. Therefore, the keyboard locks with only seven places filled in the buffer.

6.10.9.5 Auto Repeat – If only one key is in the old key buffer (in the logical processor) and if it appears continuously, it may be a candidate for auto-repeating. A key with control cannot repeat, and a nonrepeat table contains a few keys that do not repeat. These are SET-UP, NO SCROLL, ESCAPE, RETURN, BREAK, and ENTER.

A countdown timer gets loaded with a value each time the buffer changes. When there is no change for a while, the timer decrements to zero. This takes about one-half a second. Then the key is sent to the keyboard buffer a second time and the timer is loaded with a smaller value. This time the count lasts about one thirtieth of a second. The key is sent and the timer reset the same way until the key is lifted or another key is pressed while the first is still down. If the second key is lifted, the count continues at the fast rate. The timer is decremented every time a status byte is sent to the keyboard (every 1.27 ms).

CHAPTER 7
SERVICE INFORMATION

7.1 INTRODUCTION
This chapter provides information needed by the Field Service engineer or customer to configure, test, troubleshoot, adjust, and repair the VT180 terminal. Internal ROM-based self-tests and the tests provided by the diagnostic diskette are described. Information about configuring the terminal controller modules, the AVO, and the VT18X control module is also provided.

Troubleshooting is described both for those situations where a failure is indicated by a diagnostic error message or LED error code and those situations where the system has failed to a level where it is unable to run the diagnostics.

7.2 TESTING THE VT180 USING ROM DIAGNOSTICS
The VT180 has internal ROM-based self-tests that help isolate failures to a field replaceable unit (FRU). These self-tests indicate failures by LED error codes and error characters or error messages displayed on the screen. Corrective action may then be taken as directed by the error indication.

The VT180 has the following self-tests.

1. Power-up test
2. CPU test
3. Dynamic RAM test
4. Communications UART test
5. Disk drive controller/disk drive test
6. Set-up display test
7. Video adjust pattern keyboard test

Each test prints an error message or code that helps isolate a failure to the defective module.

7.2.1 Error Messages and Codes
A self-test stops automatically when it encounters an error. The screen displays an error message or a random pattern of characters. An error condition may also light the LEDs on the keyboard (L1–L4) or on the VT18X control module. If the test is set to run continuously and one or more errors occur, the video screen may change from white to black and back to white about once every second. To clear this condition, press the SET-UP key and then the 0 key (reset).

Table 7-1 shows the error message characters that may appear on the screen and the FRU that should be checked or replaced.

Table 7-1 VT180 Displayed Error Messages

Error Message or Character Displayed	Check or Replace: VT18X Control Module	Terminal Controller	Advanced Video	Keyboard	Disk Unit	Diskette Media
ROM FAILURE	X					
CPU FAILURE	X					
RAM FAILURE						
8K bytes to 64K bytes	X					
0K bytes to 8K bytes	X					
RTC	X					
TERMINAL-PRINTER	X					
CONSOLE	X					
COMM PORT	X					
FLOPPY ERROR, INTERNAL REGISTER	X					
FLOPPY ERROR, RESTORE FAILURE, DRIVE [n]	X				X	
FLOPPY ERROR, STEP FAILURE, DRIVE [n]	X				X	
FLOPPY ERROR, INDEX PULSE FAILURE, DRIVE [n]					X (no diskette)	
FLOPPY ERROR, MOTOR SPEED FAILURE, DRIVE [n]	X				X	
FLOPPY ERROR, SEEK FAILURE, DRIVE [n]	X				X	X (unfor-matted)
FLOPPY ERROR, READ SECTOR FAILURE, DRIVE [n]	X				X	X
ROM DISK LOADER FAILURE OR DISKETTE BOOT FAILURE					X (no diskette loaded)	
1			X			
2		X(NVM)*				
3		X	X			
4				X		
5			X	X		
6		X		X		
7		X	X	X		
8		X				

n = Drive number: A, B, C, or D
*If you have replaced ROM, enter set-up and perform a save operation.

Table 7-1 VT180 Displayed Error Messages (Cont)

Error Message or Character Displayed		Check or Replace				
	VT18X Control Module	Terminal Controller	Advanced Video	Keyboard	Disk Unit	Diskette Media
9		X	X			
:		X				
;		X	X			
>		X		X		
=		X	X	X		
<		X		X		
?		X	X	X		
@		X				
A		X	X			
B		X				
C		X	X			
D		X		X		
E		X	X	X		
F		X		X		
G		X	X	X		
H		X				
I		X	X			
J		X				
K		X	X			
L		X		X		
M		X	X	X		
N		X		X		
O		X	X	X		

n = Drive number: A, B, C, or D
*If you have replaced ROM, enter set-up and perform a save operation.

7.2.2 Power-Up Test
The terminal automatically performs the following tests during power-up.

1. It writes a 1 and a 0 (in turn) in each bit location of RAM on the basic terminal controller module to verify that the RAM can store each bit.

2. It writes a 1 and a 0 (in turn) in each bit location of RAM on the advanced video option (AVO) to verify that the option RAM can store each bit. If the AVO is not present, the test does not check this part of the terminal.

3. It reads the contents of the nonvolatile RAM (NVR), computes a checksum, and then compares the checksum to the checksum stored in the NVR.

4. It reads the contents of each ROM chip, computes a checksum, and then compares the checksum to the checksum stored in each ROM chip.

5. It turns on all keyboard LEDs, rings the keyboard bell, and looks for the end-of-scan character from the keyboard to determine if the keyboard is functional.

CAUTION
Before turning the power to the disk drives on or off, remove all diskettes.

Performing the Test
Any one of the following methods will start the power-up test. The terminal must be in ANSI mode. Check the SET-UP B features to see if you are in ANSI mode. To save the set-up features, press the shift and S key together (a shifted S).

1. Turn the terminal power on.

2. Press the SET-UP key and then the 0 (reset) key.

3. Press SET-UP and 4, placing the VT180 in local mode. Type the following sequence to perform the power-up test once.

   <ESC>[2;1y

4. Place the terminal in local mode. Type the following sequence to perform the test continuously.

   <ESC>[2;9y

NOTE
The continuously running test stops if an error is found or if power is turned off.

Any error found by the power-up test is printed on the video screen. Table 7-2 explains the error messages and codes displayed by either VT18X control module LEDs or keyboard LEDs.

Table 7-2 LED Error Codes

Keyboard LEDs				Error Detected	Field Replaceable Unit			
					Terminal Controller	VT18X Control Module	Disk Unit	Diskette Media
L1	L2	L3	L4					
O	O	O	X	ROM 1	X			
O	O	X	O	ROM 2	X			
O	O	X	X	ROM 3	X			
O	X	O	O	ROM 4	X			
O	X	O	X	Main data RAM	X			

X = On; O = Off

Table 7-2 LED Error Codes (Cont)

VT18X Control Module LEDs 4	3	2	1	Error Detected	Field Replaceable Unit: Terminal Controller	VT18X Control Module	Disk Unit	Diskette Media
X	X	X	X	ROM FAILURE		X		
X	X	X	O	CPU FAILURE		X		
X	X	O	X	RAM FAILURE 8K byte to 64K byte			X	
X	X	O	O	RAM FAILURE 0K byte to 8K byte			X	
X	O	X	X	RTC		X		
X	O	X	O	TERMINAL-PRINTER		X		
X	O	O	X	CONSOLE		X		
X	O	O	O	COMM PORT		X		
O	X	X	X	FLOPPY ERROR, INTERNAL REGISTER		X		
O	X	X	O	FLOPPY ERROR, RESTORE FAILURE, DRIVE n		X	X	
O	X	O	X	FLOPPY ERROR, STEP FAILURE, DRIVE n		X	X	
O	X	O	O	FLOPPY ERROR, INDEX PULSE FAILURE, DRIVE n; MOTOR SPEED FAILURE, DRIVE n		X	X (no diskette in drive)	
O	O	X	X	FLOPPY ERROR, SEEK FAILURE, DRIVE n		X	X	X (unformatted diskette)
O	O	X	O	FLOPPY ERROR, READ SECTOR FAILURE, DRIVE n		X	X	X
O	O	O	X	ROM DISK LOADER FAILURE OR DISKETTE BOOT FAILURE			X (no diskette in drive)	
O	O	O	O	TEST PASSED				

X = On; O = Off

7.2.3 Keyboard Tests

The power-up test checks if a keyboard is present. A key may be tested by placing the terminal off-line and enabling keyclick. All keys typed should produce a click except NO SCROLL, CAPS LOCK, SHIFT, BREAK, and CTRL. Typing the keys should cause the corresponding characters to be displayed on the screen.

Typing <CTRL>G should cause the bell to sound. This checks both the bell circuitry and the CTRL key. Keys typed with CAPS LOCK and SHIFT verify the operation of those keys. After enabling XON/XOFF and placing the terminal on-line, the BREAK and NO SCROLL keys should produce a click when typed.

7.2.4 CPU, Dynamic RAM, Communication UART, and Disk Drive Controller Tests

These tests are run automatically when the system is turned on or optionally when the terminal is reset. These tests check the VT18X control module — its ROMs, CPU, RAMs, PUSARTs, and disk drive controller circuitry. The power-up test assumes that there are no diskettes loaded in the disk drives.

If these tests run successfully, the following menu message is printed on the video terminal.

VT180-XX Version n.n
Copyright 1982 Digital Equipment Corporation
PRESS A, B, C, D, S, or T

A = Start System (drive A)
B = Start System (drive B)
C = Start System (drive C)
D = Start System (drive D)
S = Execute Self-Test
T = Enter Terminal Mode

If an error occurs during any of these tests, a message is printed on the video terminal. See Table 7-1 for a list of error messages.

7.2.5 Set-Up Screen Test

In set-up the terminal exercises all of its display functions. The functions available in the VT180 include double-height, double-width characters (shown as SET-UP A); double-width, single-height characters (shown as TO EXIT PRESS "SET-UP"); and the reverse or underline attribute (selected by the cursor setting and displayed by the cursor and the tab ruler).

In addition to the basic VT180 functions, the functions available in the VT180 with advanced video option include 24 lines with 132 columns (test with the video adjust pattern, Paragraph 7.2.6), and more character attributes.

The following set-up features can be checked with the keyboard controls.

1. Intensity (up and down arrow keys)
2. 80/132 column
3. Tab setting and clearing
4. Transmit and receive speeds
5. Reset
6. Smooth/jump scroll
7. Auto-repeat
8. Reverse screen
9. Margin bell

10. Keyclick
11. United States/United Kingdom character set
12. Wraparound
13. On-line/off-line control

To perform the test, enter the two set-up displays and check that the details agree with those that follow.

SET-UP A is shown in Figure 2-9. The bottom ruler on the display shows the position of the tab stops that are set in the terminal.

SET-UP B, shown in Figure 2-10, displays the current setting for the terminal's features. Figure 2-12 is a summary of features found in SET-UP B.

CP/M application software requires that certain SET-UP B features be set to one mode rather than the other. The remaining features can be set according to the user's preference. The required feature settings are listed in Table 7-3.

Table 7-3 Required Settings for Features

Feature	Required Setting
ANSI/VT52	1 (ANSI) (see note below)
Auto XON/XOFF	1 (on) (must be left on)
Wraparound	0 (off)
New line	0 (off)
Power	0 or 1 (60 Hz or 50 Hz)

NOTE

You can use VT52 mode in the VT180, but you should not save the VT52 features. Upon power-up, the VT18X control module interrogates the terminal controller module to find its parameters. This is done using an ANSI control sequence.

To test the advanced video option, check that the words SET-UP A change from normal to reverse video in boldface, the words TO EXIT PRESS "SET-UP" are underlined, and the tab ruler has alternating normal and reverse video, even if the cursor selected is an underline.

7.2.6 Video Adjust Test

The video adjust test provides a screen full of Es for the display height, width, and linearity adjustments. The test pattern is internal to the terminal and is not sent to the host computer.

Performing the Test

Use the following procedure to display the test pattern.

1. Place the terminal in ANSI mode.
2. Place the terminal in local mode.
3. Type <ESC>#8 to display the pattern.
4. Check smooth scrolling by typing <LF>.

7.3 MODULE CONFIGURATIONS

This section describes the information needed to configure the jumpers and switches on the terminal controller module, the VT18X control module, and the advanced video option (AVO) for use in the VT180 terminal.

7.3.1 VT18X Control Module Configuration

The VT18X control module contains 14 jumpers and a 20-pin DIP switchpack (E22) that allows the user to select various operating features. The switchpack and jumper locations are shown in Figure 7-1. The communication switches configuration is described in Table 3-2 and the jumper configuration in Table 7-4.

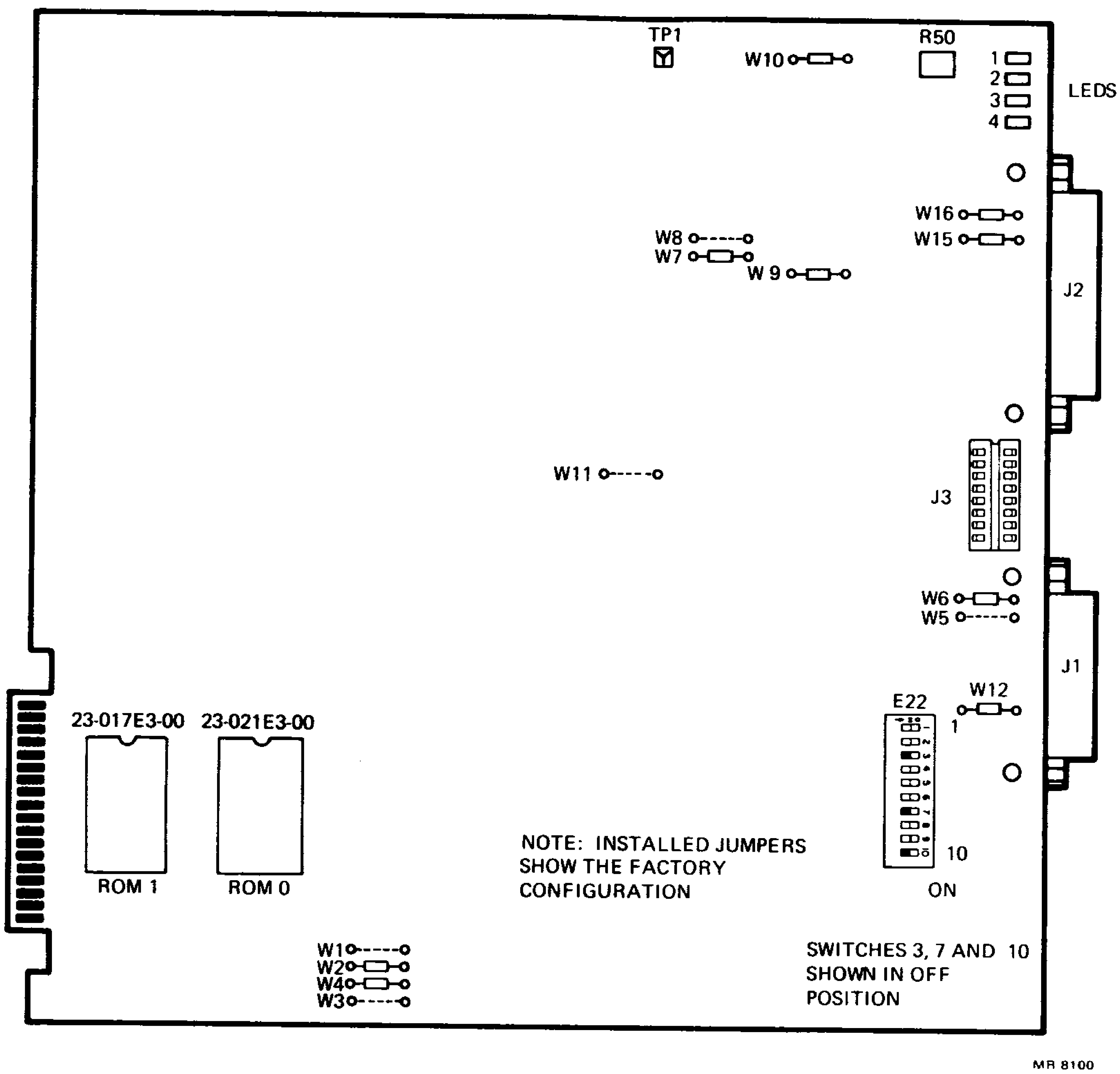


Figure 7-1 VT18X Control Module Jumpers, Switches, LEDs and ROM Locations

Table 7-4 CP/M Processor Factory Jumper Configuration

Jumper	Jumper State	Function
W1	Out	Connects +5 to pin 21 of 2716 ROM 1 (2K × 8).
W2	In	Connects address bit All to pin 21 of 2732 ROM 1 (4K × 8).
W3	Out	Connects +5 to pin 21 of 2716 ROM 0 (2K × 8).
W2	In	Connects address bit All to pin 21 of 2732 ROM 0 (4K × 8).
W5	Out	When installed, disk drive supplies ready (DREADY L) signal.
W6	In	Asserts DREADY L all the time.
W7	In	Selects double-density operation.
W8	Out	Selects single-density operation.
W9	In	Turns on the disk drive motor.
W10	In	Selects double-density data separator. When out, selects single-density data separator.
W11	Out	Installed only during manufacturing testing.
W15	In	Installed for normal operation, removed for FCC testing.
W16	In	Installed for normal operation, removed for FCC testing.

7.3.2 Terminal Controller Module ROMs

The four ROMs used on the terminal controller module for the VT100 are the same as those required for the VT180. Figure 3-6 shows the Digital part numbers of the ROMs and their location on the module.

7.3.3 Advanced Video Option Configuration

Except for a VT180 with a word processing option installed, the VT180 uses no ROMs or jumpers on the advanced video option. A terminal with a word processing option (VT100-WA, -WB) has one ROM installed in the ROM A position on the advanced video option. The configuration of the advanced video option when used for word processing is described in Paragraph 3.4.13.

7.4 DISKETTE DIAGNOSTICS

The VT18X diskette resident diagnostics check the VT18X control module more thoroughly than the self-tests provided by the ROM-based diagnostics. The diskette resident diagnostics have two tests that chain individual diagnostics so that they may be run more easily by end users. The individual diagnostics are intended mainly for field service use.

7.4.1 Diagnostic Operation

When the diagnostic diskette is booted from the Main System menu, it displays the following head and menu.

Diskette Diagnostic Menu

VT180 DISKETTE DIAGNOSTICS VERSION 1.0
DIGITAL EQUIPMENT CORP. 12-31-81

Select one of the following:

1 Basic Test
2 Extended Test
3 Individual Tests

Type <E> to exit to Main System Menu.

CAUTION

If version 2.1 appears on your Main System menu, the disk drive motors will run continuously as long as the menu appears on the screen, allowing you to boot a diskette from any disk drive. If you intend to leave your terminal on for an extended length of time, overnight for example, press T to enter terminal mode. The disk drive motors will then shut off automatically and extend their life.

The user diagnostics are selected by typing a 1 or a 2. Typing a 3 will display a menu of the individual diagnostics. Typing E causes the ROM-based Main System menu to be displayed.

7.4.1.1 Basic Test Operation – The basic test is a diskette diagnostic that checks the disk drives more thoroughly than the ROM diagnostics. The basic test requires two formatted diskettes to be run. Data on these diskettes is NOT preserved. The procedure for formatting diskettes is described in Paragraph 4.10.3.

When the basic test is selected from the Diskette Diagnostic menu, it enters the following dialog.

1 Basic Test

Number of disk drives? (2 or 4)
<u>2</u>
Remove system disk and install FORMATTED disks in A&B drives.
WARNING: Contents of diskettes will be destroyed.
Type <P> to proceed with test.
Type <E> to Exit to Diskette Diagnostic Menu.
<u>P</u>

During the test, the screen will display the following messages.

FLOPPY DISK DIAGNOSTIC TESTS, rev (1.1)

Drive N selected
End of part M

The N will be the drive currently under test and the M will be a number that increments from one to thirteen.

The test will run until an error is detected or until drives A and B have been tested. If the number of disk drives was four, the message that follows appears when drives A and B complete the test without any errors. The message is displayed only if the number of disk drives selected is four.

Install FORMATTED diskettes in <C and D> drives.

Type <P> to proceed with test.
<u>P</u>

When the testing of all disk drives is complete, the following message is displayed on the CRT.

IMPORTANT: Restore the DIAGNOSTIC System Diskette.

Type <P> to proceed with test.
<u>P</u>

The diagnostic diskette must be placed in drive A before pressing P. The basic test is complete at this point. When P is typed, the Diskette Diagnostic menu is displayed again.

If an error is detected in the basic test, the test halts and an error message is displayed. Refer to Paragraph 7.4.5 and Table 7-5 for information on error messages and their possible causes.

Table 7-5 Diskette Error Messages

Diskette Error Messages	Possible Cause
No index pulse, no diskette, or drive	No diskette, disk drive not connected, door open, I/O cable disconnected
Disk rotation too slow	Bad RX180 disk drive unit
No track 0	VT18X control module bad or A, B,C, or D drive bad
Track register wrong value	VT18X control module bad
Step in error, controller module bad	VT18X control module bad
Direction output low	VT18X control module bad
Direction output high	VT18X control module bad
Step in error,?	Disk drive unit, VT18X control module, or cable bad
Timing wrong for single track move	Disk too fast or too slow, RX180 disk drive
Seek not completed in time (with no verify)	VT18X control module bad

Table 7-5 Diskette Error Messages (Cont)

Diskette Error Messages	Possible Cause
Step error	Disk drive unit, or cable bad
Timing wrong for multitrack move (too fast or too slow)	Disk drive unit bad
No seek error	VT18X control module bad
Seek error (no verify)	VT18X control module bad
Seek error (with verify)	Disk drive unit, using unformatted diskette, or diskette not write-protected
CRC error on header	Diskette or VT18X control module bad
No CRC error on header	Diskette or VT18X control module bad
No CRC error on data,?	VT18X control module bad
CRC error on data,?	Diskette, RX180 disk drive, or VT18X control module bad
Seek not completed in time (with verify)	Diskette bad, RX180 disk drive, using unformatted diskette in disk drive, or VT18X control module bad
Track 0 bit set?	RX180 disk drive or VT18X control module bad
Step out error	VT18X control module bad
Write gate high on write	VT18X control module bad
Write gate low on read	VT18X control module bad
Timing wrong for motor shut off	VT18X control module bad
Motor select bit high	VT18X control module bad
One shot too fast (too slow)	VT18X control module bad
Motor bit high	VT18X control module bad
No record not found	VT18X control module bad
No lost data	VT18X control module bad
Record not found error	Diskette, RX180 disk drive, or VT18X control module bad
Write fault	VT18X control module bad
Write-protected	Tried to format with metal tape on diskette
Bad data	Diskette, RX180 disk drive, or VT18X control module

Table 7-5 Diskette Error Messages(Cont)

Diskette Error Messages	Possible Cause
Ready set	VT18X control module bad
Busy set	Tried to select a nonexistent disk drive
Lost data	VT18X control module bad
RAM Test Error Messages	
Error Message	VT18X control module bad
CPU FAILURE	
RAM FAILURE BIT ?	
RAM FAILURE BIT 0	
RAM FAILURE BIT 1	
RAM FAILURE BIT 2	
RAM FAILURE BIT 3	
RAM FAILURE BIT 4	
RAM FAILURE BIT 5	
RAM FAILURE BIT 6	
RAM FAILURE BIT 7	
ADDRESS FAILURE	
Communications Test Error Messages	
Error Message	VT18X control module bad
INCORRECT VECTOR	
UNSOLICITED INTERRUPT	
RTC FAILURE	
CONSOLE FAILURE	
COMM FAILURE	
PRINTER FAILURE	
GENERAL PURPOSE FAILURE	
PRINTER GENERAL PURPOSE FAILURE	

7.4.1.2 Extended Test Operation – The extended test starts exactly as the basic test does. The only apparent change is the test header. The dialog follows.

2 Extended Test

Number of disk drives? (2 or 4)
2

Remove system disk and install FORMATTED disks in A and B drives.

WARNING: Contents of diskettes will be destroyed.

Type <P> to proceed with test.
Type <E> to Exit to Diskette Diagnostic Menu.
P

During the diskette test, the screen will display the following messages.

FLOPPY DISK DIAGNOSTIC TESTS, rev (1.0)

Drive N selected
End of part M

The N will be the drive currently under test and the M will be a number that increments from one to thirteen.

The test will run until an error is detected or until drives A and B have been tested. If the number of disk drives was four, the following message appears when drives A and B complete the test without any errors. This message is only displayed if the number of disk drives selected was four.

Install FORMATTED diskettes in <C and D> drives.

Type <P> to proceed with test.
P

When testing of all disk drives is complete, a message is displayed on the screen.

IMPORTANT: Restore the Diagnostic System Diskette.

Type <P> to proceed with test.
P

The extended test goes on to test the RAM and communications ports. If these tests run without errors, the Diskette Diagnostic menu is displayed again. If an error is detected in any of the tests, the test halts and displays an error message. Refer to Paragraph 7.4.5 and Table 7-5 for information on error messages.

During the RAM test the following message blinks on the screen.

2 RAM Test

7.4.1.3 Individual Diagnostics – To test a printer or to test a specific communications port, use the individual tests. Select these tests by typing 3 after the diagnostic menu. The following Individual Test menu is displayed on the video screen.

Individual Test Menu

1 Floppy Test
2 RAM Test
3 Basic Comm. Test (No Loop-Back Plug)
4 Comm. Test – Printer Port With Loop-Back Plug
5 Comm. Test – General Purpose Port with Loop-Back Plug
6 Comm. Test – Comm. Port with Loop-Back Plug
7 Printer Confidence Test on General Purpose Port
8 Printer Confidence Test on Printer Port
9 Synchronous Comm. Test

Type <E> to Exit to Diskette Diagnostic Menu.

Type the number of the test desired and follow the instructions printed on the video screen for the specific test. The terminal echos the number of the test selected and prints:

Type <P> to proceed with test.

The following conditions can be used to run the selected test.

1. Type P to run the test once.

2. Type ,nP to run the test n number of times, where n = 1 to 9.

3. Type -P to run the test continuously. To stop a continuously running test, reset the terminal by pressing SET-UP 0. Boot the diagnostic diskette again to get the menu.

When the selected test starts, it displays the test name followed by any required dialog.

NOTES

1. **An external loopback connector (Digital part number 12-15336) must be attached to the terminal to run test 4, 5, or 6. These tests detect failures in the EIA line drivers and receivers, which are not checked on power-up or during self-test. The transmit and receive baud rates for the terminal must be identical.**

2. **The printer confidence tests (7 and 8) send a line of text that you type to the printer. The printer must be set up for these parameters.**

BAUD RATE:1200*
BIT/CHARACTER:8
PARITY:NONE
STOP BITS:1

*A later revision ROM allows the baud rate to be either 300 or 1200. This is established using the P SETUP command. Refer to Chapter 5 to use this command.

3. **The synchronous communications test (test 9) requires that the terminal's transmit and receive speeds be identical and be at 2400 baud or less. The communications port is tested in loopback mode; however, no loopback connector is required for this test. Enter SET-UP B and change the baud rate if you desire to run this test.**

If the test runs without detecting any errors, the following message is displayed each time the test is successful.

TEST PASSED

When the test has run the specified number of times, the Individual Test menu will be displayed again.

7.4.1.4 Individual Test Example Dialog – The following dialog provides a simple example of selecting an individual test and running it with a repeat count of three. The test used in the example is the basic communications test. The example assumes that the system diagnostic diskette has been booted.

Diskette Diagnostic Menu

VT18X DISKETTE DIAGNOSTICS Version 1.0
DIGITAL EQUIPMENT CORP. 12-32-81

Select one of the following:

1 Basic Test
2 Extended Test
3 Individual Tests

Type <E> to exit to Main System Menu.
3

Individual Test Menu

1 Floppy Test
2 RAM Test
3 Basic Comm. Test (No Loop-Back Plug)
4 Comm. Test – Printer Port With Loop-Back Plug
5 Comm. Test – General Purpose Port with Loop-Back Plug
6 Comm. Test – Comm. Port with Loop-Back Plug
7 Printer Confidence Test on General Purpose Port
8 Printer Confidence Test on Printer Port
9 Synchronous Comm. Test

Type <E> to Exit to Diskette Diagnostic Menu.
3

Type <P> to proceed with test.
,3P

3 Basic Comm Test (No Loop-Back Plug)
TEST PASSED
TEST PASSED
TEST PASSED

Individual Test Menu

1 Floppy Test
2 RAM Test
3 Basic Comm. Test (No Loop-Back Plug)
4 Comm. Test – Printer Port With Loop-Back Plug
5 Comm. Test – General Purpose Port with Loop-Back Plug
6 Comm. Test – Comm. Port with Loop-Back Plug
7 Printer Confidence Test on General Purpose Port
8 Printer Confidence Test on Printer Port
9 Synchronous Comm. Test

Type <E> to Exit to Diskette Diagnostic Menu.

This example showed the dialog needed to run the basic communications test with a repeat count of three. It assumed that no errors were detected while running the test.

7.4.2 Floppy Test

The floppy test performs an extensive checkout of the disk drive controller and the selected disk drives. The floppy test is run in both the basic and extended tests. It also may be run individually with a greater number of operator options.

This paragraph explains operation of the floppy disk test when selected individually. It also gives a basic description of what the test does.

7.4.2.1 Floppy Test Operation – When the floppy test is selected from the Individual Test menu, it enters the following dialog.

1 Floppy Test

The screen is cleared and the following dialog is displayed.

FLOPPY DISK DIAGNOSTIC TESTS, rev (x.0)

Select drive(s) to be tested. <A,B,C,D>

Press RETURN to continue
N

The N is the user's response. This response can be any combination of A, B, C, or D repeated any number of times. For example, AABBCCAADD would test drive A twice followed by drives B and C twice each, drive A would then be tested twice again followed by two tests on drive D. The test requires about 4 minutes per drive, so the example would take about 40 minutes.

After the drives are entered and RETURN is pressed, the screen is cleared again and the following dialog is displayed.

FLOPPY DISK DIAGNOSTIC TESTS, rev (x.0)

Insert formatted disks into drives

WARNING, CONTENTS OF DISKS ARE DESTROYED!

Press RETURN to continue

This test requires formatted diskettes for each drive that is to be tested. These diskettes must be in good condition and have no data that must be saved. Any data that is on these diskettes will be destroyed.

When formatted diskettes have been installed in the drives to be tested, press RETURN.

The screen will be cleared again, and the following message will be displayed.

FLOPPY DISK DIAGNOSTIC TESTS, rev (1.0)

Drive N selected
End of part M

The N is the drive currently under test and the M is a number that increments from one to thirteen.

When all of the selected drives have been tested and no errors have been detected, the test exits to the Individual Test menu.

If an error is detected during the diskette test, the test will wait on the error and display an error message. (Refer to Paragraph 7.4.5 and Table 7-5 for more information on error messages.)

7.4.2.2 Floppy Test Description – The floppy test has an initialization section and 13 tests.

The initialization section presents the drive selection dialog and the message to insert formatted diskettes into the selected disk drives. If no selection was made and RETURN was typed, the initialization section selects drive A as a default. It then displays the selected drive.

Test one uses the index pulse from the selected drive to check motor speed over a four second period. There should be 20 index pulses in 4 seconds. If the number of pulses is not 20, the motor speed is either too fast or too slow.

Test two checks the restore command. It issues a restore command to the selected drive and waits 1.5 seconds for a track 0 bit to be set. If the bit does not set, another drive is tested to determine if the problem is in the controller or a drive. The track register is tested to be sure that it has been reset.

Test three checks part of the diagnostic read register and the general control register. The test also checks restore timing and head load timing.

Test four checks the step in command to see that the head moves away from track 0 and that the track register is incremented.

Test five verifies head speed using the restore command. The track register is also checked to ensure that it was reset.

Test six checks head motion and the track register using step in and step out commands.

Test seven checks the proper step command and track register performance.

Test eight puts the head at track 40 and then times a restore command. It also checks the track register.

Test nine does seek testing. First, sequential seeks are done from track 0 to track 40 with no verify. After each seek, the control and status register is tested for seek or CRC errors. When the last track is found, it seeks to tracks 10, 30, 20, 25, 5, 35, and 15 to move the head in a random fashion. The test is then repeated with a verify after each seek.

Test ten checks the controller write logic. Errors are forced to ensure that the proper errors are detected. Forced errors are: record not found, lost data, seek error, and CRC error on the header. During the lost data test, the write gate is tested to be sure it goes low.

Test eleven writes data to tracks 0, 20, 40, 4, 36, 8, 32, 12, 28, 16, and 24. The data is left for the read sector test. If errors are encountered, an appropriate error message is displayed.

Test twelve checks the controller read logic. Errors are forced to ensure that the proper errors are detected. Forced errors are: record not found, lost data, and CRC error on the data field. During the lost data test, the write gate is tested to be sure it stays high.

Test thirteen reads and verifies the data written in test eleven. If an error is detected, an appropriate error message is displayed.

Refer to Paragraph 7.4.5 and Table 7-5 for information on errors.

7.4.3 RAM Test

The RAM test performs an extensive check on the VT18X control module RAM and the refresh circuitry of the Z80 CPU. The RAM test takes from 10 to 12 minutes to complete. It is run as a part of the extended test, although it may be run individually. When the RAM test starts, it displays the following header.

    2 RAM Test

The RAM test has subtests that check the following aspects of RAM performance.

1. Z80 refresh register
2. RAM refresh
3. Addressing
4. Data integrity
5. Code execution
6. Gallop pattern
7. Alpha radiation

There are no operator dialogs needed within the RAM test. The possible error messages from this test follow.

    CPU FAILURE
    ADDRESS FAILURE
    RAM FAILURE BIT 0
    RAM FAILURE BIT 1
    RAM FAILURE BIT 2
    RAM FAILURE BIT 3
    RAM FAILURE BIT 4
    RAM FAILURE BIT 5

RAM FAILURE BIT 6
RAM FAILURE BIT 7
RAM FAILURE BIT ?

The question mark after the last message means that the test could not determine which bit failed.

7.4.4 Communications Tests
The communications tests include:

1. A basic communications test
2. A synchronous communications test
3. A printer confidence test on the general purpose port
4. A printer confidence test on the printer port
5. A loopback plug test on the printer port
6. A loopback plug test on the general purpose port
7. A loopback plug test on the communications port.

The basic communications test runs when the extended test is selected from the Diskette Diagnostic menu. The synchronous communications test, the loopback connector tests, and the printer confidence tests must be selected individually from the Individual Test menu. The basic communications test can also be selected individually from the Individual Test menu.

7.4.4.1 Basic Communications Test – This test checks the operation of all the VT18X control module's PUSARTs in asynchronous mode. The test uses the loopback multiplexer on the control board to loop back the PUSART outputs. The test also checks the real time clock and interrupts.

The basic communications test is run as part of the extended test and can also be run individually.

When the basic communications test is selected from the Individual Test menu, it displays the following header.

3 Basic Comm. Test (No Loop-Back Plug)

7.4.4.2 Synchronous Communications Test – This test checks the operation of the communications port PUSART in synchronous mode.

To run this test, the transmit and receive speeds set in SET-UP B must be 2400 or lower. The speeds must also be equal. This is because the baud rate clock from the terminal controller module is used for the communications port PUSART. The actual transmission frequency is 16 times the frequency selected in SET-UP B. The limitations of the PUSART do not allow higher speeds to be used.

The communications port is operated in loopback mode during the test. Its output is looped back to its input. This is done with the loopback multiplexer on the VT18X control module. The external loopback connector is not used for this test.

When this test is selected from the Individual Test menu, it displays the following message.

9 Synchronous Comm. Test

If the transmit and receive speeds from SET-UP B exceed 2400, the following error message is displayed.

CANNOT RUN TEST BECAUSE SELECTED BAUD RATE
EXCEEDS 2400 BAUD. CHANGE BAUD RATE USING
SETUP IF YOU DESIRE TO RUN THE TEST.

The test then returns to the Individual Test menu.

If the test detects a failure, the following error message is displayed.

COMM FAILURE

7.4.4.3 Loopback Plug Tests – This test is designed to detect failures in the EIA drivers and receivers that were not checked by tests using the loopback multiplexer. The tests use an external loopback connector to loop an individual PUSART's output back to its input through the EIA drivers and receivers.

When a loopback test is selected from the Individual Test menu, one of the following messages is displayed.

4 Comm. Test – Printer Port with Loop-Back Plug
DEPRESS Y WHEN CONNECTOR IS ON

5 Comm. Test – General Purpose Port with Loop-Back Plug
DEPRESS Y WHEN CONNECTOR IS ON

6 Comm. Test – Comm. Port with Loop-Back Plug
DEPRESS Y WHEN CONNECTOR IS ON

The external loopback connector must be connected to the selected port before typing the Y. To connect the loopback connector, the cable access cover must be removed and any cable connected to the selected port must be disconnected. Remember to replace any cables disconnected when the test is complete.

The Y will be echoed on the line following the message.

The error messages possible from these tests follow.

PRINTER FAILURE

GENERAL PURPOSE FAILURE

COMM FAILURE

If there were no failures indicated in self-test, the extended test, or the basic communications test diagnostics, one of these messages indicates a failure in the EIA drivers or receivers.

7.4.4.4 Printer Confidence Tests – These tests are used to send a line of text to a printer or printing terminal connected to the printer port or the general purpose port. They are included as confidence tests for the printer and general purpose ports. They are not intended to be printer tests.

When one of these tests is selected from the Individual Test menu, it displays the following header and message.

7 Printer Confidence Test on General Purpose Port

8 Printer Confidence Test on Printer Port

INPUT ONE LINE OF TEXT FOLLOWED BY AN <ESC>

The text is echoed on the line following the message.

When the test detects an ESC at the end of the text, it starts transmitting the text to the printer. The text can be up to 124 characters, including returns. Each return counts as two characters of the 124.

NOTE

This test always uses the following parameters to transmit data.

BAUD RATE: 1200
BITS/CHARACTER: 8
PARITY: NONE
STOP BITS:

The printer must be set up for these parameters to run this test.

When the <ESC> is detected at the end of the text, the following message is displayed.

Starting Transmission

If the printer confidence tests are selected with a repeat count, the starting transmission message is only output once. The text only has to be entered once.

7.4.5 Diskette-Based Diagnostic Error Messages

When an error has been detected by a diagnostic test, the test will display an error message followed by these messages.

WAITING ON ERROR, TYPE <P> TO PROCEED, <L> TO LOOP
X

The X is the echoed response to the message. If loop is selected as the response to the message, the following message is displayed after 100 loops.

PERCENTAGE OF ERROR ##%

This message is updated each time 100 loops have been done.

If P is typed, testing proceeds from the point at which the error was detected.

Table 7-5 lists the error messages that can be displayed by the diskette-based diagnostics.

7.5 TROUBLESHOOTING

All terminals in the VT180 series are based on the VT100 video terminal, with the VT18X personal office computing option added to the terminal. Therefore, when troubleshooting the VT180, you should attempt to isolate the problem first to the VT100 and then to the VT18X control module or RX180 disk drive unit(s). If a screen display or LED indication is obtained, the troubleshooting procedure generally involves running the ROM-based self-tests to isolate the failure to a FRU and then running the more extensive tests provided by the diskette-based diagnostics.

CAUTION

Before turning the power to the disk drives on or off, remove all diskettes.

7.5.1 Troubleshooting the Basic VT180

The VT180 internal self-tests help isolate failures in the VT180 caused by a field-replaceable unit (FRU). Paragraph 7.2 describes the tests and how to run them. Table 7-1 lists the displayed error messages and Table 7-2 lists the keyboard and VT18X control module LED error codes the tests provide, the failures they indicate, and the FRU that should be replaced.

The ROM-based diagnostics will be complete after approximately 15 seconds, and the following will be displayed on the video screen. (This printout is subject to change.)

VT18X VERSION 2.1 28-JUN-82

COPYRIGHT 1982 DIGITAL EQUIPMENT CORPORATION

PRESS A, B, C, D, S, or T

A = Start System (drive A)
B = Start System (drive B)
C = Start System (drive C)
D = Start System (drive D)

S = Execute Self-Test

T = Enter Terminal Mode

At this time you may insert a diskette into a drive and start the diskette; or you may enter VT100 terminal mode, not using the diskette; or you may start the self-test again.

To boot a diskette, type the letter of the drive that has the diskette installed. For example, to boot a diskette in drive A, type A.

If you want the VT180 to communicate with an external system, type T to enter VT100 terminal mode. If you want to run the internal extended self-test, place the formatted diskettes in drives A and B and type S.

7.5.2 Troubleshooting the VT180 with the Diagnostic Diskette

The diagnostic diskette includes the following programs.

1. CPU test
2. Dynamic RAM test
3. Communications UART test
4. Floppy controller/drive test

The CPU test verifies that the CPU processor on the VT18X control module is operating correctly.

The dynamic RAM test checks the RAMs on the VT18X control module for short or open circuits.

The communications UART test uses various data patterns and baud rates. Data is looped internally from the transmit of one UART to the receive of another.

The floppy controller/drive test checks many of the functions the ROM diagnostic does but is more extensive. These tests include register tests, timing and seek tests, sector read and write tests, and data tests.

7.5.2.1 Starting the Diagnostic Diskette – Turn the system on by pressing the 1/0 switch on the top of the disk drive unit (or upper disk drive unit if there are two) to 1. The following message appears on the terminal.

VT18X Version 2.1

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PRESS A, B, C, D, S, or T

Place the diagnostic diskette into drive A (the left drive of the top disk drive unit) and type A.

7.5.2.2 Diagnostic Error Messages – The diagnostic test will print an error message on the video screen. Upon detection of an error, the diagnostic will wait in error mode and will require you to type either a command to proceed (P) or a command to loop (L) on the error detected. The error message will appear as follows.

ROM DISK LOADER FAILURE

WAITING ON ERROR

If P is typed, the waiting on error message disappears and the diagnostic proceeds to the next test. If L is typed, the waiting on error message disappears and the following message takes its place.

LOOPING ON ERROR

XXX% OF FAILURE

The percent of failure is updated every 100 loops.

7.5.3 Troubleshooting the VT180 with no Printout

If the terminal has a problem and no start-up printout occurs, perform the following procedure.

1. Turn the power off by setting the 1/0 switch on the top (or only) disk drive unit to the off (0) position.

   NOTE
   If two disk drive units are installed, the 1/0 switch on the bottom disk drive unit should always remain set to 1.

2. The 1/0 switch on the back of the video terminal should be set to 1.

3. Check the voltage selector switches on the back of the disk drive unit(s) and the video terminal; they should match the system's power — 115 Vac or 230 Vac (Figure 3-25).

4. Check the ac power cables for correct configuration (Figures 3-26 and 3-27). These cables should be connected as follows.

   a. The wall receptacle to the top (or only) disk drive unit.
   b. The top disk drive unit to the bottom disk drive unit.
   c. The bottom (or only) disk drive unit to the terminal.

5. Check the I/O cable for correct configuration (Figures 3-26 and 3-27).

   a. A BC26K I/O cable connects from the disk drive port on the back of the video terminal to the left connector (as seen from the back) on the bottom (or only) disk drive unit.

   NOTE

   In a system with two disk drive units, the BC26K I/O cable must connect from the terminal to the RX180-AD, the bottom disk drive unit (drives C and D). Drive A of the RX180-AB, the top disk drive unit, has a resistor pack for terminating the I/O bus; therefore, drive A must always be last on the I/O bus.

   b. A BC26Z 20 cm (8 inch) disk-to-disk I/O cable (17-00298) connects the bottom disk drive unit to the left connector (as seen from the back) on the top disk drive unit.

6. Check that the keyboard cord is plugged into the keyboard connector at the back of the terminal.

7. Turn the 1/0 switch on the top (or only) disk drive unit to 1 (on). The system performs its power-up test. (Refer to the power-up test description in Paragraph 7.2.2 for more information about the power-up test.)

Problems that occur with the VT180 can be isolated to the VT100 terminal controller, the keyboard, the monitor, the VT18X control module, the VT180 paddle board, the RX180 disk drive unit(s), or any option added to the VT180.

Table 7-6 lists the more common VT180 failures and the indications linked with these failures. In using the table, select the indication that matches the failure and note the following.

1. Table 7-6 assumes that only one field-replaceable unit (FRU) has failed.
2. Do not ignore the chance of a component failure after the module has been replaced.
3. Turn off power before disconnecting or replacing any of the FRUs.

The indication displayed may represent a multiple failure, and as a result, the indication may change as FRUs are replaced. Always troubleshoot according to the current indication.

Table 7-6 Basic VT180 Troubleshooting Procedure

Indication	Probable Cause	Corrective Action
No response when the power switch is set to the on position. The CRT filament is not lit and 1/0 switches on the disk drive units are not on. The LEDs on the terminal are not on.	Not plugged in; no power at the wall socket.	Plug in the VT180; use a different wall socket if possible.
	Main power fuse.	Replace the fuse. (if the fuse blows again there may be a shorting problem. Use the appropriate troubleshooting methods.)
	Disk drive fuse.	Replace the fuse.

Table 7-6 Basic VT180 Troubleshooting Procedure (Cont)

Indication	Probable Cause	Corrective Action
	Power supply.	Replace the power supply.
	AC line cord.	Check for an open or short and replce the line cord.
The disk drive 1/0 switch light is off. The terminal is on.	The power cable is incorrectly installed.	Check for the correct daisy-chain of power through each disk drive unit to the terminal.
	The disk drive unit or power supply.	Replace the disk drive unit.
On a system with two disk drive units, the bottom left drive select light comes on when power is turned on. The diskette may have read errors.	The two disk drive units are installed in reverse order.	See Chapter 3 for installing two disk drive units.
Disk drive A fails; drive B functions correctly.	EMI static from the video terminal or disk drive failure.	Place the disk drive unit on the side of the terminal and test drive A again. If drive A still fails, replace the entire disk drive unit.
Disk drive B fails; drive A functions correctly.	The disk drive.	Replace the disk drive unit.
The disk drive select LED is on, but the terminal has no power. The CRT filament is not on.	The power cable from the disk drive unit to the terminal is unplugged or the switch is off.	Check for the correct daisy-chain of power through each disk drive unit to the terminal. Check the setting of 1/0 switches on each disk drive unit and on the back of the terminal.
	The power harness is not firmly attached to the expansion backplane.	Check the power harness.
	The dc power harness.	Replace the harness.
	Expansion backplane.	Replace the backplane.
	Terminal power supply.	Replace the terminal power supply.
No audible tone is heard when the terminal is turned on. The keyboard LEDs are lit.	Keyboard.	Replace the keyboard.
	Keyboard cable.	Replace the keyboard cable.
	Terminal controller.	Replace the terminal controller.

Table 7-6 **Basic VT180 Troubleshooting Procedure (Cont)**

Indication	Probable Cause	Corrective Action
	Speaker.	Replace the speaker.
	Keyboard cable.	Replace the keyboard cable.
A flashing 4 appears on the screen, but no audible alarm sounds when the terminal is turned on and no keyboard light comes on.	The keyboard is disconnected.	Connect the keyboard.
	Power cables.	Check the power cables.
	Keyboard cable.	Replace the keyboard cable.
	Keyboard.	Replace the keyboard.
	Terminal controller.	Replace the terminal controller.
An audible tone has sounded on the keyboard ON-LINE light is on, but the start-up message does not appear on the screen 30 seconds after the terminal is powered up.	The screen brightness is too low.	Adjust monitor brightness.
The start-up message appears when the system is powered up or reset, but the diagnostic diskette does not run when the drive is specified. The terminal displays ROM DISK LOADER FAILURE or DISKETTE BOOT FAILURE.	There is no diskette in the specified drive.	Install the diagnostic diskette in drive A.
	The drive door is not closed.	Close the door.
	An unformatted or wrong diskette is installed.	Change the diskette and try again.
The wrong character appears on the screen when typed in local mode.	Set-up features may be set incorrectly.	Enter SET-UP A and press 0 (reset). Then check SET-UP B features. The required feature settings are listed below. **Feature** **Setting** ANSI/VT52 1 AUTO XON XOFF 1 Wraparound 0 New Line 0 Power 0 to 1 (The power matches the power line frequency, 60 Hz or 50 Hz.)
	The ROMs on the terminal controller may need to be changed.	Check the ROM part numbers and replace them if necessary.

Table 7-6 Basic VT180 Troubleshooting Procedure (Cont)

Indication	Probable Cause	Corrective Action
The wrong character appears on the screen when typed in on-line mode. The terminal is functional in local mode.	Set-up features may be set incorrectly.	Enter SET-UP B and then check SET-UP B features.
	Transmit or receive speed.	Set the speed to match the computer.
	Alternate character set or alternate keypad mode or cursor key mode is selected.	Clear the condition with power-up or reset.
	Terminal controller ROMs.	Check and replace the terminal controller ROMs if necessary.
	The bits per character feature is set incorrectly.	Set the feature to match the computer.
	The parity feature is set incorrectly to match the computer.	Set the parity and/or parity sense feature.
	Communications switches on the VT18X control module may be set incorrectly.	Check the settings of the communications switches. (See Chapter 3.)
	Communications facility problem.	Check the communications facility.
A horizontal or vertical line appears on the screen.	Monitor connectors.	Check and reconnect the monitor.
	Monitor board.	Replace the monitor board.
	CRT and yoke	Replace the CRT and yoke assembly.
The screen display is distorted. The characters are narrow on the left or right side of the screen.	The monitor is maladjusted.	Adjust the monitor.
	Monitor board.	Replace the monitor board.
	Flyback transformer.	Replace the flyback transformer.
	CRT and yoke assembly.	Replace the CRT and yoke assembly.
	Terminal controller.	Replace the terminal controller.

Table 7-6 Basic VT180 Troubleshooting Procedure (Cont)

Indication	Probable Cause	Corrective Action
The display bows in or out.	The yoke pincushion is maladjusted.	Replace the CRT and the yoke assembly.
The display is jumpy	The interlace feature is on.	Turn the feature off.
	The power feature is set incorrectly.	Set the feature to the correct line frequency.
	Terminal controller.	Replace the terminal controller.
	Power supply.	Replace the power supply.
	Monitor board.	Replace the monitor board.
	Flyback transformer.	Replace the flyback transformer.
	Keyboard.	Replace the keyboard.
	Controller.	Replace the controller.
The messages received are incomplete.	XON/XOFF feature is set incorrectly.	Set the feature.
	Terminal controller.	Replace the terminal controller.
All characters are displayed as a white area (black with reverse screen).	An alternate character set is selected and not available.	Clear the condition with power-up or reset.
Only the top or bottom half of the characters are displayed on the screen.	Incorrect use of the double-height escape sequence.	Check the escape sequence.
The set-up features do not work correctly (multiple alarms may sound on power-up or recall).	The save operation was not performed.	Perform the save operation.
	Terminal controller	Replace the terminal controller.
The terminal does not respond to the escape sequences.	The ANSI/VT52 feature is set incorrectly.	Set this feature to ANSI.

7.5.4 Troubleshooting the Options

Troubleshoot any terminal option module by removing it and then checking the basic terminal. If the problem occurs when the module is reinstalled, replace the module.

7.6 VIDEO ALIGNMENT

This section describes how to align the video monitor made by Elston. (For early model terminals, refer to the *VT100 Series Pocket Service Guide.*) Each adjustment should be checked because an adjustment may affect others that follow it. However, if a check shows the correct indication, do not perform that adjustment; instead, go on to the next procedure.

All adjustments must be made under the following conditions.

1. Normal video (dark background)
2. 80 characters per line
3. ANSI mode
4. Local mode
5. Not in either set-up mode
6. CRT alignment template attached to the screen
7. Top cover removed
8. When all of these conditions are met, type <ESC>#8 to fill the screen with a test pattern consisting of all Es.

7.6.1 Alignment Template

Figure 7-2 shows the alignment dimensions used in this procedure. If the mylar adjustment templates (94-03220-03 and 94-03270-03) are not available, use the dimensions in Figure 7-2 to help you make a template from a sheet of paper. Paragraph 7.6.1.1 describes this procedure. A correctly made paper template serves the purpose of the mylar template.

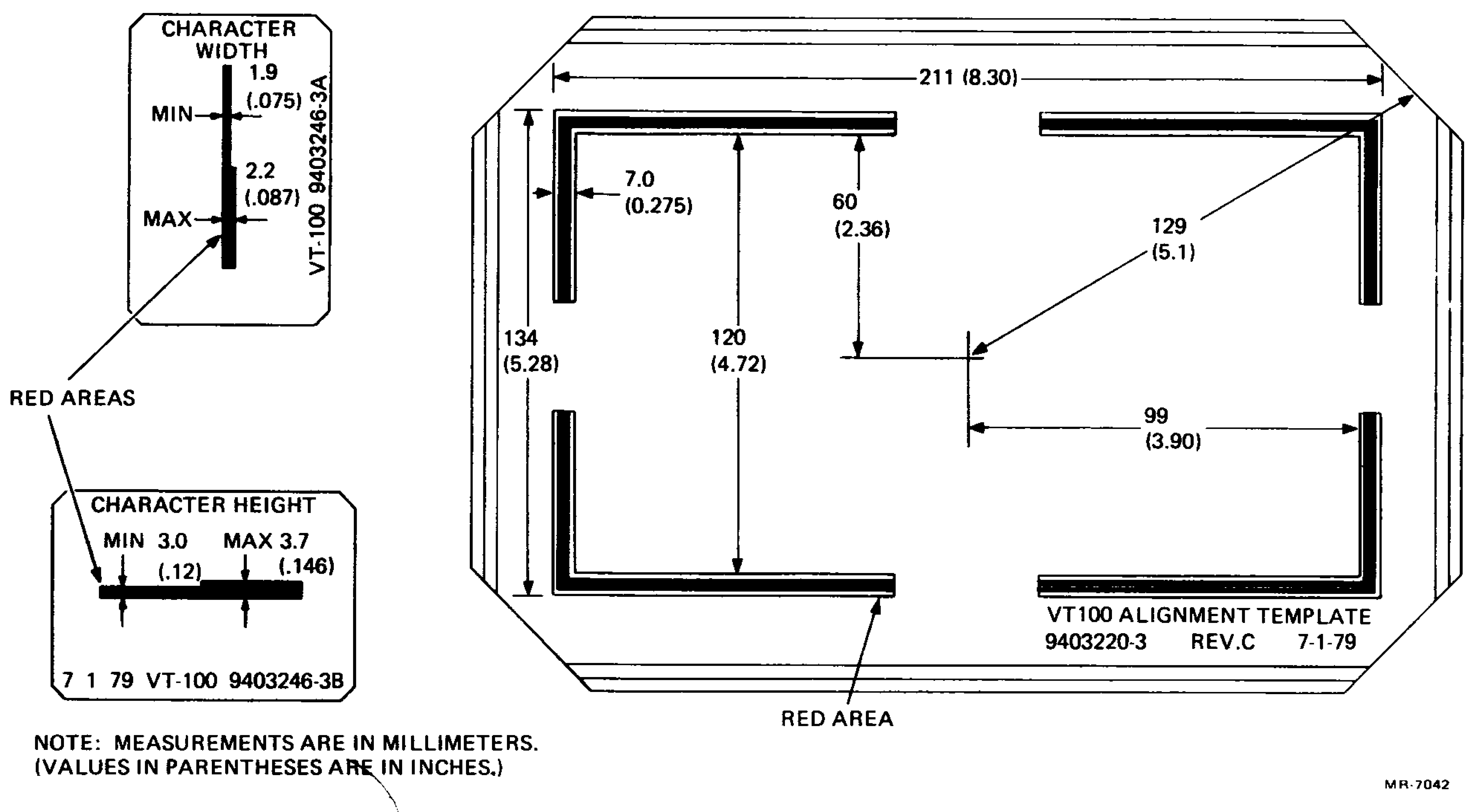

Figure 7-2 Video Alignment Template Dimensions

7.6.1.1 Making a Paper Template – You need a pen, a ruler, a triangle (or anything that can help you draw a right angle), scissors, and a 20 by 28 cm (8 by 11 inch) sheet of paper.

1. Mark a dot in the center of the sheet of paper.

2. Referring to Figure 7-2, make a rectangle on your paper that measures to the inside of the red area. Draw a rectangle using the triangle, as shown in Figure 7-3.

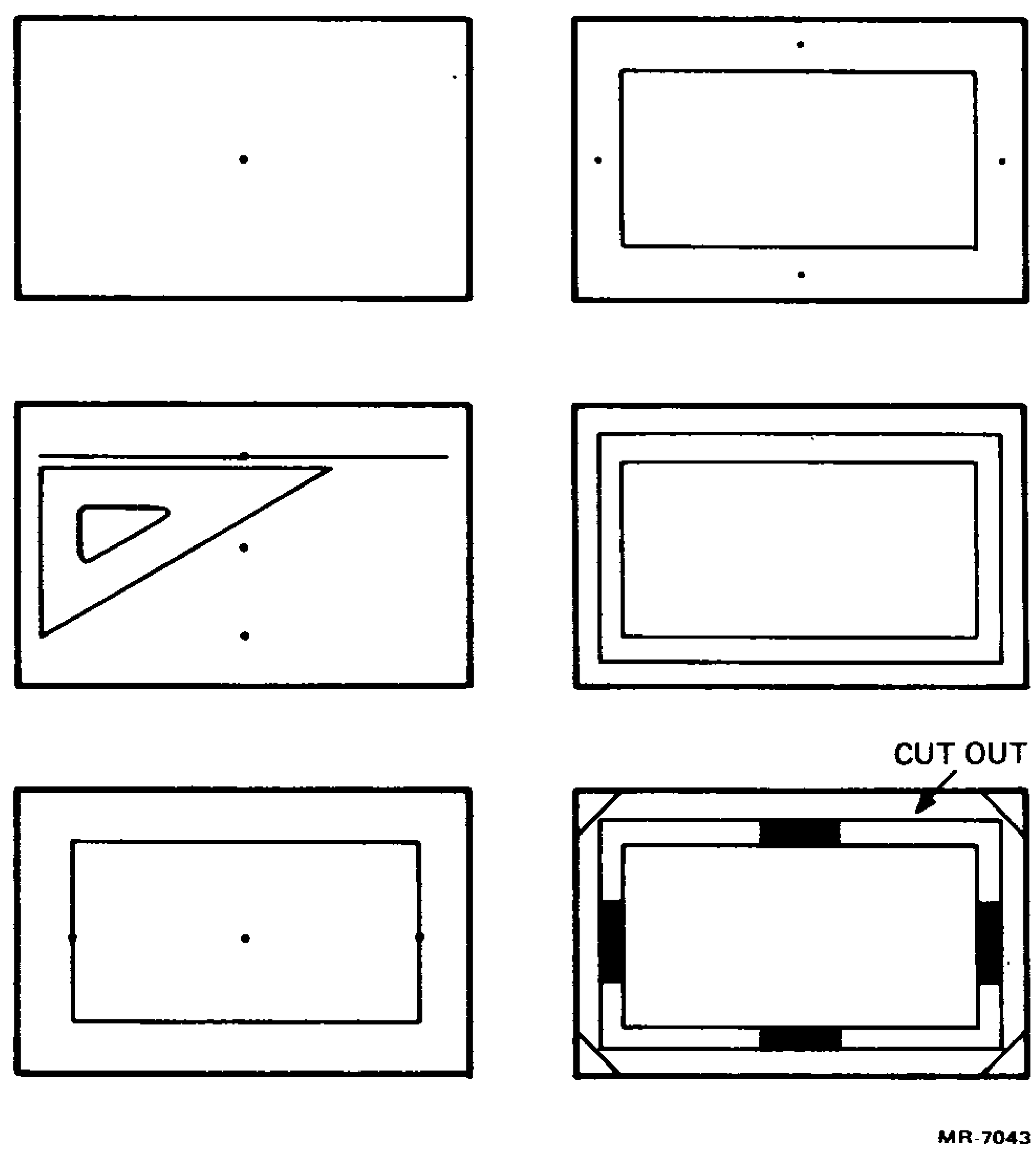

Figure 7-3 Making a Paper Alignment Template

3. On the alignment template the width of the red area is 7 mm (.275 inch). Place a dot 7 mm outside each of the four sides of the rectangle.

4. Draw a line through each dot to form another rectangle around the previous one.

5. Between the two rectangles, mark an area in the center of each side to leave for support (the black areas in Figure 7-3). With scissors cut out the corners between the two rectangles.

6. Measure 12.9 cm (5.1 inches) from the center of the paper to each corner and cut the corners off. This allows you to center the paper template on the CRT.

7.6.1.2 Attaching the Template – The CRT alignment template (94-03220-03) must remain on the screen during all adjustment procedures. However, if you are using a paper template, you may have to remove it for brightness and linearity adjustments. Attach the template to the CRT using the following procedure.

1. Using the bezel around the screen as a guide, mark the four edges of the screen with water-soluble ink from a soft-tip pen.

2. Remove the terminal's top cover. (Refer to Chapter 3, Paragraph 3.4.3.)

3. Tape the CRT alignment template to the screen with all four corners of the template the same distance from the marks you made in step 1.

7.6.2 Monitor Adjustments

The Elston monitor can be identified by the position of the flyback transformer, which is found on the monitor sideplate opposite the monitor board. Also, the yoke assembly does not have a connector card.

All adjustments must be made under the conditions listed in Paragraph 7.6.

7.6.2.1 Brightness Adjustment – Perform the following steps to adjust the screen's brightness.

1. Increase the brightness to the maximum level with the ↑ key in either SET-UP A or B.

2. Adjust R109 (Figure 7-4) until the display raster is visible; then turn R109 in the opposite direction until the raster disappears.

3. Return the brightness to its usual intensity with the ↓ key in either SET-UP A or B.

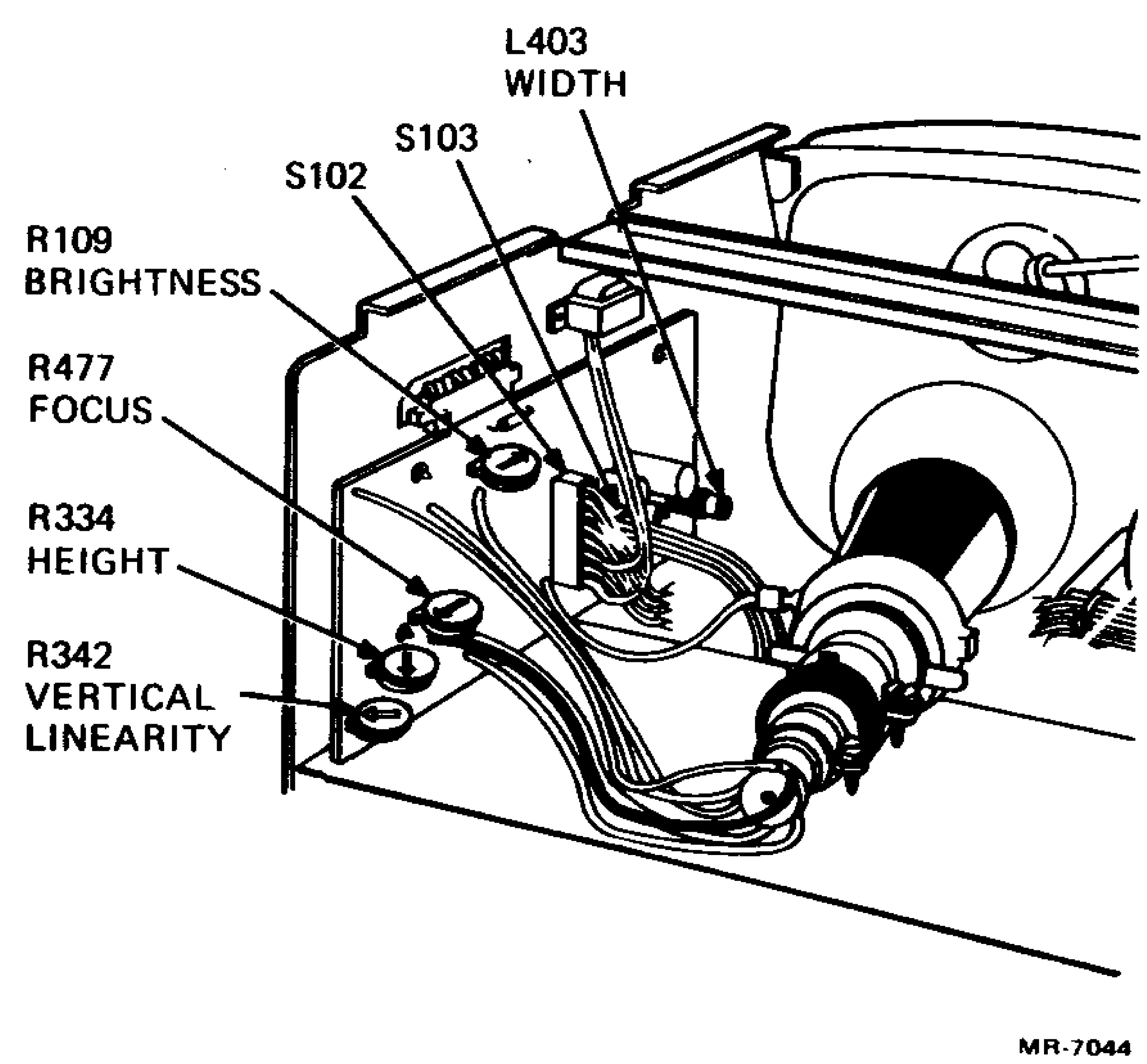

Figure 7-4 Digital/Elston Video Monitor Board Adjustments

7.6.2.2 Yoke Adjustment – Perform the following steps to adjust the yoke.

1. Check that all four sides of the screen display are parallel to the red area of the alignment template.

2. If not parallel, loosen the yoke collar clamp screw (Figure 7-5) and turn the yoke until the four sides of the screen display are parallel to the red area of the alignment template.

3. Check that the yoke is pushed all the way forward toward the face of the CRT. Tighten the yoke collar clamp screen while holding the yoke in place.

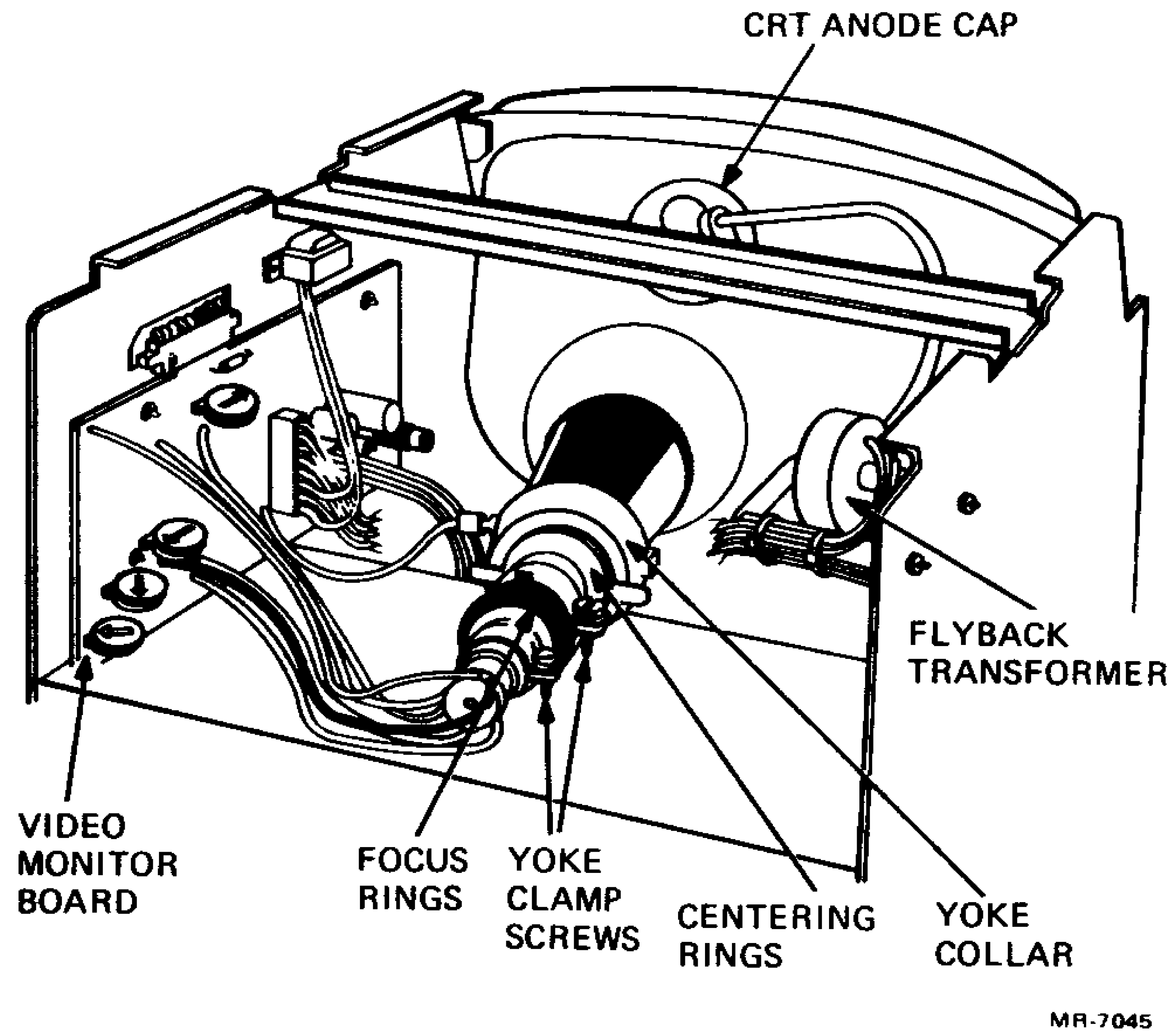

Figure 7-5 Digital/Elston Monitor CRT Adjustments

7.6.2.3 Vertical Height Adjustment – Perform the following steps to adjust the vertical height of the display.

1. Check that the top and bottom lines of the display are covered by the red area of the alignment template.

2. Adjust the vertical height control R334.

7.6.2.4 Horizontal Width Adjustment – Perform the following steps to adjust the horizontal width of the display.

1. Check that the first and last columns of the display are covered by the red area of the adjustment template.

2. Adjust the horizontal width coil L403 with a monitor alignment tool (29-23190).

7.6.2.5 Center Adjustment – Perform the following steps to adjust the display to the center of the video screen.

1. Check that the screen display is in the center of the red area on the alignment template.

2. If necessary, move the display to the center by rotating the front rings found on the neck of the CRT (Figure 7-5).

7.6.2.6 Vertical Linearity Adjustment – Perform the following steps to adjust the vertical linearity.

1. Use the character height template (94-03270-03) to check that the heights of the characters, found at the four corners and the center of the display, are between the minimum and maximum sections of the template.

2. Adjust the vertical linearity using R342.

3. Check and adjust the vertical height (Paragraph 7.6.2.3).

7.6.2.7 Focus Adjustment – Perform the following steps to adjust the focus.

1. Increase the brightness to the maximum level with the ↑ key in set-up. Decrease the brightness eight steps by pressing the ↓ key eight times.

2. Look at the characters at the four corners and in the center of the screen. The discrete dots in the vertical segment of the E should be visible in each character.

NOTE

Some users may want the focus slightly different for their needs. If the focus is adjusted correctly, go to step 5.

3. Adjust R477 (Figure 7-4) for the best character display.

4. Adjust the focus rings, found farthest from the yoke, for the best focus at all four corners (Figure 7-5). Adjust R477 again if necessary.

5. Remove the CRT alignment template, clean the marks from the screen, and replace the terminal's top cover if no more adjustments are needed.

7.7 MODULE AND MECHANICAL ASSEMBLY REMOVAL AND INSTALLATION

This section describes the removal and replacement procedures for modules and mechanical assemblies of the VT180 series of terminals. Unless otherwise stated, each procedure applies to all terminals in the series. Figure 7-6 shows the sequence in which the procedures are to be performed.

7.7.1 Cable Access Cover (Wort Cover) and Module Access Cover (Rear Shield)

Perform the following steps to remove the cable access cover (wort cover) and module access cover (rear shield).

1. Turn the power off by setting the 1/0 switch on the top (or only) disk drive unit to 0 (off). Disconnect the ac power cord from the wall receptacle.

2. Remove the cable access cover (wort cover) from the back of the video terminal by removing the four 6-32 by 5/16 inch screws.

3. Unplug the keyboard cable attached to the back of the module access cover (rear shield). (See Figure 3-20.)

4. Disconnect the BC26K disk drive cable from the disk drive port on the module access cover.

5. Disconnect the communications cable (if installed) from the communications port.

6. Disconnect the printer cable (if installed) from the printer connector.

7. Disconnect any other cables (video-in, video-out, general-purpose serial cables) attached to the module access cover.

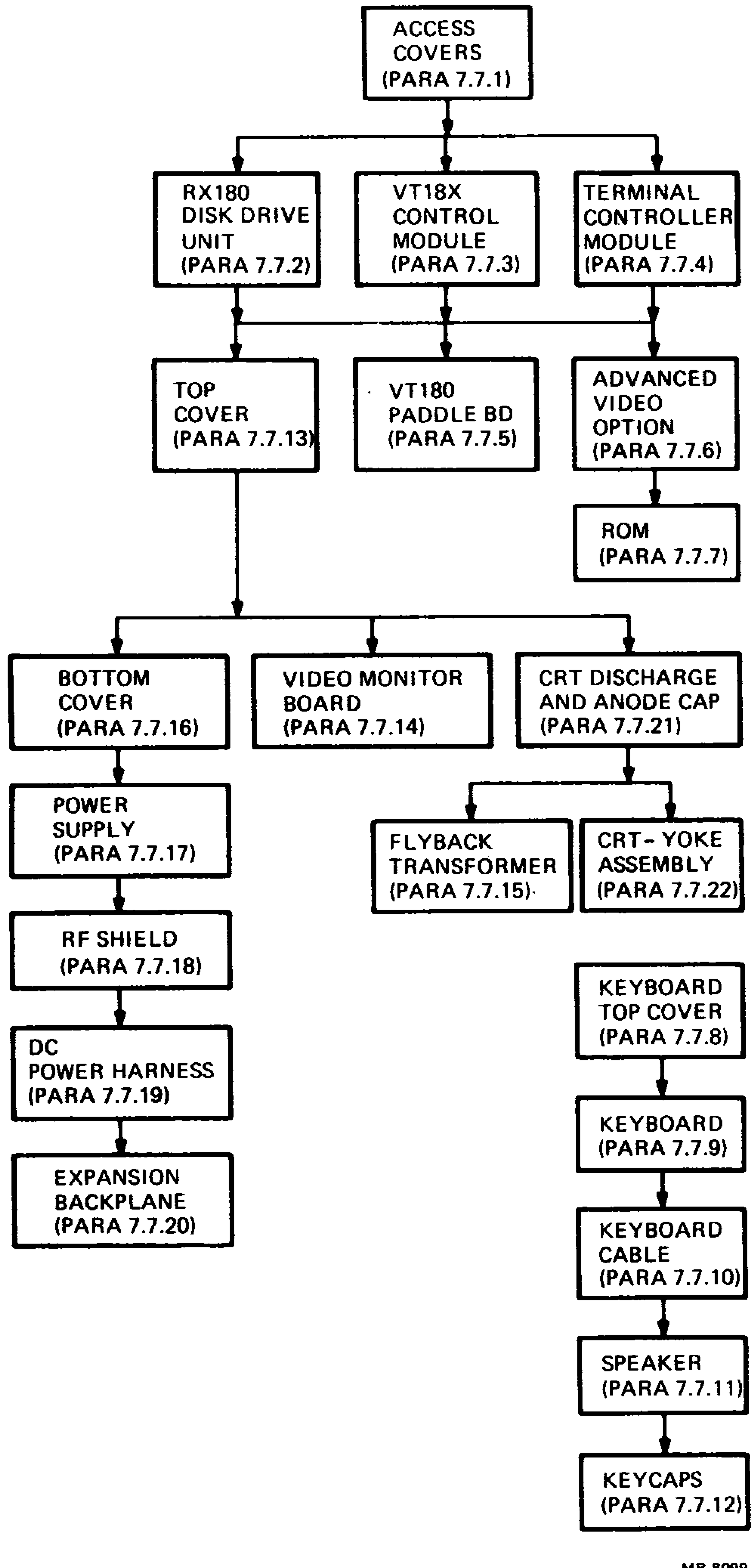

Figure 7-6 Removal Procedure Sequence

8. Remove the hex standoff from each corner of the module access cover (Figure 3-20). Remove the 6-32 by 5/16 inch screw from the center of the module access cover. This screw grounds the VT18X control module to the chassis.

9. Remove the module access cover.

To install the module access cover and cable access cover, perform steps 1 through 8 in reverse.

7.7.2 Disk Drive Unit(s)

Perform the following steps to remove one or two RX180 disk drive units.

CAUTION

Remove all diskettes from the disk drive unit(s) before turning the power on or off.

1. Set the 1/0 switch on the top (or only) disk drive unit to 0 (off).
2. Disconnect the ac line cord from the wall receptacle and from the back of the top (or only) disk drive unit.
3. Remove the ac line cord that connects the terminal to the back of the bottom (or only) disk drive unit.
4. Remove the cable access cover (Paragraph 7.7.1).
5. Disconnect the BC26K disk drive cable from the disk drive port on the module access cover and from the back of the bottom (or only) disk drive unit.

NOTE

If two disk drive units are installed, continue with step 6; if one is installed, go to step 8.

6. Disconnect the BC26Z cable that connects one disk drive unit to the other.
7. Disconnect the ac line cord that connects one disk drive unit to the other.
8. Lift the top disk drive unit (RX180-AB) off the bottom disk drive unit (RX180-AD).

NOTE

When installing two disk drive units, the RX180-AB must be placed on top and cabled so that it is the last disk drive unit on the I/O bus.

Install the disk drive unit(s) by performing steps 1 through 8 in reverse. See Figures 3-26 and 3-27 for correct cable installation.

NOTE

When placing the disk drive unit(s) on top of the video terminal, do not cover the ventilation openings on the terminal.

The authorized spare disk drive unit is the RX180-AB (drives A and B) part number 30-19308-01. To convert this unit to the RX180-AD (drives C and D), refer to special procedures in Paragraph 3.4.12.2.

CAUTION

When replacing a disk drive unit in the field, always set the ac voltage selector on the back of the disk drive unit for the line voltage of the system — 115 Vac or 230 Vac. If set incorrectly, you may damage the power supply.

7.7.3 VT18X Control Module

Perform the following steps to remove the VT18X control module.

1. Remove the cable access cover and module access cover (Paragraph 7.7.1).

2. Pull the VT18X control module out from J2 of the backplane and partially out of the card cage (Figure 3-18).

CAUTION

The ribbon cable connectors in step 3 damage easily. Gently lift each end of the connector with a small flat screwdriver.

3. Disconnect the ribbon cable attached to the IC connector on this module. (This cable comes from the VT180 paddle board in the STP connector.)

4. Remove the VT18X control module from the card cage.

To install this module, perform steps 1 through 4 in reverse.

7.7.4 Terminal Controller Module

Perform the following steps to remove the terminal controller module.

1. Remove the cable access cover and module access cover (Paragraph 7.7.1).

2. Pull the VT18X control module (Figure 3-18) partially out of the card cage and disconnect the ribbon cable from the IC connector on the module.

3. Remove the chassis ground screw from the paddle board and pull the terminal controller module partially out of the card cage. Disconnect the ground wire (if present) from the metal bracket at the EIA connector.

4. Remove the terminal controller module from the card cage.

5. Remove the VT180 paddle board from the STP connector on the terminal controller module (Paragraph 7.7.5).

6. If you are installing a new terminal controller module, remove the advanced video option (if present) from the old module and place it on the new module (Paragraph 7.7.6).

To install the terminal controller module, perform steps 1 through 6 in reverse. Be sure to connect the cables and any ground wires.

NOTE

Check the terminal controller module and the advanced video option for their correct ROM configuration. (See Chapter 3.) Refer to Paragraph 3.4.13 for ROM removal and installation procedures.

Remember to reconfigure the terminal to the customer's original set-up selections, which should be listed on the set-up label under the keyboard.

7.7.5 VT180 Paddle Board

Perform the following steps to remove the VT180 paddle board.

1. Remove the cable access cover and the module access cover (Paragraph 7.7.1).
2. Remove the VT18X control module (Paragraph 7.7.3).
3. Remove the terminal controller module (Paragraph 7.7.4).
4. Remove the screw and washer holding the VT180 paddle board to the terminal controller module (Figure 3-9).
5. Gently pull the paddle board out of the STP connector on the terminal controller module.
6. Using a small flat screw driver, remove the 16-pin flat cable from the VT180 paddle board.

To install the paddle board, perform steps 1 through 6 in reverse.

NOTE

If you remove the VT180 paddle board from the terminal controller module, check that all pairs of contacts in the STP connector come together to make electrical contact.

7.7.6 Advanced Video Option (AVO)

Perform the following steps to remove the advanced video option (AVO).

1. Remove the cable access cover and module access cover (Paragraph 7.7.1).
2. Remove the terminal controller module (Paragraph 7.7.4).
3. Hold the advanced video option by its edges and lift it straight up and off the terminal controller module (Figure 3-5).

To install the advanced video option (AVO), perform steps 1 through 3 in reverse.

NOTE

Check the AVO for the presence of ROMs and jumpers installed (or switches set). Refer to Chapter 3 for correct configuration.

7.7.7 Terminal Controller Module ROMs

If a ROM is defective or if the terminal is a variation with special ROMs, refer to Paragraphs 3.4.13 for the ROM removal and installation procedure.

7.7.8 Keyboard Top Cover

Perform the following steps to remove the keyboard top cover.

1. Set the 1/0 switch on the top (or only) disk drive unit to 0 (off).
2. Unplug the keyboard from the video terminal.

3. With a flat screwdriver, loosen the captive screws on the bottom of the keyboard that hold the keyboard together (Figure 7-7).

4. Remove the top cover by lifting it straight up.

To install the keyboard top cover, perform steps 1 through 4 in reverse.

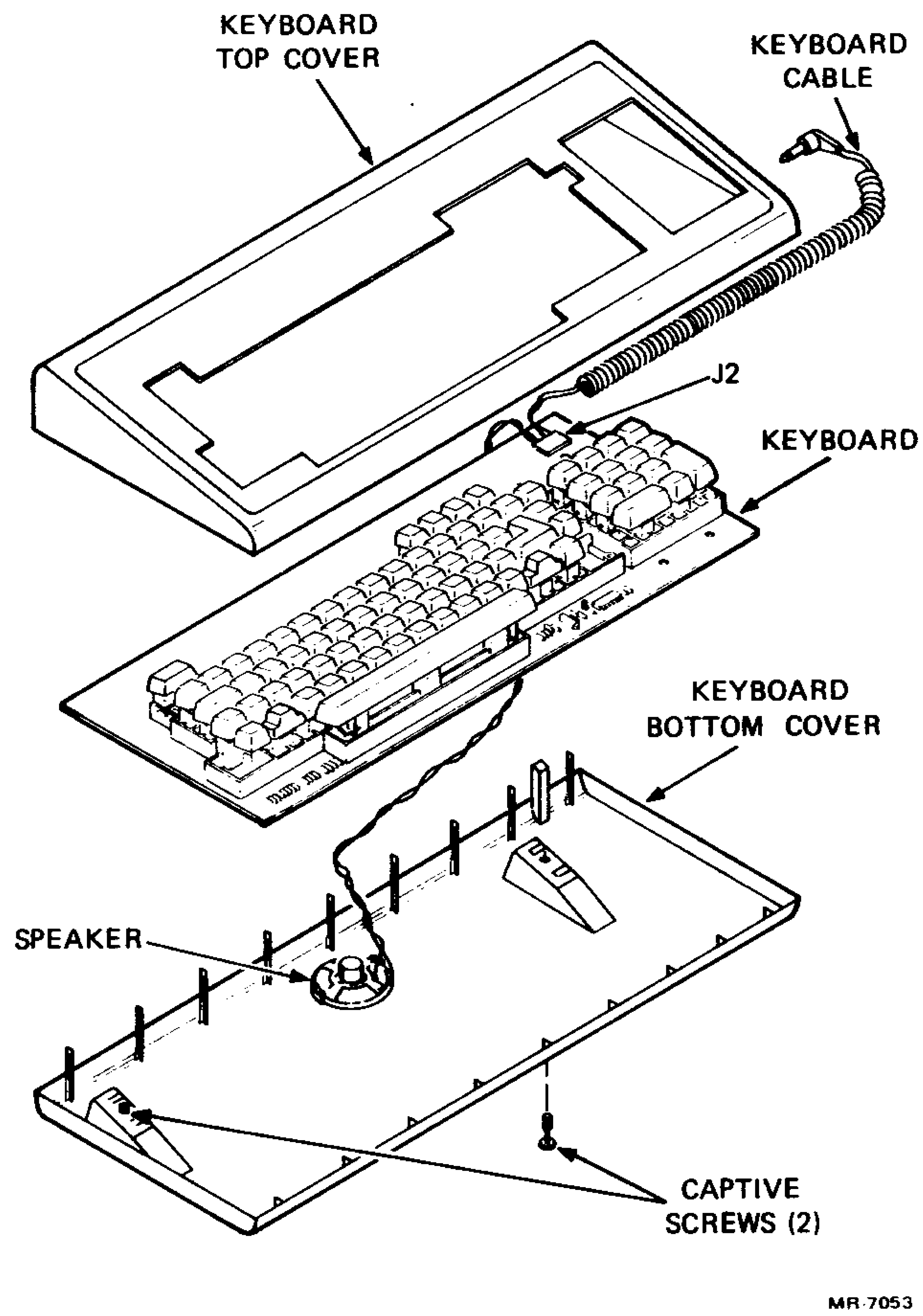

Figure 7-7 Keyboard Disassembly

7.7.9 Keyboard
Perform the following steps to remove the keyboard.

1. Remove the keyboard top cover (Paragraph 7.7.8).
2. Disconnect keyboard cable J2 from the keyboard.
3. Remove the keyboard.

To install the keyboard, perform steps 1 through 3 in reverse.

7.7.10 Keyboard Cable
Perform the following steps to remove the keyboard cable.

1. Remove the keyboard top cover (Paragraph 7.7.8).
2. Remove the keyboard (Paragraph 7.7.9).

3. Disconnect the keyboard cable from the speaker.
4. Remove the keyboard cable.

To install the keyboard cable, perform steps 1 through 4 in reverse.

7.7.11 Keyboard Speaker

Perform the following steps to remove the keyboard speaker.

1. Remove the keyboard top cover (Paragraph 7.7.8).
2. Remove the keyboard (Paragraph 7.7.9).
3. Remove the keyboard cable (Paragraph 7.7.10).
4. Remove the speaker by moving it toward the front edge of the keyboard cover.

To install the keyboard speaker, perform steps 1 through 4 in reverse.

7.7.12 Keycaps

The tools needed to remove and install keycaps are a keycap puller and a pair of needlenose pliers. Perform the following steps to remove keycaps. Reverse the procedure to install them.

1. Remove power from the terminal by turning it off.

2. Starting at the upper left corner of the keyboard, insert the keycap puller between the first keycap to be replaced and the adjacent keycap (Figure 7-8).

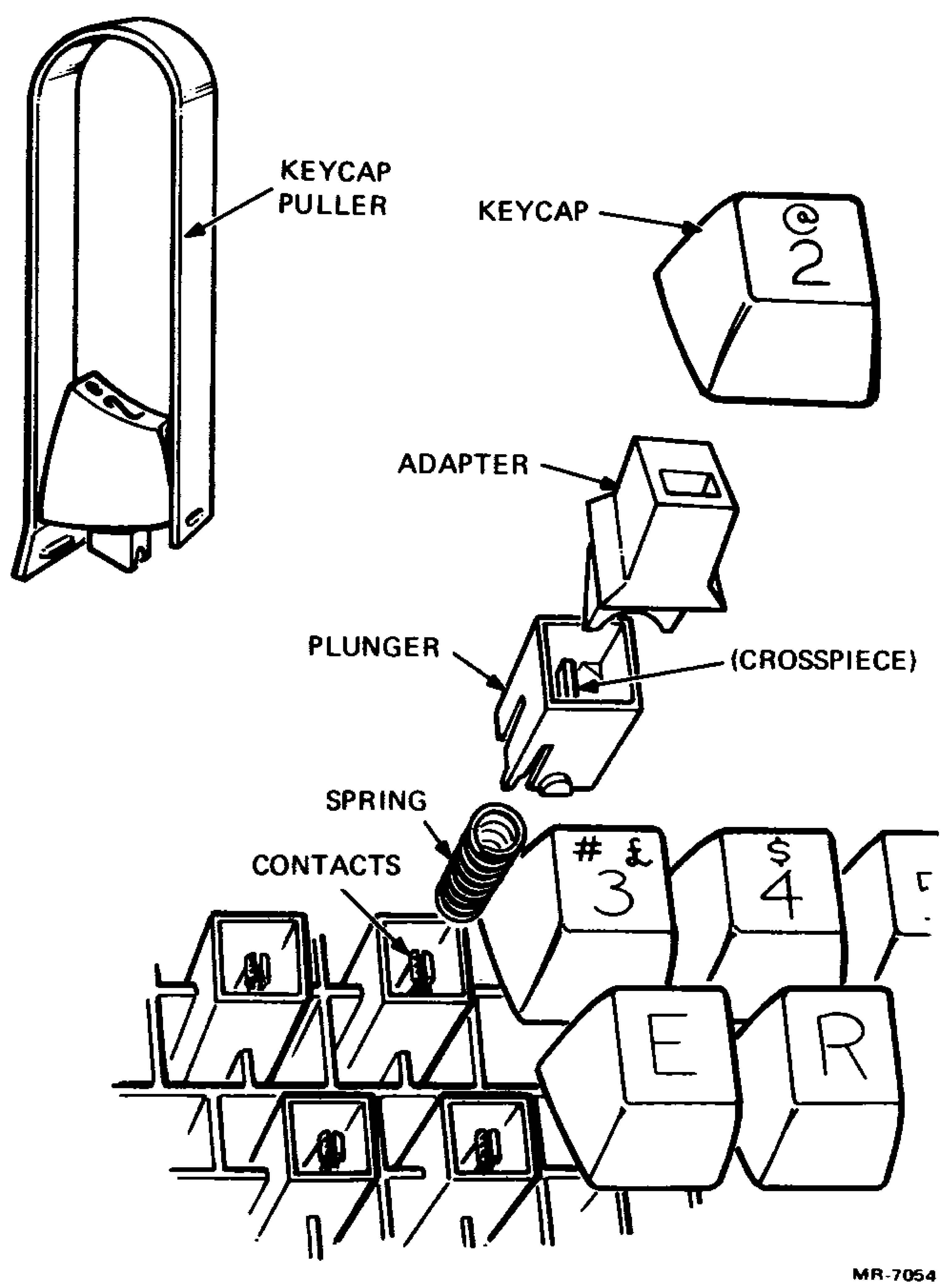

Figure 7-8 Keycap Removal

3. Compress the puller around the keycap and slowly pull it straight up.

4. If the adapter does not come off with the keycap, carefully remove the adapter with needlenose pliers. Reinstall the adapter in the keycap, making sure the pointed end faces the front of the keycap.

NOTE
In some keyboards the adapter and the keycap are one part.

5. In the event that the plunger comes off, take care to prevent the spring from flying out. Referring to Figure 7-8, replace the plunger and spring as follows.

CAUTION
You must follow this procedure carefully to prevent damage to key contacts.

   a. Slide the spring into the plunger. Place the spring and plunger into the slot and over the key contacts. Make sure the crosspiece of the plunger is vertical, not horizontal.

   b. Slowly push the plunger down until the crosspiece touches the contacts. Release the plunger and check that the contacts are separated.

6. Find a correct replacement keycap. Gently press the keycap straight down onto the plunger until it is completely installed.

7. Repeat this procedure for each keycap to be replaced.

8. Store all spare keycaps in a safe location for later use.

Test After Installation
Perform the following steps to check that the keycaps are correctly installed.

1. Place the terminal off-line.

2. Press each replacement keycap (both lowercase and uppercase) and make sure the correct character(s) are displayed on the screen.

7.7.13 Top Cover
Perform the following steps to remove and install the top cover.

1. Remove the cable access cover and the module access cover (Paragraph 7.7.1).

2. Remove the ac power cord from the terminal and, if installed on top of the terminal, remove the disk drive unit(s) from the terminal.

3. With a small scriber or a pointed tool, release the four front pop fasteners found under the front and rear edge of the terminal (Figure 3-10).

4. Remove the top cover by lifting it straight up.

5. Check if the VT180 logo has been installed. If not, position the top cover face down on a soft surface to remove and replace the VT100 logo. To remove the logo, use a pair of needlenose pliers and a flat blade screwdriver to pry up the retaining rings from the back of the VT100 logo and install the VT180 logo. See Figure 3-19.

6. To install the top cover, seat the top cover on the bottom cover and push the pop fasteners up into the top cover until they lock into place.

7. Attach the ac power cord from the wall receptacle to the top (or only) disk drive unit. Daisy-chain the power with a power cord to the second disk drive unit (if installed), then to the terminal (Figures 3-26 and 3-27).

8. Install the module access cover and the cable access cover (Paragraph 7.7.1).

7.7.14 Video Monitor Board (Digital or Elston)

Perform the following steps to remove the video monitor board (Digital or Elston).

1. Remove the top cover (Paragraph 7.7.13).
2. Remove the circular connector from the base of the CRT (Figure 7-9).
3. Disconnect the white wire connecting the video monitor board to the yoke ground lug.
4. Disconnect the 8-pin connector from the video monitor board.
5. Disconnect the 4-pin connector from the video monitor board.
6. Disconnect the video input connector from the top edge of the video monitor board.
7. Release the four standoffs and remove the video monitor board.

To install the video monitor board, perform steps 1 through 7 in reverse.

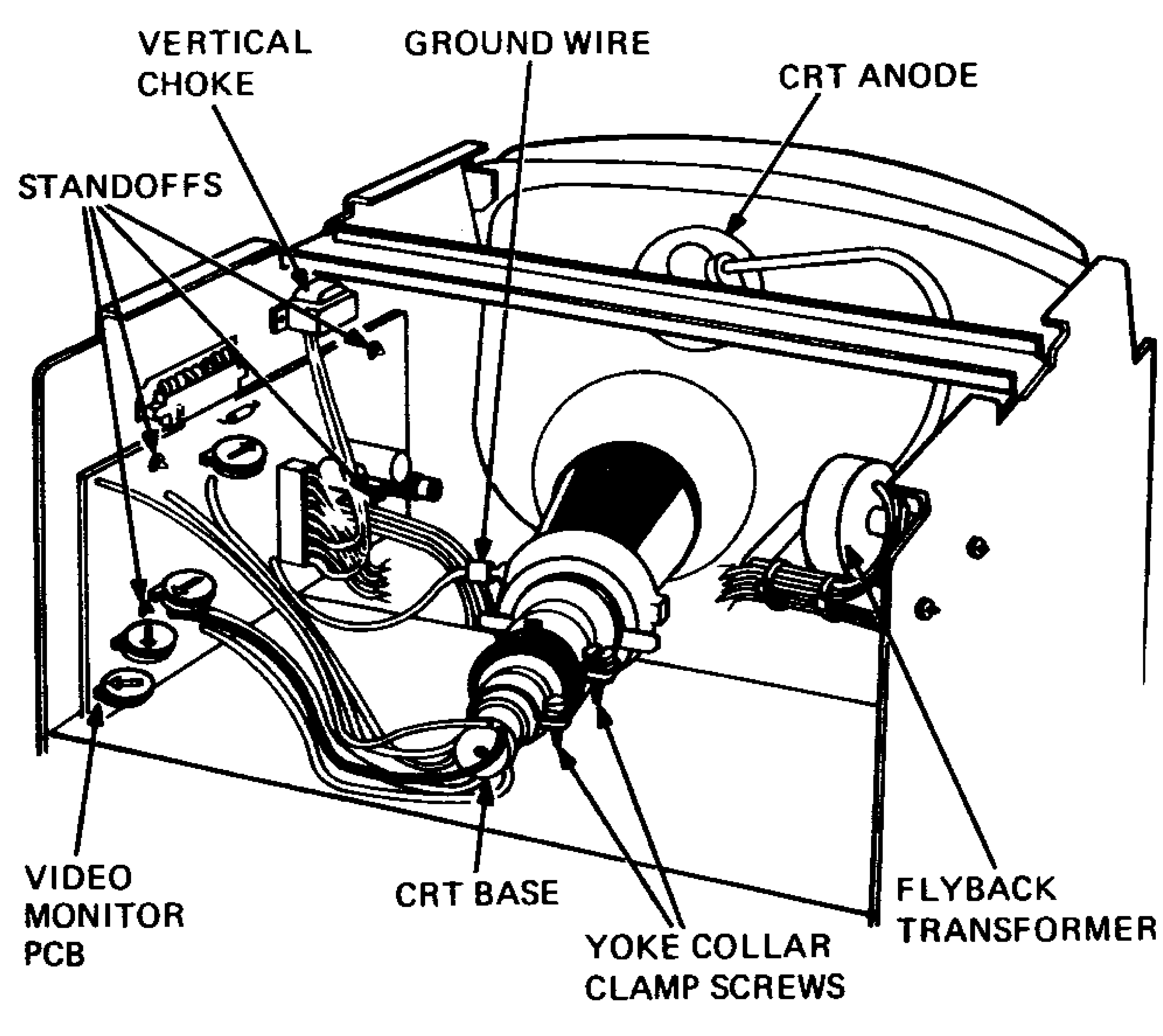

Figure 7-9 Video Monitor Board Removal

CAUTION
Be sure to align the 8-pin connector correctly when connecting the cable. The video monitor board may be damaged if the connector is not installed correctly.

7.7.15 Flyback Transformer (Digital or Elston)

Perform the following steps to remove the flyback transformer (Digital or Elston) (Figure 7-9).

WARNING
The CRT anode may hold high voltage. Refer to Paragraph 7.7.21.1 for the anode discharge procedure.

1. Remove the top cover (Paragraph 7.7.13).
2. Disconnect the 8-pin connector from the video monitor board.
3. Remove the screw and washer fastening the vertical choke to the monitor chassis. Remove the vertical choke.
4. Discharge the high voltage at the CRT anode. Refer to Paragraph 7.7.22.1 for this procedure.
5. Disconnect the CRT anode wire from the CRT. Refer to Paragraph 7.7.22.2 for this procedure.
6. Using a ¼ inch nutdriver, remove the two nuts mounting the flyback transformer to the monitor chassis.

To install the flyback transformer, perform steps 1 through 6 in reverse.

CAUTION
Be sure to align the 8-pin connector correctly when connecting the cable. The video monitor board may be damaged if the connector is not installed correctly.

7.7.16 Bottom Cover Removal and Installation

The removal and installation procedure for the bottom cover is described in Paragraphs 3.4.3 and 3.4.8.

7.7.17 Power Supply

Perform the following steps to remove the power supply.

1. Remove the top cover (Paragraph 7.7.13).
2. Remove the bottom cover (Paragraph 7.7.16).
3. Find the three pop fasteners on the side of the chassis. Release these pop fasteners by pulling their plungers out (Figure 7-10).

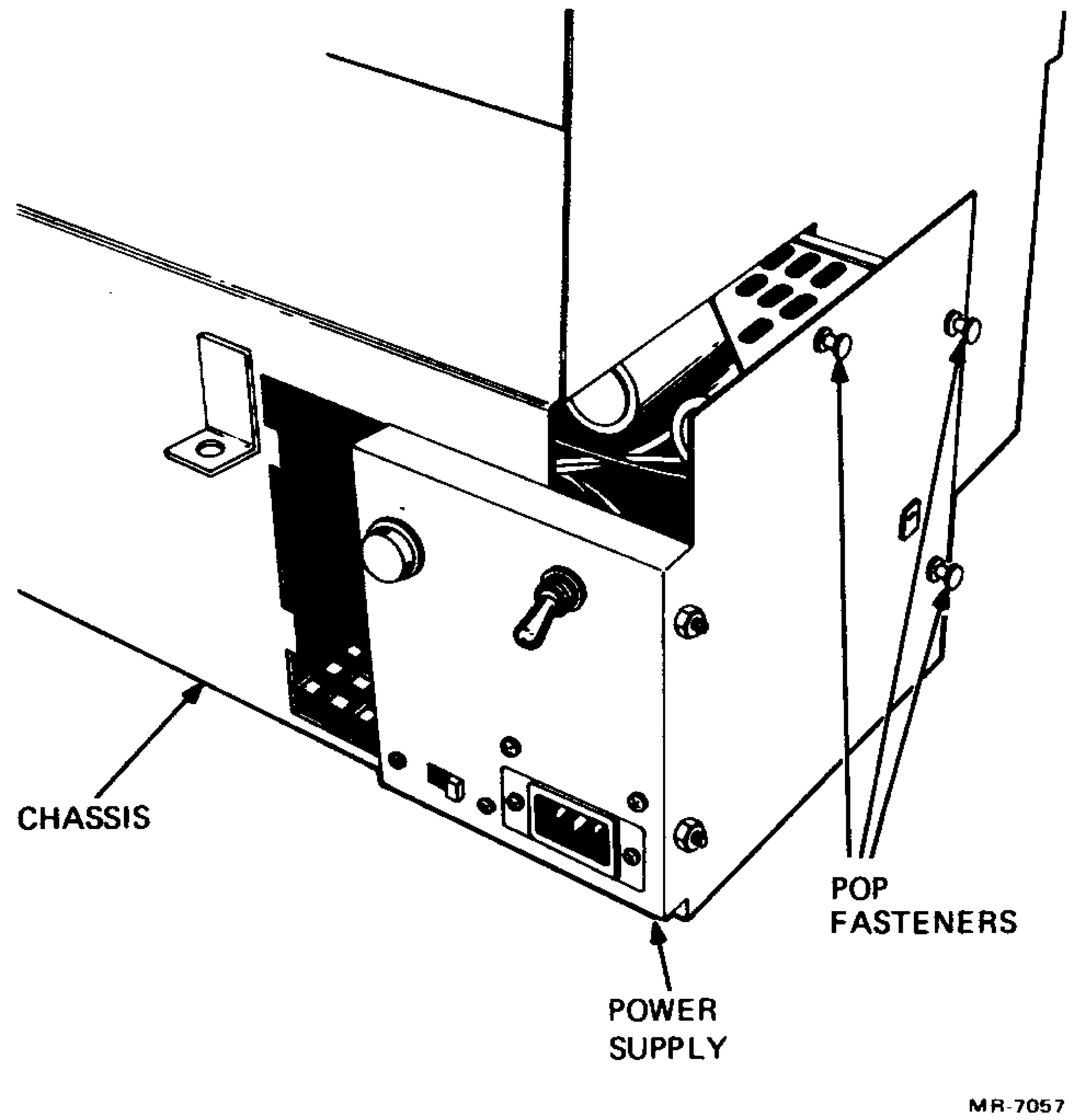

Figure 7-10 Power Supply Removal

WARNING

Capacitors C9, C14, and the circuits in the same area hold 300 Vdc. To discharge the capacitors, leave the power supply plugged into the terminal for a minimum of four minutes after the power cord is removed.

After the power supply is out of the terminal, make sure the capacitors are completely discharged. Short the capacitors with an insulated wire as shown in Figure 7-11.

4. Hold the power supply by its end plate and pull it straight out.

To install the power supply, perform steps 1 through 4 in reverse. Note that there is a grounding tab on the back of the chassis that fits into a small slot in the end of the power supply's switch plate.

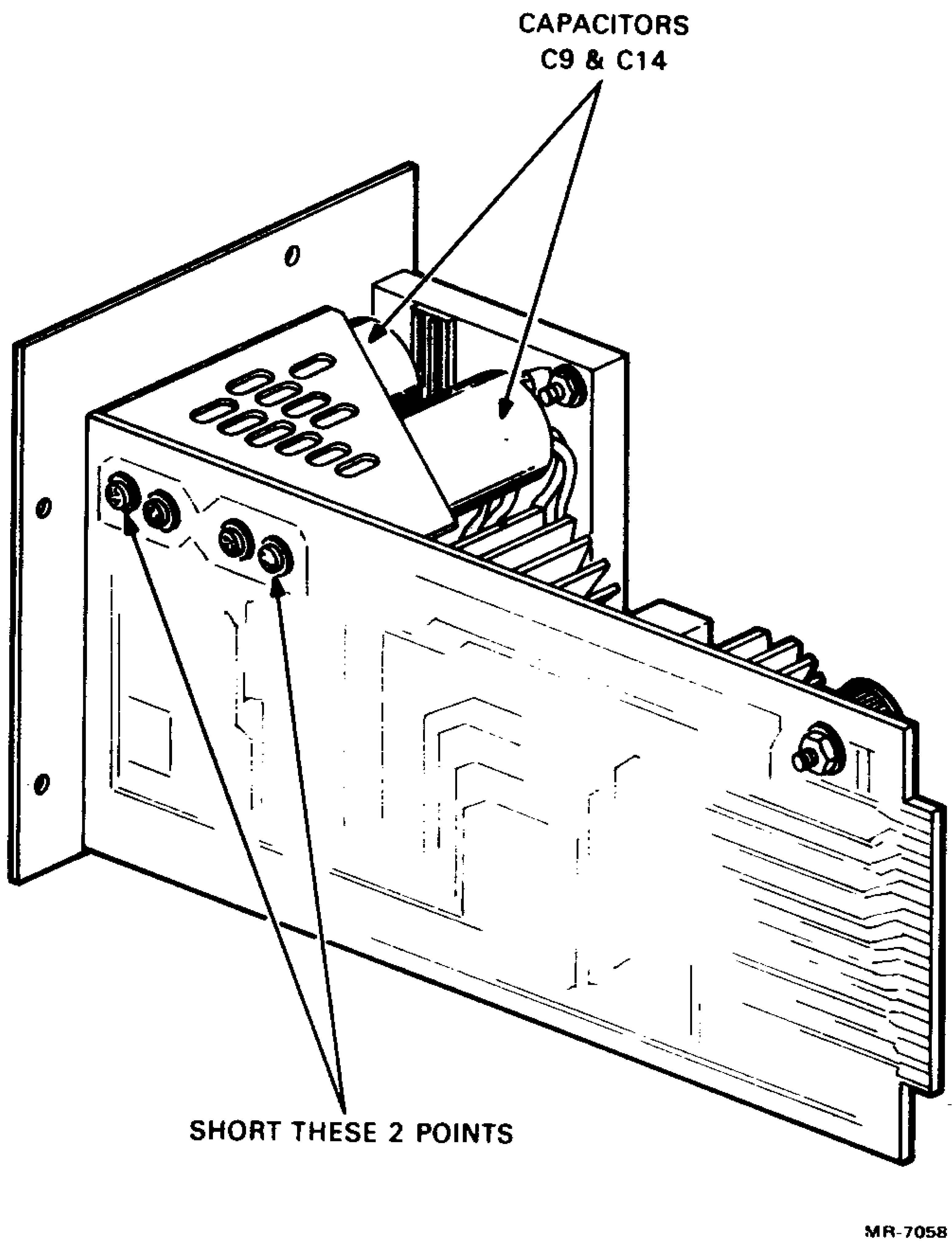

Figure 7-11 Discharging the Power Supply Capacitors

7.7.18 RF Shield Removal

Perform the following steps to remove the RF (radio frequency) shield.

1. Remove the cable access cover and module access cover (Paragraph 7.7.1).
2. Remove the disk drive unit(s) from the terminal (Paragraph 7.7.2).
3. Remove the VT18X control module (Paragraph 7.7.3).
4. Remove the terminal controller module (Paragraph 7.7.4).
5. Remove the top cover (Paragraph 7.7.13).
6. Remove the bottom cover (Paragraph 7.7.16).
7. Set the chassis on end with the card cage up.
8. Remove four ¼ inch hex-head screws from the top and bottom of the RF shield (Figure 7-12).
9. Carefully remove the RF shield from around the card cage. Take care not to damage the shield.

To install the RF shield, use a scriber to line up the screw holes and install the (four) screws.

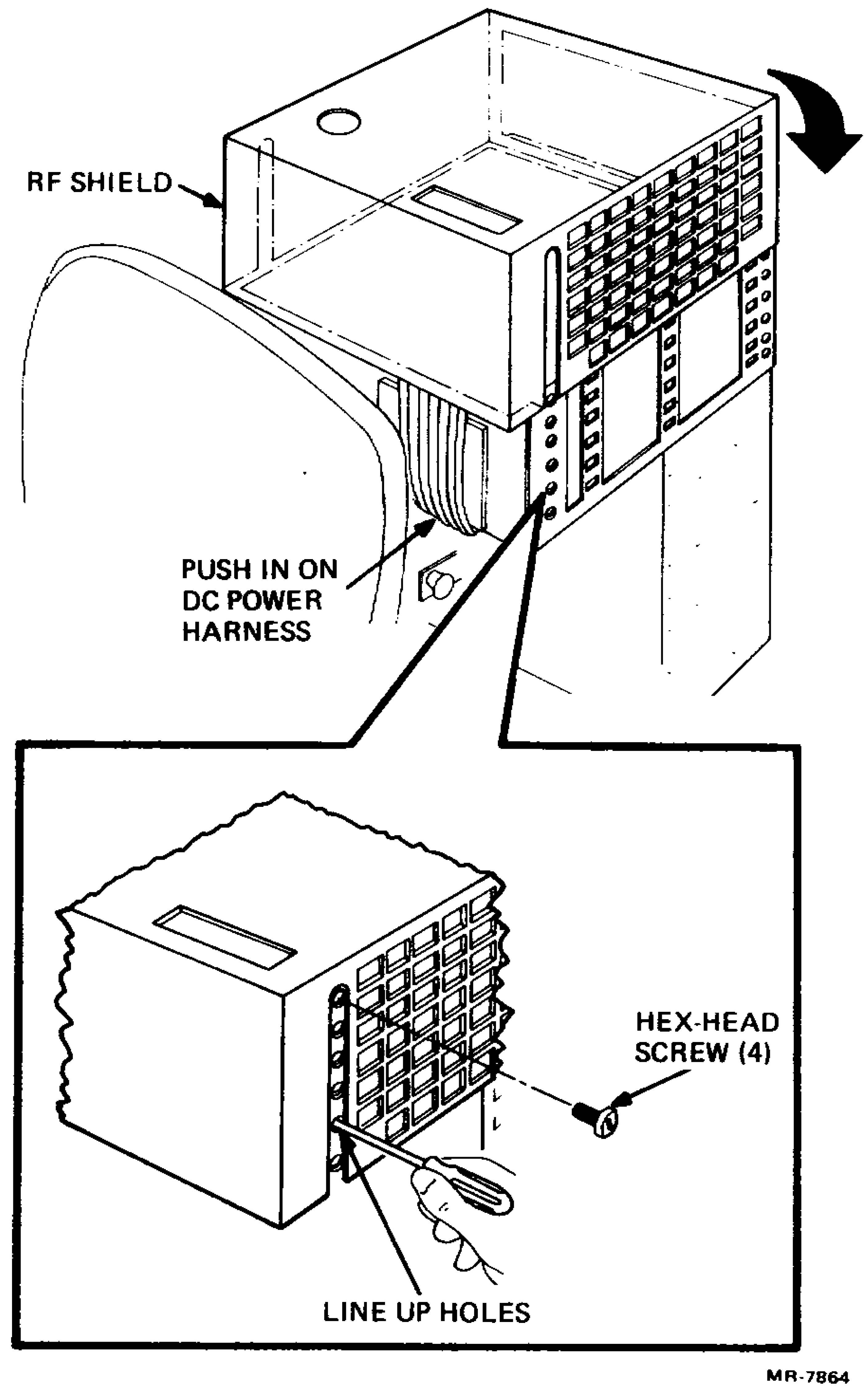

Figure 7-12 RF Shield Removal and Installation

7.7.19 DC Power Harness

Perform the following steps to remove the dc power harness.

1. Remove the cable access cover and module access cover (Paragraph 7.7.1).
2. Remove the disk drive unit(s) from the terminal (Paragraph 7.7.2).
3. Remove the VT18X control module (Paragraph 7.7.3).
4. Remove the terminal controller module (Paragraph 7.7.4).
5. Remove the top cover (Paragraph 7.7.13).
6. Remove the bottom cover (Paragraph 7.7.16).
7. Remove the RF shield (Paragraph 7.7.18).
8. Remove the power supply (Paragraph 7.7.17).

9. Disconnect the dc power harness from the expansion backplane.

10. Disconnect the 10-pin edge connector J101 from the video monitor board.

11. Remove the card cage by releasing the two pop fasteners that hold the top of the card cage to the chassis. (Remove two Phillips screws on late model terminals.) Tilt the card cage out slightly, then lift the card cage out of the bottom holding clips (chassis slots on late model terminals).

12. Disconnect the ground wire from the 10-pin connector to the monitor chassis.

13. Remove the two E-ring fasteners (spread the spring clips on late model terminals), holding the 18-pin edge connector to the chassis. Remove the connector.

14. Remove the dc power harness.

To install the dc power harness, perform steps 1 through 14 in reverse.

7.7.20 Expansion Backplane Removal
Perform the following steps to remove the expansion backplane.

1. Remove the cable access cover and module access cover (Paragraph 7.7.1).

2. Remove the disk drive unit(s) from the terminal (Paragraph 7.7.2).

3. Remove the VT18X control module (Paragraph 7.7.3).

4. Remove the terminal controller module (Paragraph 7.7.4).

5. Remove the top cover (Paragraph 7.7.13).

6. Remove the bottom cover (Paragraph 7.7.16).

7. Remove the RF shield (Paragraph 7.7.18).

8. Disconnect the dc power harness from the expansion backplane.

9. Remove the four 4-40 by ½ inch screws, spacers, and kep nuts fastening the expansion backplane to the card cage (Figure 3-14).

To install the expansion backplane, perform steps 1 through 9 in reverse.

7.7.21 CRT Discharge and Anode Cap

7.7.21.1 CRT Anode Discharge – To discharge the CRT anode, use either of the following methods.

- Connect the plug end of a VOM lead to chassis ground. Discharge the anode by touching the probe to the CRT anode (Figure 7-13).

- Gently place the end of a screwdriver with an insulated handle under the plastic anode cap on top of the CRT while shorting the other end of the screwdriver to an unpainted part of the CRT chassis.

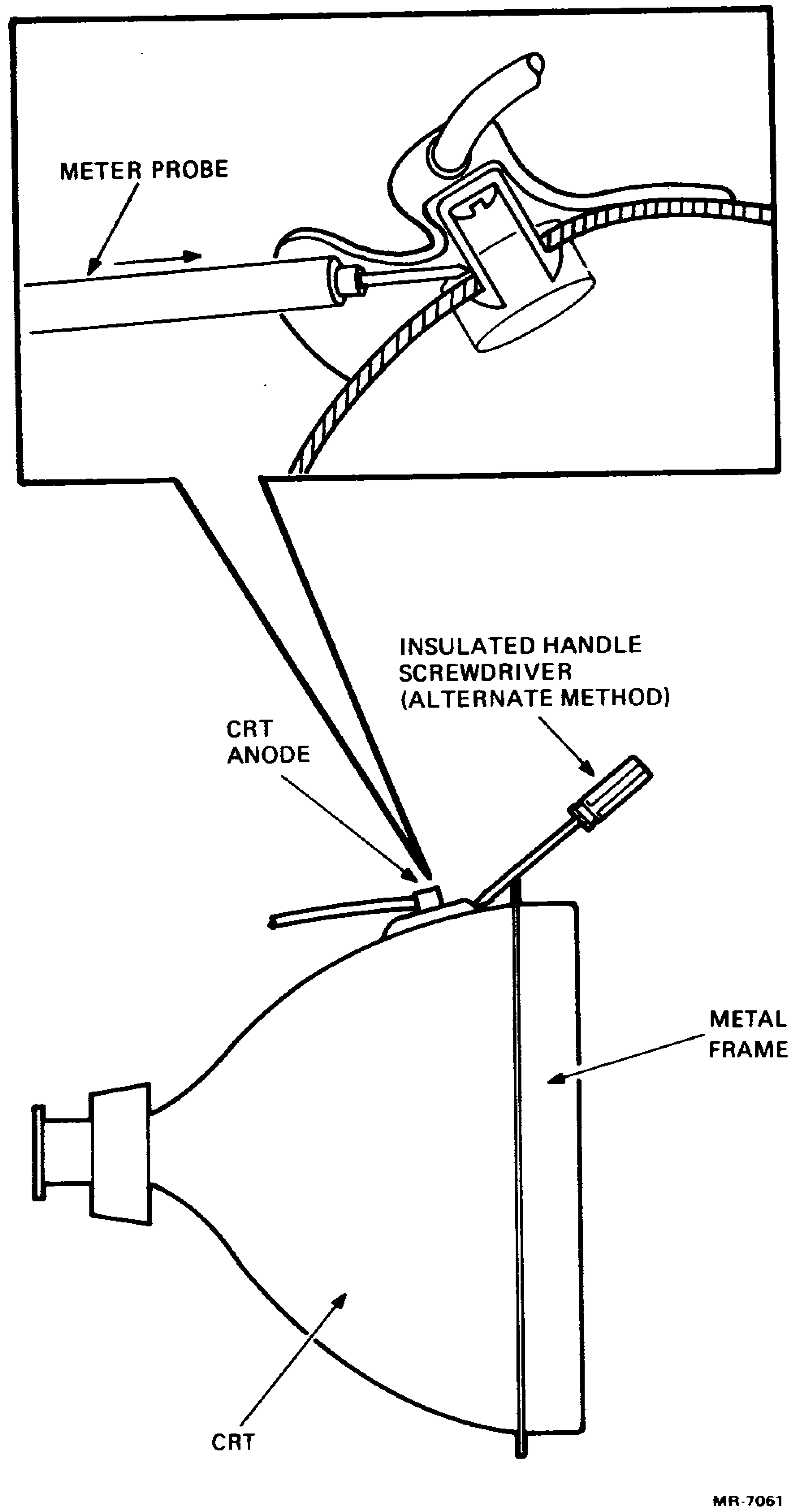

Figure 7-13 Discharging the CRT Anode

7.7.21.2 Anode Cap Removal and Installation – Perform the following steps to disconnect the CRT anode cap from the CRT.

1. Note the position of the anode wire.

2. The connector holds itself in place with spring barbs in the anode socket of the tube. Push against one barb, allowing it to clear the edge of the anode socket (Figure 7-14).

3. Push up in the opposite direction to release the other barb.

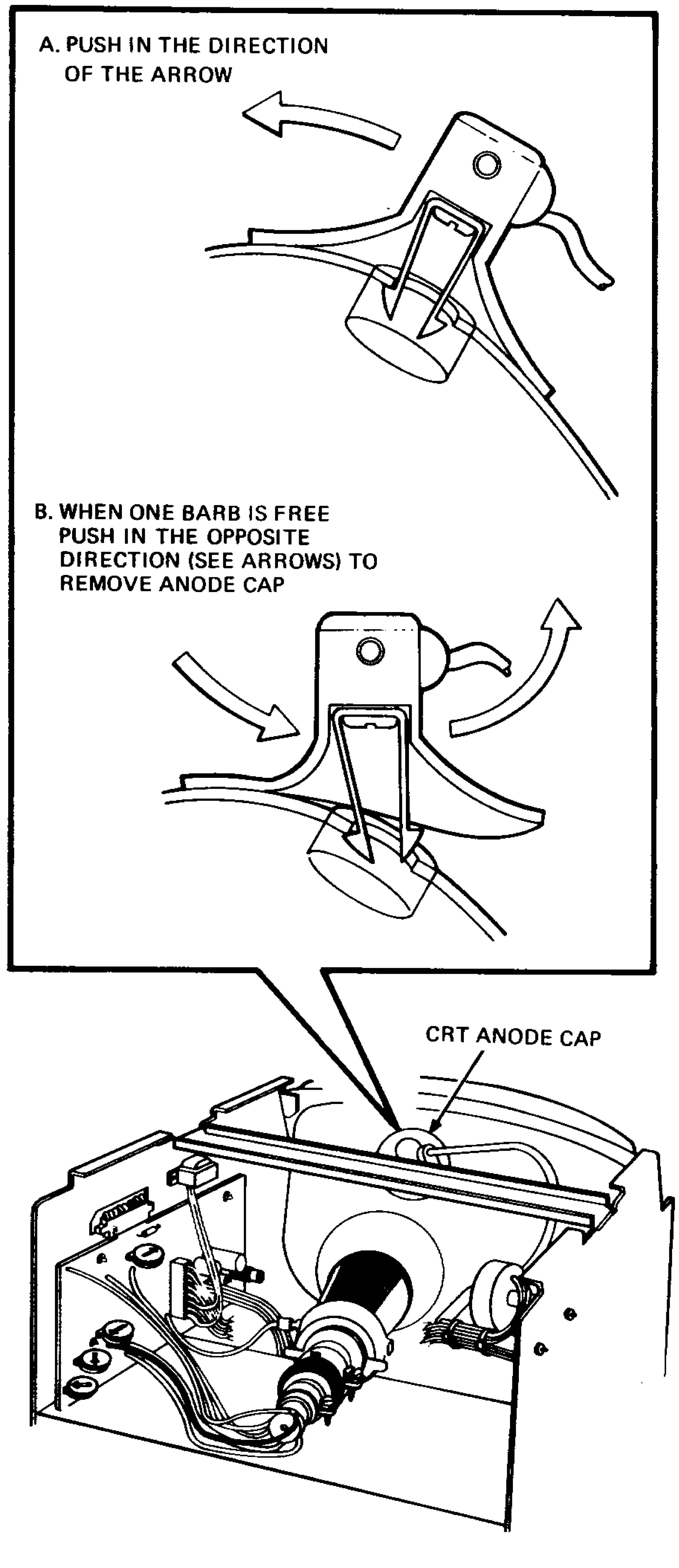

Figure 7-14 Removing the Anode Cap

7.7.22 CRT and Yoke Assembly

Elston terminals can be repaired with a new CRT and yoke assembly without having to replace the complete chassis assembly. When replacing the CRT and yoke on early model terminals, replace the flyback, choke, and monitor board with Elston parts at the same time. Perform the following steps to remove the CRT and yoke assembly.

WARNING
High voltage is present at the CRT anode. Refer to Paragraph 7.7.21.1 to discharge the anode.

1. Remove power from the terminal by setting the 1/0 switch on the top (or only) disk drive unit to 0 (off). Remove the ac power cord from the back of the video terminal.

2. If placed on top, remove the disk drive unit(s) from the video terminal (Paragraph 7.7.2). Remove the top cover of the terminal (Paragraph 7.7.13).

3. Discharge the CRT anode (Paragraph 7.7.21.1).

4. Disconnect the CRT high-voltage anode wire (Paragraph 7.7.21.2).

5. Disconnect the circular connector from the CRT base (Figure 7-9).

6. Disconnect the white wire connecting the video monitor board to the yoke ground connector.

7. Disconnect the 4-pin yoke connector from the monitor board.

8. While supporting the assembly from the bottom rear of the CRT, remove the top two screws and then the bottom two screws from the CRT frame.

9. Remove the CRT and yoke assembly.

WARNING
Handle the tube by the sides next to its face, never by its neck. Do not rest the tube on its neck.

To install the CRT and yoke assembly, perform steps 1 through 8 in reverse.

NOTE
Refer to Paragraph 7.7.23 for storing and discarding the CRT.

7.7.23 Field Handling of CRTs

You must use the following procedures when replacing, handling, storing, or discarding a CRT in the field.

7.7.23.1 Replacing a CRT – Note the following when replacing a CRT.

1. Only Digital service personnel should be in the area during replacement.

2. Any service person replacing a CRT must wear goggles (or safety glasses with side guards) and gloves. The part numbers for these items are:

   29-16141 (goggles)
   29-16146 (gloves).

3. Before servicing the CRT or its connected circuits, you must discharge the anode (Paragraph 7.7.21.1).

7.7.23.2 Handling the CRT – Use the following precautions when handling a CRT.

CAUTION

- **Handle the CRT by the sides adjacent to the tube face. Never handle the CRT by its neck.**
- **Do not allow the neck to bump anything.**
- **Never rest a CRT on its neck.**
- **Never scratch the glass of the CRT. Take special care when working around the CRT with any tool.**
- **Never touch the glass of a CRT with a hot soldering tool.**

7.7.23.3 Storing a CRT – All CRTs must be either stored in a closed container or correctly mounted in the product. Never store a CRT without a protective enclosure.

7.7.23.4 Discarding a CRT – If your region has a procedure for discarding CRTs, use that procedure. If not, perform the following steps to discard a CRT. Destroy any CRT that cannot be returned for repair.

WARNING
Use extreme caution when performing this procedure.

1. Place the CRT into the container in which the replacement was received.

2. Close and seal the container, leaving only the end of the CRT's neck exposed (Figure 7-15).

3. With a pair of pliers or wire cutters, carefully break the CRT evacuation point. The evacuation point is found in the center of the CRT neck's end. If the procedure is done correctly, you will hear a sudden rush of air. This means the CRT no longer has a vacuum and can no longer implode.

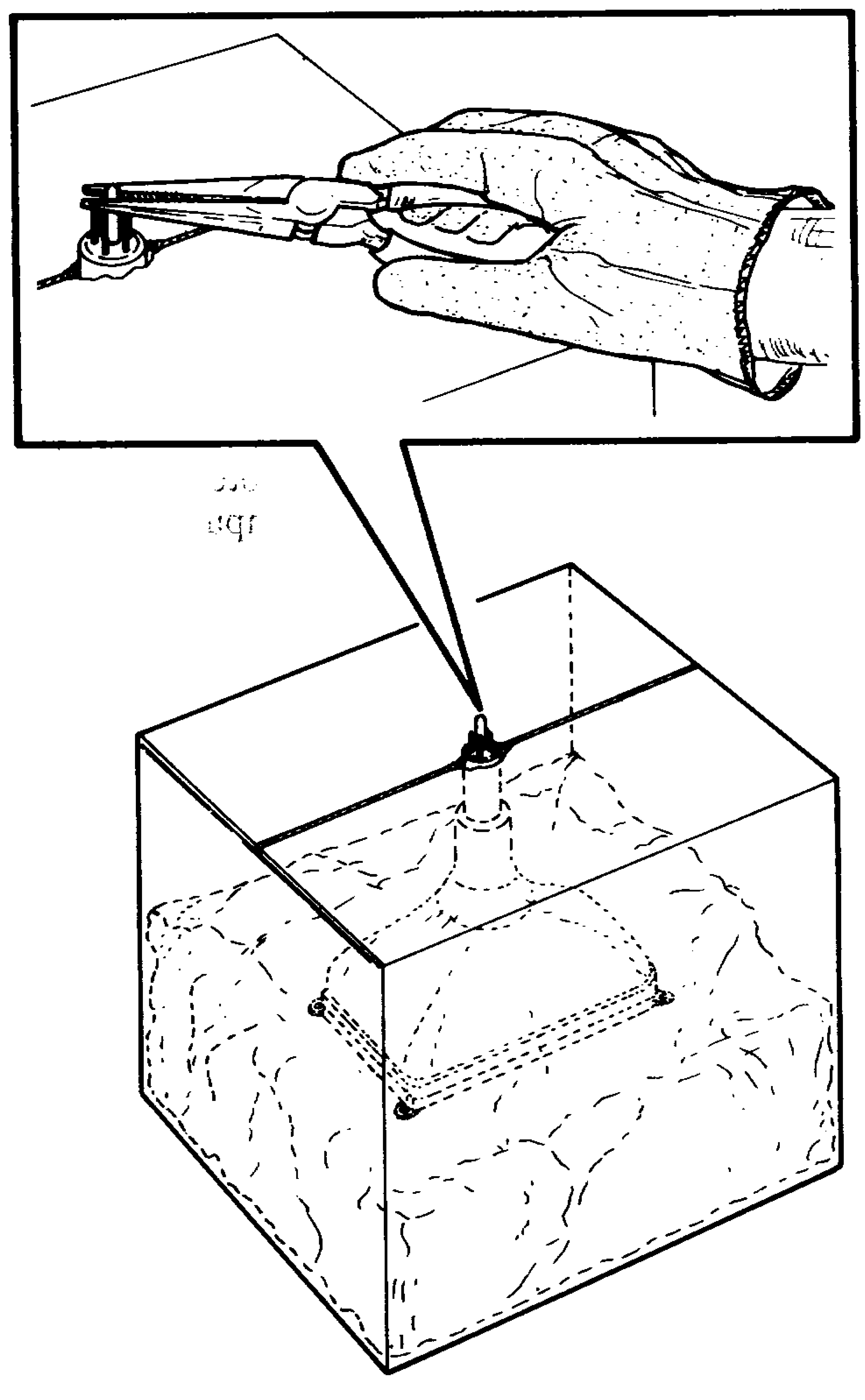

Figure 7-15 Disposing of the CRT

APPENDIX A
VT180 PROGRAMMING INFORMATION

A.1 GENERAL INFORMATION
The VT180 can be operated in either terminal mode or personal computer mode.

The VT180 operating in terminal mode normally performs a two part function. It is an input device that transmits information entered through the keyboard to a host computer, and it is simultaneously an output device that displays the received data from the host computer on the video screen.

This appendix discusses data flow between the VT180 and a remote host computer only when it is operated in terminal mode. When the VT180 is operated in personal computer mode, the terminal is disconnected from the host computer and it runs under control of the internal computer and the CP/M operating program. Programming information for the VT180 in personal computer mode is described in the *VT180 User's Guide* (AA-M044A-TV).

Included in this discussion are the codes generated by the keyboard, the transmission protocol followed by the terminal, and the actions and reactions of the terminal to control codes and escape sequences in both ANSI and VT52 modes of operation.

The VT180 is an upward and downward software compatible terminal; that is, previous Digital video terminals have Digital private standards for control sequences. The American National Standards Institute (ANSI) has since standardized escape and control sequences in terminals. These standards appear in documents X3.41–1974 and X3.64–1977. ANSI standards allow the manufacturer flexibility in implementing each function. This appendix describes how the VT180 responds to the implemented ANSI control functions.

The VT180 is compatible with both the previous Digital standard and ANSI standards. Customers may use existing Digital software designed around the VT52, VT100, or the new CP/M software. The VT180 has a VT52 compatible mode in which the VT180 responds to escape sequences like a VT52. In this mode, most of the new VT180 features cannot be used.

Throughout this discussion references are made to VT52 mode or ANSI mode. These two terms indicate the VT180's software compatibility. All new software should be designed around the ANSI mode. Future Digital video terminals will not necessarily be committed to VT52 compatibility.

A.2 VT180 KEYBOARD
The VT180 keyboard has a key arrangement similar to an ordinary office typewriter. In addition to the standard typewriter keys, the VT180 has keys and indicators that generate escape and control sequences, cursor control commands, and current terminal status.

The operator uses the keyboard to transmit codes to the host. Some keys transmit one or more codes to the host immediately when typed. Other keys, such as CTRL and SHIFT do not transmit codes when typed but modify the codes transmitted by other keys. The code-transmitting keys cause the terminal to make a clicking sound to verify to the operator that the keystroke has been processed by the terminal. If two code-transmitting keys are pressed together, two codes will be transmitted according to the order in which the keys were typed. The terminal does not wait for the keys to be lifted but transmits both codes as soon as possible after the keys are first typed. If three such keys are pressed simultaneously, the codes for the first two keys are transmitted immediately; the code for the third is transmitted when one of the first two keys is lifted.

A.2.1 LED Indicators

The keyboard has seven light emitting diodes (LEDs), two of which are committed to the complementary on-line/local function. If the keyboard is connected and power is on, one of the two LEDs is on.

A third LED indicates a keyboard locked condition. In this condition the keyboard has been turned off automatically by the terminal due to a full buffer or by the host through the transmission of an XOFF to the terminal.

The four remaining LEDs are programmable and can be assigned any meaning for specific applications. The code sequences to turn these LEDs on or off are discussed later.

A.2.2 SET-UP Key

The SET-UP key is at the upper-left corner of the main key array. Operations performed in set-up mode can be stored in nonvolatile memory (NVR) so that turning terminal power off does not, by itself, alter the terminal configuration.

The procedures to change the set-up features are provided in Chapter 2 of this manual. Set-up features that may be modified by the host are listed in Table A-1 and described in detail under the control sequences.

A.2.3 Alphabetic Keys

The VT180 transmits lowercase code unless either or both SHIFT keys are down, or unless the CAPS LOCK key is down. Pressing CAPS LOCK locks only the 26 alphabetic keys in the shifted (uppercase) mode. Table A-2 shows the codes generated by the alphabetic keys.

Table A-1 Set-Up Features and Machine States

Set-Up Feature or Machine State	Changeable from Host Computer*	Saved in NVR and Changeable in Set-Up
Alternate keypad mode	Yes(DECKPAM/DECKPNM)	No
ANSI/VT52	Yes(DECANM)	Yes
Auto repeat	Yes(DECARM)	Yes
AUTO XON XOFF	No	Yes
Bits per character	No	Yes
Characters per line	Yes(DECCOLM)	Yes
Cursor	No	Yes
Cursor key mode	Yes(DECCKM)	No
Graphics mode	Yes(DECGON/DECGOFF)	No
Interlace	Yes(DECINLM)	Yes
New line	Yes(LNM)	Yes
Keyclick	No	Yes
Margin bell	No	Yes
Origin mode	Yes(DECOM)	No
Parity	No	Yes
Parity sense	No	Yes
Power	No	Yes
Receive speed	No	Yes
Screen	Yes(DECSCNM)	Yes
Scroll	Yes(DECSCLM)	Yes
Tabs	Yes(HTS/TBC)	Yes
Transmit speed	No	Yes
Wraparound	Yes(DECAWM)	Yes
# £ 3 (shifted)	Yes	Yes

*The appropriate control or escape sequence mnemonic is indicated in parentheses.

Table A-2 Alphabetic Key Codes (Octal)

Key	Upper-case	Lower-case
A	101	141
B	102	142
C	103	143
D	104	144
E	105	145
F	106	146
G	107	147
H	110	150
I	111	151
J	112	152
K	113	153
L	114	154
M	115	155
N	116	156
O	117	157
P	120	160
Q	121	161
R	122	162
S	123	163
T	124	164
U	125	165
V	126	166
W	127	167
X	130	170
Y	131	171
Z	132	172

A.2.4 Nonalphabetic Keys

Each nonalphabetic key can generate two different codes. One code is generated if neither SHIFT key is pressed. The other code is generated if either or both SHIFT keys are down. Unlike the shift lock key of a typewriter, the CAPS LOCK key does not affect these keys; it affects only the alphabetic keys. Table A-3 shows the nonalphabetic keys and the codes they generate.

Table A-3 Nonalphabetic Key Codes (Octal)

Lower-case	Neither SHIFT Key Down (Octal)	Upper-case	Either or Both SHIFT Keys Down (Octal)
1	061	!	041
2	062	@	100
3	063	# or £	043
4	064	$	044
5	065	%	045
6	066		136
7	067	&	046
8	070	*	052
9	071	(	050
0	060	)	051
–	055	—	137
=	075	+	053
[	133	{	173
:	073	:	072
’	047	“	042
,	054	<	074
.	056	>	076
/	057	?	077
\	134	|	174
`	140	~	176
]	135	}	175

A.2.5 Function Keys

Several keys on the keyboard transmit control codes. Control codes do not produce displayable characters but are codes for functions. If these codes are received by the terminal, the VT180 performs the associated function shown in Table A-4.

Table A-4 Function Key Codes

Key	Octal Value of Code Sent or Received by VT180	Action Terminal Would Take if Host Sent That Code
RETURN*	015	Carriage return function.
LINE FEED	012	Line feed.
BACKSPACE	010	Backspace function.
TAB	011	Tab function.
SPACE BAR	040	Deposit a space on the screen erasing what was there before.
ESC	033	The initial delimiter of an escape sequence. Interpret the following character string from the host as a command, rather than displaying it.
DELETE	177	Ignored by the VT180.

* The RETURN key can be redefined so that it issues 015, 012 (octal) (carriage return, line feed). The new line feature in set-up mode provides this capability.

A.2.6 NO SCROLL

When NO SCROLL is pressed it generates a single XOFF code and inhibits further scrolling. When pressed again the same key generates XON. In practice, if the software recognizes XOFF, the host stops transmitting until NO SCROLL is pressed again to allow scrolling. If the XOFF/XON feature is disabled (set-up function) NO SCROLL causes no action.

A.2.7 BREAK

Pressing BREAK forces the transmission line to its space state for 0.2333 seconds ±10 percent. If either SHIFT key is down, the time increases to 3.5 seconds ±10 percent.

SHIFT and BREAK pressed together provide the long break disconnect function. Used with properly configured modems with RS232-C levels, it disconnects both the local and remote data sets.

CTRL and BREAK pressed together cause the transmission of the answerback message.

BREAK does not function when the VT180 is in local mode.

A.2.8 CTRL (Control)

CTRL is used in conjunction with other keys on the keyboard to generate control codes. If CTRL is held down when any of the keys in Table A-5 are pressed, the code actually transmitted is in the range 000_8–037_8.

Table A-5 Control Codes Generated

Key Pressed with CTRL Key Down (Shifted or Unshifted)	Octal Code Transmitted	Function Mnemonic
Space Bar	000	NUL
A	001	SOH
B	002	STX
C	003	ETX
D	004	EOT
E	005	ENQ
F	006	ACK
G	007	BELL
H	010	BS
I	011	HT
J	012	LF
K	013	VT
L	014	FF
M	015	CR
N	016	SO
O	017	SI
P	020	DLE
Q	021	DC1 or XON
R	022	DC2
S	023	DC3 or XOFF
T	024	DC4
U	025	NAK
V	026	SYN
W	027	ETB
X	030	CAN
Y	031	EM
Z	032	SUB
[	033	ESC
\	034	FS
]	035	GS
~	036	RS
?	037	US

A.2.9 Auto Repeating

All keys auto repeat except SET-UP, ESC, NO SCROLL, TAB, RETURN, and any key pressed with CTRL. Auto repeating may be disabled (set-up function). Auto repeating works as follows. When a key is pressed, its code(s) is sent once, immediately. If the key is held down for more than one-half second, the code(s) is sent repeatedly at a rate of approximately 30 Hz (less if low transmit baud rates are used) until the key is released.

A.2.10 Cursor Control Keys

The keyboard contains four keys labeled with arrows in each of four directions. These keys transmit escape sequences. If the host echoes these escape sequences back to the terminal, the cursor moves one character up, down, right, or left. Table A-6 shows the escape sequences generated by each key.

Table A-6 Cursor Control Key Codes

Cursor Key	VT52 Mode	ANSI Mode and Cursor Key Mode Reset	ANSI Mode and Cursor Key Mode Set
Up	ESC A	ESC [A	ESC O A
Down	ESC B	ESC [B	ESC O B
Right	ESC C	ESC [C	ESC O C
Left	ESC D	ESC [D	ESC O D

A.2.11 Auxiliary Keypad

The keys on the auxiliary keypad normally transmit codes for the numerals, decimal point, minus sign, and comma. ENTER transmits the same code as RETURN. The host cannot tell if these keys were pressed on the auxiliary keypad or on the main keyboard. Therefore, software that requires considerable numeric data entry need not be rewritten to use the keypad.

However, if software must distinguish between pressing a key on the auxiliary keypad and pressing the corresponding key on the main keyboard, the host can give the terminal a command to place it in keypad application mode. In keypad application mode all keys on the auxiliary keypad are defined to give escape sequences that may be used by the host as user-defined functions.

The codes sent by the auxiliary keypad for the four combinations of the VT52/ANSI mode and keypad numeric/application mode are shown in Tables A-7 and A-8. None of the keys are affected by pressing SHIFT, CAPS LOCK, or CTRL.

NOTE

In ANSI mode, if the codes are echoed back to the VT180 or if the terminal is in local mode, the last character of the sequence is displayed on the screen; that is, PF1 displays a P.

Table A-7 VT52 Mode Auxiliary Keypad Codes

Key	Numeric Mode	Application Mode
0	0	ESC ? p
1	1	ESC ? q
2	2	ESC ? r
3	3	ESC ? s
4	4	ESC ? t
5	5	ESC ? u
6	6	ESC ? v
7	7	ESC ? w
8	8	ESC ? x
9	9	ESC ? y
-	-	ESC ? m
,	,	ESC ? l
.	.	ESC ? n
ENTER	Same as RETURN key	ESC ? M
PF1	ESC P	ESC P
PF2	ESC Q	ESC Q
PF3	ESC R	ESC R
PF4	ESC S	ESC S

Table A-8 ANSI Mode Auxiliary Keypad Codes

Key	Numeric Mode	Application Mode
0	0	ESC O p
1	1	ESC O q
2	2	ESC O r
3	3	ESC O s
4	4	ESC O t
5	5	ESC O u
6	6	ESC O v
7	7	ESC O w
8	8	ESC O x
9	9	ESC O y
-	-	ESC O m
,	,	ESC O l
.	.	ESC O n
ENTER	Same as RETURN key	ESC O M
PF1	ESC O P	ESC O P
PF2	ESC O Q	ESC O Q
PF3	ESC O R	ESC O R
PF4	ESC O S	ESC O S

A.3 TERMINAL CONTROL COMMANDS

The VT180 has many control commands that cause it to take action other than displaying a character on the screen. In this way, the host commands the terminal to move the cursor, change modes, ring the bell, etc. The following paragraphs discuss terminal control commands.

A.3.1 Control Characters

Control characters have values of 000_8–037_8 and 177_8. The control characters recognized by the VT180 are shown in Table A-9. All other control codes cause no action to be taken.

Table A-9 Control Characters

Control Character	Octal Code	Action Taken
NUL	000	Ignored on input (not stored in input buffer; see full-duplex protocol).
ENQ	005	Transmit the answerback message.
BEL	007	Sound the bell tone from keyboard.
BS	010	Move the cursor left one character position unless it is at the left margin in which case no action occurs.
HT	011	Move the cursor to the next tab stop or to the right margin if no further tab stops are present on-line.
LF	012	Causes line feed or new line operation (see new line mode).
VT	013	Interpreted as LF.
FF	014	Interpreted as LF.
CR	015	Move the cursor to the left margin on the current line.
SO	016	Select the G1 character set, as selected by the ESC) sequence.
SI	017	Select G0 character set, as selected by the ESC(sequence.
XON	021	Causes the terminal to resume transmission.
XOFF	023	Causes the terminal to stop transmitting all codes except XOFF and XON.
CAN	030	If sent during an escape or control sequence, the sequence is immediately terminated and not executed. It also causes the error character to be displayed.
SUB	032	Interpreted as CAN.
ESC	033	Introduces an escape sequence.
DEL	177	Ignored on input (not stored in the input buffer).

Control characters (codes 0_8 to 37_8 inclusive) are specifically excluded from the control sequence syntax but may be embedded within a control sequence. Embedded control characters are executed as soon as they are encountered by the VT180. The processing of the control sequence then continues with the next character received. If the character ESC occurs, the current control sequence is aborted, and a new one commences beginning with the ESC just received. If the character CAN (30_8) or the character SUB (32_8) occurs, the current control sequence is aborted. The ability to embed control characters allows the synchronization characters XON and XOFF to be interpreted properly without affecting the control sequence.

A.3.2 ANSI Control Sequences

All of the following escape and control sequences are transmitted from the host computer to the VT180 unless otherwise noted. All of the control sequences are a subset of those specified in ANSI X-3.64 1977 and ANSI X-3.41 1974.

CPR Cursor Position Report – VT180 to Host
Format: ESC [Pn; Pn R **Default value: 1**
The CPR sequence reports the active position by means of the parameters. This sequence has two parameter values, the first specifying the line and the second specifying the column. The default condition with no parameters present or parameters of zero is equivalent to a cursor at home position. Numbering of lines depends on the state of the origin mode (DECOM). This control sequence is solicited by a device status report (DSR) sent from the host.

CUB Cursor Backward – Host to VT180 and VT180 to Host
Editor Function; format: ESC [Pn D **Default value: 1**
The CUB sequence moves the active position to the left. The parameter determines the distance moved. If the parameter value is zero or one, the active position moves one position to the left. If the parameter value is n, the active position moves n positions to the left. If an attempt is made to move the cursor to the left of the left margin, the cursor stops at the left margin.

CUD Cursor Down – Host to VT180 and VT180 to Host
Editor Function; format: ESC [Pn B **Default value: 1**
The CUD sequence moves the active position downward without altering the column position. The parameter determines the number of lines moved. If the parameter value is zero or one, the active position moves one line downward. If the parameter value is n, the active position moves n lines downward. If an attempt is made to move the cursor below the bottom margin, the cursor stops at the bottom margin.

CUF Cursor Forward – Host to VT180 and VT180 to Host
Editor Function; format: ESC [Pn C **Default value: 1**
The CUF sequence moves the active position to the right. The parameter determines the distance moved. A parameter value of zero or one moves the active position one position to the right. A parameter value of n moves the active position n positions to the right. If an attempt is made to move the cursor to the right of the right margin, the cursor stops at the right margin.

CUP Cursor Position
Editor Function; format: ESC [Pn; Pn H **Default value: 1**
The CUP sequence moves the active position to the position specified by the parameters. This sequence has two parameter values, the first specifying the line position and the second specifying the column position. A parameter value of zero or one for the first or second parameter moves the active position to the first line or column in the display, respectively. The default condition with no parameters present is equivalent to a cursor to home action. In the VT180, this control behaves identically with its format effector counterpart, HVP. The numbering of lines depends on the state of the origin mode (DECOM).

CUU Cursor Up – Host to VT180 and VT180 to Host
Editor Function; format: ESC [Pn A **Default value: 1**
This sequence moves the active position upward without altering the column position. The parameter determines the number of lines moved. A parameter value of zero or one moves the active position one line upward. A parameter value of n moves the active position n lines upward. If an attempt is made to move the cursor above the top margin, the cursor stops at the top margin.

DA Device Attributes
Format: ESC [Pn c **Default value: 0**
The host requests the VT180 to send a device attributes (DA) control sequence to identify itself by sending the DA control sequence with either no parameter or a parameter of zero. Response to this request (VT180 to host) is generated by the VT180 as a DA control sequence with the numeric parameters as shown in Table A-10.

Table A-10 DA Control Sequences

Option Present	Sequence Sent
No options	ESC [?1;0c
Processor option (STP)	ESC [?1;1c
Advanced video option (AVO)	ESC [?1;2c
AVO and STP	ESC [?1;3c

DECALN Screen Alignment Display (Digital Private)
Format: ESC #8
This command fills the entire screen area with uppercase Es for screen focus and alignment. This command is used by Digital manufacturing and Field Service personnel.

DECANM ANSI/VT52 Mode (Digital Private)
This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes only VT52 compatible escape sequences to be interpreted and executed. The set state causes only ANSI compatible escape and control sequences to be interpreted and executed.

DECARM Auto Repeat Mode (Digital Private)
This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes no keyboard keys to auto repeat. The set state causes certain keyboard keys to auto repeat.

DECAWM Auto Wrap Mode (Digital Private)
This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes any displayable characters received when the cursor is at the right margin to replace any previous characters there. The set state causes these characters to advance to the start of the next line, doing a scroll up if required and permitted.

DECCOLM Column Mode (Digital Private)
This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes a maximum of 80 columns on the screen. The set state causes a maximum of 132 columns on the screen.

DECCKM Cursor Keys Mode (Digital Private)
This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. This mode is only effective when the terminal is in keypad application mode (see DECKPAM) and the ANSI/VT52 mode (DECANM) is set (see DECANM). Under these conditions, if the cursor key mode is reset, the four cursor function keys send ANSI cursor control commands. If cursor key mode is set, the four cursor function keys send application functions.

DECDHL Double-Height Line (Digital Private)
Format: Top Half: ESC #3, Bottom Half: ESC #4
These sequences cause the line containing the active position to become the top or bottom half of a double-height, double-width line. The sequences must be used in pairs on adjacent lines and the same character output must be sent to both lines to form full double-height characters. If the line was single-width, single-height, all characters to the right of the center of the screen are lost. The cursor remains over the same character position unless it would be to the right of the right margin, in which case it is moved to the right margin.

DECDWL Double-Width Line (Digital Private)
Format: ESC #6
This sequence causes the line that contains the active position to become double-width, single-height. If the line was single-width, single-height, all characters to the right of screen center are lost. The cursor remains over the same character position unless it would be to the right of the right margin, in which case it is moved to the right margin.

DECHCP Hard Copy (Digital Private)
Format: ESC #7
This sequence causes the screen to cease updating and freeze while the hard copy output is enabled. The screen resumes normal operation when the hard copy has been completed. This command is ignored if no hard copy option is installed.

DECID Identify Terminal (Digital Private)
Format: ESC Z
This sequence causes the same response as the ANSI device attributes (DA). DECID will not be supported in future Digital terminals; therefore, DA should be used by any new software.

DECINLM Interlace Mode (Digital Private)
This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state (noninterlace) causes the video processor to display 240 scan lines per frame. The set state (interlace) causes the video processor to display 480 scan lines per frame. There is no increase in character resolution.

DECKPAM Keypad Application Mode (Digital Private)
Format: ESC =
Auxiliary keypad keys and cursor control keys transmit escape sequences.

DECKPNM Keypad Numeric Mode (Digital Private)
Format: ESC >
Auxiliary keypad keys send ASCII codes corresponding to the characters on the keys. Cursor control keys send cursor controls.

DECLL Load LEDs (Digital Private)
Format: ESC [Ps q **Default value: 0**
Load the four programmable LEDs on the keyboard according to the parameter(s) shown in Table A-11. LED numbers are indicated on the keyboard.

Table A-11 Load LEDs Parameters

Parameter	Meaning
0	Clear LEDs 1 through 4
1	Light LED 1
2	Light LED 2
3	Light LED 3
4	Light LED 4

DECOM Origin Mode (Digital Private)
This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes the origin to be at the upper-left character position on the screen. Line numbers are therefore independent of current margin settings. The cursor may be positioned outside the margins with a cursor position (CUP) or horizontal and vertical position (HVP) control.

The set state causes the origin to be at the upper-left character position within the margins. Line numbers are therefore relative to the current margin settings. The cursor cannot be positioned outside the margins.

The cursor moves to the new home position when this mode is set or reset. Lines and columns are numbered consecutively, with the origin being line 1, column 1.

DECRC Restore Cursor (Digital Private)
Format: ESC 8
This sequence causes the previously saved cursor position, graphic rendition, and character set to be restored.

DECREPTPARM Report Terminal Parameters
Format: ESC [<sol>; <par>; <nbits>; <xspeed>; <rspeed>; <clkmul>; <flags>x
These sequence parameters are explained below in the DECREQTPARM sequence.

DECREQTPARM Request Terminal Parameters
Format: ESC [<sol>x
This sequence is sent by the terminal controller to notify the host of the status of selected terminal parameters. The status sequence may be sent when requested by the host or at the terminal's discretion. DECREPTPARM is sent upon receipt of a DECREQTPARM.

The meanings of the DECREQTPARM sequence parameters are shown in Table A-12.

DECSC Save Cursor (Digital Private)
Format: ESC 7
This sequence causes the cursor position, graphic rendition, and character set to be saved. (See DECRC.)

DECSCLM Scrolling Mode (Digital Private)
This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes scrolls to jump instantaneously. The set state causes scrolls to be smooth at a maximum rate of six lines per second.

Table A-12 DECREQTPARM Sequence Parameters

Parameter	Value	Meaning
<sol>	0 or none	This message is a request (DECREQTPARM). The terminal is allowed to send unsolicited reports.
	1	This message is a request. From now on the terminal may only report in response to a request.
	2	This message is a report (DECREPTPARM).
	3	This message is a report and the terminal is only reporting on request.
<par>	1	No parity is set.
	4	Parity is set and odd.
	5	Parity is set and even.
<nbits>	1	Eight bits per character.
	2	Seven bits per character.
<xspeed>		Bits per second
<rspeed>	0	50
	8	75
	16	110
	24	134.5
	32	150
	40	200
	48	300
	56	600
	64	1200
	72	1800
	80	2000
	88	2400
	96	3600
	104	4800
	112	9600
	120	19,200
<clkmul>	1	The bit rate multiplier is 16.
<flags>	0–15	This value communicates the four switch values in block 5 of SET-UP B, which are only visible to the user when an STP option is installed. These bits may be assigned for an STP device. The four bits are a decimal-encoded binary number.

DECSCNM Screen Mode (Digital Private)
This is a private parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes the screen to be black with white characters. The set state causes the screen to be white with black characters.

DECSTBM Set Top and Bottom Margins (Digital Private)
Format: ESC [Pn; Pn r **Default values: (See the following paragraph.)**
This sequence sets the top and bottom margins to define the scrolling region. The first parameter is the line number of the first line in the scrolling region. The second parameter is the line number of the bottom line in the scrolling region. Default is the entire screen (no margins). The minimum size of the scrolling region allowed is two lines, that is, the top margin must be less than the bottom margin.

DECSWL Single-Width Line (Digital Private)
Format: ESC #5
This causes the line that contains the active position to become single-width, single-height. The cursor remains on the same character position. This is the default condition for all new lines on the screen.

DECTST Invoke Confidence Test
Format: ESC [2 ; Ps y
Ps is the parameter indicating the test to be done. Ps is computed by taking the weight indicated for each desired test and adding them together. Table A-13 gives the test weights. If Ps is 0 no test is performed but the VT180 is reset.

Table A-13 DECTST Test Weights

Test	Weight
Power-up self-test (ROM checksum, RAM, NVR, keyboard, and AVO if installed)	1
Data loopback	2 (loopback connector required)
Repeat selected test(s) indefinitely (until failure or power-off)	8

DSR Device Status Report
Format: ESC [Ps r **Default value: 0**
This sequence requests and reports the general status of the VT180 according to the parameter(s) in Table A-14. DSR with a parameter value of 0 or 3 is always sent as a response to a requesting DSR with a parameter value of 5.

Table A-14 Device Status Report Parameters

Parameter	Meaning
0	Response from VT180 – Ready, no malfunctions detected (default).
3	Response from VT180 – Malfunction, retry.
5	Command from host – Please report status (using a DSR control sequence).
6	Command from host – Please report active position (using a CPR control sequence).

ED Erase In Display
Editor Function; format: ESC [Ps J **Default value: 0**
This sequence erases some or all characters in the display according to the parameter. Any complete line erased by this sequence returns that line to single-width mode. Table A-15 shows the erase in display parameters.

Table A-15 Erase In Display Parameters

Parameter	Meaning
0	Erase from the active position to the end of the screen, inclusive (default).
1	Erase from start of the screen to the active position, inclusive.
2	Erase all of the display. All lines are erased, changed to single-width, and the cursor does not move.

EL Erase In Line
Editor Function; format: ESC [Ps K **Default value: 0**
Erases some or all characters in the active line according to the parameters in Table A-16.

Table A-16 Erase In Line Parameters

Parameter	Meaning
0	Erase from the active position to the end of the line, inclusive (default).
1	Erase from the start of the screen to the active position, inclusive.
2	Erase all of the line, inclusive.

HTS Horizontal Tabulation Set
Format Effector; format: ESC H
Set one horizontal stop at the active position.

HVP Horizontal and Vertical Position
Format Effector; format: ESC [Pn; Pn f **Default value: 1**
This sequence moves the active position to the position specified by the parameters. This sequence has two parameter values; the first specifies the line position, the second specifies the column. A parameter value of either zero or one causes the active position to move to the first line or column in the display, respectively. The default condition with no parameters present moves the active position to the home position. In the VT180, this control behaves identically with its editor function counterpart, CUP. Numbering lines and columns depends on the reset or set state of the origin mode (DECOM).

IND Index
Format Effector; format: ESC D
This sequence causes the active position to move downward one line without changing column position. If the active position is at the bottom margin, a scroll up is performed.

LNM Line Feed/New Line Mode
This is a parameter applicable to set mode (SM) and reset mode (RM) control sequences. The reset state causes the interpretation of the line feed (LF), defined in ANSI Standard X3.4-1977, to imply only vertical movement of the active position and causes the RETURN key (CR) to send the single code CR. The set state causes the LF to imply movement to the first position of the following line and causes the RETURN key to send the two codes (CR, LF). This is the new line (NL) option. This mode does not affect the index (IND) or next line (NEL) format effectors.

NEL Next Line
Format Effector; format: ESC E
This sequence causes the active position to move to the first position on the next line downward. If the active position is at the bottom margin, a scroll up is performed.

RI Reverse Index
Format Effector; format: ESC M
This sequence moves the active position to the same horizontal position on the preceding line. If the active position is at the top margin, a scroll down is performed.

RIS Reset to Initial State
Format: ESC c
Resets the VT180 to its initial state, that is, the state it has after it is powered on. This also causes the execution of the power-up self-test and signal INIT H to be asserted briefly.

RM Reset Mode
Format: ESC [Ps ;Ps ; ...; Ps l **Default value: none**
Resets one or more VT180 modes as specified by each selective parameter in the parameter string. Each mode to be reset is specified by a separate parameter. (See modes and set mode (SM) following this section.)

SCS Select Character Set
The appropriate G0 and G1 character sets are selected from the five possible character sets. G0 and G1 are selected by codes SI and SO (shift in and shift out) respectively. Table A-17 shows the character set selection.

Table A-17 Character Set Selection

G0 Sets Sequence	G1 Sets Sequence	Meaning
ESC (A	ESC) A	United Kingdom set
ESC (B	ESC) B	ASCII set
ESC (0	ESC) 0	Special graphics
ESC (1	ESC) 1	Alternate character ROM Standard character set
ESC (2	ESC) 2	Alternate character ROM Special graphics

The United Kingdom and ASCII sets conform to the ISO international register of character sets to be used with escape sequences. The other sets are private character sets. Special graphics means that the graphic characters for the codes 137_8 to 176_8 are replaced with other characters. The specified character set will be used until another SCS is received.

SGR Select Graphic Rendition
Format Effector; format: ESC [Ps; ...; Ps m **Default value: 0**
Invoke the graphic rendition specified by the parameter(s). All following characters transmitted to the VT180 are rendered according to the parameter(s) until the next occurrence of SGR. Table A-18 shows the parameters. All other parameter values are ignored.

Table A-18 Select Graphic Rendition Parameters

Parameter	Meaning
0	Attributes off
1	Bold or increased intensity
4	Underscore
5	Blink
7	Negative (reverse) image

Without the advanced video option only one character attribute is possible as determined by the cursor selection. In that case, specifying either the underscore or the reverse attribute activates the currently selected attribute.

SM Set Mode
Format: ESC [Ps; ...; Ps h **Default value: none**
Causes one or more modes to be set within the VT180 as specified by each selective parameter in the parameter string. Each mode to be set is specified by a separate parameter. A mode is considered set until it is reset by a reset mode (RM) control sequence.

TBC Tabulation Clear
Format Effector; format: ESC [Ps g **Default value: 0**
Table A-19 details the tabulation clear parameters. Any other parameter values are ignored.

Table A-19 Tabulation Clear Parameters

Parameter	Meaning
0	Clear the horizontal tab stop at the active position (the default case).
3	Clear all horizontal tab stops.

A.3.3 Modes

Table A-20 is a list of VT180 modes that may be changed with set mode (SM) and reset mode (RM) controls.

Table A-20 ANSI Specified Modes

Parameter	Mode Mnemonic	Function
0		Error (ignored)
20	LNM	Line feed new line mode

A.3.3.1 Digital Private Modes – If the first character in the parameter string is ? (77_8), the parameters are interpreted as Digital private parameters according to the modes in Table A-21. Any other parameter values are ignored.

Table A-21 Digital Private Parameter Functions

Parameter	Mode Mnemonic	Function
0		Error (ignored)
1	DECCKM	Cursor key
2	DECANM	ANSI/VT52
3	DECCOLM	Column
4	DECSCLM	Scrolling
5	DECSCNM	Screen
6	DECOM	Origin
7	DECAWM	Auto wrap
8	DECARM	Auto repeating
9	DECINLM	Interlace

A.3.3.2 ANSI Standard Modes – The modes in Table A-22, specified in ANSI X3.64-1977 standard, may be considered to be permanently set, permanently reset, or not applicable, as noted. Refer to that standard for further information concerning these modes.

Table A-22 ANSI Standard Modes

Mnemonic	Function	State
CRM	Control representation	Reset
EBM	Editing boundary	Reset
ERM	Erasure	Set
FEAM	Format effector action	Reset
FETM	Format effector transfer	Reset
GATM	Guarded area transfer	NA
HEM	Horizontal editing	NA
IRM	Insertion-replacement	Reset
KAM	Keyboard action	Reset
MATM	Multiple area transfer	NA
PUM	Positioning unit	Reset
SATM	Selected area transfer	NA
SRTM	Status reporting transfer	Reset
TSM	Tabulation stop	Reset
TTM	Transfer termination	NA
VEM	Vertical editing	NA

A.3.3.3 Valid VT52 Mode Control Sequences

Cursor Up
Format: ESC A
Move the active position upward one position without altering the horizontal position. If an attempt is made to move the cursor above the top margin, the cursor stops at the top margin.

Cursor Down
Format: ESC B
Move the active position downward one position without altering the horizontal position. If an attempt is made to move the cursor below the bottom margin, the cursor stops at the bottom margin.

Cursor Right
Format: ESC C
Move the active position to the right. If an attempt is made to move the cursor to the right of the right margin, the cursor stops at the right margin.

Cursor Left
Format: ESC D
Move the active position one position to the left. If an attempt is made to move the cursor to the left of the left margin, the cursor stops at the left margin.

Cursor to Home
Format: ESC H
Move the cursor to the home position.

Reverse Line Feed
Format: ESC I
Move the active position upward one position without altering the column position. If the active position is at the top margin, a scroll down is performed.

Erase to End of Screen
Format: ESC J
Erase all characters from the active position to the end of the screen. The active position is not changed.

Erase to End of Line
Format: ESC K
Erase all characters from the active position to the end of the current line. The active position is not changed.

Direct Cursor Address
Format: ESC Y line column
Move the cursor to the specified line and column. The line and column numbers are sent as ASCII codes whose values are the number plus 037_8. For example, 040_8 refers to the first line or column, 050_8 refers to the eighth line or column, etc.

Identify
Format: ESC Z
This causes the terminal to send its identifier escape sequence to the host. The sequence is ESC / Z.

NOTE
Information regarding options must be obtained in ANSI mode, using the device attributes (DA) control sequence.

Enter Alternate Keypad Mode
Format: ESC =
Auxiliary keypad keys send unique identifiable escape sequences for use by application programs.

Exit Alternate Keypad Mode
Format: ESC >
Auxiliary keypad keys send ASCII codes for functions or characters on the key.

Enter ANSI Mode
Format: ESC <
All subsequent escape sequences will be interpreted according to ANSI Standards X3.64-1977 and X3.41-1974. The VT52 escape sequence in this section will not be recognized.

A.4 CONTROL SEQUENCE SUMMARY (ANSI AND VT52)
The following is a summary of the control sequences that are software compatible with the VT180 when it is operated in the ANSI or VT52 mode.

A.4.1 ANSI Compatible Mode
Table A-23 gives the ANSI compatible mode sequences. Table A-24 lists the line size commands.

Table A-23 ANSI Compatible Mode Sequences

Feature	ANSI Compatible Mode Sequence
Cursor up	ESC [Pn A
Cursor down	ESC [Pn B
Cursor forward (right)	ESC [Pn C
Cursor backward (left)	ESC [Pn D
Direct cursor addressing	ESC [Pl; Pc H * or ESC [Pl; Pc f *
Index	ESC D
Reverse index	ESC M
Save cursor and attributes	ESC 7
Restore cursor and attributes	ESC 8

*Pl = Line number; Pc = Column number

NOTE

Pn refers to a decimal parameter expressed as a string of ASCII digits. Multiple parameters are separated by the semicolon character (073_8). If a parameter is omitted or specified to be 0, the default parameter value is used. For the cursor movement commands, the default parameter value is 1.

Table A-24 Line Size Commands

Command	Sequence
Change this line to double-height top half	ESC#3
Change this line to double-height bottom half	ESC#4
Change this line to single-width, single-height	ESC#5
Change this line to double-width, single-height	ESC#6

A.4.1.1 Character Attributes – The sequence is

ESC [Ps;Ps;Ps;....Ps m

Ps refers to a selective parameter. Multiple parameters are separated by the semicolon character (073_8). The parameters are executed in order. Table A-25 gives the parameter meanings. Any other parameter values are ignored.

Table A-25 Character Attribute Parameters

Parameter	Meaning
0 or none	All attributes off
1	Bold on
4	Underscore on
5	Blink on
7	Reverse video on

A.4.1.2 Erasing – Table A-26 lists the erasing sequences.

Table A-26 Erasing Sequences

Erasing Feature	Sequence
From cursor to end of line	ESC [K or ESC [O K
From beginning of line to cursor	ESC [1 K
Entire line containing cursor	ESC [2 K
From cursor to end of screen	ESC [J or ESC [O J
From beginning of screen to cursor	ESC [1 J
Entire screen	ESC [2 J

A.4.1.3 Programmable LEDs – The sequence is

ESC [Ps; Ps;...Ps q

Ps are selective parameters separated by semicolons (073_8) and executed in order, as shown in Table A-27. Any other parameter values are ignored.

Table A-27 LED Parameters

Parameter	Meaning
0 or none	All LEDs off
1	LED #1 on
2	LED #2 on
3	LED #3 on
4	LED #4 on

A.4.1.4 Character Sets (G0 and G1 Designators) – The G0 and G1 character sets are designated as seen in Table A-28.

Table A-28 Character Set Designations

Character Set	G0	G1
United Kingdom (UK)	ESC (A	ESC) A
United States (USASCII)	ESC (B	ESC) B
Alternate character ROM	ESC (1	ESC) 1

A.4.1.5 Scrolling Region – The sequence is

ESC [Pt ; Pb r

Pt is the number of the top line of the scrolling region. Pb is the number of the bottom line of the scrolling region and must be greater than Pc.

A.4.1.6 Tab Stops – Table A-29 lists the tab stop sequences.

Table A-29 Tab Stop Sequences

Feature	Sequence
Set tab at current column	ESC H
Clear tab at current column	ESC [g or ESC [0 g
Clear all tabs	ESC [3 g

A.4.1.7 Modes – Table A-30 lists the modes and sequences.

Table A-30 Mode Sequences

Mode Name	To Set Mode	Sequence	To Reset Mode	Sequence
Line feed/new line	New line	ESC [20h	Line feed	ESC [20l
Cursor key mode	Application	ESC [?1h	Cursor	ESC [?1l
ANSI/VT52	ANSI	N/A	VT52	ESC [?2l
Column mode	132 column	ESC [?3h	80 column	ESC [?3l
Scrolling mode	Smooth	ESC [?4h	Jump	ESC [?4l
Screen mode	Reverse	ESC [?5h	Normal	ESC [?5l
Origin mode	Relative	ESC [?6h	Absolute	ESC [?6l
Wraparound	On	ESC [?7h	Off	ESC [?7l
Auto repeat	On	ESC [?8h	Off	ESC [?8l
Interlace	On	ESC [?9h	Off	ESC [?9l
Keypad mode	Application	ESC =	Numeric	ESC >

A.4.1.8 Reports – The cursor position report is invoked by

ESC [6 n

The response is

ESC [Pl ; Pc R

where Pl equals line number and Pc equals column number.

Status report is invoked by

ESC [5 n

The response is

ESC [0 n (terminal ok)
ESC [3 n (terminal not ok)

A.4.1.8 What Are You – This is invoked by

ESC [c
or
ESC [O c

The response is

ESC [? 1 ; Ps c

Ps is the option present parameter with the meanings shown in Table A-31. It is alternately invoked by ESC Z (not recommended). The response is the same.

Table A-31 Option Present Parameters

Ps	Meaning
0	Base VT100, no options
1	Processor option (STP)
2	Advanced video option (AVO)
3	AVO and STP

A.4.1.9 Reset – Reset causes the power-up reset routine to be excecuted.

ESC c

A.4.1.10 Confidence Tests – The sequence to fill the screen with Es is

ESC # 8

The sequence to invoke test(s) is

ESC [2 ; Ps y

Ps is the parameter indicating the test to be done and is a decimal number computed by taking the weight indicated for each desired test and adding them together. See Table A-32.

Table A-32 Test Weights

Test	Weight
Power-up, self-test (ROM checksum, RAM, NVR, keyboard, and AVO if installed)	1
Data loopback	2 (loopback connector required)
EIA modem control test	4 (loopback connector required)
Repeat selected tests(s) indefinitely (until failure or power off)	8

A.4.2 VT52 Compatible Mode

Table A-33 gives the VT52 compatible mode sequences.

Table A-33 VT52 Compatible Mode Sequences

Feature	Sequence
Cursor up	ESC A
Cursor down	ESC B
Cursor right	ESC C
Cursor left	ESC D
Select special graphics character set	ESC F
Select ASC11 character set	ESC G
Cursor to home	ESC H
Reverse line feed	ESC I
Erase to end of screen	ESC J
Erase to end of line	ESC K
Direct cursor address	ESC Ylc*
Identify	ESC Z**
Enter alternate keypad mode	ESC =
Exit alternate keypad mode	ESC >
Enter ANSI mode	ESC <

* Line and column numbers for direct cursor address are single character codes whose values are the desired number plus 37_8. Line and column numbers start at 1.

** Response to ESC Z is ESC/Z.

APPENDIX B
VT180 RECOMMENDED SPARES LIST (RSL)

Table B-1 lists the recommended spares for the basic VT180.

Table B-1 VT180 Recommended Spares

Qty	Part Number/Description
1	30-19308-01 RX180-AB Dual Disk Drive Unit
1	70-17362-00 Monitor PCB (Elston)
1	70-17363-00 Flyback Assembly (Elston)
1	70-17364-00 CRT and Yoke Assembly
1	54-15150 VT180 Paddle Board
1	54-15152 VT180 Control Module
1	54-13009-03 Terminal Controller PCB
1	54-13384-01 Expansion Backplane
1	54-13097-00 Advanced Video PCB
1	BC26R-10 EIA Communications Cable (M-F) (10 ft)
1	BC26U-15 EIA Printer Cable (null modem) (15 ft)
1	70-15765-00 LK01 Keyboard
1	70-14652 Cable Assembly, Keyboard
1	12-15050 Speaker
1	12-14333-72 LK07 Keycap Set
1	12-14333-91 LK08 Keycap Set
1	74-16355 Keycap Removal Tool
1	70-14979 Power Supply Assembly
1	12-15232 Power Switch
1	12-16901-00 Voltage Select Switch
10	90-07217 Fuse 3 Amp*
1	17-00083-09 Line Cord, 115 V
1	17-00083-10 Line Cord, 230 V
1	70-14978-01 DC Power Distribution Cable
1	70-14978-03 DC Power Distribution Cable
6	12-12405-00 Card Guide
5	90-10007 Retainer Ring*
2	90-09257 Retaining Ring*
5	90-09747-01 Support*, Chassis
5	90-10016-00 Cable Clamp*

*These items are expendable.

Table B-1 VT180 Recommended Spares (Cont)

Qty	Part Number/Description
15	90-09964 Plunger*, Chassis Mounting
15	90-09966-01 Grommet*, Chassis
15	12-14740-00 Plunger*, Base Mounting
15	90-09965-00 Plunger*, Base Mounting
5	90-09747-03 Standoff*, AVO
15	90-09966-02 Grommet*, Base
5	12-14817 Mounting Screw*
5	90-09624-00 Feet*
1	12-12893 Fuse Holder*
5	90-09680-04 Screw*, tap 6-32 × ½ Hex
5	90-06021-01 Screw*, 6-32 × 5/16
1	94-03220-03 CRT Mask, Alignment
1	94-03270-03 CRT Mask, Character Alignment
1	29-23189-00 Shaft Extender
1	29-23190-00 Alignment Tool, Monitor
1	29-23187 Kit, Carrying Case
1	99-05812 I.C. Container
1	17-00150-01 Line Cord, Coiled
1	17-00150-02 Line Cord, Coiled
1	17-00297 BC26K Cable, Terminal-to-Disk
1	17-00298 BC26Z Cable, Disk-to-Disk
1	70-08612-OM 16-Conductor Flat Cable
1	23-061E2-00 ROM, Basic Video
1	23-032E2-00 ROM, Basic Video
1	23-033E2-00 ROM, Basic Video
1	23-034E2-00 ROM, Basic Video
1	23-017E3-00 ROM1, VT18X Control Module
1	23-021E3-00 ROM0, VT18X Control Module
4	90-00001-12 Standoff* 6-32
4	90-06970-00 Spacer, Fiber*
1	90-06706-00 Washer, Nylon Flat*
4	90-06013-01 Screw*, 4-40 × ½
4	90-06557-00 Kep Nut*, 4-40
1	90-08301-01 Screw*, 4-40 × ½

*These items are expendable.

APPENDIX C
GLOSSARY OF TERMS AND ABBREVIATIONS

75 ohm – Source and terminating impedance for video inputs and outputs.

7FH – Hexadecimal value representing 0111 1111 in binary; the terminator at the end of each line of characters; also, the last keyboard address, always returned at the end of a scan.

8080 – The microprocessor device on the terminal controller module.

8224 – The clock generator device.

8228 – The system controller and bus driver device.

8251 – The PUSART.

A0,A1,...,Ax – Address bus.

Active position – The active column and active line position in which the next displayable character will be placed. The active line is the line in which the cursor is presently located. The active column is the cursor location on the active line.

ADDR – Address.

ADDR CNT – Address count. The signal that drives the address counters in the video processor.

ADDR CNT ON – Address count on. The signal inside the DC011 that controls the output of address count signals.

ADDR LD – Address load. The signal that loads the address bytes from the end of a line into the presettable address counters; it also stores line attributes.

Advanced video option – An optional circuit board that contains extra screen RAM, extra attribute RAM, and program ROM sockets and decoders.

ALT CHAR SET – Alternate character set. If the AVO is present, a ROM with a different character set can be installed in a socket on the terminal controller and selected with a control function.

ALU – Arithmetic logic unit.

ANSI – American National Standards Institute.

ANSI mode – A mode in which the terminal recognizes and responds only to control functions whose syntax and meaning follow ANSI specifications.

ASCII – American Standards Committee for Information Interchange, standard code in which each character is represented by a 7- or 8-bit code.

Asynchronous – For serial data transmission, a method that allows sender and receiver to operate with nonidentical clocks.

Attribute – A display feature such as blinking characters, double-width lines, or reverse screen.

AVO – Advanced video option.

Base attribute – The one attribute that characters on the screen can have when the AVO is not present. Selectable at set-up to be either reverse or underline.

Baud rate – The rate of data exchange on a serial interface.

Bipolar – A kind of transistor construction used in TTL and high speed LSI.

Blink – An attribute that makes a character blink.

Bold – An attribute that makes a character brighter.

Bottom half – In a double-height line, this is asserted for the bottom half of the line.

Bus – A group of wires carrying several separate but related signals.

Byte – Eight bits treated as a unit.

C/D – Command/data.

Caps lock – A key that forces alphabetics to uppercase without affecting numeric and symbolic keys.

CAS – Column address strobe.

Cathode – The element that is driven to control intensity of the electron beam in the CRT.

CHAR CLK – Character clock. A clock in the video processor with a period equal to the time between characters on the display. It varies according to 80- or 132-column mode.

Character – A pattern of dots on the CRT screen representing an ASCII character; a pattern that represents an element of written language or mathematics; a group of seven or eight bits representing a control or graphic entity. In serial-by-bit transmission, a character is transferred from low-order bit to high-order bit.

Character generator – A ROM that translates character codes into patterns for display.

Character position – That portion of a visual display that is displaying or is capable of displaying a graphic symbol.

Checksum – A number created specifically to detect errors in stored or exchanged data.

Column mode – The number of character positions provided on a line; 80 or 132.

COM RXC – Communication receiver clock from the terminal controller baud rate generator.

COM TXC – Communication transmitter clock from the terminal controller baud rate generator.

COMP SYNC – Composite sync signal.

Composite sync – The signal that coordinates the motion of the electron beam in a video monitor that is external to the VT180.

CON CLK – The console operating clock from the video processor in the terminal controller module.

CON DTR – The console data terminal ready signal from the terminal controller PUSART.

CON REC DATA – The console received data from terminal controller PUSART.

CON XMIT DATA – Console transmitted data to the terminal controller PUSART.

Control – The term control refers to a control function. A control function is implemented through the use of a control character, escape sequence, control sequence, or control string.

Control (key) – Produces control characters when pressed with other keys.

Control chip – The DC012.

Control character – A single character whose occurrence in a particular context initiates, modifies, or stops a control function. The value of a control character ranges from 0 to 37_8 using 7-bit characters. The delete character (177_8) is also a control character.

Control function – A special action the terminal can perform to affect recording, processing, transmitting, or interpreting data. A control function refers to a control character, an escape sequence, a control sequence, or a control string.

Control Q – An ASCII control character meaning XON.

Control S – An ASCII control character meaning XOFF.

Control sequence – A sequence of characters used for control purposes to perform a control function, which begins with the control sequence introducer (CSI) and ends with the first occurrence of a final character (100_8–176_8). A control sequence may contain one or more parameter characters (060–077_8) and/or intermediate characters (040–057_8).

Control sequence introducer – A prefix to a control sequence that provides supplementary control functions. The CSI for the VT180 series is ESC [or 033_8 133_8.

Control string – A control function with an opening and closing delimiter control character. Control strings are not used in the VT180.

CP/M – A control program for microprocessors. The program used as the operating system by the Z80A.

CPU – Central processing unit.

CRT – Cathode ray tube. The display device in a monitor.

CPU ZRFSH – RAM refresh signal from the Z80A.

CRC – Cyclic redundancy check.

CSI – Control sequence introducer

Cursor – A visual representation of the active position, which is either a blinking reverse-video or blinking underline.

Cursor control – An editor function that moves the active position.

D0,D1,...,Dx – Individual lines on the data bus.

DB bus – The bidirectionally buffered data bus.

DC011 – A timing chip for the video processor. It produces timing signals, clocks, and line buffer addressing.

DC012 – The control chip for the video processor. It controls DMAs and the generation of character video.

DCA – Direct cursor addressing.

DDEN – Double-density.

Default – The value that is assumed by a program when the user does not supply a specific value.

Demultiplexer – Routes a signal to one of several outputs according to control signals.

DH – Double-height.

DIRC – Direction.

Display – The current active area of the screen, that is, the area inside the scrolling region or the entire screen, depending on the origin mode.

Direct drive – This controls movement of an electron beam in the CRT with separate horizontal and vertical signals rather than combining the control signals into the single composite video signal.

Direct memory access – An action by which the video processor can read data directly from the microprocessor's memory.

DMA – Direct memory access.

DMA ENABLE – A signal allowing a DMA to occur.

DO bus – The buffered, write-only (output-only) data bus.

Dot – The smallest displayable unit of information on the screen.

DOT CLK – The fastest clock in the video processor; it clocks the video shift register. It varies with 80- or 132-column mode.

Dot stretcher – In the DC012, this adds one dot to each row of contiguous dots. It ensures that the bandwidth requirement of the CRT is met.

Double-height – This makes each line display in 20 scans instead of the regular 10.

Double-width – This makes each character display in 20 dots instead of the regular 10.

DRQ – Data request.

DSR – Data set ready.

DTR – Data terminal ready.

DW – Double-width.

EAROM – Electrically alterable read-only memory; the NVR.

Editor function – A control that affects the layout or positioning of previously entered or received information in a printing or cathode ray tube device and that is intended to be interpreted and executed without remaining in the data stream. (See format effector.)

EIA – The Electronic Industries Association; in reference to the EIA standard voltage I/O interface, RS-232-C.

ER1400 – Nonvolatile RAM.

ESC – Escape character (ASCII 033_8).

Escape – A control character ESC (033_8) that provides supplementary characters or code extensions. ESC introduces a control or an escape sequence.

Escape sequence – A sequence of characters that performs a control function. The sequence begins with ESC and ends with the first occurrence of a final character ($060–176_8$). An escape sequence may also have one or more intermediate characters ($040–057_8$).

Exclusive-OR – A logical function that provides an output only when one or the other input signal is present but not when both or neither are present.

EXT – External.

Field – That part of a video image displayed during one vertical sweep of the CRT beam from the top of the screen to the bottom.

Fill line – A terminator and a pair of address bytes. Synchronizes the DMA process in the video processor without requiring a full line of memory.

Firmware – A computer program (software) that is implemented in hardware, such as read-only memory.

Flag – An internal signal to the microprocessor.

Flyback transformer – This generates high voltages in the CRT monitor.

Format effector – A control that affects the layout or positioning of information on the screen and that may remain in the data stream subsequent to interpretation and processing. (See editor function.)

Frame – A complete video image.

Full-duplex – A communication channel that can simultaneously and independently transmit and receive data.

Graphic character – A character, other than a control character, that has a visual representation normally handwritten, printed, or displayed.

Half-duplex – A communication channel that can receive and transmit but cannot do both simultaneously.

Halt – A condition in the microprocessor when no instructions are performed.

Hard copy – Computer output that can be carried away from the output device in human-readable form.

Hardware – The electrical and mechanical structure of a device.

Hex – Hexidecimal number system.

HLT – Head load timing.

HOLD REQ – Hold request. A signal asking the microprocessor to give up use of the address, data, and control buses to the video processor.

HORIZ BLANK – Horizontal blank. A signal that turns the electron beam off during the horizontal retrace interval.

HORIZ DRIVE – Horizontal drive. A direct drive signal from the video processor that synchronizes horizontal deflection in the internal monitor.

HORIZONTAL TIME – The gating signal inside the DC012.

Host – The computer that the VT180 communicates with.

Hysteresis – A characteristic of detection circuits that makes the threshold of detection different for different directions of change of the input signal.

IOASEL – Input/output address select.

I/O RD – Input/output read. A microprocessor control bus signal.

I/O WR – Input/output write. A microprocessor control bus signal.

IC – Integrated circuit.

Idle – On a communication line, a state when no information is being exchanged.

INIT – Initialize. The signal that informs options and internal devices that the VT180 has performed a reset operation.

INTA – Interrupt acknowledge. The signal the 8080 produces to indicate it is ready for a RST instruction containing an interrupt vector. The signal enables the outputs on the interrupt vector buffer.

MEM DISABLE – Memory disable. The signal used by the AVO to disable main memory outputs when other memory is being addressed.

MEM RD – Memory read. A microprocessor control bus signal.

MEM WR – Memory write. A microprocessor control bus signal.

MFM – Modified frequency modulated.

MFU – Multifrequency unit.

Microprocessor – The 8080 and associated devices that control the VT180, and the Z80A that controls operation of the CP/M processor module.

MNOS – Metal nitride oxide semiconductor. The semiconductor technology used in the nonvolatile RAM.

Mode instruction – The command to the PUSART that sets up the basic operating protocol.

Modem – A device that converts the VT180's EIA output to audio tones that can pass over telephone lines.

Modulus – The largest unique value in a counter. If incremented beyond its modulus, a counter returns to zero and counts up again.

MOS – Metal oxide semiconductor. A class of devices distinct from bipolar.

MREQ – Memory request.

ms – Millisecond.

Multiplexer – A device that selects from several inputs to give one output.

MUX – Multiplexer.

New scroll zone – A signal inside the DC012 that indicates the beginning of a scroll zone and commands a new DMA.

NMOS – N-channel metal oxide semiconductor. Class of device used in the 8080 and 8251 and 2114 (memory chip).

No Scroll – A key that stops new data from entering the screen.

Nonvolatile RAM – Writable memory that does not lose its data when power is off.

NTSC – National Television Standards Committee

Null modem cable – A cable used to connect two RS232 devices when a modem is not needed. The transmit and receive lines are reversed at the cable connectors.

Numeric parameter – A string of bit combinations that represents a number, designated by Pn.

NVR – Nonvolatile RAM.

Offset – The number of scans a line is moved from the normal display position in a given frame during a smooth scroll. Also, the rearrangement of line display order according to LATOFS.

On-line – A condition in which all keyboard information passes to the host computer and the screen receives its data from the host.

Overrun error – Occurs in the PUSART if the microprocessor did not read a character before the next one arrived on top of it.

Parallel – A data path where all bits travel simultaneously on separate wires.

Parameter – A string of one or more characters that represent a single value or the value so represented.

Parameter string – A string of characters that represent one or more parameter values.

Parity – An error detection system based on the number of bits set in each data byte.

Parity error – An error condition indicating that at least one of the bits in a byte changed.

Parser – A process that separates a sequence into its component parts.

PD – Pump down. The signal that decreases the frequency of the voltage controlled oscillator.

PLL – Phase locked loop.

Pn – Parameter.

Pop – The microprocessor retrieves data from the stack.

Port – A place where data can enter or exit a device.

PRI INT – Printer interrupt.

PRI REC DATA – Received data from the printer.

PRI XMT DATA – Transmitted data to the printer.

PU – Pump up. The signal that increases the frequency of the voltage controlled oscillator.

Pulse width modulation – Encoding of data by varying the duty cycle of a continuous clock.

PUSART – Programmable universal synchronous/asynchronous receiver/transmitter. The communication devices in the terminal controller module and VT18X control module.

Push – The microprocessor puts data in the stack.

PWM – Pulse width modulation.

RAM – Random-access memory (also known as read/write memory).

RAS – Row address strobe. The signal that enables the row address decoder in the 64K RAM.

Raster – On a CRT screen, the effect of continuous vertical and horizontal deflections of the electron beam covering the full height and width of the screen. If the beam is turned off, the raster is not visible.

RCLK – Receive clock.

RDD – Raw read data from a disk drive unit.

Ready – A control line that forces a wait state in the 8080. Not used in the VT180.

Recall – A routine that sets set-up data from the NVR.

Refresh – The process of repeatedly rewriting the screen with data so it appears to to be constantly lit.

Reset – Setting a device to a starting condition, often for clearing errors.

Restart – Instruction the 8080 or Z80A performs when interrupted.

Retrace – Rapid movement of the turned-off CRT beam from the end of one pass to the beginning of another.

Reverse video – A character attribute. Characters are seen as dark areas in fields of light.

Reverse screen – A screen attribute. The entire screen is normally rendered as black characters on a white background.

Rollover – Ability to accept more than one key pressed at the same time.

ROM – Read-only memory.

ROMCS0 – ROM chip select 0.

ROMCS1 – ROM chip select 1.

Routine – Set of instructions to the microprocessor that makes it perform a particular function.

RS-170 – An EIA standard that dictates television signal characteristics.

RS-232-C – An EIA standard for communications between terminals and modems, using serial binary data. Signals may be unbalanced with a binary 1 (off or mark) being any signal between −3 V and −25 V, and a binary 0 (on or space) being any signal between +3 V and +25 V.

RSL – Recommended spares list.

RST – Restart instruction.

RTC – Real time clock.

RTS – Request to send; modem control signal.

RXC – Receiver clock for the communications PUSART.

RxD – Receive data; PUSART.

RxRDY – Receiver ready; PUSART.

Save – Process of storing set-up data in the NVR.

Scan – One horizontal pass of the CRT beam; also, the character information displayed in that pass.

Scan count – The video processor keeps count to help decide when to initiate a DMA and to provide addresses for the character generator ROM.

SCD – Secondary carrier detect. A modem control signal.

Schmitt trigger – A device that accepts a slowly varying signal to an input with hysteresis in its threshold of detection. It outputs clean transitions when the input passes the threshold of detection in either direction.

Scratch RAM – That portion of RAM used for 8080 microprocessor operations.

Screen – Face of CRT on which data is displayed.

Screen attribute – Applies to the entire display area: reverse screen, smooth scrolling.

Screen RAM – That portion of RAM used for display storage.

Scroll – Upward or downward movement of data on the screen.

SEL ATT RAM – Select attribute RAM. Signal for reading and writing data in the attribute RAM on the AVO under microprocessor control.

Selective parameter – A string of bit combinations that selects a subfunction from a specified list of subfunctions, designated by Ps. In general, a control sequence with more than one selective parameter causes the same effect as several control sequences, each with one selective parameter. For example, CSI Psa; Psb; Psc F is identical to CSI Psa F CSI Psb F CSI Psc F.

Serial – Transmission of data bit-by-bit over a single data line.

Set-up – Special mode of terminal operation for entering operating parameters from the keyboard.

Set-up specifications – Those terminal operating parameters entered from the keyboard or changeable from the host.

SHUFAD – Shuffle address. The pointer address location that changes during a shuffle.

SHUFDT – Shuffle data. The pointer address stored in SHUFAD during a shuffle.

Shuffle – The process of quickly rearranging pointer addresses when a line scrolls off or on the screen.

SILIN – The address where the next character enters the silo.

Silo – A scratch RAM area where data coming from the communication port is buffered on a first-in/first-out basis.

SILOUT – The address where the next character exits the silo.

Smooth scroll – Scrolling in which the data on the screen moves only one scan per frame.

Soft copy – Computer output that only exists as light on a screen.

Space – One state of a communication line. Generally defined as a high signal level or the absence of current. (See also mark.)

SPDI – Speed indicator. A modem control signal.

SPDS – Speed select. A modem control signal.

Split screen – Display operation where one part of the screen can scroll while another part remains stationary.

SR – Shift register. The device that performs parallel to serial conversion of data from the character generator ROM to the CRT. Also, the parallel-to-serial (or s-to-p converter) in UARTs and PUSARTs.

SRTS – Secondary request to send. A modem control signal.

Stack – Area of scratch RAM where the 8080 microprocessor places its current status while processing an interrupt or subroutine call.

Start bit – The first bit in a serial, asynchronous byte transmission, always a space.

Status byte – A byte of information about the operation of the 8080 that it outputs during the first machine cycle of an instruction. The byte is latched and decoded into control signals by the 8228 system controller.

Stop bit – The last bit in a serial, asynchronous byte transmission, always a mark.

STP – Standard terminal port. A connector on the terminal controller module. The CP/M processor module communicates with the terminal controller module through this connection.

STSTB – Status strobe. Signal output by the 8080 to latch the status byte into the 8228.

Sync – Any signal that allows one device to operate precisely in step with another. Particularly applies to synchronization of the electron beam in a monitor to the video data that modulates the beam.

Synchronous – Processes that occur in synchronism.

TBMT – Transmit buffer empty. A signal from the keyboard UART.

TC – Terminal controller. The main VT180 circuit board.

TCLK – Transmit clock.

Terminator – A character mixed in with screen data that signals the end of a line and causes the video processor to advance to the next line.

Timing chip – The DC011.

Toggle – To alternate the state of a device between two values.

Top half – In a double-height line, this is asserted for the top half of the line.

TRM DTR – Data terminal ready from general purpose serial port connector.

TRM REC DATA – Received data from general purpose serial port connector.

TRM XMT DATA – Transmitted data to general purpose serial port connector.

TxC – Transmitter clock for the communications PUSART.

TxD – Transmitter data. PUSART serial data output.

TxEMPTY – Transmitter empty. PUSART control output.

TxEN – Transmitter enable. A bit in the PUSART command instruction.

TxRDY – Transmitter ready. PUSART control output.

UART – Universal asynchronous receiver-transmitter. Wire-programmed device used in the keyboard interface.

Underline – A character attribute that forces scan 9 to show during a character.

μs – Microsecond.

VCO – Voltage controlled oscillator. An oscillator whose frequency output is varied by increasing or decreasing the amplitude of a dc voltage input.

Vector – The address of the first instruction for an interrupt handling routine.

VERT BLANK – Vertical blank. The signal that turns off the CRT beam during the vertical interval.

VERT DRIVE – Vertical drive. The direct drive signal from the video processor that synchronizes vertical deflection in the monitor.

VERT RESET – The signal that occurs at the bottom of the screen to start the video processor at the top.

Vertical interval – The portion of a raster when the beam is turned off and returning to the top of the screen.

VID WR 1 – Video write 1. The signal to load control data into the DC011.

VID WR 2 – Video write 2. The signal to load control data into the DC012.

Video processor – The circuitry that converts character codes stored in RAM into video signals that display as graphic characters on the screen.

VID IN – Video input (to the DC012).

VID OUT – Video output (two outputs from the DC012).

VSR LD – Video shift register load. A signal that determines whether the video shift register performs a parallel load or a shift when clocked.

VT52 – The Digital video terminal that preceded the VT180 and VT100. It responded to escape sequences conforming to an internal Digital Equipment Corporation standard.

VT52 mode – A VT180 mode in which it recognizes and responds only to escape sequences that Digital VT52 type terminals use.

Wait – Displayed message for operator during NVR operations. Also, an indefinite state in the 8080 controlled by ready (and not used in the VT180).

WRDOUT – Write data output. Write data to the disk drive.

WG – Write gate. This signal enables the write circuits in the disk drive.

WHO INIT – Who initialized. A CP/M processor signal.

Wire-ANDed – TTL devices with open-collector outputs can be tied together to form a logical AND gate at the outputs.

WRITE LB – Write line buffer. The signal that writes a character into the line buffer.

XMIT flag – Transmit flag. The signal to 8080 microprocessor from TxRDY at PUSART.

XOFF – Control character that asks the sender to stop sending.

XON – Control character that asks the sender to resume sending.

Z80A – The microprocessor device on the VT18X control module.

ZINT – The ORed interrupt signal from the four PUSARTs and the RTC. It is used to interrupt the Z80A.

ZRD – Z80A read output signal.

ZWR – Z80A write output signal.

ZIORQ – Z80A input/output request.

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