VOLUME 11, NO. 2 FEBRUARY 1981

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VOLUME 11, NO. 2 FEBRUARY 1981

Digital Design
Computers • Peripherals • Systems

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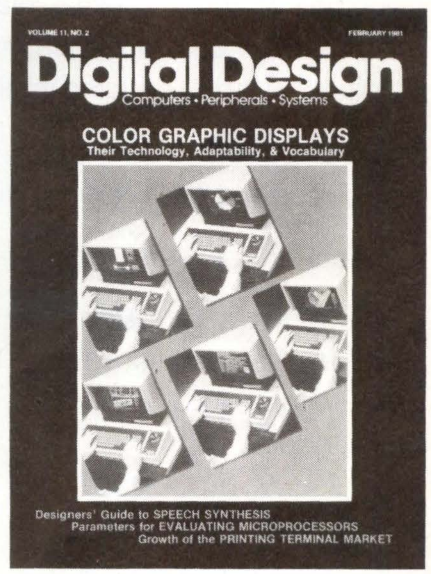
FEATURES

DEPARTMENTS



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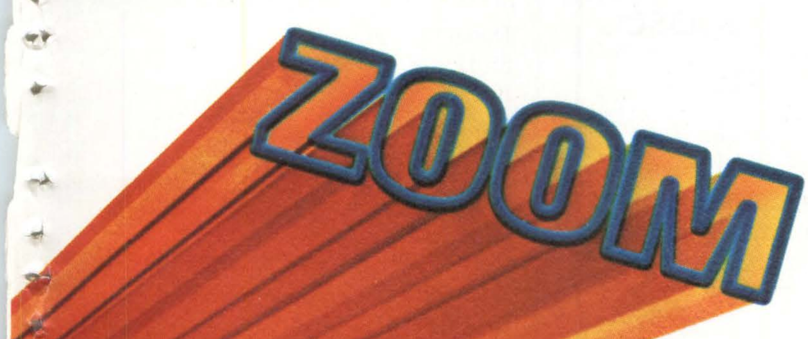

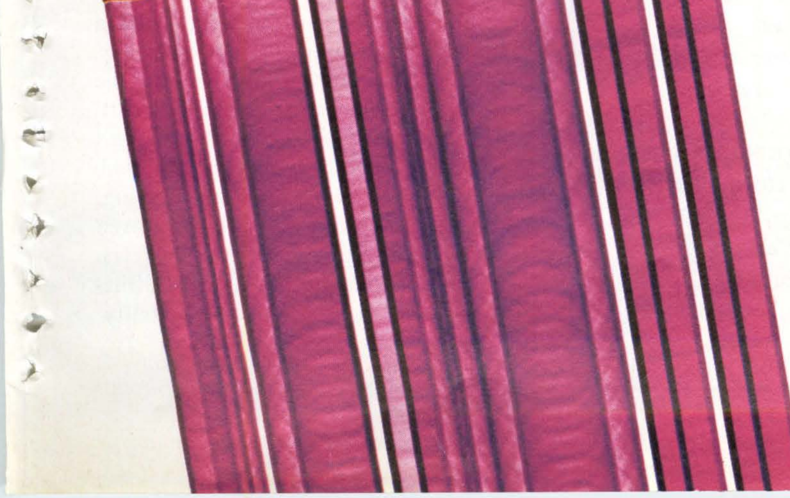

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Letters

No Solution?

Dear Editor:

As a former teacher, I taught math. I left teaching to enter engineering for the very reasons described in September's Speakout, "Time Is Running Out."

Administrators harass teachers who fail too many students. The result? Students are graded on how much they achieve based on their "ability to achieve" — a nebulous quantity that's determined by the teacher. Therefore, all students "pass" on the theory that it's better for the student to stay with his/her peer group. It is also known as "teacher self preservation." (Any teacher knocking the system is discredited by professional degradation and is harrassed by the administrators.) Students learn it's almost impossible to flunk a subject, so why work at it?

Donald L. Olson
Sr. Des. Engr.
Boeing
Seattle, WA

Disagrees

Dear Editor:

Your editorial commenting on the increasingly poor quality of newer workers (*Digital Design,* September, 1980) was, in many ways, accurate. But do not blame the poor quality of recent graduates from some American engineering schools on the poor high school training they receive.

The fact is that some graduates from American public schools are *the same* very bright people now beating down the doors of medical schools! Surely you cannot say *all* American public school graduates are poorly trained.

Many American companies have a solution: hire more foreign engineers. But it's counter-productive to the health of America's technical effort. These actions further discourage bright American kids from entering the engineering profession. Such alien hirings result in an increased surplus of even lower paid, more mediocre engineers. It will lead to the inevitable destruction of America's technical capability.

Irwin Feerst
Massapequa Park, NY

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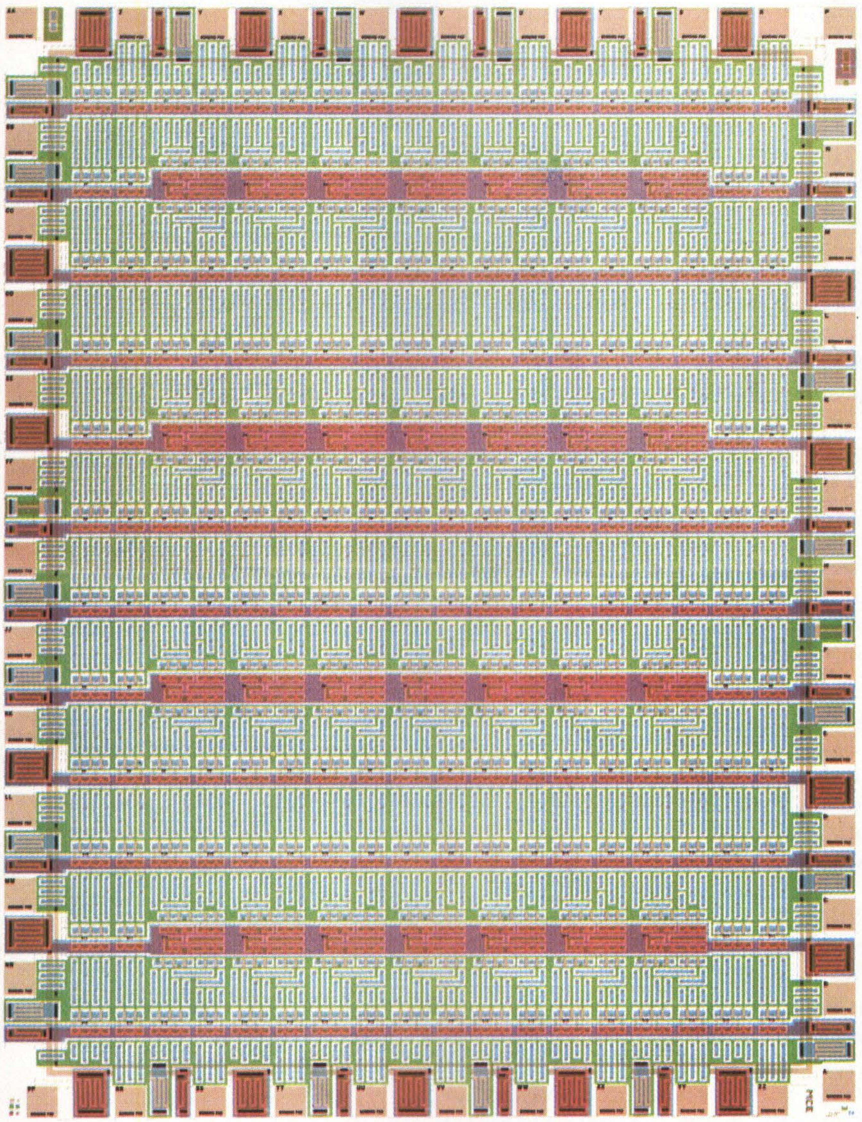

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Description	Specification at 25°C (5 volts)
444 equivalent gates	3 to 5 volts supply
28 dedicated D-type flip flops arranged in 4 rows of 7 each	Average propagation delay of 13ns (FO = 2)
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40 I/O/cells, 22 of which can be connected as three-state outputs	Storage temperature range: -55 to +150°C
136 x 174 mils	Operating temperature range: -55 to +125°C
44 pins max.	Proven metal gate CMOS technology

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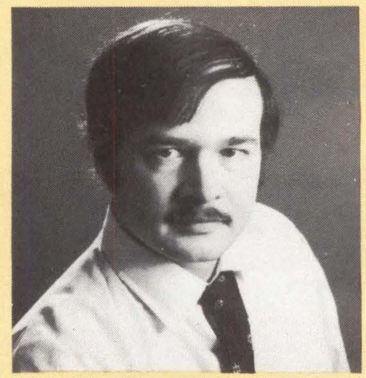
Speakout

Paul Snigier, *Editor*

Behind the Scenes — Part One



Foreign startups and purchases of U.S. electronics and computer firms will grow in the 1980s. That could affect our industry more than any other factor. Leafing through the somewhat defensive speeches and papers delivered by corporate executives of foreign computer firms invading the U.S. makes for interesting reading: it's basically fluff meant to obfuscate underlying causes. Why are foreign computer and electronics industries invading the U.S. so successfully? Is it merely due to sloppy American QC and dismal yields? Or, is it due to lazy U.S. engineers? Or, perhaps due to incompetent U.S. executives? Or, is it due to foreign workers with a yen to work hard (for low wages)? Or, perhaps due to the humanistic way foreign firms claim they treat their workers? The true reasons we found aren't the usual fluff you've read. Let's go behing the scenes.

The rapidity with which foreign startups are growing on the West Coast is astonishing many industry observers. These startups are not only getting into production fast, but are horizontal, and in every imaginable aspect of electronics (components, batteries, connectors, backplanes, displays, board-stuffing, semiconductor fabrication, computer systems). American firms that lack capital to expand fast enough are good targets for foreign interests. With the tighter capital-formation problems of the 1970s still plaguing us, and with entry prices into starting firms so high (and the cost of miscalculation so great), venture-capital groups remain reluctant to buy into startup firms and send in top managers to turn it around. The industry and trade press have called for action. We agree. But lowered maximum capital-gains tax, R&D tax credits, faster depreciation, ending double taxation on dividends and other measures, though sorely needed to keep U.S. computer makers, OEMs and system builders on an equal footing, *are not enough.*

The actual driving forces behind the accelerating foreign purchases of shares or controlling interest and growing foreign startups go deeper, and these remedies will not suffice. EEs, editors and most executives are totally unaware of the causes now affecting our electronics industry. The driving forces involve financial institutions in this country and abroad, and their major stockholders, all who have major political clout.

Foreign banks are now being encouraged by the Fed and U.S. officials to buy into the U.S. economic system; and, already, foreign interests control 4% of U.S. bank assets (up to 567% in eight years). In reality, 4% is more like 12% if you consider *total* U.S. banking assets involved. This will affect U.S. electronics.

To see how this works, let's consider the larger U.S. multinational banks; they hold significant blocks of stock in U.S. firms (like Sears and Avco) and in each other, and also in smaller banks in the electronics-intensive states (California, New York, Massachusetts, Texas). Thus, a foreign bank purchase of any of these megabanks would let foreign interests partially control the U.S. economy – and the U.S. electronics/computer industry – via this interlocking network of controls.

In the New York and San Francisco Federal Reserve districts – both situated in vital electronics and computer centers of our nation – foreign banks already have clout. In New York, for example, they already control half the votes needed to control the election of two (of nine) directors of the Federal Reserve Bank of NY. Will foreign banks use assets they acquire by taking over U.S. banks to finance their own electronics and computer industries?

In other words, can foreign banks finance foreign electronic and computer firms that compete with U.S. firms? It's not unlikely that these foreign banks will use assets acquired by takeover of U.S. banks to finance their own nation's computer firms. For an example of what could happen to the U.S. computer industry, look at the unlucky U.S. steel industry. With pension funds invested in (mostly) U.S. banks, which loaned more than just a little to the Japanese steel industry, the (unknowing) U.S. steelworkers essentially cut their own throats. The banks, their major stockholders and internationalist megabankers got richer; the U.S. steelworkers lost their jobs, and the U.S. steel industry was hurt. Now, if these banks were purchased or partially controlled by foreign interests, would these loans be decreased? Not very likely. If this can be done to the U.S. steel industry, what's to protect the U.S. electronics and computer industry?

Many financial institutions, through pension funds, control sizeable blocks of their own stocks. Sears, for example, uses its bank holdings and insurance to control a fifth of its stock (via Sears' pension fund investments in that firm). More computer firms are in the same situation. Now, if you assume a foreign purchase of these firms, then a potential throat-slitting situation.emerges, with U.S. pension funds financing foreign firms' R&D, manufacturing, and plant expansion to compete with U.S. computer manufacturers.

Continued next issue.

Paul Snigier

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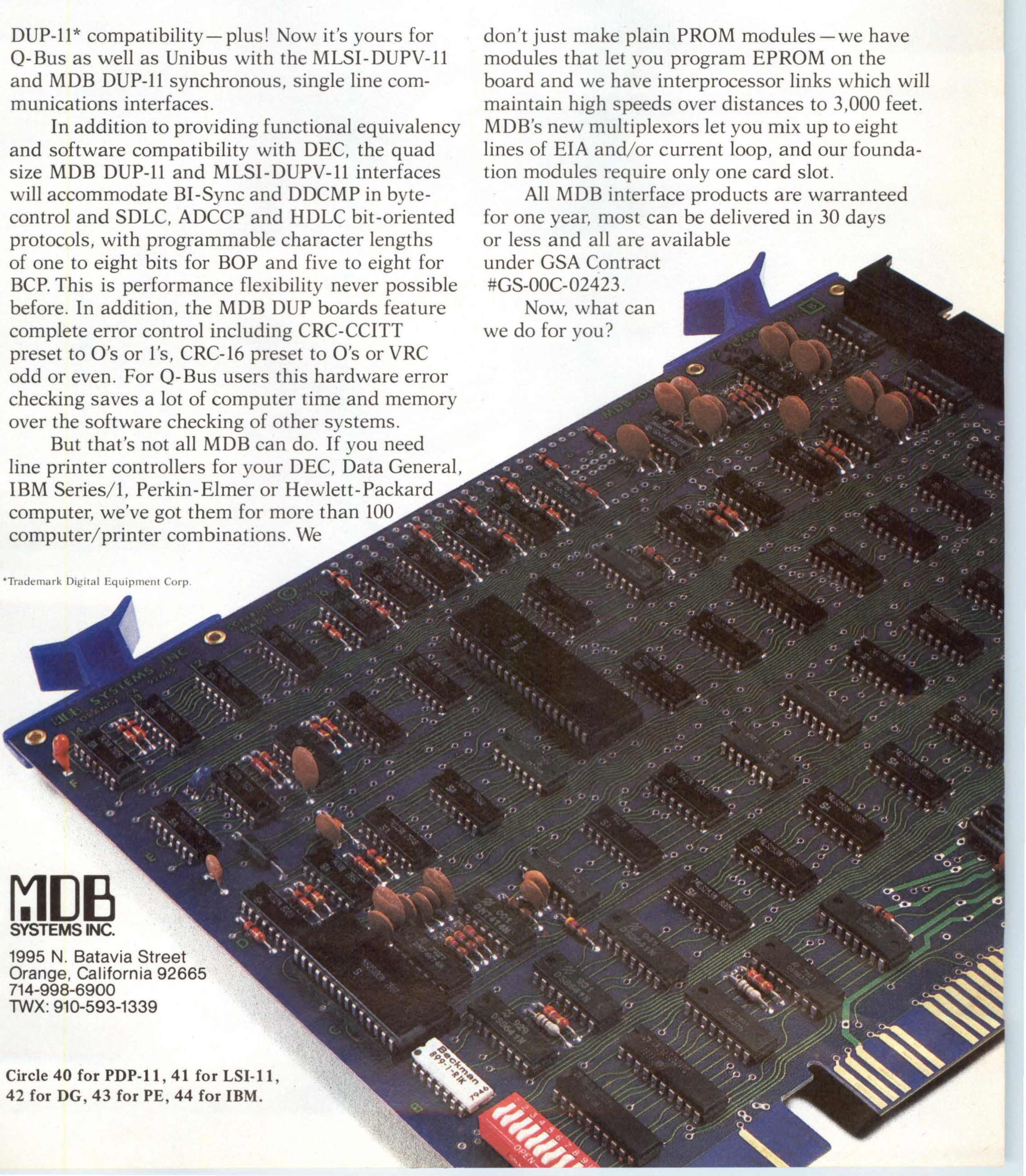

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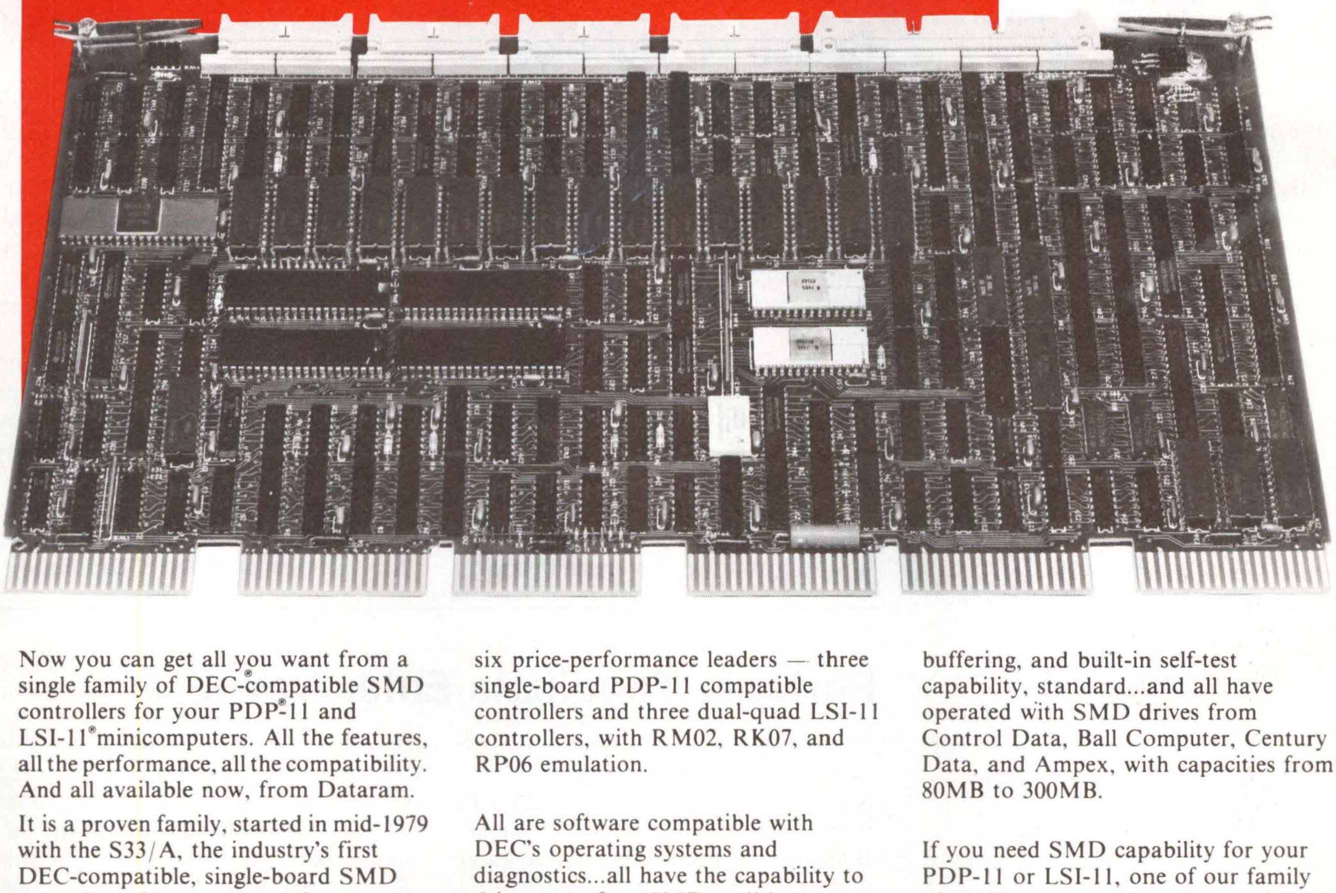

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LSI-11	S03/A	S03/B	S03/C	S03/D

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Data Recovery From Damaged Disks

"Data Recovery" is a process that can salvage data from damaged, crashed or marginal disk packs, cartridges and floppies, covering the whole technological spectrum. But can damaged media be used again on a system without causing significant damage? They can, provided an expert technician performs all required plastic surgery needed by the media, drive, R/W heads and software. The process is now being done safely, in minutes, and with no loss of data (in most cases.)

David Brown, to whom we talked, is the engineer who developed "Data Recovery." Methods Brown uses took years to perfect and already have proven successful in jobs throughout the United States. Need for such a service became apparent when records of a large corporation were virtually destroyed several years ago, due to a massive head crash involving almost every disk pack in the house. Brown recovered all that precious data.

He has since been hired by large corporations, hotels, small businesses and government agencies to repeat that delicate task. For the fired Las Vegas hotel, as an example, he retrieved the names of all the victims as well as all the guests staying at the hotel. IBM had backed out when asked by the hotel to try.

In 65 attempts, successful data recovery was achieved in varying degrees; 45 had 100% of the data salvaged; 13 had 90%; 7 had 80%; and there were two cases in which only a small amount of information could be recovered from the ruins. All Brown's attempts have been completed within two days and without further damage or downtime to equipment.

We asked Brown to provide us with some technical information and more details of his process. The technique Brown uses involves a familiarity with aerodynamics (a field in which Brown specializes) and a cross-disciplinary knowledge of several other fields. Because the procedures have not been patented (nor enforceable if they had been) Brown, understandably, declined to reveal his methods. However, if you've lost some important data and need to recover them, contact Joe Ludka II or Mark Myer at (213) 595-8301. You can reach them at Data Maintenance, (Div. of Randomex, Inc.,) 1100 East Willow St., Siganl Hill, CA 90806. Or you can write to David A. Brown, PO Box 3392, Anaheim, CA 92803. Tel. (714) 821-7639.

Bullish on Bubbles

On the road to success, magnetic bubble memories stumbled badly in 1981. Now, things are changing. The bubble memory market is ready to fulfill expectations. According to a new report from Venture Developement Corp., shipments will grow from $18 million last year to $226 million in 1985, or an average annual growth rate of 68%. Initial use will be in machine process control and portable terminals; but stationary computer and WP applications will become increasingly important.

Bubble prices will decline over the next five years as bubble makers learn how to make their product in quantity. The bubble chip requires auxilliary circuits to be useful. Intel designed ancillary ICs to accompany its megabit bubble memory device which will reduce component count ten fold. Although the system has been slow getting into production, this sort of circuit simplification is what users want. TI is the leading bubble memory producer; Rockwell International and Intel are other leading independent producers. IBM and AT&T perform research, with the latter producing units for its own systems. National Semi and Motorola are newer market entrants; Fujitsu, Hitachi, Siemens, SAGEM and NEC are foreign bubble producers.

Portable Terminals Enter New Era

Competition in the markets for handheld and briefcase terminals will intensify during the next five years with new vendors such as Tandy, Apple, IBM, DEC and Sears expected to enter the marketplace. However, current indicators point to a market that is expanding rapidly enough to permit success by many participants. This is the substance of an analysis of the portable terminals industry released recently by Creative Strategies International. Expect worldwide revenues for these terminals of nearly $900 million by 1985 – a compound annual growth rate of 31.5%. The growth rate for foreign revenues will be considerably higher as many U.S. vendors make a concerted effort to penetrate overseas markets.

The portable terminal has two major segments: handheld and briefcase. A handheld model has all portable terminal characteristics and is carried in one hand or cradled in one arm, while the other hand operates the terminal. A briefcase unit is a portable terminal that weighs under 40 lbs., and, when fully configured, fits within its own carrying case with handle.

Traditional applications, including order entry for inventory replenishment, currently account for over three-quarters of the market for handheld units, but this percentage will see a dramatic decrease by 1985. One of the largest new markets is in the area of route accounting. Major handheld vendors are marketing units in the softdrink, dairy, liquor, tobacco, and pharmaceutical distribution fields for regular sales and delivery routes.

Expect an even more dramatic growth rate for handheld terminal

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A must for your consideration because the Series 630 starts where other terminals stop.

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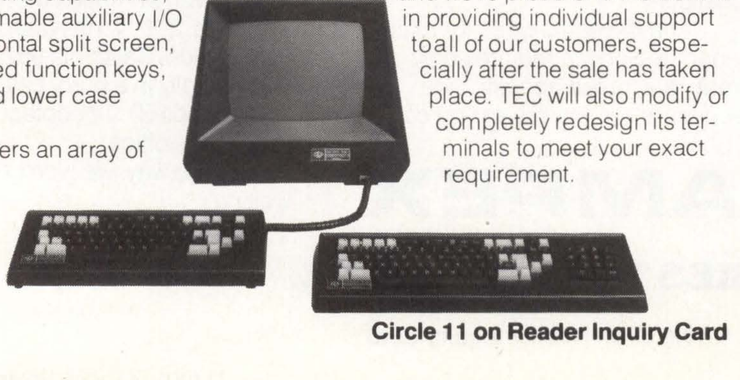

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revenues through 1985. The increasing popularity of higher-priced programmable units as well as an overall growth in unit shipments will be responsible for this rapid increase.

We have already seen the beginning of a more extensive type of briefcase function – distributive data processing. Terminals are being manufactured that are self-contained programmable μC systems with internal, as well as removable storage. Presently, most end users are engineers or specially-trained programmers in field analysis and testing. This end-user configuration will change significantly in the future as new industries, (such as insurance and real estate,) become fully automated.

Increased competition and new technological developments will result in big price drops for nonintelligent, smart, and μC-based briefcase units. But, despite these lower prices, revenues for this market will more than triple by 1985.

μC Group For IBM 360/370 μCs

The long-awaited single-chip μC with the IBM 370 instruction set is just over the horizon, and in a few years we will have the equivalent of a modest IBM 370/135 system on a desktop for under $20,000, with expansion memory less than $10,000/megabyte. Mokurai Cherlin of APL Business Consultants, Box 1131, Mt. Shasta, CA, doesn't want to wait until the desktop versions appear to form an interest group. Membership in Group/380, is $10 for individuals and $25 for corporations and groups. IBM, Intel and Motorola have all put the 370 instruction set on a chip. It is now only a question of waiting for it to go into production and then for someone to put it on an S-100 board. This approach will impose some arbitrary limitations, such as 16 bit memory access rather than 32 bit, and only 16 megabytes of real memory according to the IEEE standard, but users can live with this for a while. Intel and Motorola can provide full 32 bit bus implementations for those who want gigabyte memories.

There is more free, public domain software for the 360 than you can buy for all present micros together, including operating systems, languages, tools and applications. There have probably been about a thousand languages brought up on a 360 or 370 over the last 16 years. IBM itself has a list of more than 2500 public domain programs available for a copying and media charge, and the universities and users generally have lots more.

AAES: Friend Or Foe?

Is the new AAES a "pass the responsibility" ploy by top IEEE officials to get rid of embarrassing professional issues, like age discrimination? In a recent letter to Chairpersons of IEEE sections, Irwin Feerst urges scheduling one meeting to discuss IEEE's participation in the new and controverisial umbrella organization, the American Association of Engineering Societies. Feerst claims IEEE's action in supporting and funding AAES was done in secrecy, with no meaningful discussions or comments solicited, and that "the same people who opposed IEEE's professional activities in the past are now spokesmen for AAES."

First VHSIC Complexity Chip

Honeywell's Solid State Electronics Center has completed its initial wafer run of a bipolar VHSIC demo chip that establishes feasibility of DOD VHSIC Phase I speed and density goals. The chip is 200 × 250 mils and has about 7,000 gates, 5,000 in a gate array and the balance in a programmable logic array, register stack and 16-bit shift register latch.

This chip has less than 0.6-ns gate delay on the high-speed logic family and under 2 ns on the high-density family, which reaches 74,000 gates/cm^2.

Pro And Con

User self-maintenance offers vendors a partial solution to rising costs resulting from high wages, transportation costs, levels of training required, and for smaller companies, recruiting time needed to continue growth and to offset high turnover. Maintenance reve-

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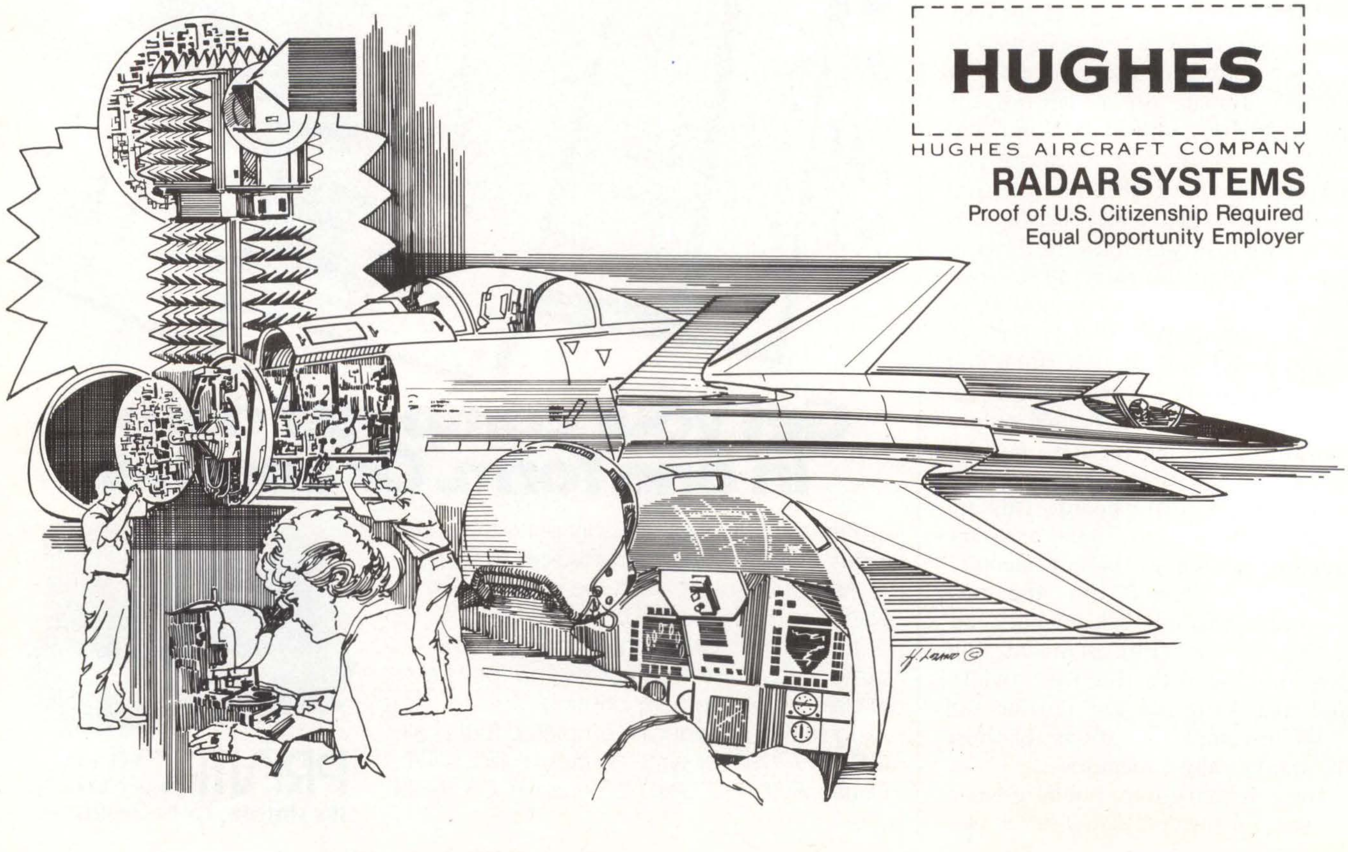

nues for information processing equipment in the U.S. was about $6 billion last year. However, if too much self-maintenance is built into product offerings, the overall impact can be adverse, according to Walter Smith of Input in Palo Alto, CA. Each 1% shift of revenues into user self-maintenance means a "loss" of $60 million in annual maintenance revenues. Vendors will need to balance cost, revenue growth and profit.

Super-Speed Technology Emerges

Honeywell, IBM and a number of other large "computer companies" have always been considered big, silent giants. Although publicity releases and product announcements have flowed in abundance from these companies, corporate officers rarely came out of their dens to make public speeches of press conferences. They have participated as keynote speakers at various ACM, NCC and related functions. Other than that they have stayed pretty much out of the public eye. Now, corporate officials of Honeywell are touring the country and talking to the technical press about developments in its high-technology research. This touring company is proving quite popular with audiences and the procedure is likely to be followed by Rockwell, IBM, TI and others.

Result of these developments, say the Honeywell people, will someday be seen in end products which will all end up on one chip. The Cray Machine, world's most powerful computer, for example, will operate from only two chips.

Existing Software Cuts Costs

Werner L. Frank of Informatics Inc. of Woodland Hills, CA, warns OEMers that hardware availability and pricing are becoming secondary to software availability and implementation. Frank offers several tips.

To increase OEM productivity when software isn't your firm's forte, minimize new internal development and follow these rules. First, use as much existing software as possible to reduce new development costs. Leave these latter expenses to be borne by software producers who can spread costs over a wider base. Second, avoid developing in-house system programs; try to use available general purpose software products. Third, if you must build your own application programs, use modern implementation systems. Build a prototype system as fast as possible to get the application up and running in parallel, on live data, then sit back and ask "Is this what's really needed?" Revise the prototype and use it as soon as possible. Finally, refine the programs for production efficiency.

There's no hope for software breakthroughs that will make programming easier, faster or more economical. Neither Pascal, Ada nor anything else holds promise. Rather, the availability today of a wide spectrum of software firms producing standard implementation and application packages is about the only way to get a quantum jump, Frank added.

Software development in the near future will make computers "user-friendly." This is necessary because of the increase of smaller systems and growing population of first-time users.

"Most applications will be built from the current level of people expenditures, even though software complexity will increase," Frank said. "Unfortunately, throwing more people at the problem will only contribute to the problem – if great care is not given to assure that they are the best."

Logic Arrays Enter The VLSI Era

Ever-decreasing circuit geometries allow an increasing number of active element groups (AEGs) to be incorporated on a single chip. The increasing complexity at a lower cost/AEG resulted in an explosive demand. However, as semiconductor complexity increases, time and cost of circuit design multiplies. How affordabile are VLSI circuit designs? They involve a much larger share of the overall system design and become more specialized in nature.

A big problem emerges: as complexity increases from a few AEGs/

chip to thousands of AEGs, parts required to construct a system decreases; however, the number of end-use systems served by identical parts also decreases. Taking this concept to the foreseeable limits of VLSI technology – where a single VLSI part will fulfill the total system requirement – a new custom part would be required for each system application!

An alternative to the high cost of customizing individual dedicated systems has come from the development of a new class of "programmable system components." The architecture of the component remains essentially the same until the final masks are processed. Then the part is customized through "solid-state programmation."

The single-chip μC exemplifies this. During final processing of the slice, the software program developed to define the system's functional specifications is converted into a single-level mask, then imprinted in the memory. This offers a cost improvement of 1000:1 over the same system implemented with standard discrete semiconductors, and more than 15:1 over the same system implemented in custom LSI circuitry. However, the level of complexity achieved to date has limited this approach to relatively simple, high-volume applications, most of which have been digital in nature. With the tenfold increase in complexity possible with VLSI, the concept of programmability, with its associated lower costs, will be able to serve much larger numbers of system applications.

A programmable system component that offers great promise as a system solution for a growing number of VLSI logic-circuit requirements is the logic array. This is an array of unconnected logic elements arranged so that they can be interconnected to perform a logic function.

The benefits of using programmed logic arrays versus custom logic can be seen by comparing the design-cycle times and costs. Logic-array times reduce costs in two ways. The first is processing time. TI fabricates and stockpiles the logic-array master. Programmation – the customizing steps – is then added in the final two metallization steps. The second reduction in design-cycle time comes from the use of automated interconnection layout software to perform I/O programming, gate partitioning, gate placement, contact assignment, and routing. The cycle times using logic arrays is generally less than 25% that of custom logic, with the design costs ranging from 33% to 10% of the cost of custom-logic design. As the industry moves into the VLSI era, the increased use of E-Beam direct slice writing will undoubtedly play a vital role in further minimizing prototype cycle time.

As semiconductor technology changes, corresponding changes will impact the customer interface. Where production volumes are very large, there will continue to be custom logic designs supplied by the component manufacturer, but this relationship will be strained significantly with the advent of higher complexity parts, the need to transfer very large amounts of data, and the resulting higher design costs per product.

The growing capability of logic arrays and other programmable system components will relieve much of the need for specialized custom logic. To use these components effectively, the component manufacturer must provide a fast-turnaround product-prototyping capability and a computer-aided-design utility to the systems manufacturer.

The TI family of Schottky Transistor Logic (STL) logic arrays is supported by a totally integrated design utility. The software-support system incorporates advanced simulation and verification of the logic design, as well as routability analysis, test pattern and program generation.

Clustered Systems To Lead ITs

Sale of intelligent terminals (ITs) in the U.S. will increase dramatically over the next five years, approaching \$2 billion by 1985. While the total IT industry is expected to grow at a compound annual rate of nearly 32%, growth rates for each of the major product segments will differ significantly. The IT industry can be segmented in two ways: by amount of intelligence (e.g., standalone versus clustered systems); and by type of storage (diskette, cassette, hard disk, and others). Over the next five years, the clustered IT market will show the highest rate of growth.

Unlike standalone terminals, which will decline in price, the average cost per clustered system will increase; according to CSI of San Jose, CA. This is

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due to a higher mean number of clustered terminals per system and the cost of additional CPU overhead to accommodate input/output handling and processing necessary to support the additional terminals. The combination of faster growth and higher revenues per system will result in clustered systems overtaking standalones in terms of revenue by the end of 1985.

Computer Industry to Continue 15% Growth

Although both inflation and recession have had significant impact on other parts of the economy, the U.S. computer industry will continue relatively unscathed. From $27.9 billion in 1978, industry shipments will grow at an annualized rate of 15.3% to reach $49.2B in 1982.

The value of computer peripherals will increase by 14.8% annually. The fastest growing products in this category will be graphic CRT terminals. Shipments of these terminals will increase by 34.7% annually. Non-impact printers will also show an exceptional growth rate of 30.0%. Speed and versatility will continue to be critical qualities in the peripherals area. Another aspect of this market noted in study by VDC of Wellesley, MA, is the desirability of increased intelligence in virtually every product category.

The value of data storage or memory devices will grow at a slightly lower rate than the other two industry categories: 13.8% annually. While tape drives will show only modest growth, disk drive shipments will expand significantly. Floppy disk drives will be the fastest growing product in the category with shipment value increasing by 40.5% annually.

Enhancements Improve Diskettes

Floppy disks differ drastically. What should you look for? "Mechanical improvements, particularly reinforced hub rings, help avoid disk centering problems. Other improvements in lubricants, burnishing and liner material also enhance product life and protect data for diskette users," according to Rod Crisp, Verbatim marketing manager. Crisp lists seven factors: longer-lasting lubricant, improved liner, a thicker and more uniform oxide coating, advanced burnishing techniques, reinforcing hub rings, stricter and more extensive testing standards, and a revised certification program that exceeds ANSI and ISO standards. Oxide coating improvement provides enhanced adhesive and cohesive strength. A thicker coating provides 10% more protective lubricant and an optimized signal for read/record heads. The lubricant is more resistant to diffusion and protects against media wear from head-to-disk contact. Advanced burnishing techniques result in smoother disk surfaces and less head wear. More uniform liners remove debris more efficiently and allow more lubricant to reach the head to minimize head wear. Finally, look for reinforcing hub rings to eliminate slippage, reduce errors, prevent pinching, aid in registration and allow better alignment repeatability.

Innovative Design

Telescoping Actuator Positions Winchester R/W Heads

All of the important performance characteristics of any Winchester drive hinge directly on its R/W head positioning ability. Higher positioning accuracy means higher information density and, correspondingly, higher capacity and faster data seek time.

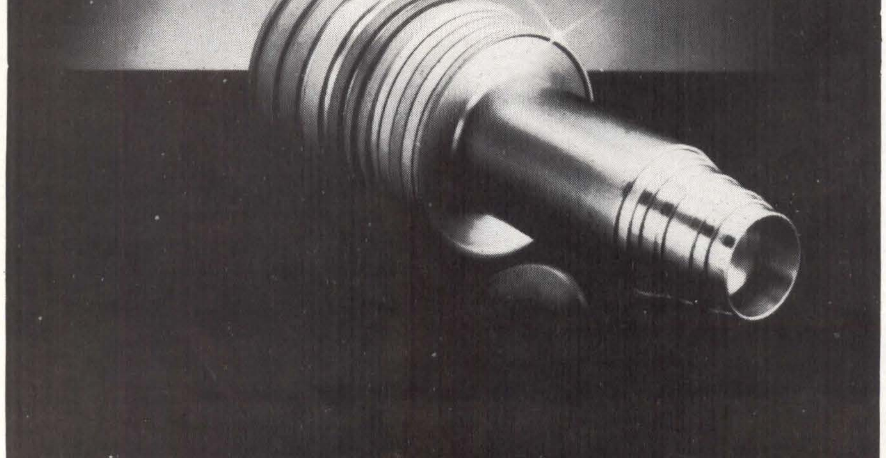
Head positioning devices, or "actuators" usually are either stepper motors (in lower priced units) or voice coils (generally in more expensive units). Ontrax Corp. recently announced a family of drives using a unique actuator system they claim is "simpler, less expensive and more accurate than existing rotary actuator devices."

Ontrax's actuator is a telescoping cylinder comprised of nine concentric elements. A carriage attaches to this cylinder and holds two R/W heads for each disk surface it services. Totally expanded, the Ontrax actuator moves 3/4″. Since the actual usable surface of a standard 8″ disk is only 1.5″ in radius, two R/W heads cover the entire disk.

Each of the actuator's nine elements has a specific range; each element travels twice the linear distance of the previous one. By choosing the proper combination of elements, the intelligent unit can telescope a R/W head to any one of 512 discrete locations on the disk surface.

Upon reaching the indicated location, the head uses an embedded servo technique for position verification, checking for any errors due to temperature or other operating conditions.

If the head is off-mark, a squeeze-coil positioner, with a total movement range of only two mils, performs fine-tuning. The squeeze coil is a very stiff spring opposed by an electromagnetic coil. Current applied to the coil causes the squeeze coil to move slightly – its two mils of total movement subdivide into 256 steps.



Air space between elements provides a natural damping, eliminating "crash stops" inherent in conventional actuators. Allowing the proper rate of air leakage from interstitial space between the elements acts as a brake, cushioning the tail end of the positioner's travel in either direction.

Ontrax stresses that their drive family, called Series 8, uses no servo head, servo arm, servo surface or servo read channel. Embedded servo techniques assist only in position verification, not in actual head positioning. Lack of any disk surface area delegated to servo positioning sensing and feedback increases data storage space accordingly.

Using five platters, Ontrax's highest capacity drive puts 136 MB (unformatted) on 9600 data tracks. Model 136 uses two positioners controlling 16 R/W heads (only eight of the ten disk surfaces perform data storage). Also available are 68- and 34-MB drives using three and two platters, respectively.

Each of the three drives is comprised of both the disk drive and an integral power supply system. Each achieves a data rate of over 9.2 megabits per second, with an average rotational latency of seven msecs. Data density is 7158 bpi and data seek times average 25 msecs.

Elimination of voice coil positioners, which have large, heavy permanent magnets, reduces overall size and weight of the Series 8 drives; each drive measures 21.5 cm wide by 17 cm high by 61 cm deep, and weighs approximately 27 kg.

Ontrax Model 136, with ANSI interface, costs approximately $4000 in quantities of 250-500. With controller, the price is $5500. Lower capacity drives are available for several hundred dollars less.

–Bob Hirshon

Ontrax Corp., 611 Vaqueros Ave., Sunnyvale, CA 94086. **Circle 197**

Rotating LED Array

Generation of three-dimensional images is a combination of science and art, still in its infancy. In fact, all of the 3-D imaging technologies developed to date would fit into a single paragraph.

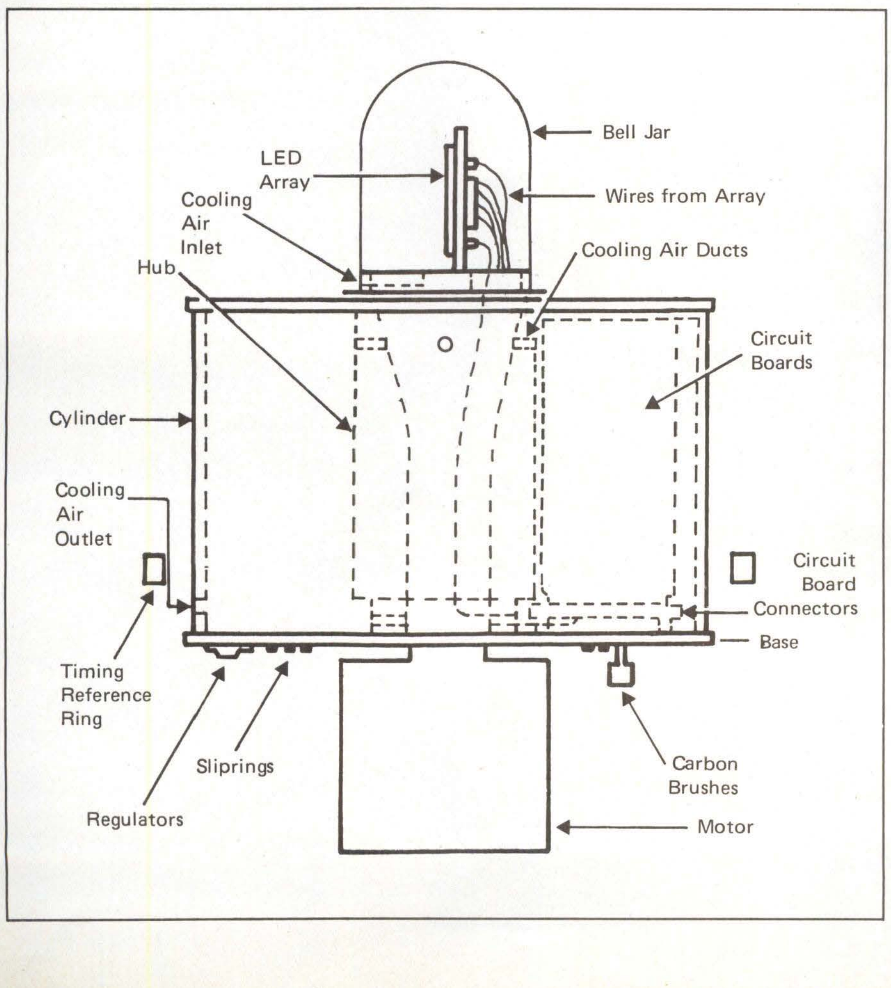
Stereoscopic viewing with special eyeglasses came first, but found little use in the science world and only brief success in the art world. Holograms, images which viewers can walk around and actually view from different angles, showed considerably more promise, but remain expensive on a cost-per-image basis, and are at least temporarily confined to very specialized use. Vibrating mirror technology, in which a mirrored surface flexes rapidly, altering its focal length, thereby creating a Z-dimension in any image it reflects, is an exciting new concept. But observers must remain stationary; if they walk behind the viewing area, they see not the back of the object, but the back of the mirror. This same limitation is true of graphic displays that simulate the third dimension.

To this short history, MIT's Innovation Center adds a new entry. Nameless thus far, MIT's video system consists of a flat array of LEDs spun at 15 revolutions per second by a synchronous motor. Image cross-sections flash sequentially on the array as it rotates. Observers cannot detect the rapidly displayed cross-sections but rather, due to an optical phenomenon known as "persistance of vision," slur the series of cross-sections into a single, 3-D image, seemingly hanging in the space above the motor.

As with a true three-dimensional object, observers can walk around the image to view it from all sides. In addition, an operator may control data directing the LEDs, thereby moving the image itself in almost any manner.

Invention and development of the imaging system was a purely in-house effort of MIT's seven-year-old Innovation Center. Edwin P. Berling, Jr., now an MIT graduate, came up with the original idea of a rotating array, while he was student at the center. Three other Innovation Center students who have since graduated, Glen Dash, John Goodhue, and Isidor Strauss, invented the high-speed data link required to put the concept into practice.

David Jansson, director of the center, first recognized the promise of Berlin's idea, and directed efforts to get a prototype constructed. Funding for the project came thanks to a Michigan neurologist who envisioned using MIT's device to display 3-D data produced by computerized axial tomograph (CAT) scanners, that record images of nerve cells. The neurologist organized a group of investors and founded Tri-Vi Corp., expressly to support development of the technology.



The prototype device at MIT has an array only two inches square, with a resolution of 32 LEDs per inch. Jansson envisions units with larger displays for use in computer-aided design, radar and sonar displays, and non-destructive testing. "Our immediate interest," says Jansson, "is in the commercialization of our device by selling or licensing the technology to a company anxious to manufacture and market this new product."

—Bob Hirshon

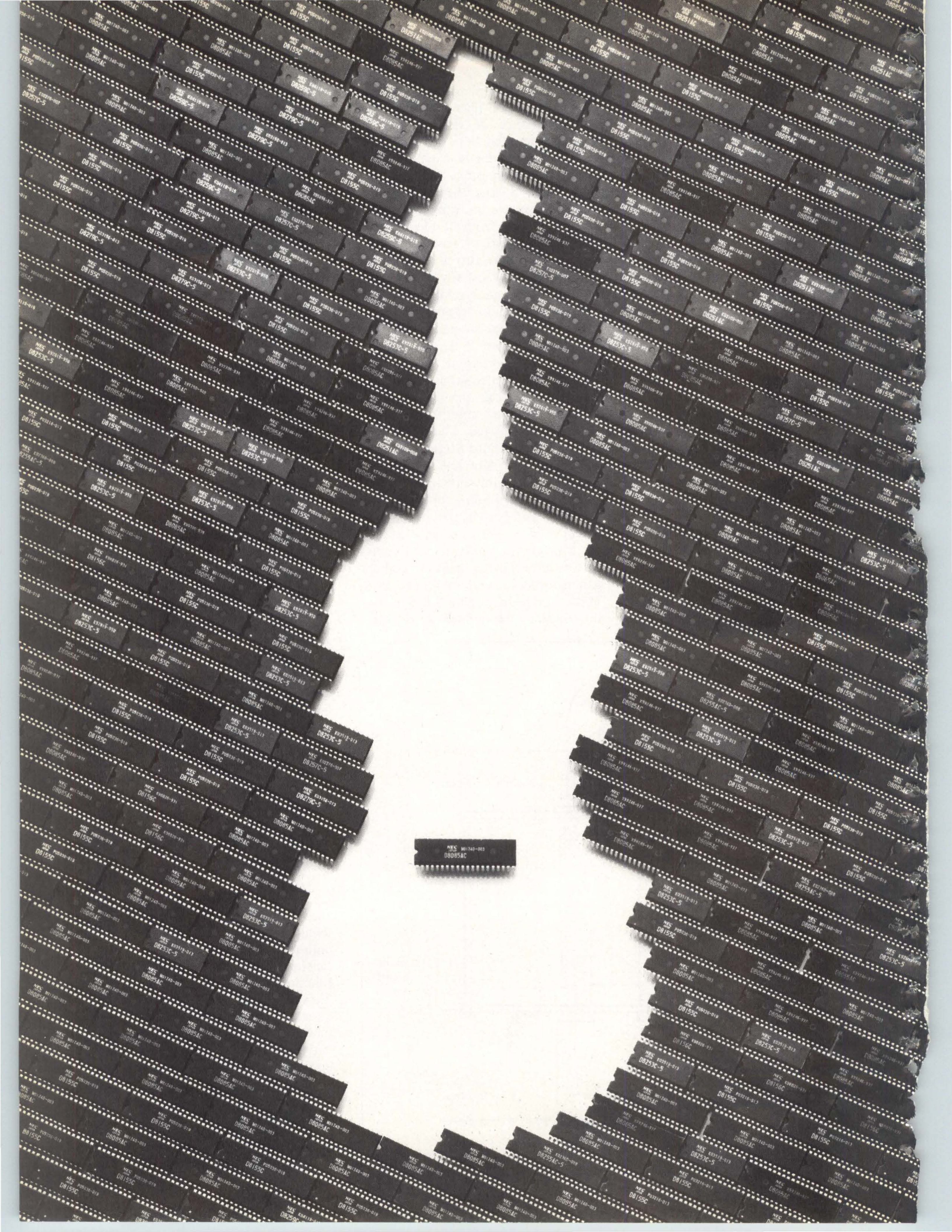
MIT Information Center, David Jansson, Rm. W91-208, Cambridge, MA 02139. **Circle 198**

VLSI Master Logic Arrays

Texas Instruments' Dallas Division recently introduced its own family of efficient, high-performance LSI master logic arrays. These devices provide greater circuit density through higher levels of integration and improved cost effectiveness in the design and manufacture of digital systems. Two members of the STL array family are currently in production: the TAT008, a 1008-gate master logic array, and the TAT004 with 540 gates. Nominal internal-array gate performance is 2.5 nanoseconds at 600 microwatts, with a maximum flip-flop clock frequency of 80MHz. All inputs and outputs are compatible with low-power Schottky TTL.

These TI master logic arrays are the beginning of series of high-performance, VLSI logic arrays which are interconnect-configured to a customer's unique logic requirements, allowing efficient implementation of custom IC functions with minimal time and cost. They are structured specifically to facilitate automatic layout, with a cellular organization that provides spaces between cells dedicated to global interconnection.

The TAT008 1008-gate master logic array has 108 I/Os, and the 540-gate TAT004 has 84. Both are offered in a variety of packages, including standard DIPs, chip-carriers, and 100-mil-array-of-pins packaging.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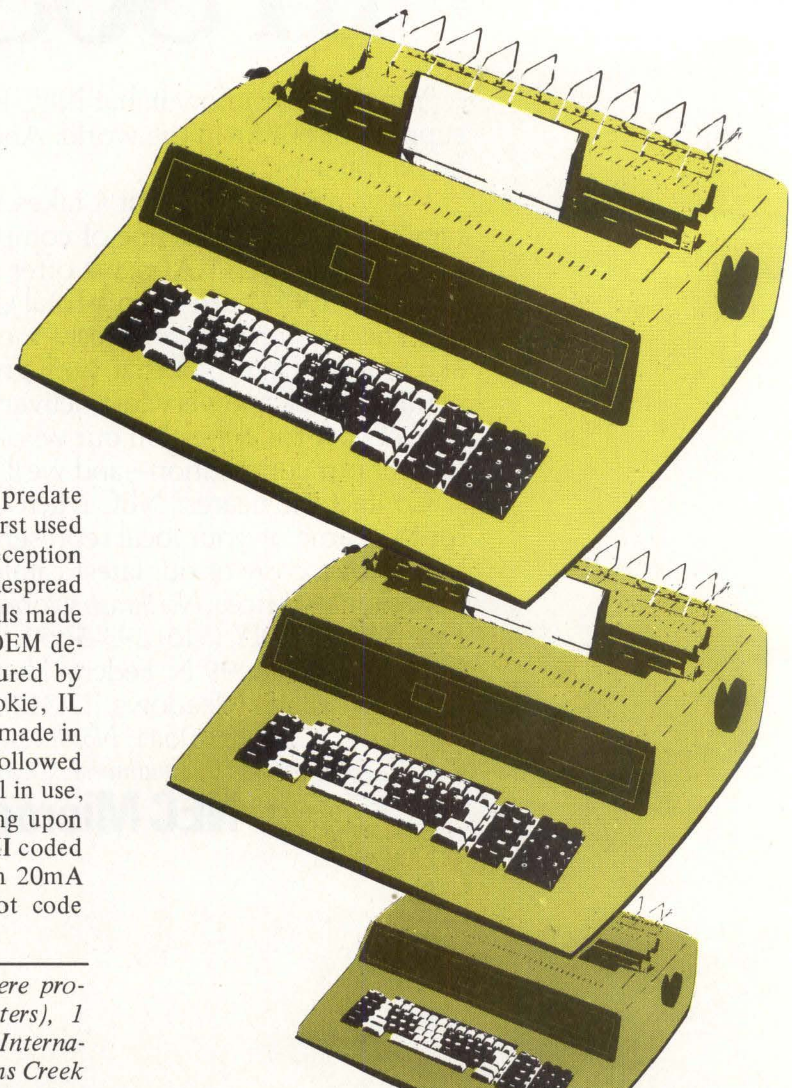
Printing Terminal Growth Continues

A Staff Report



The printing terminal market continues to grow, with the predicted shakeout of smaller teleprinter manufacturers not a significant factor.

Sudden change

Unlike video display terminals, printing terminals predate the computer age by three decades. Teleprinters, first used to transmit messages over wires, found ready reception among early (pre-1976) computer users. The widespread usage and ready availability of such printing terminals made them an instant success with computer users and OEM designers. The universal TTY or teletype, manufactured by the Teletype Corp. (an AT&T subsidiary) of Skokie, IL (which holds a trade mark on the name), was first made in the 1920s. The 11, 12 and 14 models were first, followed by the 15, 19, 28 and 32 – many of which are still in use, with prices ranging from $30 up to $500, depending upon condition. Models 33, 35 and 400 (all 8-level ASCII coded machines that directly interface to most CPUs with 20mA current loop) replaced the earlier 5-level Baudot code antiques.

Facts and predictions contained in this article were provided by Venture Development Corp. (teleprinters), 1 Washington St, Wellesley, MA; Creative Strategies International (teleprinters, portable terminals), 4340 Stevens Creek Blvd, Suite 275, San Jose, CA; International Resource Development Inc., (voice-activated typewriters), 30 High St, Norwalk, CT. For detailed studies on these subjects, contact these firms directly.

But it was the ASR-33 that became so ubiquitous and popular (over 800,000 machines sold) that it was the machine thought of when reference was made to teleprinters. The ASR-33, an automatic send/receive unit, included keyboard, printer, tape reader and punch. For early development systems – used to develop programs of limited length – the slow and klunky teleprinter sufficed. But, by 1976, more EEs found the traditional teleprinter wasted time. With efficient program editors, but with slow 10-cps TTYS and paper tape, waiting for a program to be retyped each pass wasted endless hours. If his application program was 10,000 lines long, the programmer could count on wasting four hours watching it crawl through his TTY on a second pass.

The ASR-33, number 3320, 3JA was probably the most common version in use. It operated at 10 cps with an 11-bit word (110 baud), with the transmitted word consisting of one start bit, two stop bits and eight data bits (with the eighth bit an even parity bit). Several manufacturers made teleprinters similar to the ASR-33; most dropped out; and the only serious competitor the TTY had was the Olivetti 308/318, which I used in 1976 to write 3850 programs. Although a superior teletype, it never achieved the success in America that the ASR-33 did, and it was just as frustrating to use. By 1976, EEs and their employers recognized that the "penny wise, pound foolish" savings of the traditional teleprinter for what it was: a mirage. At this stage, Teletype and IBM owned the market.

New printing terminals

The growing need for improved printing terminals created pressure for improved video display terminals and improved printing terminals. The pressures resulted in faster terminals, terminals with greater capability, and terminal lines that were broadened to meet OEM and user demands. The growth from 1976 to 1981 has exceeded all predictions.

These improved printing terminals used Daisy wheel, impact-cylindrical wheel, Selectric ball, rotating belt, Carousel print cup, and 7x7 and 7x9 matrix impact printing terminals. Some used thermal and electrosensitive print techniques; these were suited to portable units resembling oversized briefcases. With the entry of TI's Silent 700 series, delivery times stretched out to half a year. Everyone expanded their production facilities, unaware that it was a saturable market and that many teleprinters were in user applications that are relatively more sensitive to recession.

Shakeout for some

Shipments of teleprinter terminals last year were lower than some industry prognosticators had predicted. Although the first dip of the recession did not hit the computer industry, the teleprinter terminal market was hurt. Were teleprinter manufacturers upset? Not really, since they felt this downward trend would not continue. Will shipments in 1981 make up for 1980? If worldwide sales were to exceed $2B in four years, this still wouldn't help in 1981, since the second dip of this recession may be worse than the first.

How can teleprinter sales decline when demand is strong? With teleprinter sales dropping $200M or so, and with DEC and Teletype unable to meet supply, the fact is that these two industry leaders saw larger than expected growth rates last year. The vast majority saw flat or negative growth last year. One West Coast manufacturer echoed the sentiments of many smaller teleprinter manufacturers: "Competition from the big guys is getting fierce. They're lowering prices, and we can't afford to do that. It looks like we'll be getting out of this business pretty soon."

Will there be a shake-out in the teleprinter industry in the near future? Yes. Of the 32 U.S.-based teleprinter manufacturers, three industry leaders control over 60% of the 1980 shipments. Growth potential for these and 15 others is good; but, the rest of the pack will lose market share. As major teleprinter manufacturers grow, some will replace their current product lines with newer technologies.

The fastest-growing sector of the market is non-impact teleprinters. Despite two major drawbacks of non-impact teleprinters (thermal types require expensive heat-sensitive paper, and they print one copy) great growth potential is in this area. Some big manufacturers who are not yet in this area will start production of non-impact teleprinters in the near future.

The daisywheel segment of the impact teleprinter market is doing well. These suppliers have more on their minds than just growth rates: a few industry executives worry over Japanese entering the daisywheel market. Why? Japanese daisywheel manufacturers are coming out with improved technologies at lower prices, but most U.S. manufacturers have no plans to drastically lower prices. Instead, they want to improve their price/performance ratios. Is this a better strategy? Probably. Users want performance over cost.

User acceptance of new transmission codes and protocols is coming. Since the 1974 introduction of IBM's Synchronous Data Link Control protocol, SDLC gained acceptance. It may become a de factor standard.

Installed base manufacturers' market share is as follows: Teletype, 45.7%; DEC, 13.7%; TI, 10.0%; Extel, 5.5%; GE, 5.5%; IBM, 5.5%; Honeywell, 4.6%; Others, 9.5%.

The bright side

Aside from some shakeouts of smaller manufacturers, new growth opportunities will spur teleprinter sales. Some predict that by 1985, the compound annual growth rate will exceed 21% and that unit shipments will increase at a rate of 30.9%, compounded annually.

Business-oriented data communications networks will remain strong markets for teleprinters in the distributed processing framework. In addition to traditional business situations in which teleprinters have been successful, there is a tremendous potential for teleprinter use in conjuction with public data networks, automated electronic mail, and the vast, untapped home consumer market.

In general, products from today's teleprinter industry are more communications oriented than similarly-priced counterparts in the office products marketplace. They lack the standard WP software of most office keyboard printers (i.e., intelligent typewriters and printer-based word-processing terminals). Many teleprinter entries will be office oriented. Anderson-Jacobson's AJ410 Electronic Mailbox, which typifies this forward trend, provides typewriter functions and high-speed, electronic mail capabilities to inter- and intra-office communications and other remote terminal locations. As a result, 18% of all teleprinters installed over the next five years will be related to electronic mail, office automation and interoffice message systems.

Public data networks (PDNs) will provide the entry vehicle for teleprinting terminals into the home market. Network services, such as those providing stock information, selected types of news and weather data, and others, are already available on a modest scale. PDN firms will become large customers for low-value-added teleprinters. These firms, in turn, will sell or lease these terminals to their subscribers and thus facilitate an increased usage of other PDN applications available to the home. Subscribers may also purchase terminals directly from traditional terminal vendors. Other potential home applications include newspaper/magazine delivery, electronic U.S. mail, text editing, word processing, electronic yellow pages, travel planning and reservations, library research, family bookkeeping, keyboard entertainment, etc.

At the high end, the teleprinter market is driven by sophistication of functional capability. Price is still important, but function is the key. The technological rate of change in the 80s will be more important than in the 70s. With new technologies often becoming obsolete within three years of introduction, product flexibility and extensibility will become critical.

CRTs: no threat

Are CRT devices serious contenders for the attention of teleprinter users? Teleprinters and video display devices will evolve toward separate markets. Both have attractive market potential. Rather than full-size CRT displays used with teleprinter activities, a 1- to 3-line LED/LCD display will be incorporated into the teleprinter to facilitate input, reading and editing of material prior to transmission.

Portable terminal growth explosive

Handheld and briefcase (self-contained) terminals are a rapidly-growing market. Before 1984, new vendors will include Tandy, Apple, IBM, DEC and Sears. This won't hurt, since this market is growing so fast.

Worldwide revenues for these terminals could exceed $900 million by 1985 (a compound annual growth rate of 31.5%). The growth rate for foreign revenues will be considerably higher, since many U.S. vendors will try to penetrate overseas markets.

A portable terminal, a handheld or briefcase terminal, has some type of communication capability, costs under $10,000, and is used mostly for business applications. There are two major types: handheld and briefcase terminals. A handheld model has all the portable terminal characteristics and is held in one hand or cradled in one arm, while the other hand operates the terminal. A briefcase unit weighs under forty pounds, and, when fully configured, it fits within its own carrying case with handle.

Traditional applications, including order entry for inventory replenishment, currently hold over three-quarters of the market for handheld units; by 1985, this percentage will decline dramatically. One of the largest new markets is in route accounting. Major handheld vendors are marketing units in the softdrink, dairy, liquor, tobacco and pharmaceutical distribution fields for regular sales and delivery routes.

Handhelds to exceed briefcase terminals

There will be an even more dramatic growth rate for handheld terminal revenues through 1985. The increasing popularity of higher-priced programmable units as well as an overall growth in unit shipments will cause this rapid increase. This decade will see the beginning of a more extensive type of briefcase function: distributive data processing, terminals that are self-contained programmable μC systems with internal and removable storage. At present, most end users are engineers or specially-trained programmers in field analysis and testing. This end-user configuration will change significantly as new industries (such as insurance and real estate) become fully automated.

Increased competition and new technological developments will result in substantial price decreases for nonintelligent, smart and microcomputer-based briefcase units during the forecast period. Despite these lower prices, revenues for this market will more than triple by 1985.

Voice-activated printing terminals by 1983?

Faster-than-expected progress in the development of speech recognition technology will result in the commercial availability of voice-activated printing terminals and typewriters by 1983; they will be in "widespread" use by the end of the decade. A competitive battle will develop between IBM, Xerox and Matsushita for dominance of this market in the mid-1980s. More than one million typists and secretaries will lose their jobs due to these new machines.

Secretaries "Clean Up" machine guesses

The first commercial versions of the voice-activated unit will correctly recognize about 95% of "typical" business English as spoken by the average executive. The first IBM units will have a CRT screen to display the spoken words. Then the dictator or his secretary will type in those words which the machine failed to recognize correctly. The recently-announced IBM Displaywriter product may form the basis for an expanded family of word processing devices, including speech recognition equipment.

IBM is already including a 50,000 word vocabulary as a standard feature in the Displaywriter, as reported earlier in *Digital Design*. It will be logical for IBM to use this vocabulary as the basis for "guessing" the correct spelling of words dictated to the machine. Although the English language has plenty of homonyms and other features which make 100%-accurate machine-recognition almost impossible, Displaywriter already recognizes possible homonyms and highlights them for possible correction.

Languages which are more phonetic than English are much easier to use in speech recognition applications. Thus, Matsushita's voice-activated unit (expected in 1983) will do a better job on Japanese than the IBM machine will do on English! A "very high quality" voice-activated unit is also expected from Xerox by 1984. Other potential suppliers may include Olivetti and Wang.

Keyboard printing terminal extinction?

Will voice-activated printing terminals kill off keyboard-entry printing terminals? Not at first. Let's look into the future. Here's a timetable.

Last year (1980), we saw rapid advances in speech recognition by Threshold Technology, IBM, Xerox/Kurzweil, Matsushita, Perception Technology and others. The first announcement of commercial voice activated units was made by Matsushita for a 1983 delivery. By 1983, IBM will start delivering voice-activated versions of Displaywriter products. Xerox will announce high-end units. Matsushita will deliver Japanese units. By 1985, worldwide shipments will reach 25,000, and other U.S. companies, probably including Exxon, will get into this market. Then, trouble. By 1986, some "Luddite" labor problems will hit the European and U.S. market, as typists and keyboard operators are layed off. The labor union resistance will be unable to stop the voice-activated printing terminal; and, by 1987, shipments will exceed 100,000. Larger volumes will lead to significant price drops. By 1990, cumulative shipments will approach one million. By this time, there will emerge a noticeable impact on most office routines. Value of shipments will exceed value of regular keyboard units shipped.

Magnetic Bubble Memory Systems:

Interfacing and Sub-Systems Meet Designers' Objectives

Roger Haggard
Texas Instruments
Dallas, TX

The Bubble Memory Controller (BMC) is the high-level interface between the host system and the modular memory unit (MMU). The MMU consists of the MBM and a group of interface ICs that must be repeated for each MBM added to the system. These recurring interface circuits include the Bipolar Coil Drivers (TIB0804), Write Function Driver (TIB0884), Read Function Driver (TIB0864), Schottky Diode Array (SDA) and the Dual-Channel Sense Amplifier (TIB0834). Since the hardware interfacing between the host system and the bubble memory subsystem occurs almost entirely between the host CPU and the bubble memory controller, the primary topic of this article is the BMC and its operation.

MBM Controller

The functions of the controller are to start and stop bubble movement, maintain page position information, control generation and swapping of data, and supervise block replication of data and replication of redundancy information. In addition, the TIB0903 provides the I/O control, data buffering, and bubble tracking necessary to interface to a Communications Register Unit (CRU) type I/O port. Other features of the controller include direct compatibility with the TMS 9900, TMS 9980 and TMS 9940 CPUs, interrupt or polled I/O operation, on-chip synchronization, operation from a single 5-V supply and operation with a bubble field rate and data rate of 100 kHz.

The TIB0903 interfaces to the CPU through the CRU. The CRU interface consists of four address select lines (S0-S3), a chip select and three control lines (CRUIN, CRUOUT and CRUCLK). The communications register unit is a bit-addressable (4096 input and 4096 output bits), synchronous, serial interface used by the TMS 9900 family of CPUs. It is through this interface that a single CPU instruction can transfer between one and 16 bits serially. Each one of the 4096 bits of the CRU space has a unique address and can be read and written to. During a multi-bit CRU transfer, the CRU address is automatically incremented at the beginning of each CRU cycle to point to the next consecutive CRU bit. In data transfers between the CPU and the controller, when the chip select line becomes active (LOW), the four address select lines address the CRU bit being accessed. During a write operation when data is being transferred from the CPU to the controller, the CRUOUT line carries the data which is strobed by CRUCLK. When controller data is being read by the CPU, the CRUIN line is used as the output by the controller.

During system initialization, the redundancy map stored in the bubble memory's redundancy loop is transferred to the redundancy map RAM in the controller. Then during a write operation, the redundancy information is used to gate the data stream as it is used to generate bubbles. Actually, input data to the controller first enters the CRU serial/parallel interface block. From there data bytes (8 parallel bits) are transferred to the FIFO data buffer under direction of the FIFO CTL (control) block. The data is then transferred serially to the sequencer where the redundancy information

MANUFACTURER	BOARD NUMBER	BUBBLE MEMORY DEVICE USED	BIT STORAGE CAPACITY	COMMENTS
TI	TBB50005	TIM0500	512K	Board size 24 sq. in.
TI	TBB5010	TIB1000	1 M	Board size 24 sq. in.
TI	TBB5910	TIB1000	2 M	Uses 2-1 M bit bubble devices
Rockwell	RLM658	RBM256	1 M	Uses 4-256K bit bubble devices, requires separate controller board (RCM650)
Rockwell	RMS121/122	RBM256	256K/512K	RMS122 uses 2-256K bit devices
Rockwell	RMS141/142	RBM411	1 M/2 M	RMS142 uses 2-1 M bit devices
Intel	IMB100	7110	1 M	Board size 16 sq. in.
Intel	ISBC250	7110	1 M	Expandible beyond 1 M bit.
National	NBS100/101	NBM2256	256K/1 M	NBS101 is a storage expansion board for NBS100

Board Level Bubble Memory Systems

is used to insert zeros in the bit stream representing defective loops in the bubble memory. The output of the controller is the BGEN line which connects to the function timing generator which in turn produces a bubble generate signal to generate a bubble in the write track of the bubble device. During a read operation, redundancy is handled in much the same way. As the serial data enters the controller from the bubble memory, it is gated into the serial-to-parallel converter with the redundancy information used to remove the zeros that were added to the bit stream during a write operation. The data is then transferred to the FIFO and from there passes through the output multiplexer and CRU serial parallel interface to the CPU.

PC Board MBM Subsystems

To compete in the market, Magnetic Bubble Memory products need features which offer systems designers optimum flexibility regarding transfer rate, access time, cost-per-byte, system cost, power consumption and storage capacity. Texas Instruments has met these needs by developing and producing 92-bit, 256-bit, 512-bit, and 1-Mbit magnetic bubble memories. To support these products TI has developed complete families of interface circuits which allow the designer to concentrate on the system design without the need to become intimately familiar with the electrical and magnetic properties of bubble memories. These support circuits require only TTL compatible inputs which provide efficient and expandable designs for any bubble memory application. Then, to make these products even easier to use, TI has developed and produced a line of printed-circuit boards containing complete bubble memory subsystems. These board products are available in a variety of sizes and types in order to meet the capacity and interfacing requirements of many different types of applications.

These are by no means the only MBM board products; there are others. While the above board products are complete MBM subsystems that can meet interface requirements of a variety of systems, some designers want to design their own custom interface. Two prototyping boards are available: TBB5990A with 92-kbit bubble memory and TBB5910A with 1-Mbit family of devices. Each has a large pad array for custom prototyping or development work. These boards remove the burden of designing the Bubble Memory Module (consisting of the bubble memory device and its support and drive circuits) which requires special layout considerations. These subsystems share the advantages of other bubble memory products such as small size, fast access time, solid state reliability, low power consumption, light weight, natural non-volatility and no required maintenance.

μC module add-in

The TM 990/210 is an assembled, tested non-volatile MBM board compatible with the TM 990 series of SBC products. This member of the TI line of OEM computer products contains two, four, or six TIB0203 92-kbit MBM devices which provide up to 69 kbytes of data storage. The board uses parallel, memory mapped I/O to interface to either the TM 990/100 or TM 990/101 CPU modules. The 92-kbit device is a more mature product than some of the recent entries into the bubble memory market. This gives the TM 990/210 two advantages. One is lower cost and the other is that the devices can be more easily screened for higher temperature operations. Thus, the TM 990/210 is available with two operating temperature classifications: 0-50°C and 0-70°C. Another feature of the memory board is software support. This consists of an interactive monitor called TIBUB (TM990/451 which may be located anywhere within the addressing range of the CPU module. This is a separate option which is housed in two TMS 2716 EPROM's. The monitor allows inspection and modification of bubble memory locations in a byte orientated fashion. Program Load, Debug, Disassembly and Execution are also supported. TIBUB may be used as a bootloader to load bootstrap programs for bubble memory based systems. TIBUB supports direct write and read subroutine calls to the TM 990/210 which simplifies application programming. A complete verification test for the TM 990/210 is also included in TIBUB. In addition to TIBUB, TM990/453 TI Power Basic also supports the TM990/210 with a file manager that offers reading/writing of user data and loading/storing of program data under program control using named files in the bubble memory.

Applications

Because the TM 990/210 board shares the advantages of TI's other bubble memory products, it finds application in many of the same areas. Some of these include telephone switching systems, digital voice recorders, process control equipment, add-in memory boards to enhance disk and tape systems, and navigational control systems for military applications.

Interfacing

TBB7090 interfaces to the CPU via a 16-bit address bus, an 8-bit data bus, and nine control lines, all of which are TTL buffered. The board may be run asynchronously from the CPU clock such as when the CPU is the 6800, or synchronously with the clock such as when the CPU is the Z-80 or 8085. The WAITQ/ signal allows fast μPs to be used but also requires the use of an external wait state generator when 4-MHz processors, such as the Z-80, are used.

To communicate with the CPU, the bubble memory controller is equipped with an 8-bit bi-directional data port which has data buffers between the controller and the system data bus. Sixteen memory mapped registers are presented to the CPU through 16 contiguous memory locations whose base address is selected via DIP switches. Twelve bits of the address bus are compared with the address set up on the switches. If the addresses are equal, then the data buffers are enabled and data is transferred.

Summary

Three magnetic bubble memory boards have been discussed in terms of their features, functional block diagrams, interfacing details and applications. The primary purpose of these boards is to enable a designer to benefit from all of the advantages of bubble memories without having to completely design the bubble memory system. This has been achieved through flexible hardware interfacing and easy-to-use software. In all cases, the hardware interfacing has already been done and all the designer needs to do is select the position of certain jumpers and plug in the board. Software interfacing is also greatly simplified through the use of the optional TIBUB interactive monitor and Power Basic file management capabilities. These MBM boards are also comparatively low cost memories and are very cost competitive in today's market. With these many advantages, the MBM board products are finding application in electronic terminals, telecommunication equipment, business machines, industrial applications, disk and tape replacement, and military applications.

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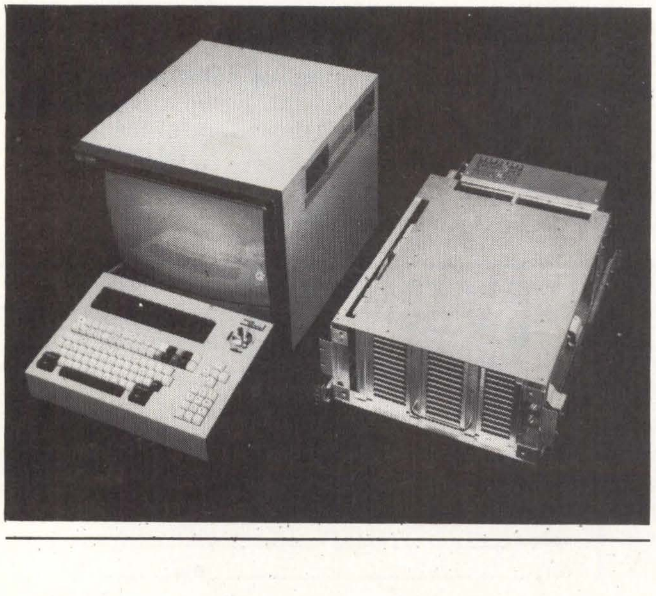
The Expanding Field of Graphics Displays

Harry Shershow, *Editor*



Graphic-display terminals were first developed at MIT in 1953 as a component of the new Whirlwind computer. Whirlwind was the first "general purpose" computer to be developed during and after World War II. Its hardware later became the skeleton around which Digital Equipment Corporation constructed its commercial PDP-1 "low price" computer." Ken Olsen, a research assistant on the Whirlwind project, founded DEC in the late 1950's, a few years after the project was abandoned, (government research money having been halted.) From both Whirlwind and DEC have come the progenitors of today's graphics displays. Those early terminals (non-CRT) sold from $50,000 to $120,000 each and were as large as today's mainframes. With their point-plotting technology they were used primarily in engineering and scientific research.

Like chocolate and vanilla ice cream, display terminals today are available in two popular flavors: alphanumeric or graphic. The alphanumeric variety, work horse of the DP industry, displays and manipulates information. The graphics terminal, on the other hand, is the gone-to-college, smart-alecky, sophisticated offspring. Hardly old enough to walk by itself, it still drags umbilical cords behind it which are attached to joysticks or digitizers and which are used to manipulate screen images in a performance of amazing acrobatics.

Graphic displays are offered in four different technologies: raster scan, stroke writer, storage tube and plasma display. The storage tube, grandfather of the whole family, was the first technology in computer display. An electron beam sweeps across the face of the screen and produces a light green picture against a dark green background. Face of the tube can retain the image up to several hours because of the slow decomposition of the phosphorescent screen coating. The great disadvantages to storage tube display are its slowness and the necessity of redrawing an entire image when only a single part requires change. It also must be viewed in room lighting, is not suitable for interactive situations, its tube life is short and replacement is expensive.

The stroke writer does not store the image on the screen like the storage tube, but uses, instead, a brief computer listing to generate the image. This listing permits modification of selected portions of the image and makes possible some dynamic functions like rotation and scrolling. Three colors can be used in stroke writing on a beam-penetration tube. Very high resolution rates are possible but the user must pay for it with an annoying increase in flicker.

Plasma panel display uses a sandwich of three sheets of glass instead of the CRT tube. The center sheet is perforated with many holes filled with gas. Electrical charges on the outside glass plates cause the gas to glow in a low-intensity orange hue at selected points. Like the storage tube, the panel display stores the image on the screen. Such displays have found military acceptance where flatness and ruggedness are required.

Raster scan is the dominant technology in graphics displays. Besides universal use in television, it has been refined for the sophisticated demands of business, research and industry. The screen is scanned by an electron beam moving across and down and turning off at selected points. This movement of the beam is induced by an electromagnetic deflection yoke in the neck of the CRT. The screen uses three colors of phosphor and offers an unlimited palette of different colors and gray scale values (more than two million). In addition, a broad range of brightness levels is possible by varying the intensity of the electron beam through the control grid on the CRT. Raster scan has brought with it a wide range of screen resolutions. Displays can now be ordered in a choice of resolutions depending on applications and economics. Lower resolutions mean lower costs for the terminal.

In today's computer society, terminal is a word with a hazy connotation. Generally, it is considered a device that communicates with, or receives communications from, a computer. Sippi's COMPUTER DICTIONARY lists 73 different definitions of the word by itself or as part of a compound noun like Terminal Polling. Aydin Controls Company, a leading manufacturer of raster scan and random scan color graphic computer display equipment, defines "terminal" as a graphic display station with some essential components (CRT monitor, display generator and host computer.) Aydin separates its raster scan products into two distinct groups: Limited Graphics and Full Graphics.

The **Limited Graphics** family of display products is equipped with 256 preprogrammed alphanumeric and graphic displays. These products are designed for use in process control applications where terminals are located at key monitoring positions. Aydin classifies this product line as being character or semi-graphics. A semi-graphic display generator is offered by the company in either single-channel or multi-channel configurations.

A single-channel display terminal is configured in several selectable options from an OEM-version output-only display driver, to a "stand-alone" end user microcomputer system with semi-graphic color display capability. The term **stand-alone**, explains Aydin, as applied to color graphic terminals, is somewhat of a misnomer in the sense that the vast majority of terminals are tied to a system either directly or through some form of data communications link. Aydin considers "stand-alone" to mean the existince of local processing and mass storage capability, even though the terminal may be connected to a system in some way.

The multi-channel controller type of semi-graphic display is designed as a component of larger Supervisory Command and Data Acquisition (SCADA) systems and large process control systems. These systems require a number of operator stations at a central facility for monitoring and control of system functions. Each operator station is a terminal configuration with one or more CRT monitors. It has an operator's keyboard with alphanumeric, fixed function and programmable function keys. In addition to alphanumeric and full graphic displays, data trending (waterfall or strip chart) and full graphic displays of moderate resolution (512X256) can be generated. All Aydin's display terminals are interfaced to the host computer via one or more high-speed parallel interfaces which provide for rapid update of each operator station in a highly interactive mode.

Aydin's **Full Graphics** products are more sophisticated with programmable graphics functions, pixel addressability and up to 4096 colors. Instead of graphic generators, the full graphics products are controlled by Aydin's Display Computers which are configured to customers specification.

Graphic color systems, in general, use four memory planes, one for each of three colors (red, blue, green) and one for black and white alphanumerics. Memory graphics planes are offered in dimensions from 74.1 X 65.5 bits (4,854) up to 4096 X 4096 bits (16,777,216); the alphanumerics memory plane is usually in the 32,000 bit range. Data and bits in each memory plane can be independently manipulated allowing words and numbers to be changed easily; and unlimited alterations and positions of color images are possible.

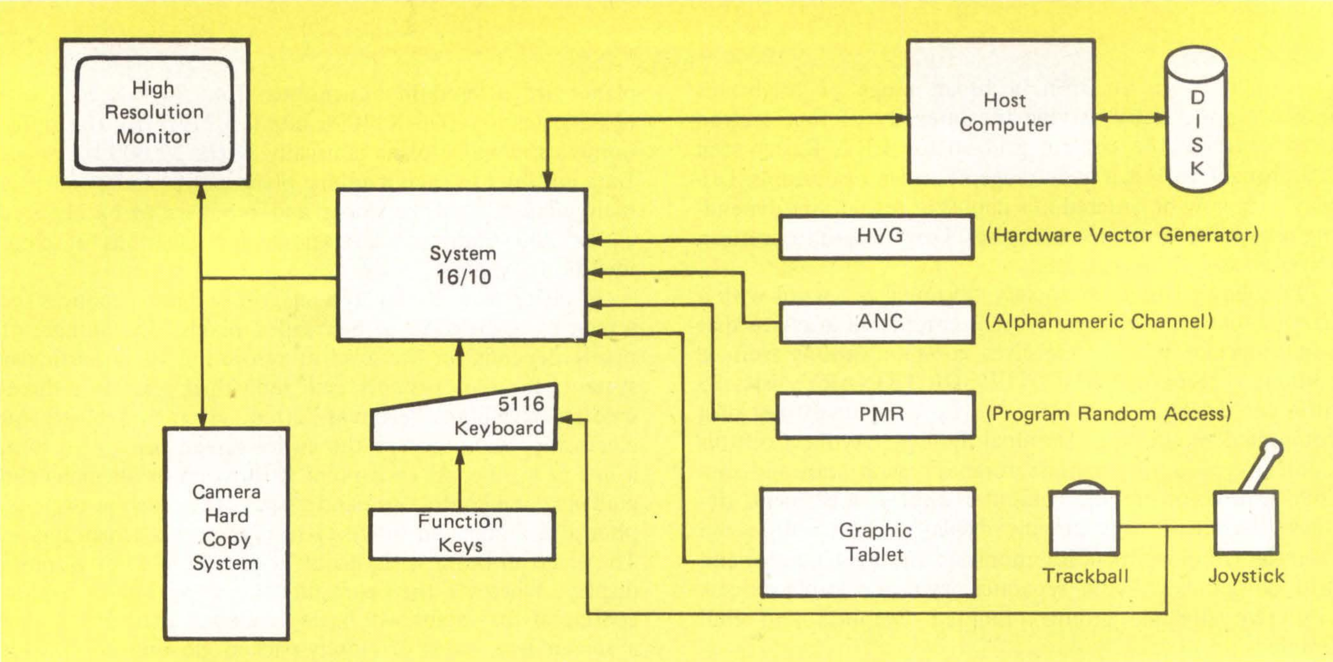
In raster scan display systems, the computer reduces the screen to addressable points called pixels. The number of pixels depends on the level of resolution for a particular system. In color systems each individual pixel is a three-colored phosphor "element," (red, green and blue.) An electronic beam sweeps the entire screen top to bottom, a line at a time. At each point it turns on or off under the guidance of a control grid and singles out one color of phosphor at a designated intensity to construct a screen image. The electron beam is the paint brush of the color graphics display. Wherever the beam hits the screen, the phosphor coating at that point will begin to glow. (A straight line on a screen is a series of closely-packed glowing dots.) This glow can last as long as several hours (in direct view storage tubes) or as briefly as 50 milliseconds (in raster scanning.) Because of its evanescent characteristic, a raster-scanned image must be refreshed (bombarded continuously with electrons) at least 30 times per second to prevent image dimming or flickering. Horizontal scans are made in 54 microseconds; a vertical scan, 17 milliseconds. The high-speed electron beam, therefore, is able to refresh each phosphor element before it burns out on the screen and before the next image frame is projected.

For alphanumeric applications, character "cells" of 7X10 pixels are usually employed. Characters in these cells can be colored, blinked, reversed or shown at different brightness levels. The background color can also be changed freely.

All graphic displays on computer terminals are obtained in one of two general ways: vector or raster. The vector method uses XY coordinates that define the end points of a line. Images are analyzed in terms of the straight lines in their construction. Curves become short, straight line segments. Input devices for capturing image information and transmitting it to the screen via the computer include: digitizer (data tablet); joystick; track ball; keyboard; light pen; function keys; and camera digitizer.

In the raster method, pictures are broken into small screen "cells." Each cell contains one of a range of colors and shades. The cells are called pixels (picture elements.) The quality of a raster picture depends on the number of pixels per unit area (resolution), the range of colors and shades, the size of the pixel. Vector input is used for capturing and transmitting information that is essentially linear; raster input is used with continuous-tone information.

Spatial "resolution" of a raster image is the product of the number of horizontal pixels times the number of vertical pixels. Color resolution is the number of bits per pixel and depends on the number of color/intensity choices possible at each pixel. A graphics system with 256 X 256 by 4 bits resolution has 65,536 pixels, each of which may display 2^4 (16) colors/intensities. A RAM frame buffer holds a digital version of an image. This buffer is scanned by the graphics interface and converted into video information. A 256 X 256 X 4 bit resolution requires at least an equivalent size buffer. However, the buffer can exist in the form of modules (all the same size) to increase the resolution.



Graphics display systems are all built from identical construction blocks. A typical layout of a graphics display system is Aydin Controls System 16/10. Designed to operate in conjunction with a host computer, System 16/10 uses Aydin's Model 5216 Display Computer. The system receives data and commands from either the host computer or a keyboard.

Three buffer modules, or memory planes of 256 X 256 X 4 bits each have a final resolution of 256 X 256 X 12 bits. This resolution offers 65,536 pixels each of which can display 2^{12} (4096) colors/intensities.

As stand-alones, color-graphics terminals are used in such fields as small process control systems, graphic hard-copy generating systems, business management systems, design functions (CAD/CAM), art generation, and motion picture production.

As monitors, the terminals are used in plant/process control, building automation systems, geological exploration, and satellite information retrieval.

As system components, the terminals form part of SCADA systems, large process control systems, military command and control centers, equipment simulation displays for training, educational display stations, plant management automation systems, graphic display stations for management systems, hospital patients' condition monitoring, output for X-ray or CAT scans, CAD/CAM, 3D terrain maps, and electronic art. Prices for Aydin's product line begin at $3,500 for a stripped-down OEM output-only, and soar into the $100,000 field for a full-graphic system with a 16-bit word processor, 1 MB of memory and color capability up to 4096 through look-up table.

Graphics market forecasts predict a climb from the current $1.4 billion in sales to more than $4 billion in the next five years. Also seen in the future of this industry is an increase in software costs and a decrease in hardware costs.

CAD/CAM will, as always, capture the largest share of the expanding market. Costs for such systems will come down also as the cost for memory (a major factor in high raster-graphics costs) decreases steadily. This huge increase in the growing graphics market will affect the sales of graphics terminals. Technology will also be affected as higher resolutions are achieved and as panel displays emerge.

What does Aydin see in its crystal ball as it peers into the future? "Touch sensor screens for all CRTs. Full graphic overlays for alphanumeric terminals. Low-cost color terminals and systems for business applications. Voice input and output. OEM plug-in display modules. Faster, more efficient drawing and memory use. Graphics software packages including 3D and special applications."

The continuing growth of the computer graphics market can be measured by the increase in membership of the newly formed National Computer Graphics Association, 2033 M St. NW, Washington, DC. The November roll listed 1500 names, a 25% jump over its August enrollment figure. Writing in the NCGA Nov., 1980 Newsletter, Jerry Borrell, of the Congressional Research Service, Library of Congress, sees the decade of the 80's as the time when computer graphics will be entering the home through television channels.

"Information provision for the home is not a new concept," writes Borrell. "Newspapers, radio, and television have all been with us now for quite awhile. As the cost of providing these sources of information increases, and as newer means of providing information become more practical, computer graphics will become the basis for a new generation of information devices. Direct broadcasting by satellites and fiber optics, for instance, are making available data communications to the home which have been heretofore impossible. The reasons promoting the widespread use of computer graphics are obvious: consumers like pictures and color; they want hardcopy to crumple and fold; and if the convenience of tableshopping or other electronics message systems is added, they will expend their hard-earned resources to obtain such technology."

In an editorial in the same Nov. NCGA Newsletter, Editor Joel Orr described some current problems in the mushrooming industry. "There can be no doubt that computer graphics technologies are advancing rapidly", he wrote. "Nor can anyone deny the tremendous potential for productivity improvement implicit in these technologies – a potential convincingly evidenced by a growing army of satisfied users.

"On the other hand computer graphics is beginning to display the symptoms of a syndrome exhibited by its parent, computer technology: the false panacea syndrome. Like other patterns of promises unintentionally made and inadequately fulfilled, it leads rapidly to loss of credibility.

"Why is this happening? The answer to this question lies in a desire which is perceived as an inalienable right by most of modern American society: instant gratification. As computers did in the past, computer graphics seems to promise the solution to **all** business problems. The automatic production of beautiful colored pictures solves everything – doesn't it?

"In fact it does not. Generally, the wrong issues are being addressed. Methods for understanding problems are being ignored. The **technology** is receiving too much attention. We have, by and large, forgotten that the solution of business problems requires systematic thinking. We want to buy a piece of technology that will solve our problems, plop-fizz. But technology is not the problem.

"Here are some guidelines for focusing on the **right** issues – helping to keep computer graphics in its place, serving business.

"1) Computer graphics can't solve any business problems. *People* solve business problems. Computer graphics is a tool people can use. 2) Automating a business system will not make it better; it may not even make it faster. Systems must be systemized **prior** to being automated. 3) In business graphics, the right questions are: Which data should be graphed? Why? In what form? How often? Off-the-shelf technology is available over a broad spectrum of cost/future tradeoffs. Once the right questions are answered, selecting the appropriate software and hardware is simple. 4) Computer graphics is still expensive and complex; less than it was, but much more than it will be in years to come. Waiting may be a good idea.

"As NCGA members, we are in the forefront of efforts to promulgate computer graphics technology. Let us also be the leading exponents of sanity in its application to business problems."

Graphics Terminal Manufacturers

For additional information on color graphics terminals write to the companies listed. A more complete listing of graphics terminals manufacturers is now being prepared. If you have not been named here and if you would like to appear in the newer, expanded listing, please send information on your products to New Products Editor, DIGITAL DESIGN, 1050 Commonwealth Ave., Boston, MA 02215.

Grinnell Systems; 2159 Bering Drive; San Jose, CA 95131

TeleVideo Inc.; 2149 Paragon Dr.; San Jose, CA 95131

Magnavox Display Systems; 2131 S. Coliseum Blvd.; Ft. Wayne, IN 46803

Tec, Inc.; 2727 N. Fairview Ave.; Tucson, AZ 85705

Beehive International; 4910 Amelia Earhart Dr.; Salt Lake City, UT 84116

GR Electronics Ltd.; 1640 Fifth St.; Santa Monica, CA 90401

Spatial Data Systems, Inc.; PO Box 249; 508 S. Fairview Ave.; Goleta, CA 93017

Information Technology; 56 Kearney Rd.; Needham, MA 02194

Hitachi America, Ltd.; 100 California St.; San Francisco, CA 94111

Soroc Technology; 165 Freedom Ave.; Anaheim, CA 92801

Audiotronics Video Display Div.; 8299 Central Ave., NE; Spring Lake Pk., MN 55432

Ann Arbor Terminals, Inc.; 6107 Jackson Rd.; Ann Arbor, MI 48103

Megatek Corp.; 3931 Sorrento Valley Blvd.; San Diego, CA 92121

Sanders Associates Inc.; Daniel Webster Hwy.; Nashua, NH 03061

Andromeda Systems, Inc.; 900 Eton Ave.; Canoga Park, CA 91304

DeAnza Systems Inc.; 118 Charcot Ave.; San Jose, CA 95131

Aydin Controls; 414 Commerce Drive; Fort Washington, PA 19034

Comtal; PO Box 5087; Pasadena, CA 91107

Genisco Computers; 17805 Sky Park Circle Dr.; Irvine, CA 92714

Advanced Electronics Design, Inc.; 440 Potrero Ave.; Sunnyvale, CA 94086

Colorado Video; PO Box 928; Boulder, CO 80306

Lexidata Corp.; 37 North Ave.; Burlington, MA 01803

Industrial Data Terminals Corp.; 1550 W. Henderson Rd., Columbus, OH 43220

Zentec Corp.; 2400 Walsh Ave.; Santa Clara, CA 95050

Ramtek Corp.; 2211 Lawson Lane; Santa Clara, CA 95050

Stanford Technology Corp.; 650 N. Mary Ave.; Sunnyvale, CA 94086

Lear Siegler; 714 N. Brookhurst St.; Anaheim, CA 92801

IBM; 1133 Westchester Ave.; White Plains, NY 10604

Ontel Corp.; 250 Crossways Park Drive; Woodbury, NY 11797

Watkins-Johnson; 333 Hillview Ave.; Palo Alto, CA 94304

Objective Design Inc.; Box 20325; Tallahassee, FL 32304

Selanar Corp.; 2403 DeLaCruz Blvd.; Santa Clara, CA 95050

International Imaging Systems; 650 N. Mary Ave.; Sunnyvale, CA 94086

Datacube; 670 Main St.; Reading, MA 01867

Bell and Howell (CEC Div.); 360 Sierra Madra Villa; Pasadena, CA 94111

Fernseh Display Devices (Bell & Howell); 4000 Birch St.; Newport Beach, CA 92660

Adage; 1 Fortune Drive; Billerica, MA 01821

Advanced Technology Systems; 17-01 Pollitt Drive; Fair Lawn, NJ 07410

Control Data Corp.; 2401 N. Fairview Ave.; Roseville, MN 55113

Digital Equipment Corp.; 146 Main St.; Maynard, MA 01754

Evans & Sutherland Co.; 580 Arapeen Drive; Salt Lake City, UT 84108

General Dynamics; (Electronics Division,) PO Box 81127; San Diego, CA 92138

Hazeltine Corp.; Greenlawn, NY 11740

Imlac Corp.; 150 A Street; Needham, MA 02194

Information Displays; 709 Westchester Ave.; White Plains, NY 10604

Lundy Electronics Systems, Inc.; 28 Park Pl; Paramus, NJ 07652

Raytheon Data Systems; 528 Boston Post Road; Sudbury, MA 01776

Three Rivers Computer Co.; 160 N. Craig St.; Pittsburgh, PA 15213
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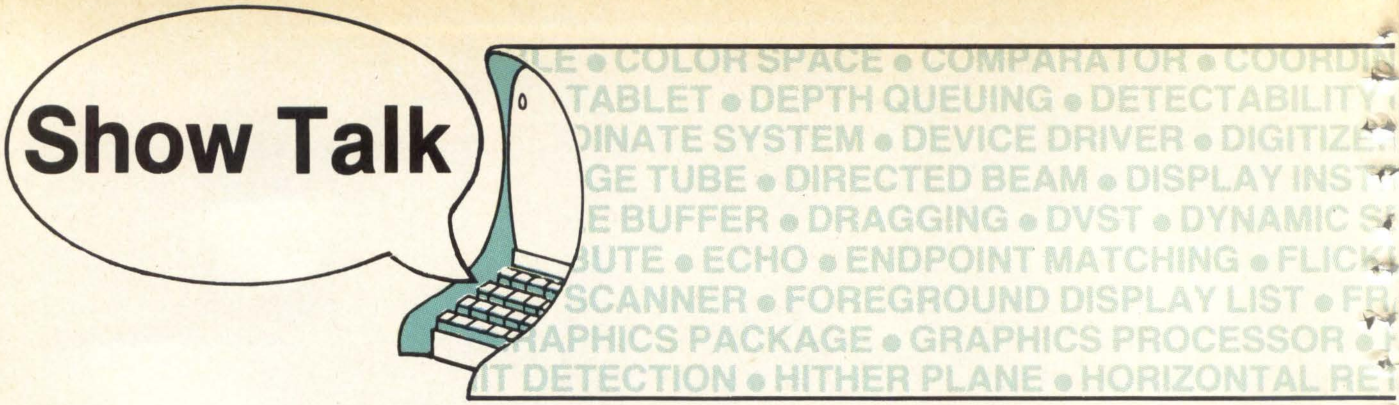

The field of computer graphics requires the use of its own special vocabulary, just as do the specialized fields of semiconductors, power supplies, disk drives, etc. The following definitions have been extracted from Megatek's (Megatek Corp., 3931 Sorrento Valley Blvd., San Diego, CA 92121) complete "glossary of Computer Graphics Terms."

Absolute Vector — Vector whose endpoints are defined in terms of units from the specified origin.

Addressability — Range of Addressable Points or Device Coordinates.

Beam Penetration CRT — CRT Display which produces color by varying the electron beam penetration of a multi-layer Phosphor Display Surface.

Bit Map — Digitized representation of a Display Image as a pattern of bits, where each bit maps to one or more Pixels. Multiple bit maps may be used in color graphics to assign values to each Pixel, which are used as indices into the Color Look-Up Table, if one exists.

Blackness — Characteristic of a color defining its percentage difference from a gray of the same Whiteness.

Blanked Region — Bounded area in Display Space, inside which Display Elements are not visible.

Bounding Box — Rectangle with dimensions the same as the width and height of a symbol.

Boxing — Visibility test incorporated in Clipping which uses a Bounding Box to test whether an entire symbol is outside the Clipping Boundaries.

Buffer — Storage area which receives and subsequently releases transient data.

Calligraphic (or Stroke Writing) — Line drawing, as opposed to Raster Scan.

Center of Projection — The common point from which all Projectors emanate in a Perspective Projection.

Character Generator — Hardware device which accesses character patterns in a ROM and generates them at specified Display Surface positions.

Clip Boundary — Boundary in Display Space, beyond which any portion of a Display Element will not be visible.

Clipping — Process of determining which portion or portions of a Display Element lie outside the specified Clip Boundary and making them invisible.

Coded Graphics — Specification of a Display as a set of Display Instructions.

Coherence — A property used in Raster Scan which recognizes that if a given Pixel is visible or invisible, adjacent Pixels are likely to be the same.

Color Look-Up Table (or Color Map) — A table designed to provide a range of colors by defining different mixtures of the red, green, and blue color components. A component in indirect color specification schemes, where colors are specified in terms of elements in the table.

Color Space — Conceptual geometric model that describes the characteristics of color (Hue, Whiteness, Blackness).

Comparator — Device that compares the proximity of a Cursor to the Vector currently being drawn.

Coordinate — Location of a point in terms of units from the specified Origin.

Core — A proposed graphics standard developed by the ACM Special Interest Group on Graphics (SIGGRAPH).

Data Tablet — Flat surfaced Graphic Input Device used with a Stylus for Inking and Cursor movement, or with a Puck for digitizing.

Depth Queuing — Technique used to suggest depth in a three dimensional Display Item by varying Intensity Levels in relation to distance from the viewer.

Illustrated by Jacky Brill

Detectability — A Dynamic Segment Attribute which determines if Display Items can be picked by a Pick Device.

Device Coordinate System — A coordinate system which represents the internal digital limits of the Display Device (Output).

Device Driver — Device dependent software which generates Display Instructions from the invocations of a Graphics Package.

Digitizer — A Data Tablet that generates coordinate data from visual data through the use of a Puck.

Direct View Storage Tube — A type of CRT with extremely long Phosphor Persistence.

Directed Beam — The technique to produce Vectors by having the electron beam stroke them in a selected order.

Display Instruction — The coded information specifying the Vectors and Characters to be drawn on the Display Surface.

Double Buffer — Technique used to speed data access by alternatively addressing two Buffers. When one Buffer is passing data, the other can receive data to be transmitted in the next access.

Dragging — Moving a Display Item by Translating it along a path determined by a Graphic Input Device.

DVST — Direct View Storage Tube

Dynamic Segment Attribute — The Attributes of a Segment which can be changed after its creation (Visibility, Highlighting, Image Transformation, and Detectability.)

Echo — The mode of a Graphics Input Device which provides visual feedback to the Operator (Cursor, text strings, etc.)

Endpoint Matching — Accuracy of the Vector Generator in drawing two or more Vectors emanating from the same point.

Flicker — Noticeable dimming of the Display prior to each Refresh, caused when the Refresh Rate exceeds the Phosphor Persistence.

Flying Spot Scanner — Device for scanning a picture to record it as a Pixel Array.

Foreground Display List — Display List whose Refresh is time-critical. May be Refreshed several times for each Refresh of a Background Display List.

Frame — One Refresh of a Raster Display Image.

Graphics Package — Series of software subroutines which provides the user access to the graphics hardware for generating a Display.

Graphics Processor — A controller which accesses the Display List, interprets the display data, and passes Coordinates to the Vector Generator.

Hidden Lines — Line Segments which should not be visible to a viewer of a three dimensional Display Item because they are "behind" other parts of the same or other Display Items.

Hit Detection — The returning of a Pick Stack when a valid Pick is made by a Graphic Input Device.

Hither Plane — The front clipping plane used in Z-Clipping to define a finite View Volume.

Horizontal Retrace — Turning off and repositioning the Electron Beam down and to the left during Raster Scan to begin the sweep of the next Scan Line.

Hue — A characteristic of color defining its gradation.

Intensity Level — One of a discrete set of brightness levels attainable with a CRT.

Interlace — A Raster Scan technique which alternately Refreshes the even and odd Scan Lines with each pass.

Mapping Function — Method of transforming an Image definition expressed in one Coordinate system to another.

Marker — User defined symbol which can be invoked repeatedly on the Display Surface.

Memory Management — Scheme used to allocate a memory to the Segments composing a Display List.

Menu — List of program execution options appearing on the Display Surface which prompts the user to choose one or more through the use of a Graphic Input Device.

Momentary — Mode setting for Function Switches which places a switch in an active state only while it is depressed by the user.

Mouse — Rounded hand held device used with a Data Tablet that positions a Cursor on the Display Surface by the movement of two wheels against the tablet's surface, one for the X Coordinate and one for Y.

Move — To reset the Current Position without producing an Output Primitive.

New Frame Action — Refresh of the Display Surface which produces an updated Display.

Non-Interlace — Raster Scan technique which Refreshes every Scan Line with each pass.

Non-Retained Segment — The Segment which is open when all Retained Segments are closed, and whose Segment Attributes cannot be modified.

Normalized Device Coordinate Space — Addressable area defined in terms of Normalized Device Coordinates.

Normalized Device Coordinates — Device independent Coordinates in the range of 0 to 1 which are mapped to the Device Space.

Orthographic Projection — Parallel Projection whose direction is determined by a Vector perpendicular to the View Plane.

Painting — Technique similar to Inking, but used only on Raster Displays where Line Width and color may vary.

Parallel Projection — A projection in which the Projectors are all parallel to a specified Vector.

Passive Graphics — Method allowing no Operator dynamic interaction with a Display.

PEL — Picture element. (See Pixel.)

Perspective Projection — Projection in which the Projectors all originate at a specified Center of Projection.

Phosphor — Chemical coating on the Display Surface of a CRT which glows when excited by an electron beam.

Phosphor Persistence — Measure of time it takes for a Phosphor's brightness to drop to one-tenth of its initial value.

Pick — An Event triggered by a Pick Device which generates an Event Report (Pick Identifier of the detected Display Item and name of Segment containing it.)

Pick Device — Event Device, such as a Light Pen or a Locator Device with a Comparator, which causes Picks when pointed at Detectable Display Items.

Pixel — Discrete Display Element of a Raster Display, represented as a single point with a specified color or Intensity Level.

Plasma Panel — Type of CRT whose Display Surface consists of a matrix of points which can be turned on and off individually, and which remain "on" until turned "off".

Point — A Line Segment of zero length.

Projector — A line passing through an Object to intersect with the Viewplane in a projection.

Puck — Hand held device with a transparent portion containing crosshairs. Used for inputting Coordinate data from a Data Tablet through the use of programmable buttons.

Raster Scan — Generation of a Display on a Raster Display by having the electron beam follow a set pattern through the Scan Lines, applying varying color or intensities to each individual Pixel.

Refresh — Process of repeatedly drawing a Display on the Display Surface of a Refresh Tube.

Relative Vector — Vector whose Endpoints are specified in reference to the Current Position.

Repeatability — Accuracy of the Vector Generator in minimizing the deviation from precise overlap when redrawing Vectors.

Resolution — The precision of a CRT, measured as its Addressability.

Retained Segment — A user named and defined Segment whose Segment Attributes may be modified at any time.

Run Length Encoding — A Scan Conversion technique to compress Scan Line information by storing counts of number of identifical consecutive Pixels and their respective colors or intensities across each line.

Roam — To translate a Window about the View Plane.

Rotate — To transform a Display or Display Item by *revolving it around* a specified axis.

Sample — To query a Graphic Input Device to determine if any inputs have occurred since the last query.

Scan Line — Horizontal line of Pixels on a Raster Display that is swept by the electron beam during Refresh.

Scan Conversion — Process of converting a Display to a Bit Map.

Segment — Named portion of Display List that defines a Display Item.

Selective Erase — Ability to delete portions of a Display without affecting the remainder.

Shadow Mask — A metal plate positioned behind the Display Surface of a color Raster Display and pierced with small holes. When the Triad is focused on holes, the electrons from each gun only strike their respective Phosphors.

Shielding — An opague Viewport or Window in which to display a Menu, a title, or a message to Operator.

Soft Copy — Copy of a Display in video form, as on videotape.

Storage Tube — A CRT which maintains a Display on the Display Surface without Refresh.

(continued on page 77)

Advanced Raster Display Techniques

Peter Shaw
Megatek Corp.

Typical of today's sophisticated color graphics displays is a new unit from Megatek. The WHIZZARD 6250 system is a 13-inch color raster monitor packaged in a desk style cabinet complete with keyboard and joystick. Its 14-slot chassis includes a 32-bit graphics processor, vector memory, intelligent RS-232 serial asynchronous interface, high speed digital vector generator, raster memory, video output circuitry, and room for optional modules. Available options include additional vector memory, a hard copy output interface and a data tablet input interface. This new unit provides dynamic line drawing capabilities for use in distributed CAD/CAM applications.

CAD/CAM graphic systems generally are used for automating design, drafting, engineering and manufacturing tasks. The benefits of using such systems include large savings in time plus significant improvements in productivity. This results in better new product development lead times; savings resulting from engineering analysis performed in simulation, not in trial and error manufacture; better quality of designs due to improved dimensional accuracy; and better utilization of materials.

In the past, the most common graphics display used in CAD/CAM systems was the storage tube, primarily because of its low cost. But a tradeoff had to be made for that low cost, because storage tube terminals did not offer multiple colors, were slow in drawing screen images, and had little dynamic interaction between the operator and the terminal on-line design and analysis tasks. Most importantly, the storage tube did not allow "selective erase". Once a drawing has been made on the storage tube screen, the entire picture must be re-drawn if any element of the picture is to be changed. This means that although an engineer can draw high resolution designs, the process is slowed tremendously by the inability to interact dynamically with the screen image and to change it easily for design analysis. This has led to a "hit REPAINT and drink a cup of coffee" syndrome among design engineers.

High performance vector refresh and linedrawing color raster graphic systems provide these benefits but they usually cost more – anywhere from $30,000 to more than $100,000. The introduction of the 6250 changes the picture dramatically.

Market growth

In 1979, more than 50,000 graphic terminals were shipped, totalling about $280 million in sales worldwide. Of these, one fourth were high performance displays and three fourths were low cost storage tube or raster types. By the end of 1984 this total graphics display market is expected to have grown at a compounded annual rate of 35% to a total of more than $1.1 billion in annual size. However, the breakdown by performance will have changed. One fourth of this total will still be high performance, high cost displays. The remainder will be low cost terminals. But there will be a noticeable improvement in how much work can be done with new types of low cost, low performance terminals of today to provide new levels of capability for a broad variety of engineering needs.

A recent study has shown that there are just over one million engineers in the United States and of these, more than 85% are involved in electrical, mechanical, civil and industrial engineering – all prime users or prospects for CAD/CAM systems. The study theorizes that the U.S. market for these systems in the top four engineering areas alone amounts to an estimated 26,000 systems – each with anywhere from two to 16 display terminals.

Megatek has been able to incorporate into the 6250

Peter Shaw is V.P. of Megatek Corp., 3931 Sorrento Valley Blvd., San Diego, CA 92121.

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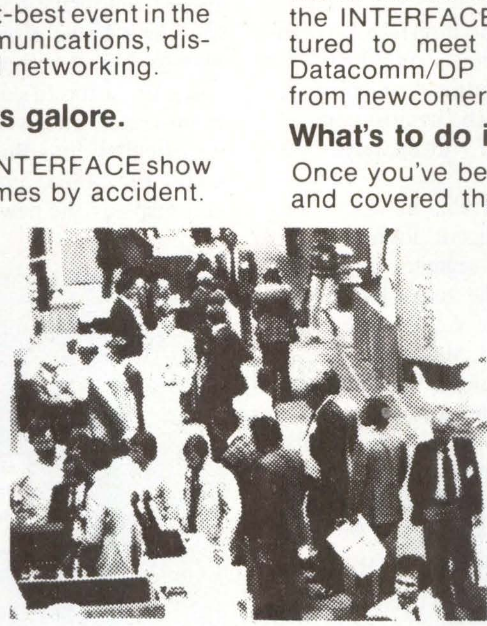

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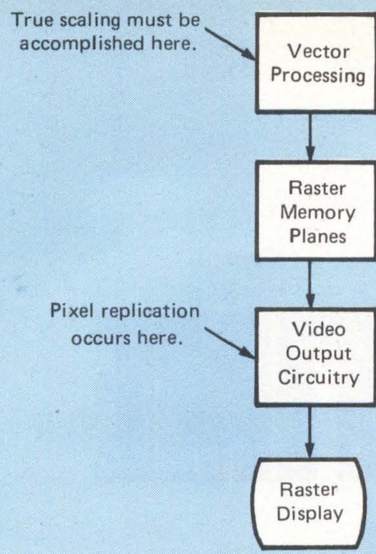

Figure 1: Vector to Raster Conversion Process

the advantages of vector (stroke) refresh displays. Not only does the 6250 have the color and high density (large vector count) display capabilities of traditional raster displays; it also has the dynamics of a stroke refresh system, allowing full-screen updates of complex images at rates far exceeding animation rates.

Features of new unit

The 6250 incorporates an intelligent interface for handling serial communications with the host computer. This interface uses a high-level communications protocol designed to minimize communications with the host computer, thus improving throughput and, ultimately, user productivity.

To further improve performance of this new unit and offload the host computer, the intelligent interface also handles all memory management and segment addressing in a way which is transparent to the user. By placing memory management functions in the 6250, a dramatic improvement in performance is achieved. Memory addresses do not have to be passed, since all segments and subsegments are addressed by a unique label. Unused memory is made available as required. When a portion of the display is deallocated, the memory is automatically made available for later use. All this is done locally in the 6250's intelligent, microprocessor-based interface, alleviating the host and its communications link from what would otherwise be serious time-consuming tasks.

Our vector-processing "Graphics Engine," combined with the very fast vector-to-raster conversion circuitry and double-buffered raster memory planes allows display update rates far beyond that available on other raster displays. The speed of the WHIZZARD 6250 produces features not available in other raster displays, including real-time pan and zoom, "selective erase", and "decluttering".

Display data is specified by vector endpoints in a 4096 X 4096 virtual space. Real time pan and binary zoom capabilities allow the user to perform true scaling locally and in real time. This is not the "pixel replication" of most other raster displays; it is a true scale, with more information being introduced to the screen as the operator zooms in on a portion of the 4096 X 4096 virtual space. By combining the translation and scaling facilities, the user can activate a real-time continuous pan through the virtual address space using a 512, 1K or 2K window.

Real-time scaling

MEGATEK achieves true scaling rather than the more common "pixel replication" by a unique combination of vector processing and vector generation techniques. All line-drawing raster displays incorporate some variation of the process pictured in Figure 1. First, vector endpoint data must be "Rasterized" to convert it to raster pixel information. This pixel data is then stored in the raster memory planes. Memory planes are then read, scan-line by scan-line, by the video output circuitry to accomplish the refresh of the raster display. Scaling can be done at either of two times in this process. The first and best place to accomplish scaling is during the vector processing cycle. This allows true scaling of vectors, with scaled vectors being then "Rasterized" and written into raster memory planes for display.

MEGATEK achieves true scaling in the 6250 by increasing the speed and ease of the vector processing cycle and modifying the way raster memory is organized. The display list of vector endpoint data maintained locally in the 6250 avoids the need to retransmit vector information from the host computer. The vector processing and rasterization circuitry speeds the execution of complex graphic instructions.

Another feature of the WHIZZARD 6250 is its "double-buffering" of the raster memory planes (figure 2). Double buffering allows regeneration of modified displays without erasing the image on the display screen. On a typical cycle, the image being displayed is contained in Buffer 1. The display is being refreshed from this buffer. While this is going on, a modified image (perhaps scaled and translated) is processed and written by the high-speed vector processing circuitry into Buffer 2. When vector processing is complete, the video output circuitry starts reading Buffer 2 and displays the new information without the need to erase

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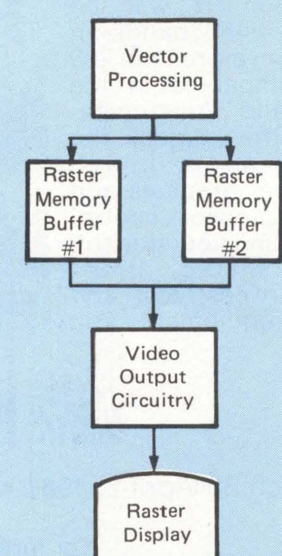

Figure 2: Vector to raster conversion process as implemented in the WHIZZARD 6250 using double-buffered raster memory. The display is refreshed from one buffer while display updates are written into the other buffer. When updates are completed, the display toggles to the new buffer for refresh.

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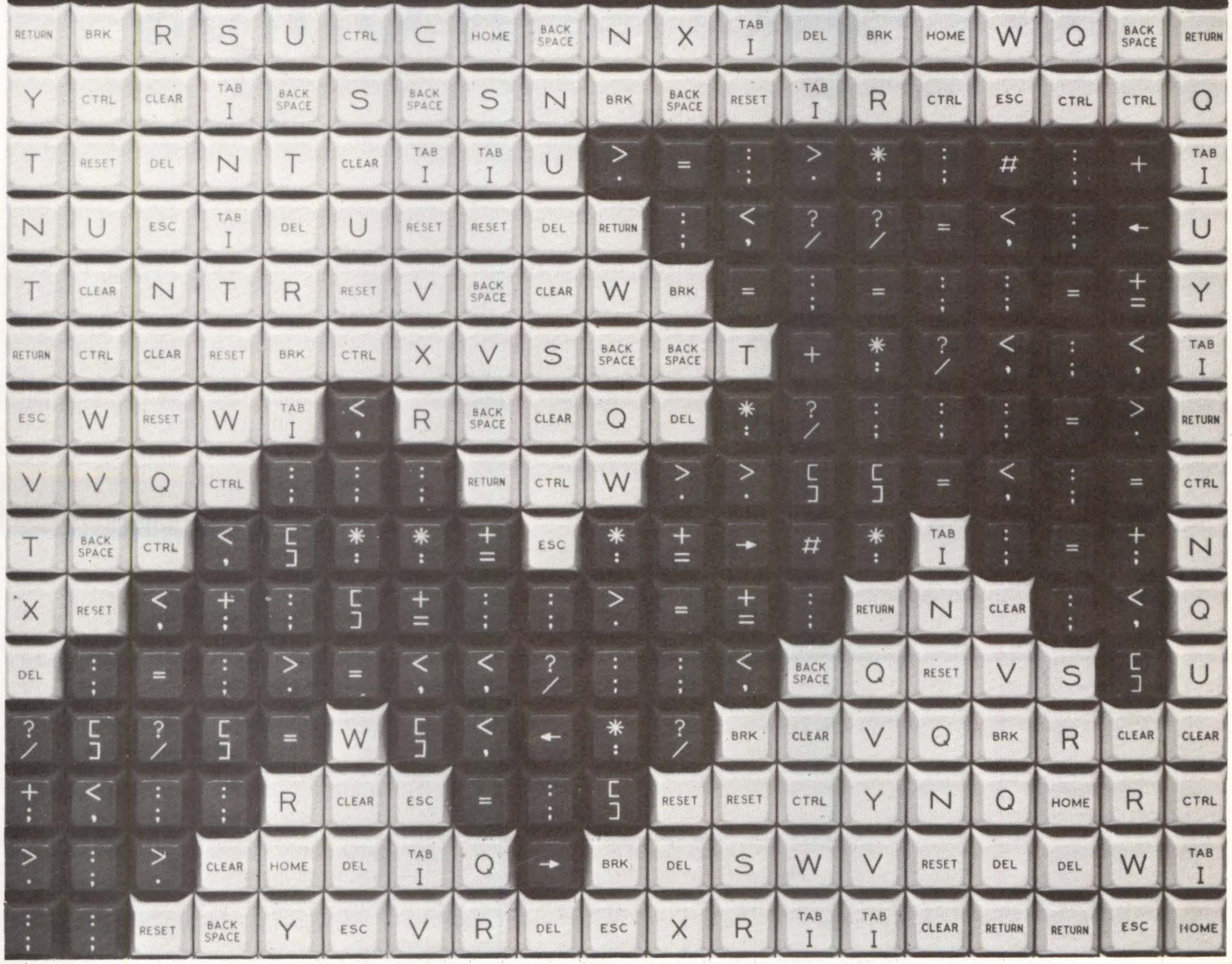

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NCC '81

IC Peripheral Chips

Joseph H. Kroeger
Advanced Micro Devices, Inc,
Sunnyvale, CA 94086

Integrated circuit peripheral devices (ICPDs) belong to two classes: those that collapse interface functions, such as peripheral and communication controllers, and those that improve system performance, such as hardware floating-point mathematic units. Neither area is rigidly defined; some devices fit both categories. But all ICPDs have one thing in common: improving the cost/performance of processor-based systems.

Why make a processor with microsecond instruction wait for a peripheral that takes milliseconds to transfer data? Soon the processor will be spending 90% of its time waiting for data and only 10% doing useful work. By acting as a buffer between the CPU and the peripheral device, a peripheral interface can help solve this problem.

In its simplest form, the interface might be a register or latch that accepts data at CPU speeds and outputs it at peripheral speeds, or vice versa. However, interfaces range widely in complexity and programmability.

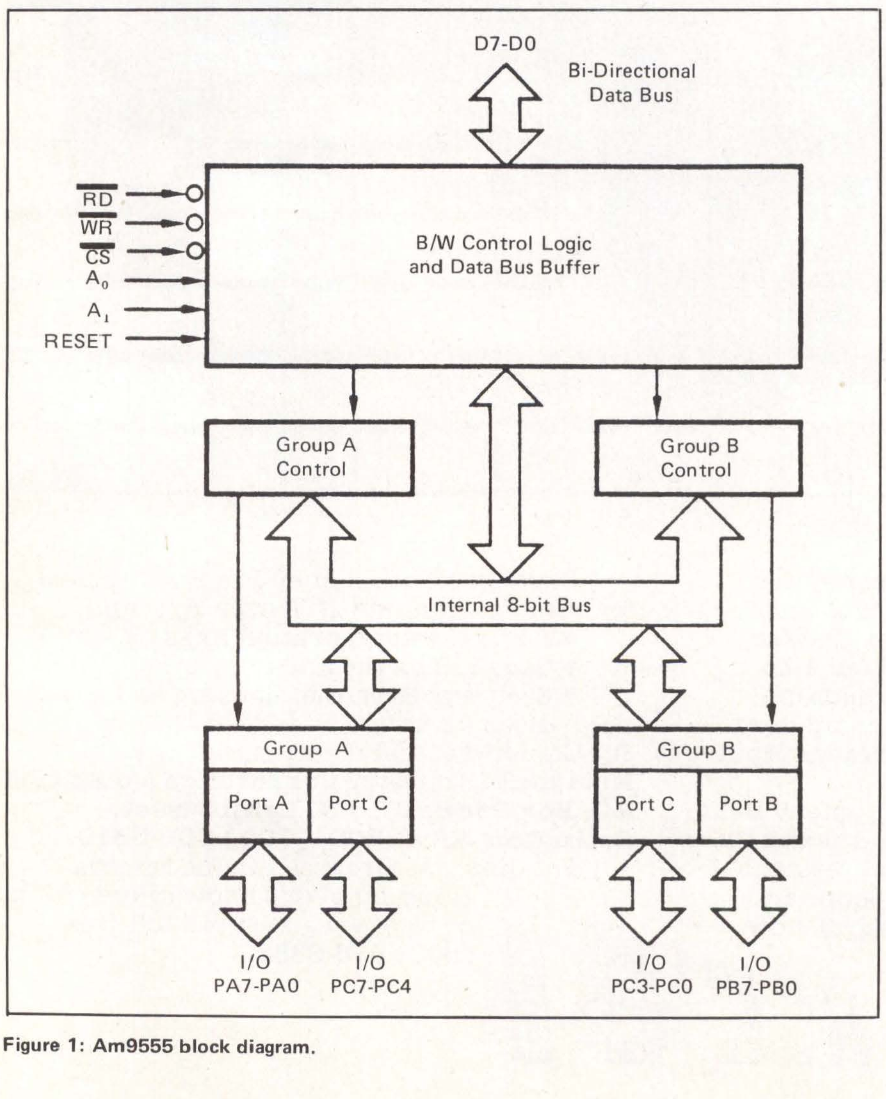


Figure 1: Am9555 block diagram.

Programmable peripheral interfaces

Besides simplifying processor-to-peripheral interfacing, the programmable peripheral interface (PPI) expands the number of available I/O lines. For example, the Am9555 PPI connects one 8-bit bidirectional μP bus to 24 I/O pins serving as inputs, outputs or both under program control. It acts as both information buffer and electrical buffer because it can latch data in either direction and can handle a higher sink and source current than the CPU.

Some programmable ICPDs contain little internal intelligence; the CPU must transmit explicit commands and command sequences through the interface to the peripheral. But the Am9555, for example, is general and can be used with many types of peripherals.

As the peripheral circuit becomes smarter, it can become more limited in scope because it grows more specialized. Some peripherals have become orders of magnitude more complex than the simple PPI; they can even be more complex than the processor they serve.

Peripheral controllers

One intelligent interface is a peripheral controller (such as a floppy disk controller) that provides the

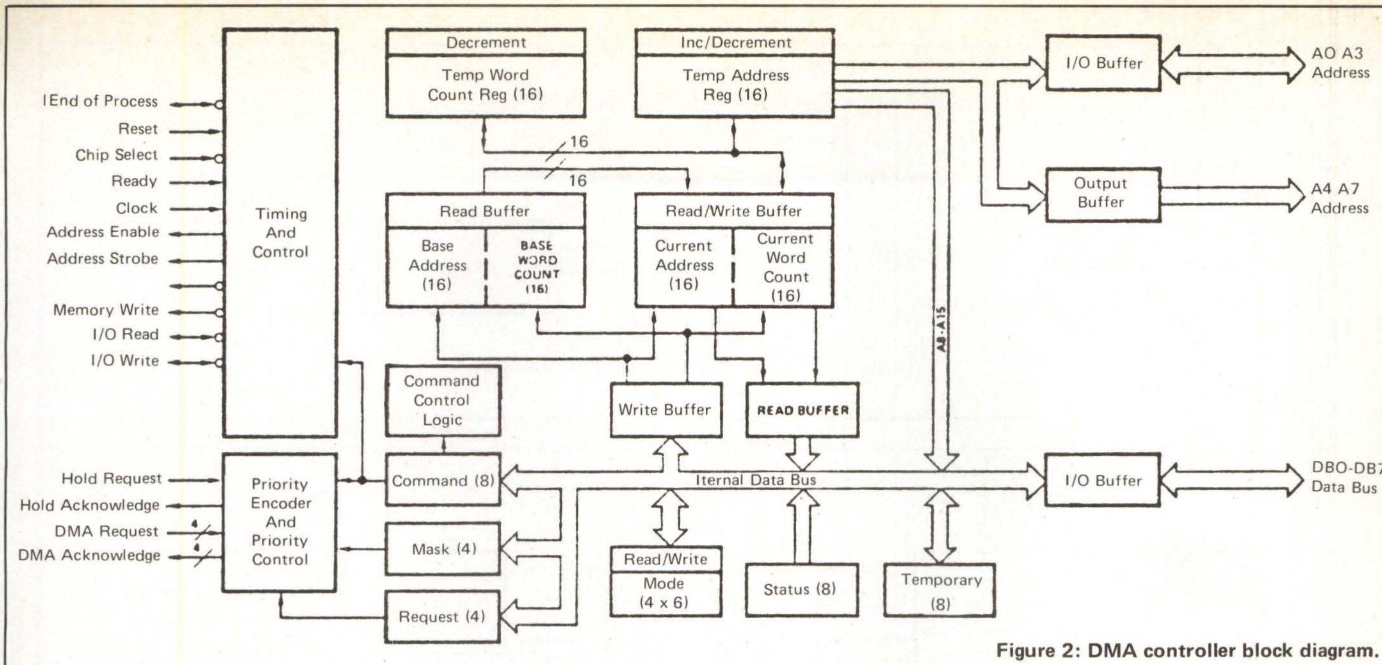


Figure 2: DMA controller block diagram.

essential timing and control signals and sequencing logic previously handled by the CPU, as well as data buffers for the peripheral device. This often reduces the CPU function to supplying the necessary command and appropriate data or data addresses. The interface decodes the command and initiates a series of actions to execute it, allowing the CPU to proceed to another task.

A variation of this type of interface is the DMA controller illustrated in **Fig 2**. This block diagram of the Am9517 shows all the interface signals, the internal functional blocks and their data interconnection.

Long a feature of minicomputer and mainframe computer architecture, DMA provides data transfer between system memory and peripheral devices at speeds exceeding those obtainable under CPU control. This method bypasses the CPU, creating a direct path between memory and the peripheral device.

DMA capability can significantly enhance throughput performance. Because a CPU reads an instruction from memory, decodes it, performs any address calculations necessary to locate operands, and then executes the specified operation, it may take several instruction fetch/execute sequences to transfer each byte or word. For repetitive sequential data movement operations, DMA removes the CPU from the transfer path, simplifying the normal fetch/execution steps.

Fig 3 illustrates a data acquisition subrouting flow chart. The subroutine transfers bytes of data from an external source into successive memory locations. The main loop consists of

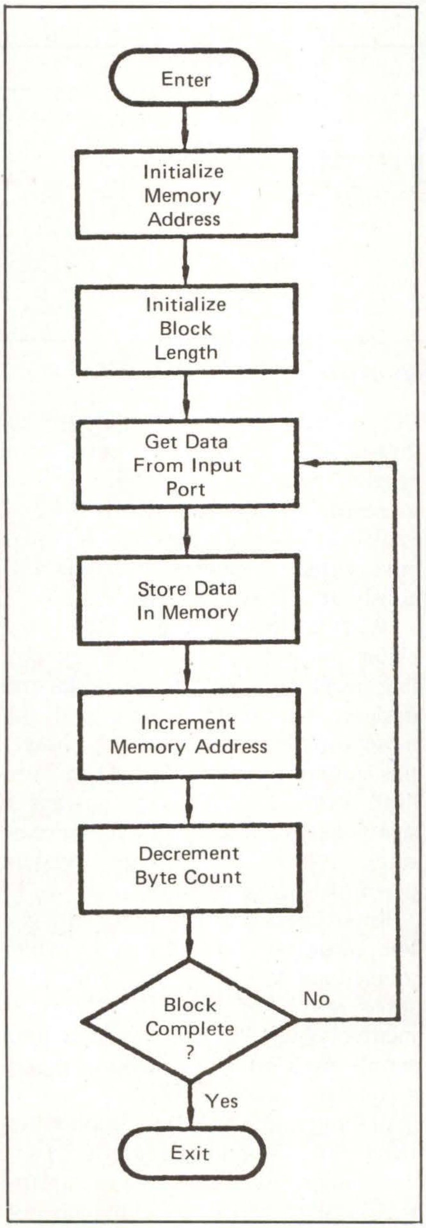


Figure 3: Data block transfer routine.

several instructions requiring many clock cycles for each word transferred.

However, much overhead can be eliminated by specialized hardware logic that provides access to system memory without CPU intervention. DMA replaces software loop functions with dedicated hardware, reducing cycles required/word transferred and dramatically increasing information transfer rate.

Fig 3's flow chart, coded in 8080A/8085 assembly language, shows a more concrete comparison. The transfer loop takes 10 bytes of program and executes in 46 clock cycles/byte. The same task executed in the Am9517 requires more initialization time but produces a transfer loop taking only 3 clock cycles/byte.

MOS/LSI's ever increasing density has put the logic required in a multichannel DMA controlller on a single chip, while allowing μP evolution into sophisticated computing elements. As such processors are called on to support more complex applications, DMA capability will keep improving system performance.

Display/keyboard interfaces

Another example of integraring interface operations, the Am8279 Display/Keyboard Interface **(Fig 4)**, puts two functions on the same bit of silicon. Am8279 is a general-purpose programmable keyboard and display interface circuit designed for several types of μPs. The keyboard interface can be used with a sensor array or with strobed keys such as the Hall-effect and Ferrite variety. Key depressions can be 2-key-lockout or N-key-roll-

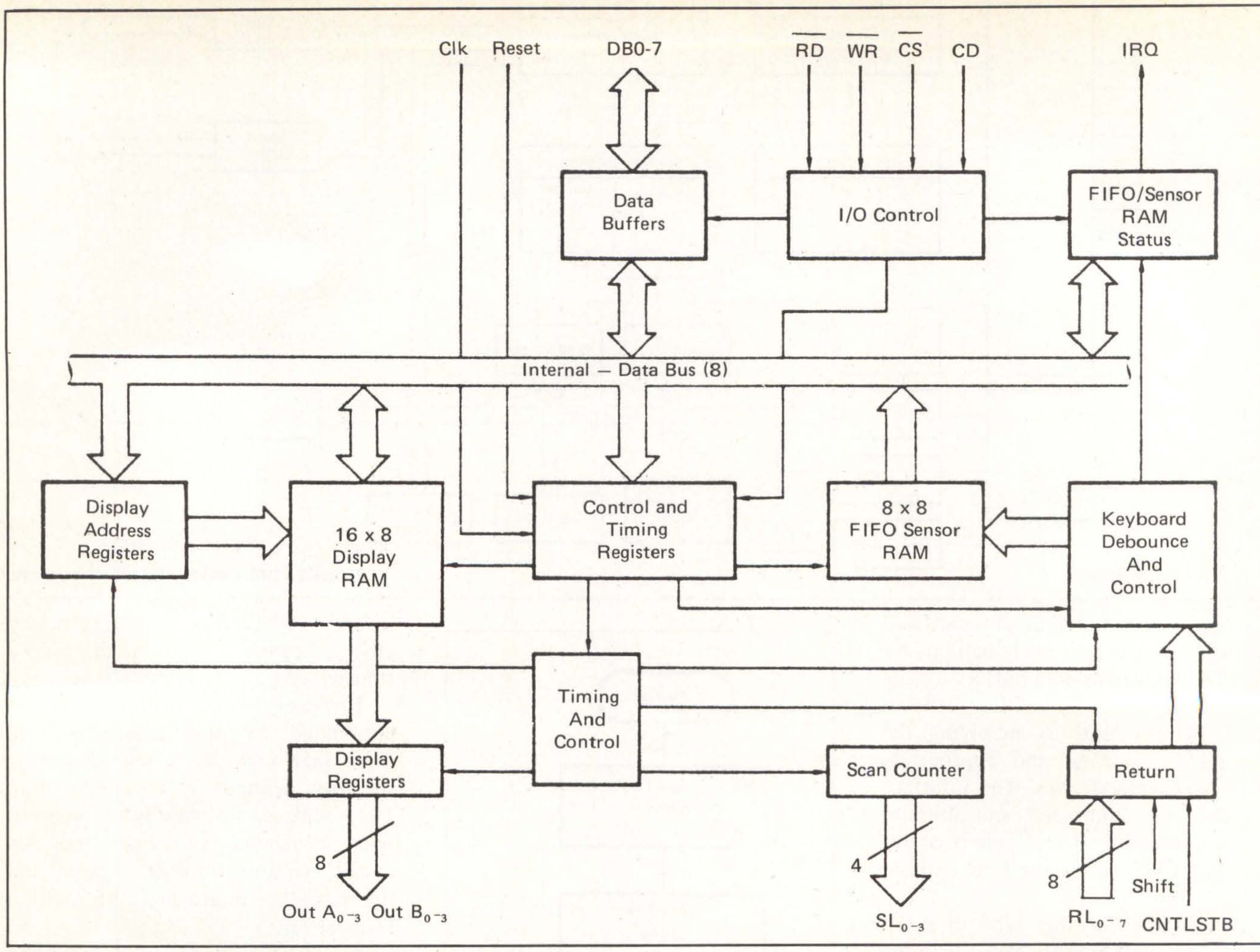


Figure 4: Am8279 keyboard/display controller block diagram.

over. Key entries are debounced and stored in an 8-character FIFO. Overrun status is set if more than 8 characters are entered.

This chip's display section provides a scanned display interface for various display technologies. Numeric and alphanumeric displays can be used, as well as simple bit indicators. The Am8279 has a 16 x 8 display buffer that can be loaded or interrogated by the associated processor. Right-entry calculator and left-entry typewriter formats can be used.

Interrupt controllers

An interrupt controller shown in **Fig 5**, is a more intimate part of the CPU function than typical peripheral interfaces. Processors are tools for implementing system transfer functions; processor systems include at least one peripheral device to communicate with system user. The processor not only manipulates information in the system, but handles its transfer to and from peripherals. All I/O devices must be serviced by the processor.

Processors initiate and coordinate I/O activity via program-controlled service or interrupt-driven service. In program-controlled transfers, the processor schedules all peripheral events; an interrupt-driven system permits external devices to asynchronously modify system activities.

With no interrupt capability, processors must depend on software polling techniques to service peripheral devices. The more devices and the more complex the service, the longer the polling program takes. The overhead devoted to polling becomes a significant fraction of available processing resources, limiting system performance.

Interrupts enhance processor system throughput and response time by minimizing or eliminating the need for software polling procedures. An elementary single interrupt could be used simply to alert the processor that a service is desired and thus to initiate a polling routine. More complex systems may have multiple interrupts and vectoring protocols to further improve performance and often eliminate polling requirements.

A processor support device that enhances the interrupt capability of many processors, the Am9519 Interrupt Controller manages the masking, priority resolution and vectoring of up to eight interrupts. It can be expanded by adding other Am9519 chips to handle a nearly unlimited set of interrupt inputs.

The Am9519 provides any mix of 1-, 2-, 3- and 4-byte responses to the host processor during the interrupt acknowledge process. The response bytes are all fully programmable; any appropriate addressing, vectoring, instruction or other message protocol can be used. Contention among multiple interrupts is managed internally with either fixed or rotating priority resolution circuitry. The direct vectoring capability of the Am9519 can be by passed with the polled-mode option.

An internal mask register permits individual interrupts to be disabled. It can be loaded in parallel by the host processor with any bit pattern, or mask bits can be individually controlled. The interrupt inputs use "pulse-catching" circuitry so that an external register is not needed to cap-

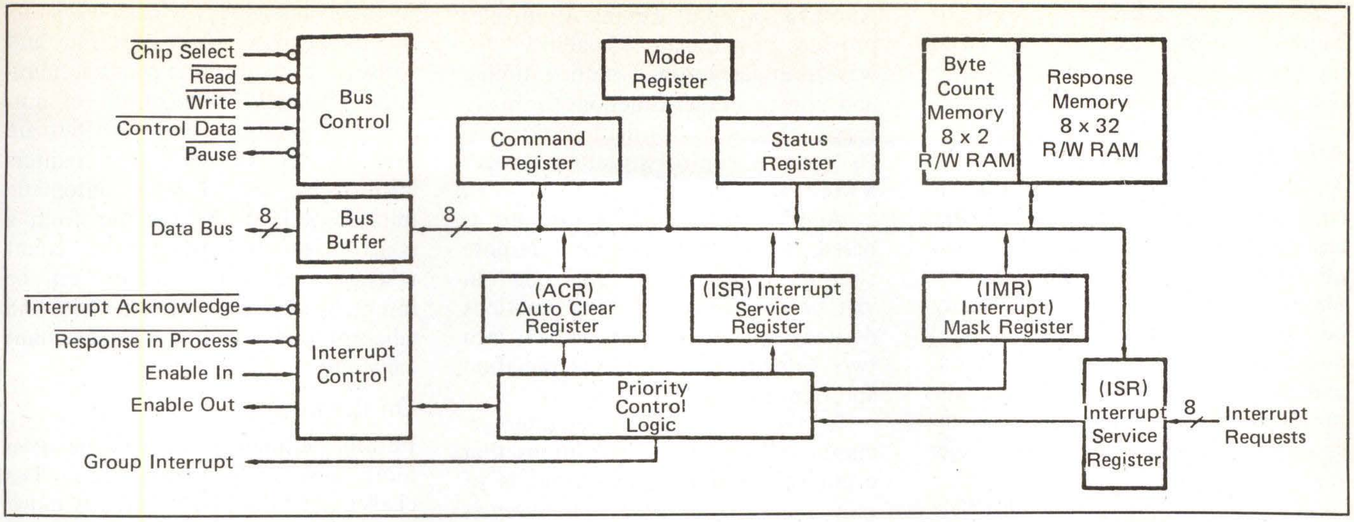


Figure 5: Am 9519 interrupt controller block diagram.

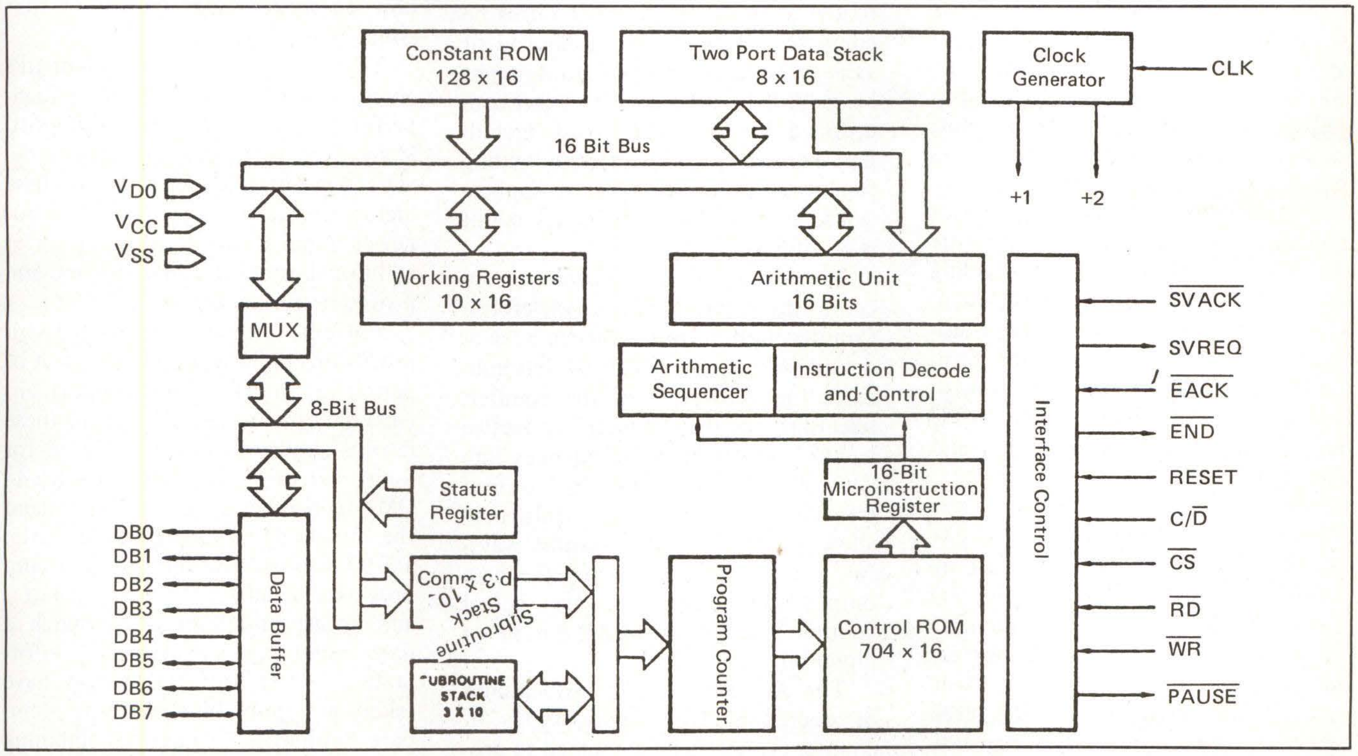


Figure 6: Am9511 arithmetic processing unit.

ture transient interrupts. Narrow noise pulses, however, are ignored. The interrupt polarity can be selected as active-high or active-low.

The Am9519 also handles software interrupts. The host processor can set interrupt requests under program control, permitting hardware to resolve the priority of software tasks.

All the above devices are specialized MOS/LSI devices; despite their programmable versatility, they are designed for one task area. Bipolar interfaces are used where more output drive capability is required or where speed is paramount, such as in bit-slice μP designs. Typical parts include latches, transceivers, microprogram controllers, sequencers, word and address counters and bidirectional byte ports.

Preprogrammed single-chip micros

Recently, another LSI device has emerged in the interface area: the preprogrammed single-chip microcomputer. Most single-chip microcomputers find use as logic replacement and as dedicated controllers. Since they contain unique customer application software masked into their on-chip memory, they are usually custom chips.

Some manufacturers are now putting their own program on-chip to dedicate the microcomputer to a specific task. This way, the manufacturer only has to make one part and program it for each function, bringing the cost/function and design-time down. However, the chip must be more complex than a dedicated design, because not all features are needed for all functions. Furthermore, this approach is still a software solution and generally cannot match the performance of a dedicated design.

Redesigned μPs

A middle step between dedicated and fully programmable devices is the slightly redesigned microprocessor that adds needed functions and eliminates uneeded ones, such as the I/O processor. It grows out of multiprocessor systems in which two or more CPUs work together to increase bandwidth.

Gradually one CPU will begin to handle most data manipulation while the other handles I/O, leading to chip optimization.

Arithmetic processors

Another general class of peripheral circuits attacks the bottlenecks of typcial microprocessor systems. Most μP systems need some number manipulating ability, which usually occurs under software control and, depending on the nature of the data, and the operation, can require a few hundred to many thousands of instructions cycles – not fast enough for real-time systems.

For many math-intensive applications, μP evolution has come full circle. In the beginning, when CPUs were expensive and had speed to spare, everything was done in software. Since hardware costs keep falling, but software costs do not, more software functions are being cast in hardware.

A complex arithmetic processor contained within a single chip, the Am9511 Arithmetic Processing Unit (**Fig 6**) performs basic add, subtract, multiply, divide and transcendental operations. It offers both fixed- and floating-point modes with 16- and 32-bit precision. The CPU need only supply commands and data to the APU.

Timing controllers

Another system area susceptible to hardware integration is counting and timing. Manipulation and coordination of timing parameters and event sequences are universal system attributes. At the most fundamental levels of control, time sequences are intimately embedded in the essential hardware and interface concepts of all processors. At the interface level, both internal and external hardware coordination require several types of timing-oriented exchanges.

Time-related activities fall into many categories, including frequency generation, waveform duty-cycle control, event counting, interval measurement, precise periodic interrupts, time-of-day accumulation, delays and gap detection. Accomplishing several of these activities, especially concurrently, can consume a significant portion of the system's available processing resources. Throughput limitations easily arise.

A specialized circuit able to handle many types of counting and timing functions can simplify software and improve system performance. The Am9513 System Timing Controller provides significant capability for waveform generation, counting, timing and intervalometer functions for many types of processor-oriented systems. Its versatile control structure services a wide variety of applications.

Am9513 operating philosophy is based on the use of general-purpose counters that can be controlled in various ways to produce the functions desired. Use of the counters falls into two categories: count accumulation and frequency division.

In the first case, the counter accumulates a count of transitions that occur on its unput; an output is of only incidental interest. The counter value should be available at any time to the associated CPU or it might be compared with some independent value. The accumulated count might be modified or the counter input conditioned by various controls, including hardware and software gating functions. In these types of applications, the value of the actual count is of interest.

Frequency division, however, concerns itself with output waveform. Counter input information can be incidental. With an output signal that indicates the zero state of the counter, selection of the counter's effective length and the input frequency are controlled to provide desired output frequency. Additional controls may allow various types of output waveforms to be generated from the base output frequency, but the actual counter value will usually not be of direct interest.

The Am9513 handles both modes of operation. Often both types of counter usage will be combined to provide the desired function. A single Am9513 contains an internal oscillator and associated frequency-scaling circuitry plus five general-purpose 16-bit counters. Control circuitry supporting each counter allows it to be independently configured dor various tasks. figured for various tasks.

The internal frequency source is designed for use with an external frequency-determining crystal or other reactive network. The output of the oscillator is scaled so that five different internal frequencies are available for selection as inputs for each counter. Any internal frequency can be brought out for use in other parts of the system.

Each counter can be programmed to count up or down and in binary or BCD. Sixteen counting sources are available for each counter; input polarity is also individually selectable. Gating functions allow direct hardware and software control of the count accumulation. Several combinations of output configurations and polarities are available. Modulo control of counters is provided by allowing automatic initialization of the counter from a control register when the count reaches zero. Any counters can be internally connected in series with and adjacent one to form a larger count capability.

On the horizon

Future peripheral ICs will be even more complex than those today. The challenge will not be to see how much can be put on a single silicon chip, but how to make good use of all that could be put there.

The new generation of 16-bit μPs entering the market will need high-performance peripheral ICs as support. Many present system performance devices can interface directly to these high-performance processors, but newer families of devices will offer additional support functions and improved performance.

For example, the AmZ8000 16-bit processor family will include a host of peripheral interface and support circuits along with the CPU, among these devices similar to those produced for 8-bit systems, such as the CRT and DMA controllers. Others will expand the functions of recognizable parts: a CIO (central I/O multiplexor) chip providing parallel I/O ports, a counter and enough intelligence to match a data input against preloaded information (previously this would have taken a byte-by-byte software compare routine); a FIO device combining a 128-byte FIFO memory with an I/O port, bus interface and data matching; an SIO serial protocol chip providing two independent channels capable of handling synchronous, asynchronous or SDLC protocols, along with modem interfaces.

Most exciting will be the completely new parts, such as memory management units. While 8-bit μPs did not need memory management, the vast memory space of new CPUs, such as the 8 MB of the AmZ8000, will use an MMU to translate logical addresses to physical addresses.

While these devices represent a healthy start, new devices on the way will represent significant challenges for system designers. Users too will have interesting opportunities as they exploit the capabilities of available peripheral and support circuits.

Designers' Guide to Speech Synthesis

Jim Smith and Dave Weinrich,
National Semiconductor Corp.

Speech synthesis is an explosive growth area that designers must understand to use. Speech circuits offer a new dimension of sophistication to many modern machines.

This article describes the versatility and flexibility of low-cost speech and tone synthesis for products ranging from consumer items to computers.

A different approach . . .

One approach to speech synthesis samples, digitizes and compresses the speech waveform by 1) elimination of symmetrical redundancy and silent intervals, 2) the use of adaptive delta modulation, 3) the adjustment of phase information in the digitized speech, and 4) replacing the low level portion of a pitch period with silence (half-period zeroing). In this way, speech elements can be synthesized as phonemes, phoneme groups, words or even whole phrases. Also, the attributes of the original speaker can be maintained if the synthesized elements are not broken down incorrectly (i.e. inflection can modify the sound of a phoneme if it occurs at the end of a word or phrase rather than at the beginning).

In a speech compression system, unvoiced sounds are usually standardized. During the compression algorithm, voiced and unvoiced sounds are separated and the voiced sounds are compressed. Unvoiced sounds, however, are compared to available sounds and synthesized by substitution. This approach is successful because unvoiced sounds have very few speaker defined characteristics. As a result, a relatively small set of unvoiced sounds can be used repeatedly.

This speech compression technique offers excellent quality at a low data rate. Synthesis of a male voice, using English, will usually require an average of 1000 bits/word. Because the technique can be applied to any voice frequency signal, it is also capable of synthesizing women and children's voices, music and tones. This flexibility, plus the realistic quality of the synthesized speech, makes this technique attractive.

Speech processor chip (SPC)

Our speech synthesis consists of the SPC device plus the speech memory (ROM) required to assemble a complete "Digitalker" kit. To this kit a customer must add a clock input signal or necessary oscillator components, an audio filter and amplifier and control circuit function. This is the minimum configuration. The maximum amount of directly addressable speech memory accessible by the SPC is 128 Kbits, but external page addressing by the control circuit function can increase this ROM field as required. We use an elaborate computer program to analyze a high fidelity tape recording and generate a ROM pattern that faithfully synthesizes the original voice message.

SPC's eight-bit start address bus allows up to 256 separately-defined sounds or expressions to be stored in the speech ROM. The control interface to the start address port can take the form of decoding logic, a Microbus port or mechanical switches. When the WR goes high, the start address code is loaded into the control word address register. The SPC uses this control address to fetch the control word, from ROM, for the first block of speech data. The control word contains waveform information, repeat information and the address of the speech data. This address is loaded into the phoneme address register and is used to fetch the speech data used to recreate the speech waveform. Before the synthesis takes place, the waveform data must be decoded to provide information such as male or female, voiced or unvoiced, half-period zeroed or not half-period zeroed and silence.

The unsynthesized waveform for a typical voiced pitch period might look a bit like a jagged, damped "sinusoid." In the process of converting this signal to a synthetic form, several operations are performed. First, the phase delay of the signal can be adjusted so as to create a symmetrical waveform about the center of the pitch period. The next step will replace the low level beginning and ending quarters of the waveform with silence. The result is a compression factor of 4 to 1 on the original voice data. Now, delta modulation is applied, and synthesis of the waveform starts with a period of silence (no speech data required), a quarter period of adaptive delta mod generated speech followed by the same

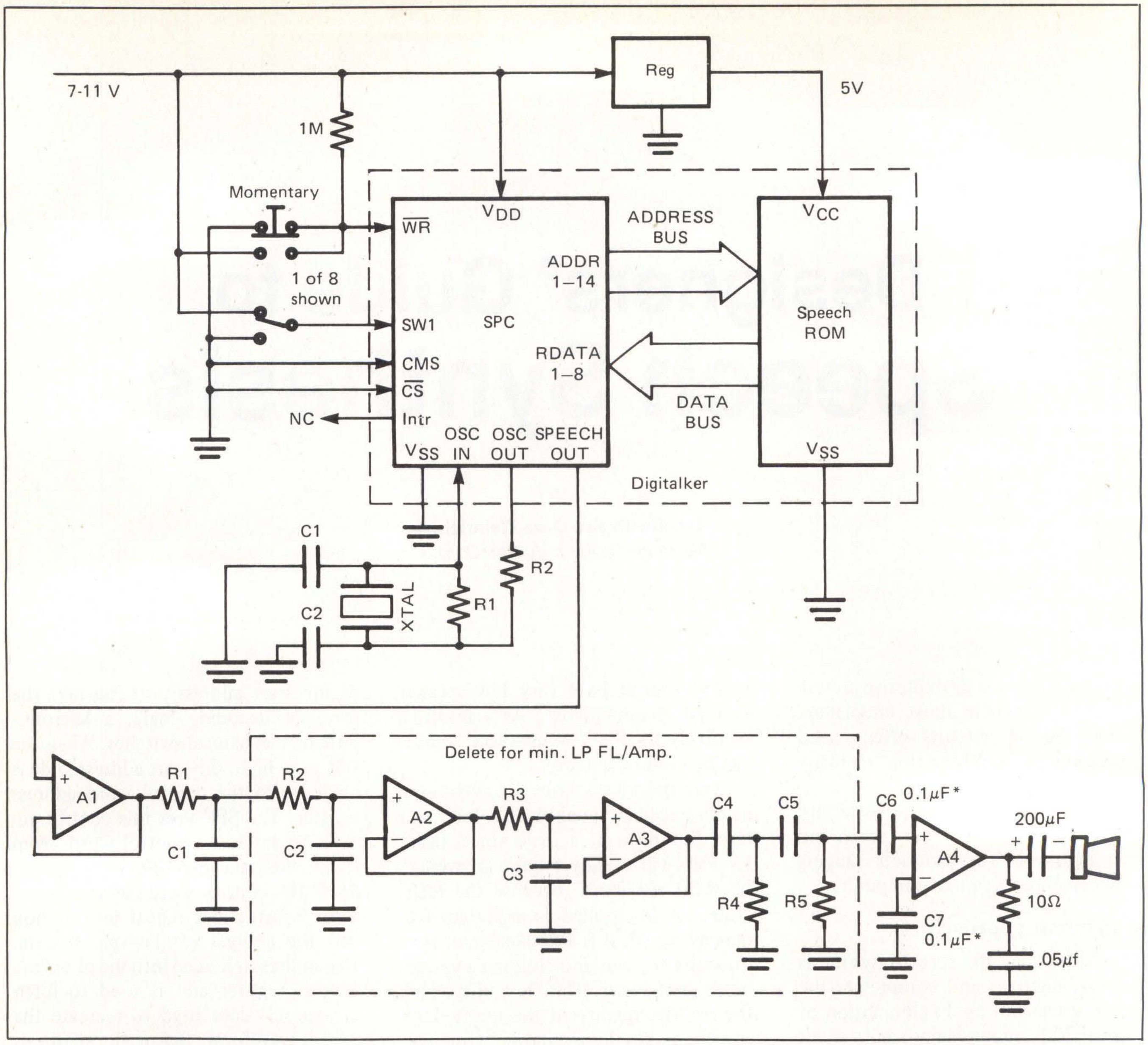


Figure 1: For a minimum configuration, all that's needed is the crystal oscillator, filter-amplifier-speaker, and regulator. "Start Address Code" inputs to SW1-8; "Write Strobe", into WR; "Command Select," into CMA; "Chip Select," into CS. "Interrupt" is outputed from "INTR" (but is shown with "no connection" in this switch interface circuit). For a minimum low-pass filter/amplier, delete the components inside the dotted box, and add two 0.1μF series capacitors (C6, C7) on the two A4(LM386) inputs. Min. LP FL/Amp. f_c=200 Hz=$(2\pi R1C1)_{-1}$. For a maximum filter response circuit—leave everything in (but delete C6, C7)—f_c=7 kHz=$(2\pi R1C1)_{-1}$=$(2\pi R2C2)_{-1}$, and f_c=200 Hz=$(2\pi R3C3)_{-1}$=$(2\pi R4C4)_{-1}$=$(2\pi R5C5)_{-1}$.

speech data fetched in reverse. Finally, the SPC will finish the last quarter cycle of the speech block period with silence (no speech data required), a quarter period of adaptive delta mod speech.

At the end of a waveform or speech block, the SPC makes a decision about repeating the sequence. Each waveform of a typical voiced signal may be repeated an average of 3 to 4 times. The typical unvoiced waveform may be repeated approximately 7 to 8 times. Once the proper number of repeats has been generated, the SPC will begin a new speech block sequence. This operation continues until the SPC has executed all control words associated with the original eight-bit start address code.

SPC speech signals are stored as adaptive delta modulation data. This encoding technique exploits the relatively predictable and slowly changing characteristic of voiced speech. Because of the small differential between successive speech samples, a delta value rather than an absolute value can be used to determine the actual speech signal. Addition of the delta value to previously accumulated values will result in a new output waveform signal level. An adaptive technique is used so that the delta step size can change in response to slope variations. This technique uses multiple delta mod step sizes to obtain a more accurate resolution and yet the required amount of stored data remains lower than the information required for a more conventional encoding scheme.

The internal SPC clock is derived from a programmable frequency generator. Variations in the frequency of this clock, through the control word, allow the SPC to add a rising and falling pitch to speech sounds and syllables. This derived pitch variation adds a natural inflection to the synthetic speech.

Just as pitch variations are used to increase realism, so must the SPC use gain variations. Both techniques are controlled by data stored at the beginning of the speech data and the programmable oscillator and output amplifier circuit blocks of the SPC.

Use of the SPC kit is quite straightforward. However, a point on application that must be covered in this note concerns the frequency response of the output speech. The ultimate quality of the SPC kit will strongly depend upon the filter, amplifier and speaker choices made by the user. For that reason, it is important to understand the output characteristics of the device.

Because the synthesized speech data is derived from a differentiated and sampled input signal, it is necessary to pass the output waveform through a low pass filter with a cutoff frequency of approximately 200 Hz and an attenuation characteristic of 20 dB/decade. This compensates for the high frequency pre-emphasis used in the synthesis technique. If the system of interest has a natural roll-off near 200Hz, this low pass filter can be eliminated. The important item is that the entire audio system should have a cutoff frequency of approximately 200Hz regardless of whether or not a discrete filter is used. The placement of the cutoff frequency may be adjusted for the particular type of voice being synthesized. A low pitched man's voice might sound better with a 100 Hz cutoff point while women and children's voices may show improvements with a 300Hz cutoff.

To see how the overall frequency response of a particular application can minimize the need for extra filtering, consider the SPC kit as a voice announcement circuit in a telephone system.

In this case, the telephone network provides a natural attenuation to high frequencies that balances the SPC high frequency pre-emphasis. As a result, the low-pass filter previously mentioned can be eliminated. However, because signal frequencies above 3 kHz must be attenuated before they are allowed to pass into the telephone network, a cutoff filter of 3400 Hz may be required in place of the previously mentioned 200 Hz low pass filter. A good filter for the application is the AF133 Active Filter or equivalent.

In addition to the 200-Hz to 3400-Hz low-pass filter, an extra stage of filtering can be used for frequencies above 7 kHz. This filter is optional and is normally only used to further reduce sampling noise. Most systems can omit this filter, especially if the overall system bandwidth is not very wide. A second, optional filter can be included to limit the overall low frequency response of the system. This high pass filter would normally cutoff below 200 Hz (adjusted to match the 200-Hz low-pass, if provided). This high pass filter limits low frequency noise, and can usually be omitted if system characteristic's do not require this function.

Applications

While the variety of synthetic speech applications seems endless, actual implementation is usually limited to one of the following three techniques: single-channel, hardware control logic; single-channel, software control logic; or multichannel, hardware or software control logic.

Certain applications require a relatively small number of sentences or announcements with very little similarity between the different sentences. An example of this application might be a talking elevator controller where the messages are brief and non-redundant (e.g., "going up, first floor, second floor," etc.). In this application, certain words are used repeatedly but the number of messages is limited and the length of each message is short. This application and others just like it do not require the assembly of short phrases into complete sentences, nor do they require a dynamic message structure as would be required with an automatic bank teller (e.g., "your change is ten dollars") where a monetary amount may change from message to message. This fixed message application, therefore, may only require the minimum control circuit.

The SPC receives a separate coded input for each complete sentence or message that is synthesized. This input code is received by the SPC through the SW1-8 port.

The circuit uses a mechanical switch group to interface the SPC while the circuit uses a hardware logic controller to input the coded message control data.

After the proper message address is established on the SW1-8 port, a momentary pulse must be applied to the WR line. If this signal is applied with a momentary action switch, normally closed, then an external pull-up resistor should be used to pull the WR line up to logic high and complete the on chip switch debounce circuitry. The suggested value of this resistance is one megaohm. The WR input signal will latch the coded message address into the SPC on the rising edge of WR and initiate the synthetic speech message. Since each complete message uses a unique address code of the SW1-8 port, no further control action is required after this point. The SPC will synthesize the requested message and return to the idle state. If a new input command signal is received during a message, the SPC will immediately abort the current message and begin the new one.

A message is initiated whenever a valid code word is applied to the eight bit SW1-8 port of the SPC. The valid code is detected by the combinational logic decoder and timed to insure all transitions have died. Once the valid code is timed, an SR latch is set and a WR rising edge is generated to start the SPC. This latch circuit also prevents retriggering of the SPC until after the present speech message is completed. Once the synthesized message has ended, the SPC will set the INTR line to the logic one state and a reset pulse will be generated to reset the lock-out latch. A new speech message can now be started by momentarily applying an idle address code followed by a valid code on the SW1-8 input port.

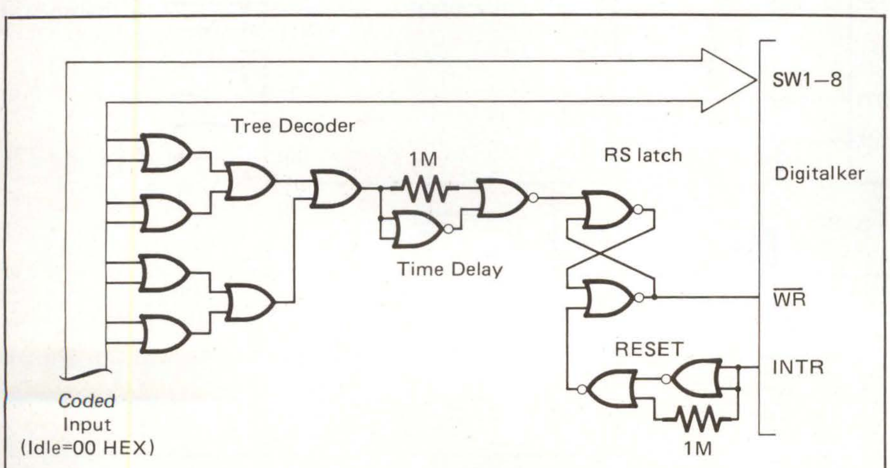


Figure 2: SPC with logic control interface. Connect Digitalker pins as in Figure 1: regulator to "V_{DD}" and "V_{CC}"; crystal oscillator circuit to "OSC IN" and "OSC OUT"; V_{SS}, CMS and CS to ground; "speech" to the minimum OR gates are MM74C32; NORs, MM74C02.

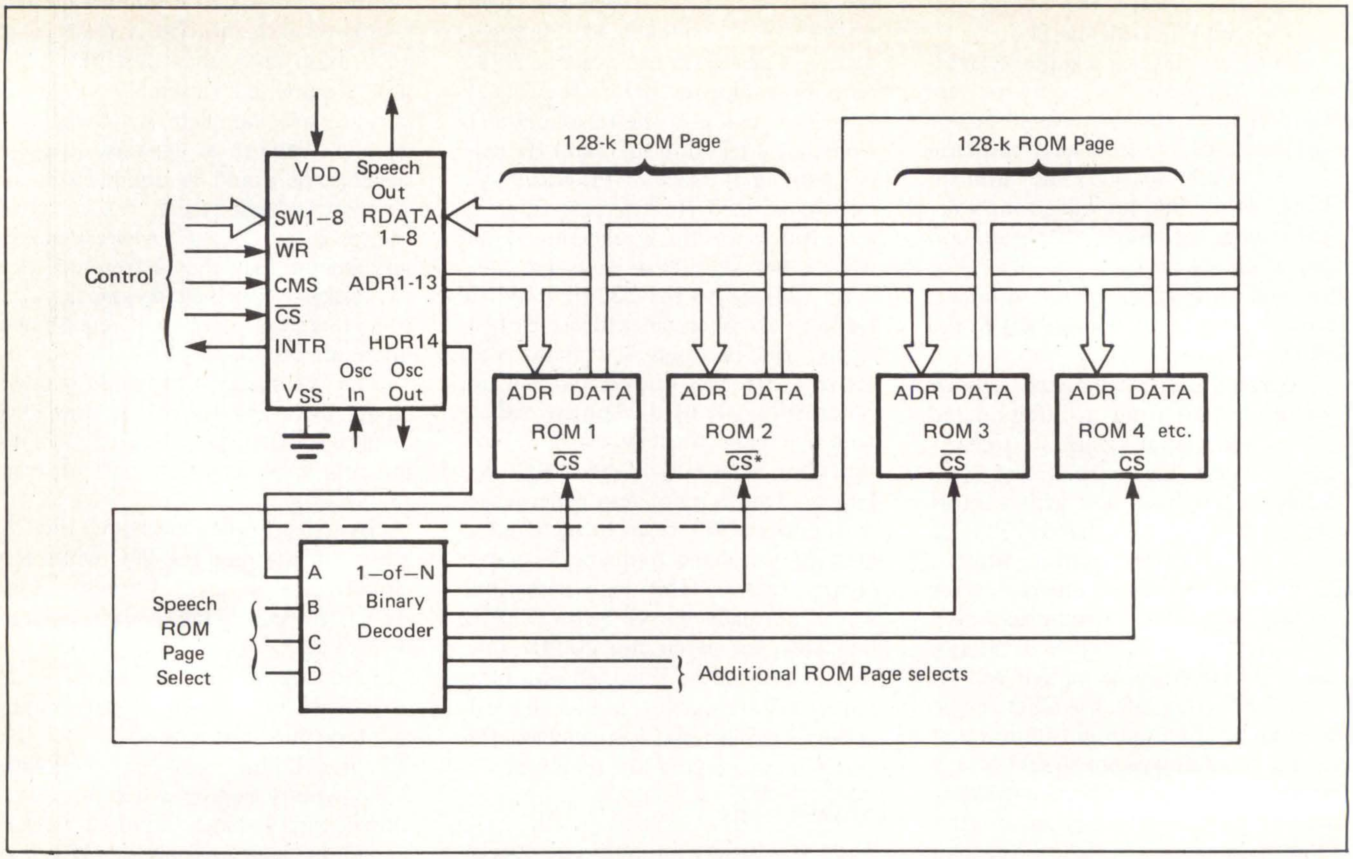


Figure 3: Typical speech ROM circuit uses two 64-k (MM 52164) ROMs, IC1/IC2. SPC pin ADR14 outputs to ROM "chip select" inputs (ROM2 has no overbar). For ROM expansion (shown in the box), HDR14 inputs to the decoder, whose outputs select the chip(s). When chip select is active, the ROM can be read from; when non-active, data cannot be retrieved and data output pin(s) go to high-impedance, so that an array of memories' output pins may be connected together without affecting the others. The active mode pin controls the output. ADR 1–13 selects the address.

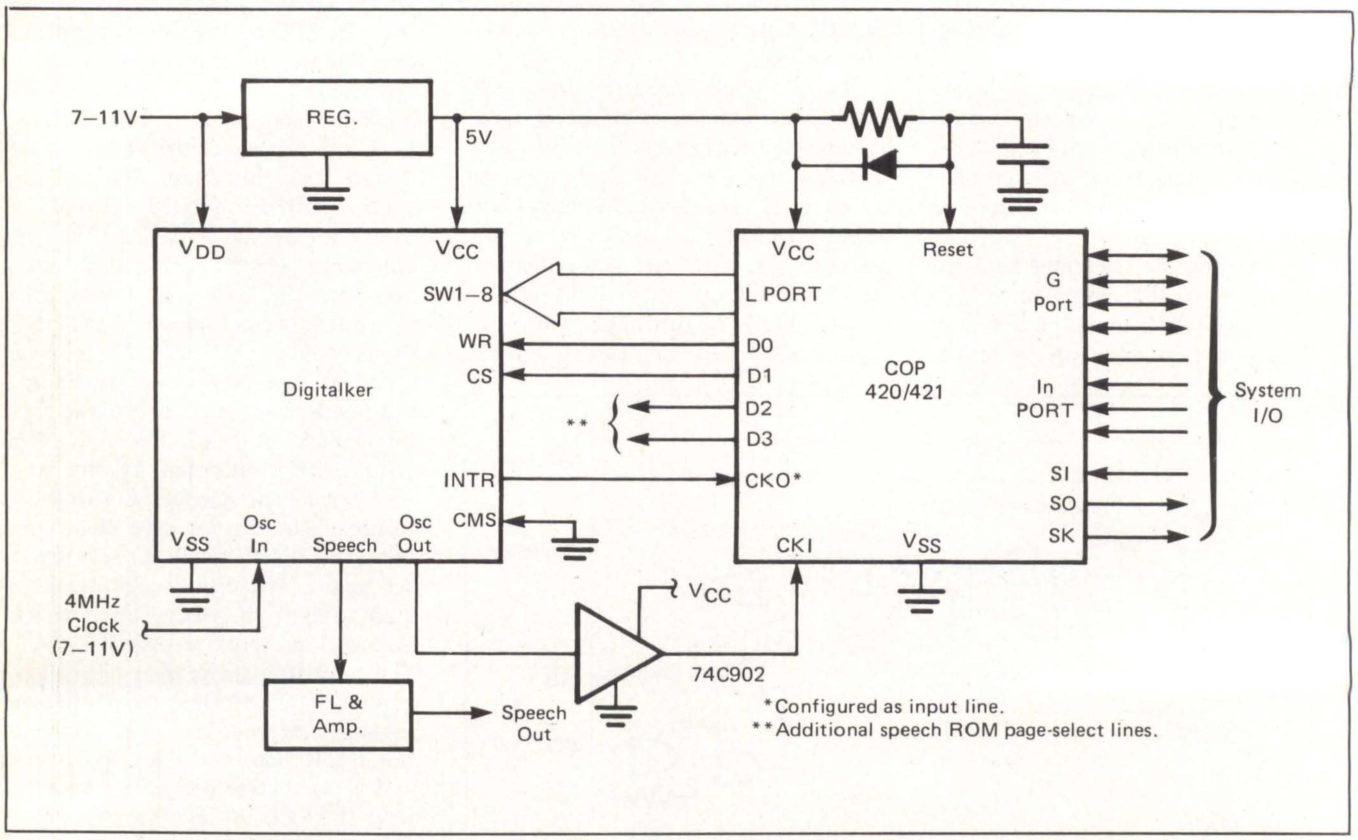


Figure 4: SPC with a COP 420/421 interface. However, for a μP ("Micro-Bus") interface (not shown), use the Digitalker with the crystal oscillator of Figure 1. "Micro-Bus" Data Bus inputs to SW1–8; Write Strobe, to WR; AO, to CMS; Chip Select, to CS. Interrupt is outputted from INTR, to the bus. The three Digitalker power supply pins remain as shown. Speech output pin goes to filter and amplifier, as shown in Figure 3.

The SPC will directly address up to 128K bits of speech memory. This shows a typical speech ROM configuration of 128K using two 64K ROMs. The types of ROMs used have mask programmable chip selects, therefore no extra decode logic is required for memory requirements of less than 128K. Although this memory size is usually sufficient for most applications, certain systems may require added speech ROM addressing. The circuit involved shows how the speech ROM of an SPC kit can be expanded in 128K bit pages or modules. Each page is arranged to contain a complete portion of the entire speech library for a particular system. Each single speech data block, as addressed via the start address port of the SPC, must be contained within one ROM page. No page boundaries can be crossed during the synthesis of a speech expression.

While the simple control schemes discussed so far can be used in many applications, a far more important group of applications will take advantage of the SPC's ability to construct sentences from a group of words, sounds and phrases. This type of application uses an intelligent controller (i.e., μP) to string together a group of synthesized phrases to form a complete sentence. The electronic bank teller mentioned earlier is a good example of this application. The μP controls the stringing of SPC code addresses and applies them, one-at-a-time, to the SW1-8 port of the SPC. Handshake timing between the μP and the SPC is provided with the INTR line. This μP interface arrangement is known as Micro-Bus.

The use of a μP controller expands the versatility of the SPC tremendously. Messages that are composed of numerical responses or fixed phrases in random sequence can be easily constructed from a library speech memory. In addition, various tones or warnings can be synthesized and added before, during or after an announcement to identify the urgency of each message. For example, an automobile message may state that "oil pressure is low." Alone, that message may only mean that pressure has dropped but no immediate hazard exists. If, however, pressure has dropped below a critical value, the message could be compounded to say "warning, oil pressure is low, pull over and stop engine." In this latter case, phrases of high urgency are added to the initial message to increase its level of importance. Of course, the second message is not completely separate from the first but is instead an expansion of the first. This technique allows fewer input address codes to initiate a larger number of messages without assigning a separate address code for each message and for each of its derivatives. This would be particularly important to an electronic bank teller since a large number of monetary amounts must be synthesized for a relatively small number of finished sentences.

When preparing a speech ROM for an SPC that will synthesize whole sentences from groups of phrases, it is important to note the desired inflections. The SPC has the ability to synthesize all of the important speech attributes including pitch and gain variations, emphasis, inflection, etc. This leads to very high quality life-like synthetic speech if the stringing of phrases does not result in an artificial emphasis or inflection. It is important to choose phrases carefully and to record them with the attribute required for a realistic sentence string. The stringing of phonemes should be avoided whenever possible because the natural inflection is usually lost in such an arrangement.

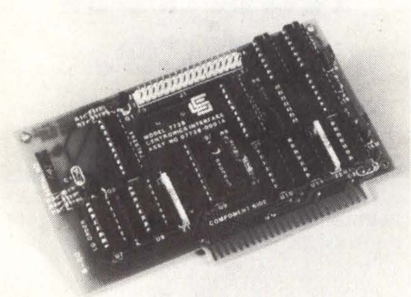
A low-cost intelligent controller for the SPC is the COP400 series of microcontrollers. There is one possible arrangement of an SPC system and a COP420. The COP provides all of the interface at a relatively low cost. Because of its limited I/O structure, the COP's serial I/O port is expanded as required to obtain the desired number of input lines.

The final application technique is the multichannel configuration. The previous arrangements used an SPC and a dedicated set of speech ROMs to provide a single channel of synthetic speech. Appliances, autos, toys and games, terminals, etc. would probably use a single channel SPC arrangement. But an entirely different group of products could take advantage of a multiple channel approach to reduce the ROM requirements. This group of products includes multiple elevator controllers, electronic bank tellers, multiple pupil learning centers, voice response telephone answering equipment, telephone switching system call announcement centers, etc. In this application, each channel would use a separate SPC and amplifier circuit, but several channels would share a common controller and speech library ROM.

Other applications exist, and the near future should see widespread use of speech synthesis as designers scramble to incorporate speech synthesis into their products and systems.

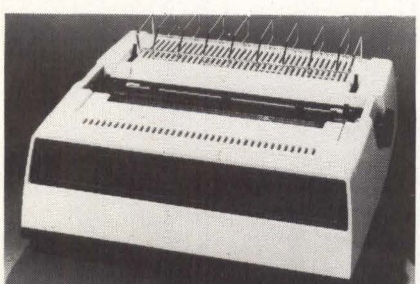
New Products

APPLE II PRINTER INTERFACE gives the Apple II compatibility with a variety of printers using Centronics-type parallel interfaces. An on-board 256-byte ROM provides driver firmware and controls ASCII character output to the printer. The driver responds to standard Apple II printer commands for selection of command characters,



characters per line, auto feed, and video echo. The standard ROMs may be replaced with RAMs. A ROM/RAM jumper makes the necessary logic changes. The printer interface includes an 8-bit data output bus, 4 status inputs, Data Strobe and Acknowledge handshake signals. The 7728 is $120 with documentation. Cables for the different printers are available separately. **California Computer Systems,** 250 Caribbean Dr, Sunnyvale, CA 94086 **Circle 175**

IMPACT PRINTER is compatible with the Telex 274/276 and IBM 3274/3276 control units, or directly with the IBM 4300. Plug-compatible with IBM's 3287, the μP-based printer is designed with bus-organized logic with

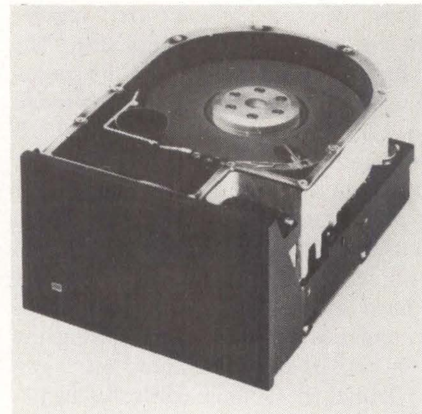


10 or 12 characters/in. and 6 or 8 lines/in. printout. The 286C Model 1 has a 1345A Hy Type II printer mechanism, while the 286C Model 2 has a 1355 WP Hy Type II mechanism utilizing a metallized printwheel for applications requiring maximum high print quality. Averaging 45 cps, the 286C has bi-directional printing and a "look ahead" feature for a faster print speed of 60 to 80 cps. A choice of ASCII-B or EBCDIC character sets is offered. The Model 1 is $4600; Model 2 is $4900; 60 days ARO. **Telex Computer Products, Inc,** 6422 E. 41st St, Tulsa, OK 74135 **Circle 192**

VIDEO TERMINAL. The C. Itoh VIT 100, designed as a replacement for the DEC VT100, has been renamed the CIT 101 to reflect its new compatability with a range of computer systems. The CIT 101 is an 80 and 132-column video terminal with detachable keyboard and numeric/function keypad. Standard display format is 24 lines × 132 columns. The 12″ diagonal screen delivers selectable single and double-width/double-height character size, selectable reverse character display, split-screen capability, fixed and settable tabs, variable-speed smooth scroll and page and line window erase. **ACRO Corp,** 18003 L Skypark S., Irvine, CA 92714 **Circle 148**

DUAL OUTPUT SWITCHERS. The 2050-1 powers the Rockwell AIM-65 microcomputer with +5V@6A output. It will also power additional memory, DC/DC Converters, data acquisition boards and PROM programmers. A second output provides +24V@0.5A average and 2.5A peak for the AIM-65 printer or other mechanical devices. The 2050-2 powers DEC's LSI-11 based systems with either +5VDC@8A or +12VDC@1.5A. The power supply input offers pin strapable voltage ranges of either 85 to 135 VAC or, 170 to 250 VAC at 47 Hz to 470 Hz. An RFI input line filter is standard. From $123 (Open Frame) to $133 (Enclosed). **Power General,** 152 Will Dr, Canton, MA 02021 **Circle 168**

5-1/4″ MINI-WINCHESTER DISK DRIVES have unformatted storage capacities from 3.19MB to 11.5MB. They are available in 1, 2 and 3 platter models. Track-to-track access time is 3 ms, average access time (1/3 of total stroke) is 168 ms, including head setting time; and 245 ms in the extended cylinder version. Recording density is 7690 bpi and rotating speed is 3600 rpm. The drives can interpret and generate control signals; move R/W head to the correct position; and,



read and write data. The electronics are packaged on two PCBs which contain logic and R/W circuitry, and motor control. Up to 4 TM 600s can be daisy-chained on a single bus. From $1400-$1600. **Tandon Magnetics Corp,** 9333 Oso Ave, Chatsworth, CA 91311 **Circle 172**

MAG TAPE/FLOPPY SYSTEM combines hard and flexible disk storage with a magnetic tape backup unit (MTU). The system includes a Data Electronics 1/4″ "Funnel" cartridge tape drive, with Shugart 8″ floppy and 14″ Winchester hard disk drives. It supports 1-4 users simultaneously. The

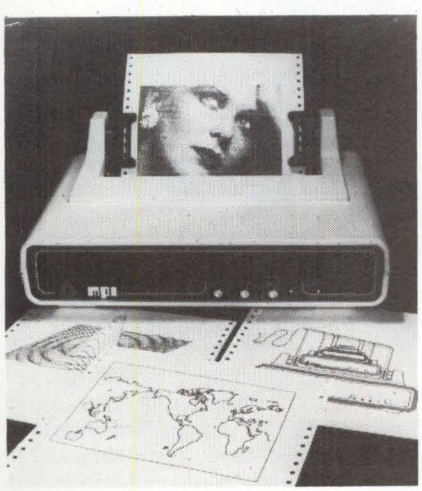
MTU includes a 450 ft. tape cartridge with 17MB of storage capacity. R/W is performed on 4 tracks at 30 ips. The drive searches at 90 ips in either direction and packing density is 6400 bpi. The ACS8000-6 is $12,650, OEM discounts available, 90 days ARO. **Altos Computer Systems, 2360 Bering Dr, San Jose, CA 95131.** **Circle 160**

CRT CONTROLLER BOOK, by Gerry Kane, describes all of the controller devices currently on the market. Learn how to achieve maximum efficiency through a simple design that will cost less. A tutorial chapter explains the principles of CRT operation – how a

CRT works and what a CRT controller is expected to do. Devices are covered including pins, signals, registers, μP interface, screen memory, transparent memory addressing, character generator interface and more. ($6.99). **Osborne/McGraw-Hill,** 630 Bancroft Way, Berkeley, CA 94710 **Inquire Direct**

AUDIO D/A CONVERTERS. Data sheets are available on the MP1926 high speed 16-bit audio D/A converter, and the MP201A audio distortion suppressor. The MP1926 reconstructs dynamic complex waveforms from digital data, particularly audio or acoustic signals with information in the vicinity of zero volts midrange. Its internal sign/magnitude architecture gives 18 bits of linearity for signals near zero volts and a 3μs settling time. The MP201A suppresses harmonic distortion at the output of the MP1926 and other D/A converters. It keeps distortion below −86dB over the frequency range from 20Hz to 20kHz. **Analogic Corp,** Audubon Rd, Wakefield, MA 01880 **Circle 128**

IMPACT MATRIX PRINTER features 100 cps bidirectional or unidirectional printing with a short line "Quick Cancel" feature, giving thruput rates of up to 150 lpm. A full upper and lower case 96 character ASCII set is printed in a 7 x 7 matrix with print line formats of 80, 96 or 132 columns/line over an 8" print area. Double-wide characters are software selectable in any of the font styles or character densities and can be intermixed. A high resolution dot addressable graphics option can be added. It includes a stepper motor driven paper feed system with 16 selectable form lengths and a skip-over-perf feature. The μP controlled interface accepts either RS232C data up to 1200 baud or TTL level parallel data at 1000 cps.

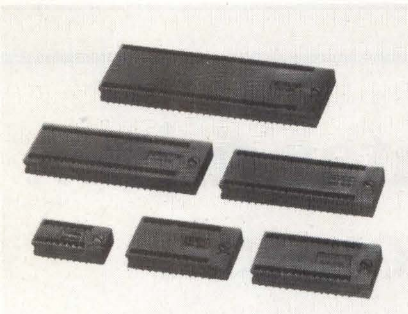


Options are available for 9600 baud and for 20mA current loop applications. An IEEE/Parallel interface adapter and 2K buffer are also available. The Model 88G is $799, OEM discounts available. **MPI,** 2099 West 2200 South, Salt Lake City, UT 84119. **Circle 207**

ENHANCED PASCAL MICROENGINE. Major software enhancements and a new memory module are available for the Pascal MICROENGINE microprocessor and microcomputer product line. With an interface connector and second memory card, memory size is doubled from 64 kB to 128 kB. Programs can be executed faster because additional stack space eliminates swapping. No memory banking or memory map is required. Program size can be increased from 7,000 to 30,000 lines. The Pascal MICROENGINE μP-based system is designed to optimize execution of high order languages. It features the 16-bit Pascal MICROENGINE processor, 64 kB of RAM memory, fully-integrated floppy disk controller, two RS-232 async/sync ports, two 8-bit parallel ports, and a power supply. MICROENGINE is $4100. **Western Digital Corp,** 3128 Red Hill Ave, Newport Beach, CA 92663. **Circle 216**

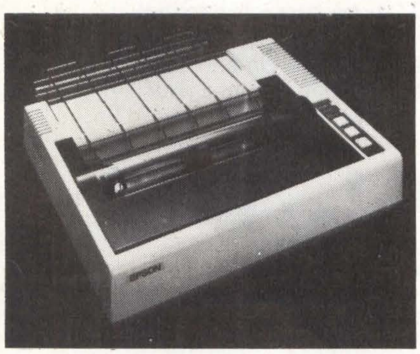
New Products

64 LEAD SOCKETS are available in 16, 24, 28, 40, 48, and 64 pin models for mounting on standard .100″ centers on either axis. Device protection features including wide entry holes to accept bent or distorted leads that don't have to be reformed prior to insertion, a screw driver operated metal cam for easy operation and prevention of accidental unloading, and long life. At the 1000 quantity, the ECONOZIP sockets are from $1.55 (16 pins), to $4.62



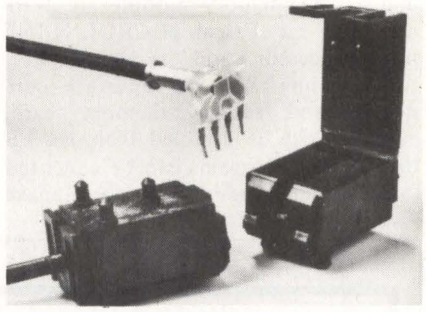
(64 pins). **3M,** Textool Products Dept, 1410 W. Pioneer Dr, Irving, TX 75061 **Circle 144**

DOT MATRIX PRINTER. When its disposable printhead has reached its life expectancy, 50 to 100 million characters, it snaps out. A new one is $30 and can be installed by hand. The



MX-80 prints a full character set in up to 12 print modes. It prints bidirectionally at 80 cps, with a logical seeking function to minimize print head travel time and maximize throughput. Print densities of 40, 66, 80 or 132 printing columns in an 8″ field are possible, and the adjustable minitractor accomodates paper widths from 4″ to 10″. ($650). **Epson America, Inc,** 23844 Hawthorne Blvd, Torrance, CA 90505 **Circle 130**

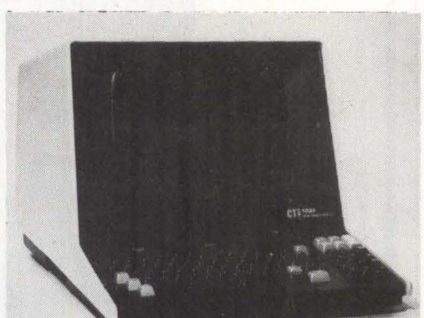
BI-DIRECTIONAL FIBER OPTIC DATA LINK consists of a pair of transceivers and a fiber optic cable. It forms a unit which, through multiplexing, can receive and transmit over a single fiber. This eliminates the need tor 2 receivers, 2 transmitters, and 2 lengths of cable. Intended for distances to 10 meters, it has a bandwidth of 1.5 MHz. With a LED drive current of 50 mA and a V_R of 12 V through 3 meters of cable, photodiode output current is 200 nA minimum. Parts for the OPB-



950 are $39.95 at the 1K level, for a complete data link. **TRW Optron,** 1201 Tappan Circle, Carrollton, TX 75006 **Circle 176**

DATA SCREEN TERMINALS BROCHURE. This 4 pg. brochure describes the Series 570 & 670 Data Screen terminal. They feature upper and lower case with descenders; conversational or buffered data communication capabilities, including line or page transmits, at 16 different baud rates (50 through 19.2K baud); and, software controlled keyboard lock/unlock and local and TTY lock keys. Switch selectable features discussed are: 10-or 11-bit async ASCII data bytes with odd, even, or mark parity; space code suppression during transmit; and, automatic carriage return. A powerful editing package is standard equipment. **TEC, Inc,** 2727 N. Fairview Ave, Tucson, AZ 85705 **Circle 137**

IBM COMPATIBLE DISPLAY is compatible with the IBM 2740 and 3767 keyboard printers. It can support 2 printers either as slave units or directly addressable by the host processor. The CTi 1000 is μP-based, and features a

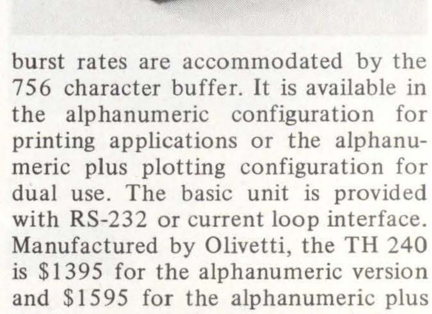


12″ diagonal screen with 23, 80-character lines. The 24th line is an operator status and diagnostic line. Messages from the host can be routed selectively to either the printer or the display. Screen formats, operator prompts and other productivity aids can be created at a central location, then loaded down-line to CTi 1000 terminals and stored locally for faster access by the operator. Formats can also be stored in the terminal's non-volatile memory. ($2,350). **Custom Terminals,** Box 19906, Raleigh, NC 27619 **Circle 194**

DUAL-MODE MATRIX PRINTER can be used in data processing (DP) as well as word processing (WP) applications. Output speeds range from 165 cps to 250 cps in the DP mode and 42 to 60 cps in the letter quality mode, depending on the font selected. Numerous character fonts are available. The printer can store up to 6 different character fonts in ROM with a DP and a WP version of each for a total of 12

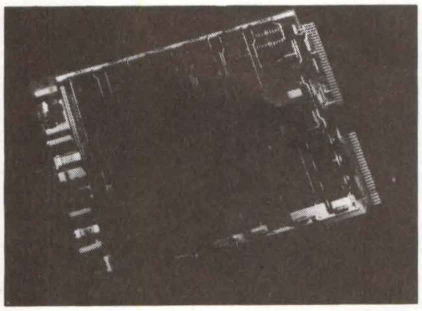
speed/font options. The user may also design custom character sets and download them to the printer. Universal forms handling permits the use of single sheet and pin-feed paper. Multiple part forms are also accommodated. Deliveries for the Model 200 begin in March 1981. **Malibu Electronics Corp,** 2301 Townsgate Rd, Westlake Village, CA 91361 **Circle 190**

PRINTER/PLOTTER. This 80 column thermal printer operates at 240 lpm and up to 1200 baud on-line. Faster



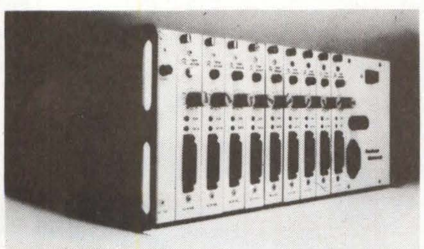
burst rates are accommodated by the 756 character buffer. It is available in the alphanumeric configuration for printing applications or the alphanumeric plus plotting configuration for dual use. The basic unit is provided with RS-232 or current loop interface. Manufactured by Olivetti, the TH 240 is $1395 for the alphanumeric version and $1595 for the alphanumeric plus plotting version. **Printer Systems Corp,** 1 W. Deer Park Rd, Suite 104, Gaithersburg, MD 20760 **Circle 191**

MICRONOVA BOARDS. These computer peripheral boards are a combination analog and digital I/O interface, a video interface, a RAM/EPROM memory board, and an I/O CMOS memory board. The I/O interface (Model 4335-S) is designed for compact packaging into data acquisition and process control applications. The Video Interface (4337-S) gives OEMs direct control over formatting information. The RAM/EPROM Memories (8688 and 8689) extend PROM-able capabilities to the microNOVA MP/200 computer. The I/O CMOS Memory (8316) provides the capability of



a portable memory. From $630 to $1900 depending on model, 90 days ARO. **Data General Corp,** Rt. 9, Westboro, MA 01581 **Circle 186**

UNIVAC PORT CONCENTRATOR interfaces with a mix of terminals, including hard copy and CRT devices, of various speeds. Data rates of the terminals can range from 110 to 19,200 bps. Communication is via UTS 400 protocol. For non-Univac terminals,



the Model 871 provides the necessary display and formatting control functions. Its multiple μP architecture allows operation at up to 19,200 bps simultaneously on all lines. It enables a single Univac System port to support 31 clusters of 8 terminals each, for a total of 248 devices. Any of the ASCII devices can be supported and ports can be added with Line Interface Modules (LIM). The basic 871-1A with one LIM is $4765; additional LIMs are $690. **Kaufman Research Manufacturing, Inc,** 14100 Donelson Place, Los Altos Hills, CA 94022 **Circle 187**

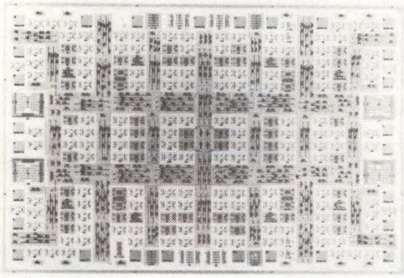
SMD DISC CONTROLLER. This single hex size board plugs into any PDP-11 SPC slot to control up to 4 SMD drives. When used with a CDC 80MB drive or equivalent, it is completely software compatible to all DEC operating systems having RM02 support. A 300MB drive will yield RM05 compatibility. The DC-231 has self-diagnosis, the results of which are displayed on 5 LED indicators on the board. $3150/unit, OEM qty. discounts available, 60 days ARO. **Western Peripherals,** Div. of Wespercorp, 14321 Myford Rd, Tustin, CA 92680

Circle 135

LSI 32-BIT MINICOMPUTER The new VAX-11/750 is completely software-compatible with the VAX-11/780. Features include 2MB of ECC MOS main memory; 4 kB integral cache memory; cartridge tape drive for software updates, diagnostics or auxiliary data storage; an integral UNIBUS interface for terminals, serial devices and medium-speed peripherals; and up to 3 optional MASSBUS adapers for up to 24 high-speed disk and tape units. For OEMs, the VAX-11/750 CPU, with 512 kB of memory, communications multiplexer for 8 EIA terminals, and LA38 DECwriter IV console terminal, is $47,000. Delivery begins in April 1981. **Digital Equipment Corp,** Maynard, MA 01754 **Circle 188**

New Products

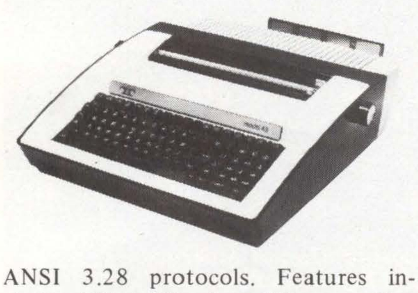
LINEAR ARRAY. The MOM (EM-OH-EM) Monochip includes over 800 linear components. It operates up to 20V and has 28 available bonding



pads. It reduces large scale discrete, MSI, or hybrid circuitry to a single linear IC. New components include vertical PNPs for grounded collector configurations with either input or output stages and special geometry (low wide band noise) NPNs for use in input stages of audio, RF, and instrumentation circuitry. The MOK Design Kit, containing all the information needed to design a MOM IC is $59. The integration fee which includes 50 prototypes is $7000. **Interdesign Inc,** 1255 Reamwood Ave, Sunnyvale, CA 94086 **Circle 157**

ENHANCED DIABLO 3000. The data communications option for this small business system allows access to proprietary data bases. Up to 4 additional printers or workstations in any combination can be added to the basic console and printer configuration of the computer with the multi-peripheral option. Workstations may be either display or hard-copy terminals with both daisywheel and matrix Diablo printers. Each terminal/printer port is individually selectable as either RS232C or current loop under program control. Communications can be either sync or async, using a modem or acoustic coupler. **Xerox Corp,** 701 S. Aviation Blvd, El Segundo, CA 90245 **Circle 169**

TELEPRINTER, for multi-point private line systems, is a μP driven tabletop unit compatible with a variety of



ANSI 3.28 protocols. Features include: 16K buffer for editing, sending and receiving; independent local/line operation; 80 keyboard selectable options; remote options load routine; auxiliary port for an optional Teletype character or line printer; line speeds from 10 to 240 cps; priority store capability; full formatting controls; and longitudinal redundancy error checking with automatic retransmission. The 43 BSR teleprinter in a pinfeed version is $2662, 60 days ARO. **Teletype Corp,** 5555 Touhy Ave, Skokie, IL 60077 **Circle 158**

TURNKEY GRAPHICS SYSTEMS. The IGS 400 is a standalone graphics system with a 64K word system processor, 50 MB disk drive, floppy disk subsystem with 128KW (16 bit word) capacity and user workstation. The workstation includes its own picture processor, two CRT screens (one alphanumeric and one raster/scan graphics), keyboard, graphics tablet and joystick. The 400 can be expanded to 256KW (16 bit word) of memory; other options include additional disk storage, plotter, large digitizer and impact matrix printer/plotter. A basic IGS 400, including system software, is $89,000,

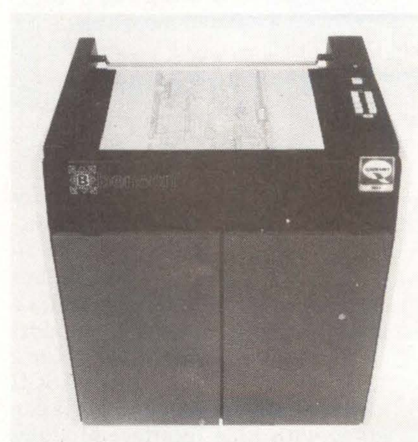
90 days ARO. For remote interactive graphics, the IGS 300, a satellite system, links to a central system for transmitting drawing files. Its configuration is similar to the 400, but is supported with a sync communication line instead of floppy disks. The IGS 300 can support all IGS 400 options, plus dual floppy disk drives with 128KW (16 bit words) byte capacity. ($85,000). Both can be upgraded to an IGS 500 with multiple workstations operating simultaneously. **California Computer Products,** 2411 W. LaPalma Ave, Anaheim, CA 92801 **Circle 167**

12-BIT A/D CONVERTER. The HI-5712A guarantees ±1/2 LSB maximum nonlinearity and differential nonlinearity over its entire specified temperature range. Different grades specify either commercial (0°C to $+75^\circ$C) or military (-55°C to $+125^\circ$C) temperature ranges, with the latter also available with MIL-STD-883 Class B screening. Other features include a 10 μs maximum conversion time and a gain TC of 15 ppm/$^\circ$C. A lower priced version, the HI-5712, is available for less critical applications. Both can be software programmed to operate as 10, 8 or 6-bit converters with a corresponding reduction in conversion time. Both will accept either unipolar or bipolar inputs, are compatible with DTL, TTL, and CMOS logic, and offer both serial and tri-state parallel outputs. From $100/100 for the HI-5712; from $200/100 for the HI-5712A. **Harris Semiconductor Products,** Box 883, Melbourne, FL 32901. **Circle 163**

10MB FIXED DISK DRIVE. This low cost drive is a direct replacement, and is interface compatible to CDC, Perkin-Elmer, Dynex and other cartridge

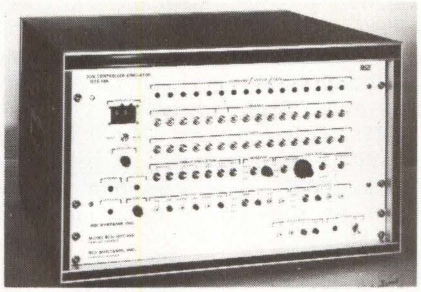
disk drives. With the Dynex 10 MB Series 6000 cartridge disk drive ($2100), it allows low cost system expansion to 40 MB in any combination of fixed disk and removable cartridge drives. Each drive has its own built-in backup. Documentation for the Series 4000 and a yr. mechanical, 90 day electronics warranty is standard. Delivery is 90 days ARO. ($1650). **Western Dynex Corp,** 3536 W. Osborn Rd, Phoenix, AZ 85019 **Circle 155**

METRIC ELECTROSTATIC PRINTER/PLOTTER produces a resolution of 100 dots/cm (254 dots/in.). The Quadramet 9424 plots at 2.54 cm/sec (1.0 in) at a plot width of 59.51 cm/



sec (23.43 in). The Quadramet 9436 plots at 1.27 cm/sec (0.5 in) across an 89.59 cm (35.27 in) plot width. Since most foreign countries use metric dimensions this series is designed to reduce the time consuming process of metric conversion to English dimensions. The 9424 is $29,500, the 9436 is $39,800. **Benson-Varian, Inc,** 385 Ravendale Dr, Mountain View, CA 94043 **Circle 152**

DATA BUS TESTER. Compatible with MIL-STD-1553 A/B, Model BCS/IEEE-488 is controllable by companion devices with IEEE-488 or GPIB port.



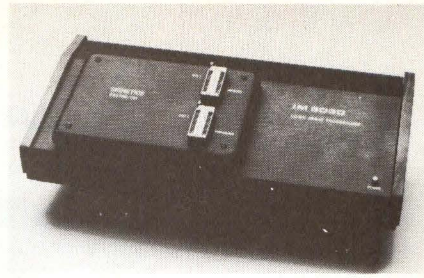
The unit also operates in a stand-alone manual mode performing as a bus controller with full capability to send and receive data bus messages. It features several error simulations in both operating modes and provides LED display of command, data, and status words. Qty. of 3 each is $8,000, 90 days ARO. **SCI Systems, Inc,** 8600 S. Memorial Pkwy, Huntsville, AL 35802.

Circle 179

SPRINT 3 INTERFACES. The CS-1, a QUME Sprint 3 interface, is an intelligent RS-232 Serial interface providing complete text processing at selectable baud rates from 150 to 9600, with full hardware/software handshaking. Standard features include: a 16k input buffer allowing high-speed throughput plus margin justification, true proportional spacing, micro spacing, auto centering and vertical tabbing, without special hardware options. Word and character control may be enabled for auto super and subscripting, boldface, shadowprint, underline and overstrike. Line manipulation is provided for bi-directional printing, direct tabbing and backspacing. Vector plotting is also provided in the CS-1. ($695). The CS-2 interface provides complete handshaking and communications capabilities to all standard 8-bit Centronics parallel ports. It is compatible with the TRS-80 Modle I and II, Apple II, Exidy Sorcerer, Atari 850 and other personal and professional computers. The CS-2 printed circuit card is bolted to the back of a Sprint 3 printer and includes a standard Centronics connector. ($395). Dealer and OEM discounts available. **Data Wholesale Corp,** 700 Whitney St, San Leandro, CA 94577.

Circle 211

UNIVERSAL LOGIC ARRAY programmer is designed to program all present and future logic array devices including PALS and FPLAs. When interfaced with a CRT, the powerful menu-driven EDITOR provides complete program development for defining output levels, product terms and sum terms. The CPU provides the capability of complete software LOGIC VERIFY. Data input for programming may be supplied by a Master Device, User Terminal input, or Computer Formatted input. Operating modes include EDIT of device terms; DISPLAY terms; PROGRAM logic device; VERIFY logic device fuse pattern; software VERIFY; DUPLICATE; and LOAD/DUMP paper tape format. It also provides a hardware LOGIC VERIFY against a Master Device. Standard features of the IM3030 include: menu-driven software; dual RS232 ports for interfacing to development systems; switch selectable baud rates from 110 to 9600 and

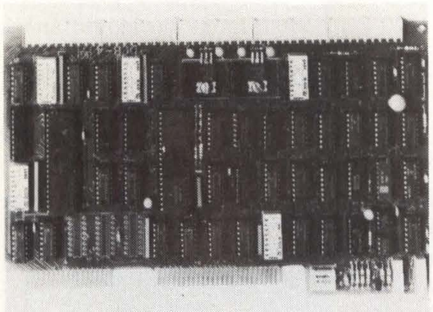


20 ma current loop. The Main frame is $1595; modules from $595. **International Microsystems, Inc,** 11554 C Ave, Auburn, CA 95603.

Circle 233

New Products

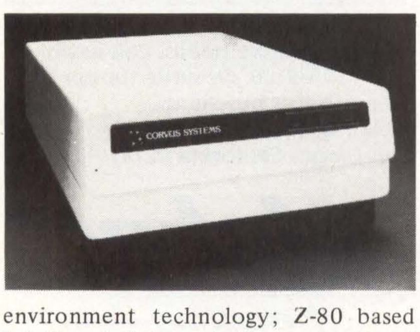
DOUBLE DENSITY CONTROLLER BOARD. This SS-50 bus double density controller board has 336 kB of storage on a single minifloppy and can handle four 5 1/4" and four 8" drives simultaneously. It is fully compatible



with hard disk systems and allows selection of either single or double-sided operation; single or double density data; stepping rate; 40- or 35-track density on 5 1/4" drives, as well as the system boot configuration. The Disk Master occupies 16 bytes of memory space and can R/W a single sector by itself. The DCB-4 Disk Master, including DOS68D or 69D, monitor object code and manual, is $449. **Smoke Signal Broadcasting,** 31336 Via Colinas, Westlake Village, CA 91361 **Circle 150**

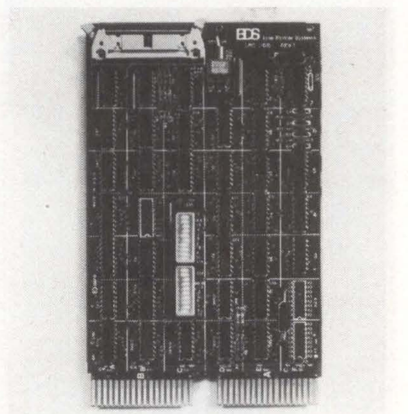
CIRCULAR CONNECTORS. This 36 pg. illustrated catalog features Amphenol 97 and 69 Series standard circular connectors. A guide to circular connector selection is divided into several steps, including considerations about environmental capabilities, wire gauges, plug and receptable requirements, shell-type needs (solid or split), socket location and finish options. The full range of available circular connector styles are summarized in a chart. **Amphenol North America Div,** Bunker Ramo Corp, 2122 York Rd, Oak Brook, IL 60521 **Circle 154**

20 MB WINCHESTER DISK. The system consists of a compact 8" IMI-7720 Winchester disk drive employing sealed-



environment technology; Z-80 based intelligent disk controller supporting 4 drives; plus an intelligent personality module for each computer. ($6450). Up to 3 add-on disk drives with either 10 or 20 MB capacity can be incorporated into the system. ($5750/drive). **Corvus Systems, Inc,** 2029 O'Toole Ave, San Jose, CA 95131 **Circle 139**

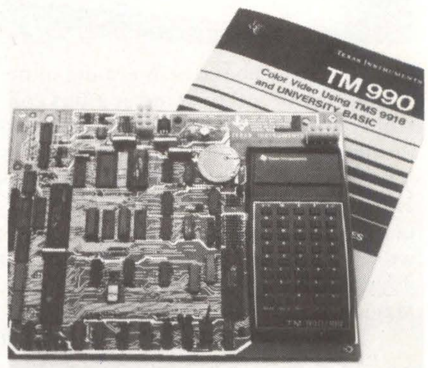
SINGLE–BOARD CONTROLLERS AND PRINTERS provide the LSI-11, 11/2, 11/23 and PDP-11/03 microcomputers with serial or line printing. The LPC-03 controller is fully plug-compatible with the Unibus and software transparent to the operating system. The 180 and 340 cps printers have a 7 by 7 dot matrix with 64/96 character set. The 300 lpm band printers have 64 fully-formed upper-case character sets with 96 upper-lower-case character sets as options. LPC-03 controllers occupy one quad-size slot in the chassis. Power required is +5Vdc



@ 0.8A. The LPC controller is $795; the 180 cps printer is $2700; the 340 cps printer is $3400 and the 300 lpm printer is $5400. **BDS Computer Corp.** 1120 Crane St., Menlo Park, CA 94025 **Circle 138**

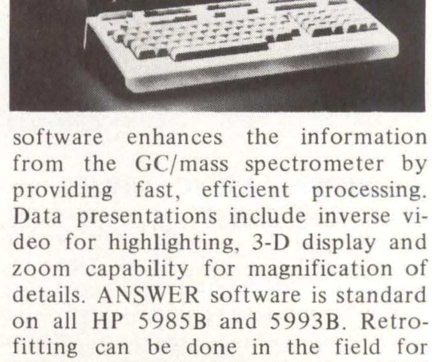
FFT PROCESSOR DESIGN. "An Introduction to Digital Spectrum Analysis, Including a High Speed FFT Processor Design" is a 45 pg application note by Richard J. Karwoski. It explains the differences between a discrete Fourier transform (DFT) and fast Fourier transform (FFT), including sampled data spectrum and aliasing as well as truncation effects and spectral resolution. The decimation-in-time (DIT) FFT is described with emphasis on computational and flow diagrams. The design of the high speed FFT processor is covered both theoretically and practically. First, computational considerations for in-place algorithms are described. Then the data arithmetic unit (DAU) design is detailed complete with timing diagrams and block diagrams that illustrate use of the TDC1010J, 16 × 16-bit multiplier-accumulator, **TRW LSI Products,** 2525 E. El Segundo Blvd., El Segundo, CA 90245 **Circle 153**

UNIVERSITY BOARD WITH BASIC. This single-board microcomputer aids in learning high-level languages, 16-bit μP fundamentals and interfacing techniques. It comes with the University Basic ROM Kit, with additional hardware features: 1kB extra RAM, async communication port, on-board relay for audio cassette interface, off-board CRU expansion. The TM990/189-1 is $399. For upgrading, the University Basic ROM Kit is a 6K implementation of TI's Power Basic industrial



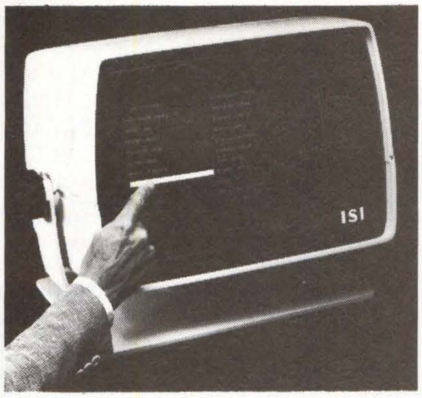
programming language. It consists of 2 ROM's which plug into the standard TM990/189 board. The system supports a single user on the on-board microterminal, an RS-232-C keyboard, or a 20ma current-loop terminal. ($110). **Texas Instruments Inc,** Box 225012. M/S 308, Dallas. TX 75265 **Circle 159**

GRAPHICS FOR GC/MS. With ANSWER software and the HP 2648 graphics terminal with a fast FORTRAN processor, intelligent graphics is available to the analytical chemist for GC/MS data processing. ANSWER



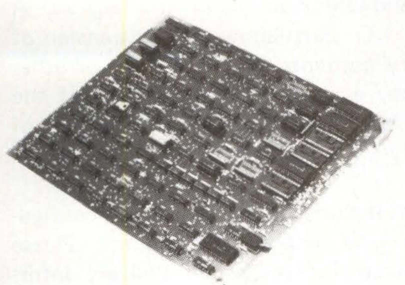
software enhances the information from the GC/mass spectrometer by providing fast, efficient processing. Data presentations include inverse video for highlighting, 3-D display and zoom capability for magnification of details. ANSWER software is standard on all HP 5985B and 5993B. Retrofitting can be done in the field for $1550. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304 **Circle 162**

TOUCH-SENSITIVE CRT KITS, for integration of touch-sensitive capability into CRT terminals, allows data to be inputted to a data processing sys-



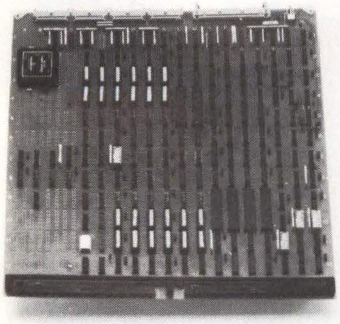
tem by simply touching the area where information is displayed on a CRT screen. The CRT add-on kits utilize a capacitance-sensitive faceplate which is mounted in front of the CRT monitor of the terminal. It does not employ mechanical contacts, nor active electromagnetic or acoustic elements. Standard kits are provided in 32 touch-position configurations for 12″ and 15″ (diagonal) CRT monitors. Standard electronic outputs are provided for either parallel or serial interfaces. Custom configurations are also available. The CRT add-on kits are $300 in Qty, 90 days ARO. **Interaction Systems Inc,** 24 Munroe St, Newtonville, MA 02160. **Circle 232**

PRINTER MODULE is a direct replacement for the Logic A circuit boards used in the Printronix line printers. It provides a 96 character



upper and lower case ASCII set at 10, 13-1/3 or 16-2/3 cpi. Double high characters may be generated in each of the character sets. Optional character sets may be ordered for 1056 printable characters. TRILAX provides standard ASCII, two densities of compressed ASCII, block characters, bar codes and special character sets. Each is selectable by software command. It prints up to 220 characters on full width, or 132 characters on 8-1/2″ width paper. A switch or software selectable feature allows printing at either 6 or 8 lines/in. **Trilog, Inc.,** 17391 Murphy Ave, Irvine, CA 92714. **Circle 127**

EMULATING DISK CONTROLLER provides total emulation of the MSM-80 and MSM-300 Perkin-Elmer disk subsystems while attaching up to 4



80MB or 300MB compatible drives. Through expanded emulation, SMD drives of any capacity can be attached. Complete compatibility with the full range of P-E 16- and 32-bit minis is provided by the SPECTRA 14. Its dual bipolar μP design controls both the CPU channel and disk interfaces simultaneously, accommodating the 2MB/sec transfer rate. Included are on-board self-test microdiagnostics and a 32-bit ECC. Spectra 14 is $4500/25. **Spectra Logic Corp,** 2316 Walsh Ave, Santa Clara, CA 95051. **Circle 184**

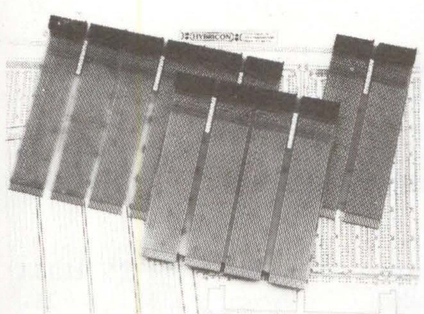
DEC CONTROLLERS. These controllers interface Mannesmann Tally printers with PDP-11 LSI-11/24 and VAX computers. Featuring single-card construction, the controller fits into the DEC UNIBUS without hardware or software modification. The printer controller can be used with both serial and line printers from 160 cps to 300 lpm. The controller is compatible with all DEC operating systems. A self-test capability, isolated from the computer, sends a 96 character ASCII test pattern to the printer. The self-test can locate faults to the printer, controller or computer. For addressing, 12 position DIP switches allow the status, data and vector registers to be addressed in any available I/O space in the host computer. **Mannesmann Tally,** 8301 S. 180th, Kent, WA 98031.

Circle 226

DATA TEST SET PRINTER provides a permanent, unattended record of data interface test results. It is designed to operate with the WECo 1ARDT (Radio Digital Terminal) and WECo 914B Data Test Sets equipped with the IDS Model 25 Full-Duplex Long Word Converter Kit or the Model 15 Full-Duplex Adapter Kit. The printer can be used on-line to obtain a record of failures of critical signals or off-line for a record of data errors, block errors, and failure of EIA interface signals. Features include a pre-settable real time clock, 3 selectable print routines, 6 selectable trigger channels, and 7 selectable print intervals. Model 2910 is $4410. Also available is a pocket-size interface monitor that provides access to all 25 conductors of the EIA RS-232-C (CCITT V.24) Interface between a data modem and data terminal. Installed on-line at the data interface, it uses 12 LEDs to monitor line conditions of the most commonly used EIA signals. An additional LED allows any other EIA signal to be monitored. Test points provide access to all 25 conductors of the EIA interface and allow the connection of meters, oscilloscopes, or logic analyzers for additional signal analysis. The Model 50 requires no external power and has no moving parts. ($140). **International Data Sciences, Inc,** 7 Wellington Rd, Lincoln, RI 02865. **Circle 229**

5 1/4" DISK DRIVE is available for the 6809-series of Chieftain small business computers. The drive's double-track, double-bit, and double-sided design provides 1.5MB of formatted storage capacity in its standard dual-drive configuration. Chieftain Model 9524 also incorporates 32K RAM, 2 serial ports, monitor in ROM and SSB's DOS69. Recording density of the drive is 5,877 bpi with 80 tracks/side. Track-to-track time is 3 ms at 96 tpi. The Chieftain Model 9524 is $4,075 with OEM and dealer discounts available. **Smoke Signal Broadcasting,** 31336 Via Colinas, Westlake Village, CA 91362. **Circle 217**

EXTENDER BOARDS. This line of Extender Boards is compatible with DEC products. All cards use gold plated, double looped test points on every connection between the card under test and the backplane. Each test point is identified with the connector contact number and is arranged in a staggered fashion so that probes



can be attached without danger of short circuit. The double loop configuration allows test probes to hang at any angle, thus preventing damage to probes and eliminates fall-off from pull stress. DE2ET, compatible with the Dual Board, $65; DE4ET, compatible with Quad Board, $119; DE6ET, compatible with the Hex Board, $165. All come with the connectors and double looped test points installed. **Hybricon Corp,** 410 Great Rd, Littleton, MA 01460. **Circle 228**

INCREASED WCS. A 4096 word Writable Control Store (WCS) for the family of System 3400 raster-scan display processors is a 4X increase over the previous 1024 word WCS capacity. Users will be able to program extensively and directly into the microcode of a display, various high-speed graphics and image manipulation functions that previously had to be hardwired or done in much slower host CPU or intelligent front-end software. The 4K WCS Option is $2500. DEC and DG cross-assemblers are $750. **Lexidata Corp,** 755 Middlesex Tpke, Billerica, MA 01865. **Circle 202**

Product Index

To obtain detailed information on ads appearing in this issue use the Reader Inquiry Card. Circle appropriate numbers (as many as you desire), detach the card from binding and mail to *Digital Design*.

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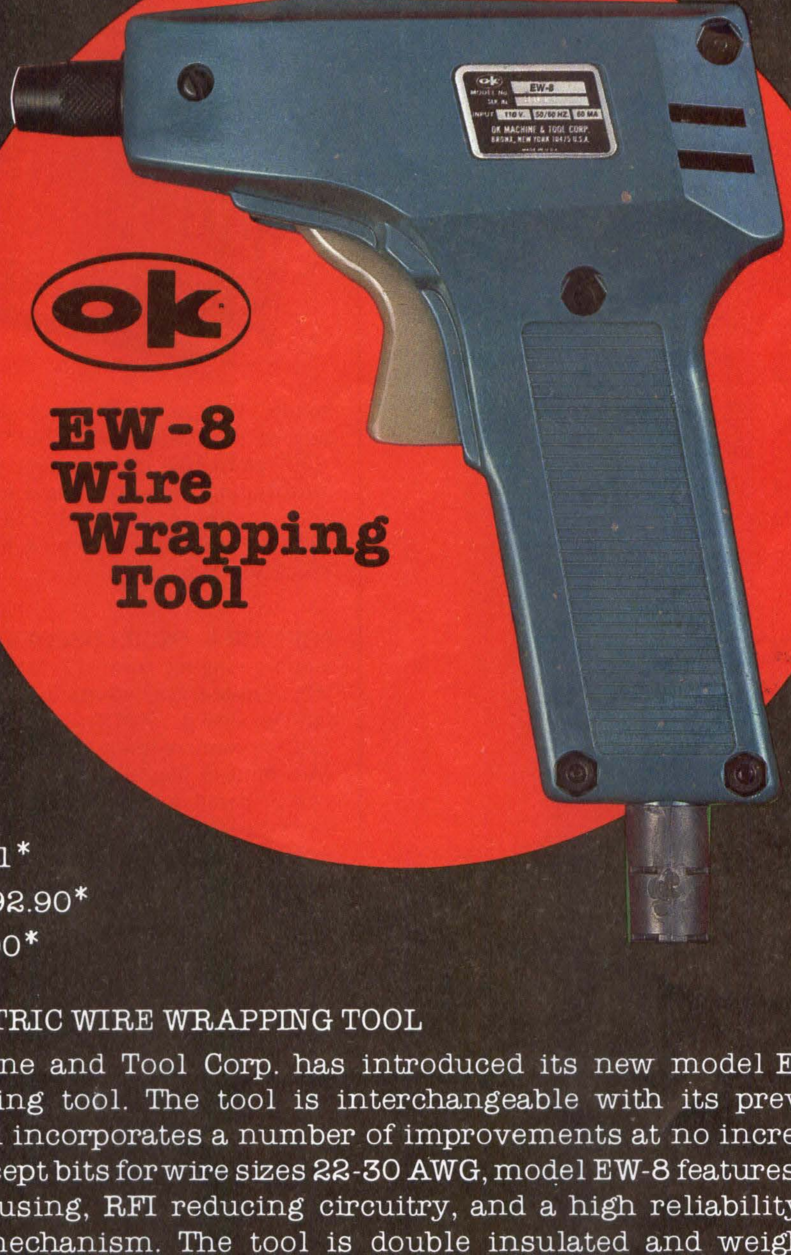


EW-8 $85.11*
EW-8-BF $92.90*
VIT-1 $15.00*

NEW ELECTRIC WIRE WRAPPING TOOL

O.K. Machine and Tool Corp. has introduced its new model EW-8 electric wire-wrapping tool. The tool is interchangeable with its previous model EW-7D, and incorporates a number of improvements at no increase in price. Rated to accept bits for wire sizes 22-30 AWG, model EW-8 features a reinforced Lexan(TM) housing, RFI reducing circuitry, and a high reliability motor and indexing mechanism. The tool is double insulated and weights only 14 ounces. Available with optional anti-overwrapping device as model EW-8-BF. Also available with accessory tool VIT-1 which permits easy resetting of indexing position in 45 degree increments.

Available ex-stock from

(TM) General Electric

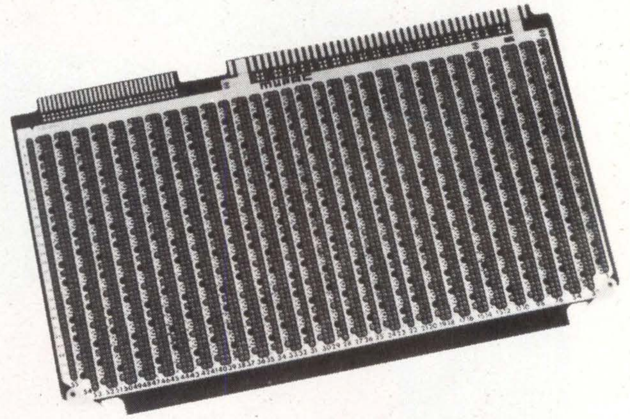
OK Machine & Tool Corporation
3455 Conner St., Bronx, N.Y. 10475 U.S.A.
Tel. (212) 994-6600 Telex 125091

*Minimum billings $25.00, add shipping charge $2.00
New York State residents add applicable tax

Circle 32 on Reader Inquiry Card

New Products

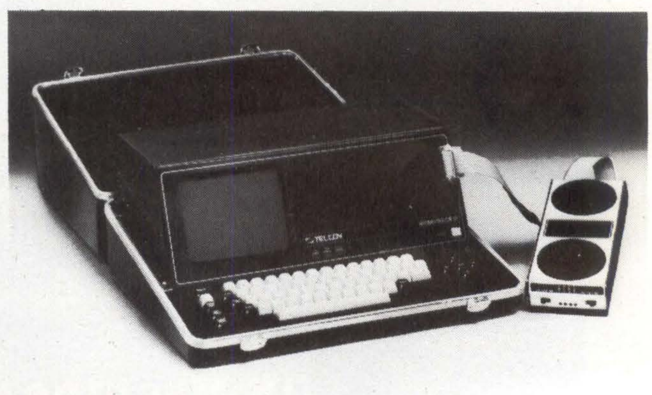
WIRE WRAPPABLE PANEL. This MULTIBUS compatible high density universal wire wrappable panel can package up to 150 ICs and has the same outline as the SBC80 family of



boards. The universal layout of wrappable pins allows plugging of devices with leads on .300, .400, .500, .600, .700, .800, and .900 inch centers plus others. It is suited for prototyping and evaluating single board computers. The 1-9 price for the panel is $397.90 with gold plated pins and $353.63 with tin plated pins. **Mupac Corp,** 646 Summer St, Brockton, MA 02402. **Circle 189**

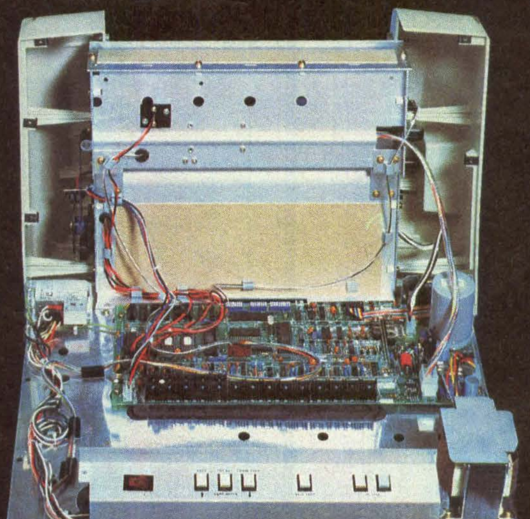
PORTABLE OSCILLOSCOPE. The 500 Series consists of models ranging from 12 MHz to 60 MHz, including: 60 MHz triple-trace, alternate sweep. 40MHz triple-trace, alternate sweep. 40MHz triple-trace, versatile trigger, with built-in counter-timer, 40MHz triple-trace, versatile trigger, with built-in digital multimeter. 12MHz dual-trace triggered sweep, parallax-free graticule. 12MHz single-trace triggered sweep, parallax-free graticule. Special features include light weight, with a data readout option. Brochure available. **Soltec Corp,** 11684 Pendleton St, Sun Valley, CA 91352. **Circle 196**

PORTABLE TERMINALS. Weighing less than 20 lbs, the Ambassador III includes built-in 300 baud acoustical coupler. The Ambassador IV provides a built-in 80 column



printer with electric discharge at 2 lps. Both feature a selectric-style keyboard offering characters, numbers, symbols, and function keys. Full 7″ diagonal screens provide 24 X 80 character display using 128 ASCII character set. The terminals work in both page or character mode and feature transmission in 7 or 8 level code at a data rate keyboard selectable from 110 to 9600 baud. **Telcon Industries, Inc,** 1401 NW 69th St, Fort Lauderdale, FL 33309. **Circle 174**

Say Ahh...



Our New grafixPLUS™ 80-column printer opens wide for easy servicing.

Introducing the newest members of our grafixPLUS™ family—the DP-9000 Series 80/132 column printers—built on the same tradition of quality printout, solid design and low cost of ownership established by our 132/220 column DP-9500 Series.

A Case for Serviceability

Not that is comes up often, but want to get inside? Simple. Just remove a few screws and the clam-shell case swings open exposing all major components. This easy access plus built-in self-test and minimum component count yields an MTTR of one-half hour. The 9-wire print head replacement's even simpler . . . two screws and it's out. Without opening the case. And without a service call.

Performance Plus

The DP-9000 Series prints the full ASCII 96 character set, including descenders and underlining, bi-directionally, at up to 200 CPS. Number of columns can go up to 80 or 132, depending on character density—switch or data source selectable from 10 to 16.7 characters per inch. And all characters can be printed double width. The print head produces razor-sharp characters and high-density graphics with dot resolutions of 72X75 dots/inch under direct data source control.

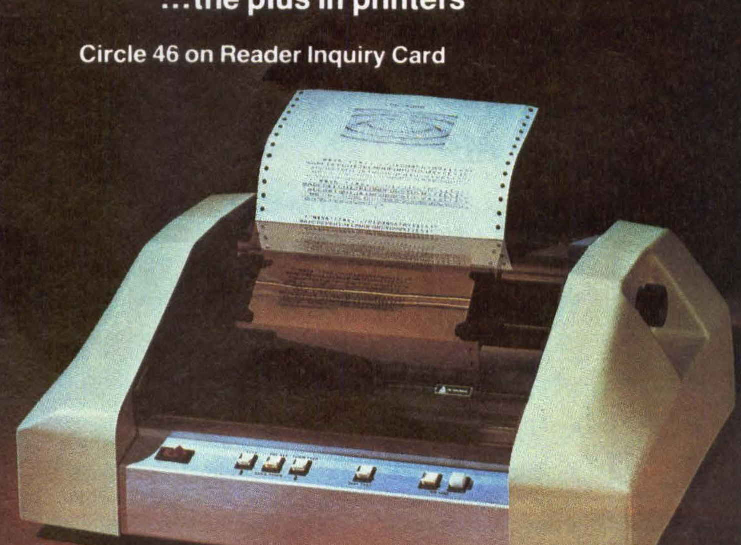
Interface Flexibility

The three ASCII compatible interfaces (parallel, RS-232-C and current loop) are standard, so connecting your computer is usually a matter of plug-it-in and print. Also standard are: a sophisticated communications interface for printer control and full point-to-point communications, DEC PROTOCOL, and a 700 character FIFO buffer. An additional 2K buffer is optional.

When you're ready for a printer (or several thousand), look into the grafixPLUS DP-9000 Series from Anadex—you'll find an open and shut case for quality. Contact us today for details, discounts and demonstrations.

Anadex®
...the plus in printers

Circle 46 on Reader Inquiry Card



. . . close please.

SALES OFFICES: San Jose, CA (408) 247-3933
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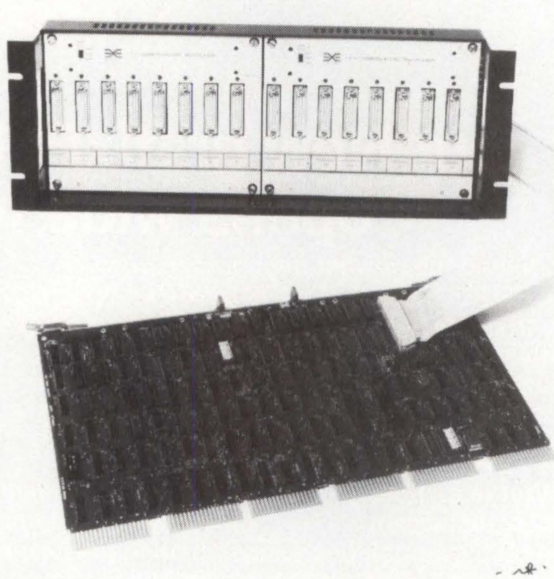
Circle 46 on Reader Inquiry Card

New Products

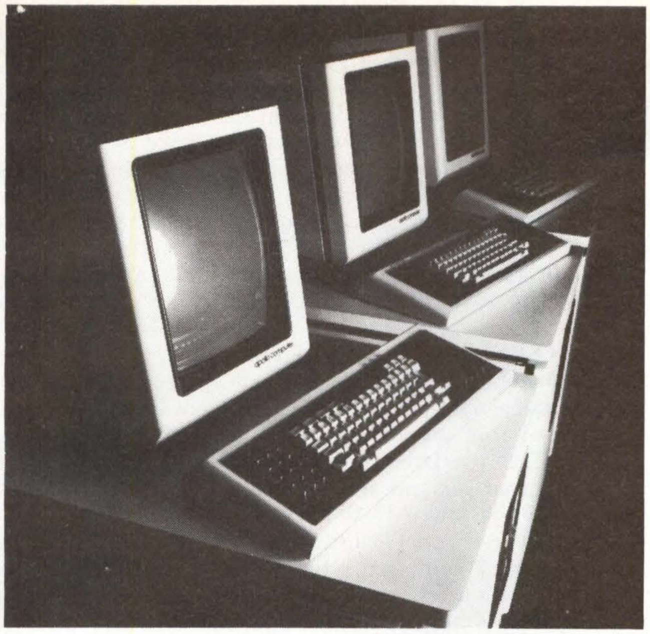
TELEPRINTER TERMINAL. This daisywheel terminal features a programmable keyboard, non-volatile memory and bi-directional printing. Optional text enhancements include proportional spacing, bold face printing, automatic centering, justification and underscoring. Its non-volatile memory stores margins, tab settings, forms control and program key settings, pitch and plot modes. Print speed is 45 cps. A full 128 ASCII character set is standard. The AJ 833 operates at selectable rates of 110, 150, 300 or 450 bps, and optionally at 600 or 1200 bps. A 2 kB internal buffer is expandable by 32 kB. ($3995). **Anderson Jacobson, Inc**, 521 Charcot Ave, San Jose, CA 95131. **Circle 201**

DEC MULTIPLEXER SUBSYSTEM provides DEC's DH11 multiplexer with improved line handling capabilities. The CS11/H communications multiplexer connects up to 64 async communications line devices to a single controller board within the CPU backplane. Additional lines may be connected by adding a communications controller card to



the CPU and line adapter cards to external distribution panels. The multiplexer uses a single hex size circuit board for the Communications Controller. This is connected by a 34-conductor ribbon cable to up to 4 CP11 Distribution Panels, each with its own integral power supply and either one or two 8-channel CA11 Line Adapters. The line adapters provide data and modem interface circuitry plus UART-type circuitry for serial-to-parallel and parallel-to-serial conversions. The UART's also have a baud rate generator. Line adapters may be configured initially for either RS-232 or current loop interface standards. All of the line-interfacing variations are located outside the CPU eliminating restructuring the CPU chassis or adding expansion boxes to accommodate additional lines. A basic configuration of one controller and one distribution panel with adapters for 16 channels is $5800. To expand in increments of 8 lines, an additional panel and an 8-line adapter is $2500. To expand in increments of 16 lines, and additional panel and two 8-line adapters is $3900. OEM discounts available. **Emulex Corp**, 2001 East Deere Ave, Santa Ana, CA 92705. **Circle 140**

NETWORK PROCESSING SYSTEM. The DOMAIN (Distributed Operating Multi-Access Interactive Network) processing is based on a high-performance local network of dedicated computers in a distributed environment. It has the advantages of both timesharing and dedicated minicom-

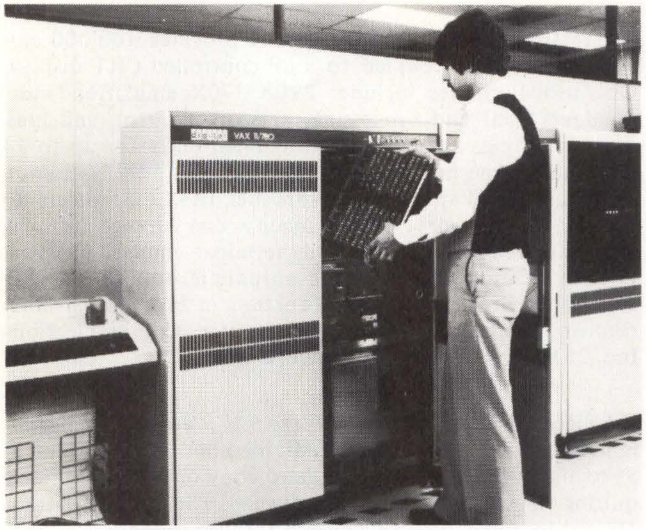


puter technology. Features include: a VLSI CPU (with 32-bit architecture) dedicated to each user on the network, a high-resolution bit map display permitting each user to run multiple programs simultaneously, and network-level modularity providing a wide range of growth capability. The essence of DOMAIN is a network of nodes. Each user can access his own data or his neighbor's with comparable speed and functionality. The failure of one node will not affect the performance of another. The display system supports multiple windows into different processes. These windows can be presented side-by-side or overlaid in whole or part. While there are several basic nodes on the network with which to build complex applications, the Computational Node is the backbone of the system. Additional nodes include the Peripheral Node for shared peripherals such as line printers and magtapes. The Computational Node will sell in the low $20,000 range. **Apollo Computer Inc,** 5 Executive Park Dr, N. Billerica, MA 01862. **Circle 208**

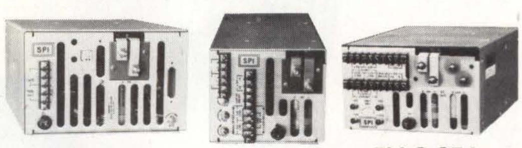
COMMUNICATIONS PROCESSOR provides 400,000 cps, sync throughput coupled to a μP controlled CRT display. Operational modes include: 270X/370X emulation, independent front end processing, network control, and message switching, all with plug-in compatibility for up to 14 IBM mainframe host computers. Handling up to 1232 lines, in a mixture of speeds and protocols, the CC-85 offers up to 512 kB memory, large capacity disk storage options, automatic baud-rate detection, terminal emulation, dynamic application selection and automatic polling. The μP-controlled CRT display can function in supervisor, monitor or engineering modes. **Computer Communications Inc,** 2610 Columbia St, Torrance, CA 90503. **Circle 177**

MATRIX PRINTER. This 125 cps 9 X 9 dot matrix printer is designed for Intel's Intellec Microcomputer Development Systems. It provides low cost, hard copy output without requiring special hardware or software. The printer, with a 10′ cable, plugs directly into all Intellec models. An automatic on/off control allows the printer to be activated directly from the Intellec console. The MDP-125 features bi-directional operation, 96-character ASCII character set with true upper and lower case characters, plus underlining, and produces an original plus 5 copies. $1235, (80-col); $1345, (136-col). **EMC Corp,** 385 Elliot St, Newton, MA 02164. **Circle 178**

VAX-11/780 ADD-IN MEMORY. This plug-in memory card for DEC's VAX-11/780 comes in either 512 kB or 1,024 kB versions. The module is organized as 64K or 128K



words of 72 bits each, and may be used to expand basic VAX-11/780 memories up to 4 MB. The MU-5780 operates at speeds determined by the VAX-11/780 memory controller with which it is both hardware- and software-compatible. Typical READ cycle and access times are 530 and 250 ns. In 3- to 5-unit qty, the 512 kB MU-5780 is $4,350; the 1,024 kB version is $8,400. **Intel Corp,** 1302 N. Mathilda Ave, Sunnyvale, CA 94086. **Circle 132**



ENCORE 100 FLEXIBLE DISK. This Flexible Disc Unit is an alternative to the Mag Tape Unit for the ENCORE 100 Datacom diagnostic system. ENCORE 100 permits both passive monitoring of the data links and interactive simulation of the system hardware and software components. The double-sided, dual-density Flexible Disc Unit operates at speeds 4 to 20 times faster than the tape drive with data and RS-232 interface status recorded from a 56K bps half-duplex line. The ENCORE 100 with flexible disc is $21,000. The flexible disc alone is $3,875. **Digitech Ind., Inc.,** 66 Grove St., Ridgefield, CT 06877. **Circle 215**

MULTIPLEXER-A/D CONVERTERS. Designed for high-speed analog data multiplexing and A/D conversion between analog data sensors and a μP, the converter series consists of four monolithic CMOS devices. Each contains a multiplexer, A/D converter, and μP compatible control logic. All four versions are identical in function except that the ADC0808 and ADC0809 contain a 3-bit address decoder and 8-channel multiplexer, while the ADC0816 and ADC0817 contain a 4-bit address decoder and a 16-channel multiplexer. 100-Piece price: ADC0808N, $15.84; ADC0809N, 4.32; ADC0816N, 17.28; ADC0817N, .58. **Texas Instruments Inc.,** Box 225012, M/S 308, Dallas, TX 75265 **Circle 212**

DEC COMP. AC POWER CONTROLLLER is interchangeable with DECs Model 861 and sells for 40% less. It features 12 outlet receptacles, 4 direct outlets for auxiliary and maintenance equipment and 8 "switched" outlets that can be controlled either locally or remotely. The unit also features differential and common mode type EMI line filter. It has 2 I/O connectors for remote enable and disable of one or multiple units. Optional delayed output for AC power sequencing of multiple units is available. The 115/230 is $265/10. With delay output option included, $285/10. **Marway Products, Inc.,** 2421 S. Birch St., Santa Ana, CA 92707 **Circle 213**

ADD-IN MEMORY BOARD offers lower power dissipation. It has 128K X 22 capacity on a 15″ X 15″ X 44″ card, and is hardware and software compatible with DG ECLIPSE computers. The power characteristics are: for +15 volts, .1A max standby and .65A max active; for +5 volts, the max standby and active are both 3.7A; for –5/–15 volts, both max standby and active are 12/35 mA; and for +5 volts backup, the max standby and active is .65A. Three error correction options and on-board LEDs allow analysis at RAM level while running the diagnostics. Error correction options are Independent ECC either 21 or 22 bits; Dependent ECC generated on-board; and 16-bit non-ECC with no ECC bits on-board. The MK8024 carries a full year warranty. $5,810 with OEM, educational and government discounts available. **Mostek Corp,** 1215 W. Crosby Rd, Carrollton, TX 75006. **Circle 195**

PROGRAM SECURITY SYSTEMS are available for HP 9835A and 9845E/C desktop computers. OEMSEC enciphers the stored version of a program and irreversibly alters its structure. The program will run normally but cannot be edited or modified an a way that accesses any of the existing program symboles. Any attempt to list the program will produce meaningless garbage. ($2000). With NODUP, software is protected against duplication. It protects programs stored on tape cartridge and continues to provide protection if the programs are loaded onto either floppy disc or hard disc for production use. A program will run normally when loaded from the original tape cartridge or can be loaded from disc as long as the original tape is in the drive. ($2500). **Structured Software Systems, Inc,** Box 1072, Irick Rd, Mt. Holly, NJ 08060. **Circle 129**

(continued from page 42)

Transformation Function	Function which modifies a Display by introducing Rotation, Scaling or Translation.
Translate	To transform a Display Item on the Display Surface by repositioning it to another Coordinate location.
Triad	Three Electron Guns grouped in a triangle for use with a Shadow Mask, with each gun responsible for either the red, green, or blue color component.
Unposting	Setting the Visibility Segment Attribute to "off".
Valuator Device	A Graphic Input Device, such as a Control Dial, that inputs scalar values within a user defined range.
Vector	A directed Line Segment.
Vector Generator	Device which takes Coordinate data and converts it to deflection signals for the Electron Gun.
Vertical Retrace	Turning off and repositioning the Electron Beam to the upper left corner of the Display Surface after the last Scan Line has been drawn during Raster Scan.
Whiteness	A characteristic of color defining its percentage ranking on a scale from light to dark.
Window	Specified area on the View Plane containing the projections to be displayed.
Window Clipping	Bounding of a View Volume in the X and Y directions by passing Projectors through the corners of the Window to define its sides.
World Coordinate System	The device independent coordinate system used to define Objects meant for display.
World Coordinate Transformation	A transformation which transforms the World Coordinate System of a Model to the default World Coordinate System of a Graphics Package which is in effect immediately prior to a Viewing Operation.
Wraparound	Positioning a Display Item so that it overlaps the border of the Device Space, resulting in a display on the opposite side of the Display Surface.
Yon Plane	Back clipping plane used in Z-Clipping to define a finite View Volume.
Z-Clipping	The bounding of a View Volume in the Z direction by defining a Hither Plane and a Yon Plane parallel to the View Plane.

(continued from page 46)

the screen. The old image is simply replaced by the new image in the space of a single refresh cycle (typically one-thirtieth of a second). This releases Buffer 1 to receive a new image. By toggling back and forth between these two buffers, real-time dynamics can be achieved incorporating true scaling, panning through the 4096 × 4096 data base, and allowing a variety of other real-time modifications of the display.

Selective erase

The 6250 erases a vector by deleting it from the display list. Then on the next vector processing cycle (typically one-twentieth or one-thirtieth of a second, depending on the length of the display list), the display image is regenerated without the vector. But no "holes" are left in its place.

The 6250 allows local "decluttering" without requiring retransmission of data. By appropriately organizing the data to be displayed, portions of the data can be turned "on" or "off" (displayed or not displayed) depending on detail the operator wishes to observe. Most of the detail can be turned off when viewing the entire image, and then recalled as the image is scaled. Only the detail appropriate to the scale factor need be on the screen at a given time.

Increased productivity

These capabilities have real meaning in the production-oriented CAD/CAM environment. Design applications require frequent modifications of a display. Most raster displays require blanking the screen and retransmitting the entire display from the host computer, a process which can take from several seconds to a minute or more. This "repaint" process is costly production-time lost and a very unfriendly interface to the engineer/designer. The 6250 minimizes such inefficiencies.

Intelligent peripheral control unit

Real-time vector processing in the WHIZZARD 6250 is complemented by local handling of graphics peripherals, again off-loading the host computer. The Intelligent Peripheral Control Unit (IPCU) is a microprocessor-based interface to the 6250 system for the keyboard and joystick, and an optional data tablet. The microprocessor-based IPCU provides an interface between the graphics and peripheral buses, significantly reducing the host computer loading required to service peripheral interrupts. The IPCU also performs local tracking, updating status registers in Vector Memory with position information, without interrupting the host computer. Characters can be entered from the keyboard into a user-defined scrolling text area of the screen. The joystick or tablet can control a locating cursor on the screen without host interaction.

Price/performance

Looking into the future and, as stated above, we expect to see an increase in performance in low to moderately priced graphics systems and terminals. Megatek's WHIZZARD 6250 brings that future into today's market. It brings with it some of the highest performance raster technology available at a terminal price much lower than previously available. The production savings that CAD/CAM allows will be expanded to a much broader customer base than was ever possible. Potential users who might otherwise postpone CAD/CAM implementation because of the cost now have an alternative in Megatek's WHIZZARD 6250.

Designers' Notebook

Designing a μP-Based Energy Control System

System designers can extend system performance by using single-chip μCs to take over functions normally handled by the larger system. Although the following set/back-set/forward thermostat timer was designed as a stand-alone unit, it is an example of such subsystems that can extend system performance.

This subsystem could replace an existing mechanical one. I will describe it briefly as a full spec would be too long. It has four 7-segment displays, eight annunciators, triac control of heater and air conditioner, A/D for indoor/outdoor temperatures, nine touch-control key-pads and two options (12- or 24-hr. operation/°C or °F). Upon power-up, everything is cleared except the clock, which reads 12:00 AM if in the 12-hr. mode, and 12:00 if in the 24-hr. mode. The mode button cycles through the clock, indoor/outdoor temperature, time-period one, two, and three. While in clock mode, the clock can be set or cleared. The indoor/outdoor temperatures are just displayed. Time periods ONE, TWO and THREE are the settable control periods. During each period, the start-time, stop-time and temperature are settable. The user can also choose either a HI or LO temperature. The increment button increments by 1 at a 2-Hz rate for one second and 10Hz for the next 5 sec., and 100Hz from then on (if the button is held).

A good spec goes into great detail about system requirements. Data entry via the front panel must be defined on error conditions and how their states are reported (does the display flash or blink or an annunciator come on?). Is there battery back-up when power goes out? If so, what information is saved? Or, to conserve power, have the display active when there is keyboard activity: after a certain period, the display would automatically turn off. For additional features, the times/temperatures could be set on a weekly basis; on weekends, temperature patterns more closely reflect living patterns by having 7-day-of-the-week flags and set times and temperatures for each day. You must take all these things into consideration and define them before designing. Although reality is never so well-defined intitial planning cuts spec changes and makes your project go a lot smoother.

Next, finding the right processor means **the least-costly, most-reliable system.** It may be cheap, but if it requires additional support chips or discrete components, is it your system solution? Perhaps not. Since 4-bit single-chip μPs are now more powerful and less costly, they often are best.

In our case, we knew we needed much external hardware or an 8-bit processor (especially for A/D). Even to do a keyboard with options and annunciators seems like a lot; however, if the keyboard and display are multiplexed and A/D is done on-chip – as with the S2200, for example, then the system is rather simple.

S2200 has 2048 bytes of ROM on-chip for program storage, which can be expanded to a total of 8192 on- and off-chip, and 128 nibbles of RAM for variable storage. It has an 8-bit ADC and two-level, maskable priority-interrupt stack with provision for a software interrupt. There is a programmable 8-bit timer/event counter on-chip and table look-up capability. There are 13 outputs, 8 bidirectional three-state lines, and 8 independently software-defined I/O lines.

I/O assignments, an important step, were not made arbitrarily. Multiplexing the keyboard/display is a must. On one 40-pin chip, there are too few pins. The same A (output) lines can be used as the strobe for both the row of keyboard and display. Display data is output via D lines; keys are read via K lines. Jumbered options are also read via a K line. Heater and air conditioner are controlled via A line to triacs. The A/D for indoor/outdoor temperature each come in on a K line. Those are the system I/O.

Assignment of A lines for display/keyboard were made with RAM assignments in mind. Your RAM map will differ from ours. In the S2200, the line is strobed by presetting BL (lower 4 bits of RAM address) to correspond to the desired A line. For the display, if data is in the RAM location pointed to by BL, then no separate code is needed to get data to display. Data to be displayed in digit one is in RAM location 01.

```
LAI   1   ; Load Accumulator with 1
            (digit one)
XAB       ; Set BL = 1
PSH       ; Preset High A Line Selected
            by BL
LAM   0   ; Data Out of RAM Location
            01 to Accumulator
MVS       ; Strobe A1
DISN      ; Output the Data from the
            Accumulator
PSL       : Preset Low A Line Selected
            by BL
```

If data were in location 0A, and the A line to digit one was still one, then the code would be:

```
LAI   1   ; Load Accumulator with 1
            (digit one)
XAB       ; Set BL = 1
PSH       ; Preset High A Line Selected
            by BL
LAI   $A  ; Load Accumulator with $A
            (where the data is kept)
XAB       ; Set BL=$A (to address the
            RAM where the data is kept)
LAM   0   ; Data Out of RAM Location
            01 to Accumulator
MVS       ; Strobe A1
DISN      ; Output the Data from the
            Accumulator
PSL       ; Preset Low A Line Selected
            by BL
```

To output all four of the digits the codes might be:

```
LAI   0   ; Load Accumulator with 0
            (digit zero)
XAB       ; Set BL = 0
PSH       ; Preset High A Line Selected
            by BL (set to strobe A line)
LAM   0   ; Data Out of RAM Location
            00 to Accumulator
MVS       ; Strobe A0
DISN      ; Output the Data from the
            Accumulator
PSL       ; Preset Low A Line Selected
            by BL (set to unstrobe A line)
*
LAI   1   ; Load Accumulator with 1
            (digit 1)
```

```
XAB          ; Set BL = 1
PSH          ; Preset High A Line Selected
               by BL
LAM    0     ; Data Out of RAM Location
               01 to Accumulator
MVS          ; Strobe A1 – Unstrobe A0
DISN         ; Output the Data from the
               Accumulator
PSL          ; Preset Low A Line Selected
               by BL
 *
LAI    2     ; Load Accumulator with 2
               (digit 2)
XAB          ; Set BL = 2
PSH          ; Preset High A Line Selected
               by BL (set to strobe A line)
LAM    0     ; Data Out of RAM Location
               02 to Accumulator
MVS          ; Strobe A2 – Unstrobe A1
DISN         ; Output the Data from the
               Accumulator
PSL          ; Preset Low A Line Selected
               by BL (set to unstrobe A line)
 *
LAI    3     ; Load Accumulator with 3
               (digit three)
XAB          ; Set BL = 3
PSH          ; Preset High A Line Selected
               by BY (set to strobe A line)
LAM    0     ; Data Out of RAM Location
               03 to Accumulator
MVS          ; Strobe A3 – Unstrobe A2
DISN         ; Output the Data from the
               Accumulator
PSL          ; Preset Low A Line Selected
               by BL (set to strobe A line)
MVS          ; Unstrobe A3
```

Now, to carry this one step further and put the sequence in a loop optimize the code.

```
(Loop)
LAI    3     ; Load Accumulator with 3
               (digit 3)
XAB          ; Set BL = 3
PSH          ; Preset High A Line Selected
               by BL (set to strobe A line)
LAM    0     ; Data Out of RAM Location
               01 to accumulator
MVS          ; Strobe A – Unstrobe A
DISN         ; Output the Data from the
               Accumulator
PSL          ; Preset Low A Line Selected
               by BL (set to unstrobe A line)
JMS    Delay
XC     0     ; This Pair of Instructions
               Decrements the BL Without
               Destroying
XCD          ; Any Data in RAM – and
               Loops until BL = 0 before
               the Decrement
JMP    Loop
```

So, for a couple of added instructions, all data are output. We added the delay routine so each digit is left on for a length of time depending upon the required duty cycle.

Once the system definition is complete, make a macro flowchart. It shows program flow and logical re*lationship* between program parts. Writing the program in modular form reduces coding and debugging, and permits developing routines useful in subsequent programs. For example, a time-of-day clock in this program would also be useable in any timer application (such as a microwave or conventional oven controller). It's important to use an executive type controlling sequence to minimize code. The program breaks down in convenient blocks (keyboard scan, display scan, etc).

The S2200 adapts well to modular programming; it contains a 5-level stack (uncommon in 4-bit μCs). If interrupts were used, the stack would only be three levels deep. The stack is useful where there is insufficient ROM for redundant code (usually the case).

S2200 A/D begins by starting conversion with instruction "SANG" and waiting for 10 cycles; then, reading the analog register into RAM and accumulator with instruction "RANG." In our thermostat, A/D is used to measure indoor/outdoor temperatures. To convert to degrees Celcius or Fahrenheit, table look-up could be used. There could be two tables – one for Celcius; one for Fahrenheit. Or, a conversion routine could convert one to the other.

The four-bit μCs are easy to design and use. Programming is slightly different because instruction sets are not complex (as with 8- or 16-bit μPs.) One is dealing with bits and nibbles here, rather than with bytes and words. However, it is just as important to follow good programming practices.

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Telecommunications for Terminal Users

With the number of data communication devices available and their growing user base, an understanding of these products and their functions can save system designers some headaches.

Some Basic Definitions

Modem is a contraction of the terms Modulator – Demodulator. The phone system is designed to handle voice communications in a frequency range of 300 Hz to 3300 Hz. Since we are attempting to transmit data (or digital signals) through that telephone system, signals must be conditioned to operate in the environment designed for voice.

Why use the phone system for transmission of data? Simple: it reaches nearly every point in the world.

In data communications jargon, *simplex* means *broadcast* – very much like a TV station broadcast to a TV receiver. The station sends out the signal blindly, expecting no response at all; of course, your receiver must be tuned to the proper channel.

Half duplex is similar to two Ham radio operators who state "over" at the end of each transmission so that the receiving party (or terminal) "recognizes" they may begin transmission. This sequence is called a communication *Protocol.*

With modems, signals called RTS (Request to Send) and CTS (Clear to Send) are generated from the terminal and computer to determine which unit can transmit. Half Duplex communication is strictly ONE WAY at any time.

Full Duplex means that both ends can transmit and receive *simultaneously.* Full Duplex also infers that the data rate in each direction is identical.

Again, talking about *half duplex* – if modem A wants to transmit to modem B, the *terminal or computer* associated with modem A must raise a signal in it's interface called Request to Send (RTS), which is similar to "over" for the Ham operator, only it is at the beginning rather than the end of the transmission. The system protocol and software determine what the individual characteristics are for any specific installations.

From the *Users* standpoint, be certain that the terminal, computer, and everything in between can support the "Request to Send – Clear to Send" handshake if you plan to or are using "half duplex" modems. These would be equivalent to the Bell 202, 201, 208 or 209 types.

Full Duplex, as we mentioned, means simultaneous bi-directional communications. In data communications, it means that the modem is essentially invisible to the link between the terminal and the computer. Full Duplex in data communications terminology means that the link between the terminal and computer is totally transparent – as if the terminal was "hardwired" to the CPU. There is a switch on most terminals labeled Half Duplex (or Local Copy) vs Full Duplex (possibly "Echo").

In "terminal terminology", the terms previously discussed under modems have a *totally different* meaning.

In a terminal, the *half duplex* (local copy) mode means that the character generated by a key stroke is sent to the display (CRT or printer) and to the modem (or computer) at the same time.

Full duplex mode with a terminal means that the character is sent to the computer and is echoed back before being displayed.

There is a reason for this important distinction. Most minicomputers were constructed to work with local terminals. If a terminal is *directly* connected to a computer, few errors in transmission/reception can result; but as soon as modems and the telephone lines are used, errors can occur.

The most rudimentary form of error detection is the operator seeing if the character displayed is the same as a keystroke. Full duplex – echoplex operation provides this feedback.

Bear in mind that the terms "Half" and "Full Duplex" have different meanings for terminals vs modems.

Telephone Networks

Some understanding of the telephone network is important to make the proper selection of modems.

The phone line from your location to the phone company's central office is called a subscriber loop. The subscriber loops are made up of a *pair* of wires (two-wire circuit). At the central office, the pair is run through a "Hybrid" circuit that splits traffic into transmit and receive pairs between central offices.

Amplifiers and echo suppressors exist in the circuit to allow traffic to flow only in one direction on that wire pair. Another circuit component is a loading coil. Remember that the telephone system was designed to pass voice frequencies (300 Hz to 3300 Hz) and any modems must live with this frequency bandwidth constraint.

Sometimes when using the telephone, a call must be re-dialed because of noise, cross talk, or echos on the line. When this happens, the odds are good that the re-try will produce a better line. With modems in the dial-up environment, the same thing can happen.

Whether to run your terminals via dial-up or leased lines is purely an economic decision and involves comparing toll charges to monthly lease rates. A leased line will average $4/mile/month.

The 103 type modem is the most common device to be found in use. All time-shared computer services offer 0-30 character/second (0-300 bps) service using 103 type modems. It is a full duplex modem using two "sub-carriers" within the telephone bandwidth.

Two areas of confusion exist with 103 type modems: (1) The 103 has the ability to automatically switch from the "originate" mode to the "answer" mode upon detection of a Ring signal. Whereas the 113 A is "originate" only and the 113 B is answer only! (2) The terms *originate* and *answer* relate only to the frequencies modems use for transmit and receive – not to who starts or receives the call.

Pricing varies depending on the specific telephone company, but this shows the average charge to expect. An equivalent/Bell compatible modem from an independent supplier can be purchased for about $375. Quick cal= culations show that buying vs renting will pay off within 10 months.

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