Digital Scientific META 4™

COMPUTER SYSTEM READ-ONLY MEMORY

(ROM)

REFERENCE MANUAL

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1.0 INTRODUCTION

The Digital Scientific META 4™ Computer System Read-Only Memory (ROM) * was designed for speed compatibility to keep up with the fastest available commercial logic. The ROM is the source of "firmware" machine-language instructions, which permit the system designer to mold or tailor the machine to his own needs and desires. State-of-the-art logic circuits allow instructions of this type to be executed at speeds under 100 nanoseconds. The ROM itself has an access time of under 40 nanoseconds. Speed, which is second only to reliability, was considered carefully in the design of the ROM and its associated logic.

1.1 COMPUTER SYSTEM ORGANIZATION

The META 4 Computer's microprogrammed organization offers the system designer an opportunity to match internal hardware facilities to a particular set of requirements. The META 4 hardware can be custom configured and the command structure of the processor can be easily altered completely to fit the hardware architecture and the specific application.

Organization of the META 4 System is independent of the machine language instruction set in main memory. The firmware permits flexibility in specifying operations for functional elements such as arithmetic and Boolean units, registers, memory, and input/output (I/O) devices.

In a nonmicroprogrammed computer, specially wired circuits control each sequence. The main memory instruction set is fixed and can be changed only by rewiring the computer. In the META 4 Computer, a high-speed control memory (the ROM) replaces the specially wired circuitry. Control memory instructions (the microprogram) specify operations of the functional elements.

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* Patent applied for.

1.2 READ-ONLY MEMORY (ROM) CAPABILITY

The high-speed computing capability is controlled by Digital Scientific Corporation's unique ROM. ROM-controlled instruction cycle times are less than 100 nanoseconds, which permits 9 or more microinstructions to be executed during each core memory cycle.

Speeds of the ROM in executing its instruction set are such that the META 4 Computer, at the micro level, can match or outperform third-generation hardware techniques.

The computer organization and the high-speed ROM allow applications, which would normally require special hardware designs, to be easily implemented in firmware with a META 4 Computer.

For example:

- Instruction Set Emulator for Other Computers (with improved performance)

  An IBM 1130/1800 can be emulated completely and can be improved upon by adding any instruction such as floating-point and register-to-register instructions.

- Channel Interface or Peripheral Equipment Controller for Other Computers

  A disc controller with code and format conversion capabilities can be microprogrammed to operate at high speeds to provide economical standard interfacing to a variety of other computers.

- Communications Line Controller, Buffer, Editor, and Preprocessor

  Serial-to-parallel conversion and data editing for multiple nonsynchronous lines can be done at high speed to relieve a data processing system of a substantial overhead load.

1.2.1 Multiple Operations

Any combination of the above can operate in a time-shared machine.

The ROM is loaded with firmware contents by sliding in pattern boards that have adhesive-bonded metallic "bit-patch" patterns organized in rows and columns representing bit positions in sequential instructions. A bit patch is binary "1" and the absence of a patch represents a binary "0."

2.0 ROM ORGANIZATION

Contents of the ROM can be readily modified or replaced in the field by either Digital Scientific Corporation or user personnel. The ROM is organized into 16-bit words. Instruction words must be located at even addresses. Logically indexed references to data words may use either even or odd addresses. Up to 4096 single words may be installed in multiples of 1024 words. Each reference to the ROM calls up a double word so that access time is identical for single words and double words.

Rom instructions are executed in sequence unless a Branch instruction causes transfer to another sequence. Branches occur in one of three ways: if specified during a register-to-register (RR) format instruction, the next instruction is unconditionally taken from the address in the Link register (Register 2); if, when tested, the counter section of the Condition/Counter register (Register 1) does not decrement to zero during an RR format instruction, the next instruction is taken from the address in the Link register; if the Branch instruction to test various data or machine conditions is successful, the next instruction is taken from the data field of the instruction and logical indexing by the Link register is selectable.

A four-bit field in the Branch instruction "points" at any single bit of any addressable register. Branching may be selected for the true or false state of the specified bit, allowing tests for data sign, arithmetic carry/overflow, shift carry, or any other single bit condition. Branching on zero or nonzero half words or single words is selected by a modified Branch instruction.

The system is initialized by an externally applied signal which clears the I/O register controls and the ROM Address register. Execution of the instruction at ROM address 000_{16} (normally a Branch) can lead to a firmware routine that initializes other parts of the system such as internal working registers.

3.0 ROM ADDRESSING

ROM addressing uses two different decoders (see Figure 1):

- The Counter Address Decoder ("normal" decoder) decodes the address stored in the program counter register, which does bookkeeping for normal sequential memory references by incrementing or "counting" each time an instruction is fetched from memory.

- A Branch or Jump Address Decoder decodes the Jump address when an instruction fetches an instruction word from other than the next sequential address.

The Jump address normally replaces the contents in the Program Counter register. The use of two decoders speeds up the address. This permits the address to be settled and ready for possible use when the tests and decisions are finally made to jump or not to jump. The Branch instruction word contains the new address.

The ROM address is an 11-bit word divided as illustrated in Figure 2.

Address bits 20 and 21 are used to gate data from the desired ROM module onto the ROM address data bus. Read-only memories fetch the word at the location specified by the word/board-select data contained in the address word. Since the ROM holds 1024 16-bit words, certain applications requiring more instructions will need multi-ROM configurations consisting of specialized program or emulation instructions. Data from each ROM is OR'ed onto the ROM data bus and into the ROM data register. Thus, undesired data from other multi-ROM's (if any) must be inhibited.

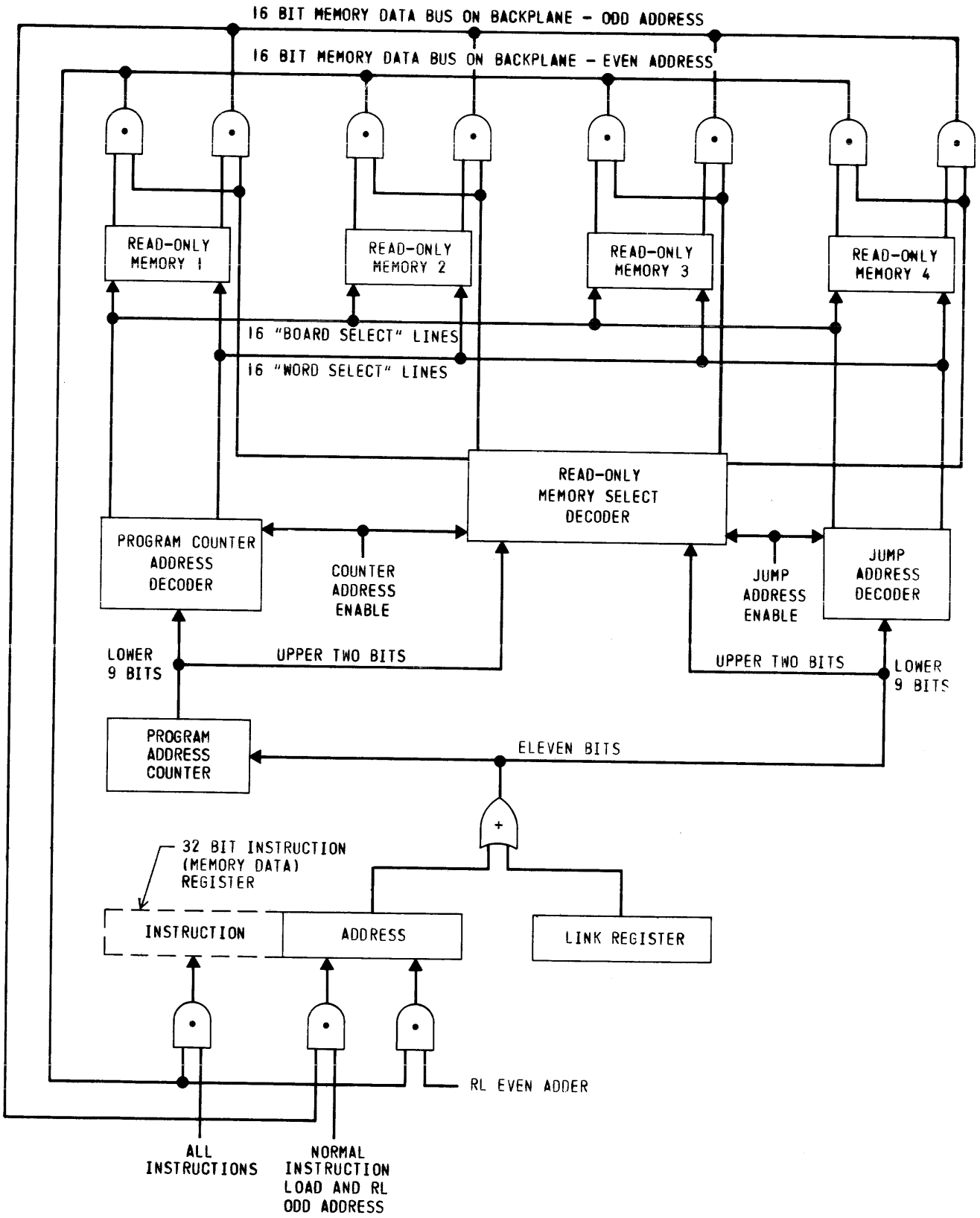

FIGURE 1. READ-ONLY MEMORY (ROM) ADDRESSING, BLOCK DIAGRAM

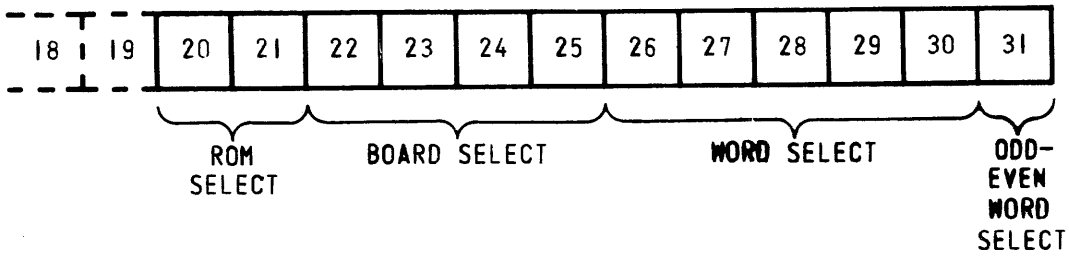

FIGURE 2. ROM ADDRESS WORD

4.0 ROM PHYSICAL DESCRIPTION

Each ROM is made up of a stack of 16 boards as illustrated below in Figure 3. Each board has 32 word-select circuits that provide the excitation to read one of the 32 words stored on the board. A typical board pattern is shown in Figure 4. The word-select circuits are chosen by the 5-bit word-select portion (Figure 2) of either the counter address or the jump address decoder outputs which are OR'ed into the word and board-select input gates. The particular board (of the stack of 16) to be referred to is selected by the 4-bit board-select portion (Figure 2) of the address word.

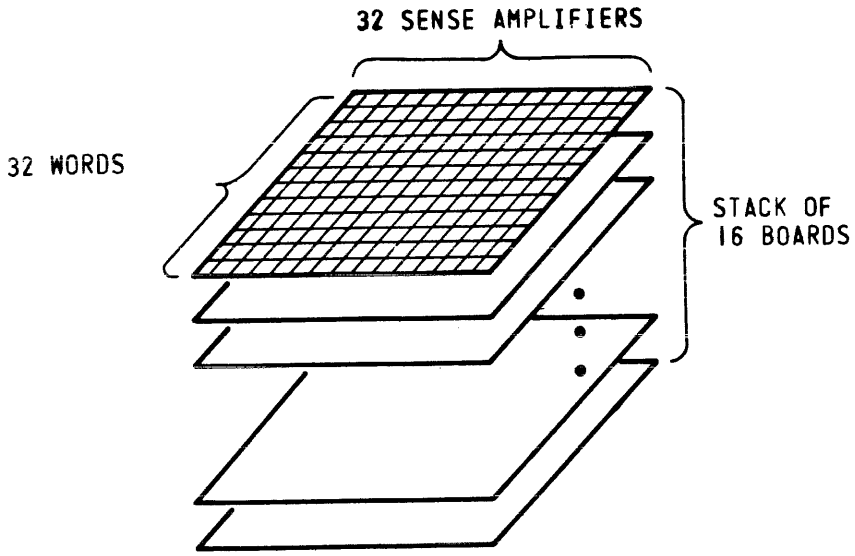

FIGURE 3. ROM STACK

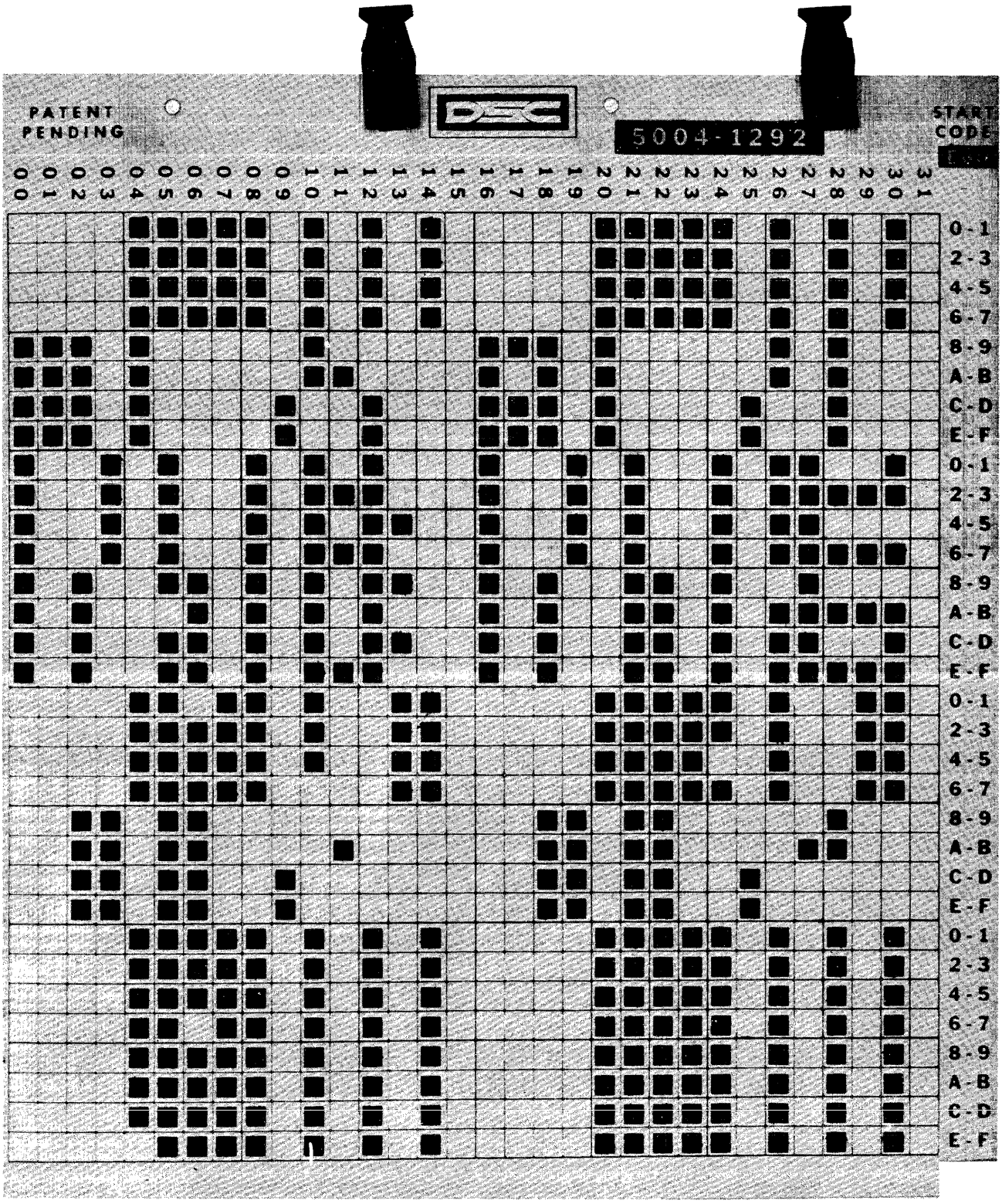

FIGURE 4. DIGITAL SCIENTIFIC META 4 COMPUTER SYSTEM
ROM BOARD, TYPICAL PATTERN

Data from each of the respective bit positions of the 512 words stored in a ROM is sensed by amplifiers and gated to the ROM data (instruction) register. If a Register Load instruction causes the memory reference, the upper 16 bits (bits 0 through 15) of the returning data word are duplicated in the lower 16 bits (bits 16 through 31) of the same word for subsequent use as an operand on the A-bus.

4.1 ROM PHYSICAL CONSIDERATIONS

The ROM boards and their stacking are a precision assembly. Particular care must be exercised in the use of the ROM. Board configuration has been designed to give precision indexing. The ROM program boards must be seated so that the indexing notches are tight against the stacking posts (see Figure 5).

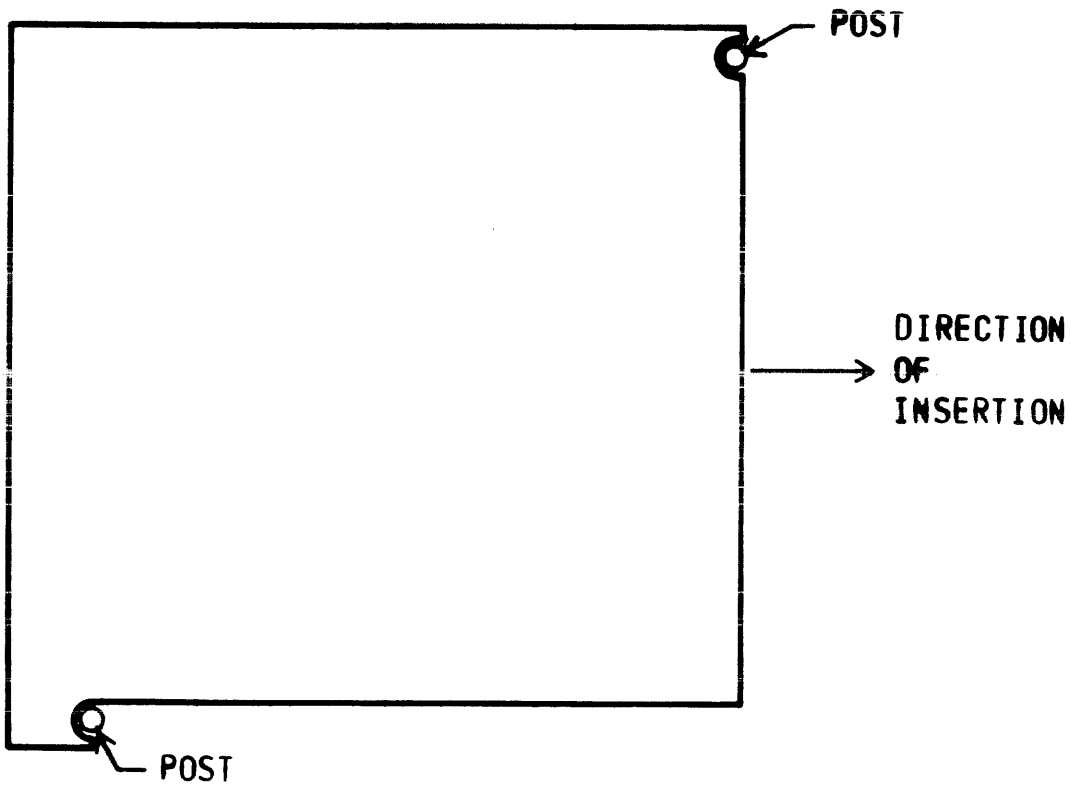

FIGURE 5. ROM INDEXING

Program boards must be flush against respective selection boards (Figure 6 illustrates the assembly procedure).

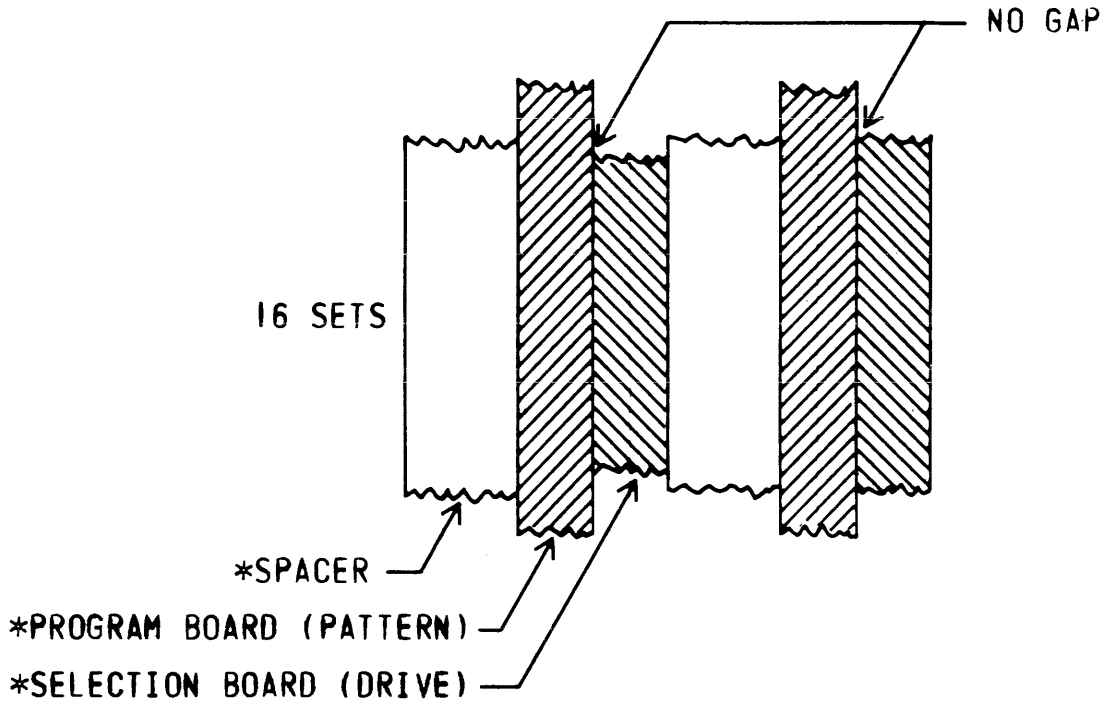

FIGURE 6. ROM STACKING ASSEMBLY, FRONT VIEW

4.1.1 ROM Removal and Replacement Procedures

- Remove ROM from socket.
- Loosen four screws.
- Remove pattern board.
- Reverse this simple procedure to replace ROM.

Figure 7 illustrates the removal and replacement procedure for the ROM. A simple tool has been designed for ease of board removal and insertion.

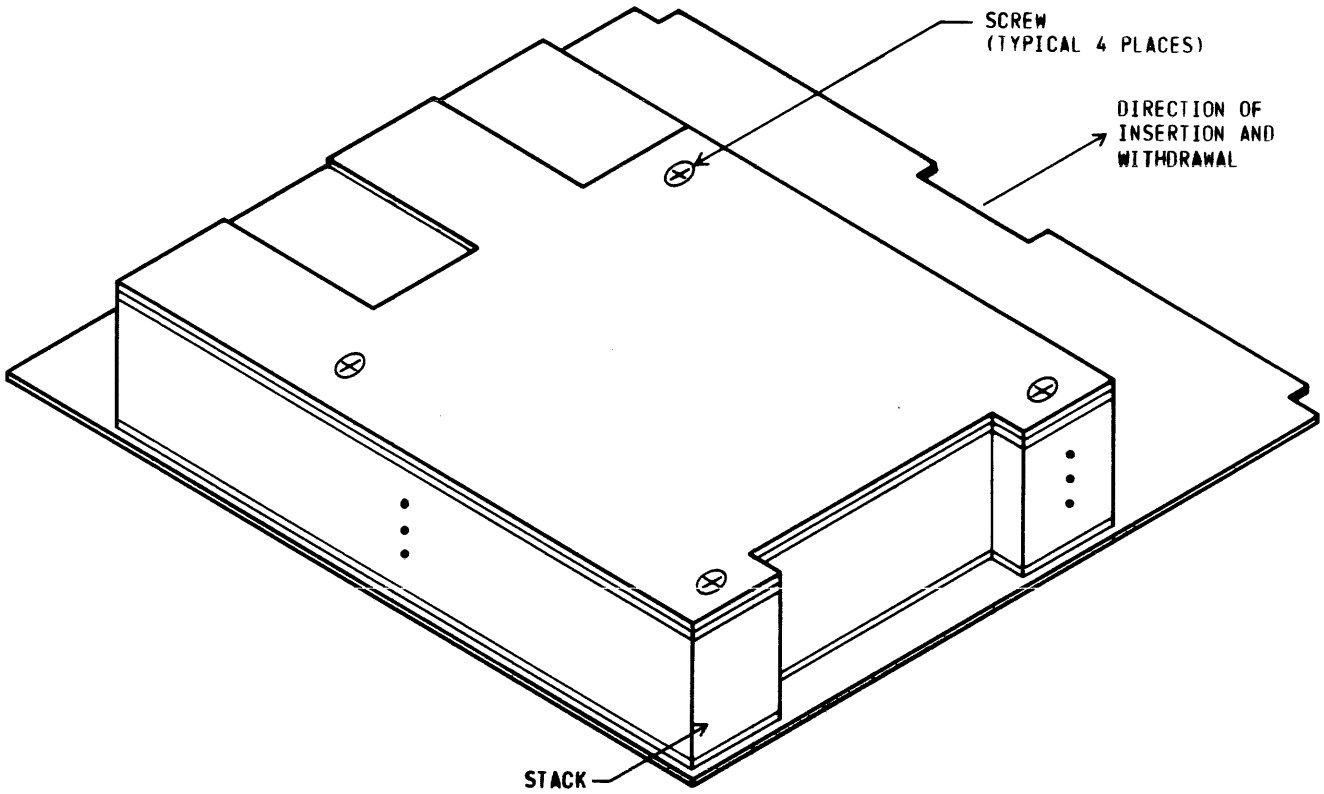

FIGURE 7. ROM ASSEMBLY, REMOVAL AND REPLACEMENT

4.1.2 Securing the ROM Stack

CAUTION

Tighten the ROM stack very carefully and deliberately to prevent damage to the stack and/or to individual boards in the stack.

When securing the ROM stack, make sure that no gaps show between boards, but do not overtighten. Overtightening can cause distortion, which can degrade performance.

4.1.3 Positioning the Bit Patches

Bit patches must be positioned accurately. The program boards have a precision grid, as shown in Figure 8.

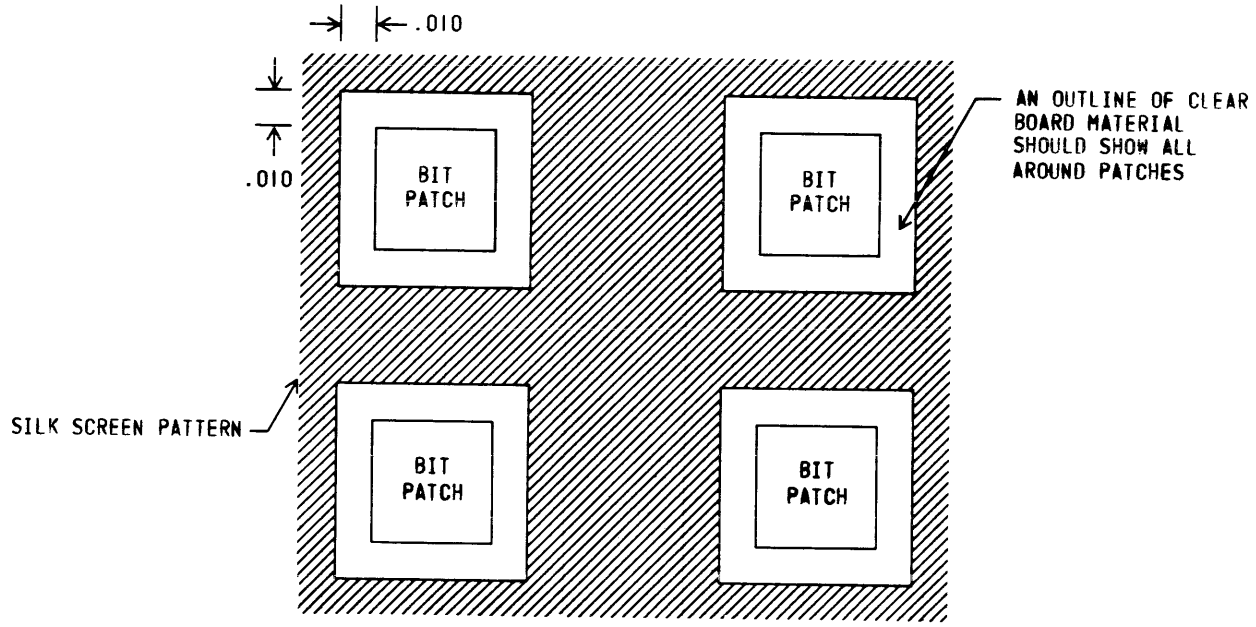

FIGURE 8. ROM SILK-SCREEN PATTERN

4.2 NEW PROGRAM BOARDS

To add new programs to a ROM stack, remove patches from a full board. The bit patches can be easily removed to form the desired pattern by use of a sharp-edged X-acto knife, or equivalent.

To replace patches, proceed as follows:

- Keep surface of board clean; the bit patches are backed with pressure sensitive adhesive requiring a clean surface for a good bond.

- Slide the X-acto knife, or equivalent, under a corner of the patch. The adhesive backing will secure the patch to the knife until relocation.

CAUTION

Bit patch replacement requires care and proper positioning. If a patch has been inadvertently removed, it can be replaced or repositioned. However, make sure that it is undamaged; i.e., that no holes or scars from the removal procedure mar its surface.

- When the patch is in position, press it lightly to prevent shifting and slide the knife blade out from the corner very carefully.

- Press the patch firmly in place.

- Check for good bond by looking at patches through back of board. Good bond is dark; bad bond is light.

5.0 DOCUMENTATION

The Digital Scientific META 4 Computer System ROM instructions, modifiers, programming techniques and examples are described in Sections 2 and 4 of DSC Publication No. 7006MO (Rev. D), META 4 Series 16 Computer System Manual.

Refer also to DSC Publication No. M4/005-170, META 4 Computer System Typical ROM Pattern Listing and Program to Simulate the IBM 1130 Instruction Set.

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COMMENT SHEET

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