A STUDY OF THE TRANSIENT BEHAVIOR OF A HIGH SPEED TUNNEL-DIODE SWITCHING CIRCUIT USING AN ANALOG COMPUTER

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I. ANALYSIS OF SWITCHING CIRCUIT

The switching circuit is best understood by reference to the simplified schematic drawing in Figure 1. The voltages V_+ and V_- are bias voltages provided by an external source, and are assumed to be equal in magnitude and opposite in polarity. The tunnel diodes TD_1 and TD_2 are identical. If no inputs or loads are connected to the circuit, the same current will flow through both diodes. If the volt-ampere curve of the diodes always exhibits a positive resistance characteristic, the voltage drops across the diodes will be identical, and the voltage at the juncture of the diodes will be zero.

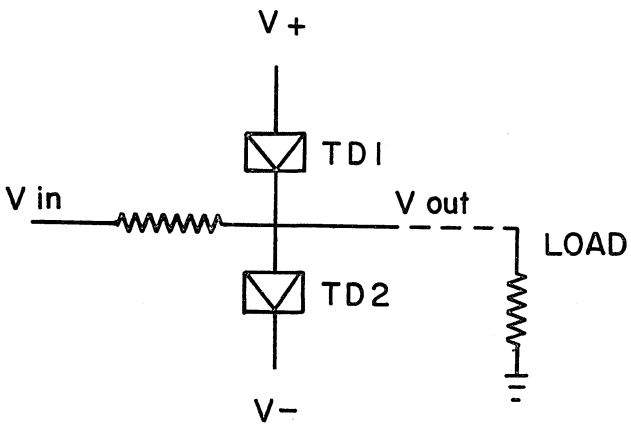

Figure 1. Simplified Schematic for Tunnel-Diode Switching Circuit

The characteristic curve of a typical tunnel diode is given in Figure 2. Note that the slope is negative over the greater portion of the operating range (from about 60 to 300 millivolts). The existence of this negative resistance region means that the equilibrium described in the preceding paragraph will be unstable. A very slight disturbance will upset the summetry described above, causing a very much larger voltage to appear across one diode than across the other. This sensitivity to small input disturbances enables the circuit to function as a high-gain high-speed switch.

Assume V_+ and V_- are initially zero and that V_+ gradually increases while V_- decreases, such that $V_+ + V_- = 0$. Then the operating point of each diode will move from the origin in Figure 2 along the characteristic curve toward the peak. The voltage at the junction will remain zero, as before. After the peak has been passed, the voltages and currents for the two diodes should remain identical (by symmetry), and the voltage at the junction should remain zero. However, since the diodes are now in their negative resistance region, this equilibrium will prove extremely unstable.

Suppose, for instance, that the circuit is unbalanced by a small positive voltage at the input terminal. Then tunnel diode #2 will have a slightly greater voltage across it than tunnel diode #1, and as the bias voltage increases, tunnel diode #2 will pass its peak first. Further increases in the voltage across TD2 will result in a decrease in the current through it, and hence a decrease in the current through TD1 as well. Since TD1 is still in its positive resistance region, a decrease in its current will decrease its voltage drop, increasing the voltage drop across TD2 (since the tunnel diodes are acting as a voltage divider, and the sum of their voltage drops must equal $2V_+$). It follows that TD2 will move rapidly through its negative resistance region, at a speed limited only by circuit reactances, and stabilize somewhere in the positive resistance region above 300 millivolts, while TD1 stabilizes in the positive resistance region below 60 millivolts.

Since most of the voltage drop between the two bias sources appears across TD2, it follows that the voltage at the junction (the output voltage) will be positive. A positive input voltage will therefore produce a positive output voltage. The output voltage will be of the same order of magnitude as the bias voltage V_+, while the input voltage need only be large enough to overcome any inherent imbalance in the diode characteristics. The input voltage can thus be made very small, and the gain of the circuit is limited only by the closeness of the match between diode characteristics and between

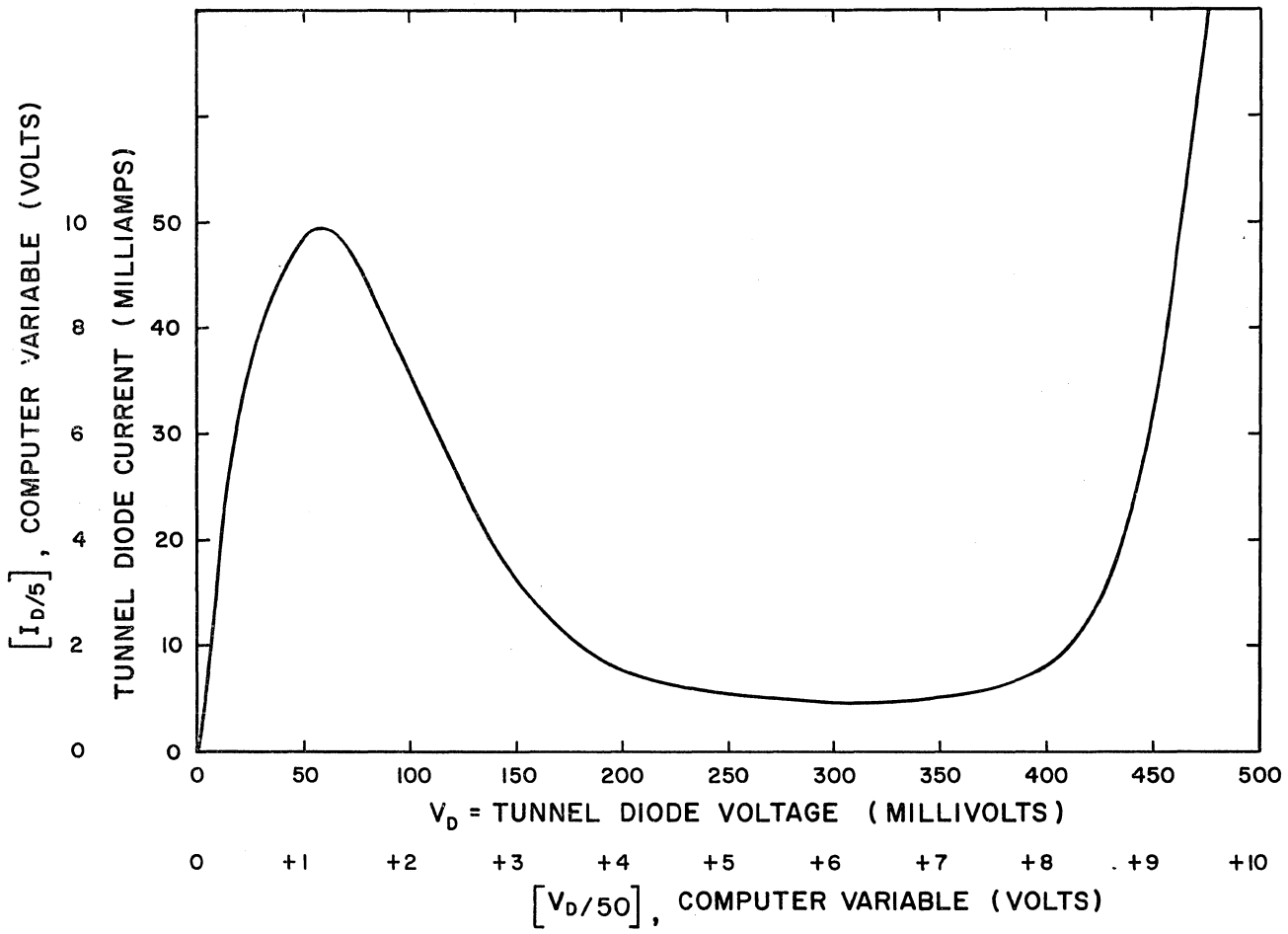

Figure 2. Tunnel-Diode Characteristic Curve

the positive and negative power supplies. If the input and output voltages are equal in magnitude, as is the case with cascaded logic elements of similar design, high gain means that very large resistors can be used, resulting in very large fan-in and fan-out figures.

In high-speed logic and arithmetic circuits, the voltages V_+ and V_- will be out-of-phase alternating voltages with approximately sinusoidal waveshapes. D-C levels will be superimposed on these sinusoids and, in most applications, this bias will just equal the amplitude of oscillation assuring that the bias voltages do not change sign. The alternating bias voltages will then serve as a "clock," supplying the necessary timing signals for high-speed arithmetic and logic. An output can be obtained only during that part of the bias cycle when the bias voltage is large enough to switch one of the diodes into its negative resistance region.

The attractiveness of this circuit for digital applications lies in the fact that the input need only be large enough to unbalance a symmetric circuit. If all components were perfectly matched, the slightest input disturbance would unbalance the circuit in the proper direction, and the theoretical gain would be infinite. In practice, the gain will be limited by component tolerances. An estimate of the gain (or, equivalently, the fan-in/fan-out capability) of the circuit can be made from a static analysis of the tunnel-diode characteristic and a knowledge of circuit tolerances. Such an analysis has been made by Chow (4) who predicted large gains for closely matched diodes.

The above analysis is essentially static. For design purposes, a dynamic analysis, which takes circuit reactances into account, is necessary for at least two reasons:

1. A knowledge of the switching time is necessary to determine the maximum clock frequency (i.e., the maximum rate of information transfer) at which the system can be operated.

2. Since the circuit contains two negative-resistance elements, it may well prove unstable. Instead of the switching behavior described above, the system may break into oscillations.

Both the stability and the switching time will depend primarily on the inevitable circuit reactances. Figure 3 shows the equivalent circuit for the system, with circuit reactances and external loading taken into account. The principal reactances involved are lead inductance and case inductance (which may be lumped together) and diode shunt capacitance. Provision is also included for coupling the leads together with mutual inductance, which would correspond to dressing the power supply leads close together during construction. A moderate amount of coupling proves to have a beneficial effect on switching time when the circuit is operated at high frequencies.

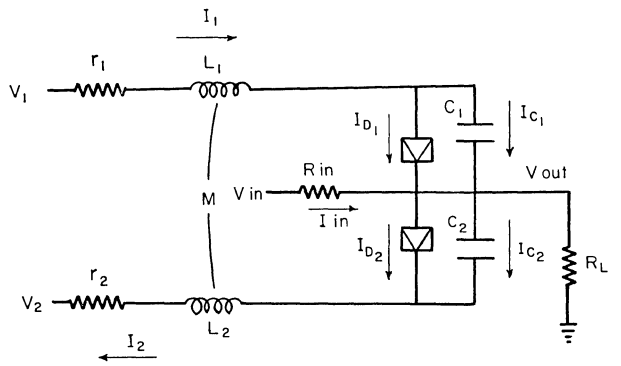

Figure 3. Equivalent Circuit Showing Reactances

Experimentation with the actual circuit is possible, but extremely difficult due to the high frequencies involved (the range of clock frequencies to be investigated is from 100 to 1000 mc.). The basic simplicity of the equivalent circuit makes it easy to write equations to describe the system and thus study the mathematical model (the equations) rather than the system itself.

II. THE MATHEMATICAL MODEL

The equations describing the system are given below. These equations are straightforward applications of Kirchoff's laws and the known properties of resistors, capacitors, and inductors. They may be written down immediately upon inspection of Figure 3.

$$V_1 = I_1 r_1 + L_1 \dot{I}_1 - M \dot{I}_2 + V_{D_1} + V_{out} \quad (1)$$

$$-V_2 = I_2 r_2 + L_2 \dot{I}_2 - M \dot{I}_1 + V_{D_2} - V_{out} \quad (2)$$

$$V_1 = -V_2 = E_{DC} - A \sin \omega t \quad (3)$$

$$\dot{V}_{D_1} = \frac{1}{C_1} I_{C_1} \quad (4)$$

$$\dot{V}_{D_2} = \frac{1}{C_2} I_{C_2} \quad (5)$$

$$I_{C_1} = I_1 - I_{D_1} \quad (6)$$

$$I_{C_2} = I_2 - I_{D_2} \quad (7)$$

$$I_{D_1} = f(V_{D_1}) \quad (8)$$

$$I_{D_2} = f(V_{D_2}) \quad (9)$$

$$V_{out} = (I_1 - I_2 + I_{in}) R_L \quad (10)$$

$$I_{in} = \frac{V_{in} - V_{out}}{R_{in}} \quad (11)$$

Equations 1 and 2 are Kirchoff voltage equations for the two major loops. Equation 3 is simply the statement that the bias or "clock" voltages are out-of-phase sinusoids with DC levels superimposed. Equations 4 and 5 state the basic volt-ampere relation of a capacitor, and 6 and 7 are Kirchoff current equations. Equations 8 and 9 state the characteristic relation between voltage and current in the tunnel diodes (see Figure 2). On the computer, these curves will be represented by function generators. Equations 10 and 11 are, of course, statements of Ohm's Law.

Equation 11 was omitted for the purposes of this simulation, and replaced by the assumption that the input current I_{in} was constant. Values from 0.5 up to 2.0 ma. were tried. The assumption of constant input current implies a constant-current source, which is not very realistic. This simplification is not necessary, and equation 11 could be programmed directly by adding one additional summer and one inverter to the analog circuit. The simplification was made in the present study so that the results could be compared directly with Herzog's digital solution (Ref. 2), since Herzog also made this assumption.

III. THE COMPUTER PROGRAM

A. Solving for the Derivatives $\dot{I}_1$ and $\dot{I}_2$

The first step in deriving a computer program is

to solve all differential equations for the highest derivatives. This has already been done in equations 4 and 5, but equations 1 and 2 contain the derivatives $\dot{I}_1$ and $\dot{I}_2$, and each derivative appears in both equations. To solve for $\dot{I}_1$ and $\dot{I}_2$, we must treat these as a simultaneous system of two equations in two unknowns. This system may be solved by determinants, but the resulting computer circuit would be unnecessarily complex. A far simpler approach is to solve equation 1 for $\dot{I}_1$ and equation 2 for $\dot{I}_2$, giving

$$\dot{I}_1 = \frac{1}{L_1}(V_1 - I_1 r_1 + M\dot{I}_2 - V_{D_1} - V_{out}) \qquad (1^*)$$

$$\dot{I}_2 = \frac{1}{L_2}(-V_2 - I_2 r_2 + M\dot{I}_1 - V_{D_2} + V_{out}) \qquad (2^*)$$

These equations give $\dot{I}_1$ in terms of $\dot{I}_2$ and vice versa. Programming them directly leads to an algebraic loop (a loop with no integrators), and since this is a two-amplifier loop, positive feedback is present. For stability, we must have a loop gain of less than one (Ref 5). By inspection of the circuit, it is easily seen that the loop gain is M^2/L_1L_2. Since this is always less than one on physical grounds, the loop is stable and the correct values of $\dot{I}_1$ and $\dot{I}_2$ may be obtained without determinants (Reference 6).

B. Generating the Characteristic Curve

The tunnel-diode characteristic in Figure 2 presents a problem in function generation no matter which simulation method is used. On a digital computer, the function values can be stored in main memory in tabular form, perhaps with an interpolation subroutine to fill in the gaps between tabulated values. If enough values and/or a sufficiently sophisticated interpolation scheme are stored, a tremendous demand is made upon the memory. If the digital computer is not called upon to solve the dynamic equations as well, this is an acceptable technique. This was the approach used by Axelrod (3). The simulation was essentially analog, with the digital computer serving only as a function generator.

Herzog (2) uses a digital computer for the entire problem. The characteristic curve is represented by an analytic expression of four terms involving a polynomial, two exponential functions and a fractional power. This expression, which was obtained from a separate digital computer run by curve-fitting, can be programmed with standard subroutines.

On an analog computer, the best approach is straightforward use of a standard function generator. The diode function generator (DFG) uses biased diode networks to approximate a curve by straight-line segments. On the TR-48 variable-breakpoint DFG, eleven segments are available. The breakpoints (corners) of the curve may be varied so as to group many short straight-line segments together where the graph curves most sharply and use fewer segments where the graph is straighter. In this way, an over-all accuracy of about 1% is maintained for this particular curve.

TABLE 1
SETUP TABLE FOR VARIABLE DFG

INPUT (VOLTS)	OUTPUT (VOLTS)
0.00	0.00
0.35	5.81
0.85	9.34
1.10	9.93
1.45	9.36
2.85	3.67
3.85	1.69
6.20	0.89
7.90	1.56
8.55	3.20
9.00	6.75
9.50	12.00

Table 1 gives the appropriate breakpoints and the corresponding function values. Note that one of the DFG's must accept the input $-V_{D1}/50$ and produce the output $+I_{D1}/5$. Its input-output graph will look like Figure 2 reflected around the vertical axis. The appropriate table is obtained from Table 1 by making all the input voltages negative. The second DFG accepts positive inputs and produces negative outputs; its graph looks like Figure 2 reflected around the horizontal axis.

The volt-ampere curve in Figure 2 requires very sharp changes of slope. Since these sharp slopes exceed the capabilities of the DFG, a potentiometer must be placed in the feedback path of the output amplifier to increase the gain of the DFG.

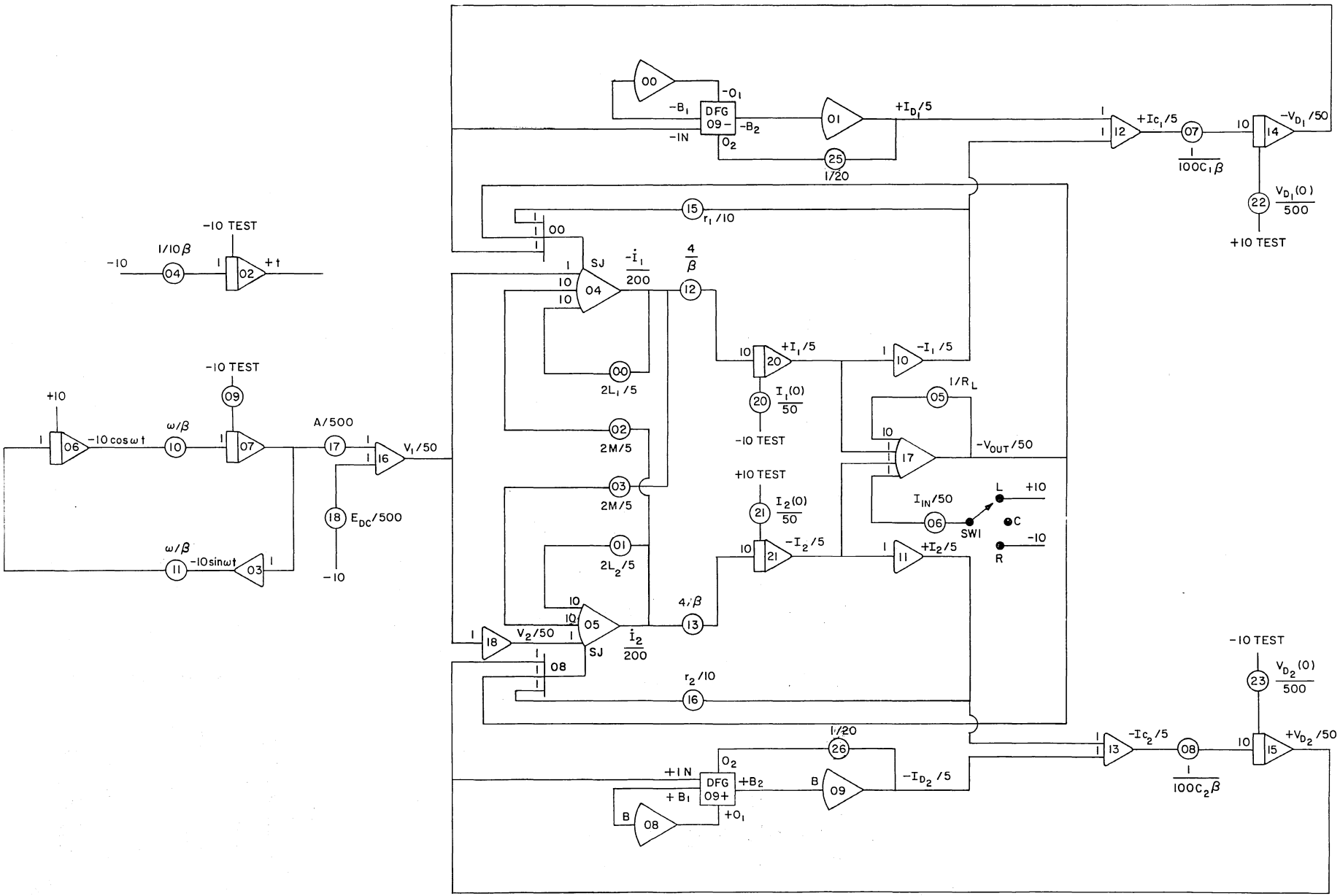

Figure 4. Analog Computer Circuit Diagram

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TR-48 POTENTIOMETER ASSIGNMENT SHEET

P00—P29

DATE 6/1/63 PROBLEM TUNNEL DIODE

POT NO	PARAMETER DESCRIPTION	SETTING STATIC CHECK	STATIC CHECK OUTPUT VOLTAGE	SETTING RUN NUMBER 1	NOTES	POT NO
00	$2L_1/5$	.160	+0.166			00
01	$2L_2/5$	.160	-0.134			01
02	$2M/5$	0.000	0.00			02
03	$2M/5$	0.000	0.00			03
04	$1/10\beta$	.020	-0.20			04
05	$1/R_L$	.125	-0.02			05
06	$I_{IN}/50$	.020	+0.20			06
07	$1/100C_1\beta$	.200	-0.97			07
08	$1/100C_2\beta$	.200	+0.97			08
09	I.C. A07	.640	-6.40		ARTIFICIAL I.C. TEST ONLY	09
10	ω/β	.188	-1.88			10
11	ω/β	.188	-1.20			11
12	$4/\beta$	.800	+0.83			12
13	$4/\beta$	.800	-0.67			13
14						14
15	$r_1/10$	.300	-1.50			15
16	$r_2/10$	.300	+1.50			16
17	$A/500$	.250	+1.60	.260		17
18	$E_{DC}/500$	.260	-2.60			18
19						19
20	$1/50\ I_1(0)$	.500	-5.00			20
21	$1/50\ \lvert I_2(0)\rvert$	.500	+5.00			21
22	$1/500\ V_{D_1}(0)$	.100	+1.00			22
23	$1/500\ \lvert V_{D_2}(0)\rvert$	.100	-1.00			23
24						24
25	$1/20$	.050	+0.49			25
26	$1/20$	.050	-0.49			26
27						27
28						28
~~29~~	SWITCH #1	LEFT				29

M654

Figure 5. Potentiometer Assignment Sheet

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TR -48 AMPLIFIER ASSIGNMENT SHEET

DATE 6/1/63 A00 – A23 PROBLEM TUNNEL DIODE

AMP NO.	FB	OUTPUT VARIABLE	STATIC CHECK				NOTES
			CALCULATED		MEASURED		
			CHECK PT.	OUTPUT	CHECK PT.	OUTPUT	
00		PART OF DFG					USE INPUT RESISTORS WITH 04
01	H	$+I_{D_1}/5$		+9.84			
02	∫	$+t$	+0.20	+10.00			
03	–	$-10 \sin \omega t$		-6.40			
04	H	$-\dot{I}_1/200$		+1.0375			
05	H	$+\dot{I}_2/200$		-0.8375			
06	∫	$-10 \cos \omega t$	+1.20	-10.00			
07	∫	$+10 \sin \omega t$	+1.88	+6.40			
08		PART OF DFG					USE INPUT RESISTORS WITH 05
09	H	$-I_{D_2}/5$		-9.84			
10	–	$-I_1/5$		-5.00			
11	–	$+I_2/5$		+5.00			
12	Σ	$+I_{C_1}/5$		-4.84			
13	Σ	$-I_{C_2}/5$		+4.84			
14	∫	$-V_{D_1}/50$	+9.68	-1.00			
15	∫	$+V_{D_2}/50$	-9.68	+1.00			
16	Σ	$\frac{V_1}{50} = \frac{-V_2}{50}$		+1.00			
17	H	$-V_{OUT}/50$		-0.16			
18	–	$V_2/50$		-1.00			
19							
20	∫	$+I_1/5$	-8.30	+5.00			
21	∫	$-I_2/5$	+6.70	-5.00			
22							
23							

M653

Figure 6. Amplifier Assignment Sheet

TABLE 2
SUMMARY OF VARIABLES

Original Variable	Max Value	Scale factor	Scaled Variable
V_{D_1}, V_{D_2}, V_1, V_2	500 mv	$\frac{1}{50}$ Volt/mv	$\left[\frac{1}{50} V\right]$
I_{D_1}, I_{D_2}	50 ma	$\frac{1}{5}$ Volt/ma	$\left[\frac{1}{5} I_D\right]$
I_1, I_2	50 ma	$\frac{1}{5}$ Volt/ma	$\left[\frac{1}{5} I\right]$
$\dot{I}_1$, $\dot{I}_2$	2000 ma/ns	$\frac{1}{200}$ Volt/ma/ns	$\left[\frac{1}{200} \dot{I}\right]$
I_{C_1}, I_{C_2}	50 ma	$\frac{1}{5}$ Volt/ma	$\left[\frac{1}{5} I_C\right]$

$$\beta = \frac{\text{5 seconds machine time}}{\text{1 nanosecond problem time}}$$

TABLE 3. SUMMARY OF UNITS OF MEASUREMENT USED

Voltage: millivolts
Current: milliamps
Resistance: ohms
Inductance: nanohenries (10^{-9} henry)
Capacitance: nanofarads (10^{-9} farad)
Time: nanoseconds (10^{-9} sec)

Note: The use of the somewhat unusual units for inductance and capacitance guarantees that the equations $I = C\dot{V}$ and $V = L\dot{I}$ will hold in this system of units.

G. Summary of Static Check Conditions

For static check calculations, convenient values are selected for all integrator output signals (in this case I_1, I_2, V_{D1}, and V_{D2}) and for the driving functions, V_1, V_2, and I_{in}. These values may be chosen arbitrarily, but they should be small enough to avoid amplifier overloads and large enough to provide amplifier output signals that can be measured with reasonable accuracy. The values chosen were:

$I_1 = +25$ ma. $\quad V_{D_1} = +50$ mv.

$I_2 = +25$ ma. $\quad V_{D2} = +50$ mv.

TABLE 4
SUMMARY OF PARAMETERS

$r_1 = r_2 = 3$ ohms

$R_L = 8$ ohms

$C_1 = C_2 = 10^{-2}$ nanofarads

$L_1 = L_2 = 0.4$ nanohenry

$M = \leq\sqrt{L_1 L_2}$ Try M = 0 for first run. Probable maximum value around 0.2 nanohenry.

$I_{in} = 1.0$ ma.

A = 130 millivolts

Edc = 130 millivolts

f = 150 megacycles/second = 0.15 cycles/nanosecond

$\omega = 2\pi f = 0.9425$ radians/n.s.

$V_1 = +50$ mv. $V_2 = -V_1 = -50$ mv.

$I_{in} = +1.0$ ma.

Parameter values are the same as those for the first run. The values for all variables may be calculated from equations 1 - 10. These values are given below.

$I_{D_1} = +49.2$ ma. $I_{D_2} = +49.2$ ma.

$I_{C_1} = -24.2$ ma. $I_{C_2} = -24.2$ ma.

$V_{out} = +8$ mv.

The derivatives may be calculated from equations 1*, 2*, 4, and 5. These are:

$\dot{V}_{D_1} = \dot{V}_{D_2} = -2420$ millivolts/nanosecond

$\dot{I}_1 = -207.50$ milliamps/nanosecond

$\dot{I}_2 = -167.50$ milliamps/nanosecond.

All variables that have been calculated can now be translated into amplifier output voltages. These voltages appear on the amplifier assignment sheet. They may be checked against values calculated on the circuit diagram (to check the programming and scaling) and later checked against actual measured voltages on the computer (to check the patching and the functioning of the components). The checkpoints should also be calculated and measured for integrators. (The checkpoint of an integrator is minus the sum of its input voltages. It may be read out by patching the summing junction of the integrator temporarily to the summing junction of a summing amplifier that is not being used in the problem). These calculated values are also tabulated in the amplifier assignment sheet.

The initial condition voltages marked "Test" are for static test purposes only, and not for the actual run. They should be removed prior to the first run.

Note that the static test value of the mutual inductance M is zero. This value was chosen to break the algebraic loop in the static test mode, since otherwise it would be very hard to troubleshoot. However, this static test value does not check the algebraic loop itself, and a supplementary test should be included with $M \neq 0$. For this supplementary test, we may as well assume that the artificial initial conditions on voltages and currents are zero, since this part of the circuit has already been checked by the main static check. Equations 1 and 2 then become:

$$V_1 = L_1\dot{I}_1 - M\dot{I}_2$$

$$-V_2 = L_2\dot{I}_2 - M\dot{I}_1$$

Solving by determinants:

$$\dot{I}_1 = \frac{V_1 L_2 - M V_2}{L_1 L_2 - M^2} \quad ; \quad \dot{I}_2 = \frac{-L_1 V_2 + M V_1}{L_1 L_2 - M^2}$$

If we let $V_1 = 50$ mv, $V_2 = -50$ mv, $L_1 = L_2 = 0.4$ nanohenry and $M = 0.2$ nanohenry, then $\dot{I}_1 = \dot{I}_2 = +250.0$ milliamps/nanosecond.

The output of amplifier 04 should be $-\dot{I}_1/200 = -1.25$ volts, and the output of amplifier 05 should be $+1.25$ volts.

IV. RESULTS AND CONCLUSIONS

The switching transients and output waveshapes for constant input current are shown in Figures 7 and 8. Note in particular that at 300 megacycles the output voltage goes through an initial oscillation before switching. The output is high for only a short period of time late in the bias cycle. At 150 megacycles, the output rises much more sharply and gives a good waveshape.

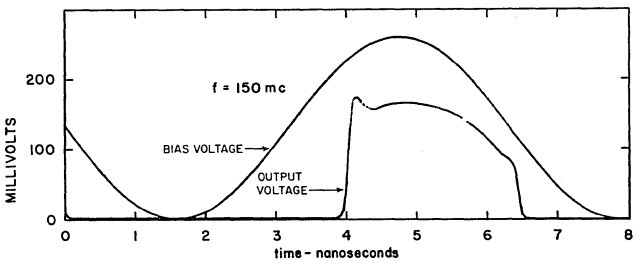

Figure 7. Output Waveshape of Switching Circuit at 150 Megacycle Clock Frequency

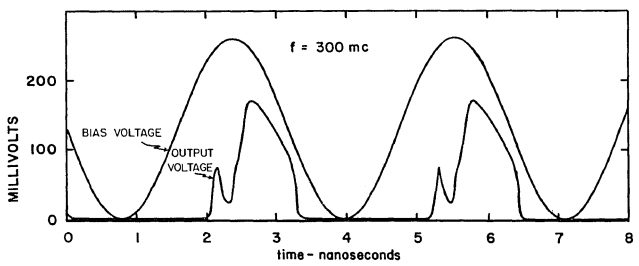

Figure 8. Output Waveshape at 300 Megacycle Clock Frequency

Operation at 300 megacycles is possible, but marginal. Further experimentation with the model indicates that for reliable operation with sufficiently large fan in/fan out capability the circuit should not be operated above about 200 or 250 megacycles.

It is significant that a preliminary pencil-and-paper analysis indicated that the system ought to operate at frequencies up to 1000 megacycles. A circuit designed to operate at this frequency would not function properly and would be extremely hard to troubleshoot, due to the circuit loading of the measuring devices. The computer solution facilitates fundamental understanding of the nature of the switching process, as well as providing actual solutions. The ease of parameter changing on the analog computer makes it especially easy to investigate the trade-off between gain (i.e. fan in/fan out capability) and frequency.

The results agree quite well with Herzog's digital simulation, using the Edsac II computer at Cambridge University, and for further analysis of the results, the reader is referred to Herzog's paper (2). It is instructive to compare the two simulations from the point of view of flexibility and convenience.

a. The digital program requires the equations to be written as a set of first-order equations, solved for the highest derivatives, and then converted into algebraic equations by the Runge-Kutta or a similar integration scheme. While standard software is available in many installations to simplify this task, it is completely eliminated in an analog simulation, since the analog solves differential equations as differential equations.

b. The running time for the Edsac II was, according to Herzog, about three minutes per solution, as opposed to 25 seconds on the TR-48 computer -- a speed advantage of seven to one. Nothing precludes running even faster than this, since the components are operating well within their frequency-response limitations. The solution also can be run in repetitive operation, in which case the solution takes only 50 milliseconds -- effectively zero solution time as far as the operator is concerned.

c. Even more important than running time per se is the time required to obtain meaningful and useful results. The output of the analog unit is a continuous graph, drawn in ink on 11 x 17" paper. . . a form of output which an engineer can readily observe and interpret. By contrast, the digital results were obtained from an on-line printer, and considerable manual effort was required to translate these results into graphical form.

Of course, on-line devices are available for producing graphical readout from a digital computer. Some of Herzog's graphical results were obtained by oscilloscope photography. Although this method eliminates the tedium of point-plotting, it is messy and time-consuming, and offers limited resolution. Perhaps the best form of readout (certainly the most convenient) involves the use of a digital-to-analog converter and an analog X-Y plotter. While this method is acceptable, it requires expensive conversion equipment to translate the data into analog voltages for plotting. Such conversion equipment is unnecessary with the TR-48 computer since the signal is an analog voltage in the first place.

d. Since only about half of the computing capacity of the TR-48 computer is used, the simulation can easily be expanded to take additional effects into account. Herzog's equations assumed a constant current input and ignored the fact that the load is not purely resistive. These simplifications could easily be removed on an analog simulation by addition of a few more amplifiers and potentiometers. On a digital computer, any additional complexity in the equations would increase the running time.

An attractive alternative, for example, would be to simulate an additional tunnel-diode circuit on the analog computer and feed the output of the first into the second. This would enable the designer to determine how flat the output waveshape of the first circuit would have to be in order to trigger the second successfully.

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