# CS02/H1

# COMMUNICATIONS SUBSYSTEM

# TECHNICAL MANUAL

# (DH11/DM11 OR DHV11 COMPATIBLE)


3545 Harbor Boulevard
Costa Mesa, California 92626
(714) 662-5600  TWX 910-595-2521

CS0251001-00 Rev K
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**WARNING**

This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Commission (FCC) Rules, which are designed to provide reasonable protection against such interference when operating in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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## EMULEX PRODUCT WARRANTY

CONTROLLER WARRANTY: Emulex warrants for a period of twelve (12) months from the date of shipment that each Emulex controller product supplied shall be free from defects in material and workmanship.

CABLE WARRANTY: All Emulex provided cables are warranted for ninety (90) days from the time of shipment.

The above warranties shall not apply to expendable components such as fuses, bulbs, and the like, nor to connectors, adaptors, and other items not a part of the basic product. Emulex shall have no obligation to make repairs or to cause replacement required through normal wear and tear or necessitated in whole or in part by catastrophe, fault or negligence of the user, improper or unauthorized use of the product, or use of the product is such a manner for which it was not designed, or by causes external to the product, such as but not limited to, power failure or air conditioning. Emulex's sole obligation hereunder shall be to repair or replace any defective product, and, unless otherwise stated, pay return transportation cost for such replacement. Purchaser shall provide labor for removal of the defective product, shipping charges for return to Emulex and installation of its replacement.

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# SECTION 1
# GENERAL DESCRIPTION

## 1.1 INTRODUCTION

This manual is designed to help you install and use your CS02/H Communications Subsystem, manufactured by Emulex Corporation, in the most efficient and straightforward manner possible. The manual's eight sections and five appendices are described briefly below.

Section 1 General Description: This section contains an overview of the CS02/H Communications Subsystem.

Section 2 Subsystem Specification: This section contains a specification for each component of the subsystem.

Section 3 Application and Configuration: This section contains the information necessary to plan your installation.

Section 4 Installation: This section contains the information needed to set-up and physically install the subsystem.

Section 5 Operator Switches and Indicators: This section describes the function of the subsystem switches and indicators.

Section 6 Troubleshooting: This section describes fault isolation procedures that can be used to pinpoint trouble spots.

Section 7 Controller Registers and Programming: This section contains a description of the subsystem's DH11-, DM11- and DHV11-type registers. This section also provides programming notes and describes the controller architecture.

Section 8 Interfaces: This section describes the subsystem Q-Bus and serial interfaces.

Appendix A Cable Schematics: This appendix contains schematics of the EIA cables required to attach terminals, printers, modems and wrap-around connectors to ports of the CS02/H.

Appendix B DH11 Diagnostic: This appendix contains operating instructions and patches for the DH11 diagnostic, ZDHMD0.

Appendix C DHV11 Diagnostics: This appendix contains operating instructions for the DHV11 diagnostics.

Appendix D Code Conversion Table: This appendix provides an ASCII and decimal/hexadecimal/octal table.

Appendix E PROM Removal and Replacement: This appendix contains PROM removal/replacement instructions to allow the user to change the CC02 Controller Module's PROMs in the field. A list of firmware PROM numbers and their locations on the PCBA is also provided here.

### 1.1.1 RELATED DOCUMENTATION

This manual is the main piece of documentation for the CS02/H1 subsystem. Two other manuals come with the subsystem: a distribution panel technical manual and a diagnostic manual (if diagnostics were ordered). These other manuals are used only during specific parts of the installation procedure and this manual will clearly reference the other manuals any time you need them.

## 1.2 SUBSYSTEM OVERVIEW

This manual explains the use and installation of the CS02/H Communications Subsystem. The CS02/H Communications Subsystem emulates one Digital Equipment Corporation (DEC) 16-channel DH11 Asynchronous Communications Multiplexer, including partial DM11 modem control for all channels, or it emulates two DEC eight-channel DHV11 Asynchronous Multiplexers. The CS02/H Communications Subsystem is designed for use with DEC Q-Bus based processors.

The CS02/H Communications Subsystem consists of a controller module and istribution panel. The controller module takes multiplexed data from the host central processing unit (CPU), demultiplexes the data, and sends it to the ports on the distribution panel(s). Conversely, data from the distribution panel(s) is multiplexed by the controller module, and sent to the host CPU. The controller module also serializes and deserializes data.

The distribution panels hold the connectors that allow external devices such as terminals, printers and modems to be connected to the subsystem.

The CS02/H incorporates several advanced features for communications multiplexers. These features include direct memory access (DMA) on transmit, programed input/output (I/O) on reception, a 256-character receive silo with programmable fill alarm, individually programmable channel parameters, and data rates of up to 38,400 bits per second (bps). These features and the CS02/H's bus register structure are fully compatible with DEC's DH11 communications multiplexer with DM11 modem control, and with DEC's DHV11 asynchronous multiplexer.

## 1.3 PHYSICAL ORGANIZATION OVERVIEW

The CS02/H Communications Subsystem is a modular, microprocessor-based controller that connects directly to the host computer's Q-Bus backplane. The microprocessor architecture ensures excellent reliability and compactness, while significantly reducing communications overhead for the host computer.

The CS02/H1 Communications Subsystem consists of two units: the CC02 Controller Module, and a distribution panel. Distribution panels are available that fit in either an LSI-11 CPU or a Micro/PDP-11 or MicroVAX chassis. Two asynchronous interfaces are available, RS-232 and RS-423.

The relationship of the CS02/H components in an LSI-11 is shown in Figure 1-1. The relationship of CS02/H components in a Micro/PDP-11 or MicroVAX is shown in Figure 1-2. The component relationships for both applications are described in the following subsections.

### 1.3.1 CC02 CONTROLLER MODULE

The microprocessor-based CC02 is contained on a single quad-wide printed circuit board assembly (PCBA) which plugs directly into any Q-Bus backplane slot. The CC02's firmware-driven microprocessor performs the DH11/DM11 or DHV11 emulation.

### 1.3.2 LSI-11 DISTRIBUTION PANELS (CP22 and CP25)

When the CS02/H Communications Subsystem is mounted in an LSI-11, the CC02 Controller Module is used with either the CP22 or CP25 Distribution Panels. The CC02 Controller Module interfaces with the distribution panel via two 50-wire and one 16-wire flat cables. Signals are distributed by the distribution panel via 16 subminiature D-type connectors.

The LSI-11 distribution panels are designed to be rack-mounted on the rear RETMA rails of a CPU cabinet. An Emulex two-panel rack mount chassis accompanies these distribution panel.

### 1.3.3 CP24 DISTRIBUTION PANEL

When the CS02/H Communications Subsystem is mounted in a Micro/PDP-11 or MicroVAX, the CC02 Controller Module is used with the CP24 Distribution Panel. The CP24 Distribution Panel is mounted in the rear bulkhead of the Micro/PDP-11 cabinet. The CC02 Controller Module interfaces with the CP24 Distribution Panel via two 50-wire flat cables. Signals are distributed by the CP24 Distribution Panel via 16 nine-pin subminiature D-type connectors.

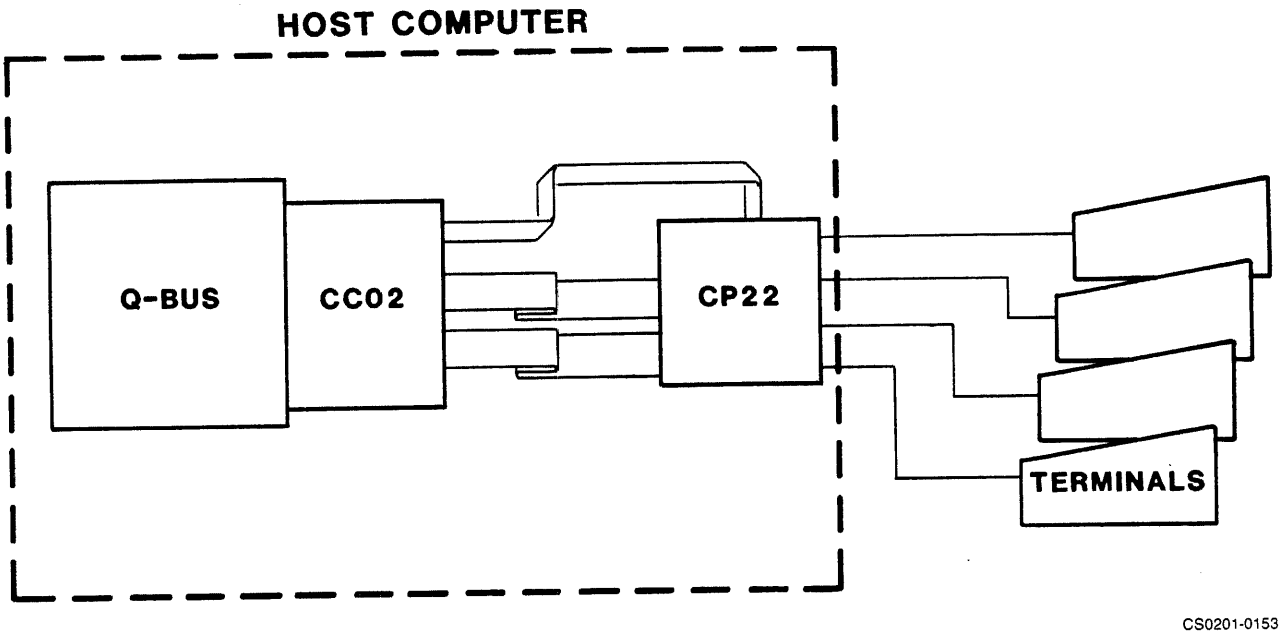



Figure 1-1. Subsystem Configuration in an LSI-11

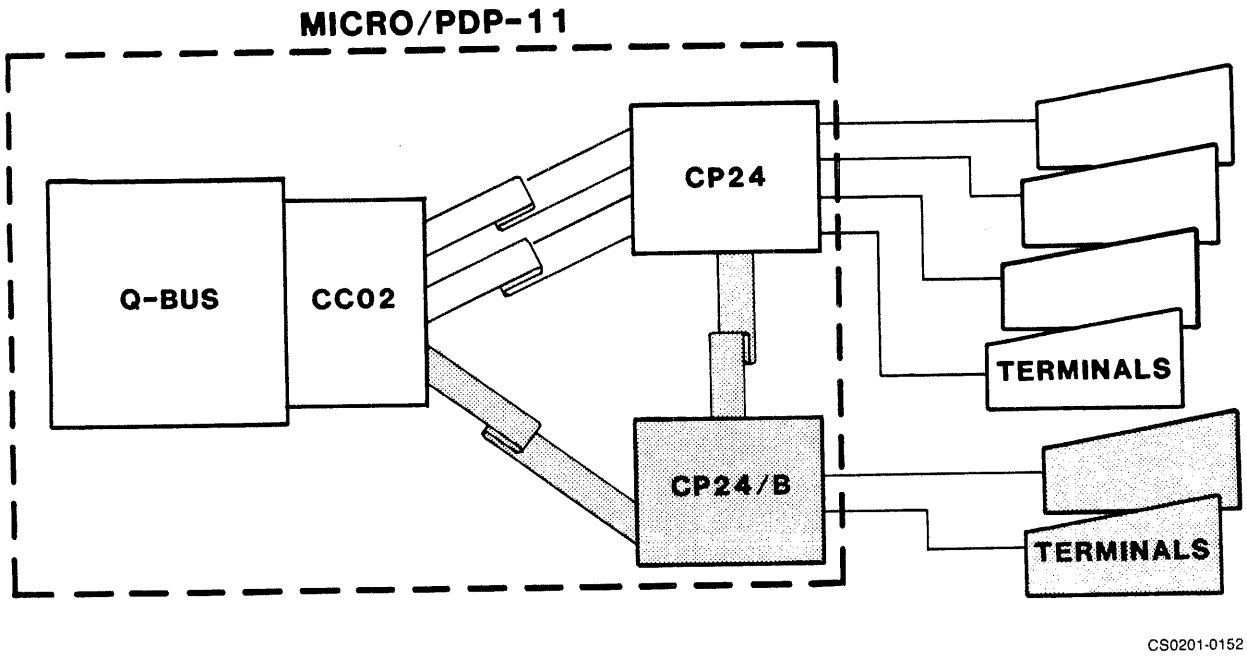



Figure 1-2. Subsystem Configuration in a Micro PDP/VAX

### 1.3.4 CP24/B DISTRIBUTION PANEL

When the CS02/H Communications Subsystem is mounted in the Micro/PDP-11 or MicroVAX, an optional CP24/B Distribution Panel may be used in addition to the CP24 Distribution Panel. The CP24/B Distribution Panel provides extra modem control signals for the first four channels, and replaces CH.0 through CH.3 on the CP24 Distribution Panel. The CC02 Controller interfaces to the CP24/B Distribution Panel via one 16-wire flat cable. The CP24 Distribution Panel interfaces with the CP24/B Distribution Panel via one 34-wire flat cable. Signals are distributed by the CP24/B Distribution Panel via four RS-232-C compatible subminiature D-type connectors.

## 1.4 SUBSYSTEM MODELS AND OPTIONS

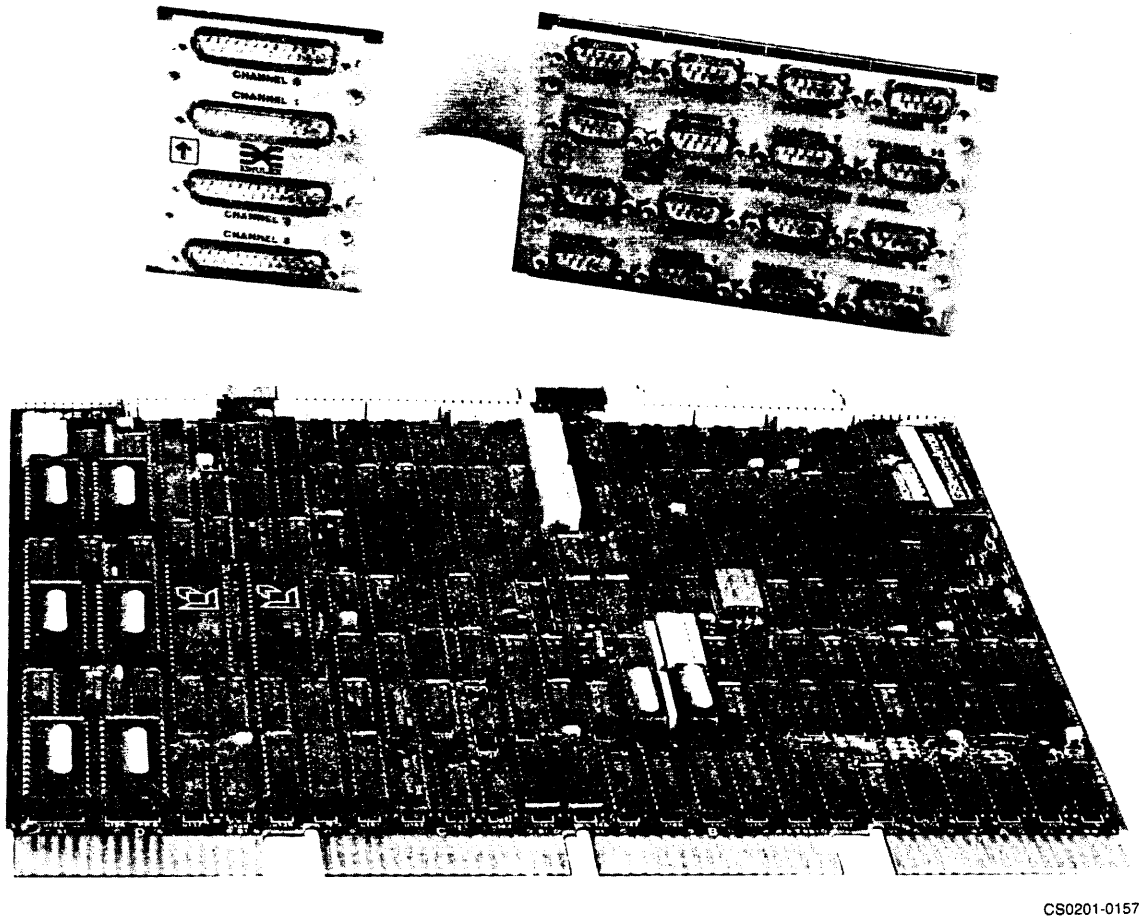
Table 1-1 shows the contents of the CS02/H subsystem. Subsection 1.4.1 describes the distribution panels available and lists their part numbers. Figure 1-2 shows the CS02/H with a CP22 Distribution Panel.

Table 1-1. CS02/H Contents and Part Numbers

| Itm | Qty | Description | Part Number | Comment |
|---|---|---|---|---|
| 1 | 1 | CC02 Controller Module | CS0210201-H1X | |
| 2 | 1 | CS02 Extended Address Option Kit | CS0113001 | For 22-bit addressing |
| 3 | 1 | Distribution Panel | Varies | See subsection 1.4.1 |
| 4 | 1 | Wrap-Around Connector | Varies | For diagnostic testing with distribution panel |
| 5 | | Ribbon Cable(s) | Varies | CC02 to distribution panel--see subsection 1.4.2 |
| 6 | 1 | CS02/H Technical Manual | CS0251001 | |
| 7 | 1 | Distribution Panel Technical Manual | Varies | |

### 1.4.1 DISTRIBUTION PANELS

Three distribution panels can be used with the CS02/H: the CP22 (RS-232-C), the CP24 (RS-232-C for the Micro/PDP-11 and MicroVAX), and the CP25 (RS-422-A). All of these panels are FCC compliant.



CS0201-0157

Figure 1-3. CS02/H Basic Communications Subsystem (shown with CP24 and CP24/B Distribution Panels)

The CP22 and CP25 distribution panels each contain 16 ports. They are the same size as DEC's DMF32 distribution panel and can be mounted directly in its place in CPU cabinets that are DMF32 compatible. They can also be mounted directly on RETMA rails if the rack mount chassis option is used. Mounting options are covered in more detail in the distribution panel technical manual.

The CP22 and CP25 support partial modem control on all 16 ports. The CP22 also supports full modem controls on the first four channels.

The CP22 can be ordered with EMI filters installed. This is a special order item, however, and is not generally required.

The CP24 Distribution Panel is designed to be mounted in a Micro/PDP-11 or MicroVAX chassis. The CP24 contains 16 ports with partial modem control. The CP24 uses 9-pin connectors on its 16 ports. If the optional CP24/B is ordered, the first four channels use standard 25-pin connectors and support full modem controls.

Table 1-2 lists the features and part numbers of each of the distribution panels.

Table 1-2. Distribution Panels Available for the CS02/H

| Dist. Panel | Part Number | Description |
|---|---|---|
| CP22-01 | CP2210201-01 | RS-232-C |
| CP22-02 | CP2210201-02 | RS-232-C, with EMI filters |
| CP24 | CP2410201-00 | RS-232-C, for Micro/PDP/VAX |
| CP24/B | CP2410202 | RS-232-C, provides full modem control on first four lines when used with CP24 |
| CP25 | CP2510401 | RS422-A or RS-232-C |

### 1.4.2 CABLES FOR THE CS02/H SUBSYSTEM

The cables used to attach the distribution panel to the CC02 controller module vary depending on the distribution panel used. Table 1-3 shows the cables required for each type of distribution panel.

Table 1-3. Distribution Panel Cables

| Dist. Panel | Cables Required | Comment |
|---|---|---|
| CP22 | CU2111201-02 (2)<br>CU0211201-03 | 50-wire ribbon cable, 8 foot<br>16-wire ribbon cable, 8 foot (provides full modem control on first four channels) |
| CP24 | CU2411202 (2) | 50-wire ribbon cable, 1 foot |
| CP24/B | CU2411201 | 34-wire ribbon cable, .25 feet (connects CP24/B to CP24) |
| | CU0211201-01 | 16-wire ribbon cable, 1.5 feet (connects CP24/B to CC02) |
| CP25 | CU2111201-02 (2) | 50-wire ribbon cable |

## 1.5 FEATURES

Several features enhance the usefulness of the CS02/H Communications Subsystem.

### 1.5.1 MICROPROCESSOR DESIGN

The CS02/H design incorporates an eight-bit, high-performance bipolar microprocessor to perform all controller functions. The microprocessor approach provides a reduced component count, high reliability, easy maintainability, and most importantly the ability to perform an emulation of the equivalent DEC controller. Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate by providing enhancement features such as built-in self-test during power-up, and channel-loop test.

### 1.5.2 FCC COMPLIANCE

The CS02/H Communications Subsystem complies with the appropriate Federal Communications Commission (FCC) standards that limit EMI radiation from computing devices. All models, if operated within Class A compliant cabinets, comply with the limits for FCC Class A.

### 1.5.3 SELF-TEST

The CC02 Controller Module incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, the on-board memory, and the dual universal asynchronous receiver transmitters (DUARTs). Although this test does not completely test all circuitry, successful execution indicates a very high probability that the CC02 Controller Module and the DUARTs are operational. The CC02 Controller Module uses on-board light emitting diodes (LEDs) to indicate self-test failure. In the event of self-test failure, the CC02 Controller Module cannot be addressed from the CPU.

### 1.5.4 PROGRAMMABLE CHANNEL PARAMETERS

Parameters on all 16 channels provided by the CS02/H Communications Subsystem can be set individually under program control.

Parameters for channels include:

- All popular data rates from 50 to 38,400 bps
- The number of stop bits per character
- Parity (odd, even, or none)
- The number of data bits per character.

### 1.5.5 DMA ON TRANSMIT

The subsystem performs full-word direct memory access (DMA) on transmit. This feature considerably reduces the CPU overhead associated with data communications, especially when the host system is running terminal-I/O intensive software.

## 1.6 COMPATIBILITY

### 1.6.1 DIAGNOSTICS

The CS02/H Communications Subsystem executes the standard DEC DH11 and DM11 Diagnostics when Emulex-supplied patches are used (see Appendix B). The CS02/H also executes the standard DHV11 diagnostics.

### 1.6.2 OPERATING SYSTEMS

The CS02/H Communications Subsystem is compatible (with minor modification if 22-bit addressing is used for the DH11 emulation), with all DEC LSI-11 and Micro/PDP-11 operating systems that support the DEC DH11 Communications Multiplexer and the DEC DHV11 Asynchronous Multiplexer. It is also compatible with all MicroVAX operating systems if the CC02 firmware set is Revision F or higher.

### 1.6.3 HARDWARE

The CS02/H Communications Subsystem is electrically and mechanically compatible with all Q-Bus applications.

### 1.6.4 DISTRIBUTION PANEL CONNECTORS

Emulex distribution panels are available that are compatible with the following interfaces:

- RS-232-C
- RS-422-A
- 20 mA current loop (requires nonstandard backplane wiring)

Details of distribution panel compatibility and functionality are in the distribution panel technical manual that came with your communications subsystem.

### 1.6.5 MODEM CONTROLS SUPPORTED

Modem controls necessary for full-duplex operation are available on all channels. Pin/signal assignments vary with distribution panels, but the following modem controls are available on all distribution panels:

- Carrier Detect
- Data Terminal Ready
- Ring Indicator

On the CP22 and CP24/B, the following additional modem control signals are available on the first four channels:

- Request to Send
- Clear to Send
- Data Set Ready

Consult your distribution panel technical manual for more details on the port interface signal assignments.

## 2.1 OVERVIEW

This section contains general, physical, and environmental specifications for the CS02/H controller module. Specifications for the distribution panels are contained in their technical manuals. Controller specifications are contained in tables, each in its own subsection. The subsections include:

| Subsection | Title |
|---|---|
| 2.2 | General and Electrical Specifications |
| 2.3 | Physical Specifications |
| 2.4 | Environmental Specifications |

## 2.2 GENERAL SPECIFICATIONS

General specifications for the CS02/H Communications Subsystem are contained in Table 2-1.

Table 2-1. CS02/H General Specifications

| Parameter | Description |
|---|---|
| **Emulation** | Provides complete functional emulation of one DEC DH11 multiplexer and partial emulation of the associated DM11 modem control units, or complete functional emulation of two DHV11 multiplexers |
| Operating System Compatibility | RSX-11M, RSX-11M+, RSTS/E. MicroVMS supported by firmware revision F and higher. |
| Diagnostic Compatibility | |
| DH11 | ZDHMD0 |
| DHV11 | CVDHAA0, CVDHBA0, CVDHCA0 |
| Number of Channels | 16 |
| Throughput Rate | 50,000 characters per second |

continued on next page

Table 2-1. CS02/H General Specifications (continued)

| Parameter | Description |
|---|---|
| Receive Silo | 64-character FIFO buffer for each DH11, expandable to 256, interrupt programmable for any FIFO fill level; 256-character FIFO for each DHV11 |
| Transmission Modes | Full-duplex, Half-duplex |
| Transmission Speeds | 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600, 19200, 38400 bps |
| Character Formats | Character lengths: 5 to 8 bit<br>Stop bits: 1, 1.5, or 2<br>Parity: odd, even, or none |
| Modem Status | CD, Ring, CTS, DSR |
| Modem Control | RTS, DTR |
| **Emulex Distribution Panels Supported** | CP22<br>CP24<br>CP24/B<br>CP25 |
| **Indicators** | On Line<br>Fault<br>Activity |
| **Option Switches** | DIP switches for selection of controller options |
| **CPU Interface** | Standard Q-Bus interface. One bus load for both DH11 and DM11, or one bus load for DHV11. |
| DMA Address Range | 0 - 4.19 megabytes |
| DMA Transfer | 16-bit word with parity check |
| Device Address | Switch selectable to cover most DEC-defined addresses |

continued on next page

Table 2-1. CS02/H General Specifications (continued)

| Parameter | Description |
|---|---|
| Vector Address | Switch selectable to cover most DEC defined vector addresses. |
| Priority Level | BR5 for DH11<br>BR4 for DM11<br>BR5 for DHV11 (firmware Rev E and below)<br>BR4 for DHV11 (firmware Rev F and above) |
| **Electrical** | |
| Power | +5 VDC ± 5%, 6.2 amps (typical)<br>+12 VDC ± 5%, 0.5 amps (typical) |

## 2.3 PHYSICAL SPECIFICATION

Table 2-2 contains the physical specifications for the CC02 controller module. Figure 2-1 depicts the CC02 Controller Module PCBA.

Table 2-2. CC02 Controller Module Physical Specifications

| Parameter | Description |
|---|---|
| **Packaging** | Single quad-sized, four-layer PCBA |
| Dimensions | 10.4 inches x 8.7 inches |
| Shipping Weight | 4 pounds |
| **Connectors** | |
| Q-Bus | Standard DEC PCBA edge connectors |
| Distribution Panel | One 16-pin and two 50-pin male header connectors |

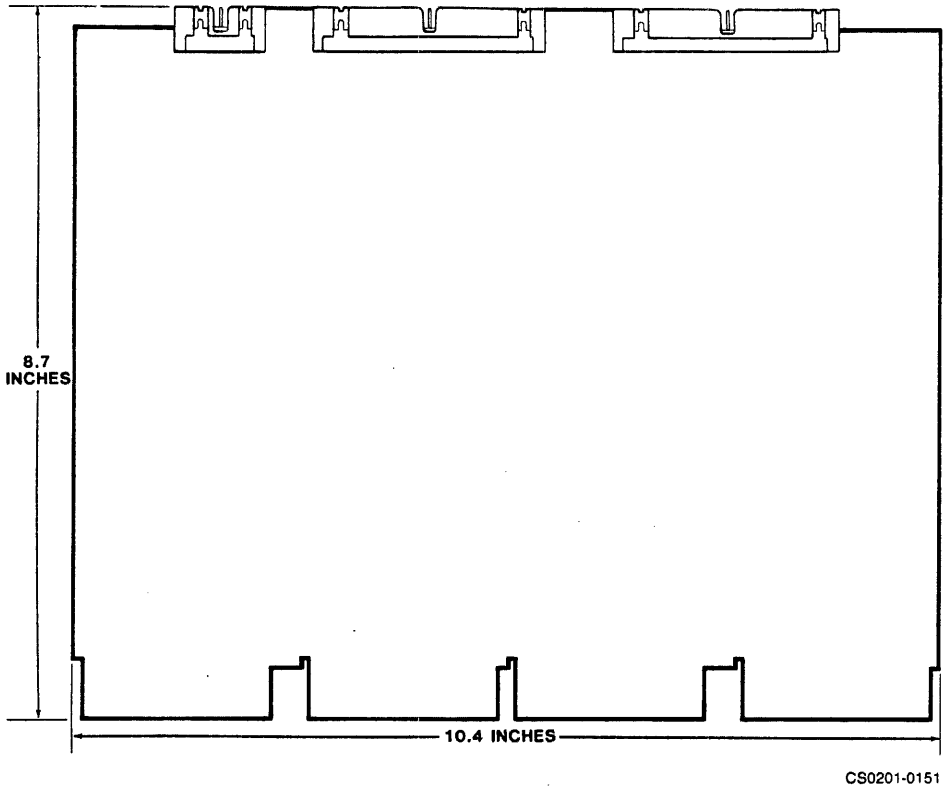



Figure 2-1. CC02 Controller Module Dimensions

## 2.4 ENVIRONMENTAL SPECIFICATIONS

Table 2-3 contains environmental specifications for the CC02 Controller Module.

Table 2-3. CC02 Controller Module Environmental Specifications

| Parameter | Description |
|---|---|
| **Operating Temperature** | 10°C (50°F) to 40°C (104°F)<br><br>Maximum temperature is reduced 1.8°C per 1000 meters (1°F per 1000 feet) altitude |
| **Relative Humidity** | 10% to 90% with a maximum wet bulb of 28°C (82°F) and a minimum dewpoint of 2°C (3.6°F) |
| **Cooling** | 11 cubic feet per minute |
| **Heat Dissipation** | 70 BTU per hour |

## 3.1 OVERVIEW

This section is designed to help you plan the installation of your CS02/H Communications Subsystem. Taking a few minutes and planning the configuration of your subsystem before beginning its installation will result in a smoother installation with less system down time. As a planning tool, this section contains discussions of some of the practical matters that need to be considered before you begin your installation.

This section contains CS02/H application examples and configuration procedures. The subsections include:

| Subsection | Title |
|---|---|
| 3.2 | Configurations |
| 3.3 | Application Examples |
| 3.3 | Q-Bus Addresses and Vectors |

The procedures contained in these subsections will ensure that you get the most from your CS02/H Communications Subsystem.

### 3.1.1 Q-BUS ADDRESS CONVENTION

The Q-Bus addresses used in this manual are for a 22-bit Q-Bus. For 18-bit addressing subtract $17000000_8$ to obtain the desired address.

### 3.1.2 CONFIGURATION DEFINED

As used in the computer industry, the term configuration is generally used in reference to the physical and logical arrangement of a system, or put another way, the manner in which the parts of a system relate to one another.

When used this way, the word configuration has quite a number of implications: size (capacity, speed, bandwidth), cabling (what is hooked to what), logical arrangement (which functions are combined on which components), location (bus slot, bus address, vector, unit address), and so on.

Many of these factors can be affected by the user, either through the use of switches or by cabling the system one way instead of another. In other words, the configuration, and thus the function, of a system is defined and determined by the user.

## 3.2 CONFIGURATIONS

The CS02/H is designed to provide 16 asynchronous communications channels. The CS02/H emulates either a DEC DH11 with associated DM11 modem control, or two DEC DHV11s. The CS02/H Subsystem allows a certain number of variables. The subsections below describe the functions and options on each distribution panel that should be considered before configuring the CS02/H Subsystem.

### 3.2.1 DISTRIBUTION PANELS

Different distribution panels have different features, and which distribution panel you use depends on what applications you are planning to use the CS02/H for.

Three Emulex distribution panels can be used with the CS02/H: the CP22, CP24, and CP25. There are several main differences among them:

- The CP24 is the only panel that mounts in a Micro/PDP-11 or MicroVAX chassis.
- The CP22 and CP24/B offer full modem controls on the first four channels. The CP25 supports partial modem control on all channels.
- The CP25 offers an RS-422-A interface as an option on each port. The CP22 uses an RS-232-C interface. If you are planning to operate your terminals more than a few hundred feet from the distribution panel, the RS-422-A option is particularly useful. To use this option, your terminals must have RS-422-A interface circuits or you must use an RS-422-A converter, such as Emulex's CV422.

#### 3.2.1.1 CP22 Distribution Panel

The CP22 is a passive, FCC-compliant distribution panel which can be mounted directly in DMF32-compatible CPU cabinets or rack-mounted on RETMA rails. It provides an RS-232-C interface on all ports.

Channels zero through three on the CP22 may be individually reconfigured to to provide an RS-423 interface. The CP22 Technical Manual describes the procedure for making this change.

Channels zero through three also provide the additional modem signals necessary for half-duplex operation.

#### 3.2.1.2 CP24 and CP24/B Distribution Panels

The CP24 is a passive, FCC-compliant distribution panel which can be mounted in a Micro/PDP-11 or MicroVAX chassis. It uses 9-pin connectors and provides an RS-232-C interface at each of its 16 ports.

The CP24/B is an optional panel and is used in addition to the CP24. The CP24/B contains four 25-pin subminiature connectors that replace the first four channels of the CP24. If it is used, the first four channels provide full modem control support (the CP24 by itself provides partial modem support on all 16 ports).

Channels zero through three on the CP24 may be individually reconfigured to to provide an RS-423 interface. The CP24 Technical Manual describes the procedure for making this change.

#### 3.2.1.4 CP25 Distribution Panel

The CP25 is an active, FCC-compliant distribution panel which can be directly mounted in DMF32-compatible CPU cabinets or rack-mounted on RETMA rails. It provides either an RS-232-C or an RS-422-A interface at each port. Each port can be configured independently.

The RS-422-A interface allows higher transmission speeds and much longer cable lengths than the RS-232-C interface. For example, at 9600 baud the maximum practical cable length with the RS-232-C interface is 250 feet, and performance is guaranteed only up to 50 feet. The RS-422-A interface, however, allows cable lengths as long as 4000 feet with every transmission speed supported by the CS02/H.

## 3.3 APPLICATION EXAMPLES

The CS02/H Communications Subsystem has several applications. Some examples are presented below.

Example 3-1. Figure 3-1 illustrates a typical LSI-11 application with a half-duplex remote line. This subsystem consists of the CC02 Controller Module and the CP22 Distribution Panel. The two components are mounted in a DEC LSI-11 computer. A half-duplex modem is connected to CH.0 of the CP22 Distribution Panel. Terminals and printers are connected to the remaining 15 channels of the panel.

Example 3-2. Figure 3-2 illustrates a typical Micro/PDP-11 or MicroVAX application with a full- and half-duplex remote line. This subsystem consists of the CC02 Controller Module, the CP24 Distribution Panel and the optional CP24/B Distribution Panel. The three components are mounted in a DEC Micro/PDP/VAX computer. A half-duplex modem is connected to Channel 0 of the CP24/B Distribution Panel. A full-duplex modem is connected to Channel 4 of the CP24 Distribution Panel. Terminals and printers are connected to Channels 1 through 3 of the CP24/B Distribution Panel and to Channels 5 through 15 of the CP24 Distribution Panel. Channels 0 through 3 on the CP24 Distribution Panel are shaded to indicate that they are not used when the CP24/B Distribution Panel is used.

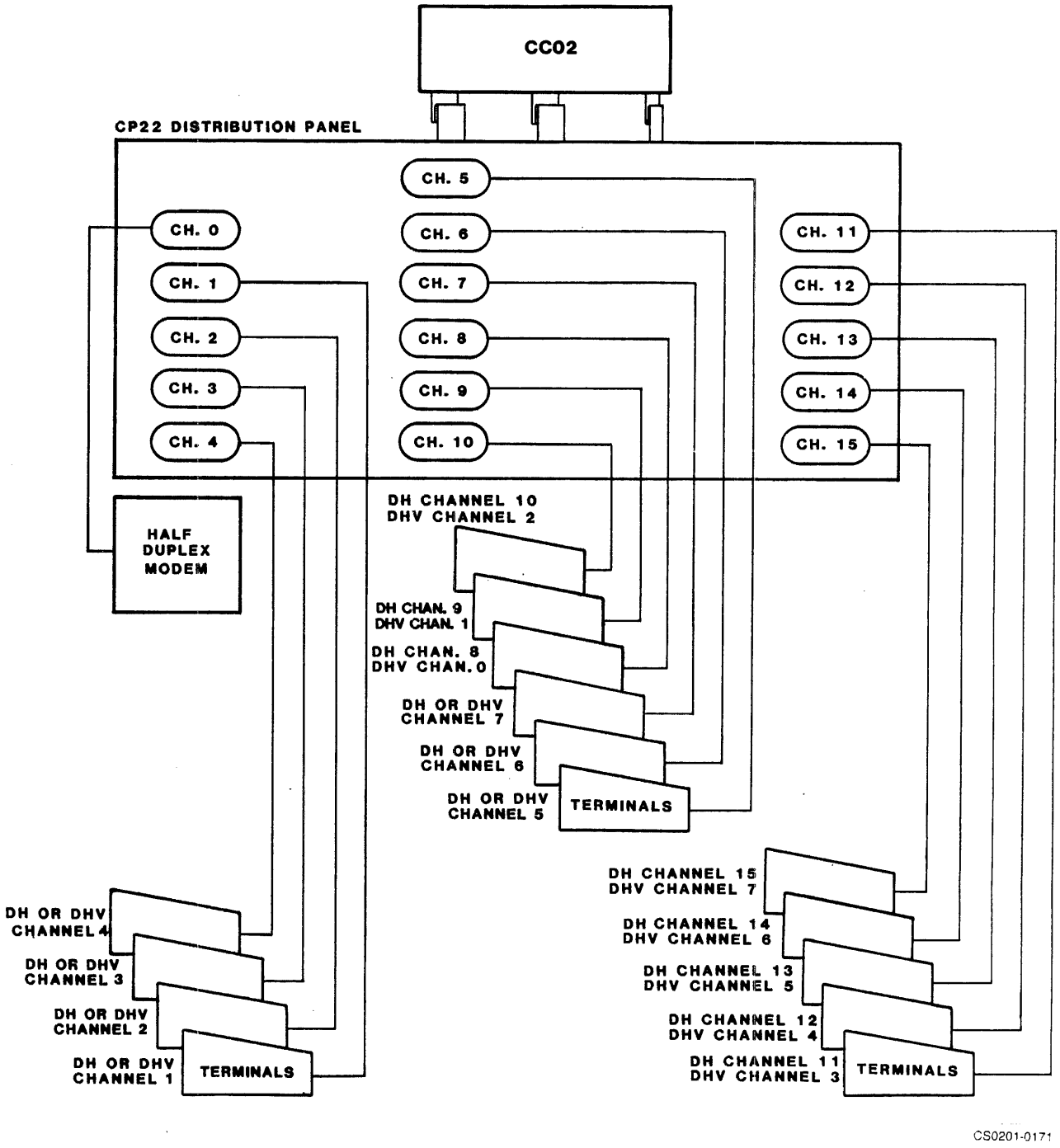



Figure 3-1. An LSI-11 Application

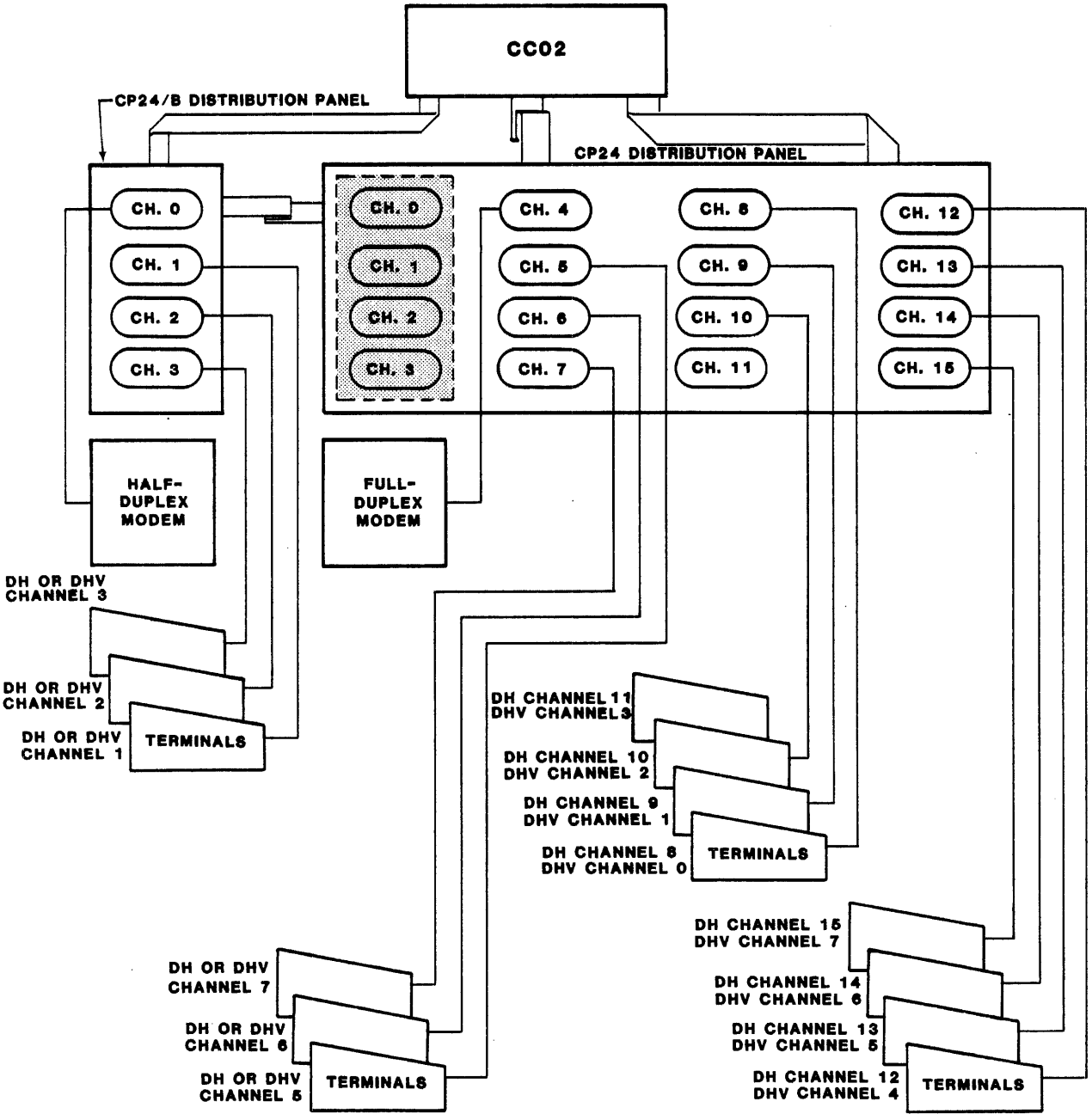



Figure 3-2. A Micro/PDP/VAX Application

## 3.4 Q-BUS ADDRESSES AND VECTORS

The CS02/H interfaces directly with the DEC host computer's Q-Bus backplane. The CS02/H performs one DH11/DM11 emulation, or two DHV11 emulations. The DH11 emulation uses a block of eight addresses which are selected from a pool of floating addresses. Each DM11 uses a block of two bus addresses. Addresses for DM11-type devices are assigned to a specific range. The DHV11 emulation uses a block of eight addresses which are selected from a pool of floating addresses in the Q-Bus I/O page.

The DH11 emulations require two vector addresses; each DM11 emulation uses only one vector address. The DHV11 emulation requires two vector addresses. The vector addresses for all types of devices are selected from a pool of floating vector addresses assigned by the user according to an algorithm that has been defined by DEC.

The following discussion presents the algorithm for assigning floating bus address space and vectors for RSTS/E, RSX-11M, and MicroVMS. DM11 bus addresses are discussed in subsection 4.3.2.1.

### 3.4.1 DETERMINING THE BUS ADDRESS FOR USE WITH AUTOCONFIGURE

The term Autoconfigure refers to a software utility that is run when the computer is bootstrapped. This utility finds and identifies I/O devices in the I/O page of system memory.

Addresses for those devices not assigned fixed numbers are selected from the floating address space ($17760010_8$ - $17763776_8$) of the Q-Bus input/output (I/O) page. This means that the presence or absence of floating devices will affect the assignment of addresses to other floating-address devices. Similarly, many devices have floating interrupt vector addresses. According to the DEC standard, vectors must be assigned in a specific sequence and the presence of one type of device will affect the correct assignment of vectors for other devices.

The bus address for a floating-address device is selected according to the algorithm used during autoconfigure. The algorithm is used in conjunction with a Device Table, Table 3-1.

Some devices (like the DM11) have fixed addresses reserved for them. Autoconfigure detects their presence by simply testing their standard address for a response. For the DH11 emulation, the System Control Register (SCR) address, which is the first register of the block, is tested. For the DHV11 emulation, the Control Status Register (CSR), which is the first register of the block, is tested.

Essentially, Autoconfigure checks each valid bus address in the floating address space for the presence of a device. Autoconfigure expects any devices installed in that space to be in the order specified by the Device Table. Also, the utility expects an eight-byte block to be reserved for each device that is not installed in the

system. Each empty block tells Autoconfigure to look at the next valid address for the next device on the list.

When a device is detected, a block of addresses is reserved for the device according to the number of registers it employs. The utility then looks at the next first register for that device type. If there is a device there, it is assumed to be of the same type as the one before it and a block is reserved for that device. If there is no response at the next address, that space is reserved to indicate that there are no more devices of that type. Then the utility checks the starting address (at the appropriate boundary) for the next device in the table.

Table 3-1. SYSGEN Device Table

| Rank | Device | Number of Registers | Octal Modulus | Rank | Device | Number of Registers | Octal Modulus |
|---|---|---|---|---|---|---|---|
| 1 | DJ11 | 4 | 10 | 16 | KW11-C | 4 | 10 |
| 2 | **DH11** | 8 | 20 | 17 | Reserved | 4 | 10 |
| 3 | DQ11 | 4 | 10 | 18 | RX11[2] | 4 | 10 |
| 4 | DU11,DUV11 | 4 | 10 | 18 | RX211[2] | 4 | 10 |
| 5 | DUP11 | 4 | 10 | 18 | RXV11[2] | 4 | 10 |
| 6 | LK11A | 4 | 10 | 18 | RXV21[2] | 4 | 10 |
| 7 | DMC11 | 4 | 10 | 19 | DR11-W | 4 | 10 |
| 7 | DMR11 | 4 | 10 | 20 | DR11-B[3] | 4 | 10 |
| 8 | DZ11[1] | 4 | 10 | 21 | DMP11 | 4 | 10 |
| 8 | DZV11 | 4 | 10 | 22 | DPV11 | 4 | 10 |
| 8 | DZS11 | 4 | 10 | 23 | ISB11 | 4 | 10 |
| 8 | DZ32 | 4 | 10 | 24 | DMV11 | 8 | 20 |
| 9 | KMC11 | 4 | 10 | 25 | DEUNA[2] | 4 | 10 |
| 10 | LPP11 | 4 | 10 | 26 | UDA50[2] | 2 | 4 |
| 11 | VMV21 | 4 | 10 | 27 | DMF32 | 16 | 40 |
| 12 | VMV31 | 8 | 20 | 28 | KMS11 | 6 | 20 |
| 13 | DWR70 | 4 | 10 | 29 | VS100 | 8 | 20 |
| 14 | RL11[2] | 4 | 10 | 30 | Reserved | 2 | 4 |
| 14 | RLV11[2] | 4 | 10 | 31 | KMV11 | 8 | 20 |
| 15 | LPA11-K[2] | 8 | 20 | 32 | **DHV11** | 8 | 20 |

[1]DZ11-E and DZ11-F are treated as two DZ11s.
[2]The first device of this type has a fixed address. Any extra devices have a floating address.
[3]The first two devices of this type have a fixed address. Any extra devices have a floating address.

In summary, there are four rules that pertain to the assignment of device addresses in floating address space:

1. Devices with floating addresses must be attached (assigned addresses) in the order in which they are listed in the Device Table, Table 3-1.

2. The bus address for a given device type must be assigned on word boundaries according to the number of Q-Bus-accessible registers that the device has. The following table relates the number of device registers to possible word boundaries.

| Number of Device Registers[1] | Possible Boundaries |
|---|---|
| 1 | Any Word |
| 2 | XXXXX0, XXXXX4 |
| 3,4 | XXXXX0 |
| 5,6,7,8 | XXXX00,XXXX20,XXXX40,XXXX60 |
| 9 thru 16 | XXXX00,XXXX40 |

[1]See Table 3-1.

The Autoconfigure utility inspects for a given device type only at one of the possible boundaries for that device. That is, the utility does not look for a DZV11 (4 registers) at an address that ends in 4.

3. A gap must follow the register block of any installed device to indicate that there are no more of that type of device. This gap must start on the proper bus address boundary for that type of device.

4. A gap must be reserved in floating address space for each device type that is not installed in the current system. The gap must start on the proper word boundary for the type of device the gap represents. That is, a single DZV11 installed at $17760120_8$ would be followed by a gap starting at $17760130_8$ to show a change of device types. A gap to show that there are none of the next device on the list, a KMC11, would begin at $17760140_8$, the next legal boundary for a KMC11-type device.

### 3.4.2 DETERMINING THE VECTOR ADDRESS FOR USE WITH AUTOCONFIGURE

There is a floating vector address convention that is used for communications and other devices which interface with the Q-Bus. These vector addresses are assigned in order starting at $300_8$ and proceeding upwards to $774_8$. Table 3-2 shows the assignment sequence. For a given system configuration, the device with the highest floating vector rank (1) would be assigned to vector address 300. Additional devices of the same type would be assigned subsequent vector addresses according to the number of vectors required per device, and according to the starting boundary assigned to that device type.

Table 3-2. Priority Ranking for Floating Vectors Addresses (starting at $300_8$ and proceeding upwards)

| Rank | Device | Number of Vectors | Octal Modulus (address) |
|---|---|---|---|
| 1 | DC11 | 4 | 10 |
| 1 | TU58 | 4 | 10 |
| 2 | KL11[1] | 4 | 10 |
| 2 | DL11-A[1] | 4 | 10 |
| 2 | DL11-B[1] | 4 | 10 |
| 2 | DLV11-J[1] | 16 | 10 |
| 2 | DLV11,DLV11-F[1] | 4 | 10 |
| 3 | DP11 | 4 | 10 |
| 4 | DM11-A | 4 | 10 |
| 5 | DN11 | 2 | 4 |
| 6 | **DM11-BB/BA** | 2 | 4 |
| 7 | DH11 modem control | 2 | 4 |
| 8 | DR11-A, DRV11-B | 4 | 10 |
| 9 | DR11-C, DRV11 | 4 | 10 |
| 10 | PA611 (reader+punch) | 8 | 10 |
| 11 | LPD11 | 4 | 10 |
| 12 | DI07 | 4 | 10 |
| 13 | DX11 | 4 | 10 |
| 14 | DL11-C to DLV11-F | 4 | 10 |
| 15 | DJ11 | 4 | 10 |
| 16 | **DH11** | 4 | 10 |
| 17 | VT40 | 8 | 10 |
| 17 | VSV11 | 8 | 10 |
| 18 | LPS11 | 12 | 10 |
| 19 | DQ11 | 4 | 10 |
| 20 | KW11-W, KWV11 | 4 | 10 |
| 21 | DU11, DUV11 | 4 | 10 |
| 22 | DUP11 | 4 | 10 |
| 23 | DV11 + modem control | 6 | 10 |
| 24 | LK11-A | 4 | 10 |
| 25 | DWUN | 4 | 10 |
| 26 | DMC11 | 4 | 10 |
| 26 | DMR11 | 4 | 10 |
| 27 | DZ11/DZS11/DZV11 | 4 | 10 |
| 27 | DZ32 | 4 | 10 |
| 28 | KMC11 | 4 | 10 |
| 29 | LPP11 | 4 | 10 |
| 30 | VMV21 | 4 | 10 |
| 31 | VMV31 | 4 | 10 |
| 32 | VTV01 | 4 | 10 |
| 33 | DWR70 | 4 | 10 |
| 34 | RL11/RLV11[2] | 2 | 4 |
| 35 | TS11[2], TU80[2] | 2 | 4 |
| 36 | LPA11-K | 4 | 10 |

continued on next page

Table 3-2. Priority Ranking for Floating Vectors Addresses (starting at $300_8$ and proceeding upwards) (continued)

| Rank | Device | Number of Vectors | Octal Modulus (address) |
|---|---|---|---|
| 37 | IP11/IP300[2] | 2 | 4 |
| 38 | KW11-C | 4 | 10 |
| 39 | RX11[2] | 2 | 4 |
| 39 | RX211[2] | 2 | 4 |
| 39 | RXV11[2] | 2 | 4 |
| 39 | RXV21[2] | 2 | 4 |
| 40 | DR11-W | 2 | 4 |
| 41 | DR11-B[2] | 2 | 4 |
| 42 | DMP11 | 4 | 10 |
| 43 | DPV11 | 4 | 10 |
| 44 | ML11[3] | 2 | 4 |
| 45 | ISB11 | 4 | 10 |
| 46 | DMV11 | 4 | 10 |
| 47 | DUENA[2] | 2 | 4 |
| 48 | UDA50[2] | 2 | 4 |
| 49 | DMF32 | 16 | 4 |
| 50 | KMS11 | 6 | 10 |
| 51 | PCL11-B | 4 | 10 |
| 52 | VS100 | 2 | 4 |
| 53 | Reserved | 2 | 4 |
| 54 | KMV11 | 4 | 10 |
| 55 | Reserved | 4 | 10 |
| 56 | IEX | 4 | 10 |
| 57 | **DHV11** | 4 | 10 |

[1]A KL11 or DL11 used as a console, has a fixed vector.
[2]The first device of this type has a fixed vector. Any extra devices have a floating vector.
[3]ML11 is a Massbus device which can connect to a Unibus via a bus adapter.

Vector addresses are assigned on the boundaries indicated in the modulus column of Table 3-2. That is, if the modulus is 10, then the first vector address for that device must end with zero (XX0). If the modulus is 4, then the first vector address can end with zero or 4 (XX0, XX4).

Vector addresses always fall on modulo-4 boundaries (XX0, XX4). That is, a vector address never ends in any number but four or zero. Consequently, if a device has two vectors and the first must start on a modulo-10 boundary, then, using $350_8$ as a starting point, the vectors will be $350_8$ and $354_8$.

### 3.4.3 DH11 SYSTEM CONFIGURATION EXAMPLE

Table 3-3 contains an example of a system configuration that includes devices with fixed addresses and vectors, and floating addresses and/or vectors.

Table 3-4 shows how the device addresses for the floating address devices in Table 3-3 were computed, including gaps.

Table 3-3. Bus and Vector Address Example

| Device | Qty. Devices | Vector Address | Bus Address (in octal) |
|---|---|---|---|
| DM11 | 1 | 300 | 17770500 |
| **DH11** | 1 | 310 | 17760020 |
| DZV11 | 1 | 320 | 17760130 |
| DMV11 | 1 | 330 | 17760360 |
| KMV11 | 1 | 340 | 17760520 |

Table 3-4. Floating Address Computation

| Installed | Device | Number of Registers | | Address (in octal) |
|---|---|---|---|---|
| | DJ11 | 4 | Gap | 17760010 |
| ---> | **DH11** | 8 | | 17760020 |
| | | | Gap | 17760040 |
| | DQ11 | 4 | Gap | 17760050 |
| | DU11 | 4 | Gap | 17760060 |
| | DUP11 | 4 | Gap | 17760070 |
| | LK11A | 4 | Gap | 17760100 |
| | DMC11 | 4 | Gap | 17760110 |
| ---> | **DZV11** | 4 | | 17760120 |
| | | | Gap | 17760130 |
| | KMC11 | 4 | Gap | 17760140 |
| | LPP11 | 4 | Gap | 17760150 |
| | VMV21 | 4 | Gap | 17760160 |
| | VMV31 | 8 | Gap | 17760200 |
| | DWR70 | 4 | Gap | 17760210 |
| | RL11 | 4 | Gap | 17760220 |
| | LPA11-K | 8 | Gap | 17760240 |
| | KW11-C | 4 | Gap | 17760250 |
| | Reserved | 4 | Gap | 17760260 |
| | RX11 | 4 | Gap | 17760270 |
| | DR11-W | 4 | Gap | 17760300 |

continued on next page

Table 3-4. Floating Address Computation (continued)

| Installed | Device | Number of Registers | | Address (in octal) |
|---|---|---|---|---|
| | DR11-B | 4 | Gap | 17760310 |
| | DMP11 | 4 | Gap | 17760320 |
| | DPV11 | 4 | Gap | 17760330 |
| | ISB11 | 4 | Gap | 17760340 |
| ---> | **DMV11** | 8 | | 17760360 |
| | | | Gap | 17760400 |
| | DEUNA | 4 | Gap | 17760410 |
| | UDA50 | 2 | Gap | 17760414 |
| | DMF32 | 16 | Gap | 17760440 |
| | KMS11 | 6 | Gap | 17760460 |
| | VS100 | 8 | Gap | 17760500 |
| | Reserved | 2 | Gap | 17760504 |
| ---> | **KMV11** | 8 | | 17760520 |
| | | | Gap | 17760540 |
| | DHV11 | 8 | Gap | 17760560 |

### 3.4.4 DHV11 SYSTEM CONFIGURATION EXAMPLE

This example uses the same devices as the DH11 example, but substitutes two DHV11's for the single DH11/DM11. Table 3-5 shows the devices and their floating addresses and vectors. Table 3-6 shows how the floating addresses were calculated.

Table 3-5. Bus and Vector Address Example

| Device | Qty. Devices | Vector Address | Bus Address (in octal) |
|---|---|---|---|
| DZV11 | 1 | 310 | 17760100 |
| DMV11 | 1 | 320 | 17760340 |
| KMV11 | 1 | 330 | 17760460 |
| DHV11 | 2 | 340 | 17760520 |
| | | 350 | 17760540 |

Table 3-6. Floating Address Computation

| Installed | Device | Number of Registers | | Address (in octal) |
|---|---|---|---|---|
| | DJ11 | 4 | Gap | 17760010 |
| | DH11 | 8 | Gap | 17760020 |
| | DQ11 | 4 | Gap | 17760030 |
| | DU11 | 4 | Gap | 17760040 |
| | DUP11 | 4 | Gap | 17760050 |
| | LK11A | 4 | Gap | 17760060 |
| | DMC11 | 4 | Gap | 17760070 |
| ---> | **DZV11** | 4 | | 17760100 |
| | | | Gap | 17760110 |
| | KMC11 | 4 | Gap | 17760120 |
| | LPP11 | 4 | Gap | 17760130 |
| | VMV21 | 4 | Gap | 17760140 |
| | VMV31 | 8 | Gap | 17760160 |
| | DWR70 | 4 | Gap | 17760170 |
| | RL11 | 4 | Gap | 17760200 |
| | LPA11-K | 8 | Gap | 17760220 |
| | KW11-C | 4 | Gap | 17760230 |
| | Reserved | 4 | Gap | 17760240 |
| | RX11 | 4 | Gap | 17760250 |
| | DR11-W | 4 | Gap | 17760260 |
| | DR11-B | 4 | Gap | 17760270 |
| | DMP11 | 4 | Gap | 17760300 |
| | DPV11 | 4 | Gap | 17760310 |
| | ISB11 | 4 | Gap | 17760320 |
| ---> | **DMV11** | 8 | | 17760340 |
| | | | Gap | 17760360 |
| | DEUNA | 4 | Gap | 17760370 |
| | UDA50 | 2 | Gap | 17760374 |
| | DMF32 | 16 | Gap | 17760400 |
| | KMS11 | 6 | Gap | 17760420 |
| | VS100 | 8 | Gap | 17760440 |
| | Reserved | 2 | Gap | 17760444 |
| ---> | **KMV11** | 8 | | 17760460 |
| | | | Gap | 17760500 |
| ---> | **DHV11** | 8 | | 17760520 |
| | | | | 17760540 |
| | | | Gap | 17760560 |

## 4.1 OVERVIEW

This section describes the step-by-step procedure for installing the CS02/H Communications Subsystem. The procedure is divided into component-oriented subsections. The subsection titles are listed below to serve as an outline of the procedure.

| Subsection | Title |
|---|---|
| 4.1 | Overview |
| 4.2 | Inspection |
| 4.3 | CC02 Controller Module Setup |
| 4.4 | Distribution Panel Setup |
| 4.5 | Installation of the CC02 in an LSI-11 |
| 4.6 | Installation of the CC02 in a Micro/PDP-11 or MicroVAX |
| 4.7 | Subsystem Power-Up and Verification |

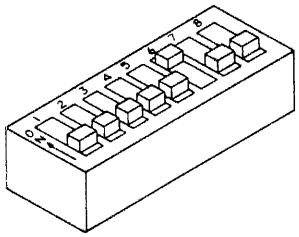
If you are unfamiliar with the subsystem installation procedure, Emulex recommends reading this Installation Section before beginning.

### 4.1.1 SUBSYSTEM CONFIGURATIONS

The information contained in this section is limited to switch setting data and physical installation instructions. **If you are not familiar with the rules for assigning addresses and vectors to devices on the Q-Bus, we strongly recommend reading Section 3, Application and Configuration, before attempting to install this subsystem.**

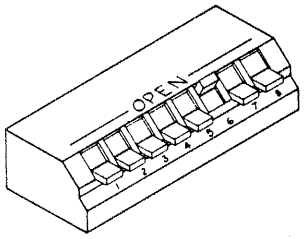
### 4.1.2 DIP SWITCH TYPES

DIP switches used in this product may be any of the following two types:



Slide Switch:

To place a slide switch in the ON position, simply slide the switch in the direction marked ON or CLOSED. To place a slide switch in the OFF position, simply slide the switch in the direction marked OFF or OPEN.




CS0201-0034

Piano Switch:

To place a piano switch in the ON position, move the switch toward the ON or CLOSED position. To place a piano switch in the OFF position, move the switch toward the OFF or OPEN position.

Switch-setting tables in this manual use the numeral one (1) to indicate the ON (closed) position and the numeral zero (0) to indicate the OFF (open) position.

### 4.1.3 Q-BUS ADDRESS CONVENTION

The Q-Bus addresses used in this manual are for a 22-bit Q-Bus. For 18-bit addressing subtract $17000000_8$ to obtain the desired address.

## 4.2 INSPECTION

Emulex products are shipped in special containers designed to provide full protection under normal shipping conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

Unpack the CS02/H subsystem and verify that all components listed on the shipping invoice are present (see subsection 1.4 for an explanation of model numbers and detailed lists of kit contents). Verify that the model or part number (P/N) designation, revision level, and serial numbers agree with those on shipping invoice. These verifications are important to confirm warranty. If evidence of physical damage or identity mismatch is found, notify an Emulex representative immediately.

### 4.2.1 CC02 CONTROLLER MODULE INSPECTION

A visual inspection of the CC02 Controller Module is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage.

All socketed components should be examined carefully to ensure they are properly seated.

### 4.2.2 DISTRIBUTION PANEL INSPECTION

Inspect the distribution panel(s) in the manner described for the CC02 Controller Module.

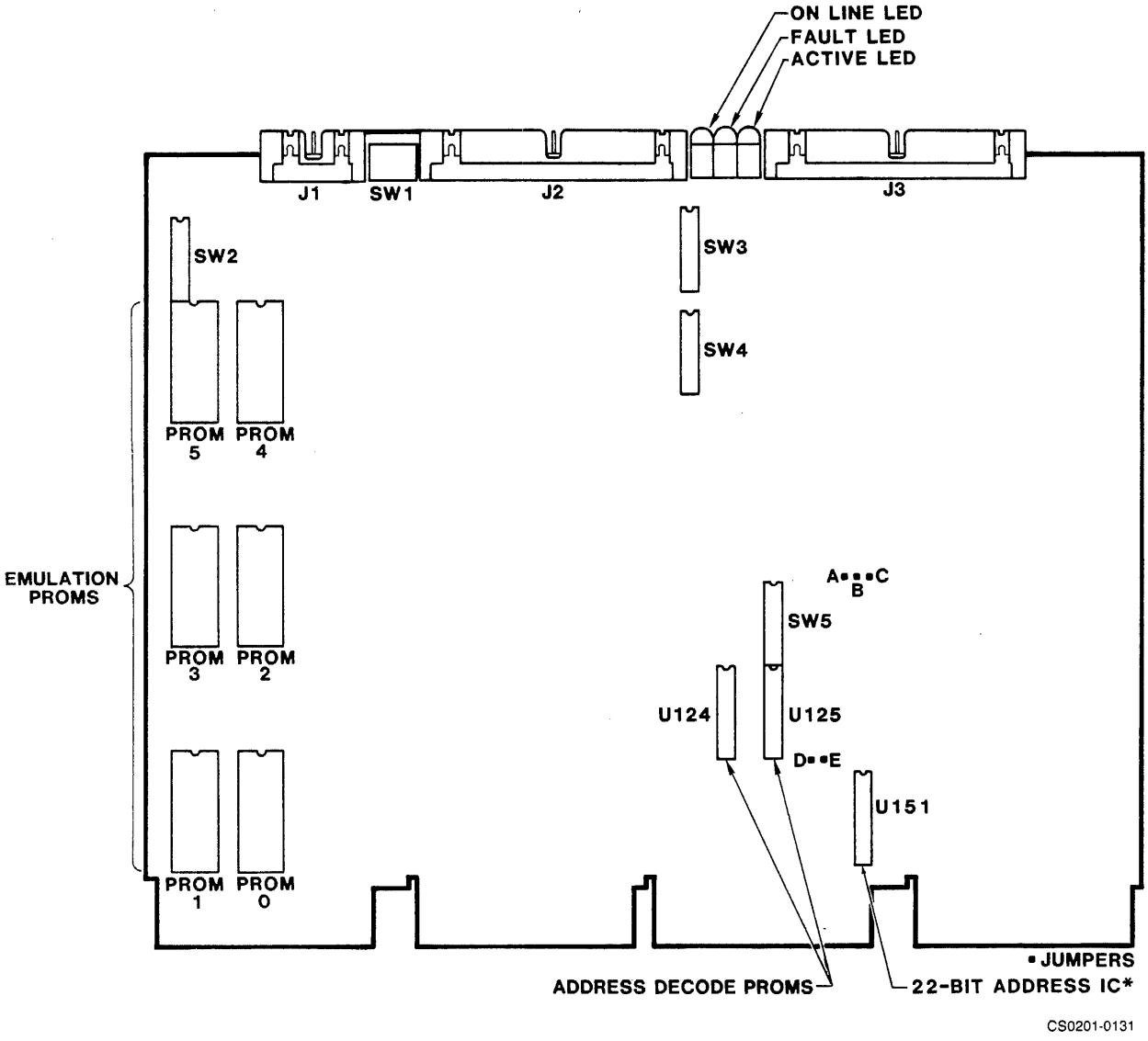
## 4.3 CC02 CONTROLLER MODULE SETUP

See Figure 4-1 for the locations of the configuration switches referenced in the subsections below. The configuration switches should be set before the unit is installed in the CPU card cage because they are not accessible after the unit is installed.

**NOTE**

If any switch position is changed on the CC02 Controller Module, the unit must be either reset by using switch SW1-1 or by removing and restoring the unit's power. This reset is required because the switches are read by an initialization routine in the unit's firmware.

Table 4-1 lists the function and factory configuration of all switches on the CC02 Controller Module for the DH11/DM11 emulation. Table 4-2 lists the function and factory configuration of all switches on the CC02 Controller Module for the DHV11 emulation. The factory configuration switch settings are defined as the minimum necessary to operate the CS02/H subsystem. Table 4-3 lists the functions and factory configuration of all jumpers on the CC02 Controller Module.




*See subsection 4.3.5.7.

Figure 4-1. CC02 Controller Module Component Locations

Table 4-1. DH11/DM11 CC02 Switch Definitions/Factory Configuration

| SW | OFF(0) | ON(1) | Fact | Function | Section |
|---|---|---|---|---|---|
| SW1-1 | Run | Halt/Reset | OFF(0) | Controller Run/Halt | 4.3.5.1 |
| SW1-2 | - | Int Test | OFF(0) | Internal Test Select | 4.3.5.2 |
| SW1-3 | - | Int Test | OFF(0) | Internal Test Select | 4.3.5.2 |
| SW1-4 | - | Int Test | OFF(0) | Internal Test Select | 4.3.5.2 |
| SW2-1 | Disable | Enable | OFF(0) | Clear to Send Flow Control | 4.3.5.9 |
| SW2-2 | 4-15 | All | OFF(0) | CTS Tied To DTR | 4.3.5.3 |
| SW2-3 | 19200 | 100 | OFF(0) | Baud Rate Option | 4.3.5.4 |
| SW2-4 | Disable | Enable | OFF(0) | Expanded Silo | 4.3.5.5 |
| SW2-5 | - | - | OFF(0)* | Not Used | |
| SW2-6 | Disable | Enable | OFF(0) | Force 2 Stop Bits All Channels | 4.3.5.6 |
| SW2-7 | Disable | Enable | OFF(0) | 22-Bit Addressing Mode | 4.3.5.7 |
| SW2-8 | - | - | OFF(0)* | Not Used | |
| SW3-1 | - | - | NS | DH11 Vector Address | 4.3.4.1 |
| SW3-2 | - | - | NS | DH11 Vector Address | 4.3.4.1 |
| SW3-3 | - | - | NS | DH11 Vector Address | 4.3.4.1 |
| SW3-4 | - | - | NS | DH11 Vector Address | 4.3.4.1 |
| SW3-5 | - | - | NS | DH11 Vector Address | 4.3.4.1 |
| SW3-6 | - | - | OFF(0)* | Not Used | |
| SW3-7 | - | - | OFF(0)* | Not Used | |
| SW3-8 | - | - | OFF(0)* | Not Used | |
| SW4-1 | - | - | NS | DM11 Vector Address | 4.3.4.3 |
| SW4-2 | - | - | NS | DM11 Vector Address | 4.3.4.3 |
| SW4-3 | - | - | NS | DM11 Vector Address | 4.3.4.3 |
| SW4-4 | - | - | NS | DM11 Vector Address | 4.3.4.3 |
| SW4-5 | - | - | NS | DM11 Vector Address | 4.3.4.3 |
| SW4-6 | - | - | NS | DM11 Vector Address | 4.3.4.3 |
| SW4-7 | - | - | OFF(0)* | Not Used | |
| SW4-8 | - | - | OFF(0)* | Not Used | |
| SW5-1 | DHV11 | **DH11/DM11** | OFF(0) | **Emulation Selection** | 4.3.2 |
| SW5-2 | - | - | NS | DH11/DM11 Bus Address | 4.3.3.1 |
| SW5-3 | - | - | NS | DH11/DM11 Bus Address | 4.3.3.1 |
| SW5-4 | - | - | NS | DH11/DM11 Bus Address | 4.3.3.1 |
| SW5-5 | - | - | NS | DH11/DM11 Bus Address | 4.3.3.1 |
| SW5-6 | - | - | NS | DH11/DM11 Bus Address | 4.3.3.1 |
| SW5-7 | Monitor | Ignore | OFF(0) | Monitor Q-Bus DC Power OK Sgnl | 4.3.5.8 |
| SW5-8 | - | - | OFF(0)* | Not Used | |

OFF(0) = Open
ON(1) = Closed
* = Switch must be in factory setting
Fact = Factory switch setting
Int = Internal
NS = No Standard
Sgnl = Signal

Table 4-2. DHV11[1] CC02 Switch Definitions/Factory Configuration

| SW | OFF(0) | ON(1) | Fact | Function | Section |
|---|---|---|---|---|---|
| SW1-1 | Run | Halt/Reset | OFF(0) | Controller Run/Halt | 4.3.5.1 |
| SW1-2 | - | Int Test | OFF(0) | Internal Test Select | 4.3.5.2 |
| SW1-3 | - | Int Test | OFF(0) | Internal Test Select | 4.3.5.2 |
| SW1-4 | - | Int Test | OFF(0) | Internal Test Select | 4.3.5.2 |
| SW2-1 | - | - | OFF(0)* | Not Used | |
| SW2-2 | 4-15 | All | OFF(0) | CTS Tied To DTR | 4.3.5.3 |
| SW2-3 | - | - | OFF(0)* | Not Used | |
| SW2-4 | - | - | OFF(0)* | Not Used | |
| SW2-5 | - | - | OFF(0)* | Not Used | |
| SW2-6 | Disable | Enable | OFF(0) | Force 2 Stop Bits All Chnls | 4.3.5.6 |
| SW2-7 | - | - | OFF(0)* | Not Used | |
| SW2-8 | - | - | OFF(0)* | Not Used | |
| SW3-1 | - | - | NS | DHV11 Vector Address | 4.3.4.2 |
| SW3-2 | - | - | NS | DHV11 Vector Address | 4.3.4.2 |
| SW3-3 | - | - | NS | DHV11 Vector Address | 4.3.4.2 |
| SW3-4 | - | - | NS | DHV11 Vector Address | 4.3.4.2 |
| SW3-5 | - | - | NS | DHV11 Vector Address | 4.3.4.2 |
| SW3-6 | - | - | OFF(0)* | Not Used | |
| SW3-7 | - | - | OFF(0)* | Not Used | |
| SW3-8 | - | - | OFF(0)* | Not Used | |
| SW4-1 | - | - | OFF(0) | Level Flow Control | 4.3.5.10 |
| SW4-2 | - | - | OFF(0) | Level Flow Control | 4.3.5.10 |
| SW4-3 | - | - | OFF(0) | Level Flow Control | 4.3.5.10 |
| SW4-4 | Disable | Enable | OFF(0) | High Performance Option | 4.3.5.11 |
| SW4-5 | 2000 | 38400 | OFF(0) | 38400 Baud Option | 4.3.5.12 |
| SW4-6 | - | - | OFF(0)* | Not Used | |
| SW4-7 | - | - | OFF(0)* | Not Used | |
| SW4-8 | - | - | OFF(0)* | Not Used | |
| SW5-1 | **DHV11** | DH11/DM11 | OFF(0) | **Emulation Selection** | 4.3.2 |
| SW5-2 | - | - | NS | DHV11 Bus Address | 4.3.3.2 |
| SW5-3 | - | - | NS | DHV11 Bus Address | 4.3.3.2 |
| SW5-4 | - | - | NS | DHV11 Bus Address | 4.3.3.2 |
| SW5-5 | - | - | NS | DHV11 Bus Address | 4.3.3.2 |
| SW5-6 | - | - | NS | DHV11 Bus Address | 4.3.3.2 |
| SW5-7 | Monitor | Ignore | OFF(0) | Monitor Q-Bus DC Pwr OK Sgnl | 4.3.5.8 |
| SW5-8 | - | - | OFF(0)* | Not Used | |

OFF(0) = Open
ON(1) = Closed
* = Switch must be in factory setting
Fact = Factory switch setting
NS = No Standard
Pwr = Power
Sgnl = Signal

[1]DHV11 emulation requires 22-bit addressing. See section 4.3.5.7.

Table 4-3. CC02 Jumper Definition/Factory Configuration

| Jumper | Factory | Function |
|---|---|---|
| A to B | Out | Production Test Jumper |
| B to C | In | Connects microprocessor clock |
| D to E | Out | Production Test Jumper |

### 4.3.1 DIP HEADER CONFIGURATION

All CC02 Controller Module PCBAs with assembly number CU0210402 Rev B or above are shipped with a zero ohm pack installed in the socket located at U81. The zero ohm pack should be removed and replaced by a DIP header, which is shipped with the distribution panel. This DIP header determines whether or not power (+5V and -15V) is available at CC02 connectors J2 and J3 (the distribution panel interface). Power is not required to operate the CP22 or CP24 Distribution Panels; power is required to operate the CP25 Distribution Panel. Figure 4-2, below, shows the proper orientation of the DIP header for all of these distribution panels.

If the header is accidentally reversed (rotated 180°) and power is applied to the CC02 with the distribution panel attached, the fuses on the DIP header will blow. If this happens, replace the header with the spare supplied. Additional DIP headers can be ordered from Emulex, using part number CS2113001.

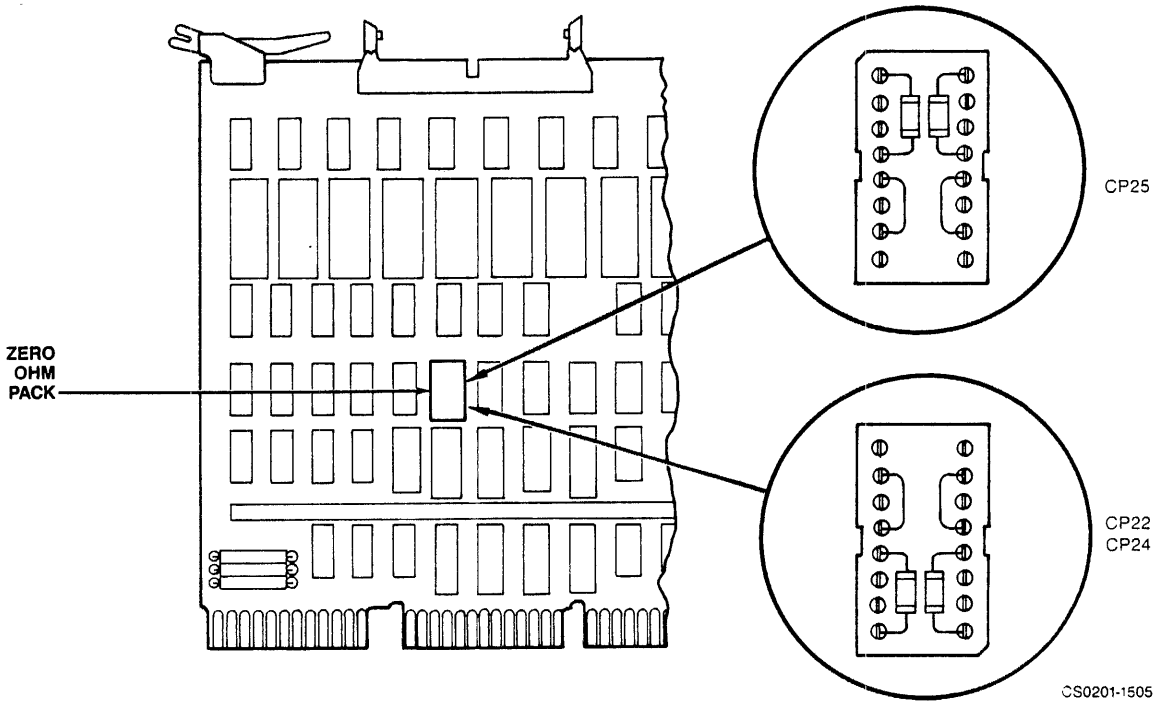



Figure 4-2. CC02 DIP Header Orientation

### 4.3.2 EMULATION SELECTION (SW5-1)

The CS02/H has the ability to emulate either a DEC DH11 with associated modem control, or two DEC DHV11s. The DH11 with DM11 is a 16-channel asynchronous multiplexer. The DHV11 is an eight-channel asynchronous multiplexer. Table 4-1 lists and defines the functions of the switches on the CC02 Controller Module for the DH11/DM11 emulation. Table 4-2 lists and defines the functions of the switches on the CC02 Controller Module for the DHV11 emulation. A single 16-channel DH11/DM11 emulation is enabled by setting switch SW5-1 closed/ON. Two eight-channel DHV11 emulations are enabled by setting switch SW5-1 open/OFF.

| Switch | Off | On | Factory |
|---|---|---|---|
| SW5-1 | DHV11 | DH11/DM11 | OFF |

### 4.3.3 CC02 DEVICE ADDRESS SELECTION (SW5-2:SW5-6)

DH11-type and DHV11-type devices are assigned Q-Bus addresses from the floating address section of the Q-Bus I/O page. If you are unfamiliar with the rules for assigning device addresses on the Q-Bus, see subsection 3.4.1 for the bus address determination procedure.

Two address PROMs are available for the CC02 (at location U124). Use Table 4-4 if you are using address PROM No. 997; use Table 4-4A if you are using the alternate address PROM No. D20.

When the emulation selection switch (SW5-1) is set to the DH11/DM11 setting, the DH11/DHV11 column in Table 4-4 is used for the DH11 bus address, and the DM11 column in Table 4-4 is used for the DM11 bus address. When the DHV11 emulation is selected, the DH11/DHV11 column is used for the DHV11 bus address, and the DM11 column can be ignored.

### 4.3.3.1 DH11/DM11 Device Register Addresses

When you have determined the proper address for the DH11 and DM11 registers, set CC02 Controller Module switches SW5-2 through SW5-6 according to Table 4-4 or 4-4A. The address specified is for the System Control Register of the DH11 emulation.

A block of addresses from $17770500_8$ to $17770676_8$ in the Q-Bus I/O page are reserved for DM11-type devices. The autoconfigure utilities of DEC operating systems recognize the DM11 if it is located anywhere within that range. The CS02/H has a DM11 for each DH11.

As is shown in Tables 4-4 and 4-4A, the starting address for any DM11 depends on the selection of the DH11 starting address. For example, if the DH11 address is $17760020_8$, the DM11 address is $17770500_8$.

Table 4-4. CS02/H Q-Bus Address Selection
PROM No. 997

| DH11/DHV11 Address (in octal) | DM11 Address (in octal) | SW5 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| 17760020 | 17770500 | 0 | 0 | 0 | 0 | 1 |
| 17760040 | 17770510 | 1 | 0 | 0 | 0 | 1 |
| 17760060 | 17770520 | 0 | 1 | 0 | 0 | 1 |
| 17760100 | 17770530 | 1 | 1 | 0 | 0 | 1 |
| 17760120 | 17770540 | 0 | 0 | 1 | 0 | 1 |
| 17760140 | 17770550 | 1 | 0 | 1 | 0 | 1 |
| 17760160 | 17770560 | 0 | 1 | 1 | 0 | 1 |
| 17760200 | 17770570 | 1 | 1 | 1 | 0 | 1 |
| 17760220 | 17770600 | 0 | 0 | 0 | 1 | 1 |
| 17760240 | 17770610 | 1 | 0 | 0 | 1 | 1 |
| 17760260 | 17770620 | 0 | 1 | 0 | 1 | 1 |
| 17760300 | 17770630 | 1 | 1 | 0 | 1 | 1 |
| 17760320 | 17770640 | 0 | 0 | 1 | 1 | 1 |
| 17760340 | 17770650 | 1 | 0 | 0 | 0 | 0 |
| 17760360 | 17770660 | 0 | 1 | 0 | 0 | 0 |
| 17760400 | 17770670 | 1 | 1 | 0 | 0 | 0 |
| 17760420 | 17770700 | 0 | 0 | 1 | 0 | 0 |
| 17760440 | 17770710 | 1 | 0 | 1 | 0 | 0 |
| 17760460 | 17770720 | 0 | 1 | 1 | 0 | 0 |
| 17760500 | 17770730 | 1 | 1 | 1 | 0 | 0 |
| 17760520 | 17770740 | 0 | 0 | 0 | 1 | 0 |
| 17760540 | 17770750 | 1 | 0 | 0 | 1 | 0 |
| 17760560 | 17770760 | 0 | 1 | 0 | 1 | 0 |
| 17760600 | 17770770 | 1 | 1 | 0 | 1 | 0 |
| 17760620 | 17771000 | 0 | 0 | 1 | 1 | 0 |

0 = open/OFF
1 = closed/ON

Table 4-4A. CS02/H Q-Bus Address Selection
PROM No. D20

| DH11/DHV11 Address (in octal) | DM11 Address (in octal) | ------ SW5 ------ 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| 17760420 | 17770700 | 0 | 0 | 0 | 0 | 1 |
| 17760440 | 17770710 | 1 | 0 | 0 | 0 | 1 |
| 17760460 | 17770740 | 0 | 1 | 0 | 0 | 1 |
| 17760500 | 17770730 | 1 | 1 | 0 | 0 | 1 |
| 17760520 | 17770740 | 0 | 0 | 1 | 0 | 1 |
| 17760540 | 17770550 | 1 | 0 | 1 | 0 | 1 |
| 17760560 | 17770760 | 0 | 1 | 1 | 0 | 1 |
| 17760600 | 17770770 | 1 | 1 | 1 | 0 | 1 |
| 17760620 | 17771000 | 0 | 0 | 0 | 1 | 1 |
| 17760640 | 17771010 | 1 | 0 | 0 | 1 | 1 |
| 17760660 | 17771020 | 0 | 1 | 0 | 1 | 1 |
| 17760700 | 17771030 | 1 | 1 | 0 | 1 | 1 |
| 17760720 | 17771040 | 0 | 0 | 1 | 1 | 1 |
| 17760740 | 17771050 | 1 | 0 | 0 | 0 | 0 |
| 17760760 | 17771060 | 0 | 1 | 0 | 0 | 0 |
| 17761000 | 17771070 | 1 | 1 | 0 | 0 | 0 |
| 17761020 | 17771100 | 0 | 0 | 1 | 0 | 0 |
| 17761040 | 17771110 | 1 | 0 | 1 | 0 | 0 |
| 17761060 | 17771120 | 0 | 1 | 1 | 0 | 0 |
| 17761100 | 17771130 | 1 | 1 | 1 | 0 | 0 |
| 17761120 | 17771140 | 0 | 0 | 0 | 1 | 0 |
| 17761140 | 17771150 | 1 | 0 | 0 | 1 | 0 |
| 17761160 | 17771160 | 0 | 1 | 0 | 1 | 0 |
| 17761200 | 17771170 | 1 | 1 | 0 | 1 | 0 |
| 17761220 | 17771200 | 0 | 0 | 1 | 1 | 0 |

0 = open/OFF
1 = closed/ON

Example 4-1. One DH11 with associated DM11 modem control unit. Address of DH11 emulation set to $17760260_8$ using SW5.

| Address | | ------ SW5 ------ | | | | |
|---|---|---|---|---|---|---|
| DH11 | DM11 | 2 | 3 | 4 | 5 | 6 |
| $17760260_8$ | $17770620_8$ | 0 | 1 | 0 | 1 | 1 |
| 0 = open/OFF 1 = closed/ON | | | | | | |

#### 4.3.3.2 DHV11 Device Register Address

When you have determined the proper DHV11 register address, set CC02 Controller Module switches SW5-2 through SW5-6 according to Table 4-4. The address specified is for the Control Status Register.

There is no DM11 emulation associated with the DHV11.

Example 4-2. Two DHV11 emulations. Address of first DHV11 emulation set to $17760260_8$ using SW5.

| Emulation Number | DHV11 Address | SW5 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| 1 | $17760260_8$ | 0 | 1 | 0 | 1 | 1 |
| 2 | $17760300_8$ | | | | | |
| 0 = open/OFF 1 = closed/ON | | | | | | |

### 4.3.4 CC02 INTERRUPT VECTOR ADDRESSES (SW3-1:SW3-5,SW4-1:SW4-6)

A floating vector convention is used to select vectors for DH11, DHV11 and DM11 type devices. These vector addresses are assigned from the floating vector block that starts at address $300_8$ and proceeds upwards to $777_8$. See Section 3 for a detailed description of the vector selection algorithm.

When the emulation selection switch (SW5-1) is set to the DH11/DM11 setting, use Table 4-5 to determine the switch settings for the vector address of the DH11 emulation, and use Table 4-6 to determine the switch settings for the vector address of the DM11 emulation. When the emulation selection is set to the DHV11 setting, use Table 4-5 to determine the switch settings for the vector address of the DHV11 emulation, and the switches described in Table 4-6 are not used.

#### 4.3.4.1 DH11 Vector Addresses

The DH11 emulation requires two interrupt vector addresses, one for the receive function and one for the transmit function. The receive vector is first, and it is always on a modulo-10 boundary (XX0). It is followed consecutively by the transmit vector on a modulo-four boundary (XX4). The DH11 interrupt vector addresses are set using five switches as specified in Table 4-5. Only the receive vector is selected using Table 4-5. The transmit vector follows the receive vector, and is automatically assigned by the firmware.

Table 4-5. DH11/DHV11 Vector Address Selection

| Octal Address | SW3 1 | 2 | 3 | 4 | 5 | Octal Address | SW3 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 300 | 0 | 0 | 0 | 0 | 0 | 500 | 0 | 0 | 0 | 0 | 1 |
| 310 | 1 | 0 | 0 | 0 | 0 | 510 | 1 | 0 | 0 | 0 | 1 |
| 320 | 0 | 1 | 0 | 0 | 0 | 520 | 0 | 1 | 0 | 0 | 1 |
| 330 | 1 | 1 | 0 | 0 | 0 | 530 | 1 | 1 | 0 | 0 | 1 |
| 340 | 0 | 0 | 1 | 0 | 0 | 540 | 0 | 0 | 1 | 0 | 1 |
| 350 | 1 | 0 | 1 | 0 | 0 | 550 | 1 | 0 | 1 | 0 | 1 |
| 360 | 0 | 1 | 1 | 0 | 0 | 560 | 0 | 1 | 1 | 0 | 1 |
| 370 | 1 | 1 | 1 | 0 | 0 | 570 | 1 | 1 | 1 | 0 | 1 |
| 400 | 0 | 0 | 0 | 1 | 0 | 600 | 0 | 0 | 0 | 1 | 1 |
| 410 | 1 | 0 | 0 | 1 | 0 | 610 | 1 | 0 | 0 | 1 | 1 |
| 420 | 0 | 1 | 0 | 1 | 0 | 620 | 0 | 1 | 0 | 1 | 1 |
| 430 | 1 | 1 | 0 | 1 | 0 | 630 | 1 | 1 | 0 | 1 | 1 |
| 440 | 0 | 0 | 1 | 1 | 0 | 640 | 0 | 0 | 1 | 1 | 1 |
| 450 | 1 | 0 | 1 | 1 | 0 | 650 | 1 | 0 | 1 | 1 | 1 |
| 460 | 0 | 1 | 1 | 1 | 0 | 660 | 0 | 1 | 1 | 1 | 1 |
| 470 | 1 | 1 | 1 | 1 | 0 | 670 | 1 | 1 | 1 | 1 | 1 |

0 = open/OFF
1 = closed/ON

Example 4-3. A DH11 with associated DM11 modem control unit. Using Table 4-5, switch SW3 is set to select a receive vector address of $340_8$. The transmit vector is $344_8$.

| | DH11 Vector | SW3 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|
| Receive | $340_8$ | 0 | 0 | 1 | 0 | 0 |
| Transmit | $344_8$ | | | | | |

0 = open/OFF 1 = closed/ON

4.3.4.2 DHV11 Vector Addresses

Each DHV11 emulation requires two interrupt vector addresses, one for the receive function and one for the transmit function. The receive vector is first, and it is always on a modulo-10 boundary (XX0). It is followed consecutively by the transmit vector on a modulo-four boundary (XX4). The DHV11 interrupt vector addresses are set using five switches as specified in Table 4-5. Only the receive vector of the first emulation is selected using Table 4-5. The transmit vector follows the receive vector, and is automatically assigned by the

firmware. The interrupt vectors for the second emulation follow the transmit and receive vectors for the first emulation.

Example 4-4. Two DHV11 emulations. Using Table 4-5, switch SW3 is set to select a receive vector address of $340_8$ for the first DHV11.

| | DHV11 Emulation Number | DHV11 Vector | SW3 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|---|
| Receive | 1 | $340_8$ | 0 | 0 | 1 | 0 | 0 |
| Transmit | | $344_8$ | | | | | |
| Receive | 2 | $350_8$ | | | | | |
| Transmit | | $354_8$ | | | | | |
| 0 = open/OFF 1 = closed/ON | | | | | | | |

4.3.4.3 DM11 Vector

Each DM11 requires one interrupt vector on a modulo-four boundary. The DM11 interrupt vector address is set as specified in Table 4-6.

**NOTE**

If the system configuration requires the DH11 vector address to be assigned directly prior to (numerically) the DM11 vector, the DM11 vector must be assigned to an address $10_8$ greater than the DH11 vector. This is because the DH11 requires two vectors per emulation.

Example 4-5. A DH11 with associated DM11 modem control unit. Using Table 4-6, switch SW4 is set to equal a starting DM11 vector address of $310_8$.

| DM11 Vector | SW4 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| $310_8$ | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 = open/OFF 1 = closed/ON | | | | | | |

Table 4-6. DM11 Vector Address Selection

| Octal Address | SW4 1 | 2 | 3 | 4 | 5 | 6 | Octal Address | SW4 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 300 | 0 | 0 | 0 | 0 | 0 | 0 | 500 | 0 | 0 | 0 | 0 | 0 | 1 |
| 304 | 1 | 0 | 0 | 0 | 0 | 0 | 504 | 1 | 0 | 0 | 0 | 0 | 1 |
| 310 | 0 | 1 | 0 | 0 | 0 | 0 | 510 | 0 | 1 | 0 | 0 | 0 | 1 |
| 314 | 1 | 1 | 0 | 0 | 0 | 0 | 514 | 1 | 1 | 0 | 0 | 0 | 1 |
| 320 | 0 | 0 | 1 | 0 | 0 | 0 | 520 | 0 | 0 | 1 | 0 | 0 | 1 |
| 324 | 1 | 0 | 1 | 0 | 0 | 0 | 524 | 1 | 0 | 1 | 0 | 0 | 1 |
| 330 | 0 | 1 | 1 | 0 | 0 | 0 | 530 | 0 | 1 | 1 | 0 | 0 | 1 |
| 334 | 1 | 1 | 1 | 0 | 0 | 0 | 534 | 1 | 1 | 1 | 0 | 0 | 1 |
| 340 | 0 | 0 | 0 | 1 | 0 | 0 | 540 | 0 | 0 | 0 | 1 | 0 | 1 |
| 344 | 1 | 0 | 0 | 1 | 0 | 0 | 544 | 1 | 0 | 0 | 1 | 0 | 1 |
| 350 | 0 | 1 | 0 | 1 | 0 | 0 | 550 | 0 | 1 | 0 | 1 | 0 | 1 |
| 354 | 1 | 1 | 0 | 1 | 0 | 0 | 554 | 1 | 1 | 0 | 1 | 0 | 1 |
| 360 | 0 | 0 | 1 | 1 | 0 | 0 | 560 | 0 | 0 | 1 | 1 | 0 | 1 |
| 364 | 1 | 0 | 1 | 1 | 0 | 0 | 564 | 1 | 0 | 1 | 1 | 0 | 1 |
| 370 | 0 | 1 | 1 | 1 | 0 | 0 | 570 | 0 | 1 | 1 | 1 | 0 | 1 |
| 374 | 1 | 1 | 1 | 1 | 0 | 0 | 574 | 1 | 1 | 1 | 1 | 0 | 1 |
| 400 | 0 | 0 | 0 | 0 | 1 | 0 | 600 | 0 | 0 | 0 | 0 | 1 | 1 |
| 404 | 1 | 0 | 0 | 0 | 1 | 0 | 604 | 1 | 0 | 0 | 0 | 1 | 1 |
| 410 | 0 | 1 | 0 | 0 | 1 | 0 | 610 | 0 | 1 | 0 | 0 | 1 | 1 |
| 414 | 1 | 1 | 0 | 0 | 1 | 0 | 614 | 1 | 1 | 0 | 0 | 1 | 1 |
| 420 | 0 | 0 | 1 | 0 | 1 | 0 | 620 | 0 | 0 | 1 | 0 | 1 | 1 |
| 424 | 1 | 0 | 1 | 0 | 1 | 0 | 624 | 1 | 0 | 1 | 0 | 1 | 1 |
| 430 | 0 | 1 | 1 | 0 | 1 | 0 | 630 | 0 | 1 | 1 | 0 | 1 | 1 |
| 434 | 1 | 1 | 1 | 0 | 1 | 0 | 634 | 1 | 1 | 1 | 0 | 1 | 1 |
| 440 | 0 | 0 | 0 | 1 | 1 | 0 | 640 | 0 | 0 | 0 | 1 | 1 | 1 |
| 444 | 1 | 0 | 0 | 1 | 1 | 0 | 644 | 1 | 0 | 0 | 1 | 1 | 1 |
| 450 | 0 | 1 | 0 | 1 | 1 | 0 | 650 | 0 | 1 | 0 | 1 | 1 | 1 |
| 454 | 1 | 1 | 0 | 1 | 1 | 0 | 654 | 1 | 1 | 0 | 1 | 1 | 1 |
| 460 | 0 | 0 | 1 | 1 | 1 | 0 | 660 | 0 | 0 | 1 | 1 | 1 | 1 |
| 464 | 1 | 0 | 1 | 1 | 1 | 0 | 664 | 1 | 0 | 1 | 1 | 1 | 1 |
| 470 | 0 | 1 | 1 | 1 | 1 | 0 | 670 | 0 | 1 | 1 | 1 | 1 | 1 |
| 474 | 1 | 1 | 1 | 1 | 1 | 0 | 674 | 1 | 1 | 1 | 1 | 1 | 1 |

0 = open/OFF
1 = closed/ON

### 4.3.5 OPTIONS

Other switches are used to select various options. This subsection explains those switch functions and options.

#### 4.3.5.1 CC02 Run/Halt/Reset Switch (SW1-1)

When placed in the ON (closed) position, switch SW1-1 locks the CC02's microprocessor in a reset condition. Upon placing the switch back in the OFF (open) position, the CC02 Controller Module executes its initialization routine and comes on-line.

| Switch | OFF | ON | Factory |
|---|---|---|---|
| SW1-1 | Normal | Halt/Reset | OFF |

#### 4.3.5.2 CC02 Internal Test Select (SW1-2:SW1-4)

Switches SW1-2 through SW1-4 select one of four internal micro tests. The available selections are briefly described in Table 4-7 (see Section 6 for further details). To activate these tests, set the switches to the desired mode, then toggle the Reset switch (SW1-1).

**NOTE**

Switches SW1-2 through SW1-4 must be OFF (open) for normal operation of the controller. Test modes three and four (see Table 4-7) are used for off-line testing only.

#### 4.3.5.3 CC02 Tie CTS To DTR (SW2-2)

This option is available only with Revision F or higher firmware. Normally, since the Clear To Send modem signal is not supported on the CS02, the CTS signal is faked by tying it to the Data Terminal Ready signal on all lines. However, newer CP22 Distribution Panels (those with three connectors on the back) support CTS on channels 0 through 3. By setting switch SW2-2 OFF, the CTS signal is only tied to DTR on channels 4 through 15. This allows independent control of CTS by software on channels 0 through 3. When SW2-2 is ON, CTS is tied to DTR on all lines.

| Switch | OFF | ON | Factory |
|---|---|---|---|
| SW2-2 | Channels 4-15 | All Channels | OFF |

Table 4-7. CC02 Internal Micro Test

| Test Mode | Test Mode Description | --SW1-- 2 | 3 | 4 |
|---|---|---|---|---|
| 1 | Normal Run Mode - Fault LED blinks if any channel fails internal loopback test. | 0 | 0 | 0 |
| 2 | Override Mode - Fault LED blinks only if no channels pass internal loopback test. Controller will run with lines that pass. | 0 | 0 | 1 |
| 3 | Continuous External Loopback Mode - Fault LED blinks if any error is detected on any channel. | 0 | 1 | 0 |
| 4 | Search Mode - Fault LED goes off if at least one channel is good. If no channels are good, the Fault LED blinks. | 0 | 1 | 1 |
| 5 | Echo Mode - Characters received from any terminal will be echoed. Revision E and above firmware only. | 1 | 0 | 0 |
| 0 = open/OFF 1 = closed/ON | | | | |

4.3.5.4 DH11 Baud Rate Option (SW2-3)

This switch determines the baud rate selected for a channel when the code '1110' is selected in the Line Parameter Register. (See Table 7-1.) When switch SW2-3 is set to the OFF (open) position, the transmit and receive baud rate selected by this code is 19200 bps. When switch SW2-3 is set to the ON (closed) position the transmit and receive baud rate selected by this code is 100 bps.

| Switch | OFF | ON | Factory |
|---|---|---|---|
| SW2-3 | 19200 | 100 | OFF |

4.3.5.5 DH11 Expanded Silo (SW2-4)

Selecting this option causes the 64-character receive silo to expand to a 256-character silo. The silo is expanded by setting switch SW2-4 ON (closed).

| Switch | OFF | ON | Factory |
|---|---|---|---|
| SW2-4 | Disable | Enable | OFF |

#### 4.3.5.6 CC02 Force Two Stop Bits (SW2-6)

This option overrides program control of the number of stop bits per character. When this option is selected, all channels will transmit two stop bits with every character. This option is useful in situations where a continuous stream of asynchronous characters are being transmitted and the transmit station's data rate is slightly faster than the receive station's data rate. In some cases one stop bit between characters does not allow enough time for the receiving DUART to synchronize on the start bit which immediately follows the single stop bit. Two stop bits simply allow more time between characters to ensure that the receiving DUART has enough time to internally set up to sense the next start bit.

| Switch | OFF | ON | Factory |
|---|---|---|---|
| SW2-6 | Disable | Enable | OFF |

#### 4.3.5.7 DH11 22-Bit Addressing Mode (SW2-7)

Because the DH11 register definition (see Section 7) allows a maximum of 18 bits of addressing, it is necessary to provide a means for operation on computers which support a 22-bit address. Selecting this option allows the DH11 emulation to run on a 22-bit address system by redefining some of the register definitions for the standard DH11. The details of these changes are contained in the Register and Programming Section (Section 7) of this manual. Essentially, the changes allow the specification of a 22-bit memory address for DMA operations instead of the normal 18-bit address.

| Switch | OFF | ON | Factory |
|---|---|---|---|
| SW2-7 | Disable | Enable | OFF |

In addition to setting switch SW2-7, an IC must be inserted on the CC02 Controller Module to enable DH11 22-bit addressing. A CC02 Extended Address Option Kit (Emulex part number CS0113001)

accompanies the CC02 Controller Module. Included in this kit is an integrated circuit (IC). This IC must be inserted in the socket at location U151 on the CC02 Controller Module.

**CAUTION**

Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing the CC02 Controller Module with the Extended Address IC **will** damage the option IC. Before installing the option confirm that there is neither positive or negative potential between lines BC1, BD1, BE1, BF1 and logic ground. A CC02 without the Extended Address IC installed will not be damaged if power is present on those lines.

#### 4.3.5.8 Monitor Q-Bus DC Power OK Signal (SW5-7)

When placed in the ON (closed) position, switch SW5-7 causes the controller to inhibit monitoring of the Q-Bus 'DC Power O.K.' signal. When SW5-7 is OFF (open), the controller will reset when the Q-Bus 'DC Power O.K.' signal is not present.

| Switch | OFF | ON | Factory |
|---|---|---|---|
| SW5-7 | Monitor | Ignore | ON |

#### 4.3.5.9 DH11 Clear To Send Flow Control

Channels zero through three support a Clear to Send (CTS) input signal on pin five of the 25-pin subminiature D-type connector. (The nine-pin connectors on the CP24 do not carry this signal). When switch SW2-1 is OFF (open), the CTS signal is ignored by the CC02 firmware. When switch SW2-1 is ON (closed) and the CTS signal is inactive, the firmware will suspend transmission of characters on that line. The line will transmit characters only when the CTS line is active.

| Switch | OFF | ON | Factory |
|---|---|---|---|
| SW2-1 | Disable | Enable | OFF |

### 4.3.5.10 DHV11 Level Flow Control Option

This option is available only with Revision H or higher firmware. When the level flow control option is enabled, the CS02/H controls transmitted data flow by monitoring the Carrier input at the distribution panel. When Carrier is negated, the CS02/H generates an XOFF character, halting transmission of data. When Carrier is asserted, the CS02/H generates an XON character, reenabling transmission. This feature is normally implemented by cabling the DTR line of the terminal to the Carrier input of the distribution panel. Thus, when the terminal drops DTR, the CS03 halts data transmission.

Keep the following things in mind if you enable this option:

- This option works on transmitted data only. It cannot be used to halt the received data flow.
- Lines enabled for this option will not report modem status changes (Carrier, DSR, CTS) to the host operating system. Modem control signals (DTR, RTS) are not affected.
- Standard DHV11 auto input/output XON/XOFF flow control will be ignored on lines with this option enabled.

The level flow control option can be enabled on lines 9 through 15 by setting switches SW4-1 through SW4-3. Table 4-8 shows the switch settings.

**NOTE**

The level flow control option switches must all be OFF to run the DEC DHV11 diagnostics.

Table 4-8. Level Flow Control Switch Settings

| -SW4- 1 | 2 | 3 | Lines Enabled |
|---|---|---|---|
| 0 | 0 | 0 | No lines enabled |
| 1 | 0 | 0 | Line 15 enabled |
| 0 | 1 | 0 | Lines 14 through 15 enabled |
| 1 | 1 | 0 | Lines 13 through 15 enabled |
| 0 | 0 | 1 | Lines 12 through 15 enabled |
| 1 | 0 | 1 | Lines 11 through 15 enabled |
| 0 | 1 | 1 | Lines 10 through 15 enabled |
| 1 | 1 | 1 | Lines 9 through 15 enabled |

#### 4.3.5.11 DHV11 High Performance Throughput Option

This option is available only with Revision H or higher firmware. In previous releases of the CS02/H, the transmit character throughput in programmed I/O mode (PIO) was reduced considerably in order to retain compatability with the DEC DHV11 diagnostics. Setting switch SW4-4 ON eliminates the throughput reduction and allows the CS02/H to run much faster than the DEC DHV11.

The increase in PIO transmit speed may not be detectable under normal operating system conditions due to the inability of the DHV11 driver to immediately service the transmit PIO interrupt. However, if a simple benchmark program were designed capable of transmitting a continuous PIO data stream to two terminals, one on the CS02/H and the other on the DEC DHV11, one would see a remarkable difference in throughput simply by watching the two terminals.

**NOTE**

Switch SW4-4 must be OFF to run the DEC DHV11 diagnostics.

| Switch | OFF | ON | Factory |
|---|---|---|---|
| SW4-4 | Disable | Enable | OFF |

#### 4.3.5.12 DHV11 38400 Baud Option

This option is available only with Revision H or higher firmware. It allows you to run at 38400 baud on a MicroVAX even though the DHV11 driver on the MicroVAX does not support operation at this speed. The CS02/H allows you to run at 38400 baud on a MicroVAX if you do three things:

- Set switch SW4-5 ON.
- Configure the operating system for 2000 baud. If switch SW4-5 is ON, any line configured for 2000 baud will operate instead at 38400 baud.
- Set your terminal(s) for 38400 baud.

**NOTE**

Switch SW4-5 must be OFF to run the DEC DHV11 diagnostics.

| Switch | OFF | ON | Factory |
|---|---|---|---|
| SW4-5 | 2000 | 38400 | OFF |

## 4.4 DISTRIBUTION PANEL SETUP

Before you begin the installation of the CS02/H subsystem, you may need to set certain jumpers on the distribution panel. See the setup section of you distribution panel technical manual for details.

When you are finished setting up the panel, return to this manual for instructions on installing the CC02 in the Q-Bus backplane.

## 4.5 INSTALLATION OF THE CC02 IN AN LSI-11

### 4.5.1 SYSTEM PREPARATION

Power down the system and switch OFF the main AC breaker. Remove the side covers from the CPU cabinet and otherwise make the Q-Bus accessible.

**NOTE**

If you are using a CP23 distribution panel (20 mA current loop) with the CS02/H, you must modify your backplane so that -15 VDC is supplied on Q-Bus lines AB2 and BB2. This is a nonstandard backplane configuration and should only be implemented by a qualified technician.

### 4.5.2 CONTROLLER INSTALLATION

The CC02 Controller Module can be inserted into any backplane slot in the DEC LSI-11 computer chassis. The closer a module is to the CPU, the higher its interrupt priority. As a general rule, the CC02 Controller Module should be placed in front of mass storage peripherals which have large buffers, and behind small disk and tape controllers which have little buffering. There should be no open slots between the CPU module and the last device on the bus.

The controller PCBA must be plugged into the backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the PCBA with the computer power OFF to avoid possible damage to the circuitry. Be sure that the PCBA is properly seated in the throat of the connector before attempting to seat the PCBA by means of the extractor handles.

### 4.5.3 DISTRIBUTION PANEL INSTALLATION AND CABLING

The CP22, CP23, and CP25 distribution panels are designed to mount on the rear RETMA rails of the CPU cabinet or an expansion cabinet, or directly in a DMF32 cutout in the rear of DMF32-compatible CPUs. Mounting and cabling instructions for these distribution panels are covered in their respective technical manuals. When you are finished mounting and cabling the distribution panel, turn to subsection 4.7 of this manual (Subsystem Power-Up and Verification) to complete the installation.

## 4.6 INSTALLATION OF THE CC02 IN A MICRO/PDP-11 OR MICROVAX

This subsection describes the procedure for mounting and cabling the CC02 Controller Module, in a Micro/PDP-11 or MicroVAX. The CS02/H subsystem may be mounted in the tabletop, floor-mount or rack-mount DEC Micro/PDP-11 or MicroVAX. The following steps form a procedure for the CS02/H subsystem installation.

1. Turn off the system power (using the front panel switch) and unplug the AC power cord from the wall.

2. Remove the rear plastic cover of the Micro/PDP/VAX to expose the system I/O panel. (The rack-mount version does not have a rear cover.)

3. Using a blade screwdriver, loosen the captive screws that retain the patch and filter panel mounted in the system I/O panel. Figure 4-3 depicts the patch and filter panel. Lift the panel slightly, and pull it out, leaving the cables connected.

4. Pull the M8639 board (RQDX1) out of the backplane without disconnecting its cable.

5. The M8639 must occupy the last slot in the backplane.

   a. For the floor-mount version, insert the M8639 board one position (slot) to the left of the slot from which it was removed.

   b. For the tabletop or rack-mount version, insert the M8639 board one position (slot) below the slot from which it was removed.

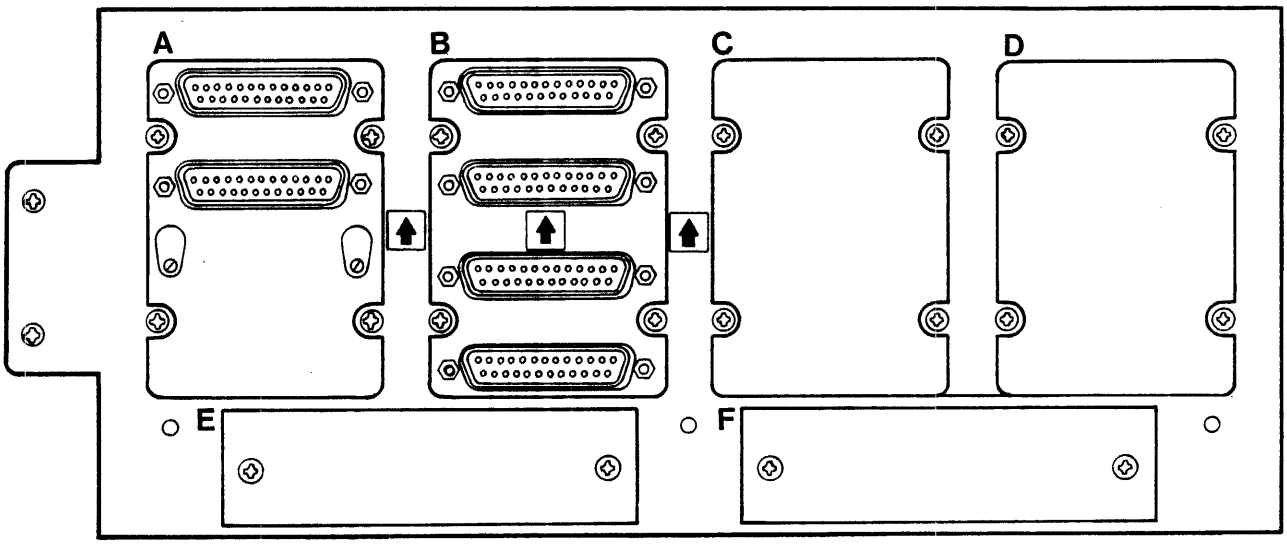



Figure 4-3. Micro/PDP/VAX Patch and Filter Panel Assembly

6. Insert the CC02 Controller Module in the slot from which the M8639 was removed, with the components oriented in the same direction as the CPU and other modules in the backplane.

7. The controller module is now installed. To complete the installation, you must refer to the installation section of the CP24 manual, which describes how to mount the CP24 and CP24/B and cable them to the controller module. When you are finished with the cabling, reattach the patch panel, using the screws you removed earlier. Then return to subsection 4.7 of this manual to complete the installation.

## 4.7 SUBSYSTEM POWER-UP AND VERIFICATION

When you have finished configuring and installing your CS02/H Communications Subsystem, you need to confirm that it is indeed installed and functioning properly. This subsection is designed to help you to verify proper subsystem operation quickly and efficiently. The verification procedure is outlined below:

1. Power-up the subsystem and observe self-test results

2. Test the CC02 Controller Module

3. Test each distribution panel.

If each of the tests described in this subsection are passed successfully, then you can be confident that the subsystem is ready to use.

No troubleshooting procedures are included in this subsection. If one of the tests described here fails, see Section 6, Troubleshooting, for a detailed fault isolation procedure.

### 4.7.1 CC02 CONTROLLER MODULE VERIFICATION

Switches SW1-3 and SW1-4 are assumed to be OFF before the CPU and controller are initially powered up.

The CC02 Controller Module performs a self-test on power-up or when reset. The results of this self-test is indicated using LEDs located at the edge of the CC02 Controller Module. A successful completion of the power-up self-test will be indicated by the green On-Line LED being ON, and by the two red LEDs being OFF.

When power is applied to the CPU, or when SW1-1 on the edge of the CC02 Controller Module is turned ON and then OFF again (close/open), the controller automatically executes a built-in self-test. The test is not executed with every Bus INIT, but only on power-up (i.e., DCLO) or reset of the CC02 Controller Module.

As power is applied to the system, watch the Fault LED located at the edge of the controller module. Of the three LEDs which are visible, the Fault LED is the center one and is red. Normally, the Fault LED flashes ON momentarily when power is first applied and then goes out. After the red Fault LED goes out, the green On-Line LED should come on. This sequence indicates that the controller module itself is operational.

If the Fault LED stays ON, or continues to FLASH, see Section 6 for fault isolation instructions.

### 4.7.2 PANEL VERIFICATION

Operater-initiated self-diagnostics can be used to verify the channels on the distribution panel(s). See subsection 6.4 for instructions on initiating the self-diagnostics.

### 4.7.3 DIAGNOSTICS

Emulex offers diagnostics for both the DH11 and DHV11 emulation of the CS02/H. Instructions for running them are in the **PDP-11/LSI-11 Diagnostic Distribution Kit for All Products** (part number PD9951801).

The CS02/H can also run the DEC diagnostics. Instructions for running the DEC ZDHMD0 DH11 diagnostic on an LSI-11 CPU can be found in Appendix B. Instructions for running the DHV11 diagnostics can be found in Appendix C.

Section 5
OPERATOR SWITCHES AND INDICATORS

## 5.1 OVERVIEW

This section describes the operating switches and indicators of the CS02/H Communication Subsystem. Excluding this overview, the section is divided into two main subsections.

| Subsection | Title |
|---|---|
| 5.1 | Overview |
| 5.2 | CC02 Controller Module Switches and Displays |
| 5.3 | Distribution Panels Switches and Displays |

## 5.2 CC02 CONTROLLER MODULE SWITCHES AND DISPLAYS

The CC02 Controller Module PCBA has several switches located in DIPs. All but four of these switches are used only when initially configuring the subsystem and have no use during normal operation.

There are also three indicator LEDs located on the PCBA. SW1 and the LEDs are shown in Figure 5-1.

### 5.2.1 SWITCHES

Of the several DIP switch packs located on the CC02 Controller Module, only one is accessible when the controller is installed in a Q-Bus chassis. That four-switch piano-type DIP is designated SW1, and is located on the outside edge of the controller PCBA.

The HALT/RESET switch, SW1-1, halts the controller's microprocessor and re-initializes its internal program counter and logic when closed (DOWN). When opened (UP), the microprocessor runs normally after executing its self-test and initialization routines.

Switch SW1-2 is not used, and SW1-3 and SW1-4 are used to select self-diagnostic modes (see subsection 6.4).

### 5.2.2 DISPLAYS

The three LEDs are labeled Activity, Fault and On-Line. When viewing the CC02 Controller Module from the edge, with the components facing up, the On-Line LED is on the right, and the Active LED is on the left. The LED functions are set up so that once power is provided to

the CS02/H, either the On-Line LED or the Fault LED will be ON. The LED's funtions are as follows:

On-Line LED

This green LED indicates that the CS02/H Communication Subsystem is on-line. This LED will be OFF when switch SW1-1 is ON (closed).

Fault LED

When the microprocessor is running its self-test, this red LED serves as a fault indicator. The fault indications are explained in subsection 6.4. This LED will be ON when switch SW1-1 is ON (closed). The controller cannot be addressed while this LED is ON.

Active LED

This red LED serves as an activity indicator. Thus, it flickers or glows dimly, depending on the level of controller activity.

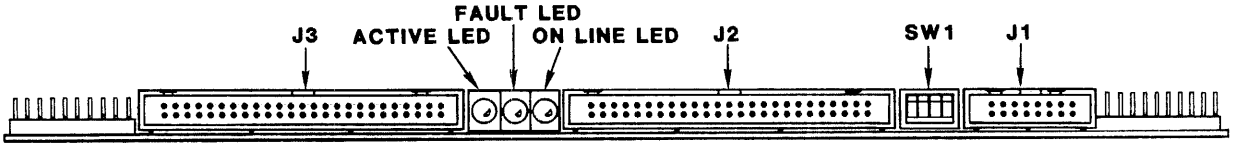



Figure 5-1. CC02 Controller Module Operator Controls and Indicators

## 5.3 DISTRIBUTION PANEL SWITCHES AND DISPLAYS

There are no switches or LEDs on any of the distribution panels which are a part of the CS02/H Communications Subsystem.

## 6.1 OVERVIEW

This section describes the several diagnostic features with which the CS02/H is equipped, and outlines fault isolation procedures that use these diagnostic features.

| Subsection | Title |
|---|---|
| 6.1 | Overview |
| 6.2 | Fault Isolation Procedures |
| 6.3 | Power-Up Self-Tests |
| 6.4 | CC02 Operator Initiated Self-Diagnostics |

### 6.1.1 SERVICE

The components of your Emulex CS02/H Communications Subsystem have been designed to give years of trouble-free service, and they were thoroughly tested before leaving the factory.

Should one of these fault isolation procedures indicate that a component is not working properly, the component must be returned to the factory or one of Emulex's authorized repair centers for service. Emulex products are not designed to be repaired in the field.

Before returning the component to Emulex, whether the product is under warranty or not, you must contact the factory or the factory's representative for instructions and a Return Materials Authorization (RMA) number.

**DO NOT RETURN A COMPONENT TO EMULEX WITHOUT AUTHORIZATION.** A component returned for service without an authorization will be returned to the owner at the owner's expense.

In the continental United States, Alaska, and Hawaii contact:

Emulex Technical Support
3545 Harbor Boulevard
Costa Mesa, CA 92626
(714)662-5600 TWX 910-595-2521

Outside of the United States, contact the distributer from whom the subsystem was initially purchased.

To help you efficiently, Emulex or its representative requires certain information about our product and the environment in which it is installed. Figure 6-1 on the facing page contains a list of the information required and shows where the information can be found.

After you have contacted Emulex and received an RMA, package the component (preferably using the original packing material) and send the the component **POSTAGE PAID** to the address given you by the Emulex representative. The sender must also insure the package.

### 6.1.2 TEST CONNECTOR

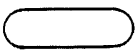
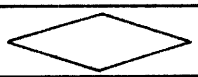
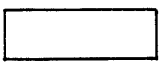
The external loop tests described in subsections 6.4.3 and 6.4.4 require a wrap-around connector. One connector or a full set of 16 can be ordered from Emulex. You may build your own test connector for any of the Emulex distribution panels by strapping a DB25S connector (for the CP22, CP24/B, or CP25) or a DE09S connector (for the CP24). The type of wrap-around depends on the emulation you have chosen for the CS02/H, the type of interface (RS-232 or RS-422), and the model of distribution panel. Instructions for building wrap-arounds are contained in the distribution panel technical manuals.

## 6.2 FAULT ISOLATION PROCEDURES

A fault isolation procedure is provided in flow chart format. The procedure is based on the self-tests incorporated into the subsystem. The procedure is designed to isolate and identify bad lines.

The chart symbols are defined in Table 6-1. The three- and four-digit numbers in the process boxes (for example, 6.4.4) are the numbers of the subsections that describe the test specified as the process.

Table 6-1. Flow Chart Symbol Definitions

| Symbol | Description |
|---|---|
|  | **Start point, ending point.** |
|  | **Decision, go ahead according with YES or NO.** |
|  | **Connector, go to same-numbered symbol on another sheet.** |
|  | **Process.** |

When the fault isolation procedure indicates a problem, see subsection 6.1.1 for service instructions.

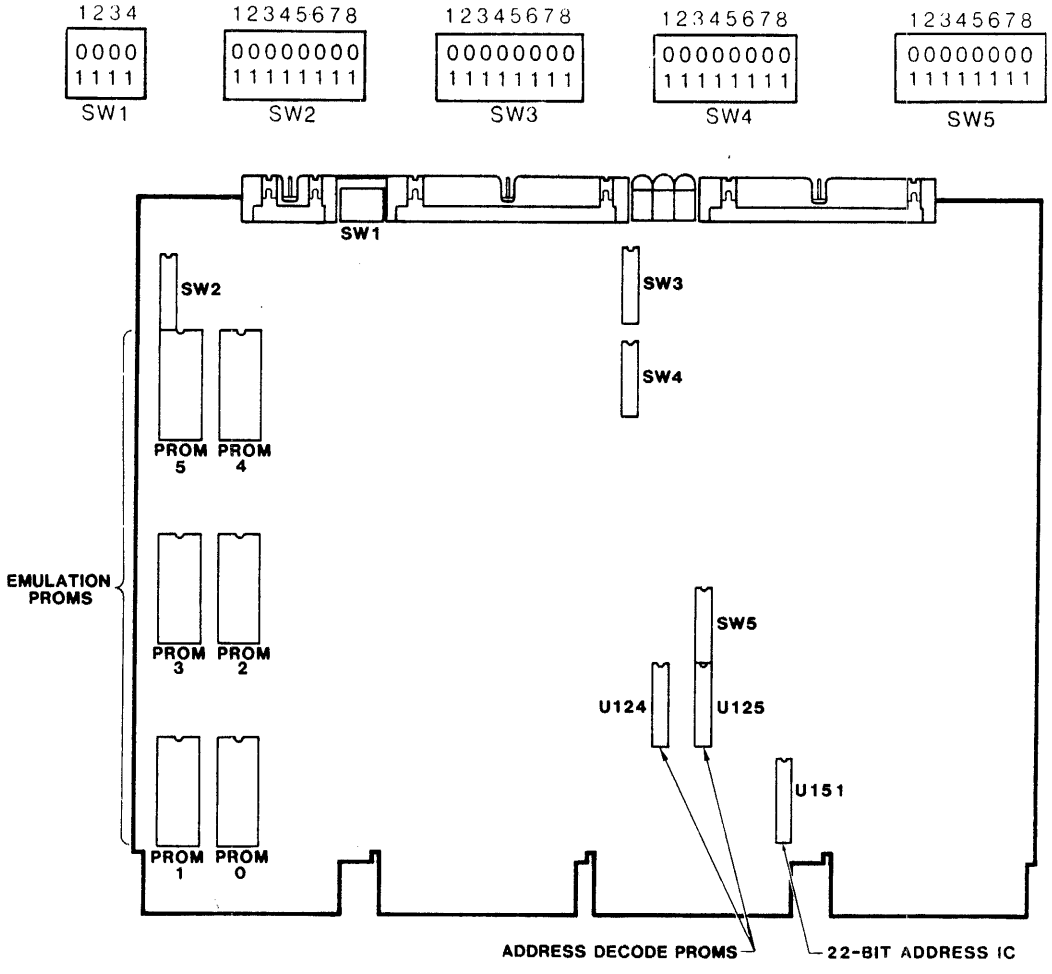
## CS02/H CONFIGURATION RECORD SHEET

GENERAL INFORMATION

1. Host computer type _____
2. Host computer operating system _____
3. Type of memory _____
4. Amount of memory _____
5. Terminal types _____

CC02 CONTROLLER MODULE

1. Emulation PROM numbers range from _____ to _____
2. Warranty expiration date _____
3. Top assembly number _____
4. Serial number _____
5. Address PROM numbers _____ and _____
6. Q-Bus address _____
7. Interrupt vector address _____ and _____
8. Switch settings (circle 1 or 0)




Use Pencil

Figure 6-1. CS02/H Configuration Reference Sheet

### 6.2.1 SELF-TEST FAILURE FAULT ISOLATION

The flow chart shown in Figure 6-2 is a representation of the subsystem verification procedure recommended in subsection 4.7 with fault isolation techniques added. The isolation techniques are designed to pinpoint the cause of most self-test failures.

The starting point is the initial power-up of the subsystem which, of course, causes all power-up self-tests to be performed. Each power-up self-test is represented by one or more decision diamonds in the chart. If a self-test fails, the failure branch of the decision diamond indicates additional operator-initiated self-diagnostics that can be performed to isolate the fault.

Aside from a wrap-around connector, no special test equipment is required. Subsystem cables can be checked by substitution or with the aid of a multimeter. All subsystem cables are shown schematically in Appendix A.

## 6.3 POWER-UP SELF-TESTS

The following subsections describe the self-tests performed by the major components of the subsystem. If any of these components completely fail their self-tests, you do not need to proceed with further tests. Package the units as described in subsection 6.1.1 and return them to the factory for repair. The major subsystem components are not designed to be serviced in the field.

### 6.3.1 CC02 CONTROLLER MODULE SELF-TEST

This power up self-test is a very thorough check of the CC02's functional integrity. Three functional areas are checked:

1. The on-board PROM and RAM memories
2. The on-board DUARTs (with the exception of the EIA drivers)
3. The microprocessor itself.

**NOTE**

Switches SW1-2 through SW1-4 must be OFF when the tests described are executed.

When power is applied to the CPU, or when switch SW1-1 on edge of the CC02 controller PCBA is turned ON and then OFF again (close/open), the controller automatically executes a built-in self-test. The test is not executed with every Bus INIT but only on power-up (i.e., DCLO asserted).

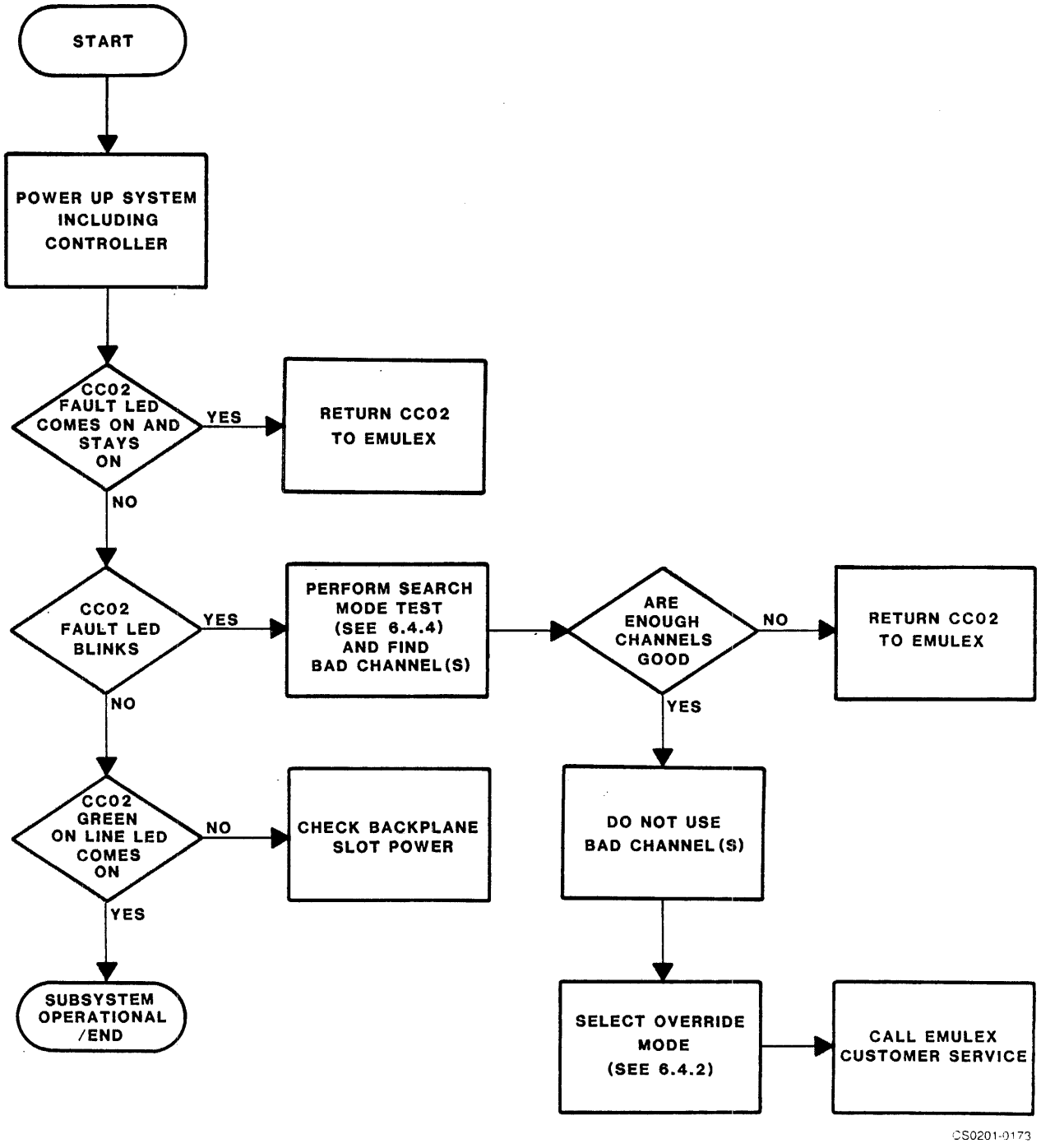



Figure 6-2. Self-Test Failure Fault Isolation Chart

During the self-test the Fault LED on the top edge of the CC02 control module is ON. If the self-test is completed successfully, the on-board microprocessor turns the Fault LED OFF. If the LED goes ON when power is applied and stays ON, a complete failure of the self-test is indicated. When the LED is ON, the CS02/H cannot be addressed by the CPU.

## 6.4 CC02 OPERATOR-INITIATED SELF-DIAGNOSTICS

There are several CS02/H self-diagnostics that can be selected by the operator using switches SW1-2 through SW1-4 on the CC02 Controller PCBA. The combinations of switch positions and the test modes that they produce are summarized in Table 6-2, below. The operation of the various test modes is detailed in subsections 6.4.1 through 6.4.4.

Table 6-2. Self-Test Modes

| Test Mode | Test Mode Description | --SW1-- 2 | 3 | 4 |
|---|---|---|---|---|
| 1 | Normal Run Mode - Fault LED blinks if any channel fails internal loopback test. | 0 | 0 | 0 |
| 2 | Override Mode - Fault LED blinks only if no channels pass internal loopback test. Controller will run with lines that pass. | 0 | 0 | 1 |
| 3 | Continuous External Loopback Mode - Fault LED blinks if any error is detected on any channel. | 0 | 1 | 0 |
| 4 | Search Mode - Fault LED goes off if at least channel is good. If no channels are good, the LED blinks. | 0 | 1 | 1 |
| 5 | Echo Mode - Characters received from any terminal at any baud rate will be echoed. Revision E firmware and above only. | 1 | 0 | 0 |
| 0 = open/OFF 1 = closed/ON | | | | |

### 6.4.1 NORMAL RUN MODE

The controller is placed in this mode for normal operation. In the Normal Run mode, the controller executes its standard self-test on power-up or when SW1-1 is closed and then opened (ON/OFF) (see subsection 6.3).

### 6.4.2 OVERRIDE MODE

All power-up diagnostic routines are performed in the Override mode, but the CC02 operates if at least one good serial port is detected. All of the serial ports that have passed the Internal Loopback test should function normally.

### 6.4.3 CONTINUOUS EXTERNAL LOOPBACK MODE

In this mode, the controller executes an External Loopback test continuously. For the controller to pass this test, all ports must be externally looped back. This loopback may be accomplished by placing loopback connectors on every port. If a port fails this test, the LED blinks. The bad port can then be isolated using the Search mode.

### 6.4.4 SEARCH MODE

In the Search mode, the controller executes a continuous external loopback test. If NO ports pass the test, the controller Fault LED blinks. If ONE port passes the test, the controller Fault LED goes out. This allows a faulty port to be isolated by plugging a loopback connector (see subsection 6.1.2) in each port, one port at a time. If the Fault LED goes out, that port is good. If it continues to blink, that port is bad.

### 6.4.5 ECHO MODE

In the echo mode, characters received from any terminal will be echoed back to that terminal. The terminal may be set for any baud rate. This mode is available only on Revision E and above firmware.

BLANK

## 7.1 OVERVIEW

This section contains a detailed description of the device registers which are accessible to the Q-Bus that are used to monitor and control the CS02/H Communications Subsystem. The registers are functionally compatible with those of a DEC DH11 communications multiplexer with DM11 modem control, or with those of a DEC DHV11 communications multiplexer.

This section also includes some general programming notes designed to aid the programmer who writes software to operate the CS02/H, and a brief architectural description of the CC02 Controller Module.

The following table outlines the contents of this section.

| Subsection | Title |
|---|---|
| 7.1 | Overview |
| 7.2 | DH11 Registers |
| 7.3 | DM11 Registers |
| 7.4 | DHV11 Registers |
| 7.5 | DH11/DM11 General Programming Notes |
| 7.6 | DHV11 General Programming Notes |
| 7.7 | Architecture |

For quick reference, Figure 7-1 illustrates the entire DH11- and DM11-type register set. The bit mnemonics are the same as those used in the more complete descriptions that follow. The subsection numbers in Figure 7-1 reference the appropriate descriptions.

The register address is given in terms of an offset from the device's base address. Simply add the offset to the base address to obtain the correct address for a specific register (base addresses and offsets are in octal notation). Note that the base addresses for the DH11 and DM11 register sets are different.

## 7.2 DH11 REGISTERS

There are eight 16-bit registers for the DH11. Three of these registers (LPR, CAR and BCR) are replicated for each of the 16 channels. Selection of the particular register set is made by the line number in SCR.

7.2.1 SYSTEM CONTROL REGISTER (SCR) +0

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TI | SI | TIE | SIE | MC | NXM | MM | CNI | RI | RIE | A17 | A16 | Line No. | | | |

7.2.2 RECEIVED CHARACTER REGISTER (RCR) +2

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VDP | DO | FE | PE | Line No. | | | | Received Character | | | | | | | |

7.2.3 LINE PARAMETER REGISTER (LPR) +4 (Indexed by Line No. of SCR)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | HD | Tx Speed | | | | Rx Speed | | | | OP | PE | 0 | TSB | Char. Length | |

7.2.4 CURRENT ADDRESS REGISTER (CAR) +6 (Indexed by Line No. of SCR)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Current Address | | | | | | | | | | | | | | | |

7.2.5 BYTE COUNT REGISTER (BCR) +10 (Indexed by Line No. of SCR)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Two's Complement of Number of Bytes | | | | | | | | | | | | | | | |

7.2.6 BUFFER ACTIVE REGISTER (BAR) +12

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Transmit Enable Bits | | | | | | | | | | | | | | | |

7.2.7 BREAK CONTROL REGISTER (BRCR) +14

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Break Bits | | | | | | | | | | | | | | | |

7.2.8 SILO STATUS REGISTER (SSR) +16

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SM | 0 | Silo Fill Level | | | | | | A17 | A16 | Silo Alarm Level | | | | | |

7.2.9 CONTROL AND STATUS REGISTER (CSR) +0

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RF | CF | CTS | 0 | CS | CM | MM | STP | DONE | IE | SE | BUSY | Line No. | | | |

7.2.10 LINE STATUS REGISTER (LSR) +2 (High byte indexed by Line No. of SCR, low byte indexed by Line No. of CSR)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | A21 | A20 | A19 | A18 | A17 | A16 | RNG | CAR | CTS | 0 | 0 | RTS | DTR | LE |

CS0201-0148

Figure 7-1. DH11/DM11 Registers

### 7.2.1 SYSTEM CONTROL REGISTER (SCR) +0

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TI | SI | TIE | SIE | MC | NXM | | MM | CNI | | RI | RIE | A17 | A16 | Line No. | |

Read/Write, Byte Addressable

Transmitter Interrupt (TI) - Bit 15

Read/Write

Cleared by Master Clear

This bit is set when the controller increments the byte count to zero, indicating that the last character of a DMA transfer has been loaded into a DUART transmitter holding register. Setting TI also causes an interrupt to be generated if TIE (bit 13) is set.

The line that caused TI to set can be determined by reading the BAR. The bit(s) that is reset and had been previously set to enable transmission identifies the line(s) that caused the interrupt. An exclusive-or comparison of the current contents of BAR and the pervious image will identify the interrupting line(s). TI must be reset before reading the BAR to allow the controller to post another interrupt.

Storage Interrupt (SI) - Bit 14

Read-Only

Cleared by Master Clear

This bit is set when the receiver scanner has found a receiver-holding register with a character in it and desires to store that character in the receiver silo, but cannot because the receiver silo is full. Setting this bit causes an interrupt to be generated if SIE (bit 12) is set.

Transmitter Interrupt Enable (TIE) - Bit 13

Read/Write

Cleared by Master Clear

Setting this bit allows the setting of TI or NXM (bit 15 or 10, respectively) to generate a transmitter interrupt request or non-existent memory interrupt request.

Storage Interrupt Enable (SIE) - Bit 12

Read/Write

Cleared by Master Clear

Setting this bit allows the setting of SI (bit 14) to generate an interrupt request.

Master Clear (MC) - Bit 11

Read/Write

Cleared by Master Clear

Setting this bit initializes the controller, clearing the silo, the DUARTs and the registers. The controller resets this bit when the initialization operation is complete.

Non-Existent Memory (NXM) - Bit 10

Read-Only

Cleared by Master Clear

This bit is set when the controller is bus master during NPR transfer and does not receive a SSYN from the memory within 20 microseconds NXM is also set if a parity error is detected during a DMA (memory read) operation.

Maintenance Mode (MM) - Bit 09

Read/Write

Cleared by Master Clear

Setting this bit places the controller in the Maintenance mode. When in Maintenance mode, it is possible to write bits 07, 10 and 14 of the SCR, which are normally read-only. Also, the transmitted data signal is internally looped to the received data input.

Clear Non-Existent Memory Interrupt (CNI) - Bit 08

Read/Write

Cleared by Master Clear

Setting this bit clears the non-existent memory interrupt (bit 10) and clears itself.

Receiver Interrupt (RI) - Bit 07

Read-Only

Cleared by Master Clear

Setting this bit indicates that the number of characters stored in the silo exceeds the "alarm level" specified by the low byte of the SSR. Setting this bit generates an interrupt request if RIE (bit 06) is also set.

Receiver Interrupt Enable (RIE) - Bit 06

Read/Write

Cleared by Master Clear

Setting this bit allows the setting of RI (bit 07) to generate an interrupt request.

Extended Address Bits (A17, A16) - Bits <05:04>

Read/Write

Cleared by Master Clear

These bits are bus address bits A17 and A16 for the line specified in bits <03:00>. The contents of these bits are copied into the 18-bit CAR for the line when the low-order 16 bits are loaded in the CAR. When these bits are read, they do not represent the actual status of the address bits for the selected line.

**NOTE**

If the 22-bit addressing mode option has been selected, these bits are not used. The upper six bits of the current address are written through the high byte of the LSR.

Line Number - Bits <03:00>

Read/Write

Cleared by Master Clear

Each of the 16 channels served by the controller has its own storage for channel parameter information, current address, and byte count. These storage locations are loaded by the program via the LPR, CAR, and BCR, which are indexed by the line number in the SCR.

### 7.2.2 RECEIVED CHARACTER REGISTER (RCR) +2

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| VDP | DO | FE | PE | Line No. | | | | Received Character | | | | | | | |

Read-Once, Word Addressable

This register is the bottom of the 64-word silo. Valid silo data is displayed if bit 15 is set. When this register is read the bottom word of the silo is removed, the Silo Fill Level in SSR is decremented by one, and SI in the SCR is reset.

Valid Data Present (VDP) - Bit 15

Read-Once

Cleared by Master Clear

When set, this bit indicates that the data present in bits <14:00> of this register are valid. When this register is read and bit 15 is set, the character in the low byte is valid and should be processed. The program should continue reading this register and processing characters until bit 15 is found to be reset, indicating the the receive silo is empty. An entry is lost after being read.

Data Overrun (DO) - Bit 14

Read-Once

Cleared by Master Clear

When set, this bit indicates that the received character was preceded by a character that was lost due to the inability of the receiver scanner to service the DUART receiver holding-register or because the silo is full.

Framing Error (FE) - Bit 13

Read-Once

Cleared by Master Clear

When set, this bit indicates that the receiver has sampled a line for the first stop bit, and found the line in a spacing condition (logical zero). This condition usually indicates the reception of a Break.

Parity Error (PE) - Bit 12

Read-Once

Cleared by Master Clear

When set, this bit indicates that the parity of the received character does not agree with that designated for the channel.

Line Number - Bits <11:08>

Read-Once

Cleared by Master Clear

The state of these bits indicate the line number on which the received character was received. Bit 08 is the least significant bit.

Received Character - Bits <07:00>

Read-Once

Cleared by Master Clear

These bits contain the received character, right justified, if the valid bit (bit 15) is set. The least significant bit is bit 00.

### 7.2.3 LINE PARAMETER REGISTER (LPR) +4 (Indexed by Line No. of SCR)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | HD | Tx Speed | | | | Rx Speed | | | | OP | PE | 0 | TSB | Char. Length | |

Read/Write, Byte Addressable

The LPR for all channels is cleared by Initialize and Master Clear.

Half-Duplex (HD) - Bit 14

Cleared by Master Clear

Setting this bit causes the channel to operate in half-duplex mode. If HD is reset, this channel will operate in full-duplex mode. In half-duplex operation, the receiver is blinded during transmission of a character.

Transmitter Speed - Bits <13:10>

Cleared by Master Clear

The state of these bits determines the operating speed for this channel's transmitter. See Table 7-1.

Table 7-1. Tx and Rx Speed Table

| Tx Rx | Bits 13 09 | 12 08 | 11 07 | 10 06 | Baud Rate |
|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | Disable |
| | 0 | 0 | 0 | 1 | 50 |
| | 0 | 0 | 1 | 0 | 75 |
| | 0 | 0 | 1 | 1 | 110 |
| | 0 | 1 | 0 | 0 | 134.5 |
| | 0 | 1 | 0 | 1 | 150 |
| | 0 | 1 | 1 | 0 | 200 |
| | 0 | 1 | 1 | 1 | 300 |
| | 1 | 0 | 0 | 0 | 600 |
| | 1 | 0 | 0 | 1 | 1200 |
| | 1 | 0 | 1 | 0 | 1800 |
| | 1 | 0 | 1 | 1 | 2400 |
| | 1 | 1 | 0 | 0 | 4800 |
| | 1 | 1 | 0 | 1 | 9600 |
| | 1 | 1 | 1 | 0 | 19200 or 100[1] |
| | 1 | 1 | 1 | 1 | Not Supported |

[1]The rate selected by this code is determined by SW2-3 on the CC02. See subsection 4.3.4.4.

Receiver Speed - Bits <09:06>

Cleared by Master Clear

The state of these bits determines the operating speed for this channel's receiver. See Table 7-1.

Odd Parity (OP) - Bit 05

Cleared by Master Clear

If this bit and PE (bit 04) are set, characters of odd parity are generated on this channel and incoming characters will be expected to have odd parity. If this bit is not set, but bit 04 is set, characters of even parity are generated on this channel and incoming characters are expected to have even parity. If bit 04 is not set, the setting of this bit has no meaning or affect.

Parity Enabled (PE) - Bit 04

Cleared by Master Clear

If this bit is set, characters transmitted on this channel have an appropriate parity bit affixed, and characters received on this channel have their parity checked.

Two Stop Bits (TSB) - Bit 02

Cleared by Master Clear

Setting this bit conditions a channel that is transmitting with six-, seven-, or eight-bit code to transmit characters that have two stop bits. If the channel is transmitting five-bit code, assertion of this bit causes the characters to be transmitted with 1.5 stop bits. If this bit is not asserted, one stop bit is sent.

**NOTE**

Switch SW2-6 on the CC02 Controller Module can override the code specified here. See subsection 4.3.4.6 for details.

Character Length - Bits <01:00>

Cleared by Master Clear

To receive and transmit characters of the lengths (excluding parity bit) shown, these bits should be set as listed in the following table.

| Bit 01 | Bit 00 | Bits/ Character |
|---|---|---|
| 0 | 0 | 5 bit |
| 0 | 1 | 6 bit |
| 1 | 0 | 7 bit |
| 1 | 1 | 8 bit |

### 7.2.4 CURRENT ADDRESS REGISTER (CAR) +6 (Indexed by Line No. of SCR)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Current Address | | | | | | | | | | | | | | | |

Read/Write, Word-Addressable

This register contains 16 of the 18 or 22 memory address bits for the channel specified in the SCR. This register must be loaded only after the SCR has been loaded with the desired channel number and the A17 and A16 address bits. (If the 22-bit addressing mode option has been selected, the upper six bits of the address are loaded through the upper byte of the LSR. See subsection 4.3.4.7 for details on this option.) When this register is loaded, address bits <15:00> of this register and A17 and A16 from the SCR are transferred into an 18-bit CAR for the channel.

### 7.2.5 BYTE COUNT REGISTER (BCR) +10 (Indexed by Line No. of SCR)

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Two's Complement of Number of Bytes | | | | | | | | | | | | | | | |

Read/Write, Word Addressable

This register is loaded with the two's complement of the number of bytes to be transferred.

In the same fashion as LPR and CAR, this register must not be loaded or read without first selecting the channel number in SCR.

### 7.2.6 BUFFER ACTIVE REGISTER (BAR) +12

| 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Transmit Enable Bits | | | | | | | | | | | | | | | |

Read-Modify-Write Ones-Only, Byte Addressable

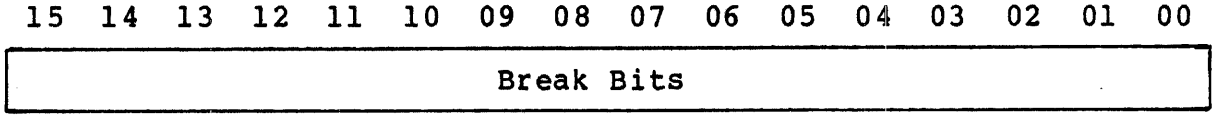
Cleared by Initialize and Master Clear

This register contains one bit for each channel. The bits are set individually using BIS instructions. Setting a bit initiates transmission on the associated channel. The bit is cleared by the controller when the last character to be transmitted on that channel is loaded in the the transmitter-holding buffer of the DUART. Although the clearing of a BAR bit does indicate that a new message may be sent, it does not indicate that the last characters from the preceding message have been completely sent. Specifically, two more characters are sent after the BAR bit clears. These are the last two

characters of the message; one of them is starting when the BAR is cleared, and one is the final character that is loaded into the holding register at time the BAR is cleared. This effect is a normal consequence of double-buffered transmission and is mentioned here for the benefit of programmers who want to write programs that control such modem leads as Request To Send.

The software driver should maintain an image of BAR. After setting a BAR bit to initiate tranmission, the software image of BAR should be updated. Upon receipt of a transmit interrupt (indicating transmission is completed), bit 15 of SCR should be reset. Then, the driver should read BAR and perform an exclusive-or comparison between BAR and the software image. This action will identify the line that completed the transmission. When the line finishes transmission, the software image of BAR should once again be updated. Note that although it is possible for multiple lines to finish transmission on a single interrupt, the driver need only read BAR once for each entry into the transmit service routine. (It is possible to find that no lines have finished transmission even though an interrupt was generated. In this case, the line that caused the interrupt was detected in BAR on the previous interrupt.)

### 7.2.7 BREAK CONTROL REGISTER (BRCR) +14




Read-Modify-Write, Byte Addressable

Cleared by Initialize and Master Clear

This register contains one bit for each channel. Setting a bit in this register immediately generates a break condition on the channel corresponding to that bit number; clearing the bit terminates the break condition. For the break condition to occur, bits <13:10> in LPR must contain a nonzero value. A zero value in these bits disables the transmitter and inhibits a break operation. The duration of the break must be controlled by a software timer. Do not use the transmission of characters during a break interval to time the interval. Cleared by Initialize and Master Clear.