SC03/B1

RM03/RM05/RM80 COMPATIBLE

DISK CONTROLLER

TECHNICAL MANUAL

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INTRODUCTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the SC03/B1 Disk Controller. In addition, this manual provides diagnostic and application information.

1.1.1 Register Addresses in this Manual

The register addresses given in this manual are standard Q-Bus addresses for an RM disk subsystem. All addresses are given for an 18-bit Q-Bus. For 22-bit addressing add 17000000 to obtain the desired register address.

1.2 OVERVIEW

1.2.1 General Description

The SC03/B1 Disk Controller is a one board, imbedded controller for LSI-11 computers manufactured by Digital Equipment Corporation. This controller can be used to interface any large disk having a Storage Module Drive (SMD) interface. The SC03/B1 controller emulates the RH11 and RH70 disk controllers manufactured by Digital Equipment Corporation for use with RM02, RM03, RM05, and RM80 disk drives.

1.3 FEATURES

1.3.1 Microprocessor Design

The SC03/B1 design incorporates a unique 16-bit bipolar microprocessor to perform all controller functions. The microprocessor approach provides for a reduced component count, high reliability, easy maintainability, and most importantly, the ability to adapt a single set of hardware to a wide range of emulation capabilities through the use of microprogramming. The Emulex controllers achieve functional capability beyond that of the DEC controllers which they emulate, by providing enhancement features such as built-in self-test during power-up, built-in disk formatting and the ability to work with disk drives of various sizes.

1.3.2 Packaging

The SC03/B1 is constructed on a single, quad-size, Multi-layer PC board which plugs directly into the LSI-11 chassis. No cabling is

required between the computer and the disk controller. The controller obtains its power from the chassis in which it is mounted.

1.3.3 Self-Test

The controller incorporates an internal self-test routine which is executed upon power-up. This test exercises all parts of the microprocessor, buffer and disk data logic. Although this test does not completely test all controller circuitry, successful execution indicates a very high probability that the controller is operational. If the controller fails the self-test, it leaves the LED ON and the controller cannot be addressed from the CPU.

1.3.4 Buffering

The controller contains a 4K x 16 high-speed RAM buffer. It is used to store the device registers of the controller plus a 14 sector data buffer. The large buffer eliminates the possibility of a data late condition and permits the controller to be operated at low bus priorities.

1.3.5 Error Correction

The controller incorporates a 32-bit error correcting code (ECC) capable of correcting a single error bit in bursts of up to 11 bits in length and detecting multiple error bits in bursts of any length. The controller determines the pattern and location of the error so that the software may correct the data after it is transferred to memory. A 16-bit CRC is employed with the header of every sector.

1.3.6 Dual Port Mode

In order to provide compatibility with dual port drivers when configured for dual port, the dual port mode is provided. This mode should be selected only when the disk drive has dual ports and is configured for dual port operation.

1.3.7 Dual Access Mode

In order to provide compatibility with dual access drivers when configured for dual access, the dual access mode is provided. When in this mode, the controller sets Dual Port Mode (Drive Type Register) and Programmable (Drive Status Register) to imitate the DEC neutral state.

Setting the Dual Port Option switch overrides the Dual Access Option except except for the one-second power-up timer disable.

1.3.8 Option and Configuration Switches

Sockets provide for insertion of optional 512 word bootstrap PROMS, 22-bit addressing and Q-Bus termination resistor packs. Provisions

are also made to enable an optional software-controlled line time clock (LTC) which is BDV11 compatible.

DIP switches are used to configure the controller for various disk sizes, Q-Bus addresses and options. It is possible to select one of several possible combinations of disk characteristics for the two drives which can be handled by the controller, including mixtures of disk sizes and drive type codes.

1.4 FUNCTIONAL COMPATIBILITY

1.4.1 Media Compatibility

In all cases, the headers written on the drives are standard RM02, RM03, RM05 and RM80 headers. Packs may be formatted by utilizing the hardware formatting capability of the extended command set. Disk packs formatted with an SC03/B1 controller are media compatible with other Emulex controllers and with the equivalent DEC packs when appropriate disk drives are used.

1.4.2 Disk Mapping

Depending upon the type and size of the disk drive, one or two logical units may be mapped on it. Various mapping organizations are used; some of which do not leave direct 1:1 correlation between the logical and physical addresses.

1.4.3 Diagnostics

The SC03/B1 will run the following DEC diagnostics on LSI-11 computers.

- ZRMA Formatter
- ZRMB Performance Exerciser
- ZRMC Functional Controller, Part I*
- ZRMD Functional Controller, Part II*
- ZRME Functional Controller, Part III*
- ZRMF Extended Drive Test
- ZRMI Drive Compatibility Test

The diagnostics marked with an asterisk require certain patches to bypass unsupported maintenance functions. All diagnostics require patches to run with drive sizes other than that of a standard RM02/RM03. See Appendix B for diagnostic patches.

Emulex provides self-sizing diagnostics for the SC03. They are listed at the end of Appendix B.

1.4.4 Operating Systems

The SC03/B1 is compatible with all DEC operating systems running on LSI-11 computers that support the appropriate DEC disk subsystems. No operating system modifications are required when running standard sized disk drives.

Table 1-1
General Specifications

FUNCTIONAL	
Emulation	DEC RM02, RM03, RM05 and RM80
Media Compatibility	DEC RM02, RM03 and RM05 when using appropriate disk drives.
Drive Interface	SMD
Drive Ports	2
Error Control	32-bit ECC for data and 16-bit CRC for headers. Correction of single data error burst of up to 11 bits.
Sector Size	256 words (512 bytes)
Sectors/Track	Selectable for each drive.
Tracks/Cylinder	Selectable for each drive.
Cylinders/Drive	Selectable for each drive.
Drive Type Code	Selectable for each drive.
Computer Interface	Q-Bus
Q-Bus Address	
Standard	776700-776752
Alternate	776300-776352
Vector Address	
Standard	254
Alternates	50, 150, 270, 274, 354, 370, 374
Priority Level	BR4
Data Bufferring	14 full sectors
Data Transfer	High speed NPR operation.
Maximum Disk Data Rate	16 MHz (2 MBytes/second)

Table 1-1 (cont'd)

Self-Test	Extensive internal self-test on powering up.
Indicators	Activity/Fault LED
DESIGN	High-speed bipolar microprocessor using 2901 bit slice components.
PHYSICAL	
Packaging	One DEC quad-size board.
Mounting	Any slot in CPU or expansion box.
Connectors	One 60-pin A cable flat connector and two 26-pin B cable connectors. (Flat cable type.)
Electrical	
Q-Bus Interface	DEC approved line drivers and receivers.
Drive Interfaces	Differential line drivers and receivers. A cable accumulative length to 35 feet. B cable length to 25 feet.
Power	+5 v, 8 Amp. max.

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2.1 CONTROLLER ORGANIZATION

A block diagram showing the major functional elements of the SC03/B1 controller is shown in Figure 2-1. The controller is organized around a 16-bit high-speed bipolar microprocessor. The ALU and register file portion of the microprocessor are implemented with four 2901 bit slice components. The microinstruction is 48 bits in length and the control memory of 2K words is implemented with six 2K x 8 PROMs.

The controller incorporates a 4K x 16 high-speed RAM buffer which is used to store the controller's device registers and 14 sectors of data buffering.

The A Cable Register (ACR) latches all A cable signals going to or from the disk drives. The inputs from the selected drive are testable by the microprocessor.

The Shift Register converts parallel write data from the data bus to serial data for the disk drives. The register also converts serial read data from the drives back into parallel data. Serial read and write data is provided to the ECC logic via the Shift Register.

Serial data from the drive is converted into eight-bit parallel data and transferred to the buffer via the microprocessor. Likewise, the data access from the buffer by the microprocessor is serialized and sent to the drive under the control of the servo clock received from the drive. A 32-bit ECC Shift Register is used to generate and check the ECC for the data field. The same register is also used in a 16-bit CRC mode for the headers. The actual ECC polynomial operation is done independently of the microprocessor, but the determination of the error position and error pattern is done under the control of the microprocessor.

The Q-Bus interface consists of 42 bidirectional lines (which include lines A18 to A21) and two unidirectional signal lines. The Q-Bus interface is used for programmed I/O, CPU interrupts, and data transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed controller register. The microprocessor also controls all DMA operations and transfers data between the Q-Bus data lines and the buffer.

2.2 PHYSICAL DESCRIPTION

The SC03/B1 controller consists of a single quad-size board which plugs directly into an LSI-11 chassis. The controller PCBA is shown in Figure 2-2.

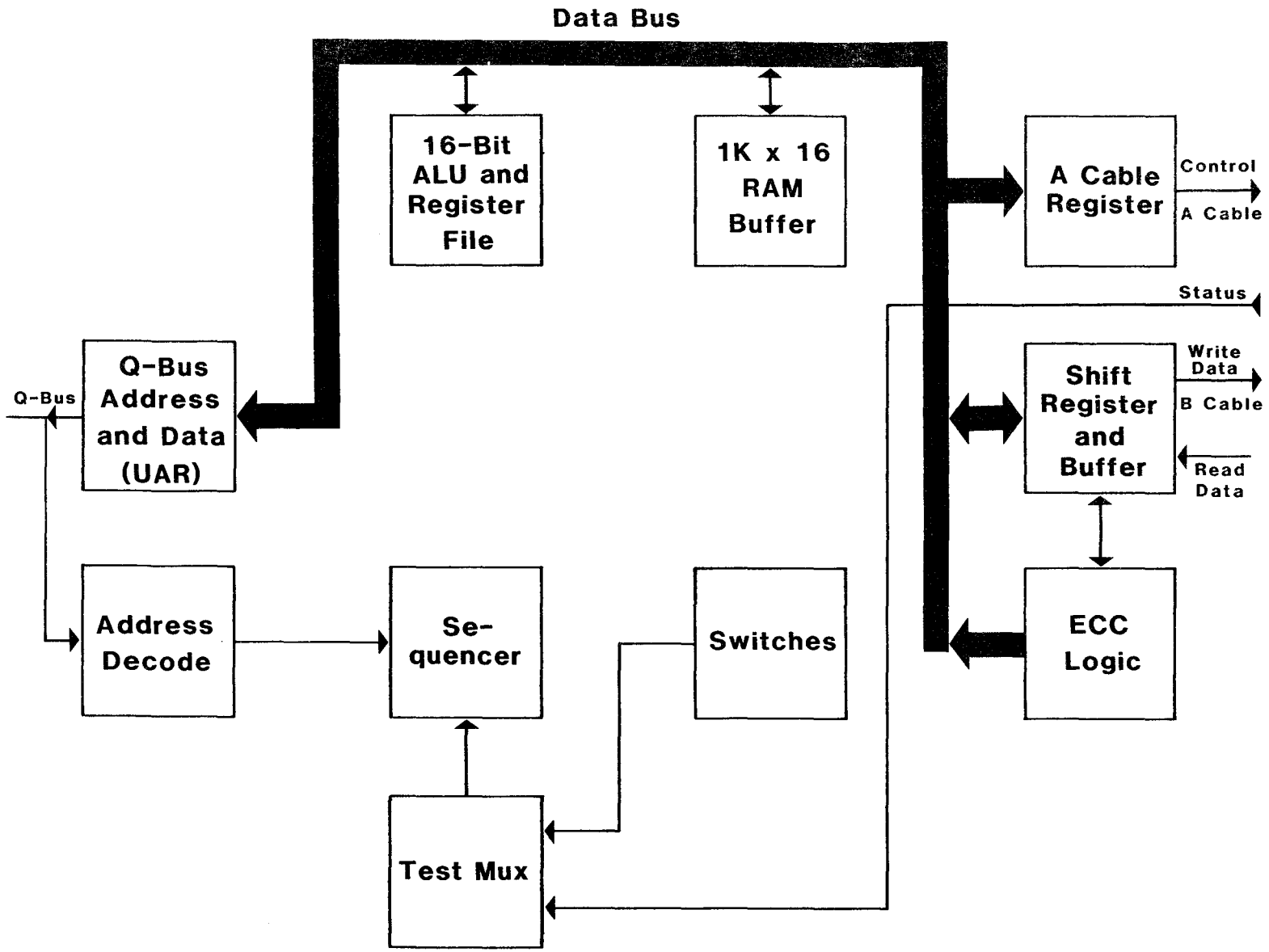
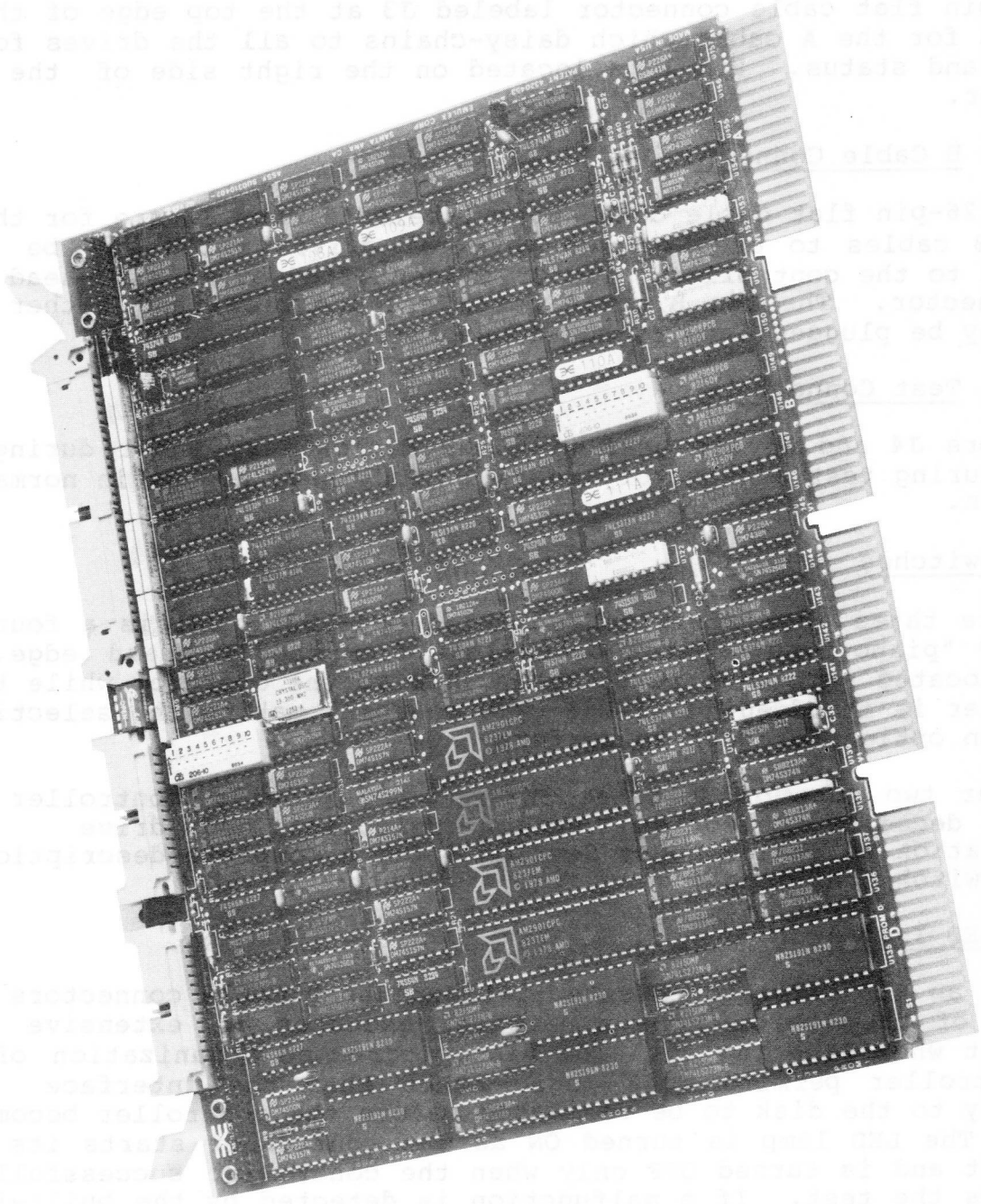


Figure 2-1 SC03 Block Diagram



2.2.1 Connectors

2.2.1.1 A Cable Connector

The 60-pin flat cable connector labeled J3 at the top edge of the board is for the A cable which daisy-chains to all the drives for control and status. Pin 1 is located on the right side of the connector.

2.2.1.2 B Cable Connector

The two 26-pin flat cable connectors labeled J1 and J2 are for the radial B cables to each of two physical drives which may be attached to the controller. Pin 1 is identified by an arrowhead on the connector. The two B cable ports are identical and either drive may be plugged into either connector.

2.2.1.3 Test Connectors

Connectors J4 and J5 are used with the Emulex test panel during manufacturing test and factory repair. They have no use in normal operation.

2.2.2 Switches

There are three sets of switches labled SW1-SW3. SW1 is a four pole DIP "piano-type" switch accessible from the PC board edge. SW1 is located such that it is accessible to the operator while the controller is imbedded in an LSI type chassis, making the selection of common options simpler to perform.

The other two sets of switches SW2 and SW3 provide controller address decoding selection, option selection and drive configuration selection. (See Section 3 for a complete description of the switch functions.)

2.2.3 LED Indicator

There is an LED indicator mounted between the B Cable connectors at the top of the board. The controller executes an extensive self-test when powering up. The microprogrammed organization of the controller permits most logic other than the interface circuitry to the disk to be validated before the controller becomes ready. The LED lamp is turned ON as the controller starts its self-test and is turned OFF only when the controller successfully completes the test. If a malfunction is detected by the built-in diagnostics, the LED remains ON and the controller will not respond to program I/O. The LED blinks at approximately a one second rate if the self-test is successful but no drive is seen on-line. The LED also functions as an activity indicator during read and write operations.

2.2.4 Firmware PROMs

There are six PROM sockets, used for the control memory, located along the left edge of the board. The sockets are labeled PROM 0 through PROM 5 in a discontinuous physical order. The numbers on the top of the PROM ICs are Emulex part numbers, which identify the unique pattern of the PROM. When inserting PROMs in the board, the ID numbers are placed in the same sequence as the PROM numbers on the board beside each socket.

2.2.5 Bootstrap PROMs

There are two sockets provided for the installation of optional bootstrap PROMs. They are at location U71 and location U92. PROM number B02 or B04 goes in location U92, and PROM number B03 or B05 goes in location U71. The Emulex part number of the option kit is SC0313001. See paragraph 3.4.4.2 for installation instructions, and section 6 for operating instructions.

2.3 INTERFACES

2.3.1 Disk Interface

The controllers's disk interface conforms to the Flat Cable Interface Specification for the SMD, MMD, and CMD (CDC Document No. 64712400). The controller has been tested with most drives using the SMD, MMD and CMD interfaces and is compatible with these drives electrically and in timing.

The following defines the electrical interface and the recommended cables.

2.3.1.1 A Cable

The 60-conductor A cable is daisy-chained to all drives and terminated at the last drive. The signals in this cable are listed in Table 2-1 along with their function when the control tag (Tag 3) is asserted. The A cable should be a 30-twisted-pair flat cable with an impedance of 100 ohms and a cumulative length of no greater than 35 feet.

Spectra-Strip P/N 455-248-60 flat cable or its equivalent is recommended. It is possible to order A-Cable assemblies from Emulex that are made up in one of four lengths:

EMULEX P/N	LENGTH (FT.)
SU1111201	8.0
SU1111203	15.0
SU1111205	25.0
SU1111207	35.0

Table 2-1
Disk Drive Connections

Pins Lo/Hi	Signal	(Tag 3 Function)	From/To
A Cable:			
22,52	Unit Select Tag		To
23,53	Unit Select bit 0		To
24,54	Unit Select bit 1		To
26,56	Unit Select bit 2		To
27,57	Unit Select bit 3		To
1,31	Tag 1		To
2,32	Tag 2		To
3,33	Tag 3		To
4,34	Bit 0	(Write Gate)	To
5,35	Bit 1	(Read Gate)	To
6,36	Bit 2	(Servo Offset Plus)	To
7,37	Bit 3	(Servo Offset Minus)	To
8,38	Bit 4	(Fault Clear)	To
9,39	Bit 5	(AM Enable)	To
10,40	Bit 6	(Return to Zero)	To
11,41	Bit 7	(Data Strobe Early)	To
12,42	Bit 8	(Data Strobe Late)	To
13,43	Bit 9	(Release)	To
30,60	Bit 10		To
14,44	Open Cable Detect		To
15,45	Fault		From
16,46	Seek Error		From
17,47	On Cylinder		From
18,48	Index		From
19,49	Unit Ready		From
20,50	Not Used		From
21,51	Busy (dual port only)		From
25,55	Sector		From
28,58	Write Protected		From
29	Power Sequence Hold		To
59	Power Sequence Pick		To
B Cable:			
8,20	Write Data		To
6,19	Write Clock		To
2,14	Servo Clock		From
3,16	Read Data		From
5,17	Read Clock		From
10,23	Not Used		From
22,9	Unit Selected		From
12,24	Not Used		From
13,26	Not Used		From

2.3.1.2 B Cable

The 26-conductor B cable is radial to all drives and contains the data and clock signals. The signals and grounds in this cable are listed in Table 2-1. The B cable should be 26 conductor flat cable with ground plane and drain wire. The impedance should be 130 ohms and the length must not be greater than 25 feet.

3M-P/N 3476/26 flat cable or its equivalent is recommended. It is possible to order B-cable assemblies from Emulex that are made up in one of three lengths:

EMULEX P/N	LENGTH (FT.)
SU1111202	8.0
SU1111204	15.0
SU1111206	25.0

2.3.2 Q-Bus Interface

The LSI-11 Bus consists of 42 bidirectional and 2 unidirectional signal lines. These form the lines along which the processor, memory and I/O devices communicate with each other.

Addresses, data, and control information are sent along these signal lines, some of which contain time-multiplexed information. The lines are divided as follows:

1. Sixteen data/address lines - <BDAL00:BDAL15>
2. Six address lines - <BDAL21:BDAL16>
3. Six data transfer control lines - BBS7, BDIN, BDOUT, BRPLY, BSYNC, BWTBT
4. Three direct memory access control lines - BDMGI, BDMR, BSACK
5. Six interrupt control lines - BEVENT, BIAKO, BIRQ4, BIRQ5, BIRQ6, BIRQ7
6. Five system control lines - BPCOK, BHALT, BINIT, BPOK, BREF.

The MS four data/address lines (BDAL <21:18>) are used only for addressing and do not carry data. BDAL <17:16> reflect the parity status of the 16-bit data word during the data transfer portion of the bus cycle.

Table 2-2
Q-Bus Connections

	A		B	
	1	2	1	2
A	BIRQ5	+5V	BPCOK	+5V
B	BIRQ6		BPOK	
C	BDAL16	GND	BDAL18	GND
D	BDAL17		BDAL19	
E		BDOUT	BDAL20	BDAL02
F		BRPLY	BDAL21	BDAL03
H		BDIN		BDAL04
J	GND	BSYNC	GND	BDAL05
K		BWTBT		BDAL06
L		BIRQ4		BDAL07
M	GND	BIAKI	GND	BDAL08
N	BDMR	BIAKO	BSACK	BDAL09
P	BHALT	BBS7	BIRQ7	BDAL10
R	BREF	BDMGI	BEVENT	BDAL11
S		BDMGO		BDAL12
T	GND	BINIT	GND	BDAL13
U		BDAL00		BDAL14
V		BDAL01		BDAL15

2.3.2.1 Interrupt Priority Level

The controller is hardwired to issue level 4 interrupt requests and monitor level 5. The level 4 request is necessary to allow compatibility with either a LSI-11 or LSI-11/2 processor.

2.3.2.2 Register Address

The register address and the number of registers assigned to the controller are decoded by a PROM at U124. The selections available are determined by configuration switches SW3-7 and SW3-8 as discussed in Section 3.

2.3.2.3 DCOK and INIT Signals

The DCOK and INIT signals both perform a controller clear. The self-test is performed only when DC power is initially applied.

2.4 DISK FORMAT

2.4.1 Disk Pack Organization

The formatting of a disk pack and the mapping of one or two logical drives onto a physical drive varies with the drive size. Some of this information is supplied by the configuration PROM. The rest is computed based upon configuration PROM information.

2.4.2 Mapping

Depending upon the type and size of the disk drive, one or two logical units may be mapped on it. The controller can handle a maximum of four logical units distributed across a maximum of two physical drives. A logical drive may not be mapped across a physical unit boundary.

In most cases there is a 1:1 correspondence between logical and physical disk addresses. The controller has the capability to alter a logical address to a different physical address in order to accommodate drives that do not match the number of tracks and cylinders for the RM unit being emulated.

2.4.3 Sector Organization

Figure 2-3 shows the typical sector format used by the controller. Each track of 20,160 bytes is divided into 32 sectors of 630 bytes. The four byte header is preceded by a preamble of 30 bytes ending in the sync byte and is followed by a two byte CRC. The 256-word data field is preceded by a preamble of 20 bytes ending in the sync byte, and is followed by four bytes of ECC. This format is compatible with that of the DEC RM02, RM03, RM05, and RM80.

If the actual size of the useful data information is less than 256 words, the remainder of the data field will be filled with 0's until 256 words have been written. During disk formatting

procedures, each data track is located and recorded with header information by means of the Write Header and Data command. A disk pack should be formatted and the format verified before any real data is written on it. Once formatted, individual or groups of sectors should not be reformatted unless absolutely necessary.

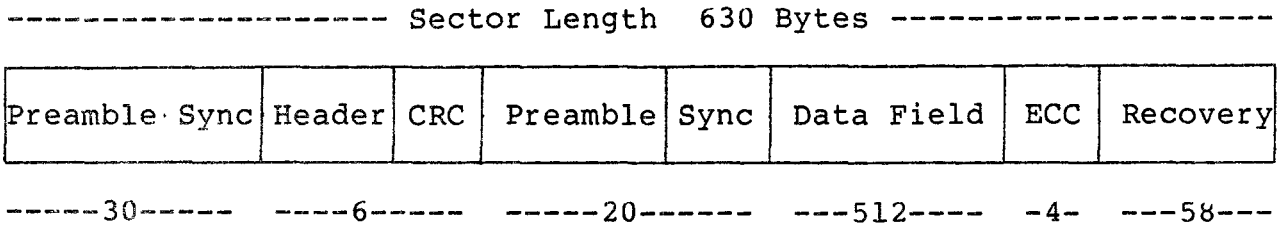
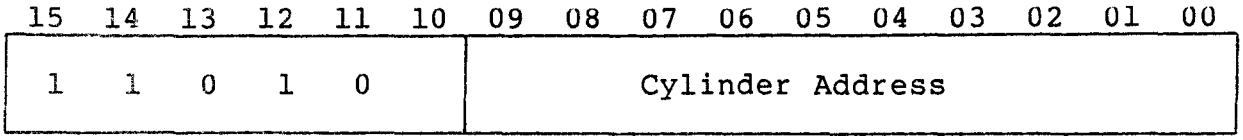
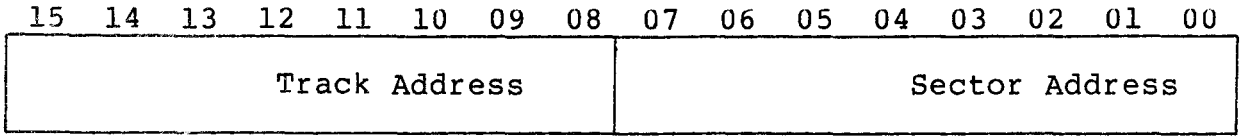


Figure 2-3
Sector Format

Header Word 1:



Header Word 2:



Header Word 3:

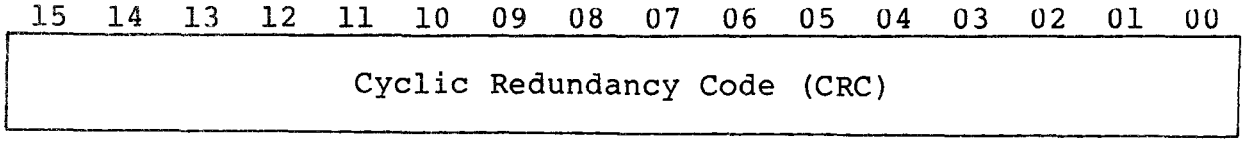


Figure 2-4
Header Format

2.4.4 Header

2.4.4.1 Header Description

Figure 2-4 shows the header format, which consists of the following three words:

Word One: This word contains the cylinder address. It contains a 1 in bit 12 to identify 16-bit format to the software and 1-bits in bit positions 14 and 15 to identify a good sector. For RM80 emulations only, bit 13 will contain a 1-bit to identify skipped sectors and a 0-bit for normal sectors.

Word Two: The low-order eight bits of this word contain the sector address. Each track on the drive typically contains 32 sectors. The upper byte of this word contain the track address.

Word Three: This is the CRC word which is generated and checked by the controller logic. This word is not available to the software.

2.4.4.2 Header Field Handling

After the drive reports that it is on cylinder, the controller locates the desired sector by means of the sector counters. The sector counters for each drive are maintained in the controller. The controller compares the first two words of the header against the desired track, sector and cylinder and then checks the CRC word for errors. An error in the header field is indicated by turning on the appropriate error bit in the error register (format error, header compare error, bad sector error, skip sector error or CRC error). A header error is only valid when the sector count field of the RMLA register and the sector field of the RMDA have already matched. It is immaterial where a CRC error occurs in the header field since the controller cannot determine its location in the field. However, software may read the header to memory by means of a Read Header and Data command. The header compare may be inhibited by setting the HCI bit in the RMOF register.

2.5 GENERAL PROGRAMMING INFORMATION

2.5.1 Clearing the Controller

The controller has the following clearing methods:

a. Controller Clear - Controller Clear is performed by writing a 1-bit into the CLR bit (bit 05 of RMCS2) or Q-Bus INIT. This causes the following to be cleared:

- o RMCS1 bits <15:12>, <10:08>, <06:00>; RMCS2 bits <15:07>, <05:00>; RMBA bits <15:00>; RMBAE bits <05:00>; RMCS3 bits <15:04>. Sets RMCS2 bit 06 and RMCS1 bit 07.

- o In all drives: RMER1; RMER2; RMDA; RMAS ATA bit; RMEC2; RMDS ATA, ERR and LST bits; RMMR1 bits <15:04>, <02:00>. Sets bit 03 of RMMR1.

b. Error Clear - The Error Clear is performed by writing a 1-bit into the TRE bit (bit 14 of RMCS1). This causes a clearing of RMCS1 bits 13 and 14, bits <15:08> of RMCS2 and bits <15:11> of RMCS3. Clears the SC bit (bit 15 of RMCS1) if RMAS=0.

c. Drive Clear - The Drive Clear is a command (Code 11). This causes the following registers in the drive selected by U2-U0 to be cleared:

- • RMER1; RMER2; RMAS ATA bit; RMEC2; RMDS ATA and ERR bits; RMMR1 bits <15:04>, <02:00>. Sets bit 03 of RMMR1.

2.5.2 Interrupt Conditions

The controller generates an interrupt on the following conditions:

a. Upon termination of data transfer if interrupt enable is set when the controller becomes ready.

b. Upon assertion of attention or occurence of a controller error (SC being set) while the controller is not busy and the interrupt enable is set.

c. When the program writes 1 into IE and RDY at the same time. Note that this can be done by Read-Modify-Write instructions (BIS, BIC, etc.) which set the IE bit.

2.5.3 Termination of Data Transfers

A data transfer which has been successfully started may terminate in the following ways:

a. Normal Termination - Word count overflows to 0 and the controller becomes ready at the end of the current sector.

b. Controller Error - An error occurs in the RMCS2 register bits <15:08>. Any of these errors sets TRE which terminates the data transfer immediately and makes the controller ready.

c. Drive Error - The ERR bit in the RMDS register and at least one bit in an RMER1 or RMER2 register are set. TRE is also set and the controller becomes ready. The ATA for the drive doing the data transfer becomes asserted.

d. Program-Caused Abort - By performing a Controller Clear or a RESET instruction, the program can cause an abort of any operation. Status and error information is lost when this is done, and the controller and drive become ready immediately.

2.5.4 Ready Bits

RDY is the ready indicator for the controller. When RDY = 1, the controller is ready to accept a data transfer command. RDY is reset when the controller is doing a data transfer command. DRY is the ready indicator for the selected drive and is the complement of the drive's GO bit. To successfully initiate a data transfer command, both of these bits must be asserted. However, a non-data transfer command (Search, Drive Clear) may be issued to a drive at any time DRY is asserted regardless of the state of the RDY bit.

When a data transfer command is successfully initiated, both RDY and DRY become negated. When a non-data transfer command is successfully initiated, only DRY bit becomes negated.

The assertion of RDY after the execution of a data transfer command will not occur until the DRY bit is set and the controller is done. RDY is asserted on the completion of the last memory cycle (or at the time of an abort condition) and the last disk transfer.

If any command other than Drive Clear is issued to a drive which has ERR asserted, the command is ignored by the drive. If a Data Transfer command is issued to a drive which has ERR asserted, the drive does not execute the command and the missed transfer error (MXF, bit 09 in RMCS2 register) is set.

2.5.5 22-Bit Memory Addressing

Twenty-two-bit addressing capability is available as an option for the SC03/B1. The Emulex part number for the option kit is SC0313002. The kit consists of a single AMD2908 IC which is placed in socket U150 on the SC03 PCBA.

The controller can be switched from an RH11 mode (18-bit addressing) to an RH70 mode (22-bit addressing) by closing SW2-3. This will allow access to the RMBAE and RMCS3 registers which are a part of the RH70 only.

WARNING

Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing an SC03 with the extended addressing option in such a system will damage the option IC. Before installing the option confirm that there is neither positive nor negative potential between lines BC1, BD1, BE1, BF1 and logic ground. An SC03 without the addressing option will not be damaged if power is present on those lines.

2.5.6 Line Time Clock (LTC)

The Line Time Clock is a 60 Hz clock generated by the power supply and distributed on the backplane as the BEVNT signal. A high to low transition of this signal interrupts the processor. BEVNT has the highest external interrupt priority; only processor interrupts have higher priorities. If external interrupts are enabled (PS bit 07 = 0), the processor PC (R7) and PS words are pushed onto the processor stack. The LTC (or external event device) service routine is entered by vector address 100; the usual interrupt vector adddress input operation by the processor is not required since vector 100 is generated by the processor.

The LTC can be software controlled by using the Line Clock Register on the SC03/B1. The Line Clock Register has a bus address of 777546. It is a one-bit, write-only register. Reads to this register return all-zero data. Bit 06 is the only bit implemented. A write to this register with bit 06 set enables the line clock. A write to this register with bit 06 reset disables the line clock. The enable bit need not be set again after an interrupt has been processed. The clock will continue to interrupt until bit 06 is reset or an INIT is generated.

See paragraph 3.4.4.4 for information on how to configure the processor for use with the LTC.

2.5.7 Bootstrap Routines

Installing the Emulex bootstrap option kit (number SC0313001) makes available two bootstrap routines: the standard console bootstrap and auto-boot sequence. See paragraph 3.4.4.2 for installation instructions, and section 6 for operating instructions.

2.6 DUAL CONTROLLER OPERATION

SMD drives may be equipped with a dual port option which provides the capability for two controllers (generally on separate computers) to access the drive. The SC03/B1 controller supports this type of operation as a standard feature. This mode of controller operation is selected by setting SW2-6 ON. Most of the

dual port funtions of the DEC controller being emulated are supported, and those which are not should be transparent to a properly written dual port driver. Table 2-4 summarizes the controller register responses in dual port operation.

2.6.1 Dual Port Drives

The two drive ports are known as Channel I and Channel II. Because only one controller may access the drive at a time, access is granted on a first-come, first-served basis. Once a controller has gained access to the drive, the other controller is denied access until the first controller's operation is complete. However, each channel has a physical disable switch which can disable the port and prevent the associated controller from having access to it.

2.6.2 Unseized State

The drive is in the unseized state when it is not connected to either controller. The CPU must issue a request for the controller to seize the drive. This request is done in one of the following ways:

a. Writing into any drive register, including read-only registers.

b. Writing a one-bit into the drive's ATA bit in RMAS. The bit does not have to be set.

2.6.3 Seized State

The drive is seized when it is logically connected to one of the controllers. At that time DVA (RMCS1, bit 11) is set indicating that the drive is ready to communicate with the controller which has seized it. If the drive has already been seized by the other controller, then the DVA bit will not set, all the drive registers will read as zeros and any write to a register will be ignored. Attempts to seize a drive which is busy with the other port are remembered and then acted upon when the drive is released by the other controller.

2.6.4 Returning to the Unseized State

The drive is released and returned to the unseized state by issuing a release command. In addition, a one second timer in the controller will timeout and release the drive if one of the events listed in section 2.6.2 for seizing the drive is not performed periodically to keep resetting the timeout timer. Reading the RMCS1 register will also reset the timeout timer if the drive is currently seized. This allows the CPU to check a drive's seized state, and if seized, not have to worry about a time-out release occurring.

When the controller sees a previously busy drive becoming unseized, it checks its request flag. If the flag is set (the drive had been

requested while busy on the other port), the controller will seize the drive and set ATA causing an interrupt to the CPU if the IE bit is set. If the CPU does not respond to the attention within one second the drive will be released, but ATA remains set.

2.6.5 DEC Compatibility

The SC03/B1 controller differs from the equivalent DEC controller in three important areas.

First, there is no neutral state. Since the SC03 does not have instantaneous access to all drives at the same time (a limitation of the daisy-chained A cable and the microprocessor organization of the controller), the controller assumes the drive is busy on the other port if the controller has not already seized it. Thus, a read of RMCS1 will always indicate that the drive is seized by the other controller (DVA, bit 11 equals zero) unless the drive has been previously requested. The CPU must request the drive by writing into any drive register and wait until the ATA bit is set which indicates that the controller has seized the drive. If the drive was in reality not seized by the other controller, this will happen almost immediately. The DEC controllers, however, can switch from neutral to seized state within the time required to do a single read or write of a drive register. Thus, if the drive is not already seized, no ATA is set and the drive is immediately available to the seizing controller.

Second, the release command is not instantaneous since the controller takes a few microseconds to execute the command. During this time the drive will appear to be unseized.

Third, during a data transfer the timeout timers will not operate and the drives can not be polled to see if they are not busy. Therefore no drives are seized or released during the execution of a data transfer.

The software driver should not issue a Release command and then attempt to save the current status of a drive, since the Release command will immediately show the drive in the unseized state, thus returning zero data for the drive registers. In order to allow the other controller time to poll the drive, the CPU should not communicate with any of the released drive's registers until required to seize the drive again.

2.6.6 Dual Port Drives in Single Port Mode

When using an operating system which does not have dual port drive software support, it may still be advantageous to use dual port drives while operating in the controller in single port mode. This will allow for a non-dynamic type of operation between two CPUs. In this type of operation the controller does not unseize the drive and, in effect, it is seized by both controllers all the time.

The one second timeout timer (and the release command) operate exactly as stated in Paragraph 2.6.4. Even when released, a drive will still appear to be seized to the releasing controller. No attention is generated when the other controller finds the drive not busy. Should a command be issued to a controller while a drive is busy on the other port, the controller will wait until the drive becomes unbusy before executing the command. No timer exists in this case.

This mode of operation eliminates the need for manually switching the drive from one controller to another.

2.6.7 Dual Access Mode

In order to provide compatibility with dual access software, the dual access mode is provided (SW2-7 ON). When in this mode, the controller sets Dual Port Mode (Drive Type Register) and Programmable (Drive Status Register) to imitate the DEC neutral state.

When DPM and PGM are set, the operating system will attempt to seize a drive by simply writing a command to it. If the drive is unbusy the command is executed. If the drive is already busy on its other port, the controller simply waits until it is released and then seizes and commands it. Software timers are sufficently long to prevent causing a timeout when it is forced to wait.

The first time the SC03 sees a drive, it is ignored for one second. This one-second stall occurs once for each drive on the controller. It prevents the controller from seeing erroneous status information when power is applied to the drive after the controller has been powered-up. For a drive in dual port mode the stall will prevent the other CPU from accessing the drive until the stall completes. The dual access option switch bypasses the stall in all cases. For proper system operation with the dual access option switch ON, all drives must have power applied before either controller is powered-up.

Setting the Dual Port Option switch overrides the Dual Access Option.

2.6.8 Dual Port Drives Busy Signal

When operating dual port drives it is necessary to unbias the busy signal. This is accomplished by setting SW2-9 OFF (open). When operating single port drives it is necessary to bias-off the undriven busy signal. This is accomplished by setting SW2-9 ON (closed). In two-drive configurations both drives must be of the same type (i.e., either both dual port or both single port dives). A dual port drive cannot be properly run with a single port drive that does not drive the busy signal on the A cable.

Table 2-3
Register Access on Dual Controller Operation

Controller Action Drive State:	Response With Respect To Action On Ch. I
Read RMCS1	
Drive Not Seized:	Reads the controller portion of the RMCS1 only. The drive's portion is read as all zeros. No request flag is set.
Drive Seized by Ch. I:	DVA = 1; reads the register. Resets timer.
Drive Seized by Ch. II:	Reads the controller portion of RMCS1 only. The drive's portion is read as all zeros. No request flag is set.
Read any other drive register	
Drive Not Seized:	Reads all zeros.
Drive Seized by Ch. I:	Reads the register.
Drive Seized by Ch. II:	Reads all zeros.
Write RMCS1	
Drive Not Seized:	The function code is attempted if GO = 1. A port request flag is set.
Drive Seized by Ch. I:	Loads the function code. (Switches to unseized if the function is a Release).
Drive Seized by Ch. II:	The function code is attempted if GO = 1. A port request flag is set.
Write any drive register	
Drive Not Seized:	The write is ignored, and a port request flag is set.
Drive Seized by Ch. I:	Loads the register.
Drive Seized by Ch. II:	The write is ignored, and a port request flag is set.

Section 3
INSTALLATION

This section describes the step-by-step procedure for installation of the SC03/B1 Disk Controller in an LSI-11 system. The following list is an outline of the procedure. Each step corresponds to a second level heading in this section (i.e., item one, Inspect the SC03, is covered in paragraph 3.1).

Emulex recommends that Section 3 be read in its entirety before installation is begun.

1. Inspect the SC03.
2. Prepare the disk drives.
3. Prepare the LSI-11.
4. Configure the SC03.
5. Install the SC03.
6. Route the drive I/O cables.
7. Test the system.

3.1 INSPECTION

A visual inspection of the board is recommended after unpacking. Specific checks should be made for such items as bent or broken connector pins, damaged components or any other visual evidence of physical damage. The PROMs should be examined carefully to insure that they are firmly and completely seated in their sockets.

3.2 DISK DRIVE PREPARATION

3.2.1 Drive Placement

Uncrate and install the disk drives according to the manufacturer's instructions. Position and level the disk drives in their final places before beginning the installation of the SC03. This allows the I/O cable routing and length to be accurately judged. Place the drives side by side to make installation of the daisy-chained cable simpler.

3.2.2 Local/Remote

The LOCAL/REMOTE switch controls whether the drive can be powered up from the drive (local) or the controller (remote). Place the switch in the REMOTE position. With the LSI-11 powered down, press

the START switch on the front panel of each of the drives (the START LED will light, but the drive will not spin up and become ready). When the LSI-11 is powered up, the drives will spin up sequentially. This prevents the heavy current draw that would be caused if all of the drives were powered up at once. When in the remote mode the drives will power down when the LSI-11 is powered down. While the LSI-11 is powered ON, the drives may be powered up and down individually (to change disk media, for example) using the drive START switch.

3.2.3 Sectoring

See Appendix A, Configuration Selection, for the correct sector count settings for the disk drives in use. The exact method of entering the sector count differs from one drive manufacturer to another and the particular drive manual should be consulted for the exact procedure. A minimum of 609 bytes per sector are required for proper operation.

3.2.4 Index and Sector Pulse Selection

The SC03 controller is designed to have the Index and Sector signals on the daisy chained A cable and the signals must be gated by the unit select logic within the drive.

3.2.5 Unit Addressing

An ID plug in the range of 0-1 should be placed in the drive. Be careful that the drives do not have the same number. Some drives have their address selected by means of switches on one of the logic cards and do not use an ID plug. See the drive manuafacturer's manual for details.

3.2.6 Lark Drive Configuration

With SC03/B1 firmware revisions A and B, SW2-5 on the SC03 must be ON for Lark drive compatibility. Revision C of the SC03 firmware makes the compatibility automatic as long as the Seek-On-Head-Select switch on the Lark drive is ON. See the Lark drive hardware maintenance manual.

3.3 SYSTEM PREPARATION

3.3.1 Powering Down the System

Power down the system and switch OFF the main AC breaker at the rear of the cabinet (the AC power indicator will remain lit). Slide the CPU out of the cabinet and remove the top cover. Tilt the card cage up to obtain access to the CPU and other modules.

3.4 CONTROLLER SETUP

Several configuration setups must be made on the controller before inserting it into the chassis. These are made by SW1, SW2 and SW3.

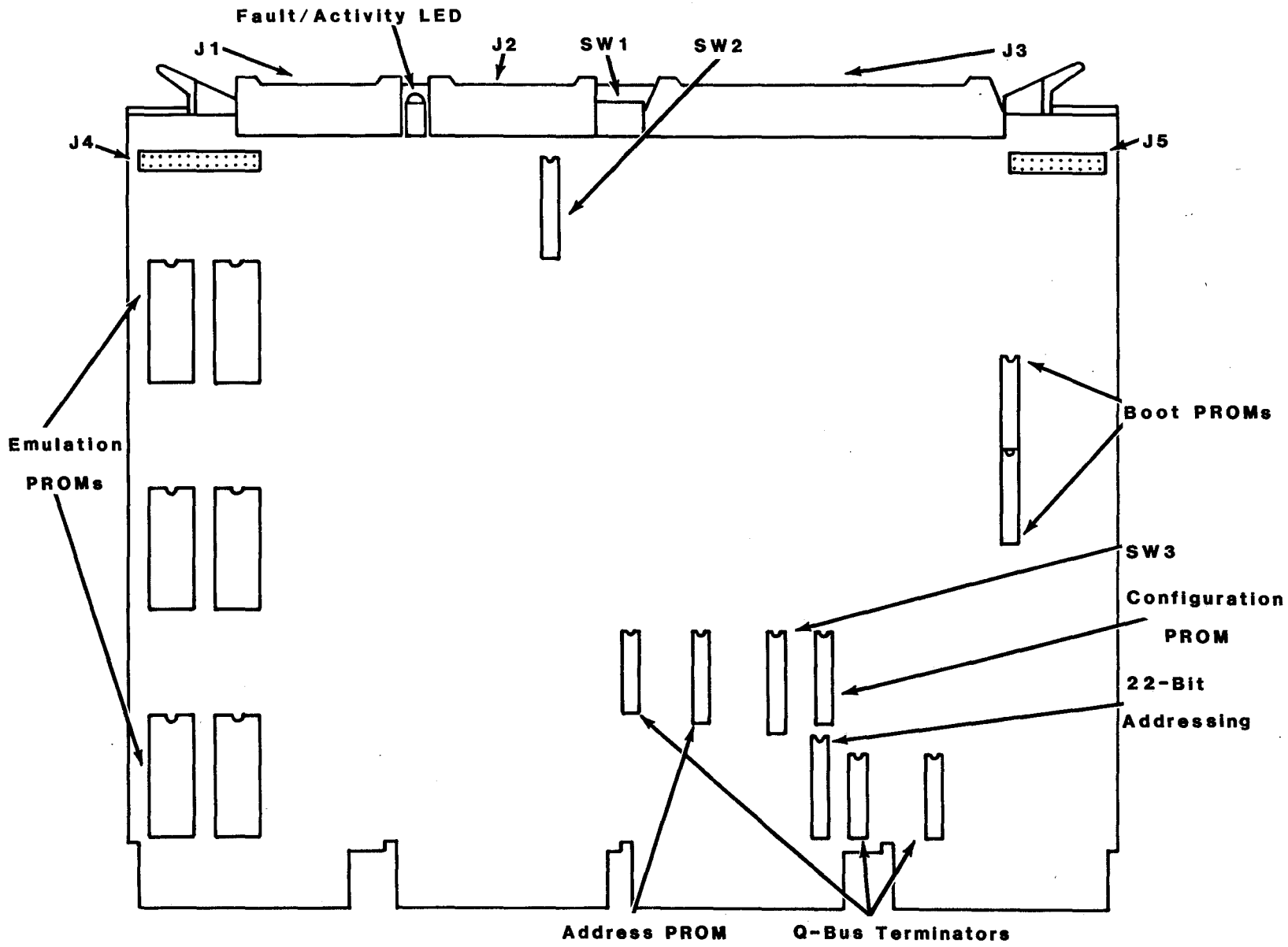


Figure 3-1 SC03 Controller Assembly

3.4.1 Controller Address Selection

All Q-Bus controllers have a block of several command and status registers through which the system can command and monitor the controller. The registers are addressed sequentially from a starting address assigned to that device type, in this case a disk controller.

The starting address for the controller's Q-Bus registers is selected by DIP switch SW3. A normal starting address of 776700 is obtained by placing switch SW3-8 in the ON position. An alternate address of 776300 is available by closing SW3-7. Both SW3-7 and SW3-8 must not be closed at the same time.

3.4.2 Interrupt Vector Address

The interrupt vector address is selected by means of SW1-4, SW2-1 and SW2-2. The standard vector address is 254. The alternates are 50, 150, 270, 274, 354, 370 and 374. Listed below are the switch settings for the standard and alternate interrupt vector addresses.

SW1-4	SW2-2	SW2-1	Vector
O	O	O	254 (Standard)
O	O	C	150 (Alternate)
O	C	O	370 (Alternate)
O	C	C	374 (Alternate)
C	O	O	354 (Alternate)
C	O	C	50 (Alternate)
C	C	O	270 (Alternate)
C	C	C	274 (Alternate)

3.4.3 Drive Configuration Selection

The phrase "drive configuration selection" describes the process that is used to configure the SC03 to use a particular type of physical disk drive to perform the RM02, RM03, RM05, or RM80 emulation. That is, you have a particular set of physical disk drives. You must tell the controller what kind of physical disk drives you are going to use. On the SC03, switches SW3-1 through SW3-6 are used for that purpose.

For ease of manual maintenance the configuration table for the SC03 is contained in Appendix A.

3.4.4 Options

There are a number of other SC03 options that can be implemented by the user. These features are selected by physically installing the option on the PCBA or enabling it using one of the option switches.

3.4.4.1 Q-Bus Terminator Option

To provide the equivalent of 120 ohms electrical termination to the Q-Bus, DIP resistor networks are installed in U122, U151, and U153. These resistor packs provide a 180 ohm resistor connection to +5 volts and a 390 ohm resistor connection to ground on each Q-Bus line.

These three resistor networks may be ordered from Emulex or the customer may provide his own terminating resistor networks by using an equivalent part such as BOURNS P/N 4116R-003-181/391, or BECKMAN 898-5-R180/390, or CTS 761-5-R181/391.

WARNING

> Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing an SC03 with the Q-Bus Terminator Option in such a system will damage the option ICs. Before installing the option confirm that there is neither positive nor negative potential between lines BC1, BD1, BE1, BF1 and logic ground. If there is power on any of the above lines and you wish to use the terminator option, cut pins 2, 3, 4 and 5 of the IC in socket U151. An SC03 without the option will not be damaged if power is present on those lines.

3.4.4.2 Bootstrap PROM Option

The Bootstrap Option is a firmware routine executed by the CPU that loads the system memory with software that is stored on disk or tape. The option kit consists of two pairs of PROMs. Its Emulex part number is SC0313001. See section 6 for operating information. This feature is enabled by opening (OFF) SW3-9 on the SC03 PCBA.

The bootstrap option has two sections; standard console bootstrap and auto-boot. The standard console bootstrap routine is entered by the CPU at address 773000, DEC's conventional starting address. The auto boot sequence is entered at address 765000.

The LSI-11 and LSI-11/02 both require that power-up mode 2 be selected to take advantage of the standard console bootstrap option. This is done by installing jumper W6 and removing jumper W5 on the CPU PCBA. The configuration for both the LSI-11 and the LSI-11/02 is the same. The auto-boot routine is not available for these units.

The LSI-11/23 may be configured to take advantage of either the standard console boot or the auto-boot routines. This CPU also requires that power-up mode 2 be selected (install jumper W6 and remove jumper W5 on the CPU PCBA). The bootstrap starting address, however, is selected using jumpers W8 through W15. To select the standard console bootstrap routine install W8. This will cause the

processor to default to starting address 773000. To use the auto-boot option, remove W8, W10 and W12; install W9, W11, W13, W14 and W15. To use this option on an LSI-11/23 PLUS, a jumper connection must be made from J15 to J10 on the CPU PCBA.

3.4.4.3 22-Bit Memory Addressing

Twenty-two-bit addressing capability is available as an option for the SC03. The Emulex part number for the option kit is CS0113001. The kit consists of a single AMD2908 IC which is placed in socket U150 on the SC03 PCBA. The controller can be switched from RH11 (18-bit) mode to RH70 (22-bit) mode by closing SW2-3. See paragraph 2.5.5 for programming instructions.

WARNING

> Some manufacturers of Q-Bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing an SC03 with the extended addressing option in such a system will damage the option IC. Before installing the option confirm that there is neither positive nor negative potential between lines BC1, BD1, BE1, BF1 and logic ground. An SC03 without the addressing option will not be damaged if power is present on those lines.

3.4.4.4 Line Time Clock Option

The Line Time Clock Option allows program control of the Line Time Clock. This feature is enabled by opening (OFF) SW3-10 on the SC03 PCBA. See paragraph 2.5.6 for programming instructions.

Before the LTC can be used, the CPU must be configured to enable that feature. On the LSI-11 and LSI-11/02, remove jumper W3 (BEVNT Line Enable). On the LSI-11/23, remove jumper W4 (BEVENT Line Enable). The LTC switch on the front panel must also be ON.

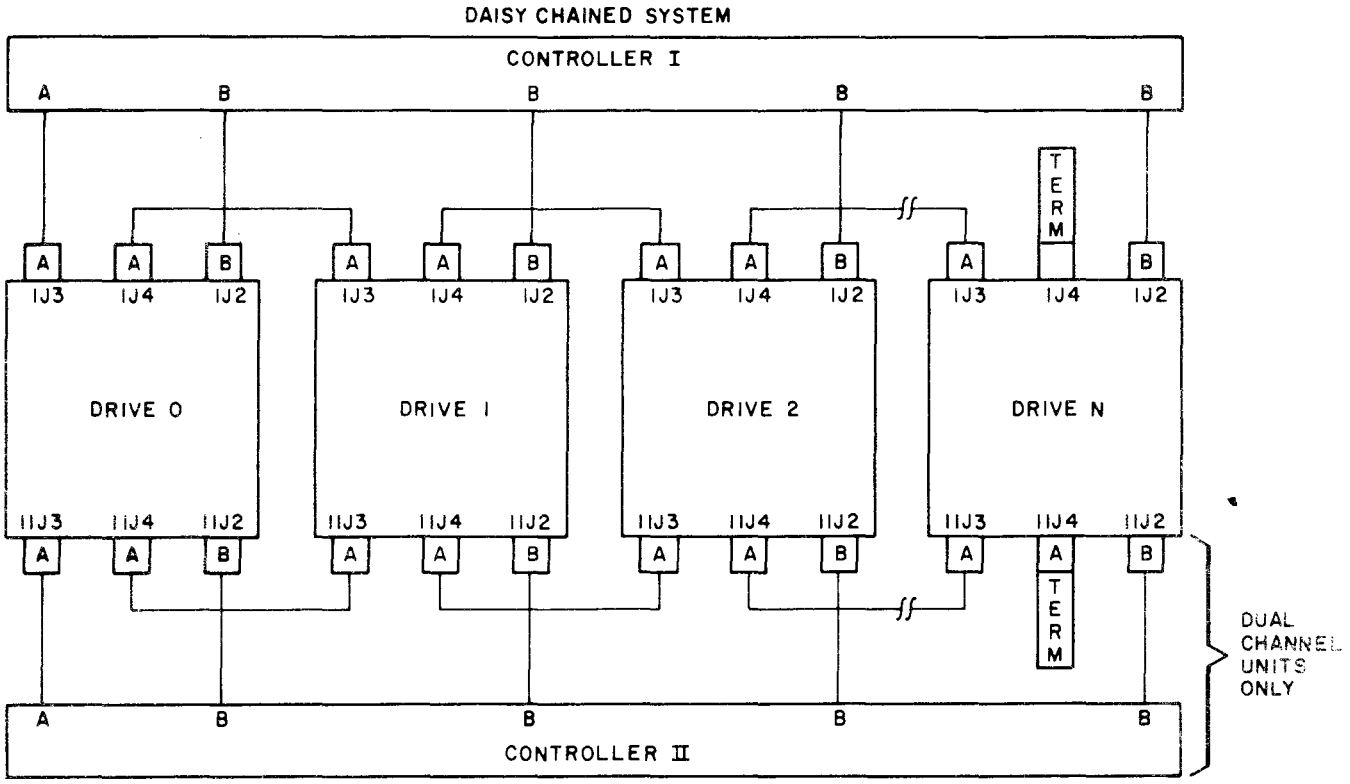
When using the SC03 with the RSTS operating system, the Line Time Clock Option must be enabled (SW3-10 = open). The CPU should be configured to enable the option.

3.5 PHYSICAL INSTALLATION

3.5.1 Slot Selection

If the three optional Q-Bus terminator resistor networks are installed, the SC03 should be installed in a quad slot such that it provides the termination required at the end of the bus.

If the optional Q-Bus terminators are not installed, the SC03 may be assigned to any desired slot since it uses the LSI four-level interrupt scheme to perform distributed interrupt arbitration.



NOTES:

1. MAXIMUM INDIVIDUAL A CABLE LENGTHS = 100 FEET
2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET

Figure 3-2 Cabling Schematic

SC0301-0001

3.5.2 Mounting

The controller board should be plugged into the LSI-11 backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the boards with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly positioned in the throat of the connector before attempting to seat the board by means of the extractor handles.

3.6 CABLING

The subsystem cabling of the drives and controller is shown in Figure 3-2.

3.6.1 A Cable

The 60-wire A cable should be plugged into the large connector on the controller and wired to the first drive. If more than one drive is used, it is then daisy-chained to the other drives. The last drive on the A cable must have a terminator installed. This part is available from the drive manufacturer. The terminator is generally plugged into one of two A cable connectors on the drive. In some cases, a ground wire emerging from the terminator assembly

will have to be connected to the drive to provide a ground return for the resistors in the terminator. Pin 1 of the board connector is on the right. Pin 1 of the cable connector has a notch on the connector body to identify it. Twist and flat cable will have brown-brown twist followed by red-brown twist on the pin 1 edge of the cable. The cable will normally egress to the rear of the controller.

NOTE: The connector is not keyed and can be physically reversed in the header. No damage should result, but the system will not operate.

3.6.2 B Cable

Each drive must have a 26-wire B cable wired from the drive to one of the B ports of the controller. It makes no difference which B port connection is used by a drive. No external terminators are used with the B cable. Pin 1 of the cable connector has a notch on the connector body to identify it. The pin 1 edge of the cable has a black stripe. Pin 1 of the board connector is on the right.

NOTE: Observe the same caution on connector reversal given in paragraph 3.6.1.

3.6.3 Grounding

For proper operation of the disk subsystem, it is very important that the disk drives have a good ground connection to the logic ground of the computer. The ground connection should be a 1/4 inch braid (preferably insulated) or AWG No. 10 wire or larger. The grounding wire may daisy-chain between drives. If the drive has a switch or jumper which connects the logical signal ground to the cabinet ground (DC ground to AC ground), this connection should be removed once the drive is put on-line with the controller. It can be connected for performing local off-line maintenance on the drive.

NOTE: Failure to observe proper grounding methods will generally result in marginal operation with random error conditions.

3.7 TESTING

Note: The register addresses given below are 18-bit addresses. For 22-bit machines add 17000000 to obtain the correct address for each register (i.e., 776700 becomes 17776700).

3.7.1 Self-Test

When power is applied to the CPU, the controller automatically executes a built-in self-test. This self-test is not executed with every bus INIT but only on powering up. If the self-test has been executed successfully, the LED on the top edge of the controller board will be OFF or flashing. The LED flashes when the controller cannot properly address at least one drive after successfully

executing its self-test. This will occur if the A and B cables are not properly plugged in, a drive is not powered up with a code plug, or two drives have an identical code plug. If the LED is ON steadily the controller did not pass its self-test and the controller cannot be addressed from the CPU.

3.7.2 Register Examination

After powering up the CPU and noting that the LED indicator is not ON steadily, a quick check should be made to ensure that the controller registers can be read from the computer console. The Control Status Register 1 (RMCS1) 776700 will contain 004200 if the controller and drive 0 are ready and the drive is plugged into the controller.

3.7.3 Hardware Formatting the Disk

The controller has the means to format the disk by writing headers and zero data in all sectors of the disk. This command does not verify the data or headers.

If the drive is on line, the formatting is carried out as follows:

1. Perform a subsystem clear by depositing 000040 into RMCS2 (776710).

2. Select the drive to be formatted by depositing the drive number in the three least significant bits of RMCS2 (776710).

3. Deposit a pack acknowledge command (23) in RMCS1 (776700).

4. Deposit a 1777777 in RMHR (776736).

5. Deposit a hardware format command (77) in RMCS1 (776700) to start formatting. The Activity LED will be lit during the format. The operation will finish in a couple of minutes with the RDY bit set in RMCS1.

3.7.4 Diagnostics

The SC03/B1 will run the following DEC diagnostics on LSI-11 computers.

- ZRMA Formatter
- ZRMB Performance Exerciser
- ZRMC Functional Controller, Part I*
- ZRMD Functional Controller, Part II*
- ZRME Functional Controller, Part III*
- ZRMF Extended Drive Test
- ZRMI Drive Compatibility Test

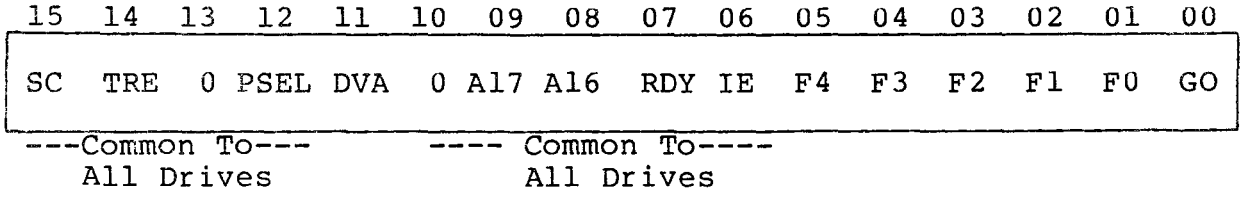
The diagnostics marked with an asterisk require certain patches to bypass unsupported maintenance functions. All diagnostics require patches to run with drive sizes other than that of a standard RM02/RM03. See Appendix B for diagnostic patches.

Emulex provides self-sizing diagnostics for the SC03. They are listed at the end of Appendix B.

There are 22 device registers in the SC03/B1. These are used to interface the controller to the drives and the computer. The registers are loaded and/or read under program control in order to initiate selected disk commands and monitor status and error conditions. Most registers can be written into with word or byte operations.

The RMWC, RMBA, RMCS2, RMBAE, RMCS3, RMDB and bits <15:12> and <10:06> of RMCS1 are common to all drives. Loading and reading of these registers is independent of the unit selected. A separate set of the other registers and bits 11 and <05:00> of RMCS1 exists for each of the drives. Loading and reading of these registers is dependent on the drive selected by the unit number in RMCS2. In addition, the eight ATA bits in RMAS are each associated with an individual drive. Any attempt to write into the drive registers (except RMAS) while the drive's GO bit is asserted will cause a register modification refused error and the register is not modified.

4.1 CONTROLLER/STATUS REGISTER 1 (RMCS1) 776700



The RMCS1 register can be read or written by program control, and is used to store the current disk command function code and operational status of the controller.

Setting the GO bit will cause the controller to recognize the function code in the register and initiate the operation for the corresponding drive. The actual start of execution of the command does not begin when the function code is loaded into the control register but commences when the controller has finished any previous operation and polls through the drive RMCS1's in search of a command needing initiation.

If a drive is currently seized (see 2.6.3), reading RMCS1 will reset the timeout timer.

Special Condition (SC) - Bit 15

This read only bit is set as long as TRE in RMCS1 or any of the drive's ATA bits are set. This bit causes a CPU interrupt if IE is also set.

Transfer Error (TRE) - Bit 14

This read/write bit is set by DLT, WCE, UPE, NED, NEM, PGE, MXF, or a drive error during a data transfer. Writing a 1 into the bit causes the controller error bits in RMCS2 to be cleared. They are also cleared at the start of every data transfer operation.

Port Select (PSEL) - Bit 12

This is a read/write bit that has no effect on any controller operations. (It is for diagnostic compatibility). This bit cannot be written into when the controller is operating in RH70 mode.

Drive Available (DVA) - Bit 11

This read-only bit is set when the drive is seized by the controller. When not in dual port mode, the drive is seized as long as it is powered-up.

Extended Bus Address (A16, A17) - Bits 08, 09

Upper extension of the RMBA register. This two-bit counter is incremented by one every time RMBA overflows. These bits cannot be altered if RDY = 0 and no error results when attempted. They appear as bits 00 and 01 of RMBAE when the controller is operating in RH70 mode.

Ready (RDY) - Bit 07

This read-only bit is reset when the controller starts a Data Transfer Command (codes 51 - 77) and is set at the termination of the data transfer.

Interrupt Enable (IE) - Bit 06

When IE is set an interrupt can be generated when RDY is asserted at the end of a data transfer or by any ATA being asserted. It is reset automatically when the interrupt is accepted by the CPU. When a zero is written into IE by the program, any pending interrupts are cancelled. An interrupt is generated by writing 1's into IE and RDY at the same time. This bit is replicated in RMCS3 when the controller is operating in RH70 mode.

Function Code (F4-F0) - Bits <05:01>

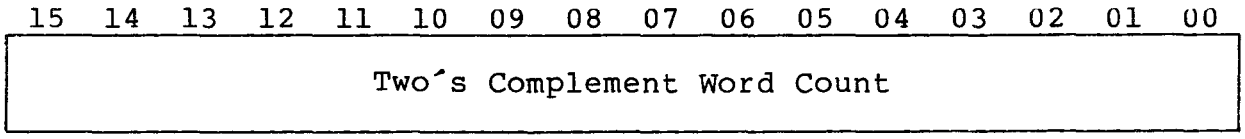
F4-F0 and the GO bit make up the function (command) code which determines the action to be performed by the controller and drive as shown below:

01	No Operation	25	DMA Bandwidth Set (Optional)
05	Seek Command	31	Search Command
07	Recalibrate	51	Write Check Data
11	Drive Clear	53	Write Check Header and Data
13	Release	61	Write Data
15	Offset Command	63	Write Header and Data
17	Return to Centerline	71	Read Data
21	Read-In Preset	73	Read Header and Data
23	Pack Acknowledge	77	Format (Optional)

GO (GO) - Bit 00

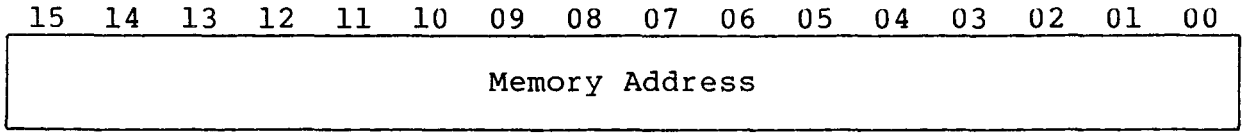
The GO bit must be set to cause the controller to respond to a command. The GO bit is reset after command termination.

4.2 WORD COUNT REGISTER (RMWC) 776702



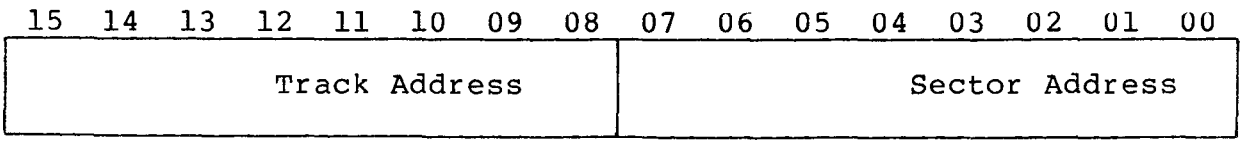
The RMWC register is loaded with the two's complement of the number of data words to be transferred to or from main memory. The register is incremented by one after each word transferred, and accommodates a maximum transfer of 65,536 words. The RMWC register is not cleared by INIT or controller clear.

4.3 Q-BUS ADDRESS REGISTER (RMBA) 776704



The RMBA register is initially loaded with the low-order 16 bits of the memory address for a data transfer. The low-order bit (00) is always forced to a zero. The RMBA register is incremented by two after transfer of a word to or from memory, unless the BAI bit is set.

4.4 DISK ADDRESS REGISTER (RMDA) 776706



This register is used to address the sector and track on the disk to or from which a transfer is desired. It can only be loaded as a word. The RMDA is incremented each time a sector of data is transferred so that consecutive blocks are automatically addressed

when the word count indicates that more than one block is to be transferred. At the end of a transfer, RMDA contains the address of the sector following the last one involved in data transfer.

The RMDA contains an eight-bit sector counter providing up to 256 sectors per track. The register also contains an 8-bit track counter which is incremented by one every time the sector counter overflows. When the sector address and the track address reach their maximum counts, they are reset to 0 and the RMDC is incremented by one. The invalid address error (IAE, RMER1, bit 10) is set if the address in the RMDA is invalid when a data transfer, Seek, or Search function is initiated. The maximum sector, track and cylinder addresses are obtained from the selected configuration. Typically, the number of sectors per track is 32 (31 for RM80).

4.5 CONTROL/STATUS REGISTER 2 (RMCS2) 776710

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	WCE	UPE	NED	NEM	PGE	MXF	MDPE	OR	IR	CLR	PAT	BAI	U2	U1	U0

The RMCS2 register can be read or written under program control and is used to store the current drive select code and controller operational status. In addition, the register can initiate a controller clear operation. It is recommended that writes to the unit select bits be done with byte-writes since two of the error bits in the upper byte are read/write, when the controller is operating in RH11 mode.

Data Late (DLT) - Bit 15

This bit cannot normally be set because of the fourteen sector buffer in the controller. It can be set by accessing RMDB without the appropriate status bit (06 or 07) in RMCS2 set to a 1. This is a read-only bit.

Write Check Error (WCE) - Bit 14

Set when the controller is performing a write check operation and a word from the disk does not match the corresponding word in memory. When the mismatch occurs, the reading of the disk terminates and the WCE bit is set. The memory address displayed in RMBA is the address of the word following the one which did not match (if BAI is not set). The mismatched data word on the disk is displayed in the data buffer (RMDB). This is a read-only bit.

Q-Bus Parity Error (UPE) - Bit 13

Set if a parity error occurs in the Q-Bus memory while the controller is performing a write or write check command. When the error occurs, the RMBA register contains the address of the word

following the word with the parity error (if BAI is not set). This is a read/write bit only if the controller is operating in RH11 mode.

Nonexistent Drive (NED) - Bit 12

Set when the program reads or writes a device register associated with a drive (selected by U2-U0) which is not recognized because of a wrong code plug, not powered up, or is non-existent. This is a read-only bit.

Nonexistent Memory (NEM) - Bit 11

Set when the controller is performing a DMA transfer and the memory does not respond within 10 microseconds. The memory address displayed in RMBA is the address of the word following the memory location causing the error. This is a read-only bit.

Program Error (PGE) - Bit 10

Set when the program attempts to initiate a data transfer operation while the controller is currently performing one. This is a read-only bit.

Missed Transfer (MXF) - Bit 09

Set if a data transfer cannot be executed (RMDS ERR bit = 1). This is a read/write bit only if the controller is operating in RH11 mode.

Massbus Data Bus Parity (MDPE) - Bit 08

This read-only bit is always a zero.

Output Ready (OR) - Bit 07

Set when a word is present in RMDB and can be read by the program. Cleared by reading RMDB. Any attempt to read RMDB register before OR is asserted will cause a DLT error. This is a read-only bit.

Input Ready (IR) - Bit 06

This read-only bit is always a 1.

Controller Clear (CLR) - Bit 05

When a 1-bit is written into this bit position, the controller is initialized (Paragraph 2.5.1). This is a write-only bit. It is always read as a zero.

Parity Test (PAT) - Bit 04

This read-write bit has no effect on any controller operation. (For diagnostic compatibility.)

Q-Bus Address Increment Inhibit (BAI) - Bit 03

When BAI is set, the controller will not increment the RMBA register during data transfers, causing all data words to be read from or written into the same memory location. This is a read/write bit.

Unit Select (U2-U0) - Bits <02:00>

These bits select one of eight logical units for communicating with the CPU. The unit select bits can be changed at any time without interfering with the current operations. These are read/write bits.

4.6 DRIVE STATUS REGISTER (RMDS) 776712

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATA	ERR	PIP	MOL	WRL	LST	PGM	DPR	DRY	VV	0	0	0	0	0	OFM

This register contains various status indicators for the drive selected by the unit number in RMCS2. The register is a read-only register.

Attention Active (ATA) - Bit 15

An attention condition will set the ATA bit in this register and the Attention Summary register (RMAS). It is cleared by INIT, controller clear, loading a command with the GO bit set or loading a 1-bit in RMAS register coresponding to the drive's unit number. The last method of clearing the ATA bit will not clear the error indicators.

An attention condition is caused by: an error in the error registers; the completion of a positioning operation; the change of state of the MOL bit; dual port operation with the drive presently available if previously not available; correct sector identification for the Search command.

Error (ERR) - Bit 14

Set when one or more of the errors in the error registers (RMER1 or RMER2) for a selected drive is set. While ERR is asserted, commands other than Drive Clear are not accepted.

Positioning in Progress (PIP) - Bit 13

Set when a positioning command is accepted. These commands are: Seek, Recalibrate, and Search. Cleared when the moving function is completed at the time the DRY and ATA bits are set. Also set if MOL is reset for all emulations except RM80.

Medium On-Line (MOL) - Bit 12

Set when the unit ready line from the drive is asserted indicating that the drive is up to speed, the heads are positioned over the recording tracks and no fault condition exists within the drive. Cleared when the spindle is powered down or the drive is off-line. Whenever the MOL bit changes state, the ATA bit is set.

Write-Lock (WRL) - Bit 11

Set when the write protected line from the drive is asserted as enabled by a switch located on the drive. A write command on a write-locked drive will cause the write-lock error (WLE, bit 11 of RMER1) to be set. For RM80 emulations: set if MOL is reset.

Last Sector Transfer (LST) - Bit 10

Set when the last addressable sector on the disk pack has been read or written. Cleared when a new write to RMDA is received.

At the time LST is set, the RMDA register is reset to 0 and the RMDC register increments by one to the first illegal cylinder address. If the RMWC register is not 0, a mid transfer seek is aborted which will cause the AOE status bit (RMER1, bit 09) to be set, indicating that the desired cylinder register overflowed during a read or write.

Programmable (PGM) - Bit 09

This bit is set when dual port or dual access operation is enabled.

Drive Present (DPR) - Bit 08

This bit is set if the controller has seized the drive and is reset when the other controller has seized the drive. This bit is a reflection of the DVA bit in RMCS1.

Drive Ready (DRY) - Bit 07

Set at the completion of every command and cleared at the initiation of a command. When set, this bit indicates the readiness of the drive to accept a command. If a mechanical movement command was initiated, the ATA bit will also be set when DRY is set. This bit is the complement of the drive's GO bit.

Volume Valid (VV) - Bit 06

Set by the Pack Acknowledge or Read-In Present commands. Cleared whenever the drive cycles up from the OFF state. When reset, this bit indicates that the drive has been off-line and a disk pack may have been changed.

Offset Mode (OFM) - Bit 00

Set by the offset command to indicate that a read will be done with the heads in the offset position as determined by RMOF bit 07. Cleared by a Read-in Preset, Return-to-Centerline, Recalibrate or write command, or a mid-transfer seek.

4.7 ERROR REGISTER 1 (RMER1) 776714

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DCK	UNS	OPI	DTE	WLE	IAE	AOE	HCRC	HCE	ECH	WCF	FER	PAR	RMR	ILR	ILF

The RMER1 register is a read/write register that is used to store the error status of the drive whose unit number is in RMCS2. The RMER1 register can only be written as a word. Any attempt to write a byte will cause an entire word to be written. If the program attempts to write into this register while the drive is busy, an RMR (RMER1 register, bit 02) error is set, and the contents of the register are not otherwise modified. Writing 0's into this register should not be used as the normal way of clearing errors. The Drive Clear command should be used instead.

Data Check (DCK) - Bit 15

Set during a read operation when the ECC hardware detects an ECC error. The data transfer terminates with the current sector. If the Error Correction Inhibit (ECI) bit is off, the controller will go into the error correction process, and the RDY bit will not be set until the end of the process. If ECI bit is on, the error correction process is inhibited, and the RDY bit is set at the end of the sector.

Unsafe (UNS) - Bit 14

This bit is a composite error bit of the unsafe and seek incomplete error conditions in the RMER2 register. With UNS set, correct results on any operation cannot be guaranteed. Some faults must be cleared by manual intervention at the drive.

Operation Incomplete (OPI) - Bit 13

Set when a read or write command involving header search cannot find the physical sector within three index pulses. Also set during a search operation where a sector count match is not made within three index pulses. When OPI is set, the GO bit is cleared and the RDY bit is set.

Drive Timing Error (DTE) - Bit 12

Set when either the header or data sync pattern is not found. When DTE is set, the GO bit will be cleared and the RDY bit set. Also

set if a sector pulse occurs before the end of a sector's data field.

Write Lock Error (WLE) - Bit 11

Set when a write command is issued to a write-locked drive.

Invalid Address Error (IAE) - Bit 10

Set when the address in RMDC or RMDA is invalid and a Seek, Search or data transfer command is initiated.

Address Overflow Error (AOE) - Bit 09

Set when the RMDC register overflows during a read or write operation indicating that the address has exceeded the cylinder/address limit. With AOE set, the controller will terminate the operation when the last sector of the last cylinder has been read or written.

Header CRC Error (HCRC) - Bit 08

Set by a CRC error in the header. If a CRC error is detected during a read or write command, the controller will not make any data transfer. In the event of a CRC error during a read/write-check header and data command, the entire sector will be transferred with the HCRC bit set.

Header Compare Error (HCE) - Bit 07

Set when the first two words of the header read at the sector whose count is equal to the desired sector field of RMDA do not match the contents of RMDC and RMDA. If the HCE bit is set during a read or write command, the controller will not perform any data transfer. In the event of a read/write-check header and data command, the entire sector will be transferred with the HCE bit set.

ECC Hard Error (ECH) - Bit 06

Set when the error correction procedure indicates that the error was a non-correctable ECC error. DCK (Bit 15) is also set. This bit will never be set if ECI is on.

Write Clock Fail (WCF) - Bit 05

This bit is normally a zero unless written into.

Format Error (FER) - Bit 04

Set if the FMT16 bit in RMOF does not match bit 12 in word one of a sector's header. Although the controller implements both 18-bit and 16-bit formats, all sectors contain 256 16-bit words in either format. If FER is set, then HCE may not be set.

Parity Error (PAR) - Bit 03

This bit is normally a zero unless written into.

Register Modification Refused (RMR) - Bit 02

Set when a write is attempted to any drive register (except RMAS or RMMR1) with DRY=0. The drive will continue to execute the command in progress.

Illegal Register (ILR) - Bit 01

This bit is normally a zero unless written into.

Illegal Function (ILF) - Bit 00

Set when the function code in RMCS1 is illegal and the GO bit is set.

4.8 ATTENTION SUMMARY REGISTER (RMAS) 776716

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	ATA 7	ATA 6	ATA 5	ATA 4	ATA 3	ATA 2	ATA 1	ATA 0

The RMAS register allows the program to examine the attention status of all drives with only one register read operation. It also provides a means of resetting the attention logic in a selected group of drives. The eight low-order bits of this register correspond to the ATA bits in the RMDS of the drive having the same unit number as the bit position of this register.

A drive's ATA bit can be reset by loading a 1 into the bit position corresponding to the drive's unit number. Loading a 0 has no effect. For a program to use the RMAS without losing status information, the program must use MOV instructions for all writes to this register. An instruction that does a read-restore (such as BIS) may cause bits that became asserted just prior to the read to be lost. This register can be read or written at any time.

A persistent error, just like any error condition, will cause the ATA bit to be reasserted. Attempts by the controller to clear the error will not work in this case.

4.9 LOOK-AHEAD REGISTER (RMLA) 776720

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	Sector Counter							0	0	0	0	0	0

The RMLA register contains the drive sector counter and is used to present the angular position of the disk relative to the read/write heads for the disk whose unit number appears in RMCS2. The purpose of this register is to provide the programmer with a means of optimizing disk accesses by minimizing rotational delays. The counter counts from 0 to the maximum logical sector number (usually 31).

4.10 DATA BUFFER (RMDB) 776722

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Data Buffer															

The RMDB register provides a maintenance tool to check the controller data paths. The IR (input ready) and OR (output ready) status indicators in RMCS2 registers are provided so that the programmer can determine when words can be read from or written into RMDB.

RMDB is used as an access to the Silo Buffer for an RH11. This controller has no Silo Buffer. All writes to this register are ignored. If a write-check error occurs, the data word as read from the disk is placed in RMDB and the OR bit in RMCS2 is set. Reading RMDB resets OR. Any further attempts to read RMDB will create a DLT error.

4.11 MAINTENANCE REGISTER 1 (RMMR1) 776724

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	MUR	MOC	MSER	MDF	0	0	MWP	0	0	DMD

RMMR1 is a read/write register that allows a program to simulate various signals from the disk for diagnostic testing of the controller. The DMD bit must be set before any other bit has an effect on the controller. This register may be written into as a word or a byte. Writing to RMMR1 can occur at any time regardless of the status of the drive. A drive or controller clear resets this register except for bit 03, which is set.

Maintenance Unit Ready (MUR) - Bit 09

Set by a diagnostic program to simulate the Unit Ready signal from the drive.

Maintenance On Cylinder (MOC) - Bit 08

Set by a diagnostic program to simulate the On Cylinder signal from the drive.

Maintenance Seek Error (MSER) - Bit 07

Set by a diagnostic program to simulate the Seek Error signal from the drive.

Maintenance Drive Fault (MDF) - Bit 06

Set by a diagnostic program to simulate the Fault signal from the drive.

Maintenance Write Protect (MWP) - Bit 03

Set by a diagnostic program to simulate the Write Protect signal from the drive.

Diagnostic Mode (DMD) - Bit 00

Set by the diagnostic program to reconfigure the drive into maintenance mode. None of the other bits in this register have any effect on the controller unless DMD is 1. Before a drive can be set to maintenance mode, it must first be ready and not busy. No positioner motion is initiated for a Seek, Home, Search or Implied Seek and all data transfer commands are ignored.

4.12 DRIVE TYPE REGISTER (RMDT) 776726

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	MOH	0	DPM	0	0	0	Drive Type Code							

Moving-Head (MOH) - Bit 13

This bit is always a 1 indicating that the drive is a moving head device.

Dual Port Mode (DPM) - Bit 11

This bit signifies that the drive is operating in dual port mode as enabled by SW2-6, or in dual access mode as enabled by SW2-7.

Drive Type Code - Bits <07:00>

This code specifies the type of drive as follows:

24 - RM03, 25 - RM02, 26 - RM80, 27 - RM05.

4.13 SERIAL NUMBER REGISTER (RMSN) 776730

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SW2 -8	SW2 -7	SW2 -6	SW2 -5	SW2 -4	SW2 -3	SW2 -2	SW2 -1	Firmware Rev.				Port No.			

The purpose of the RMSN register was to distinguish a drive from similar drives attached to the controller by means of a four decade serial number. Here it consists of the controller port number for which the drive is attached, the firmware revision level, and the eight SW2 switch settings.

4.14 OFFSET REGISTER (RMOF) 776732

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	FMT 16	ECI	HCI	SSEI	0	OFS 7	0	0	0	0	0	0	0

The RMOF register contains three inhibit bits and the drive offset direction bit. The offset direction bit determines if a read will be done with the heads advanced or retarded from normal centerline position. The actual offset determination is done by the status of RMDS bit 00. All bits of this register are cleared by Read-in Preset command.

Format Bit (FMT16) - Bit 12

Set for 16 bit mode and reset for 18 bit mode. Since the controller only handles 16 bits/word format, this bit should always be a 1.

Error Correction Code Inhibit (ECI) - Bit 11

Set to inhibit error correction when an ECC error is detected. See paragraph 4.7, bit 15.

Header Compare Inhibit (HCI) - Bit 10

Set to inhibit header compare and CRC check. With HCI set, the controller depends only on the sector count for sector identification. It is recommended that the HCI bit be reset during a write operation.

Skip Sector Error Inhibit (SEI) - Bit 09

For RM80 emulations only. Set to inhibit skip sector errors during a header check. When this bit is set the drive operates with 32 sectors per track. This bit is reset whenever a data transfer command increments RMDA to a new track address. This bit cannot be set unless the FMT 16 bit is already set.

Offset Direction (OFS7) - Bit 07

Set under software control to select the direction of positioner offset. A one retards the heads and a zero advances the heads.

4.15 DESIRED CYLINDER REGISTER (RMDC) 776734

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Desired Cylinder Address										

The RMDC register contains the address of the cylinder to which the positioner is to move. The RMDC register will be cleared by the Read-in Preset command. Following an initial load, the value in the RMDC register will be incremented by 1 whenever the RMDA register is reset to 0 during a data transfer. When the RMDC register is incremented and the RMWC register is not equal to 0, a mid-transfer seek is initiated by the controller.

The Invalid Address Error (IAE) bit will be set when, upon asserting the GO bit, the RMDC register contains an address greater than the largest addressable cylinder.

4.16 HOLDING REGISTER (RMHR) 776736

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RMHR is a read-only register that always returns a zero when read except as follows: If the register is written into with one of the values listed below, it is possible to read out the configured size of the selected disk from the same register.

100027 - Maximum cylinder address
100030 - Maximum track address
100031 - Maximum sector address

Writing a 177777 into the register enables the optional Format command to be executed when loaded into RMCS1. The enable is cleared when any data transfer command terminates. The maximum sector address is dependant upon the status of the FMT16 bit in the RMOF register. For an RM80, it is dependant upon the status of both the FMT16 and the SSEI bits.

4.17 MAINTENANCE REGISTER 2 (RMMR2) 776740

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
11777_8															

RMMR2 is a read-only register that always returns 11777_8 when read.

4.18 ERROR REGISTER 2 (RMER2) 776742

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BSE	SKI	OPE	IVC	LSC	LBC	MDS	0	DVC	ACU	SSE	0	DPE	0	0	0

Error Register 2 is a read/write register that contains status information relating to the electromechanical performance of the drive whose unit number is in RMCS2. This register may be written as either a word or a byte. If any bit is set in this register, then the ERR bit in RMDS is also set. In some cases, the UNS bit in RMER1 will also be set. Writing zeros into this register should not be used as the normal way of clearing errors. A drive clear or a controller clear should be used instead. If the program attempts to write into this register while the drive is busy, the RMR bit in RMER1 will be set and the write will be ignored.

Bad Sector Error (BSE) - Bit 15

Set whenever the controller detects a zero in bit 14 or 15 of the first header word and the HCI bit in RMOF = 0. HCE in RMER1 may also be set.

Seek Incomplete (SKI) - Bit 14

Set whenever a Seek Error is received from the drive. This error also sets the UNS bit in RMER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive if a Seek Error is detected.

Operator Plug Error (OPE) - Bit 13

Set whenever the drive's address plug is removed and then reinstalled. This bit can be cleared by issuing a drive clear.

Invalid Command (IVC) - Bit 12

Set whenever any command is issued to a drive with MOL = 0. Set whenever any command except a Read-in Preset or a Pack Acknowledge is issued to a drive with VV = 0.

Loss of Sector Clock (LSC) - Bit 11

Set when the controller detects more than 127 Sector pulses without an Index pulse.

Loss of Bit Clock (LBC) - Bit 10

Set if the controller does not detect at least 16 servo clocks within 3.0 microseconds.

Multiple Drive Select (MDS) - Bit 09

Set when more than one drive responds to a logical address on the A cable. This bit cannot be set by a program.

Device Check (DVC) - Bit 07

Set if a Fault indication is received from the drive. This error also sets the UNS bit in RMER1. The controller automatically issues a Fault Clear and a Return-to-Zero to the drive if a Fault is detected.

AC Power Unsafe (ACU) - Bit 06

Set if an ACLO indication is received from the Q-Bus.

Skip Sector Error (SSE) - Bit 05

For RM80 emulations only. Set whenever bit 13 of the header Word One is set and bit 09 of RMOF is reset. This error indicates that the sector has been skipped and the data resides in the next sector. This bit cannot be written into unless the drive is an RM80.

Data Parity Error (DPE) - Bit 03

This bit is normally a zero unless written into.

4.19 ECC POSITION REGISTER (RMEC1) 776744

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	ECC Position												

The Error Correction Code (ECC) Position register is a read-only register that contains the position of the error pattern as determined by the ECC correction procedure. The error position is the number of bit positions from the beginning of the sector's data field to (and including) the right-most bit position of the error pattern stored in RMEC2. If the detected error is not correctable using ECC, the ECH error bit in RMER1 will be set.

4.20 ECC PATTERN REGISTER (RMEC2) 776746

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	Error Pattern										

The Error Correction Code (ECC) Pattern register is a read-only register that contains the 11-bit error correction pattern obtained from the ECC correction procedure. A 1 in the error pattern indicates a bit of the data in memory from the last read sector

which is in error. The error pattern may straddle two 16-bit words in memory. The bit displacement to the right most bit of the pattern is determined by the bit count in RMEC1. The actual correction is done by an exclusive-OR of the error pattern and the data in memory.

4.21 BUS ADDRESS EXTENSION (RMBAE) 776750

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	A21	A20	A19	A18	A17	A16

This register contains the upper 6 bits of the memory address which is combined with the lower 16 bits in RMBA to form the complete 22-bit address. The 6-bit field is incremented each time the RMBA overflows. Note that A16 and A17 are replicated in RMCS1. Writing in either affects both. This register is accessible only when the controller is operating in RH70 mode.

4.22 CONTROL/STATUS REGISTER 3 (RMCS3) 776752

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	DPE HI	DPE LO	WCE HI	WCE LO	0	0	0	0	IE	0	0	IP 3	IP 2	IP 1	IP 0

This register is accessible only when the controller is operating in the RH70 mode.

Data Parity Errors (DPE HI and LO) - Bits 14 and 13

Set if parity error is detected on data read from memory when performing a write or write check command. Also sets UPE in RMCS2.

Write Check Errors (WCE HI and LO) - Bits 12 and 11

Set if data fails to compare between memory and the disk on a write check command. Also sets WCE of RMCS2.

Interrupt Enable (IE) - Bit 06

When IE = 1, an interrupt may occur due to RDY or SC being asserted. Cleared when the interrupt is recognized. Writing 0 into IE by the program cancels any pending interrupts. This bit is replicated in RMCS1. Writing into either affects both.

Invert Parity (IP3:IP0) - Bits <03:00>

These bits are used to invert and test cache parity on a DEC RH70 controller. They have no effect on the Q-Bus.

BLANK

Operations are initiated on the drive selected by the unit select bits in RMCS2 by loading the function code and GO bit into RMCS1. The function code specifies a specific command. The commands can be divided into three categories: data transfer commands, positioning commands, and housekeeping commands. Commands and their corresponding function codes (always odd since the GO bit must be asserted to execute the command) are described below:

5.1 DATA TRANSFER COMMANDS

These commands involve data transfers to or from the disk and are designated by function codes 51 through 77.

All data transfer commands have seek and sector search functions implied. When the desired cylinder does not equal the current cylinder during the execution of the data transfer, a seek will be issued to the desired cylinder. The controller will then search the desired track for the desired sector and, when found, will start the data transfer. On all commands except the Write Header and Data command (which is the format operation) and Read/Write-Check Header and Data command, a match of the sector header must be made before the data transfer is started. If the header compare inhibit (HCI bit 10 in RMOF) is set, the header will not be compared or checked and, like the Write Header and Data command, the transfer will be started based on the pre-recorded sector pulses. With the HCI bit set, header errors will not be reported. With the HCI bit cleared, the transfer will be aborted if a header error is detected. The Read/Write-Check Header and Data command aborts only the transfers following the sector that caused the error.

The desired sector, track and cylinder addresses are updated after the transfer of a sector. Therefore, at the end of a transfer, the disk is set up to transfer the next sequential sector. This allows multiple sector transfers and spiral transfers across tracks and cylinders. When the desired cylinder address changes during a transfer, the implied seek is performed and is termed a mid-transfer seek.

The data transfer commands are described below:

5.1.1 Write Check Data (51)

This command reads data from the selected drive and compares it on a word by word basis with that obtained from memory. If the data fails to compare, the WCE status bit is set and the command is terminated immediately. For additional information on write check errors see Section 4.10 and the WCE bit in Section 4.5.

5.1.2 Write Check Header and Data (53)

This command reads the header field and data field from the selected drive and compares it on a word by word basis with data obtained from memory. If the header and data fail to compare, the WCE status bit is set and the command is terminated immediately.

5.1.3 Write Data (61)

This command writes the 256-word data field of the selected sector with words obtained from memory. A two word ECC is appended to each sector. If the word count in RMWC goes to zero during the sector, the rest of the sector is zero filled. After a sector transfer the word count in RMWC is checked, and if not zero, the data transfer operation is continued to the next sector; otherwise the command is terminated by setting the RDY bit.

5.1.4 Write Header and Data (format operation) (63)

This command writes the 2-word header field and the 256-word data field of the selected sector with words obtained from memory. A one word CRC is appended to each header field, and a two word ECC is appended to each data field. After a sector transfer the word count in RMWC is checked, and if not zero, the data transfer operation is continued to the next sector; otherwise the command is terminated by setting the RDY bit. If RMWC goes to zero during the sector, the rest of the sector is zero filled.

5.1.5 Read Data (71)

This command reads the 256-word data field from the selected sector and transfers the data to memory. When the sector data transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RMOF is reset) to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction information. Assuming no data errors, the word count in RMWC is checked; if not zero, the data transfer operation is repeated with the next sector. If RMWC goes to zero during the sector, the rest of the sector is not transferred.

5.1.6 Read Header and Data (73)

This command transfers the 2-word sector header field and the 256-word data field from the selected sector to memory. When the sector data transfer is complete, the ECC is checked to ensure that the data read from the disk was error free. If a data error occurred, the ECC correction procedure is initiated (if the ECI bit in RMOF is reset) to determine whether the error is correctable. When finished, the command is terminated to allow software to apply the correction information. Assuming no data errors, the word count in RMWC is checked; if not zero the data transfer operation is repeated with the next sector.

5.2 POSITIONING COMMANDS

Positioning commands are mechanical movememt commands used to position the heads over the disk pack and take milliseconds to complete. Upon initiating the positioning commands, the controller will set the PIP bit and reset the DRY bit. Upon completion of the positioning operation, the controller resets the PIP and GO bits, sets the DRY bit and sets the ATA bit. The positioning commands are described below:

5.2.1 Seek Command (5)

This command causes the heads to be moved to the cylinder address specified by the contents of RMDC. When the controller sees the Seek command with the GO bit set, it sends the cylinder address to the corresponding drive. Any attempt to write into RMDC while the seek is in progress will cause the RMR bit to be set and RMDC will not be modified. Upon completion of the seek operation, the ATA and DRY bits in RMDS are set, and the GO bit is reset. If the drive is unable to complete a move within 500 milliseconds or if it has moved the carriage to a position outside the recording field, the drive asserts the seek error signal and the controller sets the SKI error bit in RMER2 and the ERR, ATA and DRY bits in RMDS. The controller will automatically issue a Fault Clear and a Return-to-Zero to the drive so that a Drive Clear command can clear the error.

5.2.2 Recalibrate (7)

This command will cause the drive positioner to position the heads over cylinder 0. A Return-to-Zero is automatically performed with each head load sequence, and whenever a Fault or Seek Error is detected. This command clears the OFM bit in RMDS.

5.2.3 Offset Command (15)

This command causes the OFM bit in RMDS to be set. Subsequent reads will be done with the heads offset from track centerline in the direction specified by RMOF bit 07. This operation offers additional data recovery attempts over that provided by the ECC capability when an ECC error is detected. If an ECC hard error occurs, two offset positions should be used. At the completion of the offset command, the ATA bit is set indicating that a read command should be issued to the cylinder and track in order to recover data.

The OFM bit in RMDS will be cleared by any one of the following:

a. Seek to another cylinder by means of implied or mid-transfer seek.
b. Write command.
c. Return-to-centerline command.
d. Recalibrate command.
e. Read-in preset command.

5.2.4 Return-to-Centerline Command (17)

This command is used to clear the OFM bit and set the ATA bit in RMDS. It also resets OFS7 in RMOF.

5.2.5. Search Command (31)

The search command causes the controller to first perform a seek to the desired cylinder and then compare the sector counter with the desired sector in the RMDA register. When they match, it sets the ATA bit causing an interrupt to the computer if IE in RMCS1 is set. An unsuccessful completion of a search command occurs when a sector count and desired sector address match is not made during the interval of three index pulses, in which case the OPI bit is set.

5.3 HOUSEKEEPING COMMANDS

Housekeeping commands are used to place drive logic into a known or initialized state and usually take only a few microseconds to execute. The housekeeping commands are listed below.

5.3.1 NO OP (1)

This command does not perform any operation, except to clear the ATA bit.

5.3.2 Drive Clear (11)

This command causes the following registers and conditions associated with the drive selected by the unit select bits in RMCS2 to be cleared: ATA and ERR in RMDS, RMER1, RMER2, RMEC2, RMMR1 (except bit 03 which is set) and ATA bit in RMAS.

5.3.3 Release Command (13)

This command performs a drive clear function, and then releases the drive for use by the other port when in dual port mode of operation.

5.3.4 Read-In Preset (21)

This command sets the VV (volume valid) bit, clears the RMDC and RMDA registers, clears the RMOF register, and clears the OFM bit in the RMDS register.

5.3.5 Pack Acknowledge (23)

This command sets the VV bit for the command controller. This command or a Read-in Preset command must be issued before any data transfer or positioning command can be given if the pack has gone off-line and then on-line (i.e., MOL change of state). It is primarily intended to avoid unknown pack changes.

5.4 OPTIONAL COMMANDS

The Format command can be executed only after writing a 177777 into RMHR.

5.4.1 Format (77)

This command executes a Return-to-Zero; clears RMDC, and RMDA; and formats the entire pack in standard format. Each sector has bits 15, 14, and the FMT16 bit set in Header Word 1 and an all 0's data field. RMDC will be set to the last cylinder number plus one at completion, the LST bit in RMDS will be set, and the FMT16 bit in RMOF will be set.

5.4.2 DMA Bandwidth Set (25)

This command requires option switch SW2-8 to be ON. The switch has a dual purpose: it activates the DMA bandwidth control during DMA transfers, and it makes this command code legal. This command allows the program to alter the amount of delay time between DMA bursts on a drive-by-drive basis. If ERR = 0 and DRY = 1 for the drive selected via RMCS2, then this op code takes the contents of RMWC, treats it as an unsigned 16-bit positive number, and saves it for use during subsequent data transfer operations. Each count equals a delay of 0.6 microseconds with a count of 0 = 0.9 microseconds. Any number in the range 0-65535(10) is legal. This results in a delay range of 0.9 microseconds to 39.33 milliseconds in 0.6 microsecond increments. Each drive is individually programmable, and a default count of twelve (8.0 microseconds) is preset at power-up time. This delay is in addition to the 3.3 microseconds of delay between DMA bursts that is fixed in the firmware as system overhead.

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6.1 OVERVIEW

The Bootstrap PROM Option Kit is available for use with the SC03/B1 in an LSI-11 computer system environment. The kit consists of two sets of two PROMs. One PROM set is for interactive ODT Bootstrap applications and the other is for unattended Auto Bootstrap operations. The kit's Emulex part number is SC0313001.

The two PROM sets are described in the following subsections:

Subsection	Title
6.2	ODT Bootstrap Operation
6.3	Auto Bootstrap Operation

Installation instructions for both PROM sets are given in subsection 3.4.4.2.

NOTE

Do not use this option with the MicroVAX I or MicroVAX II. This option is not designed for use with those CPUs.

These bootstrap PROMs contain a memory test, cache test, and bootstrap routines that allow the system to be bootstrapped from most DEC disk and tape subsystems. The option kit contains two sets of PROMs as listed in Table 6-1.

Table 6-1. Bootstrap Option Kit PROMs

Set Number	PROM Number	SC03 Socket	Description
1	B02 B03	U92 U71	ODT Bootstrap
2	B04 B05	U92 U71	Auto Bootstrap

6.2 ODT BOOTSTRAP

The ODT Bootstrap set uses Console ODT to query the operator for the boot device. This option is useful if you frequently need to boot from a variety of subsystems.

This option allows the user to bootstrap the system from the desired device by entering the two-letter device mnemonic on the console terminal. Table 6-2 lists the supported boot devices and their two-letter mnemonics.

Table 6-2. ODT Boot Devices

Mnemonic	Boot Device
DB	RM02/03/05/80
DB	RP04/05/06
DU	EMULEX MSCP CONTROLLERS*
DM	RK06/07
DL	RL01/02
MS	TS11/TSV05/TQK25**
MT	TM11

* Emulex only. Will not boot DEC devices.
** Unit zero only.

All boot devices must be at the standard address and vector for that device type.

The ODT Bootstrap PROM set supports the following CPUs:

- 11/23
- 11/23+
- 11/73
- 11/73+

The ODT Bootstrap Option performs the following functions:

- The option determines the type of CPU in the system.
- It performs a memory test on the first 28K bytes of memory in the system.
- If the program finds an 11/73, it tests the cache memory for proper operation. If a cache error occurs the program prints a message informing the operator and disables the cache to allow system operation without the cache.
- The option performs a Flush Cache operation.
- No CPU tests are performed during bootstrap.

6.2.1 OPERATION

The ODT bootstrap option may be invoked in any of four ways:

- Power up
- Activating the RESTART switch on the front panel of the CPU chassis
- Entering 173000G via the system console when the system is halted in ODT with the @ prompt displayed on the system console
- At the prompt (11/73+ only):

  Enter Boot Device: **BO B<return>**

  Enter "BO B" to cause the 11/73+ to begin executing the bootstrap routine in the SC03/B1.

After the memory and cache (where applicable) are complete, the program prints a $ prompt on the system console and waits for the operator to enter a two-letter device mnemonic followed by a carriage return. Choose one of the mnemonics listed in Table 6-2.

Once the device mnemonic is entered, the program tests for a valid device type and attempts to load the first two blocks of data from the device to memory, starting at location zero. If the device type is not valid, the program prints "?" and another $ prompt on the console and waits for new input. If the desired device is valid but not present, the program prints a $ prompt on the console and waits for new input. If the desired device is present but the device is not ready (i.e., drive not online or spun up), the program goes into an infinite wait loop, retrying the operation.

When the desired device is brought online or spins up and becomes ready, the load takes place. If an error occurs during the load operation, the program goes into an infinite wait loop, retrying the operation. At this point, the operation can be stopped by halting the CPU or by performing a restart.

If the load operation is successful, the boot program jumps to location zero in memory and the CPU begins executing the program loaded there by the boot device.

6.3 AUTO BOOTSTRAP

The Auto Bootstrap set requires no operator intervention, unless the bootstrap attempt fails (no device, etc).

Table 6-3 lists the supported boot devices and their priority in the device search.

Table 6-3. Auto Bootstrap Device Priority List

Mnemonic	Boot Device
DB	RM02/03/05/80, RP04/05/06
DU	EMULEX MSCP CONTROLLERS*
DL	RL01/02
DM	RK06/07
MS	TS11/TSV05/TQK25

All boot devices must be at the standard address and vector for that device type.

The Auto Bootstrap PROM set supports the following CPUs:

- 11/23
- 11/23+
- 11/73

The Auto Bootstrap Option performs the following functions:

- The option determines the type of CPU in the system.
- It performs a memory test on the first 28K bytes of memory in the system.
- If the program finds an 11/73, it tests the cache memory for proper operation. If a cache error occurs the program prints a message informing the operator and disables the cache to allow system operation without the cache.
- The option performs a Flush Cache operation.
- No CPU tests are performed during bootstrap.

6.3.1 OPERATION

The Auto Bootstrap process may be invoked in any of three ways:

- Power Up
- Activating the RESTART switch on the CPU front panel.
- Entering 173000G on the system console when the CPU is halted in ODT with the @ prompt displayed on the system console.

Starting with the the first device in the table, the program attempts to load the first two blocks from drive zero to memory starting at location zero.

If the device is not present, not ready, or an error occurs during the load operation, the program steps to the next device in the table and retries the load operation. If the load operation is successful, the program checks the contents of location zero for the presence of a 2XX, 4XX, or 6XX. If one of these values is present, the program assumes that the bootstrap is probably a valid DEC bootstrap and jumps to location zero to begin executing the program loaded from the boot device. If the contents of location zero are not valid, the program steps to the next device in the table and retries the load operation.

If all the disk type devices in the table are tried without success, the program prints the message "NO BOOT DISK, LOAD MS BOOT TAPE" and tests for the presence of an MS tape device (TSV05, TQK25, or other LSI-11 TS11 emulation). If none is present, the program halts at location 173772. If an MS type device is present, the program enters an infinite loop, waiting for the device to be loaded and become ready. When this occurs, the program attempts a load operation from the tape device. If the load is successful, the program jumps to location zero and begins executing the program loaded from the boot tape. When using the tape load, the program does not check location zero for a valid boot block.

6.3.2 ALTERNATE BOOTSTRAP DEVICES

The Auto Bootstrap Option attempts to load only from drive zero of each available boot device. If you want to boot for a drive other than zero, or if you want to boot from a specific device without performing the memory test, the program allows for manual intervention bootstrap. This is accomplished by halting the CPU and using console ODT to load the desired drive number, device CSR, and starting address of the device boot code as follows.

1. Halt the CPU.
2. Load the drive number in R0.
3. Load device CSR in R1.
4. Enter the device boot address, followed by **G**

Example Boot from DR3

1. Halt the CPU.
2. Load 3 in R0.
3. Load **176700** in R1.
4. Enter **165364G** on the console.

This method assumes that the desired boot drive is ready and the media contains a valid boot block. If not, the results are unpredictable because the boot program will not have set up the pointers to its internal device table. Table 6-4 lists the device CSRs and starting addresses for all supported devices.

Table 6-4. Alternate Boot Device Address

Device	CSR in R1	Start Address
QUICK START (bypass mem test)	N/A	173434
RM02/03/05/80, RP04/05/06	176700	165364
EMULEX DU DEVICES	172150	173246
RL01/02	174400	165104
RK06/07	177440	165312
TS11/TSV05/TQK25	172522	173612

6.4 PROGRAM MESSAGES

During operation, the bootstrap option program prints a number of messages on the system console. Table 6-5 lists the messages and their meanings.

Table 6-5. Boot Option Messages

Message	Meaning
1173 Cache + Mem Test	CPU type and memory test performed.
1123 Mem Test Only	CPU type and memory test performed.
No Cache Response	1173 CPU Cache control register not functional.
Cache Parity Fail. Cache Disabled	Parity error detected while testing cache memory. Cache memory is disabled.
NXM in first 28 K	A bus time out trap occurred while testing the first 28K bytes of memory.
No Boot Disk. Load MS BOOT Tape	No bootable disk device was found on the system. The boot must be performed from an MS type device.
Halt at location 173772	The MS boot device is not on the system, or an attempt to load from the MS device resulted in an error. In this case, location 1762 contains the address of the MS device message buffer that contains the error status.

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APPENDIX A

SC03/B1 CONFIGURATION AND OPTION SELECTION

A.1 INTRODUCTION

To allow the SC03/B1 user maximum flexibility in disk drive selection, the SC03/B1 supports a wide variety of disk types. This appendix provides the switch settings which make possible this flexibility.

A.2 CONTROLLER CONFIGURATION

The SC03/B1 unit is capable of supporting a wide variety of disk drives. Switches SW3-1 to SW3-6 select the various configurations that are supported, and a list of these drive types and sizes may be found in Table A-1. Table A-2 gives the proper switch settings for each of the various configurations.

A.2.1 Physical vs Logical Disk Numbering

A primary feature of the SC03/B1 is its ability to emulate four DEC disk subsystems using only two physical disk drives. This is accomplished by mapping two logical disk subsystems onto one disk drive which contains twice as much capacity as the standard DEC subsystem. In the event of this usage the mapping of logical units onto physical units is as follows:

Physical Unit Number	Logical Unit Numbers
0	0 and 2
1	1 and 3

The physical/logical assignments for specific disk configurations can be found by comparing the Physical drive column to the Logical drive column in Table A-2.

A.2.2 Drive Configuration Selection

The SC03/B1 emulates four different DEC disk subsystems, the RM02, the RM03, RM05, and the RM80. The RM02 and RM03 have an unformatted capacity of 80 Mb. The RM05 has an unformatted capacity of 300 Mb, and the RM80 has an unformatted capacity of 160 Mb.

There are essentially three different types of drive configurations. With the first type each emulated DEC drive exists on one physical drive. In the second type two emulated drives are mapped onto one physical drive. The third type is a combination of the first two.

To find the configuration switch settings which are compatible with your system use the following process. Note that all configurations require that drives be set with the required number of hard sectors, (SEC column of Table A-1). See the manufacturer's installation manual for instructions.

1. Locate your drive type and size in Table A-1. Note the KEY assigned to each type of drive you intend to use.

2. Scan down the KEY column of Table A-2 until you find your drive's number. Check the corresponding emulation in the Logical Drive column. If the emulation is not one that you require, continue to scan the KEY column in search of the required emulation.

3. After finding a suitable match for Drive 0, check the drive key and type for Drive 1 for that configuration row. It is not necessary to use both drive ports.

4. When you have found an entire configuration which is suitable, set the configuration switches as indicated.

Table A-1
Drives Supported

Mfg.	Model	Key	Cyl	Trk	Sec	Configurations
Ampex	330	1024-16	1024	16	32	9,12,14
Ampex	93160	1645-05	1645	5	32	10
Ampex	93160M	1646-05	1646	5	32	11
CDC	9448-96	823-06	823	6	32	0A,0B,0C
CDC	9457	624-04	624	4	32	1C
CDC	9730-80	823-05	823	5	32	0,4,5,15,16,18,19,1B
CDC	9730-160	823-10	823	10	32	2,3,4,5,14,17,18,19
CDC	9760	411-05	411	5	32	0D
CDC	9762	823-05	823	5	32	0,4,5,15,16,18,19,1B
CDC	9766	823-19	823	19	32	1,7,8,0B,0C,15,1B
CDC	9775	842-40	842	40	32	6,7,8,13
Century	T82RM	823-05	823	5	32	0,4,5,15,16,18,19,1B
Century	T302RM	823-19	823	19	32	1,7,8,0B,0C,15,1B
Fujitsu	2280	823-05	823	5	32	0,4,5,15,16,18,19,1B
Fujitsu	2284	823-10	823	10	32	2,3,4,5,14,17,18,19
Fujitsu	2294	1024-16	1024	16	32	9,12,14
Fujitsu	2312	589-07	589	07	32	0E
Priam	3350	561-03	561	3	32	1F

Table A-2
Drive Configurations PROM# 697

CONF. NO.	SW3- 6	5	4	3	2	1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
00	O	O	O	O	O	O	823-05	0	32	0 = RM03	A
							823-05	1	32	1 = RM03	A
01	O	O	O	O	O	C	823-19	0	32	0 = RM05	A
							823-19	1	32	1 = RM05	A
02	O	O	O	O	C	O	823-10	0	32	0,2 = RM03	A
							823-10	1	32	1,3 = RM03	A
03	O	O	O	O	C	C	823-10	0	32	0 = RM80	A
							823-10	1	32	1 = RM80	A
04	O	O	O	C	O	O	823-05	0	32	0 = RM03	A
							823-10	1	32	1,3 = RM03	A
05	O	O	O	C	O	C	823-10	0	32	0,2 = RM03	A
							823-05	1	32	1 = RM03	A
06	O	O	O	C	C	O	842-40	0	32	0,2 = RM05	A
							842-40	1	32	1,3 = RM05	A
07	O	O	O	C	C	C	823-19	0	32	0 = RM05	A
							842-40	1	32	1,3 = RM05	A
08	O	O	C	O	O	O	842-40	0	32	0,2 = RM05	A
							823-19	1	32	1 = RM05	A
09	O	O	C	O	O	C	1024-16	0	32	0 = RM05	A
							1024-16	1	32	1 = RM05	A
0A	O	O	C	O	C	O	823-06	0	32	0,2 = RM03/RM02	B*
							823-06	1	32	1,3 = RM03/RM02	B*
0B	O	O	C	O	C	C	823-06	0	32	0,2 = RM03/RM02	B*
							823-19	1	32	1 = RM05	B*
0C	O	O	C	C	O	O	823-19	0	32	0 = RM05	B*
							823-06	1	32	1,3 = RM03/RM02	B*
0D	O	O	C	C	O	C	411-05	0	32	0 = RM03	A*
							411-05	1	32	1 = RM03	A*
0E	O	O	C	C	C	O	589-07	0	32	0 = RM03	A
							589-07	1	32	1 = RM03	A
0F	O	O	C	C	C	C	823-10	0	32	0 = RM03	A*
							823-10	1	32	1 = RM03	A*
10	O	C	O	O	O	O	1645-05	0	32	0 = RM03	A*
							1645-05	1	32	1 = RM03	A*
11	O	C	O	O	O	C	1646-05	0	32	0,2 = RM03	A
							1646-05	1	32	1,3 = RM03	A
12	O	C	O	O	C	O	1024-16	0	32	0 = RM05	A*
							1024-16	1	32	1 = RM05	A*
13	O	C	O	O	C	C	842-40	0	32	0 = RM05	A*
							842-40	1	32	1 = RM05	A*
14	O	C	O	C	O	O	823-10	0	32	0,2 = RM03	A*
							1024-16	1	32	1 = RM05	A*
15	O	C	O	C	O	C	823-05	0	32	0 = RM03	A
							823-19	1	32	1 = RM05	A
16	O	C	O	C	C	O	823-05	0	32	0 = RM02	B
							823-05	1	32	1 = RM02	B
17	O	C	O	C	C	C	823-10	0	32	0,2 = RM02/RM02	B
							823-10	1	32	1,3 = RM02/RM02	B

Table A-2 (con't)
Drive Configurations PROM# 697

CONF. NO.	SW3- 6	5	4	3	2	1	PHYSICAL KEY	Unit	SEC	LOGICAL Unit(s) = Dr Type	Rev
18	O	C	C	O	O	O	823-05	0	32	0 = RM02	B
							823-10	1	32	1,3 = RM02/RM02	B
19	O	C	C	O	O	C	823-10	0	32	0,2 = RM02/RM02	B
							823-05	1	32	1 = RM02	B
1A	O	C	C	O	C	O	589-07	0	32	0 = RM02	B
							589-07	1	32	1 = RM02	B
1B	O	C	C	O	C	C	823-05	0	32	0 = RM02	B
							823-19	1	32	1 = RM05	B
1C	O	C	C	C	O	O	624-04	0	32	0,2 = RM02	C*
							624-04	1	32	1,3 = RM02	C*
1D	O	C	C	C	O	C					
							Not Used				
1E	O	C	C	C	C	O					
1F	O	C	C	C	C	C	561-03	0	32	0 = RM03	A*
							561-03	1	32	1 = RM03	A*

*These configurations have a non-standard cylinder and/or track number and are not supported by DEC Diagnostics or DEC operating systems. [Bey are supported by Emulex self-sizing diagnostics.

A.3 USER SELECTABLE OPTIONS

Several other options including the register starting address for the SC03/B1 can be user selected. The factory switch settings are listed in Table A-3. The functions of the switches that select those options are defined in Tables A-4, A-5 and A-6, below.

TABLE A-3
SC03 FACTORY SWITCH SETTINGS

Switch	Setting	Switch	Setting	Switch	Setting
SW1-1	OFF	SW2-1	OFF	SW3-1	OFF
SW1-2	OFF	SW2-2	OFF	SW3-2	OFF
SW1-3	OFF	SW2-3	OFF	SW3-3	OFF
SW1-4	OFF	SW2-4	OFF	SW3-4	OFF
		SW2-5	OFF	SW3-5	OFF
		SW2-6	OFF	SW3-6	OFF
		SW2-7	OFF	SW3-7	OFF
		SW2-8	OFF	SW3-8	ON
		SW2-9	ON	SW3-9	ON
		SW2-10	OFF	SW3-10	ON

The factory switch settings enable a standard register address of 776700 and a standard interrupt vector address of 254.

TABLE A-4
OPTION SWITCH SW1 SETTINGS

Option Sw	Open	Closed	Function
SW1-1	Run	Halt-Reset	Controller Run/Halt-Reset
SW1-2			Not used[1]
SW1-3			Not used[1]
SW1-4			Interrupt vector select #3[2]

[1]All unused switches MUST BE OFF.

[2]See paragraph 3.4.2.

TABLE A-5
OPTION SWITCH SW2 SETTINGS

Option Sw	Open	Closed	Function
SW2-1			Interrupt vector select #1[4]
SW2-2			Interrupt vector select #2[4]
SW2-3	RH11	RH70	RH11 vs RH70 select
SW2-4	Disable	Enable	Swap logical units 0 and 1 with 2 and 3
SW2-5			Not used[5]
SW2-6	Disable	Enable	Dual port mode
SW2-7	Disable	Enable	Dual access mode
SW2-8	Disable	Enable	DMA bandwidth control[3]
SW2-9	No bias	Biased Off	Unit-Busy-Off Bias[1]
SW2-10	2K	4K	PROM size[2]

[1]Must be CLOSED unless all drives attached to the controller are dual ported.

[2]Must be OPEN.

[3]See paragraph 5.4.2.

[4]See paragraph 3.4.2.

[5]This switch is "Not used" for firmware revisions C and above. For firmware revisions A and B, setting SW2-5 ON enabled Lark drive compatibility mode.

TABLE A-6
OPTION SWITCH SW3 SETTINGS

Option Sw	Open	Closed	Function
SW3-1			Drive configuration[1]
SW3-2			Drive configuration[1]
SW3-3			Drive configuration[1]
SW3-4			Drive configuration[1]
SW3-5			Drive configuration[1]
SW3-6			Drive configuration[1]
SW3-7		776300	Controller address (Alternate)
SW3-8		776700	Controller address (Standard)
SW3-9	Enable	Disable	Bootstrap PROMs
SW3-10	Enable	Disable	Line time clock

NOTE: SW3-7 and SW3-8 must not both be closed at the same time.

[1]See Table A-2.

Appendix B
Modifications for DEC Diagnostics

The SC03/B1 controller executes all DEC RM02/RM03 diagnostics. Several of the lower level diagnostics require patching to by-pass unsupported maintenance mode functions.

Emulex provides diagnostics which are self-sizing and need no patching. They are listed at the end of this appendix.

The following describes how to patch the DEC diagnostics for non-standard disk sizes. All locations and contents are in octal.

B.1 ZRMA-C0 FORMATTER (August 1977)

B.1.1 Modifications to Correct Programming Errors

Location	From	To
12632	10011	1
23630	13746	12746
27154	1750	1503
27512	10164	110164
31602	10164	110164
32772-32774	5702, 1426	4737, 34676
32776-33000	4737, 34676	5702, 1424

B.1.2 Modifications For Number of Cylinders and Tracks

Location	From	To
30044	4037	406
11260-11262	112737, 4	113737, 31472
11266-11270	12737, 1466	13737, 31470
11510-11512	22737, 151466	23737, 31466
11520-11522	22737, 2000	23737, 31464
12530-12532	12702, 1466	13702, 31470
12560-12562	12737, 5	13737, 5660
12612-12614	62737, 5	63737, 5660
15200-15202	22737, 1466	23737, 31470
15210-15212	122737, 4	123737, 31472
15402-15404	122737, 1466	123737, 31470
15410-15412	112737, 4	113737, 31472
16410-16412	22737, 4	23737, 31472
16430-16432	22737, 1466	23737, 31470
16440-16442	122737, 4	123737, 31472
16502-16504	22737, 1467	23737, 5652
20070-20072	12737, 1466	13737, 31470
20076-20100	12737, 4	13737, 31472
27176-27200	22705, 20024	122705, 24
27204-27206	22705, 24024	122705, 27
27220-27222	22705, 20025	122705, 25

Modifications For Number of Cylinders and Tracks (con't)

Location	From	To
27226-27230	22705, 24025	122705, 26
10734-10740	12737, 1466, 1320	104412, 13703, 26644
10742-10746	132762, 3, 26526	13702, 1220, 10263
10750-10752	1003, 12737	10, 4737
10754-10756	1466, 1320	31320, 104413

The following subroutine must be inserted where indicated. It replaces a rotational position sensing routine that the formatter does not need since it only formats one drive at a time. The contents of the existing routine are not shown.

Locations: 31320-31452

Contents: 62703, 36, 12713, 100027, 11304, 12713, 100030, 11305, 12713, 100036, 10437, 1320, 10537, 1324, 12703, 31464, 105023, 110523, 10413, 52723, 150000, 10423, 10523, 5204, 5205, 10437, 5652, 10537, 5660, 10437, 5666, 10537, 5674, 10437, 5704, 10537, 5712, 10437, 5730, 10537, 5736, 10437, 5754, 10537, 5762, 207.

B.1.3 Formatter Operation

The Formatter program writes either all zeros, all ones or a worst case pattern in every sector, and at the same time it writes the headers. It does this by writing the complete track at one time. The program will print out five errors while attempting to read the Bad Sector File on the last track of the disk if the pack has not been previously formatted. After the errors it will continue in a normal manner and will put a Bad Sector File on the pack. The program will ask for a pack I.D. if none already exists in the Bad Sector File.

The program can be loaded by XXDP. The normal starting location is 200_8, but should be started at 204_8 initially if it is desired to change the Unibus address or vector.

The program will type:

MODE (C OR F)

C should be typed for check and F for format, followed by a carriage return. Format mode does one pass, check mode does three passes with a rotating worst-case data pattern.

The program will then ask:

OPERATE IN 32 SECTOR (16 Bit) MODE (Y or N)

Y followed by carriage return should be typed.

The program will then ask for a drive:

DRIVE:

Enter the number (0-7) of the drive to be formatted followed by a carriage return.

The program will ask for address limits:

ENTER ADDRESS LIMITS:

Min and max sector, track and cylinder numbers may be entered in decimal followed by a carriage return. Just a carriage return will use the normal values. A period followed by a carriage return will terminate this phase.

The program will then ask for data pattern to which a carriage return should be typed to select worst-case. No pattern is asked for in Check mode.

The program will then type:

STARTING FORMAT (CHECK) ON DRIVE N

The program will list all errors and will indicate when it is done. The Bad Sector File is written just prior to the done message. During the format, typing a Control-O will display the current cylinder and track being formatted.

B.2 ZRMB-B0 PERFORMANCE EXERCISER (August 1977)

B.2.1 Modifications to Correct Programming Errors

Location	From	To
11134-11136	400, 46116	100000, 46144
32144 13746	12746	
35130 1750	1503	
35466 10164	110164	
37556 10164	110164	
41036-41040	5702, 1426	4737, 34676
41042-41044	4737, 34676	5702, 1424

All of the above items are unidentified program bugs.

B.2.2 Modifications For Number of Cylinders and Tracks

Location	From	To
4440	57512	60410
4472	57512	60410
6364-6366	22760, 1465	26060, 106
13534-13540	123727, 1415, 5	240, 4737, 60304
13554-13560	23727, 1412, 151466	240, 4737, 60230
16654-16656	62705, 5	66005, 112
16672-16676	20527, 4, 101402	26005, 112, 3002
16700-16702	162705, 5	16005, 112
22614-22616	112766, 4	116066, 112
25442-25446	10004, 62704, 2	10046, 4737, 60064
25664	12737	402
25762-25764	16403, 55252	4737, 60206
26214-26220	12737, 1466, 40674	240, 4737, 60262
26222-26226	112737, 4, 40673	240, 4737, 60326
35152-35154	22705, 20024	122705, 24
35160-35162	22705, 24024	122705, 27
35174-35176	22705, 20025	122705, 25
35202-35204	22705, 24025	122705, 26

The following subroutine must be added to the end of the program at the indicated locations.

Locations: 60064-60204

Contents: 10146, 111001, 13704, 34620, 4037, 35050, 401, 403, 105761, 34512, 1375, 105761, 34472, 3424, 62704, 36, 6301, 6301, 62701, 60350, 12714, 100027, 11421, 11400, 5300, 10037, 1446, 12714, 100030, 11421, 11437, 1444, 12714, 100036, 12601, 16604, 2, 12600, 62704, 2, 200.

Locations: 60206-60346

Contents: 16403, 55252, 13763, 1444, 16, 13763, 1444, 24, 207, 5046, 111016, 6316, 6316, 67716, 60350, 13646, 52716, 150000, 5216, 22637, 1412, 207, 5046, 111016, 6316, 6316, 62716, 60350, 13637, 46074, 207, 5046, 111016, 6316, 6316, 62716, 60352, 123637, 1415, 207, 5046, 111016, 6316, 6316, 62716, 60352, 113637, 46073, 207.

Those users running on drives with more than 80 MB capacity will require the following patches. The Performance Exerciser limits the number of allowable bad sectors on any drive to 16, even though the Bad Sector File can handle 126. The following patches allow the program to run with 126 bad sectors or less. The first two patches move the base address of the buffer. These locations have already been patched, and the "from" column reflects those patches.

Location	From	To
4440	60410	70410
4472	60410	70410
17202	20	176
17206	62702	16002
20274	12701	16001
20300	60001	240
20304	20	176
25504	14	22
25510	162	154
25716	122	126
26166	62701	16001
26174	40	400
26344	62701	16001
26352	40	400
43146	0	60410
43452	0	61410
43756	0	62410
44262	0	63410
44566	0	64410
45072	0	65410
45376	0	66410
45702	0	67410

B.2.3 Performance Exerciser Operation

This program has the ability to do various operations on one to four drives. The Formatter must be run before this program can be run so as to provide proper patterns and a Bad Sector File.

A carriage return can be given to the requests for date and operator I.D. The program will then type:

ENTER PARAMETERS:

A carriage return should be given since it is normally not necessary to change the program parameters and the full instructions would be needed. After listing the availability of the eight drives the program is started with those drives that are on-line if started at location 200. Starting at 204 requires further keyboard commands as follows:

The program can be commanded from the keyboard by typing Control-C. It will then respond with ENTER COMMANDS. The command letter followed by the drive number (or the letter A for all drives) and a carriage return should be typed. The commands are:

T - Do normal random testing on drives.

D - Deassign a drive from testing.

W - Write data pattern starting at min address and proceeding to max address. Headers and Bad Spot File are not written.

R - Read data starting at min address and proceeding to max address.

WT - Same as write command, but then does test command.

S - Summary of current status.

Most of the commands will ask for min and max address limits. Sector, track and cylinder numbers may be entered in decimal, or a carriage return will give normal values. A period followed by a carriage return will terminate the requests.

The program will then ask for a Drive I.D. A 0-6 character I.D. followed by a carriage return should be entered. The I.D. is used during the status summary printouts that occur every 5 minutes.

Once the I.D. has been entered the program begins execution.

B.3 ZRMC-B0 FUNCTIONAL TEST - PART 1 (August 1977)

B.3.1 Modifications For Correct Operation

Loc.	From	To
25024, 25026	4737, 43216	137,25622
10730	40001	0
13062	1012	412
26600	1007	407
27014	1011	411
35570	1406	406
45152	4	10
60000	7	1405
66074	13746	12746
10356-10362	5007, 110102, 1	11102, 105002, 240

B.3.2 Modifications For Number of Cylinders and Tracks

Location	From	To
7634	24024	20026
7654	24025	20027
7732-7734	12706, 1100	4737, 104106
27500-27502	12737, 1466	13737, 104400
30522-30524	22726, 1000	23726, 104400
31372-31374	12737, 1466	13737, 104400
32022-32024	12737, 1466	13737, 104400
32240-32242	22737, 1466	23737, 104400
32730-32732	12737, 2400	13737, 104410
33224	3400	37400

Modifications For Number of Cylinders and Tracks (con't)

Location	From	To
33250-33252	12737, 2400	13737, 104410
33344-33346	12737, 1467	13737, 104402
33636	2000	4000
33662-33664	12737, 1467	13737, 104402
36364	633	40
36370	634	41
36754	634	40
36760	633	41
37436-37440	12737, 2400	13737, 104410
37700	4000	40000
37724-37726	12737, 2400	13737, 104410
40032-40034	12737, 1467	13737, 104402
40304	2000	4000
40330-40332	12737, 1467	13737, 104402
51114	177770	177700
51134-51140	23727, 51702, 240	23737, 51702, 104412
51150-51152	162737, 5	163737, 104412
51224-51226	22737, 1467	23737, 104402
51340-51342	22737, 1467	23737, 104402
51600	176000	170000
52236-52242	23727, 1432, 1466	23737, 1432, 104400
52304-52310	123727, 1405, 4	123737, 1405, 104404
57730-57736	23727, 1432, 1466	23737, 1432, 104400
57776-60002	123727, 7, 4	123737, 1405, 104404

The following subroutine must be inserted where indicated. The previous contents of the locations should all be zeros.

Locations: 104106-104174

Contents: 13700, 1276, 062700, 36, 12701, 104400, 12710, 100027, 11021, 11011, 5221, 12710, 100030, 11021, 11011, 5221, 105021, 116121, 177775, 12710, 100036, 16100, 177776, 6200, 6200, 6200, 10011, 207.

B.4 ZRMD-B0 FUNCTIONAL TEST - PART 2 (August 1977)

B.4.1 Modifications for Correct Operation

Location	From	To
40452	4	10
63360	13746	12746

Both of the above modifications correct unidentified program bugs.

B.4.2 Modifications For Number of Cylinders and Tracks

Location	From	To
7656	24024	20026
7674	24025	20027
7732-7734	12700, 1100	4737, 101550
17514-17516	12737, 2037	13737, 102514
20374-20376	12737, 1466	13737, 102500
22272-22274	22737, 2000	23737, 102506
22300	103402	101402
23014-23016	22737, 1466	23737, 102500
23076-23100	12737, 1466	13737, 102500
23104-23106	12737, 2037	13737, 102514
23374-23376	12737, 1466	13737, 102500
23402-23404	12737, 2037	13737, 102514
24406-24410	12737, 2400	13737, 102510
25066	3400	37400
25126-25130	12737, 1467	13737, 102502
25614	1777	3777
34714	5737	0
36766-36770	122763, 4	123763, 102504
44414	177770	177700
44434-44440	23727, 45202, 240	23737, 45202, 102512
44450-44452	162737, 240	163737, 102512
44474-44500	23727, 45200, 5	23737, 45200, 102506
44510-44512	162737, 5	163737, 102506
44524-44526	22737, 1467	23737, 102502
44640-44642	22737, 1467	23737, 102502
45100	176000	170000
45536-45542	23727, 1434, 1466	23737, 1434, 102500
45604-45610	123727, 1407, 4	123737, 1407, 102506
53764-53766	22737, 1466	23737, 102500
54002-54004	122737, 4	123737, 102504

The following subroutine must be inserted where indicated. The previous contents of the locations should be all zeros.

Location: 101550-10646

Contents: 13700, 1276, 62700, 36, 12701, 102500, 12710, 100027, 11021, 11011, 5221, 12710, 100030, 11021, 11011, 5221, 105021, 116121, 177775, 12710, 100036, 16100, 177776, 6200, 6200, 6200, 10021, 112721, 37, 116111, 177767, 207.

B.5 ZRME-B0 FUNCTIONAL TEST - PART 3 (August 1977)

B.5.1 Modifications For Correct Operation

Location	From	To
31032	42702	52702
30070, 30072	404, 240	402, 0
30076, 30100	137, 30470	5237, 1336
30416, 30420,	404, 240	402, 0
30424, 30426	137, 30470	5237, 1336
44472	4	10
67364	13746	12746

B.5.2 Modifications For Number of Cylinders and Tracks

Location	From	To
7632	24024	20026
7652	24025	20027
7706-7710	12706, 1100	4737, 111760
20040-20042	12737, 1466	13737, 112100
20444-20442	12737, 1466	13737, 112100
22076-22100	12737, 2037	13737, 112114
32604-32610	23727, 1434, 1400	23737, 1434, 112100
32710-32712	12737, 2037	13737, 112114
36722-36724	22737, 2037	23737, 112114
41000-41002	12737, 2000	13737, 112116
41006-41010	12737, 1466	13737, 112100
42012-42014	12737, 2012	13737, 112120
42426-42430	112737, 4	123737, 112104
42446-42450	22737, 1466	23737, 112100
42516-42520	122737, 4	123737, 112104
42536-42540	22737, 1466	23737, 112100
43006-43010	122763, 4	123763, 112104
50434	177770	177700
50454-50460	23727, 51222, 240	23737, 51222, 112112
50470-50472	162737, 240	163737, 112112
50514-50520	23727, 51220, 5	23737, 51220, 112106
50530-50532	162737, 5	163737, 112106
50544-50546	22737, 1467	23737, 112102
50660-50662	22737, 1467	23737, 112102
51120	176000	170000
51556-51562	23727, 1434, 1466	23737, 1434, 112100
51624-51630	123727, 1407, 4	123737, 1407, 112104
60004-60006	22737, 1466	23737, 112100
60022-60024	122737, 4	123737, 112104

The following subroutine must be added to the test at:

Locations: 111760-112052

Contents: 13700, 1276, 62700, 36, 12701, 112100, 12710, 100027, 11021, 11011, 5221, 12710, 100030, 11021, 11011, 5221, 105021, 116121, 177775, 12710, 100036, 16100, 177776, 6200, 6200, 6200, 10021, 112721, 37, 116121, 177767, 105021, 116121, 177776, 112721, 12, 116111, 177776, 207.

B.6 ZRMF-B0 EXTENDED DRIVE TEST (August 1977)

B.6.1 Modifications for Correct Operation

Location	From	To
21464	13746	12746
27722-27726	5737, 4322, 1011	32737, 100000, 4350
27730-27734	32737, 100000, 4350	1405, 12737, 177777
27736-27742	1405, 12737, 177777	1446, 137, 30370
27744-27750	1446, 137, 30370	5737, 4322, 1401
37246	1750	1503
37604	10164	110164
41674	10164	110164
43064-43066	5702, 1426	4737, 44770
43070-43072	4737, 44770	5702, 1424

All of the above are unidentified program bugs.

B.6.2 Modifications For Number of Cylinders and Tracks

**Note: Required on drives of less than 100 logical cylinders only

Location	From	To
1774	400	1466
2040	400	1466
2176	144	100**
37270-37272	22705, 20024	122705, 24
37276-37300	22705, 24024	122705, 27
37312-37314	22705, 20025	122705, 25
37320-37322	22705, 24025	122705, 26
17574-17576	20127, 1466	20137, 1574
17602-17604	20227, 4	20237, 1602
17022-17026	22700, 5, 3365	23700, 1602, 2365
17222-17224	122737, 4	123737, 1602
20312-20314	122737, 5	123737, 1602
20320	3370	2370
33530-33534	122702, 5, 3003	123702, 1602, 2003

The following subroutine must be inserted where indicated. It replaces an existing subroutine of similar function that is no longer needed. The contents of the existing routine are not shown.

Locations: 26632-27004

Contents: 104412, 113704, 1102, 6304, 16401, 1620, 13704, 1450, 62704, 36, 12702, 1566, 5003, 12122, 6237, 1566, 103002, 12122, 401, 5022, 5203, 20327, 14, 1405, 20327, 3, 1363, 24242, 761, 12714, 100027, 11405, 12703, 1574, 5713, 1412, 21327, 1466, 1407, 21327, 1465, 1002, 5305, 402, 20513, 2001, 10513, 12714, 100030, 11437, 1602, 104413, 207.

B.7 ZRMI-B0 DRIVE COMPATIBILITY TEST (August 1977)

B.7.1 Modifications For Correct Operation

Location	From	To
21000	13746	12746

The above item is an unidentified program bug.

There are no Part 2 modifications to this test. It is impractical to rewrite this test. To do so would require allocating an indeterminant amount of buffer space near the beginning of the test. The test uses cylinders 0-800 (but not all of them), and tracks 0-4. Any configuration with 801 or more cylinders and 5 or more tracks is compatible with this test.

B.8 EMULEX DIAGNOSTICS

Self-sizing diagnostics for the RM02, RM03, and RM05 may be ordered from Emulex. The diagnostics are as follows:

S1B18X Formatter
S1B19X Performance Exerciser
S1B10X Functional Test (Part 1)
S1B11X Functional Test (Part 2)
S1B12X Functional Test (Part 3)
S1B13X Extended Drive Test

BLANK