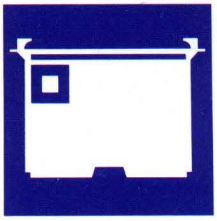
DATA BOOK



HARDWARE

FORCE COMPUTERS

VMEbus Hardware Products

1991

DATA BOOK 1991

VMEbus Products

FORCE COMPUTERS®

VME at its best

First Edition
09.90/30.0/DB/A1/Rev. 1

General Information

16-Bit CPU Boards

32-Bit CPU Boards

Memory Boards

Controller Boards

I/O Boards

Accessories

General Information

16-Bit CPU Boards

32-Bit CPU Boards

Memory Boards

Controller Boards

I/O Boards

Accessories

General Information

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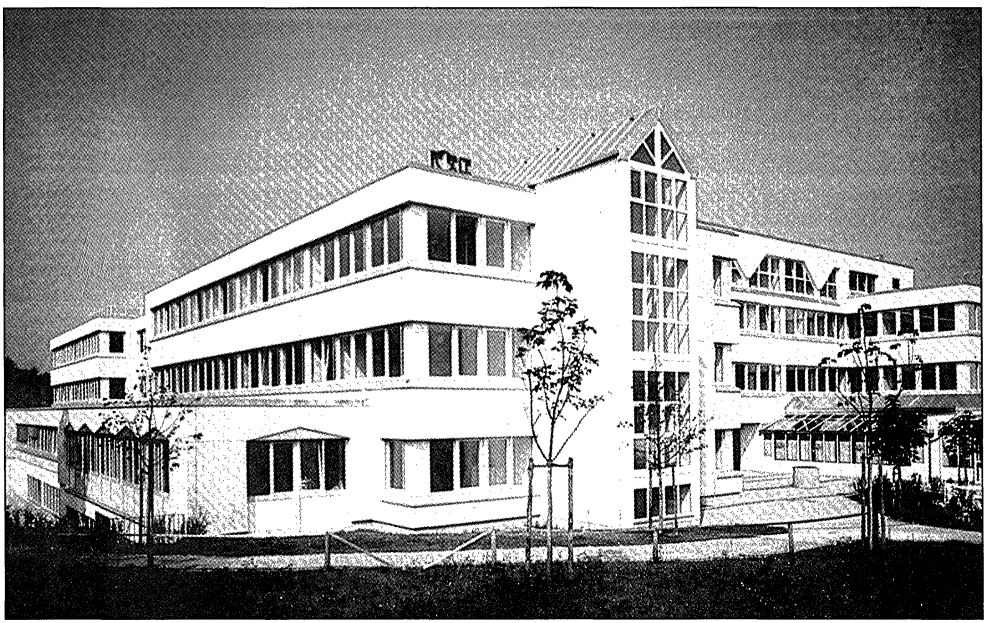
FORCE COMPUTERS, INC.

European Headquarters
FORCE COMPUTERS GmbH



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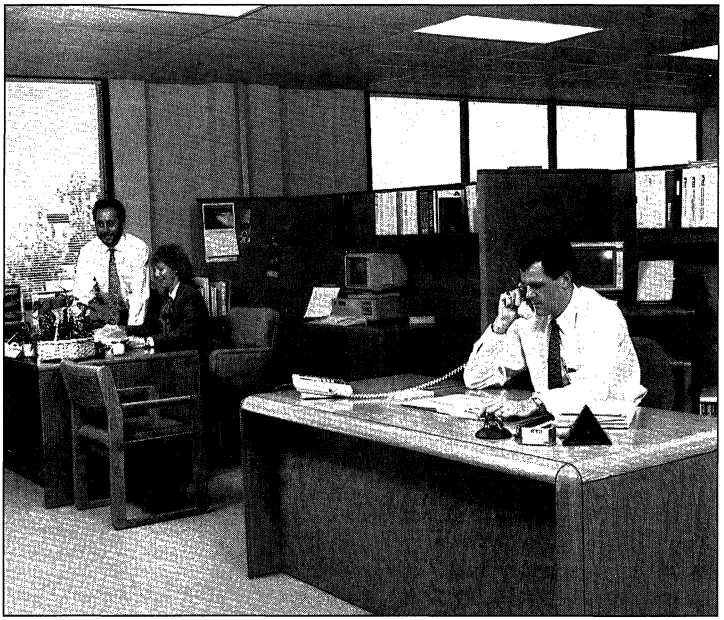
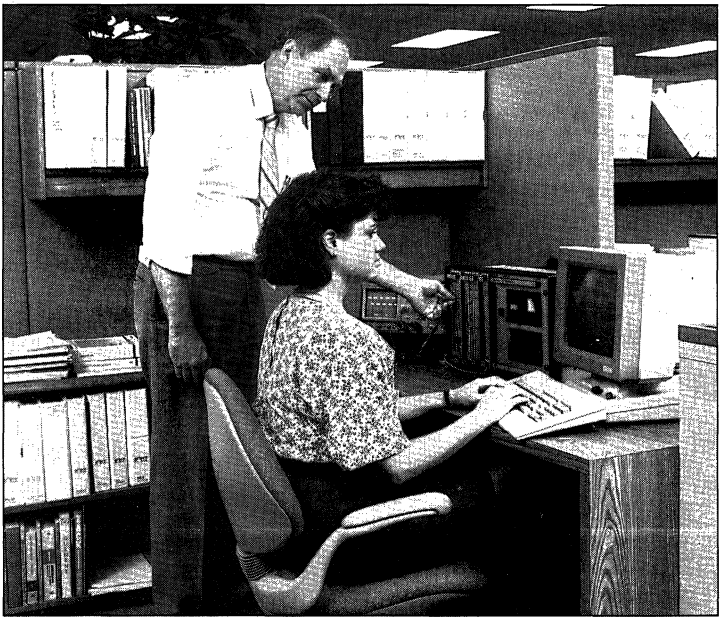
Commercial Service from Sales Personnel



Technical Service from Applications Teams



Commitment to Service

FORCE COMPUTERS believes that service to our customers is as much a product of the company as the VMEbus boards, systems and software we design, manufacture and sell. Accordingly, we commit fully to providing customers with the best possible level of service worldwide. The services we offer are comprehensive, including pre- and post-sales consulting, customer application support, design-in activities, problem diagnosis, field test, Beta-site arrangements, delivery expediting, credit and many more. Our services are provided by fully-trained Field Sales and Technical Support personnel. Authorized FORCE distributors and representatives are also trained by us and are eager to help you with the selection and application of FORCE products.

For further information, please contact FORCE at any of the addresses listed on page 11.

Introduction to FORCE COMPUTERS Product Guide

This is the FORCE COMPUTERS product guide, our comprehensive catalog of products and services. For the sake of completeness, the guide includes products that are not recommended for new designs. These products are either obsolete or will become obsolete under FORCE COMPUTERS' controlled End Of Lifetime Buy procedure. This procedure helps provide maximum notice to customers regarding a product's planned obsolescence. In every possible case, FORCE recommends an alternate product. For existing customers, FORCE may continue to produce products not recommended for new designs as long as all component parts are available.

Part No.	Product	Description	Recommended for new Designs	Suggested Alternative
	32-Bit CPU Boards			
101106	SYS68K/CPU-22X	68020/16.7 MHz/1 Mbyte S-DPR SRAM	yes	
101102	SYS68K/CPU-22XA	68020/20.0 MHz/1 Mbyte S-DPR SRAM	yes	
101120	SYS68K/CPU-23XS	68020/12.5 MHz/1 Mbyte Shared SRAM	yes	
101121	SYS68K/CPU-23X	68020/16.7 MHz/1 Mbyte Shared SRAM	no	CPU-23XB
101122	SYS68K/CPU-23XB	68020/25.0 MHz/1 Mbyte Shared SRAM	yes	
101134	SYS68K/CPU-26XS	68020/12.5 MHz/1 Mbyte Shared DRAM	yes	
101130	SYS68K/CPU-26X	68020/16.7 MHz/1 Mbyte Shared DRAM	no	CPU-26XS, CPU-26XA
101131	SYS68K/CPU-26XA	68020/20.0 MHz/1 Mbyte Shared DRAM	yes	
101132	SYS68K/CPU-26ZA	68020/20.0 MHz/4 Mbyte Shared DRAM	yes	
101171	SYS68K/CPU-27X	68020/16.7 MHz/1 Mbyte DRAM	no	CPU-27XB
101172	SYS68K/CPU-27XB	68020/25.0 MHz/1 Mbyte DRAM	yes	
101173	SYS68K/CPU-27XBE	68020/25.0 MHz/1 Mbyte DRAM/ETH	yes	
101152	SYS68K/CPU-29X	68020/16.7 MHz/1 Mbyte SRAM 0WS	no	CPU-29XB, CPU-29XC, CPU-33XB
101159	SYS68K/CPU-29XB	68020/25.0 MHz/1 Mbyte SRAM 0WS	yes	
101154	SYS68K/CPU-29XC	68020/30.0 MHz/1 Mbyte SRAM 0WS	yes	
101302	SYS68K/CPU-30ZA	68030/20.0 MHz/4 Mbyte Shared DRAM	yes	
101305	SYS68K/CPU-30ZBE	68030/25.0 MHz/4 Mbyte Shared DRAM/ETH	yes	
101306	SYS68K/CPU-30BE/16	68030/25.0 MHz/16 Mbyte Shared DRAM/ETH	yes	
101312	SYS68K/CPU-31XA	68030/20.0 MHz/1 Mbyte S-DPR SRAM	yes	
101314	SYS68K/CPU-31XB	68030/25.0 MHz/1 Mbyte S-DPR SRAM	yes	
101326	SYS68K/CPU-32XB	68030/25.0 MHz/1 Mbyte SRAM 0WS	yes	
101333	SYS68K/CPU-32XC	68030/30.0 MHz/1 Mbyte SRAM 0WS	yes	
101340	SYS68K/CPU-33XN	CPU-33X without FPU (68882)	yes	
101341	SYS68K/CPU-33X	68030/16.7 MHz/1 Mbyte Shared DRAM	yes	
101342	SYS68K/CPU-33XB	68030/25.0 MHz/1 Mbyte Shared DRAM	yes	
101343	SYS68K/CPU-33ZB	68030/25.0 MHz/4 Mbyte Shared DRAM	yes	
101427	SYS68K/CPU-37X	68030/16.7 MHz/1 Mbyte DRAM	no	CPU-30ZA
101423	SYS68K/CPU-37Z	68030/16.7 MHz/4 Mbyte DRAM	no	CPU-30ZA
101422	SYS68K/CPU-37XBE	68030/25.0 MHz/1 Mbyte DRAM/ETH	no	CPU-30ZBE
101426	SYS68K/CPU-37ZBE	68030/25.0 MHz/4 Mbyte DRAM/ETH	no	CPU-30ZBE
105001	SYS68K/CPU-386A	80386/16.0 MHz/2 Mbyte DRAM	yes	
105003	SYS68K/CPU-386C	80386/16.0 MHz/8 Mbyte DRAM	yes	

Part No.	Product	Description	Recommended for new Designs	Suggested Alternative
102000	SYS68K/CPU-40B/4-00	68040/25.0 MHz/4 Mbyte Shared DRAM	yes	
102001	SYS68K/CPU-40B/4-01	68040/25.0 MHz/EAGLE-01/4 Mbyte Shared DRAM	yes	
102100	SYS68K/CPU-40B/16-00	68040/25.0 MHz/16 Mbyte Shared DRAM	yes	
102101	SYS68K/CPU-40B/16-01	68040/25.0 MHz/EAGLE-01/16 Mbyte Shared DRAM	yes	
102200	SYS68K/CPU-40D/4-00	68040/33.0 MHz/4 Mbyte Shared DRAM	yes	
102201	SYS68K/CPU-40D/4-01	68040/33.0 MHz/EAGLE-01/4 Mbyte Shared DRAM	yes	
102300	SYS68K/CPU-40D/16-00	68040/33.0 MHz/16 Mbyte Shared DRAM	yes	
102301	SYS68K/CPU-40D/16-01	68040/33.0 MHz/EAGLE-01/16 Mbyte Shared DRAM	yes	
510053	SYS88K/CPU-80A/4	88100/20.0 MHz/ 4 Mbyte Shared DRAM/SCSI	yes	
510054	SYS88K/CPU-80A/16	88100/20.0 MHz/16 Mbyte Shared DRAM/SCSI	yes	
510056	SYS88K/CPU-80B/16	88100/25.0 MHz/16 Mbyte Shared DRAM/SCSI	yes	
510001	SYS88K/CPU-81A/4	88100/20.0 MHz/ 4 Mbyte Shared DRAM/VSB	yes	
510081	SYS88K/CPU-81A/16	88100/20.0 MHz/16 Mbyte Shared DRAM/VSB	yes	
510083	SYS88K/CPU-81B/16	88100/25.0 MHz/16 Mbyte Shared DRAM/VSB	yes	
	16-Bit CPU Boards			
100213	SYS68K/CPU-2VC	68010/10.0 MHz/1024 Kbyte Shared DRAM	no	CPU-33XN
100413	SYS68K/CPU-4VC	68010/12.5 MHz/ 128 Kbyte SRAM	yes	
100501	SYS68K/CPU-5A	68000/16.7 MHz/ 128 Kbyte SRAM 0WS/FPU	yes	
100602	SYS68K/CPU-6A	68000/12.5 MHz/ 512 Kbyte DRAM	yes	
100610	SYS68K/CPU-6VA	68010/12.5 MHz/ 512 Kbyte DRAM	yes	
	32-Bit Memories			
200150	SYS68K/DRAM-8A	2 Mbyte DRAM A32, A24 : D32, D24, D16, D8	yes	
200151	SYS68K/DRAM-8B	4 Mbyte DRAM A32, A24 : D32, D24, D16, D8	yes	
200152	SYS68K/DRAM-8C	8 Mbyte DRAM A32, A24 : D32, D24, D16, D8	yes	
200153	SYS68K/DRAM-8D	16 Mbyte DRAM A32, A24 : D32,D24,D16,D8	yes	
200154	SYS68K/DRAM-8E	32 Mbyte DRAM A32,A24 : D32,D24,D16,D8	yes	
200200	SYS68K/RR-2	Naked PROM/EPROM/EEPROM/SRAM/VMX	yes	
200402	SYS68K/SRAM-3B	1 Mbyte SRAM A32 : D32 VME/VMX	yes	
200502	SYS68K/SRAM-4B	1 Mbyte SRAM A32 : D32 VME	no	SRAM-6
200504	SYS68K/SRAM-5	512 Kbyte SRAM A32 : D32 VME	no	SRAM-6
200505	SYS68K/SRAM-6	2 Mbyte SRAM A32 : D32 VME	yes	
	16-Bit Memories			
200010	SYS68K/RR-1	Naked ROM/PROM/EPROM/SRAM	no	RR-2

Part No.	Product	Description	Recommended for new Designs	Suggested Alternative
	Controller Boards			
400023	SYS68K/AGC-2	Graphics Controller	yes	
400050	SYS68K/AGC-3	Advanced Graphics Controller	yes	
700007	SYS68K/ASCU-2	Advanced SYS Cont. W GPIB	yes	
300100	SYS68K/ILANC-1	Intelligent Ethernet Controller	no	CPU-30ZBE
300020	SYS68K/ISCSI-1	Intelligent SCSI Controller	yes	
	Input/Output Boards			
310050	SYS68K/IPIO-1	Intelligent Parallel I/O	yes	
310030	SYS68K/ISIO-1	8 Channel Serial I/O RS232/68010	no	ISIO-2
310031	SYS68K/ISIO-2	8 Channel Serial I/O RS232/RS422/68010	yes	
310004	SYS68K/SIO-2	6 Channel Serial I/O RS232/RS422	yes	
310011	SYS68K/OPIO-1	Parallel I/O: Opto Coupled	yes	
310010	SYS68K/PIO-1	Parallel I/O: TTL	yes	
330000	SYS68K/ICC-1	Intelligent Communications Controller	yes	
	Chassis and Accessories			
610500	SYS68K/TARGET-32	TARGET-32 Chassis/20 slots	yes	
610190	SYS68K/CHAS19-21E/12HE	12HE Chassis/21 Slots	no	TARGET-32
510020	SYS68K/MSM-42	42 Mbyte Hard/1 Mbyte Floppy/3.5"	yes	
510021	SYS68K/MSM-84	84 Mbyte Hard/1 Mbyte Floppy/3.5"	yes	
510092	SYS88K/TSM-168	155 Mbyte Streamer/168 Mbyte Hard	yes	
	Motherboards			
500005	SYS68K/MOTH-05B	5 Slot Motherboard/J1	yes	
500011	SYS68K/MOTH-09B	9 Slot Motherboard/J1	yes	
500006	SYS68K/MOTH-12B	12 Slot Motherboard/J1	yes	
500007	SYS68K/MOTH-21B	21 Slot Motherboard/J1	yes	
500008	SYS68K/MOTH-E05A	5 Slot 32 Bit Extension/J2	yes	
500012	SYS68K/MOTH-E09A	9 Slot 32 Bit Extension/J2	yes	
500009	SYS68K/MOTH-E12A	12 Slot 32 Bit Extension/J2	yes	
500010	SYS68K/MOTH-E21A	21 Slot 32 Bit Extension/J2	yes	
	Power Supplies			
700008	SYS68K/PWR-09A/220V	280 W Power Supply	yes	
700009	SYS68K/PWR-20/220V	750 W Power Supply	yes	

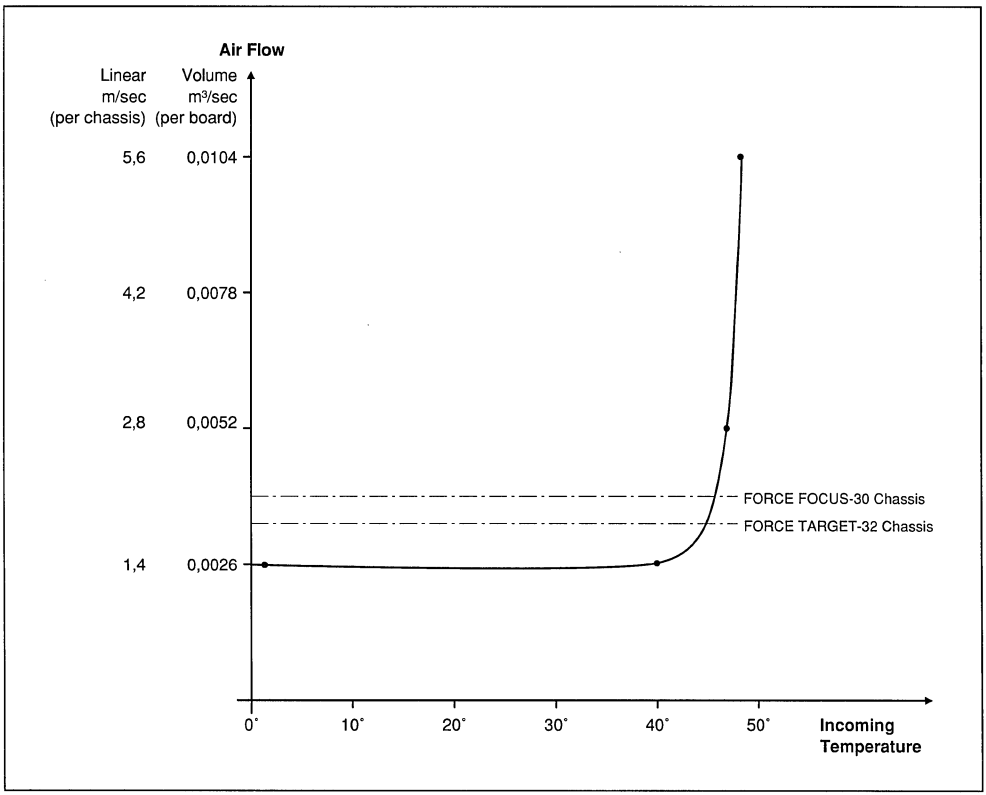
Environmental conditions for normal board operation

FORCE COMPUTERS' board level products are designed and tested for reliable operation under strictly specified environmental conditions.

The specification of these conditions are:

Operating temperature	0 to + 50 °C (with forced air cooling)
Storage temperature	– 40 to + 85 °C (non-operating)
Relative humidity	+ 5 to + 95 % (non-condensing)

These conditions refer to the environment surrounding the board within the user environment. Operating temperature refers to the temperature of the air circulating around the board and not the actual component temperature. To ensure the operating conditions are met, forced air cooling is required within the chassis environment. This should be achieved by driving air through the air gap between the boards in the chassis. Fans should be installed in the underside of the chassis, evenly placed under the loaded boards. The volume of air required per second is dependent on the number of boards installed in the system. The linear air speed is specified to ensure correct air circulation around the board level components. The other major factor influencing the air-flow requirement is the air temperature at the air inlet to the chassis. The following graph shows the air speed and air volume per board required to ensure correct operation of boards versus external or incoming air temperature. Both of these criteria need to be met to ensure correct, reliable and long-lived board operation.



Design

Design

FORCE COMPUTERS has achieved a leadership position in the markets it serves, namely original equipment manufacturers and system integrators who build VMEbus-based computers. FORCE rigorously controls the design phase of our new products. Control is essential to maintain compatibility and ensure continuity of product introductions. At FORCE COMPUTERS we commit to excellence with the objective of designing quality into every product.

Rules and Procedures

FORCE COMPUTERS designs its products to meet the requirement of the VMEbus specification (IEEE 1014). The electrical and mechanical rules of the VMEbus specification are the baseline conditions for the development of board level products and systems. FORCE uses modern CAD equipment for board layout. We thoroughly check and compare all films with original drawings and circuit schematics.

Component Selections

FORCE COMPUTERS uses the best commercial grade components (industrial grade where applicable) in the design and manufacture of our products. The availability of second sources is a key criterion in the decision to design-in a particular device. We only consider components with proven reliability and acceptable quality levels. Vendors must supply environmental test data for critical items; we purchase components that have undergone high-temperature burn-in. In addition, we also conduct regular vendor surveys to determine the adequacy of quality programs and production controls.

Prototype Development Phase

During the prototype phase of development, engineering and quality assurance work together to assure proper production methods and test procedures for all products. The responsible design and qualification engineers debug products and production methods. Custom test programs exercise new boards according to the design specification, intended functionality and conformance to the VMEbus specification. Full temperature cycling tests precede prototype release. This is often the longest phase of new product development due to the need to debug design, production and test issues. Reiteration of these procedures assures a smooth transition to pre-series production.

Pre-Series Production

Upon successful completion of the prototype phase, we release the product for pre-series (limited) production. Next, we write in-circuit, functional and burn-in test programs. We also embark on the writing of the VMEbus industry's most detailed and comprehensive product documentation (User's Manual). A limited lot (10–25 boards) is manufactured following documented work instructions, using a prototype board as production master. FORCE Engineering use these pre-series boards to validate the product for series production. Results of the validation effort are fed back to design and production. The completed test programs and documents form a part of the total release package for manufacturing. Before final release, Quality Assurance tests the product once again for functional compatibility with other products. For example, Quality Assurance tests a new RAM board with all CPU boards to ensure compatibility throughout a product family. Stress testing verifies multi-processor capabilities and simulates worst-case work conditions.

Manufacturing

Manufacturing

The task of manufacturing is to convert the high technology designs developed by Engineering into top quality, long-lived products. The manufacturing system at each working location is defined by considerations of "integrated quality" (see the Quality Assurance section of this book). We design the manufacturing flow flexibly to accommodate demand fluctuation without degradation of efficiency, quality or customer service.

Manufacturing Planning

Today and in the future the major purposes of manufacturing planning are to ensure timely production and delivery of customer orders and to keep manufacturing capacity in line with market demand. FORCE COMPUTERS' MRP System (Manufacturing Resource Planning) handles manufacturing logistics. This is a company-wide system that monitors orders and sales forecasts at one end and provides order fulfillment data at the other.

The FORCE MRP system helps to provide maximum service benefit to our customers by allowing us to establish realistic capabilities for surge capacity. In the future, our MRP system will enable the implementation of just-in-time (JIT) manufacturing procedures. We already accommodate our customer's JIT needs through the MRP system.

Component Purchasing

In every design, we use only Engineering-approved vendors for each component. Only components of leading suppliers can be approved. If Manufacturing or Purchasing suggests additional suppliers for specific components, QA Control applies a very strict approval procedure. Our MRP System determines the demand for each component based upon the production schedule and component lead-time information. We negotiate annual delivery contracts with our major suppliers to ensure continued, reliable supply.

Manufacturing Planning

Component Warehouse

Component Receiving Quality Control

Upon arrival at FORCE COMPUTERS, components are immediately subjected to quality control procedures. Besides the outward appearance of incoming components, we also check the internal manufacturer approval, data codes, and revision level. We store approved components in the component warehouse under conditions specified by the manufacturer.

Manufacturing Monitor and Control

From the product documentation provided by Design Engineering, Product Engineering generates the manufacturing documents to enable production to start. Product Engineering uses the MRP System to maintain Components Parts Lists for each FORCE product. Product Engineering is also responsible for the implementation of design revisions within manufacturing to ensure a maximum degree of functional transparency for board and product revision. We coordinate design revision worldwide by the common use of ECO's (Engineering Change Orders); QA monitors implementation of ECO's. When the MRP system calls up a production lot of a particular product in line with demand, the component warehouse provides the lot size of component kits for that product. The programmable devices (PAL, EPROMs etc.) are issued first to be programmed and then returned to the warehouse. This helps to ensure that only complete component kits (or picks) enter the manufacturing flow.

Board Assembly

FORCE employs state-of-the-art through-hole and surface mount board assembly procedures. Because our VMEbus products are often at the cutting edge of performance, we develop many of our own assembly tools. Regardless of the board assembly technique called for by a product's design, our board assembly procedures adhere to strict quality regulations. Our manufacturing process employs all QA measures that are standard in advanced PCB assembly companies. We monitor and calibrate our assembly equipment following the manufacturer's recommendations. To prevent damage, we transport the assembled products in custom-designed anti-static carriers between all assembly and test locations. We mark each board after assembly with a number that denotes lot number, assembly location, date, revision level and a unique serial number; we also inspect each board before it is passed to In-Circuit test.

In-Circuit Test

In-circuit testing, using Genrad 2276E test equipment, is the currently approved method. The bed-of-nails and the test program for each procedure are generated, modified and improved at the Design Center that developed the product. All other in-circuit test facilities use adapters and programs from one central source. This helps to ensure uniform testing at FORCE COMPUTERS facilities worldwide. Dedicated software in the test computer generates test reports at the product and component levels. We then provide these reports to the QA and Purchasing departments. Specific component suppliers may be excluded from further delivery if inadequate quality should be detected. Figure 1 shows a flow chart of the In-Circuit Test procedure.

In-Circuit Test

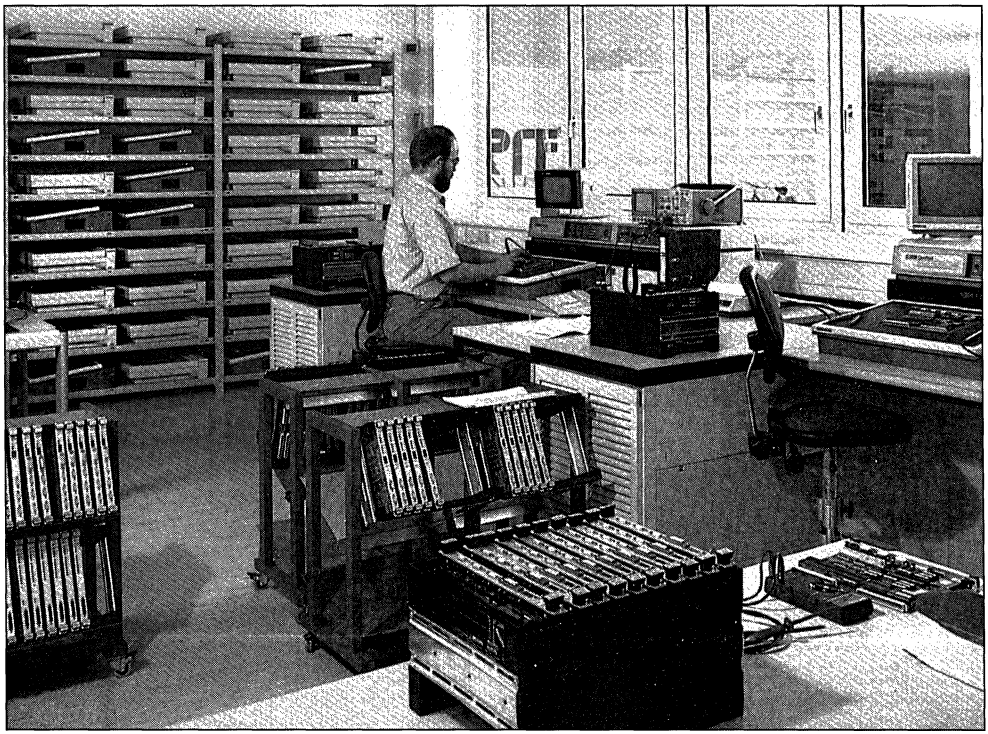
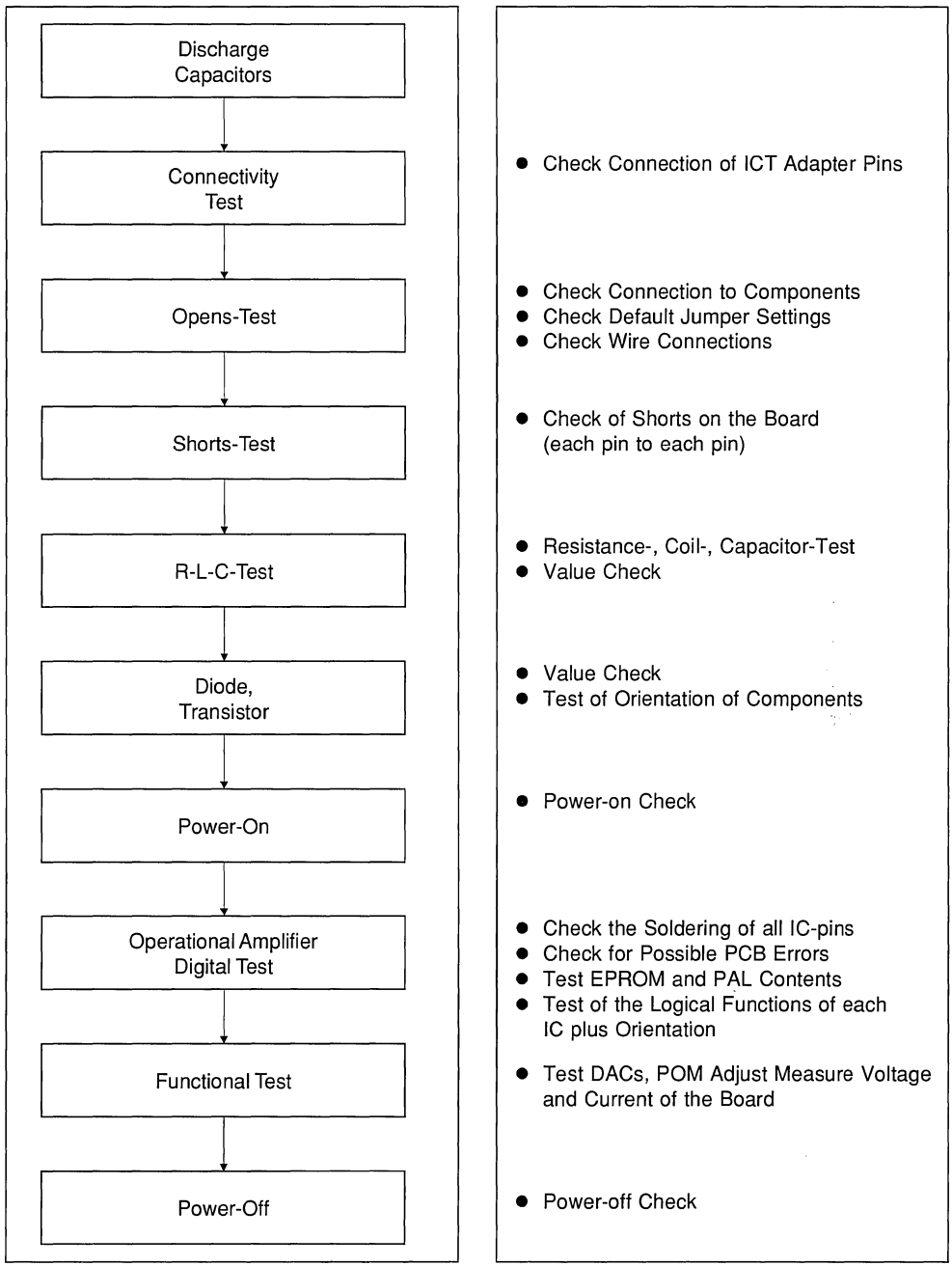


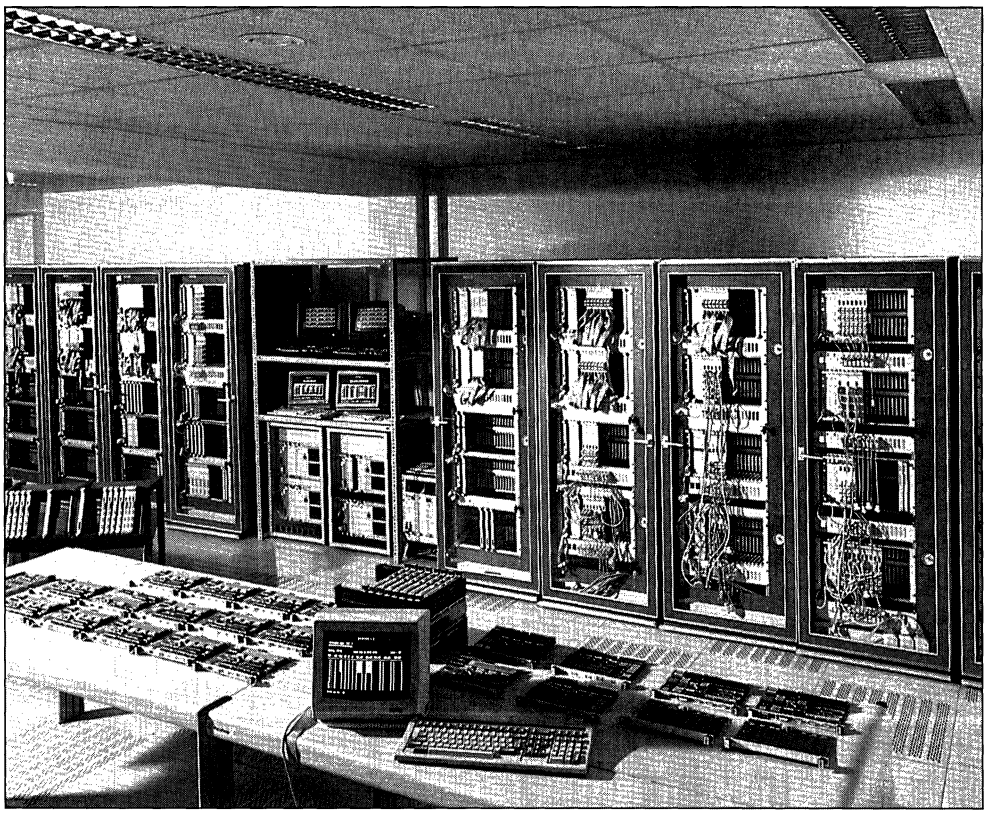
Figure 1 In-Circuit Test Flow Chart



Burn-In Test

A short functional test of each board follows the In-Circuit Test and precedes the Burn-In Test. The functional test uses a board-specific software routine written simultaneously with the board design. This ensures burn-in time only for functional boards. Burn-in tests are also functional tests that run for 48 hours at a minimum of 50 degrees C. We use test racks that provide a VME operating environment for the boards under test. A high-performance control system operating in a real-time, multi-tasking mode controls and monitors the test racks and the testing tasks. We endeavor to fully exercise all electronic components during the burn-in. All burn-in test departments (worldwide) use these racks with the control unit.

Burn-In Test Racks

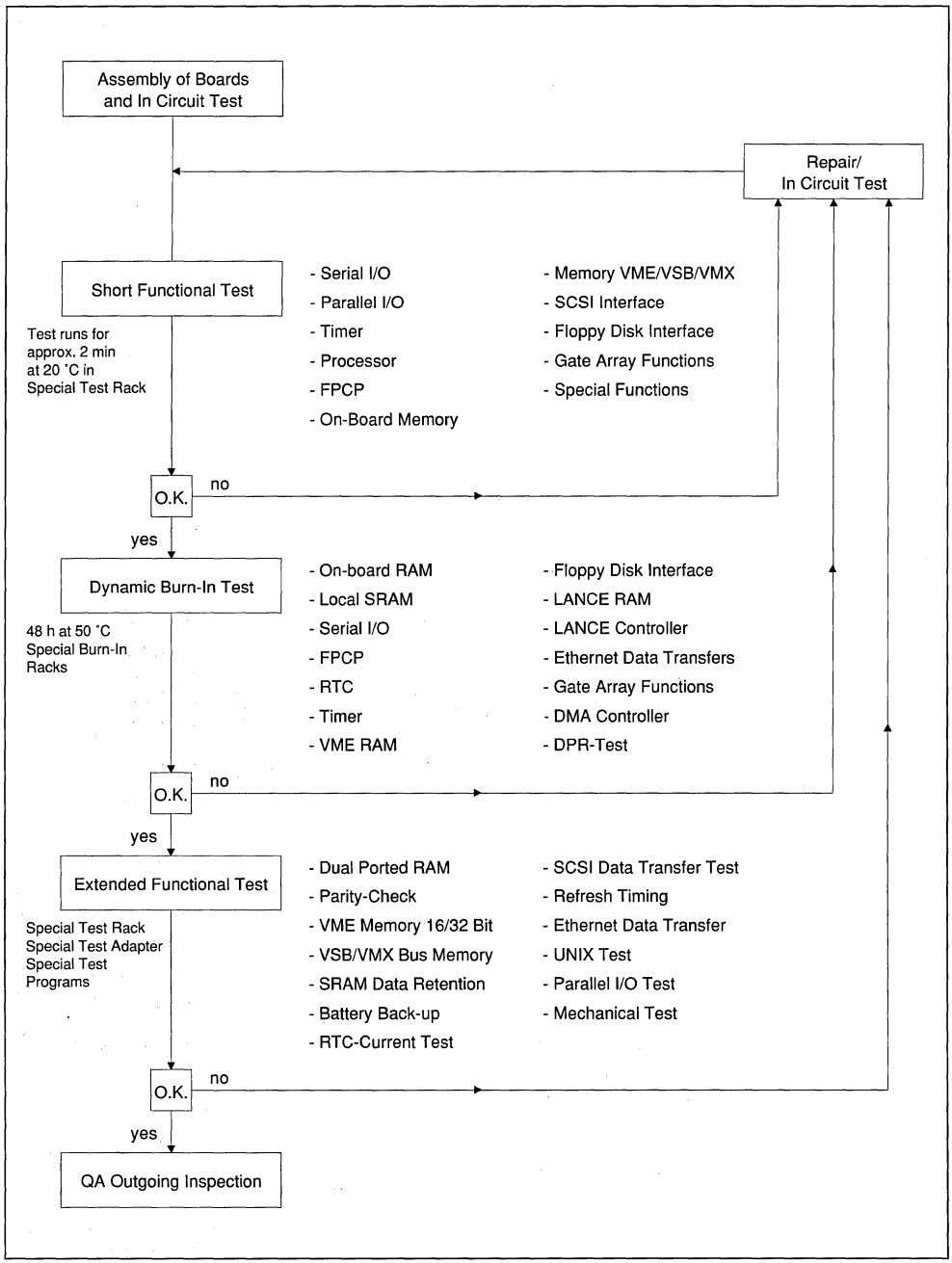


Full Functional Test

In this part of the manufacturing flow, we check all on-board functions under real-time conditions in a typical or similar user operating environment. Coordinated generation, modification and expansion of these test programs, in our Design Centers, ensures that identical functional tests will be used for a specific product worldwide. For newly introduced products, a team of programmers is constantly developing new program modules to integrate these functional test programs. In addition, we regularly maintain, expand and improve our test programs to increase their utility and accuracy. After passing full functional test, we set each board's factory defaults and submit the boards to QA for outgoing inspection. Figure 2 shows a flow chart of the Functional Test and Burn-In procedure.

Full Functional Test

Figure 2 Functional and Burn-In Test Flow Chart



Warehouse and Shipping

Following the outgoing inspection, the QA Department transfers the boards and systems to the Finished Goods Warehouse; here, we store the products in anti-static and dust-proof packages. The order schedule determines when the goods are prepared for shipping, when the documentation is included and when they are put into the shipping boxes. We take great care to develop customized shipping containers adequate to protect the product during transport to the customer. The customer will generally specify the shipment procedure. Still, for very urgent orders, FORCE COMPUTERS uses its expertise and connections to provide the optimum means of transportation for timely delivery. Practical packaging, professional documentation and fast delivery are additional features that give the final touch to FORCE COMPUTERS' high-technology products.

Finished Goods Warehouse

Quality Assurance

Quality Assurance

The FORCE COMPUTERS quality system incorporates a total quality assurance concept encompassing management, design, purchasing, manufacturing, test, inspection, and documentation. The FORCE Quality Assurance Control program ensures that products conform to published specifications and customer's quality requirements. Records which track the effective operation of FORCE quality systems are available for review at FORCE COMPUTERS by designated purchasing authorities and source inspectors.

Organization

Quality is the responsibility of management and it is the policy of management that quality needs to be controlled. A quality assurance organization must be independent of other organizations to function effectively. FORCE COMPUTERS' quality assurance manager reports directly to the general manager and has full authority to resolve matters on quality. FORCE delegates responsibility and authority to those personnel performing quality functions to identify and evaluate quality problems, and to initiate, recommend, or provide solutions. Management regularly reviews the status and adequacy of the quality program.

Records

Records are one principal form of objective evidence of quality. FORCE COMPUTERS maintains and uses records for inspection, test, corrective actions, and calibration. Maintained test and inspection records suggest the nature or type of observation, the number of observations made, and number and type of deficiencies found. Corrective actions records detail the nature of the action and effective dates of correction. We also maintain records showing the calibration history and status for test and measurement equipment.

Documentation and Change Control

In industries where innovation, redesign, and product improvement predominate, control of documentation is of critical importance to product quality and reliability. FORCE COMPUTERS maintains control over documentation relating to the design and manufacture of its products. Current issues of appropriate documents are available at all locations where operations essential to the effective functioning of the quality system are done. All changes to documentation are in writing. We also maintain written records of all changes made.

Statistical Quality Control and Analysis

FORCE COMPUTERS uses statistical analysis and tests to maintain the required control of quality. Sampling inspection adheres to MIL-STD-105D. Acceptable quality levels (AQL) apply to both the receiving inspection and final electrical and mechanical/visual inspection. Using modern test equipment, we generate data and analysis on yields as well as product quality trends. Causes of defects or significant variations in manufacturing operations can be identified and the necessary corrective actions quickly carried out.

Control of Inspection, Measuring and Test Equipment

Proper maintenance and control of test and measurement equipment helps ensure product conformance to specifications and required quality levels. We maintain calibration records and label equipment to show calibration intervals and status. The calibration system conforms to NATO Measurement and Calibration System Requirements for Industry (AQAP-6).

Test Programs and Procedures

FORCE COMPUTERS has developed sophisticated test programs using state-of-the-art test and measurement equipment for its board level and system products. Board level products are subjected to 100 percent In-Circuit Tests using Genrad 2276E automatic (bed of nails) testers. Data related to yields and product quality trends are collected, analyzed, and used as a basis for product improvement programs. Defect data feedback serves to initiate corrective actions. To screen-out infant mortalities, all boards are subjected to a dynamic burn-in for 48 hours at 50 degrees centigrade. Real-Time software-driven test programs enable board-level products to be tested in functional environments at elevated ambient temperatures. Using proprietary test programs in embedded software, we test all board-level products for full functionality in a VME system environment simulating the end use of

the product. Processor, memory, and controller chips, for example, are exercised to test performance in the intended application. A post-test electrical and visual sample inspection on all finished products verifies that all tests have been completed as specified.

Board Test and Inspection

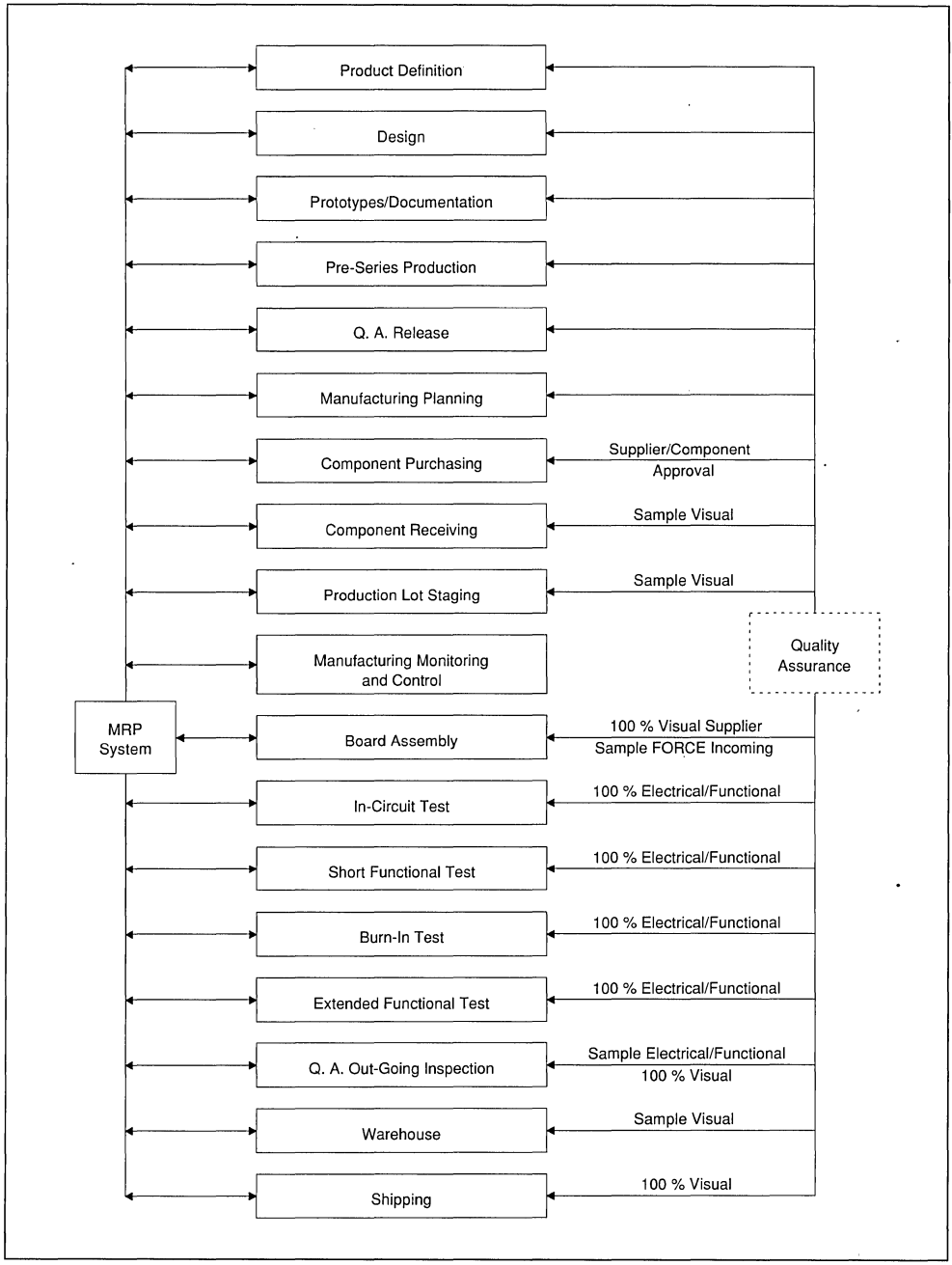
Standards and Specifications

The FORCE COMPUTERS' quality system conforms with and applies the following standards and specifications.

BS5750-Part 1	Specifications for Design
MIL-Q-9858A	Quality program requirements
AQAP-1	NATO Quality Control System Requirements for Industry
AQAP-6	NATO Measurement and Calibration System Requirements for Industry
IPC-SM-840	Qualification and Performance of Permanent Polymer Coatings
MIL-P-55110C	Military specification printed wiring boards
IPC-A-600C	Acceptability of printed wiring boards
IPC-ML-910A	Design and end production specification for rigid multi-layer boards
MIL-STD-275D	Printed wiring for electronic equipment
Workmanship standards	As published by Martin Marietta Aerospace

A complete manufacturing flow chart with QA involvement is shown in Figure 3. A comprehensive description of the FORCE COMPUTERS' quality system is available in handbook form: Quality Assurance and Reliability Handbook.

Figure 3 Quality Assurance Product Connected Target Areas



16-Bit CPU Boards

FORCE COMPUTERS

16-bit CPU Board Introduction

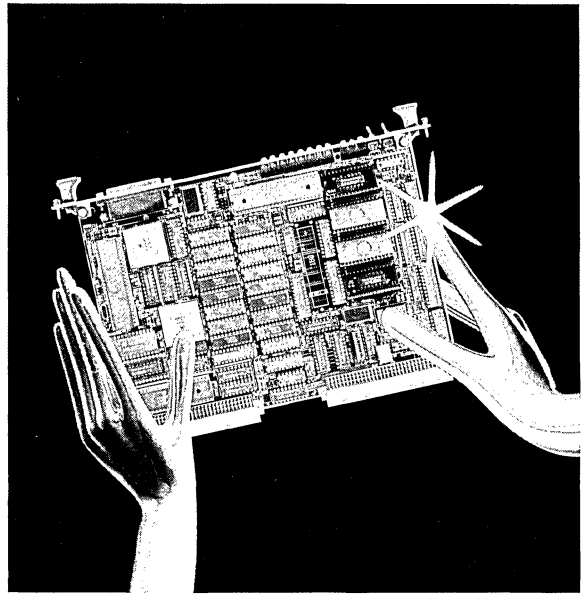
There are three basic designs in the FORCE family of 16-bit CPU boards. For general purpose flexibility and functionality, the SYS68K/CPU-6 provides all the features that the user could ever need. The CPU-6 family was designed as a functional update for the extremely popular CPU-1 family. It was designed for complete S/W compatibility to the CPU-1 family providing all the same features, whilst conforming fully to the IEEE 1014 VMEbus specification. The CPU-6 includes 512 Kbyte DRAM, 4 EPROM sockets and 2 serial I/O channels as standard. The CPU-6 is the general purpose 16-bit solution.

If your application requires that small to medium sized applications be committed to EPROM, then the SYS68K/CPU-4VC is designed especially for you. With 8 JEDEC compatible sockets, the user has 512 Kbyte of EPROM space. Coupled with the powerful 68010 microprocessor, DMA controller with optional floppy disk controller and serial and parallel I/O, the CPU-4VC is the standalone solution.

For true raw performance, the SYS68K/CPU-5A offers the maximum computing power available with a 16-bit 68000 microprocessor. With the local CPU and floating point co-processor running at 16.67 MHz and with the 128 Kbyte of local RAM inducing no wait states on the CPU, the CPU-5A is the 68000 performance standard.

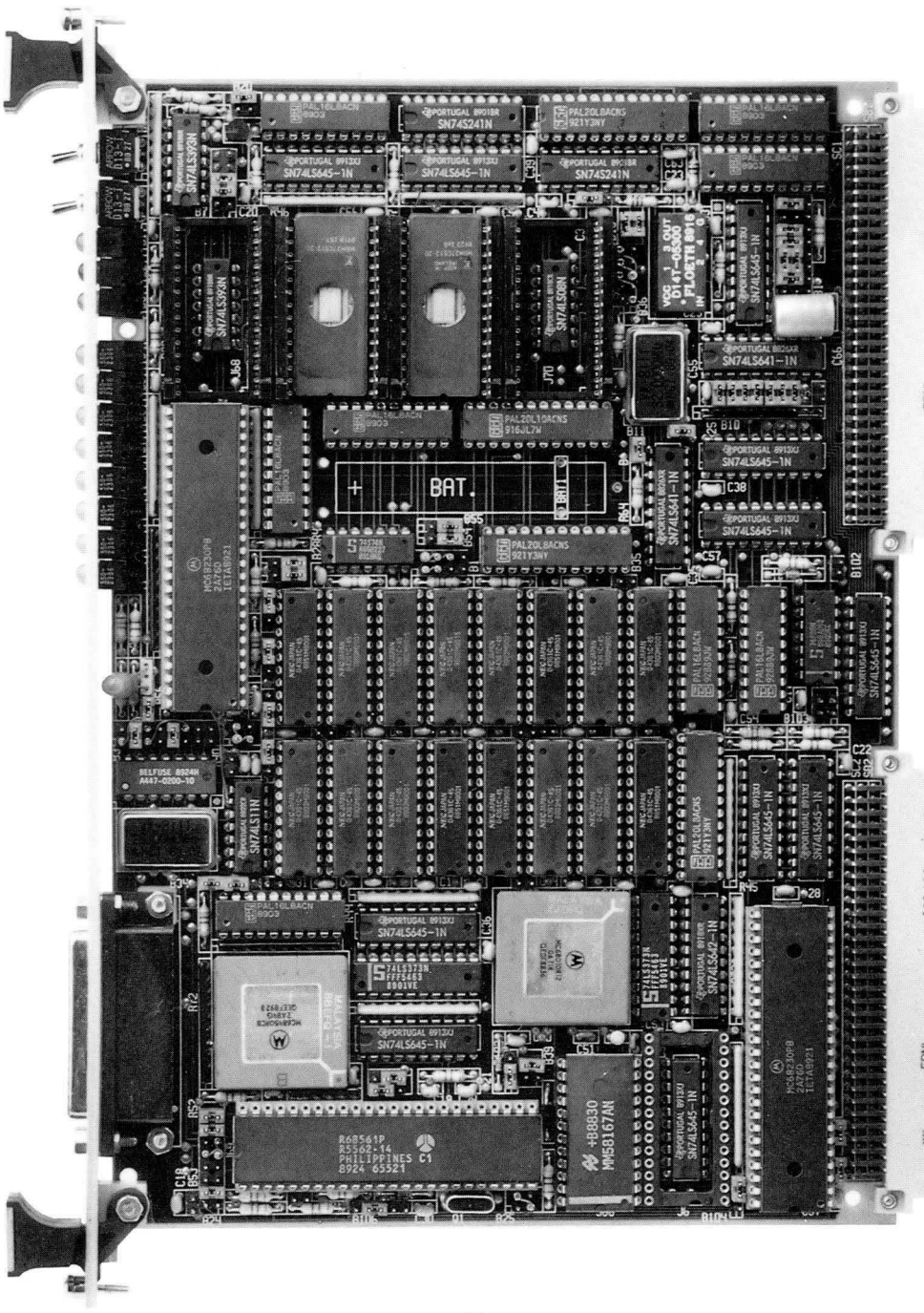
16-Bit CPU Boards (68000/68010-Based)

FAMILY	CPU-4VC	CPU-5A	CPU-6A	CPU-6VA
Processor type	68010	68000	68000	68010
FPCP type	no	68881	no	no
Frequency min. max.	12.5 MHz 12.5 MHz	16.7 MHz 16.7 MHz	12.5 MHz 12.5 MHz	12.5 MHz 12.5 MHz
DMAC type Frequency max.	68450 8 MHz	68450 8 MHz	no no	no no
Main memory type Capacity min. max. No. of wait states RAM function	SRAM (on-board back-up) 128 Kbyte 128 Kbyte 0 local	SRAM 128 Kbyte 128 Kbyte 0 local	DRAM 512 Kbyte 512 Kbyte 1 local	DRAM 512 Kbyte 512 Kbyte 1 local
No. of EPROM sockets Max. capacity Data bus width	8 512 Kbyte 16 Bit	4 256 Kbyte 16 Bit	4 256 Kbyte 16 Bit	4 256 Kbyte 16 Bit
Serial I/O (total) RS232 RS232/RS422/RS485 Controller chip	1 1 0 68561 (MPCC)	2 2 0 68561 (MPCC)	3 3 0 6850 (ACIA)	3 3 0 6850 (ACIA)
Parallel I/O	20 Bit	no	24 Bit	24 Bit
Timer	2 × 24 Bit	1 × 24 Bit	1 × 24 Bit	1 × 24 Bit
Real Time Clock	yes	no	yes	yes
Mass storage interface Floppy SCSI	 optional no	 no no	 no no	 no no
VMEbus arbiter	Four level	Single level	Single level	Single level
Secondary bus interface	no	VMX	no	no



System 68000 VME
SYS68K/CPU-4VC

68010 CPU Board with SRAM and Battery Back-up

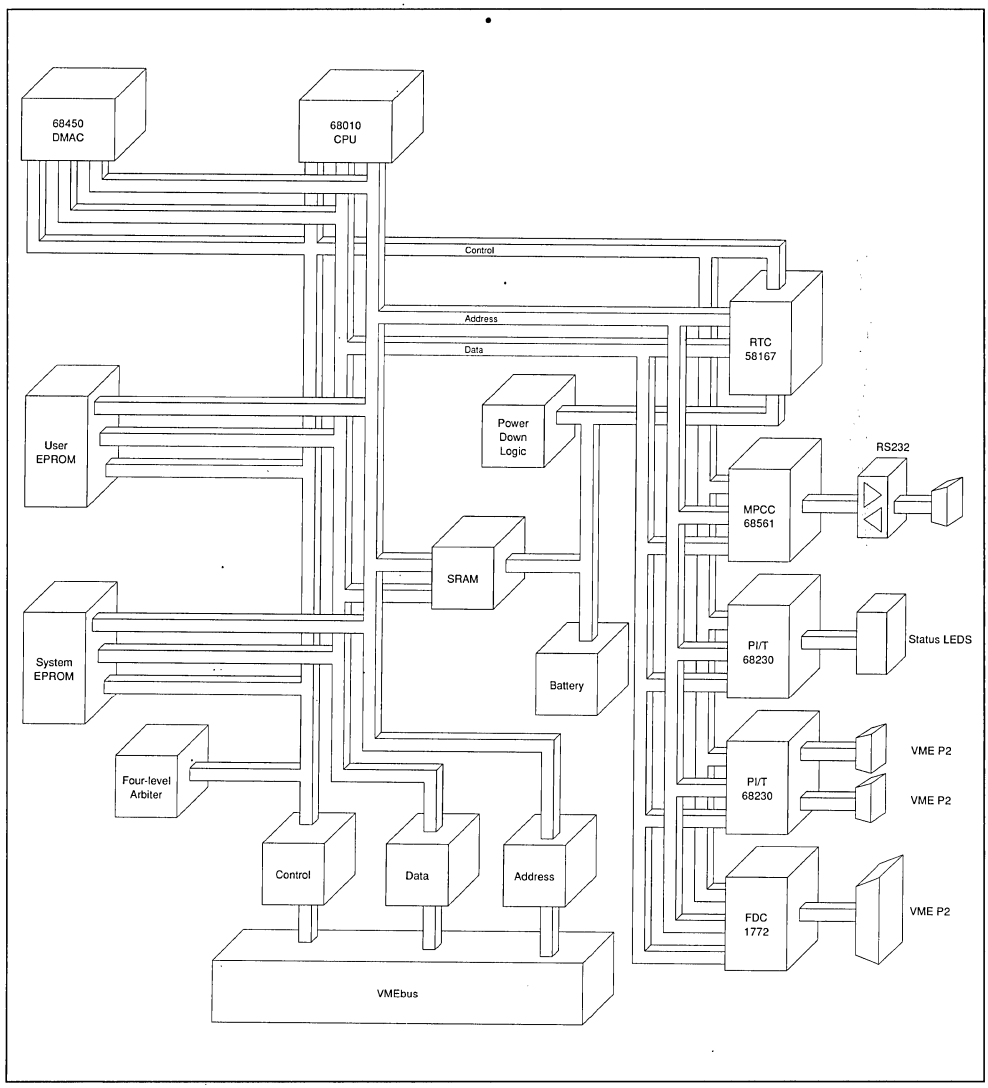

BAT.
SN74LS645-1N
SN74LS241N
SN74LS641-1N
PAL16L8ACN
PAL20L8ACNS
PAL20L10ACNS
PAL20L8ACNS
PAL16L8ACN
SN74LS640-1N
SN74LS373N
SN74LS138N
SN74LS32N
SN74LS11N
BELFUSE 8924H
A447-0200-10
R68561P
R5562-14
PHILIPPINES C1
8924 65521
MC68B30CP
MM58167AN

General Description

The SYS68K/CPU-4VC board is a high performance multi-processor computer board built around the virtual 68010 CPU and the VMEbus.
It contains a Direct Memory Access Controller, 128 Kbyte SRAM, up to 512 Kbyte EPROM and powerful control functions.

The implemented VMEbus interface is fully VMEbus and IEEE 1014 Standard compatible and includes a slave bus arbitration as well as a four level prioritized arbiter.
The block diagram shows the SYS68K/CPU-4VC board structure in detail.

Block Diagram of the SYS68K/CPU-4VC



Features of the SYS68K/CPU-4VC

- 68010 CPU with 12.5 MHz clock frequency
- 68450 Direct Memory Access Controller with 8 MHz clock frequency
- 68561 Multi-Protocol Communications Controller with an RS232-compatible interface
- 68230 Parallel Interface and Timer Module with 8 MHz clock frequency for local control and status display
- 68230 PI/T with 8 MHz clock frequency for parallel I/O on P2 connector
- 58167 Real Time Clock with battery back-up
- 128 Kbyte of high-speed static RAM with on-board battery back-up
- 8 EPROM sockets for system and/or user programs (max. 512 Kbyte)
- All on-board devices are able to interrupt the CPU
- 4 level bus arbiter (prioritized scheme)
- Bus requestor on a jumper-selectable level (0–3)
- RESET and ABORT function switches
- 8 status LEDs
- Powerful real time monitor/debugger VMEPROM on board
- High level real time operating systems are available for different applications
- Optionally available:
  1772 Floppy Disk Controller for up to four 3", 3½", 5¼" drives

Functional Description

The DMA Controller and Multi-Protocol Communication Controller communicate with the CPU via the unbuffered address and data bus. The EPROM areas, static RAM, Real Time Clock, Parallel Interface and Timer Module as well as the VMEbus interface communicate with the CPU via the buffered address bus.
Table 1 shows the global memory layout, and the various functional areas of the board are described briefly in the following paragraphs.

1. 68010 Central Processing Unit

The high performance 68010 CPU with its upgraded 68000 instruction set and virtual memory support offers a total of 16 Mbyte of addressable memory through its 24 address signals. The fully asynchronous 16-bit data bus allows high speed data transfers to/from the on-board or VMEbus memory and I/O areas.

The SYS68K/CPU-4VC series uses a 12.5 MHz 68010 processor. To provide for fault tolerant systems, the CPU provides excellent exception handling if an error or interrupt occurs. The state and all addresses as well as the fault address are stored on the stack to provide diagnostic and correction as well as re-run functions.

CPU-4VC Memory Layout

Address	Description
000000 to 000007	Start Vectors from System EPROM
000008 to 01FFFF	Static RAM
020000 to EFFFFF	VMEbus Addresses
F00000 to F7FFFF	System and User EPROM Area
F80000 to F8FFFF	Local I/O Devices
F90000 to FEFFFF	VMEbus Addresses
FF0000 to FFFFFF	Short I/O VMEbus Addresses

2. 68450 Direct Memory Access Controller

A high-speed DMA Controller with 8 MHz clock frequency is used on the board to move date to and from the VMEbus. Its four channels can be used from the operating system and/or shared with user programs.
The DMAC has a maximum data transfer speed of 4 Mbyte per second. Data can thus be loaded into the local RAM via the DMAC, giving time-critical number cruncher applications no time overhead through the VMEbus. This also results in a lower VMEbus load.

3. The Static RAM

The SYS68K/CPU-4VC contains a static memory of 128 Kbyte with a maximum access time of 70 nsec. A separate power-down logic on every board is used to disable the SRAM chips when the main power is out of spec. The on-board battery is used for the standby power of the SRAM chips (approx. 1000 h data retention).
Each static RAM access (read and write) of the processor runs without any wait states at 12.5 MHz clock frequency.

4. The System and User Area

The system area consists of two sockets for JEDEC-compatible EPROM devices. The VMEPROM firmware resides with its boot-up and I/O control functions in two EPROM devices (included in the shipment).
The user area (6 sockets) is provided for the use of EPROMs or SRAMs (JEDEC-compatible pin-out).

Usable Device Type for Each Area

Device	Type	Organi-zation	System Area	User Area1–3	Total Capacity
2764	EPROM	8 K × 8	X	X	64 Kbyte
27128	EPROM	16 K × 8	X	X	128 Kbyte
27256	EPROM	32 K × 8	X	X	256 Kbyte
27512	EPROM	64 K × 8	X	X	512 Kbyte
6264	SRAM	8 K × 8		X	32 Kbyte

The access speeds for the system and for the user areas are jumper-selectable from 100 nsec to 400 nsec.

5. 68561 Multi-Protocol Communication Controller (MPCC)

The MPCC contains different protocols to communicate via the RS232-compatible interface to a user-supplied serial communication device.

Protocols:
- IBM binary synchronous (ASCII or EBCDIC)
- Character oriented protocols (BSC, DDCMP, X3.38, X.21, ECMA 16 etc.)
- Synchronous bit-oriented protocols (SDLC, HDLC, ADCCP, X.25)

A software-programmable baud rate from 110 to 38400 baud and a local loop-back mode provide maximum flexibility.
The I/O signal assignment of the 4 input and 4 output signals to the 25-pin D-Sub connector on the front panel is jumper-selectable.
The MPCC is able to force an interrupt with 3 different software-programmable vectors to the CPU.

6. The Local Control

The Parallel Interface and Timer Module (PI/T) with its 8 MHz clock frequency allows an optical status display through eight yellow status LEDs on the front panel.
Each interrupt request level (0–7) can be enabled or disabled independently from each other through the CPU. The exception signals ACFAIL* and SYSFAIL* are monitored through the third PI/T port. The bus release functions are also software-programmable through the third port.
The PI/T includes a 24-bit programmable timer with a 5-bit prescaler. This timer may be used for measuring time delays or as a watchdog timer. The PI/T timer interrupt request signal is used to force an auto-vectored interrupt to the CPU.

7. The Parallel I/O Port

The second PI/T is used on the board to provide parallel I/O via the P2 connector. Two 8-bit bi-directional ports can be used for bit I/O or special control functions via 4 handshake interface signals.
The port interrupt causes an interrupt request to the on-board CPU on level 4. The 4 different software-programmable IRQ vectors offer maximum flexibility for program handling.

8. 58167 Programmable Real Time Clock

The on-board RTC with its RAM array allows various applications such as time scheduling, time measurement and time-out counters.
Additionally, the RTC may act as an actual time base independent from the main power, providing month, day of month, and day of week. An on-board battery ensures time base operation during power-down.

9. 1772 Floppy Disk Controller Option

The optionally available Single Chip Floppy Disk Controller (FDC) offers the capability of using the

SYS68K/CPU-4VC board versions in process control applications without any other mass memory controllers.
The FDC controls up to 4 different drives (3", 3½" or 5¼") either single or double sided with single or double density (software-programmable).
Additionally, the step-rate is software-programmable from 1 msec to 6 msec.
All drive select signals and status lines from the disk interface are controlled via the PI/T. Easy interface is provided through the P2 I/O pins, which fit into a 1 : 1 connection via a flat cable to the floppy drive edge connector.
An interrupt after operation completion can be generated to the CPU via the PI/T. For high asynchronous use of the floppy, the FDC is connected to the DMAC via its data request signal. The DMA is provided on the board to use the FDC in critical real-time applications. The CPU and the DMAC/FDC work fully asynchronous. The FDC may be ordered as an option for the CPU-4VC.

10. On-Board Exception Handling

The board contains two switches, one for RESET and one for ABORT. During an activated RESET, all on-board devices along with the CPU are reset. Additionally, the reset (SYSRESET*) can be forced to the VMEbus if this card is used as the system controller (slot 1 functions).
During a pushed ABORT switch, an interrupt (non-maskable) is forced to the CPU.

11. On-Board Interrupt Handling

All on-board devices are able to force interrupts to the CPU on different levels. Table 3 shows the interrupt structure of the SYS68K/CPU-4VC.

Device	Name	IRQ Level	Interrupt Auto Vector	Software-prog. Interrupt Vector
SWITCH	ABORT	7	X	
58167A	RTC	6	X	
68230	PI/T 1	5	X	
68230	PI/T 2	4		X
68561	MPCC	3		X
68450	DMAC	2		X

12. The VMEbus Interface

The implemented VMEbus interface includes 23 address, 16 data, 6 address modifier and different control signals.
A four-level bus arbiter with a prioritized scheme provides fast bus arbitration (if required).
A separate bus arbitration on a jumper-selectable level (0 – 3) provides the bus request/bus busy handshake to the used bus arbiter. Each VMEbus interrupt request level may be enabled or disabled via a jumper to provide multi-processing capabilities. The board supports the Release When Done (RWD), Release on Bus Clear (RBCLR) as well as the Release after Time-out (RAT) function (all software-programmable).
The 16 MHz SYSCLK signal can be driven to the VMEbus (jumper-selectable).

13. Software

It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE · regarding availability of any software not listed in this datasheet.

CPU-4 Software Support

Operating System/Kernel	Vendor/Support
PDOS	FORCE COMPUTERS
OS-9/9000	Contact FORCE for availability
VMEPROM	FORCE COMPUTERS
VxWORKS	Contact FORCE for availability
VRTX-32	Contact FORCE for availability
pSOS	Contact FORCE for availability

As a courtesy, FORCE provides the user with the ability to immediately start a real time application by including VMEPROM on every CPU card, free of charge and free of licensing costs.
VMEPROM is an EPROM-based Real Time Multi-tasking Kernel/Monitor. The complete package resides in 256 Kbyte of EPROM and uses 32 Kbyte of RAM. VMEPROM fully supports all of the on-board I/O devices.
VMEPROM is composed of a highly sophisticated Real Time Kernel, which is based on the PDOS Real Time Kernel. A file manager supporting sequential, random and shared files is also included.
The user interface contains more than 60 commands perfectly suited for program debugging, host computer communications, as well as task and file management. It includes a powerful debugger, supporting line assembler/disassembler for the microprocessor.

Features of VMEPROM

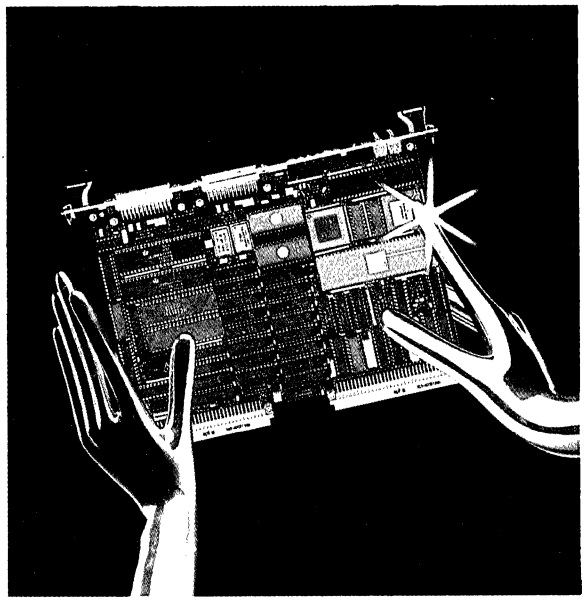
- Real Time Kernel supporting multi-tasking, up to 64 tasks
- File manager, supporting up to 64 open files at the same time
- Line assembler/disassembler with full support of all 680x0 instructions
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify
- S-record up/downloading from any port defined in the system
- Disk support for RAM disk, floppy and Winchester disks
- VMEPROM allows disk formatting and initialization
- Serial I/O support for up to two SIO-2 or ISIO-2 boards in the system; local serial I/O devices are also supported
- EPROM programming utility using the SYS68K/RR-2 board
- Full screen editor
- I/O re-direction to files or ports from the command line
- Over 100 system calls to the kernel

Specifications

68010	Frequency	12.5 MHz
68450	Frequency	8 MHz
Memory	SRAM Battery back-up EPROM	128 Kbyte/0 wait state yes 4 JEDEC Sockets 512 Kbyte (max)
Serial I/O	Channels Controller	1 (RS 232) 68561
Parallel I/O	Channels Width Controller	2 8-bit with 2-bit handshake 68230
Real Time Clock Controller		58167
VMEPROM firmware installed on all board versions		yes
VMEbus	Interface Arbiter	A24, A16 : D16, D8 (master) 4 level
Power requirements	+ 5 V + 12 V – 12 V	3.9 A (max) 0.2 A (max) 0.2 A (max)
Operating temperature Relative humidity Storage temperature		0 to + 50 °C 5 to 95 % – 40 to + 85 °C
Board dimensions		234 × 160 mm : 9.2 × 6.3 in

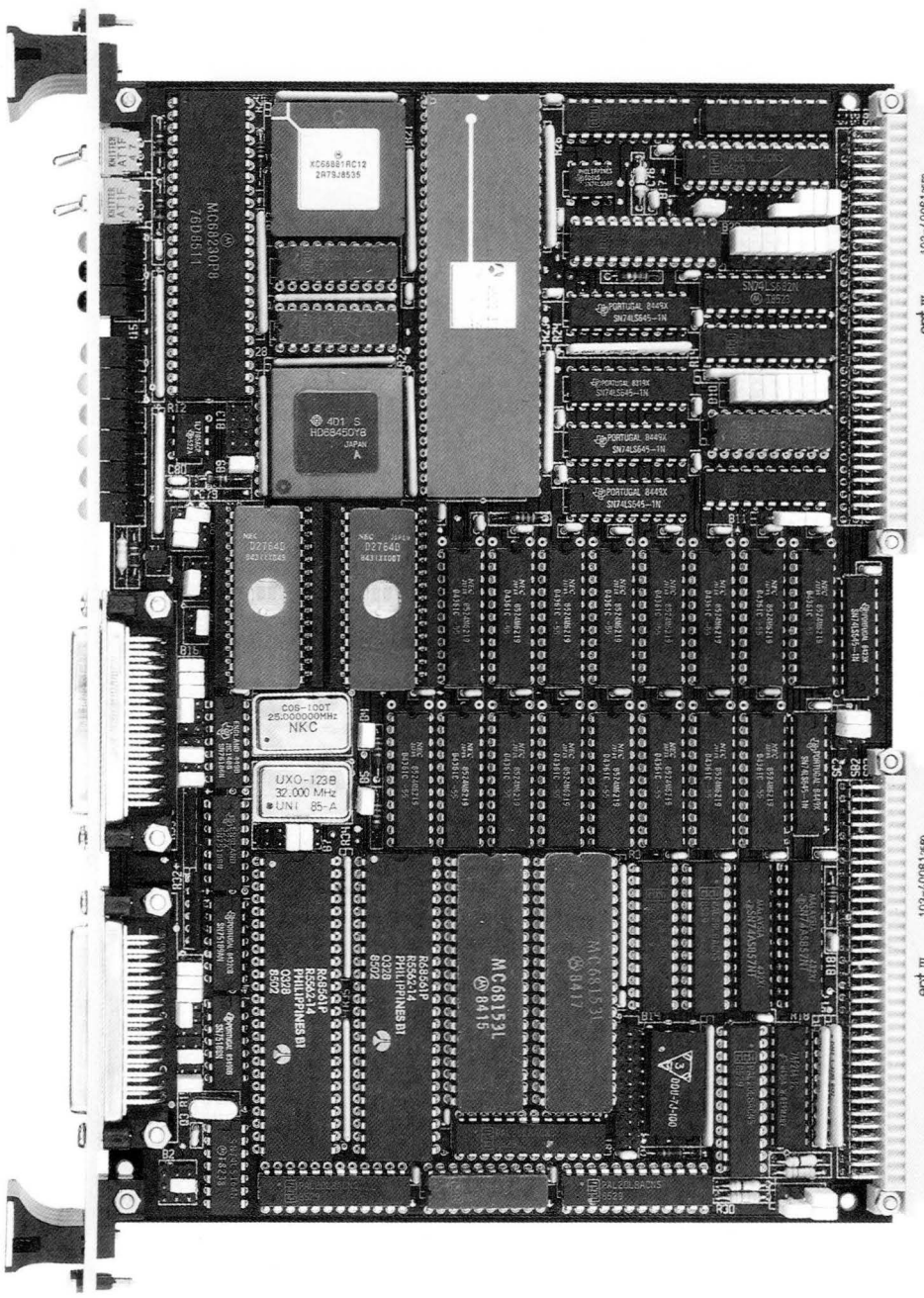
Ordering Information

SYS68K/CPU-4VC Part No. 100413	68010 CPU Board with 12.5 MHz CPU and 128 Kbyte SRAM (with battery back-up). VMEPROM and documentation included.
SYS68K/CPU-4FDC Part No. 110040	Floppy Disk Controller option (1772) supporting up to four drives (3", 3½", or 5¼").
SYS68K/VMEPROM/4/UP	VMEPROM update service for CPU-4 series.
SYS68K/CPU-4VC/UM Part No. 800102	User's Manual for CPU-4VC.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM User's Manual.



System 68000 VME
SYS68K/CPU-5A

16 MHz 68000 CPU with Floating Point Co-Processor


epf III 103-40081250
epf III 103-40081250

General Description

The SYS68K/CPU-5A boards are high speed computer boards built around the 68000 CPU and the Floating Point Co-Processor 68881. Zero wait state operation is performed at 16.7 MHz CPU clock frequency by accessing the 128 Kbyte high speed static RAM.

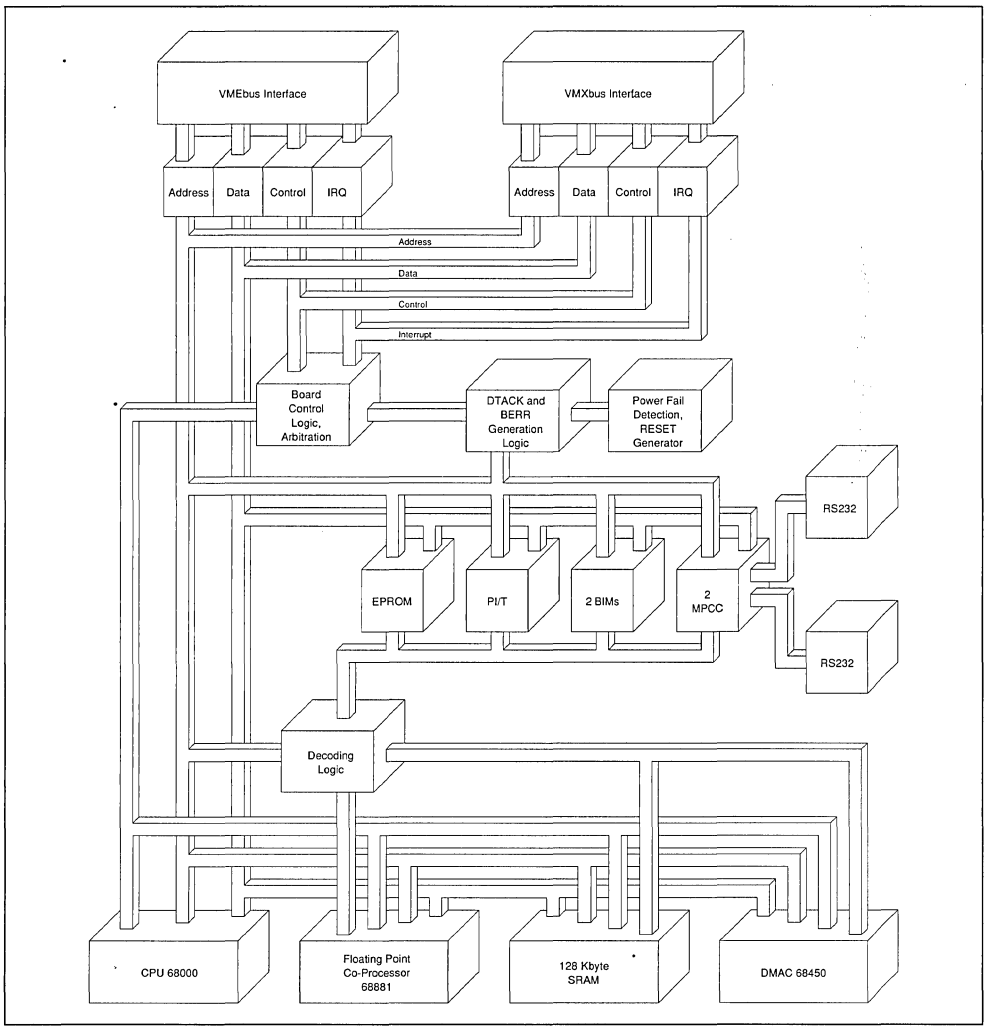
The installed four channel DMA Controller is capable of transferring data from memory to memory or from the two serial interfaces to memory.

One Parallel Interface and Timer Module offers a software-programmable timer as well as VMEbus exception signal handling.

The implemented VMEbus interface is fully VMEbus and IEEE 1014 Standard compatible and includes a one-level arbiter.

The primary VMXbus interface completes the board and offers optimized multi-processing support. The block diagram shows the board structure of the CPU-5 in detail.

Block Diagram of the SYS68K/CPU-5A



Features of the SYS68K/CPU-5A

- 68000 CPU with 16.7 MHz clock frequency
- 68881 Floating Point Co-Processor with 16.7 MHz clock frequency
- 68450 DMA Controller with 8 MHz clock frequency
- 68561 Multi-Protocol Communications Controllers with two RS232-compatible interfaces
- 68230 Parallel Interface and Timer Module with 8 MHz clock frequency
- 128 Kbyte of zero wait state static RAM
- 4 EPROM sockets for system and/or user programs
- All on-board interrupt requests are software-programmable (level and vector)
- Each VMEbus IRQ (1 to 7) can be enabled or disabled via software through the PI/T
- Single level arbiter
- VMEbus interface
  (A24 : D8, D16; A16 : D8, D16)
- VMXbus primary master interface (A24 : D16)
- Powerful Real Time Monitor/Debugger VMEPROM on-board
- 9 status LEDs, RESET and ABORT function switch

1. 68000 Central Processing Unit

The high performance 68000 CPU offers a total of 16 Mbyte of addressable memory through its 24 address signals. The fully asynchronous 16-bit data bus allows high speed data transfers to/from the on-board, VME- or VMXbus memory and I/O areas.
The SYS68K/CPU-5A uses a 16.7 MHz 68000 processor and runs constantly without wait states from the 128 Kbyte of static RAM.

The following table shows the global memory layout of the CPU-5A board:

Address	Description
000000 to 000007	Start Vectors from System EPROM
000008 to 01FFFF	On-board Static RAM (128 Kbyte)
020000 to xxxxxx	VME or VMXbus Addresses
xxxxxx to EFFFFF	VMX or VMEbus Addresses
F00000 to F3FFFF	System and User EPROM Area
F80000 to F8FFFF	Local I/O Devices
F90000 to FEFFFF	VMEbus Addresses
FF0000 to FFFFFF	Short I/O VMEbus Addresses

2. The Floating Point Co-Processor:

The 68881 Floating Point Co-Processor is a full implementation of the IEEE Standard 754 for Floating Point Arithmetic.

A set of 8 general Floating Point Data Registers, supporting full 80-bit extended precision are available for arithmetic operations such as:

Add	Sine, cosine, hyperbolic sine and cosine
Subtract	Tangent, cotangent, hyperbolic
Multiply	tangent and cotangent
Divide	e EXP(x)
Compare	e EXP(x–1)
Scale Exponent	E EXP(xtract (4))
Modulo	ln (x),ln (x + 1)
Conditional branches	log 10 (x),log2 (x)
Absolute value	2 EXP(x),10 EXP (x) Square root Conditional Trap (32)

The FPCP supports the following data types:
- Byte, word and long integers
- Single, double and extended precision real numbers
- Packed BCD string real numbers

The SYS68K/CPU-5A is fitted with a 16.7 MHz FPCP.

3. The Static RAM

Zero wait state operation for the CPU (16.7 MHz) and the DMAC (8 MHz) is provided by using the 16 static RAMs.
128 Kbyte of SRAM with maximum access time of 55 nsec is provided on each CPU-5A board for program and/or data storage.

4. The System and User Area

The CPU-5A contains four sockets for JEDEC-compatible EPROM devices. Two 27512 devices are used for VMEPROM (included in the shipment).
The following table lists the usable EPROM types for each area.

Device	Organization	Total Capacity
2764	8 K × 8	32 Kbyte
27128	16 K × 8	64 Kbyte
27256	32 K × 8	128 Kbyte
27512	64 K × 8	256 Kbyte

The access time for both areas is jumper-selectable in the range of 100-400 nsec to adapt different EPROM access times.

5. 68450 Direct Memory Access Controller

A high-speed DMA Controller with 8 MHz clock frequency is used on the board to move data on the local, VMX- and the VMEbus. Its four channels can be used from the operating system and/or shared with user programs.
The DMAC has a maximum data transfer speed of 4 Mbyte per second. Time critical programs can thus be loaded into the local RAM via the DMAC, which allows number cruncher applications to run without the time overhead through the VME/VMXbus. This also results in a lower bus load.

6. 68561 Multi-Protocol Communication Controllers (MPCC)

The CPU-5A board contains two serial interfaces for communication to a terminal and/or printer/host computer.
The MPCC offers different protocols to communicate via the RS232-compatible interface to a user-supplied serial communication device.

Protocols:
- IBM binary synchronous (ASCII or EBCDIC)
- Character oriented protocols (BSC, DDCMP, X3.28, X.21, ECMA 16 etc.)
- Synchronous bit-oriented protocols (SDLC, HDLC, ADCCP, X.25)

A software-programmable baud rate from 110 to 38400 baud and a local loop-back mode provide maximum flexibility.
The I/O signal assignment of the 4 input and 4 output signals per channel to the 25-pin D-Sub connectors on the front panel is jumper-selectable.

The MPCC is able to force an interrupt with 3 different software-programmable vectors to the CPU.

7. The Local Control

The Parallel Interface and Timer Module (PI/T) with its 8 MHz clock frequency allows an optical status display through six yellow status LEDs mounted on the front panel.
Each interrupt request level from the VMEbus can be enabled or disabled independently from each other through the CPU (dynamically). The VMEbus signals ACFAIL* and SYSFAIL* are monitored through the third PI/T port.
The bus release functions described in the VMEbus section are also software-programmable. The PI/T includes a 24-bit programmable timer with a 5-bit prescaler. This timer may be used for measuring time delays or as a watchdog timer.

8. The Interrupt Structure

The CPU-5A contains two Bus Interrupter Modules to provide a flexible interrupt structure for multi-processor applications.
Each on-board interrupt request is software-programmable to one of the IRQ levels of the CPU. The vector is also software-programmable.
The following table lists all the on-board interrupt sources:

Interrupt	Device
ABORT	SWITCH
TIMER	PI/T
Serial I/O 1	MPCC 1
Serial I/O 2	MPCC 2
DMAC	DMAC
ACFAIL*	VMEbus
SYSFAIL*	VMEbus
IRQVMX	VMXbus

The VMXbus interrupt request is routed into the on-board IRQ structure to offer maximum flexibility (software-programmable level and vector).
The VMEbus interrupt requests can be dynamically enabled or disabled to the CPU through the PI/T device. This allows dynamic adaption for high end multi-processor environments because each of the IRQs (1–7) can be selected separately under run time of the CPU (no jumper settings are required).

9. The VMXbus Interface

The CPU-5A board contains a primary VMXbus interface with a jumper-selectable access address range in the whole address space of 16 Mbyte. 24 address lines and 16 data lines are supported from the VMXbus interface. The early DTACK option can be used to speed up the access cycles.

10. The VMEbus Interface

The implemented VMEbus interface supports 24 address, 16 data, 6 address modifiers and different control signals.
The transfer of 8 and 16 bits of data (A24 : D8, D16) is supported. Software-programmable bus release functions allow flexible adjustment to the various application dependent requirements.

ROR = Release On Request
RBCLR = Release On Bus Clear
RAT = Release After Time-Out
RWD = Release When Done

The single level arbiter included on the board simplifies installation of the CPU-5A into a VMEbus environment.

11. Software

It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-5 Software Support

Operating System/Kernel	Vendor/Support
PDOS	FORCE COMPUTERS
OS-9/9000	Contact FORCE for availability
VMEPROM	FORCE COMPUTERS
VxWORKS	Contact FORCE for availability
VRTX-32	Contact FORCE for availability
pSOS	Contact FORCE for availability

As a courtesy, FORCE provides the user with the ability to immediately start a real time application by including VMEPROM on every CPU card, free of charge and free of licensing costs.
VMEPROM is an EPROM-based Real Time Multi-tasking Kernel/Monitor. The complete package resides in 256 Kbyte of EPROM and uses 32 Kbyte of RAM. VMEPROM fully supports all of the on-board I/O devices.
VMEPROM is composed of a highly sophisticated Real Time Kernel, which is based on the PDOS Real Time Kernel. A file manager supporting sequential, random and shared files is also included.
The user interface contains more than 60 commands perfectly suited for program debugging, host computer communications, as well as task and file management. It includes a powerful debugger, supporting line assembler/disassembler for the microprocessor.

Features of VMEPROM

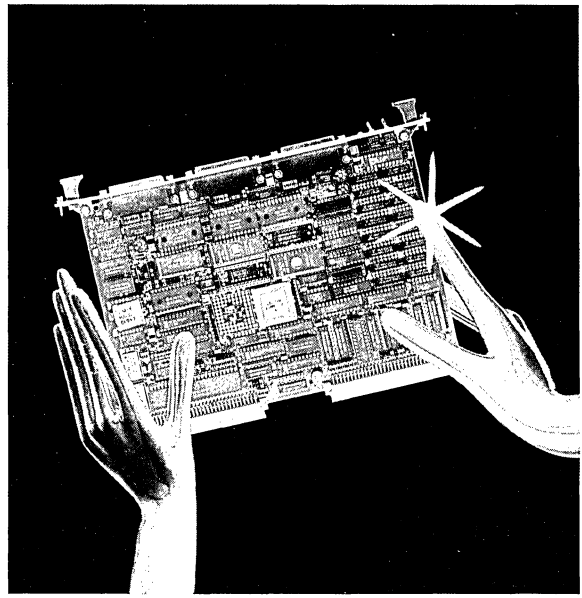
- Real Time Kernel supporting multi-tasking, up to 64 tasks
- File manager, supporting up to 64 open files at the same time
- Line assembler/disassembler with full support of all 680x0 instructions
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify
- S-record up/downloading from any port defined in the system
- Disk support for RAM disk, floppy and Winchester disks
- VMEPROM allows disk formatting and initialization
- Serial I/O support for up to two SIO-2 or ISIO-2 boards in the system; local serial I/O devices are also supported
- EPROM programming utility using the SYS68K/RR-2 board
- Full screen editor
- I/O re-direction to files or ports from the command line
- Over 100 system calls to the kernel

Specifications

68000 frequency	16.7 MHz
68881 frequency	16.7 MHz
68450 frequency	8 MHz
Memory SRAM Wait states EPROM	128 Kbyte 0 4 JEDEC Sockets 256 Kbyte (max)
Serial I/O channels controller	2 (RS 232) 68561
VMEPROM firmware installed on all board versions	yes
VMXbus interface	A24, A16, D16 (Primary I/F)
VMEbus interface arbiter interrupts	A24, A16 : D16, D8 (master) Single level IH 1–7
Power requirements + 5 V + 12 V – 12 V	5.0 A (max) 0.2 A (max) 0.2 A (max)
Operating temperature Storage temperature Relative humidity (non-condensing)	0 to + 50 °C – 50 to + 85 °C 5 to 95 %
Board dimensions	234 × 160 mm : 9.2 × 6.3 in

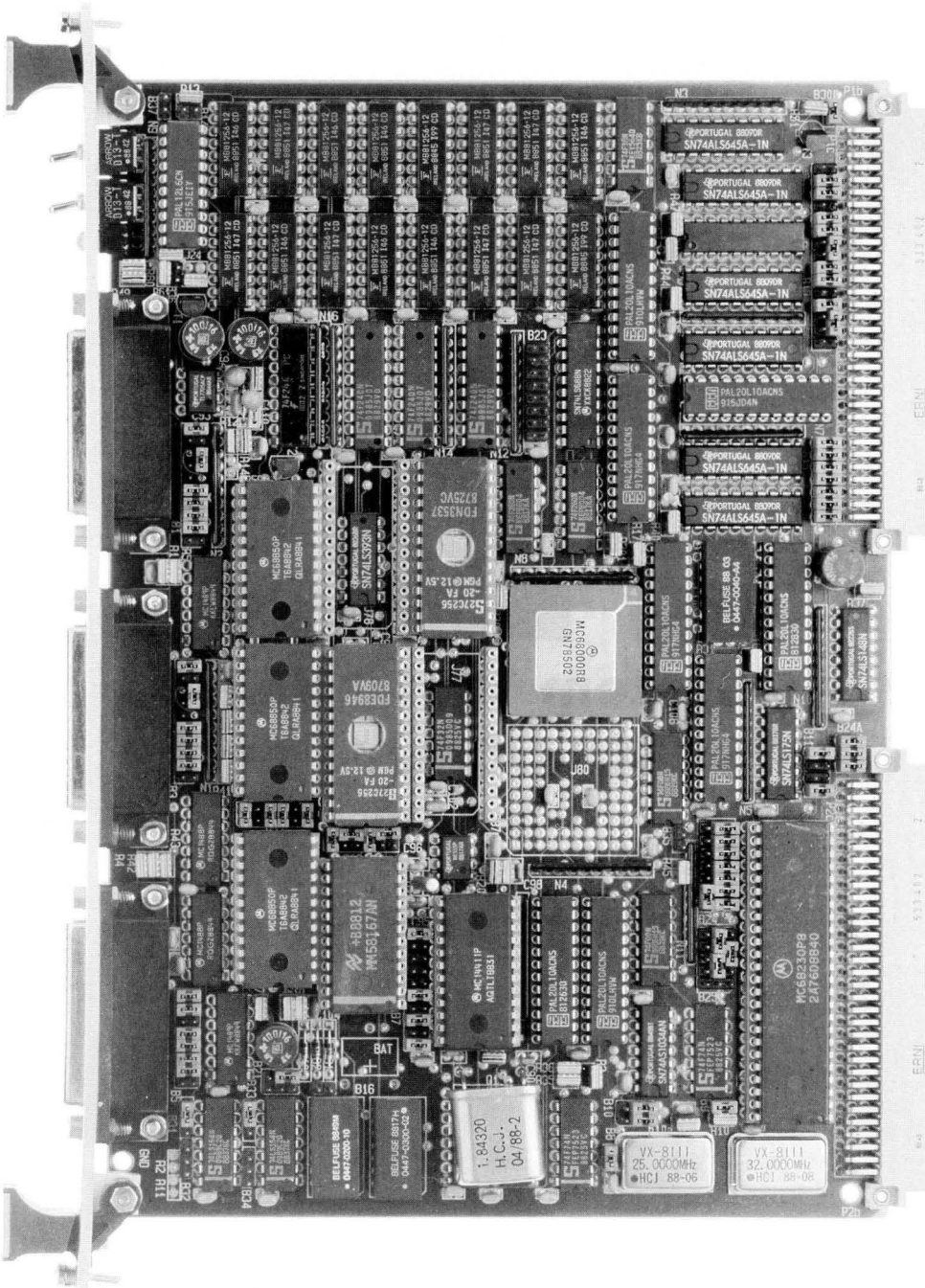
Ordering Information

SYS68K/CPU-5A Part No. 100501	16.7 MHz 68000 CPU board with Floating Point Co-Processor (16.7 MHz) and VMEPROM. Documentation included.
SYS68K/VMEPROM/5/UP Part No. 145104	VMEPROM Update service for CPU-5 series.
SYS68K/CPU-5A/UM Part No. 800078	User's Manual for CPU-5A.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM User's Manual.



System 68000 VME
SYS68K/CPU-6

Flexible General Purpose 16-Bit CPU Board with Floating Point



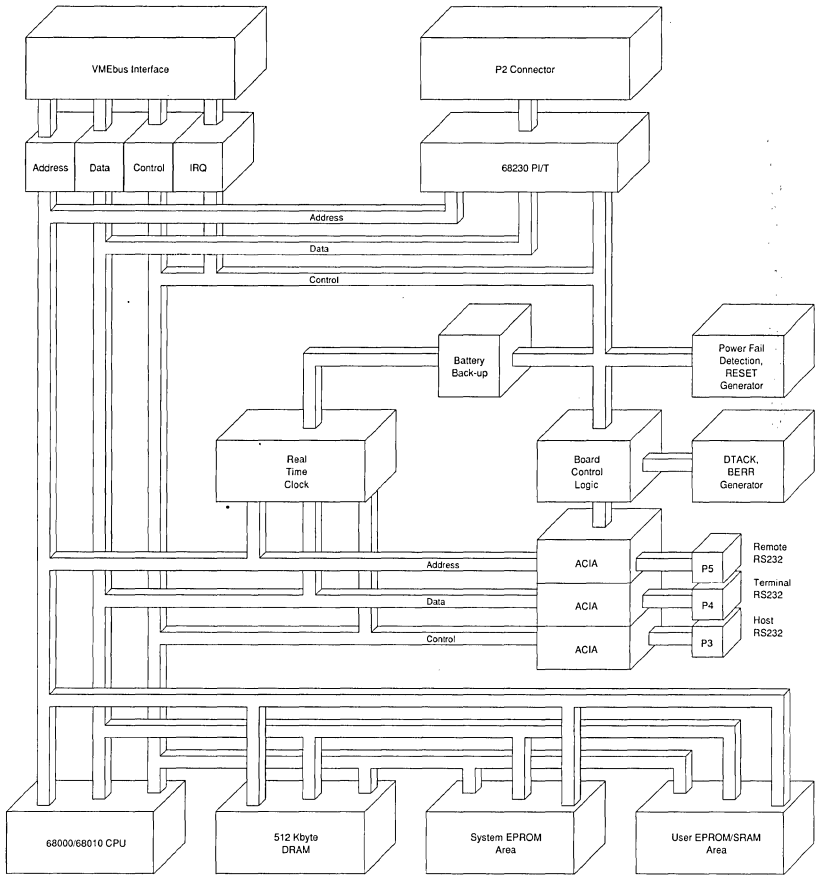
General Description

The general purpose SYS68K/CPU-6 board is a high speed VMEbus board based on a 68000/68010 processor. It contains 512 Kbyte of dynamic RAM, 3 serial I/O interfaces, up to 256 Kbyte of EPROM and a parallel I/O interface as well as a Real Time Clock.

The implemented VMEbus interface is IEEE 1014 Standard compatible, and features a single level arbiter, a SYSCLK driver and a power monitor/ RESET generator.

Details of the structure of CPU-6 are shown in the block diagram.

Block Diagram of the SYS68K/CPU-6



Features of the SYS68K/CPU-6

- 68000 CPU (12.5 MHz) on CPU-6A
  68010 CPU (12.5 MHz) on CPU-6VA
- 512 Kbyte of dynamic RAM
  1 wait state at 12.5 MHz
  Distributed hardware refresh every 15 µsec
- 4 EPROM sockets provide 256 Kbyte space
- 3 serial communication ports (RS232-compatible)
- Parallel I/O interface to P2 connector
- Real Time Clock with on-board battery back-up
- 24-bit timer with 5-bit prescaler
- Local interrupt service via auto-vectoring
- Fully VMEbus IEEE 1014 Standard compatible
- RESET and ABORT function switches
- Double Eurocard form factor
- Powerful Real Time Monitor/Debugger VMEPROM on board
- Fully software and I/O signal compatible to the SYS68K/CPU-1B series

1. 68000/68010 Central Processing Unit

The high performance 68010 CPU with its upgraded 68000 instruction set and virtual memory support offers a total of 16 Mbyte of addressable memory through its 23 address signals. The fully asynchronous 16-bit data bus allows high speed data transfer to/from the on-board and VMEbus memory.

2. The Dynamic RAM

512 Kbyte DRAM is provided on all CPU-6 versions.
CPU-6A and 6VA are equipped with a 12.5 MHz processor and need only 1 wait state to read data from the local DRAM.
For critical real time applications the distributed "RAS only" refresh can delay every 15 msec a pending access for a maximum of 290 nsec. The refresh works asynchronous to the CPU and guarantees refreshing of the DRAMs independent of the processor state.

The global memory layout and the I/O address assignment are outlined below:

START Address	END Address	Type
000000	000007	Initialization vectors from system EPROM
000008	07FFFF	Dynamic RAM
080008	09FFFF	System EPROM
0A0000	0BFFFF	User EPROM
0C0000	0FFFFF	I/O interfaces
100000	FEFFFF	VMEbus standard addressing (A24:)
FF0000	FFFFFF	VMEbus short I/O addressing (A16:)

3. The EPROM Memory

The SYS68K/CPU-6 contains two different EPROM banks, both 16 bits wide and 128 Kbyte deep. The System Area and the User Area can be configured for the following devices:

Device	Type	Organization	System Area	User Area
2764	EPROM	8 K×8	x	x
27128	EPROM	16 K×8	x	x
27256	EPROM	32 K×8	x	x
27512	EPROM	64 K×8	x	x
6264	SRAM	8 K×8		x
62256	SRAM	32 K×8		x

The total capacity of both areas is 256 Kbyte using four 27512 devices. Access time selection between 150 and 350 nsec for both areas allows the use of a wide variety of chips.

4. Serial Communication Ports
Three asynchronous serial communication ports (using a 68B50 ACIA chip) designated for the terminal, for the host, and for user applications are provided on the board. All of these ports are RS232-compatible. The terminal acts as a user interface and works in conjunction with VMEPPROM. A transparent mode condition is callable via the system monitor. This transparent mode effectively bypasses the board and allows the terminal to communicate directly with the host. The third serial communication port interfaces either to a printer or acts as a remote link to another computer. Each serial port has a jumper-selectable data transfer rate (110–9600 or 600–19200 baud). For each serial port, each of the I/O signals can be assigned to one of the 25-pin D-sub female connectors on the front panel.

5. Parallel I/O
The board contains a Parallel Interface and Timer chip (PI/T 68230) with a clock frequency of 8 MHz. The PI/T operates in uni- or bi-directional mode either 8 or 16 bits wide.
Each of the I/O lines can be configured as an input or as an output by programming the PI/T.
For asynchronous software control, the third 8-bit port can be configured to drive an interrupt on level 5 to the CPU.

6. Programmable Timer
The PI/T includes a 24-bit programmable timer with a 5-bit prescaler. The timer is a synchronous counter to be used for generating or measuring time delays and various frequencies.

7. Programmable Real Time Clock
The on-board Real Time Clock (58167 ARTC) allows various applications, such as time scheduling, time comparison, time-out counter, etc. Additionally, the RTC may act as an actual time base providing month, day of month and day of week. An on-board battery back-up ensures time base operating during power-down times.

8. On-Board Interrupt Handling
All on-board devices are able to force interrupts on different levels to the CPU. In this case the auto-interrupt vector of the 68000 will be forced and each device has its own interrupt vector.

The following table shows the interrupt structure of the CPU-6.

Description	Device	Level	Vector No.
ABORT	Switch	7	31
Real Time Clock	58167A	6	30
Parallel Interface and Timer	68230	5	29
Terminal ACIA	68B50	4	28
Remote ACIA	68B50	3	27
Host ACIA	68B50	2	26

9. The VMEbus Interrupts
Each of the 7 defined VMEbus IRQs can be separately enabled or disabled for servicing through the local CPU. Only a jumper setting is required to enable the corresponding VMEbus IRQ.

10. The VMEbus Interface
The implemented VMEbus interface supports 23 address, 16 data, 6 address modifier and all the control signals defined in the IEEE 1014 Standard. All the electrical, mechanical and timing specifications are realized on the CPU-6 series of boards.
The following address and data transfer types are supported:

A16 : D8, D16
A24 : D8, D16

To support single processor and multi-master applications, CPU-6 includes a Single Level Arbiter and a SYSCLK driver. Both functions can be disabled for multi-processor applications.
Bus mastership is only requested if the VMEbus is addressed. The level is jumper-selectable (0, 1, 2 or 3). A time-out counter for bus mastership (RAT) and the Release on Bus Clear (RBCLR) options are installed on the board to allow the use of CPU-6 in high end multi-processor environments.
A RESET generator, a power monitor and a time-out counter for local and VMEbus accesses completes the board.

11. Software

It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-6 Software Support

Operating System/Kernel	Vendor/Support
PDOS	FORCE COMPUTERS
OS-9/9000	FORCE COMPUTERS/ MICROWARE
VMEPROM	FORCE COMPUTERS
VxWORKS	Contact FORCE for availability
VRTX-32	Contact FORCE for availability
pSOS	SOFTWARE COMPONENT GROUP
ARTX	Contact FORCE for availability
Telesoft ADA	Contact FORCE for availability

As a courtesy, FORCE provides the user with the ability to immediately start a real time application by including VMEPROM on every CPU card, free of charge and free of licensing costs.
VMEPROM is an EPROM-based Real Time Multi-tasking Kernel/Monitor. The complete package resides in 256 Kbyte of EPROM and uses 32 Kbyte of RAM. VMEPROM fully supports all of the on-board I/O devices.
VMEPROM is composed of a highly sophisticated Real Time Kernel, which is based on the PDOS Real Time Kernel. A file manager supporting sequential, random and shared files is also included.
The user interface contains more than 60 commands perfectly suited for program debugging, host computer communications, as well as task and file management. It includes a powerful debugger, supporting line assembler/disassembler for the microprocessor.

Features of VMEPROM

- Real Time Kernel supporting multi-tasking, up to 64 tasks
- File manager, supporting up to 64 open files at the same time
- Line assembler/disassembler with full support of all 680x0 instructions
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify
- S-record up/downloading from any port defined in the system
- Disk support for RAM disk, floppy and Winchester disks
- VMEPROM allows disk formatting and initialization
- Serial I/O support for up to two SIO-2 or ISIO-2 boards in the system; local serial I/O devices are also supported
- EPROM programming utility using the SYS68K/RR-2 board
- Full screen editor
- I/O re-direction to files or ports from the command line
- Over 100 system calls to the kernel

Specifications

CPU	68000, 12.5 MHz CPU-6A 68010, 12.5 MHz CPU-6VA
DRAM	512 Kbyte dynamic RAM 1 wait state at 12.5 MHz Distributed hardware refresh
EPROM	128 Kbyte for the System area 16–128 Kbyte for the User area
Serial I/O	3 RS232 interfaces built with 6850 devices (ACIA) Strap selectable baud rate from 110–19200 baud Strap selectable I/O signal assignments to the three 25-pin D-Sub connectors.
Parallel I/O	68230 PI/T with 24 I/O signals connected to P2 connector
Timer	24-bit timer included in the PI/T
Real Time Clock	58167 RTC with on-board battery back-up
Interrupts	All on-board devices are capable of generating interrupts to the CPU on a fixed IRQ level. Local interrupts do not cause a VMEbus request.
VMEbus interface	Jumper-selectable VMEbus request level (0–3) Transfer modes A16 : D8, D16 A24 : D8, D16 Interrupt Handler (1–7) Single level arbiter SYSCLK driver Power monitor RESET generator Bus Release Options: RBCLR, RAT
VMEPROM firmware installed on all board versions	yes
Power requirements	+ 5 V/2.9 A + 12 V/0.2 A – 12 V/0.2 A
Operating temperature Storage temperature Relative humidity (non-condensing)	0 to + 50 °C – 50 to + 85 °C 5 to 95 %
Board dimensions	Double Eurocard 234 × 160 mm : 9.2 × 6.3 in

Ordering Information

SYS68K/CPU-6A Part No. 100602	68000 CPU Board (12.5 MHz), 512 Kbyte DRAM. Documentation included.
SYS68K/CPU-6VA Part No. 100610	68010 CPU Board (12.5 MHz), 512 Kbyte DRAM. Documentation included.
SYS68K/VMEPROM/6/UP Part No. 145105	VMEPROM update service for CPU-6 series.
SYS68K/CPU-6/UM Part No. 800094	User's Manual for all CPU-6 products.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM User's Manual.

32-Bit CPU Boards

FORCE COMPUTERS

32-bit CPU Board Introduction

The depth of features and performance available from the range of 32-bit CPU boards from FORCE COMPUTERS is truely without parallel. With 15 different CPU types, all with memory density and clock frequency variations, the offering covers all application areas.

FORCE COMPUTERS has earned an excellent reputation for performance, quality and support. This reputation, coupled with a commitment to timely product delivery has made FORCE the number 1 supplier for performance solutions on the VMEbus. The design of the FGA-002, supporting multi-processing features such as FORCE Message Broadcast (FMB) and Synchronized Dual Ported RAM (S-DPR) have benefitted the entire VMEbus community.

The CPU-33 is the entry level 32-bit performance board. It features 1 Mbyte or 4 Mbyte of shared memory, a 68030 processor plus the FGA-002 with FMB and DMA. For single board solution applications, the performance of the CPU-30 is unsurpassed. The CPU-30 offers up to 16 Mbyte of DRAM, 4 serial ports, one parallel port, SCSI, floppy disk and Ethernet interfaces. The FGA-002 and a floating point unit are also installed as standard. The CPU-30 architecture is also offered in 68020 based boards as CPU-23 (SRAM) and CPU-26 (DRAM).

For multiprocessing applications, the CPU-22 (68020) and CPU-31 (68030) offer unique features such as the Synchronized Dual Ported RAM, which allows continuous zero wait state performance for the on-board CPU, even during VMEbus accesses. The FMB message broadcast facility, multiprocessor mailboxes and high speed DMA controller all contribute to provide the most comprehensive multiprocessing solutions for the VMEbus.

For true performance, both the CPU-29 (68020) and the CPU-32 (68030) offer zero wait state operation for the processor on all memory cycles, all the way up to 30 MHz. This has been achieved only through the use of high speed logic and the fastest available SRAMs.

RISC performance is also offered with the CPU-80 and CPU-81 88100 based RISC processor boards. The dual cache/memory management architecture gives these boards the ultimate in performance capabilities. Coupled with up to 16 Mbyte of shared DRAM and VSB/SCSI, serial I/O and full VMEbus slot 1 capability provides the ideal performance VMEbus solution.

For true 680x0 upward compatibility coupled with RISC performance levels, the CPU-40/41 is the ultimate. The CPU-40/41 family offers the flexibility to be an upgrade to CPU-30, CPU-31 or CPU-33. Hardware and software compatibility with existing products has been achieved through the use of an ingenious modular approach called FLXi. The CPU-40/41 are the solution for the 1990s.

32-Bit CPU Boards (68020-Based)

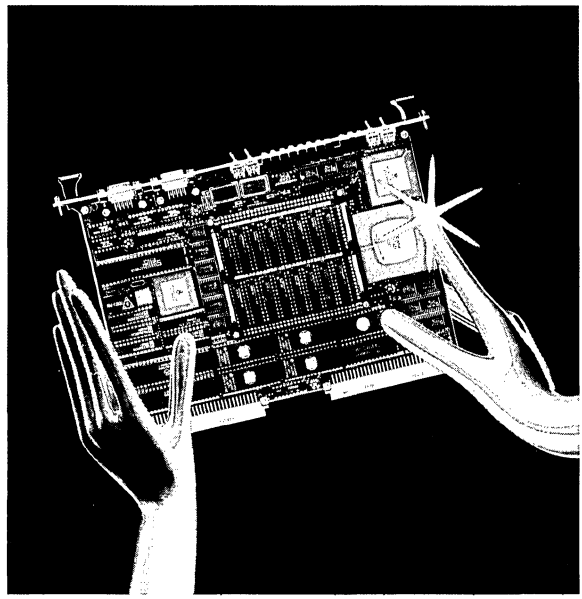
FAMILY	CPU-22	CPU-23	CPU-26	CPU-27	CPU-29
Processor type	68020	68020	68020	68020	68020
FPCP type	68882	68882	68882	68882	68882
Frequency min. max.	16.7 MHz 20.0 MHz	12.5 MHz 25.0 MHz	12.5 MHz 20.0 MHz	16.7 MHz 25.0 MHz	16.7 MHz 30.0 MHz
DMAC type Frequency max.	FGA-002 20.0 MHz	FGA-002 25.0 MHz	FGA-002 20.0 MHz	no no	no no
Main memory type Capacity min. max. No. of wait states RAM function	SRAM 1 Mbyte 1 Mbyte 0 S-DPR	SRAM 1 Mbyte 1 Mbyte 0/2 shared	DRAM 1 Mbyte 4 Mbyte 0/2 shared	SRAM 1 Mbyte 1 Mbyte 0/2 local	SRAM 1 Mbyte 1 Mbyte 0 local
SRAM (on-board battery back-up)	32 Kbyte (default) 512 Kbyte (max.)	32 Kbyte (default) 512 Kbyte (max.)	32 Kbyte (default) 512 Kbyte (max.)	32 Kbyte (default) 512 Kbyte (max.)	No
No. of EPROM sockets Max. capacity Data bus width	4 4 Mbyte 32 Bit	4 4 Mbyte 32 Bit	4 4 Mbyte 32 Bit	2 2 Mbyte 16 Bit	4 4 Mbyte 32 Bit
Serial I/O (total) RS232 only RS232/RS422/RS485 Controller chip	2 0 2 68562 (DUSCC)	4 0 4 2x68562 (DUSCC)	4 0 4 2x68562 (DUSCC)	3 0 3 68901 (MFP/1), 68562 (DUSCC/2)	2 1 1 2x68561 (MPCC)
Parallel I/O	12 Bit	12 Bit	12 Bit	38 Bit	12 Bit
Timer (8 bit/24 bit)	1/2	1/2	1/2	0/2	0/2
Real Time Clock	yes (72421)	yes (72421)	yes (72421)	yes (72421)	yes (72421)
Mass storage interface Floppy SCSI	 no no	 yes, with DMA yes, with DMA	 yes, with DMA yes, with DMA	 No Yes	 No No
Ethernet interface	no	no	no	optional, with 64 Kbyte buffer	No
Multiprocessing support	FMB 8 mailboxes remote reset	FMB 8 mailboxes remote reset	FMB 8 mailboxes remote reset	no	no
VMEbus arbiter	Single level	Single level	Single level	Single level	Single level
Secondary bus interface	VMX with DMA	no	no	no	VSB

32-Bit CPU Boards (68030 Based)

FAMILY	CPU-30	CPU-31	CPU-32	CPU-33
Processor type	68030	68030	68030	68030
FPCP type	68882	68882	68882	68882
MMU type	68030 (on-chip)	68030 (on-chip)	68030 (on-chip)	68030 (on-chip)
Frequency min. max.	20.0 MHz 25.0 MHz	20.0 MHz 25.0 MHz	25.0 MHz 30.0 MHz	16.7 MHz 25.0 MHz
DMAC type Frequency max.	FGA-002 25.0 MHz	FGA-002 25.0 MHz	no no	FGA-002 25.0 MHz
Main memory type Capacity min. max. No. of wait states RAM function	DRAM (burst fill) 4 Mbyte 16 Mbyte 0/2 shared	SRAM 1 Mbyte 1 Mbyte 0 S-DPR	SRAM 1 Mbyte 1 Mbyte 0 local	DRAM 1 Mbyte 4 Mbyte 0/2 shared
SRAM (on-board battery back-up)	32 Kbyte (default) 512 Kbyte (max.)	32 Kbyte (default) 512 Kbyte (max.)	no	2 Kbyte 512 Kbyte (max.)
No. of EPROM Sockets Max. capacity Data bus width	4 4 Mbyte 32 Bit	4 4 Mbyte 32 Bit	4 4 Mbyte 32 Bit	2 2 Mbyte 16 Bit
Serial I/O (total) RS232 only RS232/RS422/RS485 Controller chip	4 1 3 68562 (DUSCC)	2 0 2 68562 (DUSCC)	2 1 1 68561 (MPCC)	2 0 2 68562 (DUSCC)
Parallel I/O	12 Bit	12 Bit	12 Bit	12 Bit
Timer (8 bit/24 bit)	1/2	1/2	0/2	1/2
Real Time Clock	yes (72421)	yes (72421)	yes (72421)	yes (72421)
Mass storage interface Floppy SCSI	 yes, with DMA yes, with DMA	 no no	 no no	 no no
Ethernet interface	optional, with 64 Kbyte Buffer	no	no	no
Multiprocessing support	FMB 8 mailboxes remote reset	FMB 8 mailboxes remote reset	no	FMB 8 Mailboxes Remote Reset
VMEbus arbiter	Single level	Single level	Single level	Four level
Secondary bus interface	no	VSB with DMA	VSB	FGA-002 I/O-Port with DMA

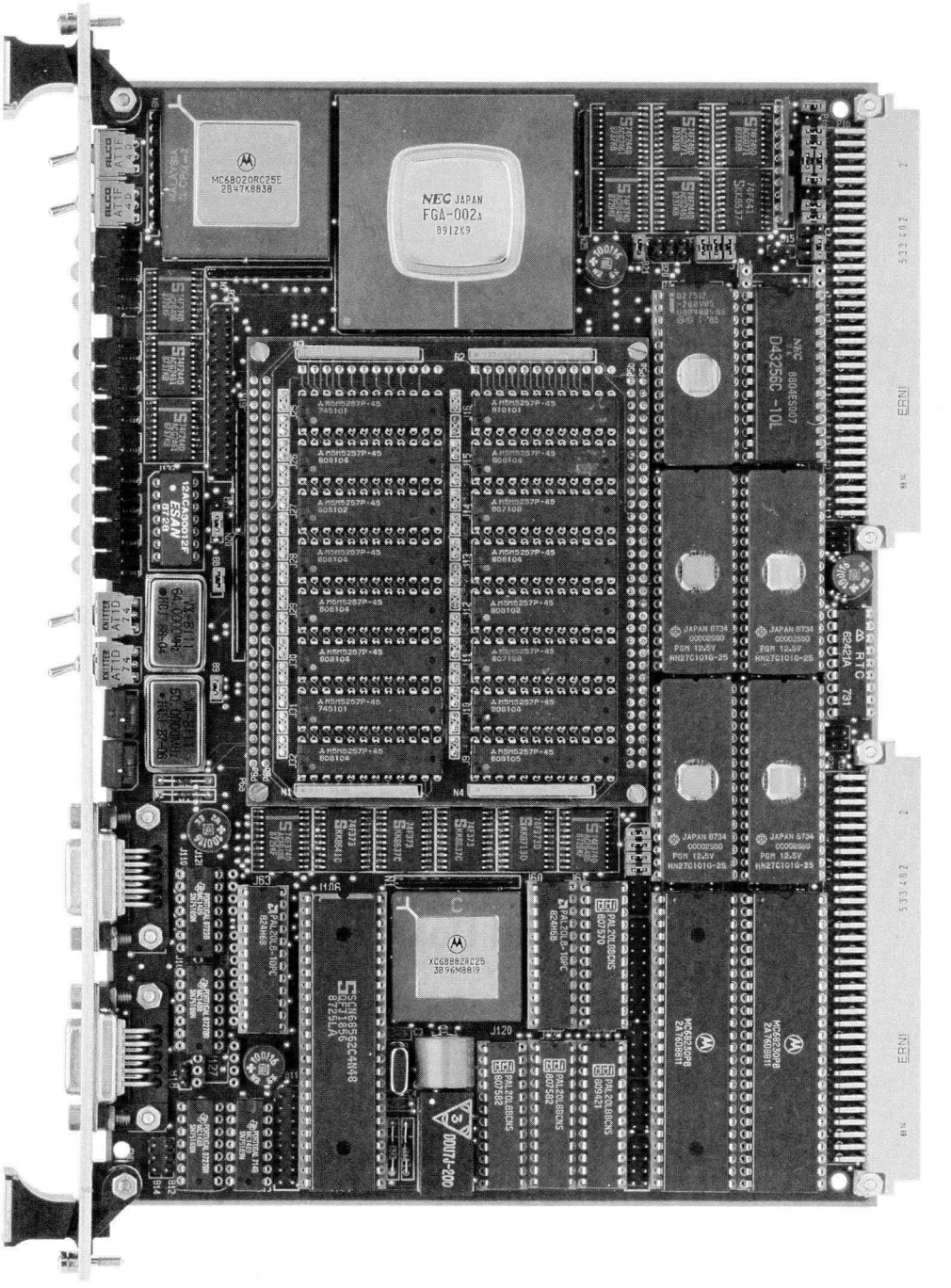
32-Bit CPU Boards (68040, 80386, 88000)

FAMILY	CPU-40	CPU-41	CPU-386	CPU-80	CPU-81
Processor type	68040	68040	80386	88100	88100
FPCP type	68040 (on-chip)	68040 (on-chip)	80387 (optional)	88100 (on-chip)	88100 (on-chip)
MMU type	68040 (on-chip)	68040 (on-chip)	80386 (on-chip)	2 × 88200	2 × 88200
Frequency min. max.	25.0 MHz 33.0 MHz	25.0 MHz 33.0 MHz	16.7 MHz 16.7 MHz	25.0 MHz 25.0 MHz	20.0 MHz 25.0 MHz
DMAC type Frequency max.	FGA-002 25.0 MHz	FGA-002 25.0 MHz	no no	no no	no no
Main memory type Capacity min. max. No. of wait states RAM function	DRAM (burst fill) 4 Mbyte 16 Mbyte 0/2 shared	SRAM 1 Mbyte 4 Mbyte 0 shared	DRAM 2 Mbyte 8 Mbyte 0 local	DRAM (burst fill) 4 Mbyte 16 Mbyte – shared	DRAM (burst fill) 4 Mbyte 16 Mbyte – shared
SRAM (on-board battery back-up)	32 Kbyte (default) 512 Kbyte (max.)	32 Kbyte (default) 512 Kbyte (max.)	no	2 Kbyte	2 Kbyte
No. of EPROM sockets Max. capacity Data bus width	2 2 Mbyte 32 Bit	2 2 Mbyte 32 Bit	4 256 Kbyte 32 Bit	4 4 Mbyte 32 Bit	4 4 Mbyte 32 Bit
Serial I/O (total) RS232/RS422/RS485 Controller chip	4 4 68562 (DUSCC)	4 4 68562 (DUSCC)	3 3 68901 (MFP/1), 68562 (DUSCC/2)	2 2 68562 (DUSCC)	2 2 68562 (DUSCC)
Parallel I/O	12 Bit (68230)	12 Bit (68230)	12 Bit (68230)	12 Bit (68230)	no
Timer (8 bit/24 bit)	1/2	1/2	3/2 (16 Bit)	2(16 Bit)/1	2(16 Bit)/1
Real Time Clock	yes (72423)	yes (72423)	yes (7170)	yes (48T02)	yes (48T02)
Mass storage interface Floppy SCSI	EAGLE-01 (optional) yes, with DMA yes, with DMA	EAGLE-01 (optional) yes, with DMA yes, with DMA	 no no	 no yes	 no no
Ethernet interface	EAGLE-01/-02 (optional) with 64 Kbyte buffer	EAGLE-01/-02 (optional) with 64 Kbyte buffer	no	no	no
Multiprocessing support	FMB 8 mailboxes remote reset	FMB 8 mailboxes remote reset	no	FMB	° FMB
VMEbus arbiter	Four level	Four level	Four level	Four level	Four level
Secondary bus interface	EAGLE-02 (optional) VSB with DMA	EAGLE-02 (optional) VSB with DMA	Local expansion interface	Dyadic bus interface	VSB and Dyadic bus interface



System 68000 VME
SYS68K/CPU-22

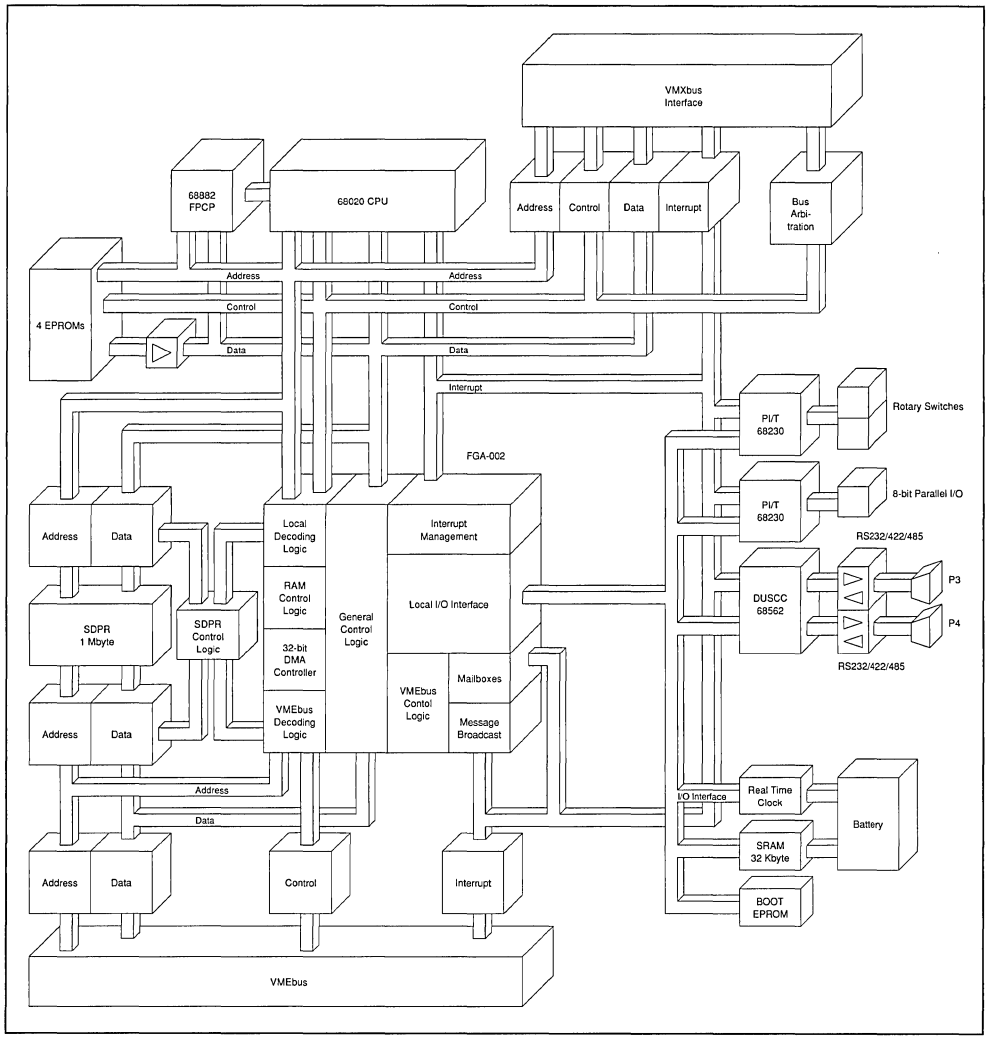
Multi-Processor 68020 CPU Board with DMA, Message Broadcast and Synchronized Dual Ported Memory


MC68020RC25E
2847KB838
NEC JAPAN
FGA-002A
8912K9
D43256C-10L
XC68B82RC25
3B96KB815
J120

General Description

The SYS68K/CPU-22 is a 68020/68882 based CPU board providing 1 Mbyte of Synchronized Dual Ported RAM (S-DPR). A full 32-bit DMA controller, supporting data transfers to/from VMEbus memory as well as to/from local RAM is provided by the 281-pin FORCE Gate Array.
Serial communication is provided through two fully independent multi-protocol channels. A full 32-bit VMXbus interface is installed on all CPU-22 board versions. The VMX interface is fully supported by the 32-bit DMA controller inside FGA-002. Additional features include up to 4 Mbyte EPROM capacity, up to 512 Kbyte SRAM and a Real Time Clock. VMEPROM, the Real Time Kernel, is installed by default. Two FORCE Message Broadcast channels and eight mailbox interrupts complete the board.

Block Diagram of the SYS68K/CPU-22



Features of the SYS68K/CPU-22

- 68020 CPU:
  16.7 MHz on CPU-22X
  20.0 MHz on CPU-22XA
- 68882 FPCP:
  16.7 MHz on CPU-22X
  20.0 MHz on CPU-22XA
- 32-bit high speed DMA controller for S-DPR/ VMEbus/VMX data transfers
- 1 Mbyte of constant zero wait state Synchronized Dual Ported RAM (S-DPR)
- FORCE Message Broadcast (FMB)
- 8 software-programmable multi-processor mailboxes
- Two serial I/O interfaces, RS232/RS422- and RS485-compatible
- 8-bit parallel interface with handshake
- Four system EPROM devices supporting 28- and 32-pin devices, using a 32-bit data path
  - 1 wait state access possible by using 100 nsec devices (CPU Clock 16.67 MHz)
- One boot EPROM for local booting and initialization of the I/O interface chips and the gate array
- Up to 512 Kbyte SRAM with battery back-up, using one 28/32-pin socket (JEDEC Standard)
- Real Time Clock with calendar and on-board battery back-up
- Two 24-bit timers with 5-bit prescaler
- One 8-bit timer
- All local I/O devices are able to interrupt the local CPU on a software-programmable level
- BERR handling fully under software control
- VMXbus Primary master interface with serial arbiter:
  - A32: D8, D16, D32
- Full 32-bit VMEbus master/slave interface supporting the following data transfer types:
  - A32, A24, A16 : D8, D16, D32 – Master
  - A32 : D8, D16, D32 – Slave
  - UAT, ADO and RMW cycles are also supported
- Single-level VMEbus arbiter
- SYSCLK driver
- VMEbus Interrupt Handler
- Support for ACFAIL* and SYSFAIL*
- Bus time-out counters for local and VMEbus accesses (15 µsec)
- VMEPROM, the Real Time Monitor with file manager and Real Time Kernel

1. Hardware Description

1.1 The 68020 CPU

The 68020 with its 32-bit address and data paths is installed on the SYS68K/CPU-22 board. The CPU includes a 256-byte instruction cache which significantly reduces the number of bus cycles needed for program fetches.
The 68020 CPU accesses the S-DPR constantly without the insertion of wait states.
Communication of the local I/O interfaces, local SRAM and the VMEbus interface to the 68020 CPU is provided through the specially designed 281-pin gate array, FGA-002.
The EPROM area, the Floating Point Co-Processor and the S-DPR are directly connected to the CPU data and address bus interface (as shown in the block diagram of the SYS68K/CPU-22).
The clock frequency of the 68020 CPU board is 16.7 MHz or 20.0 MHz.

1.2 The Floating Point Co-Processor

The SYS68K/CPU-22 is fitted with the enhanced 68882 Floating Point Co-Processor (FPCP). The clock frequencies of the CPU and the FPCP are identical. The FPCP conforms to the IEEE 754 Floating Point Standard. Intercommunication between the CPU and the FPCP is built in silicon. An internal register set inside the FPCP of eight general purpose registers (80 bit wide) yields fast execution times.

Features of the FPCP

- Eight general purpose registers (80-bit : 64-bit mantissa, 15-bit exponent and 1 sign bit)
- 67-bit on-chip ALU
- 67-bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 Standard
- Full support of trigonometric and logarithmic functions such as:
  - Sine, cosine, tangent and cotangent
  - Hyperbolic functions
  - Logarithmic functions (4)
  - Square root and exponential functions (4)
- The 68882 is fully software-compatible to the 68881 FPCP

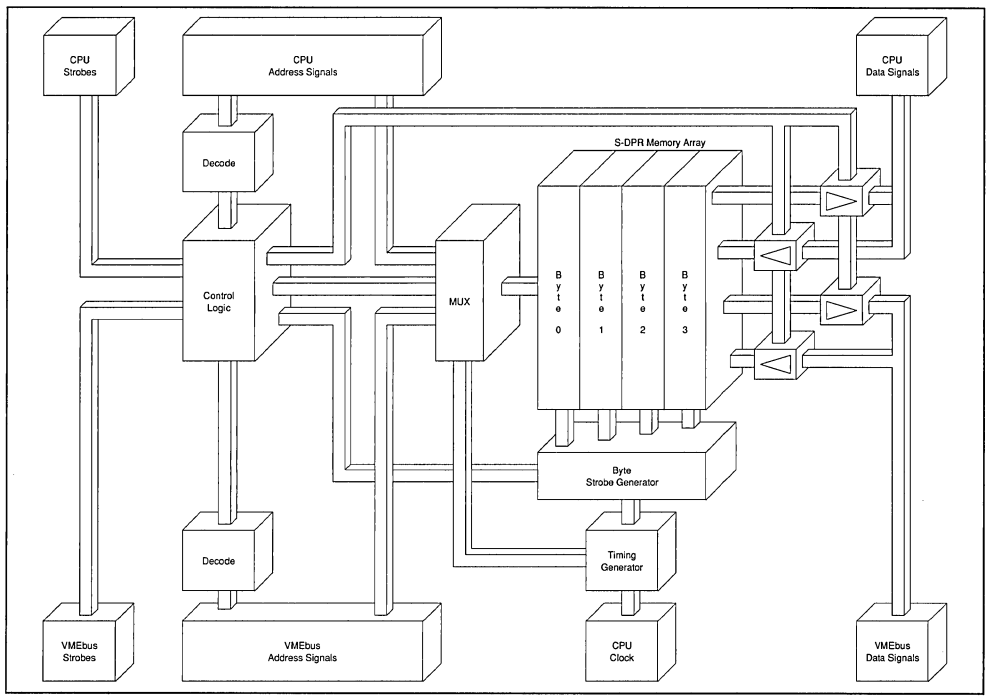
1.3 The Synchronized Dual Ported RAM

The SYS68K/CPU-22 contains a Synchronized Dual Ported static RAM design, S-DPR, which constantly supports zero wait state accesses of the local CPU. All accesses of the 68020 CPU to the S-DPR are immediately serviced while the VMEbus accesses the S-DPR between the 68020 access cycles.

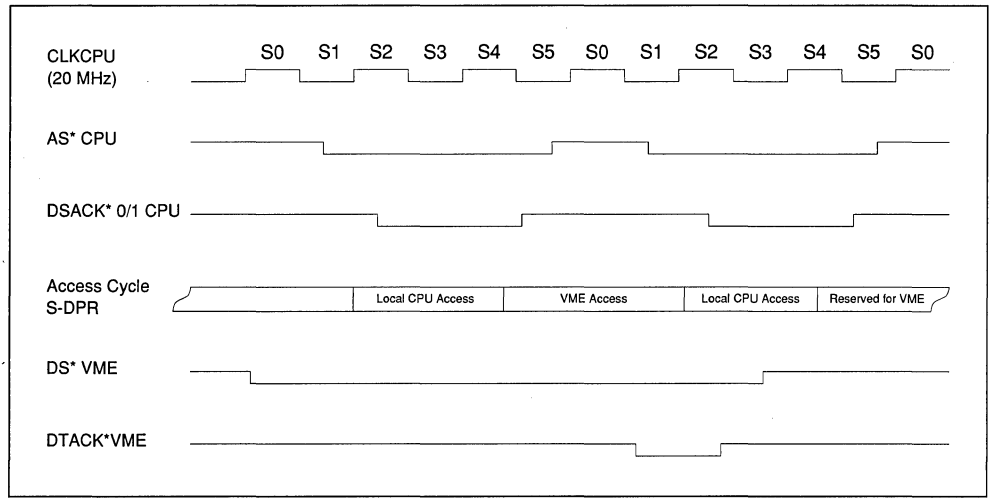
This technique allows the SYS68K/CPU-22 to guarantee a constant runtime of all programs regardless of whether an access to the S-DPR from another VMEbus board is made or not. The bandwidth of the S-DPR for the local CPU is 25 Mbyte/sec plus 15 Mbyte/sec for the VMEbus. This results in a total S-DPR bandwidth of 40 Mbyte/sec. A detailed block diagram of the S-DPR control mechanism and a global timing are outlined below.

A key advantage of the S-DPR technology is that the SYS68K/CPU-22 can be used in critical real time applications without losing the real time capabilities through external accesses to the S-DPR. Alternative technologies such as the dual gated mechanism (the CPU is halted during VMEbus accesses), or the dual buffered function (alternate accesses to the DPR while one requestor is waiting until the RAM is unused) cannot guarantee constant zero wait state operation. In non-S-DPR configurations the CPU normally waits or is halted during a VMEbus access cycle which results in a decreased CPU throughput. The SYS68K/CPU-22 combines the highest possible throughput (zero wait state accesses) with the Dual Ported RAM structure without decreasing performance at a CPU clock frequency of 16.7 or 20.0 MHz. The memory capacity is 1 Mbyte. The access address of the S-DPR from the VMEbus is fully software-programmable in 4 Kbyte increments through the installed gate array within the 4 Gbyte address range of the processor. Address and address modifier decoding for the VMEbus accesses are software-programmable through the gate array.

Block Diagram of the S-DPR



Timing Diagram of the S-DPR



1.4 The Local SRAM

A 32-Kbyte SRAM (battery back-up on-board) is installed on all SYS68K/CPU-22 board versions which supports data storage during power-down phases for up to one year.
The SRAM is directly connected to the FORCE Gate Array (FGA-002) I/O interface. Long word, word and byte transfers are automatically controlled via the gate array. Normal read/write operations to the SRAM are allowed, if the power is within the specification detected by a separate power sensor. The board is delivered with a 32 K x 8 SRAM. Higher density devices (e.g. future 512 K x 8 devices) or EEPROM devices may be inserted as the 32-pin socket allows the use of all JEDEC-compatible devices.

1.5 The System EPROMs

The SYS68K/CPU-22 contains four system EPROM sockets supporting four 28- and/or 32-pin EPROM devices.
Maximum data throughput to the 68020 CPU is provided through the fast decoding logic and separate data transceivers supporting one wait state operation, if 100 nsec devices are installed (CPU Clock 16.67 MHz).
The EPROM devices are read by the local 68020 CPU using 32-bit accesses which enables maximum performance.

Supported Device Types in the System EPROM Area:

Device Type	Pins	Organization	Total Memory Capacity
27512	28	64 K × 8	256 Kbyte
2710xx	32	128 K × 8	512 Kbyte
2720xx	32	256 K × 8	1 Mbyte
TBD	32	512 K × 8	2 Mbyte
TBD	32	1 M × 8	4 Mbyte

1.6 The Boot EPROM

The SYS68K/CPU-22 board contains, in addition to the four system EPROMs, a single boot EPROM to boot the local CPU, initialize all I/O devices and program the board dependent functions of the gate array FGA-002. All the presetting and initialization of the I/O devices are made using parameters programmed in the boot EPROM.

1.7 The DMA Controller

A high speed DMA controller is installed on the SYS68K/CPU-22. It features a maximum data transfer speed of up to 9.33 Mbyte/sec on the VMEbus and 18.8 Mbyte/sec to the S-DPR. DMA

execution on the VMEbus is performed without any degradation of performance for the local CPU. This allows a program to be run while loading new data into the shared RAM or writing processed data to global RAM or I/O controller boards. If the data has to be stored or read to/from the shared RAM, the DMA controller requests bus mastership from the local CPU.
To increase the data throughput, the DMA controller operates using a 32-byte FIFO for internal data storage. The read and write operations are executed in eight cycles, 4 byte at a time, which results in eight read cycles followed by eight write cycles.
This feature significantly increases data throughput and functionality because the local CPU maintains the real time capabilities by being interruptable during DMA transfers.
This technology allows data transfers between the shared RAM and the VMEbus by first collecting data from the VMEbus, giving up bus mastership and then transferring the data to the shared RAM. A second VMEbus board can transfer data on the VMEbus while the DMA controller transfers the stored data to the shared RAM.
The following table shows the 68020 performance during the DMA data transfers:

Area 1		Area 2	CPU Operation	Note
VMEbus	⇔	VMEbus	100 %	–
VMEbus	⇔	S-DPR	60–70 %	1
VMX	⇔	VMX	10 %	2
VMX	⇔	S-DPR	10 %	2
VMX	⇔	VMEbus	50–60 %	1/2
S-DPR	⇔	S-DPR	10 %	–

Note 1: CPU operation depends on the transfer speed of the addressed VMEbus board.
Note 2: CPU operation depends on the transfer speed of the addressed VSB board.

The CPU can operate in parallel to the DMA controller data transfers because of the 32-byte FIFO and the structure of the SYS68K/CPU-22. This means that during DMA transfers, the CPU can access all local I/O devices, the EPROM area as well as the shared RAM.

When the CPU wants to access the VMEbus, it has to wait until the DMA controller has completed the transfers from its FIFO (max. eight transfers).
Additionally, the DMA controller is connected to the VMX interface, allowing data transfer between the S-DPR and devices connected to VMX. The DMA controller supports aligned and unaligned data transfers. The internal control logic first aligns the data transfers to take full advantage of the 32-bit bus structure.

Register Set of the DMA Controller

8	Interrupt Control Normal Termination
8	Interrupt Control Error Termination
8	Source Attribute Register
8	Destination Attribute Register
8	General Control Register
8	Interrupt Status Normal Termination
8	Interrupt Status Error Termination
8	Run Control Register
8	Mode Status Register
32	Source Address
32	Destination Address
32	Transfer Count

1.8 The Local I/O Devices

The SYS68K/CPU-22 contains a gate array FGA-002 which provides an 8-bit local I/O interface used to interconnect the CPU and the I/O devices. The Real Time Clock, serial I/O controllers, the parallel I/O, control and status registers are connected to this local I/O interface.

1.9 The Serial I/O Interfaces

A Dual Universal Serial Communication Controller (DUSCC 68562) is installed on the CPU-22 to communicate to terminals, computers or other equipment.

Features of the DUSCC

- Dual full-duplex synchronous and asynchronous receiver and transmitter (programmable)
- Multi-protocol operation enabling support of bit- or character-oriented protocols. With additional software this allows the support of HDLC, SDLC, X.25, X.75, BISYNC, etc.
- Programmable data encoding formats: NRZ, NRZI, FM0, FM1, Manchester
- 4 character receiver/transmitter FIFOs
- Individual programmable baud rate for each receiver and transmitter supported by a digital phase locked loop
- Modem control signals for each channel: RTS, CTS, DCD

Serial I/O Signal Assignments

Pin	DUSCC Channels 1 + 2	
	RS232	RS422/485
1	DCD	TXD-
2	RXD	RTS-
3	TXD	CTS+
4	DTR	RXD+
5	GND	RXD-
6	DSR	TXD+
7	RTS	RTS+
8	CTS	CTS-
9	GND	RXD-

Both serial I/O channels are routed to 9-pin D-sub connectors on the front panel. Both serial I/O channels are connected to RS232-compatible drivers/receivers. They can also be configured for RS422/485-compatibility. The DUSCC can interrupt the local CPU on a software-programmable level (1 to 7). It is also possible to connect TxClk and RxClk to the 9-pin connectors via a jumper field. This is necessary for synchronous communication.

1.10 The Real Time Clock

A software-programmable Real Time Clock (RTC-72421) with on-board battery back-up is installed on the SYS68K/CPU-22 boards.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12 hr/24 hr clock switch-over
- Automatic leap year setting
- Interrupt masking
- CMOS design provides low power consumption during power-down mode

The Real Time Clock is able to interrupt the local CPU on a level programmable through the gate array (1 to 7).

1.11 The Input/Output Ports

A total of two 8-bit input ports and one 12-bit input/output port (8-bit data 4-bit handshake) are available on the SYS68K/CPU-22. The first 8-bit input port is connected to the two 4-bit HEX rotary switches provided on the front panel. These are available for user-dependent board and firmware configuration settings.
The second 8-bit input port allows the memory capacity of the shared memory to be read. Each SYS68K/CPU-22 board has three readable status bits describing the memory capacity. In addition, the CPU board type can be read via the remaining 5 bits. The 12-bit I/O port is routed to a 24-pin header which allows the connection of a flat cable. 8 bits are connected to the port A of a PI/T and can be used as inputs or outputs, the remaining 4 bits are connected to the handshake pins of the PI/T. This port can be used for parallel I/O applications such as a Centronics-compatible printer interface. The remaining signals of the two PI/T 68230 devices are used for on-board control as well as for four user LEDs on the front panel of the CPU-22.

1.12 The Timers

A total of three independent timers are available for the user. These timers offer maximum flexibility because each timer can be used to

force an interrupt to the CPU on a software-programmable IRQ-level (1 to 7).
The first two timers each provide a 24-bit timer with an individual 5-bit prescaler. The third timer can also be used to generate interrupts to the CPU and the SYSFAIL* signal to the VMEbus. It can also be used to act as a watchdog.
This timer is an 8-bit timer with programmable source clock divider installed in the gate array FGA-002. SYSFAIL* can be used in multi-processor systems to signal that one board has detected a failure.

The watchdog timer needs to be reset periodically (software-programmable). Without such a reset a SYSFAIL* will be asserted on the VMEbus. All installed timers can be used as a watchdog timer or can generate interrupts on a periodical basis.

1.13 Benchmarks

	CPU-22X	CPU-22XA	Unit
Dhrystones	4716	5952	Dhryst./sec
Whetstones	909	1111	KWhet./sec
Sieve	4.24	3.46	sec/100 iterations
DMA–Local	16.45	18.80	Mbyte/sec
DMA–VME	8.31	9.33	Mbyte/sec

2. The VMXbus Interface

The SYS68K/CPU-22 board is delivered with a full 32-bit VMXbus primary master interface. Maximum data throughput is provided on the VMXbus interface, supporting 32 bits of data via the 16 Mbyte address range. The following data transfer types are supported:
- A24 : D8, D16, D32
- Unaligned transfers
- Addres only cycles
- Read-Modify-Write transfers

3. The VMEbus Interface

The SYS68K/CPU-22 includes a full 32-bit VMEbus interface. The address modifier codes for A16, A24 and A32 addressing are fully supported in master mode. All slave accesses to the shared memory and to the two FMB channels have to be A32.
The gate array controls the access cycle to the S-DPR and determines if an access is to be allowed (read/write protection). Read-Modify-Write cycles are fully supported to allow multiple CPU boards to be synchronized via the shared RAM.
By default VMEPROM disables the support for on-board RMW cycles from the VMEbus to the on-board memory to reduce the overhead for accesses. The support for RMW cycles can easily be enabled by reprogramming the FGA-002.
These bus arbitration modes are supported:

REC	=	Release Every Cycle
RWD	=	Release When Done
ROR	=	Release On Request
RBCLR	=	Release On Bus Clear
RV	=	Release Voluntarily

Each of the listed modes is software-programmable inside the gate array. The bus request level of the SYS68K/CPU-22 is jumper-selectable (BR0–3*).
The SYS68K/CPU-22 contains a DMA controller, which is able to access the VMEbus interface independent from the CPU. A single level arbiter, a power monitor, SYSCLCK, a SYSRESET* generator and support for ACFAIL* and SYSFAIL* complete the VMEbus interface.

4. The Memory Map

The memory map of the SYS68K/CPU-22 is listed in the following table:

Start Address	End Address	Type
00000000	000FFFFF	S-DPR, 1 Mbyte
00100000	F9FFFFFF	VMEbus, A32 : D32, D16, D8
FA000000	FAFFFFFF	Message Broadcast Area
FB000000	FBFEFFFF	VMEbus, A24 : D32, D24, D16, D8
FBFF0000	FBFFFFFF	VMEbus, A16 : D32, D24, D16, D8
FC000000	FCFEFFFF	VMEbus, A24 : D16, D8
FCFF0000	FCFFFFFF	VMEbus, A16 : D16, D8
FD000000	FDFFFFFF	VMXbus, A24 : D32, D16, D8
FE000000	FEFFFFFF	VMXbus, A24 : D16, D8
FF000000	FF7FFFFF	Sytem EPROM
FF800000	FFBFFFFF	Local I/O
FFC00000	FFCFFFFF	Local SRAM
FFD00000	FFDFFFFF	Registers of FGA-002
FFE00000	FFEFFFFF	Boot EPROM
FFF00000	FFFFFFFF	Reserved

5. The Interrupt Structure

The gate array installed on the SYS68K/CPU-22 handles all local and VMEbus interrupts. Each interrupt request from the local bus through the DUSCC, RTC and the two timers, as well as the gate array specific interrupt requests, are combined with the seven VMEbus IRQs and the VMXbus IRQ.

Each IRQ source, including the VMEbus IRQs, can be programmed to interrupt the CPU on an individual programmable level (1 to 7). The gate array supplies the vector, or initiates an interrupt vector fetch from the I/O device or from the VMEbus. In addition to the local interrupts, the ACFAIL* and SYSFAIL* signals can be used to interrupt the CPU on a software-programmable level. This results in a total of 40 individual IRQs, handled through the gate array on the CPU-22 board. The interrupt vectors supplied by the gate array have a basic vector and fixed increments for each source. The basic vector is software-programmable.

6. The Multi-Processor Mailboxes

The SYS68K/CPU-22 includes eight multi-processor mailboxes. Every mailbox allows an interrupt to be forced to the local 68020 CPU. All interrupt levels are software-programmable and an individual interrupt vector for each level may be passed to the CPU. This function allows the triggering of an interrupt on the SYS68K/CPU-22 from multiple masters on the VMEbus. The mailboxes are accessed via RMW access, thus allowing multiple masters on the VMEbus to share the same mailbox channel.

7. FORCE Message Broadcast

The FORCE Message Broadcast (FMB) is a fast and effective mechanism to communicate with and to synchronize up to 20 CPU boards in a VMEbus system in only one VMEbus write cycle. It offers a unique support feature for building multi-processing systems based on the VMEbus. An FMB transfer is a standard VMEbus write cycle and complies fully to the IEEE 1014 Specification. Any VMEbus master may be a message transmitter. The transmitter decides which boards in the system should be addressed (one, two or up to twenty boards) and writes the message to a specific address.

All addressed boards receive the message at the same time and generate an interrupt request on a programmable level to their local microprocessor. This ensures that there is no time delay between the synchronization of different boards in the system. The ability to communicate with and synchronize multiple CPUs in the system by the FMB mechanism allows the VMEbus to be used in a wide range of application areas, particularly multi-processor environments.

Without the FMB mechanism, communication between and synchronisation of system boards has to be managed via the seven interrupt

request lines. FMB reduces the massive time overhead normally needed to process the interrupt cycles to just one write cycle.
All FORCE VME/PLUS boards provide two fully independent message broadcast channels. Channel 0 stores 8-bit messages in an eight stage deep FIFO, channel 1 stores one 8-bit message and can therefore be used for high priority messages.

8. Software

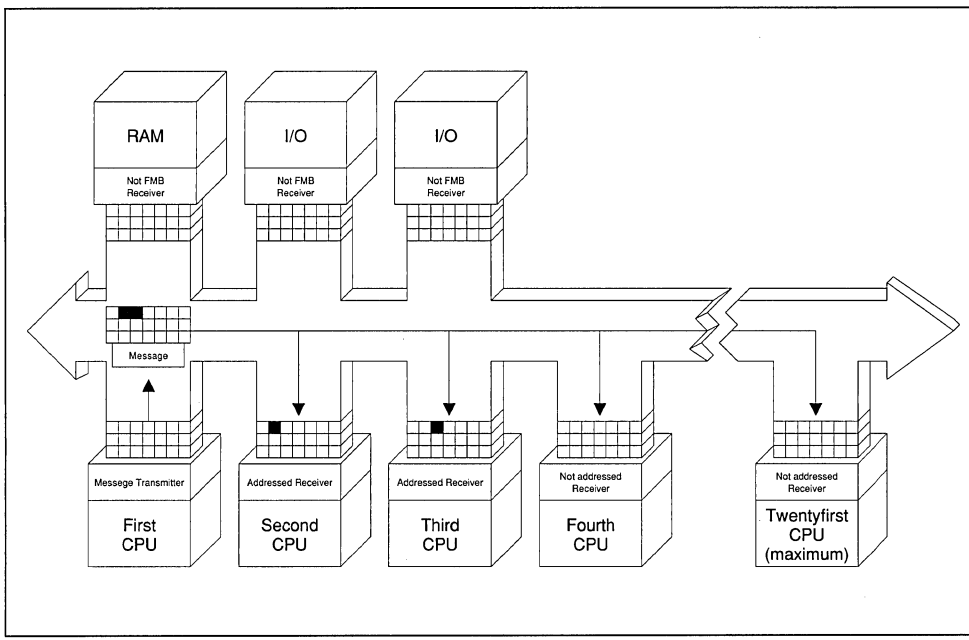
It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-22 Software Support

Operating System/Kernel	Vendor/Support
PDOS	Contact FORCE for availability
OS-9/9000	Contact FORCE for availability
VMEPROM	FORCE COMPUTERS
VxWORKS	Contact FORCE for availability
VRTX-32	Contact FORCE for availability
pSOS	Contact FORCE for availability
ARTX	Contact FORCE for availability
Telesoft ADA	Contact FORCE for availability

As a courtesy, FORCE provides the user with the ability to immediately start a real time application by including VMEPROM on every CPU card, free of charge and free of licensing costs.
VMEPROM is an EPROM-based Real Time Multi-tasking Kernel/Monitor. The complete package resides in 256 Kbyte of EPROM and uses 32 Kbyte of RAM. VMEPROM fully supports all of the on-board I/O devices.

Block Diagram of the FORCE Message Broadcast



VMEPROM is composed of a highly sophisticated Real Time Kernel, which is based on the PDOS Real Time Kernel. A file manager supporting sequential, random and shared files is also included.
The user interface contains more than 60 commands perfectly suited for program debugging, host computer communications, as well as task and file management. It includes a powerful debugger, supporting line assembler/disassembler for the microprocessor.

Features of VMEPROM

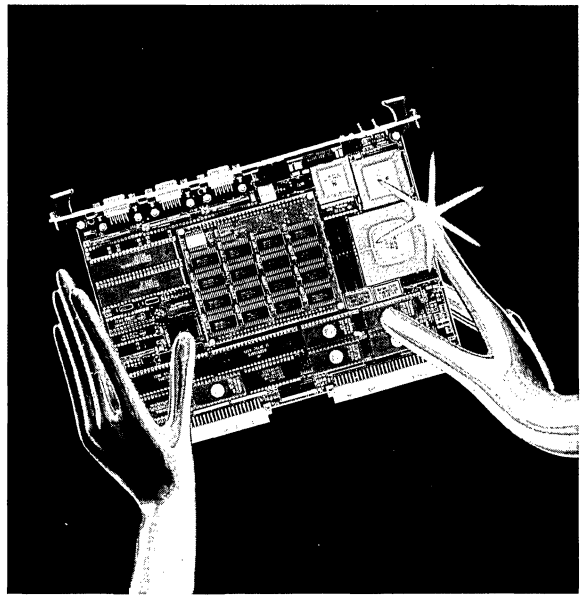
- Real Time Kernel supporting multi-tasking, up to 64 tasks
- File manager, supporting up to 64 open files at the same time
- Line assembler/disassembler with full support of all 680x0 instructions
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify
- S-record up/downloading from any port defined in the system
- Disk support for RAM disk, floppy and Winchester disks
- VMEPROM allows disk formatting and initialization
- Serial I/O support for up to two SIO-2 or ISIO-2 boards in the system; local serial I/O devices are also supported
- EPROM programming utility using the SYS68K/RR-2 board
- Full screen editor
- I/O re-direction to files or ports from the command line
- Over 100 system calls to the kernel

Specifications

Function	
CPU/FPCP	68020/68882
CPU and FPCP clock frequency on: CPU-22X CPU-22XA	16.7 MHz 20.0 MHz
Shared DRAM capacity	1 Mbyte
SRAM capacity with on-board battery back-up	32 Kbyte
No. of system EPROM sockets Data path	4 32-bit
Serial I/O interface (68562) RS232/422/485-compatible	2 2
Parallel I/O interface (68230)	12 lines
Real Time Clock with on-board battery back-up	72421
24-bit timer with 5-bit prescaler 8-bit timer	2 1
VMXbus Primary Master Interface A24, A16 : D8, D16, D32, UAT, RMW Interrupt Handler	yes yes IHP
VMEbus interface A32, A24, A16 : D8, D16, D32, UAT, RMW, ADO A32 : D8, D16, D32, UAT, RMW, ADO Shared memory access time from VMEbus (read/write)	Master Slave Typ: 330 nsec
SYSCLK driver Mailbox interrupts	yes 8
FORCE Message Broadcast FMB-FIFO 0 FMB-FIFO 1	8 byte 1 byte
VMEbus and local interrupt handler All sources can be routed to a software-programmable IRQ level Total number of IRQ sources	1 to 7 yes 40
RESET and ABORT switches	yes
VMEPROM firmware installed on all board versions	yes
Power requirements + 5 V min : max + 12 V min : max – 12 V min : max	5.3 A : 6.3 A 0.1 A : 0.2 A 0.1 A : 0.2 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)	0 to + 50 °C – 40 to + 85 °C 5 to 95 %
Board dimensions	234 × 160 mm : 9.2 × 6.3 in
No. of slots used	1

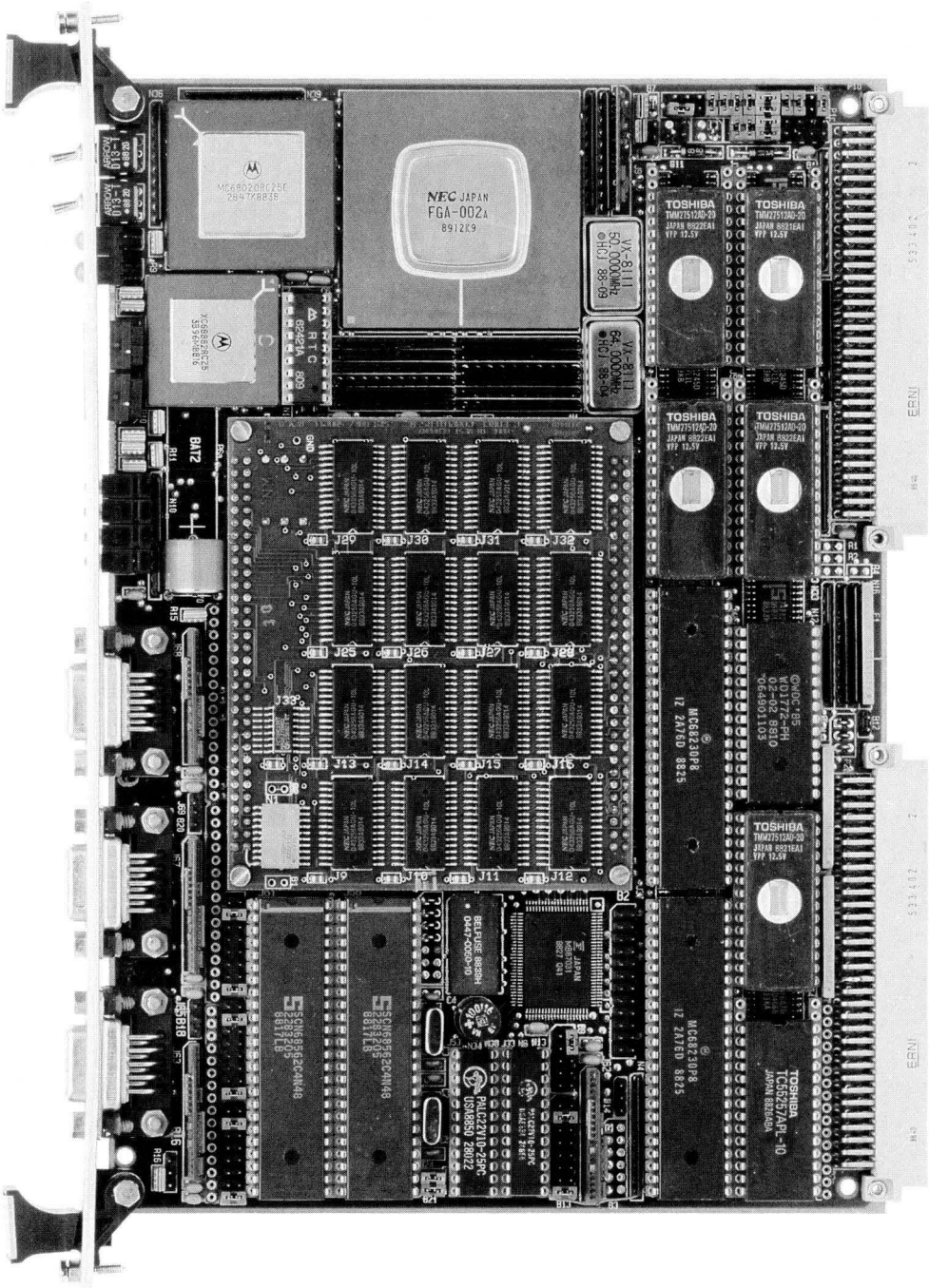
Ordering Information

SYS68K/CPU-22X Part No. 101106	16.7 MHz 68020 based CPU board with 68882 FPCP, DMAC, 1 Mbyte S-DPR capacity, VMXbus interface and VMEPROM. Documentation included.
SYS68K/CPU-22XA Part No. 101312	20.0 MHz 68020 based CPU board with 68882 FPCP, DMAC, 1 Mbyte S-DPR capacity, VMXbus interface and VMEPROM. Documentation included.
SYS68K/VMEPROM/22/UP Part No. 145106	VMEPROM update service for CPU-22 series.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM user's manual
SYS68K/CPU-22/UM Part No. 800136	User's manual for the SYS68K/CPU-22 products, including VMEPROM user's manual.



System 68000 VME
SYS68K/CPU-23

High Performance General Purpose 68020 CPU Board with Shared Memory, DMA and Mass Memory Control


NEC JAPAN
FGA-002A
8912K9
TOSHIBA
TMM27512AD-20
JAPAN 8922EA1
VFF 12.5Y
TOSHIBA
TMM27512AD-20
JAPAN 8921EA1
VFF 12.5Y
TOSHIBA
TMM27512AD-20
JAPAN 8922EA1
VFF 12.5Y
TOSHIBA
TMM27512AD-20
JAPAN 8922EA1
VFF 12.5Y
TOSHIBA
TMM27512AD-20
JAPAN 8921EA1
VFF 12.5Y
TOSHIBA
TC5565PJAFL-10
JAPAN 8822AGA
MC68230P8
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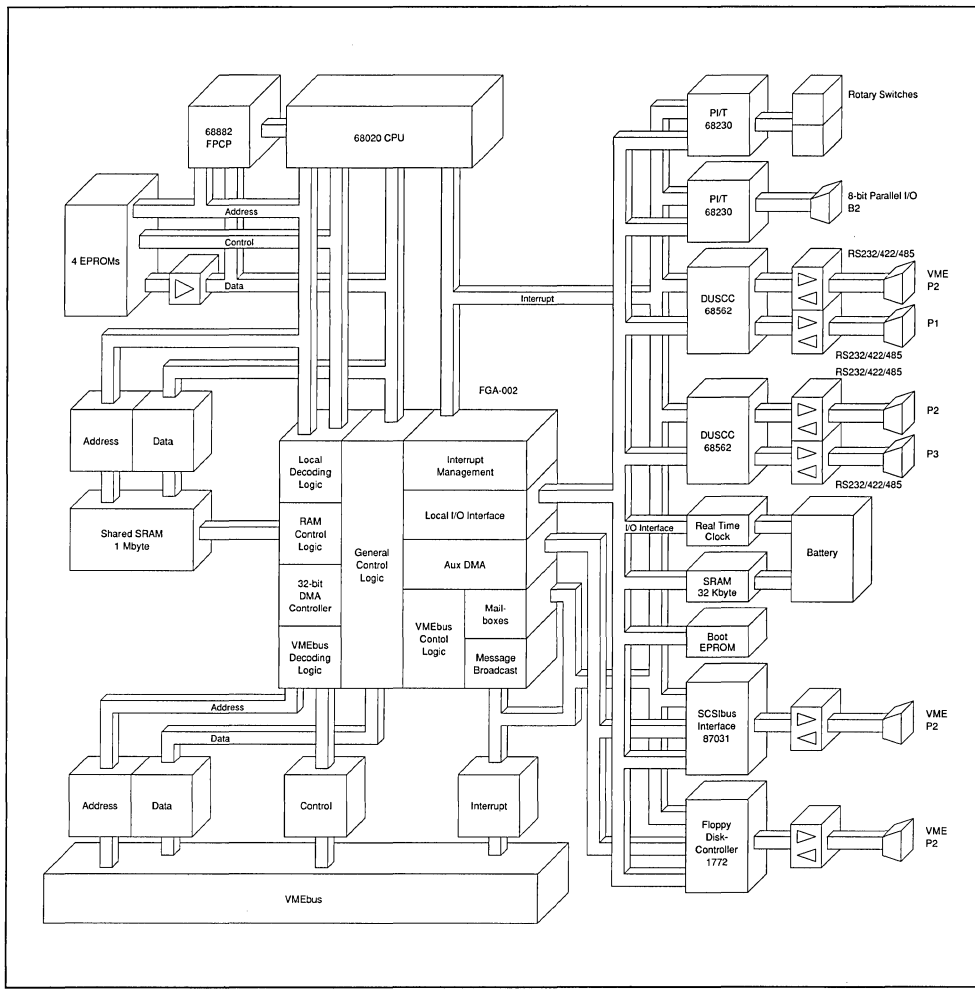
J12
BAT2
VX-8111
50.0000MHz
HCJ 88-09
VX-8111
64.0000MHz
HCJ 88-04
DALC22V10-25PC
USA8850 28022
BELFUSE 8883H
0447-0003-10

General Description

The SYS68K/CPU-23 is a 68020 based CPU board providing 1 Mbyte of shared memory.
A full 32-bit DMA controller supporting data transfers to/from VMEbus memory as well as to/from local RAM, is provided by the 281-pin FORCE Gate Array. Mass memory control is provided through the SCSI controller and the single chip floppy disk controller. Both are connected to the 32-bit DMA controller providing rapid data throughput to connected mass memory devices.
Serial communication is provided through four fully independent synchronous/asynchronous multi-protocol communication channels.
Additional features include four 32-pin EPROM sockets (32-bit wide), 32 Kbyte SRAM with battery back-up and a Real Time Clock.
The two independent 8-bit wide VMEbus FORCE Message Broadcast channels and eight multiprocessor mailboxes are also included. To complete the board, VMEPROM, the Real Time Kernel is installed.

Block Diagram of the SYS68K/CPU-23



Features of the SYS68K/CPU-23

- 68020 CPU:
  12.5 MHz on CPU-23XS
  25.0 MHz on CPU-23XB
- 68882 FPCP:
  12.5 MHz on CPU-23XS
  25.0 MHz on CPU-23XB
- 1 Mbyte of shared SRAM accessed from the local CPU without wait states (12.5 MHz)
- SRAM is accessible from the VMEbus via the gate array (FGA-002)
- 32-bit high speed DMA controller for data transfers to/from the shared RAM and/or to/from the VMEbus
  – 32 byte internal FIFO for burst DMA
- FORCE Message Broadcast (FMB)
- Four serial I/O interfaces, RS232/RS422/RS485-compatible
- 8-bit parallel interface with handshake
- Four system EPROM devices providing a 32-bit data path. 1 wait state access possible by using 100 nsec devices
- One boot EPROM for local booting and initialization of the I/O interface chips and the gate array
- 32 Kbyte of local SRAM with on-board battery back-up (8-bit data path)
- Real Time Clock with calendar and on-board battery back-up
- Two 24-bit timers with 5-bit prescaler
- One 8-bit timer
- Full 32-bit VMEbus interface
  – A32, A24, A16 : D8, D16, D32 – Master
  – A32 : D8, D16, D32 – Slave
- SCSI interface
- Floppy disk interface (SA460 compatible) for connection of 3", 3½" and 5¼" drives
- All local I/O devices are able to interrupt the local CPU on a software-programmable level
- 8 indicator LEDs which are under software control and free for user defined applications
- SYSCLK driver
- Single level VMEbus arbiter
- VMEbus Interrupt Handler (IH 1 to 7)
- Support for ACFAIL* and SYSFAIL* via software-programmable IRQ levels
- Bus time-out counters for local and VMEbus accesses (15 µsec)
- VMEPROM, the Real Time Monitor with file manager and Real Time Kernel

1. Hardware Description

1.1 The 68020 CPU

The 68020 with its 32-bit address and data paths is installed on the SYS68K/CPU-23 board. The CPU includes a 256-byte instruction cache which significantly reduces the number of bus cycles needed for program fetches.
The 68020 CPU accesses the shared memory constantly without the insertion of wait states (12.5 MHz).
Communication of the local I/O interfaces, local SRAM and the VMEbus interface to the 68020 CPU is provided through the specially designed 281-pin gate array, FGA-002.
The EPROM area, the Floating Point Co-Processor and the shared RAM are directly connected to the CPU data and address bus interface (as shown in the block diagram of the SYS68K/CPU-23). The clock frequency of the 68020 CPU board is 12.5 MHz or 25.0 MHz.

1.2 The Floating Point Co-Processor

The SYS68K/CPU-23 is fitted with the enhanced 68882 Floating Point Co-Processor (FPCP). The clock frequencies of the CPU and the FPCP are identical. The FPCP conforms to the IEEE 754 Floating Point Standard. Intercommunication between the CPU and the FPCP is built in silicon. An internal register set inside the FPCP of eight general purpose registers (80-bit wide) yields fast execution times.

Features of the FPCP

- 8 general purpose registers (80-bit : 64-bit mantissa, 15-bit exponent and 1 sign bit)
- 67-bit on-chip ALU
- 67-bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 Standard
- Full support of trigonometric and logarithmic functions such as:
  – Sine, cosine, tangent and cotangent
  – Hyperbolic functions
  – Logarithmic functions (4)
  – Square root and exponential functions (4)
- The 68882 is software-compatible to the 68881 FPCP

1.3 The Shared RAM

The SYS68K/CPU-23 contains an SRAM area with a capacity of 1 Mbyte. The local CPU and the DMA controller (installed in the FGA-002) can access the SRAM constantly without wait states (12.5 MHz). Data retention during power-down is provided via the 5VSTBY signal of the VMEbus. The SRAM is also accessible from the VMEbus through the installed FORCE Gate Array (FGA-002). The access address range and the address modifier codes are programmable by the local CPU.

The start and end access addresses are programmable in 4 Kbyte increments. The defined memory range can be write-protected in combination with the address modifier codes. For example, in supervisor mode, the memory can be read and written; in user mode, it can only be read. The read/write protection mechanism is fully under the user's software control. The SRAM is accessed from the VMEbus side by requesting local bus mastership from the local CPU via the FGA-002. After the CPU has granted local bus mastership to the FGA-002, the access cycle is executed and all data is latched on read cycles, while a normal write cycle is executed and terminated after storing data into the SRAM cells. The read and write cycles are terminated on the local bus side. The FGA-002 immediately releases bus mastership to the CPU while completing the fully asynchronous VMEbus access cycle. The early completion of the read and write cycle from the VMEbus side to the SRAMs is twice as fast as waiting for the completion of the VMEbus cycle. This allows the local CPU to run with a minimum of overhead.

1.4 The Local SRAM

32 Kbyte of SRAM is installed on all CPU-23 board versions and supports data storage during power-down phases for up to one year. The SRAM is directly connected to the FORCE Gate Array I/O interface. Long word, word and byte transfers are automatically controlled via the gate array.

Normal read and write operations to the single 32 K x 8 SRAM are allowed if the power is within the specification detected by a separate power sensor. Higher density devices (e.g. future 128 K x 8 devices) may be inserted as the 32-pin socket allows the use of all JEDEC-compatible devices.

1.5 The System EPROMs

The SYS68K/CPU-23 contains four system EPROM sockets supporting four 28- and/or 32-pin EPROM devices. Maximum data throughput to the 68020 CPU is provided through the fast decoding logic and separate data transceivers supporting one wait state operation, if 100 nsec devices are installed. The EPROM devices are accessed by the local 68020 CPU using 32-bit accesses which enables maximum performance when accessing the EPROM area.

Supported Device Types in the System EPROM Area:

Device Type	Pins	Organization	Total Memory Capacity
27512	28	64 K × 8	256 Kbyte
2710xx	32	128 K × 8	512 Kbyte
2720xx	32	256 K × 8	1 Mbyte
TBD	32	512 K × 8	2 Mbyte
TBD	32	1 M × 8	4 Mbyte

1.6 The Boot EPROM

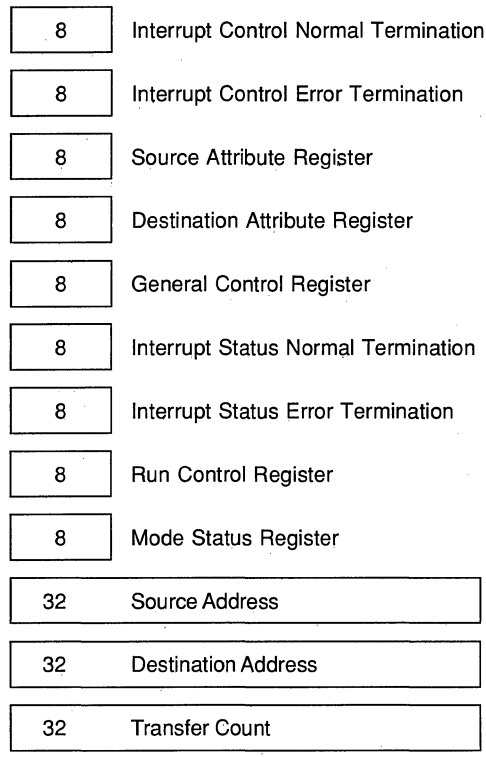
The SYS68K/CPU-23 board contains, in addition to the four system EPROMs, a single boot EPROM to boot the local CPU, initialize all I/O devices and program the board-dependent functions of the gate array, FGA-002. All the presetting and initialization of the I/O devices are made through the system EPROM to ease the adaptation of the complex board functions to the application needs.

1.7 The DMA Controller

A high speed DMA controller is installed in the FGA-002 on the SYS68K/CPU-23. It features a data transfer speed of up to 9 Mbyte/sec on the VMEbus and up to 18 Mbyte/sec to the shared RAM. The DMA controller allows the transfer of data between VMEbus memory (two different memory areas), or between VMEbus memory and the shared RAM. The DMA controller supports 32-bit data and address paths and fully

programmable address modifier codes for both source and destination.
DMA execution on the VMEbus is performed without any degradation of performance to the local CPU. This allows a program to be run while loading new data into the shared RAM or writing processed data to global RAM or I/O controller boards. Access to the shared RAM, by the DMA controller, is done by requesting bus mastership from the local CPU.
To increase the data throughput and maintain multi-processor functionality, the DMA controller operates in burst mode by using its 32-byte FIFO for internal data storage. The read and write operations are executed in eight cycles fetching 4 bytes at a time, which results in eight read cycles followed by eight write cycles. This feature maintains the real time capabilities by allowing interrupts during all DMA transfers. This technology allows data transfers between the shared RAM and the VMEbus by first collecting the data from the VMEbus, giving up bus mastership and then transferring the data to the shared RAM. A second VMEbus board can transfer data on the VMEbus while the DMA controller transfers the stored data to the shared RAM.
The CPU can operate in parallel to the DMA controller data transfers because of the 32-byte FIFO and structure of the SYS68K/CPU-23.
CPU operation means that the CPU can access all local I/O devices, the EPROM area as well as the shared RAM. When the CPU wants to access the VMEbus, it must wait until the DMA controller has finished its data transfers from its FIFO (max. eight data transfers).
Additionally, the DMA controller is connected to the on-board SCSI and floppy disk controller, allowing data transfer between mass memory devices and the shared RAM or the VMEbus memory.

Register Set of the DMA Controller



The following table shows the 68020 performance during DMA data transfer:

Area 1		Area 2	CPU Operation	Note
VMEbus	⇔	VMEbus	100 %	–
VMEbus	⇔	DPR	60–70 %	1
VMEbus	⇔	SCSI	100 %	–
VMEbus	⇔	FDC	100 %	–
DPR	⇔	SCSI	60–80 %	2
DPR	⇔	FDC	95 %	–

Note 1: CPU operation depends on the transfer speed of the addressed VMEbus board.
Note 2: CPU operation depends on the transfer speed of the SCSI device.

1.8 DMA Controller VMEbus Interface

The DMA controller supports aligned and unaligned data transfers. The internal control logic first aligns the data transfers to take full advantage of the 32-bit bus structure. The data transfer speed to the VMEbus depends on the access time of the addressed VMEbus module. By using DRAM boards the effective transfer speed reaches 6–8 Mbyte/sec. The maximum speed of 9.3 Mbyte/sec can be achieved, if high speed SRAM boards are used. The theoretical maximum transfer speed is 25 Mbyte/sec.

1.9 Benchmarks

	CPU-23XS	CPU-23XB	Unit
Dhrystones	3144	6250	Dhryst./sec
Whetstones	714	1428	KWhet./sec
Sieve	5.68	2.80	sec/100 iterations
DMA-Local	9.55	18.65	Mbyte/sec
DMA-VME	9.32	9.36	Mbyte/sec

1.10 The Local I/O Devices

The SYS68K/CPU-23 contains the gate array FGA-002 which interfaces the CPU to the I/O devices via an 8-bit local I/O bus. The Real Time Clock, serial I/O controllers, control and status registers, SCSI and the floppy disk controller interface to this local I/O bus.

1.11 The Real Time Clock

A software-programmable Real Time Clock (RTC-72421) with on-board battery back-up is installed on the SYS68K/CPU-23 boards.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12hr/24hr clock switch-over
- Automatic leap year setting
- Interrupt masking

The Real Time Clock is able to interrupt the local CPU on a software-programmable level (1 to 7).

1.12 The Parallel Interface

The CPU-23 contains a 12-bit parallel interface. This consists of 8 data bits and 4 control bits which may be configured for handshake signals. The parallel interface can easily be configured to support Centronics printers.

1.13 The Serial I/O Interfaces

Two Dual Universal Serial Communication Controllers (DUSCC 68562) are installed on the SYS68K/CPU-23 to communicate to terminals, computers or other equipment.

Features of the DUSCC

- Dual full-duplex synchronous/asynchronous receiver and transmitter (programmable)
- Multi-protocol operation enabling support of bit- or character-oriented protocols. With additional software, this allows the support of HDLC, SDLC, X.25, X.75, BISYNC, etc.
- Programmable data encoding formats: NRZ, NRZI, FM0, FM1, Manchester
- Four character receiver/transmitter FIFOs
- Individual programmable baud rate for each receiver and transmitter supported by a digital phase locked loop
- Modem control signals for each channel: RTS, CTS, DCD

The I/O Signal Assignments

Pin	RS232	RS422/485
1	DCD	TXD–
2	RXD	RTS–
3	TXD	CTS+
4	DTR	RXD+
5	GND	RXD–
6	DSR	TXD+
7	RTS	RTS+
8	CTS	CTS–
9	GND	RXD–

It is also possible to connect TxC and RxC to the 9-pin connectors via a jumper field. This is necessary for synchronous communication. The signals of DUSCC1, channel 1 are available on

the P2 connector. DUSCC1, channel 2 is configured to enable the connection of a terminal via the RS232 interface. All four channels can be configured to be RS232-or RS422/RS485-compatible. Resistive components can be installed to adapt to various cable lengths and reduce reflections for the RS422/RS485 interface. The two DUSCCs are able to interrupt the local CPU on a software-programmable IRQ-level (1 to 7) by supplying their own software-programmable IRQ vectors.

1.14 The Input/Output Ports

A total of three 8-bit I/O ports are available on the SYS68K/CPU-23. These ports are built using two 68230 PI/T devices. The remaining signals of the PI/T devices are used for various on-board control functions such as the signals for the FDC or the software readable board type and memory size. The first 8-bit port is an input port to read the two 4-bit Hex rotary switches provided on the front panel. The second port is an output which is used to control the eight LEDs on the front panel of the SYS68K/ CPU-23. The last port is an 8-bit I/O port with four handshake signals. These signals are routed to a 24-pin header which allows the connection of a flat cable. This port can be used for parallel I/O applications such as a Centronics compatible printer interface.

1.15 The Timers

A total of three independent timers are available for the user. These timers can be used to trigger an interrupt to the CPU on a software-programmable IRQ-level (1 to 7).
The first two timers provided by the PI/Ts (68230) are 24-bit timers with individual 5-bit prescalers, the third timer (FGA-002) is 8-bit wide. This timer can be used to generate the SYSFAIL* signal to the VMEbus. SYSFAIL* can be used in multiprocessor systems to signal that one board has detected a failure. All timers can be used as a watchdog or can generate interrupts on a periodical basis.

1.16 The SCSI Interface

The MB87031 SCSI controller is installed on the SYS68K/CPU-23 to interface directly to SCSI Winchester disks, optical disk drives or tape streamers.

Features of the 87031 SCSI Controller

- Full support for SCSI control
- Service of either initiator or target device
- 8-byte data buffer register incorporated
- Transfer byte counter (24-bit)
- Independent control and data transfer bus

The SCSI controller with its 8-bit DMA channel is directly connected to the installed DMA controller (inside the FGA-002).
This DMA controller includes a 32-byte FIFO which is able to wait until the 32-bytes are filled and then request local bus mastership to transfer the data in only eight cycles (32-bit for each cycle).
In addition to the 32-byte DMA FIFO, the DMA channel includes a second FIFO (8-byte deep) which is filled by the DMA controller when the main 32-byte DMA FIFO is transferring data to the destination address. This allows the transfer of data on the local DMA bus continuously.
This technique permits the CPU to perform all real time functions because the ratio between CPU and DMA operation at the maximum SCSI data transfer rate is 63 % for the CPU, 30 % for the DMA controller and 7 % for the local bus arbitration overhead (BR*, BG*, BGACK* handshake).
The VMEbus P2 I/O signal assignment of the single-ended SCSI interface is fully compatible to the assignment of the SYS68K/ISCSI-1 board.
The SCSI controller on the SYS68K/CPU-23 is fully supported from the installed Real Time Kernel/ Monitor VMEPROM.

1.17 The Floppy Disk Interface

The SYS68K/CPU-23 contains a single chip floppy controller, the WD1772. The installed driver/ receiver circuits allow direct connection of 3", 3½" and 5¼" floppy drives.
All I/O signals are available on the user-defined pins of the P2 connector. The I/O signal assignment is compatible to the SYS68K/IOBP-1.

Features of the WD1772 Controller

- Built-in data separator
- Built-in write precompensation
- 128, 256, 512 or 1024 byte sector lengths
- 5¼ single and double density
- Programmable stepping rate (1 to 6 msec)

The WD1772 controller is connected via an 8-bit DMA bus to the DMA controller. The DMA interface between the floppy disk controller and the DMA controller in the FGA-002 uses the same 32-byte FIFO as the SCSI interface. This enables the DMA interface to transfer data fully asynchronous to the operation of the CPU.
The floppy disk controller is fully supported by the on-board Real Time Kernel/Monitor VMEPROM.

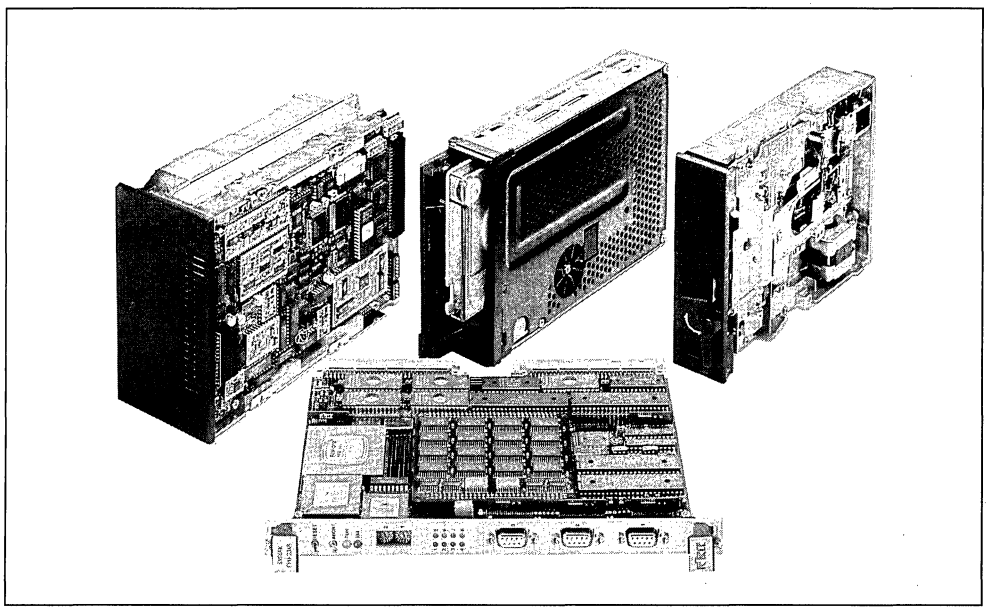
2. The VMEbus Interface
The SYS68K/CPU-23 includes a full 32-bit VMEbus interface, thereby taking full advantage of the VMEbus specification.
The address modifier codes for A16, A24 and A32 addressing are fully supported in master mode.
In slave mode, the FGA-002 decodes the AMcodes and the address signals of the VMEbus and signals the on-board control logic, if the board is addressed correctly and if the access is to be granted (read/write protection).
The gate array forces the access cycle to the shared RAM and controls the data flow (8-, 16-, 24- or 32-bit of data) automatically.

The termination of the VMEbus cycle is performed independently by the FGA-002, which allows the CPU to continue normal operation.

Supported Data Transfer Modes
The following data transfer types are supported in master and slave mode:

Transfer Type	D31-24	D23-16	D15-8	D7-0
Byte				x
			x	
Word			x	x
Long Word	x	x	x	x
Unaligned Transfers	x	x	x	
		x	x	
		x	x	x
Read Modify Write				x
			x	x
	x	x	x	x

Picture of the SYS68K/CPU-23 with Mass Memory Devices



The Read-Modify-Write cycles are fully supported to synchronize multiple CPU boards via the shared RAM.
The access times to access the shared RAM from the VMEbus are listed in the following table:

Access Times	Min	Typ	Max
Read	600 nsec	800 nsec	1650 nsec
Write	600 nsec	800 nsec	1650 nsec

The SYS68K/CPU-23 includes the following bus arbitration modes:

RWD = Release When Done
ROR = Release On Request
RBCLR = Release On Bus Clear
RAT = Release After Timeout

In addition, a fair arbitration mechanism is implemented to allow access to the VMEbus by all masters in a heavily loaded system (Request on No Request-RNR). Each of the listed modes is software-programmable inside the gate array. The bus request level of the SYS68K/CPU-23 is jumper-selectable (BR0–3*). A single level arbiter, a power monitor, a SYSESET generator and support for ACFAIL* and SYSFAIL* complete the VMEbus interface.

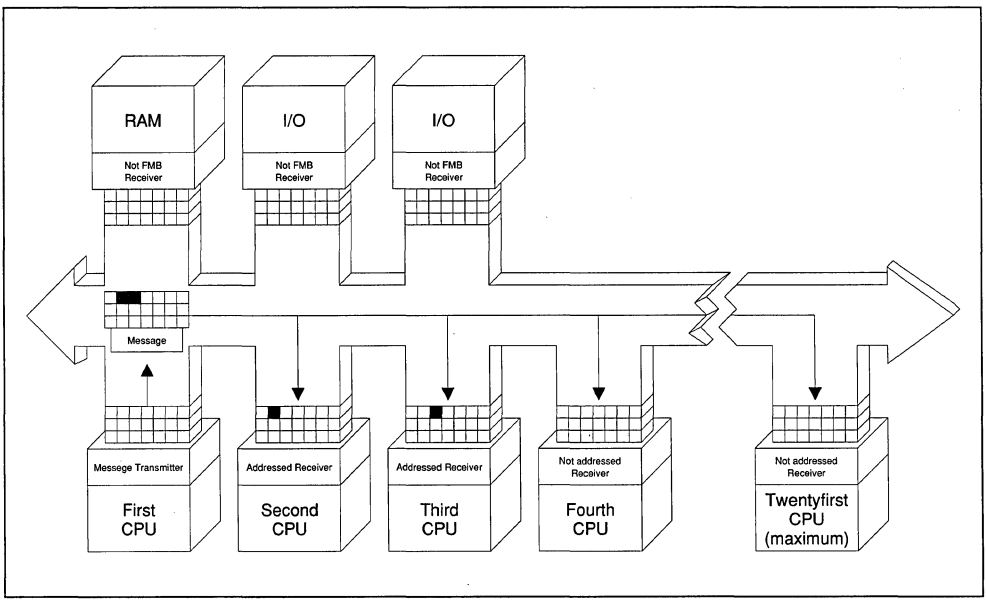
3. The Multi-Processor Mailboxes

The SYS68K/CPU-23 includes eight multiprocessor mailboxes. Each of these allows an interrupt to be forced to the local 68020 CPU. The interrupt level of each mailbox is software-programmable and an individual interrupt vector for each is supplied to the CPU.
This function allows the triggering of an interrupt on the SYS68K/CPU-23 from multiple masters on the VMEbus. The mailboxes are accessed using a RMW cycle, therefore allowing multiple masters on the VMEbus to share the same mailbox channel.

4. FORCE Message Broadcast

The FORCE Message Broadcast (FMB) is a fast and effective mechanism to communicate with and synchronize up to 20 CPU boards in a VMEbus system in only one VMEbus write cycle. It offers a unique support feature for building multi-processing systems based on the VMEbus.

Block Diagram of the FORCE Message Broadcast



An FMB transfer is a standard VMEbus write cycle and complies fully to the IEEE 1014 Specification. Any VMEbus master may be a message transmitter. The transmitter decides which boards in the system should be addressed (one, two or up to twenty boards) and writes the message to a specific address.
All addressed boards receive the message at the same time and generate an interrupt request on a programmable level to their local microprocessor. This ensures that there is no time delay between the synchronization of different boards in the system. The ability to communicate with and synchronize multiple CPUs in the system by the FMB mechanism allows the VMEbus to be used in a wide range of application areas, particularly multi-processor environments.
Without the FMB mechanism, communication between and synchronisation of system boards has to be managed via the seven interrupt request lines. FMB reduces the massive time overhead normally needed to process the interrupt cycles to just one write cycle.
All FORCE VME/PLUS boards provide two fully independent message broadcast channels. Channel 0 stores 8-bit messages in an eight stage deep FIFO, channel 1 stores one 8-bit message and can therefore be used for high priority messages.

5. The Interrupt Structure

The gate array installed on the SYS68K/CPU-23 handles all local and VMEbus interrupts. Each interrupt request via the local bus from any of the on-board devices, i.e. SCSI and floppy disk controller, the DUSCC, RTC and the two timers, as well as the gate array specific interrupt requests are combined with the seven VMEbus interrupt requests. Each IRQ source, including the VMEbus IRQs, can be programmed to interrupt the CPU on an individual programmable level (1 to 7).
The gate array supports the vector or initiates an interrupt vector fetch from the I/O device or from the VMEbus.
In addition to the local interrupts, the ACFAIL* and SYSFAIL* signals can be used to interrupt the CPU on a software-programmable level. This results in a total of 42 individual IRQs handled through the gate array on the SYS68K/CPU-23 board. The interrupt vectors supplied by this gate array have a basic vector and fixed increments for each source. The basic vector is software-programmable.

6. The Memory Map

The memory map of the SYS68K/CPU-23 is listed in the following table:

Start Address	End Address	Type
00000000	000FFFFF	Shared Memory 1 Mbyte
00100000	F9FFFFFF	VMEbus, A32 : D32, D24, D16, D8
FA000000	FAFFFFFF	Message Broadcast Area
FB000000	FBFEFFFF	VMEbus, A24 : D32, D24, D16, D8
FBFF0000	FBFFFFFF	VMEbus, A16 : D32, D24, D16, D8
FC000000	FCFEFFFF	VMEbus, A24 : D16, D8
FCFF0000	FCFFFFFF	VMEbus, A16 : D16, D8
FD000000	FEFFFFFF	Reserved
FF000000	FF7FFFFF	System EPROM
FF800000	FFBFFFFF	Local I/O
FFC00000	FFCFFFFF	Local SRAM
FFD00000	FFDFFFFF	Registers of FGA-002
FFE00000	FFEFFFFF	Boot EPROM
FFF00000	FFFFFFFF	Reserved

7. Software

It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest

level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-23 Software Support

Operating System/Kernel	Vendor/Support
PDOS	FORCE COMPUTERS
OS-9/9000	Contact FORCE for availability
VMEPROM	FORCE COMPUTERS
VxWORKS	Contact FORCE for availability
VRTX-32	READY SYSTEMS
pSOS	Contact FORCE for availability
ARTX	Contact FORCE for availability
Telesoft ADA	Contact FORCE for availability

As a courtesy, FORCE provides the user with the ability to immediately start a real time application by including VMEPROM on every CPU card, free of charge and free of licensing costs.
VMEPROM is an EPROM-based Real Time Multi-tasking Kernel/Monitor. The complete package resides in 256 Kbyte of EPROM and uses 32 Kbyte of RAM. VMEPROM fully supports all of the on-board I/O devices.
VMEPROM is composed of a highly sophisticated Real Time Kernel, which is based on the PDOS Real Time Kernel. A file manager supporting sequential, random and shared files is also included.
The user interface contains more than 60 commands perfectly suited for program debugging, host computer communications, as well as task and file management. It includes a powerful debugger, supporting line assembler/disassembler for the microprocessor.

Features of VMEPROM

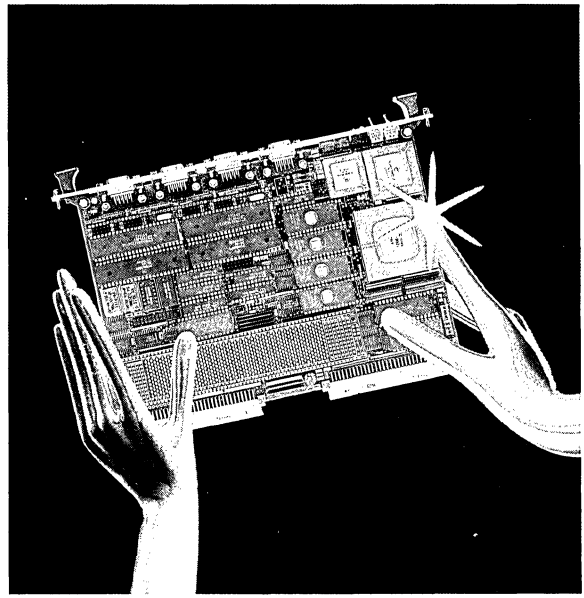
- Real Time Kernel supporting multi-tasking, up to 64 tasks
- File manager, supporting up to 64 open files at the same time
- Line assembler/disassembler with full support of all 680x0 instructions
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify
- S-record up/downloading from any port defined in the system
- Disk support for RAM disk, floppy and Winchester disks
- VMEPROM allows disk formatting and initialization
- Serial I/O support for up to two SIO-2 or ISIO-2 boards in the system; local serial I/O devices are also supported
- EPROM programming utility using the SYS68K/RR-2 board
- Full screen editor
- I/O re-direction to files or ports from the command line
- Over 100 system calls to the kernel

Specifications

Function		
68020 CPU clock frequency on:	CPU-23XS CPU-23XB	12.5 MHz 25.0 MHz
68882 FPCP clock frequency on:	CPU-23XS CPU-23XB	12.5 MHz 25.0 MHz
Shared RAM capacity Local SRAM capacity with on-board battery back-up		1 Mbyte 32 Kbyte
No. of EPROM sockets (32-bit data path)		4
Serial I/O interface (total) Used controller RS232- or RS422/RS485-compatible		4 2 × 68562 4
Parallel I/O interface (68230)		12 lines
Real Time Clock with on-board battery back-up		72421
SCSI controller chip SCSI interface		87031 Single-ended
Floppy Disk Controller Interface		1772 SA 460
VMEbus interface Master: A32, A24, A16 : D8, D16, D32, UAT, RMW Slave: A32 : D8, D16, D32, UAT, RMW Software-programmable access address and address modifier code Shared RAM read/write access time (min : typ : max)		 yes yes yes 600 : 800 : 1600 nsec
FORCE Message Broadcast channels		2
24-bit timer with 5-bit prescaler 8-bit timer		2 1
VMEbus interrupt handler Local interrupt handler		IH 1 to 7 IH 1 to 7
VMEPROM firmware installed on all board versions		yes
Power requirements	+ 5 V min : max + 12 V min : max – 12 V min : max	4.2 A : 5.9 A 0.1 A : 0.2 A 0.1 A : 0.2 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)		0 to + 50 °C – 40 to + 85 °C 5 to 95 %
Board dimensions		234 × 160 mm : 9.2 × 6.3 in
No. of slots used		1

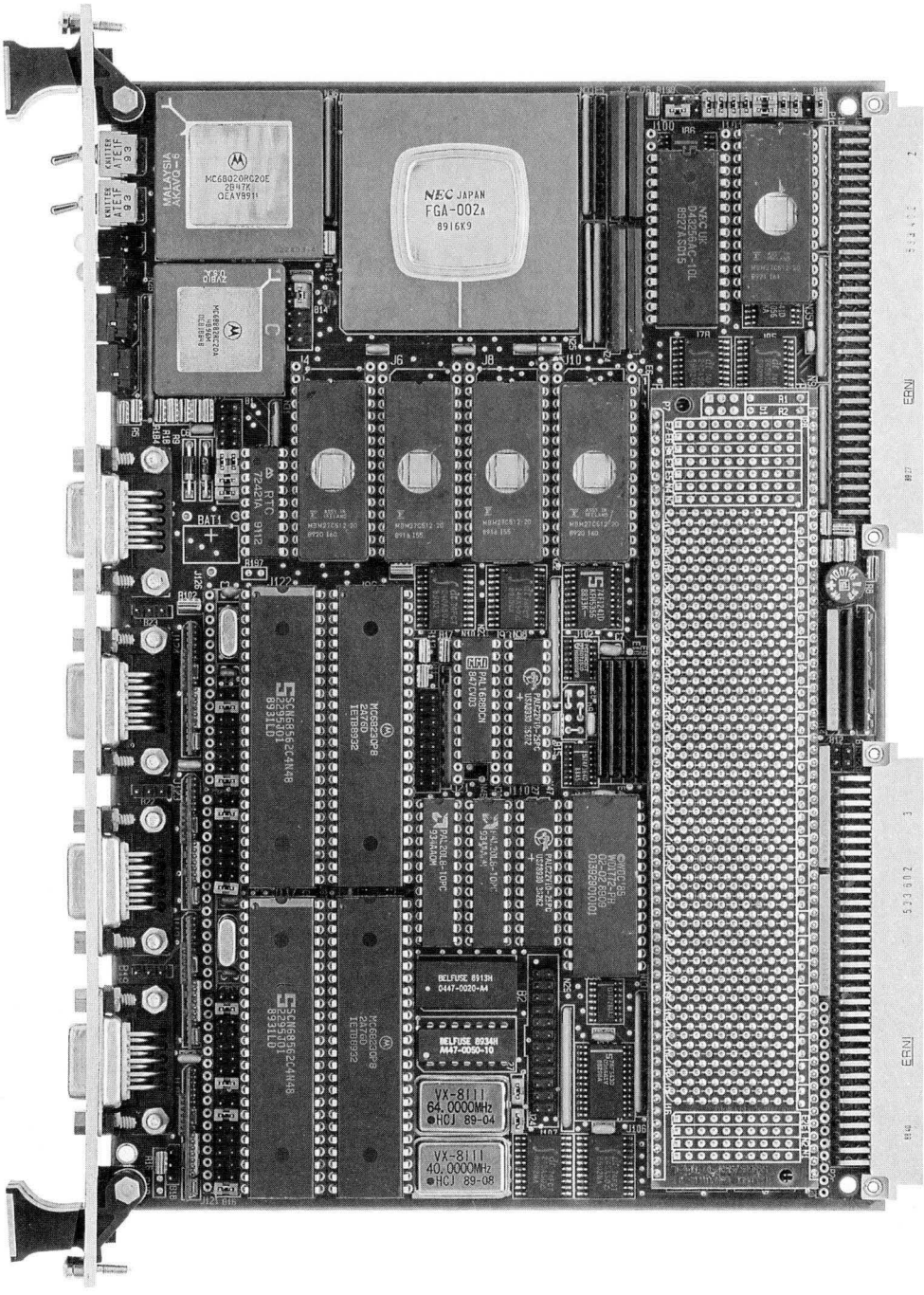
Ordering Information

SYS68K/CPU-23XS Part No. 101120	12.5 MHz 68020 based CPU board with 68882 FPCP, DMA, 1 Mbyte shared RAM, four serial I/O, SCSI, FDC, VMEPROM. Documentation included.
SYS68K/CPU-23XB Part No. 101122	25.0 MHz 68020 based CPU board with 68882 FPCP, DMA, 1 Mbyte shared RAM, four serial I/O, SCSI, FDC, VMEPROM. Documentation included.
SYS68K/IOBP-1 Part No. 300021	Back panel for the CPU-23 boards providing connectors for SCSI, floppy disk and one serial channel.
SYS68K/VMEPROM/23/UP Part No. 145111	VMEPROM update service for the CPU-23 series.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM user's manual, excluding the SYS68K/CPU-23 description.
SYS68K/CPU-23/UM Part No. 800142	User's manual for the SYS68K/CPU-23 including VMEPROM and FGA-002 user's manual.



System 68000 VME
SYS68K/CPU-26

High Performance General Purpose 68020 CPU Board with Shared Memory, DMA and Mass Memory Control


NEC JAPAN
FGA-002A
8916K9
MALAYSIA
MC68020RC20E
MC68881RC20A
BAT1
VX-8111
64.0000MHz
HCJ 89-04
VX-8111
40.0000MHz
HCJ 89-08
BELFUSE 8913H
0447-0020-A4
BELFUSE 8934H
A447-0050-10

General Description

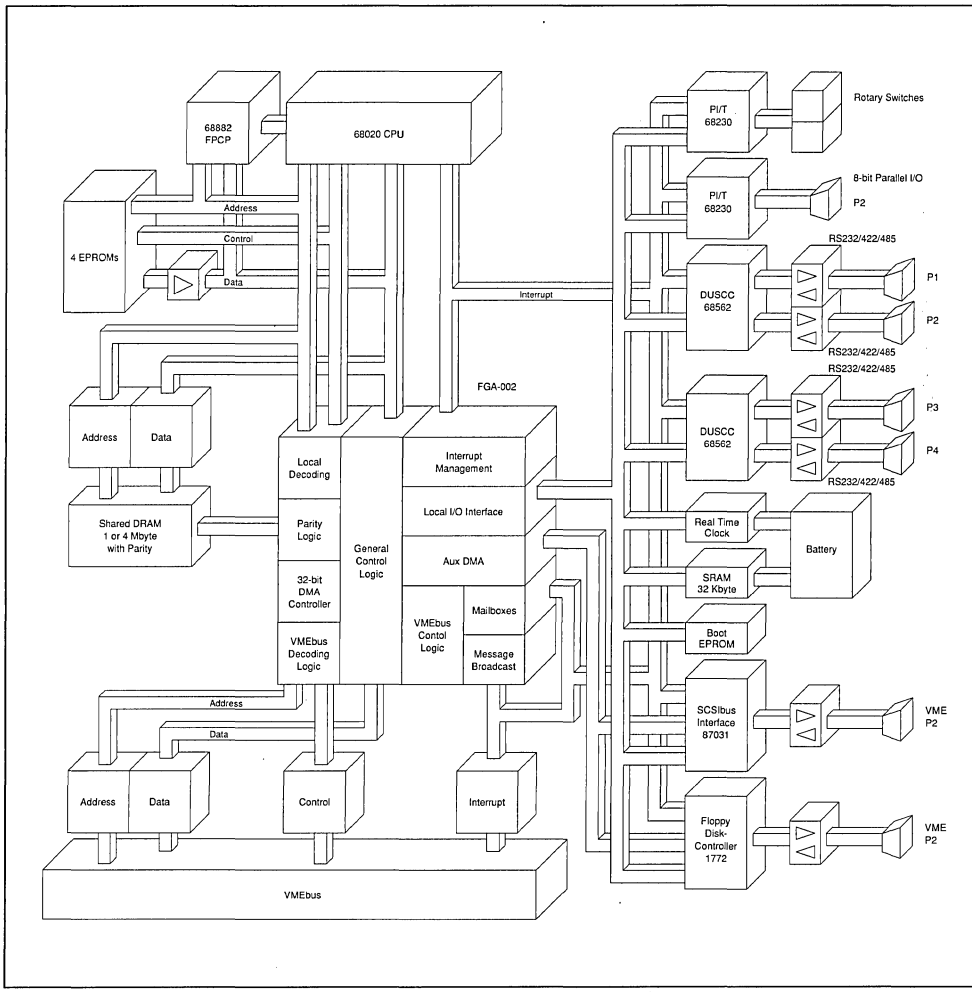
The SYS68K/CPU-26 is a 68020 based CPU board providing 1 or 4 Mbyte of shared memory. A full 32-bit DMA controller supporting data transfers to/from VMEbus memory as well as to/from local RAM, is provided by the 281-pin FORCE Gate Array. Mass memory control is provided through the SCSI controller and the single chip floppy disk controller. Both are connected to the 32-bit DMA controller providing rapid data throughput to connected mass memory devices.

Serial communication is provided through four fully independent synchronous/asynchronous multi-protocol communication channels.

Additional features include four 32-pin EPROM sockets (32-bit wide), 32 Kbyte SRAM with battery back-up and a Real Time Clock.

The two independent 8-bit wide VMEbus FORCE Message Broadcast channels and eight multi-processor mailboxes are also included. To complete the board, VMEPROM, the Real Time Kernel is installed.

Block Diagram of the SYS68K/CPU-26



Features of the SYS68K/CPU-26

- 68020 CPU:
  12.5 MHz on CPU-26XS
  20.0 MHz on CPU-26XA, CPU-26ZA
- 68882 FPCP:
  12.5 MHz on CPU-26XS
  20.0 MHz on CPU-26XA, CPU-26ZA
- 1 or 4 Mbyte of shared DRAM including byte parity generation and check
- DRAM is accessible from the VMEbus via the FORCE Gate Array FGA-002
- 32-bit high speed DMA controller for data transfers to/from the shared RAM and/or to/from the VMEbus
  – 32-byte internal FIFO for burst DMA
- FORCE Message Broadcast (FMB)
- 4 serial I/O interfaces, RS232/RS422/RS485-compatible
- 8-bit parallel interface with handshake
- 4 system EPROM devices providing a 32-bit data path. One wait state access possible by using 100 nsec devices
- 1 boot EPROM for local booting and initialization of the I/O interface chips and the gate array.
- 32 Kbyte of local SRAM with on-board battery back-up (8-bit data path)
- Real Time Clock with calendar and on-board battery back-up
- Two 24-bit timers with 5-bit prescaler
- One 8-bit timer
- Full 32-bit VMEbus interface
  – A32, A24, A16 : D8, D16, D32 – Master
  – A32, A24 : D8, D16, D32 – Slave
- SCSI interface
- Floppy disk interface (SA460 compatible) for connection of 3", 3½" and 5¼" drives
- All local I/O devices are able to interrupt the local CPU on a software-programmable level
- SYSCLK driver
- Single level VMEbus arbiter
- VMEbus Interrupt Handler (IH 1 to 7)
- Support for ACFAIL* and SYSFAIL* via software-programmable IRQ levels
- Bus time-out counters for local and VMEbus accesses (15 µsec)
- VMEPROM, the Real Time Monitor with file manager and Real Time Kernel

1. Hardware Description

1.1 The 68020 CPU

The 68020 with its 32-bit address and data paths is installed on the SYS68K/CPU-26 board. The CPU includes a 256-byte instruction cache which significantly reduces the number of bus cycles needed for program fetches.
Communication of the local I/O interfaces, local SRAM and the VMEbus interface to the 68020 CPU is provided through the specially designed 281-pin FORCE Gate Array, FGA-002.
The EPROM area, the Floating Point Co-Processor and the shared RAM are directly connected to the CPU data and address bus interface (as shown in the block diagram of the CPU-26).
The clock frequency of the 68020 CPU board is 12.5 MHz or 20.0 MHz.

1.2 The Floating Point Co-Processor

The SYS68K/CPU-26 is fitted with the enhanced 68882 Floating Point Co-Processor (FPCP). The clock frequencies of the CPU and the FPCP are identical. The FPCP conforms to the IEEE 754 Floating Point Standard. Intercommunication between the CPU and the FPCP is built in silicon.
An internal register set inside the FPCP of eight general purpose registers (80-bit wide) yields fast execution times.

Features of the FPCP

- 8 general purpose registers (80-bit : 64-bit mantissa, 15-bit exponent and 1 sign bit)
- 67-bit on-chip ALU
- 67-bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 Standard
- Full support of trigonometric and logarithmic functions such as:
  – Sine, cosine, tangent and cotangent
  – Hyperbolic functions
  – Logarithmic functions (4)
  – Square root and exponential functions (4)
- The 68882 is software-compatible to the 68881 FPCP

1.3 The Shared RAM

The SYS68K/CPU-26 contains a DRAM area with a capacity of 1or 4 Mbyte. The DRAM operates with a 200 nsec cycle time which results in a four clock access period for both the CPU and for the DMA controller at 20.0 MHz. The bandwidth of the DRAM on the SYS68K/CPU-26 is therefore 20 Mbyte/sec.
Distributed asynchronous refresh is provided every 15 µsec and an access during a pending refresh cycle is delayed by a maximum of five additional clocks.
The DRAM is also accessible from the VMEbus. The access address range and the address modifier codes are programmable by the local CPU. The start and end access addresses are programmable in 4 Kbyte increments. The defined memory range can be write-protected in combination with the address modifier codes. For example, in supervisor mode, the memory can be read and written; in user mode, it can only be read. The read/write protection mechanism is fully under the user's software control. The DRAM is accessed from the VMEbus by requesting the local bus from the CPU via the FGA-002. When the CPU has granted local bus mastership to the FGA-002 the access cycle is executed. On read cycles all data is latched, while write cycles are terminated after storing data into the DRAM cells. On completion of the read/write cycle, the FGA-002 immediately releases bus mastership to the CPU while completing the VMEbus cycle asynchronously. This early completion of VMEbus read/write cycles effectively halves the overhead to the CPU for an external access. The SYS68K/ CPU-26 includes byte parity check. A parity error, detected during an access from the VMEbus, results in a VMEbus BERR. A parity error, during a local access, results in a local interrupt. The access address which caused the parity error is stored in an FGA-002 register.

1.4 The Local SRAM

32 Kbyte of SRAM is installed on all CPU-26 board versions and supports data storage during power-down phases for up to one year. The SRAM is directly connected to the FORCE Gate Array I/O interface. Long word, word and byte transfers are automatically controlled via the gate array.
Normal read and write operations to the single 32 K x 8 SRAM are allowed if the power is within the specification detected by a separate power sensor. Higher density devices (e.g. future 512 K x 8 devices) may be inserted as the 32-pin socket allows the use of all JEDEC-compatible devices.

1.5 The System EPROMs

The SYS68K/CPU-26 contains four system EPROM sockets supporting four 28- and/or 32-pin EPROM devices. Maximum data throughput to the 68020 CPU is provided through the fast decoding logic and separate data transceivers supporting one wait state operation, if 100 nsec devices are installed. The EPROM devices are accessed by the local 68020 CPU using 32-bit accesses which enables maximum performance when accessing the EPROM area.

Supported Device Types in the System EPROM Area:

Device Type	Pins	Organization	Total Memory Capacity
27512	28	64 K × 8	256 Kbyte
2710xx	32	128 K × 8	512 Kbyte
2720xx	32	256 K × 8	1 Mbyte
TBD	32	512 K × 8	2 Mbyte
TBD	32	1 M × 8	4 Mbyte

1.6 The Boot EPROM

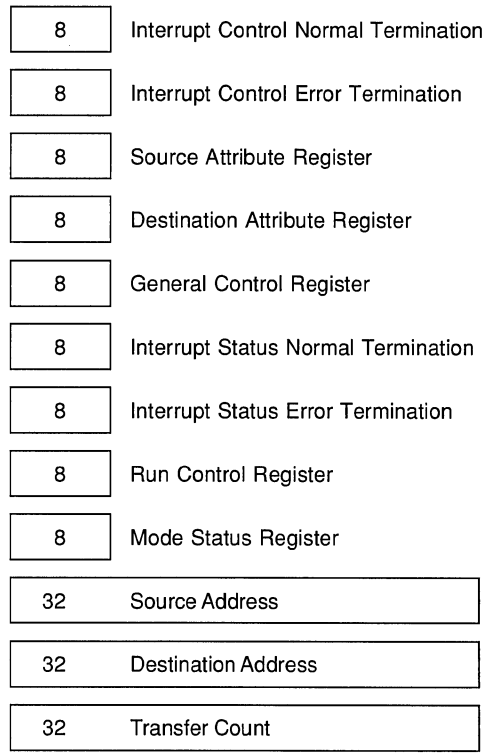
The SYS68K/CPU-26 board contains, in addition to the four system EPROMs, a single boot EPROM to boot the local CPU, initialize all I/O devices and program the board-dependent functions of the gate array, FGA-002. All the presetting and initialization of the I/O devices are made through the system EPROM to ease the adaptation of the complex board functions to the application needs.

1.7 The DMA Controller

A high speed DMA controller is installed in the FGA-002 on the SYS68K/CPU-26. It features a data transfer speed of up to 12 Mbyte/sec on the VMEbus and up to 14 Mbyte/sec to the shared RAM. The DMA controller allows the transfer of

data between VMEbus memory (two different memory areas), or between VMEbus memory and the shared RAM. The DMA controller supports 32-bit data and address paths and fully programmable address modifier codes for both source and destination.
DMA execution on the VMEbus is performed without any degradation of performance to the local CPU. This allows a program to be run while loading new data into the shared RAM or writing processed data to global RAM or I/O controller boards. Access to the shared RAM, by the DMA controller, is done by requesting bus mastership from the local CPU.
To increase the data throughput and maintain multi-processor functionality, the DMA controller operates in burst mode by using its 32-byte FIFO for internal data storage. The read and write operations are executed in eight cycles fetching 4 bytes at a time, which results in eight read cycles followed by eight write cycles. This feature maintains the real time capabilities by allowing interrupts during all DMA transfers. This technology allows data transfers between the shared RAM and the VMEbus by first collecting the data from the VMEbus, giving up bus mastership and then transferring the data to the shared RAM. A second VMEbus board can transfer data on the VMEbus while the DMA controller transfers the stored data to the shared RAM.
The CPU can operate in parallel to the DMA controller data transfers because of the 32-byte FIFO and structure of the SYS68K/CPU-26.
CPU operation means that the CPU can access all local I/O devices, the EPROM area as well as the shared RAM. When the CPU wants to access the VMEbus, it must wait until the DMA controller has finished its data transfers from its FIFO (max. eight data transfers).
Additionally, the DMA controller is connected to the on-board SCSI and floppy disk controller, allowing data transfer between mass memory devices and the shared RAM or the VMEbus memory.

Register Set of the DMA Controller



The following table shows the 68020 performance during DMA data transfer:

Area 1		Area 2	CPU Operation	Note
VMEbus	⇔	VMEbus	100 %	–
VMEbus	⇔	DPR	60–70 %	1
VMEbus	⇔	SCSI	100 %	–
VMEbus	⇔	FDC	100 %	–
DPR	⇔	SCSI	60–80 %	2
DPR	⇔	FDC	95 %	–

Note 1: CPU operation depends on the transfer speed of the addressed VMEbus board.
Note 2: CPU operation depends on the transfer speed of the SCSI device.

1.8 DMA Controller VMEbus Interface

The DMA controller supports aligned and unaligned data transfers. The internal control logic first aligns the data transfers to take full advantage of the 32-bit bus structure. The data transfer speed to the VMEbus depends on the access time of the addressed VMEbus module. By using DRAM boards the effective transfer speed reaches 8–10 Mbytes/sec. The maximum speed of 12.2 Mbyte/sec can be achieved, if high speed SRAM boards are used. The theoretical maximum transfer speed is 25 Mbyte/sec.

1.9 Benchmarks

	CPU-26XS	CPU-26XA	Unit
Dhrystones	3067	4950	Dhryst./sec
Whetstones	714	1111	KWhet./sec
Sieve	5.69	3.53	sec/100 iterations
DMA – Local	9.22	14.85	Mbyte/sec
DMA–VME	9.34	12.21	Mbyte/sec

1.10 The Local I/O Devices

The SYS68K/CPU-26 contains the gate array FGA-002 which interfaces the CPU to the I/O devices via an 8-bit-local I/O bus.
The Real Time Clock, serial I/O controllers, control and status registers, SCSI and the floppy disk controller interface to this local I/O bus.

1.11 The Real Time Clock

A software-programmable Real Time Clock (RTC-72421) with on-board battery back-up is installed on the SYS68K/CPU-26 boards.

Features of the Real Time Clock:

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12 hr/24 hr clock switch-over
- Automatic leap year setting
- Interrupt masking

The Real Time Clock is able to interrupt the local CPU on a software-programmable level (1 to 7).

1.12 The Parallel Interface

The CPU-26 contains a 12-bit parallel interface. This consists of 8 data bits and 4 control bits which may be configured for handshake signals. The parallel interface can easily be configured to support Centronics printers.

1.13 The Serial I/O Interfaces

Two Dual Universal Serial Communication Controllers (DUSCC 68562) are installed on the SYS68K/CPU-26 to communicate to terminals, computers or other equipment.

Features of the DUSCC

- Dual full-duplex synchronous/asynchronous receiver and transmitter (programmable)
- Multi-protocol operation enabling support of bit- or character-oriented protocols. With additional software, this allows the support of HDLC, SDLC, X.25, X.75, BISYNC, etc.
- Programmable data encoding formats: NRZ, NRZI, FM0, FM1, Manchester
- 4 character receiver/transmitter FIFOs
- Individual programmable baud rate for each receiver and transmitter supported by a digital phase locked loop
- Modem control signals for each channel: RTS, CTS, DCD

The I/O Signal Assignments

Pin	RS232	RS422/485
1	DCD	TXD–
2	RXD	RTS–
3	TXD	CTS+
4	DTR	RXD+
5	GND	RXD–
6	DSR	TXD+
7	RTS	RTS+
8	CTS	CTS–
9	GND	RXD–

It is also possible to connect TxC and RxC to the 9-pin conntectors via a jumper field. This is necessary for synchronous communication. The signals of DUSCC1, channel 1 are available on the P2 connector. DUSCC1, channel 2 is

configured to enable the connection of a terminal via the RS232 interface. All four channels can be configured to be RS232- or RS422/RS485-compatible. Resistive components can be installed to adapt to various cable lengths and reduce reflections for the RS422/RS485 interface. The two DUSCCs are able to interrupt the local CPU on a software-programmable IRQ-level (1 to 7) by supplying their own software-programmable IRQ vectors.

1.14 The Input/Output Ports

A total of three 8-bit I/O ports are available on the SYS68K/CPU-26. These ports are built using two 68230 PI/T devices. The remaining signals of the PI/T devices are used for various on-board control functions such as the signals for the FDC or the software readable board type and memory size. The first 8-bit port is an input port to read the two 4-bit Hex rotary switches provided on the front panel. The second port is an 8-bit I/O port with four handshake signals. These signals are routed to a 24-pin header which allows the connection of a flat cable. This port can be used for parallel I/O applications such as a Centronics compatible printer interface.

1.15 The Timers

A total of three independent timers are available for the user. These timers can be used to trigger an interrupt to the CPU on a software-programmable IRQ-level (1 to 7). The first two timers provided by the PI/Ts (68230) are 24-bit timers with individual 5-bit prescalers, the third timer (FGA-002) is 8-bit wide. This timer can be used to generate the SYSFAIL* signal to the VMEbus. SYSFAIL* can be used in multi-processor systems to signal that one board has detected a failure. All timers can be used as a watchdog or can generate interrupts on a periodical basis.

1.16 The SCSI Interface

The MB87031 SCSI controller is installed on the SYS68K/CPU-26 to interface directly to SCSI Winchester disks, optical disk drives or tape streamers.

Features of the 87031 SCSI Controller

- Full support for SCSI control
- Service of either initiator or target device
- 8-byte data buffer register incorporated
- Transfer byte counter (24-bit)
- Independent control and data transfer bus

The SCSI controller with its 8-bit DMA channel is directly connected to the installed DMA controller (inside FGA-002).
This DMA controller includes a 32-byte FIFO which is able to wait until the 32-bytes are filled and then request local bus mastership to transfer the data in only eight cycles (32-bit for each cycle).
In addition to the 32-byte DMA FIFO, the DMA channel includes a second FIFO (8-byte deep) which is filled by the DMA controller when the main 32-byte DMA FIFO is transferring data to the destination address. This allows the transfer of data on the local DMA bus continuously.
This technique permits the CPU to perform all real time functions because the ratio between CPU and DMA operation at the maximum SCSI data transfer rate is 63 % for the CPU, 30 % for the DMA controller and 7 % for the local bus arbitration overhead (BR*, BG*, BGACK* handshake).
The VMEbus P2 I/O signal assignment of the single-ended SCSI interface is fully compatible to the assignment of the SYS68K/ISCSI-1 board.
The SCSI controller on the SYS68K/CPU-26 is fully supported from the installed Real Time Kernel/Monitor VMEPROM.

1.17 The Floppy Disk Interface

The SYS68K/CPU-26 contains a single chip floppy controller, the WD1772. The installed driver/ receiver circuits allow direct connection of 3", 3½" and 5¼" floppy drives. All I/O signals are available on the user-defined pins of the P2 connector. The I/O signal assignment is compatible to the SYS68K/IOBP-1.

Features of the WD1772 Controller

- Built-in data separator
- Built-in write precompensation
- 128, 256, 512 or 1024 byte sector lengths 5¼" single and double density
- Programmable stepping rate (2 to 6 msec)

The WD1772 controller is connected via an 8-bit DMA bus to the DMA controller. The DMA interface between the floppy disk controller and the DMA controller in the FGA-002 uses the same

32-byte FIFO as the SCSI interface. This enables the DMA interface to transfer data fully asynchronous to the operation of the CPU.
The floppy disk controller is fully supported by the on-board Real Time Kernel/Monitor VMEPROM.

2. The VMEbus Interface
The SYS68K/CPU-26 includes a full 32-bit VMEbus interface, thereby taking full advantage of the VMEbus specification.
The address modifier codes for A16, A24 and A32 addressing are fully supported in master and slave mode.
In slave mode, the FGA-002 decodes the AM-codes and the address signals of the VMEbus and signals the on-board control logic, if the board is addressed correctly and if the access is to be granted (read/write protection).
The gate array forces the access cycle to the shared RAM and controls the data flow (8, 16, 24 or 32-bit of data) automatically.
The termination of the VMEbus cycle is performed independently by the FGA-002, which allows the CPU to continue normal operation.

Supported Data Transfer Modes
The following data transfer types are supported in master and slave mode:

Transfer Type	D31-24	D23-16	D15-8	D7-0
Byte				x
			x	
Word			x	x
Long Word	x	x	x	x
Unaligned Transfers	x	x	x	
		x	x	
		x	x	x
Read Modify Write				x
			x	x
	x	x	x	x

The Read-Modify-Write cycles are fully supported to synchronize multiple CPU boards via the shared RAM.

The access times to access the shared RAM from the VMEbus are listed in the following table:

Access Times	Min.	Typ	Max.
Read	600 nsec	800 nsec	1650 nsec
Write	600 nsec	800 nsec	1650 nsec

The SYS68K/CPU-26 includes the following bus arbitration modes:

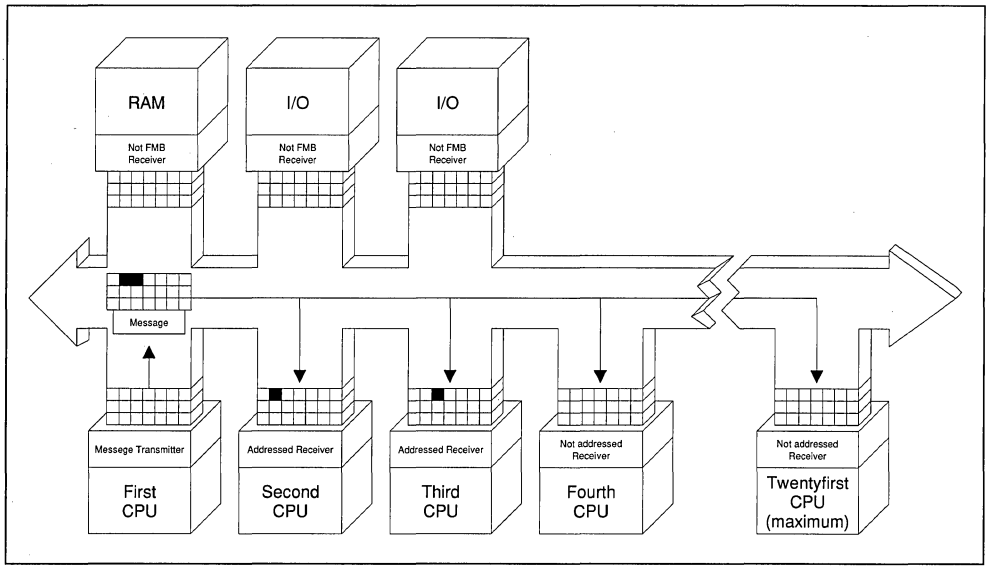
REC = Release Every Cycle
ROR = Release On Request
RBCLR = Release On Bus Clear
RAT = Release After Timeout

In addition, a fair arbitration mechanism is implemented to allow access to the VMEbus by all masters in a heavily loaded system (Request on No Request-RNR). Each of the listed modes is software-programmable inside the gate array. The bus request level of the SYS68K/CPU-26 is jumper-selectable (BR0–3*). A single level arbiter, a power monitor, a SYSRESET* generator and support for ACFAIL* and SYSFAIL* complete the VMEbus interface.

3. The Multi-Processor Mailboxes
The SYS68K/CPU-26 includes eight multi-processor mailboxes. Each of these allows an interrupt to be forced to the local 68020 CPU. The interrupt level of each mailbox is software-programmable and an individual interrupt vector for each is supplied to the CPU.
This function allows the triggering of an interrupt on the SYS68K/CPU-26 from multiple masters on the VMEbus. The mailboxes are accessed using a RMW cycle, therefore allowing multiple masters on the VMEbus to share the same mailbox channel.

4. FORCE Message Broadcast
The FORCE Message Broadcast (FMB) is a fast and effective mechanism to communicate with and to synchronize up to 20 CPU boards in a VMEbus system in only one VMEbus write cycle. It offers a unique support feature for building multi-processing systems based on the VMEbus.

Block Diagram of the FORCE Message Broadcast



An FMB transfer is a standard VMEbus write cycle and complies fully to the IEEE 1014 Specification. Any VMEbus master may be a message transmitter. The transmitter decides which boards in the system should be addressed (one, two or up to twenty boards) and writes the message to a specific address.
All addressed boards receive the message at the same time and generate an interrupt request on a programmable level to their local microprocessor. This ensures that there is no time delay between the synchronization of different boards in the system. The ability to communicate with and synchronize multiple CPUs in the system by the FMB mechanism allows the VMEbus to be used in a wide range of application areas, particularly multi-processor environments.
Without the FMB mechanism, communication between and synchronisation of system boards has to be managed via the seven interrupt request lines. FMB reduces the massive time overhead normally needed to process the interrupt cycles to just one write cycle.
All FORCE VME/PLUS boards provide two fully independent message broadcast channels. Channel 0 stores 8-bit messages in an eight stage deep FIFO, channel 1 stores one 8-bit message and can therefore be used for high priority messages.

5. The Interrupt Structure

The gate array installed on the SYS68K/CPU-26 handles all local and VMEbus interrupts. Each interrupt request via the local bus from any of the on-board devices, i.e. SCSI and floppy disk controller, the DUSCC, RTC and the two timers, as well as the gate array specific interrupt requests are combined with the seven VMEbus interrupt requests.
Each IRQ source, including the VMEbus IRQs, can be programmed to interrupt the CPU on an individual programmable level (1 to 7).
The gate array supports the vector or initiates an interrupt vector fetch from the I/O device or from the VMEbus.
In addition to the local interrupts, the ACFAIL* and SYSFAIL* signals can be used to interrupt the CPU on a software-programmable level. This results in a total of 42 individual IRQs handled through the gate array on the SYS68K/CPU-26 board. The interrupt vectors supplied by this gate array have a basic vector and fixed increments for each source. The basic vector is software-programmable.

6. The Memory Map

The memory map of the SYS68K/CPU-26ZA is listed in the following table:

Start Address	End Address	Type
00000000	003FFFFF	Shared Memory 4 Mbyte
00400000	F9FFFFFF	VMEbus, A32 : D32, D24, D16, D8
FA000000	FAFFFFFF	Message Broadcast Area
FB000000	FBFEFFFF	VMEbus, A24 : D32, D24, D16, D8
FBFF0000	FBFFFFFF	VMEbus, A16 : D32, D24, D16, D8
FC000000	FCFEFFFF	VMEbus, A24 : D16, D8
FCFF0000	FCFFFFFF	VMEbus, A16 : D16, D8
FD000000	FEFFFFFF	Reserved
FF000000	FF7FFFFF	System EPROM
FF800000	FFBFFFFF	Local I/O
FFC00000	FFCFFFFF	Local SRAM
FFD00000	FFDFFFFF	Registers of FGA-002
FFE00000	FFEFFFFF	Boot EPROM
FFF00000	FFFFFFFF	Reserved

7. Software

It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-26 Software Support

Operating System/Kernel	Vendor/Support
PDOS	FORCE COMPUTERS
OS-9/9000	Contact FORCE for availabilty
VMEPROM	FORCE COMPUTERS
VxWORKS	FORCE COMPUTERS/ Wind River Systems
VRTX-32	READY SYSTEMS
pSOS	Contact FORCE for availability
ARTX	Contact FORCE for availability
Telesoft ADA	Contact FORCE for availability

As a courtesy, FORCE provides the user with the ability to immediately start a real time application by including VMEPROM on every CPU card, free of charge and free of licensing costs.
VMEPROM is an EPROM-based Real Time Multi-tasking Kernel/Monitor. The complete package resides in 256 Kbyte of EPROM and uses 32 Kbyte of RAM. VMEPROM fully supports all of the on-board I/O devices.
VMEPROM is composed of a highly sophisticated Real Time Kernel, which is based on the PDOS Real Time Kernel. A file manager supporting sequential, random and shared files is also included.
The user interface contains more than 60 commands perfectly suited for program debugging, host computer communications, as well as task and file management. It includes a powerful debugger, supporting line assembler/disassembler for the microprocessor.

Features of VMEPROM

- Real Time Kernel supporting multi-tasking, up to 64 tasks
- File manager, supporting up to 64 open files at the same time
- Line assembler/disassembler with full support of all 680x0 instructions
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify
- S-record up/downloading from any port defined in the system
- Disk support for RAM disk, floppy and Winchester disks

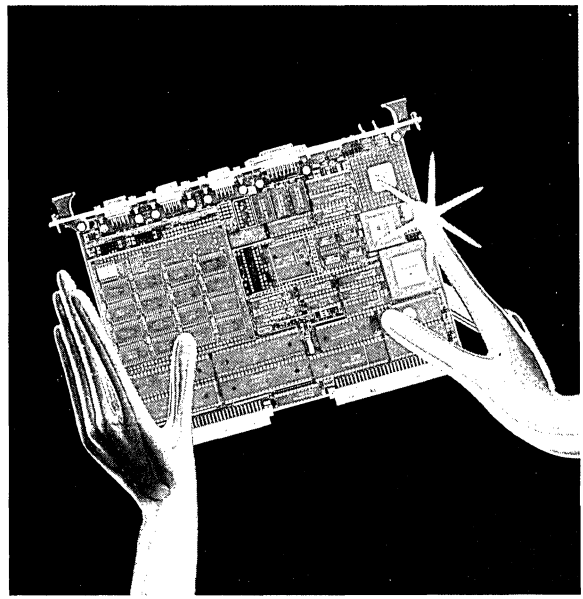
- VMEPROM allows disk formatting and initialization
- Serial I/O support for up to two SIO-2 or ISIO-2 boards in the system; local serial I/O devices are also supported
- EPROM programming utility using the SYS68K/RR-2 board
- Full screen editor
- I/O re-direction to files or ports from the command line
- Over 100 system calls to the kernel

Specifications

Function		
68020 CPU clock frequency on:	CPU-26XS CPU-26XA	12.5 MHz 20.0 MHz
68882 FPCP clock frequency on:	CPU-26XS CPU-26XA	12.5 MHz 20.0 MHz
Shared DRAM capacity with parity Local SRAM capacity with on-board battery back-up		1 or 4 Mbyte 32 Kbyte
No. of EPROM sockets (32-bit data path)		4
Serial I/O interface (total) Used controller RS232- or RS422/RS485-compatible		4 2 × 68562 4
Parallel I/O interface (68230)		12 lines
Real Time Clock with on-board battery back-up		72421
SCSI controller chip SCSI interface		87031 Single-ended
Floppy Disk Controller Interface		1772 SA 460
VMEbus interface Master: A32, A24, A16 : D8, D16, D32, UAT, RMW Slave: A32, A24 : D8, D16, D32, UAT, RMW Software-programmable access address and address modifier code Shared RAM read/write access time (min : typ : max)		 yes yes yes 600 : 800 : 1600 nsec
FORCE Message Broadcast channels		2
24-bit timers with 5-bit prescaler 8-bit timer		2 1
VMEbus interrupt handler Local interrupt handler		IH 1–7 IH 1–7
VMEPROM firmware installed on all board versions		yes
Power requirements	+ 5 V min : max + 12 V min : max – 12 V min : max	4.2 A : 5.9 A 0.1 A : 0.2 A 0.1 A : 0.2 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)		0 to + 50 °C – 40 to + 85 °C 5 to 95 %
Board dimensions		234 × 160 mm : 9.2 × 6.3 in
No. of slots used		1

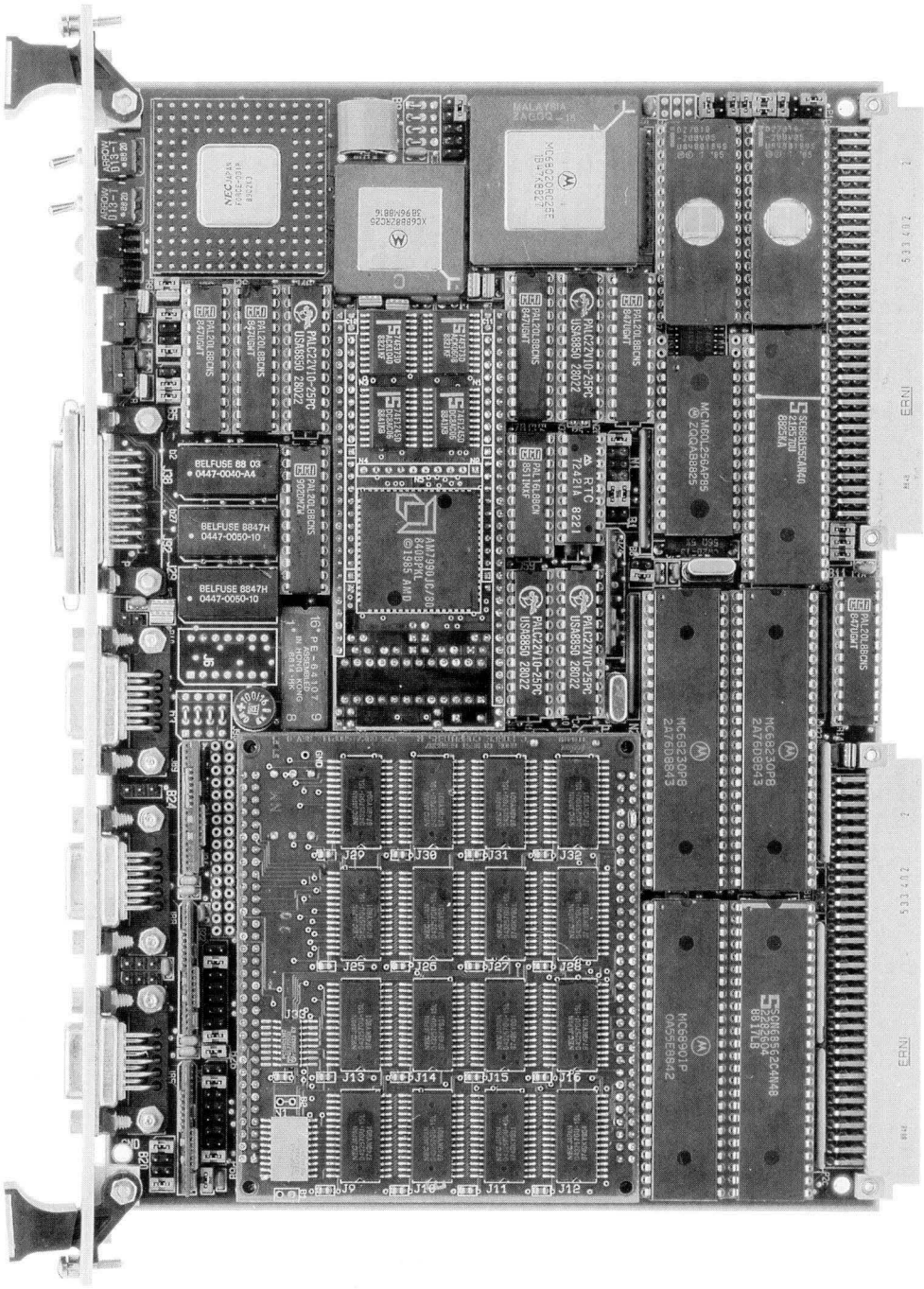
Ordering Information

SYS68K/CPU-26XS Part No. 101134	12.5 MHz 68020 based CPU board with 68882 FPCP, DMA, 1 Mbyte shared DRAM, four serial I/O, SCSI, FDC, VMEPROM. Documentation included.
SYS68K/CPU-26XA Part No. 101131	20.0 MHz 68020 based CPU board with 68882 FPCP, DMA, 1 Mbyte shared DRAM, four serial I/O, SCSI, FDC, VMEPROM. Documentation included.
SYS68K/CPU-26ZA Part No. 101132	20.0 MHz 68020 based CPU board with 68882 FPCP, DMA, 4 Mbyte shared RAM, four serial I/O, SCSI, FDC, VMEPROM. Documentation included.
SYS68K/IOBP-1 Part No. 300021	Back panel for the CPU-26 boards providing connectors for SCSI, floppy disk and one serial channel.
SYS68K/VMEPROM/26/UP Part No. 145112	VMEPROM update service for the CPU-26 series.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM user's manual, excluding the SYS68K/CPU-26 description.
SYS68K/CPU-26/UM Part No. 800141	User's manual for the SYS68K/CPU-26 including VMEPROM and FGA-002 user's manual.



System 68000 VME
SYS68K/CPU-27

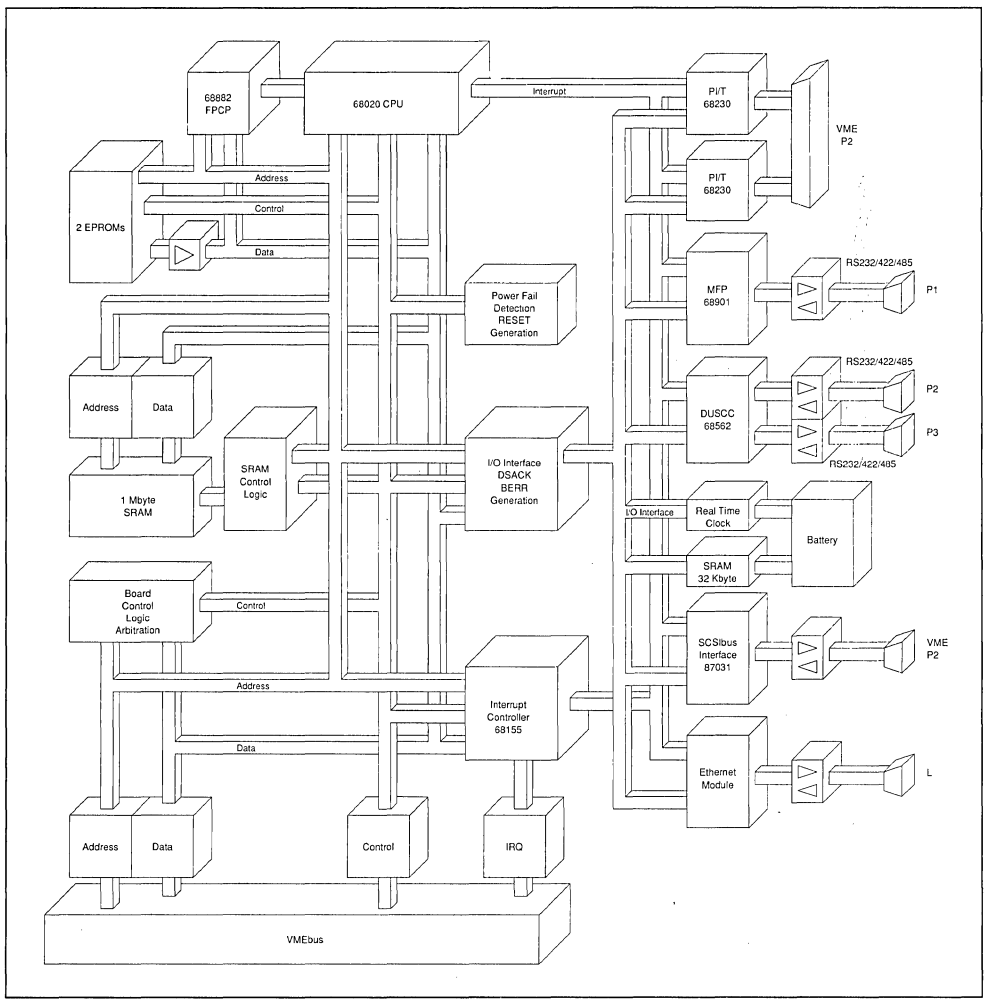
Flexible 68020 Single Board Computer with Parallel I/O


BELFUSE 88 03
0447-0040-A4
BELFUSE 8847H
0447-0050-10
BELFUSE 8847H
0447-0050-10
J9
J10
J11
J12
J13
J14
J15
J16
J25
J26
J27
J28
J29
J30
J31
J32
J33
MALAYSIA

General Description

The SYS68K/CPU-27 is a high speed CPU board using a 68020 with a clock frequency of 25 MHz. The CPU is supported by a 68882 FPCP with the same clock frequency and 1 Mbyte Static RAM.
During power-down, data retention of the static RAM area can be provided by connecting the + 5 V STBY signal of the VMEbus with a battery. Mass memory control is provided through an on-board SCSI controller. The Ethernet controller with a 64 Kbyte dedicated buffer which is provided on some board versions, allows the connection of the CPU-27 to a local area network.
Three serial I/O interfaces (one RS232- and two RS232/RS422- or RS485-compatible) support asynchronous and synchronous data transfer.
The EPROM area consists of 2 devices supporting the 28- and 32-pin JEDEC standard providing a maximum capacity of 2 Mbyte. One additional 28/32-pin JEDEC standard socket provides 32 Kbyte SRAM with battery back-up on-board.

Block Diagram of the SYS68K/CPU-27



38 parallel I/O signals are provided on the P2 connector. Two 24-bit timers and four additional independent 8-bit timers, a Real Time Clock with an on-board battery back-up and the full 32-bit VMEbus, IEEE 1014, master interface are provided on the board.
In addition, VMEPROM, the PDOS kernel based Real Time Kernel/Monitor is installed on the SYS68K/CPU-27 boards.

Features of the SYS68K/CPU-27

- 25.0 MHz 68020 CPU
- 25.0 MHz 68882 FPCP
- 1 Mbyte static RAM
- 3 serial I/O channels
  - DUSCC (68562), 2 channels
  - MFP (68901), 1 channel
- Two Parallel Interfaces (68230) and Timer devices for parallel I/O, local control and timer functions
- 68901 Multi-Function Peripheral Controller for serial I/O data transfers (RS232-compatible), parallel I/O for local control and four dependent 8-bit timers
- 68155 VMEbus and local Interrupt Handler
- SCSI bus controller using MB87031
- Local Area Network controller using AMD7990, with 64 Kbyte dedicated buffer
- Real Time Clock with on-board battery back-up (72421)
- Up to 2 Mbyte of EPROM using 2 EPROMs (28- and 32-pin JEDEC Standard)
- 32 Kbyte SRAM using one 28/32-pin socket (JEDEC Standard)
- VMEbus interface (full 32-bit) with single level arbiter:
  - A32, A24, A16 : D8, D16, D32
- Unaligned Transfer (UAT)
- Read Modify Write (RMW)
- Bus Error Timer
- Power Monitor
- SYSRESET* Generator
- Status indication LEDs
- 2 hex rotary switches
- VMEPROM installed

1. Hardware Description

1.1 The 68020 CPU

The 68020 with its 32-bit address and data paths is installed on the SYS68K/CPU-27 board. The CPU includes a 256-byte instruction cache which significantly reduces the number of bus cycles for data processing.
The EPROM area, the Floating Point Co-Processor and the SRAM are directly connected to the CPU data and address bus interface (as shown in the block diagram of the SYS68K/CPU-27). The clock frequency of the CPU is 25 MHz.

1.2 The Floating Point Co-Processor:

The SYS68K/CPU-27 is fitted with the enhanced 68882 Floating Point Co-Processor (FPCP). The clock frequency of the CPU and the FPCP is identical. The FPCP conforms to the IEEE 754 Floating Point Standard.
Easy floating point operation control to the co-processor is provided because the inter-communication between the CPU and the FPCP is built in silicon. An internal register set inside the FPCP of 8 general purpose registers (80-bit wide) yields fast execution times.

Features of the FPCP

- 8 general purpose floating point registers (80-bit, 64-bit Mantissa, 15-bit exponent and one sign bit)
- 67-bit on-chip ALU
- 67-bit barrel shifter
- 46 instruction tpyes including 35 arithmetic operations
- IEEE 754 Standard
- Full support of trigonometric and logarithmic functions such as:
  - Sine, cosine, tangent and cotangent
  - Hyperbolic functions
  - Logarithmic functions (4)
  - Square root and exponential functions (4)
- The 68882 is fully software-compatible to the 68881 FPCP

1.3. The Static RAM

The SYS68K/CPU-27 contains a static RAM area with 1 Mbyte capacity.
The 1 Mbyte static RAM area is built using 32 RAM devices which are organized as 32 K × 8 bit. Battery back-up during power-down times is provided via + 5 V STBY signal of the VMEbus. A minimum of 3V have to be supplied on this signal to guarantee data retention during power-down. The standby current is typically less than 100 µA.

1.4 The EPROM Area

The SYS68K/CPU-27 contains two user EPROM sockets supporting 28- or 32-pin JEDEC-compatible EPROM devices. Maximum data throughput to the 68020 CPU is provided through the fast decoding logic and separate data transceivers. Various EPROM memory capacities are supported from the default 256 Kbyte (using 2710xx devices) to 2 Mbyte (using 1 Mbyte × 8 devices, when available).

1.5 The SRAM Area

A 32-pin JEDEC-compatible socket is installed on the SYS68K/CPU-27. A 32 Kbyte SRAM device is installed in the socket as standard, which is supported with battery backup. The user may replace the SRAM device with larger or smaller capacity SRAM devices or EEPROM devices as required.

1.6 The Local Control Devices

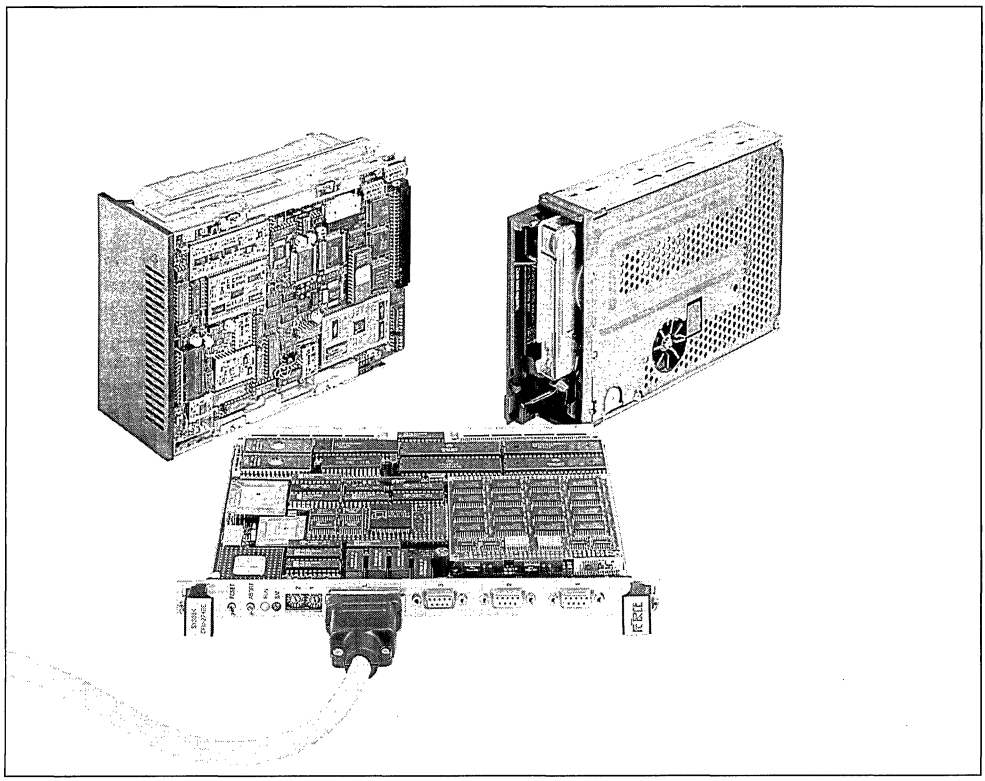
The SYS68K/CPU-27 contains two Parallel Interface and Timer (PI/T 68230) devices for local control and parallel interface control. The clock frequency of each PI/T is 8 MHz on all different board versions. Eight control bits can be read via the PI/T1 port A. These control bits can be set via two hex rotary switches available on the front panel.

The fully independent 24-bit timers can be used to interrupt the local CPU.

Both port B and C of the PI/T are partially used for local control. The SYSFAIL* and ACFAIL* signals of the VMEbus are connected to the PI/T1 and may be monitored by the local CPU.

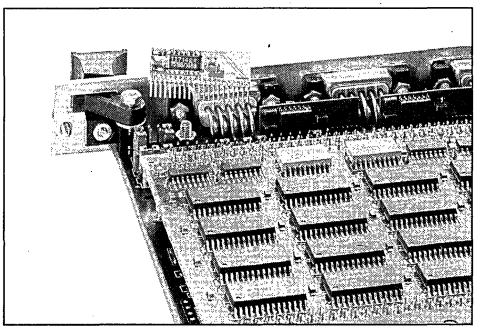
In addition to the parallel ports available on the PI/T, the multi-functional peripheral controller (MFP) 68901 has one 8-bit parallel I/O port which is also used for local control. The MFP also

Picture of the CPU-27 with I/O Devices



allows programming of the bus arbitration modes.

Serial Interface Hybrid Modules



1.7 The Serial I/O Channels

One Dual Universal Serial Communication Controller (DUSCC 68562) is installed on the SYS68K/CPU-27 to provide two ports to communicate to terminals, computers or other equipment. A Multi-Function Peripherial Controller (MFP 68901) is also installed, which provides a debug port. All three serial I/O channels are connected directly to the front panel via standard 9-pin D-Sub connectors.

Features of the DUSCC

- Dual full-duplex synchronous/asynchronous receiver and transmitter (programmable)
- Multi-protocol operation enabling support of bit-orientated and character-orientated protocols. With additional software this allows the support of HDLC, SDLC, X.25, X.75, BISYNC, etc.
- Programmable data encoding formats: NRZ, NRZI, FM0, FM1, Manchester
- Four character receiver/transmitter FIFOs
- Individual programmable baud rate for each receiver and transmitter
- Modem control signals for each channel: RTS, CTS, DCD

Each channel can be configured to work as an RS232 or as an RS422/RS485-compatible interface and is easily configurable via a socketed hybrid interface driver. The DUSCC is able to interrupt the local CPU on IRQ-level 4.

The MFP 68901

The SYS68K/CPU-27 also contains one Multi-Function Peripheral controller (MFP68901) which provides one serial interface. The RS232-compatible interface is provided on the front panel via a 9-pin D-Sub connector. The MFP is able to interrupt the local CPU on IRQ-level 3.

The following I/O signals are supported with on-board driver/receiver circuits for the three serial I/O channels by default. The DUSCC signals available on the connectors on the front panel are user-selectable via a jumperfield (e.g. TxClk, RxClk, etc.).

Pin	DUSCC Ch. 1 + DUSCC Ch. 2		MFP
	RS232	RS422/RS485	RS232
1	DCD	TXD–	N/C
2	RXD	RTS–	RXD
3	TXD	CTS+	TXD
4	DTR	RXD+	N/C
5	GND	RXD–	GND
6	DSR	TXD+	N/C
7	RTS	RTS+	RTS
8	CTS	CTS–	CTS
9	GND	RXD–	N/C

1.8 The Parallel I/O Interface of the CPU-27

38 parallel I/O signals are provided on the P2 connector of the CPU-27 as shown in the table (CPU-27 P2 Pin Assignment). These signals are controlled by two Parallel Interface and Timer (PI/T 68230) devices. Both the ports and the handshake signals of the two parallel I/O devices are provided on the P2 interface. So all functions of the 68230 can be used in the user's application.

The two parallel I/O devices are capable of interrupting the on-board processor on interrupt level 5 and 6.

The CPU-27 P2 Pin Assignment

Pin No.	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	DB 0	+ 5 V	PIT 2 PA 0
2	DB 1	GND	PIT 2 PA 1
3	DB 2	RESERVED	PIT 2 PA 2
4	DB 3	A24	PIT 2 PA 3
5	DB 4	A25	PIT 2 PA 4
6	DB 5	A26	PIT 2 PA 5
7	DB 6	A27	PIT 2 PA 6
8	DB 7	A28	PIT 2 PA 7
9	DB P	A29	PIT 2 H 1
10	GND	A30	PIT 2 H 2
11	GND	A31	PIT 2 H 3
12	GND	GND	PIT 2 H 4
13	TERMPWR	+ 5 V	PIT 2 PB 0
14	GND	D16	PIT 2 PB 1
15	GND	D17	PIT 2 PB 2
16	ATN	D18	PIT 2 PB 3
17	GND	D19	PIT 2 PB 4
18	BSY	D20	PIT 2 PB 5
19	ACK	D21	PIT 2 PB 6
20	RST	D22	PIT 2 PB 7
21	MSG	D23	PIT 2 PC 0
22	SEL	GND	PIT 2 PC 1
23	C/D	D24	PIT 2 PC 2
24	REQ	D25	PIT 2 PC 4
25	I/O	D26	PIT 1 PB 0
26	RESERVED	D27	PIT 1 PB 1
27	PIT 1 H 3	D28	PIT 1 PB 2
28	PIT 1 H 4	D29	PIT 1 PB 3
29	PIT 1 PC 4	D30	PIT 1 PB 4
30	PIT 1 PC 2	D31	PIT 1 PB 5
31	PIT 1 PC 1	GND	PIT 1 PB 6
32	PIT 1 PC 0	+ 5 V	PIT 1 PB 7

Features of the Parallel I/O Interface

- Bit I/O on all 38 signals
- Uni-directional and bi-directional 8- and 16-bit I/O
- Programmable handshake options such as interlocked or pulsed handshake

1.9 The Real Time Clock

A software-programmable Real Time Clock (RTC 72421) supported by on-board battery back-up is installed on the SYS68K/CPU-27 boards. The features of the Real Time Clock are listed below.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12 hr/24 hr clock switch-over
- Automatic leap year setting
- Interrupt masking
- CMOS design provides low power consumption during power-down mode

1.10 Local Interrupt Sources

The Interrupt Handler (68155) is installed on the SYS68K/CPU-27 to manage all the local and VMEbus interrupts. The features of the 68155 are listed below.

Features of the 68155

- Receives and prioritizes one non-maskable, seven local and six system bus interrupts
- Interrupts may be polled instead of real time operation
- Programmable local interrupt response
- Complete device status including last interrupt acknowledgement

Local Interrupt Sources:

– Test Switch	Level 7 (NMI)
– PI/T	Level 6
– PI/T	Level 5
– DUSCC	Level 4
– MFP	Level 3
– LAN Controller	Level 2
– SCSI Controller	Level 1

1.11 The SCSI Interface

The MB87031 SCSI controller is installed on the SYS68K/CPU-27 to interface directly to SCSI-compatible devices.

Features of the 87031 SCSI controller

- Service of either initiator or target device
- 8-byte data buffer register incorporated
- Transfer byte counter (24-bit)
- Synchronous/asynchronous data transfer operation

The P2 I/O signal assignment of the SCSI interface is compatible to the SYS68K/IOBP-1 board.

The SCSI interface is fully supported by VMEPROM.

1.12 Timers

The timers for the SYS68K/CPU-27 are supplied by the MFP 68901 and the PI/T 68230. The MFP provides four 8-bit timers with programmable prescalers. One of the MFP timers is used for the serial interface baud rate generator. Each PI/T provides one 24-bit timer with 5-bit prescaler.

1.13 The LAN Controller AM7990

The CPU board contains the Local Area Network Controller AM7990 (LANCE). This chip provides the user with a complete interface for Ethernet.

Features of the AM7990

- Compatible with IEEE 802.3 Rev.0
- On-chip DMA and buffer management
- 48-byte FIFO
- 24-bit wide linear addressing
- Network and packet error reporting

The chip set used provides conformance to the IEEE 802.3 Ethernet Interface Standard. This allows with additional software the support of higher level local area network communication protocols.

The LAN functional module also provides a dedicated 64 Kbyte buffer for Ethernet data transfers. This buffer is dual-ported, allowing access from both the AM7990 and from the local CPU. This 64 Kbyte closely coupled local memory allows the Ethernet Interface to function at full speed without causing CPU performance degradation. This is bacause the AM7990 functions in its own 64 Kbyte local environment during data transfers using its on-chip DMA controller, while the CPU operates unaffected on the board's main memory array. This means that the CPU and the Ethernet Controller can access memory in parallel.

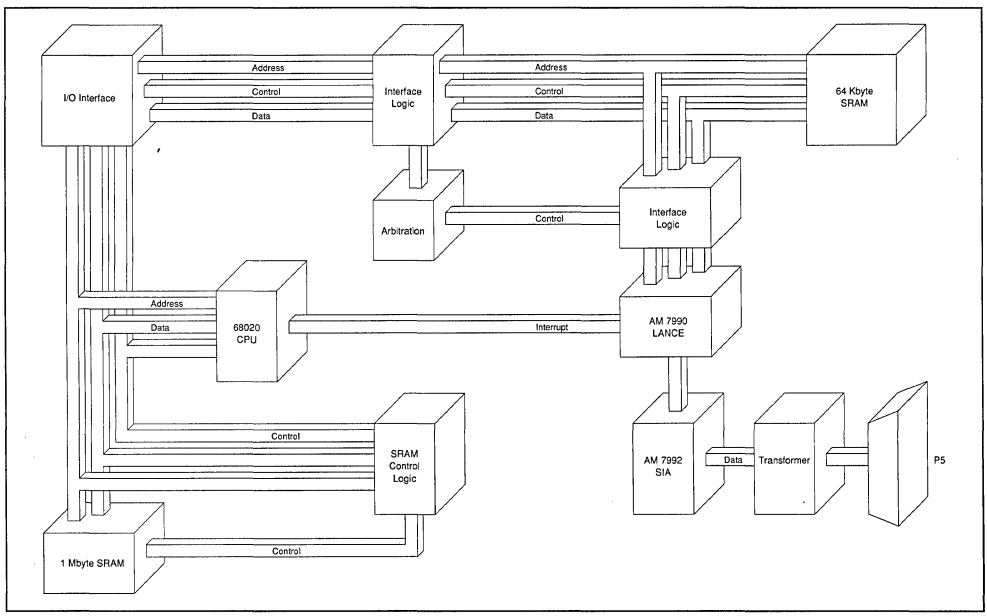
The Ethernet controller and associated support logic is only available on specific board versions.

2. The VMEbus Interface

SYS68K/CPU-27 includes a full 32-bit VMEbus interface, thereby taking full advantage of the VMEbus specification.

The address modifier codes for A16, A24 and A32 addressing modes are fully supported,

Block Diagram of the Ethernet Module



allowing 8-bit, 16-bit, 24-bit and 32-bit data transfers.
The single level arbiter on the SYS68K/CPU-27 includes the following bus arbitration modes:

REC = Release Every Cycle
ROR = Release On Request
RBCLR = Release On Bus Clear
RAT = Release After Timeout

Each of the listed modes is software-programmable. The bus request level of the CPU-27 is jumper-selectable (BR0–3*). A power monitor and a SYSRESET* generator complete the VMEbus interface.
The following data transfer types are supported:

Transfer Type	D31-24	D23-16	D15-8	D7-0
Byte				x
			x	
Word			x	x
Long Word	x	x	x	x
Unaligned Transfers	x	x	x	
		x	x	
		x	x	x
Read Modify Write				x
			x	x
	x	x	x	x

3. Software

It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-27 Software Support

Operating System/Kernel	Vendor/Support
PDOS	Contact FORCE for availability
OS-9/9000	Contact FORCE for availability
VMEPROM	FORCE COMPUTERS
VxWORKS	Contact FORCE for availability
VRTX-32	Contact FORCE for availability
pSOS	Contact FORCE for availability
ARTX	Contact FORCE for availability
Telesoft ADA	Contact FORCE for availability

As a courtesy, FORCE provides the user with the ability to immediately start a real time application by including VMEPROM on every CPU card, free of charge and free of licensing costs.
VMEPROM is an EPROM-based Real Time Multi-tasking Kernel/Monitor. The complete package resides in 256 Kbyte of EPROM and uses 32 Kbyte of RAM. VMEPROM fully supports all of the on-board I/O devices.
VMEPROM is composed of a highly sophisticated Real Time Kernel, which is based on the PDOS Real Time Kernel. A file manager supporting sequential, random and shared files is also included.
The user interface contains more than 60 commands perfectly suited for program debugging, host computer communications, as well as task and file management. It includes a powerful debugger, supporting line assembler/disassembler for the microprocessor.

Features of VMEPROM

- Real Time Kernel supporting multi-tasking, up to 64 tasks
- File manager, supporting up to 64 open files at the same time
- Line assembler/disassembler with full support of all 680x0 instructions
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify
- S-record up/downloading from any port defined in the system
- Disk support for RAM disk, floppy and Winchester disks

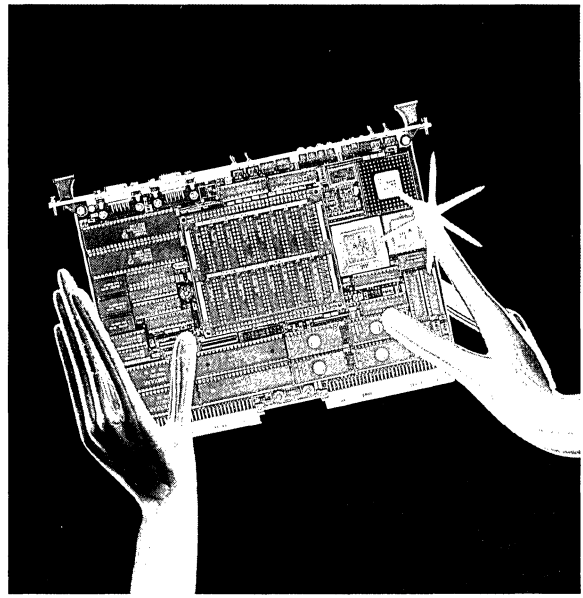
- VMEPROM allows disk formatting and initialization
- Serial I/O support for up to two SIO-2 or ISIO-2 boards in the system; local serial I/O devices are also supported
- EPROM programming utility using the SYS68K/RR-2 board
- Full screen editor
- I/O re-direction to files or ports from the command line
- Over 100 system calls to the kernel

Specifications

Function	
CPU type FPCP type	68020 68882
CPU and FPCP clock frequency on: CPU-27XB(E)	25.0 MHz
RAM type RAM capacity	SRAM 1 Mbyte
SRAM Capacity with battery back-up	32 Kbyte
No. of EPROM Sockets (32-pin) No. of wait states (min/max)	2 1/8
Serial I/O Interfaces Used Controller RS232-compatible RS232/422/485-compatible	3 68562/68901 1 of 3 2 of 3
Real Time Clock with battery back-up	72421
8-Bit Timers with programmable prescaler 24-Bit Timers with 5-bit prescaler	4 2
Parallel I/O signals Used controller Signals routed to	38 68230 P2
SCSI controller chip SCSI Interface I/O Signals routed to	87031 single-ended P2
LAN controller chip LAN memory (dual ported to local CPU)	AM7990 (Ethernet) 64 Kbyte
VMEbus A32,A24,A16: D(0),D8,D16,D32,UAT,RMW Single level bus arbiter and Slot 1 functions VMEbus Interrupt Handler	master interface yes IH 1 to 7
RESET, ABORT, function switches	yes
VMEPROM firmware installed on all board versions	yes
Power requirements + 5 V typ : max + 12 V typ : max – 12 V typ : max	5.5 : 6.0 A 0.2 : 0.4 A 0.2 : 0.4 A
Operating tempemperature with forced air cooling Storage temperature Relative humidity (non-condensing)	0 to + 50 °C – 40 to + 85 °C 5 to 95%
Board dimensions	234 × 160 mm : 9.2 × 6.3 in
No. of Slots used	1

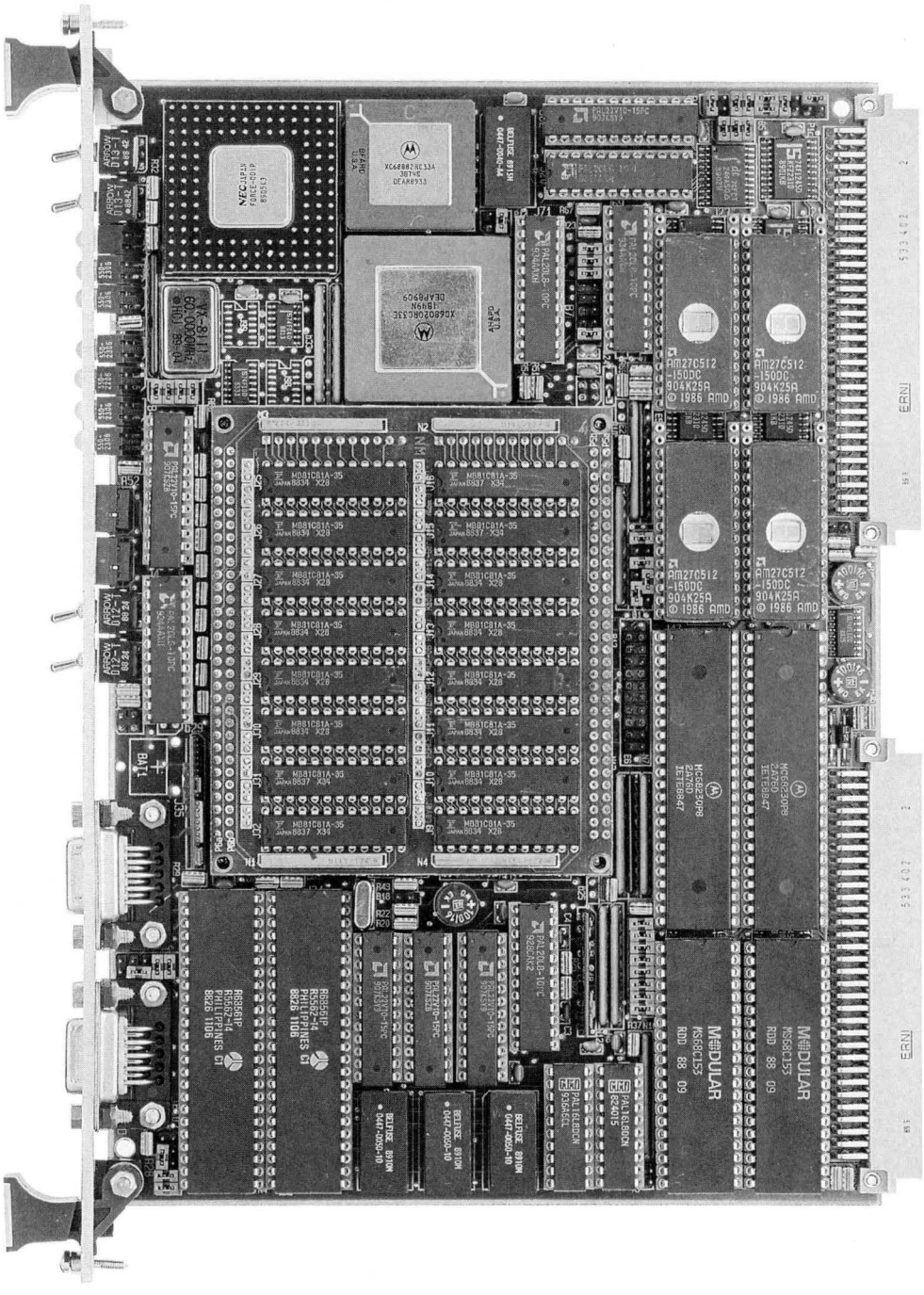
Ordering Information

SYS68K/CPU-27XB Part No. 101172	25.0 MHz 68020 based CPU board with 68882 FPCP, 1 Mbyte SRAM, 3 serial I/O, 38 parallel I/O, SCSI and VMEPROM. Documentation included.
SYS68K/CPU-27XBE Part No. 101173	25.0 MHz 68020 based CPU board with 68882 FPCP, Ethernet, 1 Mbyte SRAM, 3 serial I/O, 38 parallel I/O, SCSI and VMEPROM. Documentation included.
SYS68K/IOBP-1 Part No. 700043	Back panel for the CPU-27 board providing SCSIbus controller connectors.
SYS68K/VMEPROM/27/UP Part No. 145113	VMEPROM update service for CPU-27.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM user's manual excluding the SYS68K/CPU-27 description.
SYS68K/CPU-27/UM Part No. 800143	User Manual of SYS68K/CPU-27 family, normally included with CPU-27 shipments.



System 68000 VME
SYS68K/CPU-29

High Performance 68020 CPU Board with VSB Interface


AM27C512
-150DC
904K25A
© 1986 AMD
MODULAR
MS68C153
RDD 88 09
MC68230PR
2378D
1ETE8847
MB81C81A-35
MB81C81A-30
PAL16L8DCN
PAL20L8-10PC
PAL20R4-10PC
R6856P
R6562-14
PHILIPPINES
8826 1106
BDTIME BDTDM
0447-0004-10
BDTIME BDTDN
0447-0004-44
ERNI

General Description

The SYS68K/CPU-29 is an ultra high speed CPU board using a 68020 with a clock frequency of up to 30 MHz. This board is software-compatible to the SYS68K/CPU-21 board. The CPU-29 uses a single VMEbus slot.

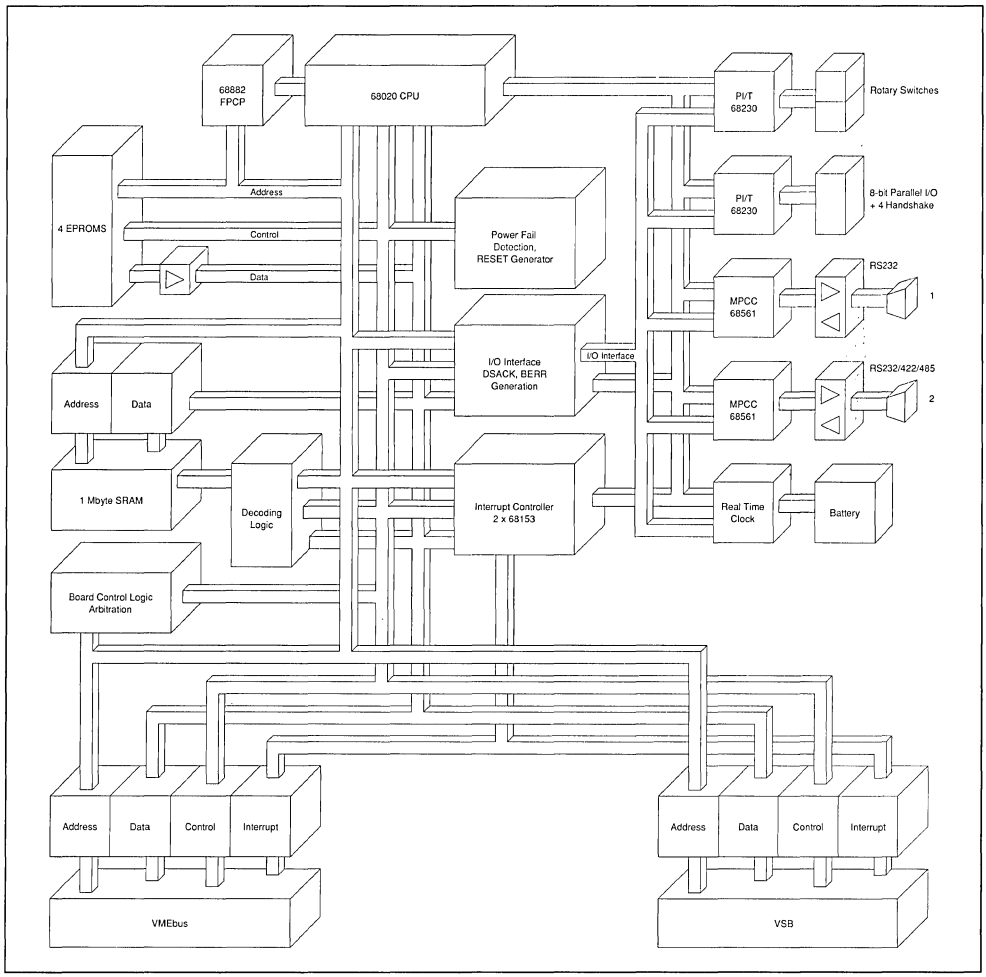
SRAM of up to 1 Mbyte capacity can be accessed from the CPU (30 MHz clock frequency) without the insertion of wait states for all read and write cycles. A full 32-bit VSB interface including bus arbitration and interrupt handling is installed on all CPU-29 board versions.

Two serial I/O interfaces (one RS232-compatible and one RS232/RS422/RS485-compatible) provide asynchronous data transfers. The EPROM area consists of four devices supporting the 28- and 32-pin JEDEC Standard which provides a maximum capacity of 4 Mbyte.

Two independent 24-bit timers, a Real Time Clock with battery back-up and a full 32-bit VMEbus master interface complete the board.

In addition, VMEPROM, the PDOS-compatible multi-user Real Time Kernel/Monitor is installed on the SYS68K/CPU-29 boards.

Block Diagram of the SYS68K/CPU-29



Features of the SYS68K/CPU-29

- 68020 CPU:
  25.0 MHz on CPU-29XB
  30.0 MHz on CPU-29XC
- 68882 FPCP:
  25.0 MHz on CPU-29XB
  30.0 MHz on CPU-29XC
- 1 Mbyte of constant zero wait state SRAM
- One 8-bit parallel interface with handshake
- Local and VMEbus interrupt management using 68153
- Two serial I/O channels, one RS232-compatible and one RS232/RS422/RS485-compatible
- Four EPROM sockets (28- and 32-pin JEDEC Standard) providing a 32-bit data path
- VSB master interface (full 32-bit) with serial arbiter:
  – A32 : D8, D16, D32
- VMEbus interface (full 32-bit) with single level arbiter:
  – A32, A24, A16 : D8, D16, D32
- Bus timer
- Power monitor
- SYSRESET* generator
- RUN/HALT, CACHE and ABORT function switches
- Status indication LEDs
- Two HEX rotary switches
- VMEPROM installed

1. Hardware Description

1.1 The 68020 CPU

The 68020 with its 32-bit address and data paths is installed on the SYS68K/CPU-29 board.
The CPU includes a 256-byte instruction cache which significantly reduces the number of bus cycles needed for program fetches. A CACHE switch on the front panel allows the user to enable or disable the on-chip cache.
The 68020 CPU accesses the SRAM with 30 MHz clock frequency without the insertion of wait states. This allows the design to take full advantage of the throughput of the CPU.
The EPROM area, the Floating Point Co-Processor, the SRAM and the VSB interface are directly connected to the CPU data and address bus interface (as shown in the block diagram of the SYS68K/CPU-29). The clock frequency of the CPU ranges from 25.0 MHz to 30.0 MHz.

1.2 The Floating Point Co-Processor

The SYS68K/CPU-29 is fitted with the enhanced 68882 Floating Point Co-Processor (FPCP). The clock frequencies of the CPU and the FPCP are identical. The FPCP conforms to the IEEE 754 Floating Point Standard.
Easy floating point operation control to the co-processor is provided because the intercommunication between the CPU and the FPCP is built in silicon.
An internal register set inside the FPCP consists of eight general purpose registers (80-bit wide) which yield fast execution times.

Features of the FPCP

- Eight general purpose registers (80-bit : 64-bit mantissa, 15-bit exponent and 1 sign bit)
- 67-bit on-chip ALU
- 67-bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 Standard
- Full support of trigonometric and logarithmic functions such as:
  – Sine, cosine, tangent and cotangent
  – Hyperbolic functions
  – Logarithmic functions (4)
  – Square root and exponential functions (4)
- The 68882 is fully software-compatible to the 68881 FPCP

1.3 The SRAM

The SYS68K/CPU-29 contains high speed SRAM offering constant no wait state access for CPU access cycles. The memory bandwidth of the SYS68K/CPU-29 reaches 40 Mbyte/sec in the 30 MHz version without any need for refresh because static RAMs are used.
All board versions access the 1 Mbyte SRAM constantly without wait states.

The following table lists the CPU board type and the wait states for SRAM accesses:

Board Type	CPU Clock Frequency	SRAM Capacity	No. of Wait States
CPU-29XB	25.0 MHz	1 Mbyte	0
CPU-29XC	30.0 MHz	1 Mbyte	0

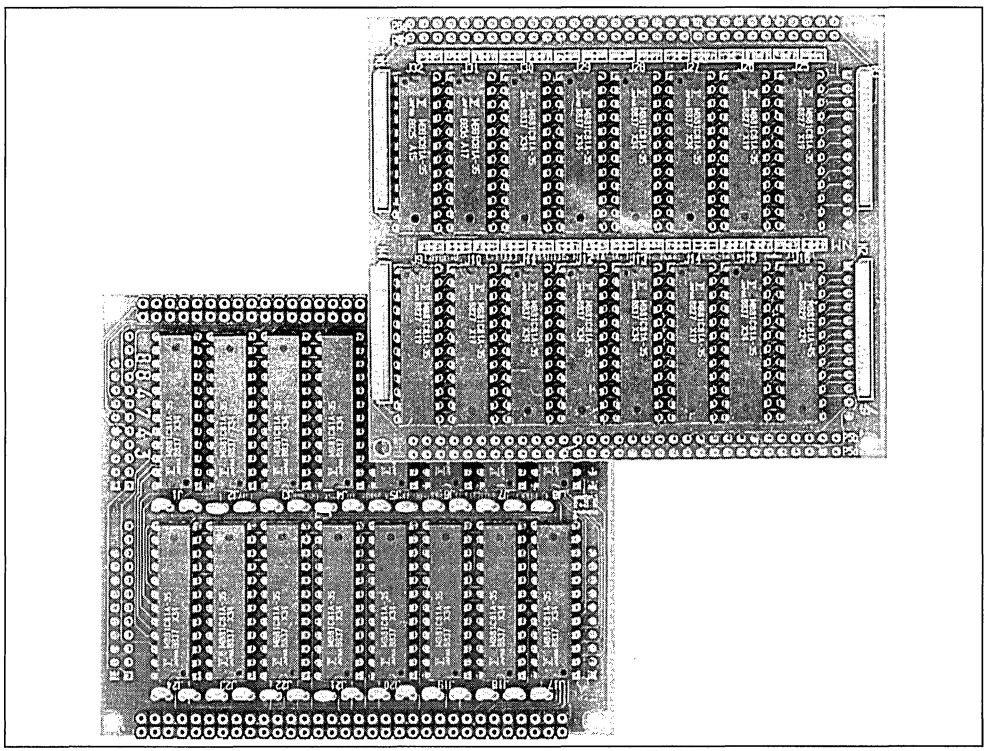
1.4 The EPROM Area

The SYS68K/CPU-29 contains four system EPROM sockets supporting 28- or 32-pin EPROM devices. Maximum data throughput to the 68020 CPU is provided through the fast decoding logic and separate data transceivers supporting one wait state operation, when 100 nsec devices are used. The following table lists the supported device types and the memory capacity.

Supported Device Types in the User EPROM Area:

Device Type	Pins	Organization	Total Memory Capacity
2764	28	8 K × 8	32 Kbyte
27128	28	16 K × 8	64 Kbyte
27256	28	32 K × 8	128 Kbyte
27512	28	64 K × 8	256 Kbyte
2710xx	32	128 K × 8	512 Kbyte
2720xx	32	256 K × 8	1 Mbyte
TBD	32	512 K × 8	2 Mbyte
TBD	32	1 M × 8	4 Mbyte

SYS68K/CPU-29 and the Memory Module



1.5 The Serial I/O Channels

The SYS68K/CPU-29 contains two Multi Protocol Communication Controllers (MPCC 68561) which include the following protocol features:

- Character-oriented protocols
- CRC check selectable
- 8-character receiver and transmit buffer
- Software-programmable baud rate
- Data rate of up to 38,400 baud

The two serial interfaces are connected to 9-pin D-Sub connectors on the front panel of the board. One interface is RS232-compatible only, the other is RS232-compatible and can be easily reconfigured to be RS422/RS485-compatible by exchanging the hybrid module supplied with the board.
Each MPCC is able to interrupt the local CPU on a software-programmable level. The interrupt vector is also software-programmable.
The following table shows the RS232 and RS422 pin assignment for the connectors on the front panel:

Pin	MPCC 1	MPCC 2	
	RS232	RS232	RS422/485
1	DCD	DCD	TXD–
2	RXD	RXD	RTS–
3	TXD	TXD	CTS+
4	DTR	DTR	RXD+
5	GND	GND	RXD–
6	DSR	DSR	TXD+
7	RTS	RTS	RTS+
8	CTS	CTS	CTS–
9	GND	GND	RXD–

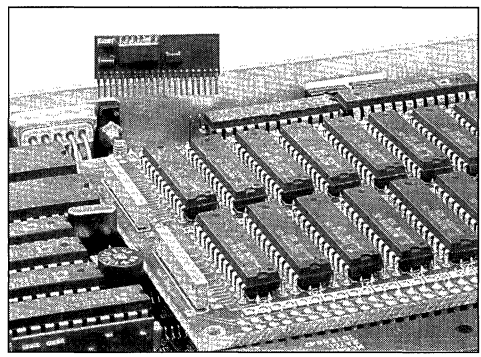
1.6 The Local Control Devices

The SYS68K/CPU-29 contains two independent Parallel Interface and Timer devices (PI/T 68230), for local control and status display.
Eight control bits can be read via the PI/T port A. These control bits can be set via two HEX rotary switches available on the front panel for manipulation. In addition, an 8-bit parallel port with two handshake signals is available on the second PI/T. This parallel port can be configured to support parallel I/O for industrial applications or parallel printers.
The PI/T also allows to program the bus release functions such as:

REC	=	Release Every Cycle
ROR	=	Release On Request
RBCLR	=	Release On Bus Clear
RAT	=	Release After Timeout

In addition, the board type (CPU-29) and the installed memory capacity can be read via a PI/T.
The two fully independent 24-bit timers with 5-bit prescalers can be used to interrupt the local CPU on a software-programmable level. The interrupt vector is also software-programmable inside the Bus Interrupter Module (68153).
All seven interrupt request levels of the CPU can be separately enabled or disabled via port B of the first PI/T.
One additional signal is used to enable/disable all VMEbus interrupts. For example, this allows the user to disable all interrupts on a certain IRQ-level while debugging application software.

Picture of the Serial Interface Hybrid Module



1.7 The Real Time Clock

A software-programmable Real Time Clock (RTC-72421) with on-board battery back-up is installed on the SYS68K/CPU-29 boards. The features of the Real Time Clock are listed below.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12 hr/24 hr clock switch-over
- Automatic leap year setting
- Interrupt masking
- CMOS design provides low power consumption during power-down mode

The Real Time Clock is able to interrupt the local CPU on a software-programmable level (1 to 7).

1.8 The Local Interrupt Sources

Two Bus Interrupter Modules (BIM 68153) are installed on the SYS68K/CPU-29 to manage all the local interrupts. Each local interrupt source can be routed to one of the seven different IRQ-levels of the CPU. The interrupt vector is also software-programmable.

Local Interrupt Sources:

1) Test Switch
2) MPCC 1
3) MPCC 2
4) PI/T 1 Timer
5) PI/T 2 Timer
6) RTC
7) VSB-IRQ
8) ACFAIL*
9) SYSFAIL*

1.9 Benchmarks

	CPU-29XB	CPU-29XC	Unit
Dhrystones	7352	8928	Dhryst./sec
Whetstones	1428	1667	KWhet./sec
Sieve	2.75	2.29	sec/100 iterations

2. The VSB Interface

The SYS68K/CPU-29 board is delivered with a full 32-bit VSB master interface.
Maximum data throughput is provided on the VSB interface, supporting 32-bit of data in the 4 Gbyte address range.
The following data transfer types are supported:

- A32 : D8, D16, D32
- Unaligned transfers
- Address only cycles
- Read-Modify-Write transfers

The VSB interface allows the systems' integrator to build contiguous local memory beyond the local SRAM. The local control logic provides an access cycle to the VSB interface before addressing the VMEbus. This technique allows an increase of the overall throughput of systems using the secondary bus. If the VSB interface is not required, a jumper setting allows it to be disabled and forces VMEbus accesses, if no on-board access cycle is decoded. The serial arbiter and the IHP Interrupt Handler complete the VSB interface.

3. The VMEbus Interface

The SYS68K/CPU-29 includes a full 32-bit VME-bus interface, thereby taking full advantage of the VMEbus specification.
The address modifier codes for A16, A24 and A32 addressing are fully supported.

Supported data transfer types:

Transfer Type	D31-24	D23-16	D15-8	D7-0
Byte				x
			x	
Word			x	x
Long Word	x	x	x	x
Unaligned Transfers	x	x	x	
		x	x	
		x	x	x
Read Modify Write				x
			x	x
	x	x	x	x

The SYS68K/CPU-29 includes the following bus release modes:

REC = Release Every Cycle
ROR = Release On Request
RBCLR = Release On Bus Clear
RAT = Release After Timeout

The bus request level of the SYS68K/CPU-29 is jumper-selectable (BR0-3*). A single level arbiter, a power monitor, a SYSRESET* generator

and support for ACFAIL* and SYSFAIL* complete the VMEbus interface.

4. Software

It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-29 Software Support

Operating System/Kernel	Vendor/Support
PDOS	FORCE COMPUTERS
OS-9/9000	FORCE COMPUTERS/MICROWARE
VMEPROM	FORCE COMPUTERS
VxWORKS	FORCE COMPUTERS/ Wind River Systems
VRTX-32	READY SYSTEMS
pSOS	Software Components Group
ARTX	Contact FORCE for availability
Telesoft	Contact FORCE for availability

As a courtesy, FORCE provides the user with the ability to immediately start a real time application by including VMEPROM on every CPU card, free of charge and free of licensing costs.

VMEPROM is an EPROM-based Real Time Multi-tasking Kernel/Monitor. The complete package resides in 256 Kbyte of EPROM and uses 32 Kbyte of RAM. VMEPROM fully supports all of the on-board I/O devices.

VMEPROM is composed of a highly sophisticated Real Time Kernel, which is based on the PDOS Real Time Kernel. A file manager supporting sequential, random and shared files is also included.

The user interface contains more than 60 commands perfectly suited for program debugging, host computer communications, as well as task and file management. It includes a powerful debugger, supporting line assembler/disassembler for the microprocessor.

Features of VMEPROM

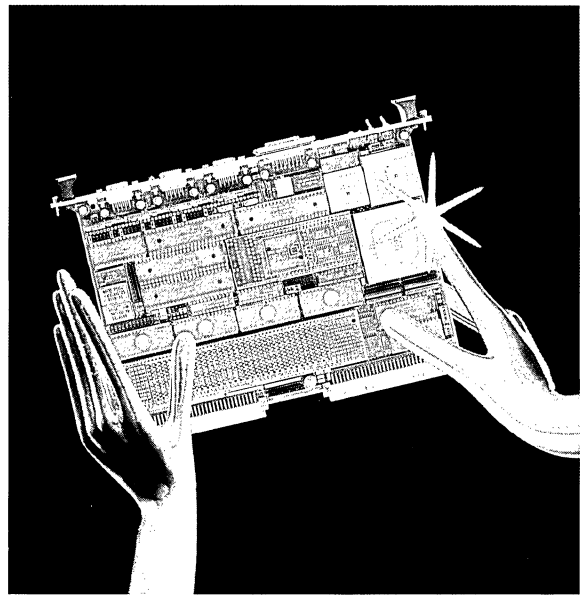
- Real Time Kernel supporting multi-tasking, up to 64 tasks
- File manager, supporting up to 64 open files at the same time
- Line assembler/disassembler with full support of all 680x0 instructions
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify
- S-record up/downloading from any port defined in the system
- Disk support for RAM disk, floppy and Winchester disks
- VMEPROM allows disk formatting and initialization
- Serial I/O support for up to two SIO-2 or ISIO-2 boards in the system; local serial I/O devices are also supported
- EPROM programming utility using the SYS68K/RR-2 board
- Full screen editor
- I/O re-direction to files or ports from the command line
- Over 100 system calls to the kernel

Specifications

Function	
68020/68882 CPU clock frequency on: CPU-29XB CPU-29XC	25.0 MHz 30.0 MHz
SRAM capacity Data path No. of wait states	1 Mbyte 32-bit 0 (all cycles)
No. of EPROM sockets (32-bit data path) Data path Max. capacity	4 32-bit 4 Mbyte
Serial I/O interface (total) Used controller RS232-compatible RS232- or RS422/RS485-compatible	2 2 × 68561 1 of 2 1 of 2
Parallel I/O interface	12 lines
Real Time Clock (type) with on-board battery back-up	72421
24-bit timers	2
VSB master interface A32: D8, D16, D32 Arbiter Interrupt handler	yes Serial IHP
VMEbus master interface A32, A24, A16: D8, D16, D32, UAT, RMW Single level bus arbiter VMEbus interrupt handler	yes yes yes IH 1 to 7
RESET, ABORT, CACHE, RUN/HALT function switches	yes
VMEPROM firmware on all board versions	yes
Power requirements + 5 V typ : max + 12 V typ : max – 12 V typ : max	4.3 A : 5.7 A 0.1 A : 0.2 A 0.1 A : 0.2 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)	0 to + 50 °C – 40 to + 85 °C 5 to 95 %
Board dimensions	234 × 160 mm : 9.2 × 6.3 in
No. of slots used	1

Ordering Information

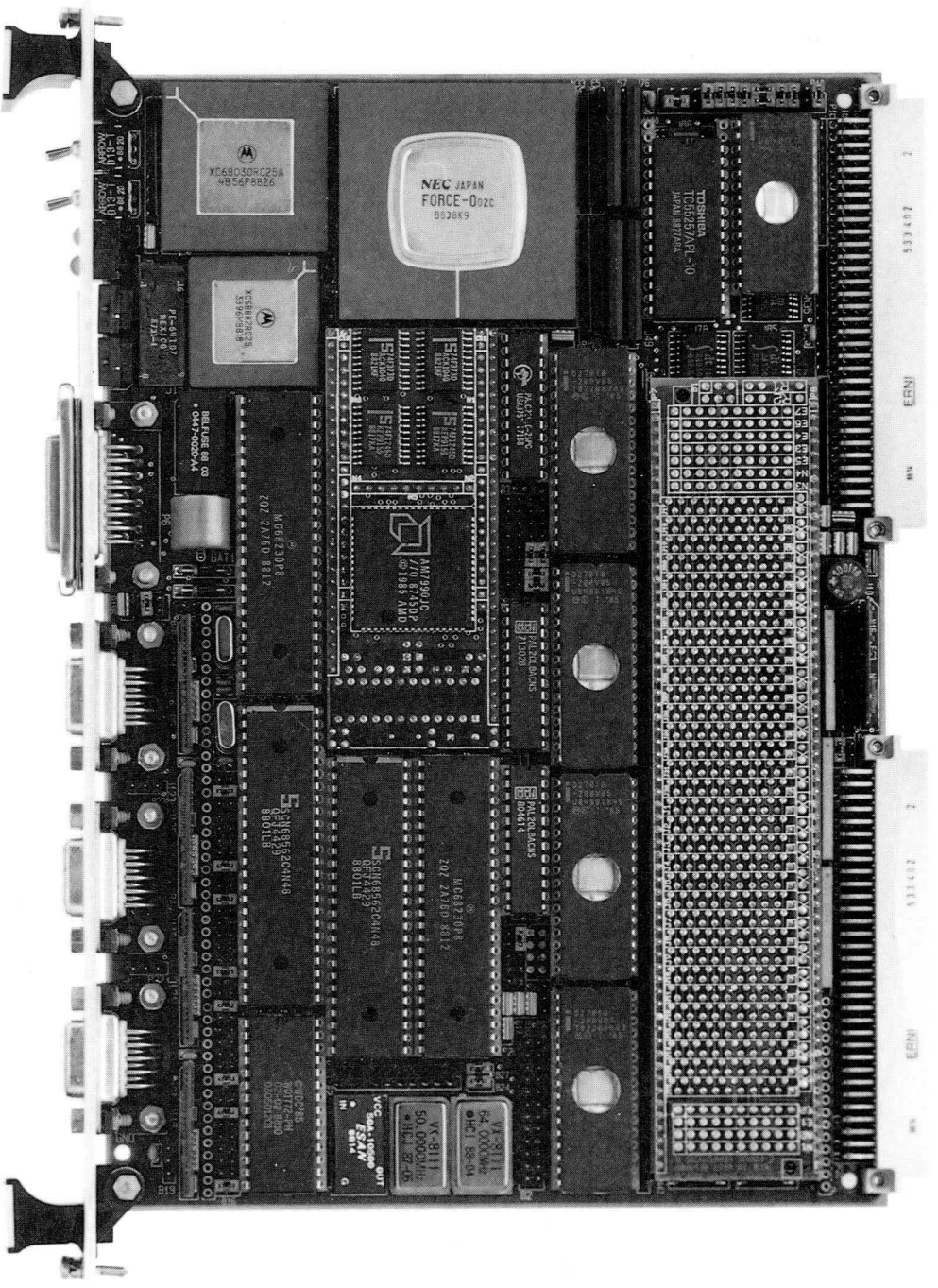
SYS68K/CPU-29XB Part No. 101153	25.0 MHz 68020 CPU board with 1 Mbyte zero wait state SRAM, FPCP, parallel I/O, 2 serial I/O, VSB and VMEPROM. Documentation included.
SYS68K/CPU-29XC Part No. 101154	30.0 MHz 68020 CPU board with 1 Mbyte zero wait state SRAM, FPCP, parallel I/O, 2 serial I/O, VSB and VMEPROM. Documentation included.
SYS68K/VMEPROM/29/UP Part No. 145107	VMEPROM update service for the CPU-29 series.
SYS68K/VMEPROM/UM Part No. 800140	User's manual of VMEPROM, excluding documentation of the SYS68K/CPU-29.
SYS68K/CPU-29/UM Part No. 800145	User's manual for all SYS68K/CPU-29 board versions, VMEPROM documentation included.



System 68000 VME

SYS68K/CPU-30

High Performance General Purpose 68030 CPU Board with Shared Memory, DMA and Mass Memory Control

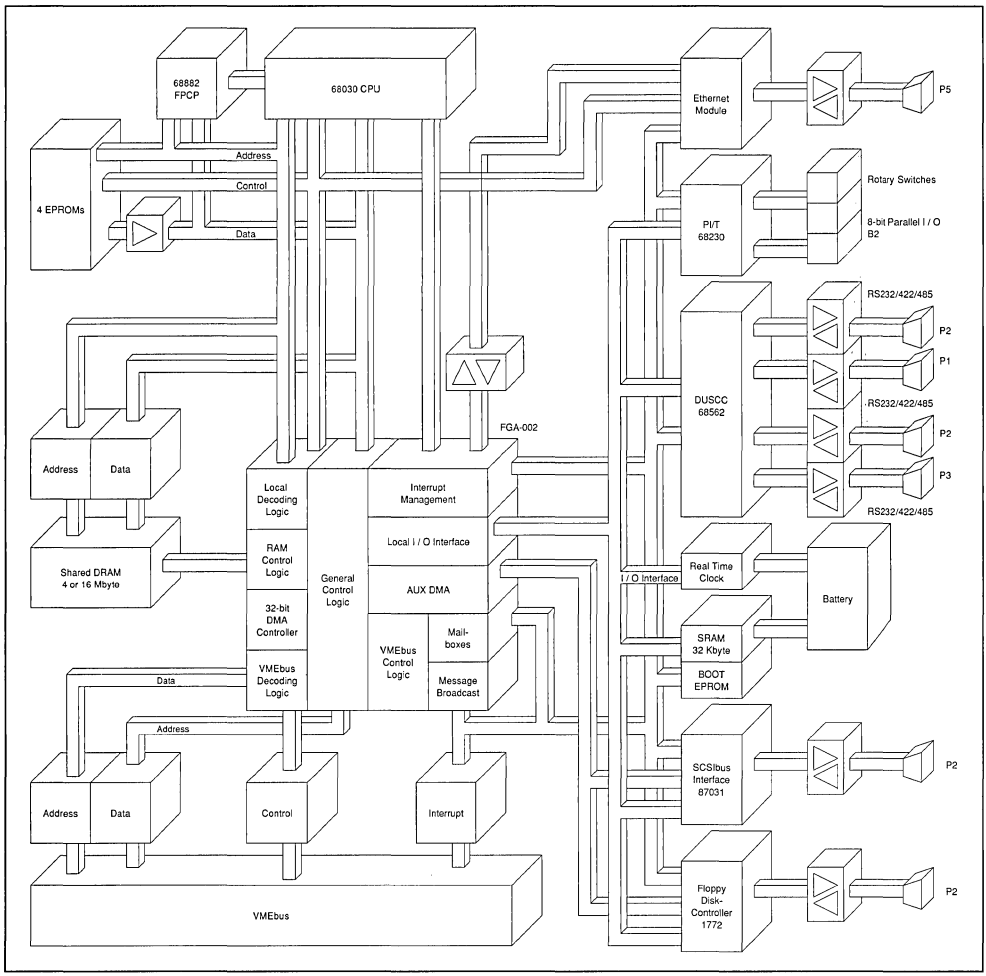

XC68030RC25A
4B56P8826
NEC JAPAN
FORCE-002C
8838K9
TOSHIBA
TC55257APL-10
AM7990JC
/70 8745DP
©1985 AMD
MC68230P8
9Z7 7AY6D 8812
MC68562C4N40
9Z7 7AT6D 8812
MC68562C4N40
9Z7 7AT6D 8812
PAL20L8ACNS
PAL20L8ACNS
VK-8111
64.000MHz
VK-8111
50.000MHz
VCC-SAA-1099P
ESAM
8814

General Description

The SYS68K/CPU-30 is a 68030/68882 based CPU board providing up to 16 Mbyte of shared memory. A full 32-bit DMA controller, supporting data transfers to/from VMEbus memory as well as to/from local RAM is provided by the 281-pin FORCE Gate Array (FGA-002).

Mass memory control is provided through a SCSI controller and a single chip floppy disk controller. Both are connected to the 32-bit DMA controller providing rapid data throughput to connected mass memory devices. Serial communication is provided through four fully independent multi-protocol channels. A LAN controller with its own 64 Kbyte data buffer allows the interconnection of the CPU-30 board via a standard Ethernet connector installed on the front panel. The LAN controller is available only on specific board versions. Additional features include up to 4 Mbyte EPROM capacity, 32 Kbyte SRAM and a Real Time Clock. VMEPROM, the Real Time Kernel, is installed by default. Two FORCE Message Broadcast channels and eight mailbox interrupts complete the board.

Block Diagram of the SYS68K/CPU-30



Features of the SYS68K/CPU-30

- 68030 CPU:
  20.0 MHz on CPU-30ZA
  25.0 MHz on CPU-30ZBE, -30BE/16
- 68882 FPCP:
  20.0 MHz on CPU-30ZA
  25.0 MHz on CPU-30ZBE, -30BE/16
- 32-bit high speed DMA controller for data transfers to/from the shared RAM and/or to/from VMEbus memory
  - 32-byte internal FIFO for burst DMA
- 4 or 16 Mbyte of shared DRAM with byte parity, supporting the 68030 burst fill mode
- The DRAM is accessible from the VMEbus via the FORCE Gate Array, FGA-002
- FORCE Message Broadcast (FMB)
- Four serial I/O interfaces, RS232/RS422/RS485-compatible
- 8-bit parallel interface with handshake
- Four system EPROM devices supporting 28- and 32-pin devices, using a 32-bit data path
  - 1 wait state access possible by using 100 nsec devices
- One boot EPROM for local booting and initialization of the I/O interface chips and the gate array
- 32 Kbyte SRAM with battery back-up on-board, using one 28/32-pin socket (JEDEC Standard)
- Real Time Clock with calendar and on-board battery back-up
- SCSI interface connected to the on-board DMA controller
- Floppy disk interface (SA460-compatible) for connection of 3", 3½" and 5¼" drives
- Local Area Network Controller for connection to Ethernet
- Two 24-bit timers with 5-bit prescaler
- One 8-bit timer
- All local I/O devices are able to interrupt the local CPU on a software-programmable level
- BERR handling fully under software control via different counters for local and VMEbus accesses
- Full 32-bit VMEbus master/slave interface supporting the following data transfer types:
  - A32, A24, A16 : D8, D16, D32 – Master
  - A32 : D8, D16, D32 – Slave
  - UAT and Read-Modify-Write cycles are also supported
- Single-level VMEbus arbiter
- SYSCLK driver
- VMEbus Interrupt Handler
- Support for ACFAIL* and SYSFAIL* via software-programmable IRQ levels
- Bus time-out counters for local and VMEbus accesses (15 µsec)
- VMEPROM, the Real Time Monitor with file manager and Real Time Kernel

1. Hardware Description

1.1 The 68030 CPU

The 68030 with its 32-bit address and data paths is installed on the SYS68K/CPU-30 board. The CPU includes a 256-byte instruction and a 256-byte data cache which significantly reduces the number of bus cycles needed for program fetches.
The 68030 CPU can access the DRAM in normal and burst fill mode. This allows the design to take full advantage of the throughput of the CPU.
Communication with the local I/O interfaces, local SRAM and the VMEbus interface to the 68030 CPU is provided through a specially designed 281-pin gate array, called FGA-002.
The EPROM area, the Floating Point Co-Processor and the shared DRAM are directly connected to the CPU data and address bus interface (as shown in the block diagram of the CPU-30).
The clock frequency of the 68030 CPU is 20.0 MHz or 25.0 MHz.

1.2 The Floating Point Co-Processor

The SYS68K/CPU-30 is fitted with the enhanced 68882 Floating Point Co-Processor (FPCP). The clock frequencies of the CPU and the FPCP are identical. The FPCP conforms to the IEEE 754 Floating Point Standard. Intercommunication between the CPU and the FPCP is built in silicon. An internal register set inside the FPCP of eight general purpose registers (80-bit wide) yields fast execution times.

Features of the FPCP

- Eight general purpose registers (80-bit : 64-bit mantissa, 15-bit exponent and 1 sign bit)
- 67-bit on-chip ALU
- 67-bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 Standard

- Full support of trigonometric and logarithmic functions such as:
  - Sine, cosine, tangent and cotangent
  - Hyperbolic functions
  - Logarithmic functions (4)
  - Square root and exponential functions (4)
- The 68882 is fully software-compatible to the 68881 FPCP

1.3 The Shared RAM

The SYS68K/CPU-30 contains a DRAM area with a capacity of 4 or 16 Mbyte. The DRAM is accessible from the 68030 CPU both in the "normal" mode and "burst fill" mode. At 25 MHz every DRAM access takes 5 clock cycles. Subsequent burst accesses operate at 2 clock cycles each. The bandwidth of the DRAM on the CPU-30 is therefore 36 Mbyte/sec.

Distributed asynchronous refresh is provided every 15 µsec and an access during a pending refresh cycle is delayed by a maximum of five additional clocks.

The DRAM is also accessible from the VMEbus. The access address range and the address modifier codes are programmable by the local CPU.

The start and end access addresses are programmable in 4-Kbyte increments. The defined memory range can be write-protected in combination with the address modifier codes. For example, in supervisor mode, the memory can be read and written; in user mode, it can only be read. The read/write protection mechanism is fully under the user's software control.

The DRAM is accessed from the VMEbus by requesting the local bus from the CPU via the FGA-002. When the CPU has granted local bus mastership to the FGA-002 the access cycle is executed. On read cycles all data is latched, while write cycles are terminated after storing data into the DRAM cells. On completion of the read/write cycle, the FGA-002 immediately releases bus mastership to the CPU while completing the VMEbus cycle asynchronously. This early completion of VMEbus read/write cycles effectively halves the overhead to the CPU for an external access.

The SYS68K/CPU-30 includes byte parity check. A parity error, detected during an access from the VMEbus, results in a VMEbus BERR. A parity error, during a local access, results in a local interrupt. The access address which caused the parity error is stored in an FGA-002 register.

1.4 The Local SRAM

A 32-Kbyte SRAM (battery back-up on-board) is installed on all SYS68K/CPU-30 board versions which supports data storage during power-down phases for up to one year. The SRAM is directly connected to the FORCE Gate Array (FGA-002) I/O interface. Long word, word and byte transfers are automatically controlled via the gate array.

Normal read/write operations to the SRAM are allowed, if the power is within the specification detected by a separate power sensor. The board is delivered with a 32 K x 8 SRAM. Higher density devices (e.g. future 512 K x 8 devices) or EPROM devices may be inserted as the 32-pin socket allows the use of all JEDEC-compatible devices.

1.5 The System EPROMs

The SYS68K/CPU-30 contains four system EPROM sockets supporting four 28- and/or 32-pin EPROM devices. Maximum data throughput to the 68030 CPU is provided through the fast decoding logic and separate data transceivers supporting one wait state operation, if 100 nsec devices are installed. The EPROM devices are read by the local 68030 CPU using 32-bit accesses which enables maximum performance.

Supported Device Types in the System EPROM Area:

Device Type	Pins	Organization	Total Memory Capacity
27512	28	64 K × 8	256 Kbyte
2710xx	32	128 K × 8	512 Kbyte
2720xx	32	256 K × 8	1 Mbyte
TBD	32	512 K × 8	2 Mbyte
TBD	32	1 M × 8	4 Mbyte

1.6 The Boot EPROM

The SYS68K/CPU-30 board contains, in addition to the four system EPROMs, a single boot EPROM to boot the local CPU, initialize all I/O devices and program the board dependent functions of the gate array (FGA-002). All the presetting and initialization of the I/O devices are made through the boot EPROM.

1.7 The DMA Controller

A high speed DMA controller is installed on the SYS68K/CPU-30. It features a maximum data transfer speed of up to 12.9 Mbyte/sec on the VMEbus and 14.9 Mbyte/sec to the shared RAM. DMA execution on the VMEbus is performed without any degradation of performance for the local CPU. This allows a program to be run while loading new data into the shared RAM or writing processed data to global RAM or I/O controller boards. If the data has to be stored or read to/from the shared RAM, the DMA controller requests bus mastership from the local CPU.
To increase the data throughput, the DMA controller operates using a 32-byte FIFO for internal data storage. The read and write operations are executed in eight cycles, 4 byte at a time, which results in eight read cycles followed by eight write cycles.
This feature significantly increases data throughput because the local CPU maintains the real time capabilities by being interruptable during DMA transfers on the VMEbus.
This technology allows data transfers between the shared RAM and the VMEbus by first collecting data from the VMEbus, giving up bus mastership and then transferring the data to the shared RAM. A second VMEbus board can transfer data on the VMEbus while the DMA controller transfers the stored data to the shared RAM.

The CPU can operate in parallel to the DMA controller data transfers because of the 32-byte FIFO and the structure of the SYS68K/CPU-30.
This means that during DMA transfers, the CPU can access all local I/O devices, the EPROM area as well as the shared RAM. When the CPU wants to access the VMEbus, it has to wait until the DMA controller has completed the transfers from its FIFO (max. eight transfers). Additionally, the DMA controller is connected to the on-board SCSI and floppy disk controller, allowing data transfer between mass memory devices and the shared RAM or the VMEbus memory. The DMA controller supports aligned and unaligned data transfers. The internal control logic first aligns the data transfers to take full advantage of the 32-bit bus structure.

The following table shows the 68030 performance during the DMA data transfers:

Area 1		Area 2	CPU Operation	Note
VMEbus	⇔	VMEbus	100 %	–
VMEbus	⇔	DPR	60–70 %	1
VMEbus	⇔	SCSI	100 %	–
VMEbus	⇔	FDC	100 %	–
DPR	⇔	SCSI	70–90 %	2
DPR	⇔	FDC	95 %	–

Note 1: CPU operation depends on the transfer speed of the addressed VMEbus board.
Note 2: CPU operation depends on the transfer speed of the SCSI device.

Register Set of the DMA Controller

8	Interrupt Control Normal Termination
8	Interrupt Control Error Termination
8	Source Attribute Register
8	Destination Attribute Register
8	General Control Register
8	Interrupt Status Normal Termination
8	Interrupt Status Error Termination
8	Run Control Register
8	Mode Status Register
32	Source Address
32	Destination Address
32	Transfer Count

1.8 The Local I/O Devices

The SYS68K/CPU-30 contains a gate array (FGA-002) which provides an 8-bit local I/O interface used to interconnect the CPU and the I/O devices.
The Real Time Clock, serial I/O controllers, the parallel I/O, control and status registers, SCSI and the floppy disk controller are connected to this local I/O interface. The Ethernet controller and the 64 Kbyte memory of the Ethernet module are connected to the CPU and controlled by the on-board logic.

1.9 The Serial I/O Interfaces

Two Dual Universal Serial Communication Controllers (DUSCC 68562) are installed on the SYS68K/CPU-30 to communicate to terminals, computers or other equipment.

Features of the DUSCC

- Dual full-duplex synchronous and asynchronous receiver and transmitter (programmable)
- Multi-protocol operation enabling support of bit- or character-oriented protocols. With additional software this allows the support of HDLC, SDLC, X.25, X.75, BISYNC, etc.
- Programmable data encoding formats: NRZ, NRZI, FM0, FM1, Manchester
- 4 character receiver/transmitter FIFOs
- Individual programmable baud rate for each receiver and transmitter supported by a digital phase locked loop
- Modem control signals for each channel: RTS, CTS, DCD

One of the four available serial I/O channels is connected to the VMEbus P2 connector. The remaining three channels are routed to 9-pin D-sub connectors on the front panel. All four serial I/O channels are connected to RS232-compatible drivers/receivers and can also be configured for RS422/485-compatibility. The DUSCCs can interrupt the local CPU on a software-programmable level (1 to 7).
It is also possible to connect TxClk and RxClk to the 9-pin connectors via a jumperfield. This is necessary for synchronous communication.

Serial I/O Signal Assignments

Pin	RS232	RS422/485
1	DCD	TXD-
2	RXD	RTS-
3	TXD	CTS+
4	DTR	RXD+
5	GND	RXD-
6	DSR	TXD+
7	RTS	RTS+
8	CTS	CTS-
9	GND	RXD-

1.10 The Real Time Clock

A software-programmable Real Time Clock (RTC-72421) with on-board battery back-up is installed on the SYS68K/CPU-30 boards.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12 hr/24 hr clock switch-over
- Automatic leap year setting
- Interrupt masking
- CMOS design provides low power consumption during power-down mode

The Real Time Clock is able to interrupt the local CPU on a level programmable through the gate array (1 to 7).

1.11 The Input/Output Ports

A total of three 8-bit input ports and one 12-bit input/output port (8-bit data 4-bit handshake) are available on the SYS68K/CPU-30.
The first 8-bit input port is connected to the two 4-bit HEX rotary switches provided on the front panel. These are available for user dependent board and firmware configuration settings.
The second 8-bit input port allows the jumper settings to be read (one or zero) on a jumper field installed on the SYS68K/CPU-30 PCB. This jumper field can be used to define application dependent presettings.
The third 8-bit input port allows the memory capacity of the shared memory to be read. Each SYS68K/CPU-30 board has three readable status bits describing the memory capacity. In addition, the CPU board type can be read via the remaining 5 bits.
The 12-bit I/O port is routed to a 24-pin header which allows the connection of a flat cable. 8 bits are connected to the port A of a PI/T and can be used as inputs or outputs, the remaining 4 bits are connected to the handshake pins of the PI/T.
This port can be used for parallel I/O applications such as a Centronics-compatible printer interface.

1.12 The Timers

A total of three independent timers are available for the user. These timers offer maximum flexibility because each timer can be used to force an interrupt to the CPU on a software-programmable IRQ-level (1 to 7).
The first two timers each provide a 24-bit timer with an individual 5-bit prescaler. The third timer can also be used to generate interrupts to the CPU and the SYSFAIL* signal to the VMEbus. It can also be used to act as a watchdog. This timer is an 8-bit timer with programmable source clock divider installed in the gate array (FGA-002). SYSFAIL* can be used in multi-processor systems to signal that one board has detected a failure. The watchdog timer needs to be reset periodically (software-programmable). Without such a reset a SYSFAIL* will be asserted on the VMEbus. All installed timers can be used as a watchdog timer or can generate interrupts on a periodical basis.

1.13 The SCSI Interface

The MB87031 SCSI controller is installed on the SYS68K/CPU-30 to interface directly to SCSI Winchester disks, optical drives or tape streamers. The SCSI controller with its 8-bit DMA channel is directly connected to the installed DMA controller (inside FGA-002). In addition to the 32-byte DMA FIFO, the DMA channel includes a second FIFO (which is 8-byte deep) which substitutes for the main DMA FIFO, when DMA transfers to the main memory are taking place. This allows the transfer of data on the local DMA interface continuously.
The I/O signal assignment of the single-ended SCSI interface is fully compatible to the assignment of the SYS68K/ISCSI-1 board which allows the use of the SYS68K/IOBP-1 for interconnection to mass memory devices.

Features of the 87031 SCSI Controller

- Full support for SCSI control
- Service of either initiator or target device
- 8-byte data buffer register incorporated
- Transfer byte counter (24-bit)
- Independent control and data transfer bus

1.14 The Floppy Disk Interface

The SYS68K/CPU-30 contains a single chip floppy disk controller, the WD1772. The installed driver/receiver circuits allow direct connection of 3", 3½" and 5¼" floppy drives.

Features of the WD1772 Controller

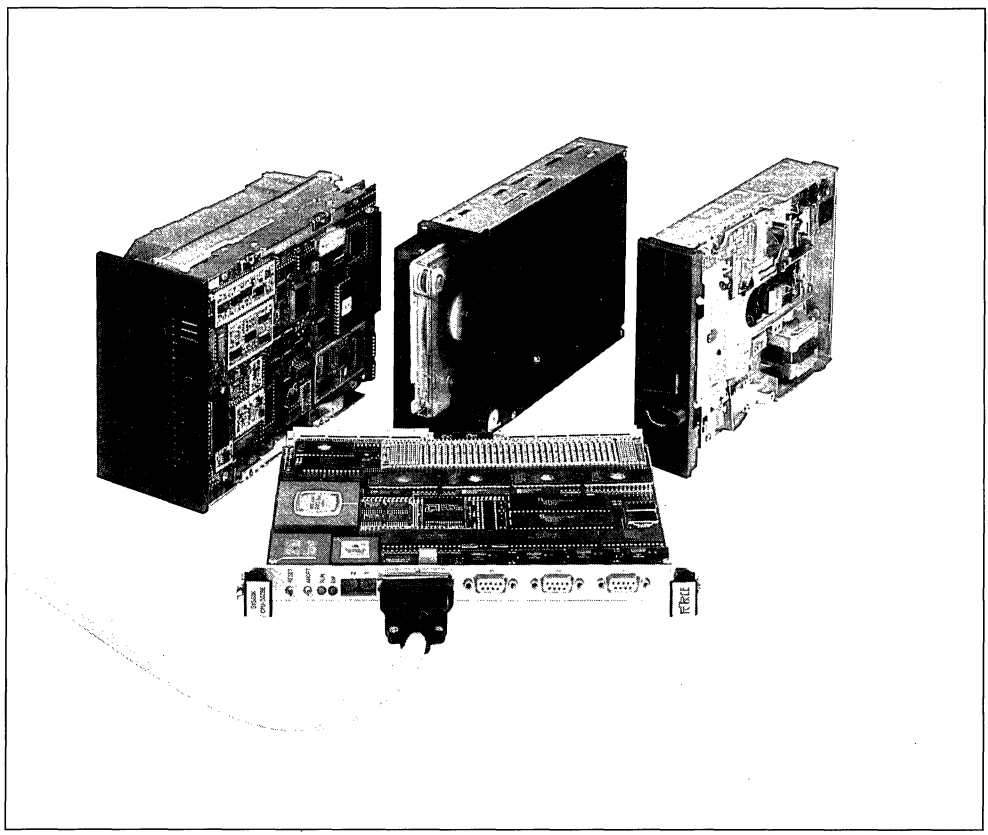
- Built-in data separator
- Built-in write precompensation
- 128, 256, 512 or 1024 byte sector lengths
- 5¼" single and double density
- Programmable stepping rate (2 to 6 msec)

All I/O signals are available on the user-defined pins of the P2 connector. The I/O signal assignment is compatible to the SYS68K/ISCSI-1 controller which allows the use of the SYS68K/IOBP-1 for interconnection to mass memory devices. The WD1772 controller is connected via an 8-bit bus to the DMA controller in the FGA-002, which allows the transfer of data fully asynchronous to the operation of the CPU. The single chip floppy disk controller includes a phase locked loop and data separation logic which means there is no need for adjustment. The floppy disk controller is fully supported by the on-board Real Time Monitor VMEPROM.

1.15 The LAN Controller AM7990

Some versions of the CPU board contain the Local Area Network Controller AM7990 (LANCE). This chip provides the user with a complete interface for Ethernet.

SYS68K/CPU-30 and Mass Memory Devices



Features of the AM7990

- Compatible with IEEE 802.3 Rev.0
- On-chip DMA and buffer management
- 48-byte FIFO
- 24-bit wide linear addressing
- Network and packet error reporting
- Diagnostic routines

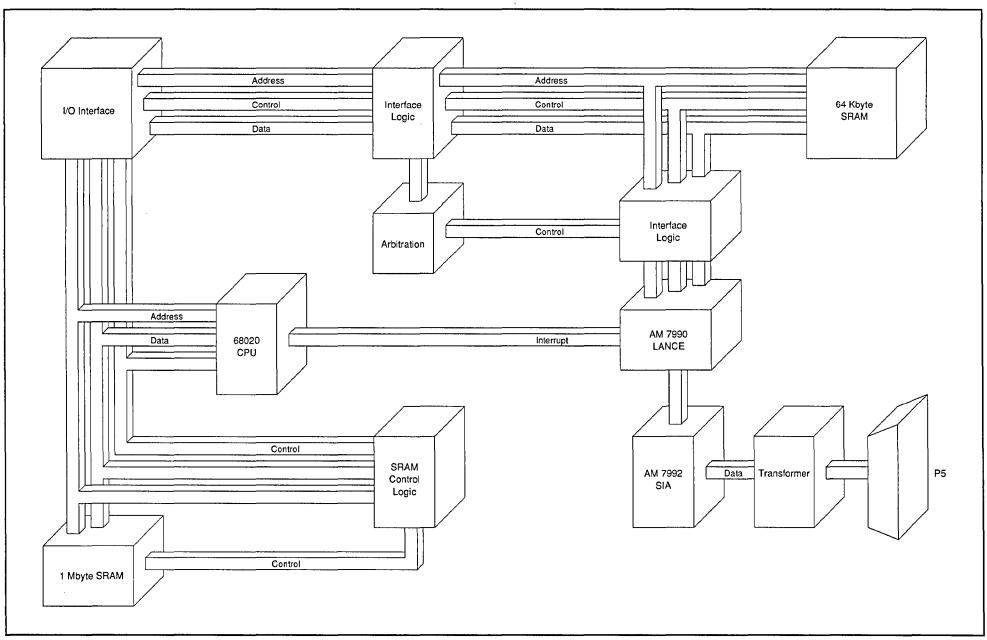
The chip set used provides conformance to the IEEE 802.3 Ethernet Interface Standard. This allows, with additional software, the support of higher level local area network communication protocols. The LAN functional module also provides a dedicated 64 Kbyte buffer for Ethernet data transfers. This buffer is a shared memory array, allowing access from both the AM7990 and from the local CPU. This 64-Kbyte closely coupled memory allows the Ethernet interface to function at full speed without causing CPU performance degradation. This is because the AM7990 can function independently, using its on-chip DMA controller, while the CPU operates unaffected in the board's main memory. This means that the CPU and the Ethernet controller can operate in parallel.

The Ethernet controller and associated support logic is only available on "E" board versions.

1.16 Benchmarks

	CPU-30ZA	CPU-30ZBE	Unit
Dhrystones	6172	6756	Dhryst./sec
Whetstones	1111	1428	KWhet./sec
Sieve	3.41	2.72	sec/100 iterations
DMA – Local	14.35	14.91	Mbyte/sec
DMA–VME	12.16	12.90	Mbyte/sec

Block Diagram of the Ethernet Module



2. The Memory Map

The memory map of the SYS68K/CPU-30BE/16 is listed in the following table:

Start Address	End Address	Type
00000000	00FFFFFF	Shared Memory, 16 Mbyte
01000000	F9FFFFFF	VMEbus, A32 : D32, D24, D16, D8
FA000000	FAFFFFFF	Message Broadcast Area
FB000000	FBFEFFFF	VMEbus, A24 : D32, D24, D16, D8
FBFF0000	FBFFFFFF	VMEbus, A16 : D32, D24, D16, D8
FC000000	FCFEFFFF	VMEbus, A24 : D16, D8
FCFF0000	FCFFFFFF	VMEbus, A16 : D16, D8
FD000000	FEEFFFFF	Reserved
FEF00000	FEF0FFFF	Ethernet SRAM
FEF10000	FEF7FFFF	Reserved
FEF80000	FEF80003	LAN Controller
FEF80004	FEFFFFFF	Reserved
FF000000	FF7FFFFF	System EPROM
FF800000	FFBFFFFF	Local I/O
FFC00000	FFCFFFFF	Local SRAM
FFD00000	FFDFFFFF	Registers of FGA-002
FFE00000	FFEFFFFF	Boot EPROM
FFF00000	FFFFFFFF	Reserved

3. The VMEbus Interface

The SYS68K/CPU-30 includes a full 32-bit VMEbus interface. The address modifier codes for A16, A24 and A32 addressing are fully supported in master mode. All slave accesses to the shared memory and to the two FMB channels have to be A32.

The gate array controls the access cycle to the DRAM and determines if an access is to be allowed (read/write protection). Read-Modify-Write cycles are fully supported to allow multiple CPU boards to be synchronized via the shared RAM.
By default VMEPROM disables the support for on-board RMW cycles from the VMEbus to the on-board memory to reduce the overhead for the access. The support for RMW cycles can easily be enabled by reprogramming the FGA-002.

These bus arbitration modes are supported:

RWD = Release When Done
ROR = Release On Request
RBCLR = Release On Bus Clear
RAT = Release After Timeout
RV = Release Voluntarily

In addition, a fair arbitration mechanism is implemented to allow access to the VMEbus by all masters in a heavily loaded system (Request on No Request-RNR).
Each of the listed modes is software-programmable inside the gate array. The bus request level of the SYS68K/CPU-30 is jumper-selectable (BR0-3*). The SYS68K/CPU-30 contains a DMA controller, which is able to access the VMEbus interface independent from the CPU.
A single level arbiter, a power monitor, a SYSRESET* generator and support for ACFAIL* and SYSFAIL* complete the VMEbus interface.

4. The Interrupt Structure

The gate array installed on the SYS68K/CPU-30 handles all local and VMEbus interrupts. Each interrupt request from the local bus through the SCSI and floppy disk controller, the DUSCC, RTC, the LAN controller and the two timers, as well as the gate array specific interrupt requests, are combined with the seven VMEbus IRQs.
Each IRQ source, including the VMEbus IRQs, can be programmed to interrupt the CPU on an individual programmable level (1 to 7). The gate array supplies the vector or initiates an interrupt vector fetch from the I/O device or from the VMEbus.
In addition to the local interrupts, the ACFAIL* and SYSFAIL* signals can be used to interrupt the CPU on a software-programmable level.

This results in a total of 42 individual IRQs, handled through the gate array on the CPU-30 board. The interrupt vectors supplied by the gate array have a basic vector and fixed increments for each source. The basic vector is software-programmable.

5. The Multi-Processor Mailboxes

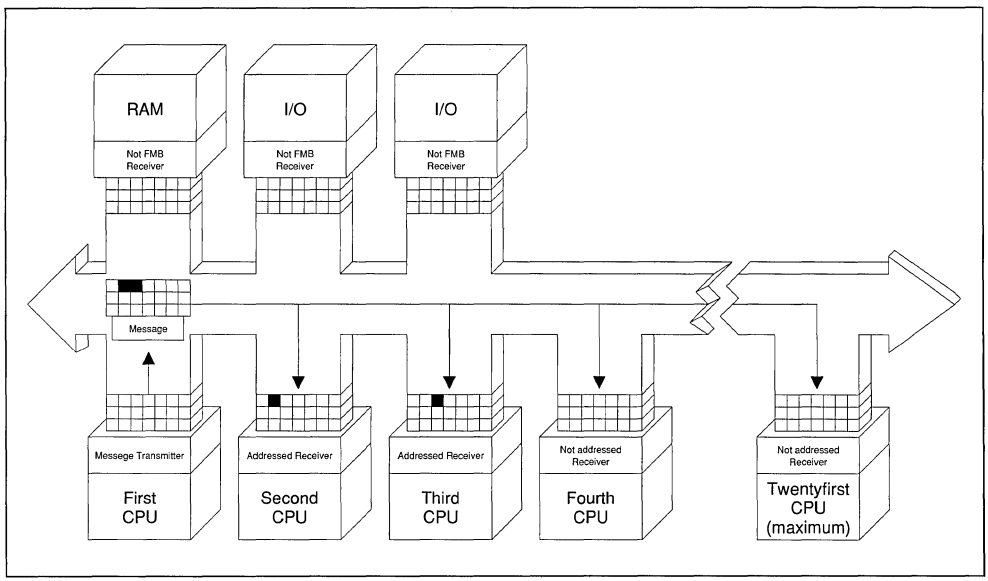
The SYS68K/CPU-30 includes eight multi-processor mailboxes. Each of these allows an interrupt to be forced to the local 68030 CPU. The interrupt level of each is software-programmable and an individual interrupt vector for each may be passed to the CPU.
This function allows the triggering of an interrupt on the SYS68K/CPU-30 from multiple masters on the VMEbus. The mailboxes are accessed via RMW access, thus allowing multiple masters on the VMEbus to share the same mailbox channel.

6. FORCE Message Broadcast

The FORCE Message Broadcast (FMB) is a fast and effective mechanism to communicate with and to synchronize up to 20 CPU boards in a VMEbus system in only one VMEbus write cycle. It offers a unique support feature for building multi-processing systems based on the VMEbus.

An FMB transfer is a standard VMEbus write cycle and complies fully to the IEEE 1014 Specification. Any VMEbus master may be a message transmitter. The transmitter decides which boards in the system should be addressed (one, two or up to twenty boards) and writes the message to a specific address.
All addressed boards receive the message at the same time and generate an interrupt request on a programmable level to their local microprocessor. This ensures that there is no time delay between the synchronization of different boards in the system. The ability to communicate with and synchronize multiple CPUs in the system by the FMB mechanism allows the VMEbus to be used in a wide range of application areas, particularly multi-processor environments.
Without the FMB mechanism, communication between and synchronisation of system boards has to be managed via the seven interrupt request lines. FMB reduces the massive time overhead normally needed to process the interrupt cycles to just one write cycle.
All FORCE VME/PLUS boards provide two fully independent message broadcast channels. Channel 0 stores 8-bit messages in an eight stage deep FIFO, channel 1 stores one 8-bit

Block Diagram of the FORCE Message Broadcast



message and can therefore be used for high priority messages.

13. Software

It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-30 Software Support

Operating System/Kernel	Vendor/Support
UNIX V.4 and V.4	FORCE COMPUTERS
PDOS	FORCE COMPUTERS
OS-9/9000	FORCE COMPUTERS/ MICROWARE
UNIFLEX	Contact FORCE for availability
VERSADOS	Contact FORCE for availability
VMEPROM	FORCE COMPUTERS
VxWORKS	FORCE COMPUTERS/ Wind River Systems
VRTX-32	READY SYSTEMS
pSOS	Software Components Group
ARTX	Contact FORCE for availability
Telesoft ADA	Contact FORCE for availability

As a courtesy, FORCE provides the user with the ability to immediately start a real time application by including VMEPROM on every CPU card, free of charge and free of licensing costs.
VMEPROM is an EPROM-based Real Time Multi-tasking Kernel/Monitor. The complete package resides in 256 Kbyte of EPROM and uses 32 Kbyte of RAM. VMEPROM fully supports all of the on-board I/O devices.
VMEPROM is composed of a highly sophisticated Real Time Kernel, which is based on the PDOS Real Time Kernel. A file manager supporting sequential, random and shared files is also included.
The user interface contains more than 60 commands perfectly suited for program debugging, host computer communications, as well as task and file management. It includes a powerful debugger, supporting line assembler/disassembler for the microprocessor.

Features of VMEPROM

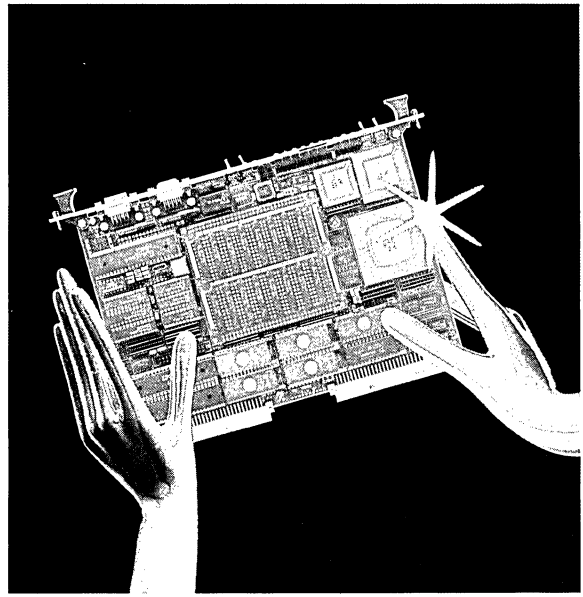
- Real Time Kernel supporting multi-tasking, up to 64 tasks
- File manager, supporting up to 64 open files at the same time
- Line assembler/disassembler with full support of all 680x0 instructions
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify
- S-record up/downloading from any port defined in the system
- Disk support for RAM disk, floppy and Winchester disks
- VMEPROM allows disk formatting and initialization
- Serial I/O support for up to two SIO-2 or ISIO-2 boards in the system; local serial I/O devices are also supported
- EPROM programming utility using the SYS68K/RR-2 board
- Full screen editor
- I/O re-direction to files or ports from the command line
- Over 100 system calls to the kernel

Specifications

Function		
CPU/FPCP		68030/68882
CPU and FPCP clock frequency on:	CPU-30ZA CPU-30ZBE, -30BE/16	20.0 MHz
Shared DRAM capacity with parity	CPU-30ZA, -30ZBE CPU-30BE/16	4 Mbyte 16 Mbyte
SRAM capacity with on-board battery back-up		32 Kbyte
No. of system EPROM sockets Data path		4 32-bit
Serial I/O interfaces (68562) RS232/422/RS485-compatible		4 4
Ethernet interface on CPU-30ZAE and CPU-30ZBE Ethernet SRAM		AM7990 64 Kbyte
Parallel I/O interface (68230)		12 lines
Real Time Clock with on-board battery back-up		72421
SCSI interface (87031)		Single-ended
Floppy Disk Interface (WD1772)		SA 460
24-bit timer with 5-bit prescaler 8-bit timer		2 1
VMEbus interface Shared memory access time from VMEbus (read/write)	A32, A24, A16 : D8, D16, D32, UAT, RMW A32 : D8, D16, D32, RMW	Master Slave 900 nsec typ
SYSCLK driver Mailbox interrupts		yes 8
FORCE Message Broadcast	FMB-FIFO 0 FMB-FIFO 1	8 byte 1 byte
VMEbus and local interrupt handler All sources can be routed to a software-programmable IRQ level Total number of IRQ sources		1 to 7 yes 42
RESET, ABORT switches		yes
VMEPROM firmware installed on all board versions		yes
Power requirements	+ 5 V min : max + 12 V min : max – 12 V min : max	5.2 A : 6.0 A 0.1 A : 0.3 A 0.1 A : 0.3 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)		0 to + 50 °C – 40 to + 85 °C 5 to 95 %
Board dimensions		234 × 160 mm : 9.2 × 6.3 in
No. of slots used		1

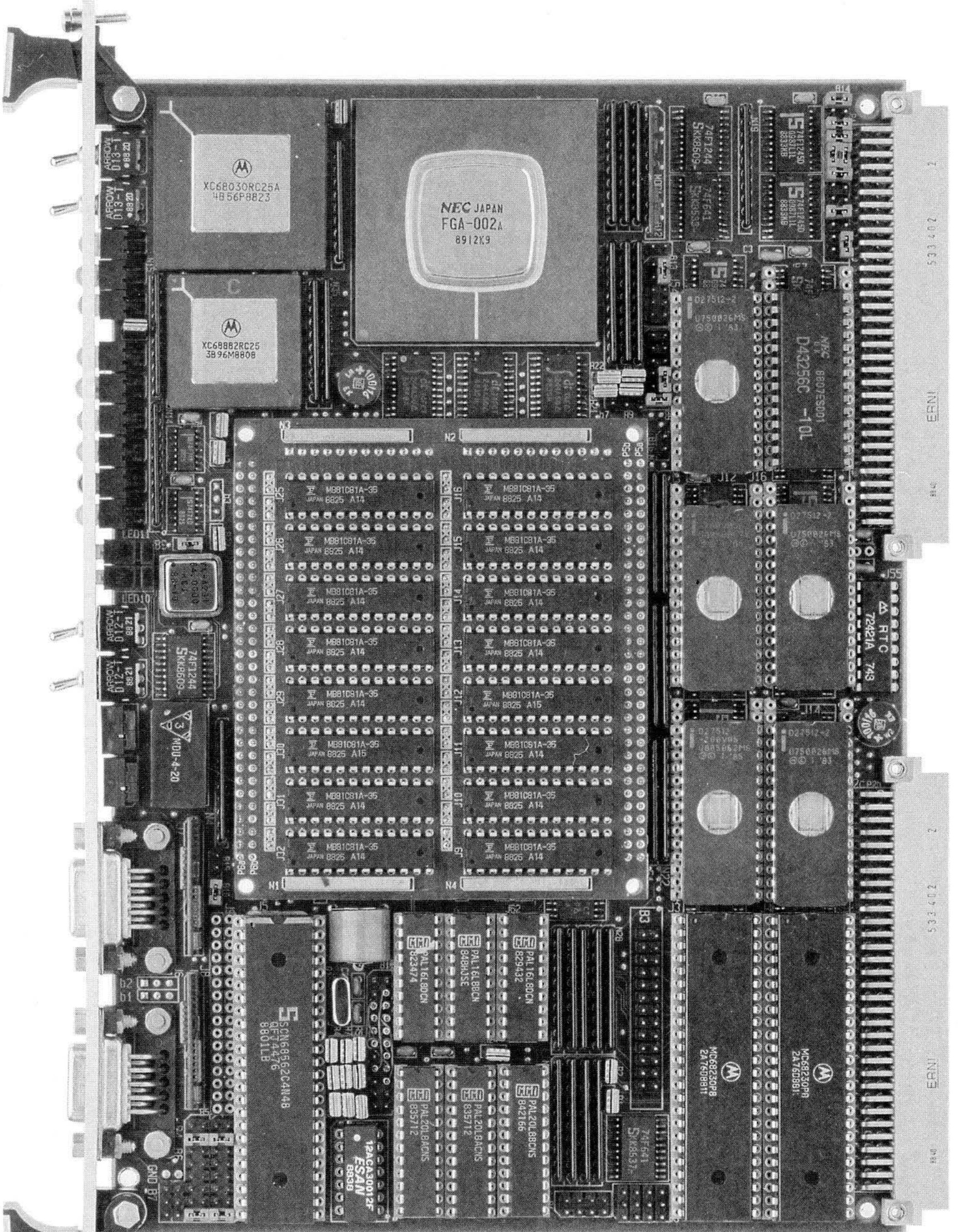
Ordering Information

SYS68K/CPU-30ZA Part No. 101302	20.0 MHz 68030 based CPU board with 68882 FPCP, DMA, 4 Mbyte shared memory, 4 serial I/O channels, SCSI and floppy disk interface, VMEPROM. Documentation included.
SYS68K/CPU-30ZBE Part No. 101305	25.0 MHz 68030 based CPU board with 68882 FPCP, DMA, 4 Mbyte shared memory, 4 serial I/O channels, SCSI and floppy disk interface, Ethernet, VMEPROM. Documentation included.
SYS68K/CPU-30BE/16 Part No. 101306	25.0 MHz 68030 based CPU board with 68882 FPCP, DMA, 16 Mbyte shared memory, 4 serial I/O channels, SCSI and floppy disk interface, Ethernet, VMEPROM. Documentation included.
SYS68K/IOBP-1 Part No. 700043	Back panel for the CPU-30 boards providing serial I/O, SCSI and floppy disk controller connectors.
SYS68K/VMEPROM/30/UP Part No. 145109	VMEPROM update service for the CPU-30 series.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM user's manual, excluding the SYS68K/CPU-30 description.
SYS68K/CPU-30/UM Part No. 800146	User's manual for the SYS68K/CPU-30 including VMEPROM and FGA-002 user's manual.



System 68000 VME
SYS68K/CPU-31

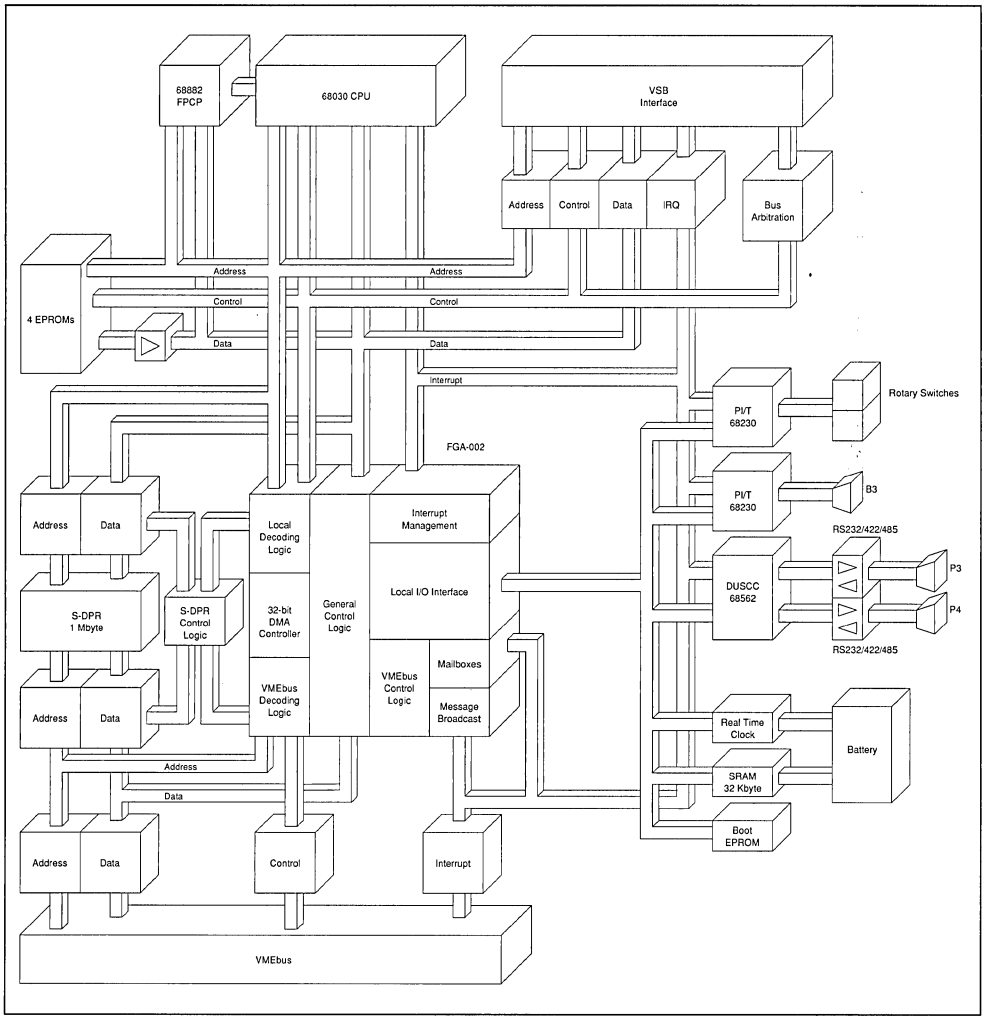
Multi-Processor 68030 based CPU Board with Synchronized Dual Ported RAM


XC68030RC25A
XC68882RC25
NEC JAPAN
FGA-002A
8912K9
D43256C -10L
RTC
72421A
MDU-4-20
ERNI

General Description

The SYS68K/CPU-31 is a 68030/68882 based CPU board providing 1 Mbyte of Synchronized Dual Ported RAM (S-DPR). A full 32-bit DMA controller, supporting data transfers to/from VMEbus memory as well as to/from local RAM is provided by the 281-pin FORCE Gate Array.
Serial communication is provided through two fully independent multi-protocol channels. A full 32-bit VSB interface including bus arbitration and interrupt handling is installed on all CPU-31 board versions. The VSB interface is fully supported by the 32-bit DMA controller inside the FGA-002. Additional features include up to 4 Mbyte EPROM capacity, up to 512 Kbyte SRAM and a Real Time Clock. VMEPROM, the Real Time Kernel, is installed by default. Two FORCE Message Broadcast channels and eight mailbox interrupts complete the board.

Block Diagram of the SYS68K/CPU-31



Features of the SYS68K/CPU-31

- 68030 CPU:
  20.0 MHz on CPU-31XA
  25.0 MHz on CPU-31XB
- 68882 FPCP:
  20.0 MHz on CPU-31XA
  25.0 MHz on CPU-31XB
- 32-bit high speed DMA controller for S-DPR/ VMEbus/VSB data transfers
- 1 Mbyte of constant zero wait state Synchronized Dual Ported RAM (S-DPR)
- FORCE Message Broadcast (FMB)
- Two serial I/O interfaces, RS232/RS422- and RS485-compatible
- 8-bit parallel interface with handshake
- Four system EPROM devices supporting 28- and 32-pin devices, using a 32-bit data path
- One boot EPROM for local booting and initialization of the I/O interface chips and the gate array
- Up to 512 Kbyte SRAM with battery back-up
- Real Time Clock with calendar and on-board battery back-up
- Two 24-bit timers with 5-bit prescaler
- One 8-bit timer
- All local I/O devices are able to interrupt the local CPU on a software-programmable level
- BERR handling fully under software control
- VSB master interface with serial arbiter:
  - A32: D8, D16, D32
- Full 32-bit VMEbus master/slave interface supporting the following data transfer types:
  - A32, A24, A16 : D8, D16, D32 – Master
  - A32, A24 : D8, D16, D32 – Slave
  - UAT, ADO and RMW cycles are also supported
- Single-level VMEbus arbiter
- SYSCLK driver
- VMEbus Interrupt Handler
- Support for ACFAIL* and SYSFAIL*
- Bus time-out counters for local and VMEbus accesses (15 µsec)
- VMEPROM, the Real Time Monitor with file manager and Real Time Kernel

1. Hardware Description

1.1 The 68030 CPU

The 68030 with its 32-bit address and data paths is installed on the CPU-31 board. The CPU includes a 256-byte instruction and a 256-byte data cache which significantly reduce the number of bus cycles needed for program execution.
The 68030 CPU can access the SRAM constantly without wait states. This allows the design to take full advantage of the throughput of the CPU. Communication with the local I/O interfaces, local SRAM and the VMEbus interface to the 68030 CPU is provided through a specially designed 281-pin gate array, called FGA-002. The EPROM area, the Floating Point Co-Processor and the S-DPR are directly connected to the CPU data and address bus interface. The clock frequency of the CPU is 20.0 MHz or 25.0 MHz.

1.2 The Floating Point Co-Processor

The SYS68K/CPU-31 is fitted with the enhanced 68882 Floating Point Co-Processor (FPCP). The clock frequencies of the CPU and the FPCP are identical. The FPCP conforms to the IEEE 754 Floating Point Standard. Communication between the CPU and the FPCP is built in silicon. An internal register set inside the FPCP of eight general purpose registers (80-bit wide) yields fast execution times.

Features of the FPCP

- Eight general purpose registers (80-bit : 64-bit mantissa, 15-bit exponent and 1 sign bit)
- 67-bit on-chip ALU
- 67-bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 Standard
- Full support of trigonometric and logarithmic functions such as:
  - Sine, cosine, tangent and cotangent
  - Hyperbolic functions
  - Logarithmic functions (4)
  - Square root and exponential functions (4)
- The 68882 is fully software-compatible to the 68881 FPCP

1.3 The Synchronized Dual Ported RAM

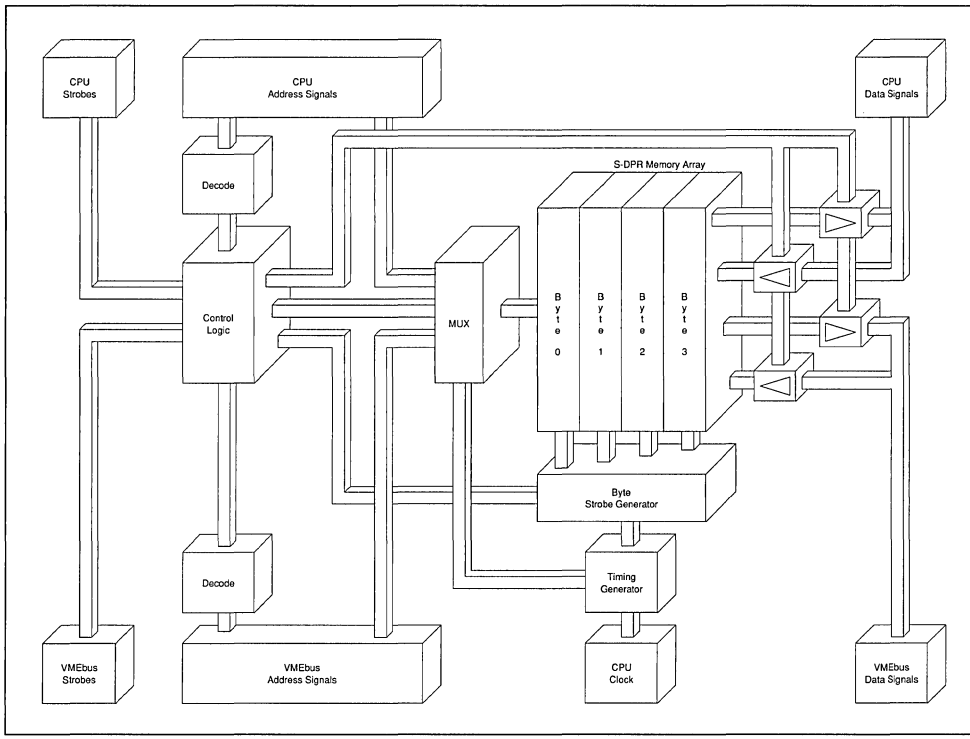
The SYS68K/CPU-31 contains a Synchronized Dual Ported static RAM design, S-DPR, which constantly supports zero wait state accesses of the local CPU. All accesses of the 68030 CPU to the S-DPR are immediately serviced while the VMEbus accesses the S-DPR between the 68030 access cycles.

This technique allows the SYS68K/CPU-31 to guarantee a constant runtime of all programs regardless of whether an access to the S-DPR from another VMEbus board is made or not. The bandwidth of the S-DPR for the local CPU is 40 Mbyte/sec plus 20 Mbyte/sec for the VMEbus. This results in a total S-DPR bandwidth of 60 Mbyte/sec. A detailed block diagram of the S-DPR control mechanism and a global timing are outlined below.

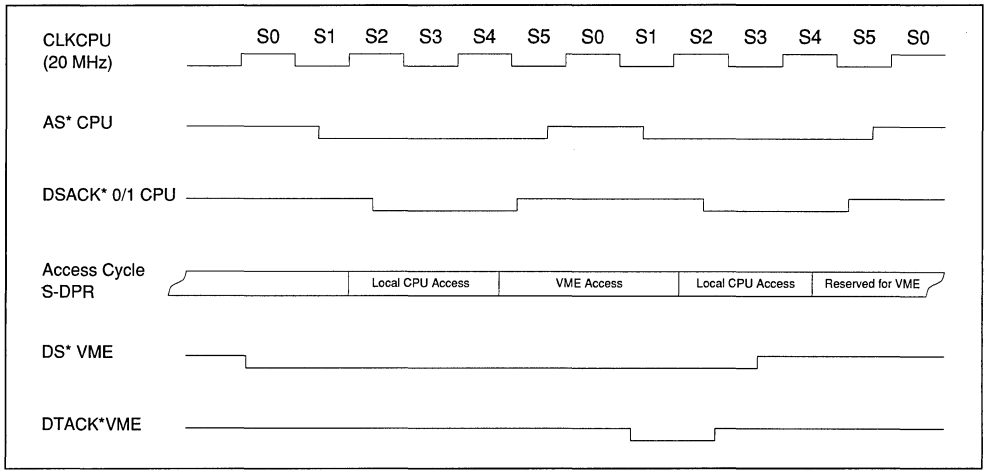
A key advantage of the S-DPR technology is that the SYS68K/CPU-31 can be used in critical real time applications without losing the real time capabilities through external accesses to the S-DPR. Alternative technologies such as the dual gated mechanism (the CPU is halted during VMEbus accesses), or the dual buffered function (alternate accesses to the DPR while one requestor is waiting until the RAM is unused) cannot guarantee constant zero wait state operation.

In non-S-DPR configurations the CPU normally waits or is halted during a VMEbus access cycle which results in a decreased CPU throughput. The SYS68K/CPU-31 combines the highest possible throughput (zero wait state accesses) with the dual ported RAM structure without decreasing performance at all CPU clock frequencies. The memory capacity is 1 Mbyte. The access address of the S-DPR from the VMEbus is fully software-programmable through the installed gate array within the 4 Gbyte address range of the processor. Address and address modifier decoding for the VMEbus

Block Diagram S-DPR



Timing Diagram of the S-DPR



accesses are software-programmable through the gate array.
The start and end access addresses are programmable in 4-Kbyte increments. The defined memory range can be write-protected in combination with the address modifier codes. For example, in supervisor mode, the memory can be read and written; in user mode, it can only be read. The read/write protection mechanism is fully under the user's software control.

1.4 The Local SRAM

A 32 Kbyte SRAM (battery back-up on-board) is installed on all SYS68K/CPU-31 board versions which supports data storage during power-down phases for up to one year.
The SRAM is directly connected to the FORCE Gate Array (FGA-002) I/O interface. Long word, word and byte transfers are automatically controlled via the gate array. Normal read/write operations to the SRAM are allowed, if the power is within the specification detected by a separate power sensor. The board is delivered with a 32 K x 8 SRAM. Higher density devices (e.g. future 512 K x 8 devices) or EEPROM devices may be inserted as the 32-pin socket allows the use of all JEDEC-compatible devices.

1.5 The System EPROMs

The SYS68K/CPU-31 contains four system EPROM sockets supporting four 28 and/or 32 pin EPROM devices. Maximum data throughput to the 68030 CPU is provided through the fast decoding logic and separate data transceivers.
The EPROM devices are read by the local 68030 CPU using 32-bit accesses which enables maximum performance.

Supported Device Types in the System EPROM Area:

Device	Pins	Organization	Total Memory Capacity
27512	28	64 K × 8	256 Kbyte
2710xx	32	128 K × 8	512 Kbyte
2720xx	32	256 K × 8	1 Mbyte
TBD	32	512 K × 8	2 Mbyte
TBD	32	1 M × 8	4 Mbyte

1.6 The Boot EPROM

The CPU-31 board contains, in addition to the four system EPROMs, a single boot EPROM to boot the local CPU, initialize all I/O devices and program the board-dependent functions of the gate array (FGA-002). All the presetting and initialization of the I/O devices are made using parameters programmed in the boot EPROM.

1.7 The DMA Controller

A high speed DMA controller is installed on the SYS68K/CPU-31. It features a maximum data transfer speed of up to 12.72 Mbyte/sec on the VMEbus and 21.47 Mbyte/sec to the S-DPR. DMA execution on the VMEbus is performed without any degradation of performance for the local CPU. This allows a program to be run while loading new data into the shared RAM or writing processed data to global RAM or I/O controller boards. If the data has to be stored or read to/from the shared RAM, the DMA controller requests bus mastership from the local CPU.
To increase the data throughput, the DMA controller operates using a 32-byte FIFO for internal data storage. The read and write operations are executed in eight cycles, 4 byte at a time, which results in eight read cycles followed by eight write cycles.
This feature significantly increases data throughput and functionality because the local CPU maintains the real time capabilities by being interruptable during DMA transfers.
This technology allows data transfers between the shared RAM and the VMEbus by first collecting data from the VMEbus, giving up bus mastership and then transferring the data to the shared RAM. A second VMEbus board can transfer data on the VMEbus while the DMA controller transfers the stored data to the shared RAM.
The following table shows the 68030 performance during the DMA data transfers:

Area 1		Area 2	CPU Operation	Note
VMEbus	⇔	VMEbus	100 %	–
VMEbus	⇔	S-DPR	60–70 %	1
VSB	⇔	VSB	10 %	2
VSB	⇔	S-DPR	10 %	2
VSB	⇔	VMEbus	50–60 %	1/2
S-DPR	⇔	S-DPR	10 %	–

Note 1: CPU operation depends on the transfer speed of the addressed VMEbus board.
Note 2: CPU operation depends on the transfer speed of the addressed VSB board.

The CPU can operate in parallel to the DMA controller data transfers because of the 32-byte FIFO and the structure of the SYS68K/CPU-31. This means that during DMA transfers, the CPU can access all local I/O devices, the EPROM area as well as the shared RAM.
When the CPU wants to access the VMEbus, it has to wait until the DMA controller has completed the transfers from its FIFO (max. eight transfers). Additionally, the DMA controller is connected to the VSB interface, allowing data transfer between the S-DPR and devices connected to VSB. The DMA controller supports aligned and unaligned data transfers. The internal control logic first aligns the data transfers to take full advantage of the 32-bit bus structure.

Register Set of the DMA Controller

8	Interrupt Control Normal Termination
8	Interrupt Control Error Termination
8	Source Attribute Register
8	Destination Attribute Register
8	General Control Register
8	Interrupt Status Normal Termination
8	Interrupt Status Error Termination
8	Run Control Register
8	Mode Status Register
32	Source Address
32	Destination Address
32	Transfer Count

1.8 The Local I/O Devices

The SYS68K/CPU-31 contains a gate array (FGA-002) which provides an 8-bit local I/O interface used to interconnect the CPU and the I/O devices. The Real Time Clock, serial I/O

controllers, the parallel I/O, control and status registers are connected to this local I/O interface.

1.9 The Serial I/O Interfaces

A Dual Universal Serial Communication Controller (DUSCC 68562) is installed on the CPU-31 to communicate to terminals, computers or other equipment.

Features of the DUSCC

- Dual full-duplex synchronous and asynchronous receiver and transmitter (programmable)
- Multi-protocol operation enabling support of bit- or character-oriented protocols. With additional software this allows the support of HDLC, SDLC, X.25, X.75, BISYNC, etc.
- Programmable data encoding formats: NRZ, NRZI, FM0, FM1, Manchester
- 4 character receiver/transmitter FIFOs
- Individual programmable baud rate for each receiver and transmitter supported by a digital phase locked loop
- Modem control signals for each channel: RTS, CTS, DCD

Serial I/O Signal Assignments

Pin	RS232	RS422
1	DCD	TXD-
2	RXD	RTS-
3	TXD	CTS+
4	DTR	RXD+
5	GND	RXD-
6	DSR	TXD+
7	RTS	RTS+
8	CTS	CTS-
9	GND	RXD-

Both serial I/O channels are routed to 9-pin D-sub connectors on the front panel. Both serial I/O channels are connected to RS232-compatible drivers/receivers. They can also be configured for RS422/485-compatibility.

The DUSCC can interrupt the local CPU on a software-programmable level (1 to 7). It is also possible to connect TxClk and RxClk to the 9-pin connectors via a jumper field. This is necessary for synchronous communication.

1.10 The Real Time Clock

A software-programmable Real Time Clock (RTC-72421) with on-board battery back-up is installed on the SYS68K/CPU-31 boards.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12 hr/24 hr clock switch-over
- Automatic leap year setting
- Interrupt masking
- C-MOS design provides low power consumption during power-down mode

The Real Time Clock is able to interrupt the local CPU on a level programmable through the gate array (1 to 7).

1.11 The Input/Output Ports

A total of two 8-bit input ports and one 12-bit input/output port (8-bit data 4-bit handshake) are available on the SYS68K/CPU-31. The first 8-bit input port is connected to the two 4-bit hex rotary switches provided on the front panel. These are available for user-dependent board and firmware configuration settings.

The second 8-bit input port allows the memory capacity of the shared memory to be read. Each SYS68K/CPU-31 board has three readable status bits describing the memory capacity. In addition, the CPU board type can be read via the remaining 5 bits. The 12-bit I/O port is routed to a 24-pin header which allows the connection of a flat cable. 8 bits are connected to the port A of a PI/T and can be used as inputs or outputs, the remaining 4 bits are connected to the handshake pins of the PI/T. This port can be used for parallel I/O applications such as a Centronics-compatible printer interface.

The remaining signals of the two PI/T 68230 devices are used for on-board control as well as for the four user LEDs on the front panel of the CPU-31.

1.12 The Timers

A total of three independent timers are available for the user. These timers offer maximum flexibility because each timer can be used to force an interrupt to the CPU on a software-programmable IRQ-level (1 to 7).
The first two timers each provide a 24-bit timer with an individual 5-bit prescaler. The third timer can also be used to generate interrupts to the CPU and the SYSFAIL* signal to the VMEbus. It can also be used to act as a watchdog.
This timer is an 8-bit timer with programmable source clock divider installed in the gate array (FGA-002). SYSFAIL* can be used in multi-processor systems to signal that one board has detected a failure. The watchdog timer needs to be reset periodically (software-programmable). Without such a reset a SYSFAIL* will be asserted on the VMEbus. All installed timers can be used as a watchdog timer or can generate interrupts on a periodical basis.

1.13 Benchmarks

	CPU-31XA	CPU-31XB	Unit
Dhrystones	6600	8064	Dhryst./sec
Whetstones	1111	1428.6	KWhet./sec
Sieve	3.42	2.73	sec/100 iterations
DMA–Local	18.85	21.47	Mbyte/sec
DMA–VME	8.96	12.72	Mbyte/sec

2. The VSB Interface

The SYS68K/CPU-31 board is delivered with a full 32-bit VSB master interface. Maximum data throughput is provided on the VSB interface, supporting 32 bits of data via the 4 Gbyte address range. The following data transfer types are supported:

- A32 : D8, D16, D32
- Unaligned transfers
- Address only cycles
- Read-Modify-Write transfers

The VSB interface allows the system integrator to build contiguous local memory beyond the local SRAM. The local control logic provides an access cycle to the VSB interface before addressing the VMEbus. This technique allows an increase of the overall throughput of systems using the secondary bus. If the VSB interface is not required, a jumper allows it to be disabled and forces VMEbus accesses if an off-board access cycle is decoded. The serial arbiter and an IHP Interrupt Handler complete the VSB interface.

3. The VMEbus Interface

The SYS68K/CPU-31 includes a full 32-bit VMEbus interface. The address modifier codes for A16, A24 and A32 addressing are fully supported in master mode. All slave accesses to the shared memory may be A32 or A24 and the two FMB channels have to be A32.
The gate array controls the access cycle to the S-DPR and determines if an access is to be allowed (read/write protection). Read-Modify-Write cycles are fully supported to allow multiple CPU boards to be synchronized via the shared RAM.
By default VMEPROM disables the support for on-board RMW cycles from the VMEbus to the on-board memory to reduce the overhead for accesses. The support for RMW cycles can easily be enabled by reprogramming the FGA-002. These bus arbitration modes are supported:

REC = Release Every Cycle
RWD = Release When Done
ROR = Release On Request
RBCLR = Release On Bus Clear
RV = Release Voluntarily

In addition, a fair arbitration mechanism is implemented to allow access to the VMEbus by all masters in a heavily loaded system (Request on No Request-RNR).
Each of the listed modes is software-programmable inside the gate array. The bus request level of the SYS68K/CPU-31 is jumper-selectable (BR0-3*).
The SYS68K/CPU-31 contains a DMA controller, which is able to access the VMEbus interface independent from the CPU. A single level arbiter, a power monitor, SYSCLK, a SYSRESET* generator and support for ACFAIL* and SYSFAIL* complete the VMEbus interface.

4. The Memory Map

The memory map of the SYS68K/CPU-31 is listed in the following table:

Start Address	End Address	Type
00000000	000FFFFF	S-DPR, 1 Mbyte
00100000	F9FFFFFF	VMEbus, A32 : D32, D16, D8 or VSB*, A32 : D32, D16, D8
FA000000	FAFFFFFF	Message Broadcast Area
FB000000	FBFEFFFF	VMEbus, A24 : D32, D24, D16, D8
FBFF0000	FBFFFFFF	VMEbus, A16 : D32, D24, D16, D8
FC000000	FCFEFFFF	VMEbus, A24 : D16, D8
FCFF0000	FCFFFFFF	VMEbus, A16 : D16, D8
FD000000	FEFFFFFF	VSB*, A32 : D32, D16, D8
FF000000	FF7FFFFF	Sytem EPROM
FF800000	FFBFFFFF	Local I/O
FFC00000	FFCFFFFF	Local SRAM
FFD00000	FFDFFFFF	Registers of FGA-002
FFE00000	FFEFFFFF	Boot EPROM
FFF00000	FFFFFFFF	Reserved

* Note: VSB can be accessed either overlaid or memory mapped.

5. The Interrupt Structure

The gate array installed on the SYS68K/CPU-31 handles all local and VMEbus interrupts. Each interrupt request from the local bus through the DUSCC, RTC and the two timers, as well as the gate array specific interrupt requests, are combined with the seven VMEbus IRQs and the VSB IRQ.

Each IRQ source, including the VMEbus IRQs, can be programmed to interrupt the CPU on an individual programmable level (1 to 7). The gate array supplies the vector, or initiates an interrupt vector fetch from the I/O device or from the VMEbus. In addition to the local interrupts, the ACFAIL* and SYSFAIL* signals can be used to interrupt the CPU on a software-programmable level. This results in a total of 40 individual IRQs, handled through the gate array on the CPU-31 board. The interrupt vectors supplied by the gate array have a basic vector and fixed increments for each source. The basic vector is software-programmable.

6. The Multi-Processor Mailboxes

The SYS68K/CPU-31 includes eight multi-processor mailboxes. Every mailbox allows an interrupt to be forced to the local 68030 CPU. All interrupt levels are software-programmable and an individual interrupt vector for each level may be passed to the CPU.

This function allows the triggering of an interrupt on the SYS68K/CPU-31 from multiple masters on the VMEbus. The mailboxes are accessed via RMW access, thus allowing multiple masters on the VMEbus to share the same mailbox channel.

7. FORCE Message Broadcast

The FORCE Message Broadcast (FMB) is a fast and effective mechanism to communicate with and to synchronize up to 20 CPU boards in a VMEbus system in only one VMEbus write cycle. It offers a unique support feature for building multi-processing systems based on the VMEbus. An FMB transfer is a standard VMEbus write cycle and complies fully to the IEEE 1014 Specification. Any VMEbus master may be a message transmitter. The transmitter decides which boards in the system should be addressed (one, two or up to twenty boards) and writes the message to a specific address.

All addressed boards receive the message at the same time and generate an interrupt request on a programmable level to their local microprocessor. This ensures that there is no time delay between the synchronization of different boards in the system. The ability to communicate with and synchronize multiple CPUs in the system by the FMB mechanism allows the VMEbus to be used in a wide range of application areas, particularly multi-processor environments.

Without the FMB mechanism, communication between and synchronisation of system boards

has to be managed via the seven interrupt request lines. FMB reduces the massive time overhead normally needed to process the interrupt cycles to just one write cycle.
All FORCE VME/PLUS boards provide two fully independent message broadcast channels. Channel 0 stores 8-bit messages in an eight stage deep FIFO, channel 1 stores one 8-bit message and can therefore be used for high priority messages.

8. Software

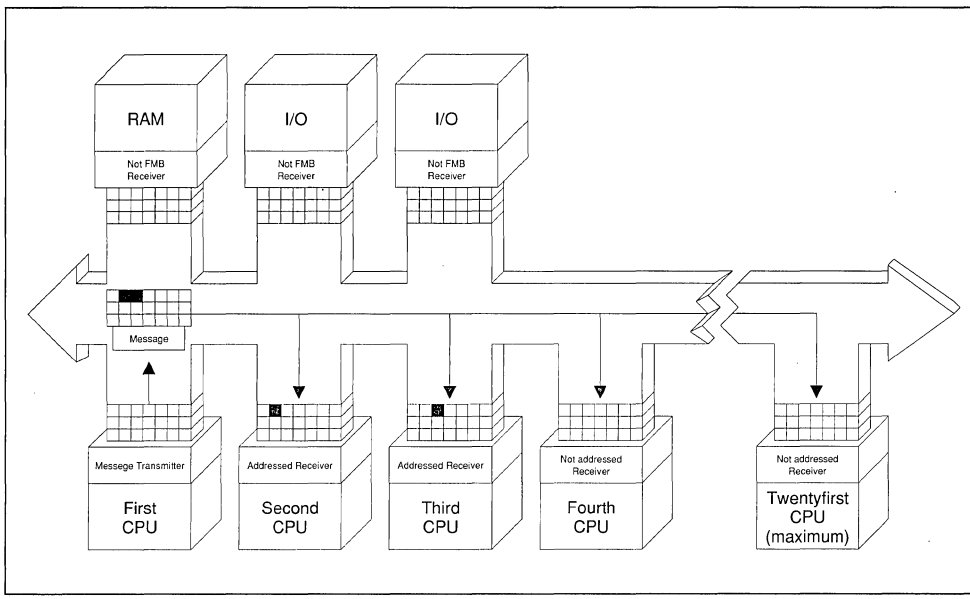
It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-31 Software Support

Operating System/Kernel	Vendor/Support
UNIX V.3/V.4	Contact FORCE for availability
PDOS	FORCE COMPUTERS
OS-9/9000	Contact FORCE for availability
VMEPROM	FORCE COMPUTERS
VxWORKS	Contact FORCE for availability
VRTX-32	READY SYSTEMS
pSOS	Contact FORCE for availability
ARTX	Contact FORCE for availability
Telesoft ADA	Telesoft

As a courtesy, FORCE provides the user with the ability to immediately start a real time application by including VMEPROM on every CPU card, free of charge and free of licensing costs.
VMEPROM is an EPROM-based Real Time Multi-tasking Kernel/Monitor. The complete package resides in 256 Kbyte of EPROM and uses 32 Kbyte of RAM. VMEPROM fully supports all of the on-board I/O devices.

Block Diagram of the FORCE Message Broadcast



VMEPROM is composed of a highly sophisticated Real Time Kernel, which is based on the PDOS Real Time Kernel. A file manager supporting sequential, random and shared files is also included.
The user interface contains more than 60 commands perfectly suited for program debugging, host computer communications, as well as task and file management. It includes a powerful debugger, supporting line assembler/disassembler for the microprocessor.

Features of VMEPROM

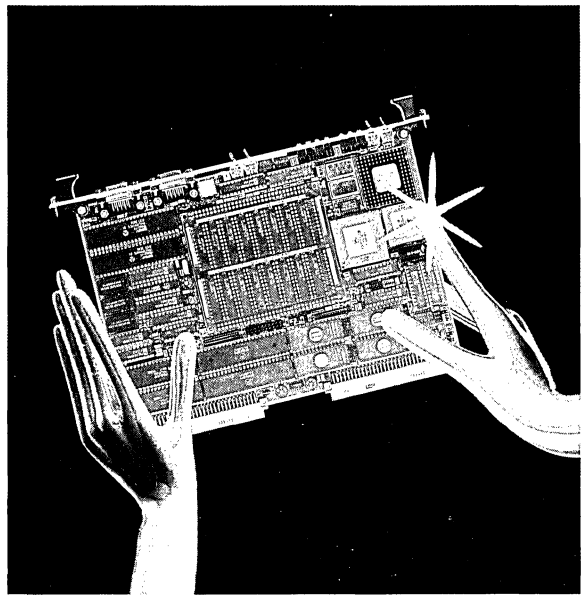
- Real Time Kernel supporting multi-tasking, up to 64 tasks
- File manager, supporting up to 64 open files at the same time
- Line assembler/disassembler with full support of all 680x0 instructions
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify
- S-record up/downloading from any port defined in the system
- Disk support for RAM disk, floppy and Winchester disks
- VMEPROM allows disk formatting and initialization
- Serial I/O support for up to two SIO-2 or ISIO-2 boards in the system; local serial I/O devices are also supported
- EPROM programming utility using the SYS68K/RR-2 board
- Full screen editor
- I/O re-direction to files or ports from the command line
- Over 100 system calls to the kernel

Specifications

Function	
CPU/FPCP	68030/68882
CPU and FPCP clock frequency on: CPU-31XA CPU-31XB	20.0 MHz 25.0 MHz
S-DPR capacity	1 Mbyte
SRAM capacity with on-board battery back-up	32 Kbyte
No. of system EPROM sockets Data path	4 32-bit
Serial I/O interface (68562) RS232/422-compatible	2 2
Parallel I/O interface (68230)	12 lines
Real Time Clock with on-board battery back-up	72421
24-bit timer with 5-bit prescaler 8-bit timer	2 1
VSB Master Interface A32 : D8, D16, D32, UAT, RMW Bus Arbiter Interrupt Handler	yes yes serial IHP
VMEbus interface A32, A24, A16 : D8, D16, D32, UAT, RMW, ADO A32, A24: D8, D16, D32, UAT, RMW S-DPR access time (typ) from VMEbus (read/write)	Master Slave Typ: 420 ns
SYSCLK driver Mailbox interrupts	yes 8
FORCE Message Broadcast FMB-FIFO 0 FMB-FIFO 1	8 byte 1 byte
VMEbus and local interrupt handler All sources can be routed to a software-programmable IRQ level Total number of IRQ sources	1 to 7 yes 40
RESET, ABORT, CACHE and RUN/HALT switches	yes
VMEPROM firmware installed on all board versions	yes
Power requirements + 5 V min : max + 12 V min : max – 12 V min : max	5.2 A : 7.3 A 0.1 A : 0.2 A 0.1 A : 0.2 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)	0 to + 50 °C – 40 to + 85 °C 5 to 95 %
Board dimensions	234 × 160 mm : 9.2 × 6.3 in
No. of slots used	1

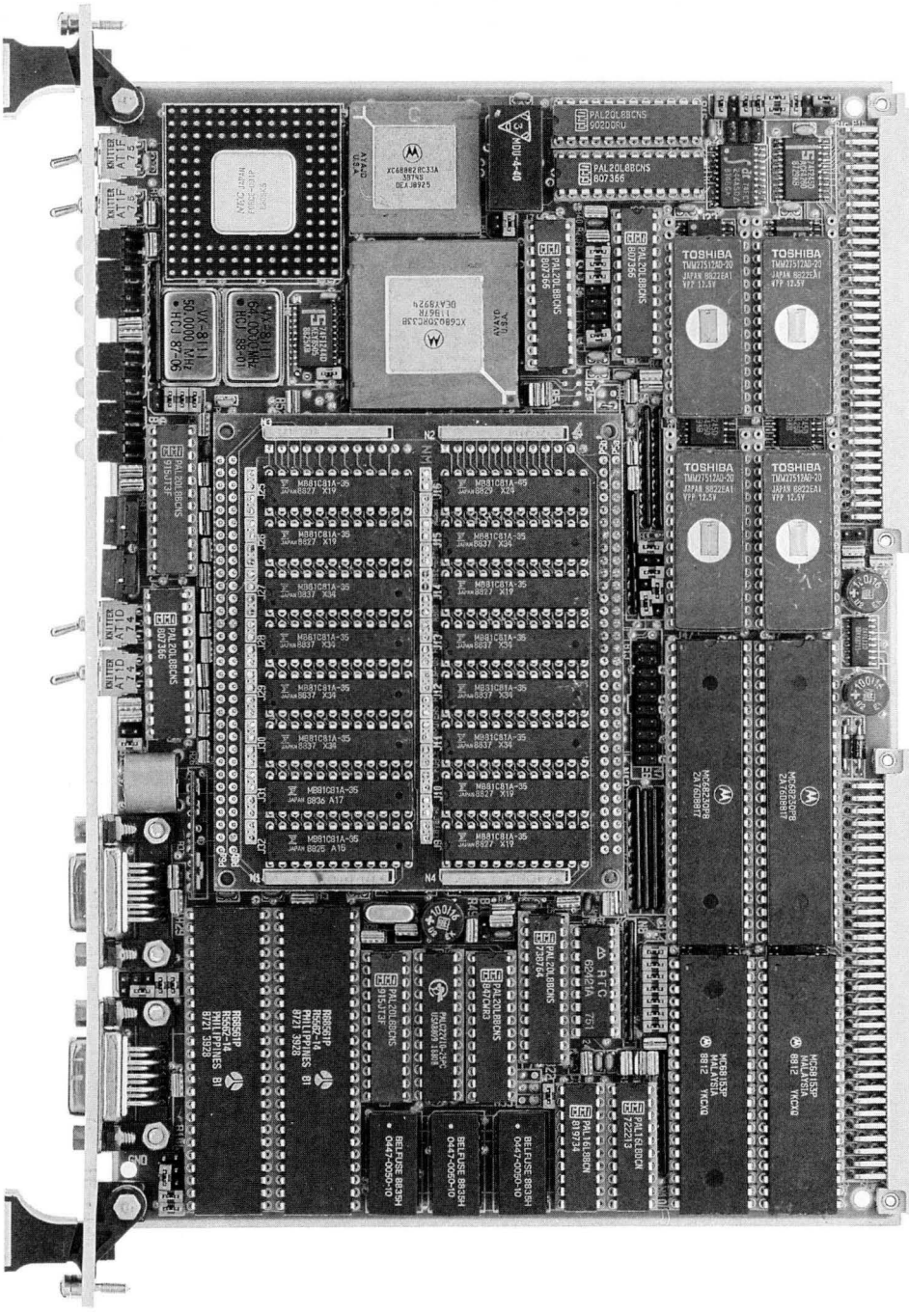
Ordering Information

SYS68K/CPU-31XA Part No. 101312	20.0 MHz 68030 based CPU board with 68882 FPCP, DMA, 1 Mbyte S-DPR, 2 serial channels, VSB, VMEPROM. Documentation included.
SYS68K/CPU-31XB Part No. 101314	25.0 MHz 68030 based CPU board with 68882 FPCP, DMA, 1 Mbyte S-DPR, 2 serial channels, VSB, VMEPROM. Documentation included.
SYS68K/CPU-31/UM Part No. 800147	CPU-31 user's manual including VMEPROM manual and FGA-002 manual.
SYS68K/VMEPROM/CPU-31/UP Part No. 145115	VMEPROM update service for the CPU-31 series.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM user's manual, excluding the SYS68K/CPU-31 description.



System 68000 VME
SYS68K/CPU-32

High Performance 68030 CPU with VSB Interface

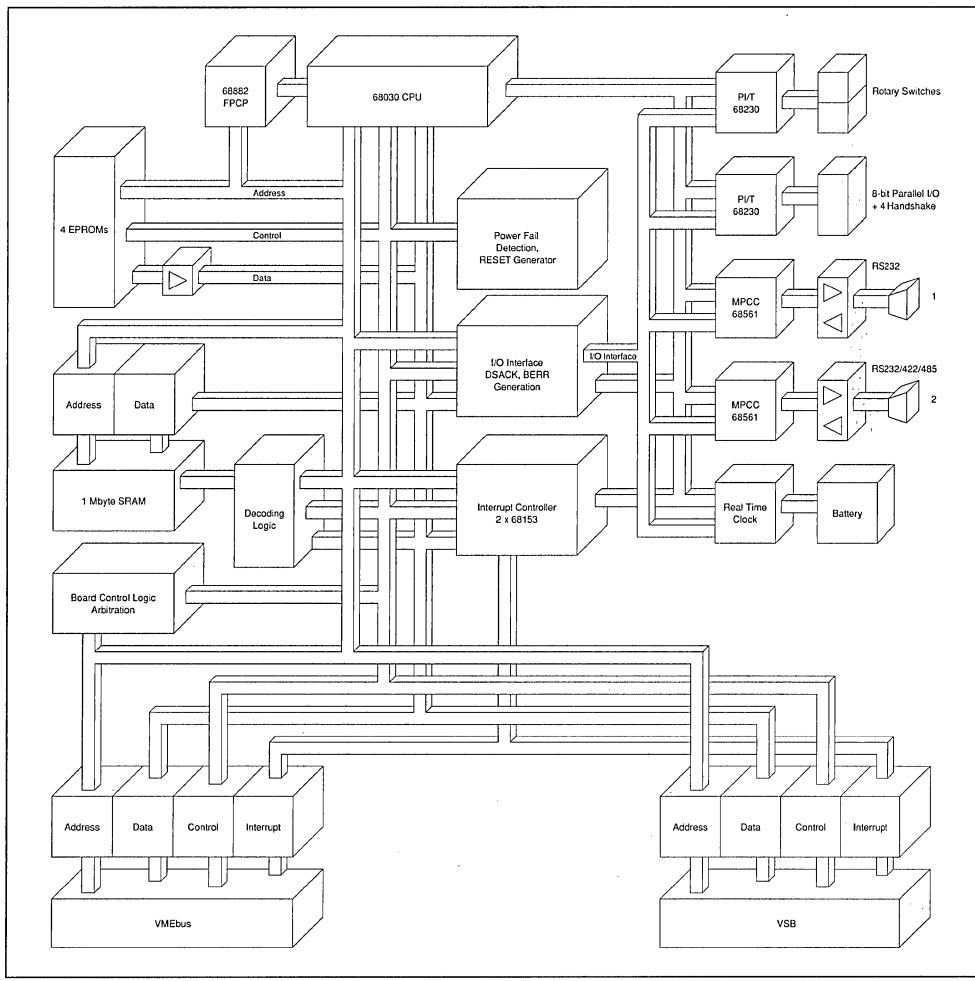


General Description

The SYS68K/CPU-32 is an ultra high speed CPU board using a 68030 with a clock frequency of up to 30 MHz. The SYS68K/CPU-32 is software-compatible to the SYS68K/CPU-29 board. SRAM with a capacity of 1 Mbyte can be accessed from the CPU (30 MHz clock frequency) without the insertion of wait states for all read and write cycles. A full 32-bit VSB interface including bus arbitration and interrupt handling is installed on all CPU-32 board versions. Two serial I/O interfaces (one RS232-compatible and one RS232/RS422/RS485-compatible) providing support for asynchronous data transfers are implemented on the board.

The EPROM area consists of four devices supporting the 28- and 32-pin JEDEC Standard which provides a maximum capacity of 4 Mbyte. Two fully independent 24-bit timers, a Real Time Clock with on-board battery back-up and the full 32-bit VMEbus master interface complete the board. In addition, VMEPROM, the PDOS-compatible multi-user Real Time Kernel/Monitor, is installed on all SYS68K/CPU-32 boards.

Block Diagram of the SYS68K/CPU-32



Features of the SYS68K/CPU-32

- 68030 CPU:
  25.0 MHz on CPU-32XB
  30.0 MHz on CPU-32XC
- 68882 FPCP:
  25.0 MHz on CPU-32XB
  30.0 MHz on CPU-32XC
- 1 Mbyte of constant zero wait state static RAM
- One 8-bit parallel interface with handshake
- Local interrupt management using 68153
- Local control and timers using 68230 (2)
- Two serial I/O interfaces, one RS232-compatible and one RS232/RS422/RS485-compatible
- Four EPROM sockets (28- or 32-pin JEDEC-compatible) providing a 32-bit data path
- VSB master interface (full 32-bit) with serial arbiter:
  – A32 : D8, D16, D32
- VMEbus interface (full 32-bit) with single level arbiter:
  – A32, A24, A16 : D8, D16, D32
- Bus timer
- Power monitor
- SYSRESET* generator
- RUN/HALT, CACHE and ABORT switches
- Status indication LEDs
- Two hex rotary switches
- VMEPROM installed

1. Hardware Description

1.1 The 68030 CPU

The 68030 CPU with its 32-bit address and data paths is installed on the SYS68K/CPU-32 board. The CPU includes a 256 byte instruction and data cache which significantly reduce the number of bus cycles needed for program fetches. A CACHE switch on the front panel allows the user to enable or disable the on-chip cache.
On some board versions the 68030 CPU accesses the SRAM without the insertion of wait states. This allows the design to take full advantage of the throughput of the CPU. The EPROM area, the Floating Point Co-Processor, the SRAM and the VSB interface are directly connected to the CPU data and address bus interface (as shown in the block diagram of the CPU-32).
The clock frequency of the CPU ranges from 25.0 MHz to 30 MHz.

1.2 The Floating Point Co-Processor

The SYS68K/CPU-32 is fitted with the enhanced 68882 Floating Point Co-Processor (FPCP). The clock frequencies of the CPU and the FPCP are identical. The FPCP conforms to the IEEE 754 Floating Point Standard.
Easy floating point operation control to the co-processor is provided by the built-in inter-communication between the CPU and the FPCP. An internal register set inside the FPCP of eight general purpose registers (80-bit wide) yields fast execution times.

Features of the FPCP

- Eight general purpose registers (80-bit : 64-bit mantissa, 15-bit exponent and 1 sign bit)
- 67-bit on-chip ALU
- 67-bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 Standard
- Full support of trigonometric and logarithmic functions such as:
  – Sine, cosine, tangent and cotangent
  – Hyperbolic functions
  – Logarithmic functions (4)
  – Square root and exponential functions (4)
- The 68882 is software-compatible to the 68881 FPCP

1.3 The SRAM

The SYS68K/CPU-32 contains high speed static RAM offering constant no wait state access for CPU access cycles. The memory bandwidth of the SYS68K/CPU-32 reaches 40 Mbyte/sec in the 30 MHz version without any need for refresh because SRAMs are used.

The following table lists the CPU board type and wait states for SRAM accesses:

Board Type	CPU Clock Frequency	SRAM Capacity	No. of Wait States
CPU-32XB	25.0 MHz	1 Mbyte	0
CPU-32XC	30.0 MHz	1 Mbyte	0

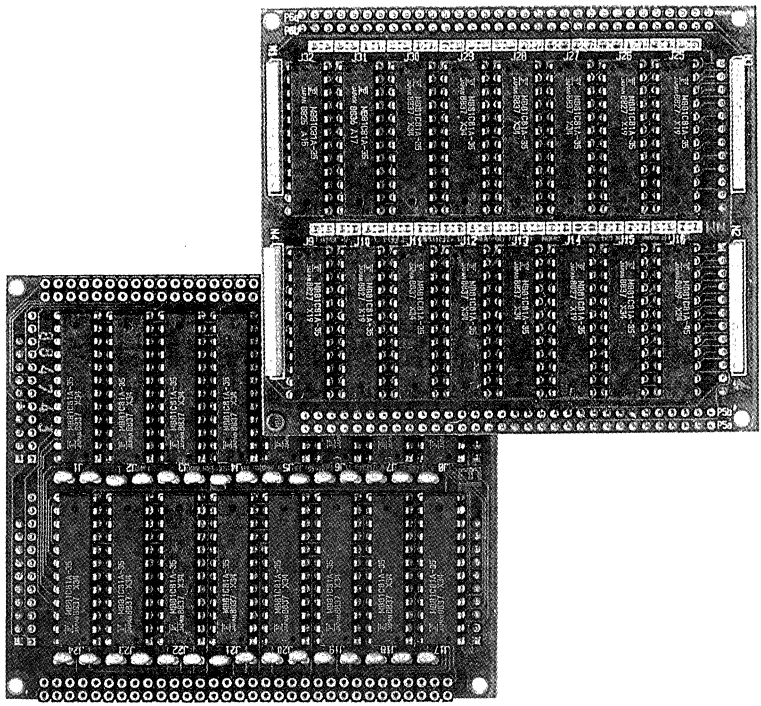
1.4 The EPROM Area

The SYS68K/CPU-32 contains four system EPROM sockets supporting 28- or 32-pin EPROM devices. Maximum data throughput to the 68030 CPU is provided through the fast decoding logic and separate data transceivers supporting one wait state operation, when 100 nsec devices are used. The following table lists the supported device types and the memory capacity.

Supported Device Types in the User EPROM Area:

Device Type	Pins	Organization	Total Memory Capacity
2764	28	8 K × 8	32 Kbyte
27128	28	16 K × 8	64 Kbyte
27256	28	32 K × 8	28 Kbyte
27512	28	64 K × 8	256 Kbyte
2710xx	32	128 K × 8	512 Kbyte
2720xx	32	256 K × 8	1 Mbyte
TBD	32	512 K × 8	2 Mbyte
TBD	32	1 M × 8	4 Mbyte

Picture of the Memory Module



1.5 The Serial I/O Channels

The SYS68K/CPU-32 contains two Multi-Protocol Communication Controllers (MPCC 68561) which include the following protocol features:

- Character-oriented protocols
- CRC check selectable
- 8-character receiver and transmit buffer
- Software-programmable baud rate
- Data rate of up to 38,400 baud

The two serial interfaces are connected to 9-pin D-Sub connectors on the front panel of the board. One interface is RS232-compatible only, the other interface is RS232 and can be easily be reconfigured to be RS422/RS485-compatible by exchanging the hybrid module supplied with the board.
Each MPCC is able to interrupt the local CPU on a software-programmable level. The interrupt vector is also software-programmable.
The following table shows the RS232 and RS422 pin assignment for the connectors on the front panel:

Pin	MPCC1	MPCC2	
	RS232	RS232	RS422/485
1	DCD	DCD	TXD-
2	RXD	RXD	RTS-
3	TXD	TXD	CTS+
4	DTR	DTR	RXD+
5	GND	GND	RXD-
6	DSR	DSR	TXD+
7	RTS	RTS	RTS+
8	CTS	CTS	CTS-
9	GND	GND	RXD-

1.6 The Local Control Devices

The SYS68K/CPU-32 contains two independent Parallel Interface and Timer devices (PI/T 68230) for local control and status display.
The clock frequency of each PI/T is 8.064 MHz. Eight control bits can be read via the PI/T port A. These control bits can be set via two HEX rotary switches available on the front panel for manipulation. In addition, an 8-bit parallel port with two handshake signals is available on the second PI/T. This parallel port can be configured to support parallel I/O for industrial applications or parallel printers.
The PI/T also allows to program the bus release functions such as:

REC = Release Every Cycle
ROR = Release On Request
RBCLR = Release On Bus Clear
RAT = Release After Timeout

In addition, the board type (CPU-32) and the installed memory capacity can be read via a PI/T. The two fully independent 24-bit timers with their 5-bit prescalers can be used to interrupt the local CPU on a software-programmable level. The interrupt vector is also software-programmable inside a Bus Interrupter Module (68153). All seven interrupt request levels of the CPU can be separately enabled or disabled via port B of the first PI/T.
One additional signal is used to enable/disable all VMEbus interrupts. For example, this allows the user to disable all interrupts on a certain IRQ level while debugging the application software. The SYSFAIL* and ACFAIL* signals of the VMEbus are connected to the first PI/T to interrupt the local CPU (if enabled) or to monitor the status of these signals.

1.7 The Real Time Clock

A software-programmable Real Time Clock (RTC-72421) with on-board battery back-up is installed on the SYS68K/CPU-32 boards. The features of the Real Time Clock are listed below.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12 hr/24 hr clock switchover
- Automatic leap year setting
- Interrupt masking
- C-MOS design provides low power consumption during power down mode

The Real Time Clock is able to interrupt the local CPU on a software-programmable level (1 to 7).

1.8 The Local Interrupt Sources

Two Bus Interrupter Modules (BIM 68153) are in-stalled on the SYS68K/CPU-32 to manage all the local interrupts. Each local interrupt source can be routed to one of the seven different IRQ levels of the CPU. The interrupt vector is also software-programmable.

Local Interrupt Sources:

- Test Switch
- MPCC 1
- MPCC 2
- PI/T 1 Timer
- PI/T 2 Timer
- RTC
- VSB-IRQ
- ACFAIL*
- SYSFAIL*

1.9 Benchmarks

	CPU-32XB	CPU-32XC	Unit
Dhrystones	8064	9433	Dhryst./sec
Whetstones	1428	1667	KWhet./sec
Sieve	2.73	2.26	sec/100 iterations

2. The VSB Interface

The SYS68K/CPU-32 board is delivered with a full 32-bit VSB master interface.
Maximum data throughput is provided on the VSB interface, supporting 32-bits of data via the 4 Gbyte address range. The following data transfer types are supported:

- A32 : D8, D16, D32
- Unaligned transfers
- Address only cycles
- Read-Modify-Write transfers

The VSB interface allows the system integrator to build contiguous local memory beyond the local SRAM. The local control logic provides an access cycle to the VSB interface before addressing the VMEbus. This technique allows an increase of the overall throughput of systems using the secondary bus. If the VSB interface is not required, a jumper allows it to be disabled and forces VMEbus accesses, if no on-board access cycle is decoded.
The serial arbiter and an IHP Interrupt Handler complete the VSB interface.

3. The VMEbus Interface

The SYS68K/CPU-32 includes a full 32-bit VMEbus interface, thereby taking maximum advantage of the VMEbus specification.
The address modifier codes for A16, A24 and A32 addressing are fully supported.

Supported data transfer types:

Transfer Type	D31-24	D23-16	D15-8	D7-0
Byte				x
			x	
Word			x	x
Long Word	x	x	x	x
Unaligned Transfers	x	x	x	
		x	x	
		x	x	x
Read Modify Write				x
			x	x
	x	x	x	x

The SYS68K/CPU-32 includes the following bus release modes:

REC = Release Every Cycle
ROR = Release On Request
RBCLR = Release On Bus Clear
RAT = Release After Timeout

The bus request level of the SYS68K/CPU-32 is jumper-selectable (BR0-3*). A single level arbiter, a power monitor, a SYSRESET* generator and support for ACFAIL* and SYSFAIL* complete the VMEbus interface.

4. Software

It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest

level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-32 Software Support

Operating System/Kernel	Vendor/Support
UNIX V.3	FORCE COMPUTERS
PDOS	FORCE COMPUTERS
OS-9/9000	Contact FORCE for availability
VMEPROM	FORCE COMPUTERS
VxWORKS	FORCE COMPUTERS/ Wind River Systems
VRTX-32	READY SYSTEMS
pSOS	Software Components Group
ARTX	Contact FORCE for availability
Telesoft ADA	Telesoft

As a courtesy, FORCE provides the user with the ability to immediately start a real time application by including VMEPROM on every CPU card, free of charge and free of licensing costs.
VMEPROM is an EPROM-based Real Time Multi-tasking Kernel/Monitor. The complete package resides in 256 Kbyte of EPROM and uses 32 Kbyte of RAM. VMEPROM fully supports all of the on-board I/O devices.
VMEPROM is composed of a highly sophisticated Real Time Kernel, which is based on the PDOS Real Time Kernel. A file manager supporting sequential, random and shared files is also included.
The user interface contains more than 60 commands perfectly suited for program debugging, host computer communications, as well as task and file management. It includes a powerful debugger, supporting line assembler/disassembler for the microprocessor.

Features of VMEPROM

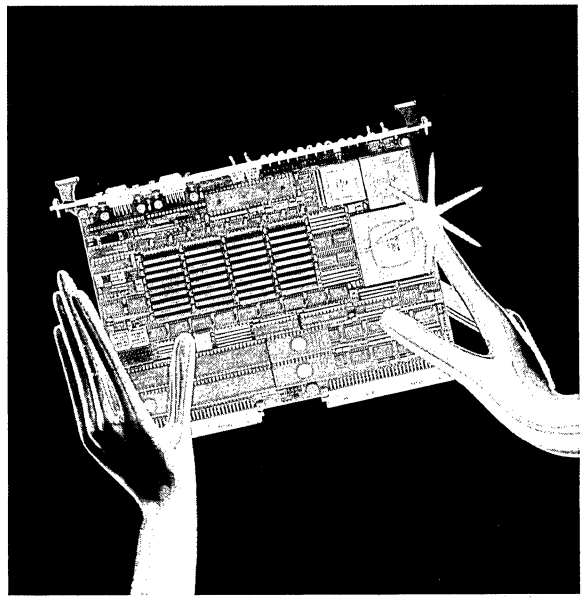
- Real Time Kernel supporting multi-tasking, up to 64 tasks
- File manager, supporting up to 64 open files at the same time
- Line assembler/disassembler with full support of all 680x0 instructions
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify
- S-record up/downloading from any port defined in the system
- Disk support for RAM disk, floppy and Winchester disks
- VMEPROM allows disk formatting and initialization
- Serial I/O support for up to two SIO-2 or ISIO-2 boards in the system; local serial I/O devices are also supported
- EPROM programming utility using the SYS68K/RR-2 board
- Full screen editor
- I/O re-direction to files or ports from the command line
- Over 100 system calls to the kernel

Specifications

Function		
68030/68882 clock frequency on:	CPU-32XB CPU-32XC	25.0 MHz 30.0 MHz
SRAM capacity Data path External battery back-up for SRAMs No. of wait states		1 Mbyte 32-bit yes 0 (all cycles)
No. of system EPROM sockets Data path Max. capacity No. of wait states (min : max)		4 32-bit 4 Mbyte 1 : 8
Serial I/O interface (total) Controller used RS232-compatible only RS232/422/RS485-compatible		2 2 × 68561 1 of 2 1 of 2
Real Time Clock (Type) with on-board battery back-up		72421
24-bit timers		2
VSB master interface A32 : D8, D16, D32 Arbiter Interrupt handler		yes yes Serial IHP
VMEbus master interface A32, A24, A16 : D8, D16, D32, UAT, RMW Single level bus arbiter VMEbus interrupt handler		 yes yes IH 1 to 7
RESET, ABORT, CACHE, HALT function switches		yes
VMEPROM firmware on all board versions		yes
Power requirements	+ 5 V min : max + 12 V min : max – 12 V min : max	4.9 A : 5.9 A 0.1 A : 0.2 A 0.1 A : 0.2 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)		0 to + 50 °C – 40 to + 85 °C 5 to 95 %
Board dimensions		234 × 160 mm : 9.2 × 6.3 in
No. of slots used		1

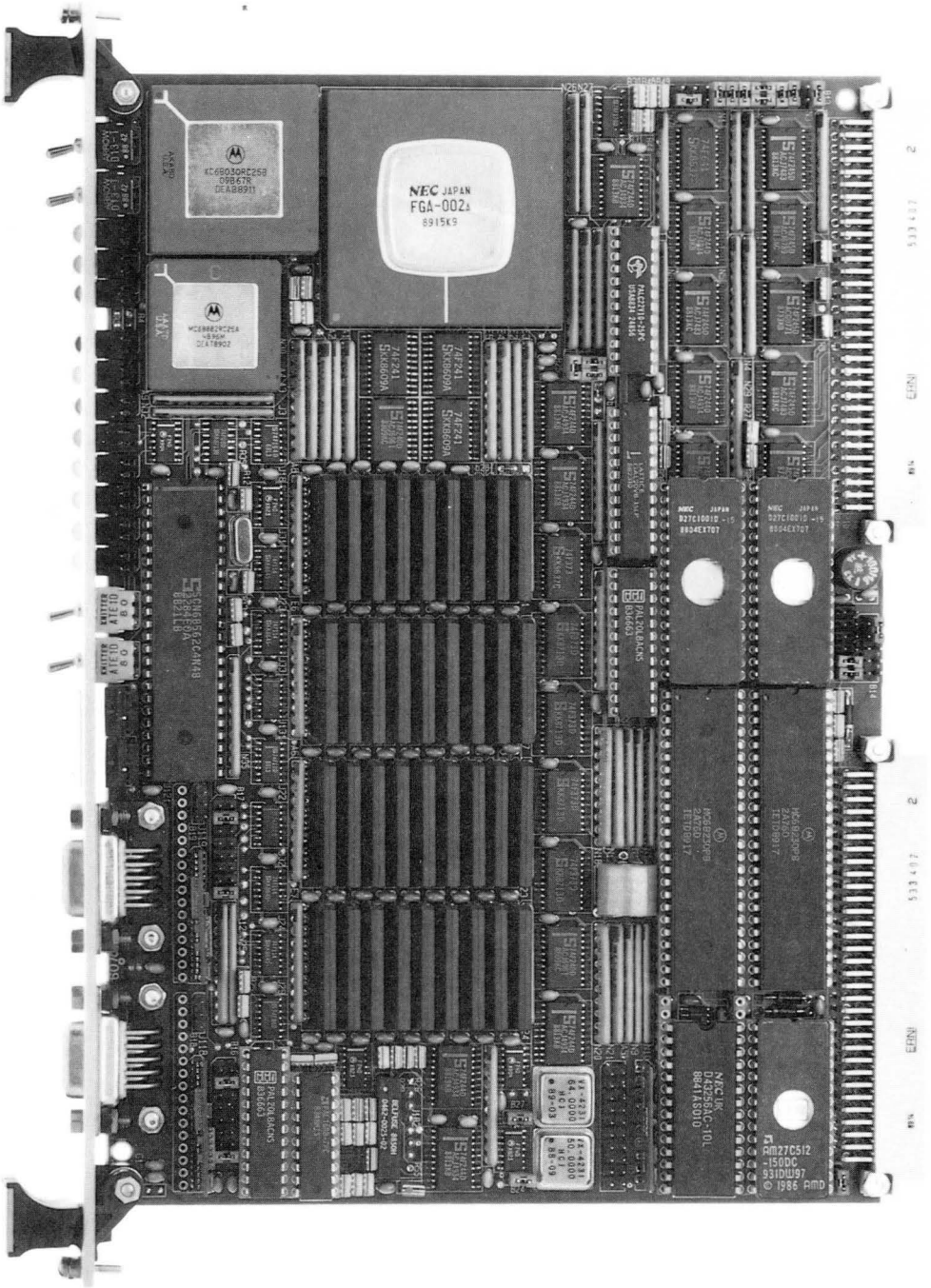
Ordering Information

SYS68K/CPU-32XB Part No. 101322	25.0 MHz 68030 CPU board with 1 Mbyte zero wait state SRAM, FPCP, parallel I/O, 2 serial I/O, VSB and VMEPROM. Documentation included.
SYS68K/CPU-32XC Part No. 101333	30.0 MHz 68030 CPU board with 1 Mbyte zero wait state SRAM, FPCP, parallel I/O, 2 serial I/O, VSB and VMEPROM. Documentation included.
SYS68K/VMEPROM/32/UP Part No. 145108	VMEPROM update service for the CPU-32 series.
SYS68K/VMEPROM/UM Part No. 800140	User's Manual of VMEPROM, excluding documentation of the SYS68K/CPU-32.
SYS68K/CPU-32/UM Part No. 800148	User's manual for the SYS68K/CPU-32 board versions, VMEPROM documentation included.



System 68000 VME
SYS68K/CPU-33

68030 CPU Board with Shared Memory and DMA


NEC JAPAN
FGA-002A
8915K9
MC68882RC25A
AM27C512
-150DC
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General Description

The SYS68K/CPU-33 is a 68030 based CPU board providing 1 or 4 Mbyte of shared memory. A 68882 Floating Point Co-Processor is also available for some board versions.

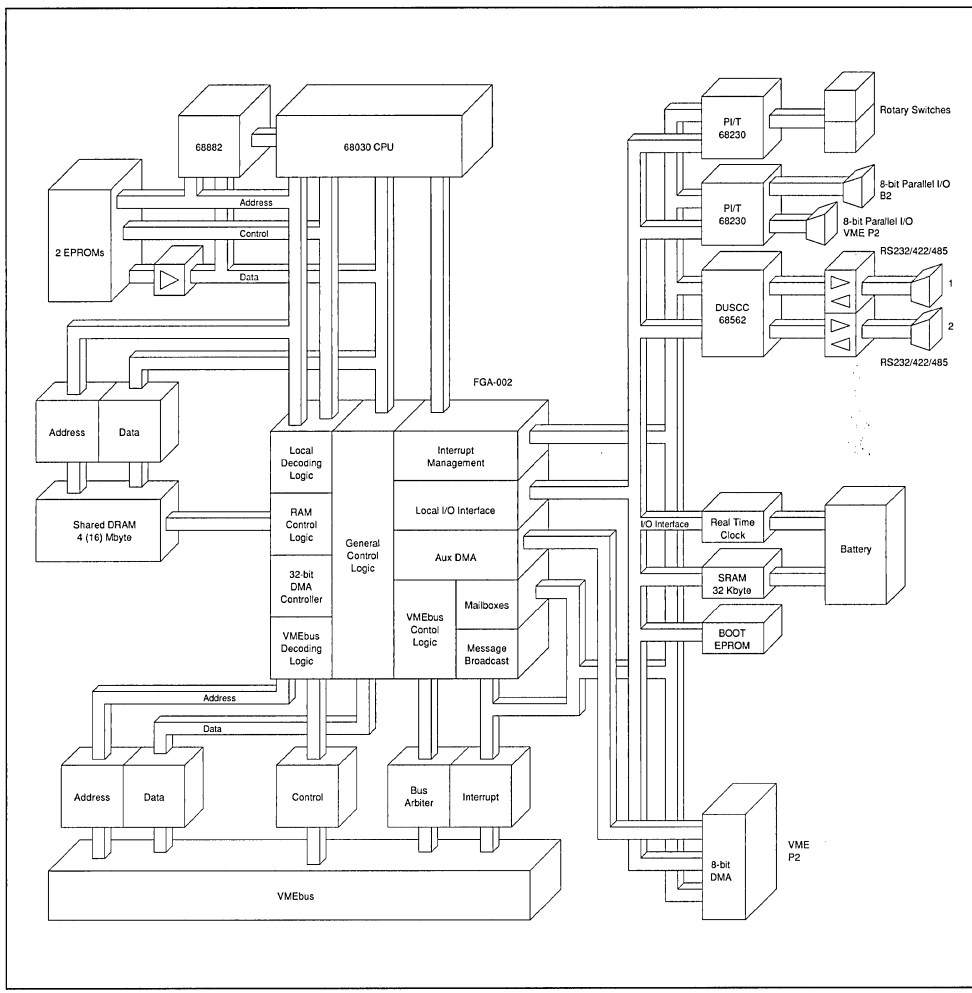
A full 32-bit DMA controller, supporting data transfers to/from VMEbus memory as well as to/from on-board RAM as well as two FORCE Message Broadcast channels and eight mailbox interrupts are provided by the 281-pin FORCE Gate Array.

Serial communication is provided through two fully independent multi-protocol channels.

Additional features include up to 2 Mbyte EPROM capacity, 32 Kbyte SRAM and a Real Time Clock. VMEPROM, the Real Time Kernel, is installed by default.

A complete 32-bit master and slave VMEbus interface and a 4-level VMEbus arbiter complete the board.

Block Diagram of the SYS68K/CPU-33



Features of the SYS68K/CPU-33

- 68030 CPU:
  16.7 MHz on CPU-33X(N),
  25.0 MHz on CPU-33XB, -33ZB
- 68882 FPCP:
  16.7 MHz on CPU-33X,
  25.0 MHz on CPU-33XB, -33ZB
- 32-bit high speed DMA controller for data transfers to/from the shared RAM and/or to/from the VMEbus memory
  - 32-byte internal FIFO for burst DMA
- 1 or 4 Mbyte of shared DRAM
- FORCE Message Broadcast (FMB)
- Two serial I/O interfaces built using one Dual Universal Serial Communication Controller (DUSCC 68562). Both channels are RS232/RS422/RS485-compatible
- 8-bit parallel interface with handshake available on P2
- 8-bit I/O bus interface with DMA on P2
- Two system EPROMs supporting 28- and 32-pin devices, using a 16-bit data path
  - 1 wait state access possible by using 100 nsec devices
- One boot EPROM for local booting and initialization of the I/O interface chips and the gate array
- 32 Kbyte SRAM with battery back-up on board, using one 28/32-pin socket (JEDEC Standard)
- Real Time Clock with calendar and on-board battery back-up
- Two 24-bit timers with 5-bit prescaler
- One 8-bit timer
- All local I/O devices are able to interrupt the local CPU on a software-programmable level
- Full 32-bit VMEbus master/slave interface supporting the following data transfer types:
  - A32, A24, A16 : D8, D16, D32 – Master
  - A32, A24 : D8, D16, D32 – Slave
  - Unaligned transfers
  - Read-Modify-Write
- BERR handling fully under software control for local and VMEbus accesses
- Four level VMEbus arbiter
- SYSCLK driver
- VME SYSRESET* driver and receiver
- IACK daisy chain driver
- VMEbus Interrupt Handler
- Support for ACFAIL* and SYSFAIL* via software-programmable IRQ levels
- Software-selectable bus time-out counters for local and VMEbus accesses
- VMEPROM, the Real Time Kernel/Monitor with file manager

1. Hardware Description

1.1 The 68030 CPU

The 68030 with its 32-bit address and data paths is installed on the SYS68K/CPU-33 board. The CPU includes a 256-byte instruction and a 256-byte data cache which significantly reduces the number of bus cycles needed for program fetches. Communication with the local I/O interfaces, local SRAM and the VMEbus interface to the 68030 CPU is provided through the specially designed 281-pin FORCE Gate Array FGA-002. The EPROM area, the optional Floating Point Co-Processor and the shared DRAM are directly connected to the CPU data and address bus interface (as shown in the block diagram of the SYS68K/CPU-33). The clock frequency of the 68030 CPU is 16.7 MHz or 25.0 MHz.

1.2 The Floating Point Co-Processor

The SYS68K/CPU-33X, -33XB and -33ZB versions are fitted with the enhanced 68882 Floating Point Co-Processor (FPCP). The clock frequencies of the CPU and the FPCP are identical. The FPCP conforms to the IEEE 754 Floating Point Standard. Intercommunication between the CPU and the FPCP is built in silicon. An internal register set inside the FPCP of eight general purpose registers (80-bit wide) yields fast execution times.

Features of the FPCP

- 8 general purpose registers (80-bit : 64-bit mantissa, 15-bit exponent and 1 sign bit)
- 67-bit on-chip ALU
- 67-bit barrel shifter
- 46 instruction types including 35 arithmetic operations
- IEEE 754 standard
- Full support of trigonometric and logarithmic functions such as:
  - Sine, cosine, tangent and cotangent
  - Hyperbolic functions
  - Logarithmic functions (4)
  - Square root and exponential functions (4)
- The 68882 is fully software-compatible to the 68881 FPCP

1.3 The Shared RAM

The SYS68K/CPU-33 contains a DRAM area with a capacity of 1 Mbyte (without parity) or 4 Mbyte (with parity).
The DRAM is accessible both from the 68030 CPU and from the VMEbus. The cycle time of the DRAM devices is 200 nsec, resulting in a four clock access period for both the CPU and for the DMA controller at 16.7 MHz. In addition, the 4 Mbyte version supports the burst-fill mode of the 68030.
Distributed asynchronous refresh is provided every 15 µsec and an access during a pending refresh cycle is delayed by a maximum of five additional clocks. The DRAM is also accessible from the VMEbus. The access address range and the address modifier codes are programmable by the local CPU.
The start and end access addresses are programmable in 4 Kbyte increments. The defined memory range can be write-protected in combination with the address modifier codes. For example, in supervisor mode, the memory may be read and written; in user mode, it may only be read. The read/write protection mechanism is fully under the user's software control.
The DRAM is accessed from the VMEbus by requesting the local bus from the CPU via the FGA-002. When the CPU has granted local bus mastership to the FGA-002, the access cycle will be executed. On read cycles all data is latched, while write cycles are terminated after storing data into the DRAM cells. On completion of the read/write cycle, the FGA-002 immediately releases bus mastership to the CPU while completing the VMEbus cycle asynchronously. This early completion of VMEbus read/write cycles effectively halves the overhead to the CPU for an external access.

1.4 The Local SRAM

A 32 Kbyte SRAM (battery back-up on-board) is installed on all SYS68K/CPU-33 board versions which supports data storage during power-down phases for up to one year. The SRAM is directly connected to the FORCE Gate Array (FGA-002) I/O interface. Long word, word and byte transfers are automatically controlled via the gate array.
Normal read/write operations to the SRAM are allowed, if the power is within the specification detected by a separate power sensor. The board is delivered with a 32 K x 8 SRAM. Higher density devices (e.g. future 128 K x 8 or 512 K x 8 devices) or EPROM devices may be inserted as the 32-pin socket allows the use of JEDEC-compatible devices.

1.5 The System EPROMs

The SYS68K/CPU-33 contains two system EPROM sockets supporting two 28- or 32-pin EPROM devices. Maximum data throughput to the 68030 CPU is provided through the fast decoding logic and separate data transceivers supporting one wait state operation, if 100 nsec devices are installed. The EPROM devices are accessed by the local 68030 CPU using a 16-bit data path.

Supported Device Types in the System EPROM Area:

Device Type	Pins	Organization	Total Memory Capacity
27512	28	64 K × 8	128 Kbyte
2710xx	32	128 K × 8	256 Kbyte
2720xx	32	256 K × 8	512 Kbyte
TBD	32	512 K × 8	1 Mbyte
TBD	32	1 M × 8	2 Mbyte

1.6 The Boot EPROM

The SYS68K/CPU-33 board contains, in addition to the two system EPROMs, a single boot EPROM to boot the local CPU, initialize all I/O devices and program the board dependent functions of the FORCE Gate Array (FGA-002). All presetting and initialization of the I/O devices are made through the boot EPROM.

1.7 The DMA Controller

A high speed DMA controller inside the FGA-002 is available on the SYS68K/CPU-33. It features a maximum data transfer speed of up to 11.14 Mbyte/sec on the VMEbus and 13.6 Mbyte/sec to the shared RAM.
DMA execution on the VMEbus is performed without any degradation of performance for the local CPU. This allows a program to be run while loading new data into the shared RAM or writing

processed data to global RAM or I/O controller boards. If the data has to be stored or read to/from the shared RAM, the DMA controller requests bus mastership from the local CPU.
To increase the data throughput, the DMA controller operates using a 32-byte FIFO for internal data storage. The read and write operations are executed in bursts of eight transfers with 4 bytes per transfer. This results in eight read cycles followed by eight write cycles.
This feature significantly increases data throughput because the local CPU maintains the real time capabilities by being interruptable during DMA transfers on the VMEbus.
This technology allows data transfers between the shared RAM and the VMEbus by first collecting data from the VMEbus, giving up bus mastership and then transferring the data to the shared RAM. A second VMEbus board can transfer data on the VMEbus while the DMA controller transfers the stored data to the shared RAM. The CPU can operate in parallel to the DMA controller because of the 32-byte FIFO and the structure of the SYS68K/CPU-33.
This means that during DMA transfers, the CPU can access all local I/O devices, the EPROM area as well as the shared RAM. If the CPU wants to access the VMEbus, it has to wait until the DMA controller has completed the transfers from its FIFO (max. eight transfers).

The following table shows the 68030 performance during the DMA data transfers:

Area 1		Area 2	CPU Operation	Note
VMEbus	⇔	VMEbus	100 %	–
VMEbus	⇔	DPR	60–70 %	1

Note 1: CPU operation depends on the transfer speed of the addressed VMEbus board.

The DMA controller supports aligned and unaligned data transfers. The internal control logic first aligns the data transfers to take full advantage of the 32-bit bus structure.

Register Set of the DMA Controller

8	Interrupt Control Normal Termination
8	Interrupt Control Error Termination
8	Source Attribute Register
8	Destination Attribute Register
8	General Control Register
8	Interrupt Status Normal Termination
8	Interrupt Status Error Termination
8	Run Control Register
8	Mode Status Register
32	Source Address
32	Destination Address
32	Transfer Count

1.8 Benchmarks

	CPU-33X 16.7 MHz	CPU-33XB 25 MHz	Unit
Dhrystones	4347	7642	Dhryst./sec
Whetstones	909	1428	KWhet./sec
Sieve	4.32	2.78	sec/100 iterations
DMA – Local	7.80	12.73	Mbyte/sec
DMA – VME	8.31	12.29	Mbyte/sec

1.9 The Local I/O Devices

The SYS68K/CPU-33 contains a gate array (FGA-002) which provides an 8-bit local I/O interface used to interconnect the CPU and the I/O devices.
The Real Time Clock as well as the serial I/O controller and the parallel I/O controller are connected to this local I/O interface.

1.10 I/O bus

The auxiliary DMA channel of the FGA-002 provides a high speed 8-bit port which is connected to the P2 connector of the CPU-33. This additional interface allows the user of the CPU-33 to build application specific I/O interfaces to have a direct connection to the CPU-33 and the DMA controller in the FGA-002.

1.11 The Serial I/O Interfaces

One Dual Universal Serial Communication Controller (DUSCC 68562) is installed on the SYS68K/CPU-33 to communicate to terminals, computers or other equipment.

Serial I/O Signal Assignments

Pin	DUSCC Channels 1 + 2	
	RS232	RS422/485
1	DCD	TXD–
2	RXD	RTS–
3	TXD	CTS+
4	DTR	RXD+
5	GND	RXD–
6	DSR	TXD+
7	RTS	RTS+
8	CTS	CTS–
9	GND	RXD–

Features of the DUSCC

- Dual full-duplex synchronous and asynchronous receiver and transmitter (programmable)
- Multi-protocol operation enabling support of bit- or character-oriented protocols. With additional software this allows the support of HDLC, SDLC, X.25, X.75, BISYNC, etc.
- Programmable data encoding formats: NRZ, NRZI, FM0, FM1, Manchester
- 4 character receiver/transmitter FIFOs
- Individual programmable baud rate for each receiver and transmitter supported by a digital phase locked loop
- Modem control signals for each channel: RTS, CTS, DCD
- Both channels of the 68562 are connected to 9-pin D-sub connectors on the front panel via RS232-compatible drivers/receivers
- The DUSCC can interrupt the local CPU on a software-programmable level (1 to 7)

1.12 The Real Time Clock

A software-programmable Real Time Clock (RTC-72421) with on-board battery back-up is installed on the SYS68K/CPU-33 boards.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12 hr/24 hr clock switch-over
- Automatic leap year setting
- Interrupt masking
- CMOS design provides low power consumption during power-down mode

The Real Time Clock is able to interrupt the local CPU on a level programmable through the gate array (1 to 7).

1.13 The Input/Output Ports

The SYS68K/CPU-33 contains two 68230 PI/T devices. The I/O ports of these devices are used for on-board control and user interfaces.
The first 68230 is connected to the rotary switches on the front panel and to an 8-bit header which is free for user applications. The front panel switches are used by the boot EPROM and by VMEPROM to select various software options. The second 68230 supports a user I/O port on the P2 connector with 8-bit data path and 4 handshake signals. In conjunction with off-board drivers this port can be used to build a Centronics-compatible parallel interface or for other high speed parallel data transfers. In addition, the memory size and the board type as well as the set-up of the mode of the 4-level arbiter can be read in via the second PI/T chip.

1.14 The Timers

A total of three independent timers are available for the user. These timers offer maximum flexibility because each timer can be used to force an interrupt to the CPU on a software-programmable IRQ-level (1 to 7).
The first two timers are 24-bit timers with individual 5-bit prescaler. One of these two timers can optionally be used to reset the 4-level arbiter if BBSY is not driven within a software-programmable time after a bus grant has been issued. This avoids potential hang-ups of the arbiter. The third timer is an 8-bit timer with programmable source clock divider installed in the gate array (FGA-002). This timer can also be used as a watchdog to generate SYSFAIL* on the VMEbus.
SYSFAIL* can be used in multi-processor systems to signal that one board has detected a failure. The watchdog timer needs to be reset periodically (software-programmable). Without such a reset, a SYSFAIL* will be asserted on the VMEbus.
All installed timers can be used as continuous timers or can generate interrupts on a periodical or on a single shot basis.

2. The Memory Map

The memory map of the SYS68K/CPU-33 is listed in the following table:

Start Address	End Address	Type
00000000	003FFFFF	Shared Mememory 4 Mbyte
00400000	F9FFFFFF	VMEbus, A32 : D32, D24, D16, D8
FA000000	FAFFFFFF	Message Broadcast Area
FB000000	FBFEFFFF	VMEbus, A24 : D32, D24, D16, D8
FBFF0000	FBFFFFFF	VMEbus, A16 : D32, D24, D16, D8
FC000000	FCFEFFFF	VMEbus, A24 : D16, D8
FCFF0000	FCFFFFFF	VMEbus, A16 : D16, D8
FD000000	FEFFFFFF	Reserved
FF000000	FF7FFFFF	System EPROM
FF800000	FFBFFFFF	Local I/O
FFC00000	FFCFFFFF	Local SRAM
FFD00000	FFDFFFFF	Registers of FGA-002
FFE00000	FFEFFFFF	Boot EPROM
FFF00000	FFFFFFFF	Reserved

3. The VMEbus Interface

The SYS68K/CPU-33 includes a full 32-bit VMEbus interface. The address modifier codes for A16, A24 and A32 addressing are fully supported in master mode.
The gate array controls the access cycle to the DRAM and determines if an access is to be allowed (read/write protection). Read-Modify-Write cycles are fully supported to allow multiple CPU boards to be synchronized via the shared RAM. By default VMEPROM disables the support for on-board RMW cycles from the VMEbus to the on-board memory to reduce the overhead for the access. The support for RMW cycles can easily be enabled by reprogramming the FGA-002.

The following bus release modes are supported by the SYS68K/CPU-33:

ROR: Release on Request with a programmable inhibit time-out. This function releases bus mastership if another request is pending after a programmable time. The shortest inhibit time is 500 nsec and the longest is 64 µsec.

RBCLR: Release on Bus Clear. The bus mastership is released when the BCLR signal becomes active.

RV: Release voluntarily. The VMEbus mastership is released voluntarily after 100 µsec if there are no accesses to the VMEbus in that time period.

RACFAIL: Release on ACFAIL*. The VMEbus mastership is released immediately if the ACFAIL* signal becomes active. As long as ACFAIL* is active, the CPU-33 will not request VMEbus mastership.

Each of the listed modes is software-programmable inside the gate array. The bus request level of the SYS68K/CPU-33 is jumper-selectable (BR0-3*).

The 4-level arbiter of the SYS68K/CPU-33 can be set to one of the following modes:

PRI: Prioritized, with BR3* having the highest priority and BR0* the lowest.

PRR: Prioritized round robin. The request level 3 is prioritized and the levels 2-0 served in round robin mode.

RRS: Round robin. All bus requests are served in round robin mode.

All modes are jumper-selectable and the mode can be read back by software via the second PI/T. The DMA controller of the SYS68K/CPU-33 can access the VMEbus independently from the CPU. This allows the DMA to transfer data across the VMEbus while the processor is accessing the on-board memory or I/O devices.
A power monitor and a SYSRESET* driver and receiver complete the VMEbus interface.

4. The Interrupt Structure

The gate array installed on the SYS68K/CPU-33 handles all local and VMEbus interrupts. Each interrupt request from the DUSCC, RTC, and the PI/T devices, as well as the gate array specific interrupt requests, are combined with the seven VMEbus IRQs and are handled inside the FGA-002.
Each IRQ source, including the VMEbus IRQs, can be programmed to interrupt the CPU on an individual programmable level (1 to 7).
The gate array supports the vector, or initiates an interrupt vector fetch from the I/O device or from the VMEbus.
In addition to the local interrupts, the ACFAIL* and SYSFAIL* signals can be used to interrupt the CPU on a software-programmable level.The VMEbus interrupt levels can be programmed inside the gate array to cause an interrupt request on a different level to the CPU. For example, a level 7 VMEbus interrupt request can be programmed to cause a level 2 interrupt to the processor. In addition, every interrupt level can be enabled/disabled individually within the gate array by software. The gate array supplied interrupt vectors have a basic vector and fixed increments for each source. The basic vector is software-programmable.

5. The Multi-Processor Mailboxes

The SYS68K/CPU-33 includes eight multi-processor mailboxes. Each of these allows an interrupt to be forced to the local 68030 CPU. The interrupt level of each is software-programmable and an individual interrupt vector for each may be passed to the CPU. This function allows the triggering of an interrupt on the SYS68K/CPU-33 from multiple masters on the VMEbus. The mailboxes are accessed via a Read-Modify-Write cycle, thus allowing multiple masters on the VMEbus to share the same mailbox channel.

6. FORCE Message Broadcast

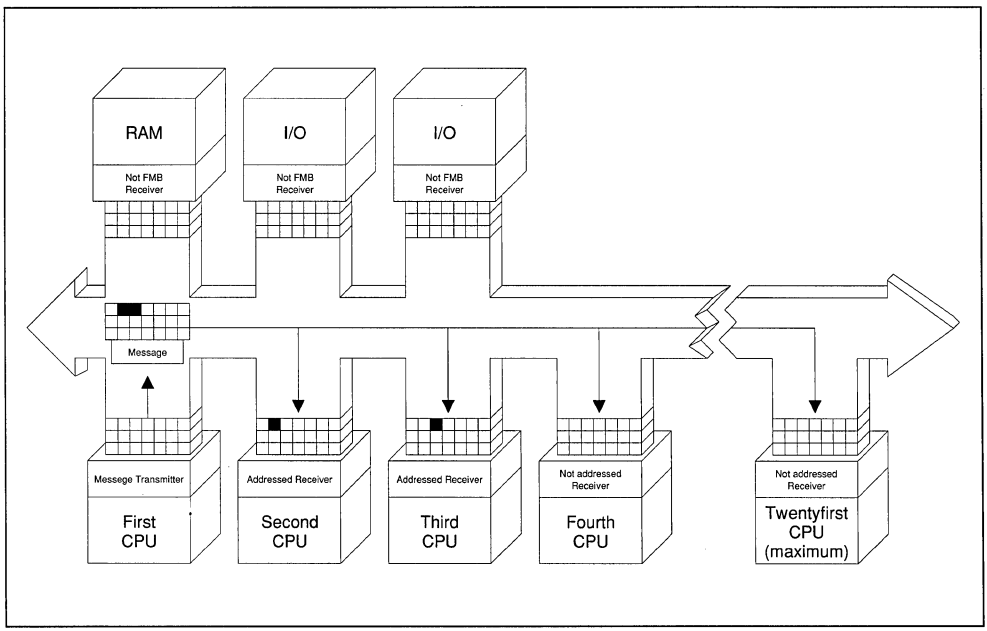
The FORCE Message Broadcast (FMB) is a fast and effective mechanism to communicate with and to synchronize up to 20 CPU boards in a VMEbus system in only one VMEbus write cycle. It offers a unique support feature for building multi-processing systems based on the VMEbus. An FMB transfer is a standard VMEbus write cycle and complies fully to the IEEE 1014 Specification. Any VMEbus master may be a message transmitter. The transmitter decides which boards in the system should be addressed (one, two or up to twenty boards) and writes the message to a specific address.

All addressed boards receive the message at the same time and generate an interrupt request on a programmable level to their local microprocessor. This ensures that there is no time delay between the synchronization of different boards in the system. The ability to communicate with and synchronize multiple CPUs in the system by the FMB mechanism allows the VMEbus to be used in a wide range of application areas, particularly multi-processor environments.

Without the FMB mechanism, communication between and synchronisation of system boards has to be managed via the seven interrupt request lines. FMB reduces the massive time overhead normally needed to process the interrupt cycles to just one write cycle.

All FORCE VME/PLUS boards provide two fully independent message broadcast channels. Channel 0 stores 8-bit messages in an eight stage deep FIFO, channel 1 stores one 8-bit message and can therefore be used for high priority messages.

Block Diagram of the FORCE Message Broadcast



7. Software

It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-33 Software Support

Operating System/Kernel	Vendor/Support
UNIX V.3/V.4	Contact FORCE for availability
PDOS	FORCE COMPUTERS
OS-9/9000	FORCE COMPUTERS/MICROWARE
VMEPROM	FORCE COMPUTERS
VxWORKS	FORCE COMPUTERS/ Wind River Systems
VRTX-32	READY SYSTEMS
pSOS	Software Components Group
ARTX	Contact FORCE for availability
Telesoft ADA	Contact FORCE for availability

As a courtesy, FORCE provides the user with the ability to immediately start a real time application by including VMEPROM on every CPU card, free of charge and free of licensing costs.
VMEPROM is an EPROM-based Real Time Multi-tasking Kernel/Monitor. The complete package resides in 256 Kbyte of EPROM and uses 32 Kbyte of RAM. VMEPROM fully supports all of the on-board I/O devices.
VMEPROM is composed of a highly sophisticated Real Time Kernel, which is based on the PDOS Real Time Kernel. A file manager supporting sequential, random and shared files is also included.
The user interface contains more than 60 commands perfectly suited for program debugging, host computer communications, as well as task and file management. It includes a powerful debugger, supporting line assembler/disassembler for the microprocessor.

Features of VMEPROM

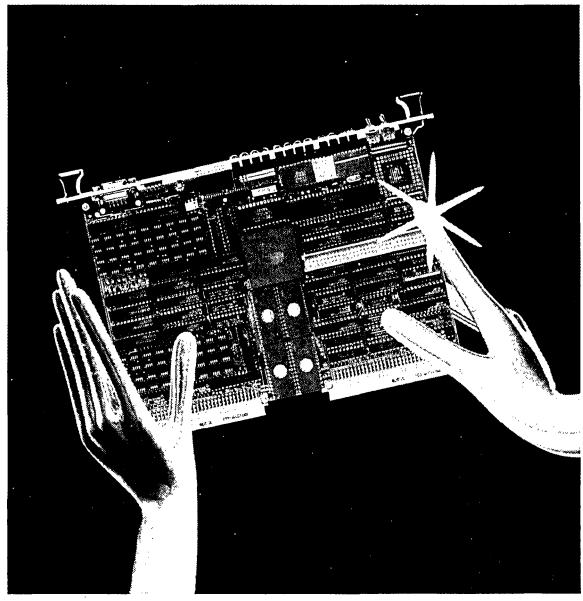
- Real Time Kernel supporting multi-tasking, up to 64 tasks
- File manager, supporting up to 64 open files at the same time
- Line assembler/disassembler with full support of all 680x0 instructions
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify
- S-record up/downloading from any port defined in the system
- Disk support for RAM disk, floppy and Winchester disks
- VMEPROM allows disk formatting and initialization
- Serial I/O support for up to two SIO-2 or ISIO-2 boards in the system; local serial I/O devices are also supported
- EPROM programming utility using the SYS68K/RR-2 board
- Full screen editor
- I/O re-direction to files or ports from the command line
- Over 100 system calls to the kernel

Specifications

Function		
CPU		68030
FPCP Type CPU-33X, -XB, -ZB		68882
CPU clock frequency on:	CPU-33X, -XN CPU-33XB, -ZB	16.7 MHz 25.0 MHz
Shared DRAM capacity	CPU-33X, -XN, -XB CPU-33ZB	1 Mbyte 4 Mbyte
Parity protection of the main memory		CPU-33ZB
SRAM capacity with on-board battery back-up		32 Kbyte
No. of system EPROM sockets Data path		2 16-bit
Serial I/O interface (68562), RS232/422/485-compatible		2
I/Obus on P2 DMA via FGA-002		8-bit yes
Parallel I/O interface (68230) on P2		12 lines
Real Time Clock with on-board battery back-up		72421
24-bit timers with 5-bit prescaler 8-bit timer		2 1
VMEbus interface Shared memory access time from VMEbus (read/write) min : typ : max	A32, A24, A16 : D8, D16, D32, UAT, RMW A32, A24 : D8, D16, D32, RMW	master slave 600 : 900 : 1600 nsec
SYSCLK driver Mailbox interrupts		yes 8
FORCE Message Broadcast	FMB-FIFO 0 FMB-FIFO 1	8 byte 1 byte
VMEbus and local interrupt handler All sources can be routed to a software-programmable IRQ level		IH 1–7 yes
RESET and ABORT switch		yes
VMEPROM firmware installed on all board versions		yes
Power requirements	+ 5 V min : max + 12 V min : max – 12 V min : max	4.2 A : 4.8 A 0.1 A : 0.3 A 0.1 A : 0.3 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)		0 to + 50 °C – 40 to + 85 °C 5 to 95 %
Board dimensions (mm : in)		234 × 160 mm : 9.2 × 6.3 in
No. of slots used		1

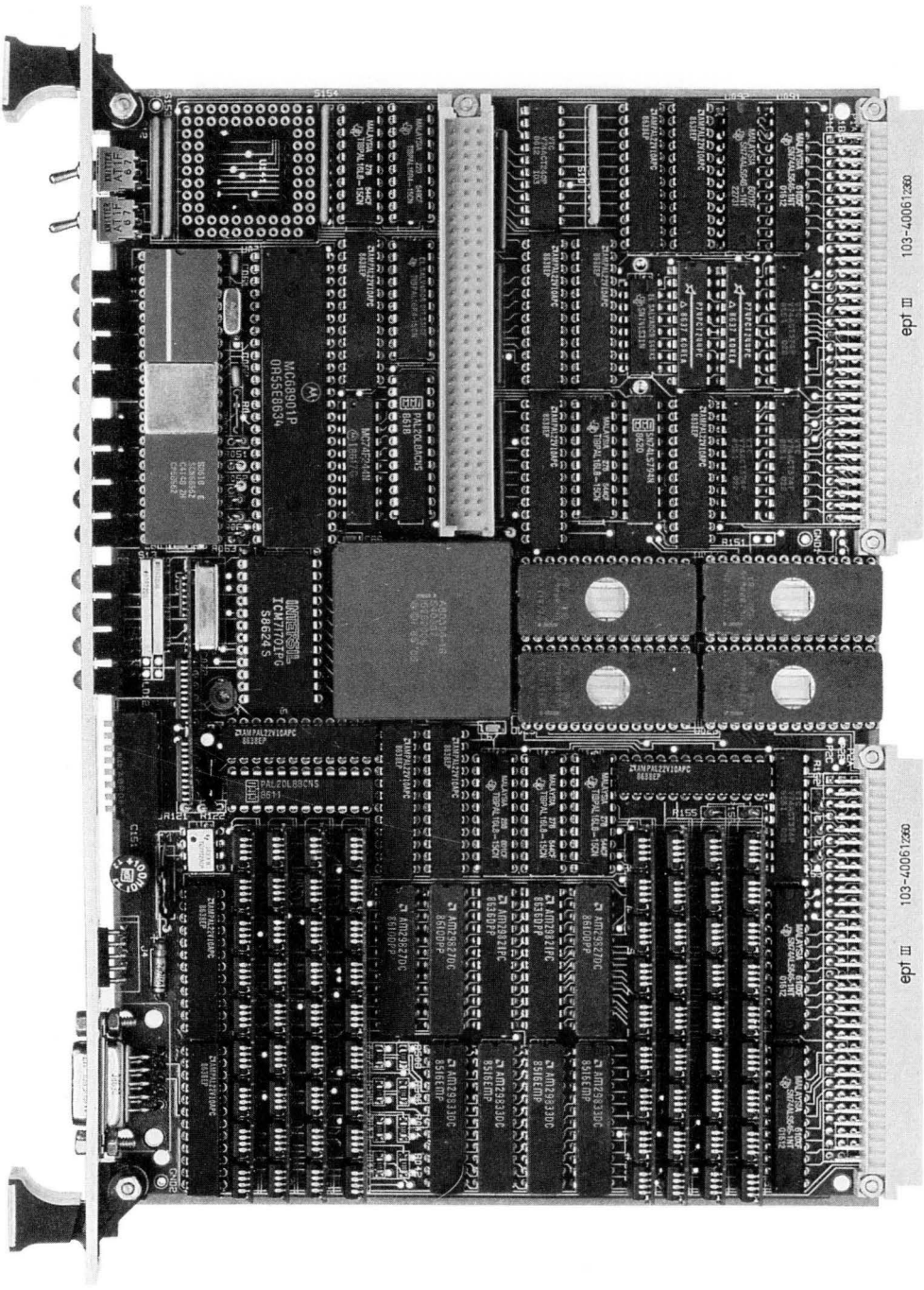
Ordering Information

SYS68K/CPU-33XN Part No. 101340	16 MHz 68030 based CPU, no coprocessor, 1 Mbyte shared DRAM, 2 serial ports, parallel port, DMA. Documentation included.
SYS68K/CPU-33X Part No. 101341	16 MHz 68030 based CPU, with coprocessor, 1 Mbyte shared DRAM, 2 serial ports, parallel port, DMA. Documentation included.
SYS68K/CPU-33XB Part No. 101342	25 MHz 68030 based CPU, with coprocessor, 1 Mbyte shared DRAM, 2 serial ports, parallel port, DMA. Documentation included.
SYS68K/CPU-33ZB Part No. 101343	25 MHz 68030 based CPU, with coprocessor, 4 Mbyte shared DRAM, 2 serial ports, parallel port, DMA. Documentation included.
SYS68K/VMEPROM/33/UP Part No. 145116	VMEPROM update service for the CPU-33 series.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM user's manual, excluding the SYS68K/CPU-33 description.
SYS68K/CPU-33/UM Part No. 800171	User's manual for the SYS68K/CPU-33, VMEPROM and FGA-002 user's manuals included.



System 80386 VME
SYS80K/CPU-386

80386 High Performance 32-Bit CPU Board

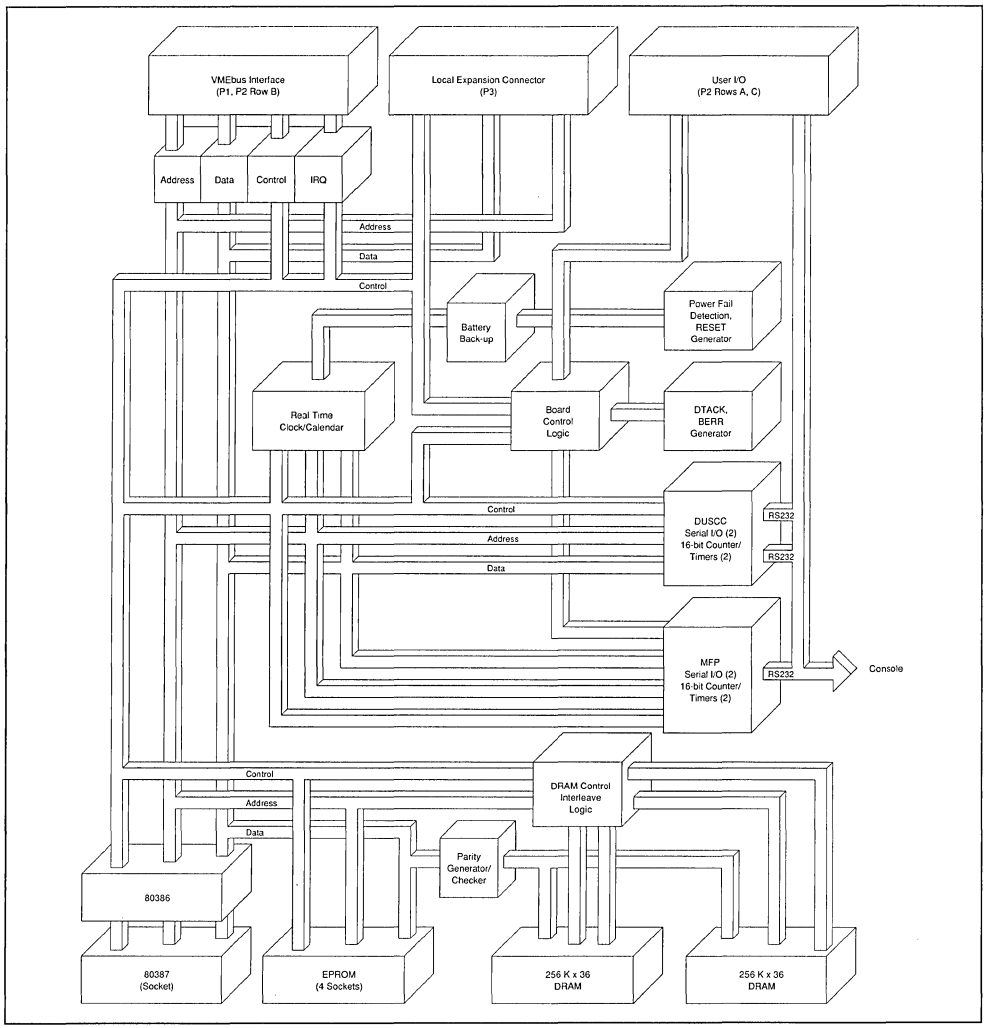

epf III 103-400612360
epf III 103-400612360

General Description

The SYS80K/CPU-386 is a high performance CPU board designed using an 80386 32-bit microprocessor and 80387 numeric co-processor. The board is built for the VMEbus IEEE 1014 system environment and provides four sockets for JEDEC-compatible memory devices (EPROMs, EEPROMS), 3 serial I/O ports, time-of-day/Real Time Clock/Calendar, two 16-bit and three 8-bit counters/timers.

The SYS80K/CPU-386 is available with 2 or 8 Mbyte of parity-checked dynamic RAM. This local memory has been configured to provide zero wait state operation at 16 MHz for read and write cycles. A powerful debugging package with full 80386 and 80387 line assembler/disassembler capabilities called FORCEbug/386 is included. FORCEbug/386 also features test facilities, floating point co-processor support, benchmark routines, and macro facilities.

Block Diagram of the SYS80K/CPU-386



Features of the CPU-386

- 16 MHz 80386 processor
- 16 MHz 80387 numeric co-processor
- 3 serial I/O interfaces (RS232)
- 7170 Real Time Clock
- 2 or 8 Mbyte of zero wait state, dynamic RAM with parity
- 4 sockets for 8 K × 8 to 64 K × 8 EPROMs, EEPROMs and page-mode byte-wide devices
- Three 8-bit timers
- Fully buffered 32-bit local address and data buses
- Full VMEbus master interface:
  - A32, A24, A16 : D8, D16, D32
  - Unaligned transfer
  - Address pipelining
  - SYSCLCK driver
- 4-level bus arbiter
- Interrupt Handler (Local, VME IRQ1-IRQ7, optional autovectors, and two non-maskable interrupts)
- Bus timer for BERR generation
- RESET generator
- Front panel LED indicators: green: EPROM, RAM, I/O & VMEbus accesses, red: HALT, SHUTDOWN, PARITY & BERR, yellow: four user-definable indicators
- Front panel switches: RESET and ABORT
- "Smart" jumpers set under program control
- Custom geographical addressing simplifies configuration
- Electronic Tag Module Socket for providing user-defined configuration information
- Four debug registers and programmable single-step flag for simplified program debugging
- FORCEbug/386 debugger firmware with 80387 numeric co-processor support, macro facilities and assembler/disassembler

1. Hardware Description

1.1 The 80386 CPU

The 80386 processor is a highly-integrated device containing a central processing unit, memory management unit and bus interface unit. This processor features 32-bit wide internal and external data buses, and is implemented on-board to take full advantage of the 32-bit VMEbus structure.
The clock speed of the 80386 is set at 16 MHz. Coupled with a pipelined architecture, zero wait state, 32-bit wide dynamic RAM, and a 16-byte prefetch instruction queue that reduces bus overhead, the 80386 operates with 3 to 4 MIPS of effective computing power.
An extensive instruction set which includes eleven addressing modes has been incorporated into the 80386. All instructions are orthogonal supporting 8-, 16-, 24- and 32-bit data structures. The 80386 can address 4 Gbyte of physical memory and the on-chip memory management unit fully supports virtual addressing. Additionally, the 80386, in emulation mode, will execute programs written for the 8086/8088/80286/80386 family. A fully buffered address and data bus has been implemented for the CPU to communicate to local I/O and memory.

1.2 The 80387 Numeric Co-Processor

The 80387 is a high performance Floating Point Co-Processor designed to improve the throughput of 80386 mathematical and trigonometric calculations. The 80387 implements the IEEE 754 Floating Point Standard, with high-precision 80-bit architecture and full support for single, double, and extended precision operations.

1.3 The Serial I/O Channels

The CPU-386 board contains three serial communication channels. The 68562 Dual Universal Serial Communications Controller (DUSCC) provides two of the three channels.

Features of the DUSCC

- Dual full-duplex synchronous and asynchronous receiver and transmitter (programmable)
- Multi-protocol operation enabling support of bit- or character-oriented protocols. With additional software this allows the support of HDLC, SDLC, X.25, X.75, BISYNC, etc.
- Programmable data encoding formats: NRZ, NRZI, FM0, FM1, Manchester
- 4 character receiver/transmitter FIFOs
- Individual programmable baud rate for each receiver and transmitter supported by a digital phase locked loop
- Modem control signals for each channel: RTS, CTS, DCD

RS232-compatible interfaces (both ports) are installed on the board to provide direct connection

to standard terminals. User connection has been configured such that a standard flat cable terminated in a 9-pin D-sub connector provides an IBM PC/AT style interface (both ports). The second port also supports modem control signals. Both serial ports are accessible through the VMEbus P2 connector.
A 68901 Multi-Function Peripheral Controller (MFP) provides a third serial communication channel. This port is normally programmed to 9600 baud by FORCEbug/386 at power-up, and an IBM AT style 9-pin D-sub connector on the front panel enables this channel to be used as console and debugging port with the following features:

- Full duplex operation
- Asynchronous to 19,200 bits/sec
- Synchronous to 1 Mbit/sec

Each of the three serial I/O channels (DUSCC and MFP) is capable of issuing an interrupt to the processor. The interrupt vector values are programmable.

1.4 Real Time Clock

A 7170 Real Time Clock, with 10-year battery back-up, provides a user-accessible clock/calendar. Year, month, date, day, hours, minutes, seconds and hundredths of a second may be read and written under program control. An alarm function can also be programmed and enabled to generate an interrupt. The real time clock can be used to output a periodic interrupt at any one of six different rates from 100 Hz to once per day.

1.5 Programmable Counter/Timers

Three programmable counter/timers available to applications are provided on the CPU-386 board. The counter/timers are 8 bits wide and are included in the 68901 (A, B, C).
8-bit counter A may be programmed to operate in delay, count, or pulse-width mode. Counter C functions primarily as a rate generator. Prescale selection of 4 to 200 extends the dynamic range of these three counters. Additionally, counters A and B have their auxiliary inputs, used in pulse-width mode, connected to the user I/O pins on the VMEbus P2 connector. Interrupts for counters A, B and C may be enabled/disabled under program control.

1.6 Interrupt Handling

The 80386 processor provides vector-defined interrupt support. Two interrupt lines, one maskable, the other non-maskable, are used to inform the 80386 of interrupt requests. All interrupts generated by IRQ1*–IRQ6* from the VMEbus, as well all local (on-board) devices, are routed to the maskable interrupt input of the 80386. The VMEbus IRQ1*–IRQ6* interrupts are individually maskable through bits programmatically set and reset in the board interrupt mask register. Interrupts IRQ1*, IRQ3* and IRQ5* may also be implemented using autovectoring. The non-maskable interrupt input of the 80386 supports two functions; VMEbus IRQ7* and the ABORT switch on the front panel of the CPU-386.

1.7 Local Read/Write Memory

2 Mbyte configured as two banks of 256 K × 36 bits or 8 Mbyte configured as 1 Mbyte × 36 bits of dynamic read/write, pipelined zero wait state memory are provided on the CPU-386 board. Dividing the on-board memory into two logical banks and using look-ahead logic for interleave access improves memory response time for transfer speeds to 32 Mbyte/sec. Parity checking is also provided.
The refresh algorithm for the on-board RAM further improves memory access speed by minimizing interference with processor memory accesses. Under normal conditions, a refresh cycle occurs only when both banks of memory are idle. Memory integrity is ensured by an on-board timer that converts memory refresh to a high priority request. A 16-byte pre-fetch instruction queue on the 80386 further eliminates most processor hold-offs due to refresh activity. The 80386 transfers opcodes to the queue in bursts of memory accesses, and then executes instructions from this queue. Memory refreshes can then occur while the 80386 is executing opcodes from its on-chip resources. In this way, the majority of refresh cycles are transparent.

1.8 Local EPROM Support

The CPU-386 contains four sockets for 28-pin JEDEC-compatible EPROM devices: 2764 through 27512 or equivalent. Configuration of these sockets for devices is accomplished with "smart jumpering". EPROM, as well as EEPROM, type, size, and speed is conveniently selected by

the front panel DIP switch. EPROM capacity is from 32 Kbyte to 256 Kbyte, and switch-selectable support of page mode devices increases capacity to 512 Kbyte. EPROM access is 32-bit wide, and access times down to 100 nsec (one wait state) are supported.

Device Type	Organization	Total Memory Capacity
2764	8 K × 8	32 Kbyte
27128	16 K × 8	64 Kbyte
27256	32 K × 8	128 Kbyte
27512	64 M× 8	256 Kbyte

Interrupt Source	Interrupt Generator
ABORT SWITCH	Direct (NMI)
VMEbus IRQ7*	Direct (NMI)
DUSCC serial I/O (2)	DUSCC (MI)
MFP serial I/O (1)	MFP (MI)
Real Time Clock	MFP (MI)
MFP 8-bit counter/timer (A, B, C)	MFP (MI)
DUSCC 16-bit counter/timer (A, B)	DUSCC (MI)
VMEbus ACFAIL*	MFP (MI)
VMEbus SYSFAIL* MFP	(MI)
DRAM memory parity error	MFP (MI)
VMEbus IRQ1*– IRQ6*	BIMR (MI)
VMEbus IRQ1*, IRQ3*, IRQ5*, autovector	MFP (MI)

Note: DUSCC = Dual Universal Serial Communications Controller
MFP = 68901 Multi-Function Peripheral
MI = Maskable Interrupt
NMI = Non-Maskable Interrupt
BIMR = Board Interrupt Mask Register

1.9 The VMEbus Interface

A full 32-bit VMEbus interface is implemented on the CPU-386 to communicate with global memory, I/O, and other functions.

The 4 Gbyte physical address space of the 80386 processor is fully decoded. 8-, 16-, 24- and 32-bit data transfers are supported.

As an example, the support of unaligned transfers allows the 80386 CPU to operate with efficient throughput because a 16-bit transfer to an odd address needs only one bus cycle. Without unaligned transfer support, two bus cycles are needed because the single transfer must be split into 2 cycles, thereby impeding performance of the processor.

The CPU-386 board is designed to support fully the VMEbus address pipelining function. During normal VMEbus operation, a master completes all handshaking requirements of the current bus cycle prior to initiating the next one. Support of address pipelining enables the CPU-386 to begin subsequent cycles as soon as DTACK* (slave acknowledge) is returned.

This capability reduces bus transaction overhead by overlapping address broadcasting with data transfers, and thereby improves throughput of data on the VMEbus.

Further improvement in VMEbus performance is provided by two VMEbus-related features of the CPU-386. The CPU-386 determines VMEbus access requests in advance of when a normal VMEbus cycle begins. This enables the CPU-386 to gain control of the system immediately following a release by the current master. On the completing end of the cycle, the CPU-386 is capable of "early BBSY* (Bus Busy) release", informing other masters that the VMEbus will be available. This enables the completion of arbitration by the next VMEbus master, and control of the bus is transferred immediately following release by the CPU-386. In addition, if the VMEbus is required for the next cycle, the CPU-386 will continue to assert BBSY*, prohibiting another master from arbitrating for the VMEbus. This allows the CPU-386 to retain control without arbitration. Both of these features improve the overall performance of the VMEbus by minimizing unnecessary wait time due to arbitration.

A VMEbus system controller and bus arbiter is installed on the CPU-386 for multiple CPU board configurations. The four-level VMEbus arbiter may be programmed to operate in one of three modes: "round robin", prioritized, and single-level, providing flexibility in implementing a system for highest performance.

1.10 Expansion Connector (P3)

A 96-pin local bus connector is provided on the CPU-386 board to support memory and I/O enhancements. Address, data, and controls are brought directly from the 80386 to the connector. This connector is reserved for future use by FORCE Computers.

1.11 VMEbus User I/O Connector (P2A, P2C)

The P2 connector of the CPU-386 board enables access to user I/O signals on the VMEbus backplane. Serial I/O, parallel I/O, interrupts, counter/timer inputs and outputs, and board and user status lines (LEDs) are available at rows A and C on the P2 connector. See P2 connector pin assignment.

2. Software Description

2.1 General Description

FORCEbug/386 is an EPROM-resident debugging package for the CPU-386 board. It features test facilities, debugging tools, a powerful line assembler/disassembler for the 80386 processor, and a macro facility for use with all FORCEbug/386 commands.

2.2 Features of the FORCEbug/386

- Powerful command set including:
  - Test facilities
  - Debugging tools
  - Program upload/download facilities
  - Benchmark programs
- Line assembler/disassembler fully supporting all 80386 and 80387 opcodes/mnemonics and addressing modes
- Macro facility for FORCEbug/386 commands
- Recall of previous input lines using Control A
- Program execution timer with 10 msec resolution

2.3 Command Summary

The test facilities allow the user to test and debug hardware on the external bus as well as to prove functionality of all on-board devices.

The debugging tools are well suited to download programs from a host computer and debug them on the board. Included is breakpoint setting, single-stepping, continuous tracing, display and modify all processor registers and memory contents. With the macro facility, several FORCEbug/386 commands can be combined in one command name and then executed together. Upload and download of user application programs supports both Intel Hex or Motorola S-records. The upload/download facilities of FORCEbug/386 may then be used to transfer binary program and data between a CPU-386 serial I/O port and a host system serial I/O port.

FORCEbug/386 requires 64 Kbyte of EPROM space, and resides in four 27128 EPROMS. Additionally, approximately 8 Kbyte of read/write memory are used by FORCEbug/386 for vector, parameter and macro storage.

3. Software

It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-386 Software Support

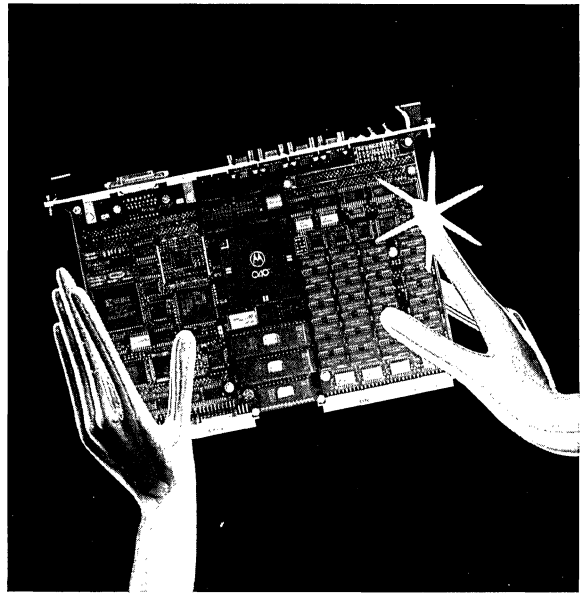
Operating System/Kernel	Vendor/Support
UNIX V.3/V.4	Contact FORCE for availability
OS-9/9000	Contact FORCE for availability
VxWORKS	Contact FORCE for availability
VRTX-32	Contact FORCE for availability
pSOS	Contact FORCE for availability
ARTX	Contact FORCE for availability

Specifications

CPU/FPCP		80386/80387
Clock frequency		16 MHz
On-board DRAM No. of wait states Byte parity	CPU-386A CPU-386C	2 Mbyte 8 Mbyte 0 yes
Used EPROM Sockets		Four 28-pin JEDEC
EPROM Capacity (Max)		512 Kbyte
Serial I/O interfaces		3 RS-232 (2 Multi-mode)
VMEbus Interface A32, A24, A16 : D8, D16, D32, UAT, RMW		Master
VMEbus interrupts (Software-selectable)	Maskable Non-Maskable Autovector option for	IRQ1-IRQ6 IRQ7 IRQ1, IRQ3, IRQ5
4-level Arbiter	Round Robin Prioritized Single Level	yes yes yes
RESET & ABORT Switches		yes
FORCEbug/80386 Firmware		yes
Power requirements	+ 5 V max + 12 V max – 12 V max	6.0 A 0.3 A 0.3 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)		0 to + 50 °C – 40 to + 85 °C 5 to 95 %
Board dimensions		234 × 160 mm : 9.2 × 6.3 in
No. of VMEbus slots required		1

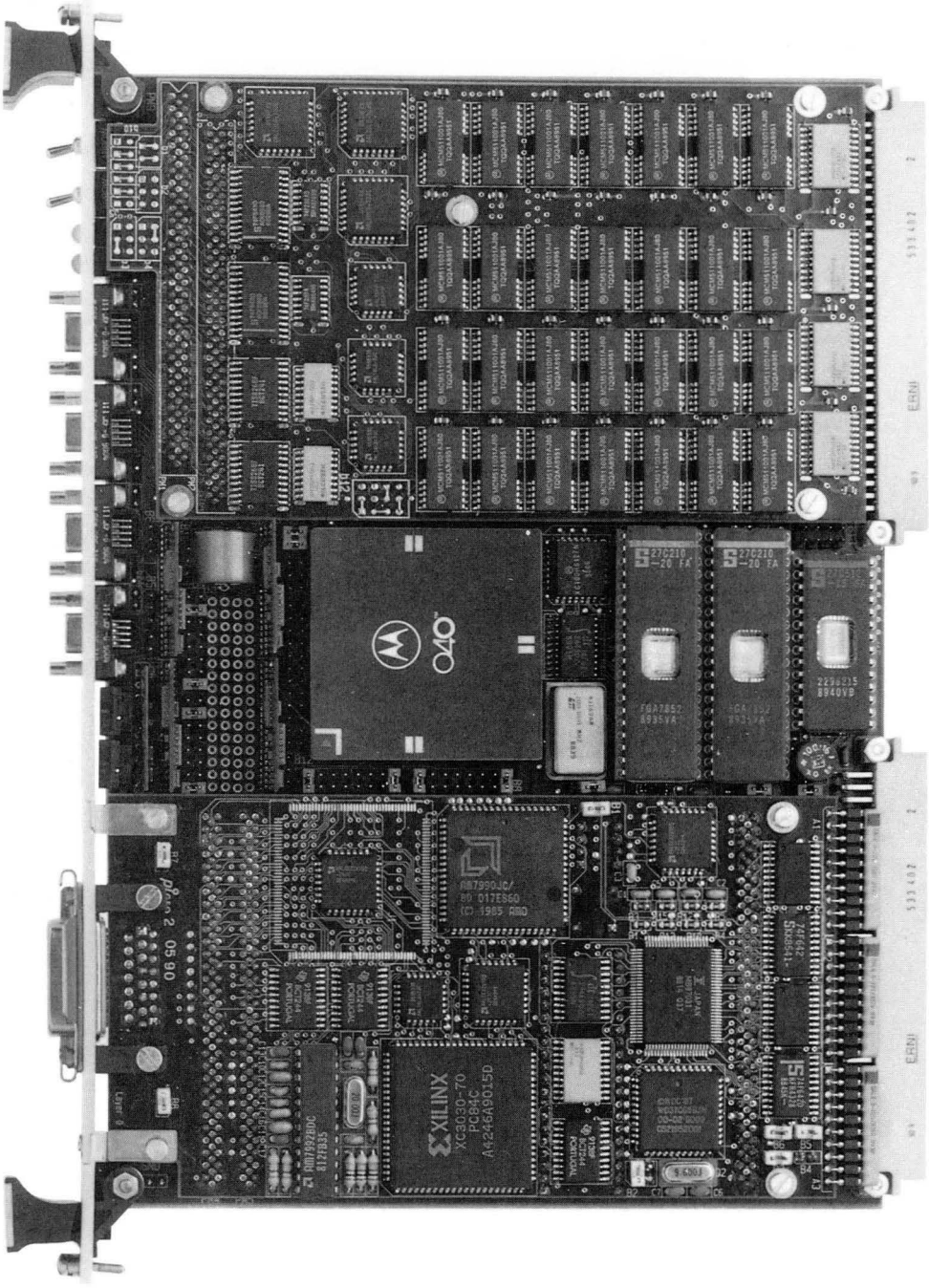
Ordering Information

SYS80K/CPU-386A Part No. 105001	80386 CPU board with 80387 numeric co-processor at 16 MHz clock frequency and 2 Mbyte of zero wait state RAM including documentation and FORCEbug/386 debugger firmware.
SYS80K/CPU-386C Part No. 105003	80386 CPU board with 80387 numeric co-processor at 16 MHz clock frequency and 8 Mbytes of zero wait-state RAM including documentation and FORCEbug/386 debugger firmware.
SYS80K/CPU-386/UM Part No. 800500	User's manual for all CPU-386 versions.



System 68000 VME SYS68K/CPU-40

High Performance Multi-Purpose 68040 CPU Board with Shared Memory, DMA and FLXi

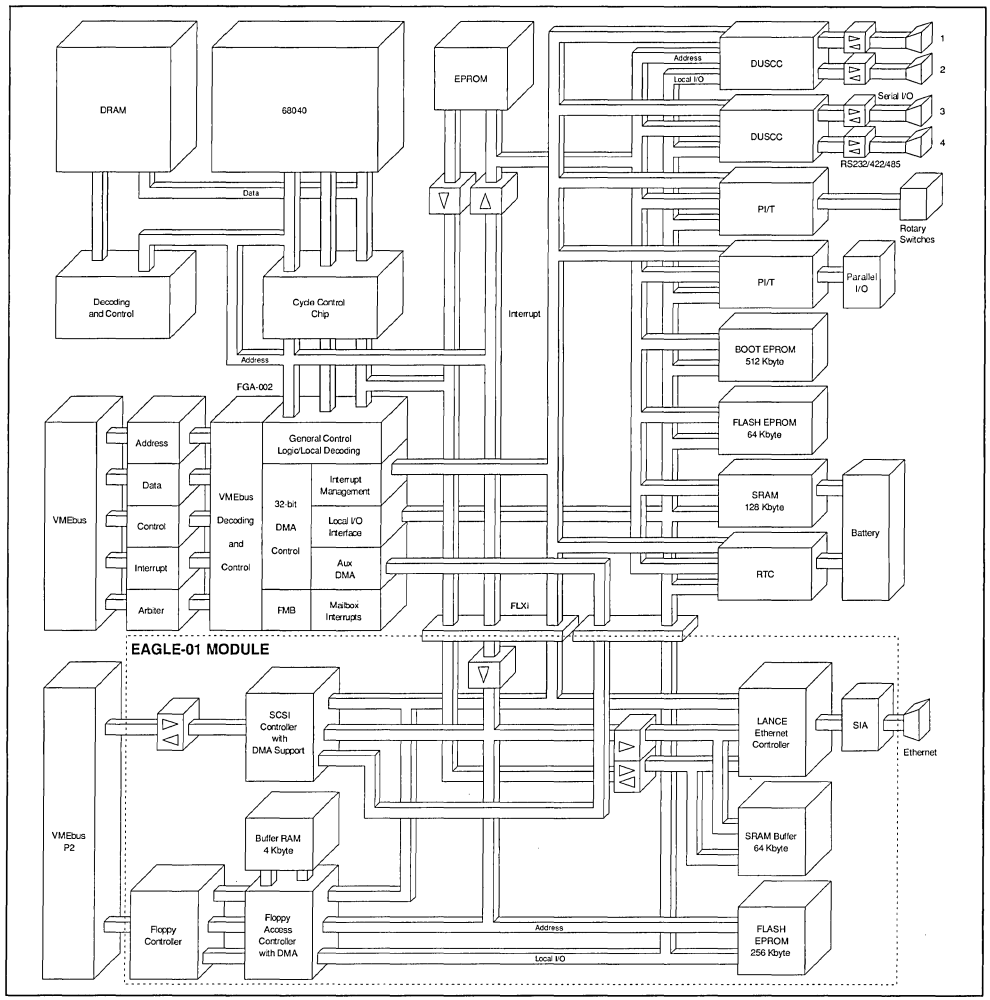

040
XILINX
XC3030-70
PC84C
A4246A9015D
27C210
-20 FA
ETHERNET

General Description

The SYS68K/CPU-40 is a high performance CPU-board based on the 68040 microprocessor and the VMEbus. The board incorporates a modular I/O subsystem which provides a high degree of flexibility for a wide variety of applications. The CPU-40 can be used with or without an I/O subsystem, called an "EAGLE" module, and all of the EAGLE modules offered by FORCE COMPUTERS are fully compatible with the CPU-40. The board is available with 4 Mbyte and 16 Mbyte shared DRAM options, both with byte parity, as well as a 4 Mbyte SRAM option (SYS68K/CPU-41). The CPU-40 family design utilizes all of the features of the powerful FORCE Gate Array (FGA-002). Among its features is a 32-bit DMA controller which supports local (shared) memory, VMEbus and I/O data transfers for maximum performance, parallel real time operation and responsiveness.

The EAGLE modules are installed on the SYS68K/CPU-40 via the FLXi (FORCE Local

Block Diagram of the SYS68K/CPU-40



eXpansion interface). This provides a full 32-bit interface between the base board and the EAGLE module I/O subsystem, providing a range of I/O options.
Four multi-protocol serial I/O channels, a parallel I/O channel and a Real Time Clock with on-board battery back-up are installed on the base board which, in combination with EAGLE modules, make the SYS68K/CPU-40 a true single board computer system.
A broad range of operating systems and kernels is available for the CPU-40. However, as with all FORCE COMPUTERS' CPU cards, VMEPROM firmware is provided with the board at no extra cost. VMEPROM is a Real Time Kernel and is installed on the CPU-40 in the two 32-bit wide EPROM sockets, ensuring that the board is supplied ready to use.

Features of the SYS68K/CPU-40

- 68040 microprocessor:
  25.0 MHz on CPU-40B/x
  33.0 MHz on CPU-40D/x
- Shared DRAM :
  4 Mbyte on CPU-40x/4
  16 Mbyte on CPU-40x/16
- All DRAM modules support full byte parity and the burst fill mode of the 68040. The DRAM is accessible from the local 68040 microprocessor as well as from the VMEbus (Shared RAM)
- 32-bit high speed DMA controller for data transfers to/from the shared RAM, VMEbus memory and EAGLE modules; DMA controller is installed in the FGA-002
- Two system EPROM devices supporting 40-pin devices. Access from the 68040 using a 32-bit data path
- One boot EPROM for local booting, initialization of the I/O chips and configuration of the FGA-002
- 128 Kbyte SRAM with on-board battery back-up
- 64 Kbyte FLASH EPROM
- FLXi interface for installation of one EAGLE module
- Four Serial I/O interfaces, configurable as RS232/RS422/RS485, available on the front panel
- 8-bit parallel interface with 4-bit handshake
- Two 24-bit timers with 5-bit prescaler
- One 8-bit timer
- Real Time Clock with calendar and on-board battery back-up
- Full 32-bit VMEbus master/slave interface, supporting the following data transfer types:
  – A32, A24, A16 : D8, D16, D32 – Master
  – A32, A24 : D8, D16, D32 – Slave
  – UAT, RMW, ADO
- FORCE Message Broadcast (FMB), two channels
- Four-level VMEbus arbiter
- SYSCLK driver
- VMEbus interrupter (IR 1-7)
- VMEbus interrupt handler (IH 1-7)
- Support for ACFAIL* and SYSFAIL*
- Bus time-out counters for local and VMEbus access (15 µsec)
- VMEPROM, Real Time Multi-tasking Kernel with monitor, file manager and debugger

1. Hardware Description

1.1 68040 Overview

The 68040 integrates a 68020/030-compatible microprocessor core, a 68881/2-compatible concurrent floating point core, separate 4 Kbyte instruction and data caches and a dual paged memory management unit on one VLSI device. The 68040 is a full 32-bit implementation of the 68000 architecture, with a high speed 32-bit data path, instruction pipeline, and bus interface. The implementation of the 68040 has been optimized to minimize instruction execution time for compiler generated code.

Features of the 68040 at 25/33 MHz

- 19/25 MIPS sustained integer unit
- 3.6/4.7 MFLOPS concurrent Floating Point Unit
- Flexible high bandwidth synchronous bus
- 68020/68030-compatible integer unit
- 68881/68882-compatible floating point execution unit
- Independent data and instruction memory management units
- Dual 4 Kbyte on-chip caches for instructions and data
- Multimaster/multi-processor support via bus snooping
- 4 Gbyte addressing range
- Upward user object code compatible with the 68020/030 and 68881/2

1.2 The Shared RAM

The CPU-40 design uses memory modules for maximum flexibility of memory type and size. All modules provide a memory which is shared by the 68040 microprocessor and the VMEbus. The CPU-40 provides the user with DRAM and the CPU-41 will offer an SRAM option.

1.2.1 The Shared DRAM

The main memory area of the CPU-40 is installed on a DRAM memory module which is populated with 1 Mbit or 4 Mbit capacity devices to provide 4 Mbyte or 16 Mbyte of main memory respectively. The memory module contains all the memory decoding logic, DRAM control logic, refresh generation, byte parity generation and checking, as well as address multiplexers/ drivers.

The DRAM modules fully support the burst fill mode of the 68040 microprocessor. This enables 16 bytes of data to be read or written in 8 microprocessor clocks at both 25 MHz and at 33 MHz (5 clocks for the first cycle and 1 clock for each of the three subsequent cycles of a burst fill). This gives an effective memory bandwidth of 50 Mbyte/sec at 25 MHz using the burst fill mode and 32-bit access. Using a 33 MHz processor, the memory bandwidth is 66 Mbyte/sec. The data path for 25 and 33 MHz frequency options is 32 (+ 4) bits wide.

Memory modules supporting 128-bit wide data paths will be used to support the planned higher frequency versions of the 68040 microprocessor. This will effectively increase the memory bandwidth of microprocessors operating at, or above, 40 MHz, which would otherwise be limited due to access times offered by current RAM technology.

The start and end VMEbus access addresses to the shared RAM are programmable in 4 Kbyte increments via the FGA-002. The defined memory range can be write-protected in combination with the address modifier codes. For example, the FGA-002 may be programmed so that, in supervisor mode, the memory may be read or written from the VMEbus while, in user mode, it may only be read. The read/write protection mechanism is fully under the user's software control.

The DRAM is accessed from the VMEbus by requesting the local bus from the local arbiter via the FGA-002. When the local arbiter has granted local bus mastership to the FGA-002, the access cycle is executed. On completion of the read/write cycle, the FGA-002 immediately releases bus mastership to the microprocessor while completing the VMEbus cycle asynchronously. This early completion of VMEbus read/write cycles effectively halves the overhead to the microprocessor for an external access.

1.2.2 The Cycle Control Chip

The installation of a specially designed gate array, called a Cycle Control Chip (CCC), enables the 68040 to "snoop" VMEbus accesses to the shared RAM. The CCC gate array translates the dynamic bus sizing of the 68020 and 68030 microprocessors into allowed and supported 68040 bus cycles. All cycles translated by the CCC can be snooped by the 68040.

The CCC also allows the single 8-bit wide SRAM and EPROM to be seen as 32-bit wide contiguous memory by the 68040. The CCC initiates 4 (or 2) individual read or write cycles for each long word (or word) transfer. Because all 4 (or 2) bytes are stored in the CCC, a 32-bit acknowledge signal is presented to the 68040.

Furthermore, the CCC handles accesses to the I/O devices and preserves I/O software drivers written for the 68020 or 68030 microprocessors. Since the 68040 is only able to access I/O devices in increments of 4 bytes, the CCC has been designed to allow I/O devices to reside on a 2 byte boundary but still be compatible with the 68040. This feature ensures full software upward compatibility with 68020 or 68030 based board designs from FORCE COMPUTERS.

1.2.3 The Shared SRAM

Since main memory is installed on a module, an SRAM version of the CPU-40 family can readily be made available. Called the CPU-41, the SRAM card will become available during the second half of 1991. However, since the CPU-40 and CPU-41 have identical base boards and can both use the same EAGLE modules, software development for applications requiring SRAM can begin immediately, using a CPU-40, and the code can then be transferred to the CPU-41 at a later date without any changes.

The first CPU-41 will offer 4 Mbyte of SRAM and will provide a 128-bit wide memory organisation. The SRAM can be battery backed via the + 5 V

STDBY line of the VMEbus enabling full data retention during power down and/or power failures. With this feature, the CPU-41 is particularly suited to industrial applications.

1.3 The DMA Controller

A high speed 32-bit DMA controller is installed on the SYS68K/CPU-40 inside the FGA-002. DMA execution on the VMEbus is performed without any degradation in performance of the local microprocessor. The DMA controller runs fully independently of the 68040 microprocessor and is able to perform transfers to/from the shared RAM, to/from the VMEbus, and to/from the EAGLE modules connected to the FLXi.

To increase the data throughput, the DMA controller uses a 32-byte FIFO for internal data storage. The read and write operations are executed in bursts of eight cycles, 4 byte at a time. The result is that only eight read cycles followed by eight write cycles are required to transfer 32 byte of data.

The 32 byte FIFO as well as the parallel architecture of the CPU-40 enables the microprocessor to operate in parallel to the DMA controller during data transfers. For example, during VMEbus DMA transfers, the microprocessor can access all local I/O devices, the EPROM area and the shared RAM without any performance degradation. In addition, the DMA controller is connected to the FLXi, allowing fast data transfers between EAGLE modules and the shared RAM or VMEbus memory. The DMA controller supports aligned and unaligned data transfers. The internal control logic first aligns the data transfers to take full advantage of the 32-bit structure of the VMEbus and the shared RAM.

1.4 The FORCE Local eXpansion interface

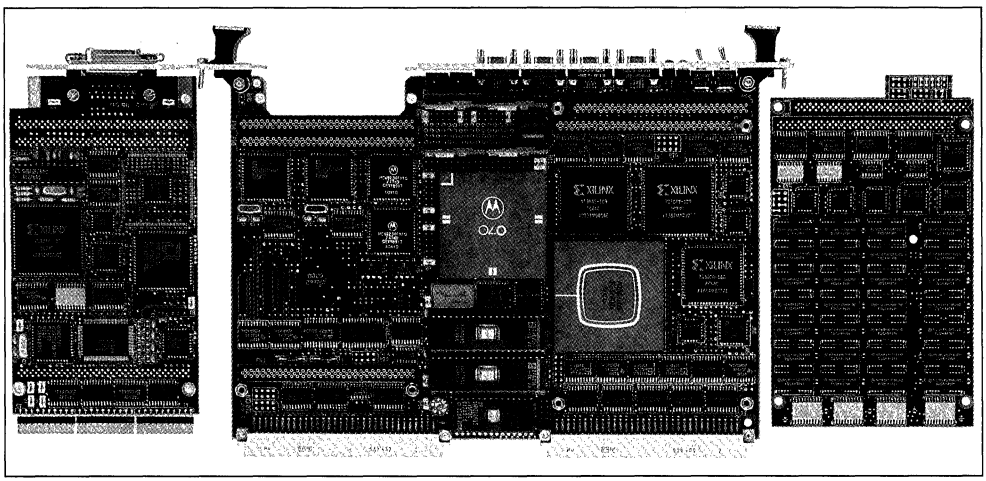
The FORCE Local eXpansion interface (FLXi) is installed on the SYS68K/CPU-40. The FLXi provides the following interfaces from the SYS68K/CPU-40 board to the EAGLE module:

- 32-bit data and address bus for standard microprocessor and DMA access using 68020 compatible bus timing and dynamic bus sizing
- Direct connection to the 64 user I/O pins on the VMEbus P2 connector

The FLXi is a connector interface which allows the installation of one EAGLE module. The interface and the EAGLE modules are designed to allow a complete SYS68K/CPU-40 and EAGLE module solution to occupy only one VMEbus slot. When installed, the EAGLE module's front panel becomes part of the SYS68K/CPU-40's front panel.

The FLXi allows the EAGLE module to access the resources of the base board in addition to the 68040 on the base board being able to access the resources on the EAGLE module.

SYS68K/CPU-40 with EAGLE-01 and Memory Module



1.5 The Local SRAM

128 Kbyte SRAM with on-board battery back-up is installed on all SYS68K/CPU-40 board versions. This supports data storage during power-down phases for at least one year. The SRAM is directly connected to the I/O interface of the FGA-002 VMEbus.

1.6 The FLASH EPROM

64 Kbyte FLASH EPROM is included on the base board of the CPU-40 which can be used as additional data back-up under conditions of power down for long periods. FLASH EPROM is ideal to hold details of the board status, such as software revision or user data which is to be kept permanently.

1.7 The System EPROMs

The SYS68K/CPU-40 offers two 40-pin EPROM sockets for the installation of two 16-bit wide EPROM devices. The EPROMs operate with a 200 ns access cycle time and therefore a data throughput of 20 Mbyte/sec. The EPROMs present a full 32-bit data path to the processor, enabling maximum performance.
The following devices are supported in the system EPROM area:

Organization	Total Capacity
64 K × 16	256 Kbyte
128 K × 16	512 Kbyte
256 K × 16	1 Mbyte

1.8 The Boot EPROM

The SYS68K/CPU-40 board contains, in addition to the two system EPROMs, a single boot EPROM to boot the local microprocessor, initialize all I/O devices and program the board-dependent functions of the FGA-002. All basic initialization of the I/O devices and the FGA-002 are made through the boot EPROM.
In addition, the boot EPROM contains user utility routines, which may be called out of the user's application program. These routines provide easy software access to the functionality of the FGA-002 (DMA controller, FORCE Message Broadcast, Interrupt Management, etc.).

1.9 The Serial I/O Interfaces

Two Dual Universal Serial Communication Controllers (DUSCC 68562) are installed on the SYS68K/CPU-40 to provide serial communication to other parts of the user's system.

Features of the DUSCC

- Dual full-duplex synchronous and asynchronous receiver and transmitter (programmable)
- Multi-protocol operation enabling support of bit or character-oriented protocols. With additional software, this allows the support of HDLC, SDLC, X.25, X.75, BISYNC, etc.

All four channels are routed to the 9-pin micro D-sub connectors on the front panel. The CPU-40 is supplied with all four serial I/O channels connected to RS232-compatible socketed hybrid drivers/receivers. All channels can be individually configured for RS422/485 compatibility by simply exchanging the hybrid modules. The DUSCCs can interrupt the local microprocessor on a software-programmable level (1 to 7).
To support synchronous communication, a jumper field is provided to allow the user to connect TxClk and RxClk to the 9-pin connectors.
An adapter cable is provided with the CPU-40 to enable connection to the 9-pin micro D-sub connectors.

1.10 The Real Time Clock

A software-programmable Real Time Clock (RTC 72423) with on-board battery back-up is installed on the SYS68K/CPU-40 boards. Battery back-up ensures continued operation of the RTC for at least one year after power-down.

Features of the Real Time Clock

- Time of day and date counter included (year, month, week, day)
- Built-in quartz oscillator
- 12 hr/24 hr clock switch-over
- Automatic leap year setting
- CMOS design provides low power consumption during power-down mode

1.11 The Parallel Port

The 12-bit I/O port is routed to a 24-pin header which allows the connection of a flat cable. 8 bits are connected to port A of a PI/T (Parallel Interface and Timer MC68230) and can be used as

inputs or outputs, the remaining 4 bits are connected to the handshake pins of the PI/T. This port can be used for parallel I/O applications such as a Centronics-compatible printer interface.

1.12 The Timers

A total of three independent timers are available for the user. These timers offer maximum flexibility because each timer can be used to force an interrupt to the microprocessor on a software-programmable IRQ-level (1 to 7). The first two timers are 24-bit with individual 5-bit prescalers. The third timer can be used to generate interrupts to the microprocessor and the SYSFAIL* signal to the VMEbus. It can also be used to act as a watchdog. This timer is an 8-bit timer with a programmable source clock divider installed in the gate array (FGA-002). SYSFAIL* can be used in multi-processor systems to signal that one board has detected a failure. It is asserted if the watchdog timer is not regularly reset. The reset time interval to prevent SYSFAIL* being asserted is fully softwareprogrammable.

2. The EAGLE Modules

EAGLE modules are I/O subsystems designed not only to increase the functionality of the board but to add the exact I/O features to fit the application requirement. EAGLE modules connect directly onto the FLXi of the base board. FLXi and EAGLE modules will be a feature on future FORCE board generations to ensure continued flexibility.

2.1 The EAGLE-01

The EAGLE-01 connects to the FLXi on the base board. This I/O subsystem module provides disk and networking support to complement the features of the base board.

Features of EAGLE-01

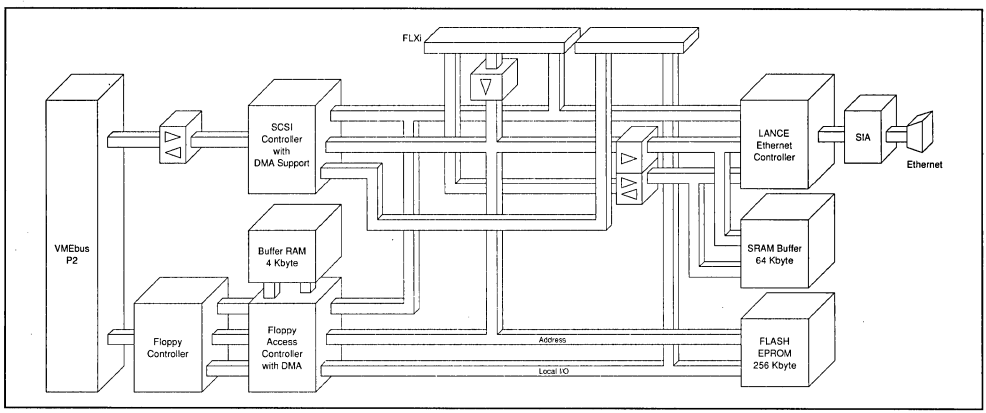
- SCSI controller, 87031 connected to 8-bit DMA interface of the FGA-002
- Floppy Disk Controller 37C65 with dedicated 4 Kbyte sector buffer
- Local Area Network Controller 7990 providing a complete Ethernet interface
- 64 Kbyte SRAM for buffering Ethernet packets
- 256 Kbyte FLASH EPROM containing all firmware for the control of the functional I/O units on the EAGLE-01

2.1.1 The SCSI Interface

The 87031 SCSI controller is installed on the EAGLE-01 to interface directly to SCSI Winchester disks, optical disk drives, tape streamers or any other SCSI-compatible device. The 8-bit DMA channel of the SCSI controller is directly connected to the DMA controller inside the FGA-002.

The I/O signals of the single-ended SCSI interface are provided directly on the VMEbus P2 connector of the base board and are fully compatible to the assignment of the SYS68K/IOBP-1 (Input/Output Back Panel) for interconnection to mass memory devices.

Block Diagram of the EAGLE-01



Features of the 87031 SCSI Controller

- Full support for SCSI control
- Service of either initiator or target device
- 8-byte data buffer register incorporated
- Transfer byte counter (24-bit)
- Independent control and data transfer bus

2.1.2 The Floppy Disk Interface

The 37C65, installed on the EAGLE-01, provides the interface between the CPU-40 and a floppy disk drive. The architecture incorporates a buffer memory and a DMA controller to ensure maximum performance and minimum degradation of the real time responsiveness of the board at all times. A DMA controller is housed in a gate array which is installed on EAGLE-01 and performs DMA transfers between the 37C65 and the 4 Kbyte sector buffer memory. The sector buffer is a shared RAM between the Floppy Disk Controller and the 68040. This architecture allows the microprocessor to function at full performance without being affected by floppy disk transfers.
The floppy disk controller fully supports double density and high density floppy media on up to four 3", 3½" and 5¼" drives.
The floppy interface is routed through FLXi to the VMEbus P2 connector of the base board and is fully compatible to the SYS68K/IOBP-1 interconnection pin assignment.

2.1.3 The Ethernet Controller

The chip set used provides conformance to the IEEE 802.3 Ethernet Interface Standard. This allows, with additional software, the support of higher level Local Area Network (LAN) communication protocols.

Features of the 7990 Ethernet Interface

- Compatible with IEEE 802.3 Rev.0
- On-chip DMA and buffer management
- 48-byte FIFO
- 24-bit wide linear addressing
- Network and packet error reporting
- Back-to-back reception with as little as 4.1 µsec inter-packet gaptime
- Diagnostic routines

The LAN functional module includes a dedicated 64 Kbyte buffer memory for Ethernet data transfers. This buffer is a shared memory array, allowing access from both the 7990 and from the local microprocessor. This 64 Kbyte buffer stores outgoing or incoming data packets until either the system is ready to allow data transmission from the CPU-40 mode or the CPU-40 is ready to process the incoming data.
An incoming data packet is transferred to the buffer memory under control of the DMA controller contained within the 7990. The presence of the data is flagged to the 68040 via an interrupt and the application software determines when the packet should be transferred from the buffer memory. This transfer is then achieved by the DMA controller inside the FGA-002. An outgoing packet is transferred into the buffer memory by the FGA-002 DMA controller or by the 68040. The 7990 DMA controller then transfers the data out again when it is ready to transmit onto the network.
The benefit of this architecture is that the microprocessor and the Ethernet controller can operate in parallel which maintains the full real time capability of the board in an Ethernet environment.
The Ethernet interface is available on a standard 15-pin D-sub transceiver connector routed to the front panel of the board. The Ethernet mode address is programmed into the FLASH EPROM installed on the EAGLE-01 module.

2.1.4 The FLASH EPROM

256 Kbyte FLASH EPROM is installed on the EAGLE-01 module to contain the low level drivers of the module's I/O devices. FLASH EPROM ensures easy maintenance and update of software since code can be erased and re-programmed without having to remove the board from the system. FLASH EPROMs do not have to be removed from the board to be re-programmed. It is even possible to change or load code remotely via a network or even a telephone line, saving the need for costly down-time or service visits.

2.1.5 The Parallel Architecture

The parallel architecture of the SYS68K/CPU-40 together with the EAGLE-01 ensures the maintenance of full real time capability, even if numerous I/O transfers have to be performed whilst the microprocessor fulfils number crunching tasks. This is achieved by implementing different independent data transfer paths with

dedicated DMA support on the single board system. For example, DMA transfers to/from floppy disk, Ethernet or SCSI are fully asynchronous and independent of each other. During DMA transfers from all devices, the 68040 has full access to the shared RAM and the VMEbus. The full Real Time Responsiveness (RTR) of the 68040 is maintained.
The following table shows the 68040 performance during DMA transfers with an EAGLE-01 installed:

Transfer to/from	Transfer from/to	CPU Performance
VMEbus	SCSI	100 %
VMEbus	Floppy Disk Buffer	> 80 %
VMEbus	Ethernet Buffer	> 65 %
Shared RAM	SCSI	> 90 %
Shared RAM	Ethernet Buffer	> 65 %

2.2 Additional EAGLE Modules

The flexible architecture of the SYS68K/CPU-40 also allows the installation of other EAGLE modules on the FLXi. Several standard EAGLE modules are being made available by FORCE COMPUTERS to offer various I/O options such as VSB interface or high speed serial I/O (X.25). However, the EAGLE module concept is intended to adapt any FORCE board incorporating the FORCE Local eXpansion interface to the particular application environment. In order to shorten design times of EAGLE modules, and to allow easier customer EAGLE module development, FORCE COMPUTERS is designing a custom device, the I/O Controller (IOC), to interface directly between the FLXi and module based I/O devices. This chip is numbered the FC68165 and will be made available for application-specific EAGLE module design during the first half of 1991.

3. The Memory Map

Start Address	End Address	Type
00000000	00FFFFFF	Shared Memory (16 Mbyte)
01000000	F9FFFFFF	VMEbus Addresses (16 Mbyte) A32 : D32, D24, D16, D8
FA000000	FAFFFFFF	Message Broadcast Area (Slave and Master Mode)
FB000000	FBFEFFFF	VMEbus, A24 : D32, D24, D16, D8
FBFF0000	FBFFFFFF	VMEbus, A16 : D32, D24, D16, D8
FC000000	FCFEFFFF	VMEbus, A16 : D16, D8
FCFF0000	FCFFFFFF	VMEbus, A16 : D16, D8
FD000000	FEFFFFFF	Reserved
FF000000	FF7FFFFF	System-EPROM
FF800000	FFBFFFFF	Local I/O
FFC00000	FFC7FFFF	Local SRAM
FFC80000	FFCFFFFF	FLASH EPROM
FFD00000	FFDFFFFF	Registers of FGA-002
FFE00000	FFEFFFFF	Boot EPROM
FFF00000	FFFFFFFF	Reserved
FF800C00	FF800DFF	PI/T 1
FF800E00	FF800FFF	PI/T 2
FF802000	FF8021FF	DUSCC 1
FF802200	FF8023FF	DUSCC 2
FF803000	FF8031FF	RTC-1

4. The VMEbus Interface

The SYS68K/CPU-40 has a full 32-bit VMEbus interface. The address modifier codes for A16, A24 and A32 addressing are fully supported in master mode. In slave mode, the address modifiers for A32 and A24 are fully supported.
Read-Modify-Write cycles are fully supported to allow multiple CPU boards to be synchronized via the shared RAM. The FGA-002 determines whether or not an access to the shared RAM is allowed and, if allowed, controls the access cycle.
The CPU-40 provides an interrupt handler capability (IH 1-7) which can be enabled/disabled by programming the FGA-002. The CPU-40 also provides an interrupter function which enables the board to send interrupts to the VMEbus on seven programmable levels with a software-programmable vector.
The following bus release modes are supported:

RWD	=	Release When Done
ROR	=	Release On Request
RBCLR	=	Release On Bus Clear
RAT	=	Release After Timeout
REC	=	Release Every Cycle
ROACF	=	Release on ACFAIL*

Each of the listed modes is software-programmable inside the gate array. The bus request level of the SYS68K/CPU-40 is jumper-selectable (BR0-3*).
The DMA controller installed in the FGA-002 on the SYS68K/CPU-40 is able to access the VMEbus interface independently from the microprocessor, enabling VMEbus communication to take place without impacting the processing capabilities of the rest of the board for number crunching or servicing on-board I/O.
A four level arbiter with round robin and prioritized round robin arbitration modes, a power monitor, a SYSRESET* generator, IACK* daisy-chain driver and support for ACFAIL*, SYSFAIL* and SYSCLK complete the VMEbus interface.

5. The Interrupt Structure

The gate array installed on the SYS68K/CPU-40 handles all local and VMEbus interrupts. All interrupt requests from the local bus, the DUSCC, the two timers, as well as the gate array specific interrupt requests, are combined with the seven VMEbus IRQs by the FGA-002. Interrupts from the FLXi are also channelled through the FGA-002.
The FGA-002 can be programmed by the user to prioritize interrupts from any source and then to interrupt the microprocessor on any interrupt level (1 to 7).
The gate array supplies the vector, or initiates an interrupt vector fetch from the I/O device depending on the programmed configuration of the FGA-002 or from the VMEbus. This process is fully under the control of the application.

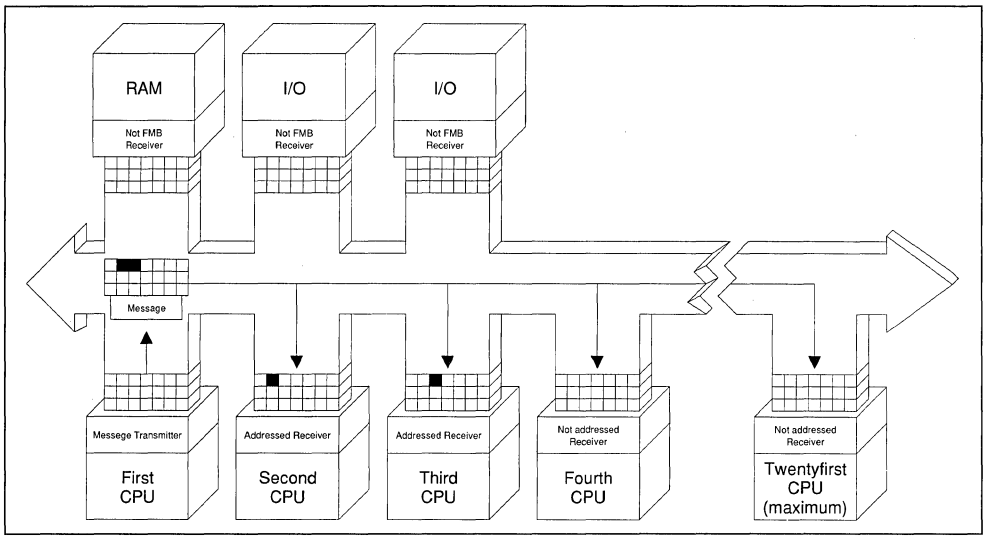
6. The Multi-Processor Mailboxes

The SYS68K/CPU-40 includes eight multi-processor mailboxes. Each of these allows an interrupt to be generated to the local 68040 microprocessor. The interrupt level of each multi-processor mailbox is software-programmable and an individual interrupt vector for each mailbox may be passed to the microprocessor.
This function allows the triggering of an interrupt on the SYS68K/CPU-40 from multiple masters on the VMEbus. The mailboxes are accessed via RMW access, thus allowing multiple masters on the VMEbus to share the same mailbox channel.

7. FORCE Message Broadcast

The FORCE Message Broadcast (FMB) is a fast and effective mechanism to communicate with and to synchronize up to 20 CPU boards in a VMEbus system in only one VMEbus write cycle. It offers a unique support feature for building multi-processing systems based on the VMEbus. An FMB transfer is a standard VMEbus write cycle and complies fully to the IEEE 1014 Specification. Any VMEbus master may be a message transmitter. The transmitter decides which boards in the system should be addressed (one, two or up to twenty boards) and writes the message to a specific address.
All addressed boards receive the message at the same time and generate an interrupt request on a programmable level to their local microprocessor. This ensures that there is no time delay between the synchronization of different boards in the system. The ability to communicate with and synchronize multiple CPUs in the system by the FMB mechanism allows the VMEbus to be used in a wide range of application areas, particularly multi-processor environments.

Block Diagram of the FORCE Message Broadcast (FMB)



Without the FMB mechanism, communication between and synchronisation of system boards has to be managed via the seven interrupt request lines. FMB reduces the massive time overhead normally needed to process the interrupt cycles to just one write cycle.
All FORCE VME/PLUS boards provide two fully independent message broadcast channels. Channel 0 stores 8-bit messages in an eight stage deep FIFO, channel 1 stores one 8-bit message and can therefore be used for high priority messages.

8. The I/O Back Panel

To simplify connection of its single board computers within system environments, FORCE COMPUTERS also offers a SYS68K/IOBP-1 which splits the pins of the VMEbus P2 connector of the VMEbus backplane into 2 cables with industry standard connectors. The IOBP-1 is compatible with the pin-out of all FORCE CPU cards. IOBP-1 directly connects to the I/O pins of the P2 connector of the VMEbus backplane and routes them via two ribbon cables to flat connectors. The first connector connects a standard SCSI flat cable with full support for the ground shield. The second is used to interface directly to floppy disk drive(s), and also fully supports the ground shield.

9. Software

It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-40 Software Support

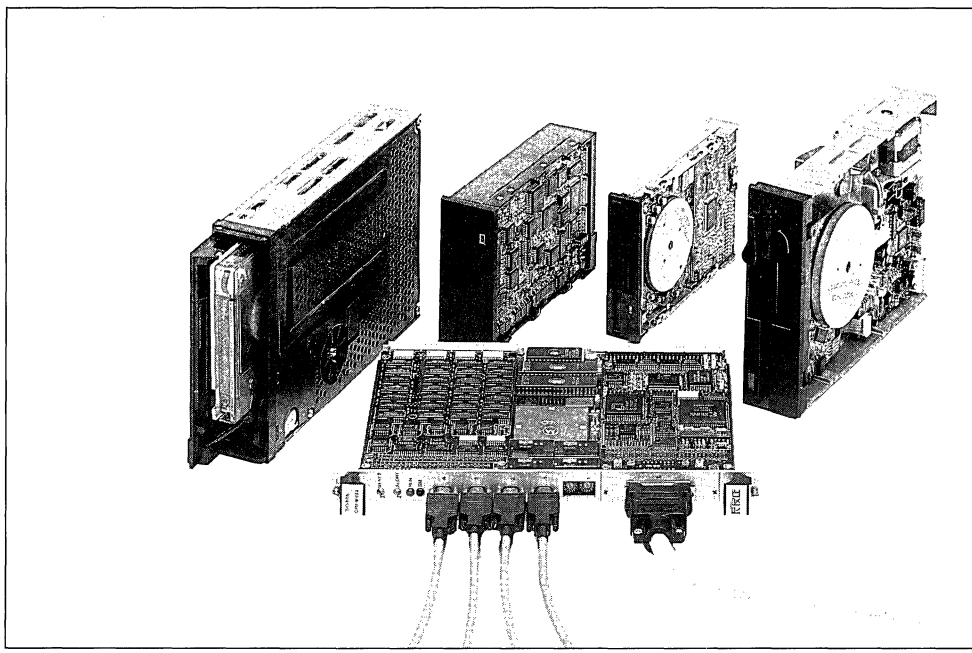
Operating System/Kernel	Vendor/Support
UNIX V.4	FORCE COMPUTERS
PDOS	FORCE COMPUTERS
VMEPROM	FORCE COMPUTERS
OS-9	FORCE COMPUTERS/MICROWARE
VRTX-32	READY SYSTEMS
VxWORKS	FORCE COMPUTERS/ Wind River Systems
pSOS	Software Components Group

As a courtesy, FORCE provides the user with the ability to immediately start a real time application by including VMEPROM on every CPU card, free of charge and free of licensing costs.
VMEPROM is an EPROM-based Real Time Multi-tasking Kernel/Monitor. The complete package resides in 256 Kbyte of EPROM and uses 32 Kbyte of RAM. VMEPROM fully supports all of the on-board I/O devices.
VMEPROM is composed of a highly sophisticated Real Time Kernel, which is based on the PDOS Real Time Kernel. A file manager supporting sequential, random and shared files is also included.
The user interface contains more than 60 commands perfectly suited for program debugging, host computer communications, as well as task and file management. It includes a powerful debugger, supporting line assembler/disassembler for the microprocessor.

Features of VMEPROM

- Real Time Kernel supporting multi-tasking, up to 64 tasks
- File manager, supporting up to 64 open files at the same time
- Line assembler/disassembler with full support of all 680x0 instructions
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify
- S-record up/downloading from any port defined in the system
- Disk support for RAM disk, floppy and Winchester disks
- VMEPROM allows disk formatting and initialization
- Serial I/O support for up to two SIO-2 or ISIO-2 boards in the system; local serial I/O devices are also supported
- EPROM programming utility using the SYS68K/RR-2 board
- Full screen editor
- I/O re-direction to files or ports from the command line
- Over 100 system calls to the kernel

SYS68K/CPU-40 and Mass Memory Devices



Specifications

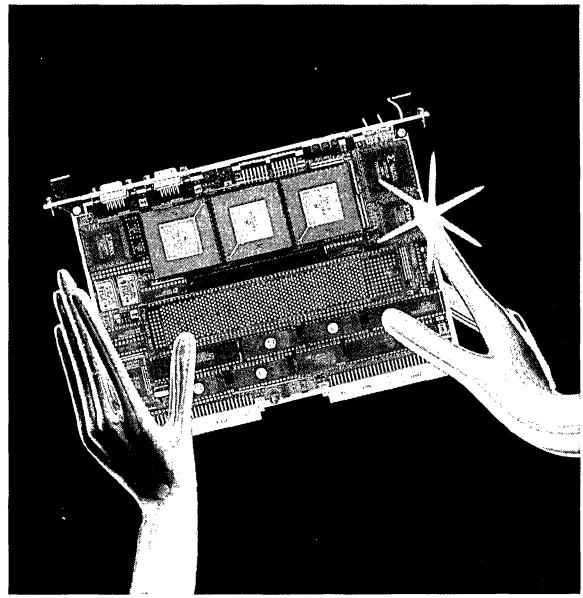
Function		
CPU type		68040
CPU clock frequency	CPU-40B/X CPU-40D/X	25.0 MHz 33.0 MHz
Shared DRAM capacity with parity	CPU-40X/4 CPU-40X/16	4 Mbyte 16 Mbyte
SRAM capacity with on-board battery back-up FLASH EPROM		128 Kbyte 64 Kbyte
No. of system EPROM sockets Data path		2 32-bit
Serial I/O interfaces (68562) RS232/422/485-compatible		4 4 of 4
24-bit timer with 5-bit prescaler 8-bit timer		2 1
Parallel I/O interface (68230)		12 lines
Real Time Clock with on-board battery back-up		72423
VMEbus interface	A32, A24, A16 : D8, D16, D32, UAT, RMW A32, A24 : D8, D16, D32, RMW	Master Slave
Four-level arbiter SYSCLK driver Mailbox interrupts		yes yes 8
FORCE Message Broadcast	FMB-FIFO 0 FMB-FIFO 1	8 byte 1 byte
VMEbus interrupter/VMEbus and local interrupt handler All sources can be routed to a software-programmable IRQ-level		1 to 7 yes
RESET/ABORT switch		yes
VMEPROM firmware installed on all board versions		256 Kbyte
Power requirements	+ 5 V min : max + 12 V min : max – 12 V min : max	5.2 A : 6.0 A 0.1 A : 0.3 A 1.0 A : 0.3 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing) Board dimensions No. of slots used		0 to + 50 °C – 40 to + 85 °C 5 to 95 % 234 × 160 mm : 9.2 × 6.3 in 1

EAGLE-01 Specifications

No. of slots when used with CPU-40	1
Ethernet interface Ethernet SRAM	AM7990 64 Kbyte
SCSI Interface (87031)	Single-ended
Floppy disk interface (37C65)	SA 460

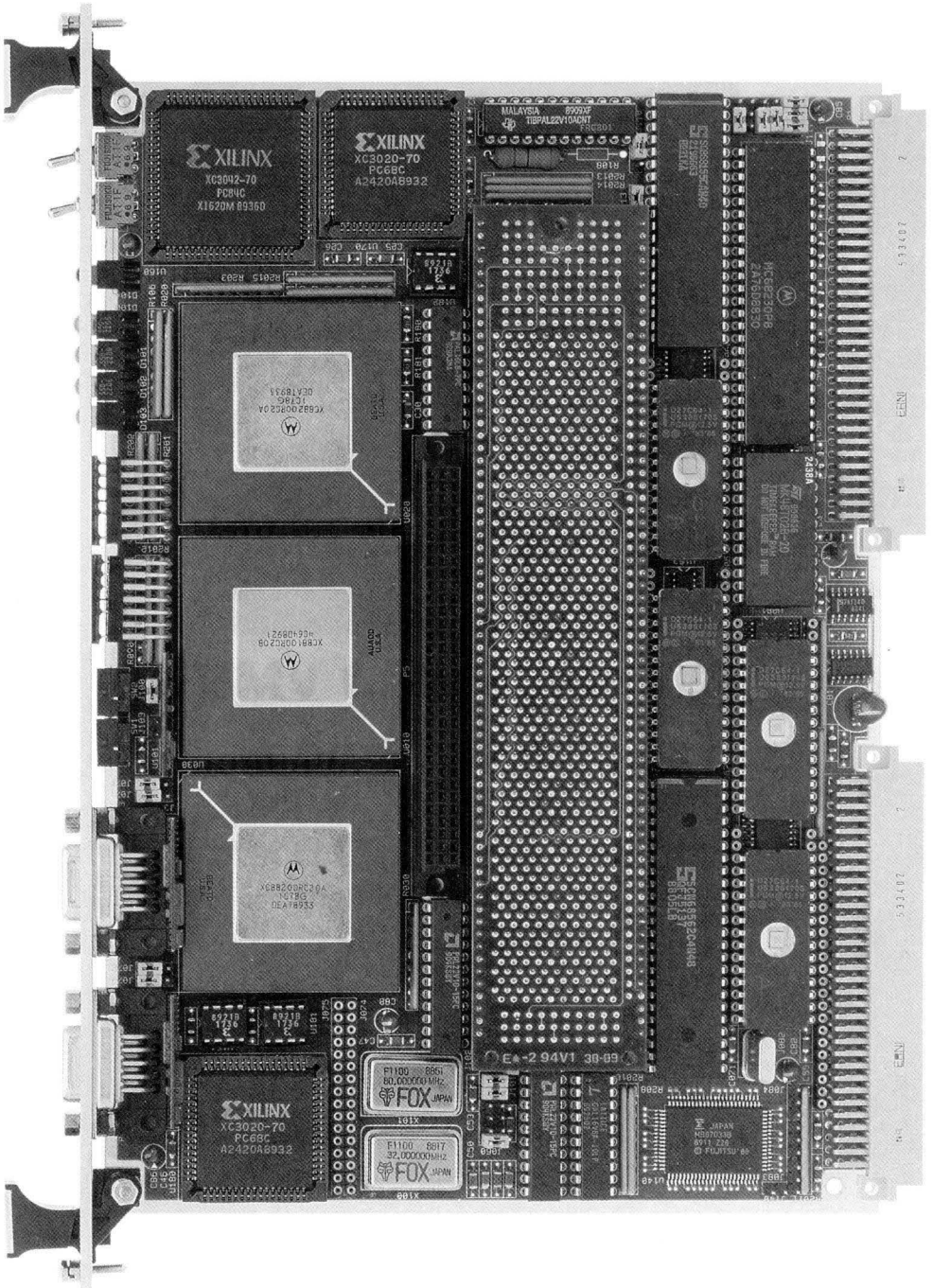
Ordering Information

SYS68K/CPU-40B/4-00 Part No. 102000	25.0 MHz 68040-based CPU board with DMA, 4 Mbyte shared memory, 4 serial I/O channels, FLXi, VMEPROM. Documentation included.
SYS68K/CPU-40B/4-01 Part No. 102001	25.0 MHz 68040-based CPU board with DMA, 4 Mbyte shared memory, 4 serial I/O channels, EAGLE-01 (SCSI, floppy disk and Ethernet interface), VMEPROM. Documentation included.
SYS68K/CPU-40B/16-00 Part No. 102100	25.0 MHz 68040-based CPU board with DMA, 16 Mbyte shared memory, 4 serial I/O channels, FLXi, VMEPROM. Documentation included.
SYS68K/CPU-40B/16-01 Part No. 102101	25.0 MHz 68040-based CPU board with DMA, 16 Mbyte shared memory, 4 serial I/O channels, EAGLE-01 (SCSI, floppy disk and Ethernet interface), VMEPROM. Documentation included.
SYS68K/CPU-40D/4-00 Part No. 102200	33.0 MHz 68040-based CPU board with DMA, 4 Mbyte shared memory, 4 serial I/O channels, FLXi, VMEPROM. Documentation included.
SYS68K/CPU-40D/4-01 Part No. 102201	33.0 MHz 68040-based CPU board with DMA, 4 Mbyte shared memory, 4 serial I/O channels, EAGLE-01 (SCSI, floppy disk and Ethernet interface), VMEPROM. Documentation included.
SYS68K/CPU-40D/16-00 Part No. 102300	33.0 MHz 68040-based CPU board with DMA, 16 Mbyte shared memory, 4 serial I/O channels, FLXi, VMEPROM. Documentation included.
SYS68K/CPU-40D/16-01 Part No. 102301	33.0 MHz 68040-based CPU board with DMA, 16 Mbyte shared memory, 4 serial I/O channels, EAGLE-01 (SCSI, floppy disk and Ethernet interface), VMEPROM. Documentation included.
SYS68K/IOBP-1 Part No. 700043	Back panel for single board computers providing SCSI and floppy disk drive connectors.
SYS68K/CABLE MICRO-9 SET 1 Part No. 700101	Set of three adapter cables 9-pin micro D-sub male connector to 9-pin D-sub female connector, length 2 m.
SYS68K/CABLE MICRO-9 SET 2 Part No. 700102	Set of four adapter cables 9-pin micro D-sub male connector to 25-pin D-sub female connector, length 2 m.
SYS68K/VMEPROM/40/UP Part No. 145120	VMEPROM update service for the SYS68K/CPU-40 series.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM user's manual.
SYS68K/CPU-40/UM Part No. 800300	User's manual for the SYS68K/CPU-40 including VMEPROM and FGA-002 user's manual.



System 88000 VME
SYS88K/CPU-80

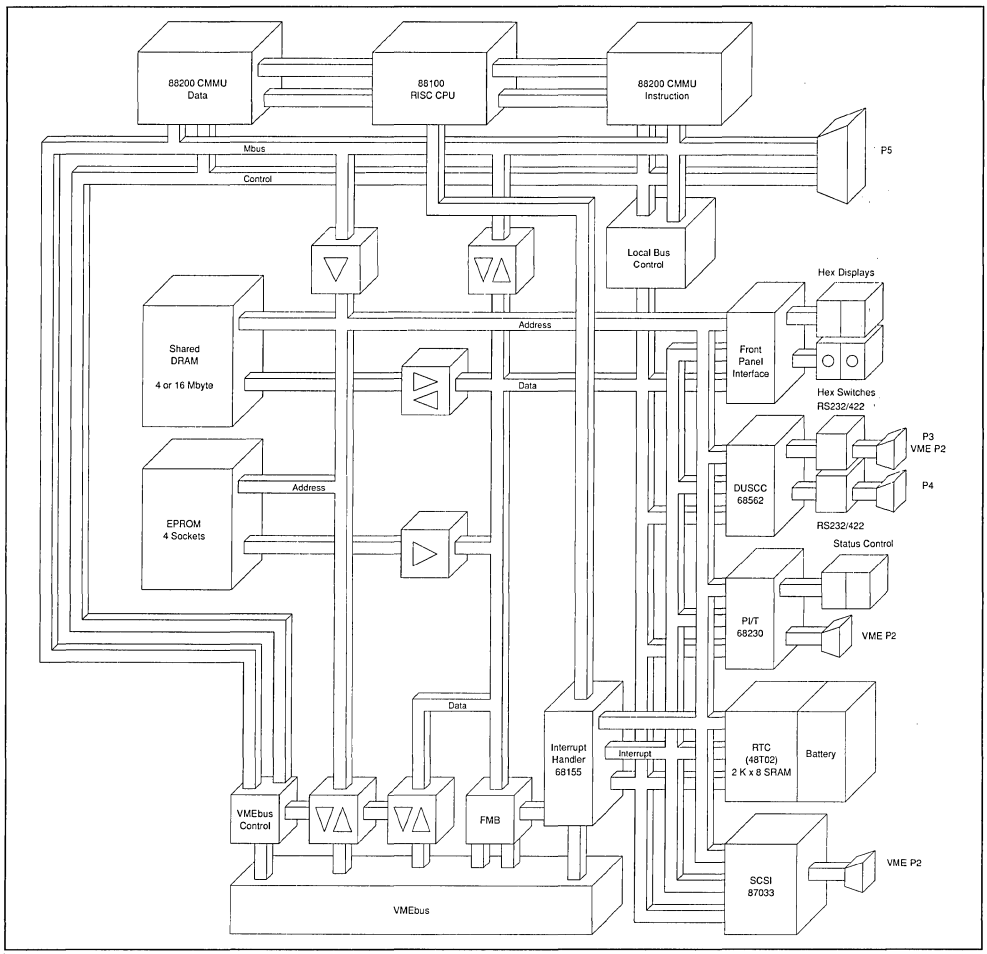
Ultra High Performance Multi-Processing CPU Board with 88K RISC, SCSI and Shared Memory


XILINX
XC3042-70
PC84C
XILINX
XC3020-70
PC68C
A2420A8932
MALAYSIA
TIBPAL22V10ACNT
FOX
JAPAN
XILINX
XC3020-70
PC68C
A2420A8932

General Description

The SYS88K/CPU-80 series product family consists of ultra high performance Reduced Instruction Set Computer (RISC) based CPU boards providing 4 or 16 Mbyte of shared dynamic RAM. The RISC processor is supported by two Cache and Memory Management Units (CMMUs), each containing 16 Kbyte zero wait state local cache memory. One CMMU is used for instructions, the other is used for data. Two multi-mode synchronous/asynchronous serial I/O ports provide serial communications. An SCSI interface is provided on the board to provide direct connection to disk drives and other SCSI-compatible devices. The CPU-80 includes IEEE 754-compatible Floating Point Arithmetic capabilities. Additional features include up to 4 Mbyte of EPROM capacity (32-bit wide), 2 Kbyte of static RAM, and Real Time Clock/Calendar. Both the static RAM and the Real Time Clock are battery backed-up for a ten-year data retention period. A monitor, FORCEbug/88K, is also included with each CPU-80 series CPU board product. FORCEbug/88K provides an effective software foundation on which to build application programs.

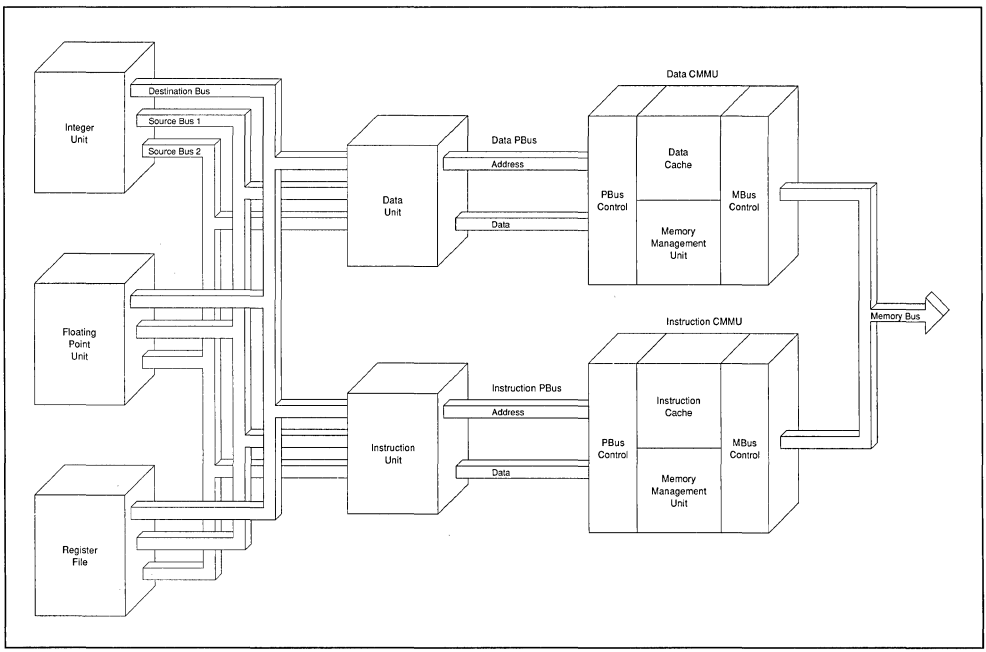
Block Diagram of the SYS88K/CPU-80



Features of the SYS88K/CPU-80 Series

- M88100 RISC CPU with 20.0 MHz or 25.0 MHz clock frequency
- M88200 instruction CMMU with 16 Kbyte instruction cache, 20.0 MHz or 25.0 MHz
- M88200 data CMMU with 16 Kbyte data cache, 20.0 MHz or 25.0 MHz
- 4 or 16 Mbyte shared high speed memory organized to effectively support cache accesses
- Two serial I/O interfaces, RS232/RS422-compatible
- SCSI interface using MB87033 controller chip
- Support for four user EPROM devices providing a 32-bit data path with up to 4 Mbyte capacity
- Interprocessor interrupt capability (Multiprocessor configurations)
- 2 Kbyte static RAM with battery back-up
- Real Time Clock with battery back-up
- Programmable 24-bit counter/timer provided in the Parallel Interface/Timer (PI/T 68230)
- Local I/O device interrupt support
- BERR handling for local and VME accesses
- Two fully independent FORCE Message Broadcast (FMB) channels
- Full 32-bit VMEbus master/slave interface supporting the following data transfer types:
  - Master: A32, A24, A16 : D8, D16, D32
  - Slave: A32, A24 : D8, D16, D32
  - Address only
  - Read-Modify-Write cycles are also supported
- Four-level VMEbus arbiter
- SYSCLK driver
- IACK daisy chain driver
- VMEbus Interrupt Handler (levels 1–7 dynamically configurable)
- Support for ACFAIL* and SYSFAIL* interrupts
- Bus timeout for local and VMEbus access
- Front panel switches for user-selectable configuration data
- Two software-controlled front panel hexadecimal displays

Block Diagram of the M88100 RISC Processor



1. Hardware Description

1.1 The M88100 RISC Processor

The CPU device utilized on the CPU-80 series products is the ultra high performance 32-bit M88100 Reduced Instruction Set Computer (RISC) microprocessor. Using a Harvard architecture and implemented in HCMOS technology, the M88100 features 32-bit registers and separate data and instruction paths. Over 90 % of the 51 instructions implemented in the M88100 are executed in one clock cycle. Achieving this level of throughput requires the incorporation of four independent execution units coupled with separate, fully concurrent execution pipelines.
The M88100 accesses instructions and data directly from two M88200 Cache/Memory Management Units (CMMU). Data not directly available in either of the M88200 CMMUs are retrieved from on-board shared memory consisting of fast nibble-mode DRAM.

1.2 The M88200 CMMU

Two M88200 CMMUs (Cache/Memory Management Units) each provide 16 Kbyte of four-way set-associative cache memory designed to support the high speed memory access requirements of the M88100 processor. One CMMU is used for instruction caching and the other CMMU supports data caching. Both CMMUs provide system interfacing to the M88100 processor. A demand-paged virtual memory management function supporting a segmented architecture is provided by the CMMUs. Two Address Translation Caches (ATC) residing in the CMMUs increase memory management performance. The data caching functions incorporate a 16 Kbyte, four-way set associative cache for instruction or data storage, using a Least-Recently-Used (LRU) replacement algorithm for managing cache and shared memory. The cache features both copy-back and write-through memory update policies. The M88200 CMMU includes a non-multiplexed, pipelined processor bus and a multiplexed system bus interface.
The M88200 on-chip 16 Kbyte data or instruction cache provides high speed access to a subset of system memory, significantly reducing conventional memory access delays. Further, by implementing the cache memory, the cache control, and the memory management unit on the same device, the address translation and the cache set selection are performed concurrently in a single cycle. This concurrency eliminates memory access delays due to address translation for the entries stored in the cache. Entries are cached by physical address rather than by logical address, significantly reducing the cache management overhead.

1.3 Shared Dynamic RAM

4 Mbyte or 16 Mbyte of shared, parity-checked, dynamic memory 32 bits wide are provided on the CPU-80 series. Nibble-mode memory chips are used to allow fast access to consecutive memory locations. Most DRAM accesses are expected to be four-word, block fill, cache line transfers. Thus, the first word access takes approximately 80 nsec, followed by three accesses taking approximately 30 nsec each.
The shared dynamic RAM is accessed by one of two M88200 CMMUs when data or instructions are determined not to be in the local 16 Kbyte cache.
The combined characteristics of nibble-mode DRAM and M88200 cache line accesses produce a main memory that is nearly as fast as static RAM, but with the density and cost advantages of dynamic RAM. The on-board DRAM is configured as 32 bit wide. Each 8-bit byte is protected by one parity bit, creating a 36-bit wide configuration. Parity is generated and checked by on-board logic. Parity errors are reported as interrupts.

1.4 The Local SRAM

A 48T02 2048-byte static RAM/Real Time Clock (RTC) device is installed on the CPU-80 series products. This battery backed-up device supports data storage during power-down phases for a minimum of ten years and can be utilized to store user configuration information. Power sensor circuitry ensures that normal read and write operations to the SRAM and/or Real Time Clock are allowed only when the power is within specifications. The SRAM/RTC is connected to the local I/O interface bus. Byte transfers are handled on word-boundary accesses.

1.5 The EPROM Area

The CPU-80 series provides four user EPROM sockets supporting four 28-pin or 32-pin memory devices. Maximum data throughput to the

M88200 CMMUs is provided through the simultaneous access and decoding of the EPROM address. Supported device types are shown below.

Device	Pins	Organization	Capacity
27256	28	32 K × 8	128 Kbyte
27512	28	64 K × 8	256 Kbyte
2710xx	32	128 K × 8	512 Kbyte
2720xx	32	256 K × 8	1 Mbyte
TBD	32	512 K × 8	2 Mbyte
TBD	32	1 M × 8	4 Mbyte

1.6 The Serial I/O Interfaces

One 68562 Dual Universal Serial Communication Controller (DUSCC) is installed on the CPU-80 to communicate with terminals, computers, modems, or other equipment.
The I/O signal assignment of each channel is listed below.

Pin	RS232	RS422
1	DCD	TXD–
2	RXD	RTS–
3	TXD	CTS+
4	DTR	RXD+
5	GND	RXD–
6	DSR	N/C
7	RTS	RTS+
8	CTS	CTS–
9	GND	RXD–

Features of the DUSCC

- Dual full-duplex synchronous and asynchronous receiver and transmitter (programmable)
- Multi-protocol operation enabling support of bit- or character-oriented protocols. With additional software this allows the support of HDLC, SDLC, X.25, X.75, BISYNC, etc.
- Programmable data encoding formats: NRZ, NRZI, FM0, FM1, Manchester
- 4 character receiver/transmitter FIFOs
- Individual programmable baud rate for each receiver and transmitter supported by a digital phase locked loop
- Modem control signals for each channel: RTS, CTS, DCD

Each channel can be configured to work with RS232 or RS422-compatible interfaces. Transmit and/or receive clocks may be jumpered to the DB9 connector for support of synchronous protocols. The DUSCC can be programmed to interrupt the local CPU with software-programmable priority and programmable interrupt vector.

1.7 The Real Time Clock

A Real Time Clock/Calendar is permanently integrated with the SRAM and occupies the last 8 bytes of the 2 Kbyte SRAM address space. The RTC is software-programmable and is supported with battery back-up.

Features of the Real Time Clock

- Time of day and date counter (year, month, day, hour, minute, second)
- Built-in quartz oscillator
- Automatic leap year setting
- CMOS design for low-power consumption during power-down
- Guaranteed minimum battery life of 10 years
- Internal battery, no external battery required
- Automatic power fail detect and switch-over

1.8 The Front Panel Switch Register

The front panel switch register is a read-only register which allows application programs to access two 16-position rotary switches located on the front panel of the CPU-80 boards. These switches can be set to any one of 256 possible combinations.

1.9 The Front Panel Status Register

The front panel status register is a read/write register which enables software to read and set the two easy-to-read hex displays located on the front panel. The current state of these displays can be read at any time to determine the last information written to this register.

1.10 The Timer

A programmable 16-bit counter/timer is provided in the DUSCC. A 24-bit programmable counter/timer is provided by the PI/T. This may be programmed to act as a software timer. Interrupt generation for this timer is programmable.

1.11 The SCSI Interface

An MB87033 SCSI Controller is used on the CPU-80 to provide data transfer support between the CPU-80 and Small Computer System Interface devices such as SCSI disk drives, optical drives and tape drives.

Features of the 87033 SCSI Controller:

- Full support of SCSI control
- Service of either initiator or target modes
- 8-byte data buffer register on-chip
- Transfer byte count of 28 bits (256 Mbyte)
- MPU bus parity generator
- Arbitration fail interrupt
- ATN condition detect interrupt
- On-chip single-ended drivers
- Software-compatible with SCSI devices used with other FORCE CPU products

The on-chip SCSI controller can be used by application software to provide mass storage capabilities for the CPU-80 board. The 87033 can be programmed to the needs of the application, thus providing a solution for those system implementations requiring program downloading, data logging storage, report generation and other mass memory configurations.

1.12 The Parallel Ports

A total of three parallel ports are provided on the CPU-80. Two are used for on-board status and control. A third port is available at P2 for off-board parallel I/O functions, such as a Centronics-compatible printer interface.

1.13 Expansion Connector

The CPU-80 is installed with a 96-pin expansion connector (P5) which directly connects to the unbuffered Mbus of the CMMUs. The connector is made available for the user to build memory expansion or multi-processing modules for the CPU-80.

2. The VMEbus Interface

2.1 The VMEbus Time-out Timer

A VMEbus timer is provided on the CPU-80 to ensure continuous operation. If, after 26 µsec, a slave has not responded with DTACK*, the timer will generate a BERR* signal to indicate an incomplete VMEbus access cycle.

2.2 VMEbus Data Transfers

The CPU-80 series includes a full 32-bit VMEbus interface, thereby taking full advantage of the VMEbus IEEE 1014 Specification. Address modifier (AM) codes for A16 (master only), A24 and A32 addressing are supported in master and slave mode. In slave mode, on-board logic decodes the AM codes and address signals of the VMEbus. Additional control logic determines if the programmable decoding range is addressed correctly and if the access cycle is to be executed. This provides effective write protection for on-board memory. Data transfers of 8-, 16-, 24- or 32-bit are supported automatically.
The following data transfer types are supported in master and slave mode:

Transfer Type	D31-24	D23-16	D15-8	D7-0
Byte				x
			x	
Word			x	x
Long Word	x	x	x	x
Unaligned Transfers*	x	x	x	
		x	x	
		x	x	x
Read Modify Write				x
			x	x
	x	x	x	x

* Slave mode only

Read-Modify-Write cycles are fully supported to synchronize multiple CPU boards via the shared RAM. Access time to shared RAM from the VMEbus are as follows:

Access Cycle	Typical Access Time
Read Write	400 nsec 400 nsec

2.3 The VMEbus System Controller

The CPU-80 series supports the following bus release modes as requestors:

REC = Release Every Cycle
RAT = Release After Timeout
RBCLR = Release On Bus Clear

Arbitration modes supported:

PRI = Prioritized
PRR = Prioritized/Round Robin
RRS = Round Robin
SGL = Single Level

Each of the arbitration modes is software-programmable. The bus request level of the CPU-80 is jumper-selectable (BR0* – BR3*). A four-level arbiter, IACK* daisy-chain driver, SYSRESET* generator and support for ACFAIL*, SYSFAIL*, and SYSCLK drivers complete the VMEbus interface.

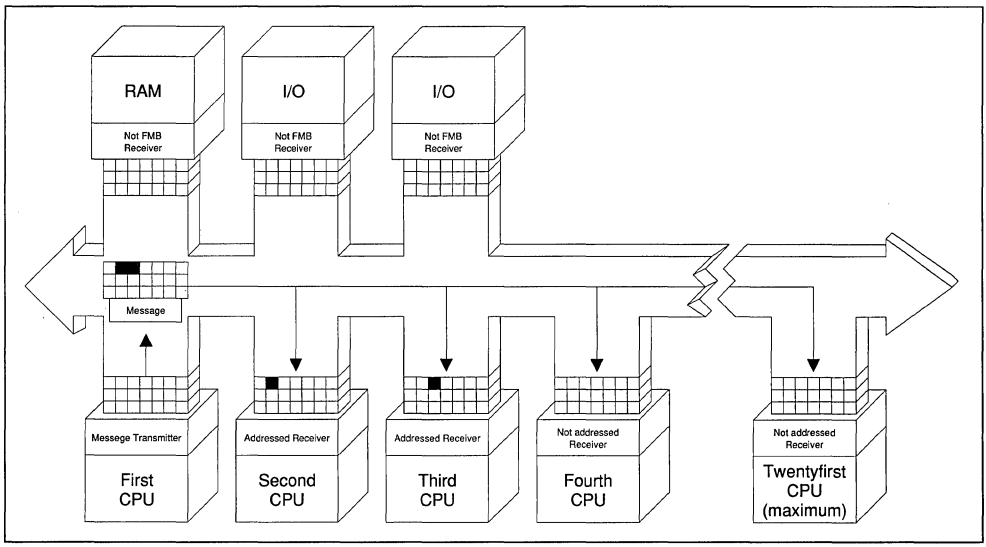
3. FORCE Message Broadcast

The FORCE Message Broadcast (FMB) is a fast and effective mechanism to communicate with and to synchronize up to 20 CPU boards in a VMEbus system in only one VMEbus write cycle. It offers a unique support feature for building multi-processing systems based on the VMEbus. An FMB transfer is a standard VMEbus write cycle and complies fully to the IEEE 1014 Specification. Any VMEbus master may be a message transmitter. The transmitter decides which boards in the system should be addressed (one, two or up to twenty boards) and writes the message to a specific address.

All addressed boards receive the message at the same time and generate an interrupt request on a programmable level to their local microprocessor. This ensures that there is no time delay between the synchronization of different boards in the system. The ability to communicate with and synchronize multiple CPUs in the system by the FMB mechanism allows the VMEbus to be used in a wide range of application areas, particularly multi-processor environments.

Without the FMB mechanism, communication between and synchronisation of system boards has to be managed via the seven interrupt request lines. FMB reduces the massive time

Block Diagram of the FORCE Message Broadcast



overhead normally needed to process the interrupt cycles to just one write cycle.
All CPU-80 boards provide two fully independent message broadcast channels, each designed to store one 8-bit message.

4. The Interrupt Structure
Special on-board logic installed on the CPU-80 series handles all local and VMEbus interrupts. Each interrupt request from the local bus devices, including DUSCC and timers are combined with the seven VMEbus interrupt requests.
Each IRQ-source including the VMEbus IRQs can be programmed to interrupt the CPU. On-board logic initiates an interrupt vector fetch from the VMEbus.

5. The Memory Organization
The CPU-80 memory organization is shown below. Starting VMEbus addresses and size of shared memory (DRAM) are programmable. Programmable addresses are retained in SRAM during power-down.

Start Address	End Address	Type
00000000	00FFFFFF	Shared Memory (CPU-80)
01000000	03FFFFFF	Reserved
04000000	FBFFFFFF	VMEbus Address A32 : D32, D24, D16, D8
FA000000	FAFFFFFF	FMB Address Space
FB000000	FBFEFFFF	VMEbus Address A24 : D32, D24, D16, D8
FBFF0000	FBFFFFFF	VMEbus Address A16 : D16, D8
FC000000	FEFFFFFF	Reserved
FF000000	FF7FFFFF	EPROM
FF800000	FFBFFFFF	Local I/O
FFC00000	FFFFFFFF	Control Space, CMMU Registers

6. FORCEbug/88K
FORCEbug/88K is an EPROM-based monitor. Residing in 256 Kbyte of EPROM and requiring only 64 Kbyte of RAM, FORCEbug/88K provides real time support capabilities for embedded control applications. FORCEbug/88K comprises of a monitor and software drivers.

6.1 Monitor/Debugger
The monitor supports interactive command execution for debugging. A powerful set of debugging facilities is provided to simplify program debugging activities.
These software routines include interactive assembler, symbolic disassembler, breakpoints, single stepping, memory and register display/modification. FORCEbug/88K supports definition of symbolic commands and placing symbols in a symbol table. The symbol table and use of a base register enhance the ease and capability of the debugging environment. A set of benchmark routines and a command timer provide support for system performance evaluation.

6.2 Target System Support
FORCEbug/88K is easily used in target system configurations. For these kinds of system implementations, FORCEbug/88K applications are easily programmed into EPROM.

7. Benchmarks
Performance in any CPU system depends upon many complex factors. The use of simulators or benchmarks to predict performance should be used carefully and conservatively. Provided below are published performance numbers for three common benchmark programs.

	Clock 20.0 MHz	Clock 25.0 MHz
MIPS	17	21
Dhrystones	36,000	41,000
Whetstones	16 Million	18 Million
Linpack	5,300	5,600

8. Software

It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-80 Software Support

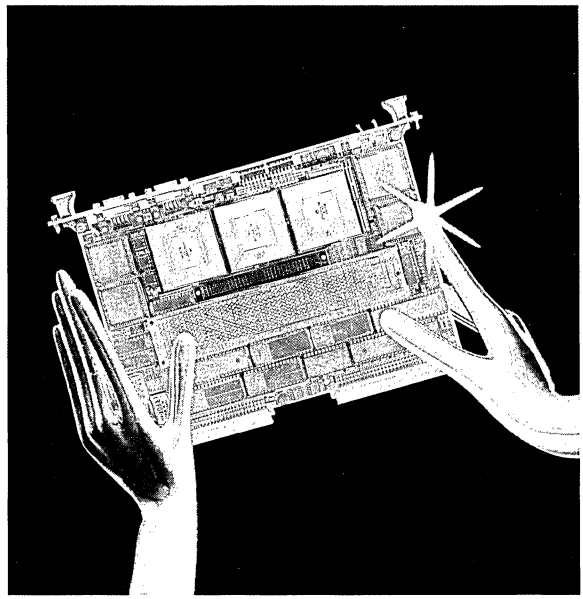
Operating System/Kernel	Vendor/Support
UNIX V.3	FORCE COMPUTERS
OS-9/9000	Contact FORCE for availability
VxWORKS	Contact FORCE for availability
VRTX-32	Contact FORCE for availability
pSOS	Software Components Group
ARTX	Contact FORCE for availability
Telesoft ADA	Contact FORCE for availability

Specifications

Function		
M88100/M88200 frequency	CPU-80A/4, CPU-80A/16 CPU-80B/16	20.0 MHz 25.0 MHz
On-board cache memory (M88200):	data cache size instruction cache size	16 Kbyte 16 Kbyte
Shared nibble-mode, DRAM with parity Static RAM configuration Device used Battery back-up		4 Mbyte or 16 Mbyte 2 Kbyte MK48T02 yes
Real Time Clock/calendar with on-board battery back-up		MK48T02
No. of system EPROM sockets Data path Max. capacity (as devices become available)		4 32-bit 4 Mbyte
SCSI interface (87033)		single-ended
Serial I/O interfaces (total) controller used RS232/422-compatible Parallel interface		2 68562 2 8-bit with handshake
Counters/timers	24-bit with 5-bit prescale	1
VMEbus interface IACK* daisy chain driver Four-level VMEbus arbiter SYSCLK driver	A32, A24, A16 : D32, D16, D8 A32, A24 : D32, D16, D8, UAT	Master Slave yes yes yes
FORCE Message Broadcast 	 FMB-FIFO-1 FMB-FIFO-2	yes 1 byte 1 byte
Front panel switches/indicators 	 RESET, ABORT switches Hexadecimal LED displays	 yes 2
Power requirements	+ 5 V min : max + 12 V min : max – 12 V min : max	4.0 A : 5.2 A 0.1 A : 0.3 A 0.1 A : 0.3 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)		0 to + 50 °C – 40 to + 85 °C 5 to 95 %
Board dimensions		234 × 160 mm : 9.2 × 6.3 in
No. of slots used		1

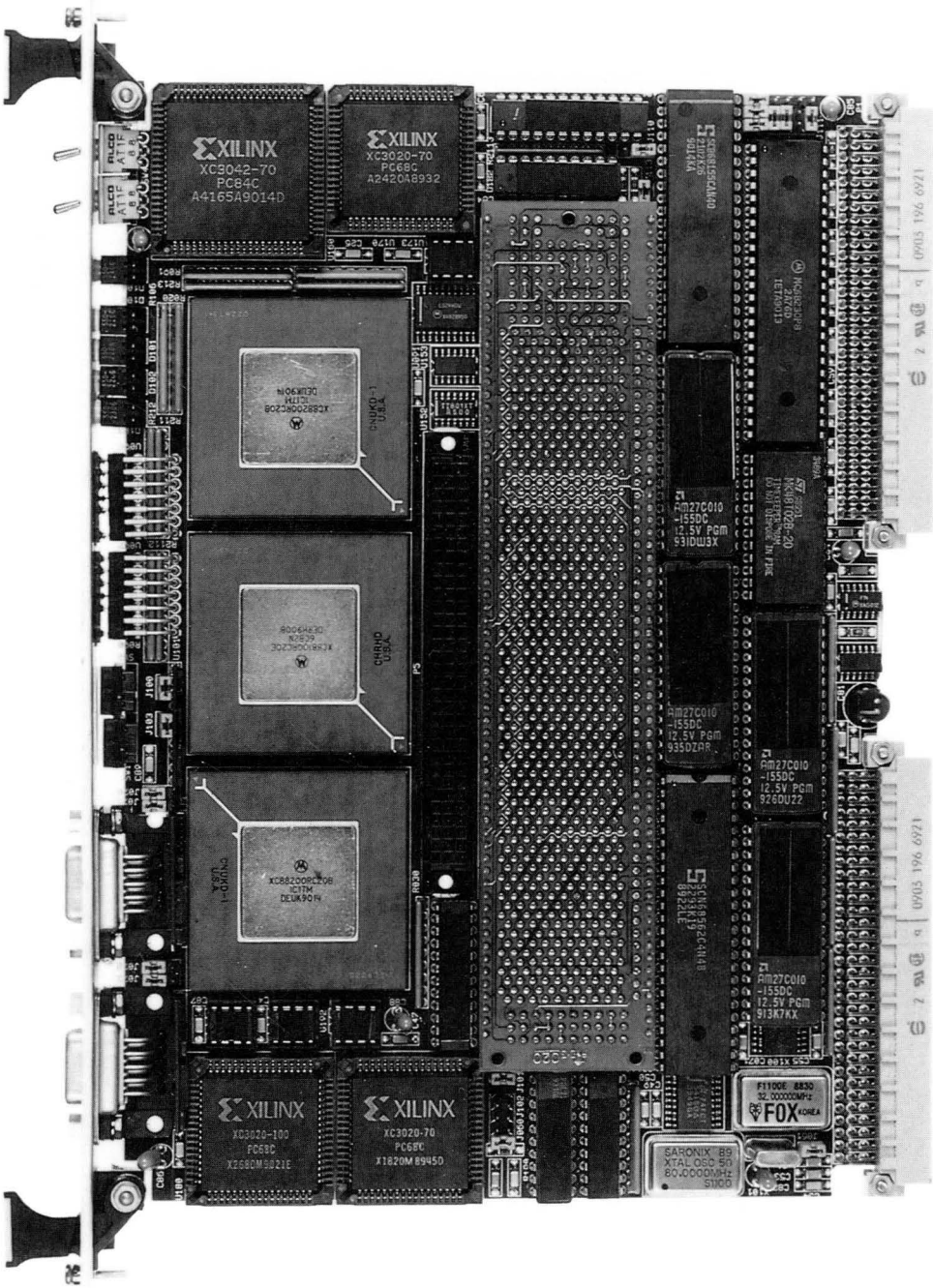
Ordering Information

SYS88K/CPU-80A/4 Part No. 510053	20.0 MHz M88100 RISC-based CPU board with two M88200 CMMUs, 4 Mbyte shared nibble-mode dynamic RAM and SCSI interface. Documentation included.
SYS88K/CPU-80A/16 Part No. 510054	20.0 MHz M88100 RISC-based CPU board with two M88200 CMMUs, 16 Mbyte shared nibble dynamic RAM and SCSI interface. Documentation included.
SYS88K/CPU-80B/16 Part No. 510086	25.0 MHz M88100 RISC-based CPU board with two M88200 CMMUs, 16 Mbyte shared nibble-mode dynamic RAM and SCSI interface. Documentation included.
SYS88K/CPU-80/UM Part No. 510089	User's manual for CPU-80 series including hardware and software descriptions.



System 88000 VME
SYS88K/CPU-81

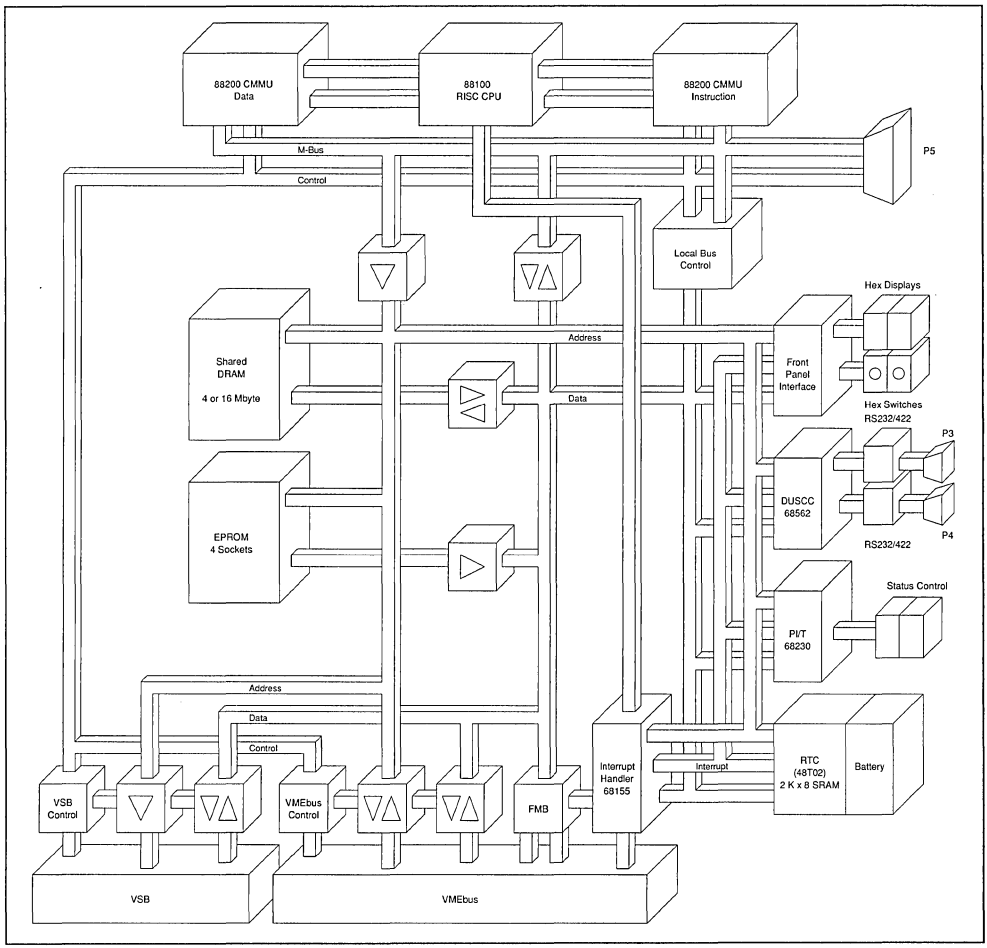
Ultra High Performance Multi-Processing CPU with 88K RISC Processor, Shared Memory and VSB


XILINX
XC3042-70
PC84C
A4165A9014D
XILINX
XC2020-70
PC68C
A2420A8932
XILINX
XC3020-100
PC68C
XILINX
XC3020-70
PC68C
AM27C010
-155DC
12.5V PGM
FOX

General Description

The SYS88K/CPU-81 series product family consists of ultra high performance Reduced Instruction Set Computer (RISC) based CPU boards providing 4 or 16 Mbyte of shared dynamic RAM. The RISC processor is supported by two Cache and Memory Management Units (CMMUs), each containing 16 Kbyte zero wait state local cache memory. One CMMU is used for instructions, the other is used for data. Two multi-mode synchronous/asynchronous serial I/O ports provide serial communications. A VME Subsystem Bus (VSB) interface provides local bus access to VSB-compatible products, such as memory boards. The CPU-81 includes IEEE 754-compatible Floating Point Arithmetic capabilities. Additional features include up to 4 Mbyte of EPROM capacity (32-bit wide), 2 Kbyte of static RAM, and Real Time Clock/Calendar. Both the static RAM and the Real Time Clock are battery backed-up for a ten year data retention period. A monitor, FORCEbug/88K, is also included with each CPU-81 series CPU board product. FORCEbug/88K provides an effective software foundation on which to build application programs.

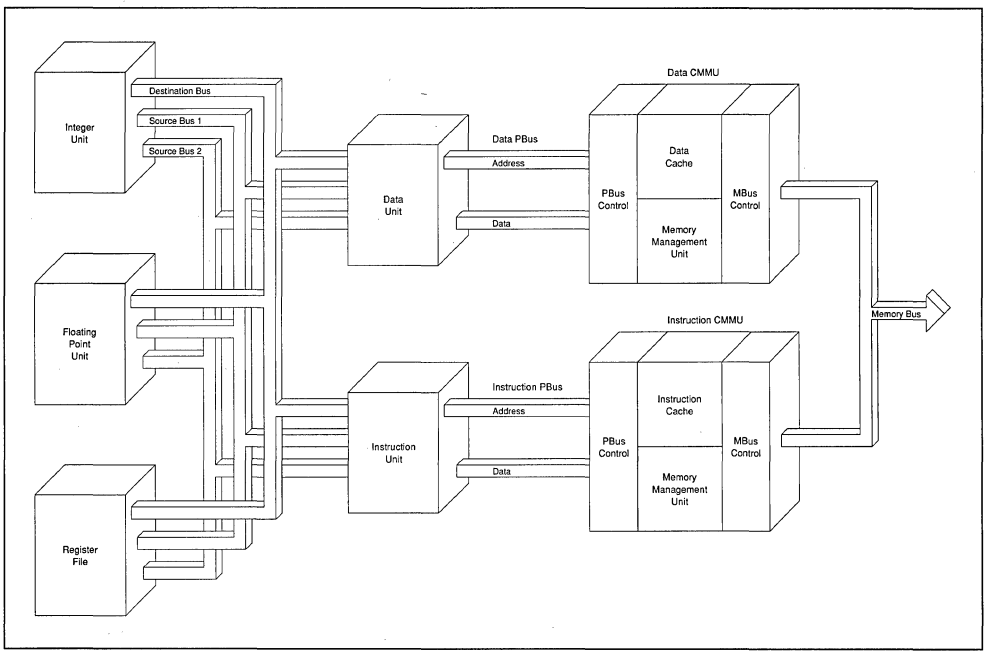
Block Diagram of the SYS88K/CPU-81



Features of the SYS88K/CPU-81 Series

- M88100 RISC CPU with 20.0 MHz or 25.0 MHz clock frequency
- M88200 instruction CMMU with 16 Kbyte instruction cache, 20.0 MHz or 25.0 MHz
- M88200 data CMMU with 16 Kbyte data cache, 20.0 MHz or 25.0 MHz
- 4 or 16 Mbyte shared high-speed memory organized to effectively support cache accesses
- Two serial I/O interfaces, RS232/RS422-compatible
- Support for four user EPROM devices providing a 32-bit data path with up to 4 Mbyte capacity
- Interprocessor interrupt capability (Multiprocessor configurations)
- 2 Kbyte static RAM with battery back-up
- Real Time Clock with battery back-up
- Programmable 24-bit counter/timer provided in the Parallel Interface/Timer (PI/T 68230)
- Local I/O device interrupt support
- BERR handling for local and VME accesses
- Two fully independent FORCE Message Broadcast (FMB) channels
- Full 32-bit VMEbus master/slave interface supporting the following data transfer types:
  - Master: A32, A24, A16 : D8, D16, D32
  - Slave: A32, A24 : D8, D16, D32
  - Address only
  - Read-Modify-Write cycles are also supported
- Four-level VMEbus arbiter
- SYSCLK driver
- IACK daisy chain driver
- VMEbus Interrupt Handler (levels 1–7 dynamically configurable)
- Support for ACFAIL* and SYSFAIL* interrupts
- VSB master interface for memory and I/O expansion
  - VSB arbiter
  - VSB interrupt handler
- Bus timeout for local and VMEbus access
- Front panel switches for user-selectable configuration data
- Two software-controlled front panel hexadecimal displays

Block Diagram of M88100 RISC Processor



1. Hardware Description

1.1 The M88100 RISC Processor

The CPU device utilized on the CPU-81 series products is the ultra high-performance 32-bit M88100 Reduced Instruction Set Computer (RISC) microprocessor. Using a Harvard architecture and implemented in HCMOS technology, the M88100 features 32-bit registers and separate data and instruction paths. Over 90 % of the 51 instructions implemented in the M88100 are executed in one clock cycle. Achieving this level of throughput requires the incorporation of four independent execution units coupled with separate, fully concurrent execution pipelines.

The M88100 accesses instructions and data directly from two M88200 Cache/Memory Management Units (CMMU). Data not directly available in either of the M88200 CMMUs is retrieved from on-board shared memory consisting of fast nibble-mode DRAM.

1.2 The M88200 CMMU

Two M88200 CMMUs (Cache/Memory Management Units) each provide 16 Kbyte of four-way set-associative cache memory designed to support the high-speed memory access requirements of the M88100 processor. One CMMU is used for instruction caching and the other CMMU supports data caching. Both CMMUs provide system interfacing to the M88100 processor. A demand-paged virtual memory management function supporting a segmented architecture is provided by the CMMUs. Two Address Translation Caches (ATC) residing in the CMMUs increase memory management performance. The data caching functions incorporate a 16 Kbyte, four-way set associative cache for instruction or data storage, using a Least-Recently-Used (LRU) replacement algorithm for managing cache and shared memory. The cache features both copy-back and write-through memory update policies. The M88200 CMMU includes a non-multiplexed, pipelined processor bus and a multiplexed system bus interface.

The M88200 on-chip 16 Kbyte data or instruction cache provides high-speed access to a subset of system memory, significantly reducing conventional memory access delays. Further, by implementing the cache memory, the cache control, and the memory management unit on the same device, the address translation and the cache set selection are performed concurrently in a single cycle. This concurrency eliminates memory access delays due to address translation for the entries stored in the cache. Entries are cached by physical address rather than by logical address, significantly reducing the cache management overhead.

1.3 Shared Dynamic RAM

4 Mbyte or 16 Mbyte of shared, parity-checked, dynamic memory 32 bit wide are provided on the CPU-81 series. Nibble-mode memory chips are used to allow fast access to consecutive memory locations. Most DRAM accesses are expected to be four-word, block fill, cache line transfers. Thus, the first word access takes approximately 80 nsec, followed by three accesses taking approximately 40 ns each.

The shared dynamic RAM is accessed by one of two M88200 CMMUs when data or instructions are determined not to be in the local 16 Kbyte cache. The combined characteristics of nibble-mode DRAM and M88200 cache line accesses produce a main memory that is nearly as fast as static RAM, but with the density and cost advantages of dynamic RAM. The on-board DRAM is configured as 32 bit wide. Each 8-bit byte is protected by one parity bit, creating a 36-bit wide configuration. Parity is generated and checked by on-board logic. Parity errors are reported as interrupts.

1.4 The Local SRAM

A 48T02 2048 byte static RAM/Real Time Clock (RTC) device is installed on the CPU-81 series products. This battery backed-up device supports data storage during power-down phases for a minimum of ten years and can be utilized to store user configuration information. Power sensor circuitry ensures that normal read and write operations to the SRAM and/or Real Time Clock are allowed only when the power is within specifications. The SRAM/RTC is connected to the local I/O interface bus. Byte transfers are handled on word-boundary accesses.

1.5 The EPROM Area

The CPU-81 series provides four user EPROM sockets supporting four 28-pin or 32-pin memory devices. Maximum data throughput to the M88200 CMMUs is provided through the

simultaneous access and decoding of the EPROM address. Supported device types are shown below.

Device	Pins	Organization	Capacity
27256	28	32 K × 8	128 Kbyte
27512	28	64 K × 8	256 Kbyte
271001	32	128 K × 8	512 Kbyte
272001	32	256 K × 8	1 Mbyte
TBD	32	512 K × 8	2 Mbyte
TBD	32	1 M × 8	4 Mbyte

1.6 The Serial I/O Interfaces

One 68562 Dual Universal Serial Communication Controller (DUSCC) is installed on the CPU-81 to communicate with terminals, computers, modems, or other equipment.
The I/O signal assignment of each channel is listed below.

Pin	RS232	RS422
1	DCD	TXD–
2	RXD	RTS–
3	TXD	CTS+
4	DTR	RXD+
5	GND	RXD–
6	DSR	TXD+
7	RTS	RTS+
8	CTS	CTS–
9	GND	RXD–

Each channel can be configured to work with RS232 or RS422-compatible interfaces. Transmit and/or receive clocks may be jumpered to the DB9 connector for support of synchronous protocols. The DUSCC can be programmed to interrupt the local CPU with software-programmable priority and programmable interrupt vector.

Features of the DUSCC

- Dual full-duplex synchronous and asynchronous receiver and transmitter (programmable)
- Multi-protocol operation enabling support of bit- or character-oriented protocols. With additional software this allows the support of HDLC, SDLC, X.25, X.75, BISYNC, etc.
- Programmable data encoding formats: NRZ, NRZI, FM0, FM1, Manchester
- 4 character receiver/transmitter FIFOs
- Individual programmable baud rate for each receiver and transmitter supported by a digital phase locked loop
- Modem control signals for each channel: RTS, CTS, DCD

1.7 The Real Time Clock

A Real Time Clock/Calendar is permanently integrated with the SRAM and occupies the last 8 byte of the 2 Kbyte SRAM address space. The RTC is software-programmable and is supported with battery back-up.

Features of the Real Time Clock

- Time of day and date counter (year, month, day, hour, minute, second)
- Built-in quartz oscillator
- Automatic leap year setting
- C-MOS design for low power consumption during power-down
- Guaranteed minimum battery life of 10 years
- Internal battery, no external battery required
- Automatic power fail detect and switch-over

1.8 The Front Panel Switch Register

The front panel switch register is a read-only register which allows application programs to access two 16-position rotary switches located on the front panel of the CPU-81 boards. These switches can be set to any one of 256 possible combinations.

1.9 The Front Panel Status Register

The front panel status register is a read/write register which enables software to read and set the two easy-to-read hex displays located on the front panel. The current state of these displays can be read at any time to determine the last information written to this register.

1.10 The Timer

The 16-bit counter/timer is provided by the PI/T. This may be programmed to act as a software timer. Interrupt generation for this timer is programmable.

1.11 Expansion Connector

The CPU-80 is installed with a 96-pin expansion connector (P5) which directly connects to the unbuffered Mbus of the CMMUs. The connector is made available for the user to build memory expansion or multi-processing modules for the CPU-80.

2. The VMEbus Interface

2.1 VMEbus Data Transfers

The CPU-81 series includes a full 32-bit VMEbus interface, thereby taking full advantage of the VMEbus IEEE 1014 Specification. Address modifier (AM) codes for A16 (Master only), A24 and A32 addressing are supported in master and slave mode. In slave mode, on-board logic decodes the AM codes and address signals of the VMEbus.

Additional control logic determines if the programmable decoding range is addressed correctly and if the access cycle is to be executed. This provides effective write protection for on-board memory. Data transfers of 8-, 16-, 24- or 32-bits are supported automatically.

The following data transfer types are supported in master and slave mode:

Transfer Type	D31-24	D23-16	D15-8	D7-0
Byte				x
			x	
Word			x	x
Long Word	x	x	x	x
Unaligned Transfers*	x	x	x	
		x	x	
		x	x	x
Read Modify Write				x
			x	x
	x	x	x	x

* Slave mode only

Read-Modify-Write cycles are fully supported to synchronize multiple CPU boards via the shared RAM. Access time to shared RAM from the VMEbus are as follows:

Access Cycle	Typical Access Time
Read	400 nsec
Write	400 nsec

2.2 The VMEbus System Controller

The CPU-81 series supports the following bus release modes as requestors:

REC = Release Every Cycle
RAT = Release After Timeout
RBCLR = Release On Bus Clear

Arbitration modes supported:

PRI = Prioritized
PRR = Prioritized/Round Robin
RRS = Round Robin
SGL = Single Level

Each of the arbitration modes is software-programmable. The bus request level of the CPU-81 is jumper-selectable (BR0* - BR3*). A four-level arbiter, IACK* daisy chain driver, SYSRESET* generator and support for ACFAIL*, SYSFAIL*, and SYSCLK drivers complete the VMEbus interface.

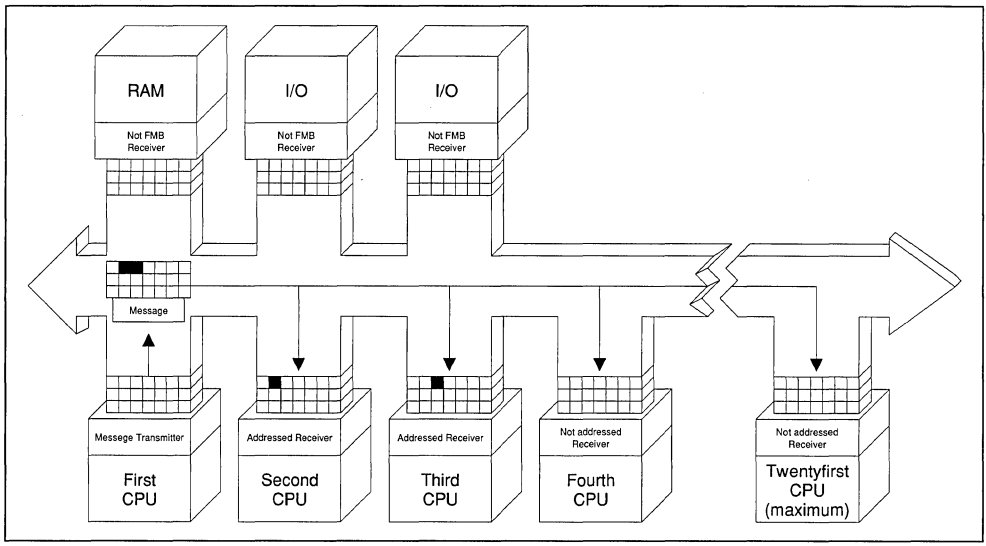
2.3 The VMEbus Time-Out Timer

A VMEbus timer is provided on the CPU-81 to ensure continuous operation. If, after 26 µsec, a slave has not responded with DTACK*, the timer will generate a BERR* signal to indicate an incomplete VMEbus access cycle.

3. FORCE Message Broadcast

The FORCE Message Broadcast (FMB) is a fast and effective mechanism to communicate with and to synchronize up to 20 CPU boards in a VMEbus system in only one VMEbus write cycle. It offers a unique support feature for building multi-processing systems based on the VMEbus. An FMB transfer is a standard VMEbus write cycle and complies fully to the IEEE 1014 Specification. Any VMEbus master may be a message transmitter. The transmitter decides which

Block Diagram of the FORCE Message Broadcast



boards in the system should be addressed (one, two or up to twenty boards) and writes the message to a specific address.
All addressed boards receive the message at the same time and generate an interrupt request on a programmable level to their local microprocessor. This ensures that there is no time delay between the synchronization of different boards in the system. The ability to communicate with and synchronize multiple CPUs in the system by the FMB mechanism allows the VMEbus to be used in a wide range of application areas, particularly multi-processor environments.
Without the FMB mechanism, communication between and synchronisation of system boards has to be managed via the seven interrupt request lines. FMB reduces the massive time overhead normally needed to process the interrupt cycles to just one write cycle.
All CPU-81 boards provide two fully independent message broadcast channels, each designed to store one 8-bit message.

4. The Secondary Bus Interface

To support increased functionality and higher performance, the CPU-81 series processor boards feature a VME Subsystem Bus (VSB) interface. The VSB interface on the CPU-81 is a full VSB master interface, supporting read, write and Read-Modify-Write cycles, for byte, word and long word transactions. The CPU-81 contains full VSB controller functions including serial arbiter, and interrupt handler capability. This allows the CPU-81 to be used in VSB multi-master configurations.

5. The Interrupt Structure

Special on-board logic installed on the CPU-81 series handles all local and VMEbus interrupts. Each interrupt request from the local bus devices, including DUSCC and timers are combined with the seven VMEbus interrupt requests.
Each IRQ-source including the VMEbus IRQs can be programmed to interrupt the CPU. On-board logic initiates an interrupt vector fetch from the VMEbus.

6. The Memory Organization

Memory on the CPU-81 series is configured as shown in CPU-81 series memory organization. Starting VMEbus addresses and size of shared memory (DRAM) are programmable. Programmable addresses are retained in SRAM during power-down.

CPU-81 Series Memory Organization

Start Address	End Address	Type
00000000	00FFFFFF	Shared Memory (CPU-81)
01000000	03FFFFFF	Reserved
04000000	FBFFFFFF	VMEbus Address A32 : D32, D24, D16, D8
FA000000	FAFFFFFF	FMB Address Space
FB000000	FBFEFFFF	VMEbus Address A16 : D16, D8
FC000000	FEFFFFFF	Reserved
FF000000	FF7FFFFF	EPROM
FF800000	FFBFFFFF	Local I/O
FFC00000	FFFFFFFF	Control Space, CMMU Registers

7. FORCEbug/88K

FORCEbug/88K is an EPROM-based monitor. Residing in 256 Kbyte of EPROM and requiring only 64 Kbyte of RAM, FORCEbug/88K provides real time support capabilities for embedded control applications. FORCEbug/88K comprises of a monitor and software drivers.

7.1 Monitor/Debugger

The monitor supports interactive command execution for debugging. A powerful set of debugging facilities is provided to simplify program debugging activities.

These software routines include interactive assembler, symbolic disassembler, breakpoints, single stepping, memory and register display/modification. FORCEbug/88K supports definition of symbolic commands and placing symbols in a symbol table. The symbol table and use of a base register enhance the ease and capability of the debugging environment. A set of benchmark routines and a command timer provide support for system performance evaluation.

7.2 Target System Support

FORCEbug/88K is easily used in target system configurations. For these kinds of system implementations, FORCEbug/88K applications are easily programmed into EPROM.

8. Benchmarks

Performance in any CPU system depends upon many complex factors. The use of simulators or benchmarks to predict performance should be used carefully and conservatively. Provided below are published performance numbers for three common benchmark programs.

	Clock 20.0 MHz	Clock 25.0 MHz
MIPS	17	21
Dhrystones	36,000	41,000
Whetstones	16 Million	18 Million
Linpack	5,300	5,600

9. Software

It is FORCE COMPUTERS' policy to ensure that as many operating systems and kernels as possible are available to enable the user to select the most appropriate and complete solution. The software is made available and supported either by FORCE COMPUTERS or the third party vendor as outlined in the software availability table. Selection of supply and support source has been made to ensure the highest level of expertise. Since FORCE has an on-going policy to expand its software offering, please contact FORCE regarding availability of any software not listed in this datasheet.

CPU-81 Software Support

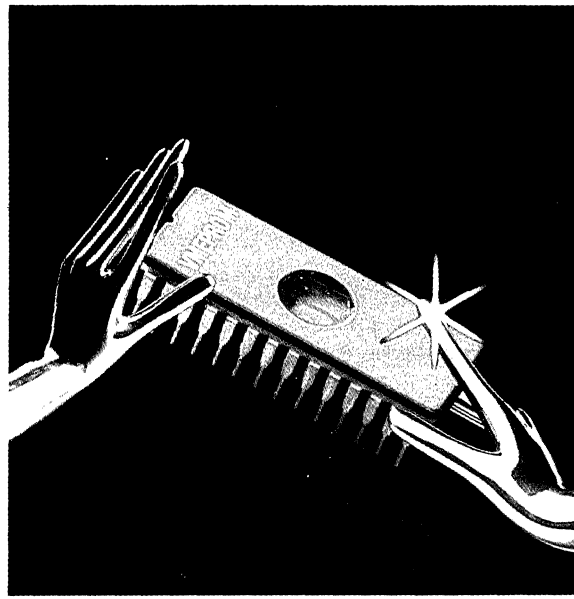
Operating System/Kernel	Vendor/Support
UNIX V.3/V.4	Contact FORCE for availability
OS-9/9000	Contact FORCE for availability
VxWORKS	Contact FORCE for availability
VRTX-32	READY SYSTEMS
pSOS	Contact FORCE for availability
ARTX	Contact FORCE for availability
Telesoft ADA	Contact FORCE for availability

Specifications

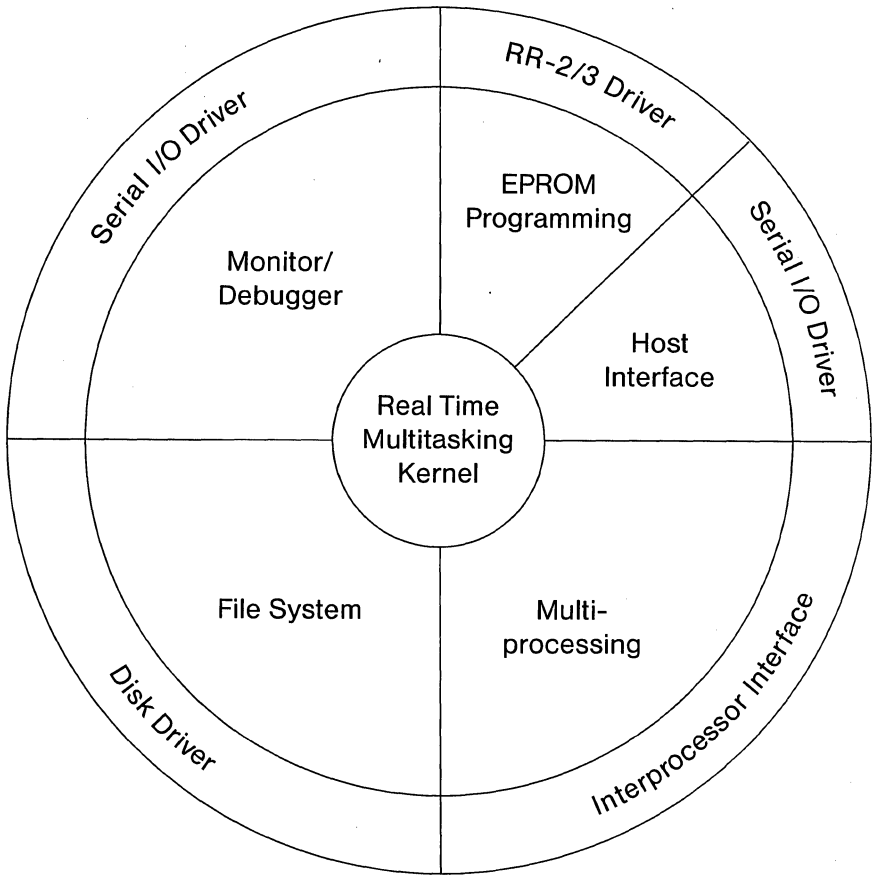
Function		
M88100/M88200 Frequency	CPU-81A/4, -81A/16 CPU-81B/16	20.0 MHz 25.0 MHz
On-board cache memory (M88200)	data cache size instruction cache size	16 Kbyte 16 Kbyte
Shared nibble mode, DRAM with parity Static RAM configuration Device used Battery back-up	CPU-81A/4 CPU-81A/16, -B/16	4 Mbyte 16 Mbyte 2 Kbyte MK48T02 yes
Real Time Clock/calendar with on-board battery back-up		MK48T02
No. of system EPROM sockets Data path Max. capacity (as devices become available)		4 32-bit 4 Mbyte
Serial I/O interfaces (total) Controller used RS232/422-compatible		2 68562 2
Counters/timers	24-bit with 5-bit prescale 16-bit with 8-bit prescale	1 2
VMEbus interface	A32, A24, A16 : D32, D16, D8 A32, A24 : D32, D16, D8, UAT IACK* daisy chain driver Four-level VMEbus arbiter SYSCLK driver	Master Slave yes yes yes
FORCE Message Broadcast FMB-FIFO -1 FMB-FIFO-2		yes 1 byte 1 byte
Front panel switches/indicators	RESET, ABORT switches Hexadecimal LED displays	yes 2
VME subsystem bus (VSB) primary master interface A32 : D8, D16, D32, UAT, RMW VSB arbiter VSB interrupt handler		yes yes serial yes
Power requirements	+ 5 V min : max + 12 V min : max – 12 V min : max	4.0 A : 5.2 A 0.1 A : 0.3 A 0.1 A : 0.3 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)		0 to + 50 °C – 40 to + 85 °C 5 to 95%
Board dimensions No. of slots used		234 × 160 mm : 9.2 × 6.3 in 1

Ordering Information

SYS88K/CPU-81A/4 Part No. 510001	20.0 MHz M88100 RISC-based CPU board with two M88200 CMMUs, 4 Mbyte shared nibble mode dynamic RAM. Documentation included.
SYS88K/CPU-81A/16 Part No. 510081	20 MHz M88100 RISC-based CPU board with two M88200 CMMUs, 16 Mbyte shared nibble mode dynamic RAM. Documentation included.
SYS88K/CPU-81B/16 Part No. 510083	25.0 MHz M88100 RISC-based CPU board with two M88200 CMMUs, 16 Mbyte shared nibble mode dynamic RAM. Documentation included.
SYS88K/CPU-80/81/UM Part No. 510008	User's manual for CPU-81 series including hardware and software descriptions.



System 68000
SYS68K/VMEPROM
PDOS Based Real Time Operating Monitor


RR-2/3 Driver
Serial I/O Driver
Serial I/O Driver
Disk Driver
Interprocessor Interface
EPROM
Programming
Monitor/
Debugger
Host
Interface
Real Time
Multitasking
Kernel
File System
Multi-
processing

General Description

VMEPROM is an EPROM based Real Time Kernel and Monitor, which is installed on all FORCE COMPUTERS 680x0 CPU boards. The complete package resides in the EPROM space on the CPU board and uses 32 Kbyte of RAM for stack and kernel parameters.

VMEPROM comprises the powerful PDOS Real Time Kernel and the PDOS file manager. These modules combined with the BIOS modules provided in each board version provide the user with a complete real time environment and support for all the on-board functions of each CPU board.

The user interface contains about 80 commands, for low-level debugging, task and file manipulation and management, real time intertask communications and board specific functions. A line assembler/disassembler for the CPU/FPCP installed on the board version is also included.

VMEPROM also contains a system call interface for use by the programmer to access the real time functions of VMEPROM from an application program. Over 100 system calls are supported allowing VMEPROM to be used as the kernel in all real time embedded application environments.

Features of the VMEPROM:

- Real Time Multi-Tasking Kernel supporting up to 64 tasks
- File management support for sequential, random and shared files. Up to 64 files may be opened at the same time
- Task management system calls
- Line assembler/disassembler with full support of all 680x0, 6888x instructions
- Over 20 commands for program debugging, including breakpoints, tracing, processor register display and modify
- Display and modify floating point data registers of the 68881/2
- S-record up/downloading from any port defined in the system
- Time stamping of user programs
- Built-in benchmarks
- Disk support for RAM-disk, floppy and Winchester disks. Either a SYS68K/ISCSI-1 or the on-board (if installed) mass memory controller may be used. VMEPROM also allows disk formatting and initialization
- Serial I/O support for up to two SIO-2 or ISIO-1/2 boards in the system
- EPROM programming utility using the SYS68K/RR-2/3 boards
- Full screen editor
- More than 30 commands to control the PDOS kernel and file manager
- Complete task management
- I/O redirection to files or ports from the command line
- Over 100 system calls to the kernel are supported
- Data conversion system calls
- Terminal I/O functions

1. VMEPROM User Interface

The user interface of VMEPROM allows I/O redirection to files or to any port defined within the system. Multiple commands may be entered on a single command line. The user console input is interrupt driven and allows type-ahead. About 80 commands are built into the VMEPROM user interface and are directly accessible without destroying memory.

The command set covers functions such as program execution, breakpoints, tracing and a powerful line assembler/disassembler. Also resident are file system functions such as append, delete, copy, rename and show file. These are applicable for RAM disk, floppy or hard disk. The task management functions cover create task, kill task, alter task priority and list tasks.

2. Kernel Functions

The kernel of VMEPROM is written in 680x0 assembly language for fast and efficient execution. It provides multi-tasking, system clock, event processing and memory management. Ready tasks are scheduled with a prioritized round-robin method. Up to 64 tasks may be defined simultaneously.

Semaphores and events provide a low overhead facility for one task to signal another. Messages and mailboxes are used in conjunction with task lock, unlock, suspend and event primitives.

VMEPROM handles user console, system clock and other hardware interrupts.

A task can be suspended pending a hardware or software event. Control is switched to a suspended task within 28 µsec (68020, 25 MHz) after the occurence of the event.

3. File Manager Functions

The file manager module provides sequential, random, read only and shared access to named files on RAM disk, floppy or hard disk. New files are automatically defined contiguously to improve access speed.
These low overhead file primitives use a linked, random access file structure and a logical sector bit map for storage allocation. Files are time stamped with the date and time of creation and last update. Up to 64 files may be open at the same time.

4. Supported VMEbus Hardware

Upon power-up, VMEPROM checks the VMEbus for the availability of several controller boards. Up to two serial I/O boards are supported, which may be the SYS68K/SIO-2 or the ISIO-2.
In addition, up to four disk drivers are supported by VMEPROM. These drivers control the SYS68K/ISCSI-1 and an on-board SCSI-controller, for example. Both the serial I/O controllers and the disk controllers are interrupt driven. EPROM programming is supported by VMEPROM utilizing the SYS68K/RR-3 board. Two commands are available to program EPROMs directly from the VMEPROM command line. The code to be programmed may reside in memory, on RAM disk or an external mass storage device such as a floppy disk or a Winchester disk.

5. Target System Support

VMEPROM can easily be used in target systems. For these systems, the application program can be put into EPROM with or without the user interface. The application programs can be started either by a command line or directly after reset without user input.
The minimum EPROM space required by the VMEPROM kernel and file manager is about 64 Kbyte. Small ROMable applications can be put in EPROMs easily without the overhead of the user interface.

6. Networking Support

Networking support is provided for VMEPROM on boards which have an Ethernet interface, e.g. CPU-30 and CPU-37. The networking package, SYS68K/EMOD-VM/xx is delivered on a floppy disk and provides support for the TCP/IP networking protocols, FTP (File Transfer Protocol) and Telnet (Remote Login). In addition, VMEPROM also supports basic single data packet I/O over Ethernet through simple system calls.

7. Development Systems

Currently either one of the FORCE PDOS or UNIX System V development stations may be used for software development for VMEPROM. Compilers, assemblers, and libraries are available together with utilities for program downloading. These tools are well suited to help in program development and debugging.

7.1 UNIX System V Development Systems

The FORCE FOCUS UNIX System V family of development systems contains the UNIX to VMEPROM link. This package is available free of charge on every FORCE UNIX system. It consists of C – libraries and utilities making the software development for VMEPROM under UNIX an easy task.
Also supported under UNIX are EPROM programming as well as program downloading to the target system using S-records.
A transparent mode is also available thus supporting the debugging and execution of VMEPROM tasks from the UNIX console. Optionally available is a High Level Debugger (SYS68K/HLD) which allows C-Language source level debugging for VMEPROM applications from a FORCE UNIX host. A VMEPROM to UNIX communication package (SYS68K/VUCP) is also available, which allows UNIX processes and VMEPROM tasks to communicate with each other at runtime either via the VMEbus backplane or via a serial interface.

7.2 PDOS Development Systems

As VMEPROM is based on the powerful PDOS* Real Time Kernel, the PDOS operating system is well suited for software development for VMEPROM. The PDOS operating system supports EPROM programming and code downloading to VMEPROM via S-records. The transparent mode is also supported under PDOS to allow program debugging from the PDOS terminal.
No additional tools or utilities are required when using the PDOS operating system for software development for VMEPROM.

7.3 IBM-PC/AT Development Systems

VMEPROM is also supported by the family of IBM-AT or true compatible development systems. The link comprises a C-compiler and a cross assembler for the 680x0 processor family and utilities to download the code to the target systems for debugging.

7.4 Other Development Systems

The support of VMEPROM through other development systems like the SUN workstation or the VAX is available through third parties. These cross-software development packages include compilers, cross-assemblers and libraries to fully support program development for VMEPROM based target systems.

8. Licensing

No license is required for VMEPROM. VMEPROM is delivered free of charge and is currently implemented on the following FORCE CPU-boards:

- SYS68K/CPU-4
- SYS68K/CPU-5
- SYS68K/CPU-6
- SYS68K/CPU-22
- SYS68K/CPU-23
- SYS68K/CPU-26
- SYS68K/CPU-27
- SYS68K/CPU-29
- SYS68K/CPU-30
- SYS68K/CPU-31
- SYS68K/CPU-32
- SYS68K/CPU-33
- SYS68K/CPU-37
- SYS68K/CPU-40
- SYS68K/CPU-41

This gives full software compatibility and portability between the above listed CPU-boards.

9. Command Set Summary

#	Name Processor
AF	Append File
ARB	Set Arbiter
AS	Line Assembler
ASSIGN	Set Port Number
BASE	Set Base
BENCH	Benchmarks
BF	Block Fill
BM	Block Move
BOOT	Boot an Operating System
BP	Baud Port
BR	Breakpoints
BS	Block Search
BT	Block Test
BV	Block Verify
CF	Copy File(s)
CONFIG	Configure VMEbus
COLD	Coldstart VMEPROM
CT	Create Task
DD	Disk Dump
DF	Define File
DI	Disassembler
DL	Delete File(s)
DN	Disk Name
DR	Display Registers
DRF	Display 68881 Regs
DT	Show Date/time
DU	Dump S-Record
ED	Screen Editor
ER	Display Error
EV	Events
FD	File Dump
FM	Free Memory
FRMT	Format Disk
FS	File Slot Usage
G	Execute Program
GD	Go Direct
GM	Get Memory
GO	Alias for G
GOTO	Goto String
GT	Go W/Temp. Break
HIST*	Command History
IA	File Altered
ID	Set Date and Time
IN*	Install Programs
INFO*	CPU-board Information
INIT	Init Disk
INSTALL	Install Driver
KM	Kill Message
KT	Kill Task
LC	List Directory Compact
LD	Load File to Mem
LO	Load S-Record
LS	List Directory
LT	List Tasks
LV	Directory Level
M	Modify Memory
MD	Dump Memory
MEM	Set Bus Width
MF	Make File
MM	Alias for M
MS	Memory Set
PROMPT	Change Prompt
RC	Reset Console
RD	Set RAM Disk
RM	Register Modify
RN	Rename File(s)
RR2	Program EPROMs
RS	Reset Disk
SA	Set Attribute
SF	Show File
SM	Send Message
SP	Disk Space
ST	Set Terminal Type
SV	Save to File
SY	Set System Disk
T	Trace Program
TC	Set Trace Count
TIME	Measure Runtime
TJ	Trace on Jumps
TM	Transparent Mode
TP	Set Task Priority
TT	Alias for T
UN	Set Unit Mask
ZM	Zero Memory

* = available on 32-bit CPUs

10. System Call Summary

X881	SAVE 68881 ENABLE
XAPF	APPEND FILE
XBCP	BAUD CONSOLE PORT
XCBC	CHECK FOR BREAK CHARACTER
XCBD	CONVERT BINARY TO DECIMAL
XCBH	CONVERT BINARY TO HEX
XCBM	CONVERT TO DECIMAL W/MESSAGE
XCBP	CHECK FOR BREAK OR PAUSE
XCBX	CONVERT TO DECIMAL IN BUFFER
XCDB	CONVERT ASCII TO BINARY
XCFA	CLOSE FILE W/ATTRIBUTE
XCHX	CONVERT BINARY TO HEX IN BUFFER
XCLF	CLOSE FILE
XCLS	CLEAR SCREEN
XCPY	COPY FILE
XCTB	CREATE TASK BLOCK
XDEV	DELAY SET/RESET EVENT
XDFL	DEFINE FILE
XDLF	DELETE FILE
XDMP	DUMP MEMORY FROM STACK
XDPE	DELAY PHYSICAL EVENT
XDTV	DEFINE TRAP VECTORS
XERR	RETURN ERROR TO VMEPROM
XEXC	EXECUTE PDOS CALL D7.W
XEXT	EXIT TO VMEPROM
XFAC	FILE ALTERED CHECK
XFBF	FLUSH BUFFERS
XFFN	FIX FILE NAME
XFTD	FIX TIME & DATE
XFUM	FREE USER MEMORY
XGCB	CONDITIONAL GET CHARACTER
XGCC	GET CHARACTER CONDITIONAL
XGCP	GET PORT CHARACTER
XGCR	GET CHARACTER
XGLB	GET LINE IN BUFFER
XGLM	GET LINE IN MONITOR BUFFER
XGLU	GET LINE IN USER BUFFER
XGML	GET MEMORY LIMITS
XGMP	GET MESSAGE POINTER
XGNP	GET NEXT PARAMETER
XGTM	GET TASK MESSAGE
XGUM	GET USER MEMORY
XISE	INITIALIZE SECTOR
XKTB	KILL TASK
XKTM	KILL TASK MESSAGE
XLDF	LOAD FILE
XLER	LOAD ERROR REGISTER
XLFN	LOOK FOR NAME IN FILE SLOTS
XLKF	LOCK FILE
XLKT	LOCK TASK
XLSR	LOAD STATUS REGISTER
XNOP	OPEN SHARED RANDOM FILE
XPAD	PACK ASCII DATE
XPBC	PUT BUFFER TO CONSOLE
XPCC	PUT CHARACTER(S) TO CONSOLE
XPCL	PUT CRLF TO CONSOLE
XPCP	PLACE CHARACTER IN PORT BUFFER
XPCR	PUT CHARACTER RAW
XPDC	PUT DATA TO CONSOLE
XPEL	PUT ENCODED LINE TO CONSOLE
XPEM	PUT ENCODED MESSAGE TO CONSOLE
XPLC	PUT LINE TO CONSOLE
XPMC	PUT MESSAGE TO CONSOLE
XPSC	POSITION CURSOR
XPSF	POSITION FILE
XPSP	PUT SPACE TO CONSOLE
XRBF	READ BYTES FROM FILE
XRCN	RESET CONSOLE INPUTS
XRCP	READ PORT CURSOR POSITION
XRDE	READ NEXT DIRECTORY ENTRY
XRDM	DUMP REGISTERS
XRDN	READ DIRECTORY ENTRY BY NAME
XRDT	READ DATE
XRFA	READ FILE ATTRIBUTES
XRFP	READ FILE POSITION
XRLF	READ LINE FROM FILE
XRNF	RENAME FILE
XROO	OPEN RANDOM READ ONLY FILE
XROP	OPEN RANDOM
XRPS	READ PORT STATUS
XRSE	READ SECTOR
XRSR	READ STATUS REGISTER
XRST	RESET DISK
XRSZ	READ SECTOR ZERO
XRTE	RETURN FROM INTERRUPT
XRTM	READ TIME
XRTP	READ TIME PARAMETERS
XRTS	READ TASK STATUS
XRWF	REWIND FILE
XSEF	SET EVENT FLAG W/SWAP
XSEV	SET EVENT FLAG
XSMP	SEND MESSAGE POINTER
XSOE	SUSPEND ON PHYSICAL EVENT
XSOP	OPEN SEQUENTIAL FILE
XSPF	SET PORT FLAG

XSTM SEND TASK MESSAGE	XULT UNLOCK TASK
XSTP SET/READ TASK PRIORITY	XUSP RETURN TO USER MODE
XSUI SUSPEND UNTIL INTERRUPT	XUTM UNPACK TIME
XSUP ENTER SUPERVISOR MODE	XVEC SET/READ EXCEPTION VECTOR
XSWP SWAP TO NEXT TASK	XWBF WRITE BYTES TO FILE
XSZF GET DISK SIZE	XWDT WRITE DATE
XTAB TAB TO COLUMN	XWFA WRITE FILE ATTRIBUTES
XTEF TEST EVENT FLAG	XWFP WRITE FILE PARAMETERS
XTLP TRANSLATE LOGICAL TO PHYSICAL EVENT	XWLF WRITE LINE TO FILE
	XWSE WRITE SECTOR
XUAD UNPACK ASCII DATE	XWTM WRITE TIME
XUDT UNPACK DATE	XZFL ZERO FILE
XULF UNLOCK FILE	

Ordering Information

SYS68K/EMOD-VM/30 Part No. 141114	TCP/IP Software support for CPU-30 VMEPROM. Documentation included.
SYS68K/EMOD-VM/37 Part No. 141113	TCP/IP Software support for CPU-37 VMEPROM. Documentation included.
SYS68K/HLD Part No. 141100	High level C language debugger for VMEPROM tasks, running on a UNIX host. Documentation included.
SYS68K/VUCP Part No. 140109	VMEPROM/UNIX runtime communication package. Documentation included.
SYS68K/EMOD-PDOS/UM Part No. 800172	EMOD User's Manual for TCP/IP for PDOS and VMEPROM.
SYS68K/VMEPROM Link-1 Part No. 140110	Software link from the IBM-AT to VMEPROM. Documentation included.
SYS68K/VMEPROM/UM Part No. 800140	VMEPROM User's Manual.
SYS68K/VMEPROM Link-1/UM Part No. 800150	User's Manual for IBM PC/AT VMEPROM cross development.

Note: VMEPROM will be supplied free of charge on all future 680x0-based CPU board designs from FORCE COMPUTERS.

General Information

16-Bit CPU Boards

32-Bit CPU Boards

Memory Boards

Controller Boards

I/O Cards

Accessories

FORCE COMPUTERS

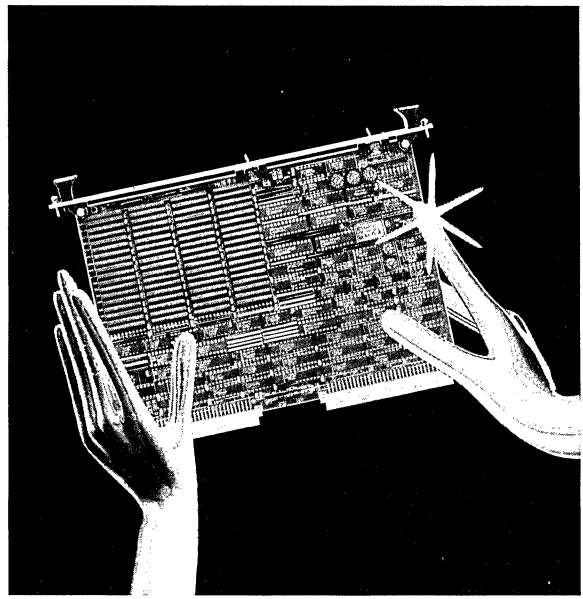
Memory Board Introduction

The DRAM-8 dynamic RAM board is offered in 2 Mbyte, 4 Mbyte, 8 Mbyte, 16 Mbyte or 32 Mbyte configurations. The board is in volume production and offers the best "price per bit" in the industry. The flexibility in density, offered as a single slot solution allows the DRAM-8 to be configured into virtually any application environment. FORCE also offers one of the fastest SRAM boards on the market. SRAM-6 provides 2 Mbyte of static memory with read and write accesses of 55 nsec.

If it is an EPROM board on the VMEbus that you require, then the SYS68K/RR-2 will fit your application needs. This board offers the unique feature of being able to test your application in SRAM and then program your EPROM in a VMEbus environment without the need for expensive EPROM programmers. The board may then be used as a standard memory card. RR-2 provides the solution to EPROM resident applications.

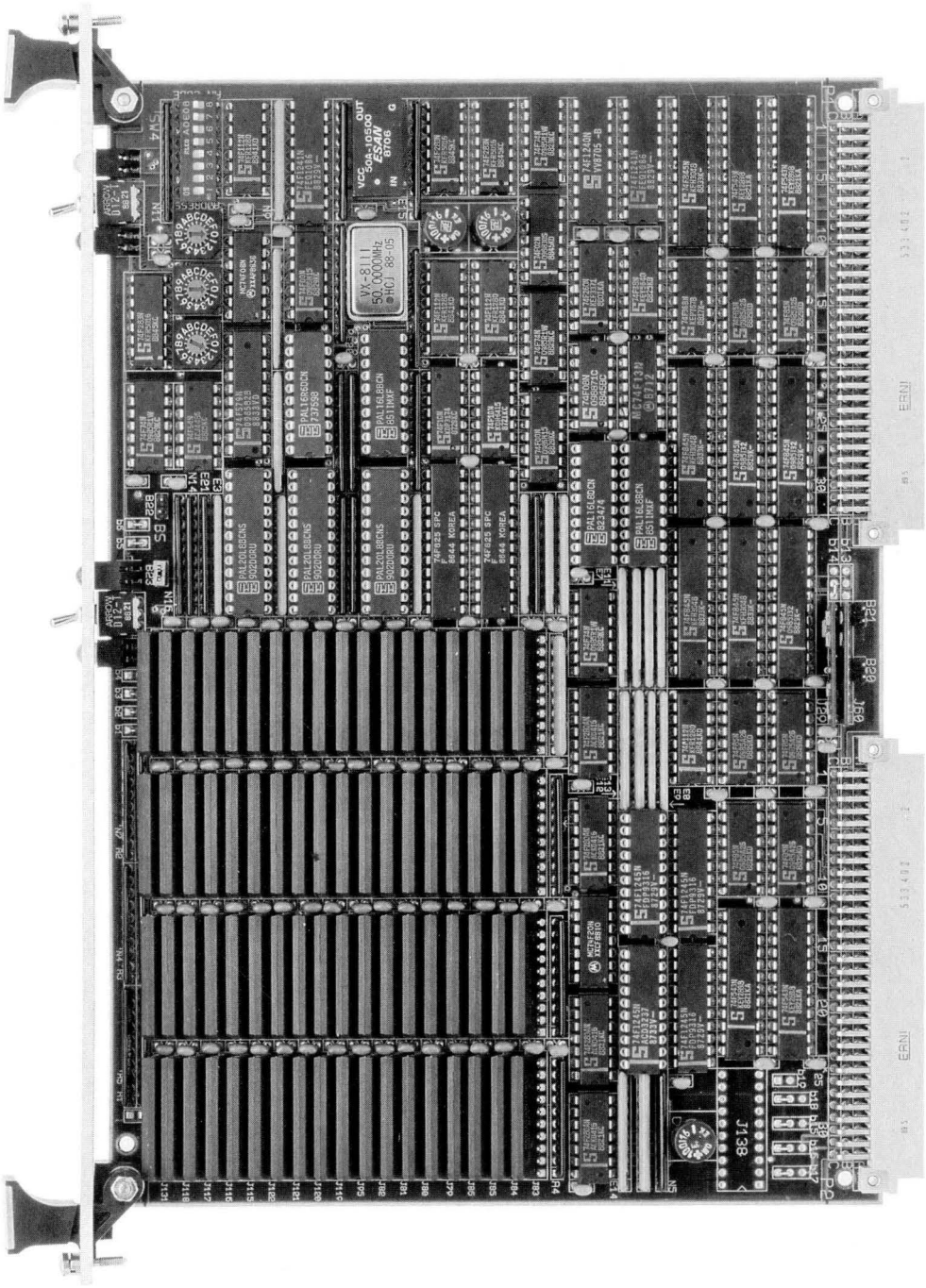
Memory Boards

FAMILY	DRAM-8	SRAM-3B	SRAM-6	RR-2
Memory type	Dynamic RAM	Static RAM	Static RAM	Static RAM ROM, EPROM, EEPROM
Capacity min. max. No. of memory areas No. of JEDEC sockets	2 Mbyte 32 Mbyte 1/2 0	1 Mbyte 1 Mbyte 2 16	2 Mbyte 2 Mbyte 2 0	 16 Mbyte 2 16
Device organization	256 Kbyte × 1, 1 Mbyte × 1, 4 Mbyte × 1	32 Kbyte × 8	256 Kbyte × 1	various
Byte parity	yes	no	no	no
Battery back-up Retension time (calculated)	yes (via P1/P2) depending on supply	yes (on-board) 6000 h	yes (on-board) 6000 h	yes (on-board) device dependent
Address decoding Decoding boundary Data transfer size	A24, A32 1 Mbyte D8, D16, D32	A24, A32 512 Kbyte D8, D16, D32	A24, A32 2 Mbyte D8, D16, D32	A24, A32 various D8, D16, D32
Unaligned transfers	yes	yes	yes	yes
Read Modify Write	yes	yes	yes	yes
Read access time typ. Write access time typ.	250 nsec 100 nsec	210 nsec 80 nsec	55 nsec 55 nsec	selectable selectable
VMXbus interface	no	yes	no	yes
Address decoding Decoding boundary Data transfer size		A24 512 Kbyte D8, D16, D32		A24 various D8, D16, D32
Unaligned transfers Read Modify Write	yes yes	yes yes	yes yes	yes yes



System 68000 VME
SYS68K/DRAM-8

Flexible 32-Bit Dynamic Memory Board

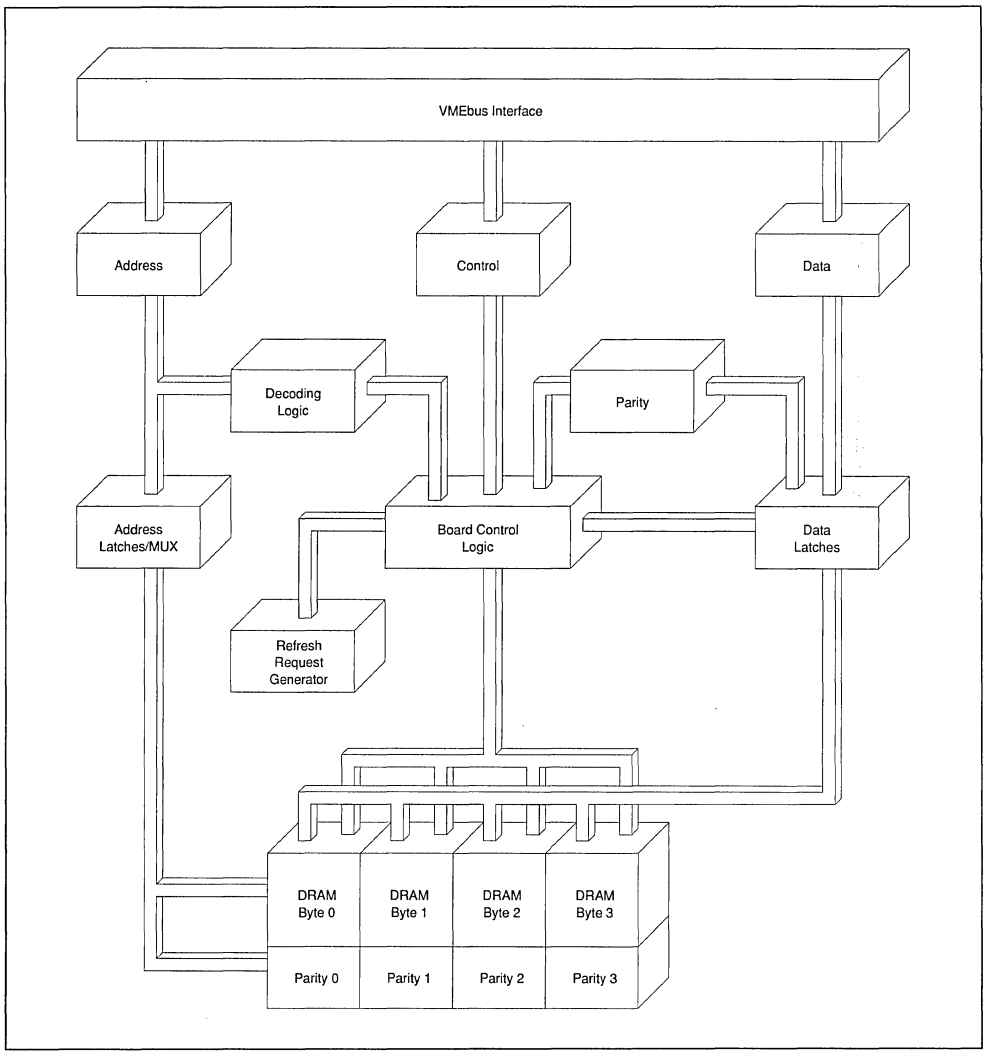


General Description

The SYS68K/DRAM-8 board is a flexible memory board using dynamic RAMs. It provides up to 32 Mbyte of memory, including byte parity generation/check, supporting all 32 address and 32 data lines as defined in the IEEE 1014 Standard (VMEbus Rev. C). The access address and address modifier are selectable via switches.

High speed data throughput on the VMEbus is provided by the on-board logic which allows typical read access times of 230 nsec and write access times of 80 nsec using 120 nsec DRAMs. Easy installation is possible because the access address and the address modifier are selectable via switches in steps of 1 Mbyte.

Block Diagram of the SYS68K/DRAM-8



Features of the SYS68K/DRAM-8

- 2 Mbyte DRAM on DRAM-8A
  4 Mbyte DRAM on DRAM-8B
  8 Mbyte DRAM on DRAM-8C
  16 Mbyte DRAM on DRAM-8D
  32 Mbyte DRAM on DRAM-8E
- Access Times: Read: 230 nsec (typ)
  Write: 80 nsec (typ)
- 32 address and 32 data signals supported
- Switchable byte parity generation/check
- Interleaved refresh every 15 µsec
- Memory content retention possible via additional external supply
- VMEbus interface:
  - A32 : D32, D16, D8, UAT, RMW, ADO
  - A24 : D32, D16, D8, UAT, RMW, ADO
- RUN/LOCAL switch
- Write protect switch
- Access indicator LED
- Write protect LED
- FAIL indicator

1. Memory Capacity and Organization

The DRAM-8 consists of one or two memory banks, depending on capacity. Each bank uses 32 RAM chips for data storage and four devices for parity information.
The memory capacity of the DRAM-8 versions is shown in the table below:

Type	No. of Banks	Capacity per Bank	Total Capacity	Used Devices
DRAM-8A	2	1 Mbyte	2 Mbyte	256 K × 1
DRAM-8B	1	4 Mbyte	4 Mbyte	1 M × 1
DRAM-8C	2	4 Mbyte	8 Mbyte	1 M × 1
DRAM-8D	1	16 Mbyte	16 Mbyte	4 M × 1
DRAM-8E	2	16 Mbyte	32 Mbyte	4 M × 1

The selected address modifier code for standard or extended addressing defines the decoding range of the memory (A24 or A32). Automatic adjustment to the VMEbus data transfer type (D8, D16, D24 or D32) is provided. The IEEE 1014 unaligned transfers (Read, Write and Read-Modify-Write) are supported.

Transfer	D31-24	D23-16	D15-8	D7-0	RMW
Byte				x	x
			x		x
Word			x	x	x
Long Word	x	x	x	x	x
Unaligned Transfers	x	x	x		x
		x	x		x
		x	x	x	x

1.1 The Parity Check

Byte parity check circuitry is installed on the board to provide error checking.
If a parity error occurs, the red fail LED on the front panel illuminates and a BERR is driven on the VMEbus. The latched error status can be reset via the Run/Local switch or a SYSRESET*.

1.2 Access Times

The DRAM-8 contains address and data latches to provide high speed throughput to the VMEbus. If an access is performed on the DRAM-8 board, the green access LED on the front panel is illuminated.

Access mode	Typ	Max
Write	80	100
Read	230	250
Overhead time for refresh	245	320

1.3 Refresh

After an access cycle is completed, a pending refresh request (every 15 µsec) is executed independent from all VMEbus activities. Therefore the VMEbus protocol overhead time is used to refresh the DRAMs. In addition to the refresh interleave, a refresh to the DRAMs is performed if no on-board access is detected 15 µsec after the execution of the last refresh.

1.4 The Address Selection

Easy selection of address and address modifier codes is provided through switches. The access address is selectable in increments of 1 Mbyte, throughout the entire 4 Gbyte address range of the VMEbus.
The following address modifier codes are selectable via switches. Each of the AM-codes can be enabled separately via a switch setting.

Usable Address Modifier Codes:

Hex Code	Address Modifier	Function
3E	HHHHHL	Standard Supervisory Program Access
3D	HHHHLH	Standard Supervisory Data Access
3A	HHHLHL	Standard Non Privileged Program Access
39	HHHLLH	Standard Non Privileged Data Access
0E	LLHHHL	Extended Supervisory Program Access
0D	LLHHLH	Extended Supervisory Data Access
0A	LLHLHL	Extended Non Privileged Program Access
09	LLHLLH	Extended Non Privileged Data Access

1.5 RUN/LOCAL Switch

A RUN/LOCAL switch can be used to isolate the DRAM-8 board from the VMEbus during maintenance or for test purposes.

1.6 Write Protect Switch

A write protect switch is available on the front panel of the DRAM-8. This switch allows the user to protect the memory from write accesses from the VMEbus. This is useful for debugging software which will later be programmed in EPROMs.

1.7 Memory Back-up

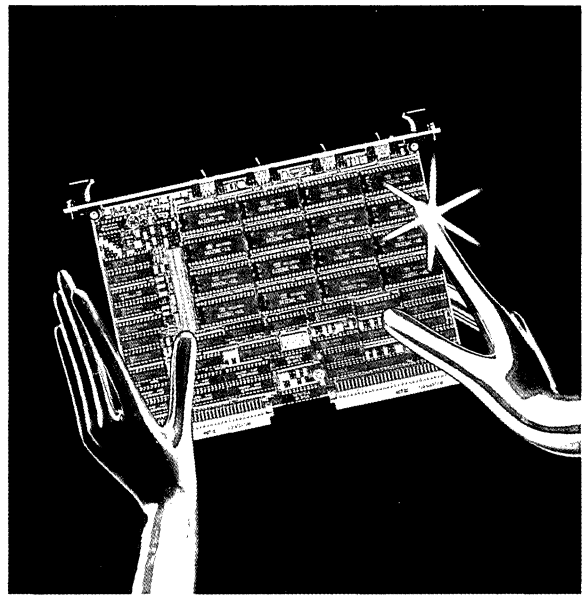
The DRAM-8 allows an exclusive external supply for the RAM area and the refresh circuitry. If the VMEbus power fails, the information in the DRAM chips is preserved. (The external supply is connected via the P1 and P2 connectors of the VMEbus interface, pins P1/31b, P2/30a, P2/31a, P2/32a.)

Specifications

Function		
Memory Capacity:	DRAM-8A DRAM-8B DRAM-8C DRAM-8D DRAM-8E	2 Mbyte 4 Mbyte 8 Mbyte 16 Mbyte 32 Mbyte
Used DRAM devices:	DRAM-8A DRAM-8B DRAM-8C DRAM-8D DRAM-8E	256 K × 4 1 M × 1 1 M × 1 4 M × 1 4 M × 1
IEEE 1014 interface compatible A32 : D32, D16, D8, UAT, RMW, ADO A24 : D32, D16, D8, UAT, RMW, ADO		yes yes yes
Access Times: Read access time without refresh (typ : max) Write access time without refresh (typ : max)		 230 nsec : 250 nsec 80 nsec : 250 nsec
Power requirements:	+ 5 V (refresh/peak) + 5 V (max) + 5 V (typ)	7.6 A 4.5 A 3.8 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)		0 to + 50 °C – 55 to + 85 °C 5 to 95 %
Board dimensions		234 × 160 mm : 9.2 × 6.3 in

Ordering Information

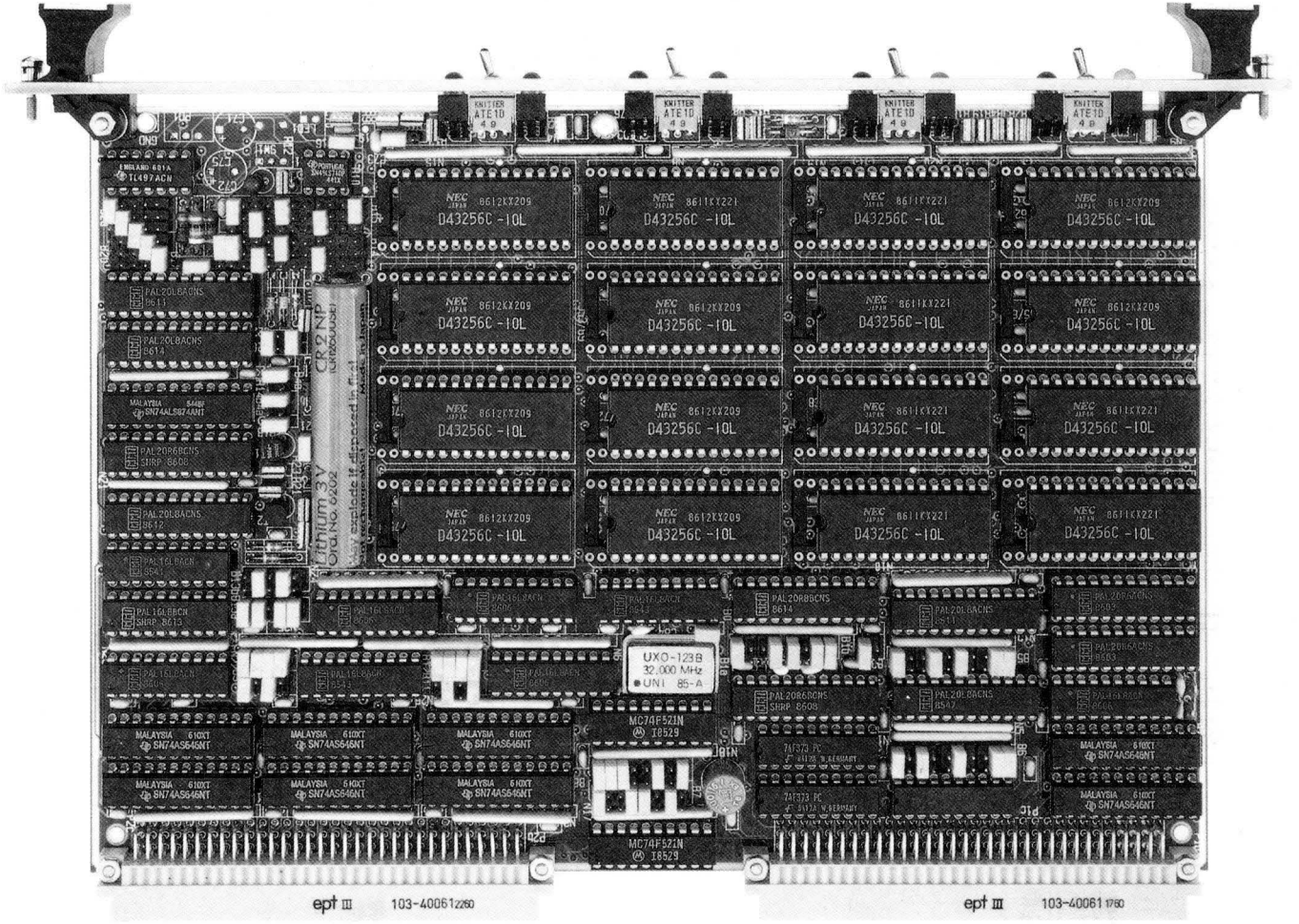
SYS68K/DRAM-8A Part No. 200150	2 Mbyte DRAM board. Documentation included.
SYS68K/DRAM-8B Part No. 200151	4 Mbyte DRAM board. Documentation included.
SYS68K/DRAM-8C Part No. 200152	8 Mbyte DRAM board. Documentation included.
SYS68K/DRAM-8D Part No. 200153	16 Mbyte DRAM board. Documentation included.
SYS68K/DRAM-8E Part No. 200154	32 Mbyte DRAM board. Documentation included.
SYS68K/DRAM-8/UM Part No. 800156	Hardware User's Manual for the SYS68K/DRAM-8 board.



System 68000 VME

SYS68K/SRAM-3B

32-Bit Static RAM Board with VMEbus and VMXbus Interface

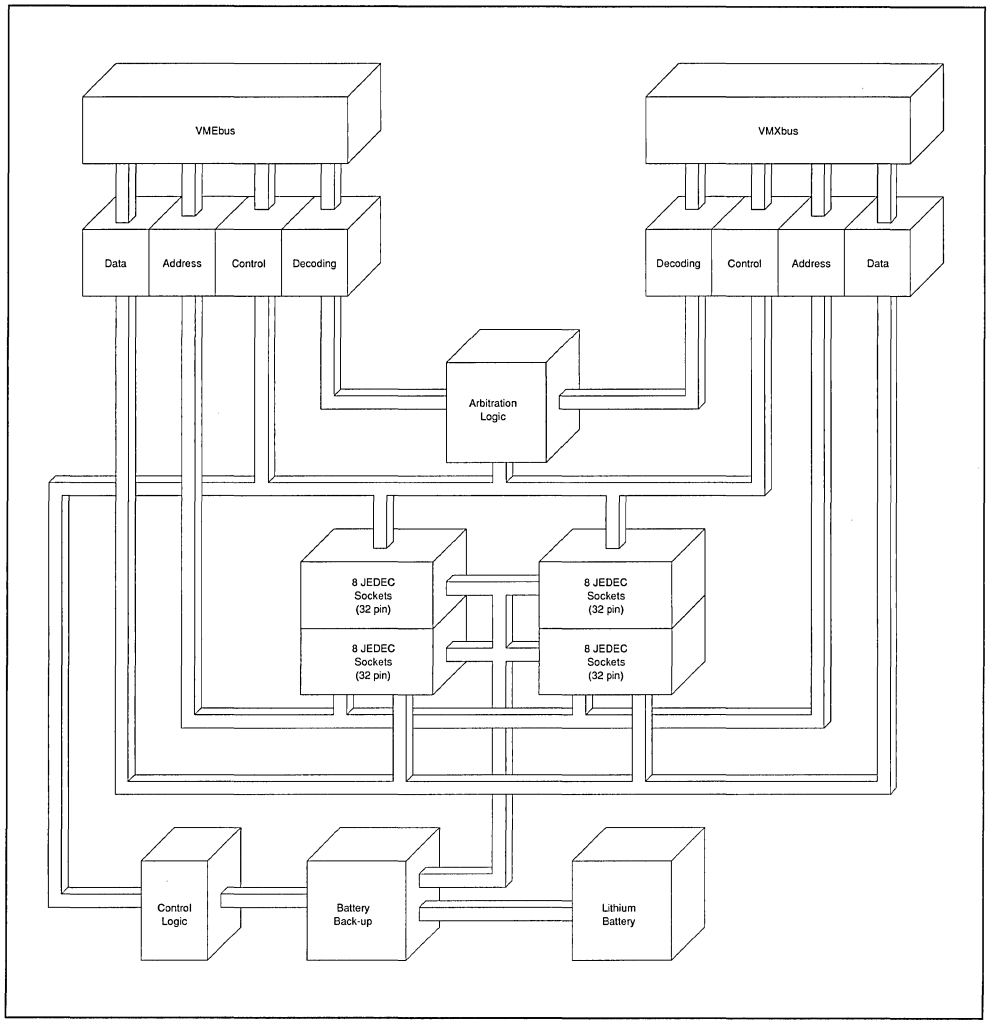

KNITTER ATE10 49
NEC JAPAN 8612KX209 D43256C-10L
NEC JAPAN 8611KX221 D43256C-10L
Lithium 3V CR2NP
UXO-123B 32.000 MHz UNI 85-A
MC74F521N
MALAYSIA 610XT SN74AS646NT
ept III 103-40061 2260
ept III 103-40061 1760

General Description

The SYS68K/SRAM-3B board provide full static memory with an on-board battery back-up accessible from the VMEbus as well as from the VMXbus. The 32-bit address and data support in conjunction with the fast static RAMs offers high data throughput with maximum reliability. Access address and address modifier code of the two memory areas are jumper-selectable.

The SRAM-3B provides 1 Mbyte of dual ported high speed static RAM. The two memory areas, both holding half of the memory capacity can be assigned to respond to VMEbus only, VMXbus only, or VMEbus and VMXbus transfers. An on-board voltage sensor detects if the main power is out of specification and enables the on-board battery back-up for the SRAMs realized with a lithium battery.

Block Diagram of the SYS68K/SRAM-3B



Features of the SYS68K/SRAM-3B

- 1024 Kbyte SRAM
- VMEbus interface supporting the following date transfer modes:
  A24 : D32, D16, D8, UAT,RMW, ADO
  A32 : D32, D16, D8, UAT,RMW, ADO
  Read-Modify-Write cycles are supported for multi-processor synchronization with the VMXbus
- VMXbus interface supporting the following data transfer modes:
  A24 : D32, D16, D8, UAT,RMW, ADO
  Read-Modify-Write cycles are supported for multi-processor synchronization with the VMEbus
- Two memory areas which each have separate jumper-selectable access addresses and address modifier codes
- On-board battery back-up provides data retention for up to one year

Typical access times:

	VMEbus	VMXbus
Write	80 nsec	70 nsec
Read	210 nsec	210 nsec

1. Functional Description

The SRAM-3B static RAM board provides 1 Mbyte of dual ported memory. VMXbus and VMEbus accesses are supported and a fast arbitration logic provides only 35 nsec overhead when switching from one bus interface to the other. The fully latched address and data buses provide an interleaved write operation to minimize bus overhead and support a maximum transfer rate on the VMEbus of 4M transfer/sec which results in a 16 Mbyte/sec data throughput using 32-bit data path.
Installation in 16- or 32-bit environments is provided through the address modifier decoding (A24 or A32 mode) which defines the address range to be decoded. Automatic data bus sizing and adaptation to 16- or 32-bit environments is provided through the on-board hardware logic. The functional details of the VMEbus and VMXbus interface, the battery back-up and the decoding are described in the following paragraphs.

1.1 The VMEbus Interface

A full VMEbus IEEE 1014 Standard compatible interface which supports the unaligned transfers is installed on the SRAM-3B boards.
32-bit of data and address are supported to take full advantage of 16- and 32-bit processor boards and DMA Controllers.
The following table lists the supported data transfer modes:

Transfer Type	D31–24	D23–16	D15–8	D7–0
Byte			x	x
Word			x	x
(unaligned)		x	x	
3 Byte		x	x	x
(unaligned)	x	x	x	
Long Word	x	x	x	x

The address and data transfer modes supported on the SRAM-3B board are:

A24 : D32, D16, D8, UAT,RMW, ADO
A32 : D32, D16, D8, UAT,RMW, ADO

Installation in 16- and 32-bit environments is possible using the address modifier selection. Each of the two fully independent memory areas, each consisting of half of the memory size, contains its own decoding logic, which allows the separation and assignment of different data/program segments. A RUN/LOCAL switch to enable or disable accesses from the VMEbus is installed on the SRAM-3B board. This switch allows the assignment of the board to the VMXbus or as a dual ported memory if the corresponding switch for the VMXbus interface is set to disable the VMXbus interface, only VMEbus transfers are allowed.
For multi-processor synchronization, all defined Read-Modify-Write cycles are supported. A VMEbus Read and the following Write transfer cannot be interrupted by a VMXbus data transfer modifying the same memory location.
The maximum data throughput of the SRAM-3B is 16 Mbyte/sec without any concurrent VMXbus data transfers.

1.2 The VMXbus Interface

A VMXbus Rev. B compatible interface supporting 32-bit data transfers is installed on the SRAM-3B. The supported VMEbus data transfer modes are: A24, D32, D16, D8.
The 23 address lines of the VMXbus are decoded and the access addresses for each of the two memory areas are jumper-selectable within the A24 address range.
The access addresses of the VMEbus standard addressing mode and the VMXbus are identical to maintain linear addressing.
Via front panel switches the SRAM-3B can be set into the following modes:

Mode A:	VMEbus access only
Mode B:	VMXbus access only
Mode C:	VMEbus and VMXbus accesses
Mode D:	Disable of the VMEbus and VMXbus interface

The Read-Modify-Write cycles defined in the VMXbus specification are supported to synchronize multiple CPU boards if the VMEbus and the VMXbus interface is enabled.
The real data throughput on the VMXbus interface without concurrent transfers on the VMEbus side is 13 Mbyte/s using 32-bit data transfers.

VMXbus Acess Times:

Write:	70 ns	No concurrent
Read:	210 ns	VMEbus accesses

1.3 Address Decoding

Unique address decoding logic providing a jumper-selectable access address is installed on the SRAM-3B. The address lines A31 to A24 of the VMEbus are only decoded if the Extended Address Modifier code is selected. Otherwise, only the address signals up to A23 of the VMEbus and the VMXbus are used if the board is addressed or not. The two independent memory areas can be placed in the 4 Gbyte address range in 512 Kbyte steps, depending on the memory capacity. This allows the adaption of the SRAM-3B to various applications without mirroring memory and losing capacity.

The memory capacity of the SRAM-3B board split into two memory areas, each consisting of exactly half the total capacity of 1 Mbyte.
The SRAM-3B contains 32 sockets supporting 32 devices with a 32 K × 8 organization.

1.4 Battery Back-Up

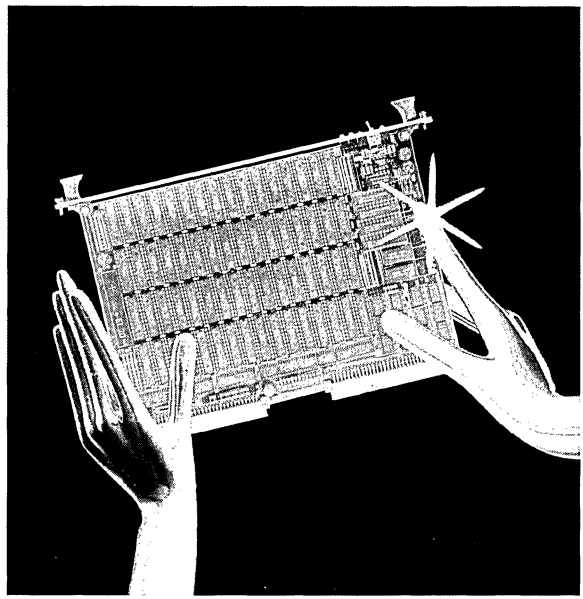
The SRAM-3B includes power fail detection circuitry and a lithium battery to guarantee data retention of the static RAMs for up to one year (calculated). Data retention is also supported via the + 5 V STDBY line.
The board automatically detects when the + 5 V power drops below 4.65V and does not respond to the VMEbus and the VMXbus. In this case all the chip enable and select signals are driven inactive and the power-down mode is activated.

Specifications

Function	
Memory capacity Memory banks (Independent) Memory devices used Independent Write protection for each bank	1 Mbyte 2 32 K × 8 yes
VMEbus interface A32 : D32, D16, D8, UAT, RMW, ADO A24 : D32, D16, D8, UAT, RMW	 yes yes
VMXbus interface (Rev. B) A24 : D32, D16, D8, UAT, RMW	 yes
VMEbus access times Read min : max Write min : max	 210 : 370 ns 80 : 240 ns
VMEbus access times Read min : max Write min : max	 210 : 380 ns 70 : 250 ns
Data retention with on-board battery	8000 hours (calculated)
Power Requirements + 5 V	5.6 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non condensing)	0 to + 50 °C – 50 to + 85 °C 5 to 90 %
Board dimensions	233 × 160 mm : 9.2 × 6.3 in

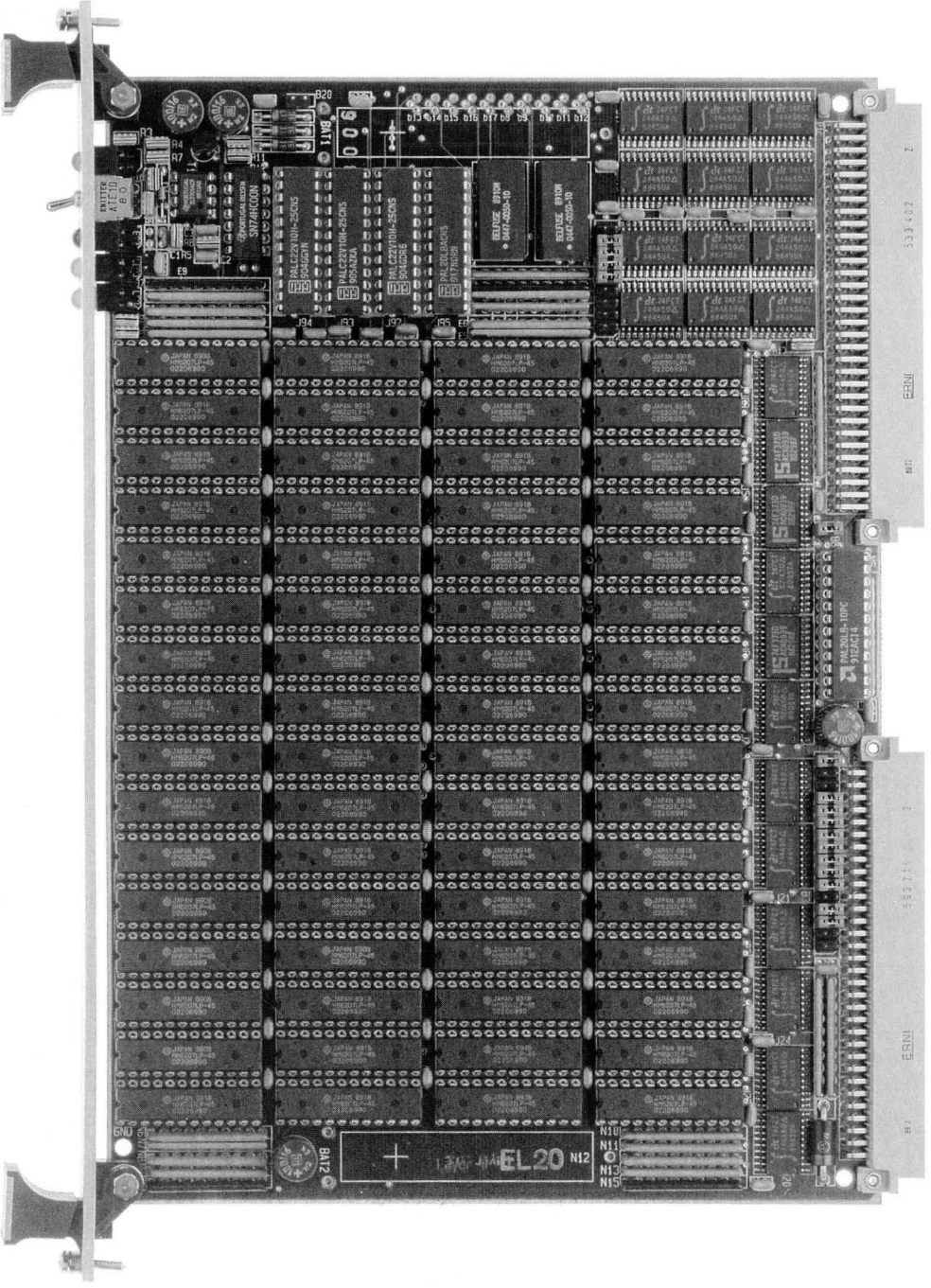
Ordering Information

SYS68K/SRAM-3B Part No. 200402	1 Mbyte static RAM board with VMEbus and VMXbus interface. Documentation included.
SYS68K/SRAM-3B/UM Part No. 800104	User's Manual for the SYS68K/SRAM-3B board.



System 68000 VME
SYS68K/SRAM-6

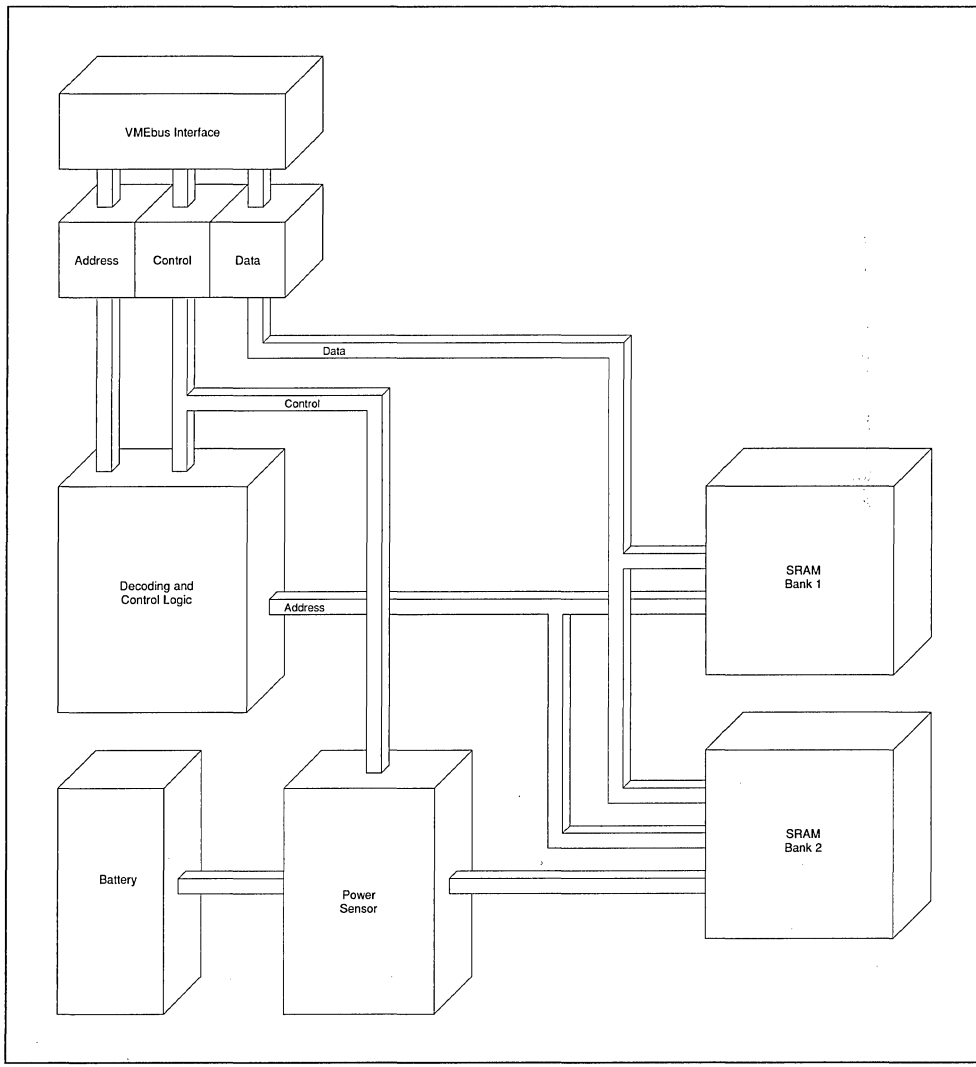
32-Bit High Speed
Static RAM Board


BAT1
BAT2
EL20
N12
J94
J93
J92
J95
J21
J24
ERNI

General Description

The SYS68K/SRAM-6 boards provides 2 Mbyte fast static memory which is accessible via the VMEbus, taking full advantage of the VMEbus bandwidth. The-32 bit address and data support, in conjunction with the fast static RAMs, offers high data throughput with maximum reliability. The Access address and address modifier codes of the two memory areas are jumper-selectable. An on-board voltage sensor detects if the supply voltage is out of specification and enables the on-board battery back-up (two lithium batteries) for the SRAMs.

Block Diagram of the SYS68K/SRAM-6



Features of the SYS68K/SRAM-6

- SRAM-6: 2048 Kbyte SRAM
- VMEbus interface supports the following data transfer modes:
  A24 : D32, D16, D8, UAT, RMW, ADO
  A32 : D32, D16, D8, UAT, RMW, ADO
  Read-Modify-Write cycles are supported.
- Two memory areas with high speed static CMOS RAMs
  Write Access Time 55 ns (max), 50 nsec (typ)
  Read Access Time 55 ns (max), 50 nsec (typ
- On-board battery back-up provides date retention for up to one year

1. Functional Description

The fully latched address and data bus provide interleaved Read and Write operation to minimize bus overhead and to support a maximum transfer rate on the VMEbus of 9M transfer/sec. This results in a 36 Mbyte data throughput using 32-bit data. Installation in 16- or 32-bit environments is provided through the address modifier decoding (A24 or A32 mode) which defines the address range to be decoded. Automatic data bus sizing and adaptation to 16- or 32-bit environments are provided through on-board hardware logic.

1.1 The VMEbus Interface

A full VMEbus IEEE 1014 (Rev. C) compatible interface which supports the unaligned transfers is installed on the SRAM-6 board. 32-bit of data and address are supported to take full advantage of 16- and 32-bit processor boards and DMA Controllers. The following table lists the supported data transfer modes:

Transfer Type	D31–24	D23–16	D15–8	D7–0
Byte Byte			 x	x
Word Word (unaligned)		 x	x x	x
3 Byte (unaligned)	 x	x x	x x	x
Long Word	x	x	x	x

The addressing and data transfer modes supported on the SRAM-6 boards are:

A24 : D32, D16, D8, UAT, RMW, ADO
A32 : D32,D16, D8, UAT, RMW, ADO

Installation in 16- and 32-bit environments is possible using the address modifier selection. Each of the two fully independent memory areas, which consist of half of the memory size, contain their own decoding logic. This allows the separation and assignment of different data/program segments. A RUN/LOCAL switch to enable or disable accesses from the VMEbus is installed on each of the SRAM-6 boards. For multiprocessor synchronization, all defined Read-Modify-Write cycles are supported. The maximum data throughput of the SRAM-6 board is 36 Mbyte/sec. VMEbus worst case access times:

Write	55 nsec
Read	55 nsec

1.2 Address Decoding

A unique address decoding logic which provides a jumper-selectable access address is installed on the SRAM-6 board. The address lines A31 to A24 of the VMEbus are only decoded if the extended address modifier code is selected; otherwise, only the address signals up to A23 of the VMEbus are used in order to detect whether or not the board is adressed. The independent memory areas can be placed anywhere in the 4 Gbyte address range in 2 Mbyte steps. This allows the adaption of the SRAM-6 board to various applications without mirroring memory and losing capacity.

1.3 Battery Back-up

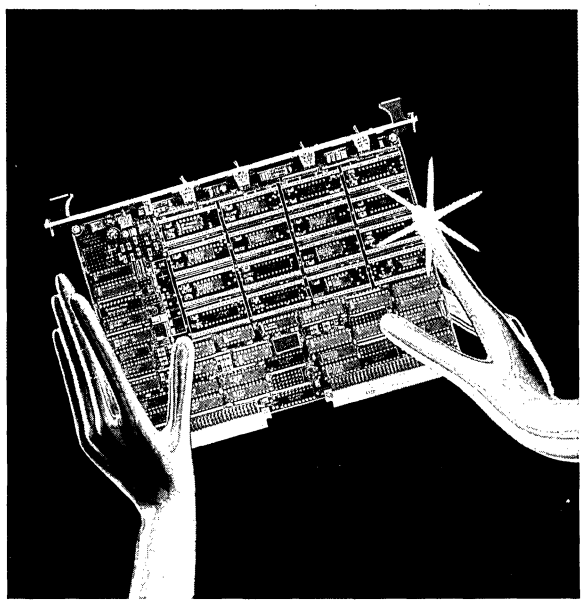
The SRAM-6 board includes power fail detection circuitry and two lithium batteries to guarantee data retention of the static RAMs for up to one year (calculated). Data retention is also supported via the + 5 V STDBY line. The board automatically detects when the + 5 V supply voltage drops below 4.65 V and does not respond to the VMEbus. In this case all the chip enable and select signals are driven inactive and the power-down mode is activated.

Specifications

Function	
Memory capacity	2 Mbyte
VMEbus interface A32 : D32, D16, D8, UAT, RMW, ADO A24 : D32, D16, D8, UAT, RMW, ADO	 yes yes
Maximum access times Write Read	55 nsec 55 nsec
Data retention times (all times are calculated)	6000 h (typical)
Special hardware functions On-board voltage sensor supporting the battery back-up of the SRAMs RUN/LOCAL switch Status and access control LEDs on the front panel	 yes yes
Power requirements + 5 V	3.5 A (typ) 6 A (max)
Operating temperature with forced air cooling Storage temperature Relative humidity (non condensing)	0 to + 50 °C – 50 to + 85 °C 5 to 90 %
Dimensions	234 × 160 mm : 9.2 × 6.3 in.

Ordering Information

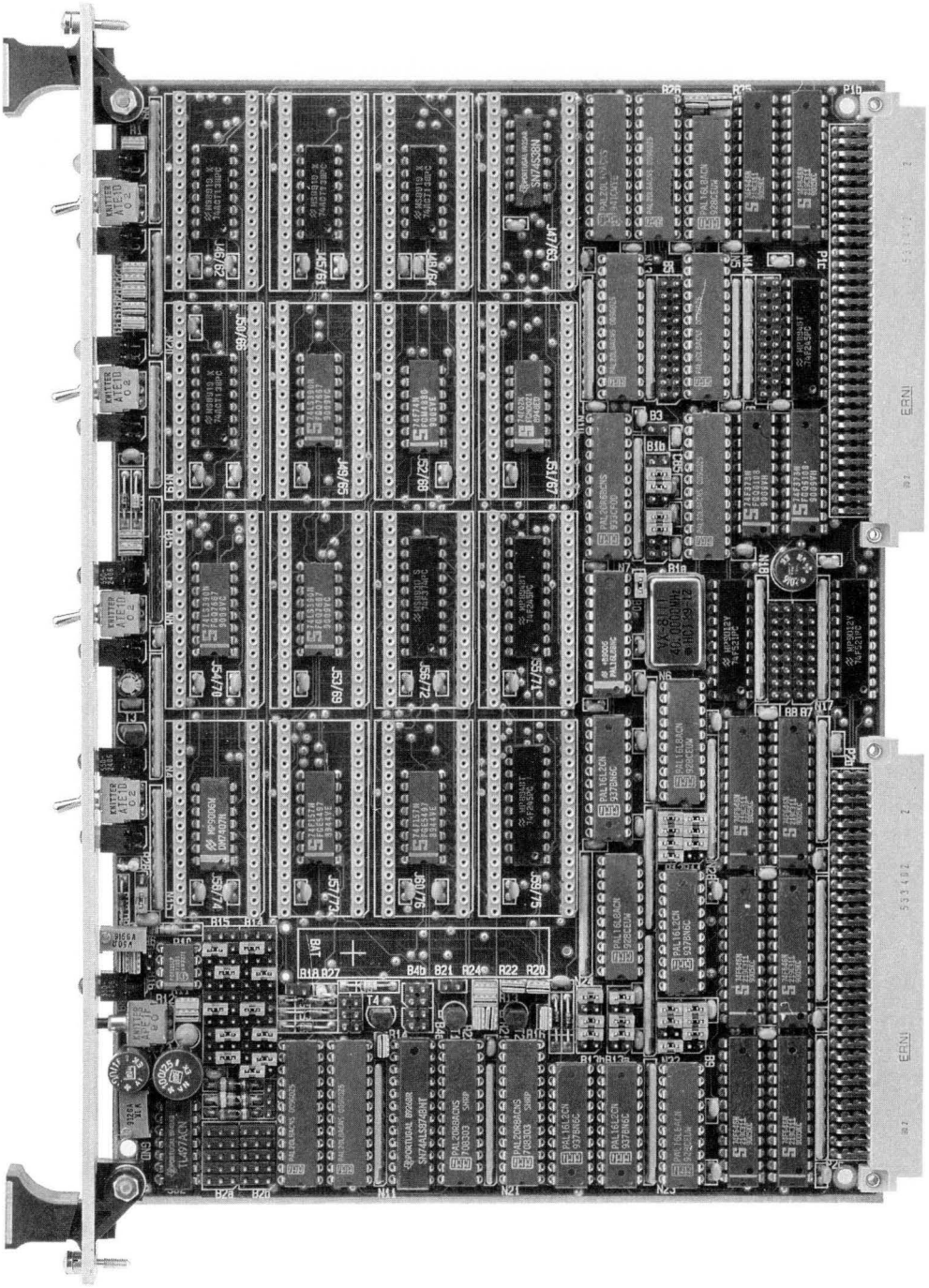
SYS68K/SRAM-6 Part No. 200506	2 Mbyte static RAM board with VMEbus interface. Documentation included.
SYS68K/SRAM-6UM Part No. 800137	User's Manual for all SYS68K/SRAM-6 board versions.



System 68000 VME

SYS68K/RR-2

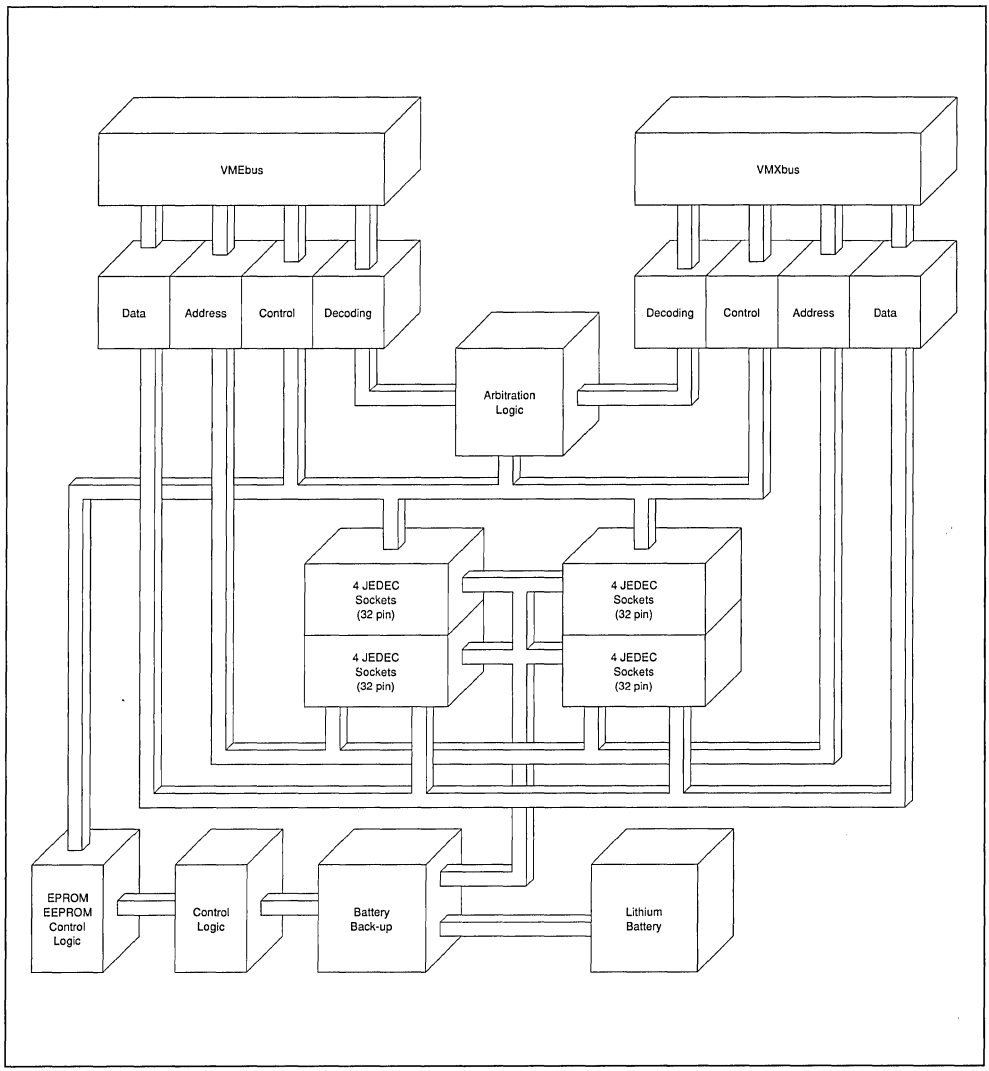
32-Bit RAM/ROM Board with VMEbus and VMXbus Interface



General Description

The SYS68K/RR-2 board is a high speed 32-bit memory board using up to 16 JEDEC-compatible devices. The VMEbus interface is capable of transferring 8-, 16-, 24- and 32-bit of data.
In addition to the 32-bit VMEbus interface, a full 32-bit VMXbus interface is installed on the RR-2. It supports unaligned transfers from the VMEbus as well as from the VMXbus. Read-Modify-Write cycles for multi-processor synchronisation are also supported. The VMEbus and the VMXbus interface can separately be enabled or disabled via two switches installed on the front panel.
A dual port control logic is installed on the RR-2 to control the accesses of the two independent asynchronous buses.

Block Diagram of the SYS68K/RR-2



Features of the SYS68K/RR-2

- VMEbus interface supporting 32 data and 32 address lines
- Jumper-selectable access address and address modifier code
- 16 sockets for JEDEC-compatible devices using the 28- or 32-pin standard
- VMXbus interface (Rev. B) supporting 32 data and 32 address lines
- Arbitration mechanism between VMXbus and VMEbus accesses supporting Read, Write and Read-Modify-Write cycles
- Two independent memory areas each consisting of 8 devices
- Battery back-up for static RAMs
- Programming of EPROMs and chip erase function switch
- Programming of EPROMs (21 V and 12 V types)
- Write protection switch for each of the two memory areas
- RUN/LOCAL switch for the VMEbus and VMXbus interface
- Jumper-selectable access address and address modifier code for each of the two memory areas.
- Status and Access indication LEDs

1. Functional Description

The two different memory areas, each consisting of 8 sockets, are accessible via the VMEbus or VMXbus interface and provide global memory such as static RAM, EPROM or EEPROM.

The two bus interfaces allow the use of the RR-2 board as a global Dual Ported Memory accessible through the VMXbus interface for the host CPU and accessible through the VMEbus interface from other CPU-boards for multi-processing or from an intelligent controller board featuring DMA.

The Read-Modify-Write cycles from both bus interfaces are supported to provide multi-processor synchronisation as well as shared memory resources.

Both the 28-pin and the 32-pin standard for SRAMs, EPROMs and EEPROMs are supported to offer a maximum EPROM capacity of 2 Mbyte if 128 K × 8 devices are used. Two different memory areas, each consisting of 8 sockets, are installed on the board to allow mixing of device types (i.e. one SRAM and one EPROM area).

Each memory area has a jumper-selectable access address in device dependent boundaries and a set of selectable address modifier codes. The access speed for each memory area is jumper-selectable to adapt the access times of the used devices. A battery back-up with a voltage sensor is installed on the RR-2 to allow data retention for SRAM devices for up to one year.

A Write Protect switch for each memory area installed on the front panel allows the protection of the memory area against non-privileged modification.

EPROMs and EEPROMs can be programmed via special on-board hardware logic which makes a PROM programmer obsolete for most of the ROMable software development packages. The EPROM programming feature of the RR-2 is supported under the real time multi user miltitasking operating system PDOS.

1.1 The VMEbus Interface

The RR-2 contains a full 32-bit VMEbus providing highest data throughput. A RUN/LOCAL switch can disable the VMEbus interface to allow use of the board as a VMXbus board.

On Write cycles, the 32-bit data and address are latched and a DTACK* will be generated immediately if this operation is completed, and if the Write protection is not activated for the addressed memory area.

The internal Write cycle starts in parallel and will be executed depending on the selected access time of the used devices.

The access times on Read and Write cycles depend on the load from the VMXbus interface as well as on Read cycles on the access time of the installed devices.

Write: 80 nsec
Read: 210 nsec (using 100 nsec SRAMs)
310 nsec (using 200 nsec EPROMs)

All listed times are the maximum response times measured without accessing the RR-2 board from the VMXbus interface.

The access address of the two independent memory areas is jumper-selectable in device dependent steps.

The unaligned transfers, defined in the VMEbus specification, are fully supported to take advantage of the 68020/030 data bus handling.

Data transfer modes:
A24 : D32, D16, D8, UAT, RMW, ADO
A32 : D32, D16, D8, UAT, RMW, ADO

The maximum data transfer speed over the VMEbus without concurring accesses via the VMXbus is 16 Mbyte/sec using 100 nsec SRAM devices.

1.2 The VMXbus Interface

A 32-bit VMXbus interface is installed on the RR-2 to offer a dual port function together with the VMEbus. The access address for the two memory areas is identical to the decoding of the lower address lines of the VMEbus (A24 Mode). A RUN/LOCAL switch for the two memory banks is used to disable accesses to the board from the VMXbus side if only VMEbus transfers need to be supported.
The following data transfer modes are supported:
A24 : D32, D16, D8, UAT, RMW, ADO

The unaligned and the Read-Modify-Write cycles are supported on the VMEbus and VMXbus for multi-processor synchronization.
The Read and Write access times of the VMXbus interface depend on the load from the VMEbus interface (number of initiated transfers) and on the access times of the installed devices. The time values listed below are measured without any load from the VMEbus.

Write: 80 nsec (independent of the device acess time)
Read: 190 nsec (using 100 nsec SRAM and no VME access)

Times are measured between a driven data strobe and a driven DTACK* on the VMXbus. The early DTACK* option of the VMXbus is not used for measurement.

1.3 Access Address Selection

Each of the two memory areas provides an individual selectable access address which is device capacity dependent. The address modifier code can also be selected for each memory area.
The access address which is compared depends on the selected address modifier code. The hardware logic of the RR-2 automatically detects if A24 or A32 decoding is selected (extended or standard addressing).
Each of the 8 defined address modifier-codes can be separately enabled or disabled via jumper settings.
The VMXbus access address decoding is identical to the A24 address set-up of the VMEbus interface to guarantee linear addressing.

1.4 Use of EPROM Devices

The RR-2 is designed to support 28- and 32-pin JEDEC-compatible devices.
16 sockets each consisting of 32 pins are installed on the RR-2 to support the following device types:

Device	Organization	No. of Pins Used	Total Capacity
2764	8 K × 8	28	128 Kbyte
27128	16 K × 8	28	256 Kbyte
27256	32 K × 8	28	512 Kbyte
27512	64 K × 8	28	1 Mbyte
2710xx	128 K × 8	32	2 Mbyte
2720xx	256 K × 8	32	4 Mbyte
TBD	512 K × 8	32	8 Mbyte
TBD	1 M × 8	32	16 Mbyte

Each memory area can be equipped with different device types allowing the insertion of SRAMs, EPROMs and EEPROMs at the user's discretion. A Write Protect switch on the front panel protects the board from being written to.

1.5 Use of EEPROM Devices

The RR-2 accepts EEPROM devices from 64 Kbit capacity (8 K × 8 organization). Logic to program EEPROMs is installed on the board to allow the modification of parameters during runtime without exchanging the devices.
A chip erase switch is installed on the board to erase up to 4 chips at a time (depending on the initiated data transfer which enables the chip erase function for the selected devices). A Write

protect switch allows each memory bank to be protected against overwriting.
The following table lists all supported devices and the total capacity if all sockets are fitted with identical devices.

Device Type	Organi-zation	No. of Pins Used	Total Capacity
58064, 2864, 5233	8 K × 8	28	128 Kbyte
TBD	32 K × 8	28	512 Kbyte
TBD	64 K × 8	32	1 Mbyte
TBD	128 K × 8	32	2 Mbyte
TBD	256 K × 8	32	4 Mbyte
TBD	512 K × 8	32	8 Mbyte

1.6 Use of SRAM Devices

The RR-2 contains 16 sockets which may be used for static RAM insertion. The standard pin assignments for 8 K × 8 and 32 K × 8 devices are supported, resulting in a capacity of 128 or 512 Kbyte.
Expansion of the memory capacity is provided by using 32-pin devices.

The following table lists the supported devices and the future extension:

Device Type	Organi-zation	No. of Pins Used	Total Capacity
6264	5 K × 8	28	128 Kbyte
62256	32 K × 8	28	512 Kbyte
TBD	128 K × 8	32	2 Mbyte
TBD	512 K × 8	32	8 Mbyte

An on-board lithium battery and a voltage sensor provide battery back-up of "low power" specified SRAMs (CMOS) of up to one year (SRAM dependent). The on-board logic can be adjusted to the access time of the SRAMs to support various devices and optimize data throughput to the VMEbus and VMXbus interface.

Specifications

Function		
Memory capacity (max).	EPROM EEPROM SRAM	16 Mbyte 8 Mbyte 8 Mbyte
Memory devices supported	EPROM EEPROM SRAM	28-pin or 32-pin JEDEC 28-pin or 32-pin JEDEC 28-pin or 32-pin JEDEC
Memory banks (independent) Independent address decoding, VMEbus and VMXbus		2 yes
VMEbus interface A32 : D32, D16, D8, UAT, RMW, ADO A24 : D32, D16, D8, UAT, RMW, ADO Independent Run/Local, write protect switches		 yes yes yes
VMX interface (Rev. B) A24 : D32, D16, D8, UAT, RMW Independent Run/Local, write protect switches		 yes yes
Access times, reconfigurable in 25 nsec steps from min. access time max. access time		yes 75 nsec 475 nsec
EPROM programming voltages EEPROM programming voltages EEPROM chip erase		+ 12 V, + 21 V yes, (+ 5 V devices) yes
Power requirements (unpopulated)	+ 5 V + 12 V	3.4 A 0.2 A
Operating temperature with forced air cooling Storage temperature, non-operating Relative humidity (non-condensing)		0 to + 50 °C – 50 to + 85 °C 5 to 90 %
Board dimensions		234 × 160 mm : 9.2 × 6.3 in

Ordering Information

SYS68K/RR-2 Part No. 200200	32-Bit RAM/ROM board with VMEbus and VMXbus interface. Documentation included.
SYS68K/RR-2/UM Part No. 800103	User's manual for the SYS68K/RR-2.

Controller Boards

FORCE COMPUTERS

Controller Board Introduction

FORCE COMPUTERS' range of VMEbus based boards includes a comprehensive selection of boards designed to match system requirements for mass (magnetic media) memory control, graphics and system control.

Mass memory

The SYS68K/ISCSI-1 features an intelligent interface to the high speed SCSI bus. Intelligence is provided via the on-board 68010 (10 MHz) CPU and the installed firmware provides an effective user interface and supports hashing and cashing algorithms to increase performance. Data rates of up to 1.5 Mbyte per second are supported across the SCSI bus under the control of the on-board DMA controller. Maximum performance is guaranteed from the 68010 due to zero wait state access to the on-board dual ported 128 Kbyte SRAM.

Graphics

If you need high level graphic solutions offered by the 63484 ACRTC, the SYS68K/AGC-2 will fit your specification. The board offers 1 Mbyte of video memory and the 63484 offering 4-bit/pixel graphical display at up to 1160 × 876 resolution. The AGC-2 is the low cost graphics solution.
The AGC-3 offers even higher performance due to cascading QPDMs (Quad Pixel Dataflow Managers). The AGC-3 offers display resolutions of up to 1280 × 1024, 8 bit per pixel, non-interlaced. Two serial channels are also provided for connection of a keyboard or mouse.

System controllers

If your application requires multi-level bus arbitration, additional I/O and specialist multiprocessing features, then the SYS68K/ASCU-2 system controller board may fit your specification. The board supports the full IEEE 1014 Standard 4 level bus arbitration options, Centronics printer interface, serial I/O interface and a Real Time Clock. Additionally, the ASCU-2 also supports an IEEE-488 (GPIB) interface and the facility to trigger H/W interrupts on the VMEbus from software. This added feature makes the ASCU-2 the ideal choice for multiprocessing applications.

Mass Memory Controllers

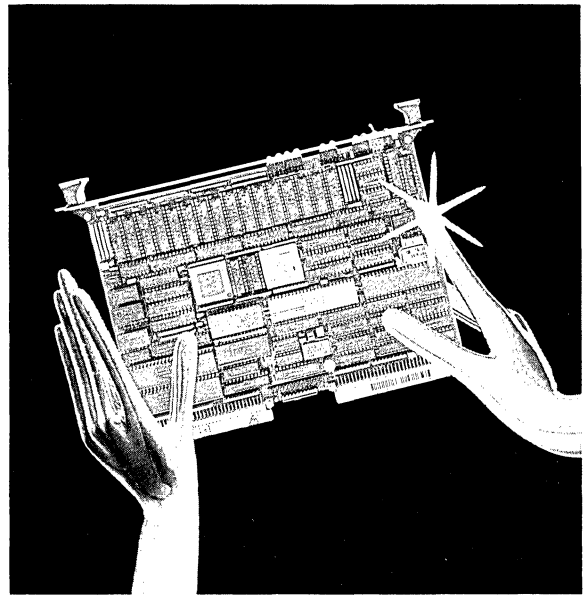
FAMILY	ISCSI-1
Mass memory interface	SCSI/SA460
Maximum disk data transfer rate Synchronous Asynchronous	SCSI – 1.5 Mbyte/sec
VMEbus interface	16 bit
Dual-ported RAM Capacity	yes 128 Kbyte
Local processor Frequency	68010 10 MHz
No. of supported disks	7 (SCSI) 4 × Floppy
Driver/receiver circuits on board	yes
No. of different interrupts to VMEbus	4

Graphics Controllers

FAMILY	AGC-3	AGC-2
Used controller chip	95C60 (QPDM)	63484 (ACRTC)
Used color lookup chip (CLUT)	Bt459 (RAMDAC)	IMS G170
Pixel frequency	30/75/125 MHz	16/32 MHz
Pixel depth	4 or 8 Bit	4 Bit
Resolution examples 50 Hz non-interlaced (32 MHz) 60 Hz non-interlaced (32 MHz) 60 Hz interlaced (32 MHz) 70 Hz non-interlaced (125 MHz) 70 Hz non-interlaced (75 MHz) 70 Hz non-interlaced (30 MHz)	 – – – 1280 × 1024 1024 × 768 640 × 480	 800 × 600 720 × 560 1024 × 800 – – –
No. of different simultaneously displayable colors Total no. of colors	16 or 256 16777216	16 262144
Video RAM capacity min. max.	2 Mbyte 4 Mbyte	1 Mbyte 1 Mbyte
Video outputs	R,G,B H-Sync V/COMP-Sync	R,G,B COMP-Sync
Interfaces Light pen Serial I/O	no 2	yes 0
Cursor features	Hardware (CLUT) Cross-Hair	Hardware (AGC-2)
Character generator	yes (QPDM)	–
VMEbus interface type Address decoding Data transfer size Unaligned transfers Read Modify Write cycles	Slave A24, A16 D8, D16, D32 yes yes	Slave A24, A16 D8, D16 yes yes
Secondary bus interface type Data transfer size	VSB-Slave D8, D16, D32	–

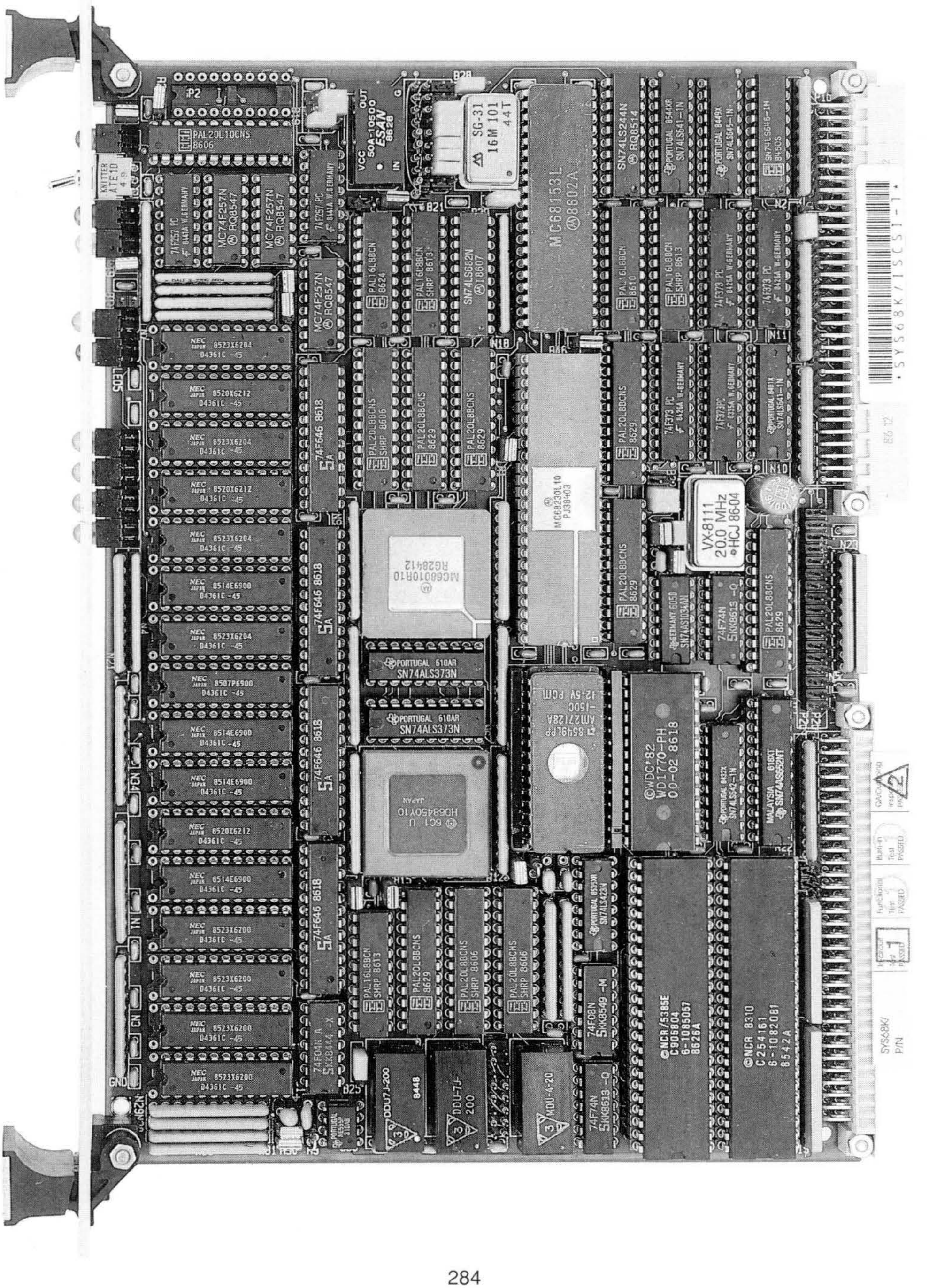
Systems Controllers

FAMILY	ASCU-2
Bus arbiter	4-level Round Robin 4-level prioritized 4-level prioritized Round Robin
SYSCLK driver SYSRESET* switch and generator Power monitor VMEbus time-out generator VMEbus arbitration time-out generator	yes yes yes yes yes
Interrupt generator to VMEbus No. of channels Total no. of different interrupts to VMEbus	yes 8 16
Serial I/O interface (RS232/RS422) Parallel I/O interface Real Time Clock with battery back-up IEEE 488 (GPIB/HPIB) interface Timer	1 Centronics yes yes 2 × 24 bit



System 68000 VME
SYS68K/ISCSI-1

Intelligent Mass Memory Controller Board

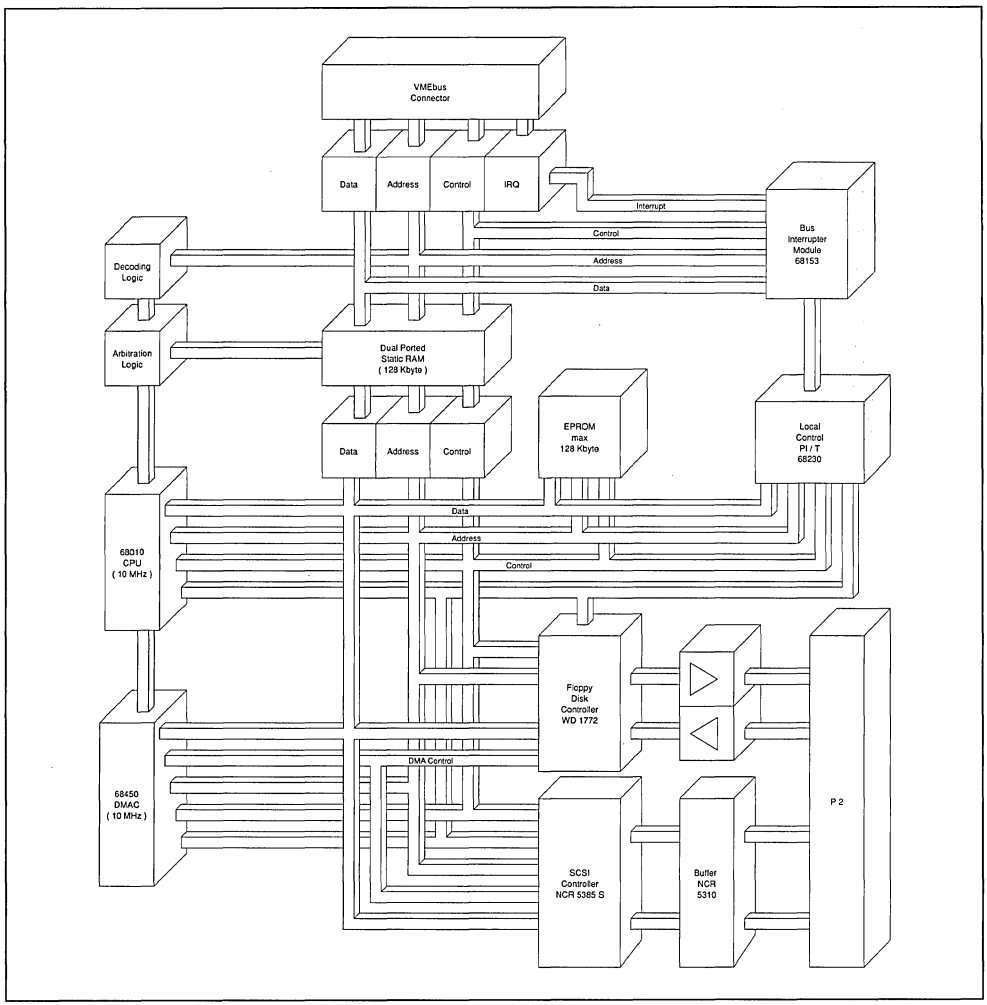

SYS68K/ISCSI-1
MC68153L
SN74ALS373N
VX-8111
20.0 MHz
LED5
GND

General Description

The SYS68K/ISCSI-1 is a high-performance intelligent mass memory controller board with a 68010 CPU and a high-speed DMA Controller. The DMA Controller is coupled with the SCSI controller and the on-board floppy disk controller. 128 Kbyte of Dual Ported RAM on the ISCSI-1 are used to store commands and data. Highest throughput in the 68010 CPU and 68450 DMA Controller is provided by the arbitration mechanism of the Dual Ported RAM. The DMA Controller and the CPU access the DPR constantly without any wait states, independent from all VMEbus accesses.

The initiator and the target mode are supported on the ISCSI-1 board to offer a wide variety of applications. All the driver and receiver circuitries are installed on the board to provide direct P2 interfacing and easy installation into VMEbus environments. The on-board floppy disk controller (WD 1772) allows the connection of up to four 3", 3½" and 5¼" drives.

Block Diagram of the SYS68K/ISCSI-1



Features of the SYS68K/ISCSI-1

- 68010 CPU for local control (10 MHz)
- 68450 DMA Controller (10 MHz) connected to the SCSI controller and the floppy disk controller
- Dual Ported 128 Kbyte zero wait state static RAM between the VMEbus and the local CPU/DMA Controller (ISCSI-1)
- SCSI interface built with the NCR 5386S SCSI controller programmable as initiator or target
- SA460 compatible floppy interface with a WD 1772 floppy disk controller for connection of up to 4 floppy disk drives
- All SCSI interface and floppy disk interface signals are available on the P2 connector
- Four different interrupt request channels to the VMEbus. Each channel contains a software-programmable IRQ-level (1–7) and vector
- Local parallel interface for controlling and monitoring board functions
- VMEbus IEEE 1014-compatible slave interface (A24 : D16, D8)
- Watchdog timer controlling correct functions of on-board hardware and software
- Status and control LEDs for monitoring local activities
- High-level handling firmware for communication, self-test, data cashing/hashing and control

1. The Hardware Functions

The local CPU reacts on the commands and initialization parameters within the Dual Ported RAM. Constant run times are guaranteed through the special hardware logic, providing zero wait state operation from the Dual Ported RAM, independent from the accesses from the VMEbus to the Dual Ported RAM.

The ISCSI-1 consists of self-test functions as well as of a hardware watchdog timer which controls the activities of the 68010 CPU and the 68450 DMA Controller running with 10 MHz clock frequency.

User-supplied programs can be loaded into the Dual Ported RAM and executed from the local CPU to adapt and extend board functionality. The local CPU controls the DMA Controller, SCSI bus controller and the floppy disk controller via local interrupts and communicates to the host CPU via the DPR and/or via interrupt requests to the VMEbus generated by a Bus Interrupter Module.

All I/O signals of the SCSI controller and the floppy disk controller are buffered and are available at the P2 connector of the board.

1.1 The Local 68010 CPU

A 10 MHz 68010 CPU is installed on the ISCSI-1 to control the data traffic between the SCSI controller, floppy disk controller and the VMEbus for the host CPU(s). Two EPROMs with a maximum capacity of 128 Kbyte are installed on the ISCSI-1 to contain the handling firmware. Constant zero wait state operation from the EPROM guarantees maximum CPU throughput and a fixed program runtime. The 128 Kbyte of Dual Ported RAM is also accessible without the insertion of wait states by using a CPU clock synchronized arbitration mechanism. The accesses from the CPU to the DPR are not delayed if a VMEbus access is pending or being executed.

A local timer included in the PI/T is used to interrupt the CPU for task scheduling, command interpretation and execution.

The CPU and all I/O devices can be reset through a system reset via the SYSRESET* signal of the VMEbus, or by accessing a dedicated location within the DPR reserved for this function.

1.2 The 68450 DMAC

The ISCSI-1 contains a 4 channel DMA Controller (68450) with a clock frequency of 10 MHz. The DMA Controller is connected to the floppy disk controller and the SCSI controller to offer maximum data throughput to/from the mass memory devices.

The DMA Controller accesses the Dual Ported RAM constantly without the insertion of wait states. The DMA Controller transfers data from the device directly to the memory in a single cycle mode.

Special hardware logic on the board collects 2×8 bit of date and forces one 16-bit transfer to the Dual Ported RAM to enhance and optimize data throughput.

The minimum guaranteed data transfer rate, including handshaking on the SCSI is 1.25 Mbyte/sec if an appropriate SCSI data transfer rate of the mass memory device is provided.

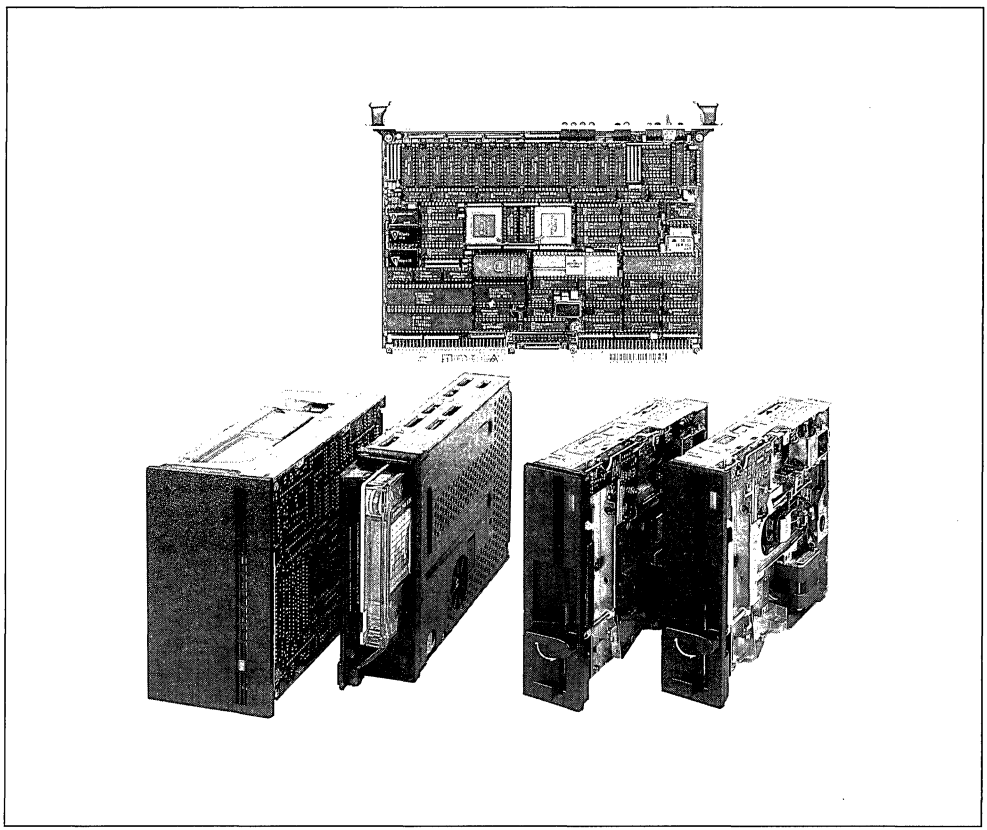
1.3 The SCSI Controller

The SYS68K/ISCSI-1 contains an NCR 5386S SCSI controller chip and an NCR 5310 SCSI driver/transceiver. The 5386S controller is directly connected to the on-board DMA Controller to transport the incoming/outgoing data via the DMA Controller to/from the Dual Ported RAM.
The initiator and the target mode of the SCSI specification are fully supported with the controller and the on-board firmware. Parity generation and check are automatically handled inside the controller to guarantee maximum data integrity.
The installation of the 5310 SCSI driver/receiver circuitry allows easy adaption and installation in a VMEbus rack because all I/O signals are available on the P2 connector and fully buffered with 48 mA drivers (single-ended version).

1.4 The Floppy Disk Controller

The ISCSI-1 board contains a WD 1772 floppy disk controller to directly control 3", 3½" and 5¼" floppy disk drives. All the driver and receiver circuitries are installed on the board and the I/O signals are available on the P2 connector for easy interfacing.
The floppy disk controller data bus is directly connected to the DMA Controller allowing highest throughput from the floppy disk to the Dual Ported Memory. The single chip floppy disk controller includes all the phase locked loop and data separation without the need for adjustments and adaptions.
The floppy disk controller WD 1772 is able to control single and double density floppy disk drives (single or double sided). The selection of each mode is made via the local PI/T.

Picture of ISCSI-1 with Mass Memory Devices



1.5 The PI/T 68230

A 68230 Parallel Interface and Timer chip is installed on the SYS68K/ISCSI-1 to control and display the status of all on-board activities. The PI/T is also used to force and monitor the interrupt request lines to the Bus Interrupter Module which initiates the interrupts to the VMEbus under control of the host CPU.
One handshake pin is used to interrupt the local CPU if the host CPU accesses a defined location within the DPR. One output signal is used to force a SYSFAIL* signal to the VMEbus if an on-board failure has been detected or if the board initializes the DPR after RESET or power-up. The timer also included in the PI/T is the time base for the on-board handling firmware and the scheduler for handling the macro commands.
A watchdog timer for processor control is installed on the board to detect software or hardware errors independent from the on-board CPU. The SCSI bus RESET signal is controlled from the local PI/T. One input of the PI/T indicates the state of the SCSI bus RESET and one output can be used to force an SCSI bus reset.

1.6 The Dual Ported RAM

128 Kbyte of Dual Ported static RAM is installed on the SYS68K/ISCSI-1. The DPR is used to service all applications requiring fast operations and large amounts of data areas. The local 68010 CPU runs without the insertion of wait states from the DPR because the CPU clock synchronized arbitration logic and a fully buffered and latched VMEbus interface is installed on the ISCSI-1.
Between two CPU access cycles, a VMEbus cycle is serviced and completed. On VMEbus Read cycles, the data pattern is latched and the internal cycle of the DPR is terminated while the VMEbus cycle is decoupled.
A partition of the DPR is reserved for the local CPU for vector storage, the program counter and temporary buffers. This partition is used from the VMEbus side for programming the BIM and initiating an interrupt which will be handled from the on-board CPU or by driving a local RESET.
The local DMA Controller, which is connected to the SCSI bus controller and the floppy disk controller, also runs without the insertion of wait states by accessing the Dual Ported RAM. The access address and the Address Modifier codes are jumper-selectable within the standard address range (A24 : D16, D8). The access times of the DPR depends on the accesses made by the local CPU as the local 68010 has priority over VMEbus accesses.

1.7 The VMEbus Interface

A fully VMEbus IEEE 1014-compatible interface is installed on the SYS68K/ISCSI-1 to allow an access to the DPR and the Bus Interrupter Module. The 16-bit data width (D16, D8) of the DPR and the decoding of the standard address range (A24) allow easy installation in all VMEbus environments. During power-up and after RESET has been executed from the local CPU, the ISCSI-1 drives the VMEbus signal SYSFAIL* active to signal each board in the VMEbus environment that the board is not ready or has detected a malfunction.
A RESET as well as an interrupt for the local CPU can be initiated by accessing another location within the DPR, signalling the on-board processor that a command has been given, or that an exception has to be taken.
The Dual Ported RAM can be accessed at least every 640 nsec because this is the worst case cycle time. The data transfer rate to/from the ISCSI-1 is 3 to 4 Mbyte/sec including the VMEbus protocol.

	Access Time	Cycle Time
Best Case	330	400
Average	430	500
Worst Case	560	630

1.8 The Bus Interrupter Module

To allow fully asynchronous operation, the ISCSI contains a Bus Interrupter Module (BIM 68153) providing four individually programmable interrupt channels. Each channel is able to force an interrupt request to the VMEbus. For each channel, the IRQ-level (1 to 7) as well as the interrupt vector is fully software-programmable.
The local CPU forces the interrupt requests to the BIM and the host CPU can program the interrupt vector and the level. This allows dynamic change of the interrupt level and vector in multi-processor environments.

1.9 The Optional Backpanel

A backpanel which can be plugged into the P2 connector of the ISCSI-1 board is optionally available. Included on this board is a 50-pin 2-row conncector for the SCSI and a 34-pin 2-row connector for the floppy disk for direct connection of a flat cable.

2. The Firmware

The SYS68K/ISCSI-1 intelligent SCSI controller board operates under the control of the local handling firmware which is supplied – as standard – with the board free of charge. This EPROM resident firmware package executes the commands which are placed in the Dual Ported RAM and returns control and error messages.
The host interface consisting of a command block, buffers for I/O and command chaining exists twice for easy implementation into a multiprocessor system.

The handling firmware is divided into different modules which are:
- I/O initialization and self-test routines
- SCSI initiator and target mode control
- Command chaining routines
- Block buffering and hashing structures
- Handling for up to four floppy disk drives
- Command execution routines

Each of the two command blocks are used to pass commands and parameters to the firmware. When the command is executed, an interrupt can be generated. The return values, containing complete codes and parameters are placed in the command block.

2.1 Features of the Firmware

- Multi-processor support
- Sector size translation
- Support for up to five logical units
- Support for down-loadable user programs

2.2 SCSI Support

- Full support for SCSI Common Command Set
- Optional SCSI commands may be installed for up to seven devices
- Emulation of the SCSI commands COPY, COMPARE and SEARCH
- BACKUP command
- Support of the RESERVE/RELEASE commands, and of the DISCONNECT/RESELECT operation
- Automatic handling of REQUEST SENSE
- Transparent mode to the SCSI interface for unique vendor specific commands or software debugging

2.3 Floppy Disk Support

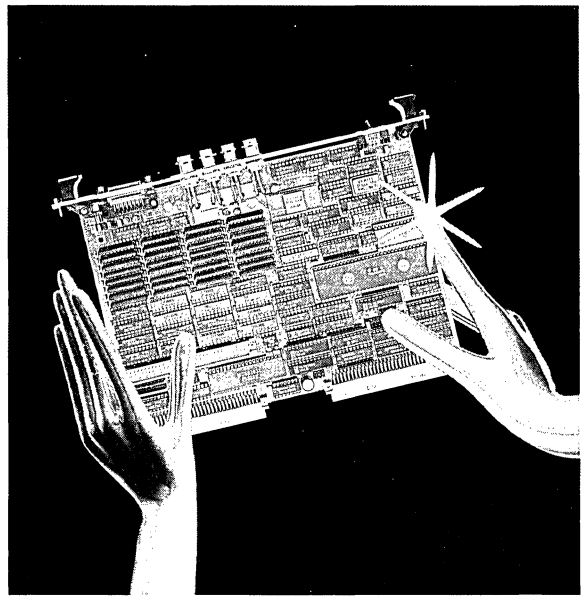
- Supporting FORMAT, FORMAT TRACK, COMPARE, COPY and BACKUP commands
- Disk parameters and format interleaves are fully installable and changeable

Specifications

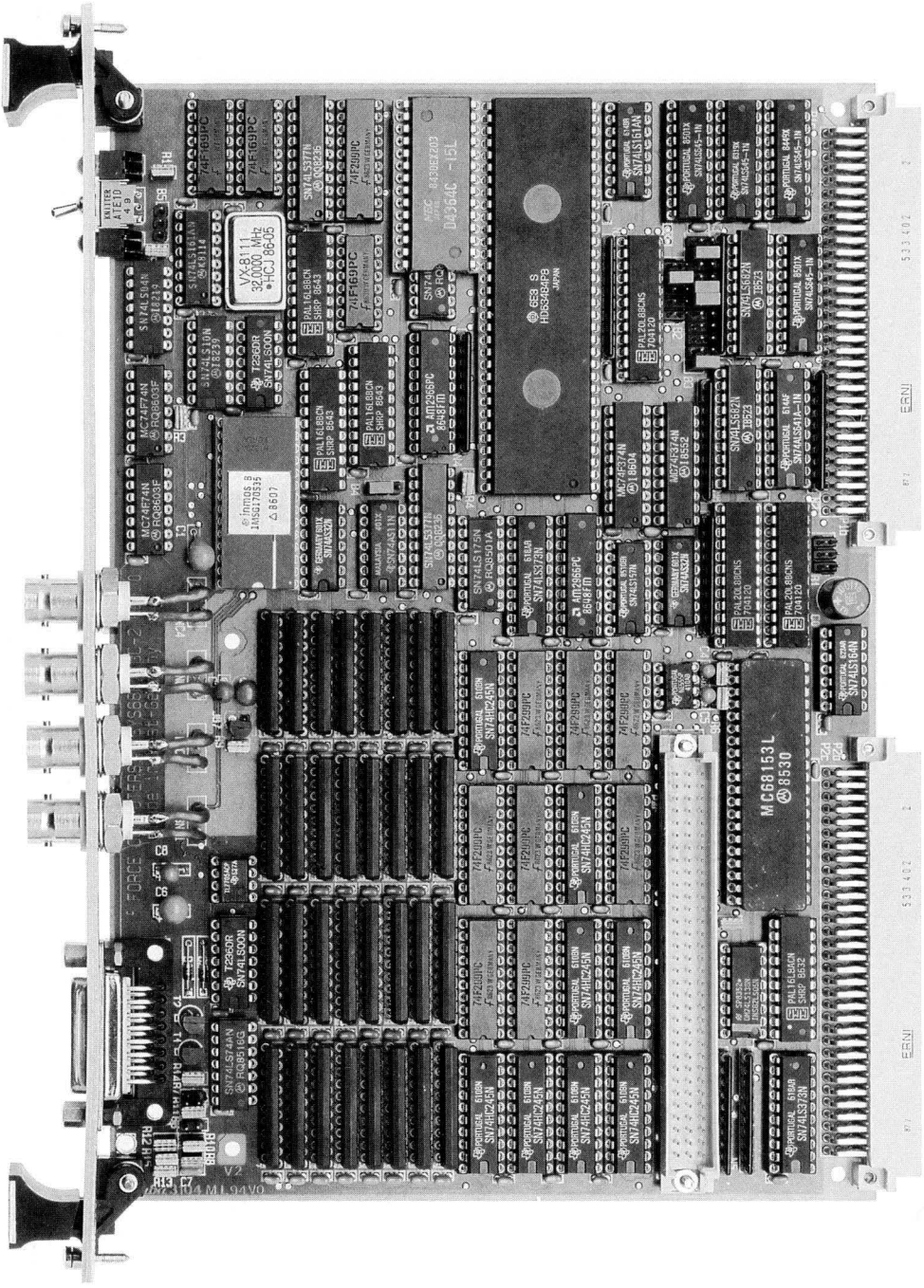
Function	
68010 CPU clock frequency 68450 DMA controller clock frequency	10 MHz 10 MHz
Dual Ported PAM (0 wait state) VMEbus access time (typ)	128 Kbyte 430 nsec
EPROM capacity (max)	128 Kbyte
SCSI controller SCSI signals routed to	NCR 5310 P2
Floppy disk controller Floppy interface	WD 1772 SA460
VMEbus slave interface A24 : D8, D16	yes
Firmware installed on all board versions	yes
Power requirements + 5 V (max)	5.6 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)	0 to + 50 °C – 40 to + 85 °C 5 to 95 %
Board dimensions	234 × 160 mm : 9.3 × 6.3 in
No. of slots used	1

Ordering Information

SYS68K/ISCSI-1 Part No. 300020	Intelligent SCSI/Floppy Disk Controller, 128 Kbyte Dual Ported RAM, with local DMA controller, including firmware and documentation.
SYS68K/IOBP-1 Part No. 700043	Back panel for the ISCSI-1 board providing SCSI and floppy disk controller connectors.
SYS68K/ISCSI-1/UM Part No. 800114	User's manual for the ISCSI-1.
SYS68K/ISCSI-1SC Part No. 300022	Source code of the local handling firmware.



System 68000 VME
SYS68K/AGC-2
Advanced Color Graphics Controller Board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General Description

The SYS68K/AGC-2 is a high-performance graphics board which combines a powerful graphics processor, the 63484 ACRTC, with 1 Mbyte video RAM and a digital-to-analog convertor, the IMS G170, with a color look-up-table. The maximum resolution to be displayed at 50 Hz is 1160 × 870 pixel with 4 bit/pixel color information and interlaced display mode.

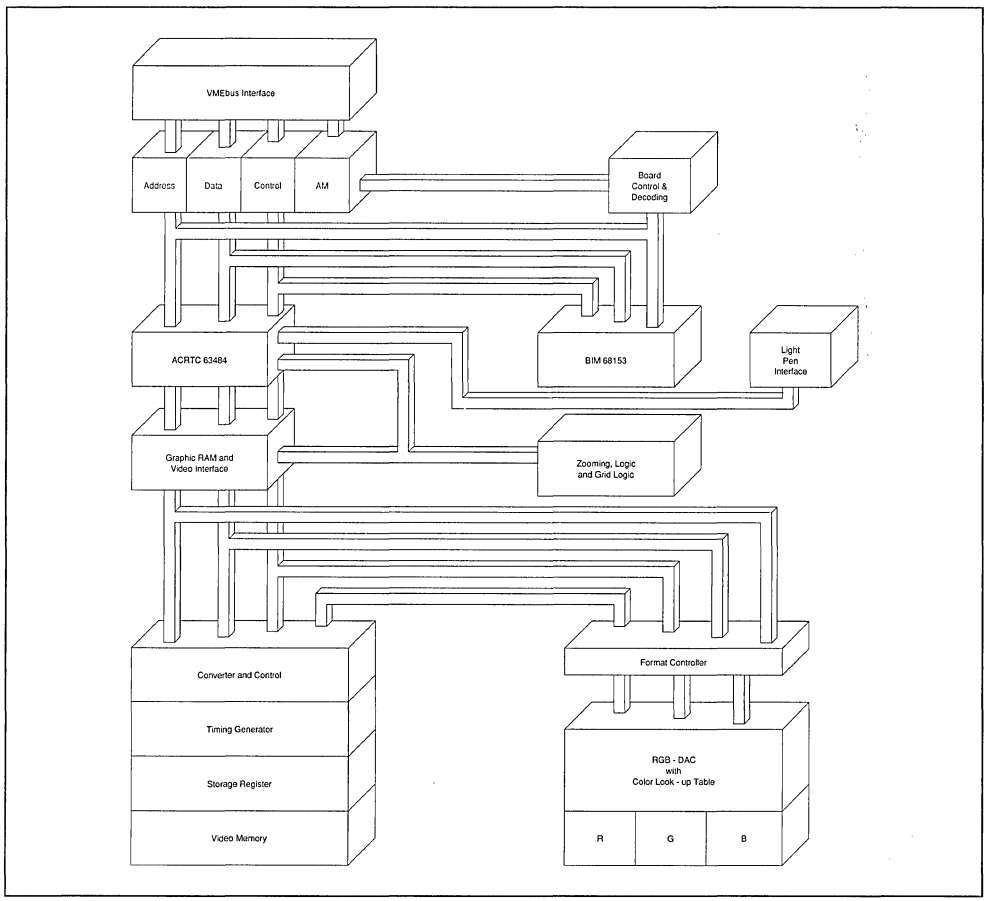
Flicker-free display in the non-interlaced mode is provided by using the 800 × 600 display format which provides 50 Hz frequency and 4 bit/pixel color information. The pixel frequency of the RGB output is 32 MHz, or 16 MHz to allow the connection of various monitors.

To provide maximum flexibility, 16 different colors, out of 262144, can be simultaneously displayed at the maximum format of 1160 × 870 pixels using the 50 Hz interlaced display mode. The 1 Mbyte video RAM is accessible via the ACRTC by using its powerful command set.

The local control, which consists of a Bus Interrupter Module (BIM), offers software control for programming the ACRTC and updating the frame buffer of the color look-up table during vertical retrace.

The AGC-2 also provides a standard light pen interface which is accessible on the front panel. The VMEbus interface is IEEE 1014-compatible.

Block Diagram of the SYS68K/AGC-2



Features of the SYS68K/AGC-2

- ACRTC 63484, 4 MHz
- 23 high level graphic commands
- 1 Mbyte video RAM
- Free programmable cursor independent from zoom and window limits
- Grid logic in combination with zooming
- RGB and composite SYNC output
- Three different screens with software-programmable positions
- One graphics color RGB-DAC with color look-up table providing 16 simultaneously displayable colors out of a palette of 262144 colors
- Light pen interface
- VMEbus/IEEE 1014 interface
  A24, A16 : D8, D16
- Interrupter to VMEbus with software-programmable IRQ-level and vector
- RUN/LOCAL switch to disable VMEbus accesses
- Full decoding of the address modifiers

1. Functional Description

The ACRTC 63484 receives the drawing commands from a CPU board through the VMEbus interface. All address calculations to the video RAM are made internally to deload the CPU-board programs by using only x- and y-co-ordinates.
The controller chip automatically generates the timing for the screen after initialization.
4 bits/pixel provide 16 colors to be displayed out of the complete range of 262144 colors.

1.1 The ACRTC 63484

The Advance CRT Controller 63484 provides 38 commands including 23 graphic drawing commands. A 16 byte on-chip Read/Write FIFO reduces communication overhead of the CPU board. Automatic conversion of the x-/y- co-ordinates to physical frame buffer addresses is provided through the on-chip drawing processor. All timing parameters for the used monitor are software-programmable, and the ACRTC generates all the necessary timings to the RGB and SYNC outputs. The Controller also allows the use of up to three different screens (upper, lower and base screen) plus one window screen. The size and the position, as well as the smooth scroll for each screen, is software-programmable.
The light pen interface of the ACRTC is supported via the 15-pin D-sub connector available on the front panel.

1.2 The Video RAM

1 Mbyte of video RAM is installed on the AGC-2 board. The video RAM enables the use of multiple pictures to be held in the video memory (depending on the display size and the zoom factor).
The video RAM can be accessed via the ACRTC using its data transfer commands.

1.3 The Color Look-up Table

The AGC-2 contains the IMS G170 RGB-DAC with color look-up table, 4 bits/pixel provide 16 colors to be displayed out of the complete range of 262144 colors.
The color look-up table is accessible through the VMEbus/IEEE 1014 interface.
An interrupt in the V-sync phase can be generated to load the color look-up table without any flicker on the monitor.

1.4 The Video Outputs

Four BNC connectors for the connection of a color monitor are provided on the front panel of the AGC-2 board. The RGB outputs have the following characteristics: 0 to 1 V (analog) at 75 Ohm and 32 MHz maximum pixel frequency. A composite SYNC output is also available on the front panel.

1.5 Light Pen Interface

The light pen input of the ACRTC chip is supported via a standard light pen interface and the 15-pin D-sub connector available on the front panel.

1.6 Display Formats

The resolution to be displayed depends on the monitor parameters as well as on the AGC-2 hardware set-ups. The following table lists standard display formats which are supported from the AGC-2 hardware and which are tested with various monitors. All display parameters are software-programmable to offer maximum flexibility and minimize software overhead.

Horizontal × Vertical	Bit/Pixel	No. of Colors	Pixel Frequency	Frame Period	Mode
1160 × 870	4	16	32 MHz	50 Hz	Interlaced
1024 × 800	4	16	32 MHz	60 Hz	Interlaced
800 × 600	4	16	32 MHz	50 Hz	non-Interlaced
720 × 560	4	16	32 MHz	60 Hz	non-Interlaced
690 × 520	4	16	16 MHz	50 Hz	Interlaced
640 × 480	4	16	16 MHz	60 Hz	Interlaced

1.7 The VMEbus Interface

A full VMEbus IEEE 1014 standard interface is installed on the AGC-2 board. The access address and the address modifier code of the board are jumper-selectable within the standard address range (A24 : D8, D16) and short I/O range (A16: D8, D16). The ACRTC, the Bus Interrupter Module BIM 68153, the RGB-DAC IMS G170 and the cursor RAM are accessible under the same address modifier codes. All address, data and control signals are latched and buffered to build the local bus.

1.8 Bus Interrupter Function

A Bus Interrupter Module, BIM 68153, is installed on the AGC-2 board supporting the ACRTC-IRQ output as well as an IRQ on vertical and horizontal SYNC. The BIM includes four channels, each providing interrupt request generation on a software-programmable level (IRQ 1 to 7) with a programmable interrupt vector.

2. Special Functions

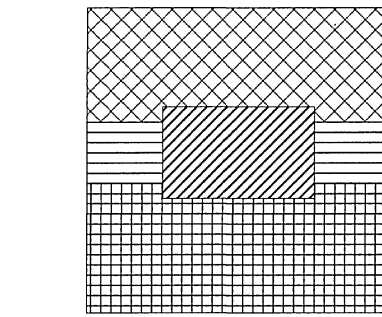
The AGC-2 board contains special hardware logic for zoom, a cursor (independent from zooming and windows) and grid logic (combined with zooming).

2.1 Zoom

A hardware zoom for zoom factors 1 to 16 is installed to provide a flicker-free display supporting the base screen. The x and y zoom factors are independently programmable.

2.2 The Split Screens

The ACRTC offers four different screens which may be displayed simultaneously or independently. The size and position of the base screen, the lower sreen, the upper screen and the windows screen on the monitor is software-programmable. The data for each screen is held in separately defined areas within the frame buffer and the ACRTC handlers the adressing of the appropriate locations to produce the correct complete image:



2.3 The Cursor

The ACRTC chip provides a software controlled cursor which is implemented in hardware on the AGC-2. 8 Kbyte static RAM, accessible via the VMEbus interface and independent from the video RAM, provides a cursor with free programmable color and form in a maximum size of 128 × 128 pixels. The position is independent from zoom and window limits, and is programmable in 1 pixel steps in both horizontal and vertical directions.

2.4 The Grid

A grid with 1 pixel width and the distance of the actual zoom factor can be filled in. The color of the grid is user-programmable.

3. The ACRTC Command Set

The ACRTC chip contains a set of 38 commands dedicated to three groups, register access, data transfer and graphic drawing commands. The five register access commands allow access to the pattern RAM and to the drawing parameter registers. Ten data transfer commands are used to move data between the video memory and the VMEbus host, or within the video memory.

The 23 graphic drawing commands cause the ACRTC to perform drawing separations. The parameters for these commands are specified using logical x-y coordinates. All 38 commands' parameters and data are transferred via the ACRTC Read and Write FIFOs. The following table lists all commands installed on the ACRTC chip:

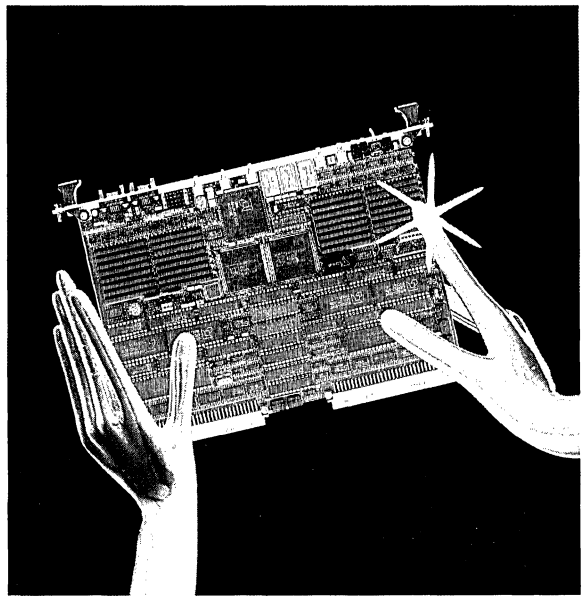
Type	Mnemonic	Function
Register Access Commands	ORG RPR,WPR RPT,WPTN	Set Origin Point Read/Write Parameter Registers Read/Write Pattern RAM
Data Transfer Commands	RD,WT,MOD CLR,SCLR, CPY,SCPY	Read/Write/Modify Clear Copy
Drawing Commands	AMOVE,RMOVE ALINE,RLINE ARCT,PRCT APLL,RPLL APLG,RPLG CRCL ELPS AARC,RARC AEARC,REARC AFRTC,RFRTC PAINT DOT PTN AGCPY,RGCPY	Move Line Rectangle Polyline Polygon Circle Ellipse Arc Ellipse Arc Filled Rectangle Paint Dot Pattern Graphic Copy

Specifications

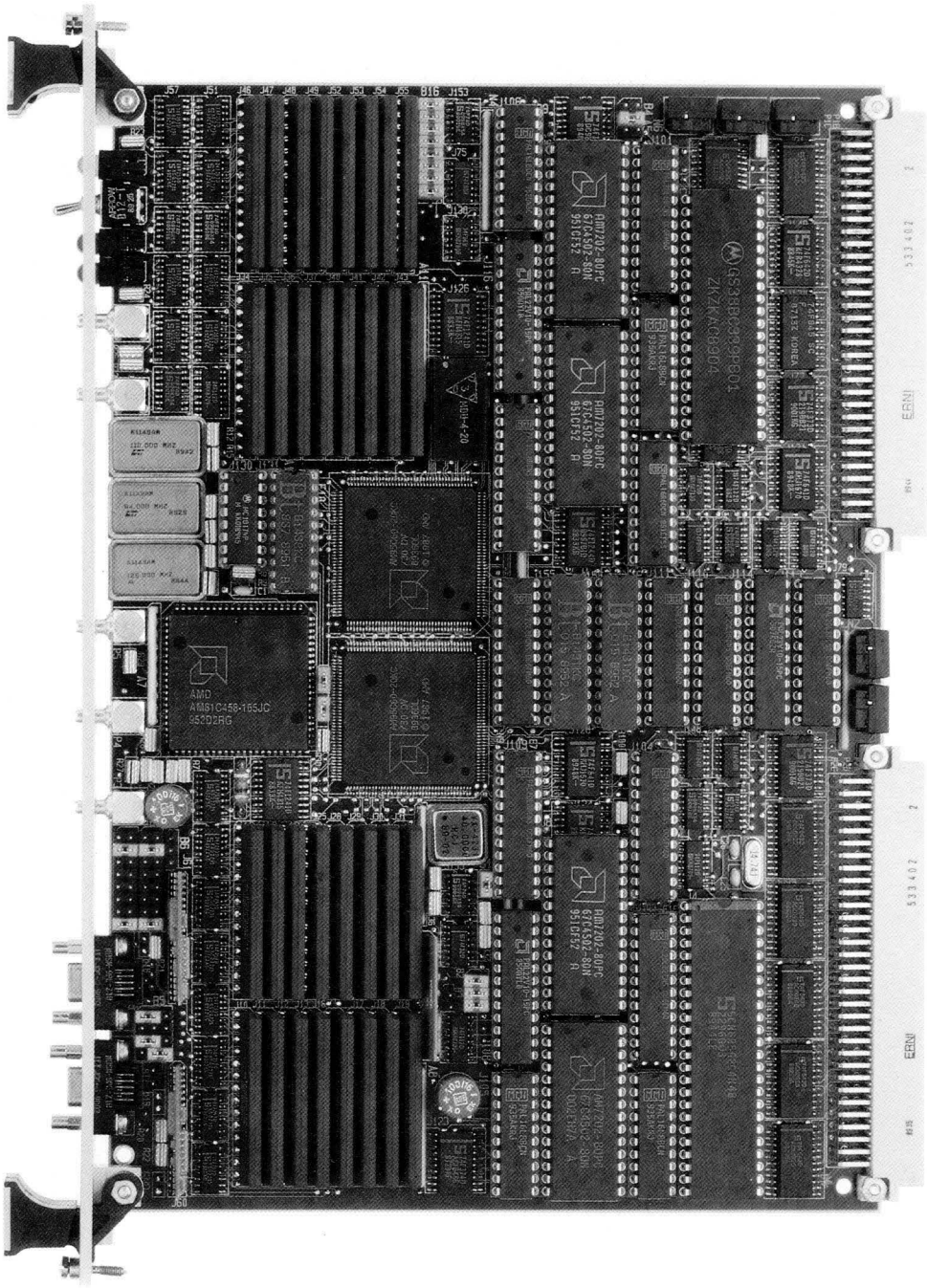
Function	
63484 Graphics Controller	4 MHz
Video memory	1 Mbyte
Display formats (max) 50 Hz interlaced 60 Hz interlaced 50 Hz non-interlaced 60 Hz non-interlaced	 1160 × 870 1024 × 800 800 × 600 720 × 560
Pixed depth Color selection	4 bit 16 of 262144
Video outputs RGB SYNC	16 or 32 MHz 1.0 Vss (75 Ohm) TTL (75 Ohm)
Special functions Hardware Zoom S/W / M/W Cursor Grid Logic Light Pen I/f	 yes yes yes yes
VMEbus Interface: A24, A16 : D8, D16	yes
Power requirements + 5 V (max) + 12 V (max) – 12 V (max)	 3.2 A 0.1 A 0.2 A
Operating temperature with forced air cooling Storage temperature Relative humidity	0 to + 50 °C – 50 to + 85 °C 5 to 90 %
Dimensions	234 × 160 mm : 9.2 × 6.3 in
No. of slots used	1

Ordering Information

SYS68K/AGC-2 Part No. 400023	Advanced Graphics Controller Board. Documentation included.
SYS68K/AGC-2/UM Part No. 800139	User's manual for the SYS68K/AGC-2.



System 68000 VME
SYS68K/AGC-3
Advanced Color Graphics Controller Board


AMD
AM61C458-165JC
9520ZRG

General Description

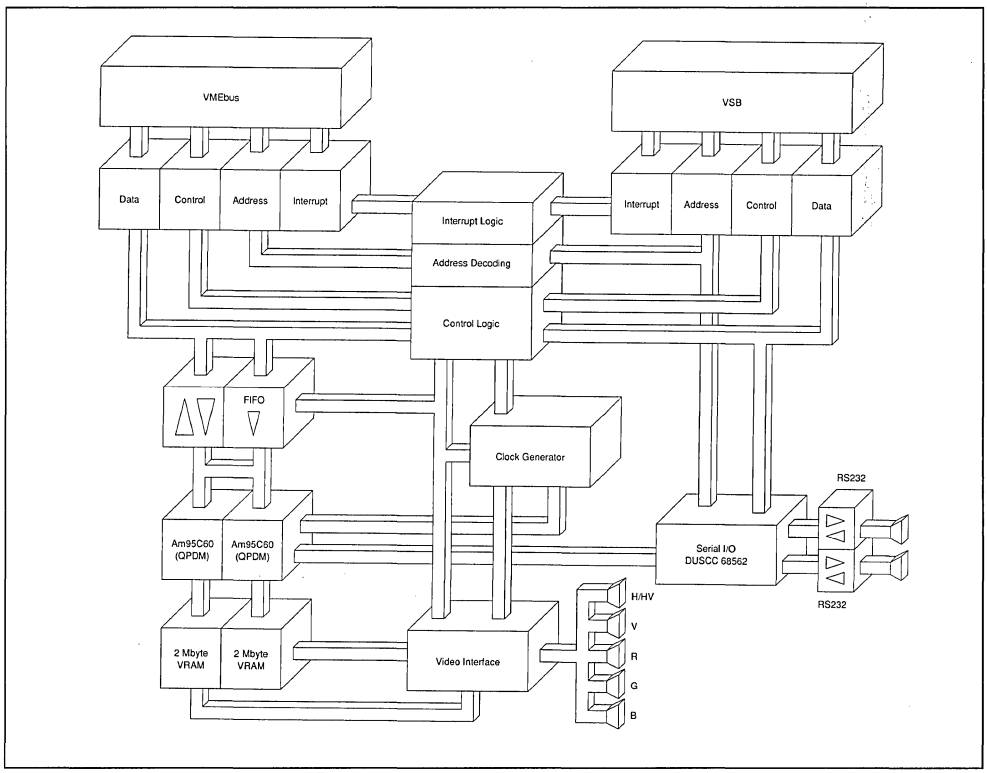
The SYS68K/AGC-3 is a high performance graphics controller board which combines a powerful graphics controller (Quad Pixel Dataflow Manager QPDM) with up to 4 Mbyte video RAM and a color look-up table.
The SYS68K/AGC-3 supports for example the following resolutions and pixel frequencies:

- 1280 × 1024 pixel, 125 MHz pixel frequency
- 1024 × 768 pixel, 75 MHz pixel frequency
- 640 × 480 pixel, 30 MHz pixel frequency.

All resolutions are supported with 4 or 8 bits/pixel and 70 Hz non-interlaced display mode.
Each QPDM is able to handle 4 bits/pixel. Therefore the 4 bits/pixel version of the AGC-3 is installed with one QPDM and the 8 bits/pixel version is installed with two QPDMs. The QPDMs are directly accessible through the VMEbus/VSB or through a FIFO.

The SYS68K/AGC-3 is installed with either 2 Mbyte or 4 Mbyte of video memory.
Two serial I/O channels (RS232-compatible) are provided through a 68562 DUSCC chip and may be used to connect e.g. a mouse and a keyboard.
The interrupts of the on-board devices are handled by the 68153 Bus Interrupter Module (BIM) and are passed to the VMEbus.
The user may configure the SYS68K/AGC-3 to be used in either a VMEbus or a VSB environment via a jumper. The VMEbus slave interface is fully IEEE 1014-compatible. The access address is selectable via a rotary switch and the address modifier codes for access to the on-board devices are jumper-selectable. The VSB Rev.C compatible slave interface contains a switch-selectable access address and a jumper-selectable address space selection for access to the on-board devices.

Block Diagram of the SYS68K/AGC-3 Board



Features of the SYS68K/AGC-3

- Am95C60 (QPDM) graphics controller with a clock frequency of 20 MHz: One QPDM on SYS68K/AGC-3/2, two QPDMs on SYS68K/AGC-3/4
- Video RAM accessible via the QPDM: 2 Mbyte on SYS68K/AGC-3/2, 4 Mbyte on SYS68K/AGC-3/4
- R-G-B and composite SYNC, HSYNC and VSYNC outputs
- Supported features of QPDM: Windowing, Panning and Scrolling
- Graphics color look-up table Bt 459 providing 16/256 simultaneously displayable colors out of a palette of 16.8 million
- Hardware cursor (64 × 64 pixel or cross hair)
- 2 serial I/O interfaces RS232-compatible
- VMEbus/IEEE 1014 slave interface
  A24, A16 : D32, D16, D8
- VSB interface Rev. C compatible
- 32-bit wide FIFO to the QPDM accessible from VMEbus/VSB
- Interrupter to VMEbus with software-programmable IRQ level and vector via BIM
- VSB INTP interrupter
- RUN/LOCAL switch to disable VMEbus/VSB accesses
- Switch-selectable access address
- Jumper-selectable VME address modifiers
- Jumper-selectable VSB address space

1. Functional Description

The QPDM receives the drawing commands from a CPU board through the VMEbus/VSB interface. All address calculations to the video RAM are made internally, which unloads the CPU board, because only x- and y-coordinates may be used. The QPDM chip generates the video memory timing after initialization. According to the board type 1 or 2 QPDMs (with 2/4 Mbyte video memory) are installed driving 4 or 8 color bits/pixel.
4 bits/pixel provide 16 colors and 8 bits/pixel provide 256 colors to be displayed, both out of a complete range of 16777216 colors.

1.1 The QPDM

The Am95C60 Quad Pixel Dataflow Manager (QPDM) is a CMOS graphics processor which contains the necessary circuitry and control functions for driving four bit-mapped memory arrays. Featuring a system clock speed of 20 MHz, the Am95C60 can draw vectors up to 3.3 million pixels per second, or place text at a rate of 50,000 characters per second. Such performance allows the user to efficiently mix text and graphics within the bit map. The Am95C60 also contains graphics primitives which allow easy implementation of graphics standards.
Each Am95C60 interfaces directly to memory planes consisting of dual-port video dynamic memories (VRAMs) and is capable of supporting four planes and display screens up to 2 Kbyte by 2 Kbyte pixels.
The Am95C60 QPDM provides support for the drawing of anti-aliased vectors and circles with various user-defined line styles. Other features include windowing, independent X and Y zoom factors, smooth panning and soft scrolling, picking and clipping.

1.2 The FIFO

A FIFO with a depth of 1024 is installed on the SYS68K/AGC-3 decoupling the VMEbus from the QPDM interface in order to reduce the bus load and latency time for the main CPU. This enables the CPU to write the instructions and data into the FIFO independent from the time the QPDM needs to execute the commands. The differentiation between direct access and FIFO access is achieved through different access addresses.
The FIFO is able to send a "Half Full" interrupt to the bus to inform the CPU about its status.
On the SYS68K/AGC-3/4 the FIFO is 32-bit wide, which results in a total FIFO size of 4 Kbyte. The 32-bit wide organization allows to write data/instructions to the two QPDMs either separately or to both with only one write cycle, thus reducing the bus load.
The FIFO on the SYS68K/AGC-3/2 is 16-bit wide, which results in a total size of 2 Kbyte.

1.3 The Video RAM

For each QPDM 2 Mbyte of video RAM are installed on the SYS68K/AGC-3 board. The size of video RAM allows multiple pictures to be held in the video memory. The number of pictures is obviously depending on the display size and the programmed resolution.
The dual port video RAM can be accessed via the QPDM using its data transfer commands. The serial shift register port of the VRAMs is serving the color look-up table.

1.4 The Color Look-Up Table

One Bt459 CMOS Color Palette is installed on the SYS68K/AGC-3. The RS-343A-compatible Bt459 drives all three primary colors (red, green, blue) of a standard color monitor. It is designed specifically for the high-resolution color graphics market for applications such as image processing, CAE/CAD/CAM, solid modeling, and animation. The Bt459 operates at a video data rate of 125 MHz, which is sufficient to support monitor resolutions of up to 1280 × 1024 pixels. Depending on the board variant, 16 or 256 colors out of an available set of 16777216 colors can be displayed.

The on-chip features of the Bt459 include a 256 × 24 color palette RAM, 16 × 24 overlay color palette RAM, 4:1 input multiplexing of the pixel and overlay ports, bit plane masking and blinking, pixel panning support and 1 × to 16 × integer horizontal zoom support. Overlay and cursor information may optionally be enabled on a pixel-by-pixel basis. The Bt459 has an on-chip three-color 64 x 64 pixel cursor and a three-color full screen or full window cross hair cursor, both fully supported by the SYS68K/AGC-3.

1.5 The Video Outputs

The following video signals are routed to SMB connectors on the front panel of the SYS68K/AGC-3:

R, G, B: Color information (Green composite SYNC via G output possible)
H : Horizontal SYNC
V : Vertical SYNC or Composite SYNC

1.6 The Serial I/O Interfaces

One Dual Universal Serial Communications Controller (DUSCC 68562) is installed on the SYS68K/AGC-3. The Dual Universal Serial Communications Controller 68562 is a single-chip MOS-LSI communications device that provides two independent, multi-protocol, full duplex receiver/transmitter channels in a single package. Each channel consists of a receiver, a transmitter, a 16-bit multi-function counter/timer, a digital phaselocked loop (DPLL), a parity/CRC generator and checker, and associated control circuits.

The two serial I/O channels (RS232-compatible) are available on the front panel via 9-pin micro D-Sub connectors. The serial channels could, for example, be used to connect a mouse and/or a keyboard.

1.7 Display Formats

The resolution to be displayed depends on the monitor parameters as well as on the SYS68K/AGC-3 initialization. The following table lists, as an example, standard display formats which are supported by the SYS68K/AGC-3. Any other resolution can be achieved by re-programming the QPDM, if it is based on one of the three fixed pixel frequencies 30 MHz, 75 MHz or 125 MHz.

1.8 The VMEbus Interface

A full VMEbus IEEE 1014 slave interface is installed on the SYS68K/AGC-3 board. The access address of the board is selectable within the standard address range (A24 : D32, D16, D8) and short I/O range (A16 : D32, D16, D8) in 4 Kbyte steps via on-board rotary switches.

Horizontal × Vertical	Bit/Pixel	No. of Colors	Pixel Frequency	Frame Period	Mode
1280 × 1024	4	16	125 MHz	70 Hz	non-interlaced
1280 × 1024	8	256	125 MHz	70 Hz	non-interlaced
1024 × 768	4	16	75 MHz	70 Hz	non-interlaced
1024 × 560	8	256	75 MHz	70 Hz	non-interlaced
690 × 520	4	16	30 MHz	70 Hz	non-interlaced
640 × 480	8	256	30 MHz	70 Hz	non-interlaced

The QPDM, the FIFO, the Bus Interrupter Module BIM 68153, the Color Palette Bt459 and the Serial I/O Controller DUSCC 68562 are accessible through the VMEbus interface. The AM-codes for standard supervisory and non-privileged as well as short supervisory and non-privileged accesses are jumper-selectable.
Instead of the VMEbus interface the VSB interface can be enabled by another jumper.

1.9 The VSB Interface

The VSB interface which is installed on the SYS68K/AGC-3 is Rev.C compatible. The access address is rotary switch-selectable in 4 Kbyte steps and the address space can be designated by jumpers.
The SYS68K/AGC-3 acts as a D32, D16, D8 slave on the VSB and supports ADO cycles. The alternate, I/O and system address spaces are supported.
The QPDM, the FIFO, the Bus Interrupter Module BIM 68153, the Color Palette Bt459 and the Serial I/O Controller DUSCC 68562 are accessible in the same address space.

1.10 The Interrupt Structure

A Bus Interrupter Module, BIM 68153, is installed on the SYS68K/AGC-3 board supporting the interrupts generated by the QPDM, the DUSCC and the FIFO.
If the SYS68K/AGC-3 is set up to use the VMEbus interface, the BIM provides interrupt request generation on a software-programmable level (IRQ 1 to 7) with a programmable interrupt vector.
If the SYS68K/AGC-3 is set up to use the VSB interface, an interrupt request is handled in the INTP Mode.

2. The QPDM Command Set
Instruction Set Grouped by Classification

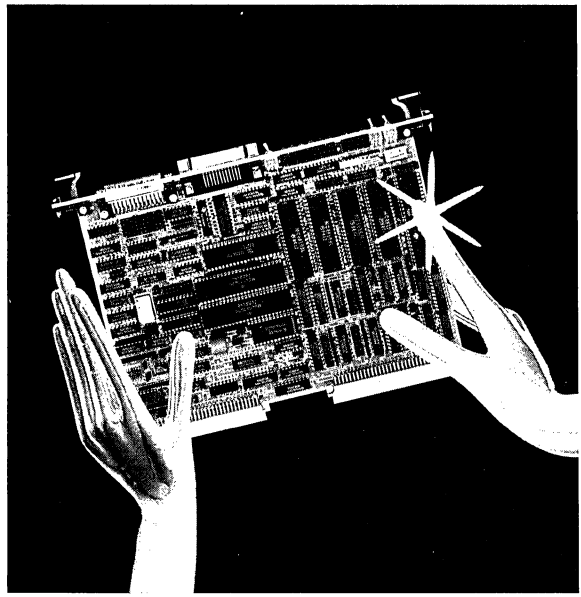
Drawing Primitives	System Control
Arc Arc Current Circle Circle Current Line Line Current Line Reversible Line Reversible Current Move Pen Point Point Current String String Current	Call Control Clipping Control Picking Define Logical PEL Inquire Jump No Operation Output Current Pen Position Pop Current Pen Position Push Current Pen Position Return Set Activity Bits Set Anti-aliasing Distance Set Listen Bits Set QPDM Position Set Stack Boundaries Signal Store Current Pen Position
Fill Instructions	**Display Control**
Fill Bounded Region Fill Bounded Region Current Fill Connected Region Fill Connected Region Current Filled Rectangle Filled Rectangle Current Filled Triangle Filled Triangle Current	Set Block Size Set Character Font Base Set Character Font Base Current Set Clipping Boundary Set Clipping Boundary current Set Color Bits Set Search Color Set Line Style Set Line Style Phase Set Picking Region Set Picking Region Current Set Scale Factor Set Viewport Location Set Viewport Location Current Store Immediate Store Immediate Current
Block Manipulation	
Copy Block Copy Block Current Input Block Input Block Current Output Block Output Block Current Transform Block Transform Block Current	

Specifications

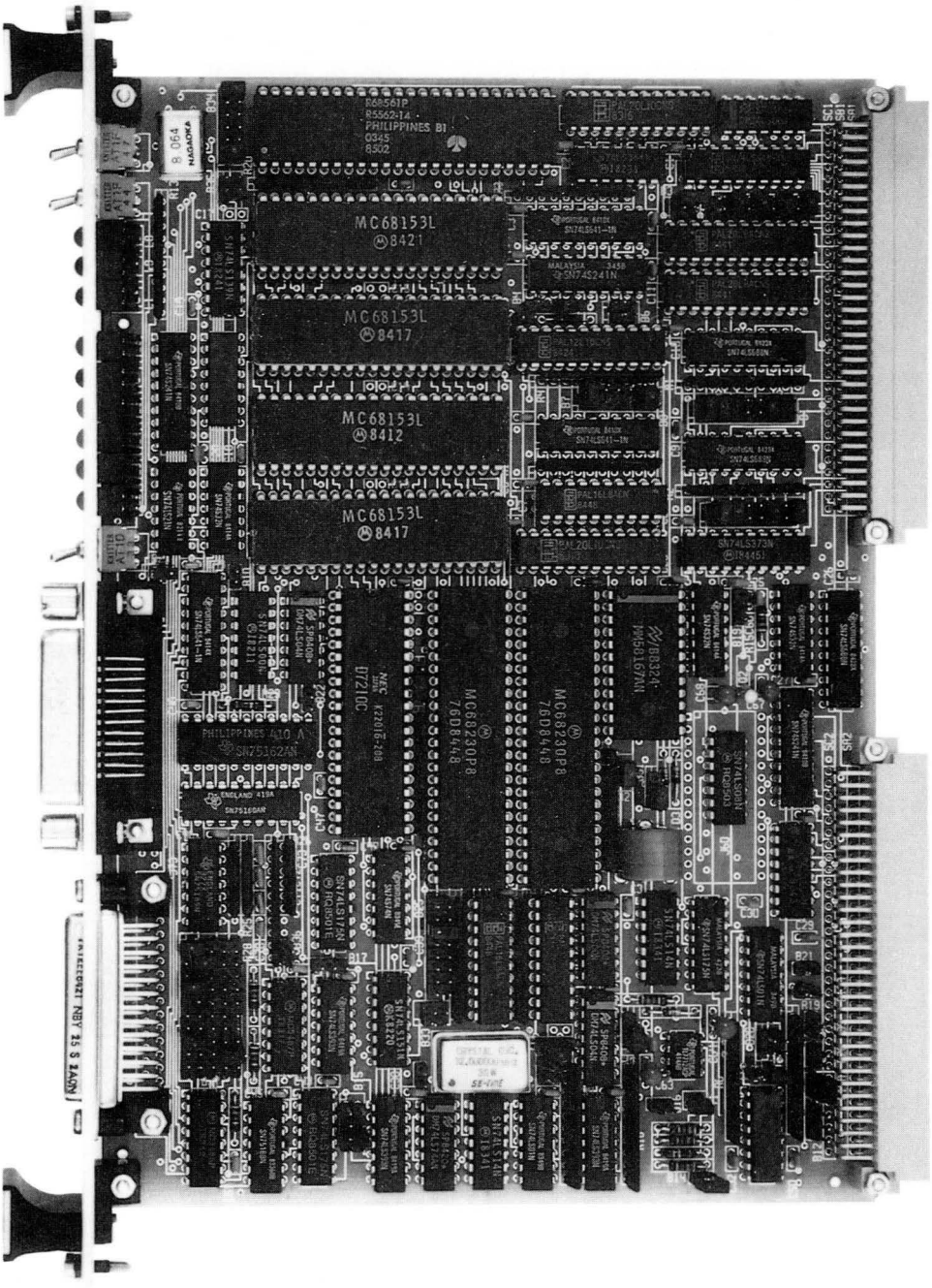
Function		
Graphics controller		Am95C60 (QPDM)
Graphics controller clock frequency		20 MHz
Display format examples at 70 Hz non-interlaced		1280 × 1024 1024 × 768 640 × 480
Video memory	SYS68K/AGC-3/2 SYS68K/AGC-3/4	2 Mbyte 4 Mbyte
Pixel depth	SYS68K/AGC-3/2 SYS68K/AGC-3/4	4 bit 8 bit
Color selection	SYS68K/AGC-3/2 SYS68K/AGC-3/4	16 of 16777216 256 of 16777216
Video outputs	 RGB Horizontal SYNC Vertical or composite SYNC	30, 75 or 125 MHz 1.0 Vss (75 Ohm) TTL (75 Ohm) TTL (75 Ohm)
Special functions	Hardware Cursor Windowing Panning Scrolling Character generation	yes yes yes yes yes (QPDM)
VMEbus interface (IEEE1014): A24, A16 : D8, D16, D32, ADO, RMW		Slave
VSB interface (Rev. C): A32 : D8, D16, D32, ADO		Slave
Power requirements	+ 5V min : max + 12V min : max – 12V min : max	5.2 A : 6.0 A 0.1 A : 0.3 A 1.0 A : 0.3 A
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)		0 to + 50 °C – 40 to + 85 °C 5 to 95 %
Board dimensions		234 x 160 mm : 9.2 x 6.3 in
No. of slots used		1

Ordering Information

SYS68K/AGC-3/2 Part No. 400100	Advanced Graphics Controller Board with one QPDM, 2 Mbyte video memory, 2 serial I/O channels. Documentation included.
SYS68K/AGC-3/4 Part No. 400101	Advanced Graphics Controller Board with two QPDMs, 4 Mbyte video memory, 2 serial I/O channels. Documentation included.
SYS68K/AGC-3/LIB Part No. 400120	Source code of the SYS68K/AGC-3 software library and terminal emulation in C language.
SYS68K/AGC-3/UM Part No. 800190	User's manual for the SYS68K/AGC-3.
SYS68K/CABLE AGC-3 Part No. 700110	Set of five adapter cables SMB to BNC connector, length 1m.
SYS68K/CABLE MICRO-9 SET 1 Part No. 700101	Set of three adapter cables 9-pin micro D-sub male connector to 9-pin D-sub female connector, length 2 m.
SYS68K/CABLE MICRO-9 SET 2 Part No. 700102	Set of four adapter cables 9-pin micro D-sub male connector to 25-pin D-sub female connector, length 2 m.



System 68000 VME
SYS68K/ASCU-2
Advanced System Control Unit


MC68153L
8421
MC68153L
8417
MC68153L
8412
MC68153L
8417
MC68230P8
76D8448
MC68230P8
76D8448

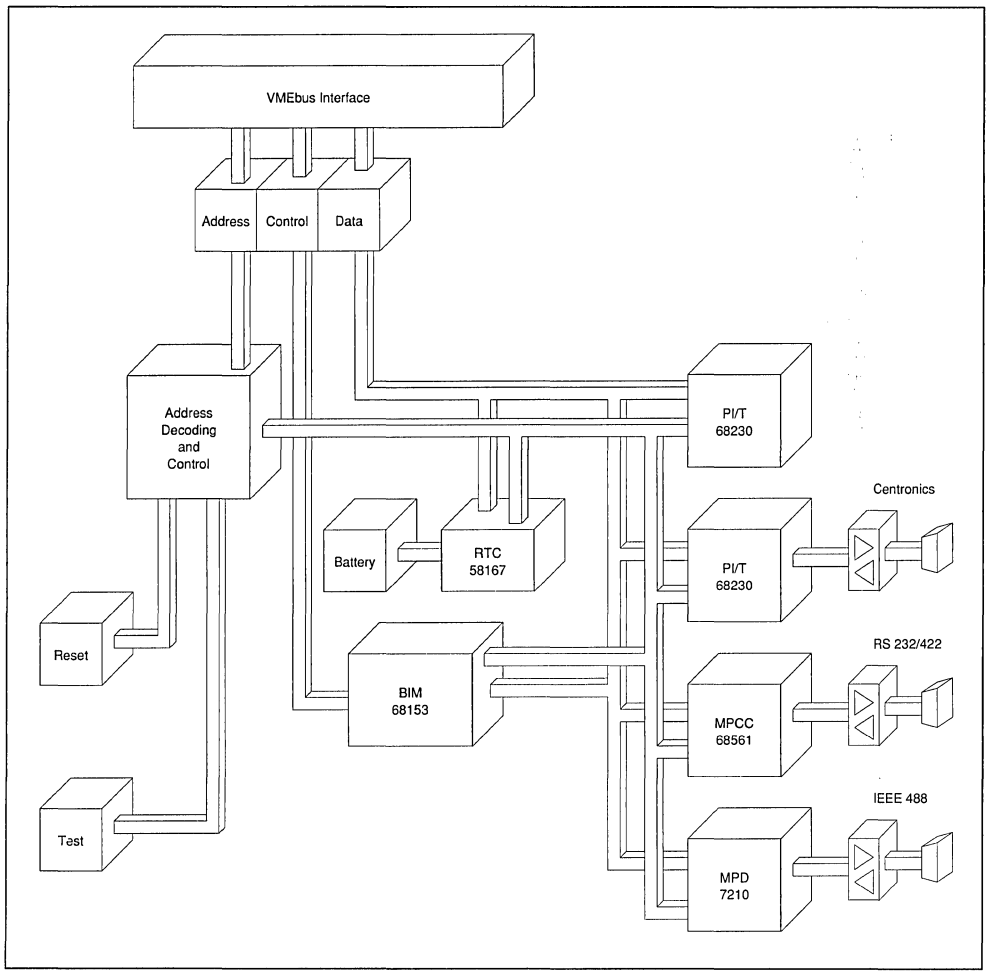
General Description

The SYS68K/ASCU-2 board is a high-performance system controller which handles all exception signals on the VMEbus and contains powerful I/O devices such as a serial interface (RS232- and RS422-compatible), a Centronics parallel interface, a Real Time Clock with battery back-up, and a four-level bus arbiter. The block diagram shows the different building blocks in detail.

Features of the SYS68K/ASCU-2

- Four-level bus arbiter with prioritized, Round Robin, and prioritized Round Robin operating modes
- LEDs show the current bus master level (0–3)
- High-speed serial I/O channel with built-in 68561 Multi-Protocol Communications Controller, RS232/RS422
- Centronics parallel interface for printer connection
- General Purpose Interface Bus (IEEE 448) talker, listener, and controller functions

Block Diagram of the SYS68K/ASCU-2



- Eight different interrupts to the VMEbus (level and vector programmable)
- Four user interrupts (buffered inputs through P2 connector)
- 58167A Real Time Clock with on-board battery back-up
- Power Monitor provides automatic power-up/power-down and ACFAIL*/SYSRESET* handling through power fail detection. A reset function switch generates a SYSRESET* to the VMEbus
- SYSCLOCK driver (16 MHz)
- Bus Timer with software-selectable time-outs for bus error generation
- Timer interrupt can be used for time measurements or as a watchdog
- Software-selectable option for generating an interrupt on ACFAIL* detection
- Test function switch generates an interrupt to the VMEbus on a software-programmable level
- Every I/O device interrupt can be programmed to one of the 7 IRQ-levels on the priority interrupt bus
- Jumper-selectable access address and address modifier codes
- VMEbus slave interface

1. The Serial I/O Interface

A Multi-Protocol Communications Controller (MPCC 68651) with an 8/16-bit data path is used on the ASCU-2 to provide maximum flexibility for serial communications.

Protocols:

- IBM synchronous (ASCII or EBCDIC)
- Character oriented protocols (BSC, DDCMP, X3.28, X.21, ECAMA 16, etc.)
- Synchronous bit-oriented protocols (SDLC, HDLC, ADCCP, X.25)
- Standard asynchronous protocol

A software-programmable baud rate generator (from 100 to 38400 baud) and the local loop-back are provided. The pin assignments to the 25-pin D-sub connector on the front panel of the two interfaces (one RS232/RS422-compatible interface) are jumper-selectable.

The MPCC can initiate an interrupt to the VMEbus on a software-programmable level; three different interrupt vectors are programmable.

2. The Centronics Interface

A Parallel Interface and Timer device (68230 PI/T) is used on the SYS68K/ASCU-2 to provide a Centronics parallel interface. All of the interface signals are fully buffered in both directions and are connected to the user I/O pins of connector P2.

Interrupts on a software-programmable level and vector can be generated through the on-board Bus Interrupter Modules (68153 BIM).

3. The GPIB Interface

The board contains an IEEE 488 interface with a standard connector available on the front panel. The advanced controller (µPD7210) provides full protocol handling of the different modes.

Each of the talker, listener, and controller functions are software-programmable. The talker and the listener address is jumper-selectable and readable via port B of the additional Parallel Interface and Timer device (PI/T 68230).

4. The Interrupt Generator

The ASCU-2 contains four Bus Interrupter Modules (BIM 68153) for a complete set of 16 different interrupts. Two BIM devices are used on the ASCU-2 to provide, in conjunction with port A of the additional PI/T, 8 software-programmable interrupts to the VMEbus. This feature allows easy multi-processor communication because the level and the vector of each IRQ is separately software-programmable. The interrupt line is released following an access to a BIM register.

5. The User Interrupts

Five different interrupt sources can be connected to the P2 connector to provide external exception setting. This feature allows external devices or other systems to issue interrupts to a VMEbus system. The input signals are fully buffered.

6. The Real Time Clock

The Real Time Clock (58167A RTC) allows various applications such as time scheduling, time measurement, counting and simple calendar functions. The RTC is proviced with battery back-up from the on-board lithium battery.

The RTC is able to generate an interrupt to the VMEbus on a software-programmable interrupt level. The interrupt vector is also software-programmable.

7. Local Control and the Bus Timer

The PI/T is used on the SYS68K/ASCU-2 to provide a Centronics parallel interface. Additional PI/T I/O lines are used to control the VMEbus error time-out values. The ASCU-2 contains 8 different software-programmable bus time-out values. One of the 8 possible time-outs can be selected to generate a BERR to the VMEbus (1, 2, 4, 8, 16, 32, 64 or 8000 µsec). As an IACK cycle chain may take between 1 and 10 µsec more time than a normal cycle, a separate BERR time-out mechanism is included for IACK cycles. This time-out is selectable in the range from 30 to 120 µsec.

8. The Test Switch

The ASCU-2 board contains a test switch which generates an interrupt to the VMEbus on a software-programmable level and vector. The P2 connector can also be used in parallel to connect an external switch for interrupt generation.

9. The ACFAIL* Handling

If a POWERFAIL is detected on the VMEbus ACFAIL* line or on an additional input on the P2 connector, a SYSRESET* is generated after a defined time (please refer to paragraph 10).

10. The RESET Handling

The SYS68K/ASCU-2 handles the power-up/ power-down mechanism on the VMEbus.
The ASCU-2 contains a power monitor module as well as a counter for the ACFAIL* time to generate a SYSRESET* (jumper-selectable from 1 to 16 µsec).
A RESET of the whole system may be programmed through the PI/T. Additionally, a switch on the front panel can generate a SYSRESET*. Provision is made on the P2 connector to use an additional RESET switch (all the logic for the switch is included).

11. The Four-Level Bus Arbiter

A special bus arbiter is built on the ASCU-2 card to provide maximum flexibility for multi-processor environments.
The three modes are jumper-selectable for the arbiter

- Prioritized scheme
- Round Robin scheme
- Prioritized Round Robin scheme

In all modes the bus clear signal (BCLR*) will be generated if a higher prioritized request is pending. Additionally a time-out is provided to avoid potential hang-ups which may occur if the bus has been granted to a master which has not taken ownership of the bus by asserting BBSY (bus busy).
The current VMEbus master level and the activities on the bus clear line are shown on five LEDs on the front panel.

12. The Access Selection

The SYS68K/ASCU-2 can be accessed under a jumper-selectable access address and address modifier code.
The following modes are automatically assigned through an enabled address-modifier code:

A24, A16 : D8, D16

The following address-modifier codes are jumper-selectable:

No	AM-Code	Decode	Hex Code
1)	Standard Supervisory Data Access	A24	3D
2)	Standard Non-privileged Data	A24	39
3)	Access Short Supervisory	A16	2D
4)	I/O Access Short Non-privileged	A16	29
5)	I/O Access Ignore all AM Codes	A24	–

Specifications

Description	
IEEE 488 (GPIB) interface	yes
Serial/IO interface RS422	yes
RS232	yes
Centronics parallel interface	yes
Real Time Clock with battery back-up	yes
Software-programmable bus timer (2 to 12000 µs)	yes
ACFAIL* handling	yes
SYSFAIL* handling	yes
TEST/RESET* switches	yes
IACK* daisy chain driver	yes
Interrupts to priority interrupt bus	16
Software-programmable interrupts	8
User interrupts on P2	5
Four-level bus arbiter	yes
Address selection A24, A16 : D16	yes
Power requirements + 5 V (max)	3.6 A
+ 12 V (max)	200 mA
– 12 V (max)	200 mA
Operating temperature with forced air-cooling	0 to + 60 °C
Storage temperature	– 55 to + 85 °C
Relative humidity (non-condensing)	5 to 95 %
Board dimensions	233 × 160 mm : 9.2 × 6.3 in

Ordering Information

SYS68K/ASCU-2 Part No. 700007	System control unit with IEEE 488 interface and interrupt generator for eight independent interrupts. Documentation included.
SYS68K/ASCU-2/UM Part No. 800047	Hardware user's manual for ASCU-2.

I/O Boards

FORCE COMPUTERS

Serial and Parallel I/O Board Introduction

FORCE COMPUTERS offers a full selection of general purpose I/O boards that satisfies most general purpose application needs for both serial and parallel I/O. The family includes not only straight serial I/O boards but also considerable intelligence and performance advantages offered by the ISIO and IPIO families.

For general purpose parallel I/O, look no further than the SYS68K/PIO-1. This board provides four 8-bit interface channels provided by the four 68230 parallel interface and timer chips installed on the board. The board offers four 8-bit output ports and four opto-coupled 8-bit parallel input ports. Both the input and the output ports are supported by two handshake signals each.

If your application also requires a DMA controller on your parallel I/O board or the facility of being totally opto-isolated from the interface, then the SYS68K/OPIO-1 board may be the board for you. This board is also installed with four 8-bit parallel interfaces via four 68230 parallel interface and timer chips. The board additionally offers full opto-isolation (1000 V) on both the input and the output channels. As an added feature, a 4-channel DMA controller is installed on the board to allow high speed data transfers to/from VMEbus memory and the 68230 PI/T chips.

The SYS68K/IPIO-1 offers 64 lines of parallel I/O controlled by a 68000 processor on-board. The CPU, running out of 128 Kbyte of zero wait state SRAM, controls the parallel I/O functions under VMEPROM. The user interfaces to VMEPROM via the VMEPROM shell, which provides an interface to the VMEbus via a serial port emulation. The IPIO-1 may be installed with different modules which allow the user to configure for TTL I/O, optically isolated I/O or relays.

For general purpose serial I/O applications, the SYS68K/SIO-2 board offers 6 channels, configurable for either RS232 or RS422 communication. Available baud rates are from 110-38.4 K and all synchronous and asynchronous protocols are supported. These interfaces provide high security, high reliability and data integrity over a serial interface.

For high performance intelligent serial I/O interfaces, the SYS68K/ISIO-2 board provides no wait state performance. The board features high performance serial I/O using the 68010 (10 MHz) for the on-board intelligence. The processor runs without wait states from the on-board RAM. The ISIO-2 has 128 Kbyte of on-board memory and may be configured to communicate using the RS232 or the RS422 communication standard. The ISIO-1/2 families are the intelligent serial communication solution.

For completeness, FORCE COMPUTERS has also provided advanced information on its new Intelligent Communication Controller, the ICC-1. Providing up to 6 lines of full duplex serial I/O, each with individual DMA control, 68020 intelligence, FGA-002 based VMEbus interface and up to 4 Mbyte of DRAM or SRAM, ICC-1 is the communication controller of the 90's.

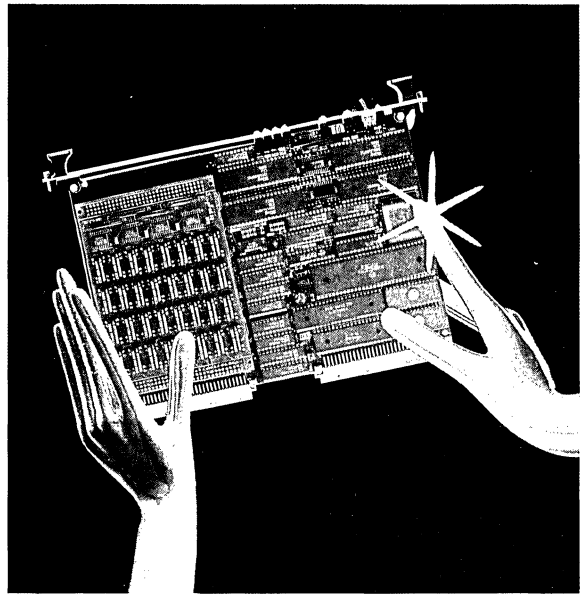
Parallel I/O Boards

FAMILY	IPIO-1	PIO-1	OPIO-1
Processor type Frequency	68000 10 MHz	– –	– –
Dual-ported SRAM No. of wait states	128 Kbyte 0	– –	– –
EPROM capacity	128 Kbyte	–	–
VMEPROM	yes	–	–
No. of output signals Interface type Isolation voltage Propagation delay (max.)	32 TTL/OPTO/Relay[1)] up to 1000 V[1)] [1)]	32 TTL (64 mA) 5 V 10 nsec	32 opto-coupled (30 mA) 1000 V 50 nsec
No of input signals Interface type Isolation voltage Propagation delay (max.)	32 TTL/OPTO/Relay[1)] up to 1000 V[1)] [1)]	32 opto-coupled 1000 V 50 nsec	32 opto-coupled 1000 V 50 nsec
No. of Parallel Ports Input Output No. of handshake signals per port	4 × 8 bit 4 × 8 bit 2	4 × 8 bit 4 × 8 bit 2	4 × 8 bit 4 × 8 bit 2
No. of timers (24-bit/16-bit)	1/4	4/0	4/0
Used parallel interface chips	Z8536 (4 ×)	68230 (4 ×)	68230 (4 ×)
No. of different IRQs No. of different IRQ vectors IRQ -level to the VMEbus	4 4 1-7 (SW-progr.)	8 8 1 (fixed)	8 8 1-7 (SW-progr.)
DMA controller Clock frequency Data transfer capability	68450 10 MHz 8-bit	– – –	68450 8 MHz 8-, 16-bit

1) Depending on used I/O module

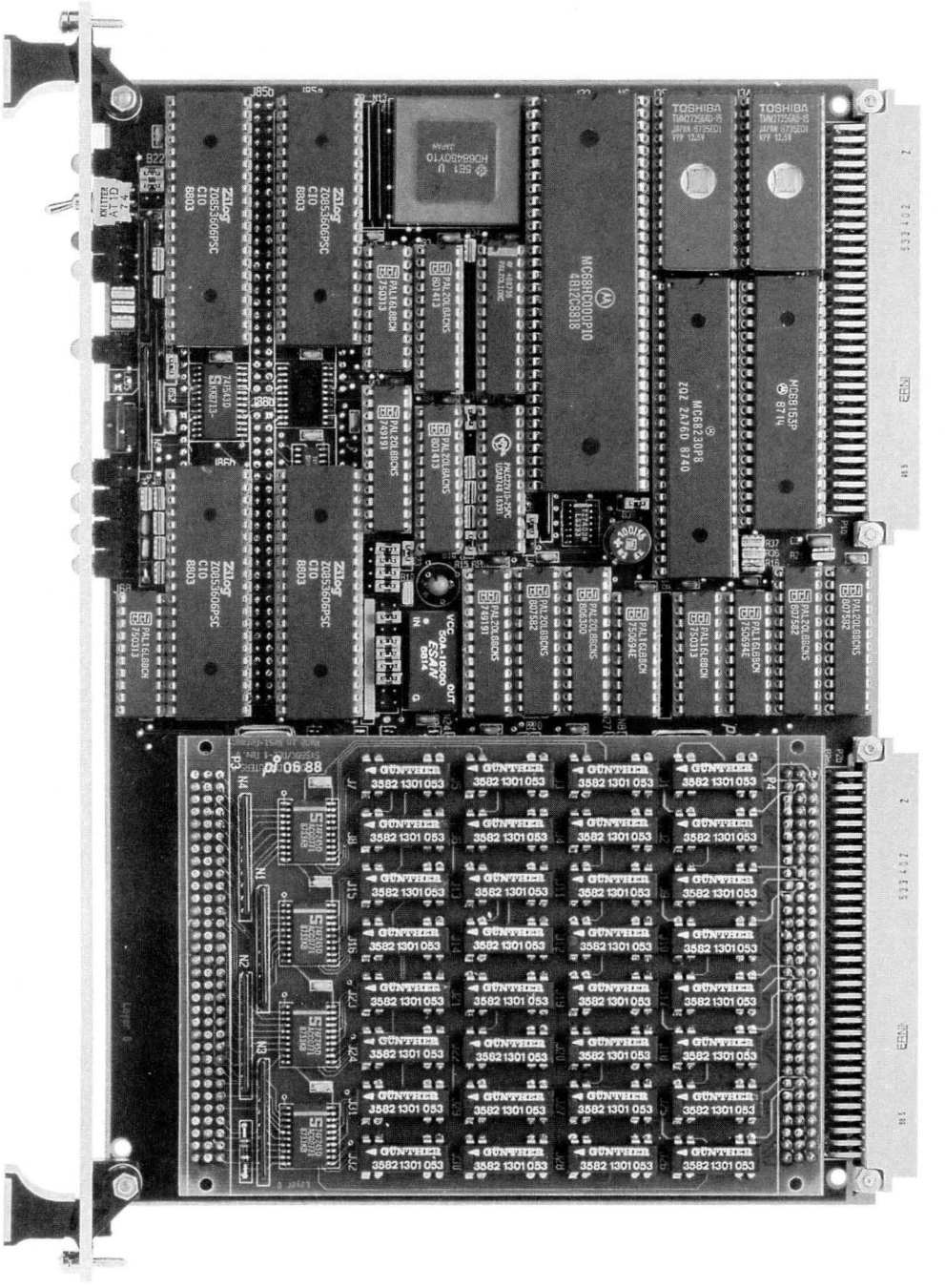
Serial I/O Boards

FAMILY	SIO-2	ISIO-2	ICC-1
No. of ports Synchronous/asynchronous RS232 RS422 RS485 Baud rate	6 yes 6 6 0 150–38400	8 yes 8 8 0 50–38400	4/7 yes 4/7 3/6 3/6 150–38400
Used controller chips	68561 (6×) (MPCC)	68562 (6×) (DUSCC)	68302 (1/2) (IMP)
Processor type Frequency		68010 10.0 MHz	68020 25.0 MHz
DMA controller type Frequency			FGA-002 25.0 MHz
Main memory type Capacity min. max. No. of wait states RAM function		SRAM 128 Kbyte 128 Kbyte 0 shared	SRAM/DRAM 1 Mbyte 4 Mbyte 0 shared
Buffer memory type Capacity min. max. No. of wait states RAM function			SRAM 512 Kbyte 1 Mbyte 0 shared
EPROM type Capacity max. Data bus width		Standard 128 Kbyte 16 Bit	FLASH/Standard 1 Mbyte/512 Kbyte 16 Bit/8 Bit
VMEbus interrupt vectors		4 IRQs selectable	7 (software-programmable)
VMEbus interface type Address decoding Data transfer size Unaligned transfers Read Modify Write	Slave A24, A16 D8, D16 yes yes	Slave A24, A16 D8, D16 yes yes	Master/Slave A32, A24, A16/A32, A24 D8, D16, D32/D8, D16, D32 yes yes



System 68000 VME
SYS68K/IPIO-1

Intelligent Parallel I/O Controller Board


Zilog
Z0853606PSC
C10
8803
MC68HC000P10
4B12C8318
MC68230P8
ZOZ 2A16D 8740
TOSHIBA
TMM2256AP-15
PAL16L8BCN
PAL20L8BCNS
PAL20L8BCNS
GÜNTHER
3582 1301 053

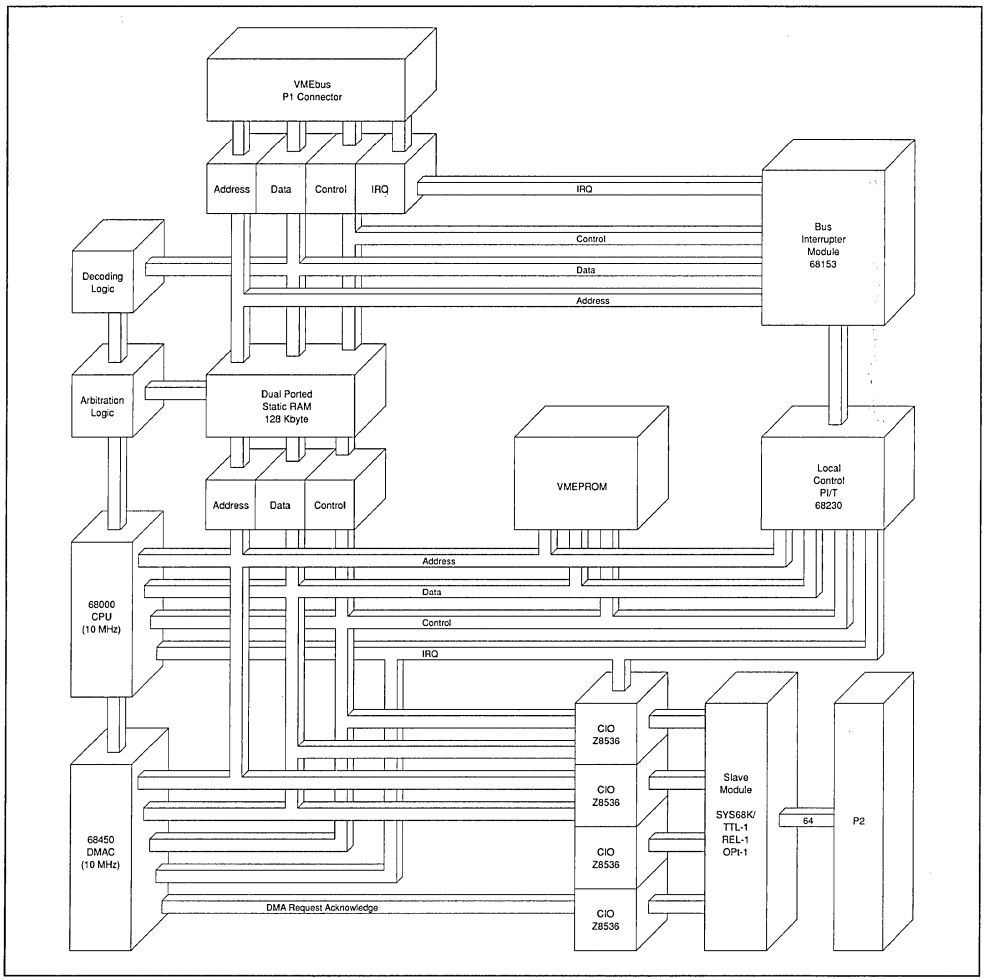
General Description

The SYS68K/IPIO-1 is a high performance intelligent parallel I/O controller board, providing local intelligence with a 68000 CPU and a high speed DMA controller. The four channels of the DMA controller may be coupled with four 8-bit ports of the four parallel I/O chips to optimize data throughput.

128 Kbyte Dual Ported RAM (DPR) is used to store commands and data, which the DMA controller and the CPU access without wait states, independent from all VMEbus accesses.

The parallel interfaces of the IPIO-1 controller board are built using four Z8536 CIO devices. Each of these devices contains two independent double buffered 8-bit I/O ports, one special purpose 4-bit I/O port, and three 16-bit counter/timers. The parallel I/O signals of the Z8536 devices are connected to a piggy-back module mounted on the IPIO-1 board. This module adapts the IPIO-1 board to various applications such as opto-isolated I/O, TTL I/O or relay output. All I/O signals are connected to the VMEbus P2 connector of the IPIO-1 board.

Block Diagram of the SYS68K/IPIO-1



The IPIO-1 contains a VMEbus, IEEE 1014-compatible interface to communicate to host CPUs via 128 Kbyte of dual-ported memory. The firmware of the IPIO-1 board is built using a subset of VMEPROM, a Real Time Kernel/ Monitor based on the Real Time Kernel of PDOS.
This firmware package provides facilities for program downloading and debugging. Debugged software can be burned into the EPROM for target environments using the Real Time Kernel.

Features of the SYS68K/IPIO-1

- 68000 CPU for local control (10 MHz)
- 68450 DMA controller (10 MHz) connected to the four Z8536 I/O devices
- Dual-ported 128 Kbyte zero wait state SRAM
- 64-bit parallel I/O signals available on the P2 connector grouped into eight 8-bit ports
- 16-bit special purpose I/O bits for DMA interconnection, handshaking or timer control
- Twelve 16-bit counter/timers
- Interrupt on pattern recognition location to interrupt via "AND" or "OR" mask, or the "OR Priority Encoded Vector" mode
- Four different interrupt request channels to the VMEbus. Each channel contains a software-programmable IRQ level (1 to 7) and vector
- Local parallel interface for controlling and monitoring board functions
- VMEbus IEEE 1014-compatible slave interface (A24 : D8, D16)
- Watchdog timer monitoring functions of on-board hardware and software
- Status and control LEDs for monitoring local activities
- Rotary switch on the front panel for software set-up options
- VMEPROM on-board, including Real Time Kernel and debugging monitor

1. The Hardware Functions

The local CPU responds to commands and initialization parameters placed in the 128 Kbyte Dual Ported RAM. Constant runtimes are guaranteed through the synchronous arbitration logic which provides zero wait state operation for the local 68000 CPU from the Dual Ported RAM, independent of the accesses from the VMEbus. The IPIO-1 provides self-test functions as well as a hardware watchdog timer which monitors the activities of the 68000 CPU and the 68450 DMA Controller running at 10 MHz clock frequency. User supplied programs can be loaded into the Dual Ported RAM and executed from the local CPU to adapt the IPIO-1 to user applications. The local CPU manages the DMA controller and four parallel I/O devices while communicating to the host CPU through the DPR and/or by way of the interrupt requests to the VMEbus generated by a Bus Interrupter Module.

1.1 The Local 68000 CPU

A 10 MHz 68000 CPU is installed on the IPIO-1 to control the data traffic between the parallel I/O interface(s) and the Dual Ported RAM. Two EPROMs with a total capacity of 128 Kbyte are installed on the IPIO-1 which contain VMEPROM. Constant zero wait state operation from the EPROM guarantees maximum CPU throughput. The 128 Kbyte of Dual Ported RAM is accessible constantly without the insertion of wait states. The accesses from the CPU to the DPR are not delayed if a VMEbus access is pending or being executed.
A local timer included in the on-board PI/T is used to interrupt the CPU for task scheduling, command interpretation, and execution.
The CPU and all I/O devices can be reset through a system reset via the SYSRESET* signal of the VMEbus or by accessing a dedicated location within the DPR reserved for this function.

1.2 The 68450 DMAC

The IPIO-1 contains a four-channel DMA controller (68450) with a clock frequency of 10 MHz. The DMA controller is connected to four of the eight 8-bit ports of the IPIO-1 to maximize data throughput to/from the parallel I/O interface and to free the local 68000 processor from data transfers. The DMA controller accesses the Dual Ported RAM without the insertion of wait states.

1.3 The Parallel I/O Interfaces

The SYS68K/IPIO-1 contains four Z8536 CIO chips for parallel I/O. Each device contains two general purpose 8-bit ports and one special purpose 4-bit port. All 80 pins are connected to a piggy-back module which connects the eight 8-bit ports to the P2 connector. Four of the eight 8-bit ports are also coupled with the four channels of the 68450 DMA controller.

The parallel I/O port of the Z8536 CIO devices features double buffered, bi-directional I/O ports, four handshake modes, and flexible pattern recognition logic. The pattern recognition logic allows interrupt generation on an input or output pattern. Three operating modes are supported which are "1's catcher", "AND" and "OR".
The special purpose 4-bit I/O port of each parallel I/O chip may be used for bit I/O, for one of four different handshake modes, or for connection to one of the four DMA channels provided by the 68450 DMA controller of the IPIO-1.

1.4 The Counter/Timers

Each of the four Z8536 CIO devices on the SYS68K/IPIO-1 contains three 16-bit counter/timers. A total of 12 counter/timers are available for the user. The timers feature four external access lines for each counter/timer and three output duty cycles, programmable as retriggerable or non-retriggerable.

1.5 The PI/T 68230

A 68230 Parallel Interface and Timer (PI/T) chip is installed on the SYS68K/IPIO-1 to control and display the status of all on-board activities. The PI/T is also used to force and monitor interrupt request lines to the Bus Interrupter Module which initiates the interrupts to the VMEbus under control of the host CPU. One handshake pin is used to interrupt the local CPU if a defined location within the DPR is accessed from the VMEbus. One output signal is used to force a SYSFAIL* signal to the VMEbus if an on-board failure has been detected. The timer, also included in the PI/T, is the time base for the on-board handling firmware and the Real Time Kernel. A watchdog timer for processor monitoring is installed on the board to signal software or hardware errors independent from the on-board CPU.
The 4-bit rotary switch located on the front panel of the IPIO-1 can be read via the PI/T device. The first four of the 16 positions are predefined by VMEPROM, the additional 12 positions are free for use by application programs.
A 4-bit code identifies which interface module is used on the IPIO-1 board. This code is readable by software via the PI/T device so that the user program can take the necessary actions required for the special module.

1.6 The Dual-Ported RAM

128 Kbyte of dual-ported SRAM with 45 nsec access time is installed on the SYS68K/IPIO-1 to service applications requiring fast operations and large data areas. The local 68000 CPU runs without the insertion of wait states from the DPR because CPU clock synchronized arbitration logic and a fully buffered and latched VMEbus interface are implemented on the IPIO-1.
A VMEbus cycle is serviced and completed between two CPU access cycles.
A partition of the DPR is reserved for the local CPU as vector storage and temporary buffers. This partition can be accessed from the VMEbus to program the BIM to initiate an interrupt to be handled by the on-board CPU to generate a local RESET.
The local DMA controller, which is connected to four Z8536 I/O devices also runs without the insertion of wait states when accessing the Dual Ported RAM. The VMEbus access address and address modifier codes are jumper-selectable in 128 Kbyte increments within the standard address range (A24 : D8, D16). The VMEbus access times of the DPR depend on the accesses made by the local CPU as the local 68000 has priority over VMEbus accesses.

2. The Parallel Interface Mezzanine Modules

In the default configuration the eight 8-bit ports of the Z8536 CIO device are directly connected to the P2 connector of the IPIO-1 board. If a decoupling of the parallel I/O devices is required several modules are available.

2.1 Opto-Isolated Module

The SYS68K/OPT-1 provides a maximum of 32 opto-isolated input and 32 opto-isolated output pins. 16 pins may be used as handshake pins instead of 8 in- and 8 output pins. Four GND pins and four VCC pins for external supply of the opto-coupler are available. This configuration reduces the number of I/O signals by eight.
The output pins can be used as four 8-bit parallel ports or two 16-bit parallel ports. The same is valid for input pins.
Bi-directional data transfer is possible if the in- and output pins are externally connected.

2.2 TTL I/O Module

The SYS68K/TTL-1 provides a maximum of 32 in- and 32 output pins. 16 pins may be used as handshake pins instead of 8 in- and 8 output pins. Four GND pins are available to make the GND connection between TTL-1 modules via the 64 user pins of the VMEbus P2 connector if the VMEbus system GND is not used. However, this option reduces the number of I/O signals by four. The output pins can be used as four 8-bit parallel ports or two 16-bit parallel ports. The same is valid for the input ports. An input voltage between 0 V and 0.8 V is recognized as logical low and an input voltage between 2.4 V and 24 V as logical high. The inputs have Schmitt Trigger Logic. Bi-directional data transfer is possible if the in- and output pins are connected externally.

2.3. Relay Output Module

The SYS68K/REL-1 supplies 32 relay outputs. Each output consists of two signal lines which can be connected via a relay. The maximum switch current is 0.5 A and the maximum voltage is 100 V. The total power is limited to 10 W per relay.

3. The VMEbus Interface

A VMEbus IEEE 1014 interface is installed on the SYS68K/IPIO-1, to allow accesses to the DPR. The access address and the address modifier code is jumper-selectable. The 16-bit data width (D8, D16) of the DPR and the decoding of the standard address range (A24) allow easy installation in all VMEbus environments.

A Bus Interrupter Module (BIM 68153) is implemented on the board to support fully asynchronous operation with the four different software-programmable interrupt request channels.

During power-up and after reset has been executed, the IPIO-1 drives the VMEbus signal SYSFAIL* active to signal each board in the VMEbus environment that the board is not yet successfully initialized. A reset for the local CPU can be initiated by accessing a dedicated address within the DPR. All local devices as well as the CPU will be reset through this access.

VMEbus to DPR	Access Time	Cycle Time
Best case	330 nsec	400 nsec
Average	430 nsec	500 nsec
Worst case	560 nsec	630 nsec

An interrupt to the local CPU can be forced by accessing another location within the DPR, signaling the on-board processor that a command has been given, or that an exception has to be taken.

3.1 The Bus Interrupter Module

To allow fully asynchronous operation, the IPIO-1 contains a Bus Interrupter Module (BIM 68153) providing four individually programmable interrupt channels. Each channel is able to force an interrupt request to the VMEbus. For each channel, the IRQ-level (1 to 7) as well as the interrupt vector is fully software-programmable. The local CPU forces interrupt requests to the BIM and the host CPU can program the interrupt vector and level. This allows dynamic assignment of the interrupt level and vector in multi-processor environments.

4. Firmware

Firmware for the IPIO-1 is based on VMEPROM, an EPROM-resident Real Time Kernel/Monitor, supplied as standard on the board free of charge. The complete package resides in 64 Kbyte of the on-board 128 Kbyte EPROM space. 64 Kbyte of EPROM space is free for the user's application programs. VMEPROM is composed of the powerful PDOS Real Time Kernel. The kernel features over 80 system calls which are available for user programs. The user interface is an I/O Port which is emulated in the DPR. The user interface contains more than 30 commands perfectly suited for program debugging.

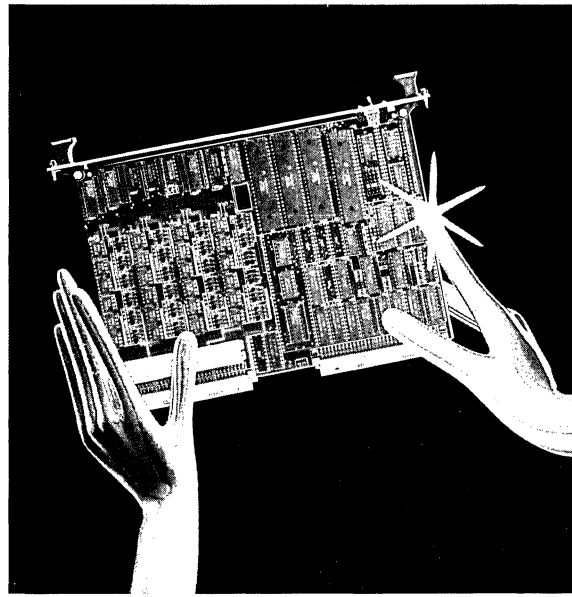
Debugged user programs can be loaded into EPROM and may be executed automatically after power-up or reset. The user program is invoked after the on-board self-test is executed and the kernel is initialized.

Specifications of the SYS68K/IPIO-1 and Modules

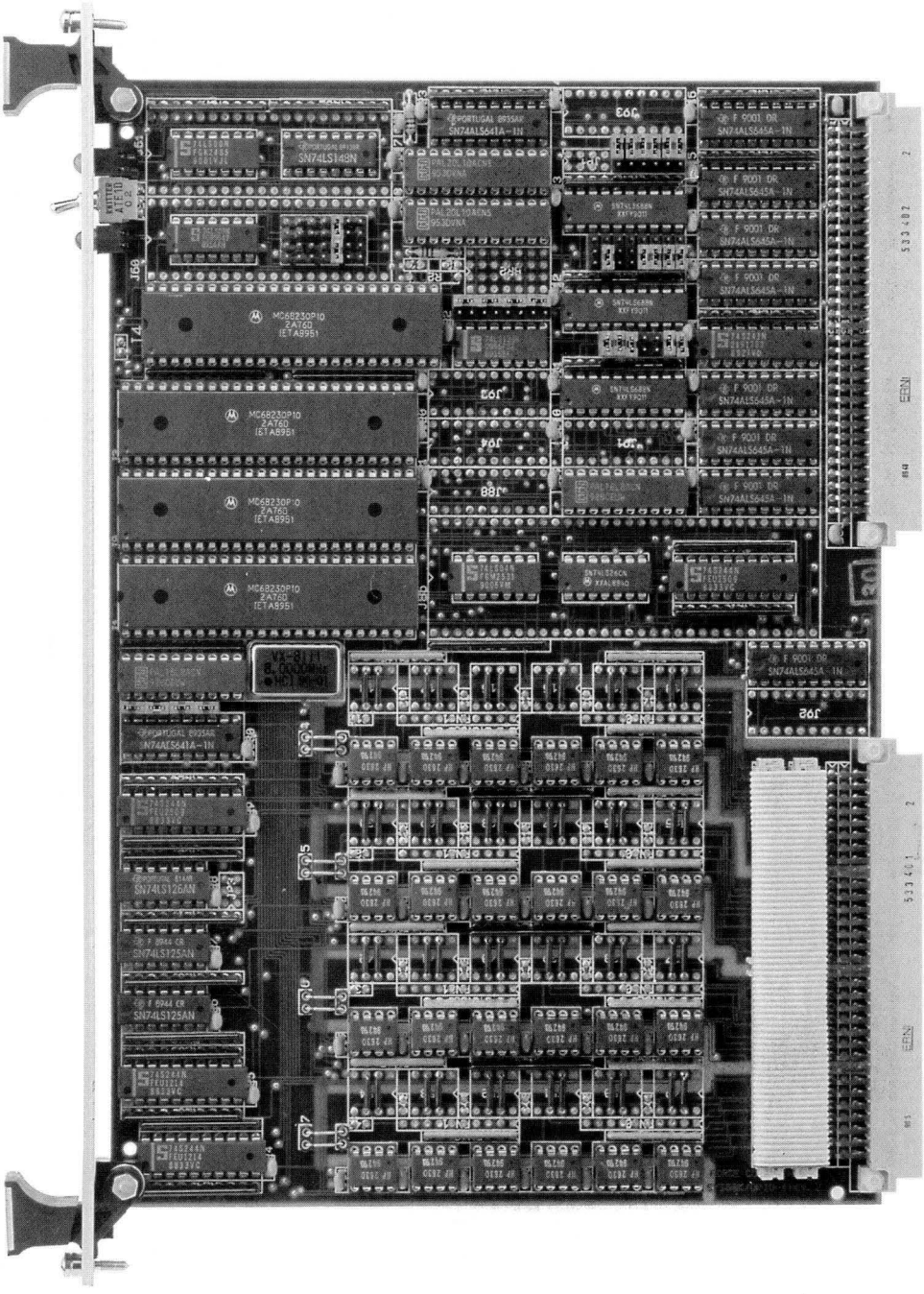
SYS68K/IPIO-1	
68000 CPU clock frequency 68450 DMA clock frequency	10 MHz 10 MHz
EPROM capacity EPROM wait states	128 Kbyte 0
Dual-ported RAM Local CPU wait states	128 Kbyte 0
I/O channels Controller chip used 8-bit channels available DMA support for 8-bit channels	 Z8536 8 4 channels
Firmware support	VMEPROM
Power requirements + 5 V (max)	4.5 A
Operating temperature with forced air cooling Storage temperature (non-operating) Relative humidity (non-condensing)	0 to + 50 °C – 50 to + 85 °C 5 to 90 %
Board dimensions	234 × 160 mm : 9.3 × 6.3 in
SYS68K/OPT-1	
Input/output signals	32
Opto-isolation	1000 V
Power requirements + 5 V (max)	1.5 A
SYS68K/TTL-1	
Input signals with Schmitt Triggers Logical low voltage Logical high voltage	32 0 V to 0.8 V 2.4 V to 24 V
Output signals Logical low voltage Logical high voltage Output current	32 6 V to 6.7 V 3 V to 5 V 40 mA (max)
Power requirements + 5 V (max)	1.5 A
SYS68K/REL-1	
Output signals	32
Switching voltage (max) Switching current (max)	100 V 0.5 A
Power requirements + 5 V (max)	1.5 A

Ordering Information

SYS68K/IPIO-1 Part No. 310050	Intelligent parallel I/O controller board with local DMA controller, including VMEPROM. Documentation included.
SYS68K/TTL-1 Part No. 310054	32 output signals, 32 TTL input signals. Documentation included.
SYS68K/OPT-1 Part No. 310053	32 opto-isolated output lines with 1000 V isolation, 32 opto-isolated input lines with 1000 V isolation. Documentation included.
SYS68K/REL-1 Part No. 310052	32 relay outputs capable of switching up to 100 V. Documentation included.
SYS68K/IPIO-1/UM Part No. 800163	User's manual for the IPIO-1.



System 68000 VME
SYS68K/PIO-1
Multi-Channel Parallel I/O Board



General Description

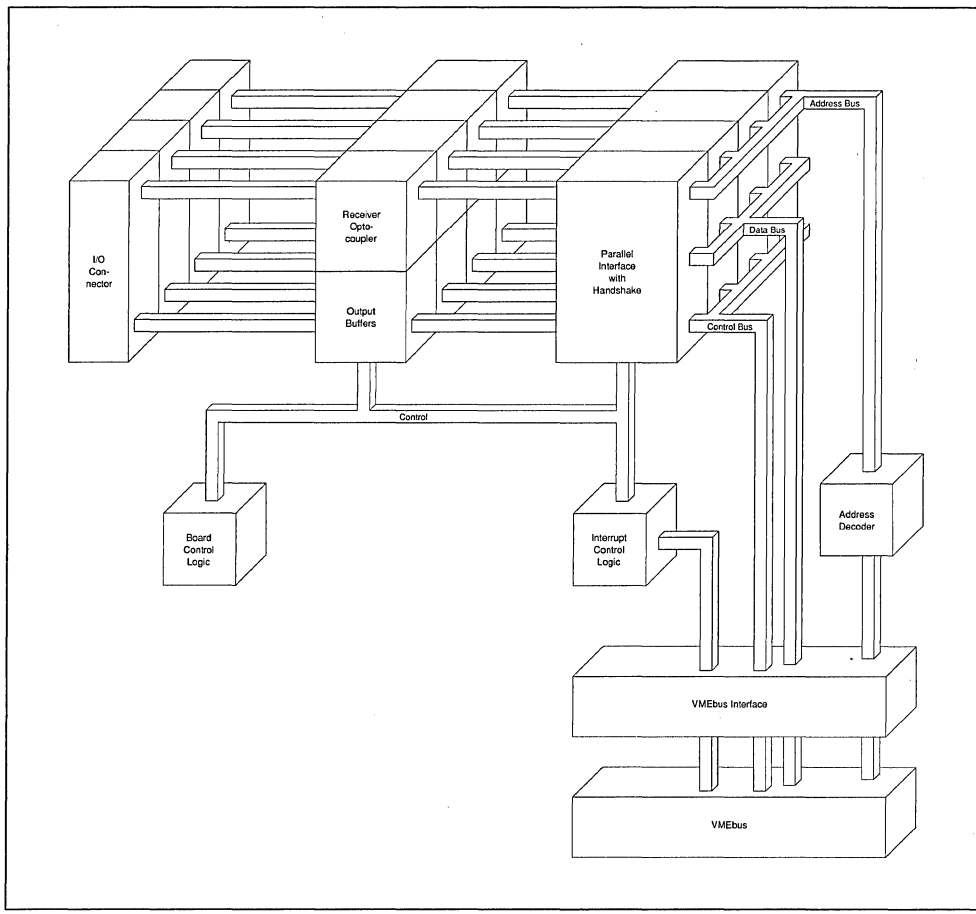
The SYS68K/PIO-1 is a high performance parallel I/O board based on the VMEbus. Four interface units provide four input and four output channels, each 8-bit wide.

Each input signal is opto-coupled, providing current sensing. Each output signal is driven by TTL buffers. To allow fully asynchronous operation of the SYS68K/PIO-1, each Parallel Interface and Timer module (PI/T) can force handshake or timer interrupts to the VMEbus. The interrupt vectors are software-programmable, the level is jumper-selectable.

Features of the SYS68K/PIO-1

- Four TTL buffered 8-bit parallel output ports with two handshake signals per port
- Four opto-coupled 8-bit parallel input ports with two handshake signals per port
- Four timers (24-bit)
- Interrupt capabilities: Four timer interrupts, four I/O handshake interrupts; each interrupt has a software-programmable vector
- Jumper-selectable access address and address modifier code
- Fully VMEbus compatible
- RUN/LOCAL function switch
- RUN/LOCAL indicators

Block Diagram of the SYS68K/PIO-1



1. The Parallel Ports

The parallel I/O is designed using 4 Parallel Interfaces and Timer devices (PI/T 68230/ -8 MHz).
Each PI/T includes the following features:

- All registers are directly addressable with Read/Write cycles
- Special port interrupt service request
- Four different interrupt vectors for the port interrupts
- 8-bit output port
- 8-bit input port
- Selectable handshaking modes

All input and handshake input signals are routed to high speed opto-couplers (HCPL2630) to provide maximum flexibility of the voltage ranges. The typical propagation delay of each opto-coupler is 50 nsec. Each I/O channel with the two ports contains a separate power supply input to provide a supply voltage for the opto-coupler. Alternately, the standard power from the VMEbus (+ 5 V) can be used to drive the opto-coupler.
Each I/O signal is available through two 64-pin I/O connectors or through the 64-pin DIN connector (P2). The SYS68K/PIO-1 is able to operate in a 16-bit parallel mode because two of the 4 PI/T devices are connected to the lower data bus (D0–D7) and the other two devices are connected to the upper data bus (D8–D15). This allows parallel transfer of 16-bit data with a common handshake.

2. The Timer Operation

Each PI/T device contains a 24-bit timer capable of generating an interrupt. Therefore four different timer interrupts can be generated from the SYS68K/PIO-1.

3. The Interrupt Structure

The four PI/T port service request and timer interrupt request outputs are gated to drive one jumper-selectable request level on the VMEbus. The port service request interrupt has four software-programmable vectors, and the timer interrupt has one software-programmable vector per PI/T. 20 software-programmable interrupt vectors are provided for by the SYS68K/PIO-1.

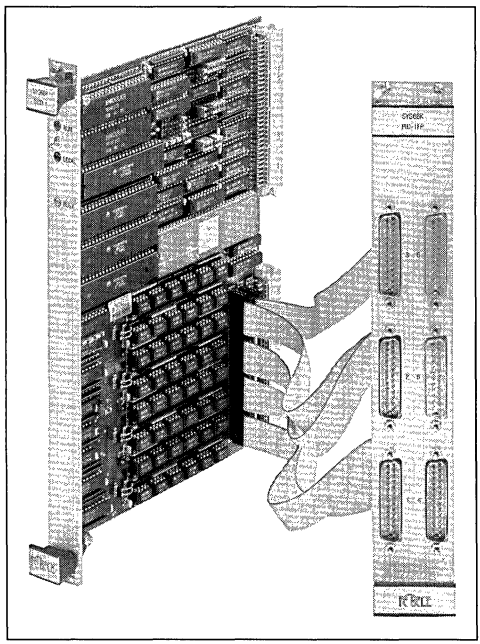
4. The Addressing

The SYS68K/PIO-1 contains flexible address and address modifier decoding logic. The access address and the address modifier code are jumper-selectable (A24 or A16 mode). Therefore, both standard and the short I/O addressing modes are supported.

5. Front Panel with Six I/O Connectors

The SYS68K/PIO-1FP is a double-width (12HE/8TE) front panel, providing six 25-pin D-sub male connectors, each with flat cable which plug into the 64-pin headers on the SYS68K/PIO-1.
The connectors 1, 2, 3 and 4 are configurable for bi-directional operation. Connectors 5 and 6 are each configurable for either in- or output. The assignment of the connectors to the I/O channels is user-selectable, as well as the individual configuration of the bi-directional I/O ports or separate input and output ports.

SYS68K/PIO-1FP

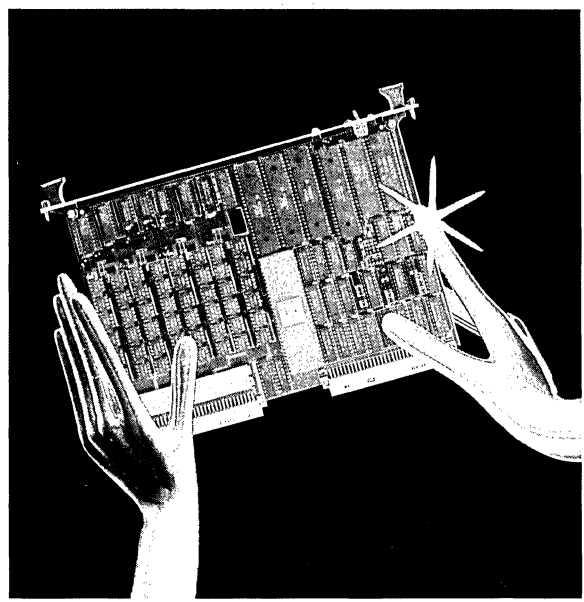


Specifications

Interface	4 TTL level parallel I/O channels
Channel configuration	Input: 8 lines data 2 lines handshake Output: 8 lines data (64 mA sink) 2 lines handshake direction control
Channel level	TTL compatible voltage Receiver sinks 8 mA for logic 0
Devices	Four Parallel Interface/Timer (68230) 24 opto-couplers (HCPL2630)
Interrupt	Jumper-selectable interrupt request level 20 different interrupt vectors possible
VMEbus interface	(A24, A16 : D16)) Jumper-selectable board base address Address modifier decoding
Address space	512 byte
Power requirements	+ 5 V/2.0 A (typ) + 5 V/2.5 A (max)
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)	0 to + 50 °C – 50 to + 90 °C 5 to 95 %
Board dimensions	234 × 160 mm : 9.2 × 6.3 in

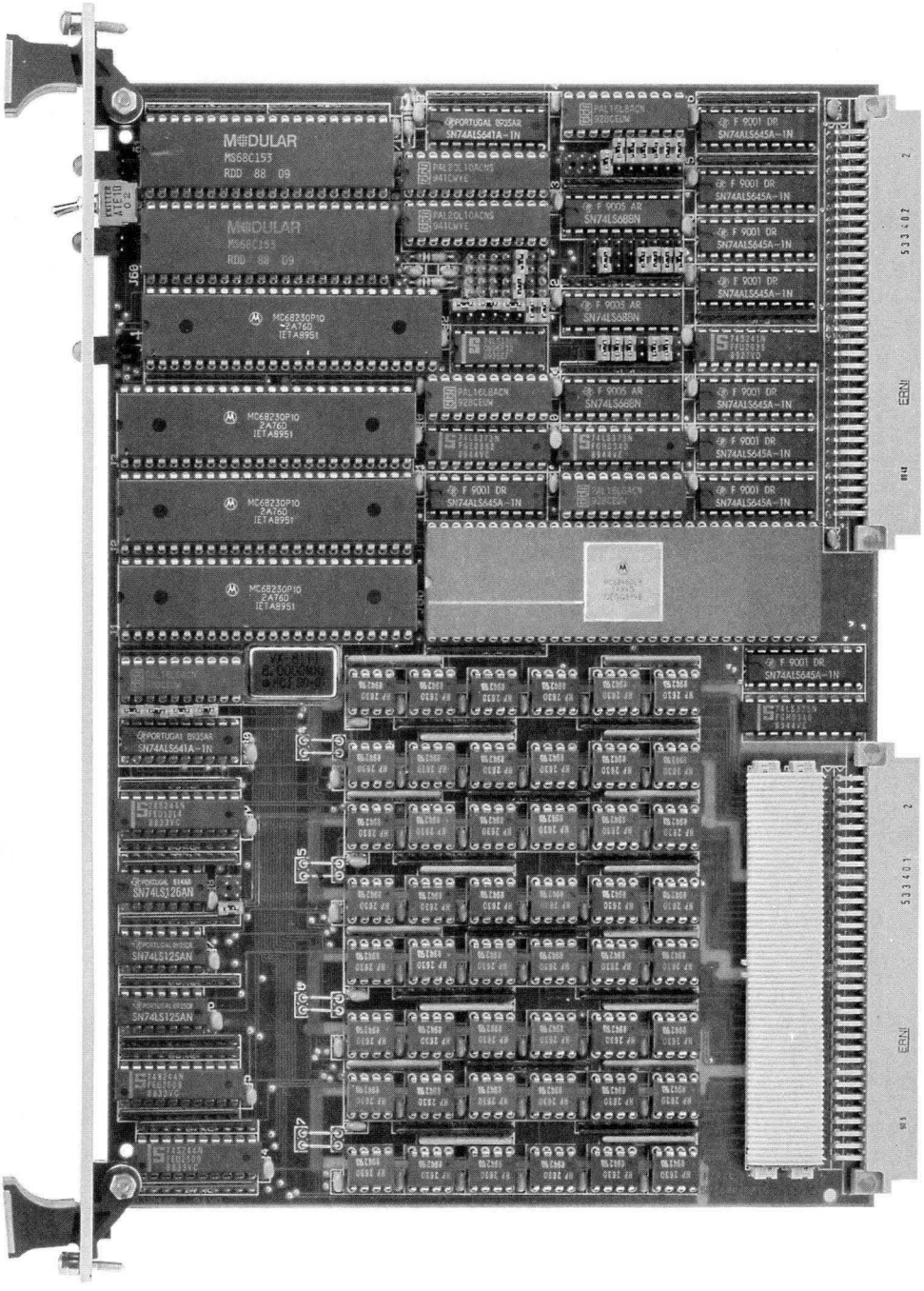
Ordering Information

SYS68K/PIO-1 Part No. 310010	Parallel I/O board. Documentation included.
SYS68K/PIO-1FP Part No. 310012	Front panel for the parallel I/O signals.
SYS68K/PIO-1/UM Part No. 800028	User's manual for the SYS68K/PIO-1 board.



System 68000 VME
SYS68K/OPIO-1

Multi-Channel Opto-Isolated Parallel I/O Board with DMA


MODULAR
MS68C153
RDD 88 09
MODULAR
MS68C153
RDD 88 09
MC68230P10
2A760
IETA8951
MC68230P10
2A760
IETA8951
MC68230P10
2A760
IETA8951
MC68230P10
2A760
IETA8951
PORTUGAL 8935AR
SN74ALS641A-1N
F 9001 DR
SN74ALS645A-1N
F 9005 AR
SN74LS688N
PORTUGAL 8935AR
SN74ALS641A-1N
SN74LS126AN
SN74LS125AN
SN74LS125AN
533402
533401

General Description

The SYS68K/OPIO-1 is a high performance parallel I/O board based on the VMEbus. Four interface units provide four input and four output channels, each 8-bit wide.

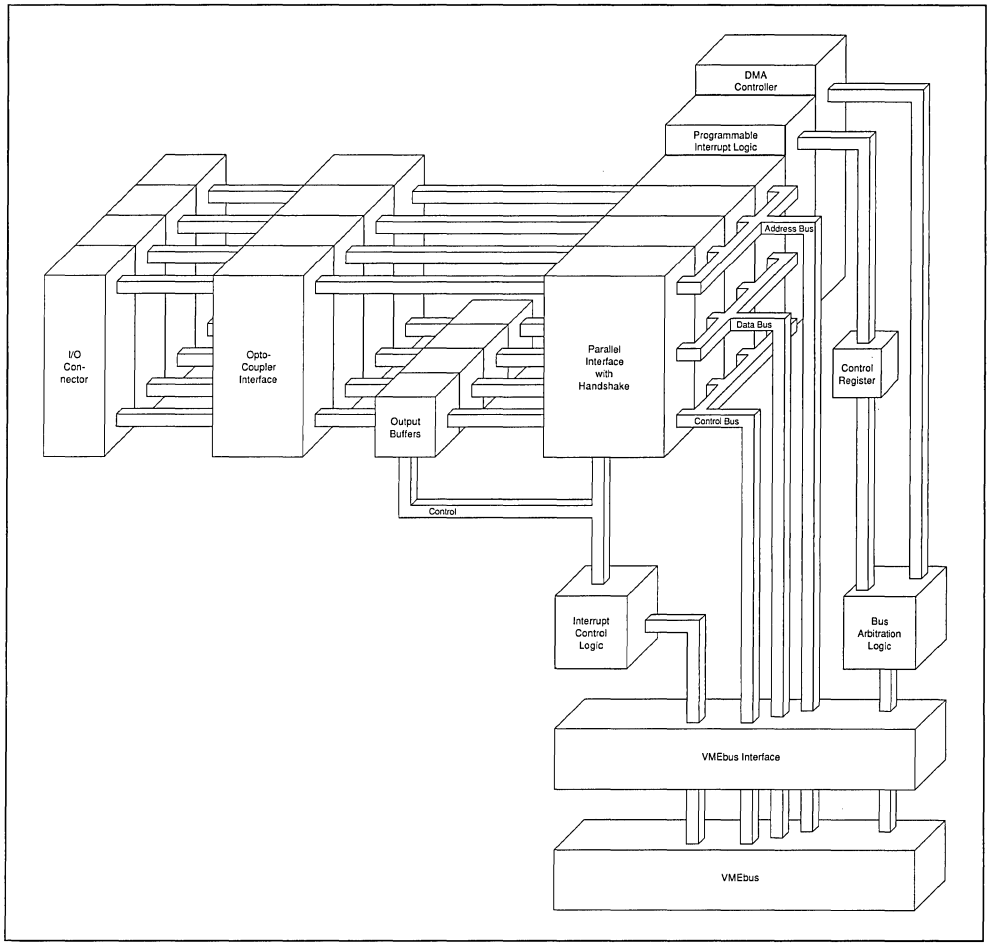
Each input and output signal is opto-coupled to provide maximum flexibility. For high speed data transfers, a four-channel DMA controller is provided on the board.

To allow fully asynchronous operation of the SYS68K/OPIO-1, each Parallel Interface and Timer module (PI/T) can force handshake or timer interrupts to the VMEbus. The interrupt vector and the level are both software-programmable.

Features of the SYS68K/OPIO-1

- Four opto-isolated to 1000 V 8-bit parallel output ports with two handshake signals per port (opto-isolated)
- Four opto-isolated to 1000 V 8-bit parallel input ports with two handshake signals per port (opto-isolated)
- DMA Controller directly coupled to the I/O ports for high speed transfers, directly coupled to the I/O ports

Block Diagram of the SYS68K/OPIO-1



- VMEbus master/slave interface for the DMAC
- Four timers (24-bit)
- Interrupt capabilities: Four timer interrupts, four I/O handshake interrupts, one DMA controller interrupt, each interrupt has a software-programmable vector and level (1–7)
- Control register to perform flexible bus release functions (RWD, ROR, RAT)
- Jumper-selectable access address and address modifier code
- Fully VMEbus compatible
- RUN/LOCAL function switch
- RUN/LOCAL and DMA busy indicators

1. The Parallel Ports

- The parallel I/O is designed using 4 Parallel Interface and Timer devices (PI/T 68230-8 MHz). The clock frequency is 8 MHz. Each PI/T includes the following features:
- All registers are directly addressable with Read/Write cycles
- Special port interrupt service request
- Four different interrupt vectors for the port interrupts
- 8-bit output port
- 8-bit input port
- Selectable handshaking modes

All I/O and handshake signals are routed to high speed opto-coupler (HCPL2630) to provide maximum flexibility of the voltage ranges. The typical propagation delay of each opto-coupler is 50 nsec. Each I/O channel contains a separate power supply input to provide a supply voltage for the opto-coupler. Alternately, the standard power from the VMEbus (+ 5 V) can be used to drive the opto-coupler.
Each I/O signal is available through two 64-pin I/O connectors or through the 64-pin DIN connector (P2). The SYS68K/OPIO-1 is able to operate in a 16-bit parallel mode because two of the 4 PI/T devices are on the lower data bus (D0–D7), and the other two devices are connected to the upper data bus (D8–D15). This allows a parallel transfer of 16-bit data with a common handshake.

2. The DMA Controller

Each PI/T device is connected to a request input of the four channel DMA Controller (68458-8 MHz). Each I/O channel can then be selected to operate with or without DMA control.

Features of the DMAC

- Four independent DMA channels
- Array-chained and linked-array-chained operations
- 72 registers for complete software control
- Interface lines that provide for requesting and acknowledging
- Programmable channel prioritization
- Two vectored interrupts for each channel
- Auto-request and external-request transfer mode

For easy installation of the SYS68K/OPIO-1 into a system, the board supports several bus release functions:

RWD = Release When Done
ROR = Release On Request
RAT = Relase After Time-out

The RAT function and the ROR function are software-programmable through the on-board control register. The RAT function contains eight different time-out values (6 µsec to 800 µsec) which are software-programmable. The DMA Controller can operate on the VMEbus in the following transfer modes:

- OPIO to Memory
- Memory to OPIO
- Memory to Memory

The bus request level (0–3) for the VMEbus mastership is jumper-selectable.

3. The Timer Operation

Each PI/T device contains a 24-bit timer capable of generating an interrupt. Therefore four different timer interrupts can be generated from the OPIO-1.

4. The Interrupt Structure

The PI/T devices and the DMA Controller can generate interrupts. These interrupt request signals are used as an input for the two Bus Interrupter Modules (BIM 68153). The BIM contains registers which are Read/Write accessible to define which interrupt request levels are assigned to the IRQ-inputs.

This structure allows the user to program the interrupt level and vector for all on-board interrupt sources.

5. The Addressing

The SYS68K/OPIO-1 provides a flexible address and address modifier decoding logic. The access address and the address modifier codes are jumper-selectable (A24 or A16 mode). Therefore, both standard and short I/O addressing modes are supported.

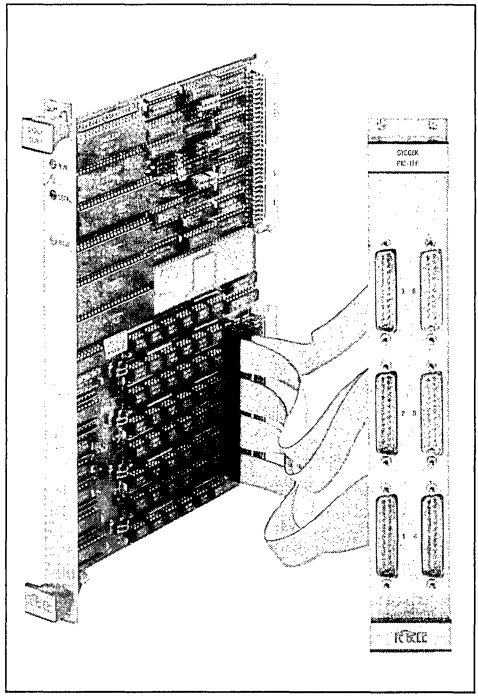
For DMA transfers on the VMEbus, address modifer codes (A24, A16) are user-programmable in user register.

6. Front Panel with Six I/O Connectors

The SYS68K/PIO-1FP is a double-width (12HE/8TE) front panel, providing six 25-pin D-sub male connectors, each with flat cable which plug into the 64-pin headers on the SYS68K/OPIO-1.

The connectors 1, 2, 3 and 4 are configurable for bi-directional operation. Connectors 5 and 6 are each configurable for either in- or output. The assignment of the connector to the I/O channels is user-selectable, as well as the individual configuration of the bi-directional I/O ports or separate input and output ports.

SYS68K/PIO-1FP

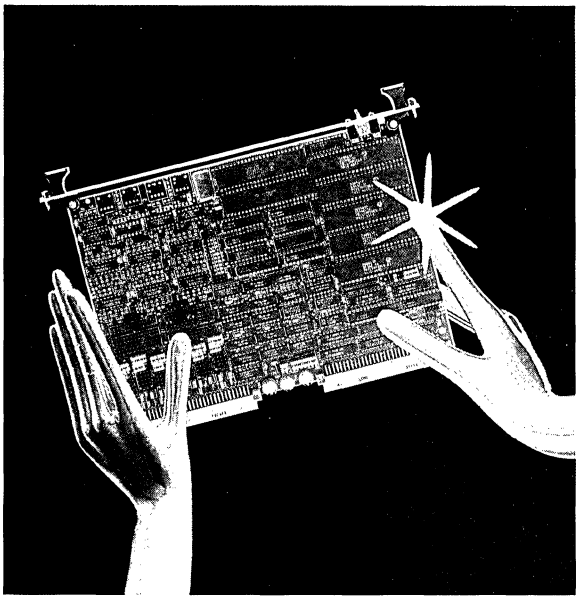


Specifications

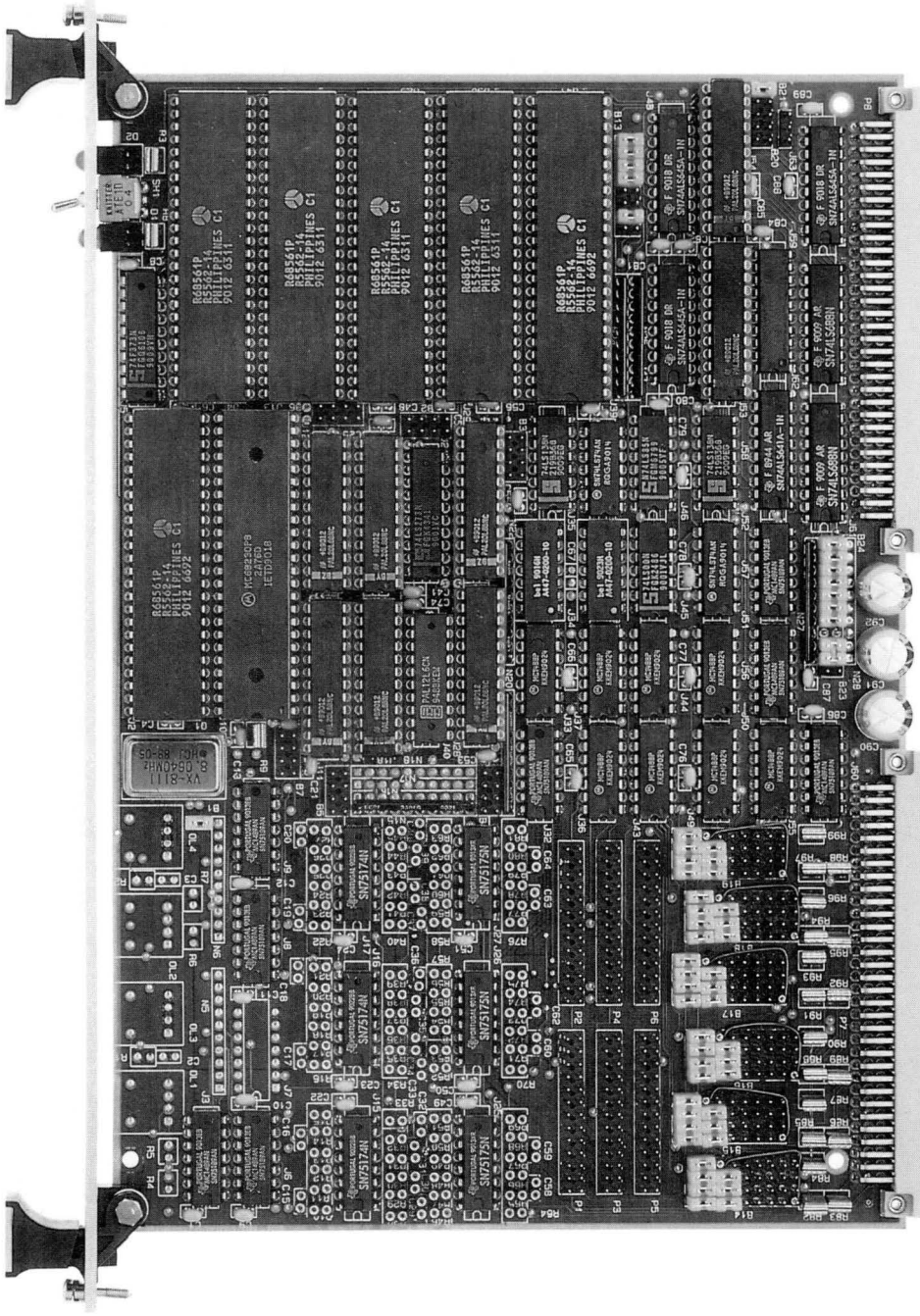
Interface	4 opto-isolated TTL level parallel I/O channels
Channel isolation	1000 V
Channel configuraqtion	Input: 8 lines data 2 lines handshake Output: 8 lines data 2 lines handshake Direction control Internal or external GND and VCC (+ 5 V)
Channel level	TTL compatible voltage Receiver sinks 8 mA for logic 0.
Devices	4 Parallel Interface/Timer (68230) 1 Direct Memory Access Controller (68450) 2 Bus Interrupter Module (68153) 48 opto-couplers (HCPL2630)
Interrupt	Individually software-programmable interrupt request level for 8 interrupts 28 different interrupt vectors possible
DMA	Dual cycle transfers as bus master Each I/O channel can request the DMAC
VMEbus	A24, A16 : D16 Jumper-selectable board base address Address modifier decoding
Address space	512 byte
Power requirements	+ 5 V/2.5 A (typ) + 5 V/3 A (max)
Operating temperature with forced air cooling Storage temperature Relative humidity (non-condensing)	0 to + 50 °C – 50 to + 90 °C 5 to 95 %
Board dimensions	234 × 160 mm : 9.2 × 6.3 in

Ordering Information

SYS68K/OPIO-1 Part No. 310011	Opto-isolated parallel I/O board. Documentation included.
SYS68K/PIO-1FP Part No. 310012	Front panel for the parallel I/O signals.
SYS68K/OPIO-1/UM Part No. 800029	User's manual for the SYS68K/OPIO-1 board.



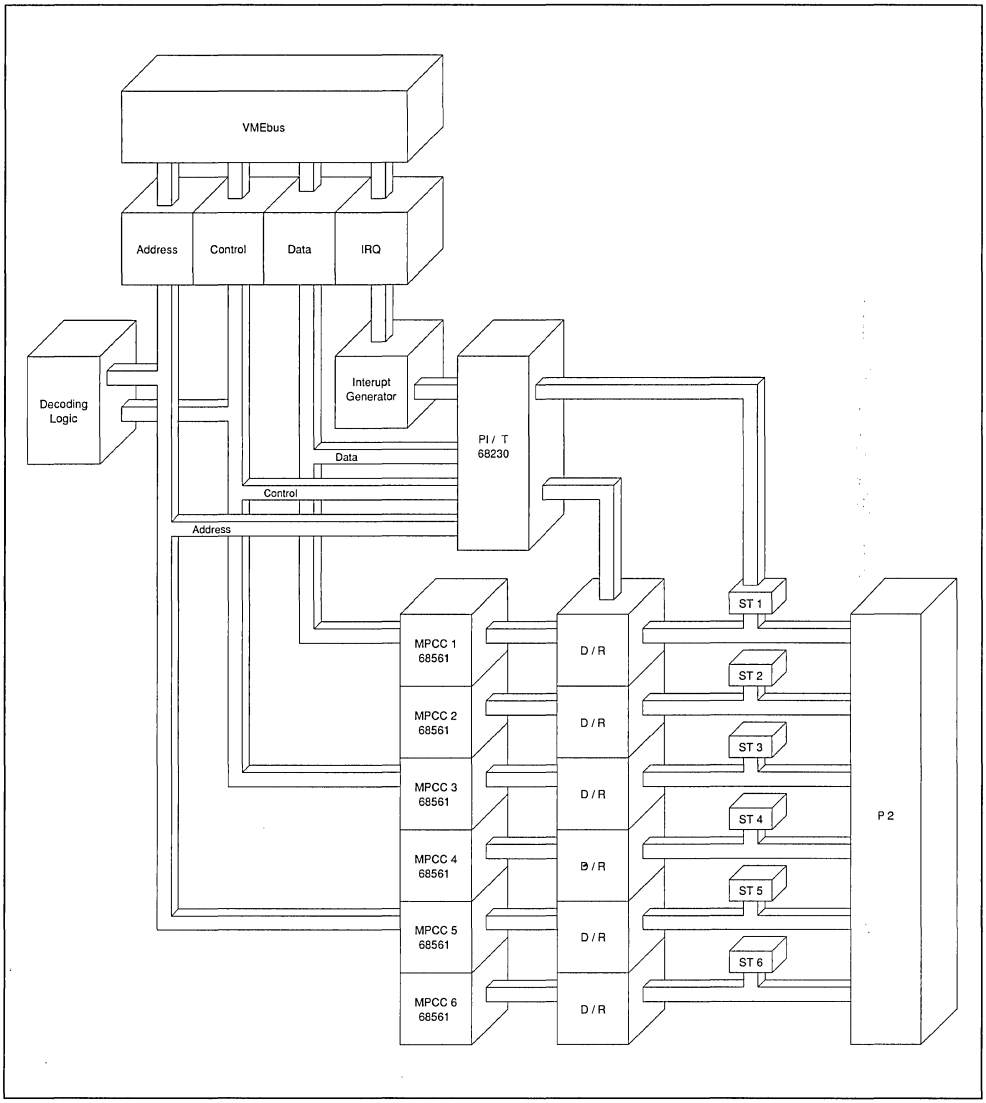
System 68000 VME
SYS68K/SIO-2
Multi-Protocol Serial I/O Controller Board



General Description

The SYS68K/SIO-2 board contains six serial I/O channels based on six Multi-Protocol Communications Controllers (MPCC) supporting asynchronous or synchronous protocols and an 8-character receiver and transmitter buffer register. Each MPCC is able to generate an interrupt to the VMEbus (levels 1–7) and to drive three different interrupt vectors.
The interface to the communication equipment is RS232- or RS422-compatible (user-selectable).

Block Diagram of the SYS68K/SIO-2



Features of the SYS68K/SIO-2

- 6 serial I/O channels
- Fully IEEE 1014, VMEbus compatible
- Multi-Protocol Communications Controller (68561) for each channel allows:
  - Asynchronous/synchronous receiver/transmitter functions
  - Full/half duplex, auto-echo and local loopback modes
- The 68561 supports the following protocols:
  - IBM binary synchronous communications in ASCII or EBCDIC format
  - Character Oriented Protocols (COP) BSC, DDCMP, X3.28, X.21, ISO IS1745, ECMA 16, etc.
  - Synchronous Bit-Oriented Protocols (BOP) SDLC, HDLC/ADCCP, X.25, etc.
  - Asynchronous or synchronous mode
- Modem handshake interface
- Selectable parity (enable odd, even) and CRC (control field enable, CRC-16, CCITT, V.41, VRC/LRC)
- 22 directly addressable registers for flexible option selection, complete status reporting and data transfer
- 8-character receiver and transmitter buffer register
- Three separate programmable and maskable interrupt vector numbers for the receiver, transmitter, and serial interface
- Software-programmable baud rate from 110 to 38400 baud
- 8- and 16-bit data bus
- A24 and A16 decoding
- Free configurable I/O interface signal assignment through wire wrap areas for each channel
  5 drivers (RS232-compatible)
  6 receivers (RS232-compatible)
  2 drivers (RS422-compatible)
  2 receivers (RS422-compatible)
- All I/O signals are routed to the P2 connector
- Local PI/T for interface type selection of the MPCCs during initialization
- User-selectable access address and address modifier code of the 6 MPCCs and the PI/T
- RUN/LOCAL mode indicated by LEDs

Each MPCC is able to use the listed protocols. The internal 8-character receiver/transmitter buffer register (FIFO) and the three separate maskable interrupt vector numbers (transmitter, receiver, or handshake interface) reduce overall software overhead.

All the MPCCs on the board operate completely asnychronous to the VMEbus and respond to a VMEbus master on a user-selectable access address and address modifier code.

The RUN/LOCAL switch isolates the board from the VMEbus. This mode is indicated by two LEDs on the front panel.

Each serial I/O channel contains RS232/RS422 driver (5/2) and receiver (6/2) circuits. Each of the I/O signals is connected to the 26-pin male connector installed on the board to allow the connection of a flat cable. The SYS68K/SIO-1FP offers the connection of six 25-pin D-sub connectors on a standard front panel as shown on the next page.

In addition to the 26-pin male connectors, all I/O signals are available on a wire wrap area where the user can select the I/O signals to be connected to the P2 connector.

The I/O signal assignment on the P2 connector is compatible to the I/O signal assignment of the SYS68K/ISIO-2 boards.

SYS68K/SIO-1FP Description

The SYS68K/SIO-1FP is a double-width front panel containing six 25-pin D-sub connectors with flat wire cables to be used in conjunction with the SYS68K/SIO-2 multi-protocol serial I/O controller board.

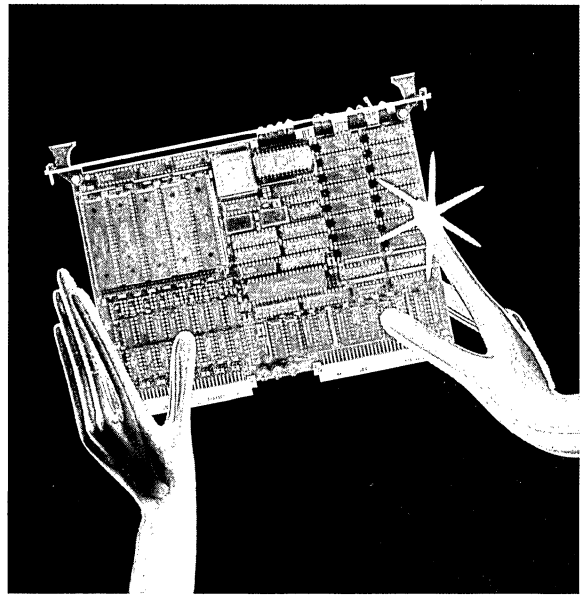
The SYS68K/SIO-1FP allows easy plug-in of the serial I/O ports relieving the user from individual wiring problems in systems applications.

Specifications

Interface	6 independent serial I/O channels RS232- or RS422-compatible (jumper-selectable)
Communications controller	6 Multi-Protocol Communications Controller (68561 MPCC)
Protocols	IBM BSC:ASCII EBCDIC COP:BSC,DDCMP X3.28,X.21 BOP:SDLC HDLC/ADCCP X.25 Asynchronous and synchronous modes Full/half duplex, auto-echo and local loop-back modes Software-programmable baud rate (110–38400 baud) Maximum synchronous data rate: 2 Mbit/s (RS422)
Interrupt	Free selectable interrupt request level (1 to 7) in common for six I/O channels. 18 different auto-interrupt vectors are programmable (3 per channel)
VMEbus interface	A24, A16 : D8, D16. Jumper-selectable board base address and address modifier decoding
Power requirements	+ 5 V/2.1 A (typ), 2.5 A (max) + 12 V/0.1 A (typ), 0.3 A (max) – 12 V/0.1 A (typ), 0.3 A (max)
Operating temperature with forced air cooling Storage temperature Relative humidity	0 to + 50 °C – 50 to + 90 °C (non-operating) 5 to 95 % (non-condensing)
Board dimensions	234 × 160 mm : 9.2 × 6.3 in

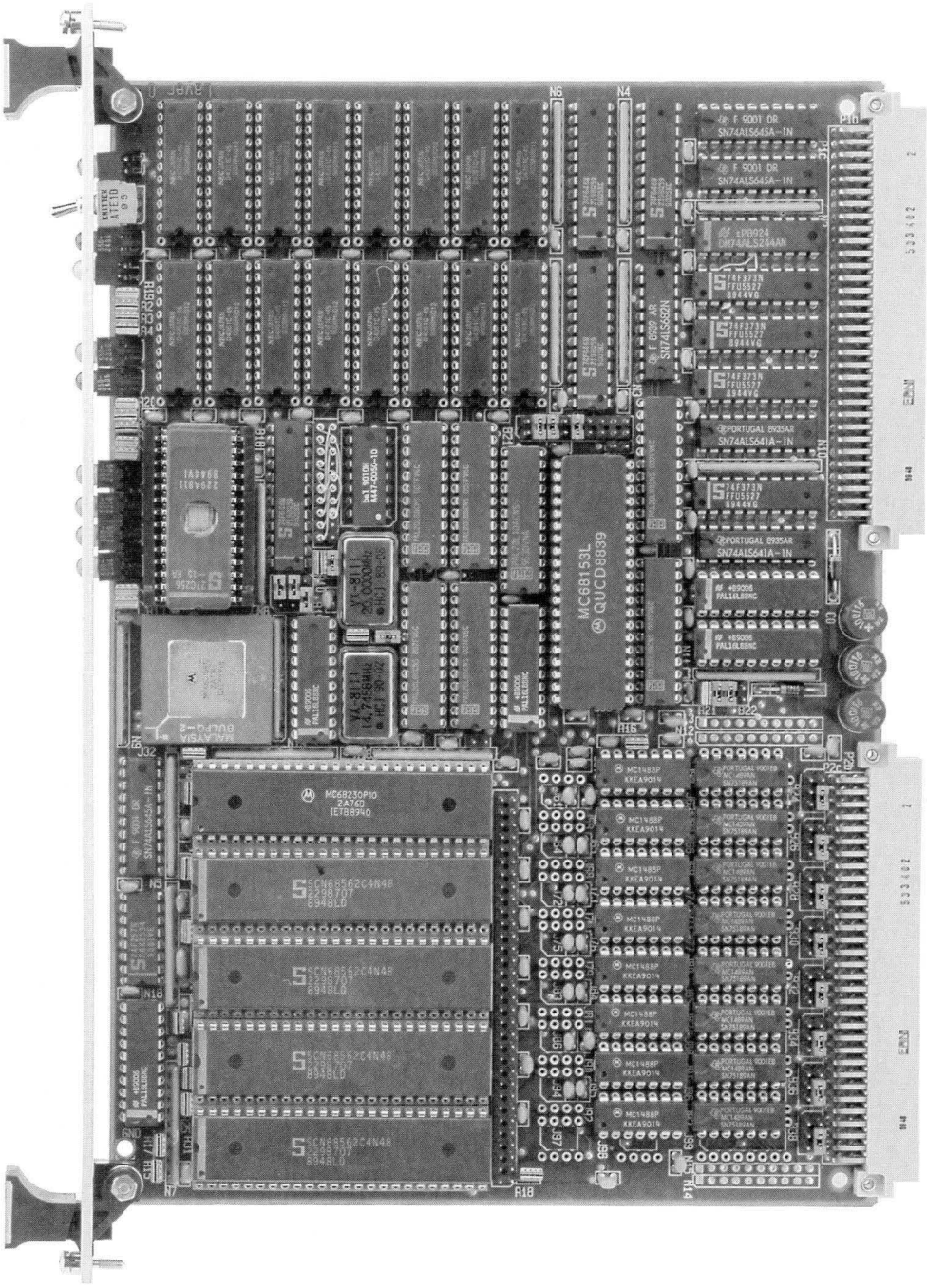
Ordering Information

SYS68K/SIO-2 Part No. 310004	6 channel Multi-Protocol Serial I/O Controller board. Documentation included.
SYS68K/SIO-1FP Part No. 310001	Front panel with six 25-pin D-sub connectors
SYS68K/SIO-2/UM Part No. 800129	User's manual for the SYS68K/SIO-2 board



System 68000 VME
SYS68K/ISIO-2

Intelligent Serial I/O Controller Board


MC68153L
QUCD8839
MC6B230P10
SN74ALS645A-1N
SN74ALS641A-1N
SN74ALS624AN
SN74ALS682N
SCN68562C4N48
PAL16L8BNC
PORTUGAL B935AR
74F373N
FTUS527
8944VG

General Description

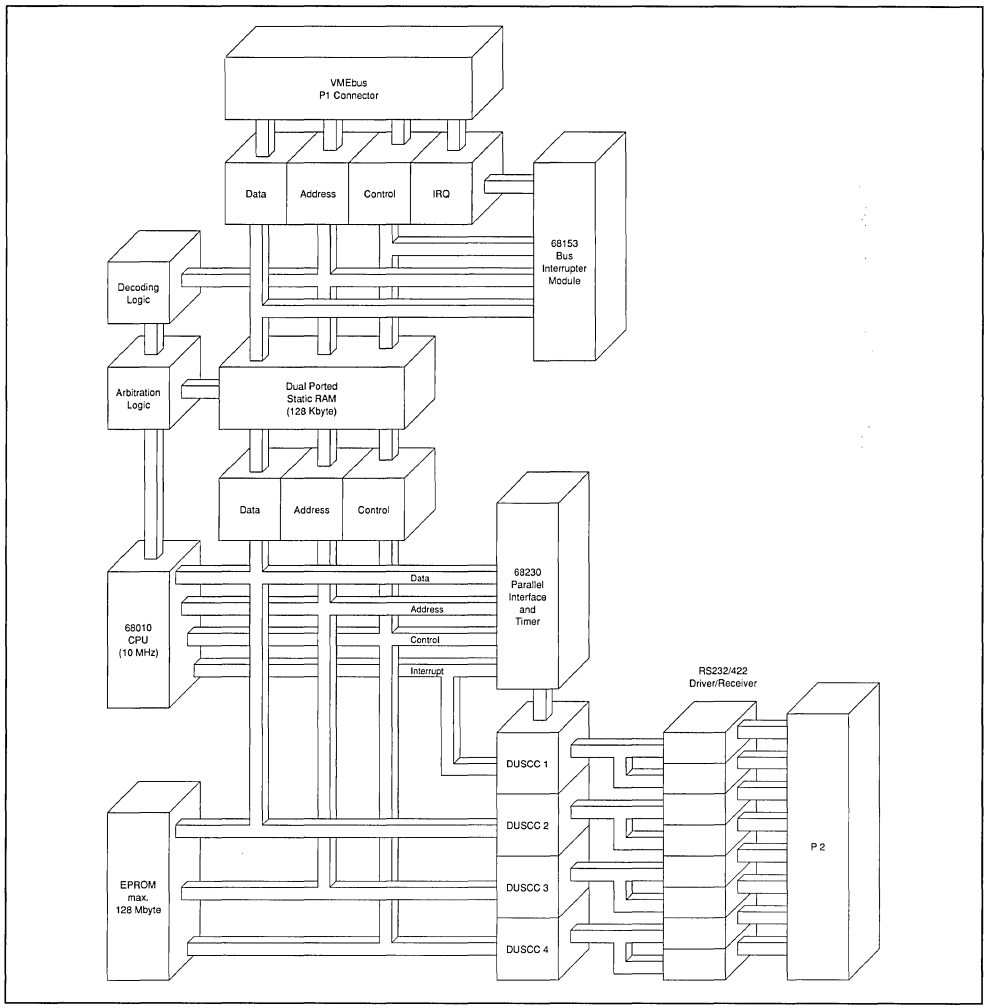
The SYS68K/ISIO-2 is a high performance intelligent serial I/O board, providing local intelligence with a 68010 CPU and eight serial I/O channels configurable for RS232 or RS422 communication standards.

128 Kbyte Dual Ported RAM (DPR) is used to store commands and data. Highest throughput is guaranteed by using a 10 MHz 68010 CPU running constantly without the insertion of wait states out of the 128 Kbyte EPROM area or out of the DPR (independent from VMEbus accesses). Four Dual Universal Serial Communication Controllers DUSCC 68562 are used to interface to as many as eight serial channels.

To enable easy system design, all I/O signals are routed to the P2 connector which results in eight I/O signals per channel being supported.

The ISIO-2 contains a VMEbus, IEEE 1014-compatible interface to communicate with host CPUs via its 128 Kbyte DPR. The access address and the address modifier code are jumper-selectable.

Block Diagram of the SYS68K/ISIO-2



A Bus Interrupter Module (BIM 68153) is installed on the board to support fully asynchronous operation with the four different software-programmable interrupt request channels.
The firmware of the ISIO-2 handles all activities to/from the serial I/O channels including code conversion, search and copy functions.

Features of the SYS68K/ISIO-2

- 68010 CPU for local control (10 MHz)
- Dual-ported 128 Kbyte zero wait state RAM between the VMEbus and the local CPU
- Eight serial I/O channels built with four 68562 DUSCC chips. Independent software-programmable baud rate for each channel from 50 to 38400 baud
- All serial I/O channels independently configurable to either RS232 or RS422
- All I/O signals available on P2 connector
- Four different interrupt request signals to the VMEbus. Each channel contains a software-programmable IRQ-level (1 to 7) and vector
- Local parallel interface for controlling and monitoring all board functions
- VMEbus IEEE 1014-compatible interface (A24 : D8, D16)
- Local watchdog timer controlling correct functions of on-board hard- and software
- Status and control LEDs for monitoring of local activities
- High level handling firmware for communication, self-test and control

1. The Hardware Functions

The local CPU interprets the commands and initialization parameters within the 128 Kbyte DPR. Constant runtimes are guaranteed through the special hardware logic providing zero wait state operation from the DPR, independent from the accesses between the VMEbus and the DPR.
The ISIO-2 contains self-test functions as well as a hardware watchdog timer which monitors the activities of the 10 MHz 68010 CPU. User supplied programs can be loaded into the DPR and executed by the local CPU to adapt and extend board functionality.
A time scheduler and a prioritization mechanism are installed in the firmware to adapt the ISIO-2 to a wide variety of applications such as terminal controller, print spooler, etc.

The local CPU controls all eight serial I/O channels via local interrupts and communicates with the host CPU via the DPR or via interrupt requests to the VMEbus generated by a Bus Interrupter Module.
The I/O signals to be supported through the DUSCC chips are jumper-selectable which allows each channel to be adapted individually to suit the application need.

1.1 The Local 68010 CPU

A 10 MHz 68010 CPU is installed on the ISIO-2 to control the data traffic between the serial I/O channels and the VMEbus host CPU(s).
Two EPROMs with a maximum capacity of 128 Kbyte are installed on the ISIO-2 to contain the handling firmware. Constant zero wait state operation from the EPROM guarantees maximum CPU throughput and a fixed program runtime.
The 128 Kbyte of dual-ported RAM is also accessible without the insertion of wait states by using a CPU clock synchronized arbitration mechanism. The accesses from the CPU to the DPR are not delayed if a VMEbus access is pending or being executed.
A local timer, installed in the Parallel Interface/Timer device (68230-PI/T), is used to interrupt the CPU for task scheduling, command interpretation and execution.
The CPU and all I/O devices can be reset via the SYSRESET* signal of the VMEbus or by accessing a dedicated location within the DPR reserved for this function.

1.2 The Serial I/O Interfaces

The ISIO-2 contains four Dual Universal Serial Communication Controllers (DUSCC 68562). Each DUSCC chip provides the following features:

- Dual full duplex synchronous/asynchronous receiver and transmitter
- Multi-protocol operation consisting of:
  BOP*: HDLC/ADCCP, SDLC, SDLC Loop
  COP*: BISYNC, DDCMP, X.21
  ASYNC: 5 to 8 bit plus optional parity
- 4 character receiver and transmitter FIFOs

* Note: Standard firmware supports asynchronous and chip level synchronous communication only.

- Programmable baud rate for each receiver and transmitter
  - 50 to 38400 baud (asynchronous)
  - Digital phase locked loop
  - User-programmable counter/timer
- Programmable channel modes
  - full/half duplex
  - auto echo
  - local loopback
- Modem control signals for each channel RTS, CTS, DCD
  CTS and DCD programmable auto enables for receiver (RX) and transmitter (TX)
  Programmable interrupt on change of CTS or DCD

A set of eight I/O signals is supported on each channel providing maximum flexibility.
The ISIO-2 board offers two different interface types for each channel. The board is equipped by default with RS232 driver and receiver circuits supporting seven I/O signals as listed in paragraph 1.2.1.
Each of the eight channels can be reconfigured to meet the RS422 standard. Both of the driver and receiver circuits reside on the sockets and can easily be removed or exchanged. All combinations of RS232 or RS422 interfaces are possible dependent on application needs. Resistors networks can be installed in the RS422 mode do adapt the various cable length. A detailed description of the RS422 interface is shown in paragraph 1.2.2.

1.2.1 The RS232 Interface

All RS232-compatible driver and receiver circuitries are installed on the ISIO-2.
The I/O signal assignment on the P2 connector is organized in eight groups of eight signals. An example is shown in the following table:

Signal	Input	Output	P2-Pin	9-pin D-sub Connector	Description
DCD	x		c1	1	Data Carrier Detect
RXD	x		c2	2	Receive Data
TXD		x	c3	3	Transmit Data
DTR		x	c4	4	Data Terminal Ready
GND			a4	5	Signal GND
DSR	x	x	a1	6	Data Set Ready
RTS		x	a2	7	Request to Send
CTS			a3	8	Clear to Send
–		–	–	9	Not Connected

1.2.2 The RS422 Interface

By default the RS232 driver and receiver circuits are installed on the ISIO-2 board. Each of the 8 I/O channels can be reconfigured to the RS422 Standard by using the other supplied interface chips.
All RS422 signals can be adapted to various cable length termination requirements via socketed resistors and capacitors.
The I/O signal assignments to the P2 connector is organized in eight groups of four signals. An example is shown in the following table:

Signal	Input	Output	P2-Pin	9-Pin D-sub Connector	Description
TXD-A		x	a1	6	Transmit
TXD-B		x	c1	1	Data
RTS-A		x	a2	7	Request to
RTS-B		x	c2	2	send
CTS-A	x		a3	8	Clear to
CTS-B	x		c3	3	send
RXD-A	x		a4	5	Receive
RXD-B	x		c4	4	Data

1.3 The PI/T 68230

A 68230 Parallel Interface and Timer chip is installed on the ISIO-2 to control and display the status of all on-board activities. The PI/T is also used to issue and monitor the interrupt request lines to the Bus Interrupter Module (BIM), which initiates the interrupts to the VMEbus (under control of the host CPU).

One handshake pin is used to interrupt the local CPU if the host CPU accesses a defined location within the DPR. One output signal is used to activate the SYSFAIL* signal to the VMEbus if an on-board error has been detected or if the board initializes the DPR after RESET or power-up.

The timer, also included in the PI/T, is the time base for the on-board handling firmware and the scheduler for the macro commands.

A watchdog timer, for processor control, is installed on the board to detect software or hardware errors independent from the on-board CPU. For this purpose, one output of the PI/T is used to retrigger the watchdog timer within defined time frames.

It the on-board CPU does not work properly, or if the hardware does not work correctly, the timer will not be retriggered, and the SYSFAIL* signal of the VMEbus will be activated. The host CPU can then initiate a software controlled RESET for the ISIO-2, or start other maintenance activities.

1.4 The Dual Ported RAM

128 Kbyte of Dual Ported Static RAM with 45 nsec access time is installed on the ISIO-2 to service all applications requiring fast operations.

The local 68010 CPU runs without the insertion of wait states out of the DPR because the CPU clock synchronized arbitration logic and a fully buffered and latched VMEbus interface is installed on the ISIO-2. A VMEbus cycle is serviced and completed between two CPU access cycles. On VMEbus Read cycles, the data pattern is latched, and the internal cycle of the DPR is aborted while the VMEbus cycle is decoupled.

A partition of the DPR is reserved for the local CPU for vector storage and temporary buffers. This partition is used from the VMEbus side for programming the BIM and initiating an interrupt, which will be handled by the on-board CPU, or for driving a local reset.

The access address and the address modifier code(s) are jumper-selectable in 128 Kbyte increments within the standard address range (A24 : D8, D16).

1.5 The VMEbus Interface

A full VMEbus IEEE 1014-compatible interface is installed on the ISIO-2 to allow an access to the DPR and the Bus Interrupter Module.

The 16-bit data width (D16, D8) of the DPR and the decoding of the standard address range (A24) allows easy installation in all VMEbus environments. During power-up and after a reset has been executed from the local CPU, the ISIO-2 drives the VMEbus signal SYSFAIL* active to signal each board in the VMEbus environment that the board is not ready or has detected a malfunction.

A reset for the local CPU can be initiated by accessing a dedicated address within the 128 Kbyte boundary of the DPR. All local devices as well as the CPU will be reset through this access.

An interrupt to the local CPU can be forced by accessing another location within the DPR, signaling the on-board processor that a command has been given, or that an exception has to be taken.

1.6 The Bus Interrupter Module

To allow fully asynchronous operation, the ISIO-2 contains a Bus Interrupter Module – BIM 68153 – providing 4 individually programmable interrupt channels. Each channel is able to force an interrupt request to the VMEbus. For each channel, the IRQ level (1 to 7) as well as the interrupt vector is fully software-programmable.

The local CPU asserts a request to the BIM and the host CPU may program the interrupt vector and level at its discretion. This allows dynamic change of the interrupt level and vector in multi-processor environments.

Memory Layout of the Dual Ported RAM

Offset to Base Address	Description
$000000–$0007FF	BIM providing 4 programmable interrupt levels and vectors on VME.
$000800–$000FFF	Status register, read only.
$001000–$0017FF	Local interrupt, reading this address generates a local interrupt.
$001800–$001FFF	Local reset, reading this address generates a local reset.
$002000–$007FFF	This part of the dual ported RAM is used by the local firmware and must not be modified from the VMEbus.
$008000–$0080FF	16 command channels to program the 8 input and 8 output channels.
$008100–$01FFFF	16 data arrays for the I/O channels.

2. The Firmware

The SYS68K/ISIO-2 intelligent serial I/O board operates under the control of the local handling firmware which is supplied – as standard – with the board free of charge. This EPROM resident firmware package executes the commands which are placed in the dual ported RAM and returns control and error messages. All commands are executed under the supervision of a local Real Time Kernel which coordinates the eight input and eight output tasks.

Each of the 16 command blocks are used to pass commands and parameters to the corresponding channel. When the command is executed an interrupt can be generated. The return value containing end codes and parameters is placed in the command block.

The handling firmware is devided into different modules which are:

- Initialization commands
- Input commands
- Output commands
- Copy commands
- Special commands

The source code for the firmware is available for adapation to specific application needs.

3. The Optional Front Panel

A front panel consisting of eight 9-pin D-sub connectors is optionally available to allow direct connection to the eight serial I/O channels of the ISIO-2 board.

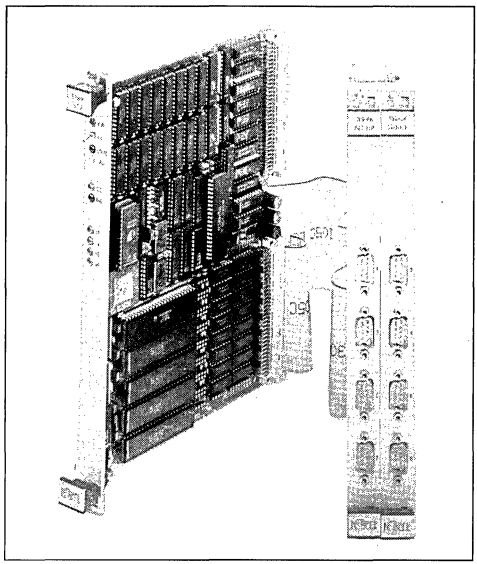
The pin-out for each of the eight D-sub connectors is configurable on the ISIO-2 board.

The following figure shows the ISIO-1FP and the interconnection to the ISIO-2 board in detail.

Each of the seven I/O signals is connected to a jumperfield on the ISIO-1FP board to allow adaptation of the I/O signals to the various applications.

In addition, there is a half-height back panel for the TARGET 32 chassis available which provides eight 9-pin D-sub connectors routed to the back of the TARGET 32.

SYS68K/ISIO-1FP



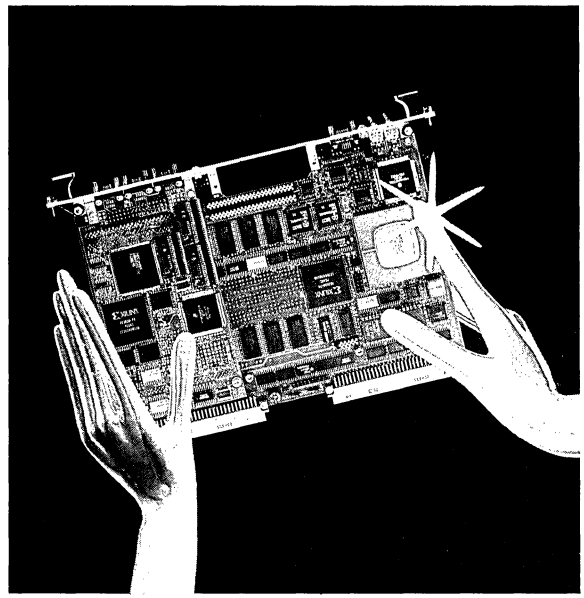
Specifications

Local CPU	68010 with 10 MHz clock frequency
EPROM	128 Kbyte maximum capacity Zero wait state operation
Dual Ported RAM	128 Kbyte capacity using static RAMs Zero wait state operation from local CPU 330 nsec best case VMEbus access time 430 nsec average VMEbus access time 560 nsec worst case VMEbus access time
Serial I/O interfaces	eight channels seven I/O signals per channel (RS232-compatible) or eight I/O signals per channel (RS422-compatible) All I/O signals available on P2 connector
Serial I/O controller	68562 DUSCC providing Software-programmable baud rate (50 to 38400 Baud) HDLC and SDLC protocols* Automatic hardware handshake programmable
VMEbus interface	A24: D8, D16 mode Four IQRs with software-programmable level (1 to 7) and vector Access address jumper-selectable in 128 Kbyte increments SYSFAIL* supported
Firmware	In EPROM with macro commands for all I/O channels installed
Power requirements	+ 5 V : 5.4 A (max) + 12 V : 0.6 A (max) – 12 V : 0.6 A (max)
Operating temperature with forced air cooling Storage temperature Relative humidity	0 to 50 °C – 50 to + 85 °C 5 to 90 % (non-condensing)
Board dimensions	234 mm × 160 mm : 9.2 × 6.3 in

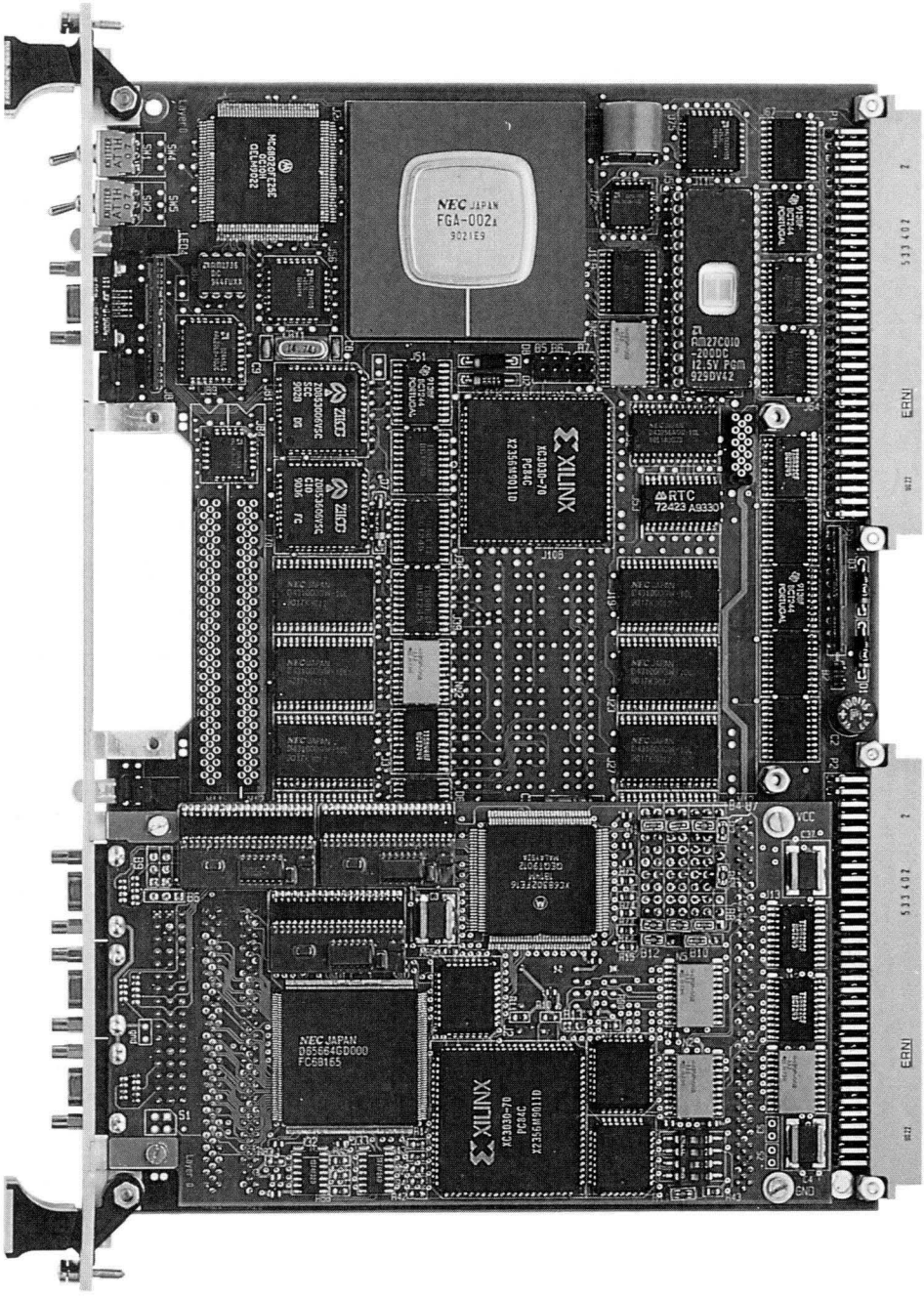
* Not supported in standard firmware

Ordering Information

SYS68K/ISIO-2 Part No. 310031	Eight channel intelligent serial I/O controller board (RS232- or RS422-configurable). Documentation and firmware included.
SYS68K/ISIO-1FP Part No. 310034	Front panel for the ISIO-2 board providing eight 9-pin D-sub connectors.
SYS68K/ISIO-2/UM Part No. 800110	User's manual for the ISIO-2.
SYS68K/ISIO-2SC Part No. 310033	Source code of the local handling firmware.



System 68000 VME
SYS68K/ICC-1
Intelligent Communications Controller

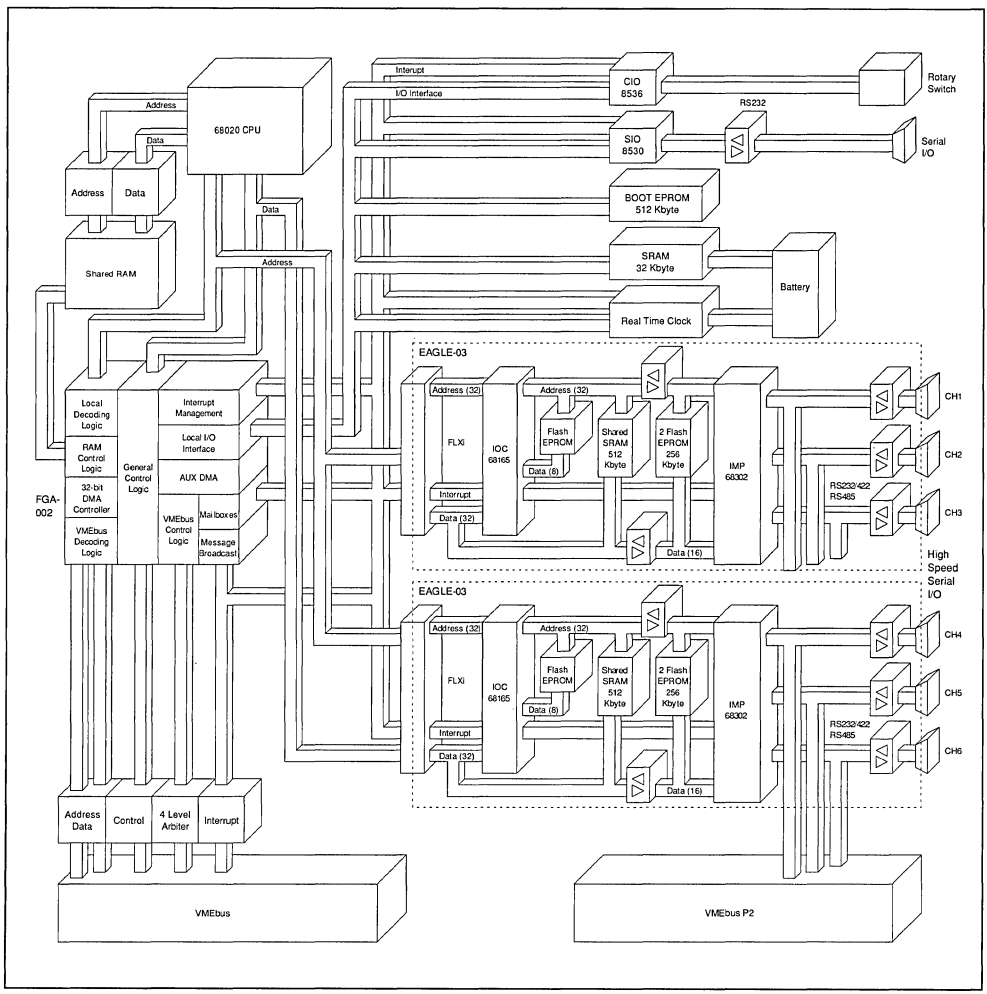

NEC JAPAN
FGA-002
XILINX
RTC
72423 A9330
NEC JAPAN
D656646D000
FC88165
XILINX
ERNI

General Description

The SYS68K/ICC-1 is a 68020 based intelligent serial communications controller for the VMEbus, providing up to six high speed serial I/O channels supporting protocols such as X.25. The board fully incorporates FORCE COMPUTERS' EAGLE module concept, which ensures high performance and flexible I/O. The SYS68K/ICC-1 is offered with either one or two EAGLE-03 modules installed, each providing three high speed serial I/O channels. The EAGLE I/O subsystem modules are connected to the base board via the FORCE Local Expansion interface (FLXi).

The base board provides a 68020 CPU for on-board intelligence and performance. A 32-bit DMA controller, two Message Broadcast channels and eight multi-processing mailboxes are provided by the FORCE Gate Array FGA-002. The base board is offered in two configurations: one with 2 Mbyte of shared SRAM and one with 4 Mbyte of shared DRAM. The shared main

Block Diagram of the SYS68K/ICC-1



memory area is accessible from the local CPU, the DMA controller, the EAGLE modules and the VMEbus. In addition to the high speed serial I/O channels on the EAGLE modules, a front panel serial I/O port serves as a debugging port. Further features include 32 Kbyte SRAM and a Real Time Clock, both with on-board battery back-up.
Each EAGLE-03 module offers three high speed serial I/O channels built around a 68302 Integrated Multi-Protocol Processor, an additional 512 Kbyte shared SRAM and 256 Kbyte of FLASH EPROM.
With two EAGLE-03's installed, the ICC-1 provides a total of six high speed serial I/O channels which can be configured for synchronous and/or asynchronous communication. All six channels are routed to the front panel of the board and can be set up as RS232, RS449, RS422 or RS485 via socketed hybrid modules. Three of the six channels are routed additionally to the VMEbus P2 connector.
To allow concurrent high speed full-duplex operation of all six channels, the board offers a total of three CPUs (one 68020, and a 68000 within each of the 68302's) and fifteen independent DMA controllers (one in the FGA-002, and fourteen in the two 68302's).
The SYS68K/ICC-1 is built in a unique Multi-level Parallel Architecture, which fully supports the implementation of complex protocols required in applications such as X.25, ISDN etc. The architecture allows the execution of all layers of the OSI communication model on different processors on one single slot VMEbus board, thus enabling multi-channel high speed serial transfers and multiple layer protocol handling to be performed locally on the Intelligent Communications Controller.
The implementation of several independent parallel data paths and the use of multiple DMA controllers ensure that pure data movement tasks can be split from protocol handling and data processing tasks.
The firmware installed on the SYS68K/ICC-1 is based on the VMEPROM Real Time Kernel/ Monitor and supports low-level debugging as well as asynchronous communication via the serial ports.
A software support package for the X.25 protocol is optionally available.

Features of the SYS68K/ICC-1

- CPU

A 68020 with 25.0 MHz clock frequency is used as the main CPU.

- Main memory

The main memory on the base board consists of 2 Mbyte of shared SRAM (battery back-up via +5V STDBY line of the VMEbus), supporting zero wait state operation of the CPU, or 4 Mbyte of shared DRAM. The main memory is accessible from the local CPU, the DMA controllers, the VMEbus and the 68302 through the FLXi. The start and end access addresses are software-programmable in 4 Kbyte increments via the FGA-002. In addition, a write protection can be enabled by software.

- DMA controller

A 32-bit high speed DMA controller for data transfers to/from the shared RAM, to/from VMEbus memory and to/from the EAGLE modules off-loads the 68020 CPU from pure data transfer tasks. The DMA controller is installed in the FGA-002. It runs entirely independently from the local CPU and is able to perform data transfers (e.g. across the VMEbus, without affecting the CPU's performance).

- The FLXi

Two FORCE Local eXpansion interfaces (FLXi) are placed on the base board to enable one or two EAGLE modules to be installed. The FLXi provides the following interfaces from the base board to the EAGLE module:

- 32-bit data and address bus for standard microprocessor and DMA access using 68020 compatible bus timing and dynamic bus sizing.
- Direct connection of the 64 VMEbus P2 user I/O pins to one of the two EAGLE modules (EAGLE interface 1).

The FLXi is a connector interface which allows the installation of an EAGLE module. The interface and the EAGLE modules are designed to allow a complete SYS68K/ICC-1 solution to occupy only one VMEbus slot. When installed, the EAGLE module's front panel becomes part of the base board's front panel.
The FLXi allows the EAGLE module to access

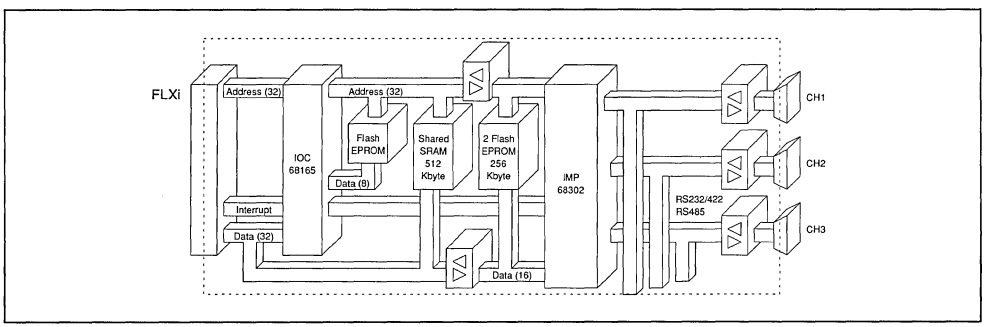
the resources of the base board in addition to the 68020 on the base board being able to access the resources on the EAGLE module.

- EAGLE-03

The SYS68K/ICC-1 is offered with either one or two EAGLE-03 modules installed. Each EAGLE-03 module offers:

- 68302 Integrated Multi-Protocol Processor, combining
  - a 68000 CPU core,
  - a System Integration Block with an independent DMA controller and a 1152 byte dual-port on-chip RAM,
  - a Communications Processor with a RISC main controller, three independent full-duplex Serial Communications Controllers and six serial DMA channels. The Communications Processor supports various protocols such as HDLC/SDLC, UART, BISYNC, DDCMP, V.110.
- High speed serial I/O channels
  Each EAGLE-03 module provides three serial channels, each supporting high data transfer rates in full duplex mode.
  The signals of the ports are routed to the front panel of the board. If the EAGLE module is installed on the EAGLE interface 1 connectors, which provide a direct connection of the 64 VMEbus P2 user I/O pins, the three serial channels are also available at the VMEbus P2 connector. The signals available at the 9-pin micro D-sub front panel connectors are driven through hybrid modules, which allow a channel by channel configuration, such as RS232, RS449, RS422 or RS485, simply by exchanging the hybrid. The signals available at the VMEbus P2 connector are unbuffered at TTL level to allow an application specific configuration.
- 512 Kbyte shared buffer SRAM
  The EAGLE module SRAM can be accessed by the 68302 via a 16-bit data path and by the 68020 CPU and the DMA controller on the base board via the FLXi 32-bit data path. This architecture allows data transfers between the base board and the EAGLE module's shared RAM with a rate of up to 10 Mbyte/sec. Local transfers on the EAGLE module between the 68302 and the shared RAM can be performed at up to 4 Mbyte/sec.
- FLASH EPROM
  The EAGLE module's system EPROM area consists of two FLASH EPROM devices which are connected to the 68302 with a 16-bit data path and provides a total capacity of 256 Kbyte. This area is intended for the installation of low level drivers and protocol software for the 68302. The FLASH EPROM technology permits an update of the software without the need for exchanging EPROM devices or removing the board from the system. The parallel architecture of the EAGLE-03 allows the 68302 to run out of its FLASH EPROM area while the base board accesses the module's shared RAM. The 32-bit DMA controller on the base board, for example, can transfer the next block of data which is to be processed by the 68302 out of the shared RAM on the base board into the buffer RAM on the EAGLE-03, while the 68302 performs a high speed transmission out of its on-chip dual-port RAM to the serial ports.

Block Diagram of the EAGLE-03



Another FLASH EPROM device contains the initialization parameters for the I/O Controller Chip (IOC-FC68165), which interfaces the EAGLE-03 to the FLXi.

- Boot EPROM

The base board EPROM (up to 512 Kbyte) resides in a 32-pin JEDEC-compatible socket and performs local booting, initialization of the I/O chips, configuration of the FGA-002 and loading of the driver software.

- 32 Kbyte SRAM

32 Kbyte SRAM with on-board battery back-up is installed on the base board of the ICC-1. This supports data storage during power-down phases for at least one year. Back-up can also be provided via the +5V STDBY line of the VMEbus.

- Real Time Clock

A software-programmable Real Time Clock (RTC-72423) with on-board battery back-up or back-up via +5V STDBY line of the VMEbus is also installed. Battery back-up ensures continued operation of the RTC for at least one year after power-down.

- Timers

A total of four independent timers is available for the user. Each timer can be used to force an interrupt to the 68020 CPU on a software-programmable IRQ-level (1 to 7).
Three 16-bit timers are located within the 85C36 Counter/Timer and Parallel I/O device (CIO), two of which can be linked to become one 32-bit timer. One 8-bit timer, installed in the gate array FGA-002, provides sixteen software-programmable source clocks and can be used as a watchdog timer.

- FORCE Message Broadcast (FMB) – two channels

The FORCE Message Broadcast (FMB) is a fast and effective mechanism to communicate with and synchronize up to 20 CPU boards in a VMEbus system in only one VMEbus write cycle. It offers a unique support feature for building multi-processing systems based on the VMEbus. All FORCE VME/PLUS boards, including the SYS68K/ICC-1, provide two fully independent message broadcast channels which are implemented within the FGA-002. Channel 0 stores 8-bit messages in an eight-stage deep FIFO, channel 1 stores one 8-bit message and can therefore be used for high priority messages.

- Eight Multi-Processor Mailboxes

The SYS68K/ICC-1 includes eight multi-processor mailboxes. Each of these allows an interrupt to be generated to the local 68020 microprocessor. The interrupt level of each multi-processor mailbox is software-programmable and an individual interrupt vector for each mailbox may be passed to the microprocessor.
This function allows the triggering of an interrupt on the SYS68K/ICC-1 from multiple masters on the VMEbus. The mailboxes are accessed via RMW access, thus allowing multiple masters on the VMEbus to share the same mailbox channel.

- Full 32-bit VMEbus master/slave interface

The VMEbus interface on the SYS68K/ICC-1 allows the board to act as both master and slave for data transfers across the VMEbus.
The following data transfer types are supported:
- A32, A24, A16:D8, D16, D32 – Master
- A32, A24:D8, D16, D32 – Slave
- UAT, RMW, ADO

The VMEbus interface also provides all the features of a slot 1 VMEbus card, which allows the board to be used in a VMEbus system without any additional System Controller or host CPU board:
- Four Level VMEbus Arbiter
  A four level arbiter with round robin and prioritized round robin arbitration modes allows the SYS68K/ICC-1 to act as the system controller in a multi-master VMEbus system.
- VMEbus Requester
  The following bus release modes are supported:
  RWD = Release When Done
  ROR = Release On Request
  RBCLR = Release On Bus Clear
  ROACF= Release on ACFAIL*

  Each of the listed modes is software-programmable through the FGA-002 gate array. The

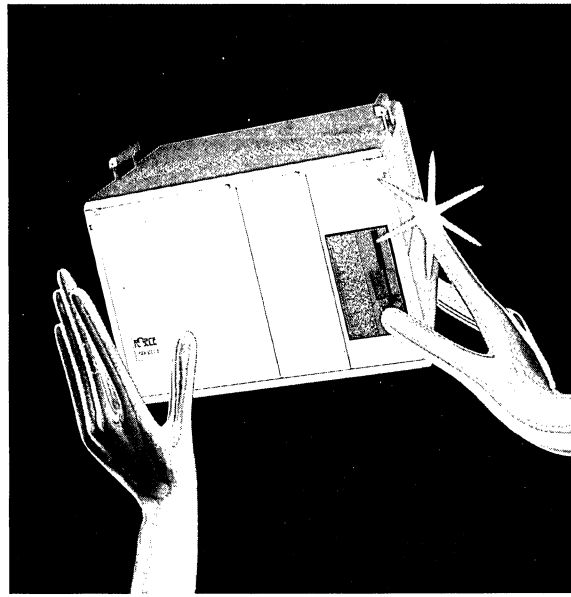
bus request level of the SYS68K/ICC-1 is jumper-selectable (BR0–3*).

- VMEbus interrupt handler (IH 1–7)
  The FGA-002 gate array installed on the SYS68K/ICC-1 handles all local and VMEbus interrupts. The gate array can be programmed by the user to prioritize interrupts from any source and then to interrupt the 68020 microprocessor on any interrupt level (1 to 7). The gate array supplies the vector, or initiates an interrupt vector fetch from the I/O device or from the VMEbus, depending on the programmed configuration of the FGA-002. This process is fully under the control of the application.
- VMEbus interrupter (IR 1-7)
  The SYS68K/ICC-1 supports the interrupter function for all seven VMEbus interrupt levels. Separate interrupt channels with unique interrupt vectors are assigned to the seven VMEbus IRQs. The interrupt vectors are software-programmable.
- IACK Daisy Chain Driver
- Support for ACFAIL*, SYSFAIL* and SYSRESET*
- SYSCLK driver
- Bus time-out counters for local and VMEbus access (15 µsec)

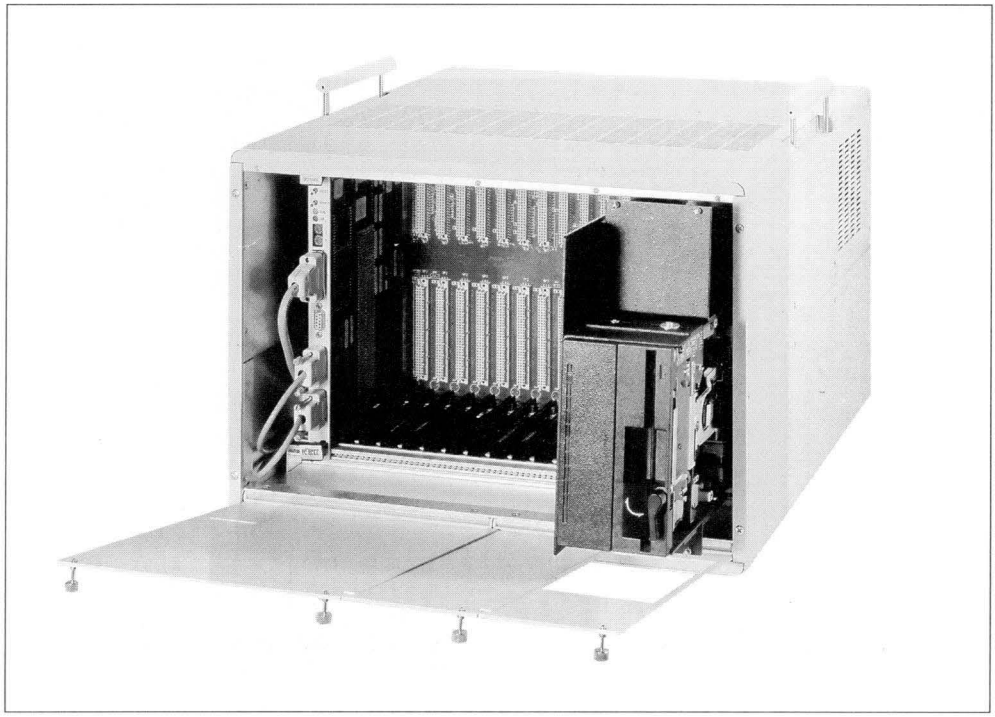
Further Details

The SYS68K/ICC-1 will become available by the end of Q1/1991. For further information on the features of the SYS68K/ICC-1 and software support, please contact your nearest FORCE sales office.

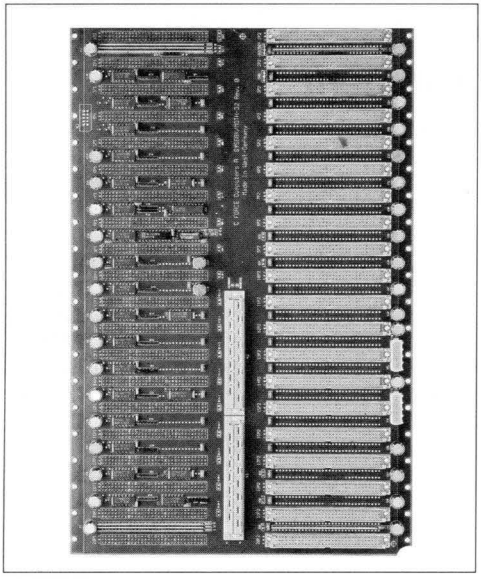
Accessories



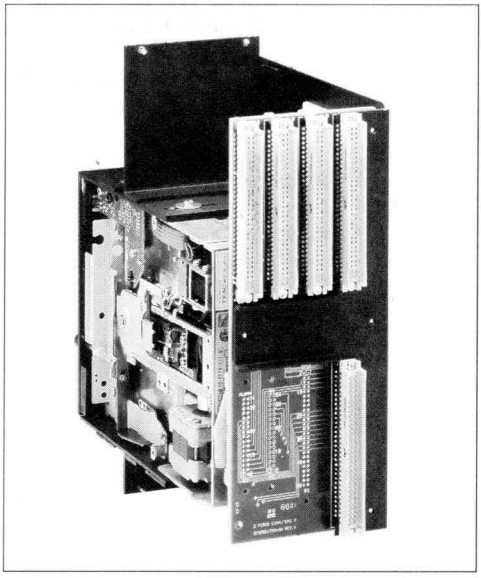
System 68000 VME
TARGET 32
Application Environment



Motherboard



Disk Module



General Description
The SYS68K/TARGET 32 chassis provides the basis for a series of full 32-bit target and development environments based on the VMEbus. The systems may be used standalone or in a 19" rack. The system contains a 20 slot full-height motherboard (J1 and J2), a 500 W power supply. Mass media module options for Winchester disks, streaming tape units and floppy disks are available. Reliability is enhanced as all the modules in the system plug directly into the motherboard and avoid the need for additional cabling.

Features of the TARGET 32
- 19", 7 U chassis
- 20 slot J1–J2 VMEbus motherboard
  - Automatic daisy-chain configuration
  - Connectors for direct connection of power supply
- Fully integrated 500 W power supply
- Cooling system with four fans
- Retractable handles and fold-down front panels
- Dimensions:
  - length × width × height
  - 440 × 450 × 311* mm
    (17.3 × 17.7 × 12.2* in.)
    (* 325 mm [12.8 in.] with feet)

1. The Motherboard
The 20 slot, full-height motherboard provides two connectors, J1 and J2, for each slot and has been designed according to the VMEbus specification IEEE 1014. Automatic active daisy-chain switches are implemented on the motherboard to simplify the installation and removal of boards within the system. All daisy-chain signals of the VMEbus specification are supported by this new feature, which means that no jumper settings are necessary. This is useful when system configurations are being changed.
The motherboard allows the specially designed power supply to be directly connected without the need for a cable harness. Power for all the different modules in the system is distributed via the motherboard. The J2 connectors of the motherboard are easily accessible to the user on the reverse side of the motherboard and are installed with 96-pin male connectors to ease the installation of cables for the distribution of user-defined signals.

2. The Chassis
The TARGET 32 is of a 19", 7 U metal chassis. It can be used both as a desktop system or in a 19" rack. The cooling requirements of the system are provided for by four fans mounted in the floor of the chassis, below the installed boards.
Retractable handles are provided to ease the transportation of the system. To protect the VME boards installed in the system, the chassis can be closed using removable panels.

3. The Power Supply
The installed power supply is a 500 W primary switched unit.

Specification of the Power Supply:
- 110/220 V 50–60 Hz input voltage
- 700 W input and 500 W output power
  - + 5 V* 80 A
  - + 12 V* 8 A (8 A peak)
  - – 12 V* 5 A (6 A peak)
- Operating temperature 0 to + 50 °C
- Supports ACFAIL*, SYSRESET*, SHUTDOWN*
- Separate cooling system with own fan
- Safety class: VDE 0806 – RFI: VDE 0871 Class B

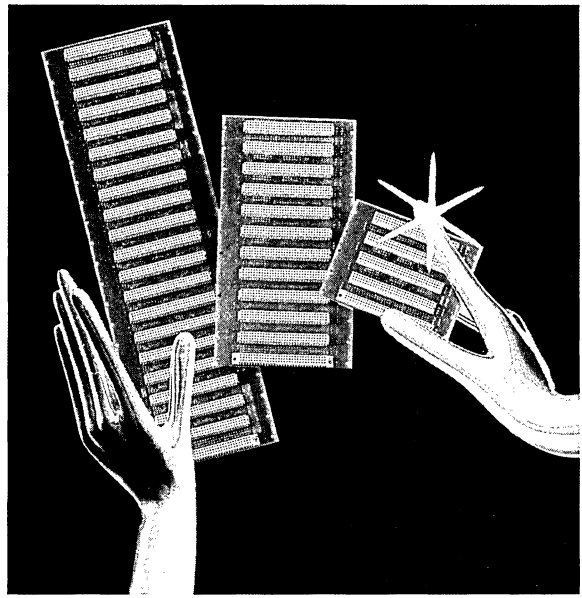
4. The Magnetic Media Module
Magnetic media can be installed in the chassis using the SYS68K/TMMOD-32 magnetic media module. The TMMOD-32 is a flexible frame which can hold either one full-height or two half-height drives. The module plugs directly into the motherboard in the TARGET 32 chassis and occupies five double-height VMEbus slots. The TMMOD-32 module can be supplied either with or without drives.

5. Configurations
Standard system configurations are available. These systems are supplied fully configured and tested, and include power supply, VMEbus board(s), magnetic media and cabling for the I/O interfaces. Operating systems installed are either PDOS, UNIX, or OS-9.
Standard configurations use 90 or 175 Mbyte hard disk, 1 Mbyte floppy disk and, in case of UNIX systems, a 125 Mbyte streaming tape unit.

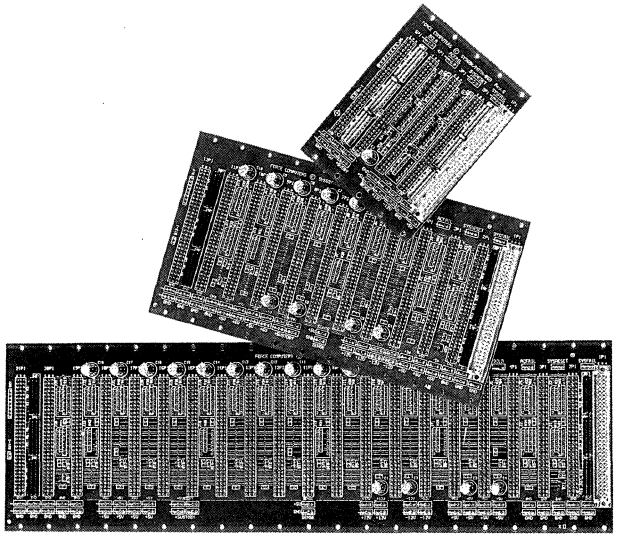
* Maximum combined output power is 500 W.

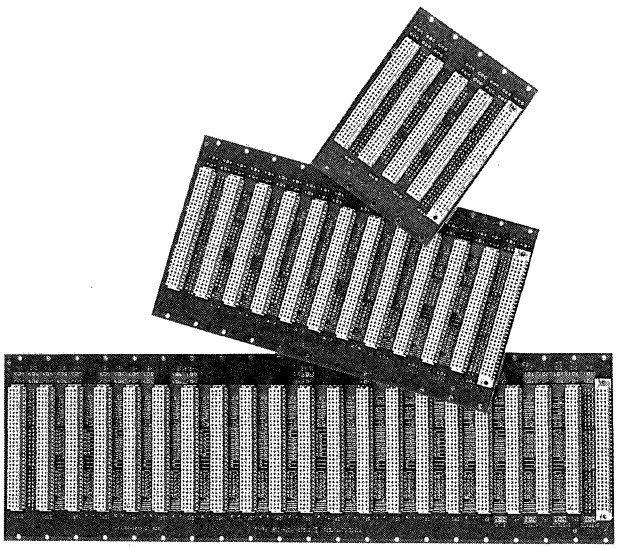
Ordering Information

SYS68K/TARGET 32 Part No. 610500	TARGET 32 chassis with power supply, cooling fans and motherboard. Documentation included.
SYS68K/IOBP-1 Part No. 700043	Internal panel to facilitate connection of disk devices to mass media modules.
SYS68K/RGBBP Part No. 700046	Back panel for AGC-1/AGC-2/AGC-3 with RGB connectors on rear of TARGET 32 chassis.
SYS68K/SIOBP Part No. 700047	Back panel for 8 serial I/O interfaces on rear of TARGET 32 chassis.
SYS68K/64BP Part No. 700048	Back panel for direct connection of VMEbus P2 to rear of TARGET 32 chassis.
SYS68K/TMMOD-32 Part No. 610501	Magnetic media module without disk drives. Documentation included.
SYS68K/TMM-FLOP Part No. 700515	Magnetic media module with 1 Mbyte floppy (SA 460). Documentation included.
SYS68K/TMM-STR Part No. 700514	Magnetic media module with 1 Mbyte floppy (SA 460) and 120 Mbyte streaming tape unit. Documentation included.
SYS68K/TMM-90 Part No. 700500	Magnetic media module with 90 Mbyte hard disk (SCSI), 1 Mbyte floppy (SA 460). Documentation included.
SYS68K/TMM-175 Part No. 700510	Magnetic media module with 175 Mbyte hard disk (SCSI). Documentation included.
SYS68K/TMM-765 Part No. 700516	Magnetic media module with 765 Mbyte hard disk (SCSI). Documentation included.



System 68000 VME
SYS68K/MOTH
VMEbus Motherboards





General Description

The SYS68K/MOTH family conforms fully to the mechanical requiments of the VMEbus IEEE 1014 Specification. This family is a range of 5, 9, 12 or 21 slot VMEbus (IEEE 1014) motherboards containing standard DIN 41612C 96-pin connectors.

Two different backplane versions are defined in the IEEE 1014 Standard Specification, the J1 and J2 backplane. The J1 backplane offers operations with 24 address and 16 data lines which are primarily used for 16-bit processors. The J2 backplane offers an extension to 32-bit processors because by adding 8 address and 16 data lines to fully support 32-bit address and data when used with the J1 backplane. J2 also provides additional power driving capabilities for 16-bit environments.

A 5-slot backplane (SYS68K/MOTH-05B), a 12-slot backplane (SYS68K/MOTH-12B) and a 21-slot J2 backplane (SYS68K/MOTH-E21A) are shown on the previous page.

1. Board Assembly

The SYS68K/MOTH motherboard is produced with gold-plated fast-on connectors for power connections. Additionally, the motherboard (J1 backplane) contains four connectors for the VMEbus, IEEE 1014 bus exception signals:

- BERR*
- ACFAIL*
- SYSFAIL* and
- SYSRESET*

Each signal line is terminated according to the VMEbus Specification with 330/470 Ohm resistors to guarantee the logic high voltage of 2.94 V. The J1 backplane contains 6 resistor networks and the J2 backplane contains two resistor networks for termination.

All IACK* and bus-grant daisy-chain signals on the J1 backplane can be jumpered directly to the next slot to establish the daisy-chain. All jumpers for the daisy-chain are included.

2. Electrical Environment

Power is supplied to the backplanes (J1 and J2) through gold-plated fast-on connectors.

A supply current of maximum 25 A per connector may be drawn.

For a reduction of the contact resistance, the motherboard contains more power connections than required to satisfy the maximum allowed value (approximately 7.2 A per slot at 20 °C ambient). To connect the sense signals of the power supply to the Motherboard, 2 sense signals (+ 5 V SENSE and GND SENSE) are installed in the middle of each backplane.

The SYS68K/MOTH family conforms fully to the mechanical requirements of the VMEbus IEEE 1014 Specification.

The following table lists the number of power points for each supply voltage for each motherboard.

Type		No. of Slots	No. of Connectors				
			+ 5 V	+ 12 V	– 12 V	+ 5 V STDBY	GND
MOTH-05B	J1	5	4	2	2	2	4
MOTH-09B	J1	9	8	2	2	2	8
MOTH-12B	J1	12	12	4	4	4	12
MOTH-21B	J1	21	16	8	8	4	20
MOTH-E05A	J2	5	4	–	–	–	4
MOTH-E09A	J2	9	8	–	–	–	8
MOTH-E12A	J2	12	12	–	–	–	12
MOTH-E21A	J2	21	16	–	–	–	20

3. Mechanical Environment

Each J1 backplane can be used together with each J2 backplane. The J2 backplanes have wire wrap type connector pins on the backside to interconnect to a user-specific I/O module or to a VMXbus or VSB backplane.

Both motherboard types regardless of slot count can be mounted in a standard 19" rack.

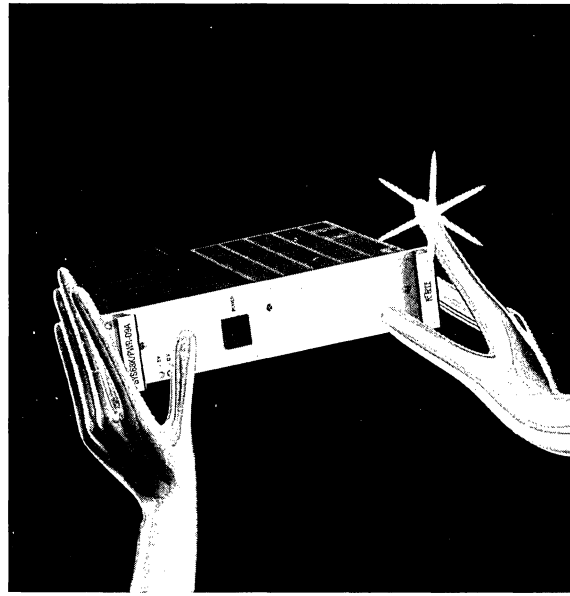
Dimensions	Length (mm)	Length (in)
J1/J2 5 slot	100	39
J1/J2 9 slot	181	71
J1/J2 12 slot	242	95
J1/J2 21 slot	425	167

Specifications

Backplane wiring	Utilizes all specified signal and power supply lines of the VMEbus Specification
Construction	All connectors are supplied in press fit technique J1 backplane 6 layers J2 backplane 2 layers
Connectors	DIN 41612C female connector Gold-plated fast-on connectors for power supply connection and exception signals (4)
Daisy-chain	All daisy-chain signals can be jumpered from the rear of the motherboard
Bus terminators	All specified signal lines have termination networks at both ends of the motherboards (330 Ohm/470 Ohm)
Power requirements	5.5 W (typ) 5 V/1.1 A (typ) J1 backplane 5.5 W (typ) 5 V/0.34 A (typ) J2 backplane
Operating temperature Storage temperature Operating humidity (non-condensing)	0 to + 70 °C – 25 to + 90 °C 5 to 95 %

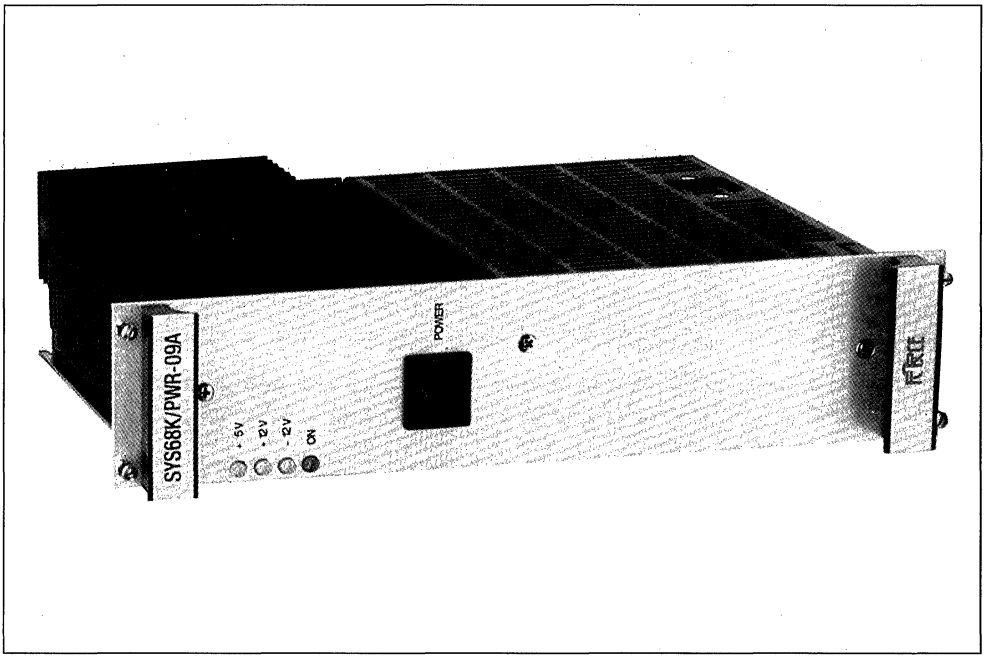
Ordering Information

SYS68K/MOTH-05B Part No. 500005	5 slot J1 motherboard with daisy-chain jumpers. Documentation included.
SYS68K/MOTH-09B Part. No. 500011	9 slot J1 motherboard with daisy-chain jumpers. Documentation included.
SYS68K/MOTH-12B Part No. 500006	12 slot J1 motherboard with daisy-chain jumpers. Documentation included.
SYS68K/MOTH-21B Part No. 500007	21 slot J1 motherboard with daisy-chain jumpers. Documentation included.
SYS68K/MOTH-E05A Part No. 500008	5 slot J2 motherboard with daisy-chain jumpers. Documentation included.
SYS68K/MOTH-E09A Part No. 500012	9 slot J2 motherboard with daisy-chain jumpers. Documentation included.
SYS68K/MOTH-E12A Part No. 500009	12 slot J2 motherboard with daisy-chain jumpers. Documentation included.
SYS68K/MOTH-E21A Part No. 500010	21 slot J2 motherboard with daisy-chain jumpers. Documentation included.
SYS68K/MOTH-B/UM Part No. 800072	Hardware user's manual for all backplanes.

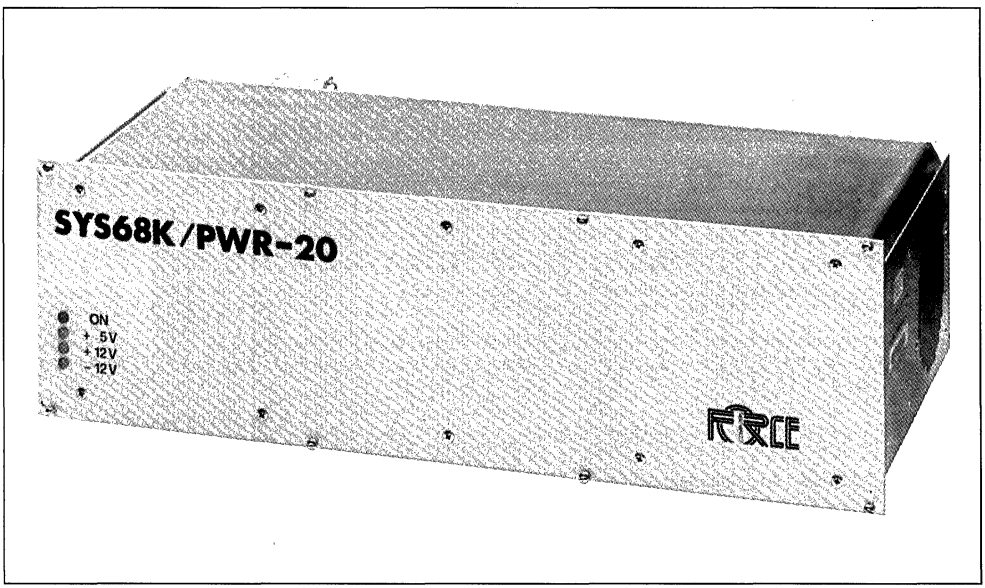


System 68000 VME
SYS68K/PWR-09A/20
250 W/750 W Power Supplies

SYS68K/PWR-09A



SYS68K/PWR-20



General Description

The SYS68K/PWR-09A and SYS68K/PWR-20 are high performance primary switching power supplies. Both are designed especially for highly integrated systems and include VMEbus compatible signals (SYSRESET* and ACFAIL*). PWR-09A and PWR-20 can be powered from 110 V or 220 V AC at 50 to 60 Hz, and provide outputs of + 5 V, + 12 V and – 12 V each with their own control LEDs on the front panel.

The PWR-09A output is on two DIN 41612 connectors mounted on the rear of the unit, allowing easy installation into a system. A cable subassembly is also provided for direct connection to floppy/Winchester drives and a VMEbus motherboard.

The PWR-20 output is on a single HIS DIN 41612 connector mounted on the rear of the unit. An inhibit switch signal is also supported on PWR-20 for the control of the output voltages.

Features of PWR-09A

- Output + 5 V/36 A
  + 12 V/ 6 A
  – 12 V/ 2 A
- 19" rack compatible
- SYSRESET*, ACFAIL* VMEbus signal compatible
- Input 110 V/220 V at 50–60 Hz
- Sense line for + 5 V

Features of PWR-20

- Output + 5 V/90 A
  + 12 V/20 A
  – 12 V/ 5 A
- 19" rack compatible
- SYSRESET*, ACFAIL* VMEbus signal compatible
- Input 110 V/220 V at 50–60 Hz
- Sense lines for + 5 V, + 12 V, CWD
- Inhibit Switch Signal

Specifications PWR-09A

Input voltage	110/220 V AC +/– 10 % user-selectable via fuse		
Input frequency	50 – 60 Hz		
Input current	220 V AC : 2.5 A (typ), 50 A (max) input peak 110 V AC : 5 A (typ), 50 A (max) input peak		
Output voltage	+ 5 V	+ 12 V	– 12 V
Output current	36 A	6 A	2 A
Efficiency	> 75 % (5 V)		
Pard (periodic ripple) (random noise)	50 mVPP (30 MHz bandwidth) < 50 MVr.m.s (10 MHz bandwidth)		
Dynamic behavior	For instantaneous load changes (dIo/dt = 0.5 A/µsec) the transient recovery time to settle within 1.5 % of output voltage: 2 msec for Io = 30 % – 80 % IA nominal For transient voltage changes (overshoot) which could exceed the regulation limits: 200 mV for IA nom. = 30 % – 80 % or 80 % – 30 %		
Regulation	for +/– 10 % main input variations + 5 V stat +/– 1 %		
Turn-on delay time	< 800 msec to reach load specification at 25 °C		
Turn-off decay time	> 10 msec at nom. load and nom. mains		
Output protection	Full overload protection of all outputs short approx. 9,66 × IA nom. OVP (5 V) approx. 1.3 × UA nom.		
Operating temperature Storage temperature	0 to + 50 °C with free convection or forced cooling (3 m/sec) – 25 to + 85 °C		
Relative humidity	10 to 90 % (non-condensing)		
Safety Class RFI	Conforms to Class I VDE 0804 VDE 0871 class B		
Connectors	Two H 15 DIN 41612		
Dimensions	Full metal cassette 6 U/12TE, depth 210 mm/8.26 inch 266.4 mm/60.96 mm		
Weight	3.0 kg		

Specifications PWR-20

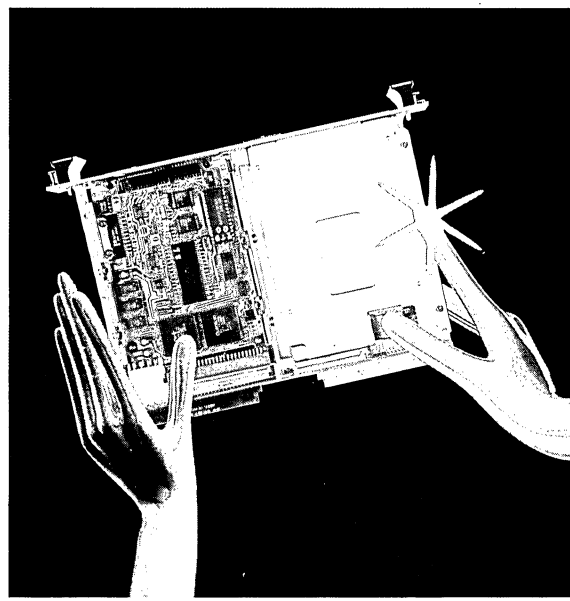
Input voltage	110 V AC +/– 20 % user-selectable 220 V AC + 20 %,– 10 % user-selectable		
Input frequency	50–60 Hz		
Input current	220 V AC : 8 A (typ) 100 A (max) input peak 110 V AC : 16 A (typ) 100 A (max) input peak		
Output voltage	+ 5 V	+ 12 V	– 12 V
Output current	90 A	20 A	5 A
Efficiency	> 75 % (5 V)		
Pard (periodic ripple) (random noise)	< 50 mVPP (30 MHz bandwidth) < 30 mVr.m.s (10 MHz bandwidth)		
Dynamic behavior	For instantaneous load changes (dIo/dt = 0.5 A/υs) the transient recovery time to settle within 1.5 % of output voltage: 2 msec for Io = 30 % – 80 % IA nominal For transient voltage changes (overshoot) which could exceed the regulation limits: 200 mV for IA nom. = 30 % – 80 % or 80 % – 30 %		
Regulation	for +/– 10 % main input variations + 5 V stat +/– 1 %		
Turn-on delay time	< 800 msec to reach load specification at 25 °C		
Turn-off decay time	> 10 msec at nom. load and nom. mains		
Output protection	Full overload protection of all outputs short approx. 9,66 × IA nom. OVP (5V) approx. 1.3 × UA nom.		
Operating temperature Storage temperature Relative humidity	With free convection or forced cooling (3 m/sec) 0 to + 50 °C – 25 to + 85 °C 10 to 90 % (non-condensing)		
Safety class RFI	Conforms to class I VDE 0804 VDE 0871 class B		
Connectors	One H 15 DIN 41612 and two cupreous flanges		
Dimensions	Full metal cassette 3 U/84TE,depth 200 mm/7.86 inch		
Weight	10.5 kg		

Ordering Information PWR-09A

SYS68K/PWR-09A Part No. 700008	Power supply PWR-09A. Documentation included.
SYS68K/PWR-09A/CA Part No. 700018	Cable assembly for the PWR-09A.
SYS68K/PWR-09A/UM Part No. 800060	User's manual for SYS68K/PWR-09A.

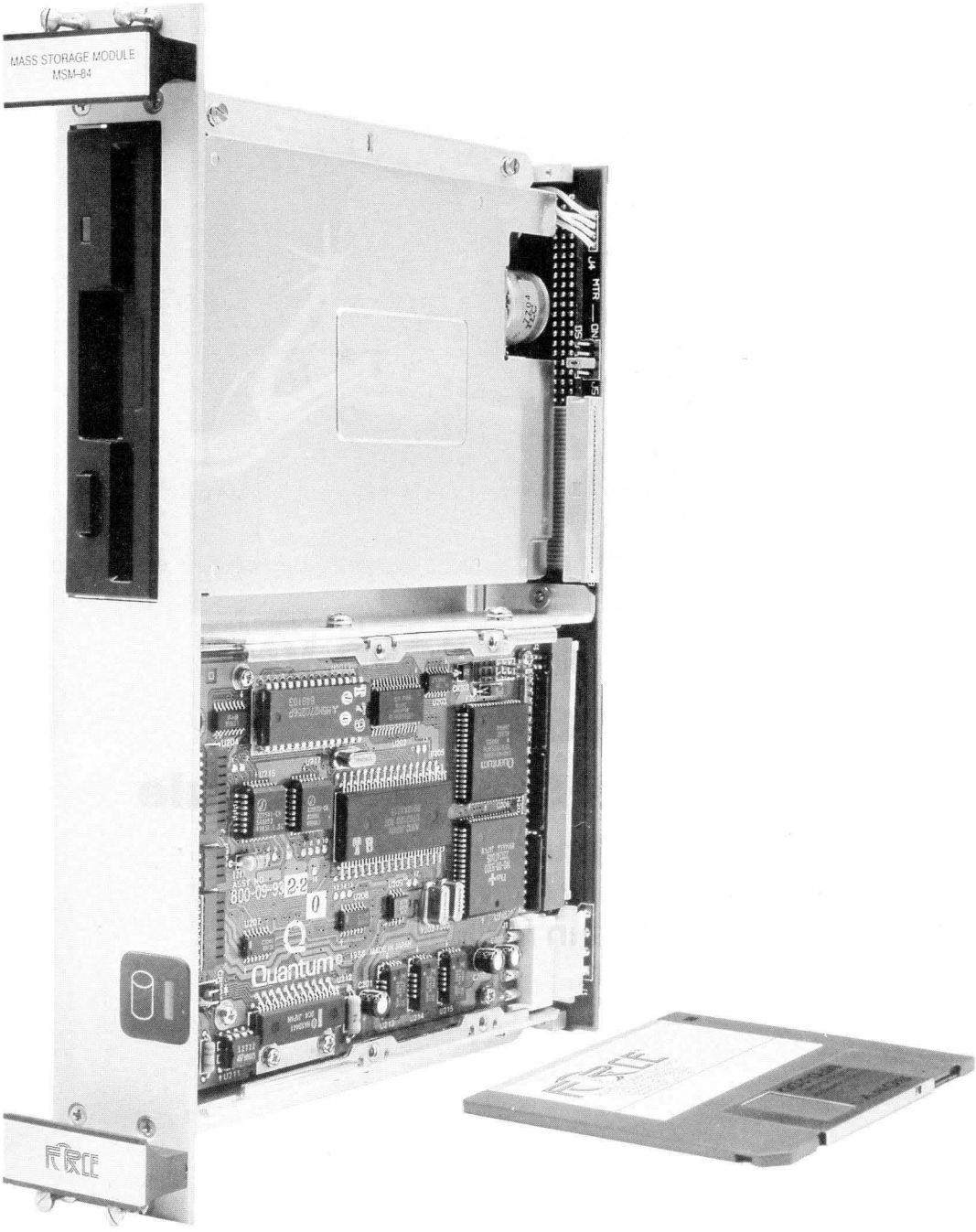
Ordering Information PWR-20

SYS68K/PWR-20 Part No. 700009	Power supply PWR-20. Documentation included.
SYS68K/PWR-20/CA Part No. 700030	Cable assembly for the PWR-20.
SYS68K/PWR-20/UM Part No. 800070	User's manual for SYS68K/PWR-20.



System 68000 VME SYS68K/MSM Mass Storage Module

SCSI Winchester and Floppy Drive Module in VMEbus Card Format


MASS STORAGE MODULE
MSM-84
J4 MTR ON
Quantum
FORCE

General Description

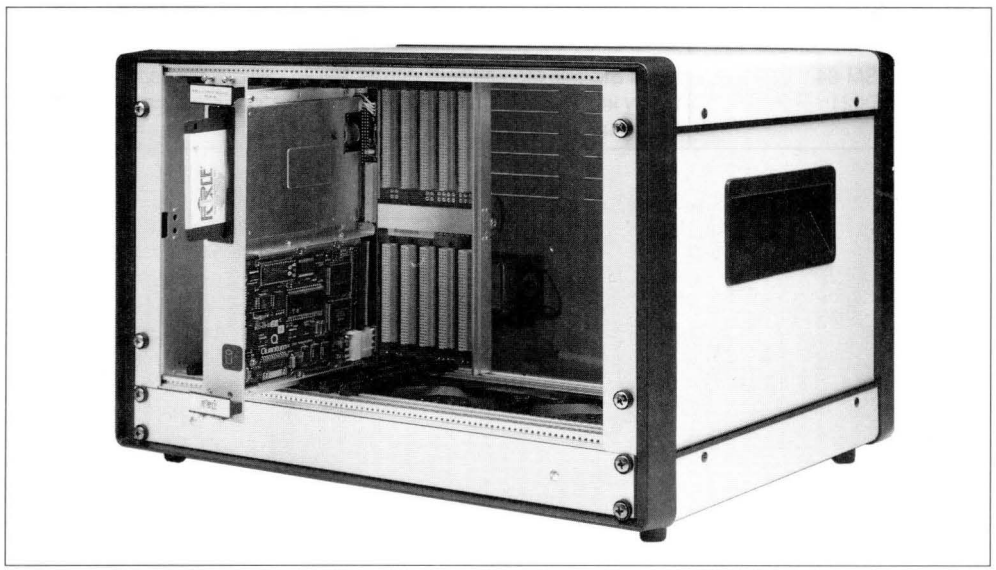
The MSM-42 and MSM-84 Mass Storage Module product provides a hard disk and floppy disk combination to support mass storage requirements in VMEbus systems. Both MSM-42 and MSM-84 occupy only two VMEbus slots, making available more system slots for additional VMEbus boards.

The MSM-42 utilizes industry-standard 3 1/2" disk drives providing 42 Mbyte (formatted) of nonremovable (Winchester) disk space and 720 Kbyte (formatted) of removable (floppy) disk storage in a compact, low power VMEbus board format. The MSM-84 provides an 84 Mbyte and 720 Kbyte configuration. The MSM-42 and MSM-84 are designed for complete compatibility with FORCE COMPUTERS' CPU-23, CPU-26, CPU-37 and CPU-30 single board computers, and ISCSI-1 Intelligent SCSI Controller board. Both the MSM-42 and MSM-84 will work also with any other VMEbus products which support the SCSI and SA-460 interface specifications.

MSM-42 and MSM-84 Features

- High-capacity, high-speed 3 1/2" Winchester disk drive
  - 42 Mbyte (MSM-42) or 84 Mbyte (MSM-84) formatted configurations
  - 19 msec average access time
  - Industry standard Small Computer Systems Interface (SCSI)
  - 2.0 Mbyte/sec asynchronous, 4.0 Mbyte synchronous data transfers
- 720 Kbyte 3 1/2" floppy disk drive
  - SA 460 interface
  - 250 Kbyte/sec transfer rate
- Up to 7 Mass Storage Modules can be cascaded to increase storage capacity
- Requires only two (2= VMEbus slots 6U high form factor)
  - End slot compatible
- Easy insertion and removal for protecting data in secure environments
- Power drawn directly from VMEbus P1 connector
- Pin-compatible with FORCE COMPUTERS CPU-23, CPU-26, CPU-37, CPU-30 and ISCSI-1
  - Simple connection to host board through flat-ribbon cables (included)
  - Front panel LEDs for activity indicators

Mass Storage Module installed in Card Cage

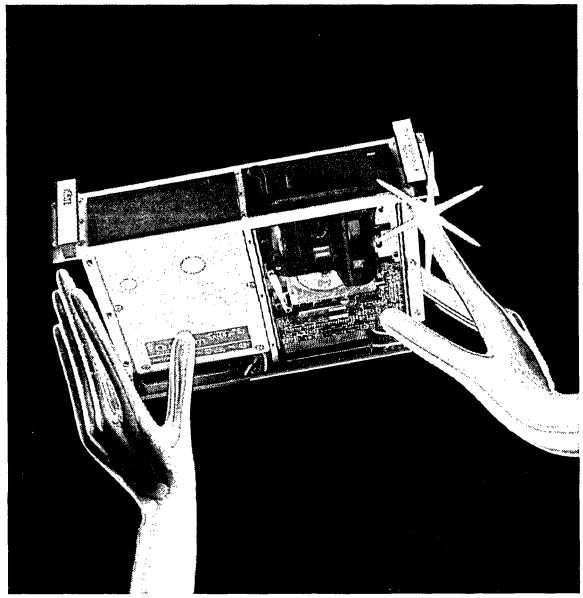


Specifications

Function	MSM-42	MSM-84
Capacity Winchester (formatted) Floppy (formatted)	 42 Mbyte 720 Kbyte	 84 Mbyte 720 Kbyte
Transfer Rate Winchester (Async/Sync) Floppy	 2/4 Mbyte/sec 250 Kbyte/sec	 2/4 Mbyte/sec 250 Kbyte/sec
Interface Winchester Floppy	 SCSI SA460	 SCSI SA460
Power (Typ/Max) + 12 VDC + 5 VDC	 0.8/1.6 Amps 0.6 Amps	 0.8/1.6 Amps 0.6 Amps
Operating temperature Relative humidity	+ 10 C – 46 C + 10 % – 80 %	+ 10 C – 46 C + 10 % – 80 %
Connectors	VMEbus P1 and P2	VMEbus P1 and P2
Dimension Millimeters Inches	 233.35 × 160 × 40.64 9.18 × 6.3 × 1.6	 233.35 × 160 × 40.64 9.18 × 6.3 × 1.6

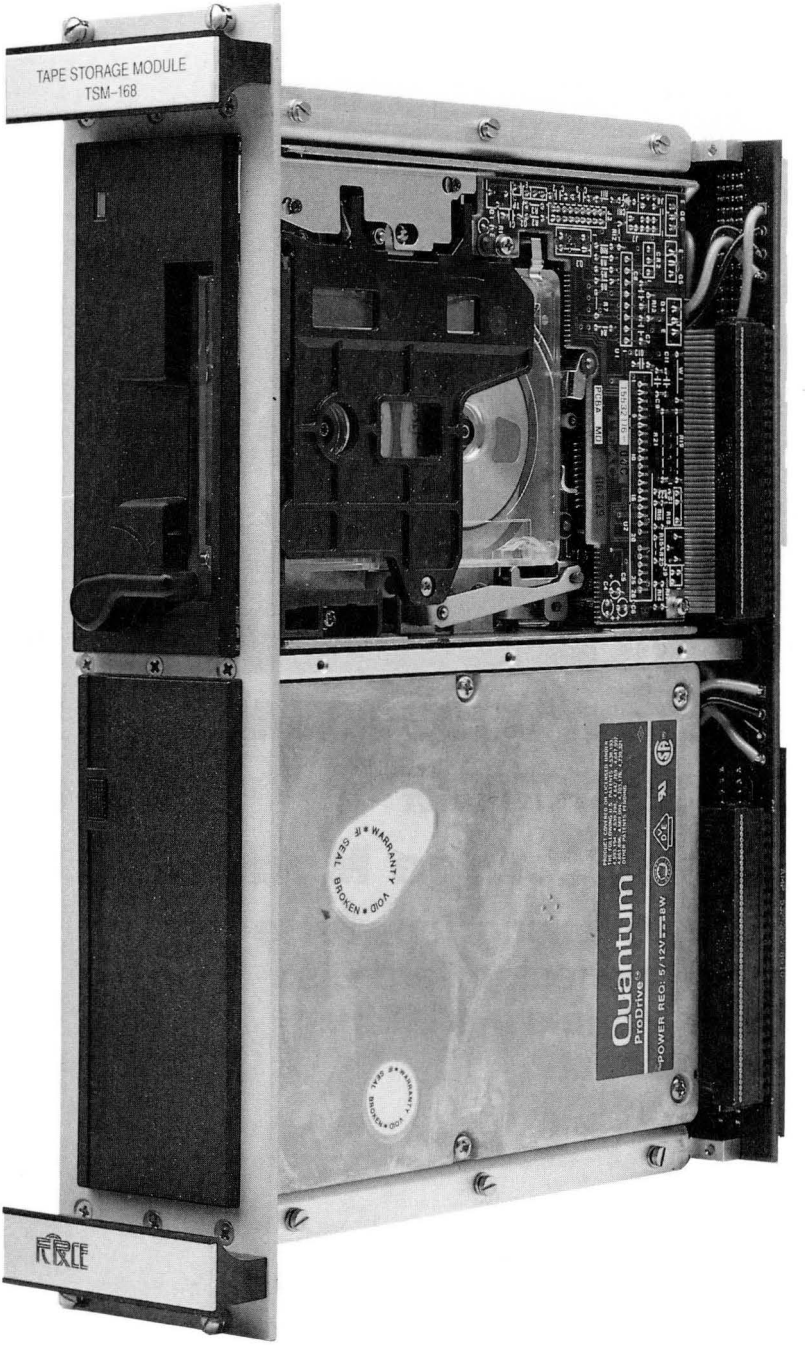
Ordering Information

SYS88K/MSM-42 Part No. 510020	Mass Storage Module card with 42 Mbyte Winchester and 720 Kbyte floppy in VMEbus card format, including cables as well as user and OEM manuals.
SYS88K/MSM-84 Part No. 510021	Mass Storage Module card with 84 Mbyte Winchester and 720 Kbyte floppy in VMEbus card format, including cables as well as user and OEM manuals.



System 88000 VME
SYS88K/TSM
Tape Storage Module

SCSI Streaming Tape Drive and Winchester Hard Disk Drive Module in VMEbus card format


TAPE STORAGE MODULE
TSM-168
FORCE
Quantum
ProDrive
POWER REQ: 5/12V
WARRANTY VOID BROKEN SEAL

General Description

The TSM-168 Tape Storage Module product provides a hard disk and tape drive combination to support mass storage requirements in VMEbus systems. The TSM-168 occupies only three VMEbus slots, making available more system slots for additional VMEbus boards.

The TSM-168 utilizes industry-standard 3 ½" devices providing 155 Mbyte of streaming tape back-up and 168 Mbyte (formatted) of non-removable (Winchester) disk space in a compact, low power VMEbus board format. The TSM-168 is designed for complete compatibility with FORCE COMPUTERS' CPU-30 and CPU-37 single board computers, and ISCSI-1 Intelligent SCSI Controller board. The TSM-168 will work also with any other VMEbus products which support the SCSI interface specifications.

TSM-168 Features

- High-capacity, high-speed 3 ½" Winchester disk drive
  - 168 Mbyte formatted
  - 19 msec average access time
  - SCSI interface
- 3 ½" streaming tape drive
  - 155 Mbyte back-up in 23 minutes
  - 90 inches/sec tape speed
  - 12,800 bpi recording density
  - Uses compact, cassette-size tape units
  - SCSI interface
- Industry standard Small Computer Systems Interface (SCSI)
  - 1.5 Mbyte/sec asynchronous, 4.0 Mbyte synchronous data transfers
- Up to 3 Tape Storage Modules can be cascaded to increase storage capacity
  - TSM-168 can operate on same SCSI interface as FORCE'S MSM-42 and MSM-84
- Requires only three (3) VMEbus slots (6U high form factor)
- Power drawn directly from VMEbus P1 connectors
- Easy insertion and removal for protecting data in secure environmentsecure environments
- Pin-compatible with FORCE COMPUTERS CPU-30, CPU-37, and ISCSI-1
  - Simple connection to host board through flat-ribbon cable (included)
- Front panel LED activity indicators

Specifications

	TSM-168
Capacity	
Winchester (formatted)	168 Mbyte
Tape drive	155 Mbyte
Interface	
Winchester	SCSI
Tape Drive	SCSI
Power	
+ 12 VDC	2.0 Amps
+ 5 VDC	2.5 Amps
Operating temperature	+ 10 to + 46 °C
Relative humidity	10 to 80 %
Connectors	VMEbus P1 and P2

Ordering Information

SYS88K/TSM 168 Part No. 510092	Tape Storage Module card with 155 Mbyte Streaming Tape Drive and 168 Mbyte Winchester hard disk drive in VMEbus card format, including user and OEM manuals.

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"Critical components" covers any component of a life support device or system whose failure to perform can be expected to cause the failure of the life support system or device, or to negatively affect its safety or effectiveness.

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