SPARC CPU-2CE
USER'S INSTALLATION MANUAL

FORCE COMPUTERS Inc./GmbH

Part Number 049-12443-101 Ver. A4

NOTE

The information in this document has been carefully checked and is believed to be entirely reliable. FORCE COMPUTERS makes no warranty of any kind with regard to the material in this document, and assumes no responsibility for any errors that may appear in this document. FORCE COMPUTERS reserves the right to make changes without notice to this, or any of its products, to improve reliability, performance, or design.

FORCE COMPUTERS assumes no responsibility for the use of any circuitry other than circuitry which is part of a product of FORCE COMPUTERS Inc./GmbH

FORCE COMPUTERS does not convey to the purchaser of the product described herein any license under the patent rights of FORCE COMPUTERS Inc./GmbH nor the rights of others.

FORCE COMPUTERS Inc.
2001 Logic Drive
San Jose, CA 95124
U.S.A.

Phone : (408) 371-5900
FAX : (408) 371-3382

FORCE COMPUTERS FRANCE Sarl
Le Volta
17-19 Rue Jeanne Braconnier
F-92366 Meudon La Foret/Cedex

When dialing from U.S.:
Phone : (1) 41 07 95 15
FAX : (1) 45 37 06 19

FORCE COMPUTERS GmbH
Prof.-Messerschmitt-Strasse 1
D-85579 Neubiberg/Munchen
Germany

When dialing from U.S.:
Phone : (089)-608 14-0
Telex : 524-190 forc-d
FAX : (089) 609 77 93

FORCE COMPUTERS UK Ltd.
No. 1 Holly Court
3 Tring Road
Wendover
Buckinghamshire HP22 6PE
England

When dialing from U.S.:
Phone : (0296) 625456
Telex : 838033
FAX : (0296) 624027

TABLE OF CONTENTS

Section 1

Section 2

List of Tables

List of Figures

Section 1

1.0 INTRODUCTION

A complete VMEbus-based SPARCstation™ 2 architecture with Sbus expansion. The SPARC CPU-2CE is the latest innovation resulting from the technology partnership of FORCE COMPUTERS and Sun Microsystems. Combining a true SPARCstation 2 architecture with FORCE COMPUTERS expertise and experience in standard 6U Eurocards has resulted in a faithful SPARCstation 2 implementation in a single VMEbus slot.

The SPARC CPU-2CE™ offers the same I/O interfaces as the SPARCstation 2, including DMA supported SCSI and Ethernet ports along with audio, keyboard/mouse and two serial channels with full modem support. Two Sbus sockets allow the installation of standard, off-the-shelf Sbus modules such as graphic frame buffers or accelerators or any other of over 300 Sbus cards available from third-party vendors.

Through its binary compatibility with the Sun SPARCstation 2 family, the SPARC CPU-2CE runs current versions of SunOS™/Solaris™ as well as the more than 4,000 shrink-wrapped SPARCware™ applications available today. In addition, a variety of real-time operating systems will be available.

Its IEEE 1014 compatible VMEbus interface enables the SPARC CPU-2CE user to build high-performance embedded UNIX® systems, SPARC®- based real-time systems and hybrid UNIX/real-time systems linked via the VMEbus or local- and/or wide-area networks.

The SPARC CPU-2CE is a compact single board computer that brings the power and functionality of the popular Sun SPARCstation 2 to the industry-standard VMEbus for use in UNIX and real-time applications.

Figure: 1.1 Block Diagram

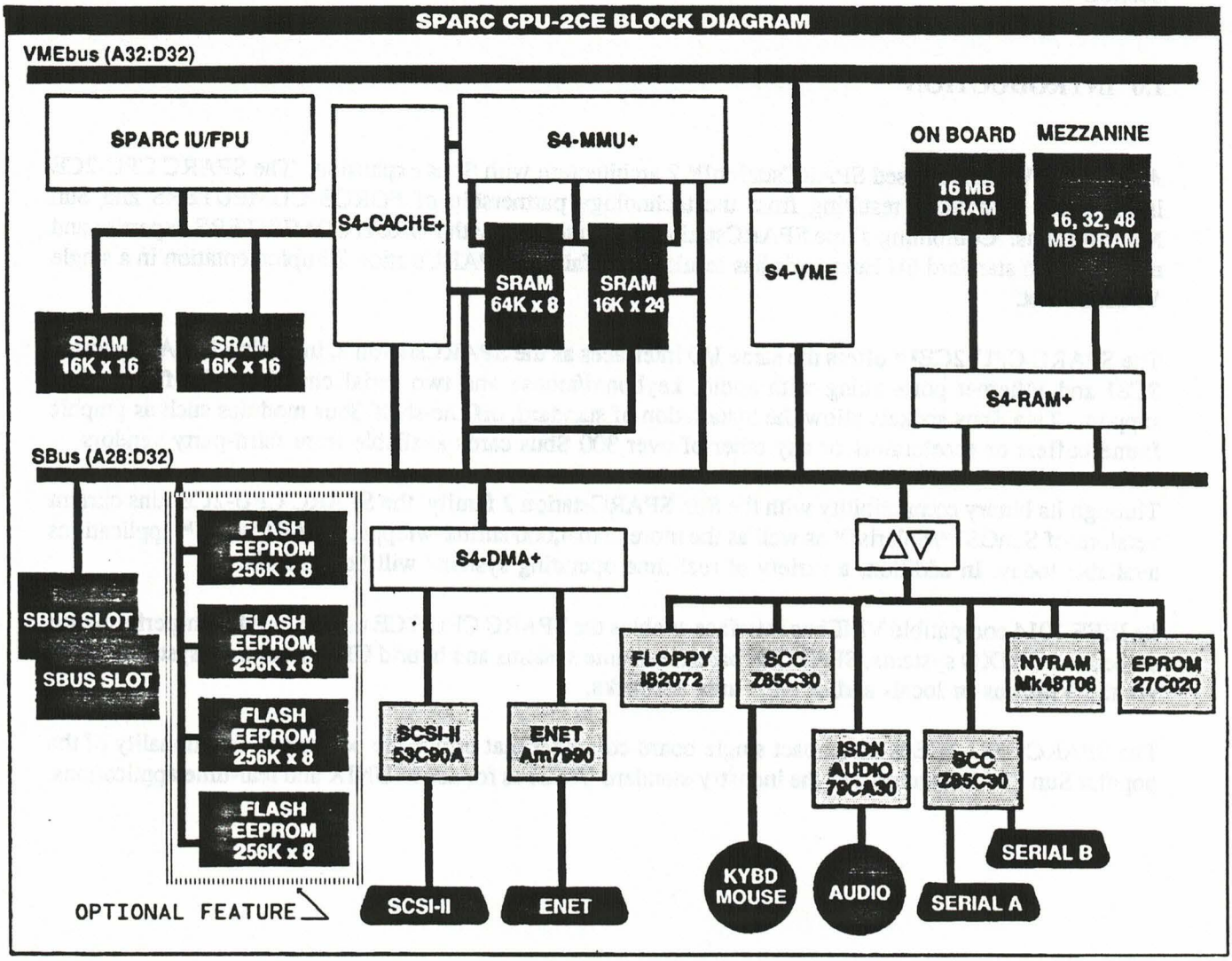
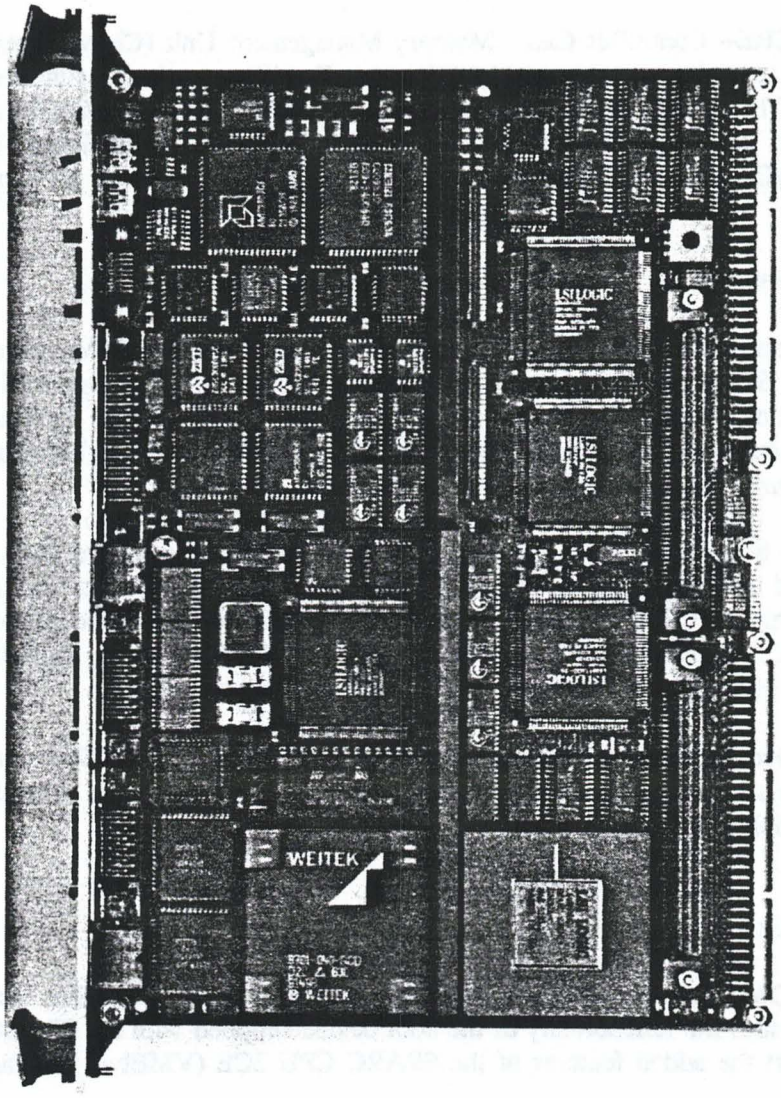


Figure: 1.2 Photo Page



1.1 The Processor

A 40-Mhz SPARC (Scalable Processor ARChitecture) 32-bit RISC processor chip set is at the core of the SPARC CPU-2CE. It is comprised of an integrated Integer Unit/Floating Point Unit (IU/FPU), a Sun standard SRAM-based Memory Management Unit (S4-MMU+), a Cache Controller (S4-Cache+) and two Cache RAM chips. Operating at 40 Mhz, the IU/FPU provides 28.5 MIPS integer performance and 4.2 MFLOPS floating point performance. The Cache Controller provides a 2-Kbyte tag array for a 64-Kbyte, virtual, write-through cache.

The integrated S4-CACHE+ Controller Cache/Memory Management Unit (CMMU) handles the cache memory, provides path to main memory over the SBus, handles SBus controller function, and works at 40 MHz clock speed. The SPARC CPU-2CE has two cache RAMs that are 16K x 16 devices and run at 40 MHz clock speed. The large cache and double word write buffer means higher hit ratios and the ability to sustain high I/O DMA bandwidths with only a small reduction in local CPU performance.

1.2 The Memory Subsystem

The SPARC CPU-2CE chip set includes the S4-RAM+, an Sbus-compatible DRAM controller with single clock burst capability. S4-RAM+ operates the DRAM in fast page mode to support 8-, 16-, 32-, and 64-byte bursts at one transfer per clock after an initial access latency of 4 clocks for reads and 2 clocks for writes. The configuration supports up to 64 Mbytes of 32-bit wide DRAM on board and incorporates parity generation and parity error detection.

The SPARC CPU-2CE is available with 16-, 32-, 48-, or 64-Mbytes of on-board DRAM. 16 Mbytes reside on the base-board and are implemented using high-reliability TSOP devices. Additional capacity, up to 64 Mbytes, is achieved using separate mezzanine modules which retain the single-slot capability without interfering with Sbus expandability on the SPARC CPU-2CE. Memory capacity upgrades are possible since the DRAM mezzanine modules are designed for field installation.

Memory can be expanded beyond the 64-Mbyte on-board limit via an SBus SRX-2 card. This option expands Type0 memory space by up to 64 Mbytes and is cacheable, an advantage over other Sbus-based memory expansion modules.

1.3 System EPROM Open Boot™:

The Open Boot™ EPROM on the SPARC CPU-2CE is located in a single 32 bit DIP socket that enables easy upgrading. It provides the functionality of the boot device supplied with the SPARCstation 2, with enhancements to support the added features of the SPARC CPU-2CE (VMEbus interface and optional Flash EEPROM).

There is an EPROM-based monitor/debugger called Open Boot™. Open Boot is a trademark by Sun.

1.4 FLASH EEPROM (Optional Feature)

In addition to the boot device, the SPARC CPU-2CE employs 4 FLASH EEPROMs in TSOP packages for flexibility and customization. This 1-Mbyte FLASH EEPROM is organized to be 32-bits wide and is mapped in place of the Sun SPARCstation 2 Sbus Slot 3.

These EEPROMs are erasable and writable by the user and allow the system integrator to incorporate FCODE drivers for system specific VME-based products using routines supplied in the boot ROM. With 150 ns EEPROMs, the access time is 4 clocks.

The SPARC CPU-2CE allows integrators to specify their product as the console or boot device without having to modify the on-board firmware. It also allows them to take advantage of SunOS loadable drivers for their VME products. This feature provides a path to firmware-assisted system auto-configuration.

1.5 Local I/O

Ethernet, SCSI interfaces, two serial interface ports, a keyboard serial port, a mouse serial port, a floppy disk controller, and an audio input / output port are provided.

Serial Interface Ports

The Zilog Z85C30 Serial Communications Controller (SCC) supports two serial interface ports using 26-pin connectors on the front panel for synchronous and asynchronous communications. Data rates up to 64 Kbaud are supported and are user configurable, with a pluggable shunt for either RS-232C or RS-423C, and offer full modem control and interrupt capability. Both ports must be set identical as either RS-232 or RS-423.

Keyboard/Mouse Port

The connector for the keyboard/mouse port uses a SPARCstation Type 2 8-pin Mini-circular DIN connector on the front panel. The Z85C30 SCC for the keyboard/mouse port is terminated with TTL buffers and uses all TTL-compatible data signals. The interface is fully compatible with Sun SPARCstation 2 keyboard and mouse product offerings and uses the same cables.

Floppy Disk Controller

An Intel i82072 functions as the floppy disk controller and is fully compatible with the Sun SPARCstation 2. The floppy disk controller signals are available on the User I/O lines of the P2 connector.

Audio Port

The audio interface is implemented with an AMD Am79CA30 ISDN/audio controller device and is fully compatible with the Sun SPARCstation 2. The audio connector on the front panel is an 8-pin Mini-circular DIN connector. As in the SPARCstation 2, the ISDN functionality of the Am79CA30 is not implemented.

1.6 S4+DMA

The DMA ASIC provides DMA and data assembly-disassembly functions for both the Ethernet and SCSI interfaces. The ASIC contains a 32 byte FIFO for each interface and performs DMA in 16 byte bursts when alignment and transfer length permit.

1.7 Small Computer Systems Interface (SCSI)

The SCSI interface provides a standard interface to a wide variety of mass storage devices, such as hard disks, tapes, and CD-ROMs.

The SPARC CPU-2CE board features a Small Computer System Interface (SCSI) controller device using the NCR 53C90A controller chip augmented by the S4+DMA(D-channel). This provides SCSI-I functionality and can transfer at up to 5 Mbytes/sec, depending on the speed of the target.

The SCSI controller on the SPARC CPU-2CE acts as a SCSI initiator. Up to seven SCSI target devices can be connected to a SPARC CPU-2CE board. The SCSI bus is properly buffered and terminated on the SPARC CPU-2CE, so that the connection of SCSI devices is simple and straight forward. Just attach a terminated SCSI device with a cable and the CPU-2CE will automatically adjust for proper termination.

The DMA features full SCSI specification, ANSI X3.131/1986, compatibility. It supports both synchronous and asychronous operation with SCSIbus signals connected to the front panel connector and VMEbus P2 connector. Single ended mode is supported only.

The SCSI bus is routed to both the front panel, via a 50-pin SCSI-II connector, and to the board's P2 User I/O pins.

1.8 Ethernet Interface

The Ethernet interface is comprised of the S4-DMA+ interface chip for DMA, the AMD Am7990 Local Area Network Controller (LANCE) chip and the AMD Am7992B Serial Interface Adapter (SIA). The IEEE 802.3 Ethernet interface is available via a 15-pin Micro-D connector on the front panel. An adapter cable for the MicoD to the regular DB15 is available. The S4-DMA+ chip contains a 32-byte FIFO and increases performance through its 16-byte DMA burst capability.

The Ethernet interface features compatibility to the IEEE 802.3 Ethernet specification, DMA burst capability, data rate of up to 10 Mbit/sec, interrupt generation (Level 6), and utilization of up to 128 Kbytes of memory.

1.9 Real-Time Clock/NVRAM

The SPARC CPU-2CE board uses the Mostek MK48T08 RTC-NVRAM chip. This device includes an 8-Kbyte non-volatile static RAM, of which 2 Kbyte is user programmable, and a clock/calendar circuit. Both are supported by a 10-year shelf-life lithium battery, in order to retain data when the board is powered down.

1.10 SBus Interface

The SBus is a high performance CMOS bus and the basic interconnection mechanism for the system between the CPU and main memory and I/O devices. Two Sbus connectors are available for I/O expansion into the next VME slot.

The Sbus is a high-performance expansion bus with a bandwidth of over 50 Mbytes/sec. The Sbus forms the local memory and I/O bus for the SPARC CPU-2CE and features 32-bit virtual addressing, 28-bit physical addressing, 32-bit data path, synchronous data transfer and master/slave capability. The SPARC CPU-2CE incorporates two Sbus sockets for I/O expansion. These provide support and compatibility with the hundreds of third-party Sbus expansion products on the market, including products for video and graphics, connectivity and networking, manufacturing and process control, engineering, and scientific instrumentation.

FORCE offers a 6U VMEbus Front Panel with two SBus board cutouts used to mount SBus boards to the CPU-2CE.

1.11 VMEbus Interface

The SPARC CPU-2CE utilizes the Sun S4-VME Chip to provide a complete 32-bit VMEbus interface. Since this is the same device used on the SPARC CPU-1E from FORCE COMPUTERS system performance upgrades with minimal software changes are guaranteed. Supported functions include master and slave data transfer capabilities, and VMEbus interrupt handling and arbitration functions. Additional VMEbus utility functions and a special loop-back cycle for standalone testing of the interface are provided.

The VMEbus interface on the SPARC CPU-2CE is fully supported by a driver for the SunOS/Solaris operating system. The software support also includes an implementation of the ONC/VME protocol which supports standard networking protocols such as TCP/IP, NFS and RPCs across the VMEbus backplane. The VME Driver is needed to implement VME software.

1.11.1 Master Interface

The VMEbus master interface allows 16-, 24-, and 32-bit addressing with 8-, 16-, and 32-bit data transfers. A full 4-GByte address range is available and may be mapped contiguously without the 512-Mbyte limitation typically imposed by the 28-bit Sbus definition. This is done by directing normally unused MMU signals to VMEbus decoding logic, external to the S4-VME chip. A software switch enables the standard S4-VME 512-Mbyte address mode with window mapping registers. This 28-bit mode emulates the SPARC CPU-1E VMEbus addressing scheme, allowing customers a migration path to help preserve a previous investment in custom VMEbus drivers.

Read-modify-write cycles are supported for master accesses, and a 300 µsec VMEbus timer is included.

NOTE: Unaligned transfers are not supported by the S4-VME chip.

1.11.2 Slave Interface

Access to the on-board DRAM is allowed to a 1-Mbyte page configurable on 1-Mbyte boundaries within the local address space. Addressing is recognized for both 32- and 24-bit standard accesses, with 16-bit accesses reserved for the mail box interrupt. Address modifiers are supported, and any slave access as a Direct Virtual Memory Access (DVMA) device is set to the local supervisor mode in accordance with the Sun-4™ architecture. The 1-Mbyte VME address space selected is always mapped to the highest megabyte in the virtual address space in accordance with the Sun-4 architecture. Unaligned slave accesses are not supported by the S4-VME chip. See the chapter on the VMEbus Interface for more details.

A mail box interrupt function allows other VMEbus devices to interrupt the SPARC CPU-2CE. This mail box detects accesses to the specific A16 address space set in the mail box register. Mail box accesses are acknowledged as standard VMEbus cycles, and trigger an on-board level 13 interrupt.

1.11.3 Interrupts

The on-board interrupt handler selectively supports all seven VMEbus interrupt levels which are routed directly to the S4-MMU interrupt logic. Control of interrupts is handled via software in the interrupt enable register.

1.11.4 System Controller

The SPARC CPU-2CE is capable of providing Slot 1 system controller functions. The S4-VMEbus requestor is a release on request (ROR) requestor. Bus requests are made on BR3.

The VMEbus arbiter function is used when the SPARC CPU-2CE is configured for system controller functions (Slot 1 jumper). Both single-level (SGL) and round robin (RRS) arbitration are provided. Bus timer logic is included to prevent a VMEbus lockup to a non-responding bus requestor or to a non-existent slave device.

Additional system controller functions are automatically activated, when the Slot 1 jumper is enabled. These capabilities include: IACK Daisy Chain Driver, SYSRESET, SYSFAIL and VMEbus system clock.

1.12 Software Description

With full SPARCstation 2 architecture compatibility, the SPARC CPU-2CE runs the Solaris operating system, including enhancements specific to the Sun SPARCstation product line. Solaris provides an advanced development and run-time environment for the SPARC CPU-2CE. As the first "shrink-wrapped" distributed computing solution, Solaris is comprised of SunOS, ONC© networking environments, OpenWindows™, OPEN LOOK® and DeskSet™. SunOS is the highest quality and most widely supported enriched UNIX implementation available today.

By carefully merging the most robust functionality of UNIX System V™, Berkeley BSD™, and Xenix™; SunOS offers the optimum balance of UNIX capability, reliability, and performance. Further functionality includes:

- Standards Conformance (POSIX, X/Open, XPG, SVID and FIPS)

- The OpenWindows "Look and Feel" Graphical User Interface

• Hierarchical and consistent format file system that includes support for MS-DOS®, CD-ROM and RFS, among others

• ONC networking environment for distributed computing across multivendor networks

• Enhanced UNIX kernel with internationalization, system accounting, security and redundancy

• A comprehensive range of third-party software that include databases, design automation and artificial intelligence

• VMEbus driver configured for Sun-4/SPARCserver™ type expansion interface allowing the use of existing Sun-compatible VMEbus device drivers

ONC is the industry standard for heterogeneous networking. OpenWindows is the network-extensible graphical application development platform. OPEN LOOK is an intuitive graphical user interface, and Deskset is a suite of personal and workgroup productivity applications.

1.13 Development

By using the SPARC CPU-2CE as both the development and the target system, equipment costs and time-to-market can be reduced. Solaris on the SPARC CPU-2CE provides all the tools necessary to take a project from conception through delivery. This includes: project planning aids (e.g. mail, diary, print facilities, etc.); design aids (e.g. compilers, assemblers, debuggers, and libraries); test facilities (e.g. compliance checkers, performance monitors, profilers, and system diagnostics); documentation tools (e.g. text formatters, print filters, and PostScript® interfaces); archiving and maintenance (e.g. source-code control systems, archivers, and backup systems); and others.

Optimizing compilers available from Sun include: C, C++, FORTRAN-77, Pascal, Modula-2, and Common Lisp. Independent software developers furnish many other languages, including Ada, APL, BASIC, COBOL, Forth, Mainsail, PL/I, and Prolog. Sun languages have full access to systems, graphics, networking, and user interface packages. Third-party cross compilers allow C, FORTRAN, or Pascal programmers to produce executable binary code for multiple architectures from a single FORCE SPARC CPU-2CE.

1.14 Sun Tools

Standard software provided with Solaris includes a powerful user interface. This allows access to Solaris resource management functions, as well as industry- standard UNIX editors, command shells, and all UNIX commands for file management and manipulation, system administration, I/O system control, and other software development tools.

1.15 Graphical User Interface

OpenWindows is a full-featured windowing environment based on the X-Window Standard and the Network extensible Windowing System (NeWS™). OPEN LOOK is a graphical user interface that uses X-Windows and NeWS to provide an intuitive, "look and feel" desktop. The DeskSet is a group of personal productivity tools and system service applications which includes a File Manager, Calendar, Debugger, Mailer, and others.

1.16 Real-Time

The SPARC CPU-2CE with Solaris, which supports a wide range of VMEbus and SBus-based hardware and software solutions, creates an ideal embedded system. New releases of Solaris will provide the SPARC CPU-2CE with real-time extension for use in "soft" real-time applications. These extensions include: fixed priority processes, priority manipulation, pre-emptive scheduling, process priority inheritance, guaranteed dispatch latency and memory locking.

Several hard real-time operating systems are available for or are being ported to the SPARC CPU-2CE. These typically provide high-speed multi-tasking, pre-emptive scheduling, and fast interrupt response. They include facilities for intertask communications and synchronization, efficient memory management, system clock and timing, optimized floating point support, and high-performance I/O and file systems. Real-time development tools usually include an interactive debug Shell, a linking loader, symbolic debugger, performance monitor, exception and signal handling, libraries, utility routines, extensive system and task information utilities, and source level debuggers.

1.17 Networking

ONC networking environment is a suite of software modules and services that are the de facto standard for distributed computing. FORCE COMPUTERS provides a VMEbus driver utility as a standard item in conjunction with the Solaris operating system. This driver combines the standard Sun-4 SPARCserver treatment of the VMEbus expansion interface with the additional capability to run ONC over the VMEbus backplane. This provides an optimal platform for both tightly coupled networking and distributed processing applications, as well as the ability to utilize existing drivers for add-in VMEbus peripheral controllers.

The Remote Procedure Call (RPC) is the core of ONC and is used to build services such as the Network File System (NFS™), Network Information Service (NIS) and Network System Boot.

Solaris also supports an extensive set of networking tools that allow developers to take advantage of industry standards. Solaris supports internet protocols, including raw (IP), datagram (UDP/IP) and stream (TCP/IP). User-accessible interfaces allow development of custom interfaces and protocols. Sun will also offer a Solaris Serial Line Internet Protocol (SLIP) for serial line_based wide-area networks (WANs).

Optional software provides support for: DECnet; SNA, including IBM's Advanced Program-to-Program Communications (APPC) and Document Interchange Architecture (DIA); OSI support which adheres to MAP 2.1 and TOP 1.0 specifications, Layers 1 through 7 for MAP applications; FTAM (File Transfer Access and Management); and CASE (Common Application Services Elements).

Table: 1.1 Board Function & Specification

Central Processing Unit	SPARC RISC
Clock Frequency	40 MHz
Integer Performance	28.5 MIPS
Floating Point	4.2 MFLOPS @ 40 MHz Double Precision
Block Transfer DMA	50 Mbytes/sec (80 Mbyte/sec peak)
Cache: Data & Instruction	64 Kbytes
Basic DRAM TSOP Capacity	16 Mbytes
Error Detection	Byte Parity
Local DRAM Expansion (Single Slot)	16, 32, 48 via mezzanine
Maximum On-Board DRAM	64 Mbytes
SRAM (Battery Backed Up)	8 Kbytes
MMU	Sun-4 MMU ASIC
SBus Expansion	2 Slots
VMEbus	32-bit IEEE/ANSI-standard
VMEBus Master	A32, A24, A16: D8, D16, D32, RMW
VMEBus Slave	A32, A24: D8, D16, D32, RMW, BLT
VMEBus Interrupt Handler	1 through 7 (Selectable)
VMEBus Arbiter	4 level SGL
Mutiprocessor Mailbox	Yes (A16 access)
Ethernet (IEEE 802.3)	7990 Lance, AMD 7992B SIA
Ethernet Transfer Rate	10 Mbits/sec
SCSI Controller	NCR 53C90A and S4 DMA+
SCSI Transfer Rate	ASYC 1.5 Mbyte/sec, SYNC up to 5 Mbyte/sec
Serial Ports	2 Async/Sync; RS-232-C/RS-423
Serial Data Rates	64 Kbaud
NVRAM TOD Clock/Calendar	MK 48T08
EPROM Size	2 Mbyte, 8-bit wide
FLASH EEPROM Size (Optional Feature)	1 Mbyte, 32-bit wide
Reset Switch	Yes
Abort Switch	Yes

Hex Rotary Switch, switch input port	1
LEDs	2 (bi-color Red/Green)
Programmable Timers	2
Watchdog	Yes
Keyboard/Mouse Port	Sun-4 Standard
Floppy Disk Controller	Intel 82072
Audio Controller	AMD 79C30
CD ROM Support	Yes
Front Panel	Yes
Power Requirements + 5V	4 Amps (W/O Optional SBus Cards)
+12 V	0.1 Amp /max .6 Amp
-12 V	0.1 Amp /max 0.2 Amp
2A Minifuse	Schurter P/N 3402.0012.xx
630ma Minifuse	Schurter P/N 3402.0008.xx
Number of VME Slots Used	1
Board	14 Layers
Board Dimensions	6.29" X 9.18" (160 x 233 mm)
SunOS or UNIX™ Operating System	4.1.1 or SunOS/Solaris or current
Warranty	1 Year

See the ordering information table on the next page for adapters available from FORCE. Contact your local sales office for additional options.

Table: 1.2 Removed

This page is intentionally left blank.

This page is intentionally left blank.

Table: 1.3 Compatiable Peripherials

Tape Drive	Archive 2150s	1/2" cartridge drive
Tape Drive	Exabyte 8200	8mm cartridge 2.5 GB
Tape Drive	Exabyte 8500	8mm cartridge 5 GB***
Floppy Drive	Sony F17W-FP	3 1/2" 1.44 MB
Hard Drive	Maxtor LXT-213SY	210 MB 3 1/2 inch SUN 207
Hard Drive	Segate ST1480N	424 MB 3 1/2 inch SUN424*
Hard Drive	SEgate ST4766N	669 MB 5 1/4 inch SUN669
Hard Drive	Segate ST41200N	1.GB 5 1/4 inch SUN1.0G**
Hard Drive	Segate ST41600N	1.3 GB SUN1.3G*
CDROM	Sony CDU-8012	

* Not in SUNOS 4.1e
** Not in SUNOS 4.1.1b
*** Only Supported in SUNOS 4.12

1.18 Determining Revision Level

You can determine the revision code and serial number of a SPARC CPU-2CE by inspecting the label attached to the P1 connector of each card.

Section 2

INSTALLATION and DIAGNOSTICS

WARNING

TO AVOID MALFUNCTIONS AND COMPONENT DAMAGE, PLEASE READ THE COMPLETE INSTALLATION PROCEDURE BEFORE THE BOARD IS INSTALLED IN A SYSTEM ENVIRONMENT.

STATIC KILLS

2.1 Power Up

This chapter will cover the instructions and considerations for powering up to insure proper operation of the CPU-2CE.

The only mechanical jumper blocks for the CPU-2CE are to configure the serial ports and to configure the VME. The serial ports are RS-232-C or RS-423 with the default being RS-232-C. If RS-423 is needed, set the block before power up. Move the jumpers position to set RS-423. Both ports must be set identical as either RS-232 or RS-423. The VME default is VME slot 1 device with the jumper installed in JMP1. Removing Jumper 1 selects the card to be non-slot 1 VME device. VME backplane must be terminated according to spec.

Backplane Slot Configuration Requirements

The SPARC CPU-2CE can be plugged into any VMEbus slot. If a SPARC CPU-2CE is installed in a slot other than 1 with empty slots between it and the slot 1 controller. Each of the empty slots must be configured as described below. See your backplane manual for documentation on the location of these jumpers.

Jumper IACKIN* to IACKOUT* on the backplane:

Pins A21 and A22 on the backplane must be jumpered together.

The signals Bus Grant [0:3] must be jumpered across empty slots, as follows:

BGO: jumper pins 4 and 5 Row B

BG1: jumper pins 6 and 7 Row B

BG2: jumper pins 8 and 9 Row B

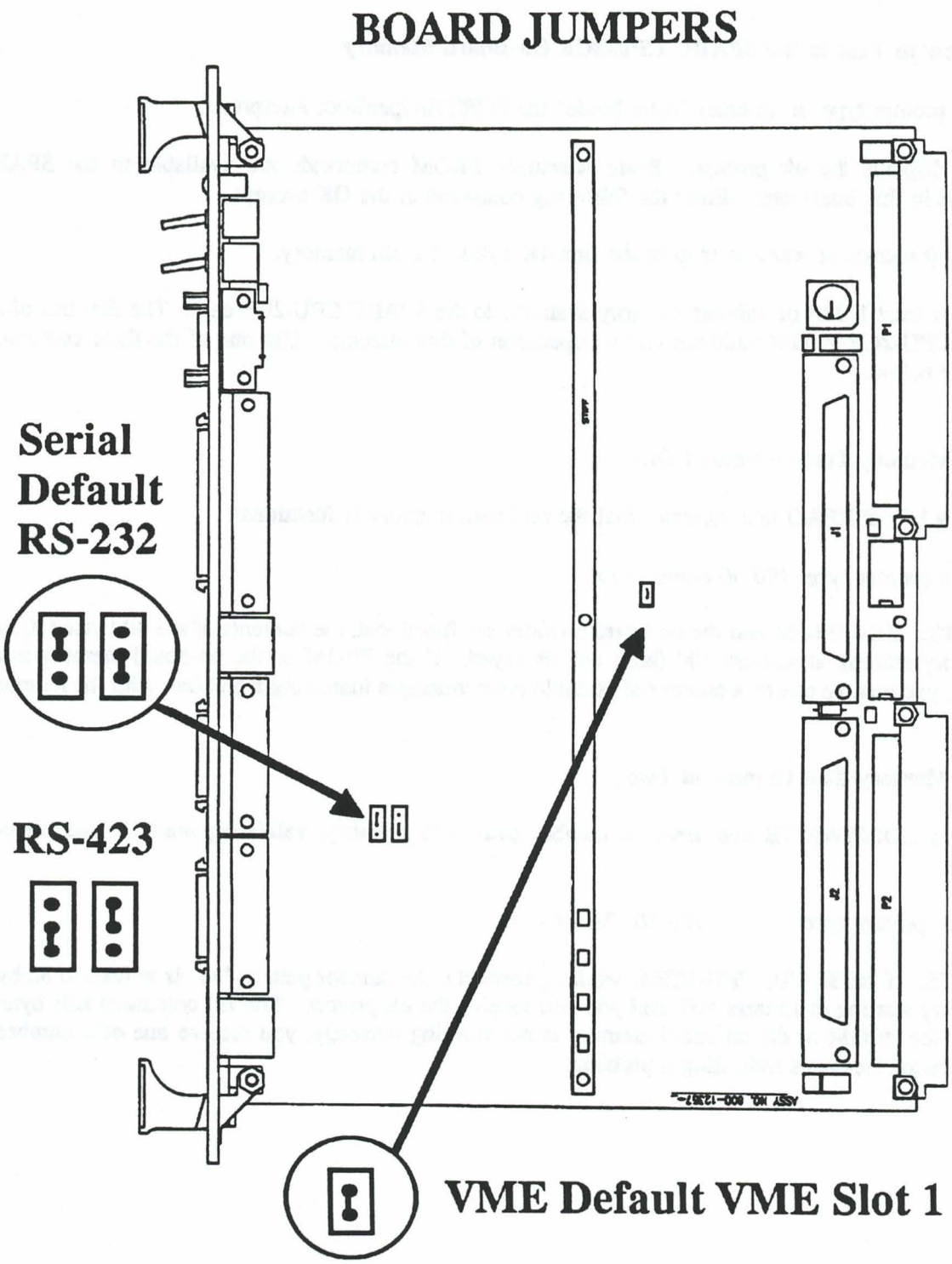
BG3: jumpered pins 10 and 11 Row B

The CPU-2CE can power up without a computer terminal and keyboard, but you cannot enter the appropriate commands to test the card without a means to enter commands and view the results. FORCE recommends the initial power up to be performed with a computer terminal connected to serial port A of the CPU-2CE. By using the computer terminal, additional possible error producing factors; a nonfunctioning SBus card, SBus frame buffer card connector, or monitor can be detected. Connecting a terminal is simpler than connecting a frame buffer, monitor, and keyboard. The optional serial cable is available by ordering the accessories kit.

The power-up sequence consists of a series of component functional tests and initialization, followed by booting. Turn on the power to the backplane.

In the default autoboot mode, the SPARC CPU-2CE attempts to boot SunOS from an attached SCSI disk. If a disk is not attached, the Open PROM displays an identification banner and enters the command mode of the "PROM Monitor" (a program that monitors the activity of the keyboard). The PROM displays a > prompt.

Figure: 2.1 RS-232/423 Jumper Blocks



2.2 Post Power Up Procedures

2.2.1 How to Talk to the SPARC CPU-2CE On-Board Memory

At the > prompt type *n* to enter "New Mode" the FORTH/OpenBoot interpreter.

FORTH displays the **ok** prompt. Basic Assembly PROM commands are available to the SPARC CPU-2CE in this interpreter. Enter the following command at the OK prompt.

0 obmem 0 map-page <cr> to map in the first 4K bytes of main memory.

There is at least 16MB of onboard memory available to the SPARC CPU-2CE card. The first test of the SPARC CPU-2CE PROM validates correct operation of this memory. Use one of the three commands explained below:

2.2.1.1 Memory Test Command One

Perform a LOOP/READ that validates that the on-board memory is functional:

At the **ok** prompt type *100 50 dump <cr>*

RESULTS: If the PROM and the on-board memory are functional, the contents of the 80 bytes (50 hex) of memory starting at address 100 (hex) are displayed. If the PROM or the on-board memory is not working, you receive one of a number of possible error messages indicating a problem with the memory.

2.2.1.2 Memory Test Command Two

Perform a LOOP/WRITE that writes a number pattern to memory, validating memory and memory response:

At the **ok** prompt type *100 50 78 fill <cr>*

RESULTS: If the SPARC CPU-2CE is working correctly, the number pattern "78" is written to 80 bytes of memory starting at address 100, and you will receive the **ok** prompt. The fill command fills byte by byte. If the PROM or the on-board memory is not working correctly, you receive one of a number of possible error messages indicating a problem.

2.2.1.3 Memory Test Command Three

Perform a memory test that exercises the on-board memory. This test does not reside in the PROM, and must be keyed in at the FORTH prompt. (Memory must be mapped according to section 2.2.1)

Key in the following program:

```
: memory-test ( -- )
    150 100 do                          \from 0x100 to 0x150
      12345678  i 1!                    \longword write
      i 1@ dup                          \longword read (result left
                                        \on stack)

      12345678 <>                       \compare
      if ." obs = " .
         ." exp = " 12345678 .
         ." adr = " i . cr
      then
      drop
    4 +loop
;
```

When this code has been correctly entered, you can perform the memory test:

memory-test <cr>

Also, the following command runs the Open Boot memory test:

test /memory or *test-memory*

This test is the same as the Open Boot POST test and will take approximately 4 minutes for 32 megabytes.

RESULTS: If the SPARC CPU-2CE is working correctly, the memory is erased and tested, and you will receive the ok prompt. If the PROM or the on-board memory is not working correctly, you receive one of a number of possible error messages indicating a problem.

Connect the cables for the additional devices you wish to test with the SPARC CPU-2CE: SCSI, Keyboard, Ethernet, Serial Ports A and B. (Make sure the power is off before connecting any cables to the CPU-2CE.)

2.2.2 Test the Ethernet Port

Test the Ethernet port by connecting a MAU (Medium Access Unit) to the Ethernet port and while in Forth/OpenBoot and typing:

test net <net>

2.2.3 How to Talk to the SPARC CPU-2CE Buses

Access to the devices available on the SPARC buses in general requires mapping, reading, and writing the device. This test is performed only when testing an SBus memory card. The procedure below can be used to map in memory. Devices are mapped in two stages:

2.2.3.1 Mapping Memory

Select unused segments, virtual address range and size. Map in the segments, e.g., seg# = 0x80, va = 0x1000000, size = 0x4000.

80 1000000 0x4000 map-segments <cr>

Select a physical address range and space (SBus Slot2). Map in the page e.g., pa = 0xFC000000, space = SBus.

FC000000 sbus 1000000 4000 map-pages <cr>

2.2.3.2 Accessing Memory

To dump out memory at the ok prompt type *1000 000 50 Dump <cr>*

2.2.4 How to Talk to the SBus

SBus devices are handled using the IDPROM onboard the SBus card. The IDPROM contains a driver for the SBus card which is read at boot time and interpreted by the Open PROM. During debug of an SBus device or it's driver a device in an SBus slot may be mapped in using **map-sbus**. (See the ***Open PROM Toolkit User's Manual*** for a description of the map-sbus).

2.3 Running PROM Diagnostics

Setting the diagnostic switch and resetting the card will cause the card to come-up into the extended selftests.

CAUTION: This command disables the monitor and keyboard and enables Serial Interface A as the I/O device.

type: *setenv diag-switch? true <cr>*

reset type: *reset* or *lift the reset switch* on the front panel. The board will exit automatically.

NOTE: You must have a tty device attached to Serial Port A. Setting the diag-switch to true puts messages to the serial port A console.

2.4 Running Functional Tests

The following tests are available for testing functional units on the CPU-2CE. These tests are automatically run at a reset or a power-up.

The functional test can be run individually by leaving the PROM monitor and entering the FORTH/OpenBoot interpreter.

At the > prompt, enter *n*.

At the ok prompt, enter one of the following commands.

test /memory or test-memory
test /sbus/le
test net
test floppy (requires floppy drive and Sun formatted FD formatted disk)
watch-clock
probe-scsi

NOTE: For a complete listing of diagnostics available from the PROM, type *help diag* or *help test*

2.5 Returning To Monitor Mode

To return to the > prompt from the OK prompt,
enter the following:

ok *old-mode* *<CR>*

2.6 Diagnostics

This chapter describes the different types of diagnostic firmware and software tools available and how they are related.

2.6.1 Main Categories of Diagnostics

- Boot PROM diagnostics
  - Power-On Self-Test
  - On-Board Diagnostics
- Sundiag System Exerciser (SunOS)

This chapter will also briefly cover the Forth/OpenBoot Toolkit, which is an interactive command interpreter based on the Forth programming language. Additional information on the Sun Forth Toolkit can be found in the Open Boot PROM 2.0 Toolkit User's Guide in the SBus Developers Kit.

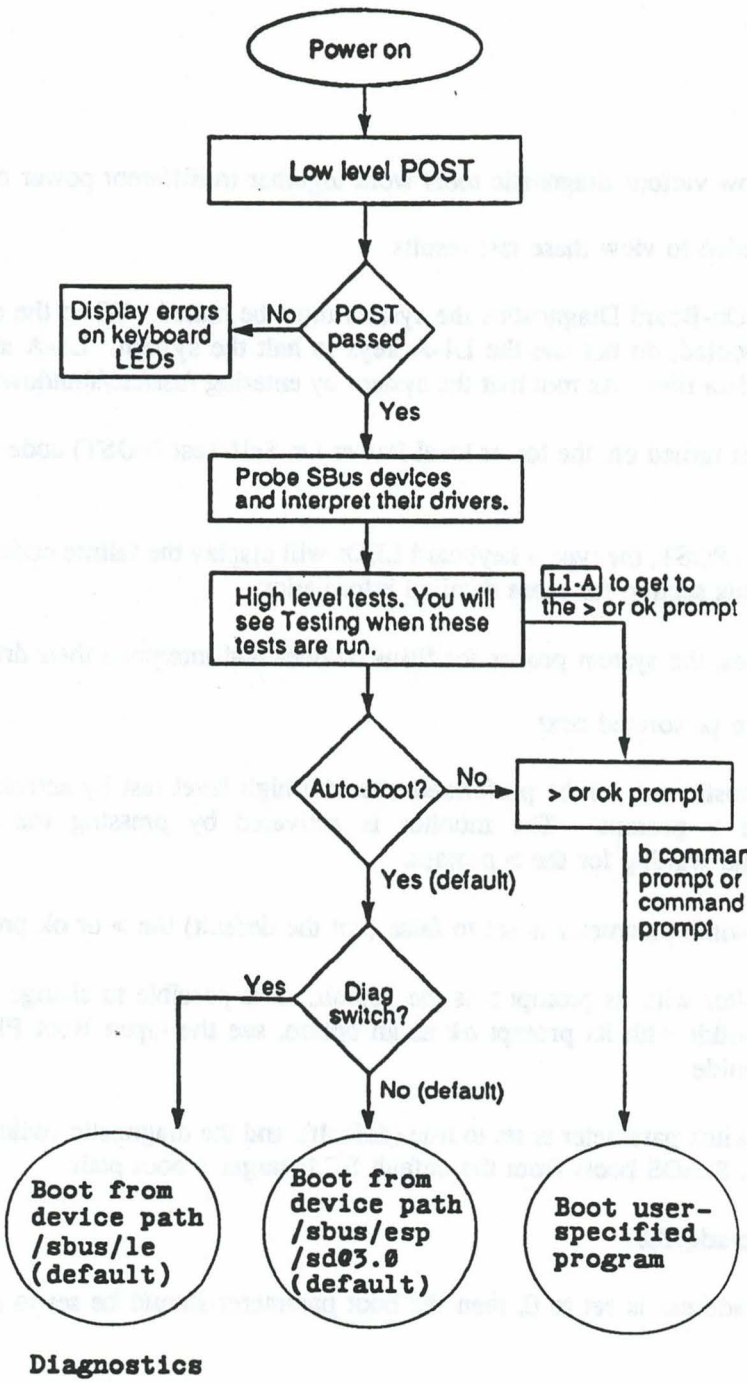
2.6.2 Diagnostic Selections

Table: 2.1 Diagnostic Tools

Diagnostic Tool	When to use
Power On Self Test (POST)	The POST code resides in the boot PROM and is driven automatically by a signal from the power supply when first powered on. The CPU performs the self-test. POST shows if there is a failure of the main components on the main logic board.
On Board Diagnostics	Individual test, ie memory, Ethernet, etc., available when in Forth Toolkit. Enter n from the > prompt to enter the Forth Toolkit. The on board diagnostics reside in the boot PROM.
Sundiag System Exerciser	Using SunOS, it displays realtime use of system resources and peripherals. Sundiag will show if your system is functioning properly. If Sundiag fails, run the Power On Self Test.
Monitor	Monitor will be activated when the system crashes. Monitor is the > prompt. Typing ***b*** boots, ***c*** resumes or continues program halted, or ***n*** to enter Forth Toolkit.
Forth Toolkit	Performs all functions available through the Monitor, except entering the Forth Toolkit i.e. changing the NVRAM parameters, resetting the system, running diagnostics, displaying system information, redirecting input and output, etc. There is more in this chapter and the Open Boot PROM 2.0 Toolkit User's Guide.

Figure: 2.2 POST

FIGURE 2.3 Power On Self Test Flow Chart



Diagnostics

The Forth Toolkit offers an extensive set of functions for performing the following:

- Hardware Development
- Problem Determination (fault isolation)
- Software Development
- Debugging

This section will detail how various diagnostic tools work together in different power on modes.

NOTE: A terminal is needed to view these test results.

CAUTION- To run the On-Board Diagnostics the system must be halted. When the operating system or application has been booted, do not use the L1-A keys to halt the system. L1-A abruptly halts the system and may damage data files. As root halt the system by entering /usr/etc/shutdown or /etc/fasthalt.

- When the power is turned on, the lower level Power On Self Test (POST) code is executed from the Boot PROM.
- If failure occurs in POST, the type 4 keyboard LEDs will display the failure code. See The Power On Self Test in this section for more detailed information.
- If the POST passes, the system probes for SBus devices and interprets their drivers.
- High level test are performed next.
- Specialized diagnostic test can be performed after the high level test by activating the Monitor, indicated by the > prompt. The monitor is activated by pressing the *L1* and *A* keys simultaneously and waiting for the > prompt.
- If the autoboot switch parameter is set to false (not the default) the > or ok prompt will show.

  The monitor with its prompt > is the default. It is possible to change the default to the Forth Toolkit with its prompt ***ok*** as an option, see the Open Boot PROM 2.0 Toolkit User's Guide.

- If the autoboot switch parameter is set to true (default), and the diagnostic switch parameter is set to false (default), SunOS boots from the default SCSI target 3 boot path:

  /sbus/esp/sd@3,0

  If the hard disk address is set to 0, then the boot parameter should be set to /sbus/esp/sd@0,0.

- For normal booting boot /sbus/esp will automatically find and boot the disk.

- If the autoboot switch parameter is set to true (default), and the diagnostics switch parameter is set to true (not the default), SunOS boots from the bootpath:

  /sbus/le

- To boot user-specified programs, such as the SunDiagnostic Executive, you must be at the > or ok prompt. On Board Diagnostics section later in this chapter will detail how to obtain the > and ok prompts with fasthalt.

Table: 2.2 Diagnostic Switches

Autoboot Switch Parameter	Diagnostic Switch Parameter	Result
False	(Don't care)	> or ok prompt
True	False	boot SunOS (vmunix) from SCSI ID 3 (/sbus/esp/sd@3,0)
True	True	boot SunOs (vmunix) from network*(/sbus/le)

* The boot parameters represented here are default settings. The defaults may be changed by following the procedures listed in the Open Boot PROM 2.0 Toolkit User's Guide.

2.6.3 Boot PROM Diagnostics

The diagnostics contained in the boot PROM include the following:

Power-On Self-Test

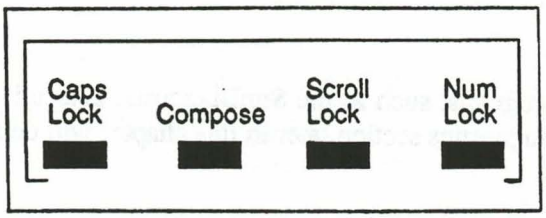
On-Board Diagnostics

2.6.3.1 POST

The Power On Self Test (POST) is the default mode. The POST consist of a sequence of test designed to test the major hardware components of the main logic board before SunOS is booted. Only major failures can be detected by POST. For additional more thorough diagnostics run the extended on-board diagnostics for items including Memory, Ethernet, diskette drives, etc.

Figure: 2.3 Keyboard LED Diagnostic Codes

Arrangement of Sun4 Keyboard LEDs



Sun4 Keyboard LED Diagnostic Code

LED Display Pattern	Unit	Meaning of Pattern
		Unassigned. Testing completed, SunOS is booted.
	Boot PROM	Bad checksum in boot PROM.
	NVRAM/TOD	NVRAM/Time-of-Day Clock failed.
	SPARC 2	SPARC 2 component failed.

2.6.3.2 On Board Diagnostics

1. Save all your work and quite all applications
2. As root, halt the system by entering

/usr/etc/fasthalt

The returning prompt will either be a default prompt > or the prompt **ok**. To change the prompt see the Open Boot PROM 2.0 Toolkit User's Guide.

If you see the > prompt, go to the next step. If you see the **ok** prompt go to step 4.

3. Enter **n** to enter the Forth/OpenBoot Toolkit.

The **ok** prompt signifies the Forth Toolkit mode.

4. Enter **help diag** to get a listing of on-board diagnostic test.

5. To return to the monitor > prompt, type the following command

old-mode

2.6.4 Sundiag System Exerciser

The Sundiag System exerciser verifies that the system is functioning properly. Sundiag runs under SunOs and displays real-time use of system resources and peripheral equipment such as Desktop Storage Packs and External Storage Modules.

Exerciser is shipped with SunOS. If it was selected during SunInstall (operating system loading) procedure, it can be run at any time. The file is found in the directory /usr/diag/sundiag. The file can also be loaded from tape or CD. You must also have Sunview and the file userdiag loaded on your disk. Become root on your system then type sundiag. See the Sundiag User's Guide for further information.

2.6.5 Monitor and Forth Toolkit

The Monitor is a basic diagnostic utility. If there is a problem with the operating system the Monitor will automatically start, indicated by the > prompt.

Table: 2.3 Non-Volatile System Configuration Parameter Defaults

Parameter Name	Default Value
selfest-#megs	1
oem-logo	
oem-logo?	false
oem-banner	
oem-banner?	false
output-device	screen
input-device	keyboard
sbus-probe-list	0123
keyboard-click?	false
keymap	
ttyb-rts-dtr-off	false
ttyb-ignore-cd	true
ttya-rts-dtr-off	false
ttya-ignore-cd	true
ttyb-mode	9600,8,n,1,-
ttya-mode	9600,8,n,1,-
diag-file	
diag-device	net
boot-file	
boot-device	disk
auto-boot?	true
watchdog-reboot	false
fcode-debug?	false
local-mac-address?	false
use-nvramrc?	false
nvramrc	
screen-#columns	80
screen-#rows	34

sunmon-compat?	true
security-mode	none
security-password	
security-initiator-id	7
hardware-revision	
last-hardware-update	
testarea	0
mfg-switch?	false
diag-switch?	false

Table: 2.4 NVRAM VME Configuration Parameters

Parameter	Description	Def
vme-slavemap	Address space for system DVMA access	0
vme-a32map	Re-map VMe address bits A[31:29]	0
vme-intena	Interrupt enable register	254
vme-mailbox	Select VME address for mailbox interrupt	0
vme-buslock	Enables atomic RMW	0
net-boot-device	Selects network device to boot from	le()
vm-server-slavemap	Client's server slavemap address	0
vm-server-addr	Client's server internet address	0
vm-ip-addr	Client's internet address	0
next-prom	If true, jump to second PROM on exit from first	false

2.7 SPARC CPU-2CE-Unique NVRAM Parameters

This section lists and defines the NVRAM parameters unique to SPARC CPU-2CE architecture. Each parameter will be presented in the following format:

parameter [options][default]
parameter and a description of the parameter's function.

vme-slavemap [range:0-15][0]
vme-slavemap selects a one megabyte space for system DVMA access. vme-slavemap will select one of the first 16 MB of VME space.

vme-a32map [0x0,0x20,0x40,0x60,0x80,0xa0,0xc0,0xe0][0]
vme-a32map remaps VME address bits A[31:29] enabling full 4GB mapping.

vme-intena [0-255][254]
vme-intena selectively enables VME interrupt levels by setting a bit mask that corresponds to the Interrupt Enable Register. The default value of 0xfe enables all intertupts and disables Round-Robin Arbitration.

vme-mailbox [0-255][0]
vme-mailbox selects a VME address to be monitored. If enabled, generates a mailbox interrupt to the IU by way of an on-card interrupt. This mailbox detects accesses to A16 address space at a location programmed in the Mail Box register. No real memory is provided at this location, but the mailbox responds with a VME DTACK, acknowledging the access and generating a level 13 interrupt if the enable bit is set.

vme-buslock [0,1][0]]
vme-buslock is a bus locker function that enables the CPU to do an Atomic Read-Modify-Write (RMW) to its on-card memory without being interrupted by an incoming RMW form another VMEbus master. This parameter should only be used in a multiprocessing environment.

vm-server-slavemap [0-15][0]
vm-server-slavemap sets the slavemap location of the client's server. See the **SunOS 4.1e Release Manaul, ONC/VME** and the description of vme-slavemap above.

vm-server-address [internet address][0]
vm-server-address is the internet address of the client's server. This address is made up of four hexadecimal numbers expressed in decimal form. For example, the number 199.9.9.1 (all decimal numbers), converts to the hexidecimal value 0xc7090901. See the **SunOS 4.1e Release Manaul, ONC/VME.**

vm-ip-addr [internet address][0]
vm-ip-addr is the internet address of the client. This address is made up of four hexadecimal numbers expressed in decimal form. For example, the number 199.9.9.1 (all decimal numbers), converts to the hexidecimal value 0xc7090901.

Table: 2.5 Front Panel

LEGEND	DESCRIPTION
SWLED (A,B)	2 software controlled LEDs
Reset	Resets the Board
Abort	Aborts Process
ENET	Ethernet 15 pin Micro-D connector
KBD	Keyboard, mouse circular DIN connector
Serial A	26 pin connector for serial ports
Serial B	26 pin connector for serial ports
AUDIO	Audio circular DIN connector
SCSI	SCSI-II 50 pin Micro-D connector

Table: 2.6 CPU-2CE Connectors

FUNCTION	Board Manufactures PN Front Panel	Cable Mate Mfg Part #
SCSI-II	AMP 749831-5	AMP 749621-5
Ethernet	ITT CANNON MDSM-15PE-Z10	ITT CANNON MDSM-15PE_Z11
Serial I/O	AMP 749830-2	AMP 749621-2
Audio	AMP 749232-1	AMP 750208-2
Keybd, Mouse	AMP 749232-1	AMP7502 08-2

Figure: 2.4 Font Panel

CPU-2CE FRONT PANEL

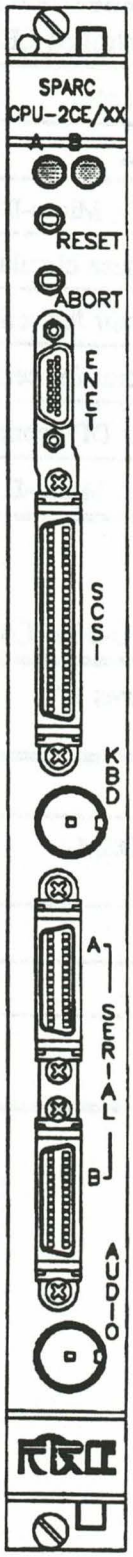


Figure: 2.5 Component Side

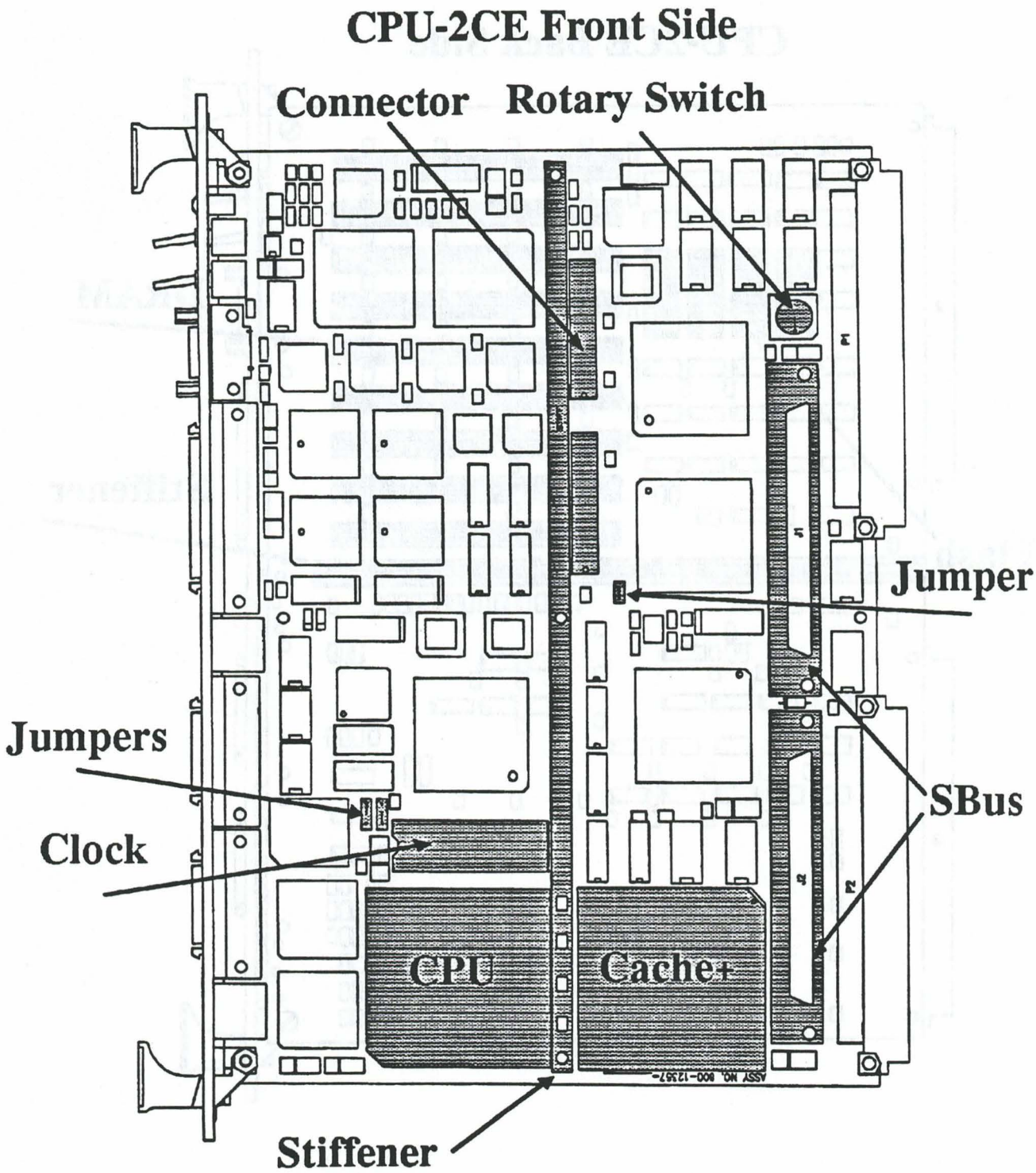


Figure: 2.6 Solder Side

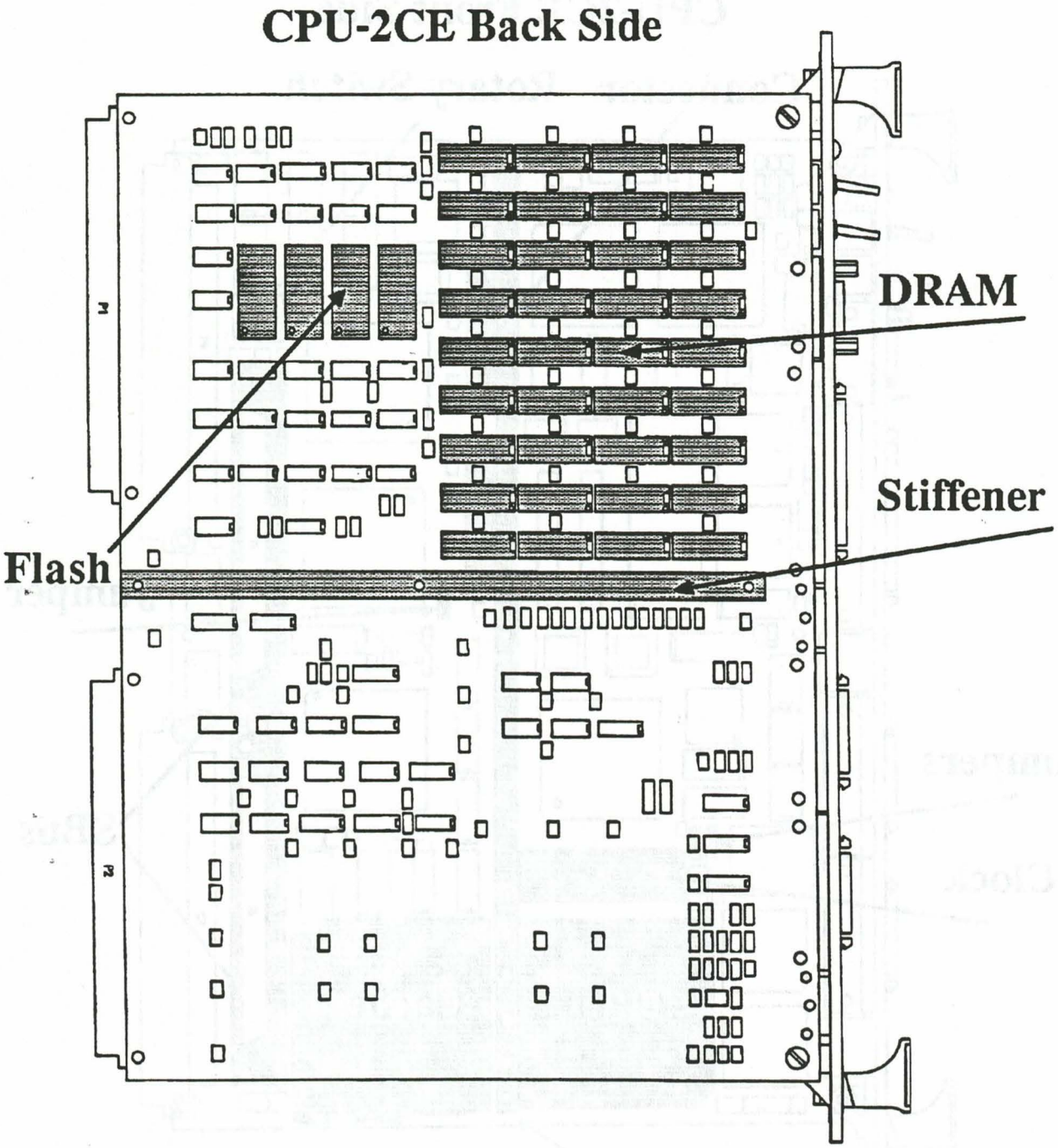
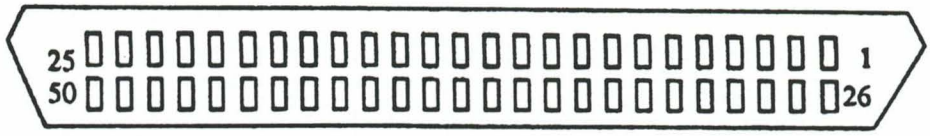


Table: 2.7 SCSI Pinout List

Type	Pin #	Comment	Type	Pin #	Comment
GND	1	Ground	SD0-	26	SCSI Data0-
GND	2	Ground	SD1-	27	SCSI Data1-
GND	3	Ground	SD2-	28	SCSI Data2-
GND	4	Ground	SD3-	29	SCSI Data3-
GND	5	Ground	SD4-	30	SCSI Data4-
GND	6	Ground	SD5-	31	SCSI Data5-
GND	7	Ground	SD6-	32	SCSI Data6-
GND	8	Ground	SD7-	33	SCSI Data7-
GND	9	Ground	SDP-	34	SCSI Parity-
GND	10	Ground	GND	35	Ground
GND	11	Ground	GND	36	Ground
NC	12	No Connect	NC	37	No Connect
NC	13	No Connect	TRMPWR	38	Term. Power (+5V DC, Fused, 3 Amps)
NC	14	No Connect	NC	39	No Connect
GND	15	Ground	GND	40	Ground
GND	16	Ground	ATN-	41	Attention-
GND	17	Ground	NC	42	No Connect
GND	18	Ground	BSY-	43	Busy-
GND	19	Ground	ACK-	44	Acknowledge-
GND	20	Ground	RST-	45	Reset-
GND	21	Ground	MSG-	46	Message-
GND	22	Ground	SEL-	47	Select-
GND	23	Ground	CD-	48	Command/Data-
GND	24	Ground	REQ-	49	Request-
GND	25	Ground	IO-	50	Input/Output-

Figure: 2.7 SCSI Connector and Pins (Front View)



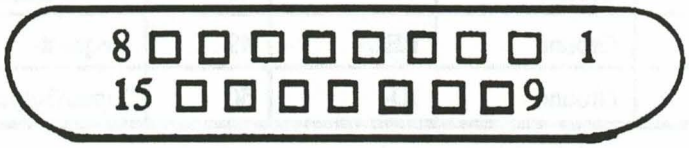
Ethernet Connector Pinout List

The following table is a pinout of the Ethernet connector. Figure 2.8 Shows the Ethernet connector and pin numbers.

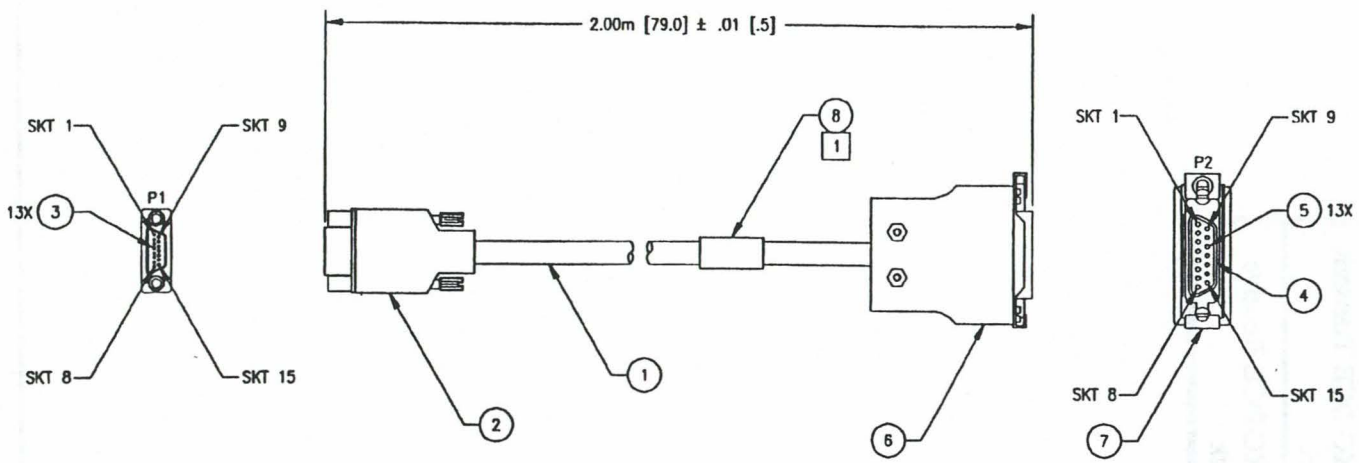
Table: 2.8 Ethernet Pinout List

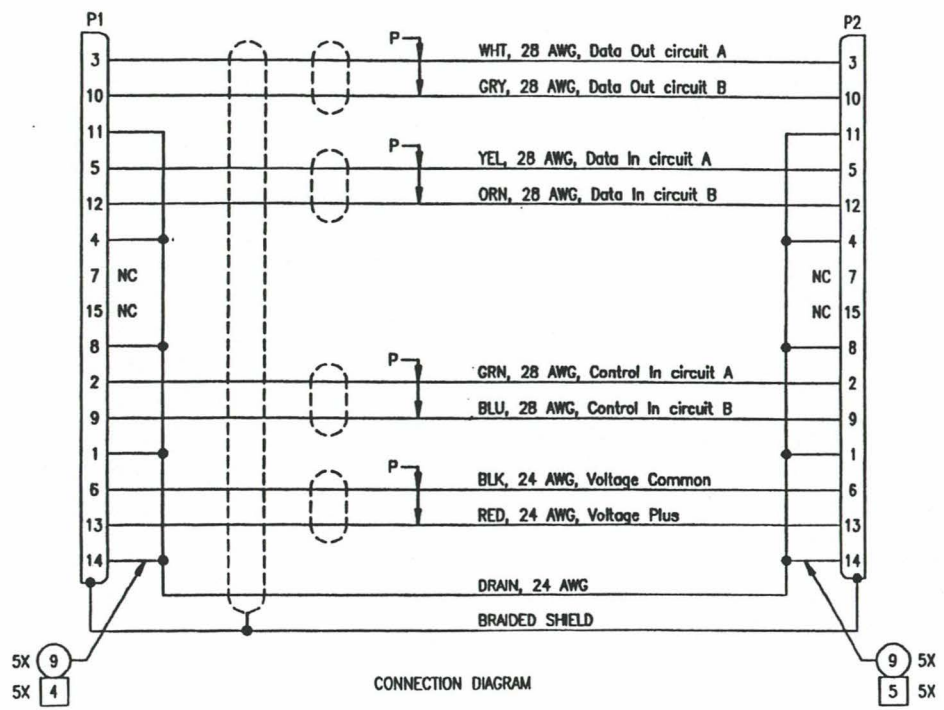
Pin	Function
1	N.C.
2	Collision+
3	Transmit Data+
4	N.C.
5	Receive Data+
6	Ground
7	N.C.
8	N.C.
9	Collision-
10	Transmit Data-
11	N.C.
12	Receive Data-
13	+12VDC
14	N.C.
15	N.C.

Figure: 2.8 Ethernet Cable Connector and Pins (Front View)



REVISIONS					
DASH	REV	DESCRIPTION	BY	DATE	APPROVED
101	A	PRE-PROD RLSE PER ECO 1375	JS	6/92	
101	A1	PROD RLSE PER ECO 1418	JS	8/92	





CONNECTION DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK ASSEMBLY PART NUMBER AND REV LEVEL WITH CONTRASTING PERMANENT COLOR ON ITEM 8 (LABEL) AND LOCATE NEAR CENTER OF CABLE.
2. DIMENSIONS ARE IN METERS, INCHES ARE IN [ ].
3. CABLE WIRING PAIR FOR "Control Out" SIGNALS NOT INCLUDED.
4. SOLDER ONE END OF ITEM 9 (WIRE) TO DRAIN WIRE OF ITEM 1 (CABLE), THEN ATTACH ITEM 3 (CONTACT) TO OTHER END OF ITEM 9.
5. SOLDER ONE END OF ITEM 9 (WIRE) TO DRAIN WIRE OF ITEM 1 (CABLE), THEN ATTACH ITEM 5 (CONTACT) TO OTHER END OF ITEM 9.

PARTS LIST

ITEM NO.	QTY REQ'D	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION
9	AR		9028	WIRE, BLACK, 28 AWG	BELDEN
8	1		TAG-22-100	LABEL, ADHESIVE	TYTON
7	1		DA51220-1	SLIDE LATCH KIT	ITTCANNON
6	1		DA121073-150	BACKSHELL, SHIELDED	ITTCANNON
5	13		D110238-478	CONT, SKT, CRIMP, 24-28 AWG	ITTCANNON
4	1		DMA15S-A197-F0	CONN, DSUB, FEM, 15 PIN	ITTCANNON
3	13		MDS-S-TS	CONT, SKT, CRIMP, 26-28 AWG	ITTCANNON
2	1		MDSM-15SC-211	CONN, MICRO-D, FEM, 15 PIN	ITTCANNON
1	2m		9903	CABLE, ROUND, B/C, 4 PR, 28(24) AWG, SHLD	BELDEN

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE: DECIMALS .XX ±.02, .XXX ±.005; ANGLES ±0°-30'

MATERIAL: SEE PARTS LIST

FINISH:

DO NOT SCALE DRAWING

APPROVALS		DATE
DRAWN	J. STODDEN	6/92
RESP. ENGR.		
CHECKED		
ISSUED		

FORCE COMPUTERS INC.
CAMPBELL, CALIFORNIA

CABLE ASSEMBLY,
CPU2 ETHERNET

SIZE	FSCM NO.	DWG. NO.	REV.
C		720-12257-101	A1

SCALE 1=1 | FILE NAME 12257 | SHEET 1 OF 1

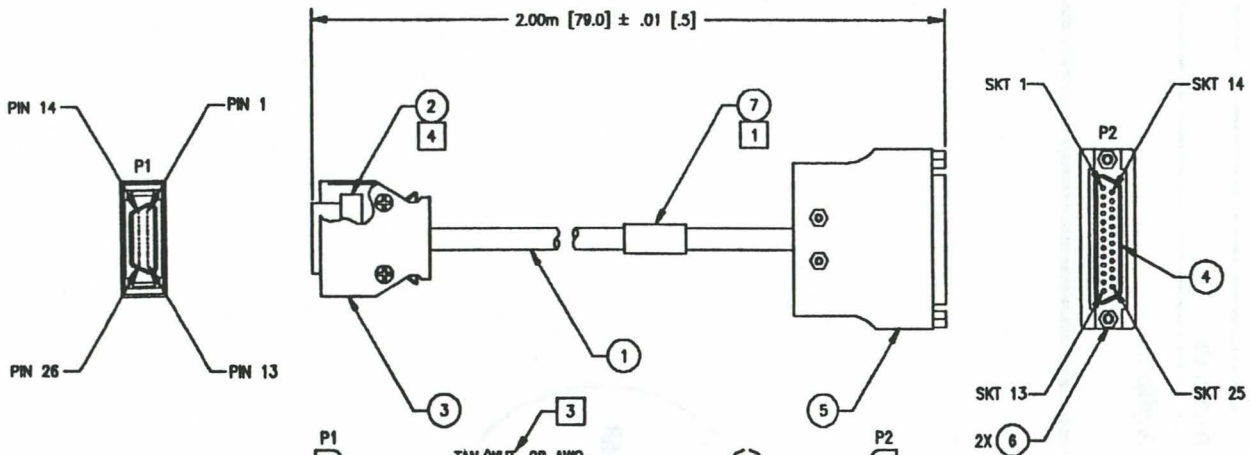
Table: 2.9 Serial Pinout List

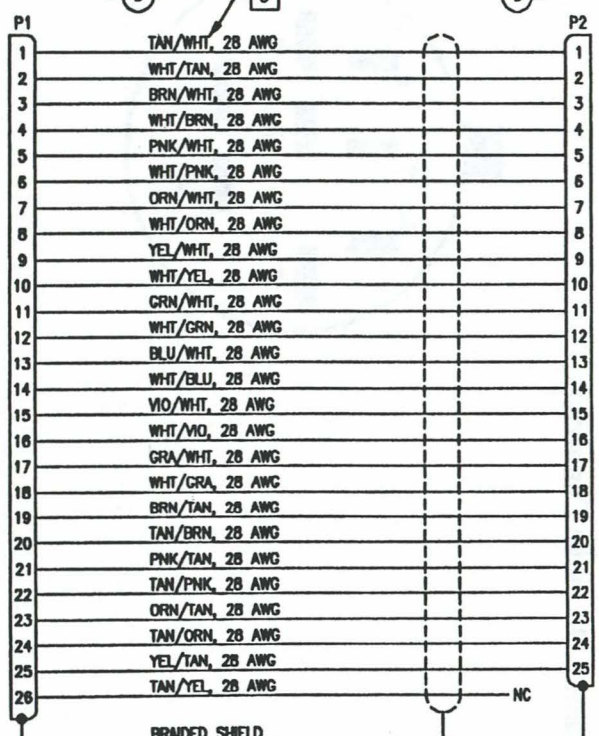
Pin	Transmitted Signals	Pin	Received Signals
2	TxD-Transmit Data	3	RxD- Receive Data
4	RTS-Request To Send	5	CTS-Clear to Send
7	Ground	6	SYNC*
20	DTR-Data Terminal Ready	8	DCD-Data Carrier Detect
24	TRXC-DTE Transmit Clock	15	TRXC-DCE Transmit Clock
		17	RTXC-DCE Receive Clock

* Connector casing is also grounded

DWG. NO. 720-12432-101 | SHT 1 | REV 1

REVISIONS					
DASH	REV	DESCRIPTION	BY	DATE	APPROVED
101	1	PROTOTYPE	JS	7/92	





CONNECTION DIAGRAM

NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK ASSEMBLY PART NUMBER AND REV LEVEL WITH CONTRASTING PERMANENT COLOR ON ITEM 7 (LABEL) AND LOCATE NEAR CENTER OF CABLE.
2. DIMENSIONS ARE IN METERS, INCHES ARE IN [ ].
3. ALL CABLE CONDUCTORS FEATURE A RING BAND STRIPING. THE SECOND COLOR LISTED REPRESENTS THE RING BAND STRIPE.
4. ITEM 2 (PLUG ASSEMBLY) INCLUDES 2 TERMINATING COVERS.

PARTS LIST

ITEM NO.	QTY. REQ'D	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION
7	1		TAD-22-100	LABEL, ADHESIVE	TYTON
6	2		747223-3	SCREWLOCK KIT, FEMALE	AMP
5	1		748676-3	CABLE CLAMP KIT	AMP
4	1		745485-1	RECEPTACLE ASSEMBLY	AMP
3	1		748608-1	BACKSHELL KIT	AMP
2	1		748621-2	PLUG ASSEMBLY	AMP
1	2m		26SDK00025	CABLE, ROUND, 26/C, 28 AWG, SHLD	MADISON

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES ARE: DECIMALS .XX ±.02, .XXX ±.005; ANGLES ±0°-30'

MATERIAL: SEE PARTS LIST

FINISH:

DO NOT SCALE DRAWING

THIS DRAWING IS THE PROPERTY OF FORCE COMPUTERS, INC. AND CONTAINS INFORMATION THAT IS CONFIDENTIAL AND PROPRIETARY TO FORCE COMPUTERS, INC. NO PART OF THIS DRAWING MAY BE COPIED, REPRODUCED OR DISCLOSED TO THIRD PARTIES WITHOUT THE PRIOR WRITTEN CONSENT OF FORCE COMPUTERS, INC.

APPROVALS	DATE
DRAWN J. STODDEN	7/92
RESP. ENGR.	
CHECKED	
ISSUED	

FORCE COMPUTERS INC. CAMPBELL, CALIFORNIA

CABLE ASSEMBLY, CPU-2CE SERIAL

SIZE	FSCM NO.	DWG. NO.	REV.
C		720-12432-101	1

SCALE 1=1 | FILE NAME 12432 | SHEET 1 OF 1

Table: 2.10 Audio Connector (Din 8)

PIN	Description	
1	lin1	
2	lin2	
3	ain-	Audio in
4	lout1	
5	lout2	
6	ain+	Audio in
7	shield	Audio out
8	audio out	

*ISDN signals not supported

Figure: 2.11 Audio Connector

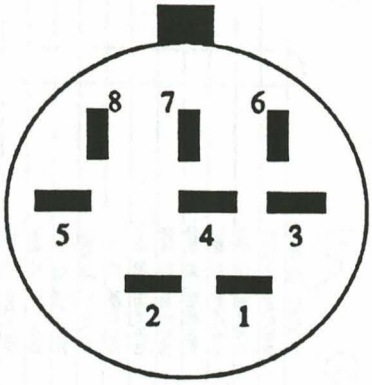


Table: 2.11 Keyboard/Mouse Connector Pinout List

Pin #	Description
1	Ground
2	Ground
3	+5 VDC
4	Mouse In
5	Keyboard Out
6	Keyboard In
7	Ground*
8	+5 VDC
	All signals TTL Levels. +5V current-limited

* All signals TTL Levels. +5V current-limited. May be jumpered to Mouse Output.

Figure: 2.12 Keyboard/Mouse Connector

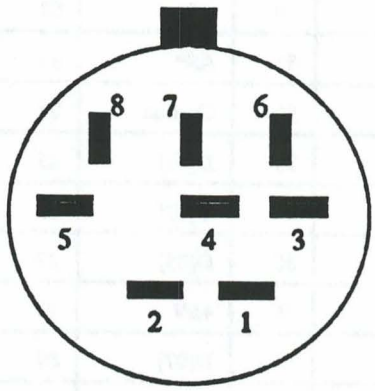


Table: 2.12 SBus Connector Pinout

Pin	Signal	Pin	Signal	Pin	Signal
1	Ground	33	PA[06]	65	D[18]
2	BR*	34	PA[08]	66	D[20]
3	Sel*	35	PA[10]	67	D[22]
4	IntReq[1]	36	err	68	Ground
5	D[00]	37	PA[12]	69	D[24]
6	D[02]	38	PA[14]	70	D[26]
7	D[04]	39	PA[16]	71	D[28]
8	IntReq[2]	40	Ack[1]	72	+5V
9	D[06]	41	PA[18]	73	D[30]
10	D[08]	42	PA[20]	74	Siz[1]
11	D[10]	43	PA[22]	75	Rd
12	IntReq[3]	44	Ack[32]	76	Ground
13	D[12]	45	PA[24]	77	PA[01]
14	D[14]	46	Ground	78	PA[03]
15	D[16]	47	Spare	79	PA[05]
16	IntReq[4]	48	-12V	80	+5V
17	D[19]	49	Clk	81	PA[07]
18	D[21]	50	BG*	82	PA[09]
19	D[23]	51	AS*	83	PA[11]
20	IntReq[5]	52	Ground	84	Ground
21	D[25]	53	D[01]	85	PA[13]
22	D[27]	54	D[03]	86	PA[15]
23	D[29]	55	D[05]	87	PA[17]
24	IntReq[6]	56	+5V	88	+5V
25	D[31]	57	D[07]	89	PA[19]
26	Siz[0]	58	D[09]	90	PA[21]
27	Siz[2]	59	D[11]	91	PA[23]
28	IntReq[7]	60	Ground	92	Ground
29	PA[00]	61	D[13]	93	Ground
30	PA[02]	62	D[15]	94	Ground
31	PA[04]	63	D[17]	95	Reset*
32	LErr*	64	+5V	96	+12V

Table: 2.13 P1 Bus Pinout List

Signal	Row A	Signal	Row B	Signal	ROW C
D(0)	1	BBSY*	1	D(8)	1
D(1)	2	BCLR*	2	D(9)	2
D(2)	3	ACFAIL*	3	D(10)	3
D(3)	4	BGIN(0)	4	D(11)	4
D(4)	5	BGOUT(0)	5	D(12)	5
D(5)	6	BGIN(1)	6	D(13)	6
D(6)	7	BGOUT(1)	7	D(14)	7
D(7)	8	BGIN(2)	8	D(15)	8
GND	9	BGOUT(2)	9	GND	9
SYSCLK	10	BGIN(3)	10	SYSFAIL*	10
GND	11	BGOUT(3)	11	BERR*	11
DS1*	12	BR(0)	12	SYSRESET*	12
DS0*	13	BR(1)	13	LWORD*	13
WRITE*	14	BR(2)	14	AM(5)	14
GND	15	BR(3)	15	A(23)	15
DTACK	16	AM(0)	16	A(22)	16
GND	17	AM(1)	17	A(21)	17
AS*	18	AM(2)	18	A(20)	18
GND*	19	AM(3)	19	A(19)	19
IACK*	20	GND	20	A(18)	20
IACKIN*	21	SERCLK	21	A(17)	21
IACKOUT*	22	GNDSERDAT*	22	A(16)	22
AM (4)	23	GND	23	A(15)	23
A(7)	24	IRQ(7)	24	A(14)	24
A(6)	25	IRQ(6)	25	A(13)	25
A(5)	26	IRQ(5)	26	A(12)	26
A(4)	27	IRQ(4)	27	A(11)	27
A(3)	28	IRQ(3)	28	A(10)	28
A(2)	29	IRQ(2)	29	A(9)	29
A(1)	30	IRQ(1)	30	A(8)	30
-12 VDC	31	+5 VSTBY	31	+12 VDC	31
+5 VDC	32	+5 VDC	32	+5 VDC	32

Table: 2.14 P2 Bus Pinout List

Signal	Row A	Signal	Row B	Signal	Row C
SCSI_DATA0	1	+5 VDC	1	NC	1
SCSI_DATA1	2	GND	2	fp4	2
SCSI_DATA2	3	P1_RETRY*	3	NC	3
SCSI_DATA3	4	P1_A(24)	4	fp8	4
SCSI_DATA4	5	P1_A(25)	5	drvsel	5
SCSI_DATA5	6	P1_A(26)	6	NC	6
SCSI_DATA6	7	P1_A(27)	7	NC	7
SCSI_DATA7	8	P1_A(28)	8	fp16	8
SCSI_DATA8	9	P1_A(29)	9	fp18	9
GND	10	P1_A(30)	10	fp20	10
SCSI_BP*	11	P1_A(31)	11	fp22	11
GND	12	GND	12	fp24	12
TERMPWR	13	+5 VDC	13	fp26	13
GND	14	P1_D(16)	14	fp28	14
GND	15	P1_D(17)	15	fp30	15
SCSI_CNTR2	16	P1_D(18)	16	fp32	16
GND	17	P1_D(19)	17	fp34ct	17
SCSI_CNTR1	18	P1_D(20)	18	feject	18
SCSI_CNTR3	19	P1_D(21)	19	NC	19
SCSI_CNTR5	20	P1_D(22)	20	NC	20
SCSI_CNTR6	21	P1_D(23)	21	NC	21
SCSI_CNTR0	22	GND	22	NC	22
SCSI_CNTR7	23	P1_D(24)	23	NC	23
SCSI_CNTR4	24	P1_D(25)	24	NC	24
SCSI_CNTR8	25	P1_D(26)	25	NC	25
spkr1	26	P1_D(27)	26	NC	26
led_out	27	P1_D(28)	27	NC	27
spkr2	28	P1_D(29)	28	NC	28
NC	29	P1_D(30)	29	NC	29
NC	30	P1_D(31)	30	NC	30
NC	31	GND	31	NC	31
NC	32	+5 VDC	32	NC	32

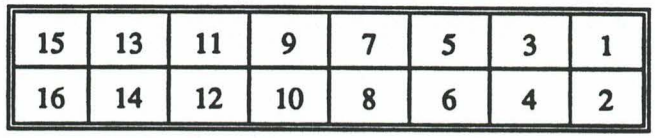
Expansion Connector Mechanical Layout

The Expansion Connector is an 8-pin header on 0.1" centers with the following pinout:

Table: 2.15 Expansion Connector Electrical Pinout

Pin #	Function	Signal Description
1	Pa26	SBus physical address line 26
2	ramclk1	A 20 MHz clock for a SS-2 ram controller. It has a 25-75 duty cycle.
3	ramsel1*	Second ram controller chip select. Asserted low whenever a virtual address translates to a legal page in Type0 address space between 0x8000000 and 0xFFFFFFF (pa27 high).
4	Ground	Logic ground for the system
5	ParCS1*	Parity register chip select for second ram controller. Asserted low whenever a virtual address translates to a valid page in Type1 space with a physical address of 0xF4000008 - 0xF400000F.
6	RamClk	A 20 MHz clock for an SS-2 ram controller. It has a 75-25 duty cycle.
7	Pa25	SBus physical address line 25.
8	PErr*	Parity Error signal. This open drain signal is similar to the SBus signal **LErr*** except that it must meet SBus timings *with the data in error*, rather than one clock later.
9	Pa27	
10	EXMP	
11	GND	
12	VCC	
13	GND	
14	VCC	
15	GND	
16	VCC	

Figure: 2.13 Sun Expansion Connector Pin Orientation



Section 3

GLOSSARY

• SPARC CPU-2CE Hardware Documentation Glossary

The manuals listed below are available for the SPARC CPU-2CE outside of FORCE through Sun. These manuals provide information about the other cards that currently make up the SPARC CPU family.

Table: 3.1 SPARCengine Reference Materials Available from Sun

Sun Part No.	Title	Type
800-1736-xx	***PROM User's Manual***	SunOS Documentation
800-5480-xx	***Release Manual for SunOS 4.1.1***	SunOS Documentation
800-1399-xx	***The SPARC Architecture Manual***	SunOS Documentation
850-1930-xx	***SBus Developer's Kit***	
800-5322-xx	***SBus Device Drivers Manual***	SBus Developer's Kit
800-4456-xx	***SBus FORTH Drivers Manual***	SBus Developer's Kit
800-5323-xx	***SBus Specification A.2***	SBus Developer's Kit
800-5279-xx	***PROM Toolkit User's Guide***	SBus Developer's Kit
800-5280-xx	***PROM Toolkit Reference Summary***	SBus Developer's Kit
825-1219-xx	***Open Boot PROM Toolkit User's Manual***	SBus Developer's Kit
800-3817-xx	***SUNDIAG User's Manual***	
800-xxxx-xx	***The SPARCengine 2 Color & Monochrome Video Cards User's Manuals***	

Open Boot 2.0 Contact Sun's SBUS Development Group

Summit Group Distributor Phone: (408) 395-9522 ***Sun Catalyst Catalog***

Table: 3.2 Documentation Available Other Places

Cypress CY7C600 Technical Manual Cypress Semiconductor

Signetics NE5170 Octal Line Driver Technical Manual, Signetics, December, 1988

Toshiba TC55464P/J-20 Static Random Access Memory Technical Manual, Toshiba

VMEbus Specification Revision C.1, 1987.

• **Suggested Reference Material for the SCSI Interface**

SCSA (SUN Common SCSI Architecture) Sun Part Number: 800-4701-XX

SCSI Implementation Guide SUN Common SCSI Architecture Sun Part Number: 800-4700-xx

NCR 53C90 Enhanced SCSI Processor Data Sheet,
(SCSI Registers Definition), NCR Corporation, November 87.

SCSI, Understanding the Small Computer System Interface
NCR Corporation, Prentice-Hall, 1990

ANSI Specification X3.131_1986
Federal Information Processing Standard (FIPS), X3.131_1986

• **Ethernet Interface**

Am7990 Local Area Network Controller (LANCE) Technical Manual,
Advanced Micro Devices, Inc., 1986.

Am7992B Serial Interface Adapter (SIA) Technical Manual, Advanced
Micro Devices, October, Inc., 1985.

ANSI Specification 802.3, 1986, also known as:

ISO/Draft International Standard 8802/3, February 1989.

Federal Information Processing Standard (FIPS) 107, February 1989.

• **Suggested Reference Material for Serial Interface A/B**

EIA Standard -- RS-232-C, Electronic Industries Association, August, 1969.

EIA Standard -- RS-423-A, Electronic Industries Association, December, 1978.

Z8030/Z8530 Serial Communications Controller (SCC) Technical Manual, Zilog, Inc., January 1983.

Z8030/AmZ8530 Serial Communications Controller (SCC) Technical Manual, Advanced Micro Devices,
Inc., 1982.

• **Suggested Reference Material for Keyboard/Mouse Interface**

Reference material suggested for a complete definition of the Keyboard/Mouse Interface:

Z8030/Z8530 Serial Communications Controller (SCC) Technical Manual, Zilog, Inc., January 1983.

AmZ8030/AmZ8530 Serial Communications Controller (SCC) Technical Manual,Advanced Micro Devices, Inc., 1982.

• **Suggested Reading for FORTH**

Inside F83
By C. H. Ting
Offete Enterprises, Inc. 13065 South B Street, San Mateo, CA

Starting FORTH
By Loe Brodie/FORTH INC.
Prentence-Hall, Inc. Englewood Cliffs, New Jersey
ISBN 0-13-843079-9