INTRODUCTION TO THE SYS68K/DRAM-EXXX

USER'S MANUAL
First Edition
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FORCE COMPUTERS Inc./GmbH

N O T E

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Figure 1: Photo of the SYS68K/DRAM-E3M1

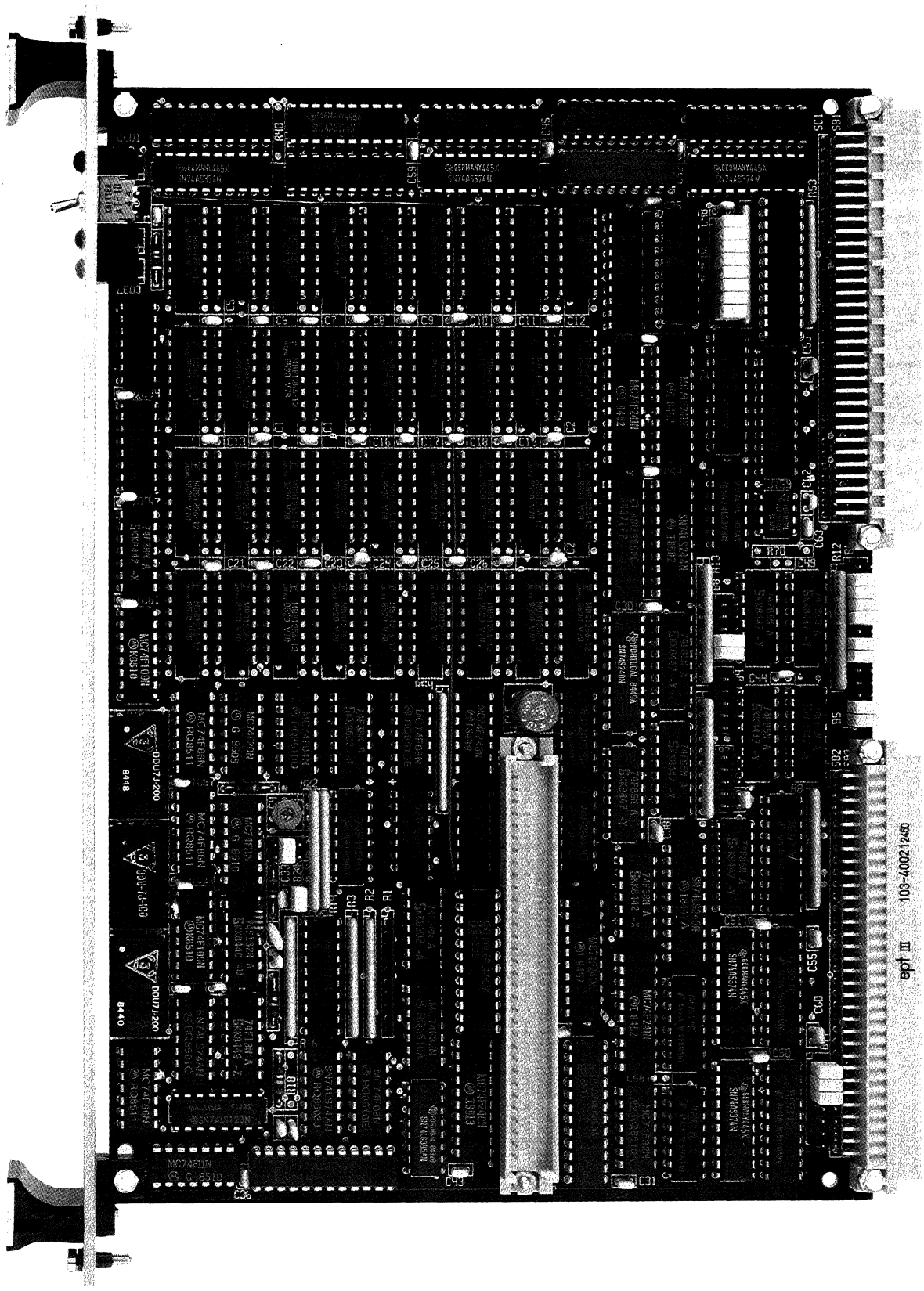


Figure 2: Photo of the SYS68K/DRAM-E3S3

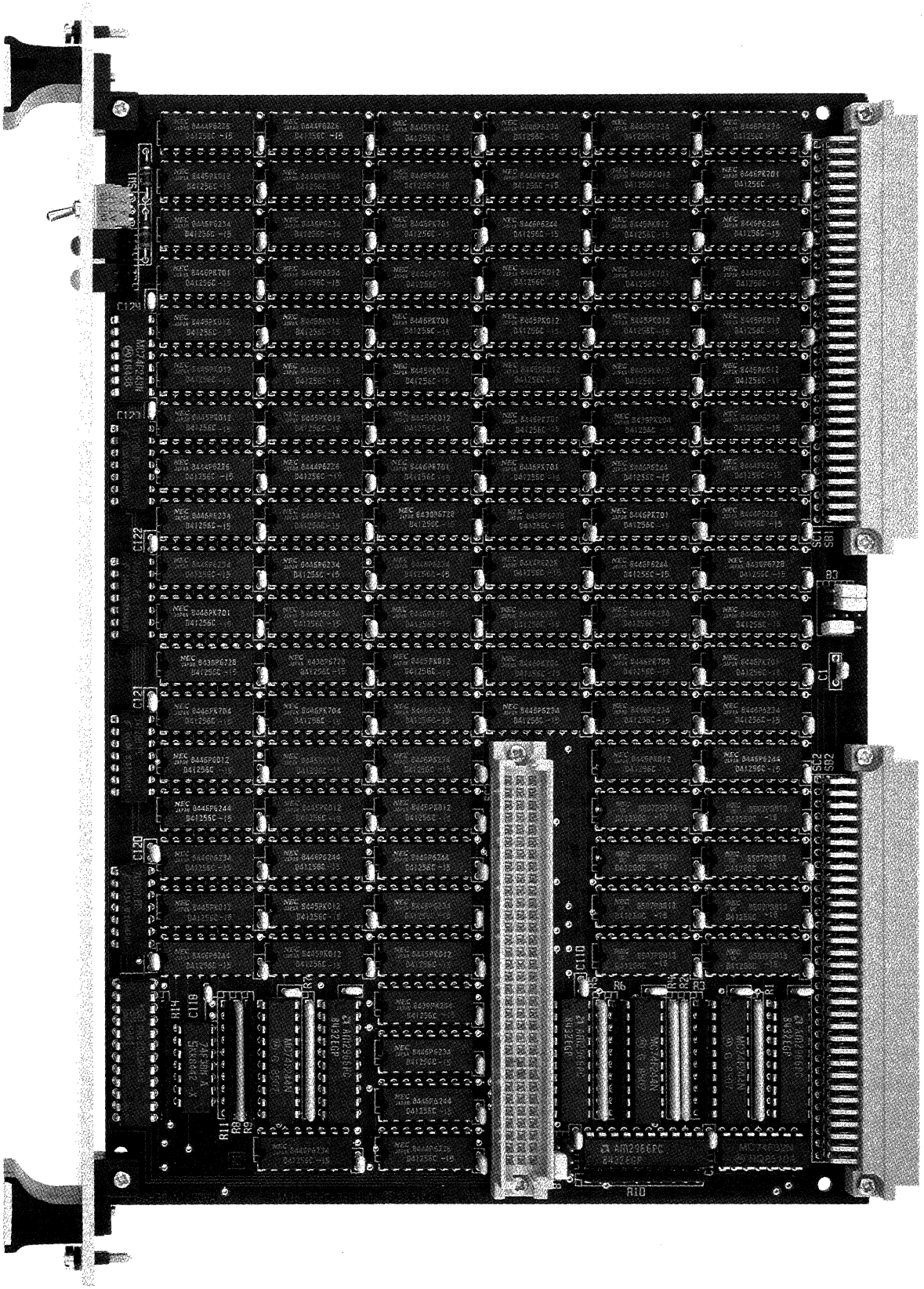


Figure 3: Photo of the SYS68K/DRAM-E4M4

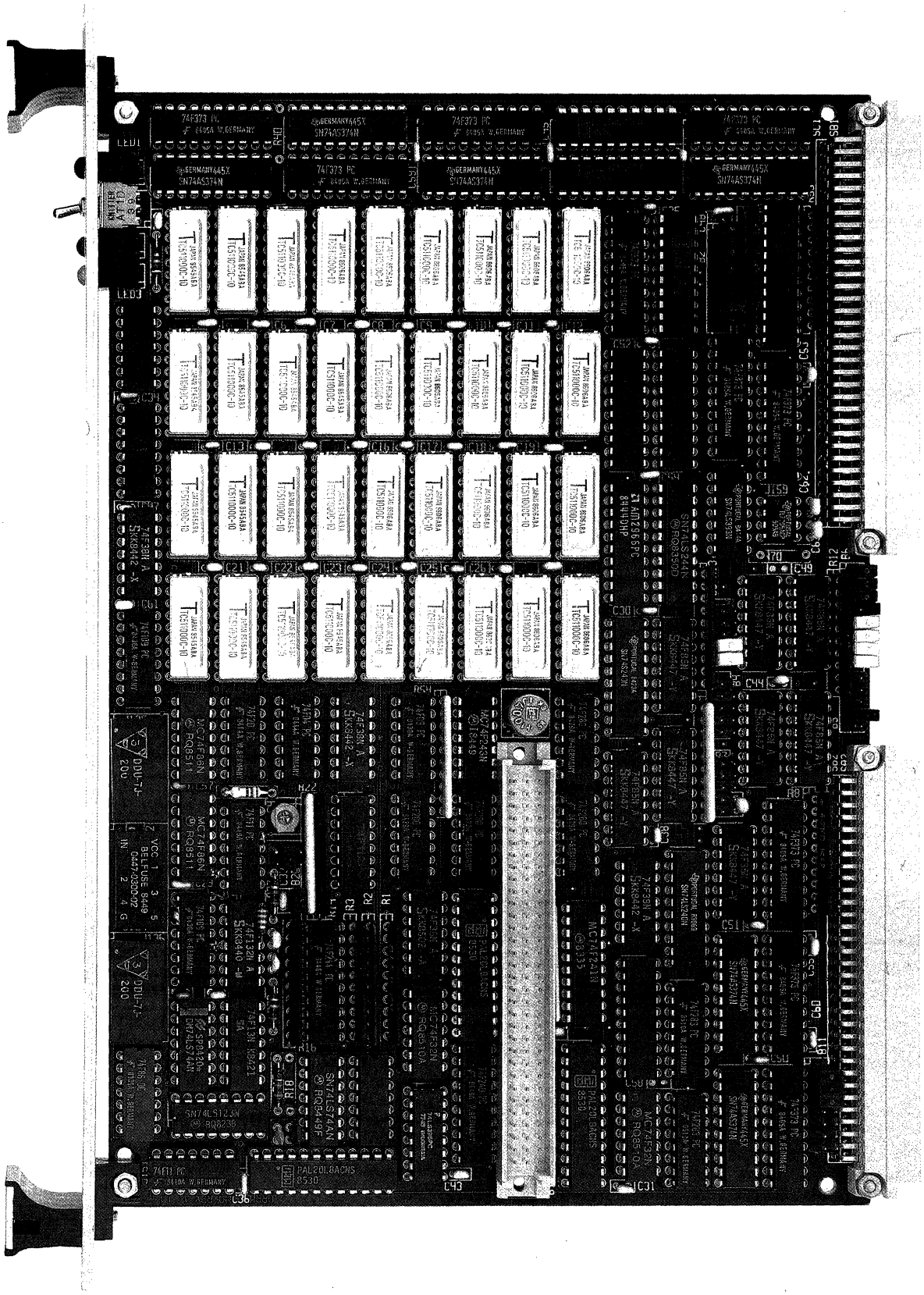
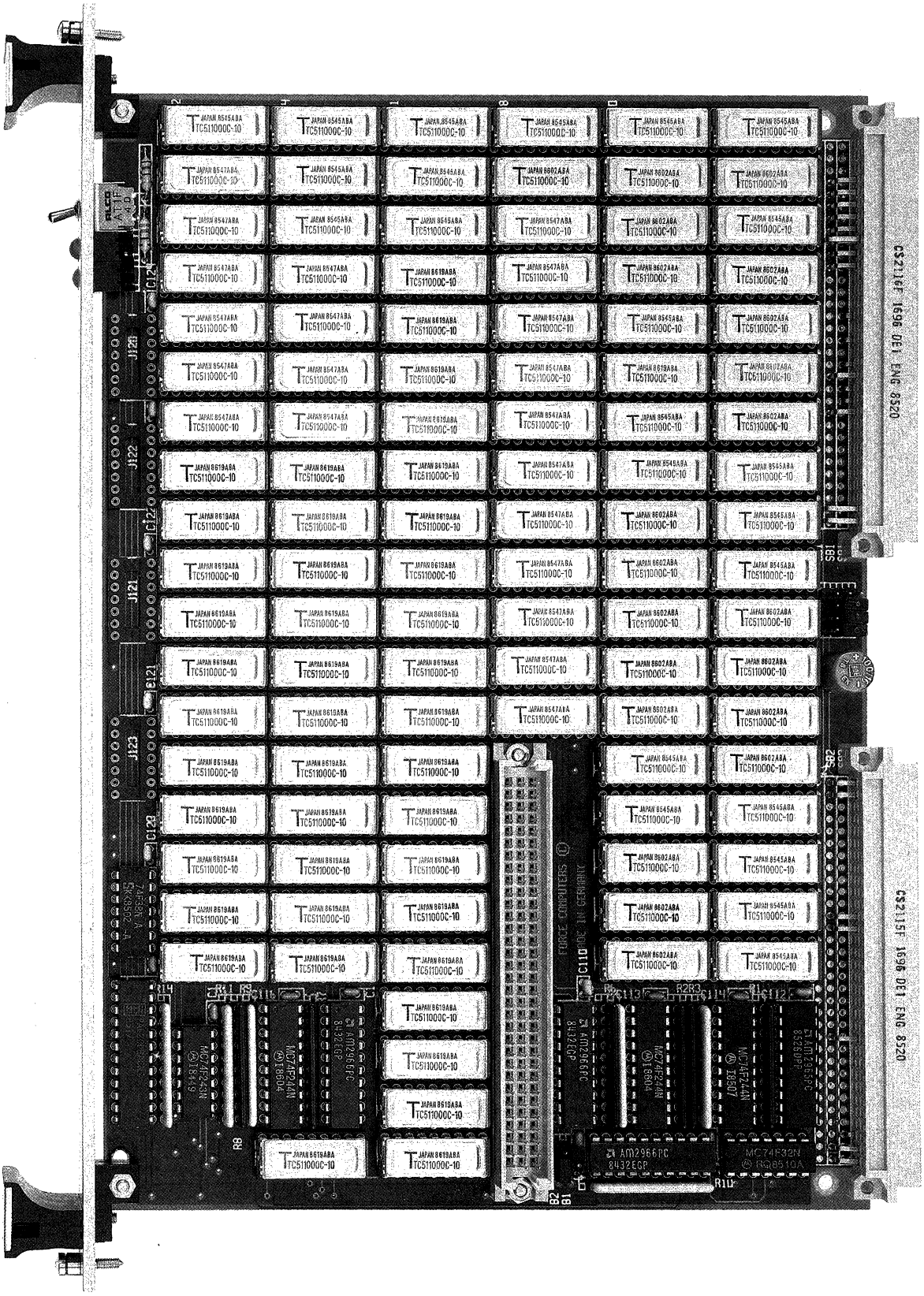


Figure 4: Photo of the SYS68K/DRAM-E4S12



1.Ø General Description

The SYS68K/DRAM-E3 and E4 family of memory boards are high-speed, low cost memory extensions to the VMEbus.

The memory capacity ranges from 1 to 28Mbyte, using 1 to 3 boards.

A dynamic memory boards contain byte parity check circuits to detect single but errors. The access time of the RAM boards is as low as 7Øns for write, and 245ns for read cycles, including parity generation and check.

The photo of the DRAM-E4M4, a 4byte single board solution, is shown in Figure 1-1.

Easy memory expansion of the main board is provided by adding FME slave boards, which are fully controlled from the FME master board, and which contain only the necessary driver/receiver circuits as well as the dynamic memory chips.

The FME concept is shown in Figure 1-3, while Figure 1-2 outlines the block diagram of the DRAM-E4M4 board.

Figure 6: Block Diagram of the SYS68K/DRAM-EXMX

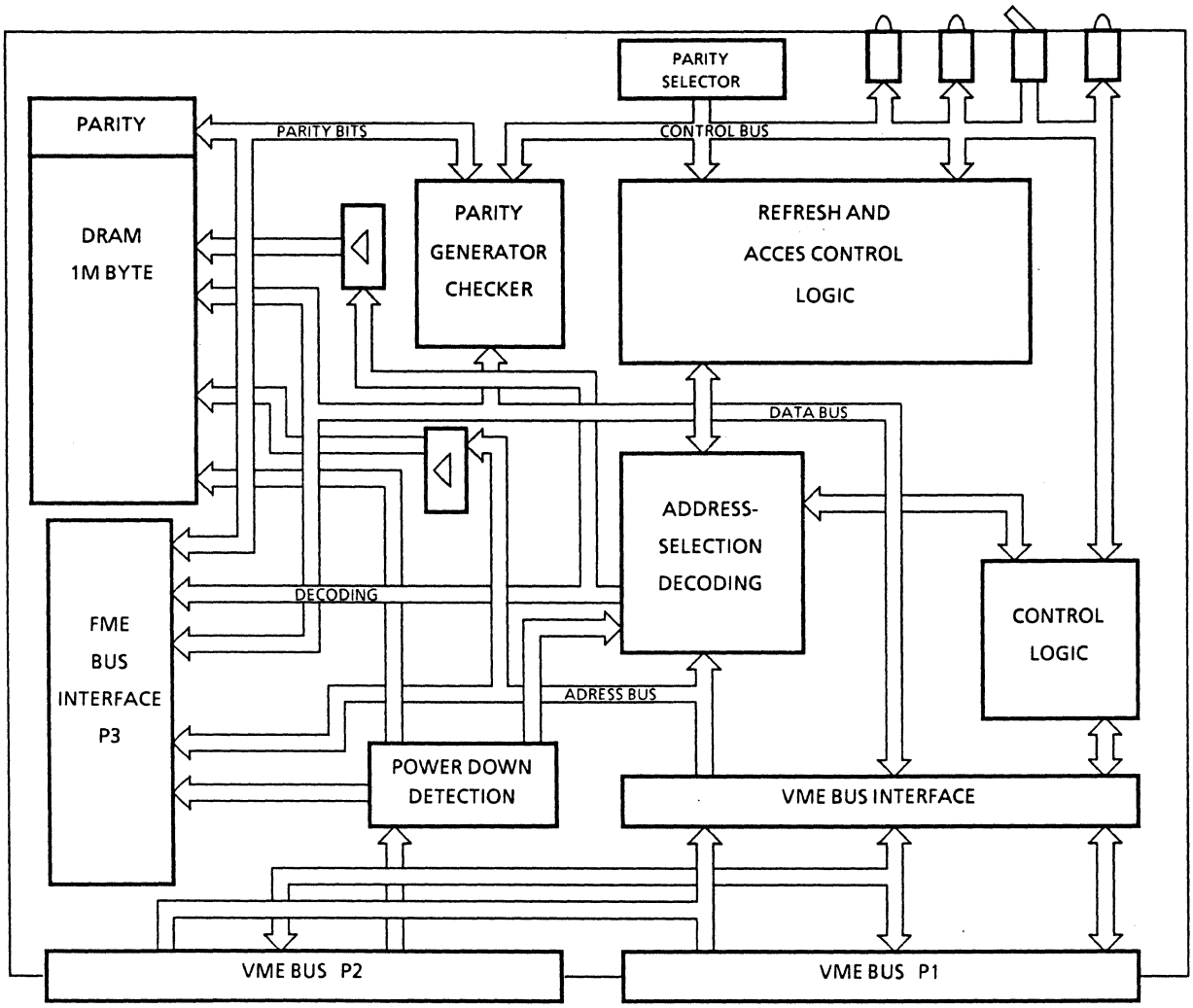
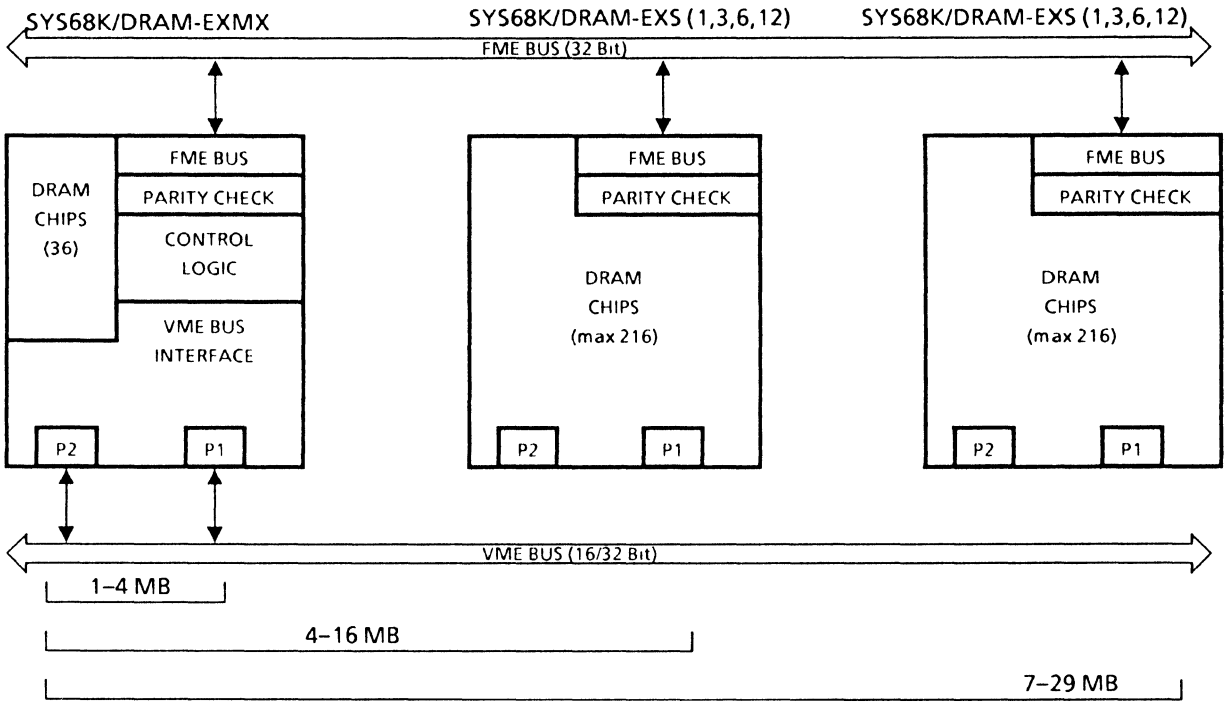


Figure 7: The FME Concept



2.0 The RAM Board Concept

Each of the following memory boards contains a dynamic RAM consisting of a minimum of 1Mbyte, which can be expanded via the FME slave boards, as listed in Table 2-1.

Table 2-1: Existing FME Memory Boards

Type	Capacity	Connectable with:
DRAM-E3M1	1Mbyte	E3S1, E3S3 (1), E3S6 (1)
DRAM-E3S1	1Mbyte	E3M1
DRAM-E3S3	3Mbyte	E3M1, E3S3 (1)
DRAM-E3S6	6Mbyte	E3M1
DRAM-E4M4	4Mbyte	E4S4, E4S12 (2)
DRAM-E4S4	4Mbyte	E4M4
DRAM-E4S12	12Mbyte	E4M4, E4S12 (1)

Caution: DRAM-E3 and DRAM-E4 products cannot be combined or connected together.

INSTALLATION AND WARNINGS

Please read the complete installation procedure before the board is installed in a VMEbus environment to avoid malfunctions and component damages.

1.Ø General Overview

Easy installation of the DRAM-E3/4 boards is provided because all jumper settings are made to access the boards under standard conditions. The boards are configured to be directly accessed via the standard and the extended address range from address $1ØØ.ØØØ onwards.

The decoding set up for each of the different boards is outlined in the Hardware User's Manual of the DRAM-ExMx boards.

1.1 The Function Switch Positions

The board contains 1 function switch (R/L) for isolating the board from the VMEbus.

The two positions of the switch are defined as "up" and "down" for first installation.

Please toggle the switch sometime before installing the board in the rack to detect damages of the switch during transportation.

1.2 The Default Hardware Setup

The VMEbus interface of the DRAM-E3M1 and DRAM-E4M4 is configured for immediate use with 16 and 32-bit CPU boards. The following table lists the default setup in detail:

Table 1-1: Default Setups

Board	Start Address	End Address	AMCode
DRAM-E3M1	XX1ØØ.ØØØ	XX1FF.FFF	Ø9,ØA,ØD,ØE
DRAM-E3M1	XX1ØØ.ØØØ	XX1FF.FFF	39,3A,3D,3E
DRAM-E4M4	XX1ØØ.ØØØ	XX4FF.FFF	Ø9,ØA,ØD,ØE
DRAM-E4M4	XX1ØØ.ØØØ	XX4FF.FFF	39,3A,3D,3E

If the full 32 address decoding should be enabled (A32 decoding), the jumper B18 has to be installed.

By default, the jumper is removed and only the address lines up to A23 are decoded.

2.Ø Installation in the Rack

The main and the slave board are screwed together and can immediately be mounted into a VME rack at slot 2 or higher.

Caution:

1) Switch off power before installing the board to avoid electrical damages of the components.

2) The boards contain a special ejector (the handles).

   The boards have to be plugged in and the screws of the front panel must be turned on to guarantee proper installation.

3) Unplug every other VMEbus or VMXbus memory board to avoid conflicts.

2.1 Power On

If the board is correctly installed, the switches are in the correct positions, the power for the VMEbus rack can be switched on, and the board can be initialized.

HARDWARE USER'S MANUAL

DRAM-E3M1 and E4M4

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Figure 1-1: Photo of the SYS68K/DRAM-E3M1

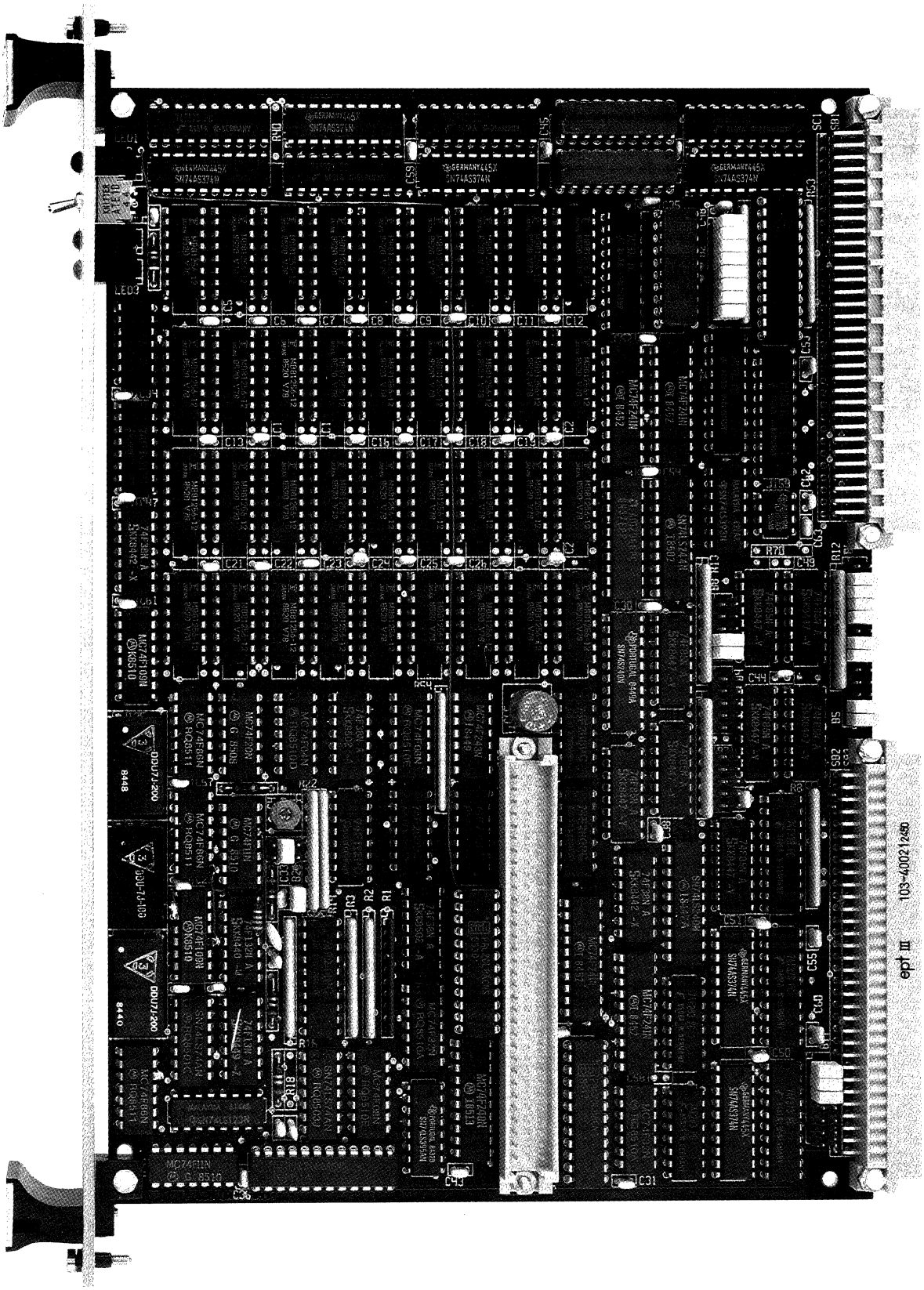
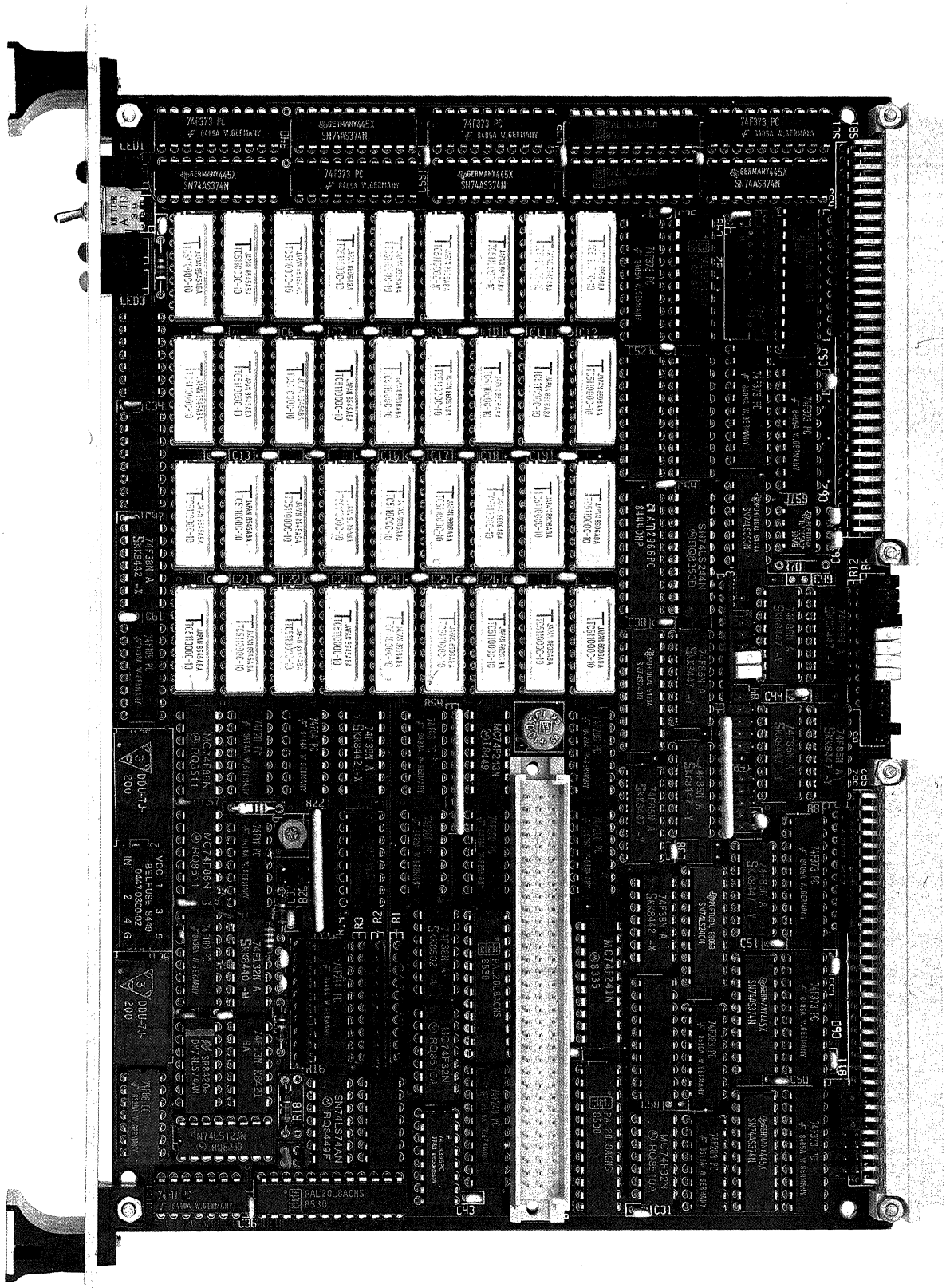


Figure 1-2: Photo of the SYS68K/DRAM-E4M4



1.Ø General Information

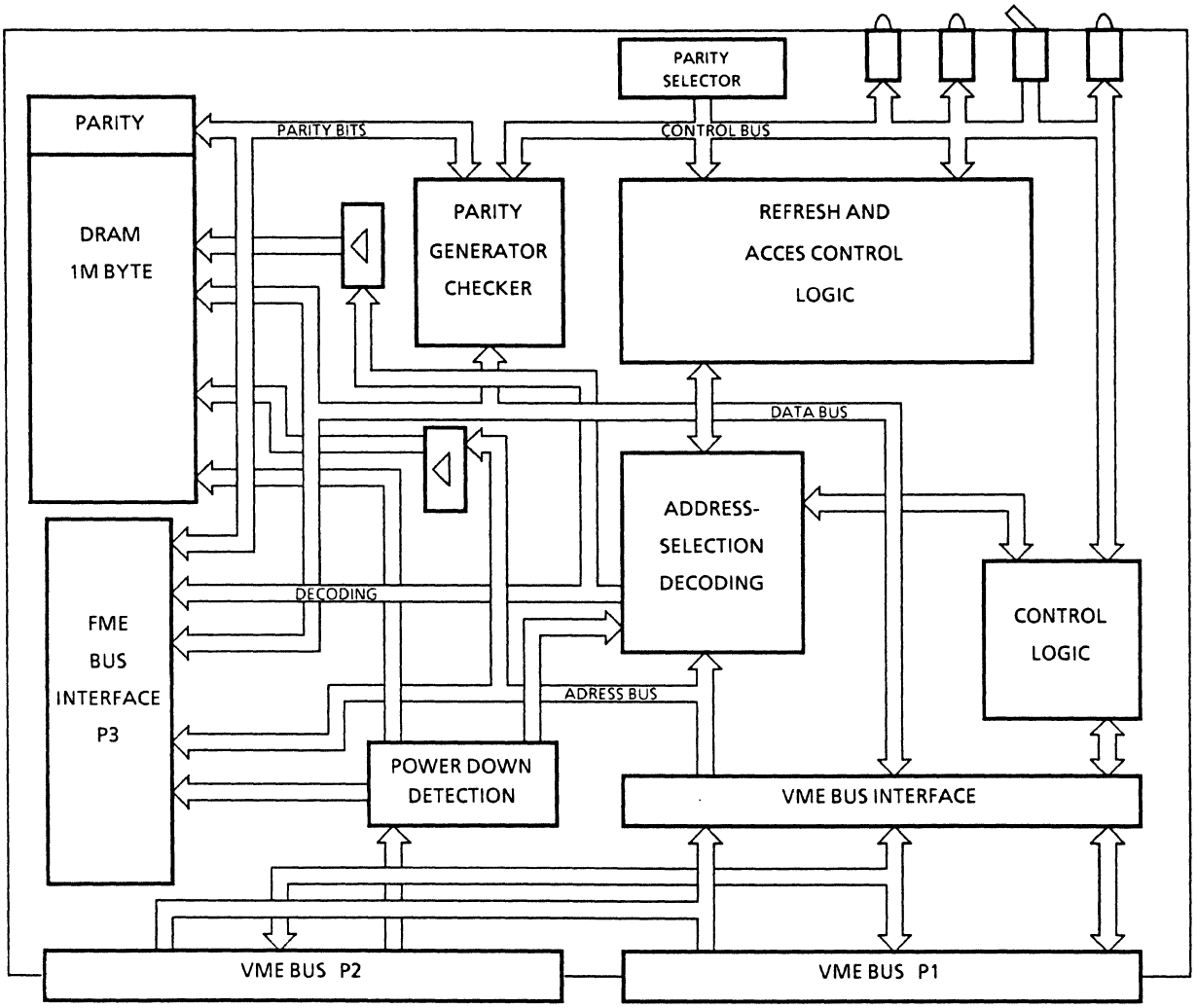
The SYS68K/DRAM-EXMX high speed dynamic memory boards are designed for VMEbus/P1Ø14* environments, and offer 4Mbyte of RAM capacity.

The boards are able to transfer 8, 16, 24 or 32 bits of data in the whole address range of 16M byte or 4G Byte because all 32 address lines of the VME/P1Ø14* bus are supported. Additionally, an FMEbus master interface for memory expansion is included. Battery backup is provided through a connection on P2.

Three LEDs for status display and a RUN/LOCAL switch allow easy handling of the boards.

IEEE P1Ø14* Bus specification (VMEbus) of the IEEE Computer Society TC.

Figure 2-1: Block Diagram SYS68K/DRAM-EXMX



2.Ø General Operation

The SYS68K/DRAM-E4M4 (see Figure 1-1) contains the VMEbus interface, timing and control logic, refresh circuitry and the RAM storage array (1M or 4Mbyte). The board also contains circuitry to generate and check parity and to generate a bus error if a Parity Error is detected.

Easy access address selection in 256K byte increments is provided through jumper fields. The FMEbus master interface allows easy memory expansion through SYS68K/DRAM-EXSX boards.

If a Parity Error is detected, a BERR* is driven to the VMEbus as long as the parity check is enabled.

A RUN/LOCAL switch can separate the board from the VMEbus without loss of data. This mode is displayed by an LED. An access LED is required on the front panel to inform the user that an access to a DRAM area is pending.

A general block diagram of the SYS68K/DRAM-E4M4 is shown in Figure 2-1.

3.Ø Hardware Description

The address selection, VMEbus response timing diagram, functional description and the jumper settings are described in the following sections.

3.1 Supported Transfer Types

The SYS68K/DRAM-EXMX is capable of transferring 8, 16, 24 or 32 bits of data. The VMEbus/PlØ14* spec defines the transfer type as well as the number of bytes to be transferred.

Table 3-1 lists all transfer types supported by the DRAM-EXMX and the DRAM-EXSX boards connected to the DRAM-EXMX.

The VME/PlØ14 specification defines the relationship between the control signals and the transfer type. Please refer to the specification for further details.

Table 3-1: Supported Data Transfer Types

Data Transfer Type		D24-D31	D16-D23	D8-D15	DØ-D7	Note
Address Only						
Single Byte (8 bit)	EVEN			x		
	ODD				x	
Double Byte (16 bit)				x	x	
Quad Byte (32 bit)		x	x	x	x	
Single Byte Read Modify Write (8 bit RMW)	EVEN			x		
	ODD				x	
Double Byte Read Modify Write (16 bit RMW)				x	x	
Quad Byte Read Modify Write (32 bit RMW)		x	x	x	x	
Unaligned Transfers			x	x		
		x	x	x		
			x	x	x	
Unaligned RMW Transfers			x	x		
		x	x	x		
			x	x	x	

3.2 Access to the DRAM-EXMX Board

Easy access address and address modifier code selection to the DRAM-EXMX board is provided through jumperfields. The access address is jumper selectable in 256K byte steps to allow contiguous memory configuration to other VME/P1Ø14 bus based boards.

3.2.1 The Access Address Selection of the DRAM-EXMX Board

This chapter describes the address selection of the DRAM-EXMX board excluding slave boards (DRAM-EXSX) because the access address selection of the board including the slave boards is described in Chapter 4.1. The memory capacity of the DRAM-EXMX board is 1M byte.

The comparator ICs J118 to J125 decode the address range out of the whole range of 16M byte (A24 mode) or 4G byte (A32 mode).

The least significant address signal which can be modified is A18.

A24 decoding:

23	22	21	2Ø	19	18	17	16
y	y	y	y	y	y	x	x

y = set to logical Ø or 1
x = don't care

To allow a flexible lay-out, the DRAM-EXMX board allows the access address selection in 256K byte boundaries by jumper settings in jumper areas (3 jumperfields each).

One jumper area defines the start address at which the board can be accessed.

The other jumper area defines the first address at which the board cannot be accessed. The address range at which the board responds to is set by default from $FF1ØØØØØ to $FF1FFFFF or from $FF1ØØØØØ to $FF4FFFFF.

In a standard environment (68ØØØ or 68Ø1Ø processor) the address lines A24 to A31 are not driven (A24 mode). The decoding logic of the DRAM-EXMX board provides the A32 mode and offers a full 32 bit decoding. For this purpose the address lines A24 to A31 are decoded every time. In an A24 environment, the upper address lines A24 to A31 have to be ignored from the decoding logic. This is provided through internal pull-up resistor networks which pull the upper address lines to high state. This results in the need to jumper the start address to $FF1Ø ØØØØ for parallel decoding in the A24 and A32 mode.

Figure 3-1 outlines the decoding logic in a general block diagram and Table 3-2 lists the relation between the jumperfields and the address range to be selected.

Jumperfields B4, B5 and B6 define the start address because B7, B8 and B9 define the first address which is not on the DRAM-EXMX.

Figure 3-2 outlines the location diagram of the access address selection jumperfields.

Tables 3-3 and 3-4 list the default connection of the DRAM-EXMX board during manufacturing (delivery version).

Table 3-5 lists the default connection of the DRAM-E4M4 board during manufacturing (delivery version).

Figure 3-1: The Decoding Logic Block Diagram

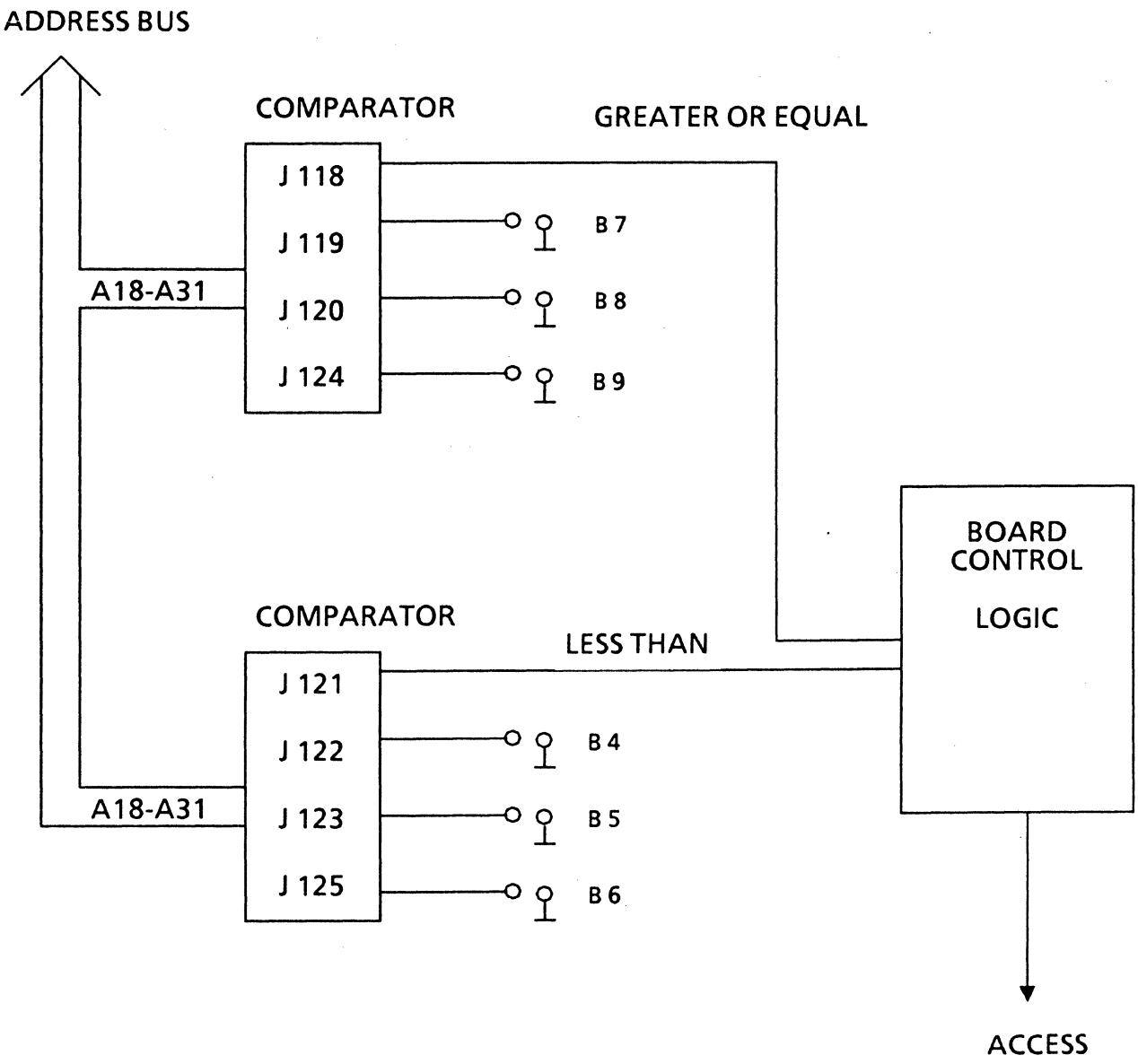


Figure 3-2: Location Diagram of the Access Address Selection Jumper

Please see Register 4 for the complete location diagram.

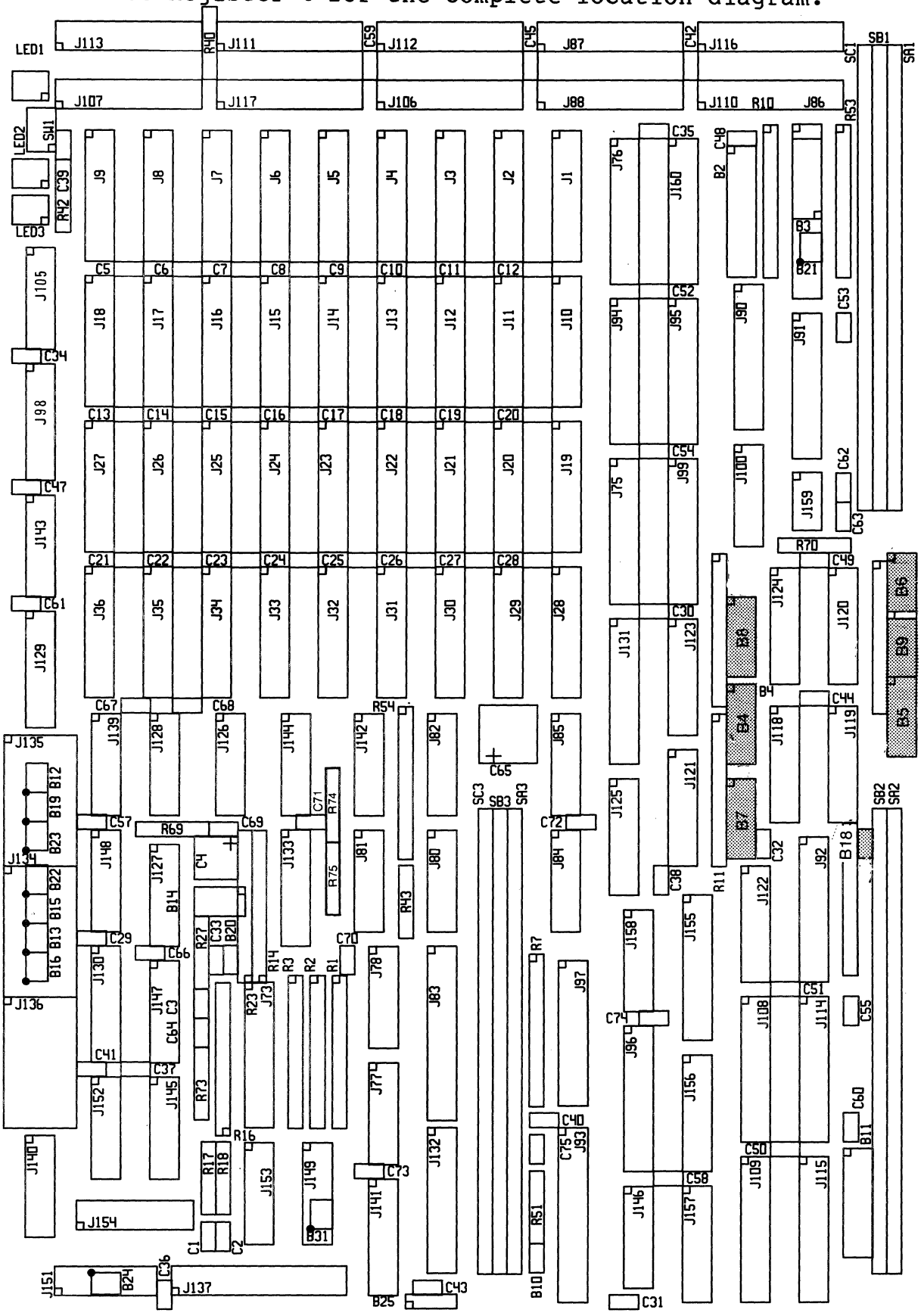


Table 3-2: Jumperfield Assignment to Access Address Selection

START Address Selection				Selection of 1st not on-board Addr		
Jumperfield			Corresponding Bus Address Signal	Jumperfield		
B7	B8	B9		B4	B5	B6
1-10			A31	1-10		
2-9			A30	2-9		
3-8			A29	3-8		
4-7			A28	4-7		
5-6			A27	5-6		
	1-10		A26		1-10	
	2-9		A25		2-9	
	3-8		A24		3-8	
	4-7		A23		4-7	
	5-6		A22		5-6	
		1-8	A21			1-8
		2-7	A20			2-7
		3-6	A19			3-6
		4-5	A18			4-5

Table 3-3: Default Access Address Selection for the DRAM-E3M1

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
	5-6			5-6		A22
		1-8				A21
					2-7	A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FF1F FFFF	$1F FFFF
First not on-board Address:	$FF20 0000	$20 0000
Boundary:	$0010 0000	$10 0000
	1M byte	1M byte

Table 3-4: Default Access Address Selection for DRAM-E4M4

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
	5-6					A22
		1-8			1-8	A21
						A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FF4F FFFF	$4F FFFF
First not on-board Address:	$FF50 0000	$50 0000
Boundary:	$0040 0000	$40 0000
	4M byte	4M byte

3.2.2 Modification of the Access Address of the DRAM-EXMX

Due to the full decoding of the 21 address signals, the DRAM-EXMX can be jumpered to react on different access address ranges. Tables 3-5, 3-6 and 3-7 outline 3 examples of the DRAM-EXMX configuration for different memory ranges.

To adapt the board access address range to the appropriate range, please follow the following rules:

1) Calculate the start address of the board and list the address line value A31 to A18 in binary form (Ø or 1)

2) Calculate the first not on-board address by adding the boundary and list the address line value A31 to A18 in binary form (Ø or 1)

3) Install or remove the jumpers in the jumperfields B4 to B9 in the following way:

a Ø on the corresponding address signal is equivalent to an inserted jumper,

a 1 on the corresponding address signal is equivalent to a removed jumper.

Table 3-1Ø gives an empty form for installation of the used setup.

Note: 1) If the A32 and the A24 mode is used, the address signals A24 to A31 must be high for a valid A24 decoding. If not, the A24 decoding is disabled.

2) If only the A32 mode is used, there are no limitations regarding address selection.

3a) If only the A24 mode is used, A24 to A31 must be high (provided through on-board pull-up register networks) if not disabled (see 3b).

3b) If only the A24 mode is used, A24 to A31 can be disabled by removing the jumper at jumperfield B18.

Caution: In the default configuration B18 is not inserted (A24 mode is enabled!)

Table 3-5: Access Address Selection Example 1 for DRAM-E3M1

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
	5-6			5-6		A22
		1-8			1-8	A21
		2-7				A20
						A19
		4-5			4-5	A18

	A32	A24
Start Address:	$FF08 0000	$08 0000
End Address:	$FF17 FFFF	$17 FFFF
First not on-board Address:	$FF18 0000	$18 0000
Boundary:	$0010 0000	$10 0000
	1M byte	1M byte

Table 3-6: Access Address Selection Example 2 for DRAM-E3M1

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
						A22
						A21
		2-7				A20
		3-6			3-6	A19
						A18

	A32	A24
Start Address:	$FF64 0000	$64 0000
End Address:	$FF73 FFFF	$73 FFFF
First not on-board Address:	$FF74 0000	$74 0000
Boundary:	$0010 0000	$10 0000
	1M byte	1M byte

Table 3-7: Access Address Selection Example 3 for DRAM-E3M1

Jumper B18 must be inserted (Mode A32)

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
1-10			1-10			A31
2-9			2-9			A30
						A29
						A28
5-6			5-6			A27
						A26
						A25
	3-8			3-8		A24
	4-7			4-7		A23
						A22
		1-8			1-8	A21
		2-7				A20
		3-6			3-6	A19
						A18

	A32	A24
Start Address:	$3644 0000	
End Address:	$3653 FFFF	NOT
First not on-board Address:	$3654 0000	DECODED
Boundary:	$0010 0000	
	1M byte	1M byte

Table 3-8: Access Address Selection Example 1 for DRAM-E4M4

Jumper B18 must be removed (Mode A24)

Start Address			First not on-board Address			Corresponding Bus Address Signal	
B7	B8	B9	B4	B5	B6		HEX
						A31	8
						A30	4
						A29	2
						A28	1
						A27	8
						A26	4
						A25	2
						A24	1
	4-7			4-7		A23	8
	5-6					A22	4
		1-8			1-8	A21	2
						A20	1
		3-6			3-6	A19	8
		4-5			4-5	A18	4

Default	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FF4F FFFF	$4F FFFF
First not on-board Address:	$FF50 0000	$50 0000
Boundary:	$ 40 0000	$40 0000
	4M byte	4M byte

Table 3-9: Access Address Selection Example 2 for DRAM-E4M4

Jumper B18 must be removed (Mode A32)

Start Address			First not on-board Address			Corresponding Bus Address Signal	
B7	B8	B9	B4	B5	B6		HEX
1-10			1-10			A31	8
2-9			2-9			A30	4
3-8			3-8			A29	2
4-7			4-7			A28	1
5-6			5-6			A27	8
	1-10			1-10		A26	4
	2-9			2-9		A25	2
	3-8			3-8		A24	1
	4-7			4-7		A23	8
	5-6					A22	4
		1-8			1-8	A21	2
						A20	1
		3-6			3-6	A19	8
		4-5			4-5	A18	4

Default	A32	A24
Start Address:	$0010 0000	
End Address:	$004F FFFF	
First not on-board Address:	$0050 0000	
Boundary:	$ 40 0000	
	4M byte	

Table 3-10: Access Address Selection for DRAM-E3M1

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
						A22
		1-8			1-8	A21
		2-7				A20
						A19
		4-5			4-5	A18

	A32	A24
Start Address:	$	$ 480000
End Address:	$	$
First not on-board Address:	$	$ 580000
Boundary:	$	$ 100000
	1M byte	1M byte

Table 3-11: Access Address Selection for DRAM-E4M4

Start Address			First not on-board Address			Corresponding Bus Address Signal	
B7	B8	B9	B4	B5	B6		HEX
						A31	8
						A30	4
						A29	2
						A28	1
						A27	8
						A26	4
						A25	2
						A24	1
	4-7			4-7		A23	8
	5-6					A22	4
		1-8			1-8	A21	2
		2-7			2-7	A20	1
						A19	8
		4-5			4-5	A18	4

	A32	A24
Start Address:	$	$ 080000
End Address:	$	$
First not on-board Address:	$	$ 480000
Boundary:	$	$ 400000
	4M byte	4M byte

3.3 The Address Modifier Decoding

The VME/P1Ø14 specification defines address modifier (AM-) codes which are decoded in parallel to the address signals. The 6 AM Code signals are routed directly into a PAL and a total number of 1Ø different codes can be separately enabled via jumper settings. Table 3-12 lists the AM-Codes which are defined in the VME/P1Ø14 specification.

A short I/O access to the DRAM-EXMX is not necessary because the memory range of the board is greater than the range for this AM-Code.

Additionally, the block transfer is not supported through the DRAM-EXMX board. Therefore, the AM codes, listed in Table 3-13 are allowed. To enable each of the AM-Codes separately, the jumperfields B2, B3 and B21 are installed on the board. Figure 3-3 outlines the location diagram of the AM-Code jumperfields.

Figure 3-3: The AM-Code Jumperfields

Please see Register 4 for the complete location diagram.

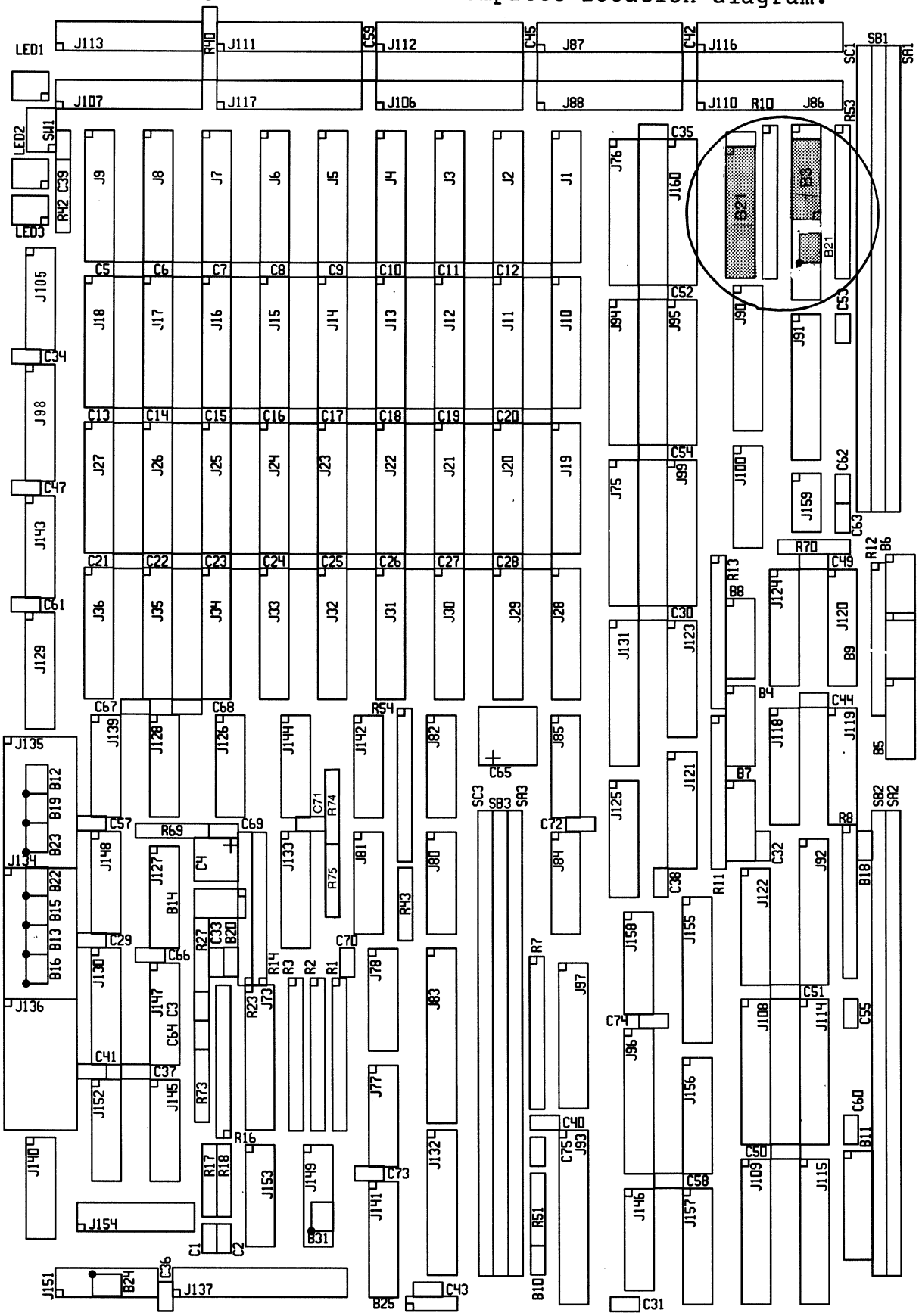


Table 3-12: The Address Modifier Codes

HEX CODE	Address Modifier 5	4	3	2	1	Ø	Function
3F	H	H	H	H	H	H	Standard Supervisory Block Transfer
3E	H	H	H	H	H	L	Standard Supervisory Program Access
3D	H	H	H	H	L	H	Standard Supervisory Data Access
3C	H	H	H	H	L	L	Reserved
3B	H	H	H	L	H	H	Standard Non-Privileged Block Transfer
3A	H	H	H	L	H	L	Standard Non-Privileged Program Access
39	H	H	H	L	L	H	Standard Non-Privileged Data Access
38	H	H	H	L	L	L	Reserved
37	H	H	L	H	H	H	Reserved
36	H	H	L	H	H	L	Reserved
35	H	H	L	H	L	H	Reserved
34	H	H	L	H	L	L	Reserved
33	H	H	L	L	H	H	Reserved
32	H	H	L	L	H	L	Reserved
31	H	H	L	L	L	H	Reserved
3Ø	H	H	L	L	L	L	Reserved
2F	H	L	H	H	H	H	Reserved
2E	H	L	H	H	H	L	Reserved
2D	H	L	H	H	L	H	Short Supervisory Access
2C	H	L	H	H	L	L	Reserved
2B	H	L	H	L	H	H	Reserved
2A	H	L	H	L	H	L	Reserved
29	H	L	H	L	L	H	Short Non-Privileged Access
28	H	L	H	L	L	L	Reserved
27	H	L	L	H	H	H	Reserved
26	H	L	L	H	H	L	Reserved
25	H	L	L	H	L	H	Reserved
24	H	L	L	H	L	L	Reserved
23	H	L	L	L	H	H	Reserved
22	H	L	L	L	H	L	Reserved
21	H	L	L	L	L	H	Reserved
2Ø	H	L	L	L	L	L	Reserved

L = low signal level
H = high signal level

Table 3-12 cont'd

HEX CODE	Address Modifier 5	4	3	2	1	Ø	Function
1F	L	H	H	H	H	H	User defined
1E	L	H	H	H	H	L	User defined
1D	L	H	H	H	L	H	User defined
1C	L	H	H	H	L	L	User defined
1B	L	H	H	L	H	H	User defined
1A	L	H	H	L	H	L	User defined
19	L	H	H	L	L	H	User defined
18	L	H	H	L	L	L	User defined
17	L	H	L	H	H	H	User defined
16	L	H	L	H	H	L	User defined
15	L	H	L	H	L	H	User defined
14	L	H	L	H	L	L	User defined
13	L	H	L	L	H	H	User defined
12	L	H	L	L	H	L	User defined
11	L	H	L	L	L	H	User defined
1Ø	L	H	L	L	L	L	User defined
ØF	L	L	H	H	H	H	Extended Supervisory Block Transfer
ØE	L	L	H	H	H	L	Extended Supervisory Program Access
ØD	L	L	H	H	L	H	Extended Supervisory Data Access
ØC	L	L	H	H	L	L	Reserved
ØB	L	L	H	L	H	H	Extended Non-Privileged Block Transfer
ØA	L	L	H	L	H	L	Extended Non-Privileged Program Access
Ø9	L	L	H	L	L	H	Extended Non-Privileged Data Access
Ø8	L	L	H	L	L	L	Reserved
Ø7	L	L	L	H	H	H	Reserved
Ø6	L	L	L	H	H	L	Reserved
Ø5	L	L	L	H	L	H	Reserved
Ø4	L	L	L	H	L	L	Reserved
Ø3	L	L	L	L	H	H	Reserved
Ø2	L	L	L	L	H	L	Reserved
Ø1	L	L	L	L	L	H	Reserved
ØØ	L	L	L	L	L	L	Reserved

L = low signal level
H = high signal level

The following table lists the selectable AM-Codes.

Table 3-13: The AM-Code Selection

Jumperfield B2	Jumperfield B3	HEX Code	Function
1-16		3E	Standard Supervisor Program Access
2-15		3D	Standard Supervisor Data Access
3-14		3A	Standard Non-Privileged Program Access
4-13		39	Standard Non-Privileged Data Access
5-12		ØE	Extended Supervisor Program Access
6-11		ØD	Extended Supervisor Data Access
7-1Ø		ØA	Extended Non-Privileged Program Access
8-9		Ø9	Extended Non-Privileged Data Access
	1-1Ø	1Ø	USER defined
	3-8	11	USER defined
	4-7		*
	5-6		*
	2-9		Respond always *

* for test purposes only.

Caution: Jumperfield B21 is for in-circuit test purposes only and has to be disconnected during normal operation.

Each of the AM-Codes may be used in the environment. To enable an AM-Code, the corresponding connection has to be provided.

Table 3-14 lists the default condition during manufacturing. If the default set-up is not usable and a special set-up has to made, please follow the following 2 rules:

1) Define the AM-Codes for the DRAM-EXMX board.

2) Insert or remove the jumpers in jumperfield B2 and/or install or remove a wire on the jumperfield B3 in the following way:

An inserted jumper/wire enables the corresponding AM-Code (as listed in Table 3-13) because a removed jumper/wire will disable the corresponding AM-Code.

Tables 3-15, 3-16 and 3-17 list examples for AM-Code combinations. Table 3-18 is an empty form.

Table 3-14: Default AM-Code Selection

Jumperfield Connections		AM-Code	Enabled AM-Code (x)
B2	B3		
1-16		3E	Y
2-15		3D	Y
3-14		3A	Y
4-13		39	Y
5-12		ØE	Y
6-11		ØD	Y
7-1Ø		ØA	Y
8-9		Ø9	Y
		1Ø	N
		11	N

Table 3-15: AM-Code Selection Example 1

Jumperfield Connections		AM-Code	Enabled AM-Code (x)
B2	B3		
1-16		3E	Y
2-15		3D	Y
		3A	N
		39	N
5-12		ØE	Y
6-11		ØD	Y
		ØA	N
		Ø9	N
		1Ø	N
		11	N

Example 1: The DRAM-EXMX responds to 24 bit and 32 bit addressing (A24 and A32 mode) only under Supervisor mode. All non-privileged accesses are ignored.

Table 3-16: AM-Code Selection Example 2

Jumperfield Connections		AM-Code	Enabled AM-Code (x)
B2	B3		
1-16		3E	Y
2-15		3D	Y
3-14		3A	Y
4-13		39	Y
		ØE	N
		ØD	N
		ØA	N
		Ø9	N
		1Ø	N
		11	N

Example 2: All A32 mode accesses are ignored by the DRAM-EXMX board. Only A24 mode accesses are supported.

Table 3-17: AM-Code Selection Example 3

Jumperfield Connections		AM-Code	Enabled AM-Code (x)
B2	B3		
		3E	N
		3D	N
		3A	N
		39	N
5-12		ØE	Y
6-11		ØD	Y
7-1Ø		ØA	Y
8-9		Ø9	Y
	1-1Ø	1Ø	Y
	3-8	11	Y

Example 3: A32 mode accesses as well as the user defined AM-Codes 1Ø and 11 are supported. All other AM-Codes (i.e. the A24 mode) are ignored.

Table 3-18: AM-Code Selection

Jumperfield Connection		AM-Code	Enabled AM-Code (x)
B2	B3		
		3E	
		3D	
		3A	
		39	
		ØE	
		ØD	
		ØA	
		Ø9	
		1Ø	
		11	

3.4 The Parity Check

The DRAM-EXMX board contains 36 memory chips (256K * 1 or 1M * 1 bit); 32 bits for data storage and 4 bits for byte parity information.

The board supports 8, 16, 24 and 32 bit data transfers. Each of the 4 bytes which may be read or written at the same time, has a separately controlled parity checker/generator.

The parity generator is activated on every write access only for the selected bytes (up to 4) which are transferred.

On read accesses the parity checker for the selected byte(s) is activated by default during manufacturing.

If a parity error is detected and if the parity check is enabled, the DRAM-EXMX board drives the BERR signal instead of the DTACK* signal. On occurrence of a parity error, the red FAIL LED on the front panel lights up.

The byte parity check can easily be disabled by following the rules listed below:

1) Remove jumper at jumperfield B2Ø

2) Remove jumper between pin 2 and pin 5 at jumperfield B14

3) Install a jumper between pin 1 and pin 6 at jumperfield B14.

The default connections during manufacturing for the enabled parity check are listed below:

Table 3-19: Parity Check Jumper Fields

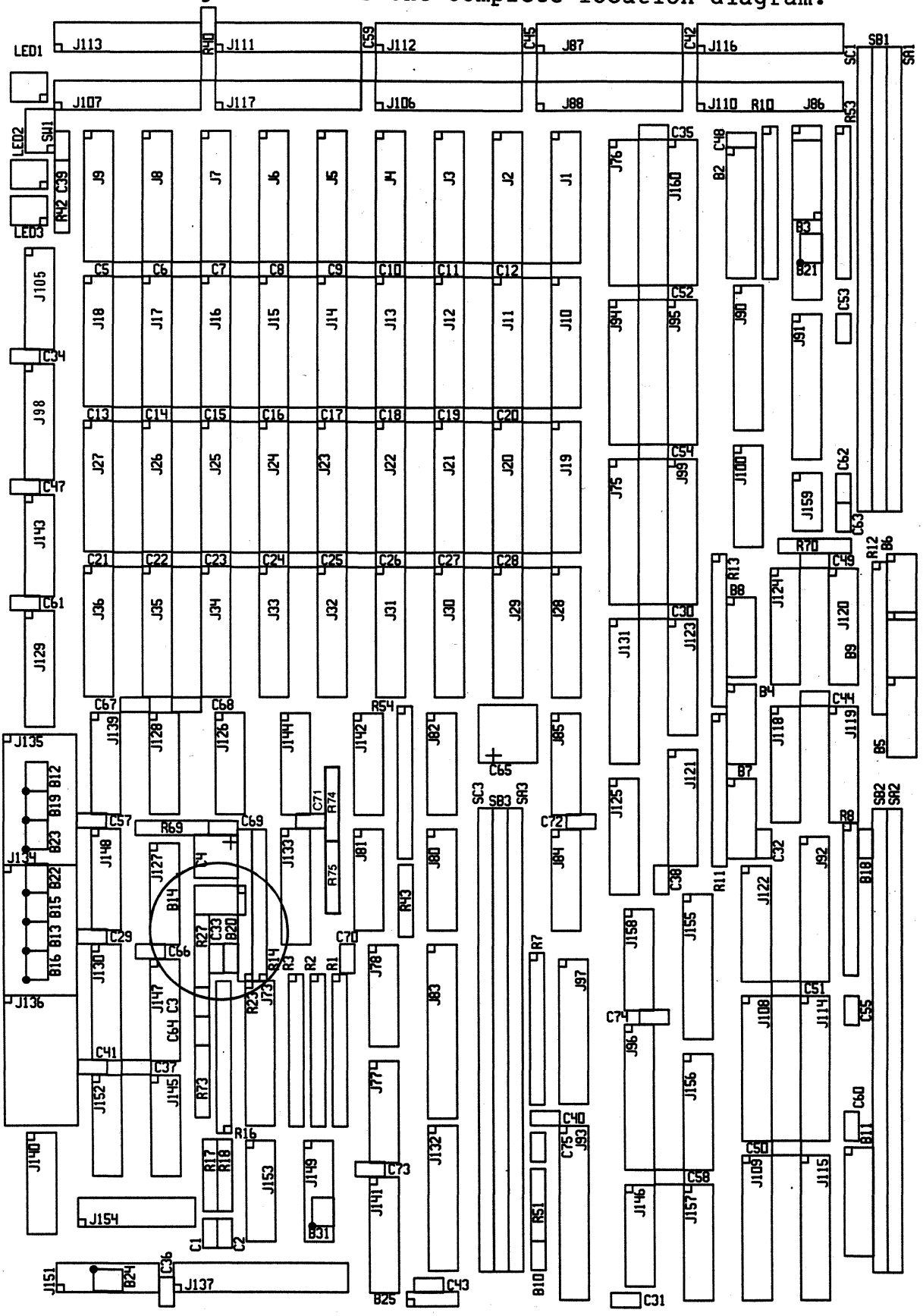
B20	B14	Mode	Note
IN	2 - 5	Parity Error Check enabled	*
OUT	1 - 6	Parity Error Check Disabled	

* Default condition

Figure 3-4 outlines the location diagram of the parity check jumperfields.

Figure 3-4: Parity Check Jumperfield Locations

Please see Register 4 for the complete location diagram.



3.5 The Access Times

The DRAM-EXMX board is a high speed dynamic RAM board which provides the following access times:

Table 3-20: Access Times of the DRAM-EXMX

Access Times	Type	Max
WRITE with Parity Generation	70ns	80ns
READ with Parity Check	245ns	265ns
READ without Parity Check	210ns	225ns

The access time is measured from the falling edge of one of the two data strobes to the falling edge of DTACK* generated from the DRAM-EXMX board.

The cycle time from the beginning of a cycle is 295ns typ / 315ns max.

Due to the interleave structure of the board (decoding and next access are interleaved), a high throughput is provided. If an access was forced, the next access can occur within the following time frames:

Next Access after	TYP	MAX
WRITE	250ns	270ns
READ	70ns	90ns

Therefore, the following transfer capacity is provided on the VME/P1014 bus (if the transfer device has an ideal VME/P1014 timing).

Cycle	TYP	MIN
WRITE	12.0M byte/s	11.0M byte/s
READ	12.0M byte/s	11.0M byte/s

3.6 The Refresh

The refresh for the dynamic RAMs is distributed over 4ms and provision is made to minimize the overhead and delay to the VMEbus accesses.

After the internal read cycle of the DRAMs is finished and the data on a read cycle has been stored in the output data latches, a pending refresh request (every 15us) is executed independent from all VMEbus activities. Therefore, the overhead time for the VMEbus protocol is used to refresh the RAMs. In addition to the refresh interleave, a refresh to the DRAMs is forced if a not on-board access is detected between 11 and 15us after the execution of the last refresh.

A 68Ø1Ø processor with a clock frequency of 1ØMHz can access the DRAM-EXMX board without extra wait states for the DRAM refresh if the used program runs on the DRAM-EXMX or DRAM-EXSX.

The refresh control logic for the FMEbus slave modules (memory expansion) is included on the DRAM-EXMX board.

	TYP	MAX
Overhead time for refresh	12Øns	45Øns

An access can stay for a longer time than the refresh period (15us) because every access cycle on the board is aborted if the correct data is stored on the RAMs or in the output latches to the VMEbus.

Therefore, correct refresh is provided if a system hang-up occurs or if a bus master holds an access for a long time.

If the board is jumpered to work from the standby power, refresh for the dynamic RAMs is provided during main power down.

3.7 The Battery Backup Option

The DRAM-EXMX board can be powered from the +5V main power or from the +5VBAT pins of P2 connector (SA-30/31/32).

The default condition during manufacturing is the connection to the +5V Main Power.

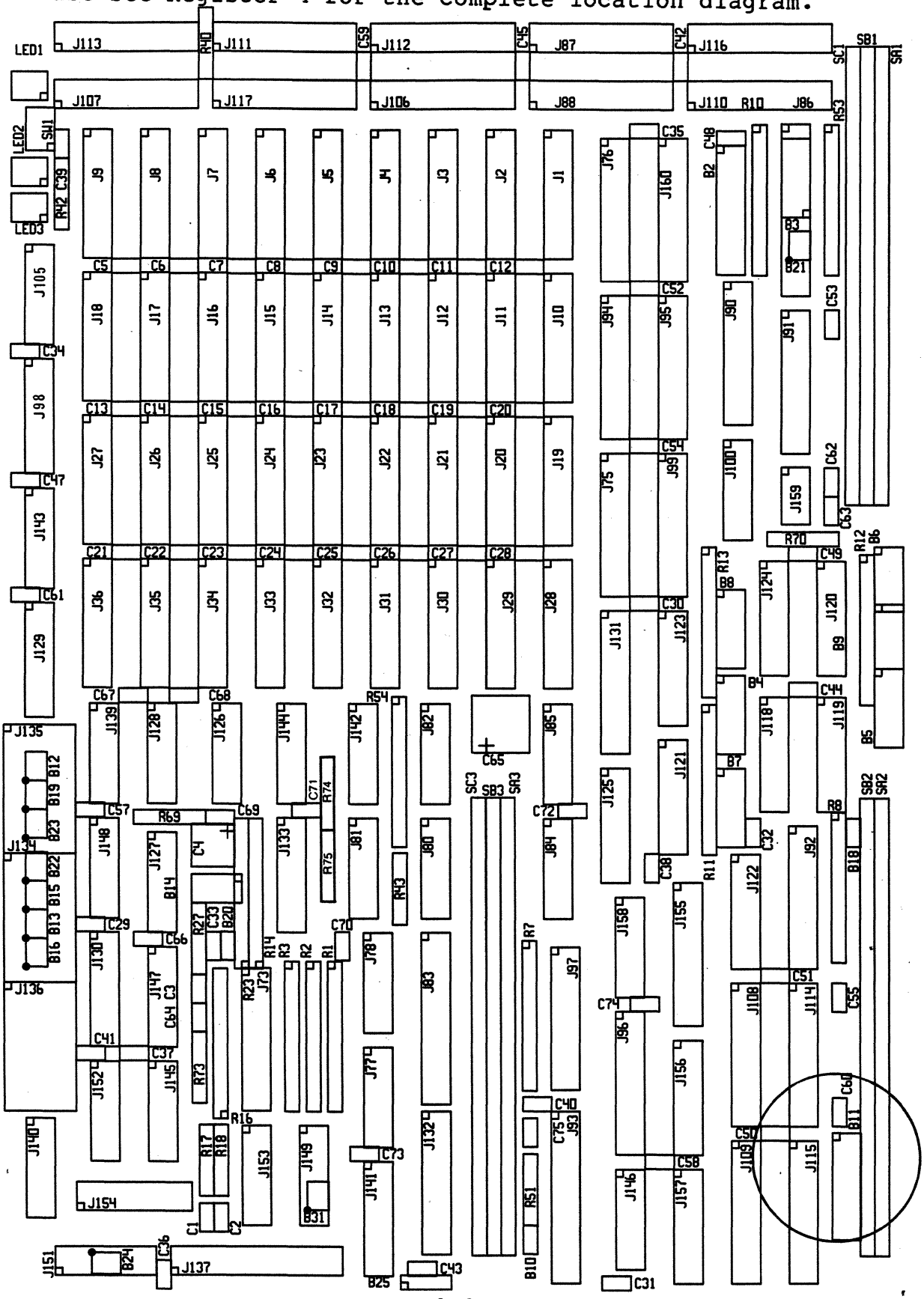
Table 3-21 lists the jumper settings which have to be made for the different modes, and Figure 3-5 outlines the location diagram of the jumperfields.

Table 3-21: The Battery Backup Option

Option	B11
Battery Backup	5-10 6-9 7-8
5V STDBY (optional)	4-11
+5V MAIN	1-14 2-13 3-12

Figure 3-5: Location Diagram of the Battery Backup Jumperfields

Please see Register 4 for the complete location diagram.



3.8 The Front Panel

The DRAM-EXMX board contains a RUN/LOCAL switch which disables the board from the VME/P1Ø14 bus if set to LOCAL. In RUN position, the green "RUN" LED on the front panel turns on, and the red "FAIL" LED lights up if the board is in LOCAL mode.

During normal operation the "FAIL" LED may turn on if a parity error is detected. The parity error is latched and only reset if the board is reset through the SYSRESET* signal from the VMEbus or through a RUN-LOCAL-RUN change of the RUN/LOCAL switch.

Additionally, a yellow SELect LED is installed. The LED turns on if the board is selected (an access is pending).

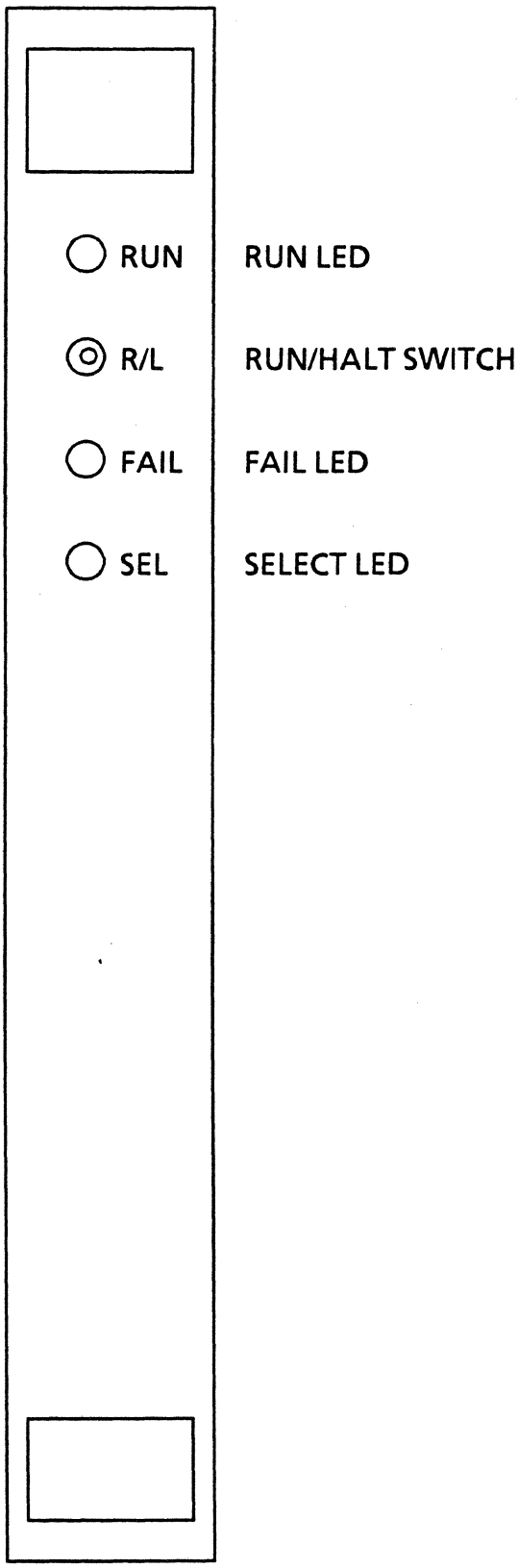
Figure 3-6 shows the front panel lay-out in detail.

RUN	FAIL	Function
-	X	Board in LOCAL mode
X	-	Board in RUN mode
X	X	Board in FAIL mode

Note: All other combinations are not possible.

X = LED active.

Figure 3-6: The Front Panel of the SYS68K/DRAM-EXMX



4.Ø The FMEbus Interface

The DRAM-EXMX board contains an FMEbus interface for memory expansion. All the control logic for access and refresh is included on the DRAM-EXMX board to allow cost effective memory expansions.

The general block diagram of the FME concept is shown in Figure 4-1.

Cost and space intensive ICs are spent only on the master interface (DRAM-EXMX) and only driver circuitries are included on the DRAM-EXSX boards. This allows easy memory expansion through 1 or 2 slave boards.

The following slave boards are now available to interconnect the DRAM boards:

a) DRAM-E3M1:

Board	Capacity
DRAM-E3S1	1Mbyte
DRAM-E3S3	3Mbyte
DRAM-E3S6	6Mbyte

A maximum of 7Mbyte DRAM is provided using a DRAM-E3M1 and two DRAM-E3S3 boards or a DRAM-E3M1 and a DRAM-E3S6 board.

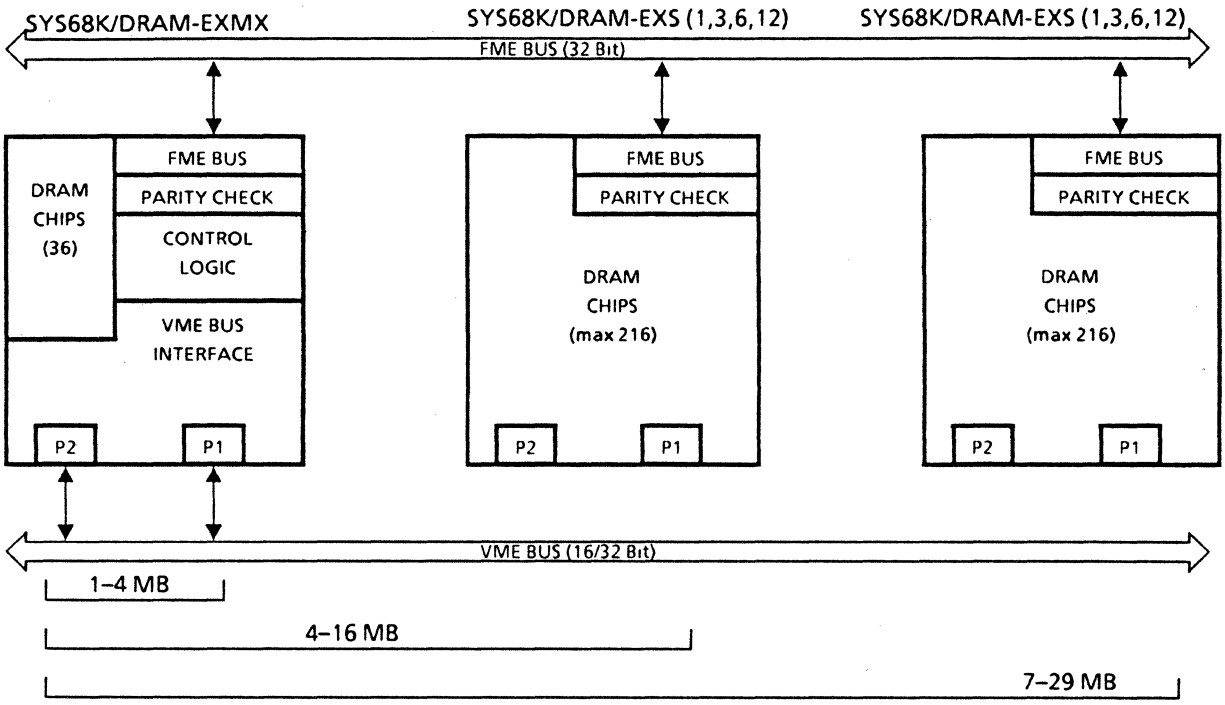
b) DRAM-E4M4:

Board	Capacity
DRAM-E4S4	4Mbyte
DRAM-E4S12	12Mbyte

A maximum of 28Mbyte DRAM is provided using a DRAM-E4M4 and two DRAM-E4S12 boards.

Easy installation of the slave boards is provided through the 3rd 96 pin DIN connector.

Figure 4-1: The FME Concept



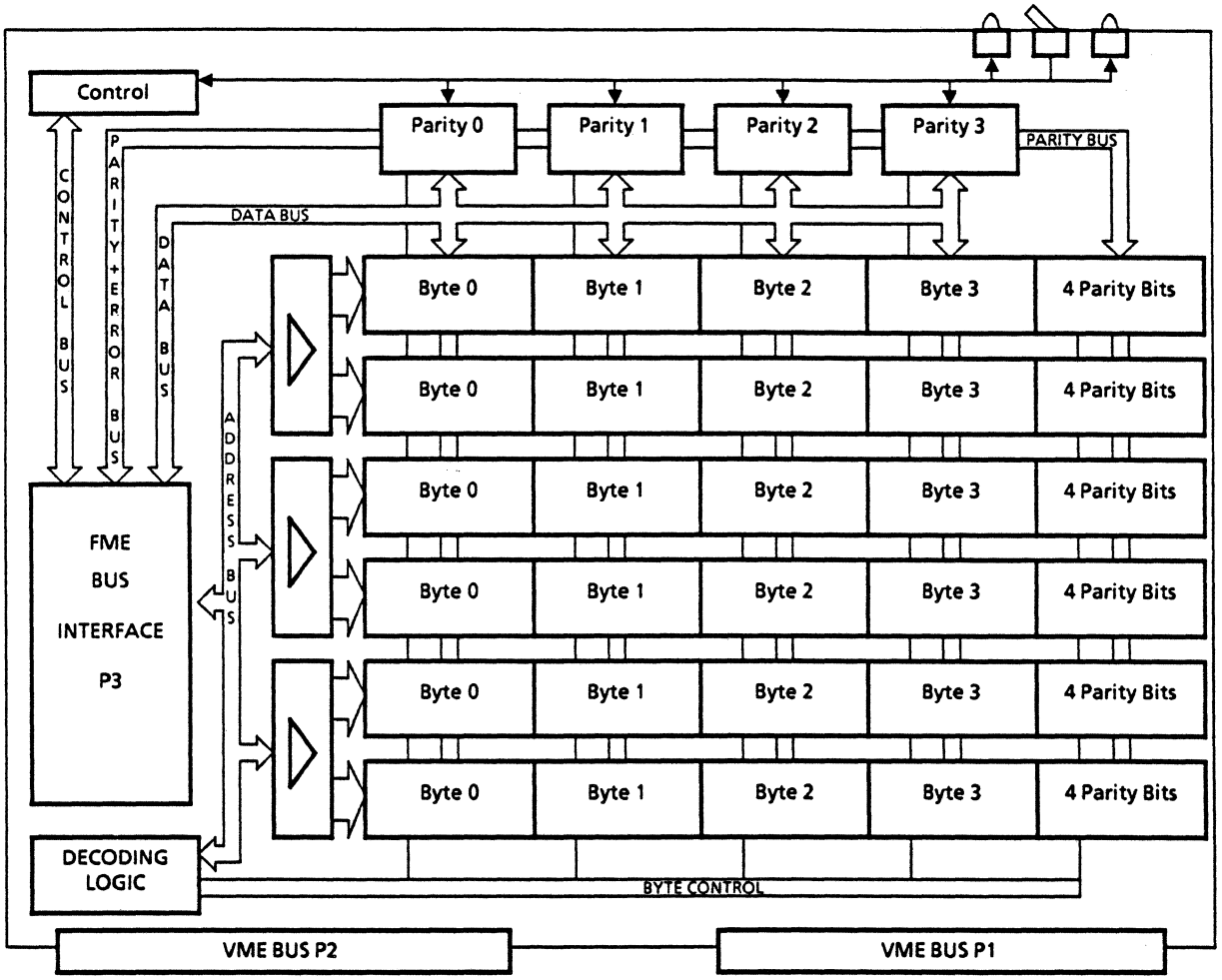
The connection as a second slave board requires a fulfilled first slave board (boards may be exchanged in order of position). Please follow the installation rules described in the Installation section of this manual (Register 2).

Table 4-1: Usable Slave Board Combinations

	1st Slave	2nd Slave	Total Memory Capacity
E3M1	--	--	1M byte
E3M1	E3S1	--	2M byte
E3M1	E3S3	--	4M byte
E3M1	E3S3	E3S1	5M byte
E3M1	E3S3	E3S3	7M byte
E3M1	E3S6	--	7M byte
E4M4	--	--	4M byte
E4M4	E4S4	--	8M byte
E4M4	E4S12	--	16M byte
E4M4	E4S12	E4S12	28M byte

A general block diagram of the DRAM-E3S6 board is shown in Figure 4-2.

Figure 4-2: Block Diagram of the SYS68K/DRAM-E3S6



4.1 Access Address Selection using FME Slave Boards

Due to the fact that the memory capacity is expanded using DRAM-E3SX boards (see Table 4-1), the access address selection has to be changed. The general calculation rules, outlined in Chapter 3.2.2, are usable to reconfigure the default setup of the board.

The default access address selection of each DRAM-EXMX board is outlined in Chapter 3.2.1.

Table 4-2 lists the extension of the default access address selection using a DRAM-E3S1 board. Table 4-3 lists the extension using a DRAM-E3S3 board while Table 4-4 lists the extension with a DRAM-E3S6 board. All other modifications are similar to the listed examples.

Table 4-6 lists the extension of the default access address selection using a DRAM-E4S12 board. Table 4-7 lists the extension using two DRAM-E4S12 boards.

Warning: The simultaneous use of SYS68K/DRAM-E3MX and SYS68K/DRAM-E4SX boards is not allowed. Should this warning be ignored, then the RAM modules may be destroyed.

Table 4-2: Access Address Selection using one DRAM-E3S1

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
	5-6			5-6		A22
		1-8				A21
						A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FF2F FFFF	$2F FFFF
First not on-board Address:	$FF30 0000	$30 0000
Boundary:	$0020 0000	$20 0000
	2M byte	2M byte

Table 4-3: Access Address Selection using one DRAM-E3S3

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
	5-6					A22
		1-8			1-8	A21
						A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FF4F FFFF	$4F FFFF
First not on-board Address:	$FF50 0000	$50 0000
Boundary:	$0040 0000	$40 0000
	4M byte	4M byte

Table 4-4: Access Address Selection using one DRAM-E3S6 or two DRAM-E3S3 Boards

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7					A23
	5-6			5-6		A22
		1-8			1-8	A21
					2-7	A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FF7F FFFF	$7F FFFF
First not on-board Address:	$FF80 0000	$80 0000
Boundary:	$0070 0000	$70 0000
	7M byte	7M byte

Table 4-5: Access Address Selection using two DRAM-E3S6

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7					A23
	5-6					A22
		1-8				A21
					2-7	A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FFDF FFFF	$DF FFFF
First not on-board Address:	$FFE0 0000	$E0 0000
Boundary:	$00D0 0000	$D00 000
	13M byte	13M byte

Table 4-6: Access Address Selection using DRAM-E4S12

Jumper B18 must be inserted. (Mode A32)

Start Address			First not on-board Address			Corresponding Bus Address Signal	
B7	B8	B9	B4	B5	B6		HEX
1-10			1-10			A31	8
2-9			2-9			A30	4
3-8			3-8			A29	2
4-7			4-7			A28	1
5-6			5-6			A27	8
	1-10			1-10		A26	4
	2-9			2-9		A25	2
	3-8					A24	1
	4-7			4-7		A23	8
	5-6			5-6		A22	4
		1-8			1-8	A21	2
						A20	1
		3-6			3-6	A19	8
		4-5			4-5	A18	4

	A32	A24
Start Address:	$0010 0000	
End Address:	$010F FFFF	
First not on-board Address:	$0110 0000	
Boundary:	$0100 0000	
	16M byte	

Table 4-7: Access Address Selection using two DRAM-E4S12 Boards

Jumper B18 must be inserted (Mode A32)

Start Address			First not on-board Address			Corresponding Bus Address Signal	
B7	B8	B9	B4	B5	B6		HEX
1-10			1-10			A31	8
2-9			2-9			A30	4
3-8			3-8			A29	2
4-7			4-7			A28	1
5-6			5-6			A27	8
	1-10			1-10		A26	4
	2-9			2-9		A25	2
	3-8					A24	1
	4-7					A23	8
	5-6					A22	4
		1-8			1-8	A21	2
						A20	1
		3-6			3-6	A19	8
		4-5			4-5	A18	4

	A32	A24
Start Address:	$0010 0000	
End Address:	$01CF FFFF	
First not on-board Address:	$D1D0 0000	
Boundary:	$01C0 0000	
	29M byte	

5.Ø Preparation for Use

a) Please read the complete manual for easy and correct board handling.

b) Make optical check of the multi-layer board and the components for eventual damages prior to mounting the board.

c) Use adequate electrical outlets for check.

d) Use adequate equipment for electrical check (i.e. volt meter).

e) Use power supply with sufficient drive capacity within the VMEbus tolerances.

f) To initialize the DRAM-EXMX and its connected slave boards an initialization routine has to be installed before reading from the board.

The following program example (subroutine) is useful for initialization:

```
STARTADR    =    first on-board address
ENDADR      =    last on-board address

        START   LEA.L    STARTADR,AØ
                LEA.L    ENDADR,Al
        LOOP    MOVE.W   #Ø,(AØ)+
                CMPA.L   Al,AØ
                BLT.S    LOOP
                RTS
```

Note: The initialization of the DRAM cells has to be done with word moves.

5.1 Power On

When the board is mounted in a VMEbus environment and the power is stable, transfers to and from the board can be forced.

Caution: If the board has not been initialized, parity errors may occur during read cycle because the data bits of the DRAMs are not in a definite state after power up.

Normal access can be forced to the default set address ranges if the following items are provided:

a) RUN/LOCAL switch is in RUN mode.

b) The current bus master can force an access to this board under the default access address range and AM code.

Access Address Range:	$FF1Ø Ø ØØ	Start A32 Mode
	$FF1FF FFF	End A32 Mode
	$1Ø Ø ØØ	Start A24 Mode
	$1FF FFF	End A24 Mode
Selected AM Codes:	Ø9, ØA, ØD, ØE	
	39, 3A, 3D, 3E	

APPENDIX TO THE HARDWARE USER'S MANUAL FOR DRAM-E3M1/E4M4

Appendices

Appendix A

Specification SYS68K/DRAM-E3M1

Capacity:	1M byte dynamic RAM including Byte Parity Check
Organisation:	36 bit internally including 4 parity bits
Data Transfer Modes:	A24:D8 ; A24:D16 ; A24:D24 ; A24:D32 A32:D8 ; A32:D16 ; A32:D24 ; A32:D32
Access Times:	Write: 70ns (typ) with Parity generation Read: 245ns (typ) with Parity check 210ns (typ) without Parity check
Refresh:	Interleave every 15us
Decoding:	Jumper selectable Access Address in 256K byte increments and Address Modifier Code (any combination of 10 AM codes)
Specials:	Through FMEbus (up to 13M bytes)
Memory Expansion:	Battery backup through P2 RUN/LOCAL switch RUN/LOCAL & ERROR/ACCESS LEDs
Power Requirements:	+5V 5.9A (refresh peak) +5V 4.3A (average max) +5V 3.2A (average typ) +5V STDBY 3.9A (refresh peak) +5V STDBY 1.9A (average max) +5V STDBY 1.7A (average typ)
Operating Temperature:	0 to +60 degrees C
Storage Temperature:	-55 to +85 degrees C
Relative Humidity:	0-95% (non-condensing)
Dimensions:	Double Eurocard 233x160mm (9.2x6.3")

Appendix A

Specification SYS68K/DRAM-E4M4

Capacity:	4Mbyte dynamic RAM including Byte Parity Check
Organisation:	36 bit internally including 4 parity bits
Data Transfer Modes:	A24:D8 ; A24:D16 ; A24:D24 ; A24:D32 A32:D8 ; A32:D16 ; A32:D24 ; A32:D32
Access Times:	Write: 65ns (typ) with Parity generation Read: 240ns (typ) with Parity check 210ns (typ) without Parity check
Refresh:	Interleave every 15us
Decoding:	Jumper selectable Access Address in 256K byte increments and Address Modifier Code (any combination of 10 AM codes)
Specials:	Battery backup through P2 RUN/LOCAL switch RUN/LOCAL & ERROR/ACCESS LEDs
Memory Expansion:	Through FMEbus (up to 29Mbytes)
Power Requirements:	+5V 5.9A (refresh peak) +5V 4.3A (average max) +5V 3.2A (average typ) +5V STDBY 2.4A (refresh peak) +5V STDBY 1.9A (average max) +5V STDBY 1.7A (average typ)
Operating Temperature:	0 to +60 degrees C
Storage Temperature:	-55 to +85 degrees C
Relative Humidity:	0-95% (non-condensing)
Dimensions:	Double Eurocard 233x160mm (9.2x6.3")

Appendix B

Component Part List **SYS68K/DRAM-E3M1** and **SYS68K/DRAM-E4M4**
BB Rev. 5 BB Rev.0
PRN 500 PRN 001
Date 26/9/86 Date 13/8/86

ICs

Location	Type	Manufacturer
J1 - J36	RAMs	See page B-10
J73	74F244	MOT, F, VALVO
J75	AM2966	AMD
J76	74F373	MOT, F, VALVO
J77	74F32	MOT, F, VALVO
J78	74F38	MOT, F, VALVO
J80	74F280A	MOT, VALVO
J81	74F280A	MOT, VALVO
J82	74F243	MOT, F, VALVO
J83	FRC 82	FORCE 20L8A (MMI)
J84	74F280A	MOT, VALVO
J85	74F280A	MOT, VALVO
J86	FRC 79	FORCE 20L8A (MMI)
J87	FRC 77	FORCE 16L8A (MMI)
J88	FRC 78	FORCE 16L8A (MMI)
J90	74F373	MOT, F, VALVO
J91	74F373	MOT, F, VALVO
J92	74F373	MOT, F, VALVO
J93	Decoder	See page B10
J94	74F241	MOT, F, VALVO

A p p e n d i x B

Component Part List SYS68K/DRAM-E3M1 and DRAM-E4M4

ICs

Location	Type	Manufacturer
J95	74F241	MOT, F, VALVO
J96	74F241	MOT, F, VALVO
J97	74F241	MOT, F, VALVO
J98	74F112	MOT, F, VALVO
J99	74LS244	MOT, TI
J100	74LS393	MOT, TI
J105	74F74	MOT, F, VALVO
J106	74AS374	TI
J107	74AS374	TI
J108	74AS374	TI
J109	74AS374	TI
J110	74AS374	TI
J111	74AS374	TI
J112	74F373	MOT, F, VALVO
J113	74F373	MOT, F, VALVO
J114	74F373	MOT, F, VALVO
J115	74F373	MOT, F, VALVO
J116	74F373	MOT, F, VALVO
J117	74F373	MOT, F, VALVO
J118	74F85	MOT, F, VALVO

A p p e n d i x B

Component Part List SYS68K/DRAM-E3M1 and DRAM-E4M4

ICs

Location	Type	Manufacturer
J119	74F85	MOT, F, VALVO
J120	74F85	MOT, F, VALVO
J121	74F85	MOT, F, VALVO
J122	74F85	MOT, F, VALVO
J123	74F85	MOT, F, VALVO
J124	74F85	MOT, F, VALVO
J125	74F85	MOT, F, VALVO
J126	74F04	MOT, F, VALVO
J127	74F11	MOT, F, VALVO
J128	74F20	MOT, F, VALVO
J129	74F109	MOT, F, VALVO
J130	74F109	MOT, F, VALVO
J131	74S240	TI, MOT
J132	74F240	MOT, F, VALVO
J133	74F112	MOT, F, VALVO
J134	DDU-7J-100	TOKO
J135	DDU-7J-200	TOKO
J136	DDU-7J-200	TOKO
J137	FRC 76	FORCE 20L8A (MMI)
J139	74F86	MOT, F, VALVO

Appendix B

Component Part List SYS68K/DRAM-E3M1 and DRAM-E4M4

ICs

Location	Type	Manufacturer
J140	74F86	MOT, F, VALVO
J141	74LS395	MOT, TI
J142	74F08	MOT, F, VALVO
J143	74F38	MOT, F, VALVO
J144	74F38	MOT, F, VALVO
J145	74F13	MOT, F, VALVO
J146	74F32	MOT, F, VALVO
J147	74F132	MOT, F, VALVO
J148	74F86	MOT, F, VALVO
J149	74F08	MOT, F, VALVO
J151	74F11	MOT, F, VALVO
J152	74LS74A	MOT, TI
J153	74LS74A	MOT, TI
J154	74LS123	MOT, TI
J155	75LS240	MOT, TI
J156	74F283	MOT, F, VALVO
J157	74F283	MOT, F, VALVO
J158	74F38	MOT, F, VALVO
J159	TL7705	TI
J160	FRC 81	FORCE 16L8A (MMI)

A p p e n d i x B

Component Part List SYS68K/DRAM-E3M1 and DRAM-E4M4

DIODES

Location	Type	Manufacturer
LD1	2206	DIALIGHT (GREEN)
LD2	2406	DIALIGHT (RED)
LD3	2306	DIALIGHT (YELLOW)

RESISTORS, NETWORKS

Location	Type	Manufacturer
R1	5*33 10 PIN	VARIOUS
R2	5*47 10 PIN	VARIOUS
R3	9*3.3K 10 PIN	VARIOUS
R7	9*680 10 PIN	VARIOUS
R8	9*3.3K 10 PIN	VARIOUS
R10	9*3.3K 10 PIN	VARIOUS
R11	9*3.3K 10 PIN	VARIOUS
R12	9*3.3K 10 PIN	VARIOUS
R13	9*3.3K 10 PIN	VARIOUS
R14	9*3.3K 10 PIN	VARIOUS
R16	9*3.3K 10 PIN	VARIOUS

Appendix B

Component Part List SYS68K/DRAM-E3M1 and DRAM-E4M4

RESISTORS, NETWORKS

Location	Type	Manufacturer
R17	3.3K	VARIOUS
R18	----	---
R23	5*100 10 PIN	VARIOUS
R27	100	VARIOUS
R40	150	VARIOUS
R42	27	VARIOUS
R43	2.2K	VARIOUS
R51	3.3K	VARIOUS
R53	9*3.3K 10 PIN	VARIOUS
R54	9*680 10 PIN	VARIOUS
R69	68	VARIOUS
R70	330	VARIOUS
R73	3.3K	VARIOUS
R74	220	VARIOUS
R75	3.3K	VARIOUS

A p p e n d i x B

Component Part List SYS68K/DRAM-E3M1 and DRAM-E4M4

CAPACITORS

Location	Type	Manufacturer
C1	0.015uF	VARIOUS
C2	4700pF	VARIOUS
C3	470pF ± 5%	VARIOUS
C4	10.5-60pF	VARIOUS
C5-C60	100nF	VARIOUS
C61	0.luF ± 5%	VARIOUS
C62	0.luF ± 5%	VARIOUS
C63	0.luF ± 5%	VARIOUS
C64	680pF ± 5%	VARIOUS
C65	100uF/10V ELKO RM 5.08mm	VARIOUS

Appendix B

Component Part List SYS68K/DRAM-E3M1 and DRAM-E4M4

MECHANICAL PARTS

Location	Type	Manufacturer
B2	DW16	VARIOUS
B4 + B5	DW10	VARIOUS
B6 + B9	DW16	VARIOUS
B7 + B8	DW10	VARIOUS
B10	--	---
B11	DW14	VARIOUS
B14	DW6	VARIOUS
B18	EW2	VARIOUS
B20	EW2	VARIOUS
B25	EW3	VARIOUS
SW1	AT-1D SWITCH	KNITTER
P1	VG CONNEC 96	VARIOUS
P2	VG103-40021	VARIOUS
P3	VG115-40062	VARIOUS
J83	24 PIN SOCKET	VARIOUS
J86	24 PIN SOCKET	VARIOUS
J87	20 PIN SOCKET	VARIOUS
J88	20 PIN SOCKET	VARIOUS
J93	24 PIN SOCKET	VARIOUS
J137	24 PIN SOCKET	VARIOUS
J160	20 PIN SOCKET	VARIOUS
	Jumpers-A	Jumpers for Headers (23)

A p p e n d i x B

Component Part List SYS68K/DRAM-E3M1 and DRAM-E4M4

MECHANICAL PARTS

	ATTACHED PARTS
1)	SYS68K/DRAM-E3XX User's Manual
2)	Product Release Note

Appendix B

Component Part List SYS68K/DRAM-E3M1 and DRAM-E4M4

Component Part List SYS68K/DRAM-E3M1

Location	Type	Manufacturer
J1 to J36	RAMs 256 Kbit 120ns	Toshiba TMK41256P-12 NEC uPD41256C-12 HIT Mitsu
J93	FRC 80	FORCE 20L8B
DRAM-E3MD	PCB	FORCE
DRAM-E3FP	Front Panel	FORCE

Component Part List SYS68K/DRAM-E4M4

Location	Type	Manufacturer
J1 to J36	RAMs 1 Mbit 120ns	Toshiba TC511000C-12 NEC uPD411000C-12 HIT
J93	FRC 117	FORCE 20L8B
J1 to J36	18 PIN Socket	VARIOUS
DRAM-E4M4	PCB	FORCE
DRAM-E4FP	Front Panel	FORCE

Appendix C

Description of the Jumperfields

Appendix C

Description of the Jumperfields

Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B2	Address Modifier Code Selection	1-16 2-15 3-14 4-13 5-12 6-11 7-10 8- 9	6-01	162	29	28

Default: B2 all Jumpers IN

Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B3	Address Modifier Code Selection	-	6-01	162	29	28

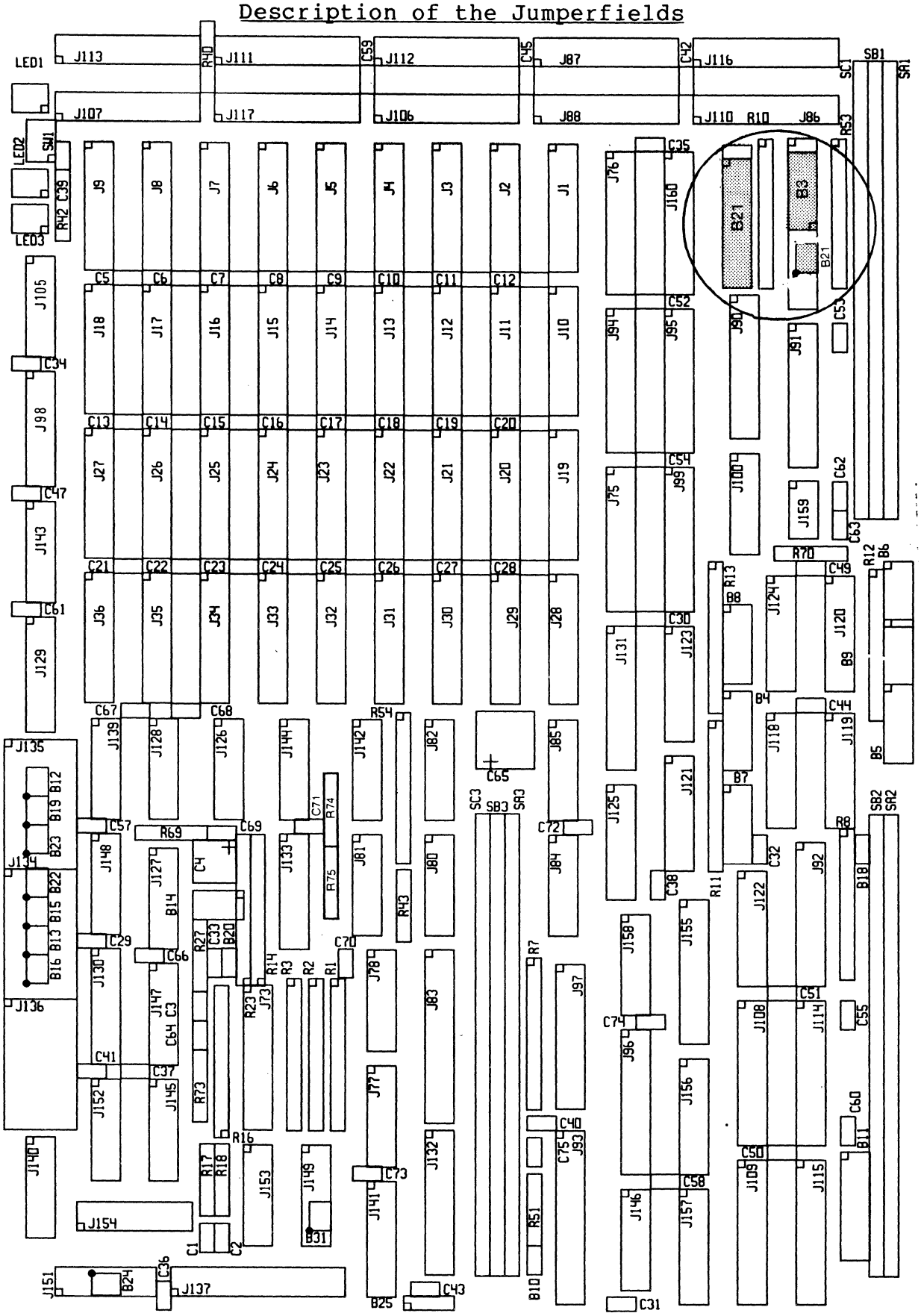
Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B21	Address Modifier Code	-	6-C2	147	18	-

- for internal use only.

B3 and B21 are only connected with soldering bridges.

Appendix C

Description of the Jumperfields



Appendix C

Description of the Jumperfields

Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B4		-				
+B5	Access Address Selection First not on board Address (MAD)	5-A1 4-7 5-6	5-A1	89/29 90/6 107/6		17
+B6		2-7 3-6 4-7				
B7		-				
+B8	Access Address Selection First on board address Start address (LAD)	5-A3 4-7 5-6	5-A3	75/29 105/29 95/6		17
+B9		1-8 3-6 4-7				

Default Address: For 24 Bit B18 OUT

First not on board	$	XX10	0000
First not on board	$	XX20	0000

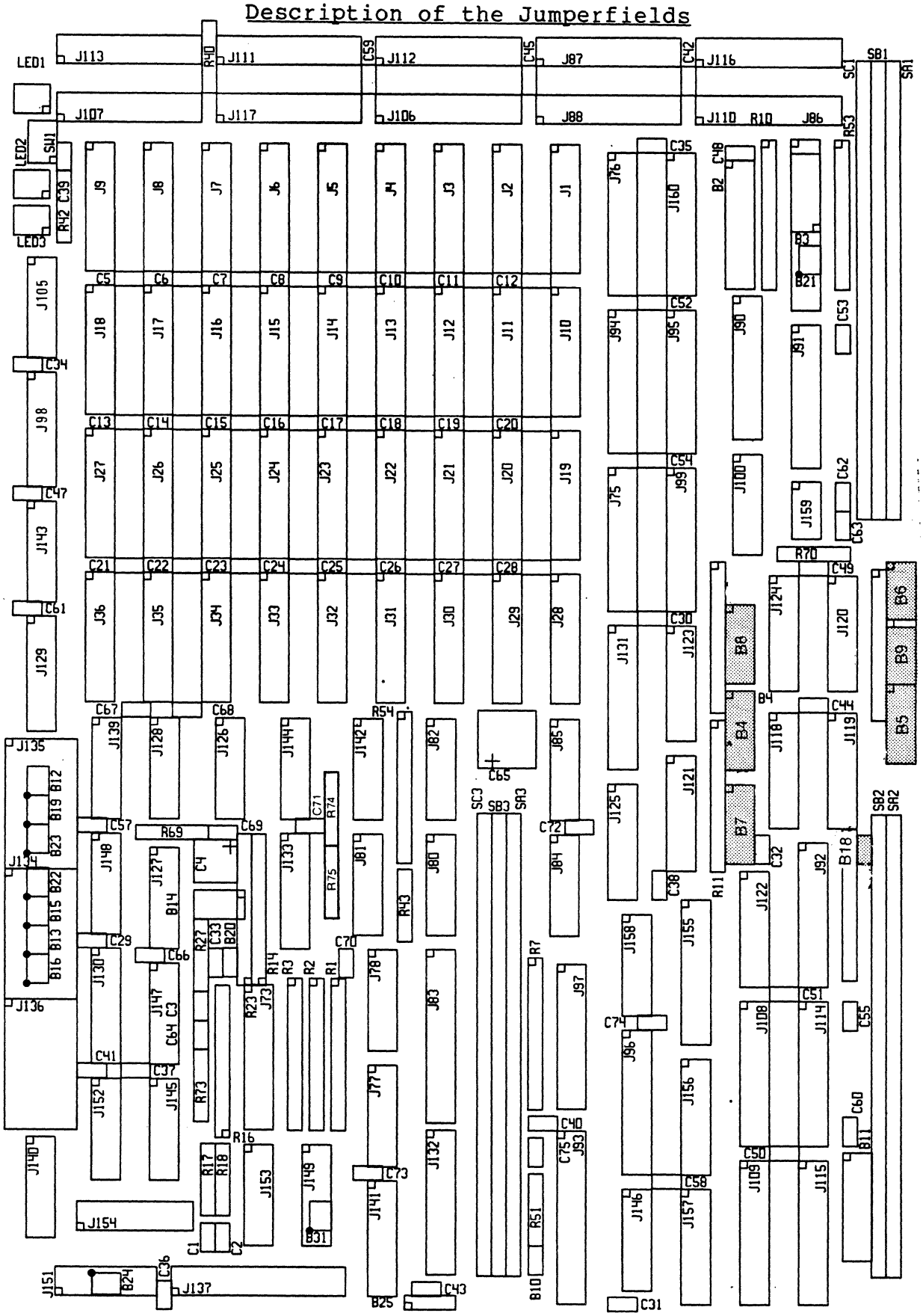
For 32 Bit B18 IN

First not on board	$	FF10	0000
First on board	$	FF20	0000

Jumper-Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B18	Disable/Enable Address Lines A24-A31	-	3-B2	69/10		19

Appendix C

Description of the Jumperfields



Appendix C

Description of the Jumperfields

Jumper Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B11	Battery Backup Option	1-14 2-13 3-12	2-B4	25/12		40

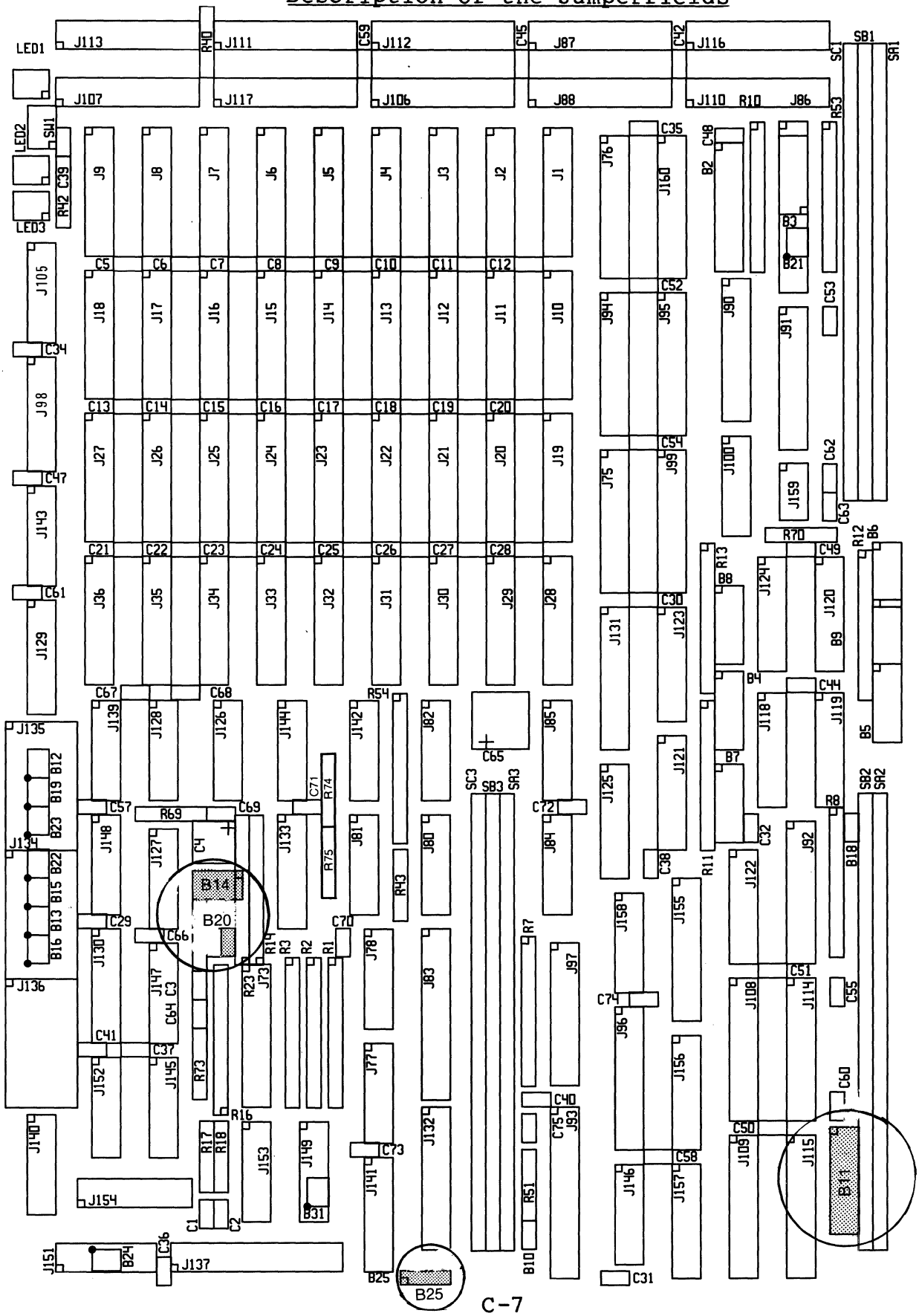
Jumper -Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B14	Read Access Select	2-5	7-A4	60/94		36
B20	Parity Error to BERR	1-2	2C-3	54/96		36

Jumper -Field	Description	Default Cond.	Schematics	Location Coord. x	Location Coord. y	see pg
B25	AS* Start AS* and DSO* or DS1	1 O 2 O 3 O	2-C1	15/86		-

- for internal use only.

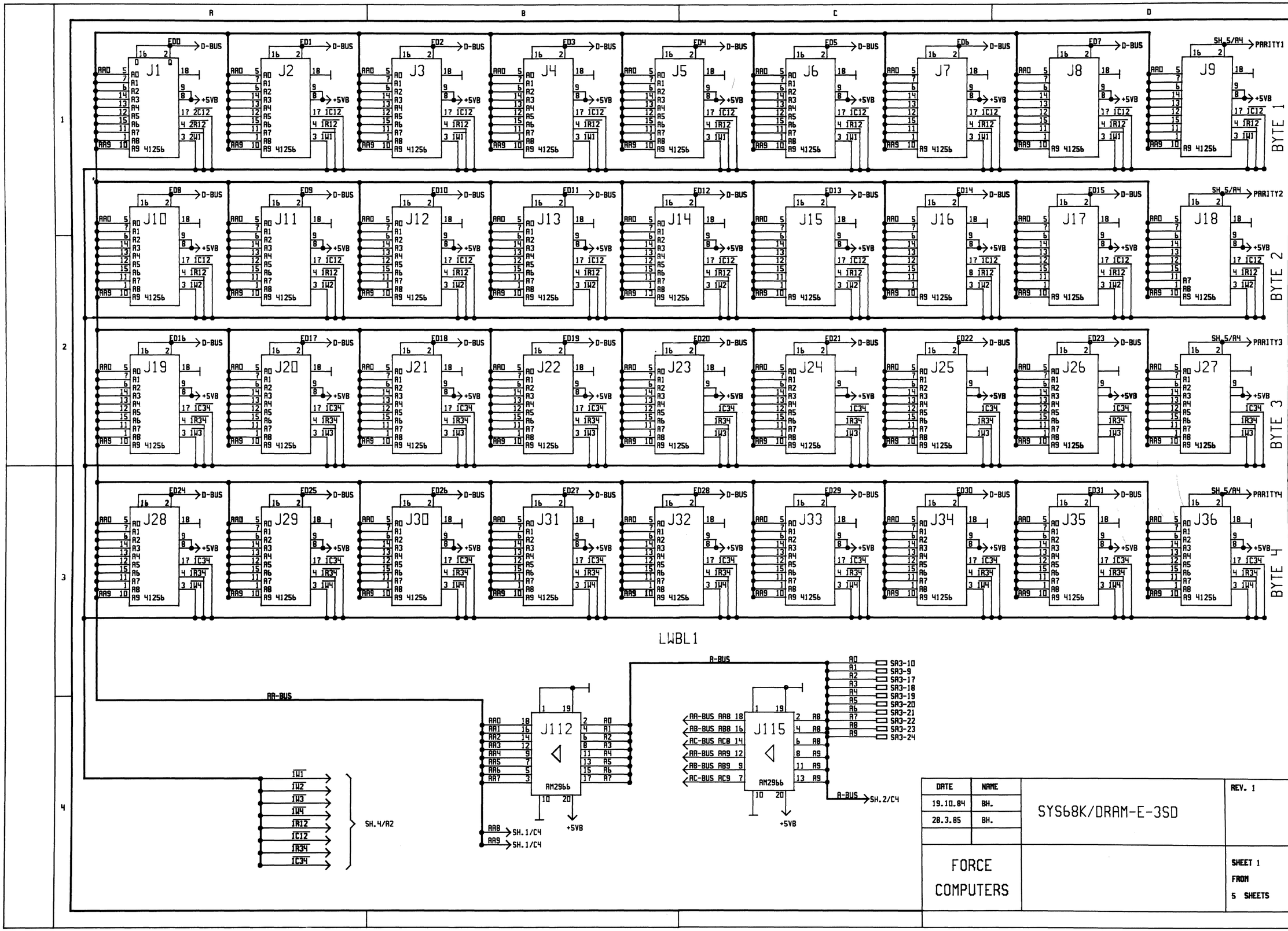
Appendix C

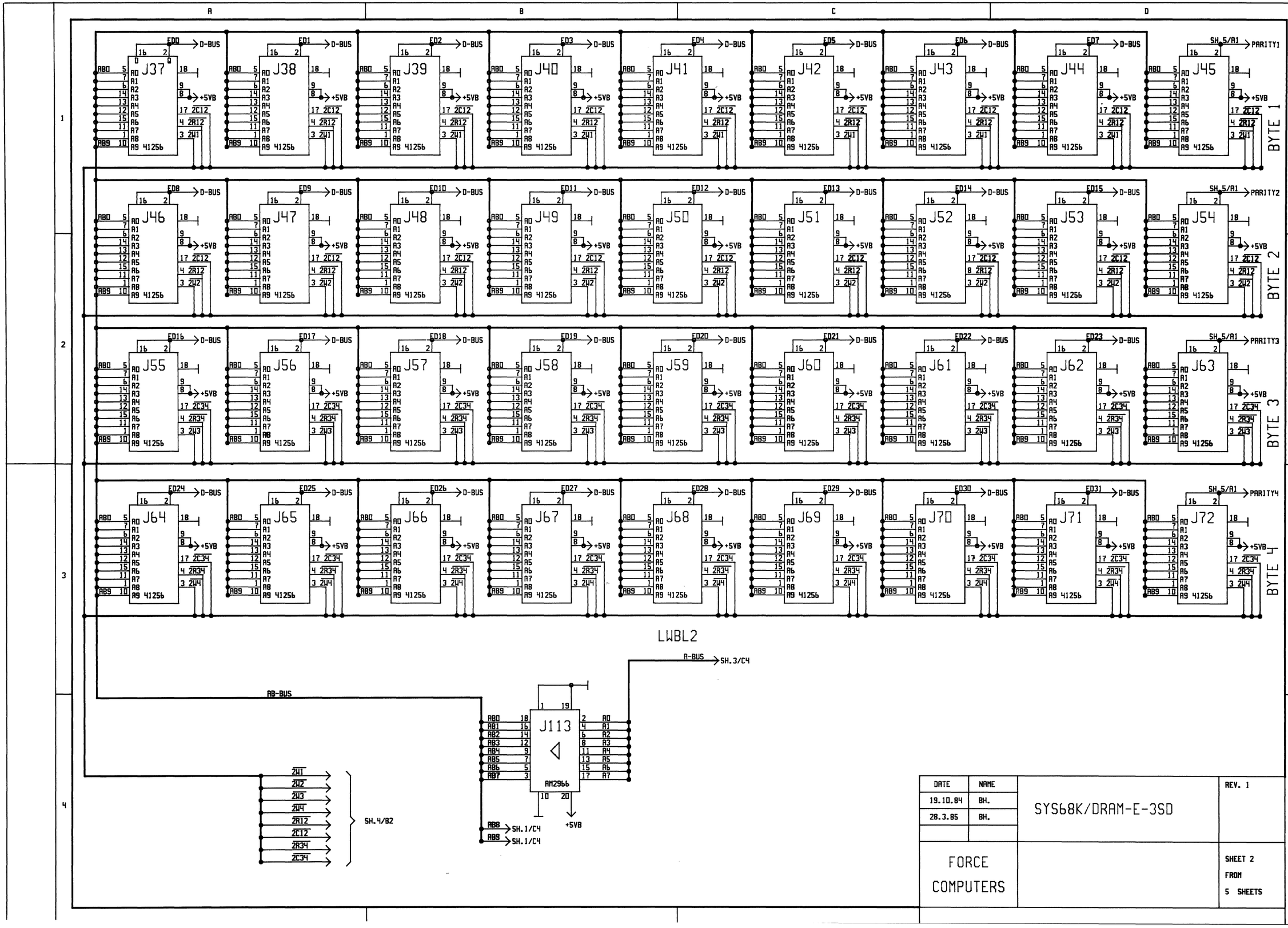
Description of the Jumperfields



Appendix D

Circuit Schematics


A
B
C
D
1
2
3
4
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
J13
J14
J15
J16
J17
J18
J19
J20
J21
J22
J23
J24
J25
J26
J27
J28
J29
J30
J31
J32
J33
J34
J35
J36
D-BUS
+5VB
A9 41256
BYTE 1
BYTE 2
BYTE 3
BYTE 4
PARITY1
PARITY2
PARITY3
PARITY4
LWBL1
A-BUS
AA-BUS
J112
J115
AM2966
SH.4/A2
SH.1/C4
SH.2/C4
SA3-10
SA3-9
SA3-17
SA3-18
SA3-19
SA3-20
SA3-21
SA3-22
SA3-23
SA3-24
DATE
NAME
19.10.84
BH.
28.3.85
BH.
SYS68K/DRAM-E-3SD
REV. 1
FORCE
COMPUTERS
SHEET 1
FROM
5 SHEETS


A
B
C
D
1
2
3
4
ED0 D-BUS J37 BYTE 1
ED1 D-BUS J38
ED2 D-BUS J39
ED3 D-BUS J40
ED4 D-BUS J41
ED5 D-BUS J42
ED6 D-BUS J43
ED7 D-BUS J44
SH.5/A1 PARITY1 J45
ED8 D-BUS J46 BYTE 2
ED9 D-BUS J47
ED10 D-BUS J48
ED11 D-BUS J49
ED12 D-BUS J50
ED13 D-BUS J51
ED14 D-BUS J52
ED15 D-BUS J53
SH.5/A1 PARITY2 J54
ED16 D-BUS J55 BYTE 3
ED17 D-BUS J56
ED18 D-BUS J57
ED19 D-BUS J58
ED20 D-BUS J59
ED21 D-BUS J60
ED22 D-BUS J61
ED23 D-BUS J62
SH.5/A1 PARITY3 J63
ED24 D-BUS J64 BYTE 4
ED25 D-BUS J65
ED26 D-BUS J66
ED27 D-BUS J67
ED28 D-BUS J68
ED29 D-BUS J69
ED30 D-BUS J70
ED31 D-BUS J71
SH.5/A1 PARITY4 J72
AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 AB9
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 41256
+5VB
2C12 2R12 2W1
2C12 2R12 2W2
2C34 2R34 2W3
2C34 2R34 2W4
LWBL2
A-BUS
SH.3/C4
AB-BUS
J113
AM2966
SH.1/C4
SH.1/C4
+5VB
2W1 2W2 2W3 2W4 2R12 2C12 2R34 2C34
SH.4/B2
DATE NAME
19.10.84 BH.
28.3.85 BH.
SYS68K/DRAM-E-3SD
REV. 1
FORCE COMPUTERS
SHEET 2 FROM 5 SHEETS

DATE	NAME		REV.
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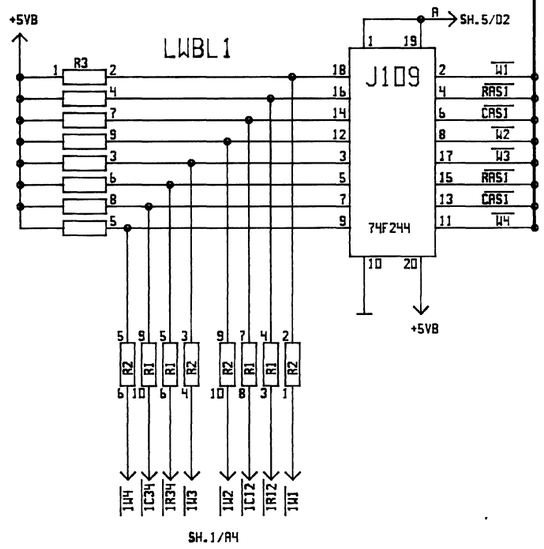
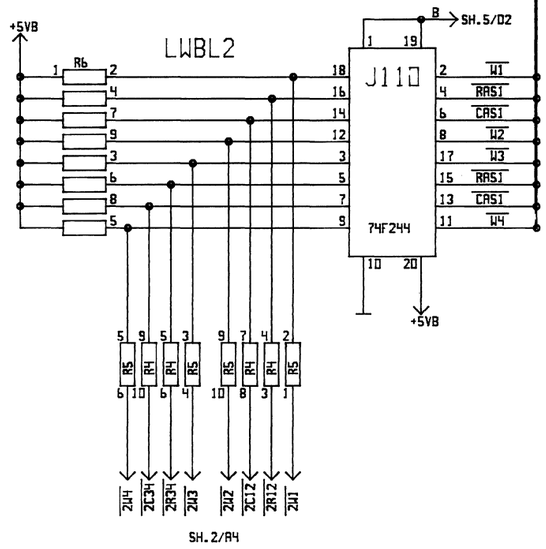
28.3.85	BH.		
FORCE COMPUTERS			SHEET 3 FROM 5 SHEETS



SH.1/A4



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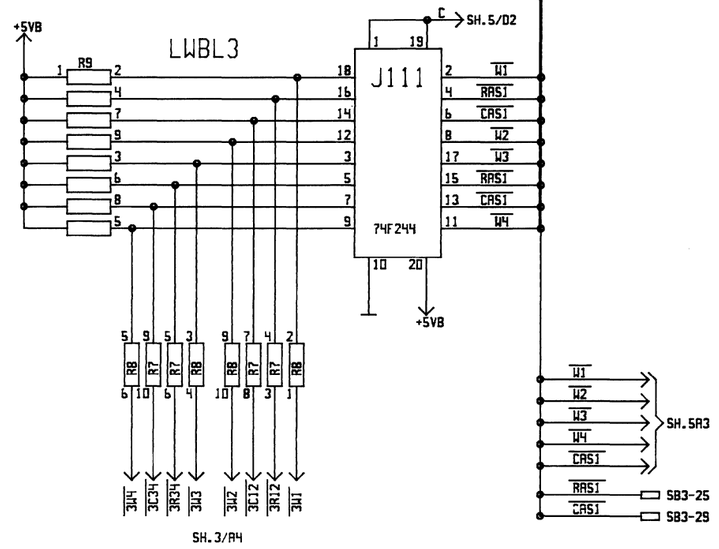

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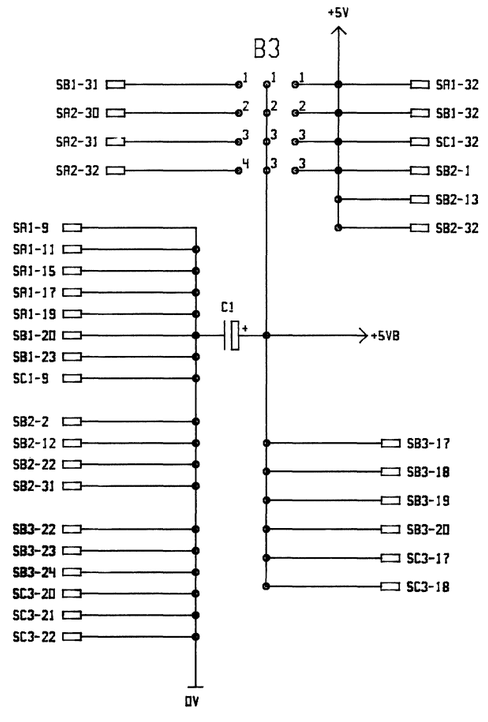

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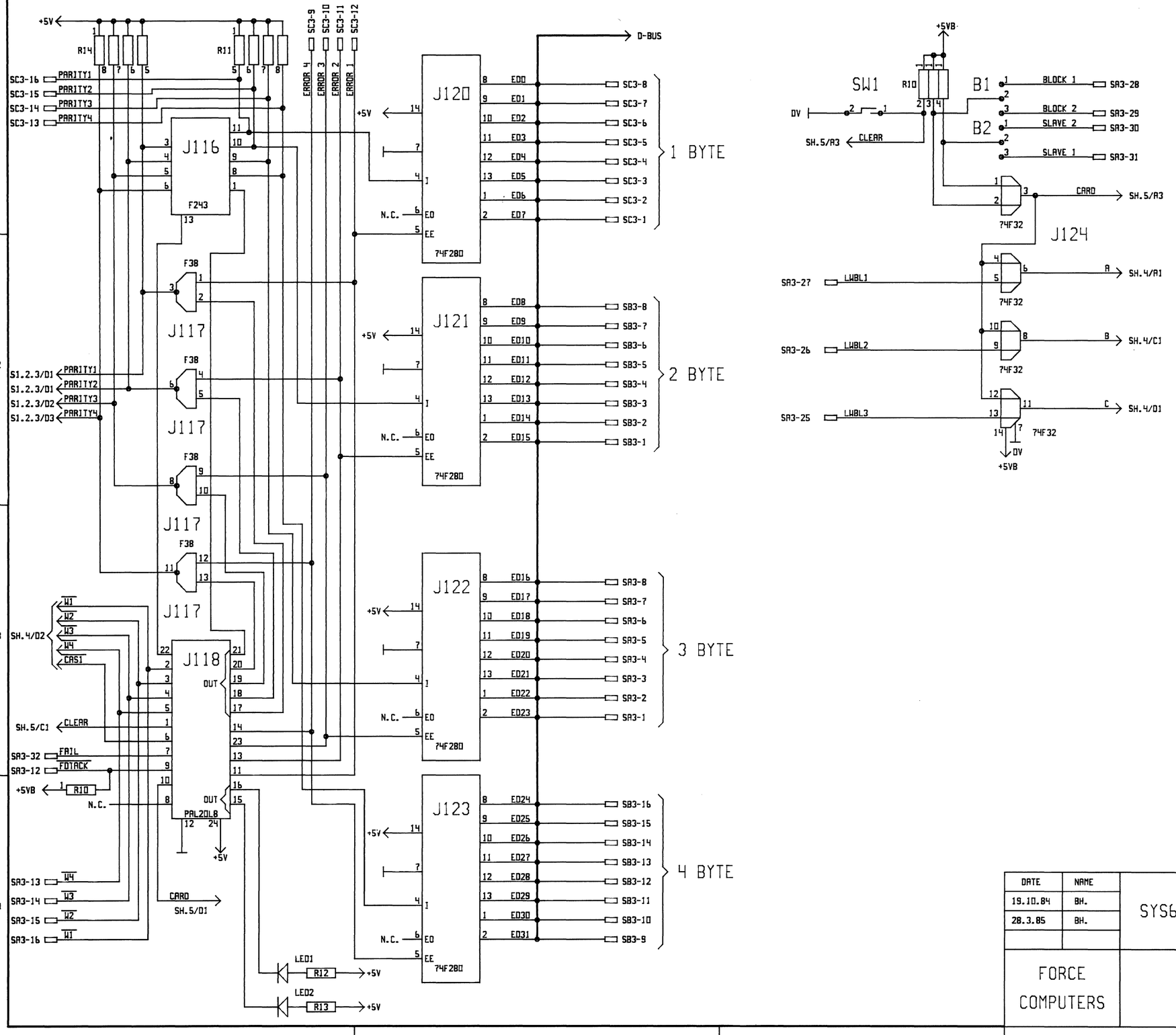

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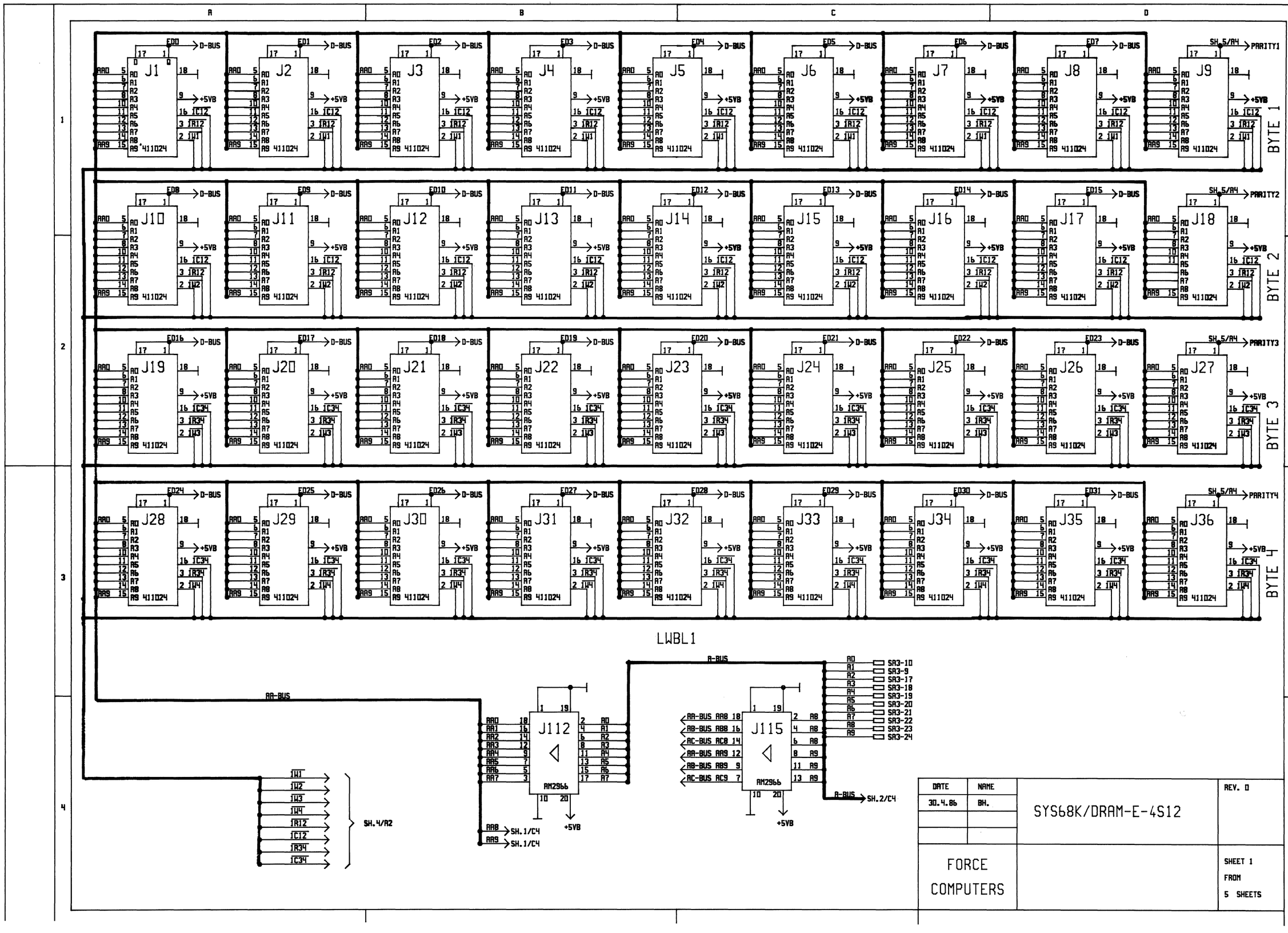
FORCE COMPUTERS			SHEET 5 FROM 5 SHEETS



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FORCE COMPUTERS			SHEET 1 FROM 5 SHEETS

DATE	NAME		REV. D
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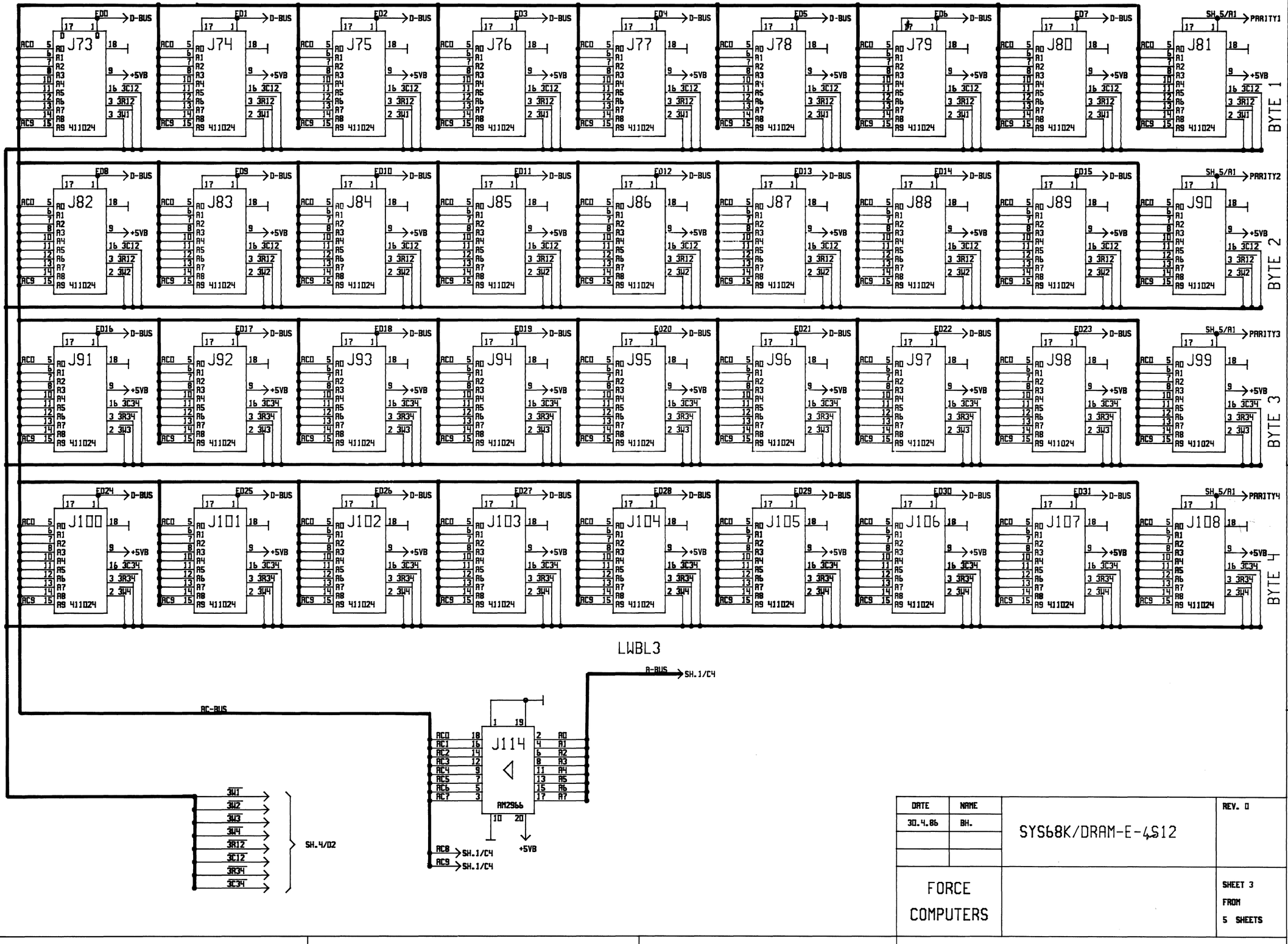

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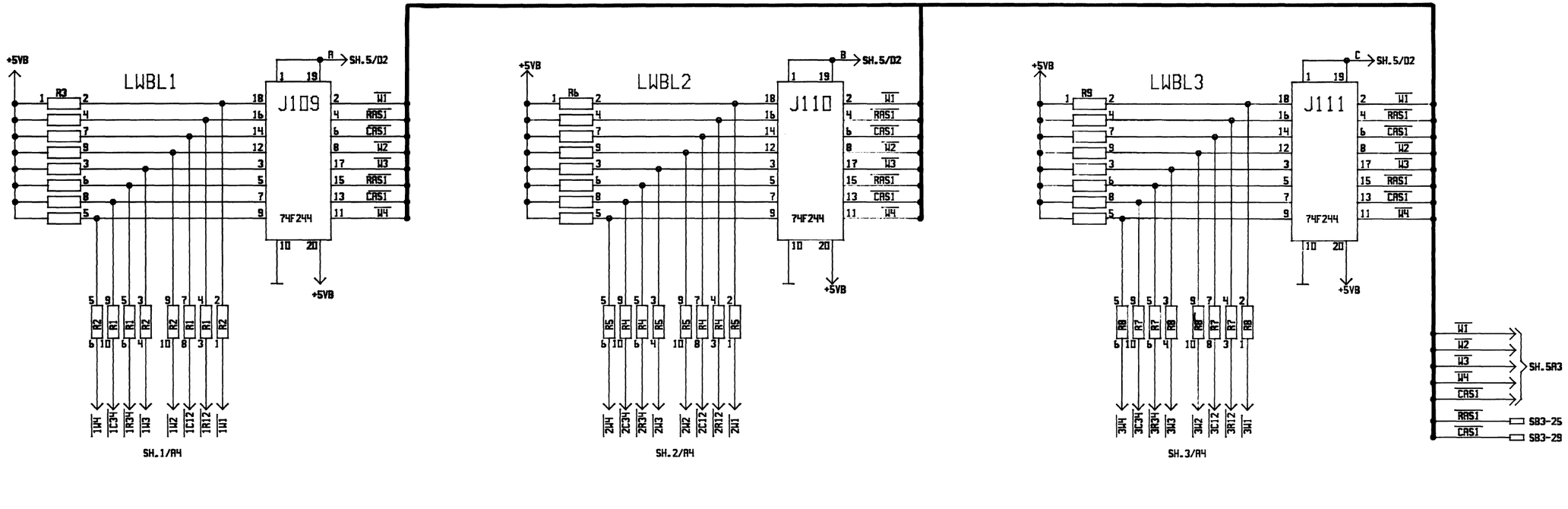

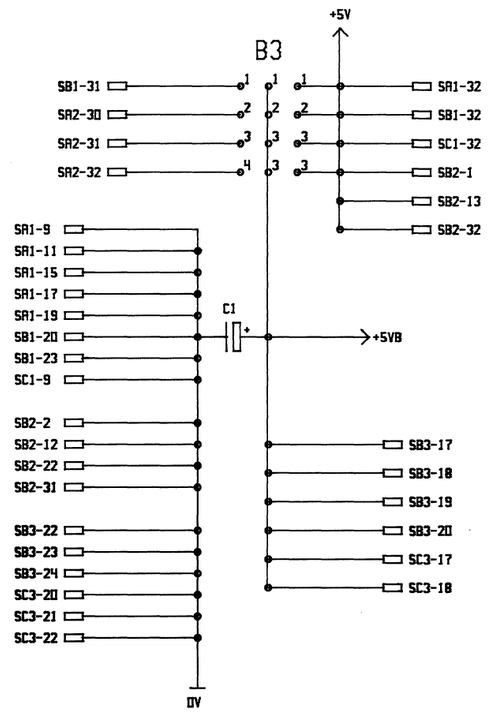

DATE	NAME		REV. D
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FORCE COMPUTERS			SHEET 4 FROM 5 SHEETS

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B
C
D
1
2
3
4
+5V
R14
R11
SC3-16
SC3-15
SC3-14
SC3-13
PARITY1
PARITY2
PARITY3
PARITY4
ERROR 4
ERROR 3
ERROR 2
ERROR 1
SC3-9
SC3-10
SC3-11
SC3-12
J116
F243
J117
F38
S1.2.3/D1
S1.2.3/D1
S1.2.3/D2
S1.2.3/D3
SH.4/D2
W1
W2
W3
W4
CAS1
J118
PAL20L8
OUT
SH.5/C1
CLEAR
SA3-32
FAIL
SA3-12
FDTACK
+5VB
R10
N.C.
SA3-13
SA3-14
SA3-15
SA3-16
CARD
SH.5/D1
LED1
R12
LED2
R13
D-BUS
J120
J121
J122
J123
74F280
N.C.
EO
EE
ED0
ED1
ED2
ED3
ED4
ED5
ED6
ED7
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SA3-8
SA3-7
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Appendix E

P3 Pin Assignment to FME Interface

Component Side

PIN NUMBER	ROW C SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW A SIGNAL MNEMONIC
1	Byte 1/7	Byte 2/7	Byte 3/7
2	Byte 1/6	Byte 2/6	Byte 3/6
3	Byte 1/5	Byte 2/5	Byte 3/5
4	Byte 1/4	Byte 2/4	Byte 3/4
5	Byte 1/3	Byte 2/3	Byte 3/3
6	Byte 1/2	Byte 2/2	Byte 3/2
7	Byte 1/1	Byte 2/1	Byte 3/1
8	Byte 1/Ø	Byte 2/Ø	Byte 3/Ø
9	Error 4	Byte 4/7	Address 2
1Ø	Error 3	Byte 4/6	Address 1
11	Error 2	Byte 4/5	EFDTACK*
12	Error 1	Byte 4/4	FDTACK*
13	Parity 4	Byte 4/3	WR 4
14	Parity 3	Byte 4/2	WR 3
15	Parity 2	Byte 4/1	WR 2
16	Parity 1	Byte 4/Ø	WR 1
17	+5V BATT.	+5V-	Address 3
18	+5V BATT.	+5V |-BATT.	Address 4
19	Reserved	+5V |	Address 5
2Ø	ØV	+5V-	Address 6
21	ØV	Reserved	Address 7
22	ØV	ØV	Address 8
23	Address 11	ØV	Address 9
24	Address 12	ØV	Address 1Ø
25	Address 13	RAS 1	LWBL 3
26	Address 14	RAS 2	LWBL 2
27	Address 15	RAS 3	LWBL 1
28	Address 16	RAS 4	Card 1(Block 1)
29	Address 17	CAS 1	Card 2(Block 2)
3Ø	Address 18	CAS 2	Card 3(Slave 2)
31	Address 19	CAS 3	Card 4(Slave 1)
32	Address 2Ø	CAS 4	FAIL

Appendix E

P3 Pin Assignments to FME Interface

Backside

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	Byte 3/7	Byte 2/7	Byte 1/7
2	Byte 3/6	Byte 2/6	Byte 1/6
3	Byte 3/5	Byte 2/5	Byte 1/5
4	Byte 3/4	Byte 2/4	Byte 1/4
5	Byte 3/3	Byte 2/3	Byte 1/3
6	Byte 3/2	Byte 2/2	Byte 1/2
7	Byte 3/1	Byte 2/1	Byte 1/1
8	Byte 3/Ø	Byte 2/Ø	Byte 1/Ø
9	Address 2	Byte 4/7	Error 4
1Ø	Address 1	Byte 4/6	Error 3
11	EFDTACK*	Byte 4/5	Error 2
12	FDTACK*	Byte 4/4	Error 1
13	WR 4	Byte 4/3	Parity 4
14	WR 3	Byte 4/2	Parity 3
15	WR 2	Byte 4/1	Parity 2
16	WR 1	Byte 4/Ø	Parity 1
17	Address 3	+5V-	+5V BATT.
18	Address 4	+5V |-BATT.	+5V BATT.
19	Address 5	+5V |	Reserved
2Ø	Address 6	+5V-	ØV
21	Address 7	Reserved	ØV
22	Address 8	ØV	ØV
23	Address 9	ØV	Address 11
24	Address 1Ø	ØV	Address 12
25	LWBL 3	RAS 1	Address 13
26	LWBL 2	RAS 2	Address 14
27	LWBL 1	RAS 3	Address 15
28	Card 1(Block 1)	RAS 4	Address 16
29	Card 2(Block 2)	CAS 1	Address 17
3Ø	Card 3(Slave 2)	CAS 2	Address 18
31	Card 4(Slave 1)	CAS 3	Address 19
32	FAIL	CAS 4	Address 2Ø

Appendix E

P1 Pin Assignments to VMEbus

PIN Number	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	D00	-	D08
2	D01	-	D09
3	D02	-	D10
4	D03	BG0IN* (1)	D11
5	D04	BG0OUT* (1)	D12
6	D05	BG1IN* (1)	D13
7	D06	BG1OUT* (1)	D14
8	D07	BG2IN* (1)	D15
9	GND	BG2OUT* (1)	GND
10	SYSCLK	BG3IN* (1)	-
11	GND	BG3OUT* (1)	BERR*
12	DS1*	-	SYSRESET*
13	DS0*	-	LWORD*
14	WRITE*	-	AM5
15	GND	-	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	-	GND	A18
21	IACKIN*	(1)	-A17
22	IACKOUT*	(1)	-A16
23	AM4	GND	A15
24	A07	-	A14
25	A06	-	A13
26	A05	-	A12
27	A04	-	A11
28	A03	-	A10
29	A02	-	A09
30	A01	-	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

Note (1): IN to OUT Connected

Appendix E

P2 Pin Assignments to VMEbus

PIN Number	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	-	+5V Volts	-
2	-	GND	-
3	-	RESERVED	-
4	-	A24	-
5	-	A25	-
6	-	A26	-
7	-	A27	-
8	-	A28	-
9	-	A29	-
10	-	A30	-
11	-	A31	-
12	-	GND	-
13	-	+5 Volts	-
14	-	D16	-
15	-	D17	-
16	-	D18	-
17	-	D19	-
18	-	D20	-
19	-	D21	-
20	-	D22	-
21	-	D23	-
22	-	GND	-
23	-	D24	-
24	-	D25	-
25	-	D26	-
26	-	D27	-
27	-	D28	-
28	-	D29	-
29	-	D30	-
30	User I/O	D31	-
31	User I/O	GND	-
32	User I/O	+5 Volts	-

User I/O for standby power connection.

Appendix F

PRODUCT ERROR REPORT

DEAR CUSTOMER,

WHILE FORCE COMPUTERS HAS ACHIEVED A VERY HIGH STANDARD OF QUALITY IN OUR PRODUCTS AND DOCUMENTATION, WE CONTINUALLY SEEK SUGGESTIONS FOR IMPROVEMENTS.

WE WOULD APPRECIATE ANY FEEDBACK YOU CARE TO OFFER.

PLEASE USE ATTACHED "PRODUCT ERROR REPORT" FORM FOR YOUR COMMENTS AND RETURN IT TO ONE OF OUR FORCE COMPUTERS OFFICES.

SINCERELY

FORCE COMPUTERS

HARDWARE USER'S MANUAL

DRAM-E3SX AND E4SX

Table of Contents

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List of Tables

1.Ø General Information

The family of SYS68K/DRAM-EXSX boards are high speed dynamic memory boards designed to the FLME (FORCE Local Memory Expansion) concept.

The SYS68K/DRAM-E3SX boards have 1, 3 or 6Mbyte of memory per FLME slave board available to extend the memory capacity of the master board.

The SYS68K/DRAM-E4SX boards have 4, 8 or 12Mbyte of memory per FLME slave board available to extend the memory capacity of the master board.

All of the DRAM-EXSX boards are able to transfer 8, 16, 24 or 32 bits of data. LEDs on the front panel show whether an access is pending or a parity error has been detected.

Figure 1-1 shows a photo of the SYS68K/DRAM-E4S12 board and Figure 1-2 shows a photo of the SYS68K/DRAM-E3S3 board.

Figure 1-1: Photo of the SYS68K/DRAM-E4S12

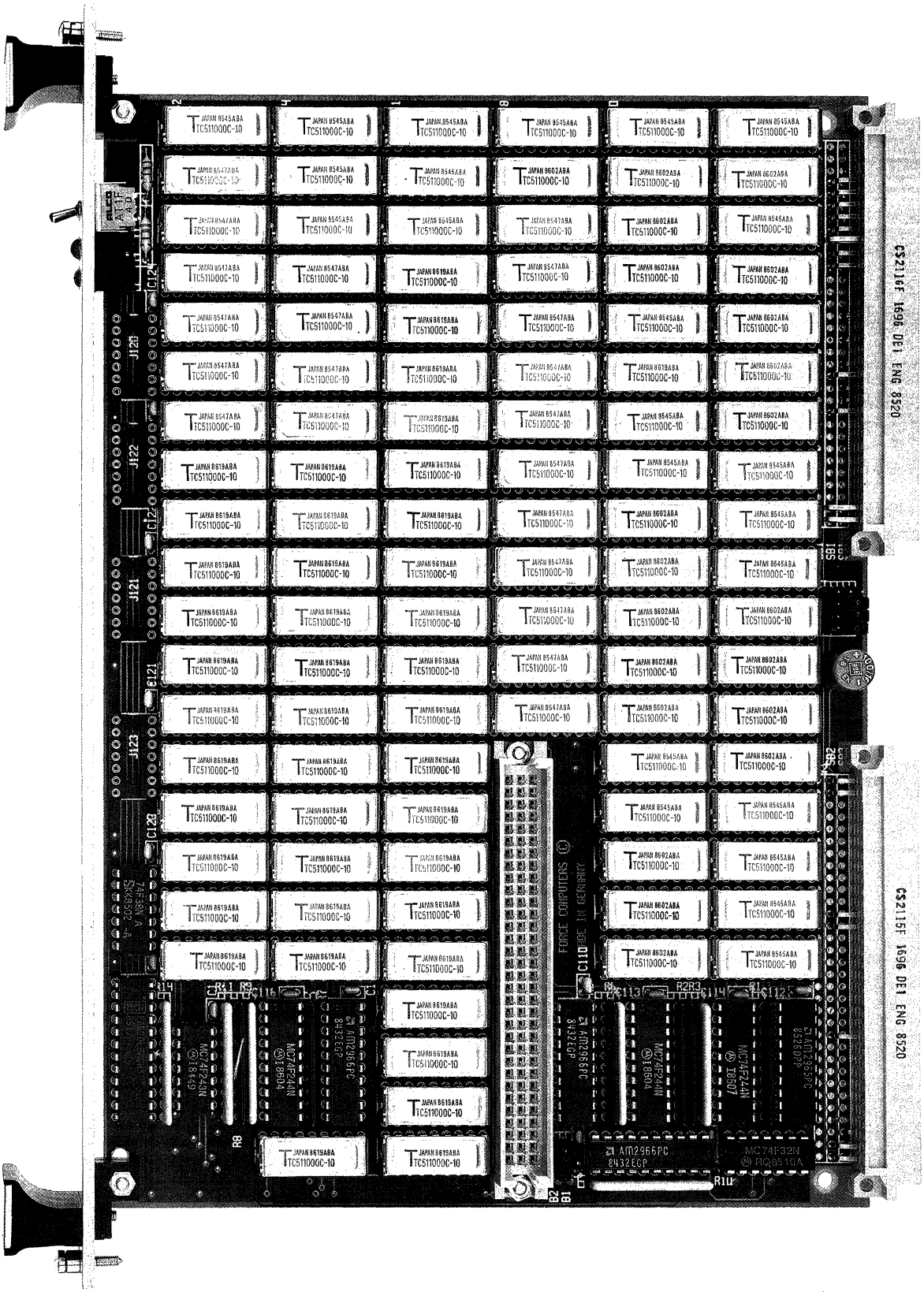
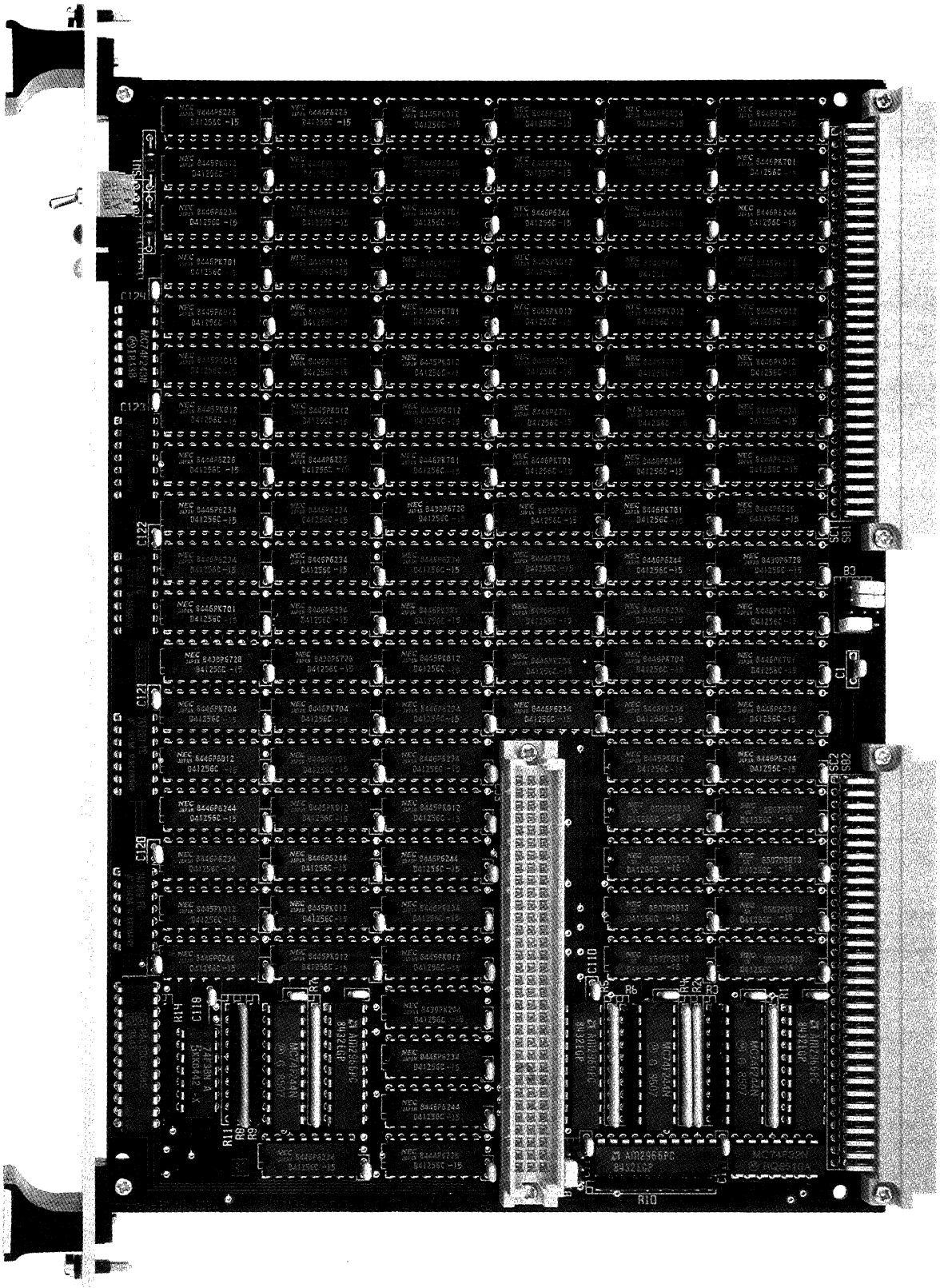


Figure 1-2: Photo of the SYS68K/DRAM-E3S3



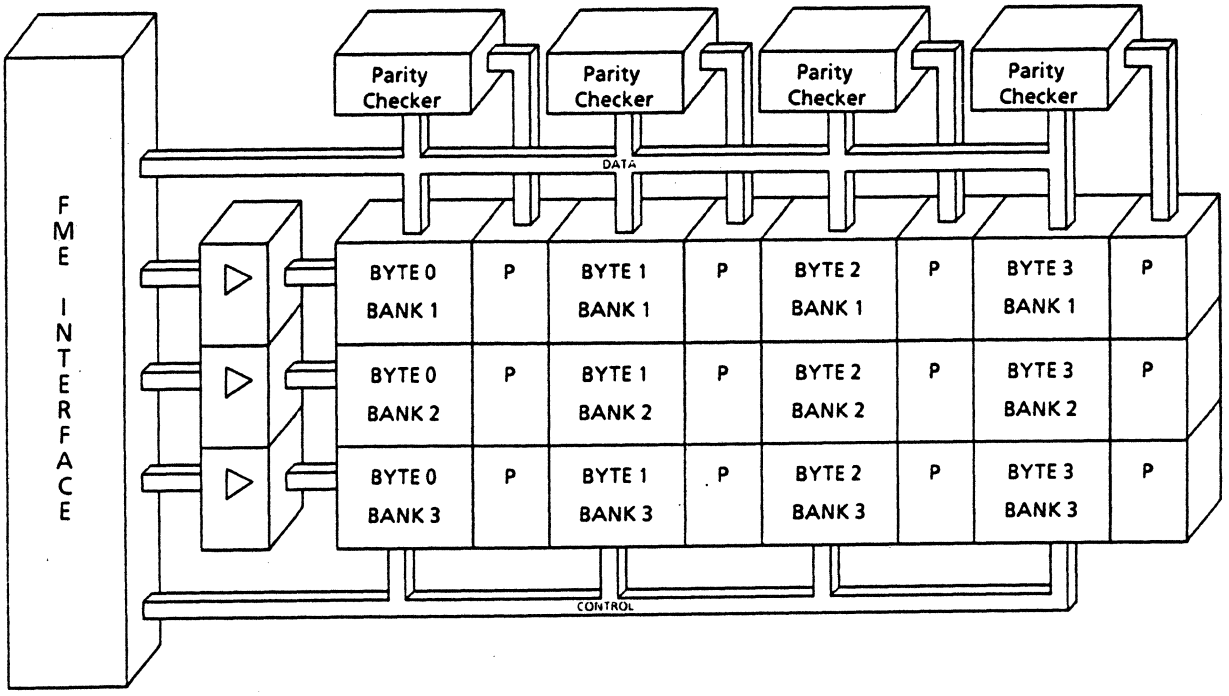
2.Ø General Operation

The DRAM-EXS series of boards contains all the necessary driver logic for the dynamic RAMs as well as the DRAM chips (36, 1Ø8 or 216pcs). This offers either 1, 3 or 6Mbyte of capacity (by using 256K by 1 oriented DRAM chips) or 4, 8 or 12Mbyte of capacity (by using 1Mbit by 1 oriented DRAM chips).

The board also contains sockets for circuitries to generate and detect parity errors.

A general block diagram of the DRAM-EXSX is shown in Figure 2-1, while Figure 2-2 shows the block diagram of the DRAM-E3S6.

Figure 2-1: Block Diagram of the SYS68K/DRAM-E4S12



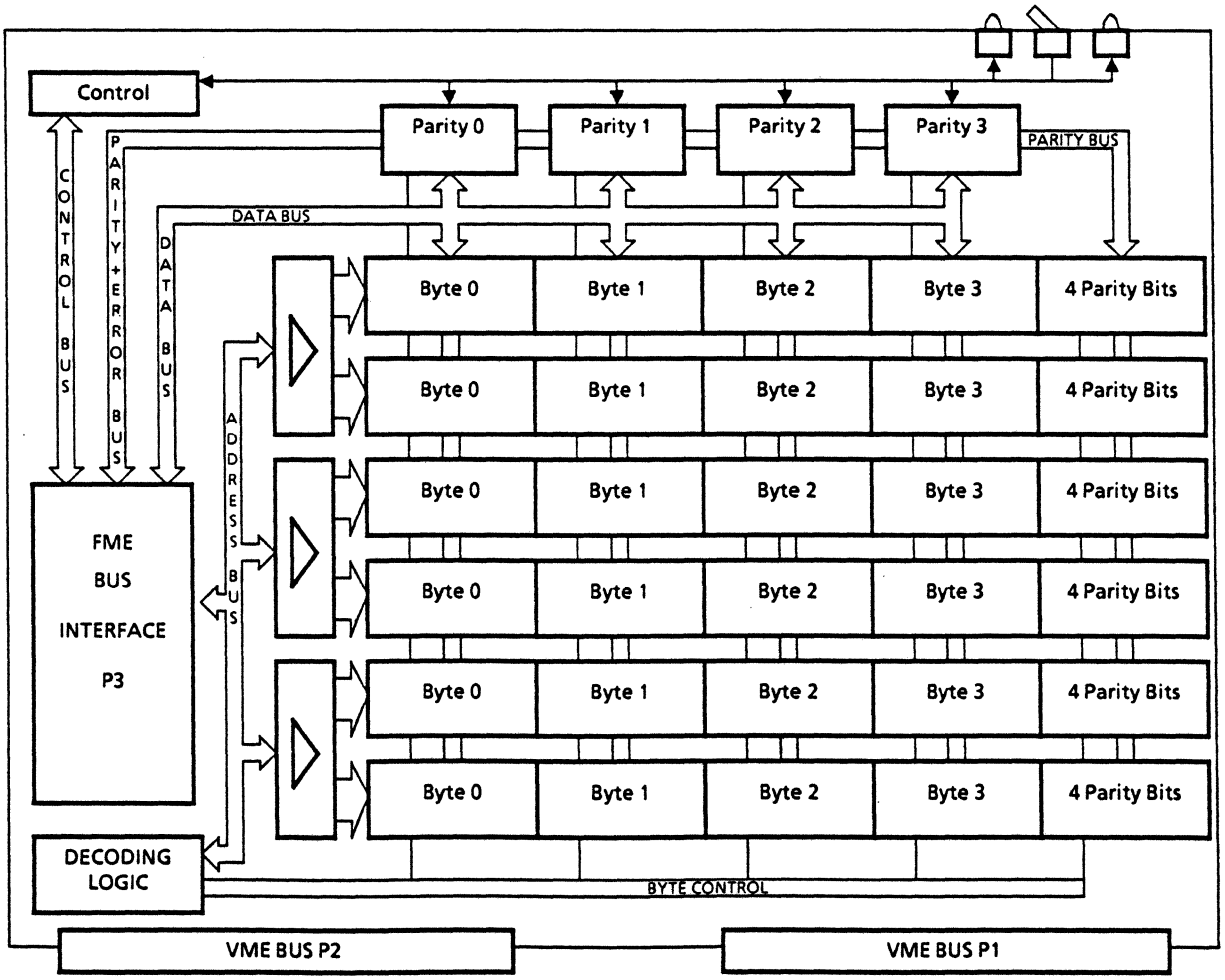
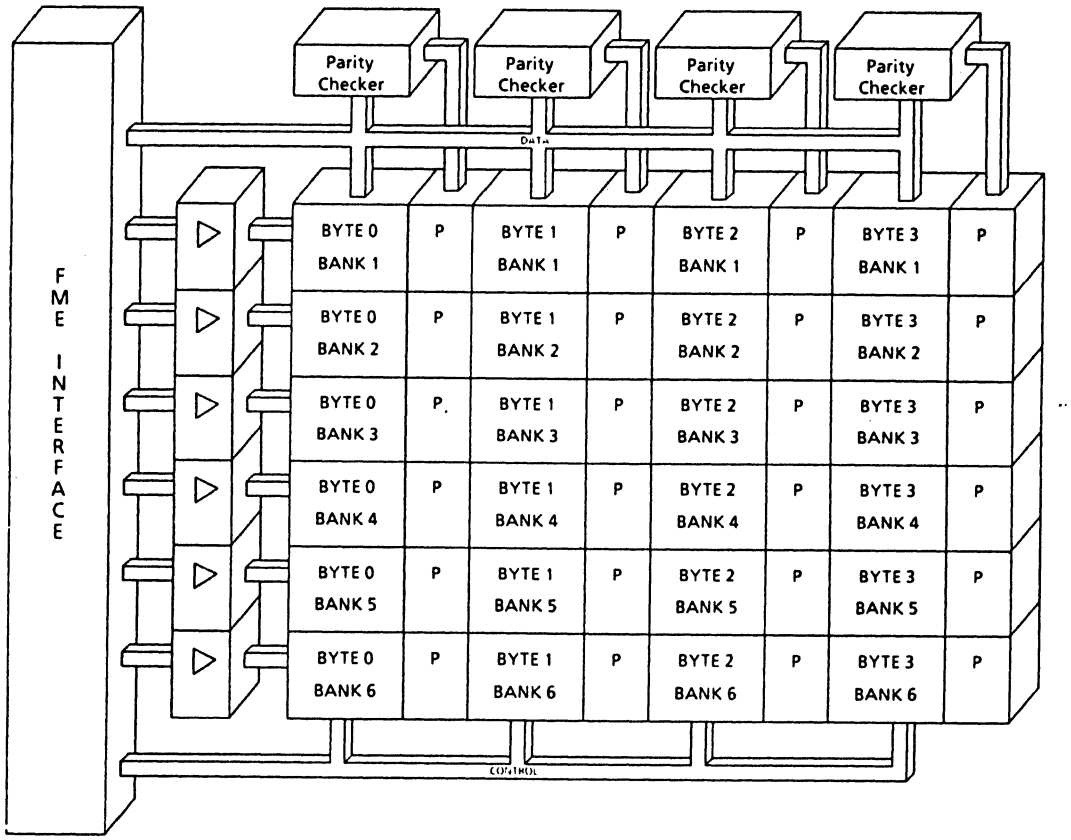


Figure 2-2: Block Diagram of the SYS68K/DRAM-E3S6



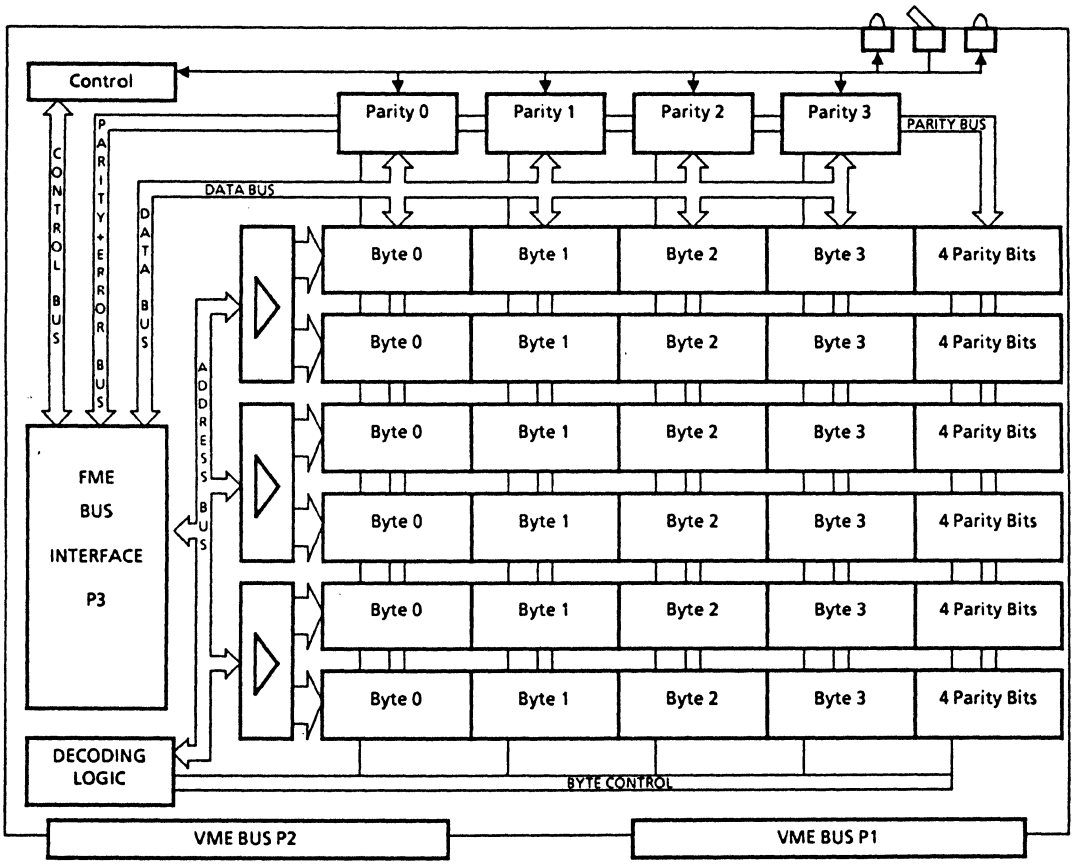
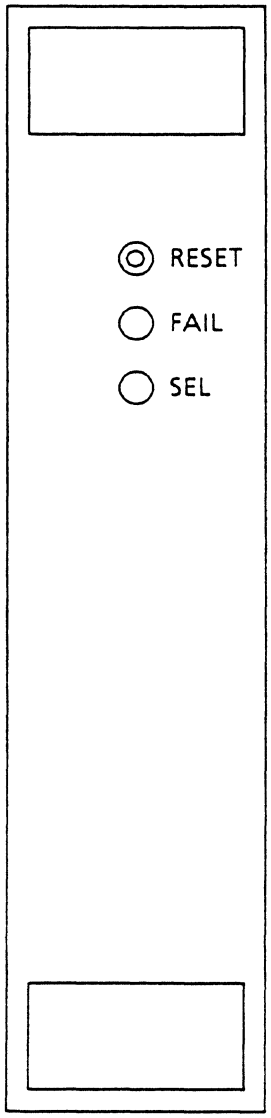


Figure 3-1: The Front Panel of the SYS68K/DRAM-E3SX



3.Ø Hardware Description

The address selection and the DRAM control logic are provided on the controller board for the DRAM-EXSX boards and only driver circuitries and DRAM chips are mounted on the boards.

The FLME interface for dynamic RAMs is designed to transfer data in groups of 8 bits (32 bit maximum) in parallel. Each byte is strobed separately to support 8, 16, 24 and 32 bit transfers at one time.

Table 3-1: Supported Data Transfer Types

	D24-D31	D16-D23	D15-D8	D7-DØ
Single Byte				x
			x	
		x		
	x			
Double Byte			x	x
		x	x	
	x	x		
		x		x
	x			x
	x		x	
Triple Byte		x	x	x
	x	x	x	
Quad Byte	x	x	x	x

The front panel of the DRAM-EXSX is shown in Figure 3-1.

The red FAIL LED turns on if the parity checker detects a parity error. This FAIL LED is held and shown until the board receives a RESET pulse or if the local RESET switch available on the front panel has been pushed.

The yellow SELect LED turns on if the board is selected during an access cycle of the controlling master board.

Figure 3-1 shows the front panel of the DRAM-EXSX boards in detail.

3.1 The CARD Select

A maximum of two FLME slave boards (DRAM-EXSX) boards are allowed in an FLME environment. Therefore, different jumper settings for each of the two cards are necessary for proper operation.

Tables 3-2 and 3-3 list the CARD select jumper settings for each card position and Figures 3-2 and 3-3 show the location diagram of the jumperfield in detail.

Table 3-2: CARD Select Jumperfield for DRAM-E3SX and DRAM-E4SX

	B2	B1
Jumper for Select Card 1	1 o | 2 o 3 o	1 o 2 o 3 o

	B2	B1
Jumper for Select Card 2	1 o 2 o 3 o	1 o | 2 o 3 o

Figure 3-2: Location Diagram of the CARD Select Jumperfield for DRAM-E3SX and DRAM-E4SX

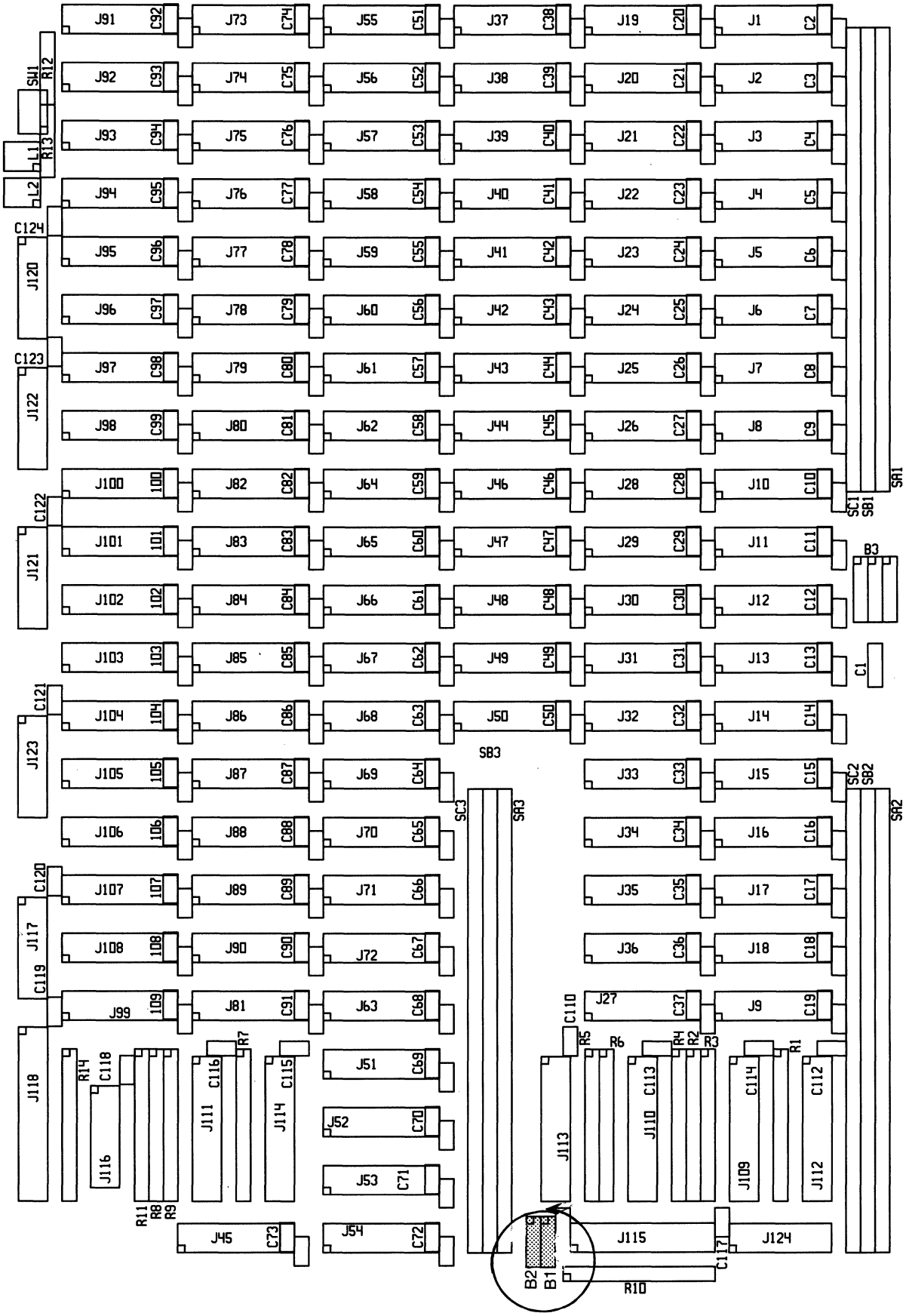
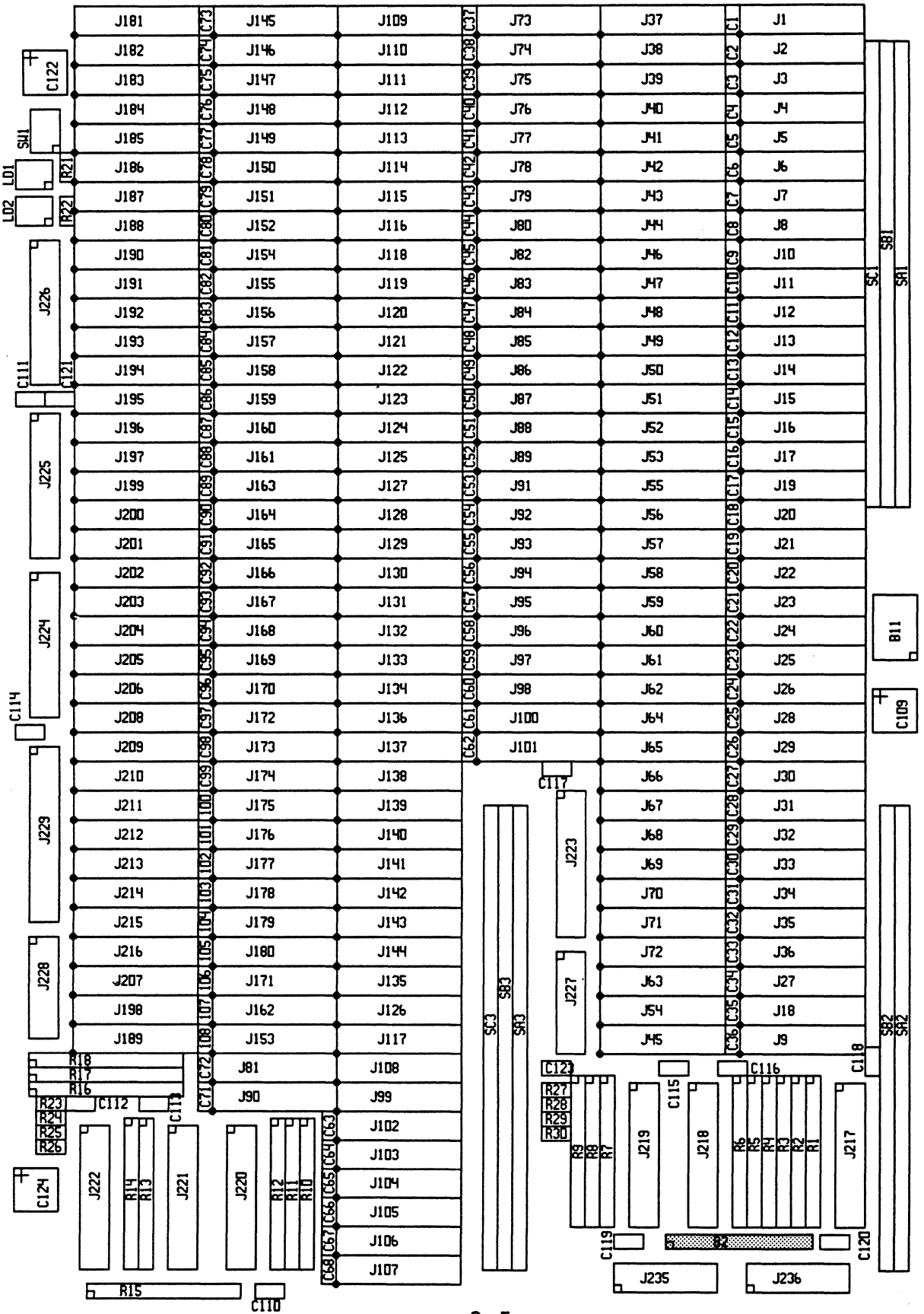


Table 3-3: CARD Select Jumperfield for the DRAM-E3S6

	B2
Jumper for Select Card 1	2 - 3 4 - 5 7 - 8

	B2
Jumper for Select Card 2	1 - 2 4 - 5 7 - 8

Figure 3-3: Location Diagram of the CARD Select Jumperfield for DRAM-E3S6



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CAUTION: Only fully populated boards can be mixed and connected to one master card. Tables 3-4 and 3-5 list the possible configurations.

Table 3-4: DRAM-E3SX Combinations

First Slave	Second Slave	Slave's Total Capacity
DRAM-E3S1	Not allowed	1Mbyte
DRAM-E3S3	Not allowed	3Mbyte
DRAM-E3S3	DRAM-E3S1	4Mbyte
DRAM-E3S3	DRAM-E3S3	6Mbyte
DRAM-E3S6	Not allowed	6Mbyte

To calculate the total memory capacity of an FLME sub-system, the capacity of the master board has to be added (i.e. 1Mbyte on the DRAM-E3M1 board).

Table 3-5: DRAM-E4SX Combinations

First Slave	Second Slave	Slave's Total Capacity
DRAM-E4S4	Not allowed	4Mbyte
DRAM-E4S8	Not allowed	8Mbyte
DRAM-E4S12	Not allowed	12Mbyte
DRAM-E4S12	DRAM-E4S4	16Mbyte
DRAM-E4S12	DRAM-E4S8	20Mbyte
DRAM-E4S12	DRAM-E4S12	24Mbyte

To calculate the total memory capacity of an FLME sub-system, the capacity of the master board has to be added (i.e. 4Mbyte on the DRAM-E4M4 board).

Warning: The simultaneous use of SYS68K/DRAM-E3MX and SYS68K/DRAM-E4SX boards is not allowed. Should this warning be ignored, then the RAM modules may be destroyed.

3.2 The Battery Backup Option

The DRAM-EXSX boards can be powered from the +5V main power or from the +5VBAT pins of the P2 connector (SA-30/31/32). The default condition during manufacturing is the connection to the +5V Main Power.

Table 3-6 lists the jumper settings which have to be made for the different modes, and Figure 3-4 outlines the location diagram of the jumperfields.

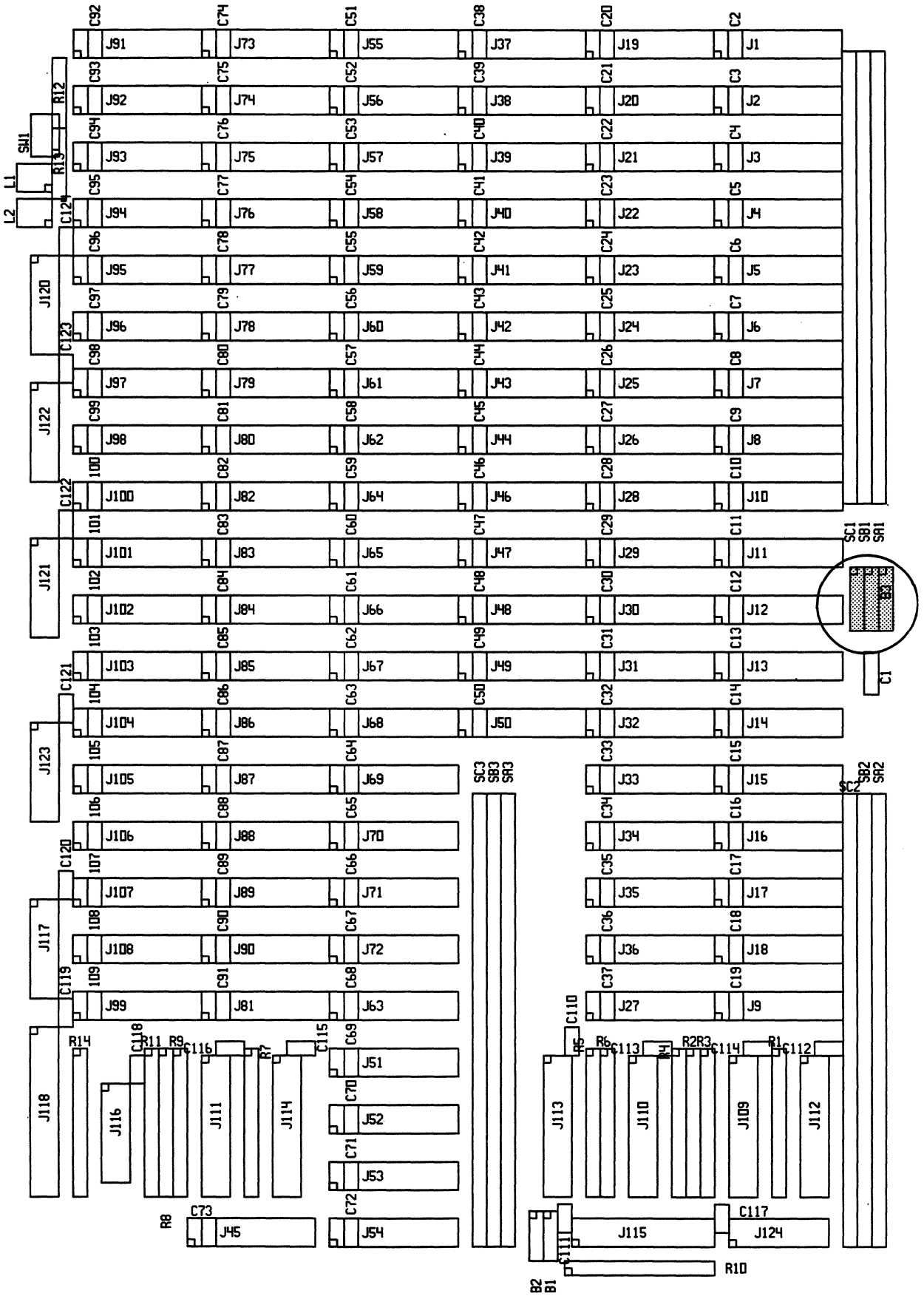
Table 3-6: The Battery Backup Option

	B3	
+5V STDBY (option)	o o o	
Battery Backup	o--o o o--o o o--o o	

	B3	
+5V STDBY (option)	o o--o	*
+5 MAIN	o o--o o o--o o o--o	* * *

* default condition during Manufacturing.

Figure 3-4: Location Diagram of the Battery Backup Jumperfields



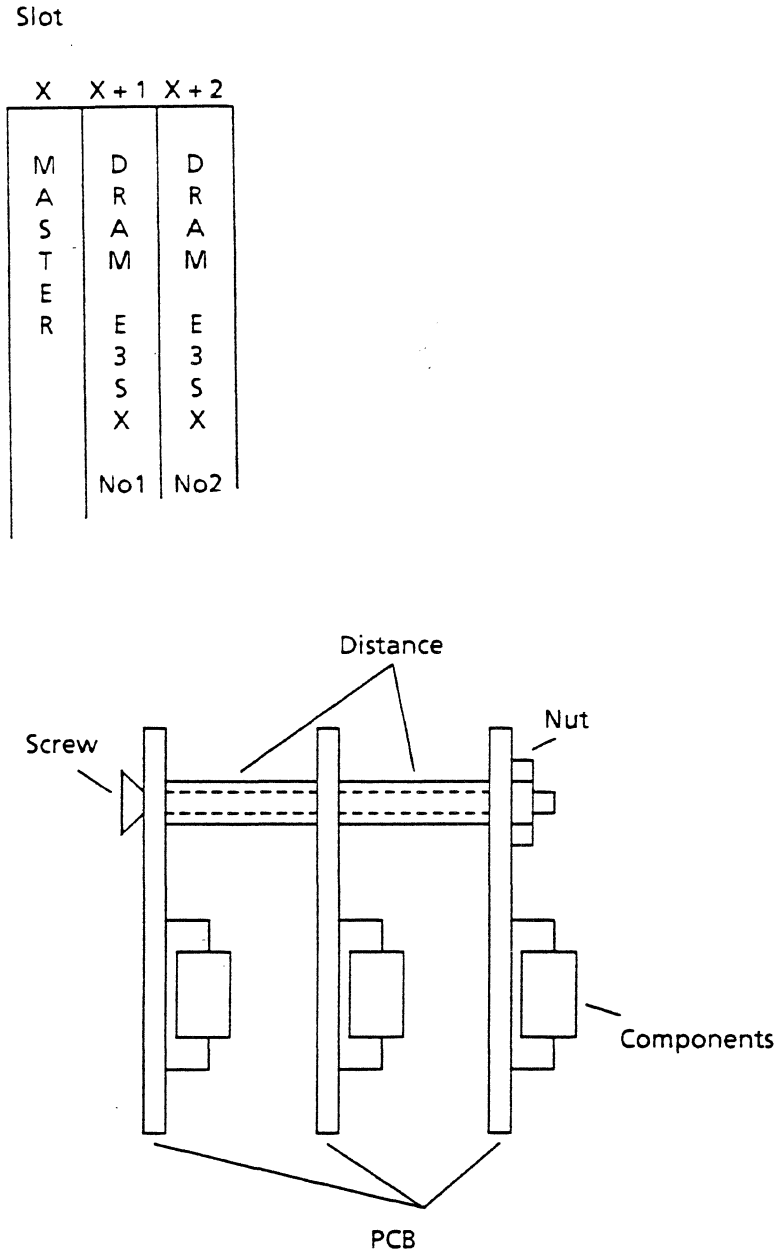
3.3 Board Interconnection

The DRAM-EXSX boards contain a 96 pin DIN connector (P3) in the middle of the board. All FLME control signals are included on this interface and only power is connected through P1 and P2 (VMEbus connectors). The master board contains the opposite connector and has to be connected before the boards are mounted into the VMEbus environment.

For easy distance generation, plastic distance spacers are included in the shipment.

The board installation of an FLME board is always as shown in Figure 3-5.

Figure 3-5: Interconnection of FLME Modules



APPENDIX TO THE HARDWARE USER'S MANUAL FOR DRAM-E3SX/E4SX

A P P E N D I C E S

Appendix A

Specification of the SYS68K/DRAM-E3SX Boards

	E3S1	E3S3	E3S6
Memory Capacity	1Mbyte	3Mbyte	6Mbyte
Organization	32+4 Bit	32+4 Bit	32+4 Bit
Data Transfer Mode any of 4 Bytes	Yes	Yes	Yes
Used DRAM Chip Organisation	256K x 1	256K x 1	256K x 1
DRAM Chips	36pcs	108pcs	216pcs
RAS DRAM Access Time	120ns	120ns	120ns
Bus Interface	FLME (slave)	FLME (slave)	FLME (slave)
Access Times Write	70	70	70
Read without Parity Check	210	210	210
Read with Parity Check	260	260	260
Power Requirements			
+5V (Refresh Peak)	3.3A	3.5A	5.0A
+5V (Average Max)	2.7A	3.0A	4.8A
+5V (Average Typ)	2.5A	2.8A	4.6A
Operating Temperature (deg C)	0 to +60	0 to +60	0 to +60
Storage Temperature (deg C)	-55 to +85	-55 to +85	-55 to +85
Relative Humidity (non-condensing)	0-95%	0-95%	0-95%
Double Eurocard 233 x 160mm (9.2 x 6.3")	Yes	Yes	Yes

Appendix A

Specification of the SYS68K/DRAM-E4SX Boards

	E4S4	E4S8	E4S12
Memory Capacity	4Mbyte	8Mbyte	12Mbyte
Organization	32+4 Bit	32+4 Bit	32+4 Bit
Data Transfer Mode any of 4 Bytes	Yes	Yes	Yes
Used DRAM Chip Organisation	1Mbit x 1	1Mbit x 1	1Mbit x 1
DRAM Chips	36pcs	72pcs	108pcs
RAS DRAM Access Time	120ns	120ns	120ns
Bus Interface	FLME (slave)	FLME (slave)	FLME (slave)
Access Times Write	70	70	70
Read without Parity Check	210	210	210
Read with Parity Check	260	260	260
Power Requirements			
+5V (Refresh Peak)	3.3A	3.5A	3.8A
+5V (Average Max)	2.7A	3.0A	3.3A
+5V (Average Typ)	2.5A	2.8A	3.1A
Operating Temperature (deg C)	0 to +60	0 to +60	0 to +60
Storage Temperature (deg C)	-55 to +85	-55 to +85	-55 to +85
Relative Humidity (non-condensing)	0-95%	0-95%	0-95%
Double Eurocard 233 x 160mm (9.2 x 6.3")	Yes	Yes	Yes

Appendix B

BB Rev. 1
PRN 100
Date 10/10/86

Component Part List SYS68K/DRAM-E3S1 and DRAM-E3S3

ICs

Location	Type	Manufacturer
J1 to J36 J37 to J108 *	RAMs 256Kbit 120ns	Toshiba TMK41256P-12 NEC uPD41256C-12 Hitachi Mitsubishi
J109	74F244	MOT, F, VALVO
J110	74F244	MOT, F, VALVO
J111	74F244	MOT, F, VALVO
J112	2966	AMD
J113	2966	AMD
J114	2966	AMD
J115	2966	AMD
J116	74F243	MOT, F, VALVO
J117	74F38	MOT, F, VALVO
J118	FRC 30	FORCE - PAL 20L8B
J120	--	
J121	--	
J122	--	
J123	--	
J124	74F32	MOT, F, VALVO

* ONLY ON THE DRAM-E3S3

Appendix B

BB Rev. 1
PRN 100
Date 10/10/86

Component Part List SYS68K/DRAM-E3S1 and DRAM-E3S3

RESISTORS

Location	Type	Manufacturer
R1	5 * 33	VARIOUS
R2	5 * 47	VARIOUS
R3	9 * 4.7K	VARIOUS
R4	5 * 33	VARIOUS
R5	5 * 47	VARIOUS
R6	9 * 4.7K	VARIOUS
R7	5 * 33	VARIOUS
R8	5 * 47	VARIOUS
R9	9 * 4.7K	VARIOUS
R10	9 * 4.7K	VARIOUS
R11	9 * 4.7K	VARIOUS
R12	1 * 150	VARIOUS
R13	1 * 29	VARIOUS
R14	9 * 680	VARIOUS

A p p e n d i x B

BB Rev. 1
PRN 100
Date 10/10/86

Component Part List SYS68K/DRAM-E3S1 and DRAM-E3S3

CAPACITORS

Location	Type	Manufacturer
C1	100uF/10V ELKO RM 5.08mm	VARIOUS
C2 - C124	10nF	VARIOUS

LEDs

Location	Type	Manufacturer
LD1	2406	DIALIGHT (RED)
LD2	2306	DIALIGHT (YELLOW)

Appendix B

BB Rev. 1
PRN 100
Date 10/10/86

Component Part List SYS68K/DRAM-E3S1 and DRAM-E3S3

MECHANICAL PARTS

Location	Type	Manufacturer
J118	SOCKET 24 PIN	VARIOUS
SW1	SWITCH	KNITTER
B1, B2	DW6	VARIOUS
B3	TW12	VARIOUS
P1	FORCE 983039	VARIOUS
P2	FORCE 983038	VARIOUS
P3	FORCE 983040 + FORCE 983041	VARIOUS
DRAM-E3FP	FRONT PANEL	FORCE
DRAM-E3SD	PCB	FORCE
	Jumpers-A	Jumpers for Headers (5)

A p p e n d i x B

BB Rev. 1
PRN 100
Date 10/10/86

Component Part List SYS68K/DRAM-E3S1 and DRAM-E3S3

	ATTACHED PARTS	
1)	SYS68K/DRAM-EXXX/HUM	HARDWARE USER'S MANUAL
2)	PRODUCT RELEASE NOTE	

Appendix C

BB Rev. Ø
PRN 1ØØ
Date 1Ø/1Ø/86

Component Part List SYS68K/DRAM-E3S6

ICs

Location	Type	Manufacturer
J1 to J216	RAMs Zick-Zack 256Kbit 12Øns	MITSU - M5M4256L-12 NEC
J217	74F244	MOT, FAIR, VALVO
J218	74F244	MOT, FAIR, VALVO
J219	74F244	MOT, FAIR, VALVO
J22Ø	74F244	MOT, FAIR, VALVO
J221	74F244	MOT, FAIR, VALVO
J222	74F244	MOT, FAIR, VALVO
J223	AM2966	AMD
J224	AM2966	AMD
J225	AM2966	AMD
J226	AM2966	AMD
J227	74F243	MOT, FAIR, VALVO
J228	74F38	MOT, FAIR, VALVO
J229	FRC	PAL 2ØL8B
J235	74F32	MOT, FAIR, VALVO
J236	74F32	MOT, FAIR, VALVO

Appendix C

BB Rev. Ø
PRN 1ØØ
Date 1Ø/1Ø/86

Component Part List SYS68K/DRAM-E3S6

RESISTORS

Location	Type	Manufacturer
R1	9 * 4.7K	VARIOUS
R2	5 * 33	VARIOUS
R3	5 * 33	VARIOUS
R4	9 * 4.7K	VARIOUS
R5	5 * 33	VARIOUS
R6	5 * 33	VARIOUS
R7	9 * 4.7K	VARIOUS
R8	5 * 33	VARIOUS
R9	5 * 33	VARIOUS
R1Ø	9 * 4.7K	VARIOUS
R11	5 * 33	VARIOUS
R12	5 * 33	VARIOUS
R13	9 * 4.7K	VARIOUS
R14	5 * 33	VARIOUS
R15	5 * 33	VARIOUS
R16	9 * 4.7K	VARIOUS
R17	5 * 33	VARIOUS
R18	5 * 33	VARIOUS

Appendix C

BB Rev. 0
PRN 100
Date 10/10/86

Component Part List SYS68K/DRAM-E3S6

RESISTORS

Location	Type	Manufacturer
R21	150 RGU	VARIOUS
R22	22 RGU	VARIOUS
R23	680 RGU	VARIOUS
R24	680 RGU	VARIOUS
R25	680 RGU	VARIOUS
R26	680 RGU	VARIOUS
R27	4.7K RGU	VARIOUS
R28	4.7K RGU	VARIOUS
R29	4.7K RGU	VARIOUS
R30	4.7K RGU	VARIOUS

A p p e n d i x C

BB Rev. Ø
PRN 1ØØ
Date 1Ø/1Ø/86

Component Part List SYS68K/DRAM-E3S6

CAPACITORS

Location	Type	Manufacturer
12Ø PC5	1ØØnF	VARIOUS
C1Ø9	1ØØuF/1ØV ELKO RM 5.Ø8mm	VARIOUS
C122	1ØØuF/1ØV ELKO RM 5.Ø8mm	VARIOUS
C124	1ØØuF/1ØV ELKO RM 5.Ø8mm	VARIOUS

LEDs

Location	Type	Manufacturer
LD1	24Ø6	DIALIGHT (RED)
LD2	23Ø6	DIALIGHT (YELLOW)

Appendix C

BB Rev. Ø
PRN 1ØØ
Date 1Ø/1Ø/86

Component Part List SYS68K/DRAM-E3S6

MECHANICAL PARTS

Location	Type	Manufacturer
J229	SOCKET 24 PIN	VARIOUS
SW1	SWITCH	KNITTER
B2	EW9	VARIOUS
B3	TW12	VARIOUS
P1	FORCE 983Ø39	VARIOUS
P2	FORCE 983Ø38	VARIOUS
P3	FORCE 983Ø4Ø + FORCE 983Ø41	VARIOUS
DRAM-E3FP	FRONT PANEL	FORCE
DRAM-E3S6	PCB	FORCE
	Jumpers-A	Jumpers for Headers (5)

Appendix C

BB Rev. Ø
PRN 1ØØ
Date 1Ø/1Ø/86

Component Part List SYS68K/DRAM-E3S6

	ATTACHED PARTS	
1)	SYS68K/DRAM-EXXX/HUM	HARDWARE USER'S MANUAL
2)	PRODUCT RELEASE NOTE	

A p p e n d i x D

BB Rev. Ø
PRN ØØ1
Date 1Ø/1Ø/86

Component Part List SYS68K/DRAM-E4S1 and DRAM-E4S12

ICs

Location	Type	Manufacturer
J1 to J36 J37 to J1Ø8 *	RAMs 1Mbit 12Ønsec	Toshiba TC511ØØØC-12 NEC uPD411ØØØC-12 HIT
J1Ø9	74F244	MOT, F, SIGN
J11Ø	74F244	MOT, F, SIGN
J111	74F244	MOT, F, SIGN
J112	2966	AMD
J113	2966	AMD
J114	2966	AMD
J115	2966	AMD
J116	74F243	MOT, F, SIGN
J117	74F38	
J118	FRC 3Ø	FORCE - PAL 2ØL8B (MMI)
J12Ø	--	
J121	--	
J122	--	
J123	--	
J124	74F32	MOT, F, SIGN

* only on the DRAM-E4S12

A p p e n d i x D

BB Rev. Ø
PRN ØØ1
Date 1Ø/1Ø/86

Component Part List SYS68K/DRAM-E4S1 and DRAM-E4S12

RESISTORS

Location	Type	Manufacturer
R1	5 * 33	VARIOUS
R2	5 * 47	VARIOUS
R3	9 * 4.7K	VARIOUS
R4	5 * 33	VARIOUS
R5	5 * 47	VARIOUS
R6	9 * 4.7K	VARIOUS
R7	5 * 33	VARIOUS
R8	5 * 47	VARIOUS
R9	9 * 4.7K	VARIOUS
R1Ø	9 * 4.7K	VARIOUS
R11	9 * 4.7K	VARIOUS
R12	15Ø	VARIOUS
R13	27	VARIOUS
R14	9 * 68Ø	VARIOUS

A p p e n d i x D

BB Rev. Ø
PRN ØØ1
Date 1Ø/1Ø/86

Component Part List SYS68K/DRAM-E4S1 and DRAM-E4S12

CAPACITORS

Location	Type	Manufacturer
C1	1ØØuF/1ØV ELKO RM 5.8mm	VARIOUS
C2 - C124	1ØØnF	VARIOUS

LEDs

Location	Type	Manufacturer
LD1	24Ø6	DIALIGHT (RED)
LD2	23Ø6	DIALIGHT (YELLOW)

Appendix D

BB Rev. 0
PRN 001
Date 10/10/86

Component Part List SYS68K/DRAM-E4S1 and DRAM-E4S12

MECHANICAL PARTS

Location	Type	Manufacturer
SW1	AT - 1F	KNITTER
B1 + B2	DW6	VARIOUS
B3	TW12	VARIOUS
P1	FORCE 983039	VARIOUS
P2	FORCE 983038	VARIOUS
P3	FORCE 983040 + FORCE 983041	VARIOUS
DRAM-E4FP	FRONT PANEL	FORCE
DRAM-E4SD	PCB	FORCE
	2 SPACER RINGS	VARIOUS
	2 SCREWS M3X	VARIOUS
	2 NUTS M3	VARIOUS
	2 SCREWS M3X	VARIOUS
J1 to J36	SOCKET 18 PIN	VARIOUS
J37 to J108*	SOCKET 18 PIN	VARIOUS
J118	SOCKET 24 PIN	VARIOUS
	Jumpers-A	Jumpers for Headers (5)

* only on the DRAM-E4S12

Appendix D

BB Rev. Ø
PRN ØØ1
Date 1Ø/1Ø/86

Component Part List SYS68K/DRAM-E4S1 and DRAM-E4S12

	ATTACHED PARTS	
1)	SYS68K/DRAM-EXXX/HUM	HARDWARE USER'S MANUAL
2)	PRODUCT RELEASE NOTE	

Appendix E

Description of the Jumperfields

Jumper-field	Description	Default Condition	Schematics	Location Coord. x y	See Page
B1	Block-Select	1 - 2	5 - C1	54/3	
B2	Card-Select	2 - 3			

Jumper-field	Description	Default Condition	Schematics	Location Coord. x y	See Page
B3	Battery Backup Option	b a 1 - 1 2 - 2 3 - 3 4 - 4	4 - B3	4/100	

Appendix E

Location Diagram of the Jumperfields B1, B2 and B3

Appendix F

Circuit Schematics for the SYS68K/DRAM-E3S1, E3S3, E4SX

Appendix G

Circuit Schematics of the SYS68K/DRAM-E3S6

Appendix H

P1 Pin Assignments to VMEbus

PIN Number	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	-	-	-
2	-	-	-
3	-	-	-
4	-	BG0IN* (1)	-
5	-	BG0OUT* (1)	-
6	-	BG1IN* (1)	-
7	-	BG1OUT* (1)	-
8	-	BG2IN* (1)	-
9	GND	BG2OUT* (1)	GND
10	-	BG3IN* (1)	-
11	GND	BG3OUT* (1)	-
12	-	-	-
13	-	-	-
14	-	-	-
15	GND	-	-
16	-	-	-
17	GND	-	-
18	-	-	-
19	GND	-	-
20	-	GND	-
21	IACKIN* (1)	-	-
22	IACKOUT* (1)	-	-
23	-	GND	-
24	-	-	-
25	-	-	-
26	-	-	-
27	-	-	-
28	-	-	-
29	-	-	-
30	-	-	-
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

Note (1): IN to OUT Connected

Appendix H

P2 Pin Assignments to VMEbus

PIN Number	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	-	+5V Volts	-
2	-	GND	-
3	-	RESERVED	-
4	-	-	-
5	-	-	-
6	-	-	-
7	-	-	-
8	-	-	-
9	-	-	-
10	-	-	-
11	-	-	-
12	-	GND	-
13	-	+5 Volts	-
14	-	-	-
15	-	-	-
16	-	-	-
17	-	-	-
18	-	-	-
19	-	-	-
20	-	-	-
21	-	-	-
22	-	GND	-
23	-	-	-
24	-	-	-
25	-	-	-
26	-	-	-
27	-	-	-
28	-	-	-
29	-	-	-
30	User I/O (1)	-	-
31	User I/O(1)	GND	-
32	User I/O	+5 Volts	-

Note (1): User I/O for standby power connection.

Appendix H

P3 Pin Assignment to FLME Interface

Component Side

PIN NUMBER	ROW C SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW A SIGNAL MNEMONIC
1	Byte 1/7	Byte 2/7	Byte 3/7
2	Byte 1/6	Byte 2/6	Byte 3/6
3	Byte 1/5	Byte 2/5	Byte 3/5
4	Byte 1/4	Byte 2/4	Byte 3/4
5	Byte 1/3	Byte 2/3	Byte 3/3
6	Byte 1/2	Byte 2/2	Byte 3/2
7	Byte 1/1	Byte 2/1	Byte 3/1
8	Byte 1/Ø	Byte 2/Ø	Byte 3/Ø
9	Error 4	Byte 4/7	Address 2
1Ø	Error 3	Byte 4/6	Address 1
11	Error 2	Byte 4/5	EFDTACK*
12	Error 1	Byte 4/4	FDTACK*
13	Parity 4	Byte 4/3	WR 4
14	Parity 3	Byte 4/2	WR 3
15	Parity 2	Byte 4/1	WR 2
16	Parity 1	Byte 4/Ø	WR 1
17	+5V BATT.	+5V-	Address 3
18	+5V BATT.	+5V |-BATT.	Address 4
19	Reserved	+5V |	Address 5
2Ø	ØV	+5V-	Address 6
21	ØV	Reserved	Address 7
22	ØV	ØV	Address 8
23	Address 11	ØV	Address 9
24	Address 12	ØV	Address 1Ø
25	Address 13	RAS 1	LWBL 3
26	Address 14	RAS 2	LWBL 2
27	Address 15	RAS 3	LWBL 1
28	Address 16	RAS 4	Card 1(Block 1)
29	Address 17	CAS 1	Card 2(Block 2)
3Ø	Address 18	CAS 2	Card 3(Slave 2)
31	Address 19	CAS 3	Card 4(Slave 1)
32	Address 2Ø	CAS 4	FAIL

Appendix H

P3 Pin Assignments to FLME Interface

Backside

PIN NUMBER	ROW A SIGNAL MNEMONIC	ROW B SIGNAL MNEMONIC	ROW C SIGNAL MNEMONIC
1	Byte 3/7	Byte 2/7	Byte 1/7
2	Byte 3/6	Byte 2/6	Byte 1/6
3	Byte 3/5	Byte 2/5	Byte 1/5
4	Byte 3/4	Byte 2/4	Byte 1/4
5	Byte 3/3	Byte 2/3	Byte 1/3
6	Byte 3/2	Byte 2/2	Byte 1/2
7	Byte 3/1	Byte 2/1	Byte 1/1
8	Byte 3/Ø	Byte 2/Ø	Byte 1/Ø
9	Address 2	Byte 4/7	Error 4
1Ø	Address 1	Byte 4/6	Error 3
11	EFDTACK*	Byte 4/5	Error 2
12	FDTACK*	Byte 4/4	Error 1
13	WR 4	Byte 4/3	Parity 4
14	WR 3	Byte 4/2	Parity 3
15	WR 2	Byte 4/1	Parity 2
16	WR 1	Byte 4/Ø	Parity 1
17	Address 3	+5V-	+5V BATT.
18	Address 4	+5V |-BATT.	+5V BATT.
19	Address 5	+5V |	Reserved
2Ø	Address 6	+5V-	ØV
21	Address 7	Reserved	ØV
22	Address 8	ØV	ØV
23	Address 9	ØV	Address 11
24	Address 1Ø	ØV	Address 12
25	LWBL 3	RAS 1	Address 13
26	LWBL 2	RAS 2	Address 14
27	LWBL 1	RAS 3	Address 15
28	Card 1(Block 1)	RAS 4	Address 16
29	Card 2(Block 2)	CAS 1	Address 17
3Ø	Card 3(Slave 2)	CAS 2	Address 18
31	Card 4(Slave 1)	CAS 3	Address 19
32	FAIL	CAS 4	Address 2Ø

Appendix I

Product Error Report

DEAR CUSTOMER,

WHILE FORCE COMPUTERS HAS ACHIEVED A VERY HIGH STANDARD OF QUALITY IN OUR PRODUCTS AND DOCUMENTATION, WE CONTINUALLY SEEK SUGGESTIONS FOR IMPROVEMENTS.

WE WOULD APPRECIATE ANY FEEDBACK YOU CARE TO OFFER.

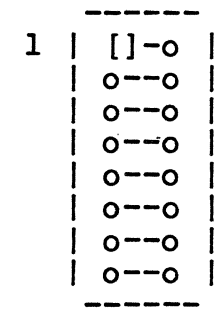
PLEASE USE ATTACHED "PRODUCT ERROR REPORT" FORM FOR YOUR COMMENTS AND RETURN IT TO ONE OF OUR FORCE COMPUTERS OFFICES.

FORCE Computers

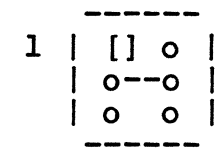
THE DEFAULT JUMPER SETTINGS

Default Jumper Settings on the Master Board

B2 Address Modifier Code Selection

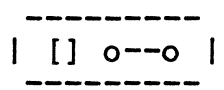


B14 Read Access Time

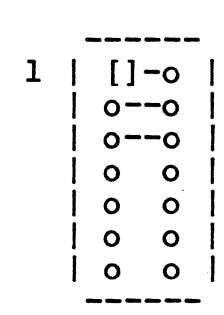


B20 Parity Error to BERR

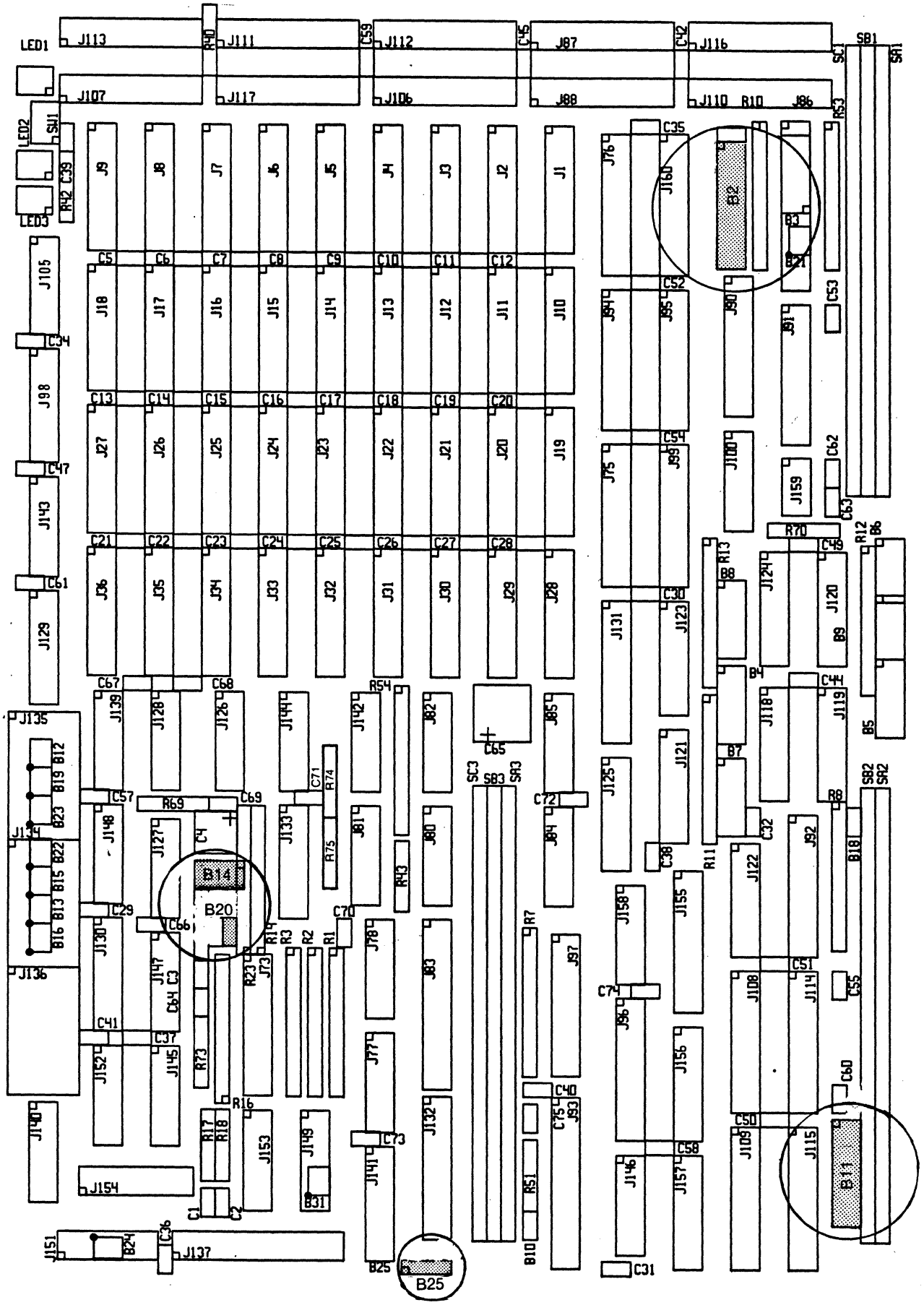
B25 Start AS/DS



B11 Battery Backup Option



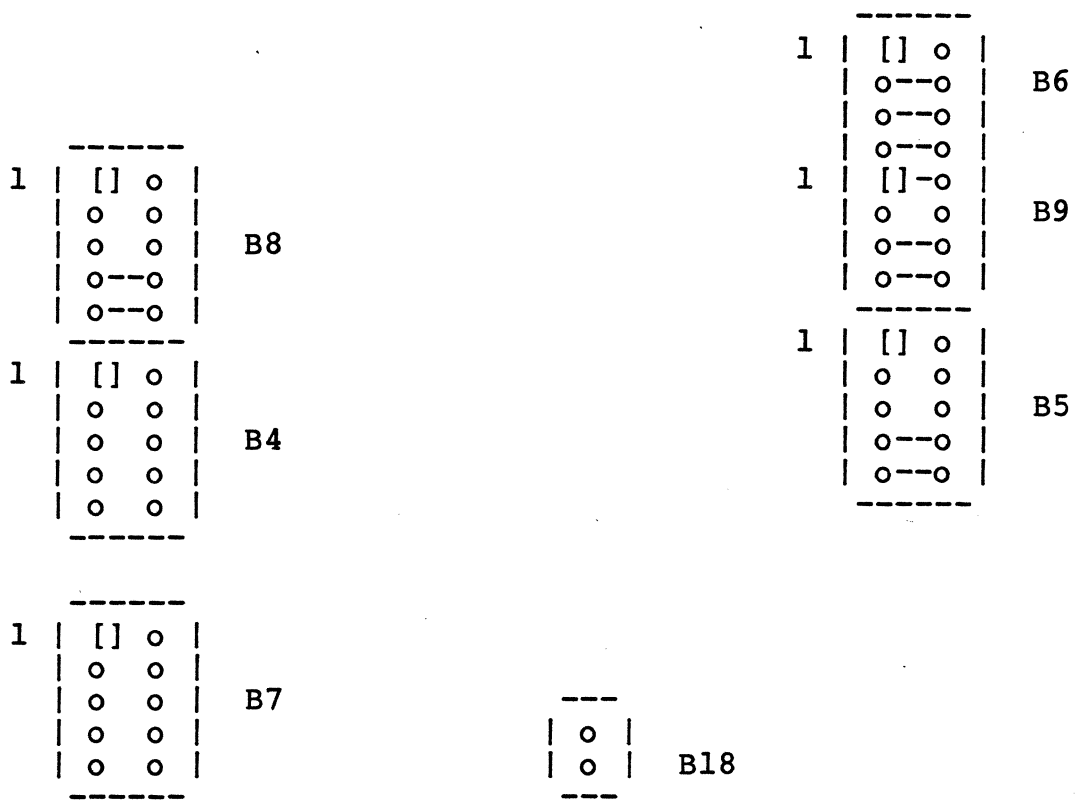
Jumper Location Diagram



Default Jumper Settings on the Master Board

Access Address Selection

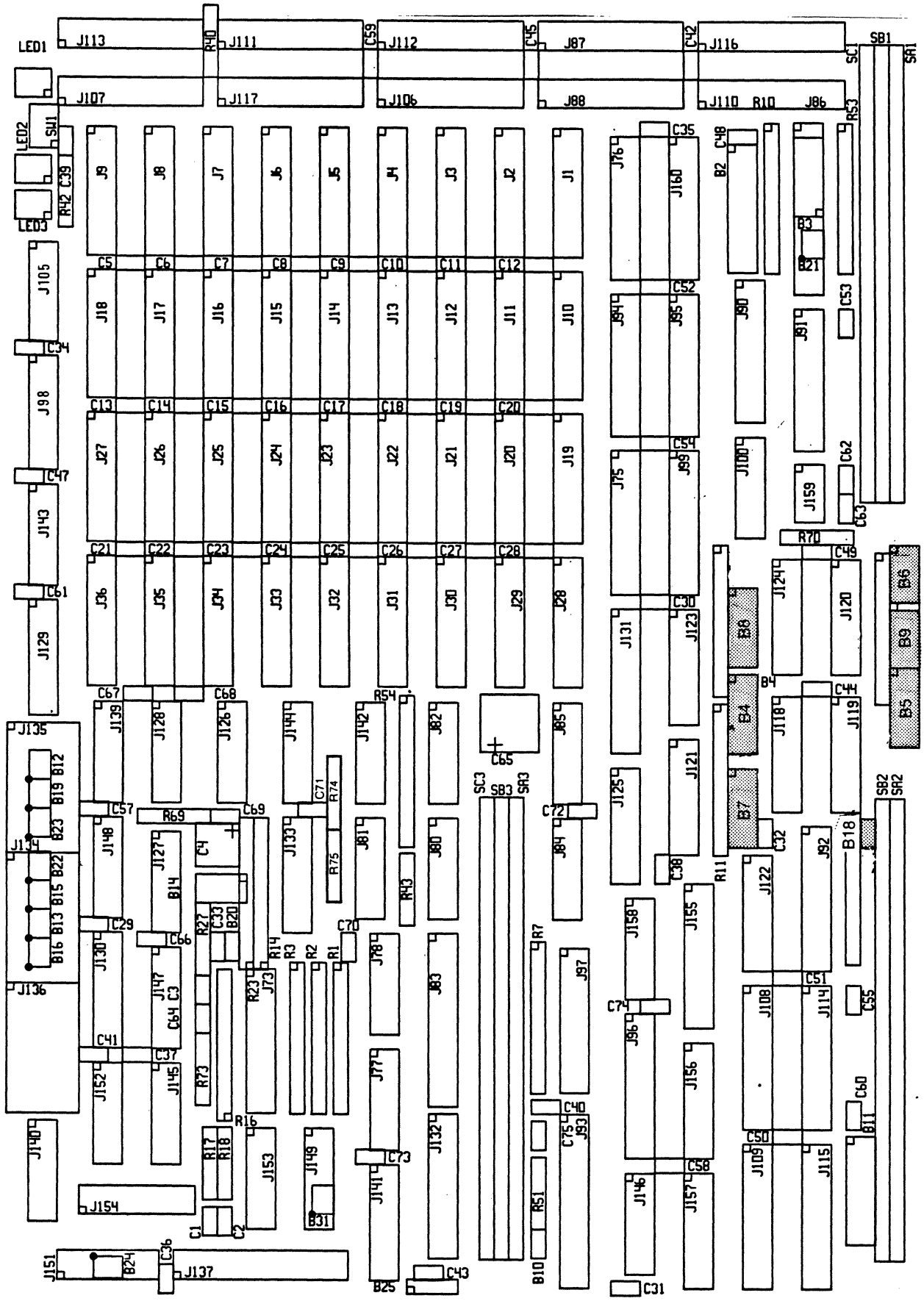
Mode: A24



Start Address : Jumper B7, B8, B9
End Address : Jumper B4, B5, B6
Address Mode : Jumper B18

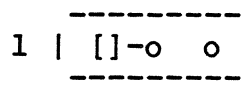
	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FF1F FFFF	$1F FFFF
First Not On-board Address:	$FF20 0000	$20 0000
Boundary:	$ 10 0000	$10 0000
		1Mbyte

Jumper Location Diagram

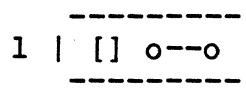


Default Jumper Settings on Slave Board

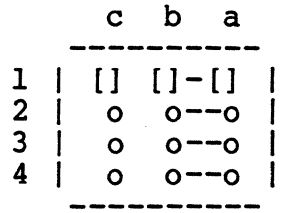
B1 Block Select



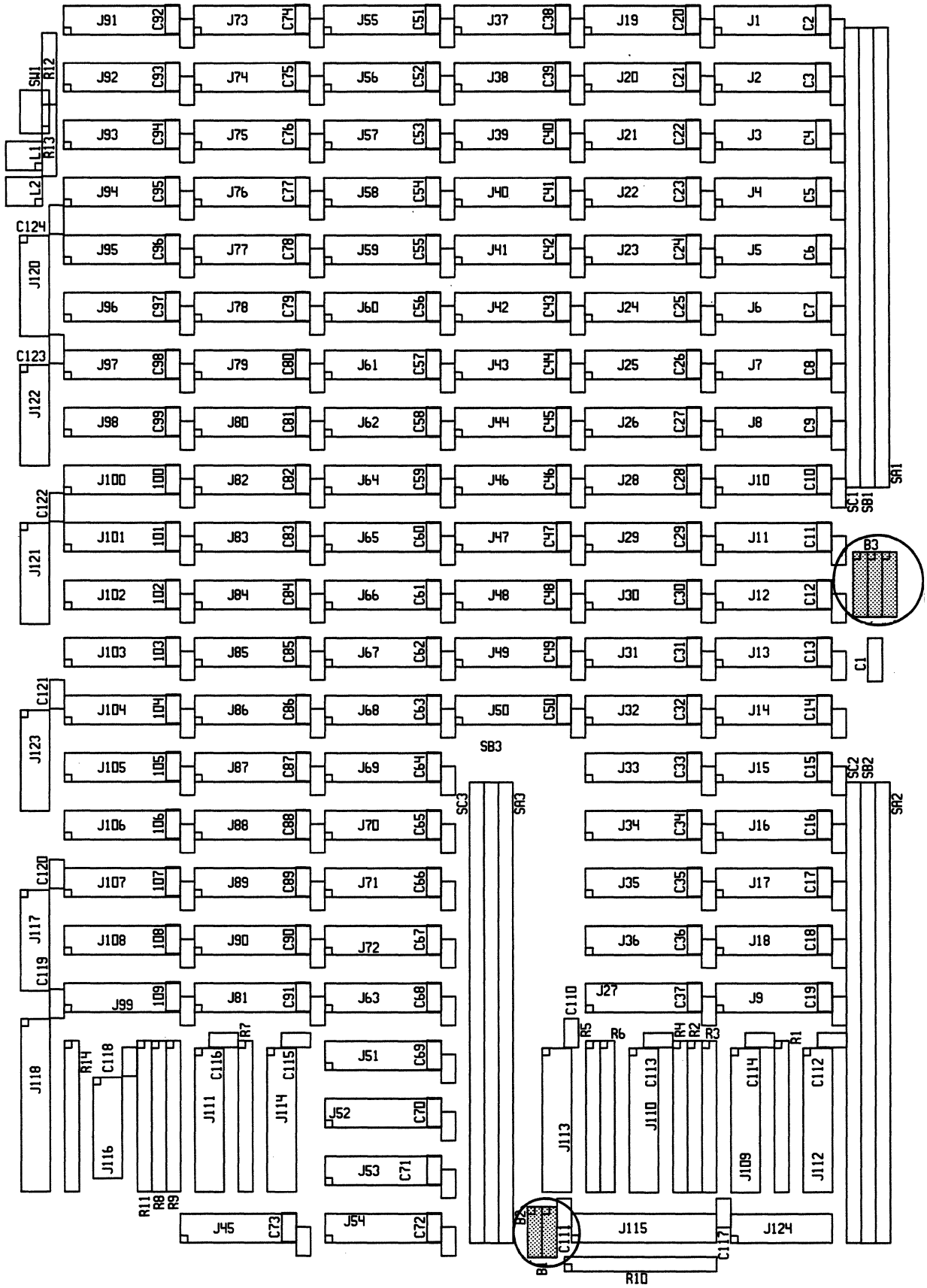
B2 Card Select



B3 Battery Backup Option



Jumper Location Diagram



Jumperfield Assignment to Access Address Selection

Mode:

START Address Selection				Selection of lst not on-board Addr		
Jumperfield			Corresponding Bus Address Signal	Jumperfield		
B7	B8	B9		B4	B5	B6
1-10			A31	1-10		
2-9			A30	2-9		
3-8			A29	3-8		
4-7			A28	4-7		
5-6			A27	5-6		
	1-10		A26		1-10	
	2-9		A25		2-9	
	3-8		A24		3-8	
	4-7		A23		4-7	
	5-6		A22		5-6	
		1-8	A21			1-8
		2-7	A20			2-7
		3-6	A19			3-6
		4-5	A18			4-5

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Default Access Address Selection for the DRAM-E3M1

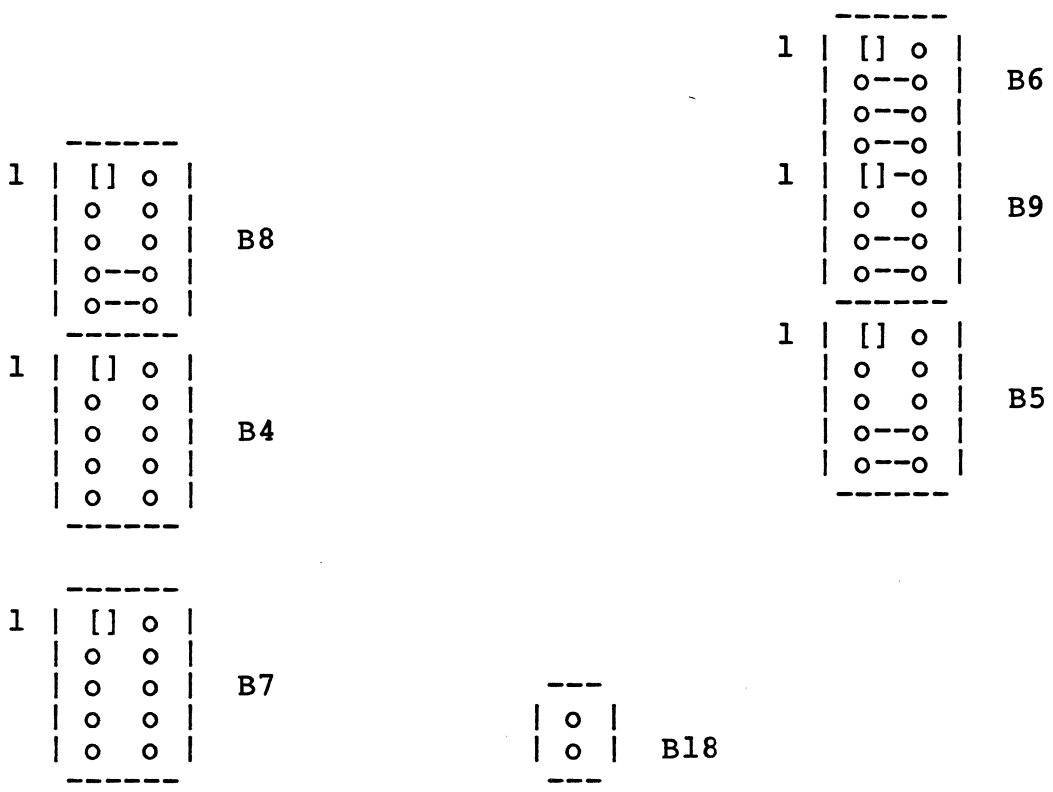
Mode: A24

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
	5-6			5-6		A22
		1-8				A21
					2-7	A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$XX10 0000	$10 0000
End Address:	$XX1F FFFF	$1F FFFF
First not on-board Address:	$XX20 0000	$20 0000
Boundary:	$0010 0000	$10 0000
	1M byte	1M byte

Default Access Address Selection for DRAM-E3M1

Mode: A24



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$XX10 0000	$10 0000
End Address:	$XX1F FFFF	$1F FFFF
First Not On-board Address:	$XX20 0000	$20 0000
Boundary:	$ 10 0000	$10 0000
	1Mbyte	1Mbyte

Access Address Selection Example 1 for DRAM-E3M1

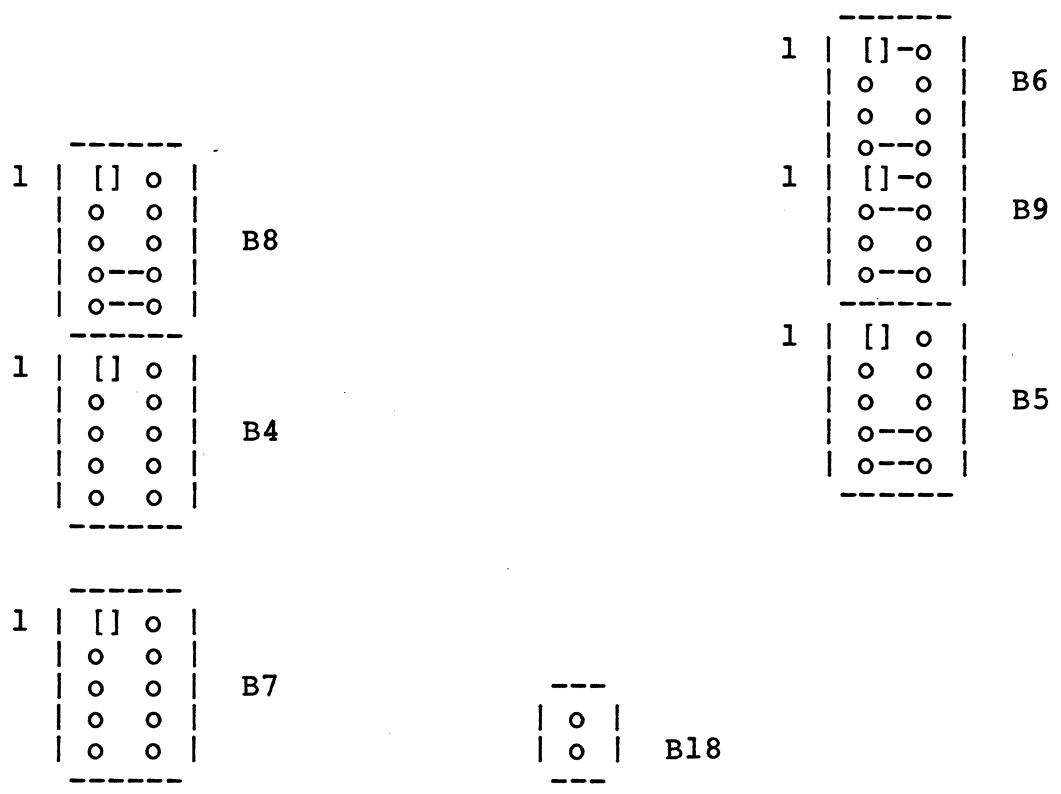
Mode: A24

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
	5-6			5-6		A22
		1-8			1-8	A21
		2-7				A20
						A19
		4-5			4-5	A18

	A32	A24
Start Address:	$XX08 0000	$08 0000
End Address:	$XX17 FFFF	$17 FFFF
First not on-board Address:	$XX18 0000	$18 0000
Boundary:	$ 10 0000	$10 0000
	1Mbyte	1Mbyte

Access Address Selection: Example 1 for DRAM-E3M1

Mode: A24



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Access Mode: Jumper B18

	A32	A24
Start Address:	$XX08 0000	$08 0000
End Address:	$XX17 FFFF	$17 FFFF
First Not On-board Address:	$XX18 0000	$18 0000
Boundary:	$ 10 0000	$10 0000
	1Mbyte	1Mbyte

Access Address Selection: Example 2 for DRAM-E3M1

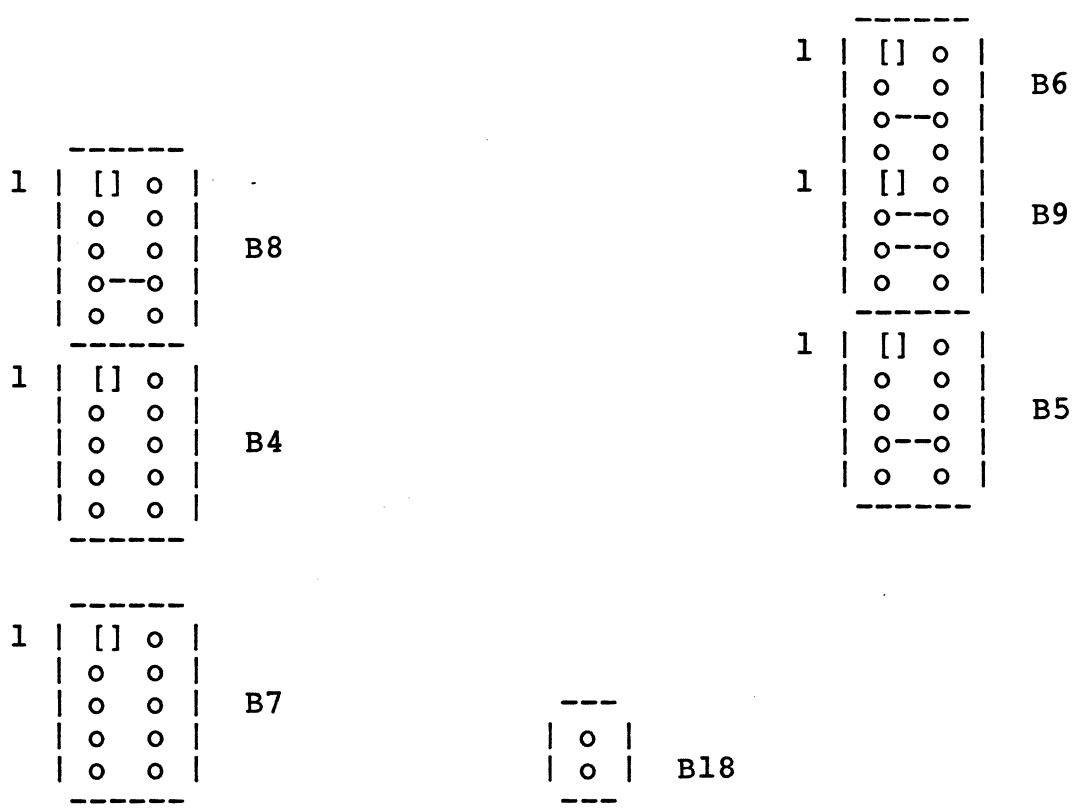
Mode: A24

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
						A22
						A21
		2-7				A20
		3-6			3-6	A19
						A18

	A32	A24
Start Address:	$XX64 0000	$64 0000
End Address:	$XX73 FFFF	$73 FFFF
First not on-board Address:	$XX74 0000	$74 0000
Boundary:	$ 10 0000	$10 0000
	1M byte	1M byte

Access Address Selection: Example 2 for DRAM-E3M1

Mode: A24



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$FF64 0000	$64 0000
End Address:	$FF73 FFFF	$73 FFFF
First Not On-board Address:	$FF74 0000	$74 0000
Boundary:	$ 10 0000	$10 0000
	1Mbyte	1Mbyte

Access Address Selection Example 3 for DRAM-E3M1

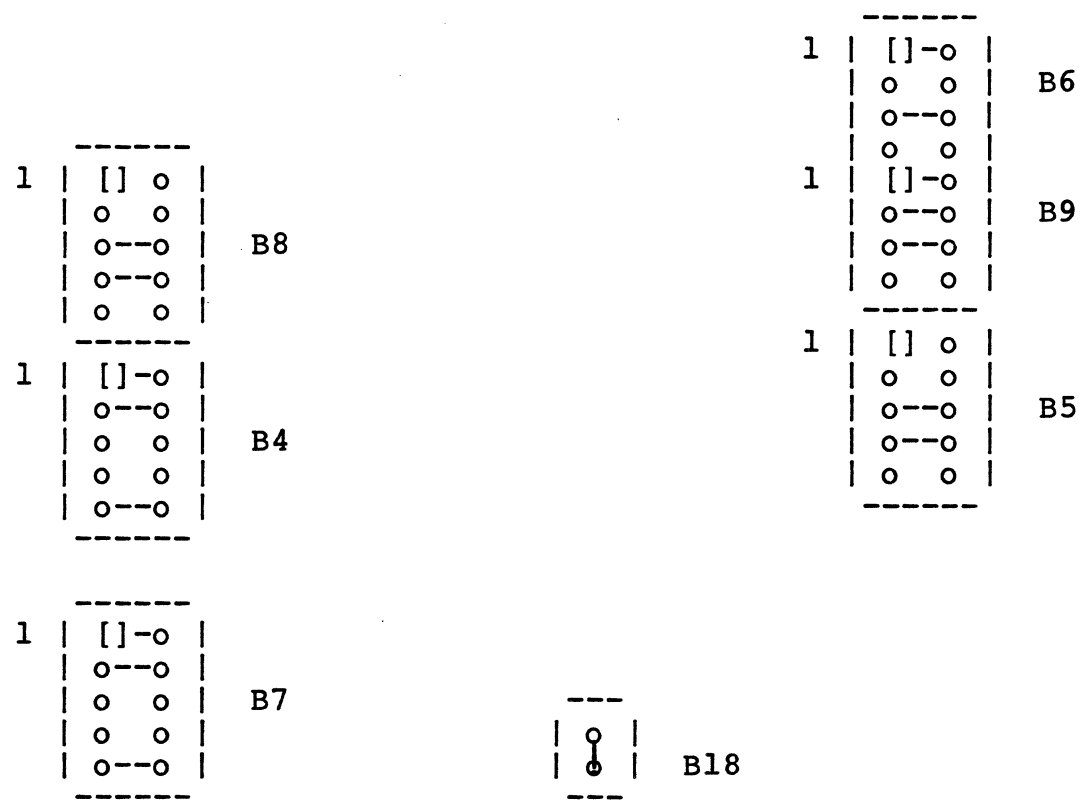
Jumper B18 must be inserted (Mode A32)

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
1-10			1-10			A31
2-9			2-9			A30
						A29
						A28
5-6			5-6			A27
						A26
						A25
	3-8			3-8		A24
	4-7			4-7		A23
						A22
		1-8			1-8	A21
		2-7				A20
		3-6			3-6	A19
						A18

	A32	A24
Start Address:	$3644 0000	
End Address:	$3653 FFFF	NOT
First not on-board Address:	$3654 0000	DECODED
Boundary:	$0010 0000	
	1M byte	1M byte

Access Address Selection: Example 3 for DRAM-E3M1

Mode: A32



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$3644 0000	
End Address:	$3653 FFFF	
First Not On-board Address:	$3654 0000	
Boundary:	$ 10 0000	
	1Mbyte	

Access Address Selection Example 4 for DRAM-E3M1

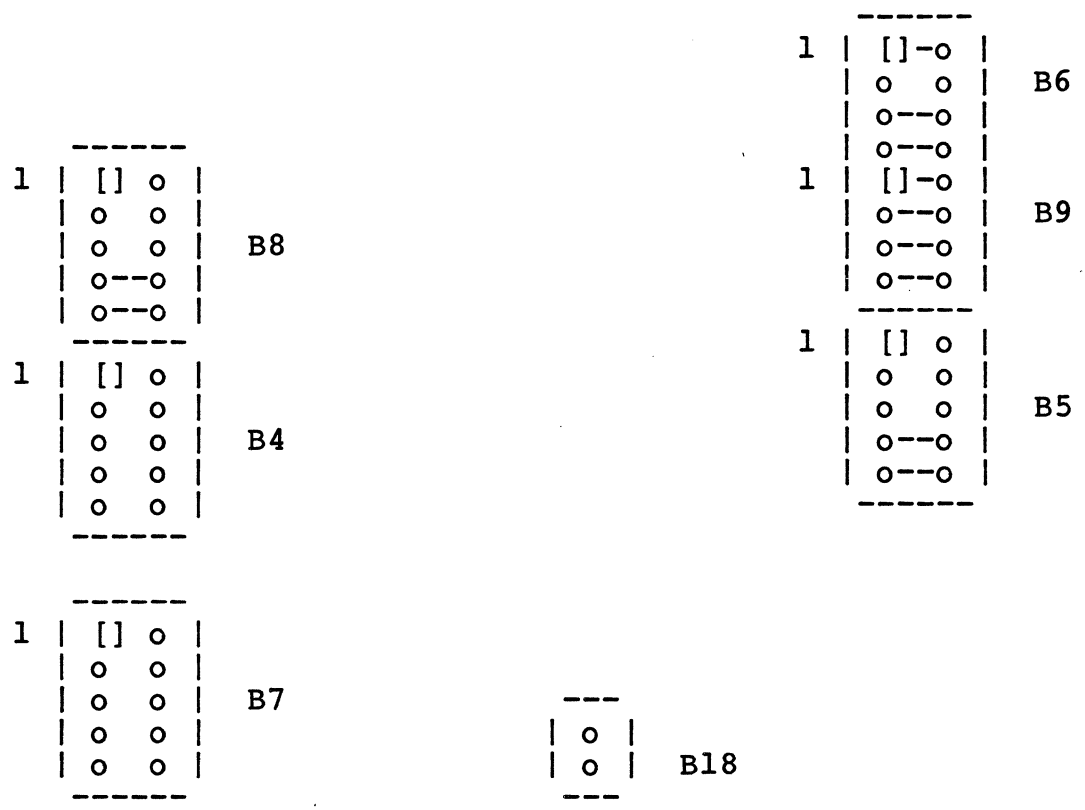
Mode: A24

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
	5-6			5-6		A22
		1-8			1-8	A21
		2-7				A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$XX00 0000	$00 0000
End Address:	$XX0F FFFF	$0F FFFF
First not on-board Address:	$XX10 0000	$10 0000
Boundary:	$ 10 0000	$10 0000
	1M byte	1M byte

Access Address Selection: Example 4 for DRAM-E3M1

Mode: A24

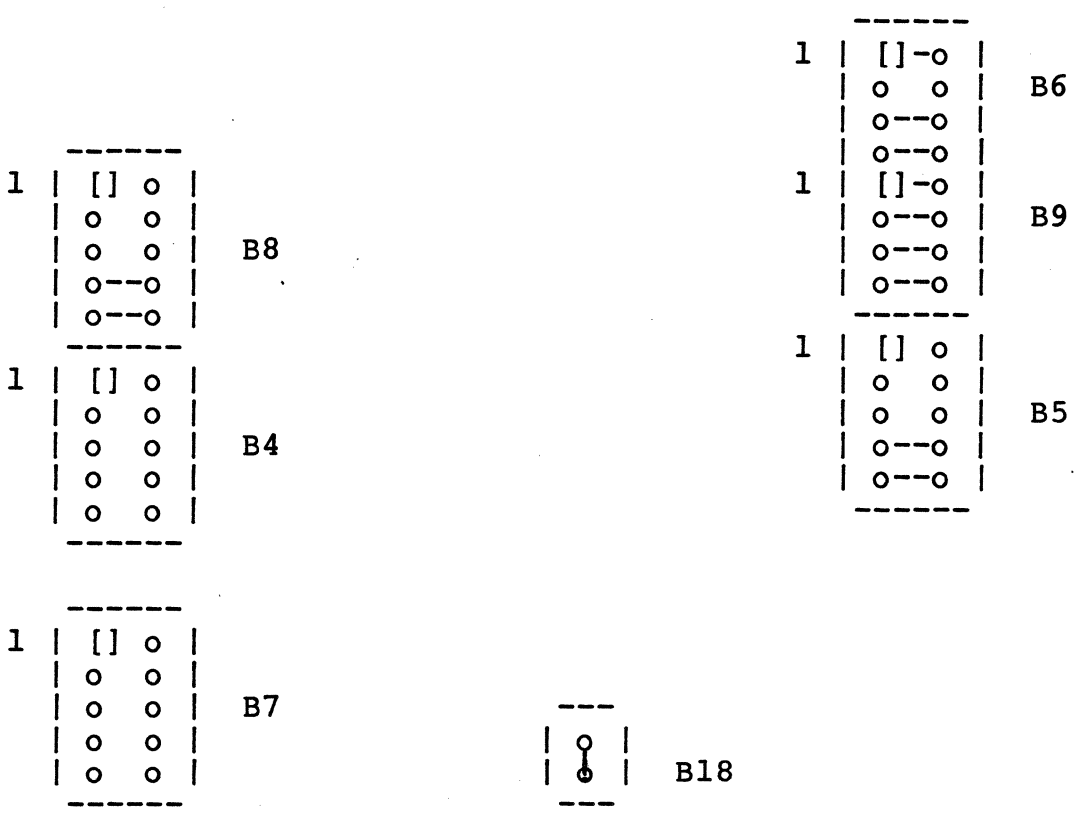


Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$XX00 0000	$00 0000
End Address:	$XX0F FFFF	$0F FFFF
First Not On-board Address:	$XX10 0000	$10 0000
Boundary:	$ 10 0000	$10 0000
	1Mbyte	1Mbyte

Access Address Selection: Example 4a for DRAM-E3M1

Mode: A32



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$FF00 0000	$00 0000
End Address:	$FF0F FFFF	$0F FFFF
First Not On-board Address:	$FF10 0000	$10 0000
Boundary:	$ 10 0000	$10 0000
	1Mbyte	1Mbyte

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Access Address Selection: Example 4b for DRAM-E3M1

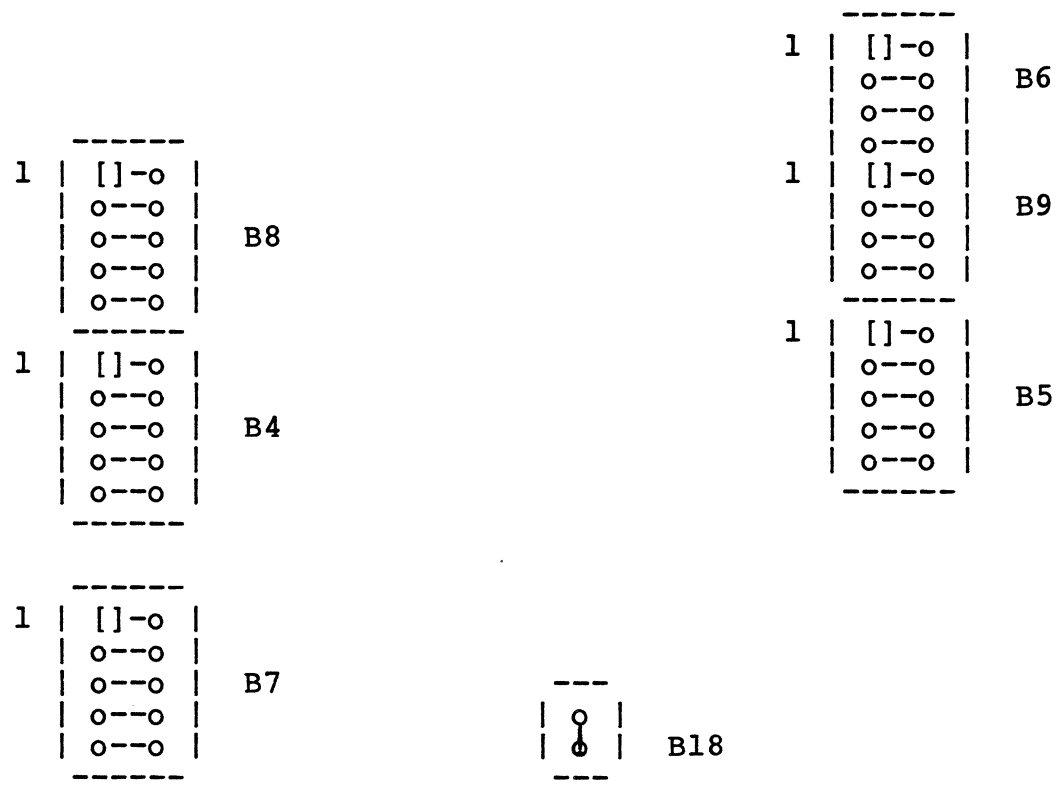
Jumper B18 must be inserted (Mode A32)

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
1-10			1-10			A31
2-9			2-9			A30
3-8			3-8			A29
4-7			4-7			A28
5-6			5-6			A27
	1-10			1-10		A26
	2-9			2-9		A25
	3-8			3-8		A24
	4-7			4-7		A23
	5-6			5-6		A22
		1-8			1-8	A21
		2-7				A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$0000 0000	
End Address:	$000F FFFF	
First not on-board Address:	$0010 0000	
Boundary:	$ 10 0000	
	1M byte	

Access Address Selection: Example 4b for DRAM-E3M1

Mode: A32



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$0000 0000	$00 0000
End Address:	$000F FFFF	$0F FFFF
First Not On-board Address:	$0010 0000	$10 0000
Boundary:	$ 10 0000	$10 0000
	1Mbyte	1Mbyte

Access Address Selection for DRAM-E3M1

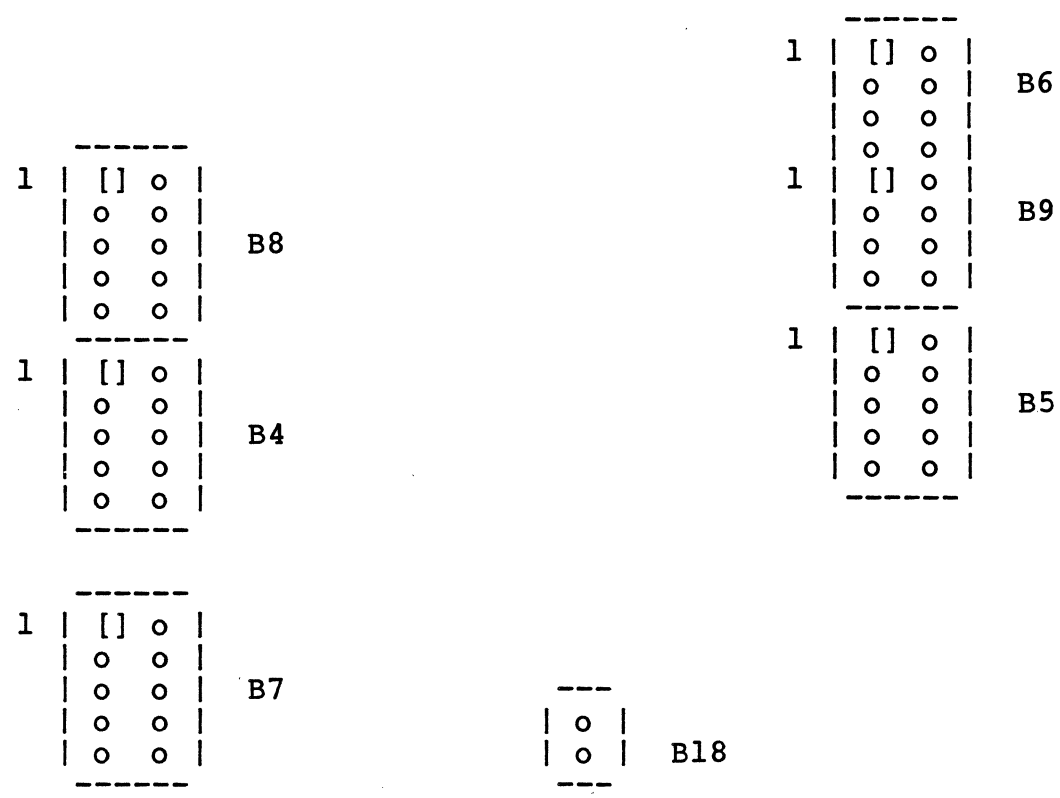
Mode:

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
						A23
						A22
						A21
						A20
						A19
						A18

	A32	A24
Start Address:	$	$
End Address:	$	$
First not on-board Address:	$	$
Boundary:	$	$
	1M byte	1M byte

Access Address Selection: Example for DRAM-E3M1

Mode:



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$ 0000	$ 0000
End Address:	$ FFFF	$ FFFF
First Not On-board Address:	$ 0000	$ 0000
Boundary:	$ 10 0000	$10 0000
	1Mbyte	1Mbyte

Default Access Address Selection for DRAM-E4M4

Mode: A24

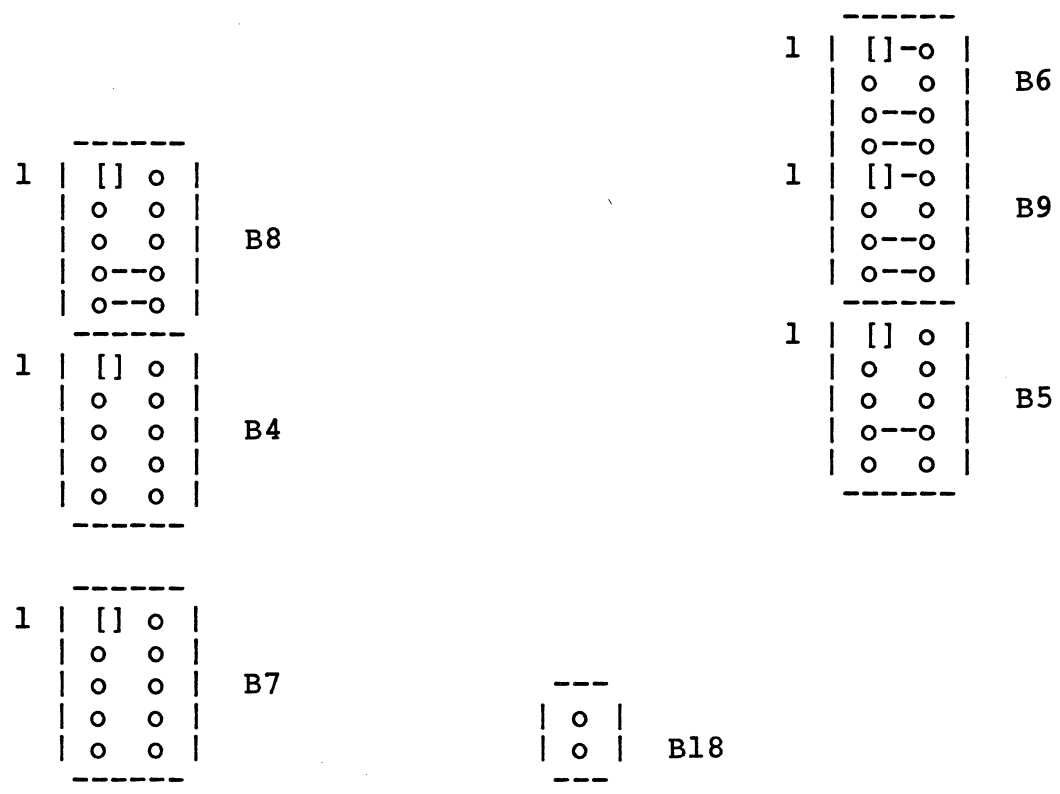
Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
	5-6					A22
		1-8			1-8	A21
						A20
		3-6			3-6	A19
		4-5			4-5	A18

Default

	A32	A24
Start Address:	$XX10 0000	$10 0000
End Address:	$XX4F FFFF	$4F FFFF
First not on-board Address:	$XX50 0000	$50 0000
Boundary:	$ 40 0000	$40 0000
	4M byte	4M byte

Default Access Address Selection: Example for DRAM-E4M4

Mode: A24



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$XX10 0000	$10 0000
End Address:	$XX4F FFFF	$4F FFFF
First Not On-board Address:	$XX50 0000	$50 0000
Boundary:	$ 40 0000	$40 0000
	4Mbyte	4Mbyte

Access Address Selection Example 1 for DRAM-E4M4

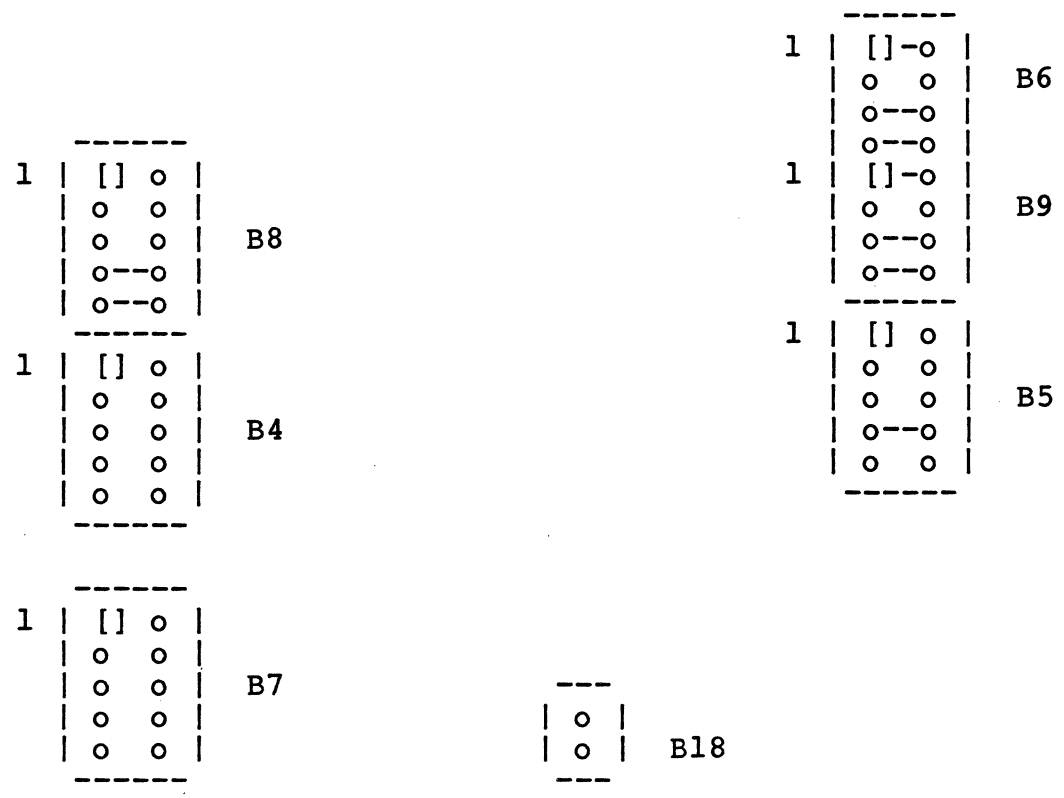
Jumper B18 must be removed (Mode A24)

Start Address			First not on-board Address			Corresponding Bus Address Signal	
B7	B8	B9	B4	B5	B6		HEX
						A31	8
						A30	4
						A29	2
						A28	1
						A27	8
						A26	4
						A25	2
						A24	1
	4-7			4-7		A23	8
	5-6					A22	4
		1-8			1-8	A21	2
						A20	1
		3-6			3-6	A19	8
		4-5			4-5	A18	4

	A32	A24
Start Address:	$XX10 0000	$10 0000
End Address:	$XX4F FFFF	$4F FFFF
First not on-board Address:	$XX50 0000	$50 0000
Boundary:	$ 40 0000	$40 0000
	4M byte	4M byte

Access Address Selection: Example 1 for DRAM-E4M4

Mode: A24

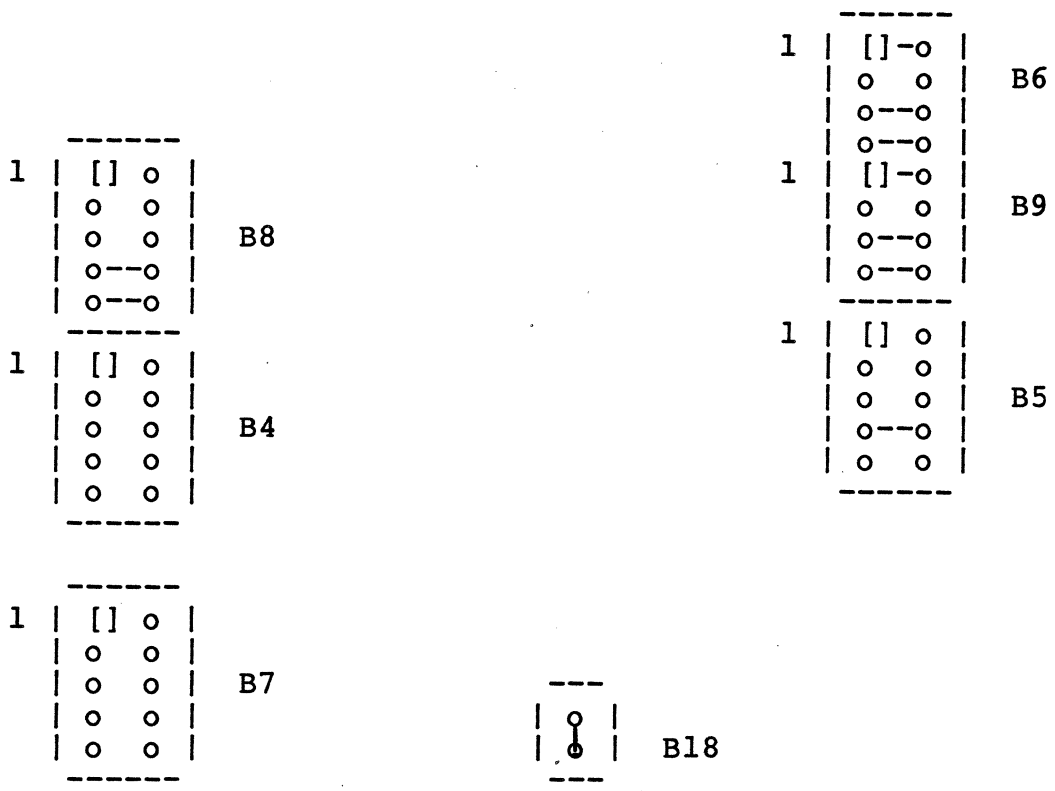


Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$XX10 0000	$10 0000
End Address:	$XX4F FFFF	$4F FFFF
First Not On-board Address:	$XX50 0000	$50 0000
Boundary:	$ 40 0000	$40 0000
	4Mbyte	4Mbyte

Access Address Selection: Example 1a for DRAM-E4M4

Mode: A32



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FF4F FFFF	$4F FFFF
First Not On-board Address:	$FF50 0000	$50 0000
Boundary:	$ 40 0000	$40 0000
	4Mbyte	4Mbyte

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Access Address Selection Example 1b for DRAM-E4M4

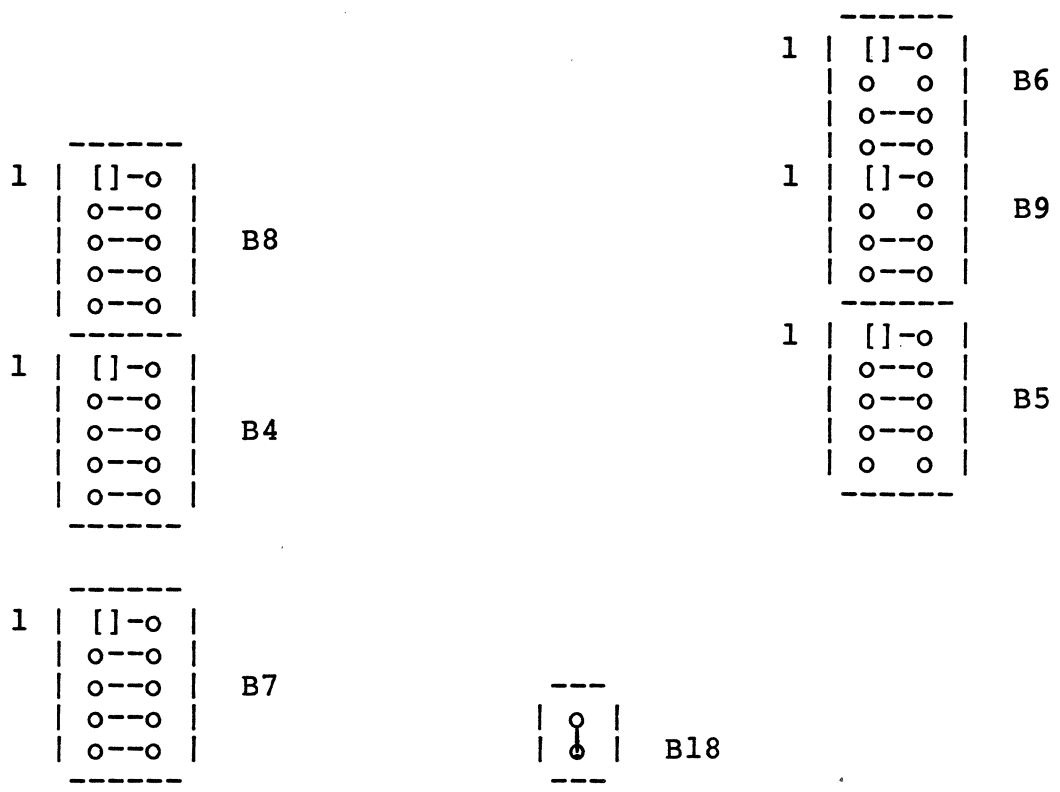
Jumper B18 must be removed (Mode A32)

Start Address			First not on-board Address			Corresponding Bus Address Signal	
B7	B8	B9	B4	B5	B6		HEX
1-10			1-10			A31	8
2-9			2-9			A30	4
3-8			3-8			A29	2
4-7			4-7			A28	1
5-6			5-6			A27	8
	1-10			1-10		A26	4
	2-9			2-9		A25	2
	3-8			3-8		A24	1
	4-7			4-7		A23	8
	5-6					A22	4
		1-8			1-8	A21	2
						A20	1
		3-6			3-6	A19	8
		4-5			4-5	A18	4

	A32	A24
Start Address:	$0010 0000	
End Address:	$004F FFFF	
First not on-board Address:	$0050 0000	
Boundary:	$ 40 0000 4M byte	

Access Address Selection: Example 1b for DRAM-E4M4

Mode: A32



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$0010 0000	
End Address:	$004F FFFF	
First Not On-board Address:	$0050 0000	
Boundary:	$ 40 0000	
	4Mbyte	

Access Address Selection Example User for DRAM-E4M4

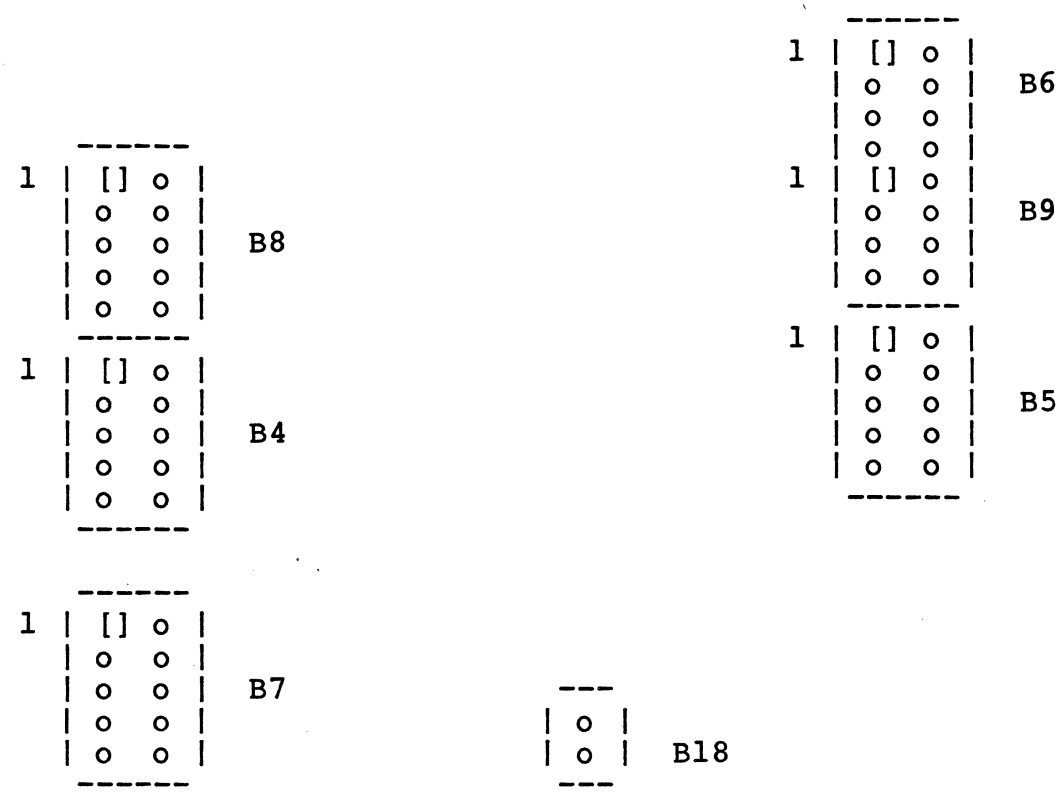
Mode:

Start Address			First not on-board Address			Corresponding Bus Address Signal	
B7	B8	B9	B4	B5	B6		HEX
						A31	8
						A30	4
						A29	2
						A28	1
						A27	8
						A26	4
						A25	2
						A24	1
						A23	8
						A22	4
						A21	2
						A20	1
						A19	8
						A18	4

	A32	A24
Start Address:	$ 0000	$ 0000
End Address:	$ FFFF	$ FFFF
First not on-board Address:	$ 0000	$ 0000
Boundary:	$ 40 0000	$40 0000
	4M byte	4Mbyte

Access Address Selection: Example User for DRAM-E4M4

Mode:



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$ 0000	$ 0000
End Address:	$ FFFF	$ FFFF
First Not On-board Address:	$ 0000	$ 0000
Boundary:	$ 40 0000	$40 0000
	4Mbyte	4Mbyte

Access Address Selection Example 1 using one DRAM-E3S1

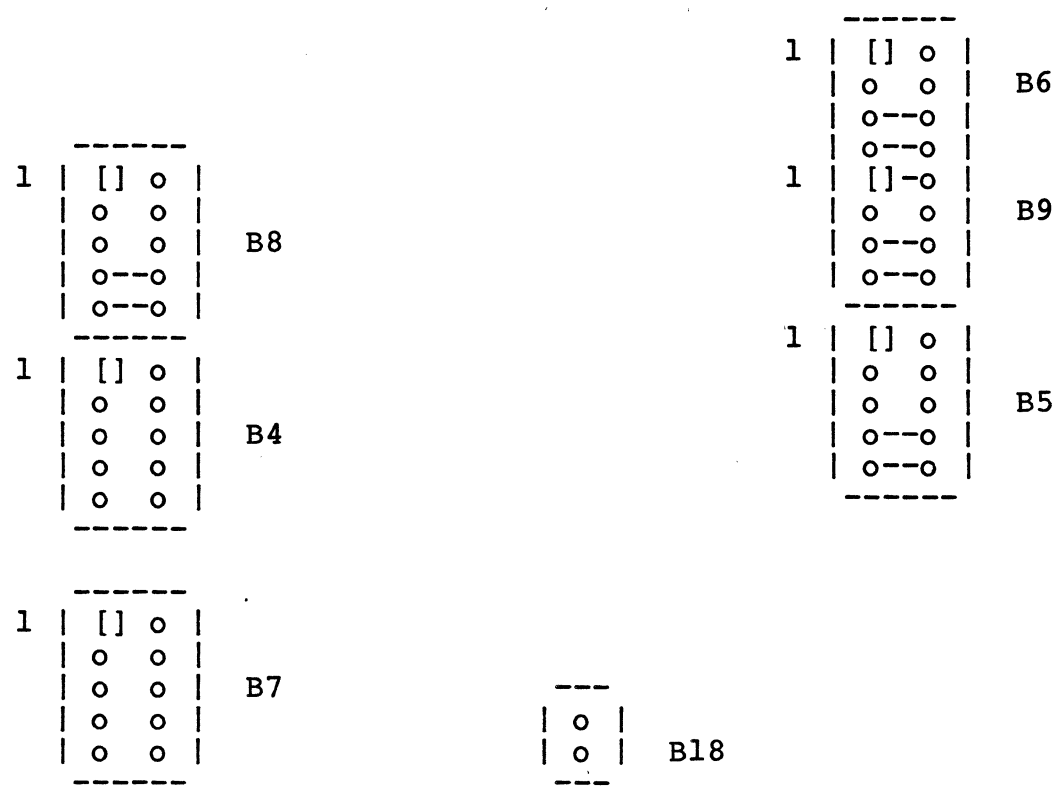
Mode: A24

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
	5-6			5-6		A22
		1-8				A21
						A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$XX10 0000	$10 0000
End Address:	$XX2F FFFF	$2F FFFF
First not on-board Address:	$XX30 0000	$30 0000
Boundary:	$0020 0000	$20 0000
	2M byte	2M byte

Access Address Selection: Example 1 using one DRAM-E3S1

Mode: A24

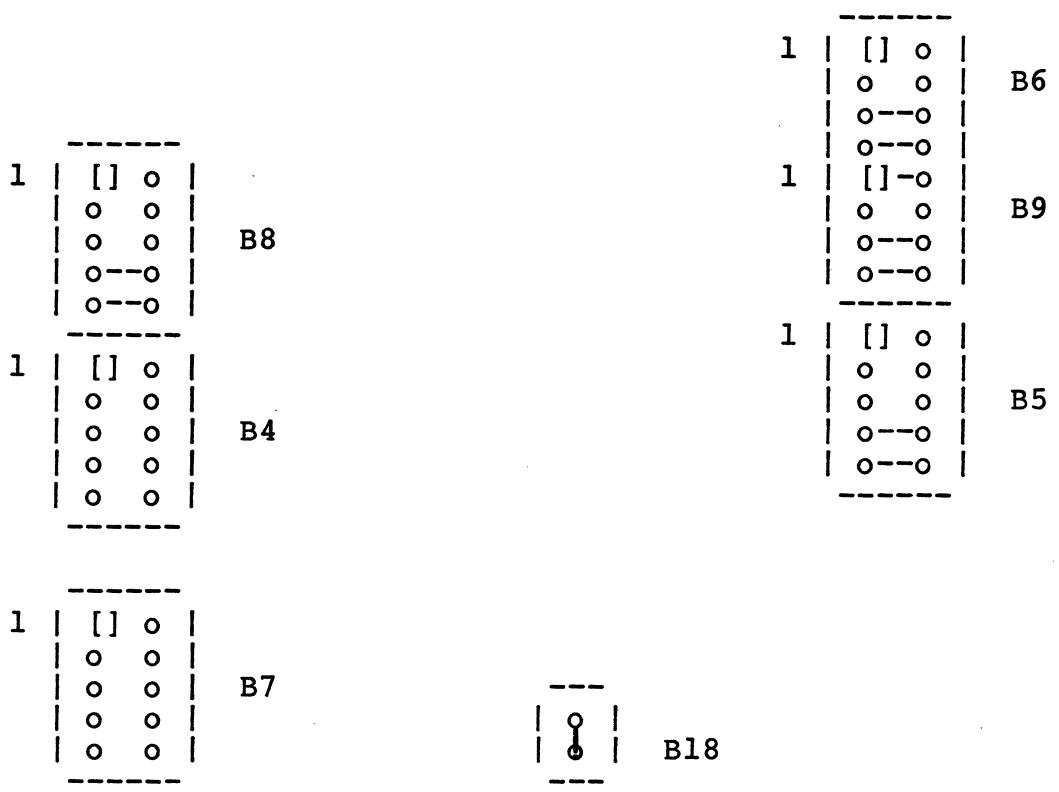


Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$XX10 0000	$10 0000
End Address:	$XX2F FFFF	$2F FFFF
First Not On-board Address:	$XX30 0000	$30 0000
Boundary:	$ 20 0000	$20 0000
	2Mbyte	2Mbyte

Access Address Selection: Example 1a using one DRAM-E3S1

Mode: A32



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FF2F FFFF	$2F FFFF
First Not On-board Address:	$FF30 0000	$30 0000
Boundary:	$ 20 0000	$20 0000
	2Mbyte	2Mbyte

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Access Address Selection Example 2 using one DRAM-E3S3

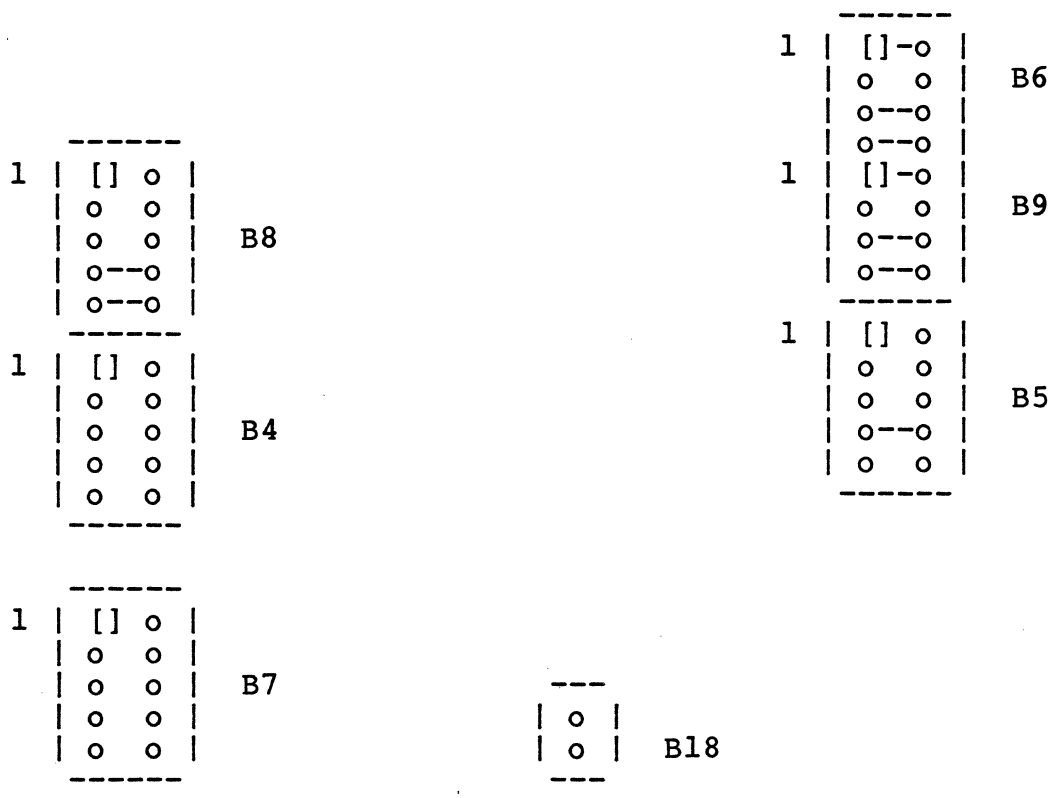
Mode: A24

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7			4-7		A23
	5-6					A22
		1-8			1-8	A21
						A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$XX10 0000	$10 0000
End Address:	$XX4F FFFF	$4F FFFF
First not on-board Address:	$XX50 0000	$50 0000
Boundary:	$0040 0000	$40 0000
	4M byte	4M byte

Access Address Selection: Example 2 using one DRAM-E3S3

Mode: A24

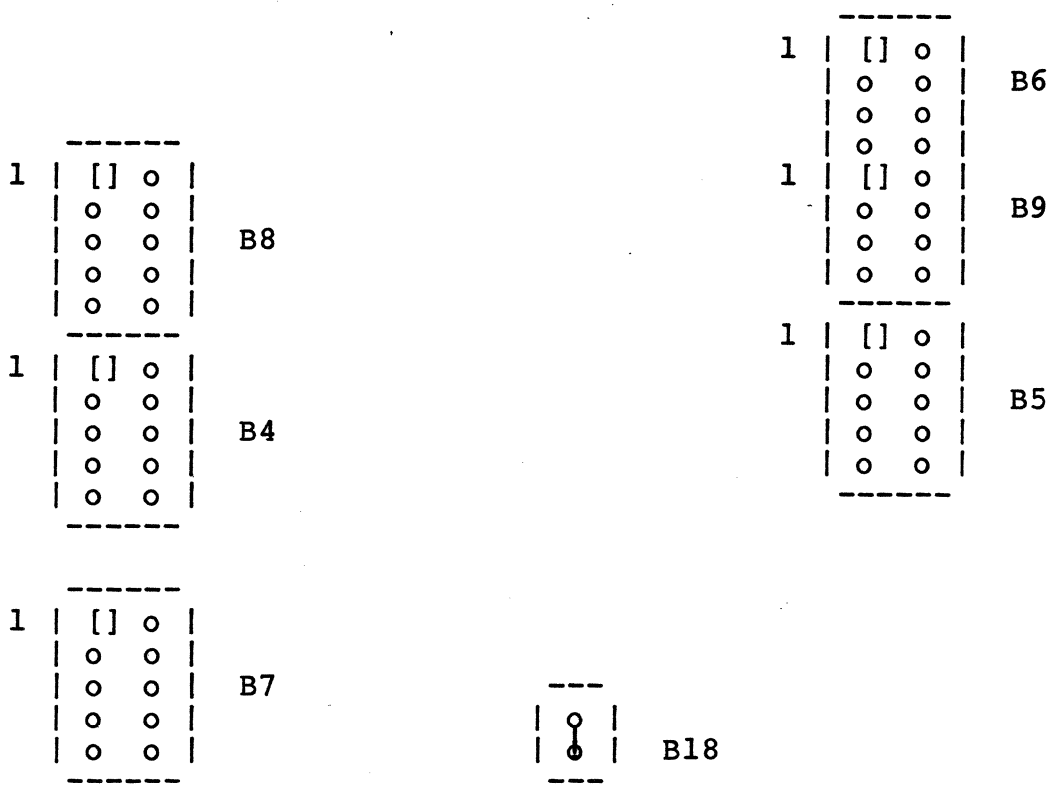


Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$XX10 0000	$10 0000
End Address:	$XX4F FFFF	$4F FFFF
First Not On-board Address:	$XX50 0000	$50 0000
Boundary:	$ 40 0000	$40 0000
	4Mbyte	4Mbyte

Access Address Selection: Example 2a using one DRAM-E3S3

Mode: A32



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FF4F FFFF	$4F FFFF
First Not On-board Address:	$FF50 0000	$50 0000
Boundary:	$ 40 0000	$40 0000
	4Mbyte	4Mbyte

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Access Address Selection: Example 2b using one DRAM-E3S3

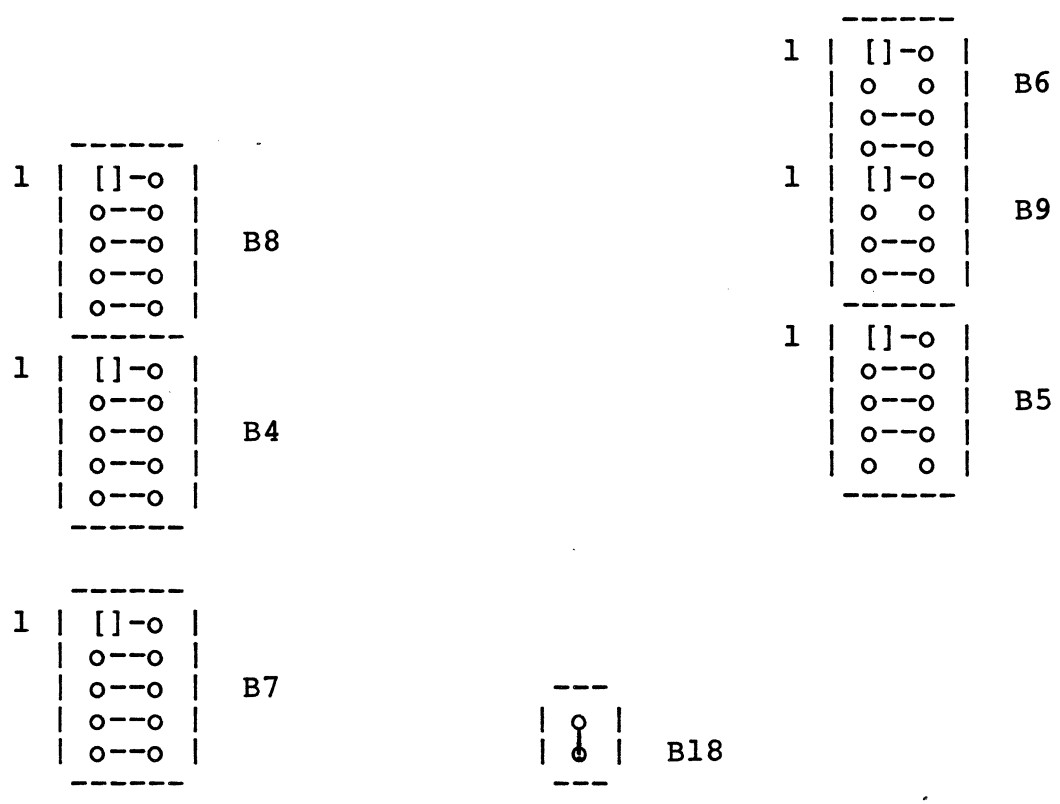
Jumper B18 must be inserted (Mode A32)

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
1-10			1-10			A31
2-9			2-9			A30
3-8			3-8			A29
4-7			4-7			A28
5-6			5-6			A27
	1-10			1-10		A26
	2-9			2-9		A25
	3-8			3-8		A24
	4-7			4-7		A23
	5-6					A22
		1-8			1-8	A21
						A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$0010 0000	
End Address:	$004F FFFF	
First not on-board Address:	$0050 0000	
Boundary:	$ 40 0000	
	4M byte	

Access Address Selection: Example 2b using one DRAM-E3S3

Mode: A32



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$0010 0000	
End Address:	$004F FFFF	
First Not On-board Address:	$0050 0000	
Boundary:	$ 40 0000	
	4Mbyte	

Access Address Selection: Example 3 using one DRAM-E3S6 or two DRAM-E3S3 Boards

Mode: A24

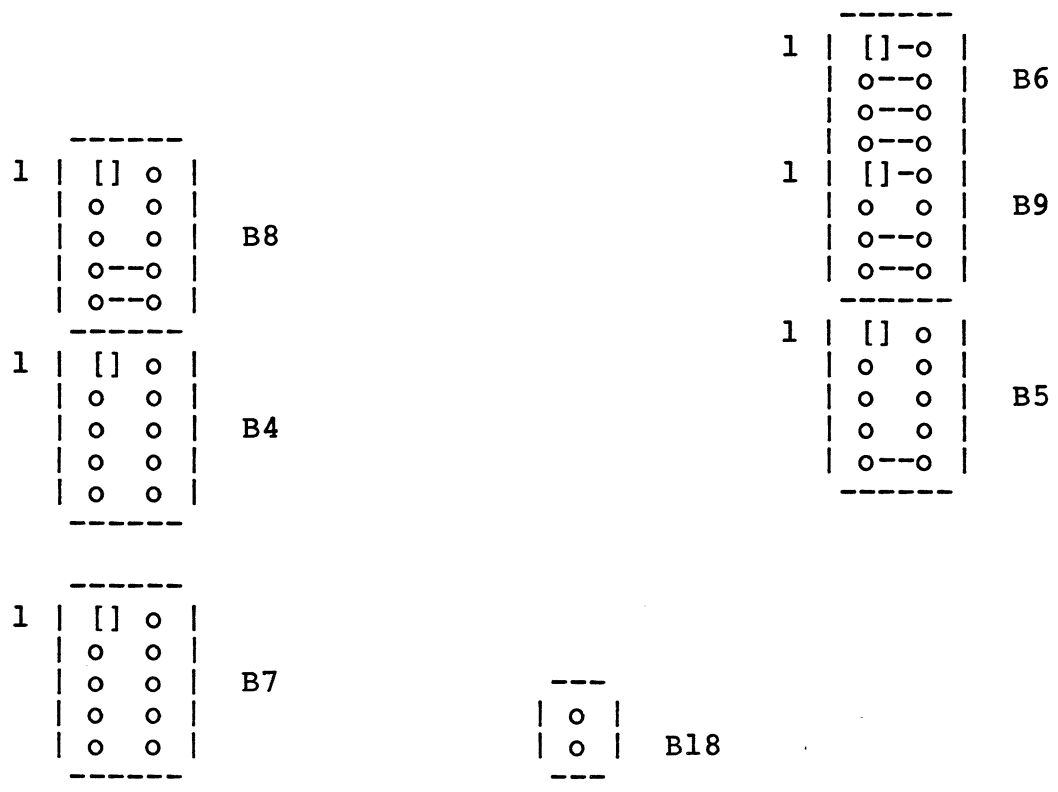
Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7					A23
	5-6			5-6		A22
		1-8			1-8	A21
					2-7	A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$XX10 0000	$10 0000
End Address:	$XX7F FFFF	$7F FFFF
First not on-board Address:	$XX80 0000	$80 0000
Boundary:	$0070 0000	$70 0000
	7M byte	7M byte

Access Address Selection: Example 3 using one DRAM-E3S6

or two DRAM-E3S3 Boards

Mode: A24

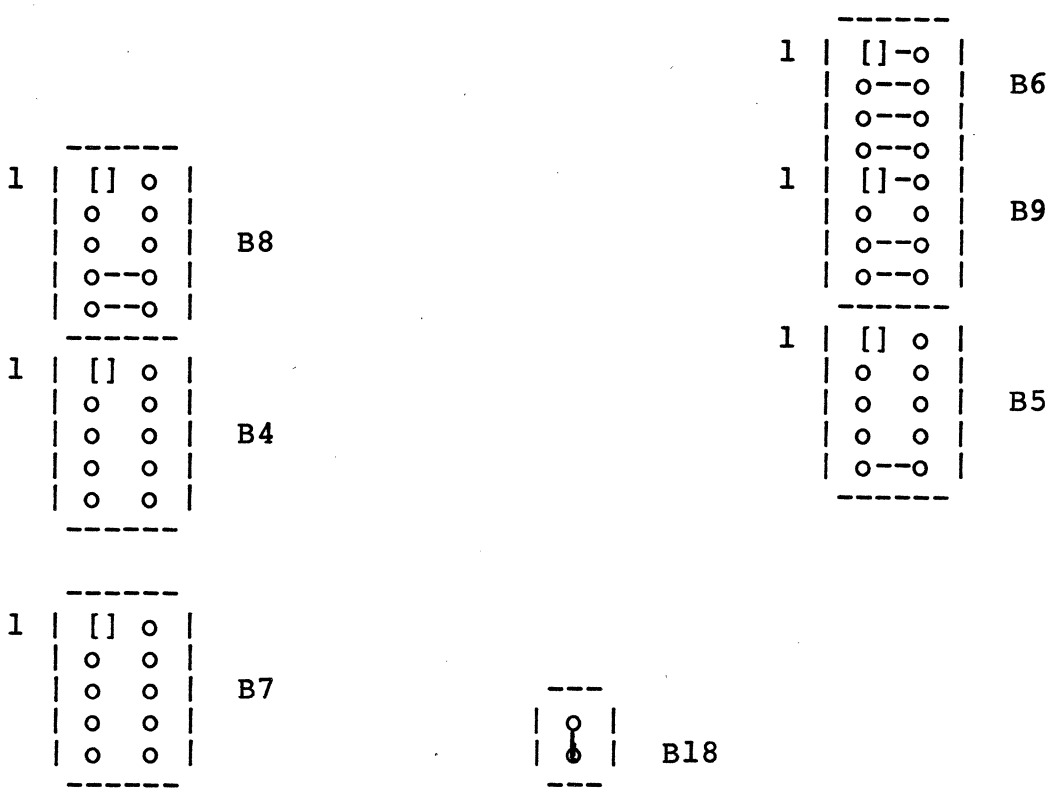


Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$XX10 0000	$10 0000
End Address:	$XX7F FFFF	$7F FFFF
First Not On-board Address:	$XX80 0000	$80 0000
Boundary:	$ 70 0000	$70 0000
	7Mbyte	7Mbyte

Access Address Selection: Example 3a using one DRAM-E3S6 or two DRAM-E3S3 Boards

Mode: A32



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FF7F FFFF	$7F FFFF
First Not On-board Address:	$FF80 0000	$80 0000
Boundary:	$ 70 0000	$70 0000
	7Mbyte	7Mbyte

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Access Address Selection: Example 3b using one DRAM-E3S6 or two DRAM-E3S3 Boards

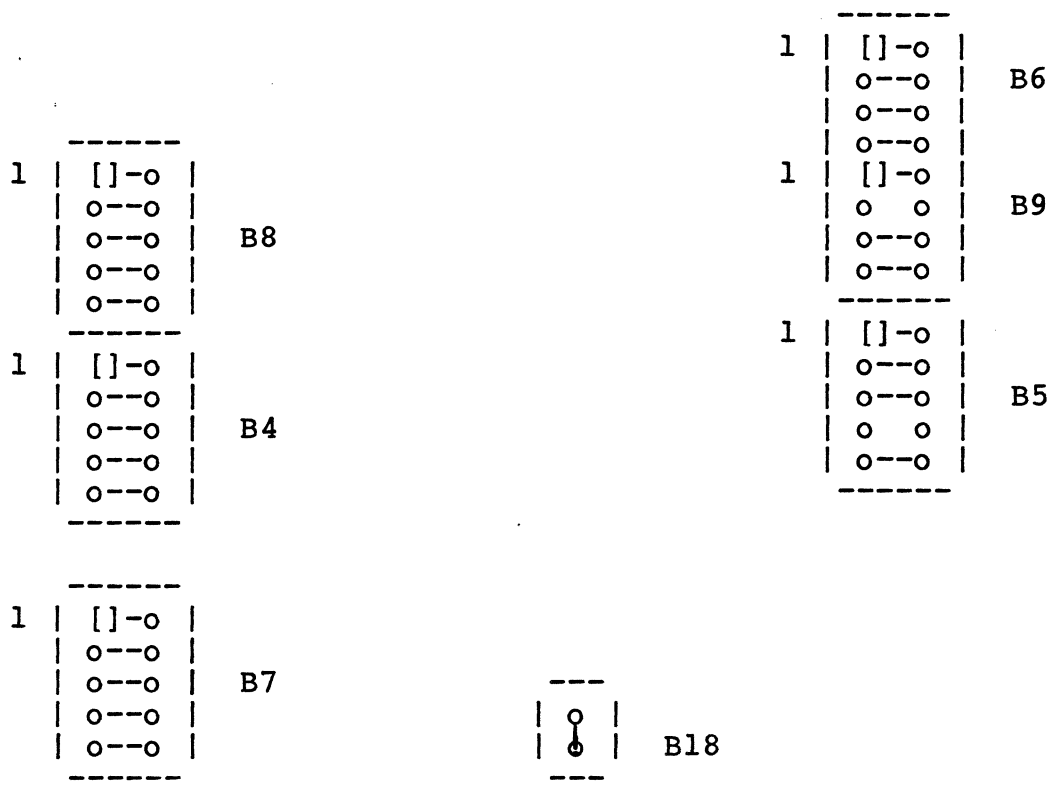
Jumper B18 must be inserted (Mode A32)

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
1-10			1-10			A31
2-9			2-9			A30
3-8			3-8			A29
4-7			4-7			A28
5-6			5-6			A27
	1-10			1-10		A26
	2-9			2-9		A25
	3-8			3-8		A24
	4-7					A23
	5-6			5-6		A22
		1-8			1-8	A21
					2-7	A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$0010 0000	
End Address:	$007F FFFF	
First not on-board Address:	$0080 0000	
Boundary:	$0070 0000	
	7Mbyte	

Access Address Selection: Example 3b using one DRAM-E3S6 or two DRAM-E3S3 Boards

Mode: A32



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$0010 0000	
End Address:	$007F FFFF	
First Not On-board Address:	$0080 0000	
Boundary:	$ 70 0000	
	7Mbyte	

Access Address Selection: Example 4 using two DRAM-E3S6

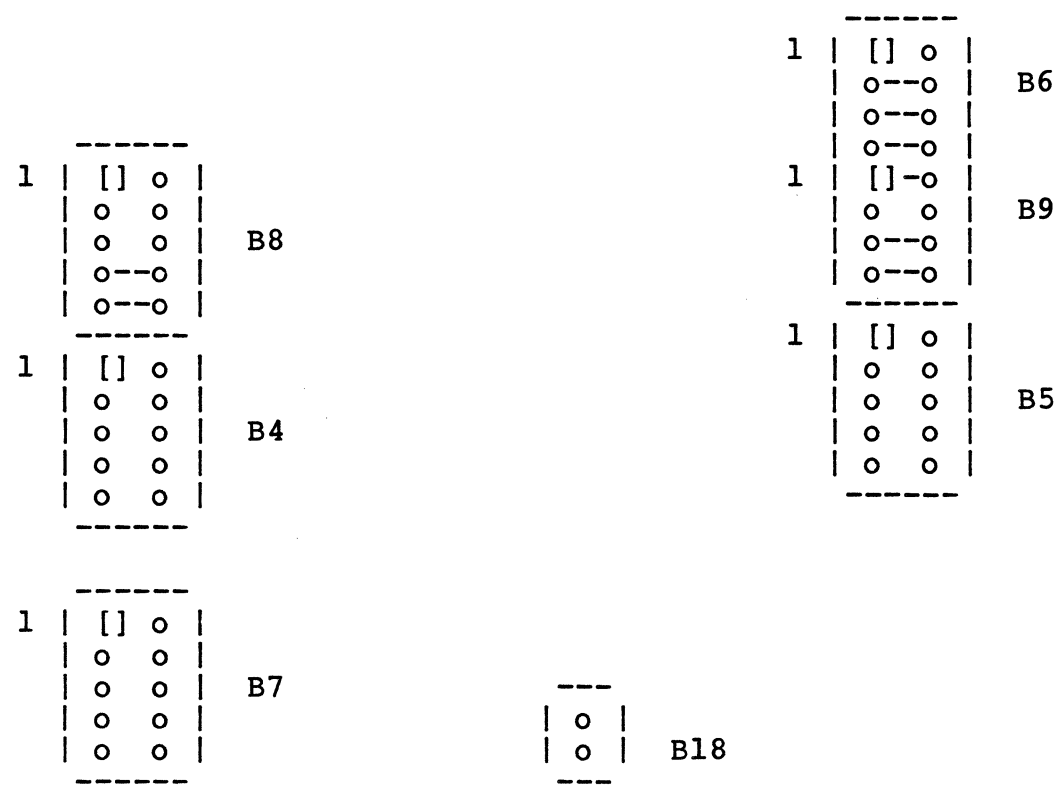
Mode: A24

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
	4-7					A23
	5-6					A22
		1-8				A21
					2-7	A20
		3-6			3-6	A19
		4-5			4-5	A18

	A32	A24
Start Address:	$XX10 0000	$10 0000
End Address:	$XXDF FFFF	$DF FFFF
First not on-board Address:	$XXE0 0000	$E0 0000
Boundary:	$00D0 0000	$D00 000
	13M byte	13M byte

Access Address Selection: Example 4 using one DRAM-E3S6

Mode: A24

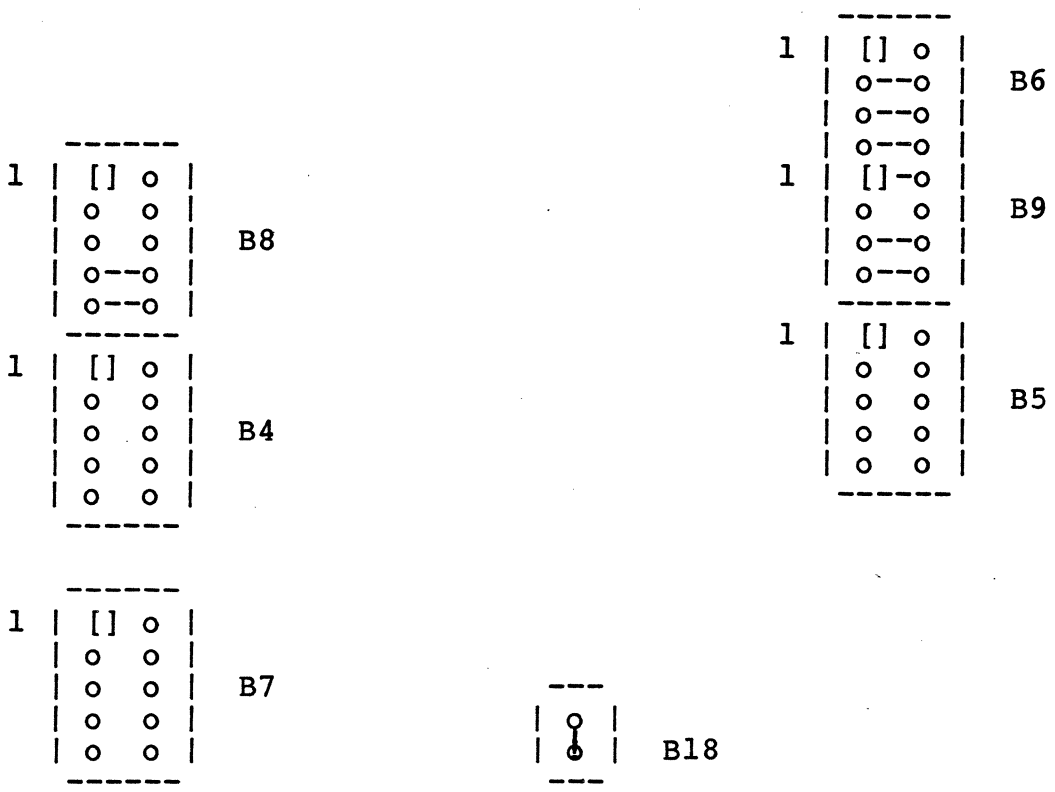


Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$XX10 0000	$10 0000
End Address:	$XXDF FFFF	$DF FFFF
First Not On-board Address:	$XXE0 0000	$E0 0000
Boundary:	$ D0 0000	$D0 0000
	13Mbyte	13Mbyte

Access Address Selection: Example 4a using one DRAM-E3S6

Mode: A32

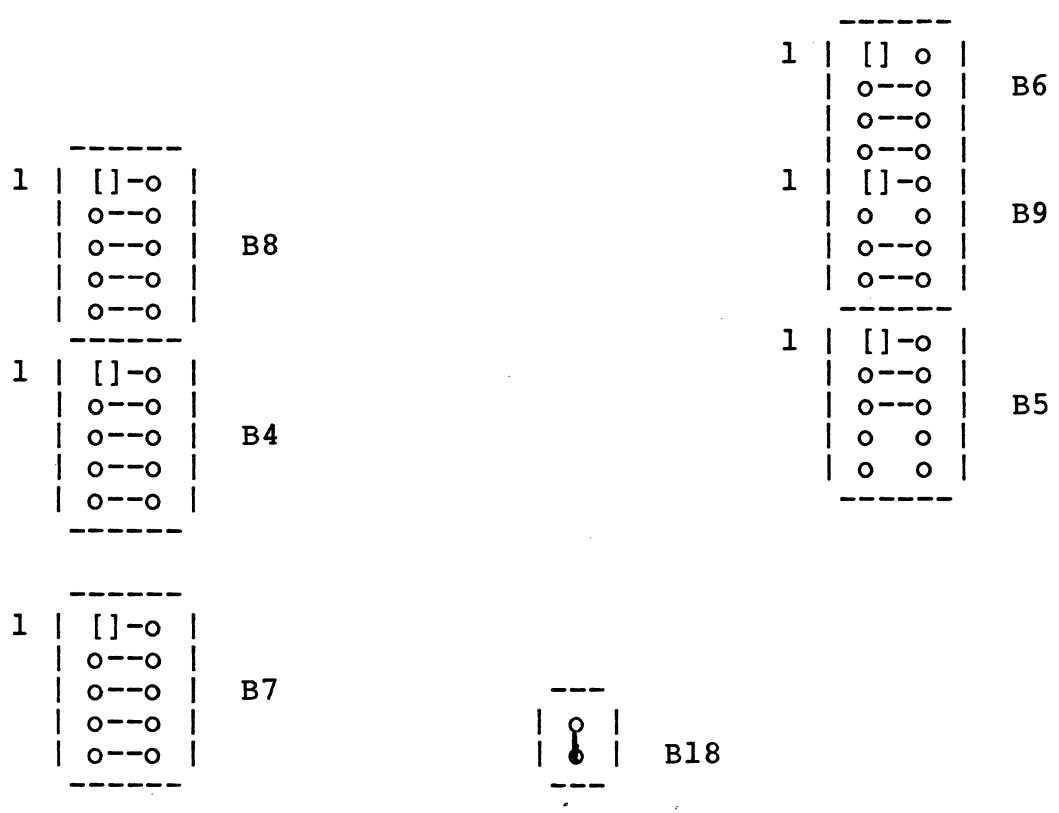


Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$FF10 0000	$10 0000
End Address:	$FFDF FFFF	$DF FFFF
First Not On-board Address:	$FFE0 0000	$E0 0000
Boundary:	$ D0 0000	$D0 0000
	13Mbyte	13Mbyte

Access Address Selection: Example 4b using one DRAM-E3S6

Mode: A32



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$0010 0000	
End Address:	$00DF FFFF	
First Not On-board Address:	$00E0 0000	
Boundary:	$ D0 0000	
	13Mbyte	

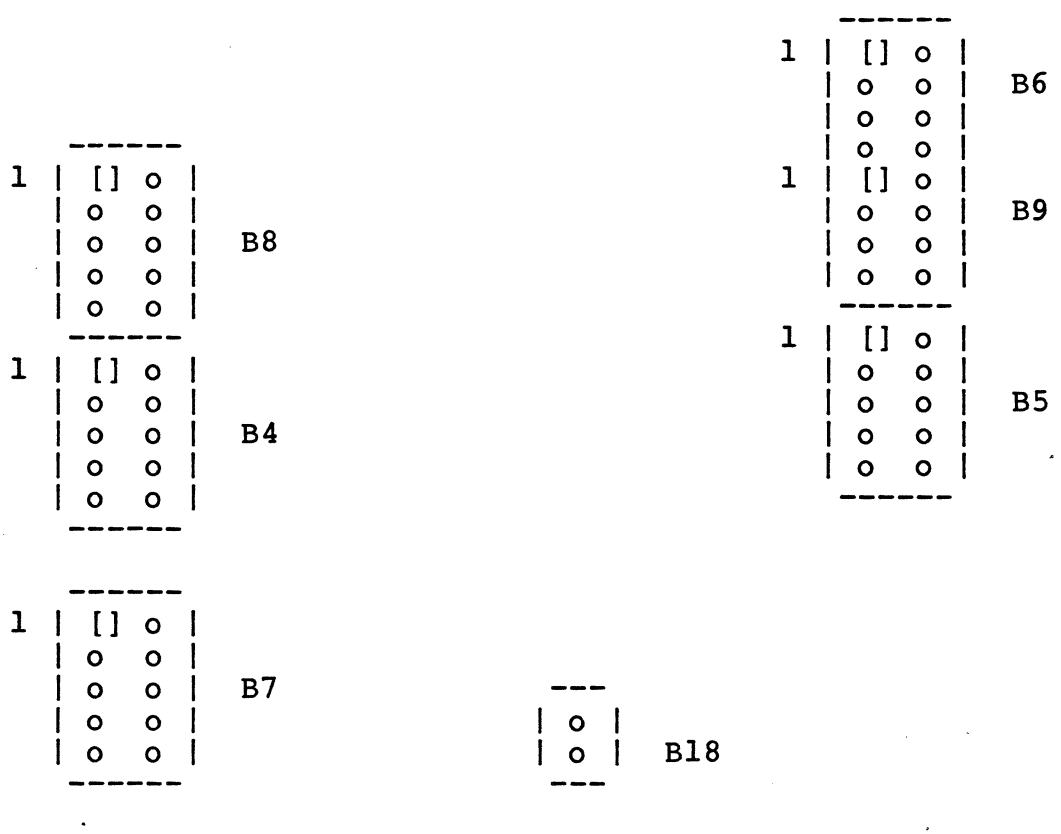
Access Address Selection Example USER using two DRAM-E3SX

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
						A23
						A22
						A21
						A20
						A19
						A18

	A32	A24
Start Address:	$	$
End Address:	$	$
First not on-board Address:	$	$
Boundary:	$	$
	1M byte	1M byte

Access Address Selection: Example USER using one DRAM-E3SX

Mode:



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$ Ø 0000	$ Ø 0000
End Address:	$ FFFF	$ FFFF
First Not On-board Address:	$ 0000	$ 0000
Boundary:	$ 0000	$ 0000
	Mbyte	Mbyte

Access Address Selection: Example 1 using one DRAM-E4S12

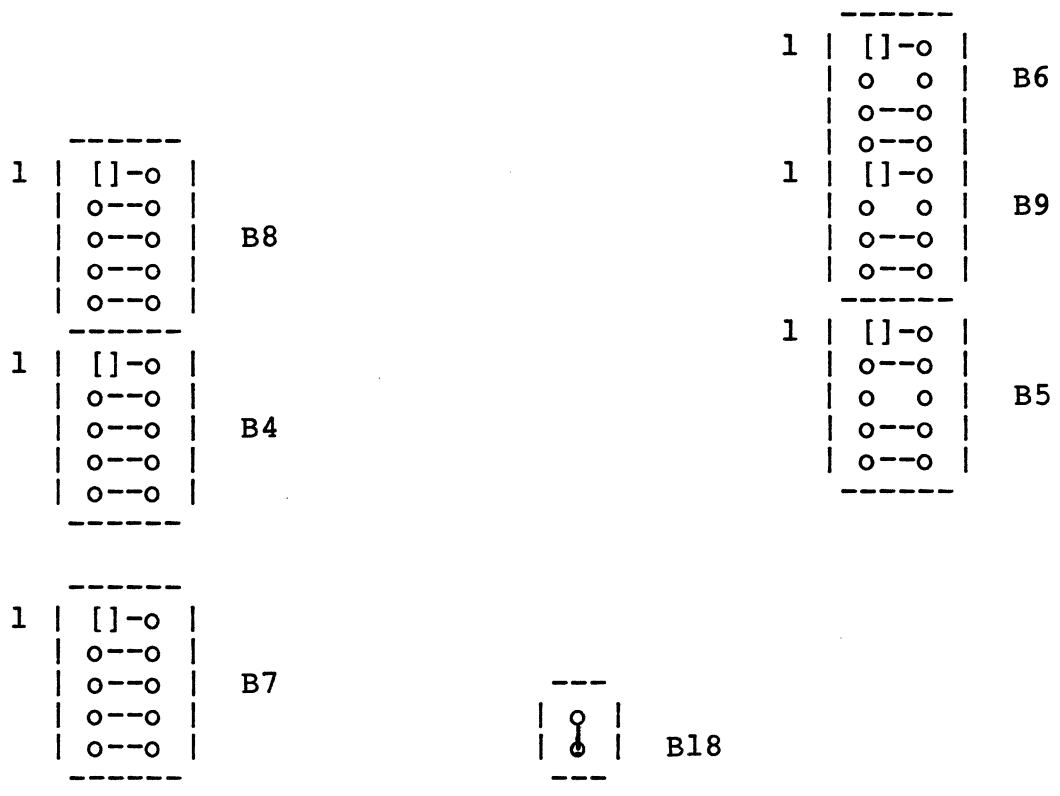
Jumper B18 must be inserted. (Mode A32)

Start Address			First not on-board Address			Corresponding Bus Address Signal	
B7	B8	B9	B4	B5	B6		HEX
1-10			1-10			A31	8
2-9			2-9			A30	4
3-8			3-8			A29	2
4-7			4-7			A28	1
5-6			5-6			A27	8
	1-10			1-10		A26	4
	2-9			2-9		A25	2
	3-8					A24	1
	4-7			4-7		A23	8
	5-6			5-6		A22	4
		1-8			1-8	A21	2
						A20	1
		3-6			3-6	A19	8
		4-5			4-5	A18	4

	A32	A24
Start Address:	$0010 0000	
End Address:	$010F FFFF	
First not on-board Address:	$0110 0000	
Boundary:	$0100 0000	
	16M byte	

Access Address Selection: Example 1 using one DRAM-E4S12

Mode: A32



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$0010 0000	
End Address:	$010F FFFF	
First Not On-board Address:	$0110 0000	
Boundary:	$ 100 0000	
	16Mbyte	

Access Address Selection USER using one DRAM-E4S12

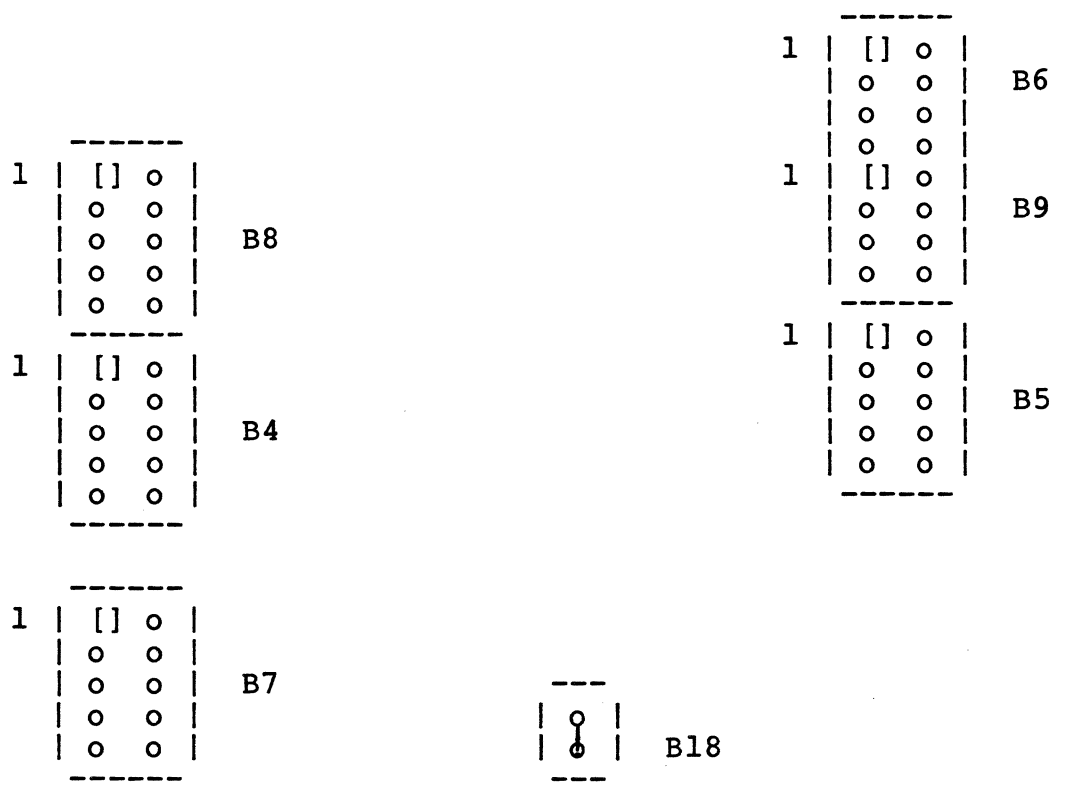
Jumper B18 must be inserted. (Mode A32)

Start Address			First not on-board Address			Corresponding Bus Address Signal	
B7	B8	B9	B4	B5	B6		HEX
						A31	8
						A30	4
						A29	2
						A28	1
						A27	8
						A26	4
						A25	2
						A24	1
						A23	8
						A22	4
						A21	2
						A20	1
						A19	8
						A18	4

	A32	A24
Start Address:	$ 0000	
End Address:	$ FFFF	
First not on-board Address:	$ 0000	
Boundary:	$ 100 0000	
	16M byte	

Access Address Selection: Example USER using one DRAM-E4S12

Mode: A32



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$ 0000	
End Address:	$ FFFF	
First Not On-board Address:	$ 0000	
Boundary:	$ 100 0000	
	16Mbyte	

Access Address Selection Example 2 using two DRAM-E4S12 Boards

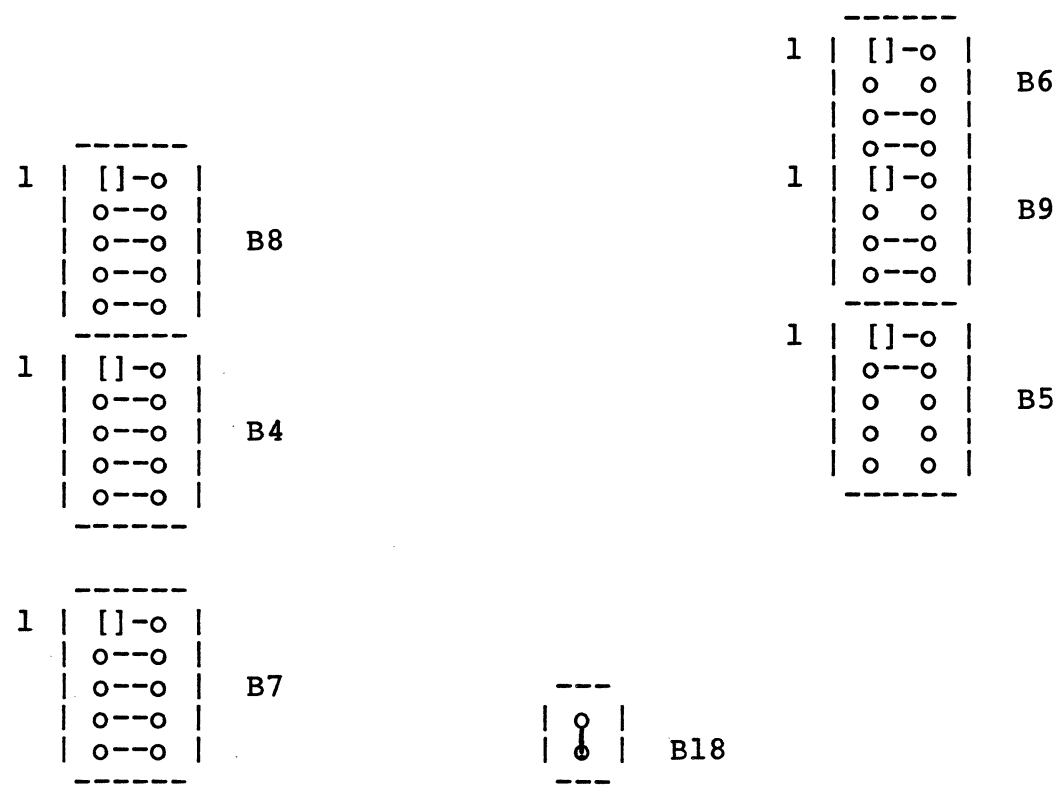
Jumper B18 must be inserted (Mode A32)

Start Address			First not on-board Address			Corresponding Bus Address Signal	
B7	B8	B9	B4	B5	B6		HEX
1-10			1-10			A31	8
2-9			2-9			A30	4
3-8			3-8			A29	2
4-7			4-7			A28	1
5-6			5-6			A27	8
	1-10			1-10		A26	4
	2-9			2-9		A25	2
	3-8					A24	1
	4-7					A23	8
	5-6					A22	4
		1-8			1-8	A21	2
						A20	1
		3-6			3-6	A19	8
		4-5			4-5	A18	4

	A32	A24
Start Address:	$0010 0000	
End Address:	$01CF FFFF	
First not on-board Address:	$01D0 0000	
Boundary:	$ 1C0 0000	
	29M byte	

Access Address Selection: Example 2 using two DRAM-E4S12

Mode: A32



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$0010 0000	
End Address:	$01CF FFFF	
First Not On-board Address:	$01D0 0000	
Boundary:	$ 1C0 0000	
	29Mbyte	

Access Address Selection USER using two DRAM-E4S12 Boards

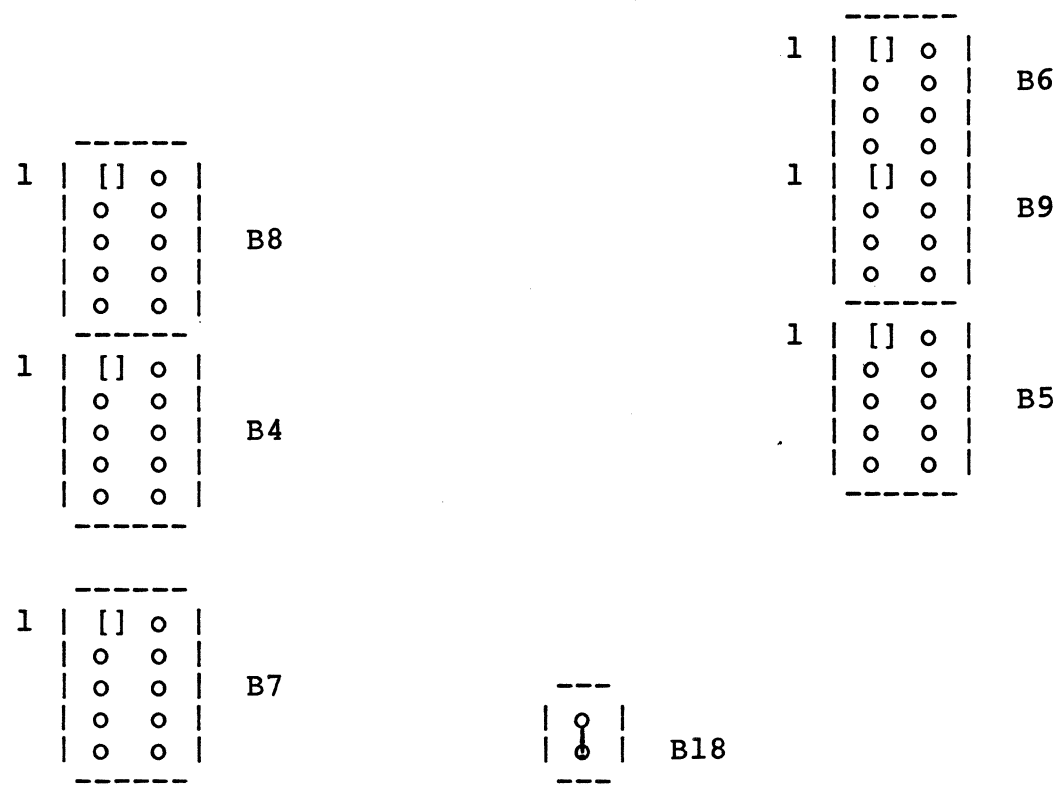
Jumper B18 must be inserted (Mode A32)

Start Address			First not on-board Address			Corresponding Bus Address Signal	
B7	B8	B9	B4	B5	B6		HEX
						A31	8
						A30	4
						A29	2
						A28	1
						A27	8
						A26	4
						A25	2
						A24	1
						A23	8
						A22	4
						A21	2
						A20	1
						A19	8
						A18	4

	A32	A24
Start Address:	$ 0000	
End Address:	$ FFFF	
First not on-board Address:	$ 0000	
Boundary:	$ 1C0 0000	
	29M byte	

Access Address Selection: Example USER using two DRAM-E4S12

Mode: A32

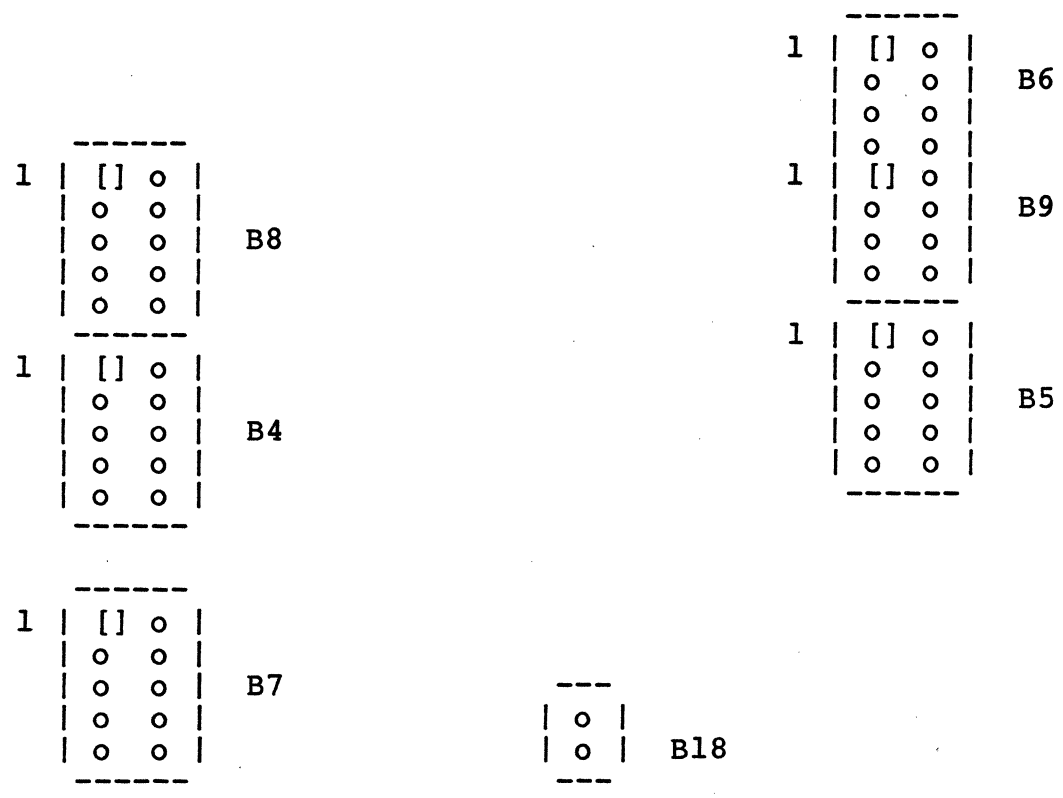


Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$ 0000	
End Address:	$ FFFF	
First Not On-board Address:	$ 0000	
Boundary:	$ 1C0 0000	
	29Mbyte	

Access Address Selection Example

Mode:



Start Address : Jumper B7, B8, B9
End Address + 1: Jumper B4, B5, B6
Address Mode: Jumper B18

	A32	A24
Start Address:	$ 0000	$ 0000
End Address:	$ FFFF	$ FFFF
First Not On-board Address:	$ 0000	$ 0000
Boundary:	$ 0000	$ 0000
	Mbyte	Mbyte

Access Address Selection

Start Address			First not on-board Address			Corresponding Bus Address Signal
B7	B8	B9	B4	B5	B6	
						A31
						A30
						A29
						A28
						A27
						A26
						A25
						A24
						A23
						A22
						A21
						A20
						A19
						A18

	A32	A24
Start Address:	$	$
End Address:	$	$
First not on-board Address:	$	$
Boundary:	$	$
	1M byte	1M byte