GE PAC® 4000

SYSTEMS MANUAL

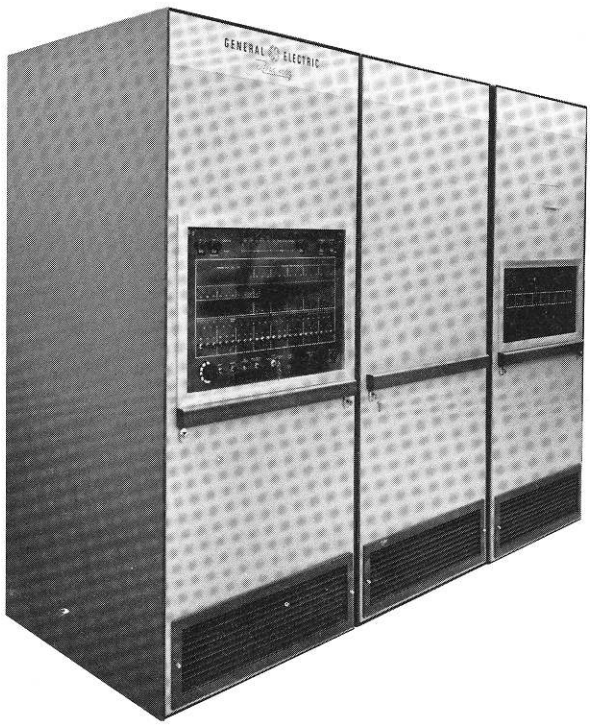
GENERAL ELECTRIC

PROCESS COMPUTER BUSINESS SECTION

PHOENIX, ARIZONA

GEPAC® 4000

SYSTEMS MANUAL



CONTENTS

CONTENTS (CONTINUED)

I GENERAL DESCRIPTION

INTRODUCTION

The GE/PAC 4000 is a digital computer system which has been designed to meet the on-line computing requirements of the process industries. The name, GE/PAC, stands for General Electric Process Automation Computer. The number assignment, 4000, designates the family of computer modules that can be organized into many configurations to meet a wide variety of applications. Specific configurations have been given family member designations, such as, GE/PAC 4040, GE/PAC 4050, and GE/PAC 4060.

The application areas of GE/PAC 4000 are many and varied, and the process industries that are beginning to apply process computers are growing rapidly. Some of the industries that already have installed process computers are steel, cement, paper, chemical, petroleum, railroads, and electric utilities. Applications vary from data acquisition systems to closed-loop control.

Benefits that users derive are also many and varied; however, they can be summarized as increased production, reduced operating costs, improved quality, safer operation, and greater management control.

GE/PAC 4000 is a major part of a wide range of industrial automation equipment that General Electric, as a single supplier, offers users. Along with the GE/PAC 4000, the following equipment is offered (all of which are compatible with GE/PAC 4000):

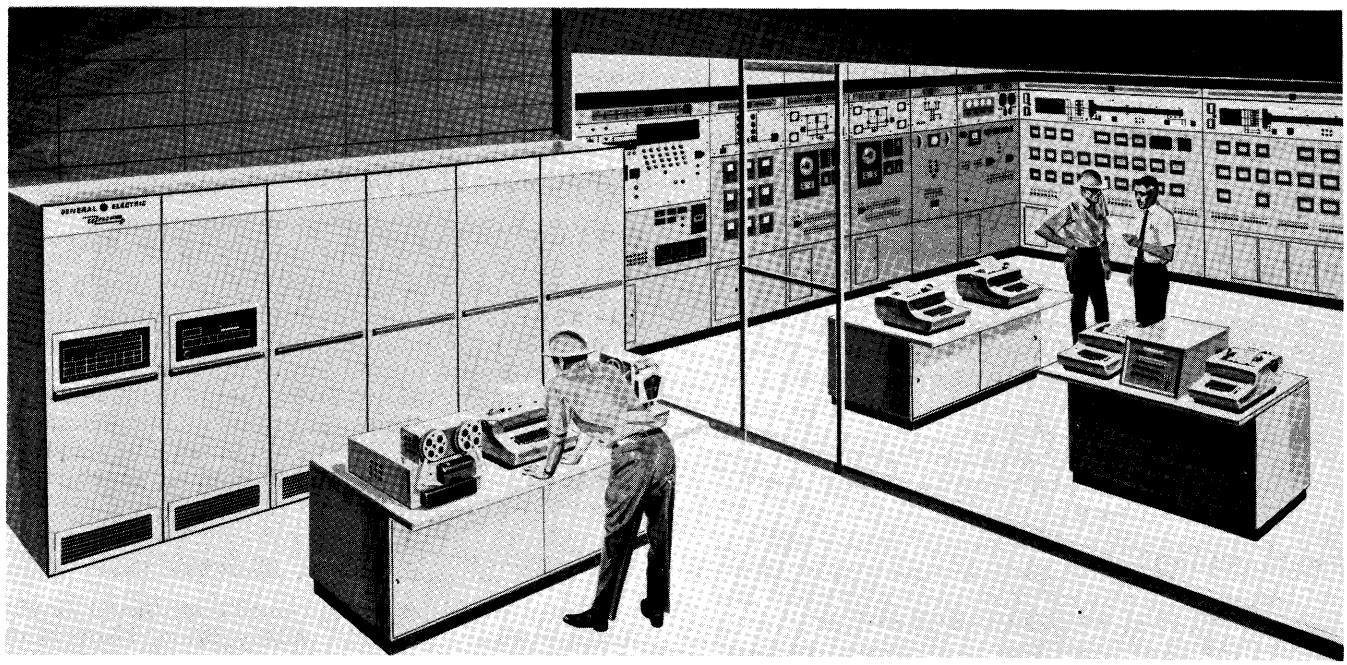


Figure 1. GE/PAC 4060 System

- Directo-Matic ® II Control
  Wired program modules for industrial control
  GE/PAC and Directo-Matic II are combined for IPC (Integrated Process Control)
- GE/MAC (General Electric Measurement And Control)
  Industrial instrumentation systems
- GE/TAC (General Electric Telemetering And Control)
- X-Ray Equipment
  On-stream analysis of chemicals
- Computer Peripherals
  Common use of peripherals between process and business computers.

GE/PAC 4000 SYSTEM FEATURES - SUMMARY

SOLID STATE - silicon transistors and diodes

OPERATING TEMPERATURE RANGE - 32 to 131 F without air conditioning

PARITY CHECKS - automatic audit of words in core memory, drum memory, and peripheral input/output

COMPACT PACKAGING

CENTRAL PROCESSOR

- Magnetic core memory
- 1.7 and 5.1 microsecond cycle times (read and write)
- 1028 to 65,536 words of core
- Magnetic drum backup memory
- 8192 to 262,144 words of drum
- Automatic Program Interrupts (API) - up to 128 (as hardware modules)
- Arithmetic unit
  Two models:
  Serial — AU 1
  Parallel — AU 2
- 7 index words in core memory

INPUT/OUTPUT

- Analog inputs - up to 148 points per second
- Digital inputs - 600,000 contacts per second
- Analog and digital outputs - 4000 outputs per second
- Peripheral Input/output
  Paper-tape read and punch, typewriters, consoles, magnetic tape, card I/O, high-speed printers, discs

PROGRAMMING

- Fixed-point and floating-point arithmetic
- Relative addressing
- Relocatable programs in core
- Bit logic operation (set, reset, and test individual bits)
- List operations
- Repeat instruction (for loop control)
- Partial-word arithmetic operation
- Accumulate into any memory location
- Software package:
  Assembler
  FORTRAN II
  MONITOR
  Mathematics subroutines
  Debugging aids

THREE SYSTEMS: GE/PAC 4040, GE/PAC 4050, GE/PAC 4060

The family of GE/PAC 4000 modules has been identified by grouping specific configurations and designating them the GE/PAC 4040, the GE/PAC 4050, and the GE/PAC 4060.

GE/PAC 4040 SYSTEM

This configuration is identified by the use of the 5-microsecond core-memory cycle (model 4010 or 4011) and the serial arithmetic unit (AU 1).

GE/PAC 4050-II SYSTEM

This configuration is identified by the use of the 3.4-microsecond core-memory cycle (models 4010, 4011 or 4013) and the parallel arithmetic unit (AU 2).

GE/PAC 4060 SYSTEM

This configuration is identified by the use of the 1.7 and 2.38-microsecond core-memory cycle (models 4012 and 4014) and the parallel arithmetic unit (AU 2).

The features of each computer can be readily determined by a reference to the features of the core memory and arithmetic unit descriptions contained in this manual.

GE/PAC 4000 FEATURES

ENVIRONMENT

All GE/PAC 4000 modules will operate in 0-55 C (32-131 F) ambient temperature range (without air conditioning), including the core memory which uses a temperature-controlled core stack, and operates over a humidity range of 5-95%. The GE/PAC 4000 system is also adequately protected against industrial hazards such as dust, shock, vibration, etc., and may be provided with ducted air in highly corrosive atmospheres.

POWER REQUIREMENTS

The power supply requirements for the GE/PAC 4000 system are 230 volts, single phase, 3-wire with grounded neutral, 60 cycles, with permitted voltage variation of ±10% and frequency variation of ±1 cycle per second (option ±3%, -7% transient for 10-15 seconds). Optional 50-cycle systems are available. Power requirements vary from 1 to 1.5 KW for a small system including blower power and up to 4 to 10 KW for a large system.

CIRCUITS

The logic circuits in GE/PAC 4000 utilize silicon semiconductors for high temperature capability and proved reliability. Circuit temperature capability is 0-70 C providing for a 15 C rise within the cabinet to meet the 55 C ambient specifications. Basic NAND logic is used, and the circuit design allows use of diodes for gates instead of transistors. Diode logic aids in reducing the total number of transistors and other components in a system with consequent high reliability.

Compatible 3 MC, 300 KC, and 20 KC logic circuit families permit using the circuit whose speed best suits a given module's requirements. These differ for various modules depending on the speed of operation and noise susceptibility. The wide choice of available circuit boards enhances the flexibility of the system in meeting a wide variety of applications. Logic is designed for operation within specifications when all varying parameters are at the most unfavorable limit of their tolerance at the same time. This is known as "worst case" design and contributes to high reliability.

PACKAGING

Printed circuit boards have a copper laminate for ground plane on one side and are coated to resist moisture and contamination in industrial environments (see Figure 2). Use of proved flow soldering and vertical component mounting techniques with wire wrapping on back panels provides high reliability and low maintenance expense. Optimized combinations of flip-flops, gates, and other circuits on the board contribute to a minimum number of components. Some components on the board are mounted on end with the lead on the high end of the component brought back through the board for soldering and to give support to the component. All boards are marked with an easily understood designation for ease of identification. The boards have provision for 51-pin terminations which fit securely in the receptacle. The receptacle also has provision for labeling the designation of the board it holds. Circuit boards are 5.4" x 4" with maximum component height of 3/4".

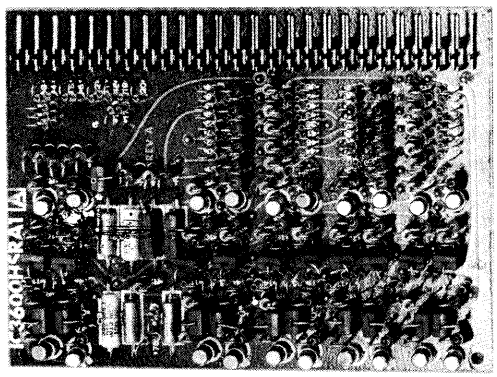


Figure 2. Printed wiring board provides higher packing density of components, cuts space. Use of glass epoxy material with special coating contributes to GE/PAC availability.

The circuit board receptacle containing 17 cards is molded Lexan* to provide high strength and rigid support for printed circuit boards. The card guides are integrally molded in the board receptacle structure with cards spaced on 1" centers. Lexan's high strength and nonfracturability guard against malformation of the board receptacle, which in turn protects the boards.

The back panel is fitted to the number of card rows required for the particular module. Modules can thus be assembled, wired, and tested in the factory before mounting in the cabinet. The availability of pre-wired assemblies makes it feasible to supply initially only the portion of the system required, with provision for future expansion in the field.

The GE/PAC 4000 cabinet consists of an enclosure of steel which mounts against the wall with all customer terminations and certain components, such as power supplies, mounted on the interior back and left side wall of the cabinet (see Figure 3).

The electronic portion of the system is mounted in frames (or pages) which contain 10 card holders of 17 cards each. They can also accommodate 19" relay racks or certain specially-mounted devices. These frames are installed similar to book pages on a roll-out assembly which is wheeled (on 4" wheels) into the cabinet enclosure. The outer two pages are hinged at the back to permit access to both sides and to the fixed center page and to facilitate short lead lengths to terminal boards on the fixed page. Certain devices, such as the computer console and display lamps, are mounted on the front panel which is rigidly supported by the assembly base and the fixed center page.

The matrix relays for the analog scanner and customer terminations are mounted on the back or left side wall of the cabinet for single-cabinet systems. They are accommodated in groups of 8 or 16 by a basic mounting block which accepts 8 or 16 customer terminations (2 or 3 wire) up to #12 conductor and plug-in capability for 16 two or three-wire switching and 16 signal-conditioning elements. The mounting module contains an additional relay for matrix switching to provide isolation of the individual matrix.

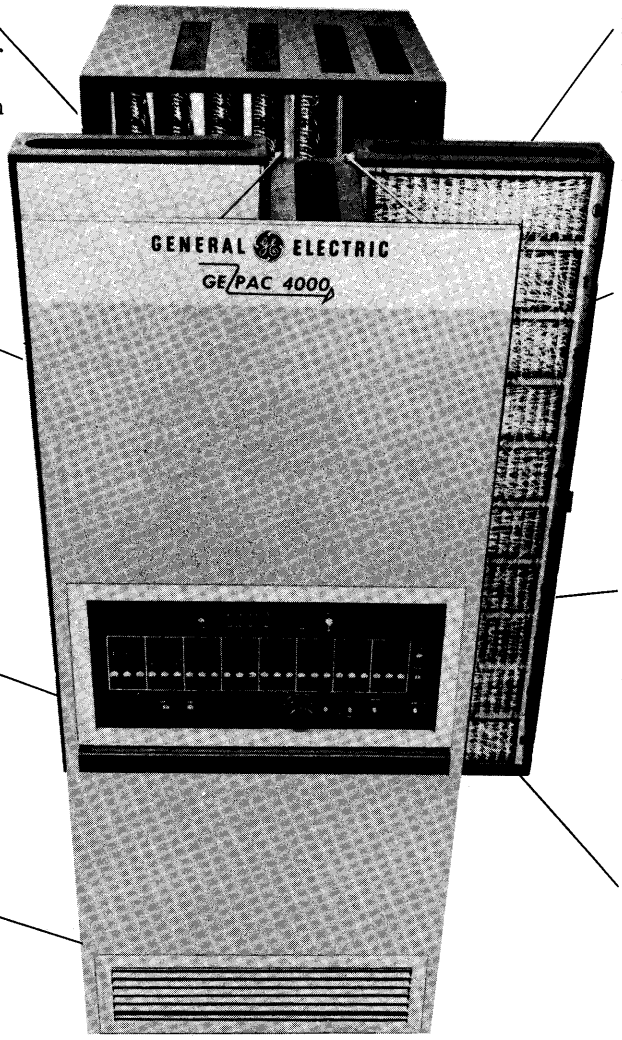
*Registered trademark of General Electric Company.

FIELD TERMINATIONS — are located at the inside rear of the cabinet. With the assembly rolled out, a man can walk into the cabinet. Back panel terminations are connected to functional modules on the assembly by wiring ribbon through an expandable rack.

INDUSTRIAL CONSTRUCTION — sturdy, yet lightweight unit is built to withstand a wide range of environments. Small systems in a single cabinet (32" wide x 36" deep x 76" high) save space. The cabinet meets NEMA I standards for industrial use.

ROLL-OUT ASSEMBLY — draws out of cabinet easily by lifting the front-mounted handle and pulling. A track at the bottom of the cabinet guides the assembly and locks it when fully open.

BLOWER AND VENTILATION SYSTEM — Internal air flow through vent in front, in and around pages of components, and out the top eliminates need for special cooling in applications up to 131 F.



HINGED PAGES — All components are mounted on three pages, two hinged on either side of a stationary center one. This provides easy access to all components. Test points on back of each page facilitate check-out and troubleshooting.

MODULAR FUNCTIONS — Each function to be performed is supplied in a standard functional module. This permits selection of only those functions you initially need, yet incorporates ease of expanding as your automation requirements grow.

PRINTED WIRING BOARDS — Boards are mounted in 10 rows of 17 cards per row in frames on each page. Each board slides in and is connected by stab-on connectors. Interconnection between boards is on the back of each page.

SILICON DIODES AND TRANSISTORS — Power consumption is cut, temperature operating range is increased by the use of silicon semiconductors throughout. GE/PAC operates reliably at ambient temperatures from 32 to 131 F.

Figure 3.

Air circulation for cooling of the circuit components is provided from a blower mounted in a plenum in the assembly base. The blower supplies about 200 CFM to each page frame.

Air enters through grillwork in the front of the cabinet, passes through the page frames and out through a drip-proof exit in the top of the cabinet. A certain portion (about 100 CFM) of the air in the base is diverted to the left to cool electronic devices which are mounted on the inside cabinet walls.

This cabinet and assembly design has several advantages. It provides front access to all system components, saving floor space normally needed for a rear aisle. It allows easy access to all components after simply withdrawing the assembly and either opening the page frames or by entering the cabinet to reach terminations, power supplies, or other devices mounted on the wall. The cabinet dimensions are 32" wide by 36" deep by 76" high, providing ample working space. Cables which must go from the cabinet wall over to the roll-out assembly use a multiconductor belt or ribbon which is flexible horizontally. These multiconductor ribbons fold up when the assembly is recessed in the cabinet. They are close to and parallel to the right side of the cabinet to permit unobstructed entry by personnel into the cabinet when the assembly is withdrawn.

II CENTRAL PROCESSOR

The GE/PAC 4000 central processor includes the following major functional units:

- High-speed magnetic core memory which provides random access storage for data and programs
- Arithmetic unit which provides control and execution of stored program instructions
- Programming and maintenance console

CORE MEMORY

The high-speed core memory utilizes a 24-bit (binary digits) word size. Parity is automatically generated for each word written into memory and checked as each word is read from memory. It consists of a temperature-controlled core stack (allowing operation of ambient temperatures from 32 to 131 F), a Memory-Data Register (MDR), a Memory-Address Register (MAR), and a parity generate and check circuit. These functional components communicate with the arithmetic and control unit and other memory-access devices such as the drum controller.

Another feature of the core memory is the preservation of memory upon detection of a power failure. When power fails, the memory logic completes its present cycle and all current sources are shunted to ground via self-latching electronic switches which remains in a latched condition until all current sources decay to a safe value. When power is restored, the program can be reinitialized from the programmer's console without having to reload the core memory with the program. The program is restarted at a predetermined initialization point. As an optional feature, automatic program restart when power is restored can be provided.

There are four options available as part of the core memory. They are:

1. Memory size option
2. Memory speed option
3. Automatic Program Load Option
4. Memory Multiplexer Option

MEMORY SIZE OPTION

	Capacity - words
Model 4010	1024 to 4096
Model 4011	4096 to 16,384
Model 4012	4096 to 16,384
Model 4013	8192 to 49,152 (expansion beyond 16K)
Model 4014	8192 to 49,152 (expansion beyond 16K)

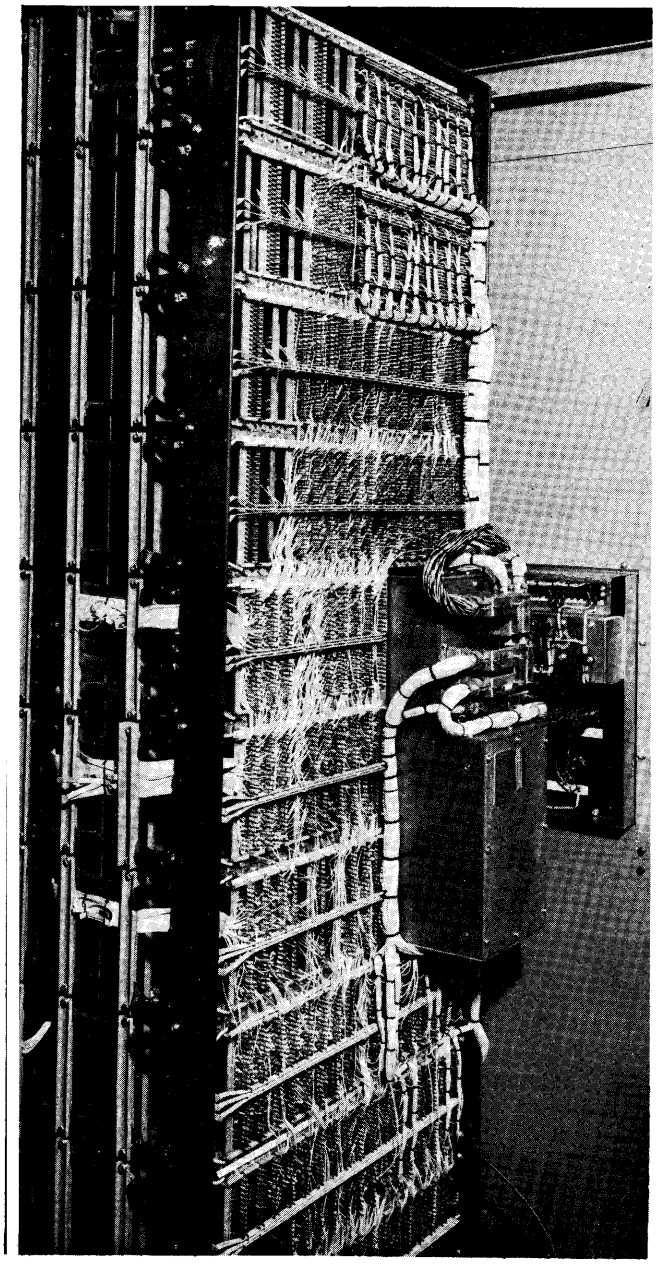


Figure 4. Core Memory

MEMORY SPEED OPTION

	Memory Cycle (read & write)	
Model 4010	5	microseconds (GE/PAC 4040)
Model 4011B	5.1	microseconds (GE/PAC 4050-I)
Model 4011C	3.4	microseconds (GE/PAC 4050-II)
Model 4012	1.7	microseconds (GE/PAC 4060)
Model 4013	4.08	microseconds (GE/PAC 4050-I)
Model 4013	4.08	microseconds (GE/PAC 4050-II)
Model 4014	2.38	microseconds (GE/PAC 4060)

Times for devices other than the arithmetic unit communicating with main or extended memory via the extended memory multiplexer adapter will be slightly longer than above.

AUTOMATIC PROGRAM LOAD OPTION

As an optional feature of the core memory, a pushbutton start-up may be included whereby location zero and consecutive core addresses from octal 001 through octal 033 is made to contain a bootstrap loader program. The bootstrap loader program is stored automatically in memory upon manual activation of a pushbutton switch located on the console.

The loader program being read-in by the bootstrap loader can come from either a paper-tape reader or from the magnetic drum.

MEMORY MULTIPLEXER OPTION

The Memory Multiplexer Option expands the memory's input/output capability from one channel to three (4010, 4011) or four (4012) channels. The arithmetic unit always occupies one channel. An expansion to two or three channels is required in order to accommodate a magnetic drum or a controller for controlling peripherals such as magnetic tape or high-speed line printers. This is illustrated below:

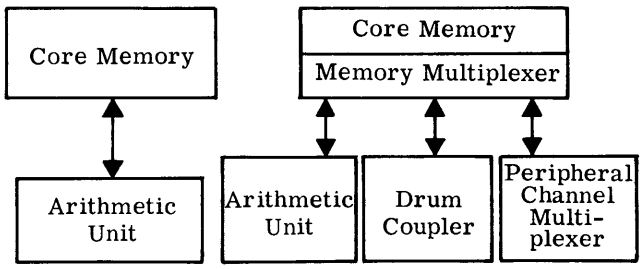


Figure 5.

MAGNETIC DRUM MEMORY

The magnetic drum auxiliary memory provides non-destructive bulk storage. The drum controller contains the necessary read-write amplifiers and control logic to enable reading and writing on the continuously rotating magnetic surface. During transfer to or from the drum, the 4060 central processor continues to execute programs at better than 97% of normal speed.

The drum controller and drum coupler are used to control two-way flow of data from drum directly to memory without disrupting operation of the arithmetic unit (see Figure 6). The transfer is in blocks of from one to 16K words by one instruction at a rate of over 15,000 words per second.

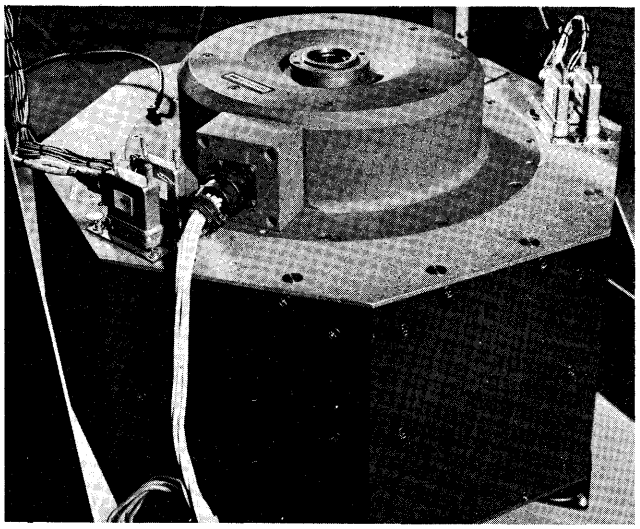


Figure 6. Magnetic Drum Memory

Drum storage capacity varies from 16,384 words to 262,144 words in increments of 8192. A parity bit is generated or verified as a result of transferring words to or from the drum. Write disable switches prevent drum tracks from being inadvertently destroyed.

ARITHMETIC UNIT

The purpose of the arithmetic unit is to perform the basic functions of add, subtract, multiply, divide, logical operations, and control for the input/output of data. It communicates directly with the core memory for the storing and retrieval of instructions and data. It controls the flow of data for analog input/output, digital input/output, console input/output, peripheral input/output, and automatic priority interrupts. These communication channels are illustrated in Figure 9.

There are two arithmetic units, known as the AU 1 and the AU 2. Basically, the AU 1 is characterized by serial internal transfer of bits, while the AU 2 is characterized by parallel internal transfer

of bits. The AU 1 is basic to the GE/PAC 4040 (with a 5-microsecond memory cycle), while the AU 2 is fundamental to the GE/PAC 4050 (with a 5.1 or 3.4 microsecond memory cycle) and the GE/PAC 4060 (with a 1.7-microsecond memory cycle).

The registers associated with the arithmetic units are as follows:

REGISTERS

A - Accumulator - 24 bits

Q - Auxiliary accumulator - 24 bits

(The Q register is implemented by a word in core memory for Arithmetic Unit 1 which is associated with GE/PAC 4040.)

P - Place counter - 14 bits (AU 1)
- 16 bits (AU 2)

I - Instruction register - 24 bits (AU 1)
- 26 bits (AU 2)

B - Memory buffer - 24 bits

J - Counter for use with logic commands - 5 bits

X - Index words, core memory locations 1-7

FEATURES OF THE ARITHMETIC UNIT 1 (for (GE/PAC 4040)

- Serial internal bit transfer
- Word size - 24 bits plus parity
- 5-microsecond memory cycle (read and write)
- Core memory addressing - 1024 words to 16,384 words
- Relative addressing
  Capability of addressing relative to the place counter. Programs entering core from drum or paper tape that are tagged for relative addressing can be located in any available core area.
- Extended function commands
  Provides automatic entry and exit linkage to subroutine implemented instructions, i.e., floating-point operations, list operation, multiply, divide, etc.
- Logic capability
  Use of bit logic operations which permits many operations on individual bits in the accumulator register.
- Test flip-flop
  Used to make logical tests on which the program can branch. Logic decision making is a large part of a process computer program.
- Instruction timing examples
  Add - 16 microseconds, non-indexed
  22 microseconds, indexed
  Full Shift - 16 microseconds
  (See instruction list for complete timing)
- Input/Output channels
  3 plus one for programming console can be expanded to 5, 7, or 9 by use of I/O buffer.

FEATURES OF THE ARITHMETIC UNIT 2 (for GE/PAC 4050 and GE/PAC 4060)

- Parallel internal bit transfer
- Word size - 24 bits plus parity
- 1.7, 3.4, or 5.1-microsecond memory cycle (read and write 2.38 or 4.08 for memory beyond 16,000 words) (depending upon which core memory module is used)
- Core memory addressing - 4096 words to 65,536 words
- Relative addressing
  (same as AU 1)
- Indirect addressing capability
- Logic capability
  (same as AU 1)
- Test flip-flop
  (same as AU 1)
- Four fixed-point modes of arithmetic operation: single, double, partial and variable-register arithmetic
  Partial word - 14 bits
  Single word - 24 bits
  Double word - 48 bits
- Floating-point operation - 2 formats
  - 24 bits for process applications
  - 48 bit for extremely accurate requirements
- List techniques - provide for stacking, circular listing, and real-time queuing lists with list full or empty conditional branches.
- Memory protect - under hardware control stores to certain parts of memory are inhibited. Also provides "branch protect" and "I/O protect" features.
- Eight input/output channels to arithmetic unit. Input/output instructions which permit direct memory communication under program control.
- Every memory location may be treated as an accumulator.
  Subroutine linkage instructions - one instruction saves all index words and accumulator in memory.
- Any memory location acts as event or time counter for direct-memory counting.
- Repeat instruction provides for single-instruction loop control.
- Instruction timing examples (1.7 microsecond memory)

  Fixed-point arithmetic

Add	3.4	microseconds
Multiply (24 x 24 bits)	16	microseconds
Divide (48 ÷ 24 bits)	28	microseconds

  Floating-point arithmetic - single word
  1 sign bit
  6 bit characteristic
  17 bit mantissa

Floating add	92 microseconds
Floating multiply	109 microseconds
Floating divide	141 microseconds

  (see instruction list for complete timing)
  (see programming section for instruction definitions)

SPECIAL FEATURES FOR PROCESS CONTROL

AUTOMATIC PROGRAM INTERRUPTS

The feature of automatic program interrupt (API) permits immediate execution of priority functions. It allows the computer system to keep under constant surveillance critical points in a process without consuming computer time by constantly scanning the points. Certain phases of a process may occur at random, and it is important that the computer immediately recognize the occurrence, promptly taking whatever action may be required.

The basic module in GE/PAC contains eight API's with optional expansion to 128 in groups of eight. By combining change detection input signals to the API, the effective number of API's can be expanded to several hundred or even more if required. The interrupt signals are connected to detection flip-flops within GE/PAC. The API module is connected to the GE/PAC system via the arithmetic unit. The interrupt module is continually searching for interrupts. The total search time for eight interrupts is approximately 8 microseconds.

By means of the interrupt module and the decrement memory and test (DMT) instruction, the API in GE/PAC can serve the functions of pulse counting and accumulation and elapsed time counting. The major classifications of API inputs become:

1. Cycles timer pulse input
2. Pulses (from process plant devices)
3. Process alarms
4. Peripherals ready (See Figure 18)

DYNAMIC PRIORITY CONTROL OF AUTOMATIC PROGRAM INTERRUPT

The capability exists within the automatic program interrupt feature of GE/PAC to establish what is known as "Dynamic Priority Control". This enables the internally stored program logic to permit or inhibit either individual API's or groups of eight API's according to a masking word contained within the core storage. This allows dynamic enabling/disabling of API's that effectively changes the priority sequencing of the inputs to the API module. Thus, GE/PAC can adjust to the changing environment of the process being controlled.

CYCLES TIMER FOR CLOCK IN MEMORY

This timer produces a level signal once each cycle (normally the line frequency is used as reference) which is used to cause an automatic-priority interrupt to operate. Normally (with 60-cycle reference), interrupt number 1 is connected to this cycle source causing a counting down from 59 to zero, using the DMT (Decrement Memory and Test) instruction. When zero count appears, one second has elapsed and an echo signal is generated. The echo is normally used as an input to another interrupt which directs the computer to the program which keeps track of seconds, minutes, and hours, stores the 24-hour clock reading, and resets the cycle word to 59. If more than a cycle has occurred before the echo interrupt is permitted, the count will be negative in the cycle word. This value must then be subtracted from 59 prior to setting the word for the next count of one second (see Figure 18).

MEMORY PROTECT FOR ON-LINE DEBUGGING

The purpose of the Memory Protect feature is to perform on-line debugging without causing possible damage to operating programs. This is a hardware feature available as an option in the GE/PAC 4050 and 4060 systems. Memory Protect provides the capability of restricting access to designated areas of core memory unless under direct control of the MONITOR program (see Section VII).

When Memory Protect is selected, there are three general classes of protection which may be independently enabled/disabled. They are:

1. Store Protect
2. Branch Protect
3. Input/Output Protect

When enabled, the Store Protect mode causes the arithmetic unit to compare the effective address of store types of instructions against the "fenced region addresses" as held in the Memory Fence Registers. If the operand address is illegal (in the protected area), the sequencing will inhibit the memory storage cycle and transfer program control to location 20_8. This location, 20_8, is an entrance point to MONITOR. MONITOR examines the instruction that has been "trapped" to determine if it can be safely executed. If it can, it will be executed under MONITOR control, but, if not, an indication will be typed out.

When enabled, the Branch Protect mode causes branch-type instructions to be inhibited and program control transferred to 20_8. The continuing sequence is similar to that described for Store Protect.

When enabled, the Input/Output Protect mode inhibits the execution of Input/Output type instructions and causes program control to be transferred to location 20_8. The continuing sequence is similar to that described for Store Protect.

The purpose, in each case, of transferring control to 20_8, is to permit the program being debugged to use the features of MONITOR or other programs as long as this can be done without endangering operational programs.

When Memory Protect is disabled, no restrictions are placed on Store, Branch, or Input/Output instructions.

PROGRAMMING AND MAINTENANCE CONSOLE

The programming and maintenance console (Figure 7) provides an indicating control center for the programmer and product service engineer. It permits manual control in contrast to automatic control. Manual control is used when initially loading the program into memory, to start program execution, to monitor the progress of the program, and occasionally to stop the program for maintenance and troubleshooting.

Figure 8 illustrates the operation and performance possible from this console. These functions are summarized as follows:

1. Power ON/OFF/INITIALIZE
2. Manual/Auto/Console Off
   Selects console operation to manual, automatic, or console off modes.

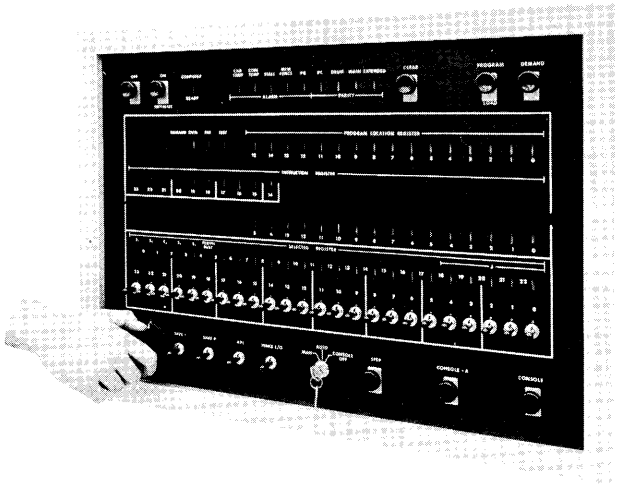


Figure 7. All necessary input and display devices are located on console in front of 4050/4060 central processors.

3. Step
   Step button steps computer one instruction or starts automatic sequencing.
4. Console - A Register
   A Register is set according to the corresponding program switch positions.
5. Clear A Register (to zeros)
6. Console - B Register
   B Register is set corresponding to program switch positions.
7. Demand
   Sets demand flip-flop which can be tested from the program.
8. Program Switches
   Twenty-four switches, corresponding to the register-bit positions, can be used to set ones in the A or B Register.
9. Register Select Switch
   The rotary switch shall select which register is displayed on the indicator lights, and is enabled in both the automatic and manual mode.
10. Clear Alarm
    Resets alarm flip-flops displayed via the indicator lights.
11. Save I Register
12. Save P Register
13. Program Load
14. API Lockout

INDICATOR LIGHTS

Alarms
- Temperature - cabinet
- Core Parity
- Peripheral Buffer Alarm
- Core Temperature
- Stall Alarm

Ready
- Peripheral
- Core
- Power

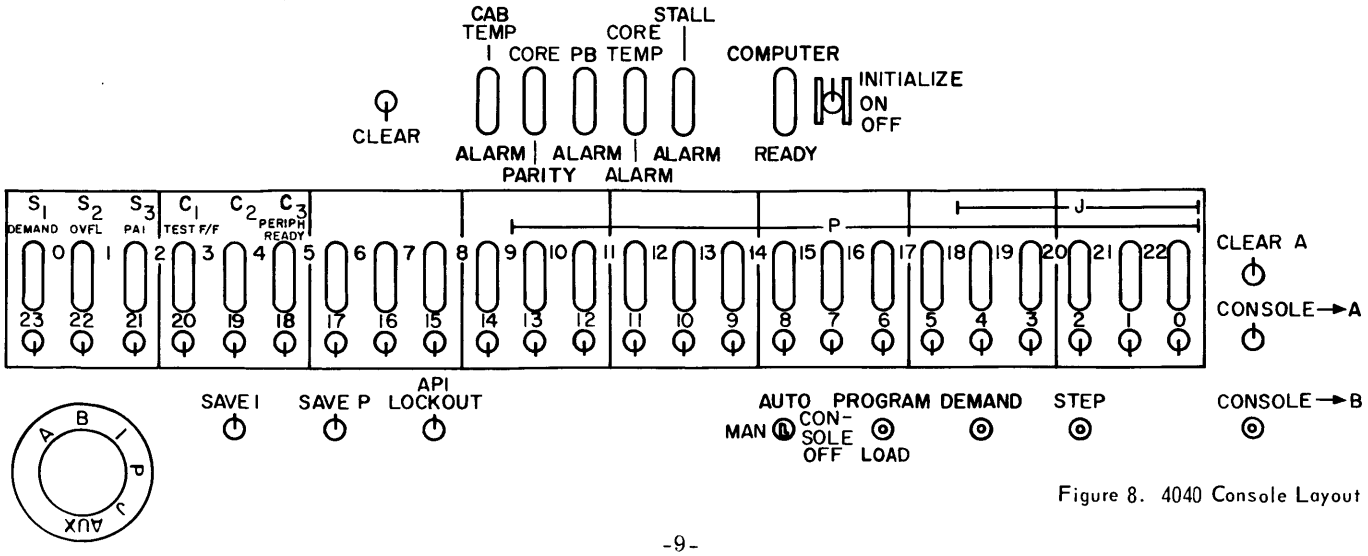


Figure 8. 4040 Console Layout

III PROCESS COMMUNICATIONS

Any instrument, sensor, or transducer with an electrical output can be used with GE/PAC systems. In addition, devices without an electrical output can be transduced to provide a suitable signal. A few common parameters and measuring devices that have been used as inputs are listed below:

Parameters	Devices
Temperature	Thermocouples
	RTD's
	Thermistors
	Pyrometers
Flow	Differential pressure transmitters
	Turbine meters
	Positive displacement meters
	Magnetic flowmeters
	Displacement-type meters
Pressure	Pressure transmitters (bourdon tubes, bellows slack diaphragm types, etc., with electronic or pneumatic outputs)
Liquid Level	Same as pressure
Speed	Tachometer generators
Composition	Chromatographs
	O_2 analyzers
	Infrared analyzers
Power	Thermal converters
	Watts/d-c transducers
Energy	Watthour meters (with contact device)
Weight	Load cells
Position	Many ways by use of a position to d-c transducer
Thickness	X-ray gages
	Beta-ray gages

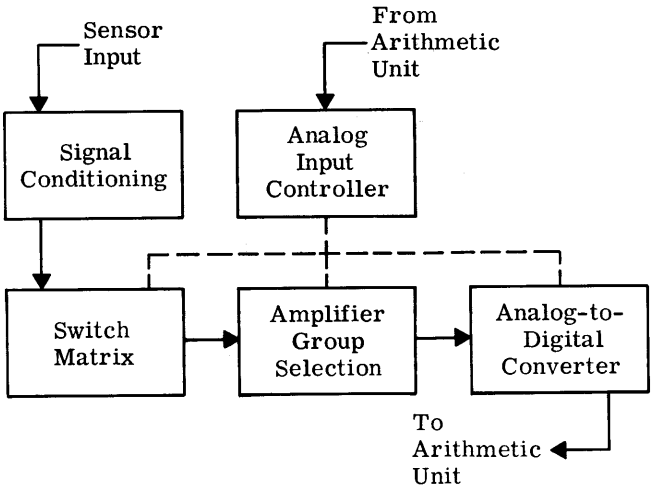
The term process communication refers to the continuous interrogation by scanning of process analog and digital inputs as well as periodically producing both analog and digital output signals as required. As can be seen in Figure 9, there are three major sections comprising process communication modules:

- Analog Inputs
- Digital Inputs
- Multiple Output
  - Analog signals
  - Latched relays
  - Timed relays

Also illustrated in Figure 9 is the fact that each of the above sections is separately controlled. This means that once given a control word, each section operates independently of the central processor as well as independently of the other input/outputs. For example, analog signals can be scanned at the same time that analog signals are being distributed or timed relay contacts can be closed at the same time that contact inputs are being scanned. Many other combinations are possible.

ANALOG INPUTS

The basic function of the analog input section is to convert input signals into equivalent binary digits. This is accomplished in several steps, namely, signal conditioning, selection, amplification, and analog-to-digital conversion. Under program control, a control word is selected and placed in the "T" register associated with the Analog Input Controller. This is illustrated below:



The functional specifications of each module illustrated above are as follows:

Analog Input Controller frees the central processor of time-consuming, low-order system control functions by providing full-buffered control of the point scan. The central processor has only to send a single control word to the input controller. The scan controller selects the proper point, gain setting, and timing to obtain the requested information. When the binary value of the measurement is available in the scanner "C" register, a ready signal is made available for testing by the central processor. The controller can select one of 256 inputs directly or one of 2048 inputs when used with group selection.

Signal Conditioning

This module provides signal filtering, fixed attenuation, milliamp to millivolt conversion, and RTD bridges within a standard module design.

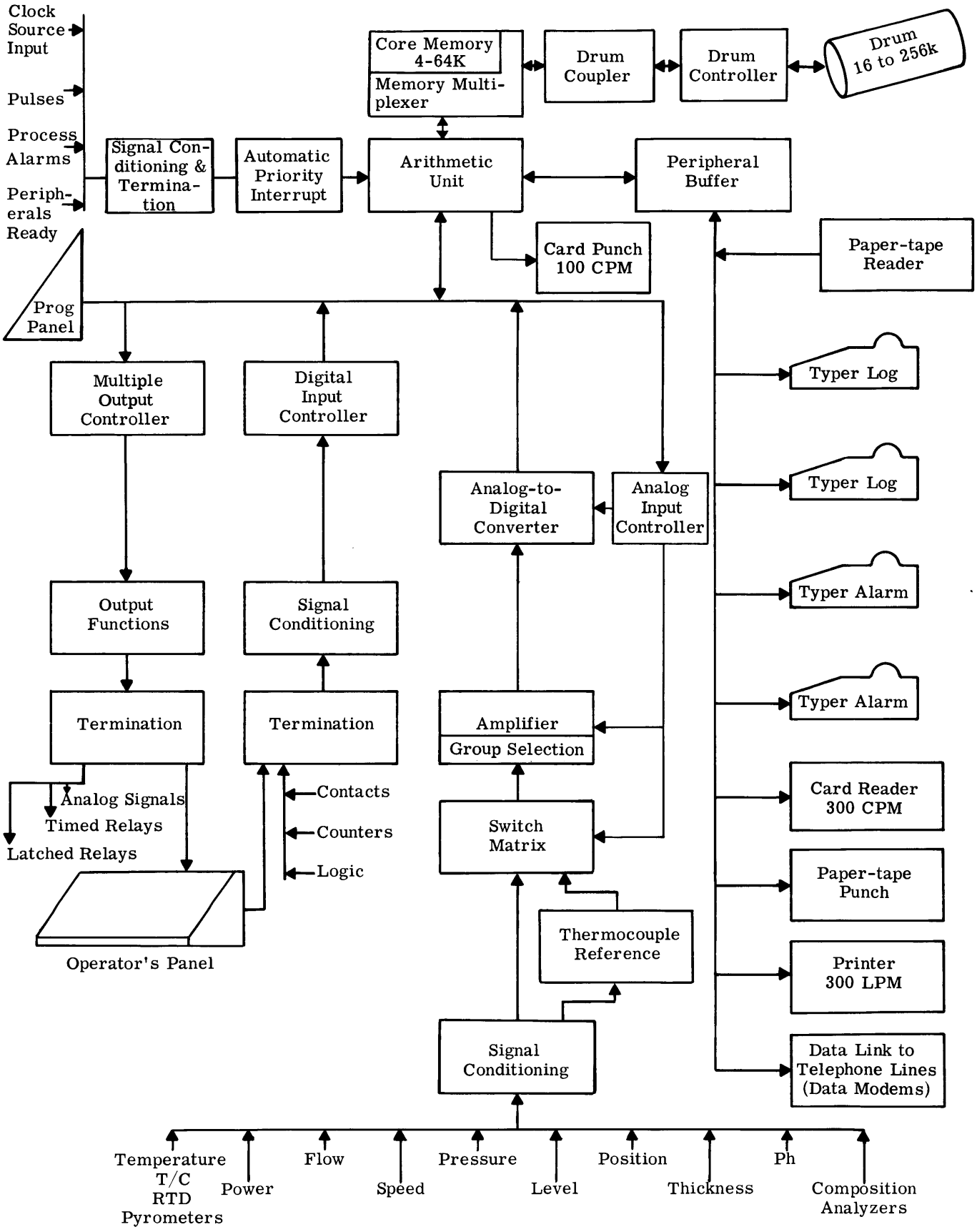

Clock Source Input
Pulses
Process Alarms
Peripherals Ready
Signal Conditioning & Termination
Automatic Priority Interrupt
Core Memory 4-64K
Memory Multiplexer
Drum Coupler
Drum Controller
Drum 16 to 256k
Arithmetic Unit
Peripheral Buffer
Card Punch 100 CPM
Paper-tape Reader
Prog Panel
Multiple Output Controller
Digital Input Controller
Typer Log
Typer Log
Analog-to-Digital Converter
Analog Input Controller
Typer Alarm
Output Functions
Signal Conditioning
Typer Alarm
Termination
Termination
Amplifier
Group Selection
Card Reader 300 CPM
Analog Signals
Timed Relays
Latched Relays
Contacts
Counters
Logic
Switch Matrix
Paper-tape Punch
Thermocouple Reference
Printer 300 LPM
Operator's Panel
Signal Conditioning
Data Link to Telephone Lines (Data Modems)
Temperature
T/C
RTD
Pyrometers
Power
Flow
Speed
Pressure
Level
Position
Thickness
Ph
Composition Analyzers

Figure 9.

Fixed Attenuation Ratios

1:1
10:1
50:1
625:1
6250:1

Maximum allowable input voltage is 500 volts.

Switch Matrix

Mercury-wetted reed switches are the standard switching device in 2-wire open termination and in 2 and 3-wire enclosed (guarded) termination. Mercury-wetted relay switching is available as an option in the 2 and 3-wire form in the enclosed (guarded) termination only.

Amplifiers

The amplifier scales selectable by program are —

Amplifier Scales

Low-order Bits of "T" Register			Low-level Amplifier	High-level Amplifier	Volt/ Frequency (Integrating) Converter
T_2	T_1	T_0			
0	0	0	10 mv	80 mv	10 mv
0	0	1	20 mv	160 mv	20 mv
0	1	0	40 mv	320 mv	40 mv
0	1	1	80 mv	640 mv	80 mv
1	0	0	160 mv	2.5 v	160 mv
1	0	1	10 v	10 v	320 mv
1	1	0	— —	— —	640 mv
1	1	1	— —	— —	1 v

Successive Approximation Analog-to-Digital Converter

Provides high-speed conversion to one part in 4000 of analog signals. The converted value is held in the "C" register as 12 counts, 1 sign, and 1 overflow.

INTEGRATING ANALOG-TO-DIGITAL CONVERTER is an alternate for applications where frequency measurement, a-c voltage signals, or integrated measurements are desired. The timing (16-2/3, 33-1/3, 100, and 1000 milliseconds) and input variable (a-c, d-c, and frequency) are program selectable. The converted value is held in the C register as 16 counts, 1 sign, and 1 overflow.

The input groups and scanning speeds for the overall analog input modules is as follows:

Groups

1 Group - 256 inputs maximum
2 Groups - 512 inputs maximum
4 Groups - 1024 inputs maximum
8 Groups - 2048 inputs maximum

Scanning Speed

Groups scanning speed for both mercury-wetted relays and mercury-wetted reed relays for the successive approximation A/D converter —

1 Group - 50 points/second
2 Groups - 90 points/second (optional)
4 Groups - 140 points/second (optional)
8 Groups - 200 points/second (optional)

For the integrating V/F converter —

For 16-2/3 millisecond cycle input - 30 points/second

For 33-1/3 millisecond cycle input - 20 points/second

Other times for counting events/unit time, counts are accumulated over 100 milliseconds or 1000 milliseconds.

Additional analog input modules shown in figure 9 are:

THERMOCOUPLE REFERENCE BLOCK provides reference for five thermocouple types. As many as 256 thermocouple inputs can be handled in one block. The reading error will be less than 1 F.

OPEN THERMOCOUPLE DETECTION provides thermocouple break detection for part or all of the thermocouples in a system.

DIGITAL INPUTS

The GE/PAC method of handling digital inputs is illustrated in Figure 9. A summary of the modules associated with digital scanning follows:

DIGITAL SIGNAL CONDITIONING enables the computer to read contacts representing process or operator-inserted information by applying a 28- or 125-volt d-c signal to a selected group of 20 contacts. The unit filters, shapes, and attenuates this signal to a +5 or 0-volt logic level. Contacts may represent coded (BCD, binary, decimal) or uncoded information.

DIGITAL INPUT CONTROLLER selects up to 64 groups of 20 inputs. Maximum input rate is 600,000 contacts per second.

MULTIPLE OUTPUTS (for outputting both analog and digital)

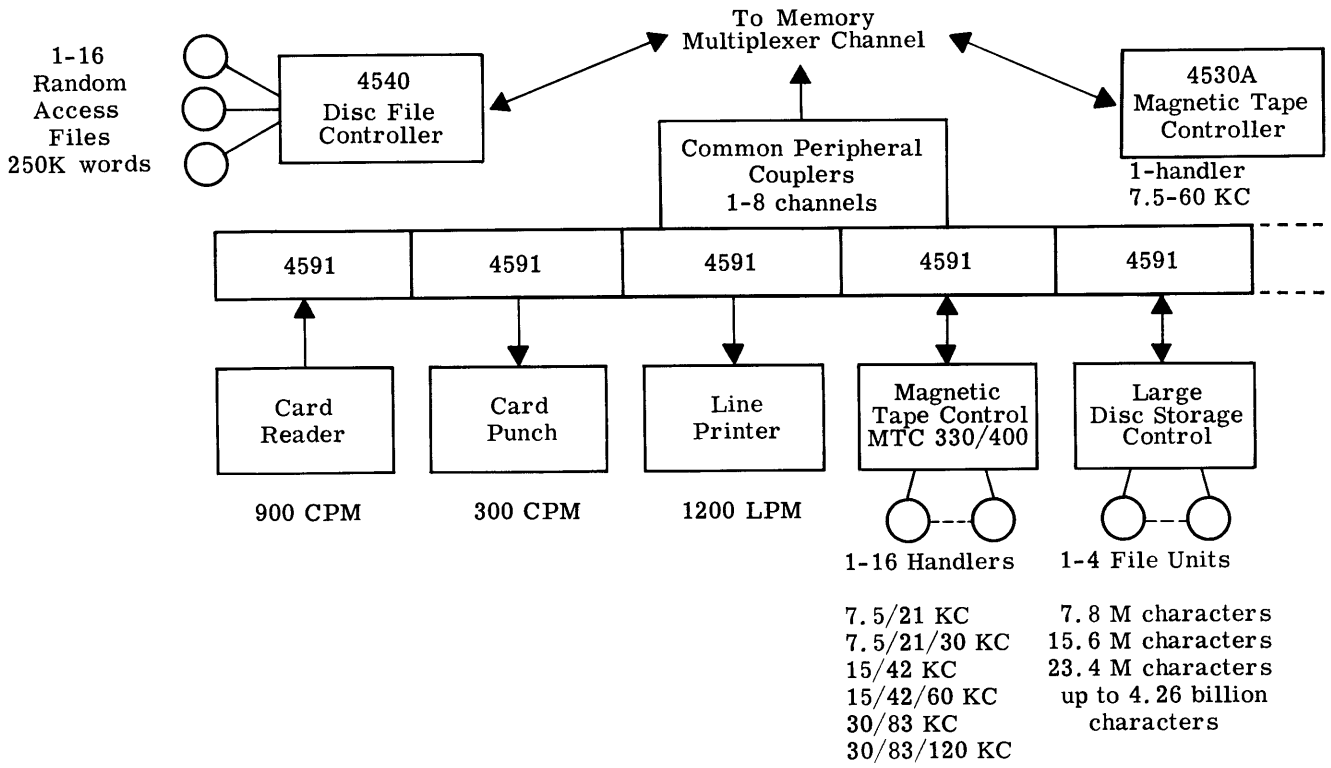
The multiple output modules are designed to provide digital-to-analog signals, and both latched and fixed-time-relay-contact outputs. A description of the modules follows (see Figure 9):

MULTIPLE OUTPUT CONTROLLER is one of three output controllers which are available. It accepts a general command from the central processor which it executes independently of the central processor. The MOC selects and actuates control in groups of 16 bits. A group may be 16 individual latching relays;

four BCD digits; or one analog signal. The analog signal resolution is ±0.1%. A single MOC can handle up to 64 groups (of 16 per group). A maximum of 4000 output operations per second is possible.

The TIMED OUTPUT CONTROLLER (TOC) is used to select and then time contact closures. The controller selects and energizes one of a maximum of 128 relays, and then holds it energized for a period of time specified by the control word. The controller is capable of holding the relay energized for up to 256 counts of a clock pulse. The clock reference frequency is determined by the application and it can be between 20 cps and 2 KC. For most applications, the line frequency of 50 cps or 60 cps will be adequate. As options, the TOC will also provide the ability to interface with GE/MAC and other set-point controllers.

IV MAN COMMUNICATIONS
DATA COMMUNICATIONS



The peripheral equipment provides communication between its operators and the computer system. Peripheral equipment as used in this manual has been distinguished from input/output equipment in that peripherals are those devices that are used for computer operation, i.e., typewriters and paper-tape readers and punches. Input/output equipment are those modules that communicate directly with the process, i.e., scanners.

The communication path into and out of the computer for peripherals is via either the peripheral buffer or the memory multiplexer. The peripheral buffer is the control unit for devices such as paper-tape readers, paper-tape punches, typewriters, and moderate speed card equipment and line printers. (See Figure 9.) The memory multiplexer is the control unit for devices such as magnetic tapes and disc files.

Peripheral equipment in this section is described under the following classifications:

- Man Communications
- Data Communications

MAN COMMUNICATIONS

Input/output Typewriters - Fixed carriage (Figure 10)

15.4 characters/second (maximum)
12 characters/inch
11-inch carriage width
15-1/2-inch carriage width (151 characters maximum)

Output Typewriters - Movable carriage

10 characters/second (maximum)
10 characters/inch
12, 20 and 30-inch carriages

Paper-tape Punch (Figure 11)

120 characters/second
8-channel paper tape

Paper-tape Reader (Figure 12)

100 or 200 characters/second
8-channel paper tape

Operator's Consoles (Figures 13 and 14)

The operator's console provides a means of communication between the operator and the process via the computer.

Data Links

Data links to Teletype models 33, 35; types RO, KSR, and ASR. Either TWX or private line communication via Dataset modens 103, 201, and TELPAK grade channels.

Data Editing Display (Figure 15)

Tube size - 14 inches, 1196 alphanumeric symbols, bar charts.

DATA COMMUNICATIONS

Card Readers (80 column, Hollerith/binary card formats)

70 CPM (Figure 16)
300 CPM (Figure 17)
900 CPM (Figure 18)

Card Punches (80 column, Hollerith/binary card formats)

100 CPM (Figure 19)
300 CPM (Figure 20)

Printers

300 LPM, 120 character positions, 10 characters/inch (Figure 21)
1200 LPM, 136 character positions, 10 characters/inch vertical format control, 27-1/2 ips skipping

Magnetic Tapes

A complete line of compatible magnetic tape handlers at 200 bpi, 556 bpi and 800 bpi.

- 7.5/21 KC, 37.5 ips, vacuum buffer, single capstan
- 7.5/21/30 KC, 37.5 ips, vacuum buffer, single capstan, 800 bpi
- 15/42 KC, 75 ips, vacuum buffer, single capstan
- 15/42/60 KC, 75 ips, vacuum buffer, single capstan, 800 bpi

(Figure 22)

- 30/83 KC, 150 ips, 4 vacuum capstans
- 30/83/120 KC, 150 ips, 4 vacuum capstans, 800 bpi

(Figure 23)

Random Access Disc Files

1. 262,000 up to 4,000,000 words, 1-16 units, write protect.

2. 1.96 million words per unit, 1-8 units, write protect. (Figure 24)

3. 5.9 million words per unit, 1-4 units, write protect.

4. 50 million up to 1 billion words is also available.

Common Peripheral Coupler

This module provides the control channel for interfacing a high-performance peripheral subsystem with the memory multiplexer. Up to eight 4591 couplers may be used on one memory channel. An option permits two, three or four subsystems to share one 4591 by switching under program control, but operation is non-simultaneous.

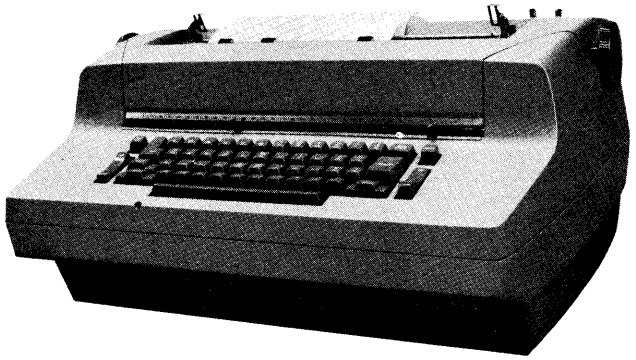


Figure 10. Input/output Typewriter

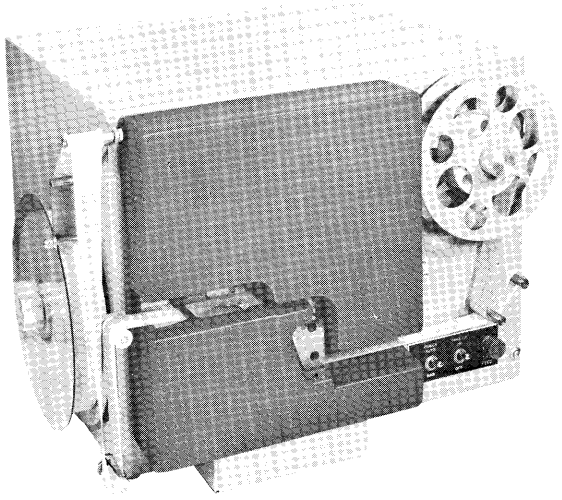


Figure 11. Paper-tape Punch

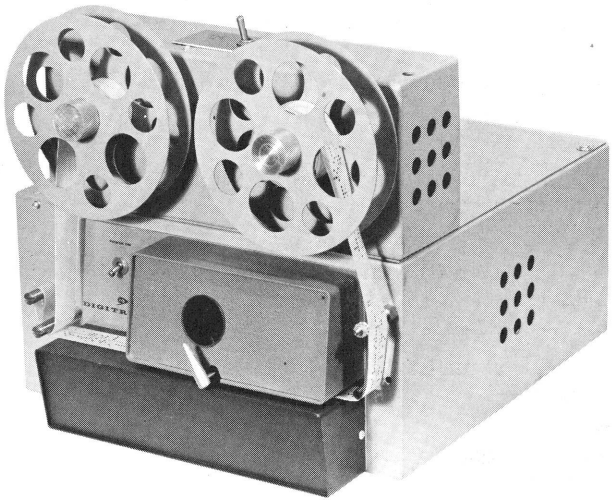


Figure 12. Paper-tape Reader

Figure 15. Data Editing Display

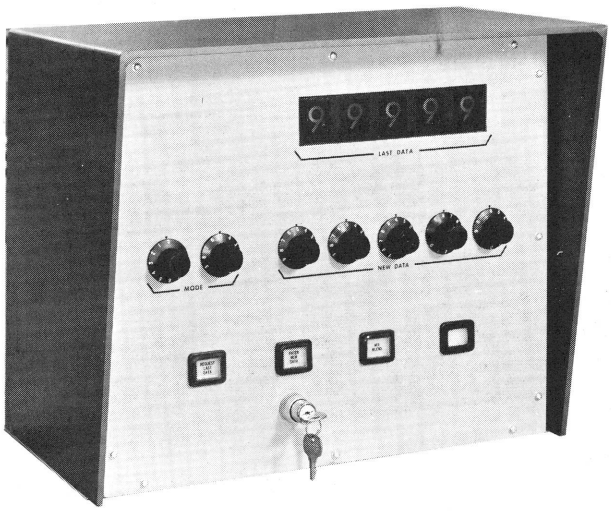


Figure 13. Operator's Console (for mounting in the control room)

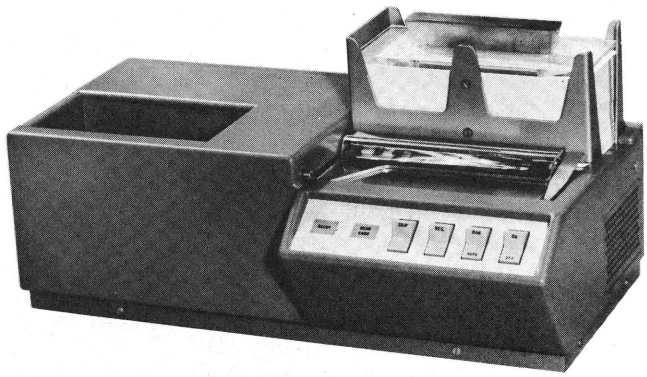


Figure 16. 70 Cards/minute Reader

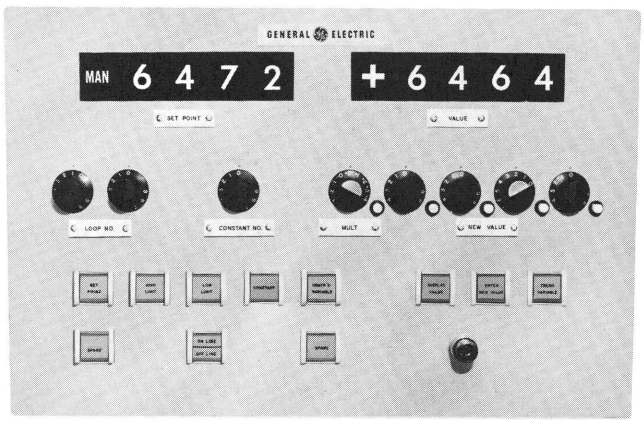


Figure 14. Operator's Console (for mounting adjacent to the process line)

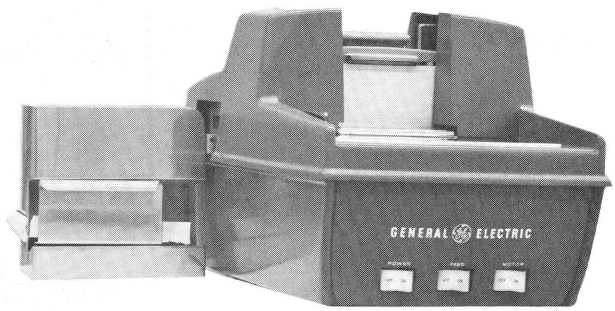


Figure 17. 300 Cards/minute Reader

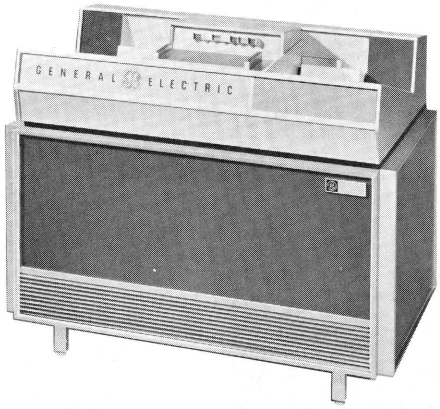


Figure 18. 900 Cards/minute Reader

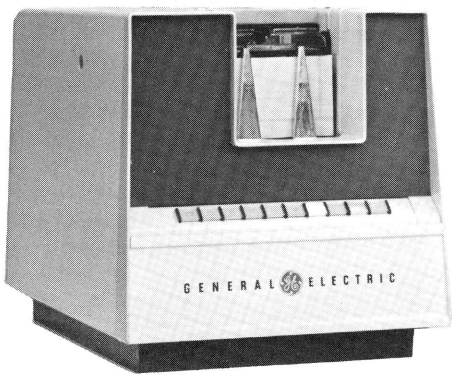


Figure 19. 100 Cards/minute Punch

Figure 20. 300 Cards/minute Punch

Figure 21. 300 LPM Printer

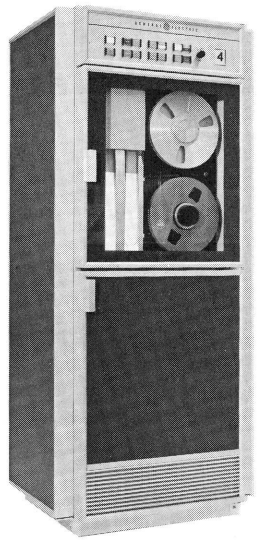


Figure 22. Magnetic Tape Handler

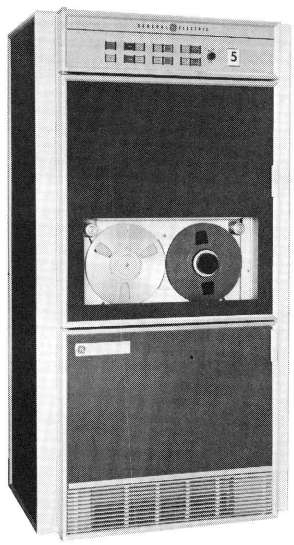


Figure 23. Magnetic Tape Handler

Figure 24. Random Access Disc File

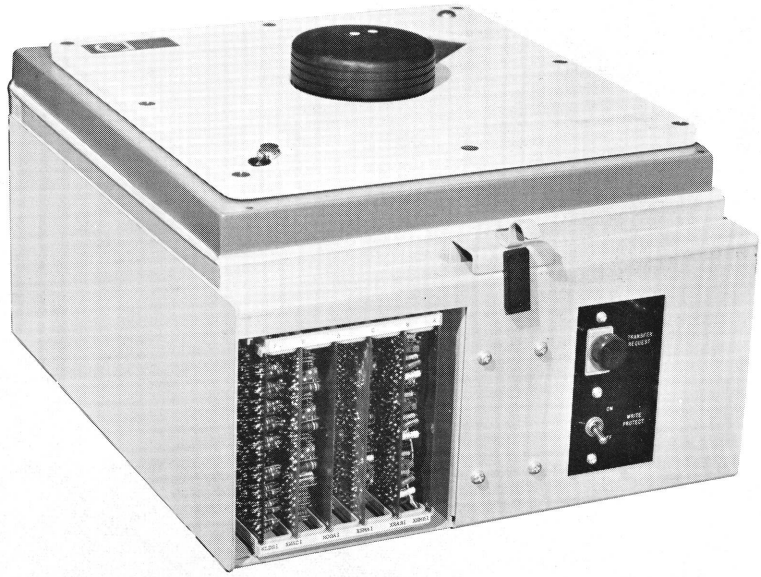


Figure 25. Random Access Disc File

V PROGRAMMING FEATURES OF GE/PAC 4000

INTRODUCTION

In the design of the GE/PAC 4000 system, cognizance has been given to the unique characteristics of real-time, on-line computer programs which distinguish them from programs written for off-line data processing applications. For this reason, the programmer will find GE/PAC 4000 more highly program-oriented than many other computers.

The typical process for which computer control is contemplated is characterized by the occurrence of many "events" or sub-processes, some continuous, some occurring periodically, and others occurring randomly. The computer is thereby required to perform many functions, seemingly simultaneously. However, a digital computer is by nature a serial device when considered at the instruction level; that is, it can perform its program steps only in a serial fashion, one by one. It is by virtue of its extreme speed that the digital computer can be successfully applied to process-control applications. In order that the computer program be able to serve the functional needs of the process, a priority system must be established for the many system functions. Simultaneous occurrence of certain combinations of events may then require a temporary reassignment of priorities. As a consequence of these requirements, real-time programs are distinctively different from their non-real-time counterparts.

The real-time program becomes in reality a system of programs which service the process functions in accordance with the established priority scheme. These programs operate under a "master control" program in such a manner that they interrupt one another as the changing process requirements dictate. There must be an underlying order in the seeming chaos which results from the interaction of so many programs, of course. Thus, it is an inherent requirement of the "master control" system that it perform efficiently a large amount of "bookkeeping" or "housekeeping." Indeed, the "housekeeping" functions, necessary to some degree in all computer programs, prove to be of primary importance in a real-time system program. For these reasons, GE/PAC 4000 incorporates several features specifically to facilitate "housekeeping" and its related functions of timekeeping and priority assignment.

In the preceding sections, the distinguishing hardware features of the GE/PAC 4000 system were discussed. It was pointed out that GE/PAC 4000 systems utilizing the AU 1 are classified as GE/PAC 4040 computers and those utilizing the AU 2 are classified as GE/PAC 4050 or GE/PAC 4060 computers. While GE/PAC 4050 and GE/PAC 4060 are more powerful computers than GE/PAC 4040 in terms of operating speed and the inclusion of certain functions not available in GE/PAC 4040, upward program compatibility has been maintained. That is, any program written for GE/PAC 4040 will run on either the GE/PAC 4050 or GE/PAC 4060 with a notable improvement in operating speed.

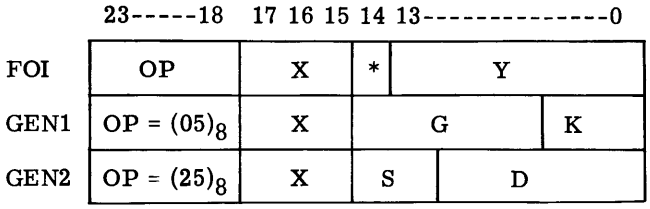
Obviously, complete downward compatibility is impossible since GE/PAC 4050 and GE/PAC 4060 incorporate features not available on GE/PAC 4040. However, use of the extended function command concept permits a high degree of downward compatibility.

The following sections are devoted to descriptions and usages of programming features applicable to the GE/PAC 4040, GE/PAC 4050, and the GE/PAC 4060 (except as noted).

PROGRAM CONTROL

A computer program consists of an ordered sequence of instructions to the computer. These instructions are placed in memory cells having sequential addresses so that the ordering of the addresses serves to order the instructions.

The following figure illustrates the three basic instruction formats used by the GE/PAC 4000 system:



OP	Instruction operation code
X	Indexing indicator
*	Relative - addressing indicator
Y	Operand address
G	GEN1 subcommand
K	Bit position or length of shift
S	GEN2 subcommand
D	Input/output device address
FOI	Full-operand instruction
	NOTE: Bit position 23: 0 = hardware instruction 1 = extended function command
GEN1	Register manipulation commands
GEN2	Input/output commands

Figure 26. GE/PAC 4000 Instruction Formats

The term "program control" is used in describing the instruction sequencing process and is associated with a location in memory. Program control is specified by the contents of the program counter. Program control normally is transferred from one location to the next sequential location as instructions are executed. Program control can be transferred to an arbitrary location by "branch" instructions. It can be made to conditionally skip a location by "jump" instructions.

MEMORY ADDRESSABILITY

The GE/PAC method of addressing core memory is the outgrowth of General Electric's recognition of two addressing requirements for process computers.

The first, and more immediate, requirement is to be able to transfer a program from bulk storage (drum memory) to core memory and instantly relocate all of its memory addressing instructions. The term "dynamic relocatability" was coined to describe this requirement. General Electric's solution is GE/PAC Relative Addressing which modifies the Y operand address of the instruction by its location in memory as the instruction is executed. It allows the on-line executive control program to instantly relocate a program from drum to any available place in core. More efficient use of both core and drum is possible. Ill effects of incorrect problem definition, system analysis, or programming analysis are minimized.

The second addressing requirement is efficient program addressability. The GE/PAC 4040 can address up to 16,384 words of core while the GE/PAC 4050 or GE/PAC 4060 can address up to 65,536 words of core.

Memory addressability by a memory addressing instruction is an "area addressability." A given instruction can generally address: 1) the area of 16,384 words at the beginning of core, 2) the area of 16,384 words extending 8192 words either side of the instruction. Indexing address modification allows the instruction to address any memory location. Indirect addressing instructions also allow addressing of any memory location.

RELATIVE ADDRESS MODIFICATION

The GE/PAC instruction format allocates a one-bit field (bit 14, Figure 26) to specify Relative Address modification. This bit is called the Relative Addressing Indicator and is designated by *. Relative Address modification may occur in any Full Operand instruction. It may not occur in any GEN1 or GEN2 instruction since this bit position I_{14} is used for other purposes in these instructions.

When I_{14} is zero in a Full Operand instruction, no relative modification occurs. When I_{14} is 1, the instruction's own address (obtained from the Program Counter) is added to its operand address before the instruction is executed.

For example:

Location Address	Operation	Bit Pos. 14	Y(Operand)	Comments
03000	LDA	*	00400	Effective Address for load A is 03000 + 00400 = 03400.

INDEXING ADDRESS MODIFICATION

The GE/PAC instruction format allocates a three-bit field I_X (I_{17-15}) to indicate Indexing Address modification. The field specifies seven consecutive core-memory locations for use as Index Words. The content of the field is called the "X-word indicator."

When Indexing Address Modification is specified (the field is non-zero), the 14-bit address(1) in the specified Index Word is added to the 14-bit operand address of the instruction in the I register to form the effective operand address.

X-Word Indicator	Effect Upon Address Modification
000	No Modification
001	Indexing Modification Using X Word 1
010	Indexing Modification Using X Word 2
011	Indexing Modification Using X Word 3
100	Indexing Modification Using X Word 4
101	Indexing Modification Using X Word 5
110	Indexing Modification Using X Word 6
111	Indexing Modification Using X Word 7

Indexing address modification occurs as defined above whenever the X-Word Indicator is non-zero for all instructions except the six Indexing Control instructions. The Indexing Control instructions provide the means to load, store, increment, and test individual index words without using the A register. The usage of X-word 1 and X-word 2 is restricted. X-word 1 is used automatically by the arithmetic unit for subroutine linkage, extended function command linkage, and Program Interrupt Linkage. X-word 2 is used automatically for extended function command linkage. As a general practice, these two X-words should not be used within a program.

EXTENDED FUNCTION COMMANDS

Extended function commands are special instructions which resemble hardware instructions, but they are actually implemented by subroutine. From the programmer's point of view, they are written in assembly language mnemonics and assembled in normal fashion. Automatic subroutine entry and exit locations are established as a special two address instruction. This concept provides the basis for the upward compatibility in changing from a GE/PAC 4040 to a GE/PAC 4050 or GE/PAC 4060. Corresponding instructions for the GE/PAC 4050 or GE/PAC 4060 are implemented by hardware.

(1) The address is 16 bits in GE/PAC 4050 and 4060.

The octal code generated specifies a fixed address in a branch vector leading to a subroutine. Its Y address is a normal operand address. The computer computes the effective operand address from the Y, *, and X fields of the instruction and saves this address in index word two. It then executes an SPB (store place and branch) instruction in the location specified by the instruction octal.

Several benefits of extended function commands are evident:

1. A richer effective instruction repertoire permits easier coding.

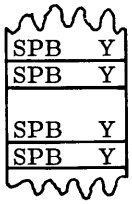
2. Upward program compatibility is possible.

3. This technique reduces memory requirements of programs when compared to the use of conventional subroutine techniques.

Figure 27 presents an example of a "Store Zero into Memory" extended function command. STZ is arbitrarily assigned 63_8 as its octal code. Note that inhibitable program interrupts are inhibited during the execution of the STZ subroutine. Note also that the first instruction of the subroutine is a STX (store X) to conform with standard subroutine convention so that program control is not lost in case a noninhibitable program interrupt executes an SPB.

Instruction octals 40_8 through 77_8 are extended function commands in GE/PAC 4040. Instruction octals 40_8 through 67_8 are hardware implemented commands in GE/PAC 4050 and 4060. Instructional octals 70_8 through 77_8 are extended function commands in GE/PAC 4050 and 4060.

Extended Function Command Area



00040	SPB Y	BRANCH VECTORS	Branches will be executed to the entry points of the subroutines.
00041	SPB Y		
00076	SPB Y		
00077	SPB Y		

SPB of this area forms the linkage with the subroutines. This instruction stores the location following the extended function command in 0001 so that a return can be made to the next normal instruction in the main program.

Some examples of extended function commands used in GE/PAC 4040 are floating-point operations, list operations, and repeat. (See the instruction list section for others.)

EXECUTE INSTRUCTION (XEC) AND ITS USAGE

In an Execute Instruction (XEC), the address portion of the instruction specifies an object instruction to be executed, but does not set the location counter to the location of the object instruction as would a branch instruction. Thus, in effect, an XEC calls a one-instruction subroutine and specifies immediate return to the main routine.

Location	Instruction	Comments
.	.	
.	.	
.	.	
Place	STZ Data	Extended function command in Main Program.
.	.	Octal code of STZ gen-
.	.	erates a jump to $(63)_8$
.	.	arbitrarily selected.
.	.	$(63)_8$ is an SPB to
.	.	subroutine.
00063	SPB STZ	Portion of Branch Vector
.	.	
.	.	
.	.	
.	.	
STZ	STX SX, 1	Store X1
	STA SA	Subroutine
	LDZ	(x1) = Place + 1
	STA 00000, 2	(x2) = Data
	LDA SA	
	LPR SX	Return to Place + 1
SA	BSS 1	Temporary Storage
SX	BSS 1	

Figure 27. Example of extended function command linkage and subroutine; store a zero into a memory location (the operation, STZ, has not been included in the extended function common instruction list. This is a short example which is intended to illustrate the principle).

The use of the XEC operation arises directly from the fact that the object instruction does not imply its own successor (unless it be a branch). The XEC simplifies modification of non-indexable instructions (such as index control instructions) as well as providing the ability to effectively "modify" programs (remotely) which, for some reason, may not be directly modified. Effective use may also be made of the XEC in the case of subroutine calling sequences where the calling sequence to the subroutine may include several parameters specified in actual machine instructions which the subroutine treats as second-order one-word subroutines.

Execute completes a set of four program-control operations:

1. Program Control is retained by the Main Program (Normal Instruction Sequencing).

2. Program Control is given to another program (Branching).

3. Program Control is usurped by another program (Program Interrupt).

4. Program Control is lent to another (one instruction) program (execute).

AUTOMATIC PRIORITY INTERRUPT (API)

Program interrupt is the only known satisfactory hardware method to synchronize a computer program with the outside world.

An occurrence of an event in the outside world may be sensed and a signal (indicating event true/ event false) connected to the GE/PAC Automatic Priority Interrupt module. Two types of event detection are provided by the GE/PAC API module:

1. The event has occurred (was and/or is true) at some time in the past and a program interrupt to acknowledge the occurrence has not yet taken place.

2. The event is now occurring (was and is true) and a program interrupt to acknowledge the occurrence has not yet taken place.

In either case, the GE/PAC API module will remember the event until a program interrupt can be made to acknowledge its occurrence. The GE/PAC API will then forget the event.

Type 1 event detection is normally used to provide:

Event recording

Pulse accumulation

Process-to-program synchronization

Type 2 event detection is designed for use in controlling interrupt-driven I/O equipment (i.e., scanner, typewriter, punch, etc.).

Two classes of Program Interrupt (with respect to program control) are provided in GE/PAC systems.

INHIBITABLE INTERRUPTS

The program has control over whether or not such interrupts may occur. Execution of an IAI (inhibit automatic interrupt) or SPB instruction places the computer in the "Program Interrupt inhibited mode." Inhibitable interrupts will be delayed until such time as a PAI (permit automatic interrupt) instruction is executed to place the computer in the "Program Interrupt permitted mode." The instructions LDP and LPR will either inhibit or permit interrupt depending upon bit 21 of the referenced memory location.

NONINHIBITABLE INTERRUPTS

The program has no control over the occurrence of such interrupts. A program interrupt acknowledging the occurrence of the event will be made within 1 to 82 micro-seconds of the occurrence of the event.

In using the SPB instruction, proper program control is assured by the programming convention of storing index register one prior to permitting additional interrupts.

A program interrupt is an "execute" function. That is, one instruction is inserted into the normal sequence, with normal incrementing of the Program Counter being inhibited during the execution of the inserted instruction. The address of the inserted instruction is generated by the control circuitry from the active position of the interrupt register. Normally, memory locations $(00100)_8$, $(00101)_8$, etc., are used for the interrupt locations corresponding to interrupts levels 0, 1, etc.

The inserted instruction will normally be one of four specific GE/PAC instructions: DMT (Decrement Memory & Test), SPB (Store Place & Branch), NOP (No Operation), or BRU (Branch). Normally, SPB will be used for inhibitable interrupts and DMT for noninhibitable interrupts. NOP would be used as a means of temporarily disabling an interrupt-driven program. BRU would be used only for entrance to an emergency-action program, since it would not permit a return to the main-line program at the point of interruption. SPB, which "remembers" the location and status of the main-line program, would be used to cause entrance to a subprogram designed to service the interrupting condition. DMT would be used to perform counting functions such as pulse accumulation or system timekeeping since it automatically decrements the number found in the operand address by one.

See Figure 28 for a typical allocation of inputs to the API Module.

SUBROUTINE LINKAGE

The subroutine linkage instruction SPB (Store Place and Branch) is an ideal example of the system approach to computer design. SPB is much more than a subroutine linkage instruction. The specifications of extended function command linkage and program interrupt are closely related to SPB.

SPB saves, in index register one, the status (interrupt, test, overflow, and program counter) of a main program, inhibits interrupt, and transfers program control as directed by the operand address. Return from a subroutine to the main program is implemented by the instructions LDP (Load P from location Y) or LPR (Load P from location Y and Restore) which restores the saved status.

TESTS AND THE CONDITIONAL BRANCH BTS

GE/PAC has two conditional branch instructions, BTS and BTR, which conditionally branch on the status (set/reset) of a test flip-flop, TSTF. With the exception of the test for arithmetic overflow, BTS/ BTR is used for all conditional branches based upon internal effect tests. The TSTF serves as a memory element to remember the result of a previous test and will retain this status until changed by program. Since its status is not destroyed by BTS/BTR, many branches may be made upon the result of a single test. The status of TSTF is saved by SPB and can be restored by LPR:

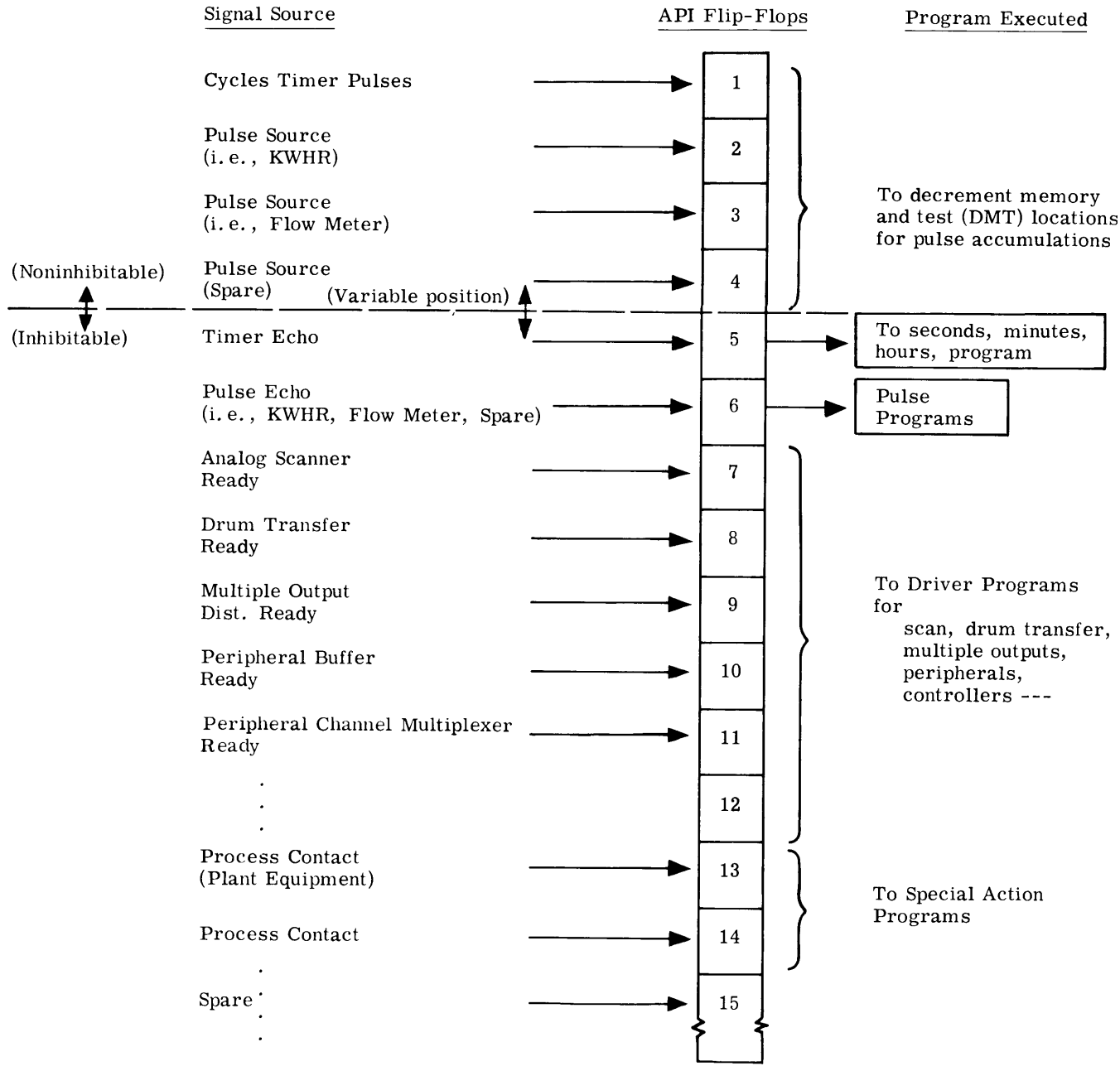


Figure 28. Typical Allocation of Inputs to API Module

There are two types of testing instructions available to the programmer:

1. The first type generally has the letter T as the first character of its mnemonic. It places the result of the test (true/false) into the TSTF.

2. The second type generally has the letter S or R as the first character of its mnemonic. It affects (sets/resets) the TSTF only if the test is true.

Type T tests are ordinarily used for conventional decision making. Type S or R tests are most useful in the evaluation of logic equations. Three Program Control Instructions (SET, RST, LPR) are available to set the TSTF to a predetermined status. (See instruction list for definitions.)

Examples of the use of test commands and BTS will follow in a later section.

DATA MANIPULATION

GENERAL

The "bit" is the elemental unit of data. A larger and sometimes more convenient unit is the "word" which (in GE/PAC) consists of an ordered set of 24 "bits." GE/PAC is word organized with respect to addressing and arithmetic; it is partially bit organized with respect to logic.

Data Manipulation is accomplished in one or more of the following registers:

A - Register

Q - Register

Addressed memory location Z.

The group of "General" instructions provides the means to load or store each register. "Arithmetic," "Logic," and "Test" instructions implement data manipulation operations.

The A Register, being the primary working register, is affected by a majority of the data manipulation operations. The Q Register is used as an extension of the A Register or as an auxiliary register. Few operations affect it. The "Operate on Memory" (OOM) instruction provides a means of applying all of the A Register Operations to an addressed memory location. "Operate on Memory" is a two-word format:

1. The first word (OOM) defines the memory location to be used as the accumulator.

2. The second word is the instruction to be executed upon the defined memory location.

FIXED-POINT AND FLOATING-POINT NUMBER REPRESENTATION

Numeric variables are represented by sequences of digits. The GE/PAC word, with bits interpreted as digits, provides binary representation of any real number with a precision of 23-binary digits.

There are three common binary representations for negative numbers:

1. Sign plus absolute value

2. "ones" complement

3. "twos" complement

In each case the left-most bit is interpreted as the sign of the number - - - -0 meaning +, and 1 meaning -.

"Two's Complement" representation is used in GE/PAC for fixed-point arithmetic.
"Sign plus absolute value" representation is used in GE/PAC for floating-point arithmetic.

The integral and fractional portions of the number are separated by a "binary point." The binary point has no analogy in hardware. In the case of fixed-point arithmetic, the binary point is supplied mentally by the programmer and is referred to as the "scale" of the number. In the case of floating-point arithmetic, the binary point is defined by an exponent within the floating-point number representation; the mantissa is always a normalized fraction. Arithmetic data formats are depicted in Figure 29.

LOGIC VARIABLES

Yes/no, true/false, on/off, and set/reset conditions are represented by Logic Variables and obey the laws of Boolean algebra. If a one-to-one correspondence between Logic Variables and bits be made, then a set of 24 such variables may be represented by a GE/PAC computer word. In such a representation, 1 usually means true and 0 means false.

GE/PAC has the conventional logical instructions (CPL, ORA, ANA, ERA) (see instruction list for definition) which address memory and operate on the addressed 24-bit words. In addition, a GEN1 class of instructions allows the programmer to address individual bits of a word in the A-Register and perform the same operations on the addressed bits. Thus:

SBK	K	Sets the Kth bit of A to a "1"
CBK	K	Changes the Kth bit of A
TOD	K	Tests the Kth bit of A

(any many others) are provided. Instructions such as CPL and shifting instructions are a natural by-product. An appreciation of the value of the operations to process control is obtained from an example: A large share of a control program consists of decision making based upon the status of true/false bit-logic variables. These conditions are normally read into the computer via a Digital Input Scanner.

Assume that one step in a start-up process consists of determining that one and only one of two pumps is "on" with its valve being open and also that a main valve is open.

A = Motor on, pump #1
B = Valve open, pump #1
C = Motor on, pump #2
D = Valve open, pump #2
E = Main valve open

The programming technique does not depend upon the arrangement of the variables; hence, all may be assumed to fall in the same word without loss of generality. The step may be expressed in the form of a logic equation:

If ((A*B*-C*-D) + (-A*-B*C*D))* E = 1, to OK; otherwise go to ALARM. GE/PAC coding for this equation is given in Figure 30.

It is possible to produce a shorter program using GE/PAC's conventional logical instructions (CPL, ORA, ANA, ERA) if rigid assumptions with respect to the location and arrangement of the bit

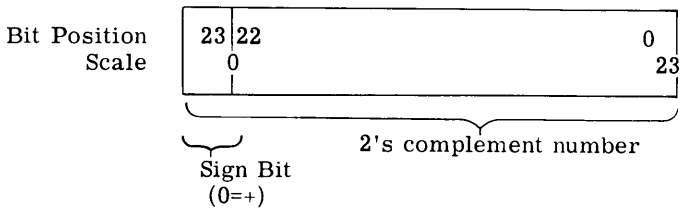
variables be made. In this latter case, all five variables must be assumed to fall in sequence in the same digital word. GE/PAC coding for the equation is given in Figure 31.

LIST - PROCESSING INSTRUCTIONS

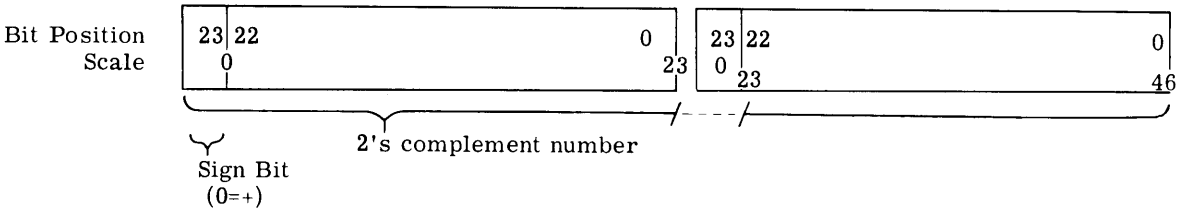
A "List" consists of an ordered set of "items" contained within a fixed-length block of memory ($2^L + 1$ words where L is an integer, $1 \leq L \leq 9$).

The first word of the block is a "list control word" and serves as the address or label of the list. The maximum size of any given list is 2^L "items." The physical ordering of a list is circular in nature; that is, the address 2^L relative to the list control word is followed sequentially by the relative address 1. The terms "beginning item" and "ending item" are arbitrarily attached to the first and last members of the set of items currently forming the list.

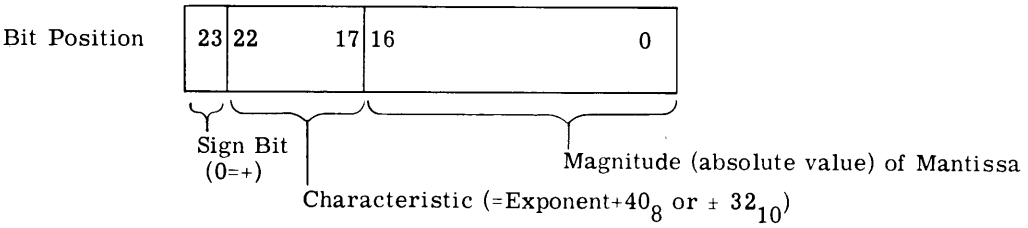
Single-Word Fixed Point



Double-Word Fixed Point



Single-Word Floating Point



Double-Word Floating Point

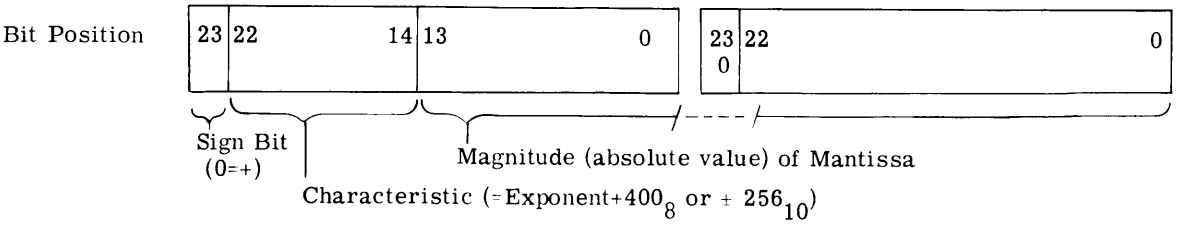


Figure 29. Arithmetic Data Formats

Location	Instruction	Address	Comments
START	LXK	0,7	CLEAR TEMPORARY
	LDA	GROUP	LOAD A WITH CONTACT STATUS
	TOD	BIT A	TEST ODD
	REV	BIT B	RESET TSTF, IF EVEN
	ROD	BIT C	RESET TSTF, IF ODD
	ROD	BIT D	T1 - A*B*-C*-D
	BTR	*+2	SAVE T1 IN TEMPORARY
	INX	1,7	
	TEV	BIT A	TEST EVEN
	ROD	BIT B	RESET TSTF, IF ODD
	REV	BIT C	RESET TSTF, IF EVEN
	REV	BIT D	T2 = -A*-B*C*D
	LDA	07	LOAD A WITH LAST VALUE OF TEST FF
	SOD	20	T3 = T2 + T1, TEST FF IN 20
	LDA	GROUP	
	REV	BIT E	T4 = T3 * E
	BTS	OK	IF T4 = 1 BRANCH TO OK
	BRU	ALARM	IF T4 ≠ 1 BRANCH TO ALARM
BIT A	EQL	5	BIT POSITIONS ARE DEFINED IN THE ASSEMBLY PROGRAM.
BIT B	EQL	6	
BIT C	EQL	7	
BIT D	EQL	8	
BIT E	EQL	9	
GROUP	EQL	1000	

Figure 30. Use of GE/PAC bit logic instructions to evaluate logic equation if (A*B*-C*-D + A*-B*C*D) * E = 1, go to OK.

Instructions are provided for appending additional items to the beginning or end of the list and for removing the beginning or ending items.

These instructions are:

ABL Z Append item to beginning of List Z
AEL Z Append item to End of List Z
RBL Z Remove beginning item from List Z
REL Z Remove ending item from List Z

An item, when appended, becomes the new beginning (ending) item. The removal of an item forces the adjacent item to be the new beginning (ending) item. The current beginning and ending items are the only items addressable by program ---- note this contrast to normal table indexing techniques which allow addressing of any entry in a table.

Location	Instruction	Address	Comments
START	LDA	GROUP	LOAD A WITH CONTACT STATUS
	SRL	1	SHIFT RIGHT LOGICAL 1
	ERA	GROUP	EXCLUSIVE OR TO A
	ERA	MASK 1	
	ANA	MASK 2	ADD (Z) TO A
	TNZ		TEST A ≠ 0
	BTS	OK	BRANCH OK IF TEST FF = 1
	BRU	ALARM	BRANCH ALARM
GROUP	EQL	1000	
MASK 1	CON	/44000000	OCTAL MASK CONSTANTS
MASK 2	CON	/5600000	

NOTE: BIT A, BIT B, BIT C, BIT D AND BIT E MUST BE IN POSITIONS 22, 21, 20, 19 AND 23.

Figure 31. Use of GE/PAC word logic instructions to evaluate logic equation if (A*B*-C*-D + -A*-B*C*D) * E = 1, go to OK.

THE QUEUING LIST AND ITS USAGE

Webster's definition of a "queue," a "waiting line, as of persons before a ticket window," describes the Queuing List quite satisfactorily.

A typical usage of the queuing list is for channeling of information to and through Input/Output devices. Suppose a request for the "on demand print-out" of the current value of some analog input be made. The scan command word and appropriate control information would be appended to a queue controlling the operation of the scanner. When available, the raw "count" value of this input will be appended to a queue awaiting conversion from binary to engineering units.

Another queue is a waiting line to the binary to BCD conversion routine. The resulting ordered set of BCD characters is appended to the output driver queue controlling a typewriter.

The instruction pair AEL, RBL are used for queuing. Just as it is possible for a "Very Important Person" to go to the "head of the line," high-priority items may be appended at the head (beginning) of the list so that it would be the next item to be removed. Thus AEL and RBL provide normal queuing; ABL is used to place high-priority items at the "head" of the list.

THE STACKING LIST AND ITS USAGE

The "stack" or "push-down list" is so named because the item most recently appended to the list is always removed prior to the removal of less recently appended items. The phrase "last in - first out" is sometimes used to describe the operation of a stack.

A typical usage of a stack is as a Common temporary storage block for programs that are subject to Program Interrupt. Each program by appending all of its intermediate results in the stack could be "clobbered" by a higher priority program. When all higher priority programs were completed, this clobbered program would be restored to continue from its point of interruption.

INPUT AND OUTPUT CONTROL

GEN2 instructions are microcoded instructions used for control of Input/Output Equipments and for certain computer actions. (See instruction format description, Figure 26.)

Device address D = 0000_8 is a ficticious address referring to the computer itself.

The following instructions are provided:

Program Control

25010000	SSA	Set Stall Alarm
25020000	PAI	Permit Automatic Program Interrupt
25030000	IAI	Inhibit Automatic Program Interrupt
25040000	JND	Jump if No Demand
25050000	RCS	Read Console Switches

Validity Tests

25060000	JNO	Jump if No Overflow
25070000	JNP	Jump if No Core Parity

Device addresses D = $11DD_8$ refer to peripheral devices. Other device addresses are defined as required for each individual system.

The generic instructions:

2500	SEL	Select Device D
2501	ACT	Activate Device D
2502	OPR	Operate Device D
2503	ABT	Abort Device D Operation
2504	OUT	Output from A Register and Initiate Operation of Device D
2505	IN	Input to A Register and Initiate Operation of Device D
2506	JNR	Jump if Not Ready
2507	JNE	Jump if No Error

are recognized by the assembly program. Specific meanings for each action are determined by the specific requirements of each given device D. The user is referred to specific descriptions of the various devices for detailed information.

Since Indexing Address Modification affects bits 13 through 0 of the instruction, indexing can change the meaning of the GEN2 instruction.

Since input/output devices in general, and in particular those referred to as peripherals ("hard-copy" devices such as paper-tape readers and punches, typewriters, and line printers), operate at speeds much slower than that of the central processor, it is imperative in a real-time system that their operation be programmed in such a manner as not to require that the system program incorporate delays to wait for their operation. For this reason their usage is normally implemented through the use of the interrupt function. The "device-ready" signal from each input/output device is wired to cause program interrupt, with SPB commands being placed in the appropriate interrupt locations in memory. Each SPB command causes entrance to a "peripheral drive program" whose sole function is to initiate the next action request for the associated device.

A function such as the typing of a log on a system typewriter is then accomplished through cooperative action of two programs. The Log Program collects and properly formats the data and control characters (spaces, tabs, carriage returns, etc.) and places them into a table in memory. It then executes the ACT command to signal, through interrupt action, to the Typer Drive Program that there is output for it to perform. The Typer Drive Program then initiates one typewriter action each time it is entered as a result of the Typewriter ready signal causing a program interrupt.

Alarm printing, analog scanning, all peripheral actions, data and program transfers between core and drum memories are all typical functions implemented as described above. Through the use of this scheme, many such functions can proceed simultaneously, with each device being driven at its maximum rate, with negligible impeding of the central processor speed and the normal program flow.

SPECIAL PROGRAMMING FEATURES OF GE/PAC 4050 AND GE/PAC 4060

The preceding sections have discussed programming features applicable to the GE/PAC 4040, GE/PAC 4050, and the GE/PAC 4060. Those instructions which are implemented as extended function commands are so indicated in the instruction list that is contained in Section VI.

Several very powerful hardware implemented instructions have been designed into the GE/PAC 4050 and GE/PAC 4060 computers which have not been implemented by extended function command in the GE/PAC 4040 computer. These are described thus:

REPEAT INSTRUCTION

The Repeat Instruction is a powerful tool in that it incorporates all the functions of program loop control into a single hardware-implemented instruction. Figure 32 compares the instruction sequences and execution times for program loops to add 1000 numbers in the A Register. Even more impressive savings are possible in programming such operations as memory searching on partial words (table look-up-field search).

Repeat operation is provided in the following manner:

1. The instruction to be repeated is executed the number of times plus one, as specified in an index register.

2. Each time the instruction to be repeated is executed the effective operand of that instruction is incremented by one.

3. After the instruction is repeated, the loop counter is incremented, and the results of the execution are tested. If the proper test condition exists, the loop is exited.

This mode allows for the loop operation with only the execution time of the repeat instruction required, and not the time of the executed instruction. For example, to add 1000 numbers would require 1003 memory cycles not 2000 or 3000 memory cycles as other computers might require without this feature. The repeat function is interruptable.

BLOCK REGISTER STORAGE AND RETRIEVAL

LDR and STR provide the ability to store or retrieve all working registers (arithmetic and index words) through single hardware instructions, a function of great utility in performing the "housekeeping" tasks so prevalent in real-time programs. These instructions also serve the function of block transfer of information. One instruction (STR) saves in memory the index registers 2-7, accumulator and auxiliary accumulator registers. Conversely, one instruction (LDR) restores these registers from memory. Other instructions save contents of place counter and flip-flop status.

I/O CONTROLLER INSTRUCTIONS

This pair of instructions, IDL and ODL, provides the ability to transfer information directly between memory and a peripheral device. IDL and ODL make use of the list-processing capability in combination with the normal GEN2 input/output hardware in such a manner that a single instruction can affect the

I. INDEX CONTROL

Location	Instruction	Address	Comments
START	LDZ		LOAD ZERO IN A
	STA	03	X 3
	ADD	TABLE, 3	
	TXH	999, 3	TEST (X) > OR =
	BTS	* + 3	
	INX	1, 3	INCREMENT X 3
	BRU	* - 4	RETURN
	BRU	OUT	COMPLETE
TABLE	BSS	1000	SAVE 1000 LOCATIONS

NOTE: ROUTINE TAKES 11,004 WORD TIMES

II. DECREMENT MEMORY AND TEST

Location	Instruction	Address	Comments
START	LDZ		LOAD ZERO IN A
	LXK	999, 3	LOAD X 3
	ADD	TABLE, 3	
	DMT	03	DECREMENT MEMORY AND TEST
	BTS	* - 2	
	BRU	OUT	
TABLE	BSS	1000	SAVE 1000 LOCATIONS

NOTE: ROUTINE TAKES 6005 WORD TIMES

III. REPEAT INSTRUCTION

Location	Instruction	Address	Comments
START	LDZ		LOAD ZERO IN A
	LXK	999, 3	LOAD X 3
	RPT	ADDR, 3	REPEAT
	BRU	OUT	
ADDR	ADD	TABLE, 3	
TABLE	BSS	1000	SAVE 1000 LOCATIONS

NOTE: ROUTINE TAKES 1008 WORD TIMES

Figure 32. Sample coding of three methods of looping with GE/PAC 4060 sum 1000 numbers stored in "table".

transfer of data from (to) a "list" to (from) the peripheral device. These instructions can, therefore, be used as one-word interrupt subroutines in much the same manner as DMT functions.

I/O BUFFER INSTRUCTIONS

This pair of instructions, LDB and STB, is designed to be used as object instructions of the RPT (repeat) instructions. Each execution of one of these instructions effects a data transfer directly between memory and an input/output device, and when coupled with RPT, can transfer information at word rates up to 580 KC (with 1.7μsec. memory).

VARIABLE FIELD ARITHMETIC AND MASKED MEMORY COMPARE

GE/PAC 4050 and GE/PAC 4060 instructions provide for maximum arithmetic operation on packed words, i.e., where one word contains more than one field of information. The word that defines the field is contained in the auxiliary accumulator register. Variable field arithmetic is comprised on the Load, Add, Subtract, and Store instructions. Memory compare instructions include Compare Equal and Compare Less instructions. These instructions provide maximum programming efficiency in memory field arithmetic and memory search techniques.

VI INSTRUCTION LIST

NOTES TO GE/PAC 4000 INSTRUCTION LIST

Z is sum of indicated operands
* = Relative Addressing Indicator
Y = Memory Location Address
K = Constant
D = Device Address
X = Indexing Address Modification Indicator

A refers to Accumulator Register
Q refers to Auxiliary Accumulator
P refers to Program Control Register
(A) should be read as "The Contents of A" (similarly for other registers)
N refers to instructions not applicable to the GE/PAC 4040

Execution times for GE/PAC 4040 are rounded to nearest microsecond.

Indexing Address Modification adds:

1.7 μsec in GE/PAC 4060 with 1.7 μs memory

3.4 μsec in GE/PAC 4050-II with 3.4 μs memory

Approximately 6 μsec in GE/PAC 4040

Underlines times; i.e., 572, listed as the execution times for the GE/PAC 4040 represent instructions implemented as extended function commands.

Refer to programming manual (PCP-102) for comments regarding indexing, timing, etc.

INSTRUCTION	SYMBOLIC CODING		EXECUTION TIME (μSEC) 4040	4050-I	4050-II	4060
APPEND TO BEGINNING OF LIST Z	ABL	*, Y, X	572	23.4	16.6	9.8
ABORT DEVICE Z OPERATION	ABT	D, X	32	32.3		29.0
ACTIVATE DEVICE Z	ACT	D, X	32	36.7	33.3	30.0
ADD (Z) TO A	ADD	*, Y, X	16	10.2	6.8	3.4
ADD ONE TO BIT Z OF A	ADO	K, X	16	18.3	14.9	11.5
APPEND TO END OF LIST Z	AEL	*, Y, Z	580	23.4	16.6	9.8
ADD FIELD OF (Z) TO A	AFA	*, Y, X	N	18.3	14.9	11.5
ADD Z TO A	AKA	*, K, X	127	5.1	3.4	1.7
AND (Z) TO A	ANA	*, Y, X	16	10.2	6.8	3.4
BRANCH UNCONDITIONALLY TO Z	BRU	*, Y, X	14	5.1	3.4	1.7
BRANCH TO Z IF TSTF IS RESET	BTR	*, Y, X	14	5.1	3.4	1.7
BRANCH TO Z IF TSTF IS SET	BTS	*, Y, X	14	5.1	3.4	1.7
CHANGE BIT Z OF A	CBK	K, X	16	18.3	14.9	11.5
COUNT LEAST SIGNIFICANT ONES	CLO		16	18.3	14.9	11.5
COUNT LEAST SIGNIFICANT ZEROS	CLZ		16	18.3	14.9	11.5
COUNT MOST SIGNIFICANT ONES	CMO		16	18.3	14.9	11.5
COUNT MOST SIGNIFICANT ZEROS	CMZ		16	18.3	14.9	11.5
COMPLEMENT (A)	CPL		16	18.3	14.9	11.5
DOUBLE LENGTH ADD (Z, Z+1) TO A, Q	DAD	*, Y, X	284	15.3	10.2	5.1
DOUBLE LEFT-SHIFT ARITHMETIC, Z PLACES	DLA	K, X	967	20.7	14.9	3.4-13.9
DOUBLE LOAD A, Q FROM Z, Z+1	DLD	*, Y, X	125	15.3	10.2	5.1
DOUBLE LEFT-SHIFT LOGICAL, Z PLACES	DLL	K, X	734	10-20.7	14.9	3.4-13.9
DECREMENT MEMORY LOCATION Z AND TEST	DMT	*, Y, X	21	15.3	10.2	5.1
DOUBLE RIGHT-SHIFT ARITHMETIC, Z PLACES	DRA	K, X	691	10-20.7	14.9	3.4-13.9
DOUBLE RIGHT-SHIFT CIRCULAR, Z PLACES	DRC	K, X	821	10-20.7	14.9	3.4-13.9
DOUBLE RIGHT-SHIFT LOGICAL, Z PLACES	DRL	K, X	797	10-20.7	14.9	3.4-13.9
DOUBLE STORE FROM A, Q TO Z, Z+1	DST	*, Y, X	132	15.3	10.2	5.1
DOUBLE SUBTRACT (Z, Z+1) FROM A, Q	DSU	*, Y, X	298	15.3	10.2	5.1
DIVIDE (A, Q) BY (Z)	DVD	*, Y, X	5344	34.6	30.9	27.8
EXCLUSIVE OR (Z) TO A	ERA	*, Y, X	16	10.2	6.8	3.4
FLOATING ADD (Z) TO A	FAD	*, Y, X	990	246.8	161.5	92.4
FLOATING DIVIDE (A) BY (Z)	FDV	*, Y, X	2631	335.6	233.0	140.2
CONVERT (A) TO FIXED-POINT FORMAT AT SCALE Z	FIX	K, X	448	324.4	228.0	34.0
CONVERT (A) TO FLOATING-POINT FORMAT FROM SCALE Z	FLO	K, X	566	265.2	185.0	34.0

INSTRUCTION	SYMBOLIC CODING		EXECUTION TIME (μSEC) 4040	4050-I	4050-II	4060
FLOATING MULTIPLY (A) BY (Z)	FMP	*, Y, X	1460	271.3	189.0	109.4
FLOATING MODE SHIFT	FMS			542.6	357.0	179.0
FLOATING SUBTRACT (Z) FROM (A)	FSU	*, Y, X	1020	267.2	175.0	99.8
INHIBIT AUTOMATIC INTERRUPT	IAI		32	10.2	6.8	3.4
ISOLATE BIT Z	IBK	K, X	16	18.3	14.9	11.5
INPUT FROM DEVICE TO LIST Z	IDL	*, Y, X	N	65.7	51.3	41.5
INPUT FROM DEVICE Z TO A	IN	D, X	32	36.5	33.3	29.9
INCREMENT (X) BY Z	INX	*, K	21	15.3	10.2	5.1
JUMP IF NO DEMAND	JND		32	10.2	6.8	3.4
JUMP IF NO ERROR ON DEVICE Z	JNE	D, X	32	36.7	33.3	29.9
JUMP IF NO OVERFLOW	JNO		32	10.2	6.8	3.4
JUMP IF NO PARITY ERROR	JNP		32	10.2	6.8	3.4
JUMP IF DEVICE Z IS NOT READY	JNR	D, X	32	36.5	33.3	29.9
LOAD BIT MASK, BIT Z	LBM	K, X	16	18.3	14.9	11.5
LOAD A WITH (Z)	LDA	*, Y, X	16	10.2	6.8	3.4
LOAD BUFFER FROM MEMORY LOCATION Z	LDB	*, Y, X	N	10.2	6.8	3.4
LOAD FIELD FROM LOCATION Z	LDF	*, Y, X	N	18.3	14.9	11.5
LOAD INDIRECT FROM LOCATION SPECIFIED BY (Z)	LDI	*, Y, X	162	15.3	10.2	5.1
LOAD Z INTO A	LDK	*, K, X	97	5.1	3.4	1.7
LOAD ONE INTO BIT Z OF A	LDO	K, X	16	15.3	14.9	11.6
LOAD P FROM LOCATION Z	LDP	*, Y, X	16	10.2	6.8	3.4
LOAD Q FROM LOCATION Z	LDQ	*, Y, X	132	10.2	6.8	3.4
LOAD REGISTERS FROM MEMORY	LDR	*, Y, X	N	76.5	51.0	25.5
LOAD X-LOCATION FROM LOCATION Z	LDX	*, Y	21	15.3	10.2	5.1
LOAD ZERO INTO A	LDZ		16	15.3	14.9	11.6
LOAD MINUS ONE INTO A	LMO		16	15.3	14.9	11.6
LOAD P FROM LOCATION Z AND RESTORE	LPR	*, Y, X	16	10.2	6.8	3.4
LOAD X-LOCATION FROM COUNTER	LXC	X	21	15.5	10.2	5.1
LOAD Z INTO X-LOCATION	LXK	*, K	21	15.5	10.2	5.1
MOVE (A) TO Q	MAQ		179	15.5	14.9	11.9
MULTIPLY (Q) BY (Z) (24 X 24) (See Notes)	MPY	*, Y, X	300	22.7	19.3	15.9
NEGATE (A)	NEG		16	15.3	14.9	11.6
NO OPERATION	NOP		21	15.3	10.2	5.1
OUTPUT TO DEVICE FROM LIST Z	ODL	*, Y, X	N	65.7	51.3	41.5
OPERATE ON MEMORY FOR NEXT INSTRUCTION	OOM	*, Y, X	263+	15.3	10.2	5.1
OPERATE DEVICE Z	OPR	D, X	32	32.5	33.3	28.9
OR (Z) TO A	ORA	*, Y, X	16	10.2	6.8	3.4
OUTPUT TO DEVICE Z FROM A	OUT	D, X	32	32.3	33.3	28.9
PERMIT AUTOMATIC INTERRUPT	PAI		32	10.2	6.8	3.4
RESET BIT Z	RBK	K, X	16	15.3	14.9	11.6
REMOVE ITEM FROM BEGINNING OF LIST Z	RBL	*, Y, X	544	23.4	16.6	9.8
READ CONSOLE SWITCHES INTO A	RCS		32	10.2	6.8	3.4
REMOVE ITEM FROM END OF LIST Z	REL	*, Y, X	627	25.1	16.6	9.8
RESET TSTF IF BIT Z IS EVEN	REV	K, X	16	15.3	14.9	11.6
RESET TSTF IF (A) IS NOT ZERO	RNZ		16	15.3	14.9	11.6
RESET TSTF IF BIT Z IS ODD	ROD	K, X	16	15.3	14.9	11.6
REPEAT INSTRUCTION AT Z, X TIMES	RPT	*, Y, X	N	10.2	17.0	3.4
RESET TSTF	RST		16	15.3	14.9	11.6
SET BIT Z	SBK	K, X	16	15.3	14.9	11.6
SELECT DEVICE Z	SEL	D, X	32	32.3	33.3	28.9
SET TSTF	SET		16	15.3	14.9	11.6
SET TSTF IF BIT Z IS EVEN	SEV	K, X	16	15.3	14.9	11.6
SUBTRACT FIELD OF (Z) FROM A	SFA	*, Y, X	N	18.3	14.9	11.5
SUBTRACT Z FROM A	SKA	*, K, X	141	5.1	3.4	1.7
SHIFT LEFT ARITHMETIC, Z PLACES	SLA	K, X	878	10-18.4	14.9	3.4-11.6
SHIFT LEFT LOGICAL, Z PLACES	SLL	K, X	698	10-18.4	14.9	3.4-11.6
SET TSTF IF (A) IS NOT ZERO	SNZ		16	15.3	14.9	11.6
SET TSTF IF BIT Z IS ODD	SOD	K, X	16	15.3	14.9	11.6
STORE P AND BRANCH TO LOCATION Z	SPB	*, Y, X	16	10.2	6.4	3.4
SHIFT RIGHT ARITHMETIC, Z PLACES	SRA	K, X	16	15.3	14.9	11.6
SHIFT RIGHT CIRCULAR, Z PLACES	SRC	K, X	16	15.3	14.9	11.6
SHIFT RIGHT LOGICAL, Z PLACES	SRL	K, X	16	15.3	14.9	11.6

INSTRUCTION	SYMBOLIC CODING		EXECUTION TIME (μSEC) 4040	4050-I	4050-II	4060
SET STALL ALARM	SSA	*,Y,X	32	10.2	6.8	3.4
STORE (A) INTO LOCATION Z	STA	*,Y,X	14	10.2	6.8	3.4
STORE BUFFER INTO LOCATION Z	STB	*,Y,X	N	10.2	6.8	3.4
STORE FIELD OF A INTO LOCATION Z	STF	*,Y,X	N	23.2	14.9	13.2
STORE INDIRECT INTO LOCATION SPECIFIED BY (Z)	STI	*,Y,X	190	15.3	10.2	5.1
STORE Q INTO LOCATION Z	STQ	*,Y,X	132	10.2	6.8	3.4
STORE REGISTERS INTO MEMORY	STR	*,Y,X	N	76.5	51.0	25.5
STORE (X-LOCATION) INTO LOCATION Z	STX	*,Y	21	15.3	10.2	5.1
SUBTRACT (Z) FROM A	SUB	*,Y,X	16	10.2	6.8	3.4
TEST EVEN BIT Z AND RESET BIT Z	TER	K,X	16	15.3	14.9	11.6
TEST EVEN BIT Z AND SET BIT Z	TES	K,X	16	15.3	14.9	11.6
TEST BIT Z EVEN	TEV	K,X	16	15.3	14.9	11.6
TEST FIELD EQUAL	TFE	*,Y,X	N	18.3	14.9	11.5
TEST FIELD LESS	TFL	*,Y,X	N	18.3	14.9	11.5
TEST NOT MINUS ONE	TNM		16	15.3	14.9	11.6
TEST A NON ZERO	TNZ		16	15.3	14.9	11.6
TEST ODD BIT Z	TOD	K,X	16	15.3	14.9	11.6
TEST ODD BIT Z AND RESET BIT Z	TOR	K,X	16	15.3	14.9	11.6
TEST ODD BIT Z AND SET BIT Z	TOS	K,X	16	15.3	14.9	11.6
TEST AND SHIFT CIRCULAR, Z PLACES	TSC	K,X	16	15.3	14.9	11.6
TEST (X) HIGHER THAN OR EQUAL TO Z	TXH	K	14	10.2	6.8	3.4
TEST A ZERO AND COMPLEMENT	TZC		16	15.3	14.9	11.6
TEXT A ZERO	TZE		16	15.3	14.9	11.6
EXECUTE INSTRUCTION IN LOCATION Z	XEC	*,Y,X	14	15.3	3.4	1.7

Notes: The GE/PAC 4040 multiply time of 300 ms is for positive integers, 12 bit by 12 bit with a 24-bit product. For a signed integer, multiply execution is 458-514 μs. A 24 bit by 24 bit signed multiply with a 48-bit product requires 2010 μs on the GE/PAC 4040.

Without the step feature, the GE/PAC 4040 timing for the following instructions is —

Floating Multiply (non-multiply step option) FMP *, Y, X 3395 μsec
Multiply (non-multiply step option) MPY *, Y, X 4934 μsec

For instruction operations which vary in speed, average values are used.

Execution Times - Floating Point Arithmetic (microseconds) GE/PAC Central Processors

		4040	4040 with FPH	4050-I	4050-I with FPH	4050-II	4050-II with FPH	4060	with FPH
	FIX	448	448	318	318	228	228	131	131
	FLO	566	566	260	260	185	185	106	106
Single	FAD	947 to 1090	186	212 to 242	72	150 to 173	51	86 to 100	30
Word	FSU	977 to 1070	186	232 to 262	72	153 to 187	51	92 to 106	30
	FMP	1460*	186	256 to 266	78	185 to 192	58	108 to 111	36
	FDV	2631	186	309 to 329	83	227 to 240	63	137 to 143	41
	FIX	991		342		248		146	
	FLO	1129		503		361		206	
Double	FAD	3016		483 to 641		343 to 459		191 to 262	
Word	FSU	3046		498 to 656		352 to 469		196 to 266	
	FMP	7230		405		300		184	
	FDV	16081		565		427		272	
MEMORY REQUIREMENTS (words) - QUASI INSTRUCTION PACKAGE (Extended Function Commands)									
With Single-Word Floating Point		759	610	185	91	185	91	185	91
With Double-Word Floating Point		892		275		275		275	

*with MPY step
FPH is the auxiliary Floating Point Arithmetic Unit

VII GE/PAC 4000 SOFTWARE

INTRODUCTION

The "software" of a computer has been broadly defined as those parts of the system which are not "hardware". More specifically, it might be defined as the intelligence of the system, as embodied in a sub-system of programs, that directs the hardware portion of the system to the effective performance of the required functions. However, software includes not only the operational system program, but also all of the aids used by programmers to produce the system program.

Complete software packages have been developed for the GE/PAC 4000 series and are available to all users. These software packages are conveniently group into three categories: Program Preparation Aids, Standard On-Line Functions, and Utility and Debugging Aids.

PROGRAM PREPARATION AIDS

Program preparation aids consist primarily of symbolic languages and language processing programs designed to simplify the task of converting functional programming specifications into actual computer instructions. It is universally recognized that such language systems are essential to the efficient production of large and complex computer programs. General Electric has developed three such systems for GE/PAC 4000. For full flexibility and efficiency, versions of PAL and FORTRAN language processors are available to operate not only on GE/PAC 4000, but also on the GE 412 or on the GE 200 series computer systems. These enable routines to be assembled or compiled at any of the many General Electric Information Processing Centers throughout the country and overseas. TASC will operate on 412 to generate GE/PAC programs.

PROCESS ASSEMBLER LANGUAGE (PAL)

The Process Assembler Language processor is essentially a one-for-one translator of symbolic PAL-coded instructions into actual machine instructions. Use of the PAL system enables the programmer to work at the machine-language level (essential to the production of the most efficient possible programs) without being burdened by the tedious bookkeeping required for the assignment and remembering of actual memory locations of instructions and constants. Numerous pseudo-instructions are included to facilitate the generation of constants, allocation of storage, and symbol definition.

The PAL processor assembles programs which make full use of the relative addressing feature of GE/PAC 4000 with provision included for specifying absolute address assignment where necessary.

Excellent checking features are built in to detect many types of coding errors. Error codes are printed on the output listing of the assembled program.

An on-line version which functions within the framework of the G-E MONITOR system enables the assembly of programs concurrently with the operation of a system program.

FORTRAN

General Electric's FORTRAN II compiler for the GE/PAC 4000 translates the widely known and used FORTRAN II language into PAL symbolic language instructions. Thus, the benefits of compiler-generation of program from "statements" written in an easily-learned language employing familiar English words and algebraic formats are made available to GE/PAC 4000 users.

Many special features have been incorporated into General Electric's FORTRAN II compiler for GE/PAC 4000 to facilitate the generation of programs meeting the special requirements of real-time systems. The programs produced are fully compatible with the G-E MONITOR system, and special statement forms are included to take advantage of GE/PAC's bit-manipulation capability and to facilitate the specification of required transfers of data and subprograms between drum and core storage. A free intermixing of FORTRAN II statements and PAL coding is possible to further facilitate full use of GE/PAC capabilities.

An on-line version of FORTRAN II functions within the framework of the G-E MONITOR system.

TABULAR SEQUENCE CONTROL (TASC)

The General Electric TASC system is comprised of the TASC language, the TASC Assembler program, and a Table Analyzer Subroutine. It is designed for the efficient production of programs to control process operations of a sequential nature such as process start-up and shut-down.

The TASC language is designed to permit a rapid symbolic encoding of sequential control logic directly from standardized flow charts. The TASC Assembler then translates the symbolic coding of the TASC language into tabular numerical control codes.

Operating under control of the G-E MONITOR system, the Table Analyzer Subroutine controls the sequential operation of a system of subroutines as specified by the tabular control codes. The subroutines, which are specific to the individual system, perform the required scanning and control actions.

The TASC system is flexible, permitting an intermix of TASC and PAL coding, and is capable of producing programs which make choices between alternate sequences on the basis of process conditions as well as fixed-sequence programs.

STANDARD ON-LINE FUNCTIONS

The G-E MONITOR system provides the skeleton of a real-time system program, incorporating in a family of highly optimized routines those functions which are common to all real-time, on-line process control applications. Several versions of MONITOR are available, each tailored to the needs of a specific industry or process.

The functions included in the MONITOR package are those incorporating the major complexities of a system program. Primary among these functions are those of timekeeping, scheduling of system functions, drum-core transfers, and input-output. Inherent in these functions are the major "housekeeping" chores of saving and restoring registers for interrupted programs, allocation of core storage to currently-operating functional programs, and monitoring of functional priorities.

With MONITOR thus providing the "heart" of a system program, it becomes relatively easy to incorporate the specific functional routines required for a specific application. MONITOR is so constructed that each specific functional program can be written essentially as if it were a straightforward off-line program, with input-output and drum-core transfer functions provided by subroutines.

In addition to MONITOR, many compatible functional routines and standard mathematical subroutines are available from the G-E Programming Library. GE/PAC users are provided with up-to-date abstracts of all such routines as they are developed.

UTILITY AND DEBUGGING AIDS

A comprehensive family of utility and debugging aid programs is also maintained by the G-E Programming Library.

Load routines provide the means for loading programs and data into the computer memory through paper-tape or card readers. Dump routines list the contents of memory on typewriters or line printers or punch the contents of memory into paper tape in standard loading formats.

Memory Change programs change the contents of specified memory locations in accordance with requests made through use of the computer console switches or an input-output typewriter, providing a record on the console typewriter of the location and its contents before and after the change.

A well-rounded collection of these utility and debugging aids are included with each GE/PAC system in such a manner as to be operable under the control of an executive routine referred to as the Operator (OPR) Program, which simplifies the computer operator's usage of the routines.

Normally, the OPR system of utility routines is incorporated into the on-line system program as a spare-time function to permit their use concurrently with the system program. Under this arrangement, safeguards are incorporated to prevent accidental disruption of the system functions.

Debugging aids also include both on-line and off-line hardware diagnostic programs which help to localize hardware malfunctions. If used in a schedule of preventive maintenance, the routines can often detect component degradation in time to forestall system failures.

NOTE: Most of the software described in this section is now available. Check with the Process Computer Section for a complete schedule of availability.

NUMBER AND TYPES OF INTERRUPTS

FUNCTION	GE/PAC 4040	GE/PAC 4050/4060
System Clock	2/1/1	2/1/1
Ea Drum, Disc or Com Periph	1/0/0	1/0/0
Analog Input Scanner	1/0/0	1/0/0 or 3/2/1
Ea 100 CPM card punch controller	N/A	2/1/1
Ea Periph. Buffer-Opt. 1[1]	2/0/0	4/1/2
P. B. Opt. 2-all Input & I/O[2]	1/0/0	2/0/1
-Ea n Output devices[3]	m/0/0	m+t/m/t
Ea P. B. 350 cpm card reader	N/A	2/1/1
Ea Output Controller		
Opt. 1[4] (MO or TCO)	1/0/0	1/0/0
Opt. 2[5] (MO)	3/1/1	3/1/1
Opt. 3[6] (MO)	3/2/2	3/2/2
Opt. 4[7] (MO)	N/A	3/1/1

LEGEND

The three figures separated by slashes denote the number and type of interrupts required for each function listed

2/1/1
- the first figure is total number of API's
- the second figure is number of non-inhibitable interrupts
- the third figure is number of echo generators

NOTES:
1. One API all input and I/O devices except 350 cpm card reader; one API for all output.
2. Except 350 cpm Card Reader
3. m n; t = 1 or = m
4. Normal output option
5. Time Latching option
6. Pulsed option
7. DDC option

VIII GENERAL ELECTRIC CONTRACT MAINTENANCE SERVICE-DOMESTIC

Contract Maintenance Service utilizes engineers who have gained experience from maintaining other process computers or from installing our process automation systems. Contract Maintenance provides maximum availability of process computer systems with minimum cost of eventual take-over of maintenance. In many instances, the service engineer assigned to the maintenance of a system is assigned to the installation of the same system.

Features with General Electric Maintenance Contract:

1. Experience gained from installation and maintenance of previously installed systems is applied to each new system.

2. High reliability means customer maintenance personnel will only get occasional work experience on the computer. This eliminates need for expensive in-factory training.

3. Permits further training on operation of computer and test equipment.

4. Special system-type diagnostic techniques can be developed peculiar to the user's own system and operation. This would be beyond standard hardware and software aids which accompany the system.

5. Informal, practical, on-the-job operating assistance can be given, using the customer's own instruction books.

6. Reduces down-time and thus increases availability.

7. Simplifies parts problems by having General Electric work directly on the problem, thus affording prompter service. Parts and test equipment are optional extras.

8. Permits General Electric to provide closer statistical monitoring and alert the user to worthwhile improvements he should consider.

Three available maintenance contracts are:

CLASS I Resident Maintenance

CLASS II Maintenance - Fixed Price (Includes on-call emergency service)

CLASS III Maintenance - Variable (On-call service is excluded but is always available at standard rates)

I. CLASS I - RESIDENT MAINTENANCE

General Electric will provide a qualified service engineer who will perform preventive and corrective maintenance eight hours per day, five days per week. He will also be available to provide on-call emergency service outside of normally scheduled working hours. If desired by the customer, he will also conduct training for customer maintenance personnel during his normal working schedule.

II. CLASS II - MAINTENANCE - FIXED PRICE, OR CLASS III - MAINTENANCE - VARIABLE PRICE

Maintenance in this category will be conducted on a pre-determined schedule of service calls to perform annual, semi-annual, and periodic preventive and corrective maintenance as required.

On-call emergency service is included with a Class II contract. Class III does not include this service, but on-call service is always available as described in Section III.

General Electric will provide a qualified service engineer who will perform preventive and corrective maintenance conducted on the following schedule:

Schedule 1 - Visit once every three weeks (GE/PAC Class III, visit once every four weeks)

Schedule 2 - Once every three months

Schedule 3 - Once every six months, with the cycle to be repeated in the remaining six-month period.

SCHEDULE 1

The following items shall be performed during the Category 1 On-Line Preventive Maintenance (Frequency of visit - as listed above)

A. Mechanical

1. Inspect blower filters to insure continuous and adequate air flow through the system.

2. Inspect and clean typewriters, punches, and readers, so that they continue to operate to the required specifications (not included in Class III).

3. Thorough visual inspection of the entire system for faulty mechanical items. Replace or arrange for repair of any defective items as required.

B. Electrical

1. Utilize the on-line diagnostics in the system program for error detection.

2. Check in a systematic manner the computational and logic circuits for any signs of electrical marginal operation in such a manner so as to have checked the entire system at least once a year. This will greatly reduce circuit failures during on-line operation.

SCHEDULE 2 (Frequency of visit - once every three months)

On-line Preventive Maintenance

A. Mechanical

1. Check the computer blowers to determine if proper cooling will occur in the event of room air conditioner failure.

2. Lubricate motors as required to reduce possibility of bearing failure and excess noise operation.

3. Lubricate and adjust typewriters, punches, and readers so that they will continue to operate to specifications. (Not included in Class III.)

B. Electrical

1. Check cabinet temperatures for operation within the specified limits.

2. Check cabinet over-temperature sensors for correct operation and correct over-temperature limits.

3. Check in a systematic manner the computational and logic circuits for any signs of electrical marginal operation in such a manner so as to have checked the entire system at least once a year. This will greatly reduce circuit failures during on-line operation.

Off-line Preventive Maintenance

1. During the above systematic checkout, the components which show marginal operation are replaced.

2. Run the complete diagnostic package periodically to check the over-all computer performance.

3. Check all power supplied for voltage level and noise content and adjust or repair to maintain the proper voltage level and acceptable ripple content. Run accuracy and repeatability routines using known calibrated input sources and recalibrate analog circuitry, as required, to maintain correct system performance.

4. Run peripheral diagnostics to verify proper operation of the typewriter, punch, and readers.

SCHEDULE 3 (Frequency of visit - once every six months)

A. Mechanical

Same as Schedules 1 and 2

B. Electrical - On-Line Preventive Maintenance

The drum and core memories are checked and adjusted for proper READ/WRITE currents and timing to assure an adequate operating margin.

The above schedules, including all three classes and types of visits, is repeated during the second six-month period to assure that the entire electrical and mechanical equipment is properly checked in the course of a one-year period. The length of time involved during each of the periodic visits is a direct function of the amount of repair to be accomplished during any subsequent visit the replacement or arrangement for repair of any defective item is accomplished to completion, no matter how much is involved.

If while making an emergency on-call service visit, the General Electric engineer determines that a failure exists in customer equipment not covered by the Maintenance Contract, the customer will be billed at standard rates for services performed outside the scope of the contract. This applies to Class I and II maintenance.

CLASS IV - EMERGENCY SERVICES

On-call emergency service is available at the following rate:

1. For normal work week hour - first eight (8) hours, Monday through Friday - $16.00 per hour.

2. For overtime, next four (4) hours, Monday through Friday, and first twelve (12) hours Saturday - $20.00 per hour.

3. After first twelve (12) hours Monday through Saturday and all Sundays and Holidays - $24.00 per hour.

Actual travel and living expenses to be added to the above.

IX PROCESS COMPUTER SERVICES

Ordering a process computer from General Electric places a wealth of experienced technical talent at your service to provide a successful application. Many of these special services are included at no extra charge—others by contract at reasonable rates. Here is a summary of these services:

STANDARD SERVICES INCLUDED WITH A PROCESS COMPUTER

PROCESS COMPUTER SPECIFICATIONS (Pre-order)

In selecting the functions to be performed by the process computer system, a detailed understanding of the computer capabilities is necessary. Each function's value/cost relationship should be carefully considered to get the most value from the computer system. Experienced application engineers who understand the computer's capability and the process are available to help customers write the specification for a proposed process computer application.

PROCESS TIE-IN CONSULTATION (Post-order)

Systems engineers provide consultation to insure proper connection of the computer system to the process. All inputs from process sensors are inspected for noise conditions and appropriate recommendations made. Compatibility between the computer's electronics and the rest of the process system equipment is investigated to anticipate any interface problems. Buffering and isolation are suggested where necessary to insure system compatibility.

CUSTOMER TRAINING

Formal courses and on-the-job training are provided for customer personnel. The formal courses are:

Basic Programming - Basic application and programming fundamentals. Includes number systems, flow charting, and console familiarization.

Application & Systems Programming - Real-time system programming techniques for GE/PAC 4000. Includes discussion of MONITOR and real-time system class problem.

Maintenance Course - A ten-week course for qualified personnel which covers the operation of the computer system and trouble-diagnosing techniques. Two weeks are spent working on the computer.

Concepts Course - A two-day orientation course for executives, engineers, and plant personnel, usually given at the customer's location.

APPLICATION CONSULTATION

An experienced application engineer will be available to render assistance in the use of standard programming aids, to consult on problems of mathematical analysis, control techniques, installation tie-in, and to offer guidance on system modification or expansion.

PROGRAMMING CONSULTATION

An experienced programming analyst is available as required for consultation or to render assistance in the use of standard programming aids, or to assist in the development of new programming techniques. General Electric process computers have an excellent library of useful, pre-tested process-oriented subroutines and programming aids which are easily adapted to the customer's needs.

ANALYTICAL CONSULTATION

Analytical assistance is available to consult with customer's technical staff. For example, it may be desirable to call specialists in control system simulation analysis in for consultation. These discussions may reveal a special study will greatly aid the project (see Analytical Assistance Section).

SPECIAL SERVICES AVAILABLE AT REASONABLE RATES

INSTALLATION GUIDANCE

This service includes a pre-installation site preparation consultation as well as guidance during the actual installation of the system. Site preparation, cable routing, and computer installation are discussed to insure proper operation.

ANALYTICAL ASSISTANCE

Analytical assistance is available to supplement the skills within the customer's organization. The General Electric Company has developed an unexcelled

capability in industrial control system analysis and simulation. Detailed studies of process reactions have been performed on hot strip mills, continuous annealing lines, oxygen steel making, steam power plant, cement plant blending and kiln operations, paper machines, and many others. In many cases, simulations were developed on analog and digital computers to study and evaluate multiple-control techniques without the necessity of expensive process experimentation. These studies are performed by experienced analytical personnel in the Process Computer Section or in the analytical units at General Electric's Schenectady Works. The G-E General Engineering Lab may also be called on for developmental work for special sensors or equipment required to solve an industrial problem.

SYSTEM ENGINEERING

Experienced systems engineers can be called on to specify the system requirements for process control. Standard equipment is used where possible; but when special equipment is required, G-E engineers design it.

CONTRACT PROGRAMMING

Where the customer does not wish to do the programming for a process computer, the Process Computer Section assigns experienced real-time programmers on a contractual basis. Here the system specifications are implemented by programming analysts, programmers, and coders. They produce a completely documented operating program that can be conveniently modified or extended at a later date. Customer's personnel may work with these programmers as the program is being developed and thus be capable of maintaining the program in the field.

MAINTENANCE

Contract maintenance consists of three categories: resident maintenance, scheduled preventive maintenance, and on-call maintenance. Since process computers are designed to operate more than 99.5% of the time, resident maintenance is seldom justified. A combination of scheduled preventive maintenance and on-call maintenance is normally recommended. Comprehensive maintenance training courses are offered for customer personnel in Phoenix.

X CABLING PRACTICES

The GE/PAC 4000 process computer system is designed for precision operation in industrial sites. Filters are included on all analog inputs to attenuate electrical noise; but to obtain the ultimate benefit in accuracy, cabling to and from the system should be given the same care and forethought as for any accurate process instrument.

The following information is a summary of generally recommended practices. For a specific installation, General Electric specialists will consult with engineers responsible for cable layout. They can often suggest techniques which will give optimum results for the computer system at no appreciable increase in installation costs.

Cabling should always be installed in the best possible manner to protect it from excessive heat, moisture, and mechanical damage. It should be run in conduits or troughs so that it is completely supported and is not subjected to excessive flexing or bending. The troughs may be constructed of expanded metal. If conduit is required, the conduit should be laid out to avoid low points where moisture can accumulate.

Cabling should be routed to avoid coupling to sources of high-intensity electric transients. Intercabling may be subdivided into three major categories: power line, control and intra-system wiring, and analog data wiring. Each category should be isolated from the others to avoid interference problems. Isolation is the most effective means of preventing noise problems. If possible, each major category should be run in separate conduits or troughs and into separate cable entrances to equipment. If they must be run in the same trough, a partition should be installed for isolation.

All wire should be twisted to minimize induced pickup. Shielding is recommended to further reduce electrostatically coupled noise. The shield should be covered with an insulated sheath appropriate to the environment to which the cable is exposed. Single-braid copper shielding with 85% or higher coverage, or copper tape shielding, are considered to be adequate shields. On an existing installation, where analog inputs are not shielded, inputs should be individually investigated. Filtering included within the computer system should be adequate in the majority of cases. Rewiring expense will be held to a minimum with this procedure.

All equipment (such as cabinets, consoles, and data presentation cabinets) are to be connected to industrial or building ground. The grounding connection should be made with one-half inch (minimum) copper braid strap. The proper ground point for each cabinet will be recommended at the time of installation.

Cable entrance to the computer system is from the bottom or top through areas provided for that purpose. After installation, the entrances are sealed to prevent infiltration of dust. To facilitate cable handling, it is recommended that there be a cable trench under each electronic equipment cabinet.

Progress Is Our Most Important Product

GENERAL ELECTRIC

3/66 (5m) 8700

Litho in U.S.A.