ASSOCIATE
Technical Reference Manual
Revision 3.0

for

System versions 3.0

Direct Comments Concerning this manual to:

DATA TECHNOLOGY INDUSTRIES, SAN LEANDRO, CALIFORNIA

(415) 638-1206

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This Revision applies to:

ASSOCIATE Version 3.0
ASSOCIATE PLUS
1000 CPU Board Revision G and H
1005 CRT Board through Revision G
PROM Monitor Version 5.07
CRT PROM Version 1.7 through 1.A
Character PROM Version 5F and 60
Keyboard PROM Version 3, 4

The major change for Revision 3.0 is the name change to the ASSOCIATE. The ASSOCIATE is built by GNAT Computers Inc. and sold as the ASSOCIATE through Data Technology Industries. Systems having F revision boards should refer to manual revisfon 1.4 or 1.5.

Version 3.0 of the ASSOCIATE uses the H revision of the 1000 CPU board. The main changes on this board are in the area of the data separator which now uses a redesigned analog device to improve the reading of the double tracking disk drives on the ASSOCIATE PLUS.

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Printed in the United States of America

APPENDIX 1. REVISION STATUS

This Manual Revision applies to:

ASSOCIATE Revision 3.0	PROM Monitor 5.06, 5.07
CRT PROM Version 1.7, 1.8, 1.9, 1.A	Character PROM 5F,60
Keyboard PROM Version 4	CP/M and Bios Rev: 2.2.4

File name (.COM if not specified)	Version Number	Vendor
ASM	2.0	C
BANR	2.00	U
BAUD	2.0	U
COMPARE	2.02	U
COPY	2.03	U
D	3.01	U
DDT	2.2	C
DUMP	2.10	U
ED	n/a	C
EJEC	1.2	U
FORMAT	3.47	U
FREE	1.0	C
INITSYS	1.53	U
LOAD	n/a	C
PIP	1.5	C
PRINT	2.03	U
SIOPORTS.LIB		U
STDDEFS.LIB		U
STAT	n/a	C
SUBMIT	n/a	C
SYSGEN	2.05	U
T9511	2.1	U
TAPE	1.9	T
TBAUD	1.0	T
TCRT	1.6	T
TCTC	1.2	T
TDISK	2.12	T
TDMA	1.04	T
TIME	1.05	T
TINT	1.02	T
TPAT	1.00	T
TPIO	1.02	T
TRS232	2.03	T
TRTC	1.02	T
TSERIAL	1.02	T
TSPD	1.0	U
VPRINT	1.0	U
WM (optional)	1.07A	
WM.HLP	1.07A	
XSUB	2.0	C

C = CP/M Utility, U = ASSOCIATE Utility, T = ASSOCIATE Test Routine

ASSOCIATE FEATURES

GENERAL

- Attractive Desktop Cabinet
- Portable
- Selectric Style Keyboard
- Software Definable Function Keys
- Accounting Style Numeric Pad
- Low Glare Screen
- Full Screen Editing

HARDWARE

- Z80A CPU
- 65K RAM
- 700K Mass Storage on Dual Minifloppys
  - Optional 1.6 Megabytes
  - Optional Hard Disk
- DMA Data Transfer
- Hard Disk Interface for Additional Mass Storage
- 2 RS232 Serial Ports (Printer and Modem)
- 1 RS449 Serial Communication Port to 500K Baud
- Programmable Baud Rates
- Separate CRT Microprocessor
- IEEE 488 GPIB Parallel I/O*
- High Speed Arithmetic Processor*

SOFTWARE

- PROM Resident Disk Boot and Diagnostic Monitor
- CP/M** Version 2 Disk Operating System
- Screen-Oriented Editor
- Word Processing Program*
- Business Software*
- Communications Software*
- Extensive Software Support*

BASIC	FORTRAN	PASCAL	RATFOR
COBOL	ASSEMBLER	PL/1	"C"

*Optional

**Trademark of Digital Research

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1000 CPU Board Schematic Diagram - 5 pages
1005 CRT Board Assembly Diagram
1005 CRT Board Schematic Diagram

B. Engineering Change Orders

OPTIONAL INFORMATION - Available To Qualified OEM's

BIOS Assembly Listing
GNAT Monitor Assembly Listing
Video Processor Assembly Listing
Keyboard PROM Listing
Character Generator PROM Listing

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Bowles, Kenneth L. "Problem Solving Using PASCAL", Springer-Verlag

Jensen, Kathleen and Niklaus Wirth. "PASCAL User Manual and Report" Springer-Verlag

REFERENCED DATA SHEETS

MOSTEK Z80 Handbook
INTEL MCS 80 Users Handbook
CP/M Disk Operating System Manual
WordMaster Screen Editor Manual
Advanced Micro Devices
  9517A DMA Controller, 9511A APU, 26LS30 RS449 Driver
  26LS32 RS449 Receiver
Mostek 4116 RAM
Western Digital 1793 Disk Controller
Texas Instrument 9914 IEEE Controller
Tandon TM 100-2 Disk Drives
C.ITOH CRT Monitor
Intel 8251 USART; 8155 RAM, Timer, I/O
Boschert 0L65 Power Supply or OSC OS65 XL Power Supply
Keytronics Keyboard
Corcom 6J4 Line Filter or 6J1, 3V1 Corcom

Chapter 1

INTRODUCTION

Purpose

This reference manual provides a detailed operating description of the ASSOCIATE. It is intended for technical users and contains complete information on modification, operation of optional features, interfacing to other devices, and services available to the System 10 user. Another publication, the ASSOCIATE Operator's Handbook, should be referred to for standard operation and an overall view of the ASSOCIATE.

The ASSOCIATE

The ASSOCIATE is a full function microcomputer built for the small businesses, communication, and front end terminal applications.

Extensive I/O capabilities include three RS232 Ports, one of which alternatively can be configured as RS449, an optional IEEE 488 Bus interface, and a high speed parallel interface for a hard disk. The I/O enables the ASSOCIATE to be a useful tool for laboratory, commun-ication, and mass storage functions. With the Communications Software Package, the ASSOCIATE becomes an excellent "Smart Terminal" for mainframe preprocessing and data entry.

A wide variety of software is available for use on the ASSOCIATE. Extensive business software is available through the Business Software Library; specialized business software can be custom written for users with particular requirements.

With CP/M, BASIC, Fortran, and assembly language, software can be easily developed on the system by OEM's for their specialized applications.

The word processing software features full screen-oriented editing, cursor movement control, and automatic file management. The function keys are defined for operations such as line delete, file up 1 screen, and move right 1 word.

Optional word processing software provides right-hand margin control, proportional spacing, and paging. These features plus others make the ASSOCIATE an outstanding computer for business and documentation purposes.

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Chapter 2

SYSTEM ARCHITECTURE

This chapter contains information about the architecture of the ASSOCIATE, both electrical and logical.

Different components of the system and their interconnections are illustrated in Figure 1, "Functional Block Diagram." A full representation of the electrical and logical architecture is contained in the schematics included as Appendix A. As will be noted, boards are designed for maximum utilization of the board and system area.

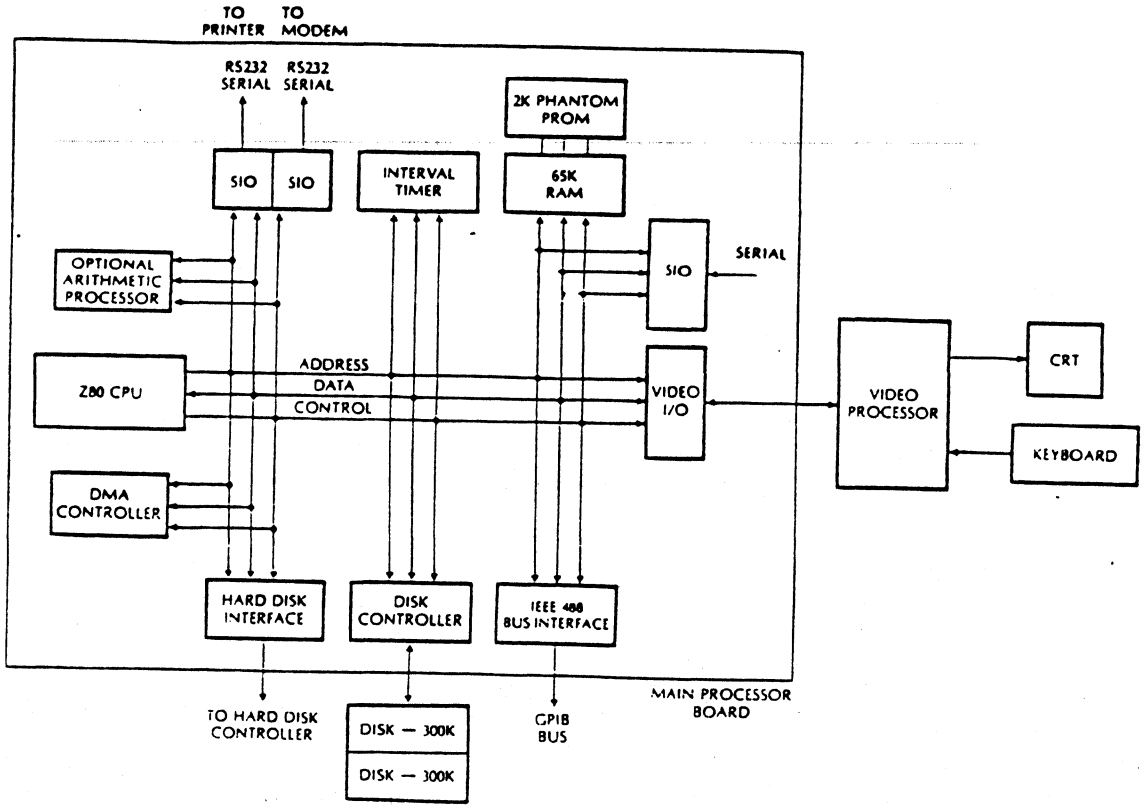


Figure 1. Functional Block Diagram

2.1 Electrical--A/C Wiring and Power Supply

The ASSOCIATE uses a switching power supply. Specifications for the power supply are as shown in Table 2-1.

Table 2-1. Power Supply Specifications

Voltage	Current Rating
+12	.5 AMP
-12	.15 AMP
+ 5	6 AMP
+12	1.8A (3 Amp Surge) (Disk Drives)

The supply is sufficient for internal operation, however, it is not recommended that peripheral devices requiring more than 0.5 amps at +5 or 0.1 amp at +- 12 volts be powered by this supply. For details on the power supply connection see "System Wiring Diagram" in Appendix A.

2.1.2 110/220 Option

The ASSOCIATE may be wired for 220 volt operation as outlined below. These changes are to installed by a qualified technician only. Failure to strictly observe all items may cause considerable damage to the computer and void the warranty on the unit.

220 Volt Set Up

1. Remove Jumper JP1 from the system power supply if supply is a Boschert or set switch to 220 volt position for the OSC supply. The power supply is located below the disk drives. See Section 8.3 for access instructions.

2. Remove and reinstall voltage selector card to the 240 volt position. This card is located on the AC connector at the rear of the unit. Note: This must show the 240 volt label toward the top.

3. Plainly label the system above the AC connector as being modified for 220 volt operation.

2.1.3 Line Filtering

The incoming A/C line is filtered with a capacitive inductive line filter. This reduces the system's susceptibility to extraneous RFI and also suppresses emissions by the system itself.

2.2 CPU Board

Central to the ASSOCIATE CPU Board is the Z80 microprocessor which is completely supported by a number of features including 65K RAM memory, AM9517 DMA Controller, Floppy Disk Controller, 4 Serial I/O Ports, and optional items - Parallel I/O, AM9511 or AM9512 Arithmetic Processor, Real Time Clock, and IEEE 488 I/O. A complete view of the CPU board is available in the "Assembly 1000 CPU" in Appendix A. The CPU board is built to fully utilize the capability of the Z80 microprocessor through extensive use of intelligent support controllers. Memory, CPU, and general purpose system features are described in this chapter; I/O features are described in Chapter 3.

2.2.1 Memory

The CPU board contains 65K of Read/Write RAM and a 2K PROM overlay controlled by restart hardware and software.

On RESET the system comes up in restart mode, which disables RAM and enables PROM until code in the PROM monitor at F800H enables RAM. The first instruction in the PROM is a JMP to "BEGIN". The second instruction, an OUT D0H, which enables RAM, thereby giving an initial operating configuration of 63K RAM and 2K PROM. The OUT D0H also sets the modem baud rate. The memory is normally reconfigured under the Disk Operating System to 65K RAM and 0K PROM. See Section 3.11 Status and Control for operational details.

The PROM Monitor normally loads the Disk Operating System upon power up or reset. The Disk Operating System can then immediately execute a user program. This capability gives users, without technical expertise, the ability to start the system and immediately run a dedicated program; it also provides the opportunity to go directly back into an application program after a power failure.

The physical layout of memory, in terms of address range and bit number, is illustrated in the "Assembly 1000 CPU" in Appendix A. Thus, if memory fails the memory test (operator command T under Section 7.1), the location of the particular memory chip to be replaced can be quickly determined from the assembly diagram.

Several areas of memory are used for various functions by the Monitor and Operating System. These are:

Table 2.1 Memory Assignments

0000H-0002H	Jump to PROM Monitor or Jump to BIOS + 3 in Operating System (Warm Boot)
0003H	I/O assignment byte
0004H	Current logical disk number and user number
0005H-0007H	BDOS entry in Operating System (locations 6 and 7 are top of user RAM in both monitor and DOS)
0008H-000AH	Unused

000BH	Latch port status
000CH	System Status (Reserved)
000DH	CRT line counter (Reserved)
000EH	Extended IOBYTE
000FH	Reserved
0010H-001FH	Interrupt Vectors Ports 72H, 70H, (SIO)
0020H-0027H	Interrupt Vectors Ports 20H, 21H, 22H, 23H (CTC)
0028H-002BH	Unused
002CH-002FH	Interrupt Vectors Ports 50H, 52H, (PIO)
0030H-0037H	Unused - reserved by CP/M
0038H-003AH	Jump to PROM Monitor Trap Entry
003BH-003FH	Unused - reserved by CP/M
0040H-004FH	Interrupt Vectors Ports 62H, 60H, (SIO)
0050H-007FH	Unused - reserved by CP/M
0080H-00FFH	DOS Boot loader

In Monitor Operation:

-F7D9H	Monitor Stack
F7D9H-F7F0H	Monitor Workspace
F7F1H-F7FFH	Trap Exit Code
F800H-FFFFH	PROM Monitor

In DOS Operation: (61K)

0100H-D7FFH	Normal User Area (TPA)
0800H-DFFFH	Console Command Processor (CCP)
EE00H-EDFFH	Disk Operating System (BDOS)
EE00H-FFFFH	System I/O Drivers (BIOS)

2.2.2 Reset

After a RESET the PROM monitor will attempt to load the first 128 bytes of Track 0 Sector 1 from the disk in the lower drive (A) into memory beginning at location 80H. This will normally be a boot for the Disk Operating System. If a the Disk Operating System is not found, a second reset will take the system to the monitor command level. Two resets in rapid succession will also take the operator to the monitor command level.

There are four ways of generating a RESET in the ASSOCIATE:

1. Manual - This RESET is generated by momentarily depressing S1 on the main CPU Board (see "Assembly 1000" schematic); S1 is accessible on the back right of the unit. This resets both the CRT and the Main Processor.

2. Keyboard - This RESET is generated through the video processor by keying in the Control-Shift-RST. This resets only the main CPU Board and not the video processor.

3. Power Failure - This RESET is exactly the same as the Manual RESET. It is activated by power detection circuitry when a power fail is detected. This feature is on 1000G and later CPU boards.

4. Software - The two software reset functions are defined in Section 3.11, Internal Status and Control; these resets affect only the floppy controller and the 9511 Arithmetic Processor.

2.2.3 System Timing

The main system timing is derived from a 16 MHz oscillator. This is divided for distribution to the 8 MHz, 4 MHz, 1 MHz, and 1/2 MHz signals used throughout the board. The most used signal for system timing is 4 MHz; this signal has the necessary circuitry to insure that the Z80A has the required levels and transition speed for proper clocking.

Baud rate generation for serial ports is accomplished through a separate crystal; the frequency of that crystal (4.9152 MHz) is an even multiple of standard baud rates. A dual software programmable divider described in Section 3.13 gives the actual baud rates to the serial I/O devices.

Circuitry is provided on the board to take care of the disk drive timing requirements. The following digital delays are used:

Motor Turn On. If the drive motors are off, a one second delay is introduced in the head load command to allow time for motor startup.

Motor Turn Off. If the floppy disk controller is not accessed for 128 seconds the disks are deselected and the motor on signal is deactivated. The disk motor turn off timing may be optionally set at other values as follows:

JP35 Motor Turn Off Delay

Pin 5 jumpered to pin 6	128 second (normal)
Pin 3 jumpered to pin 4	64 second
Pin 1 jumpered to pin 2	32 second
All open	No turn off

Screen Blanking. The CRT display will be turned off 20 minutes after the last CRT activity. The purpose of this turn off is to extend CRT phospher life. The timeout is user programmable - See Section 5.2 for the procedure. The screen will turn back on when any keyboard key is pressed or the CPU sends a character to the video processor.

2.2.4 CPU & Instruction Set

For detailed information on the Z80 microprocessor refer to "MOSTEK Microcomputer: Z80 Data Book." Based on N-Channel MOS technology, the

Z80A-CPU is packaged in an industry standard 40-pin Dual In-Line Package. Significant features include a single power supply (+5V), a single system clock signal, multiple interrupt capability, and dynamic memory refresh.

Software generation on the ASSOCIATE is simplified through the Z80's 158 instructions, unlimited subroutine nesting, vectored interrupts, and DMA capabilities. Product development and system design are enhanced by the extensive set of instructions and the varied addressing modes of the Z80, as well as its capability of directly addressing 65K 8-bit words of memory. For a detailed description of the Operating System software aids for assembly program production, refer to the "CP/M Disk Operating System Manual."

The Z80 maintains full software compatibility with the 8080 microprocessor, since the Z80 instruction set is a superset of the 8080 instruction set. The Z80 has additional addressing modes, a larger instruction set, and extended registers.

The internal architecture of the Z80 consists of eighteen 8-bit registers, four 16-bit registers, arithmetic and logic unit (ALU), and instruction register.

2.2.5 CPU Jumper Table

The following table summarizes the jumper options for the G and H revision CPU board.

Table 2.3 Jumper Definition and Defaults for 1000G,H CPU

JP #	PG #	DEFAULT	NAME-FUNCTION
1	1	used	pins 1 and 2 used by inverter in reset
1	1	open	pin 3 O.C. reset output
1	4	open	pin 4 O.C. /inen from 74S287 - PIO Control signal
1	4	open	pin 5 O.C. /outg from 74S287 - PIO Control signal
1	4	open	pin 6 O.C. /wait from 74S287 - PIO Control signal
1	4	open	pin 7 O.C. /tack from 74S287 - PIO Control signal
2	4	open output	pin 2 open 8304 PIO port A output mode
	4		pin 2 to 1 8304 PIO port A input mode
	4		pin 2 to 3 8304 controlled by latch bit D2
3	4	open	74S287 address inputs-1 to 2 A5 to B7
	4		3 to 4 A6 to B1, 5 to 6 A7 to B0
4	4	open	PIO port B data D0-D7
5	4	open	PIO port A data D0-D7
6	4	open	parallel DMA port data D0-D7
7		open	pin 2 P2 pin 49, pin 1 +5volts, pin 3 ground
7A	3	enabled	network I/O J1 Remote Gnd to chassis ground
7B			no connection
7C	3	open	network I/O pin 8, Carrier Detect Signal
7D	3	open	network I/O pin 17, RSET
8	3	2-3 grounded	RS422 input option, Network Receiver Option
9	3	2-3 grounded	RS422 input option, Network Receiver Option
10	3	2-3 grounded	RS422 input option, Network Receiver Option
11	3	1-2 RS423	1-2 26LS30 in RS423 mode, 2-3 in RS422 mode
12	3	2-3 grounded	RS422 input option, Network Receiver Option
12A	3		RS422 input option, Network Receiver Option
13	3	open	1-2 list/network port -12volts on pin 10
		open	3-4 list/network port +12volts on pin 9
13A	3	enabled	list I/O J2 Remote Gnd to chassis ground
13B	3	open	list I/O pin 6, Data Set Ready signal
14	3	2-3 RS423	26LS30 Vee 1-2 ground of RS422, 2-3 -5volts for RS423
15	3	open	1-2 modem port -12volts on pin 10
		open	3-4 modem port +12volts on pin 9
15A	3	enabled	1-2 modem I/O tset signal
		enabled	3-4 modem I/O rset signal
15B	3	open	modem I/O pin 8, Carrier Detect signal
15C	3	enabled	modem I/O Remote Gnd to chassis ground
16	4	1,2,3, open	1 ground, 2 active low parallel output enable, 3 PIO port B bit 0 for output control
16	4	4-5	output enable active low,4-2 for active hi
16A	4	6-7	6-7 for /dreq0 from PIO port B bit 3
17		not used	
18	4	open	PIO strobes-1 astb, 2 bstb, 3 ardy, 4 nc, 5 brdy
19		not used	
20	3	test points	pin 1 console serial receive data, pin 2 xmit data
20A	3	open	SIO 1 sync A
21	3	1-2 sclk0	SIO 0 A Modem receive clock
22	3	1-2 sclk1	SIO 0 B List Device clock
22A	3	open	SIO 0 rtcb 1-2 to tset driver to list pin 15
		open	SIO 0 rtcb 3-4 to rset driver to list pin 17
23	3	1-2 sclk0	SIO 0 A Modem xmit clock

24	5	open	1793 pin 29 TG43
25	4	1-2 enabled	IEEE488 data bus enable
26		test points	data bus D0-D7
27	3	1-2 sclk0	network clock internal, 2-3 for external
28	3	1-2 RS232	network I/O txd inversion, 2-3 for non inversion
29	3	1-2 RS232	network I/O dtr inversion, 2-3 for non inversion
30	3	1-2 RS232	network I/O cts inversion, 2-3 for non inversion
31	5	2-3 01	1793 clock, 1-2 for 02 speed
31A	3	open	SIO 1 sync A
32	4	open	RTC /stdbyint
33	5	1-2 enabled	disk ready input
34	1	open	spare inverters in IC 4N
35	5	5-6 128 sec	motor off delay, 3-4 for 64 sec, 1-2 for 32 sec
35A	5	open	1 62.5Khz clock, 2 500Khz clock
36	5	open	status input buffer bit 5, IC 5L 74LS244
37			Drive Side Source Select
38		not used	
39			Double Density Jumper, Single Density Open
40	1	open	/nmi Z80 CPU signal
40A	1	test points	1 /rd, 2 /wr Z80 CPU signals
41	1	1-2 02	9517a clock, 2-3 for 01
41A	1	test point	/busak Z80 CPU signal
41B	1	open	spare nand gate IC 6S
42	1	open	1-2 spare input to /dint3
	1	3-4	3-4 9511 /end to /dint2
	4	open	5-6 /exwait to /wait
	1	open	7-8 9511 /svreq to /dint2
	4	9-10	9-10 rtcrdy to /wait
	1	open	11-12 /rtcint to /dint3, RTC Interrupt
	4	13-14	13-14 /pause to /wait
	1	15-16	15-16 /i to /dint2 (external interrupt)
	1	17-18	17-18 /ieee to /dint3
43	5	open	disk I/O connector spare pins
44	5	test point	/raw data

In the above table: O.C. = Open Collector Output
/ in front signal name indicates inverted signal

Chapter 3

INPUT/OUTPUT

The I/O addressing field of the ASSOCIATE is entirely committed on the main CPU Board: there is no provision for direct external user access to the Z80 data bus. Communication with the external world is handled through the five connectors located at the back of the unit. The file SIOPORTS.LIB on the system distribution diskette contains further information on the standard port names and assignments.

Table 3-1 below describes the address range and assignments of devices addressed through the I/O instructions.

Table 3-1. I/O Addresses and Assignments

Address	Signal Name	Function
00H-0FH	S9517	DMA Controller
10H-1FH	S9511	Arithmetic Processor
20H-2FH	CTC	Interrupt Controller, Timer
30H-3FH	S9914	IEEE 488 Controller
40H-4FH	PDMA1	Parallel DMA Data Port 1
50H-5FH	PIO0	Parallel I/O
60H-61H	SIO1	Network I/O RS449
62H-63H	SIO1	Console (CRT)
70H-71H	SIO0	Modem RS232
72H-73H	SIO0	List RS232
80H-8FH	S1793	Floppy Disk Controller
90H-9FH	PDMA0	Parallel DMA Data Port 0
A0H-AFH	LATCH	Status and Control
B0H-BFH	RTC0	Real Time Clock 0
C0H-CFH	RCTC1	Real Time Clock 1
D0H-DFH	BAUD0	Modem Clock, RAM on Control RS449 Clock
E0H-EFH	BAUD1	List Clock
F0H-FFH	Not Used	

Refer to the specific Data Sheet for I/O sub-maps and operational details of a particular device.

3.1 DMA Controller 00H-0FH

The DMA Controller is an Advanced MicroDevices AM9517A chip. This chip provides direct memory access to system memory (through four channels) for the following high-speed devices:

1) High speed Parallel I/O (Channel 0)
2) Floppy Disk I/O (Channel 1)
3) IEEE Bus Interface (Channel 2)
4) Network Serial I/O (Channel 3)

The fourth channel can also be used for memory to memory transfer. For further details concerning the DMA Controller, refer to Advanced MicroDevices AM9517A data sheet.

The AM9517A uses all 16 addresses of its block of 16; it is further divided into four blocks of two addresses each, where each block of addresses corresponds to one channel of DMA control. This is followed by a sub-block of control registers occupying eight addresses. For each channel, the function of the addresses are:

1) Base current address

2) Base current word count

3.2 Arithmetic Processor 10H,11H

The Arithmetic Processor Option 9511/9512 provides the ASSOCIATE with a complete high performance arithmetic processor. It considerably enhances the arithmetic computational speed of the system and includes not only floating-point, but fixed-point processing as well. In addition to add, subtract, multiply, and divide operations the 9511 includes transcendental functions and control and conversion commands.

The 9512 is a four function (add, subtract, multiply, and divide) processor which provides single precision (32 bit) and double precision (64 bit) operations in the IEEE floating point standard. This option is specified as APU-2 when ordering.

The Arithmetic Processor occupies two address locations (10H and 11H) in the Z80 addressing field. Operation requires that the operands be written on the processor's stack at location 10H followed by the issuance of a command to the command word at location 11H. Two, four, or eight byte values are written with the least significant byte first. All required bytes must be read or written in sequence for proper operation. The desired operation code is then output to the Processor command port (11H) and the processor will calculate the result. The result can be read after completion at port 10H most significant byte first.

Completion of the processing is indicated in two ways. Port 11H serves as the status register which can be read for completion status; or the end of processing may be signaled by an interrupt.

The pause jumper JP42 must have pins 13 and 14 jumpered for proper operation with the 9511 or 9512. This jumper will cause the Z80 to enter a wait state in order to synchronize the slower read and write timing of the APU.

The user is cautioned that no attempt to read the result of the calculation should be made before the calculation is complete. The wait timeout logic will override the APU and an invalid result will be returned.

There is a jumper option for interrupt and wait operation of the Arithmetic Processor. The AM9511 uses DINT2 (interrupt 2 into the interrupt controller); that interrupt is normally driven by the END function and by a service request. Three jumper options are available for use with the APU as described below:

Jumper Pin JP42 APU Jumper Options

Pin 13 Jumpered to 14	APU Pause generates CPU Wait
Pin 7 Jumpered to 8	APU SVREQ activates Interrupt 2
Pin 3 Jumpered to 4	APU END activates Interrupt 2

The Arithmetic Processor may be reset under software control at any time. It is sent a reset by the power up sequence. A zero in Bit 3 (APURES) of the Control Word at Address A0H resets the APU. The APURES bit should be held to zero for 50 microsec. When using this reset be sure to get the status of the control latch from location 000BH in memory for the setting of the other bits in the control word.

Two sets of standard software are supplied on diskette with the APU option. These are the 9511 test routines and the 9511 Fortran Library subroutines. The file containing the test routine source is named TAPU.MAC. It is written in Z80 assembly code.

The Fortran Library subroutines are in the file APU11.REL. These can be linked into a Fortran program by linking this file in front of the FORLIB.REL. The APU11.REL file contains the following entry points, normally taken from the FORTRAN library:

Table 3-2 APU11.REL Subroutine Library Functions

ENTRY POINT	FUNCTION
RSTAPU	Perform APU Reset
$aa	add real and integer
$ab	add real and real
$da	divide real by integer
$db	divide real by real
$ea	exponentiation of real by integer
$eb	exponentiation of real by real
$ma	multiply real by integer
$mb	multiply real by real
$sa	subtract integer from real
$sb	subtract real from real
$ca,float	convert integer to real
$ch,int,ifix	convert real to integer

sqrt	real square root	acos	real arccosine
sin	real sine	atan	real arctangent
cos	real cosine	alog10	real log base 10
tan	real tangent	alog	real log base e
asin	real arcsine	exp	real e**x

3.3 Interrupt Controller and Timer 20H-23H

The Interrupt Controller provides system timing and manages inputs for the various interrupts that can be generated by other I/O devices. For detailed information refer to the Data Sheet on the MK3882/Z80A CTC. The Interrupt Controller can do three different subsets of operations:

1. Direct Interrupt Controller. The four devices which utilize the CTC for interrupt control are connected to the trigger inputs as follows:

   a. DMA Controller Interrupt Request-Trigger 0
   b. Floppy Disk Controller/ -Trigger 1
   c. 9511 Arithmetic Processor/ -Trigger 2
      Power fail
   d. IEEE Bus Controller/ -Trigger 3
      Real Time Clock

2. Interrupt Priority Enabling. The CTC is the highest priority device on the interrupt enable daisy chain. The PIO is the second device, SIO #1 is third, and SIO #0 is lowest priority.

3. Timer Operation. Any of the four CTC channels may be used as a timer its corresponding trigger input is not enabled. The slowest frequency timeout available is 62.5 Hz.

See Section 2.2.1 Memory for the memory map recommended for the interrupt vectors.

3.4 IEEE - 488 GPIB 30H-37H

The IEEE 488 GPIB Interface Option gives the ability to communicate over the general purpose interface bus. The option is designed around the Texas Instrument TMS 9914 GPIB Interface chip. The 9914 allows operation as a bus controller or as a listener/talker. A complete description of this chip and an introduction to the bus itself are given in the 9914 data sheets.

Sample software for use on the GPIB is supplied on diskette with the option and summarized in this manual.

The TMS 9914 occupies a block of 8 addresses in the addressing field. These addresses are 30H to 37H. A complete description of the function of each of these addresses is given in detail in the TMS 9914 data sheets.

A jumper option is available on the CPU board to either enable or disable a resistor termination network for the GPIB. As the ASSOCIATE is normally expected to be at the end of the GPIB cable, the termination resistor network is normally enabled. The termination enable option is JP25 located next to IC2B.

Jumper JP25 Terminator Enable

1 jumpered to 2	Terminator enabled. (Normal)
2 jumpered to 3	Terminator disabled. Clad on back of board between pins 1 and 2 must be cut!

The IEEE controller may be operated under interrupt control on CTC channel 3. This option is control at Jumper Pin Block JP42 as described below. The 9914 must be programmed to generate the desired interrupt output on pin 9 and the CTC must be programmed to use channel 3 as an external interrupt input.

Jumper JP42 IEEE Interrupt Request Option

17 jumpered to 18	Interrupt connected. (Normal)
17 open to 18	Interrupt not connected (clad on board must be cut)

The 9517A hand shake lines DREQ2 and DACK2 will perform data transfers between the 9914 and memory as programmed by the third DMA controller channel. Use of this feature requires the appropriate programming to be done for the 9517A DMA Controller chip.

With the GPIB option, sample software is provided for demonstration of its use. Currently, three sets of software are provided on disk. The first set is a collection of subroutines which may be called from Basic or Fortran. These subroutines illustrate how to initialize the TMS 9914 and how to put data on the bus and take data off the bus. The file names are:

488SUBS.DOC	Documentation file
488SUBS.MAC	Subroutine source code

The second sample software is a Rational Fortran (RATFOR) program which is used to transfer data from a IEEE 488 tape deck to the microcomputer's floppy disks. This program named TAPE488.RAT uses many of the utility subroutines described above.

The third set of sample software is a program to test the IEEE port. The T488.MAC tests the IEEE-488 option and demonstrates the use of DMA and interrupts with the 9914 device. In order for the T488.MAC to run, a second ASSOCIATE connected to the system under test must also be running the T488.MAC program.

3.5 High Speed Parallel I/O 50H-53H, 90H, 40H

High speed parallel I/O is optionally available through the rear panel connector P2 for interfacing to such devices as a hard disk. The interface consists of two 8-bit bidirectional data channels and eight-bits of control signals. These functions are provided by an MK3881/Z80A-PIO, bidirectional drivers and a 74S287 control PROM. This PROM can be defined for the application the parallel port is used on. A resistor pullup network is normally installed if the PROM functions are not required.

Several options are available for operating the parallel interface in different modes for different devices. These include jumper pin blocks JP1, JP2, JP3, JP4, JP5, JP6, JP7, and JP16. See Schematic and Assembly drawings for details.

DMA control signals from Port 90H and DMA channel 0 are used as inputs for the control PROM.

WAIT LOGIC (IC1B) allows external devices to hold the system bus for up to 15.5 microseconds during CPU or DMA data transfers. It may also be controlled by the 74LS287 PROM and jumper options.

Further details on configurations for different external devices will be given in Application Notes for those devices.

Definition of Pinouts of the external connector is listed in the following table; all signals are active low.

Table 4-3. Parallel I/O

Pin #	Name	Function
1	PC0	Parallel Control Signal
3	PC1	Parallel Control signal
5	PC2	Parallel Control Signal
7	PC3	Parallel Control Signal
9	PC4	Parallel Control Signal
11	PC5	Parallel Control Signal
13	PC6	Parallel Control Signal
15	PC7	Parallel Control Signal
17	PD0	Parallel data 0
19	PD1	Parallel data 1
21	PD2	Parallel data 2
23	PD3	Parallel data 3
25	PD4	Parallel data 4
27	PD5	Parallel data 5
29	PD6	Parallel data 6
31	PD7	Parallel data 7
33	HD0	High Speed Parallel Data 0
35	HD1	High Speed Parallel Data 1
37	HD2	High Speed Parallel Data 2
39	HD3	High Speed Parallel Data 3
41	HD4	High Speed Parallel Data 4
43	HD5	High Speed Parallel Data 5
45	HD6	High Speed Parallel Data 6
47	HD7	High Speed Parallel Data 7
49	SPARE	Spare (+5 volts optional)
2-50 EVEN	GND	Ground

When installing the PIO option, cut JP18 6 from 7. With the PIO not in the system, this jumper is necessary to pass interrupt requests through to the interrupt controller.

3.6 Network I/O 60H, 61H

This serial output port provides I/O for network communication applications with RS449 protocol. This protocol provides several features not available in RS232: higher speed and differential drive. The RS449 is a combined specification for RS422 and RS423. The following description is in terms of the RS422 and RS423.

Port 60H is data and Port 61H is status and control. The Network I/O baud rate is software programmable by the baud rate generator addressed at Port D0H and described in Section 3.13. Note that its clock is shared by the modem port. When used with the serial manifold external clocking should be selected using JP17. The Network Port can also be optionally configured to operate in RS232 protocol. When setup as RS232 the port functions as a Data Set. For each of the different protocols the following table defines the functions of the connector.

The normal configuration for C Revision and later boards is RS232.

Table 3-4. Pinouts of Different Specs

Pin#	RS422	RS423	RS232
1	Ground	Ground	Ground
2	Tx Data -	Tx Data	Tx Data (in)
3	Rx Data -	Rx Data	Rx Data (out)
4	Request to Send -	Request to Send	Request to Send (in)
5	Rx Clock +	Clear to Send	Clear to Send (out)
6	Rx Data +	Data Set Rdy	Data Set Rdy (out)
7	Signal Ground	Signal Ground	Signal Ground
9	+12	External Power	
10	-12	External Power	
14	Tx Data +	Not Used	Not Used (in)
17	Rx Clock -	Rx Clock	Rx Clock (out)
18	Data Terminal Rdy +	Not Used	Not Used (in)
19	Request to Send +	Not Used	Not Used (in)
20	Data Terminal Rdy -	Data Terminal Rdy	Data Set Ready (in)
24	Clock In -	Clock In	Clock In (in)
25	Clock In +	Not Used	Not Used (in)

The mode option defines the operation of the 26LS30 driver as follows:

Jumper JP11. Driver Mode Select

RS423 or RS232	2 Jumpered to 1(normal)
RS422	2 Jumpered to 3

Inputs to the receivers may be changed by the jumper options JP8, JP9, JP10, and JP12. For single ended modes (RS232 and RS423) the + input of the receiver is grounded. The jumper options are:

Jumpers JP8, JP9, JP10, JP12. Receiver Options

RS423 or RS232	2 Jumpered to 3 (normal)
RS422	2 Jumpered to 1

Transmitted Data may be inverted by use of Option JP28. For RS232 it must be inverted for proper RS232 level signals. The clad must be cut on the back side of the circuit board if the inverted option is implemented.

Jumper JP28. Transmitted Data Inversion Option

Inverted (RS232)	2 Jumpered to 1 (normal)
Noninverting (RS422, RS423)	2 Jumpered to 3

The Network port also has a clock option as follows:

Jumper JP27. Auxiliary Clock Option

Internal Modem Clock	2 Jumpered to 1 (normal)
External Clock	2 Jumpered to 3

The inputs of the network port have an option for installing termination resistors. These resistors RT1 through RT4, located next to device 1N, can be used in either the RS422 or RS423 mode. See the schematic and assembly drawings for further information.

The slew rate control option allows output slew rate to be controlled by capacitors CS1 through CS4 located between devices 1P and P4. For value determination refer to the 26LS30 Data Sheet.

For applications requiring a small amount of external power at + and - 12 volts, a jumper option JP13 provides power to pins 9 and 10 of the serial connector.

Jumper JP13 + and -12 volt power option

JP13 1-2 for -12 on pin 10 JP13 3-4 for +12 on pin 9

3.7 Console I/O 62H, 63H

The Console I/O transfers data between the CPU board and the Video and keyboard processor. One-half of an SIO device (2G) handles the RS232 protocol for data transfer. The clocking for this half of the SIO is supplied by the Video Processor. Refer to Chapter 5 on the Video Processor Board for complete information from the Video Board side of the I/O.

Port 62H is data and Port 63H is Status and Control.

The following table reflects pinouts from the CPU Board end of the Process:

Table 3-5. Video I/O Pinouts

Pin #	Name	Function
1,2,3,4,7,8 10,16,17,19,20	GND	Ground
6	DTR	Data Terminal Ready (from CPU)
9	TxD	Transmit Data (from CPU)
11	RxD	Receive Data (into CPU)
12	TRxC	Transmitter Receive Clock
13	CTS	Clear to Send (into CPU)
14	RTS	Request to Send (from CPU)
15	EXRESET	External Reset (into CPU)
18	VR	Video Reset (from CPU)
5		No Connection

3.8 MODEM I/O 70H, 71H

The Modem I/O is handled by half of the SIO device at location 2H and is configured according to the EIA specifications for a Data Terminal. 70H is data and Port 71H is Status and Control. Refer to the Data book describing the MK3884/Z80-SIO and the appropriate schematics for additional detail.

The modem port baud rate is software programmable by the baud rate generator at Port D0H and described in Section 3.13. Note that this baud rate generator is shared with the Network I/O Port.

Connection to a modem is made through P3, a male DB25P connector. The following table describes pinouts for the modem I/O:

Table 3-6. MODEM I/O Pinouts

Pin #	Name	Function
1	GND	Chassis Ground
2	TxD	Transmit of Data (out)
3	RxD	Receive Data (in)
4	RTS	Request to Send (out)
5	CTS	Clear to Send (in)
6	DSR	Data Set Ready (in)
7	GND	Signal Ground
9	+12	External Power - Jumper JP15 3-4
10	-12	External Power - Jumper JP15 1-2
15	TSET	Transmitter Signal Element Timing (in)
17	RSET	Receiver Signal element Timing (in)
20	DTR	Data Terminal Ready (out)
23	DSRS	Data Set Ready Secondary (terminated with 22K to +12)
24	STSET	Source Transmitter Signal element Timing (out)

There are two jumper options available with modem I/O on the timing clocks. One set of jumper pads controls the receive clock and one set is for the transmit clock.

The Transmitter Clock option is identified as JP23 on the PROM and Serial I/O schematic in Appendix A. The transmitter clock can be sourced internally or externally, but it is normally jumpered for internal.

Jumper JP23. Modem Transmitter Clock Option

Internal	2 Jumpered to 1 (normal)
External	2 Jumpered to 3
Receiver	Open

To use the external option the clad on the back of the circuit board must be cut between pins 1 and 2.

The Receiver Clock option jumpers are identified as JP21. The clock is normally jumpered to the internal clock but may be jumpered to the external receiver element timing signal or to the transmitter clock.

Jumper JP21. Modem Receiver Clock Option

Internal	2 Jumpered to 3 (normal)
External	2 Jumpered to 1
Transmitter	2 Jumpered to 4

To use the external option, the clad on the back of the circuit board must be cut between pins 2 and 3.

For applications requiring a small amount of external power at + and - 12 volts, a jumper option JP15 provides power to pins 9 and 10 of the serial connector.

Jumper JP15 + and -12 volt power option

JP15 1-2 for -12 on pin 10 JP15 3-4 for +12 on pin 9

3.9 List 72H,73H

The list function is handled by half of the SIO device at location 2H and it is designed to match EIA Data Set specifications. The interfacing chip is an MK3884/Z80A-SIO. Port 72H is data and Port 73H is Status and Control.

The list baud rate is selectable using the baud rate generator at Port E0H described in Section 3.13 of this manual. Connection to a printer is made through J3, a female DB25S connector. The following table describes pinouts for the printer:

Table 3-7. List I/O Pinouts

Pin #	Name	Function
1	GND	Chassis Ground
2	TxD	Transmit Data (in)
3	RxD	Receive Data (out)
4	RTS	Request to Send (in)
5	CTS	Clear to Send (out)
6	DSR	Data Set Ready (out)
7	GND	Signal Ground
9	+12	External Power - Jumper JP13 3-4
10	-12	External Power - Jumper JP13 1-2
15	TSET	Transmitter Signal Element Timing (out)
17	RSET	Receiver Signal element Timing (out)
20	DTR	Data Terminal Ready (in)
21	SQD	Signal Quality Detector (Driven by a 22K resistor to +12V)
22	RI	Ring Indicator (Driven by a 22K resistor to +12V)
23	DSRS	Data Signal Rate Selector (Driven by a 22K resistor to +12V)
24	TSET	External Clock (in)

Clock Source Option. Jumper Pin Block JP22 gives the option of driving the list SIO from the internal Baud Rate generator or externally from Pin 24 on the list device connector.

Jumper JP22. List Device Clock Option

Internal	2 Jumpered to 1 (normal)
External	2 Jumpered to 3

To use the external option the clad on the back of the circuit board must be cut between pins 1 and 2.

For applications requiring a small amount of external power at + and - 12 volts, a jumper option JP13 provides power to pins 9 and 10 of the serial connector.

JP13 + and -12 volt power option

JP13 1-2 for -12 on pin 10 JP13 3-4 for +12 on pin 9

3.10 Floppy Disk 80H-83H

The floppy disk controller provides I/O to run the double-sided, double-density floppy disk drives. The controller chip is a Western Digital 1793B-02; refer to the data sheet for details on its operation.

The chip is normally run under DMA control as DMA device 1. Refer to section 3.1 "DMA Controller" for information. It can also be run under interrupt control; an interrupt request is driven from interrupt request signal DINT1 - refer to section 3.3 "Interrupt Controller" for operation.

Interface to the floppy disk is through Connector P5. The following table defines the pinouts; all signals are active low:

Table 3-8. Floppy Disk Pinout

Pin #	Name	Function
2	SPARE	
4	HEAD LOAD	Loading of head
6	SPARE	
8	INDEX PULSE	Timing Signal from Disk
10	DS1	Disk Select One
12	DS2	Disk Select Two
14	SPARE	
16	MOTOR ON	Turns on the Selected Motor
18	DIRC IN	Direction in Toward Center of Disk (Low-Head Pulled in toward Center)
20	STEP	Track Step
22	WRITE DATA	Data Goes on Disk
24	WRITE GATE	
26	TRACK 0	Detection of Track Zero for the Disk
28	WR PROTECT	Write Protect
30	READ DATA	Read Data
32	SIDE SELECT	Side Select
34	READY	Indicates to 1793 that disk drives are ready
1-33 ODD	GROUND	Ground Shield

An option is provided on the board for selecting control of Side Source Select:

Jumper JP37 Side Select Source

Pin 2 jumpered to Pin 1	Side Select sourced from Control Latch (normal)
Pin 2 jumpered to Pin 3	Side Select sourced from 1797 (Clad between 1 and 2 must be cut)

3.11 Status and Control AOH

The main CPU has a single byte stored in an 8 bit latch used to control key functions in the system. This latch is set to all 0's by a RESET. The memory location OBH is reserved to store the status of this byte. This byte, written using an OUT instruction to AOH, has the following functions:

Table 3-9. Control Functions

Bit #	Signal Name	Function	
0	DS1	Drive Select (Drive A)	1=ON
1	DS2	Drive Select (Drive B)	1=ON
2	T/R	Parallel Port A Direction Control 0 = receive, 1 = transmit	
3	APURES	Reset the 9511 Arithmetic Processor	0=Reset
4	TG19	"Track greater than 19," used by Write Precompensation	1=Write Precomp on
5	SIDE SELECT	Disk Side Select (0 is bottom, 1 is top)	1=Back side
6	PROMEN	PROM Enable (0 is PROM enable, 1 is PROM disable)	0=Enable
7	DISK RESET	Floppy Disk Controller Reset	0=Reset

Status is read by the processor at address AOH with the function of the bits as follows:

Table 3-10. Status Bits

Bit #	Signal Name	Function
0	INTRQ	Disk Controller Done
1	HLT	Head Loaded
5	Spare	IC 5L Pin 13 (JP 36)
7	DRQ	Disk Controller Data Ready

A "1" indicates that the stated action has occurred.

3.12 Real Time Clock BOH,COH

The Real Time Clock (RTC) option provides the ASSOCIATE with time information ranging from thousandths of seconds to months. It is available for Systems using "F" revision or later CPU boards.

The option is based on the MM58167 clock chip with rechargeable nicad batteries to keep the time information valid even when the computer is turned off or unplugged.

The RTC occupies a block of 32 addresses. These addresses B0H to C0H are assigned as follows:

Table 3-11. Real Time Clock Functions

```
Name            Address         Function

ctrsm   equ     0C0H    ; Counter - thousandths of seconds
ctrsth  equ     0C1H    ; Counter - tenths and hundredths of seconds
ctrsec  equ     0C2H    ; Counter - seconds
ctrmin  equ     0C3H    ; Counter - minutes
ctrhr   equ     0C4H    ; Counter - hours
ctrdow  equ     0C5H    ; Counter - day of the week
ctrday  equ     0C6H    ; Counter - day of the month
ctrmon  equ     0C7H    ; Counter - months
latsm   equ     0C8H    ; Latch - thousandths of seconds
latsth  equ     0C9H    ; Latch - tenths and hundredths of seconds
latsec  equ     0CAH    ; Latch - seconds
latmin  equ     0CBH    ; Latch - minutes
lathr   equ     0CCH    ; Latch - hours
latdow  equ     0CDH    ; Latch - day of the week
latday  equ     0CEH    ; Latch - day of the month
latmon  equ     0CFH    ; Latch - months
rtcisr  equ     0B0H    ; Interrupt status register
rtcicr  equ     0B1H    ; Interrupt control register
rtctrr  equ     0B2H    ; counter reset
rtcltr  equ     0B3H    ; latch reset
rtcsts  equ     0B4H    ; status bit
rtcgo   equ     0B5H    ; "Go" command
rtcstby equ     0B6H    ; Standby interrupt
rtctst  equ     0BFH    ; Test mode
```

Two software programs are provided with the Real Time Clock option. These are: TRTC.COM, a routine that allows the operator to manually set and test all the parameters of the clock operation, and TIME.COM, a sample routine to display the current time on the monitor.

The system time may be set or reset using the 'T' option in the TRTC program. In response to prompts from this routine the user sets the current hour, minute, second, day, day of week, and month. Once set, the current time is always available by doing an input from the proper counter as shown in the above table or by executing the program 'TIME'. Day 1 of the week is Sunday.

The NICAD batteries and charging circuit provide a 10 to one ratio for backup versus on time. This ratio is set by the 330 current charge resistor R7. When the system is first used with new batteries, the AC power should be left on continuously for the first week. The voltage at pin 24 of the 58167 device should be greater than 3.4 volts with the AC power off. If the voltage is lower than this, the batteries need to be charged or replaced. 500 hours of back-up is available from fully charged batteries.

The Real Time Clock chip can be programmed to generate an interrupt at a preset time. To enable the interrupt, jumper pins 11 and 12 together on

jumper pad JP42 located between 7L and 7K. This ties the regular interrupt output of the MM58167 to Trigger 3 interrupt input of the CTC Interrupt controller. The CTC channel 3 must be set for a count of 1 to act as an interrupt controller.

Jumper Pin Block JP42 RTC Interrupt Operation

Pin 11 jumpered to 12	RTC Interrupt Enabled
Pin 11 open to 12	RTC Interrupt Disabled (Normal)

The standby interrupt output from the device, normally not used is available on Jumper Pin JP32.

A variable capacitor (C6) on the board allows minor adjustments of the clock rate of the Real Time Clock. The capacitor is located at the edge of the board next to the Clock chip at location 3S. The procedure for setting the time is as follows:

Check time against a standard to determine the number of seconds per day of error. Then select the 'S' option in the TRTC program. A series of hex numbers will be provided which should stabilize to a value between FFE0H and 001FH. This number is the Real Time Clock offset in seconds per day. If the Clock is running too slow, adjust C6 to increase this number by one for each second per day the Clock was slow (0001 is greater than FFFF). After adjustment, 90 seconds is required for the number displayed to stabilize.

3.13 Baud Rate Generator D0H,E0H

Baud Rate Generation is done by a dual software controlled timer whose source crystal frequency is 4.9152 MHz.

The normal assignment of serial ports to the Baud Rate Generator is shown in Table 3-12. This assignment may be optionally changed as described in the section for each of the individual devices.

Table 3-12. Normal Baud Rate Generator Setup

Serial Function	Baud Rate Generator Address	Default Rate
List Device	E0H	9600
Modem	D0H	300
Network	D0H	300
Video	External	48000

Each port of the baud rate generator uses only four bits of the byte written to it. The port at D0H uses only the four least significant bits. E0H Port uses the four most significant. In the following table the left and right nybbles are shown to be duplicates, which simplifies operations: an "OUT" instruction with the data from this table to port D0H or E0H will set the baud rate for that device:

Table 3-13. Baud Rate with 16x clock

Byte	Baud Rate
00	50
11	75
22	110
33	134.5
44	150
55	300
66	600
77	1200
88	1800
99	2000
AA	2400
BB	3600
CC	4800
DD	7200
EE	9600
FF	19200

For example in the PROM Monitor the procedure to set the List device to 1200 baud is:

```
QO:EO,77        (the monitor provides the colon)
```

or to set the modem port to 9600 baud:

```
QO:DO,EE
```

The baud rate generator is reset upon power up, CTRL-SHIFT-RST, or a manual reset from the rear panel. It is not changed by a CTRL-C warm reboot.

3.14 Ram On Control

An Output instruction to location DOH will clear the restart Flip/Flop thereby enabling RAM and restricting PROM addressing to locations F800H to FFFFH. No software provision is made to disable RAM once it is enabled.

3.15 Serial I/O Assignment

The CP/M Device assignments are described in the table below. The left side is the logical name and the right side of the assignment being the CP/M function.

```
CON:  =  Monitor display and keyboard
LST:  =  Printer device output
PUN:  =  Punch device output
RDR:  =  Reader device input
```

This assignment is controlled by two bytes referred to as IOBYTE and EXTIOB stored in memory locations 0003 and 0004. The default values are

11101000 (E8 HEX) and 00000000. Each of the CP/M functions is controlled by two bits out of each byte. The following table shows all the possible device assignments for each of the functions:

The bit pattern in IOBYTE determines the physical port assigned to each logical device.

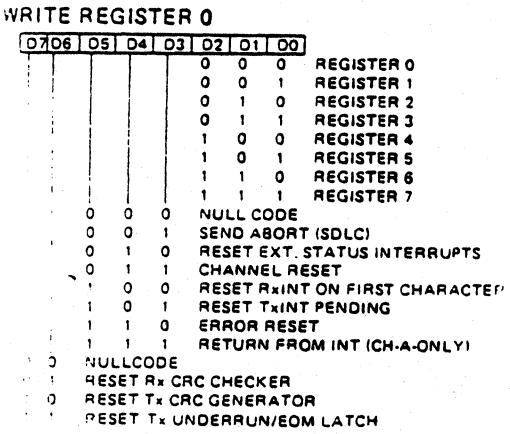
LST:	PUN:	RDR:	CON:	Back Panel Connector
00xxxxxx	xx00xxxx	xxxx00xx	xxxxxx00	
62hex	62hex	62hex	62hex	Internal CRT
01xxxxxx	xx01xxxx	xxxx01xx	xxxxxx01	
60hex	60hex	60hex	60hex	Network Port
10xxxxxx	xx10xxxx	xxxx10xx	xxxxxx10	
70hex	70hex	70hex	70hex	Modem Port
11xxxxxx	xx11xxxx	xxxx11xx	xxxxxx11	
72hex	72hex	72hex	72hex	List Port

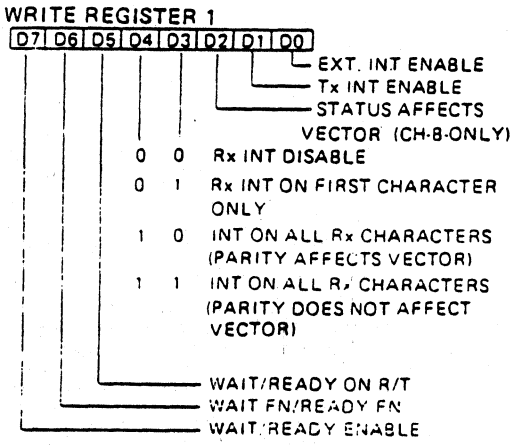
The bit pattern in IOBEXT determines the driver assigned to each logical device.

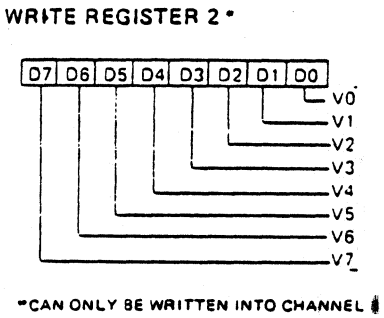
LST:	PUN:	RDR:	CON:	Driver Definition
00xxxxxx	xx00xxxx	xxxx00xx	xxxxxx00	Std is the standard assignments
iostd	iostd	iostd	iostd	
01xxxxxx	xx01xxxx	xxxx01xx	xxxxxx01	SQ indicates a Control-S and Control-Q hand-shake output
iosq	iosq	iosq	remote	
10xxxxxx	xx10xxxx	xxxx10xx	xxxxxx10	Diab is driver for Diablo printer
iodiab	iodiab	iodiab	iostd	
11xxxxxx	xx11xxxx	xxxx11xx	xxxxxx11	Remote means that the Modem Port is parallel with the CRT
null	null	null	null	

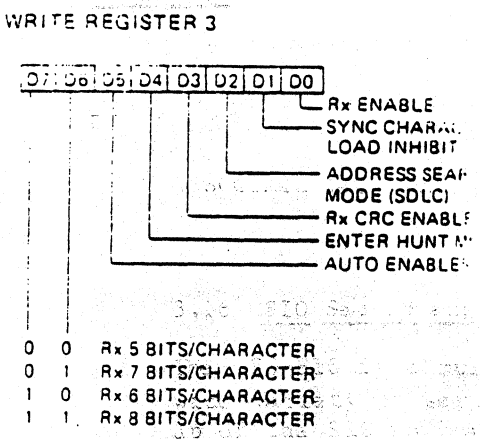
3.16 SIO Set-Up and Summary

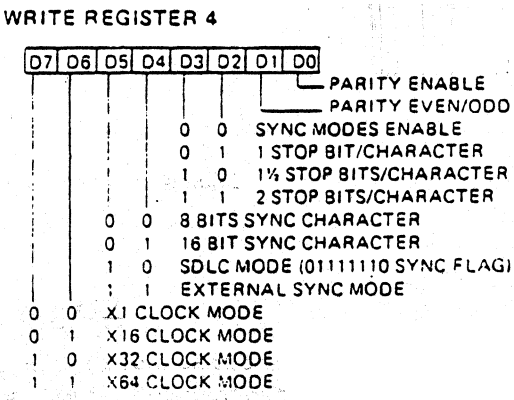
The Z80-SIO is a mult-function peripheral component designed to satisfy a wide variety of serial data communications requirements. The normal set up of the SIO is 1 start bit, 8 data bits, 1 stop bit, no parity, and x16 clock divider. The SIO 8 write registers and 3 read registers whose functions are defined below:

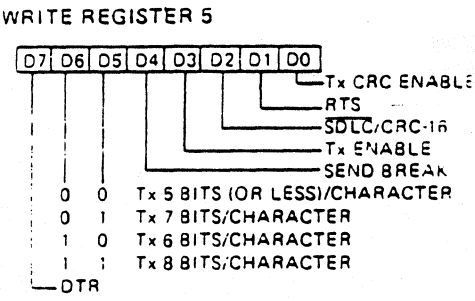


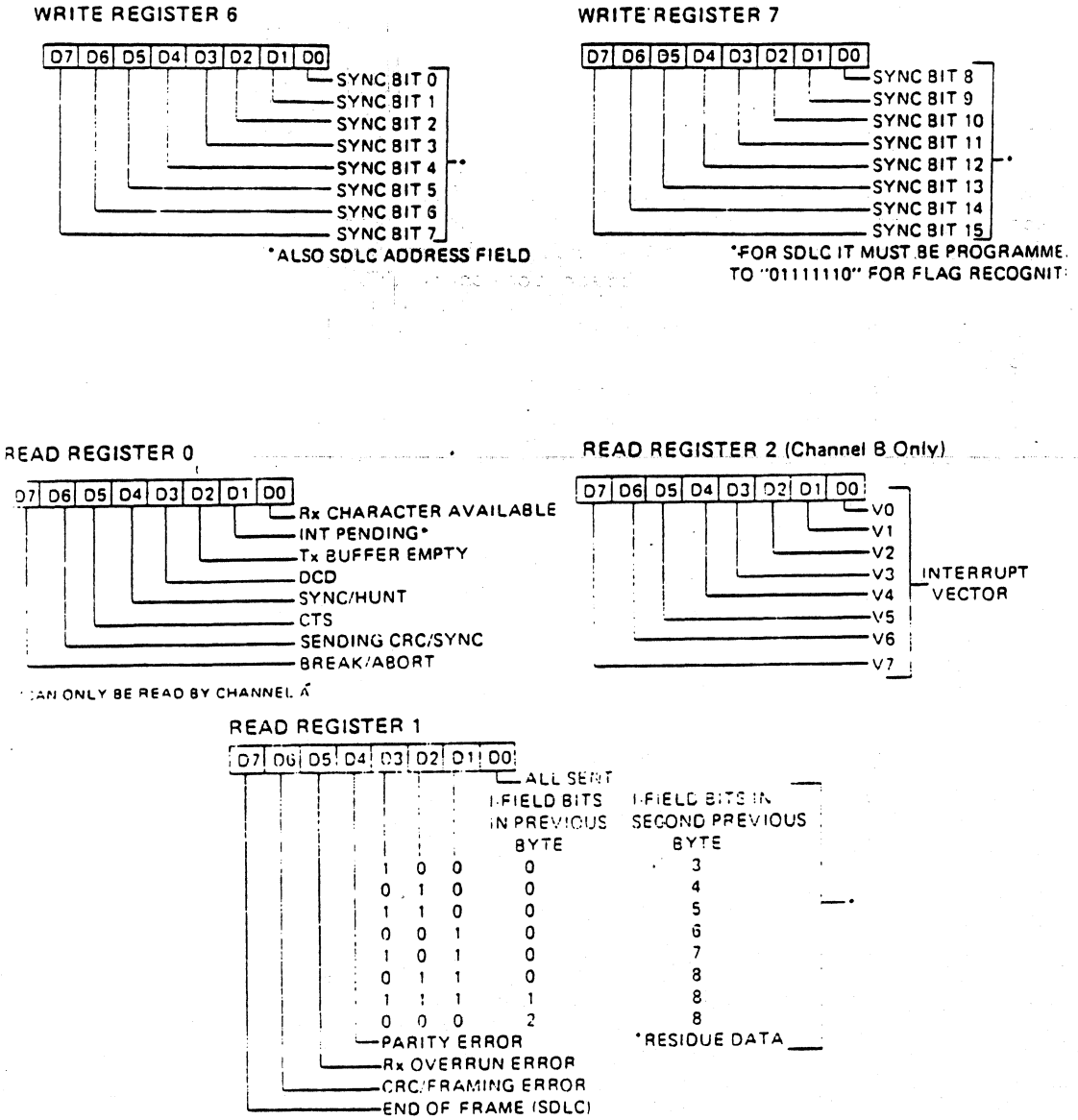












3.17 System Interfacing (Cables)

Several cables are available from to facilitate connecting the ASSOCIATE to external devices. Several of the most commonly used cables are listed below for reference. All signal line nomemclature used is defined according to EIA RS232C conventions. The (in) or (out) is with reference to the microcomputer hardware, for example any line labeled (out) will have data coming from the CPU processor board.

CA-60 ASSOCIATE to NEC Printer

This cable is used to connect the the ASSOCIATE List Port to the NEC Printer. This cable is an adapter to the NEC supplied cable. It is used so that no changes are required in the NEC cable. The wiring in the cable is one to one except for pin 20 as follows:

CA-60 Cable - ASSOCIATE to NEC Spinwriter

DB25P (List Port)		DB25S (NEC Cable)
Pin #	Function	Pin #
1	Chas Ground	1
2	Tx Data (in)	2
3	Rx Data (out)	3
4	Request to Send (in)	4
5	Clear to Send (out)	5
6	Data Set Ready (out)	6
7	Sig Ground	7
8	Rec'd line sig (out)	8
20	Data Terminal Ready (in)	19

CA-61 ASSOCIATE to TTY Model 40 Line Printer

This cable is used to connect the the ASSOCIATE List Port to the Teletype Model 40 line Printer. The wiring is one to one except for pin 4 as follows:

CA-61 ASSOCIATE to TTY Model 40 Line Printer

DB25P (List Port)		DB25S (TTY 40)
Pin #	Function	Pin #
1	Chas Ground	1
2	Tx Data (in)	2
3	Rx Data (out)	3
4	Request to Send (in)	14
6	Data Set Ready (out)	6
7	Sig Ground	7
20	Data Term Ready (in)	20

CA-62 ASSOCIATE to MODEM

This cable is used to connect the the ASSOCIATE Modem Port to a modem. This is a standard EIA - RS232C extension cable. It can also be used to connect the List or Network port to any RS232C Data Terminal Equipment such as an ASSOCIATE Terminal or the modem port of another ASSOCIATE. The wiring in the cable is one to one as follows:

CA-62 ASSOCIATE to MODEM Cable

DB25S (MODEM Port) Pin #	Function	DB25P (MODEM) Pin #
1	Chas Ground	1
2	Tx Data (out)	2
3	Rx Data (in)	3
4	Request to Send (out)	4
5	Clear to Send (in)	5
6	Data Set Ready (in)	6
7	Sig Ground	7
8	Rec'd line sig (in)	8
15	Trans Clock (in)	15
17	Rec Clock (in)	17
20	Data Term Ready (out)	20
24	Trans Clock (out)	24

CA-63 ASSOCIATE to Terminal

This cable is used to connect the the ASSOCIATE Network or List Port to a Terminal device with a female connector such as an ADM3A. The wiring in the cable is one to one as follows:

CA-63 ASSOCIATE to Terminal Cable

DB25P (NETWORK or LIST PORT) Pin #	Function	DB25P (MODEM) Pin #
1	Chas Ground	1
2	Tx Data (in)	2
3	Rx Data (out)	3
4	Request to Send (in)	4
5	Clear to Send (out)	5
6	Data Set Ready (out)	6
7	Sig Ground	7
8	Rec'd line sig (out)	8
15	Trans Clock (out)	15
17	Rec Clock (out)	17
20	Data Term Ready (in)	20
24	Trans Clock (in)	24

CA-65 ASSOCIATE to TI Model 820 Printer

This cable is used to connect the the ASSOCIATE List Port to the Texas Instrument Model 820 Printer. The wiring is one to one except for pin 4 as follows:

CA-65 ASSOCIATE to TI Model 820 Printer

DB25P (List Port) Pin #	Function	DB25P (TI 820) Pin #
1	Chas Ground	1
2	Tx Data (in)	2
3	Rx Data (out)	3
4	Request to Send (in)	11
6	Data Set Ready (out)	6
7	Sig Ground	7
8	Carrier Det (out)	8
20	Data Term Ready (in)	20

The Secondary Request To Send signal from the printer is tied to the List port Request To Send.

The TI 820 is a programmable printer. To program it for operation with the ASSOCIATE, lift the cover, slide the "configure" switch to the local position and proceed with the programming. Start by typing in a <return> and then a <tab> which will put the printer in full duplex reverse channel mode. The suggested baud rate is 9600 programmable by typing 28 <return> <tab>. No other parameters need changing. Set the "configure" switch back to its normal position for operation. See the TI manual for complete programming details.

QUME Printer Operation

The QUME Sprint 5 printer will connect directly or through a CA-62 cable to the List port. The Qume should be set up as follows:

Front Panel Switches		Inside Switches
Reset		Both switched to the left
Baud Rate	- 1200	side of the unit.
Duplex	- Full	
Parity	- Mark	Modem = off
		Rate = Hi
Reset		
Auto LF	- Off	
Twintell	- Standard	
Char Spac	- your choice	
Form Length	- 11 is standard	
Top of Form		
Form Feed		

A Qume Sprint 9 is connected to the ASSOCIATE by a 1:1 cable. The WordStar setup for the Sprint 9 is the same as the Sprint 5. For normal Sprint 9 operation with the ASSOCIATE, the internal options are set as follows:

A-8	A-7	A-6	A-5	A-4	A-3	A-2	A-1	B-8	B-7	B-6	B-5	B-4	B-3	B-2	B-1
on	on	on	off	off	on	on	on	on	on	on	on	on	on	on	off

Chapter 4

VIDEO PROCESSOR BOARD

The video processor board provides control of the ASSOCIATE CRT and keyboard. The video processor board is built to enable the CRT to run as a stand alone terminal. A separate manual is available describing the 10T Terminal version of the ASSOCIATE.

Key chips on the video processor board are the Intel 8085 Microprocessor and Motorola 6845 CRT Controller. Refer to the appropriate manufacturer's manual for detailed information on these chips. The processor has 1K of local RAM for temporary storage. The 2K video RAM is dual-ported, so either the 8085 or CRTC can address it. The CRT controller controls read-out of RAM into the video generator, and the 8085 processor can both read and write into video RAM.

Two 2K PROM chips provide program storage and character generation for the video processor. The program is stored in the first 2K of the memory of the 8085 and begins execution immediately upon power up. The second PROM is used as a character generator for the 8 x 12 dot matrix character set. Standard PROMs are TMS2516's. TMS2532's can be used with no hardware changes if more extensive CRT control programs are needed. Use of a TMS2532 for alternate character sets requires IC30 pin 18 to be jumpered to an I/O pin on the 8155. A program for generation of custom character sets is available from Data Technology.

All data going to the main processor is transferred via a serial line, with the video processor providing the clock signals to the main CPU Board. The video processor board has two parallel data channels, one for the keyboard and one for the utility port. The utility port is a general purpose parallel port which can be used for a second keyboard.

The video processor board has on it a bell normally activated by a "Control G" character.

The video processor board is mounted, vertically, in the back of the CRT. Access to the video processor board is accomplished by removing the front panel assembly as described in Section 8 of this manual.

Sections in this chapter include descriptions of the video processor board's Internal Architecture (including a memory map), keyboard I/O, Utility I/O, CPU Interface, video generator interface, and operational characteristics.

4.1 Internal Architecture

The peripheral devices on the video processor board are addressed by memory mapping as shown in the following table:

Table 4-1. Video Processor Board Memory Map

Address	Device	Description
0000-07FF	CPU PROM	Stores Program for CPU
1000-13FF	CPU RAM	CPU RAM - Scratch area for 8085 Microprocessor
2000-27FF	VRAM	Video RAM
3000	RESET OUT	Generates a RESET to the main CPU board
4000-40FF	8155 RAM	CPU RAM scratch area
4800-4803	8155 I/O	Utility and keyboard I/O
4804-4805	8155 TIMER	Baud Rate Generator
5000-5001	8251 USART	Interface to the Main CPU Board
6000	BELL	Bell
7000-7001	CRTC	CRT Controller

An option is available to allow substitution of an 8156 for the 8155 I/O device.

8155/8156 Option

CE jumpered to 5	8155 device (normal)
CE jumpered to 6	8156 device

For operation with the 8156 the clad between CE and 5 must be cut.

The CRT Controller and I/O devices drive the processor through the interrupts. The following table specifies the interrupt priority:

Table 4-2. Interrupts and Priority

Priority	Interrupt Name		Description
1	VSYNC	TRAP	Vertical Sync
2	RxRDY	R7.5	Receive Data from CPU
3	TxRDY	R6.5	Receive Data from Utility
4	INTA	R5.5	Receive Data from Keyboard
5	INTB	INTR	Transmitter to CPU Ready

4.2 Keyboard I/O

Keyboard I/O is handled through the 8155 I/O and Timer. When a key is pushed, it generates a strobe signal which clocks the keyboard data into the 8155. The 8155 will in turn generate both an interrupt and a data ready flag to the processor. Under normal software the Video Processor is interrupt driven, but could alternatively operate in a polled fashion. Refer to the Intel data sheet for complete information on the 8155.

Refer to the keyboard table in Chapter 7 of this reference manual for a complete description of data transmitted by different keys.

The following table describes the various pinout functions of the keyboard I/O. A 20 pin 3M ribbon cable is used to attach the keyboard. This cable also supplies power for the keyboard electronics.

Table 4-3. Keyboard I/O Pinouts

Pin #	Name	Function
1	ASTB	Data available from keyboard
3	ARDY	Keyboard transmit enable
5	PA7	Data bit 7
7	PA6	Data bit 6
9	PA5	Data bit 5
11	PA4	Data bit 4
13	PA3	Data bit 3
15	PA2	Data bit 2
17	PA1	Data bit 1
19	PA0	Data bit 0
2-8 Even	GND	Ground
10,12	+5V	Power
14,16	+12V	Power
18,20	-12V	Power

4.3 Utility I/O

The utility I/O is designed to be a general purpose port which can be used to attach an additional keyboard.

The following table describes the various pinout functions of the utility port. A 20 pin 3M ribbon cable is used to attach to the port:

Table 4-4. Utility I/O Pinouts

Pin #	Name	Function
1	BSTB	Data available from keyboard
3	BRDY	Keyboard transmit enable
5	PA7	Data bit 7
7	PA6	Data bit 6
9	PA5	Data bit 5
11	PA4	Data bit 4
13	PA3	Data bit 3
15	PA2	Data bit 2
17	PA1	Data bit 1
19	PA0	Data bit 0
2-8 Even	GND	Ground
10,12	+5V	Power
14,16	+12V	Power
18,20	-12V	Power

4.4 CPU Interface

An 8251 chip is used for the communication interface between the video processor board and the main CPU; it follows RS232 standard serial protocol. By having standard RS232 protocol the CRT/keyboard can function as a standalone terminal, similar in capability to an enhanced ADM 3A in terms of interaction with another computer.

The connection between the video processor board and the CPU Board is made through a 20-pin ribbon cable which connects to P6 on the CPU Board and J1 on the video board.

The following table describes Pin functions for the CPU Interface. All direction references are to the host CPU.

Table 4-5. Interface Pinout

Pin #	Name	Function
1,2,3,4,7	GND	Ground
5	DTR	Data Terminal Ready (to CPU)
6	DSR	Data Set Ready (from CPU)
9	RxD	Receive Data (from CPU)
11	TxD	Transmit Data (to CPU)
13	RTS	Request to Send (from CPU)
14	CTS	Clear to Send (to CPU)
15	RESOT	Reset Out (to CPU)
17	CLOCK	Clock (to CPU)
18	RESIN	Reset in (from CPU)

A reset from the keyboard (control shift RST) does not reset the video processor, it merely transmits the reset through to the main CPU. See Section 2.2.2 for further information on resets.

Two options are available on the Serial I/O clock. The first located below IC10 is for the clock source signal:

Clock Source Option

BDR jumpered to IN	Internal clock
BRR jumpered to EX	External clock

The clock source is normally internal; to use an external clock the jumper clad on the back of the circuit board must be cut.

The second option selects the frequency of the input into the Baud Rate divider. The source timing normally is 2.304 MHz but may be jumpered to 4.608 MHz. The faster source clock will allow operation at a higher baud rate but does exceed specification for the standard 8155 timer.

Clock Rate Option

CK jumpered to 02	2 MHz source (normal)
CK jumpered to 04	4 MHz source

To implement the 4 MHz option the clad to 02 must be cut on the back of the circuit board.

4.5 Character Generator and Video Interface

Video display information from the Video RAM is passed through a 2716 PROM used as a character generator. It is then combined with cursor information and transmitted to the CRT via connector P3 as EIA composite video. The board is configured to allow operation with a 2732 PROM thereby doubling the character set. To operate with a 2732 pin 18 must be connected to the proper level. It is normally connected to ground.

Table 4-7. Video Connector P3

Pin #	Name	Function
1	VID	Video
2	VER	Vertical Sync
3	HOR	Horizontal Sync
4	GND	Ground

Three options are available in the video generator section. They are:

Composite Video

E jumpered to D	Horizontal and Vertical Sync add to video
E jumpered to F	No sync information added to video (normal)

To add sync information, jumper between F and E.

The following options have been changed on differing levels of ECOs. See the ECO list for details - Section 2.2.6

Attribute Option

CA7 jumpered to INT	The eight bit attribute is foreground/background (normal)
CA7 jumpered to REV	The eight bit attribute is reverse/normal video

To operate the eight bit attribute in the reverse/normal mode the clad between CA7 jumpered to INT must be cut.

Video Mode

B jumpered to A	Characters are displayed white on black background (normal)
B jumpered to C	Characters are displayed black on white background

To change the display mode the clad between B and A must be cut. It is possible to jumper this option to unused pins on the 8155 and switch modes under software control.

4.6 Light Pen Interface

Interface to a standard light pen may be made by connecting to P4 on the Video Processor board. The light pen input may be either active high or active low depending on the invert option as follows:

Light Pen Invert Option

Jumpered to High	Active high signal
Jumpered to Low	Active lo signal

Chapter 5

VIDEO PROCESSOR OPERATION

This Chapter describes software and control characteristics of the video processor. The following subjects are covered: CRT Display Format, Control Sequences, Use of "Soft" keys, CRT Memory Data Areas, CRT PROM Entry Points, and Down-Loading a Program into the CRT.

5.1 CRT Display Format

The CRT has an 80 column, 24 line display area. Characters may be displayed in background (normal intensity) or foreground (high intensity or reverse video) with background as the default display mode.

Foreground/Background can be invoked in two ways:

The first method is to use control sequences to select either foreground or background mode. Once a mode has been selected, all displayable characters sent to the CRT will be displayed in that mode.

The second method is to use the high-order bit of characters sent to the CRT. If a character with the high order bit is received by the CRT, it will be displayed in the opposite of the currently selected mode.

The CRT can also display a twenty-fifth line which does not scroll with the other twenty-four. This line can display up to eighty characters or 72 characters plus time-of-day clock. Control of information displayed in the twenty-fifth line is described later in this Chapter.

The CRT is capable of displaying 128 different characters. Each character can be displayed in either foreground or background. 96 of these characters, the "printable" characters, hex values 20H to 7FH, are displayed by simply sending the character to the CRT. To display one of the other 32 special characters 00H to 1FH, an ESCAPE character is sent followed by a byte with the value of 60H added to the value of the character to display. The character will display in foreground or background, whichever is the currently selected mode. If following the ESCAPE character, the value E0H added to the value of the special character is sent, the character will display in the opposite of the currently selected mode.

The standard set of special characters is designed for use in communication applications. These are shown on the table on the next page. An alternative set of graphic characters (see chart next page) can be ordered by specifing the graphic character set with your order.

The 32 special characters may also be displayed with the alternate attribute set by setting the eigth bit. For example the character 80H will display as N_U in the opposite attribute.

CHARGEN is a program that allows design of custom character sets. With this program the user can create custom character set files that can then be programmed into the character generator PROM. Contact the Data Technology marketing department for further information.

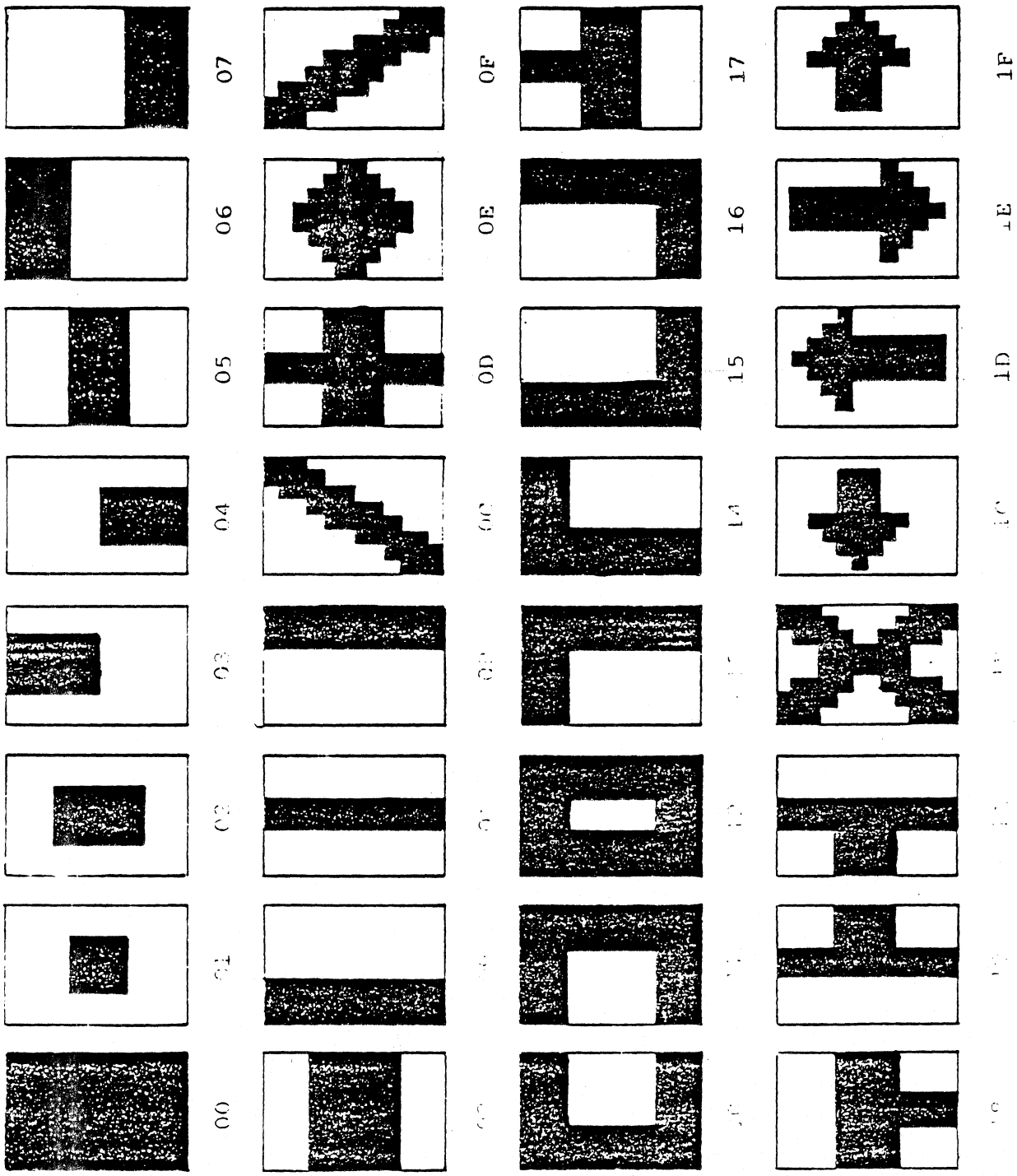
The 32 special characters are listed in the following table:

Table 5.1A Special Character display

Character	Bytes to Transmit HEX	DECIMAL	Name	Standard Display
00H	ESC 60H	ESC 96	NULL	N_U
01H	ESC 61H	ESC 97	SOH	S_H
02H	ESC 62H	ESC 98	STX	S_X
03H	ESC 63H	ESC 99	ETX	E_X
04H	ESC 64H	ESC 100	EOT	E_T
05H	ESC 65H	ESC 101	ENQ	E_Q
06H	ESC 66H	ESC 102	ACK	A_K
07H	ESC 67H	ESC 103	BELL	B_L
08H	ESC 68H	ESC 104	BACKSPACE	B_S
09H	ESC 69H	ESC 105	HORIZONTAL TAB	H_T
0A	ESC 6AH	ESC 106	LINE FEED	L_F
0B	ESC 6BH	ESC 107	VERTICAL TAB	V_T
0C	ESC 6CH	ESC 108	FORM FEED	F_F
0D	ESC 6DH	ESC 109	CARRIAGE RETURN	C_R
0E	ESC 6EH	ESC 110	SO	S_O
0F	ESC 6FH	ESC 111	SI	S_I
10	ESC 70H	ESC 112	DLE	D_L
11	ESC 71H	ESC 113	DC1	D_1
12	ESC 72H	ESC 114	DC2	D_2
13	ESC 73H	ESC 115	DC3	D_3
14	ESC 74H	ESC 116	DC4	D4
15	ESC 75H	ESC 117	NAK	N_K
16	ESC 76H	ESC 118	SYN	S_Y
17	ESC 77H	ESC 119	ETB	E_B
18	ESC 78H	ESC 120	CAN	C_N
19	ESC 79H	ESC 121	EM	E_M
1A	ESC 7AH	ESC 122	SUB	S_B
1B	ESC 7BH	ESC 123	ESC	E_C
1C	ESC 7CH	ESC 124	FS	F_S
1D	ESC 7DH	ESC 125	GS	G_S
1E	ESC 7EH	ESC 126	RS	R_S
1F	ESC 7FH	ESC 127	US	U_S

The alternate graphics set is shown on the following page:

Table 5.1B Alternate Special Character Set



5.2 Control Sequences

The CPU sends commands to the CRT in the form of control sequences. Control sequence may be in the form of single or multiple characters; multiple-character control sequences begin with an ESCAPE character. If an invalid character follows the ESCAPE, both characters are ignored, and the CRT resumes processing with the next character.

Single-Character Control Sequences

HEX VALUE	DECIMAL VALUE	ASCII NAME	Function in CRT
07	07	BELL	Sound audible tone.
08	08	BS	Move cursor left one column. If the cursor is on the first column of a row other than the top row, it will move to the last column of the next higher row.
0A	10	LF	Move cursor down one row. If the cursor is on the last row, the screen scrolls up one line.
0B	11	VT	Move cursor up one row. If the cursor is on the top row, it does not move.
0C	12	FF	Move the cursor right one column. If the cursor is in the last column of a row other than the bottom row, it moves to the first column on the next lower row.
0D	13	CR	Move cursor to the first column of the current row.
0E	14	SO	Unlock keyboard. This only functions if the keyboard lock/unlock is enabled -- see below.
0F	15	SI	Lock keyboard. This only functions if the keyboard lock/unlock is enabled -- see below.
1A	26	SUB	Clear screen and send cursor to home position.
1B	27	ESC	Lead-in character for multi-character control sequence.
1E	28	RS	Send cursor to home position.

Multi-Character Control Sequences

The ESCAPE lead-in character is not shown. A '(p)' indicates that the sequence takes further characters as parameters. An '(r)' indicates that the CRT will return one or more characters to the host CPU in response to the control sequence.

HEX VALUE	DECIMAL VALUE	ASCII NAME	Function in CRT
21	33	!	Set Background. The characters that follow will display at normal intensity.
22	34	"	Set Foreground. The characters that follow will display at high intensity.
23	35	#	Clear screen from cursor position to end of screen.
24	36	$	Clear screen from cursor position to end of line.
25	37	%	Insert line at cursor position. The line with the cursor and all lines below the cursor scroll down one line. A blank line is inserted at the cursor position and the cursor is positioned at the beginning of the new line.
26	38	&	Delete line at cursor position. The line with the cursor is deleted and all lines below the cursor scroll up. A blank line is inserted at the bottom of the screen. The cursor remains on the same line of the screen, but moves to the beginning of the line.
27	39	' (p)	Set baud rate. The parameter is a hexadecimal character (0-F) in ASCII) which selects the baud rate to be used between the CRT and the CPU from the following table:

ASCII Digit	Hex Digit	Baud Rate Selected
0	30H	Top speed
1	31H	48000
2	32H	38400
3	33H	28800
4	34H	19200
5	35H	9600
6	36H	4800
7	37H	2400
8	38H	1200
9	39H	300

28 40 ((p) Set time of day. The parameter is a string with the following form:

HHMMSS <CR>
HHMM <CR>
HH <CR>

where HH sets the hour, MM the minute, and SS the seconds. Each field is sent as two ASCII digits. The <CR> is required as a delimiter and will not be processed with its usual meaning.

For example, the parameter string (in ASCII) to set 10:30:15 a.m. is:

<esc> (103015 <CR>

Any omitted parameter will be set to zero.

To have the Time of Day appear on the screen, three separate functions must be done: Set Time of Day, Turn on the 25th Line, and Turn Clock Display on. For example to set and display the time to 10:30:15 a.m. from the Operating System:

<esc> (103015 <cr>	Set Time of Day
<esc> 8 <cr>	Turn on 25th Line
<esc> 2 <cr>	Turn on Clock Display

29 41) (p) Write 25th line and turn it on. The parameter string has the following form:

<eighty characters>

or

<fewer than eighty characters><CR>

The 25th line buffer is cleared to all spaces, and then the characters are written into the buffer. If more than eighty characters are sent without a carriage return, the first eighty will be written into the 25th line. Any following characters will be treated with their normal significance, meaning that they will probably be written to the screen at the cursor position.

2A 42 * Turn off 25th line. The data is retained and may be redisplayed by using the sequence to turn the 25th line on

2B 43 (p,r) Read Memory. This sequence causes the CRT to return to the host CPU a string of hexadecimal characters in ASCII representing the contents of memory starting at the requested address. Thus for each

byte of memory data requested two characters are returned. The first character of each pair represents the most significant nybble of each byte.

The parameter string is:

<address> <length>

The "address" consists of four ASCII hexadecimal characters representing 2 bytes of address; the low order address byte, most significant nybble first.

The "length" is a single ASCII hexadecimal character requesting the number of bytes to be returned. If the character is <0> sixteen bytes are read.

The string returned to the host CPU has the following form:

<data> <CR>

where each byte of data is transmitted as two ASCII hexadecimal characters.

2C 44 , (p) Write Memory. This sequence causes the CRT to write data sent by the host CPU into the CRT memory. The parameter string has the following form:

<address> <data> <delimiter>

where "address" consists of four ASCII hexadecimal characters representing 2 bytes of address; the low order address, most significant nibble first.

The "data" consists of pairs of ASCII hexadecimal characters, with each pair representing 1 byte of date. The first character of each pair represents the most significant nybble of each byte.

Memory write continues until the CRT receives a non-HEX character.

2D 45 - (p) Transfer to address. The parameter string has the form:

<address>

where "address" is the same as for the memory read and memory write sequences.

The CRT then calls to the address specified. The user may use a RET instruction to return.

2E 46 . (r) Read cursor address. The CRT sends three ASCII characters to the host CPU:

<y-pos> <x-pos> <CR>

The relationship between the sent characters and the value of the position is as follows:

row = <y-pos> - 20H
column = <x-pos> - 20H

where all values are bytes in hex.

2F	47	/	Reset soft keys. This sequence resets all soft keys to their default sequences.
30	48	0	Enable keyboard lock/unlock. This sequence enables the keyboard lock and unlock sequences (ASCII characters SO and SI) and unlocks the keyboard. The CRT is initialized with the keyboard unlocked and the keyboard lock disabled. The keyboard will not lock until an enable keyboard lock sequence is sent to the CRT, followed by a lock keyboard sequence.
31	49	1	Disable keyboard lock/unlock. This sequence disables the keyboard lock and unlock sequences (ASCII characters SO and SI) and unlocks the keyboard.
32	50	2	Clock display on. The clock is displayed on the 25th line, at the right. The 25th line must be enabled using the sequence <esc>8 or <esc>.
33	51	3	Clock display off. The clock display is turned off. The rest of the 25th line is unaffected.
36	52	6 (r)	Read light pen. The last CRT display address sensed by the light pen is returned in a string of the form xxwwzzyy<CR> The first eight bytes are hexadecimal characters representing two two-byte values: the current display screen base address 'wwxx' and the last light pen screen address selected 'yyzz'. For example, the string 10235624<CR> indicates that the current screen address is 2310H, and that the last address sensed by the light pen is 2456H. The row and column are calculated as follows:

(screen displacement of light pen) =
[(light pen address selected)
- (screen base address)
- (fudge factor)] MOD 2000H

(row selected) = (displacement) / 80

(column selected) = (displacement) MOD 80

37 55 7 (p) Right to Left Ticker-tape" display in the 25th line. The parameter string consists of a single character. The leftmost 72 characters of the 25th line are shifted one character to the left and the parameter character is inserted at the 72nd position. Continuous messages may be displayed by using this sequence repeatedly.

38 56 8 Turn on 25th line. The 25th line is displayed. No change is made to its data.

3C 60 < (p;r) Read characters from the display. This sequence causes the CRT to return to the host CPU the string of characters occupying the display memory beginning at the current cursor position. The parameter string consists of a single hexadecimal digit <length> which indicates how many characters are to be read back. If <length> is zero, sixteen bytes are returned.

3D 61 = (p) Position cursor. The parameter string has the following form:

<y-pos><x-pos>

where <y-pos> and <x-pos> are single characters representing the row and column of the new cursor position. The translation between <y-pos> and <x-pos> and the row and column numbers is:

<y-pos> = row + 20H
<x-pos> = column + 20H

where all values are bytes in hex.

Special Control Sequences

The following memory write sequences can be used to cause the described effects:

<ESC>,26402500<CR> Disables the "toggle" function of the RST key.

<ESC>,26402520<CR> Re-enables the "toggle" function of the RST key.

<ESC>,1940xx<CR> Changes the number of minutes until the screen goes blank to xx (value in hexadecimal).

<ESC>,3E40xx<CR> Sets the minimum time between characters sent to main CPU from video board to xx msec. This is implemented on CRT PROM 1.8 and later.

<ESC>,3F4001<CR> Disables Auto-Newline function. This is implemented on CRT PROM 1.8 and later.

<ESC>,0011210A09220070C0C9<CR><ESC>-0011 Turns off cursor blink. This is an example of a call to a program to a program in the CRT RAM.

<ESC>-0000 Completely resets video board by forcing CRT processor to branch to location zero.

5.3 Use of Soft Keys

The soft (or programmable) keys are the numeric pad keys and the top row of keys (F0-F9, cursor movement and HOME, but not RST). These are the keys whose transmitted codes may be modified.

"Soft" keys generate default codes, but they may be individually "loaded" with a variable-length string of characters. After a soft key has been loaded, whenever that key is depressed, the CRT sends to the host CPU the string that was loaded into that key, as if the operator had entered the string of characters.

These keys may be loaded with the KEYLOADER Programmable Function Key program (PFK) or as described below.

Each soft key can be loaded with up to four character strings. To illustrate, if four strings were loaded into the soft key F0, A string may be selected by entering either F0, shift-F0, ctrl-F0, or ctrl-shift-F0. These four combinations are called the four "levels" of the soft key. Or a soft key may be immune to shift and cntl by loading the same character string into one or more levels of that key. As will be explained later, in this case, only one copy of the string needs to exist in the RAM storage of the CRT.

All the soft keys have a standard default code which is a single character with the high order bit set. For example, the default code for each numeric pad (no control, no shift) key is the character shown on the keytop. The default code for the cursor control keys is the character that causes the cursor to move in the direction shown on the keytop. See the Table 6.1 for the default codes for each soft key.

Each level of each soft key generates a specific code between 0 and 127, called the "soft key code." This code, the value listed in Table 6.1, minus 80H, is used to index into the soft key pointer area. This area is a table of entries (two bytes per entry, low-order byte stored first) located at 1000H. Given a soft key code of xxH, its entry can be found at 1000H + 2*(xxH). The value can also be found in Table 5.2. The entry taken from the table is processed as follows:

If the high-order byte of the entry is zero, the entry is in the "reset" state. The CRT will send to the host CPU the soft key code which is its default value.

If the high-order byte of the entry is negative(i.e. its high-order bit is 1), the CRT will "call" the absolute value of the entry, assumed to be the entry point of a user defined subroutine in the CRT.

If the high-order byte of the entry is positive(i.e. its high order bit is zero), the entry is used as the pointer to a string of characters, called the "soft key string."

The CRT wll send to the host CPU consecutive characters starting with the first byte of the soft key string. A hexadecimal "80"character marks the end of the soft key string. When this character is found, it is not sent to the host.

The following examples show how to use the programmable features of the function keys.

Example 1: Program Function Key F0 to generate a ^D (04H).

The soft key pointer for F0 is at 10C0H.
The soft key string is 0480.
Assume the location of the soft key string will be 1108H.
Then the following sequence will set the key:

```
<ESC>,C0100811<CR>          (set soft key pointer)
<ESC>,08110480<CR>          (write soft key string)
```

Example 2: Program Function Key Cntl-F0 and ctrl-shift-F0 to both generate the string 'RUN XYZ<CR>'.

The soft key pointer for ctrl-F0 is at 1040H.
The soft key pointer for ctrl-shift-F0 is at 1000H.
The soft key string is 52564E2058595A0D80.
Assume the location of the soft key string will be 1100H.

Then the following sequence will set the keys:

```
<ESC>,40100011<CR>          (set soft key pointer for
                                 ctrl-F0)
<ESC>,00100011<CR>          (set soft key pointer for
                                 ctrl-shift-F0)
<ESC>,001152564E2058595A0D80<CR> (writesoftkey string)
```

Example 3: Program Function Key F0 is to generate a ^D (04H).
Shift-F0 is to generate ^W^D (1704H).

The soft key pointer for F0 is at 10C0H.
The soft key pointer for shift-F0 is at 1080H.
The soft key string for F0 is 0480.
The soft key string for shift-F0 is 170480.
Since the string for F0 is a right-hand substring of the string for shift-F0, the two strings can share memory.
Assume the location of the soft key string for shift-F0 will

be 1107H.
The location of the soft key string for F0 will be 1108H.
Then the following sequence will set the keys:

```
<ESC>,C0100811<CR>     (set soft key pointer for F0)
<ESC>,80100811<CR>     (set soft key pointer for shift-F0)
<ESC>,0711170480<CR>   (write soft key string)
```

Table 5.2 SOFT KEY POINTER CHART

Key	Normal	Shift	Ctrl	Ctrl-Shift
Function keys:				
Fn key 0	10C0	1080	1040	1000
Fn key 1	10C2	1082	1042	1002
Fn key 2	10C4	1084	1044	1004
Fn key 3	10C6	1086	1046	1006
Fn key 4	10C8	1088	1048	1008
Fn key 5	10CA	108A	104A	100A
Fn key 6	10CC	108C	104C	100C
Fn key 7	10CE	108E	104E	100E
Fn key 8	10DE	109E	105E	101E
Fn key 9	10D2	1092	1052	1012
Cursor movement keys:				
Back	1010	1090	1050	10D0
Down	1014	1094	1054	10D4
Up	1016	1096	1036	10D6
Left	1018	1098	1058	10D8
Home	103C	109C	101C	10DC
Numeric pad keys:				
0	1060	10A0	10E0	1020
1	1062	10A2	10E2	1022
2	1064	10A4	10E4	1024
3	1066	10A6	10E6	1026
4	1068	10A8	10E8	1028
5	106A	10AA	10EA	102A
6	106C	10AC	10EC	102C
7	106E	10AE	10EE	102E
8	1070	10B0	10F0	1030
9	1072	10B2	10F2	1032
-	105A	10BA	10FA	107A
+	1056	10B6	10F6	1076
.	105C	10BC	10FC	107C
ENTER	101A	109A	103A	10DA
"under-0"	1074	10B4	10F4	1034
"under-ENTER"	1078	10B8	10F8	1038

5.4 CRT Memory Allocation

The following data areas are defined:

HEX ADDRESS	NAME	USAGE
0021H-0023H		CRT Prom Version #
1000H-10FFH		Soft Key pointer area.
1100H-13A8H		User area.
13B0H-13FFH		Buffer for 25th line.
4000H-4005H		CPU out queue control block.
4006H-400BH		Keyboard in queue control block.
400CH	XPOS	Column number of cursor (0..79).
400DH	YPOS	Row number of cursor (0..23).
400EH	INTEN	Intensity flag. 80H = Normal intensity, 00H = High intensity.
400FH-4010H	ABSIO	Absolute cursor address
4013H-4014H	LITEPEN	Last light pen address sensed
4011H-4012H	CRTBAS	Current start of screen display area
4013H-4014H	CRSPOS	Relative cursor address
4019H	TIMEOFF	Number of minutes till screen blank
4021H	L25ENAB	Non-zero enables 25th line
4022H	CLOCKFLAG	Non-zero enables clock display
4023H	KBLFLAG	Non-zero locks keyboard
402FH	HOURS	Hours counter
4030H	MINS	Minutes counter
4031H	SECS	Seconds counter
4032H	C60THS	60ths of a second counter
4036H-403DH	UPCLOCK	ASCII unpacked clock field HH:MM:SS

5.5 CRT PROM Entry Points

The following entry points into the PROM code are defined for down-loaded programs to use:

HEX ADDR	Function performed
07E5H	Fills memory starting at HL with the value in 'B', for as many bytes as specified in 'C'. If the value in 'C' is zero, 256 bytes will be filled.
07E8H	Set cursor position from relative cursor position in HL.
07EBH	Set cursor position from x and y values in XPOS and YPOS. (x = column 0..79; y = row 0..23)
07EEH	Put character in 'C' into CRT memory at cursor location and advance cursor.

07F1H Send character in 'C' to host as two ASCII bytes representing a hex value.

07F4H Returns, in 'C', the hex value of the hexascii digit in 'C'. C-latch set if not valid hex digit.

07F7H Put character in 'C' into output queue.

07FAH Return with character in 'C' from queue given by HL. Z-latch is set if no characters were in queue.

07FDH Branch, using value in 'A' as an index, into control sequences branch table.

ASCII CODE CHART

B7 B6 B5 / B4 B3 B2 B1	ø ø ø	ø ø 1	ø 1 ø	ø 1 1	1 ø ø	1 ø 1	1 1 ø	1 1 1
	CONTROL		HIGH X & Y GRAPHIC INPUT		LOW X		LOW Y & XLOY	
ø ø ø ø	NUL ø	DLE 16	SP 32	ø 48	@ 64	P 80	` 96	p 112
ø ø ø 1	SOH 1	DC1 17	! 33	1 49	A 65	Q 81	a 97	q 113
ø ø 1 ø	STX 2	DC2 18	" 34	2 50	B 66	R 82	b 98	r 114
ø ø 1 1	ETX 3	DC3 19	# 35	3 51	C 67	S 83	c 99	s 115
ø 1 ø ø	EOT 4	DC4 20	$ 36	4 52	D 68	T 84	d 100	t 116
ø 1 ø 1	ENQ 5	NAK 21	% 37	5 53	E 69	U 85	e 101	u 117
ø 1 1 ø	ACK 6	SYN 22	& 38	6 54	F 70	V 86	f 102	v 118
ø 1 1 1	BEL 7 BELL	ETB 23	' 39	7 55	G 71	W 87	g 103	w 119
1 ø ø ø	BS 8 BACK SPACE	CAN 24	(40	8 56	H 72	X 88	h 104	x 120
1 ø ø 1	HT 9	EM 25	) 41	9 57	I 73	Y 89	i 105	y 121
1 ø 1 ø	LF 10	SUB 26	* 42	: 58	J 74	Z 90	j 106	z 122
1 ø 1 1	VT 11	ESC 27	+ 43	; 59	K 75	[91	k 107	{ 123
1 1 ø ø	FF 12	FS 28	, 44	< 60	L 76	\ 92	l 108	¦ 124
1 1 ø 1	CR 13 RETURN	GS 29	- 45	= 61	M 77	] 93	m 109	} 125
1 1 1 ø	SO 14	RS 30	. 46	> 62	N 78	^ 94	n 110	~ 126
1 1 1 1	SI 15	US 31	/ 47	? 63	O 79	_ 95	o 111	RUBOUT (DEL) 127

Note that either "LOY" column may be used for the XLOY byte, since bit 5 is not used.

Chapter 6

KEYBOARD

The ASSOCIATE keyboard is a selectric style keyboard with enhancements. It interfaces to the video processor board; for details (see Section 4.2, "Keyboard I/O").

Two keys have "local" functions which cause an immediate operation by the CRT processor. These keys are:

Local clear (control-delete), clears the CRT screen without affecting the host CPU. The 25th line remains unchanged.

Local clear (control-shift-delete), clears the CRT screen and the 25th line. The clock display remains unchanged.

Toggle key (RST, shift-RST, and control-RST) stops/starts the transfer of data to the CPU by toggling the Clear to Send (CTS) to the CPU.

Reset host key (Control-Shift-RST) unconditionally resets the host CPU.

The following features are also standard with the keyboard:

1) Redefinition of Keyboard - Keyboard PROM can be changed to change the codes generated by keyboard characters.

2) Electro-Capacitive Keyboard - The ASSOCIATE has an electro-capacitive keyboard. No mechanical contact is required to enter a character; a change of capacitance is detected on the underside of the board and that enters the character. Pressing a key changes the capacitance. All capacitive sensing is handled by a keyboard controller on the keyboard circuit board.

3) Repeat Functions - When a key is pressed the character is sent immediately to the video processor. If the key is held down for longer than 1/2 second the character is repeated at the rate of 10 characters per second.

4) CRT 25th Line - The CRT's 25th line can be downloaded in order to create prompts directly above the keyboard.

5) Selectric Format - The ASSOCIATE Keyboard is a standard selectric format.

6) Accounting Style Numeric Pad - The keyboard has an accounting style numeric pad with double wide zero and an ENTER key (the default value is the same as RETURN). The keypad keys are soft keys that can be downloaded from the host CPU as described in Chapter 5.

7) Special Purpose Keys - Several special purpose keys, such as escape, tilde, carat, and insert, are on the keyboard. All 128 ASCII codes (0 to 7FH) can be generated from the keyboard.

8) Cap Lock Key - The keyboard has a CAP LOCK key. The CAP LOCK causes all alpha characters to be transmitted as capital letters. It does not affect operation of the shift for non-alpha characters.

9) Function Keys - Four separate levels are possible on the function keys: NORMAL, SHIFT, CONTROL, and SHIFT CONTROL. Additional functions can be downloaded from the host CPU as described in Chapter 5.

10) Cursor Control - There are four cursor control keys (LEFT, RIGHT, UP, DOWN) plus a HOME key. Cursor control keys do not alter information, they reposition the cursor in the corresponding manner. HOME sends the cursor to the upper left corner of the screen. These five function keys can also be down loaded from the host CPU.

The table on the following page defines the eight standard combinations for each key in terms of the ASCII code generated:

TABLE 6.1 KEYBOARD CODE CHART

Key	Key Number	Normal	Shift	Ctrl	Ctrl-Shift
A	57	61	41	01	01
B	79	62	42	02	02
C	77	63	43	03	03
D	59	64	44	04	04
E	41	65	45	05	05
F	60	66	46	06	06
G	61	67	47	07	07
H	62	68	48	08	08
I	46	69	49	09	09
J	63	6A	4A	0A	0A
K	64	6B	4B	0B	0B
L	65	6C	4C	0C	0C
M	81	6D	4D	0D	0D
N	80	6E	4E	0E	0E
O	47	6F	4F	0F	0F
P	48	70	50	10	10
Q	39	71	51	11	11
R	42	72	52	12	12
S	58	73	53	13	13
T	43	74	54	14	14
U	45	75	55	15	15
V	78	76	56	16	16
W	40	77	57	17	17
X	76	78	58	18	18
Y	44	79	59	19	19
Z	75	7A	5A	1A	1A
1 !	20	31	21	31	21
2 @	21	32	40	32	00
3 #	22	33	23	33	23
4 $	23	34	24	34	24
5 %	24	35	25	35	25
6 '	25	36	27	36	27
7 &	26	37	26	37	26
8 *	27	38	2A	38	2A
9 (	28	39	28	39	28
0)	29	30	29	30	29
Space	90	20	20	20	20
Return	68	0D	0D	0D	0D
Bkspace	32	08	08	08	08
Tab	38	09	09	09	09
ESC |	19	1B	7C	1B	7C
^ ~	37	5E	7E	1E	7E
DEL CLR	55	7F	7F	DF	BF

Key	Number	Normal	Shift	Ctrl	Ctrl-Shift
- _	30	2D	5F	2D	1F
= +	31	3D	2B	3D	2B
[{	49	5B	7B	5B	7B
] }	50	5D	7D	1D	7D
; \	66	3B	5C	3B	1C
: "	67	3A	22	3A	22
, <	82	2C	3C	2C	3C
. >	83	2E	3E	2E	3E
/ ?	84	2F	3F	2F	3F
Function keys:					
Fn key 0	1	E0	C0	A0	80
Fn key 1	2	E1	C1	A1	81
Fn key 2	3	E2	C2	A2	82
Fn key 3	4	E3	C3	A3	83
Fn key 4	5	E4	C4	A4	84
Fn key 5	8	E5	C5	A5	85
Fn key 6	9	E6	C6	A6	86
Fn key 7	10	E7	C7	A7	87
Fn key 8	11	EF	CF	AF	8F
Fn key 9	12	E9	C9	A9	89
Cursor movement keys:					
Back	13	88	C8	A8	E8
Down	14	8A	CA	AA	EA
Up	15	8B	CB	9B	EB
Left	16	8C	CC	AC	EC
Home	17	9E	CE	8E	EE
Numeric pad keys:					
0	86	B0	D0	F0	90
1	69	B1	D1	F1	91
2	70	B2	D2	F2	92
3	71	B3	D3	F3	93
4	51	B4	D4	F4	94
5	52	B5	D5	F5	95
6	53	B6	D6	F6	96
7	33	B7	D7	F7	97
8	34	B8	D8	F8	98
9	35	B9	D9	F9	99
-	36	AD	DD	FD	BD
+	54	AB	DB	FB	BB
.	88	AE	DE	FE	BE
ENTER	72	8D	CD	9D	ED
"under-0"	87	BA	DA	FA	9A
"under-ENTER"	89	BC	DC	FC	9C

Chapter 7

PROM MONITOR

This section contains an overall description of the PROM Monitor and how it functions in the ASSOCIATE. At power up, or RESET, RAM is disabled and the system begins execution in the PROM at location 0. The first instruction is a jump into the F800 range and the second is an OUT DOH enabling RAM thereby entering its normal operating configuration. Entry into the PROM monitor disables the interrupts. The System Monitor will then attempt to boot the Disk Operating System. If the Disk Operating System cannot be loaded, a second RESET will take the Monitor to the command level.

To boot the Disk Operating System from Drive A, type the monitor command "A". After boot to disk, software can be used to disable PROM so that a full 65K of RAM will be available (see 3.2.1 Memory and 4.11 Status and Control for further detail). Return to the PROM Monitor from the CP/M Disk Operating system is accomplished by executing the program MNTR, which enables PROM and returns control to the PROM Monitor.

The following description of functions available in the PROM Monitor is in two parts: first, a brief introduction and complete listing of operator commands available through the PROM Monitor are presented; second, functions used by Monitor commands and also available to the user are described.

7.1 PROM Monitor Operator Commands

The PROM Monitor Operator Commands encompass many useful functions for working with memory and I/O. The commands perform functions such as testing, displaying, and changing memory, calculations involving addresses, performing basic I/O, and examining and changing registers. These commands are designed to give users a great deal of power in working with the processor at a machine level. The following table summarizes operator commands available through the PROM Monitor:

Summary of Commands

Command	Function	Page
A	Boot Disk Operating System Drive A(bottom)	
B	Boot Disk Operating System Drive B(top)	
C	Call External Subroutine	
D	Display Memory in Hex and ASCII	
F	Fill Memory	
G	Go to Address (optionally set breakpoints)	
H	Compute Hex Sum and Difference	
K	Calculate Check Value for Memory Range (to determine if memory accidentally modified)	
M	Move a Block of memory	
O	Calculate Relative Offset	
P	Make the ASSOCIATE a Terminal	
Q	Query I/O	
R	Read a Hex Tape	
S	Display/Alter Memory	
T	Test Memory (destructive)	
V	Verify One Memory Block Against Another	
X	Examine/Modify CPU Registers	
Y	Search Memory for String	

If the PROM Monitor is entered at startup or RESET, the System attempts to load the Disk Operating System. If the DOS is not successfully loaded a second RESET will give control to the Monitor command level. The message "GNAT System 10 Monitor Ver X" will be displayed followed by the Monitor prompt "?". After executing each operator command, with the exception of A (Boot to Disk) and, sometimes G (Go to), the prompt character is displayed. PROM Monitor Commands can be interrupted, to abort execution, by issuing a Control C. When Control C interrupts the execution of an Operator Command, Control again returns to the command level as signalled by a question mark. In separating command parameters, spaces or commas can be used interchangeably.

The following syntactic conventions will be used in specifying the format of each command:

a) Capitalized words (or letters) and symbols should be entered as shown;

b) Lower case letters or words enclosed by less than and greater than symbols indicate operator supplied parameters;

c) Items enclosed within square brackets can be optionally included, as needed.

Note that most of the operator commands are self-completing, but in some cases (such as when the number of parameters can vary) a RETURN will be necessary.

A Boot Disk system
Syntax: A

This command boots the disk operating system (CP/M in standard configurations) from Drive A(bottom) No parameters are needed.

B Boot Disk system
Syntax: B

This command boots the disk operating system (CP/M in standard configurations) from Drive B(top) No parameters are needed.

C Call External Subroutine
Syntax: C<transfer-address>[,<parm1>[,<parm2>]]

This command calls a routine external to the PROM Monitor. The external routine can return to the PROM Monitor by executing a "RET" instruction. One or two additional parameters can be supplied on the command line to the external routine; they will be passed in the H/L and D/E register pairs. If no additional parameters are supplied, zeroes are placed in the register pairs. Note that the saved Z80 registers in the user workspace are not altered by this command.

D Display Memory in Hex and ASCII
Syntax: D<start-address>,<end-address>

This command displays the contents of memory beginning at start-address and ending with the end-address. Memory is displayed in hexadecimal and ASCII with 16 bytes per CRT line. The starting location is displayed in hexadecimal at the beginning of each line.

F Fill Memory
Syntax: F<start-address>,<end-address>,<fill-character>

This command will propagate the fill-character (specified in hexadecimal) through memory from location start-address to end-address. The command is valuable in initializing a block of memory, or all of memory, to a constant value before loading a program; zero is especially useful for this purpose. As an example, the command F0,FFFF,0 fills memory with zeros.

G Go To Address
Syntax: G[<transfer-address>][,<breakpoint>[,<breakpoint>]]

This command allows transfer to another program while retaining some

Monitor control by setting breakpoints. A simple transfer to another program is executed if only transfer-address is specified on the command line. To set breakpoints, one or two addresses are added to the command. Note that this feature is software controlled, and breakpoints must occur on instruction OP-CODE in RAM. When a breakpoint is reached, the breakpoint address is printed and a Monitor prompt is given. Execution of the program can be continued by entering G or G,<breakpoint> if another breakpoint is to be implemented. The breakpoint is implemented by insertion of a RST7 instruction at the desired break location. After encountering the breakpoint the original instruction is restored. The processor status (contents of all registers) is saved in the monitor work space area.

H Compute Hex Sum and Difference
Syntax: H<start-number>, <end-number>

This command computes and displays the sum (start-number + end-number) and difference (start-number - end-number) of two hexadecimal numbers, where the numbers range between 0000H and FFFFH. If start-number is less than end-number, the result is equal to start-number +10000H - end-number.

K Calculate Check Value for Memory Range
Syntax: K<start-address>,<end-address>

This command computes and prints a 16-bit check value for a memory range: it is useful for determining if a memory range has been accidentally modified. The check value is calculated by the CRC equation: g(x)=X(16)+X(12)+X(5)+X.

M Move a Block of Memory
Syntax: M<start-address>,<end-address>,<destination-address>

This command moves the contents of a block of memory beginning at start-address and ending at end-address to another block of memory starting at destination-address. Caution should be used with this command in order to prevent the unintentional destruction of memory locations which should remain unchanged. Note that wrap around from FFFFH to 0000H takes place if the source or destination block of memory goes past FFFFH.

O Calculate Relative Offset
Syntax: O<jump-address>,<destination-address>

This command calculates offset for relative jump instructions. Jump-address is the address of the jump instruction, and destination-address is the address of the instruction jumped to. If destination is out of the 256 byte range, an "XX" will be printed.

P Port Echo
Syntax: P<serial-port>,<duplex>

The ASSOCIATE becomes a terminal with connection through the MODEM, LIST, or NETWORK I/O PORT. The CTRL-SHIFT-RST KEY will cause an exit to the Monitor. For <duplex>, a 1 selects full duplex mode and a 0 selects half duplex. This does not accept null characters. Use 80H for a null character.

Q Query I/O
Syntax: QO<port>,<value>
QI<port>

This command examines any input port or sends a value to any output port; it gives the operator a direct input/output capability from the keyboard. For example the baud rate could be changed on the list port baud rate generator by issuing:

QO:E0,77

Baud Rate Code

Baud Rate Generator

Colon provided by monitor

Output Command

Another example of the command's use might be to go to one of the I/O ports for checkout of external devices, for instance, to check input from the MODEM, issue: QI70. The computer would respond with the value found at port 70H.

R Read a Hex Tape
Syntax: R[<bias>]

This command reads check-summed hex files in the normal Intel format. A bias can be added, which will cause the object code to be placed in a location other than its intended execution location. The bias is added to what would have been the normal loading location and will wraparound to enable loading any program anywhere in memory. If non zero transfer address is received, the monitor transfers control directly to the program.

S Display/Alter Memory
Syntax: S<start-address>

This command displays, and allows modification of, memory on a byte-by-byte basis. The byte at the start-address is displayed in hexadecimal; if the value of start-address location is to be changed, the new value is entered followed by a space, otherwise entering only a space will cause display of the hexadecimal value at the next location. To terminate execution of this command, enter a RETURN. The system adds a carriage

return and line feed before displaying continuation locations with address ending with a zero or eight; the present address location is printed after each system issued carriage return and line feed.

T Test Memory (Destructive)
Syntax: T<start-address>,<end-address>

This command uses a very fast pseudo-binary sequence generator with a period of 256 bytes to test memory. The period is relatively prime to 256 and, thus, provides a good test of pattern sensitivity. Note that each number in the range 0-255 is generated by the algorithm; therefore, each bit in the range is tested to see if both zero and one bits can be written into it. Error information is displayed in the form of an address and bit number. The memory chip with the location which failed the test can be quickly determined by reference to the appropriate schematic.

V Verify memory
Syntax: V<start-address>,<end-address>,<compare-address>

This command compares the contents of the block of memory delineated by start-address and end-address to the block of memory beginning at compare-address; wraparound takes place if the compared addresses exceed FFFFH. Differences in the contents of the two memory blocks are reported in the form of address and the contents of the two locations.

X Examine/Modify CPU Registers
Syntax: X['][<register-name>]

This command displays the contents of the CPU registers; if the register-name is specified, contents of the register can be changed (or not) by specifying the new contents or a space. To display the normal system status enter only an X. To display the additional Z80 registers, enter X'. Single "prime" registers may be examined and modified in the same way as with "unprimed" registers described above.

Y Search Memory
Syntax: Y<search-string>

This command searches all memory starting at location zero for the byte string specified by search-string. Hex characters are separated by commas in specifying the search-string and up to 255 may be indicated. The starting address of each byte string found to be identical to search-string is displayed by the command.

7.2 PROM Monitor Entry Points

The following functions are available to user programs and can simplify the handling of I/O from system to system; they are also used by PROM Monitor operator commands. The functions are accessed by calling to the location specified in the Assembly listing. Whatever the currently

assigned device, these functions will perform the specified I/O operation and return to the calling program. Register conventions are as follows for any input or output device: the character to be output is in the C register and the return character will be in the A register after input or output. The functions are:

ADDRESS	NAME	FUNCTION	PARAMETER
F803	CI	CONSOLE INPUT	"A" RETURNED WITH CHAR
F806	RI	READER INPUT	"A" RETURNED WITH CHAR
F809	CO	CONSOLE OUTPUT	"C" OUTPUT TO CONSOLE
F80C	PO	PUNCH OUTPUT	"C" OUTPUT TO PUNCH
F80F	LO	LIST OUTPUT	"C" OUTPUT TO LIST
F812	CSTS	CONSOLE STATUS	"A" RETURNED WITH STATUS
F815	IOCHK	I/O CHECK	"A" RETURNED WITH IOBYTE
F818	IOSET	I/O SET	"C" PUT INTO IOBYTE LOCATION
F81E	USET	INITIALIZE I/O	NONE
F824	DATE	DATE CODE ID	
F826	TRAP	RESTART BREAKPOINT	NONE
F829	PRINT	PRINT ON CONSOLE	PRINT FROM DE TILL 00 FOUND
F82C	BOOT	LOAD FIRST SECTOR AND RUN	NONE

Chapter 8

SERVICE PROCEDURES

This chapter describes the service procedures for troubleshooting and testing the ASSOCIATE computer family. This information is intended only for the technically oriented and experienced service person.

You will find that this manual will give you most of the information you need to troubleshoot and repair the ASSOCIATE on a module basis. Repairing the various modules is a Depot function and should be referred to your nearest Depot Repair facility. Field repair should be limited to replacement of the modules only.

Operation of the machine will give you most of the initial clues you need to troubleshoot problems. Carefully note any symptoms. Try to duplicate the problem, using the operations which were in progress when trouble was first noted. Many problems can be traced to improper operation or faulty software/media. A list of potential troubles and the appropriate actions follows.

SOME THINGS TO REMEMBER

```
**********************************************************************
***                          CAUTION                               ***
***        Dangerous voltages are present in this unit.            ***
***     It is advised that personnel working inside of the         ***
***  ASSOCIATE or any electrical equipment should NOT wear         ***
***                   metal jewelry or watches.                    ***
***       Donot unscrew metal parts,disconnect cables,             ***
***           orremove components with the power on.               ***
**********************************************************************
```

Observe cable connector polarity--
The pin 1 arrows on jack and cable connector must align.

HOW TO USE THE TROUBLESHOOTING CHART TO SOLVE PROBLEMS

Before consulting the TROUBLESHOOTING CHART, attempt to verbalize the difficulty you have encountered in a meaningful sentence. For example, "It doesn't work." is not nearly as descriptive as, "Fan does not run and video display is dark." The first statement isn't very helpful but the second statement might have a simple solution as: "Is the unit plugged into a working 120 VAC outlet?" or "Is the AC Line fuse blown?"

Now that you have a description of the problem, see column 1 of the TROUBLESHOOTING CHART for a match. Column 2 will explain the possible failure and column 3 will tell you what to check.

If you need further information after the TROUBLESHOOTING CHART has directed you to a possible solution, see the column 4 for a FIGure or SECtion number to refer you more tests or the probable cause of the trouble.

ASSOCIATE TROUBLESHOOTING CHECK-LIST

PROBLEM DESCRIPTION	PROBABLE CAUSE	REPAIR ACTION	REFER TO
Continuous beep	Sticking keyboard key	Refit jammed key Adjust keyboard	SEC 8.2
	Video Processor failure	Replace 1005 pcb	SEC 8.3.1
Keys beep when pushed	Illegal operation	Check Oper. Man.	
	BIOS failure	Run diagnostics	
Cooling fan inaudible	No 120 VAC power	Plug unit in	
	Blown fuse	Check power fuse	
	Fan unplugged/bad	Check connection or replace	SEC 8.3
No disk drive noise but fan is OK	Auto power-down	30 sec inactivity	CP/M
	Bad diskette	Reboot another one	CP/M
	Not rebooting "A"	CTRL-SHFT-RESET	CP/M
	Disk drive failure	Replace drive assy	SEC 8.3.2
	Power Supply fail	Replace supply	
Unusual noise	Bad fan bearing	Replace fan	SEC 8.3
	Disk drive fail or diskette fail	POWER DOWN NOW!!! and replace	
	Power supply fail	adjust or replace	SEC 8.3.2
Character dot fade or twinkle	Power failure	Adjust pow. supply	DEPOT*
	Unit is too hot	Fan working?	
	Video process fail	Run Disk tests	Sys disk
		Replace 1005 board	SEC 8.3.1
Incorrect char appears	Improper SHFT/CTRL	Check Oper. Manual	
	Sticking kybd keys	Clean/replace kybd	SEC 8.2
	CPU failure	Run Disk Tests	Sys disk
	Video process fail	Replace 1005 board	SEC 8.3.1
Improper boldface or high intensity raster	Video process fail	Run TPAT test	Sys disk
		Replace 1005 board	SEC 8.3.1
	Brightness too high	Adjust it lower	Below CRT
Typed char appears in more than one place at the same time	Memory failure on main CPU board	Run MTEST	Monitor
		Replace 1000 board	SEC 8.1
Typed char appears in more than one place at the same time	Memory failure on video board	Run TCRT	Sys Disk
		Replace 1005 board	SEC 8.3.1

PROBLEM DESCRIPTION	PROBABLE CAUSE	REPAIR ACTION	REFER TO
Missing characters or inoperative keys	Correct Oper. Sys.? Keyboard/video fail	Check diskette Replace kybd/1005	CP/M SEC 2
Garbage displayed	CPU non-operative Video process fail Power Supply fail	Replace 1000 board Replace 1005 board Adjust/replace	SEC 8.1 SEC 8.3.1 SEC 8.4.2 DEPOT*
Bad raster, stretched compressed, deformed or rolling chars.	CRT out of adjust Video process fail Power supply fail	Adjust/Replace Run TPAT test Replace 1005 board Adjust/replace	DEPOT* Sys disk SEC 8.3.1 SEC 8.3.2 DEPOT*
Screen blank	Unit turned on? Brightness too low Video process fail CPU inoperative Power Supply fail	Plug in/turn on Adjust brighter Run TPAT test Replace 1005 board Replace 1000 board Adjust/replace	CP/M Below CRT Sys disk SEC 8.3.1 SEC 8.1 SEC 8.3.1 DEPOT*
Cursor not present (cursor might be turned off by software - try to reboot)	Does keyboard work?	YES? Bad Diskette Run MTEST NO? Bad 1005 or 1000 boards	CP/M Monitor SEC 8.3.1 SEC 8.1 DEPOT*
Cursor does not blink	Does keyboard work?	YES? Run MTEST NO? Failed 1005	Monitor SEC 8.3.1
Keys don't respond	During a prog. run? Try running tests Does unit boot? Run another program Failed CPU/Video	Strike CNTL-S once Perform disk test Try rebooting Bad diskette Replace 1005/1000	CP/M Sys disk CP/M CP/M SEC 2
Single key fails	Run another prog. Memory fail Sticking key CPU failure Video process fail Keyboard failure	Bad diskette Run MTEST Clean/replace Run Disk tests Replace Replace	 Monitor SEC 8.2 Sys disk SEC 8.3.1 SEC 8.2
Multiple keystrokes	Key held down or sticking Video process fail	Auto REPEAT Clean/replace Run Disk tests Replace 1005 board	 SEC 8.2 Sys disk SEC 8.3.1

8.2 Diagnostics

The following tests are used to check out various components. Errors are indicated by the audible tone and asterisks at the beginning of the displayed error line. Upon error the programs will wait for an operator input before proceeding. The tests are generally invoked by entering the name of the test at the System level followed by a Carriage Return. Prompts will ask for essential user-supplied information.

8.2.1 TSERIAL, TRS232 - Serial Port Test

These two programs perform the same tests on serial ports; they should be utilized whenever a user wants to check the correct action of a serial port--ports 60H, 70H or 72H. TSERIAL automatically tests the indicated ports. TRS232 tests individual ports as directed by the operator. In order to use these tests, a loop-back plug with the following pins connected together is required:

2 - 3, TxData to RxData
4 - 5, RTS to CTS
6 - 20 DSR to DTR (CD)

The test is invoked from CP/M by the following:

```
A0>TRS232  or  A0>TSERIAL
```

TRS232 will inquire for the number:

```
TEST PORT # IN HEX -
```

If the port is error free:

```
BAUD RATE = xxx
NO DATA ERRORS DETECTED
PORT 70 TEST COMPLETE
```

To return to CP/M, reply to the port # query with any character which is not a hex number.

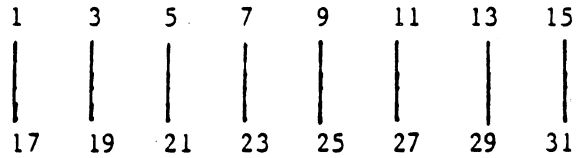
Error messages which may appear include:

```
***  CD/DSR not going on
***  CD/DSR not going off
***  CTS not going on
***  CTS not going off
***  Timeout error (possibly non-existent port)
```

8.2.2 TPIO

TPIO tests the the operation of the Parallel I/O port. For proper operation, TPIO must have the TFX003 test fixture installed in the 50-pin parallel connector on the back panel.

The test fixture is a parallel loopback plug with the following pins connected:



The PIO test is invoked by:

```
A0>TPIO
```

The program will respond with

```
TPIO - TEST PIO V1.00 as of 29-March-80
Test Complete
```

or give one of the following errors:

```
*** Output error - (port). Data = ww, Port # xx = yy. Error = zz
*** Input error - (port). Data = ww, Port # xx = yy. Error = zz
*** Timeout, data=vv, Port ww (Output)=xx, Port yy (Input)=zz
```

8.2.3 TAPU,T9512 - Arithmetic Processor Test

These programs test the optional arithmetic processor--AM9511or AM9512. TAPU repeatedly tests the AM9511 operations of: multiply, divide, SIN, ARCTANGENT, exponentiation, and power. T9512 repeatedly tests of the operations of add, subtract, multiply, and divide. The results of each function is compared with the expected result stored in the program. Any error is indicated by a printout of actual result and anticipated result.

Setup requires that the AM9511 or AM9512 and required jumpers be installed. To invoke:

```
A0>TAPU
```

or

```
A0>T9512
```

Type any character to abort the test. The following error message may result from this test:

```
*** 9511 (function) error- xxxxxxxx  expected result-yyyyyyyy
```

8.2.4 TBAUD - Baud Rate Generator Test

This diagnostic tests each port through all 16 possible baud rates. A software timing loop measures the time between sending successive characters at a given baud rate and compares that value with an expected value, giving a resolution of about 35 usec. Any difference is an error. If the test fails, port number, baud rate, expected result, and actual result are displayed. The test should be run when errors are detected in trying to set baud rate.

Setup requires serial loopback plugs on ports 70 and 72. TBAUD is invoked by the following:

```
A0>TBAUD
```

Error messages which may appear are:

```
*** Timeout, Baud rate xxx, baud port yy, test values=(expected)
    (actual) possibly no loop back
*** Error, Baud rate xxxx, baud port yy, test values - (expected)
    (actual)
```

8.2.5 TPAT - Pattern Test

TPAT causes the video board to fill up every character position on the CRT--all 25 lines and 80 characters. In addition it shows every character in the character PROM at both high and low intensity. This program allows inspection of the character set and the CRT raster. To invoke:

```
A0>TPAT
```

To get out of the Pattern Test enter a Control-Shift-RST or press the Reset switch on the back of the ASSOCIATE.

8.2.6 TCTC - Counter Timer Test

This test checks the counter timer chip to determine if it interrupts and times at the proper rate. There are four different timer circuits in the chip. For testing, each timer circuit is set up for a different rate. The program is then set to execute for a specified amount of time. The interrupts over that period of time are counted; if the count doesn't come out exactly right, TCTC indicates that the test failed. The Counter Timer Test is invoked from CP/M by the following:

```
A0>TCTC
```

The system will reply as follows when the Counter Timer checks out with no problem:

```
CTC - Test System 10 CTC Chip  V1.1 as of 23-JAN-80
CTC Test Complete
```

The error message is:

```
*** CTC test failed
Actual:   (ct0) (ct1) (ct2) (ct3) (other ints)
Expected: (ct0) (ct1) (ct2) (ct3) (other ints)
```

8.2.7 TCRT - CRT Test

This test exercises the CRT processor. It consists of several subtests:

PROM checksum. A checksum is made of the PROM data and compared against a table in the TCRT program. In the event of an error, a message is printed on the screen and the test holds at that point.

RAM. The CRT scratchpad RAM is tested. Any errors detected are printed on the screen.

VIDEO RAM is tested in two parts. The top half of the screen is tested first. If any erros are detected, the erring locations are listed in the bottom half. Upon successful completion the bottom half is tested in the same manner.

To invoke TCRT, enter the following:

```
A0>TCRT
```

To end the test, enter two Control C's.

The error message is:

```
Ram error(s) at vvvv. . wwww. . xxxx. . yyyy. . zzzz
```

8.2.8 TDISK - Disk Drive Test

TDISK provides options for testing the disk drives; the options are indicated after prompts during execution of the diagnostic program. The program indicates sectors and tracks under test. At the end of each pass, TDISK displays the number of accumulated errors. The number of read attempts is determined by the system BIOS. With the normal ten try BIOS the error rate should be less than one error per 1000 passes.

```
* ********************************************************
*                                                        *
*     Note: Testing destroys all data on a disk.         *
*             Exercise care in disk selection.           *
*                                                        *
**********************************************************
```

To see if a disk can be read, DUMP validate can be used.

To invoke TDISK:

```
A0>TDISK
```

Control C aborts the test.

8.2.9 TDMA

This program tests the memory-to-memory DMA function. The process is accomplished by repetitively testing DMA memory-to-memory transfers. To use:

```
A0>TDMA
```

Test results may include the following error messages:

```
*** DMA modified location xxxx from yy to zz
*** DMA transfer error at xxxx should be yy but is zz
```

8.2.10 TINT

This program tests that all interrupt-generating devices can generate interrupts simultaneously. The process includes configuring devices for interrupts and testing if each device generates interrupts.

The devices are configured as follows:

SIO	Ports 60, 70, and 72 setup for transmit and receive interrupts.
PIO	Setup as in TPIO
CTC	Setup as in TCTC, but with lower frequency interrupts.

Loop back test fixtures are required in the serial and parallel ports.

After delaying for a specified number of software loops, the program tests if all devices have generated interrupts.

To use:

```
A0>TINT
```

Test result error messages which may appear:

```
*** No interrupts from CTC port 0
*** No interrupts from CTC port 1
*** No interrupts from CTC port 2
*** No interrupts from CTC port 3
*** No interrupts from PIO port A
*** No interrupts from PIO port B
*** No interrupts from SIO port 70 - receive
*** No interrupts from SIO port 70 - xmit
*** No interrupts from SIO port 72 - receive
*** No interrupts from SIO port 72 - xmit
*** No interrupts from SIO port 60 - receive
*** No interrupts from SIO port 60 - xmit
```

8.2.11 TRTC - Test Real Time Clock Option

TRTC exercises and tests the real time clock option, The program performs the following functions:

1. Displays the current time.
2. Monitors any interrupts generated by the Real Time Clock
3. Allows the user to set the time and date.
4. Allows the user to set the RTC interrupt mask.
5. Allows the user to reset each individual counter and latch
6. Performs the system clock test. This test compares the RTC timing with the system clock timing.
7. Performs the "pulse test" for fine tuning the Real Time Clock crystal.

USER ENTRY	COMPUTER RESPONSE
TRTC	Computer prompts user with options

8.2.12 TSPD - Test Disk Rotational Speed

TSPD tests the rotational speed of either the A or B disk drive. It is executed by:

```
A0>TSPD
```

A prompt menu gives the user the choice of running the rotational test, selecting the drive to test, or returning to the Operating System. Using the System clock the test operates by measuring the time it takes the diskette to make five revolutions (one second's worth). This time is converted to Revolution per Minute for display on the screen. an error message will be displayed if no Index Pulse is found.

Tandon and MPI specify 1.5% speed tolerance on the disk drives. This corresponds to an error of + or - 4.5 RPM.

8.3 Disassembly and Reassembly

This section provides information for disassembly and reassembly of the major components of the ASSOCIATE. Again, only qualified technical personnell should attempt to disassemble the Microcomputer. Improper reassembly or operation may damage the unit and void the warranty.

```
**********************************************************************
***                          CAUTION                               ***
***       Dangerous voltages are present in this unit.             ***
***     It is advised that personnel working inside of the         ***
***  ASSOCIATE or any electrical equipment should NOT wear         ***
***                  metal jewelry or watches.                     ***
***       Donot unscrew metal parts,disconnect cables,             ***
***           orremove components with the power on.               ***
**********************************************************************
```

The ASSOCIATE Case is made out of injection molded structual foam. Individual components are mounted to an internal metal frame that provides mechanical support and electrical shielding.

8.3.1 Main Board

The main CPU board is accessible by removing the two screws at the lower rear panel. When these are removed, the main board slides out on tracks from the back of the case. Three cables pull out with the board allowing operation of the board outside the case.

To reassemble, slide the cables in ahead of the main board. The cables will roll back to lay across the top of main board.

8.3.2 Keyboard

To detach the keyboard assembly, remove the two screws which hold the keyboard cover to the bottom piece. These screws can be accessed from the bottom of the unit. The cover can be then be tilted up giving access to the keyboard.

The keyboard is attached with four screws which can be removed from the bottom of the case.

Key tops can be replaced by simply lifting them off, because they are attached by a press fit. If the key switches beneath the key tops need to be taken off, the bottom circuit board must be removed from the keyboard frame.

Note that the PROM for the keyboard is located at Z12 at the upper right side of the keyboard.

8.3.3 Anti-Glare Screen

The front screen is attached to the front assembly by Velcro attachments. The screen may be lifted with a blunt knife in the corner of the frame.

8.3.4 Top Cover and Front Bezel

Two bolts hold the top cover to the bottom piece. These bolts are located on the lower back of the unit. An ordinary philips screwdriver can be used.

After loosening these two bolts, the cover will swing up and forward. It can be removed and set aside giving complete access to the system components.

After removing the cover, the front bezel can now be removed. It is held in by indents in the cover and an overhanging hinge on the bottom.

8.3.5 Disk Drives

They may be removed by the following procedure:

1. Remove the Cover and Front Bezel
2. Remove the screw in between the drive assembly and CRT which holds the disk assembly side plate to the power supply bracket.
3. Take out the four screws on the outside of the drives.
4. Disconnect the ribbon cables and the power cables from the rear of the disk drives.
5. Slide the disk drives forward and out.

Note that the drive on the bottom is set up as drive A and the top as drive B. The jumper options and termination resistors must be correctly set on the drives.

Drive Jumper Set Up

Pin #'s	Drive Label	A	B
1-16	H	SHORT	SHORT
2-15	DS0	SHORT	OPEN
3-14	DS1	OPEN	SHORT
4-13	DS2	OPEN	OPEN
5-12	DS3	OPEN	OPEN
6-11	MUX	OPEN	OPEN
7-10	SPARE	OPEN	OPEN
8-9	SPARE	OPEN	OPEN
RESISTOR NETWORK		REMOVED	INSTALLED

Drive interface pin 34 must be jumpered to ground on disk drives which do not have the signal "ready" on this pin.

8.3.6 Video Board

The video board is mounted vertically with four press fit attachments in back of the CRT unit. To remove:

1. Remove the Cover and Front Bezel
2. Disconnect all cable to the 1005 board.
3. Pull off the 1005 board up with gentle pressure.

On reassembly, be sure to connect all cables to their proper socket. Incorrect connection may damage unit. Specifically, the connector to the CRT must be correct! And the keyboard cable must be correct! On these cables Pin 1 of the cable must match pin 1 of the proper connector.

8.3.7 Power Supply

To remove the power supply unit at the bottom of the disk drives:

1. Remove the Cover and Front Bezel
2. Remove the Disk Drive assembly.
3. Remove the DC distribution power cable and the AC wiring from the supply.
4. Detach the power supply by removing the four top mounting screws.

8.3.8 CRT

To take out the CRT, the entire mounting frame must be removed from the case. To do this, follow the procedure below:

1. Remove cover and front bezel.
2. Remove the 1005 Video Processor Board.
3. Remove the AC Cable to the Power Supply.
4. Take out the six bolts holding the metal frame to the bottom section and remove the entire assembly.
5. Unbolt the CRT from the metal frame.

8.4 Return of Material

In the event that equipment must be returned for repair, it should be suitably packed for shipment. Failure to package properly may result in voiding the warranty or violating the terms of the service contract.

If the ASSOCIATE was purchased from a system house or dealer, contact them rather than Data Technology. For return to Data Technology, call customer service to obtain instructions and return authorization.

ASSOCIATE FEATURES

GENERAL

- Attractive Desktop Cabinet
- Portable
- Selectric Style Keyboard
- Software Definable Function Keys
- Accounting Style Numeric Pad
- Low Glare Screen
- Full Screen Editing

HARDWARE

- Z80A CPU
- 65K RAM
- 700K Mass Storage on Dual Minifloppys
  - Optional 1.6 Megabytes
  - Optional Hard Disk
- DMA Data Transfer
- Hard Disk Interface for Additional Mass Storage
- 2 RS232 Serial Ports (Printer and Modem)
- 1 RS449 Serial Communication Port to 500K Baud
- Programmable Baud Rates
- Separate CRT Microprocessor
- IEEE 488 GPIB Parallel I/O*
- High Speed Arithmetic Processor*

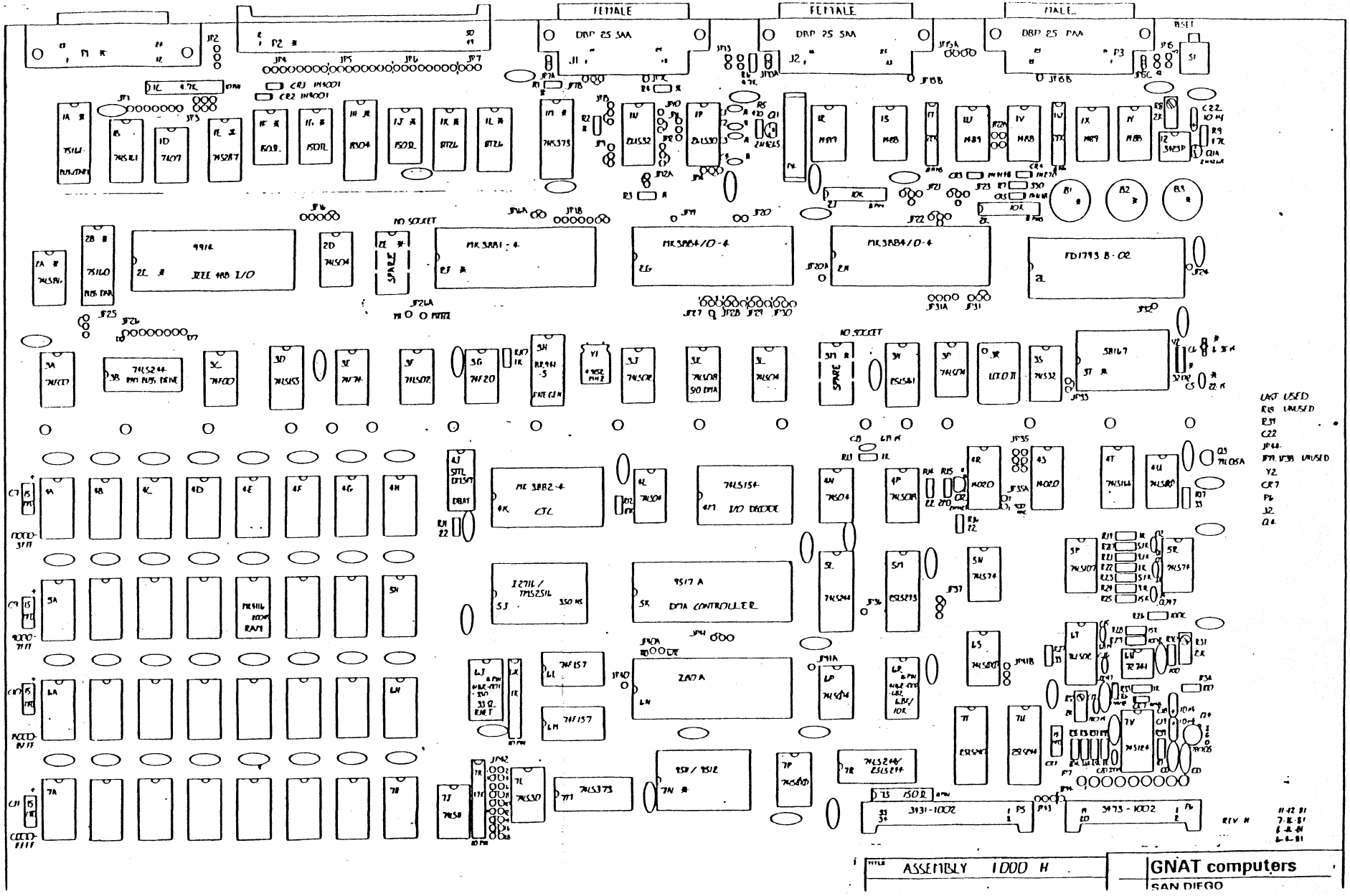
SOFTWARE

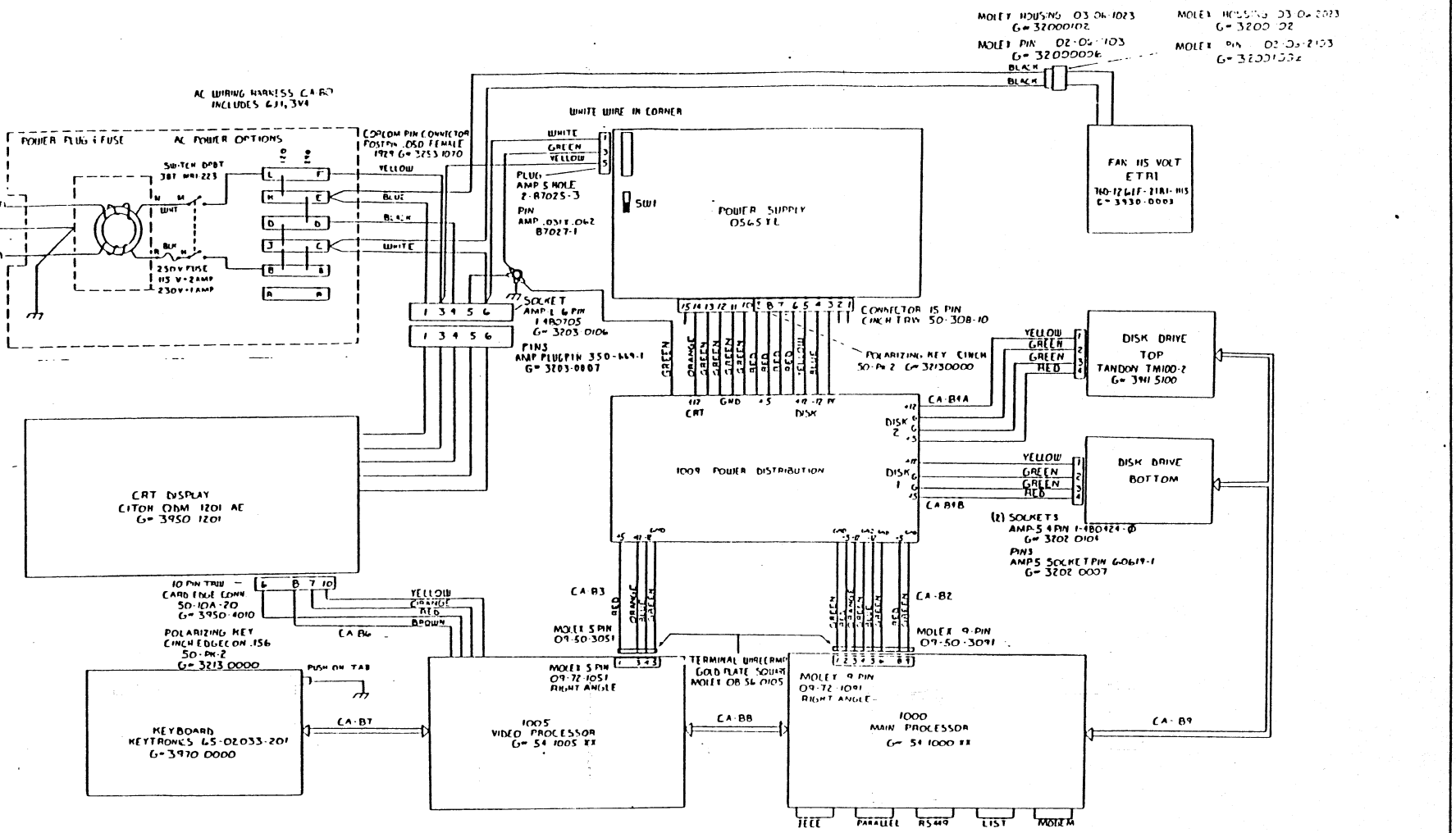
- PROM Resident Disk Boot and Diagnostic Monitor
- CP/M** Version 2 Disk Operating System
- Screen-Oriented Editor
- Word Processing Program*
- Business Software*
- Communications Software*
- Extensive Software Support*

BASIC	FORTRAN	PASCAL	RATFOR
COBOL	ASSEMBLER	PL/1	"C"

*Optional

**Trademark of Digital Research


FEMALE
FEMALE
MALE
DBP 25 SAA
DBP 25 SAA
DBP 25 PAA
NO SOCKET
NO SOCKET
9914
IEEE 488 I/O
MK 3881-4
MK 3884/0-4
MK 3884/0-4
FD1793 B-02
SPARE
SPARE
MK 3882-4
CTC
74LS154
I/O DECODE
9517 A
DMA CONTROLLER
Z80 A
74LS244
74LS244
74LS244
74LS244
74LS373
74LS373
74LS30
74LS244
74LS244
3431-1002
3473-1002
LAST USED
R18 UNUSED
R39
C22
JP44
JP1, JP3B UNUSED
Y2
CR7
P6
J2
Q4
REV H
ASSEMBLY 1000 H
GNAT computers
SAN DIEGO



DO NOT USE 110 OR 220 OPTIONS ON 6J1. THEY ARE NOT CONNECTED

FOR 115 VOLT OPERATION (120 OPTION)

1. SET SW1 TO 115 ON 0565TL POWER SUPPLY
2. SWITCH 6J1 JUMPER OPTION TO 120 POSITION (JUMPER OPTION CARD SHOULD BE REMOVED FROM BOTTOM OF FUSE HOLDER & REINSERTED WITH 120 SHOWING).
3. INSTALL 2 AMP FAST BLOW FUSE IN 6J1.
4. PLACE 120 VOLT STICKER ON 6J1.

FOR 230 VOLT OPERATION (240 VOLT OPTION)

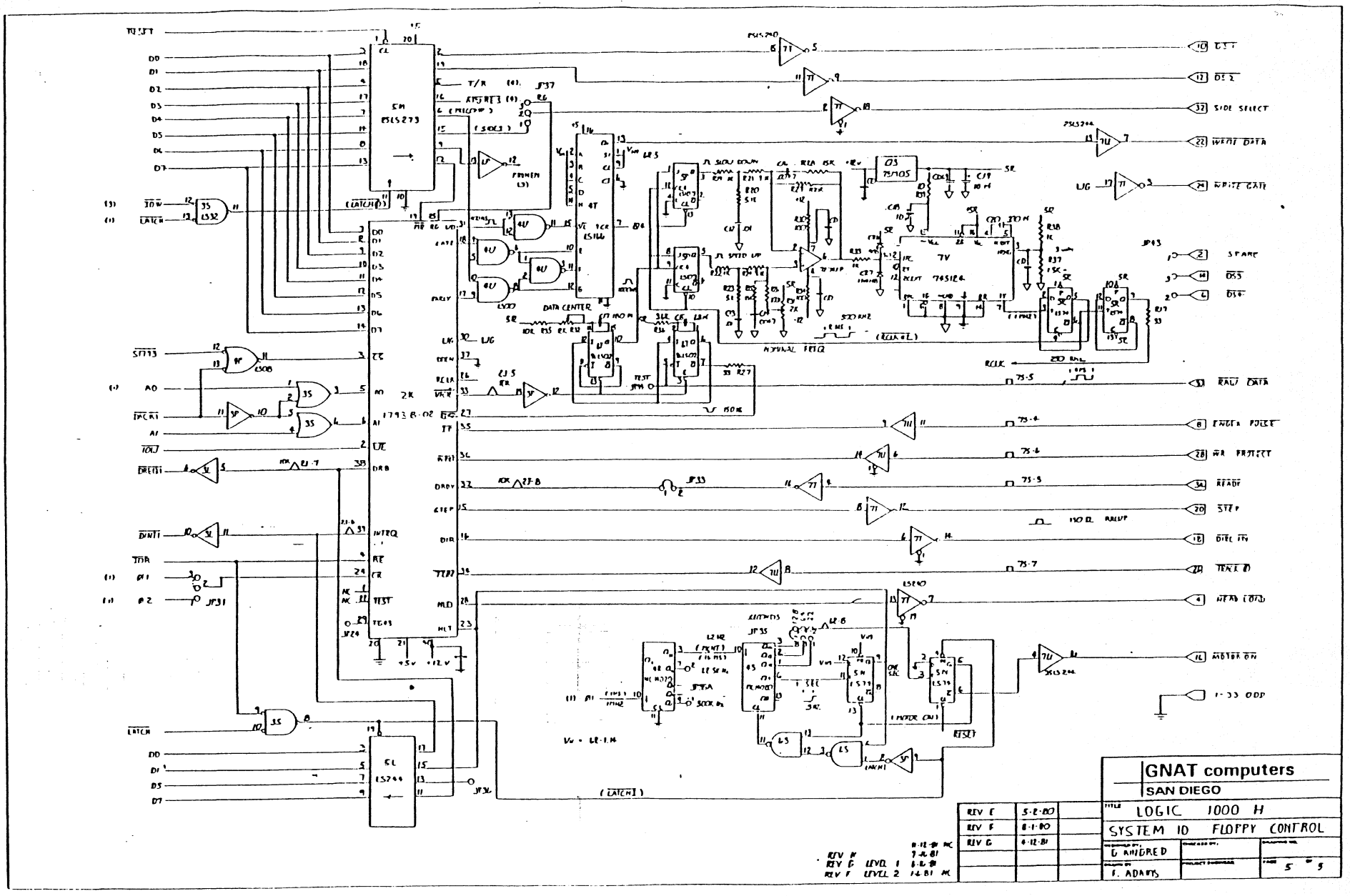
1. SET SW1 TO 230 ON 0565TL POWER SUPPLY.
2. SWITCH 6J1 JUMPER OPTION TO 240 POSITION (JUMPER OPTION CARD SHOULD BE REMOVED FROM BOTTOM OF FUSE HOLDER & REINSERTED WITH 240 SHOWING).
3. INSTALL 1 AMP FAST BLOW FUSE IN 6J1.
4. PLACE 240 VOLT STICKER ON 6J1.

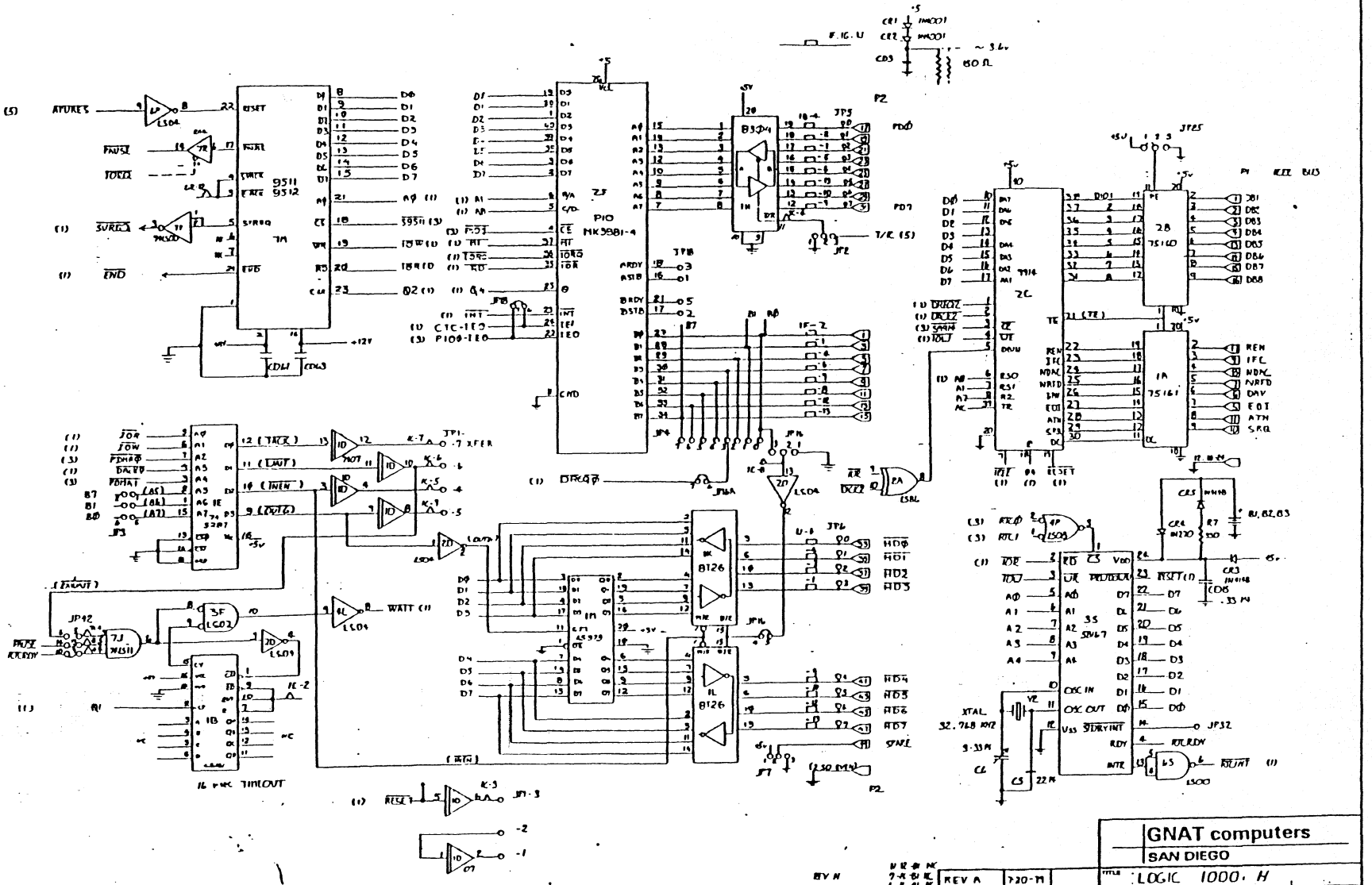
	9-2-81	

GNAT computers
SAN DIEGO

TITLE: SYSTEM 10 VERSION 2.0
WIRING DIAGRAM

DRAWN BY: T. WRIGHT


GNAT computers
SAN DIEGO
LOGIC 1000 H
SYSTEM 10 FLOPPY CONTROL
G KINDRED
F. ADAMS
REV E 5-2-80
REV F 8-1-80
REV G 4-12-81
REV H 11-12-81 MC
REV G LEVEL 1 7-16-81
REV F LEVEL 2 1-6-81
5 OF 5
DS1
DS2
SIDE SELECT
WRITE DATA
WRITE GATE
SPARE
DS3
DS4
RAW DATA
INDEX PULSE
WR PROTECT
READY
STEP
DIR IN
TRK 0
HEAD LOAD
MOTOR ON
1-33 ODD
DATA CENTER
NOMINAL FREQ
SLOW DOWN
SPEED UP
RESET
(MOTOR ON)
(LATCH)
LATCH
IOW
IOR
DRQ1
DRQ2
DACK1
IOCS1
INTRQ
DRQ
DRDY
STEP
DIR
TRK0
MLD
HLT
WPT
RDY
T/R
JP37
JP33
JP31
JP24
JP35
JP43
5M
LS273
4T
LS166
2K
1793B-02
5L
LS244
LS32
LS08
LS240
LS74
74S124
75S05
74LS14
+5V
+12V


GNAT computers
SAN DIEGO
LOGIC 1000-H
SYSTEM 10 PARALLEL I/O
D KINDRED
J. ADAMS
REV A 7-20-79
REV B 11-8-79
REV C,D 1-3-80
REV E 3-2-80
REV F 8-1-80
REV H 9-21-81
REV G 5-21-81
LEVEL 2 1-6-81
10-15-80
LEVEL 1 9-1-80
9511
9512
PIO
MK3881-4
8304
8126
8T26
75160
75161
2C
1A
2B
LS04
LS00
LS08
LS09
LS32
LS86
LS138
LS244
LS367
LS374
LS393
LS670
AS299
AS645
AS688
AS1000
AS1002
AS1003
AS1004
AS1005
AS1006
AS1007
AS1008
AS1009
AS1010
AS1011
AS1012
AS1013
AS1014
AS1015
AS1016
AS1017
AS1018
AS1019
AS1020
AS1021
AS1022
AS1023
AS1024
AS1025
AS1026
AS1027
AS1028
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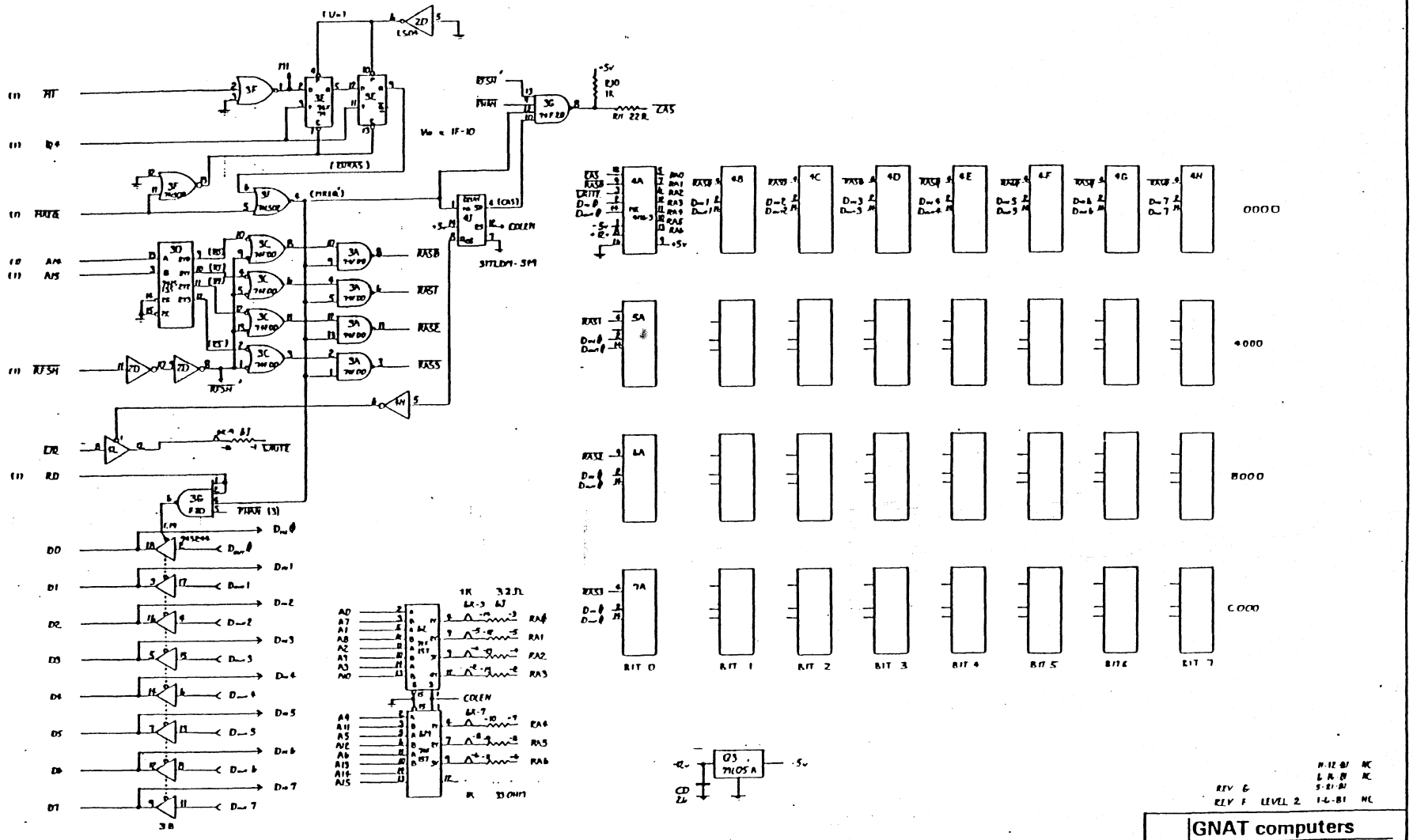
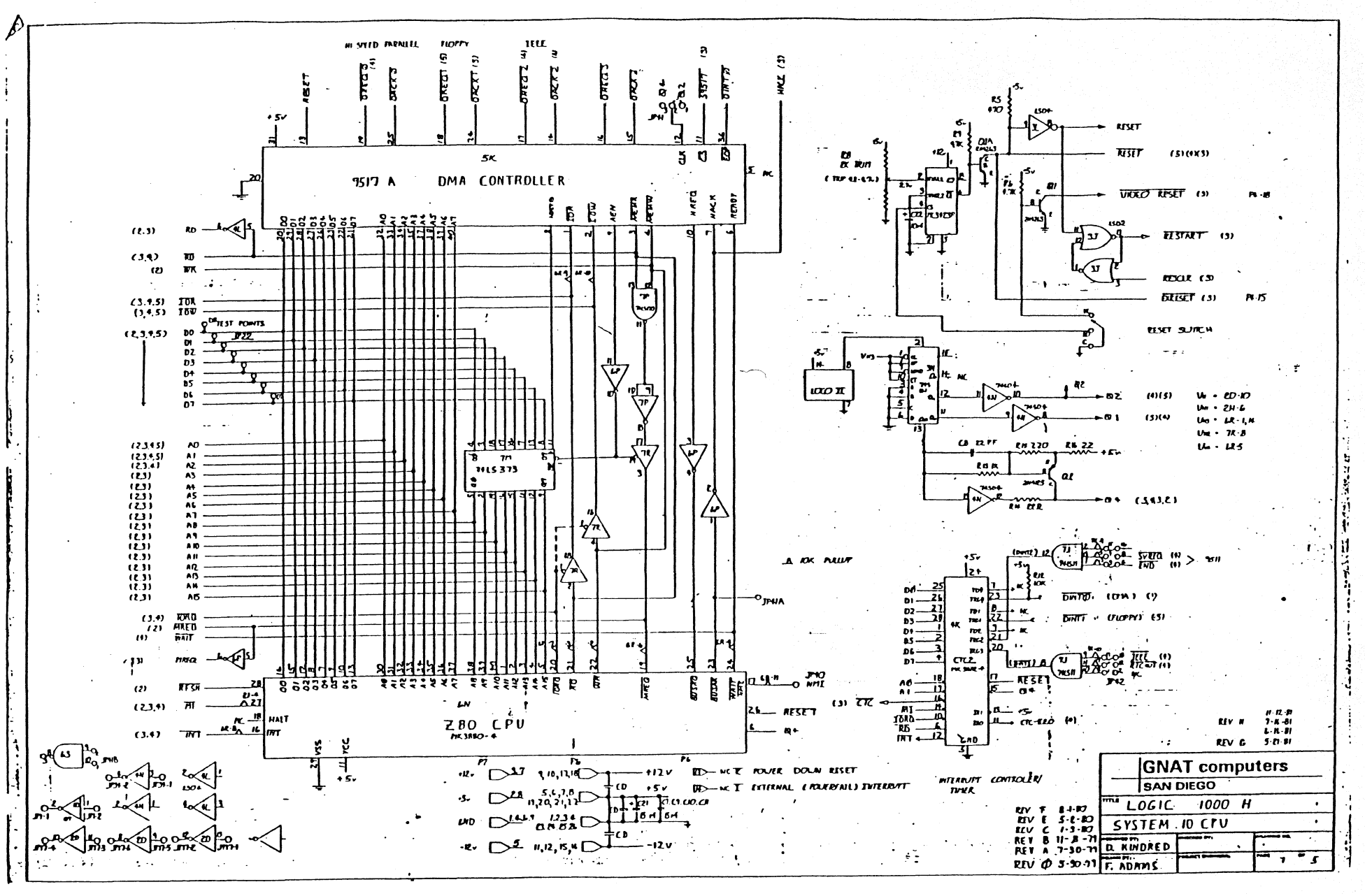
AS1037
AS1038
AS1039
AS1040
AS1041

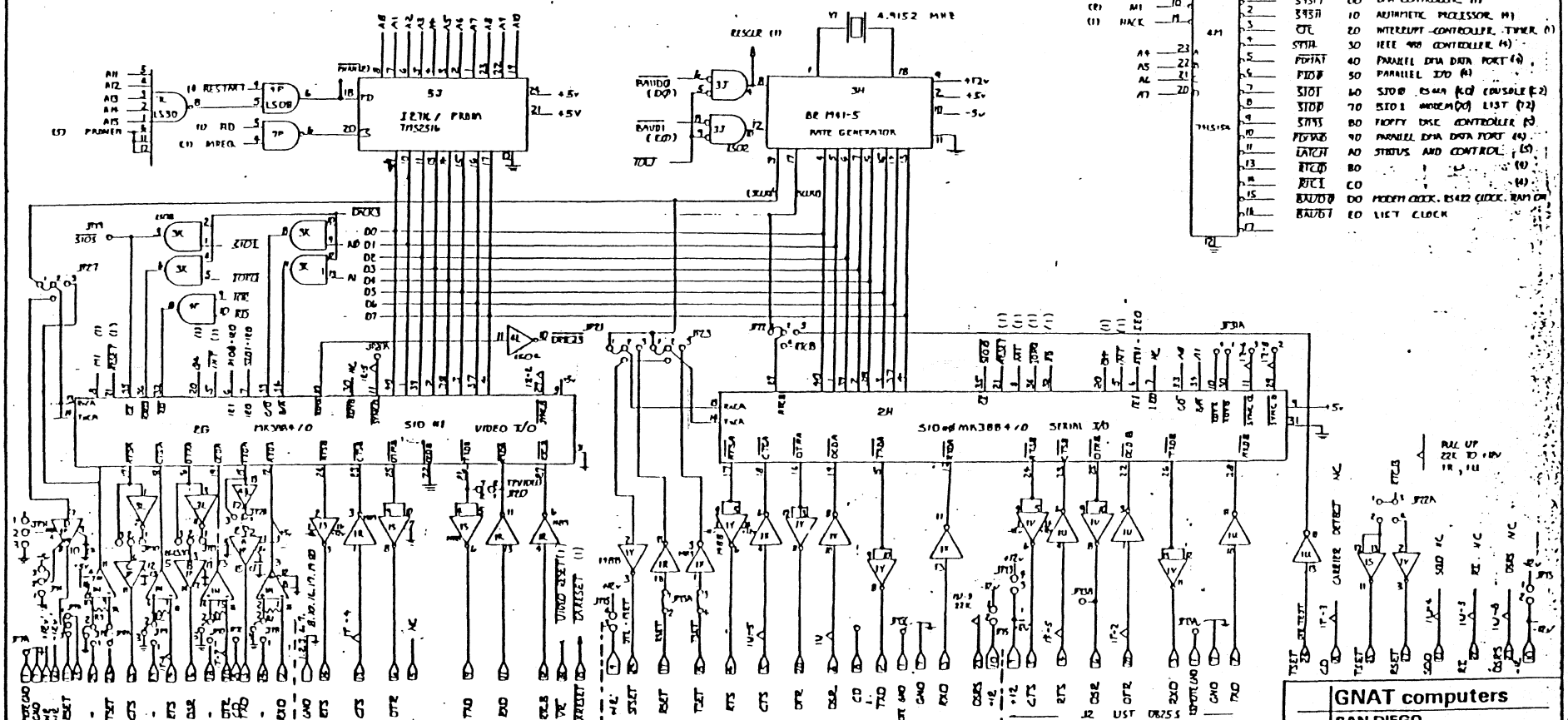

(U-1)
2D
LS04
MI
3F
3E
3C
3G
74F20
3D
74S08
74S00
3A
74F00
3H
74F10
3B
74S244
74S74
74S04
74S20
74S00
74S10
74S08
74S32
74S86
74S00
74S04
74S74
74S244



9517 A DMA CONTROLLER
ZBO CPU
74LS373
INTERRUPT CONTROLLER/ TIMER
RESET SWITCH
LOGO II
POWER DOWN RESET
EXTERNAL (POWERFAIL) INTERRUPT
GNAT computers
SAN DIEGO
LOGIC 1000 H
SYSTEM 10 CPU
D. KINDRED
F. ADAMS

BAUD RATE TABLE			
BYTE	BAUD RATE	BYTE	BAUD RATE
00	50	08	1800
11	75	99	2000
22	110	AA	2400
33	134.5	BB	3600
44	150	CC	4800
55	300	DD	7200
66	600	EE	9600
77	1200	FF	19200

BAUD1 BAUD0 BAUD1 BAUD0



DCE — DATA COMMUNICATION EQUIPMENT
DTE — DATA TERMINAL EQUIPMENT

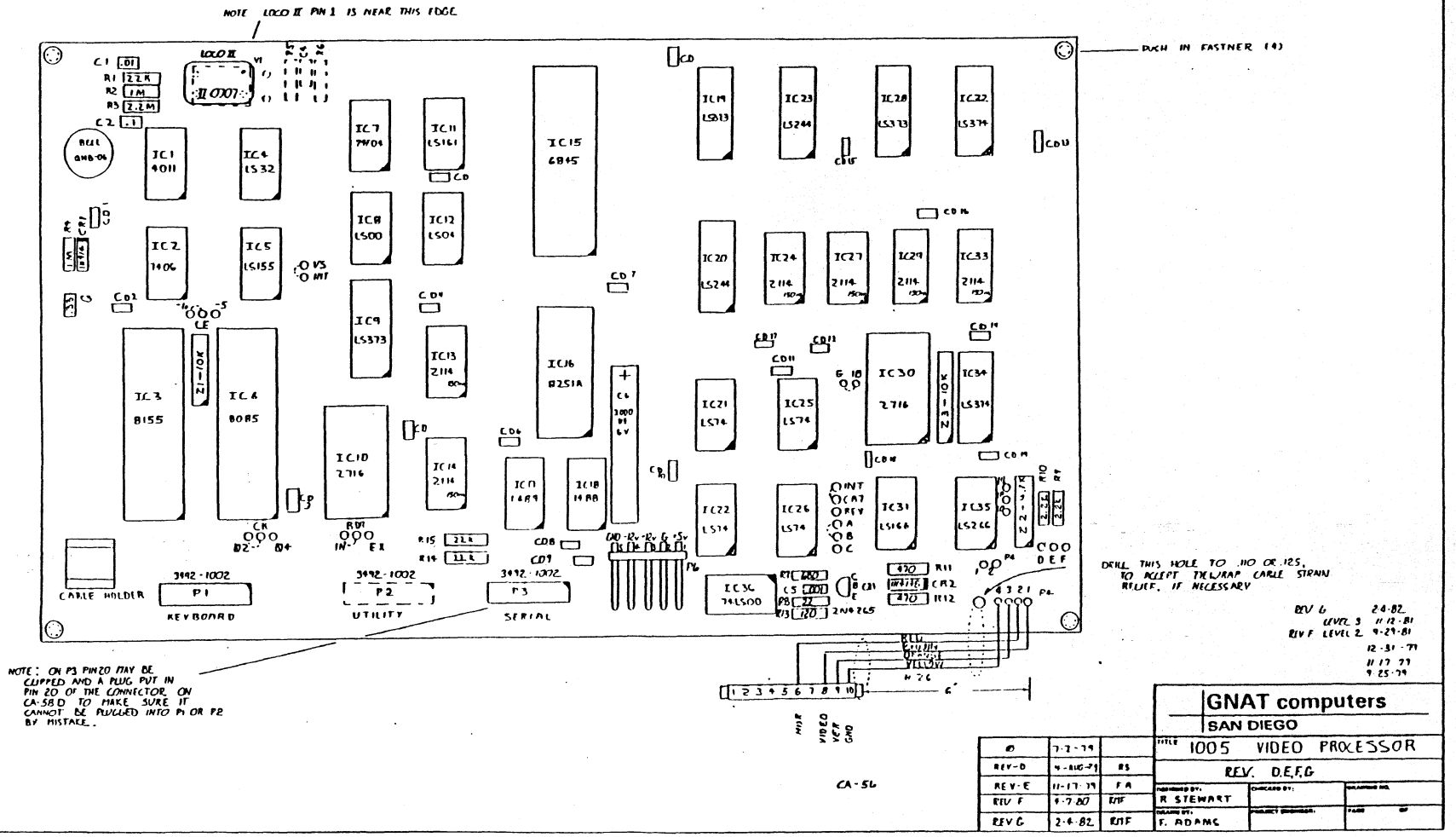
REV D	5-2-80
REV C	1-3-80
REV B	11-8-79
REV E	
REV F	8-1-80

GNAT computers
SAN DIEGO

LOGIC 1000 H
PROM AND SERIAL I/O

D. KINDRED
F. ADAMS

3 of 5



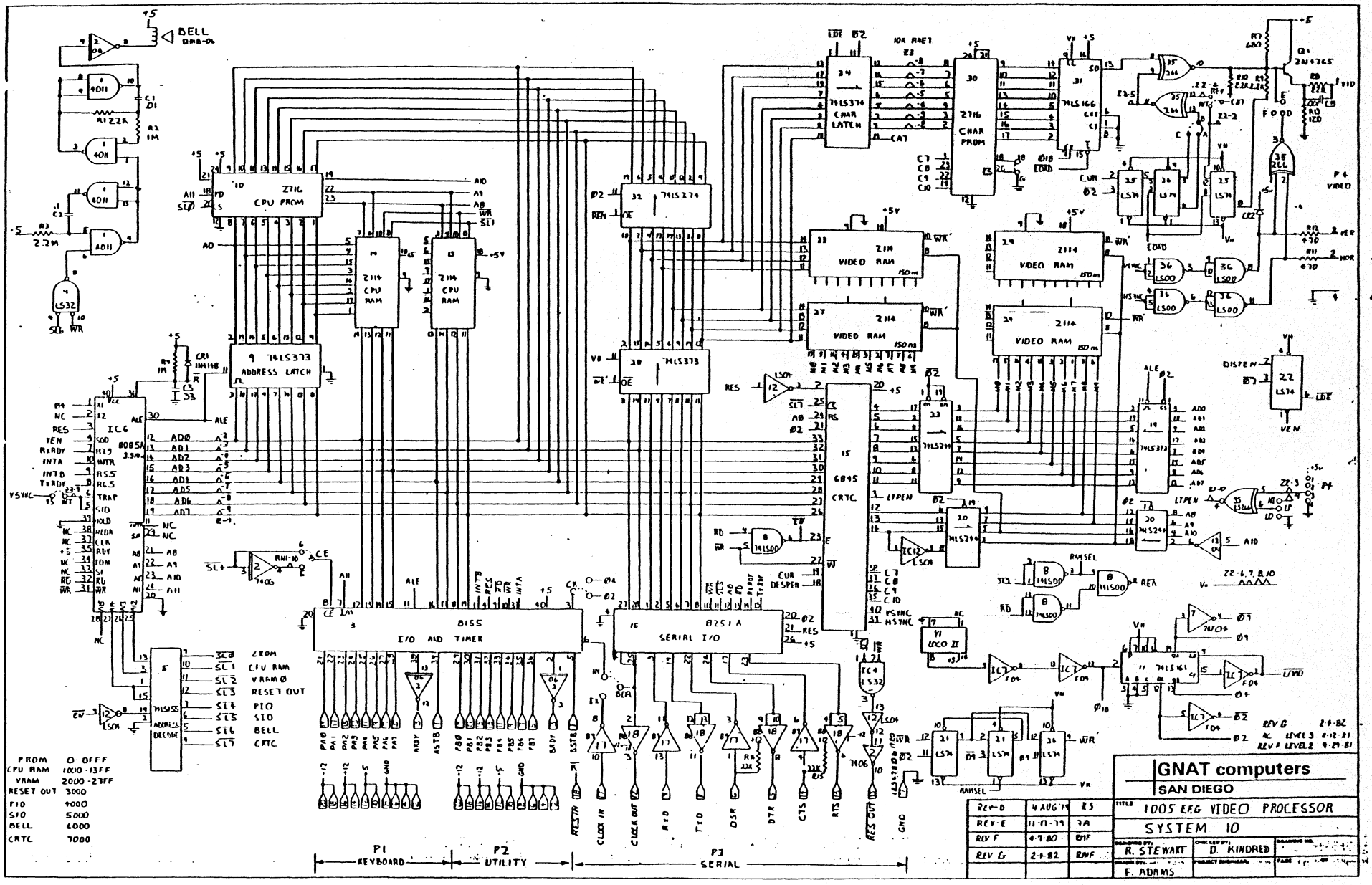
REV G 2-4-82
LEVEL 3 11-12-81
REV F LEVEL 2 9-29-81
12-31-79
11-17-79
9-25-79

ID	7-7-79	
REV-D	4-AUG-79	RS
REV-E	11-17-79	F.A
REV F	9-7-80	RMF
REV G	2-4-82	RMF

GNAT computers
SAN DIEGO

TITLE 1005 VIDEO PROCESSOR
REV. D,E,F,G

DESIGNED BY: R STEWART	CHECKED BY:	DRAWING NO.
DRAWN BY: F. ADAMS	PROJECT ENGINEER:	PAGE OF


BELL
CPU PROM
CPU RAM
ADDRESS LATCH
8085A
8155
I/O AND TIMER
8251A
SERIAL I/O
6845
CRTC
CHAR LATCH
CHAR PROM
VIDEO RAM
VIDEO RAM
VIDEO RAM
VIDEO RAM
P1 KEYBOARD
P2 UTILITY
P3 SERIAL
GNAT computers
SAN DIEGO
1005 REG VIDEO PROCESSOR
SYSTEM 10
R. STEWART
D. KINDRED
F. ADAMS